Christian Wunderl

Front-end for a high voltage DC-DC buck converter

MASTER´S THESIS

Supervised by:

Dipl.-Ing. Dr. techn. Mario Auer

Dipl.-Ing. Slawomir Malinowski

Dipl.-Ing.(FH) Dipl.-Ing. Andreas Hartberger

Institute of Electronics

Technical University Graz

Head: Univ.-Prof. Dipl.-Ing. Dr. techn. Wolfgang Bösch

Diploma Thesis number: 737

2013

Acknowledgments

I wish to thank my parents, who supported me all over the years during my studies.

Furthermore, I wish to thank my supervisors Mr. Slawomir Malinowski, Mr. Andreas Hartberger and Mr. Michael Michelitsch at Dialog Semiconductor and all the other people at Dialog Semiconductor who made this master thesis possible. I wish to thank Mrs. Rocsana Ionescu and Mrs. Olivia Reimer, who have done the main part of the layout for the test chip at Dialog Semiconductor.

I also want to thank my mentor at the Institute of Electronics at the Technical University, Mr. Mario Auer.

Finally, I also thank all my friends and colleagues, who supported me during my studies.

Statutory Declaration

I declare that I have authored this thesis independently, that I have not used other than the declared sources / resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

date	signature

Abstract

Nowadays, DC-DC switching converters (for example a buck converter) are very important. They are a main part of power supply in many devices like a battery charger. Switching converters can reduce an input voltage to a lower output voltage. They can also produce a higher output voltage than the input voltage or invert the polarity.

The efficiency of switching converters can be very high this means that the power losses are small and so it is possible to integrate these converters directly into a microchip. Depending on the application it could be necessary to place external coils and capacitors.

It is a good idea to have a DC input voltage range as large as possible. This is the reason why a front-end for a high voltage DC-DC buck converter was developed that allows a higher DC input voltage than usually. The input voltage range is 5V to 20V and the output voltage range 2.5V to 5V. The maximum output current is 2.5A. The switching frequency is variable because a hysteretic control loop is used.

High voltage NMOS transistors are used for the low-side-switch and for the high-side-switch. To supply the control-blocks for the high-side-switch an active-diode for a bootstrapping [10] supply was designed.

Five different level-shifters were designed from which the low-to-high and the high-to-low level-shifter are especially noteworthy. They also include high voltage transistors and they have to resist the fast alterations of the Lx node.

The front-end was simulated over temperature, supply voltage- and process-variations.

A testchip is fabricated in a 130nm BCD process. The evaluation of the testchip is not part of this master thesis.

Kurzfassung

Heutzutage sind DC-DC Schaltwandler (wie zum Beispiel der Buck-Konverter) sehr wichtig. Sie sind ein Hauptbestandteil für die Energieversorgung in vielen Geräten wie zum Beispiel eines Batterieladegerätes. Schaltwandler können eine gegebene Eingangsspannung auf eine niedrigere Ausgangsspannung reduzieren. Sie können ebenfalls eine höhere Ausgangsspannung als die Eingangsspannung erzeugen oder die Polarität invertieren.

Die Effizienz von Schaltwandlern kann sehr hoch sein, was bedeutet, dass die Leistungsverluste gering sind und die Wandler dadurch direkt in einem Mikrochip integriert werden können. In Abhängigkeit von der Anwendung kann es notwendig sein, externe Spulen und Kondensatoren zu platzieren.

Es ist eine gute Idee, einen möglichst großen DC Eingangsspannungsbereich zu haben. Das ist auch der Grund, warum ein front-end für einen Hochspannungs DC-DC Buck-Konverter entwickelt wurde welches einen größeren DC Eingangsspannungsbereich ermöglicht als normalerweise. Der Eingangsspannungsbereich liegt zwischen 5V und 20V und der Ausgangsspannungsbereich zwischen 2,5V und 5V. Der maximale Ausgangsstrom beträgt 2,5A. Die Schaltfrequenz ist variabel da eine hysteretische Steuerung verwendet wird.

Hochspannungs NMOS Transistoren werden für den Low-Side-Schalter und den High-Side-Schalter verwendet. Zur Versorgung der Steuerungsblöcke des High-Side-Schalters wurde eine aktive Diode für eine Bootstrapping-Versorgung [10] konstruiert.

Fünf verschiedene Pegelwandler wurden konstruiert, von denen der low-to-high und der high-to-low Pegelwandler besonders erwähnenswert sind. Sie beinhalten ebenfalls Hochspannungs Transistoren und sie müssen den schnellen Änderungen des Lx Knotens Stand halten.

Das front-end wurde über Temperatur, Versorgungsspannung- und Prozessschwankungen simuliert.

Ein Testchip wurde mittels einem 130nm BCD Prozess hergestellt. Die Evaluierung des Testchips ist nicht Bestandteil dieser Masterarbeit.

Contents

1. Introduction

1.1. Motivation

Nowadays a lot of power management applications are System-on-Chip (SoC) and they use DC-DC converters instead of linear regulators because they have a much lower power dissipation and higher efficiency for a high voltage drop between input and output voltage. But this is not always possible.

A common input voltage is 12V and for digital circuits this voltage is reduced to 3.3V or less. How are the 3.3V generated? Often this is realized by a linear regulator which has 12V on the input and 5V at the output and these 5V are reduced to 3.3V by a buck converter. A linear regulator has a poor efficiency for these conditions. To develop a DC-DC buck converter which directly converts 12V input voltage to an output voltage of 3.3V or less is a better idea.

1.2. Specification of the project

A Front-end for a high voltage DC-DC buck converter has to be developed in a 130nm BCD process for this master thesis. This contains the following parts [9]:

- Output switches
    - Design of switches using 20V devices with 5V gate oxide
- Drivers
    - Drivers for output switches including level-shifters to be able to work with 5V digital control signals
- Simplified control loop
    - Hysteretic loop for controlling the output voltage level

The goal of the master thesis is to analyse the above listed structures in full detail (research) and to provide a solution for the given problem (finalized design that meets the specification and its verification). Optimization criteria are power consumption and area requirements. Key design parameters are:

- Input voltage: 5V to 20V

- Output current capability: >2A

- Output voltage programmable: 2.5V to 5V

- Low voltage supply: 5V

A test chip will be manufactured but the measurements of this test chip are not part of the master thesis. Also the layout is not part of the thesis so it will be done by Dialog Semiconductor.

2. Theory

2.1. Linear regulators vs. Switching regulators

This part of the thesis refers to books of Robert W. Erickson, Dragan Maksimovic [1] and Ulrich Tietze, Christoph Schenk [10] and to the application note from Chester Simpson [11],[12].

A common way to reduce a voltage is using a linear regulator. Figure 1 shows a simple block diagram of a linear regulator.

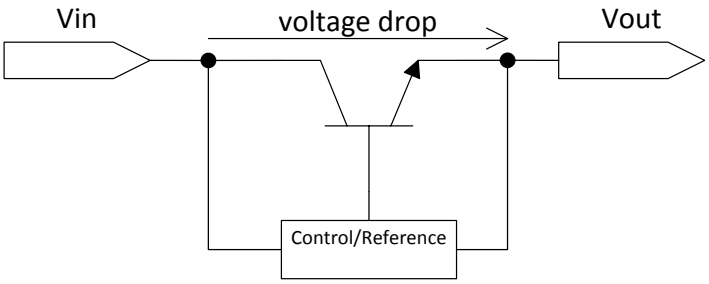

Figure 1 Simple block diagram of a linear regulator [10],[11]

The main component of a linear regulator is the transistor between input (V_{in}) and output (V_{out}). This transistor has losses dependent on the voltage difference between V_{in} and V_{out} (voltage drop). The type of the transistor defines the minimum voltage drop of the regulator. If a PNP transistor is used for the line transistor the linear regulator is called an LDO (Low Drop-Out). Table 1 gives a short overview of some different types [11]:

Transistor type	NPN	Darlington (NPN)	LDO (PNP)
Minimum voltage drop	~ V_{BE} + const.	~ 2x V_{BE} + const.	~ V_{CEsat}

Table 1 Comparison of different linear regulators

It can be seen that the LDO has the smallest voltage drop.

For comparing regulators with each other normally the efficiency η is compared:

$$\boldsymbol{\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out}+P_{losses}} = \frac{P_{in}-P_{losses}}{P_{in}}} \quad (1)$$

The power losses of the linear regulator depend on the voltage difference between input voltage and output voltage and on the load current. These power losses have to be dissipated by the linear regulator which converts the power into thermal energy. If the voltage drop increases the efficiency decreases and this is one of the main disadvantages of a linear regulator. But they can also have a good efficiency under certain conditions (for example at low voltage drop). On the other hand their advantages are simplicity, robustness and reliability.

The other option to change the input voltage is to use a switching regulator or so called DC-DC switching converter. Advantages are a higher efficiency at higher voltage drops and it is also possible to change the polarity of the input voltage (inverting/buck-boost converter) or to increase it (boost-converter) not only to decrease it (buck converter). Disadvantages are the higher complexity of the control loop for regulation of the output voltage [1]. Figure 2 shows a block diagram of a switching regulator.

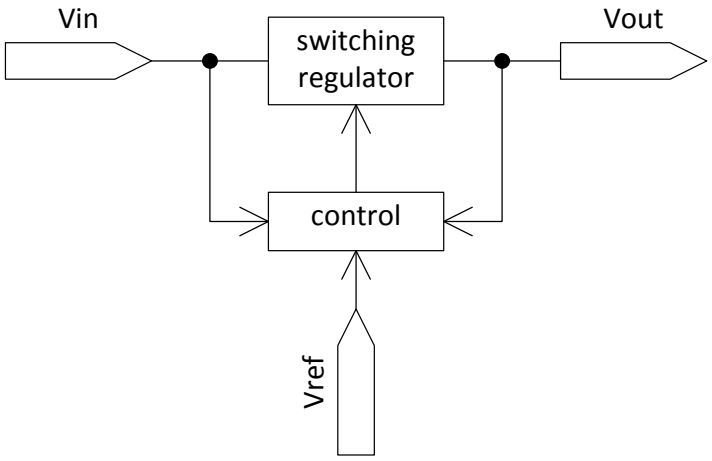

Figure 2 Simple block diagram of a switching regulator [1]

Figure 3 shows the principle of a switching regulator for decreasing the input voltage (buck converter).

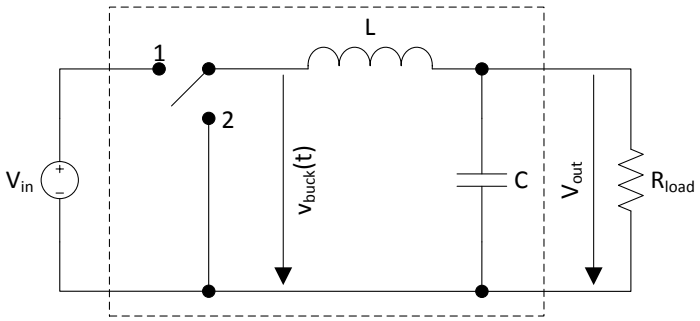

Figure 3 Principle circuit of a buck converter [1]

To understand the general function of the switching converter Figure 4 shows the internal voltage $v_{buck}(t)$ over time.

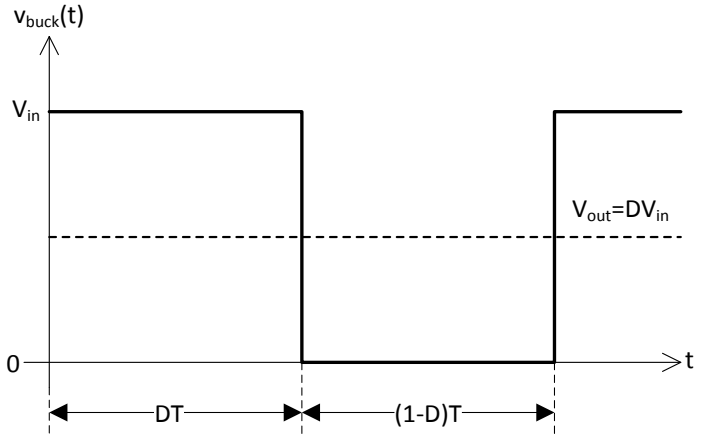

Figure 4 $v_{buck}(t)$ of the buck converter and V_{out} which is the average voltage of it [1]

During the period DT the switch is in position 1 and during the period (1-D)T it is in position 2. D is called ***duty cycle*** and has a range from 0 to 1. The average $v_{buck}(t)$ voltage over many cycles is $V_{in}D$. This averaging process is done by the output L-C filter. The L and C are ideally and lossless components, so no power is dissipated. During the period DT the input voltage supplies the buck converter so that the duty cycle defines the output voltage dependent on the input voltage:

$$V_{out} = V_{in}D \quad (2)$$

DC-DC switching converters also have losses but they are not dependent on the voltage difference between input voltage and output voltage [1]. Considering this it seems to be clear why nowadays DC-DC converters are the preferred regulators. (The losses of the DC-DC converters will be discussed in chapter 2.2.4.)

2.2. The buck converter

This part of the thesis refers to the books of Robert W. Erickson, Dragan Maksimovic [1] and Ned Mohan, Tore M. Undeland, William P. Robbins [5] and to the lecture notes from Richard Redl [4].

A buck converter is one kind of a DC-DC switching converter with the function to reduce a given input voltage. This chapter will give an overview of the function of the buck converter and its losses.

2.2.1. General

In Figure 3 the principle of a buck converter is shown by using an ideal changeover switch (SPDT). Figure 5 shows the buck converter with two switches (SPST).

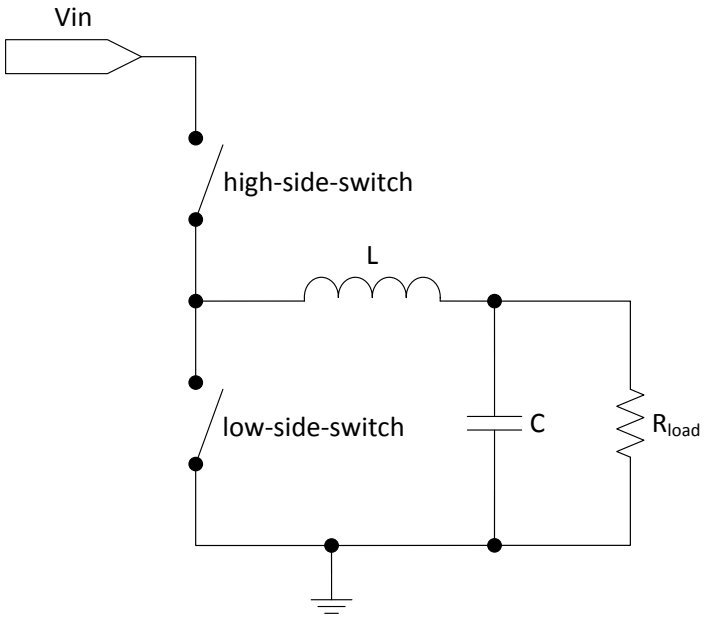

Figure 5 Shows an ideal circuit of a buck converter [1]

There are many possibilities for the realization of the high-side-switch and the low-side switch (together they are called half-bridge). Table 2 gives therefore an abridgement.

High-side-switch	PMOS transistor	NMOS transistor	PMOS transistor	NMOS transistor
Low-side-switch	Diode	Diode	NMOS transistor	NMOS transistor

Table 2 Different possibilities for low-side-switch and high-side-switch

For completeness, a PMOS transistor is not used as a low-side-switch because the costs to generate a negative supply voltage for the gate are too high. Every combination has its advantages and disadvantages. The low-side-switch could be a simple diode or an NMOS transistor. A great advantage of the diode is that it does not need a control logic.

But the advantage of using an NMOS is for example a lower voltage drop over the low-side-switch during its conducting (on) time. A diode has ~600mV voltage drop an NMOS transistor has less. Table 3 shows a small overview of the advantages and disadvantages of using the NMOS transistor as low-side-switch.

Advantages	**Disadvantages**
lower voltage drop → lower conduction losses	higher switching losses
Bidirectional power flow (for example charge/discharge)	extra costs (transistor, control)
CCM is load independent	current limit protection for reverse current

Table 3 Advantages/disadvantages of a transistor as low-side-switch [4]

One important part of this thesis is to find out which switch configuration for the high-side-switch would be the best when using transistors for both switches.

2.2.2. Principle function

Equation 3 describes what Figure 4 shows:

$$V_{out} = \frac{1}{T}\int_0^T v_{buck}(t)\,dt = DV_{in} \quad (3)$$

That is to say the output voltage is the average value of the square wave voltage which supplies the converter ($v_{buck}(t)$). During the time period DT the high-side-switch is conducting (on) and V_{in} supplies the converter ($v_{buck}(t) = V_{in}$). The current flows through the high-side-switch (I_{HSS}) and the coil (I_L). During this period the current through the coil is rising. During period (1-D)T the low-side-switch is on and V_{in} cannot supply the converter ($v_{buck}(t) = 0V$). The current flows through the low-side-switch (I_{LSS}) and the coil. During this period the current through the coil is falling. Figure 6 shows the currents through the coil and both switches during some switching cycles for a settled buck converter in Continuous-Conduction-Mode.

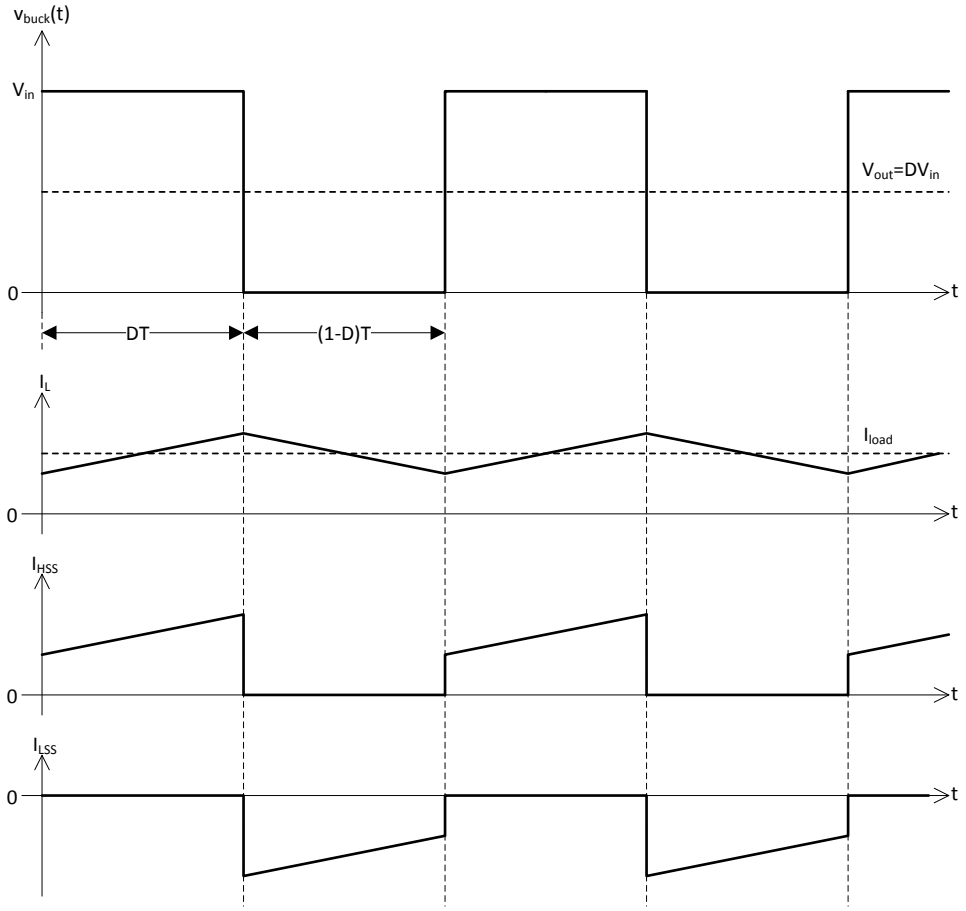

Figure 6 Shows the currents through the coil and both switches of the buck converter

For a duty cycle of 1 (100% of the time the high-side-switch is on) the output voltage will be the same as the input voltage (the losses of the converter are neglected). Figure 7 shows V_{out} over the duty cycle [1].

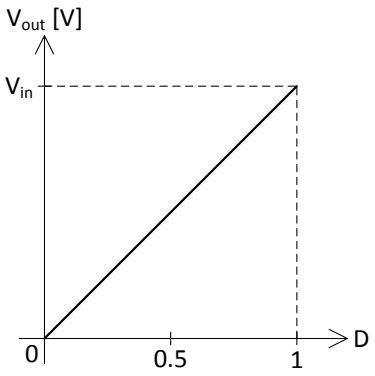

Figure 7 V_{out} vs. duty cycle for an ideal buck converter [1]

2.2.3. CCM and DCM

There are two different operating modes of a buck converter:

- Continuous-Conduction-Mode (CCM)
- Discontinuous-Conduction-Mode (DCM)

In the CCM one switch is always on. This allows a permanent coil current flow as shown in the upper diagram line of Figure 8. By using transistors for both switches the coil current could reach values below zero (negative current) (see lower diagram line).

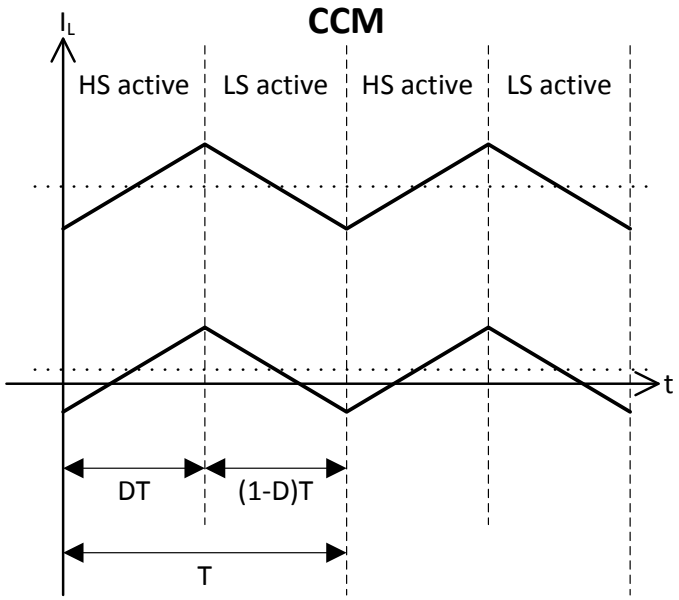

Figure 8 Shows possible coil currents of a buck converter in CCM [4]

During DT the high-side-switch is on; the coil current is rising up until the control logic sets the high-side-switch off and low-side-switch on. During time period (1-D)T the coil current is falling.

If the output current is small or the ripple (see Figure 9) high it happens that the coil current falls to zero or below which involves a negative current in the coil. This is only possible if both switches are realized by transistors. If the low-side-switch is a diode it is not possible that the current through the coil becomes negative. The current will be zero and the buck converter operates in the DCM. There are three states during a period in DCM (see Figure 10).

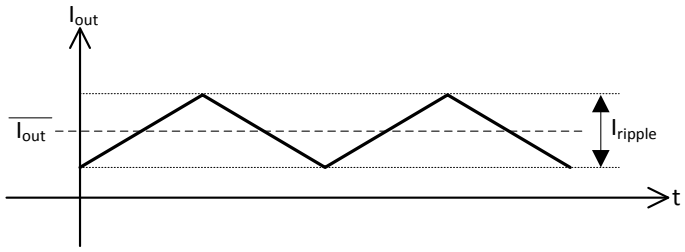

Figure 9 Shows a possible form of a current ripple

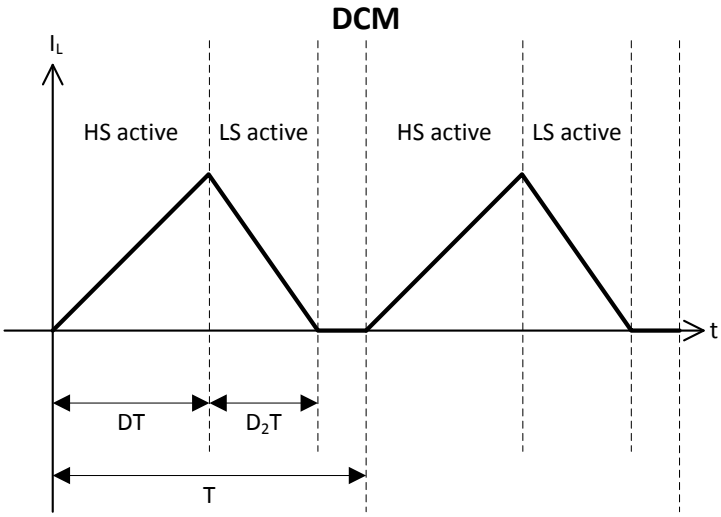

Figure 10 Shows the coil current of a buck converter in DCM [4]

During DT the high-side-switch is on and the current is rising. During D_2T the low-side-switch is on and the current is falling until it reaches zero. Subsequently high-side-switch and low-side-switch are off. This is the 3rd state which continues until the end of the period T.

To prevent a negative current through the coil a diode function of the low-side-switch is necessary because a transistor as low-side-switch allows reverse current. Hence a so called *zero-cross* comparator could be used. Its function is to monitor the current through the coil and to give a signal to the control-logic if the current approaches zero. The control-logic sets both switches off to realize the 3rd state of the DCM. Thus it is also possible to use a buck converter with transistors for both switches in DCM. This topology is called synchronous rectifier [1], [4].

2.2.4. Efficiency and Losses

The efficiency is the most important parameter for comparing different converters and it is also a benchmark for a converter itself. Perfect would be an efficiency of 100% which means that the input power is the same as the output power. But this is not possible because there are losses. The main goal for a designer is to reduce these losses and to reach a high efficiency. The efficiency is already defined in equation 1.

It is necessary to describe the losses of a converter to calculate the real efficiency. There are several losses. The most important losses can be classified as:

1. Coil copper loss
2. Switch conduction loss (R_{ON})
3. Switching losses
4. Constant (fix) losses

Coil copper loss:

A coil has a wire resistance and this resistance is the reason for the copper loss. It is possible to represent this loss by an additional resistor (R_L).

$$P_{R_L} = I_L^2 \, R_L \quad (4)$$

Normally there is information about the resistance value of R_L in the coil datasheet.

Switch conduction loss (R_{ON}):

The switch is realized by a transistor which has a resistance value based on its geometry and V_{GS} (gate-source voltage) in on state. This R_{ON} is the reason for the switch conduction loss.

$$P_{R_{ON}} = I_L^2 \, R_{ON} \quad (5)$$

This equation is only valid for a stable state. Generally a switch is not all the time on. For example the high-side-switch of a buck converter is on only during the part D of a time period. From equation 5 the equation for the high-side-switch (P_{HS}) can be derived:

$$P_{HS} = D \left(I_L^2 \, R_{ON,HS} \right) \quad (6)$$

$R_{ON,HS}$ is the resistance of the high-side-switch in on state. Complementary the equation (P_{LS}) for the power loss of the low-side-switch is:

$$P_{LS} = D' \left(I_L^2 \, R_{ON,LS} \right) \quad (7) \qquad D' = 1 - D \quad (8)$$

$R_{ON,LS}$ is the resistance of the low-side-switch in on state. Conduction losses can be summarized to one term:

$$\Longrightarrow \; P_{conduct} = P_{HS} + P_{LS} \quad (9)$$

Switching losses:

In addition to the conduction loss of a switch there are also losses during switching. During turning on as well as during turning off a switch shows power losses. These losses are depending on the parasitic capacitances of the switch. The switching loss depends on the switching frequency (f_{sw}) and the voltage to which the capacitances are charged. (This voltage is included by the Energy (W) terms see therefore [1] page 93f):

$$P_{switching} = (W_{ON} + W_{OFF})\, f_{switching} \quad (10)$$

$$\Longrightarrow \quad P_{switching} = W_{switching}\, f_{switching} \quad (11)$$

Constant (fix) losses:

The last considerable losses are the constant losses which are necessary for the function of the system (P_{fix}). This includes for example the supply of the control-logic. These losses are independent on the input and output voltage and also on the load. These losses are the reason why the efficiency is zero for an output power equal to zero.

Overall losses:

$$P_{losses} = P_{R_L} + P_{conduct} + P_{switching} + P_{fix} \quad (12)$$

There exists a frequency threshold $f_{critical}$ above which the overall losses are dominated by the switching losses; below this they are dominated by the other losses.

$$f_{critical} = \frac{P_{R_L} + P_{conduct} + P_{fix}}{W_{switching}} \quad (13)$$

Based on this fact it seems to be obvious that it is very important to reduce the switching losses to a minimum to be able to use higher frequencies. Figure 11 shows an example for random values for power losses and load power [1].

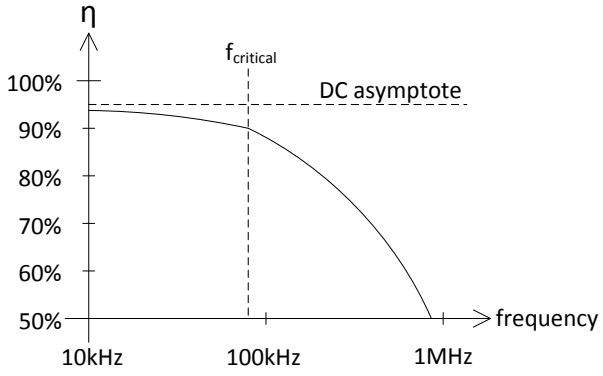

Figure 11 Shows the efficiency vs. switching frequency [1]

2.2.5. Control Loops

To maintain a stable output voltage a control loop is needed. There are basically two variants of control loops:

- Voltage Mode Control (VMC)
- Current Mode Control (CMC)

VMC compares the output voltage with a reference voltage and CMC additional compares the current through the coil or the high side switch with a reference. The important fact is that CMC generally has two control loops (CMC also includes VMC). The advantages and disadvantages of VMC and CMC are listed in Table 4 [4].

Voltage Mode Control		**Current Mode Control**	
Advantages	**Disadvantages**	**Advantages**	**Disadvantages**
single feedback loop	slower response to line or load changes	immediate response to line changes	unstable for duty cycle >50% → compensation necessary
better cross-regulation at multiple outputs	output filter offers two poles → compensation complex	only one pole of interest at the output filter → less complex	two feedback loops
good noise margin	loop gain ∝ input voltage	pulse-by-pulse current limiting is implemented by itself	problems with large current-sense signals → noise, jitter

Table 4 Advantages/disadvantages of VMC and CMC [4]

Table 5 gives an overview of different control mechanism [4].

Voltage Mode Control	Current Mode Control
peak voltage control (const. OFF time)	peak current control (const. frequency; const. OFF time)
valley voltage control (const. ON time)	valley current control (const. ON time)
input voltage feedforward	
const. frequency @ leading edge	
const. frequency @ trailing edge	
const. frequency @ dual edge	
Hysteretic	

Table 5 Different control mechanism for VMC and CMC [4]

The control loop is not the main focus of the thesis. It was decided to use a hysteretic control loop which had to be designed. This specific type will be discussed later in Chapter 3.3.

2.2.6. Sub-Blocks

For design and layout it is important to split up a system into smaller functional parts which can be implemented easier and to have a hierarchical structure for better understanding of the system. The core of the buck converter is the half-bridge which includes the high-side-switch (HSS) and the low-side-switch (LSS). Every switch needs a gate-driver. The reason for this is that the digital signal of a control-logic is not powerful enough to turn a bigger switch on or off fast enough. The half-bridge sub-block additionally contains the gate-drivers (see Figure 12 as an example).

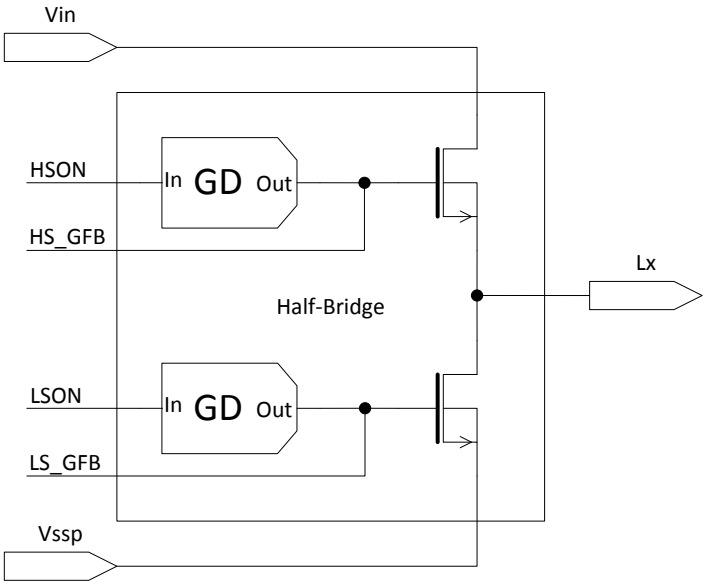

Figure 12 Example for a half-bridge sub-block

For controlling the high-side-switch of the half-bridge it is necessary to control the gate-driver (HSON signal). This involves the usage of a level-shifter (LS-). The control signals are normally in a low-voltage-domain, for example 5V for a *high* signal and 0V for a *low* signal. For the high-side (HS) a low-to-high level-shifter (LS-L2H) is necessary which shifts the control signal from the low-voltage-domain into the high-voltage-domain of the high-side-switch. Vice versa the gate-feedback signal (HS_GFB signal) of the high-side-switch must be shifted from the high-voltage-domain to the low-voltage-domain (LS-H2L). The gate-feedback is important for the control-logic (CL) to make sure that both switches are not turned on at the same time. A Schmitt-Trigger is used as a 1bit analog to digital converter for the HS_GFB signal. The digital HS_GFB signal is then shifted by the high-to-low level-shifter into the low-voltage-domain.

A Schmitt-trigger is able to have different threshold-values for the rising- and falling-edge. This generates a hysteresis which an inverter does not have. The Schmitt-trigger sets its output already to logical high when the HS_GFB signal is higher than the threshold voltage of the high-side-switch (upper threshold voltage of the Schmitt-trigger). Of course it is necessary to know the threshold voltage of the. Likewise the lower threshold voltage of the Schmitt-trigger which sets the output to logical low should guarantee that the transistor is off. This is a nice benefit of the Schmitt-trigger but more important is that the hysteresis guarantees that the output of the Schmitt-trigger does not change if there is only a small change at the input. This is one reason for using a Schmitt-trigger. Another is that the control-logic should directly get a valid logic level.

During the rising of the output voltage from the gate-driver (→ input of the Schmitt-trigger) it happens that the voltage drops once for a short time period (see Figure 13). This voltage drop is due to the Miller-effect [14] and sometimes called the *Miller-plateau*. It could change the output of an inverter but the hysteresis of the Schmitt-trigger prevents an output change.

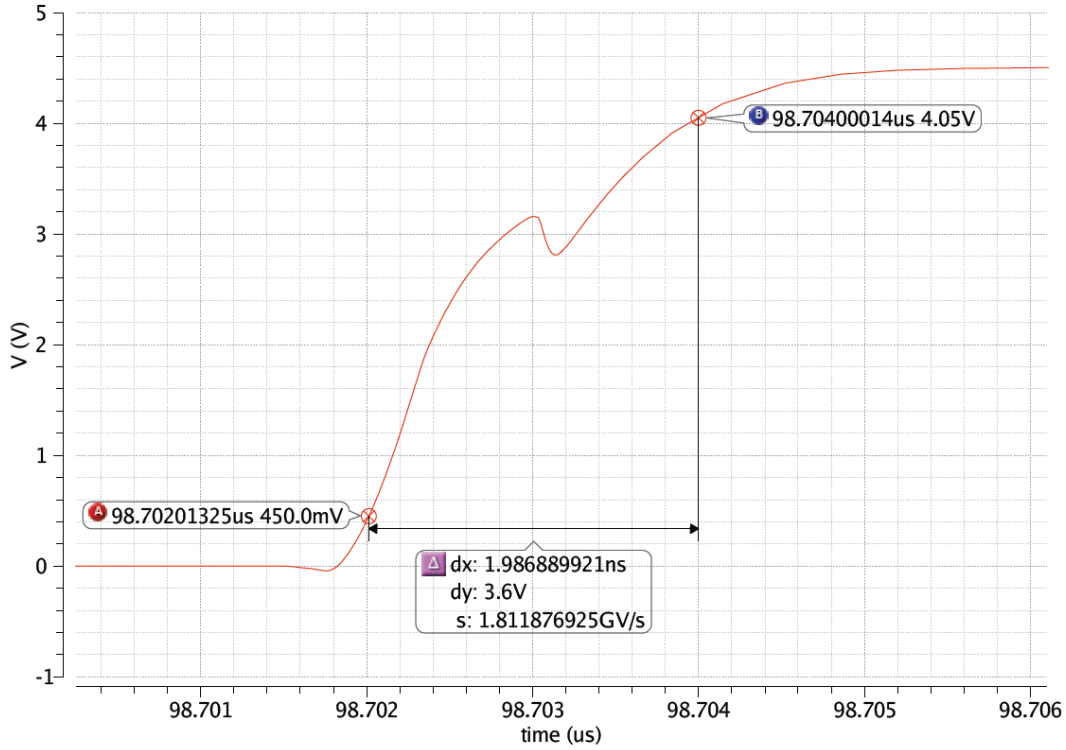

Figure 13 Shows rising of the output voltage from the gate-driver. The Miller-plateau can clearly be seen.

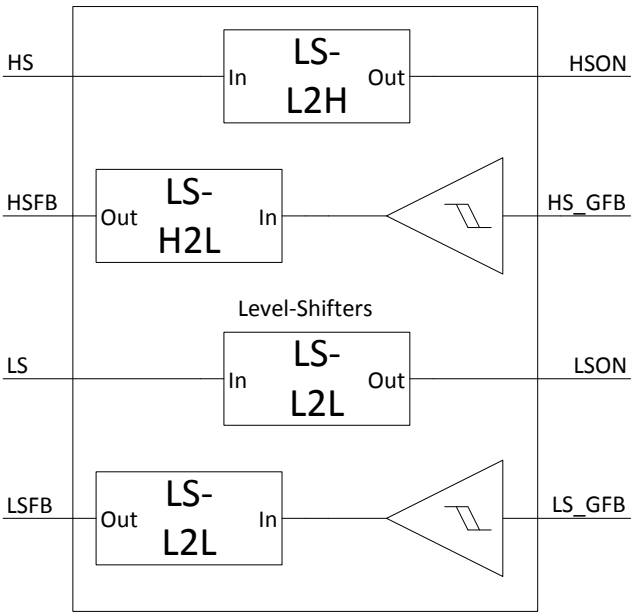

Figure 14 Shows a level-shifters and Schmitt-trigger sub-block

Also for the low-side (LS) it is advantages to use level-shifters to separate the noisy and powerful switch side from the digital side. To achieve this it is enough to use low-to-low level-shifters (LS-L2L) because the voltage difference between these two sides is small. In Figure 14 the level-shifters-block is drawn.

Another sub-block is the power supply for the high-voltage-domain. Depending on the topology of the half-bridge different solutions exist for this block.

Transistor type for HSS	**Vdd of the high-voltage-domain (Vddh) [V]**	**Vss of the high-voltage-domain (Vssh) [V]**	**Possible supply solution**
NMOS	5V / V_{in} + 5V	0 / V_{in}[1]	bootstrapping, charge-pump [14]
PMOS	V_{in}	V_{in} – 5V	LDO

Table 6 Overview of the different high-voltage-domains supply voltages

Table 6 shows that the voltage difference between Vddh and Vssh is the same like for Vdd and Vss. For a PMOS as HSS the Vdd is shifted from 5V to V_{in} and Vss from 0V to V_{in}–5V. For an NMOS transistor as HSS the supply voltages change during one switching cycle because Vssh is the voltage from the Lx node. While the HSS is turned on the voltage at the Lx node is V_{in} by neglecting the conduction loss of the HSS. While the LSS is turned on the voltage at the Lx node is 0V by neglecting the conduction loss of the LSS. The function of the block is to supply the gate-driver, the low-to-high level-shifter, the Schmitt-trigger and the high-to-low level-shifter in the high-voltage-domain. In chapter 3.8 is a more detailed description of this block referenced to the topology which is used.

Another sub-block is the comparator-feedback (CMPs_FB) block which includes the feedback divider and also the comparator for the control loop. This is the analog part of the control system.

The feedback divider divides the output voltage to a value around 1.25V because this is a common reference voltage (V_{ref}) which is normally provided by a bandgap voltage reference. Thus it is possible to define the output voltage chosen by the values for the feedback divider and the reference voltage.

[1] For an NMOS transistor as HSS the LX node is Vssh. The Lx node is switching between 0V (LSS is on) and V_{in} (HSS is on) (the losses of both switches are neglected).

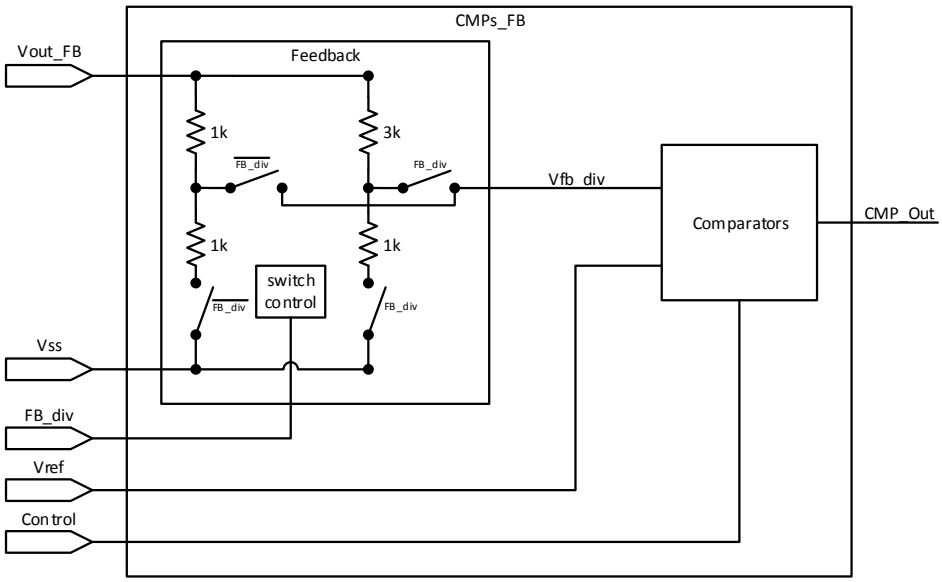

Figure 15 Shows a principle block for the feedback and the control loop comparator

In Figure 15 a principle CMPs_FB block is drawn. The comparator is depending on what type of control loop will be implemented. This is discussed in detail in chapter 3.3. The output signal of the comparator connects to the digital part of the control system; the control-logic (CL) sub-block.

The control-logic provides the control signals of the high-side-switch and the low-side-switch. Its task is to prevent a short circuit over both switches. Therefore it needs the HSFB- and LSFB-signal to check the actual states of the transistor gates. An example will explain it:

The high-side-switch is on and the low-side-switch is off. Now the CMP_Out signal changes from logical high to low which means the high-side-switch has to turn off and the low-side-switch has to turn on. The control-logic sets the HS-signal to low but there is a delay until the moment the high-side-switch is off due to the level-shifter and the gate-driver.

So the control-logic has to wait until the HSFB-signal is also low, which means that the high-side-switch is really off, to prevent a short circuit before it sets the LS-signal to high. After a delay also the LSFB-signal will rise up to high and the control-logic waits for a change of the CMP_Out signal. When the CMP_Out signal changes back to high the control-logic sets the LS-signal to low. Now it has to wait until the LSFB-signal changes to low before it sets the HS-signal to high and the process begins again.

The example assumes that the buck converter works in CCM. In chapter 2.2.3 the terms CCM, DCM and zero-cross comparator were already explained. A zero-cross comparator will not be used for the thesis. This means the buck converter will work consistently in CCM and a negative current is allowed.

Another sub-block is the c*urrent-bank*. Its function is to provide all bias currents which are necessary for the function of the other blocks. Bias currents are not shown in the block diagrams. They are only shown in the transistor level schematics. Only in schematics they will be drawn. In Figure 16 an example of a current-bank is drawn.

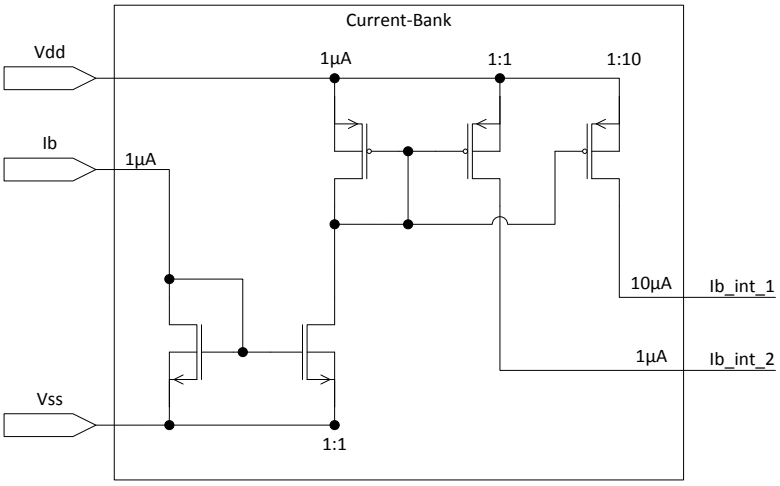

Figure 16 Shows an example for a current-bank

3. Implementation of the high voltage front-end

3.1. Process information

The used process is a 130nm BCD triple well process. This means there is the possibility to use high voltage (HV) transistors and low voltage (LV) isolated NMOS transistors. Table 7 shows the transistors and their parameters which are available for the design.

Transistor type	**|Vgs|**	**|Vds|**	**|Vbs|**	**|Vth|**
LV 5V isolated NMOS	0~5V	0~5V	0~5V	0.873V @ L=600nm
LV 5V PMOS	0~5V	0~5V	0~5V	0.85V @ L=500nm
HV 20V NMOS	0~5V	0~20V	0V	1.51V
HV 36V NMOS	0~5V	0~36V	0V	1.55V
HV 28V PMOS	0~5V	0~28V	0~5V	1.09V

Table 7 Useable transistors in a 130nm BCD process

The HV NMOS transistors and also the HV PMOS transistor have a fixed gate length. The HV NMOS transistors have a gate length of 800nm and the HV PMOS transistor has a gate length of 600nm. As Table 7 shows the bulk-source voltage of the HV NMOS transistors is zero. The reason for that is a short circuit between the bulk- and source-contact which is a characteristic of the used process. The HV transistors and the isolated LV NMOS transistor have substrate connections. For clear schematics this substrate connections are not sketched in the figures. Also the isolation contact of the LV NMOS transistor is not sketched. For the half-bridge Dialog Semiconductor decided to use the 20V HV NMOS transistor or the 28V HV PMOS transistor. Also Dialog Semiconductor decided to set the finger width of the HV transistors to 48µm. This decision is based on experience from other projects.

3.2. Topology analysis

One of the main goals of this thesis is to find out which Half-Bridge topology is the best for the given specifications. The possibilities were already introduced in chapter 2.2.1. It is necessary to have a closer look on these topologies and to compare them. Hence it is necessary to make estimations for losses and area consumption. There are mainly two topologies:

1. high-side-switch: PMOS low-side-switch: NMOS
2. high-side-switch: NMOS low-side-switch: NMOS

For completeness and to have a comparison

3. high-side-switch: PMOS low-side-switch: PMOS

is also analysed. Figure 17 shows the half-bridges for the different topologies.

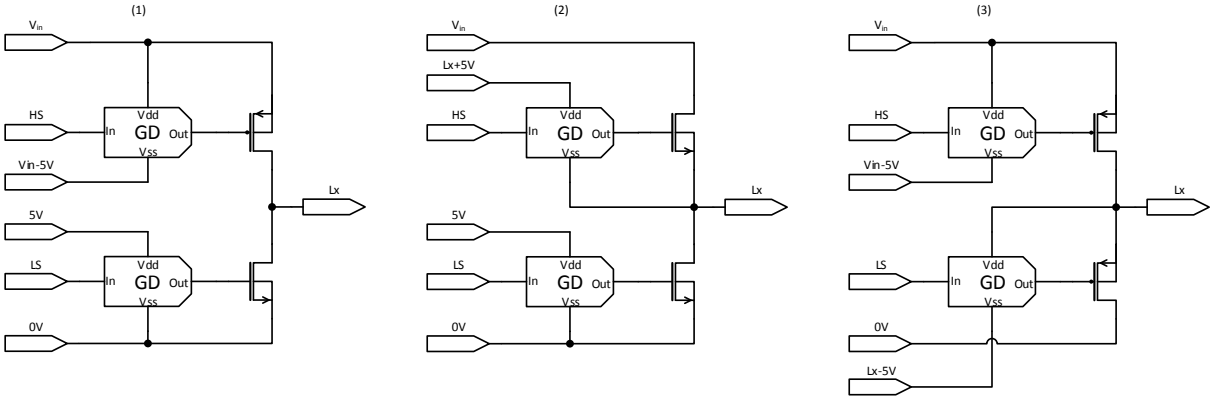

Figure 17 Shows the half-bridges for the different topologies: (1) PMOS for HSS, NMOS for LSS (2) NMOS for both switches (3) PMOS for both switches

For the calculation the power losses will be estimated by:

$$P_{losses} = P_{HS} + P_{LS} + P_{R_L} + P_{drivers} \quad (14)$$

P_{HS} and P_{LS} are the conduction losses of the high-side- and low-side-switch. P_{RL} is the coil copper loss and $P_{drivers}$ are the losses from the Gate-Drivers of both switches.

$$P_{HS} = (D\ I_L)^2\ R_{ON_{HS}} \quad (15) \qquad P_{LS} = (D'\ I_L)^2\ R_{ON_{LS}} \quad (16)$$

$$P_{Rl} = I_L^2\ R_L \quad (17) \qquad P_{drivers} = I_{drivers}\ V_{dd} \quad (18)$$

$$I_{drivers} = I_{driver_{HS}} + I_{driver_{LS}} \quad (19)$$

$$P_{in} = I_{in}\,V_{in} + I_{dd}V_{dd} \quad (20) \qquad I_{in} = D\,I_L;\;\; I_{dd} = I_{drivers} \quad (21)$$

The total input power P_{in} is the sum of all powers which are necessary for the function of the buck converter. The power consumption of the buck converter is mainly given by the losses of the gate-drivers. The link between input power, output power and losses power is very close:

$$P_{loss} = P_{in} - P_{out} \quad \rightarrow \quad P_{in} = P_{out} + P_{loss} \quad (22)$$

For the analysis it is necessary to choose R_{ON} values for both switches because this will affect the silicon area of the switches. For the chosen resistances it is necessary to make estimations for the gate-driver current consumptions. Therefore simulations with different R_{ON} values for the 20V HV NMOS transistor and the 28V HV PMOS transistor are done. Figure 18 shows the test-bench for the first simulation. The results of this simulation are the V_{DS} of the transistors for an I_{DS}=2.5A. The result of the second simulation (see Figure 19 for test-bench) is the electric charge which the gate of the transistor needs to turn on. Therefore the gate current was integrated over time. Also an estimation for the gate capacitance C_G by the parameter c_{gg}[2] is provided (for the DC operating point of the test-bench in Figure 19 @V_{GS}=5V). Table 8 shows the results of the simulations.

Note: All simulations are done in Cadence 6. If there is no additional information the simulations are done in the typical corner with the following parameters:

- temperature: 27°C
- active.scs: tt
- passive.scs: pass_nom

The reason for a typical simulation of the transistors is to save silicon area. To guarantee a specified R_{ON} for all corners the transistor will be larger than for the typical corner. The functionality will be given for all corners if the transistor is designed for the typical corner but the efficiency will be worse for some corners.

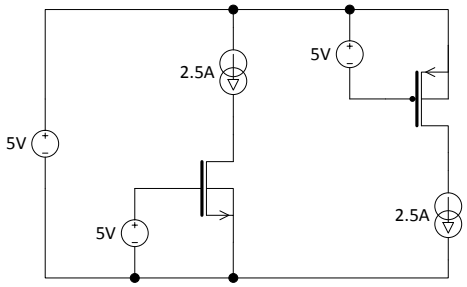

Figure 18 Test-bench for simulation of V_{DS}

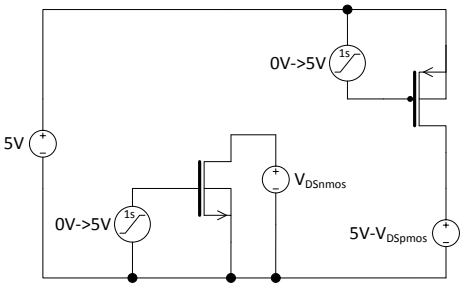

Figure 19 Test-bench for simulation of Q and C_G

[2] c_{gg} is given by dQ/dV_{gate}

Transistor type	finger width [µm]	number of fingers	multiplier	R_{ON} [mΩ]	V_{DS} [mV]	Q [nC]	C_G [pF]
20V HV NMOS	48	202	3	201.1	502.7	0.295	71.25
28V HV PMOS	48	270	10	200.3	500.7	2.216	516.2
20V HV NMOS	48	190	6	102.3	255.7	0.564	134.04
28V HV PMOS	48	290	18	101.6	254.1	4.334	998.28
20V HV NMOS	48	190	12	50.11	125.3	1.138	268.2
28V HV PMOS	48	292	36	50.01	125	8.78	2010.6

Table 8 Electric charge and gate capacitance for different values of R_{ON} of the HV transistors

It can be seen that the difference between the electric charges of the HV NMOS transistor and the HV PMOS transistor for nearly the same R_{ON} is approximately a factor of 7.5.

Table 9 gives an overview for the different values of R_{ON} of the switches and the related gate-driver average current consumptions for one period at a switching frequency of 3.3MHz (T=300ns). The gate-driver current consumptions are derived from the electric charges of the transistors. This derivation is explained in chapter 3.5.

High-side-switch	Low-side-switch	$R_{ON_{HS}}$	$R_{ON_{LS}}$	$I_{driver_{HS}}$	$I_{driver_{LS}}$	$I_{drivers}$
HV PMOS	HV PMOS	100mΩ	100mΩ	14.5mA	14.5mA	29mA
HV PMOS	HV NMOS	100mΩ	100mΩ	14.5mA	1.9mA	16.4mA
HV NMOS	HV NMOS	100mΩ	100mΩ	1.9mA	1.9mA	3.8mA
HV PMOS	HV PMOS	200mΩ	200mΩ	7.4mA	7.4mA	14.8mA
HV PMOS	HV NMOS	200mΩ	200mΩ	7.4mA	1mA	8.4mA
HV NMOS	HV NMOS	200mΩ	200mΩ	1mA	1mA	2mA

Table 9 R_{ON} of the transistors and the related gate-driver currents (rounded values)

A higher resistance of the transistor implies a lower current consumption of the Gate-Driver because the geometry of the transistor is smaller. Therefore also the parasitic capacitances which have to be charged are smaller. But the conduction loss will be greater. Table 10 shows the remaining parameters for the calculations.

$\mathbf{R_L}$	$\mathbf{V_{in}}$	$\mathbf{V_{out}}$	**D**	$\mathbf{V_{dd}}$
11mΩ[3]	5V	3.7V	0.74	5V

Table 10 Parameters for the topology analysis calculations

An input voltage of 5V and an output voltage of 3.7V are very common values e.g. battery charging.

The main goal is the comparison of the three topologies and this should be possible with the chosen parameters and losses. There are also losses from e.g. the level-shifter or other sub-blocks but they should be the same for every topology because of this they can be neglected for the comparison.

In Figure 20 and Figure 21 the results of the calculations are plotted by using equations 14 and 20 in equation 1 with the values from Table 9 and Table 10. All curves start in the origin because for a current load of zero the efficiency is also zero:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{0}{0 + P_{loss}} \xrightarrow{P_{loss}>0} \eta = 0$$

[3] A 1µH coil is used which has a R_L=11mΩ according to datasheet.

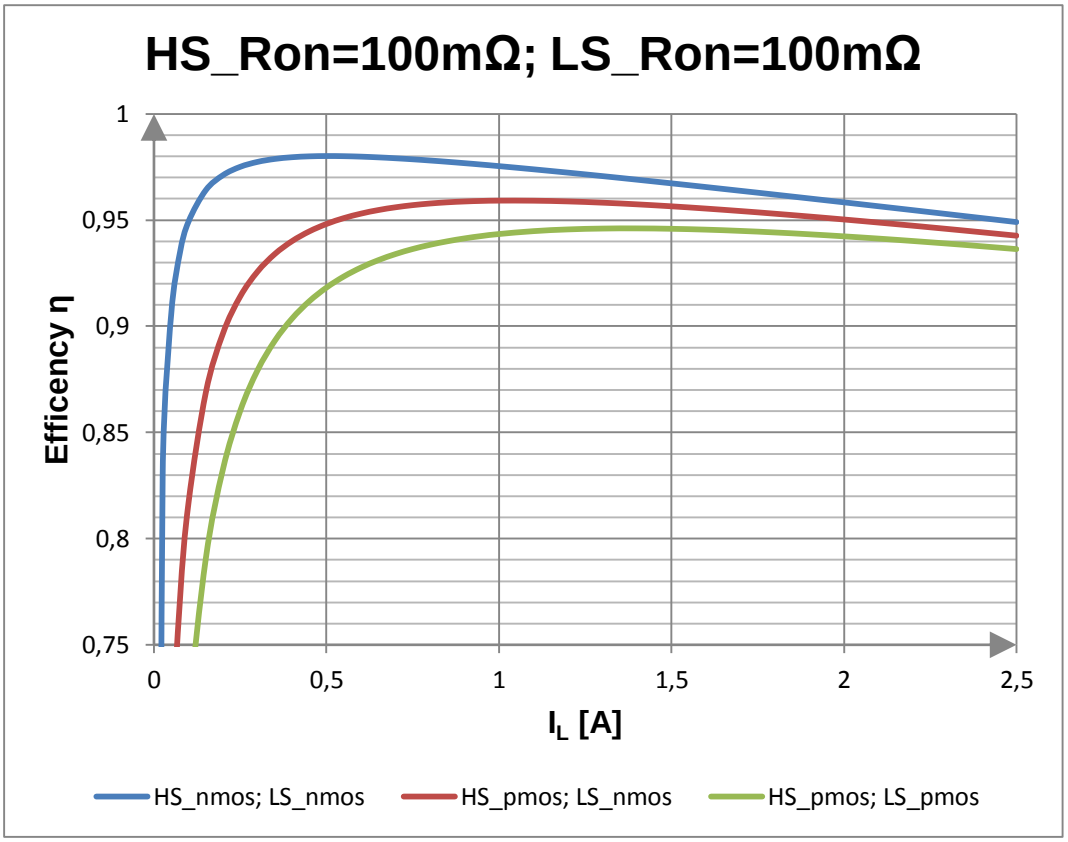

Figure 20 Results of the efficiency calculation for R_{ON}=100mΩ for both switches

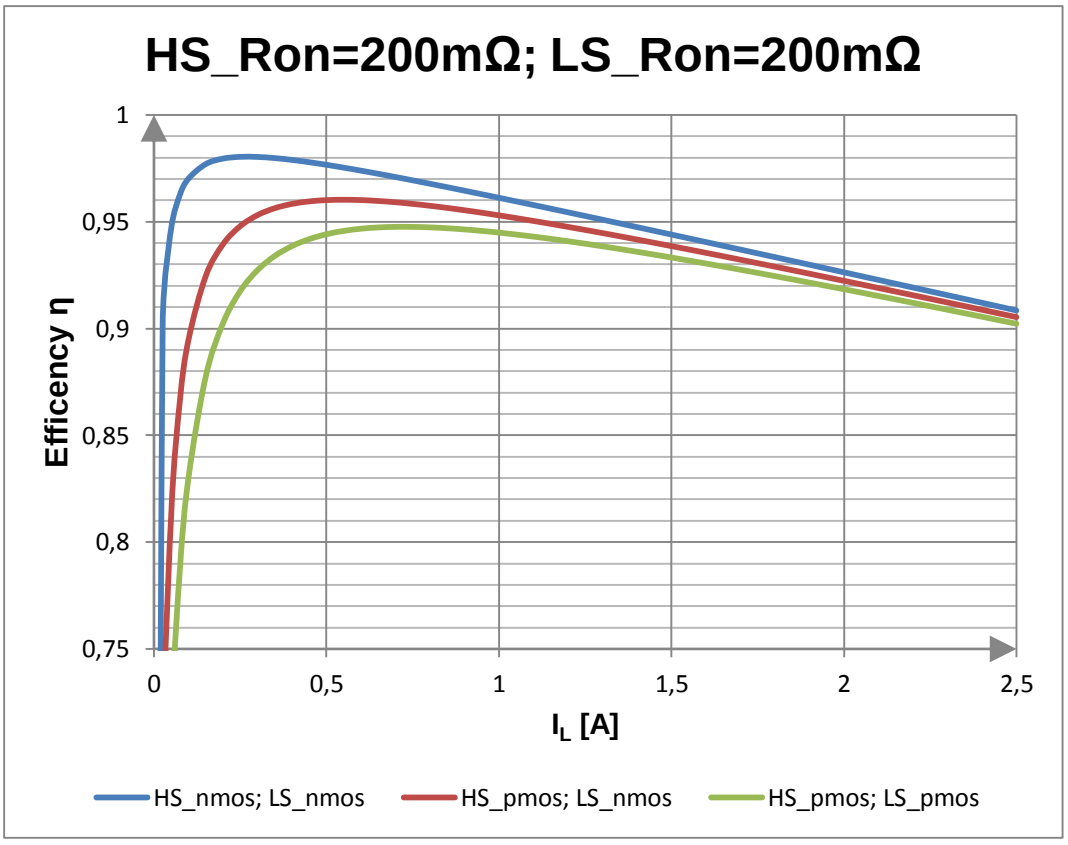

Figure 21 Results of the efficiency calculation for R_{ON}=200mΩ for both switches

As a result it is possible to say that the light load efficiency is better when the R_{ON} of the switches is higher. This is clear because then the losses of the gate-drivers are smaller. But with increasing coil current the losses of the switches increases and at a specific moment they dominate the efficiency. Because of this fact the efficiency for high loads is better for a lower R_{ON}. More interesting is the fact that both figures show that the topology with HV NMOS transistors for both switches has a better efficiency characteristic then the other topologies. It is necessary to say that the difference between the efficiency characteristics shrinks with increasing coil current. Also the difference increases for decreasing the R_{ON}. The losses of the switches depend on the conducting time of each switch. This means for the common case that the high-side-switch is turned on for 74% of one switching period. To improve the efficiency it is necessary to decrease the R_{ON} of the switches. The high-side-switch is dominating so it is a good idea to decrease only the R_{ON} of the high-side-switch. Equation 23 shows the optimal ratio between the R_{ON} of both switches.

$$\frac{\mathrm{R_{ON_{HS}}}}{\mathrm{R_{ON_{LS}}}} = \frac{D'}{D} \quad (23)$$

Table 11 shows the values for the calculation for a smaller R_{ON} of the high-side-switch and Figure 22 the results.

High-side-switch	**Low-side-switch**	$\mathbf{R_{ON_{HS}}}$	$\mathbf{R_{ON_{LS}}}$	$\mathbf{I}_{driver_{HS}}$	$\mathbf{I}_{driver_{LS}}$	$I_{drivers}$
HV PMOS	HV PMOS	50mΩ	100mΩ	29.3mA	14.5mA	43.8mA
HV PMOS	HV NMOS	50mΩ	100mΩ	29.3mA	1.9mA	31.2mA
HV NMOS	HV NMOS	50mΩ	100mΩ	3.8mA	1.9mA	5.7mA

Table 11 Gate-driver currents for R_{ON}=50mΩ for HSS and R_{ON}=100mΩ for LSS

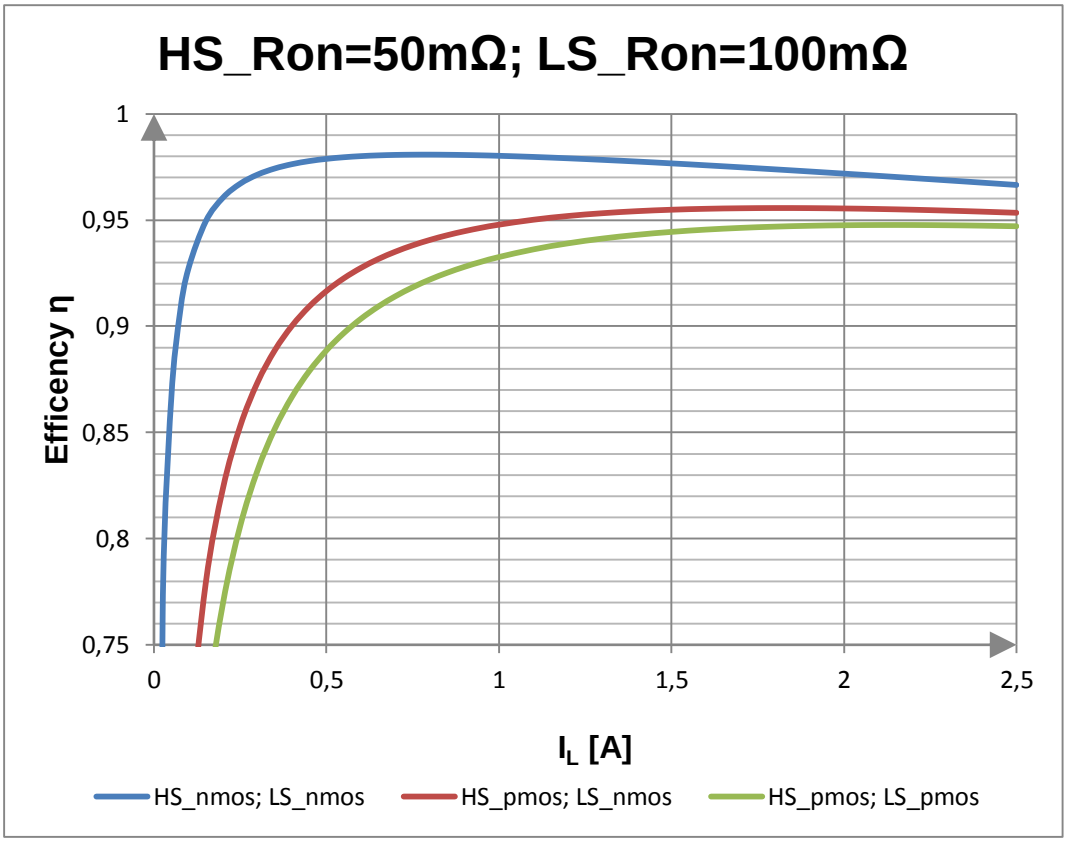

Figure 22 Results of the efficiency calculation for different values of R_{ON} for HSS and LSS

As Figure 22 shows the characteristics are improved. The fall off is lower and it can be seen that the difference between the characteristics is higher than for the previous calculations. Table 11 shows that the total gate-drivers current consumption of the topology with HV NMOS transistors for both switches is less than for one HV PMOS transistor with an R_{ON}=100mΩ. As a first conclusion it is possible to say that the topology with HV NMOS transistors for both switches is the best choice.

To confirm this conclusion Figure 23 shows the silicon area estimation of a 28V HV PMOS and a 20V HV NMOS transistor for an R_{ON}=100mΩ. Table 12 shows the parameters.

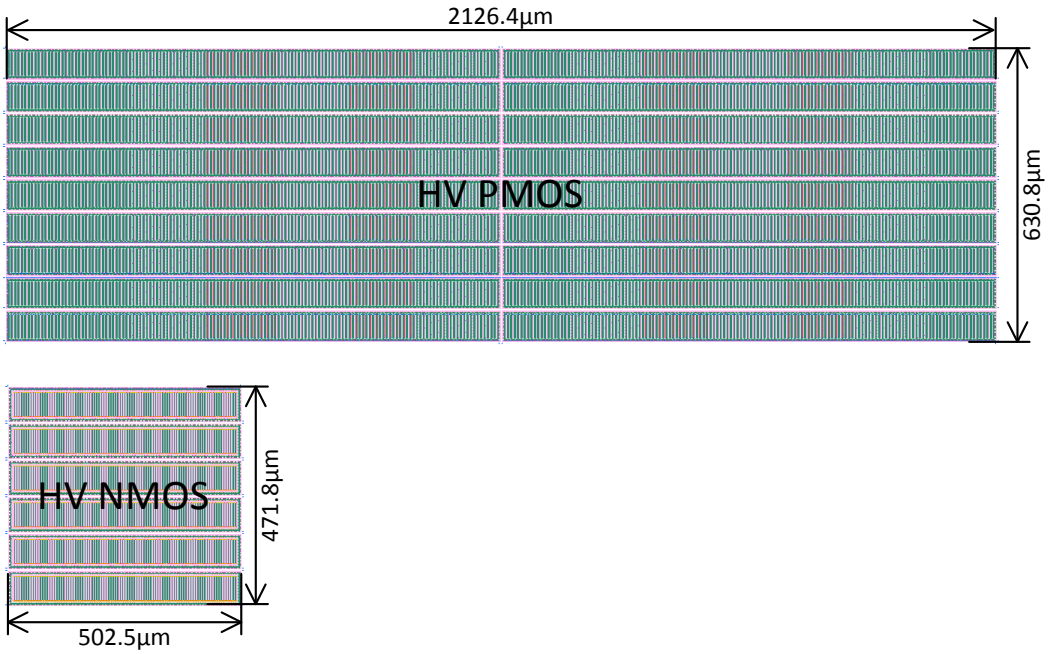

Figure 23 Silicon-area of HV PMOS transistor and HV NMOS transistor

Transistor	Length (L) [nm]	Width (W) [mm]	L.W [mm²]	Silicon area [mm²]
HV NMOS	800	54.27	~0.044	~0.24
HV PMOS	600	250.56	~0.150	~1.34

Table 12 Areas of the HV PMOS transistor and the HV NMOS transistor

The silicon area is not the same as the area by multiplication of length and width of the transistor. The reason is that length and width are only describing the area of the gate from a transistor.

Table 12 shows that the silicon area scale factor between the HV PMOS and the HV NMOS transistor is approximately 5.5. Considering the fact that the topology with HV NMOS transistors for both switches and smaller R_{ON} for the high-side-switch needs three times a HV NMOS transistor with R_{ON}=100mΩ for the half-bridge the whole half-bridge would be smaller than one HV PMOS transistor with a R_{ON}=100mΩ.

Based on the facts of gate-driver current consumption and silicon area estimation the topology with HV NMOS transistors for both switches will be used for the thesis.

3.3. Hysteretic Control Loop

After the decision which topology is used for the half-bridge a closer look for the chosen control loop is necessary. A hysteretic control loop can be used for VMC or CMC and it is a so called *hysteretic-regulator* (kind of a ripple-regulator). For the thesis a VMC hysteretic control loop is used. Figure 24 shows a principle buck converter with hysteretic control loop.

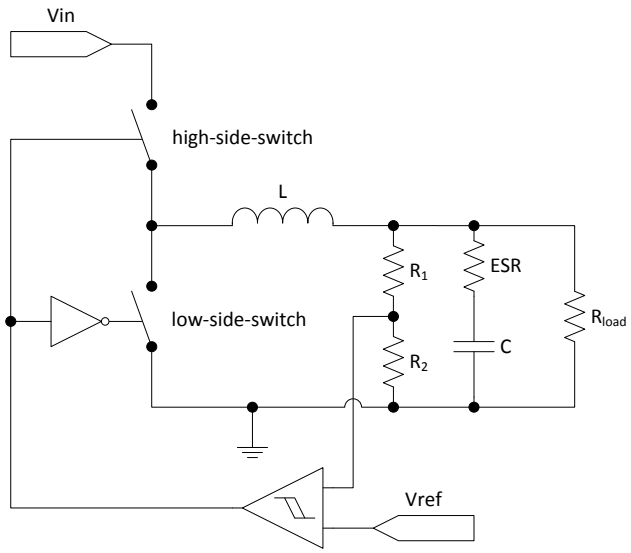

Figure 24 Shows a principle buck converter with hysteretic control loop

Figure 24 shows a resistor named ESR. This is the equivalent series resistance of the capacitor C. The ESR is very important for a hysteretic control because it generates a part of the ripple voltage which is necessary for the correct function of a hysteretic control loop. It is also important for the calculation of the switching frequency of the buck converter. It is necessary to calculate or estimate the switching frequency because the external components must be chosen based on these results. This means the external coil and capacitors must be able to work accurately at the switching frequency [4].

3.3.1. Calculations of the switching frequency in CCM

The following calculations will show how to calculate the influence of the most important parameters because the switching frequency is not only dependent on the ESR. Step by step the equation is expanded by other parameters until the final equation 33. It is necessary to know the switching frequency for the choice of the external components. The external components resonance frequency have to be above the switching frequency. For the calculations the term R_C is used instead of ESR. First the influences of the R_C and the hysteresis voltage of the hysteretic-comparator (V_H) are calculated [4].

$u = L\frac{di}{dt} \rightarrow \frac{u}{L}dt = di$ $\quad di\,R_c = du$ $\quad du \triangleq V_H$ $\quad V_{out} = V_{in}D$ (24), (25), (26), (27)

DT:

$$\frac{V_{in} - V_{out}}{L} R_C T_{ON} = V_H$$

(1-D)T:

$$\frac{V_{out}}{L} R_C T_{OFF} = V_H$$

T:

$$2V_H = \frac{V_{in} - V_{out}}{L} R_C T_{ON} + \frac{V_{out}}{L} R_C T_{OFF}$$

$$\Rightarrow \quad \frac{2V_H L}{R_C} = (V_{in} - V_{out})T_{ON} + V_{out}T_{OFF}$$

$$\Rightarrow \quad \frac{2V_H L}{R_C V_{out}} = \frac{(V_{in} - V_{out})}{V_{out}} T_{ON} + T_{OFF}$$

$$\Rightarrow \quad \frac{2V_H L}{R_C V_{out}} = \left(\frac{V_{in}}{V_{out}} - 1\right) T_{ON} + T_{OFF}$$

$$\Rightarrow \quad \frac{2V_H L}{R_C V_{out}} = \left(\frac{1}{D} - 1\right)(DT) + \big((1 - D)T\big)$$

$$\Rightarrow \quad \frac{2V_H L}{R_C V_{out}} = T\left[\left(\frac{1}{D} - 1\right)D + (1 - D)\right]$$

$$\Rightarrow \quad \frac{2V_H L}{R_C V_{out}} = T(1 - D + 1 - D)$$

$$\Rightarrow \quad \frac{2V_H L}{R_C V_{out}} = T(2 - 2D)$$

$$\Rightarrow \quad \frac{2V_H L}{R_C V_{out}} = T2(1 - D)$$

$$\Rightarrow \quad \frac{V_H L}{R_C V_{out}} \frac{1}{1-D} = T$$

$$\Rightarrow \quad \frac{V_H L}{R_C V_{out}} \frac{1}{1-\frac{V_{out}}{V_{in}}} = T$$

$$\Rightarrow \quad \frac{V_H L}{R_C V_{out}} \frac{1}{\frac{V_{in}-V_{out}}{V_{in}}} = T$$

$$\Rightarrow \quad \frac{V_H L}{R_C V_{out}} \frac{V_{in}}{V_{in}-V_{out}} = T$$

$$\Longrightarrow \quad f = \frac{R_C}{V_H L} \frac{V_{out}(V_{in}-V_{out})}{V_{in}} \quad (28)$$

V_H does not define the total ripple voltage (V_{ripple}) alone. As next step the influence of the feedback divider is added to equation 28.

$$f = \frac{R_C}{V_{ripple}\, L} \frac{V_{out}(V_{in}-V_{out})}{V_{in}} \quad (29)$$

$$V_{ripple} = V_H \left(1 + \frac{R_1}{R_2}\right) \quad (30)$$

Equation 30 shows the ripple voltage. The ripple voltage is the hysteresis voltage multiplied by the reciprocal ratio of the feedback divider. The capacitor also has an inductive parasitic component the so-called equivalent series inductance (ESL). It also has an influence on the switching frequency. For the calculations the term L_C is used instead of ESL:

DT:

$$u_{L_C} = L_C \frac{-di}{dt} \; ; \quad \frac{di}{dt} = \frac{V_{in}-V_{out}}{L} \; ; \quad u_{L_C} \triangleq V'_{ripple}$$

$$\Rightarrow \quad V'_{ripple} = L_C \frac{-(V_{in}-V_{out})}{L}$$

$$\Rightarrow \quad V'_{ripple} = (V_{out}-V_{in}) \frac{L_C}{L}$$

(1-D)T:

$$u_{L_C} = L_C \frac{di}{dt} \; ; \quad \frac{di}{dt} = \frac{-V_{out}}{L} \; ; \quad u_{L_C} \triangleq V'_{ripple}$$

$$\Rightarrow \quad V'_{ripple} = L_C \frac{-V_{out}}{L}$$

$$\Rightarrow \quad V'_{ripple} = -V_{out} \frac{L_C}{L}$$

T:

$$2V'_{ripple} = (V_{out} - V_{in})\frac{L_C}{L} + \left(-V_{out}\frac{L_C}{L}\right)$$

$$\Rightarrow \quad 2V'_{ripple} = V_{out}\frac{L_C}{L} - V_{in}\frac{L_C}{L} + V_{out}\frac{L_C}{L}$$

$$\Rightarrow \quad 2V'_{ripple} = -V_{in}\frac{L_C}{L}$$

$$\Rightarrow \quad V_{ripple} = V_H\left(1 + \frac{R_1}{R_2}\right) - V_{in}\frac{L_C}{L} \quad (31)$$

Equation 31 shows that the ESL also has an influence on the ripple voltage and consequently on the switching frequency. The last important influences of the switching frequency are the delays of the whole control-system (T_{don}, T_{doff}). T_{don} is the time that the control-systems needs from the time where the output voltage reaches the upper threshold voltage of the hysteretic-comparator (HSS is on) until the LSS is on. For T_{doff} vice versa is valid:

DT:

$$\frac{V_{in} - V_{out}}{L}R_C\left(T_{ON} + T_{d_{OFF}}\right) = V_{ripple} + V'_{ripple}$$

$$\Rightarrow \quad \frac{V_{in} - V_{out}}{L}R_C T_{ON} + \frac{V_{in} - V_{out}}{L}R_C T_{d_{OFF}} = V_{ripple} + V'_{ripple}$$

$$\Rightarrow \quad \frac{V_{in} - V_{out}}{L}R_C T_{d_{OFF}} = V'_{ripple}$$

(1-D)T:

$$\frac{V_{out}}{L}R_C\left(T_{OFF} + T_{d_{ON}}\right) = V_H + V'_{ripple}$$

$$\Rightarrow \quad \frac{V_{out}}{L}R_C T_{OFF} + \frac{V_{out}}{L}R_C T_{d_{ON}} = V_H + V'_{ripple}$$

$$\Rightarrow \quad \frac{V_{out}}{L}R_C T_{d_{ON}} = V'_{ripple}$$

T:

$$\Rightarrow \quad \frac{V_{in} - V_{out}}{L}R_C T_{d_{OFF}} + \frac{V_{out}}{L}R_C T_{d_{ON}} = 2V'_{ripple}$$

$$\Rightarrow \quad V_{ripple} = V_H\left(1 + \frac{R_1}{R_2}\right) - V_{in}\frac{L_C}{L} + \frac{V_{in} - V_{out}}{L}R_C T_{d_{OFF}} + \frac{V_{out}}{L}R_C T_{d_{ON}} \quad (32)$$

Equation 32 shows that the delays also have only a direct influence on the ripple voltage. Finally the switching frequency can be calculated by equation 33 and 34. As conclusion it can be said that a higher ripple voltage causes a lower switching frequency and vice versa.

$$\boldsymbol{f = \frac{R_C}{V_{ripple}\, L}\, \frac{V_{out}(V_{in}-V_{out})}{V_{in}}} \quad (33) \quad [4]$$

$$V_{ripple} = V_H \left(1 + \frac{R_1}{R_2}\right) - V_{in}\frac{L_C}{L} + \frac{V_{in}-V_{out}}{L} R_C T_{d_{OFF}} + \frac{V_{out}}{L} R_C T_{d_{ON}} \quad (34) \quad [4]$$

3.4. Switches

From chapter 3.1 the R_{ON} values of the HSS and LSS are known. But the switches are not realized by only one transistor for each side. To have more reusability in the future the switches are realized by parallel circuits of smaller transistors of the same size. These smaller transistors combined with a gate-driver build up a so-called IP-block (Intellectual Property). For this IP-block the R_{ON} of the transistor has to have a value of 170mΩ (this is a guideline of Dialog Semiconductor). About 30mΩ are estimated for the routing connections. This gives a total resistance of 200mΩ. For the HSS this IP-block is used in parallel four times which gives 50mΩ for the R_{ON}. For the LSS the IP-block is used in parallel two times which gives 100mΩ for the R_{ON}. The used HV NMOS transistor has a fixed gate length of 800nm. Figure 25 shows the test-bench and Figure 26 the result of a sweep simulation over the number of fingers for the transistor. The reason for V_{GS}=4.4V is to guarantee that the switch is also completely turned on in case of the worst case of Vdd=4.4V.

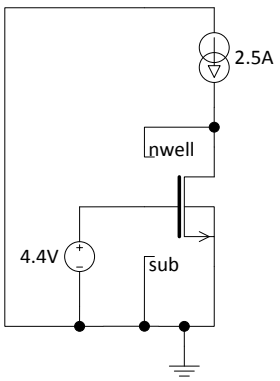

Figure 25 Test-bench for simulation of the R_{ON} of the 20V HV NMOS transistor

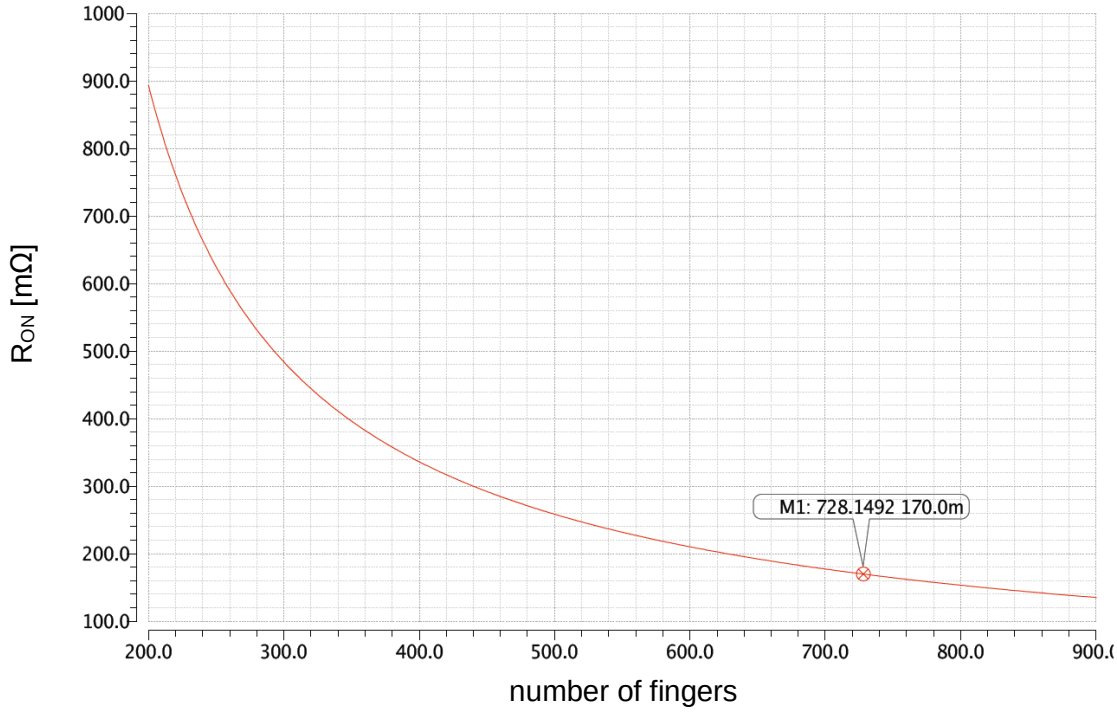

Figure 26 Sweep simulation over numbers of fingers for a 20V HV NMOS transistor

Figure 26 shows that the ideal number of fingers would be ~728. In accordance with the layout department the transistor parameters were fixed to the values in Table 13 for having a robust and reusable layout of the IP-block.

Length	**Finger-width**	**Number of fingers**	**Multiplier (m)**	**Total number of fingers**	**R_{ON}**
800nm	48µm	122	6	732	163.6mΩ

Table 13 Parameters for HV NMOS transistor of the IP-block

Results from the simulation of the HV NMOS transistor with the parameters from Table 13 are the electrical charge Q=358.4pC (which is needed to turn the transistor on) and the gate-capacitance C_G=86.4pF (for the DC operating point of the test-bench in Figure 19 @V_{GS}=5V). The gate-capacitance is very important for the design of the gate-driver because the gate-driver has to charge this gate-capacitance in a specified time for turning the switch on.

3.5. Gate-driver

For the design of the gate-driver it is necessary to define the rise-time[4] of the output-signal. The load of the gate-driver is the gate of the HV NMOS transistor. Equation 35 shows the relationship between gate-capacitance of the transistor (C_G), rise-time (t_r) and R_{ON} of the gate-driver.

$$t_r \approx 5\,\tau = 5\,R_{ON}\,C_G \quad (35)$$

The resistance of a transistor is not constant during turning on. It changes from MΩ to mΩ and the charging curve of a capacitor is non-linear. Because of these reasons calculations should be seen as estimations. Table 14 shows values for some parameters which are specified from the company.

Parameter	**Specification**
rise-time (t_r)	< 4ns
fall-time[5] (t_f)	< 4ns
I_{avg} average gate-driver current consumption for T=300ns	< 2mA

Table 14 Parameters for R_{ON} calculation of the gate-driver

The value from Table 14 for t_r used in equation 35 and the value for C_G from chapter 3.4 gives as result an R_{ON}≈9Ω.

By using the value for the electrical charge Q from the chapter before in equation 36 the average current consumption for a switching frequency of 3.3MHz (∆t=300ns) can be calculated.

$$Q = I_{avg}\ \Delta\, t \quad (36)$$

$$I_{avg} = \frac{Q}{\Delta\, t} = \frac{358.4\ 10^{-12}}{300\ 10^{-9}} = 1.195\ 10^{-3} \approx 1.2mA$$

As conclusion it can be said that the specification of 2mA is realizable. Equation 36 is also used for the current calculations in chapter 3.2.

[4] The rise-time is measured between 10% and 90% of a rising signal.
[5] The fall-time is measured between 90% and 10% of a falling signal.

During simulation of the half-bridge it can be seen that switching of the gate-signal of the high-side-switch has an influence on the gate-signal of the low-side-switch due to the Miller-effect [14] (see chapter 2.2.6) and vice versa (see Figure 27). This influence is called *crossvoltage*.

This crossvoltage must be small in positive value otherwise it could happen that the affected transistor also starts turning on which makes a short circuit. Because of this reason it was necessary to reduce the R_{ON} of transistor N9 by increasing its width. This makes N9 more powerful to keep the output voltage low and reduces in this way the crossvoltage.

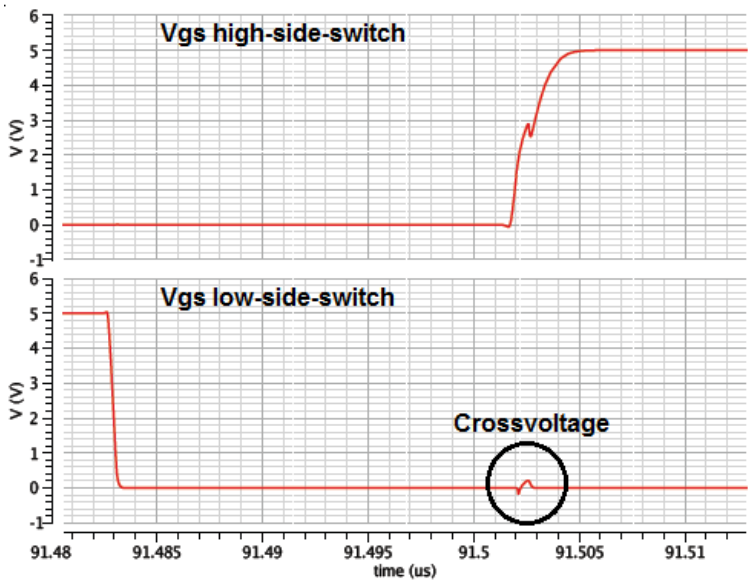

Figure 27 Shows the rising V_{GS} of the HSS and the generated crossvoltage at the LSS

The final schematic of the gate-driver is drawn in Figure 28. It is not possible to control the transistor M9 and N9 directly by a buffer or an inverter because the so-called crosscurrent which is normal for an inverter with so-called push-pull topology [3] would be too high. It was necessary to build up the gate-driver in several stages. The buffer at the input (buf1) restore the logic level for the following stages. The transistors N1 and M1 combined with the resistor R1 are realizing a small signal delay between the signal path for the PMOS of the output-stage (M9) and the signal path of the NMOS of the output-stage (N9). This delay reduces the crosscurrent in the output-stage. The inverters inv1 and inv2 have the same size. Also M2/N2 and M3/N3 have the same size. The inverters M4/N4, M6/N6 and M7/N7, M8/N8 does not have the same size. They are adjusted according to the respective output-stage transistor. To keep the delay between the two paths it is necessary that the inverters M2/N2 and M3/N3 have the same capacitive load at their outputs. Therefore the transistors M5 and N5 are inserted. They are connected as capacitors. The transistors M5 and M4 together have the same size as M6. N5 and N4 together have the same size as N6.

Function:

The gate-driver is a powerful buffer with several stages and a push-pull inverter output-stage with reduced crosscurrent. While the input signal is rising there is a crosscurrent through M1/N1. This crosscurrent causes a voltage drop over R1. Because of this voltage drop inverter inv2 changes its output to high earlier than inverter inv1. This delay makes sure that the NMOS of the output-stage (N9) is turning off a little bit earlier before the PMOS transistor (M9) is turning on. Similarly this is valid for a falling signal at the input. The crosscurrent is not equal to zero but it is significant lower than without this delay.

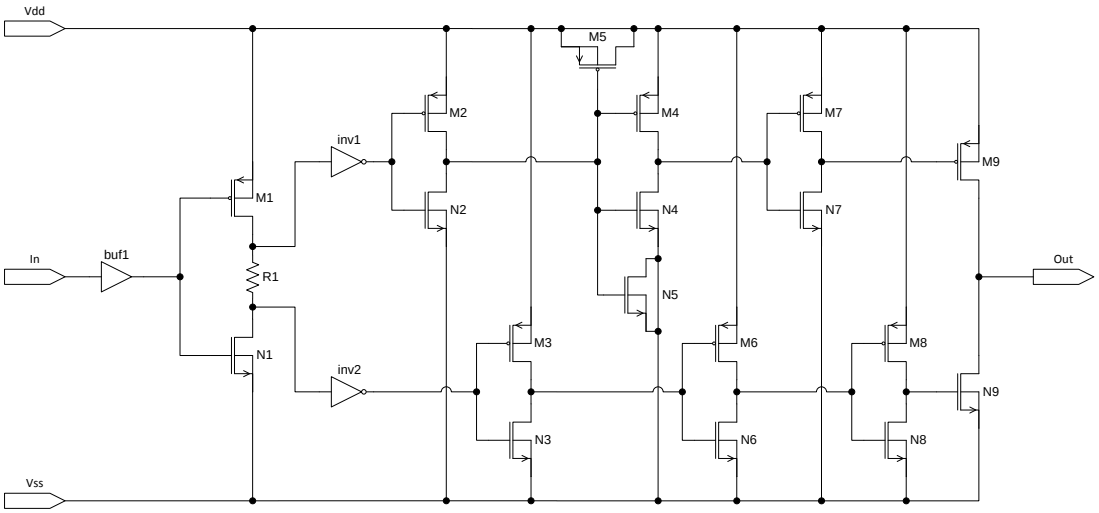

Figure 28 Shows the schematic of the gate-driver

3.6. Level-shifters

Level-shifters are necessary for shifting a signal from one voltage domain to another voltage domain. This two voltage domains could have different supply ranges or one of them is noisy and it is necessary to decouple.

3.6.1. Low-to-high level-shifter

The low-to-high level-shifter shifts the control signal for the high-side-switch from the LV-domain of the control-logic to the HV-domain of the high-side-switch. The HV-domain depends on the input voltage (V_{in}) because the Vss of the HV-domain is the Lx node of the buck converter. While the high-side-switch is turned on the voltage at the Lx node is V_{in} (the conduction loss of the high-side-switch is neglected). This means the maximum values for the HV-domain are Vssh=Lx=20V and Vddh=25V for V_{in}=20V. The unique thing here is that the Lx node is switching between 0V and V_{in}.

This fact makes the design of the low-to-high level-shifter very difficult because the voltage of the Lx node changes very fast which requires a large current. This makes it difficult to keep all transistors in the so-called Safe-Operating-Area (SOA) [13].

In Figure 29 the final schematic of the low-to-high level-shifter is drawn. The NMOS transistors N1, N2 and N5 build up a current mirror. The bias current I_b is 1µA. The transistors M1, M2, N8 and N9 build a buffer for the input signal which is powerful enough to control the HV NMOS transistor PN1.

The transistors M3 and N10 form an inverter which controls the HV NMOS transistor PN2. The two HV transistors are the main part of the level-shifter. They must resist a Vds voltage of 20V (maximum V_{in} voltage). The transistors N3 and N6 are connected as capacitors and N4 and N7 have the function to discharge these capacitors. The transistors M4, M11 and M7, M9 also build a current mirror. These two current mirrors have a relation over the so-called cross-coupled-pairs formed by the transistors M5, M6 and N11, N12. These cross-coupled-pairs speed up the switching of the level-shifter. The transistors M8 and M10 are connected as capacitors. These two capacitors decouple the gates for the changes on the Lx-node. Otherwise it could happen that these transistors leave the SOA. The transistors M12, N13 and M13, N14 form two inverters of the same size. This guarantees the same capacitive load for the transistor cross-coupled-pair N11, N12. The transistors M14, N15 build an inverter which is the output-stage of the level-shifter.

Function:

When the input-signal changes from low to high PN1 turns on and PN2 turns off. In the same moment N4 turns off and capacitor N3 (which was discharged by N4) increases the bias current until it is charged (at the same time N7 discharges the capacitor N6). By the higher current from N3 the switching of the PMOS current mirrors and the cross-coupled-pairs is stepped up and the output-stage set the output to high and vice versa. It is remarkable that after switching the low bias current of 1µA is enough to keep the correct output-signal.

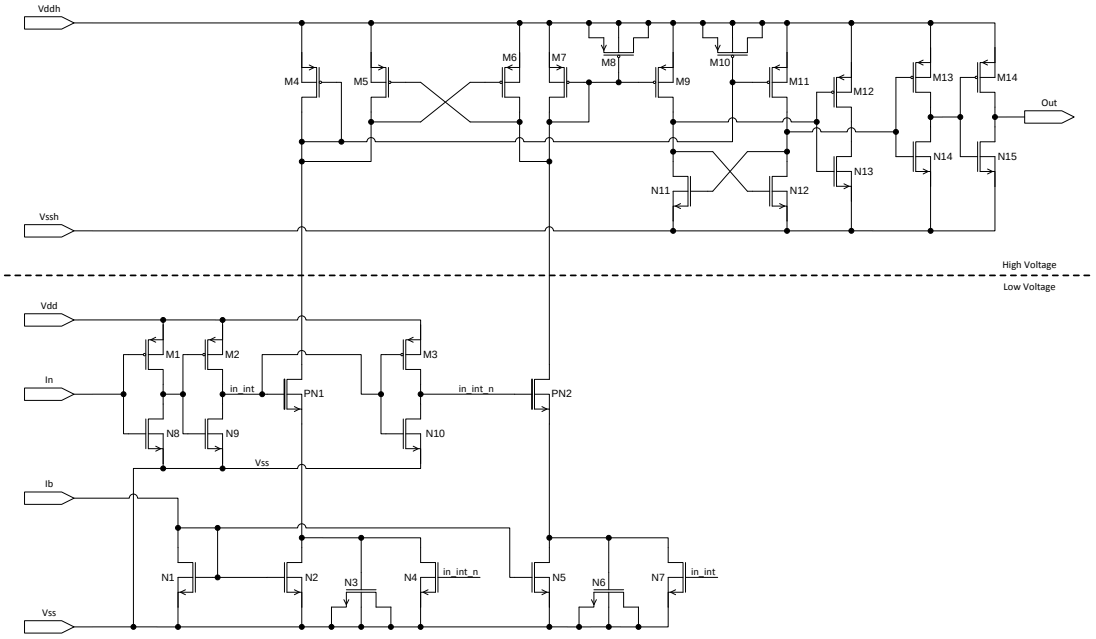

Figure 29 Shows the schematic of the low-to-high level-shifter

3.6.2. Low-to-high level-shifter for the active-diode

The low-to-high level-shifter for the active-diode shifts the control signal for the active-diode from the LV-domain to the HV-domain. The low-to-high level-shifter for active-diode is nearly the same like the low-to-high level-shifter before. Only for five transistors the parameters were adjusted. In Figure 30 the final schematic is drawn and the five adjusted transistors are marked with a yellow background-colour. The parameter changes were necessary to keep the transistors in SOA. The function is the same as before.

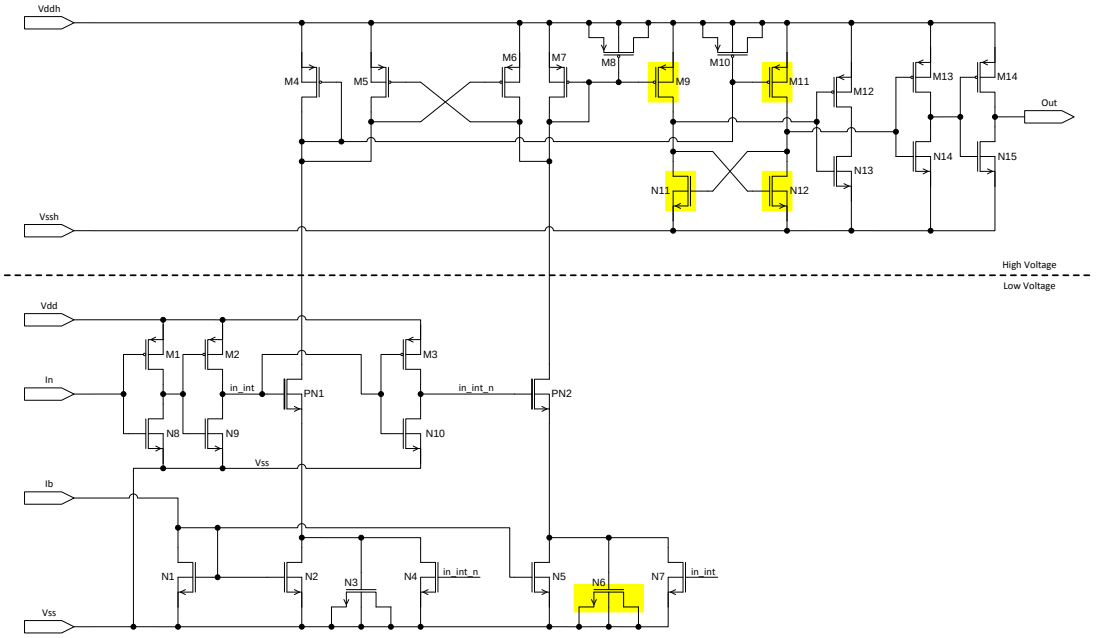

Figure 30 Shows the schematic of the low-to-high level-shifter for active-diode

3.6.3. High-to-low level-shifter

The high-to-low level-shifter shifts the gate-feedback-signal of the high-side-switch from the HV-domain to the LV-domain of the control-logic. The unique behaviour of the Lx node (see chapter 3.6.1) also makes the design of the high-to-low level-shifter difficult. In principle the design of the high-to-low level-shifter is a flipped design of the low-to-high level-shifter. Figure 31 shows the final design of the level-shifter. Like the low-to-high level-shifter the high-to-low level-shifter also contains a current mirror for the bias current. But this one is more complex because the bias current comes from the LV-domain and has to be mirrored into the HV-domain. Therefore it needs also HV transistors for the current mirror. The transistors PN1, PN2, PM3, PM4 and PM5 form this current mirror. The transistors N1, M1 and N2, M2 build an input buffer for the HV PMOS transistor PM1 and N3, M3 are an inverter for controlling PM2. M4 and M6 are transistors connected as capacitors. The transistor M5 charges M4 and M7 charges M6. It is the equivalent approach like at the low-to-high level-shifter. The capacitor C1 additionally is added to the high-to-low level-shifter.

C1 is necessary to keep the transistors in SOA the same applies to the transistors N8 and N10 which are connected as capacitors. Transistors N4, N11 and N7, N9 form two current mirrors. The outputs of these two current mirrors are combined by a cross-coupled pair (M8 and M9). N12, M10 and N13, M11 form two inverters of the same size which guarantees the same capacitive load for the cross-coupled pair M8, M9. The output-stage is like at the low-to-high level-shifter an inverter built by the transistors N14 and M12.

Function:

Function is similar to the low-to-high level-shifter. When the input-signal changes from high to low PM1 turns on and PM2 turns off. In the same moment M5 turns off and capacitor M4 (which was charged by M5) increases the bias current until it is discharged (at the same time M7 charges the capacitor M6). By the higher current from M4 the switching of the NMOS current mirrors from N4 and N6 and the cross-coupled pairs is stepped up and the output-stage set the output to low and vice versa. Again it is remarkable that after switching the low bias current of 1µA is enough to keep the correct output-signal. There is one additional feature in the high-to-low level-shifter compared to the low-to-high level-shifter. When the whole converter is disabled also the static current of the high-to-low level-shifter is disabled and the output-signal is fixed to low. The transistors N15, N16 and N17 disable the current mirrors. The transistor N18 sets the output-signal to low. The transistors N19 and M13 form a so-called transmission gate which disables the bias current.

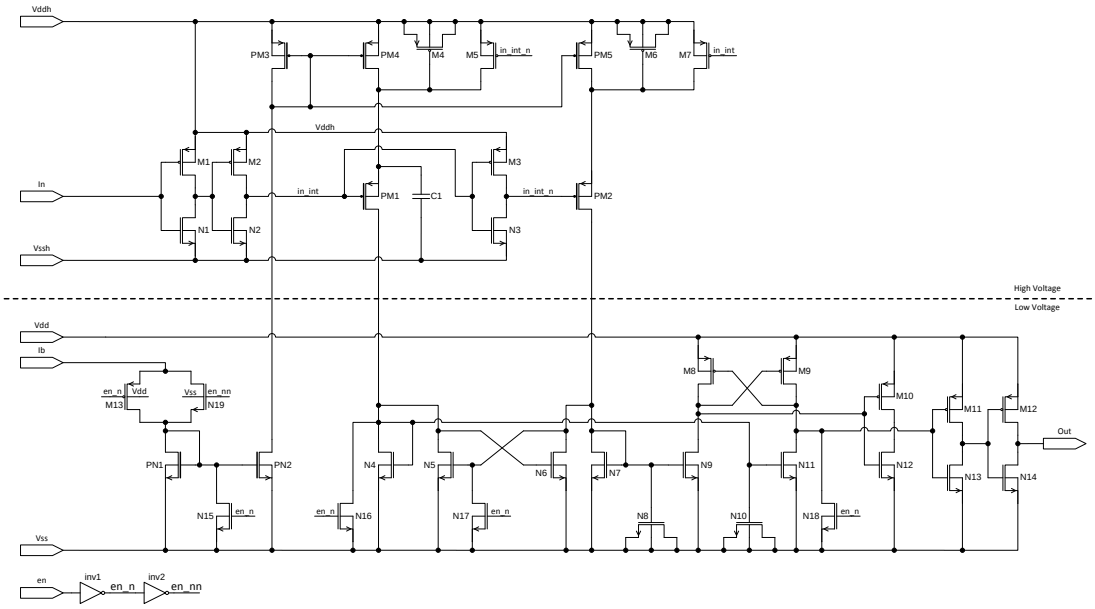

Figure 31 Shows the schematic of the high-to-low level-shifter

3.6.4. Low-to-low level-shifter for the gate-driver

The low-to-low level-shifter for the gate-driver shifts the control signal for the low-side-switch from the LV-domain of the control-logic to the power-domain of the low-side-switch. The low-to-low level-shifter is built by four stages. The first stage is the input-stage with a buffer and an inverter for the input transistors (buf1, inv1, N1 and N2). The second stage is a cross-coupled pair formed by the PMOS transistors M1 and M2. The third stage improves the signal from the second stage. It is a so-called rail-to-rail stage and contains also a cross-coupled pair (N3 and N4) and the transistors M3 and M4. The advantage of a cross-coupled pair is the provided positive feedback for faster switching. The fourth stage is a digital stage based on [8]. This logic selects always the faster edge for the change of the differential output-signal of the third stage.

Function:

When the input signal changes from low to high transistor N1 turns on and pulls down the gate from M2 to Vss. At the same time transistor N2 turns off. Also M1 turns off because N2 does not pull the gate down to Vss and the cross-coupled transistor M2 pushes the gate to Vddp. Also M3 is pulled down to Vss and M4 pushed to Vddp. Because of this N3 of the cross-coupled pair is pulled down to Vssp and M4 is pushed to Vddp. Now the logic sets the Out-signal to high and vice versa.

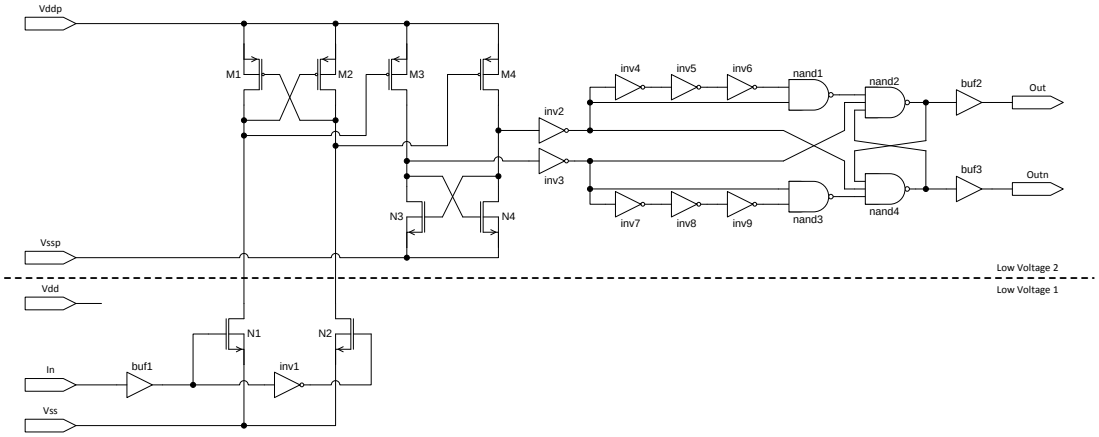

Figure 32 Shows the schematic of the low-to-low level-shifter for the gate-driver

3.6.5. Low-to-low level-shifter for the gate-feedback

The low-to-low level-shifter for the gate-feedback shifts the gate-feedback signal of the low-side-switch from the power-domain to the LV-domain of the control-logic. The low-to-low level-shifter for the gate-feedback is the flipped version of the low-to-low level-shifter for the gate-driver. The input-stage also contains an inverter (inv1) and a buffer (buf1) for the input transistors M1 and M2 (PMOS transistors instead of NMOS transistors). The second stage is an NMOS cross-coupled pair (N1 and N2). The third stage is also a rail-to-rail stage formed by the transistors N3, N4, M3 and M4. The fourth stage is again a digital stage with a logic which always detects the faster edge for the output-signal change.

Function:

It is the same way of function like at the low-to-low level-shifter for gate-driver only the type of transistors has changed (NMOS -> PMOS and vice versa).

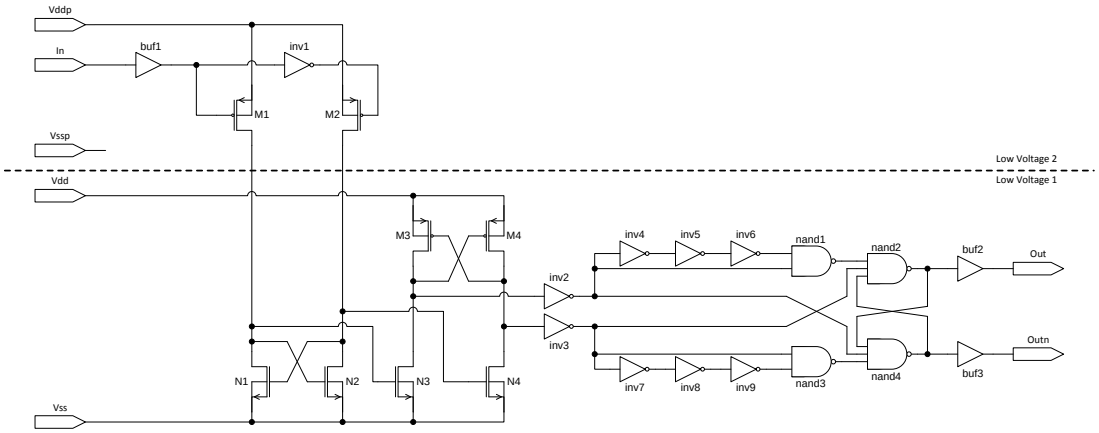

Figure 33 Shows the schematic of the low-to-low level-shifter for the gate-feedback

3.7. Schmitt-trigger

In chapter 2.2.6 the reason for using a Schmitt-Trigger is already explained. The transistors N1, N2, N3, M1, M2 and M3 form a classic Schmitt-trigger circuit. The transistors N4 and M4 form an inverter in this way the input-signal and the output-signal are non-inverted. Figure 34 shows the schematic of the Schmitt-trigger. With transistor N3 the upper threshold is defined (~2.1V) and transistor M3 defines the lower threshold (~1V). Figure 35 shows for nominal conditions a hysteresis sweep of the input-signal (signal rises from 0V to 5V and falls back to 0V).

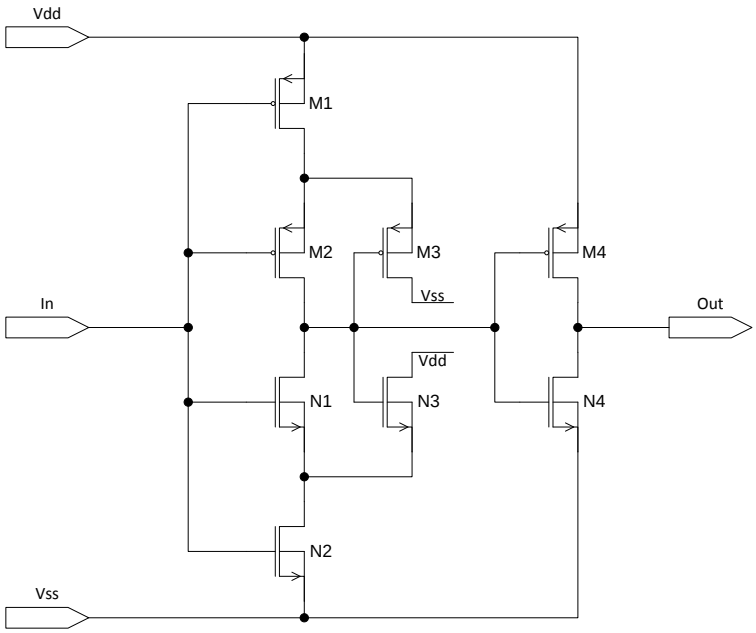

Figure 34 Shows the schematic of the Schmitt-trigger

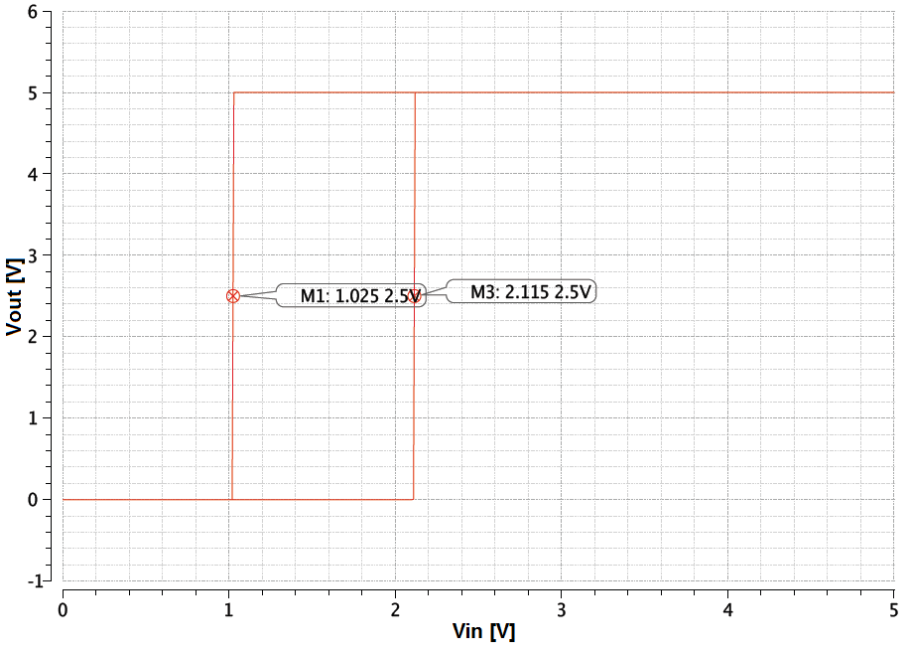

Figure 35 Shows the hysteretic characteristic of the Schmitt-trigger

3.8. Active-diode block

The active-diode block is part of the supply of the high-side. This topology of power supply is called bootstrapping. This topology is used because it is simple and inexpensive compared to a charge-pump. The high-side is supplied by an external capacitor (C_{boot}). This external capacitor is charged by the active-diode block. Figure 36 shows this block. It contains the low-to-high level-shifter for active-diode, a gate-driver and a HV PMOS transistor. This HV PMOS transistor is the active-diode that charges the external capacitor to Vdd. The capacitor can only be charged during the time when the low-side-switch is on otherwise the voltage of the capacitor (so-called bootstrapping-voltage, Vboot) is higher than Vdd. In theory a buck converter could have a duty-cycle of 100% which means the high-side-switch is turned on all the time. Thus there is no time for charging the capacitor. This problem is a big disadvantage of the bootstrapping topology but it is not focus of the thesis and so a minimum load time of 15ns is defined by Dialog Semiconductor. Because of this an estimation for the R_{ON} of the HV PMOS transistor can be done.

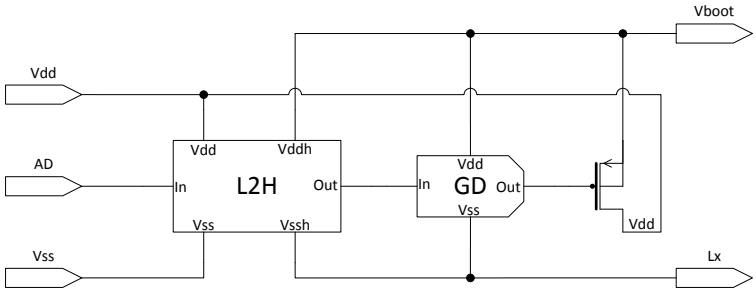

Figure 36 Shows the schematic of the active-diode block

Initially it is necessary to estimate the average current consumption of the high-side.

Estimation of the average current consumption @ 3.3MHz:

Sub-block	number	Current consumption for one period
LS_L2H	1	38µA
LS_L2H_AD	1	43µA
GD_HS	4	1.9mA
GD_AD	4	1.9mA
		15.281mA

Table 15 Estimation for the average current consumption of the sub-blocks

➔ I = 15.5mA

Now it is possible to make estimation for the R_{ON}.

Estimation of R_{ON}:

For the estimation the chosen switching frequency is again 3.3MHz (see chapter 3.2). A value of 100nF was chosen for the external bootstrapping capacitor C_{boot}. The supply voltage is 5V. The maximum load current is 2.5A because of this the maximum negative current through the low-side-switch is -2.5A. For the low-side-switch the IP-block is used in parallel two times which gives 81.8mΩ for the R_{ON} (see chapter 3.4).

T=300ns, t_{load}=15ns, C_{boot}=100nF, Vdd=5V, I_{LSS}=-2.5A, $R_{ON,LS}$=81.8mΩ

Until now the conduction loss of the low-side-switch was neglected. But the R_{ON} of the low-side-switch produces a voltage drop which decreases the voltage from the Lx node:

$$Lx = 0V + R_{ON_{LS}}\, I_{LSS} = 0 + 81.8\,10^{-3}\,(-2.5) = 0 - 204.5\,10^{-3} = -204.5\,10^{-3} \approx -200mV$$

$$Q = I.t = 15.5\,10^{-3}\,300\,10^{-9} = 4.65\,10^{-9}C$$

$$Q = C_{boot}.V \rightarrow V = \frac{Q}{C_{boot}} = \frac{4.65\,10^{-9}}{100\,10^{-9}} = 46.5\,10^{-3} = 46.5mV = V_{drop}$$

$$V_{end} = V_{dd} + L_X = 5 + (-0.2) = 4.8V$$

$$V_{start} = V_{end} - V_{drop} = 4.8 - 46.5\,10^{-3} = 4.7535V$$

$$\boldsymbol{V_{out} = V_{in}\left(1 - e^{\frac{-t}{\tau}}\right)} \quad (37)$$

$$V_{end} = V_{dd}\left(1 - e^{\frac{-x\,\tau}{\tau}}\right) \rightarrow x \approx 3.22 \rightarrow t_{end} = 3.22\tau$$

$$V_{end} = 5\left(1 - e^{\frac{-t_{end}}{\tau}}\right) = 5(1 - e^{-3.22})$$

- $V_{end} - V_{drop} = 5\left(1 - e^{\frac{-(t_{end} - t_{load})}{\tau}}\right)$

$$V_{drop} = 5(1 - e^{-3.22}) - 5\left(1 - e^{\frac{-(t_{end} - t_{load})}{\tau}}\right)$$

$$\rightarrow \frac{V_{drop}}{5} = 1 - e^{-3.22} - 1 + e^{\frac{-(t_{end} - t_{load})}{\tau}} = -e^{-3.22} + e^{\frac{-(3.22\tau - t_{load})}{\tau}}$$

$$\Rightarrow \frac{V_{drop}}{5} = -e^{-3.22}\left(1 - e^{\frac{t_{load}}{\tau}}\right)$$

$$\Rightarrow 1 - \frac{V_{drop}}{5\left(-e^{-3.22}\right)} = e^{\frac{t_{load}}{\tau}} \Rightarrow ln\left(1 - \frac{V_{drop}}{5\left(-e^{-3.22}\right)}\right) = \frac{t_{load}}{\tau}$$

$$\Rightarrow \tau = \frac{t_{load}}{ln\left(1 - \frac{V_{drop}}{5\left(-e^{-3.22}\right)}\right)}$$

$$\boldsymbol{\tau = R\,C} \Longrightarrow R = \frac{t_{load}}{C\,ln\left(1 - \frac{V_{drop}}{5\left(-e^{-3.22}\right)}\right)} \approx 715.55m\Omega \quad (38)$$

There are four active-diodes in parallel. The calculated resistance from equation 38 is valid for the total resistance of the parallel circuit. This means that for one active-diode the Ron can be four times bigger:

$$R_{on} = 4\,R \approx 2.87\Omega \quad (39)$$

The used 28V HV PMOS transistor has a fixed gate length of 600nm. Figure 37 shows the test-bench and Figure 38 the result of a sweep over the number of fingers for the transistor with multiplier of 6.

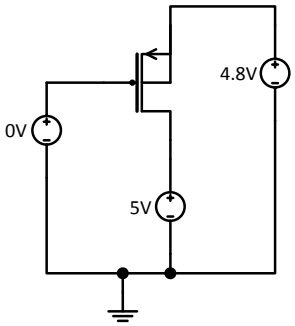

Figure 37 Test-bench for the 28V HV PMOS transistor as active-diode

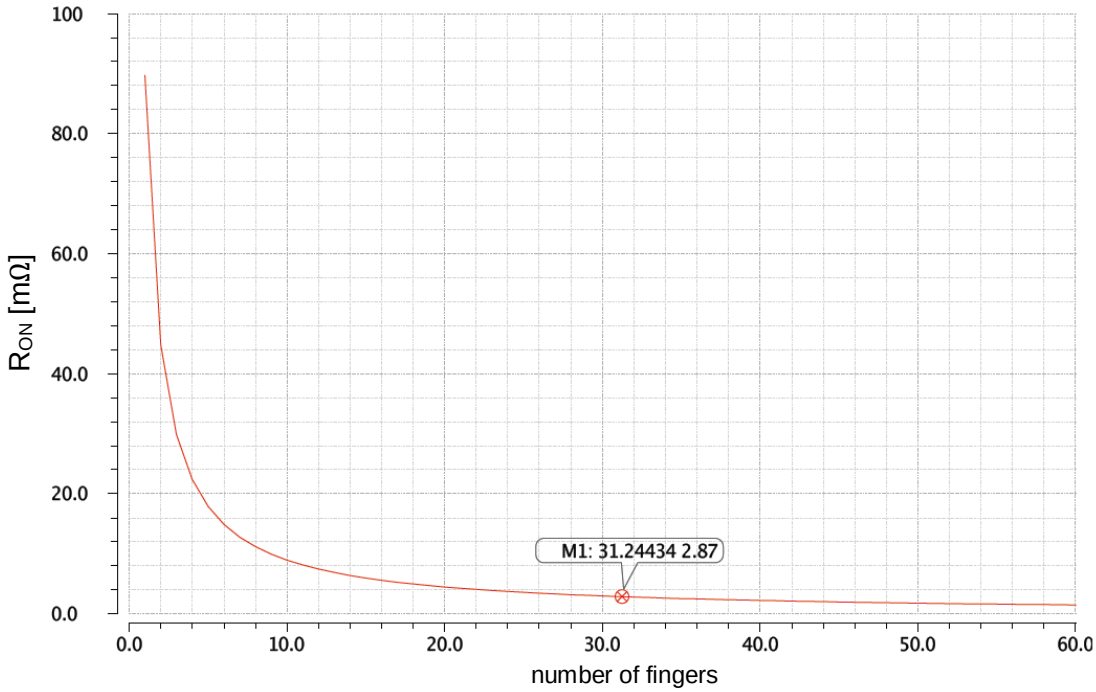

Figure 38 Sweep simulation over numbers of fingers for a 28V HV PMOS transistor

Figure 38 shows that the ideal number of fingers would be 31.24. In accordance with the layout department the transistor parameters were fixed to the values in Table 16 for having a robust and reusable layout:

Length	Finger-width	Number of fingers	Multiplier (m)	Total number of fingers
600nm	48µm	30	6	180

Table 16 Parameters for 28V HV PMOS transistor of the active-diode

3.9. Feedback

The feedback contains two voltage dividers and the logic to switch between these two. The dividers have the ratio of 3:1 and 1:1. The resistors R1 and R2 together with the capacitors C1 and C2 form the 1:1 divider. The transistors N1 and N2 enable or disable this divider dependent on the FB_div-signal and the en-signal. R1 and R2 have the same value also C1 and C2 have the same. The 3:1 divider is formed by the resistors R3 and R4 and by the capacitors C3 and C4. The transistors N3 and N4 enable or disable the divider also depending on the FB_div-signal and the en-signal. R3 is three times greater than R4 and C4 is three times greater the C3. The en-signal is the global converter enable signal. If the converter is disabled both dividers are also disabled and the output is set to low by the transistor N5.

The inverters inv1-6 and the two NAND-gates (nand1, nand2) form the logic for selecting the divider and disable the whole feedback. Figure 39 shows the final schematic. Table 17 shows a truth-table for the transistors.

en	FB_div	N1	N2	N3	N4	N5	divider-ratio
0	0	on	on	off	off	off	1:1
0	1	off	off	on	on	off	3:1
1	0	off	off	off	off	on	0
1	1	off	off	off	off	on	0

Table 17 Truth-table for the feedback dividers

Function:

For low frequencies a divider formed by resistors would be enough. But for higher frequencies (for example 3.3MHz) simulation shows that the parasitic capacitances of the resistors have an influence on the output. Hence it is necessary to use also a divider formed by capacitors parallel to the resistor divider. For higher frequencies the capacitive divider is dominating.

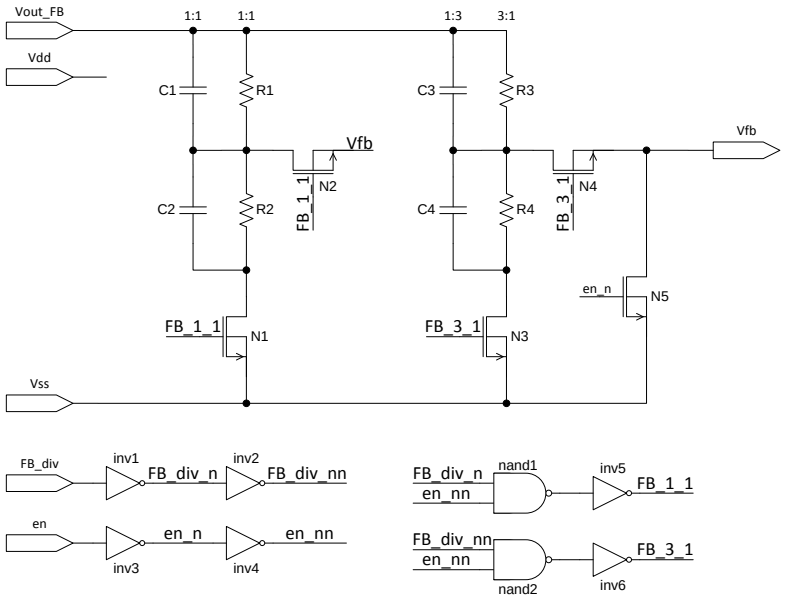

Figure 39 Shows the schematic of the feedback

3.10. Comparator

The original comparator was designed by Dialog Semiconductor. The transistors N1-N10 and M3-M7 are designed as minimum sized transistors for this work. This means the length and width of the transistors are set to the minimum value which are allowed by the process[6]. The reason therefore is to have a fast comparator. The design is based on an internal positive feedback topology to create a small hysteresis [3]. Transistors M1 and M2 form the input stage of the comparator. Transistors N8-N10 and M6, M7 disable the comparator and set the output to low. The inverters inv1 and inv2 buffer the en-signal.

Function:

Assume the gate of M1 is biased to a reference voltage and the gate of M2 is set to high. Hence M2 is turned off as well as N6 and N2. The transistors M1, N1 and N7 are turned on. Thus the gate of N2 is pulled down by transistor N7. The same is valid if the gate of M2 is set to low. A special thing in that topology is that the output stage formed by transistors N4 and M4 is followed by another buffer stage. Transistor M5 is connected to the N4/M4 buffer stage, whereas transistor N5 is connected to the N1/M1 pair which is part of the input stage.

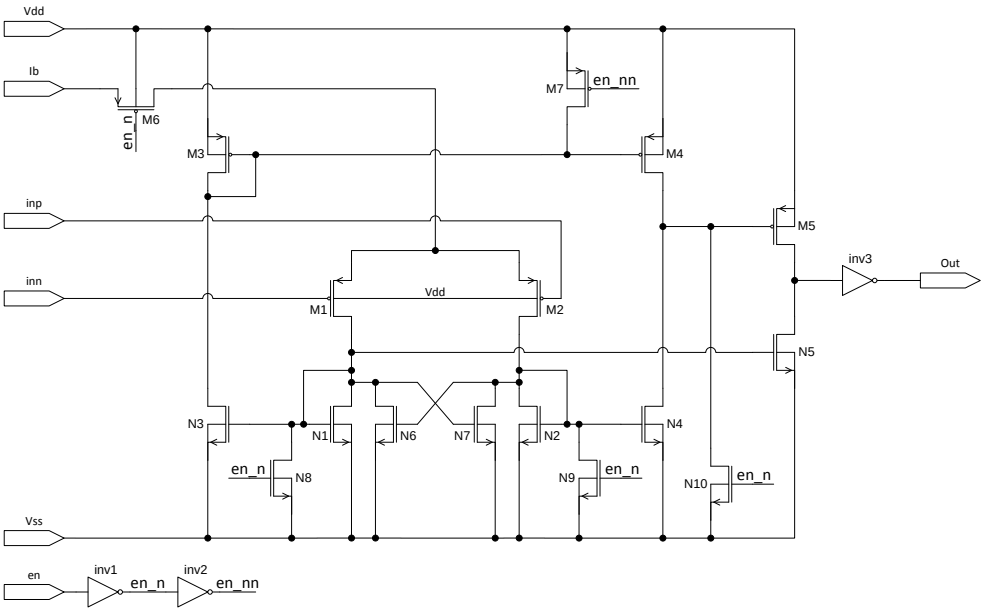

Figure 40 Shows the schematic of the comparator

[6] For NMOS transistor the minimum L=W=600nm, for PMOS transistor the minimum L=500nm and the minimum W=600nm

3.11. Hysteretic-Comparator

The hysteretic-comparator is formed by several sub-blocks. The first block is an internal current-bank formed by the transistors N1, N2, N3, N4, M1, M2, M3, M4 and M5. The topology of the current-bank is the same as in the global current-bank (chapter 3.13). The transistors M2 and M3 provide the bias currents for the two comparator instances CMP1 and CMP2. The operational amplifier AMP1 is biased by the transistors M4 and M5. This operation amplifier provides together with the transistors N6, M6 and the resistor R1 the bias current for the switchable hysteresis-voltage.

The advantage of this kind of bias current generation is that the process variations of the resistors R2 and R3 can be compensated to a large degree what increases the accuracy of the hysteresis voltage. The operational amplifier AMP1 is designed by Dialog Semiconductor. The transistors M7 and N7 provide the bias current for the NMOS transistors N8, N9, N10 and N11. The PMOS transistors M8, M9, M10 and M11 get their bias current from transistor M6. The transistors N8 and M8 provide a current of 10µA. N9 and M9 provide a current of 5µA. N10 and M10 provide a current of 2.5µA. N11 and M11 provide a current of 1µA. These four different current sources and sinks can be enabled and disabled in pairs by the transistors N12-N19. Figure 41 shows the final schematic.

The nodes Vh and Vl are connected together by the equal series resistors R2 and R3 (R2=R3=2.5kΩ). Between R2 and R3 the reference voltage V_{ref} is connected. Also Vh is connected to CMP1 and Vl is connected to CMP2. The four pairs of current sources/sinks are controlled by the logic which is formed by the inverters inv1-10 and the NAND-gates nand1-4. The second input of CMP1 is connected to Vfb which is the output-signal of the feedback (chapter 3.9). Also the second input of CMP2 is connected to Vfb. The outputs of the two comparators control a RS-FF formed by the inverter inv11 and the NAND-gates nand5-nand7. This RS-FF provides the output-signal of the hysteretic-comparator. CMP1 resets the RS-FF and CMP2 sets the RS-FF. The transistors N5, N20, N21, M12, M13 and M14 are for disable of the whole hysteretic comparator. The transistors M12 and N21 form a T-gate which disables the bias current. The transistors N5, N20, M13 and M14 disable the current mirrors. The output-signal is set to low by the comparators because the output of the comparators is low when they are disabled (chapter 3.10). The logic switches the transistors N12-N19 off.

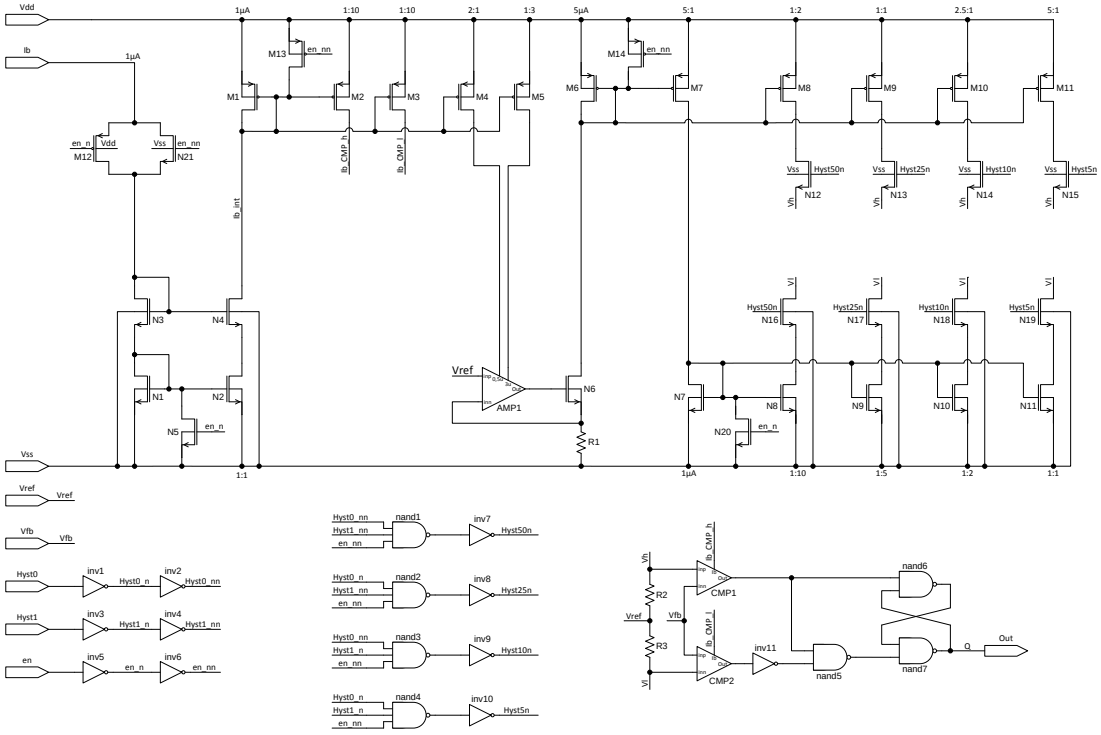

Figure 41 Shows the schematic of the hysteretic-comparator

Function:

For example if the transistors N12 and N16 are on a current of 10 µA flows through the resistors R2 and R3. This current generates a voltage-drop of 25mV at the resistor R2 and R3. Because of these voltage-drops the voltage difference between the nodes Vh and Vl is 50mV. This voltage difference is the hysteresis-voltage V_H. The reference voltage (for example 1.25V) is connected between the resistors R2 and R3. Based on this fact the voltages at nodes Vh and Vl are fixed to:

$$Vh = V_{ref} + \frac{V_H}{2} \quad (40) \qquad Vl = V_{ref} - \frac{V_H}{2} \quad (41)$$

For the example Vh=1.275V and Vl=1.225V. Vh is the reference voltage for CMP1 and Vl is the reference voltage for CMP2. If Vfb rise above 1.275V the comparator CMP1 resets the RS-FF and the output-signal is low. If Vfb falls-down under 1.225V the comparator CMP2 sets the RS-FF and the output-signal is high. By changing the current through the resistors R2 and R3 the hysteresis-voltage is changed and with that also the two reference voltages are changed. Table 18 shows a truth-table as an overview:

en	Hyst1	Hyst0	$I_{R2}=I_{R3}$ [µA]	V_H [mV]
0	0	0	1	5
0	0	1	2	10
0	1	0	5	25
0	1	1	10	50
1	x	x	0	0

Table 18 Truth-table for the hysteretic-comparator

Figure 42 shows the different hysteresis-voltages over time. Between 0µs and 5µs the circuit starts up and settles to its operating point. From 5µs to 10µs Hyst1 and Hyst0 are high the result is a hysteresis-voltage of 50mV. From 10µs to 15µs Hyst1 is high and Hyst0 is low the result is a hysteresis-voltage of 25mV.

Note: The changing of the signals Hyst0, Hyst1 and en from low to high and vice versa happen in 1ns. Also Figure 42 shows that after changing of the control signals the hysteresis-voltage needs an amount of time to settle again.

From 15µs to 20µs Hyst1 is low and Hyst0 is high the result is a hysteresis-voltage of 10mV. From 20µs to 25µs Hyst1 and Hyst0 are low the result is a hysteresis-voltage of 5mV. The en-signal is from 0µs to 25µs high and turns than to low. From 25µs to 30µs Hyst1 and Hyst0 are high again but in spite of this the hysteresis-voltage is zero because the en-signal is low.

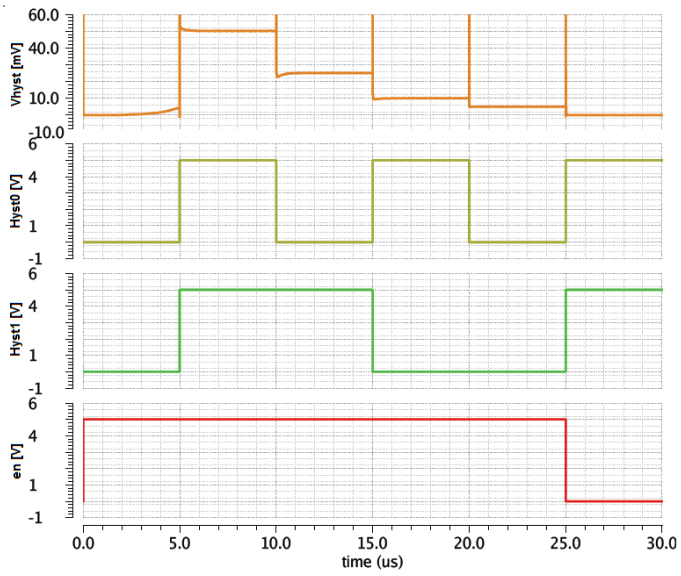

Figure 42 Shows the different hysteresis-voltages

3.12. Control-Logic (incl. Test-Logic)

The control-logic is the digital part of the control system. Its task is to provide the control signals for the high-side-switch (HS-signal), the low-side-switch (LS-signal) and the active-diode (AD-signal). Also a test-logic is designed in this block. The inverters inv18-inv29 form buffers for the input-signals. The inverters inv14-inv17 provides the inverted and buffered enable-signals for the converter and the active-diode. It is possible to disable the active-diode separately if it is wanted to use an external circuit for charging the capacitor of the high-side supply. The inverter inv5 and the NAND-gates nand3-nand5 form the RS-FF for the internal HS-signal. The RS-FF for the internal LS-signals is formed by the inverter inv6 and the NAND-gates nand6-nand8. Figure 43 shows the final schematic.

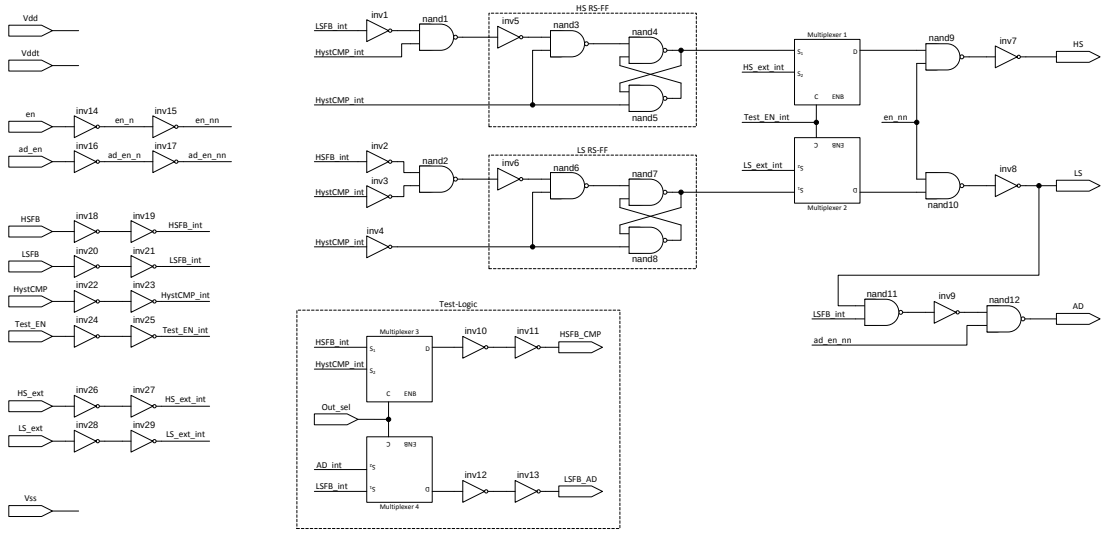

Figure 43 Shows the schematic of the control-logic

Function control-logic:

The control-logic has three parts:

1. control-signals for high-side-switch and low-side-switch (HS-signal, LS-signal)
2. control-signal for active-diode (AD-signal)
3. test-logic

Control-signals for high-side-switch and low-side-switch (HS-signal, LS-signal):

The inverter inv1 and the NAND-gate nand1 form together with the signals LSFB and HystCMP the set-logic for the RS-FF of the HS-signal. The HystCMP-signal directly controls the reset-input of the RS-FF. The inverters inv2, inv3 and the NAND-gate nand2 form together with the signals HSFB and HystCMP the set-logic for the RS-FF of the LS-signal.

The inverted HystCMP-signal (inv4) controls the reset-input of the RS-FF. Figure 44 shows the state-diagram for the HS RS-FF and Figure 45 for the LS RS-FF.

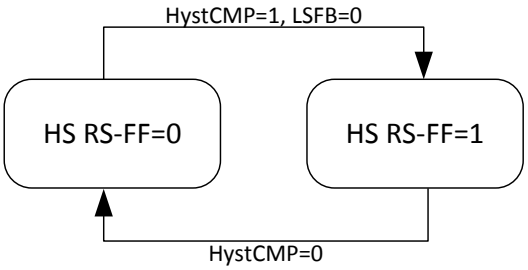

Figure 44 State-diagram for the HS RS-FF

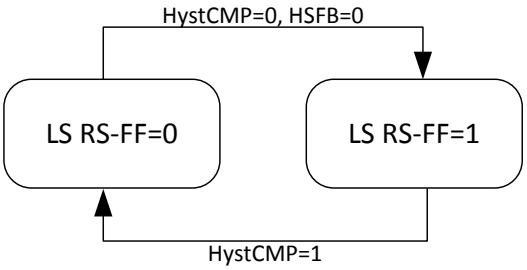

Figure 45 State-diagram for the HS LS-FF

The output-signals of the RS-FFs are multiplexed with the external signals HS_ext and LS_ext. Multiplexer1 multiplexes the HS_ext-signal and the HS-signal and Multiplexer2 multiplexes the LS_ext-signal and LS-signal. The Test_EN-signal controls which signals are forwarded through the multiplexers. If the Test_EN-signal is high the external signals (HS_ext, LS_ext) are forwarded and control directly the high-side-switch and low-side-switch. That means that the control-loop is disabled and both switches are externally controlled. If the Test_EN-signal is low the signals from the RS-FFs are forwarded and the control-loop active. The NAND-gates nand9, nand10 and the inverters inv7, inv8 form the output-stage which can be enabled and disabled by the en-signal. If the en-signal is low the HS-signal and the LS-signal are both fixed to low so the both switches are off and the converter is disabled. If the en-signal is high the signals from the multiplexers are forwarded through the output-stage.

Control-signal for active-diode (AD-signal):

The LS-signal from the output-stage is used additionally together with the LSFB-signal, the ad_en-signal, the NAND-gates nand11, nand12 and the inverter inv9 to form the AD-signal which controls the active-diode. Table 19 shows the truth-table for the AD-signal.

LS	LSFB	ad_en	AD
X	X	0	1
0	0	1	1
0	1	1	1
1	0	1	1
1	1	1	0

Table 19 Truth-table for the AD-signal

Test-logic:

The test-logic is formed by the two multiplexers Multiplexer3, Multiplexer4 and the four inverters inv10-13. The inverters inv10, inv11 and inv12, inv13 build a buffer output-stage. The task of the test-logic is to provide two signals out of four. These two signals are connected to pins and can be externally measured (HSFB_CMP-signal and LSFB_AD-signal). Multiplexer1 multiplexes the HSFB-signal and the HystCMP-signal and Multiplexer2 multiplexes the LSFB-signal and the AD-signal. The multiplexers are controlled by the Out_Sel-signal. Table 20 shows a truth-table for the output-signals HSFB_CMP and LSFB_AD.

Out_Sel	HSFB_CMP	LSFB_AD
0	HSFB	LSFB
1	CMP	AD

Table 20 Truth-table for the test-logic signals

3.13. Current-Bank

The current bank delivers the bias currents for all devices inside the converter. The current-bank is formed by two current mirrors. The first is a cascoded current-mirror build by the NMOS transistors N1, N2, N3 and N4. It mirrors the external bias current for internal usage. The second current-mirror is formed by the PMOS transistors M1, M2, M3, M4 and M5. Transistor M4 provides the bias current for the hysteretic-comparator. M3 provides the bias current for the low-to-high level-shifter for active-diode. M4 provides the bias current for the high-to-low level-shifter. M5 provides the bias current for the low-to-high level-shifter.

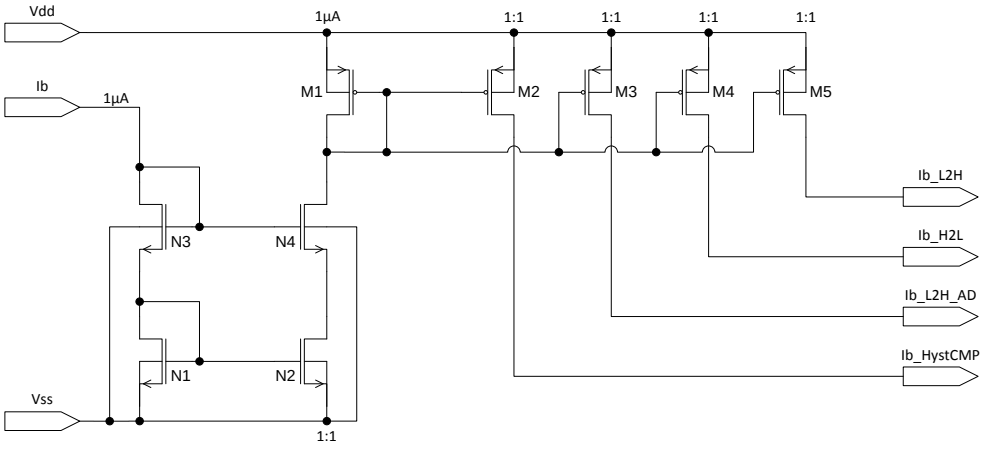

Figure 46 Shows the schematic of the current-bank

3.14. Entire design

Figure 47 shows all sub-blocks together and the external components which are necessary for the function.

Hint: For a clear schematic the substrate connections, the enable-signals, the test-signals and the bias-currents are not sketched.

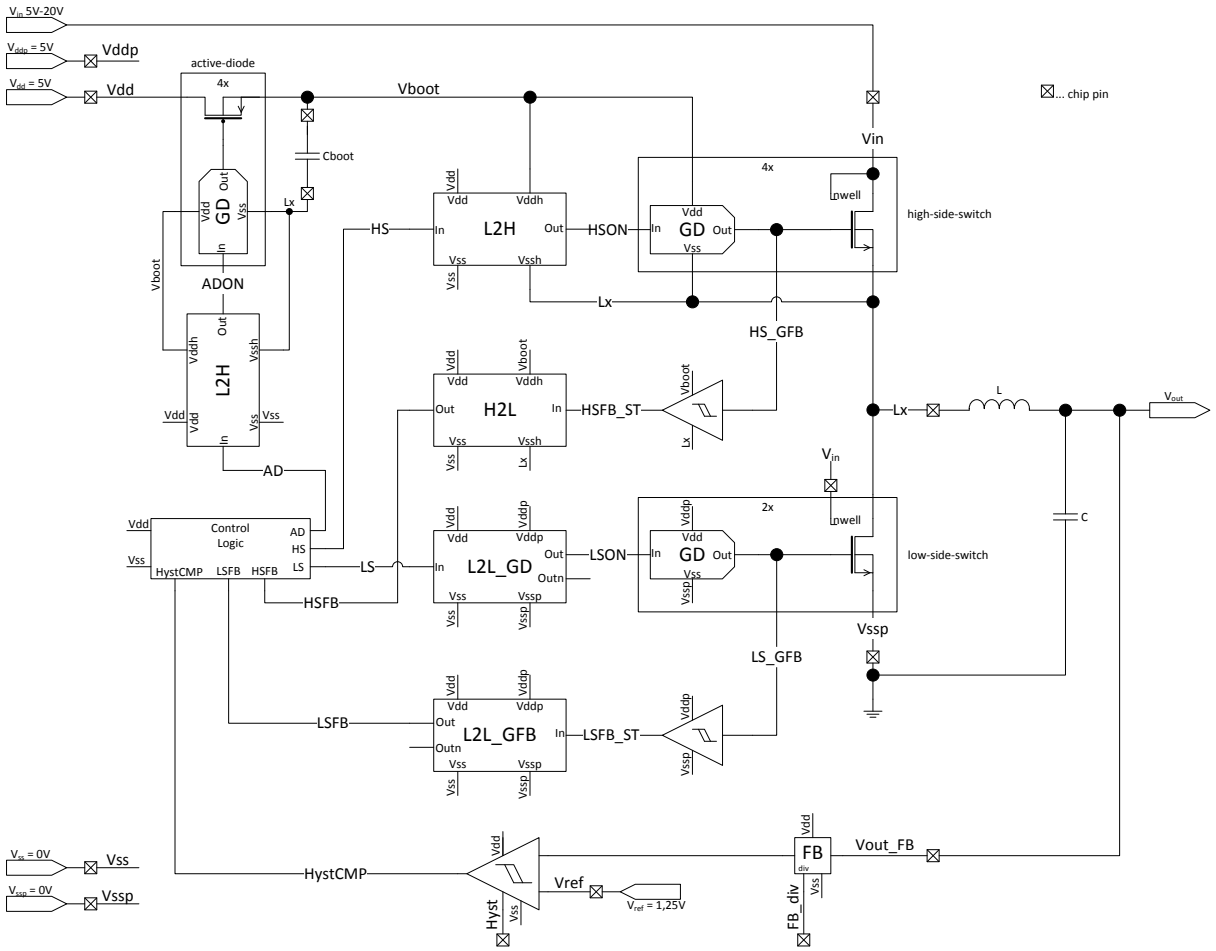

Figure 47 Shows a block diagram of the entire design

Simulations show that it is necessary to ramp up the reference voltage to prevent too high currents at the supply- and input-pins which could destroy the bond wires. For start-up a ramp-up time for the reference voltage from 0V to 1.25V of 250µs is used. It is possible to run the designed converter with a duty cycle of 100%. That means V_{in}=5V and V_{out} is forced to be also 5V. Simulation shows that the output voltage is not able to reach the 5V the reason is the R_{ON} of the high-side-switch which produces a voltage drop dependent on the load-current. Figure 48 shows the start-up of the buck converter for V_{in}=20V and a set V_{out} of 5V. It is also possible to see the behaviour of V_{out} when V_{in} drops to 5V (@300µs). The orange line is the control signal for the high-side-switch.

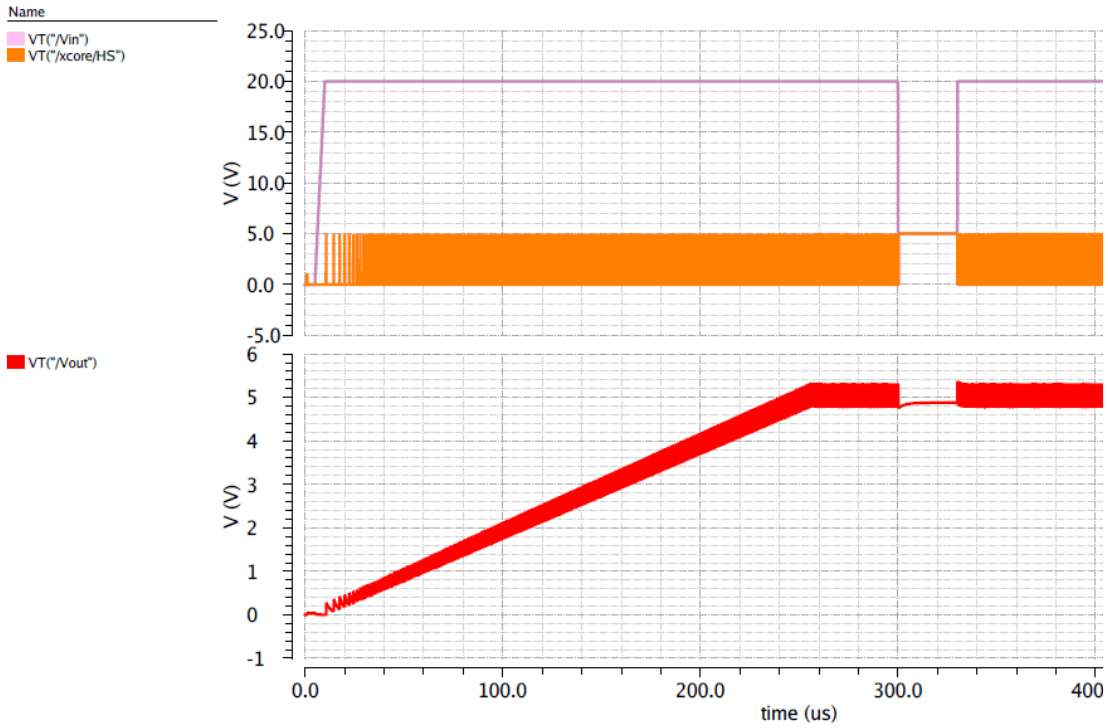

Figure 48 Shows the start-up of the buck converter for V_{in}=20V and a V_{out} of 5V

Figure 49 shows a zoom view around 300µs of Figure 48. Now it is possible to see the ripple of V_{out} more detailed. Also it can be seen that V_{out} is not able to reach 5V while V_{in}=5V.

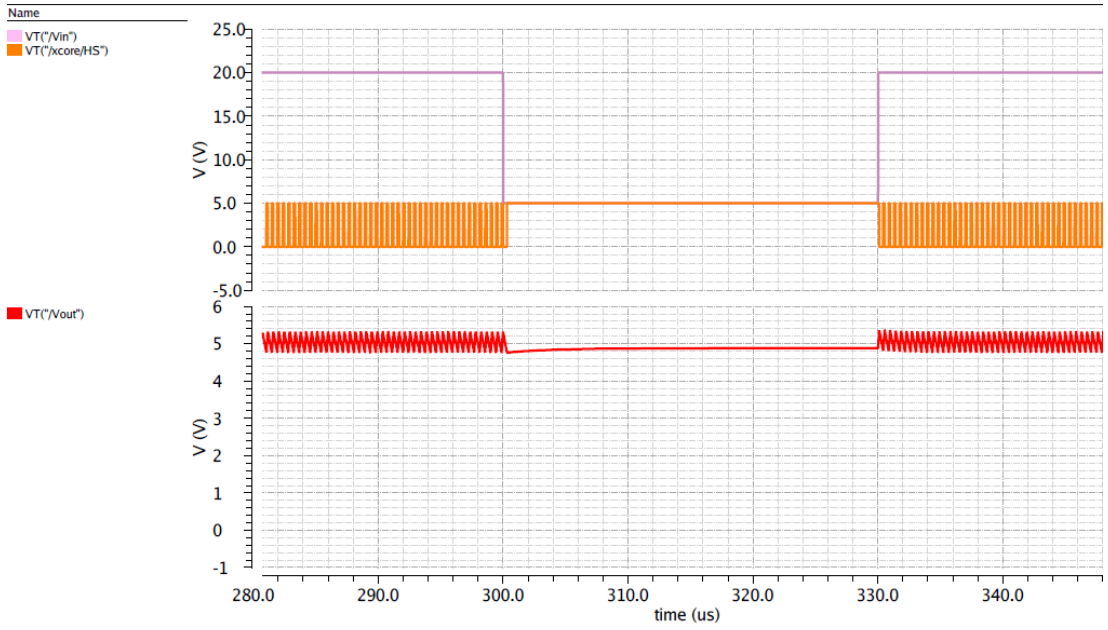

Figure 49 Shows a zoom view of Figure 48 around 300µs

3.15. Simulation results

Table 22 shows the parameters for the corner simulations. These parameters are used for all simulations. The rising- and falling-delay are measured between 50% of the signals. The rise- and fall-time are measured between 10% and 90% of the respective output-signal. Also three external components are necessary:

External component	Value
coil for the buck converter	1µH
capacitor for the buck converter	30µF
capacitor for the high-side supply	100nF

Table 21 List of the external components

Model file	**Sections used in simulation**		
active.scs	fnsp, snfp, ss, ff, tt		
passive.scs	pass_hi, pass_lo, pass_nom		
Temperature [°C]	**Typ**	**1**	**2**
Temp	27	-40	125
Supply [V], [µA]	**Typ**	**1**	**2**
Vdd – Vss	5	4.5	5.5
Vddh – Vssh [7]	5	4.5	5.5
Vddp – Vssp	5	4.5	5.5
Vss	0	0.5	-
Vssp	0	-1	0.5
Vssh [8]	0	-1	-
Vin	20	5	-
V_{ref}	1.25	-	-
Ib	1	-	-

Table 22 Parameters for corner simulations

[7] Vddh ≙ Vboot, Vssh ≙ Lx

[8] only controlled for the level-shifters L2H and H2L, switches between given value and V_{in}

Table 23 – Table 36 show for all sub-blocks the specifications and the simulation results.

Parameter	Symbol	Condition		min	typ	max	unit
resistance	Ron	Vgs=4.4V, Id=2.5A	specification		170		mΩ
			simulation	110.7	169	321.9	mΩ

Table 23 Simulation results of the 20V HV NMOS transistor for the IP-block

Parameter	Symbol	Condition		min	typ	max	unit
Crossvoltage		@ 3.3 MHz	specification			330	mV
			simulation	110.5	227	327.9	mV
propagation delay rising (GD-HS)	tprop_r_HS	@ 3.3 MHz	specification			4	ns
			simulation	1.33	1.772	2.86	ns
propagation delay falling (GD-HS)	tprop_f_HS	@ 3.3 MHz	specification			4	ns
			simulation	0.87	1.158	1.709	ns
propagation delay rising (GD-LS)	tprop_r_LS	@ 3.3 MHz	specification			4	ns
			simulation	1.458	1.915	2.843	ns
propagation delay falling (GD-LS)	tprop_f_LS	@ 3.3 MHz	specification			4	ns
			simulation	0.877	1.137	1.69	ns
rise time (GD-HS)	tr_HS	@ 3.3 MHz	specification			4	ns
			simulation	1.205	1.937	2.935	ns
fall time (GD-HS)	tf_HS	@ 3.3 MHz	specification			4	ns
			simulation	274.1	344.3	503.3	ps
rise time (GD-LS)	tr_LS	@ 3.3 MHz	specification			4	ns
			simulation	1.195	1.632	2.526	ns
fall time (GD-LS)	tf_LS	@ 3.3 MHz	specification			4	ns
			simulation	286.5	363.9	554.2	ps

Table 24 Simulation results for the gate-driver (at high-side and low-side)

Parameter	Symbol	Condition		min	typ	max	unit
propagation delay rising	tprop_r	@ 3.3 MHz	specification			3.5	ns
			simulation	0.427	0.743	1.532	ns
propagation delay falling	tprop_f	@ 3.3 MHz	specification			3.5	ns
			simulation	1.066	1.566	3.015	ns
rise time	tr	@ 3.3 MHz	specification			500	ps
			simulation	54.77	82.99	150.3	ps
fall time	tf	@ 3.3 MHz	specification			500	ps
			simulation	67.94	91.61	147	ps
supply	I_dynamic_sum[9]	@ 3.3 MHz	specification			45	µA
			simulation	20.14	27.75	36.81	µA

Table 25 Simulation results for the low-to-high level-shifter

Parameter	Symbol	Condition		min	typ	max	unit
propagation delay rising	tprop_r	@ 3.3 MHz	specification			3.5	ns
			simulation	0.452	0.79	1.628	ns
propagation delay falling	tprop_f	@ 3.3 MHz	specification			3.5	ns
			simulation	1.307	1.952	3.453	ns
rise time	tr	@ 3.3 MHz	specification			500	ps
			simulation	55.9	86.46	155	ps
fall time	tf	@ 3.3 MHz	specification			500	ps
			simulation	89.05	122.1	202	ps
supply	I_dynamic_sum	@ 3.3 MHz	specification			45	µA
			simulation	18.88	28.99	41.23	µA

Table 26 Simulation results for the low-to-high level-shifter for active-diode

Parameter	Symbol	Condition		min	typ	max	unit
propagation delay rising	tprop_r	@ 3.3 MHz	specification			3.5	ns
			simulation	1.363	2.329	3.287	ns
propagation delay falling	tprop_f	@ 3.3 MHz	specification			3.5	ns
			simulation	0.875	1.252	3.37	ns
rise time	tr	@ 3.3 MHz	specification			500	ps
			simulation	72.8	98.22	150.2	ps
fall time	tf	@ 3.3 MHz	specification			500	ps
			simulation	48.72	65.87	147.1	ps
supply	I_dynamic_sum	@ 3.3 MHz	specification			55	µA
			simulation	32.16	41.5	54.97	µA
supply	I_static_sum	DC	specification			100	nA
			simulation	0.477	0.573	10.59	nA

Table 27 Simulation results for the high-to-low level-shifter

[9] current consumption during one switching period, both supply currents together

Parameter	Symbol	Condition		min	typ	max	unit
propagation delay rising	tprop_r	@ 3.3 MHz	specification			3.5	ns
			simulation	0.57	0.78	1.63	ns
propagation delay falling	tprop_f	@ 3.3 MHz	specification			3.5	ns
			simulation	0.83	1.112	1.95	ns
rise time	tr	@ 3.3 MHz	specification			500	ps
			simulation	72.04	100.8	157.8	ps
fall time	tf	@ 3.3 MHz	specification			500	ps
			simulation	59.05	77.26	117.7	ps
supply	I_dynamic_sum	@ 3.3 MHz	specification			15	µA
			simulation	7.754	10.02	12.44	µA
supply	I_static_sum	DC	specification			100	nA
			simulation	0.262	0.308	3.859	nA

Table 28 Simulation results for the low-to-low level-shifter for the gate-driver

Parameter	Symbol	Condition		min	typ	max	unit
propagation delay rising	tprop_r	@ 3.3 MHz	specification			3.5	ns
			simulation	0.599	0.824	1.383	ns
propagation delay falling	tprop_f	@ 3.3 MHz	specification			3.5	ns
			simulation	0.758	1.052	1.785	ns
rise time	tr	@ 3.3 MHz	specification			500	ps
			simulation	116.8	159.2	241	ps
fall time	tf	@ 3.3 MHz	specification			500	ps
			simulation	79.37	104.7	160	ps
supply	I_dynamic_sum	@ 3.3 MHz	specification			15	µA
			simulation	6.597	8.593	10.73	µA
supply	I_static_sum	DC	specification			100	nA
			simulation	0.274	317.2	4.112	nA

Table 29 Simulation results for the low-to-low level-shifter for the gate-feedback

Parameter	Symbol	Condition		min	typ	max	unit
propagation delay rising	tprop_r	@ 3.3 MHz	specification			1	ns
			simulation	229.3	330.2	552.9	ps
propagation delay falling	tprop_f	@ 3.3 MHz	specification			1	ns
			simulation	261.2	362.4	578.9	ps
rise time	tr	@ 3.3 MHz	specification			500	ps
			simulation	117.3	165.5	268.9	ps
fall time	tf	@ 3.3 MHz	specification			500	ps
			simulation	117.6	153.1	228.9	ps

Table 30 Simulation results for the Schmitt-trigger

Parameter	Symbol	Condition		min	typ	max	unit
resistance	Ron	Vg=-0.2V, Vs=4.8V, Vd=5V	specification		3		Ω
			simulation	1.537	2.988	3.718	Ω

Table 31 Simulation results for the 28V HV PMOS transistor for the active-diode

Parameter	Symbol	Condition		min	typ	max	unit
supply	Vboot	T=10µs, PW=15ns	specification	4.5	5	5.5	V
			simulation	4.195	4.893	5.533	V
propagation delay rising	tprop_r	T=10µs, PW=15ns	specification			4	ns
			simulation	1.609	2.237	3.666	ns
propagation delay falling	tprop_f	T=10µs, PW=15ns	specification			7	ns
			simulation	2.368	3.621	6.361	ns

Table 32 Simulation results for the active-diode block

Parameter	Symbol	Condition		min	typ	max	unit
input current	Iout_FB	FB_div=0, DC	specification			12	µA
			simulation	6.695	8.354	10.82	µA
input current	Iout_FB	FB_div=1, DC	specification			12	µA
			simulation	6.696	8.354	10.82	µA
output voltage	Vfb	FB_div=0, DC	specification	-0.1%	1.25	+0.1%	V
			simulation	1.25	1.25	1.251	V
output voltage	Vfb	FB_div=1, DC	specification	-0.1%	1.25	+0.1%	V
			simulation	1.25	1.25	1.251	V

Table 33 Simulation results for the feedback

Parameter	Symbol	Condition		min	typ	max	unit
propagation delay rising	tprop_r	@ 3.3 MHz	specification			6	ns
			simulation	2.93	3.6	5.38	ns
propagation delay falling	tprop_f	@ 3.3 MHz	specification			7	ns
			simulation	4.1	5.27	6.92	ns
rise time	tr	@ 3.3 MHz	specification			2	ns
			simulation	0.68	1	1.51	ns
fall time	tf	@ 3.3 MHz	specification			2	ns
			simulation	0.16	0.2	0.27	ns

Table 34 Simulation results for the comparator

Parameter	Symbol	Condition		min	typ	max	unit
bias current	Ib	DC	specification	-2%	1	+2%	µA
			simulation	1	1.001	1.003	µA
bias current	Ib_int	DC	specification	-1%	1	+1%	µA
			simulation	1	1.002	1.005	µA
bias current	Ib_cmp_h	DC	specification	-1%	10	+1%	µA
			simulation	9.999	10.02	10.07	µA
bias current	Ib_cmp_l	DC	specification	-1%	10	+1%	µA
			simulation	9.999	10.02	10.07	µA
bias current	Ib_0.5µA	DC	specification	-1%	500	+1%	nA
			simulation	500.3	501.6	504	nA
bias current	Ib_3µA	DC	specification	-1%	3	+1%	µA
			simulation	3.002	3.01	3.024	µA
hysteresis	hyst50	Hyst0=1, Hyst1=1, @ 3.3 MHz	specification	-1%	50	+1%	mV
			simulation (avg)	50.03	50.11	50.35	mV
hysteresis	hyst25	Hyst0=0, Hyst1=1, @ 3.3 MHz	specification	-1%	25	+1%	mV
			simulation (avg)	25.01	25.05	25.18	mV
hysteresis	hyst10	Hyst0=1, Hyst1=0, @ 3.3 MHz	specification	-1%	10	+1%	mV
			simulation (avg)	10.01	10.02	10.07	mV
hysteresis	hyst5	Hyst0=0, Hyst1=0, @ 3.3 MHz	specification	-1%	5	+1%	mV
			simulation (avg)	5.003	5.011	5.036	mV

Table 35 Simulation results for the hysteretic-comparator

Parameter	Symbol	Condition		min	typ	max	unit
bias current	Ib_L2H	DC	specification	-2%	1	+2%	µA
			simulation	1.001	1.005	1.017	µA
bias current	Ib_L2H_AD	DC	specification	-2%	1	+2%	µA
			simulation	1.001	1.005	1.017	µA
bias current	Ib_H2L	DC	specification	-2%	1	+2%	µA
			simulation	1.001	1.004	1.018	µA
bias current	Ib_HystCMP	DC	specification	-2%	1	+2%	µA
			simulation	1	1.003	1.009	µA

Table 36 Simulation results for the current-bank

For the control-logic the timing between the signals is interesting. Figure 50 shows the timing of the signals.

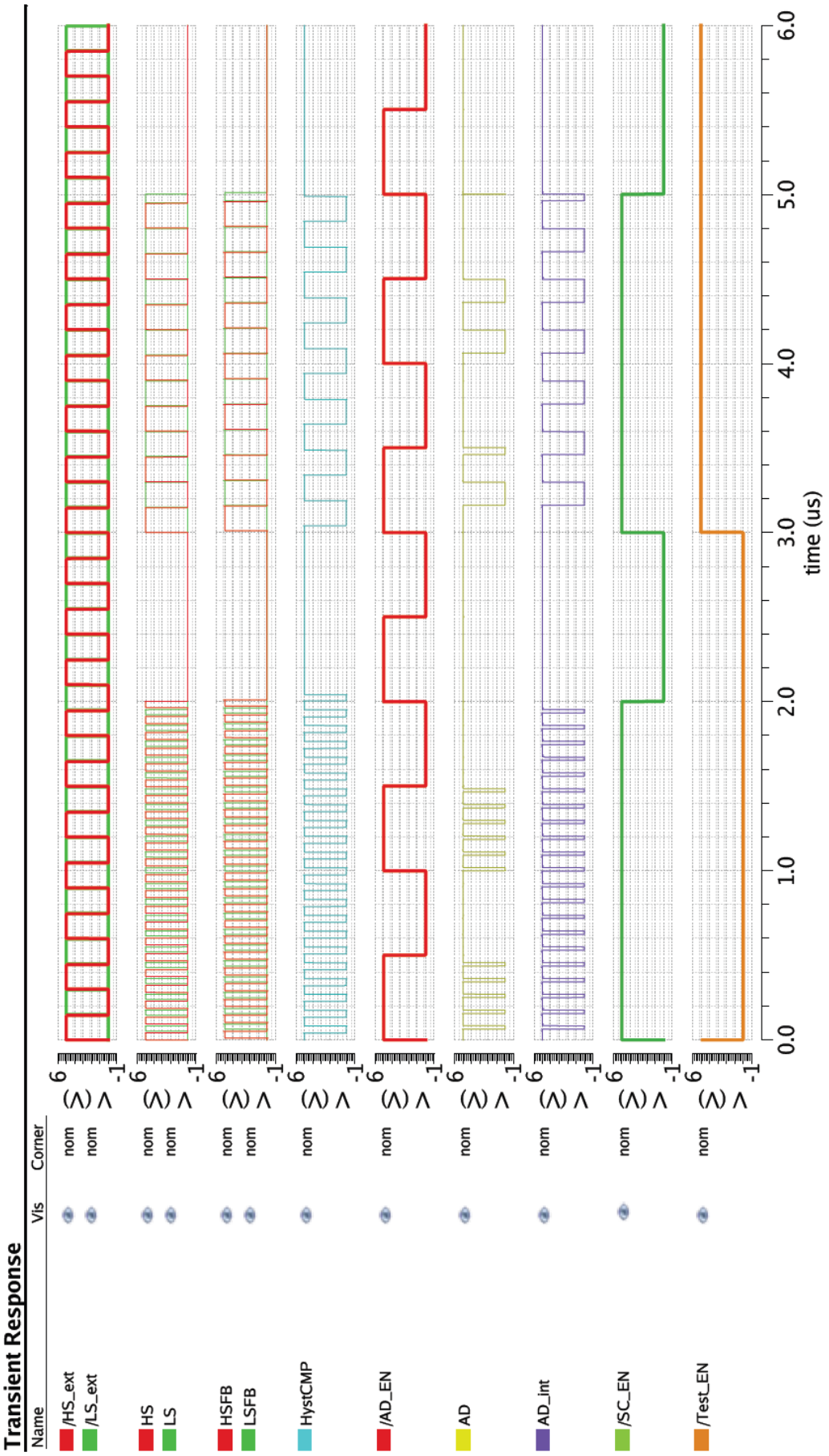

Figure 50 Shows the timing of the different signals from the control logic

3.16. Layout

The layout of the chip is not part of the thesis and has been done by Dialog Semiconductor. The most difficult part of the layout has been the half-bridge especially the high-side-switch. Depending on the package which is a thirty-two pins MQFN it is necessary to watch out for the bond-wires and the pads. Because this fact the pad placement is severely restricted. After the placement of the pads different solutions for the wiring in the metal layers have been tried. The problem is the fact that the high-side-switch and the low-side-switch are formed by multiple instances of the same IP-block. This limits the possible arrangements of the blocks in conjunction with the pads. The current has to flow uniformly between the V_{in} and Lx pads for the high-side-switch and also for the low-side-switch between Lx and Vssp. In order to optimize the switching function of the NMOS all the fingers of the transistor should have the same amount of source-drain current. The input voltage is provided by six pads which are vertically aligned. The Lx node is also provided by six pads which are horizontally aligned. The goal is to reduce the offset between the current flow of the six pads of the input voltage and the six pads of the Lx node. One pad should not carry more than 600mA. Several iterations were done until a practical solution has been reached.

Figure 53, Figure 55 and Figure 57 show the current distribution in A/µm² for the metal 6 layer and they also show the pads for the input voltage and the Lx node. The distribution should increase lineary from the first V_{in} pad (on the top of a figure) to the Lx pads over the whole width of the metallisation. It can be seen that this is not the case.

Figure 54, Figure 56 and Figure 58 show the source-drain current in A/µm for the diffusion layer and vertically aligned the V_{in} pads (the first pad is on the top). The optimum for the diffusion layer would be a uniform distribution. It can be seen that this not the case. The optimum would be that the whole figure shows the same colour (ideally green). The red regions are problematic because the current is too high and this decreases the lifetime of the transistor.

The used tool for these simulations is called R3D[10].

[10] For more information about the R3D tool please visit http://www.siliconfrontline.com/products/r3d/

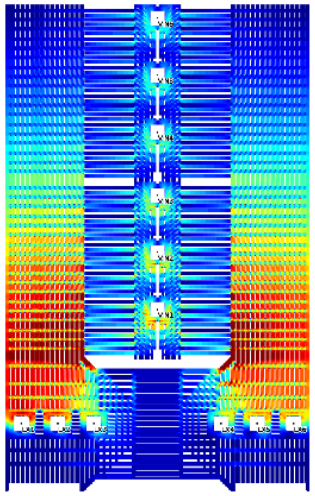

Figure 57 Shows the 1st version of the wiring in layer 6

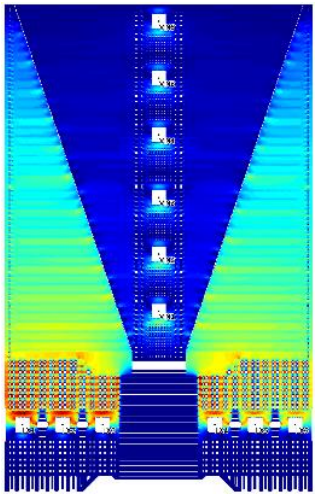

Figure 55 Shows a different approach for the wiring in layer 6

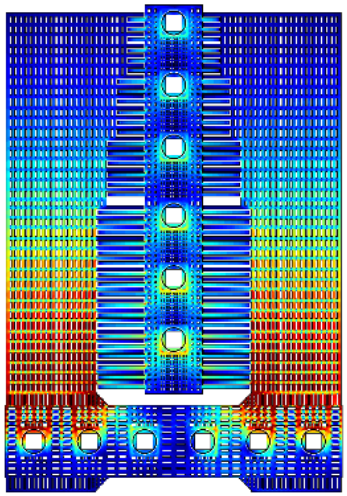

Figure 53 Shows the final version of the wiring in layer 6

Figure 51 Shows the scale: blue (0) – red (0.005)

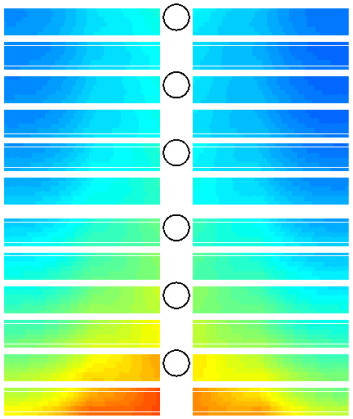

Figure 58 Shows the source-drain current distribution for the 1st version

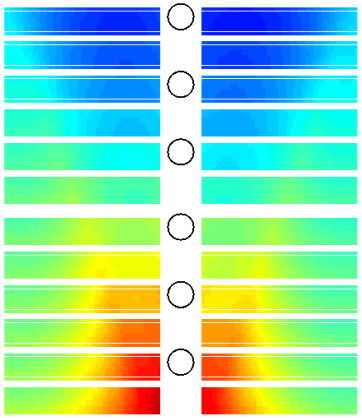

Figure 56 Shows the source-drain current distribution for a different approach

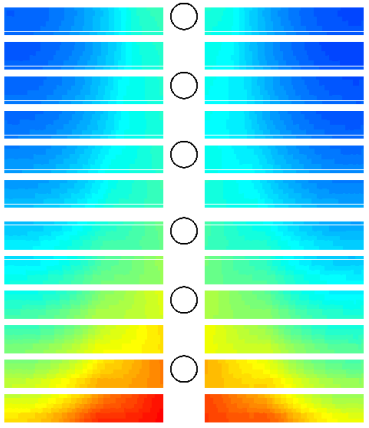

Figure 54 Shows the final source-drain current distribution of the final version

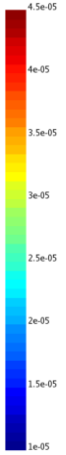

Figure 52 Shows the scale: blue (1e-5) – red (4.5e-5)

Table 37 shows the result for the 3 different wiring options in the metal layers. It is necessary to say that the results are only approximate values because the tool needs a lot of parameters and many of them are estimated because they are unknown until the testchip is manufactured.

Current @ pad	1st version [mA]	Different approach [mA]	Final version [mA]
Lx 1	657.78	700.1	672.91
Lx 2	590.39	637.02	572.14
Lx 3	537.21	591.19	485.24
Lx 4	451.38	488.65	457.64
Lx 5	438.76	461.55	471.28
Lx 6	420.81	434.24	469.17
Vin 1	646.23	609.25	642.47
Vin 2	582.12	579.96	585.33
Vin 3	527.55	557.03	534.04
Vin 4	482.75	536.84	489.54
Vin 5	446.42	521.62	454.25
Vin 6	411.27	508.04	422.75

Table 37 Shows the current through the V_{in}- and Lx-pads

It can be seen that the balance between the six pads of the input voltage and the Lx node is still not perfect. For a better distribution it would be necessary to use another package type.

Figure 59 shows the floor plan of the testchip. A floor plan is necessary to have an overview and it is also a guide for the placement of the sub-blocks. For all blocks area estimation is done and then the blocks are pre-placed. During the layout the area estimations are replaced by the finalized values and floor plan is updated if the difference between estimation and finalized values is too high.

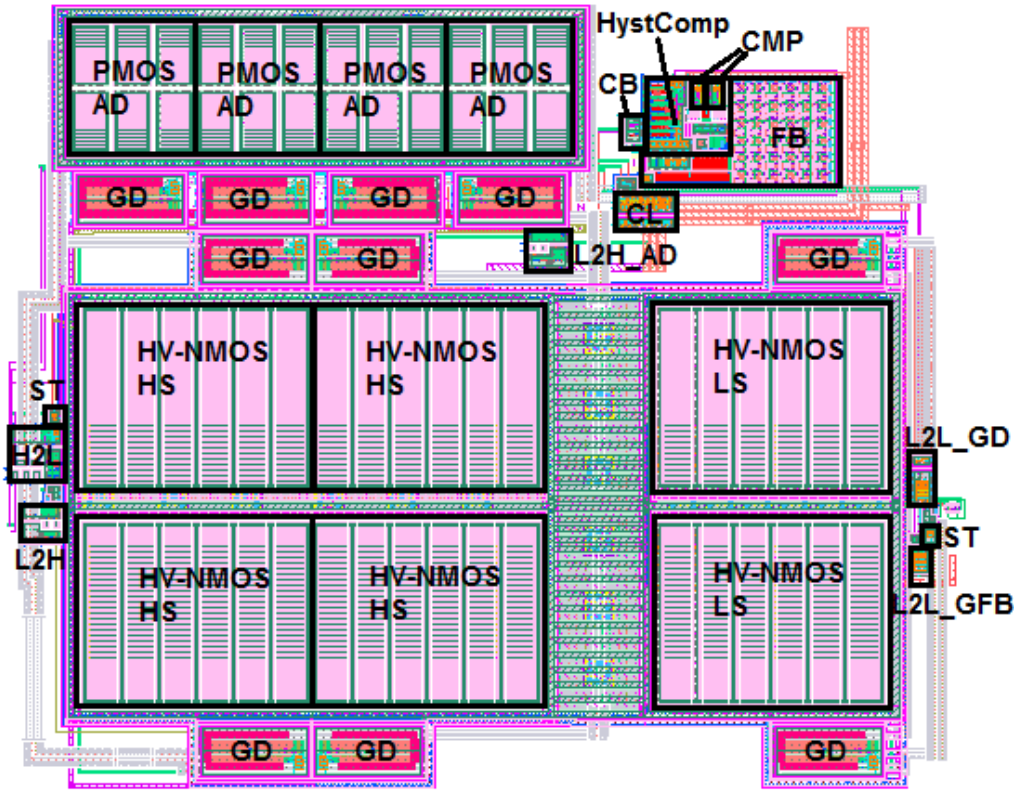

Figure 59 Shows the floor plan of the entire design

Table 38 shows the pin allocation of the testchip:

Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	Test_EN	9	n.c.	17	Vddp	25	Vss
2	n.c.	10	Vin	18	nwell_LS	26	Vddt
3	SC_EN	11	Vin	19	HS_ext	27	Ib
4	AD_EN	12	Lx	20	LS_Ext	28	Vref
5	n.c.	13	Lx	21	HSFB_CMP	29	FB_div
6	n.c.	14	Vssp	22	LSFB_AD	30	Vdd
7	n.c.	15	Vssp	23	n.c.	31	Hyst0
8	Vboot	16	Vout_FB	24	Out_Sel	32	Hyst1

Table 38 Pin allocation of the testchip

Figure 60 shows the final layout for the testchip with pads and ESD protection.

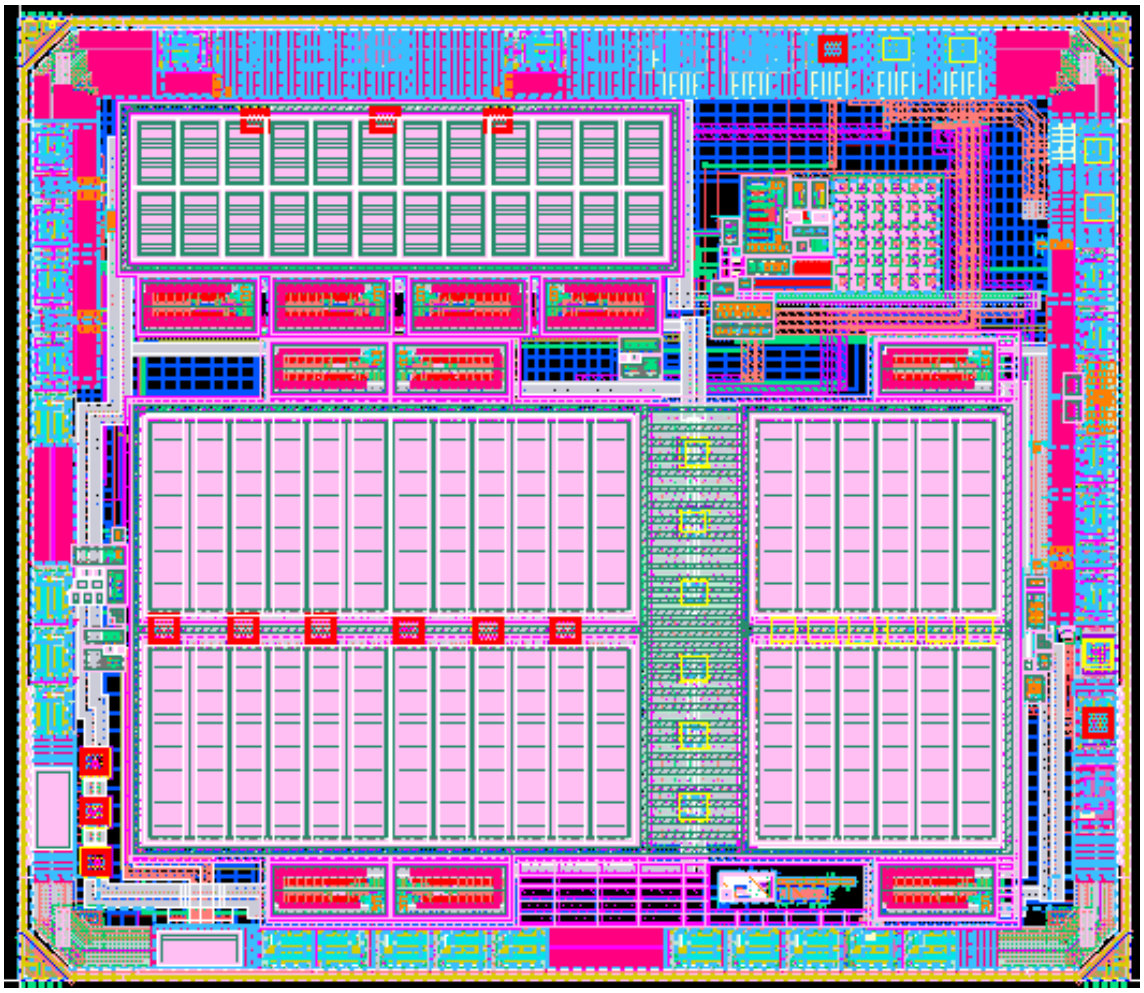

Figure 60 Shows the final layout of the testchip

4. Conclusion

A front-end for a high voltage DC-DC buck converter was designed for an input voltage range of 5V to 20V and an output voltage from 2.5V to 5V. A hysteretic control loop was designed which gives a variable switching frequency of the converter dependent on the input voltage, the output voltage, the delays of the system and the ESR of the output capacitor (Equation 33, 34).

Based on the facts that there are no fixed switching frequency and duty-cycle it was very difficult to design the active-diode. The results of the corner simulations from the active-diode block show that it is not possible to keep the specification for all corners. V_{boot} failed in many corners.

Also the fast rising and falling of the Lx node between 0V and V_{in} made the design difficult. It is necessary to have a close look on the SOAs of the transistors in the level-shifters and the other sub-blocks which are supplied by V_{boot} because it is also rising and falling fast dependent on the Lx node.

The test chip is fabricated in a 130nm BCD process. There is no praxis experience regarding the used high voltage transistors in this process. The evaluation of the designed front-end will give some experience for new designs.

5. Outlook

Some improvements could be done. At the moment it is not possible to disable (power down) the level-shifters low-to-high and low-to-high used to control active-diode. This increases the current consumption during the power down state of the chip.

During the design of the low-to-high level-shifter different topologies were tried out. A test chip with different level-shifter topologies is a good idea to see the advantages and disadvantages of the different topologies.

The integrated feedback dividers have large capacitors. Another topology may help save area or an external circuit can be used.

6. Registers

6.1. Table of figures

6.2. List of tables

7. Glossary

BCD process ..... Bipolar CMOS DMOS process

CMOS ..... Complementary Metal–Oxide–Semiconductor

DMOS ..... Double-diffused Metal–Oxide–Semiconductor

LDO ..... Low Dropout Voltage Regulator

NMOS ..... n-channel MOSFET

PMOS ..... p-channel MOSFET

MOSFET ..... Metal–Oxide–Semiconductor Field-Effect Transistor

CCM ..... Continuous Conduction Mode

DCM ..... Discontinuous Conduction Mode

VMC ..... Voltage Mode Control

CMC ..... Current Mode Control

GD ..... Gate-Driver

Lx node ..... output node from the switches to the coil

HSS ..... High-Side-Switch

LSS ..... Low-Side-Switch

HS ..... High-Side

LS ..... Low-Side

LS-xxx ..... Level-Shifter

L2H ..... Low-to-High

H2L ..... High-to-Low

L2L ..... Low-to-Low

CL ..... Control-Logic

ST ..... Schmitt-Trigger

CMP .....Comparator

FB .....Feedback

ZC .....Zero-Cross

IP.....Intellectual Property

Nx.....5V NMOS transistor

Mx .....5V PMOS transistor

PNx .....high voltage NMOS transistor

PMx.....high voltage PMOS transistor

SOA .....Safe-Operating-Area

7.1. Symbols

Symbol	Unit	Declaration
η	[1]	efficiency
100.η	[%]	efficiency
f	[Hz]	frequency
T	[s]	period time (1/f)
D	[1]	duty cycle
100.D	[%]	duty cycle
V_{in}	[V]	input voltage
V_{out}	[V]	output voltage
V_{ref}	[V]	reference voltage
V_{boot}	[V]	high-side supply
Vdd	[V]	supply
Vddp	[V]	low-side supply

Lx ≙ Vssh	[V]	external connection for the coil between high-side and low-side, high-side ground
Vss	[V]	ground
Vssp	[V]	low-side ground
C_{boot}	[F]	capacitor for high-side power supply
L	[H]	coil for buck converter
C	[F]	capacitor for buck converter
t_{load}	[s]	period time for loading C_{boot}
V_H	[V]	hysteresis-voltage
Vh	[V]	upper hysteresis threshold-voltage
Vl	[V]	lower hysteresis threshold-voltage
I_L	[A]	current through the external coil

8. Bibliography

[1]. **Robert W. Erickson, Dragan Maksimovic.** Fundamentals of Power Electronics *Second Edition*. 31.January 2001 ISBN-13: 978-0-7923-7270-7 Springer 2nd edition

[2]. **Christophe P. Basso.** Switch-Mode Power Supplies: SPICE Simulations and Practical Designs. 1.February 2008 ISBN-13: 978-0-07-150858-2 Mcgraw-Hill Professional Har/Cdr edition

[3]. **Phillip E. Allen, Douglas R. Holberg.** CMOS Analog Circuit Design (Oxford Series in Electrical and Computer Engineering). January 1987 ISBN: 0-19-510720-9 Oxford University Press Inc

[4]. **Richard Redl.** Advanced Engineering Course on Power Management. *EPFL Premises, Lausanne, Switzerland* August 29 – September 2, 2011

[5]. **Ned Mohan, Tore M. Undeland, William P. Robbins.** Power Electronics. 8. November 2002 ISBN-13: 978-0471226932 John Wiley & Sons 3rd edition

[6]. **Brian Lynch (Texas Instruments Incorporated).** Current-Mode Vs. Voltage-Mode Control In Synchronous Buck Converters. http://www.analogzone.com/pwrt0407.pdf (15.03.2013)

[7]. **Robert Mammano (Texas Instruments, Design Note).** Switching Power Supply Topology Voltage Mode vs. Current Mode. https://ps-ssl.de/regiamea.de/ablage/dn-62.pdf (15.03.2013)

[8]. **Stephan Dobretsberger, Bernhard Mayr.** A Low Power High Speed Level Shifter Design for up to 40V. *Austrochip 2010* October 6, 2010

[9]. **IFE (Institut für Elektronik).** Diplom-/Masterarbeiten. http://www.ife.tugraz.at/~ife/sites/default/files/MasterThesis_Frond-end_for_high_voltage_dcdc_converter.pdf (13.05.2013)

[10]. **Ulrich Tietze, Christoph Schenk.** Halbleiter-Schaltungstechnik *12.Auflage*. 2002 ISBN: 3-540-42849-6 Springer 12th edition

[11]. **Chester Simpson (National Semiconductor, Application Note).** Linear and Switching Voltage Regulator Fundamentals. http://www.ti.com/lit/an/snva558/snva558.pdf (17.09.2013)

[12]. **Chester Simpson (National Semiconductor, Application Note).** Linear and Switching Voltage Regulator Fundamentals. http://www.ti.com/lit/an/snva559/snva559.pdf (17.09.2013)

[13]. **Alan Hastings.** The Art of Analog Layout *Second Edition*, May 2005 ISBN-13: 978-0131464100 Prentice Hall 2nd edition

[14]. **R. Jacob Baker.** CMOS: Circuit Design, Layout, and Simulation *(IEEE Press Series on Microelectronic Systems),* October 2010 ISBN-13: 978-0470881323 John Wiley & Sons 3rd edition