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Analog Front-Ends for HF/UHF Dual Band RFID Transponders

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Kurzfassung

Kontaktlose Chipkarten haben eine große Verbreitung, vor allem in elektronischen Zahlungssystemen für den öffentlichen Nahverkehr, gefunden. Die dabei eingesetzte passive HF Radiofrequenz-Identifikations-Technologie (RFID), erlaubt eine Kommunikation zwischen einem Lesegerät und einem batterielosen Transponder, über eine Distanz von bis zu 10 cm. Die starke magnetische Kopplung bei dieser niedrigen Distanz zum Lesegerät ermöglicht eine ausreichende Energieversorgung für einen Transponder-IC, um komplexe kryptographische Funktionen – zur Betrugsbekämpfung und zum Schutz der Privatsphäre der Benutzer – auszuführen. Die begrenzte Kommunikationsreichweite erfordert andererseits, dass Benutzer ihre Chipkarte in geringe Distanz an ein Lesegerät bewegen müssen, um eine Transaktion durchzuführen. Dieser Vorgang wird in bestimmten Situationen als unbequem empfunden, wie zum Beispiel, vor dem Aussteigen aus einer Straßenbahn oder einem Bus. UHF RFID-Technologie, als eine Alternative, ermöglicht Kommunikationsreichweiten von mehreren Metern. Jedoch ist die verfügbare Leistung an einem UHF RFID-Transponder um Größenordnungen geringer als im Falle von HF RFID-Transpondern, was die Umsetzung von komplexen Funktionen zur Gewährleistung der Datensicherheit stark einschränkt.

Diese Doktorarbeit behandelt HF/UHF Dualband-RFID-Transponder für Zutrittskontrollsysteme und im Speziellen für elektronische Zahlungssysteme im öffentlichen Verkehr. Die UHF RFID-Schnittstelle ist vorgesehen, um eine Ferndetektion von Passagieren zu ermöglichen und damit den Ausstiegspunkt von Passagieren feststellen zu können. Im Anschluss an eine Diskussion der herausfordernden Einsatzbedingungen hinsichtlich der UHF RFID-Kommunikation, beschreibe ich konzeptionell die Architektur eines HF/UHF Dualband-RFID-Transponder-ICs. Die zentralen Anforderungen und Einschränkungen im Hinblick auf die analogen HF- und UHF RFID-Frontends werden besprochen, mit Betonung auf Fragen der fortschreitenden Skalierung von CMOS-Prozessen.

Im Nachfolgenden lege ich den Schwerpunkt auf die Schaltungsumsetzung von UHF RFID-Frontends, in einer 40 nm CMOS-Technologie für energiekritische Anwendungen. Die Schaltungsdesigns beruhen ausschließlich auf Transistortypen mit geringem Leckstrom und erhöhter Schwellspannung (V_{th}), die speziell dazu geeignet sind, die Leistungsaufnahme von digitalen Schaltungsblöcken zu minimieren. Die Wahl der Technologie zielt auf eine kosteneffiziente Gesamtumsetzung eines Transponder-ICs ab. Ich stelle drei differentielle RF/DC-Wandler, mit interner V_{th}-Kompensation, vor. Die eingeführte V_{th}-Kompensation erhöht die Effizienz der Leistungsumsetzung und reduziert den Gütefaktor am Eingang der RF/DC-Wandler bei geringer Eingangsleistung. Ein temperaturkompensierter DC-Spannungsbegrenzer reguliert die Ausgangsspannung der RF/DC-Wandler gegenüber einer sich ändernden Eingangsleistung. Zusätzlich dazu führe ich zwei RF-Spannungsbegrenzer ein, die das Risiko von Überspannungen an einem UHF RFID-Frontend, bei hoher Eingangslei-

stung, reduzieren können. Die RF-Spannungsbegrenzer sind, insbesondere im Hinblick auf die reduzierten Betriebsspannungen in fortschrittlichen CMOS-Technologien, von Relevanz.

Anhand von Messergebnissen zweier gefertigter UHF RFID-Frontends, demonstriere ich die Funktionalität der diskutierten Schaltungsblöcke. Die beiden Frontends erreichen eine Wandlungseffizienz von 38 % und 41 %, bei einer geringen Eingangsleistung von ungefähr −20 dBm. Der Gütefaktor der beiden Schaltungen in diesem Arbeitspunkt beträgt weniger als 16. Die beiden Frontends ermöglichen damit eine breitbandige UHF RFID Schnittstelle mit hoher Empfindlichkeit und unterstützen somit die Zuverlässigkeit der UHF RFID Kommunikation in dem herausfordernden Anwendungsszenario.

Abstract

Contactless smart cards have gained a wide spread adoption in automatic fare collection (AFC) systems for public transportation. The utilized HF radio frequency identification (RFID) technology allows communication between a reader and a batteryless transponder (tag) over a distance of up to 10 cm. The strong magnetic coupling at such a low distance to the reader allows the supply of sufficient power to a tag IC to perform sophisticated security operations to counteract fraud and safeguard the users' privacy. On the other hand, the limited communication range requires users to move the smart card in close proximity to the reader for performing a transaction. This procedure is perceived to be inconvenient in certain situations such as before alighting from a tram or a bus. UHF RFID technology, as a potential alternative, enables communication ranges of several meters. Nevertheless, the available power to supply a UHF RFID tag IC is magnitudes lower than the available power for a HF RFID tag IC, constraining the implementation of complex security functions.

This thesis considers HF/UHF dual band RFID transponders for access control systems and in particular for AFC. The UHF RFID interface is envisaged to allow a remote detection of passengers, and thus to determine the alighting point of passengers. Following a review of the demanding operating conditions of the UHF RFID link, I outline the architecture of a secured HF/UHF dual band RFID transponder IC from a conceptual point of view. The major requirements and constraints concerning the HF and the UHF RFID analog front-ends are investigated with emphasis on questions of the progressing CMOS technology scaling.

Subsequently, I focus on circuit implementations of UHF RFID front-ends in a low-power 40 nm CMOS technology. The circuit designs use exclusively low-leakage transistors with a raised threshold voltage (V_{th}), which are particularly useful for minimizing the power consumption of digital circuit blocks. The technology choice aims at achieving an overall cost-efficient implementation of a transponder IC. I present three differential RF-DC power converters with an internal V_{th} compensation. The introduced V_{th} compensation enhances the power conversion efficiency and lowers the input quality factor of the RF-DC power converters at low levels of input power. A temperature compensated DC voltage limiter regulates the output voltage of the RF-DC power converters versus a varying input power. Furthermore, I introduce two RF voltage limiters that diminish the risk of overvoltage at a UHF RFID front-end at high levels of input power. The RF voltage limiters are particularly important regarding the reduced maximum voltage ratings in scaled CMOS technologies.

Experimental results of two manufactured UHF RFID front-ends demonstrate the performance of the discussed circuit blocks. The two front-ends achieve a high power conversion efficiency of 38 % and 41 %, respectively, at a low input power of around -20 dBm. The quality factor of the two circuits at this operating point is lower than 16. The two front-ends therefore enable a highly sensitive broadband UHF RFID interface, and consequently facilitate the reliability of the UHF RFID link in the challenging application scenario.

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Contents

Acronyms

3b/8b	3 bit to 8 bit encoding
4b/16b	4 bit to 16 bit encoding
AES	Advanced Encryption Standard
AFC	Automatic fare collection
ASK	Amplitude shift keying
BLE	Bluetooth Low Energy
BPSK	Binary phase shift keying
CID	Card identification number
CIU	Contactless interface unit
CMOS	Complementary metal oxide semiconductor
COID	One-time card identification number
CPU	Central processing unit
CW	Continuous wave
DC	Direct current
DSB-ASK	Double-sideband amplitude shift keying
e-ticketing	Electronic ticketing
ECC	Elliptic curve cryptography
EEPROM	Electrically erasable programmable read-only memory
EMC	Electromagnetic compatibility
EPC	Electronic Product Code
ESD	Electrostatic discharge
FM0	Bi-phase space encoding
FSK	Frequency shift keying
GSSG	Ground-signal-signal-ground
HF	High frequency
HVQFN	Heatsink very-thin quad flat-pack no-leads
I/O	Input/output
IC	Integrated circuit

ID-1	Size of an identification card ($85.60 \times 53.98\,mm^2$) as defined in the standard ISO/IEC 7810
JLCC	J-leaded ceramic chip carrier
LF	Low frequency
LOS	Line of sight
LRRM	Line-reflect-reflect-match
MFM	Modified frequency modulation
MOS	Metal oxide semiconductor
NFC	Near field communication
NMOS	n-type metal oxide semiconductor
NRZ-L	Non-return-to-zero level
NVM	Non-volatile memory
OCR	Optical character recognition
OOK	On-off keying
OTA	Operational transconductance amplifier
p-n junction	p-doped/n-doped semiconductor junction
PCB	Printed circuit board
PIE	Pulse interval encoding
PJM	Phase jitter modulation
PLL	Phase-locked loop
PMOS	p-type metal oxide semiconductor
PPM	Pulse position modulation
PR-ASK	Phase-reversal amplitude shift keying
PSK	Phase shift keying
PTAT	Proportional to absolute temperature
RAM	Random-access memory
RF	Radio frequency
RFID	Radio frequency identification
RMS	Root mean square
ROM	Read-only memory
S	Scattering
SMA	Sub-miniature version A
SMS	Short Message Service
SMU	Source measure unit
SOS	Silicon on sapphire
SSB-ASK	Single-sideband amplitude shift keying
tag	RFID transponder
UHF	Ultra high frequency

VHBR	Very high bit rates
VNA	Vector network analyzer

Symbols

A	Area of an HF RFID transponder antenna
C_{B}	Buffer capacitance to supply a passive RFID transponder IC during modulation pulses
C_{ox}	Oxide capacitance per unit area
C_{P}	Equivalent parallel input capacitance of a UHF RFID analog front-end
C_{par}	Additional parasitic capacitance of a UHF RFID analog front-end excluding the RF charge pump
$C_{\mathrm{P,HF}}$	Equivalent parallel input capacitance of an HF RFID analog front-end
C_{S}	Equivalent series input capacitance of a UHF RFID analog front-end
$EIRP$	Equivalent isotropically radiated power
f_0	Carrier frequency
f_{r}	Resonance frequency of an HF RFID transponder
f_{sc}	Subcarrier frequency
G_{int}	RFID interrogator antenna gain
g_{m}	Transconductance of a transistor
G_{tag}	RFID transponder or tag antenna gain
$G_{\mathrm{tag,r}}$	Realized antenna gain of an RFID transponder
H_{min}	Minimum equivalent homogenous magnetic field strength that is required to operate an HF RFID transponder
I_0	Drain-source current at the upper limit of the weak inversion region normalized to W/L
I_{DC}	Output current of the RF-DC power converter of a UHF RFID analog front-end
I_{DL}	Input current of the DC voltage limiter of a UHF RFID analog front-end

$I_{\mathrm{DL,\,max}}$	Maximum specified input current of the DC voltage limiter of a UHF RFID analog front-end
I_{ds}	Drain-source current of a CMOS transistor
I_{L}	Overall current consumption of the analog and digital circuitry of a transponder IC
k	Boltzmann constant
$\mathrm{K_{GK}}$	Secret group key that enables a mutual authentication between a smart card and a reader
$\mathrm{K_{TMP}}$	Temporary key for encrypting the response of a smart card via the UHF RFID interface
L	Gate length of a CMOS transistor
L_{A}	Antenna inductance
$L_{\mathrm{A,\,HF}}$	Inductance of an HF RFID transponder antenna coil
L_{min}	Minimum gate length of a CMOS transistor
m	Modulation index
N	Number of turns of an HF RFID transponder antenna coil
n	Index for charge pump stages
N_{st}	Number of stages of an RF charge pump
n_{sub}	Subthreshold slope coefficient
p	Loss factor quantifying the polarization mismatch between two antennas
P_{av}	Available power at an RFID transponder antenna
$P_{\mathrm{av,\,min}}$	Minimum required available power to operate an RFID transponder
P_{d}	Dissipated power at the rectifying devices of an RF charge pump
$P_{\mathrm{DC,\,HF}}$	DC output power of the rectifier of an HF RFID analog front-end
P_{DC}	DC output power of the RF charge pump of a UHF RFID analog front-end
$P_{\mathrm{DC,\,min}}$	Minimum DC power required to supply the core circuitry of a transponder IC
P_{in}	RF input power of a UHF RFID analog front-end
$P_{\mathrm{in,\,HF}}$	RF input power of an HF RFID analog front-end
$P_{\mathrm{int,\,min}}$	Sensitivity of an RFID interrogator
$P_{\mathrm{int,\,TX}}$	Transmitting power of an RFID interrogator

P_{L}	Overall power consumption of the analog and digital circuitry of a transponder IC
P_{min}	Minimum RF input power that is required to operate a UHF RFID transponder IC or alternatively the sensitivity of the IC
$P_{\mathrm{min,\,HF}}$	Minimum RF input power that is required to operate an HF RFID transponder IC or alternatively the sensitivity of the IC
Q	Input quality factor of a UHF RFID analog front-end
q	Elementary charge
Q_{HF}	Quality factor of an HF RFID transponder
R_{A}	Antenna resistance
r_{ds}	Small-signal drain-source resistance of a transistor
R_{L}	Load resistance at the DC output of an RF charge pump
R_{max}	Maximum operating distance of a UHF RFID transponder
$R_{\mathrm{max,\,HF}}$	Maximum operating distance of an HF RFID transponder
R	Distance between an RFID reader and a transponder
$R_{\mathrm{max,\,rev}}$	Maximum range of the reverse communication link between a UHF RFID transponder and a reader
R_{P}	Equivalent parallel input resistance of a UHF RFID analog front-end
$R_{\mathrm{P,\,CP}}$	Equivalent parallel input resistance of the RF charge pump of a UHF RFID analog front-end
$R_{\mathrm{P,\,D}}$	Equivalent parallel input resistance of the ESD diodes and the backscatter modulator of a UHF RFID analog front-end
$R_{\mathrm{P,\,HF}}$	Equivalent parallel input resistance of an HF RFID analog front-end
$R_{\mathrm{P,\,L}}$	Equivalent parallel input resistance of the RF voltage limiter circuit of a UHF RFID analog front-end
$\mathrm{R_R}$	Random token that is transmitted by a reader to a transponder
$\mathrm{R_T}$	Random token that is generated by a transponder to send a response to a reader
R_{S}	Equivalent series input resistance of a UHF RFID analog front-end
T	Ambient temperature
T_0	Carrier period

T_K	Absolute temperature in °K
T_m	Duration of a modulation pulse
$\hat{V}_\mathrm{A}$	Open circuit antenna voltage
V_DC	DC output voltage of the RF-DC power converter of a UHF RFID analog front-end
$V_\mathrm{DC,HF}$	DC output voltage of the rectifier of an HF RFID analog front-end
$V_\mathrm{DC,max}$	Maximum voltage level at the storage capacitor of a transponder IC
$V_\mathrm{DC,min}$	Minimum required voltage level at the storage capacitor of a transponder IC to provide a stable supply for the core circuitry
$V_\mathrm{DDI,HF}$	Supply voltage of the core circuitry of an HF RFID transponder IC
$V_\mathrm{DD,max}$	Maximum supply voltage for the thin-oxide core transistors
$V_\mathrm{DD,nom}$	Nominal supply voltage for the thin-oxide core transistors
V_ds	Drain-source voltage of a CMOS transistor
V_gs	Gate-source voltage of a CMOS transistor
$\hat{V}_\mathrm{in}$	Voltage amplitude at the input of a UHF RFID analog front-end
$\hat{V}_\mathrm{in,HF}$	Voltage amplitude at the input of an HF RFID analog front-end
$\hat{V}_\mathrm{min,HF}$	Minimum input voltage amplitude that is required to operate an HF RFID transponder IC
$V_\mathrm{I/O,max}$	Maximum supply voltage for the thick-oxide I/O transistors
$V_\mathrm{I/O,nom}$	Nominal supply voltage for the thick-oxide I/O transistors
V_sb	Source-bulk voltage of a CMOS transistor
V_t0	Extrapolated threshold voltage for zero inversion layer charge
V_th	Threshold voltage of a CMOS transistor
W	Gate width of a CMOS transistor
Z_0	Characteristic impedance
Z_A	Antenna impedance
Z_IC	Input impedance of a transponder IC or front-end
α	Multiplication factor accounting for the specific modulation characteristics of a backscatter modulated signal
γ	Body effect coefficient

Γ	Reflection coefficient at the IC antenna interface of a transponder
Γ_1	Reflection coefficient depending on the first modulator state of a transponder IC
Γ_2	Reflection coefficient depending on the second modulator state of a transponder IC
Γ_m	Maximum acceptable reflection coefficient at the IC antenna interface of a transponder within a specific frequency bandwidth
Δf_HF	Frequency bandwidth of an HF RFID transponder
$\Delta P_\mathrm{av,\,min}$	Relative loss in the sensitivity of a UHF RFID front-end considering modulated waveforms in comparison to continuous wave signals
ΔQ_HF	Difference of the quality factor between the modulating and the non-modulating state of an HF RFID transponder
$\Delta\sigma$	Differential radar cross section
$\Delta\omega_\mathrm{m}$	Angular frequency bandwidth of the impedance match between an antenna and a UHF RFID transponder IC
η	Power conversion efficiency of an RF charge pump or a UHF RFID analog front-end
η_HF	Power conversion efficiency of the rectifier of an HF RFID analog front-end
λ	Wavelength
$\lambda_{\Delta\mathrm{L}}$	Parameter quantifying the channel-length modulation effect of a CMOS transistor
μ_0	Permeability of free space
μ_n	Charge carrier mobility of electrons
μ_p	Charge carrier mobility of holes
τ	Power transmission coefficient
Φ_0	Surface potential at the oxide-semiconductor interface of a MOS structure in strong inversion
Φ_t	Thermal voltage
ω	Angular frequency
ω_0	Angular carrier frequency
ω_r	Angular resonance frequency of an HF RFID transponder

1 Introduction

Radio frequency identification (RFID) describes a broad range of communication technologies that not only differ in the utilized carrier frequencies, but also in the fundamental physical operating principles. Low frequency (LF) and high frequency (HF) RFID systems are based on magnetic coupling between the antenna coils of an RFID reader or interrogator and an RFID transponder (tag) [1]. Therefore, LF and HF RFID systems only operate in the antenna near field. In contrast to this, ultra high frequency (UHF) RFID systems operate in the antenna far field, and utilize electromagnetic radiation for signaling [2]. Furthermore, RFID systems can be distinguished by means of how power is provided for operating a transponder integrated circuit (IC) and for the data communication from a transponder back to an interrogator. Active transponders incorporate an energy storage such as a battery while passive transponders are entirely powered by the magnetic or electromagnetic field that is emitted by an interrogator [1].

According to their respective characteristics, different types of RFID systems have found specific areas of application. The utilization of UHF frequencies around 900 MHz, for example, allows the construction of compact tag antennas and to achieve communication ranges of several meters for passive tags making them suitable for the tracking of goods in logistic applications [3] or for item-level inventorying in retail stores [4]. On the contrary, the maximum range of proximity HF RFID transponders operating at 13.56 MHz is typically lower than 10 cm due to the rapid decline of the magnetic near field with distance from the reader antenna. The higher level of available power at such a low distance from the reader antenna however allows the supply of passive transponders that provide sophisticated security features as required for banking applications, electronic ticketing or automatic fare collection (AFC) in public transport [1].

HF RFID enabled or contactless smart cards have gained a wide spread use in AFC systems in metropolitan regions since the start of the first pilot projects in the 1990s [5, 6]. A passenger has to move his smart card in close proximity to an RFID reader to perform a transaction and to validate his ticket when entering or alighting from a vehicle such as a bus. As alternatives to HF RFID, communication technologies like Bluetooth Low Energy (BLE) [7, 8] or passive UHF RFID [9], for example, have been investigated recently for the application in AFC systems. These alternative technologies aim at enhancing user comfort by enabling a remote data link between the AFC equipment and the mobile phone or smart card of a passenger without requiring the passenger to perform a conscious action.

This thesis investigates the feasibility of passive HF/UHF dual band RFID transponder ICs for AFC applications with a focus on the analog radio frequency (RF) front-end. Specifically, circuit implementations in a 40 nm low-power complementary metal oxide semiconductor (CMOS) technology are investigated, taking into consideration the progress of CMOS technology scaling, and thus economic aspects of manufacturing advanced transponder ICs.

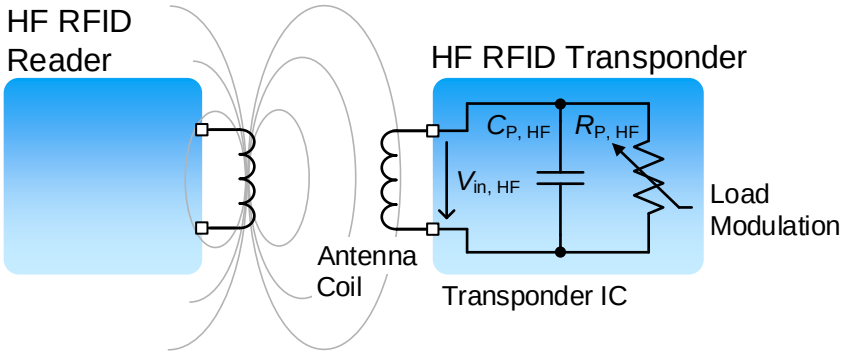


Figure 1.1: Operating principle of passive HF RFID systems. The transponder coil and the input capacitance of the connected transponder IC $C_{P,HF}$ build a parallel resonance circuit with a resonance frequency f_r that is typically close to the operation frequency of 13.56 MHz.

1.1 Passive RFID Technology

The operation without a battery implies an advantage for passive RFID transponders when it comes to cost and lifetime in comparison to active RFID and other communication technologies [1]. Especially, the low costs have been a key factor in enabling the large scale adoption of passive HF as well as UHF RFID technologies in cost sensitive applications such as AFC or logistics.

1.1.1 HF RFID Systems

HF RFID systems comprise a number of communication standards that primarily utilize an operating frequency of 13.56 MHz. These standards differ, for example, in the used modulation schemes or bit rates, and are specifically tailored for achieving certain communication ranges. Despite these differences, the basic operating principle remains the same.

Figure 1.1 illustrates the operating principle of passive HF RFID systems. The magnetic field that is emitted by the reader antenna induces a voltage in the tag antenna coil. The induced voltage is passively amplified by a parallel resonance circuit at the input of the tag, and rectified to provide a voltage supply for a tag IC. The inductance of the tag antenna $L_{A,HF}$ and the equivalent parallel input capacitance of the tag IC $C_{P,HF}$ define the angular resonance frequency of the tag ω_r or the resonance frequency f_r [10]:

$$\omega_r = \frac{1}{\sqrt{L_{A,HF} C_{P,HF}}},\ f_r = \frac{1}{2\pi\sqrt{L_{A,HF} C_{P,HF}}}. \tag{1.1}$$

The bandwidth of the resonance circuit Δf_{HF} or the HF transponder eventually can be expressed by means of the quality factor Q_{HF}:

$$\Delta f_{HF} = \frac{f_r}{Q_{HF}}. \tag{1.2}$$

An RFID reader communicates with a transponder by modulating the emitted magnetic field. As indicated by Eqn.1.2, increasing the bandwidth of the transponder, and thus allowing higher bit rates requires lowering Q_{HF}. Neglecting the parasitic capacitance and resistance of the antenna, and the interconnection to the IC, Q_{HF} depends on the equivalent parallel input resistance of the tag IC $R_{\mathrm{P,HF}}$, and the input capacitance $C_{\mathrm{P,HF}}$ [10]:

$$Q_{\mathrm{HF}} = 2\pi f_{\mathrm{r}} C_{\mathrm{P,HF}} R_{\mathrm{P,HF}} = \frac{R_{\mathrm{P,HF}}}{2\pi f_{\mathrm{r}} L_{\mathrm{A,HF}}}. \tag{1.3}$$

In the second part of Eqn.1.3, $C_{\mathrm{P,HF}}$ has been replaced by f_{r} and $L_{\mathrm{A,HF}}$, as implied by Eqn. 1.1. The input resistance $R_{\mathrm{P,HF}}$ can furthermore be expressed in terms of the voltage amplitude at the input terminals of the transponder IC $\hat{V}_{\mathrm{in,HF}}$ and the input power $P_{\mathrm{in,HF}}$:

$$R_{\mathrm{P,HF}} = \frac{\hat{V}^2_{\mathrm{in,HF}}}{2P_{\mathrm{in,HF}}}. \tag{1.4}$$

The power consumption $P_{\mathrm{in,HF}}$, and $R_{\mathrm{P,HF}}$ of an HF transponder change considerably during operation. Typically, $R_{\mathrm{P,HF}}$ shows a strongly non-linear behavior in dependence of $\hat{V}_{\mathrm{in,HF}}$ [11, 12]. The variation of $R_{\mathrm{P,HF}}$ can be caused by changing operating states of the IC or the internal voltage limiter that limits $\hat{V}_{\mathrm{in,HF}}$ in order to protect the circuit from overvoltage.

The minimum input power $P_{\mathrm{min,HF}}$ and the associated voltage amplitude $\hat{V}_{\mathrm{min,HF}}$ that are required to operate the tag IC determine the maximum operating range $R_{\mathrm{max,HF}}$ of a passive tag. $R_{\mathrm{max,HF}}$ thus equals the maximum communication range in the forward link from the reader to the tag. The minimum homogenous magnetic field strength H_{min} is used as an alternative metric for the maximum operating range that is independent of the specific reader antenna ($H_{\mathrm{min}} \sim 1/R^3_{\mathrm{max,HF}}$). Assuming the resonance frequency of a transponder is tuned exactly to the carrier frequency (ω_0=ω_{r}), H_{min} can be estimated as follows [12]:

$$H_{\mathrm{min}} = \frac{\hat{V}_{\mathrm{min,HF}}}{\sqrt{2}\mu_0 A N \omega_{\mathrm{r}} Q_{\mathrm{HF}}} = \frac{\sqrt{2} L_{\mathrm{A,HF}} P_{\mathrm{min,HF}}}{\mu_0 A N \hat{V}_{\mathrm{min,HF}}}. \tag{1.5}$$

Variables A and N in Eqn. 1.5 correspond to the area and the number of turns of the tag antenna coil, respectively. μ_0 equals the permeability of free space. As indicated by Eqn. 1.5, achieving a low H_{min} and thus a high operating range requires transponders with a high quality factor Q_{HF}. Therefore, a trade-off exists between the operating range and the bandwidth of a passive transponder with regard to Eqn. 1.2. The tolerances of the antenna inductance and the parallel capacitance nevertheless provide an upper limiter for practical values of Q_{HF} [10]. Substituting Q_{HF} in Eqn. 1.5 by Eqn. 1.3, and considering Eqn. 1.4 yields an alternative expression for H_{min}, as shown in the second term of Eqn. 1.5. H_{min} is thus proportional to the minimum input power $P_{\mathrm{min,HF}}$. Consequently, achieving a high read range requires to strongly restrict the power consumption of passive HF RFID transponder ICs.

HF RFID transponders utilize the principle of load modulation for the reverse communication link to a reader device. A tag IC modulates the antenna current by varying its input impedance according to the data stream. The change in the antenna current can be sensed at the coupled reader antenna effectively as an impedance variation [1]. As shown in Fig. 1.1, the load modulation is accomplished in the majority of tag ICs by modulating

Table 1.1: Overview of relevant proximity air interface standards for contactless smart cards operating at 13.56 MHz as specified in [14, 15].

Reader → Tag	**ISO/IEC 14443-2, Type A**	**ISO/IEC 14443-2, Type B**	**JSI X 6319-4:2010, FeliCa**
Bit rate	106 kbit/s – 27.12 Mbit/s	106 kbit/s – 27.12 Mbit/s	212 kbit/s, 424 kbit/s
Modulation	106 – 848 kbit/s: ASK ($m \approx 25$ – 100 %) 1.7 – 6.78 Mbit/s: ASK ($m \approx 10$ %) 10.17 – 27.12 Mbit/s: PSK (phase range = 60 °)	106 kbit/s – 6.78 Mbit/s: ASK ($m \approx 10$ %) 10.17 – 27.12 Mbit/s: PSK (phase range = 60 °)	ASK ($m \approx 10$ %)
Line coding	106 – 848 kbit/s: Modified Miller encoding 1.7 – 6.78 Mbit/s: NRZ-L 10.17 – 27.12 Mbit/s: 3b/8b, 4b/16b encoding	106 kbit/s – 6.78 Mbit/s: NRZ-L 10.17 – 27.12 Mbit/s: 3b/8b, 4b/16b encoding	Manchester encoding
Tag → Reader			
Bit rate	106 kbit/s – 6.78 Mbit/s	106 kbit/s – 6.78 Mbit/s	212 kbit/s, 424 kbit/s
Modulation	106 kbit/s: f_{sc} = 848 kHz, OOK 212 – 848 kbit/s: f_{sc} = 848 kHz, BPSK 1.7 – 6.78 Mbit/s: f_{sc} = bit rate, BPSK	106 – 848 kbit/s: f_{sc} = 848 kHz, BPSK 1.7 – 6.78 Mbit/s: f_{sc} = bit rate, BPSK	No subcarrier
Line coding	106 kbit/s: Manchester encoding 212 kbit/s – 6.78 Mbit/s: NRZ-L	NRZ-L	Manchester encoding

$R_{P,HF}$, and thus Q_{HF}. The load modulation amplitude that is observed at the reader antenna is proportional to the applied change of the quality factor ΔQ_{HF} at the tag side [13]. Therefore, ΔQ_{HF} or Q_{HF} may also limit the communication range of the reverse link, considering a minimum level of load modulation amplitude that can be detected by the reader [11].

The requirements of particular applications have urged the development of a set of tailored HF RFID standards. The present standards can be roughly divided into standards for proximity HF RFID systems like for contactless smart cards, and vicinity HF RFID systems for item management that feature a higher communication range.

Contactless Smart Cards

Table 1.1 provides an overview of the most relevant air interface standards for proximity contactless smart cards. The prevalent standard in the field, ISO/IEC 14443-2, defines two types of communication interfaces (type A and type B) that allow bit rates of 106 kbit/s up to 27.12 Mbit/s in the forward link [14]. Readers use amplitude shift keying (ASK) with a high modulation index m of up to 100 % and modified Miller encoding to transmit data to a tag for bit rates up to 848 kbit/s. Alternatively, ASK with a lower m of around 10 % in combination with non-return-to-zero level (NRZ-L) encoding can be applied. Tags utilize

load modulation to generate a subcarrier that is modulated by using either on-off keying (OOK) or binary phase shift keying (BPSK) for transmitting the response to the reader. The subcarrier frequency f_{sc} equals 848 kHz for bit rates up to 848 kbit/s. For very high bit rates (VHBR), from 1.7 Mbit/s up to 6.78 Mbit/s, f_{sc} equals the bit rate. In the latest version of the standard, the VHBR specification for the forward link has been extended by the introduction of phase shift keying (PSK) and a 3 bit to 8 bit (3b/8b) or a 4 bit to 16 bit (4b/16b) encoding scheme based on coding tables [14]. Bit rates higher than 106 kbit/s are optional, and indeed there are yet no commercial transponder ICs available that support the full range of VHBR including the PSK scheme. Nevertheless, the operation of the novel PSK scheme has been demonstrated in literature [16, 17].

Additionally, Table 1.1 includes the FeliCa air interface specification that has been developed by Sony Corporation [18]. FeliCa was released as an official standard in JSI X 6319-4:2010 [15]. The standard allows bit rates of 212 kbit/s or 424 kbit/s for both the forward and the return link. Manchester encoding is applied for both communication directions. In contrast to ISO/IEC 14443-2, tags do not use a subcarrier for the data transmission.

The maximum communication distance of proximity contactless smart cards is typically in a range of around 10 cm [1]. Corresponding transponders of the size of a credit card, as defined in ISO/IEC 7810 [19], have an H_{min} of several 100 mA/m (e.g., [12, 20]). In comparison, ISO/IEC 14443 defines as upper limit for H_{min} a value of 1.5 A/m regarding this specific antenna class [14]. The available power for operating a passive HF RFID transponder at such high magnetic field strengths is in a range of several 100 μW (e.g., [21]). This level of available power allows the implementation of sophisticated security mechanisms on proximity transponder ICs, comprising cryptographic co-processors and security sensors to detect physical attacks on the IC. Furthermore, state of the art transponder ICs include a light-weight central processing unit (CPU) that enables a more flexible integration of novel applications (e.g.,[22, 23]). Target applications of proximity smart cards are, for example, AFC and banking that require mutual authentication and an encrypted data exchange. The operating range of RFID transponders is usually only of a lower priority in this case.

HF RFID Tags for Item Management

In contrast to contactless smart cards, the read range is highly relevant when considering applications such as the tracking of goods in logistics or anti-theft detection systems. Table 1.2 summarizes the relevant HF RFID standards for item management. The central standard ISO/IEC 18000-3 comprises three different operating modes with respect to the air interface [24]. Mode 1 is identical to the vicinity card standard ISO/IEC 15693-2 that aims for contactless cards with a higher read range [25]. The standard allows bit rates of only 1.65 kbit/s or 26.48 kbit/s in the forward link, applying a pulse position modulation (PPM) encoding. Conforming tags utilize a subcarrier for the reply to the reader. The subcarrier modulation is based on either OOK or frequency shift keying (FSK) [25].

ISO/IEC 18000-3 Mode 2 defines a communication scheme that uses phase jitter modulation (PJM) and a modified frequency modulation (MFM) line coding in the forward link [24]. For the reverse link, one of eight possible subcarrier channels ranging from f_{sc}= 969 kHz to 3013 kHz is chosen by the tag. The bit rates in the forward and the reverse link are fixed to 424 kbit/s and 106 kbit/s, respectively.

As indicated in Table 1.2, ISO/IEC 18000-3 Mode 3 essentially equals the Electronic Product Code (EPC) Class-1 HF RFID air interface specification [26] that has been published by

Table 1.2: Overview of relevant HF RFID standards for item management at an operating frequency of 13.56 MHz, as specified in [24, 25, 26].

Reader → Tag	**ISO/IEC 18000-3 Mode 1, ISO/IEC 15693**	**ISO/IEC 18000-3 Mode 2**	**ISO/IEC 18000-3 Mode 3, EPC Class-1 HF RFID**
Bit rate	1.65 kbit/s, 26.48 kbit/s	424 kbit/s	26.7 kbit/s – 212 kbit/s
Modulation	ASK ($m \approx 10$ or 100 %)	PJM (phase $\pm 3\,^\circ$)	ASK mode, ∼ 26.7 – 100 kbit/s: ASK ($m \approx 10\,\%$) PJM mode, 212 kbit/s: PJM (phase $\pm 3\,^\circ$)
Line coding	1.65 kbit/s: PPM, 1 out of 256 26.48 kbit/s: PPM, 1 out of 4	MFM	ASK mode, ∼ 26.7 – 100 kbit/s: PIE PJM mode, 212 kbit/s: MFM
Tag → Reader			
Bit rate	∼ 6.6 kbit/s, ∼ 26.6 kbit/s	106 kbit/s	53 – 848 kbit/s
Modulation	$f_{sc} = [423.75,\ 484.28\,\text{kHz}]$, FSK $f_{sc} = 423.75$ kHz, OOK	$f_{sc} = 969$ – 3013 kHz, 8 channels, BPSK	ASK mode, 53 – 212 kbit/s: $f_{sc} = 424$ or 848 kHz, OOK or BPSK ASK mode, 424 kbit/s, 848 kbit/s: No subcarrier PJM mode, 106 kbit/s: $f_{sc} = 969$ – 3013 kHz, 8 channels, BPSK
Line Coding	Manchester encoding	MFM	ASK mode, 53 – 212 kbit/s: Manchester (OOK) or Miller encoding (BPSK) ASK mode, 424 kbit/s, 848 kbit/s: FM0 PJM mode, 106 kbit/s: MFM

GS1 EPCglobal. Mode 3 includes an optional PJM communication mode that is very similar to mode 2. Nevertheless, the primary communication mode for readers uses ASK and pulse interval encoding (PIE). Transponders respond by using a subcarrier with f_{sc}= 424 kHz, 848 kHz, or no subcarrier at all. If a subcarrier is used, either Manchester or Miller encoding can be utilized. Otherwise bi-phase space (FM0) encoding is applied.

The HF RFID standards for item management are aiming primarily for transponders with a higher read range. For example, transponders with the outline of a credit card, conforming to the ISO/IEC 15693-2 or the EPC Class-1 HF RFID specification, can reach an $R_{\text{max, HF}}$ of larger than 1 m [11]. The actual achievable read range is nevertheless highly dependent on the dimensions of the used reader antenna coil that are typically in the range of several 10 cm (e.g., [27]). Achieving such a high $R_{\text{max, HF}}$ requires a tag with an H_{min} of only a few 10 mA/m [11]. The direct current (DC) power consumption of the core circuitry of a corresponding vicinity tag IC is thus limited to approximately 10 μW or less [11]. Besides the costs, this constraint on the power consumption restricts the possible features and the complexity of vicinity HF RFID tag ICs. State of the art vicinity tag ICs incorporate merely a simple state machine based digital core to handle the communication protocol and the

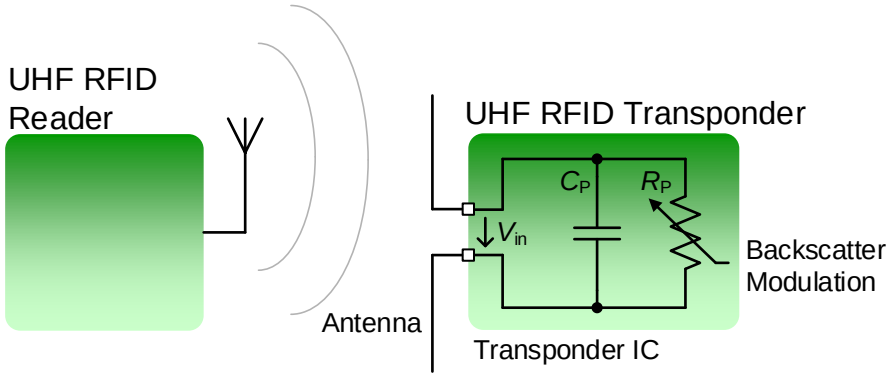


Figure 1.2: Operating principle of passive UHF RFID systems. A typical transponder includes a dipole like antenna that is directly connected to the RF input terminals of a transponder IC.

access to an integrated electrically erasable programmable read-only memory (EEPROM) (e.g., [28]).

Additional security functions for RFID based object identification have been addressed in international standards like the ISO/IEC 29167 [29]. Indeed, commercial vicinity tag ICs have been released recently that incorporate a cryptographic primitive such as the Grain 128a that enables mutual authentication and an encrypted data exchange [30]. Nevertheless, the strong limitation of the power consumption does not allow the implementation of sophisticated security features that are comparable to state of the art proximity contactless smart cards.

Furthermore, near field communication (NFC) has to be mentioned as a closely related form of technology in the context of HF RFID systems. NFC enables mobile phones or other wearables to effectively act as an HF RFID transponder (card emulation mode) or as an HF RFID reader. Parts of the FeliCa specification and the proximity HF RFID standard ISO/IEC 14443 have been incorporated in the air interface specification for NFC that has been released as an official standard in ISO/IEC 18092 [31]. In addition, ISO/IEC 18092-2 specifies a communication interface between two active NFC peers [31]. The procedure of how to distinguish between different communication modes including also the vicinity standard ISO/IEC 15693 has been specified in the extending standard ISO/IEC 21481 [32].

1.1.2 UHF RFID Systems

As shown in Fig. 1.2, the operating principle of passive UHF RFID systems is similar to HF RFID technology (see Fig. 1.1). Nevertheless, UHF RFID transponders operate predominantly in the far field of reader antennas and therefore include a resonating antenna that allows the efficient emission and reception electromagnetic waves [2]. Typical tag antennas are, for example, T-matched half-wave dipole antennas. By applying meandering and capacitive tip-loading, the dimensions of dipole antennas can be reduced to well below half the wavelength of the carrier signal $\lambda/2$ [2, 33]. For item-level tags, for example, tag antennas with maximum dimensions of less than 5 cm are used [34]. In comparison to this, $\lambda/2$ equals about 15 cm at the operating frequency of around 900 MHz.

Assuming an operation in the far field and free space wave propagation, the available power for operating a tag P_{av} at a distance R from a reader antenna can be estimated by using the Friis transmission equation [2, 35]:

$$P_{\mathrm{av}} = P_{\mathrm{int,\,TX}} G_{\mathrm{int}} G_{\mathrm{tag}} \left(\frac{\lambda}{4\pi R} \right)^2. \tag{1.6}$$

$P_{\mathrm{int,\,TX}}$ and G_{int} in Eqn. 1.6 correspond to the transmitting power and the antenna gain of an RFID interrogator, respectively. G_{tag} is the gain of the tag antenna. The sensitivity P_{min} describes the minimum level of input power that is required to operate a UHF RFID tag IC. By rearranging Eqn. 1.6, the maximum operating distance of a UHF tag R_{max} can be estimated for a given level of the sensitivity P_{min} [36]:

$$R_{\mathrm{max}} = \frac{\lambda}{4\pi} \sqrt{\frac{P_{\mathrm{int,\,TX}} G_{\mathrm{int}} G_{\mathrm{tag}} \tau p}{P_{\mathrm{min}}}}. \tag{1.7}$$

Parameter p in Eqn. 1.7 corresponds to the power loss due to the polarization mismatch between the tag and the reader antenna. Furthermore, τ quantifies the loss resulting from the impedance mismatch between the tag antenna and the tag IC that can be expressed by means of the input reflection coefficient Γ [37]:

$$\tau = 1 - |\Gamma|^2 = 1 - \left| \frac{Z_{\mathrm{IC}} - Z_{\mathrm{A}}^*}{Z_{\mathrm{IC}} + Z_{\mathrm{A}}} \right|^2. \tag{1.8}$$

As shown in the second part of Eqn. 1.8, Γ is determined by the complex input impedance of the UHF tag IC Z_{IC} and the antenna impedance Z_{A}. According to Eqn. 1.7, achieving a high R_{max} requires a transponder IC with a low sensitivity P_{min}. Moreover, τ has to approach unity to maximize the communication range. The optimum is reached if the antenna impedance Z_{A} matches exactly the complex conjugate of the transponder input impedance ($Z_{\mathrm{A}} = Z_{\mathrm{IC}}^*$), and thus $\Gamma = 0$, as indicated by Eqn. 1.8.

The input impedance Z_{IC} can be modeled by means of an equivalent parallel capacitance C_{P} and a resistance R_{P}, as shown in Fig. 1.2 [38]. In general, the input reflection coefficient is a function of frequency ($\Gamma(\omega)$), and the bandwidth $\Delta\omega_{\mathrm{m}}$ over which a targeted low level of $|\Gamma(\omega)|$ can be reached is limited. The Bode-Fano criterion yields a theoretical upper limit for the achievable matching bandwidth, considering the specific circuit constellation shown in Fig. 1.2 [39, 40, 41]:

$$\int_0^\infty \ln\left(\frac{1}{|\Gamma(\omega)|} \right) d\omega \leq \frac{\pi}{R_{\mathrm{P}} C_{\mathrm{P}}} = \frac{\pi \omega_0}{Q}. \tag{1.9}$$

Following Eqn. 1.3, the product of R_{P} and C_{P} in Eqn. 1.9 has been substituted by the input quality factor Q at a given carrier frequency ω_0. The upper limit for the matching bandwidth $\Delta\omega_{\mathrm{m}}$ can be determined by considering Eqn. 1.9, and assuming a constant maximum allowable value Γ_{m} for $|\Gamma(\omega)|$ within a frequency range of $\Delta\omega_{\mathrm{m}}$ around the center frequency ω_0 and $|\Gamma(\omega)| = 1$ otherwise [40]:

$$\Delta\omega_{\mathrm{m}} \leq \frac{\pi\omega_0}{Q}\frac{1}{\ln\left(\frac{1}{\Gamma_{\mathrm{m}}}\right)}. \tag{1.10}$$

According to Eqn.1.10, achieving a large bandwidth requires a UHF transponder IC with a low quality factor Q, similar as in case of HF RFID transponders (see Eqn.1.2). Nevertheless, there is no direct trade-off between the quality factor of a UHF tag IC and the powering range, as in case of HF RFID tag ICs (see Sect. 1.1.1). A larger bandwidth is advantageous for UHF RFID transponders to diminish detuning effects of the antenna due to changing environmental conditions in the antenna near field [42].

UHF RFID transponders utilize the principle of backscatter modulation for the reverse communication link to transmit data back to the reader. A tag IC modulates its input impedance or rather the reflection coefficient Γ according to the data stream. As shown in Fig. 1.2, the majority of tag ICs modulate primarily the real part of the input admittance R_{P} in a simple manner by switching a resistive load (e.g., [43, 44]). The change of Γ causes a proportional variation of the transponder's radar cross section $\Delta\sigma$ [36]:

$$\Delta\sigma = \frac{\lambda^2}{4\pi}G_{\mathrm{tag}}^2\alpha|\Gamma_1 - \Gamma_2|^2. \tag{1.11}$$

Eqn. 1.11 reveals that $\Delta\sigma$ is dependent on the magnitude of the difference of the reflection coefficients in the corresponding modulation states Γ_1 and Γ_2. The factor α accounts for characteristics of the baseband modulation waveform like the DC offset that does not contribute any information to the backscattered signal [36]. The maximum communication range of the reverse link $R_{\mathrm{max,\,rev}}$ can be expressed by means of $\Delta\sigma$ and the reader sensitivity $P_{\mathrm{int,\,min}}$ [2]:

$$R_{\mathrm{max,\,rev}} = \sqrt[4]{\frac{\lambda^2 P_{\mathrm{int,\,TX}} G_{\mathrm{int}}^2 \Delta\sigma}{(4\pi)^3 P_{\mathrm{int,\,min}}}}. \tag{1.12}$$

The reader sensitivity $P_{\mathrm{int,\,min}}$ corresponds to the minimum of required signal power at the receiver of the reader for achieving a specific packet error rate. $P_{\mathrm{int,\,min}}$ is limited in practice by the transmitter signal leakage into the receiver of the reader that is denoted as self-jamming [45]. The product of G_{int} and $P_{\mathrm{int,\,TX}}$, on the other hand, is generally limited by regulations (e.g., [46, 47]). Assuming the other parameters as fixed, $R_{\mathrm{max,\,rev}}$ is determined by the differential radar cross section $\Delta\sigma$ of the transponder.

As shown in Eqn. 1.11, the maximum value of $\Delta\sigma$ is reached if Γ_1 and Γ_2 equal 1 and -1, respectively, or vice versa. There is however no power available to supply the tag IC, in this case. The input impedance is switched between an open and a short connection. On the contrary, antennas of passive transponders are typically well matched to the input impedance of the tag IC during the first modulation state to supply the maximum power to the tag IC ($\Gamma_1 \approx 0$). In the second modulation state, the tag IC provides accordingly a low input impedance to modulate Γ ($\Gamma_2 \approx -1$). The design of passive transponders essentially entails a trade-off between the power supplied to the tag IC and the backscatter signal strength, and therefore between R_{max} and $R_{\mathrm{max,\,rev}}$.

UHF RFID readers can reach a low sensitivity of about $-80\,\mathrm{dBm}$ even in the presence of a considerable self-jamming signal [45]. In comparison, the sensitivity figure of state of

Table 1.3: Overview of the major protocol parameters as defined in the ISO/IEC 18000-63 [49] and the EPC Generation-2 UHF RFID standard [50].

	Reader → Tag	**Tag → Reader**
Bit rate	$\sim$ 26.7 kbit/s – 128 kbit/s	5 kbit/s – 640 kbit/s
Modulation	DSB-ASK (m = 66 – 100 %) SSB-ASK (m = 66 – 100 %) PR-ASK	5 – 320 kbit/s: f_{sc} = 40 to 640 kHz, BPSK 40 – 640 kbit/s: No subcarrier
Line coding	PIE	5 – 320 kbit/s: Miller encoding 40 – 640 kbit/s: FM0

the art transponder ICs is magnitudes higher with values ranging around -20 dBm (e.g., [48]). The communication distance between present UHF RFID transponders and readers is yet predominantly limited by the maximum range of the forward link R_{max}, and hence the sensitivity P_{min} of UHF RFID transponder ICs.

UHF RFID Tags for Item Management

The majority of present UHF RFID systems is based on the ISO/IEC 18000-63 standard that specifies a communication protocol for an RFID interface operating in the band from 860 MHz to 960 MHz [49]. The specific operating bands for a certain region or country are subject to local regulations (e.g, [46, 47]). The communication interface, as described in the ISO/IEC 18000-63, has been originally defined in the EPC Generation-2 UHF RFID standard [50]. At present, both standards are evolved in accordance with each other.

Table 1.3 provides an overview of the communication protocol as described in the ISO/IEC 18000-63 [49] and the EPC Generation-2 UHF RFID standard [50]. Corresponding readers use PIE for the data encoding in the forward link. The modulation pulses are generated by using either double-sideband amplitude shift keying (DSB-ASK), single-sideband amplitude shift keying (SSB-ASK) or phase-reversal amplitude shift keying (PR-ASK). For PR-ASK, the reader reverses the phase of the transmit signal at a modulation pulse. The limited bandwidth of the baseband signal results in a pulse in the carrier envelope that can be detected by a tag. For the reverse link, transponders use either a BPSK modulated subcarrier or no subcarrier, applying Miller or FM0 encoding, respectively. The subcarrier frequency f_{sc} is configurable in a range from 40 kHz to 640 kHz.

The ISO/IEC 18000-63 standard targets primarily low-cost transponders with a high communication range. At present, state of the art transponders can achieve read ranges of more than 10 m. The actual range that is observed in practical applications is nevertheless strongly dependent on the specific operating conditions such as the material the tag is attached to [2]. As noted, realizing a high read range requires a tag IC with a low sensitivity figure (see Eqn. 1.7). The sensitivity of a passive tag IC is directly linked to the DC power consumption of its core circuitry, as the IC is supplied entirely by the RF power impinging at the antenna. The available power budget for supplying a highly sensitive tag IC is in consequence limited to only a few μW (e.g., [43, 51]). The stringent constraints on the power consumption strongly restrict the overall circuit complexity. UHF RFID transponder ICs typically incorporate a hard-wired digital state machine to handle the communication protocol

and the access to a non-volatile memory (NVM) like an EEPROM. In case of transponder ICs for high-volume item-level tagging, the NVM may comprise only a few 100 bits to store an identification number (e.g., [48]).

The security features of UHF RFID tag ICs have been predominantly limited to simple password based mechanisms to protect the memory from unauthorized access or deactivate the tag IC. More advanced security functions that allow, for example, a mutual authentication have been already addressed in literature (e.g., [52, 53]) and in international standards like the ISO/IEC 29167 [29], as noted in Sect. 1.1.1. Furthermore, a first commercial transponder IC has been released that features a cryptographic primitive according to the Advanced Encryption Standard (AES) [54]. Nevertheless, achieving a comparable high security level as modern HF RFID smart card ICs for AFC applications is practically not possible for passive UHF RFID tag ICs due to the much stronger restrictions on the power consumption.

1.2 Automatic Fare Collection

Public transport authorities and operators have promoted the introduction of AFC systems or electronic ticketing (e-ticketing) for various reasons including countering fraud, and lowering the cost and time overhead for fare collection. Furthermore, AFC systems facilitate the implementation of integrated ticketing or pricing schemes that allow passengers to use the same ticket or the same fare medium at least on multiple modes of transport and for different transport operators [5]. Above all, integrated ticketing has been acknowledged as a key factor for enhancing the attractiveness of public transportation by simplifying the sales system [6]. Further incentives can be created for users by linking the e-ticketing scheme with additional services. For example, the usage of contactless smart cards can be extended to payments at retail shops or for parking [6].

Different fare media are used for electronic ticketing comprising magnetic stripe cards and mobile ticketing based on Short Message Service (SMS), optical character recognition (OCR) or NFC. Nevertheless, HF RFID enabled contactless smart cards are today the prevalent form of fare medium in AFC systems as deployed in densely populated metropolitan areas [6]. Replaceable personalized and transferable anonymous smart cards are issued for AFC (e.g., [55]). Anonymous smart cards typically store a prepaid account, which is charged with the fare when used. Personalized cards additionally allow a billing in the aftermath according to the recorded usage [6].

Passengers have to perform a check-in transaction at an RFID reader by using a smart card at the entry point of a public transport vehicle. In case of the metro or suburban railways, usually readers are integrated in automatic gates at stations that allow passengers only to pass on to the platforms, if a ticket has been validated. Buses and trams, on the other hand, are predominantly equipped with on-board readers. Passengers are obliged to check-in right after boarding. The reader provides an audiovisual signal to notify the passenger whether the check-in has been successful or not. Depending on the specific fare structure, passengers are required to perform an additional check-out transaction before alighting from a bus or tram, or alternatively at the station after leaving a train or metro. The following types of fare structures can be distinguished with respect to the billing of journeys [5]:

- **Flat fare:** The fare for a journey is independent from the route taken or distance traveled. Despite that, the validity period of a ticket is typically limited.
- **Route fare:** The fare for every single route or line of a transport network is determined individually. Passengers pay a fixed fare when taking a specific route irrespective of the distance traveled.
- **Zonal fare:** The transportation network is split into geographic zones. Within each zone a flat fare is charged. Passengers traveling through multiple zones pay a fee according to the number of zones crossed.
- **Distance based fare:** Single routes are divided into fare stages. Passengers pay a fare according to the number of fare stages traveled mirroring the actual distance of a journey. Moreover, the pricing of the individual fare stages may consider factors such as operating cost or demand characteristics.

For flat or route fares, a single check-in is generally sufficient. The implementation of zonal or distance based fare structures additionally necessitates the enforcement of a check-out at the point of alighting. In general, the application of smart cards significantly facilitates the introduction of more complex fare structures like distance based fares or also specifically tailored hybrid schemes that yield a more equitable pricing with respect to the utilized service of individual passengers.

The implementation of a mandatory check-out procedure nevertheless has been an issue specifically for means of transport that do not allow an installation of automatic gates without severe complications such as buses or trams. As an alternative to automatic gates, transport operators can leverage the payment procedure to motivate passengers to perform a check-out. For example, at the check-in a maximum fare price is charged, and the difference to the actual fare price is only returned when performing a check-out [55]. Introducing schemes like this however require transport operators to adopt specific regulations for handling complaints of passengers that have forgotten to check-out [6]. Passengers are apparently at a disadvantage in such a situation, which in turn could have a negative impact on the general passenger satisfaction. Indeed, numerous AFC systems based on smart cards do not enforce a check-out at the point of alighting (e.g., on buses and trams in London [5]). The decision of transport operators on whether a check-out is imposed or not is directly linked to the targeted fare structure, as noted above. With respect to the fare structure, passenger satisfaction is an important point. But it is only one among many influencing factors such as costs, technical or political aspects.

In addition to the primary task of fare collection, the data on smart card usage has evolved to be an important tool for transport operators. The statistical data on recorded journeys, for example, allows the derivation of detailed performance metrics for individual public transport routes and the optimization of schedules [56]. The quality and fidelity of the data is crucial for the accuracy of the conclusions that can be drawn. In case of AFC systems that do not impose a check-out, the information on the alighting point can only be estimated for a further analysis, which inevitably introduces errors [57].

Alternative Approaches for AFC

Technical solutions for ticket validation have been envisaged that do not require any conscious action by the passenger, and thus should enhance the passenger convenience. With

reference to the current check-in/check-out systems, these hands-free ticket validation systems are termed as be-in/be-out or walk-in/walk-out systems [6]. Already in 2000, the Swiss Federal Railways and the Public Transportation Association of Switzerland conducted field trials of a be-in/be-out system based on active LF/UHF RFID transponders [58]. Commercial vendors of AFC equipment have furthermore applied and promoted solutions based on active RFID for be-in/be-out AFC systems (e.g., [59]). Nevertheless, these systems have not been used on a larger scale by now. As noted, the battery of an active RFID transponder poses disadvantages with respect to production cost and lifetime. The usage of passive UHF RFID transponders has been investigated as a potential low-cost alternative for AFC [9]. As discussed in Sect. 1.1.2, the security level of passive UHF RFID tag ICs is however inherently limited, and probably not sufficient for AFC applications.

The wide spread adoption of mobile phones and associated mobile applications also implies promising opportunities with respect to AFC and intelligent transport systems in general. The data on mobile phone usage, for example, has been considered in literature for the analysis of passenger flows in a metro network [60]. In an alternative approach, the Bluetooth interface of mobile phones is exploited to track passengers on buses [61]. Moreover, BLE technology has been considered in conjunction with a mobile phone application for implementing a be-in/be-out AFC system [7, 8]. Indeed, system vendors at the present time are actively promoting be-in/be-out solutions using BLE and mobile phones [62, 63]. A first field trial of such an AFC system was conducted on a line of the Schweizerische Südostbahn AG [64]. The question whether be-in/be-out systems, irrespective of the detailed implementation, are suited for high-volume mass transit in larger cities still needs to be investigated. Using additionally the NFC interface of a mobile phone, possibly allows the realization a hybrid scheme, as an alternative. The NFC interface could be used for an active check-in operation, as in current AFC systems, and BLE could be applied to remotely or passively detect the alighting point of a passenger.

1.3 Scope of Thesis

This thesis considers passive HF/UHF dual band RFID transponder ICs for the application in AFC systems. The proximity HF RFID or near field interface of a corresponding dual band RFID transponder is provided to perform a check-in transaction for validating a ticket, in common with current AFC systems. The additional UHF RFID interface aims at enabling a remote communication link to the dual band smart cards of passengers over a distance of a few meters. Detecting the presence of passengers remotely inside a vehicle by using the UHF link should enable an accurate estimation of the alighting point of individual passengers, without requiring the passengers to perform any action. The proposed AFC system resembles therefore a hybrid check-in/be-out or check-in/walk-out system, as discussed in Sect. 1.2.

The operating conditions of transponders in the considered AFC application scenario are highly variable and are specifically challenging with respect to the UHF RFID link. Achieving a high detection probability over a distance of a few meters therefore imposes high requirements on the performance of the UHF RFID interface of a HF/UHF dual band RFID transponder IC.

Moreover, a suitable dual band smart card IC has to support sophisticated security features, as required by current AFC or e-ticketing systems. The advancement of security related functions, but also the trend towards integrating multiple applications on a single

smart card, have led to a rising complexity of the digital sub-system of smart card ICs. The expanding circuit complexity encourages the deployment of highly scaled CMOS technologies, with respect to economic and performance considerations.

The design of high performance UHF RFID front-ends in scaled CMOS technologies is nevertheless challenging, especially with regards to the typically strong restrictions on the fabrication cost. The main focus of this work is put therefore on the implementation of UHF analog front-ends in cost-optimized highly scaled CMOS technologies. In particular, I examine the design of major building blocks of a UHF RFID front-end in a 40 nm low-power CMOS technology that represents a probable technology option for secure HF/UHF dual band RFID transponder ICs. Three threshold voltage (V_{th}) compensated RF-DC power converters are presented, targeting the implementation of a highly sensitive and broadband UHF RFID interface. In addition, the overvoltage protection of the UHF RFID front-end emerges to be a critical factor regarding the long-term reliability of transponder ICs, as a result of the reduced maximum voltage ratings in scaled CMOS technologies. I introduce a low-power DC voltage limiter and two RF voltage limiters for protecting the core circuitry and UHF RFID front-end of a transponder IC from overvoltage conditions at high levels of input power. The operation of the proposed circuits is demonstrated by means of measurement results of fabricated circuit prototypes.

1.4 Outline and Related Work

1.4.1 HF/UHF Dual Band RFID Transponders for AFC Applications

In Ch. 2, as a first step, I review the specific operating conditions of HF/UHF dual band transponders in the considered application scenario, and evaluate the major influencing factors with regard to the RF performance of the UHF RFID link. Furthermore, questions of security and privacy are addressed, focusing specifically on the novel remote detection feature using the UHF RFID interface. I briefly summarize a security protocol that counteracts an unauthorized tracking via the UHF link to safeguard the privacy of passengers. The security scheme has been originally proposed by Raphael Spreitzer and Hannes Gross in two joint publications [65, 66] that have been created in course of the research project Secure Contactless Sphere (SeCoS).

Building upon the previous discussion, I outline the architecture of a future HF/UHF dual band transponder IC for AFC applications. The expanding complexity of the digital sub-system of smart card ICs fosters the move towards highly scaled CMOS technologies, as noted. I address the implications of technology scaling with respect to the overall circuit implementation, and more specifically concerning the HF and the UHF RFID front-ends of a passive dual band RFID transponder. The associated considerations regarding the choice of specific technology options are highlighted.

Related Work

The application of passive UHF RFID technology in AFC systems has previously been evaluated by Oberli *et al.* [9]. The investigation comprised also the usage of HF/UHF dual band RFID transponders that incorporate however merely separate off-the-shelf HF and UHF tag

ICs [9]. The requirements on dedicated dual band RFID transponders especially with respect to security have not been considered.

The research on passive HF/UHF dual band transponder ICs and front-ends has so far been focused on tag ICs for item management and low-power wireless sensors. Missoni *et al.* have published in [67] a first dual band tag IC supporting the EPC Class-1 HF RFID [26] and the EPC Generation-2 UHF RFID [50] standards. The proposed tag IC uses a single configurable analog front-end and accordingly combined antenna terminals for the HF and the UHF communication interfaces [67]. A similar approach has been adopted for the implementation of wireless sensor nodes that conform to the EPC HF and UHF RFID standards, as described in recent publications [68, 69, 70, 71]. Moreover, a first commercial dual band tag IC has been released that supports the proximity HF RFID standard ISO/IEC 14443 [14] and the EPC Generation-2 UHF RFID standard [72]. This tag IC targets applications in product authentication, in the supply chain, or the retail sector, for example [72]. HF/UHF dual band transponder ICs that integrate sophisticated security functions comparable to current smart card ICs, and a high-performance passive UHF RFID interface have not been addressed so far.

1.4.2 RF-DC Power Converters

The RF-DC power converter or alternatively the RF charge pump of a UHF RFID front-end rectifies the RF input voltage and provides additionally an up-conversion of the rectified voltage to supply the connected core circuitry. Chapter 3 provides an introduction to the design principles of CMOS RF charge pumps emphasizing especially circuit techniques termed as V_{th} compensation. V_{th} compensation techniques consist predominately in providing a DC bias to the gate terminals of the rectifying transistors, which enables an improvement of the power conversion efficiency and a reduction of the quality factor of RF charge pumps at low levels of input power.

In the following, I discuss in detail the design of three differential V_{th} compensated RF charge pumps in the considered 40 nm CMOS technology. As a measure for reducing fabrication cost, the presented designs use exclusively low-leakage or high-V_{th} transistors that are particularly suited for implementing low-power digital circuits. With respect to the raised V_{th} of the rectifying transistors, the V_{th} compensation of the RF charge pump is a key factor for realizing a high performance UHF RFID front-end.

The first charge pump design uses gate biasing for the V_{th} compensation. The gate bias voltages for the individual rectifying transistors are generated by means of auxiliary charge pumps. The circuit topology has been adopted from an existing design by Peter Herkess in a previous CMOS process node. I have enhanced the V_{th} compensation by introducing a combined gate and bulk biasing approach in the remaining two circuits, which allows an improvement of the power conversion efficiency at low input powers. Measurement results of fabricated circuit prototypes indeed reveal a high performance with respect to the power conversion efficiency and the input quality factor. A comparison to previous publications highlights the performance of the implemented RF charge pumps (see Table 3.4). Furthermore, the operation of the circuits for typical modulation waveforms and the start-up behavior are evaluated for a varying ambient temperature.

Related Work

External and internal V_{th} compensation techniques or alternatively V_{th} self-compensation techniques can be distinguished [73]. External V_{th} compensation schemes use additional circuits that operate independently from the RF charge pump to provide the bias voltages for the rectifying transistors. In contrast, in an internal V_{th} compensation, the generation of the bias voltages is tightly linked to the operation of the charge pump itself.

Umeda *et al.* proposed an external V_{th} compensation for a single-ended RF charge pump, using a switched capacitor circuit to provide a gate bias to the rectifying transistors [74]. A similar method is applied in [75] by Bakhtiar *et al.* to an externally V_{th} compensated differential charge pump. The presented scheme has been modified furthermore by using a feedback of the DC output voltage to generate the bias voltages, which therefore resembles rather an internal V_{th} compensation approach [75].

Nakamoto *et al.* previously introduced dedicated bias circuits to derive the gate biases for the rectifying transistors from the DC output voltages of the respective charge pump stages [76]. Another internal or V_{th} self-compensation technique that uses feedback connections of intermediate outputs to bias the gates of the rectifying transistors has been published by Kotani and Ito for single-ended circuits [77]. The scheme has been extended by Papotto *et al.* [78] and more recently by Hameed and Moez [79], targeting an enhancement of the bias voltages and an improved control of the bias levels. Moreover, the principle of feedback has been adopted for biasing in addition the bulk terminals of the rectifying transistors, and thus to reduce the V_{th} [80, 81, 82].

Bergler *et al.* describe in [83] an alternative V_{th} compensation approach for differential RF charge pumps that uses auxiliary charge pumps to generate a gate bias voltage for the individual rectifying transistors within a charge pump stage. Similar circuit techniques have recently been published for single-ended RF charge pumps [84, 85]. A V_{th} compensation technique using auxiliary charge pumps for providing a gate bias and concurrently a forward bulk bias to the rectifying transistors of an RF charge pump, as presented in this work, has not been considered so far.

Complementary to the research on improving the performance of RF charge pumps, automatic antenna tuning techniques have been investigated to enhance the effective bandwidth of UHF RFID transponders. The front-end circuits as proposed by Bakhtiar *et al.* [86] or Stoopman *et al.* [87] adjust the input capacitance at the RF terminals, for example, to tune the impedance matching between the antenna and the front-end, and thus to maximize the output power of the RF-DC power converter.

1.4.3 Overvoltage Protection

Chapter 4 discusses the requirements on the overvoltage protection of UHF RFID front-ends. In particular, I elaborate on questions regarding the reduced operating voltages in scaled CMOS technologies. For instance, the maximum voltage rating of the core devices in the considered 40 nm CMOS technology is as low as 1.2 V. An examination of the behavior of the individual building blocks at high input powers reveals that the lowered maximum ratings indeed require the introduction of a dedicated RF voltage limiter in addition to a DC voltage limiter to prevent damaging overvoltages at a front-end.

The focus is laid on aspects of circuit implementations. I present the design of a low-power DC voltage limiter and two stand-alone RF voltage limiters. The DC limiter includes a temperature compensation and allows the regulation the output voltage of the RF charge-pumps within a narrow range below 1.2 V versus output currents reaching from below 100 nA to 800 μA. The RF limiters utilize auxiliary charge-pumps to sense the RF input voltage and at the same time to generate the bias voltages for the active load transistors at higher input powers. This approach allows the minimization of the standby power consumption and the impact on the RF performance of an overall UHF RFID front-end at low input powers. At high input powers of up to 20 dBm, the RF voltage limiters effectively diminish the voltage amplitude at a front-end to below 1.1 V complying to the strongly constrained maximum voltage ratings in the used 40 nm CMOS process in comparison to previously used CMOS technologies (see Table 4.3). I demonstrate the functionality of the presented circuits by means of measurement results of fabricated circuit prototypes.

Related Work

The DC limiter is a central element of the power management of a passive UHF RFID tag IC. Simple circuit implementations merely comprise multiple serially connected diodes or diode connected metal oxide semiconductor (MOS) transistors to bypass the excess current, and thus to limit the output voltage of an RF charge pump [88]. The principle has been extended to self-biased circuits of various forms, including multiple shunt stages to monitor the voltage level and to control the bypass current accordingly (e.g., [89, 90, 91]). A similar approach has also been adopted for the circuit proposed in [43] by Curty *et al.* that integrates the DC limiter partly with the RF charge pump. A more accurate regulation may be achieved by utilizing an operational transconductance amplifier (OTA) based feedback control and a bandgap voltage reference, as described by Vaz *et al.* [92] or Fernández *et al.* [93], for example. Alternatively to using only a shunt regulation, the inclusion of a series regulator branch has been considered to limit the voltage level, in combination with an RF voltage limiter [94, 95].

The design of RF voltage limiter circuits has found less attention in literature regarding UHF RFID transponder ICs so far. Facen and Boni have proposed a differential UHF RFID front-end including a dedicated RF voltage limiter [96]. The presented circuit integrates the electrostatic discharge (ESD) protection tightly with the RF limiter [96]. Balachandran and Barnett *et al.* have considered combining the RF voltage limiter with the demodulator of a single-ended UHF RFID front-end [44, 97]. Furthermore, the HF/UHF dual band RFID tag ICs as presented by Missoni *et al.* [67] and Reinisch *et al.* [69, 70] include RF shunt circuits that comprise voltage regulation and load modulation capabilities. With respect to HF RFID transponder ICs, RF voltage limiters have generally been regarded on more occasions so far (e.g.,[11, 21, 98]).

The circuit designs that are presented in the publications listed above are based on CMOS technologies at or above the 120 nm process node. The deployment of more advanced process technologies and the reduced maximum voltage ratings associated with it, inevitably requires a careful revision of established concepts for the overvoltage protection of passive UHF RFID front-ends.

2 HF/UHF Dual Band RFID Transponders for AFC Applications

Passengers on public transportation may experience the usage of HF RFID enabled smart cards as counter-intuitive and inconvenient in specific situations such as when performing a check-out transaction at a reader device within a bus or a tram right before alighting. As noted in Sect. 1.2, there are alternative technologies for conducting an automated fare collection currently being investigated that should eliminate any passenger action during boarding or alighting.

Integrating HF and UHF RFID technology enables a remote detection of passengers via the UHF link while building upon established security methods and the infrastructure of current AFC systems using proximity smart cards. The deployment of passive UHF RFID technology allows the continuation of the present model of distributing low-cost smart cards as fare medium. In contrast to other mobile ticketing technologies, smart cards can be made available for everyone and thus have the potential to replace paper based ticketing schemes to a large extend.

This chapter reviews the operating conditions for HF/UHF dual band RFID transponders in an AFC system, and discusses the requirements regarding the UHF interface. I summarize the main aspects of a security protocol to safeguard passengers' privacy, and sketch the architecture of a corresponding future HF/UHF dual band RFID transponder IC that is suitable for e-ticketing applications. In the following, questions of the circuit implementation are discussed specifically focusing on the HF and UHF analog front-ends, and the implications of the progressing CMOS technology scaling in this context.

Original Publications Related to This Chapter

L. Zöscher, J. Grosinger, R. Spreitzer, U. Muehlmann, H. Gross, and W. Bösch, "Concept for a security aware automatic fare collection system using HF/UHF dual band RFID transponders," in *2015 45th European Solid State Device Research Conference (ESSDERC)*, Graz, Austria, Sept. 2015, pp. 194–197.

L. Zöscher, R. Spreitzer, H. Gross, J. Grosinger, U. Mühlmann, D. Amschl, H. Watzinger, and W. Bösch, "HF/UHF dual band RFID transponders for an information-driven public transportation system," *e & i Elektrotechnik und Informationstechnik*, vol. 133, no. 3, pp. 163–175, June 2016.

2.1 AFC System

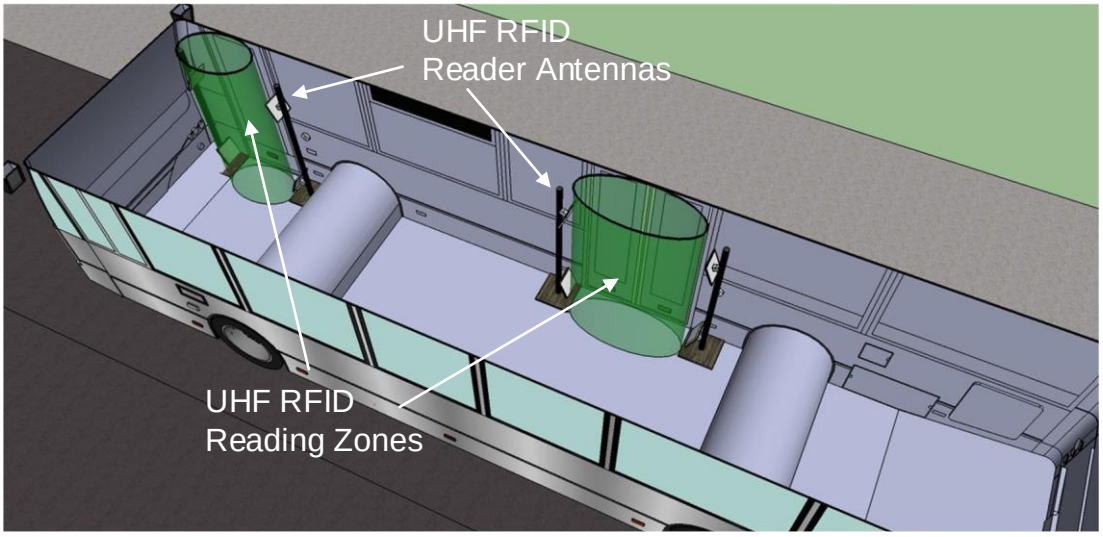
In the considered AFC system, passengers perform a check-in transaction using a dual band smart card at a stationary HF RFID reader after boarding a bus or tram. Additionally, UHF RFID readers and corresponding antennas are mounted inside the vehicle. The UHF RFID readers periodically poll the smart cards within range, and thus determine the presence of passengers inside or nearby the vehicle. Correlating the information of successful queries of a specific smart card on a time scale with the location of the vehicle allows an estimation of a passenger's alighting point. The reading probability of passive UHF RFID tags in practical applications though is limited [3, 9]. For example, Oberli *et al.* have estimated a detection probability of around 80 % for UHF RFID transponders in a public transport scenario, using a portal arrangement of antennas [9]. As a result of this, the estimated information on the alighting point of passengers is possibly too inaccurate and unreliable to be considered directly for the ticket billing. Nevertheless, the collected data on individual journeys and specifically the statistical analysis of a larger data set represents a valuable tool for transport operators or municipal authorities, as noted in Sect. 1.2.

2.1.1 UHF RFID Communication Link

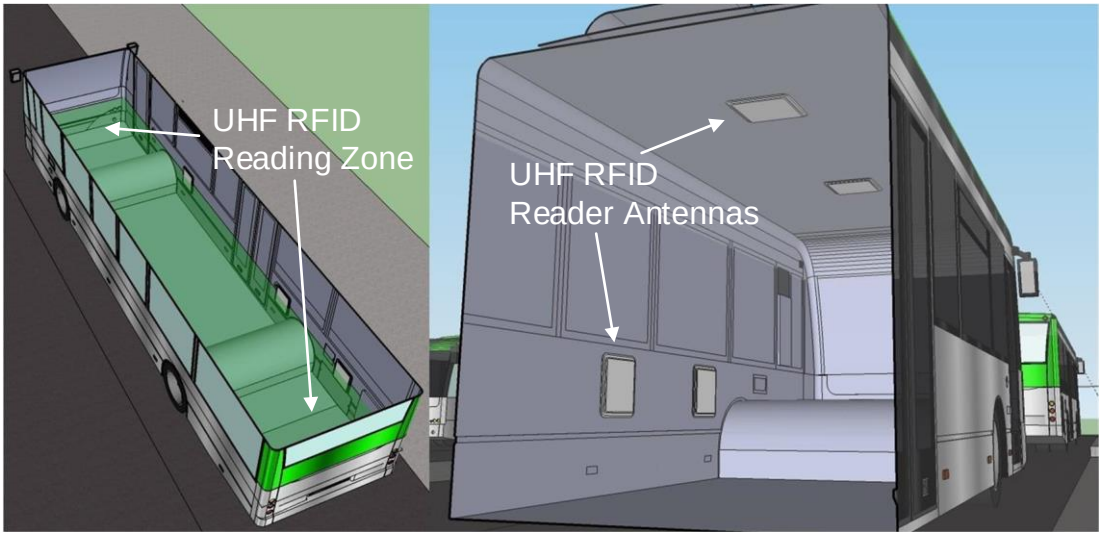
Stationary UHF RFID reader installations typically use planar circularly polarized patch antennas, whose dimensions are roughly half the wavelength of the carrier signal $(\lambda/2)$ [2]. Patch antennas for operating frequencies in a range of 860 MHz to 960 MHz [50] accordingly measure around $20 \times 20\,\mathrm{cm}^2$. Considerably more compact antenna designs can be achieved by trading off the antenna gain [99]. In comparison, the size of loop antennas for vicinity HF RFID readers as used for anti-theft systems may be in range of half a meter or more (e.g., [27]).

The compact dimensions of UHF RFID reader antennas allow a rather flexible arrangement of antennas within public transport vehicles. In particular, I consider two scenarios for the antenna arrangement, as shown in Fig. 2.1. Figure 2.1a illustrates an example for a portal arrangement of the UHF RFID reader antennas within a bus. As shown, the required range for the UHF RFID link is limited to only about 1 m to 2 m. The arrangement maximizes the reading probability of transponders near the doors of the vehicle, and thus aims at detecting passengers right before or after alighting from the bus. A passenger's alighting point can in theory be estimated with high accuracy. Nevertheless, also passengers may be detected, who stay inside the vehicle when the doors have opened. To distinguish between alighting and continuing passengers, the reader may start querying the smart cards within its range right before the arrival at the next stop, and in addition remain active for a certain period subsequent to a stop. Evaluating the number of successful reads of a specific transponder before and after a stop allows a conclusion whether the passenger has alighted or not.

In the scenario with distributed UHF RFID antennas, as shown in Fig. 2.1b, the readers periodically inventory the entire population of dual-band smart cards within the vehicle. As noted, the reading probability of UHF RFID transponders in practical situations is limited, and thus certain smart cards may not be detectable at a specific point in time. For example, objects in the line of sight (LOS) between the reader antenna and a tag may shadow or damp the emitted electromagnetic wave, preventing a successful reading operation [3]. Due to the passenger's movements, the UHF link conditions change over time, and the majority



(a) Portal arrangement of UHF RFID reader antennas.



(b) Distributed arrangement of UHF RFID reader antennas.

Figure 2.1: Examples of the UHF RFID reader antenna arrangement within a bus. The regions highlighted in green outline the UHF RFID reading zones. The HF RFID readers that passengers have to use for checking in after boarding are not shown (reprinted from [65], ©2015 IEEE).

of smart cards presumably can be detected at least occasionally. The alighting point of a passenger may be estimated by statistically analyzing the recorded reading operations of a specific smart card versus the time and the location. The distributed reader antenna arrangement aims at simplifying the reader installation within vehicles, and thus to reduce cost. For example, the UHF RFID antennas can be integrated in the roof panels of a bus, as shown in Fig. 2.1. Moreover, the number of antennas may be reduced at the expense of a lower accuracy regarding the assessment of the alighting point. The required range for the UHF RFID link in a system with distributed reader antennas is roughly 2 m to 3 m.

The operating range of a UHF RFID transponder can be estimated by Eqn. 1.7, as described in Sect. 1.1.2. Local regulations in general specify a maximum feeding power with

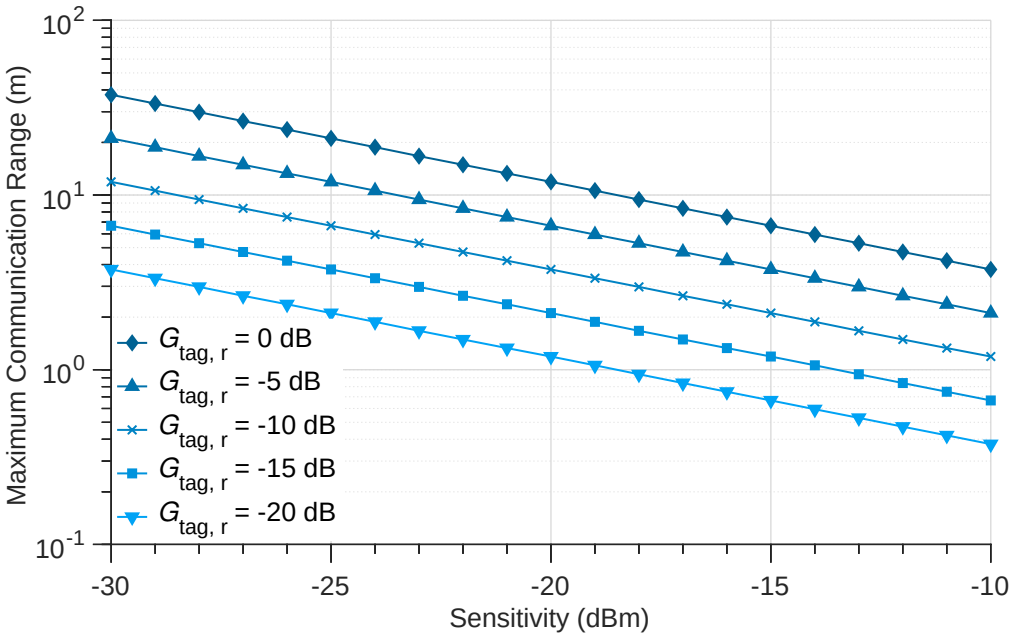


Figure 2.2: Maximum range of a UHF RFID communication link versus the sensitivity $P_{\min}$ of the used transponder IC for different values of the realized transponder antenna gain $G_{\mathrm{tag,r}}$. An $EIRP$ of 4 μW, a carrier frequency f_0 of 900 MHz and a polarization loss coefficient p of 0.5 are assumed.

respect to a reference antenna, and therefore limit the power density that may be emitted by a reader antenna in the direction of maximum gain. For example, according to FCC 47 CFR Ch. I Part 15 [46] a UHF RFID interrogator antenna in the U.S. may be operated with a maximum equivalent isotropically radiated power $EIRP$ of 4 W ($P_{\mathrm{int,TX}} G_{\mathrm{int}} \leq EIRP_{\max}$). The power transmission coefficient τ and the tag antenna gain G_{tag} can be combined to the realized antenna gain ($G_{\mathrm{tag,r}} = G_{\mathrm{tag}}\tau$), to quantify the influence of the antenna on the performance of an RFID transponder. Rewriting Eqn. 1.7 thus yields:

$$R_{\max} = \frac{\lambda}{4\pi}\sqrt{\frac{EIRP \cdot G_{\mathrm{tag,r}} \cdot p}{P_{\min}}}. \tag{2.1}$$

Figure 2.2 illustrates the free space communication range of passive UHF RFID transponders versus the sensitivity of the used transponder IC, according to Eqn. 2.1. Different values of $G_{\mathrm{tag,r}}$ are considered to illustrate the influence of the transponder antenna characteristics. The power consumption for writing to a NVM is mostly higher than for reading and therefore also the writing sensitivity of a tag IC is usually higher than the reading sensitivity. Present transponder ICs achieve reading and writing sensitivities of about -20 dBm and -15 dBm, respectively (e.g., [48]). Assuming a $G_{\mathrm{tag,r}}$ of 0 dB and considering the sensitivity figures stated above, state of the art passive transponders can reach more than 10 m read range, as shown in Fig 2.2. In contrast to this, the maximum communication distance for performing a writing operation is lower, ranging around 6 m to 7 m.

HF/UHF Dual Band Transponder Antennas

In the considered application scenario, the UHF antenna and the HF antenna coil have to be integrated in a single smart card, which typically corresponds to the ID-1 format ($85.60 \times 53.98\,\mathrm{mm}^2$), as defined in the ISO/IEC 7810 [19]. The ISO/IEC 14443 includes dedicated specifications, with respect to the usage of smaller form factors for the HF antenna coil [14, 100]. Therefore, the size of the HF antenna can be reduced considerably in favor of the UHF antenna. The confined space for the UHF antenna practically limits the bandwidth and the achievable antenna gain [33, 2].

Various forms of antennas for HF/UHF dual band transponders have been proposed in literature. They differ fundamentally in the assumptions regarding the properties and the number of the used transponder ICs. Apparently, using two separate HF and UHF transponder ICs enables the most flexibility with respect to arranging the antenna ports, and thus the two antenna structures. The dual band transponder described by Toccafondi and Braconi, for example, includes a meandered UHF dipole antenna and the HF coil next to each other [101]. Alternatively, the HF coil may be placed along the outer edged of the transponder, surrounding a dipole-like UHF antenna [102, 103, 104]. The larger coil area in this case enhances the performance of the HF RFID link. Similar design principles can be applied to transponder designs using a single HF/UHF dual band transponder IC with two dedicated RF interfaces, as demonstrated by Deleruyelle *et al.* [105] or recent commercially available HF/UHF dual band transponder inlays* (e.g., [106]).

Even compact UHF tag antennas with maximum dimension of lower than $\lambda/4$ may approach the gain of a $\lambda/2$ dipole antenna (2.15 dB) [33]. The maximum antenna gain as reported in the research literature on dual band transponders listed above nevertheless varies considerably. For practical implementations, a possible maximum gain of about 0 dB or less must be assumed for the UHF antenna of an HF/UHF dual band transponder (see [101, 104, 105]). Besides the limited available space, the coupling between the UHF antenna and the HF coil poses an additional degrading factor with respect to the antenna performance [105].

Furthermore, antenna designs for transponders using a single HF/UHF dual band tag IC with a single combined antenna interface have been proposed [107, 108]. As noted in Sect. 1.1.1, the resonance capacitance of HF RFID transponders is integrated directly on the transponder IC. The integrated capacitance is typically in a range of several 10 pF. In case of a combined HF/UHF antenna interface, the large shunt capacitance would provide a low impedance bypass path for the UHF signal, severely degrading the performance of the UHF interface. Integrating the resonance capacitor on a dual band tag IC with combined antenna interface is therefore not feasible. Instead the capacitance has to be realized as a part of the antenna structure, which complicates the antenna design (see [107, 108]). Alternatively, the HF and UHF signal paths of a combined front-end can be separated using coils integrated on the chip in combination with magnetically coupled HF or UHF booster antennas, as demonstrated by Pachler *et al.* [109].

*A transponder inlay corresponds to the assembly of an antenna and a transponder IC on a usually synthetic carrier material. An RFID label is manufactured by laminating and imprinting of the inlay.

Operating Conditions

The largest impact factor with respect to the performance of the UHF RFID link in the considered application scenario nevertheless is expected to arise from the operation of the transponders in close proximity to the human body. Body tissue is a highly absorbing material with a high dielectric constant at signal frequencies around 900 MHz [110]. In consequence, the antenna gain and the impedance matching or alternatively the realized gain $G_{\mathrm{tag,r}}$ of a transponder deteriorates considerably at a few millimeter distance from the human body. For example, the single-layer dipole-like antenna proposed by Kellomäki and Ukkonen that has specifically been designed for on-body operation shows a realized gain of lower than -10 dB at 4 mm distance to the human body [111]. Corresponding to this value of $G_{\mathrm{tag,r}}$, the theoretical read range of a transponder would decline to below 4 m, assuming a P_{min} of -20 dBm, as shown in Fig. 2.2. A sensitivity of around -18 dBm would be sufficient to achieve the required 2 m to 3 m read range for operating an AFC system.

The free space propagation model, as applied in Eqn. 2.1, neglects various effects that may be encountered in a realistic situation on a public transport vehicle. Furthermore, the operating conditions for the smart cards are mostly undefined in the AFC scenario, and can vary significantly from passenger to passenger depending on, for example, where the smart card is carried [9]. Considering the various impairments of the UHF RFID link, a UHF interface with a high sensitivity is desirable to achieve a high reading probability of the smart cards. Moreover, a high operating bandwidth is required to mitigate the effects of antenna detuning on the UHF link performance, resulting from changing conditions in the close proximity of the antenna [42]. A UHF RFID interface that covers the entire bandwidth from 860 MHz to 960 MHz, comprising the various operating bands as defined by local regulations [50], is in addition advantageous with respect to commercial aspects.

2.1.2 Security and Privacy

An AFC system that is capable of detecting and thus tracking passengers unobtrusively will inevitably increase already existing concerns regarding the protection of passengers' privacy. This affects the collection and processing of data by the operator of the AFC system, but also the data security versus unauthorized third parties.

Studies on the user acceptance of RFID technology have indicated that privacy or security concerns are relevant aspects, although less important than other factors such as the ease of use and the perceived usefulness (see [112, 113]). Regarding the introduction of novel smart card based systems however, questions of privacy usually play a prominent role in the accompanying public debate, which can influence the user adoption [114]. The availability of different types of tickets, mirroring the varying personnel notions of privacy, has been considered as one key factor for a successful adoption of smart cards [115]. For example, anonymous prepaid smart card a priori do not allow an association of personal information to the usage of a specific smart card. By incorporating additional information, the person carrying the card may be identified, nonetheless. System operators have to implement stringent policies on the collection and the usage of data to create thrust towards the users. Moreover, sufficiently strong security procedures have to be in place to prevent an unauthorized access of the collected data, or the smart cards.

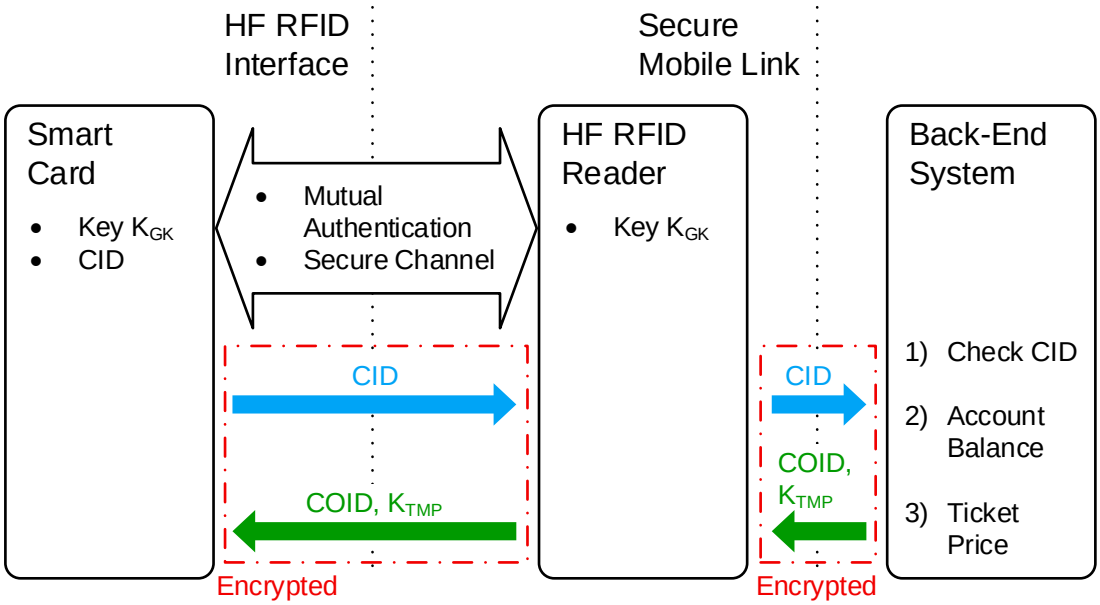


Figure 2.3: Active check-in procedure at an HF RFID reader. As in present AFC systems, the smart card is authenticated by means of a shared secret key K_{GK} (reprinted from [66], ©Springer Verlag Wien 2016).

Check-In Procedure

The check-in procedure using a HF/UHF dual band RFID transponder essentially relies on the same security mechanisms as in case of current contactless smart cards. Figure 2.3 illustrates the relevant protocol steps during a check-in at an HF RFID reader using a dual band smart card, as proposed by Gross and Spreitzer in [65, 66]. In a first step, a mutual authentication is performed and an encrypted communication channel is established. Primarily symmetric cryptographic methods (e.g., AES [116]) are applied in present AFC systems [1]. For instance, three pass mutual authentication [117] is a common security protocol to mutually authenticate two communication parties. In case of symmetric cryptography, both parties share the same secret key for encrypting and decrypting messages. The distribution of the keys in a secure way is a complex process and a major limitation of symmetric cryptography. The key K_{GK} of a specific smart card (see Fig. 2.3) is typically derived from the card identification number (CID) or from a part of it, and a master key to simplify the key management [1]. A smart card needs to transmit the conforming part of its CID unencrypted to the reader to enable the reader to calculate the correct key by using the master key. The corresponding group key K_{GK} is thus associated with a larger group of smart cards. Therefore, an unauthorized party is not able to identify and track a specific card.

As shown in Fig. 2.3, the smart card transmits its CID via the authenticated and secured channel to the back-end system in the following. The back-end checks the validity of the CID and eventually charges the associated account with the ticket price. In contrast to present AFC systems, the dual band smart card additionally receives a temporary key K_{TMP} and a one-time card identification number (COID) that are used in subsequent UHF RFID communication cycles.

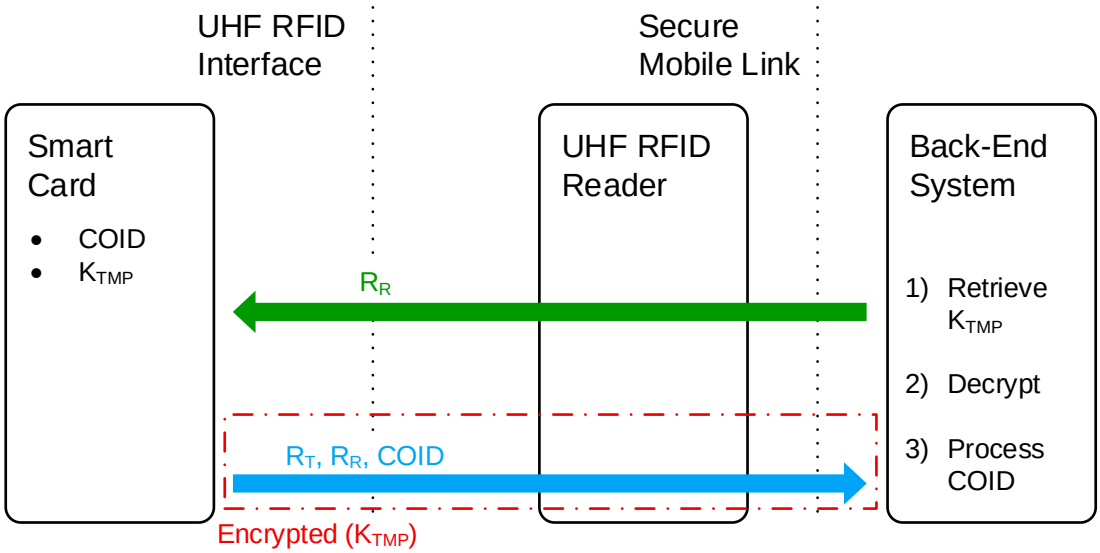


Figure 2.4: Communication protocol for a remote detection cycle of a smart card via the UHF RFID interface. The response of the smart card is encrypted using the temporary key K_{TMP} (reprinted from [66], ©Springer Verlag Wien 2016).

Remote Detection Procedure

Figure 2.4 illustrates the relevant protocol steps of a reading operation of a dual band smart card via the UHF RFID interface according to Gross and Spreitzer [65, 66]. Previous protocol steps like the anti-collision process are not shown. The back-end system initiates the communication by sending a random number or token R_R to the transponder. The transponder generates a second random token R_T. R_T, R_R and the COID are concatenated and encrypted using the key K_{TMP}. The encrypted message is sent to the back-end that retrieves K_{TMP}, and decrypts the message. In effect, the reader only acts as a means to bridge the data exchange with the back-end. Based on the received COID, the back-end determines the associated original CID of the smart card. The transponder response does not include any static information due to the two included random tokens, preventing tracking by an unauthorized party without knowledge of K_{TMP}.

The wide-spread availability of smart cards in an AFC system naturally facilitates the staging of physical attacks on the incorporated IC to retrieve stored secret information. For example, side-channel analyses allow a conclusion on the utilized secret keys by measuring and statistically evaluating specific characteristics like the power consumption of an IC during cryptographic operations [118]. Countermeasures against physical attacks require additional hardware efforts and cause a higher power consumption. An increased power consumption nevertheless degrades the sensitivity of a passive UHF RFID tag IC [52]. Eventually, it has to be assumed that the security of the UHF sub-system of an HF/UHF dual band transponder IC can be broken by a considerable lower effort than the HF sub-system due to the significantly lower demanded power consumption and the accordingly less sophisticated countermeasures against physical attacks.

The exchange of the temporary key K_{TMP} at every check-in, as illustrated in Fig. 2.3, can be utilized to mitigate the security risk regarding the UHF RFID interface. Even if K_{TMP} could be retrieved by an attacker, the key is possibly exchanged already at the next check-in

rendering the extracted secret key useless. As proposed by Gross and Spreitzer in [66], K_{TMP} may be updated once per day. More advanced schemes can be implemented at the cost of a higher effort for the key management. For example, different keys may be used for individual passes of bus or tram routes.

System Enhancements

As a consequence of the key exchange, the security of the UHF sub-system is closely connected to the protection mechanisms of the HF sub-system. If the security measures of the HF sub-system are surmounted, K_{TMP} can be captured easily. Several measures can be taken to enhance the security of the HF sub-system, and thus the entire AFC system. For example, the authentication process for the check-in may be shifted from the reader to the back-end system, which would allow the establishment of a unified secure end-to-end channel (see [66] for a more comprehensive discussion). The HF RFID reader, as a potential target for an attacker, merely bridges the communication between the back-end and a smart card in this case. The back-end can be protected more easily against physical attacks, in contrast to the multitude of readers in the field. Moreover, asymmetric or public-key cryptography* can be deployed such as elliptic curve cryptography (ECC). Public-key techniques are computationally more expensive than symmetric methods, requiring a significantly higher hardware effort, and thus also a higher power consumption [119]. Present high-end smart card ICs are already supporting the application of asymmetric cryptography like ECC (e.g., [23]). In contrast, the high power consumption or the increased computational delay as a trade-off, practically remain a considerable obstacle with respect to applying public-key methods for passive UHF RFID transponders.

2.2 HF/UHF Dual Band Transponder IC

Transport operators primarily aim at improving the effectiveness of public transportation in terms of service and cost with the introduction of AFC systems, as discussed in Sect. 1.2. Corresponding to this, the production costs of smart cards and the included transponder IC are highly sensitive factors. The cost of transponder ICs is linked to the area of the silicon die, but also the specific technology options that are used in a given process technology. Estimating a realistic scenario regarding the technology choices for future HF/UHF dual band transponder ICs requires to review possible options with respect to the IC architecture and the included HF and UHF analog front-ends.

2.2.1 IC Architecture

Figure 2.5 depicts a block diagram of the proposed HF/UHF dual band RFID transponder IC. The IC includes two separate analog front-ends, providing a proximity HF (ISO/IEC 14443 [14]) and a UHF RFID communication interface (ISO/IEC 18000-63 [49], EPC Generation-2 UHF [50]). An HF antenna coil is directly connected to the input terminals L_1 and L_2 of the HF front-end. The parallel resonance capacitor is directly integrated with the front-end

*Asymmetric cryptographic operations require the participating parties each to generate a pair of keys comprising a public and a private key. The public key is published and may be used by others to encrypt information to be sent to a specific party. Only the complementary secret private key of the intended receiving party can be used in the following to decrypt the information correctly.

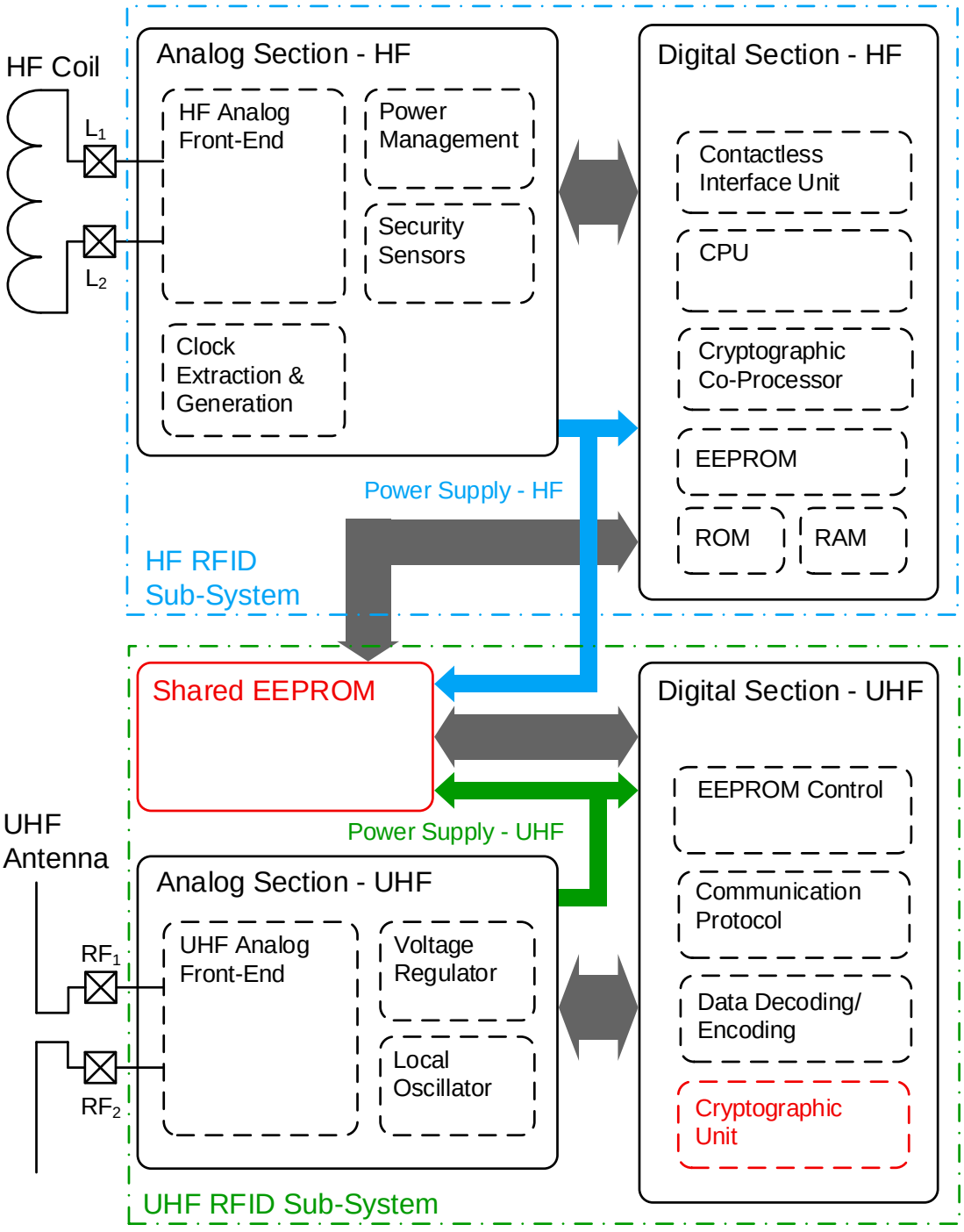


Figure 2.5: Block diagram of the proposed HF/UHF dual band RFID transponder IC for AFC applications. The transponder IC comprises two separate analog front-ends for the HF and the UHF communication interfaces that are directly connected to an HF coil and a UHF antenna, respectively (reprinted from [65], ©2015 IEEE).

circuit as in case of present HF RFID transponders (see Sect. 1.1.1). The RF input terminals of the UHF front-end RF_1 and RF_2 are connected to a separate UHF antenna.

In literature, HF/UHF dual band RFID tag ICs have been proposed that incorporate a single combined HF/UHF front-end (e.g., [67, 68, 70]). In contrast to this thesis, the listed publications however consider a combination of an EPC Class-1 HF [26] and an EPC Generation-2 UHF RFID interface [50]. Sharing a subset of the circuit structures of the front-end between both communication interfaces potentially allows to reduce the required die area, and thus fabrication costs of the IC. As noted in Sect. 2.1.1, antenna structures for combined HF/UHF front-ends are nevertheless more complex than standalone HF and UHF antennas, which might eventually pose a cost disadvantage with respect to the mass production of transponder inlays or smart cards. In case of a dual band transponder IC with separate front-ends, similar design principles and manufacturing technologies can be applied to the antennas, as used for present standalone HF and UHF RFID transponders. Using separate HF and UHF front-ends furthermore allows an optimization of the the two front-end circuits independently from each other, which is especially relevant for achieving a high performance for the UHF RFID interface.

The transponder IC depicted in Fig. 2.5 supports the protocol for securing the UHF RFID link, as described in Sect. 2.1.2. A shared EEPROM provides an interface between the HF and the UHF sub-systems for exchanging K_{TMP} and COID during a check-in operation. In a subsequent UHF communication cycle, the UHF sub-system can access the stored COID and the key K_{TMP} that is used to encrypt the response to the interrogator. The shared memory can be supplied from both the HF or the UHF domain. The power supplies of the two sub-systems are otherwise completely separated. If the two domains were connected to the same supply rail, the leakage current of the HF sub-system would pose an additional load for the UHF sub-system that could severely degenerate the sensitivity of the UHF RFID interface. A dedicated control circuitry is necessary to arbitrate the memory access and to switch the power supply for the memory accordingly.

A first commercial dual band transponder IC has been released in 2015 that comprises a proximity HF and a long-range UHF RFID interface according to the ISO/IEC 18000-63 and the ISO/IEC 14443, respectively [72]. The integrated NVM of the device is fully accessible via both communication interfaces, allowing to exchange data between the HF and the UHF operating domains. Nevertheless, this commercial tag IC does neither provide the required security features for HF nor for UHF operations (see Sect. 2.1.2).

HF RFID Sub-System

As shown in Fig. 2.5, the HF sub-system of the proposed dual band transponder IC for the most part resembles a state of the art HF RFID smart card IC (e.g., [22, 23]). Present smart card ICs incorporate a light-weight CPU requiring a random-access memory (RAM) for the execution of program code, as noted in Sect.1.1.1. The CPU typically runs a simple operating system from a read-only memory (ROM) that can handle multiple separate applets. An EEPROM allows the storage of customized application code and data, and therefore enables a flexible adaption of smart cards to new use cases. Furthermore, the digital section includes one or several dedicated cryptographic co-processors supporting symmetric or potentially also complex asymmetric cryptographic schemes such as ECC.

The contactless interface unit (CIU) shown in Fig. 2.5 constitutes the interface between the digital system and the HF analog front-end, handling the lower layers of the commu-

nication protocol according to ISO/IEC 14443. The analog section of the HF sub-system comprises power management and clock extraction circuits, besides the HF analog front-end. Providing a load modulation signal in compliance with ISO/IEC 14443 requires to recover the 13.56 MHz carrier signal that is emitted by the reader. A phase-locked loop (PLL) is typically used to extract the carrier frequency, and to generate the clock signal for the digital section [17]. In addition to this, several security sensors are incorporated to counteract physical attacks to the IC, specifically regarding the memory or the security relevant digital circuitry. These sensors can be, for example, light, temperature, and voltage sensors to monitor the environmental conditions and thus guarantee a correct operation of the digital circuits.

The features of HF RFID enabled smart card ICs have been notably increased with respect to the security and the application domain during the last decades (see [1]). This trend has been accompanied by a corresponding rise in the complexity of the digital sub-system of smart card ICs, which has eventually fostered the deployment of scaled CMOS technologies. With regard to market perspectives, an HF/UHF dual band smart card IC inevitably has to provide similarly sophisticated digital features as present contactless smart card ICs for e-ticketing, as described above. In consequence, the choice of process technology is governed by considerations of enhancing the performance, and reducing the die area or rather the cost that are associated with the digital section of the HF sub-system.

UHF RFID Sub-System

The digital section of the UHF RFID sub-system, as shown in Fig 2.5, is considerably less complex, compared to the HF sub-system. The UHF sub-system includes a hard-wired digital state-machine to handle the ISO/IEC 18000-63 communication protocol and the access to the shared EEPROM. The clock signal for the digital section is generated by an integrated local oscillator. A clock frequency of 1.92 MHz is required to reliably decode the PIE encoded signal, as defined in the ISO/IEC 18000-63 or the EPC Generation-2 UHF RFID standard [120]. The additionally included cryptographic unit implements a symmetric encryption primitive like AES, for example, to support the security protocol, as described in Sect. 2.1.2.

The feasibility of implementing symmetric cryptographic operations considering the stringent constraints on the power consumptions for UHF tag ICs has been demonstrated in literature [52, 53]. Moreover, a first commercial tag IC was released that supports cryptographic operations according to AES [54]. The circuit complexity of the cryptographic unit though is considerable in comparison to the digital logic for handling the communication protocol [52]. In line with this, the power consumption can be higher during the execution of cryptographic operations than for processing a standard read command, which diminishes the sensitivity of a passive tag IC (see Sect. 1.1.2) [53].

2.2.2 CMOS Technology

Publications on proximity HF RFID transponder ICs or front-ends (e.g.,[17, 21]), and UHF RFID circuits alike (e.g., [121, 122]), have predominately considered CMOS technologies at or above the 130 nm process node, so far. The requirements of the data processing capabilities and thus the complexity of the digital circuit domain of smart card ICs are growing vastly, as noted. The usage of more advanced CMOS technologies promises an advantage with respect to fabrication costs for successive generations of smart card ICs, as the costs per

transistor of digital circuits decrease [123]. The complexity and the cost of the fabrication process itself nevertheless rise with advancing CMOS technologies [123, 124], increasing the economic pressure of minimizing the variety of the used process options and the relative number of required processing steps, therefore.

Additionally to the improvement of cost efficiency, the scaling of CMOS technologies has enabled a continuous enhancement of power efficiency of digital circuits. The active power consumption of digital circuits decreases quadratically with the scaling factor for consecutive CMOS process nodes, according to the constant field scaling theory [125]. At technologies below the 130 nm node roughly, the power efficiency of low-power digital circuits may deteriorate, contrary to the classical scaling theory, as a result of the rising transistor leakage [126]. Minimizing the power consumption of digital circuits for a specific processing task requires effectively to find the optimum trade-off between active power consumption, static leakage power, and the processing speed.

Evidently, the architecture of the digital system of a contactless smart card IC or the considered dual band smart card IC is highly relevant for minimizing the overall power consumption and thus for achieving a low H_{min} (see Sect. 1.1.1). The instantaneous power consumption can be balanced by aligning the timing of the individual digital function blocks with the requirements of the communication protocol and the reader commands. The clock signal for inactive circuit blocks can be gated to reduce the stand-by power consumption [127]. The leakage current of the inactive circuit blocks may still pose a considerable load. Modern CMOS technologies provide multiple transistor types with different threshold voltages to facilitate the adaptation of circuit characteristics to the specific operating scenarios of digital circuit blocks [127]. Dedicated low-leakage or high-V_{th} transistors with an elevated absolute value of V_{th} enable a reduction of the leakage current of inactive digital blocks.

The architecture and the operating clocks for the different digital function blocks of UHF RFID tag ICs or the UHF sub-system of the considered dual band smart card IC have to be carefully optimized as well, to minimize the power consumption, and to achieve a low P_{min}. In principle, the same design techniques can be applied as in case of HF RFID transponder ICs. The comparably low clock rates for operating the digital logic of UHF RFID tag ICs allow in addition an aggressive lowering of the digital supply voltage, closely approaching the threshold voltage [128].

The advantage of scaled CMOS technologies in terms of power efficiency of digital circuits may potentially enhance the performance of complex HF RFID smart card ICs, but also low-power UHF RFID tag ICs (see [129]). Thoroughly assessing the potential of scaled technologies with respect to the performance of the digital section of an HF/UHF dual band transponder IC will require to consider the utilization of advanced low-power techniques specifically to tackle the issue of the increasing transistor leakage. For example, forward and revere body biasing of digital cells may enable a dynamic trade-off between data throughput versus leakage power, or power gating may be applied to decrease the stand-by leakage current [126, 127]. The investigation of power optimized architectures and implementations of the digital function blocks of an HF/UHF dual band transponder IC is out of scope of this thesis.

The choice of CMOS technology has different implications to the design of the analog front-end circuits than for the digital circuitry of an HF/UHF dual band transponder IC. In Sect. 2.2.3 and Sect. 2.2.4, I investigate the impact of technology scaling on the implementation of HF and UHF front-ends in general terms. Chapter 3 and Ch. 4 subsequently

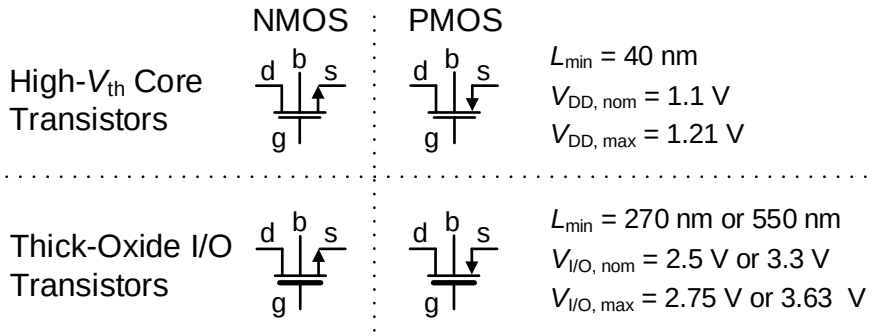


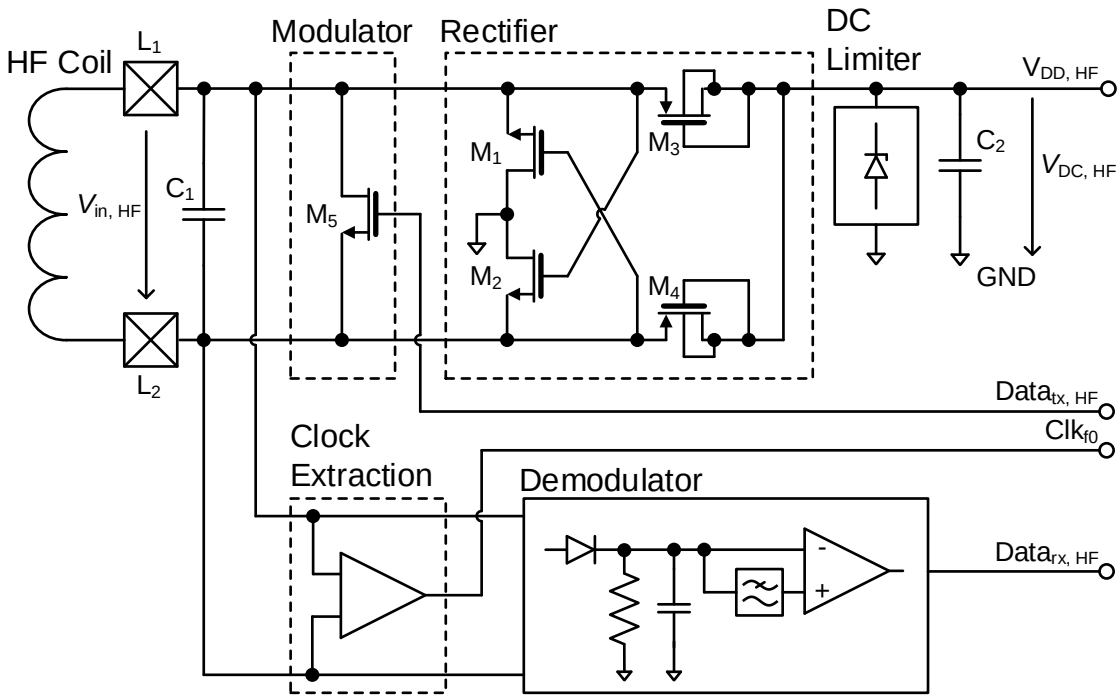
Figure 2.6: Overview of the utilized transistor types of the considered 40 nm CMOS technology and the circuit symbols used in this work. The transistor terminals are denoted by corresponding letters: gate (g), drain (d), source (s), and bulk (b).

discuss in detail examples of circuit designs of RF-DC power converters and the overvoltage protection for a passive UHF RFID front-end in an advanced process node. I consider specifically circuit designs in a low-power 40 nm CMOS process that represents a potential manufacturing technology for coming generations of smart card ICs. The chosen process provides a deep n-well implant that enables the fabrication of isolated p-wells as required for the implementation of forward and revere body biasing techniques for digital circuits (see [126]). As an additional measure to enhance the cost-efficiency, the available types of transistors are restricted to high-V_{th} core transistors and dedicated input/output (I/O) transistors with elevated maximum voltage ratings. The usage of high-V_{th} transistors allows to reduce the leakage current of digital logic cells, as noted, which is in particular relevant regarding the power consumption of the digital section of the HF RFID sub-system.

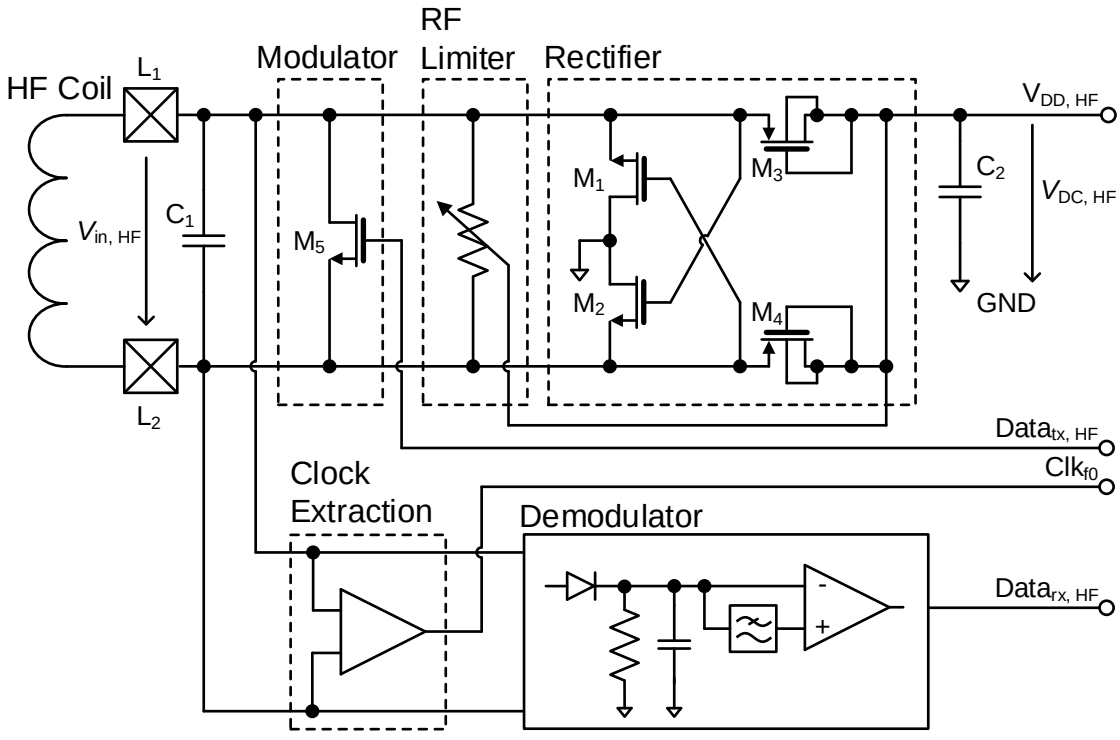
Figure 2.6 shows the circuit symbols that are used for the different transistor types in this thesis. Furthermore, the most relevant device parameters are summarized. The nominal $(V_{\mathrm{DD,nom}})$ and maximum supply voltage $(V_{\mathrm{DD,max}})$ of the thin-oxide high-V_{th} transistors equal 1.1 V and 1.21 V, respectively. In contrast to this, the nominal supply voltage of the thick-oxide I/O transistors $V_{\mathrm{I/O,nom}}$ is considerably higher with a value of 2.5 V or 3.3 V, depending on the considered minimum transistor channel length $(L_{\mathrm{min}}= 270\,\mathrm{nm}$ or $550\,\mathrm{nm})$. The corresponding maximum supply voltage of the I/O transistors $V_{\mathrm{I/O,max}}$ equals 2.75 V or 3.63 V.

2.2.3 HF RFID Analog Front-End

Figure 2.7 shows two block diagrams representing typical HF RFID analog front-ends (e.g., [11, 16]). The two diagrams are identical, with the exception of the arrangement of the voltage limiting circuits. A rectifier provides a DC supply voltage for the transponder circuit by rectifying the received carrier signal at the input terminals L_1 and L_2. The cross-coupled n-type metal oxide semiconductor (NMOS) transistor pair M_1, M_2 aligns the chip ground node GND with the negative signal peaks at L_1 and L_2. The negative voltage swing at the input terminals with respect to GND is limited effectively to a few 100 mV preventing an unintended forward biasing of the parasitic substrate diodes of MOS devices. The diode connected p-type metal oxide semiconductor (PMOS) transistors M_3, M_4 rectify the positive signal peaks. The capacitor C_2 decouples the rectified RF signal at the supply node $V_{\mathrm{DD,HF}}$.



(a) HF RFID front-end including a DC voltage limiter.



(b) HF RFID front-end including an RF voltage limiter.

Figure 2.7: Block diagrams of two HF RFID front-ends with a DC and an RF voltage limiter (e.g., [11, 16]). Both circuit arrangements effectively allow the regulation of the voltage amplitude $\hat{V}_{\text{in, HF}}$ at the RF terminals L_1, L_2 of the front-end and the rectified voltage $V_{\text{DC, HF}}$ at the internal DC supply net $V_{\text{DD, HF}}$ versus a rising magnetic field strength.

In the circuit of Fig. 2.7a, a DC voltage limiter is connected at the output of the rectifier at node $V_{DD,HF}$. The DC limiter corresponds to a shunt regulator that regulates the rectified voltage $V_{DC,HF}$ to a constant value versus a varying magnetic field strength, protecting the connected circuits from overvoltage conditions. The peak voltage at the input terminals closely follows the regulated voltage at $V_{DD,HF}$ due to the non-linear characteristic of the rectifying transistors. Therefore, the DC limiter effectively prevents an overvoltage at the devices that are directly connected to L_1 or L_2. In case of the front-end circuit shown in Fig. 2.7b, the input voltage amplitude $\hat{V}_{in,HF}$ is directly regulated by means of an RF voltage limiter. The RF limiter senses the rectified voltage at node $V_{DD,HF}$, and controls $\hat{V}_{in,HF}$ by adjusting the input resistance with respect to L_1 and L_2 (see [11]). Numerous circuit arrangements have been proposed for the regulation of $\hat{V}_{in,HF}$ and $V_{DC,HF}$ including also a hybrid approach that uses an RF and a DC limiter [16].

As illustrated in Fig. 2.7, the demodulator of an HF RFID front-end typically comprises an envelope detector and comparators to demodulate the ASK modulated signal transmitted by the reader. Demodulator architectures that support VHBR including the PSK based scheme as defined in the ISO/IEC 14443-2 [14] are considerable more complex, in contrast (e.g., [16, 17]). The shunt transistor M_5 of the load modulator allows the modulation of the input impedance of the transponder IC to send data to the reader. The digital I/Os $Data_{tx,HF}$ and $Data_{rx,HF}$ of the modulator and the demodulator, respectively, are connected to the CIU (see Fig. 2.5). The clock signal Clk_{f0} that defines the timing of the communication protocol between a reader and a transponder is extracted from the received carrier signal by means of an amplifier.

As noted in Sect. 1.1.1, the load modulation amplitude that is received at the reader antenna is strongly dependent on the applied change of the transponder's quality factor ΔQ_{HF}, and thus Q_{HF}. Considering Eqn. 1.3 and Eqn. 1.4, Q_{HF} can be expressed by means of the input voltage amplitude $\hat{V}_{in,HF}$:

$$Q_{HF} = 2\pi f_r C_{P,HF} \frac{\eta_{HF} \hat{V}_{in,HF}^2}{2P_{DC,HF}}. \tag{2.2}$$

The power conversion efficiency η_{HF} in Eqn. 2.2 relates the input power $P_{in,HF}$ to the DC power $P_{DC,HF}$ that is delivered at the output of the HF rectifier at node $V_{DD,HF}$ in Fig. 2.7 (η_{HF}=$P_{DC,HF}/P_{in,HF}$). Assuming η_{HF} and $P_{DC,HF}$ as fixed, Q_{HF} and thus the load modulation amplitude is determined by $C_{P,HF}$ and $\hat{V}_{in,HF}$.

$C_{P,HF}$ corresponds to the resonance capacitance of an HF RFID transponder, which effectively comprises the parasitic capacitances of the front-end circuit, and a dedicated integrated capacitor (C_1 in Fig. 2.7). HF RFID transponder ICs are delivered with multiple values of input capacitance to support different antenna form factors [20]. Typical values of capacitance are, for example, 20 pF for standard ID-1 antennas or 70 pF for supporting smaller antenna form factors [22]. As indicated by Eqn. 2.2, decreasing $\hat{V}_{in,HF}$ necessitates a quadratic increase of $C_{P,HF}$ to maintain an equal value of Q_{HF}. A larger value of $C_{P,HF}$ nevertheless requires a scaling of C_1, and thus an increase of the die area, which is associated with higher manufacturing costs.

Figure 2.8 shows a block diagram of the supply voltage regulation and clock generation circuits of an HF transponder IC that are directly connected to the front-end (e.g., [17, 21]). The internal supply voltage $V_{DDI,HF}$ for the analog or the digital core circuits is controlled by a series voltage regulator according to a reference voltage (V_{ref}). V_{ref} may be derived, for

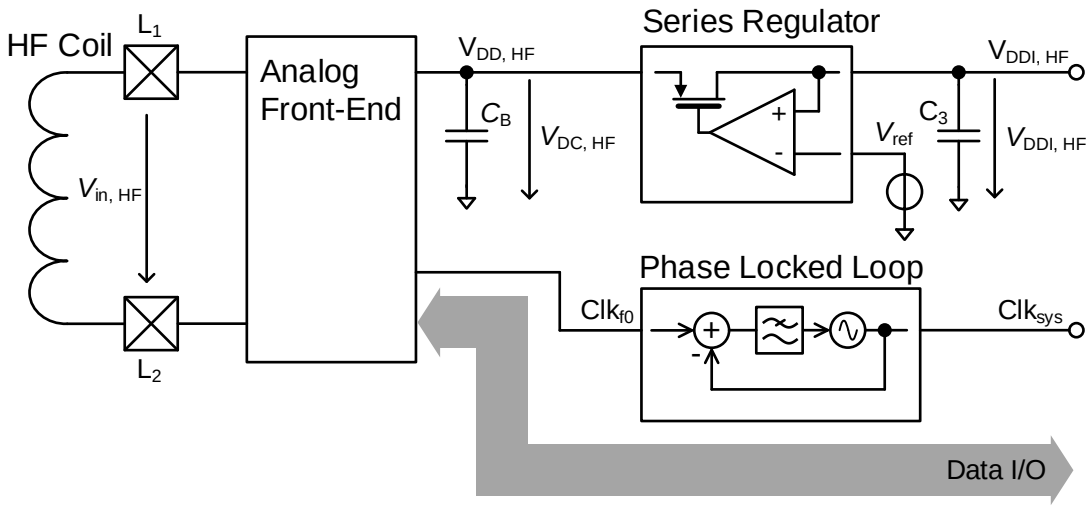


Figure 2.8: Block diagram of the voltage regulation and the clock generation circuits that build the interface between the front-end and the analog and digital core circuitry.

example, from a bandgap voltage reference. Multiple regulated supply domains are used for different sub-systems in an actual transponder IC. A PLL generates the clock signals for the digital circuit blocks using the extracted carrier frequency as a reference. During a modulation pulse of the ASK modulated reader signal (with $m \approx 100\,\%$) or the load modulated signal of the transponder, neither the reference frequency nor power are available from the magnetic field emitted by the reader. The storage capacitor C_B buffers energy to supply the transponder circuit for this period of time. Complementary to this, the PLL can be operated in an open loop mode to maintain a stable system clock during a modulation pulse.

The supply voltage $V_{\mathrm{DDI,HF}}$ for the analog and digital circuitry are fixed in general according to circuit specifications (e.g., regarding the maximum delay of a digital logic path). Assuming the usage of a series regulator, the minimum required voltage at the storage capacitor $V_{\mathrm{DC,min}}$ to allow a stable circuit operation is roughly equal to $V_{\mathrm{DDI,HF}}$. The maximum voltage at the storage capacitor $V_{\mathrm{DC,max}}$, on the other hand, is primarily determined by the maximum voltage ratings of the devices that are connected at $\mathrm{V_{DD,HF}}$ (see Fig. 2.8). The voltage limiter regulates $V_{\mathrm{DC,HF}}$ to a value of $V_{\mathrm{DC,max}}$ at high field strengths. As noted, the input voltage amplitude $\hat{V}_{\mathrm{in,HF}}$ at the front-end closely follows the regulated value of $V_{\mathrm{DC,HF}}$. Considering a constant value of the load current I_L and a specific duration T_m of a modulation pulse, a minimum value of C_B can be estimated that is required to supply the IC during a modulation pulse, preventing a power reset to occur:

$$C_\mathrm{B} \geq \frac{I_\mathrm{L} T_\mathrm{m}}{V_{\mathrm{DC,max}} - V_{\mathrm{DDI,HF}}}. \tag{2.3}$$

In an alternative approach, a switched-capacitor DC–DC converter may be used, for example, to convert the voltage level at the storage capacitor $V_{\mathrm{DC,HF}}$ to a specific value of $V_{\mathrm{DDI,HF}}$ (see [130]). In comparison to a series regulator, a voltage conversion using a switched-capacitor DC–DC converter is more efficient at higher conversion ratios and allows the discharge of C_B to a voltage level $V_{\mathrm{DC,min}}$ that is lower than $V_{\mathrm{DDI,HF}}$. $V_{\mathrm{DC,min}}$ corresponds in this case to the minimum voltage that is required to operate the switched-capacitor circuit and to provide a stable supply voltage $V_{\mathrm{DDI,HF}}$ at its output. Assuming a

constant power consumption P_L of the core circuitry and an ideal voltage converter, a minimum required value of C_B can be estimated, similarly as in the previous case considering a series voltage regulator (Eqn.2.3):

$$C_B \geq \frac{2P_L T_m}{V_{DC,max}^2 - V_{DC,min}^2}. \tag{2.4}$$

Equation 2.3 and Eqn. 2.4 imply that lowering $V_{DC,max}$ and associated with it $\hat{V}_{in,HF}$ has to be compensated by a higher value of C_B to guaranty a stable circuit operation during a modulation pulse at fixed load conditions. Scaling up the storage capacitor nevertheless requires a higher die area with regard to a specific CMOS technology. The overall storage capacitance of proximity HF RFID transponder ICs is typically in a range of several nF, and occupies a considerable fraction of the die area.

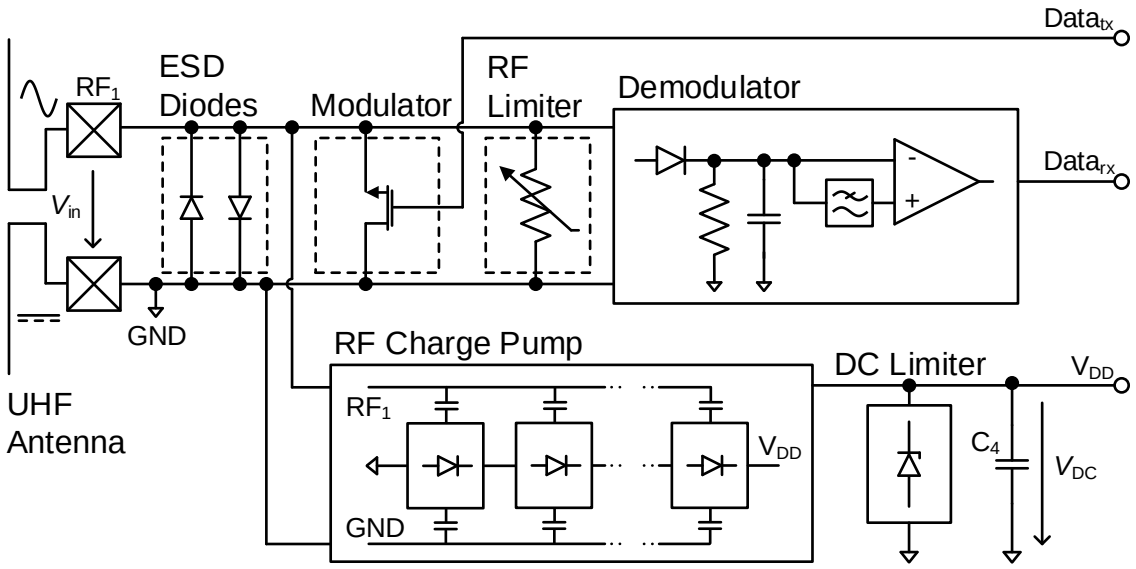
HF RFID Front-Ends in Scaled CMOS Technologies

As result of the dependence of ΔQ_{HF} (Eqn.2.2) and the sizing of the storage capacitor C_B on the input voltage amplitude $\hat{V}_{in,HF}$ (Eqn. 2.3 and Eqn. 2.4), the margin for lowering $\hat{V}_{in,HF}$ has been limited. Typical values of $\hat{V}_{in,HF}$ of present proximity HF RFID transponder ICs are in a range of about 3 V [20]. The maximum voltage rating of thin-oxide core transistors in a 180 nm CMOS technology equals about 2 V, in comparison. In the considered 40 nm process node, $V_{DD,max}$ is yet lower with a value of only 1.2 V (see Fig. 2.6). Therefore, thick-oxide I/O transistors with elevated voltage ratings have to be used for the implementation of HF RFID front-end circuits, as illustrated in Fig. 2.7 (see [131]). The characteristics of dedicated I/O transistors supporting a certain logic level (e.g., 3.3 V) have been similar for consecutive CMOS process nodes. Consequently, the same circuit structures as used in previous generations of transponder ICs can be applied for the implementation of HF RFID analog front-ends in advanced CMOS technologies, without considerable modifications.

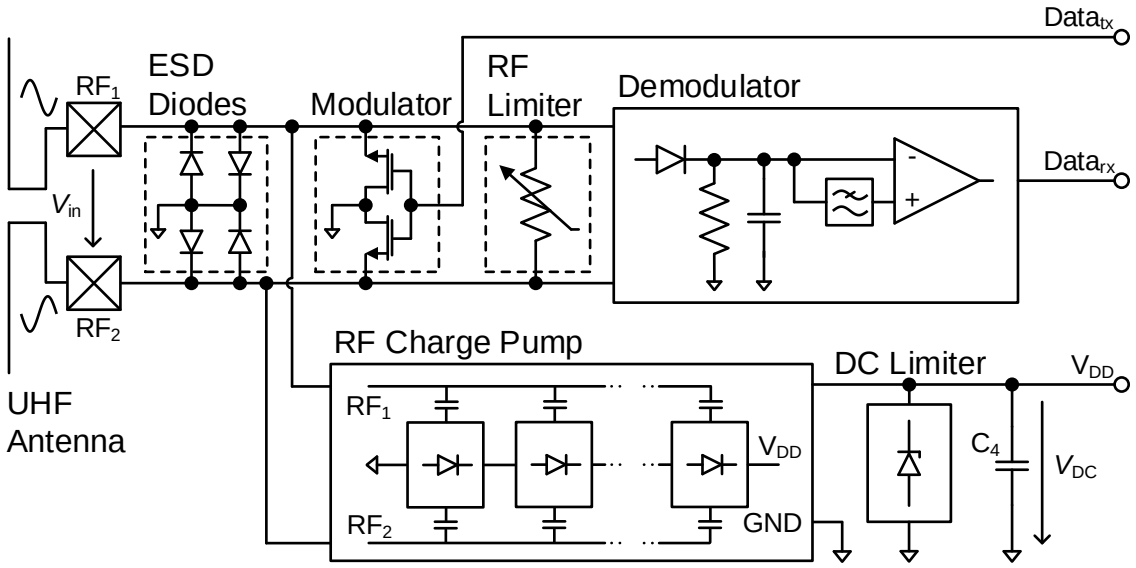
2.2.4 UHF RFID Analog Front-End

Figure 2.9 shows block diagrams of a single-ended (Fig. 2.9a) and a differential UHF RFID front-end (Fig. 2.9b). The ground node GND of a single-ended front-end is directly connected to one of the antenna terminals (e.g., [44]). In case of a differential front-end, the voltages at the RF terminals RF_1 and RF_2, with reference to GND, are defined by the circuit structures connected in between. The input circuit structures of a differential front-end are ideally symmetrical, resulting in a perfectly balanced signal swing at RF_1 and RF_2 relative to GND. Apart from that, the circuit blocks of the two depicted front-ends are functionally identical.

The RF-DC power converter or alternatively the RF charge pump, as shown in Fig. 2.9, rectifies the signal impinging at the antenna, and provides a DC voltage at its output at node V_{DD} that is used as voltage supply for the connected core circuitry. The output voltage level V_{DC} of the RF charge pump is regulated by a DC voltage limiter to protect the core circuitry from overvoltage conditions at high levels of received power. The capacitor C_4 decouples the rectified RF signal at node V_{DD}. Moreover, C_4 poses a fraction of the buffer capacitance C_B that buffers energy to supply the transponder circuit during modulation pulses.



(a) Single-ended UHF RFID front-end.



(b) Differential UHF RFID front-end.

Figure 2.9: Block diagrams of a single-ended and a differential passive UHF RFID front-end (e.g., [44, 121]). In case of a single-ended tag IC, the ground node GND of the IC is directly connected to one of the antenna terminals.

The modulator of a UHF RFID front-end consists typically of shunt transistors that allow a modulation of the backscattered signal and thus to communicate with a reader, as noted in Sect. 1.1.2. The ASK modulated signal transmitted by the reader is demodulated by means of an envelope detector and a comparator. The digital I/Os of the modulator and the demodulator Data_{tx} and Data_{rx}, respectively, are connected to the data decoding/encoding unit in the digital section of the transponder IC (see Fig. 2.5). Furthermore, the block diagrams of Fig. 2.9 comprise an ESD protection circuit and an RF voltage limiter.

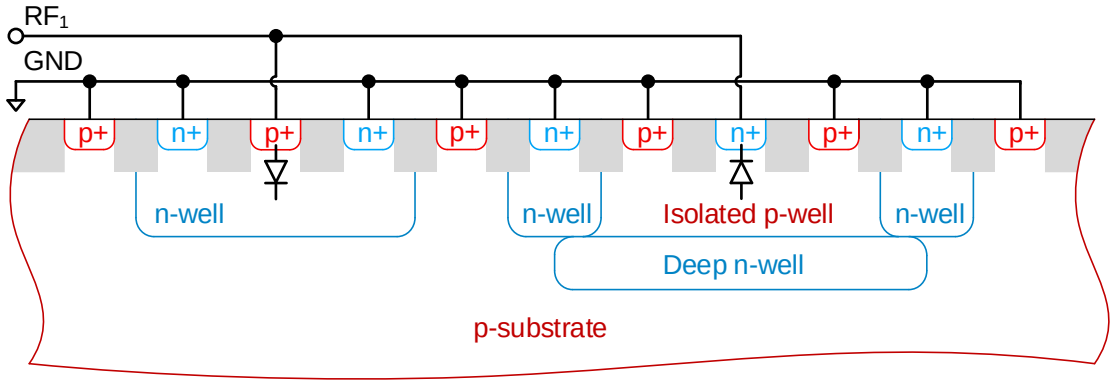


Figure 2.10: Simplified cross section of the antiparallel ESD protection diodes that are connected to the RF terminals of the front-end (see Fig. 2.9). The p-n junction diode formed at the interface between the highly doped p-diffusion p+ (n-diffusion n+) in the contact region and the n-doped well (isolated p-well) beneath is forward-biased during positive (negative) ESD pulses at RF_1 with respect to GND.

As illustrated in Fig. 2.9a, the ESD protection of a single-ended front-end may merely consist of a pair of antiparallel p-doped/n-doped semiconductor junction (p-n junction) diodes. Considering a typical forward voltage drop of roughly 0.6 V, the p-n junction diodes effectively clamp the RF input voltage amplitude $\hat{V}_{\text{in}}$ at high levels of available power at the antenna, protecting the circuit structures connected to the RF terminals from overvoltage conditions.* In this case, no additional RF limiter circuit would be necessary to avert damaging overvoltages.

Figure 2.10 exemplifies a cross sectional view of the ESD diodes. The two p-n junction diodes are formed by the highly doped p+ and n+ diffusions in the contact regions and the n and p-doped wells beneath, respectively. The well contacts are placed closely to the p+ and n+ diffusions to minimize the series resistance and thus to optimizes the effectiveness of the devices with respect to ESD events. As shown, a triple well structure may be used to form an isolated p-well, separating the n+ diffusion diode from the p-doped substrate.

UHF RFID Front-Ends in Scaled CMOS Technologies

Figure 2.10 shows that the structure of the ESD diodes is inherently asymmetric. In case of a differential UHF RFID front-end, two pairs of ESD diodes are thus connected symmetrically between RF_1 and RF_2 with reference to GND, as illustrated in Fig. 2.9b. The clamping voltage of the ESD diodes doubles in consequence, approaching values that can exceed the maximum voltage ratings of the thin-oxide core devices in advanced CMOS technologies (e.g., $V_{\text{DD,max}}$=1.2 V in the considered 40 nm CMOS process). The usage of thick-oxide I/O devices for implementing the front-end circuits is not desirable in this case due to the associated penalty in RF performance (see Sect. 3.2.3). An additional RF voltage limiter has to be used to prevent overvoltage stress at the front-end during operations and thus to mitigate potential reliability risks in the long term. This implies a higher circuit complexity

*The RF charge pump is typically operational at input voltage amplitudes lower than 300 mV, as discussed in more detail in Ch. 3. The ESD diodes show only a negligible impact with respect to the power conversion efficiency of the front-end at this level of input voltage.

for differential front-ends in contrast to single-ended circuit realizations in advanced CMOS technologies.

Nevertheless, differential front-ends show distinctive advantages with respect to other aspects compared to single-ended front-ends. The skew-symmetric input characteristic of differential circuits inherently suppresses even-order harmonic signal components that may arise due to non-linearity [132]. A reduction in the backscattered signal strength at harmonic frequencies poses a benefit with respect to electromagnetic compatibility (EMC) matters.* Moreover, differential RF charge pumps achieve typically a higher power conversion efficiency than single-ended circuit implementations, as discussed in Sect. 3.2.3 in more detail. I focus in this work therefore on the design of differential UHF RFID front-ends.

The introduction of V_{th} compensation techniques has allowed an enhancement of the power conversion efficiency and a reduction of the input quality factor of RF charge pumps at low input powers. This has facilitated the implementation highly sensitive and broadband UHF RFID transponders. Nevertheless, the restrictions on available process options that are typically imposed as cost reducing measures constitute a major challenge with respect to the design of high performance RF charge pumps. The usage of high-V_{th} transistors allows the mitigation of the increasing leakage current of digital circuit blocks, as encountered in scaled CMOS technologies. On the other hand, a higher absolute value of V_{th} requires to raise the biasing voltages for the V_{th} compensation of the rectifying transistors of the RF charge pump. Therefore, existing concepts for the associated biasing circuits have to be reconsidered in order to achieve the demanded higher bias voltages.

2.3 Summary

The introduction of HF/UHF dual band RFID transponders in AFC systems could enable transport operators and municipal authorities to gain valuable insight on the usage of high-capacity public transportation networks in a timely manner. The additional UHF RFID interface allows to remotely detect the presence of passengers, and thus to estimate their alighting point, without requiring the passenger to actively perform a check-out transaction. The specific use case poses nevertheless high requirements on the RF performance and the security of the UHF RFID communication link.

The remote detection feature may enhance the passengers' convenience, just as it might augment already existing concerns with respect to privacy. A corresponding HF/UHF dual band smart card IC has to provide appropriate security measures to prevent an unauthorized tracking of the smart card. This can be a critical factor for gaining the trust of passengers and for promoting user acceptance. The key exchange procedure relying on the secured HF RFID interface as proposed by Gross and Spreitzer in [65, 66] and summarized in Sect. 2.1.2 poses an efficient solution for securing the UHF RFID link.

The complexity of the digital domain of contactless smart card ICs is expanding in response to the growing requirements on security and the supported use cases. Inevitably, this trend fosters the usage of scaled CMOS technologies for successive generations of smart card ICs. The adoption of highly scaled CMOS technologies incorporates specific challenges with regard to the design of the UHF RFID front-end of an HF/UHF dual band smart card IC. The reduced maximum voltage ratings in advanced CMOS processes increase the risk of overvoltage at the UHF front-end at high levels of received power at the antenna potentially

*In contrast to passive HF RFID transponders, UHF RFID tags are subject to EMC regulations (e.g., [47]).

degrading the circuit reliability. Dedicated RF voltage limiter circuits have to be introduced to avert damaging overvoltages at the RF terminals of differential UHF RFID front-ends.

The economic pressure for streamlining the set of process options rises regarding the design of RFID transponder ICs in advanced CMOS process nodes, as equipment and processing costs surge. The inherent trade-off between cost and circuit performance in particular affects the RF charge pump that determines to a large extend the performance of the UHF RFID front-end. Existing circuit concepts for RF charge pumps have to be extended to account for the specific characteristics of highly scaled low-cost CMOS processes such as the raised threshold voltage of the used low-leakage transistor types.

3 RF-DC Power Converters

The bandwidth and the sensitivity of a passive UHF RFID transponder are strongly affected by the characteristics of the integrated analog front-end and specifically by the RF-DC power converter. The input quality factor Q of the RF-DC power converter or alternatively the RF charge pump gives an upper limit for the achievable operating bandwidth, on one hand (see Eqn. 1.9). The power conversion efficiency, on the other hand, determines the sensitivity of the transponder IC, assuming a fixed DC power consumption for the core circuitry of a tag IC. The introduction of V_{th} compensation techniques has enabled an improved power conversion efficiency and a lower input quality factor of CMOS RF charge pumps at low RF input powers.

This chapter provides an introduction to design principles of single-ended and differential RF charge pumps. I discuss the design trade-offs of using different circuit topologies and V_{th} compensation techniques. Subsequently, I present three RF charge pumps that have been designed in the given 40 nm CMOS technology (see Sect. 2.2.2). The circuit designs exclusively use high-V_{th} transistors, and therefore conform to a cost-effective implementation scenario for a future HF/UHF dual band RFID smart card IC. The first RF charge pump builds upon on an existing circuit topology applying only gate biasing for compensating the V_{th} of the rectifying transistors. In the remaining two circuits, I have introduced a combined gate and bulk biasing scheme to further improve the power conversion efficiency. I present measurement results of the static characteristics of the circuits for a continuous wave (CW) stimulus at room temperature. Furthermore, I demonstrate the dynamic operation of the charge pumps for modulated waveforms and investigate the start-up behavior at a varying ambient temperature.

Original Publications Related to This Chapter

L. Zöscher, P. Herkess, J. Grosinger, U. Muehlmann, D. Amschl, H. Watzinger, and W. Bösch, "Threshold voltage compensated RF-DC power converters in a 40 nm CMOS technology," in *2016 Austrochip Workshop on Microelectronics (Austrochip)*, Villach, Austria, Oct. 2016, pp. 30–34.

L. Zöscher, P. Herkess, J. Grosinger, U. Muehlmann, D. Amschl, and W. Bösch, "A differential threshold voltage compensated RF-DC power converter for RFID tag ICs," in *2017 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC)*, Graz, Austria, April 2017, pp 71–73.

L. Zöscher, P. Herkess, J. Grosinger, U. Muehlmann, D. Amschl, and W. Bösch, "Passive differential UHF RFID front-ends in a 40 nm CMOS technology," in *2017 47th European Microwave Conference (EuMC)*, Nuremberg, Germany, Oct. 2017, pp. 105–108.

Table 3.1: Design specifications of the UHF RFID front-ends, and in particular of the RF charge pumps, as presented in this work.

Parameter	Specification
$P_{\mathrm{DC,\,min}}$	$4\,\mu$W @ $V_{\mathrm{DC}} = 1$ V
η	$> 40\,\%$ @ $P_{\mathrm{DC,\,min}}$
Q	10 @ $P_{\mathrm{DC,\,min}}$
f_0	860 MHz – 960 MHz
C_{par}	~ 200 fF

3.1 Design Specifications

The operating conditions and the requirements of RF-DC power converters vary considerably, depending on the specific application. In case of RF energy harvesters, the rectified RF power is typically delivered to a larger external energy storage (e.g., [78, 87]). If the stored energy level reaches a specific threshold, a connected sensor circuit can be operated for a short period of time, for example, to perform a series of measurements and transmit the results to a central gateway node. The charging time of the energy storage can be traded off against the DC power, which is delivered by the RF energy harvester, enabling potentially a lower sensitivity value and a higher communication range.

In case of passive RFID transponders, the rectified RF power is directly supplied to the core circuitry of the transponder IC. The sensitivity is thus depending on the instantaneous power consumption of the IC. Moreover, a larger operating bandwidth is usually required to mitigate detuning effects of the antenna in consequence of the undefined operating condition of UHF RFID transponders, as noted in Sect. 2.1.1. I consider in the following section design examples of simplified RF charge pump circuits to discuss general design principles, and to substantiate specific decisions with respect to the circuit implementations that are presented in Sect. 3.3. The simplified example circuits have been designed according to the target specifications of the UHF RFID front-ends presented in this work.

Table 3.1 summarizes the target specifications for the UHF RFID front-ends or more specifically the RF charge pumps. The performance characteristics of RF charge pumps are strongly dependent on the input voltage amplitude and the load conditions at the output. Thus, the specifications of RF charge pumps are typically referred to a particular DC operating point that is defined by the output voltage V_{DC} and the output current I_{DC}, or alternatively the DC output power P_{DC}. I estimate the minimum required DC power $P_{\mathrm{DC,\,min}}$ to supply the UHF RFID sub-system of a dual band transponder, assuming an average current consumption of $2\,\mu$A and a supply voltage of 1 V. These values are roughly in line with recent publications on UHF RFID baseband processors that support symmetric cryptographic operations (see [52, 53]). For a typical backscatter modulation waveform with a duty cycle of 50 %, the RF charge pump has to deliver effectively twice the current ($4\,\mu$A) to the buffer capacitor (C_4 in Fig. 2.9) and the connected circuitry to maintain a stable supply voltage level. Thus, $P_{\mathrm{DC,\,min}}$ virtually doubles to $4\,\mu$W. As shown in Table 3.1, a power conversion efficiency η of larger than 40 % has been targeted for the RF charge pumps.* An η of 40 % corresponds to a sensitivity P_{min} of -20 dBm considering a $P_{\mathrm{DC,\,min}}$ of $4\,\mu$W.

*η relates the RF input power P_{in} to the DC output power P_{DC} of an RF charge pump or a UHF RFID front-end depending on the considered context ($\eta = P_{\mathrm{DC}} / P_{\mathrm{in}}$) analogously to η_{HF}.

The UHF RFID front-ends should exhibit a low quality factor Q of around 10 at an input power level of P_{min} to allow a broadband impedance matching to a transponder antenna. According to Eqn. 1.10, an input quality factor of 10 corresponds to a theoretical maximum bandwidth of about 250 MHz for the impedance match, assuming a center frequency of 900 MHz and a uniform return loss of 10 dB over the entire bandwidth. Thus, the front-ends enable the implementation of broadband transponders covering the entire range of operating frequencies in the band from 860 MHz to 960 MHz. The parasitic capacitances of other larger circuit structures of a front-end like the ESD protection and the modulator, which are directly connected to the RF terminals, additionally increase Q (see Eqn. 1.3). I assumed an additional parasitic capacitance C_{par} of 200 fF as a starting point for the design of the RF charge pumps.

3.2 Design Principles

3.2.1 Single-Ended RF Charge Pumps

In addition to rectifying the RF input voltage, the RF charge-pump of a UHF RFID transponder IC provides a voltage conversion between the RF input voltage amplitude $\hat{V}_{\text{in}}$ and the DC output voltage V_{DC}. The voltage conversion corresponds effectively to an impedance transformation translating a typically larger load resistance, as defined by P_{DC} and V_{DC}, to a lower input resistance. Equation 1.3 and Eqn. 2.2, rewritten below using the quantities as used in this work in the context of UHF RFID front-ends, illustrate the relationship between the quality factor Q, the equivalent parallel input resistance R_{P}, and the input voltage amplitude $\hat{V}_{\text{in}}$:

$$Q = 2\pi f_0 C_{\text{P}} R_{\text{P}} = 2\pi f_0 C_{\text{P}} \frac{\eta \hat{V}_{\text{in}}^2}{2P_{\text{DC}}}. \tag{3.1}$$

Equation 3.1 shows that lowering the input resistance R_{P} or alternatively the input voltage amplitude $\hat{V}_{\text{in}}$ results in a lower Q, assuming constant values for P_{DC} and the equivalent parallel input capacitance C_{P}.* $\hat{V}_{\text{in}}$ and thus Q can be reduced with respect to a fixed value of V_{DC} by using a multi-stage charge pump as a rectifier.

Early works on integrated front-ends for UHF RFID transponders mainly focused on single-ended charge pumps using Schottky diodes† as rectifying elements (e.g., [51, 133]). A Greinacher voltage doubler cell [134] typically builds the unit stage of a corresponding single-ended RF charge pump. The Schottky diodes can be replaced by MOS transistors that are operated in diode connection [43, 135]. The resulting circuit topology in essence equals a Dickson charge pump [136].

Figure 3.1 illustrates a CMOS implementation of a single-ended RF charge pump. The shown circuit corresponds to the unit stage number n of a charge pump comprising overall N_{st} unit stages $(1 \leq n \leq N_{\text{st}})$. Neglecting the gate bias voltages V_{N} and V_{P} in a first step, the rectifying transistors M_6 and M_7 are connected to operate effectively as diodes. The

*In this work, R_{P} and C_{P} are referring to the equivalent parallel input resistance and capacitance, respectively, of an entire UHF RFID front-end or an RF charge pump only, depending on the specific context.

†It is possible to implement Schottky diodes in standard CMOS processes without increasing the manufacturing costs by utilizing the silicide that is otherwise used to achieve low-resistance drain and source contacts (see [137]).

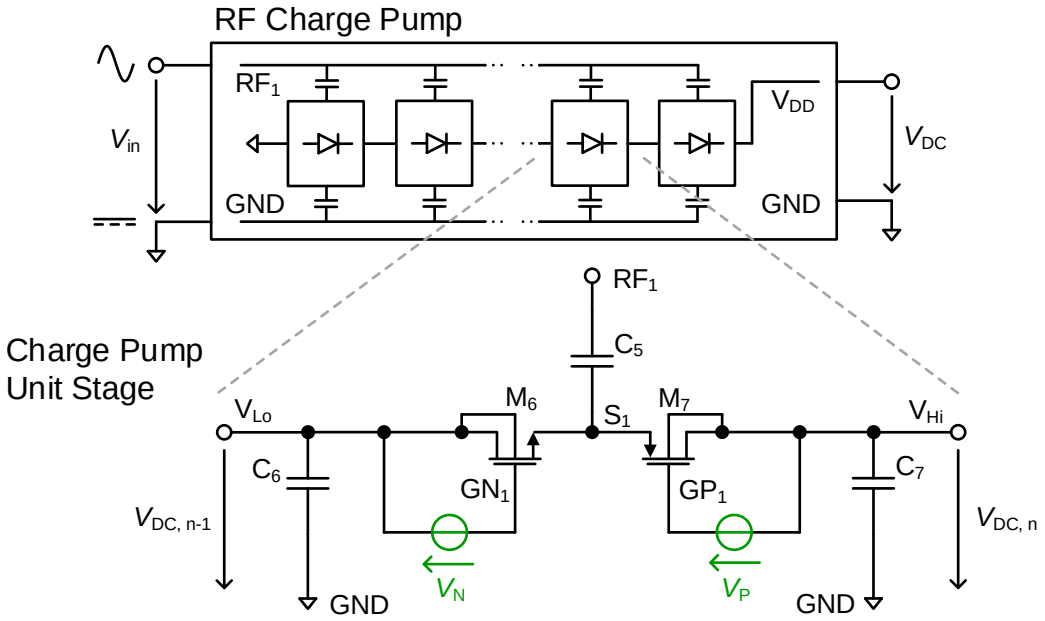


Figure 3.1: Simplified schematic of a single-ended charge pump stage. The biasing voltages V_{N} and V_{P} (highlighted in green) compensate the V_{th} of the rectifying transistors M6 and M7, respectively [76].

capacitor C_5 couples the RF input voltage to the node S_1 that is connected to the source terminals of the rectifying transistors. During the negative swing of the input voltage, the NMOS-diode M_6 becomes forward-biased and charge is transferred to the coupling capacitor C_5. During the positive half-cycle in the following the PMOS-diode M_7 is biased in forward direction and the stored charge is transferred to the capacitor C_7. The capacitors C_6 and C_7 decouple the RF signal at the DC input node V_{Lo} and the DC output node V_{Hi} of a charge pump stage, respectively. As shown in Fig. 3.1, the bulk terminal of transistor M_7 is connected to V_{Hi}. Complementary to this, the bulk of M_6 is connected to the input node. The input DC voltage $V_{\mathrm{DC,n-1}}$ of every stage except for the first stage $(\mathrm{n} > 1)$ is larger than 0 V during operations. Therefor, a triple well CMOS process has to be used that enables the implementation of an isolated p-well for the NMOS devices (see Fig.2.10).

The threshold voltage V_{th} of the rectifying transistors to a large extend determines the level of input voltage amplitude $\hat{V}_{\mathrm{in}}$ that is required to deliver a specific power P_{DC} at the output of the RF charge pump. Evidently, $\hat{V}_{\mathrm{in}}$ and the forward voltage drop at the rectifying transistors rise with an increasing V_{th}, resulting in an elevated quality factor Q (see Eqn. 3.1) and a lower power conversion efficiency η. Threshold voltage compensation techniques were introduced to improve the characteristics of RF charge pumps at low levels of RF input power by providing primarily a gate bias to the rectifying transistors [74, 76]. The bias voltage V_{N} (V_{P}) in Fig. 3.1 illustrates in a simplified manner the threshold compensation for the NMOS (PMOS) rectifying transistor M_6 (M_7).

Analytical Circuit Model

Understanding the fundamental trade-offs that are involved in applying a V_{th} compensation requires a close examination of the transient operating conditions of the rectifying

transistors. The analysis of an entire RF charge pump including N_{st} stages can be reduced to the analysis of a single rectifying transistor considering following assumptions (see [133, 135, 138]):

- The N_{st} stages of the RF charge pump are all equal and show the same behavior regardless of the DC input voltage level $V_{DC,n-1}$.
- The voltage drop with respect to the RF input voltage at the coupling capacitor C_5 (see Fig. 3.1) due to the charge that is transferred during a carrier period and the parasitic capacitance at node S_1 is negligible small.
- The voltage ripple at the decoupling capacitors C_6 and C_7, as shown in Fig. 3.1, is negligible small.
- The NMOS and the PMOS rectifying transistors of a charge pump unit stage show ideally balanced characteristics.

The listed assumptions are overall major preconditions to achieve a high performance with respect to the power conversion efficiency and the quality factor of an RF charge pump at low levels of input power. Therefore, a well implemented charge pump design will for the most part also comply with these assumptions. For example, performance variations between cascaded charge pump stages due to different bulk bias levels are typically canceled by using locally biased well structures, as shown in Fig. 3.1. The imbalances between the NMOS and PMOS rectifying transistors can be diminished by a proper sizing of the devices and a corresponding adaption of the gate bias levels (V_N and V_P in Fig. 3.1).

According to the second assumption, the voltage drop at the coupling capacitor C_5 in Fig. 3.1 can be neglected, and the RF voltage is coupled to the full extend to node S_1. This assumption is dependent on two conditions. First, the parasitic capacitance $C_{par,S1}$ at node S_1 with reference to GND is small in comparison to the coupling capacitance ($C_{par,S1}/C_5 \ll 1$). C_5 and $C_{par,S1}$ build a capacitive voltage divider diminishing the voltage amplitude at node S_1. Second, the value of C_5 is large in relation to the charge that is transferred to C_5 during a carrier period resulting in a negligible small change in the voltage at the capacitor ($I_{DC}/(C_5 f_0) \ll 1$). As indicated, the peak accumulated charge at C_5 during a carrier period can be approximately expressed by the DC output current of the charge pump I_{DC} and the carrier frequency f_0. With rising input voltage and thus rising input power, I_{DC} increases and eventually the voltage drop due to the accumulated charge cannot be neglected anymore. Therefore, the second assumption is only true for low levels of the input power P_{in}.

Figure 3.2 illustrates the simplified model of a single-ended RF charge pump that is considered for the following circuit analysis. The voltages at the gate (v_g) and source terminals (v_s) of the rectifying transistor M_6 are defined relative to the DC input voltage $V_{DC,n-1}$ of the stage number n. For a given value of the output voltage V_{DC}, the voltage gain of a single stage is determined by the number of cascaded stages N_{st}:

$$V_{DC,n} - V_{DC,n-1} = \frac{V_{DC}}{N_{st}}. \tag{3.2}$$

It has been assumed that the NMOS and the PMOS rectifying devices show a perfectly balanced characteristic. Thus, the DC offset voltage at node S_1 with respect to $V_{DC,n-1}$ equals $V_{DC}/(2N_{st})$. The voltage waveforms at the source and gate terminals of the NMOS rectifying transistor can therefore be expressed as follows (see Fig. 3.2):

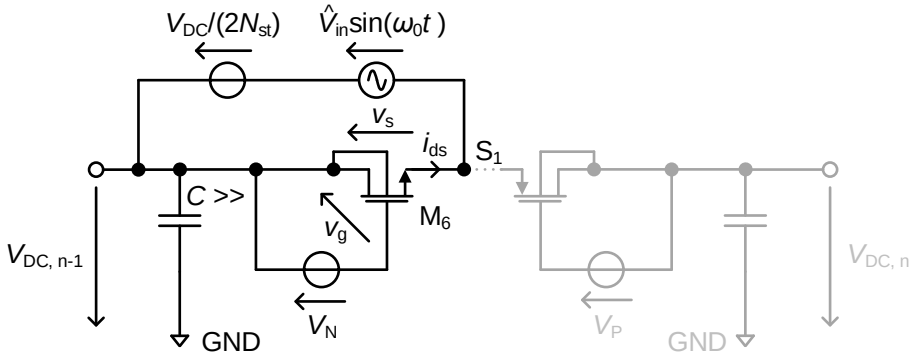


Figure 3.2: Circuit model for the analysis of a single-ended RF charge pump, as shown in Fig. 3.1. The influence of the coupling capacitor C_5 in Fig. 3.1 on the RF amplitude observed at node S_1 can be neglected at low levels of input power.

$$v_s(t) = V_{in}(t) + \frac{V_{DC}}{(2N_{st})} = \hat{V}_{in}\sin(\omega_0 t) + \frac{V_{DC}}{(2N_{st})}, \tag{3.3}$$

$$v_g(t) = V_N. \tag{3.4}$$

The drain-source current I_{ds} of MOS transistors operating in strong inversion can be expressed in an approximate manner by means of the terminal voltages as follows [139]:

$$I_{ds} = \begin{cases} \mu_n C_{ox}\frac{W}{L}\left((V_{gs}-V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right), & V_{ds} \le V_{gs}-V_{th}, \quad (3.5a) \\ \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2, & V_{ds} > V_{gs}-V_{th}. \quad (3.5b) \end{cases}$$

The parameter C_{ox} in Eqn. 3.5 represents the gate oxide capacitance per unit area and μ_n* equals the charge carrier mobility of electrons at the semiconductor surface. W and L correspond to the width and length of the transistor gate, respectively. Equation 3.5a describes the operation of MOS transistors in the linear region for drain-source voltages V_{ds} lower than the overdrive voltage that is defined by the applied gate-source voltage V_{gs} and the threshold voltage $(V_{ds} \le V_{gs} - V_{th})$. Complementary to this, Eqn. 3.5b models the transistor operation in the saturation region.

Unlike C_{ox} and μ_n, the threshold voltage V_{th} can be influenced purposefully in the circuit design to a certain extend. The V_{th} of transistors in modern CMOS technologies is typically strongly dependent on the transistor dimensions W and L [139]. Moreover, the threshold voltage can be shifted by varying the source-bulk voltage V_{sb} [139]:

$$V_{th} = V_{t0} + \gamma\left(\sqrt{\Phi_0 + V_{sb}} - \sqrt{\Phi_0}\right). \tag{3.6}$$

V_{t0} corresponds to the extrapolated threshold voltage for zero inversion layer charge. The parameter γ represents the body effect coefficient, and Φ_0 equals the potential at the

*Complementary to μ_n, the mobility of electrons, μ_p denotes the mobility of holes in this work.

semiconductor surface beneath the transistor gate in strong inversion. As shown by Eqn. 3.6, the threshold voltage can be reduced by applying a negative source-bulk bias V_{sb}.

Equation 3.5a and Eqn. 3.5b are only valid for a V_{gs} greater than V_{th}. Complementary, the subthreshold operation ($V_{\mathrm{gs}} < V_{\mathrm{th}}$) of MOS transistors can be described in a simplified manner by following expression [139]:

$$I_{\mathrm{ds}} = I_0 \frac{W}{L} \mathrm{e}^{(V_{\mathrm{gs}}-V_{\mathrm{th}})/(n_{\mathrm{sub}}\Phi_{\mathrm{t}})} \left(1 - \mathrm{e}^{-V_{\mathrm{ds}}/\Phi_{\mathrm{t}}}\right). \tag{3.7}$$

I_0 in Eqn. 3.7 corresponds to the drain-source current at the upper limit of the subthreshold region ($V_{\mathrm{gs}} \approx V_{\mathrm{th}}$). The coefficient n_{sub} defines the subthreshold slope, and Φ_{t} equals the thermal voltage that is determined by the absolute temperature T_{K}, the Boltzmann constant k, and the elementary charge q ($\Phi_{\mathrm{t}} = kT_{\mathrm{K}}/q$).

A rectifying transistor of an RF charge pump, as shown in Fig. 3.2, traverses various operating regions (Eqn. 3.5a, 3.5b, and 3.7) during a carrier period, complicating the circuit analysis (see [135, 138]). Moreover, the simplified expressions for the drain-source current in strong and weak inversion given by Eqn. 3.5 and Eqn. 3.7 typically show a low accuracy in the moderate inversion region at values of V_{gs} close to V_{th}. Therefore, I chose in this thesis for the analysis of RF charge pump circuits a single unified expression for the drain-source current of MOS transistors that is valid in all regions [139, 140]:

$$\begin{aligned} I_{\mathrm{ds}} = & \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} 2 n_{\mathrm{sub}} \Phi_{\mathrm{t}}^2 \left(\left(\ln\left(1 + \mathrm{e}^{(V_{\mathrm{gs}}-V_{\mathrm{th}})/(2n_{\mathrm{sub}}\Phi_{\mathrm{t}})}\right)\right)^2 \right. \\ & \left. - \left(\ln\left(1 + \mathrm{e}^{(V_{\mathrm{gs}}-V_{\mathrm{th}}-n_{\mathrm{sub}}V_{\mathrm{ds}})/(2n_{\mathrm{sub}}\Phi_{\mathrm{t}})}\right)\right)^2 \right). \end{aligned} \tag{3.8}$$

Equation 3.8 uses an interpolation function combining Eqn. 3.5a, 3.5b, and 3.7. Indeed, for corresponding high or low values of V_{gs}, Eqn. 3.8 approaches again Eqn. 3.5 and Eqn. 3.7, respectively.

As shown in Fig. 3.2, the transient gate-source voltage $v_{\mathrm{gs}}(t)$ and the drain-source voltage $v_{\mathrm{ds}}(t)$ to compute the associated drain-source current $i_{\mathrm{ds}}(t)$ of the NMOS rectifying transistor can be derived from $v_{\mathrm{g}}(t)$ and $v_{\mathrm{s}}(t)$, as given by Eqn. 3.4 and Eqn. 3.3, respectively. Thus, for the drain-source voltage $v_{\mathrm{ds}}(t) = -v_{\mathrm{s}}(t)$ applies. If $v_{\mathrm{ds}}(t)$ changes its polarity, the source as a reference terminal of the transistor and the drain are swapped logically. In consequence, $v_{\mathrm{gs}}(t)$ has to be described by means of two separate operating regions (A and B) that are defined by the sign of $v_{\mathrm{ds}}(t)$ or analogously $v_{\mathrm{s}}(t)$:

$$v_{\mathrm{gs}}(t) = \begin{cases} v_{\mathrm{g}}(t) - v_{\mathrm{s}}(t) = V_{\mathrm{N}} - \dfrac{V_{\mathrm{DC}}}{(2N_{\mathrm{st}})} - \hat{V}_{\mathrm{in}} \sin(\omega_0 t), & \text{Region A: } v_{\mathrm{s}}(t) \leq 0, \\ v_{\mathrm{g}}(t) = V_{\mathrm{N}}, & \text{Region B: } v_{\mathrm{s}}(t) > 0. \end{cases} \tag{3.9}$$

Figure 3.3 shows the transient waveform of the drain-source current $i_{\mathrm{ds}}(t)$ of the NMOS rectifying transistor of a single-ended charge pump stage versus two carrier periods, resulting from the analytical model (see Fig. 3.2). The operating point of the RF charge pump corresponds to a DC output current I_{DC} of 4 μW at an output voltage V_{DC} of 1 V, assuming

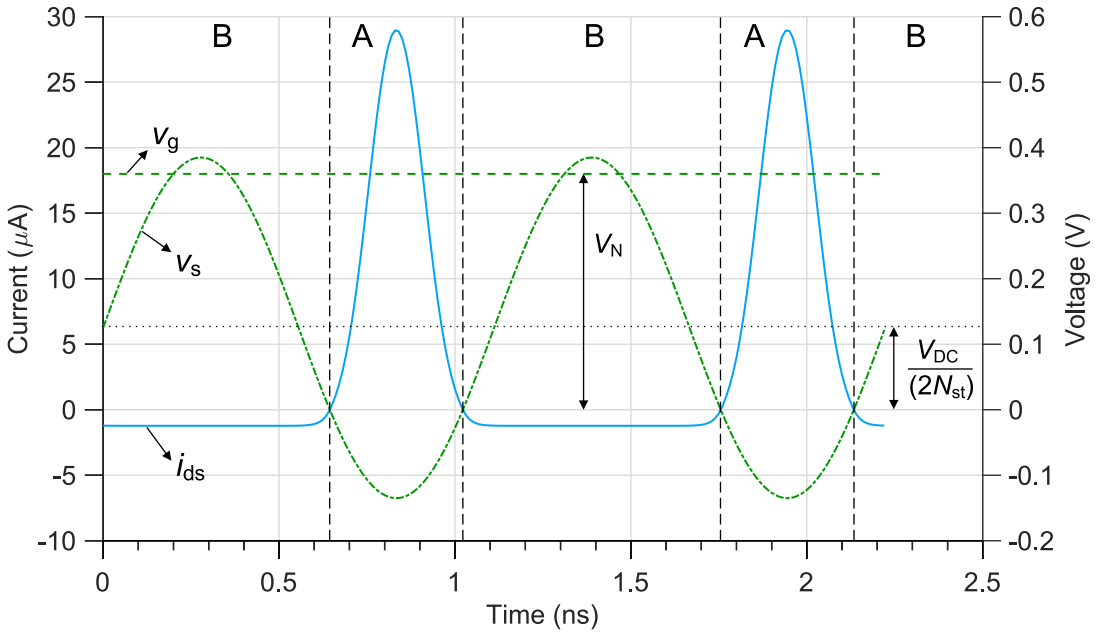


Figure 3.3: Transient waveforms of the drain-source current $i_{ds}(t)$, and the terminal voltages $(v_g(t), v_s(t))$ of the NMOS rectifying transistor of a single-ended charge pump stage, as shown in Fig. 3.1. The letters A and B indicate the different operating regions of the transistor according to the polarity of $v_s(t)$.

overall four cascaded charge pump stages. The transistor dimensions and the gate bias voltage V_N have been aligned with a design of a simplified charge pump circuit that uses ideal gate biasing sources, as depicted in Fig. 3.1. This simplified circuit has been designed in the considered 40 nm CMOS technology, and has been optimized in simulation with respect to the specifications summarized in Table 3.1. In more specific terms, the power conversion efficiency η of the charge pump has been maximized for the given DC output load, considering an additional parasitic capacitance C_{par} and the constraints on the quality factor Q, as stated in Table 3.1. The design optimization incorporated the transistor dimensions, the gate bias levels (V_N and V_P), the number of cascaded charge pump stages N_{st}, and the dimensions of the coupling capacitor. For the simulation of the coupling capacitor C_5 in Fig. 3.1, a dedicated RF capacitor model was used that takes into account the parasitic capacitance to ground (see [141]).

In region A, $v_s(t)$ becomes negative, and the NMOS-diode M_6 (see Fig. 3.1) becomes forward-biased, as shown in Fig. 3.3. $i_{ds}(t)$ rises sharply in consequence, and charge is transferred to the coupling capacitor C_5. The forward voltage drop at the diode causes a power loss during this period. In region B, $v_s(t)$ is negative, and the NMOS diode becomes reverse biased. The subthreshold leakage causes a current in the reverse direction, and an additional loss component, therefore. The behavior of the PMOS rectifying device is complementary to the NMOS diode.

By increasing the ratio of W/L of the rectifying transistors or the gate bias levels, the power loss due to the forward voltage drop can be reduced. Nevertheless, at the same time enhancing the bias or the W/L-ratio augments the power loss associated with the reverse leakage. Alternatively, the DC voltage gain per stage may be increased in relation to the forward voltage drop to enhance η. This can be achieved by reducing the number of

cascaded charge pump stages N_{st} at a given level of V_{DC}. Providing the same output current at a fixed V_{DC} using a lower number of stages requires a higher input voltage amplitude $\hat{V}_{in}$. According to Eqn. 3.1, an increase of $\hat{V}_{in}$ however causes a progressive rise of the input quality factor Q. The gate bias levels, the transistor dimensions, and the number of cascaded unit stages therefore have to be designed carefully to maximize the power conversion efficiency, considering the given specifications for Q.

Approximations for the major performance figures of an entire N_{st}-stage charge pump can be derived from the transient current and voltage waveforms of a single rectifying device, as shown in Fig. 3.3. The DC current I_{DC} that is delivered at the output of the charge pump corresponds to the time average of $i_{ds}(t)$ over one carrier period T_0 [138]:

$$I_{DC} = \frac{1}{T_0} \int_{T_0} i_{ds}(t) dt. \tag{3.10}$$

The overall power dissipation P_d at the rectifying transistors of an N_{st}-stage charge pump can be calculated from the instantaneously dissipated power of a single transistor (see [133, 138]):

$$P_d = \frac{2N_{st}}{T_0} \int_{T_0} -v_s(t) i_{ds}(t) dt. \tag{3.11}$$

Equation 3.11 implicitly follows the assumption that the NMOS and PMOS rectifying transistors as shown in Fig. 3.1 are perfectly balanced. The power dissipation at the two rectifying devices within a stage is thus equal. As noted previously, this assumption applies in a first approximation for a properly designed charge pump circuit. Equation 3.11 does not account for the losses due to the wiring resistances, and the losses associated with the parasitic coupling to the substrate.

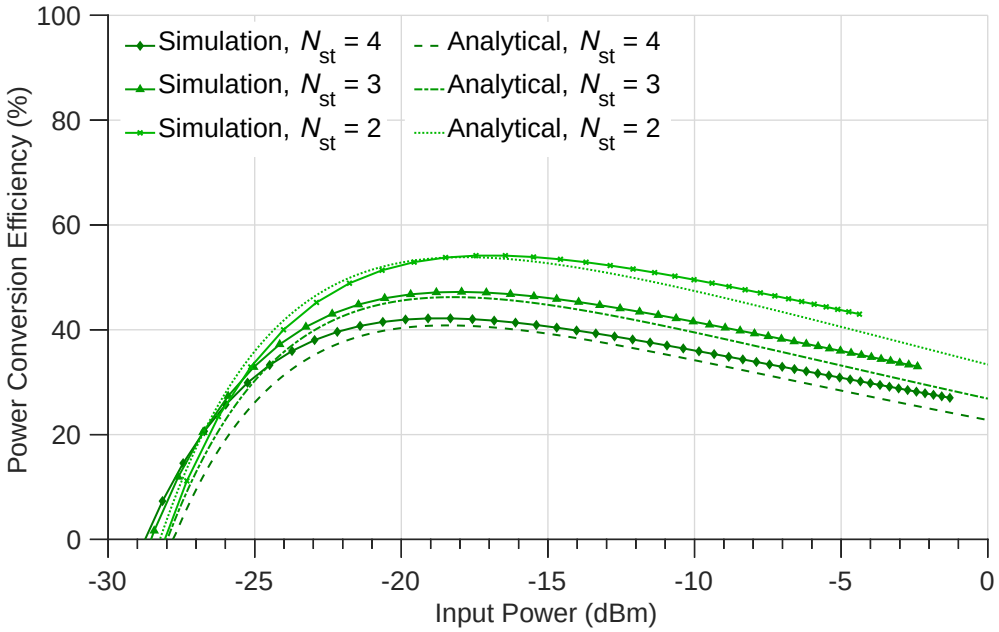
The DC output power is given by $P_{DC}{=}V_{DC} I_{DC}$. Therefore, the overall input power of an RF charge pump comprising N_{st} stages can be estimated when neglecting additional losses:

$$P_{in} = P_{DC} + P_d. \tag{3.12}$$

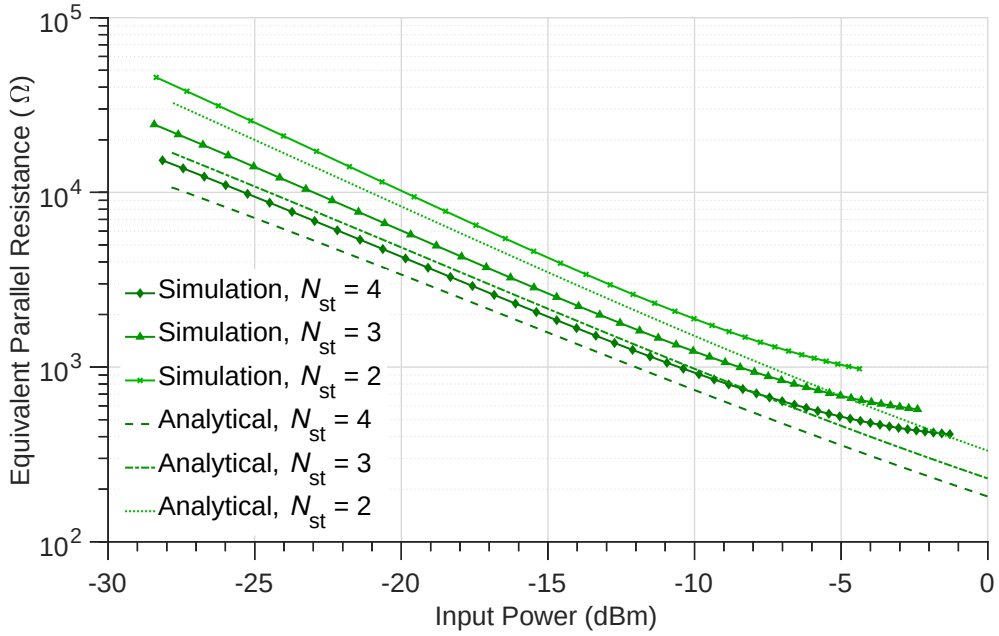
P_{in} and P_{DC} define the power conversion efficiency $\eta{=}P_{DC}/P_{in}$. Furthermore, a first estimation for the input quality factor Q can be deduced considering that Q is proportional to the equivalent parallel input resistance R_P (see Eqn. 3.1). R_P can be expressed by means of the input voltage amplitude $\hat{V}_{in}$ and the input power P_{in}, according to Eqn. 1.4. Eqn. 1.4 is rewritten below using the quantities as regarded in the context of UHF RFID front-ends in this work:

$$R_P = \frac{\hat{V}_{in}^2}{2P_{in}}. \tag{3.13}$$

Figure 3.4 shows characteristics of the power conversion efficiency η and the equivalent parallel input resistance R_P versus a varying input power P_{in} of single-ended RF charge pumps with a varying number of stages N_{st}. Calculation results of the proposed analytical model and simulation results of a simplified charge pump circuit that has been designed in the considered 40 nm CMOS technology are represented. As noted previously, this simplified



(a) η versus P_{in}.



(b) R_{P} versus P_{in}.

Figure 3.4: Characteristics of the power conversion efficiency η (a) and the equivalent parallel input resistance R_{P} (b) versus the input power P_{in} of three single-ended RF charge pumps with a varying number of stages N_{st} at $V_{\mathrm{DC}} = 1\,\mathrm{V}$ and $f_0 = 900\,\mathrm{MHz}$. Calculation results of the proposed analytical model and simulation results of a simplified single-ended charge pump circuit (see Fig. 3.1) are represented.

charge pump circuit includes ideal gate biasing sources as shown in Fig. 3.1, and has been specifically optimized with respect to the specifications listed in Table 3.1.

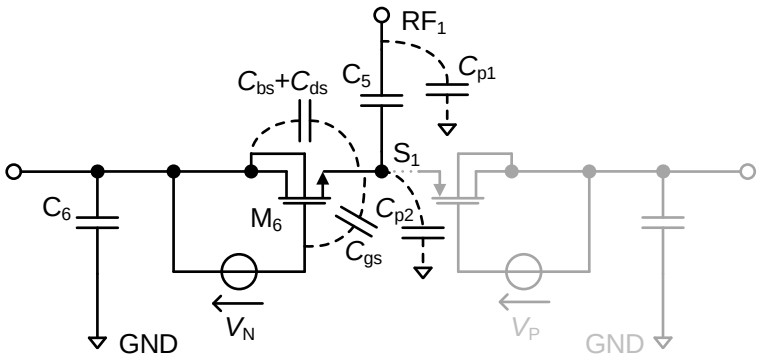


Figure 3.5: Parasitic capacitances of the rectifying transistors and the coupling capacitor of a single-ended RF charge pump stage. Only the parasitic capacitances of the NMOS transistor M_6 are shown for simplification.

The characteristics in Fig. 3.4a indicate a considerable enhancement of the power conversion efficiency that can be achieved by reducing the number of cascaded charge pump stages N_{st}. Decreasing N_{st} nevertheless causes a rise of the equivalent parallel input resistance R_P, as shown in Fig. 3.4b. An increase of R_P causes a proportional rise of the quality factor Q, assuming a fixed input capacitance C_P (see Eqn. 3.1).

The results of the circuit simulations and the analytical model depicted in Fig. 3.4 in general show an agreement with respect to both η and R_P. Nevertheless, the simulated charge pump circuit shows a slightly higher power conversion efficiency than predicted by the analytical model. The analysis of the charge pump circuit is based on a very simplistic transistor model neglecting fundamental effects like the modulation of the threshold voltage by the source-bulk bias V_{sb}, for example (see Eqn. 3.6). The bulks of the rectifying transistors are connected to the DC input and output nodes of a charge pump stage (see Fig. 3.1). In consequence, the RF voltage that is coupled to node S_1 directly modulates the V_{th} of the rectifying transistors, which effectively reduces the forward voltage drop and enhances the power conversion efficiency.

With respect to the input resistance R_P, the analytical model predicts a slightly lower value in comparison to the simulation results, which can be seen in Fig. 3.4b. The analytical model neglects the voltage drop at the coupling capacitor concerning the RF input voltage $V_{in}(t)$, as noted previously. The parasitic capacitance at node S_1 and the coupling capacitor C_5 (see Fig. 3.1) build a capacitive voltage divider that effectively increases the input voltage amplitude $\hat{V}_{in}$ for a given DC operating point. A higher $\hat{V}_{in}$ causes a corresponding increase of the input resistance R_P, as suggested by Eqn. 3.13. At an approximate input power of more than -7 dBm, the simulated characteristics of R_P flatten. The voltage deviation at the coupling capacitor due to the charge that is transferred during a carrier period becomes non-negligible at this level of input power. Indeed, R_P approaches the characteristic of a switched-capacitor circuit in fully settled operation, exhibiting a constant input resistance independent of the input voltage level (see [142]). The input resistance of the RF charge pump at high input powers is thus primarily determined by the carrier frequency, the value of the coupling capacitance, and the number of cascaded charge pump stages:

$$R_P \sim \frac{1}{f_0 N_{st} C_5}. \tag{3.14}$$

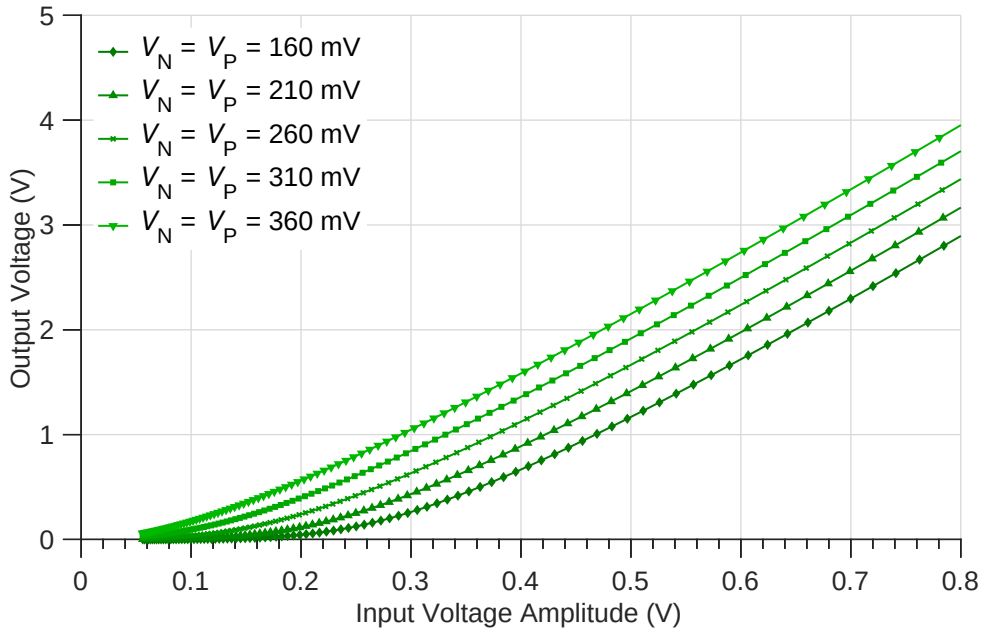


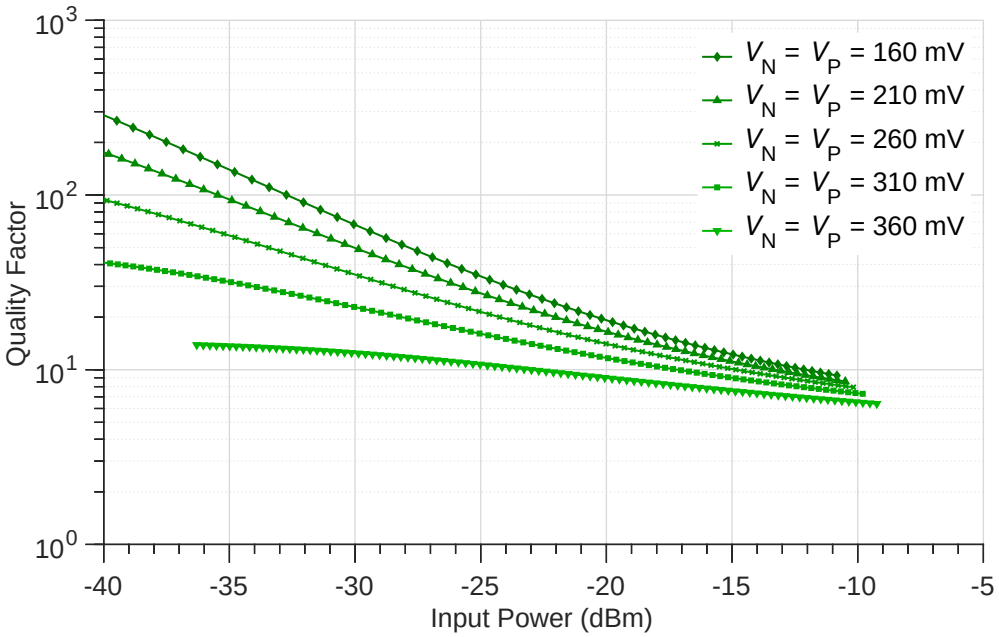
Figure 3.6: Simulation results of the DC output voltage V_{DC} versus the RF input voltage amplitude $\hat{V}_{in}$ for varying values of the gate bias voltages V_N and V_P at $f_0 = 900\,\text{MHz}$ and $R_L = 250\,\text{k}\Omega$. The simulated circuit corresponds to a single-ended four-stage charge pump including ideal bias sources (see Fig. 3.1).

Simulation Study

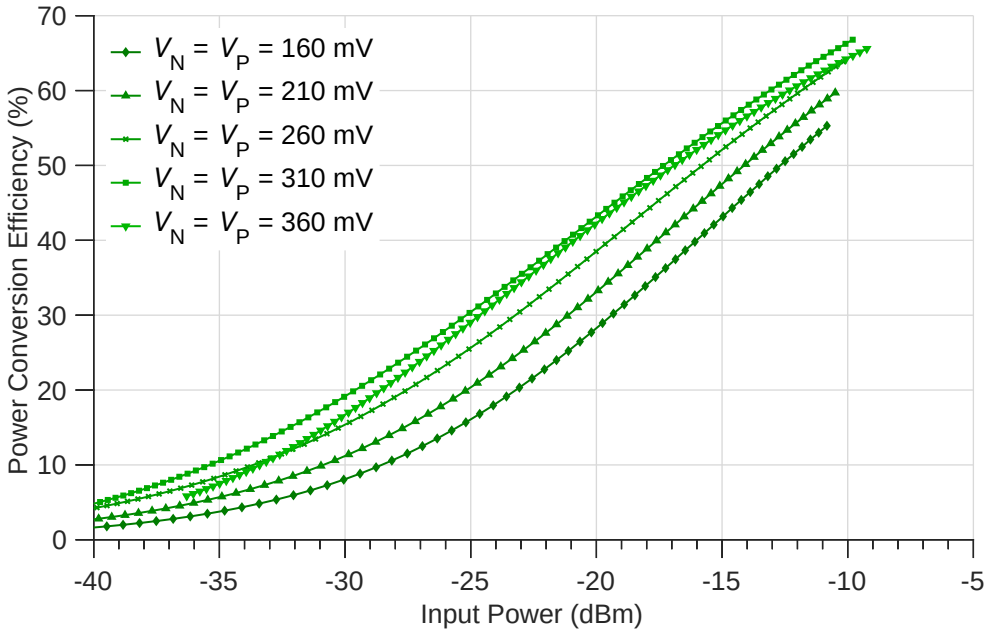
The analytical model that has been considered so far does not account for the influence of the parasitic capacitances of the devices on the circuit characteristics of an RF charge pump. An exact description of the input capacitance is required to allow an accurate circuit implementation according to specifications in particular regarding the input quality factor.

Figure 3.5 illustrates the parasitic capacitances that are associated with the rectifying transistors and the coupling capacitor of a single-ended charge pump stage. Only the parasitic capacitances of the NMOS transistor M_6 are shown. The parasitic capacitances of the PMOS device have apparently a similar impact with respect to the circuit characteristics. The gate-source capacitance C_{gs} is typically the dominant contribution with respect to the parasitic capacitances of the transistors. The effective value of C_{gs} is dependent on the gate-oxide capacitance C_{ox}, and the terminal voltages at the transistor [139]. The source-bulk capacitance C_{bs} comprises predominantly the intrinsic channel-bulk capacitance of the MOS structure, and the p-n junction capacitance of the source contact region, which are both strongly bias dependent. The drain-source capacitance C_{ds}, on the other hand, is defined by wiring capacitances. The decoupling capacitor C_6 effectively poses a short circuit for the RF signal. Thus, C_{gs}, C_{ds}, and C_{bs} directly add to the parallel input capacitance of the RF charge pump C_P.

Moreover, the parasitic capacitances of the coupling capacitor to the substrate (C_{p1} and C_{p2}) contribute to C_P, as shown in Fig. 3.5. The coupling capacitors of the RF charge pumps presented in this work are implemented by metal fringe capacitors. These devices consist of a stack of inter-digital metal fingers, using the available routing metals in a given CMOS technology. Therefore, fringe capacitors can be fabricated without additional costs [141].



(a) Q versus P_{in}.



(b) η versus P_{in}.

Figure 3.7: Simulation results of the quality factor Q (a) and the power conversion efficiency η (b) versus the input power P_{in} for varying values of the gate bias voltages V_N and V_P at $f_0 = 900\,\text{MHz}$ and $R_L = 250\,\text{k}\Omega$. The simulated circuit corresponds to a single-ended four-stage charge pump including ideal bias sources (see Fig. 3.1).

Utilizing the lateral coupling between metal wires allows the realization of a high capacitance per unit area, and a low parasitic capacitance to the substrate in relation [132].

The parasitic capacitances of the rectifying transistors and the coupling capacitor scale with the dimensions of the devices, requiring a careful trade-off in the design process with

respect to the opposing specifications for η and Q. As described previously, I investigated in a first step of the design process the influence of different design parameters on the characteristics of a simplified charge pump circuit that corresponds to the schematic shown in Fig. 3.1. The design of the threshold voltage compensation, or more specifically the level of the gate biases V_{N} and V_{P}, has evolved as a key factor for achieving a low Q and a high η at the targeted low $P_{\mathrm{DC,min}}$.

Figure 3.6 shows simulated characteristics of the DC output voltage V_{DC} versus the RF input voltage amplitude $\hat{V}_{\mathrm{in}}$ of the optimized single-ended charge pump using ideal gate bias sources (see Fig. 3.1). A load resistance R_{L} of 250 kΩ was connected at the output of the charge pump for the simulations, corresponding to a $P_{\mathrm{DC,min}}$ of 4 μW at an output voltage V_{DC} of 1 V (see Table 3.1). The characteristics for different levels of the gate bias voltages V_{N} and V_{P} are depicted. The value of 360 mV equals the optimized bias voltage level that has been determined in circuit simulations. Increasing the gate bias level effectively reduces the threshold voltage of the rectifying transistors, and thus the forward voltage drop diminishes. In consequence, the characteristic of V_{DC} is shifted towards lower values of $\hat{V}_{\mathrm{in}}$. The input voltage amplitude that is required to achieve a specific value of DC output voltage decreases. Considering Eqn. 3.1, the reduction of $\hat{V}_{\mathrm{in}}$ at a given output load P_{DC} is equal to a decrease of the input quality factor Q of the RF charge pump.

As shown in Fig. 3.7a, the characteristic of the quality factor Q flattens with increasing gate bias voltages V_{N} and V_{P}, resulting in significantly lower values for Q at low levels of input power P_{in} of around -20 dBm or less. At the same time, the power conversion efficiency η rises starting from a low bias level of 160 mV, as shown in Fig. 3.7b. It can be seen however that at an elevated bias voltage of 360 mV the power conversion efficiency decreases again slightly. The reverse leakage losses of the rectifying transistors become larger, as V_{N} and V_{P} are incremented. The increased leakage current eventually compensates the efficiency gain due to the reduced froward voltage drop at some point (see Fig. 3.3). The bias levels for the V_{th} compensation of the rectifying transistors have to be carefully optimized considering the targeted values of $P_{\mathrm{DC,min}}$ and Q to maximize the power conversion efficiency η, and thus to achieve a low value for the sensitivity P_{min}.

3.2.2 Differential RF Charge Pumps

The gate terminals of the rectifying transistors of a differential RF charge pump are actively driven by the RF input signal, in contrast to single-ended implementations. Therefore, differential RF charge pumps typically achieve a higher power conversion efficiency than comparable single-ended circuits, which will be discussed in more detail in Sect. 3.2.3.

The majority of differential RF charge pumps, which have been discussed in literature so far are based on the cross-coupled circuit topology that is shown in Fig. 3.8 (e.g., [41, 73, 75]). The depicted circuit corresponds to a single charge pump unit stage. The index n denotes the stage number considering a charge pump with N_{st} stages in total $1 \leq n \leq N_{\mathrm{st}}$. Each stage contains two parallel branches, comprising in total two NMOS and two PMOS transistors. Neglecting the gate bias voltages V_{N} in a first step, the NMOS rectifying transistors M_6 and M_8 are connected as a cross-coupled pair. The gate of M_6 is connected to the source of M_8 and vice versa. The same is valid for the two PMOS rectifying transistors M_7 and M_9.

In case of a perfectly balanced front-end circuit, the RF input signals at the input terminals RF_1 and RF_2 exhibit exactly an equal amplitude and a phase shift of 180 °. The

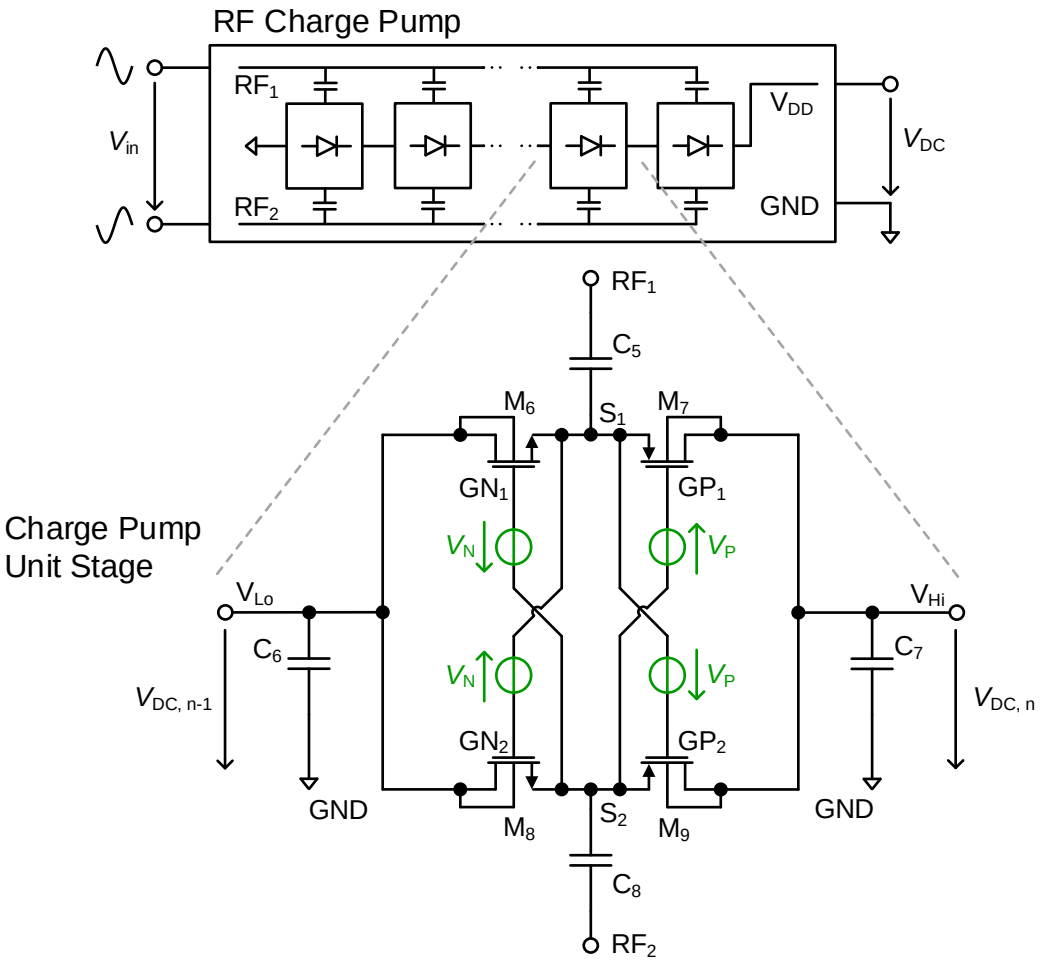


Figure 3.8: Simplified schematic of a differential RF charge pump. The biasing voltages V_N and V_P highlighted in green compensate the V_{th} of the NMOS rectifying transistors M6, M8, and the PMOS transistors M7, M9, respectively [75, 83].

capacitors C_5 and C_8 couple the RF signal to the source nodes of the NMOS and the PMOS cross-coupled pair at the nodes S_1 and S_2. As the input voltage swing at RF_1 becomes negative, the gate voltage of transistor M_6 rises. As a results of this, M_6 becomes conductive and charge is transferred to the coupling capacitor C_5. During the following positive half-wave, the PMOS transistor M_7 becomes conductive, and the stored charge is transferred to the output node V_{hi}. The capacitors C_6 and C_7 decouple the RF signal at the DC input node V_{Lo} and the DC output node V_{Hi} of a charge pump stage, respectively. In the same manner as in case of the single-ended charge pumps discussed in Sect. 3.2.1, the bulk terminals of the NMOS and PMOS rectifying transistors of the cross-coupled charge pump stage shown in Fig. 3.8 are connected to nodes V_{Lo} and V_{Hi}, requiring the usage of a triple-well CMOS process.

The NMOS and PMOS cross-coupled pairs inherently provide a minor gate bias for the rectifying transistors [73]. In addition, the bias voltages V_N and V_P have been introduced to compensate the threshold voltage of the rectifying transistors and thus to improve the circuit performance at low levels of input power [75, 83].

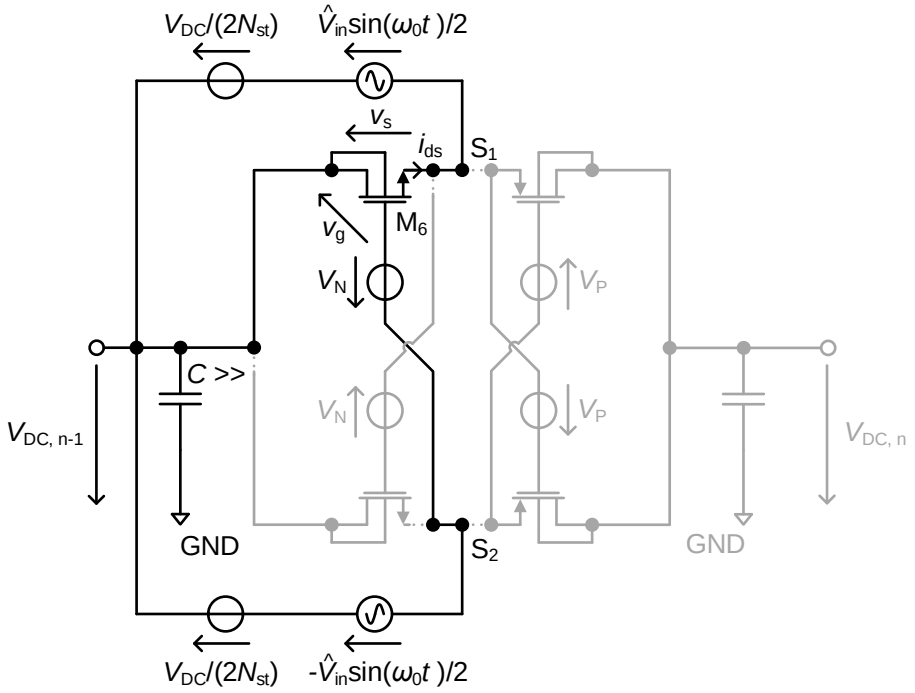


Figure 3.9: Circuit model for the analysis of a differential RF charge pump, as shown in Fig. 3.8. The influence of the coupling capacitors C_5 and C_8 (see Fig. 3.8) on the RF amplitude observed at the nodes S_1 and S_2, respectively, can be neglected at low levels of RF input power.

Analytical Circuit Model

Figure 3.9 illustrates a simplified circuit model for the analysis of a differential RF charge pump, as shown in Fig. 3.8. The model follows the same simplifications and assumptions, as described in Sect. 3.2.1 for the analysis of single-ended RF charge pumps. As illustrated in Fig. 3.9, the circuit analysis is confined to a single NMOS transistor (M_6) implicitly assuming that the associated PMOS rectifying transistor (M_7) and the second circuit branch show perfectly balanced characteristics. Furthermore, the effect of the coupling capacitors C_5 and C_8 on the signal amplitude that is observed at the nodes S_1 and S_2 is neglected. The transient voltage waveforms at the source and gate terminal of M_6, $v_s(t)$ and $v_g(t)$, respectively, can thus be expressed as follows:

$$v_s(t) = \frac{V_{in}(t)}{2} + \frac{V_{DC}}{(2N_{st})} = \frac{\hat{V}_{in}}{2}\sin(\omega_0 t) + \frac{V_{DC}}{(2N_{st})}, \tag{3.15}$$

$$v_g(t) = -\frac{V_{in}(t)}{2} + \frac{V_{DC}}{(2N_{st})} + V_N = -\frac{\hat{V}_{in}}{2}\sin(\omega_0 t) + \frac{V_{DC}}{(2N_{st})} + V_N. \tag{3.16}$$

The drain-source voltage of the NMOS transistor M_6 can be expressed as $v_{ds}(t) = -v_s(t)$ (see Fig. 3.9). Therefore, the instantaneous drain-source current $i_{ds}(t)$ of M_6 can be calculated by means of Eqn. 3.8, considering following expression for the gate-source voltage:

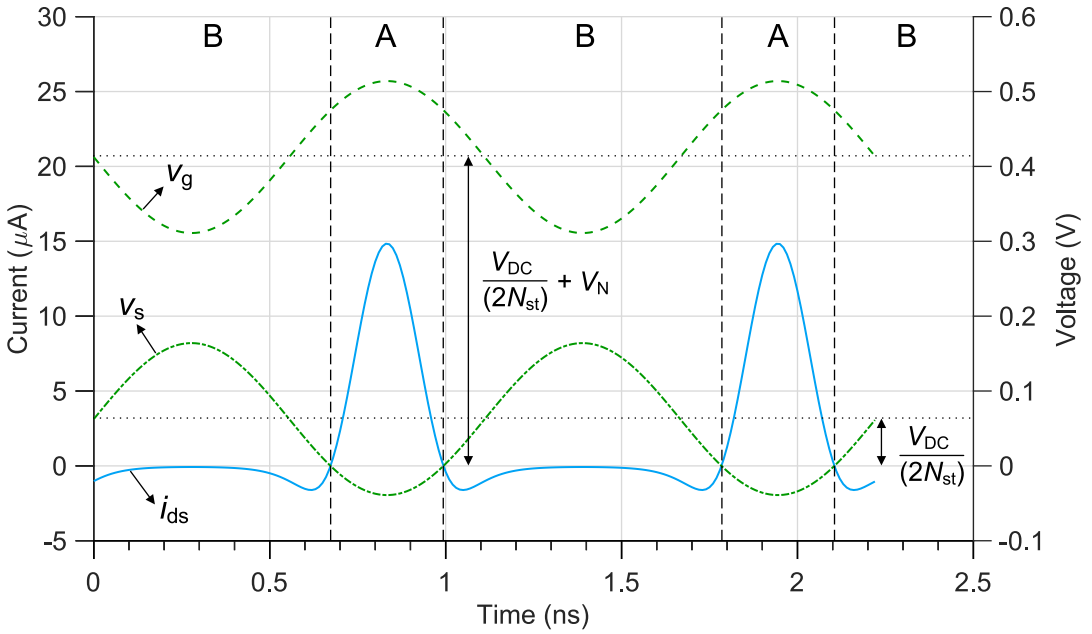


Figure 3.10: Transient waveforms of the drain-source current $i_{ds}(t)$, and the terminal voltages $v_g(t)$, $v_s(t)$ of the NMOS rectifying transistor M_6 of a cross-coupled charge pump stage, as shown in Fig. 3.8. The letters A and B indicate the different operating regions of the transistor according to the polarity of $v_s(t)$.

$$v_{gs}(t) = \begin{cases} v_g(t) - v_s(t) = V_N - \dfrac{\hat{V}_{in}}{2}\sin(\omega_0 t), & \text{Region A: } v_s(t) \leq 0, \\ v_g(t) = V_N + \dfrac{V_{DC}}{(2N_{st})} - \dfrac{\hat{V}_{in}}{2}\sin(\omega_0 t), & \text{Region B: } v_s(t) > 0. \end{cases} \tag{3.17}$$

Equation 3.17 accounts for the two operating regions (region A and B) of transistor M_6 that are defined by the sign of $v_s(t)$. As $v_s(t)$ becomes positive, the gate and source terminals of M_6 are swapped logically, and thus $v_{gs}(t)$ has to be redefined to correctly describe the transient behavior of the circuit.

Figure 3.10 shows the transient waveforms of the drain-source current $i_{ds}(t)$ and the terminals voltages $v_g(t)$ and $v_s(t)$ of the rectifying transistor M_6. The current and voltage waveforms have been calculated using the analytical model illustrated in Fig. 3.9. The shown waveforms correspond to a DC output current I_{DC} of 4 μW at an output voltage V_{DC} of 1 V considering a charge pump with eight cascaded unit stages ($N_{st} = 8$). As in case of the previous discussion of single-ended RF charge pumps in Sect. 3.2.1, the transistor dimensions W, L, and the number of charge pump stages N_{st} of the analytical circuit model have been aligned with a design of a simplified RF charge pump that includes ideal biasing sources, as shown in Fig. 3.8. The simplified cross-coupled charge pump design has been optimized in simulation with respect to the specifications listed in Table 3.1 essentially following the same procedure, as described in Sect. 3.2.1.

As can be seen in Fig. 3.10, $v_g(t)$ rises in region A, while $v_s(t)$ becomes negative. The NMOS rectifying transistor gets conductive due to the positive gate-source voltage and current is flowing to the coupling capacitor C_5 (see Fig. 3.8). The associated power dissipation

at the transistor is defined by the drain-source voltage drop in relation to the forward current.* In the transition regions before and after the zero-crossing of $v_s(t)$, current peaks in the reverse direction can be seen that pose an additional power loss. The transistor is still biased in a rather conductive state during these short periods, while $v_s(t) > 0\,\mathrm{V}$ causing the reverse current peaks. The reverse current in region B gets modulated by the input voltage, reaching its minimum at the positive peak of $v_s(t)$ that corresponds to the minimum $v_{gs}(t)$ at the NMOS rectifying transistor.

Analogously to Eqn. 3.10 and Eqn. 3.11, the DC output current I_{DC} and the overall power dissipation P_d of a cross-coupled charge pump can be estimated, considering the two parallel charge pump branches of each stage and the associated number of rectifying transistors (see [138]):

$$I_{DC} = \frac{2}{T_0} \int_{T_0} i_{ds}(t)dt, \tag{3.18}$$

$$P_d = \frac{4N_{st}}{T_0} \int_{T_0} -v_s(t) i_{ds}(t)dt. \tag{3.19}$$

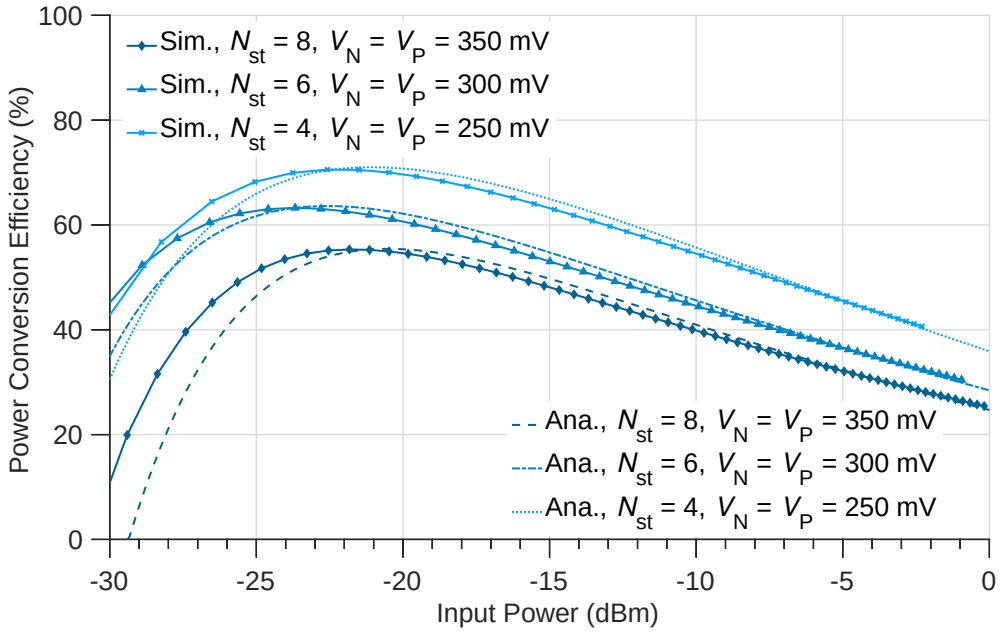
The input power P_{in} and the equivalent parallel input resistance R_P of a cross-coupled charge pump can be derived furthermore by Eqn. 3.12 and Eqn. 3.13, respectively, in the same way as in case of a single-ended charge pump.

Figure 3.11 shows characteristics for η and R_P versus the input power P_{in} of three cross-coupled charge pumps with a varying number of stages N_{st} and different gate bias levels V_N and V_P. The characteristics have been calculated by applying the analytical model illustrated in Fig. 3.9. For comparison, Fig. 3.11 includes simulation results of simplified charge pump circuits that utilize ideal bias sources (see Fig. 3.8). The input parameters for the analytical model have been aligned to the associated charge pump circuit in each case. The eight-stage charge pump with bias levels V_N and V_P equal to 350 mV corresponds to the circuit that has been optimized with respect to the specifications summarized in Table 3.1.

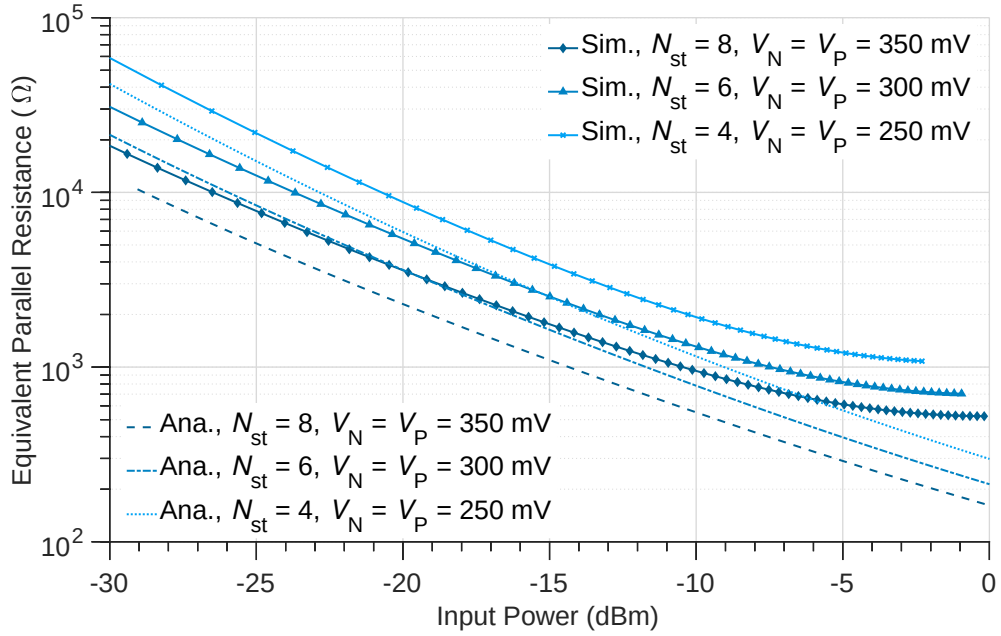
As shown in Fig. 3.11a, the power conversion efficiency η could be improved considerably by reducing the number of stages N_{st}, and simultaneously lowering the bias voltages V_N and V_P. A reduction of the number of stages increases the DC voltage gain per stage, and effectively diminishes the relative losses due to the forward voltage drop at the rectifying transistors with respect to a fixed output voltage V_{DC}. Lowering the gate bias level in addition results in a steeper voltage transition around the zero-crossing of $v_s(t)$, and thus diminishes the distinctive reverse current peaks (see Fig. 3.10). Nevertheless, reducing N_{st}, and lowering V_N and V_P at a fixed DC operating point (defined by V_{DC} and I_{DC}) inevitably induces an increase of the input voltage amplitude $\hat{V}_{in}$. As shown in Fig. 3.11b, the equivalent parallel input resistance R_P rises in consequence, which corresponds to a proportional increase of Q according to Eqn. 3.1 and assuming a constant value of C_P. The design of differential RF charge pumps comprises therefore a trade-off regarding η and Q, in a similar way as noted in Sect. 3.2.1 in the context of single-ended charge pumps.

The results of the analytical model and the simulation results in Fig. 3.11 show a good agreement. The simulation results exhibit nevertheless a higher η than the analytical model

*By analogy to the diode connected MOS transistor of a single-ended charge pump, the forward current denotes the current flow in direction of the output node V_{Hi} of a cross-coupled charge pump stage (see Fig.3.8).



(a) η versus P_{in}.



(b) R_{P} versus P_{in}.

Figure 3.11: Characteristics of the power conversion efficiency η (a) and the equivalent parallel input resistance R_{P} (b) versus the input power P_{in} of three differential RF charge pumps with a varying number of stages N_{st} and different gate bias levels V_{N}, V_{P} at $V_{\text{DC}} = 1\,\text{V}$ and $f_0 = 900\,\text{MHz}$. Shown are calculation results of the proposed analytical (Ana.) model and simulation (Sim.) results of a simplified cross-coupled charge pump circuit (see Fig. 3.8).

at low levels of input power P_{in}. Moreover, the input resistance predicted by the analytical model is notably lower in comparison to the simulation results. The simulated characteris-

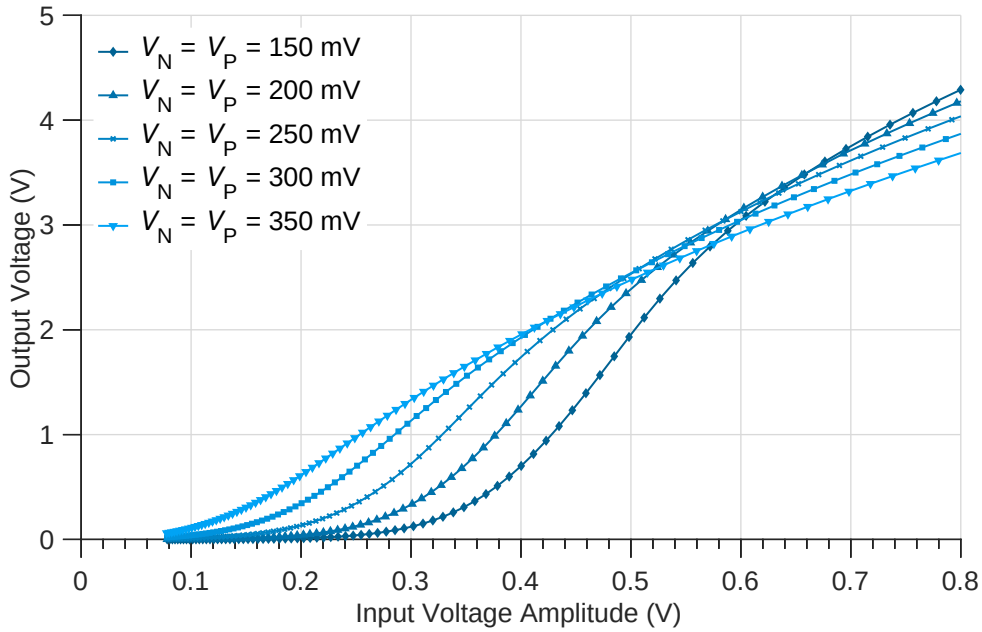


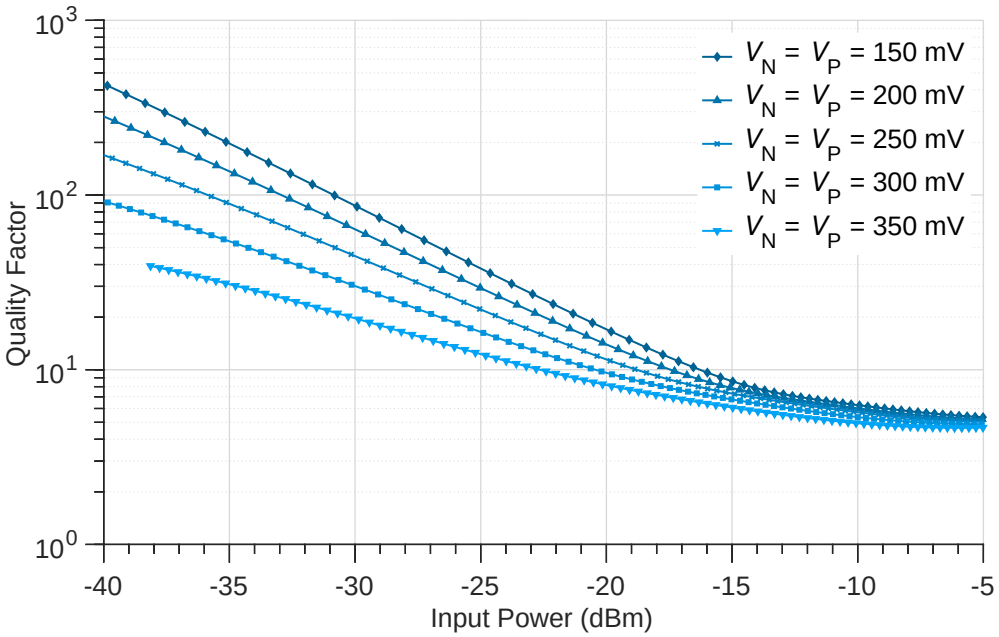
Figure 3.12: Simulation results of the DC output voltage V_{DC} versus the RF input voltage amplitude $\hat{V}_{in}$ for varying values of the gate bias voltages V_N and V_P at $f_0 = 900\,\text{MHz}$ and $R_L = 250\,\text{k}\Omega$. The simulated circuit corresponds to a differential eight-stage charge pump including ideal bias sources (see Fig. 3.8).

tics of R_P flatten in contrast to the results of the analytical model at higher values of P_{in}. The causes of these deviations are essentially the same as discussed in Sect. 3.2.1 regarding the analytical model for single-ended charge pumps. Accordingly, the deviations between analytical model and circuit simulations can be ascribed for the most part to the limitations of the considered transistor model and the applied simplifications.

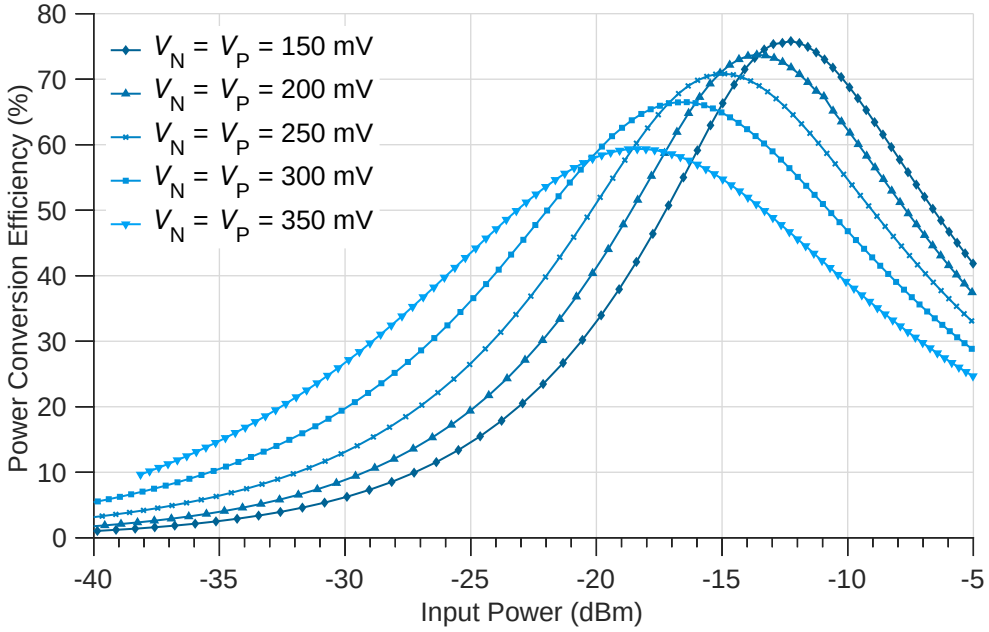
Simulation Study

The proposed analytical model does not describe the influence of the parasitic capacitances of the devices and therefore does not allow a prediction of the input capacitance C_P as well as the quality factor Q of a differential RF charge pump. The relevant parasitic capacitances that are associated with the rectifying transistors and the coupling capacitors are essentially the same as in case of a single-charge pump (see Fig. 3.5). The gate terminals of the rectifying transistors of a cross-coupled charge pump are directly coupled to the RF input signal. Therefore, the gate-bulk capacitance C_{gb} and the gate-drain capacitance C_{gd} of the rectifying transistors have to be considered in addition to accurately describe the circuit characteristics.

To study the influence of the various design parameters of a differential charge pump in a more rigorous way, I considered a simplified charge pump circuit, which includes ideal gate bias sources to model a V_{th} compensation, as illustrated in Fig. 3.8. Figure 3.12 shows simulation results for the characteristic of the output voltage V_{DC} versus the input voltage amplitude $\hat{V}_{in}$ of the simplified circuit for various values of gate bias voltages (V_N and V_P). A load resistance R_L of $250\,\text{k}\Omega$ was connected at the output of the charge pump for the simulations, corresponding to $4\,\mu\text{W}$ output power at a V_{DC} of 1 V. As shown in Fig.3.12,



(a) Q versus P_{in}.



(b) η versus P_{in}.

Figure 3.13: Simulation results of the quality factor Q (a) and the power conversion efficiency η (b) versus the input power P_{in} for varying values of the gate bias voltages V_N and V_P at $f_0 = 900\,\text{MHz}$ and $R_L = 250\,\text{k}\Omega$. The simulated circuit corresponds to a differential eight-stage charge pump including ideal bias sources (see Fig. 3.8).

V_{DC} remains essentially zero for a $\hat{V}_{in}$ lower than the effective threshold voltages of the NMOS and PMOS rectifying transistors that equal $V_{th} - V_N$ and $|V_{th}| - V_P$,* respectively. For values slightly above the effective threshold voltages, V_{DC} exhibits a steep rise with

increasing $\hat{V}_{\mathrm{in}}$ before flattening slightly at elevated values of input voltage amplitude. The onset of the rising V_{DC} is shifted towards lower values of $\hat{V}_{\mathrm{in}}$ by increasing V_{N} and V_{P}.

Figure 3.13a and Fig. 3.13b demonstrate the effect of the gate biasing on the characteristics of the quality factor Q and the power conversion efficiency η, respectively. Similar to single-ended charge pumps (see Fig. 3.7), the characteristic of Q versus P_{in} becomes flatter with increasing bias voltages V_{N} and V_{P}, resulting in significantly lower values of Q at low levels of input power P_{in}.

In contrast to this, the power conversion efficiency of differential RF charge pumps shows a decisively different behavior in comparison to single-ended implementations. η exhibits a bell shaped characteristic versus P_{in} for a fixed R_{L} with a distinct maximum, as shown in Fig. 3.13b. For input power levels to the left of this maximum, the power losses due to the forward voltage drop at the rectifying transistors dominate. At higher values of P_{in}, the reverse current peaks, as illustrated in Fig. 3.10, become more pronounced, degrading the power conversion efficiency. The characteristic of η is essentially shifted to the left by increasing the gate bias levels V_{N} and V_{P}, and thus the power conversion efficiency at low levels of P_{in} is significantly enhanced. At the same time, the peak efficiency diminishes.

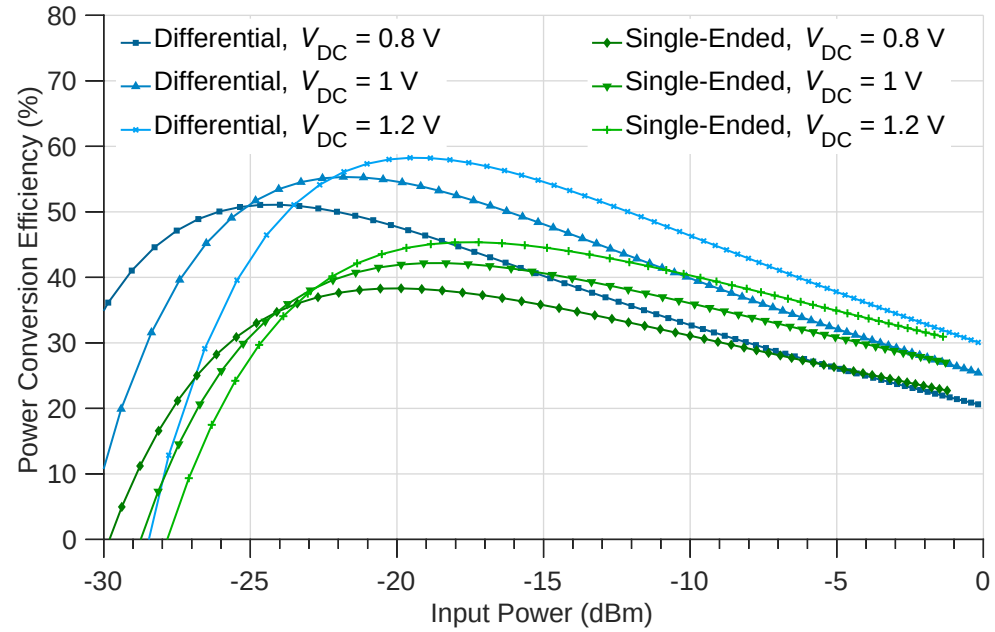
The V_{th} compensation is the key factor for realizing RF charge pumps with a low input quality factor and a high power conversion efficiency specifically at low levels of input power, as illustrated by the graphs in Fig. 3.13a and Fig. 3.13b. The generation of the required gate bias voltages V_{N} and V_{P} at a typically low input voltage amplitude of less than 300 mV poses the main challenge regarding the circuit design.

3.2.3 Single-Ended Versus Differential Circuit Topologies

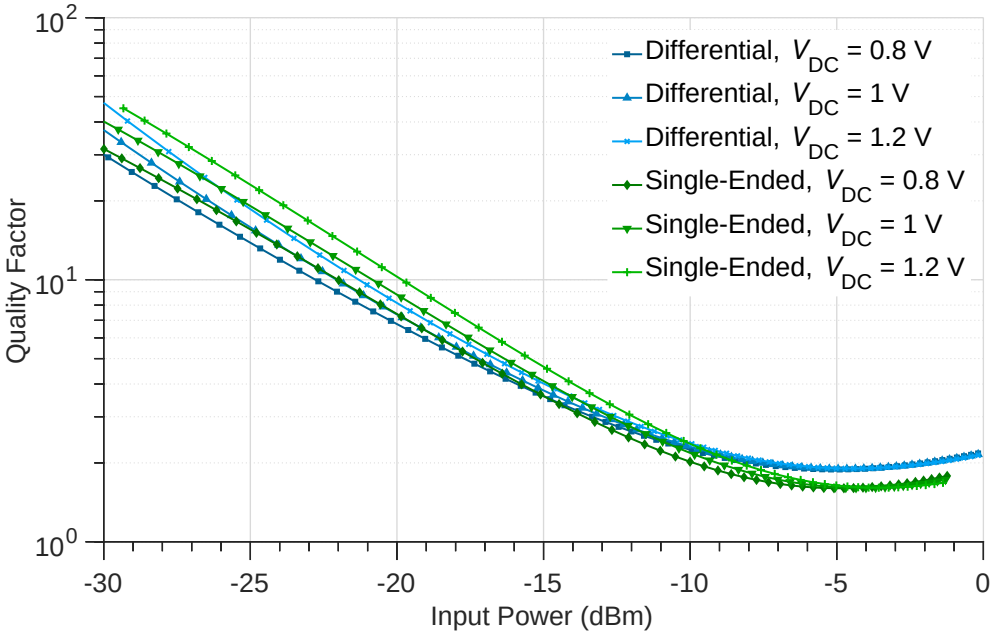
Single-ended circuit implementations generally result in a lower system complexity (e.g., a simpler signal routing), which again can be an advantage regarding costs and the required space. This argument does not hold true with respect to classical UHF RFID tags, as the tag IC and the front-end are directly attached to the antenna. The tag circuitry is isolated from the environment otherwise. A single-ended front-end can still be considered to be an advantage concerning the complexity of circuit realizations in highly scaled CMOS technologies. As noted in Sect. 2.2.4, the ESD diodes of a single-ended front-end clamp the input voltage amplitude typically to values below 1 V, which are compatible to the low maximum voltage ratings of thin-oxide transistors in advanced CMOS process nodes. Differential UHF RFID front-ends, on the other hand, potentially require a dedicated RF voltage limiter to prevent damaging overvoltages, as discussed in more detail in Ch. 4.

As previously mentioned, I investigated in simulations simplified RF charge pump circuits using ideal gate bias sources in order to asses the performance of different charge pump topologies. The power conversion efficiency of these simplified circuits has been maximized in an iterative process, considering constraints on the quality factor Q and the DC output power $P_{\mathrm{DC,\,min}}$, for example, as listed in Table 3.1. Therefore, the performance of the evaluated circuit topologies can be directly compared regarding the specifications targeted in this thesis.

*By definition, the threshold voltage of PMOS enhancement mode transistors has a negative sign. To facilitate the readability, I refer in this work to the absolute value of the threshold voltage $|V_{\mathrm{th}}|$ concerning PMOS transistors. Furthermore, I assume here that the threshold voltages of NMOS and PMOS transistors are equal in absolute value.



(a) η versus P_{in}.



(b) Q versus P_{in}.

Figure 3.14: Comparison of simulation results of η (a) and Q (b) versus P_{in} of a 4-stage single-ended and an 8-stage differential RF charge pump at $f_0 = 900\,\text{MHz}$. The simulated circuits include ideal gate biasing sources, as shown in Fig. 3.1 and Fig. 3.8.

Figure 3.14a and Fig. 3.14b show a comparison of the simulated characteristics of the power conversion efficiency η and the quality factor Q of an eight-stage differential charge pump and a four-stage single-ended charge pump for a fixed output voltage V_{DC}. The differential circuit shows a decisively higher η than the single-ended topology; especially at low input powers, which implies an advantage with respect to the sensitivity P_{min}. As shown

Table 3.2: Comparison of single-ended and differential RF charge pumps including ideal gate biasing sources (see Fig. 3.1 and Fig. 3.8) at $P_{\mathrm{DC,\,min}} = 4\,\mu\mathrm{W}$ and $V_{\mathrm{DC}} = 1\,\mathrm{V}$.

Topology	Device Type	η	P_{min}	Q	$\hat{V}_{\mathrm{in}}$	C_{P}	R_{P}
4-stage single-ended	High-V_{th}	41.8 %	−20.2 dBm	9	290 mV	362 fF	4.4 kΩ
8-stage differential	High-V_{th}	55.1 %	−21.4 dBm	9	252 mV	362 fF	4.4 kΩ
4-stage single-ended	Thick-oxide I/O	40 %	−20 dBm	9	291 mV	376 fF	4.2 kΩ
8-stage differential	Thick-oxide I/O	46.7 %	−20.7 dBm	9	253 mV	424 fF	3.7 kΩ

in Fig. 3.14b, the quality factor of the two circuits follows similar characteristics versus the input power for different values of V_{DC}.

Table 3.2 summarizes the simulation results of the evaluated charge pump circuits that were implemented using the thin-oxide high-V_{th} transistors available in the considered 40 nm CMOS technology. Additionally, results of a single-ended and a differential charge pump are included in the table that incorporate thick-oxide I/O transistors as rectifying elements. The differential RF charge pump, which uses high-V_{th} devices, shows with a value of 55.1 % the highest efficiency corresponding to an advantage in the sensitivity P_{min} of 1.2 dB and 0.7 dB over the associated single-ended topology and the differential circuit with thick-oxide devices, respectively.

3.3 Differential Threshold Voltage Compensated RF Charge Pumps

The generation of the bias voltages for the compensation of the V_{th} of the rectifying transistors, as illustrated in Fig. 3.1 and Fig. 3.8, requires additional biasing circuitry.* Providing sufficiently high bias voltages at typically low input voltage amplitudes of less than 300 mV poses a major design challenge. At the same time, the power consumption and the added parasitic capacitance of the biasing circuits have to be low to minimize the impact on the overall RF performance. Various approaches for the V_{th} compensation of RF-DC power converters have been proposed in literature that can be roughly divided into external and internal V_{th} compensation techniques [73].

3.3.1 Threshold Voltage Compensation Techniques

An external V_{th} compensation uses a dedicated circuit, which operates independently from the main charge pump, to generate and control the required bias voltages. The interface between the bias generator and the rectifying transistors of the main charge pump can be realized by means of a switched-capacitor circuit, for example [74]. The power supply for the bias generation can be provided by an external energy storage such as a battery, or alternately by means of a secondary charge-pump. The power consumption of the bias generator is usually very low, and thus the power conversion efficiency of the secondary charge pump can be relaxed in exchange for a higher voltage sensitivity.

*Indeed, the usage of floating gate transistors allows a static adjustment of the V_{th} of the rectifying transistors by depositing charge on the floating gate, as demonstrated by Mandal and Sarpeshkar [41]. This approach is nevertheless not suitable for practical circuit implementations.

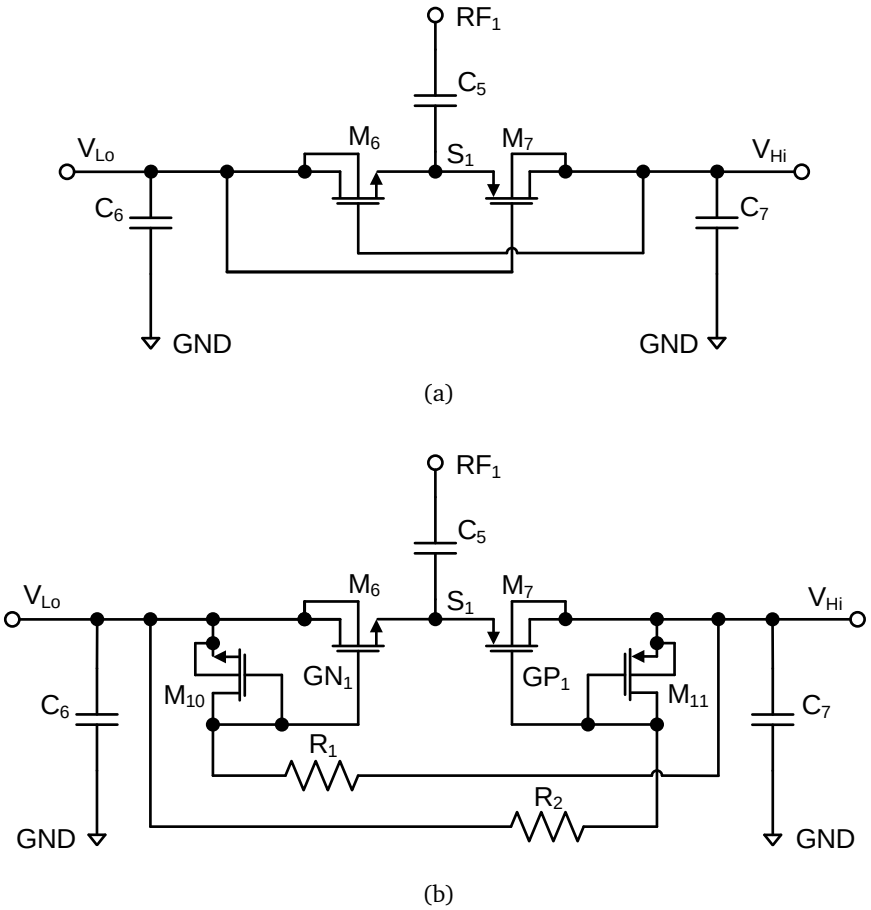


Figure 3.15: Schematics of two single-ended RF charge pumps that apply a V_{th} self-compensation technique, as proposed by (a) Kotani and Ito [77], and (b) Nakamoto *et al.* [76].

In case of an internal V_{th} compensation, the generation of the bias voltages is directly integrated in the RF charge pump itself. Figure 3.15 shows two examples of internal V_{th} compensation schemes applying a feedback approach. The illustrated schematics correspond to single-ended circuit implementations. Nevertheless, the same principles can be applied to differential RF charge pumps. In the circuit of Fig. 3.15a that has been proposed by Kotani and Ito [77], the gate of the NMOS rectifying transistor M_6 is directly connected to the output node of the charge pump stage V_{Hi}. The feedback connection results in a positive bias voltage at the gate of M_6 with respect to node S_1, once the charge pump has reached a stable operating point. In a complementary fashion, the gate of the PMOS device M_7 is connected to the input node of the stage V_{Lo} inducing a negative bias at the gate relative to S_1. The operating principle has been previously considered by Dickson for the implementation of DC-DC charge pumps [143].

The gate bias voltages at the rectifying transistors of the charge pump shown in Fig. 3.15a are directly dependent on the DC output voltage. If the output voltage rises beyond a critical point, the reverse leakage increases strongly and the power conversion efficiency of the RF charge pump collapses (see [77]). Nakamoto *et al.* have introduced a simple regulation circuit, as depicted in Fig. 3.15b, consisting of the NMOS (PMOS) diode M_{10} (M_{11}) as well as the resistor R_1 (R_2) to stabilize the bias voltage at M_6 (M_7) versus an increasing $\hat{V}_{\mathrm{in}}$ [76].

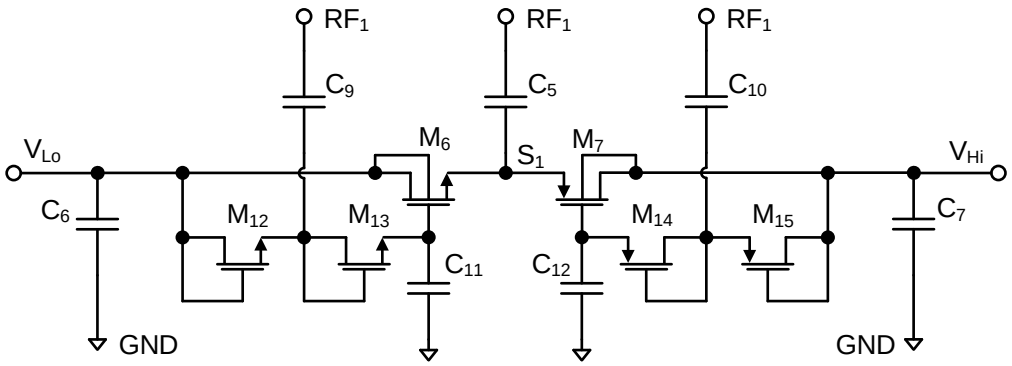


Figure 3.16: Circuit diagram of a V_{th} compensated single-ended RF charge pump stage using auxiliary charge pumps for generating the gate bias voltages for M_6 and M_7. The shown circuit corresponds to a single-ended version of the differential RF charge pump described in [83].

The bias levels, and thus the minimum values of $\hat{V}_{\mathrm{in}}$ that can be achieved by applying a single-stage feedback, as illustrated in Fig. 3.15, are limited. This is especially critical with respect to circuit implementations using transistors with an elevated value of V_{th}, as considered in this thesis. Using a multi-stage feedback scheme, as proposed by Papotto *et al.*, enables an increase of the bias levels at lower values of $\hat{V}_{\mathrm{in}}$ [78]. Nevertheless, spanning multiple charge pump stages for providing the gate bias voltages for the rectifying transistors may cause issues during the start-up of the circuits especially at low temperatures (see Sect. 3.4.3).

As an alternative, the RF charge pumps presented in this thesis utilize small-scale auxiliary charge pumps within each stage to generate the bias voltages, following the approach proposed by Bergler *et al.* [83]. Figure 3.16 illustrates an example of a single-ended charge pump stage that includes two auxiliary biasing charge pumps for the rectifying transistors. The charge pump comprising the two diode connected NMOS transistors M_{12}, M_{13}, and the capacitor C_9 provides a positive bias voltage at the gate of M_6 with reference to node S_1. In a complementary fashion, the PMOS-diodes M_{14}, M_{15}, and the capacitor C_{10} build the auxiliary charge pump to generate the negative bias voltage for M_7. The capacitors C_{11} and C_{12} decouple the remaining RF signal at the gate terminals of the rectifying transistors.

3.3.2 Combined Gate and Bulk Biasing

In this thesis, I present three differential V_{th} compensated RF charge pumps. I refer to the three circuit versions as charge pump A, B, and C throughout the following chapters. The three charge pumps primarily differ with respect to the deployed auxiliary biasing circuits. The circuit topology of charge pump A is based on an existing design in a prior CMOS technology, and uses only gate biasing for the V_{th} compensation, as illustrated in Fig. 3.8. The gate bias voltages are generated by auxiliary charge pumps, as described in detail in Sect. 3.3.3. Simulations of charge pump A revealed that the included biasing circuitry is not capable of providing sufficiently high voltages to bias the used high-V_{th} transistors in an optimum manner. I therefore extended the existing approach in the designs of charge pump B and C by introducing a forward bias at the bulk terminals of the rectifying transistors to enhance the power conversion efficiency.

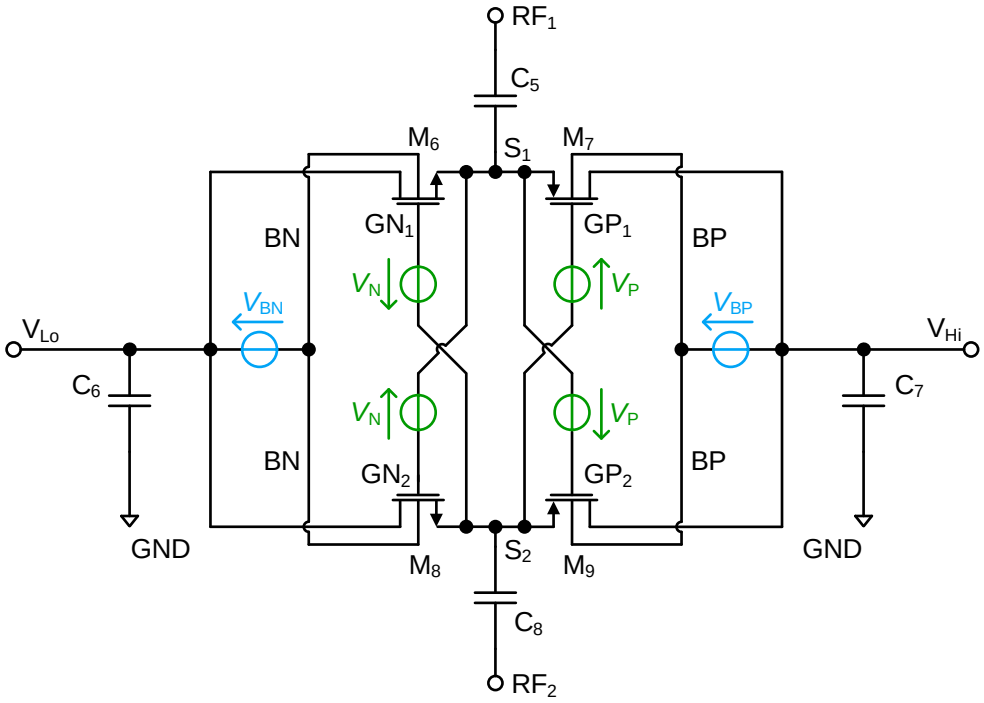


Figure 3.17: Simplified schematic of a V_{th} compensated differential RF charge pump stage applying a combined gate and bulk biasing scheme. The gate (V_N, V_P) and the bulk bias sources (V_{BN}, V_{BP}) for the rectifying transistors are highlighted in green and blue, respectively (reprinted from [144], ©2016 IEEE).

Figure 3.17 shows the schematic of a cross-coupled charge pump stage including gate and bulk biasing sources to compensate the threshold voltage of the rectifying transistors. In the same way as in the circuit diagram of Fig. 3.8, the voltage sources V_N provide a positive bias at the gate terminals of the NMOS rectifying transistors M_6 and M_8 with reference to nodes S_1 and S_2. In addition, the bulk terminals of the transistors are biased by a voltage V_{BN}. A positive bias at the bulk terminal with reference to the source (corresponding to a negative V_{sb}) decreases the V_{th} of an NMOS transistor according to Eqn. 3.6. The threshold voltage scales only with the square root of V_{sb}, which strongly mitigates the achievable effect. Moreover, the bias voltage that can be applied at the bulk terminal has to be limited to prevent a forward conduction of the p-n junction at the interface between the isolated p-well and the deep n-well. Complementary to V_N and V_{BN}, the voltage sources V_P and V_{BP} provide a bias at the gate and bulk terminals of the PMOS rectifying transistors M_7 and M_9.

3.3.3 Auxiliary Biasing Charge Pumps

In the proposed V_{th} compensation, both the gate and the bulk bias voltages are generated by means of auxiliary charge pumps. Each unit stage incorporates four biasing charge pumps, one for each of the rectifying transistors. Figure 3.18 illustrates a principle circuit of the auxiliary charge pump for the generation of the gate (V_N) and bulk bias voltage (V_{BN}) for the NMOS rectifying transistor M_6 of the cross-coupled charge pump stage depicted in Fig. 3.17. The two MOS-diodes M_{16}, M_{17}, and the capacitors C_{13}, C_{14} constitute a two-stage charge pump generating a positive voltage V_N at the gate of M_6 at node GN_1 with respect to

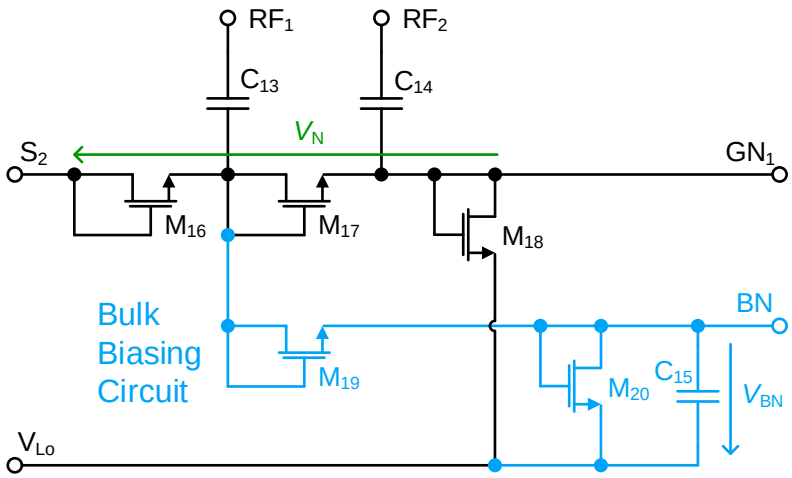


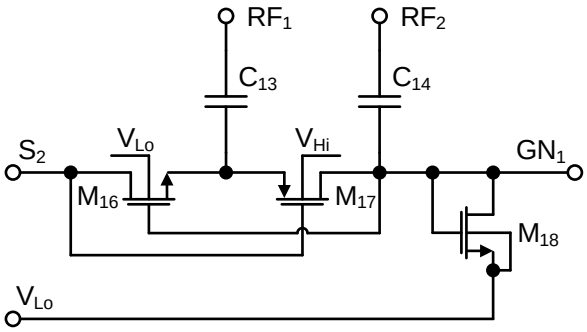
Figure 3.18: Principle circuit of an auxiliary charge pump to generate the gate and bulk bias voltages for the NMOS rectifying transistor M_6 of an unit stage as shown in Fig. 3.17 [144]. The sub-circuit providing the bulk bias voltage V_{BN} is highlighted in blue.

node S_1. The gate biasing sub-circuit mostly corresponds to the circuit principle described in [83]. The additional diode-connected transistor M_{18} regulates V_N versus a varying input voltage amplitude in a similar way as in the circuit by Nakamoto *et al.* [76], shown in Fig. 3.15b.

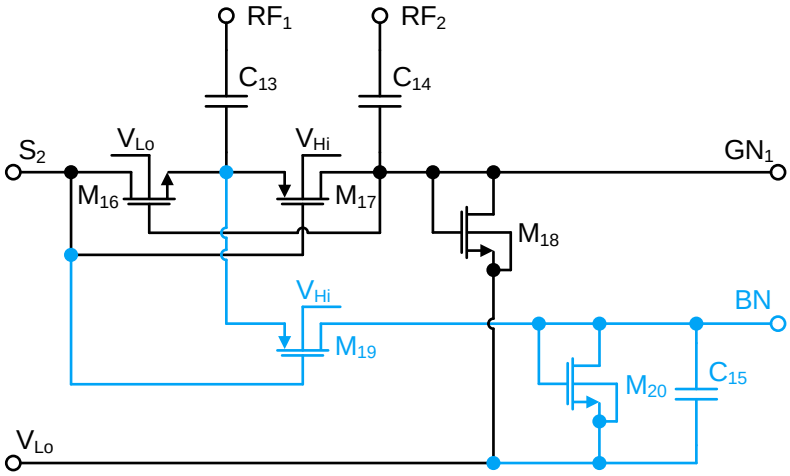
As illustrated in Fig. 3.18, transistor M_{19} taps the gate biasing charge pump at the source of M_{16} to derive the bulk bias voltage V_{BN}. The level of V_{BN} is regulated by the diode-connected transistor M_{20}. The capacitor C_{15} decouples the RF signal at node BN that is connected to the bulk terminals of both NMOS rectifying transistors M_6 and M_8 in the circuit of Fig. 3.17.

Figure 3.19 shows the detailed schematics of the auxiliary biasing charge pumps of the three RF-DC power converters presented in this work. The three schematics correspond to the biasing circuit for the NMOS rectifying transistor M_6 of an unit stage as depicted in Fig. 3.8 or Fig. 3.17. Charge pump A only applies gate biasing for the V_{th} compensation, using a two stage auxiliary charge pump for the bias generation similar to the simplified circuit of Fig. 3.18. As shown in Fig. 3.19a, the gates of the rectifying transistors M_{16} and M_{17} are connected to the drain terminals of each other, in the same manner as in the circuit proposed by Kotani and Ito [77] that is shown in Fig. 3.15a. The feedback connection inherently results in a bias voltage at the gate terminals of the rectifying transistors, which effectively increases the value of V_N for a given level of $\hat{V}_{in}$.

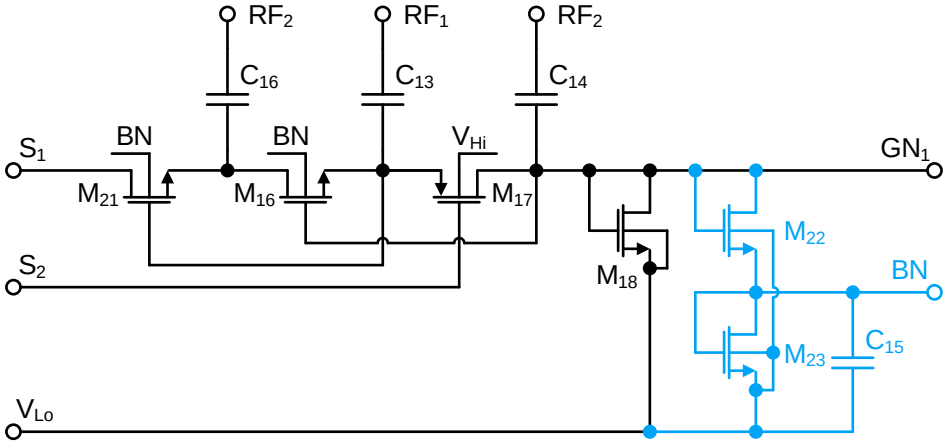
The auxiliary biasing circuit of charge pump B also includes a two-stage charge pump for generating the gate bias voltage V_N, as shown in Fig. 3.19b. In addition, the bulk terminals of the rectifying transistors of charge pump B are biased to enhance the V_{th} compensation. The bulk bias voltage V_{BN} for the NMOS rectifying transistors is generated by the sub-circuit highlighted in blue that essentially follows the same operating principle as the simplified biasing circuit shown in Fig. 3.18. The PMOS transistor M_{19} forms a second branch of the biasing charge pump to generate the bias voltage V_{BN} at node BN with reference to node V_{Lo}. Analogously to M_{17}, the gate of M_{19} is connected to the input of the biasing charge pump at the drain of M_{16}, which inherently provides a bias voltage at the gate of M_{19}.



(a) Biasing circuit of charge pump A



(b) Biasing circuit of charge pump B



(c) Biasing circuit of charge pump C

Figure 3.19: Schematics of the auxiliary charge pumps that are used to generate the bias voltages for the V_{th} compensation of the three RF charge pumps presented in this work. Shown are the biasing circuits for the NMOS rectifying transistor M_6 of an unit stage (see Fig. 3.8 or Fig. 3.17). Charge pump A (a) uses only gate biasing for the V_{th} compensation. Charge pump B (b) and charge pump C (c) additionally include a sub-circuit providing a bulk bias that is highlighted in blue (reprinted from [145, 146], ©2017 IEEE).

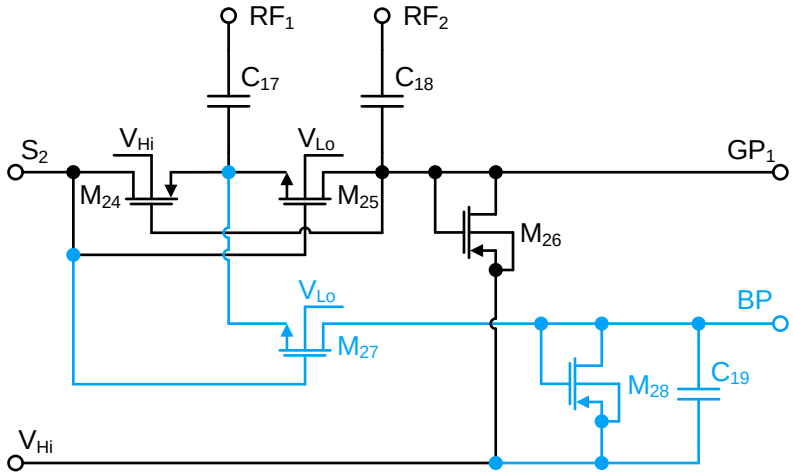
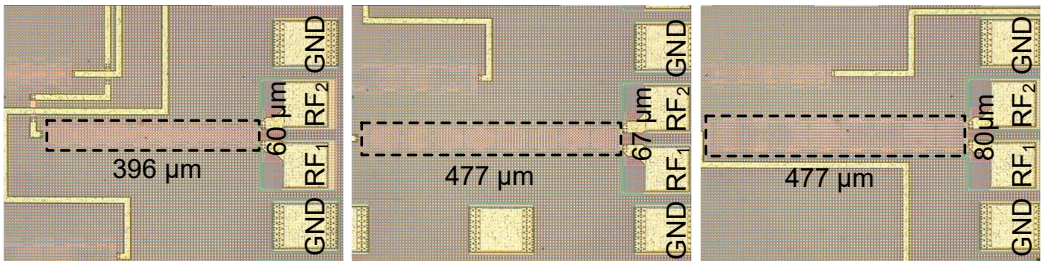


Figure 3.20: Schematic of the auxiliary biasing charge pump for the PMOS rectifying transistor M_7 of an unit stage of charge pump B (see Fig. 3.17) [144]. The circuit corresponds to a complementary version of the biasing charge pump for the NMOS rectifying transistor M_6 that is shown in Fig. 3.19b.

As shown in Fig. 3.19c, the auxiliary biasing charge pump of charge pump C has been extended by an additional stage consisting of transistor M_{21} and the capacitor C_{16}. The gates of the NMOS transistors M_{21} and M_{16} are connected to the outputs of the respective following charge pump stages, corresponding to a V_{th} self-compensation. Accordingly, the gate of the PMOS transistor M_{17} is connected to node S_2 (at the source terminals of M_8 and M_9 in Fig. 3.17) resulting in a negative bias voltage at the gate. A positive bias voltage is applied at the bulk terminals of M_{21} and M_{16} to compensate the increase of the V_{th} of the transistors, as implied by Eqn. 3.6. The bulks of M_{21}, M_{16}, and the NMOS rectifying transistors M_6 and M_8 (see Fig. 3.17) are connected to node BN within each stage, and thus share the bulk bias voltage V_{BN}. As shown in Fig. 3.19c, V_{BN} is derived from the generated gate bias at node GN_1 by a voltage divider consisting of the two MOS-diodes M_{22} and M_{23}.

The biasing circuits for the PMOS rectifying transistors of the RF charge pumps correspond to complementary versions of the circuits shown in Fig. 3.19. Figure 3.20 shows, for example, the biasing charge pump for the PMOS transistor M_7 of an unit stage of charge pump B, as illustrated in Fig. 3.17. In comparison to the circuit of Fig. 3.19b, the NMOS devices have been replaced by PMOS devices and vice verse. The circuits are otherwise functionally identical. The biasing charge pumps for the NMOS transistor M_8 and the PMOS transistor M_9, which build the second branch of a charge pump stage (see Fig. 3.8 or Fig. 3.17), equal the circuits in Fig. 3.19 and the associated complementary circuits, respectively. The connecting signals of the biasing circuits for M_8 and M_9 are exchanged accordingly.



(a) Charge pump A (b) Charge pump B (c) Charge pump C

Figure 3.21: Die photos of the fabricated charge pump circuits including the contact pads. The RF input terminals correspond to nodes RF_1 and RF_2 in Fig. 3.8 (reprinted from [144, 145], ©2016 IEEE).

3.4 Experimental Results

3.4.1 Circuit Prototypes

The three implemented RF charge pumps comprise each eight cascaded unit stages. The total number of stages and the design of the unit stages have been optimized in simulations, considering the specifications discussed in Sect. 3.1. To evaluate the performance and the functionality of the proposed circuit techniques, the three RF charge pumps have been fabricated in a 40 nm CMOS technology. The test chip includes, in addition to the stand-alone charge pumps, two UHF RFID front-ends that incorporate charge pump A and charge pump B, respectively, alongside ESD protection diodes, a backscatter modulator, and an RF limiter.* Appendix A.1 gives an overview of the fabricated test chip.

Figure 3.21 shows die photos of the three fabricated RF charge pumps. The required layout area is dominated by the metal fringe capacitors that are used for realizing the main coupling capacitors (C_5, C_8 in Fig. 3.17) and the corresponding devices of the auxiliary charge pumps (e.g., C_{13}, C_{14} in Fig. 3.19). Furthermore, the layout overhead of the n-well and the isolated p-well structures to separate the bulks of the rectifying transistors from the substrate represents a considerable portion of the required chip area. The dimensions of the well structures are defined inherently by the size of the enclosed active devices and associated design rules. The wells have been additionally increased in the layout of the RF charge pumps to minimize the impact of the well-edge proximity effect on the V_{th} of the rectifying transistors.†

In the designs of charge pump B and charge pump C, the coupling capacitors (e.g., C_5, C_8) and the dimensions of the rectifying transistors (M_{6-9} in Fig. 3.17) have been scaled up to improve the power conversion efficiency. Moreover, the additional devices but also the n-well and isolated p-well structures that are necessary for realizing the bulk biasing cause a considerable increase of the required layout area in comparison to charge pump A.

*The two manufactured UHF RFID front-ends do not include a demodulator. The envelope detector of a demodulator is typically capable to detect signal powers much below P_{min}, and therefore poses no direct limitation regarding the RF performance.

†In highly scaled CMOS technologies, the scattering of ions at photoresist edges during the ion-implantation causes a rise of the dopant levels near the well-edges, and thus an increase of the V_{th} of transistors close to the edges [147].

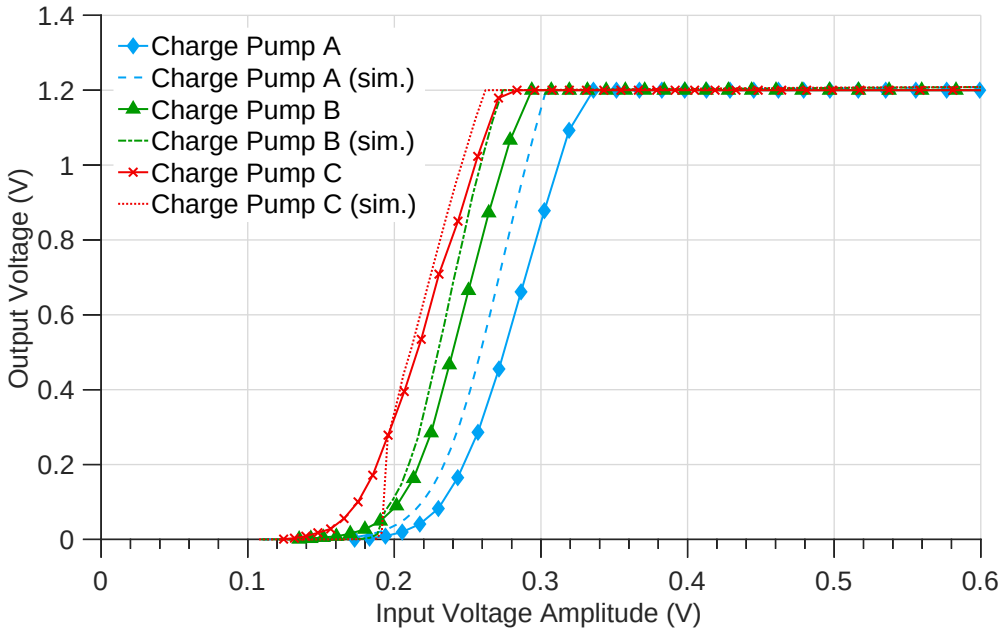


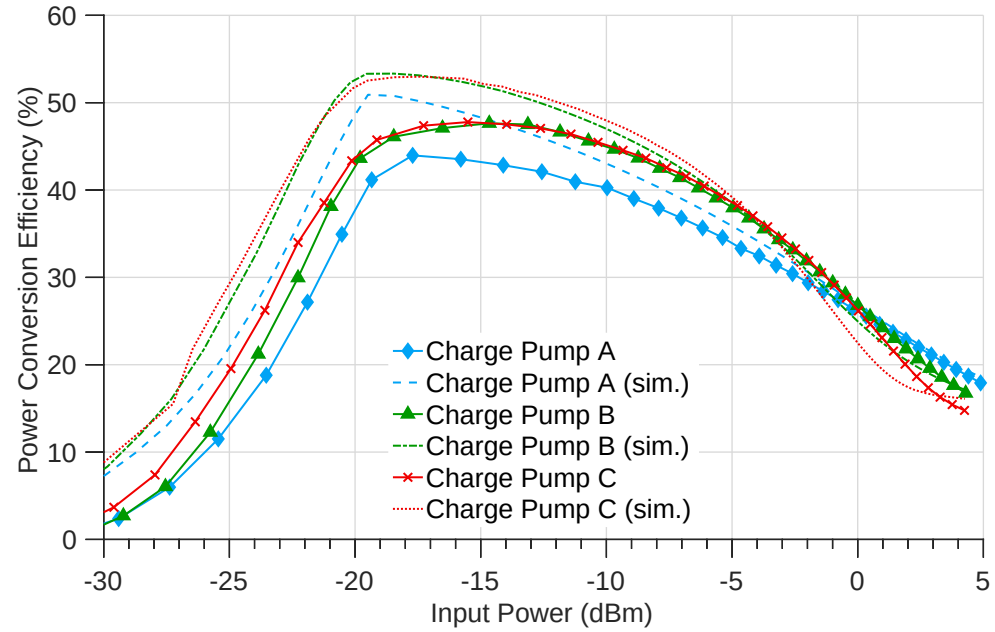
Figure 3.22: Measurement and post-layout simulation (sim.) results of the output voltage V_{DC} of the three charge pumps versus the input voltage amplitude $\hat{V}_{in}$ for a load resistance R_L of 250 kΩ and a carrier frequency f_0 of 900 MHz.

As presented in Fig. 3.21, the layout area of charge pump B and charge pump C is in total 35 % and 61 % larger, respectively, than the layout area of charge pump A.

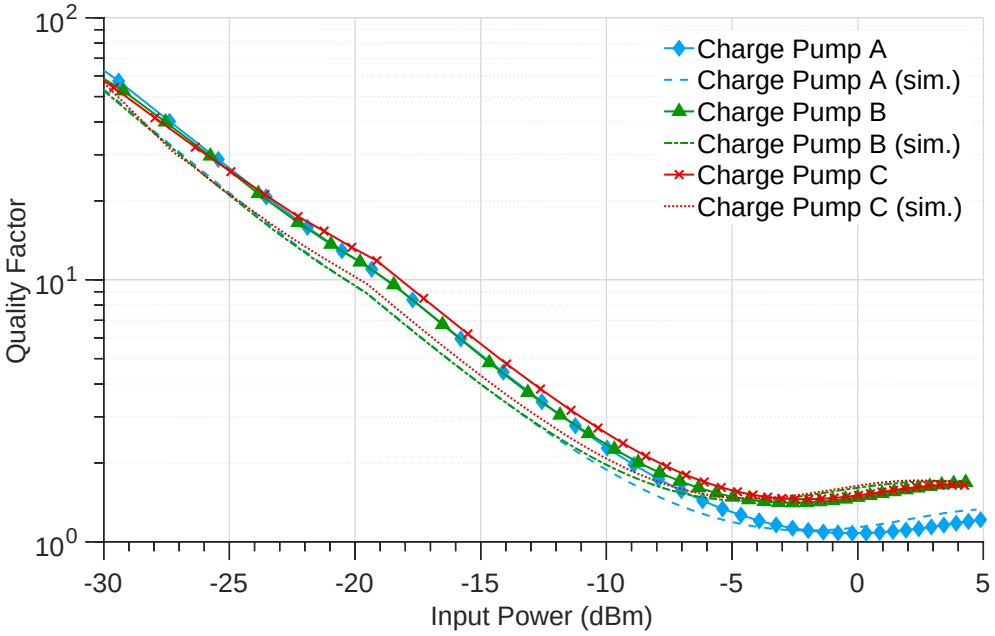
3.4.2 Static Characteristics

Samples of the fabricated test chip have been packaged in an open-cavity J-leaded ceramic chip carrier (JLCC) package. For the measurements of the static RF characteristics, the RF terminals of the test circuits were directly contacted on-chip inside the package by means of a ground-signal-signal-ground (GSSG) probe. The DC outputs of the charge pumps and the digital control signals of the test chip were bonded to package pins and were connected via a test printed circuit board (PCB) for the measurements. A vector network analyzer (VNA), which can provide a true differential stimulus, was used to measure the scattering (S) parameters at the input of the RF charge pumps versus the available power. In parallel, the DC output power P_{DC} was measured by means of a source measure unit (SMU) for fixed load resistances R_L of 250 kΩ and 50 kΩ. The SMU was configured to limit the output voltage of the charge pumps V_{DC} to a value of 1.2 V that is in compliance with the maximum voltage ratings of the thin-oxide devices of the considered 40 nm CMOS technology. Therefore, the SMU emulated the behavior of a DC limiter of a front-end (see Fig. 2.9). Appendix A.2 gives a more detailed description of the measurement setups that were used for evaluating the static characteristics of the test circuits.

Figure 3.22 shows measurement results of the DC output voltage V_{DC} versus the input voltage amplitude $\hat{V}_{in}$ of the three presented RF charge pumps. The characteristics of charge pump B and charge pump C are shifted towards lower values of $\hat{V}_{in}$ in relation to charge pump A, as a consequence of the enhanced V_{th} compensation and specifically the introduced bulk biasing. The post-layout simulation results shown in comparison closely resemble the



(a) η versus P_{in}.



(b) Q versus P_{in}.

Figure 3.23: Measurement and post-layout simulation (sim.) results of the power conversion efficiency η (a) and the quality factor Q (b) of the three charge pumps versus the input power P_{in} for a load resistance R_{L} of 250 kΩ and a carrier frequency f_0 of 900 MHz.

measured characteristics. As implied by Eqn. 3.1, a reduction of $\hat{V}_{\text{in}}$ effectively allows a larger input capacitance C_{P} without increasing the quality factor Q, assuming a fixed P_{DC} and η.

Figure 3.23a confirms that the extended V_{th} compensation, as applied in charge pump B and charge pump C (see Fig. 3.19), improves the power conversion efficiency. The two cir-

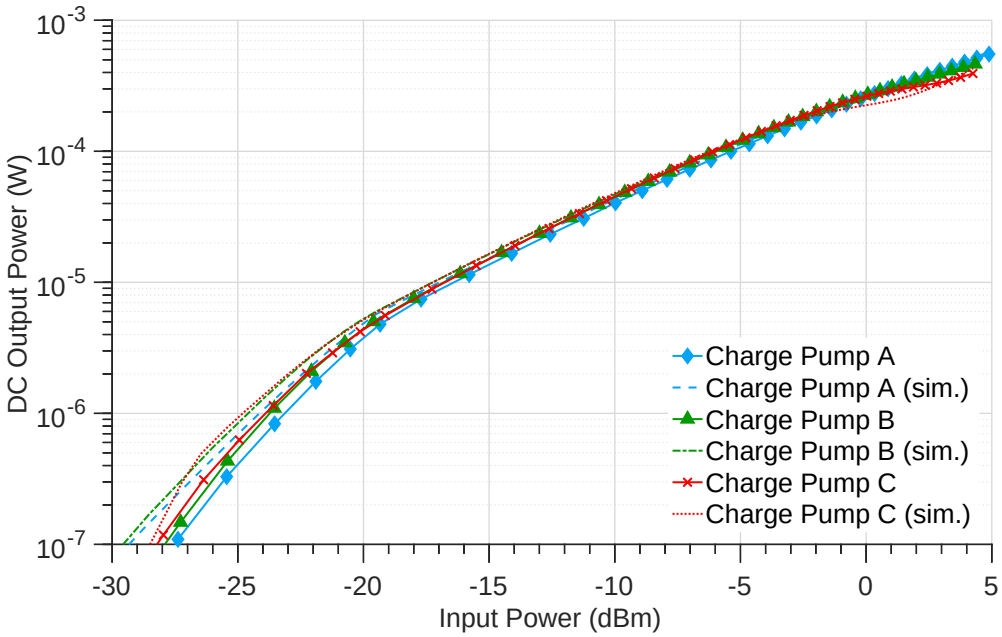


Figure 3.24: Measurement and post-layout simulation (sim.) results of the output power P_{DC} of the three charge pumps versus the input power P_{in} for a load resistance R_L of 250 kΩ and a carrier frequency f_0 of 900 MHz.

Table 3.3: Overview of the measurement results of the three RF charge pumps for a load resistance R_L of 250 kΩ and 50 kΩ at a V_{DC} of 1 V and a carrier frequency f_0 of 900 MHz.

Circuit	η	P_{in}	Q	$\hat{V}_{in}$	C_P	R_P	R_L
Charge pump A	38.9 %	−19.9 dBm	11.9	310 mV	450 fF	4.6 kΩ	250 kΩ
	36.6 %	−12.6 dBm	3.3	370 mV	460 fF	1.3 kΩ	50 kΩ
Charge pump B	42 %	−20.2 dBm	12.6	270 mV	560 fF	3.9 kΩ	250 kΩ
	42.1 %	−13.2 dBm	3.6	320 mV	590 fF	1.1 kΩ	50 kΩ
Charge pump C	42.7 %	−20.3 dBm	13.6	255 mV	690 fF	3.5 kΩ	250 kΩ
	43.4 %	−13.4 dBm	3.8	300 mV	710 fF	0.9 kΩ	50 kΩ

cuits show a considerable higher η than charge pump A over a broad input power range from about −25 dBm to −3 dBm. As shown in Fig. 3.23b, the three charge pumps demonstrate an almost equal quality factor Q over this range of P_{in}, thus allowing a direct comparison of the implemented circuit techniques with respect to the power conversion efficiency η.

Complementary to Fig. 3.23a, Fig. 3.24 shows measurement and post-layout simulation results of the DC output power P_{DC} of the three RF charge pump versus P_{in}. In consequence of the higher power conversion efficiency, charge pump B and charge pump C achieve a higher output power than charge pump A especially at lower values of input power P_{in}. The simulation results reproduce the measured characteristics for the most part. Nevertheless, the simulations predict a considerably higher output power than observed by measurements at low values of P_{in}, corresponding to a higher power conversion efficiency, as shown in Fig. 3.23a. The post-layout simulations did not account for substrate losses, which possibly cause a significant degradation in efficiency. Furthermore, the accuracy of the extracted parasitic resistances is limited.

Table 3.3 summarizes the most relevant measurement results of the three presented RF charge pumps. At the targeted output power of 4 μW, charge pump B and charge pump C achieve an almost equal η of 42 % and 42.7 %, respectively, which corresponds to an advantage of more than 3 % in comparison to charge pump A. Thus, charge pump B and charge pump C achieve a sensitivity P_{min} of approximately -20.2 dBm. The sensitivity value of charge pump A is about 0.3 dB higher relative to this value. The input quality factor of the three circuits in this operating point is lower than 14, which exceeds the targeted value of 10, as discussed in Sect. 3.1. A Q of 14 yet corresponds to a theoretical maximum bandwidth of 175 MHz for the impedance matching between an antenna and a tag IC according to Eqn. 1.10, assuming a center frequency of 900 MHz and a Γ_{m} of -10 dB.

The extended biasing circuitry of charge pump C (see Fig. 3.19c) results in a reduction of the operating input voltage amplitude $\hat{V}_{\text{in}}$ relative to charge pump B, as shown in Table 3.3. The achieved gain in efficiency, on the other hand, is only marginal. The decrease of $\hat{V}_{\text{in}}$ has been largely balanced by an increase of the input capacitance C_{P} resulting in an almost equal Q (see Eqn 3.1). The parasitic capacitances of other larger circuit structures of an overall front-end like the ESD protection, for example, but also the parasitic capacitance of the antenna assembly additionally increase C_{P} and thus Q. An intrinsically larger input capacitance of the charge pump itself results in a less pronounced degradation of Q due to additional parasitic capacitances.

Performance Comparison

Table 3.4 provides a performance comparison of the three implemented RF-DC power converters with previous publications. Although the targeted DC output power of 4 μW is higher than the specified $P_{\text{DC,min}}$ of most of the other listed works, the charge pumps presented in this work achieve similar low values of sensitivity. The three circuits show a high power conversion efficiency in comparison to the other publications, especially considering the low values of P_{in}. The 3-stage charge pump reported by Theilmann *et al.* in [138] reaches with a value of -24.7 dBm a decisively lower P_{min}, and achieves a high η of 29 % at this level of input power. Nevertheless, the used 0.25 μm silicon on sapphire (SOS) CMOS technology is not suitable for the implementation of low-cost RFID transponder ICs. The circuit designs reported in [73] and [148], on the other hand, achieve a considerably higher power conversion efficiency, but only at significantly higher levels of P_{in}. Scorcioni *et al.* propose in [148] a reconfigurable charge pump to improve the tracking of the overall conversion efficiency versus a varying input power, which reaches a peak efficiency of 60 % at a P_{in} of around -9 dBm.

A variety of different evaluation methods is applied in the listed publications, as indicated in Table 3.4, limiting the comparability of the reported results. Apparently, the decision on specific evaluation methods is tightly linked to the considered application scenario. This is also valid regarding the definition of circuit specifications and the relevance that is attributed to certain parameters. The input quality factor and the input impedance at P_{min}, for example, have been rarely reported so far. Therefore, the comparison provided in Table 3.4 is restricted to the sensitivity and the power conversion efficiency.

Table 3.4: Comparison with previous works.

Reference	Technology	Topology	Frequency	$P_{\mathrm{DC,\,min}}$	P_{min}	η
Wang *et al.* * **ISCAS 2015 [84]**	180 nm CMOS	4-stage single-ended	145 MHz	0.5 μW @ 1 V	−22.5 dBm	26 % @ −18 dBm
Scorcioni *et al.* † **MWCL 2013 [148]**	130 nm CMOS	2/4-stage differential	868 MHz	0.8 μW$^{\bullet}$ @ 2 V	−21 dBm	51 %$^{\bullet}$ @ −14.5 dBm
Theilmann *et al.* TCAS-I 2012 [138]	250 nm SOS CMOS	3-stage differential	915 MHz	1 μW @ 1 V	−24.6 dBm$^{\bullet}$	29 % @ P_{min}
Hameed *et al.* $^{*\circ}$ **TCAS-I 2015 [79]**	130 nm CMOS	12-stage single-ended	902 − 928 MHz	1 μW @ 1 V	−20.5 dBm	32 % @ −15 dBm
Papotto *et al.* ‡ **JSSC 2011 [78]**	90 nm CMOS	17-stage single-ended	915 MHz	1.4 μW @ 1.2 V	−18.9 dBm	11 % @ P_{min}
Grasso *et al.* EuMC 2016 [81]	130 nm CMOS	10-stage differential	868 MHz	2.4 μW @ 2.4 V	−22 dBm	38 % @ P_{min}
Stoopman *et al.* § **JSSC 2015 [87]**	90 nm CMOS	5-stage differential	868 MHz	3 μW$^{\bullet}$ @ 1 V	−20 dBm$^{\bullet}$	40 % @ −17 dBm
Kotani *et al.* JSSC 2009 [73]	180 nm CMOS	3-stage differential	953 MHz	20 μW$^{\bullet}$ @ 1 V	−13.5 dBm$^{\bullet}$	65 % @ −10 dBm
This Work	40 nm CMOS	8-stage differential	900 MHz	4 μW @ 1 V	−19.9 dBm	39 %
					−20.2 dBm	42 %
					−20.3 dBm	43 % @ P_{min}

$*$ Including insertion and mismatch losses of an off-chip matching network.

† Including mismatch losses of a hypothetically connected antenna.

○ Measurements using a frequency modulated stimulus.

‡ Including mismatch losses of an on-chip matching network.

§ Including gain and mismatch losses of a connected antenna.

• Estimated value based on published figures.

3.4.3 Dynamic Characteristics

In addition to the static characteristics of the RF charge pumps for pure CW stimuli, I examined the dynamic characteristics of charge pump A and charge pump B; specifically the start-up behavior and the performance for modulated waveforms. As noted, charge pump A and charge pump B have been integrated with ESD protection diodes, a backscatter modulator, and an RF voltage limiter on the test chip to form two UHF RFID front-ends. In the following, I will refer to the two front-ends correspondingly as front-end A and front-end B. The test chip has been assembled in a heatsink very-thin quad flat-pack no-leads (HVQFN) package to evaluate the dynamic characteristics. The RF terminals of the two front-ends have been bonded to package pins, in contrast to the JLCC package variant that was used for the static measurements. I designed a test PCB that comprises a discrete matching network and a discrete balun to transform the differential RF input of the packaged front-ends to a single-ended interface for connecting the measurement equipment. The input impedance of the two front-ends at P_{min} is matched to 50 Ω, considering a DC output voltage V_{DC} of 1 V and a load resistance R_{L} of 250 kΩ. A capacitance of 260 pF is connected at the DC outputs of the front-ends representing a typical value of the buffer capacitance (C_4 in Fig. 2.9) of a UHF RFID tag IC. More details on the used test PCB and the measurement setup can be found in Appendix A.3.

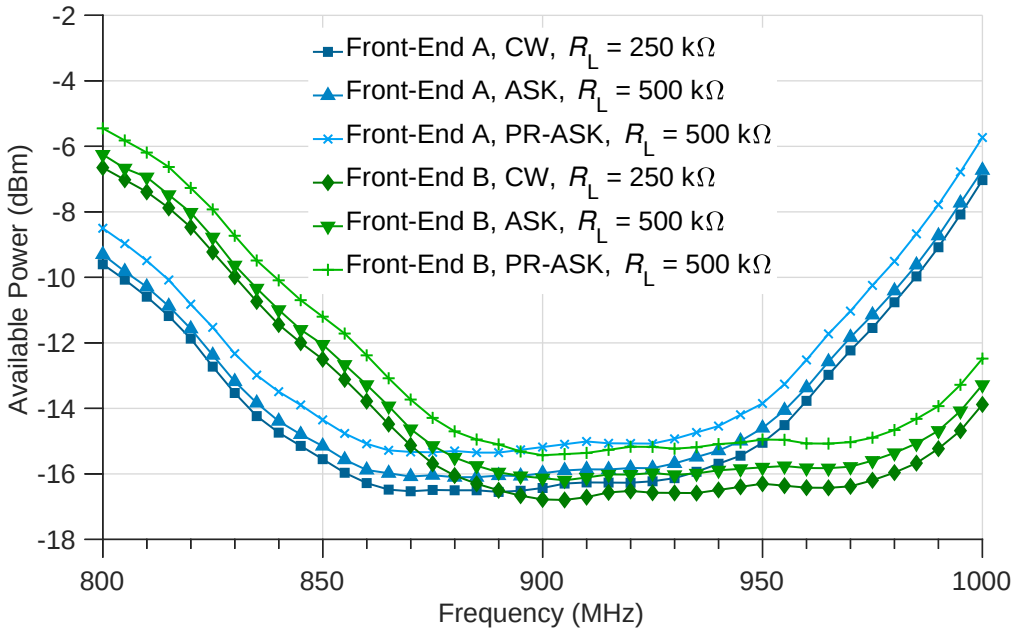


Figure 3.25: Measurement results of the minimum required available power $P_{\mathrm{av,min}}$ versus the frequency. The characteristics correspond to a CW and modulated stimuli (ASK, PR-ASK), assuming a $P_{\mathrm{DC,min}}$ of 4 μW (250 kΩ) and 2 μW (500 kΩ), respectively.

Figure 3.25 shows the measured minimum required available power at the input of the test PCB $P_{\mathrm{av,min}}$ versus the carrier frequency f_0. $P_{\mathrm{av,min}}$ has been determined considering a fixed load resistance R_{L} and minimum required root mean square (RMS) value for the output voltage V_{DC}. The DC limiter of the front-ends was disabled during the measurements. The estimated values for $P_{\mathrm{av,min}}$ or the available power P_{av} in general include return and insertion losses of the matching network and the balun, in contrast to the quantities P_{min} or P_{in}. The characteristics shown in Fig. 3.25 correspond to a CW, and modulated stimuli using ASK with a 50 % duty cycle,* and a typical PR-ASK waveform as defined in [50]. The ASK and PR-ASK waveforms have a modulation index m of 100 % and a constant modulation period of 6.25 μs that equals the minimum modulation period of a reader signal according to [50]. The estimated value of $P_{\mathrm{av,min}}$ corresponds to the peak of available power in case of measurements with modulated signals.

The two front-ends reach a minimum $P_{\mathrm{av,min}}$ of approximately −16.5 dBm considering a load resistance of 250 kΩ and a CW stimulus, as shown in Fig. 3.25. This value of $P_{\mathrm{av,min}}$ equates to an additional loss of approximately 3.5 dB at a frequency of 900 MHz in comparison to the measured P_{min} of the charge pumps, as summarized in Table 3.3. The observed insertion loss is in line with simulations of the test PCB using S-parameter models for the balun and the components of the matching network. As discussed in Sect. 3.1, I assumed an ASK modulated signal with a 50 % duty cycle would result in an equal value of the sensitivity as in case of a CW stimulus, if the DC load current is reduced by a factor of 2. In contrary to this assumption, the measurements of front-end A show an additional loss of 0.55 dB for the ASK modulated signal. In case of front-end B, the sensitivity decrease is slightly higher

*The ASK waveform is not in compliance with spectral mask requirements for reader signals as defined, for example, in the EPC Generation-2 UHF RFID standard [50], in consequence of the fast rising and falling edges. Therefore, the used ASK signal represents rather the operating condition during the backscatter modulation by the tag IC itself.

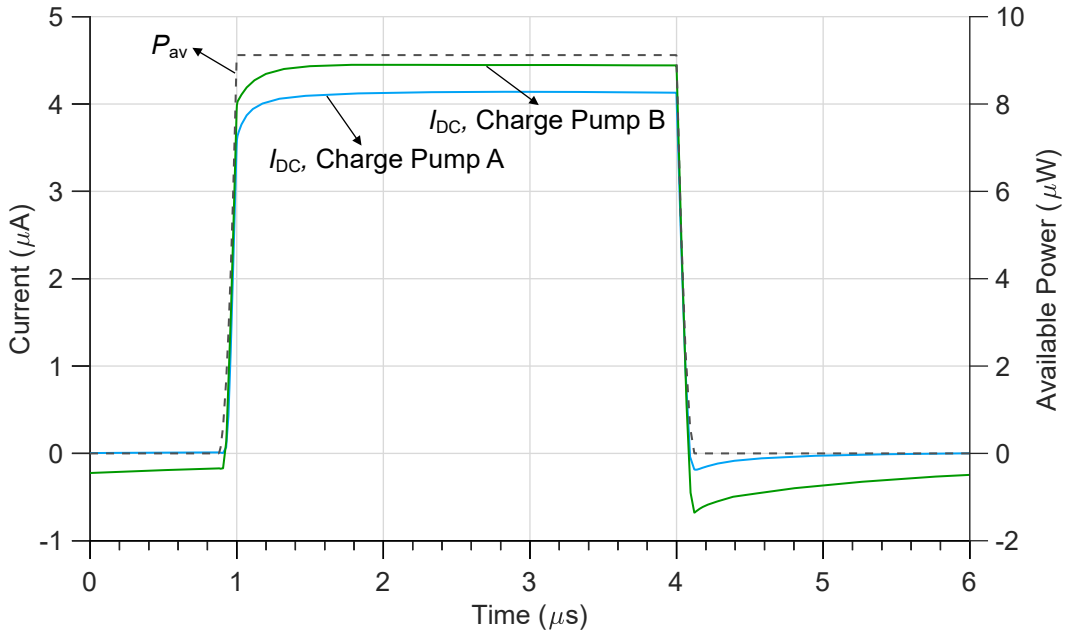


Figure 3.26: Simulation results of the instantaneous output current $I_{DC}(t)$ of charge pump A and charge pump B for an ASK modulated waveform with a carrier frequency f_0 of 900 MHz. Additionally shown is the instantaneous available power $P_{av}(t)$.

with a value of 0.75 dB. For the PR-ASK modulated signal, both front-ends exhibit an even higher loss exceeding 1 dB, although the RMS values of the normalized signal envelopes of the ASK and the PR-ASK signals are almost equal ($\sim 0.7\,V_{RMS}$).

Figure 3.26 depicts post-layout simulation results for the instantaneous output current $I_{DC}(t)$ of charge pump A and charge pump B during one modulation period of an ASK modulated RF signal. The source impedance was matched to the input impedance of the two front-ends at $P_{DC,\,min}$ for the simulations (see Table 3.1). Both front-ends exhibit a minor delay until a constant value of output current is delivered to the buffer capacitor following the rising edge of the modulation envelope. In effect, this delay corresponds to a loss in power conversion efficiency with regard to the average input and output power. At the falling edge of the waveform, a slowly decaying reverse leakage current can be observed that poses an additional power loss. Charge pump B shows a decisively higher reverse leakage in comparison to charge pump A.

The observed transient effects are directly related to the operation of the auxiliary biasing charge pumps that are illustrated in Fig. 3.19. The parasitic capacitances at the internal nodes and specifically the gate and bulk terminals of the biased rectifying transistors cause a delay of the bias voltages at the rising edge of the modulation waveform. If the available power at the input drops, the biased nodes are discharged mostly by the leakage of the MOS-diodes for the bias regulation (e.g., M_{18} in Fig. 3.19). In case of charge pump B, a comparably large decoupling capacitor is connected at the output of the sub-circuit providing the bulk bias voltage (C_{15} in Fig. 3.19b). In consequence, the bulk bias voltage decays only slowly causing a decisively higher reverse leakage. Considering a typical PR-ASK waveform, the signal power and thus the input voltage at the front-end changes only with a limited rate during a modulation pulse. The rectifying gain of the auxiliary biasing charge pumps and thus the efficiency of the RF charge pump however drops rapidly below a $\hat{V}_{in}$ of about

Table 3.5: Overview of measurement results of the two front-ends for CW, PR-ASK, and ASK (50 % duty cycle) modulated stimuli at $f_0 = 900\,\text{MHz}$.

Circuit	T	$P_{\text{av,min}}$, **CW**	$\Delta P_{\text{av,min}}$, **PR-ASK**	$\Delta P_{\text{av,min}}$, **ASK**	$\Delta P_{\text{av,min}}$, **ASK (sim.)**
Front-end A	$-40\,^{\circ}\text{C}$	$-16.65\,\text{dBm}$	$1.15\,\text{dB}$	$0.45\,\text{dB}$	$0.15\,\text{dB}$
	$27\,^{\circ}\text{C}$	$-16.45\,\text{dBm}$	$1.25\,\text{dB}$	$0.55\,\text{dB}$	$0.25\,\text{dB}$
	$85\,^{\circ}\text{C}$	$-15.95\,\text{dBm}$	$1.2\,\text{dB}$	$0.55\,\text{dB}$	$0.35\,\text{dB}$
Front-end B	$-40\,^{\circ}\text{C}$	$-16.9\,\text{dBm}$	$1.3\,\text{dB}$	$0.65\,\text{dB}$	$0.4\,\text{dB}$
	$27\,^{\circ}\text{C}$	$-16.75\,\text{dBm}$	$1.4\,\text{dB}$	$0.75\,\text{dB}$	$0.65\,\text{dB}$
	$85\,^{\circ}\text{C}$	$-16.4\,\text{dBm}$	$1.45\,\text{dB}$	$0.9\,\text{dB}$	$0.85\,\text{dB}$

250 mV to 300 mV. Therefore, the charge pump is not capable to convert a substantial portion of the applied input signal, which corresponds effectively to an additional loss with respect to the average available input power.

The two front-ends were evaluated at ambient temperatures T of $-40\,^{\circ}\text{C}$, $27\,^{\circ}\text{C}$, and $85\,^{\circ}\text{C}$. Table 3.5 summarizes the results for CW, ASK and PR-ASK modulated stimuli with a modulation period of $6.25\,\mu\text{s}$. Additionally, the circuits were measured for signals with modulation periods of $1.56\,\mu\text{s}$ and $25\,\mu\text{s}$ resulting in mostly equal characteristics. As shown, $P_{\text{av,min}}$ of front-end A and front-end B decreases only slightly with rising temperature reaching values of $-15.95\,\text{dBm}$ and $-16.4\,\text{dBm}$, respectively, at $85\,^{\circ}\text{C}$. Similarly, the observed loss in sensitivity $\Delta P_{\text{av,min}}$ when using ASK and PR-ASK modulation waveforms remains for the most part constant versus temperature. Only front-end B shows a slightly more pronounced sensitivity loss at elevated temperatures considering ASK modulated signals. Furthermore, Table 3.5 includes post-layout simulation results of $\Delta P_{\text{av,min}}$ of charge pump A and charge pump B for an ASK modulated stimulus. The simulation results in general conform to the measurements of the two front-ends, although the measured reduction in $P_{\text{av,min}}$ in all cases is slightly higher.

UHF RFID transponders need to be operational within a few milliseconds after an interrogator has started to transmit a CW signal to power-up the tags within range. According to the EPC Generation-2 UHF RFID standard, for example, an interrogator may transmit the first command already after 1.5 ms to 2 ms [50]. Thus, the settling time of RF charge pumps is highly relevant for practical circuit implementations. Figure 3.27 shows the measured settling time of the output voltage V_{DC} of front-end A and front-end B versus the available power P_{av} at an ambient temperature T of $-40\,^{\circ}\text{C}$ and $27\,^{\circ}\text{C}$. The DC limiter of the front-ends was enabled during the measurements to limit V_{DC} to a value below 1.2 V. Moreover, the settling time was evaluated for an elevated ambient temperature of $85\,^{\circ}\text{C}$. The measured characteristics for $T = 85\,^{\circ}\text{C}$ are essentially identical to the measurement results at room temperature. As shown in Fig. 3.27, the settling time increases monotonically with decreasing available power, remaining below 1 ms until a level of around $-17\,\text{dBm}$. This level of available power is already lower than the targeted sensitivity of the front-ends. At an ambient temperature of $-40\,^{\circ}\text{C}$ and an P_{av} lower than $-17\,\text{dBm}$, both front-ends exhibit a surge in the settling time.

Figure 3.28 shows examples of the transient settling of the output voltage V_{DC} of the two front-ends at an ambient temperature of $-40\,^{\circ}\text{C}$. The characteristics correspond to an available power equal to $P_{\text{av,min}}$ considering a load resistance R_{L} of $500\,\text{k}\Omega$ and a minimum required V_{DC} of 0.9 V. Both front-ends show a considerable delay until V_{DC} settles. Above

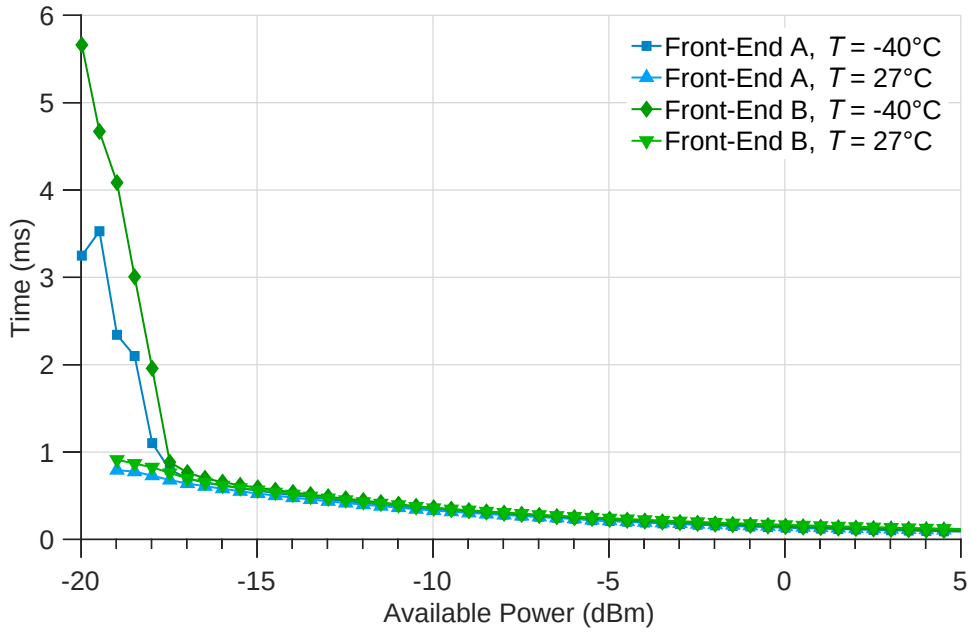


Figure 3.27: Measurement results of the settling time of the output voltage V_{DC} of front-end A and front-end B versus the applied level of available power at $f_0 = 900\,\mathrm{MHz}$, and an ambient temperature T of $-40\,^{\circ}\mathrm{C}$ and $27\,^{\circ}\mathrm{C}$. P_{av} was ramped-up reaching 90 % of the final level after $500\,\mu\mathrm{s}$.

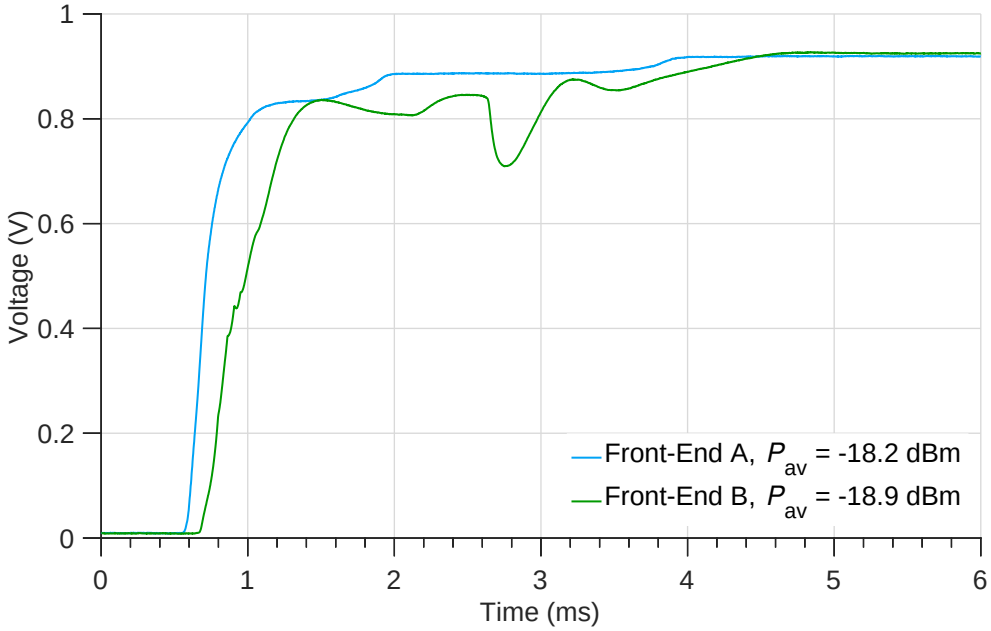


Figure 3.28: Examples of the measured transient output voltage $V_{\mathrm{DC}}(t)$ of front-end A and front-end B during the start-up at a low ambient temperature of $-40\,^{\circ}\mathrm{C}$, $f_0 = 900\,\mathrm{MHz}$, and $R_{\mathrm{L}} = 500\,\mathrm{k\Omega}$. P_{av} was ramped-up reaching 90 % of the final level after $500\,\mu\mathrm{s}$.

all, the settling transients of front-end B exhibit a rather unsteady behavior. The observed effects are primarily caused by the start-up delay of the auxiliary biasing circuits of charge pump A and charge pump B that are depicted in Fig 3.19. The auxiliary charge-pumps use

a self-biasing approach to compensate the threshold voltage of the included rectifying transistors. As a result of the incorporated feedback connections, the auxiliary charge pumps require a certain time to reach a steady operating point depending on the input voltage amplitude. The threshold voltage of CMOS transistors increases at lower temperatures [139], and thus the settling time of the biasing charge pumps rises considerably at a low ambient temperature of $-40\,^{\circ}\mathrm{C}$. In addition, the biasing circuits of different charge pumps stages, or within the same stage, may experience considerable differences regarding the settling behavior due to the random mismatch of devices, causing transient effects, as illustrated in Fig. 3.28. The settling behavior of the biasing circuits, and thus of the overall RF charge pumps can be improved to a certain extend by inserting MOS-diodes in parallel to the self-biased rectifying transistors of the auxiliary charge pumps (e.g., in parallel to transistor M_{16} in Fig. 3.19a).

3.5 Summary

Analytical considerations and the simulation study provided in this chapter substantiate the relevance of threshold compensation techniques to realize high performance RF charge pumps that achieve a high power conversion efficiency and a low input quality factor. V_{th} compensation methods can be applied in a similar manner for both single-ended and differential charge pump topologies. By investigating simplified charge pump circuits with ideal gate bias sources, I demonstrate that differential charge pump implementations achieve a considerably higher power conversion efficiency than comparable single-ended circuits assuming an equal input quality factor and output power.

I present three differential V_{th} compensated RF charge pumps in a 40 nm CMOS technology. The circuit designs use exclusively high-V_{th} transistors, corresponding to a cost-effective circuit implementation for future HF/UHF dual band smart card ICs. The usage of high-V_{th} transistors in particular poses a challenge for generating the required bias voltages for compensating the V_{th} of the rectifying transistors. The three RF charge pumps include auxiliary charge pumps for the bias voltage generation. The first circuit uses gate biasing for the V_{th} compensation. I introduced a combined gate and bulk biasing approach in the designs of the other two RF charge pumps, extending the V_{th} compensation, to improve the power conversion efficiency.

Measurement results of manufactured prototypes confirm that the enhanced V_{th} compensation results in an increase of the power conversion efficiency over a broad range of input power. At a low DC output power of 4 μW and a V_{DC} of 1 V, the two RF charge pumps using the extended V_{th} compensation reach a high power conversion efficiency of about 42 %, which corresponds to an advantage of more than 3 % in comparison to the charge pump using gate biasing only. All three circuits show an input quality factor of lower than 14 in this operating point. The low quality factor enables a broadband impedance matching between a front-end and a UHF antenna to realize a robust UHF RFID communication link. The comparison to previous works given in Table 3.4 underlines the high performance of the implemented charge pumps.

Furthermore, I demonstrate the operation of two of the RF charge pumps for modulated carrier waveforms and during the start-up at high and low ambient temperatures. The first investigated RF charge pump corresponds to the circuit using gate biasing only, while the second circuit applies the extended V_{th} compensation technique. Both circuits exhibit a sensitivity loss of more than 0.5 dB for modulated carrier waveforms. The comparably slow

response of the bulk biasing circuit of the extended V_{th} compensation to the modulation envelope causes a more pronounced loss, compensating mostly the achieved gain in static efficiency. The measurements of the start-up characteristics moreover reveal considerable delays of the settling of the output voltage of both RF charge pumps at low input powers and a low ambient temperature of $-40\,^{\circ}\mathrm{C}$. The excessive settling time is directly related to the start-up behavior of the auxiliary biasing charge pumps. At the targeted minimum operating input power nevertheless, both circuits show a low settling time of less than 1 ms. The measurement results of the dynamic characteristics of the charge pump circuits for modulated carrier waveforms, but also the start-up behavior strongly emphasize the relevance of considering dynamic effects in simulations. Different design measures to mitigate, for example, the additional efficiency loss induced by modulated carrier waveforms can be assessed by simulation in an early stage of the design process.

4 Overvoltage Protection

The available power at the antenna of a UHF RFID transponder, which is present during operations, ranges from around $-20\,\mathrm{dBm}$ up to more than $20\,\mathrm{dBm}$. UHF RFID transponder ICs incorporate therefore a DC voltage limiter to regulate the output voltage of the RF charge pump and prevent overvoltage conditions at the connected circuitry, as discussed in Sect. 2.2.4. The maximum voltage ratings of the core transistors in scaled CMOS technologies are decreasing approaching values of 1 V or less. At the same time, the threshold voltage cannot be reduced considerably, without causing an undesirable surge in the subthreshold leakage. The supply voltage window thus shrinks, which poses a challenge for the design of an appropriate DC limiter with a low current consumption at the nominal operating voltage of a tag IC. The reduced voltage ratings moreover require an adjustment of the overvoltage protection at the RF terminals of a UHF RFID front-end to mitigate potential reliability risks.

In Ch. 4, I present the design of a temperature compensated DC voltage limiter that allows the regulation of the DC output voltage of an RF charge pump in a narrow range below the maximum voltage rating of 1.2 V for the core devices in the considered 40 nm CMOS technology. In the following, I focus on the overvoltage protection at the RF input terminals of differential UHF RFID front-ends. I investigate the typical behavior of RF charge pumps, ESD protection diodes, and backscatter modulators at high levels of input power. The observed characteristics lead to the conclusion that dedicated RF voltage limiter circuits are required to avert damaging overvoltages at the RF input circuitry, as a consequence of the reduced maximum voltage ratings. I present the designs of two self-biased RF voltage limiters that allow the protection of the input structures of differential front-ends from overvoltage conditions at high levels of available power at a connected UHF antenna.

Stand-alone versions of the DC limiter and the two RF voltage limiters have been manufactured in the considered 40 nm CMOS process. Moreover, the circuits have been integrated with the RF charge pumps presented in Ch. 3, specifically charge pump A and charge pump B, to form two UHF RFID front-ends. Measurement results of the stand-alone circuits, and the two front-ends demonstrate the functionality of the proposed circuit concepts.

Original Publications Related to This Chapter

L. Zöscher, J. Grosinger, U. Muehlmann, H. Watzinger, and W. Bösch, "RF voltage limiters for passive differential UHF RFID front-ends in a 40 nm CMOS technology," in *2015 IEEE MTT-S International Microwave Symposium (IMS)*, Phoenix, AZ, May 2015, pp. 1–4.

L. Zöscher, R. Spreitzer, H. Gross, J. Grosinger, U. Mühlmann, D. Amschl, H. Watzinger, and W. Bösch, "HF/UHF dual band RFID transponders for an information-driven public transportation system," *e & i Elektrotechnik und Informationstechnik*, vol. 133, no. 3, pp. 163–175, June 2016.

L. Zöscher, "Voltage converter," European Patent 2 963 587, March 15, 2017.

L. Zöscher, P. Herkess, J. Grosinger, U. Muehlmann, D. Amschl, and W. Bösch, "Passive differential UHF RFID front-ends in a 40 nm CMOS technology," in *2017 47th European Microwave Conference (EuMC)*, Nuremberg, Germany, Oct. 2017, pp. 105–108.

4.1 Design Specifications

The maximum voltage ratings of the devices that are connected at the output node of the RF charge pump V_{DD} and the RF input terminals RF_1 and RF_2 for the most part determine the target specifications for the DC and the RF voltage limiter circuits of a UHF RFID front-end (see Fig. 2.9).

Table 4.1 summarizes the specifications of the DC voltage limiter presented in this thesis. As shown, the DC limiter has to limit V_{DC} to a value of lower than 1.2 V, assuming that thin-oxide core devices are directly connected at the output of the charge pump (see Fig. 2.6). The RF charge pumps presented in Ch. 3 deliver an output current of around 400 μA at an input voltage amplitude $\hat{V}_{in}$ of 1.1 V and a V_{DC} of 1 V. Considering an additional safety margin, I defined thus a maximum current $I_{DL,max}$ of 600 μA, which the DC limiter has to be able to sink to maintain V_{DC} below 1.2 V. At the same time, the current consumption of the circuit at the nominal supply voltage should be very low to minimize the impact on the sensitivity P_{min} of the transponder IC. The input current I_{DL} of the DC limiter at a V_{DC} of 1 V should be lower than 100 nA. In addition to this, Table 4.1 specifies a minimum value for the buffer capacitance C_B connected at V_{DD} that is primarily relevant with respect to the stability of the DC limiter circuit.

Table 4.2 provides an overview of the most relevant specifications for the RF voltage limiters. The RF limiters should be able to limit the input voltage amplitudes $\hat{V}_{in}$ to a value lower than 1.1 V at an available power P_{av} of 20 dBm, assuming a power source or more specifically an antenna that is matched to the input impedance of the front-end at P_{min}. The RF limiters have to provide therefore an equivalent parallel input resistance $R_{P,L}$ of lower than 200 Ω at a $\hat{V}_{in}$ of 1 V, considering the characteristics of the RF charge pumps presented in Ch. 3. As discussed in Sect. 3.1, the parasitic input capacitance C_{par} of the RF limiters, the ESD protection, and the backscatter modulator increase the quality factor Q, and thus reduce the achievable bandwidth of the impedance match between a front-end and a transponder antenna. The overall parasitic input capacitance C_{par} excluding the charge

Table 4.1: Major design specifications of the DC voltage limiter presented in this work.

Parameter	Specification
V_{DC}	$< 1.2\,V$ @ $I_{DL,max}$
$I_{DL,max}$	600 μA
I_{DL}	$< 100\,nA$ @ $V_{DC} = 1\,V$
C_B	$> 30\,pF$

Table 4.2: Targeted design specifications of the RF voltage limiters.

Parameter	Specification
$\hat{V}_{\text{in}}$	$< 1.1\,\text{V}\ @\ P_{\text{av}} = 20\,\text{dBm}$
$R_{\text{P,L}}$	$< 200\,\Omega\ @\ \hat{V}_{\text{in}} = 1\,\text{V}$
C_{par}	$< 200\,\text{fF}$

pump should be lower than 200 fF in accordance with the specifications of the UHF RFID front-ends, as listed in Table 3.1. The manufactured prototype circuits of the two presented RF voltage limiters indeed incorporate additionally ESD protection diodes and a backscatter modulator.

4.2 DC Voltage Limiter

4.2.1 Operating Principle

Figure 4.1 illustrates the schematic of the DC voltage limiter. The circuit uses a two-stage scheme to sense the voltage V_{DC} at node V_{DD} and to control the limiter current. The operating principle essentially corresponds to the limiter circuit described by Kaiser and Steinhagen in [89]. The PMOS transistor M_{29} is connected in common gate configuration to sense V_{DC}. The gate of M_{29} is biased by the limiter reference voltage V_{DR}. The clipping voltage level of the DC limiter is thus roughly determined by V_{DR} plus the V_{th} of M_{29}. As V_{DC} exceeds the clipping voltage level, the drain-source current of M_{29} rises, and the voltage drop V_{DN} at the resistor R_3 increases, biasing the gate of the NMOS transistor M_{30}. The drain current of M_{30} and thus the limiter current I_{DL} rises in consequence, resulting in a decrease of V_{DC} due to the output resistance of the RF charge pump. As shown in Fig. 4.1, the implemented DC limiter uses thick-oxide I/O transistors. The I/O transistors have a higher intrinsic gain and show a considerably lower leakage than the thin-oxide core transistors in the considered 40 nm CMOS technology, enabling an enhancement of the characteristics of the DC limiter.

The clipping voltage of the DC limiter is subject to process and temperature variations. Process variations can be compensated by trimming. The clipping voltage can be trimmed, for example, by switching separate sections of M_{29} to adjust the effective width of the transistor. By reducing the width of M_{29} the gate-source voltage at M_{29} and the associated level of V_{DC} that is required to turn the output device M_{30} sufficiently on via the voltage drop at R_3 rises.

The temperature variation of the clipping level on the other hand is compensated by using a reference voltage V_{DR} that is proportional to absolute temperature (PTAT). The positive temperature slope of V_{DR} balances the decline of the V_{th} of M_{29} with rising temperature, resulting in a roughly constant clipping level. The PTAT voltage is generated by a stack of NMOS transistors (M_{31-33}) that are biased in the sub-threshold region, following the circuit principle proposed by Vittoz and Neyroud [149]. Two NMOS transistors at a time (e.g., M_{31} and M_{32}) build a PTAT voltage unit stage, as depicted in Fig. 4.2 [149]. By cascading multiple unit stages the required level of V_{DR} can be adjusted, as indicated by the dotted line in Fig 4.1. The implemented DC voltage limiter incorporates overall four cascaded PTAT voltage unit cells for generating a V_{DR} of around 460 mV.

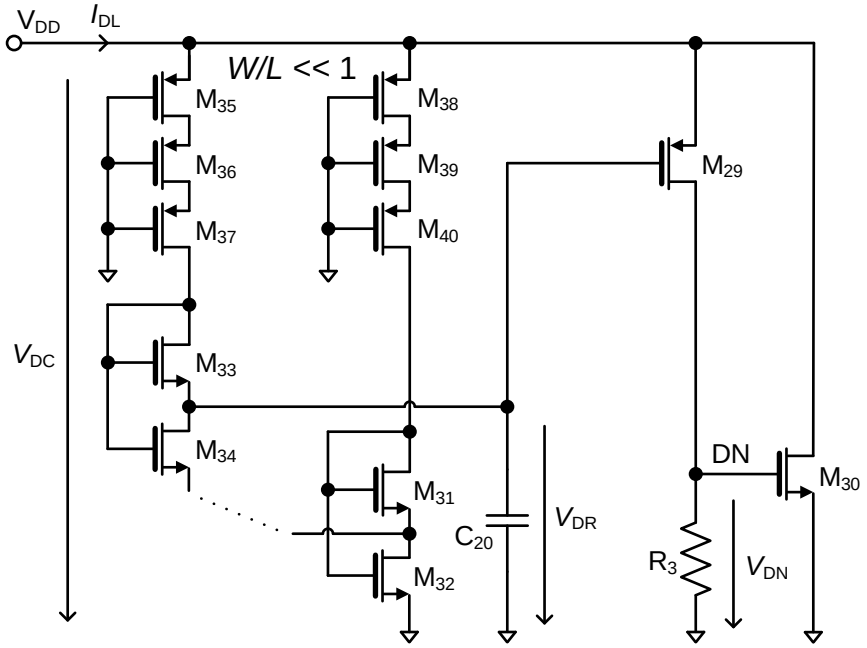


Figure 4.1: Schematic of the DC voltage limiter [146]. The PTAT reference voltage V_{DR} is generated by a cascade of four PTAT voltage unit cells each comprising two stacked NMOS transistors that are operating in the sub-threshold region.

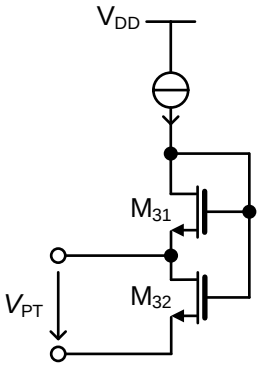


Figure 4.2: Schematic of a PTAT voltage unit cell, as proposed by Vittoz and Neyroud [149]. The temperature slope of V_{PT} can be adjusted by changing the relative W/L ratios and the current ratios of the two stacked NMOS transistors.

In contrast to the original circuit of Vittoz and Neyroud [149], which is shown in Fig. 4.2, the PTAT voltage unit cells in the proposed circuit are each biased by multiple stacked PMOS transistors with a common gate connected to ground (M_{35-40} in Fig 4.1). The chosen W to L ratio of the devices is much lower than one. The PMOS transistors thus behave in effect as large series resistances. Using series resistances for biasing the PTAT voltage unit cells instead of current sources enables a fast and robust start-up of the DC limiter circuit, which is difficult to achieve considering an additionally required bias current generator.

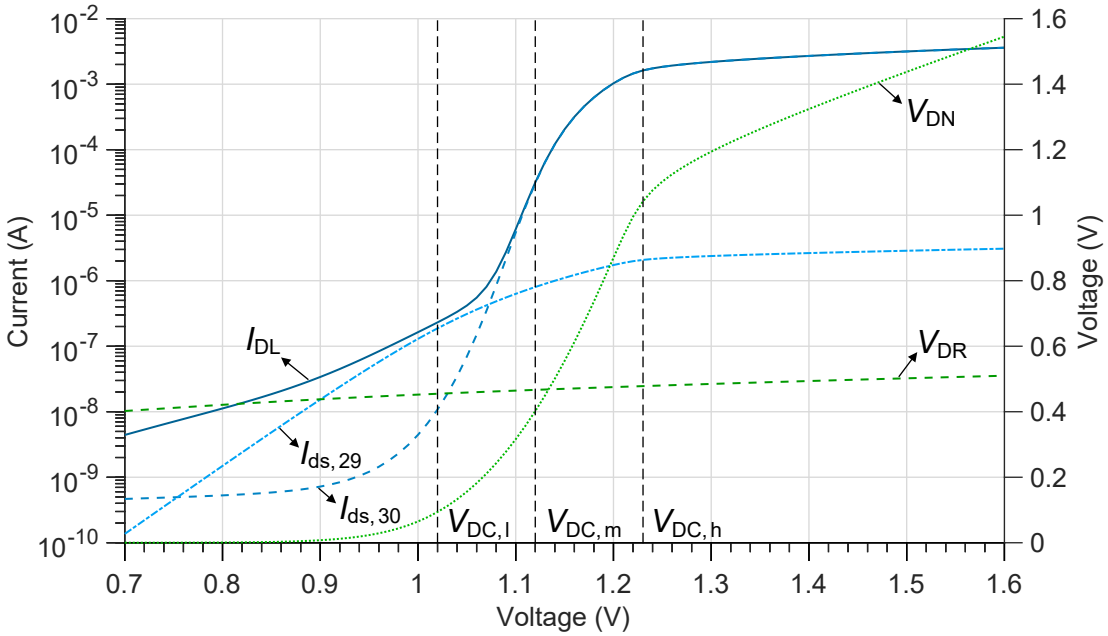


Figure 4.3: Simulation results of the DC characteristics of the DC voltage limiter versus V_{DC}. In addition to the limiter current I_{DL}, the drain-source currents of M_{29} ($I_{ds,29}$), and M_{30} ($I_{ds,30}$), the limiter reference voltage V_{DR}, and the bias voltage V_{DN} are included.

4.2.2 Design Considerations

The DC voltage limiter is entirely self-biased, requiring no static bias currents except for the PTAT voltage generation sub-circuit. The circuit therefore achieves a very low current consumption at voltages below the clipping level. As a consequence however, the bias conditions of the input PMOS transistor M_{29} and the NMOS shunt device M_{30} (see Fig 4.1) vary significantly with changing input voltage level V_{DC} or limiter current I_{DL}, which complicates the circuit design.

DC Characteristics

Figure 4.3 shows the simulated DC characteristic of the limiter current I_{DL} versus V_{DC}. Furthermore included are the drain-source currents of the input transistor M_{29} and the shunt device M_{30}, $I_{ds,29}$ and $I_{ds,30}$, respectively, the limiter reference voltage V_{DR}, and the gate bias voltage V_{DN} of the shunt transistor M_{30}. As indicated, the operating characteristic of the DC voltage limiter can be roughly divided into four different regions depending on the bias conditions.

The voltage level of $V_{DC,1}$ is defined by the reference voltage V_{DR} plus $|V_{th,29}|$,* the threshold voltage of transistor M_{29} ($V_{DC,1} = V_{DR} + |V_{th,29}|$). Therefore, $V_{DC,1}$ approximately equals the clipping voltage of the DC limiter. As shown in Fig. 4.3, the input current of the DC limiter I_{DL} around $V_{DC,1}$ is dominated by the sub-threshold leakage of M_{29}. At a V_{DC} close to $V_{DC,1}$, I_{DL} can thus be estimated considering Eqn. 3.7:

*By definition, the threshold voltage of PMOS enhancement mode transistors has a negative sign. To facilitate the readability, I refer in this work to the absolute value of the threshold voltage $|V_{th}|$ with respect to PMOS transistors.

$$I_{\mathrm{DL}} \approx I_0 \frac{W_{29}}{L_{29}} \mathrm{e}^{(V_{\mathrm{DC}} - V_{\mathrm{DR}} - |V_{\mathrm{th},29}|)/(n_{\mathrm{sub}}\Phi_{\mathrm{t}})}. \tag{4.1}$$

The logarithmic characteristics of I_{DL} flattens for decreasing values of V_{DC} below $V_{\mathrm{DC,l}}$, and becomes increasingly determined by the bias currents of the PTAT voltage source. On the other hand, as V_{DC} rises above $V_{\mathrm{DC,l}}$, the bias voltage V_{DN} at the gate of the NMOS shunt transistor M_{30} increases progressively, and the drain-source current $I_{\mathrm{ds},30}$ surges. The logarithmic characteristic of I_{DL} shows a distinctive knee as $I_{\mathrm{ds},30}$ becomes larger than the drain-source current of the sensing PMOS device $I_{\mathrm{ds},29}$, as depicted in Fig. 4.3. The onset of the strong limiter operation therefore lies at a value of V_{DC} that is slightly above $V_{\mathrm{DC,l}}$ at $V_{\mathrm{DC,l}} + \Delta V_{\mathrm{DC,on}}$. $\Delta V_{\mathrm{DC,on}}$ can be expressed by means of the parameters of the PMOS sensing transistor M_{29}, considering a specific limiter current $I_{\mathrm{DL,on}}$ characterizing a strong limiter operation (e.g., $I_{\mathrm{DL,on}} = 1\,\mu\mathrm{A}$) and an associated gate bias $V_{\mathrm{DN,on}}(I_{\mathrm{DL,on}})$:

$$\Delta V_{\mathrm{DC,on}} = \sqrt{\frac{2V_{\mathrm{DN,on}}L_{29}}{\mu_{\mathrm{p}}C_{\mathrm{ox}}R_3W_{29}}}. \tag{4.2}$$

$\Delta V_{\mathrm{DC,on}}$ equals the gate-source overdrive at M_{29} that is required to cause a voltage drop equal to $V_{\mathrm{DN,on}}$ at R_3 (see Fig. 4.1). Equ. 4.2 expresses $\Delta V_{\mathrm{DC,on}}$ by means of Eqn. 3.5b assuming M_{29} is operating in strong inversion. As can be seen, changing W_{29} or R_3 causes a slight shift of $\Delta V_{\mathrm{DC,on}}$, enabling a fine trimming of $\Delta V_{\mathrm{DC,on}}$.

At an input voltage equal to $V_{\mathrm{DC,m}}$, the bias voltage V_{DN} reaches the threshold voltage of the NMOS shunt transistor M_{30}. M_{30} becomes biased in strong inversion for increasing values of V_{DC} larger than $V_{\mathrm{DC,m}}$, and the logarithmic characteristic of I_{DL} begins to flatten. As V_{DC} approaches $V_{\mathrm{DC,h}}$, the transistor M_{29} is driven into the linear operating region, diminishing the voltage gain of the input stage, eventually. At $V_{\mathrm{DC,h}}$, the gate-source overdrive of M_{29} is exactly equal to the drain-source voltage ($V_{\mathrm{DC}} - V_{\mathrm{DR}} - |V_{\mathrm{th},29}| = V_{\mathrm{DC}} - V_{\mathrm{DN}}$). $V_{\mathrm{DC,h}}$ can thus be expressed as:

$$V_{\mathrm{DC,h}} = \sqrt{\frac{2L_{29}}{\mu_{\mathrm{p}}C_{\mathrm{ox}}R_3W_{29}}(V_{\mathrm{DR}} + |V_{\mathrm{th},29}|)} + V_{\mathrm{DR}} + |V_{\mathrm{th},29}|. \tag{4.3}$$

In a similar way, the limiter current at $V_{\mathrm{DC,h}}$, denoted by $I_{\mathrm{DL,h}}$, can be estimated considering that the overall input current is dominated by the drain-source current of the NMOS shunt transistor M_{30}:

$$I_{\mathrm{DL,h}} = \frac{1}{2}\mu_{\mathrm{n}}C_{\mathrm{ox}}\frac{W_{30}}{L_{30}}(V_{\mathrm{DR}} + |V_{\mathrm{th},29}| - V_{\mathrm{th},30})^2. \tag{4.4}$$

The threshold voltage of the input PMOS transistor M_{29} and the NMOS shunt transistor M_{30} in Fig. 4.1 decline with rising temperature. As noted previously, the proposed circuit uses a PTAT reference voltage to balance the change in V_{th} by an increase of V_{DR} to maintain roughly a constant clipping voltage versus temperature. The output voltage of a single PTAT voltage unit cell V_{PT}, as shown in Fig. 4.2, and its temperature slope are depending on the relative W/L and drain-source current ratios of the two stacked transistors [150]:

$$V_{\mathrm{PT}} = \frac{kT_{\mathrm{K}}}{q} \ln\left(1 + \frac{W_{31} L_{32} I_{\mathrm{ds},32}}{L_{31} W_{32} I_{\mathrm{ds},31}}\right). \tag{4.5}$$

A higher level of V_{DR} can be obtained by cascading multiple PTAT unit cells. As shown in Fig. 4.3, the reference voltage V_{DR} changes slightly with increasing V_{DC} due to the resistive biasing, causing a minor degradation of the limiter performance.

The definition of the appropriate level of V_{DR} and the design of the DC limiter in general is for the most part determined by the considered maximum limiter current $I_{\mathrm{DL,\,max}}$ and the maximum voltage ratings of the used circuit elements in a specific CMOS technology. The DC limiter has to be capable to limit V_{DC} to a value below $V_{\mathrm{DD,\,max}}$ at $I_{\mathrm{DL,\,max}}$ to prevent overvoltage conditions at thin-oxide devices that are connected directly at the output of the RF charge pump. On the other hand, the DC limiter should exhibit a very low current consumption at voltages lower than $V_{\mathrm{DD,\,max}}$, and specifically at $V_{\mathrm{DC,\,min}}$ to minimize the impact on the sensitivity of the transponder IC. The limiter current I_{DL} should therefore cut off rapidly within a narrow range of V_{DC} below $V_{\mathrm{DD,\,max}}$. A sharp cut off can be achieved by assuring that $V_{\mathrm{DC,\,h}}$ (Eqn. 4.3) and correspondingly $I_{\mathrm{DL,\,h}}$ (Eqn. 4.4) are higher than $V_{\mathrm{DD,\,max}}$ and $I_{\mathrm{DL,\,max}}$, respectively. The gate bias voltage $V_{\mathrm{DN,\,max}}$ at the shunt NMOS transistor M_{30} that is required to sink a current of $I_{\mathrm{DL,\,max}}$ can be expressed by means of the transistor parameters:

$$V_{\mathrm{DN,\,max}} = \sqrt{\frac{2 I_{\mathrm{DL,\,max}} L_{30}}{\mu_{\mathrm{n}} C_{\mathrm{ox}} W_{30}}} + V_{\mathrm{th},30}. \tag{4.6}$$

The corresponding gate-source overdrive $\Delta V_{\mathrm{DC,\,max}}$ at the sensing PMOS transistor M_{29} can be estimated by using Eqn. 4.2. Therefore, the limiter reference voltage V_{DR} has to fulfill following condition to maintain a V_{DC} lower than $V_{\mathrm{DD,\,max}}$ at an input current of $I_{\mathrm{DL,\,max}}$:

$$V_{\mathrm{DR}} < V_{\mathrm{DD,\,max}} - |V_{\mathrm{th},29}| - \Delta V_{\mathrm{DC,\,max}} = V_{\mathrm{DD,\,max}} - |V_{\mathrm{th},29}| - \sqrt{\frac{2 V_{\mathrm{DN,\,max}} L_{29}}{\mu_{\mathrm{p}} C_{\mathrm{ox}} R_3 W_{29}}}. \tag{4.7}$$

Equation 4.2 and similarly Eqn. 4.7 indicate that increasing W_{29}/L_{29} enables a reduction of $\Delta V_{\mathrm{DC,\,max}}$, corresponding to a sharper limiter characteristic. Nevertheless, a larger W_{29}/L_{29} of transistor M_{29} leads to an increase of the leakage current at voltage levels close to $V_{\mathrm{DC,1}}$, according to Eqn. 4.1, which can be compensated to some extent by raising V_{DR}.

The minimum DC voltage $V_{\mathrm{DC,\,min}}$ that is required for operating a transponder IC is typically defined by analog circuit blocks, ranging roughly between one and two times V_{th}. As a result of the decreasing maximum voltage ratings in scaled CMOS technologies, the supply voltage window between $V_{\mathrm{DD,\,max}}$ and $V_{\mathrm{DC,\,min}}$ shrinks considering that V_{th} remains mostly constant. The leakage current of the DC limiter at $V_{\mathrm{DC,\,min}}$ becomes therefore more critical with respect to the current consumption of the overall transponder IC.

AC Characteristics

The common-gate connected sensing transistor M_{29} and the shunt transistor M_{30} of the DC limiter, as shown in of the Fig. 4.1, form a two-stage amplifier that potentially may exhibit an

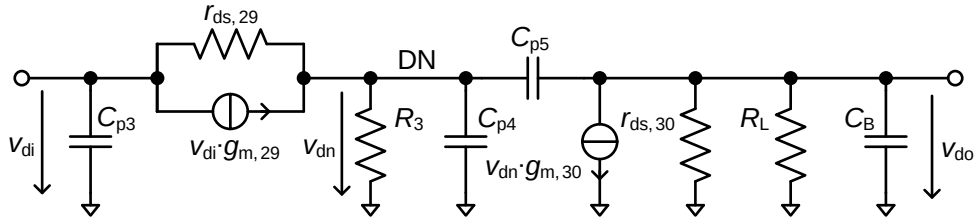


Figure 4.4: Open-loop small-signal model of the DC voltage limiter that is considered for the stability analysis of the circuit.

unstable behavior when operated in a feedback configuration. Additional design constraints have to be considered to achieve a stable limiter response under all operating conditions.

Figure 4.4 shows a small-signal model of the DC limiter in open-loop configuration. The transistors M_{29} and M_{30} are represented by their respective transconductance g_m and small-signal drain-source resistance r_{ds}. C_{p3-5} correspond to parasitic capacitances that are associated with the transistors, the wiring, and the resistor R_3. Figure 4.5 illustrates simulation results of the open-loop frequency response of the implemented DC limiter circuit. The frequency response is characterized by two poles. The buffer capacitance C_B, with typical values of several 100 pF, is significantly larger than the parasitic capacitances C_{p3-5}. Therefore, the dominant pole f_{p1} is defined for the most part by the value of the buffer capacitance C_B, the effective load resistance R_L, and the drain-source resistance $r_{ds,30}$ of transistor M_{30}. Considering the small-signal model depicted in Fig. 4.4, f_{p1} can be approximated as follows:*

$$f_{p1} \approx \frac{1}{2\pi C_B (R_L || r_{ds,30})}. \tag{4.8}$$

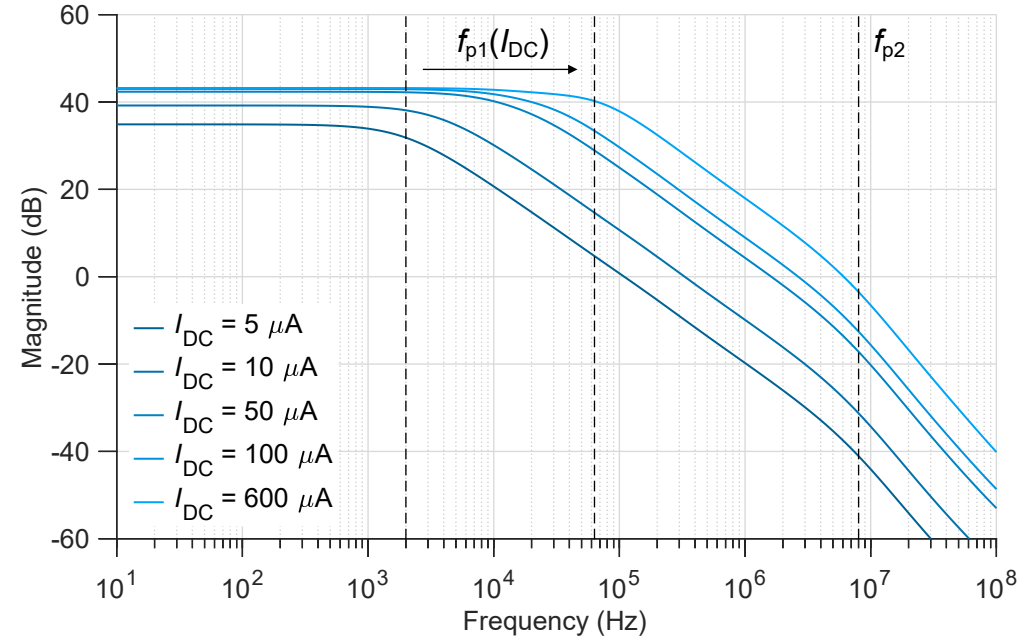
The second pole f_{p2} is mostly determined by the input stage of the DC limiter, and the associated parasitic capacitance at node DN (see Fig. 4.1). Assuming $r_{ds,29} \gg R_3$, f_{p2} can be expressed as:

$$f_{p2} \approx \frac{1}{2\pi C_{p4} R3}. \tag{4.9}$$

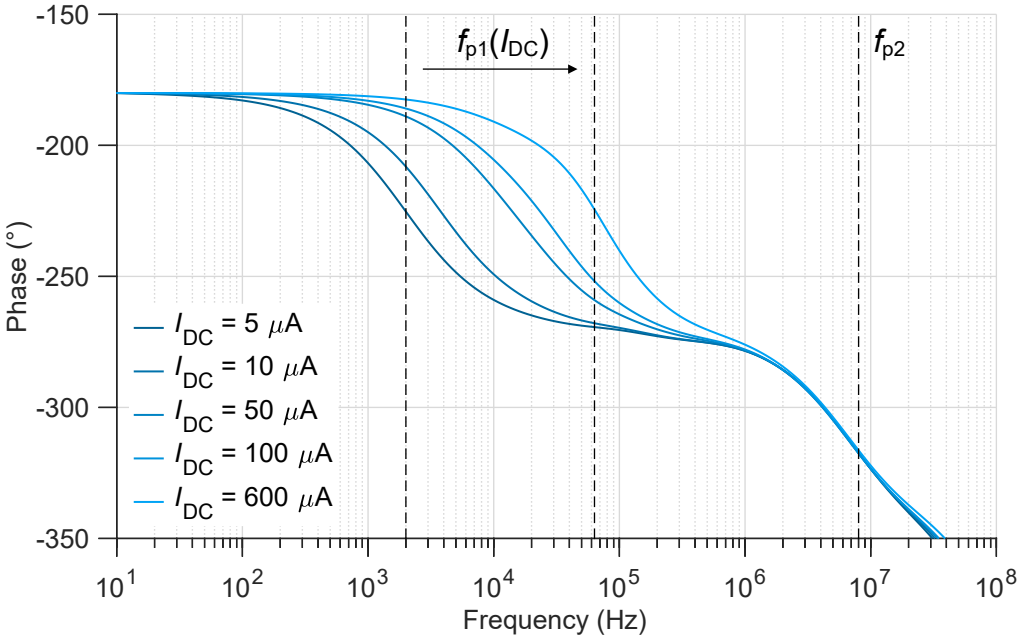
Equation 4.8 and Eqn. 4.9 neglect the influence of the parasitic capacitance C_{p5} that couples the drain of M_{30} to node DN. The gain of the output stage is considerably degraded at frequencies around f_{p2}, assuming that $f_{p2} \gg f_{p1}$. As a result, the Miller effect† and associated with it the influence of C_{p5} on the location of the poles f_{p2} and f_{p1} becomes negligible. Indeed, the pole f_{p2} has to be located at a significantly higher frequency than f_{p1} to achieve an acceptable high phase margin at the unity gain frequency of the open-loop characteristic, and thus to prevent an excessive ringing in the transient step response of the DC limiter, or oscillations as discussed, for example, in [151] in more general terms for feed-back systems.

*The operator $||$, as used in Eqn. 4.8, denotes the resistance value resulting from the parallel connection of the resistances to the left and right side of the operator.

†The Miller effect describes the increase of the equivalent input capacitance of an inverting amplifier stage depending on the gain of the amplifier stage and the capacitance between the input and output node of the amplifier stage (see [151]).



(a) Magnitude response.



(b) Phase response.

Figure 4.5: Simulated open loop frequency response of the DC voltage limiter for varying values of output current I_{DC} delivered by the RF charge pump. A load resistance R_L of 500 kΩ and a buffer capacitance C_B of 300 pF were assumed for the simulations.

Figure 4.5a and Fig. 4.5b show the simulated open-loop magnitude and phase response of the DC limiter, respectively, for varying values of I_{DC}. A load resistance R_L of 500 kΩ and a buffer capacitance C_B of 300 pF were assumed for the simulations. I_{DC} effectively comprises the limiter current I_{DL} and the load current defined by R_L. The location of pole f_{p2} remains mostly stable versus the bias condition of the limiter, as implied by Eqn. 4.9,

noting that the resistance value R_3 is fixed and the parasitic capacitance C_{p4} shows only a weak bias dependency.

f_{p1}, on the other hand, shifts to higher frequencies with an increasing level of I_{DC}, as shown in Fig. 4.5. Therefore, the DC limiter by tendency shows stronger ringing effects at higher levels of I_{DC}, as the difference between f_{p1} and f_{p2} decreases, and associated with it the phase margin. According to Eqn. 4.8, the variation of f_{p1} with changing bias conditions is caused by the drain-source resistance $r_{ds,30}$ of the shunt transistor M_{30}. In a first order approximation, r_{ds} of a CMOS transistor can be assumed to be inversely proportional to the drain-source current of the device [151]:

$$r_{ds} \approx \frac{1}{\lambda_{\Delta L} I_{ds}}. \tag{4.10}$$

Parameter $\lambda_{\Delta L}$ quantifies the channel-length modulation as a function of V_{ds}, which roughly shows an inversely proportional dependency on the channel length of the transistor ($\lambda_{\Delta L} \sim 1/L$) [151]. The minimum value of $r_{ds,30}$, and thus the maximum of f_{p1} is reached at the maximum current $I_{DL,max}$, corresponding to the most critical operating point of the DC limiter with respect to the dynamic behavior of the circuit.

Equation 4.8 and Eqn. 4.9 give additional design guidelines with respect to the sensing resistor R_3 and the output transistor M_{30} (see Fig. 4.1). The load resistor R_L and the buffer capacitance, on the contrary, are typically fixed according to architectural specifications (e.g., the minimum allowed voltage drop during a modulation pulse). Specifically, changing the dimensions of M_{30} can result in an unintended degeneration of the step response of the DC limiter that is caused by the scaling of the parasitic capacitance C_{p4} along with the transistor dimensions. It has to be noted that the considered small-signal model only allows a qualitative description of the dynamic behavior of the DC voltage limiter. The strongly non-linear characteristics of the circuit indeed require careful simulations to capture all transient effects in detail, especially also the start-up behavior.

4.3 RF Voltage Limiters

The individual circuit blocks of a UHF RFID front-end show a decisively different behavior at high levels of input power than for normal operating conditions at power levels around P_{min}. Assessing the overvoltage risk at the antenna interface, and the implementation of appropriate countermeasures to protect the front-end circuits requires to investigate the characteristics of the involved circuit blocks at high power levels.

4.3.1 Characteristics of UHF RFID Front-Ends at High Input Powers

Figure 4.6 shows a simplified model of a UHF RFID transponder that allows the description of the input voltage $\hat{V}_{in}$ at the transponder IC versus a rising level of available power P_{av} at the antenna. The transponder IC is represented by the equivalent parallel input capacitance C_P and the resistance R_P, as discussed in Sect. 1.1.2. The overall input resistance R_P is split into fractions corresponding to the contributions of different circuit blocks of a UHF RFID front-end (see Fig. 2.9). $R_{P,CP}$ and $R_{P,D}$ represent the equivalent parallel input resistances of the RF charge pump and the ESD protection diodes including the backscatter modulator,

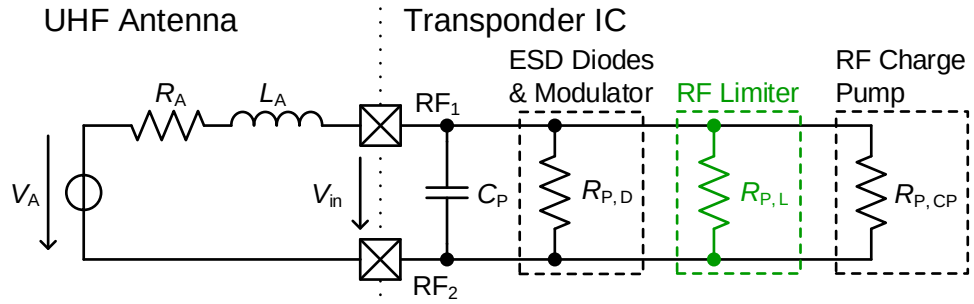


Figure 4.6: Simplified model of a UHF RFID transponder comprising an antenna and a transponder IC. The input resistances of the RF charge pump $R_{\mathrm{P,CP}}$, the ESD diodes including the modulator $R_{\mathrm{P,D}}$, and the RF limiter $R_{\mathrm{P,L}}$ (highlighted in green) determine the overall equivalent parallel input resistance R_{P} of the transponder IC.

respectively. Similarly, the RF limiter is characterized by its equivalent parallel input resistance $R_{\mathrm{P,L}}$. Complementary to this, the antenna resistance R_{A}, the inductance L_{A}, and the voltage source $\hat{V}_{\mathrm{A}}$ model the transponder antenna. The level of $\hat{V}_{\mathrm{A}}$ is depending on R_{A}, and the available power at the antenna P_{av}, assuming an ideal lossless antenna:

$$\hat{V}_{\mathrm{A}} = \sqrt{8 P_{\mathrm{av}} R_{\mathrm{A}}}. \tag{4.11}$$

The antenna impedance $Z_{\mathrm{A}} = R_{\mathrm{A}} + j\omega_0 L_{\mathrm{A}}$ is typically matched to the conjugate complex of the input impedance of the transponder IC at P_{min} ($Z_{\mathrm{A}} = Z_{\mathrm{IC}}^{*}$) to maximize the read range, as discussed in Sect. 1.1.2. Therefore, $\hat{V}_{\mathrm{in}}$ equals roughly $\hat{V}_{\mathrm{A}}/2$ at P_{min}. On the contrary, the transponder IC has to lower R_{P} at high levels of P_{av} to mitigate the rise of $\hat{V}_{\mathrm{in}}$, and thus the risk of overvoltages at the front-end.

RF Charge Pump

At low and moderate levels of input voltage, the input resistance of a UHF RFID front-end is mainly determined by the RF charge pump ($R_{\mathrm{P}} \approx R_{\mathrm{P,CP}}$). Figure 4.7 exemplifies the characteristic of $R_{\mathrm{P,CP}}$ versus $\hat{V}_{\mathrm{in}}$. Shown are measurement results of charge pump A (see Sect. 3.3) and simulation results of a simplified circuit model of an eight-stage RF charge pump. The considered circuit model corresponds to the schematic in Fig. 3.8, using ideal bias sources. A load resistance of 250 kΩ was connected at the output of the charge pumps for the simulations and the measurements. The output voltage V_{DC} was limited to 1 V. Despite the introduced simplifications concerning the gate biasing, the circuit model describes well the behavior of charge pump A with respect to $R_{\mathrm{P,CP}}$.

Figure 4.7 confirms the results from Sect. 3.2 showing a rapid decline of $R_{\mathrm{P,CP}}$ with increasing $\hat{V}_{\mathrm{in}}$ (or alternatively P_{in}) at low voltage amplitudes of around 300 mV. The characteristic flattens and eventually approaches a constant value at higher values of $\hat{V}_{\mathrm{in}}$. By increasing the gate bias levels V_{N} and V_{P} of the charge pump, the knee of the characteristic of $R_{\mathrm{P,CP}}$ is shifted towards lower input voltage amplitudes. The settled value of $R_{\mathrm{P,CP}}$ at high values of $\hat{V}_{\mathrm{in}}$ remains nevertheless equal. In contrast to this, decreasing the capacitance value of the coupling capacitors (C_5 and C_8 in Fig. 3.8) causes a proportional increase of the settled value of $R_{\mathrm{P,CP}}$, confirming Eqn. 3.14.

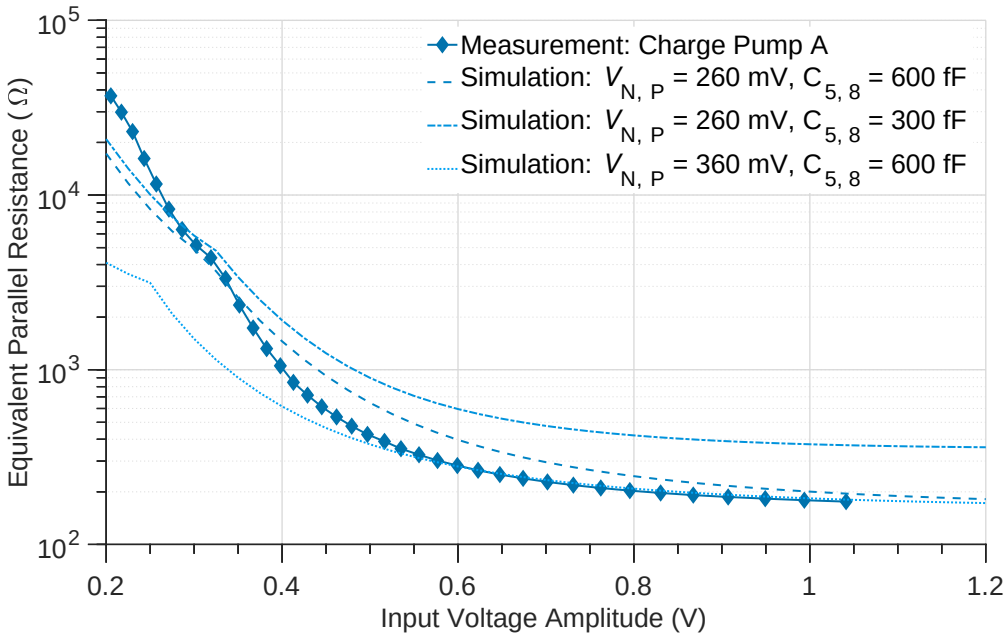


Figure 4.7: Characteristics of the equivalent parallel input resistance $R_{P,CP}$ of RF charge pumps versus the input voltage amplitude. Shown are measurement results of charge pump A that is discussed in Sect. 3.3, and simulation results of a simplified circuit model of an eight-stage RF charge pump corresponding to the circuit in Fig. 3.8.

The sharp decline of $R_{P,CP}$ inherently limits the increase of the input voltage amplitude at a rising available power at the antenna. The minimum value of $R_{P,CP}$ is determined by the dimensions of the coupling capacitors and the number of cascade charge pump stages, as described by Eqn. 3.14. Both parameters are typically optimized with respect to the power conversion efficiency and the quality factor of the RF charge pump. Therefore, these parameters do not allow an adjustment to reduce the settled value of $R_{P,CP}$ further, without causing a performance degradation.

ESD Diodes and Backscatter Modulator

The ESD protection of a differential UHF RFID front-end typically consists of two pairs of anti-parallel diodes, as illustrated in Fig. 2.9b. At low input voltage amplitudes, the diodes pose predominately a capacitive load. The same is true for the backscatter modulator that is mostly implemented using NMOS transistors. The gates of the modulator transistors are connected to ground in the inactive state, and consequently the devices behave as MOS-diodes with respect to the RF input terminals RF_1 and RF_2. I consider therefore the ESD diodes and the backscatter modulator as a single circuit block regarding the analysis of the impedance characteristics at high input power levels, as indicated in Fig 4.6.

As the input voltage amplitude reaches roughly two times the typical forward voltage drop of a p-n junction diode ($\sim 2 \times 0.6\,\mathrm{V}$), the equivalent parallel input resistance of the ESD diodes and the modulator transistors $R_{P,D}$ starts to drop progressively. In anticipation of the experimental results presented in Sect. 4.4, Fig. 4.13 shows the measured equivalent parallel input resistance of a fabricated reference circuit that comprises merely ESD diodes and modulator transistors. It can be seen that the ESD diodes and the modulator transistors

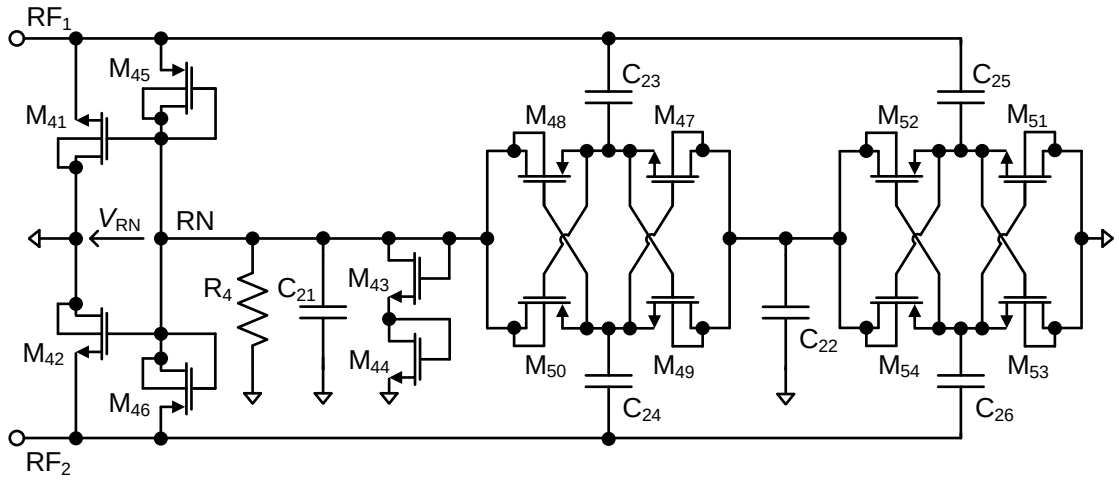


Figure 4.8: Schematic of RF limiter A using NMOS transistors as active load. The fabricated circuit prototypes include additionally ESD diodes and a backscatter modulator (reprinted from [152], ©2015 IEEE).

still show a high input impedance at the targeted maximum input voltage amplitude of 1.1 V, and therefore have only a minor effect with respect to the voltage limitation in this particular case.

4.3.2 Operating Principle and Design Considerations

The introduction of a dedicated RF voltage limiter circuit enables an additional decrease of R_P and thus a suppression of the input voltage amplitude at the front-end at elevated levels of P_av. The two RF voltage limiters presented in this work utilize the same operating principle, but differ with respect to the configuration of the active load transistors. In the following, I refer to the two circuits as RF limiter A and RF limiter B.

Figure 4.8 shows the schematic of RF limiter A. The circuit uses the NMOS transistors M_{41} and M_{42} as an active load, similar to previously proposed circuits [96, 97]. A two-stage auxiliary charge pump consisting of the transistors M_{47-54} and the capacitors C_{23-26} senses the input voltage $\hat{V}_\mathrm{in}$, and generates the bias voltage V_RN for the load device M_{41} and M_{42}. The level of V_RN is controlled by the resistor R_4 and the two diode-connected transistors M_{43} and M_{44}. The time constant associated with R_4 and the capacitor C_{21} determines the dynamic characteristics of the limiter circuit. The MOS-diodes M_{45} and M_{46} provide an additional bypass path to improve the circuit response to fast transients of the RF signal envelope.

The auxiliary charge pump of the RF limiter circuit, as shown in Fig. 4.8, does not include a threshold voltage compensation. Therefore, the bias voltage V_RN remains essentially zero for input voltage amplitudes lower than the V_th of the rectifying transistors M_{47-54}, which equals roughly 500 mV in case of the implemented circuit. The RF charge pumps discussed in Sect. 3.3, on the contrary, are operational already at a $\hat{V}_\mathrm{in}$ of lower than 300 mV due to the applied V_th compensation. The RF limiter shows a high input impedance in this operating region, and has accordingly only a minor impact with respect to the power conversion efficiency of the overall front-end. At higher voltage amplitudes, the auxiliary charge pump

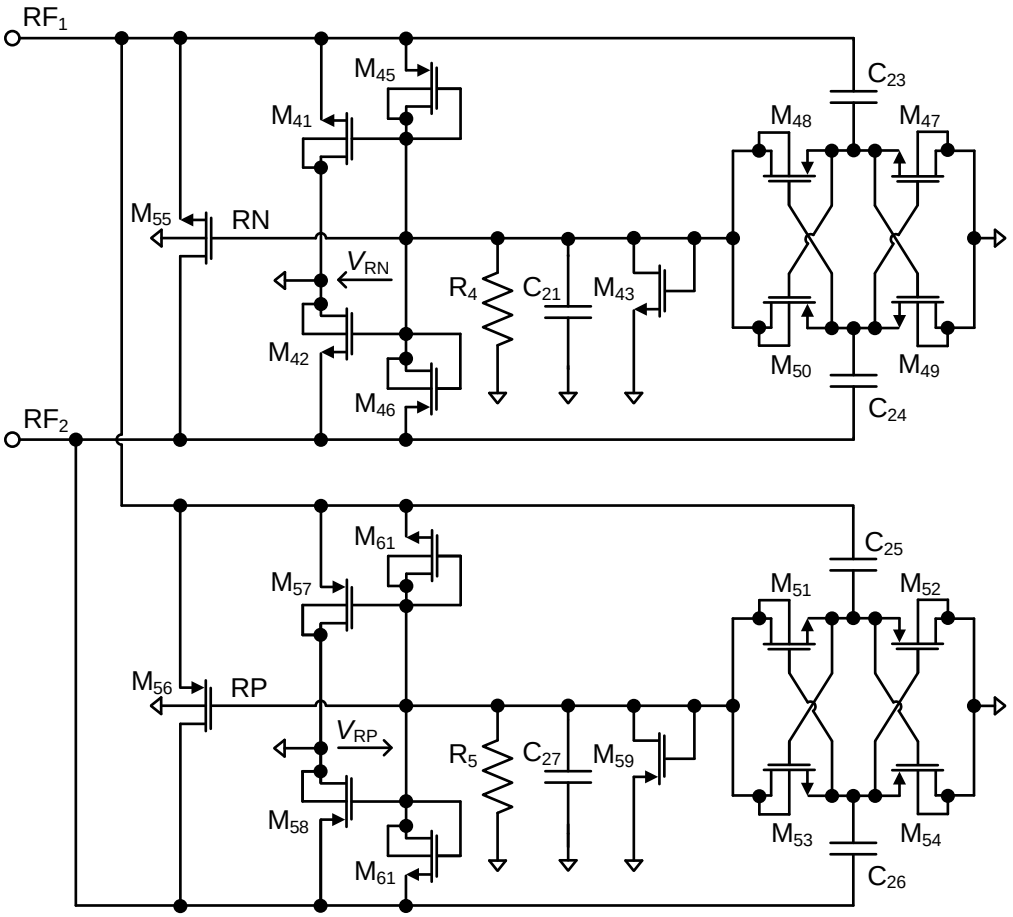
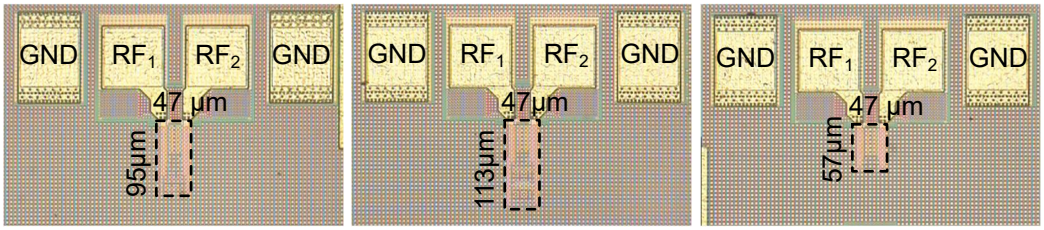


Figure 4.9: Schematic of RF limiter B using NMOS and PMOS transistors as active load [152]. The fabricated circuit prototypes include additionally ESD diodes and a backscatter modulator.

of the RF limiter becomes active, and V_{RN} increases. The equivalent parallel input resistance $R_{\mathrm{P,L}}$ of the RF limiter shows a sharp decline, in consequence.

Figure 4.9 shows the circuit diagram of RF limiter B. This circuit version uses a complementary transistor pair as active load, comprising NMOS transistor M_{55} and PMOS transistor M_{56}. In contrast to RF limiter A, the main active load transistors are connected directly between the RF terminals RF_1 and RF_2. The size of the load transistors could be decreased by about 25 % in comparison to RF limiter A, as a results. Nevertheless, M_{55} and M_{56} pose a potential weak spot regarding the ESD path between RF_1 and RF_2, requiring a careful layout of the connecting metal structures.

The operating principle of RF limiter B is essentially identical to RF limiter A, except that the NMOS and PMOS load transistors require the usage of two complementary bias circuits. The bias voltages V_{RN} and V_{RP} for the NMOS and PMOS load transistors, respectively, are generated by using two single-stage auxiliary charge pumps, as shown in Fig. 4.9. The complementary circuit branches of RF limiter B allow the implementation of an entirely balanced limiter circuit to achieve symmetric signal waveforms at RF_1 and RF_2 with respect to ground. The NMOS transistors M_{41}, M_{42} and the PMOS transistors M_{57}, M_{58} can be used to balance remaining asymmetries of the front-end circuit. Considering single-ended circuit



(a) RF limiter A (b) RF limiter B (c) Reference circuit

Figure 4.10: Die photos of the fabricated RF limiters and a reference circuit including only ESD diodes and modulator transistors. The fabricated prototypes of RF limiter A and RF limiter B incorporate in addition also ESD protection diodes and modulator transistors. (reprinted from [66], ©Springer Verlag Wien 2016).

implementations, achieving a symmetrical signal waveform with reference to the IC ground allows the suppression of even-order harmonic components of the backscattered signal that are caused by the non-linearity of the input circuitry, as described in [153]. In case of the investigated differential circuit implementation, the corresponding harmonic components of the common mode signal at RF_1 and RF_2 are suppressed including the DC component.

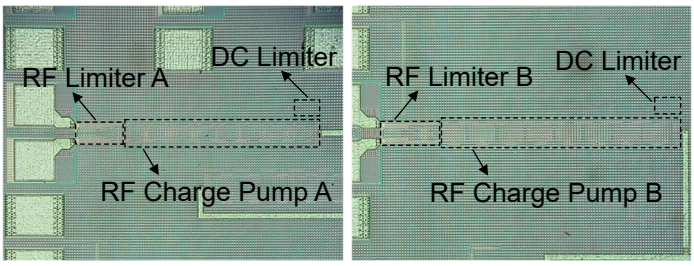
4.4 Experimental Results

4.4.1 Circuit Prototypes

The DC and the RF limiter circuits were fabricated in the considered 40 nm CMOS technology to evaluate the proposed circuit concepts. The fabricated prototypes of RF limiter A and RF limiter B include additionally modulator transistors and ESD protection diodes. A reference circuit consisting only of ESD diodes and modulator transistors allows the assessment of the circuit characteristics without the usage of a dedicated RF limiter, for comparison. As noted in Sect. 3.4.1, the implemented test chip includes moreover two UHF RFID front-ends, integrating the DC limiter, the two RF limiters, ESD diodes, a backscatter modulator, and the RF charge pumps A and B that are discussed in Sect. 3.3. A more detailed description of the fabricated test chip is given in Appendix A.1.

Figure 4.10 shows die photos of the fabricated RF limiters and the reference circuit that comprises only ESD diodes and modulator transistors. The layout area of RF limiter A is approximately 70 % larger than the layout area of the reference circuit. The major contribution regarding the increase in chip area is related to the auxiliary charge pump for the bias generation. In particular, the used metal fringe capacitors for realizing the coupling capacitors (C_{23-26} in Fig. 4.8), and the n-well and isolated p-well structures to isolate the bulks of the rectifying transistors M_{47-54} occupy a significant area. Moreover, resistor R_4 and capacitor C_{21} require a considerable layout area that is comparable to the area of the active load transistors (M_{41} and M_{42} in Fig. 4.8) including the associated wiring overhead.

As shown in Fig. 4.10b, RF limiter B occupies with $113 \times 47\,\mu m^2$ a layout area that is even larger than in case of RF limiter A, despite the decreased size of the active load transistors. The increase in area in comparison to RF limiter A for the most part can be attributed to the additional resistor R_5 and capacitor C_{27} for controlling the gate signal of the PMOS load



(a) Front-end A (b) Front-end B

Figure 4.11: Die photos of the two fabricated UHF RFID front-ends. The implemented front-end prototypes do not include a demodulator. The impact of the demodulator on the power conversion efficiency and the quality factor of a front-end is typically negligible. (reprinted from [146], ©2017 IEEE).

transistors M_{56-58} (see Fig 4.9). Moreover, the separate p-well and n-well structures of the NMOS and PMOS active load transistors cause a significant layout overhead in relation to RF limiter A.

Figure 4.11 shows die photos of the two fabricated front-ends that are denoted by front-end A and front-end B, as described in Sect. 3.4.3. The required layout area of the front-ends in each case is dominated by the RF charge pump. The DC limiter, on the other hand, occupies only a negligible small area. As indicated, front-end A comprises the discussed DC limiter (Fig. 4.1), RF limiter A (Fig. 4.8), and RF charge pump A (Fig. 3.19a) that is described in more detail Sect. 3.3. Complementary to this, front-end B incorporates RF limiter B (Fig. 4.9) and RF charge pump B (Fig. 3.19b), besides the DC limiter.

4.4.2 Static Characteristics

The static characteristics for CW stimuli of the stand-alone RF limiter circuits and the two front-ends were evaluated in the same manner as the implemented RF charge pumps (see Sect. 3.4.2). Therefore, the RF terminals of the circuit prototypes were contacted directly on-chip using a GSSG probe. The input S-parameters were measured by means of a VNA versus the available power. In case of the two front-ends, the DC output power was measured simultaneously for a fixed level of output voltage using an SMU. The test chip moreover includes the DC limiter as a stand-alone circuit block allowing a highly accurate evaluation of the DC characteristics. The I/Os of the stand-alone DC limiter have been bonded to package pins, and were contacted via a test PCB for the measurements. I used an SMU to measure the DC voltage level at the DC limiter versus a rising input current. Appendix A.2 gives a more detailed description of the used test PCB and the measurement setups for evaluating the static circuit characteristics.

DC Limiter

Figure 4.12 shows the measured input voltage of the DC limiter versus the input current I_{DL} at ambient temperatures of $-40\,^{\circ}\mathrm{C}$, $27\,^{\circ}\mathrm{C}$, and $85\,^{\circ}\mathrm{C}$. Furthermore, post-layout simulation results are included for comparison. Simulation and measurement results show in accordance that the DC limiter is able to keep the voltage level within a narrow band of

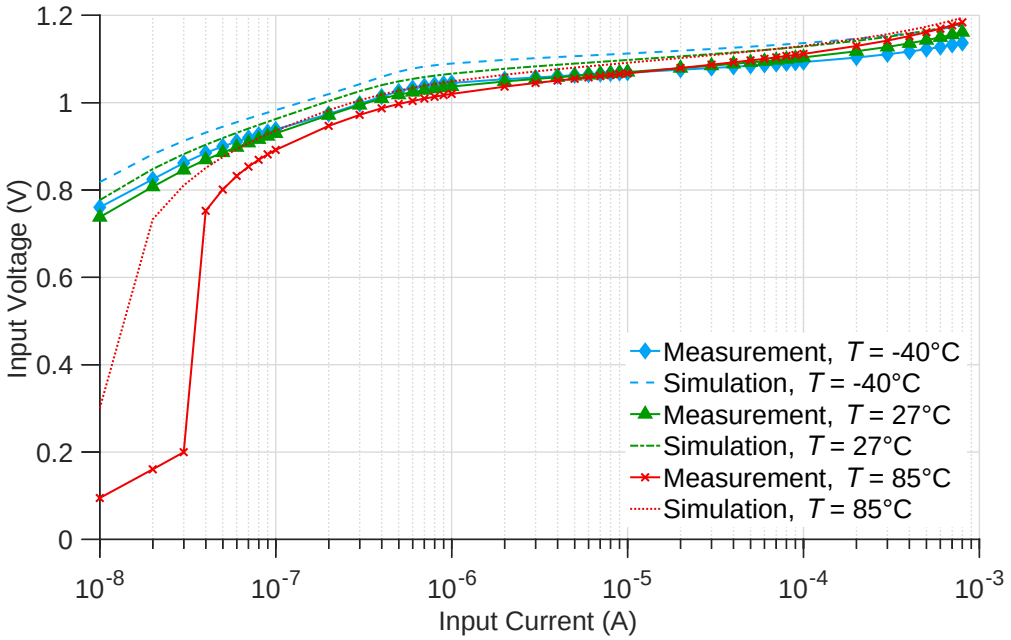


Figure 4.12: Measurement and post-layout simulation results of the input voltage at the DC limiter versus the limiter current I_{DL}. The tested circuit was trimmed at room temperature to limit the voltage to just below 1.2 V at a current level of 800 μA.

roughly 50 mV versus the considered temperature range for an I_{DL} spanning about 100 nA to 800 μA. The tested circuit was trimmed beforehand at room temperature to compensate for process variations. More specifically, the clipping level of the DC limiter was adjusted to limit the voltage level to just below 1.2 V at a current of 800 μA.

The measurement results in Fig. 4.12 show nevertheless a slight negative offset in comparison to simulations, resulting in a decisive increase of the limiter current at the considered nominal operating voltage of 1 V, as specified in Table 4.1. The specification of 100 nA current consumption for the DC limiter can be achieved, including an elevated ambient temperature of 85 °C, by lowering the nominal operating level of V_{DC} to 0.9 V. An operating voltage of 0.9 V corresponds to an increase of the supply voltage window from 0.2 V to 0.3 V with respect to a $V_{\mathrm{DD,max}}$ of 1.2 V. The DC limiter has thus only a minor impact on the sensitivity of a UHF RFID interface assuming an operating voltage of lower than 0.9 V and an overall current consumption of 2 μA for the digital and analog core circuitry.

RF Limiter

Figure 4.13 shows measurement results of the equivalent parallel input resistance of the two fabricated RF limiters and the reference circuit comprising only ESD diodes and modulator transistors. Furthermore, post-layout simulation results are included for comparison. The measurement results are in good agreement with simulations. RF limiter A and RF limiter B exhibit a high input impedance up until an input voltage amplitude $\hat{V}_{\mathrm{in}}$ of around 0.5 V. At this level, the biasing charge pumps of the RF limiter circuits, as shown in Fig. 4.8 and Fig. 4.9, become active, and the equivalent parallel resistance $R_{\mathrm{P,L}}$ drops sharply. $R_{\mathrm{P,L}}$ reaches a value of lower than 200 Ω at a $\hat{V}_{\mathrm{in}}$ of 1 V that is in compliance with the specifica-

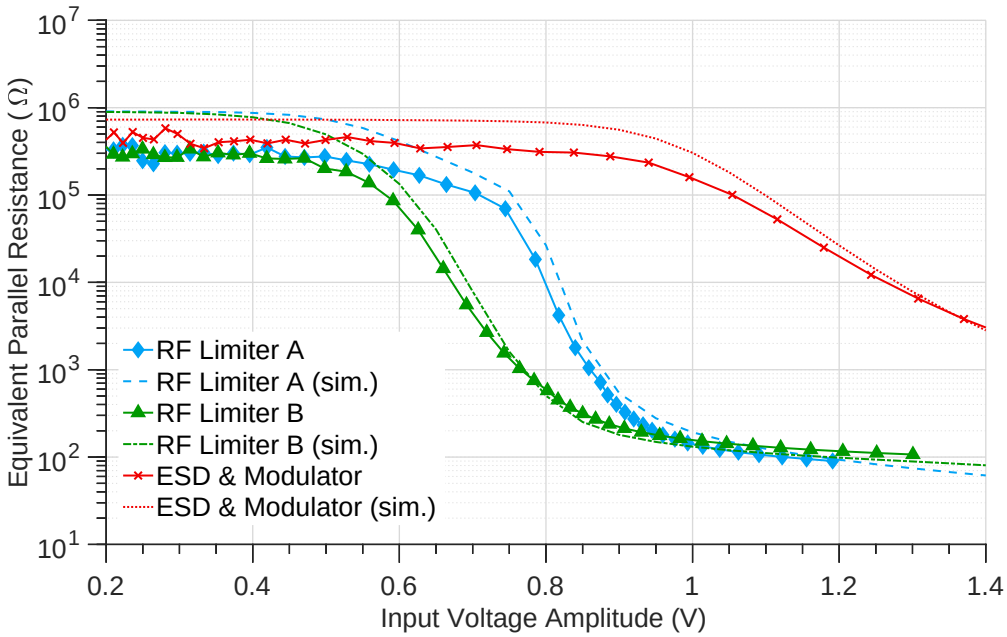


Figure 4.13: Measurement and post-layout simulation (sim.) results of the equivalent parallel input resistance versus $\hat{V}_{\text{in}}$ of the two RF limiters and the reference circuit comprising only ESD diodes and modulator transistors. A carrier frequency of 900 MHz was used for measurements and simulations.

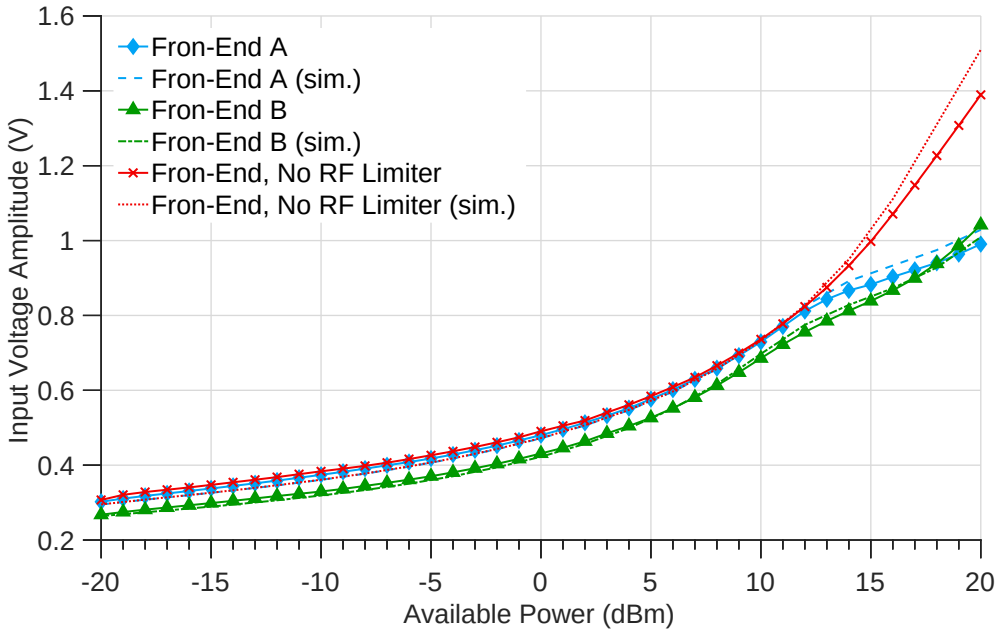


Figure 4.14: Post-processed measurement and post-layout simulation results of the input voltage amplitude versus P_{av} of three UHF RFID front-ends that include RF limiter A, RF limiter B, and the considered reference circuit comprising only ESD diodes and modulator transistors. The source impedance was matched to the input impedance of the front-ends at P_{min} assuming a $P_{\text{DC,min}}$ of 4 μW at $V_{\text{DC}} = 1$ V and $f_0 = 900$ MHz.

Table 4.3: Comparison with previous works.

Reference	Technology	Topology	$V_{DD,\,nom}$	Max. P_{av}
Facen *et al.* [*] **ISLPED 2006 [96]**	180 nm CMOS	differential	1.8 V	8.5 dBm[†]
Balachandran *et al.* TCAS-I 2010 [97]	130 nm CMOS	single-ended	1.8 V	24 dBm
This Work	40 nm CMOS	differential	1.1 V	20 dBm

∗ Simulation results.

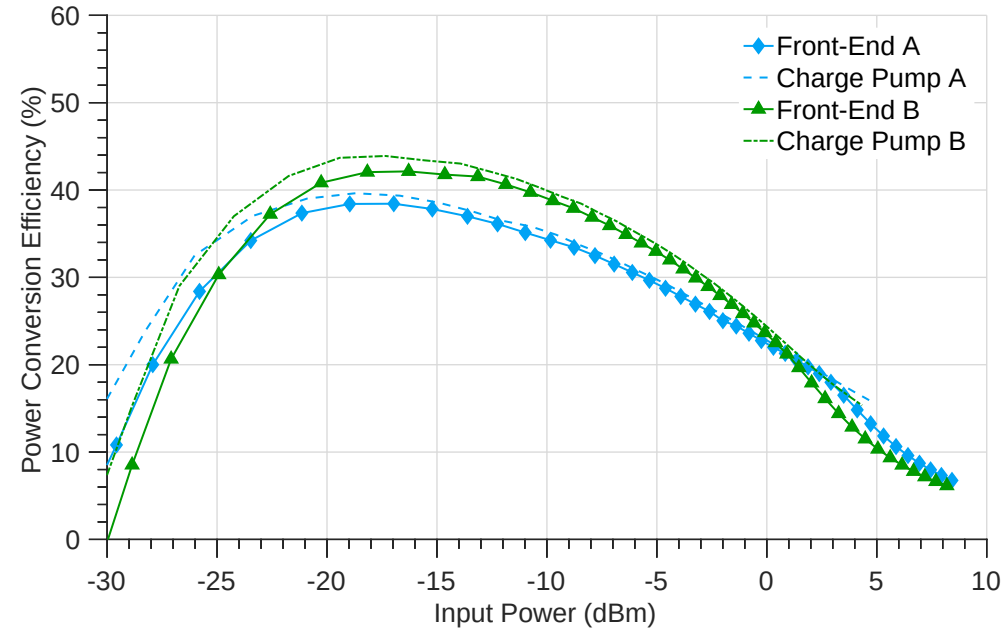
† Estimated value based on published figures.

tions summarized in Table 4.2. The ESD diodes and the backscatter modulator, in contrast, show still a high input impedance at a $\hat{V}_{in}$ of 1 V.

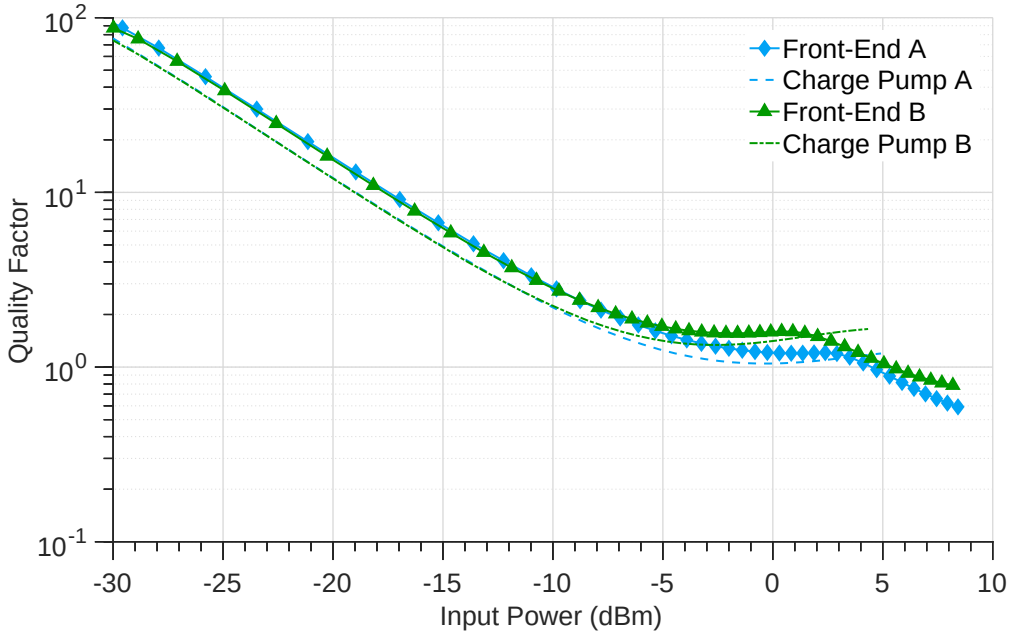
Figure 4.14 shows the characteristics of the input voltage amplitude $\hat{V}_{in}$ at front-end A and front-end B versus the available power P_{av} at a connected antenna. Moreover, the input voltage characteristic of a front-end without RF limiter is included for comparison. $\hat{V}_{in}$ was determined by post-processing the measured S-parameter data of front-end A and front-end B. In case of the front-end without RF limiter, S-parameter measurements of the stand-alone reference circuit consisting of ESD diodes and modulator, and charge pump A were analyzed. I considered the simple source model that is illustrated in Fig. 4.6 for emulating the transponder antenna. The source impedance was matched at a carrier frequency of 900 MHz to the input impedance of the front-ends at P_{min} assuming a $P_{DC,\,min}$ of 4 μW and a V_{DC} equal to 1 V.

As shown in Fig. 4.14, the post-processed measurement results show a good agreement with post-layout simulations. The input voltage amplitude at the front-ends rises only slowly in the region below 0 dBm of available power. The slow rise is directly related to the fast declining equivalent parallel input resistance of the charge pump $R_{P,CP}$ at lower values of $\hat{V}_{in}$, as shown in Fig. 4.7. At a P_{av} larger than 0 dBm, the slope of the input voltage characteristics starts to increase progressively in consequence of the saturation of $R_{P,CP}$. The three front-ends show an almost equal characteristic until a P_{av} of around 12 dBm. At this level, the RF voltage limiters become active. For the front-end without dedicated RF limiter, a $\hat{V}_{in}$ of 1.4 V is observed at a P_{av} of 20 dBm. The RF limiters incorporated in front-end A and front-end B reduce the voltage amplitude at this level of P_{av} to a value lower than 1.1 V that is in compliance with the maximum voltage rating of the thin-oxide devices of the used 40 nm CMOS technology.

Table 4.3 provides a comparison of the two implemented front-ends with previously published UHF RFID front-ends that include a dedicated RF voltage limiter. The nominal supply voltage in the considered 40 nm CMOS technology is 0.7 V lower in comparison to previously used 130 nm or 180 nm process nodes. The proposed RF limiters enable nevertheless a high maximum available power of 20 dBm at a transponder antenna, preventing a performance degradation or hard circuit failures due to overvoltage stress. It has to be noted that the majority of present publications on passive UHF RFID front-ends does not explicitly approach the topic of overvoltage protection at the RF terminals. Furthermore, the impact of voltage limiter structures on the RF performance of UHF RFID front-ends has not been discussed in literature so far.



(a) η versus P_{in}



(b) Q versus P_{in}

Figure 4.15: Comparison of the measured power conversion efficiency η (a) and the quality factor Q (b) of the two implemented UHF RFID front-ends and the corresponding stand-alone RF charge pumps (see Sect. 3.3). The measurements were conducted at a fixed DC output voltage of 1 V and a carrier frequency f_0 of 900 MHz.

Figure 4.15 compares the measurement results of the power conversion efficiency η and the input quality factor Q of front-end A, front-end B, and the corresponding stand-alone RF charge pumps. The RF limiters, besides the ESD protection and the modulator transistors of the front-ends, cause a minor reduction of η at lower values of input power P_{in}. The addi-

Table 4.4: Measurement results of the fabricated front-ends and the stand-alone RF charge pumps for a P_{DC} of 4 μW and 20 μW at a fixed DC voltage V_{DC} of 1 V and $f_0 = 900$ MHz.

Circuit	η	P_{in}	Q	$\hat{V}_{in}$	C_P	R_P	P_{DC}
Front-end A	38.0 %	−19.8 dBm	15.4	310 mV	600 fF	4.5 kΩ	4 μW
	36.3 %	−12.6 dBm	4.3	370 mV	610 fF	1.2 kΩ	20 μW
Front-end B	40.6 %	−20.1 dBm	15.8	270 mV	750 fF	3.8 kΩ	4 μW
	41.3 %	−13.1 dBm	4.6	320 mV	770 fF	1.1 kΩ	20 μW
Charge pump A	40.5 %	−20.0 dBm	11.1	310 mV	420 fF	4.7 kΩ	4 μW
	37.6 %	−12.7 dBm	3.1	370 mV	440 fF	1.3 kΩ	20 μW
Charge pump B	42 %	−20.2 dBm	12.6	270 mV	560 fF	3.9 kΩ	4 μW
	42.1 %	−13.2 dBm	3.6	320 mV	590 fF	1.1 kΩ	20 μW

tional losses are predominately related to the wiring resistances of the circuit structures and the coupling to the substrate, as a result of the increased parasitic capacitance. Moreover, the parasitic capacitances imply a rise of the input quality factor (see Eqn. 3.1) of the two front-ends in comparison to the stand-alone RF charge pumps, as shown in Fig. 4.15b. At a high level of input power of around 2 dBm, front-end A and front-end B exhibit a sudden decrease of Q, resulting from the operation of the RF limiters and the associated decline of R_P.

Table 4.4 summarizes the measurement results of front-end A, front-end B, and the corresponding stand-alone RF charge pumps* for DC output powers of 4 μW and 20 μW. The output voltage was fixed to 1 V for the measurements. The two front-ends show only a slight reduction of maximally 2.5 % with regard to the power conversion efficiency η in comparison to the respective RF charge pumps. On the other hand, the parallel equivalent input capacitance C_P, and consequently the quality factor Q, of the two front-ends are considerably increased relative to the stand-alone RF charge pumps due to the parasitic capacitances of the RF limiter, the ESD protection, and the modulator transistors. The difference regarding C_P between front-end A and RF charge pump A corresponds to 180 fF. In case of front-end B, the increase of C_P equals 190 fF. For comparison, the equivalent parallel input capacitance of the reference circuit consisting only of ESD protection diodes, and modulator transistors amounts to 150 fF. The additional contribution of RF limiter A and RF limiter B to C_P represents therefore roughly 40 fF. The two presented RF voltage limiters have only a marginal impact on the RF performance of the front-ends, in consequence.

As shown in Table 4.4, front-end A and front-end B achieve a high power conversion efficiency of 38 % and 40.6 %, respectively, at the targeted $P_{DC,\,min}$ of 4 μW. Accordingly, the sensitivity value P_{min} of the two implemented front-end circuits equals approximately −20 dBm. The input quality factor of both front-ends at P_{min} is lower than 16, which corresponds to a theoretical maximum bandwidth of 150 MHz for the impedance matching between an antenna and the front-ends according to Eqn. 1.10 assuming $f_0 = 900$ MHz and $\Gamma_m = -10$ dB. Therefore, the two presented front-ends enable the implementation of a highly sensitive and broadband UHF RFID interface, and thus a robust UHF RFID communication link in practical applications.

*The version of RF charge pump A that is integrated in front-end A uses a modified layout for the ground shield of the fringe capacitors in contrast to the circuit discussed in Sect. 3.4.2. The measurement data given in Table 4.4 for RF charge pump A corresponds to the circuit version with the modified ground shield layout.

4.4.3 Dynamic Characteristics

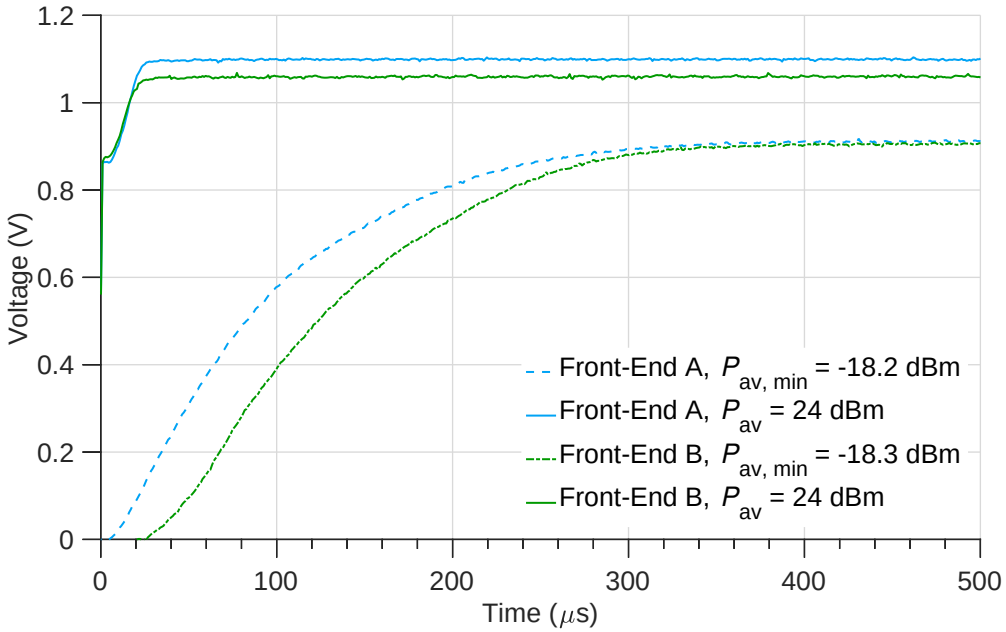
The dynamic behavior of the DC voltage limiter and the two RF limiters was evaluated indirectly by measurements of the two implemented front-end prototypes. As described in Sect. 3.4.3, I used a dedicated test PCB to evaluate the transient behavior of the front-end circuits during the start-up and for modulated carrier waveforms. The test PCB comprises a discrete balun and a discrete matching network to match the input impedance of the differential front-ends to a single-ended 50 Ω interface. Appendix A.3 describes the test PCB and the used measurement setups in more detail.

Figure 4.16 shows measurement results of the transient output voltage $V_{\mathrm{DC}}(t)$ of front-end A and front-end B during the start-up and for modulated carrier waveforms. The shown characteristics correspond to measurements at $P_{\mathrm{av,min}}$ and at a high available power P_{av} of 24 dBm with enabled DC voltage limiter. $P_{\mathrm{av,min}}$ represents the minimum available power at the input of the test PCB that is required to achieve a specific RMS level of V_{DC} at the output of the front-end, as described in Sect. 3.4.3. In this case, $P_{\mathrm{av,min}}$ has been determined for a V_{DC} of 0.9 $\mathrm{V_{RMS}}$ at a load resistance of 500 kΩ, and a carrier frequency f_0 of 900 MHz. A capacitance of 260 pF is connected at the DC output of the front-ends to emulate the buffer capacitance of a tag IC.

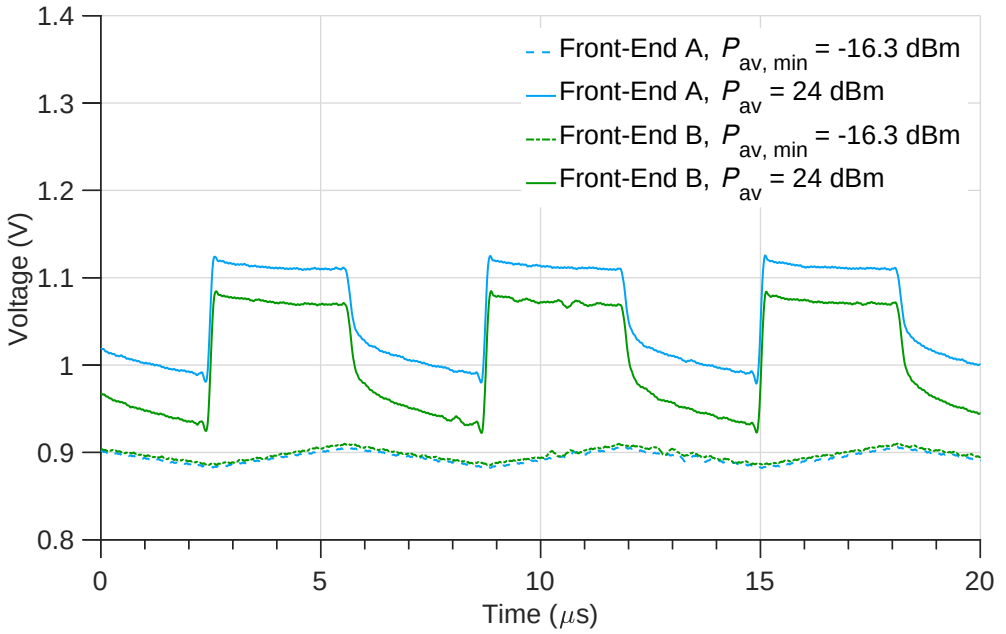
The start-up characteristic of the front-end circuits at $P_{\mathrm{av,min}}$, as shown in Fig. 4.16a, is determined by the RF charge pump, the connected buffer capacitance and the output load. The DC limiter is inactive in this operating region. For the shown measurements, the power was ramped-up with a low rise time of 1 µs. The output voltage nevertheless rises only slowly as the buffer capacitor charges, reaching a stable voltage after around 300 µs to 400 µs. At a high available power of 24 dBm, V_{DC} instantaneously follows the rising available power. The DC limiter exhibits a fast start-up, as can be seen, limiting V_{DC} to below 1.2 V. The DC limiters had been trimmed in advance to compensate process variations, considering an $I_{\mathrm{DL,max}}$ of 800 µA and a $V_{\mathrm{DD,max}}$ equal to 1.2 V. The maximum value of V_{DC} of both front-ends shows nevertheless a comparably large headroom of more than 100 mV with respect to the targeted $V_{\mathrm{DD,max}}$. Reducing the headroom further by a more appropriate trimming would enable a decrease of the leakage current of the DC limiter, mitigating the impact on the sensitivity of the front-ends.

Figure 4.16b shows the transient output voltage $V_{\mathrm{DC}}(t)$ of the two front-ends for an ASK modulated carrier waveform with $m = 100\,\%$. The used modulation waveform has a 50 % duty cycle at a modulation period of 6.25 µs, and exhibits comparably fast signal transition with a rise and fall time of 100 ns. At $P_{\mathrm{av,min}}$, $V_{\mathrm{DC}}(t)$ shows a minor ripple due to the charging and discharging of the buffer capacitor. The transient variation of $V_{\mathrm{DC}}(t)$ becomes more pronounced at a high P_{av} of 24 dBm, as a results of the DC limiter operation. The DC limiter becomes active at the rising edge of the input signal envelope, and provides a bypass path for the excess current. At the falling edge, the circuit returns quickly into a high impedance state. The offset of the $V_{\mathrm{DC}}(t)$ signals between the two front-ends is caused by process variations of the clipping level of the DC limiters. The DC limiter shows a stable transient response with respect to the applied ASK modulated carrier signal for the used buffer capacitance of 260 pF.

The fabricated front-ends were evaluated at low and high ambient temperatures of −40 °C and 85 °C in addition to the measurements at room temperature (27 °C), as presented in Fig. 4.16. Moreover, I investigated the circuit operation for various modulation waveforms including band-limited ASK and PR-ASK signals with different modulation peri-



(a) $V_{\mathrm{DC}}(t)$ during the start-up.



(b) $V_{\mathrm{DC}}(t)$ for a modulated carrier waveform.

Figure 4.16: Measured transient output voltage $V_{\mathrm{DC}}(t)$ of front-end A and front-end B during the start-up (a) and for an ASK modulated carrier waveform (b) at $P_{\mathrm{av,min}}$ and at a high available power of 24 dBm. $P_{\mathrm{av,min}}$ has been determined for an R_{L} of 500 kΩ and a V_{DC} of 0.9 $\mathrm{V_{RMS}}$ at a carrier frequency f_0 of 900 MHz.

ods. The front-end prototypes have shown a stable behavior, given the investigated operating conditions. The observed transient settling phenomena of the RF charge pumps at low temperature are discussed in more detail in Sect. 3.4.3.

4.5 Summary

The decreasing maximum voltage ratings in scaled CMOS technologies augment the risk of overvoltage at the input of UHF RFID front-ends. At the same time, the voltage window for the supply of the core circuitry of transponder ICs shrinks, as the transistor threshold cannot be scaled to lower values. In this chapter, I present a DC voltage limiter that allows the regulation of the core supply voltage of a transponder IC in a narrow range below the maximum voltage rating of the used 40 nm CMOS technology. The proposed circuit is capable to limit the voltage to below 1.2 V at a high input current of 800 μA, while exhibiting a low current consumption of 100 nA at an input voltage of 0.9 V, as demonstrated by measurements of fabricated prototypes. The DC limiter therefore has only a minor impact on the sensitivity of a transponder IC considering a nominal supply voltage of less than 0.9 V. The implemented temperature compensation moreover enables the realization of a stable clipping voltage versus a temperature range from $-40\,^{\circ}$C to $85\,^{\circ}$C.

Furthermore, I introduce two RF voltage limiter circuits to avert damaging overvoltage at the RF terminals of a differential UHF RFID front-end. The RF limiter circuits maintain a high input impedance at input voltage amplitudes of lower than 0.5 V due the implemented self-biasing scheme, and thus have only a minimum impact on the power conversion efficiency of a front-end. At higher voltage amplitudes, the RF limiters become fully biased, exhibiting a steeply declining input impedance. Experimental results of two implemented front-ends show that the RF voltage limiters reduce the input voltage amplitude at the front-ends to a value below 1.1 V at a high available power of 20 dBm. The two RF limiters therefore effectively prevent damaging overvoltages at the front-ends despite the strongly reduced maximum voltage rating in the used CMOS technology relative to previous CMOS processes, as shown in Table 4.3. A comparison between the two front-ends with the corresponding stand-alone RF charge pumps shows that the RF limiters have only a minor impact on the power conversion efficiency and the input quality factor of the implemented UHF RFID front-ends.

5 Summary and Conclusions

The application of contactless smart cards for AFC in public transport has been a key element for the realization of intelligent transportation systems in metropolitan areas. The detailed data on passenger streams and the network utilization allows transport operators to adjust services in a timely manner and to anticipate extensions or changes of the transport network, for example. From the passengers' perspective, the introduction of contactless smart cards has largely improved the user convenience by simplifying the ticketing. The flexibility provided by smart cards enables a seamless change between modes of transport and different transport operators, using different ticketing schemes.

The communication range of the utilized HF RFID technology is limited to about 10 cm. Passengers have to move their contactless smart card in close proximity to an RFID reader device to trigger a transaction, and thus to check-in. In many AFC systems, a second check-out transaction is requried at the point of alighting. The mandatory check-out is nevertheless conceived to be counterintuitive and inconvenient especially by new users in case of buses or trams, for example, that utilize on-board readers. UHF RFID technology enables communication ranges of 10 m and more under optimum conditions. The extended communication range potentially allows a remote detection of passengers, and thus to automatically determine the alighting point in a convenient way without requiring a user interaction. The application of HF/UHF dual band RFID transponders in public transportation, on one hand, enables a remote check-out of passengers using the UHF RFID interface. The HF interface, on the other hand, allows the usage of established security mechanisms to prevent fraud and to safeguard the smart card from being read by unauthorized parties.

HF/UHF Dual Band RFID Transponders for AFC Applications

In Ch. 2, I discuss the operating conditions of HF/UHF dual band RFID transponders in a public transport application scenario, focusing on the UHF RFID interface. The required read range for the UHF RFID link is limited to around 1 m to 3 m, as defined by the arrangement of UHF RFID readers in a vehicle. The achievable read range of a transponder can however decrease severely, depending on its placement and the immediate surrounding. Objects nearby the UHF antenna, such as the human body itself, may cause a considerable reduction of the antenna gain due to absorption and a detuning of the impedance matching between the antenna and the transponder IC. A high performance UHF RFID interface, with a low sensitivity value and a low quality factor, is therefore necessary to compensate for the various impairments of the UHF RFID link encountered in the considered application, and hence to achieve a high reading probability.

The extended communication range provided by the UHF RFID interface may augment already existing concerns regarding the protection of the passengers' privacy, which can

be a critical factor regarding the technology adoption. The security protocol proposed by Gross and Spreitzer in [65, 66] prevents an unauthorized tracking of passengers carrying a HF/UHF dual band smart card. The protocol utilizes a key exchange procedure during the check-in using the HF RFID interface to protect the UHF communication in the following. I outline the architecture of a corresponding HF/UHF dual band smart card IC that provides a shared NVM for exchanging cryptographic keys between the HF and the UHF sub-systems.

The circuit complexity of smart card ICs, especially concerning the digital circuitry, is rising in consequence of the increasing set of features, and the introduction of enhanced security schemes. The expanding circuit complexity fosters the adoption of scaled CMOS technologies. The usage of highly scaled CMOS technologies poses nevertheless a challenge for implementing high performance UHF RFID front-ends, considering especially the stringent requirements with respect to the fabrication cost of smart card ICs. Moreover, the decreasing maximum voltage ratings in smaller CMOS process nodes augment the risk of overvoltage at UHF RFID front-ends during operations, and thus require corresponding countermeasures on circuit level.

RF-DC Power Converters

Chapter 3 discusses general design aspects of single-ended and differential V_{th}-compensated RF-DC power converters or alternatively RF charge pumps. V_{th} compensation techniques consist typically in biasing the gate terminals of the rectifying transistors of an RF charge pump to compensate the effect of the V_{th} of the transistors. The gate biasing reduces the voltage drop at the rectifying transistors, and therefore enhances the power conversion efficiency and lowers the quality factor of an RF charge pump at low input powers. The power conversion efficiency and the quality factor furthermore determine to a large extend the achievable sensitivity and bandwidth of a UHF RFID transponder.

A simulation study of simplified RF charge pumps with ideal gate bias sources and the complementary analytical models show that the applied gate bias voltages are highly critical design parameters with respect to the circuit performance. Too high or too low bias voltages cause a strong degradation in efficiency or the quality factor, irrespective of the used circuit topology. A comparison of the investigated single-ended and differential RF charge pumps reveals a considerable advantage for differential topologies regarding the power conversion efficiency.

I present three V_{th} compensated differential RF charge pumps in a 40 nm CMOS technology. The circuit designs utilize exclusively high-V_{th} transistors that are particularly optimized to reduce the leakage of digital circuit blocks. The technology choice aims at a cost-effective circuit implementation for future HF/UHF dual band transponder ICs. The first RF charge pump is based on an existing design in a previous process node that uses small-scale auxiliary charge pumps to provide gate bias voltages for the V_{th} compensation. I enhanced the V_{th} compensation by introducing a combined gate and bulk biasing scheme in the other two charge pump designs to improve the power conversion efficiency.

Experimental results of fabricated circuit prototypes illustrate the functionality of the proposed circuit concepts. The first RF charge pump that uses only gate biasing reaches an efficiency η of 38.9 % at the targeted output power of 4 μW and an output voltage of 1 V. In comparison to this, the two circuits including the enhanced V_{th} compensation achieve an η of 42 % and 42.7 %, corresponding to an sensitivity value P_{min} of about -20 dBm. The charge pumps exhibit a quality factor of lower than 14 at P_{min}. The three RF charge pumps

therefore enable the implementation of a highly sensitive broadband UHF RFID interface for future HF/UHF dual band transponder ICs.

Overvoltage Protection

The risk of overvoltages at the input structures of UHF RFID front-ends rises with decreasing maximum voltage ratings in scaled CMOS technologies. At the same time, the permitted range of the internal supply voltage of transponder ICs becomes lower, as the transistor V_{th} can hardly be scaled to lower values to maintain acceptable levels of leakage current. The reduced supply voltage window constraints the specifications of the DC voltage limiter that regulates the output voltage of the RF charge pump of a transponder IC versus a rising input power. Chapter 4 discusses circuit implementations of a DC voltage limiter and two RF voltage limiters for UHF RFID front-ends in a 40 nm CMOS technology.

The DC voltage limiter regulates the input voltage level in a narrow range below the maximum supply voltage versus a rising input current, showing a sharply clipping voltage characteristic. The applied two-stage circuit topology allows the regulation of the output voltage of the RF charge pump to below the maximum voltage rating while maintaining a low current consumption at the nominal supply voltage of a transponder IC. A simple PTAT voltage reference is used to compensate the temperature drift of the clipping voltage due to the temperature dependency of transistor parameters. The DC limiter does not require additional bias sources, which enables a fast reaction of the circuit with respect to a rapid ramp-up of the input power at a UHF RFID front-end.

The two RF voltage limiters prevent overvoltage conditions at the antenna terminals of a UHF RFID front-end at high levels of available power at the antenna. The first RF limiter circuit uses NMOS transistors as active load. An auxiliary charge pump without V_{th} compensation senses the input voltage amplitude and generates a positive bias voltage to control the active load transistors. The second circuit includes an NMOS/PMOS complementary active load, applying the same circuit principle to generate corresponding positive and negative control voltages. The usage of uncompensated charge pumps for the bias generation in the RF limiters in combination with an V_{th} compensated main RF charge pump enables a simple regulation of the input voltage amplitude of a front-end. At a low input power, the RF limiters show a high input impedance, and therefore the RF limiters have only a minor impact on the power conversion efficiency of a front-end. At high levels of input power, on the other hand, the biasing charge pumps of the RF limiters become active, and the active load transistors provide a low shunt resistance, limiting the voltage amplitude at the antenna terminals of a UHF RFID front-end.

Prototypes of the stand-alone limiter circuits and two UHF RFID front-ends, which include the DC and the two RF voltage limiters, have been fabricated and evaluated. The measurement results show that the DC and the RF voltage limiters are capable to prevent damaging overvoltages at the RF inputs and the DC outputs of the UHF RFID front-ends at a high available power of 20 dBm at a connected transponder antenna. The DC limiter exhibits a low current consumption of less than 100 nA at a voltage level of 0.9 V over a temperature range from $-40\,^{\circ}\mathrm{C}$ to $85\,^{\circ}\mathrm{C}$. The two UHF RFID front-ends achieve a high power conversion efficiency of 38 % and 40.6 % at the targeted output power of $4\,\mu$W. In this operating point, the front-ends show a low quality factor of less than 16. The proposed DC and RF voltage limiter circuits therefore allow the implementation of a robust UHF RFID

front-end with a high RF performance, suitable for the integration in future HF/UHF dual band transponder ICs for AFC applications.

Outlook

In this thesis, I discuss the design of analog front-ends for HF/UHF dual band RFID transponders for AFC applications in public transportation. Chapter 1 and Ch. 3 touch various aspects ranging from the system architecture to considerations of security and the user acceptance of a corresponding AFC system that include potential for future research in different fields. Furthermore, the implementation of appropriate HF/UHF dual band transponder ICs entails, beside the analog front-ends, additional technical challenges. The implementation of a low-power digital core for handling the communication protocol and providing means for data encryption will be a key factor for achieving a highly sensitive passive UHF RFID interface. The increasing leakage currents in highly scaled CMOS processes might require the introduction of advanced low-power techniques like, for example, the forward and reverse body biasing of digital cells. In the same way, a low-power NVM has to be realized to achieve a low read sensitivity. A corresponding NVM that can be accessed by both the HF and the UHF sub-systems of a dual band transponder IC requires a dedicated power management and additional control logic for the arbitration, in contrast to a standard UHF tag IC.

Besides the application in AFC systems, secure HF/UHF dual band smart cards enable new use cases for UHF RFID technology in different fields such as access control management and electronic ticketing at events. UHF RFID readers can be used to monitor the access to less critical areas within a facility or to detect the presence of people in safety critical zones, for example. Furthermore, the remote detection of people via the provided UHF RFID interface can facilitate the real time monitoring and management of crowds at large events.

A Evaluation of Circuit Prototypes

A.1 Test Chip

The circuits presented in this thesis have been fabricated as part of a test chip in a 40 nm CMOS technology. Figure A.1 shows the top level layout of the test chip. The different prototypes of the discussed circuits are highlighted in blue. Overall, the test chip includes five versions of an RF charge pump, two RF voltage limiters, a DC voltage limiter, and two UHF RFID front-ends. The two RF voltage limiters include ESD protection diodes and a backscatter modulator. The test chip moreover includes for comparison a reference circuit that only consists of ESD protection diodes and a backscatter modulator. Table A.1 presents an overview of the circuit blocks of the test chip, including references to the corresponding circuit schematics.

The schematics of the RF charge pumps denoted by RF charge pump A v.1 and A v.2 are identical. The circuits differ only with respect to the layout of the ground shield below the metal fringe capacitors that are used to implement the coupling capacitors of the RF charge pumps (e.g., C_5 and C_8 in Fig. 3.8). The modified layout of the ground shield of RF charge pump A v.2 results in a minor improvement of the power conversion efficiency of less than 1 %. The same is valid with respect to RF charge pump B v.1 and RF charge pump B v.2. In Sect. 3.4.2, I report measurement results of RF charge pump A v.1 and RF charge pump B v.1.

As shown in Fig. A.1, the RF terminals (e.g., RF_1 and RF_2 in Fig. 3.8) of the RF charge pumps, the two front-ends, and the two RF voltage limiters are accessible by means of GSSG probe pads. The digital control signals of the circuit blocks (e.g., for the backscatter modulators), and the DC outputs of the RF charge pumps (e.g., V_{DD}, CP A v.1) are connected to I/O pads, on the other hand. The I/O ring of the test chip is supplied by 2.5 V. The control signals are operated internally by a voltage of 1.0 V that is provided by a dedicated core supply pad.

The GSSG probe pads are arranged as two lines in parallel to the edges of the test chip, which allow an easy connection of the pads near to the corresponding edge by probes. The digital I/O pads incorporate pull-down resistances, and thus the bonding wires at either the left or right edge of the chip can be removed to facilitate the probing of the circuit blocks. Fig. A.1 shows that the test chip incorporates additionally GSSG probe pads with open and shorted signal terminals. The open and shorted pads allow an estimation of the parasitic capacitance and series resistance of the pad structures. Nevertheless, the measurement results presented in this thesis have not been corrected for the parasitic capacitance and the series resistance of the probe pads.

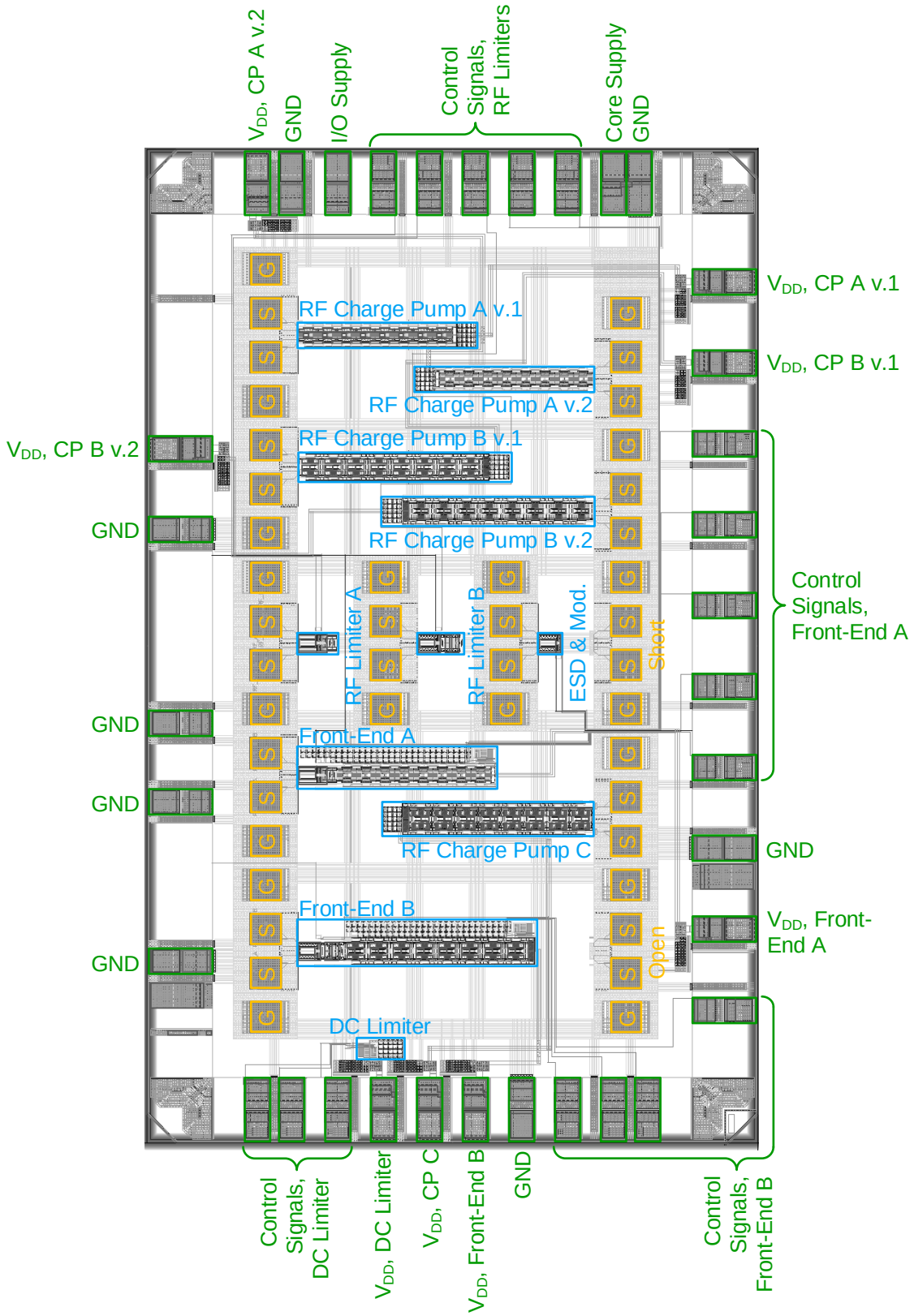


Figure A.1: Top level layout of the fabricated test chip. The GSSG probe pads and the I/O pads of the test chip are highlighted in orange and green, respectively.

Table A.1: Overview of the circuit blocks of the fabricated test chip.

Circuit	Description	Schematic
RF charge pump A v.1	Eight-stage RF charge pump using gate biasing for the V_{th}-compensation.	Fig. 3.8, Fig. 3.19a
RF charge pump A v.2	Circuit version with a modified layout of the ground shield below the used fringe capacitors.	Fig. 3.8, Fig. 3.19a
RF charge pump B v.1	Eight-stage RF charge pump using a combination of gate and bulk biasing for the V_{th}-compensation.	Fig. 3.17, Fig. 3.19b
RF charge pump B v.2	Circuit version with a modified layout of the ground shield below the used fringe capacitors.	Fig. 3.17, Fig. 3.19b
RF charge pump C	Eight-stage RF charge pump using a combination of gate and bulk biasing for the V_{th}-compensation, and extended biasing charge pumps.	Fig. 3.17, Fig. 3.19c
RF limiter A	RF voltage limiter using an NMOS active load. The circuit block includes ESD protection diodes and modulator transistors.	Fig. 4.8
RF limiter B	RF voltage limiter using an NMOS/PMOS active load. The circuit block includes ESD protection diodes and modulator transistors.	Fig. 4.9
ESD & modulator	Reference circuit consisting only of ESD protection diodes and a backscatter modulator.	-
DC limiter	DC voltage limiter with a temperature compensation.	Fig. 4.1
Front-end A	Front-end comprising RF charge pump A v.2, the DC limiter, and RF limiter A. The RF limiter includes ESD protection diodes and a backscatter modulator.	-
Front-end B	Front-end comprising RF charge pump B v.1, the DC limiter, and RF limiter B. The RF limiter includes ESD protection diodes and a backscatter modulator.	-

A.2 Measurements of Static Characteristics

The test chip was packaged in an open-cavity JLCC package for the evaluation of the static characteristics of the circuit prototypes, considering CW stimuli. The RF terminals of the circuits were directly contacted on-chip by means of a GSSG probe for the measurements. I designed a simple evaluation PCB including a socket for JLCC packages and pin headers for contacting the digital control signals of the circuit blocks and the DC outputs of the RF charge pumps. In the following, I refer to this test PCB as evaluation PCB 1.

Figure A.2 shows a photo of evaluation PCB 1. The PCB does not include any vias to allow a mounting of the PCB on the vacuum chuck of a probing station. After removing the cap of the JLCC package, the circuit prototypes at either the right or left edge of the test chip could be contacted by a GSSG probe. Two versions of the bonding diagram were used for the JLCC package variant. Either the left or right edge of the test chip was left unbonded in the two bonding diagrams to allow a probing of the corresponding circuit blocks.

Figure A.3 shows a schematic of the measurement setup that was used to evaluated the characteristics of the RF charge pumps, and the two front-ends for CW stimuli. The RF terminals of the circuits (RF_1 and RF_2 in Fig. 3.8) were contacted using a Dual |Z| Probe from Cascade Microtech [154]. The mixed-mode S-parameters at the RF input of the prototype

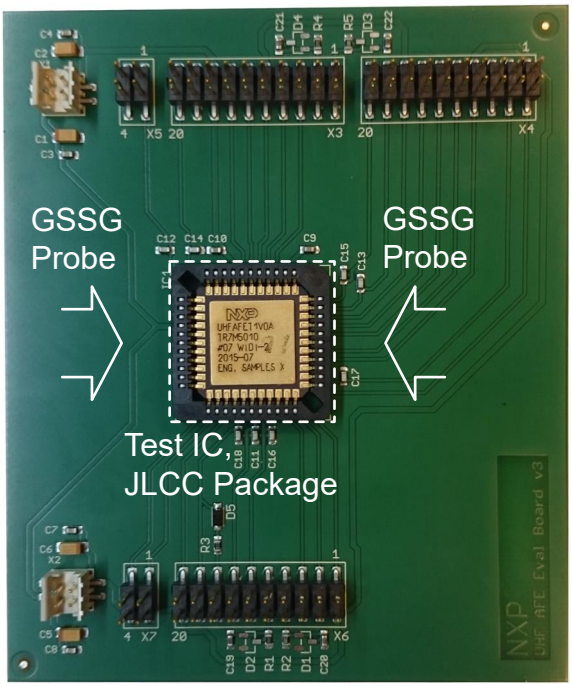


Figure A.2: Photo of evaluation PCB 1, which was used for measuring the static characteristics of the presented circuits.

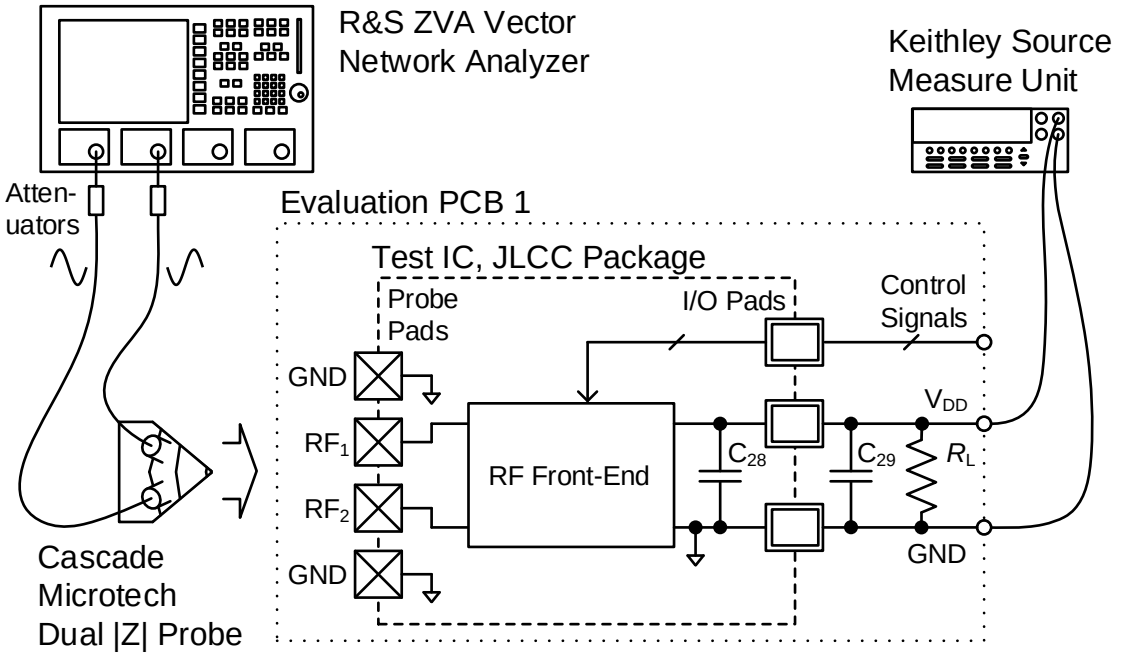


Figure A.3: Schematic of the measurement setup that was used for the evaluation of the static characteristics of the presented circuits for CW stimuli.

circuits were measured versus a rising available power using a Rohde & Schwarz ZVA network analyzer [155]. The VNA was configured to provide a true-differential measurement stimulus. A power calibration was performed for the VNA considering the connectors of the probe as reference plane. Attenuators with an attenuation of 6 dB were connected at the two

measurement ports to improve the effective source matching, and thus to reduce the source power uncertainty. A line-reflect-reflect-match (LRRM) calibration [156] was conducted at the probe tips for the S-parameter measurements, using a dedicated calibration substrate and the calibration software from Cascade Microtech. The insertion loss of the Dual |Z| Probe roughly equals 0.2 dB at a frequency of 900 MHz [154]. The measurement results presented in this work have not been corrected for the insertion loss of the used probe.

As shown in Fig. A.3, an additional buffer capacitance C_{29} is connected on the evaluation PCB to the outputs of the RF charge pumps and the front-ends in addition to a limited on-chip capacitance C_{28}. A buffer capacitance of approximately 230 pF and 260 pF is connected to the outputs of the RF charge pumps and the front-ends, respectively. The DC output power of the RF charge pumps and the two front-ends was measured for a constant load resistances R_L and for a fixed output voltage V_{DC}. A SMU from Keithley Instruments was used to measure the output voltage and current [157] simultaneously to the S-parameter measurement at the input. The SMU was configured to allow a maximum output voltage of 1.2 V for the measurements with fixed R_L. Therefore, the SMU emulated a DC voltage limiter of a UHF RFID front-end.

The input power P_{in} of the RF charge pumps and the front-ends was calculated from the available power P_{av} that was delivered by the VNA at the input of the GSSG probe and the measured mixed-mode S-parameters:

$$P_{in} = P_{av}\left(1 - |S_{dd11}|^2 - |S_{cd11}|^2\right). \tag{A.1}$$

S_{dd11} in Eqn. A.1 describes the differential to differential-mode S-parameter of the mixed-mode port number 1, and S_{cd11} equals the corresponding differential to common-mode S-parameter. The input RF terminals of a differential RF front-end constitute a single mixed-mode S-parameter port that requires nevertheless two single-ended ports of a VNA for a characterization. The measurements show that S_{cd11} can be neglected due to the highly symmetric characteristic of the investigated circuits. The simultaneous measurement of the DC output power P_{DC} enabled the evaluation of the power conversion efficiency η of the RF charge pumps and the front-ends.

The input voltage amplitude at the front-ends $\hat{V}_{in}$ was estimated in a similar way, considering P_{av} and the measured S_{dd11}:

$$\hat{V}_{in} = \left|\sqrt{4P_{av}Z_0}(S_{dd11} + 1)\right|. \tag{A.2}$$

The parameter Z_0 in Eqn. A.2 corresponds to the characteristic impedance of the used cables and the measurement equipment ($Z_0 = 50\,\Omega$). The input impedance of the front-ends Z_{IC} was calculated from S_{dd11} and Z_0:

$$Z_{IC} = 2Z_0\frac{1 + S_{dd11}}{1 - S_{dd11}}. \tag{A.3}$$

The equivalent series input resistance R_S and the equivalent series capacitance C_S of the RF charge pumps and the front-ends can be calculated from the real and imaginary part of Z_{IC}:

$$R_S = \mathrm{Re}\{Z_{IC}\}, \tag{A.4}$$

$$C_S = \frac{1}{2\pi f_0 \mathrm{Im}\{Z_{IC}\}}. \tag{A.5}$$

Moreover, the input quality factor Q can be directly derived from Z_{IC}:

$$Q = \frac{\mathrm{Im}\{Z_{IC}\}}{\mathrm{Re}\{Z_{IC}\}}. \tag{A.6}$$

The equivalent parallel input resistance R_P and the equivalent parallel input capacitance C_P of the front-ends and the RF charge pumps were determined considering R_S, C_S and Q:

$$R_P = R_S\left(Q^2 + 1\right), \tag{A.7}$$

$$C_P = C_S \frac{Q^2}{Q^2 + 1}. \tag{A.8}$$

The two RF voltage limiters and the reference circuit that only comprises ESD protection diodes and modulator transistors were evaluated in a similar way, as the RF charge pumps and the two front-ends (see Fig. A.3). In this case, no additional measurements of DC voltage and DC current were necessary. In order to evaluate the static characteristics of the DC limiter, I used an SMU to vary the input current of the circuit and to simultaneously measure the input voltage.

Overall, five samples of each circuit block have been evaluated with respect to the static circuit characteristics. The measurement results have in general shown a good compliance between the different samples. The results reported in this thesis roughly correspond to the median of the investigated samples in case of each individual circuit block.

A.3 Measurements of Dynamic Characteristics

The test chip was assembled in a HVQFN package to evaluate the characteristics of the two UHF RFID front-ends for modulated carrier waveforms and the start-up behavior. The RF terminals of the two front-ends have been bonded to package pins, using the available probe pads. Two different versions of the bonding diagram were used for the HVQFN package variant. The two bonding versions are identical with respect to the pin-out, except for the RF terminals of the front-ends. Only the two RF terminals of front-end A or front-end B are bonded using the same package pins in each case.

I designed an evaluation PCB comprising a discrete matching network and a discrete balun, which enable the connection of the front-end circuits to standard single-ended measurement equipment. I refer to this second evaluation PCB as evaluation PCB 2. Figure A.4 shows a photo of evaluation PCB 2. The PCB was originally designed for measurements using a thermostream to control the ambient temperature of the test chip. Nevertheless, the measurements were conducted using a climate cabinet for the temperature control.

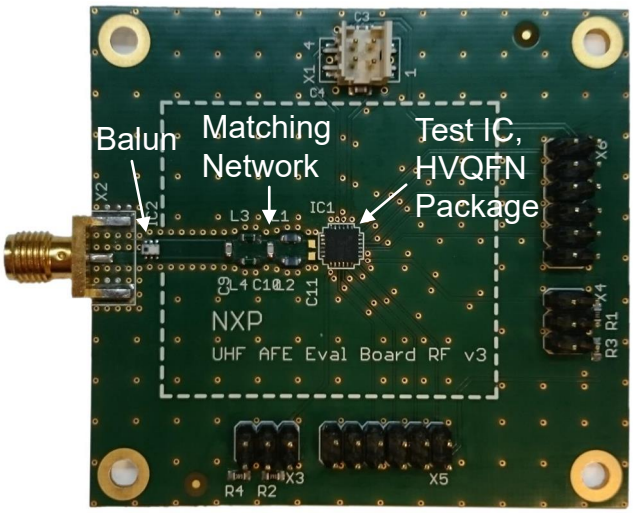


Figure A.4: Photo of evaluation PCB 2 that was used for measuring the dynamic characteristics of the two presented UHF RFID front-ends.

The balun of evaluation PCB 2 converts the unbalanced signal that is fed via the subminiature version A (SMA) connector to a balanced signal. I have used a HHM1564A4 multilayer balun from TDK that shows reasonable constant characteristics, and specifically a good amplitude and phase balance in the frequency range from 860 MHz to 960 MHz [158]. A two section L-matching network matches the 200 Ω differential impedance at the secondary side of the balun to the input impedance of the front-ends at the estimated value of P_{min} for a $P_{\mathrm{DC,\,min}}$ of 4 μW and a V_{DC} of 1 V. The matching network has been designed to achieve a broad bandwidth that covers roughly 860 MHz to 960 MHz, corresponding to the operating conditions of a typical UHF RFID transponder. The network has been specifically adapted to the different characteristics of the two front-ends in each case. Simulations of the evaluation PCB using S-parameter models for the balun and the components of the matching network revealed an insertion loss of roughly 3.5 dB to 4 dB from the SMA connector to the interfacing pins of the front-ends. This value of insertion loss is in line with the measurement results of the RF charge pumps and the front-ends for CW stimuli, as discussed in Sect. 3.4.2 and Sect. 3.4.3.

Figure A.5 shows a schematic of the measurement setup that was used to evaluate the dynamic behavior of the front-ends. The modulation and the start-up waveforms were generated using a N5182B MXG signal generator from Keysight Technologies that incorporates an arbitrary waveform generator [159]. The measurement results were corrected for the losses of the cable connecting the evaluation PCB to the measurement equipment. An additional buffer capacitance C_{29} is connected on the PCB to the output of the front-ends. Considering the on-chip capacitance C_{28}, an overall buffer capacitance of about 260 pF is connected to the output of the front-ends, which corresponds to a typical value of buffer capacitance of a UHF RFID transponder IC. The load resistance R_{L}, which is connected to the output of the front-ends, can be configured via pin-headers. The measurements were conducted for a load resistance of 50 kΩ, 250 kΩ, and 500 kΩ. The DC output voltage of the front-ends was captured using an oscilloscope from Keysight Technologies.

The start-up behavior of the front-ends was evaluated for an input signal with a fast rise time of 1 μs, and a second signal with a slow rise time equal to 500 μs that conform to the

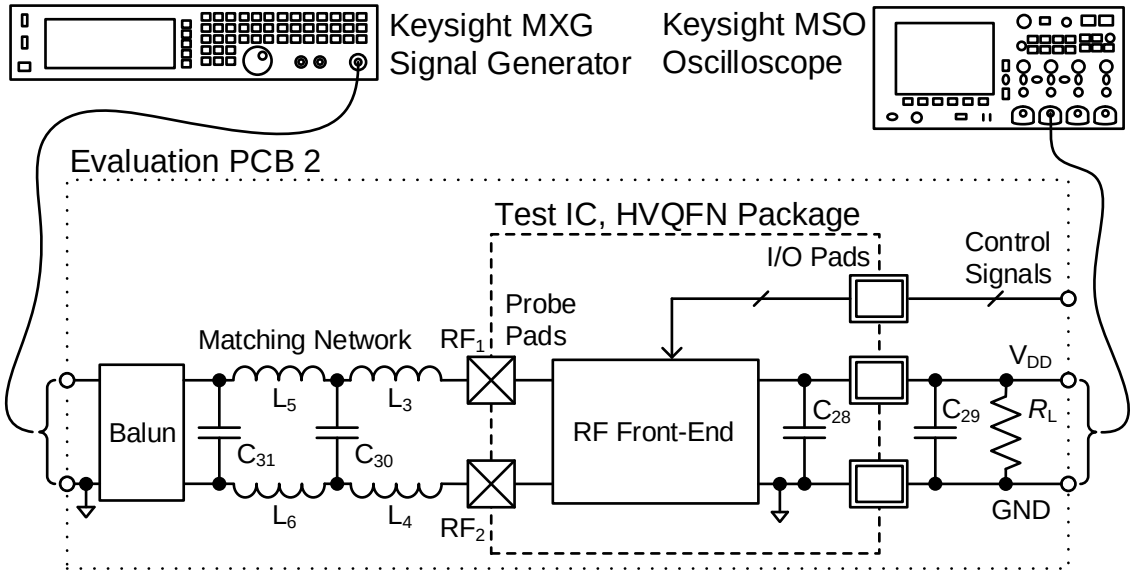


Figure A.5: Schematic of the measurement setup that was used for the evaluation of the dynamic characteristics of the two presented UHF RFID front-ends.

Table A.2: Overview of the modulation waveforms that were used for the evaluation of the two UHF RFID front-ends.

Modulation Waveform	T_{per}	T_{m}	m	T
ASK, $T_{\mathrm{r}} = T_{\mathrm{f}} = 100\,\mathrm{ns}$	$6.25\,\mu\mathrm{s}, 25\,\mu\mathrm{s}$	$0.5T_{\mathrm{per}}$	100 %	$-40\,^{\circ}\mathrm{C}$, $27\,^{\circ}\mathrm{C}$, $85\,^{\circ}\mathrm{C}$
ASK, $T_{\mathrm{r}} = T_{\mathrm{f}} = 10\,\mathrm{ns}$	$1.56\,\mu\mathrm{s}$	$0.5T_{\mathrm{per}}$	100 %	$-40\,^{\circ}\mathrm{C}$, $27\,^{\circ}\mathrm{C}$, $85\,^{\circ}\mathrm{C}$
ASK, multiple-interrogator environments [50]	$6.25\,\mu\mathrm{s}, 25\,\mu\mathrm{s}$	$0.4T_{\mathrm{per}}$	100 %	$-40\,^{\circ}\mathrm{C}$, $27\,^{\circ}\mathrm{C}$, $85\,^{\circ}\mathrm{C}$
ASK, multiple-interrogator environments [50]	$6.25\,\mu\mathrm{s}, 25\,\mu\mathrm{s}$	$0.5T_{\mathrm{per}}$	100 %	$-40\,^{\circ}\mathrm{C}$, $27\,^{\circ}\mathrm{C}$, $85\,^{\circ}\mathrm{C}$
PR-ASK, multiple-interrogator environments [50]	$6.25\,\mu\mathrm{s}, 25\,\mu\mathrm{s}$	-	-	$-40\,^{\circ}\mathrm{C}$, $27\,^{\circ}\mathrm{C}$, $85\,^{\circ}\mathrm{C}$

EPC Generation-2 UHF RFID standard [50]. The peak level of available power of the signals at the input of the evaluation PCB was varied from $-20\,\mathrm{dBm}$ to a high value of $24\,\mathrm{dBm}$. The start-up characteristics was evaluated for ambient temperatures of $-40\,^{\circ}\mathrm{C}$, $27\,^{\circ}\mathrm{C}$, and $85\,^{\circ}\mathrm{C}$.

Table A.2 provides an overview of the modulation waveforms that were used for the evaluation of the two UHF RFID front-ends. A periodic signal with a constant modulation period T_{per} was applied for each modulation waveform. The minimum required available power $P_{\mathrm{av,\,min}}$ to achieve a specific RMS value of the output voltage V_{DC} was determined by stepwise increasing P_{av} of the signal generator. Additionally, measurements with a fixed high available power of 24 dBm were conducted. The ASK modulated waveforms with a fast rise time T_{r} and fall time T_{f} of 100 ns and 10 ns do not represent practical reader signals, but rather correspond to the operating conditions during the backscatter modulation of a transponder. The remaining ASK and PR-ASK waveforms have been aligned with the spectral mask requirements for multiple-interrogator environments as specified in the EPC Generation-2 UHF RFID standard [50].

All in all, four samples of front-end A and five samples of front-end B have been evaluated with respect to the dynamic circuit characteristics. Measurements of different samples have overall shown good compliance. The results as reported in this work correspond only to a representative subset of the conducted measurements to outline the functionality of the proposed circuit concepts.

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