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A Switched Capacitor DC-DC Converter for an Integrated Power Management System

MASTER'S THESIS

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AFFIDAVIT

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Acknowledgement

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Kurzfassung

Diese Masterarbeit beschäftigt sich mit der Theorie und Implementierung eines integrierten kapazitiven geschalteten DC-DC Wandlers in einem 130nm FLASH Prozess. Es werden theoretische Aspekte der Energiewandlung in kapazitiven als auch induktiven Schaltvorgängen erläutert und Vorteile bzw. Nachteile aufgezeigt. Insbesondere wird auf die zur Verfügung stehenden Optionen der Spannungswandlung in integrierten Schaltungen näher eingegangen. Prinzipielle Überlegungen zum Konzept und Design des Wandlers werden gegeben und anschließend anhand von Simulationen analysiert. Der Konverter ist für einen Eingangsspannungsbereich von 3.6V-1.6V vorgesehen, der am Ausgang eine Spannung von 1.4V-1.6V erzeugt und eine Last von 1mA-6mA treiben kann. Um auf schnelle Belastungsänderungen im Bereich von ca. 300μA/ns reagieren zu können, wird der Wandler mit einer Taktfrequenz von 33MHz betrieben und ein diskretes Puls-Frequenz-Modulationsverfahren angewandt. Es werden lediglich ein Stützkondensator am Ausgang mit 100nF und eine gesamte Chipfläche inklusive integrierter Kapazitäten von $0.275mm^2$ benötigt. Dabei erzielt der Konverter eine maximale Energieeffizienz von 75%.

Abstract

The topic of this master thesis is the theory and implementation of a integrated switched capacitor DC-DC converter in a standard 130nm FLASH process. Theoretical aspects of the a capacitive and inductive energy conversion process are surveyed and advantages and disadvantages are mentioned. Especially, available on-chip methods to convert voltages are investigated. Basic considerations regarding the concept and design of the converter are given and simulation results are analysed. The converters input voltage range is between 3.6V-1.6V, while delivering a 1.4V-1.6V voltage at the output under a load of 1mA-6mA. To react accordingly to fast loading condition changes in the range of 300μA/ns the converter is operated at a clock frequency of 33MHz and a pulse-frequency-modulation scheme is applied. The converter needs a single external output capacitance of 100nF size and a whole chip area of about $0.275mm^2$. During operation the converter obtains a maximum energy efficiency of 75%.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

In nowadays battery powered electronic devices an important figure of merit and hence a selling point beside the computational power is the battery life time. Beside some non-ideal effects of the battery itself one of the main losses occurs during the transformation of the higher battery voltage to the needed lower on-chip voltage domains. Many ways have been invented and investigations are still going on at the moment in order to reduce these conversion losses to a minimum.
This thesis is a corporate project with Infineon Technologies Austria AG, especially the Automotive Sense and Control department at the site in Graz. The aim of this work is to give an overview of the needed theoretical knowledge and finally present the implemented design of an integrated switched capacitor (SC) DC-DC converter, that can be used for a tire-pressure-measurement sensor. The design should illustrate the advantages of an SC DC-DC converter solution against a linear voltage regulator, especially in the case of a highly charged battery the voltage drop across the voltage regulator would lead to a significant decrease of the energy efficiency.
Of course the form factor is playing a key role thus the implementation is limited by terms of chip area. A converter that is able to transfer the $3.6V$ to $1.6V$ changing battery voltage into the desired $1.5V$ nominal output voltage should be designed with 3 floating capacitors of $350pF$ each which need an area of about $245\mu m$ times $245\mu m$. This should be realized in a 130nm standard Complementary Metal Oxide Semiconductor (CMOS) process with Metal-Oxide-Semiconductor (MOS) capacitors. One external capacitor with a size of smaller than $100nF$ can be used to provide the desired voltage ripple of smaller than $5mV$ at load currents of $1mA$ to $6mA$ at the output, that can occur in ramps with a rise time of as fast as $10ns$, as can be seen in the figure. Table 1.1 summarizes all the described specifications.

Specification	**Value**
Input Voltage	$1.6V$ - $3.6V$
Output Voltage	$1.4V$ - $1.6V$
Voltage Ripple	TBD
Load Current	$1mA$ - $6mA$
Flying Capacitance	$1050pF$
Output Capacitance	$100nF$
Efficiency	$> 60\%$
Switching Frequency	TBD

Table 1.1: Required specifications of the design.

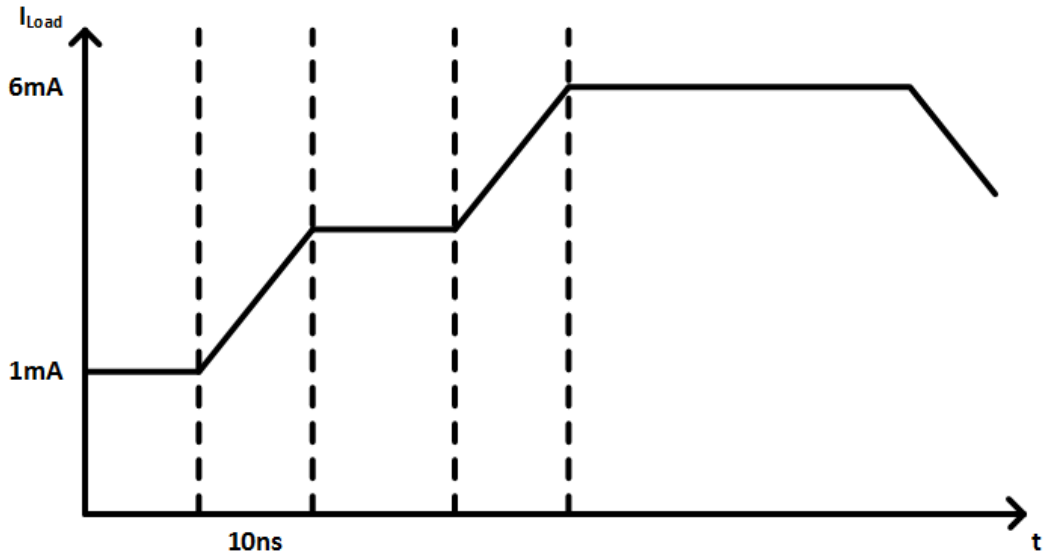

Figure 1.1: Specified load current that the SC DC-DC converter has to be able to provide at the output. A minimum current of $1mA$ up to a maximum of $6mA$ can be supplied with maximum changes of about $300\frac{\mu A}{ns}$.

1.2 Trends in Integrated Power Management Systems

Driven by the trend of the so called Internet of Things(IoT) small electronic devices and systems get embedded more and more into any part of our everyday life. To achieve as much functionality as possible the integration density per chip area is increasing and hence the transistor sizes are decreasing which leads to a decrease in the on chip voltage domains. On the other hand typical battery supply voltages are increasing. The so called voltage gap phenomenon is illustrated in 1.2. This development is the reason why efficient solutions of integrated power conversion are of interest for many applications.[1]

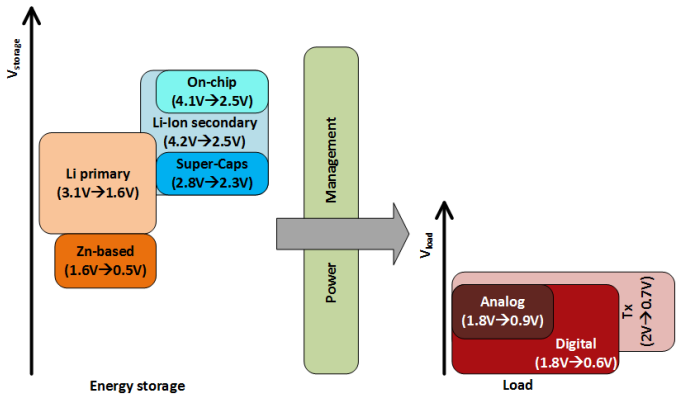

Figure 1.2: One of the tasks of the power management is to provide an efficient solution to the voltage gap between the increasing battery voltages and the decreasing on-chip voltage domains. The left plane shows different energy storage elements and their voltage levels whereas the right plane of the diagram shows typical required voltage levels of analog, digital and transceiver units.

Voltages can be converted to a desired voltage level by one of the following topologies:

- Switched-Capacitor Power Converters
- Inductive Power Converters
- Linear Voltage Regulators

Linear Voltage Regulators
In contrast to the other listed converter concepts the linear voltage regulator is only able to transfer a higher input voltage to a lower output voltage. Basically there are two types of linear voltage regulators the series converter and the shunt converter. In the case of a series converter the regulation is based on a resistive divider and hence the excess of input power is dissipated into a resistor. This working principle implies that the efficiency η_{lin} of such a converter is strongly dependent on its point of operation even if the supply current I_{cs} is neglected.

$$\eta_{lin} = \frac{P_{out}}{P_{in}} = \frac{U_{out} I_{out}}{U_{in}(I_{out} + I_{cs})}\bigg|_{I_{cs}=0} = \frac{U_{out}}{U_{in}} \tag{1.1}$$

Figure1.3 illustrates how such a converter can be implemented. The output voltage is compared against a reference and the resistance of the MOSFET is set accordingly. Because there is no need of a large integrated passive device like there is in a capacitive or inductive converter and its simple control still makes the linear voltage regulator a considerable alternative in integrated power converter solutions.[2]

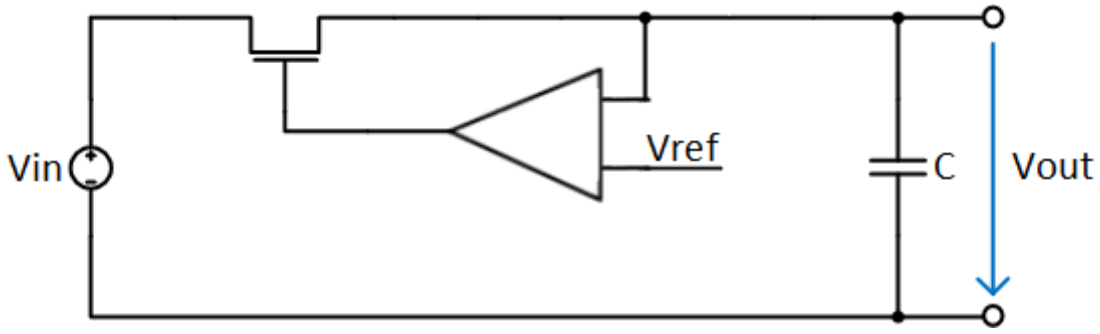

Figure 1.3: Architecture of a linear voltage regulator. By controlling the on-resistance of a transistor the output voltage is regulated.

Inductive Power Converters

Energy is stored temporarily in an inductor and an up and down conversion of the voltage is possible, figure 1.4 shows the structure of a down or so called buck converter. An air-core inductor is available in standard CMOS but the area is a main limiting factor. Also post-processed thin-film inductors with a magnetic core on top of standard CMOS, can increase the overall achievable inductance values, with the drawback that the core material reduces the quality factor and hence the efficiency. Values of about 100nH/mm2 at a peak quality factor of above 10 have been realized so far. Another option is to integrate the coil in the package of an IC, this is called System-in-Package(SiP). In a SiP approach bond wires, small discrete air-core inductors or package-trace air-core inductors can be built in the package and serve as temporary energy storage. Metal-Insulator-Metal(MIM) or high density trench capacitors are used for decoupling of the supply.[1]

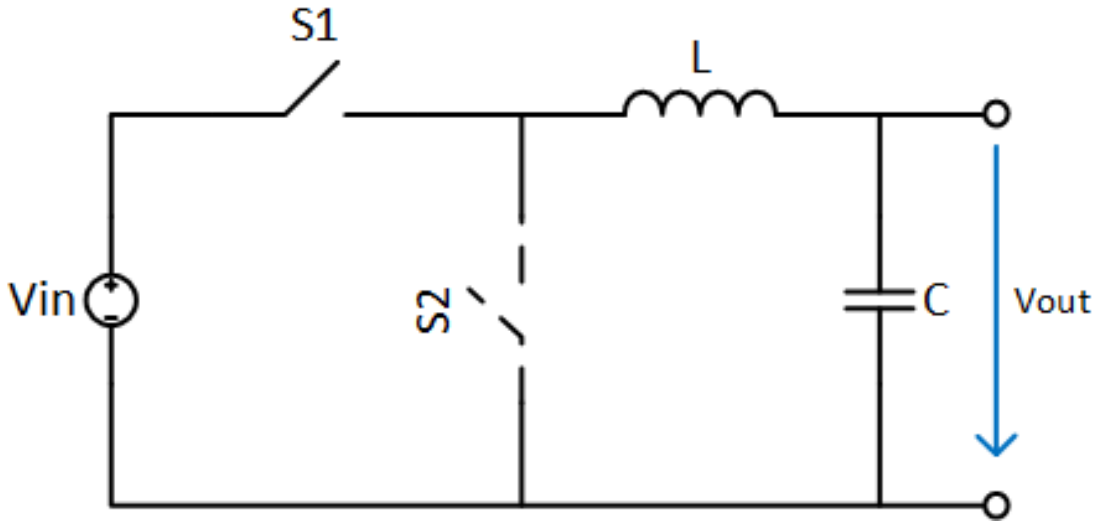

Figure 1.4: Topology of an inductive buck converter. During one cycle of operation energy is temporarily stored inside the coil and provided to the output. As there is enough voltage at the output switch $S1$ is turned off and $S2$ or a diode instead of $S2$ makes a conducting connection to the ground. The coil tries to keep the flowing current constant and hence provides energy that was stored in the magnetic field to the output. Thereby a constant average output voltage level can be obtained.

Switched-Capacitor Power Converters

Capacitive converters achieve a fixed voltage conversion ratio between the input and the output by periodically switching the so-called floating capacitors arrangement and thereby transporting small amounts of energy. A two phase switched-capacitor power converter(SCPC) is characterized by its two clock-phases where the capacitances get charged and discharged respectively. Figure 1.5 illustrates the switching between the charging phase ϕ_1 and the discharging phase ϕ_2 respectively the change of the capacitor arrangements. For the integration of SCPC the gate capacitance of MOSTs (MOSCAPS), Metal-Insulator-Metal(MIM) capacitors, MOSCAPS in SOI technology and finally external small SMD floating capacitors can be used. MOSCAPS in nm technology are available in every standard CMOS process and reach capacitance densities of $4 - 12nF/mm^2$, however they introduce quiet large bottom-plate losses. Metal-Insulator-Metal (MIM) capacitors in general have a lower bottom-plate capacitance and hence provide better efficiency, capacitance densities up to $2nF/mm^2$ are available. In SOI technology realized capacitances offer also low bottom-plate capacitances and densities up to $400nF/mm^2$. Small SMD capacitors can be used as external elements if needed.[1]

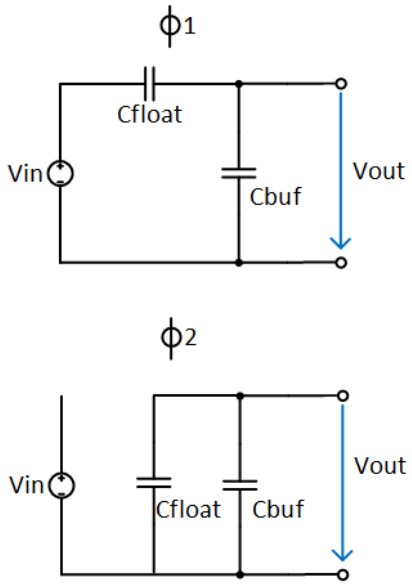

Figure 1.5: Principle of a two phase switched capacitor power converter. By changing the arrangement of the floating capacitor it is possible to generate a desired output voltage. In the circuit illustrated a $V_{out} = \frac{V_{in}}{2}$ can be achieved.

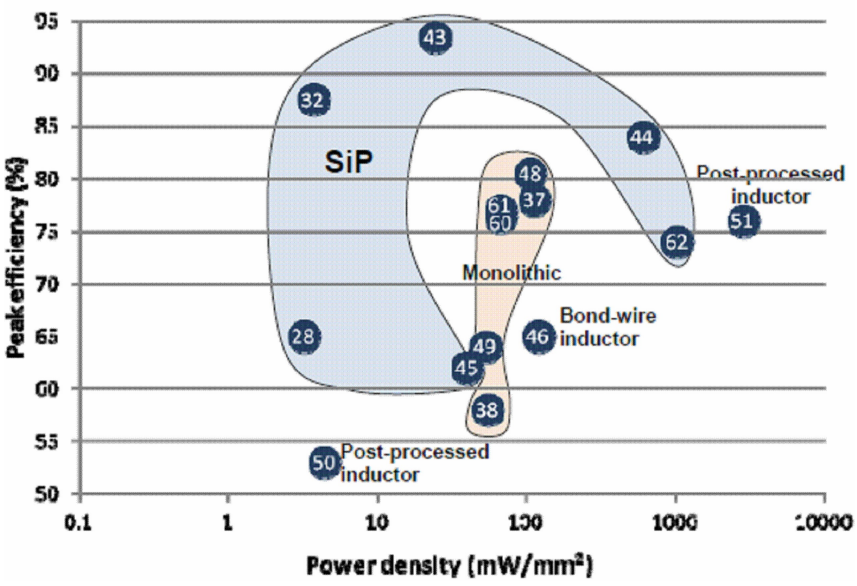

Figure 1.6: Efficiencies of different realizations of switched mode power supplies and with respect to their power densities. ©2013 IEEE [3]

Figure1.7 illustrates that there is a boundary between inductive and capacitive converter solutions depending on the required maximum output power. Capacitive solutions in general target the low to medium power range below 50mW peak, whereas for the higher power

applications the inductive converters dominate. [3]

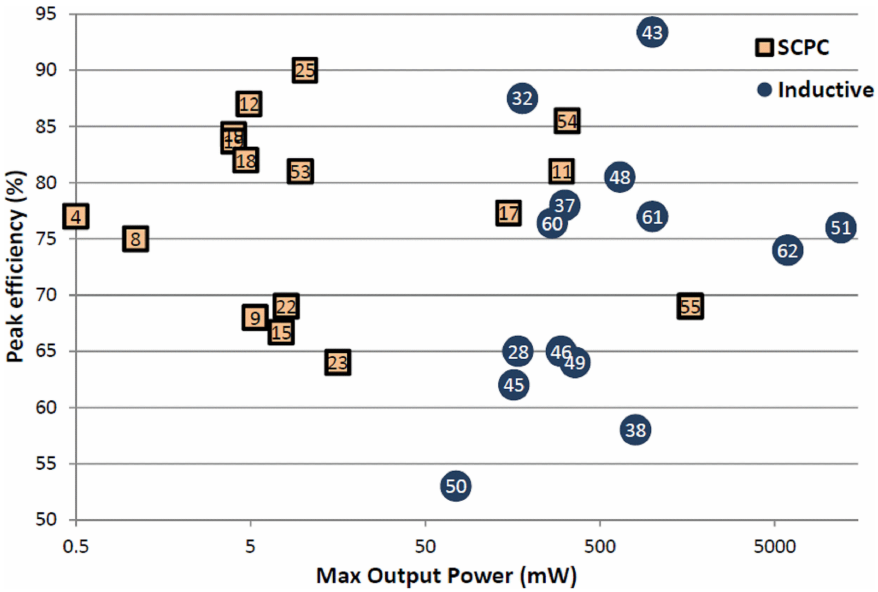

Figure 1.7: Switched capacitor designs compared to inductive converters regarding the peak efficiency with respect to their maximum output power. ©2013 IEEE [3]

Chapter 2

Theory of Switched Capacitor DC-DC Converters

This chapter deals with the theory behind switched capacitor DC-DC converter. The capacitive and the inductive approach of energy conversion are shown and the benefits of each one are discussed. Especially the losses that occur during the capacitive conversion are evaluated in detail. Based on that knowledge, the heart of each switched capacitor converter, the divider network, is explained in more detail. Several configurations of the divider and mathematical analysis methods are highlighted. Finally, an overview of commonly applied control strategies is given and the principles are shown.

2.1 Capacitive versus Inductive Energy Conversion

Capacitive Conversion
In order to transfer energy from the input of a capacitive converter to the output, the configuration of the used capacitances is changed. Thereby the energy, stored in the capacitances stays the same over one conversion cycle but the resulting voltage at the output differs from the input voltage that has been used to charge the capacitances. This process is illustrated in Fig 2.1.[4]

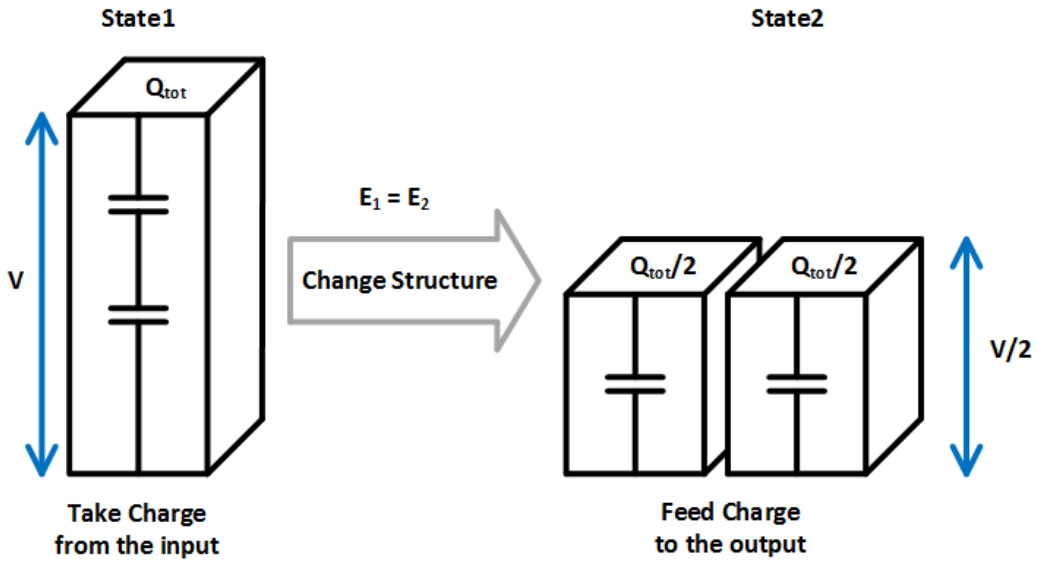

Figure 2.1: Charge in capacitances through one conversion cycle in case of a $\frac{1}{2}$ converter. In the State1 or charging phase two capacitors are connected in series and charged by a supply with the voltage V. Thereby a total amount of charge of Q_{tot} is provided to the capacitances. In the second phase of the conversion the capacitors that hold a $\frac{Q_{tot}}{2}$ each are connected in parallel and provide the same amount of energy but with a resulting voltage of $\frac{V}{2}$ to the output.

The energy in a capacitor is stored in an electric field that is created by the charge on two conductors separated by an insulating material. How much charge Q a capacitor is able to store, with respect to the applied potential difference U across it, is quantified by its capacitance C.

$$C = \frac{Q}{U} \tag{2.1}$$

The capacitance in general depends on the geometry, in case of a simple arrangement consisting of two parallel aligned plates the capacitance can be calculated by the area of the plates A, the distance between them d and the relative permittivity ϵ which characterizes the insulating material.

$$C_{ParallelPlates} = \frac{\epsilon A}{d} \tag{2.2}$$

To move an additional amount of charge dq from one plate to the other, the work dW has to be performed

$$dW = Udq = \frac{q}{C}dq \tag{2.3}$$

By loading a capacitor from 0 initial charge to Q, the total work W has to be performed.

$$W = \int_0^Q \frac{q}{C}\,\mathrm{d}q = \frac{Q^2}{2C} = \frac{CU^2}{2} \tag{2.4}$$

To describe the process of charging a capacitance, a schematic like shown in the figure 2.2 can be used to illustrate the process. Before the switch is shut, the capacitor is loaded to a voltage $V_{c,0}$. At the time the switch is shut, a current can flow to charge the capacitor to the value of the supply voltage V_{dd}. The resistor R in that case represents non ideal component properties of the connecting wire and the capacitor itself.

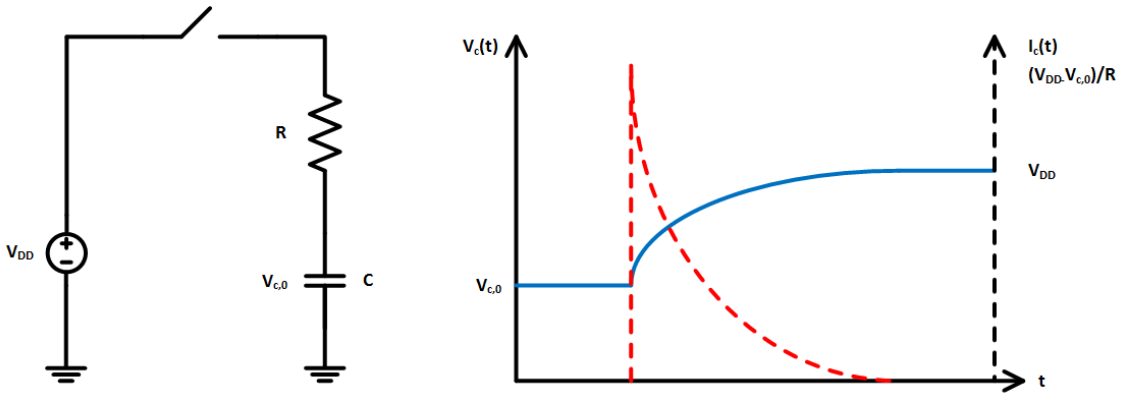

Figure 2.2: Loading process of a capacitance. The blue line shows the voltage across the capacitance over the time. The voltage reaches a maximum of V_{DD} whereas the red line illustrates the current through the capacitance that is limited by the resistor R and hence results in a maximum of $\frac{V_{DD}-V_{C,0}}{R}$.

The following differential equation expresses the charging process.

$$-V_{dd} + RC\frac{dV_C}{dt} + V_C = 0 \tag{2.5}$$

$V_C(t)$ and thus $I_C(t)$ can be derived from it and further stated by:

$$V_C(t) = V_{dd} - (V_{dd} - V_{C,0})e^{\frac{-t}{RC}} \tag{2.6}$$

$$I_C(t) = \frac{V_{dd} - V_{C,0}}{R}e^{\frac{-t}{RC}} \tag{2.7}$$

The power that is transferred to the capacitor can be calculated by the following equation.

$$P_C(t) = V_C(t)I_C(t) = \frac{V_{C,0}V_{dd} - V_{C,0}^2}{R}e^{\frac{-t}{RC}} \tag{2.8}$$

After this charging process the energy, that has been added to the capacitor is computed.

$$E_C = \int_0^\infty P_C(t)\,\mathrm{d}t = \int_0^\infty \frac{V_{C,0}V_{dd} - V_{C,0}^2}{R} e^{\frac{-t}{RC}}\,\mathrm{d}t = \frac{(V_{dd}^2 - V_{C,0}^2)}{2}C \tag{2.9}$$

Following the same procedure, the total energy that the supply has to deliver to the circuit can be calculated and the result can be stated by:

$$E_{tot} = \int_0^\infty P_{tot}(t)\,\mathrm{d}t = V_{dd}(V_{dd} - V_{C,0})C \tag{2.10}$$

A measure for the efficiency during that charging process can be determined by taking both the whole delivered energy and the final energy stored in the capacitor into account and relate them to each other. The energy that has not been inserted into the capacitor has been transformed into resistive losses in R. The final equation is stating that the efficiency to load the capacitor is not depending on R and just related to the difference between the voltage on the capacitor before the charging process and after the charging process.

$$\eta_{C,Charge} = \frac{E_C}{E_{tot}} = \frac{1}{2}\frac{V_{C,0} + V_{dd}}{V_{dd}} \tag{2.11}$$

Inductive Conversion
Analogical to the capacitive conversion converters that use inductors as energy storing elements can be built. In contrast to capacitors that use an electric field inductors use a magnetic field that is built up by a current flowing through the inductor. The voltage across an inductor V_L is dependent on the inductance L of the inductor itself, which is a measure of its ability to store a magnetic field and relates to its geometrical measures and the sudden change of the current I through the inductor.

$$V_L = L\frac{dI}{dt} \tag{2.12}$$

The current through the coil has to be provided by an external source that must perform work in order to force a current.

$$\frac{dW}{dt} = V_L I \tag{2.13}$$

Taking both equations into account the total amount of energy stored in the inductor can be further states as:

$$W = \int_0^\infty \frac{dW}{dt}\,\mathrm{d}t = \int_0^\infty V_L I\,\mathrm{d}t = \int_0^\infty L\frac{dI}{dt} I\,\mathrm{d}t = \frac{LI^2}{2} \tag{2.14}$$

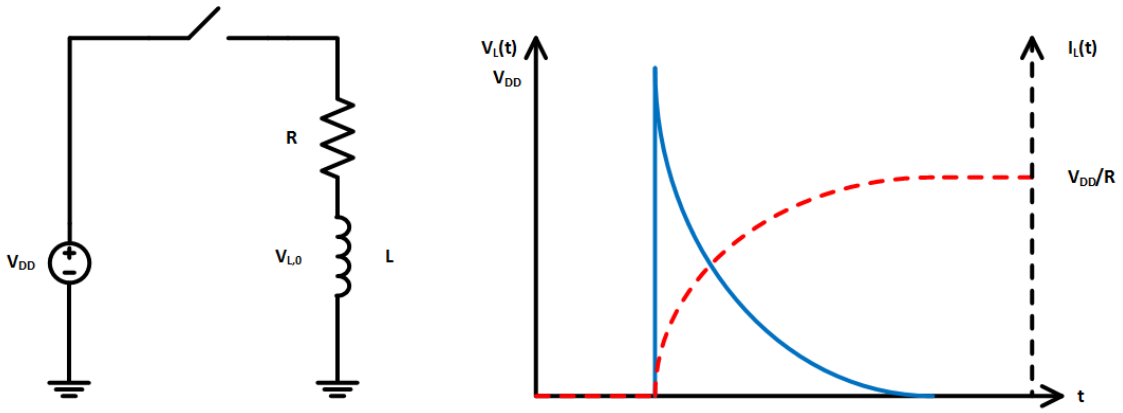

Figure 2.3: Loading process of an inductance. The blue line shows the voltage drop across the coil that has an occurring maximum of V_{DD} and exponentially decreases to zero. Whereas the current that is illustrated by the red line increases till a maximum of $\frac{V_{DD}}{R}$ is achieved.

The processes going on in the circuit can be described by the following differential equation:

$$-V_{dd} + RI_L + l\frac{dI_L}{dt} = 0 \tag{2.15}$$

Thus the voltage and current through the coil can be stated by:

$$V_L(t) = (V_{dd} - RI_L(0))e^{\frac{-tR}{L}} \tag{2.16}$$

$$I_L(t) = \frac{V_{dd}}{R} + (I_L(0) - \frac{V_{dd}}{R})e^{\frac{-tR}{L}} \tag{2.17}$$

The power and thereby the energy stored in the coil can be calculated by:

$$P_L(t) = V_L(t)I_L(t) = \frac{V_{dd}^2}{R}(e^{\frac{-tR}{L}} - e^{\frac{-2tR}{L}}) \tag{2.18}$$

$$E_L = \int_0^\infty P_L(t)\,\mathrm{d}t = \frac{LV_{dd}^2}{2R^2} \tag{2.19}$$

A look at the equation above shows that the stored energy in the inductor is proportional to the resistance R in the loading path. This means that the charging efficiency

and hence the whole conductive conversion process always depends on the quality of the coil itself and resistance due to the connection of the wires. This is a limiting factor and has to be taken in consideration when it comes to a monolithic integrated converter design.

2.2 Losses during Conversion and Converter Model

There are different types of approaches to model the losses and hence the behavior of a switched capacitor DCDC converter. One very basic model is shown in figure 2.4. As shown in chapter 2.1, the voltage ripple across a capacitance decreases the efficiency of the charge transport and can therefore be called a loss namely the intrinsic loss of a converter. This kind of loss is illustrated as a series resistance because it scales with the load current.

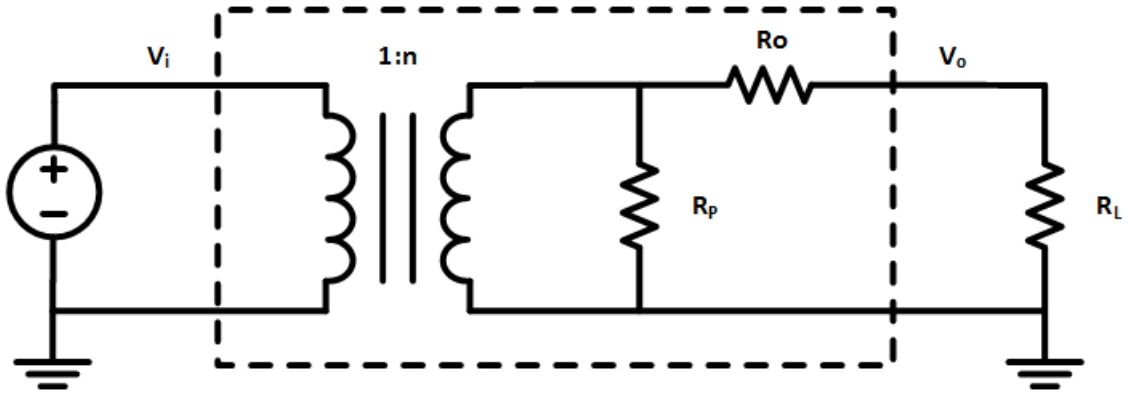

Figure 2.4: Model of a switched capacitor converter. Powered by a input voltage source with the voltage V_i the converter ideally generates a voltage conversion ratio of $1:n$ that is further decreased by a series resistance R_O that is a symbol for serial occurring losses during the conversion process. Permanent present parallel losses are represented by the resistor R_P. The loading at the output is illustrated by R_L. The resulting voltage that can be observed at the output of the converter is V_o.

As many converter supply a digital circuitry that consumes in an ideal case, the power P_{Lmin} at its minimum needed voltage V_{min} and a load current I_L.

$$P_{Lmin} = V_{min} I_L \tag{2.20}$$

Due to the voltage ripple ΔV that is unavoidable, the total average power P_{Ltot} consumed by the load increases and a small current change ΔI is introduced resulting in

$$P_{Ltot} = (V_{min} + \frac{\Delta V}{2})(I_L + \frac{\Delta I}{2}) \tag{2.21}$$

This additional inserted power in the load does not increase the performance and can hence be seen as a loss. Considering a two phase converter, the voltage ripple can be calculated as a function of the floating capacitance C_{fly}, I_L and the period time T respectively the switching frequency $f_{sw} = \frac{1}{T}$

$$\Delta V = \frac{I_L}{C_{fly}} \frac{T}{2} = \frac{I_L}{2C_{fly} f_{sw}} \tag{2.22}$$

Due to this voltage ripple the intrinsic switched capacitor losses of a converter can be stated as a function of the load current I_L, a converter type specific constant M_{cap}, the flying capacitance C_{fly} and the switching frequency $f_{sw} = \frac{1}{T}$.

$$P_{C_{fly}} = I_L \frac{\Delta V}{2} = \frac{I_L^2}{M_{cap} C_{fly} f_{sw}} \tag{2.23}$$

Additionally, the conductance of the switches used in a converter introduces a loss P_{Rsw} that is also related to the load, the on resistance R_{on} of the switch, the total width of all switches W_{sw} and a converter specific constant M_{sw}.

$$P_{Rsw} = I_L^2 \frac{R_{on}}{W_{sw}} M_{sw} \tag{2.24}$$

The final series loss can be determined by approximately:

$$P_s = I_L^2 R_0 = P_{Rsw} + P_{Cfly} \tag{2.25}$$

Furthermore, there are losses that are independent of the load current and introduced by the switching procedure to load and unload the gate and bottom plate capacitors of the switching transistors. Those losses are depicted as a resistance in parallel to the load to the ground. The parasitic capacitances especially in integrated capacitors introduce a loss $P_{bott-cap}$ that depends on the voltage swing V_o across it, the value C_{bott}, a converter specific constant M_{bott} and the switching frequency f_{sw} [5]:

$$P_{bott-cap} = M_{bott} V_0^2 C_{bott} f_{sw} \tag{2.26}$$

The loss due to the top plate in most cases is relatively small and therefore it is usually referred as bottom plate loss. Figure 2.5 shows the realization of a capacitor by means of two polysilicon layers in a double poly CMOS process and the resulting capacitance C and

parasitic capacitances C_{TP} which represents the top plate and $C_{BP} = \alpha C$ that scopes for the bottom plate and can make up to 10%.[6]

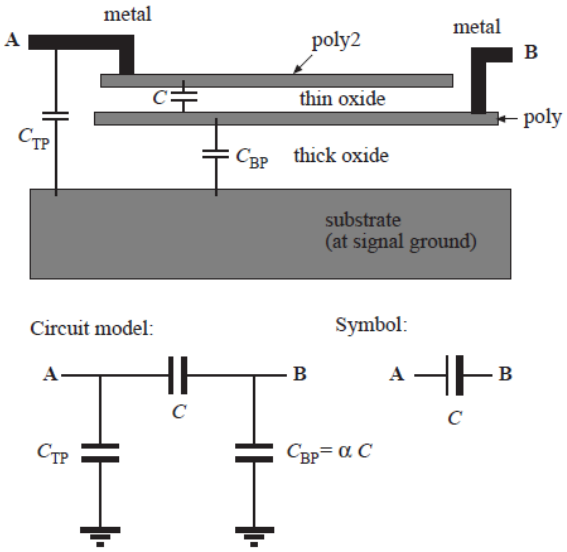

Figure 2.5: The top of the figure shows a realization of a capacitance with two poly layers. Due to the geometry, parasitic capacitances from the substrate to the metal connections named top plate capacitance C_{TP} and the substrate and the poly namely bottom plate capacitances C_{BP} occur. The purposed capacitance C thereby has to be considered with a circuit model like shown on the left.

Finally, assuming that all the switches implemented in converter are sized equally the loss $P_{gate-cap}$ due to the parasitic capacitances at the gates of the transistors can be calculated with the given voltage swing V_{sw}, the gate capacitance C_{gate}, the total width of all switches W_{sw} and the switching frequency f_{sw}:

$$P_{gate-cap} = V_{sw}^2 W_{sw} C_{gate} f_{sw} \tag{2.27}$$

2.3 Divider Networks

Each SC converter has a conversion ratio that can be observed at the output under an unloaded condition and which is just dependent on the topology respectively how the capacitances are switched over one cycle of conversion. The resulting ratio of the input voltage V_g to the output voltage V_o is called the ideal voltage conversion ratio (iVCR) M_i of a switched capacitor conversion network and can be expressed by two integer values P and Q that depend on how the capacitors are connected in the switching phases.[7]

$$M_i = \frac{V_o}{V_g} = \frac{P}{Q} \tag{2.28}$$

To find these integer values, a variety of analysis methods already exist, namely the charge flow analysis, the charge balance analysis and the branch analysis. The charge flow analysis is used to extract the charge flow vectors a_c^i that can be used to identify the role of the single capacitors in a SC network. The vectors can further be used to model the behaviour and performance of the converter. These vectors describe the amount of charge $q_i^{(j)}$ that is transferred by the capacitor i during the j state and q_{out} states the total amount of charge that is transferred during one switching cycle. That results in the case of a two phase converter in the following expression[4]

$$a_c^{(1)} = \left[q_{out}^{(1)} q_1^{(1)} ... q_n^{(1)} q_{in}^{(1)}\right] / q_{out} \tag{2.29}$$

$$a_c^{(2)} = \left[q_{out}^{(2)} q_1^{(2)} ... q_n^{(2)} q_{in}^{(2)}\right] / q_{out} \tag{2.30}$$

The elements of each vector can be found by inspection of the resulting network configurations in each phase and by obtaining Kirchhoff's current law in each node. That means the sum of charge in each node of the circuit must equal zero. In a steady state condition in every component the sum of both states must equal zero. In the following subsections this analysis method is applied on the $\frac{1}{2}$,$\frac{2}{3}$ and $\frac{3}{4}$ divider configurations of a series parallel switched capacitor network. These configurations are implemented in the converter and are therefore of interest.

2.3.1 1/2 Divider

The two phases during one switching cycle of a $\frac{1}{2}$ converter switch network can be sketched like circuits in figure 2.6. This allows the determination of the charge flow vectors in terms of:

$$a_c^{(1)} = \begin{bmatrix} q_{out}^{(1)} & q_{C1}^{(1)} & q_{in}^{(1)} \end{bmatrix} / q_{out} \tag{2.31}$$

$$= \begin{bmatrix} q_{in} & q_{in} & q_{in} \end{bmatrix} / q_{out} \tag{2.32}$$

$$a_c^{(2)} = \begin{bmatrix} q_{out}^{(2)} & q_{C1}^{(2)} & q_{in}^{(2)} \end{bmatrix} / q_{out} \tag{2.33}$$

$$= \begin{bmatrix} q_{in} & -q_{in} & 0 \end{bmatrix} / q_{out} \tag{2.34}$$

$$\tag{2.35}$$

Here q_{out} represents the sum of charge that is delivered over the two phases of one full switching cycle in this case $q_{out} = 2q_{in}$. That represents the circumstance that the charge

at the output in every phase is equal to the inserted charge.
This leads to:

$$a_c^{(1)} = \begin{bmatrix} \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.36}$$
$$a_c^{(2)} = \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} & 0 \end{bmatrix} \tag{2.37}$$
$$\tag{2.38}$$

The switching networks ideal conversion ratio can be found by the ratio between the total input charge flow $q_{in_{total}}$ with respect to the resulting output charge flow $q_{out_{total}}$

$$N = \frac{q_{in_{total}}}{q_{out_{total}}} = \frac{\frac{1}{2} + 0}{\frac{1}{2} + \frac{1}{2}} = \frac{1}{2} \tag{2.39}$$

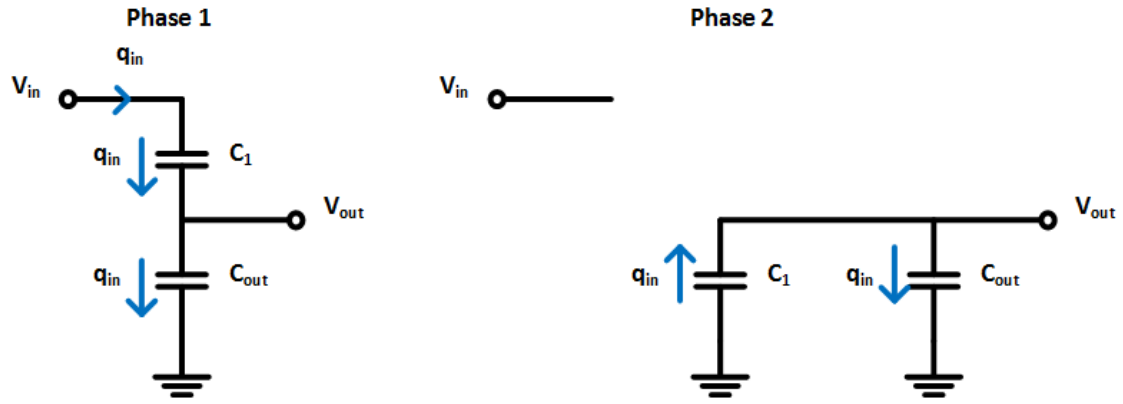

Figure 2.6: $\frac{1}{2}$ switching network. The illustration shows the charge flow in each phase of the conversion cycle through each component of the circuit.

2.3.2 2/3 Divider

In case of a two $\frac{2}{3}$-divider the phases during one switching cycle can be illustrated like circuits in figure 2.7. Thereby the charge flow vectors can be calculated as:

$$a_c^{(1)} = \begin{bmatrix} q_{out}^{(1)} & q_{C1}^{(1)} & q_{C2}^{(1)} & q_{in}^{(1)} \end{bmatrix} / q_{out} \tag{2.40}$$
$$= \begin{bmatrix} q_{in} & \frac{q_{in}}{2} & \frac{q_{in}}{2} & q_{in} \end{bmatrix} / q_{out} \tag{2.41}$$
$$a_c^{(2)} = \begin{bmatrix} q_{out}^{(2)} & q_{C1}^{(2)} & q_{C2}^{(2)} & q_{in}^{(2)} \end{bmatrix} / q_{out} \tag{2.42}$$
$$= \begin{bmatrix} \frac{q_{in}}{2} & -\frac{q_{in}}{2} & -\frac{q_{in}}{2} & 0 \end{bmatrix} / q_{out} \tag{2.43}$$
$$\tag{2.44}$$

The sum of charge at the output over the two phases q_{out} of one full switching cycle in this case equals $q_{out} = \frac{3}{2}q_{in}$. It shows that there is an amount of $\frac{1}{3}q_{in}$ that is not directly propagated to the output.
This results in:

$$a_c^{(1)} = \begin{bmatrix} \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & \frac{2}{3} \end{bmatrix} \tag{2.45}$$
$$a_c^{(2)} = \begin{bmatrix} \frac{1}{3} & -\frac{1}{3} & -\frac{1}{3} & 0 \end{bmatrix} \tag{2.46}$$
$$\tag{2.47}$$

The switching networks ideal conversion ratio can be found by the ratio between the total input charge flow $q_{in_{total}}$ with respect to the resulting output charge flow $q_{out_{total}}$.

$$N = \frac{q_{in_{total}}}{q_{out_{total}}} = \frac{\frac{2}{3} + 0}{\frac{2}{3} + \frac{1}{3}} = \frac{2}{3} \tag{2.48}$$

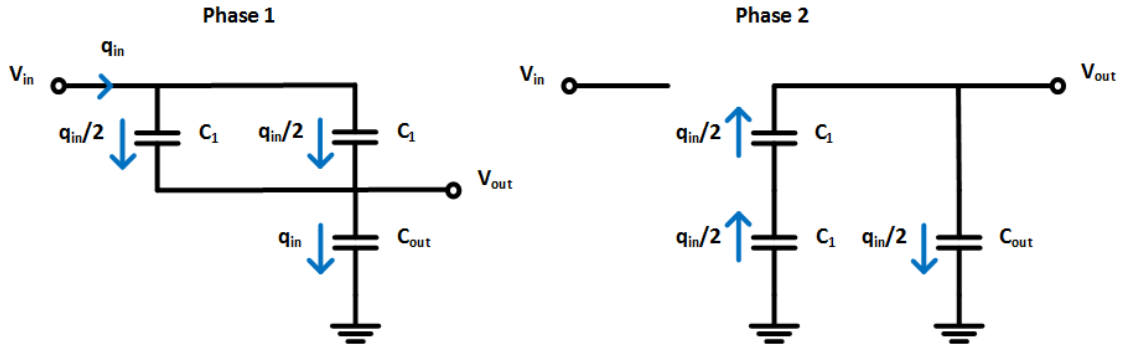

Figure 2.7: $\frac{2}{3}$ switching network. The illustration shows the charge flow in each phase of the conversion cycle through each component of the circuit.

2.3.3 3/4 Divider

The two phases during one switching cycle of a $\frac{1}{2}$ converter switch network can be sketched like circuits in figure 2.8. This allows the determination of the charge flow vectors in terms of:

$$a_c^{(1)} = \begin{bmatrix} q_{out}^{(1)} & q_{C1}^{(1)} & q_{C2}^{(1)} & q_{C3}^{(1)} & q_{in}^{(1)} \end{bmatrix} / q_{out} \tag{2.49}$$
$$= \begin{bmatrix} q_{in} & \frac{q_{in}}{3} & \frac{q_{in}}{3} & \frac{q_{in}}{3} & q_{in} \end{bmatrix} / q_{out} \tag{2.50}$$
$$a_c^{(2)} = \begin{bmatrix} q_{out}^{(2)} & q_{C1}^{(2)} & q_{C2}^{(2)} & q_{C3}^{(2)} & q_{in}^{(2)} \end{bmatrix} / q_{out} \tag{2.51}$$
$$= \begin{bmatrix} \frac{q_{in}}{3} & -\frac{q_{in}}{3} & -\frac{q_{in}}{3} & -\frac{q_{in}}{3} & 0 \end{bmatrix} / q_{out} \tag{2.52}$$
$$\tag{2.53}$$

Here q_{out} represents the charge delivered to the output over one full switching cycle in this case $q_{out} = \frac{4}{3}q_{in}$. This leads to:

$$a_c^{(1)} = \begin{bmatrix} \frac{3}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{3}{4} \end{bmatrix} \tag{2.54}$$

$$a_c^{(2)} = \begin{bmatrix} \frac{1}{4} & -\frac{1}{4} & -\frac{1}{4} & -\frac{1}{4} & 0 \end{bmatrix} \tag{2.55}$$

$$\tag{2.56}$$

The switching networks ideal conversion ratio can be found by the ratio between the total input charge flow $q_{in_{total}}$ with respect to the resulting output charge flow $q_{out_{total}}$.

$$N = \frac{q_{in_{total}}}{q_{out_{total}}} = \frac{\frac{3}{4} + 0}{\frac{3}{4} + \frac{1}{4}} = \frac{3}{4} \tag{2.57}$$

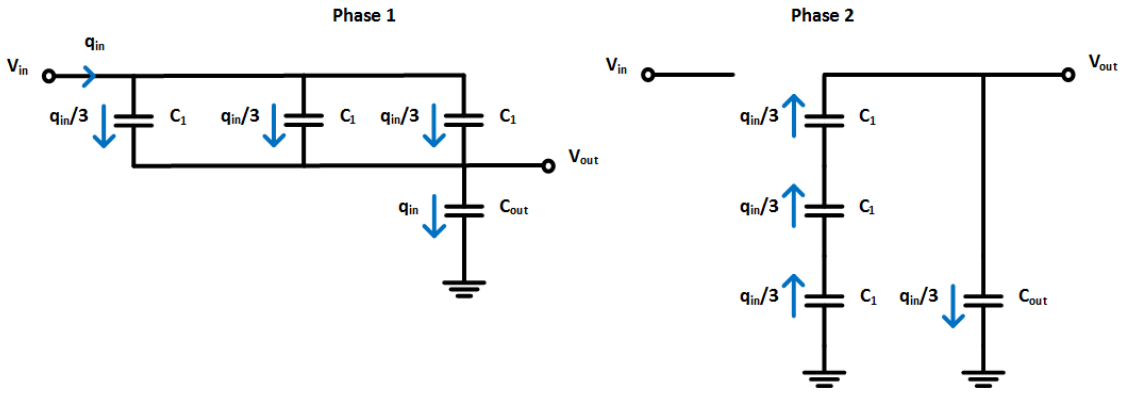

Figure 2.8: $\frac{3}{4}$ switching network. The illustration shows the charge flow in each phase of the conversion cycle through each component of the circuit.

2.4 Control Strategies

Chapter 2.3 already introduced the fact that a switched capacitor divider network has an ideal voltage conversion ratio that results at the output of a converter in an unloaded operating condition and is just dependent on the switching between the interconnections of the used capacitances. Additional loading of the output introduces an additional voltage drop that lowers the overall output voltage. Therefore different control strategies are applied to get a desired behaviour of the converter under specified load and supply conditions.

2.4.1 Topology Reconfiguration

The idea of topology reconfiguration is to switch between different configurations of available capacitances in order to achieve a desired output voltage and a reasonable efficiency

under a specific load respectively supply voltage condition. A lot of converter designs implement this kind of control technique as it can be seen in the literature for example in [8],[9],[10] and [11]. The reason is that there is a large number of iVCRs realizable with a reasonable amount of floating capacitances. Table 2.4.1 gives an overview of the possible iVCRs that can be implemented by a given number of capacitances.

Number of floating capacitors	**Possible ideal voltage conversion ratios**
1	$1, \frac{1}{2}, 2$
2	$\frac{1}{3}, \frac{1}{2}, \frac{2}{3}, 1, \frac{3}{2}, 2, 3$
3	$\frac{1}{5}, \frac{1}{4}, \frac{1}{3}, \frac{2}{5}, \frac{1}{2}, \frac{3}{5}, \frac{2}{3}, \frac{3}{4}, \frac{4}{5}, 1, \frac{5}{4}, \frac{4}{3}, \frac{3}{2}, \frac{5}{3}, 2\ \frac{5}{2}, 3, 4, 5$

Table 2.1: Possible conversion ratios with a maximum of 3 floating capacitances.

2.4.2 Pulse Frequency Modulation-PFM

One method to stabilize the output voltage of an switched capacitor DC-DC converter is the so called pulse frequency modulation (PFM). As the name suggests, it sets the switching frequency of a converter according to the conditions at the output by sensing the output voltage respectively the error between a desired voltage and the current output voltage level. In general, the implementations are divided into continuous time and discrete time control methods.

Time-continuous PFM
To implement a time-continuous PFM control two essential sub blocks are required namely a difference block and a voltage-to-time converter. As already mentioned, the output voltage is steadily compared against a reference voltage and the error between the desired and the actual output voltage is passed on to the voltage to time converter, which is in many applications a current controlled ring oscillator. One problem that arises with the use of time-continuous PFM is possible instability. The converter has a single dominant pole by nature that has a variable frequency which depends on the load variation and by inserting feedback additional poles are introduced. These poles come due to the additional control circuitry inside the feedback path and have a fixed frequency like it is shown in the figure 2.9. Depending on the position of these poles the resulting phase margin can be too small to ensure a stable behaviour of the system.

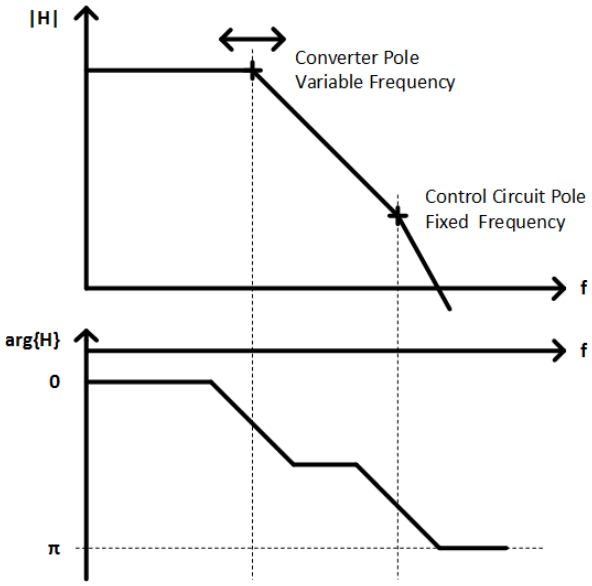

Figure 2.9: Transfer function of a continuous PFM block. The figure shows the transfer function over the frequency of a SC DCDC converter with a pole that depends on the load and a fixed pole that is introduced by the control circuitry.

Figure 2.10 shows the block diagram of a time-continuous PFM control block and the resulting signal. As can be seen the frequency scales with the error of the output voltage to the reference. [4]

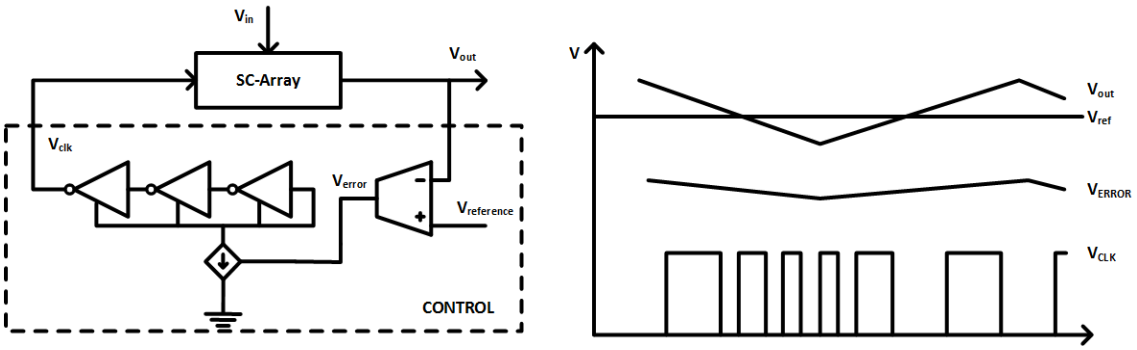

Figure 2.10: Block diagram of a time-continuous pulse frequency modulation block. The output voltage V_{out} is compared to a reference voltage V_{ref} and the resulting error V_{error} is used to settle a current controlled ring oscillator that forwards a clock signal V_{clk} to the SC-Array.

Time-discrete PFM

The mentioned stability problem with time-continuous PFM control methods does not occur in a time-discrete realization. It is shown in [4] that the discrete-time control is confined to a surface that is given by the converters structure and for any given state the converter operates in such a way that the converters state stirs to the area between the

main trajectories. This is one reason beside the simple implementation and good efficiency adjustment, why the time-discrete PFM is widely used in switched capacitor converters. A discrete-time PFM control circuit can be built by an oscillator with a fixed frequency, a comparator with a desired voltage reference and a AND gate. If the voltage at the output is below the threshold voltage of the comparator, the converter executes charge pumps with the frequency of f_{clk} and the output voltage starts to rise. When the output voltage reaches the desired level, the converter stops the charging pumps and the output voltage starts to lower depending on the load. Figure 2.11 shows the described behaviour. [10]

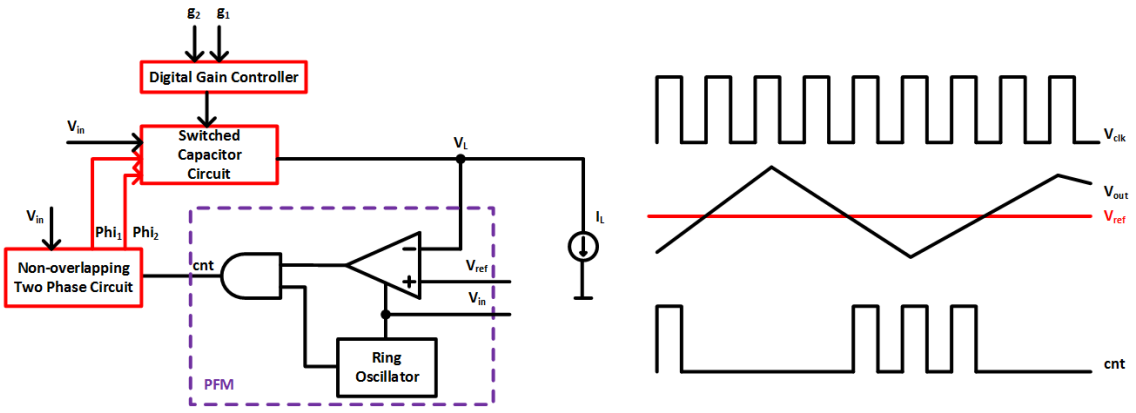

Figure 2.11: Block diagram of a time-discrete pulse frequency modulation block. The ring oscillator is operated with a constant frequency that is determined by the input voltage V_{in}. As the output voltage of the converter V_L reaches a threshold voltage that is given by V_{ref}, the pulses of the ring oscillator are forwarded to generate the charge and discharge phases of the converter.

2.4.3 Pulse Width Modulation

One way to deal with a load variation at the output is to change the output impedance of the converter and hence hold the output voltage at a desired level. As a SC converter can be illustrated, as it is shown in figure 2.4, the output voltage can be calculated by the resistive voltage divider between the load resistance R_L and the series output resistance of the converter R_O. The ideal generated output voltage that is determined by the constant N and the input voltage V_i is decreased by the resistive divider R_L and R_O and gives the resulting output voltage V_{out}

$$V_{out} = NV_i \frac{R_L}{R_L + R_o} \tag{2.58}$$

The problem that arises is the lowering of the efficiency especially in the lower output-power region, since the switching frequency itself stays constant and so do the losses at the switches of the converter. This is the main reason why this method is rarely used in SC DC-DC converters. [4]

2.4.4 Multi-Phase Interleaving and Fragmentation

In order to reduce the output voltage ripple and the furthermore the load current ripple, the multi-phase interleaving technique in combination with fragmentation of the SC DC-DC converter can be applied. Figure 2.12 illustrates the basic idea behind multiphase interleaving. In this example a converter is fragmented into four smaller units and they are switched phase shifted to each other. Thereby the delivered charge at the output stays the same as it would appear in the case of just one big divider, but the charge is delivered more finely and thus the current ripple gets reduced by the interleaving factor $k_{interleaved}$ by [5]

$$P_{Ltot} = (V_{min} + \frac{\Delta V}{2})(I_L + \frac{1}{k_{interleaved}}\frac{\Delta I}{2}) \tag{2.59}$$

It is shown in [4] that by fragmenting a SC DC-DC converter in terms of its floating capacitor and its switch sizes by a factor $k_{interleaved}$ that the resulting converter does not suffer in terms of performance respectively efficiency. Furthermore, [5] states that for many designs the number of fragmentations does not have to be that excessively large. In the proposed design 10 interleaved phases have decreased the voltage ripple to an almost neglect-able value. It has to be mentioned that multi-phase interleaving and fragmentation is a design consideration in the first place rather than a control strategy but by implementing a fragmented converter another degree of freedom in terms of load regulation is introduced. By having more than just one converter available it is easier to react on the loading demand at the output in an efficient way.

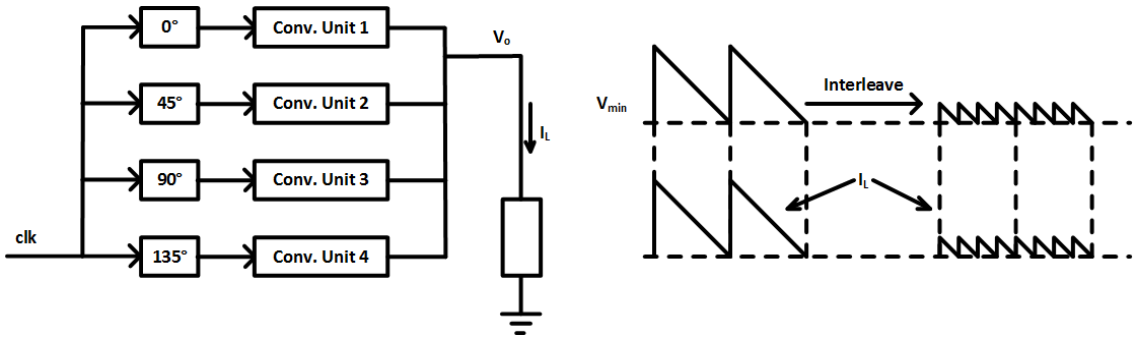

Figure 2.12: Block diagram of a 4-phase interleaved SC converter and the resulting effect on the output ripple voltage. The delivered charge at the output stays the same while the output voltage ripple is reduced by a factor of 4 due to the applied fragmentation.

Chapter 3

Design Considerations for the Converter

In the following chapter the implemented switched capacitor converter is described in detail. First, an overview of the converter architecture and a general remark on the operation is given. The necessary sub blocks that are implemented in a $130nm$ process are explained and design considerations are mentioned.

3.1 Architecture

The converters heart are the "sc_divider_circuit" cells which are switch circuitries that allow to select either 1, $\frac{3}{4}$, $\frac{2}{3}$ or $\frac{1}{2}$ input to output voltage conversions. It has two of them which are switched in a 45°-phase shifted manner that is caused by the "delay" cells. The "gate_logic" cells are decoder circuits that enable the right selection of the switches in the required phase. The decision on the right selection of the configuration of the switch circuitry is done by the "control_unit". It computes the signals from the "comparators" cell and decides if the current switch configuration setting is appropriate or changes it accordingly. Another cell that is connected to the "comparators" cell is the "PFM" cell which enables the pulse frequency modulation scheme on the charge and discharge phases of "sc_divider_circuit" cells. The charge and discharge phases must not be active at the same time and are generated out of an external $33MHz$ signal by the "non_overlapping_clk" cell. Four threshold voltages are used to enable the correct operation of the converter. An external $1.2V$ bandgap reference voltage is fed into the "threshold_generation" cell that resistively divides the voltage to the necessary voltage levels. These references are needed by the "comparators" cell which senses the output voltage of the whole converter and generates signals that are necessary for further computation. Figure 3.1 shows a block diagram of the explained converter architecture, its sub cells and their interconnections and also the interfacing connections to other blocks.

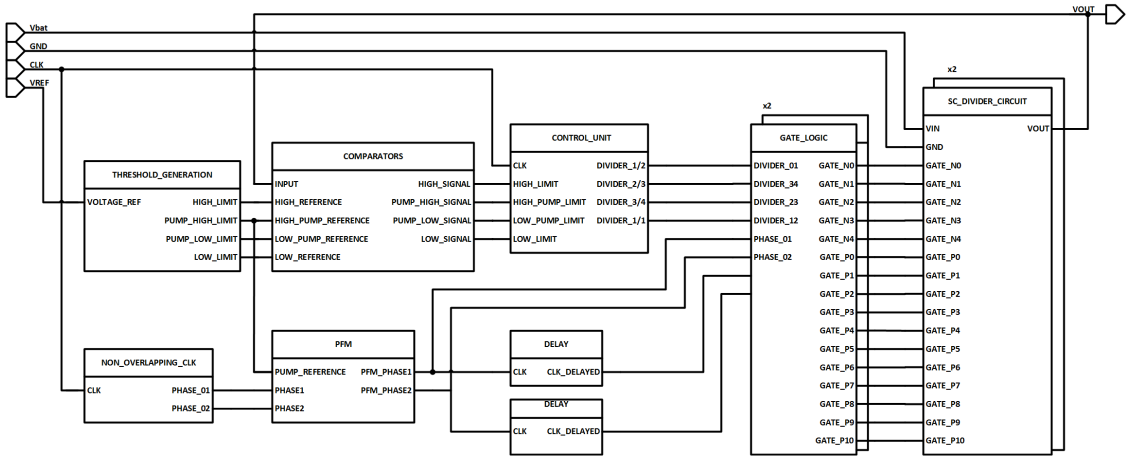

Figure 3.1: Block diagram of the implemented switched capacitor converter.

3.2 Non Overlapping Clock Generation

The charge and discharge phase during the conversion cycles must not be activated at the same time. An intersection of the two phases would lead to an charge transfer between the floating capacitors which would further result in a degradation of the overall efficiency. It is also important to reduce the time between the phases to a minimum, because parasitic elements of the capacitors would cause a discharge over time. At a period time of $30ns$ the intermediate time between the two phases of the conversion is set to less than 10% that gives $3ns$ for the whole time per phase neither $Phase1$ nor $Phase2$ is active. A circuit like it is shown in figure 3.2 is used to ensure these requirements. The external clock signal is fed into an inverter chain that causes a delay that is specified by the sum of delays of each single inverter stage. $Phase1$ which indicates the charge phase is resulting from an AND gate that connects the external input clock with the delayed clock. Similar the discharge $Phase2$ is generated by taking the inverse of the result of an OR gate of the clocking signals. Figure 3.3 shows the desired timing diagram of the signals in the non-overlapping clock generation and the charge phase $Phase1$ and discharge phase $Phase2$.

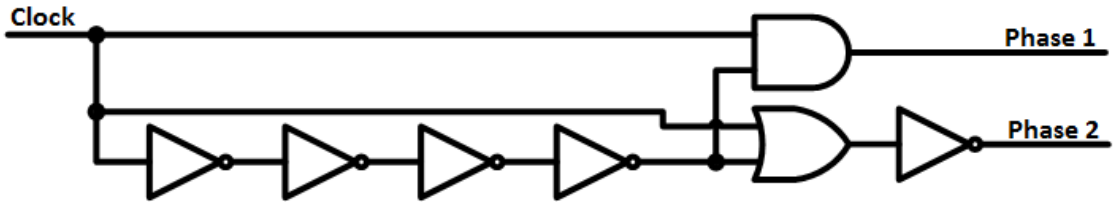

Figure 3.2: Circuit to generate a non-overlapping clock signal for the switched capacitor divider network.

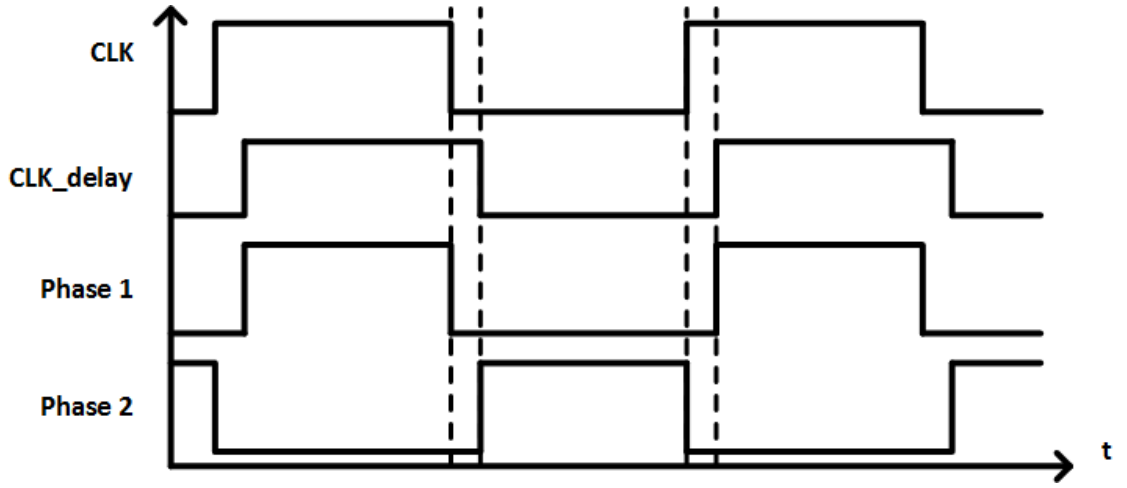

Figure 3.3: Timing diagram of the non-overlapping clock signal generation block.

3.3 Delay

In order to create a 45°-phase shifted signal from the input clock signal a RC delay is implemented. It uses an input buffer that is built up by the transistors $P1$, $P2$, $P3$, $P4$, $N1$, $N2$, $N3$ and $N4$ to charge and discharge the RC element and an output buffer composed of $P5$, $P6$, $P7$, $P8$, $N5$, $N6$, $N7$ and $N8$. The buffers are biased by the transistor $P0$ and $N0$ which also determine the maximum current that loads respectively unloads the capacitance. Since $P0$ and $N0$ are operated in the saturation region, the current through them is determined by [12]

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{3.1}$$

The current is mirrored to the transistors $P1$, $P3$, $P5$, $P7$, $N1$, $N3$, $N5$ and $N7$.

As the input signals frequency is $33MHz$ it has a period time of

$$T = \frac{1}{f_{clk}} = \frac{1}{33.3MHz} = 30ns \tag{3.2}$$

The needed time delay in order to create a 45°-phase shift is therefore

$$t_{delay} = T\frac{1}{4} = 7.5ns \tag{3.3}$$

So called current starved buffers are used because a simple inverter with an RC element would lead to a rather high resistor value in order to charge a $10fF$ capacitor that is required to keep the whole circuitry in a reasonable spacial dimension and still gives the

needed delay. Additionally, the maximum occurring crowbar current is limited by this structure.

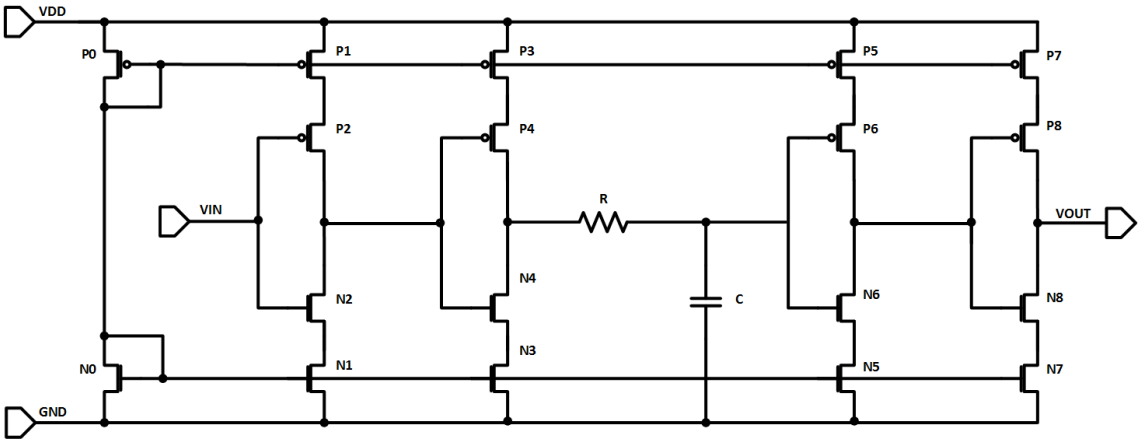

Figure 3.4: Circuit for the generation of a 7.5ns delay. P0 and N0 settle the current for the current starved inverter connected to it. The transistors P1,P2,P3,P4 and N1,N0,N3,N4 build up an input buffer that loads the RC network connected to it. P5,P6,P7,P8 and N5,N6,N7,N8 set up the output buffer that is able to drive the output of the whole cell.

3.4 PFM

A pulse frequency modulation switching scheme is implemented by a circuit that is shown in figure 3.5, it gets a "high" signal if the output voltage has crossed the threshold voltage for disabling further charge pumps. The gated clock latches enable a positive flank triggered reaction on the according event. In that way it is always $Phase1$ that starts another charge pump cycle. The resulting signal behaviour is shown in figure 3.6.

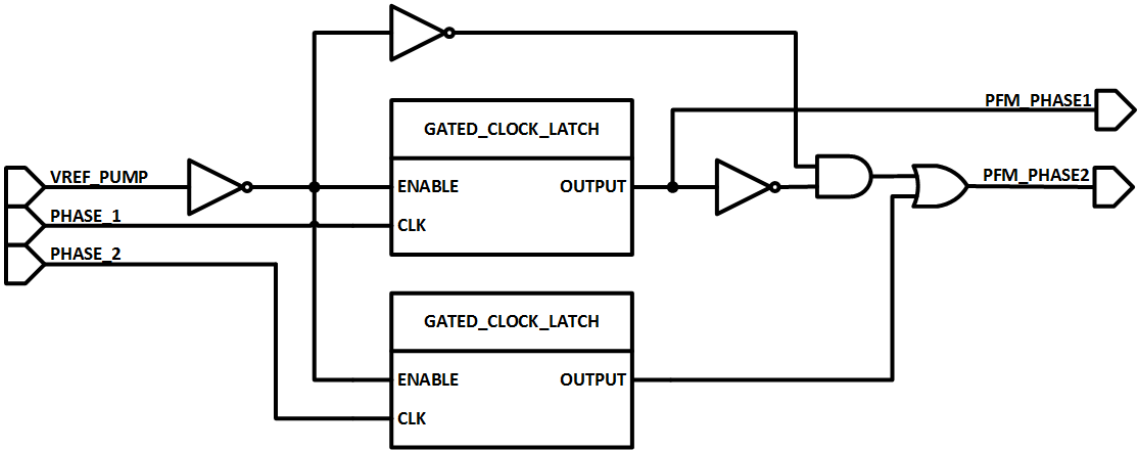

Figure 3.5: Block diagram of the PFM block.

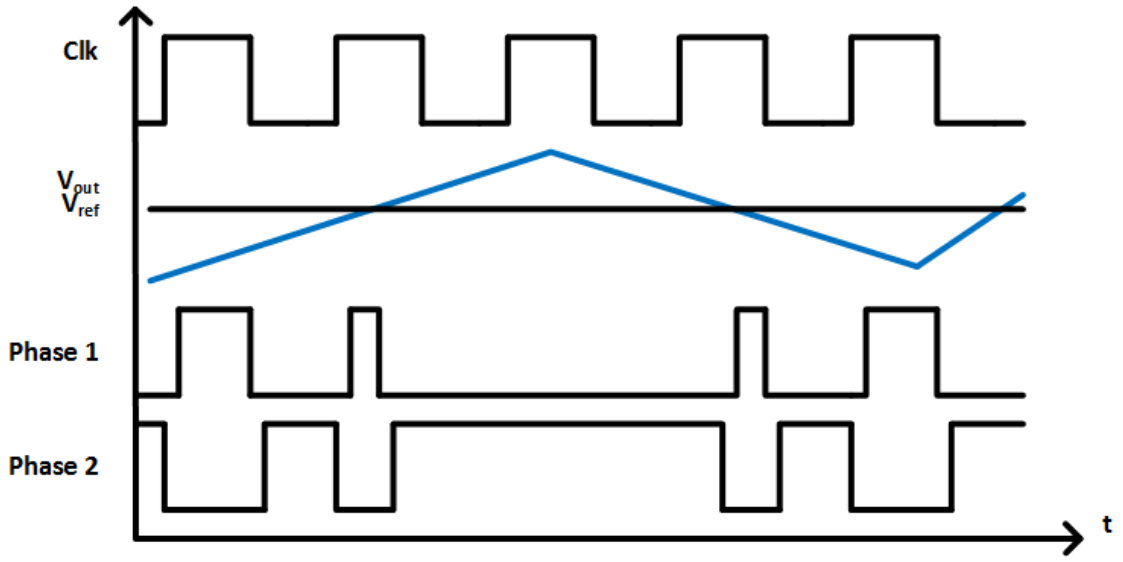

Figure 3.6: Timing diagram of the resulting signals in the PFM block. As long as the output voltage V_{out} stays beneath the reference voltage V_{ref}, the clock signal Clk is used to generate the non-overlapping phases.

3.5 Threshold Generation

A resistive voltage divider is used to create the desired voltage limits for the further processing. It gets $1.2V$ from a bandgap reference and outputs $0.8V$, $0.74V$, $0.72V$ and $0.7V$ voltages. These voltage levels are further used for the comparators as a reference where the output voltage is observed. It has to be mentioned that the comparators just see the half output voltage therefore the desired $1.5V$ result in a $0.75V$ at the comparator input. In order to generate these limits at the output the needed current was set to less than $3\mu A$ resulting in the following resistor dimensions.

$$R_0 = \frac{V_{R0}}{I} = \frac{1.2V - 0.8V}{3\mu A} = 133.3k\Omega \tag{3.4}$$

$$R_1 = \frac{V_{R1}}{I} = \frac{0.8V - 0.74V}{3\mu A} = 20k\Omega \tag{3.5}$$

$$R_2 = \frac{V_{R2}}{I} = \frac{0.74V - 0.72V}{3\mu A} = 6.66k\Omega \tag{3.6}$$

$$R_3 = \frac{V_{R3}}{I} = \frac{0.72V - 0.7V}{3\mu A} = 6.66k\Omega \tag{3.7}$$

$$R_4 = \frac{V_{R4}}{I} = \frac{0.72V}{3\mu A} = 233.3k\Omega \tag{3.8}$$

Since the output voltages are a function of the voltage reference that is assumed to be ideal and the resistor values R_0, R_1, R_2, R_3 and R_4, the difference between the ideal calculated

values and occurring ones has to be taken into account by means of the standard deviation of the output signals. The variance of the mismatch of one resistor value can be calculated by the given mismatch parameter A_R and the spacial dimensions of the resistor namely the width W and the length L by applying

$$\sigma\left(\frac{\Delta R}{R}\right) = \frac{A_R}{\sqrt{WL}} \tag{3.9}$$

Thereby the variance of R_0, R_1, R_2, R_3 and R_4 due to mismatch can be calculated according to a 3σ range that includes 99.7% of all possible occurring values.

$$\sigma_{R_0} = \frac{3 \cdot A_{R_0}}{\sqrt{W_{R_0} L_{R_0}}} = 1.257\% \tag{3.10}$$

$$\sigma_{R_1} = \frac{3 \cdot A_{R_1}}{\sqrt{W_{R_1} L_{R_1}}} = 3.307\% \tag{3.11}$$

$$\sigma_{R_2} = \frac{3 \cdot A_{R_2}}{\sqrt{W_{R_2} L_{R_2}}} = 6\% \tag{3.12}$$

$$\sigma_{R_3} = \frac{3 \cdot A_{R_3}}{\sqrt{W_{R_3} L_{R_3}}} = 6\% \tag{3.13}$$

$$\sigma_{R_4} = \frac{3 \cdot A_{R_4}}{\sqrt{W_{R_4} L_{R_4}}} = 0.949\% \tag{3.14}$$

These deviations can be used to calculate a propagation of uncertainty for all three voltage levels as for the $HIGH\_LIMIT$ V_H can be written assuming a constant reference voltage of $1.2V$.

$$V_H = V_{ref}\frac{R_1+R_2+R_3+R_4}{R_0+R_1+R_2+R_3+R_4} \tag{3.15}$$

$$\frac{\partial V_H}{\partial R_0} = -V_{ref}\frac{R_1+R_2+R_3+R_4}{(R_0+R_1+R_2+R_3+R_4)^2} = -2mV \tag{3.16}$$

$$\frac{\partial V_H}{\partial R_1} = V_{ref}\frac{R_0}{(R_0+R_1+R_2+R_3+R_4)^2} = 833.33\mu V \tag{3.17}$$

$$\frac{\partial V_H}{\partial R_2} = V_{ref}\frac{R_0}{(R_0+R_1+R_2+R_3+R_4)^2} = 833.33\mu V \tag{3.18}$$

$$\frac{\partial V_H}{\partial R_3} = V_{ref}\frac{R_0}{(R_0+R_1+R_2+R_3+R_4)^2} = 833.33\mu V \tag{3.19}$$

$$\frac{\partial V_H}{\partial R_4} = V_{ref}\frac{R_0}{(R_0+R_1+R_2+R_3+R_4)^2} = 833.33\mu V \tag{3.20}$$

$$\sigma_{VH} = \sqrt{\left(\frac{\partial V_H}{\partial R_0}\sigma_{R_0}\right)^2+\left(\frac{\partial V_H}{\partial R_1}\sigma_{R_1}\right)^2+\left(\frac{\partial V_H}{\partial R_2}\sigma_{R_2}\right)^2+\left(\frac{\partial V_H}{\partial R_3}\sigma_{R_3}\right)^2+\left(\frac{\partial V_H}{\partial R_4}\sigma_{R_4}\right)^2} \tag{3.21}$$

$$= 8.030mV \tag{3.22}$$

$$\tag{3.23}$$

The calculation for "pump_high_limit" , "pump_low_limit" and the "low_limit" can be done likely.

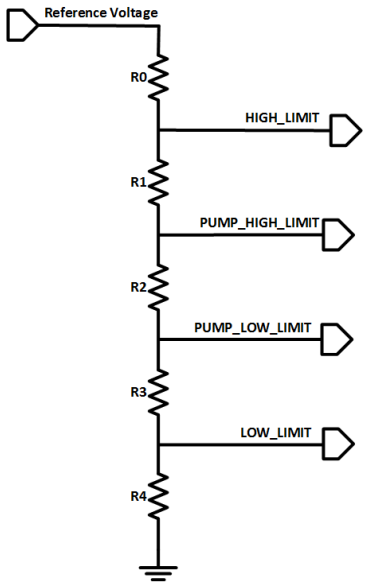

Figure 3.7: Resitive voltage divider for switching thresholds.

3.6 Comparator

To sense the output voltage in a sufficient way, comparators that are built of circuits, like shown in the figure 3.8, are used. The comparator is divided into four parts. At first there is the biasing for the circuit that is implemented by the transistor $N0$ and $N1$. They mirror the given current of $5\mu A$ and $15\mu A$ to the remaining part of the circuit. The second part is the input stage that is built up by the transistor $N2$, $N3$, $N4$, $P1$ and $P2$. A differential pair with diode connected loads are used because it offers a wide bandwidth and is thereby suitable to detect fast rising edges at the input. The lengths of the transistors $N1$ and $N2$ at the input have the minimum allowed length of about $600nm$. This minimum length helps to decrease the input capacitance and hence increases the bandwidth of the input stage. To obtain the high bandwidth and increase the gain by increasing the output resistance of the differential pair, the width of the transistors $P9$ and $P10$ is double that of the transistor $N1$ and $N2$. The fast differential pair suffers from the quite low gain due to the small current of about $5\mu A$ that is used. To make a differential to single ended conversion and increase the gain at the output in order to drive a capacitive load of about $50fF$ at the output, a single ended current mirror OTA is implemented. The comparator has an intrinsic hysteresis that is caused by the $\frac{W}{L}$ difference ratio between the transistors $P1$,$P12$ and the transistors $P7$, $P13$. An analysis of the circuit shows that if $M1$ is on and there is no signal at $M2$ which means it is turned off. The whole current produced by $M5$ is drawn by $M3$ and hence $M6$ tries to force a current that is equal to:

$$i_6 = \frac{\frac{W_6}{L_6}}{\frac{W_3}{L_3}} \tag{3.24}$$

That current raises the potential at the output node v_{o2} until it reaches V_{DD}. If a signal at $M2$ raises the voltage the current flows through, it starts to increase. Now if there is a current i_2 flowing that is equal to i_6, the upper trip point occurs. The sum of the current at the drain of $M5$ is:

$$i_5 = i_1 + i_2 = i_3 + i_6 = i_3 + \frac{\frac{W_6}{L_6}}{\frac{W_3}{L_3}} i_3 = i_3 \left(1 + \frac{\frac{W_6}{L_6}}{\frac{W_3}{L_3}}\right) \tag{3.25}$$

Therefore, the resulting current through transistor $M1$ at the trip point can be stated as:

$$i_1 = i_3 = \frac{i_5}{1 + \left(1 + \frac{\frac{W_6}{L_6}}{\frac{W_3}{L_3}}\right)} \tag{3.26}$$

The current through $M2$ in that case can be calculated by applying the KCL.

$$i_2 = i_5 - i_1 = i_5 - i_3 \tag{3.27}$$

Finally, the upper trip point can be calculated.

$$V_{TRP+} = v_{GS1} - v_{GS2} = \sqrt{\frac{2i_2}{\beta_2}} + V_{T2} - \sqrt{\frac{2i_1}{\beta_1}} + V_{T1} \tag{3.28}$$

Likewise to the upper trip point, the lower trip point can be found and stated as:

$$V_{TRP-} = v_{GS1} - v_{GS2} = \sqrt{\frac{2i_2}{\beta_2}} + V_{T2} - \sqrt{\frac{2i_1}{\beta_1}} + V_{T1} \tag{3.29}$$

With:

$$i_1 = i_5 - i_2 \tag{3.30}$$

$$i_2 = i_4 = \frac{i_5}{1 + \left(1 + \frac{\frac{W_7}{L_7}}{\frac{W_4}{L_4}}\right)} \tag{3.31}$$

[13] This hysteresis is necessary because the voltage at the input of the comparators is in a quite narrow range and thereby a undesired on-off switching behaviour of the comparator should be avoided. A hysteresis of about $6mV$ is a desired value since the voltage is regulated to a voltage range of about $20mV$ and for the absolute upper and lower limits it is in a reasonable tolerance that can be adjusted. The required gain A_0 was calculated by the required voltage levels at the output. A voltage of $1mV$ difference at the output should give the required $3.6V$ in the worst case at the output. A calculation can be done:

$$A_0 = \frac{V_{OH} - V_{OL}}{V_{diff}} = \frac{3.6V - 0V}{1mV} = 3600 \tag{3.32}$$

$$A_{0db} = 20 \cdot log(A_0) = 71.12dB \tag{3.33}$$

The rising edges that occur at the input of the converter are under worst conditions that is when the output voltage is at the "low_limit" edge and the converter applies the $\frac{1}{1}$-divider configuration as high as $612\frac{mV}{\mu s}$. The given system clock that has a period time of $30ns$ gives the upper bound for the required time that the comparator has to make a decision at the output. To make the decision within half of the period time, namely $15ns$, is the final requirement at the comparator timing. In this time the comparator has to make a voltage sweep from $0V$ up to V_{DD}.

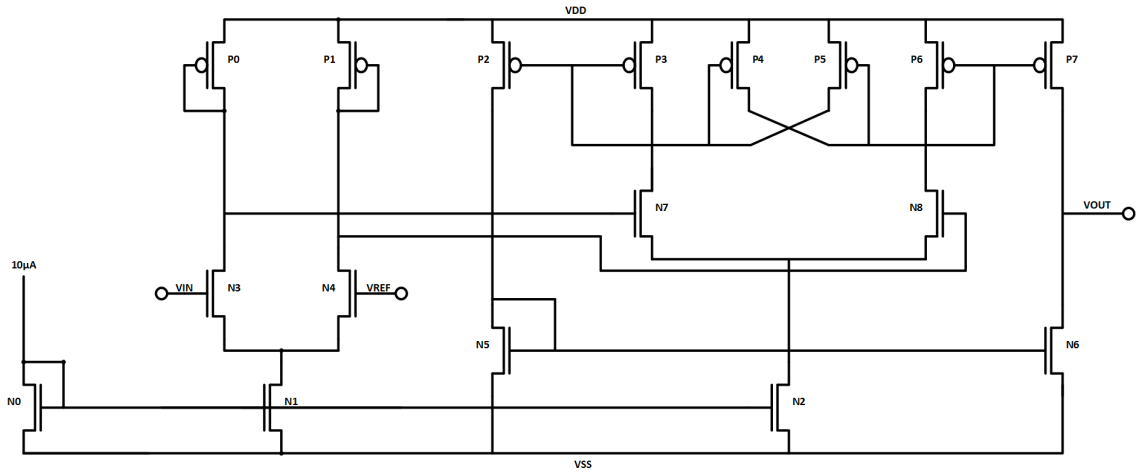

Figure 3.8: Schematic of the used comparator design.

3.7 Divider Networks

The basics of switched capacitor divider networks have already been introduced in 2.3. Here the capacitive conversion from one voltage level at the input to another voltage level at the output is executed. As the chapter 2.2 has shown an inside into the occurrence of losses and their main contributors, these impacts have to be taken into mind when it comes to the design of a switched capacitor divider network. The main design parameters for the divider networks as for switched capacitor converter as a whole are the amount of capacitance for the floating capacitors, the switching frequency at which the converter is operated and the sizing of the transistors that are used as switches. One main parameter that is of interest is the resulting output ripple that occurs at the maximum current load [5]

$$\Delta V = \frac{I_L}{C_{fly}} \frac{T}{2} = \frac{I_L}{2C_{fly} f_{sw}} \tag{3.34}$$

Especially monolithically integrated SC converters have a restricted provided amount of chip area that limits the realizable floating capacitances and thus the frequency has to be scaled up to get a small voltage ripple at a required maximum output current. For the specifications of the target design in this work, a first calculation of the switching frequency can be performed by:

$$f_{sw} = \frac{I_L}{\Delta V \cdot 2 \cdot C_{fly}} = \frac{6mA}{85mV \cdot 2 \cdot 1.05nF} = 33.61MHz \tag{3.35}$$

The scaling of the transistors is done at this switching frequency and a compromise between the losses that occur due to a small transistor that has a higher resistance and a large transistor that has a large parasitic gate-source capacitance has to be made. The fact that a transistor operates as a better switch in terms of the resistance in the triode region can be illustrated with the following formula:

$$I_d = \frac{\mu C_{Ox}}{2} \frac{W}{L} \left[2(V_{gs} - V_t) V_{ds} - V_{ds}^2 \right] \tag{3.36}$$

It shows that beside the voltage across the drain and the source V_{ds} and the voltage across the gate and the source V_{gs} the width of the transistor W is the parameter that has to be made as large and L as small as possible to introduce a high current which can be interpreted as a low resistance. While the resistance decreases the intrinsic gate-source capacitance increases accordingly to [14]:

$$C_{gs} = C_{gd} = \frac{C_{ox} W L}{2} \tag{3.37}$$

A value of $350\mu m$ for the width W of the PMOS switches and $250\mu m$ for the NMOS at a minimum length of $600nm$ for the NMOS and PMOS switches compromises the above mentioned trade-off. Figure 3.9 shows a simulation result with respect to the efficiency of the $\frac{1}{2}$ divider at a fixed input voltage of $3.6V$, without active PFM, under $1mA$ load which is shown as the red line, $3.5mA$ as the yellow line and $6mA$ load that is represented by the green line. The width of the switching transistors has been swept from $20\mu m$ up to $600\mu m$. The variable WPT states the width of the PMOS transistors, the NMOS widths WNT where changed accordingly to $WNT = WPT \cdot 1.5$ and also the buffer transistor sizes where adapted simultaneously to keep the switching transactions in balance. It shows that a width of more than $250\mu m$ does not result in a better overall efficiency instead it gets worse after that value. This trend comes due to the relative high switching frequency and the circumstance that the losses due to the switching procedure increase as well as the losses due to the bottom plate, as already highlighted in the chapter 2.2. Those losses can be found in the SC DC-DC converter model as a parallel resistor. If the width is chosen too small than the losses that are modelled as a series resistance, namely the losses in the switches and the capacitive losses due to the voltage ripple, start to dominate and decrease the efficiency rapidly. Another observation that can be seen from figure 3.9 is that the efficiency is in general higher at higher loads. This property of the divider network is also attributable to the losses that occur in the parallel resistor of the converter model. These losses are always present and in terms of efficiency gets more severe under a light load condition like the $1mA$ at the output. Hence the decrease in efficiency that is due to the losses in the gates of the switching transistors and buffers that are needed to switch them appropriately get smaller as the width of the transistors get smaller, another phenomenon that can be observed in the figure.

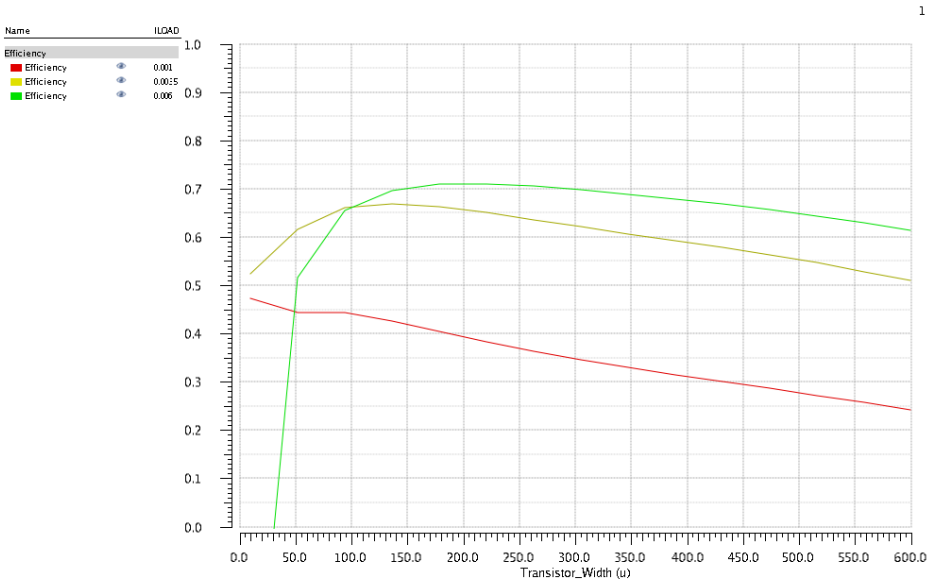

Figure 3.9: Variation of the width of the WPT of the PMOS switches versus resulting efficiency.

Figure 3.10 shows the resulting output voltages of the converter under the loading condi-

tions $1mA$, $3.5mA$ and $6mA$ with different transistor widths. It displays the fact that the output voltage in general decreases as the load increases independent from the transistor width. Referring to the converter model again, it shows that the converters output voltage is made up by a resistive voltage divider between the load resistance R_{load} and the intrinsic series resistance R_{sw}. Hence as the load current increases which can be interpreted as a decrease in R_load, the voltage at the output starts to drop too. Another trend that can be monitored is that there is a width that the transistors need to have because otherwise not enough current would be delivered in order to supply the load and the output voltage drops significantly.

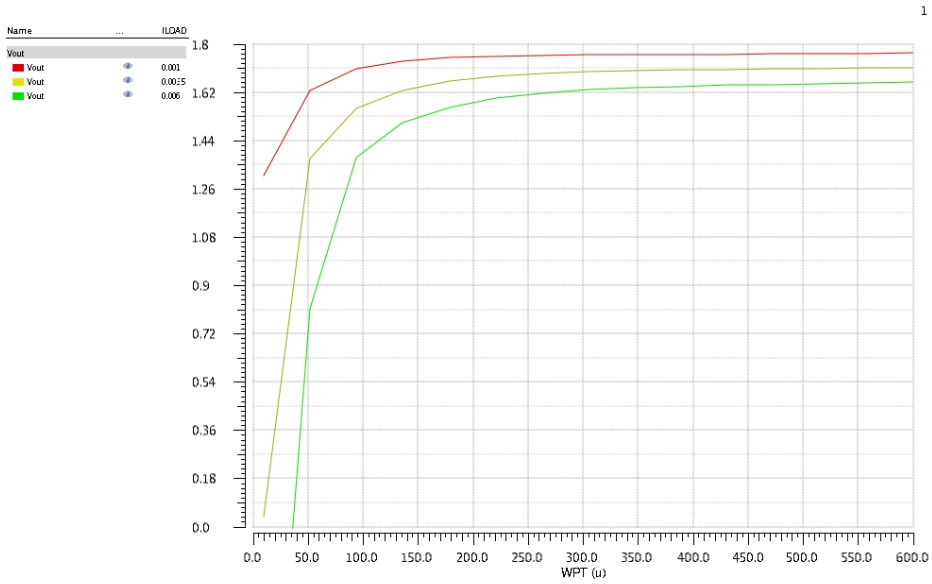

Figure 3.10: Variation of the width of the WPT of the PMOS switches versus output voltage.

A similar observation can be made in figure 3.11. Below a certain width, namely $100\mu m$, the voltage ripple at the output starts to increase drastically. Referring to figure 3.9 and efficiency the reason for the drastic decrease at smaller transistor width can be found in the voltage ripple that is an indicator for the capacitive losses.

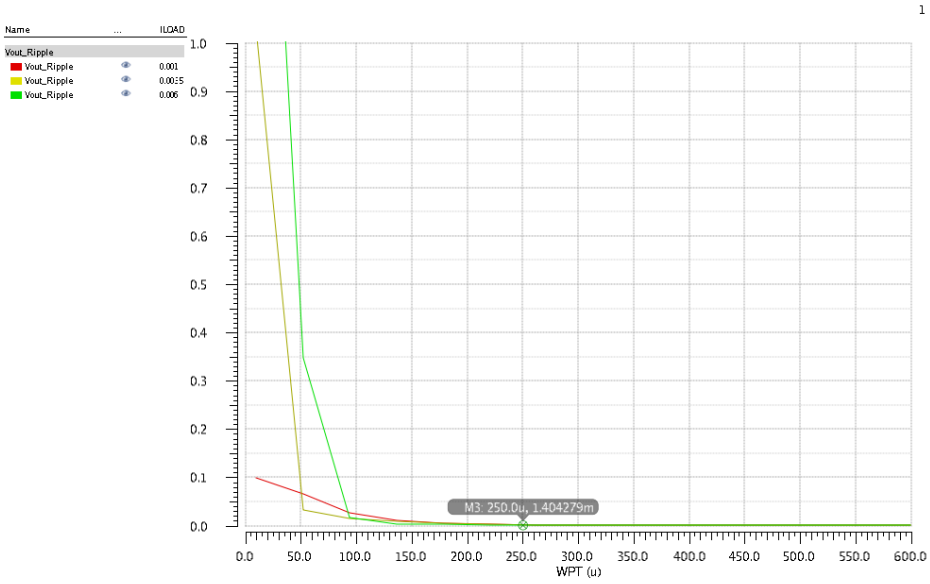

Figure 3.11: Variation of the width of the WPT of the PMOS switches versus output voltage ripple.

A general consideration with respect to the given input voltage range is that the network has to be able to perform more than just one VCR. From the maximum input voltage of $3.6V$ down to $1.8V$ the output voltage has to be in the range of $1.42V$ to $1.6V$. Chapter 2.4.1 shows that there is a relationship between the numbers of floating capacitors and the possible ideal voltage conversion ratios that can be realized. The trade off between choosing an adequate number of floating capacitors and a possible suboptimal operation range of the converter has to be made. The converter in this thesis uses two divider networks like it is shown in figure 3.12. One network is able to realize the iVCRs $\frac{1}{1}$,$\frac{3}{4}$,$\frac{2}{3}$ and $\frac{1}{2}$ by using three poly-poly capacitors of the size $175pF$ as floating capacitors. The converter networks operate in a 45°-phase shifted interleaved manner in order to reduce the voltage ripple and reduce the losses caused by it.

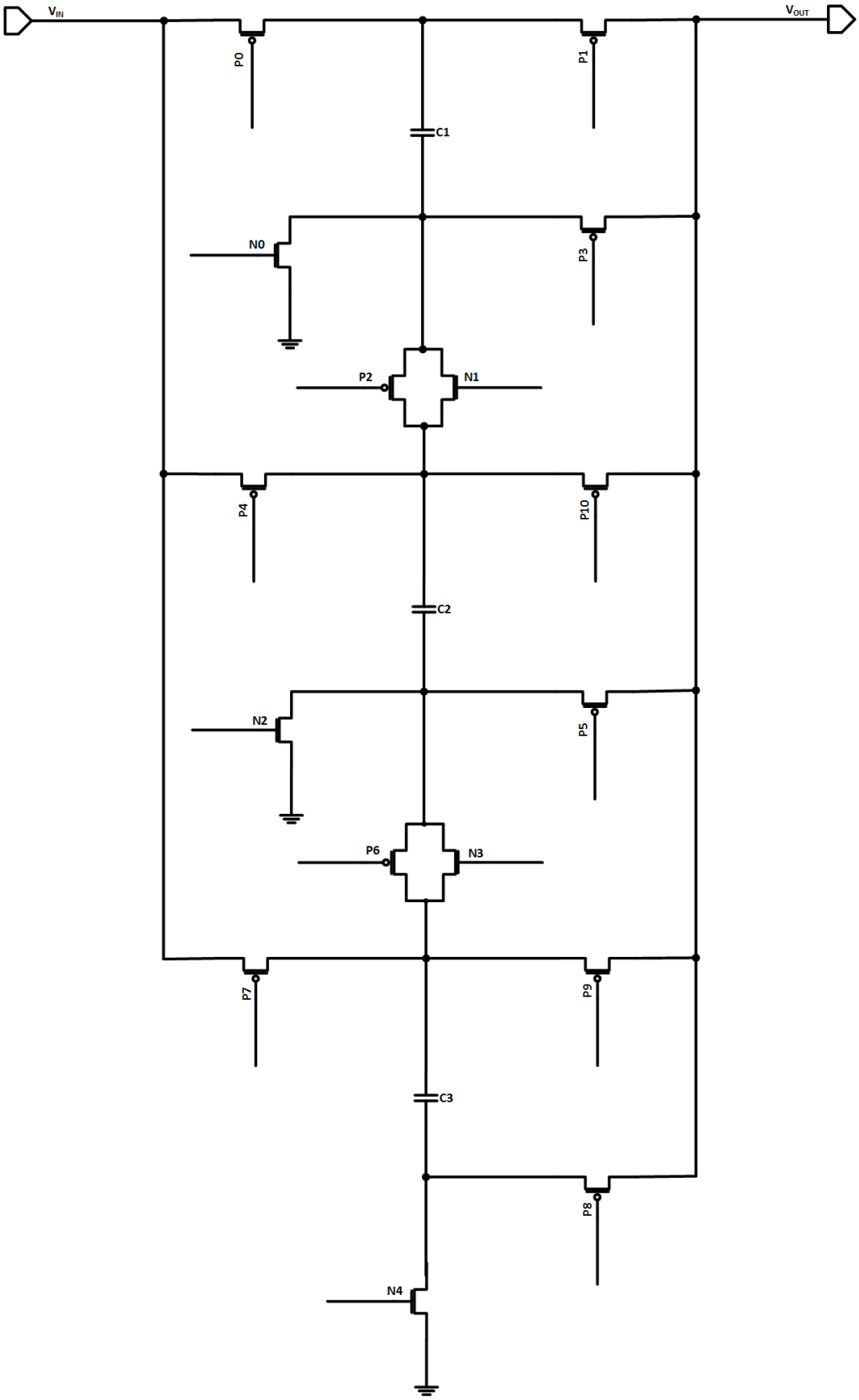

Figure 3.12: Configurable switched capacitor divider network for gain 1, $\frac{1}{2}$, $\frac{2}{3}$ and $\frac{3}{4}$.

The 16 switches are turned on or off by the "gate_logic" cell that includes a decoder and the switch drivers. According to the present divider configuration and the required charging phase, table 3.7 shows all possible required constellations of switches and their activity.

	1/1		3/4		2/3		1/2	
	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2
P0	1	0	1	0	0	0	0	0
P1	0	1	0	1	0	0	0	0
P2	0	0	0	1	0	0	0	0
P3	0	0	1	0	0	1	0	0
P4	1	0	1	0	1	0	0	0
P5	0	0	1	0	1	0	0	0
P6	0	0	0	1	0	1	0	0
P7	1	0	1	0	1	0	1	0
P8	0	0	1	0	1	0	1	0
P9	0	1	0	0	0	0	0	1
P10	0	1	0	0	0	1	0	0
N0	1	1	0	0	0	0	0	0
N1	0	0	0	1	0	0	0	0
N2	1	1	0	0	0	0	0	0
N3	0	0	0	1	0	1	0	0
N4	1	1	0	1	0	1	0	1

Table 3.1: Switch status in the activated divider configuration and charge phase.

3.8 Switch Driver

The used switches of $350\mu m$ respectively $200\mu m$ require an adequate driver circuitry to obtain that the two phases of one divider network do not overlap. Therefore, the timing constrain of loading and unloading the gate capacitance has to be fulfilled. Chapter 3.2 shows that the time between the charge and discharge phase is set to $1.5ns$. That causes the requirement for the rise time respectively the fall time. The propagation delay in the sense of efficiency is not that critical since only the mixture of both phases in one divider has to be avoided. In order to achieve the specified requirements, cascaded buffers are used to obtain a low input capacitance and hence fast settling times in the first inverter stage and a higher output current by the output inverter to switch the large transistors on and off as needed. That gives all transistors where sized at minimum length L, the PMOS transistors have about 1.6 times higher W and the output inverter is about 3 times larger than the input inverter. The final sizes of the transistors were determined by a sweep of the width while obtaining the mentioned relations to each other and a connected capacitive load of about $1pF$, the results are shown in the chapter 4.7.

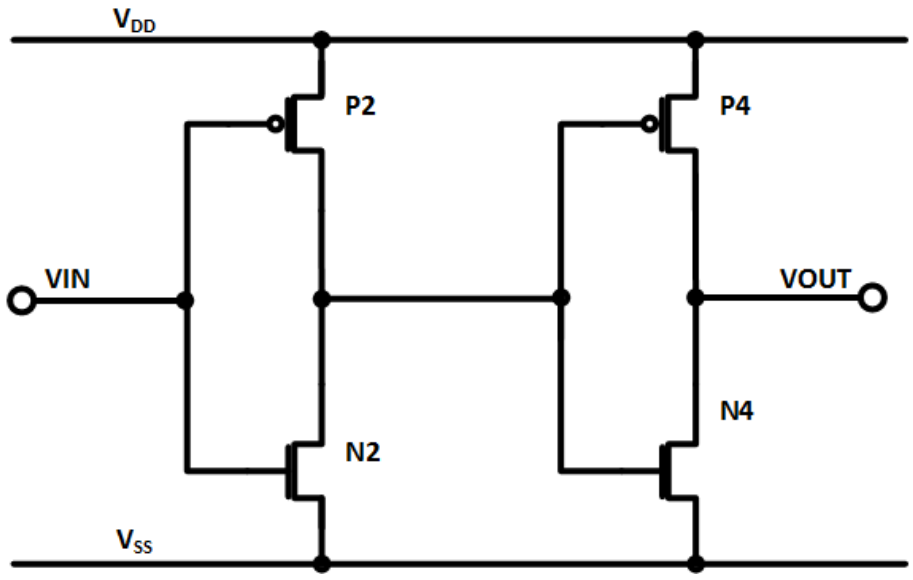

Figure 3.13: CMOS buffer structure.

3.9 Control Unit

The control unit is responsible to make a decision in which configuration the divider network should be operated and how many charging pumps have to be executed. It consists of logic gates at the input that detect the condition of the output voltage and give further signals. If the output voltage is detected at the "high_limit" or at the "low_limit", a promptly switch from the current divider configuration has to be performed. A higher one if the voltage has dropped below the "low_limit" or a lower divider in case a "high_limit" was detected is applied. Furthermore, the "control_unit" recognizes the output voltage in the range of $1.45V$ and $1.5V$ and the time it remains there with two $6-bit$ counters. The counted values are forwarded to a decoder that give a signal according to the load respectively pump condition. A $2-bit$ counter at the output realizes the 4 divider configuration signals for the further circuitry.

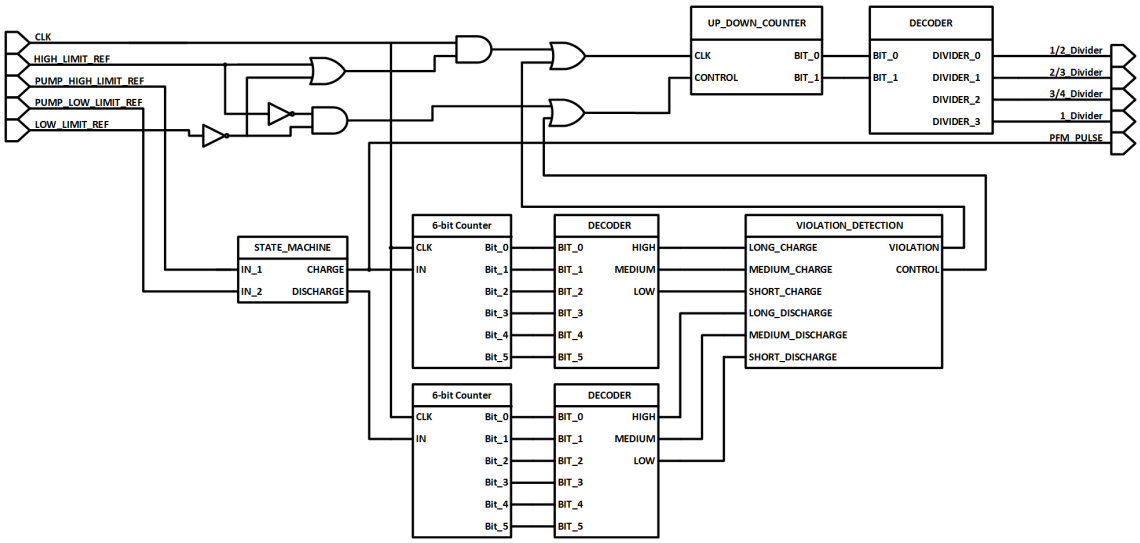

Figure 3.14: Block diagram of the control unit.

Due to the high switching frequency that is necessary to fulfil the requirements on the converter, the losses that occur to charge and discharge the MOSFET transistors can be significant, dominating in the lower load region around $1mA$. To reduce those losses that occur permanently to charge and discharge the gate capacitances of the switches and the driver buffers, a control scheme is applied. A direct measurement of the load current is not beneficial since a resistor that would be necessary at the output would always reduce the efficiency by further decreasing the resulting voltage at the output. Nonetheless, to achieve a high as possible efficiency over the whole operating range an estimation about the current that unloads the output capacitance is made by observing the time that is necessary to switch between the end and the begin of a discharge phase that is set by the "pump_high_limit" and "pump_low_limit". The time that is necessary to load the capacitance indicates if the current divider configuration is appropriate for the loading condition. It is desirable to have a continuously switching converter at high loads and a rather burst charging behaviour at the lower loads to obtain a proper efficiency.

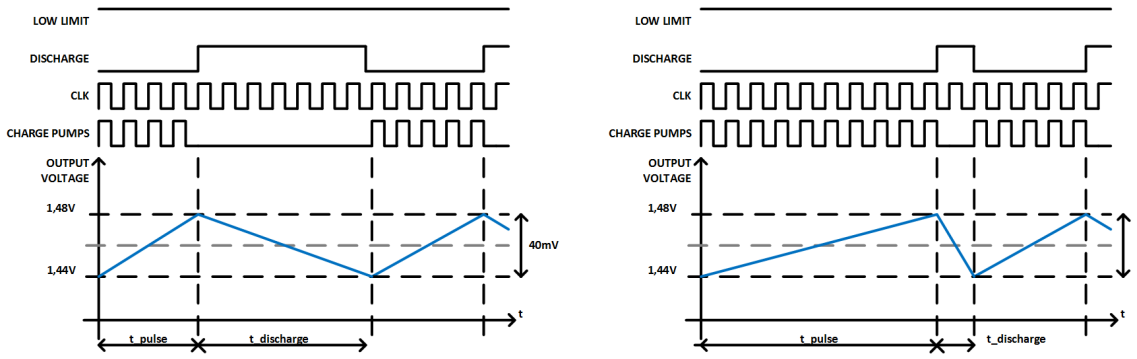

Figure 3.15: Timing diagram of the control logic concept. The left side shows the resulting behaviour of the converter under low load conditions. Whereas the right side shows how the converter acts under high loading conditions.

Figure 3.15 illustrates the basic idea of the concept. The blue line shows the output voltage that is regulated to stay within the $1.5V$ and $1.45V$. The observed time $t_{discharge}$ categorizes the current at the output into a "low_load", "medium_load" or "high_load" condition. According to the three quantized values, the range for the charging pumps is set. If a not adequate number of charge pumps under a specific load condition is performed, the "control_unit" initializes a change to another divider configuration.
The quantization of the load current is done by counting the number of clock cycles $\#cylces$ within the according phase that gives an Δt with respect to the voltage difference between the "pump_high_limit" and the "pump_low_limit" that gives an ΔU which results in an average discharging current I

$$I = C \cdot \frac{\Delta U}{\Delta t} \tag{3.38}$$

$$\Delta t = \#cylces \cdot \frac{1}{f_{sw}} \tag{3.39}$$

The counted $\#cylces$ are then forwarded to a decoder that gives a "high_load", "medium_load" or "low_load" condition signal. The same procedure is done to get a "low_cycles", "medium_cycles" and "high_cycles" signal that states the required range of number of cycles in the charging phase t_{pulse}.

Chapter 4

Simulation Results and Layout

In this chapter finally the simulation results of the implemented converter are provided. First, the results of the separated blocks under specific conditions and different corners are presented. The performance of the "non_overlapping_clock", "delay", "PFM", "threshold_generation", "comparators" and the "sc_divider_circuit" cells are shown and discussed in detail. Special focus is on the divider network configurations with respect to the achieved efficiency. Further, the whole system, respectively the converter is operated, under the specified conditions and its behaviour is analysed. The proposed converters layout and considerations to it are given.

4.1 Non Overlapping Clock Generation

To examine the behaviour of the non overlapping clock generation block "non_overlapping_clk" a transient analysis was performed with the input signal clk with a frequency of about $f_{clk} = 33MHz$ and the resulting output signals "phase_01" and "phase_02" were observed at a supply voltage of $V_{DD} = 3.6V$. As can be seen in the figure 4.1 the block performs a dead time between "phase_01" and "phase_02" that is about $1.28ns$ and $1.52ns$. The small difference of about $240ps$ comes due to the additional inverter gate at the "phase_02" that introduces a small delay. The simulated rise and fall times of the input clock signal were set to $1ps$ due to that a short overshot of about $300mV$ peak can be seen. All in all, the non overlapping clock generation block consumes $87.93\mu W$ at a supply of $3.6V$ during operation.

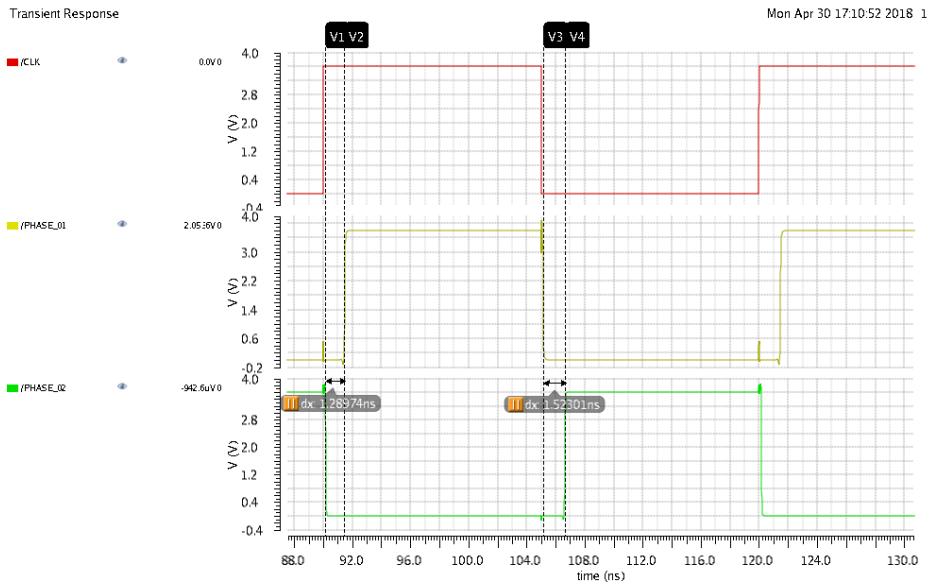

Figure 4.1: Transient analysis of the non-overlapping clock generation block.

4.2 Delay

The cell to generate the delay named "delay" is verified by a transient analysis in that a clock signal with a frequency of $f_{clk} = 33MHz$ is applied and the delayed output signal is observed. Figure 4.2 shows the simulation result of the transient analysis. It shows that the rising respectively the falling edge of the signal is larger since the maximum peaking current is limited. That results in decrease of the overall power consumption of $46.8\mu W$ at a supply voltage of $V_{DD} = 3.6V$

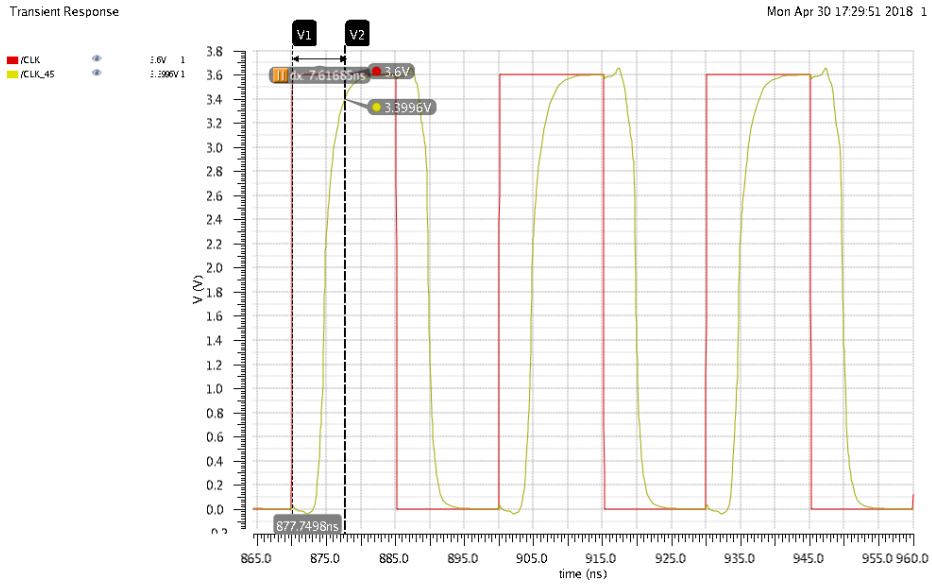

Figure 4.2: Transient analysis of the delay block.

4.3 PFM

To verify the correct behaviour of the "PFM" block a transient analysis was performed with a "vref_pump" input signal that simulates a transition at the input that the output voltage has crossed the reference voltage for further charge pumps. As can be seen in figure 4.2, the non-overlapping clock phases "pfm_phase_01" and "pfm_phase_02" are performed during the time the input signal is low and stops to deliver charge pumps when it is high. It has to be mentioned that the "pfm_phase_02" has to stay at the V_{DD} voltage cause of the use of PMOS transistors.

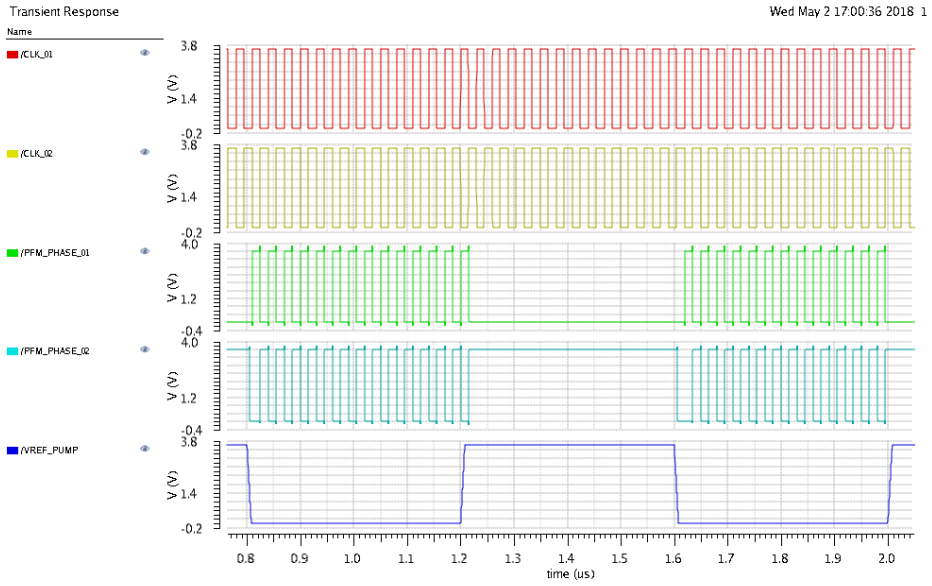

Figure 4.3: Transient analysis of the pulse frequency generation block.

4.4 Threshold Generation

For nominal conditions the calculated values for the thresholds, namely 0.8V, 0.74V, 0.72V and 0.7V, were also observed in a DC simulation. In order to analyse the resulting deviation of the reference voltage levels at the resistive voltage, a monte carlo analysis with 1000 runs was performed. The results can be seen in figure 4.4. As it can be seen, the values of the resulting voltages are nearly normal distributed and the $\pm 3\sigma$ range is between $795.793mV$ and $804.334mV$ this deviation of up to $8.541mV$ is close to the calculated one in chapter 3.5. With the given process parameters and the single resistor dimension in μm a $\pm 3\sigma$ a range of about $8.030mV$ was calculated. It has to be mentioned that the values in the Monte Carlo analysis are not perfectly independent and the value of 1000 runs might be marginal.

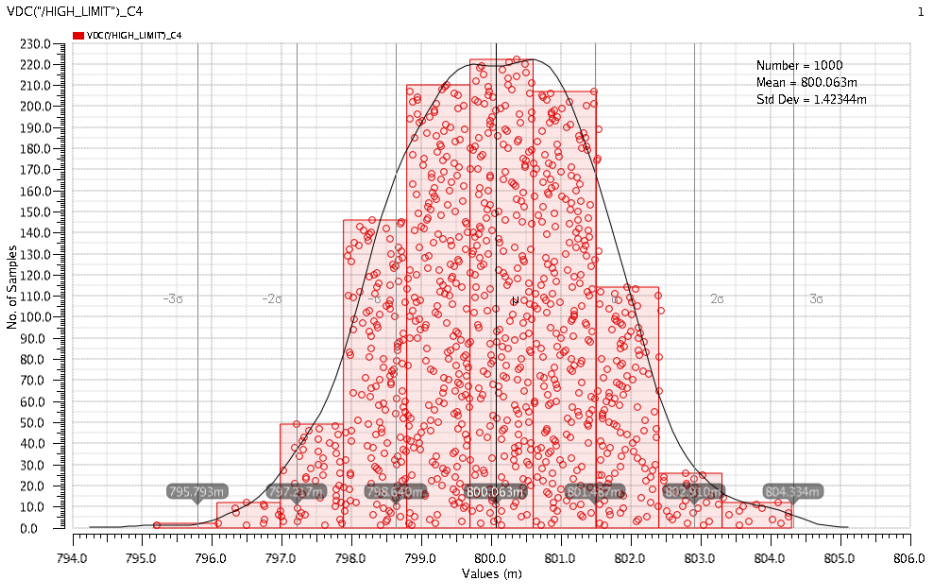

Figure 4.4: Monte Carlo analysis of the HIGH_LIMIT threshold voltage.

4.5 Comparator

Figure 4.5 shows the gain of the comparator with respect to the input signal frequency of up to $2GHz$. The supply voltage has been set to $1.6V$, the "reference" input was set to $750mV$ and a sinusoidal input signal with $750mV$ DC offset and a amplitude of $1\mu V$ was applied. The simulation shows that the comparator has a $-3dB$-bandwidth of about $1.2MHz$ and a unity gain frequency of $246MHz$ while obtaining an open loop gain of about $74dB$. The comparators bode plot shows the combination of the fast input stage and the slow output stage which result in a higher order system behaviour. This can be determined due to the fact that the magnitude starts to decrease with about $-20dB$ per decade until the second and third poles start to decrease the magnitude further with up to $-60db$ per decade which gives a third order system. Also the phase starts to decrease with about $-45°$ until the other poles start to kick in. A phase margin of about $89°$ can be measured which gives a stable overall comparator system. Since the comparator uses a kind of positive internal feedback the stability criteria has to be fulfilled.

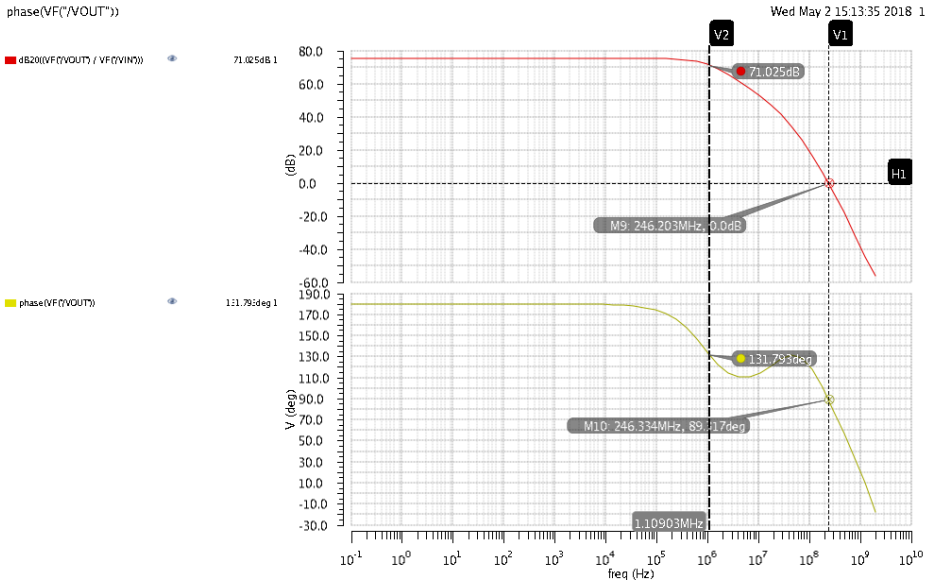

Figure 4.5: Gain of the comparator structure over the whole frequency range.

To verify the internal hysteresis, a DC simulation was performed to see the tripping points of the comparator. Especially the variation under different process corners has to be taken into mind. Therefore the simulation was performed with different process corner options, a supply voltage of $V_{DD} = 3.6V$ and a reference voltage of $750mV$ at the reference input. Figure 4.6 shows the results of the DC simulation. It can be observed that the comparator changes the output level in less than a $1mV$ difference with a hysteresis between $5mV$ and $8mV$ depending on process variations.

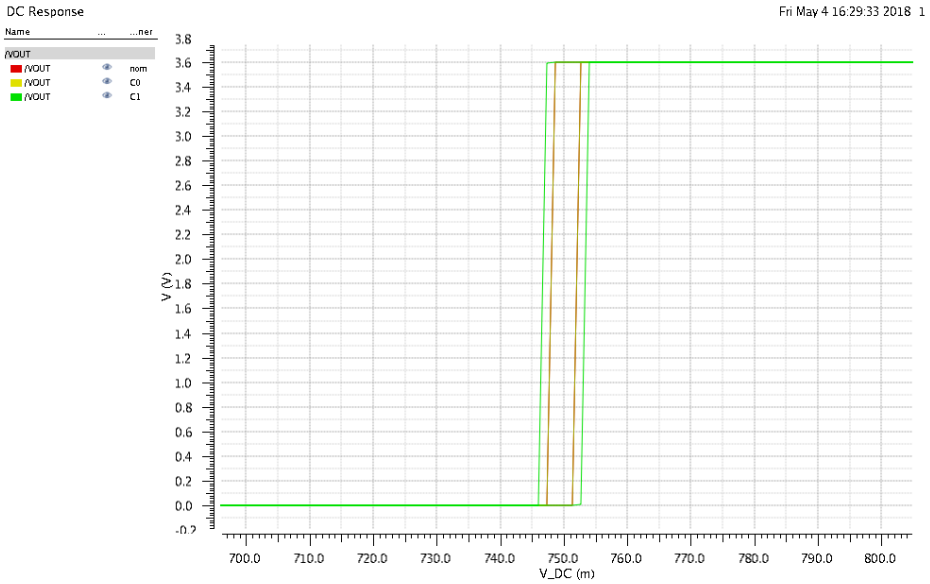

Figure 4.6: Hysteresis of the comparator under different process corners.

To verify that the delay time is also within the required limits, a transient simulation was performed to see the worst occurring deviation from the ideal value. The highest deviation will be introduced by the highest slope at the output voltage that the comparator has to sense. This is already specified in chapter 3.6 and can be up to $612\frac{mV}{\mu s}$. Therefore, an input signal with this maximum rising time respectively fall time has been applied to the input of the comparator and a compare value of $750mV$ additionally the supply voltage has been set to $1.6V$ and $3.6V$ to see further dependencies. In figure 4.7 the resulting signals can be seen. A maximum deviation of about $6mV$ to the absolute value and a possible difference between the rising edge and falling edge trigger of about $12mV$ can be observed. These values have to be considered when it comes to the absolute values for the limits of the thresholds for the hysteric control unit.

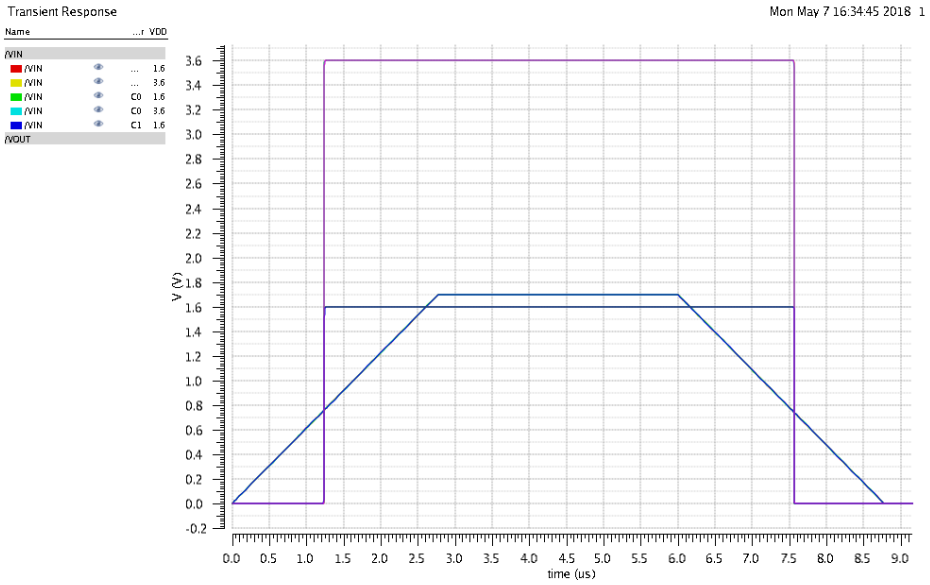

Figure 4.7: Transient simulation of the comparator at $1.6V$ and $3.6V$ at a ramp of $612\frac{mV}{\mu s}$.

Finally, four comparators with the desired input voltage references of $0.8V$ for the "high_limit", $0.74V$ for the "pump_high_limit", $0.72V$ for the "pump_low_limit" and the $0.7V$ for the "low_limit" are verified that build up the "comparators" cell. The procedure is the same as for one comparator with the difference that the input references are already supplied by the "threshold_generation" cell. Thereby by a first look at the overall deviations of the overall threshold detection of the output voltage can be taken. Figure 4.8 shows the result of the DC simulation that was performed to verify the thresholds and hysteresis of the subsystem. It shows that the maximum occurring deviation of the hysteresis is between $8.43mV$ and $10mV$.

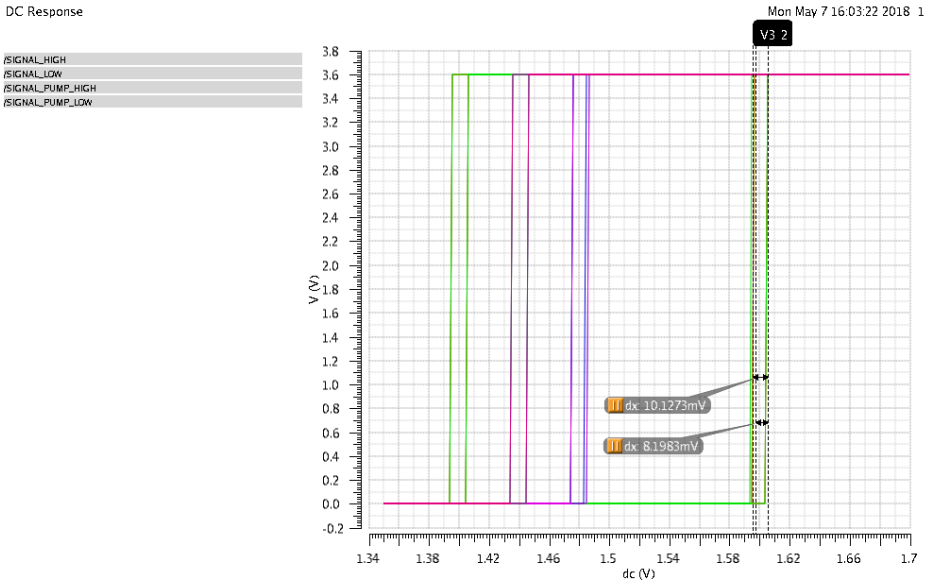

Figure 4.8: Threshold of the comparators hysteresis.

The following figure 4.9 shows the fastest possible slope at the input of the comparators and the resulting switching levels of every comparator. It shows that the maximum deviation of the actual switching level to the ideal one can be as high as $10mV$ with respect to the input voltage. This failure comes from the input delay of the comparators and is acceptable since it occurs only at the worst condition when the comparator charges at a battery voltage of $V_{DD} = 3.6V$ and at a load of $1mA$ with $\frac{1}{1}$-divider configuration. That pump behaviour is only applied if the converter has observed a violation of the "low_limit" which is only the case if the battery voltage has already dropped to lower values.

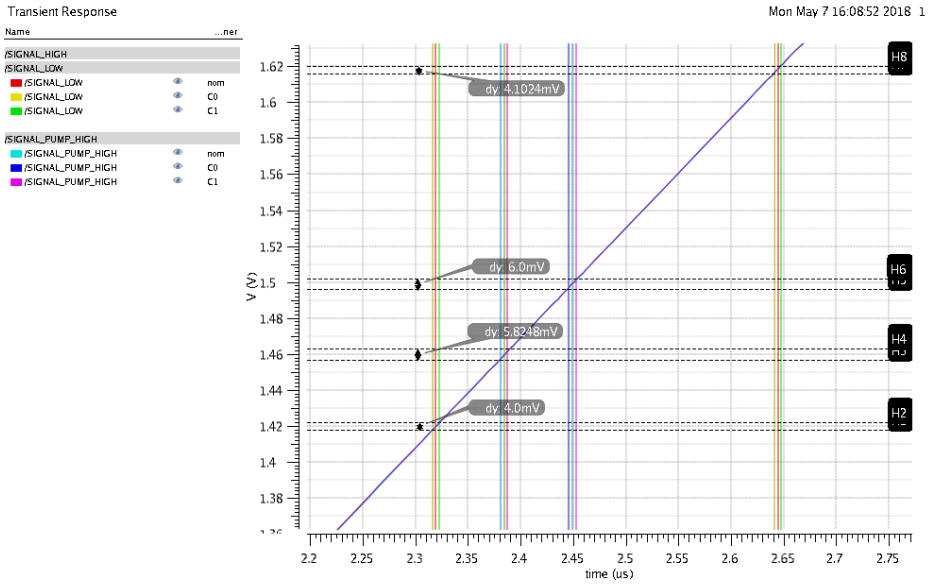

Figure 4.9: Thresholds on the rising edge of the fast transient.

4.6 Divider Networks

The realized divider configurations 1, $\frac{3}{4}$, $\frac{2}{3}$ and $\frac{1}{2}$ were simulated by manually configuring the required signal condition to force the converter to operate in a specific divider ratio. Thereby the output voltage and the maximum reachable efficiency are of the most interest to see what input voltage ranges the divider can handle and what efficiency is maximum achievable in an autonomously working converter. This section also stresses the fact that there is a need for a control circuitry that decides for the right divider configuration to keep the output voltage at a specific operating point within the specifications. Also the efficiency is strongly dependent on the load current if no further countermeasures are taken.

4.6.1 3/4 Divider

Figure 2.8 shows the resulting output voltage at the converter output over different input respectively supply voltages. Under a continuously switching behaviour the converters output voltage can be feasible for input voltages between $1.9V$ and $2.31V$ depending on the loading. It shows that there is always a small difference between the resulting output voltage and the iVCR that is almost constant over the whole voltage range and depends on the load current condition. Under a $1mA$ load condition that gives an equivalent series resistance of about 35Ω which contains the capacitive conversion losses and the on resistance switching losses. It shows as the loading condition changes to higher loads the output voltage drops because it can be interpreted as a small resistor at the output that lowers the voltage divider that is set up by the load and the series output resistance of the converter, as already described in 2.2.

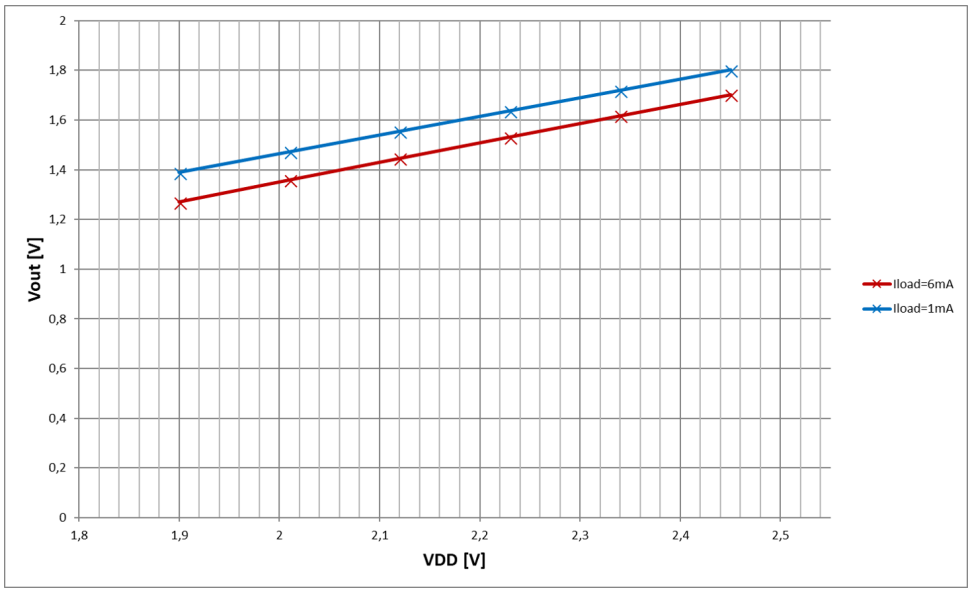

Figure 4.10: Output voltage of the $\frac{3}{4}$-divider configuration under steadily switching condition.

The observed resulting output voltage and hence the VCR is a measure for the maximum achievable efficiency η according to [4]

$$\eta_{max} = \frac{VCR}{iVCR} \tag{4.1}$$

That gives for the $\frac{3}{4}$-divider a $\eta_{max} = \frac{0.731}{0.75} = 0.974$ under a $1mA$ load this means, a loss of about 2.4% occurs due energy conversion in an ideal converter with that VCR. In a converter which is realized with MOS capacitors additional losses occur due to the parasitic bottom plate loss depending on the ratio of parasitic to used capacitance that can cause losses of up to 15% like it is shown in [11]. Figure 4.11 shows the observed efficiency of the $\frac{2}{3}$-divider. As can be seen the divider configuration enables an efficiency of up to 78% under a $6mA$ loading condition and a maximum of about 50% under a $1mA$ load. The maximum efficiency is limited by the already mentioned factors. Under a high load condition the efficiency is limited due to the systematic conversion penalty and the bottom plate losses. A light load condition is more critical due to the big switches and therefore big driver buffers that are switched with a quite high frequency of $30MHz$. As already mentioned in 2.2 these losses also scale with the supply voltage, a higher supply voltage gives an even worse efficiency.

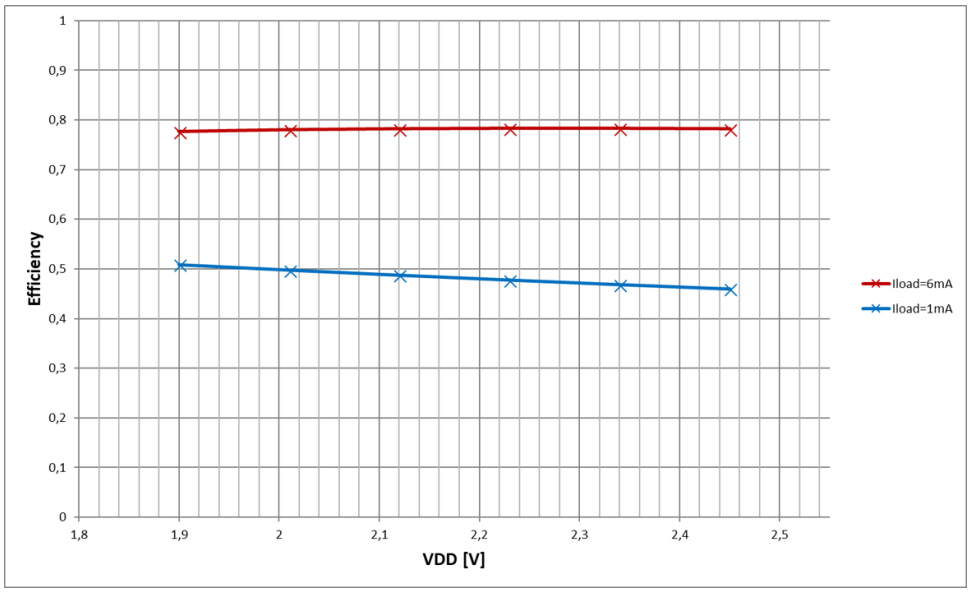

Figure 4.11: Efficiency of the $\frac{3}{4}$-divider configuration under steadily switching condition.

4.6.2 2/3 Divider

The considerations explained in 4.6.1 are valid for all divider configurations. Hence the behaviour of the $\frac{2}{3}$-divider is similar to that of the $\frac{1}{2}$-divider. Figure 4.12 shows the resulting output voltage of the converter with respect to the input voltage under the two extreme conditions of $1mA$ and $6mA$. As it can be seen, the output voltage can be directly applied for input voltages between $2.25V$ and $2.85V$ depending on the load current. The equivalent series resistance is about 38Ω at a $1mA$ load.

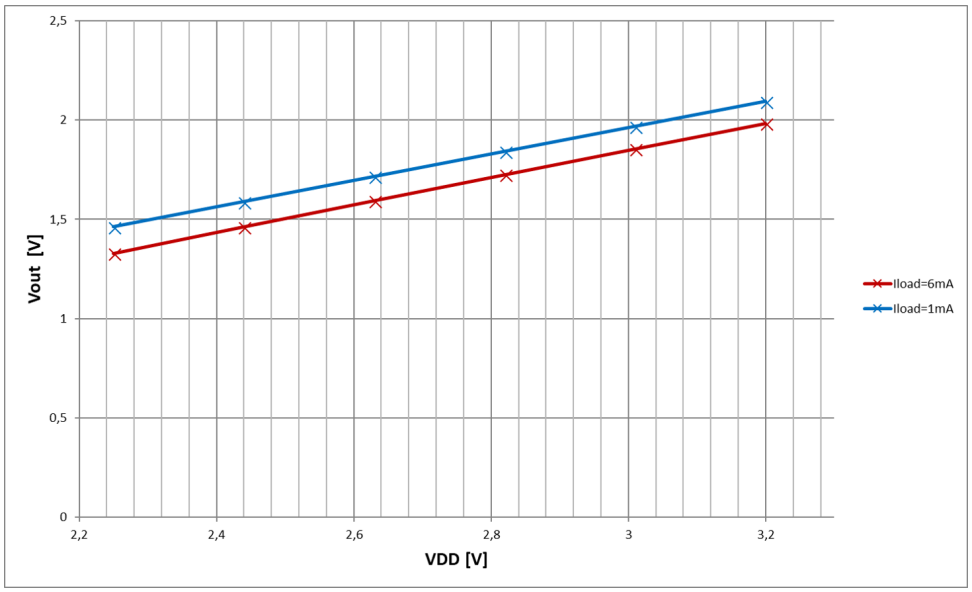

Figure 4.12: Output voltage of the $\frac{2}{3}$-divider configuration under steadily switching condition.

Also the properties regarding efficiency are similar to the $\frac{3}{4}$-divider hence the maximum achievable efficiency with that divider is quoted with $\eta_{max} = \frac{0.656}{0.666} = 0.984$ under a $1mA$ load condition. Figure 4.13 shows the observed efficiency of the converter with a maximum of about 79% at a high load of about $6mA$ and 55% at a $1mA$ load. Again the load condition with less current at the output is more critical in terms of efficiency.

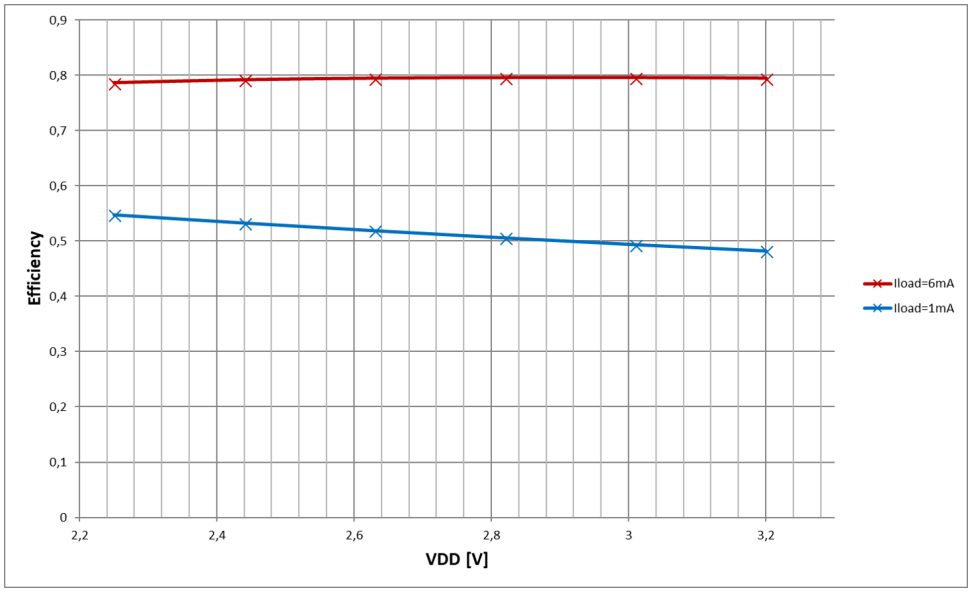

Figure 4.13: Efficiency of the $\frac{2}{3}$-divider configuration under steadily switching condition.

4.6.3 1/2 Divider

The last divider which is analysed is the $\frac{1}{2}$-divider that is determined to transform the high occurring battery voltages down to the $1.5V$ domain. Figure 4.14 illustrates the property of the $\frac{1}{2}$-divider configuration. It shows that the output voltage is suitable in a permanently switching behaviour of the converter for input voltages between $2.9V$ and $3.6V$. The voltage ratio achieved under $1mA$ is $VCR = \frac{1.758V}{3.6V} = 0.488$ with an equivalent series resistance of about 42Ω.

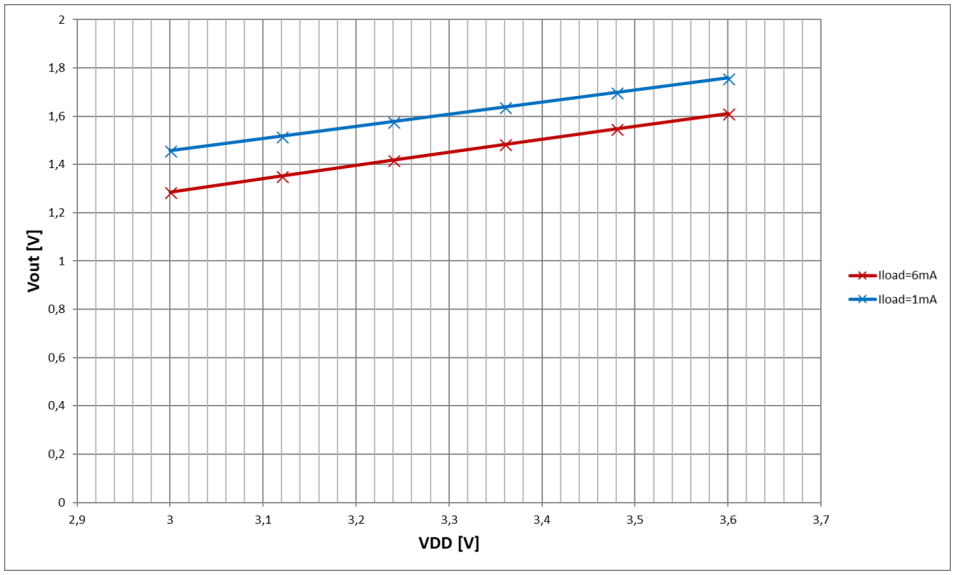

Figure 4.14: Output voltage of the $\frac{1}{2}$-divider configuration under steadily switching condition.

Similar to the previous mentioned divider configurations figure 4.15 shows the efficiency of the $\frac{1}{2}$-divider under different input voltages. The maximum efficiency of about 80% is achievable under the high load condition of about $6mA$ and about 59% at the lower loads.

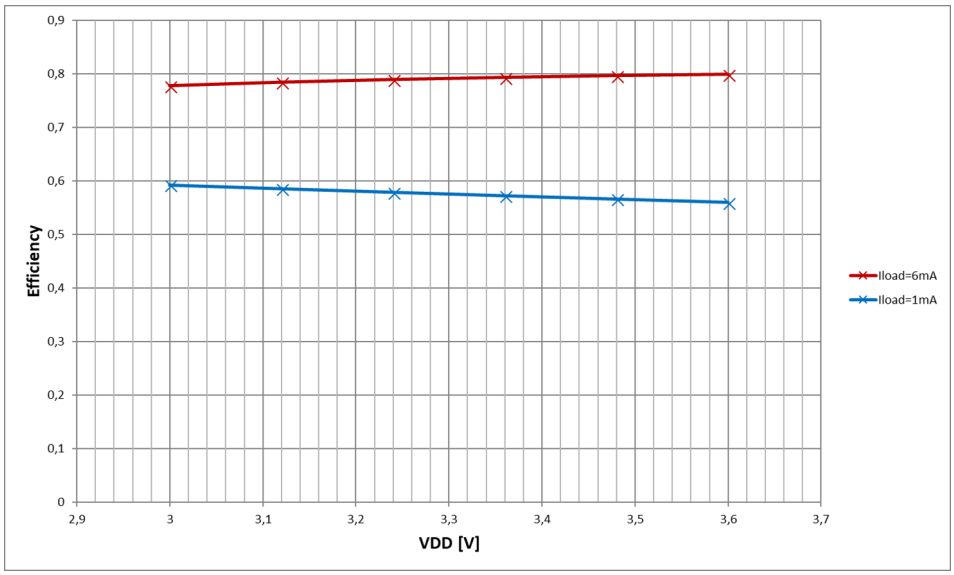

Figure 4.15: Efficiency of the $\frac{2}{3}$-divider configuration under steadily switching condition.

4.7 Switch Driver Buffers

To see if the switch driver buffers are dimensioned sufficiently, a transient analysis under different process corner conditions was performed. At an input voltage of $V_{DD} = 3.6V$ a rectangular input signal with a frequency of $f_{sw} = 33MHz$ was applied and the resulting signals at the output with a load of $C_{load} = 1pF$ were visualized. Figure 4.16 shows the simulation result. The rise and fall times are in the required range and a deviation due to process variation of about $262ps$ can be seen.

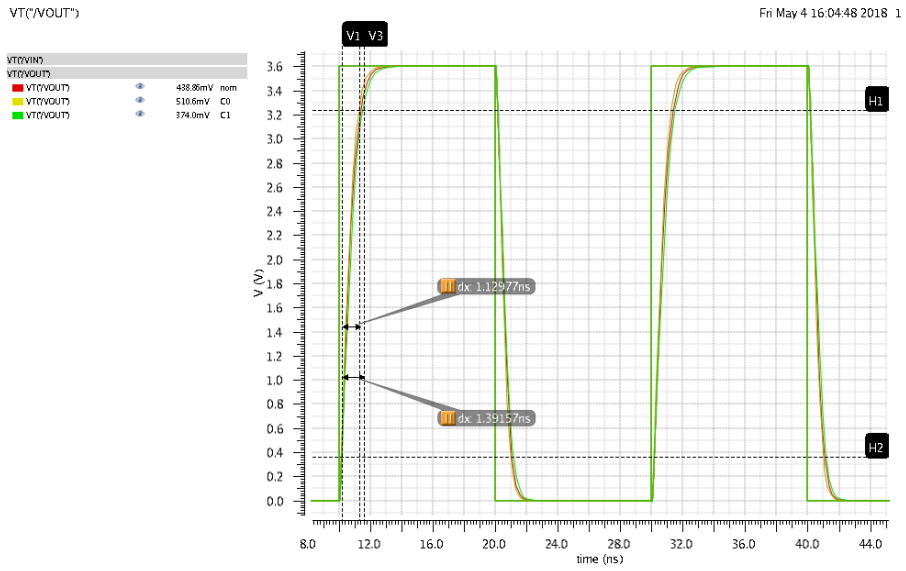

Figure 4.16: Transient behaviour of the gate buffer block.

4.8 Converter Operation and Performance

After analysing all the separated components of the converter isolated from each other an overall verification of the complete system is shown in this chapter. Since there are many signals processed in the converter that are necessary for the functionality but not for the understanding and illustration of the converter operation, just the ones with high importance are shown in the following. Figure 4.17 shows the resulting behaviour of the converter under a $6mA$ load condition and $3.6V$ input voltage. It can be seen that the output voltage stays between $1.44V$ and $1.49V$ the long charging phase is desirable to keep the efficiency high by obtaining just little ΔV per charge phase. Additionally, it can be observed that the ripple ΔV during one pump is quite low and smooth due to the phase shifted converter cells that are implemented. As soon as the converter reaches the "high_pump_limit" it stops further pumps and starts to measure the system clock cycles during the discharge phase respectively the time it needs to get below the "low_pump_limit". As there is a constant load applied at the output a stationary behaviour in which the converter does not change its conversion ratio can be seen.

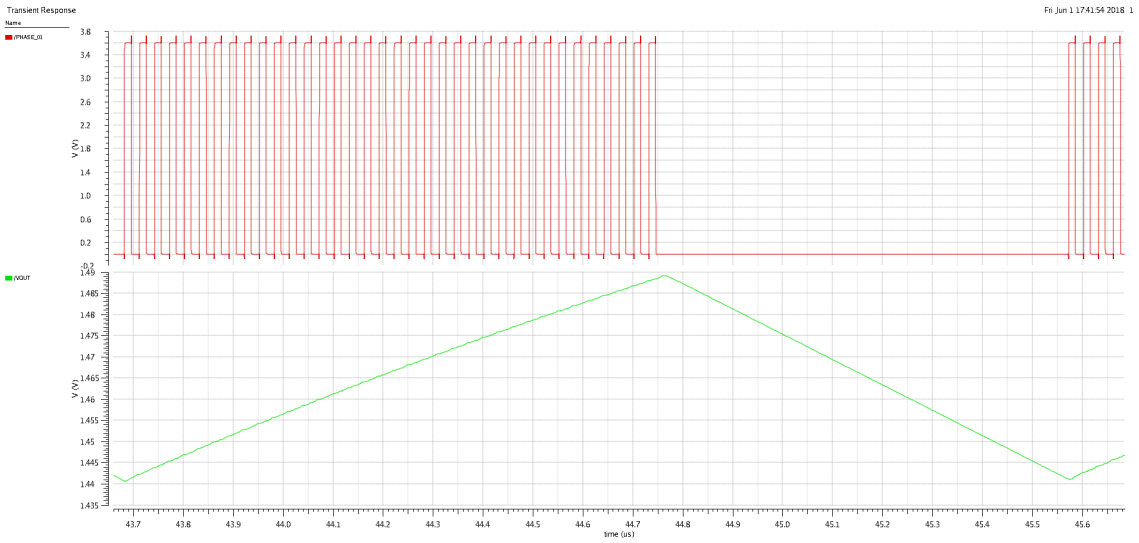

Figure 4.17: Transient analysis of the converter at $6mA$ and $V_{DD} = 3.6V$.

Figure 4.18 shows the converter under a $1mA$ load and a input voltage of about $3.6V$. In such an operating condition the converter holds the output voltage within the specified range by applying only a few pumps. Thus the parasitic losses in the gate source capacitances of the switches and drivers that would occur in a permanent switching behaviour are kept at a minimum.

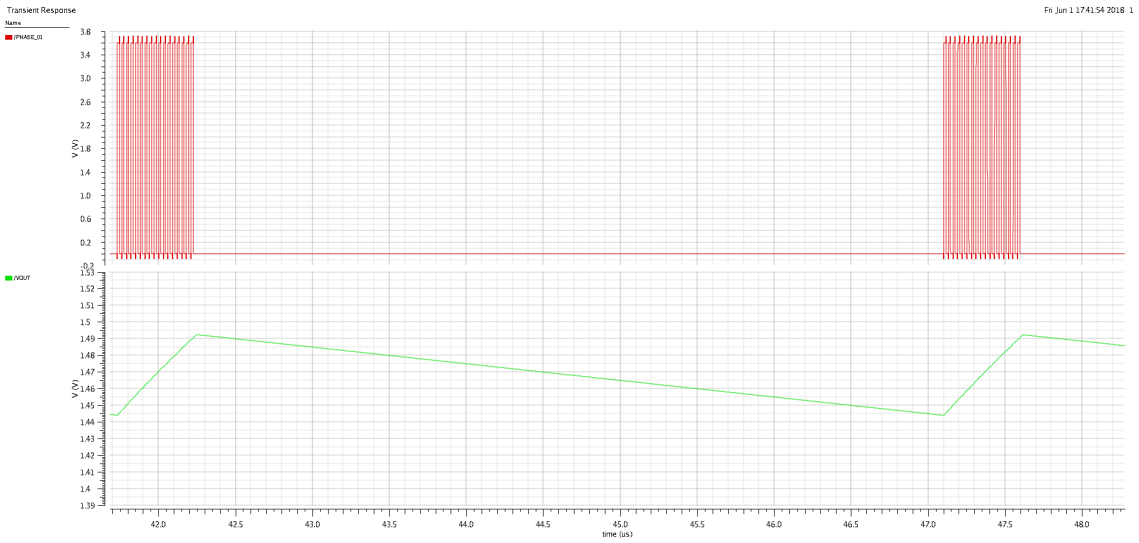

Figure 4.18: Transient analysis of the converter at $1mA$ and $V_{DD} = 3.6V$.

The following figure 4.19 shows the resulting output voltage of the converter over the whole input voltage range between $1.6V$ and $3.6V$. It shows that the converter is able to hold the output voltage within the specified voltage range until an input voltage of about $1.7V$. The variation of the output voltage within the acceptable range is between $1.44V$ and $1.49V$.

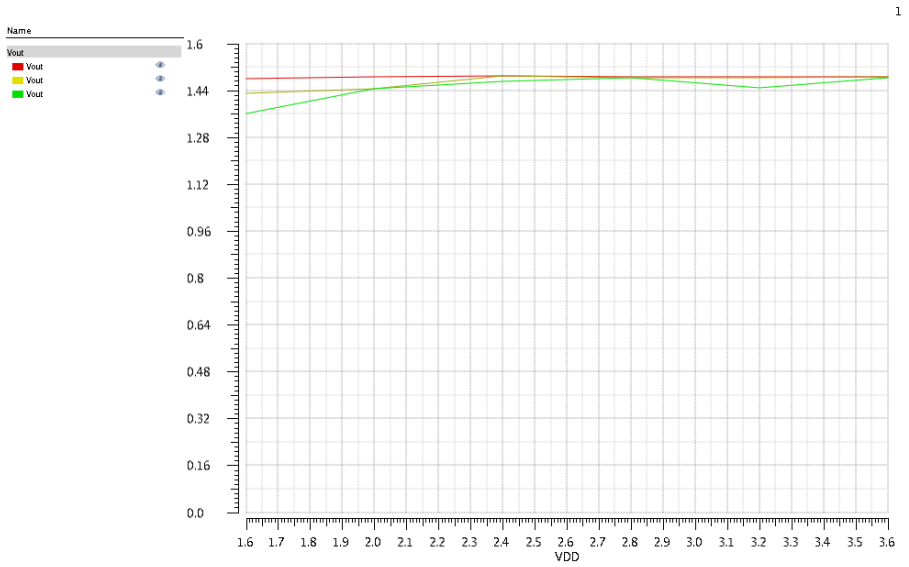

Figure 4.19: Converter output voltage over whole input voltage range.

Figure 4.20 shows the resulting voltage ripple at the converter output. These values depend on the converter divider choice, the comparator voltage level detections and therefore the occurring minimal and maximum voltages. This difference is plotted in the chart and is hence not the ripple as it is usually referred to the difference occurring only in just one charge pump cycle. As can be seen for example in figure 4.18 or figure 4.17, the voltage lifting during one cycle is much smaller.

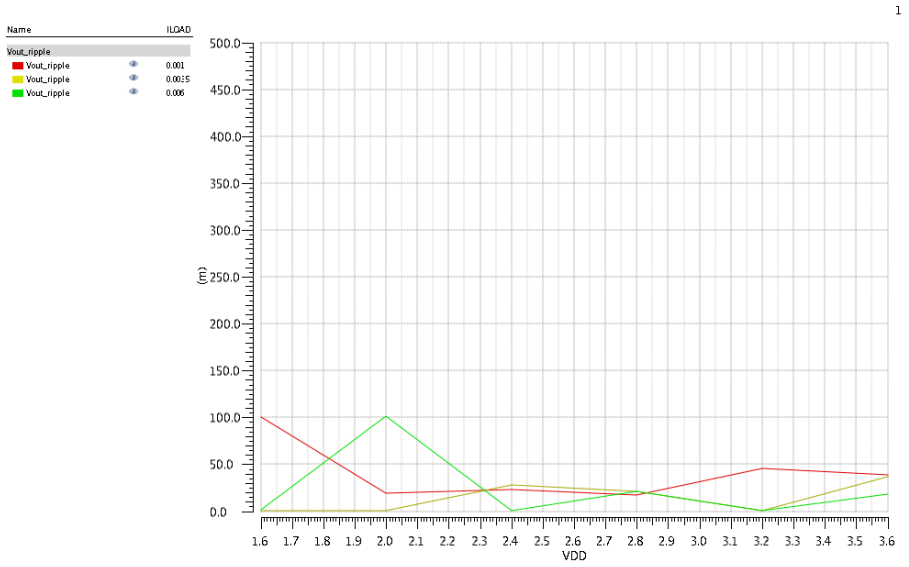

Figure 4.20: Converter output voltage ripple over the whole input voltage range.

The resulting behaviour of the converter under a loading condition change from $0mA$ to

$6mA$ within $1ns$ at a supply voltage of $V_{DD} = 3.6V$ are shown in figure 4.21. It shows that the converter holds the output voltage in the specified voltage range and adapts its divider configuration due to change in the loading condition. That can be observed in the rising and falling edges of the output voltage. As described in 3.15, the converter delivers enough at the output only with a few charge pumps to supply the load under light loading conditions. As the load increases, it changes its divider configuration and its time to deliver charge pumps.

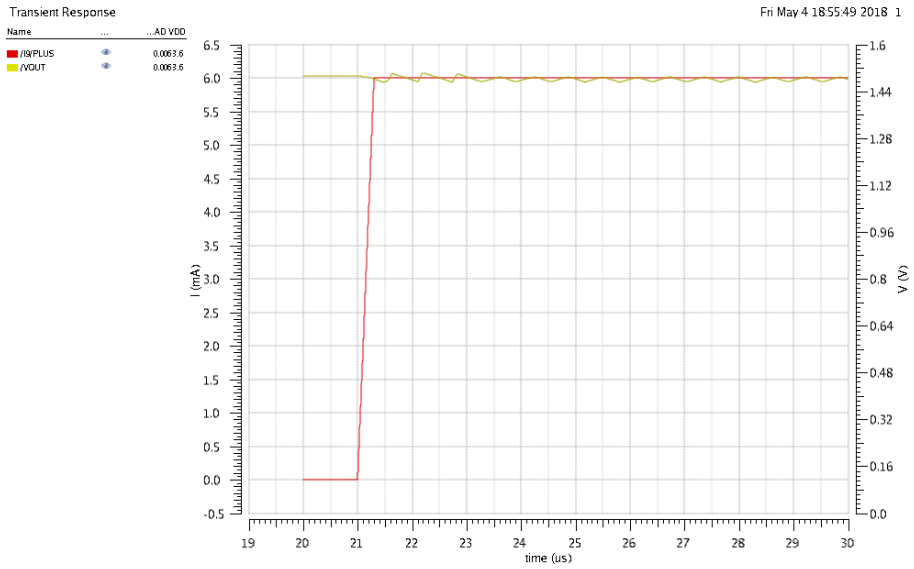

Figure 4.21: Load step at the output of the converter with 6mA.

As the converter is loaded with $1mA$, it stays in the current divider configuration as it is sufficient to deliver the required charge with only a small number of charge pumps. In this case the output voltage looks like shown in figure 4.22.

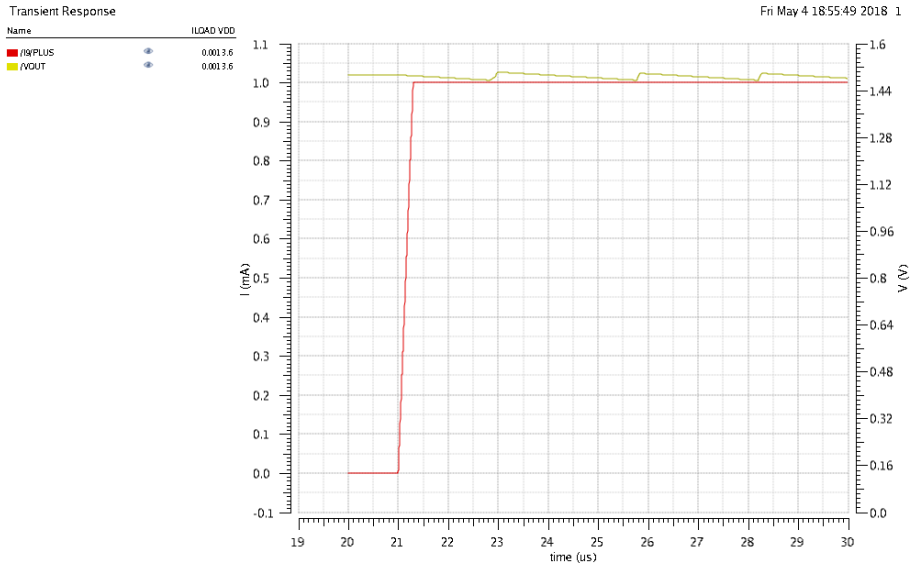

Figure 4.22: Load step at the output of the converter with 1mA.

In the case that there is no load present at the output, the converter needs about $2.24\mu s$ to charge the output capacitance and reach the desired output voltage level. As it can be seen in figure 4.23, the converter starts with the lowest divider configuration of $\frac{1}{2}$ and switches to the next higher ratio every clock cycle. Since the voltage limits for the output voltage range are not reached at the beginning, charge pumps are performed constantly in two phase cycles. As the converter reached the desired level, no further pumps are performed and the output voltage stays at this level since no current discharges the output capacitor.

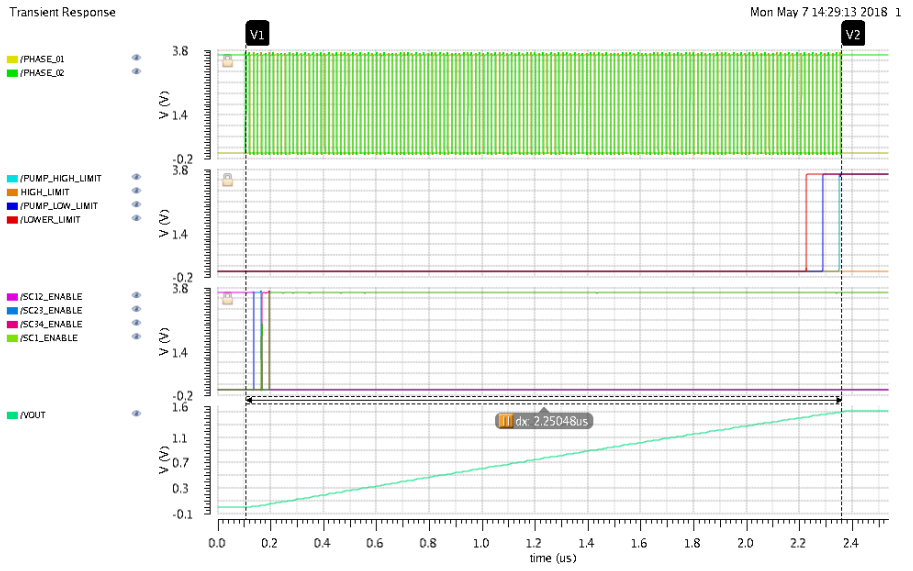

Figure 4.23: Start-up behaviour of the converter at maximum battery voltage of $3.6V$ and without loading.

Finally, the converters energy efficiency is shown in the figure 4.24. The converter reaches a maximum efficiency of up to 75%, the average efficiency is about 65%. The plot shows that a high efficiency can be obtained especially in the load range of about $6mA$ over the whole voltage range. Due to variations that have already been analysed in chapter 4. The control scheme misses the right divider configuration in the medium input voltage and medium load current condition which leads to efficiency penalties.

Figure 4.24: Efficiency of the converter over the whole input voltage range.

4.9 Layout

In order to get an estimation of the whole chip area that would be needed to implement the switched capacitor converter a layout proposal is shown in figure 4.25. It shows that the whole converter has a width of about $430\mu m$ and a length of about $640\mu m$ that gives a total consumed chip area of $0.2752mm^2$. The mentioned implemented total capacitance of $1.05nF$ that is necessary to drive the high current is the part that consumes the most area with about 84% of the total required chip area. The digital logic part is also mentionable as it consumes about 11% of the total chip area. Also large switching transistors and resistors are implemented but their spacial dimension sum up to just about 1.5%. The rest of the area is consumed by non-ideal placement respectively not perfectly uniform shapes.

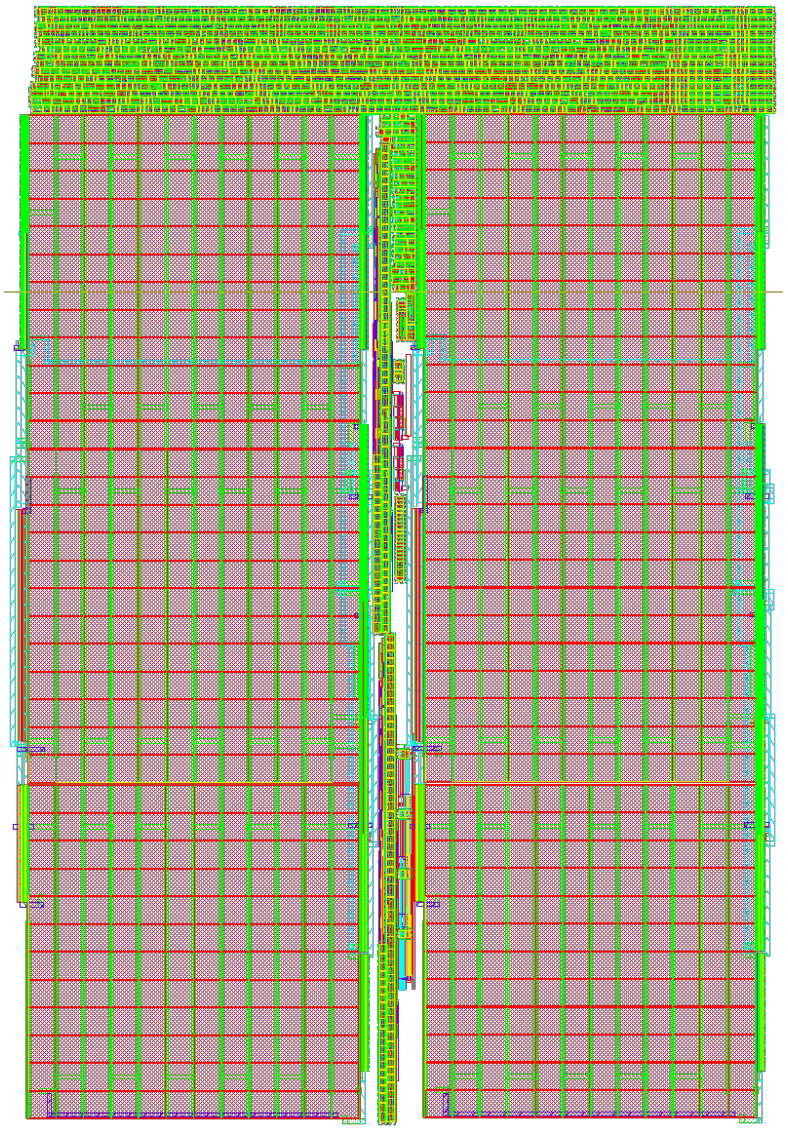

Figure 4.25: Layout of the converter.

Chapter 5

Conclusion

This work has given an introduction of what considerations have to be made and what is the theory behind the working principle of switched capacitor DC-DC converter is. Starting with necessary divider configurations to the choice of the right frequency and hence the adjustment of used switching transistor sizes and finally implementing a control strategy for the converter. As the converters usable capacitance is usually given in the case of an integrated converter by the available chip area, compromises due to the achievable efficiency have to be made. These trade-offs start with the choice of the switching frequency, since it has to be as low as possible to minimize the losses in the parasitic elements but as high as needed to obtain the voltage at the output fulfils the specifications. When it comes to the dimensioning of the transistor sizes again parasitic elements have to be taken in mind while obtaining an adequate low on-resistance. A working divider cell can than be fragmented into smaller ones that can be switched in an interleaved manner to reduce the output voltage ripple.
The simulation results have shown the operation of the essential circuitry of the converter. Also a few weaknesses of the converter have been found that can be optimized. For example the estimation of the loading condition is quite fragile since all deviations of the other circuits have to be taken into account and can sum up to a misleading interpretation for the control unit.

In table 5 the results of the converter are compared to other published designs of switched capacitor DC-DC converter. It shows that the efficiency can be further increased by the use of capacitances that are integrated for example by ferromagnetic material. Another fact that is shown, is that as the load and especially the input voltage can vary in a wide range the peak efficiency suffers. This is because of the trade-offs the analog designer has to make in order to fulfil a good overall performance instead of just one exact point of operation. The use of off-chip capacitors of course has benefits in terms of high values of available floating capacitance but might not be desirable in most of the applications since an external component always means additional area on a printed circuit board (PCB) and thereby additional costs.
Compared to other designs, the converter presented in this work offers a high input voltage range that can vary by 2.25 and a moderate output load range that can vary up a factor

of 6. Due to just one external capacitor, the chip area stays reasonable large with a size of $0.275mm^2$. The converter as a whole can be implemented in a standard CMOS process which means that there are no extraordinary cost considerations due to a special process or SiP approach.

Design	[8]	[10]	[11]	This Work
Technology	$130nm$ CMOS	$65nm$ CMOS	$180nm$ CMOS	$130nm$ CMOS
Chip Area	$0.366mm^2$	$0.493mm^2$	$29.16mm^2$	$0.275mm^2$
Capacitor Type	Ferroelectric	MIM+MOS	PMOS gate	MOS+Off-Chip
Vin	$1.5V$	$0.6V$ - $1.2V$	$2.5V$ - $5V$	$1.6V$ - $3.6V$
Vout	$0.4V$ - $1,1V$	$0.6V$,$0.8V$,$1V$	$1.3V$	$1.4V$ - $1.6V$
Conversion Ratios	Step down $1, \frac{2}{3}, \frac{1}{2}, \frac{1}{3}$	Step down $1, \frac{3}{4}, \frac{2}{3}$	Step down $\frac{1}{3}, \frac{1}{2}$	Step down $1, \frac{3}{4}, \frac{2}{3}, \frac{1}{2}$
Output Current	$20\mu A$ to $1mA$	$10\mu A$ - $800\mu A$	$250mA$	$1mA$ - $6mA$
Quoted Efficiency	93%-measured	80%-measured	76.4%-measured	75%-simulated

Table 5.1: Comparison of different published designs.

5.1 Outlook

This work can be seen as a starting point for further investigations in the topic of integrated switched capacitor DC-DC converter for a TPMS system. It already introduced some of the converters strengths but also some of its weaknesses. There is still room for improvement on the regulation of the converter. Since it was built up by logic cells that are made up of thick oxide transistors, there is still potential to save energy. A possible solution here would be to implement a $1.5V$ powered control logic domain that outputs its signals to level-shifter and hence to the rest of the remaining part of the converter. Also the use of a Verilog model here would be beneficial to increase the functionality of the control unit. The implemented design has two interleaved converter cells. Here as well a possible improvement would be to increase the number and gain a little more efficiency by reducing the output ripple current further. In general, the concept of estimating the output current has shown a lot of difficulties that arise with it. A direct current measurement at the output might be helpful to get rid of the problem that comes with the uncertainty of the comparator respectively the high rising edges. Regarding the PFM technique, also a time-continuous version would be more beneficial to get an optimal switching frequency at the output. And finally, in order to proof the simulation results of the designed converter in the real world, a test chip has to be fabricated and verified in the laboratory.

Chapter 6

Nomenclature

CMOS	Complementary Metal Oxide Semiconductor
DCDC	Direct Current Direct Current
IoT	Internet of Things
iVCR	ideal Voltage Conversion Ratio
MIM	Metal-Insulator-Metal
MOS	Metal Oxide Semiconductor
PFM	Pulse Frequency Modulation
PCB	Printed Circuit Board
SC	Switched Capacitor
SCPC	Switched-Capacitor Power Converter
SiP	System-in-Package
TPMS	Tire Pressure Measurement System
VHSIC	Very High Speed Integrated Circuit

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