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Radiation Hardened on-Chip System Monitoring for Space Applications

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Abstract

In this work a system monitoring architecture for a specific space application will be presented. More precisely, a front-end ASIC for the next generation of spaceborne fluxgate magnetometers is currently in development. This ASIC basically consists of various measurement systems which have to be monitored accurately. This opens a challenging design task due to fact of the harsh space environment. Nevertheless monitoring the available resources of an ASIC is crucial for space applications, since the available power of a spacecraft is limited to a certain amount.

A system monitoring architecture is composed of three important stages. First of all there are the sensors which are needed to monitor the selected quantities. Next a suitable sensor interface should process the obtained sensor signals. The last step in the signal chain is to convert the signal from an analog to a digital domain in order to evaluate the gained sensor values.

This thesis gives a review on state-of-the-art ADC architectures leading to the design and implementation of a fully differential second order switched capacitor delta-sigma modulator. Moreover a sensor interface composed of a programmable instrumentation amplifier for various measurements, including two methods for temperature sensing and a high-side current sensor will be employed. Radiation hardening techniques concerning the prevention of latch-up will be discussed resulting in a final layout for the test-chip including a suitable ESD protection scheme.

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Lists of abbreviations

ADC	analog-to-digital converter
ASIC	application-specific integrated circuit
CIFB	cascade of integrators distributed feedback form
CIFF	cascade of integrators distributed feed forward and input coupling form
CMFB	common mode feedback
CMRR	common mode rejection ratio
DAC	digital-to-analog converter
DUT	device under test
ELT	enclosed layout transistor
ENOB	effective number of bits
ESD	electrostatic discharge
FOM	figures-of-merit
GBW	gain-bandwidth product
HBM	human body model
IA	instrumentation amplifier
IC	integrated circuit
NTF	noise transfer function
OSR	oversampling ratio
OTA	operational transconductance amplifier
PTAT	proportional to absolute temperature
RFC	recycling folded cascode
RTD	resistance temperature detectors
SAR	successive-approximation-register
SDCT	continuous-time delta-sigma ADC
SDSC	switched capacitor delta-sigma ADC
SNDR	signal-to-noise and distortion ratio
SQNR	signal-to-quantization-noise ratio
TID	total ionizing dose

Corner analysis:

ff	fast NMOS fast PMOS
ss	slow NMOS slow PMOS
snfp	slow NMOS fast PMOS
fnsp	fast NMOS slow PMOS

Chapter 1

Introduction

The scope of this thesis is to develop a system monitoring architecture for a front-end ASIC which contains an analog read-out circuit for the upcoming generation of fluxgate-magnetometers. This thesis is composed of four chapters. The first chapter will present the system with its building blocks. Moreover the latest literature and publications are reviewed to gain an excellent basis for the development of a system monitoring architecture. The second chapter is going to focus on the implementation of a delta-sigma based analog-to-digital converter. The third chapter elaborates a solution for the sensor interface including various measurements. The last chapter will deal with design of a suitable layout including a discussion on possible radiation hardening techniques as well as the introduction of ESD protection methods of ICs.

1.1 System Monitoring for Space Applications

Monitoring the available resources is a crucial task for space applications, since the provided power of a spacecraft is limited. Additionally it can be ensured that a device works under the correct conditions, since for example a supply voltage drop can be detected. Thus it is necessary to measure the most critical quantities voltage, current and temperature. In the following figure 1.1 an implementation of a system monitoring architecture is depicted.

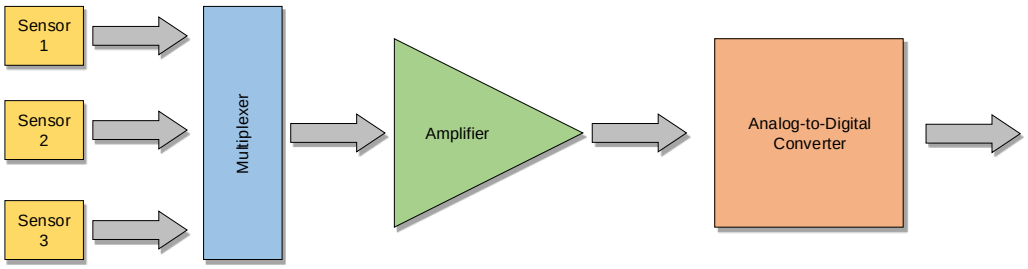

Figure 1.1: System monitoring architecture, with different sensor at the input followed by a multiplexer, an amplifier and an analog-to-digital converter which processes the sensor signals. A more detailed block diagram is in the appendix.

As mentioned before this system monitoring architecture is particularly developed for a front-end ASIC for space applications. This leads to a dedicated system specification which results in terms of numbers in the following table 1.1.

Building block	Specification
ADC	Minimum ENOB of 12bit
Chip temperature via diode	Temperature range from $-55°C$ to $+125°C$
External temperature sensor	PT1000 element (temperature range $\pm 125°C$)
Current sensor	Maximum current to be measured $I_{max} = 250mA@12V$
Voltage sensor	Measure different voltage levels (12V, 8V, 5V)

Table 1.1: System specification.

1.2 Analog-to-Digital Converter

Today a major number of different analog-to-digital converter topologies have been introduced. These architectures provide a diverse spectrum of performance, such as high conversion rates with medium accuracy, while others maintain higher accuracy with diminished conversion rates. In this way it is a challenging task to single out a suitable architecture for a given application. To overcome this difficulty a valuable overview on state-of-the-art analog-to-digital converters is established in the following chapter.

1.2.1 Introduction to Analog-to-Digital Converter Architectures

Analog-to-digital converters can roughly be restricted into two groups:

- Nyquist-rate converters, which sample at least at twice of the signal frequency. The most prominent Nyquist rate converter architectures are flash, pipelined, successive-approximation-register and folding ADCs.
- Oversampling converters, which operate much swifter than Nyquist-rate converters, usually 20 to 500 times faster. Moreover noise shaping can be employed to further reduce the quantization noise.

The following figure 1.2 illustrates these different types in regard to their noise spectrum.

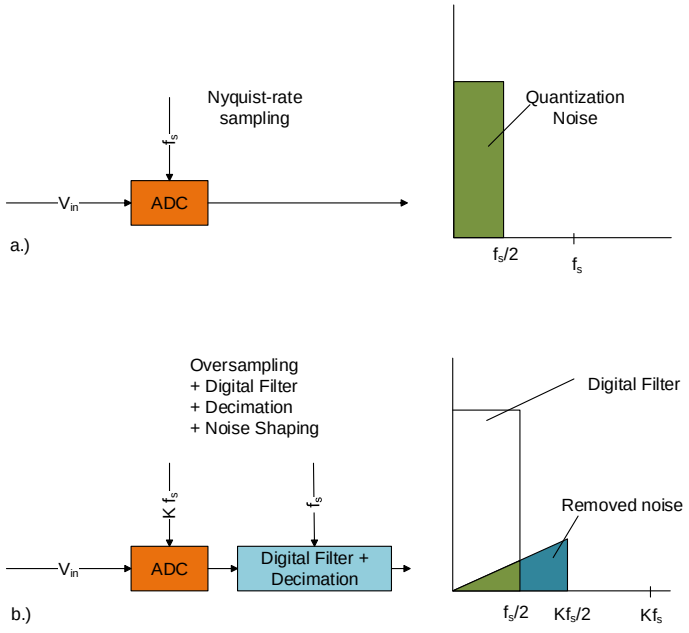

Figure 1.2: Overview of a) Nyquist-rate converter, b) oversampling converter with noise shaping including a digital filter.

Furthermore the various types of ADCs can be classified by performance (speed, accuracy) according to the recent literature [1].

Low Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low Accuracy
Integrating	SAR	Flash
Oversampling		Piplined

Table 1.2: Categorisation of ADCs according to their performance.

1.2.2 Survey on State-of-the-Art Analog-to-Digital Converter

For a more profound understanding of each converter architecture, it is crucial to review the latest publications and analyse performance characteristics. There are some eminent cited sources from Boris Murmann [2], Jose M. de la Rosa [3] or Robert H. Walden [4]. Performance benchmarking is an increasingly important task, thus it is relevant that different ADC architectures can be compared. Therefore figures-of-merit have been introduced. A FOM is a quantity used to describe the performance of a certain system relative to its alternatives.

Regarding ADCs the most popular FOM is [5]:

$$FOM = \frac{P}{f_s \cdot 2^{ENOB}} \tag{1.1}$$

This FOM sometimes stated as "Waldens FOM", combines the power dissipation of the ADC with its effective number of bits in regard to the Nyquist sampling rate. In other words it describes how efficient a conversion step can be generated, hence the smaller the value the better. Another important factor is the effective number of bits, which is defined by the signal-to-noise and-distortion ratio as follows:

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{1.2}$$

The effective number of bits quantifies the quality of an analog to digital conversion. A higher ENOB means that voltage levels recorded in an analog to digital conversion are more accurate. Thus the ENOB is a measure of the dynamic range of an ADC. In order to study ADC architectures, a valuable starting point is the open source data collection of Boris Murmann [2], which gets updated continually. The following figure 1.3 illustrates the effective number of bits of different ADCs, including flash, folding, SAR, pipelined and continuous-time as well as switched capacitor delta-sigma ADCs.

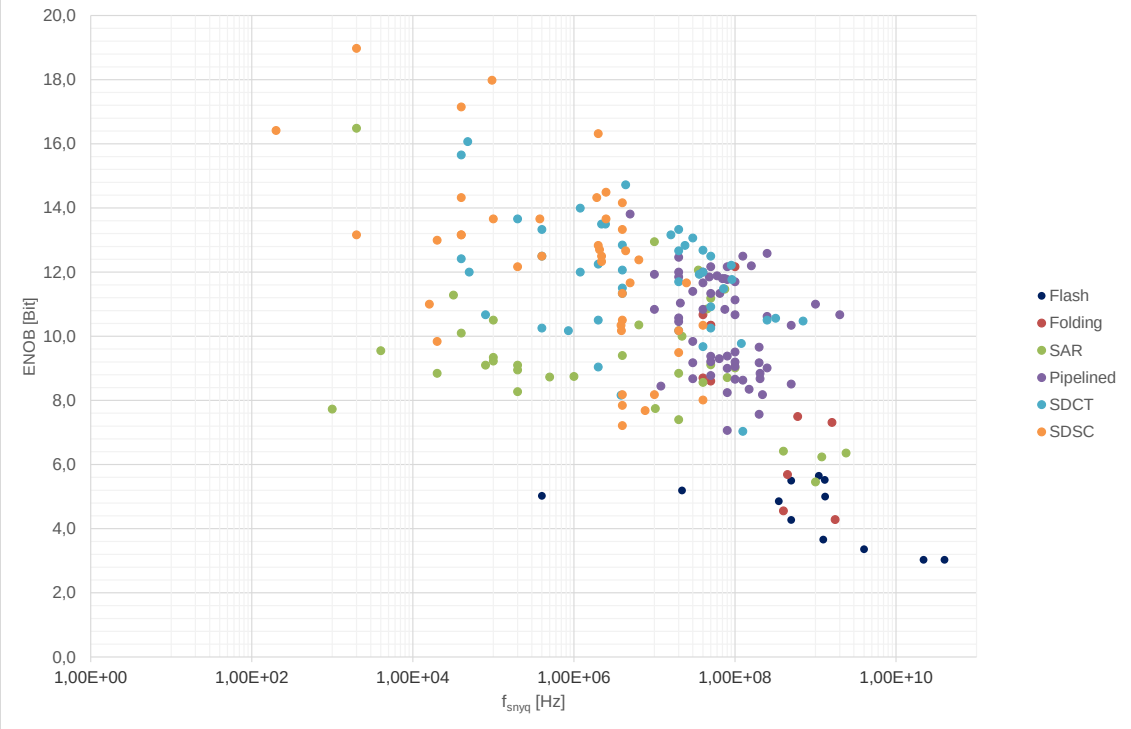

Figure 1.3: Effective number of bits of different ADCs as a function of the Nyquist sampling rate [2]. For oversampling ADCs the sampling rate is divided by the oversampling ratio.

In regard to the given system specification of table 1.1 an ENOB of 12bit is required. From the above-noted figure 1.3 it is evident that for this given value and above delta-sigma modulators are the most common ADCs. Nevertheless a pipelined ADC would also hit the required specification of 12bit easily, but these types are predestinated for higher sampling rates. On the other hand SAR ADCs lag behind delta-sigma topologies concerning higher resolutions. Moreover the power consumption is another decisive limitation. The following figure 1.4 characterizes the power consumption in dependency of the Nyquist sampling rate.

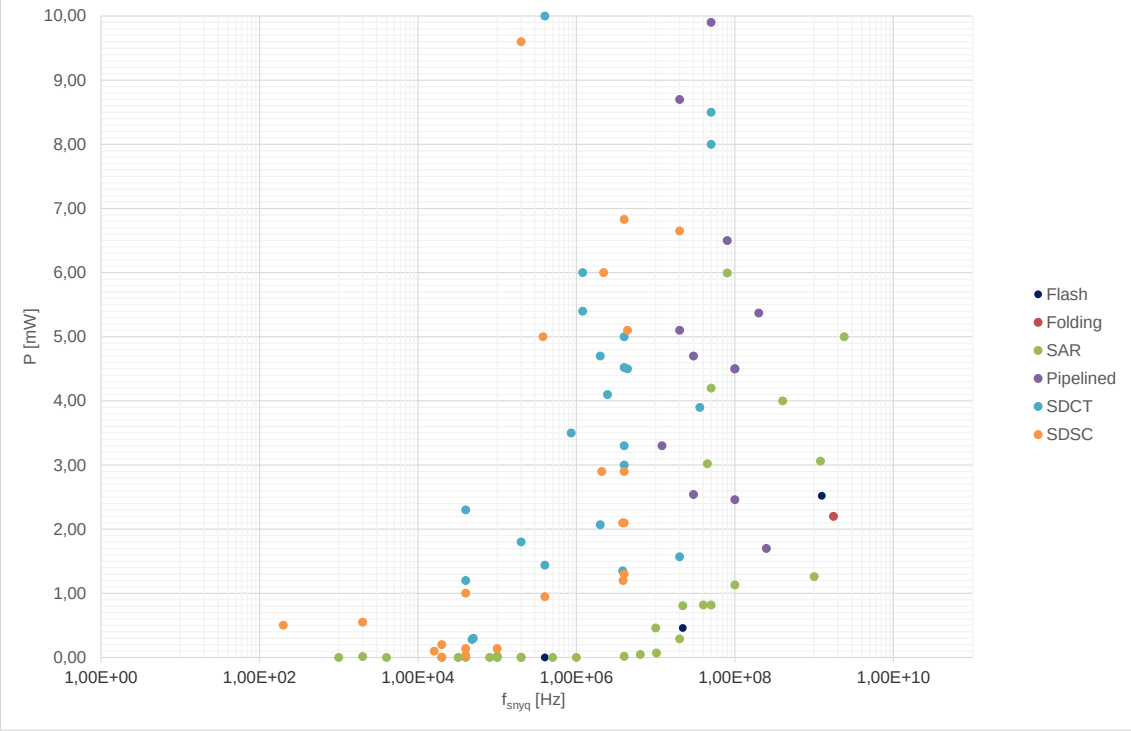

Figure 1.4: Power consumption in mW of different ADCs [2].

As can be seen from the previous plot successive-approximation-register are by far the most power efficient architecture directly followed by delta-sigma ADCs. On the contrary flash ADCs consume the most power, since they need a huge amount of comparators to achieve high resolutions. Combining the two previous illustrations results in the often used FOM from Walden.

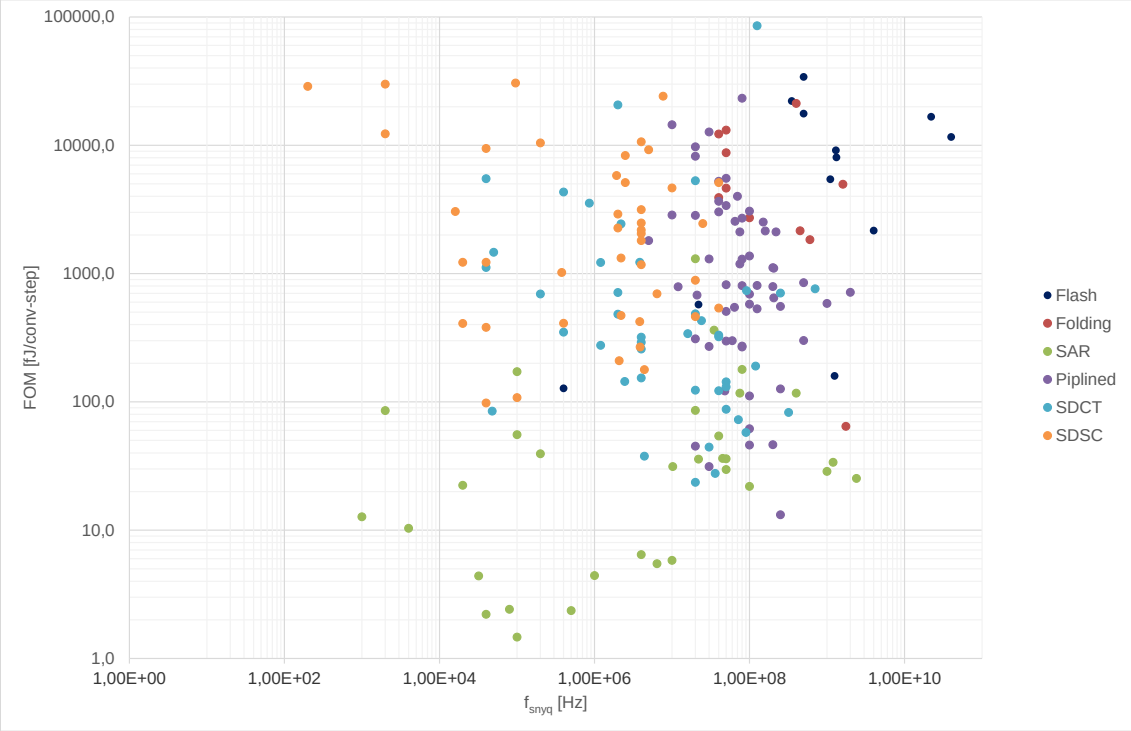

Figure 1.5: Waldens often cited FOM [2].

From the above depicted figure 1.5 it is evident that SAR ADCs are the most efficient architecture directly followed by delta-sigma ADCs. Combining the previous results the overall performance of delta-sigma ADCs is suitable for a system monitoring architecture. Delta-sigma ADCs can be implemented either as continuous-time architecture or with switched capacitor topologies. This results in a number of advantages and disadvantages associated with each choice. In continuous-time systems the active RC integrator does not have to settle to fully accuracy every half clock period, making them very attractive for high speed applications. On the other hand in switched capacitor integrators the oversampling ratio is limited by the gained bandwidth of the used operational amplifier. Regarding the circuit implementation, continuous-time systems lag behind switched capacitor system due to the fact that poly resistors are hard to implement with good accuracy, whereas in switched capacitor integrators capacitor variations are better controlled. Moreover switched capacitor system are less sensitive to clock jitter [6]. According to the preceding discussion the implementation of a switched capacitor delta-sigma ADC is proposed.

1.3 Sensors and Sensor Interfaces

Sensor interfaces play a crucial role in today's electronic based systems. This leads to a challenging assignment to design aforesaid interfaces that can handle any kind of sensors. The upcoming chapter deals with this relevant task and employs a profound solution.

1.3.1 Introduction to Sensor Interfaces

A Sensor interface typically consists of a sensor, a multiplexer and a programmable amplifier [7],[8]. Sensors can be divided into two groups according to the measured quantity: electrical and non-electrical. Electrical sensors directly measure voltage or current, whereas non-electrical sensors need a transducer to convert the non-electrical signal into the electrical domain. Most quantities that are measured are non-electrical such as temperature, pressure, displacement or humidity. Thus a device called electrical transducer is employed. Transducers can be classified based on the principle of transduction like thermo-electric, magneto-resistive or optical. Furthermore they can be split into two groups of active and passive transducers. A passive transducers is a device which needs external power for transduction, whereas active transducer can work without external power. Thus the interface should be able to handle above-said sensor types. This inducts a designated specification for the amplifier.

In general the gain of an amplifier can be set using feedback loops. There are good reasons to use a feedback loop like the desensitization of the gain, reduction of distortion and an increase of bandwidth. Typically the feedback of an amplifier is set using ratios of passive components like resistors or capacitors. In order to achieve a programmable gain these passive elements can be switched in and out of the circuit or can be bypassed with programmable switches. Since ideal switches cannot be implemented in practice the non-idealities of the switches must then be taken into consideration as they may reduce the precision of the implemented programmable component.

Typically a programmable resistor is realised by segmentation into single resistor elements. This single elements can then be bypassed with switches as shown in figure 1.6. The resistor elements are sized in a way, that the smallest resistor value is obtained if all switches being on. Another source of inaccuracy are the switches, since their non zero on resistance introduces a non-negligible resistance which should be taken into account when sizing the resistor segments. Usually the high off resistance can be neglected when a resistor element is switched in. Nevertheless the absolute accuracy of resistors is determined by fabrication tolerance and is limited to the variation of the sheet resistance.

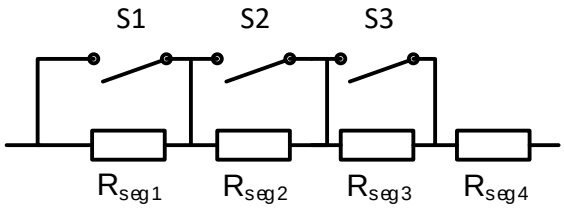

Figure 1.6: Schematic of a programmable resistor.

The concept of a programmable capacitor is depicted in figure 1.7. In case of programmable capacitors the effect of finite switch resistance can be neglected, if there is sufficient time available to charge the capacitors. On the other hand a more critical aspect is the capacitance of the switch. Nevertheless this leads to a tradeoff, since making the transistor wider decreases the charging time, but increases the parasitic capacitance of the switches. Moreover leakage current may also be a problem.

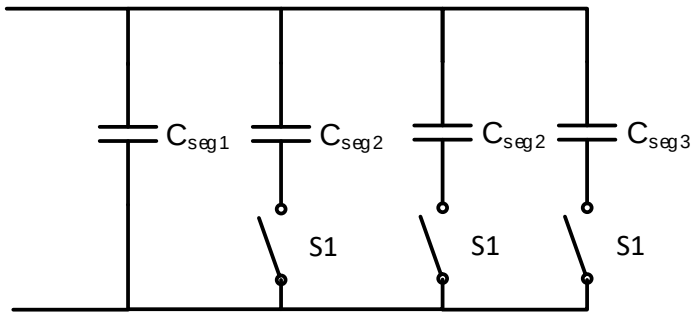

Figure 1.7: Schematic of a programmable capacitor.

1.3.2 Current Sensors

Current sensing is essential in a wide range of applications. Nevertheless it is difficult task, due to the fact that it is an intrusion in the existing system. It can be divided into two approaches which pose a trade-off in different areas:

- *High-side current sensing*: The current is sensed in the supply path of the power connection to the monitored load. This means that the load is grounded and high load currents caused by short can be detected. Nevertheless the sense amplifier must withstand high input common mode voltages.

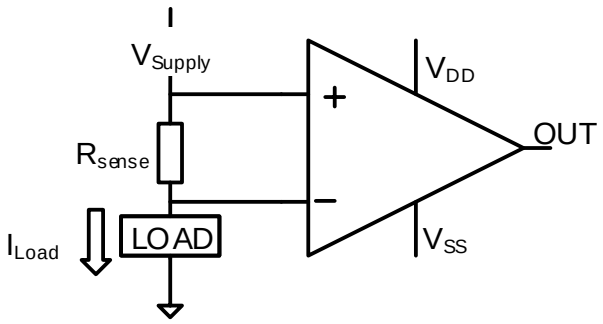

Figure 1.8: High-side current sensing concept.

- *Low-side current sensing*: The current is sensed in the ground path of the power connection to the monitored load which leads to a low input common mode voltage. Though a short can not be detected .

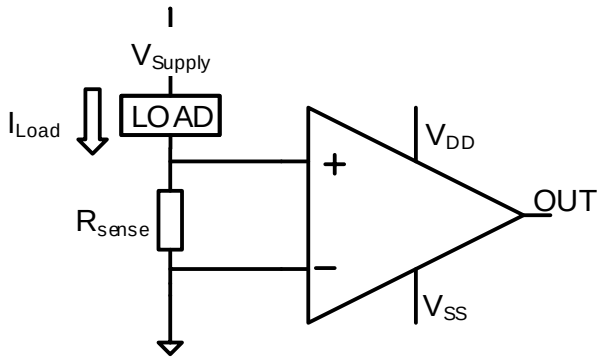

Figure 1.9: Low-side current sensing concept.

A well considered choice of the shunt resistor R_{SENSE} is a critical part of designing any of these current monitors. There a some principles which should simplify the selection of the shunt resistor. First the voltage loss of a high R_{SENSE} value diminishes the source voltage, hence a low R_{SENSE} value commits a desirable target. Next the accuracy plays a significant role in low level current measuring. This induces a tradeoff since an increase of accuracy is directly linked with an increase of the voltage drop across the sense resistor. Power dissipation of the sense resistor is also a substantial parameter, which should be taken into account when selecting the shunt resistor. For high frequency currents the inductance of the shunt resistor also must be observed.

1.3.3 Temperature Sensors

Temperature measurement is a relevant task and therefore some methods have been introduced. In general these methods rely on the fact that a parameter varies with temperature. Some of the most commonly developed approaches are thermocouples, thermistors and resistance temperature detectors [9]. Thermocouples generate a voltage due to the thermoelectric effect, whereas thermistors and RTDs have a resistance whose temperature dependent. On the other hand in semiconductor devices the thermal voltage across a pn-junction is used for temperature sensing. According to the given specification in table 1.1 this section will briefly handle on chip temperature sensing with diodes and resistive temperature measurement with a PT1000 element.

A PT1000 element consist of a platin resistor and relies on the temperature dependency of its resistance. These elements are standardised to EN 60751 which implies a temperature range of $-200°C$ to $850°C$. This temperature range is divided into two parts. For the first part from $-200°C$ to $0°C$ the following equation counts:

$$R(T) = R_0 \cdot (1 + AT + BT^2 + C(T - 100°C)T^3) \tag{1.3}$$

The next section from $0°C$ to $850°C$ is based on:

$$R(T) = R_0 \cdot (1 + AT + BT^2) \tag{1.4}$$

The standardised temperature coefficients are listed in the table below.

A	3.9083 10^{-3} $°C^{-1}$
B	-5.775 10^{-7} $°C^{-2}$
C	-4.173 10^{-12} $°C^{-4}$

Table 1.3: Temperature coefficients for a PT1000 element.

This means that for a temperature of $0°C$ the PT1000 element holds a value of 1000Ω.

A semiconductor diode consists of a pn-junction which is connected to two terminals. The Shockley diode equation describes the I-V characteristic of an ideal diode and is given as follows:

$$I = I_S \left(e^{\frac{V_D}{nV_T}} - 1 \right) \tag{1.5}$$

The current of the diode I is depending on the saturation current I_S, the voltage across the diode V_D, the thermal voltage V_T and its emission coefficient n. In this equation there are two temperature dependent parameters, the saturation current I_S and the thermal voltage V_T. The thermal voltage is derived as follows:

$$V_T = \frac{kT}{q} \tag{1.6}$$

Where k is the Boltzmann constant, T the absolute temperature and q the elementary charge. A simplified function of the saturation current is given by

$$I_S = AT^{3/n} e^{(\frac{VG}{nV_T})} \tag{1.7}$$

where A is a constant, T is the absolute temperature, V_G is the semiconductor band gap voltage, and V_T is the thermal voltage with its emission coefficient n. According to these equations a diode is a suitable device for temperature sensing. A common way to use a diode as temperature sensor is its implementation in a PTAT cell [10], [11]. This method is reviewed in detail in the third chapter.

Chapter 2

Delta Sigma Analog-to-Digital Converter

2.1 Introduction and Fundamental Principle

In general a delta-sigma ADC relies on three signal processing principles, oversampling, noise shaping and digital filtering [6]. The minimum sampling rate for a signal with a given bandwidth f_{bw} which leads to no information loss is defined as Nyquist rate $f_{nyq} = 2f_{bw}$. If this signal is then sampled with a frequency f_s higher than f_{nyq} then it is called oversampling. It is defined as:

$$OSR = \frac{f_s}{2f_{bw}} \tag{2.1}$$

Furthermore oversampling introduces another important mechanism, it allows filtering of signal and noise since the signal only reserves a fraction of the whole frequency range. This enables the opportunity to further suppress the quantization noise energy in the signal band leading to a huge increase of the in-band SNR. This suppression is called noise shaping. A digital filter can then be used to remove the out of band noise.

2.2 High-Level System Design

This chapter will deal with the high-level design of a delta-sigma modulator that fulfils the system specification presented in the table 2.1 below. A proper design methodology and a tool to efficiently design a delta-sigma modulator is introduced. The design process usually starts from the specifications, typically bandwidth and effective resolution. Next the modulator architecture including the main parameters OSR, modulator order N and quantizer resolution B is explored. From there non-linear models provided by the delta-sigma toolbox (2.2.1) should be used to extract the scaling coefficients of the NTF. The gained specifications can then be mapped to each block, which can be finally translated to transistor level.

Parameter	Symbol	Value	Unit
Bandwidth	f_b	1	kHz
Effective resolution	ENOB	12	bit
Supply voltage	V_{DD}	1.8	V

Table 2.1: Specification of the proposed ADC.

2.2.1 Delta Sigma Toolbox

The delta-sigma toolbox is an open source tool for MATLAB developed by Richard Schreier. It is a very powerful high-level modelling tool, which can help designing delta-sigma modulators. The toolbox allows the simulation of noise transfer functions for different OSR and modulator orders. Furthermore the SNR can be determined for various input amplitudes and lastly the scaling coefficients can be extracted for single-loop modulator architectures.

2.2.2 System Design

Before defining the main parameters of the delta-sigma modulator the given effective resolution has to be mapped to the allowed signal-to-quantization noise. For an effective resolution of 12bit the SQNR can be estimated as follows:

$$SQNR = N \cdot 6.02 + 1.76dB \tag{2.2}$$

To ensure the given ENOB, it is recommended to add a reasonable margin to the SQNR, because the circuit non-idealities will degrade the SQNR. This reason leads to a selected SQNR value of roughly 90dB. Next the loop filter topologies have to be discussed. The main loop filter implementations are the *distributed feedback* network and the *distributed feed forward and input coupling* network. The CIFB structure consist of cascaded integrators with the quantizer output fed back to each integrator with different weight. On the other hand a CIFF structure represents the inverse answer with a weighted fed forward summation. Both topologies pose a tradeoff, nevertheless a CIFB structure 2.1 gives more ease for the implementation of the integrators [12].

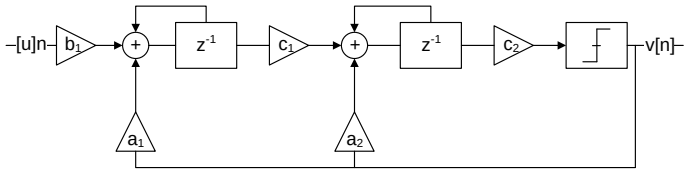

Figure 2.1: Block diagram of cascade-of-integrators feedback form.

Now the values of the main parameters are reviewed. To reach 90dB of SQNR there a multiple choices [12]. Increasing the modulator order will affect the stability of the system, hence it is desirable to aim for a lower order with a higher OSR. Selecting a clock rate of 1MHz yields in an oversampling ratio of 500 for the stated bandwidth of 1kHz. A second-order 1bit quantizer represents a good tradeoff to meet the required specification, since its available SQNR leaves some headroom [6]. Finally this leads to the following solution depicted in table 2.2.

Parameter	Symbol	Value	Unit
Sampling frequency	f_s	1	MHz
Oversampling ratio	OSR	500	-
Quantizer resolution	B	1	bit
Modulator order	N	2	-

Table 2.2: Parameters of the planned delta-sigma modulator.

The above-noted values leave some margin in regard to the given bandwidth of 1kHz. Due to the high OSR an increase of the bandwidth will not affect the required SQNR threshold to reach the desired ENOB. The next step is to use the established modulator parameters and perform a simulation of the NTF. Therefore the delta-sigma toolbox is used.

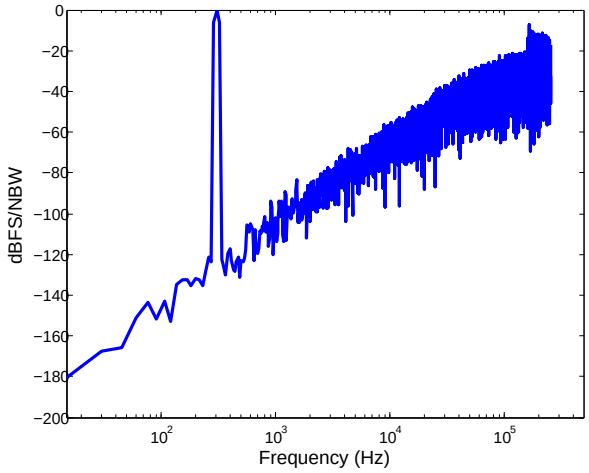

Figure 2.2: High level simulation of the NTF. With the use of the gained modulator parameters, a full scale sine wave at the input gives a SQNR of about 110dB. As can be seen the circuit non-idealities like flicker noise are not present, which would degrade the SQNR significantly.

The last step is to extract the scaling coefficients of the NTF, which is also done by the delta-sigma toolbox.

Parameter	Value
a_1	0.1406
a_2	0.1753
b_1	0.1406
c_1	0.3483
c_2	4.4203

Table 2.3: Scaling coefficients for a second order delta-sigma modulator referred to figure 2.1. The capacitor ratio of the first stage is defined by a_1 or b_1, whereas c_1 specifies the weighting factor for connecting the first integrator to the second one. The remaining coefficients a_2 and c_2 are not used in this case.

2.3 Circuit Design

This section will cover the circuit design of the various functional blocks of a delta-sigma modulator that fulfil the specifications from the previous definition.

2.3.1 Modulator Circuit

The complete modulator architecture is shown in figure 2.3.

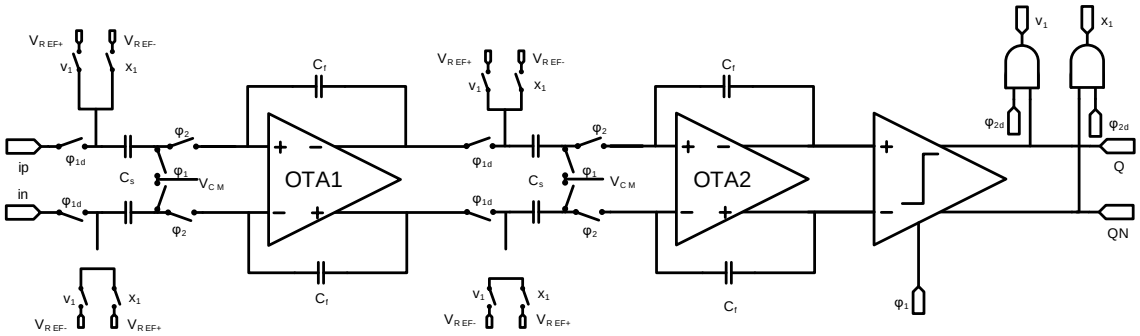

Figure 2.3: Schematic diagram of the implemented second-order single-bit modulator. It consists of two switched capacitor integrators, a single-bit quantizer and its corresponding feedback DAC including a control system. This implementation shares the sampling capacitors with the feedback DAC capacitors.

2.3.2 Integrator - Capacitor Sizing

First the integrator is observed. In order to realise a discrete time integrator it is useful to understand how such a topology is implemented. In figure 2.4 the first integrator including the feedback DAC of the modulator is depicted. This structure is often called parasitic-insensitive, because parasitic capacitances from the switches do not affect the transfer function.

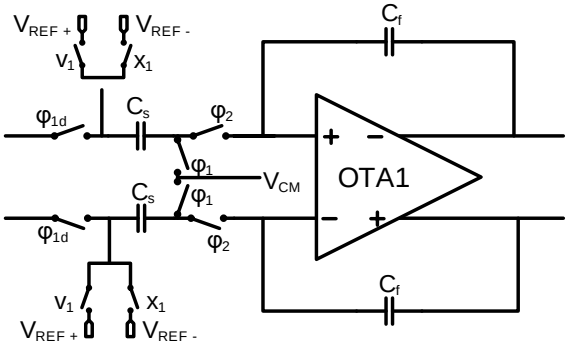

Figure 2.4: Schematic of a switched capacitor integrator. The reference voltage of the feedback DAC is controlled with v_1 and x_1 which is generated by the quantizer outputs. The clocks φ_1 and φ_{1d} define the sampling phase, whereas φ_2 starts the integration phase.

For a single ended version of the integrator the following transfer function can be derived.

$$\frac{V_o}{V_i} = \frac{C_f}{C_s} \frac{z^{-1}}{1 - z^{-1}} \tag{2.3}$$

Next the required capacitor values can be calculated [6]. The absolute value of the first sampling capacitor C_s is determined by a noise constraint. The in-band input-referred mean-square noise voltage associated with the first integrator is approximately:

$$\bar{v_n^2} = \frac{kT}{OSR \cdot C_s} \tag{2.4}$$

Thus the capacitor values can be computed by means of the gained scaling coefficients [6].

Parameter	Value	Unit
C_{1s}	204	fF
C_{1f}	2.618	pF
C_{2s}	178	fF
C_{2f}	513	fF

Table 2.4: Computed capacitor values for the integrators of the delta-sigma modulator. The capacitors C_{1s} and C_{1f} are for the first integrator (OTA1), whereas C_{1s} and C_{1f} are for the second one (OTA2).

2.3.3 Circuit Noise Analysis

In analog-to-digital converters noise plays a critical role on the overall performance. The two major noise sources are the quantization noise which can be accessed with different ADC parameters like OSR and modulator order and the noise generated from transistors. In transistors the fundamental noise contributors are thermal noise and flicker noise. As shown in figure 2.3 the central circuit block of a delta-sigma modulator which contains many transistors is the operational amplifier. The noise contribution should be kept to a minimum in order to not rely on correlated double sampling or chopper stabilisation. Thus the input referred thermal noise power is introduced with γ as the noise coefficient, gm as the transconductance of the amplifier and N_{OTA} as a topology dependent factor [10],[1].

$$S_{n,OTA} = \frac{8kT\gamma}{gm} \cdot N_{OTA} \tag{2.5}$$

This leads to the next section, which will analyse the selection of a suitable operational amplifier.

2.3.4 Operational Amplifier - Topology and Requirements

Operational amplifiers are the most critical block of a delta-sigma ADC, because they determine the overall performance and consume most of the power. The main requirements of the OTA are gain, gain-bandwidth product and output swing. First the requirements must be defined [6] . Since the supply voltage is 1.8V the output swing should be at least half of the supply voltage. Finite gain-bandwidth product will increase the in band noise, because more out of band quantization noise is allowed to fold into the pass band. For this reason the GBW should be much bigger than the sampling frequency. On the other hand finite amplifier gain causes a shift of the NTF zeros leading to an increase of the noise floor and perhaps induce distortion tones [12]. In the table 2.5 below the requirements are summarised.

Parameter	Symbol	Value	Unit
Voltage gain	A_v	≥ 60	dB
Gain-bandwidth product	GBW	≥ 1	MHz
Output swing	OSW	≥ 0.9	V

Table 2.5: Minimum requirements of the proposed OTA .

A good starting point is to review some commonly used OTA architectures represented in the table 2.6 below.

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded Cascode	Medium	Medium	High	Medium	Medium
Two Stage Miller Comp.	High	Highest	Low	Medium	Low

Table 2.6: Comparison of performance of various op-amp topologies [10].

According to the above-noted table a folded cascode architecture delivers a good tradeoff between the main requirements and is depicted in the figure below.

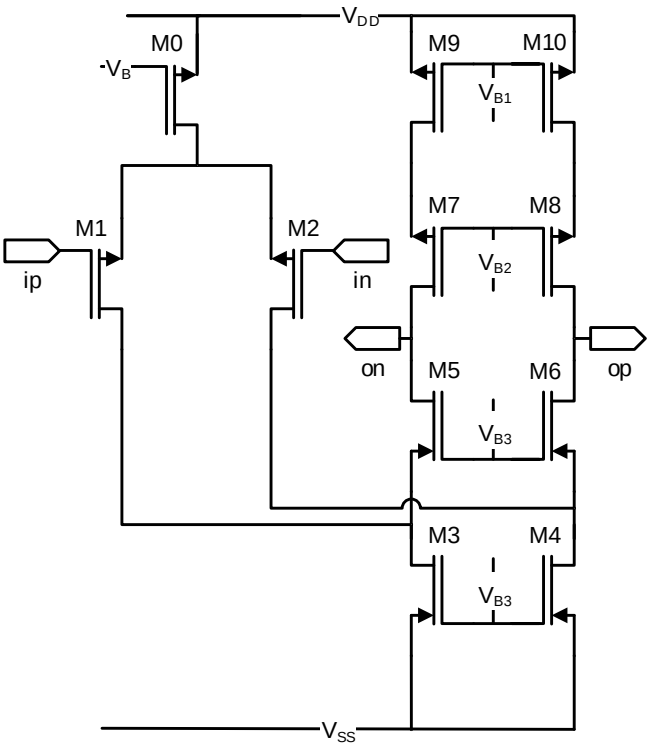

Figure 2.5: Simplified schematic of a folded cascode architecture without bias circuit and common mode feedback.

In recent publications a newer type of the folded cascode architecture is introduced, the so called recycling folded cascode [13], [14] . The proposed architecture delivers an enhanced performance including better gain and GBW. Moreover the input referred noise and offset is reduced.

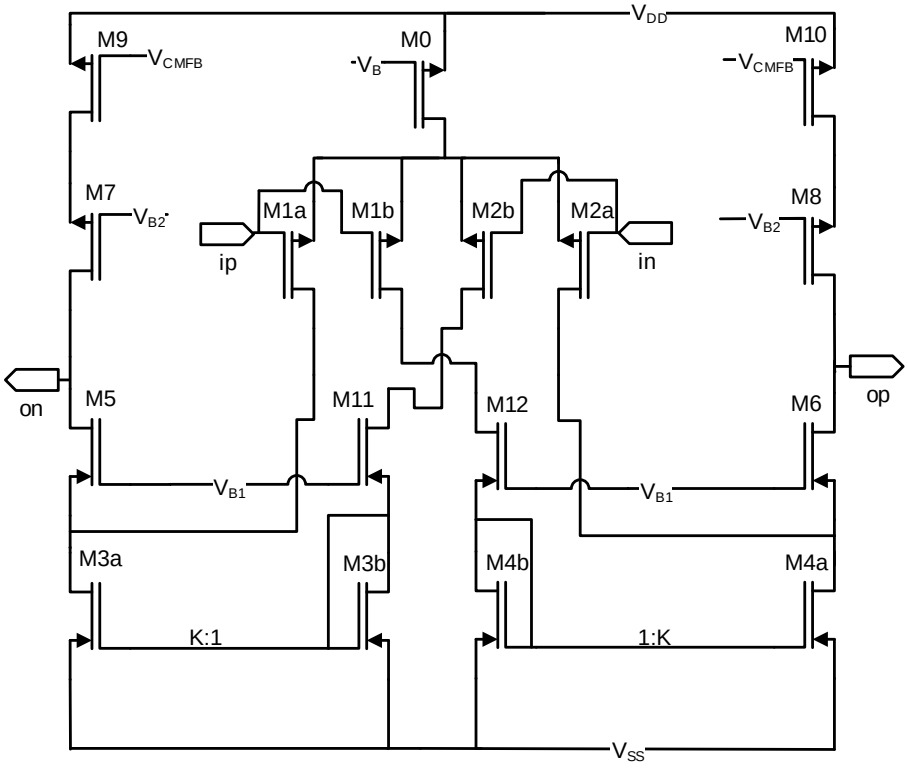

Figure 2.6: Simplified schematic of a recycling folded cascode architecture without bias circuit and common mode feedback.

As an example the improvement of the noise performance is observed in detail. The following equation shows the input referred thermal noise of a folded cascode OTA [10].

$$S_{n,FC} = \frac{8kT\gamma}{gm1} \cdot \left(1 + \frac{gm3}{gm1} + \frac{gm9}{gm1}\right) \tag{2.6}$$

In a recycling folded cascode architecture the factor K is presented [13]. This factor determines the current ratio of the input branch and the output branch. This leads to the following result for the input referred thermal noise of a recycling folded cascode OTA.

$$S_{n,RFC} = \frac{8kT\gamma}{gm1a(1+K)} \cdot \left(\frac{(1+K^2)}{1+K}\frac{gm3a}{gm1a} + \frac{1}{(1+K)}\frac{gm9}{gm1a}\right) \tag{2.7}$$

At a first look at equation 2.7 it is obvious that two terms are smaller than at equation 2.6. The same principle counts for the reduction of flicker noise. It can be seen that a recycling folded cascode architecture offers some attractive features which outperform the standard folded cascode architecture [13].

For a fully differential topology it is necessary to set the common mode feedback. There are some possibilities how a CMFB can be realised [10]. A switched capacitor CMFB presents a good tradeoff and is depicted in the figure 2.7 below.

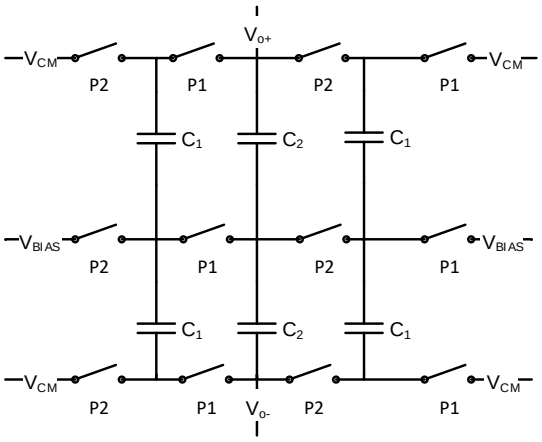

Figure 2.7: Schematic of a switched capacitor CMFB.

In closing the OTA is realised at transistor level by using the gm/id design methodology [15]. In the table below the simulation results are summarised.

Corner analysis at $27°C$						
Parameter	Symbol	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
Voltage gain	A_v	76.38	63.29	66.82	72.96	dB
Gain-bandwidth product	GBW	13.53	10.33	11.85	12.78	MHz
Phase margin	PM	55.99	49.51	51.49	54.52	°
Corner analysis at $-55°C$						
Parameter	Symbol	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
Voltage gain	A_v	74.52	59.97	63.81	70.71	dB
Gain-bandwidth product	GBW	15.83	11.55	13.34	14.38	MHz
Phase margin	PM	54.67	46.8	49.08	52.93	°
Corner analysis at $125°C$						
Parameter	Symbol	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
Voltage gain	A_v	77.45	65.35	68.62	74.26	dB
Gain-bandwidth product	GBW	11.95	9.595	10.35	11.11	MHz
Phase margin	PM	59.91	51.61	53.38	55.71	°

Table 2.7: Simulation results of the implemented recycling folded cascode OTA.

To check if the generated noise of the designed OTA is adequate a noise simulation was performed 2.8.

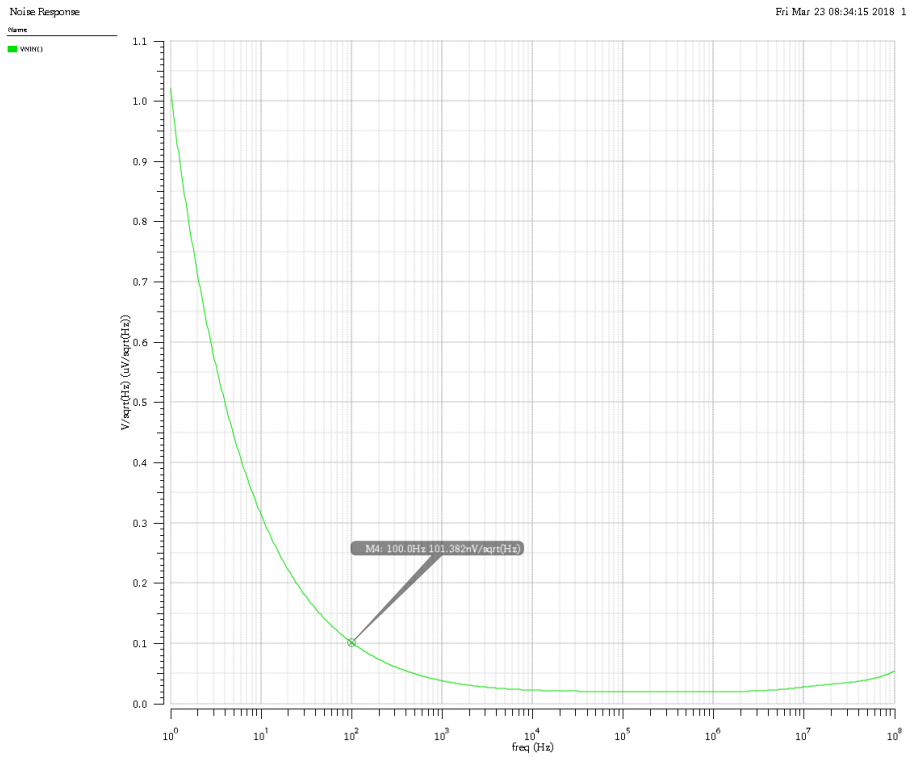

Figure 2.8: Input referred noise of the designed recycling folded cascode OTA. It can be seen that the 1/f corner is definitely below 100Hz which is sufficient enough for our application. For a value of 100Hz the input referred noise holds a value of 101.382 $\frac{nV}{\sqrt{Hz}}$.

2.3.5 Quantizer

In the proposed delta-sigma modulator a 1bit quantizer is realised using a dynamic regenerative comparator and a SR latch depicted below [16]. If the CLK signal is low the nodes at the connection of S and R are charged to the supply voltage V_{DD}. After the CLK signal goes high the nodes getting discharged by the transistors M1 and M2. The quantity of discharge currents is related to the input signals. A feedback loop via the cross-coupled transistors M5 and M6 is formed which amplifies the difference of the inputs to a full-rail output. Dependent of the decision made the result is stored by a SR latch.

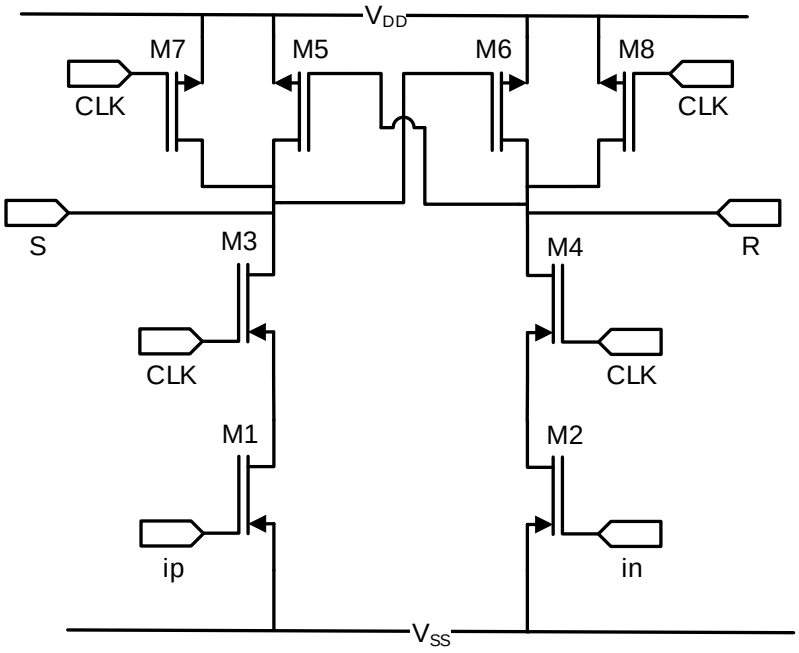

Figure 2.9: Schematic of the proposed latched comparator.

To check if the comparator works correctly a short transient simulation was performed. The comparator is clocked at the same frequency as the delta sigma modulator which is 1MHz. The negative input of the comparator was set to 900mV whereas at the positive input a voltage step was applied. The result is depicted in figure 2.10. The most important parameter of a comparator is called propagation delay. It describes how fast the comparator reacts if the input voltage changes. In detail it characterises the time which is required for the output to reach the 50% point of a transition, after the differential input signal crosses a threshold voltage.

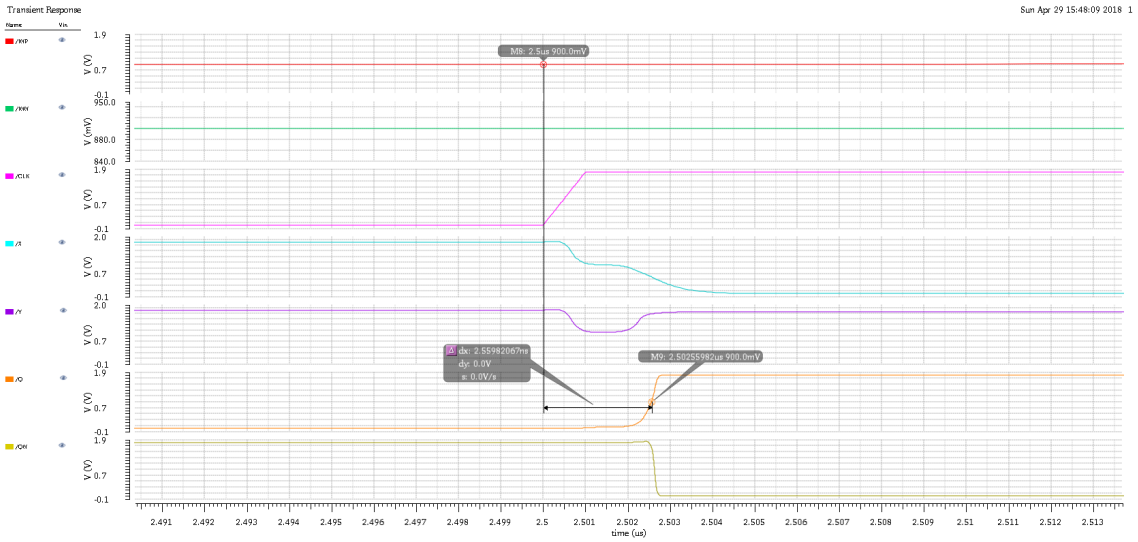

Figure 2.10: Timing diagram of the latched comparator showing the input voltages, the clock signal, the input nodes of the SR latch and the outputs.

In order to check if the comparator works under the harsh temperature conditions a corner analysis was performed.

Parameter	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
t_{pd} $[27°C]$	2.341	2.844	2.582	2.545	ns
t_{pd} $[-55°C]$	1.895	2.298	2.092	2.051	ns
t_{pd} $[125°C]$	2.81	3.409	3.086	3.067	ns

Table 2.8: Corner simulation of the implemented comparator, showing the propagation delay for different temperatures.

As shown in table 2.8 the comparator works fast enough in all temperature environments. In addition the variation of the supply voltages at a temperature of $27°C$ was checked.

Parameter	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
t_{pd} $[1.8V]$	2.341	2.844	2.582	2.545	ns
t_{pd} $[1.6V]$	2.281	2.781	2.52	2.482	ns
t_{pd} $[2V]$	2.415	2.937	2.677	2.618	ns

Table 2.9: Corner simulation of the implemented comparator, showing the propagation delay for different supply voltages.

Parameter	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
V_{off} $[27°C]$	201	127	150	173	μV

Table 2.10: Corner simulation of the implemented comparator, showing the input offset voltage for a temperature of $27°C$.

2.3.6 Clock Generator

The clock generator for producing non-overlapping phases to control the switches is shown in figure 2.11.

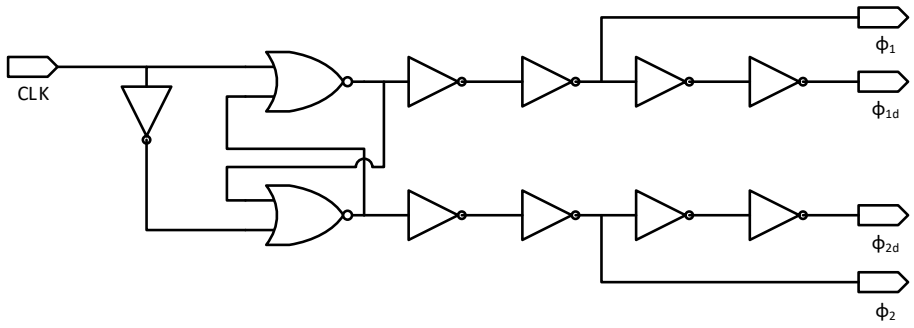

Figure 2.11: Schematic of the clock generator.

It consist of a cross-coupled NOR-gates along with inverters. Further the delayed versions of the clocks can be produced by using several inverters again. The timing diagram of non-overlapping phases and their delayed versions is given in figure 2.12.

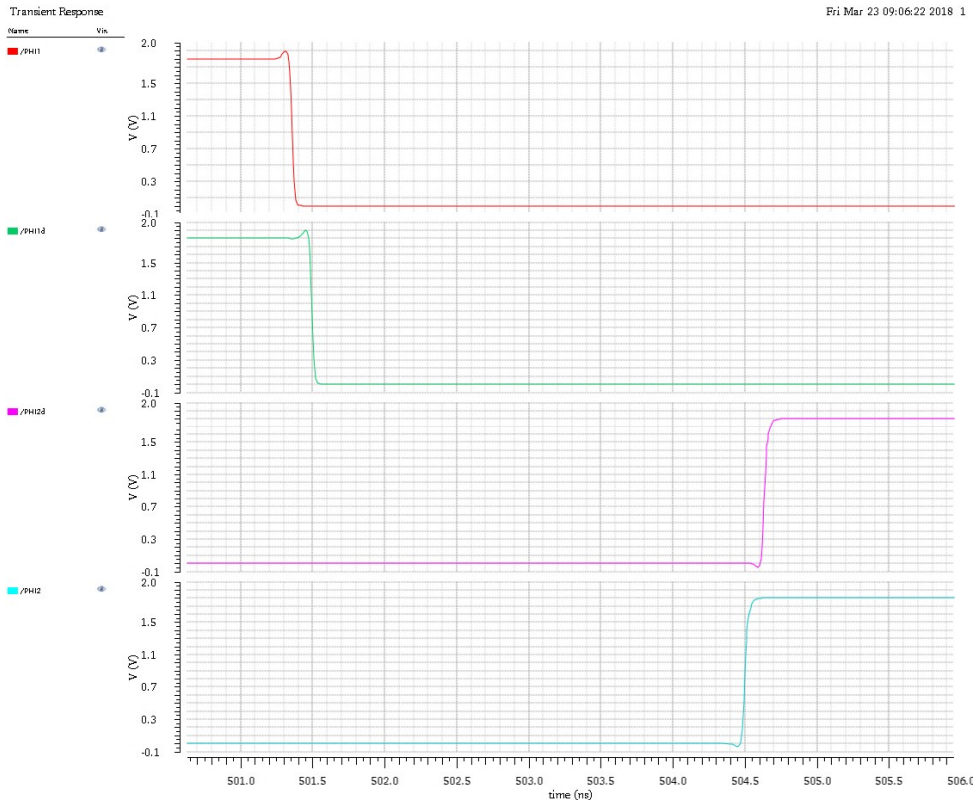

Figure 2.12: Timing diagram of non-overlapping clocks.

The sizes of the inverters are chosen to achieve sufficient delays which decide the non-overlapping time. Non-overlapping time is defined as the time between the falling edge and rising edge at a voltage threshold of 50%. In order to verify the clock generator in more detail a corner analysis was performed. A corner analysis is capable of checking the circuit performance at all process corners. The process corners are composed of a combination of fast or slow NMOS and PMOS transistors. The results of the corner analysis is presented in the table below.

Parameter	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
ϕ_1 to ϕ_2	1.518	2.002	1.704	1.756	ns
ϕ_1 to ϕ_{1d}	345.9	2.448.5	384.8	397.6	ps
$t_{r(\phi_1)}$	116.6	149	125.4	137.7	ps
$t_{f(\phi_1)}$	54.77	72.87	62.81	62.06	ps

Table 2.11: Corner simulation of the implemented clock generator, showing the non-overlapping time and the rise and fall time of ϕ_1.

In addition a monte carlo analysis was performed. A monte carlo analysis is a tool that allows to predict the circuit performance variations, which affect yield. As example the monte carlo simulation of the non overlapping time of the clocks ϕ_1 to ϕ_2 is shown in 2.13.

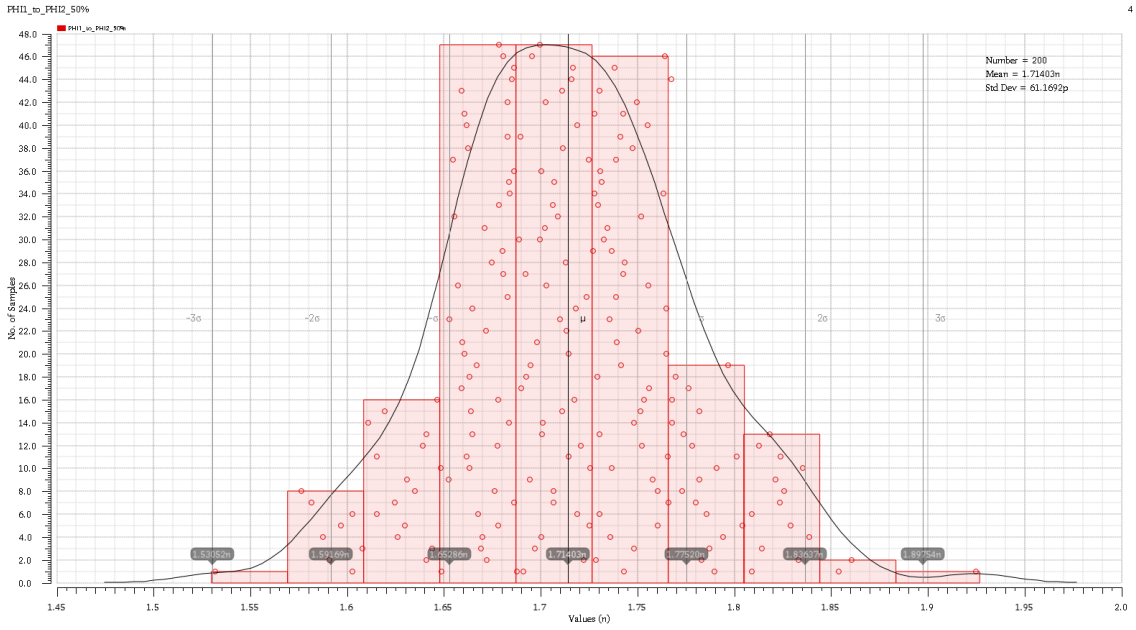

Figure 2.13: Monte carlo analysis of the implemented clock generator. 200 runs result in a mean value of 1.71403ns for the non-overlapping time with a standard deviation of 61.1692ps.

2.3.7 CMOS Switches

The design of switches used in the ADC plays an important role on the overall performance. Switches are designed in such a way that the resistances should match with that of an ideal switch (zero ON resistances and infinite OFF resistance). There is also a parasitic capacitance associated with a CMOS switch resulting in charge injection, clock feed through error, which causes non-linearity in the output such as gain error and offset error [1]. In the figure 2.14 below a transmission gate including a dummy structure to prevent charge injection and clock feed through is presented.

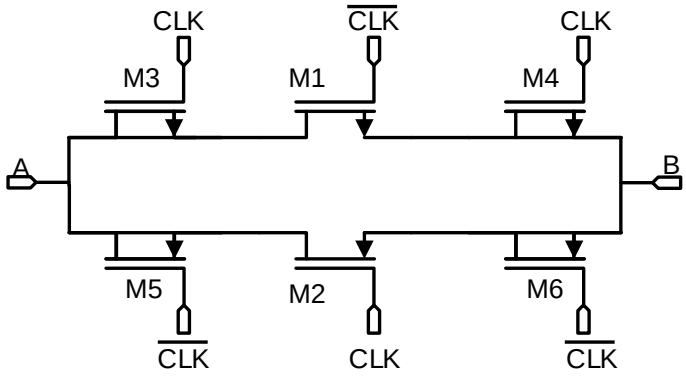

Figure 2.14: Schematic of a CMOS switch, with suitable dummy transistors.

The shown transmission gate was designed in way that the transconductance of the integrator is much bigger than the ON resistance of the transmission gate. This is due to the fact that the ON resistance affects the settling behaviour of the integrator as follows:

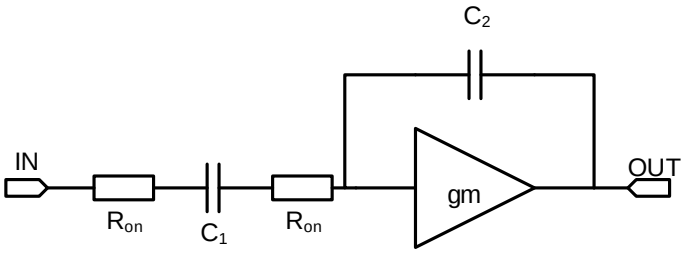

Figure 2.15: Explanation of the settling behaviour of an integrator.

$$\tau = (2R_{on} + \frac{1}{gm})C_1 \tag{2.8}$$

Thus it is necessary to keep $2R_{on} \ll \frac{1}{gm}$.

CMOS switches tend to have high OFF resistances and thus generally provide good approximations of ideal switches in their OFF states. If the OFF resistance should be boosted it can be done by increasing the channel length of the transistor. On the other hand the resistance in the ON state is far from the ideal and can have values in the $k\Omega$ range. This introduces a tradeoff since the ON resistance can be decreased by increasing the channel width which will also diminish the switch OFF resistance. In the following figure the ON resistance of the implemented switch is depicted.

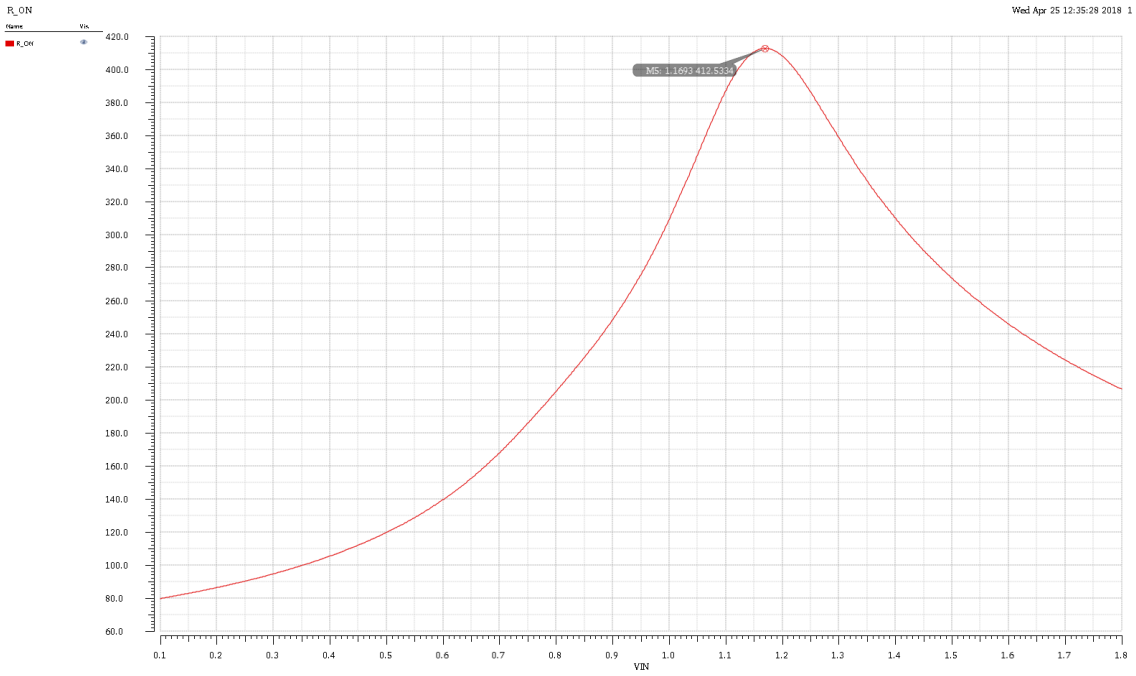

Figure 2.16: ON resistance of the CMOS switch. The input voltage was swept from 0 to 1.8V.

In order to characterise the switch more in detail a corner simulation was performed. The results are shown in the succeeding table below.

Parameter	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
R_{ON} $[27°C]$	331.2	582.6	401.6	427	Ω
R_{ON} $[-55°C]$	325.8	536.8	411.1	436.1	Ω
R_{ON} $[125°C]$	345.8	530	435.6	435.6	Ω

Table 2.12: Corner simulation of the implemented CMOS switch, showing the ON resistance for different temperatures.

2.4 Simulation Results

The delta-sigma ADC is simulated using the Spectre simulator in the Cadence Virtuoso Analog Design Environment with the UMC 180nm CMOS technology. The results are directly computed with the internal spectrum analyser tool.

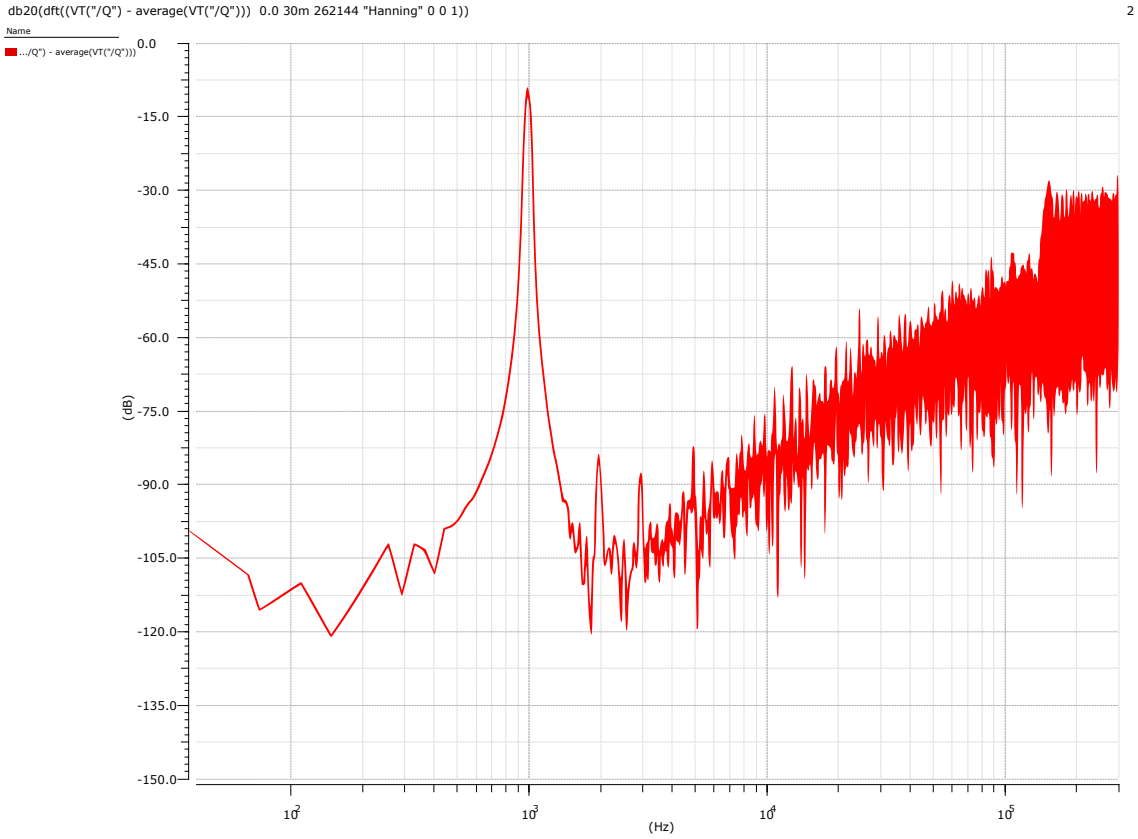

Figure 2.17: Simulation results of the implemented delta-sigma ADC.

Figure 2.17 illustrates the simulated spectrum of the modulator for a -3dBFS sinusoidal input signal at 1 kHz. The spectrum shows a SQNR of around 78dB for a selected bandwidth from 50Hz to 1050Hz, which is in line with the required SQNR level to achieve an ENOB of 12bit. Nevertheless there occur some harmonics at higher frequencies. The power consumption of the whole ADC is about $200\mu W$.

Chapter 3

Sensor and Sensor Interface

3.1 Instrumentation Amplifiers

The main difference between a normal op-amp and an instrumentation amplifier is their input impedance. An instrumentation amplifier is basically an op-amp like amplifier with the distinction that the differential input where the feedback path has been separated from the input path to enable a very high input impedance. In sensor applications there is often a need for differential readouts from source which can have rather high source resistances, hence practically any amount of load presented to the source can be problematic. In such applications instrumentation amplifiers are therefore often used in the place of normal op-amps. A common way of constructing instrumentation amplifiers is shown in figure 3.1.

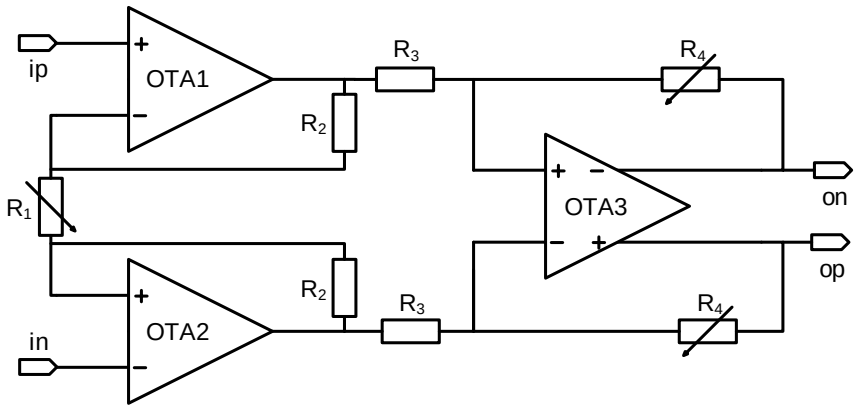

Figure 3.1: Schematic of an instrumentation amplifier.

This structure is fairly straightforward and basically consists of two op-amps at the inputs to keep the input impedance high. Nevertheless it has the problem that its CMRR ultimately depends on the accuracy with which the resistors can be matched. To deal with the different sensors at the input it is feasible to make the gain of the proposed instrumentation amplifier programmable. How a programmable gain can be realised is explained in the first chapter.

In order to amplify the various sensor signals the programmable gain was realised in two stages. The first stage provides a gain of 2,4,8,16,32,64,128 which is set by the first two operational amplifiers (OTA1 and OTA2) and its related resistors R_1 and R_2. For a finer gain tuning the second stage aims for a gain of 0.75 and 1 and is set by the resistors R_4 and R_3. The overall relation of input voltage to output voltage is represented in the following equation:

$$V_{out} = \left(1 + \frac{2R_2}{R_1}\right) \frac{R_4}{R_3} V_{in} \tag{3.1}$$

Finally the instrumentation amplifier was realised at transistor level. The topology of OTA1 and OTA2 was kept fairly simple and is shown in figure 3.2. OTA3 was implemented as folded cascode architecture (figure 2.5).

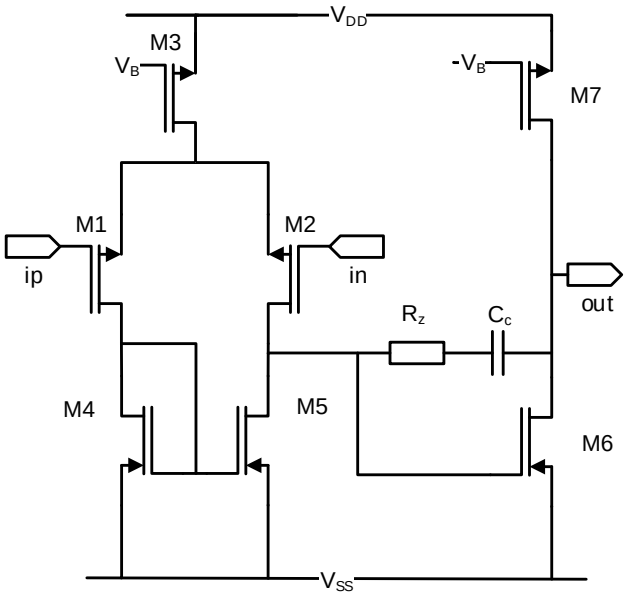

Figure 3.2: Schematic of a single ended OTA. R_z and C_c are used for compensation.

The resulting specification of the implemented operational amplifiers are shown in the table below.

		OTA1/OTA2		OTA3	
Parameter	Symbol	Value	Unit	Value	Unit
Voltage gain	A_v	$\geq$73.2	dB	$\geq$60.4	dB
Gain-bandwidth product	GBW	$\geq$10.9	MHz	$\geq$21	MHz
Phase margin	PM	$\geq$53.81	°	$\geq$72.9	°
Output swing	OSW	$\geq$1.27	V	$\geq$1.27	V

Table 3.1: Simulation results of the implemented operational amplifiers for the IA.

To check the overall performance of the implemented instrumentation amplifier a corner analysis was performed. As an example the corner analysis for a gain value of two is shown in the table below.

Parameter	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
$Gain\ [Res_{min}]$	1.978	1.957	1.976	1.96	V/V
$Gain\ [Res_{max}]$	2.011	2	2.011	2	V/V

Table 3.2: Corner simulation of the implemented instrumentation amplifier for a gain value of two. The temperature was set to $27°C$ and the resistor was varied between its minimum and maximum corner values.

Another important parameter for sensor applications is the occurring error of each individual device in the signal chain. Thus the existing percental errors are shown in the upcoming table.

Nominal Gain	Maximal Error
2	±2.15%
4	±2.18%
8	±2.18%
16	±2.06%
64	±2.7%
96	±5.4%
128	±5.94%

Table 3.3: Selected gain errors of the designed instrumentation amplifier. The values are calculated from corner analyses (e.g. table 3.2).

The minimum unity gain frequency for all possible gain settings is at least 7.4MHz for a 500fF load, whereas the phase margin holds a minimum value of 62°. The average drawn current of the final design was measured to be $118\mu A$ resulting in a total power consumption of $212.4\mu W$. This performance could be achieved with a minimum area of 170x380μm, including suitable dummy structures for the implemented resistors.

3.2 Multiplexer

To select one of the proposed sensor signals and forward them to the instrumentation amplifier a multiplexer is needed. A multiplexer basically consists of several switchable input channels which are gathered to a single output. As shown in figure 3.3 a fully differential multiplexer with four selectable channels was implemented.

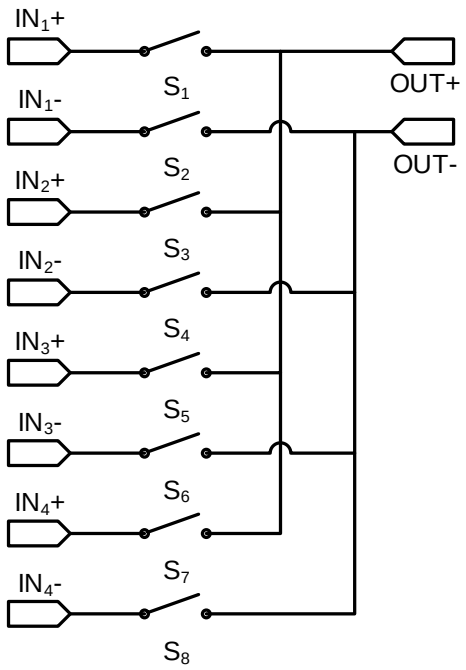

Figure 3.3: Schematic of a differential 4-channel multiplexer.

The design of a multiplexer is a challenging task, since there a some important parameters which must be taken into account. First of all the OFF isolation describes the level of attenuation seen at the output of an open switch. This effect occurs through the parasitic source-body and drain-body capacitances. Next the leakage currents are relevant parameters which must be considered. The on leakage current represents the current flowing through a closed switch and tends to have the most significant effect since it creates an offset voltage across the switch. This leads to another characteristic variable, the ON resistance of the switch which characterises the effective series resistance measured from input to output. Moreover the ON time and OFF time must be observed. The turn on time is the time required to activate an OFF switch to an ON state and is measured from the 50% point of the logic transition to the 90% point of the output transition. The turn off time on the other hand is the time required to deactivate an ON switch to an OFF state and is measured from the 50% point of the logic transition to the 10% point of the output signal.

In order to characterise the multiplexer in more detail some simulations have been performed. First of all the behaviour of the ON resistance of the multiplexer was ascertained and is shown in figure 3.4.

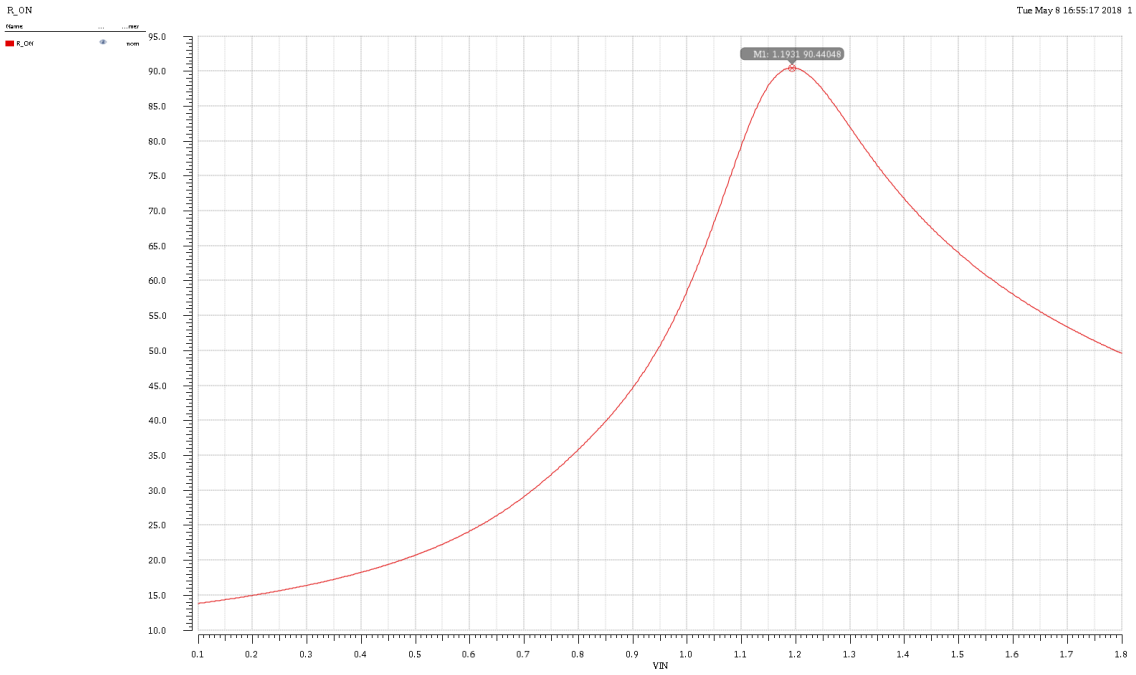

Figure 3.4: ON resistance of the multiplexer. The input voltage was swept from 0 to 1.8V.

The succeeding corner analysis of the ON resistance is shown in table below.

Parameter	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
R_{ON} $[27°C]$	71.98	119.2	87.31	94.59	Ω
R_{ON} $[-55°C]$	70.66	128.4	88.97	96.04	Ω
R_{ON} $[125°C]$	75.36	118.6	89.55	97.02	Ω

Table 3.4: Corner simulation of the implemented multiplexer, showing the ON resistance for different temperatures.

Next the OFF isolation was verified. In order to get a realistic value the output of the multiplexer was directly connected to the input of the instrumentation amplifier. This results in an average value of -70dB for the OFF isolation for an input frequency of 1kHz. The measured leakage currents are negligible, since they hold a value in the pA range. The turn on time holds an average value of 4.4ns, whereas the turn off time is much bigger with an average value of 609ns. Nevertheless the multiplexer is fast enough since the switching frequency of the channel is proposed to be 125Hz.

3.3 Control Logic

While the previous described system is primarily analog some digital control is still necessary to map the different channels of the multiplexer with the various gain settings of the instrumentation amplifier. For the synthesis of fairly simple logic it is usually sufficient to construct a truth table which is then used to synthesise the logic expressions. For the implementation on a first test chip an even simpler method is established, a so called shift register is employed which is shown in figure 3.5.

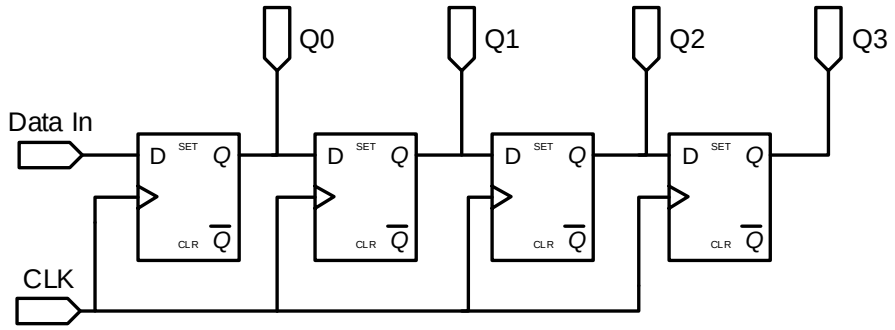

Figure 3.5: Schematic of a 4bit shift register to control the 4 channels of the multiplexer.

A shift register consists of cascaded flip flops which share the same clock signal. The output of each flip flop is then connected to the input of the next flip flop in the chain leading to a circuit that shifts the stored bit array by one position at each transition of the clock input. In detail this means that a 4bit shift register is employed to control the multiplexer and another 7bit shift register is needed to operate the different gain settings of the instrumentation amplifier.

3.4 Current Sensor

3.4.1 High-Side Current Measurement

In a high-side current sensor the measured current is sensed in the supply path with a sense resistor R_{sense} as depicted in figure 3.6. Nevertheless the sensor amplifier must withstand high input common mode voltages, thus it is feasible to reduce the voltage with a resistive voltage divider. Moreover the current consumption of the voltage divider should be kept low in order to not diminish the current through the sense resistor. As manifested in the first chapter a well-wrought choice of the sense resistor is important. In terms of numbers this means: The voltage drop of the sense resistor was set to 100mV for a maximum current of 250mA. This leads to differential voltage of 13.33mV with the resistor values shown in table 3.5. Moreover the branch current is kept low at a value of $20\mu A$.

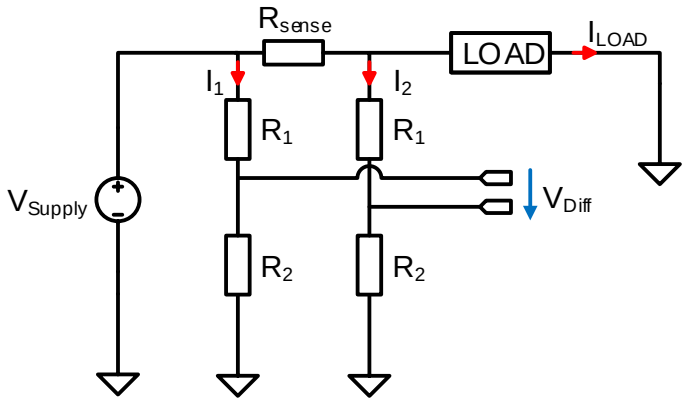

Figure 3.6: Schematic of a voltage divider for high-side current measurements.

This voltage divider was implemented with the use of high-res poly resistors. In the following table the resistor values are summarised:

Parameter	Value	Unit
R_{sense}	0.4	Ω
R_1	520k	Ω
R_2	80k	Ω

Table 3.5: Resistor values of the voltage divider. R_{sense} is accomplished as an external component.

The implementation of poly resistors is always a critical part, since the absolute accuracy of resistors is determined by fabrications tolerance and is limited to the variation of the sheet resistance. This introduces a tradeoff between the accuracy and the area of the resistor. First of all it is necessary to divide the resistor into smaller segments to gain a better matching. This results in a value of $40k\Omega$ for each segment leading to a total number of 15 segments for one branch. To gain a further improvement of the accuracy of each segment a suitable dummy structure was employed. In order to verify the designed voltage divider a monte carlo analysis was performed.

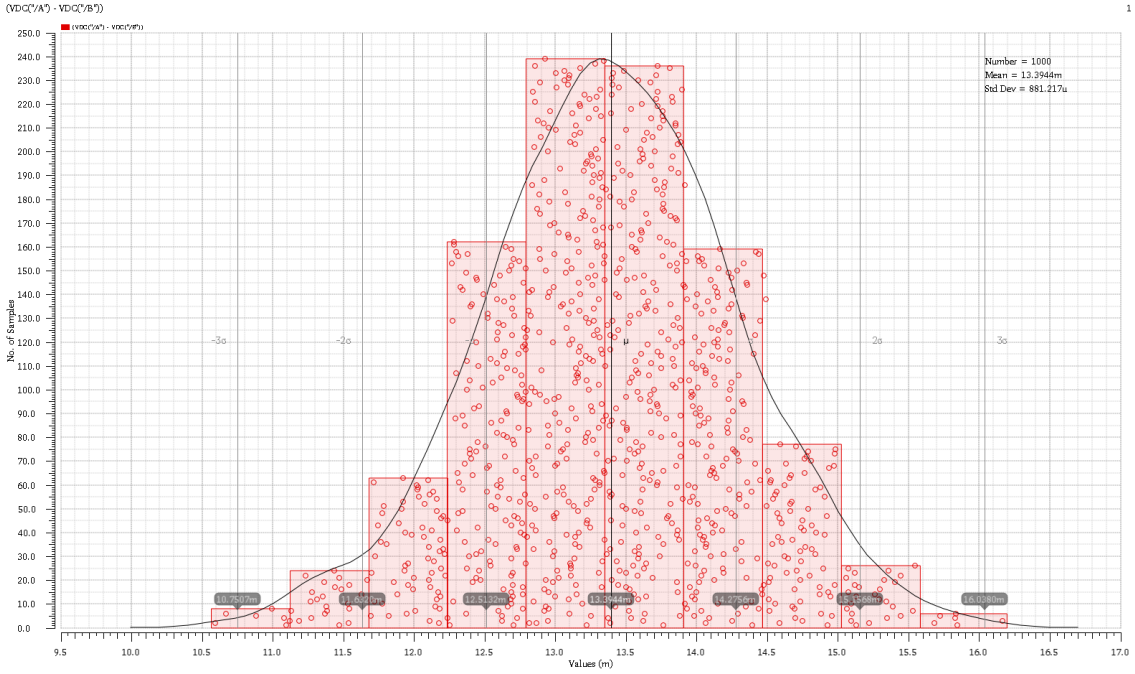

Figure 3.7: Monte carlo simulation of the voltage divider of the high-side current sensor. 1000 runs result in a mean value of 13.3944mV for the differential voltage with a standard deviation of $881.217\mu V$ which is a percental error of $\pm 6.57\%$. This mean that 68,27% of the values are in an interval of $\pm\sigma$. This design uses a total area of 175x400μm, including the dummy structures for each resistor segment.

In order to amplify the small signal to an acceptable value for the ADC a minimum gain value of 96 is preferable. For a gain of 96 the designed instrumentation amplifier holds an error value of $\pm 5.4\%$. This means that the voltage divider induces slightly more error than the instrumentation amplifier.

3.5 Temperature Sensor

3.5.1 On-Chip Temperature Measurement

The circuit of a PTAT element is depicted in figure 3.8. The function relies on the effect that the difference between the voltages of two diodes or bipolar transistors (Q1 and Q2) is proportional to the absolute temperature, if they have different areas and handle the same current. This principle is reflected in the following equation [11]:

$$V_{PTAT} = I_5 \cdot R_2 = \frac{W_5}{W_2} \frac{k \cdot T \cdot ln(n) \cdot R_2}{q \cdot R_1} \tag{3.2}$$

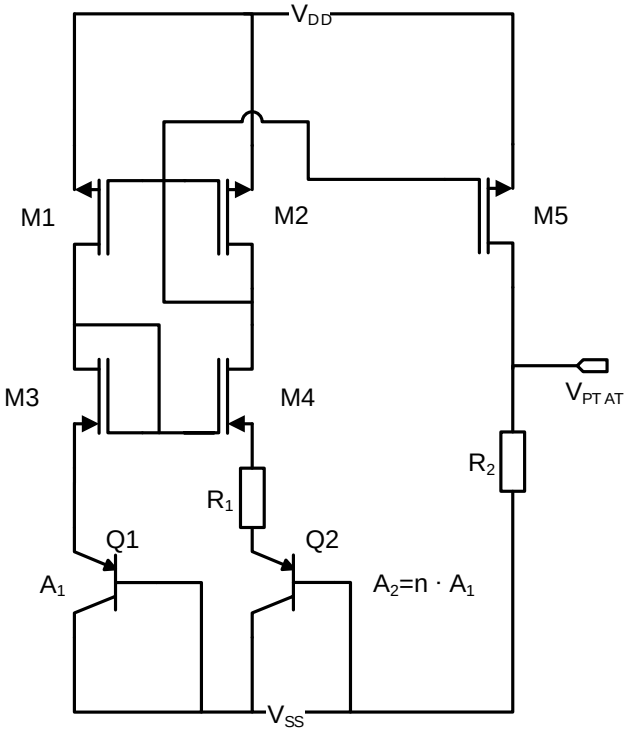

Figure 3.8: Schematic of the designed PTAT temperature sensor.

The PTAT element was designed that ratio of the resistor $\frac{R_2}{R_1}$ is 0.5 and the ratio of $\frac{W_5}{W_2}$ is 2. The scaling coefficient n describes the factor how much bigger the area of the second bipolar transistor is. This introduces a tradeoff since a bigger number results in a poor layout structure. A scaling coefficient of $n = 24$ introduces an adequate solution since the arising layout is perfect quadratic, which enables the possibility to position the transistor Q1 perfectly in the centre.

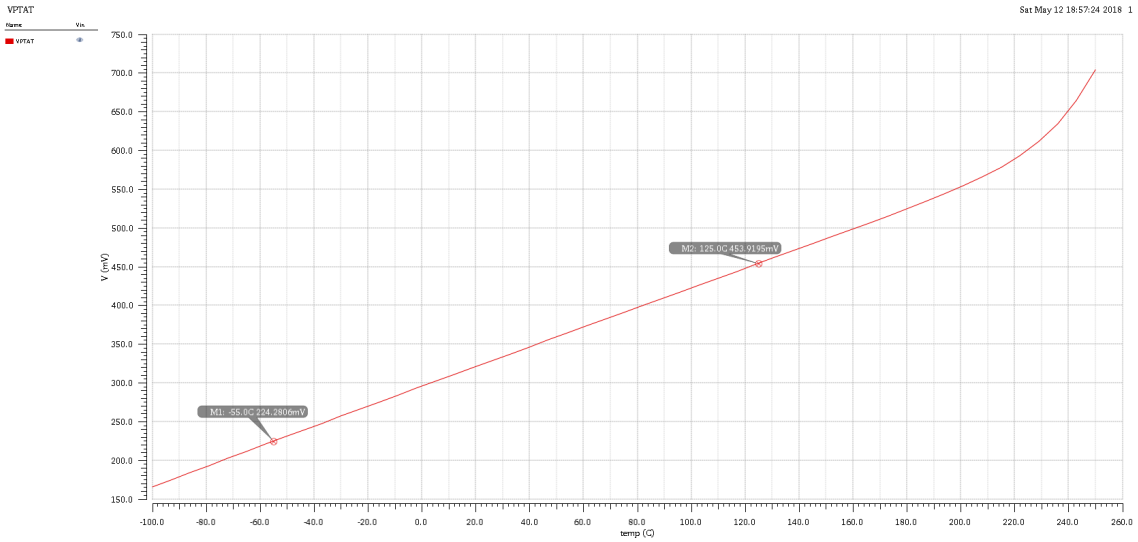

Figure 3.9: Simulation of the output voltage of the designed PTAT temperature sensor for a temperature range from $-100°C$ to $+250°C$.

As depicted in the figure above the designed PTAT cell offers a good linearity in the specified temperature range from $-55°C$ to $+125°C$ and leaves some headroom even up to $+200°C$. As a result a broad output voltage range from 224.28mV for $-55°C$ to 453.92mV for $+125°C$ is available. Another significant parameter is the sensitivity of a temperature sensor. The following table shows a corner simulation of the average sensitivity of the circuit.

Parameter	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
Sensitivity	1.296	1.307	1.299	1.296	$mV/°C$

Table 3.6: Corner simulation of the implemented PTAT temperature sensor, showing the average sensitivity.

The average drawn current of the final design was measured to be $103\mu A$ resulting in a total power consumption of $185.5\mu W$. Nevertheless the obtained values leaves some clearance for improvement, since the power consumption is slightly high with respect to the gained sensitivity.

3.5.2 Temperature Measurement with resistive Temperature Sensors

The most common way to find an unknown resistance value is the wheatstone bridge [9]. It is used to measure small resistance changes like in sensor applications, for example in resistive temperature measurements. It converts a resistance change to a voltage change. In order to dimension the wheatstone bridge for resistive temperature measurement with a PT1000 element some parameters must be clarified. First the self heating of the PT1000 element should be kept to a minimum, hence the power dissipation must be considered. Therefore a power dissipation of $100\mu W$ is a good target. For the given specification the value of the PT1000 element varies from 500.6Ω for $-125°C$ to 1479.51Ω for $+125°C$.

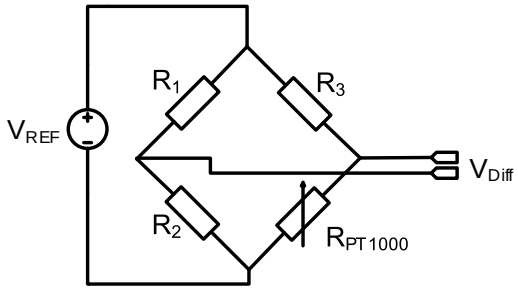

Figure 3.10: Wheatstone bridge circuit diagram. R_{PT1000} represents the unknown value which is to be measured.

The behaviour of this readout circuit is explained in the equation below:

$$V_{Diff} = \left(\frac{R_2}{R_1 + R_2} - \frac{R_{PT1000}}{R_{PT1000} + R_3} \right) V_{REF} \tag{3.3}$$

This wheatstone bridge was implemented with the use of high-res poly resistors. The following resistor values were obtained:

Parameter	Value	Unit
R_1	32.4k	Ω
R_2	14.7k	Ω
R_3	4.7k	Ω

Table 3.7: Resistor values to meet the gained specifications.

This values lead to a differential voltage range from 131mV for $+125°C$ to 389mV for $-125°C$ for a reference voltage of 1.8V. In order to calculate back to the actual temperature it is necessary to exactly known one resistor value. Therefore R_3 was carefully implemented with the use of high-res poly silicon and in addition a suitable dummy structure was established. This introduces a tradeoff between area an accuracy as discussed before in the chapter for high-side current measurement.

Chapter 4

Layout and Radiation Hardening

4.1 Radiation Hardening

Radiation hardening plays a crucial role for space applications. This section will briefly explain the most common effects and discuss possible prevention techniques [17]. First of all the effects can be divided into two groups:

- Total ionizing dose: Irradiation generates continuous particles which cause accumulative charges in a semiconductor material resulting in device failures. This effect induces threshold voltage drift of transistors, increases the channel and junction leakage currents, diminishes the transconductance and moreover degrades the gate oxide till its breakdown.
- Single event effect: In general single event effects are caused by high energy particles when they hit the semiconductor material. This induced charges are collected and effect sensitive nodes resulting in latch-up, data upset, immediate parasitic currents or voltages and may unleash a breakdown of the gate oxide.

There a some possibly methods to prevent those effects:

- Radiation hardness by process: This means that special processing techniques like silicon on insulator are employed.
- Radiation hardness by design: This method affects the cell-level design including enclosed-layout transistors and guard rings.

As a first step the use of guard rings is proposed, due to the fact that its implementation is fairly straightforward. This measure will directly reduce the occurrences of latch-up. Latch-up is caused by the interaction of parasitic bipolar transistors. This effect leads to a short between the supply rail and the ground rail, resulting in a permanent damage of the device. There are some basic rules that conduct an efficient solution:

- NMOS transistor: p+ guard ring tied to ground potential.
- PMOS transistor: n+ guard ring tied to supply potential.
- Contacts: Place substrate and well contacts as close as possible to the source connection of the MOS transistor.

In the near future the implementation of enclosed layout transistor may be proposed to ensure that the final ASIC is more resistant to radiation. In the figure below the basic structure of an enclosed layout transistor is depicted. While standard transistors 4.1 a.) do not prevent the occurence of TID induced leakage currents form source to drain some special layout strategies have been introduced. Therefore the enclosed layout transistor has been developed. As shown in figure 4.1 b.) the ELT provides a total prevention of the parasitic leakage path since the drain region is placed inside the gate. Nevertheless an ELT introduces some drawbacks as for example it exposes a significantly larger area than the standard transistor.

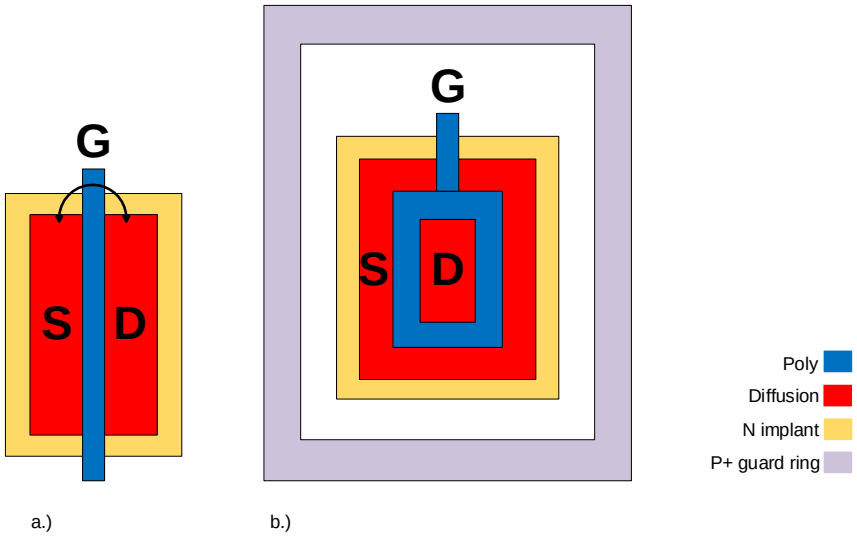

Figure 4.1: a.) Layout of a standard NMOS transistor. b.) Basic structure of an enclosed layout NMOS transistor including an appropriate p+ guard ring.

4.2 ESD Protection of Integrated Circuits

The reliability of a device is affected by several issues. The most important ones are the problems caused by ESD events which can occur during manufacturing or improper device handling. In order to increase the yield and improve the reliability a suitable protection circuit is needed to ensure the ESD robustness.

An on-chip ESD protection circuit should establish a proper current path between any possible combinations of two different pins of an IC. In figure 4.2 an ESD protection scheme is illustrated [18]. The IO pad is protect with a primary ESD circuit which bypasses the occurring ESD current to the rails. A power clamp is used to directly absorb ESD stress between VDD and GND protecting the internal circuits. To handle ESD effects between different power domains a rail-to-rail based circuit is needed.

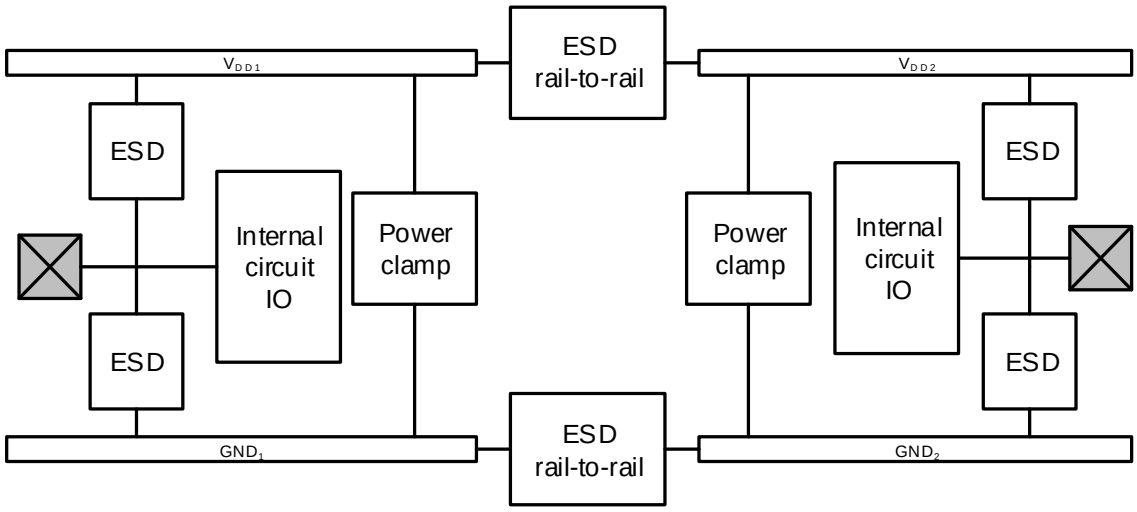

Figure 4.2: Blockdiagram of an ESD protection scheme.

In the following section a possible ESD protection solution of an analog IO pad is presented. First of all a suitable ESD protection device must be encountered. Such a device should be able to employ a proper current path between the input pad and the rails. Depending on the application this devices are usually diodes, bipolar or MOS transistors. Typically for an analog IO pad a MOS transistors is employed [18]. There exist some solutions how a MOS transistor can be used as an ESD protection device. The three most common ones are depicted in figure 4.3.

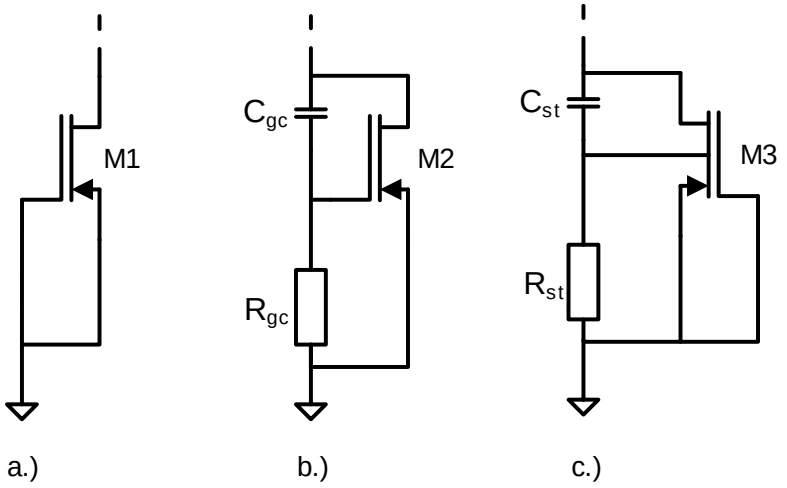

Figure 4.3: Schematic of possible implementations of MOS transistors as ESD protection devices. a.) ground-gated NMOS (ggNMOS), b.) gate-coupled NMOS (gcNMOS), c.) substrate-trigger NMOS (stNMOS)

In a ggNMOS the parasitic NPN transistor gets reversed biased if an ESD event occurs at its drain connection. The induced current which is flowing to ground introduces a voltage across the base emitter junction triggering the parasitic NPN transistor.

On the other hand in a gcNMOS the holding time of the coupled gate voltage is determined by the capacitor C_{gc} and resistor R_{gc} making the gcNMOS active only in ESD events. If an ESD event occurs the current is discharged to ground by turning on the device. This introduces a tradeoff since the turn on time is an important factor which describes the performance during ESD events. If the time is too short the gcNMOS will not have enough time to discharge the current, whereas if the time is too long the speed of the internal circuits will be diminished.

In a substrate-trigger NMOS the capacitor C_{st} and the resistor R_{st} must be tuned to couple a suitable voltage to the body of the parasitic NPN transistor in order to lower the trigger voltage of the NMOS in ESD events [19]. This method improves the turn on uniformity of the transistor. Compared with the gcNMOS design the stNMOS reduces the stress across the gate oxide resulting in an improvement of the ESD robustness.

For the used UMC 180nm technology ggNMOS transistors are recommended. In Figure 4.4 a.) a possible implementation is shown. Gated NMOS and PMOS transistors are employed to ensure the ESD path and a series resistor is used to limit the occurring current. In order to prevent latch-up of the transistors guard rings are applied.

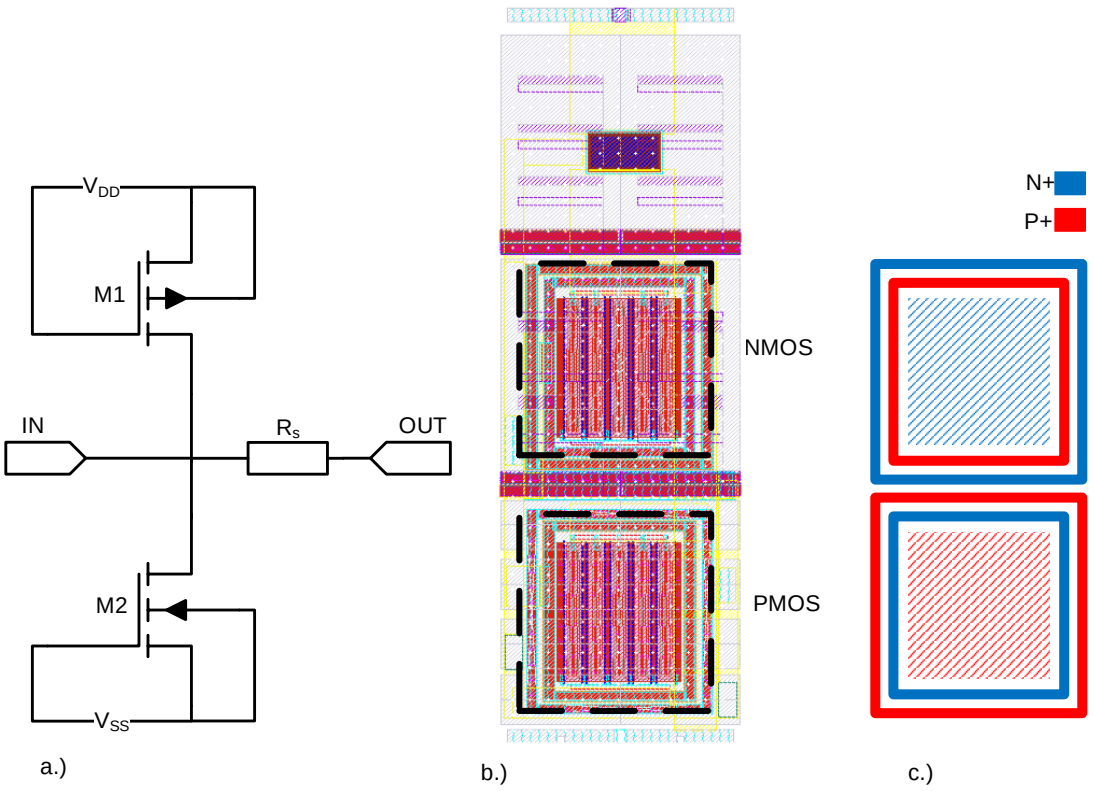

Figure 4.4: a.) Schematic of an ESD protection circuit for an analog IO structure. b.) Layout of the implemented analog IO pad. c.) latch-up prevention method. NMOS transistor: P+ pick up ring for the bulk connection and N+ guard ring. PMOS transistor: N+ pick up ring for the bulk connection and P+ guard ring.

In order to test the developed ESD protection circuit a suitable method is used. One of the most important test methods is the human body model, which describes the transfer of electrostatic charge from a charged human body to the DUT. This common industrial test method is standardised to ÖVE/ÖNORM EN 60749-26. Figure 4.5 shows a simplified equivalent circuit of HBM ESD conditions. It consists of a charging capacitor ($C_1 = 100pF$) and contact resistance ($R_1 > 1M\Omega$, $R_2 > 1.5k\Omega$) between the charge source and the DUT.

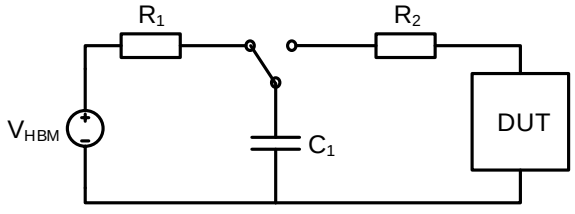

Figure 4.5: Equivalent circuit diagram of the HBM test method.

4.3 Bias Current Generation

In analog or mixed-signal circuits a number of fixed reference currents for biasing the amplifier, comparators and digital logics is required. This current can not be generated directly which means a suitable circuit must be employed. The most common topologies are the beta-multiplier or the use of an off chip resistor in combination with a reference voltage. For a first test chip the use of an off chip resistor is absolutely sufficient. In order to distribute the generated current a so called current mirror is employed as shown in the figure below.

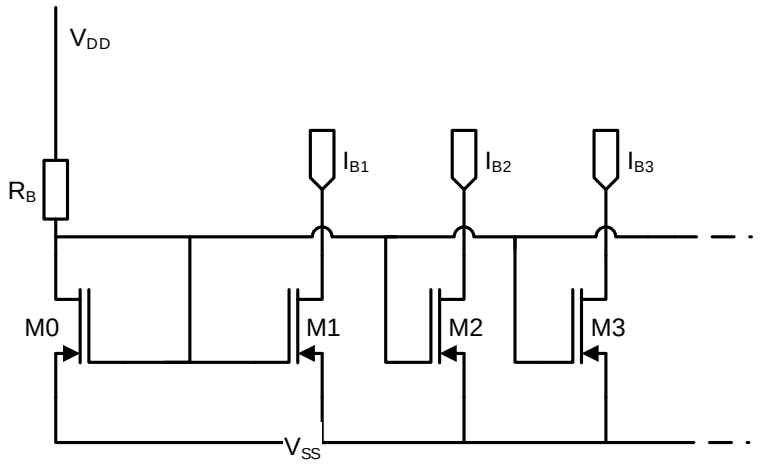

Figure 4.6: Schematic of the bias current generation. An external resistor R_B generates a reference current which is then distributed with scaled current mirrors.

Parameter	Value [ff]	Value [ss]	Value [snfp]	Value [fnsp]	Unit
I_B $[27°C]$	10.32	9.673	9.888	10.1	μA
I_B $[-55°C]$	10.18	9.492	9.726	9.935	μA
I_B $[125°C]$	10.56	9.919	10.13	10.35	μA

Table 4.1: Corner simulation of the implemented bias current generation, showing as example a 10 μA bias current for different temperatures.

4.4 Layout

The test chip is developed in 180nm CMOS technology provided by UMC. Figure 4.7 shows the implementation of the whole test chip. The key to a perfect functioning ASIC is a good layout structure resulting in a dedicated procedure. First the layout rules which are provided by the manufacturer must be followed strictly. Next a suitable floor plan should conduct a dense layout structure. Furthermore there are some basic layout guidelines that support a proper design flow [20]. In order to test if the chip works correctly or not, some testability features are employed. This includes the use of output buffers to ensure that the most relevant signal nodes can be measured correctly.

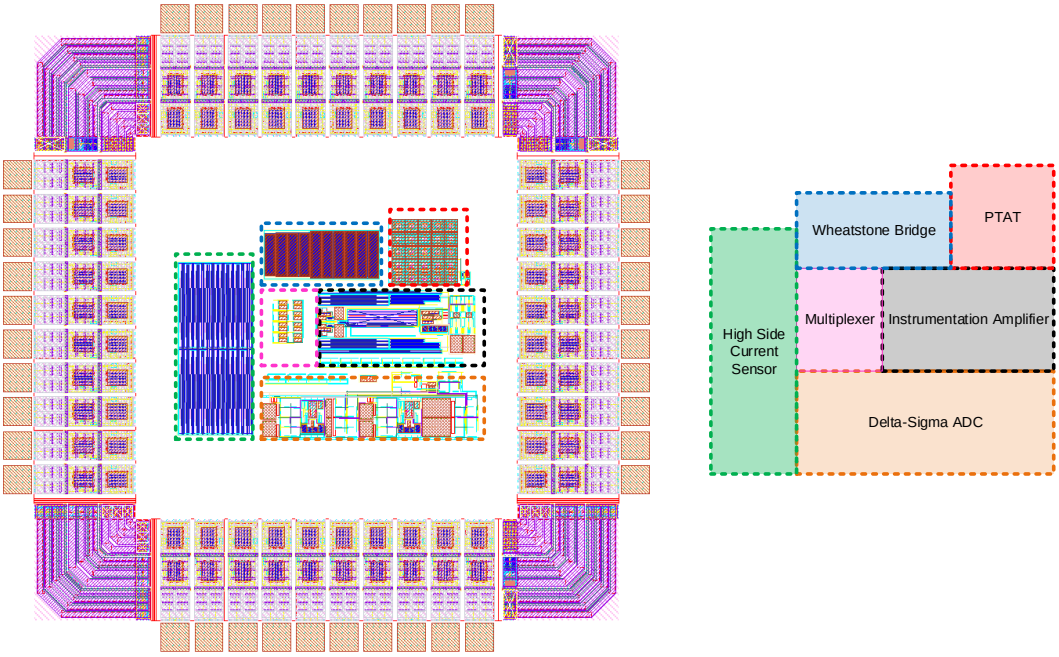

Figure 4.7: Complete layout of the test chip, illustrating a floor plan containing the designed building blocks.

Chapter 5

Conclusion and Future Work

In this work a system monitoring architecture for space applications has been presented. A fully differential second order switched capacitor delta-sigma modulator was implemented. The final simulation showed an effective resolution of 12bit which is inline with the given specification. Nevertheless the appearance of some harmonics opens a possible starting point for further optimisation.

Moreover a sensor interface for various measurements was proposed. Therefore a programmable instrumentation amplifier including a 4-channel multiplexer with a suitable control logic was designed. A high-side current sensor for accurate current measurement with the drawback of area consumption was introduced. An on-chip temperature sensor was realised with a common PTAT cell. Nevertheless the current design leaves some clearance for perfecting regarding the sensitivity as well as the power consumption. For off-chip temperature sensing a simple PT1000 element including a wheatstone bridge as readout circuit was used.

As a final step an adequate layout was designed with use of proper radiation hardening techniques. In addition an appropriate ESD protection scheme was employed. Future work deals with the measurement and verification of the fabricated test chip. Further on the measured results have to be compared with the gained simulation results.

Chapter 6

Appendix

6.1 Block Diagram

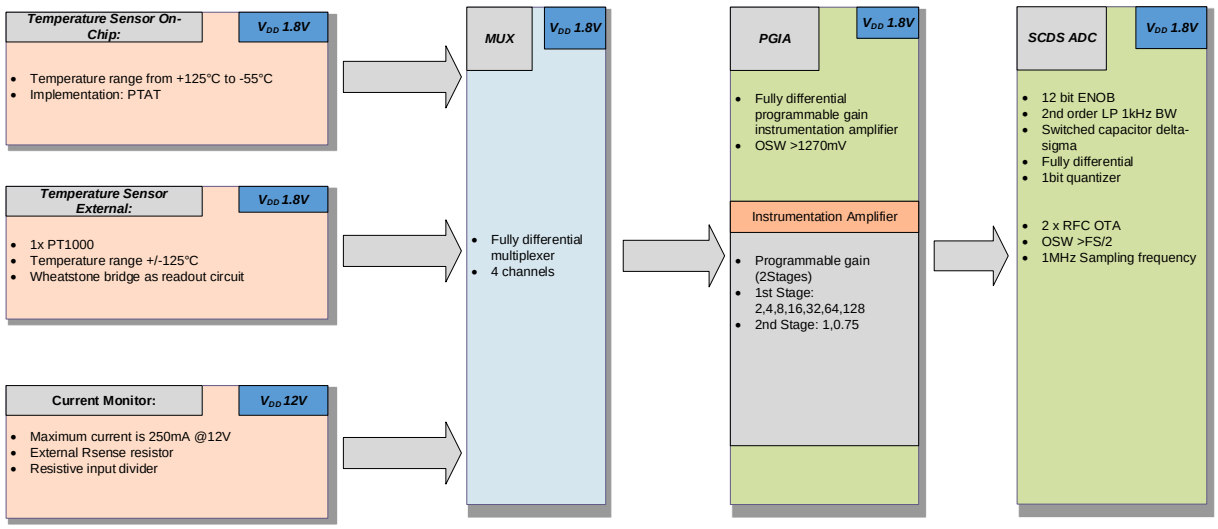

Figure 6.1: Advanced block diagram of the developed system monitoring architecture.

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