Alexander Connaughton MEng.

Secondary Side Controlled Flyback Converter

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AFFIDAVIT

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Signature

For my parents, Peter & Liz,
and my siblings, Mark & Emma.

Contents

Abstract

The ever increasing market for consumer electronics warrants continual industrial interest in consumer power supplies; particularly for laptop, tablet and mobile phone charging adapters. Consequently, universal adapters compatible with multiple devices/output voltages promise to become the new standard. The Flyback topology is a popular choice for adapters due to its low parts count and it is becoming a more attractive option for medium power (50-100 W) adapters as component performance improves and as innovative Flyback control strategies are discovered.

This thesis presents a novel Flyback control strategy herein referred to as the *Secondary Side Controlled Flyback* concept. In contrast to the conventional control approach, this concept proposes moving the controller from the input side to the output side, and communicating back to the primary switch via the coupled inductor itself. This provides direct access to the output voltage allowing simpler, faster and more precise output voltage sensing without the need for any additional optical or magnetic coupling for cross-isolation "communication".

The aim of this thesis is to investigate the concept's feasibility, viability and capability. To prove the feasibility, novel drain-source voltage sensing circuits were developed to execute the new cross-isolation "communication" approach. These were found to be faster than a more conventional opto-isolator approach and simultaneously offer soft-switching. To explore the concept's viability, these sensing circuits were employed on custom 65 W demonstrators, upon which the performance of three control schemes was tested for load-change response, switching frequency variation and efficiency. Although low-load efficiency remains a subject for future work, peak full-load efficiency was measured at 90.77 % making the proposed concept well placed to compete with other state-of-the-art Flyback control solutions. This was achieved using the novel so called "variable-frequency, variable-ON-time" control scheme. Lastly, a new reverse-power-flow concept was demonstrated to show the Secondary Side Controlled Flyback's capability for future multiple-output-voltage adapter compatibility.

Zusammenfassung

Der sich ständig vergrößernde Markt an Konsumelektronik garantiert kontinuierliches Interesse der Industrie an Netzteilen, besonders für Laptop-, Tablet- und Smartphone-Ladegeräte. Daher ist zu erwarten, dass universelle Stromversorgungen, die kompatibel zu vielen Geräten und unterschiedlichen Ausgangsspannungen sind, zu einem neuen Standard werden. Als Schaltungstopologie für solche Adapter wird, wegen des geringen Bauteilaufwands, häufig der Sperrwandler verwendet, der aber meist auf kleinere Leistungen für Telefon-Ladegeräte beschränkt ist. Dennoch gewinnt diese Topologie an Attraktivität auch für Netzteile mittlerer Leistung (50-100 W), zumal Bauteile mit verbesserten Eigenschaften verfügbar und innovative Regelungsstrategien diskutiert werden. Diese Arbeit stellt eine neue Regelungsstrategie für Sperrwandler vor, die nachfolgend als *Secondary Side Controlled Flyback* bezeichnet wird. Im Gegensatz zu üblichen Regelverfahren, wird die Regelung von der Eingangs- zur Ausgangsseite verlagert und die Kommunikation zum Primärschalter über den Leistungs-Übertrager selbst bewerkstelligt. Der damit ermöglichte direkte Zugriff auf die Ausgangsspannung durch die Regelschaltung erlaubt einfachere, schnellere und genauere Messung der Ausgangsspannung, ohne zusätzliche, über die Isolationsbarriere optisch oder magnetisch übertragene, Kommunikation, wodurch der Bauteilaufwand weiter verringert wird. Diese Arbeit untersucht die Machbarkeit, Brauchbarkeit und Eignung dieses Konzepts. Zum Nachweis der Machbarkeit wurden neue Schaltungen zur Messung der Drain-Source-Spannung entwickelt, um die neue Signalübertragung über die Isolationsschwelle hinweg umzusetzen und gleichzeitig verlustfreies Schalten anzubieten. Um die Brauchbarkeit des Konzepts auszuloten, wurden diese Messschaltungen in einem 65 W-Demonstrator eingesetzt, womit die Leistungsfähigkeit von drei Regelungsstrukturen im Hinblick auf Lastsprünge, Änderung der Schaltfrequenz und Wirkungsgrad getestet wurde. Bei Nennlast wurde ein maximaler Wirkungsgrad von 90.77 % gemessen. Schließlich wurde ein neues, verlustfreies Verfahren zur Verringerung der Ausgangsspannung mittels Leistungsumkehr demonstriert, um Kompatibilität mit künftigen Netzteilen für mehrere wählbare Ausgangsspannungen zu erzielen.

Acknowledgements

Firstly, I would like to thank Annette Mütze for her unwavering support throughout my time at TU Graz and Maryam Saeedifard for evaluating this thesis.

Secondly, there are six people without whom this thesis would not have been possible. With this in mind I would like to thank:

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Ken for the best telephone tech-support in the multiverse,
and Christiane for an entirely platonic work relationship.

Thank you all.

Chapter 1

Overview

1.1 Thesis Objectives

In co-operation with *Infineon Technologies Austria* AG, this thesis presents an investigation of a novel power adapter concept; the Secondary Side Controlled Flyback converter. The fundamentals of this new concept (detailed in Chapter 4) were presented to the author by *Infineon Technologies Austria* AG in late 2013 and acted as the starting point for the research conducted by the author. The overall research objective can be summarised as follows:

"To investigate the feasibility, viability and capability of the Secondary Side Controlled Flyback converter concept as a real-world power adapter solution."

The target application for this concept was for a 65 W universal adapter for consumer electronics, providing a clean 20 V_{DC} output from either high- or low-line input voltage (120 V_{RMS} or 230 V_{RMS}). To achieve the above objective within this context, the author focused on four diverse yet interrelated sub-objectives:

- To design precise yet inexpensive drain-source voltage sensing circuits for reliable operation.
- To develop a control scheme with as much regulation on the secondary side as possible while achieving good power adapter performance.
- To demonstrate competitive efficiency using the proposed sensing circuits and control scheme on a working prototype.
- To explore any unique features and advantages that may arise from a controller placed on the secondary side of the Flyback converter.

1.2 Credit and Contributions to State of the Art

While all prototyping, measurements and analyses presented in this thesis are the sole work of the author, the credit for some important novel ideas is split between the author and *Infineon Technologies Austria AG*. Tab. 1.1 summarizes the contribution from each side.

Table 1.1: Credit for origin of specific novel ideas presented in this thesis.

Infineon Technologies AG	Author
Secondary Side Controlled Flyback	Constant ON-time Control
Variable ON-time Control (concept)	Double-pulse Primary Side Sensing
Reverse Power Flow (concept)	Start-Up Routine
	Lossless Synchronous Rectification Sensing
	Variable ON-time Control (Implementation)
	Transformer Design Approach for COT and VOT
	Double-Pulse Primary Side Sensing for Q-ZVS
	Soft Negative Current Turn-ON requests
	Variable Frequency, Variable ON-time Control
	Reverse Power Flow (Implementation)
	VOT Reverse Power Flow

All prototype development, including simulation, PCB design and experimental analysis, was undertaken by the author.

1.3 Related Publications

This thesis resulted in the following scientific publications:

List of Journal Publications

"Investigation of a Soft-Switching Flyback Converter with Full Secondary Side Based Control" - *Alexander Connaughton, Arash P. Talei, Kennith Leong, Klaus Krischan, Annette Muetze.*

Published in *IEEE Transactions on Industry Applications*, pp. 1-15, November/December *2017* - Print ISSN: 0093-9994.

"Variable ON-time Control Scheme for the Secondary Side Controlled Flyback Converter". - *Alexander Connaughton, Arash P. Talei, Kennith Leong, Klaus Krischan, Annette Muetze.*

Submitted to *IEEE Transactions on Power Electronics*, November 2017 - Currently Under Review.

"Secondary Side Controlled Flyback with Improved Efficiency and Reverse Power Flow". - *Alexander Connaughton, Kennith Leong, Klaus Krischan, Annette Muetze.*

Submitted to *IEEE Transactions on Power Electronics*, November *2017* - Currently Under Revision.

List of Conference Publications

"New Control Concept for Soft-Switching Flyback Converters with Very High Switching Frequency" - *Alexander Connaughton, Kennith Leong, Klaus Krischan, Annette Muetze.*

Presented at/in IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 355-361, March *2016*.

"Quasi-Constant Frequency Secondary Side Controlled Flyback Concept with Variable ON-Time" - *Alexander Connaughton, Arash P. Talei, Kennith Leong, Giuseppe Bernacchia, Gerald Deboy.*

Presented at/in PCIM Europe 2017; International Exhibition and Conference for Power Conversion and Intelligent Motion, pp. 1-8, May *2017*.

1.4 Structure of Thesis

The main body of work for this thesis begins with an introduction to the Flyback converter in Chapter 2. Elementary explanations for several concepts pertinent to the presented research are included. Chapter 3 gives an overview of the existing state-of-the-art for advanced Flyback converter concepts, with reference to the preceding fundamentals.

Chapter 4 details the original Secondary Side Controlled Flyback concept as initially presented to the author, and how this concept expands upon the state-of-the-art.

Subsequent Chapters 5, 6 and 7 present the author's research in approximately chronological order, with each chapter dedicated to one part of the initial overall objective: the *feasibility*, *viability* and *capability* of the Secondary Side Controlled Flyback. Furthermore, the three sub-objectives listed in Section 1.1 (the drain-source voltage sensing, the control scheme, and efficiency) are addressed within each of these chapters, with every chapter presenting improvements based on the conclusions of the preceding chapter. These chapters each present several of the author's own improvements to the state-of-the-art, and to the original Secondary Side Controlled Flyback concept itself.

Chapter 8 summarizes all of these chapters, assessing the original objective with reference to the preceding experimental analysis. This thesis ends with suggested future work that was out of the scope or time-scale of the research presented here.

Chapter 2

Introduction

To provide context for the novel content presented in the main Chapters 5-7, this chapter gives an overview of the Flyback topology, followed by a qualitative summary of power MOSFETs. More specific technical background pertinent to the main chapters is given within the chapters themselves.

2.1 Flyback Converter Topology

Fig. 2.1 shows a schematic of the Flyback topology in its most basic form. It consists of a two-winding coupled inductor with additive polarity (L_1 and L_2), an active switch on the input side (S_1), a rectifying diode on the output side (D_0), and filter capacitors C_{IN} and C_{OUT} [1]. Functionally, the Flyback behaves like a buck-boost converter; offering an output voltage (V_{OUT}) smaller or larger than the input voltage (V_{IN}) depending on the switching duty cycle of S_1.

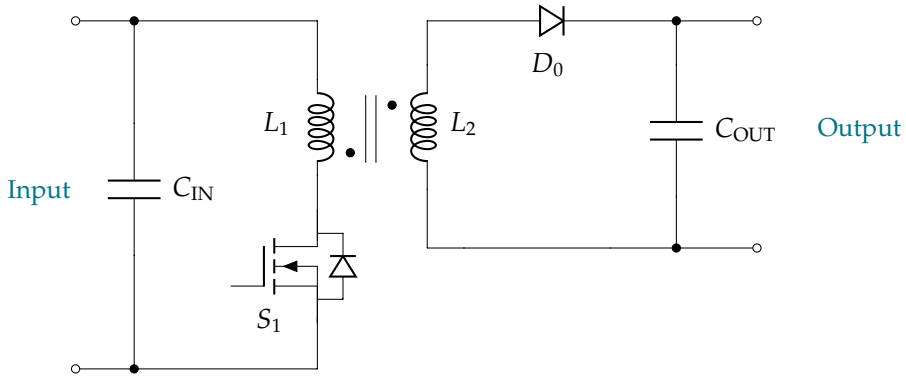


Figure 2.1: Fundamental principle schematic of the Flyback converter.

However, the split inductance offers the addition of galvanic isolation between input and output sides, a voltage transformation from a non-unity winding turns-ratio (N), and positive output polarity [1, 2]. This allows isolated DC-DC power conversion with a small parts-count. Due to the typical switching frequencies and input voltages involved, modern line adapter Flyback's are generally implemented using super-junction MOSFETs as the device for S_1 [3–5].

2.1.1 Comparison to Other Topologies

Many other comparable topologies exist for isolated DC-DC power conversion. Tab. 2.1 summarizes content from [6] and [7], comparing the advantages and disadvantages of the Flyback to other traditional topologies in (approximate) order of typical rated output power.

Table 2.1: Comparison of common isolated DC-DC converter topologies.

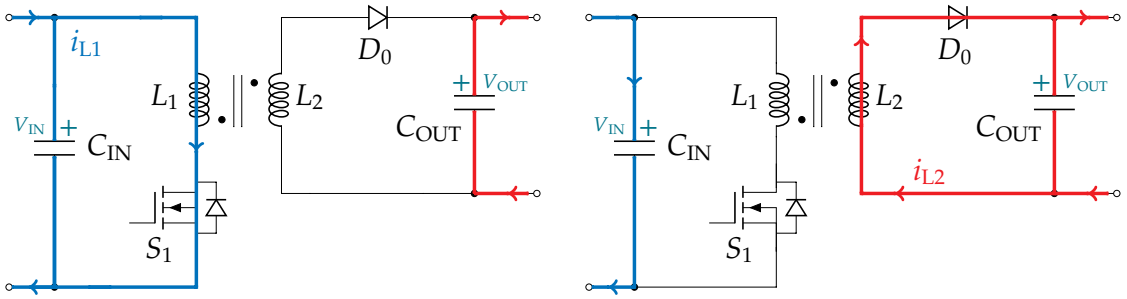
Converter	Advantages	Disadvantages
Flyback	Very low parts count. Wide operating range. Output short-circuit protection.	Poor transformer utilization. Inefficient for $>100\,\mathrm{W}$. Transistor voltage $\propto N$.
Forward	Low parts count. Low output ripple. Output short-circuit protection.	Poor transformer utilization. Critical transformer design. Transistor voltage $\propto N$.
Push-Pull	Fair transformer utilization. Applications up to 500 W. Output short-circuit protection.	High parts count. Critical switching instances. Transistor voltage is $2{\cdot}V_{\mathrm{IN}}$.
Resonant LLC	Very low switching loss. Output short-circuit protection.	Complexity. Cont. tank energization.
Isolated Half Bridge	Good transformer utilization. Transistor voltage is $1{\cdot}V_{\mathrm{IN}}$. Output short-circuit protection.	High parts count. Critical switching instances. Higher transistor current.

Although each topology offers inherent galvanic isolation, the Flyback's low parts count makes it a popular choice for low-power consumer adapters and power supplies despite the comparatively poor efficiency. State-of-the-art Flyback efficiency for small laptop adapters is discussed in Section 3.4.

2.1.2 Fundamentals of Operation

Fig. 2.2 shows the two main states for a basic Flyback converter, sometimes referred to as *energy storage* and *energy transfer* states. Respectively, they occur when S_1 is ON and when S_1 subsequently turns OFF [8]. For each state, coloured arrows are given in Fig. 2.2 to indicate the current flow through each inductor, labelled as i_{L1} and i_{L2}, as well as the current flow into and out of the filter capacitors.

By repeatedly turning S_1 ON and OFF, the Flyback alternates between *energy storage* and *energy transfer* states in order to send power from input to output. For the following introduction, circuit components are assumed to be ideal.



(a) S_1 ON - *energy storage.* (b) S_1 OFF - *energy transfer.*

Figure 2.2: Sketch of Flyback current flow during S_1 ON and OFF periods.

While S_1 is ON, a linear rise in the inductor core flux (ϕ) proportional to the input voltage (V_{IN}) and inversely proportional to the number of primary turns (N_1) occurs. The initial core flux (ϕ_0) may or may not be zero depending on whether the converter is operating in continuous conduction mode (i_{L2} does not fall to zero during *energy transfer*) or discontinuous conduction mode (i_{L2} does fall to zero during *energy transfer*). The peak flux ($\hat{\phi}$) occurs at the end of S_1 ON period – at $t = t_{ON}$.

$$\hat{\phi} = \phi_0 + \frac{V_{IN}}{N_1} t_{ON} \tag{2.1}$$

After t_{ON}, S_1 turns OFF and the energy stored in the core causes current to flow through the secondary winding and D_0. Now the flux decreases linearly and proportionally to the output voltage (V_{OUT}) and number of secondary turns (N_2) until the end of the total switching period T_S (unless it first reaches zero) [2].

For continuous conduction mode this can be expressed as:

$$\phi(t) = \hat{\phi} - \frac{V_{OUT}}{N_2}(t - t_{ON}) \qquad t_{ON} < t < T_S \tag{2.2}$$

$$\phi(T_S) = \hat{\phi} - \frac{V_{OUT}}{N_2}(T_S - t_{ON}) \tag{2.3}$$

Combining (2.1) with (2.3) gives:

$$\phi(T_S) = \phi(0) + \frac{V_{IN}}{N_1} t_{ON} - \frac{V_{OUT}}{N_2}(T_S - t_{ON}) \tag{2.4}$$

$$\phi(T_S) = \phi(0) \tag{2.5}$$

For steady state operation (constant load, output voltage and switching frequency) the net change in core flux over one period must be zero. By using (2.5) to remove the first two terms of (2.4), rearranging and incorporating the duty cycle $D = t_{ON}/T_S$, it is possible to derive the basic relation between V_{IN} and V_{OUT} for the Flyback converter:

$$V_{OUT} = \frac{N_2}{N_1} \frac{D}{1 - D} V_{IN} \tag{2.6}$$

While (2.6) is only valid for continuous conduction mode, it shows that the output voltage is affected by both the turns-ratio and switch timings. The research in this thesis deals mainly with discontinuous current mode and the appropriate equations are given in Sections 4-6. By considering the inductor currents i_{L1} and i_{L2} rather than the core flux ϕ, it is possible to model the Flyback using the inductance values L_1 and L_2 instead of the number of winding turns. E.g.,

$$\widehat{i_{L1}} = i_{L1}(0) + \frac{V_{IN}}{L_1} t_{ON} \tag{2.7}$$

Although core flux can provide an intuitive understanding of the coupled inductor, the primary and secondary inductor current is often a more useful way of discussing Flyback behaviour than core flux as it can be more easily measured and used to discuss device loss and overall power transfer. As such, inductor current is used exclusively in the main chapters of this thesis.

Since both windings are around the same core, the turns-ratio of the coupled inductor can be used to determine $\widehat{i}_{L2}$ from $\widehat{i}_{L1}$ resulting from the shared core flux:

$$\widehat{i}_{L2} = \frac{N_1}{N_2}\widehat{i}_{L1} = N\,\widehat{i}_{L1} \tag{2.8}$$

Generally, the turns-ratio (N) can be expressed in terms of inductances L_1 and L_2:

$$N = \frac{N_1}{N_2} = \sqrt{\frac{L_1}{L_2}} \tag{2.9}$$

Similarly, once S_1 turns OFF and current flows through D_0, the transformer effect causes the voltage seen by the secondary winding to be imposed on the primary winding through the turns-ratio. I.e. during *energy transfer*:

$$V_{L2} = V_{OUT} \tag{2.10}$$

$$V_{L1} = \frac{N_1}{N_2}\,V_{L2} = \frac{N_1}{N_2}\,V_{OUT} \tag{2.11}$$

It follows that during this OFF period, S_1 blocks both the input voltage and output voltage reflected through the coupled inductor. Thus, the subsequent drain-source voltage of S_1 ($V_{DS(S1)}$) is:

$$V_{DS(S1)} = V_{IN} + \frac{N_1}{N_2}\,V_{OUT} \tag{2.12}$$

Likewise, the reflected input voltage (plus the output voltage) is blocked by D_0 during the *energy storage* state. Understanding this reflective behaviour is vital when choosing a device for S_1 or designing the coupled inductor. This property is increasingly exploited by modern Flyback controllers for estimating voltages across the isolation barrier [9].

With ideal components, the blocking voltage predicted by (2.12) represents the highest voltage S_1 must block. However, with non-ideal components, peak $V_{DS(S1)}$ will be higher due to turn-OFF voltage overshoot caused by leakage inductance and parasitic capacitances and will occur immediately after S_1 turn-OFF. A common approach to mitigating this large overshoot in order to avoid S_1 breakdown is introduced in Section 2.1.5.

2.1.3 Applications

Due to its simplicity, the Flyback topology is often employed for low power, bus-to-bus DC regulation in low voltage server or telecommunication systems. It is a popular choice for multiple output converters due to the possibility of easily adding extra output windings to the same core [1, 6]; with different turns-ratios these windings can simultaneously provide multiple output voltages from a single input voltage bus without a complex control/regulation loop.

In addition, due to its low parts-count and inherent galvanic isolation, a large and growing market for Flyback converters is in single-phase AC-DC power adapters for consumer electronics [10]. Fig. 2.3 shows the basic Flyback converter with a diode rectification bridge between the AC grid voltage and input capacitor – now referred to as the DC-link capacitor ($C_{\text{DC-link}}$).

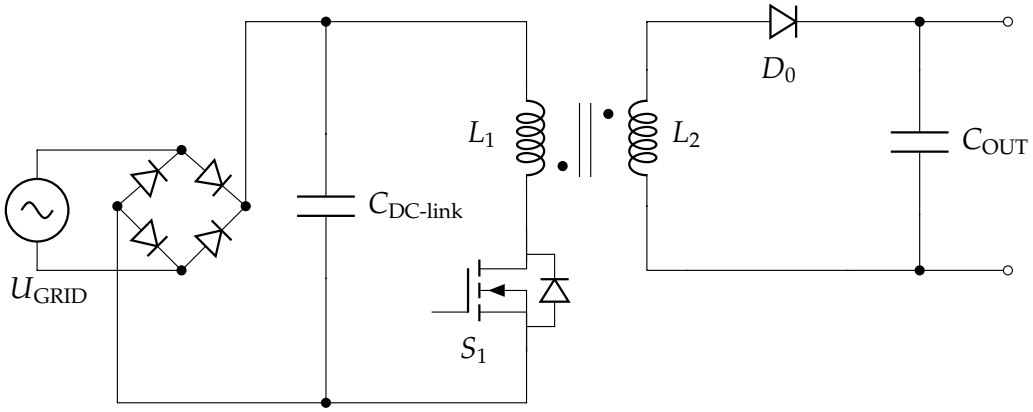


Figure 2.3: Principle schematic of the grid-connected Flyback converter.

This input diode bridge rectifies the sinusoidal input to a positive DC voltage; albeit with double grid-frequency ripple [6]. In low power applications with large input capacitance, or with sufficient duty-cycle control, any voltage ripple on the DC-link becomes either inconsequential or manageable and the Flyback can continue to operate as a DC-DC converter.

This thesis will focus on the single phase grid connected Flyback topology shown in Fig. 2.3 for use in a universal-input, medium-power adapter application. The advantages listed in Tab. 2.1 alongside the proposed control approach studied in this thesis make this a suitable context.

2.1.4 Active Synchronous Rectification

In low output voltage applications, the voltage drop of the diode rectifier D_0 in Fig. 2.3 can be the dominant loss contribution [11, 12]. In higher power converters, core and winding loss generally become more significant, although with high output current diode rectifier loss is still very large. To address this, D_0 can be replaced with a second active MOSFET (S_2) as shown in Fig. 2.4. Placing S_2 on the ground rail allows low-side gate drivers to be used.

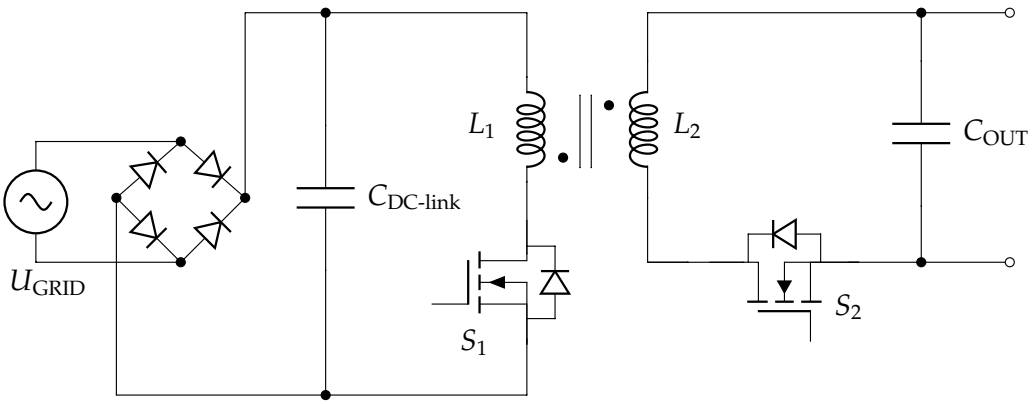


Figure 2.4: Schematic of grid-connected Flyback converter with active synchronous rectification switch S_2.

The switching behaviour of D_0 can be replicated by turning S_2 ON at the beginning of the *energy transfer* state, and then OFF at the end. By doing so, the overall behaviour of the Flyback remains unchanged, but the losses associated with the D_0's voltage drop have been replaced with smaller conduction losses associated with S_2's ON resistance [12].

In general, the drawback of active synchronous rectification is the addition of an extra control signal. The gate signal for S_2 needs to be correctly timed in respect to S_1's gate signal. For continuous conduction mode, a pair of inverted gate signals can be sufficient, but simultaneous turn-ON of S_1 and S_2 should be avoided as this would lead to an effective short circuit on both sides. For discontinuous conduction mode, accurate sensing or prediction of i_{L2} is required in order to turn OFF S_2 once i_{L2} has fallen to 0 A.

The concept investigated in this thesis builds upon this concept of active synchronous rectification for Flyback converters using discontinuous current mode.

2.1.5 Important Flyback Design Considerations

For clarity, some additional design considerations that appear frequently in Sections 4-6 are introduced here within the context of the preceding introductory Flyback discussion.

Switching Frequency

Herein, switching frequency is defined as $1/T_S$ where T_S is the time between S_1 turn-ON instances. The switching frequency of S_1 (and S_2) guides the design of the Flyback, or conversely, the hardware employed limits the converter to a range of realistic switching frequencies. Tab. 2.2 gives some examples of how switching frequency relates to Flyback components [2].

Table 2.2: Examples of components affected by switching frequency.

Component	Related Parameters
Coupled Inductor	Core & winding loss
MOSFETs	Switching & gate loss
Input Filter	Input current harmonics
Output Capacitor	Output voltage ripple

Likewise, other parameters such as peak currents and rated power are also affected by the switching frequency which further affects the overall hardware design.

Coupled Inductor

The coupled inductor is the most critical component in Flyback converter design. The inductances resulting from the number of turns, core material, core shape, and air gap determine the possible switching frequencies for a given power transfer. The turns-ratio determines the viable voltage rating of the synchronous rectification device due to the reflected DC-link voltage, and the leakage inductance should be kept low enough to avoid large voltage overshoots across S_1 at turn-OFF [5, 6, 8]. Furthermore, it should be designed to support rated power without incurring core saturation or excessive winding loss [2]. It also contributes to a significant amount of volume of the final converter, impacting the eventual power density [13].

Snubber

A snubber provides an alternative path for the inductively maintained primary current caused by energy stored in the coupled inductor's leakage inductance after S_1 turn-OFF [8]. Otherwise, depending on the leakage inductance and turn-OFF current, the leakage energy may cause a voltage overshoot across S_1 exceeding its breakdown voltage; potentially destroying S_1. A common snubber network due to its simplicity and "tune-ability" is the resistor-capacitor-diode (RCD) network shown in Fig. 2.5 [5].

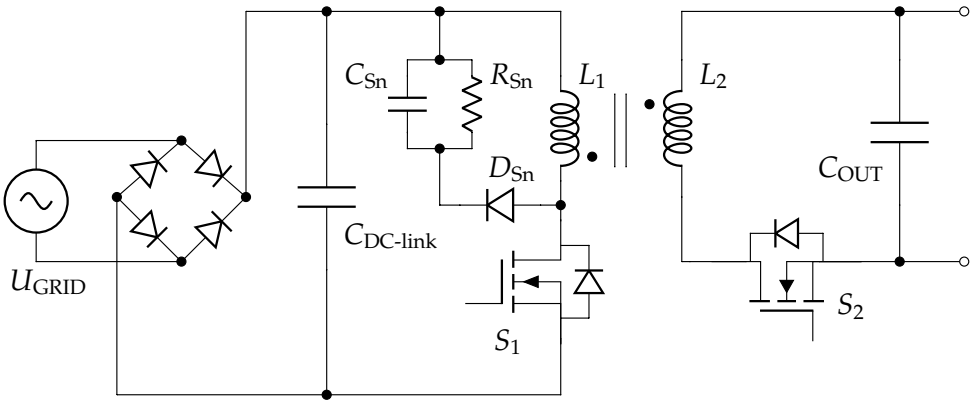


Figure 2.5: Principle schematic of a Flyback converter with S_1 RCD snubber.

This RCD snubber uses C_{Sn} and R_{Sn} to "capture" and dissipate leakage energy once S_1's drain-source voltage exceeds the DC-link voltage. Zener clamp solutions can be superior for low leakage energy and several non-dissipative snubbers also exist, but are often more complex [5, 14, 15].

Input EMI-Filter

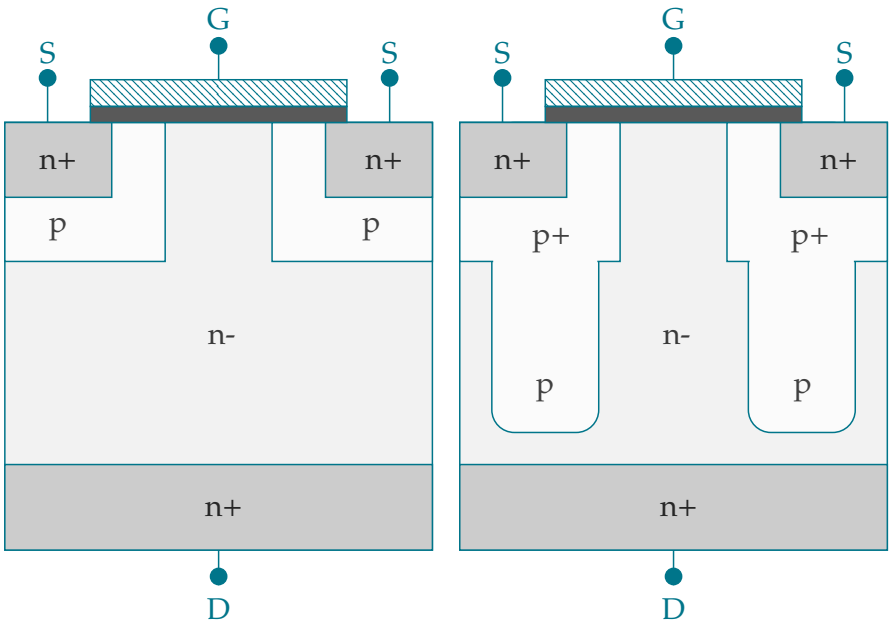
Generally, real-world switched-mode power supplies require an input filter to prevent electromagnetic interference (EMI) caused by high-frequency switching from feeding noise back to the grid [16]. This is often achieved by placing an array of L-C filters between the grid input and the rectifying diode bridge. The allowable differential- and common-mode noise depends on the exact market location and corresponding legal standards, but maximum high-frequency emmisision is typically $\approx$ 40-60 dBμV [8, 17]. Generally, the EMI-filter will not have any impact on Flyback operation, but Flyback operation will affect the requirements of the EMI-filter which will in turn affect the physical power density of the resulting power adapter.

2.2 Devices / MOSFETs

For most modern adapter Flybacks, power MOSFET's are used for S_1 (and S_2) due to their current capability and fast switching speed. Highly efficient and power-dense adapters employ superior Gallium Nitride (GaN) devices [18], although cost-benefit limitations have so-far prevented GaN based adapters from becoming ubiquitous in consumer applications [19]. The experimental verification work in this thesis was done using silicon power MOSFETs and this section gives a qualitative overview of their main characteristics.

2.2.1 Structure

Several variants of the MOSFET structure exist, but the most common type in power electronics is the N-channel type since it is "normally OFF" and the higher carrier mobility of the *n*-type results in lower ON-resistance ($R_{DS(ON)}$) [20]. Fig. 2.6 shows a sketch of two N-channel power MOSFET structures. Highly doped *n*+ regions form the source (*S*) and drain (*D*) while an isolation layer separates the gate contact (*G*) from the underlying *p* and *n* sections.



(a) Standard Power MOSFET (b) Super-junction MOSFET

Figure 2.6: Simplified sketch of vertical N-channel power MOSFETs.

This structure leads to an *npn* configuration with a reverse blocking internal body diode from source to drain. When sufficient voltage is applied between gate and source, a conductive *n*-channel forms between *n*+ regions – turning the MOSFET ON and allowing drain to source current flow.

To maximize the *n* regions and reduce $R_{DS(ON)}$, most modern high-voltage MOSFETs utilize the charge compensation principle to some degree; balancing the doping of the *n* region with enlarged *p* wells to maintain sufficient breakdown voltage. This has allowed devices to surpass the theoretical limit of on-resistance for a given breakdown voltage; the silicon limit [2, 20, 21]. For very high blocking voltages (> 600 V), super-junction MOSFETs use a comparatively thin *n*- region, with the *p* sections extended further into deep columns. While the super-junction design can block higher voltages and has low $R_{DS(ON)}$, the deep *p*-columns lead to poorer switching behaviour and a large, highly non-linear parasitic output capacitance.

2.2.2 Behaviour and Characteristics

Fig. 2.7 shows a model of the MOSFET with the parasitic capacitances that arise from the structure shown in Fig. 2.6. The MOSFET is a unipolar voltage controlled device that approximates a closed switch when its gate-source voltage (V_{GS}) is higher than its threshold value $V_{GS(th)}$. This requires C_{GS} and C_{GD} to be charged and discharged for every turn-ON instant.

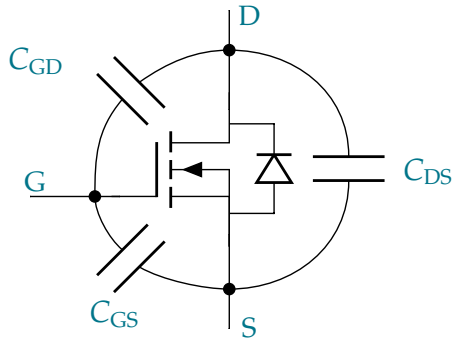
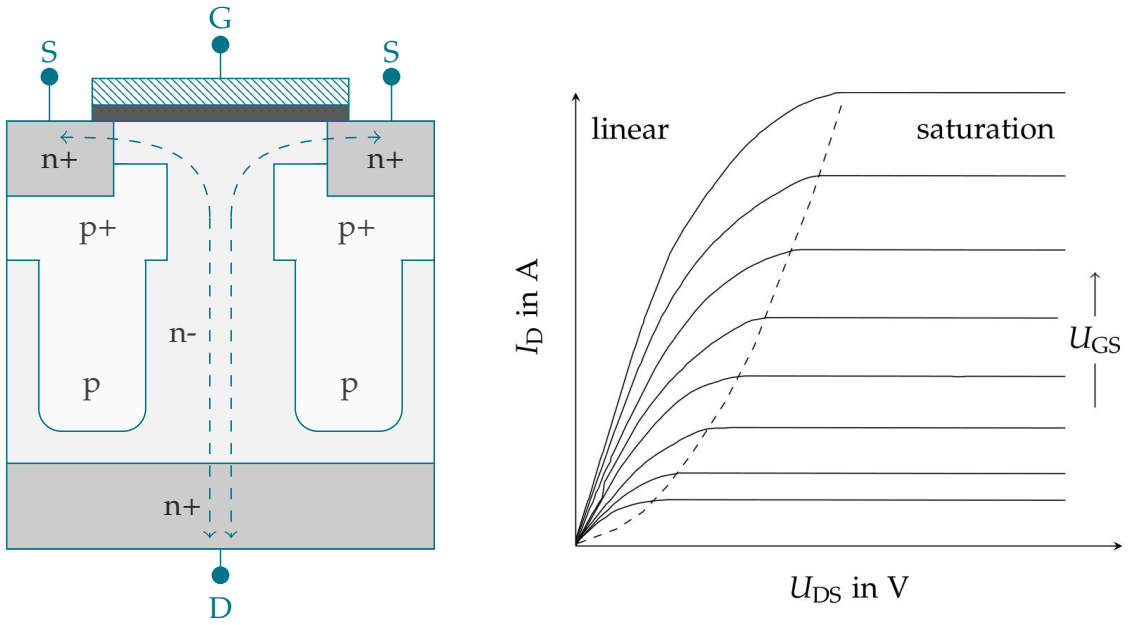


Figure 2.7: MOSFET circuit model.

The V_{GS} supplied by the device driver is typically chosen to balance the loss associated with charging the gate against the lower $R_{DS(ON)}$ and higher saturation current possible with higher V_{GS}. Fig. 2.8b shows an ideal sketch of drain-current in relation to V_{GS} and V_{DS}.

For super-junction MOSFETs, optimum gate voltage is usually between 8-20 V. Once the device is ON, current can flow from drain to source through a resistance set by the chip dimensions and the *n*-channel resulting from the applied V_{GS}. Fig. 2.8a shows a modified sketch of the super-junction structure during the conducting/ON-state with an exagerated *n*-channel formed by the gate-source voltage [22].



(a) Simplified sketch of ON state.

(b) Ideal MOSFET output characteristic, taken from [23].

Figure 2.8: Super-junction MOSFET structure during ON state (a) and ideal MOSFET output characteristic (b).

Fig. 2.7 indicates that by turning ON the device, any excess charge stored in C_{GD} and C_{DS} (together known as the lumped C_{OSS}) will discharge. This contributes to the turn-ON switching loss. C_{OSS} also impacts the turn-OFF behaviour of the device. For super-junction MOSFETs, C_{OSS} is large and highly non-linear with drain-source voltage which can introduce significant turn-OFF voltage ringing at high currents. Fig. 2.9 shows an example of super-junction device's parasitic capacitance versus drain-source voltage [24].

Despite their large and non-linear C_{OSS}, super-junction MOSFETs are generally the preferred device for the main switch in Flyback based adapters due to their high blocking voltage (especially useful for high-line grid input voltage), and their comparatively low ON-state resistance compared to other device types. In Flyback based adapters, 600 V rated super-junction MOSFETs are very common.

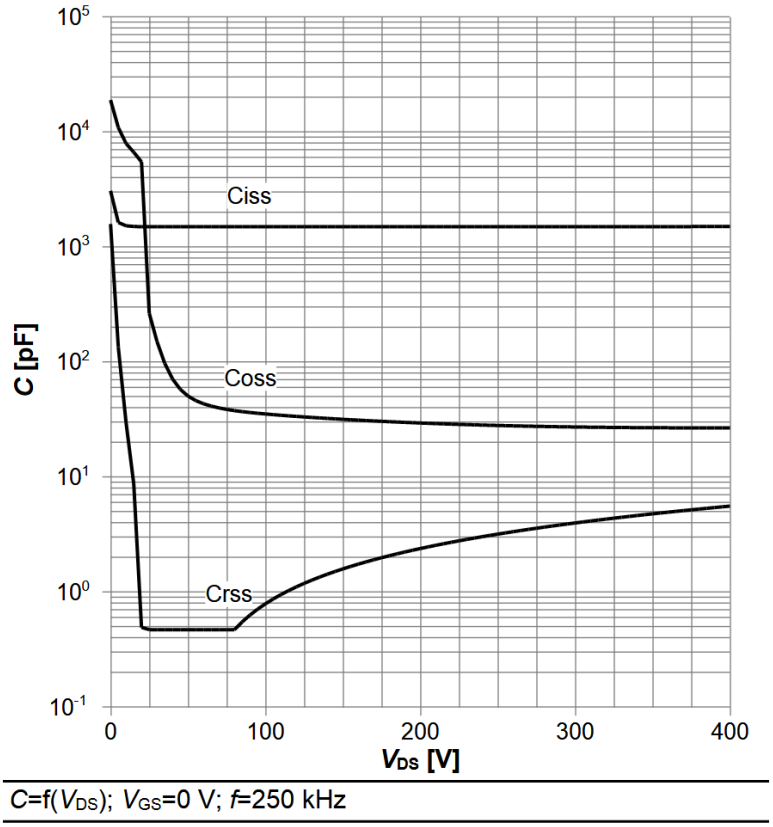


Figure 2.9: Parasitic capacitances of a 600 V CoolMOS C7 (IPL60R125C7) [24].

2.2.3 Soft Switching

The charge stored in C_{OSS} at turn-ON is a large contributor to turn-ON loss. By turning ON the MOSFET when the drain-source voltage is already low, such loss can be reduced. This is generally referred to as "soft-switching".

For a Flyback's synchronous rectification switch (S_2), soft-switching can be achieved with a small dead-time; allowing the load current to conduct through the body-diode for a short time before applying V_{GS} so that the drain-source voltage falls to the forward body diode voltage. This causes S_2 turn-ON switching loss to become negligible. For the primary side MOSFET, it is common to make use of the resonance between the coupled inductor and parasitic MOSFET capacitances; they cause the drain-source voltages to oscillate at the end of the synchronous rectification in discontinuous current mode. It is possible to turn-ON the primary switch at the valley of such oscillation to reduce primary turn-ON switching loss [20]. This is explained with more detail in Chapter 3 in context with a state-of-the-art control approach.

Chapter 3

Classic and State-of-the-Art Control Concepts

This chapter covers a selection of existing Flyback control concepts representing the state-of-the-art currently on the market, and highlighting the pros and cons of each approach with respect to one another. The chosen concepts are:

- "Classic" Control.
  - The conventional control approach alluded to in Chapter 2.
- Primary Side Regulation.
  - A control approach that does not require isolated signal coupling for output voltage feedback measurement.
- Single IC Cross-Barrier Solutions.
  - Complete solution whereby both controller and active switch are included in one IC package with direct V_{OUT} access.

This chapter finishes with a discussion of the achievable efficiency of 65 W Flyback converters using these three control concepts and silicon-based power MOSFETs.

3.1 Classic Flyback Control

Fig. 3.1 shows a block diagram of the classical control structure superimposed onto the Flyback schematic. In its simplest form, the Flyback converter is controlled from the primary side operating as outlined in Section 2.1.2: hard-switching with a diode in place of S_2 (see Fig. 2.1). Any V_{OUT} feedback must be relayed via high-voltage signal coupling (often executed with opto-isolators or magnetic coupling) to maintain galvanic isolation between input and output sides.

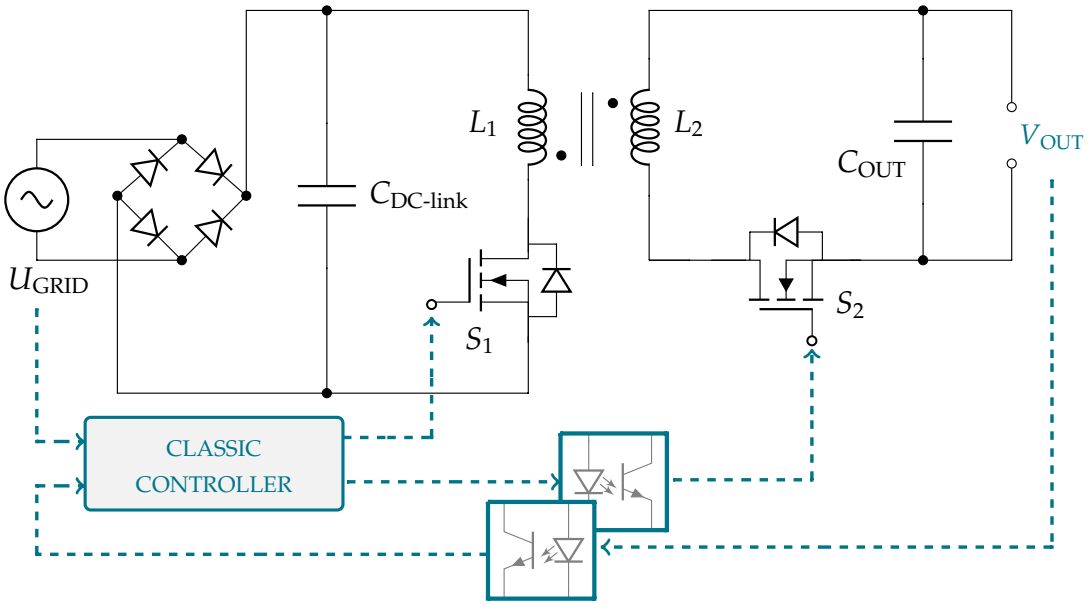


Figure 3.1: Flyback converter with block diagram of conventional control structure.

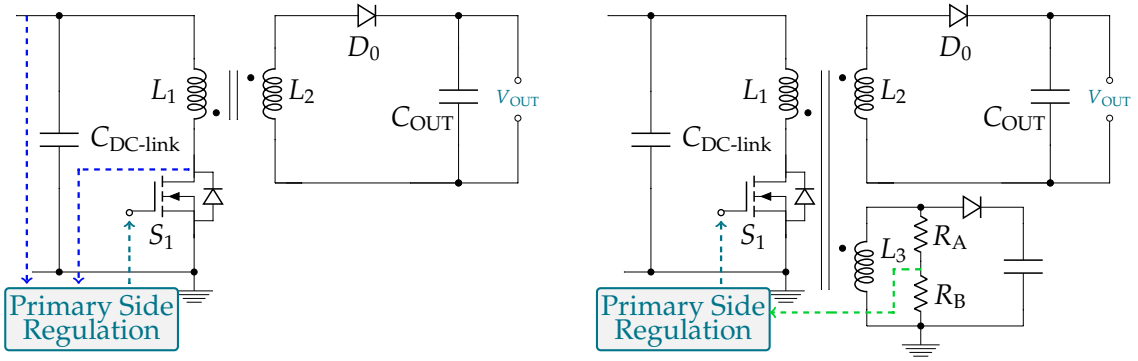
The controller can then compare the actual output voltage to a reference value and modify the switching pattern of S_1 accordingly. Several control loop types have been proven to work with the Flyback converter.Some well-known types include continuously modulated structures such as a PI controller as well as non-continuous loops such as the "bang-bang" hysteresis controller. The advantage of such an approach is ruggedness and simplicity.

When including an active synchronous rectification switch with this set-up, it requires both synchronous rectification gate signal and output voltage sensing to be transmitted via signal coupling to maintain isolation across the coupled inductor [25–30]. Such signal coupling can often be one of the most expensive and safety-critical electronic components in the adapter.

3.2 Primary Side Regulation

As shown in Section 2.1.2 and in (2.11), a Flyback's coupled inductor causes the output voltage to be reflected across the primary winding during the *energy transfer* state (shown in Fig. 2.2). This occurs when S_1 turns OFF and the coupled inductor is de-energizing into the output capacitor. By determining the primary side inductor voltage, this phenomena can be exploited to sense the output voltage from a primary side controller without any need for isolated signal coupling. For accuracy, a measurement should be made at the start of *energy-transfer* as the reflected V_{OUT} decays during the off-time. This was first effectively demonstrated in [31] and named as *primary side regulation / primary side sensing*.

Two main variations of the concept exist whereby V_{OUT} is inferred either by subtracting the DC-link voltage from the drain-source voltage of S_1, or by adding an auxiliary winding to the main inductor core [32]. Although the second approach requires an extra winding, the winding can scale the inductor voltage to avoid any high-voltage sensing components and is less vulnerable to high-frequency switching noise [33]. Fig. 3.2 shows a sketch of both variations with additional dotted lines indicating the voltage measurements for each approach. The auxiliary circuit is taken from [9].



(a) S_1 drain-source voltage method.

(b) Auxiliary winding method.

Figure 3.2: Diagram of two primary side regulation variations.

Figs. 3.3 and 3.4 show waveforms for the auxiliary winding type shown in Fig. 3.2b for both CCM and DCM modes of operation, where V_{RB} is the scaled inductor voltage measured across R_{B}. The auxiliary circuit shares a ground connection with the primary based controller, allowing a straight-forward voltage measurement.

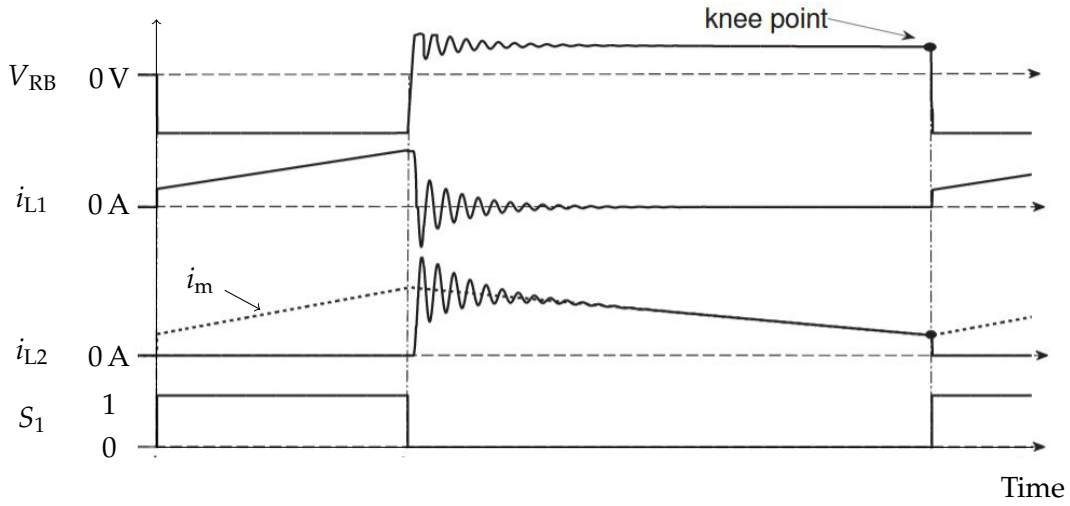


Figure 3.3: Knee-point and typical Flyback waveforms for CCM mode [9].

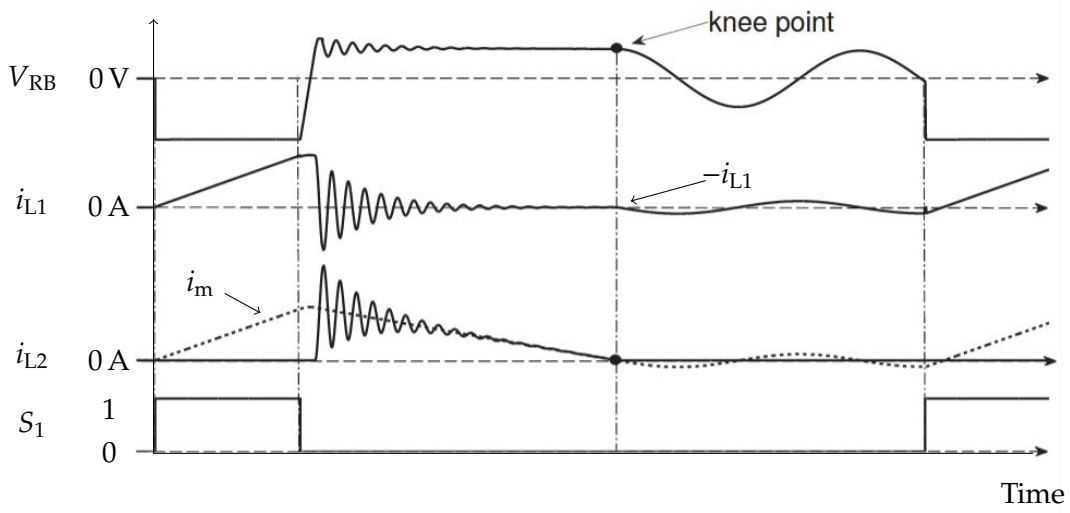


Figure 3.4: Knee-point and typical Flyback waveforms for DCM mode [9].

Figs. 3.3 and 3.4 shows that any ringing from S_1 turn-OFF is also reflected to the auxiliary winding. For this reason (and to minimize affect of non-ideal secondary side voltage drops from high current), the knee point of the inductor voltage is generally used to infer the output voltage. The same applies when adopting the drain-source voltage approach. The nature of the knee-point is different for CCM and DCM operation. For CCM the knee-point gradient is easier to sense due to the near-instantaneous reversal of inductor voltage direction.

In contrast, for DCM V_{RB} rings with a low frequency related to the main inductances, and thus undergoes a slow change once i_{L2} crosses 0 A. For fast knee-point detection, DCM operation thus requires some form of zero-current-crossing sensing for i_{L2}. However, this would require some isolated coupling to transmit the zero crossing signal, thus nullifying a main advantage of the primary side regulation. To overcome this issue, several "work-arounds" exist.

One such example can be summarized as approximating the knee-point instant by waiting for the first i_{L1} zero crossing (sensed with a shunt resistor) after a given blanking time post S_1 turn-OFF (shown in Fig. 3.4). V_{RB} is then immediately sampled. The sampled voltage can then be converted to output voltage with:

$$V_{OUT} = \frac{N_2}{N_3} \frac{R_A + R_B}{R_B} k\, V_{RB} - R_B \frac{N_1}{N_2} i_{L1} - V_D \tag{3.1}$$

Where V_D is the forward voltage of D and N_1, N_2 and N_3 are the number of turns for L_1, L_2 and L_3 respectively. To account for voltage drop due to leakage inductance the term k is included where $k = 1 + \frac{L_1}{L_2} \frac{L_2 + L_2^\sigma}{L_m}$. L_m is the primary magnetizing inductance and L_2^σ is the secondary leakage inductance. For the drain-source voltage approach without the extra winding, V_{OUT} can be approximated with:

$$V_{OUT} = \frac{N_2}{N_1} (V_{DS(S1)} - V_{DC\text{-}link}) - V_D \tag{3.2}$$

For a fast controller, the term i_{L1} is negligibly small at the zero crossing (as annotated in Fig. 3.4). With sufficient sampling speed, such an approach can yield an accurate estimate of V_{OUT}, but requires accurate knowledge of the circuit parameters and relatively complex logic.

Overall, the primary side regulation approach is an effective "opto-isolator-less" solution, especially for CCM. For DCM more effort is needed in voltage/current sensing. Primary switching loss can be reduced by including valley switching in the control logic by tracking $V_{DS(S1)}$. For DCM applications an independent synchronous rectification driver such as the LT8309 can be used to reduce secondary side diode losses, however this is not compatible for CCM operation (the best operation for primary side regulation [34]). Furthermore, the controller can never sense the output voltage in idle mode as an *energy transfer* state is required in order to infer V_{OUT} reflected across the primary switch.

3.3 Single IC Cross-Barrier Solutions

In an effort to simplify Flyback design, single IC controllers are available that house both the controller and the primary switch S_1 in a single package. Together with an intelligent PCB layout, this can help improve power density and reduce noise on signal tracks between controller, driver and switch. *Power Integrations, Inc.* extended this idea with the InnoSwitch^{TM} device family by also including the synchronous rectification sensing/driver in the package with internal high voltage isolation between primary and secondary switch circuitry [35].

Fig. 3.5 shows a schematic of the InnoSwitch3-CP with a Flyback converter. By reversing the classic Flyback control structure (Section 3.1), V_{OUT} regulation is situated on the secondary side, and the primary switch is controlled via isolated magnetic coupling within the IC package.

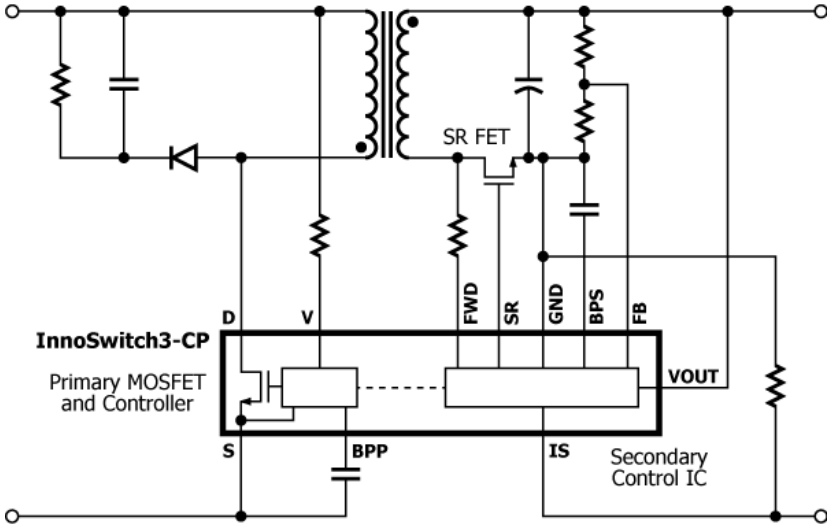


Figure 3.5: Schematic of the InnoSwitch3-CP controller [35].

Advantageously, direct V_{OUT} access is now possible with the secondary side circuitry. This results in simpler, more reliable V_{OUT} measurements without the need of a third winding or high-voltage sensing components. Furthermore, active synchronous rectification can be used for both DCM and CCM as the controller is unified on the secondary side. Valley switching is also possible by using the drain-source voltage across S_2 to infer $V_{DS(S1)}$. However, isolated signal coupling has been re-introduced, only now from the secondary controller to the primary side switch.

3.4 Flyback Efficiency

A key performance criteria of a power adapter is the overall power conversion efficiency, both for high- and low-line input voltage. Not only does the presence of synchronous rectification affect losses, but so does the switching pattern and inductor currents that emerge from the control scheme. Fig. 3.6 shows the measured efficiency of three bespoke 65 W adapter Flyback demonstrators, each of which uses one of the control schemes discussed thus far: a demonstrator using "classic" control taken from [36], a primary side regulation demonstrator taken from [37], and a InnoSwitch3 single IC controller demonstrator taken from [38].

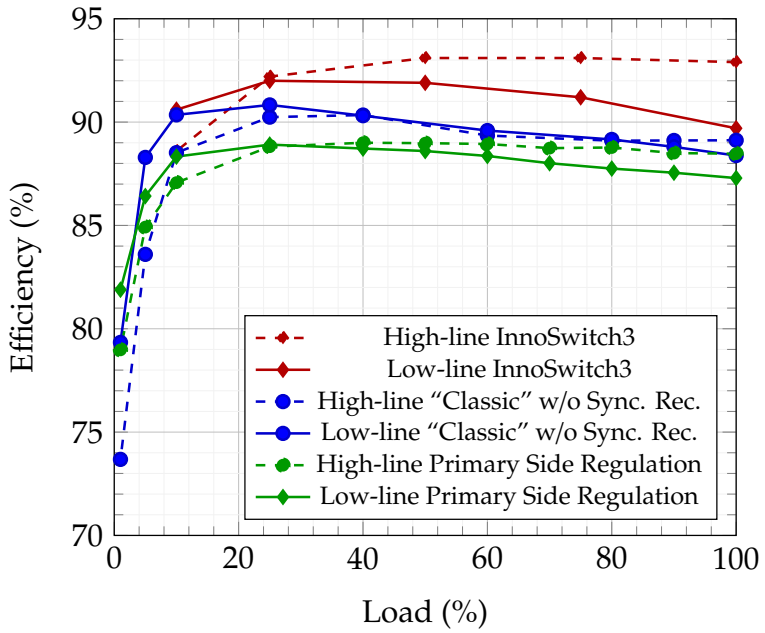


Figure 3.6: Efficiency comparison of various 65 W Flyback demonstrators examples.

Although the rated power of these demonstrators was the same, their physical design varied and the achievable efficiency of a Flyback depends greatly on the converter hardware specifications: e.g., power density, winding type and complexity, available core material, snubber dimensions and breakdown voltage of S_1. As such this plot should be treated as a reference for the *range* of efficiencies expected of bespoke 65 W Flyback adapters. All control schemes are capable of delivering $\approx 90\,\%$ efficiency at medium to high load and, interestingly, the only demonstrator employing active synchronous rectification achieved the highest efficiency.

Chapter 4

Secondary Side Controlled Flyback Concept

4.1 Chapter Outline

This chapter introduces and explains the Secondary Side Controlled Flyback concept proposed by *Infineon Technologies Austria AG*, and contrasts it with the state-of-the-art concepts introduced in Chapter 3. This top-level idea was the basis and starting point for all research contributing to this thesis.

4.2 Concept Overview

Conventionally, the Flyback converter is controlled from the primary side in either hard-switching mode (with a diode in place of S_2), or in quasi- or full-resonant mode with an active synchronous rectification switch.

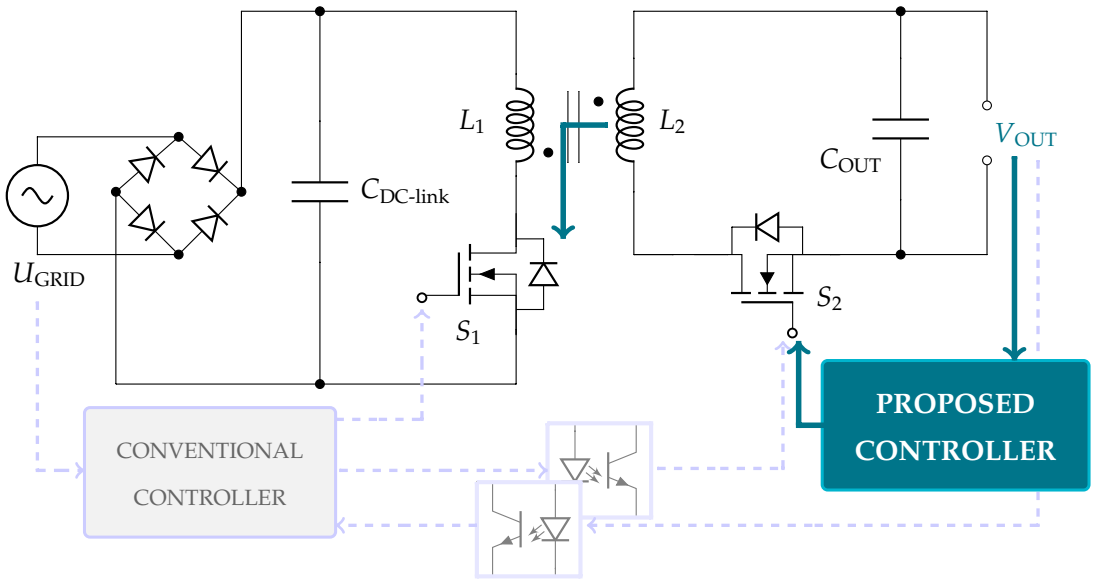


Figure 4.1: Comparison of conventional and proposed Flyback controllers.

In this case, both synchronous rectification gate signal and output voltage sensing must be transmitted via opto-isolators or magnetic coupling to maintain galvanic isolation across the coupled inductor. However, such isolated coupling can be relatively costly and cause operational issues at high frequency. Standard high-voltage opto-isolators can add a propagation delay up to 100 ns to secondary gate signals and output voltage measurement [39–41] (limiting achievable switching frequency and precision in soft-switching applications) and magnetic couplers can be vulnerable to electromagnetic noise radiated by the Flyback's coupled inductor [42, 43]. This concept proposes removing all such isolators and instead placing the controller on the secondary side of the coupled inductor.

However, unlike a synchronous rectification driver (such as the LT8309 [34]) it has the additional function of output voltage regulation by providing turn-ON commands to the primary switch (S_1) via the coupled inductor using pulses of negative current to discharge S_1's parasitic output capacitance.

4.3 Comparison to State-of-the-Art

Firstly, moving the main controller to the secondary side enables direct access to the output voltage as shown in Fig. 4.1. Direct access is advantageous in variable output voltage applications such as USB-Power-Delivery (USB-PD) / USB-Type-C [44–46] where different output voltages are required depending on the load attached. An existing USB-PD Flyback adapter from *Texas Instruments, Inc.* shown in [47] uses a hard-switching primary-based controller with opto-isolators for the output voltage feedback loop. Secondly, by eliminating the need for opto-isolators the parts-count is reduced and the corresponding propagation delay between primary and secondary side is removed. The most common opto-isolator free solution is the primary-side regulation concept whereby a primary side based controller infers the reflected output voltage using the drain-source voltage across S_1. However, this solution lacks the direct access to the output voltage offered by a secondary side controller.

An existing secondary side based controller from *Power Integrations, Inc.* is a dedicated IC controller that neatly incorporates the primary MOSFET and utilises an internal magnetic feedback link for primary-secondary communication [35]. However, this solution constrains a designer to the internal primary MOSFET – limiting the application of the IC to a specific frequency/power range. Furthermore, the product does not allow full zero voltage turn-ON of the primary switch.

In contrast, by signalling turn-ON commands to S_1 via the coupled inductor, any internal chip communication can be removed. This maintains freedom of choice for the primary device and simultaneously enables soft primary turn-ON, while still eliminating opto-isolators. Though a potential gain in efficiency might be lost due to the negative current requests, the transformer design can be relaxed as no third winding is needed, and soft switching may support volume and loss reduction within the EMI-filter.

Table 4.1: Feature comparison with state-of-the-art Flyback controllers.

Controller	Synchronous Rectification	No Signal Coupling	Direct V_{OUT} Access	Soft Primary Turn-ON
Proposed Concept	✓	✓	✓	✓
Innoswitch-CP	✓	–	✓	–
TI TPS25740	–	–	✓	✓
Fairchild SEZ1317	–	✓	–	✓

Tab. 4.1 compares features of the proposed concept against the aforementioned state-of-the-art Flyback controllers. The central improvement to the state-of-the-art is that the primary drain-source voltage ($V_{DS(S1)}$) provides the signal to turn ON the primary switch (S_1) rather than auxiliary digital or magnetic signals. The following section explains in more detail how this is possible with a secondary side based controller. A market-ready incarnation of the proposed concept would be a pair of IC chips containing the secondary side controller and the simple primary side drain-source sensing with discrete logic as depicted in Fig. 4.2.

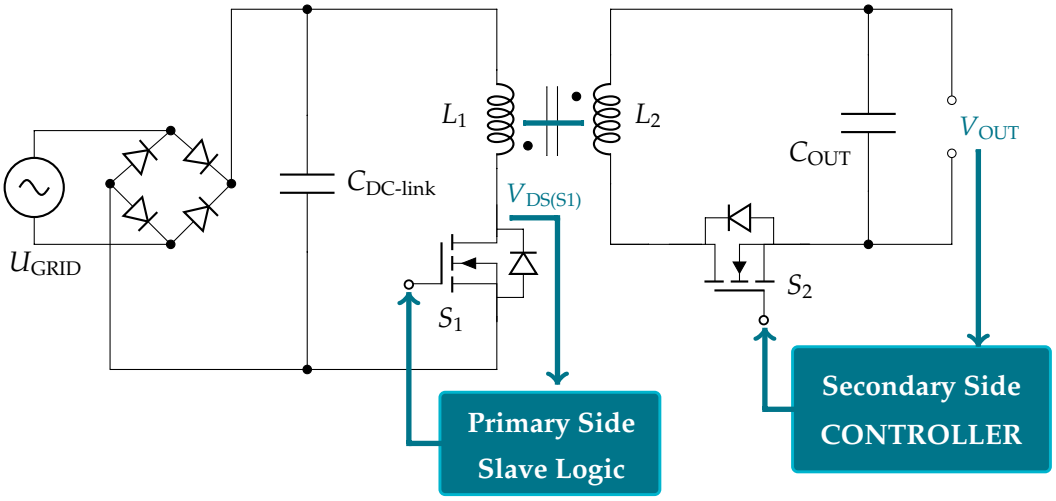


Figure 4.2: Proposed secondary side controller with independent primary side logic.

4.4 Turn-ON Requests from Secondary Side

After start-up and with the output capacitor charged, it is possible to energize the secondary inductor with "negative current" (away from the load) by turning ON S_2. Subsequently turning OFF S_2 will rapidly change the direction of secondary di/dt and the magnetic field will de-energize on the primary side; discharging the parasitic output capacitance (C_{OSS}) of S_1 [48]. The turn-ON signal for S_1 comes from a zero-voltage detection circuit connected to S_1's drain. Thus, the secondary side controller can request energy from the primary side by "sending" a small negative current pulse sufficient to discharge the parasitic output capacitance of S_1 and cause a zero voltage crossing. When turning ON S_1 at this instant, soft-switching is achieved with a zero-voltage-switching (ZVS) turn-ON.A sketch of such a ZVS turn-ON request is shown in Fig. 4.3 in context with $V_{DS(S1)}$, inductor currents and gate signals.

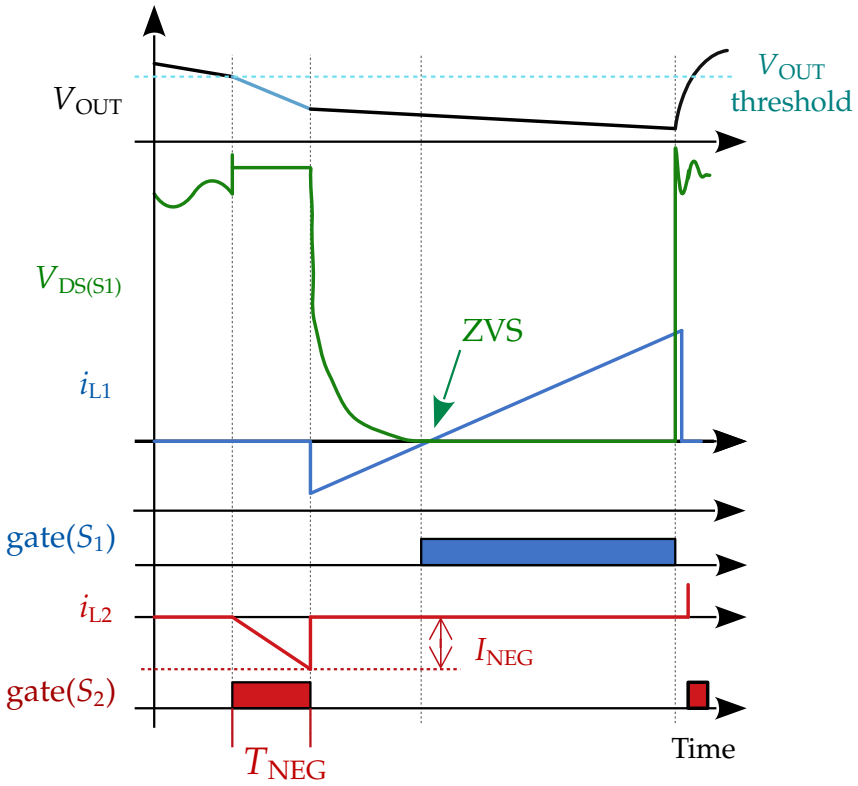


Figure 4.3: Sketched close up of proposed turn-ON request using negative current.

I_{NEG} is a constant defined as the minimum negative sedcondary side current required to induce a zero crossing of $V_{DS(S1)}$ in this way. Assuming constant C_{OSS}, a minimum estimate of I_{NEG} can be found using (4.2); although a slightly larger I_{NEG} should be used in reality to accommodate non-linear C_{OSS} and leakage inductance [49]. I_{NEG} is related to the energy stored in the main inductance of the coupled inductors and the stored charge in S_1's output capacitance ($Q_{C_{OSS}}$) [50].

$$Q_{C_{OSS}} = \int_0^{\widehat{V}_{DS}} C_{OSS}(V)\ dV \tag{4.1}$$

$$I_{NEG} = \sqrt{Q_{C_{OSS}} V_{DC\text{-}link}\, N^2/L_1} \tag{4.2}$$

where N is the coupled inductor's turns-ratio, $V_{DC\text{-}link}$ is the voltage across $C_{DC\text{-}link}$ and L_1 is the primary inductance as shown in Fig. 4.1. I_{NEG} should be dimensioned for the peak DC-link voltage T_{NEG} should be sufficient to achieve this negative current:

$$T_{NEG} = I_{NEG} L_2 \ / \ V_{OUT} \tag{4.3}$$

4.5 Steady State Operation

A sketch showing turn-ON requests and T_{NEG} in the context of steady-state operation can be seen in Fig. 4.4. Whenever the output voltage V_{OUT} falls below a reference threshold, the secondary side can request energy from the primary side by turning ON S_2 for a time T_{NEG} – "sending" a "turn-ON request" using negative current. In effect this allows the coupled inductor to transmit the turn-ON request to S_1, after which S_1 turns ON to return more energy to push V_{OUT} back above the reference threshold. By repeating this process, steady-state Flyback operation is achieved using the novel turn-ON requests transmitted from the secondary side.

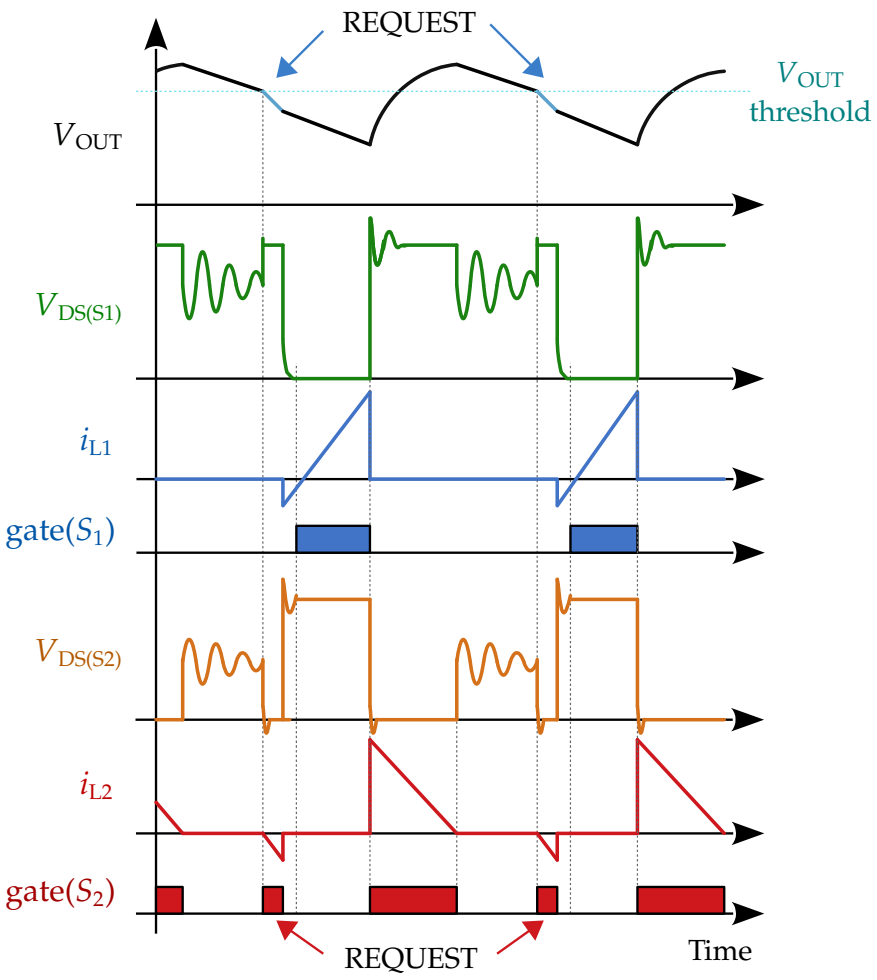


Figure 4.4: Secondary side controlled Flyback turn-ON requests with gate signals, V_{OUT}, inductor currents and drain-source voltages.

Chapter 5

Proving the Feasibility of the Secondary Side Controlled Flyback Concept

5.1 Chapter Outline

This chapter aims to demonstrate the feasibility of the Secondary Side Controlled Flyback. A 65 W demonstrator was built with two key objectives:

- Supply a stable output voltage at competitive efficiency using minimal primary side control and a working start-up routine.
- Achieve reliable control of the primary switch via the coupled-inductor with signal "propagation delay" comparable to the best market-ready opto-isolators.

Section 5.2 describes the novel sensing hardware used to achieve this cross-isolation communication, Section 5.3 describes the proposed control scheme for regulating the output voltage. Section 5.4 details parameters of the demonstrator hardware while Section 5.5 presents measurements of:

- High- and low-line steady-state operation.
- Primary side turn-ON delay.
- Autonomous zero crossing blanking.
- Start-up routine.
- Efficiency and losses.

5.2 Voltage Sensing

Reliable sensing of the zero crossing of both $V_{DS(S1)}$ and $V_{DS(S2)}$ is vital to the effectiveness and stability of the proposed Secondary Side Controlled Flyback concept. Both of these voltages were sensed using sub-circuits based on passive components and inverting high speed comparators. The primary side sensing also includes a novel network to provide autonomous passive filtering between turn-ON requests and unwanted zero voltage crossings.

5.2.1 Primary Side Switch – Double Pulse Response

Primary drain-source voltage sensing should provide the primary side logic with a turn-ON command after sensing a zero crossing of the drain source voltage. Fig. 5.1 shows the schematic of the primary side V_{DS} sensing sub-circuit. Tab. 5.5 lists specific component values used on the demonstrator.

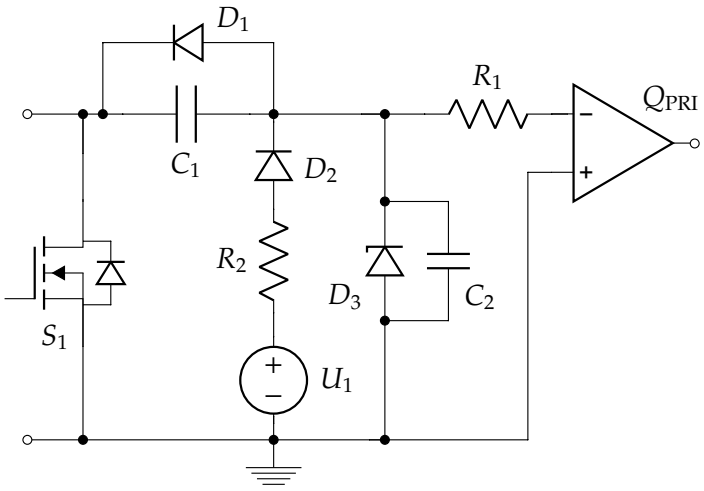


Figure 5.1: Schematic of circuit for detecting zero voltage crossings.

The network uses a capacitive divider (C_1 and C_2) to scale the drain-source voltage. Although using a simple divider would work in low frequency applications, the steep *dv/dt* across S_1 caused by a turn-ON request will also aggressively discharge the small capacitors before the zero crossing occurs; leading to an early signal from the comparator. However, adding the high-voltage diode D_1, zener diode D_3, and DC voltage source U_1 allows the comparator to indicate both a steep *dv/dt* event and the following zero voltage crossing as distinct and subsequent pulses.

If the *dv/dt* across S_1 is sufficient to cause a current through the capacitive divider greater than the maximum current from the U_1/R_2 combination ($i_{U(max)}$), C_2 will discharge and trigger the comparator before the zero crossing, just as before. However, due to the non-linear capacitance of super-junction MOSFETs and the triangular shape of the turn-ON request, the *dv/dt* slope softens as the parasitic capacitance of S_1 discharges closer toward 0 V.

This will allow C_2 to begin recharging; disabling comparator output until $V_{DS(S1)}$ falls below the DC supply voltage and crosses 0 V at which point the comparator will be triggered again. In summary, this means that a forced discharge of S_1's output capacitance from a turn-ON request will always cause a pair of quick, successive rising and falling edges from the primary comparator output – a double pulse.

By adapting the primary control accordingly, the first comparator output pulse can be acknowledged, but only a second pulse occurring within a given time window counts as a genuine signal to turn ON S_1. As an example, Fig. 5.2 shows a measured implementation of this approach using hardware described later in Section 5.4.

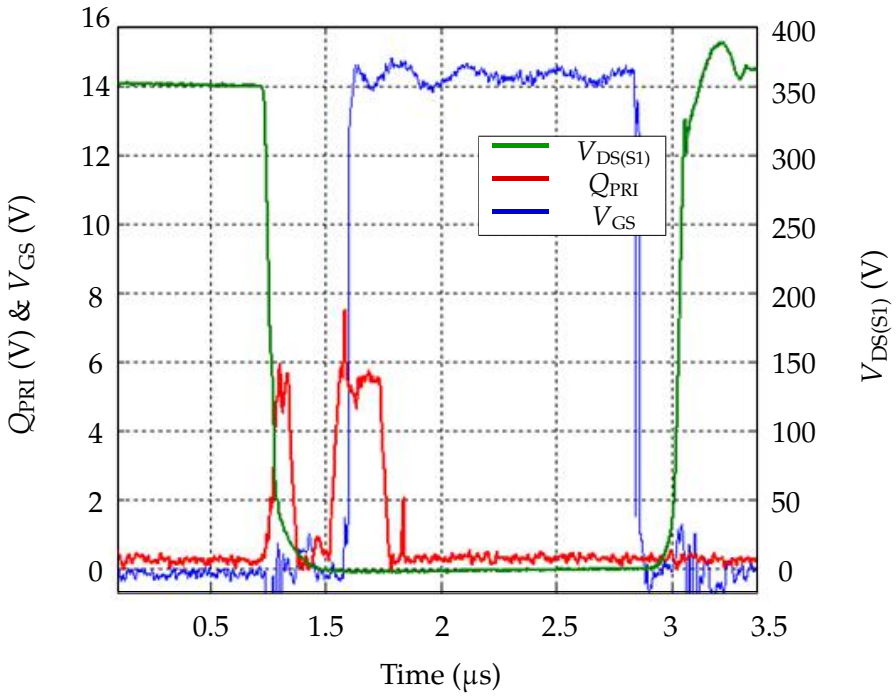


Figure 5.2: Measurement of primary V_{DS} sensing sub-circuit in operation.

If the primary logic only responds to such double pulses, the primary sensing subcircuit can autonomously distinguish intentional zero voltage crossings (caused by the turn-ON requests delivered from the secondary side) from undesired crossings that may occur during drain source voltage ringing (that cause only one pulse). There are two such ringing instances in Flyback operation:

1. "Flyback oscillation" between the main inductances and the parasitic capacitances of both MOSFETs while both S_1 and S_2 are OFF after synchronous rectification.

2. Ringing after primary switch turn-OFF whereby charge oscillates between the primary parasitic capacitance, the inductance, and the snubber network.

In the first case, the comparatively low frequency oscillations during t_{wait} incur a comparatively small *dv/dt*. If the current through C_1 remains below $i_{\text{U(max)}}$ the capacitance C_2 never fully discharges before the actual zero crossing and the comparator is only triggered at $V_{\text{DS(S1)}} < 0\,\text{V}$.

Thus the double pulse never occurs and the single pulse from the primary comparator would be "blanked" and S_1 would remain OFF. The series resistance R_2 can be used to set the sensitivity of the network's blanking capability by limiting the maximum current from U_1. It should fulfil the criteria:

$$\omega_0\, C_1\, \widehat{V}_{\text{DS(S1)}} < \frac{V_{\text{U1}}}{R_2} < C_1 \frac{d\widehat{V}_{\text{DS(S1)}}}{dt} \tag{5.1}$$

where $\widehat{V}_{\text{DS(S1)}}$ is the peak primary drain-source voltage, V_{U1} is U_1 voltage, $\widehat{dV_{\text{DS(S1)}}}/dt$ is maximum expected $V_{\text{DS(S1)}}$ slope, and ω_0 is the resonant frequency between L_1 and $C_{\text{OSS(S1)}}$ at the input voltage. The upper-limit ensures that C_2 discharges during steep *dv/dt*, the lower limit ensures that it does not during Flyback ringing. Setting $i_{\text{U(max)}}$ between these limits provides room for parameter drift and hardware tolerances.

In the second case – after S_1 turn-OFF – the overshoot amplitude and frequency is dependent on the peak inductor current, $C_{\text{OSS(S1)}}$, and the snubber. The frequency is typically very high and the *dv/dt* can exceed that caused by a turn-ON request. With insufficient snubber damping the turn-off ringing can also cause $V_{\text{DS(S1)}}$ to cross 0 V. As such the peak primary current and snubber parameters should be chosen such that a zero crossing after primary turn-OFF is impossible. This will only yield one pulse from Q_{PRI} (caused by steep *dv/dt*) ensuring that S_1 stays OFF.

5.2.2 Secondary Side – Synchronous Rectification

The secondary side V_{DS} sensing for synchronous rectification must provide two signals: when V_{DS} falls to zero (for turn-ON) and when the current falls to zero (for turn-OFF). Fig. 5.3 shows the basic comparator circuit used to achieve this. Once the body diode of S_2 is conducting, the potential at the comparator's inverting input becomes negative until the current through L_2 and S_2 falls below zero, at which point the potential flips direction indicating that synchronous rectification has ended.

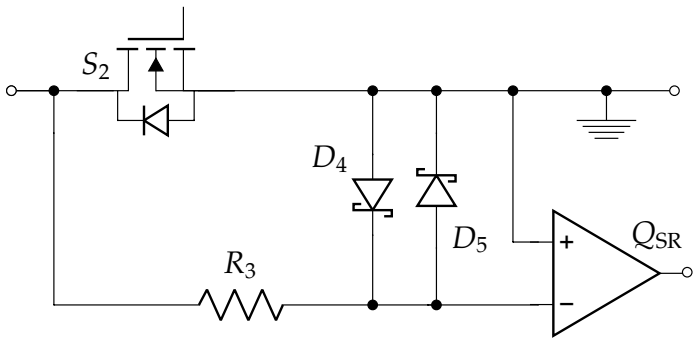


Figure 5.3: Schematic of sensing circuit for synchronous rectification.

5.2.3 Secondary Side – Output Voltage

The controller is fed a binary signal from another circuit indicating whether the output voltage is above or below a reference voltage. This simple resistive divider circuit is shown in Fig. 5.5. The reference voltage U_{REF} should be dimensioned to be equal to the desired output voltage scaled through R_4 and R_5. Once the scaled output voltage falls below this reference, the comparator output signal will be triggered.

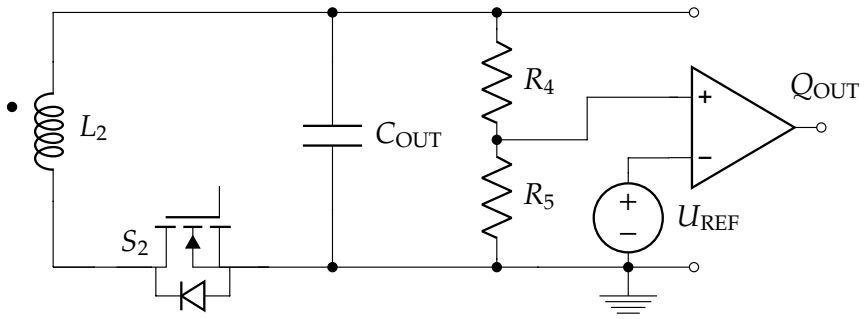


Figure 5.4: Schematic of output voltage sensing circuit in context with L_2 and S_2.

5.3 Constant ON-Time Control

Fig. 5.5 presents waveforms of the secondary side controlled Flyback during steady-state operation. The controller uses an adapted form of pulse-skipping control [51], along with triangular current mode (TCM) operation to drive the output load, generate the negative-current-turn-ON-requests and simultaneously achieve zero voltage switching (ZVS) [52].

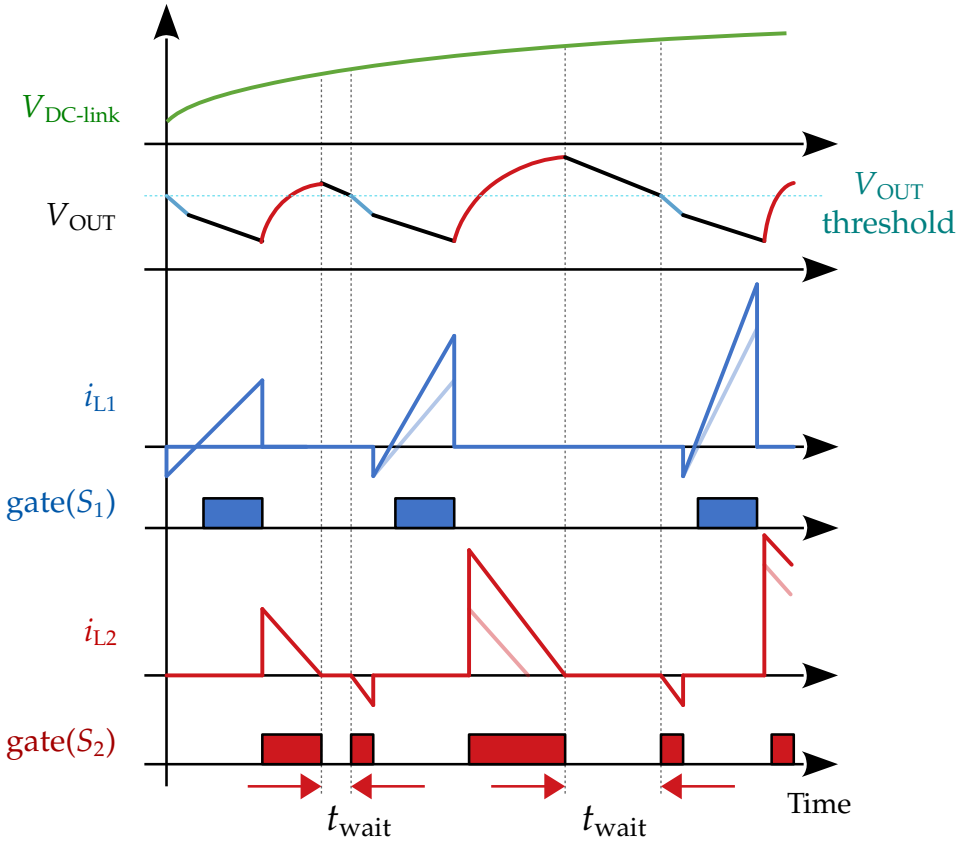


Figure 5.5: Sketch of COT control scheme with rising DC-link voltage.

As shown in Fig. 5.5, both switches are OFF during t_{wait} and the controller waits for the output voltage (V_{OUT}) to fall below its desired threshold value. The secondary switch is then turned ON for a short time T_{NEG} to energize the inductor to negative current I_{NEG} and turned OFF again to induce ZVS on the primary side and trigger a primary side turn-ON command. Independently, the primary side acts as a slave to the secondary side controller.

It constantly waits for its turn-ON command and, once it occurs, will turn ON S_1 for a fixed time T_{ON}; the ON-time required to deliver the rated power at the minimum point of expected input voltage ripple ($V_{DC\text{-}link(min)}$). A different fixed ON-time is used for high- and low-line input, but during operation, the same turn-ON-time is executed irrespective of input voltage ripple or load to keep the primary-side logic as reduced as possible. This, as indicated by the more transparent current trace in Fig. 5.5 (which shows the inductor current from the preceding switching cycle), shows that rising DC-link voltage results in rising peak inductor current. Once T_{ON} has elapsed, the primary switch turns OFF and begins to wait again for $V_{DS(S1)}$ to fall below zero. At this point S_2 acts as a synchronous rectifier: turning ON at $V_{DS(S2)}$ < 0 V and remaining ON while the secondary inductor de-energizes into the output capacitor/load. [12].

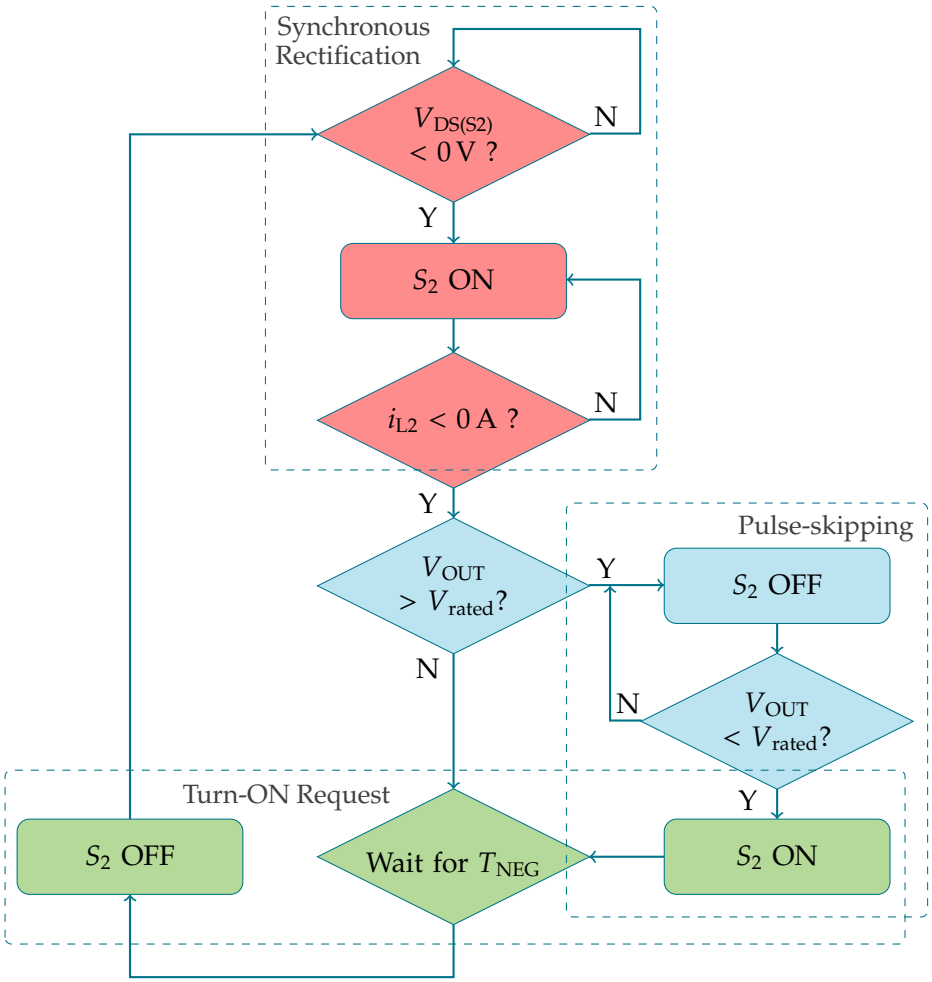


Figure 5.6: Flow chart of steady-state from perspective of secondary side controller.

Once the secondary inductor current falls to zero, the controller checks the status of the output voltage (via a simple comparator network) and either turns-OFF S_2 to begin t_{wait} and wait for the output voltage status to change ("pulse-skipping"), or leaves S_2 ON to immediately generate negative current for the next turn-ON request (T_{NEG}). Fig. 5.6 shows the basic function of the secondary side controller. Whenever the desired output voltage has been reached, the secondary side refrains from sending a negative current. A key aspect of pulse-skipping TCM is that during steady-state, the primary side "control" is in fact just the simple set response of a fixed ON-time. Due to the constant primary ON-time, the converter will operate with switching frequency that moves with the input voltage ripple and output load. When designing the converter, a maximum desired switching frequency ($f_{\text{S(max)}}$) should be selected. This switching frequency will occur at full load, minimum point of the input voltage ripple. The ON-time needed to deliver the required power at the minimum point of expected input voltage ripple ($V_{\text{DC-link(min)}}$) can be calculated using the following derived formula:

$$T_{\text{ON}} = \sqrt{\frac{2L_1 P_{\text{IN}}}{V_{\text{DC-link(min)}}{}^2 f_{\text{S(max)}}}} \tag{5.2}$$

The parameters $V_{\text{DC-link(min)}}$, P_{IN} and L_1 are defined in Section 5.3.2. Detailed analysis of primary-side based COT control for Flyback converters, including control stability and dynamic response, can be found in [53–55].

5.3.1 High- and Low-Line Input Voltage

From (4.3) and (5.2), it is evident that the control timings will change depending on whether the circuit is operating from high-line (230 V_{RMS}) or low-line (120 V_{RMS}) input voltage. For low-line, T_{NEG} can be shorter due to the reduced energy stored in $C_{\text{OSS(S1)}}$, but T_{ON} should be longer due to smaller V_{IN} across L_1. Therefore, both primary and secondary side controls should be aware of the input line voltage. The primary side has direct access to the input voltage and the secondary side can infer V_{IN} line voltage by sensing the reflected blocking voltage across S_2 while the primary switch is ON during the *energy storage* phase (during T_{ON}).

It should be noted however that the exact DC-link voltage (varying with DC-link ripple) is irrelevant due to the constant-ON time control approach. Awareness of high- or low-line input voltage is sufficient.

5.3.2 Coupled Inductor Design

With a constant-on-time/variable frequency control, it is critical to dimension the coupled inductor to supply rated power (P_{rated}) at the lowest expected input voltage ($V_{\text{DC-link(min)}}$). I.e. the minimum point of the input ripple for low line input:

$$V_{\text{DC-link(min)}}{}^2 = 2V_{\text{RMS}}{}^2 - \frac{P_{\text{rated}}}{C_{\text{DC-link}} f_{\text{grid}}} \tag{5.3}$$

Whereby V_{RMS} is the RMS grid voltage, f_{grid} is the grid frequency in hertz and $C_{\text{DC-link}}$ is the input capacitance. In such conditions, the converter's maximum effective switching frequency ($f_{\text{S(max)}}$) should occur with no pulse-skipping. With a given primary MOSFET it is possible to estimate the charge stored in its parasitic output capacitance ($Q_{C_{\text{OSS}}}$) from its datasheet using (4.1). Given that the same T_{NEG} will be used regardless of exact DC-link voltage, an estimate of the average power consumed by discharging C_{OSS} from the highest possible DC-link voltage ($V_{\text{IN(max)}}$) is defined as:

$$P_{\text{neg}} = \frac{1}{2} Q_{C_{\text{OSS}}} V_{\text{IN(max)}} f_{\text{S(max)}} \tag{5.4}$$

Again, this will only be a guiding under-estimate since constant C_{OSS} and zero leakage inductance is assumed. The total power (P_{IN}) is the sum of the P_{rated}, the circuit losses (P_{loss}) and P_{neg}:

$$P_{\text{IN}} = P_{\text{rated}} + P_{\text{neg}} + P_{\text{loss}} \tag{5.5}$$

By using the top-level specifications of output voltage (V_{OUT}) and rated power, along with the turns-ratio (N), desired maximum switching frequency and minimum input voltage ripple, it is possible to calculate the required inductances by assuming the ideal current waveforms. Using fundamental equations, it is possible to derive:

$$L_1 = \frac{1}{2 f_{\text{S(max)}} A^2 (\sqrt{P_{\text{IN}}} + \sqrt{P_{\text{neg}}})^2} \tag{5.6}$$

where:

$$A = \frac{1}{V_{\text{DC-link(min)}}} + \frac{1}{N V_{\text{OUT}}} \tag{5.7}$$

The secondary inductance can then be found using the turns-ratio and (2.12).

Due to inevitable leakage inductance, the actual magnetizing inductance will be smaller than the value given by (5.7) and therefore additional turn(s) should be added to compensate. Leakage inductance can be estimated using short and open circuit tests [56, 57]. For a universal-input adapter, low-line input voltage should be used for these calculations. However, $f_{S(max)}$ will occur with high line input due to the smaller fixed ON-time.

5.3.3 Start-Up Routine and Primary Logic

The secondary side controlled Flyback concept requires the output capacitor (C_{OUT}) to be charged before the turn-ON requests required for primary side ZVS are possible; there must therefore be a method of charging C_{OUT} at start-up. While any start-up routine must necessarily be undertaken by the primary side due to the lack of output voltage, it must be done without additional measurement/computation to maintain very simple primary side control – simple enough to be implemented with dedicated discrete logic. It was assumed that the load is disconnected from the output capacitor at start-up via a load-disconnect switch as with the existing USB-PD controller shown in [58]. Briefly stated:

1. The primary side is connected to grid input voltage.
2. The primary side sends low frequency pulses to charge C_{OUT} via S_2's body diode until secondary side "wakes up".
3. Using the synchronous-rectification sensing, the secondary side waits for the end of a charging pulse and then sends a negative current pulse putting the primary side into "slave" mode.
4. Steady-state control begins.

Specifically, as soon as C_{OUT} is charged beyond rated output voltage (V_{rated}) the controller connects to the load and takes responsibility for maintaining the output voltage. This control transition occurs at V_{rated} so that the fixed negative current time is sufficient to achieve a zero voltage crossing on the primary side. With active measurement of V_{OUT} and continuous calculation of T_{NEG}, it would be possible to begin secondary side control earlier, as soon as V_{OUT} is sufficient to power the controller. However, this was not implemented here.

Fig. 5.7 shows a flow chart of the start-up routine from the perspective of both primary and secondary side. The frequency of the initial charging pulses from the primary side must be low enough to provide plenty of time to fit the first "hands-hake" turn-ON request before the next pulse. Once the secondary side controller enters "steady-state", it follows the block diagram in Fig. 5.6.

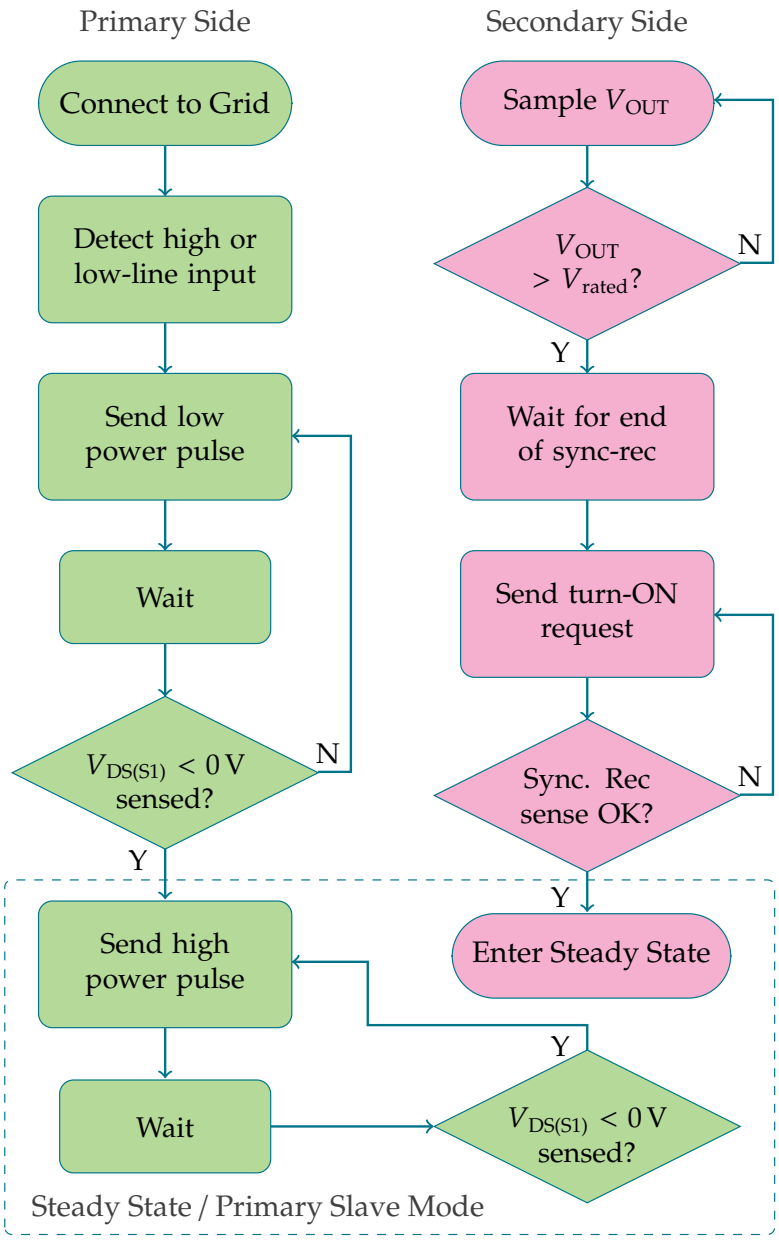


Figure 5.7: Flow chart of primary start-up routine with secondary side response.

5.4 65 W Demonstrator Hardware – SSCF1

A 65 W prototype was built to demonstrate the Secondary Side Controlled Flyback concept. It was designed to supply 20 V_{DC} output with a maximum switching frequency of 270 kHz. This specific prototype is herein referred to as *"SSCF1"* – Secondary Side Controlled Flyback 1. This section briefly describes the construction of the coupled inductor, the chosen prototyping control boards and the power board.

5.4.1 Control Boards

For prototyping purposes and to easily experiment with primary switching times, both controllers were based on external control boards with an FPGA used to process primary side double-pulse requests, rather than dedicated discrete logic. Tab. 5.1 lists the two control boards used. The FPGA board was operated with a 27 MHz clock, introducing 37 ns of additional delay to primary side turn-ON.

Table 5.1: External control boards for *SSCF1*

Primary Side	LATTICE iCE40-HX8K FPGA
Secondary Side	INFINEON XMC4500 Relax Lite

The XMC4500 incurred a synchronous rectification turn-ON delay of up to 81 ns (although this is relatively inconsequential since current can conduct through S_2's body diode). The overall delay for turn-OFF was 35 ns; creating a small pulse of negative current of ≈ -255 mA (-45 mA on primary side) at the end of each synchronous rectification period. Significant enough to incur non-negligible current circulation, but far from enough to risk causing an unwanted S_1 turn-ON command.

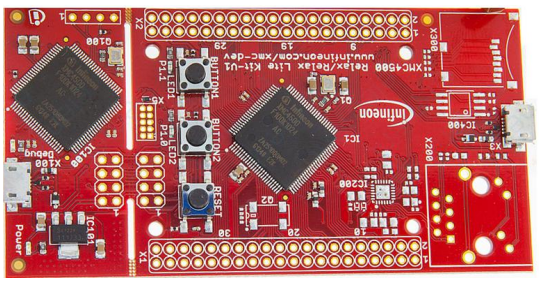


Figure 5.8: INFINEON XMC4500 Relax Lite prototyping controller board.

5.4.2 Coupled Inductor Design

In general, a Flyback's coupled inductor core/winding arrangement should avoid saturation, have low leakage and incur minimal losses. It is also preferable that the switching frequency at low- and high-line is relatively similar. A large turns-ratio (N) allows the use of secondary side MOSFETs with a lower voltage rating (generally lower device losses), but causes high-line switching frequency to rise further away from low-line. The effect of turns-ratio on total switching period can be seen in the derived equation (5.8).

$$\frac{1}{f_S} = T_{NEG} + 2P_{IN}L_1\left(\frac{1}{V_{IN}{}^2} + \frac{1}{NV_{IN}V_{OUT}} + \frac{1}{N^2V_{OUT}{}^2}\right) \tag{5.8}$$

Using MATLAB [59] and GeckoCircuits simulation software [60], a turns-ratio of $N = 5$ was found to offer a good balance between frequency range and losses [59, 60]. By using (5.6) to find the inductances required for 270 kHz operation and determining peak currents and flux densities, an appropriate core shape/size could be found as shown in Tab. 5.2.

Table 5.2: Key parameters of *SSCF1* coupled inductor

Parameter	Symbol	Value
Turns-Ratio	N	5 (15:3)
Primary Inductance	L_1	77 µH
Secondary Inductance	L_2	3.1 µH
Low-Line Peak Currents	$\hat{I}_{L1} : \hat{I}_{L2}$	4.1 A : 20.5 A
High-Line Peak Currents	$\hat{I}_{L1} : \hat{I}_{L2}$	3.9 A : 19.6 A
Core Shape/Material	–	RM10i / 3C95
Air gap	l_g	300 µm
Winding Type	pri : sec	litz : foil
Winding Arrangement	inn : out	15 : 3

To see whether the Secondary Side Controlled Flyback concept could be used on the most rudimentary power boards, a simple two-layer winding arrangement was chosen for the coupled inductor (although litz wire was used for the primary winding to help reduce winding loss).

5.4.3 Power Board

The *SSCF1* power board used the components listed in Tab. 5.3 and the assembled board is shown in Figs. 5.9 and 5.10. The large loops were included to easily measure primary and secondary inductor current but could be short-circuited when not needed – minimizing stray inductance. Excluding the loops, the boxed dimensions were 3.0 cm × 6.5 cm × 2.3 cm which equals 44.2 cm^3 (2.7 inch^3). Excluding the input emi-filter, the resulting power density was 1.47 W/cm^3 (23 W/inch^3).

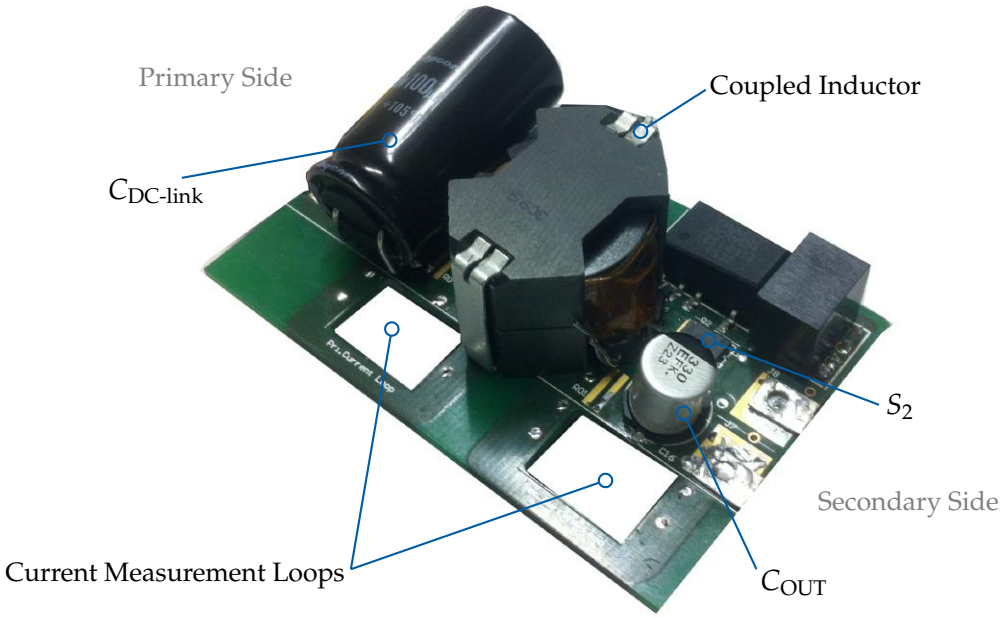


Figure 5.9: 65 W demonstrator, *SSCF1*. Dimensions: 3.0 cm x 6.5 cm x 2.3 cm.

Table 5.3: Key parameters and components of the *SSCF1* power board.

Input Capacitance	$C_{DC\text{-}link}$	110 µF
Output Capacitance	C_{OUT}	400 µF
Primary MOSFET	S_1	CoolMOS P6 255 mΩ ThinPAK 8x8
Secondary MOSFET	S_2	OptiMOS 5 3.5 mΩ (100 V) SuperS08
Gate Driver	-	Infineon Eice 2EDN7524F

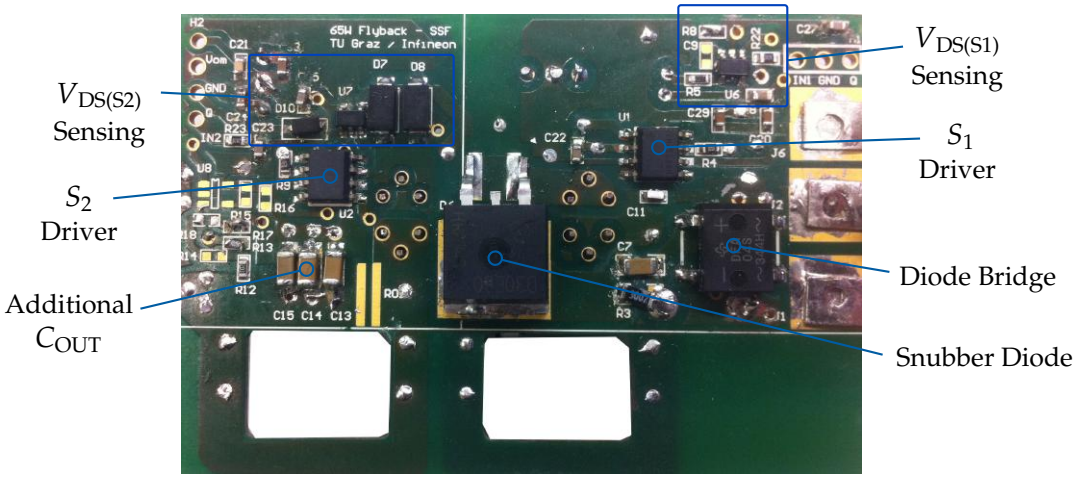


Figure 5.10: *SSCF1* back side.

Tab. 5.4 lists the snubber parameters (see Fig. 2.5) required to ensure that the peak $V_{DS(S1)}$ overshoot (due to L_1 leakage inductance) remained below the voltage rating of S_1. The employed values were first estimated via analytic calculation and were then refined empirically.

Table 5.4: RCD snubber components for *SSCF1*

Resistance	R_{Sn}	15 kΩ
Capacitance	C_{Sn}	6.4 nF
Diode	D_{Sn}	IDP08E65D1 (650 V)

An additional EMI-filter board was made to provide differential and common mode noise suppression to satisfy the Class B SMPS requirements [61–63]. Due to the variable frequency control scheme, the filter was required to provide significant damping across a range of switching frequencies – mandating a large filter [64, 65]. The final filter volume was 40.3 cm^3 (2.46 $inch^3$). The total converter volume was 84.5 cm^3 (5.16 $inch^3$) resulting in an overall power density of approximately 0.77 W/cm^3 (12.6 $W/inch^3$). The large EMI-filter is a drawback of the variable frequency/COT approach.

The various DC voltages required for the gate drivers, comparators and sensing references were derived from a single 15 V bus using a combination of on-board DC-DC converters and resistive dividers.

5.4.4 Sensing – Passive Component Parameters

Tab. 5.5 lists the components used for the drain-source voltage sensing sub-circuits shown in Fig. 5.1 and Fig. 5.3.

Table 5.5: Key components for *SSCF1* V_{DS} sensing.

High Voltage Diode	D_1	MURS160T3G (600 V)
Voltage Source Diode	D_2	DA221FHTL
Zener Diode	D_3	MM3Z47T1G (4.7 V)
High Voltage Capacitor	C_1	3 pF
Low Voltage Capacitor	C_2	60 pF
Comparator Protection	R_1	1.0 kΩ
Current Limiter	R_2	500 Ω
DC Voltage Source	U_1	5.0 V
Pri. & Sec. Comparator	-	ADCMP600
Sec. Current Limiter	R_3	5.6 kΩ
Schottky Diodes	D_4 , D_5	B340A-12-F (40 V)

The capacitances C_1 and C_2 include the estimated parasitic capacitances of the high-voltage diode and zener diode respectively. I.e. zener diode capacitance plus C_2 = 60 pF. The resistor R_2 was dimensioned with (5.1) assuming a 5 V source for U_1 and using the datasheet for S_1 listed in Tab. 5.3. In order to reduce current through the secondary side comparator's parallel zener diodes, the resistor R_3 was chosen to be as large as possible without noticeably slowing sensing response time. Tab. 5.6 lists the components used for the output voltage sensing in Fig. 5.4.

Table 5.6: Key components for *SSCF1* V_{OUT} sensing.

Resistive Divider	R_4	60 kΩ
Resistive Divider	R_5	15 kΩ
Comparator	-	ADCMP600
DC Voltage Source	U_{REF}	4.0 V

5.5 Experimental Results

This section focusses firstly on the feasibility of the secondary side Flyback controller with zero voltage primary turn-ON, and secondly on the corresponding operating consequences of using COT control with the proposed concept. The following measurements of the *SSCF1* prototype are presented in this section:

- Steady-state COT operation.
  - High- and low-line behaviour (230 V_{RMS} and 120 V_{RMS}).
  - Frequency and power limit.
  - Switching frequency vs. output load.
- Primary side drain-source voltage sensing.
  - Propagation delay vs. opto-isolators.
  - Autonomous zero crossing blanking.
- Start-up routine.
- Converter efficiency measurements and loss analysis.
  - Efficiency for both high- and low-line input voltages.
  - Component loss breakdown and suggested improvements.

5.5.1 Steady-State COT Operation

Both high- and low-line input voltages were tested between 10 % and 100 % rated load (and beyond into overload conditions). This section gives the fixed primary ON-time (T_{ON}) and turn-ON request time (T_{NEG}) used in each case, as well as selected measurements of steady-state operation and the switching frequency range for each load point.

High-Line Input Voltage

High-line steady-state operation was tested using 230 V_{AC} input voltage and with the fixed primary ON time (T_{NEG}) and negative current pulse time (T_{ON}) shown in Tab. 5.7. A 12 % larger ON-time was used than calculated with (5.2) due to losses and leakage inductance.

Table 5.7: Fixed switching times for steady-state COT high-line operation.

Secondary Negative Current Time	T_{NEG}	0.70 µs
Primary ON-time	T_{ON}	0.85 µs

Fig. 5.11 shows a measurement of primary drain-source voltage and secondary side inductor current during steady-state operation at high-line. The measurement is taken at 70 % load at the peak of the DC-link ripple, resulting in a switching frequency of 175 kHz and a peak inductor current of 4 A and 20 A for primary and secondary side respectively. The negative current on the secondary side required to discharge the chosen primary MOSFET in such conditions was −4.2 A – a relatively large current equating to −900 mA on the primary side.

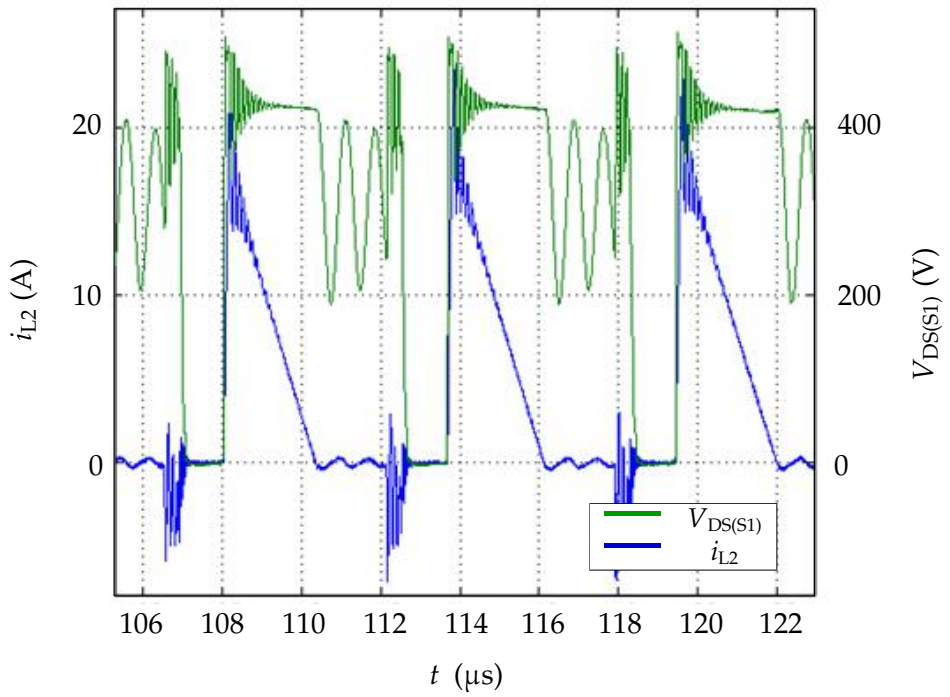


Figure 5.11: Measured $V_{DS(S1)}$ and i_{L2} in high-line steady-state COT operation.

The secondary side controller does not monitor the input ripple and therefore the same peak negative current was used throughout the entire AC grid period, regardless of exact DC-link voltage and energy stored in $C_{OSS(S1)}$. For a given output load and DC-link voltage, the binary output voltage sensing determines the switching frequency by indicating when the next switching cycle should begin.

For example, at $t = 116\,\mu s$ in Fig. 5.11, the secondary inductor has de-energized and the controller refrains from sending the subsequent negative pulse, indicating that V_{OUT} exceeds the 20 V threshold and the control has re-entered t_{wait} for pulse-skipping. At $t = 117.9\,\mu s$, the turn-ON request is sent, indicating that V_{OUT} fell below its reference value and the V_{OUT} comparator signal has fallen low.

With sufficient C_{OUT}, the output ripple is mainly dependent on the sensitivity of the output voltage sensing and the speed of the controller. To a lesser extent it is determined by the peak inductor currents and negative current pulse. A measurement of output ripple for high line corresponding to Fig. 5.11 is shown in Fig. 5.12. The peak ripple was found to be 282 mV (1.4 % of mean V_{OUT}).

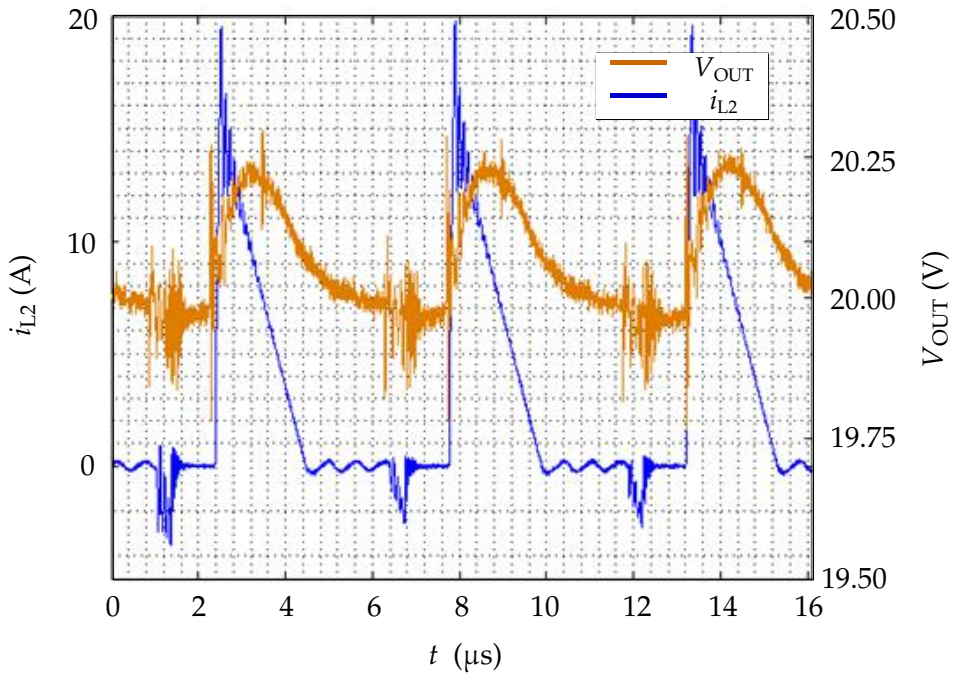


Figure 5.12: Measured V_{OUT} and i_{L2} in high-line COT steady-state operation.

Low-Line Input Voltage

Low-line tests used 120 V_{AC} input and thus employed a larger T_{ON} and smaller T_{NEG} as shown in Tab. 5.8. Though the negative current pulse is smaller for low-line, output voltage ripple was almost identical to high-line because of the increased ON-time. Peak low-line output voltage ripple was 301 mV (1.5 % of mean V_{OUT}).

Table 5.8: Fixed switching times for steady-state low-line COT operation.

Secondary Negative Current Time	T_{NEG}	0.45 µs
Primary ON-time	T_{ON}	1.75 µs

Device Stresses

To give an impression of device stress, Tab. 5.9 lists the "worst-case" blocking voltages and drain currents for primary and secondary switches. The peak V_{DS} values are measurements of the overshoot peak after each switch's respective turn-OFF.

Table 5.9: Maximum blocking voltages and drain currents for S_1 and S_2.

	S1	S2	Occurs during:
Peak V_{DS}	532 V	86.9 V	Peak DC-link voltage at high-line
RMS V_{DS}	345 V	36.8 V	High-line input at full output load
Mean V_{DS}	308 V	20.1 V	*As above.*
Peak I_d	4.10 A	20.5 A	Peak DC-link voltage at low-line
RMS I_d	1.19 A	6.73 A	Low-line input at full output load
Mean I_d	0.71 A	3.66 A	*As above.*

Outside of the specific conditions specified in Tab. 5.9, the blocking voltages and drain currents during steady-state are smaller and dependent on the input line voltage and input voltage ripple, and indirectly by the output load.

Frequency Limit and Synchronous Rectification

Each fixed primary ON-time for high- and low-line was chosen to support full load for any DC-link voltage within the expected input ripple range. It follows that within rated power, some pulse skipping will always occur. However, Fig. 5.13 shows a measurement taken above 100 % output load whereby no pulse skipping occurred at the minimum point of the input voltage ripple. It shows drain-source voltages for two low-line switching periods along with two secondary side control signals; synchronous rectification comparator output and S_2 gate-drive signal. Between $t = 1.55$ µs and $t = 3.15$ µs, comparator output is high indicating that the current through S_2 is positive and that synchronous rectification is ongoing.

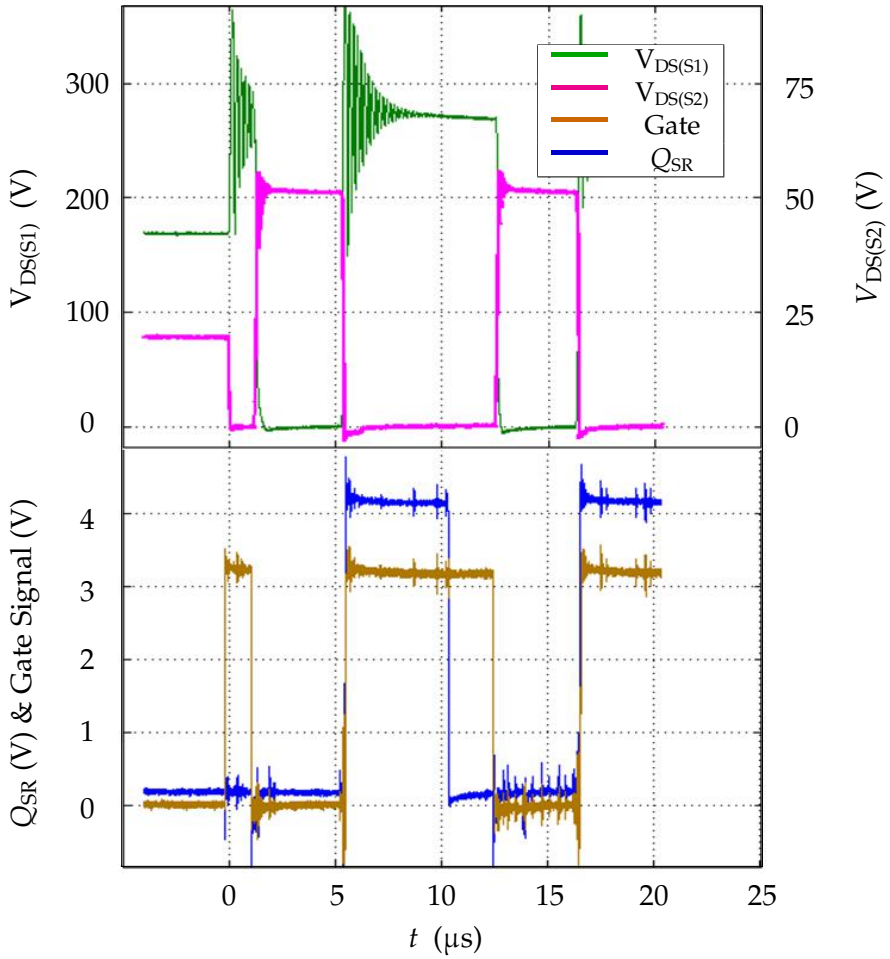


Figure 5.13: V_{DS}, sync. rec sense and S_2 gate signals in overload conditions.

Afterwards, the comparator output goes low indicating that current is now negative but S_2 is then kept ON for the fixed time (T_{NEG}) with zero t_{wait}, to immediately transition into a negative current for a turn-ON request. When no pulse-skipping occurs, the converter is operating at its power and switching frequency limit – no additional power can be delivered with the fixed ON-time and V_{OUT} will drop.

With timings optimized for rated output power and healthy grid voltage, this zero wait period will occur at minimum expected input voltage ripple and 100 % load. However, it follows that in the event of unexpected low grid voltage, optimized timings will not be able to provide stable output voltage at 100 % load. To compensate for a low grid voltage and maintain very simple primary side logic with constant ON-time, the ON-time must be oversized for regular operation – a significant disadvantage of the COT approach.

Variable Switching Frequency Range

The COT approach was chosen because it allows the primary logic to remain very simple: allowing as much control to move to the secondary side as possible. However, for a given load, such a constant primary ON-Time necessarily leads to variable switching frequency that drifts with the input voltage ripple, as explained in Section 5.3.

Using the switching times specified in Tabs. 5.7 and 5.8, the maximum and minimum switching frequencies were measured for high- and low-line. Fig. 5.14 shows the range of switching frequencies in each case for 10-100 % load. This resulted in the peak low-line switching frequency to be slightly below the 250 kHz desired maximum calculated with (5.8) due to the slightly increased ON-time used to compensate circuit losses.

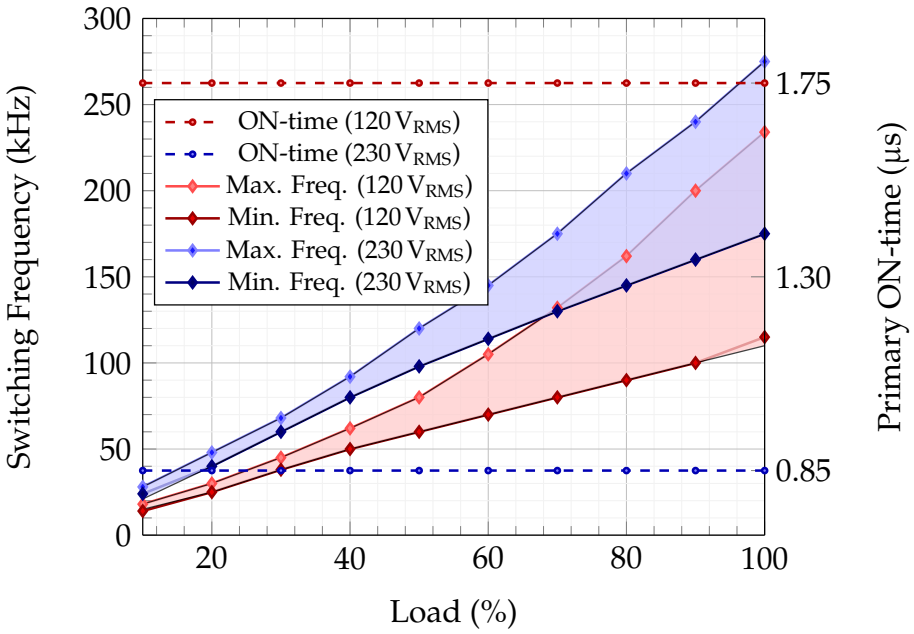


Figure 5.14: *SSCF1* Switching frequency and primary ON-time vs. output load.

The range of switching frequencies is proportionally much larger for high loads due to the larger input voltage ripple. At full load there is a difference of more than 100 kHz for both high- and low-line input. As the output load decreases, the switching frequency range and magnitude also decrease due to the ever-increasing wait time between turn-ON requests. This caused low-line operation with 10 % load to be below 20 kHz and audible.

Such a wide range in switching frequency severely limits the optimization of the coupled inductor design (core material, air gap,...) since the fixed ON-time must be large enough to support full load at the lowest input voltage ripple, meaning that peak inductor current is very high at the peak of the input voltage ripple. This further exacerbates the amount of pulse-skipping for low loads due to the smaller input voltage ripple – leading to an even lower switching frequency. As predicted by (5.8), high-line operation yielded slightly higher switching frequencies across the load range (due to larger input voltage and the reduced primary ON-time) but remained within the same general order of magnitude as with low-line (due to the increased negative current time).

5.5.2 Primary Side Drain-Source Sensing Behaviour

The primary side drain-source sensing is a critical part of proving the feasibility of the proposed opto-isolator free communication. Measurements of the double-pulse sensing operating under high- and low-line can be seen in Fig. 5.15 and Fig. 5.16 with the initial pulses (caused by the steep V_{DS} slope) occurring at $t \approx 1.55\,\mu s$ and $t \approx 0.95\,\mu s$ respectively. Overall sensing reliability has been demonstrated through continuous steady-state operation, but it is also important for the primary side sensing to be robust in terms of unwanted zero voltage crossings, and to be competitive with opto-isolators in terms of "propagation delay".

Primary Side Turn-ON Delay

A conventional primary side controller communicates to the synchronous rectification switch via an opto-isolator or magnetic coupling. Likewise, a secondary side controller would communicate to the primary switch in the same way. For the proposed strategy to compete with existing secondary side approaches, the delay between the zero crossing and subsequent S_1 turn-ON should be less than the propagation delay of a modern standard opto-isolator (70-150 ns) and it should compete with fast digital opto-isolators (25-50 ns) [66, 67]. As seen in Figs. 5.15 and 5.16, the total delay between the drain-source zero voltage crossing of S_1 and the subsequent gate signal into the driver was measured to be 71 ns at high-line, and 75 ns at low-line input voltage. Importantly, the FPGA clock causes 37 ns of this delay, meaning that the actual circuit delay is 34 ns and 38 ns for high- and low-line respectively.

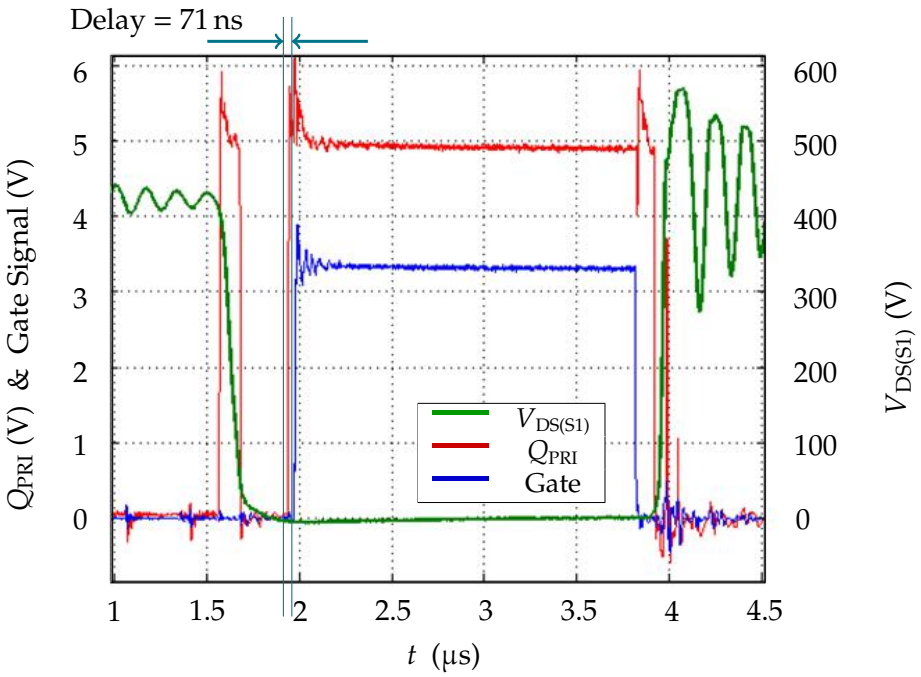


Figure 5.15: Demonstration of primary side V_{DS} sensing at high-line.

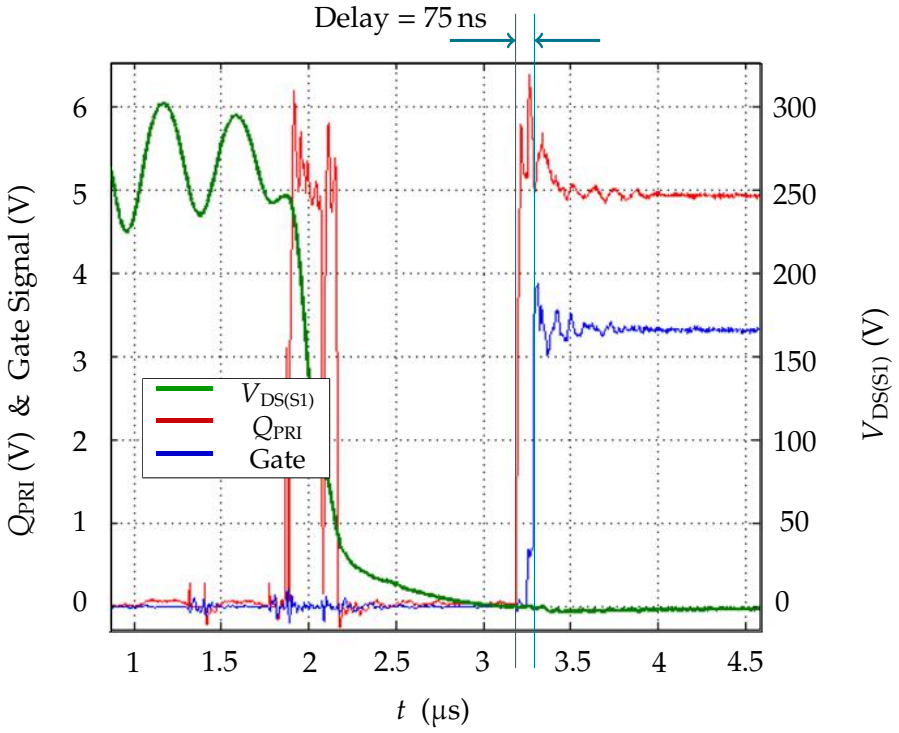


Figure 5.16: Demonstration of primary side V_{DS} sensing at low-line.

These measurements indicate that this sensing approach is indeed able to outperform most, and match the delay of the fastest opto-isolators. If the gate-driver propagation delay and MOSFET turn-ON time are also included, this prototype achieved an overall delay time of ≈112 ns which is almost as fast as standard opto-isolators alone. Tab. 5.10 lists a breakdown of primary turn-ON delay.

However, these measurements also reveal a limitation. In Fig. 5.16, the total delay between the end of the turn-ON request and primary zero voltage crossing is 395 ns. This time is determined by the magnitude of negative current and S_1's parasitic output capacitance. This limits the approach in very high switching frequency applications – 395 ns would be very large for a 1.0 MHz converter with a switching period of just 1 µs. Increasing the negative current would reduce this time, but reduce efficiency and consume more of the available duty cycle. Another option would be to use a device with significantly smaller output capacitance.

Table 5.10: Primary side sensing and turn-ON delay times.

Source	Delay Times (ns) Low-Line	High-Line
Sense Circuit	34	30
Comparator	4	4
FPGA	37	37
Total Signal Delay	75	71
Driver Propagation	20	20
Turn-ON Time	18	20
TOTAL	113	111

Flyback Ringing Blanking

To test the autonomous filtering of false turn-ON signals, the input voltage was reduced to force the primary Flyback voltage to cross 0 V after primary turn-OFF. Fig. 5.17 shows the primary control's response in such conditions. No gate signal is generated at $t = 7.5$ µs despite the definite zero crossings of $V_{DS(S1)}$ observed. The dv/dt across S_1 prior to the zero crossing is insufficient to trigger the comparator and thus the primary control only receives a single pulse – no gate signal is generated and S_1 successfully remains OFF.

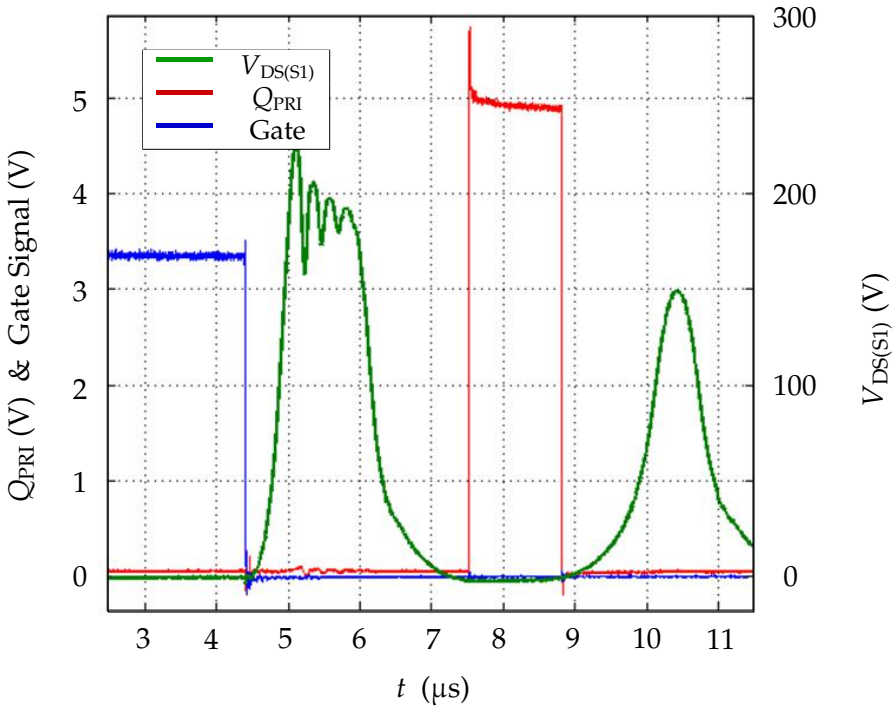


Figure 5.17: Demonstration of blanked zero voltage crossings in Flyback ringing.

5.5.3 Start-Up Routine

Measurements of the start-up routine described in Section 5.3.3 with low-line input voltage are presented here. The primary side was programmed to execute 25 kHz charging pulses with an ON-time of 550 ns, resulting in peak primary inductor current of approximately 1.2 A. Using such a small frequency and ON-time provides plenty of space for the secondary controller to deliver its initial handshake turn-ON request after rated voltage has been achieved. Fig. 5.18 shows the end of the charging phase at $t \approx 142$ ms, and the fall of the output voltage to the minimum value until the secondary side takes control and connects the output load at $t \approx 154$ ms.

A close-up view of the handshake turn-ON request is shown in Fig. 5.19. After sufficient output voltage is sensed, the secondary controller uses the synchronous rectification sensing to wait until the secondary inductor is de-energised (end of synchronous rectification). It then sends a "handshake" turn-ON request to the primary side. As soon as the forced zero voltage crossing is detected across S_1, the primary side enters "steady-state", halting the 25 kHz charging pulses and returning a single full-power pulse before waiting for the next turn-ON request.

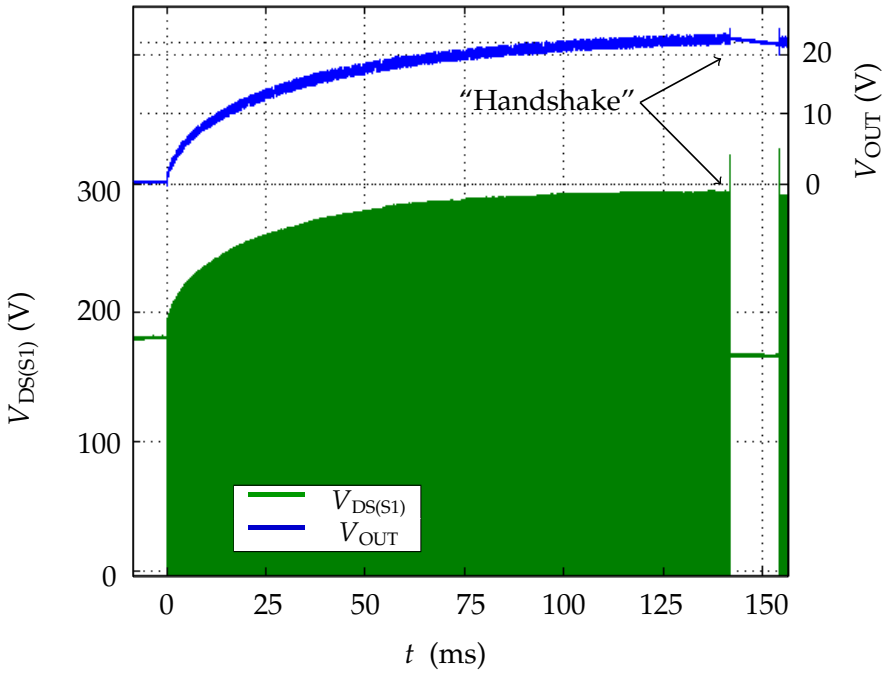


Figure 5.18: Measurement of proposed start-up routine with low-line input voltage.

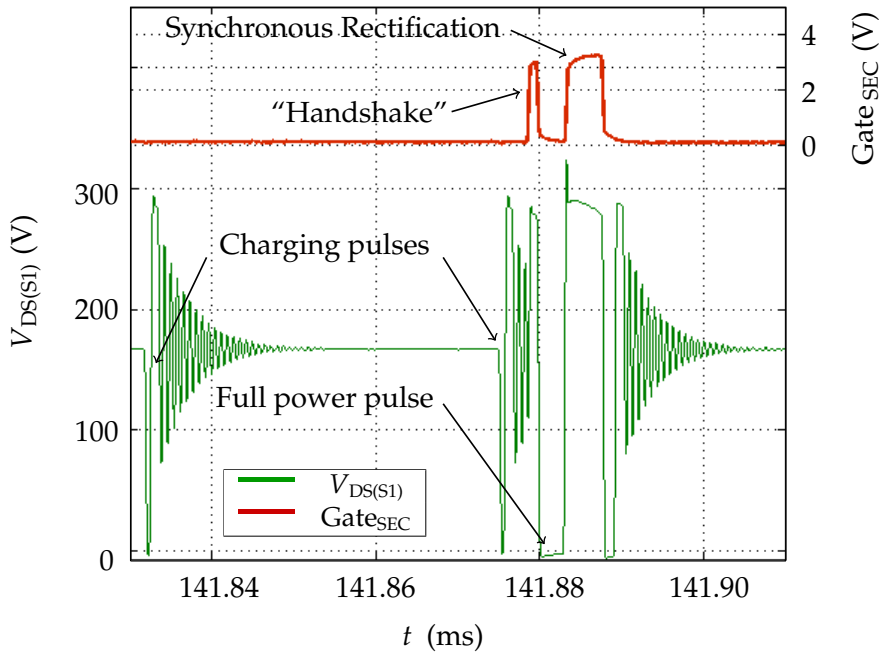


Figure 5.19: Annotated close-up of end of proposed start-up routine.

5.5.4 Efficiency Measurements

The *SSCF1* demonstrator was built to show the proposed concept as a feasible and workable control strategy, with efficiency as a secondary concern. Nonetheless, this section briefly discusses efficiency measurements taken from the *SSCF1* demonstrator and how to improve the results to match current state-of-the-art. For context, a target efficiency is taken from the PMP9208 power adapter reference design from *Texas Instruments, Inc.* [37]. This professional Flyback demonstrator has the same rated output power (65 W) and a similar output voltage of 19.5 V (rather than 20 V).

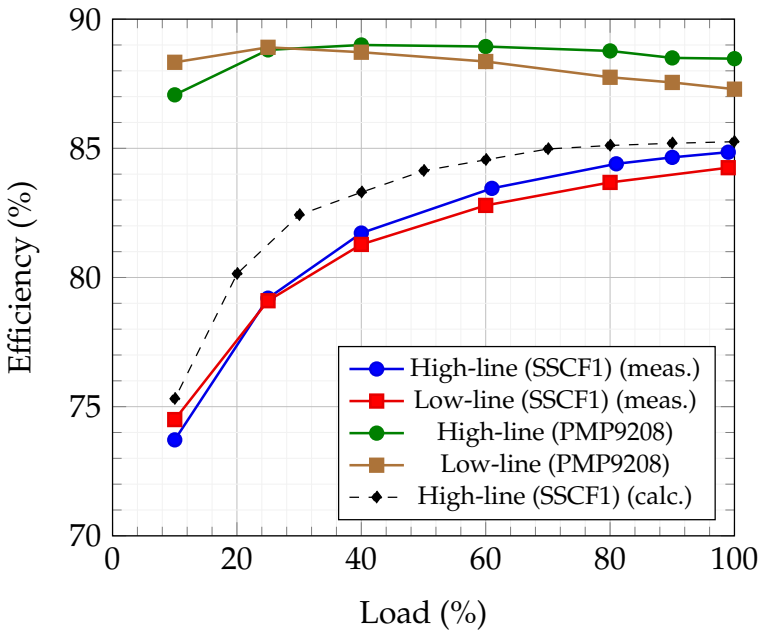


Figure 5.20: Measured and calculated *SSCF1* efficiency against PMP9208.

The PMP9208 uses a more conventional UCC28630 primary side regulation controller and conveniently uses the same coupled inductor core shape (RM10i), however the core materials are different (3C96 rather than 3C95) [68]. Input and output power were measured at multiple load points using a "Norma-5000" power analyzer and with both high- and low-line input voltage (230 and 120 V_{RMS} respectively) [69]. Fig. 5.20 shows the efficiency based on these measurements, as well as that of the PMP9208. The *SSCF1* exhibited significantly poorer efficiency than the reference design, especially at low load. The following analysis shows however, that this was mostly due to the construction of *SSCF1*'s coupled inductor rather than a direct consequence of the control scheme.

5.5.5 Loss Breakdown

Fig. 5.21 shows a breakdown of the main losses for the *SSCF1* demonstrator operating under high-line input voltage. Following the same approach specified in [70], the individual loss contributions were calculated using a combination of analytic methods and simulation. The corresponding calculated efficiency is shown in Fig. 5.20 alongside the measured values, showing an over-estimated but reasonable match. The loss breakdown for low-line input voltage is not presented here since each contribution is broadly similar to that of high-line and does not alter the following analysis.

5.5.6 Effect of Proposed Secondary Side Control on Efficiency

The proposed concept (sending turn-ON requests from secondary side to the primary side switch via the coupled inductor) incurs additional device losses when generating the negative current pulse requests. However, Fig. 5.22 shows that the loss contribution from the corresponding sources (S_2 conduction, gate, turn-ON and turn-OFF loss) are relatively small and are not responsible for the poor efficiency. Some of these additional losses are also offset by the synchronous rectification and zero voltage primary turn-ON features offered by the Secondary Side Controlled Flyback.

5.5.7 Effect of Non-Optimal Coupled Inductor on Efficiency

The two largest loss contributions (accounting for $\approx 62\,\%$ of losses) are snubber loss and core loss. The former caused by dissipating the energy stored in the leakage inductance at primary turn-OFF, and the latter caused by hysteresis and eddy current effects. [71] The magnitudes of these contributions are determined by the coupled inductor, and not by the Secondary Side Controlled Flyback concept nor directly by the COT control scheme. By contrasting the two coupled inductor designs, it is possible to estimate how the demonstrator efficiency might compare to the reference design if the core material and coupling factor were identical.

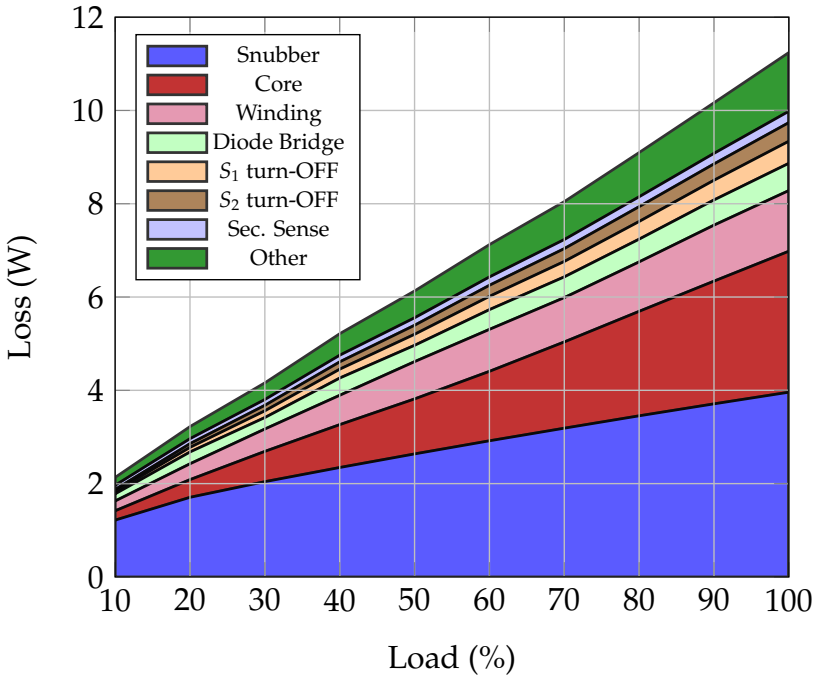


Figure 5.21: Overall loss breakdown for *SSCF1* in high-line operation (calculated).

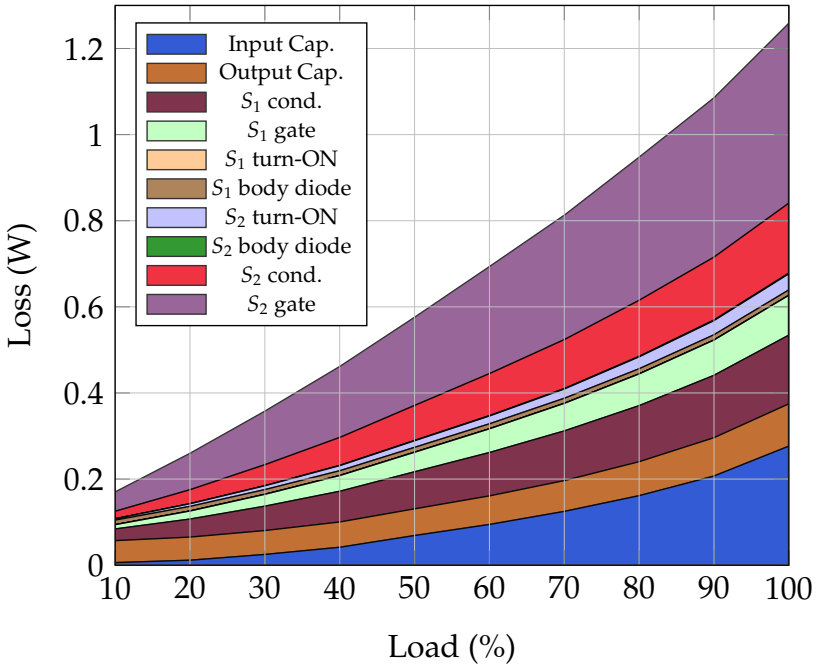


Figure 5.22: Breakdown of loss contributions labelled as "Other" in Fig. 5.21.

Leakage Inductance

The snubber loss shown in Fig. 5.21 represents the leakage energy dissipation required to keep the primary voltage overshoot safely below the rated voltage of the primary switch (600 V). The primary side leakage inductance of *SSCF1* was measured and is shown in Tab. 5.11 along with the resulting coupling factor. RCD snubber parameters are given in Tab. 5.4. A coupling factor (k) of 0.963 represents considerably inferior coupling than for the reference design, which had a coupling factor of 0.984. As well as winding type and core shape, winding arrangement is an important factor. The *SSCF1* used a simple non-interleaved arrangement whereby the entire primary winding was surrounded by the entire secondary foil winding. In contrast the reference design was interleaved with the primary wound on both sides of the secondary foil – a reliable method of reducing leakage [72].

Table 5.11: Measured leakage inductance and coupling factor for *SSCF1*.

Primary Inductance	L_1	77.0 µH
Primary Leakage Inductance	$L_1{}^{\sigma}$	2.84 µH
Coupling Factor	k	0.963

Core Material

By repeating the core loss calculation using the 3C96 material used in the reference design instead of the 3C95, the core loss reduces significantly. For example, at 100 % load, the core loss would fall from 3.02 W to 2.37 W.

Modified Loss Calculation

Replacing the *SSCF1* demonstrator's core material and coupling factor with that of the reference design shows a calculated efficiency improvement of ≈ 4 % across the load range; bringing it much closer to the PMP9208 reference efficiency – see Fig. 5.23. Even though any actual measured efficiency of the demonstrator will likely be less than calculated, these results suggest that the non-optimal coupled inductor design of *SSCF1* was a key limiting factor to the demonstrator's efficiency. The loss breakdown for the modified *SSCF1* demonstrator in Fig. 5.24 shows reduced snubber loss and an improved balance between core and winding loss.

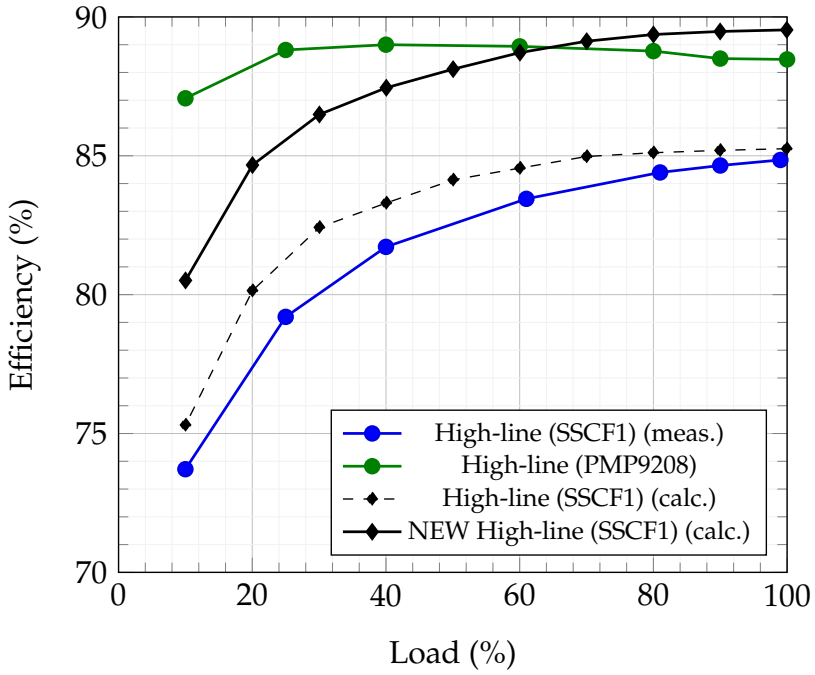


Figure 5.23: Comparison of simulated and measured efficiency of *SSCF1* using original and modified transformer versus PMP9208.

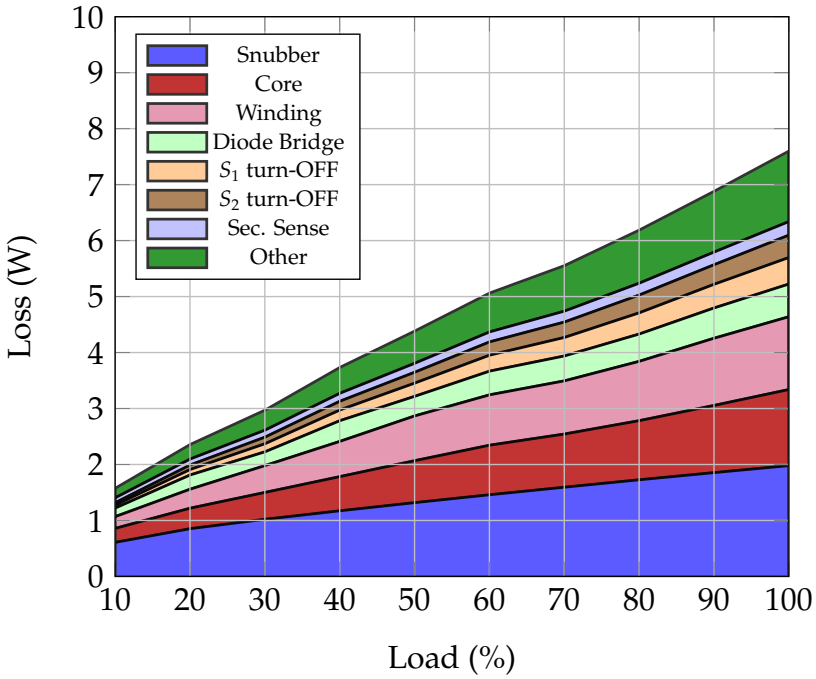


Figure 5.24: Loss breakdown assuming coupled inductor core material 3C96.

5.5.8 Effect of COT Control on Efficiency

The peak currents and switching frequencies resulting from the COT control scheme also increased losses in the coupled inductor and elsewhere in the circuit. The COT scheme requires a fixed ON-time that, at the minimum DC-link voltage, can support the rated load. Subsequently, for all other conditions (especially at low load) the peak inductor currents are "over-sized", leading to larger turn-OFF, core and winding loss throughout steady-state operation – compounding the large loss contributions from the non-optimal coupled inductor. Furthermore, the variable frequency operation arising from COT makes it difficult to optimise the coupled inductor and to select the switching devices (balancing conduction and gate loss). These effects suggest that the secondary side controlled Flyback concept would benefit from a variable ON-time control to achieve constant (or at least reduced) switching frequency.

5.6 Conclusion

This chapter aimed to demonstrate the feasibility of the Secondary Side Controlled Flyback concept in hardware by proving a reliable cross-isolation communication method without opto-isolators, a workable start-up routine, and a steady-state control scheme than can regulate the output voltage.

Firstly, the primary side switch was successfully controlled from the secondary side through the coupled inductor via zero crossings of its drain-source voltage. The proposed primary-side V_{DS} sensing protected the sensing circuitry from the large drain voltage and autonomously distinguished unwanted zero voltage crossings that may occur due to Flyback ringing during wait periods, from genuine primary turn-ON requests from the secondary side. This helps the primary side logic stay simple, independent and reliable. The primary side sensing delay was found to be as low as 34 ns; twice as fast as the typical propagation delay of a quick, modern opto-isolator. However, the time required to discharge parasitic capacitance of a super-junction MOSFET to 0 V limits the application of this technique to sub-MHz applications.

Secondly, the proposed start-up routine was also proven and demonstrates the feasibility of charging the output capacitor using the independent primary side logic before the main secondary side controller wakes up.

Thirdly, steady-state operation with variable frequency ZVS operation has been demonstrated at high- and low-line input voltage with ≈20-250 kHz switching frequency for a 65 W load. The COT control scheme achieved stable output voltage with ripple less than or equal to 1.5 % of mean output voltage and offered natural current limiting in overload conditions. However, the control scheme also adds constraints to the design of any input emi-filter or Flyback coupled inductor since they must be able to handle both the highest frequencies and the large peak currents at low frequency.

All of the main disadvantages of the proposed concept come from the switching frequency range/limit caused by COT, and the large negative current needed for full primary ZVS. The large peak inductor currents resulting from COT also harms efficiency; especially at low-load. To develop a more viable implementation of the Secondary Side Controlled Flyback concept, these issues can be solved by adapting the existing approach with two key changes:

- Variable S_1 ON-time for constant switching frequency.
- Quasi-ZVS for S_1 turn-ON commands.

Chapter 6

Improving the Viability of the Secondary Side Controlled Flyback

6.1 Chapter Outline

By addressing the conclusions drawn from the *SSCF1* prototype in Chapter 5, this chapter presents work intended to improve the viability of the Secondary Side Controlled Flyback concept.

It begins with Section 6.2 whereby a new primary side $V_{DS(S1)}$ sensing approach for quasi-zero-voltage switching (Q-ZVS) operation is presented that maintains the advantages of the previous double-pulse proposal. Section 6.3 then presents a novel lossless, ground-referenced synchronous rectification sensing circuit that provides fast zero-current crossing detection with <45 ns delay. Afterwards, Section 6.4 describes a modified primary side control approach that achieves stable switching frequency across the load range and reduces peak inductor currents. Section 6.5 describes the improved demonstrator hardware and gives a guide for dimensioning inductances and switching times for this new control scheme and for minimizing leakage inductance. Finally, Section 6.6 presents measurements of this demonstrator including:

- The response of the proposed V_{DS} sensing upgrades.
- The proposed control scheme during steady-state and step load changes.
- Measured efficiency for 120 V_{RMS} and 230 V_{RMS} input voltage.
- An analysis of switching frequency stability over the load range.

6.2 Q-ZVS Improvement

Fig. 6.1 shows a sketch of a turn-ON request where a positive voltage crossing is employed to command S_1 to turn-ON, rather than a zero-voltage crossing. This results in Q-ZVS. In comparison to the ZVS technique described in Section 4.4, discharging $C_{OSS(S1)}$ down to a positive voltage requires less negative current from the turn-ON request. At the cost of increased S_1 switching loss, Q-ZVS yields two main benefits for the secondary side controlled Flyback approach:

- Reduced current circulation for turn-ON requests; reducing MOSFET conduction loss, and freeing duty cycle space for positive power transfer.
- Reducing S_2 switching loss, turn-OFF overshoot and secondary side EMI.

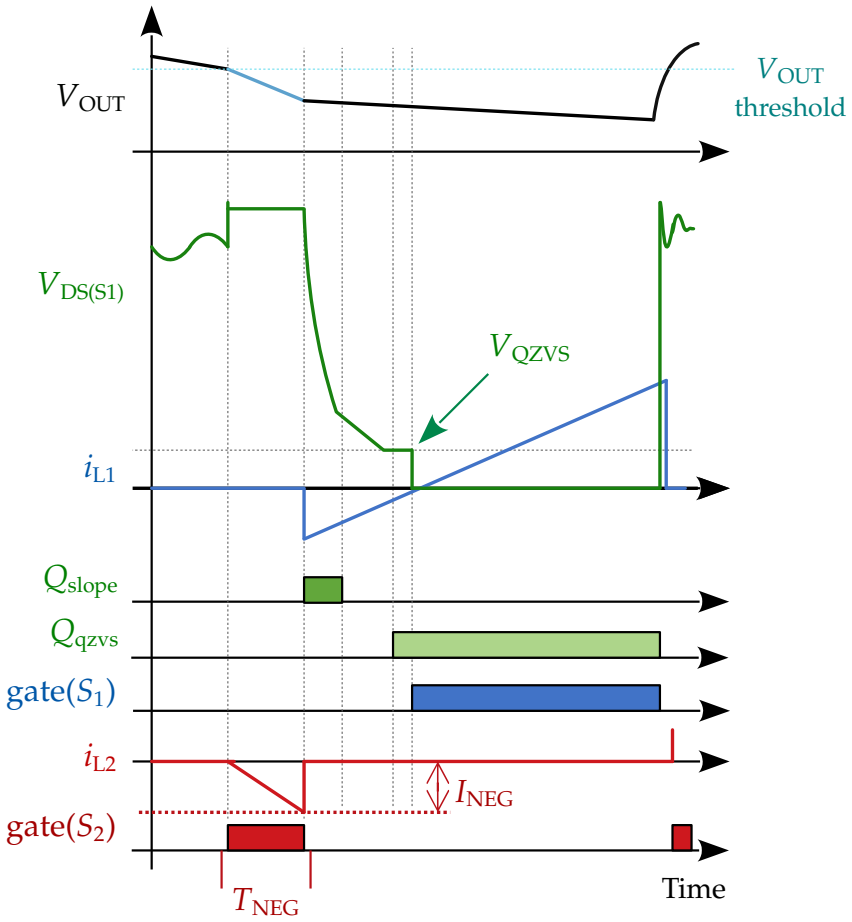


Figure 6.1: Sketch of Q-ZVS turn-ON request, with sense and gate signals.

6.2.1 Calculation of Negative Current Time

The peak secondary side negative current (I_{NEG}) and corresponding S_2 ON-time (T_{NEG}) required to reliably push $V_{DS(S1)}$ down to V_{QZVS} can be calculated with knowledge of the basic Flyback converter parameters and the parasitic output capacitance of S_1. A detailed explanation of this calculation is given in Section 4.4 for the case of forcing zero voltage crossings. The same approach is summarized here, adapted for positive Q-ZVS threshold crossings instead. Firstly, an estimate of the charge required to discharge $C_{OSS(S1)}$ to V_{QZVS} from the initial drain-source voltage ($\widehat{V}_{DS}$) can be found using (6.1):

$$Q_{C_{OSS(S1)}} = \int_{V_{QZVS}}^{\widehat{V}_{DS}} C_{OSS(S1)}(V)\, dV \tag{6.1}$$

Disregarding oscillations, $\widehat{V}_{DS}$ is equal to the DC-link voltage plus the reflected output voltage, as shown in (6.2) where N is the turns-ratio between L_1 and L_2. Secondly, the peak secondary side current required to achieve this discharge of $C_{OSS(S1)}$ can be found using (6.3) along with the corresponding secondary ON-time (T_{NEG}) using (6.4).

$$\widehat{V}_{DS} = V_{DC\text{-}link} + (N\, V_{OUT}) \tag{6.2}$$

$$I_{NEG} = \sqrt{Q_{C_{OSS}} \widehat{V}_{DS}\, N^2 / L_1} \tag{6.3}$$

$$T_{NEG} = I_{NEG} L_2 \,/\, V_{OUT} \tag{6.4}$$

This estimate for T_{NEG} should be treated as a minimum guide-line since leakage inductance, power loss and switching oscillations are not considered. A method of dimensioning the slope-detection circuit to respond adequately to the slope resulting from this negative current pulse is discussed in Section 6.2.2. An essential feature of the Secondary Side Controlled Flyback concept is that $V_{DS(S1)}$ is manipulated by the secondary side controller to control S_1. Stable and reliable sensing of $V_{DS(S1)}$ is therefore critical to the viability of the concept. Furthermore, accurate sensing of S_2 drain current is needed to execute the synchronous rectification feature promised by the secondary side based controller. The drain-connected sensing circuits developed to achieve this are presented here, including a precise and lossless synchronous rectification upgrade. The exact component parameters are given in Tab. 6.5.

6.2.2 Primary Side Drain-Source Voltage Sensing

To enable Q-ZVS based turn-ON requests and maintain the safety of the double-pulse approach from *SSCF1*, the primary side sensing looks for instances of very steep $V_{\mathrm{DS(S1)}}$ slope (indicating a genuine turn-ON request), and when $V_{\mathrm{DS(S1)}}$ has fallen below the Q-ZVS voltage threshold. Two simple, parallel comparator networks are presented each responsible for one such sensing signal.

Fig. 6.2 shows a schematic of the propsoed Q-ZVS threshold sensing circuit. The voltage at the comparator's inverting input is a scaled reflection of $V_{\mathrm{DS(S1)}}$ that depends on the ratio between C_3 and C_4. The large resistors R_6 and R_7 ensure the same scaling in cases of DC $V_{\mathrm{DS(S1)}}$. Once this voltage falls below the fixed reference U_{q}, the signal Q_{qzvs} goes high.

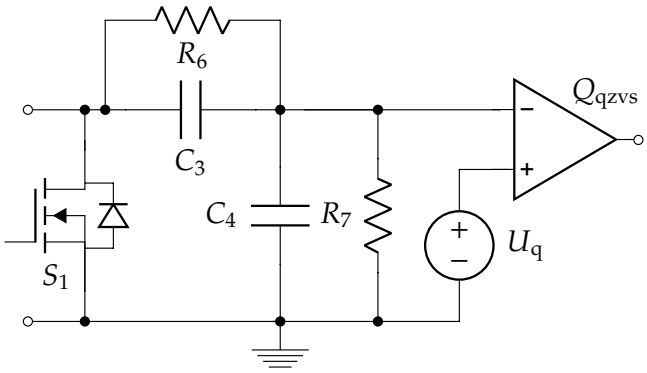


Figure 6.2: Schematic of circuit for detecting quasi-ZVS threshold crossings.

Fig. 6.3 shows the slope sensing circuit. It is comprised of a fixed offset voltage source U_{slope} along with a small RC combination to form a simple high-pass filter.

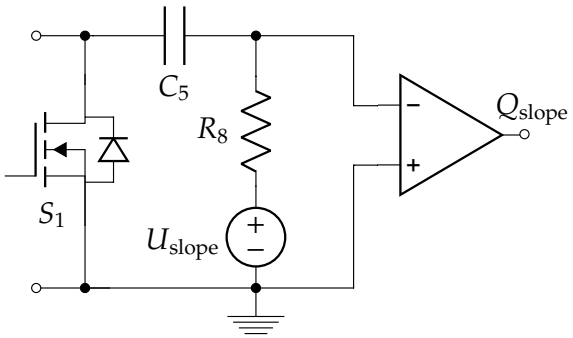


Figure 6.3: Schematic of primary V_{DS} slope sensing circuit.

Q_{slope} goes high whenever the $dV_{DS(S1)}/dt$ caused by a turn-ON request is sufficient to cause negative current through C_5; a derived equation for this is:

$$C_5 \frac{d\,V_{DS(S1)}}{dt} \geqslant \frac{U_{slope}}{R_8} \tag{6.5}$$

Parallel Signals – Double Pulse

As before, the primary side logic looks for a genuine turn-ON request made up of two distinct yet consecutive pulses. However, each component of this double pulse now comes from the two separate comparators shown in Figs. 6.2 and 6.3.

6.3 Synchronous Rectification Improvement

The synchronous rectification sensing must detect the instant the body diode of S_2 begins conducting and the instant inductor current has fallen to 0 A. Fig. 6.4 shows the proposed circuit which comprises a RC filter (R_9 and C_6) and a protective low-power MOSFET (S_{SF}) connected to S_2's drain. The gate of S_{SF} is connected to the supply voltage of Q_{SR} to create a source-follower effect whereby S_{SF} only conducts when $V_{DS(S2)}$ falls below the supply voltage minus S_{SF}'s gate-source threshold voltage.

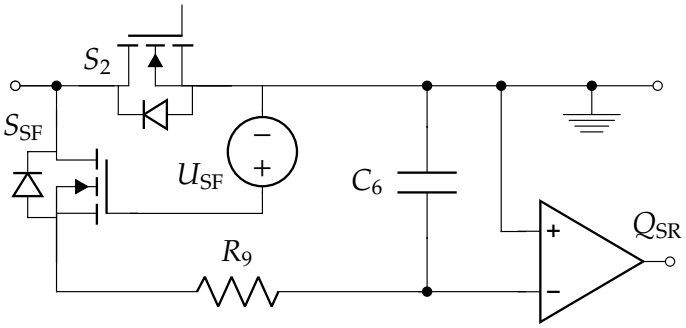


Figure 6.4: Schematic of sensing circuit for synchronous rectification.

S_{SF} protects Q_{SR} from high $V_{DS(S2)}$ with almost zero conduction loss through R_9 as C_6 can be very small. In practical terms, U_{SF} should be the supply voltage for Q_{SR}. With S_{SF} protecting Q_{SR} instead of the parallel diodes, the proposed circuit does not require such a large R_9; reducing sensing delay to tens of nanoseconds. Beneficially, this solution requires only one comparator and uses secondary side ground as the fixed comparator reference; in contrast to existing solutions that require an additional voltage reference and hysteresis op-amp [73].

6.4 Variable-ON-Time Control

6.4.1 Proposed Concept

The novel variable ON-time control (VOT) scheme proposes adding a counter to the primary side logic to measure the frequency of turn-ON requests (f_R). Then, f_R can be compared to a reference frequency (F_{REF}) to infer whether a change in the ON-time (t_{ON}) is necessary to maintain constant switching frequency (f_S). E.g., decreasing t_{ON} when f_R is lower than f_{REF} will cause the synchronous rectification time and t_{wait} to decrease and f_S to rise back towards F_{REF}. This results in a split control structure with the primary side independently helping the secondary side. Fig. 6.5 shows that for a given load, maintaining constant f_S keeps peak inductor currents constant despite DC-link ripple. To see the controller's effort to gradually change the peak inductor current, the more transparent current trace is included and shows the current from the preceding switching period.

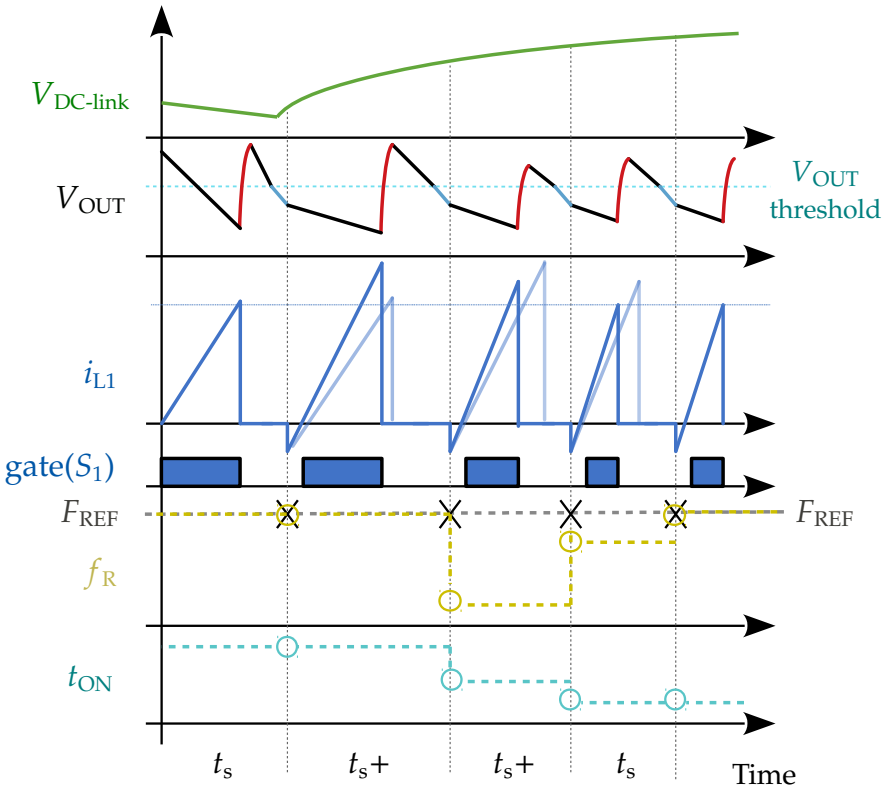


Figure 6.5: VOT control response to rising DC-link voltage.

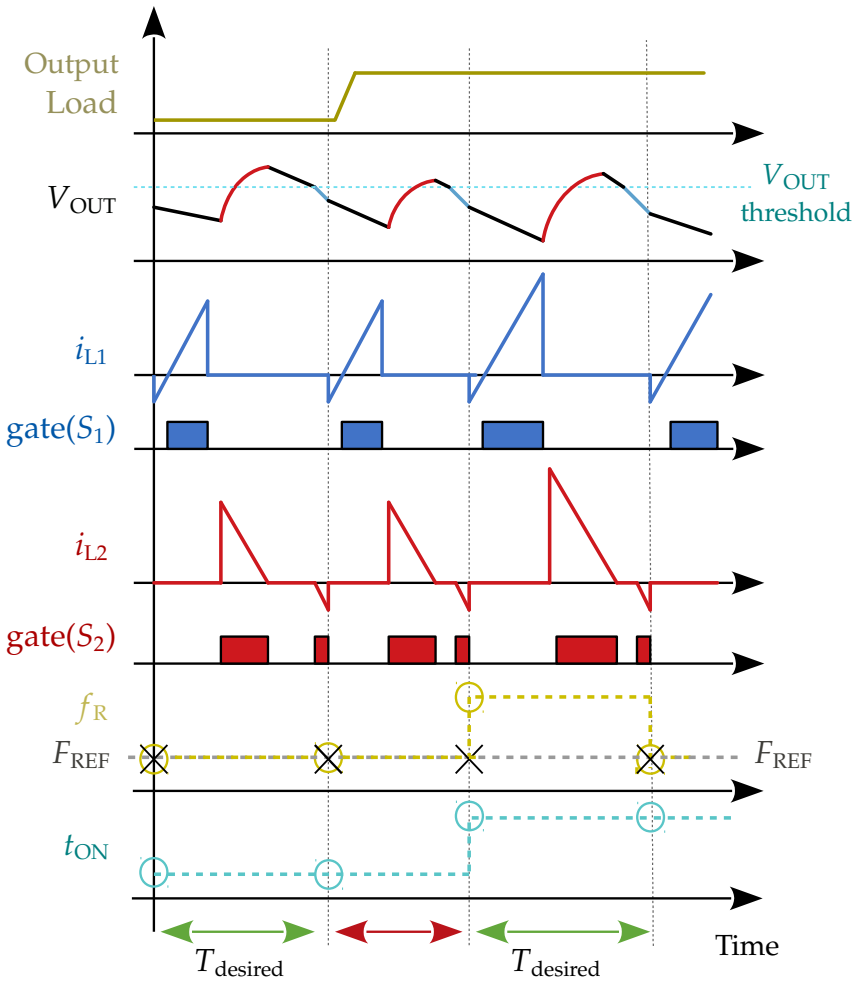


Figure 6.6: Effect of increasing output load on t_{wait} and VOT response.

Modulating t_{ON} for constant f_S also causes power flow to match the output load automatically, without direct feedback. E.g., for an increasing load (Fig. 6.6), t_{wait} will decrease due to the steeper V_{OUT} discharge slope causing f_R to rise. Increasing t_{ON} will simultaneously compensate this frequency rise and supply more power to support the load. While t_{ON} is rising, it is vital that an upper ON-time boundary (T_{UPPER}) exists to avoid core saturation or excessive $V_{DS(S1)}$ overshoot. Importantly, this same T_{UPPER} should align with rated power, circuit parameters and chosen F_{REF} such that at full-load, t_{wait} reduces to almost 0 s. A sketch of this scenario is shown in Fig. 6.7. The minimum T_{UPPER} required to supply sufficient power in this way can be calculated with (6.6) and depends on peak DC-link ripple, desired switching frequency and primary inductance – all of which are defined in Section 6.4.4.

Beneficially, T_{UPPER} also ensures natural output current limiting during overload. In such circumstances, t_{wait} will fall to zero leading to a f_S higher than F_{ref}. However, the primary side will be unable to supply more energy per switching period than the upper ON-time limit T_{UPPER} allows. This will result in falling V_{OUT} and limited output current. This is the same advantage offered by a constant ON-time control, but now the limit is defined by the upper ON-time boundary rather than the fixed ON-time.

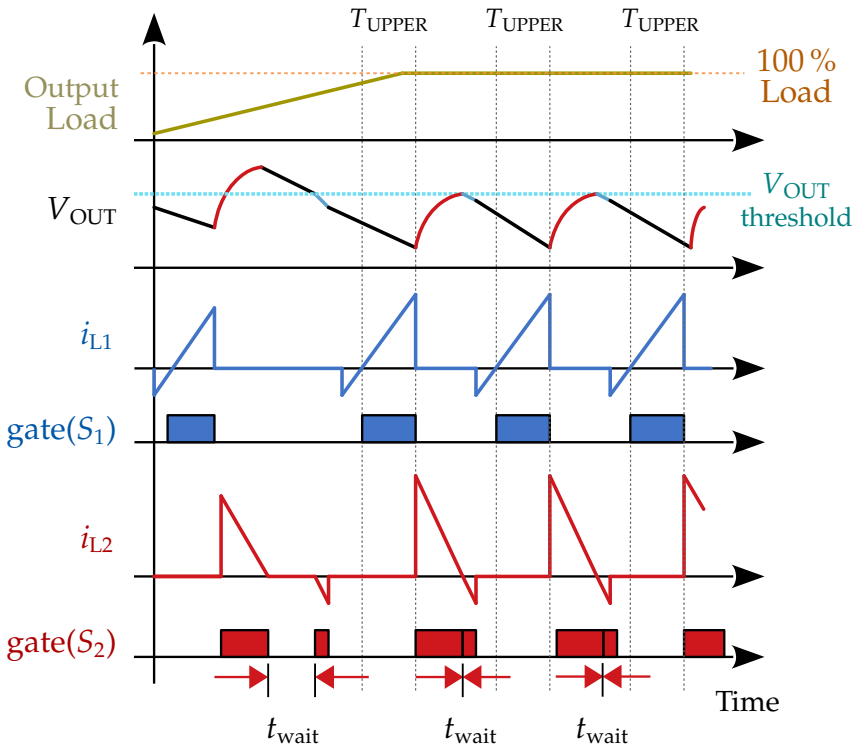


Figure 6.7: Operational effect on t_{wait} for full output load, defined by T_{UPPER}.

$$T_{UPPER} = \sqrt{\frac{2L_1 P_{IN}}{V_{DC\text{-}link(min)}{}^2 f_S}} \tag{6.6}$$

Following the same approach as many existing Flyback converters, a conventional PI control structure was used for the VOT controller's modulation of t_{ON} [74, 75]. The error signal for the control loop came from comparing the measured switching period to the reference switching period.

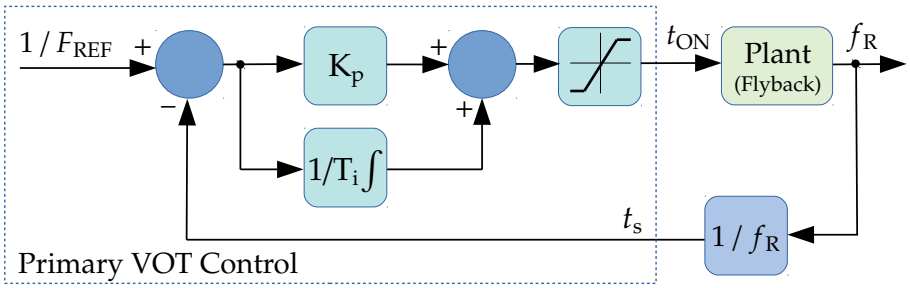


Figure 6.8: Simplified diagram of implemented primary side control loop.

6.4.2 Split Control Structure

The VOT scheme introduces a subtle change to the proposed control structure. The primary side is now not only a slave to the turn-ON requests with a fixed response, it now is responsible for switching frequency regulation. The combination of the independent switching frequency and output voltage regulation naturally results in output power regulation. Fig. 6.9 shows a diagram of the new control structure.

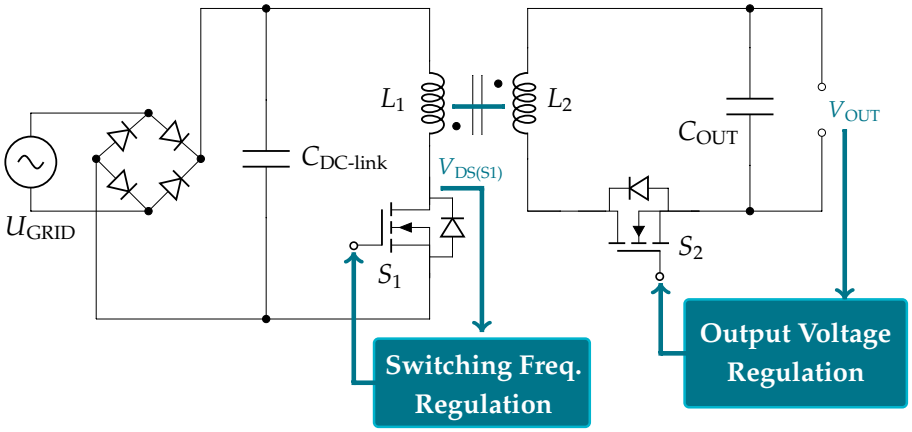


Figure 6.9: Schematic showing split regulation responsibilities resulting from VOT.

6.4.3 Start-Up Routine

The start-up routine shown in Section 5.3.2 is still applicable to the VOT concept. As soon as V_{OUT} is sufficiently high, a turn-ON request is sent back to the primary side putting the primary side into slave mode, whereupon VOT operation begins.

6.4.4 Calculating Inductances for VOT Control

Theoretically, this VOT control scheme is not limited to any specific range of switching frequencies. However, the choice of desired switching frequency has several implications on the overall Flyback circuit parameters, the choice of switching devices and the dimensioning of the novel V_{DS} sensing circuits described in Sections 6.2 and 6.3. In particular, it is critical to dimension the coupled inductor to supply full rated power with the upper primary ON-time limit (T_{UPPER}) at the lowest expected DC-link voltage (minimum point of the input ripple ($V_{DC\text{-}link(min)}$)). This process matches that used to dimension the coupled inductor for COT control, but now the switching frequency is lower and *constant*. For convenience, the same equations are repeated here. By calculating the power transfer in one grid period, it is possible to calculate $V_{DC\text{-}link(min)}$ for a given DC-link capacitance ($C_{DC\text{-}link}$):

$$V_{DC\text{-}link(min)}{}^2 = 2V_{RMS}{}^2 - \frac{P_{OUT}}{C_{DC\text{-}link} f_{grid}} \tag{6.7}$$

where V_{RMS} is the RMS grid input voltage and f_{grid} is the grid frequency in hertz. Next, it is important to estimate the maximum steady-state power required of the converter (P_{IN}). This is the sum of the rated power (P_{rated}), plus the circulating power used to achieve the turn-ON requests (P_{neg}), plus the losses (P_{loss}).

$$P_{neg} = \frac{1}{2} Q_{C_{OSS}} V_{DC\text{-}link(max)} f_S \tag{6.8}$$

$$P_{IN} = P_{rated} + P_{neg} + P_{loss} \tag{6.9}$$

Accurately knowing P_{loss} before constructing the converter is difficult but an estimate can be found using simulation or analytic methods [76–78]. A value for the primary inductance (L_1) can then be found iteratively using:

$$L_1 = \frac{1}{2 f_S A^2 (\sqrt{P_{IN}} + \sqrt{P_{neg}})^2} \tag{6.10}$$

where:

$$A = \frac{1}{V_{DC\text{-}link(min)}} + \frac{1}{N V_{OUT}} \tag{6.11}$$

N should be chosen based on desired V_{OUT}, S_2 voltage rating and loss analysis [79]. It can then be used to calculate the secondary inductance (L_2) corresponding to L_1.

6.5 65 W Demonstrator Hardware – SSCF2

6.5.1 150 kHz Power Board

Measurements of VOT operation were made using the *SSCF2*; an improved demonstrator with improved PCB layout and winding arrangement for low losses and snubber-less operation (see Fig. 6.10 and Tab. 6.1). The *SSCF2* was designed to operate at 150 kHz, converting 120 V_{RMS} / 230 V_{RMS} AC input to 20 V_{DC} with a rated power of 65 W. Overall volume including the EMI-filter is 67.0 cm^3 (4.09 $inch^3$): a 21 % volume reduction from *SSCF1* resulting in a power density of 0.97 W/cm^3 (15.9 $W/inch^3$).

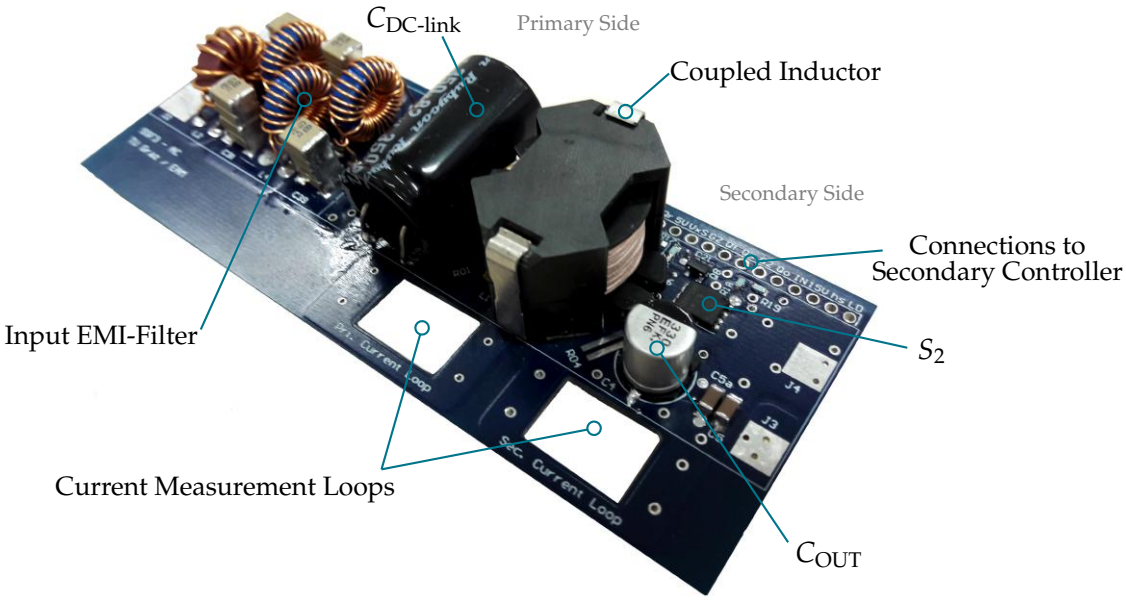


Figure 6.10: *SSCF2* power board. Dimensions: 3.0 cm x 11.4 cm x 2.6 cm.

Table 6.1: Key parameters and components of the *SSCF2* power board.

Input Capacitance	$C_{DC\text{-}link}$	86.4 µF
Output Capacitance	C_{OUT}	330 µF
Primary MOSFET	S_1	CoolMOS C7 125 mΩ ThinPAK 8x8
Secondary MOSFET	S_2	OptiMOS 5 9.8 mΩ (100 V) SuperS08
Gate Driver	-	Infineon Eice 2EDN7524F

6.5.2 Control and Adapter Boards

The SSCF1 demonstrator used a microcontroller based XMC4500 control board for prototyping the secondary side controller. This introduced a synchronous rectification turn-ON delay of up to 81 ns due to signal processing time. To reduce the S_2 body diode conduction time due to this delay the secondary control was instead executed with an FPGA based prototyping board – where the signal processing delay is equal to the clock cycle.

For prototyping purposes, both primary and secondary side regulation and gate signal generation were executed using an external FPGA demonstrator board – the Lattice iCEblink40-HX1K. The opto-isolator between the *SSCF2* power board and primary-side control board was used for safe initial sensing tests but was later removed. All measurements presented herein were taken without such opto-isolators to minimize signal propagation delay.

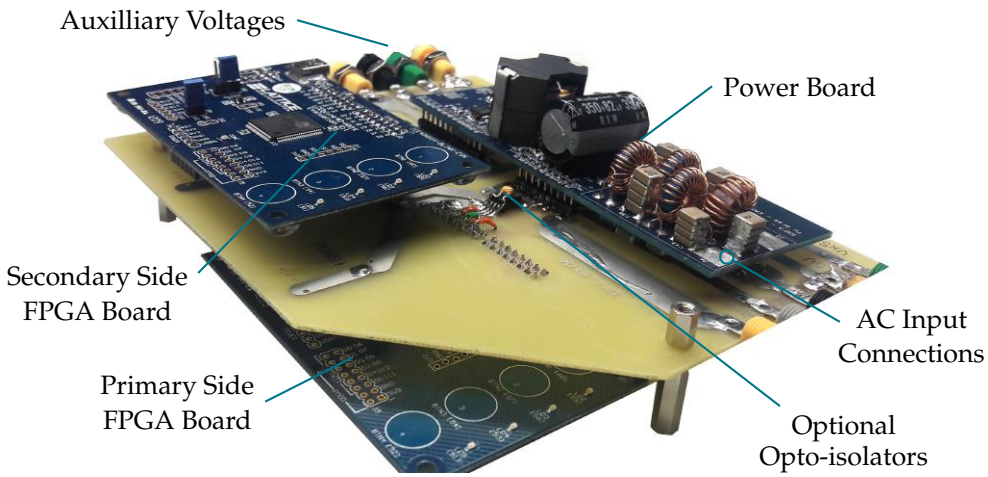


Figure 6.11: Adapter board connecting control boards to *SSCF2* power board.

Fig. 6.11 shows the complete prototyping set-up including an adapter board for short signal connections between power and control boards.

To maintain isolation, a separate control board was used for both primary and secondary side – with the primary side responsible for switching frequency regulation via VOT control, and the secondary side responsible for output voltage regulation via turn-ON requests. The iCE40-HX1K was operated with a 33 MHz clock giving a period of ≈ 33 ns.

6.5.3 Coupled Inductor Design

The chosen winding arrangement and core material should avoid core saturation while balancing core and winding losses in order to optimize size and loss [80]. For a meaningful comparison to the *SSCF1* COT demonstrator, the same turns-ratio of 5 was chosen for the *SSCF2* VOT demonstrator. Furthermore, a desired switching frequency of 150 kHz was chosen because it sits in the middle of the frequency range of the *SSCF1* COT demonstrator and within the (upper) range of existing power adapters.

Tab. 6.2 lists the inductances calculated using the methods described in Section 6.4.4 as well as the components used.

Table 6.2: Key parameters of new coupled inductor.

Parameter	Symbol	Value
Turns Ratio	N	5 (20:4)
Primary Inductance	L_1	107 µH
Secondary Inductance	L_2	4.3 µH
Winding Arrangement	inn : mid : out	5 : 4 : 15
Winding Type	pri : sec : pri	litz : foil : litz
Core Shape/Material	–	RM10i / 3C95
Air gap	l_g	430 µm
Peak Inductor Currents	$\hat{I}_{L1} : \hat{I}_{L2}$	3.4 A : 17 A
Measured Coupling Factor	k	0.994
Peak Pri. V_{DS} Overshoot	$\hat{V}_{DS(S1)}$	579.2 V

This arrangement offered very high core window utilization and the primary and secondary windings were measured to have a coupling factor of 0.994 (measured at 100 kHz) Conveniently, the corresponding primary leakage inductance was found to be low enough to avoid incorporating a snubber altogether: the maximum primary ON-time at peak DC-link voltage with 230 V_{RMS} input voltage ($\approx$ 325 V) gave a peak $V_{DS_{(S1)}}$ overshoot of 579.2 V. This is a significant improvement over the COT demonstrator as snubber loss was the largest loss source; 2.0 W at full load (3.1 %).

6.5.4 EMI-Filter for VOT

The COT control scheme resulted in large inductor currents at a wide range of switching frequencies – see Fig. 5.14. This mandated a physically large input EMI-filter [65] to satisfy the Class B SMPS noise requirements [63].

Tab. 6.3 compares the filter volume for COT and VOT demonstrators, both designed for a rated output of 65W/20V. Although in-rush currents are relatively large for both control schemes due to the operation Flyback topology, VOT only incurs maximum peak inductor current at maximum load (in contrast to COT where peak inductor current was independent from the load and varied only with DC-link ripple). VOT permits a physically smaller filter design as the damping can be focussed on a much narrower frequency range.

Table 6.3: Input EMI-filter volumes for COT (*SSCF1*) and VOT (*SSCF2*).

	Switching Frequency	Boxed Volume
COT Control	15 kHz - 275 kHz	1.8 in^3 / 29.5 cm^3
VOT Control	≈ 150 kHz	**0.81 in^3 / 13.3 cm^3**

Tab. 6.4 lists the specifications of the VOT input filter along with the components used. The VOT emi-filter can be seen on the SSCF2 power board, annotated in Fig. 6.10. The inductances for both differential- and common-mode (CM) filters were evenly split between both input lines for impedance balancing [62]. Furthermore, the differential-mode (DM) section was divided into three stages to reduce the overall volume [64] and maximize power density.

Table 6.4: emi-filter components and parameters.

Parameter	Value (no.)	(no.) Core / Capacitor
CM Inductance	320 µH (x2)	(1x) Vacuumschmelze W914
CM Capacitance	9.9 nF (x2)	(8x) Murata GA355QR7GF222
DM Inductance	22.5 µH (x6)	(3x) Power Magnetics HF044160-2
DM Capacitance	600 nF (x3)	(30x) Murata GA355ER7GB473

The final boxed emi-filter volume was 18.3 cm^3 (1.17 $inch^3$) – a 52 % reduction from the filter volume required for COT for SSCF1 (40.3 cm^3/2.46 $inch^3$).

6.5.5 Drain-Source Voltage Sensing

The drain-source voltage sensing remains a critical part of the Secondary Side Flyback concept. Tab. 6.5 lists the components and voltage reference values used for the three sensing circuits described in Section 6.2 and 6.3 for the *SSCF2*. Many of the passive component values were determined empirically.

Table 6.5: Implemented parameters for *SSCF2* drain-source voltage sensing.

Component	Symbol	Value	Package
Comparator	-	ADCMP600	SO-23-5
MOSFET	S_{SF}	IRLML0100	SO-23
Voltage Reference	U_q	380 mV	-
Voltage Reference	U_{slope}	180 mV	-
Resistor	R_6	3.0 MΩ	1206
Resistor	R_7	30 kΩ	0603
Resistor	R_8	30 Ω	0603
Resistor	R_9	240 Ω	0603
Capacitor	C_3, C_5	2.2 pF (450 V)	1206
Capacitor	C_4	220 pF (10 V)	0603
Capacitor	C_6	39 pF (10 V)	0603

For the *SSCF2*, the same output voltage sensing circuit and parameters were repurposed from the *SSCF1* demonstrator (shown in Fig. 5.4). For convenience, Tab. 6.6 lists the components used.

Table 6.6: Key components for *SSCF2* V_{OUT} sensing.

Resistive Divider	R_4	60 kΩ
Resistive Divider	R_5	15 kΩ
Comparator	-	ADCMP600
DC Voltage Source	U_{REF}	4.0 V

6.6 SSCF2 V_{DS} Sensing Measurements

6.6.1 Primary Side

Fig. 6.12 shows the primary side comparator outputs in context with *SSCF2* secondary side inductor current i_{L2} and primary drain source voltage $V_{DS(S1)}$. After the turn-ON request ends at $t = 0.5\,\mu s$, $V_{DS(S1)}$ falls rapidly (causing Q_{slope} to rise) to Q-ZVS threshold triggering Q_{qzvs} and leading to S_1 turn ON at $\approx 25\,V$ for a quasi-zero-voltage turn-ON. The turn-ON instant can be seen where $V_{DS(S1)}$ suddenly drops to 0 V from a positive valley, after the "double-pulse" comparator signals.

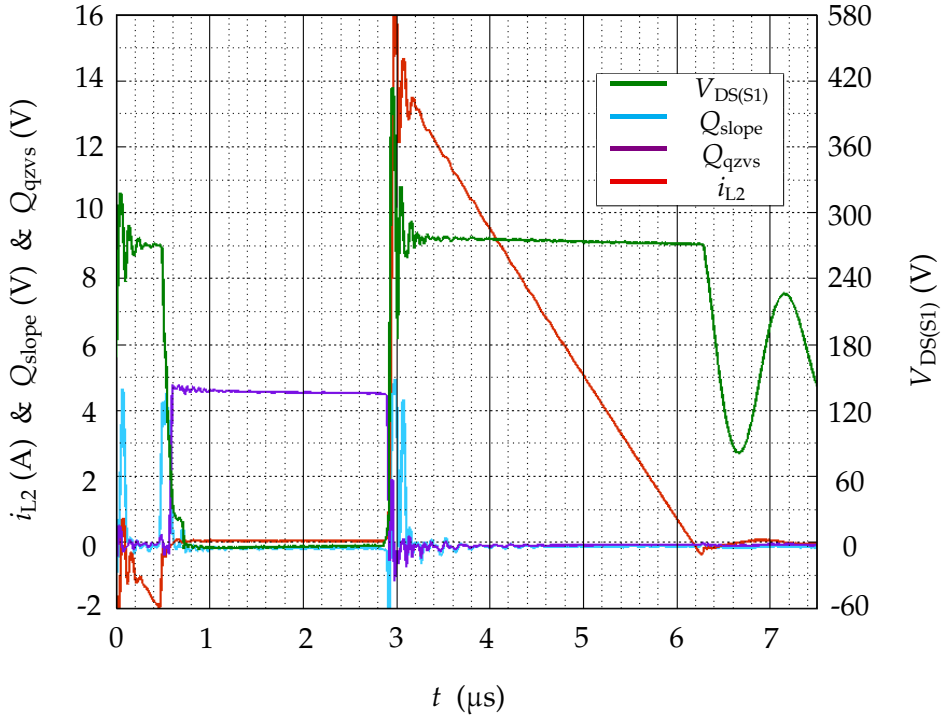


Figure 6.12: Measured response of primary *SSCF2* $V_{DS(S1)}$ sensing circuits.

The frequency of $V_{DS(S1)}$ turn-OFF oscillations are high enough to trigger Q_{slope}, but the Flyback ringing after synchronous rectification is not (indicating good dimensioning of R_1, C_1 and U_{slope}). A short blanking time should be included on the primary logic after S_1 turn-OFF in case oscillations exceed the Q-ZVS threshold. Fig. 6.13 shows a zoom of the turn-ON request being delivered. It can be seen that Q_{slope} naturally falls once the $V_{DS(S1)}$ slope begins flattening at $t = 0.76\,\mu s$.

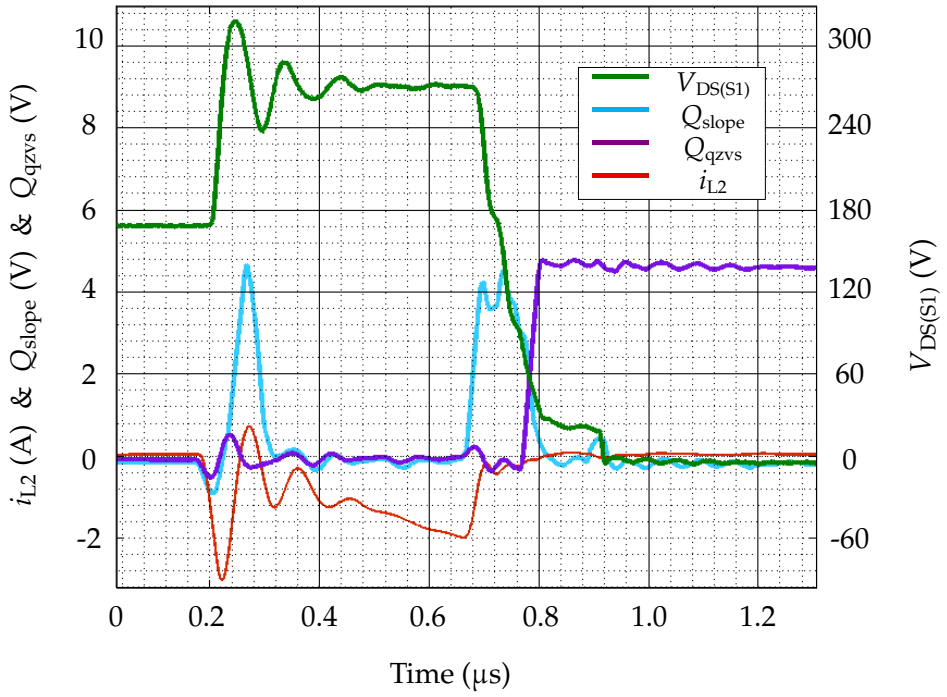


Figure 6.13: Zoomed view of turn-ON request with *SSCF2* $V_{DS(S1)}$ sensing signals.

6.6.2 Secondary Side

The novel application of the source-follower MOSFET to block V_{OUT} (and high $V_{DS(S2)}$) was proven to work and offer precise detection of positive S_2 drain current; helping reduce unnecessary negative current from circulating back to the input after synchronous rectification.

Fig. 6.14 shows a measurement of the output of the proposed synchronous rectification sensing circuit, shown in Fig. 6.4, during steady-state operation with a series of switching periods each with different inductor current. Q_{SR} indicates positive i_{L2} with the rising-edge delay measured to be 70 ns and the falling edge measured to occur consistently 45 ns before the measured zero current crossing.

Fig. 6.15 shows a zoomed plot of one such synchronous rectification period. The small rising edge delay will incur some additional body-diode conduction loss before the switch turns-ON due to the high current. However, the slightly premature falling edge is especially helpful for the Secondary Side Controlled Flyback concept: it prevents unwanted negative current circulating back after synchronous rectification by allowing the controller and driver to process the signal and turn OFF S_2 shortly before the actual zero crossing.

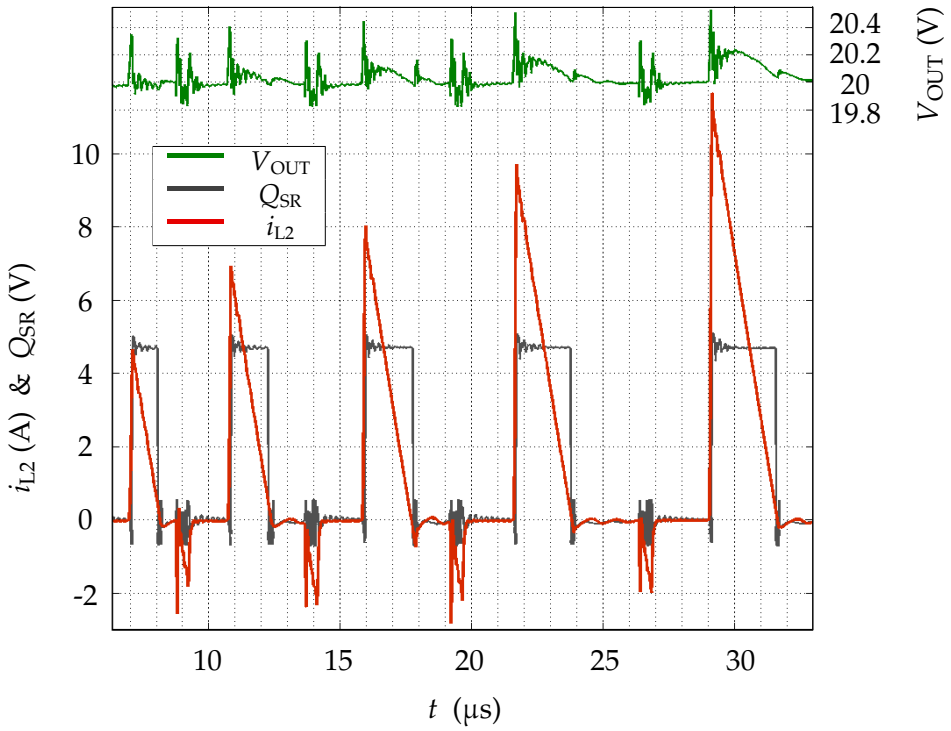


Figure 6.14: *SSCF2* synchronous rectification sense response for various currents.

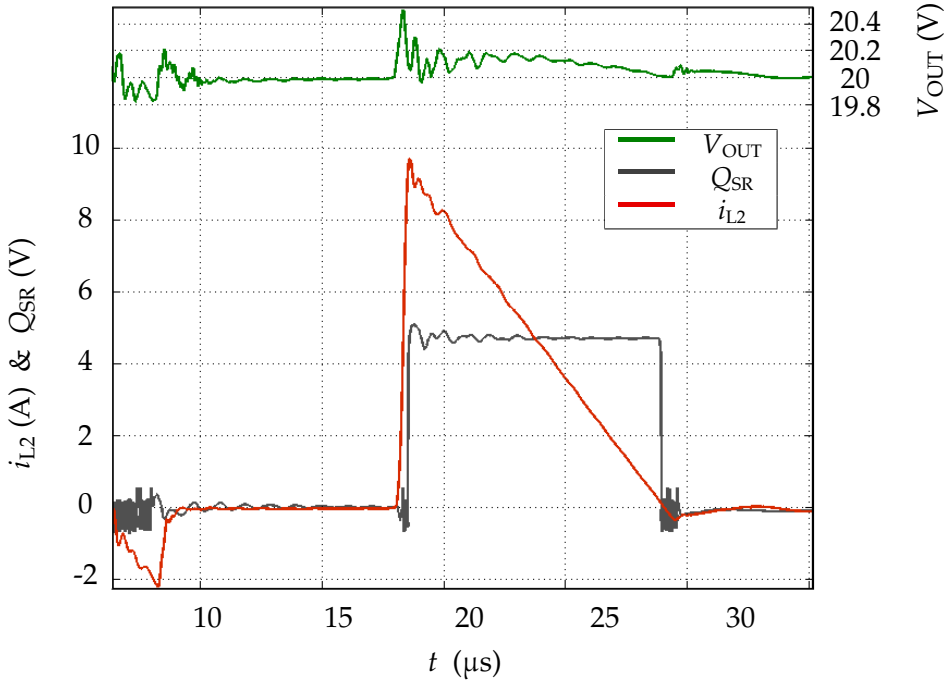


Figure 6.15: Zoom of measured *SSCF2* synchronous rectification sense response.

6.7 VOT Measurements

This section summarizes selected measurements of the 150 kHz VOT control taken with the *SSCF2* demonstrator using the settings listed in Tab. 6.7. These include:

- Steady-state operation with constant output load.
- Control response to load jumps.
- Natural current limiting in overload conditions.

Table 6.7: Implemented control settings for *SSCF2* VOT operation.

RMS Input Voltage		230 V	120 V
Secondary negative current ON-time	T_{NEG}	530 ns	360 ns
Resulting Current (V_{OUT} = 20 V)	I_{NEG}	−2.5 A	−1.7 A
Primary ON-time upper limit	T_{UPPER}	1.20 µs	2.35 µs

6.7.1 Steady State Operation

Fig. 6.16 shows *SSCF2* steady-state operation with a Q-ZVS threshold of 35 V implemented. Such Q-ZVS turn-ON requests required secondary current of −2.5 A; half the amplitude required for the full ZVS approach employed with the *SSCF1* COT demonstrator. Roughly consistent peak i_{L2} and t_{wait} indicates energy transfer matches the load. However, the peak negative currents do vary slightly despite constant V_{OUT}. This occurs because the large Flyback ringing is of very high frequency and not in sync with the FPGA clock – leading to varying S_2 turn-ON voltage. This leads to small period-to-period variations in the switching frequency since a slightly smaller negative current will result in slightly higher primary peak current for the same ON-time. The effect of this over an entire AC grid period can be seen in Fig. 6.17. Despite the small variation, the mean f_S remains stable and close to the 150 kHz set-point; compensating the DC-link voltage ripple. In summary, for a constant load, adapting primary t_{ON} for fixed frequency results in stable peak i_{L1}, i_{L2} and average f_S throughout the entire AC period, while t_{ON} and secondary t_{wait} vary in order to compensate DC-link ripple.

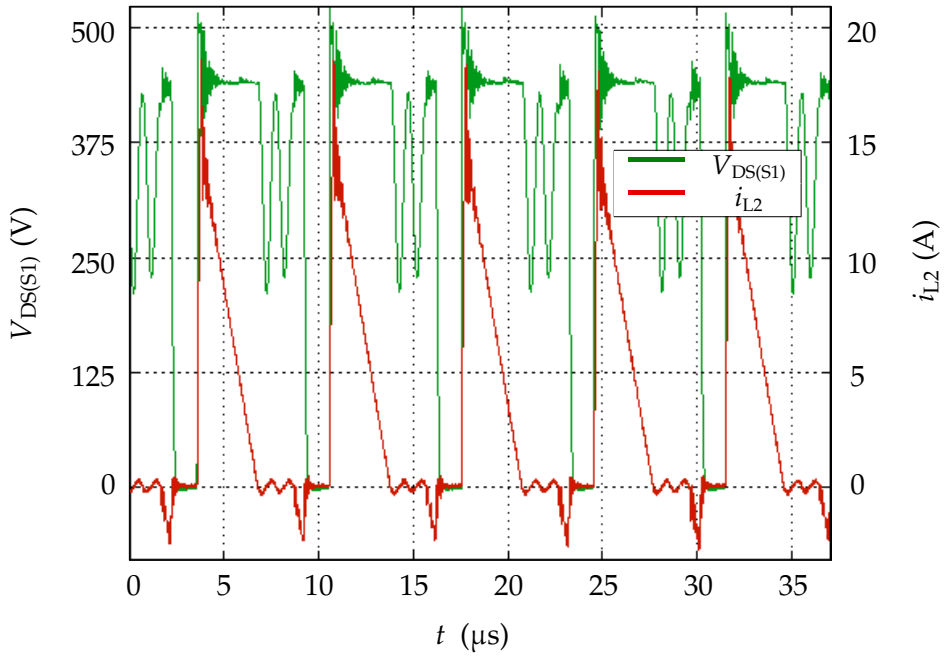


Figure 6.16: Zoom of *SSCF2* steady state VOT operation.

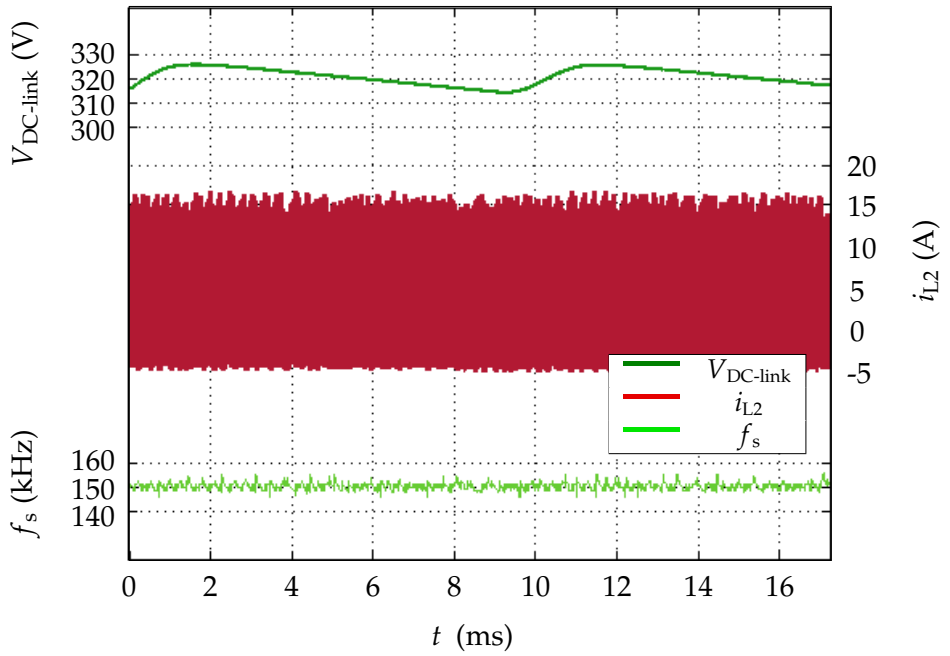


Figure 6.17: *SSCF2* steady-state VOT operation. Input: 230 V_{RMS}. Output: 20 V, 36 W.

Fig. 6.18 shows how the VOT control continuously adjusts the t_{ON} after any detected frequency change. After the first two switching periods, detected f_s drifts away from the 150 kHz set-point and the ON-time is trying to compensate with small adjustments. However, after the third turn-ON request a sharp frequency rise from 155 kHz to 174 kHz is detected. In response, the primary t_{ON} rapidly increases in order to energize the primary inductance with larger i_{L1} and to bring f_S back towards the 150 kHz set-point. Despite the relatively large temporary deviation in switching frequency, the quick adjustment in t_{ON} resulted in negligible deviation in output voltage ripple.

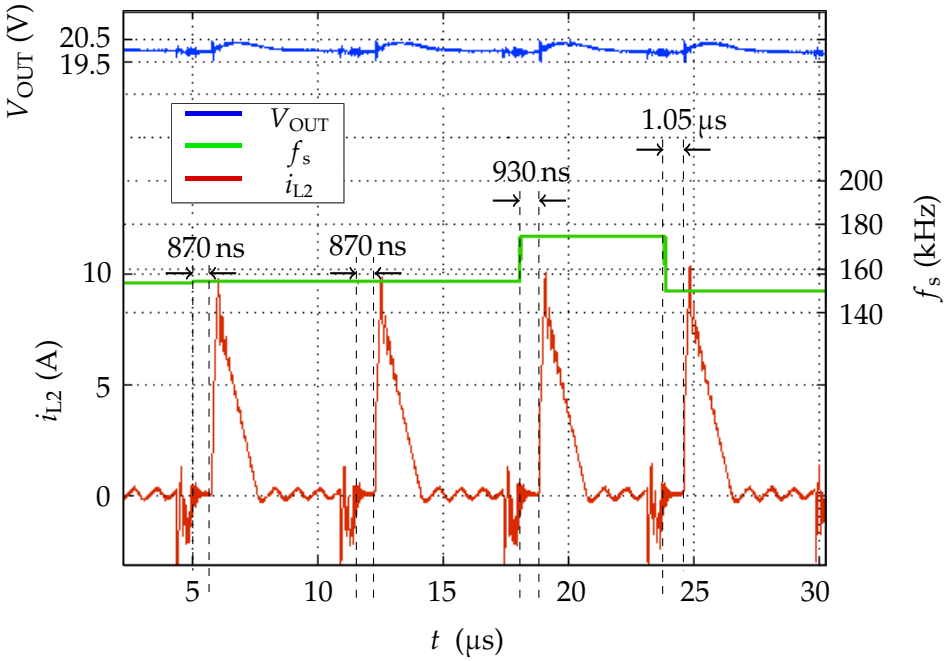


Figure 6.18: Reaction of VOT in case of frequency deviation.

6.7.2 Load Jumps

In Fig. 6.19, the *SSCF2* demonstrator undergoes an output load change from 30 % to 100 % load. When the new high load is applied to the adapter, (at around 90 µs) C_{OUT} discharges faster than before and instantaneous switching frequency surges to 227 kHz. During this transient period, the ON-time and peak inductor current begin rising to match the higher output load until the detected frequency drops back below the set point frequency of 150 kHz.

After 40 µs of transient, the system returns to the desired frequency and average output voltage as defined before – however the larger output ripple caused by the larger inductor currents can be observed for the higher load. A small drop in V_{OUT} of 590 mV can be seen during the transient due to the large, sudden load change.

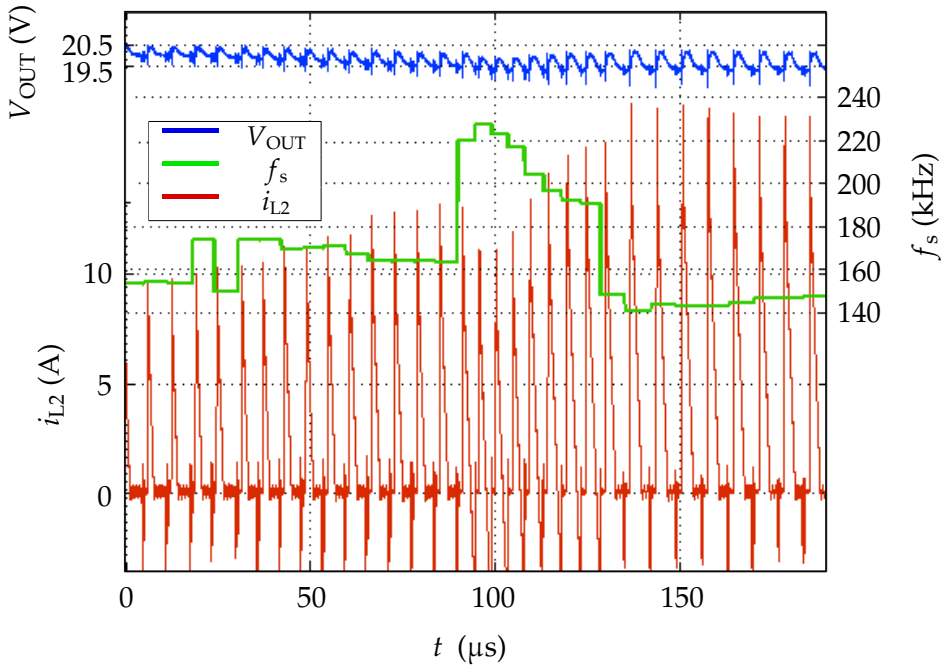


Figure 6.19: VOT reaction to jump from 30 % to 100 % load.

Fig. 6.20 shows the behaviour during a jump from higher to lower load; from 60 % to 30 %. Primary ON-time, switching frequency and secondary inductor current are plotted and the load change occurs at the time 0 µs.

Before the load change, the peak secondary inductor current is stable at ≈ 15 A while the primary ON-time is 900 ns and switching frequency is close to 150 kHz. The load jump immediately causes a significantly larger t_{wait} while V_{OUT} falls below the threshold and until the subsequent turn-ON request is initiated. The instantaneous switching frequency drops to 55 kHz and the primary ON-time drops as soon as this low frequency is detected. The primary logic then adapts to the new load and after 30 µs the ON-time settles to around 590 ns, causing peak secondary inductor current to fall to 10 A, power flow to match the reduced output load, and the switching frequency to return back to 150 kHz.

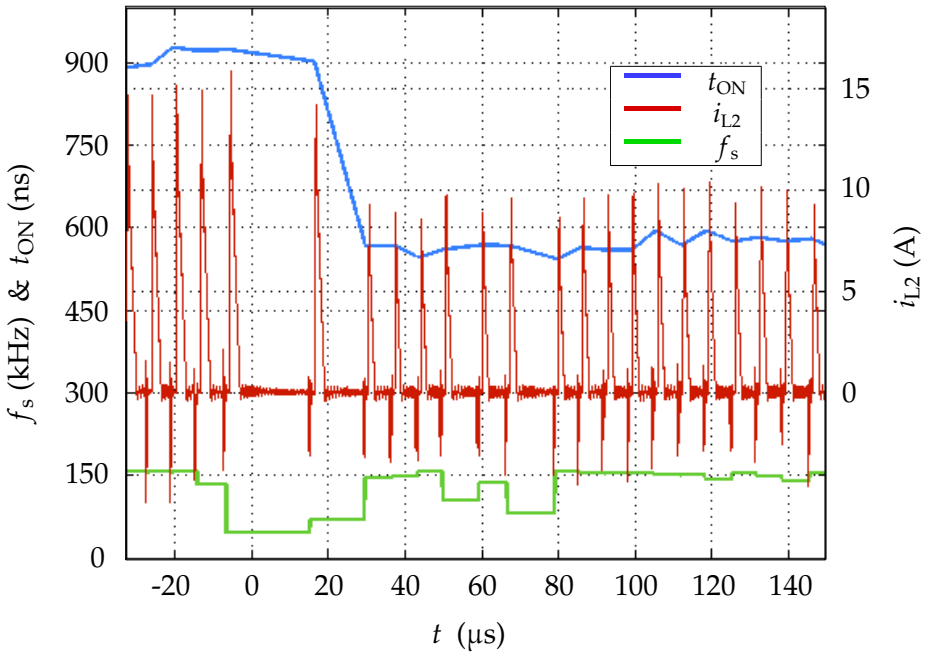


Figure 6.20: VOT reaction to jump from 60 % to 30 % load.

6.7.3 Natural Current Limiting

Fig. 6.21 shows the system's inherent overload current limiting. The *SSCF2* demonstrator is operating at 75 % load until the time labelled 160 µs, when the load increases first to 100 % load, and then beyond rated power to 110 % load at time 230 µs. The primary ON-time rises until the T_{UPPER} is reached. After this, V_{OUT} drops and the output current hits its natural limit.

Subsequently, t_{wait} reduces to zero and the switching frequency stays beyond the set-point at a maximum value dependant on the upper ON-time boundary and output load. Although the output current remains constant at the natural limit, once V_{OUT} no longer rises above the desired threshold after primary turn-OFF, the subsequent turn-ON request is generated immediately after synchronous rectification ends. Fig. 6.22 shows the transition into this zero wait time operation for the same load change. This is the equivalent scenario to that presented in Fig. 5.13 for COT control, but now upper ON-time boundary T_{UPPER} limits maximum power transfer, rather than the fixed ON-time. If the load were to return to rated power or below, the VOT control would quickly restore the rated V_{OUT} and f_S.

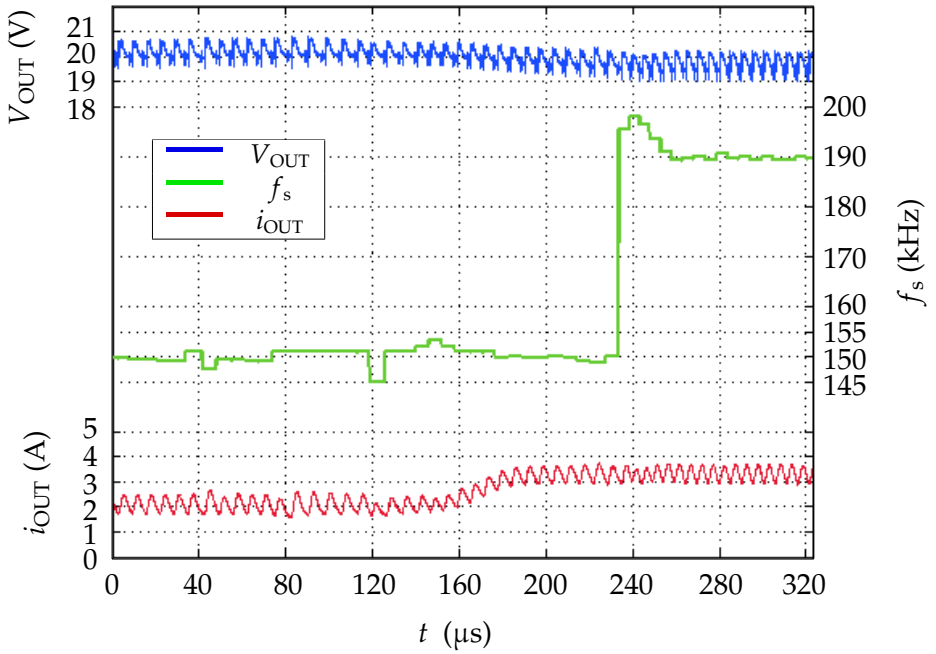


Figure 6.21: Measurement of natural output current limiting at 110 % load.

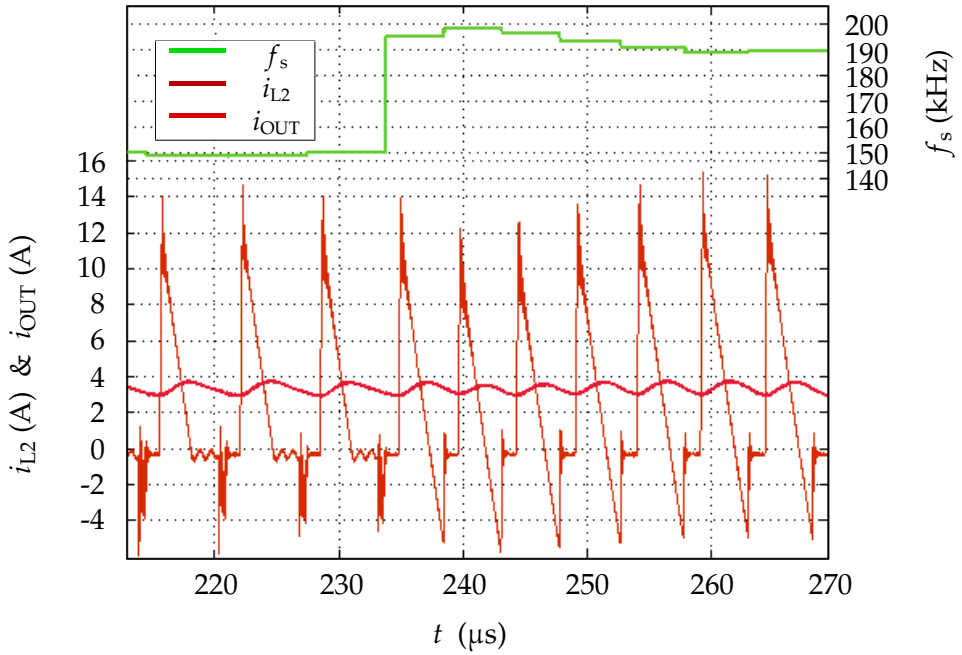


Figure 6.22: Zoomed measurement of natural output current limiting at 110 % load.

6.8 Efficiency, Losses and Frequency Variation

6.8.1 Measurements

Efficiency was again measured using a Norma N5000 [69]. Fig. 6.23 shows measurements of *SSCF2* compared to the 65 W COT demonstrator *SSCF1* in Section 5.4. The *SSCF2* demonstrator shows better high-load efficiency due to:

- Lower switching frequency at high load due to VOT.
- Interleaved windings allowing a snubber-less design.
- Lossless synchronous rectification sensing.
- Reduced circulating current and loss associated with Q-ZVS turn-ON requests compared to full ZVS requests.

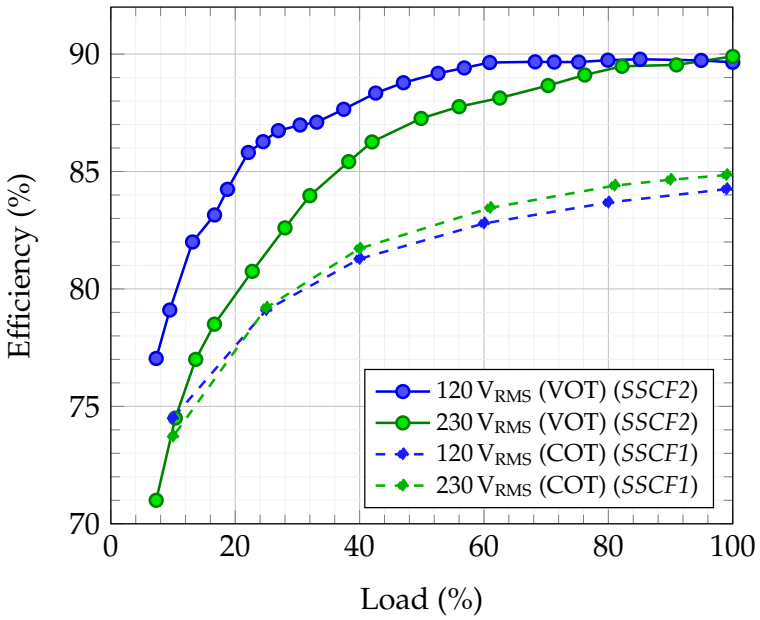


Figure 6.23: Measured efficiency of demonstrator using COT and VOT controls.

At low-load however, despite smaller inductor currents, VOT efficiency drops below the COT demonstrator due to higher low-load switching and turn-ON request frequency necessitated by the fixed frequency operation.

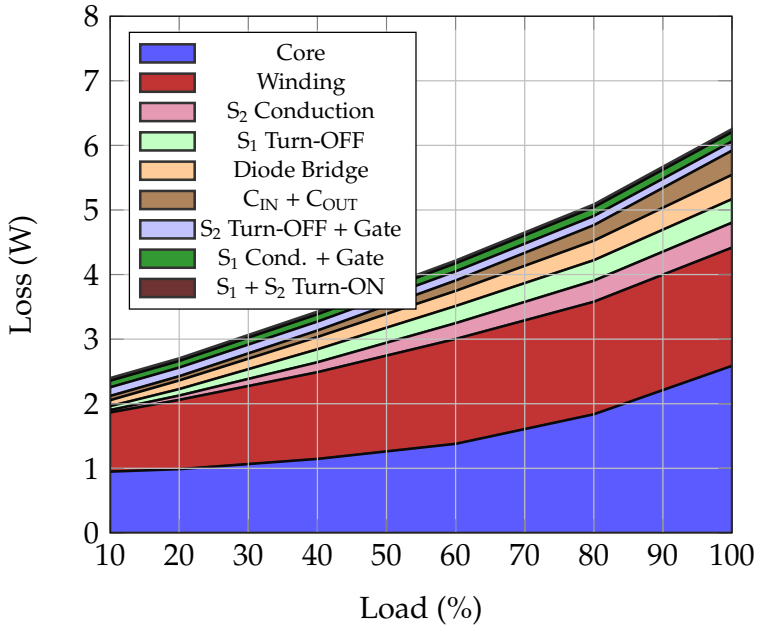


Figure 6.24: Overall loss breakdown for *SSCF2* with 230 V_{RMS} input and VOT operation (calculated).

The individual loss contributions were calculated using the appropriate analytic methods referenced in [70] and are shown in Fig. 6.24. In contrast to COT control where switching frequency drops with load (see Fig. 5.14), VOT forces switching frequency to remain constant causing losses associated with turn-ON requests to remain constant for all loads. These include the switching, gate, and conduction loss due to negative current pulses, and the energy circulated for Q-ZVS resulting in larger inductor currents that inflate winding, core and turn-OFF loss. This low-load efficiency drop is thus particularly noticeable for 230 V_{RMS} input where peak negative current for turn-ON requests is higher.

6.8.2 Switching Frequency Variation

Lastly, to assess the effectiveness of the VOT scheme, it is important to check how well it regulates the switching frequency. Fig. 6.25 is a plot of mean switching frequency (calculated over one 50 Hz grid period) versus load, along with the range of primary ON-times that occurred at each load point. Generally, the primary ON-time moves with the output load and, for a given load, the primary ON-time varies with the DC-link ripple.

Since DC-link ripple increases with load, the range of ON-times is wider at higher loads. The mean switching frequency was measured to stay within 149.1 kHz and 151.3 kHz across the load range.

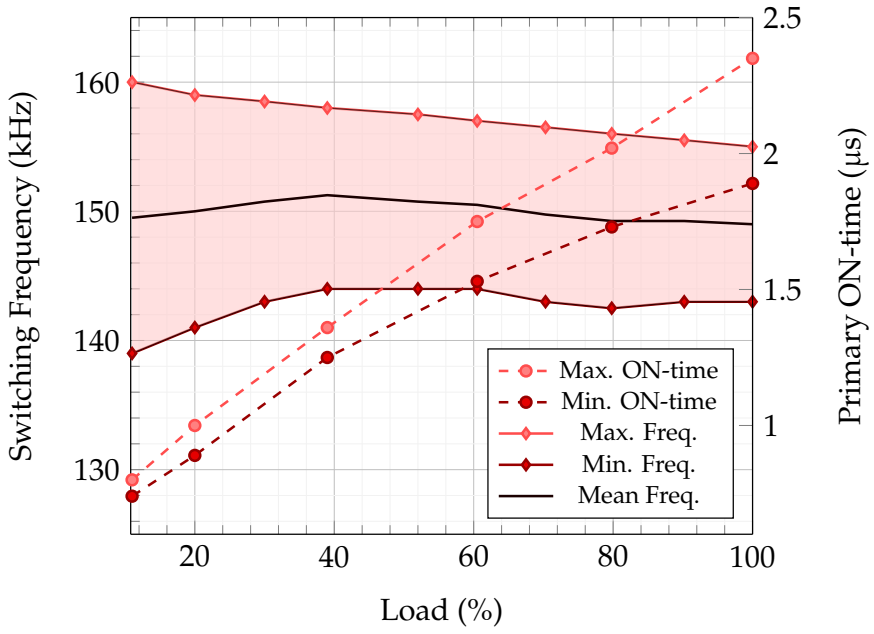


Figure 6.25: Minimum and maximum observed instantaneous f_S and t_{ON} for *SSCF2* with 120 V_{RMS} input voltage.

However, the range of instantaneous switching frequencies (occurring for one or two periods) has a wider distribution – ±6 kHz at full load, to ±10 kHz at 10 % load. Due to the nature of VOT, there will always be a range of instantaneous frequencies because the ON-time is corrected after any detected frequency drift. However, this effect is exacerbated:

- at low-load, by the relatively large 33 ns FPGA clock period – 10 % of the minimum t_{ON} for 230 V_{RMS} input,
- at high-load, by the varying S_2 turn-ON voltages due to ringing. The inductor current oscillations resulting from this hard turn-ON can either compliment or oppose the build up of negative current; causing non-static negative and peak inductor currents and frequency variation. This varying peak negative and positive current also negatively effects efficiency.

6.9 Conclusions

Based on the conclusions from Chapter 5, this chapter aimed to improve the viability of the Secondary Side Controller Flyback concept by boosting converter efficiency with a new control scheme and a modified turn-ON request approach, as well as showing system response to output load jumps. To do this, several novel sensing circuits were developed and tested using an improved prototype: the *SSCF2*.

New drain-source voltage sensing circuits were developed for both S_1 and S_2. The primary side sensing approach was able to deliver fast Q-ZVS sensing successfully while maintaining the double pulse feature from *SSCF1* to filter genuine turn-ON requests from Flyback ringing. The upgraded secondary side sensing circuit exhibited excellent synchronous rectification sensing; reliably indicating positive drain current with $< 70\,\text{ns}$ delay. It also provided accurate zero current crossing detection to avoid unwanted negative current returning to the primary side.

The VOT concept was demonstrated in combination with these sensing improvements. Various load jump measurements show the simple primary side logic's capability to autonomously match power transfer to the output load just by maintaining stable switching frequency; no direct feedback is required from the output to the primary side. VOT control was shown to effectively compensate DC-link voltage ripple resulting in constant peak inductor currents for any given load, with smaller negative current requests. As such, it exhibited improved efficiency over *SSCF1* of up to 89.9 % – putting the Secondary Side Control Concept into the range of efficiency expected of 65 W Flyback adapters (see Fig. 3.6).

Upon closer inspection however, frequency stability was found to be adversely affected by varying S_2 turn-ON voltages during Flyback ringing. This, combined with the constant negative current time for turn-ON requests, resulted in unnecessary energy circulation due to non-constant negative currents. Furthermore, low-load efficiency suffered due to the fixed frequency operation and subsequent constant losses associated with circulating energy for turn-ON requests.

To help expand the capability of the the Secondary Side Controlled Flyback concept and address the issues rising from varying S_2 turn-ON voltage and poor low-load efficiency, two modifications will be investigated:

- Using a valley or level detection to only initiate turn-ON requests for low drain-source voltages.
- Amend the VOT control scheme to drop the switching frequency at low-loads.

Chapter 7

Expanding the Capability of the Secondary Side Controlled Flyback

7.1 Chapter Outline

To explore the potential of the Secondary Side Controlled Flyback concept, this chapter proposes and presents measurements of three novel upgrades to the *SSCF2* demonstrator from Chapter 6. Two of which address issues uncovered in previous chapters while the remaining concept introduces a new application of the Secondary Side Controlled Flyback.

To address the issue of VOT's poor low-load efficiency, Section 7.2 presents a novel application of secondary side valley switching for the turn-ON requests; reducing switching loss and unnecessary energy circulation from turn-ON requests.

Section 7.3 proposes a novel hybrid control scheme that combines the advantages of the previous VOT and COT approaches without any additional hardware, into a Variable Frequency Variable ON-time (VF-VOT) scheme. In this VF-VOT scheme, VOT is used at low loads to enforce a minimum f_S while COT is used for medium/high loads to autonomously minimize f_S and maximize efficiency.

Lastly, for multiple output voltage compatibility, Section 7.4 introduces a novel reverse power flow concept that, with no additional hardware, reverses the Flyback power direction by using S_2 to transfer energy back to the DC-link; further exploiting the unique placement of the secondary side controller .

7.2 Soft Negative Current Turn-ON Requests

7.2.1 Effects of Irregular Secondary Turn-ON Voltage

As described in Section 6.7, the peak negative current for a turn-ON request is affected by Flyback ringing – not only by the magnitude and direction of inductor current at the instant of turn-ON, but also by the secondary turn-ON voltage. This is due to the different stored energy dissipated from S_2's parasitic output capacitance at turn-ON. Depending on the direction of i_{L2} at the instant of this hard turn-ON and the magnitude the subsequent oscillations, the peak negative current will vary despite consistent t_{NEG}. This varying negative current subsequently leads to varying peak primary currents and varying period-to-period switching frequency. A measured example of this effect captured with the *SSCF2* demonstrator operating with low-line input voltage is shown in Fig. 7.1. A constant negative current time (t_{NEG}) of 360 ns and constant primary t_{ON} of 2.19 µs was used.

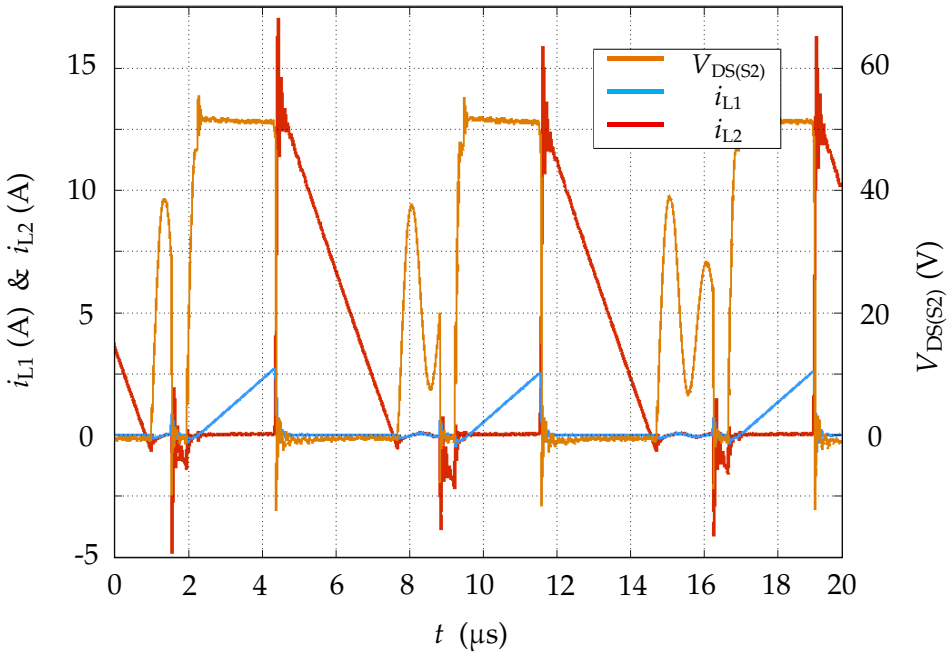


Figure 7.1: Measured effects of irregular S_2 turn-ON voltage.

Tab. 7.1 lists the turn-ON voltages, resulting inductor currents and instantaneous switching frequencies for each of the three switching periods shown in Fig. 7.1.

Table 7.1: Inductor currents resulting from different S_2 turn-ON voltages.

Switching Period	**1st**	**2nd**	**3rd**
Secondary Turn-ON Voltage	28.8 V	19.9 V	24.6 V
Secondary Negative Current	−1.34 A	−2.10 A	−1.5 A
Primary Peak Current	2.65 A	2.46 A	2.55 A
Secondary Peak Current	13.25 A	12.30 A	12.75 A
Subsequent Switching Frequency	146.5 kHz	150.2 kHz	148.0 kHz

These measurements show that relatively little turn-ON voltage deviation results in significantly different peak inductor currents. For example, the first switching period in Fig. 7.1 yields a 40 % smaller peak negative current than the subsequent period despite the same ON-time. For high-line input voltage, the effect was even more pronounced with secondary side Flyback ringing as high as 100 V. This phenomena not only affects switching frequency stability but also efficiency since t_{NEG} has to be chosen to work with for the worst-case turn-ON voltage: i.e. at the peak of Flyback ringing. It follows that unnecessary negative current is circulated for low voltage turn-ON events, increasing losses associated with turn-ON requests and energy circulation to achieve Q-ZVS.

7.2.2 Hardware

To overcome this, the circuit shown in Fig. 7.2 was added to *SSCF2* to provide a signal Q_{SOFT} to indicate whether Flyback ringing is below V_{OUT}. The network acts as a level sense with U_{SOFT} representing V_{OUT} scaled by a resistive divider.

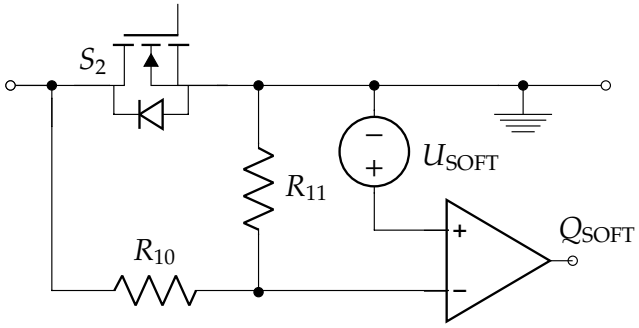


Figure 7.2: Schematic of sensing circuit for soft turn-ON requests.

Table 7.2: Key components for *SSCF2* soft turn-ON request sensing.

Resistor	R_{10}	160 kΩ
Resistor	R_{11}	8.2 kΩ
Comparator	-	ADCMP600
DC Voltage Source	U_{SOFT}	1.0 V

Tab. 7.2 lists the employed component values corresponding to Fig. 7.2. By using this signal along with the V_{OUT} comparator signal Q_{OUT} (explained in section 5.2.3) – such that a turn-ON request is only initiated when both V_{OUT} and $V_{DS(S2)}$ are below desired V_{OUT} – the range of turn-ON voltages and negative current peaks is thus limited. The "worst-case" t_{NEG} can then be reduced to the ON-time required for turn-ON at desired V_{OUT}, rather than at the ringing peak. Decreased turn-ON voltage will reduce S_2 switching loss and the frequency deviation associated with varying current peaks. However, a new source of frequency instability is introduced since a turn-ON request can now not always be initiated as soon as V_{OUT} falls below its reference, interrupting the natural VOT rhythm.

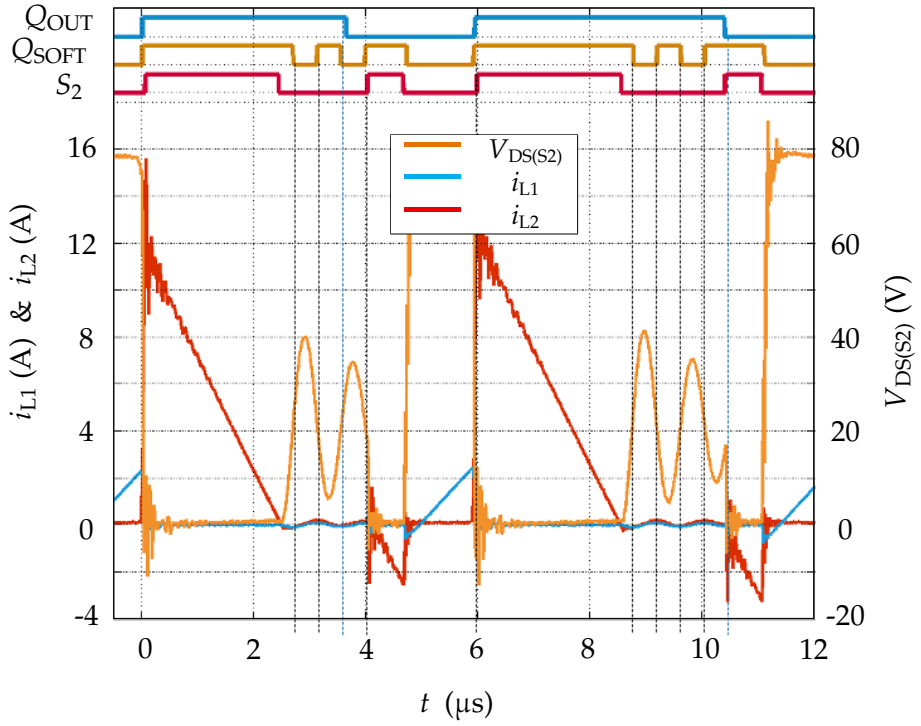


Figure 7.3: Measured application *SSCF2* using soft S_2 turn-ON requests.

Fig. 7.3 shows a measurement of *SSCF2* after being modified with the proposed sensing circuit and turn-ON reguest logic. For the first switching period, Q_{OUT} falls at $t = 9.2\,\mu s$ indicating that a turn-ON request is required. However, $V_{DS(S2)}$ is above the V_{OUT} threshold at this instant. Instead, a turn-ON request is only initiated once Q_{SOFT} goes high, indicating $V_{DS(S2)}$ is below V_{OUT} threshold. No such delay occurs for the second switching period because the Flyback ringing is already below V_{OUT} threshold when the Q_{OUT} signal goes high.

7.2.3 Frequency Variation

Fig. 7.4 compares the frequency variation of *SSCF2* operating under a 150 kHz VOT control scheme both with and without soft turn-ON requests employed. Despite Q_{SOFT} interrupting natural VOT rhythm and f_S, the overall frequency deviation is smaller than the deviation caused by varying turn-ON voltages. This is due to the competing effects of more consistent peak negative currents (reducing period-to-period frequency variation) being balanced by the interrupting effect of the soft turn-ON requests. The mean switching frequency with and without soft turn-ON requests remains close to the 150 kHz set-point.

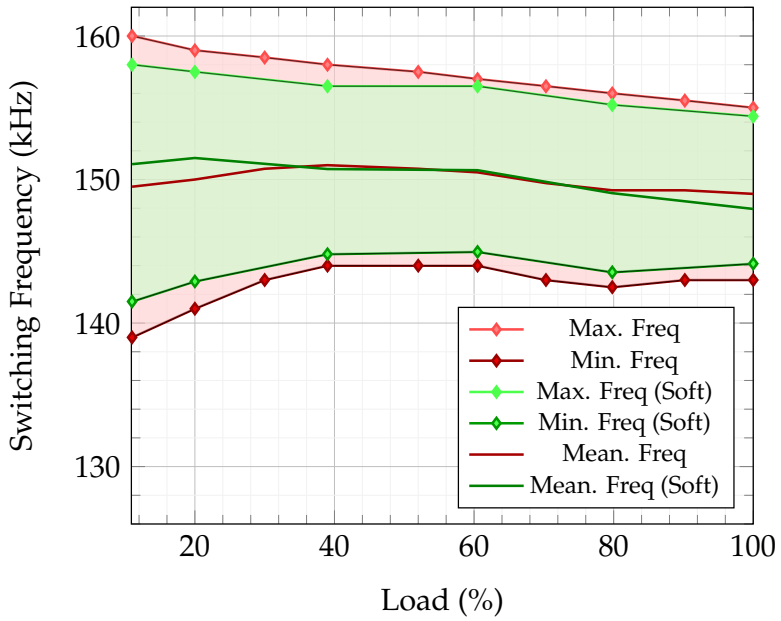


Figure 7.4: *SSCF2* switching frequency vs. load for low-line input with and without soft turn-ON requests.

7.2.4 Efficiency

As well as reducing the switching frequency deviation, the proposed soft turn-ON request approach also provides more consistent peak negative currents (allowing a 20 % reduction of t_{NEG}) as well as reduced turn-ON switching loss for S_2. As such, the efficiency of *SSCF2* was re-measured using the soft turn-ON request modification. The corresponding measured efficiency is shown in Fig. 7.5 along with *SSCF2* efficiency without the soft turn-ON requests.

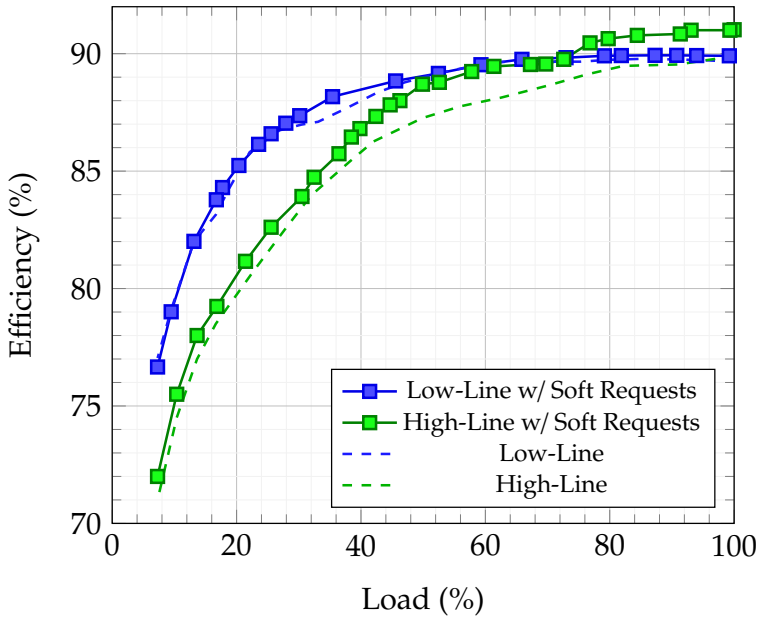


Figure 7.5: *SSCF2* VOT efficiency, with and without soft turn-ON requests.

The proposed technique improved efficiency by up to 1.5 % for high-line, high-load operation since the large S_2 turn-ON voltage caused by the compounding effects of large Flyback ringing and full duty-cycle is removed. Furthermore, the largest efficiency improvements occurred when *SSCF2* (without soft turn-ON requests) would naturally turn ON S_2 near the peaks of the Flyback ringing: therefore more switching loss was eliminated. This phenomena was observed for high-line input at 50 %, 60 %, and 78 % load and is reflected in Fig. 7.5 with small jumps in the efficiency curve. In contrast, low-load turn-ON voltage is normally small since ringing amplitude fades with longer dead time after synchronous rectification. Likewise, low-line efficiency is only marginally improved because ringing amplitude is generally smaller.

7.3 VF-VOT Concept

7.3.1 Proposed Concept

To address the low-load efficiency deficit, a novel control approach is proposed that combines the variable frequency (VF) property of the original COT scheme with VOT scheme, to create a VF-VOT scheme. The comparison of turn-ON request frequency (f_R) to a reference remains from VOT, but now both the reference frequency (f_{REF}) and primary t_{ON} are variable; resulting in a subtle but important shift. Rather than maintain constant frequency, the logic infers whether power transfer is sufficient and changes either the switching frequency (VF mode), or t_{ON} (VOT mode) depending on whether power transfer is too high or too low. While the output load determines the power required, the power transfer for a given load, t_{ON}, and f_S is set by $V_{DC\text{-}link}$. Fig. 7.6 shows a graphical depiction of the proposal. Before the primary controller decides whether to invoke VF or VOT operation, it first determines whether instantaneous f_R is higher or lower than the current f_{REF} to infer whether more or less power is needed at the output.

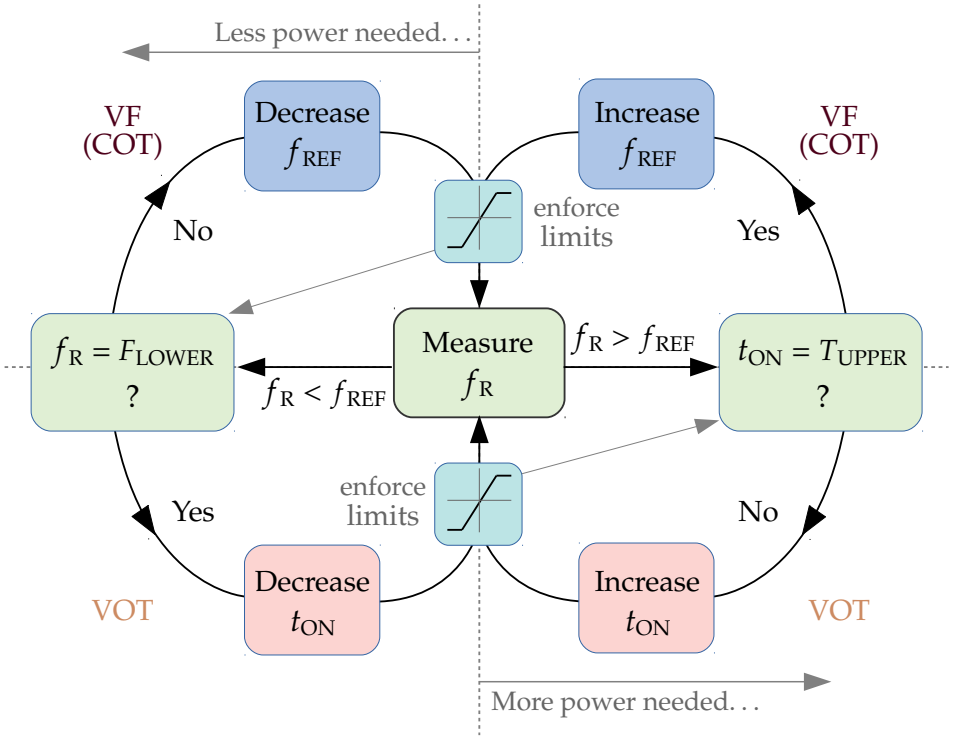


Figure 7.6: Flow chart of VF-VOT control scheme.

In the case of excessive power transfer (falling load or rising $V_{\text{DC-link}}$), the control first reduces the reference frequency to maintain maximum ON-time (VF mode). Once f_{REF} reaches a pre-set lower limit (F_{LOWER}), the control then begins reducing t_{ON} to maintain a minimum allowed switching frequency (VOT). In the case of insufficient power transfer (rising load or falling $V_{\text{DC-link}}$), the control first increases t_{ON}, transferring more energy per switching period (VOT mode). Once t_{ON} reaches the T_{UPPER} limit, the secondary controller will naturally demand more power causing f_{S} to rise instead (VF mode). A method of dimensioning T_{UPPER} for rated power at maximum desired f_{S} without risking excessive S_1 turn-OFF overshoot is given in [81].

In summary, falling power demand leads to VF mode and rising power demand leads to VOT mode and, once either of the respective lower and upper boundaries are reached, vice-versa. The VF-VOT approach ensures that the Flyback is always operating at the minimum possible switching frequency capable of supporting the output load – universally reducing the loss and circulating energy associated with switching frequency and turn-ON requests (compared to VOT control). Both t_{ON} and f_{REF} operate under two parallel standard PI control structures, similar to that shown in Fig. 6.8 [82].

7.3.2 Hardware and Control Set-Up

To make a direct efficiency comparison, the *SSCF2* demonstrator was used without any hardware changes. From *SSCF2*'s hardware parameters, VF-VOT's upper t_{ON} limit (T_{UPPER}) was chosen to give a maximum f_{S} of 150 kHz with an F_{LOWER} of 90 kHz chosen to give an equal share of VF and VOT action across the load range. A t_{ON} lower limit (T_{LOWER}) was required to avoid negligible/zero power transfer that might disturb the PI control loop. Tab. 7.3 lists the VF-VOT control boundaries employed on *SSCF2*.

Table 7.3: Implemented control limits for VF-VOT with *SSCF2*.

Maximum ON-time (High-Line)	T_{UPPER}	1.25 µs
Maximum ON-time (Low-Line)	T_{UPPER}	2.45 µs
Minimum ON-time	T_{LOWER}	0.21 µs
Minimum Switching Frequency	F_{LOWER}	90 kHz

7.3.3 Measured Switching Frequency and ON-time Behaviour

Taken from the *SSCF2* demonstrator, Figs. 7.7- 7.9 show measurements of f_S and t_{ON} with respect to DC-link ripple for a range of loads. Fig. 7.7 shows this for 90 % load, where f_S drifts naturally with DC-link ripple. However f_S never falls to F_{LOWER} meaning t_{ON} is never changed from T_{UPPER}. This COT/VF action allows the converter to operate with the lowest f_S possible with the instantaneous $V_{DC\text{-}link}$ autonomously, reducing energy circulation from turn-ON requests and switching and gate loss to a minimum.

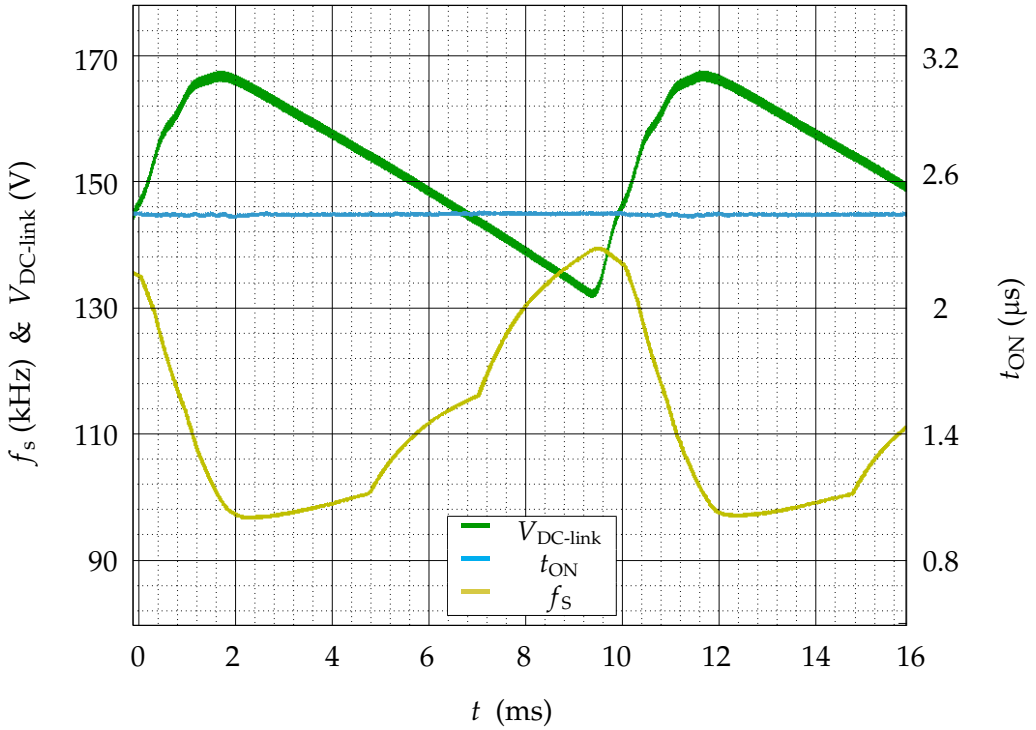


Figure 7.7: *SSCF2* low-line VF-VOT at 90 % load.

In contrast, Fig. 7.8 shows 60 % load where both VF and VOT work together to compensate DC-link ripple. As soon as the increasing $V_{DC\text{-}link}$ causes T_{UPPER} to push f_S down to F_{LOWER}, t_{ON} is reduced. This VOT action then maintains F_{LOWER} until $V_{DC\text{-}link}$ is low enough that T_{UPPER} cannot support the load, whereby f_S is then increased. The noise present in t_{ON} during rising f_S is due to the f_R estimated by the controller not matching real f_S.

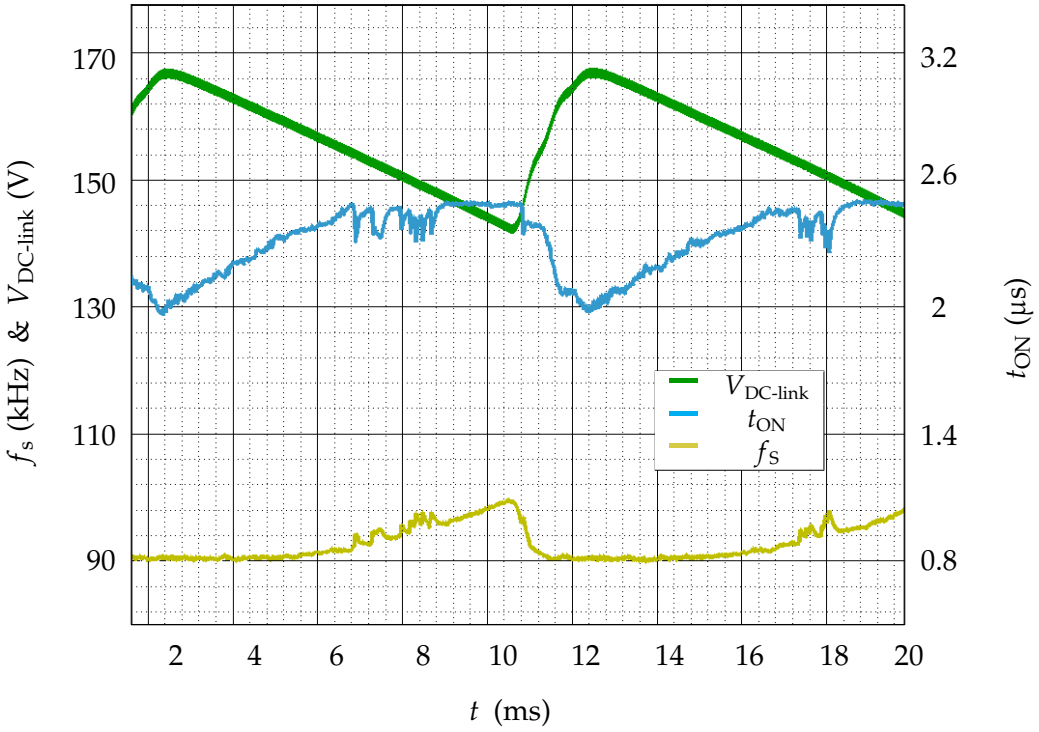


Figure 7.8: *SSCF2* low-line VF-VOT at 60 % load.

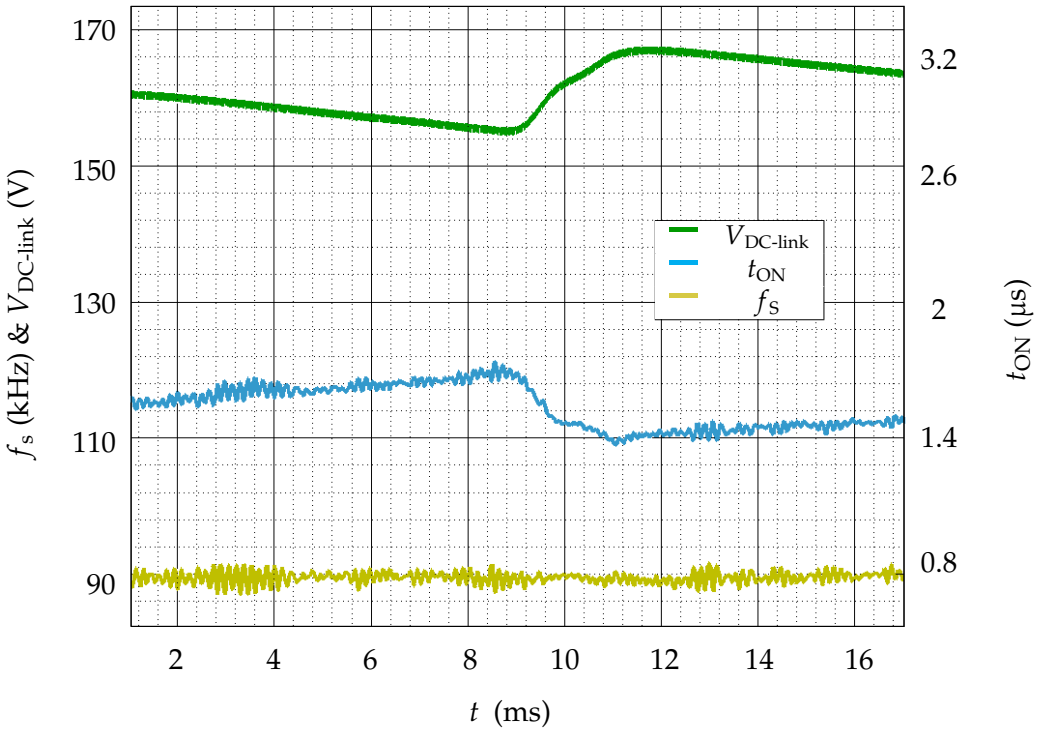


Figure 7.9: *SSCF2* low-line VF-VOT at 25 % load.

Fig. 7.9 shows the VF-VOT behaviour during 25 % load wherein the required power and DC-link ripple are low enough that t_{ON} never rises to T_{UPPER} and the converter stays in VOT mode to maintain F_{LOWER}, preventing f_S falling outside of desired lower limit. This thus represents the largest loss associated with turn-ON requests due to the "artificially" high switching frequency.

As in Chapter 6, the 65 W *SSCF2* demonstrator was operated at several load points between 10 % and 100 % load. Measurements of f_S and primary t_{ON} were taken at the extremities of the DC-link ripple at each corresponding load point, and are shown in Fig. 7.10.

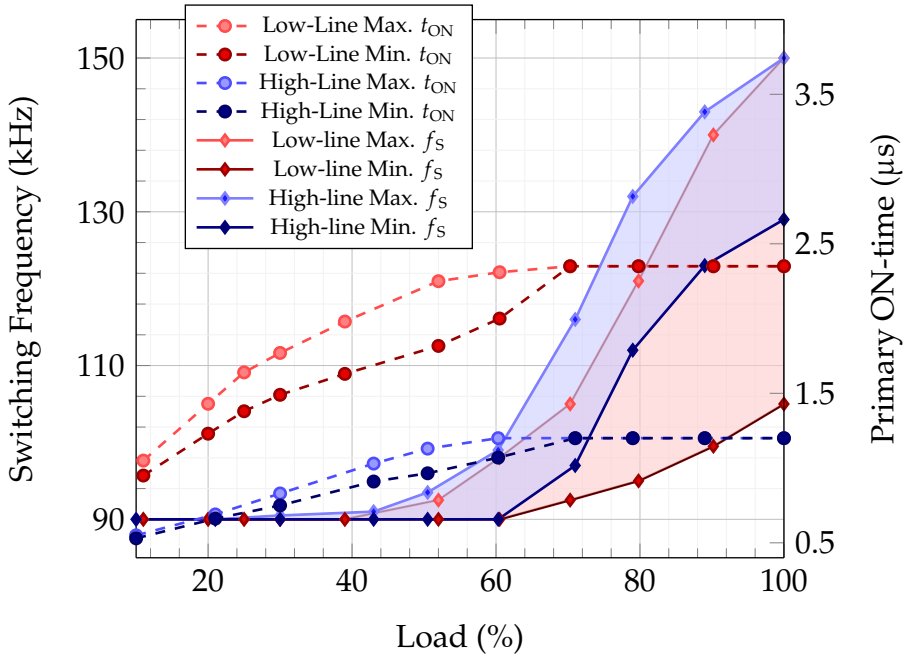


Figure 7.10: *SSCF2* VF-VOT Switching frequency and primary ON-time vs load.

As predicted, at low-loads the VOT action holds f_S at the minimum 90 kHz while at high-loads the VF action maintains maximum ON-time ensuring the minimum switching frequency possible with the instantaneous DC-link voltage. Between 30 % and 70 % load both VF and VOT actions work together to both ensure minimum possible switching frequency depending on DC-link ripple, and simultaneously ensure that F_{LOWER} is not breeched. With a lower F_{LOWER} limit, the point at which VOT takes over would occur at a lower load.

7.3.4 Efficiency

The measured efficiencies of *SSCF2* demonstrator utilising both VF-VOT and VOT control schemes are plotted in Fig. 7.11, both with the soft-turn-ON-request technique applied. For comparison, the efficiency of the professional PMP9208 is also plotted. High-load efficiency matches that achieved with VOT indicating that any loss reduction due to lower f_S is immediately cancelled by the higher constant peak currents.

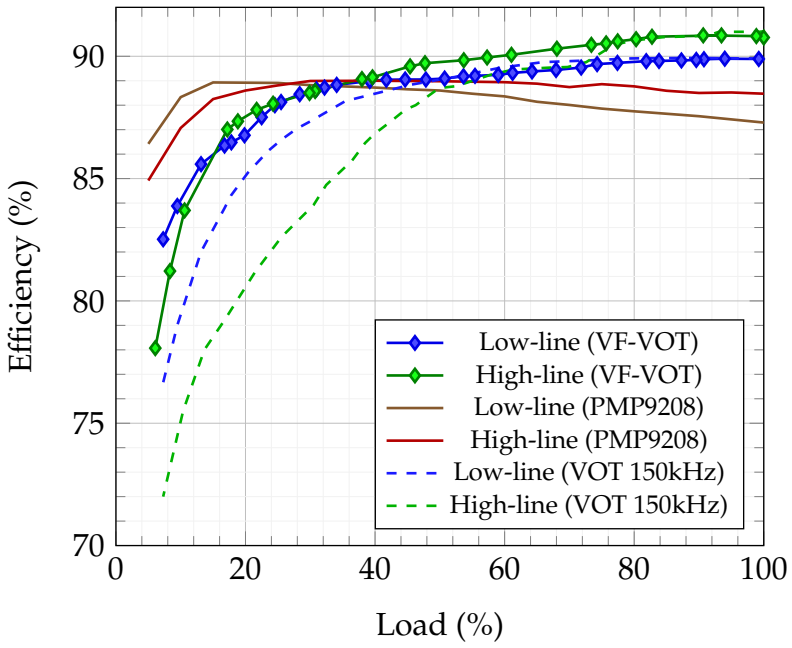


Figure 7.11: Comparison of *SSCF2* VF-VOT vs. 65 W TI PMP9208 demonstrator.

Low-load efficiency is significantly improved due to the reduced loss associated with f_S and turn-ON requests. The best efficiency (90.77 %) was achieved at high-load with high-line input; almost identical to VOT. However, high-line efficiency has a steeper drop at low-load than low-line after entering full VOT control, due to the larger negative current required for turn-ON requests. As shown in Fig. 7.10, the demonstrator enters full VOT mode below ≈ 40 % load once the F_{LOWER} limit is hit. This behaviour is reflected in Fig. 7.11 whereupon the efficiency for both high- and low-line begins to rapidly decrease. In practice, F_{LOWER} could be reduced beyond 90 kHz to continue boosting low-load efficiency.

The TI PMP9208 uses a rival opto-isolator-less control (primary side regulation) but uses the same core shape and turns-ratio. The PMP9208 uses a passive diode pair for secondary synchronous rectification whereas the Secondary Side Controlled Flyback uses an active switch S_2 and therefore exhibits superior efficiency at high-load where secondary side currents are high. However, the primary side regulation concept requires no additional negative current and energy circulation for turn-ON requests and as such boasts superior low-load efficiency.

In summary, the Secondary Side Controlled Flyback concept in combination with VF-VOT control achieved good high-load efficiency, out-performing the PMP9208 with a peak of 90.77 %. However a minimum switching frequency of 90 kHz was insufficient to push low-load efficiency in-line with that of the PMP9208, but was significantly better than 150 kHz VOT control. Low-load loss remains a disadvantage of the Secondary Side Controlled Flyback concept. By re-measuring *SSCF2* efficiency with the VOT control (described in Section 6.4) set at different reference frequencies (F_{REF}), it is possible to see how lowering F_{LOWER} in VF-VOT control would increase low-load efficiency (shown in Fig. 7.12). It is unknown how EMI-filter design might constrain how far F_{LOWER} could be reduced realistically.

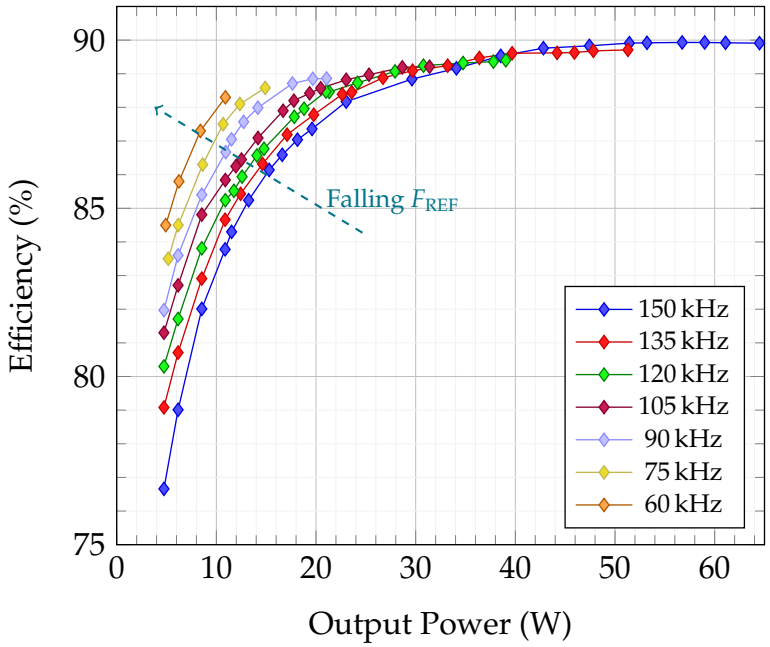


Figure 7.12: Measured low-line *SSCF2* VOT efficiency with various F_{REF}. Replicating the effect of reducing F_{LOWER} in VF-VOT control.

7.4 Reverse Power Flow for Multiple Output Voltages

Key advantages of the Secondary Side Controlled Flyback concept include the direct access to V_{OUT}, synchronous rectification switch S_2, and to any load disconnect switch [58]. Combining these features offers a novel opportunity for reverse power flow for discharging C_{OUT} back to $C_{DC\text{-}link}$ in a non-dissipative way without any additional components or signal coupling; useful for multiple output voltage applications such as USB-PD [45].

This section explores discharging C_{OUT} from 20 V to 5 V [83]. Such a change will cause an inconsequential rise in the DC-link voltage as the energy stored in C_{OUT} is typically much smaller than that of $C_{DC\text{-}link}$ due to the voltage difference.

Currently, the most common existing strategy for discharging the output capacitor (C_{OUT}) is by using an additional switch and resistor in parallel with C_{OUT} [84, 85]. In contrast, the proposed solution requires no such additional hardware and takes advantage of the secondary side controller's direct access to V_{OUT} and S_2 by simply reversing the Flyback direction, using S_2 to transfer energy back to the DC-link, turning S_1 into the synchronous the rectifications switch.

7.4.1 Proposed Concept

Reverse power flow is achieved by turning OFF the load-disconnect switch, and repeatedly switching S_2 with period $t_{NEG(R)}$ to energize the coupled inductor with negative current pulses, resulting in primary side current (i_{L1}) via S_1 body diode and net energy transfer from secondary to primary side. However, any current through S_1 body diode will discharge $C_{OSS(S1)}$ and register as a turn-ON request on the independent primary side controller, and S_1 will turn-ON. This will risk positive i_{L1} and energy returning to the output; nullifying any reverse power flow. To avoid this, the secondary controller can take advantage of the primary controller's simplicity by:

- Sending negative current pulses below the primary controller's lower frequency limit at a fixed low frequency (F_{RPF}) – tricking the VOT/VF-VOT control into reducing the primary ON-time to its minimum value (T_{LOWER}).

- Sending large negative current pulses such that S_1, turns ON for T_{LOWER} and then OFF again all while i_{L1} is negative; avoiding unnecessary positive i_{L1}.

This approach requires no additional primary side logic complexity: the primary controller will not even be aware that reverse power flow is occurring. Thus, the secondary controller can simply resume steady-state operation, with normal turn-ON requests, once V_{OUT} has fallen to the new desired value.

7.4.2 Secondary Side VOT for Safe Reverse Power Flow

Negative currents should be large enough to encompass the entire primary T_{LOWER} at high and low V_{OUT}. However, using a constant $t_{NEG(R)}$ capable of achieving sufficient current at low V_{OUT}, may yield overly large negative currents at higher V_{OUT} and result in a turn-OFF overshoot that breaches S_2's breakdown voltage. Therefore, $t_{NEG(R)}$ must be slowly increased as V_{OUT} falls.

To avoid adding any active V_{OUT} measurement, the soft turn-ON request voltage sensing proposed in Section 7.2.2 can be re-purposed along with the VOT concept discussion in Section 6.4.1 for safe variable ON-time reverse-power flow with no additional hardware. Fig. 7.13 shows an exaggerated sketch of various waveforms for the proposed concept.

As described, while V_{OUT} is decreasing, F_{RPF} ($1/T_{RPF}$) remains constant. To compensate falling V_{OUT}, $t_{NEG(R)}$ can be seen to sporadically increase, pushing the peak negative secondary inductor current (i_{L2}). To detect when $t_{NEG(R)}$ should be modified, the secondary side controller infers V_{OUT} using the existing comparator signal Q_{SOFT}. The signal Q_{SOFT} indicates whether secondary drain-source voltage ($V_{DS(S2)}$) is above or below V_{OUT}. More specifically:

1. After S_2 turn-OFF, $V_{DS(S2)}$ necessarily rises above the V_{OUT} threshold due to reflected DC-link voltage. This toggles the comparator output Q_{SOFT} to go low.

2. Q_{SOFT} stays low until the i_{L1} reduces to zero – $V_{DS(S2)}$ no longer reflects $V_{DC\text{-}link}$ and thus $V_{DS(S2)}$ falls back below V_{OUT} threshold, toggling Q_{SOFT} back to high.

3. Therefore, the time that Q_{SOFT} is low (t_{iL1}) – represents the size of the negative current pulse. If this time decreases it implies that V_{OUT} has fallen.

4. The t_{iL1} measured after the very first pulse can be used as a reference ($T_{iL1(REF)}$). If t_{iL1} falls below this reference, $t_{NEG(R)}$ increases until t_{iL1} again matches $T_{iL1(REF)}$.

This novel approach of adapting the VOT scheme to the secondary side thus requires no additional sensing hardware. It ensures consistent peak negative currents large enough to consume the minimum primary ON-time for the entire V_{OUT} range and avoids excessive S_2 turn-OFF overshoot while guaranteeing net reverse power flow.

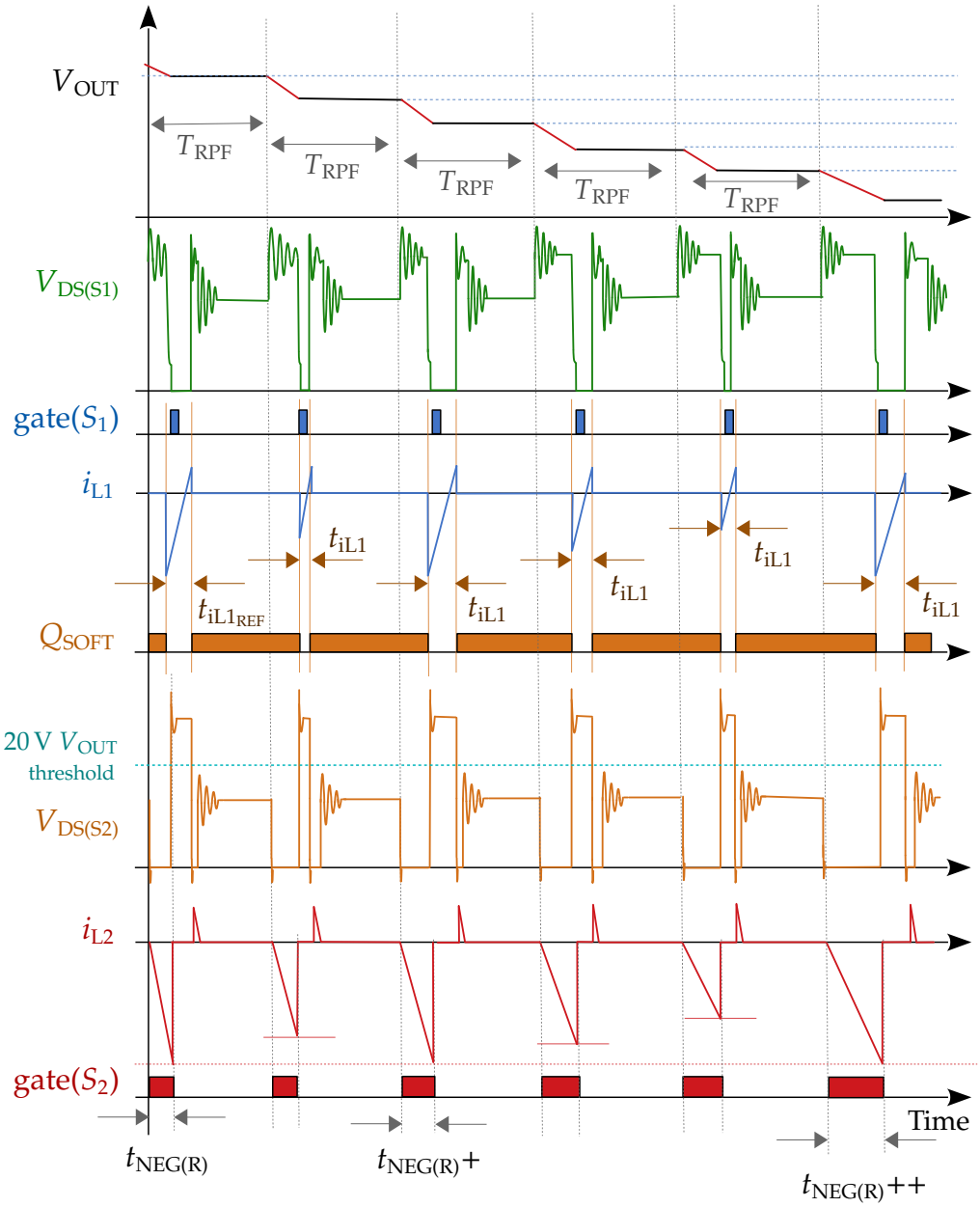


Figure 7.13: Sketch of reverse power flow concept.

7.4.3 Constraints on Minimum Negative Current Time

To ensure that negative i_{L1} always encompasses the entire primary ON-time, a lower limit for $t_{NEG(R)}$ is needed. This lower limit can be expressed as:

$$t_{NEG(R)} > \frac{N\, L_2\, V_{DC\text{-}link}}{L_1\, V_{OUT}}\, T_{LOWER} \tag{7.1}$$

Additionally, initial implementation of the proposed concept on the *SSCF2* also revealed that a minimum energy must be delivered in each switching period and must be larger than the energy needed to re-charge $C_{OSS(S1)}$ after L_1 has de-energized. Otherwise, the primary side will return more energy back to the output while re-charging $C_{OSS(S1)}$, than is delivered back to $C_{DC\text{-}link}$ in the first place. Fig. 7.14 shows a measurement of such a scenario.

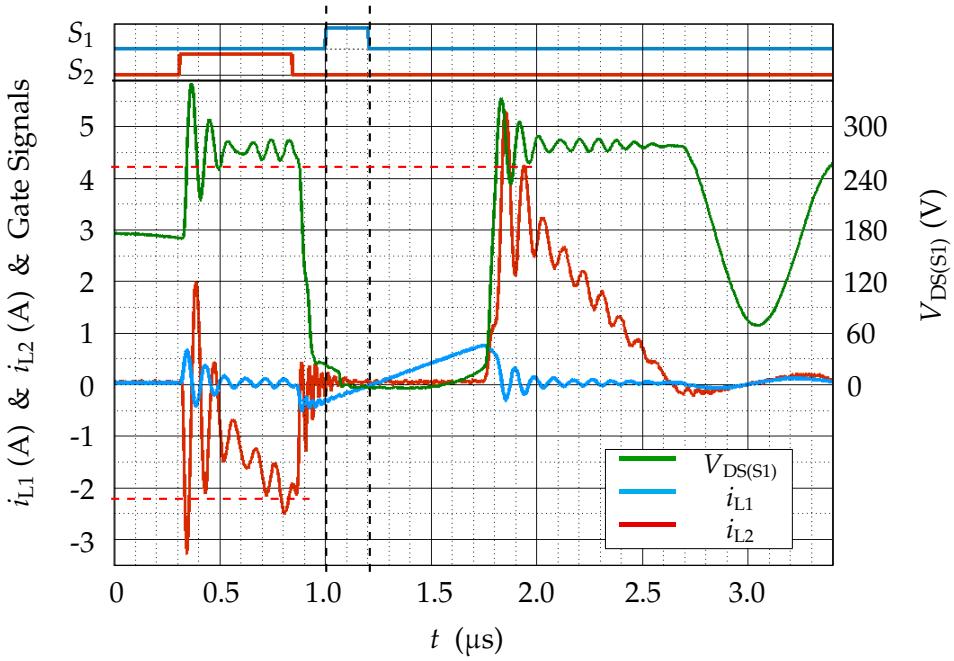


Figure 7.14: Circulating energy due to $C_{OSS(S1)}$.

The negative i_{L1} is large enough to encompass the primary T_{LOWER}, but i_{L1} continues to rise while $C_{OSS(S1)}$ charges. Subsequently, the peak positive current is larger than the peak negative current, resulting in net positive power flow from $C_{DC\text{-}link}$ to C_{OUT}. This current flow into $C_{OSS(S1)}$ (which is especially large for super-junction MOSFETs [86]) will always cause some circulation of energy back to C_{OUT} even if S_1 turns OFF during negative current.

To ensure net power flow from C_{OUT} to $C_{DC\text{-}link}$, $t_{NEG(R)}$ must always yield a negative current large enough to encompass the primary T_{LOWER} (7.1) and simultaneously return more energy than required to recharge $C_{OSS(S1)}$. This relation is given in (7.2), where $Q_{C_{OSS(S1)}}$ represents the charge required to bring $C_{OSS(S1)}$ from 0 V to $V_{DC\text{-}link}$.

$$t_{NEG(R)} > \frac{1}{V_{OUT}} \sqrt{2\, L_2\, V_{DC\text{-}link}\, Q_{C_{OSS(S1)}}} \tag{7.2}$$

To satisfy (7.1) and (7.2) during reverse power flow, $t_{NEG(R)}$ must rise as V_{OUT} falls; further justifying the proposed addition of VOT to the novel reverse power flow concept. Although satisfying both minimum $t_{NEG(R)}$ constraints and ensuring safe S_2 turn-OFF overshoot may leave a narrow allowable range for $t_{NEG(R)}$, only a single workable value for $t_{NEG(R)}$ is required for any given V_{OUT}.

7.4.4 Measurements

The concept was tested using the *SSCF2* demonstrator with VF-VOT primary control and 120 V_{RMS} input. The exact "handshake" used to indicate a required change in V_{OUT} is standardized in USB-PD and not discussed here, but information can be found in [46]. Instead, the secondary controller was programmed to supply 20 V and, after an arbitrary dead time, initiate reverse power flow to discharge to 5 V before continuing steady state operation.

Table 7.4: Settings used for reverse power flow and subsequent voltages/currents.

Fixed Discharge Switching Frequency	F_{RPF}	**65 kHz**
Initial $t_{NEG(R)}$ (V_{OUT} = 20 V)	$t_{NEG(0)}$	930 ns
Min. VF-VOT Switching Frequency	F_{LOWER}	**90 kHz**
Min. VF-VOT ON-time	T_{LOWER}	300 ns
Desired Negative i_{L2}	$I_{L2(RPF)}$	**−4.50 A**
Returned Peak i_{L2} due to $C_{OSS(S1)}$	$I_{L2(POS)}$	**3.75 A**
Resulting Peak $V_{DS(S2)}$ Overshoot	$\widehat{V}_{DS_{(S2)}}$	84 V

Fig. 7.15 shows a measurement of the entire reverse power flow procedure. The converter is initially supporting a 20 V, 30 W load using the VF-VOT control scheme, until t = 4 ms, at which point the artificial "handshake" occurs and the load-disconnect switch is turned OFF.

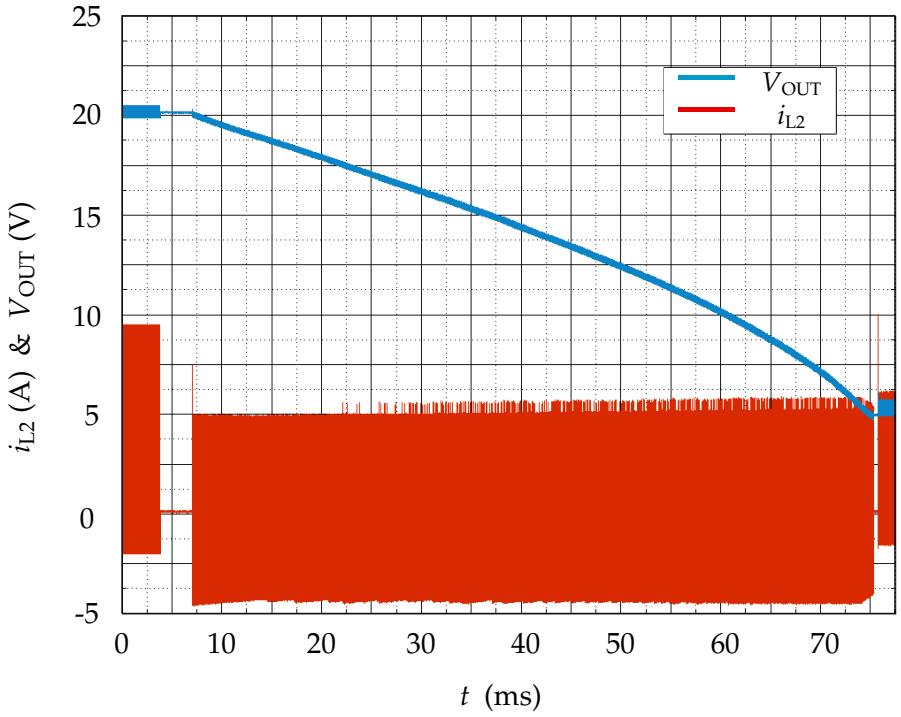


Figure 7.15: Measurement of reverse power flow; discharging 20 V to 5 V.

The secondary controller then waits for a relatively long time (4 ms) to both ensure that drain-source voltages and inductor currents stabilize before starting reverse power flow, and to force the primary ON-time down to its lower limit T_{LOWER}. The proposed VOT reverse power flow approach then begins and successfully maintains constant peak negative currents while V_{OUT} falls.

At $t = 75$ ms, the desired V_{OUT} has been achieved at which point, the load-disconnect switch is turned back ON and steady state operation resumes to support the new 5 V load. As indicated by the desired and returned currents listed in Tab. 7.4, approximately 69 % of the energy delivered in the negative current pulse is returned after charging $C_{OSS(S1)}$. Consequently the discharge takes a relatively long time of ≈ 70 ms. However, in the context of consumer USB-PD adapters undergoing occasional load change, this is a short enough discharge time that would not be noticed by an end-user. Using a primary device with a smaller C_{OSS} would result in faster reverse power flow.

This shows the Secondary Side Controlled Flyback converter's capability to discharge its own output capacitor in a non-dissipative manner without any additional primary side complexity.

7.5 Conclusion

This chapter presented three methods of expanding the capability of the Secondary Side Controlled Flyback converter: a novel soft turn-ON request concept, a new hybrid VF-VOT control scheme, and a novel reverse power flow concept for multiple output voltage capability.

Firstly, to address two main conclusions of Chapter 6, two novel concepts were proposed: soft-turn-ON-requests and Variable Frequency Variable ON-time control. The soft turn-ON requests resulted in a 1.1 % efficiency improvement at high-line, high-load due to reduced switching loss and reduced loss associated with unnecessary energy circulation from turn-ON requests. However, frequency stability only slightly improved since the soft turn-ON requests now can not always be initiated when required, but only when Flyback ringing and output voltage are simultaneously below their respective thresholds: interrupting natural VOT rhythm.

The new control scheme combined two existing control approaches (constant ON-time and variable ON-time) to make a variable frequency variable ON-time control (VF-VOT). This scheme allowed the Flyback switching frequency to drift at medium-high loads to maximize efficiency, and to vary primary ON-time at low loads to maintain a minimum switching frequency. Although low-load efficiency still dropped once VOT became dominant, this scheme resulted in an efficiency boost across most of the load range; putting the Secondary Side Flyback efficiency in line with existing Flyback demonstrators such as the TI-PMP9208.

Lastly, reverse power flow was demonstrated using a novel concept whereby the output capacitor (C_{OUT}) is discharged back to the input capacitor in a non-dissipative manner, without any added complexity to the primary side logic. While successful, several constraints on the negative currents used to discharge C_{OUT} were discovered that limit the speed of the overall discharge process. These constraints include the breakdown voltage of S_2 limiting the maximum negative current and the parasitic output capacitance of S_1 limiting the minimum workable negative current. For compatibility with USB-PD applications, an output voltage discharge from 20 V to 5 V was demonstrated and took 70 ms.

Chapter 8

Conclusions

8.1 Summary

This thesis presented an investigation of a novel power adapter concept, the Secondary Side Controlled Flyback converter, by means of sub-circuit design, control scheme conceptualization, prototyping and measurement analysis. The overall research objective was as follows:

"To investigate the feasibility, viability and capability of the Secondary Side Controlled Flyback converter concept as a real-world power adapter solution."

The target application explored in this thesis was a 65 W universal adapter providing 20 V_{DC} output from either 120 V_{RMS} or 230 V_{RMS}. To achieve the above objective within this context, the author focused on four diverse yet interrelated sub-objectives when considering the feasibility, viability and capability of the Secondary Side Controlled Flyback converter concept:

- To design precise yet inexpensive drain-source voltage sensing circuits for reliable operation.
- To develop a control scheme with as much regulation on the secondary side as possible while achieving good power adapter performance.
- To demonstrate competitive efficiency using the proposed sensing circuits and control scheme on a working prototype.
- To explore any unique features and advantages that may arise from a controller placed on the secondary side of the Flyback converter.

8.1.1 Feasibility

The general feasibility of the secondary side controlled Flyback concept was proven in hardware using a 65 W demonstrator: the *SSCF1*. The main controller was based on the secondary side of the coupled inductor and was entirely isolated from the grid input voltage. All "communication" between primary and secondary sides occurred without any auxiliary isolated signal coupling, but instead using a novel drain-source voltage sensing circuit across the primary side switch to reliably detect a so-called "turn-ON request" transmitted from the secondary side via the Flyback's coupled inductor. A working start-up routine was presented and the demonstrator was shown to sustain a stable output voltage across the load range.

To show this feasibility, the primary side switch was supplemented with a simple yet novel drain-source voltage sensing circuit that allowed the primary side to autonomously filter out unwanted zero voltage crossings, leading to reliably safe turn-ON of the primary switch that was as fast as existing opto-isolator alternatives: making the concept competitive with existing secondary side control concepts, but requiring no additional isolated signal coupling components.

To test the limits of the concept's feasibility, constant primary ON-time was used for maximum secondary side control. However the price of complete secondary side control with constant primary ON-time is that the switching frequency varies considerably with both output load and DC-link ripple. This, in combination with the large negative current required for full zero voltage turn-ON requests, resulted in poor efficiency peaking at 84.90 % (below that expected of 65 W Flyback adapters). The secondary side synchronous rectification sensing also exhibited slow zero current crossing response: leading to unwanted negative current every switching period further reducing efficiency, especially at high load/high switching frequency.

8.1.2 Viability

To improve the viability of the concept as an alternative to existing solutions, the efficiency had to be improved. In particular, the losses caused by the large negative current for turn-ON requests in combination with the large switching frequency range resulting from the constant ON-time control had to be reduced. An improved 65 W prototype (the *SSCF2*) included primary drain-source voltage sensing for quasi-zero-voltage turn-ON requests and improved synchronous rectification sensing. It was optimised for a new control scheme (variable ON-time) for operation with

constant 150 kHz switching frequency. The demonstrator and control scheme were then exposed to several load jumps to ensure viability in non ideal load conditions.

The quasi-zero-voltage (Q-ZVS) based turn-ON commands required significantly reduced negative current pulses from the secondary side; freeing more of the duty-cycle for power transfer and reducing circulating currents. The variable ON-time control resulted in a split controller structure, whereby secondary side controller still regulated the output voltage with turn-ON requests, but the primary side regulated the switching frequency with variable ON-time. This was shown to automatically match power transfer to the output load and compensate DC-link ripple to ensure constant peak inductor currents for a given load. With *SSCF2*'s improved coupled inductor, the combination of the Q-ZVS turn-ON requests with constant switching frequency led to improved efficiency across the load range, peaking at 89.90 %. This is within the expected efficiency range for bespoke 65 W Flyback adapters.

While this approach required additional primary side complexity, the improved viability is significant: optimal coupled inductor design, smaller peak inductor currents, improved efficiency and reduced EMI-filter while maintaining all key features of the proposed concept (direct output voltage access without isolated signal coupling). The main weaknesses of the approach were poor low-load efficiency due to the fixed switching frequency, and varying turn-ON voltages due to natural Flyback ringing that caused varying negative currents and varying switching frequency of ± 10 kHz (along with oversized negative current for turn-ON requests).

8.1.3 Capability

To explore the capability of the Secondary Side Controlled Flyback concept, three additional novel concepts were shown to push the efficiency and exploit the unique possibilities of a secondary side based controller with active synchronous rectification switch. These concepts were tested using the *SSCF2* demonstrator.

To address the non-consistent negative currents caused by varying turn-ON request turn-ON voltage, a level detection circuit was appended to the secondary side switch's drain that ensured turn-ON requests were only initiated for low drain-source voltages: so-called soft turn-ON requests. This was shown to both reduce switching loss and the variation of negative current peaks. This allowed the turn-ON request time to be reduced to decrease unnecessary circulating current, and boost efficiency by up to 1.5 % at high-line, high load. However, the soft-turn-ON requests necessarily interrupt the natural rhythm of the constant frequency control and thus

switching frequency variation was only slightly reduced.

To truly boost the efficiency capability of the Secondary Side Controlled Flyback, a hybrid control scheme was developed. In short: the primary side maintained constant ON-time to, allow the switching frequency to naturally drift with DC-link ripple and load, *unless* switching frequency dropped to or beyond a lower limit, at which point the ON-time became variable to ensure constant switching frequency at this lower limit. This removed the loss associated with constant switching frequency for medium to high loads, while avoiding very low switching frequencies at low loads. Combining this control with the soft turn-ON requests using *SSCF2* exhibited improved efficiency across the load range with a peak of 90.77 %.

A new capability of reversing the power flow of the Flyback using the secondary switch (in order to reduce the output voltage in a non-dissipative manner) was demonstrated for compatibility with 20 V to 5 V output voltage change. Without any additional primary side complexity, it was shown that by sending large negative current pulses from the secondary side, the primary side can operate as normal without even being aware that reverse power flow is taking place. This allows the reverse power flow and multiple output voltage compatibility to be added without adding any primary side complexity.

This showed the Secondary Side Controller Flyback converter to be capable of an efficiency rivalling that of competitor control strategies while offering direct output voltage access without any isolated signal coupling, along with multiple output voltage compatibility via reverse power flow.

8.2 Outlook: Short Term Further Work

Important further work identified by the author includes the following issues:

- A comparison of EMI-filter requirements for VOT and VF-VOT controls.
  - VF-VOT has a broader frequency range than VOT, but the peak currents are smaller when the switching frequency is at the lower limit. Is there a trade-off between low load efficiency and EMI-filter requirements?
- Repsonse to output load short circuit failure.
  - How can the secondary side sense the failure and safely shut down?
  - How can the primary side infer the shut-down and re-initiate start-up?

8.3 Outlook: Wide Band Gap Devices

A large amount of power-electronics research today is focussed on the development of gallium-nitride (GaN) and silicon-carbide (SiC) based switching devices. For the same chip area, the advantages of these materials over silicon stem from the higher energy band-gap between the valence and conduction bands (giving higher blocking voltages) and higher electron mobility (giving lower ON-state resistance ($R_{DS(ON)}$)). Furthermore, the parasitic output capacitance of a wide-band-gap device is smaller than that of a comparable silicon device [87]. SiC MOSFETs show potential for market application in high voltage applications (several kilo-volts) while GaN devices are often in competition with super-junction MOSFETs in the 600 V blocking voltage range [88]. As such, there are plenty of examples of very high-efficiency Flyback demonstrators using GaN devices [89]. Two potential benefits of using a GaN High Electron Mobility Transistor (HEMT) device in the Secondary Side Controlled Flyback concept are introduced here as suggested areas of further work.

8.3.1 Turn-ON Request Loss

The efficiency of the Secondary Side Controlled Flyback converter may benefit from a GaN based S_1. Not only because of the improved $R_{DS(ON)}$, but also due to the reduced negative current required to achieve a turn-ON request. This may allow the Flyback to be pushed into very high frequencies for high power density, while maintaining the competitive efficiency proven to be possible in this thesis.

8.3.2 Reverse Power Flow

Reverse power flow whereby C_{OUT} is discharged with short pulses with ON-time $t_{NEG(R)}$, was shown in Section 7.4 with a super-junction MOSFET for S_1. The process was slowed by the energy circulation caused by the charging and discharging of S_1's large parasitic output capacitance ($C_{OSS(S1)}$). The proposed reverse power flow approach in Section 7.4.2 maintained constant peak negative current at switching frequency F_{RPF}. As such it is possible to speculate how reverse-power-flow discharge time (t_{DIS}) would change with the ratio of $E_{NEG(R)}$ (energy removed from C_{OUT} during $t_{NEG(R)}$) to $E_{POS(R)}$ (the energy returned to C_{OUT} due to the re-charging of $C_{OSS(S1)}$). Replacing S_1 with an equivalent 600 V e-mode GaN HEMT might allow much shorter t_{DIS} due to the smaller C_{OSS} and the smaller x that would result.

$$x = \frac{E_{\mathrm{NEG(R)}}}{E_{\mathrm{POS(R)}}} \tag{8.1}$$

$$t_{\mathrm{DIS}} \approx \frac{1}{F_{\mathrm{RPF}}} \frac{E_{\mathrm{C_{OUT}}}|_{20\mathrm{V}} - E_{\mathrm{C_{OUT}}}|_{5\mathrm{V}}}{E_{\mathrm{NEG(R)}}(1-x)} \tag{8.2}$$

Fig. 8.1 shows expected t_{DIS} for varying x using (8.2) assuming the same F_{RPF} and $t_{\mathrm{NEG(R)}}$ given in Tab. 7.4. The x value for the super-junction device used for *SSCF2* (IPL60R125C7) was calculated using peak currents given in Tab. 7.4. The corresponding t_{DIS} given by (8.2) matches the measured value in Section 7.4.4 (70 ms).

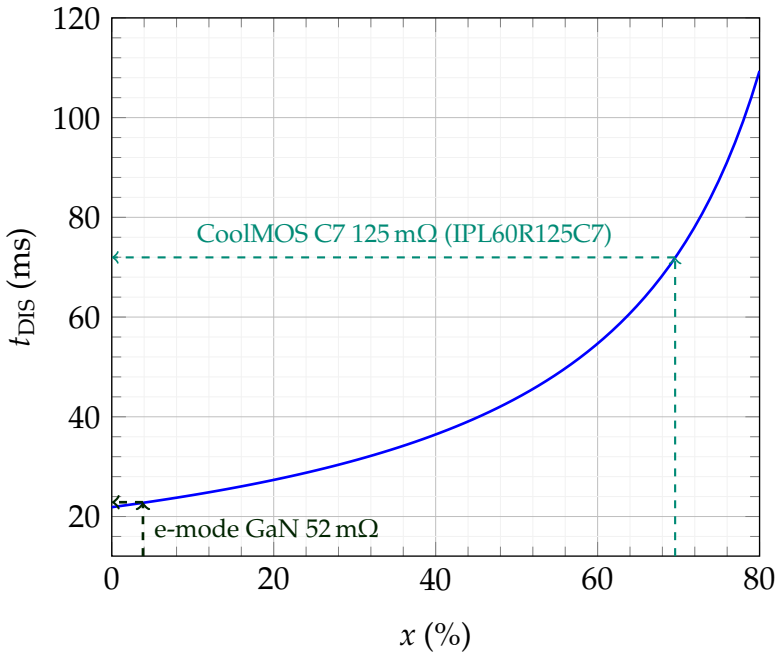


Figure 8.1: Estimated reverse power flow discharge time for versus ratio x.

By using the parameter $C_{\mathrm{O(tr)}}$ (an approximation of a device's effective C_{OSS}) the theoretical t_{DIS} for other devices can be estimated by comparing their $C_{\mathrm{O(tr)}}$ to that of the device used in *SSCF2*, and then inferring the time necessary to re-charge the new $C_{\mathrm{O(tr)}}$ to find the resulting peak currents to re-calculate x. With this method an estimate for the t_{DIS} of an e-mode GaN HEMT has been added to Fig. 8.1. Although any parasitic effects of the coupled inductor have not been considered here, Fig. 8.1 indicates that the e-mode GaN HEMT device has an x of 4 % and thus t_{DIS} could be around seventeen times faster, despite using the same F_{RPF} and $t_{\mathrm{NEG(R)}}$.

Abbreviations and Symbols

Abbreviations

Abbreviation	Definition
COT	Constant-ON-time
VOT	Variable-ON-time
VF-VOT	Variable-Frequency Variable ON-time
SSCF	Secondary Side Controlled Flyback
SMPS	Switched Mode Power Supply
ZVS	Zero-voltage-switching
Q-ZVS	Quasi-zero-voltage-switching
CM	Common mode
DM	Differential mode
RPF	Reverse Power Flow
EMI	Electromagnetic interference
MOSFET	Metal oxide semiconductor field effect transistor
FPGA	Field-programmable gate array
GaN	Gallium Nitride
SiC	Silicon Carbide
IC	Integrated Circuit
PCB	Printed Circuit Board
Pri.	Primary
Sec.	Secondary
Sync. Rec.	Synchronous Rectification
Cap.	Capacitor

Symbols

Component / Parameter Symbol	Unit	Description
$C_{\text{DC-link}}$	F	Primary side capacitance
C_{IN}	F	Alternative (more general) term for $C_{\text{DC-link}}$
C_{OUT}	F	Secondary side capacitance
C_{OSS}	F	Parasitic output capacitance
$C_{\text{OSS(S1)}}$	F	Primary side switch parasitic output capacitance
$C_{\text{O(tr)}}$	F	Effective parasitic output capacitance
C_{Sn}	F	RCD snubber capacitance
C_1	F	Capacitor for $V_{\text{DS(S1)}}$ sensing
C_2	F	Capacitor for $V_{\text{DS(S1)}}$ sensing
C_3	F	Capacitor for $V_{\text{DS(S1)}}$ Q-ZVS sensing
C_4	F	Capacitor for $V_{\text{DS(S1)}}$ Q-ZVS sensing
C_5	F	Capacitor for $V_{\text{DS(S1)}}$ Q-ZVS sensing
C_6	F	Capacitor for $V_{\text{DS(S2)}}$ sensing
D_{Sn}	-	RCD snubber diode
D_0	-	Synchronous rectifier diode
D_1	-	Diode for $V_{\text{DS(S1)}}$ sensing
D_2	-	Diode for $V_{\text{DS(S1)}}$ sensing
D_3	-	Zener Diode for $V_{\text{DS(S1)}}$ sensing
D_4	-	Diode for $V_{\text{DS(S2)}}$ sensing circuit
D_5	-	Diode for $V_{\text{DS(S2)}}$ sensing circuit
$E_{\text{C}_{\text{OUT}}}$	J	Energy stored in output capacitance C_{OUT}
$E_{\text{NEG(R)}}$	J	Energy from reverse power flow pulse
$E_{\text{POS(R)}}$	J	Energy returned after reverse power flow pulse
F_{LOWER}	Hz	Lower switching frequency limit
f_{R}	Hz	Instantaneous request switching frequency
f_{REF}	Hz	Reference switching frequency (variable)
F_{REF}	Hz	Reference switching frequency (constant)
F_{RPF}	Hz	Reverse power flow switching frequency
f_{S}	Hz	Switching frequency
$f_{\text{S(max)}}$	Hz	Maximum switching frequency
i_{d}	A	Drain current

i_{L1}	A	Primary side inductor current
i_{L2}	A	Secondary side inductor current
$I_{L2(NEG)}$	A	Negative current from reverse power flow pulse
$I_{L2(POS)}$	A	Positive current after reverse power flow pulse
I_{NEG}	A	Negative current for turn-ON request
i_{OUT}	A	Output current
k	-	Coupling factor between L_1 and L_2
L_1	H	Primary side inductance
L_2	H	Secondary side inductance
N	-	Turns-ratio of N_1 to N_2
N_1	-	Number of primary side windings
N_2	-	Number of secondary side windings
P_{IN}	W	Input power
P_{loss}	W	Power loss
P_{neg}	W	Power consumed by turn-ON requests
P_{rated}	W	Rated output power
$Q_{C_{OSS}}$	C	Parasitic output charge
Q_{OUT}	V	Output voltage sensing comparator
Q_{PRI}	V	Primary side V_{DS} sensing comparator
Q_{qzvs}	V	$V_{DS(S1)}$ sensing comparator for Q-ZVS
Q_{slope}	V	Comparator for $V_{DS(S1)}$ slope detection
Q_{SOFT}	V	Comparator for soft turn-ON requests
Q_{SR}	V	$V_{DS(S2)}$ sensing comparator
R_{Sn}	Ω	RCD snubber resistance
R_1	Ω	Resistor for $V_{DS(S1)}$ sensing
R_2	Ω	Resistor for $V_{DS(S1)}$ sensing
R_3	Ω	Resistor for $V_{DS(S2)}$ sensing circuit
R_4	Ω	Resistor for V_{OUT} sensing circuit
R_5	Ω	Resistor for V_{OUT} sensing circuit
R_6	Ω	Resistor for $V_{DS(S1)}$ Q-ZVS sensing
R_7	Ω	Resistor for $V_{DS(S1)}$ Q-ZVS sensing
R_8	Ω	Resistor for $V_{DS(S1)}$ slope sensing
R_9	Ω	Resistor for $V_{DS(S2)}$ sensing
R_{10}	Ω	Resistor for soft turn-ON request sensing
R_{11}	Ω	Resistor for soft turn-ON request sensing

S_{SF}	-	Source follower MOSFET
S_1	-	Primary side Flyback switch
S_2	-	Secondary side Flyback switch
$T_{desired}$	s	Desired switching period
t_{DIS}	s	Total reverse power flow discharge time
t_{iL1}	s	Time of positive i_{L1} after reverse power flow pulse
$T_{iL1(REF)}$	s	Reference t_{iL1} set by initial t_{iL1}
T_{LOWER}	s	Lower ON-time limit
T_{NEG}	s	Negative current ON-time for turn-ON request
$t_{NEG(R)}$	s	ON-time for reverse power flow discharge pulses
t_{ON}	s	Variable ON-time for VOT & VF-VOT
T_{ON}	s	Constant ON-time for COT
T_{RPF}	s	Reverse power flow switching period
T_S	s	Switching period (constant)
t_S	s	Switching period (variable)
T_{UPPER}	s	Upper ON-time limit
t_{wait}	s	Time between sync. rec. and turn-ON request
U_{grid}	V	AC input voltage source
U_{REF}	V	Reference voltage for V_{OUT} comparator circuit
U_{SF}	V	Gate voltage supply for S_{SF}
U_{slope}	V	Reference voltage for $V_{DS(S1)}$ slope sensing
U_{SOFT}	V	Reference voltage for soft turn-ON requests
U_q	V	Reference voltage for Q-ZVS $V_{DS(S1)}$ sensing
U_1	V	Reference voltage for $V_{DS(S1)}$ sensing
$V_{DC\text{-}link}$	V	Voltage across DC-link capacitor $C_{DC\text{-}link}$
$V_{DC\text{-}link(min)}$	V	Minimum expected $V_{DC\text{-}link}$
$V_{DC\text{-}link(min)}$	V	Maximum expected $V_{DC\text{-}link}$
V_{DS}	V	Drain-source voltage
$V_{DS(S1)}$	V	Primary switch drain-source voltage
$V_{DS(S2)}$	V	Secondary switch drain-source voltage
V_{GS}	V	Gate-source voltage
$V_{GS(th)}$	V	Gate-source threshold voltage
V_{IN}	V	Input voltage from U_{GRID}
V_{OUT}	V	Output voltage
V_{rated}	V	Rated output voltage
x	-	Ratio of $E_{NEG(R)}$ to $E_{POS(R)}$

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Appendix A

List of Experimental Equipment

This appendix details the equipment used to make the measurements given throughout the thesis. The measurements corresponding to each piece of equipment are also listed.

All switching frequencies and times were inferred using waveforms on the *LeCroy HDO 6104-MS* oscilloscope and all efficiency measurements were performed using the FLUKE Norma 5000 power analyzer. Tab. A.1 lists the measurement equipment used. All voltage and current measurements presented in this thesis are listed in Tab. A.2 along with the corresponding probes used in conjunction with the *HDO 6104-MS*.

Table A.1: Experimental equipment.

Type	Company	Instrument	Key Spec's
Passive Voltage Probe	*LeCroy*	PP008	400 V_{RMS}
Differential Voltage Probe	*LeCroy*	ADP305	1400 V
Differential Voltage Probe	*LeCroy*	ZD200	± 20 V
Current Probe	*LeCroy*	CP031	± 30 A
Digital Signal Probe (16 Ch.)	*LeCroy*	MSO-DLS-001	± 30 V
Oscilloscope (4 Ch.)	*LeCroy*	HDO 6104-MS	2.5 GS/*s*
Power Analyzer (6 Ch.)	*FLUKE*	Norma 5000	-
AC Voltage Supply	*iTech*	IT7321	300 V_{RMS}, 300 W
DC Voltage Supply	*AIM-TTI*	EX453RD	35 V

Table A.2: Measurements and corresponding probes.

Fig.	PP008	ADP305	ZD200	CP031	MSO-DLS-001
5.2	Q_{PRI} , $V_{\text{GS(S1)}}$	$V_{\text{DS(S1)}}$	-	-	-
5.11	-	$V_{\text{DS(S1)}}$	-	i_{L2}	-
5.12	V_{OUT}	-	-	i_{L2}	-
5.13	$V_{\text{DS(S2)}}$	$V_{\text{DS(S1)}}$	*Gate* , *Comp*	-	-
5.17	-	$V_{\text{DS(S1)}}$	*Gate* , *Comp*	-	-
5.15	-	$V_{\text{DS(S1)}}$	*Gate* , *Comp*	-	-
5.16	-	$V_{\text{DS(S1)}}$	*Gate* , *Comp*	-	-
5.18	V_{OUT}	$V_{\text{DS(S1)}}$	-	-	-
5.19	-	$V_{\text{DS(S1)}}$	$Gate_{SEC}$	-	-
6.12	Q_{slope} , Q_{qzvs}	$V_{\text{DS(S1)}}$	-	i_{L2}	-
6.13	Q_{slope} , Q_{qzvs}	$V_{\text{DS(S1)}}$	-	i_{L2}	-
6.14	V_{OUT} , Q_{SR}	-	-	i_{L2}	-
6.15	V_{OUT} , Q_{SR}	-	-	i_{L2}	-
6.16	-	$V_{\text{DS(S1)}}$	-	i_{L2}	-
6.17	-	$V_{\text{DC-link}}$	-	i_{L2}	-
6.18	V_{OUT}	-	-	i_{L2}	-
6.19	V_{OUT}	-	-	i_{L2}	-
6.20	-	-	-	i_{L2}	-
6.21	V_{OUT}	-	-	i_{OUT}	-
6.22	-	-	-	i_{OUT} , i_{L2}	-
7.1	$V_{\text{DS(S2)}}$	-	-	i_{L1} , i_{L2}	-
7.3	$V_{\text{DS(S2)}}$	-	-	i_{L1} , i_{L2}	Q_{OUT} , Q_{SOFT} , S_2
7.7	-	$V_{\text{DC-link}}$	-	-	-
7.8	-	$V_{\text{DC-link}}$	-	-	-
7.9	-	$V_{\text{DC-link}}$	-	-	-
7.14	-	$V_{\text{DS(S1)}}$	-	i_{L1} , i_{L2}	S_1 , S_2
7.15	V_{OUT}	-	-	i_{L2}	-