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System Level Reliability Testing Under Application Stress Conditions

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Abstract

Power semiconductors are exposed to thermo-mechanical stress during their functional use in application. The stress occurs due to *power cycling* and *thermal cycling* of the device, which results in its aging, and eventually the device will fatigue and may ultimately fail. Hence, reliability characterization of power semiconductor devices is of paramount importance during the development of new devices. To improve the reliability and operating safety of power electronic systems, knowledge about aging mechanisms and failure mechanisms is crucial. Performing *life tests* on power semiconductors requires significant development effort for a test apparatus to provide the required functionality.

This work presents a Modular Test System (MTS) architecture which focuses on flexibility, reusability and adaptability for future test requirements. It discusses essential requirements for performing sophisticated life tests. Different types of tests for different devices which are all implemented based on the same MTS concept, are introduced. Specifically, the distinction between *device-* and *application-specific* types of hardware setup, is explained. Vital parameters of the Device Under Test (DUT) can be acquired *in situ* during the running stress test. This enables the collection of drift data of these parameters. The control and data acquisition parts of the test system are clearly separated from the actual test circuit. With this physical separation, the same control unit can be used for different types of tests.

In addition, two examples of realized test systems which are based on the MTS concept are comprehensively illustrated. The first example demonstrates a test system which has an *application-specific* hardware setup for power transistors which are used for step-down DC/DC conversion. The design and functionality of the different module parts are introduced, the system's construction is explained, and measurement results from selected test runs are presented.

The second example introduces a *device-specific* hardware setup. Here, an advanced control module which is designed to fit into the MTS architecture is presented, which improves the performance of High Temperature Operating Life (HTOL) qualification

tests by the implementation of a novel embedded system. The implementation of a prototype test system and measurement results of an evaluation test run are presented in detail.

The continuous acquisition of digitized measurement data of analog signals is a common task in life test systems. A vast amount of data is produced and stored for later analysis. Life test data commonly comprise long data sets during which the monitored signals are constant or increase rather slowly but steadily. In this work, three approaches are proposed to reduce the size of the measured data and to filter for relevant information.

The last part of this work presents an overview and discussion on all realized test systems which have a *centralized* or *modular* architecture for the execution of *device-* or *application-specific* life tests. Next, guidance on aspects that should be addressed in the development of new modular life test systems is provided. In the end, an outlook is given for which further test systems based on the MTS-architecture are planned in the future.

Zusammenfassung

Leistungshalbleiter sind bei der Nutzung in ihrer Zielanwendung thermisch-mechanischem Stress ausgesetzt. Der Stress entsteht durch das Leistungs- und Temperaturzyklen des Bauteils, welches dadurch altert und letztendlich ermüdet und dann ausfällt. Daher sind Zuverlässigkeitsuntersuchungen an Leistungshalbleiterbauteilen während der Entwicklung von neuen Bauteilen von höchster Bedeutung. Um die Zuverlässigkeit und Betriebssicherheit von leistungslektronischen Systemen zu verbessern, ist es entscheidend, Kenntnisse über Alterungs- und Fehlermechanismens zu haben. Die Durchführung von *Lebensdauertests* an Leistungshalbleitern erfordert einen erheblichen Entwicklungsaufwand an das Prüfsystem, um die benötigte Funktionalität zu erhalten.

Die hier vorliegende Arbeit präsentiert eine modulare Testsystem (MTS) Architektur, welche den Fokus auf Flexibilität, Wiederverwendbarkeit und Anpassungsmöglichkeit an zukünftige Testanforderungen legt. Es werden essentielle Anforderungen für die Durchführung von hochentwickelten Lebensdauertests diskutiert und verschiedene Testtypen für verschiedene Bauteile, welche alle auf demselben MTS Konzept basierend implementiert sind, vorgestellt. Namentlich unterscheidet man zwischen *bauteil-* und *applikations-spezifischen* Arten von Hardwareaufbauten. Vitalparameter des Prüflings (DUT) können *in situ* während des laufenden Tests aufgezeichnet werden, was die Erfassung von Driftdaten dieser Parameter ermöglicht. Die Steuer- und Aufzeichnungselemente des Testsystems sind von der eigentlichen Testschaltung klar getrennt. Diese physikalische Trennung ermöglicht die Wiederverwendung derselben Steuerelemente für andere Testarten.

Darüber hinaus werden Beispiele von zwei realisierten Testsystemen, welche auf dem MTS Konzept beruhen, umfassend vorgestellt. Das erste Beispiel zeigt ein Testsytem mit einem *applikations-spezifischen* Hardwareaufbau, welches zum Testen von Leistungstransistoren für Gleichspannungswandler verwendet wird. Der Aufbau und die Funktion der verschiedenen Hardwaremodule werden vorgestellt, der Aufbau des Gesamtsystems wird erklärt, und Messergebnisse von ausgewählten Lebensdauertests werden präsentiert.

Im zweiten Beispiel wird ein *bauteil-spezifischer* Hardwareaufbau vorgestellt, der ein neuartiges Steuermodul, welches kompatibel zur MTS Architektur ist, verwendet. Es erhöht die Funktionalität bei der Durchführung von HTOL-Tests durch den Einsatz eines innovativen eingebetteten Systems. Die Realisierung eines Prototypen-Testsystems und die Messergebnisse eines damit durchgeführten Verifizierungstests werden detailliert beschrieben.

Die fortlaufende digitalisierte Aufzeichnung von Messdaten aus analogen Signalen ist eine häufig vorkommende Funktion in Lebensdauertestsystemen, welche eine enorme Datenmenge produzieren und für die spätere Analyse speichern. Lebensdauerdaten beinhalten oft lange Datensätze währenddessen die beobachteten Signale konstant sind oder nur sehr langsam aber kontinuierlich ansteigen. In der hier vorliegenden Arbeit werden drei Methoden vorgeschlagen, um die Menge der aufgezeichneten Daten zu reduzieren, jedoch gleichzeitig die relevante Information zu behalten.

Der letzte Abschnitt dieser Arbeit beinhaltet einen Überblick und diskutiert alle realisierten Testsystemvarianten, sowohl mit *zentraler* und mit *modularer* Architektur, als auch für die Durchführung von *bauteil-* oder *applikations-spezifischen* Lebensdauertests. Danach werden Empfehlungen vorgeschlagen, auf welche Aspekte man bei der Entwicklung von neuen modularen Testsystemen achten sollte. Zu guter Letzt wird eine kurze Vorschau über die zukünftig geplanten Testsysteme, welche auf der MTS-Architektur basieren werden, präsentiert.

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PURSUING a PhD thesis is like exploring new land. You do not know what you will discover and when you will succeed your endeavour.

The most important person who acted as a lighthouse guiding me through the undiscovered land, was my supervisor Prof. Annette Mütze and she is therefore mentioned at first place. I must thank her as she was aiding me from the first day we were introduced, with a clear and precise guideline which steps to take to accomplish the mission. From this first meeting I knew which milestones I must reach and she described the final goal, this work[1], in a rather early stage of my PhD studies. I can say this was of great help for me and Prof. Mütze always motivated me by considering each milestone at the time it was accomplished during the journey.

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To Natalie & Leonard

Motivation

Until the 1960s, quality targets were presumed as reached when the item under consideration was found to be free of *defects* or *systematic failures* at the time it was delivered by the manufacturer [1, p.1]. Due to the growing complexity of Integrated Circuits (ICs) and systems, as well as the costs and downtime in case of a failure, the aspects of *reliability, maintainability, availability*, and *safety* have reached a level of tremendous importance.

> "The expectation today is that complex equipment and systems are not only *free from defects* and *systematic failures* at time $t = 0$ (when they are put into operation), but also *perform* the required function *failure free* for a stated time interval and have a *fail-safe behavior* in the case of *critical* or *catastrophic failures*." [1, p.1]

The question of whether a given item will operate without failures during a stated period of time (*lifetime*) cannot be simply answered by a yes or no. Experience shows that only a *probability* for this occurrence can be given which is ascertained by *statistical analysis* of conducted *life tests*. The acquired lifetime data gained from various life tests can then be analyzed by different *lifetime models*; multiple examples for the latter may be found in [2]–[7]. Desired performance parameters as well as *reliability, maintainability, availability*, and *safety* must be *built in* during design and development and retained during the production and operation of an item [1, p.2].

Power semiconductors are exposed to electrical and thermo-mechanical stress during their functional use in power conversion applications. Dynamic stress occurs due to *power cycling* and *thermal cycling* of the device, which results in its aging, and eventually the device will degrade and may fail. Hence, reliability characterization of power semiconductor devices is of paramount importance during the development of new devices [8]. To improve the reliability and operating safety of power electronic systems [9], knowledge about aging mechanisms and failure mechanisms [10]–[13] is crucial. [1, p.87] states that *qualification tests* – and *life tests* in general – must be supported by intensive *failure analysis* to investigate relevant *failure mechanisms*.

Learn as if you were
to live forever.

(Mahatma Gandhi)

Chapter 1

Introduction

1.1 Scope of Work

In this work, state-of-the-art *life testing* including in situ *condition monitoring* of DUTs in various circuit configurations is introduced. First, an overview of various tests which must be executed by semiconductor manufacturers during development and release of new products is presented. Next, types of automatically executable life tests are introduced and their different properties and aims are explained. This work then proposes a Modular Test System which is designed to meet all the previously explained test requirements and can be relatively easily adjusted to fulfill demands of such *life tests* in the future.

In the respective literature, most reports on reliability testing focus on the behavior of the Device Under Test. Typically, the test systems are designed to analyze the wear-out of *one specific* device under certain stress conditions (e.g., [14], [15]). Only the DUT and life test results of this DUT are focused on. The publications dealing with these systems do not report on any attempt to use the available test hardware in a systematic way for different DUTs, types of tests, or both. In contrast, this work focuses on the design of the test system itself. A *modular* and *distributed* test system architecture is proposed which can be easily adapted to changing test requirements and DUTs and is able to execute all different types of tests which are discussed in this work.

After comprehensively presenting test system variants which are capable of executing life tests on DUTs within an *application-specific* test circuit, the performance enhancement of the MTS to enable the stressing of a high DUT count within an *device-specific* test circuit, is illustrated. This is achieved by introducing an advanced control module which is based on a Field Programmable Gate Array (FPGA)-microcontroller driven

control entity. The high DUT count of 231 devices is needed to execute life tests according to specific JEDEC-standards, e.g., within the HTOL-test [16].

Life test systems continuously produce an enormous amount of data which need to be stored for later analysis. The data commonly comprise long times during which the monitored signals are constant or increase rather slowly but steadily. Hence, three approaches to process and smartly reduce the data down to retain only significant information are investigated.

1.2 Author's Contribution

The author's work is embedded within a greater project, namely EM²APS[1], at Kompetenzzentrum Automobil- und Industrie-Elektronik (KAI), Villach, Austria, which is working on the MTS.

- The author's work within the project focuses on the hardware architecture of the MTS and the development of its individual modules. The control module and the Low Voltage (LV) module which are presented in Chapter 3 were developed by the author and have also been published in [17], [18].

- The FPGA-based control module (Chapter 5) to enable the performance enhancement of the MTS was developed by the author in cooperation with a master's thesis [19], a bachelor's thesis [20] and a further KAI project member (Yevhen Nikitin). Results on this test system variant have also been published in [21].

- The topic addressed on data management and smart reduction was realized in collaboration between another KAI project member (Benjamin Steinwender) and the author.

- The Mid Voltage (MV) module is outside the work of the author, but it matches the MTS architecture and is hence reviewed briefly for the sake of completeness in Section 4.2.1. The MV module has also been published in [22], [23].

- The software framework is elaborated within a separate dissertation in [24] and parts of it have been published in [25], [26].

[1]The EM²APS project was funded by the Austrian Research Promotion Agency (FFG, Project No. 860424).

1.3 Organization of the Thesis

This work is organized as follows:

Chapter 2 first presents an overview of types of tests which must be executed by semiconductor manufacturers during development and release of new products. Then, a classification of the different test configurations and hardware setups which are used for life test systems is proposed. Examples are included of the different test type variants to facilitate a better understanding.

Chapter 3 gives a detailed description of the novel architecture of the MTS. The chapter starts with the distinction between a *centralized* versus a *modular* and *distributed* test system *architecture* and discusses their advantages and disadvantages. Further on, the structure and function of the control and application modules are explained.

Chapter 4 presents multiple available implementations of *application-specific* test systems based on the MTS architecture. The LV test system is treated comprehensively by presenting the fully implemented test system with its various parts and depicting several test results to demonstrate the powerful possibilities of such systems. A method to investigate and improve the measurement accuracy of an MTS is introduced and finally one further (namely the MV) test system is presented in this chapter.

For the execution of qualification tests, like the HTOL test, a high DUT count of – at least 231 – devices is required by the JEDEC specification [16]. The control module introduced in Chapter 4 for the execution of *application-specific* tests is not powerful enough to control so many DUTs in parallel. For this reason, the performance enhancement of the MTS by realization of a novel FPGA-driven control module which is still based on the MTS architecture, is introduced in Chapter 5. Thus, this system variant is designed for *device-specific* test hardware configurations. The implementation of a prototype test system is presented in detail and results of an executed HTOL test, are demonstrated in this chapter.

Chapter 6 addresses a common challenge for life test systems: Due to the continued acquisition of digitized measurement data, a vast amount of data is produced and stored for later analysis. Hence, in this chapter, three approaches are proposed to reduce the size of measured data and to filter for relevant information.

Chapter 7 presents an overview and discussion of all realized test systems which have a centralized or modular architecture for the execution of device- or application-specific life tests. Next, a discussion is given which identifies aspects that should be addressed in the future in the development of modular life test systems. This work concludes with

an outlook on which further test systems based on the MTS-architecture are planned in the future.

1.3.1 Nomenclature of the Test Systems

In this work, three different test systems are discussed which are designed for different voltage classes. These test systems are classified as follows:

- The Low Voltage test system is designed for power transistors with a maximum voltage rating of 60 V and these transistors are typically realized in trench technology [27, pp.63-66].
- The Mid Voltage test system is aimed for stressing of power transistors with a voltage rating of up to 700 V. The used technology for these transistors is superjunction [28, pp.494-513] [29], [30] or Gallium Nitride (GaN) [31], [32].
- With the High Voltage test system, module packaged devices are tested like IGBT and Silicon Carbide (SiC) MOSFET transistors [33], [34] which are operating at a voltage of up to 1.5 kV.
- With the FPGA-based test system, automotive ICs like Smart Power Switches (SPSs) [35], are tested with a maximum voltage specification of up to 100 V.

1.4 Life Testing Requirements

1.4.1 Basic Definitions

Reliability

Reliability is a characteristic of an item, expressed by the *probability* that the item will perform its required function under given conditions for a *stated time interval* [1, p.2]. From a *qualitative* point of view, reliability can be defined as the ability of an item to remain functional. *Quantitatively*, reliability specifies the probability that no operational interruptions will occur during a certain time interval. In general, it is also important to know whether or not an item can be considered new when the life test starts. An *item* is a functional or structural unit of arbitrary complexity (e.g., component, assembly, equipment, subsystem, system) that can be considered as an entity for investigations.

In this work the *item* under consideration is always a semiconductor device which can optionally be tested within *device-* or *application-specific* circuit configurations. The *required function* specifies the item's task. For example, for given inputs, the item outputs must be constrained within specified tolerance bands which are described in the device's *specification datasheet*. The definition of the required function is the starting point for any reliability analysis, as it defines *failures*.

The required function and *operating conditions* can be time dependent. In such cases, a *mission profile* must be defined and all reliability figures will be related to it. Often the mission duration is considered as a parameter t, the reliability function is then defined by $\mathrm{R}(t)$. $\mathrm{R}(t)$ is the probability that no failure at item level will occur in the interval $(0, t)$. The item's condition at $t = 0$ (new or not) influences the final results.

Failure

The *lifetime* t of a considered item is defined as the time span between the initial operation and failure of a non-repairable item. The *failure condition* is clearly identified by a failure criterion, and if triggered, a *failure event* will be recorded. A *failure* occurs when the item stops performing its required function. The *failure-free time* τ (or more detailed the failure-free *operating time*) is generally a random variable. It is often reasonably long, but it can also be very short, for instance because of a failure caused by a transient event at turn on of a power semiconductor device. A general assumption in investigating failure-free times is that at $t = 0$ the item is free of defects and systematic failures.

Failure Rate

The *failure rate* $\lambda(t)$ of an item is the probability of a failure in a defined interval (i.e., the operating time) given that the item was new at $t = 0$. The *failure rate* of a large population of statistically identical *items* exhibits often a typical bathtub curve (Figure 1.1) with the following three phases [1, p.6]:

1. *Early failures:* The *failure rate* $\lambda(t)$ decreases rapidly with time. Failures during this phase are attributable to randomly distributed weaknesses in materials, components, or production processes.

2. *Failures with constant (or nearly so) failure rate:* Here, $\lambda(t)$ is approximately constant and failures in this phase are Poisson distributed.

3. *Wearout failures:* $\lambda(t)$ increases with time. Failures in this period are attributable to aging, wearout, and fatigue (e.g., corrosion, electromigration).

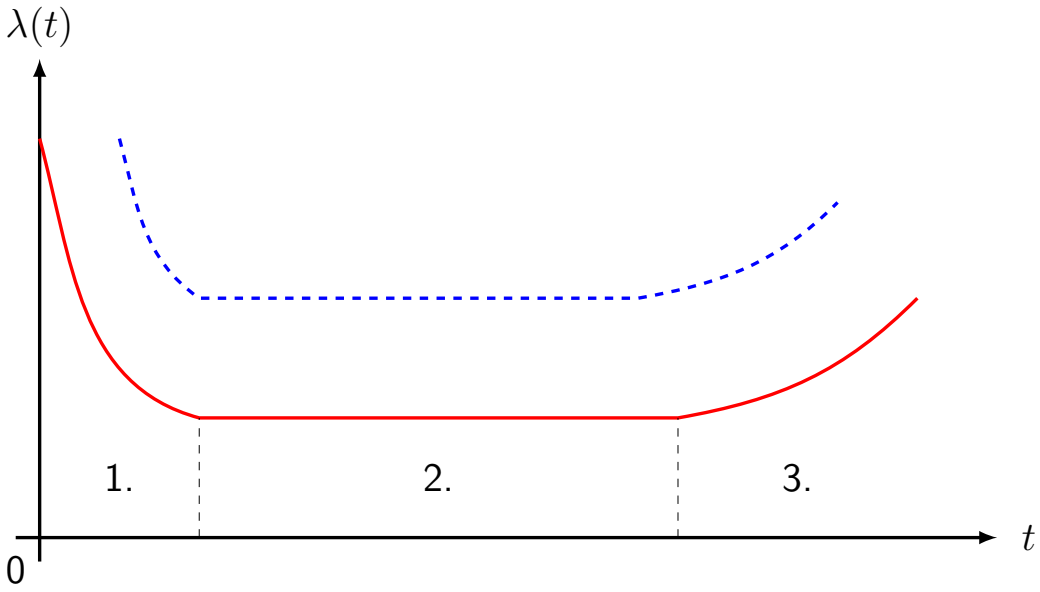


Figure 1.1: In this figure, the typical shape is depicted (commonly denoted as "*bathtub curve*") for the failure rate of a large population of statistically identical *items*. The blue dashed curve shows a possible shift for a higher stress (e.g., increased ambient temperature) [1, p.7].

To simplify calculations, reliability prediction is often performed by assuming a *constant failure rate* (as in 2. in the list above) during the *useful life* [1, p.35]

$$\lambda(t) = \lambda \tag{1.1}$$

This approximation greatly simplifies calculation, since a constant *failure rate* leads to a flow of failures described by a homogeneous *Poisson process*. In this case the *failure-free time* τ is exponentially distributed [1, p.356]. Thus, the *failure rate* λ can be determined by

$$\lambda = \frac{k}{T} \tag{1.2}$$

where T is the operating time and k is the number of failures during T. Another commonly used term in this context is the Mean Time To Failure (MTTF) which relates to the *failure rate* as follows:

$$MTTF = 1/\lambda \tag{1.3}$$

A comprehensive introduction of the terms *failure rate* and MTTF may also be found in [1, pp.4-6]. *Operating conditions* have an important influence on reliability, and hence must be specified with care. E.g., [1, p.3] states, that the *failure rate* of semiconductor devices will double for an operating temperature increase of 10 K to 20 K.

Failure Classification

Failures should be classified (as far as possible) according to the mode, cause, effect, and mechanism [1, pp.3-4].

- *Mode:* The *mode* of a failure is the *symptom* (local effect) by which a failure is observed. For power electronic components, these are: *opens* (no function, open circuit), *shorts* (no blocking capability, short circuit) or *drift* of logged device parameters.

- *Cause:* The *cause* of a failure can be *intrinsic* due to wear-out or *extrinsic*, due to errors, misuse or mishandling during design, production, or use. Extrinsic causes often lead to systematic failures which are deterministic and should be considered as *defects*. *Defects* are present at $t = 0$, even if they cannot be discovered at $t = 0$. In contrast, failures appear always in time, even if the time to failures is short as it can be with systematic or early failures.

- *Effect:* A common classification is as follows: non relevant, partial, complete, and critical failure. Since a failure can also cause further failures, distinction between *primary* (original) and *secondary* (caused by primary) failure is important.

- *Mechanism:* Failure *mechanism* is the physical, chemical or other process resulting in a failure. Further detailed information on failure mechanisms can be found in [1, p.102ff].

1.4.2 Requirements Definition

A *life test system* usually consists of several test channels to stress the DUTs in parallel. [1, p.87] states that the number of devices required for reliability tests should be determined in order to expect three to six failures during *burn-in*. However, experience from life tests at KAI shows that the number of devices to be investigated in parallel also depends on the type of test: For HTOL tests, at least 231 DUTs are required by [16]. End of Life (EOL) tests on individual semiconductor devices typically use a lower number of DUTs (e.g., 64 DUTs as in [36]). Application specific EOL tests, in which a complete circuit is built up per each test channel and are hence significantly more complex, may, as in our example, stress up to 24 DUTs [18], [23].

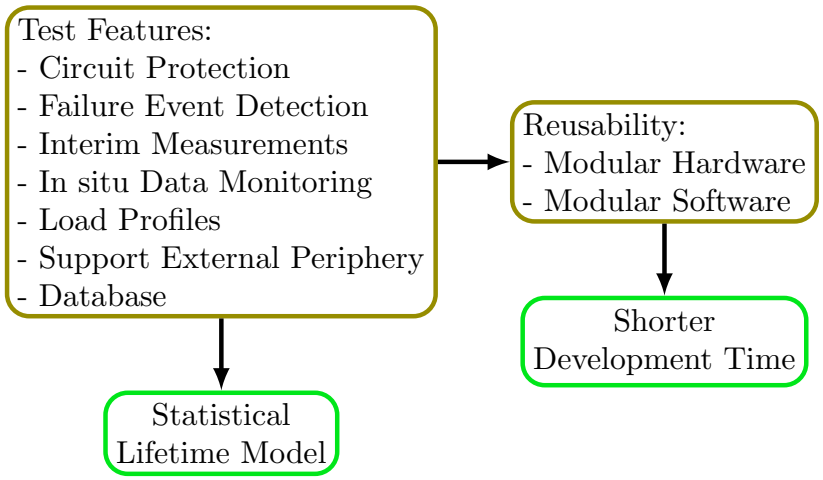


Figure 1.2: Essential features for life test systems are listed which are necessary to gather statistical analyses out of test runs. Re-usage of available test hardware and software is reasonable to provide flexibility, adaptability and future-proofness to various test applications and device requirements and to shorten the development time.

Life Test Features

In Figure 1.2 the mandatory features which state-of-the-art life test systems must provide are depicted and in the following, detailed explanations of them are given.

The main power line to the DUT or application test circuit is equipped with a *circuit protection* (also termed *guard switch*) which is operated by a control entity. This entity continuously monitors the input current during the test and shuts down the respective test channel at an overcurrent event which may usually be triggered by a broken DUT.

The time instant of this event is subsequently logged. This is a mandatory feature for an EOL test system to protect the test circuit from damage and it is denoted as *failure event detection*. Furthermore, this feature also reduces the energy imposed into the DUT after a short circuit event. Thus, the destruction to the DUT is less severe and this fosters the further investigations on the failure root case.

Such an overcurrent shut down is more generally termed a *hard* failure event. For HTOL tests, the situation is less strict, since the test parameters are set to run the DUTs in nominal operating conditions. In traditional HTOL test systems, a fuse is typically used to protect the main power line. An advanced test system may also use a guard switch for HTOL test systems.

In addition to such hard failure events, *soft* failure events (e.g., an open load condition, at which the DUT no longer turns on) may also arise. In contrast to hard failures which demand a mandatory shut down, the time-instant for soft failures is logged, but the respective DUT continues the test. So, the case may occur in which one DUT initially shows a soft failure and after further testing time, a hard failure, as well.

A *test failure* is a failure event falsely logged by the control entity while the DUT may still be fully functional. This situation may occur in the case of a test hardware malfunction or if a failure criterion is not set correctly (e.g., an overcurrent limit is set too low).

Interim measurements, also referred to in literature as *condition monitoring* [37]–[41], are required for HTOL tests [16]. These measurements can be realized in situ and, if desired, continuously during the running life test by the test system proposed herein. For *application-specific* tests, individually adjustable *load profiles* can be applied to the output of the test circuit, allowing for the investigation of different *mission profiles* [42], [43]. To enable individual load profiles, the control entity must be capable of operating *external periphery* devices such as power supply and electronic load devices.

To facilitate the collection of life time data for further statistical analysis, a system must provide possibilities to directly record the test events to a dedicated *database*. Test events may also be fed to the database manually with the advantage that test failures can be rejected before filling the database. After the stress test is terminated, the test data needs to be statistically analyzed. A *statistical model* to predict the DUTs lifetime may be derived from the test results by means of Bayesian modeling, as explained in detail in [3].

A likewise essential prerequisite for working with modular hardware is to also provide a *modular software*. The software framework which is used with the MTS is introduced

in detail in [24], [26]. However, for the purpose of HTOL testing, a new embedded system is required for performance enhancement of the MTS, which will be described in Chapter 5.

Chapter 2

Classification of Types of Tests

This chapter first presents an overview of types of tests which must be executed by semiconductor manufacturers during development and release of new products. Next, a classification of the different test configurations and hardware setups which are used for life test systems is proposed. Examples are included of the different test type variants to facilitate a better understanding. Furthermore, similar test systems found in literature are discussed for comparison and distinction of this work.[1]

2.1 General Overview of Types of Tests

At first glance, the various types of tests which must be executed by a semiconductor manufacturer, and some also by its customers, are explained from an elevated perspective. Figure 2.1 shows all necessary tests and provides a classification concerning the implementation and stress level of each test. The blue boxes indicate types of tests which are run by automated life test systems and hence fall within the scope of this work.

For the classification, we distinguish on the one hand the *implementation level* of the Unit Under Test (UUT). Either the device (*device-specific test*) is in focus of the investigation or the device within its application (*application-specific test*) and even the system as a whole may be tested (*field application test*).

On the other hand, the test can be classified by the *stress level* which is imposed on the DUT. In the low range of Figure 2.1, tests are performed in a manner so that the DUT is fully functional at test end. At higher stress level during End of Life tests, the DUT will fail and here the *time to failure* is the parameter under investigation.

[1] Parts of the content of this chapter have also been presented in [18] and [21].

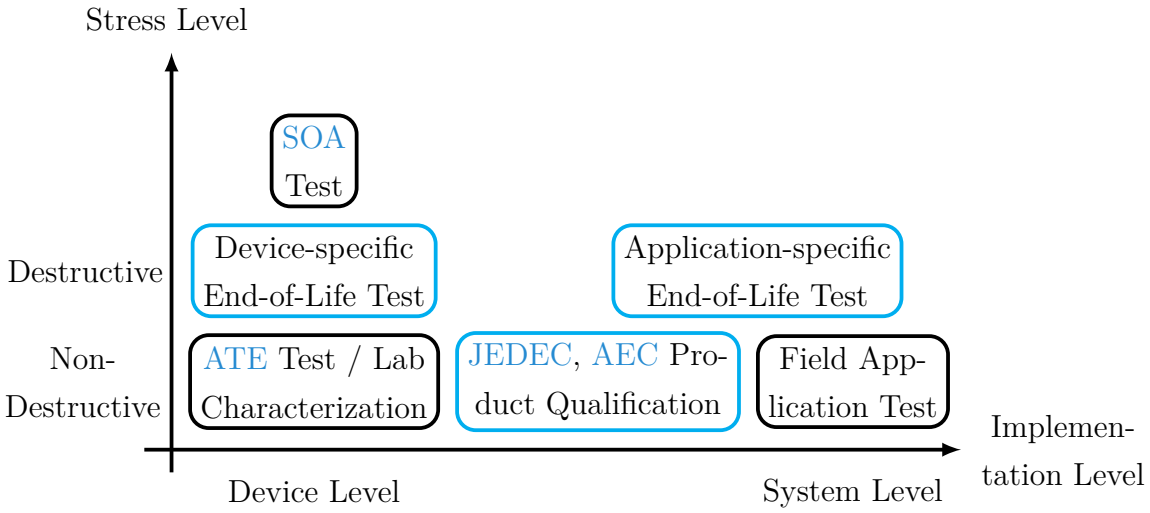


Figure 2.1: General overview of various types of tests which must be performed in the semiconductor industry. Blue boxes indicate tests which are run by automated life test systems and are in focus of this work.

In *Safe Operating Area (SOA) tests*, the stress level is increased step-wise to provoke the device failure rapidly. Repeating this test with various voltage/current combinations, the SOA of a DUT is determined and this information, derated by some safety margin, is normally published in the respective datasheet.

Automated Test Equipment (ATE) tests are performed by specialized equipment where single semiconductor devices are tested for their proper functionality. These tests normally run at high speed and at a high volume of DUTs, as every semiconductor device must be tested by ATE after production. Thus, for this type of test, the functionality of the DUT is checked immediately upon completion, but no aging or wear-out phenomena. ATE tests are executed on device level and clearly have a *non-destructive* purpose. Hence, these types of tests fall outside the scope of this work and are only mentioned for the sake of completeness.

Laboratory characterization tests belong to the same category as ATE tests, because they are also executed on device level and normally have a *non-destructive* aim. Laboratory tests are executed on special request and investigate whether designed device parameters match the properties of the real manufactured DUT. Thus, these tests accompany the development phase of a semiconductor device and are commonly executed on intermediate design steps.

Field application tests are typically executed by application manufacturers (which are customers of the semiconductor manufacturer) as they are interested in the reliability

of the system. Here, the whole system is put into an environmental chamber and tested in an exact application configuration. As only few parameters can be monitored in such a configuration, this method allows only limited relevant information to be gained on the devices' and system's life performance.

2.2 Test Types for Life Testing

In the following, test types are introduced which fall within the focus of this work. These are the tests in the blue boxes in Figure 2.1 which have several properties in common and can all be executed by the MTS introduced in Chapter 3. These common properties are:

- DUTs are stressed in parallel and under elevated or lowered ambient temperature.
- The *time to failure* or *all devices survived* are the possible results of the life test.
- Typically high electric power is injected into the DUT and a nominal or high power load is connected to the output.
- Vital parameters are acquired and logged continuously during the entire test run.
- As the life tests run over a long time period (i.e., 1000 h and longer), the test sequence shall be executed automatically.

Hence, the tests in the blue boxes in Figure 2.1 may be distinguished from each other by their hardware and software settings, but can be unified within the common MTS architecture.

This leads to the perspective which is depicted in Figure 2.2: It presents an overview of the different types of life tests which are all executable by the MTS and are only distinguished from each other by hardware and software properties.

Non-destructive tests and *destructive tests* differ in the *stress level* imposed on the DUTs which is adjustable by software. Furthermore, these test types also differ in the run time (typical 1000 h versus EOL). The terms *device-specific* versus *application-specific test* relate to the *hardware setup* of the test system. A life test is always a combination of a software configuration and a hardware setup.

Device-specific test setups are typically conducted with both *non-destructive* and *destructive* test configuration. However, *application-specific* test setups are normally

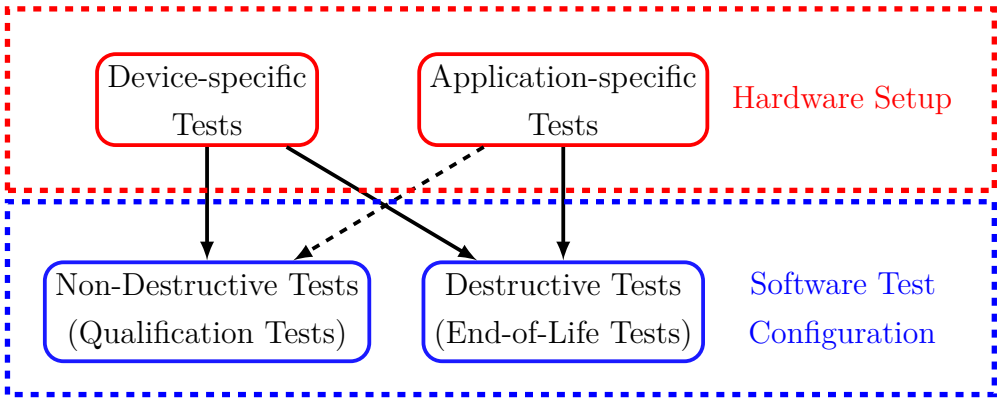


Figure 2.2: Various types of life tests which are all executable by the MTS. Which of their properties are set by hardware or software, is depicted.

used for *destructive tests* under accelerated stress conditions (i.e., elevated voltage and/or current and/or temperature), although both test configurations would be possible.

Application-specific test setups are halfway between *device-specific* tests and *field application tests*. *Application-specific* tests are realized with the DUT embedded within an *application-specific* test circuit which is similar to a *field application* test, but with the benefit that sense lines are designed into the test circuit to monitor vital parameters during life test runs, as well as protection circuits to avoid catastrophic destruction of the test setup in case of a DUT failure. Thus, the robustness of a DUT within its designated application can be well investigated by an *application-specific* test setup. However in this test setup, the exact root cause of a DUT failure cannot be typically determined. Hence, it is reasonable to additionally submit the DUT to *device-specific* tests to unveil the failure cause in detail.

The types of tests shown in the blue boxes of Figure 2.1 can be assigned to the setups and configurations depicted in Figure 2.2 as follows:

- Device-specific EOL = *device-specific* test with *EOL* software setting
- JEDEC/AEC product qualification = *device-specific* test with *non-destructive* software setting
- Application-specific Test = *application-specific* test with *EOL* software setting

In the following, the test types for life testing are comprehensively introduced and examples of test systems are explained.

2.2.1 Non-Destructive Tests

These tests are typically performed within a semiconductor manufacturer company to prove the devices' reliability under JEDEC- / AEC-standard conditions and eventually to bring new devices on the market. Non-destructive tests are also denoted as *qualification tests* and according to [1, p.87] they are often a part of a *release procedure*. The purpose of a *qualification test* is to verify the *suitability* of a given item (or device) for a stated application. Additionally, periodic *re-qualification* of critical parameters is often necessary to monitor quality and reliability. Qualification tests are described in various standards, e.g., JEDEC [16], [44], [45], AEC [46].

A specific type of qualification test is the HTOL test. The JEDEC standard states that the DUTs are biased[2] and run in a dynamic operating mode.

> "Several input parameters may be adjusted to control internal power dissipation. These include: supply voltages, clock frequencies, input signals, etc., that may be operated even outside their specified values, but resulting in predictable and non-destructive behavior of the devices under stress. The particular bias conditions should be determined to bias the maximum number of potential operating nodes[3] in the device." [16]

In HTOL tests, the DUTs should be stressed at an elevated temperature. The standard [16] further states that the minimum junction temperature of the DUTs should be +125 °C unless otherwise specified for extended use or other environments. The set of DUTs shall be composed of 77 pieces from at least three different and nonconsecutive lots. The HTOL test is performed for 1000 h [45, p.11] and subsequently, the functionality of all the devices is proven through additional measurements. The HTOL is only considered as passed, if *all* 231 tested devices still fulfill all parameter ranges defined in the datasheet specification.

Interim measurements are also specified within the standard and are usually performed outside the test system, thus increasing the overall test duration. Typically, legacy test systems for these types of tests do not offer automatic failure event detection.

[2] In the context of this JEDEC standard, *biased* means that the DUTs are supplied and operated according to their target application.

[3] In the context of this JEDEC standard, *operating nodes* describe the features which the IC offers. E.g. for an automotive four channel low-side multi-switch IC, all four load channel must be stressed in the HTOL test.

2.2.2 Destructive Tests

These tests are also denoted as EOL tests [6]. The JEDEC standard states that these tests are

> "...capable of stimulating and precipitating semiconductor device and packaging failures. The objective is to precipitate failures in an accelerated manner compared to use conditions." [45]

The bias input supply voltage is set to the maximum level specified for the DUT while still complying with the datasheet specification. A high stress, i.e., a high load current, is impressed on the device, possibly in an intermittent manner, typically to reach the maximally allowed junction temperature (T_j). For these tests, it is essential to log the failure event time, so as to be able to later elaborate lifetime models by means of a statistical analysis [5]–[7], [47]. Moreover, the aim of destructive tests is to study the wear-out of semiconductor power devices by monitoring significant changes in specific device parameters [48]–[51] until the devices fail.

2.2.3 Device-Specific Tests

In a *device-specific* test, the DUT is submitted to a certain stress in a simple test configuration, where a high number of DUTs (typically 64 and more) is stressed in parallel. This test focuses on the DUT's proper functioning and its parameters which are compared to the limits of the target specification. The *device-specific* test is performed on both types of test settings, the *non-destructive* and the *destructive* test. In the following two subsections, examples are presented of realized *device-specific* test setups with *destructive* test configuration. A corresponding example of a novel *device-specific* test setup with a *non-destructive* test configuration is provided in Chapter 5.

Automotive Repetitive Short Circuit Testing

This test is designed to stress SPSs [35], used in automotive applications. SPSs, like the Infineon PROFET™ [53], [54] (see block diagram in Figure 2.3), are equipped with integrated driving, protection and diagnostic functions. In automotive applications, such SPSs have taken the place of electromechanical relays for switching all kinds of electric loads, such as incandescent bulbs, solenoids and motors [55]. Protection against electric and thermal overload, a common feature of SPSs, is usually based on overcurrent

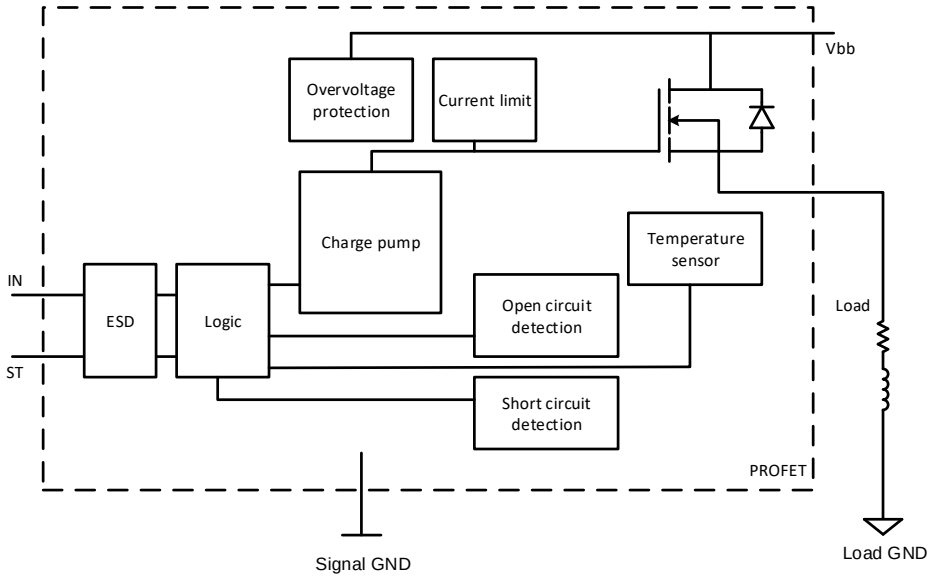
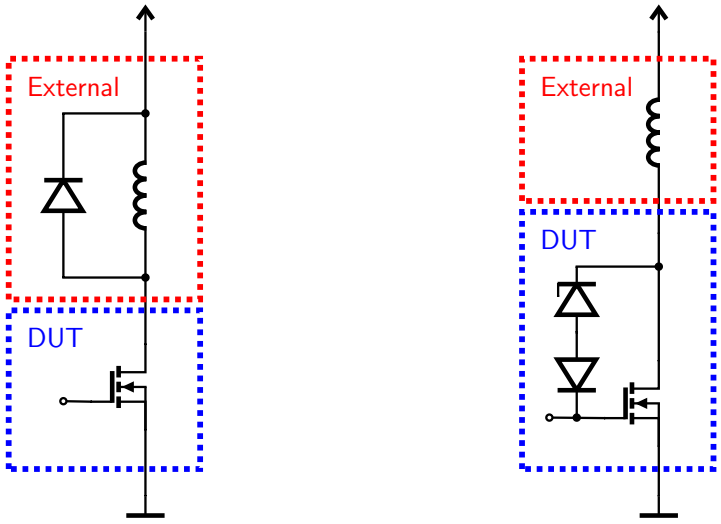


Figure 2.3: The block diagram [52] shows the circuit parts of an Infineon PROFET™device. The main function of the IC is the high-side power transistor which switches various (resistive and/or inductive) loads in automotive applications. Additionally, it is equipped with protective functions like overvoltage protection, current limiting and temperature sensing. In case of a fault condition within the application, it will shut down the power transistor and provide a status feedback.

detection and limitation, junction temperature sensing and protective shut down, if electrical or thermal maximum ratings, or both, are exceeded [56].

The AEC standard AEC-Q100-012 [57] defines the test procedures for repetitive short circuit characterization, including test circuit configuration, ambient temperature and impedances. A test system designed to perform stress on SPSs has been proposed in [36], however it has a centralized and inflexible architecture. The source and load side impedances are selectable by passive components (i.e., air coils and power resistors). These impedances emulate the cable harness in a car. The DUTs are turned on in short circuit condition. The SPS limits the load current and eventually shuts down when the DUT's junction temperature T_j reaches the temperature limit (typical value: 150 °C). The SPS is repeatedly short circuited until malfunction occurs. Parameter and lifetime data is recorded during the whole test procedure.



(a) Power MOSFET switch with separate free-wheeling path.

(b) Power MOSFET switch with integrated clamped gate circuit.

Figure 2.4: Different solutions for the switching of inductive loads. The components within the red dashed rectangles are outside the power IC.

Inductive Load Clamping

Integrated power switches for automotive applications must be capable of switching inductive loads, while employing a minimum of additional components. The common approach would be to use a freewheeling path, as shown in Figure 2.4a, to demagnetize the inductance after transistor turn off. The cost efficient solution used in automotive applications comprises an integrated gate clamp, as shown in Figure 2.4b, which limits the drain-source voltage of the power MOSFET during turn off. In fact, the Zener diode prevents the MOSFET from fully turning off until the inductive load current decreases to zero. The main drawback of this approach is that the inductive energy which dissipates in the MOSFET during turn off causes a significant rise in junction temperature, exposing severe stress on the DUT [58]–[60].

To investigate a certain device's ability to withstand such stress, repetitive inductive clamping stress tests are of interest. In [61], [62], a test system designed for such a purpose is introduced which also has a centralized architecture. Further details on the latter are given in Section 3.1.1. To properly define the stress conditions, the passive inductive loads are replaced by active driving circuits which submit the DUTs to current pulses of arbitrary shape. These driving circuits emulate the triangular switch-off current ramp an integrated power switch has to handle when connected to

a real inductive load. Also here, the DUTs are placed in an environmental chamber to accelerate the aging process by submitting them to the highest specified junction temperature.

2.2.4 Application-Specific Tests

An *application-specific* test provides a solution in between a *device-specific* and a *field application* test. In contrast to *device-specific* tests, a complete *application-specific* test circuit is built up around the DUT to collect detailed information about the life duration of the DUT. Hence, in addition to the *application circuit*, monitoring connections are routed to the DUT which allow vital parameters to be sensed continuously and during a running test. In literature, this type of life test is commonly referred to as *power cycling* [63]. To illustrate, an example of such a *destructive application-specific* life test on DC-DC converters is described below.

Power Cycling

This type of test can, e.g., apply to discrete power transistors used in various DC-DC topologies (such as a buck, boost or Čuk converter) or to integrated power transistors in a half bridge stage, including their drivers.

The duration of the stress test should reflect the time span of the corresponding application. Hence, the aging and thus the test time are accelerated by submitting the device to higher stresses than during nominal operation. The ambient temperature and self-heating of the power device are taken into account and the resulting junction temperature T_j is kept below or equal to the maximum specified operating temperature (typical values: 85 °C to 125 °C for consumer devices, 150 °C for automotive devices). The bias input supply voltage is set to the maximum level specified for the DUT to still comply with the datasheet specification. The DUTs are connected to adjustable electronic loads. The load is set to stress the DUTs at, or near, the maximum rated current [16]. The DUTs are submitted to intermittent load values which toggle between a high load of nearly 100 % until T_j reaches the maximum operating temperature and a low load of 10 %. In practical reliability tests, the timing is chosen to reach the appropriate T_j temperature. This thermal cycling increases the stress on the DUT and accelerates its aging. More details on the test system which is able to execute both *device-* and *application-specific* tests, are presented in Chapter 3.

2.3 Review of Realized Life Test Systems

Several examples of implemented test systems have been reported. Many works cited in this subsection focus on the device to be tested and the described test system is designed to fit for this *one* purpose. Some works which are cited here, only concentrate on the life test results of the investigated DUTs. The following cited literature does not report on any attempt to use the available test hardware in a systematic way for different DUTs or types of tests, or both, as it is in the focus of the MTS proposed and discussed in this work.

De Vega et al. in *"Test Setup for Accelerated Test of High Power IGBT Modules with Online Monitoring of V_{CE} and V_F Voltage During Converter Operation"* [39], introduce a test setup dedicated to conducting accelerated tests for high power Insulated Gate Bipolar Transistor (IGBT) modules. Offline and online collector-emitter voltage V_{CE} and forward voltage V_{F} measurements at high power IGBT modules are presented. Further details on the V_{CE} measurement circuit are then given by Beczkowski et al. in *"Online V_{CE} Measurement Method for Wear-Out Monitoring of High Power IGBT Modules"* [40].

Forest et al. in *"Fast Power Cycling Protocols Implemented in an Automated Test Bench Dedicated to IGBT Module Ageing"* [51], introduce a test bench for IGBT modules similar to that proposed by de Vega et al. [39]. In addition to V_{CE}, the junction temperature T_{j} is also monitored on-line. Again, this system has a centralized architecture which will make adaptations to future requirements quite difficult.

A test system for stress testing automotive smart power switches is proposed by Glavanovics et al. in *"Cycle Stress Test Equipment for Automated Short Circuit Testing of Smart Power Switches According to the AEC Q100-012 Standard"* [36]. It provides a high level of automation and a large number of devices can be submitted to stress in parallel. Three parameters (V_{DS}, I_{D}, $R_{\mathrm{DS,on}}$) are acquired in situ during a stress test run for each DUT.

A similar centralized architecture has also been used for another test system which is described by Glavanovics et al. in *"Flexible Active Cycle Stress Testing of Smart Power Switches"* [64] and also by Glavanovics et al. in *"A New Cycle Test System Emulating Inductive Switching Waveforms"* [62]. Here, the inductive clamping behavior of power Metal-Oxide Semiconductor Field Effect Transistors (MOSFETs) after turn off is analyzed.

Pedersen et al. in *"Degradation Assessment in IGBT Modules Using Four-Point Probing Approach"* [48], present another investigation in which IGBT modules are in

focus. By means of a four-point probing approach, the voltage drop within IGBT modules at the bonding wires is measured. The outcome of this work is that aged IGBT modules show a higher voltage drop due to degradation of bonding wires and solder joints.

Letor et al. in *"Life Time Prediction and Design for Reliability of Smart Power Devices for Automotive Exterior Lighting"* [65] and Russo et al. in *"Fast Thermal Fatigue on Top Metal Layer of Power Devices"* [66], present investigations on automotive smart power switches. Both papers focus on the findings from repetitive short circuit stress tests. Defects and failures that occurred on the DUTs are illustrated, but only minimal information on the used test system is provided.

Dusmez et al. in *"An Accelerated Thermal Aging Platform to Monitor Fault Precursor On-State Resistance"* [67], present an aging platform for discrete MOSFET transistors. Several transistors are stressed simultaneously and their junction temperature is controlled independently. The on-state resistance is identified as the main failure precursor. No modularization of the test setup is proposed in this work.

A similar work of Dusmez et al. in *"Comprehensive Parametric Analyses of Thermally Aged Power MOSFETs for Failure Precursor Identification and Lifetime Estimation Based on Gate Threshold Voltage"* [68], focuses on the investigation of additional parameters (namely $R_{\mathrm{DS,on}}$, V_{GS}) which can be failure precursors. These parameters are acquired outside the test setup by a curve tracer. Thus, this interesting work targets to the investigation of the failure precursors and not on the test setup design.

Bahl et al. in *"Product-level Reliability of GaN Devices"* [69] and also Bahl et al. in *"Application reliability validation of GaN power devices"* [70], address application-specific reliability testing of the emerging GaN power transistors. First, an overview which standards apply to reliability stress testing is given and it is stated that no standards explicitly exist for new GaN power transistors. Hence it may happen, that GaN transistors pass the "traditional qualification," but act poorly in the target application. As a counteract, the *double-pulse test* circuit is proposed which was published by Kaneko et al. in *"Current-collapse-free Operations up to* 850 V *by GaN-GIT utilizing Hole Injection from Drain"* [71]. By this test, two GaN failure modes are identified: Hard switching robustness and dynamic $R_{\mathrm{DS,on}}$ degradation.

Seidel et al. in *"Power Cycling Test with Power Generated by an Adjustable Part of Switching Losses"* [72], present a test bench which optionally enables the test of IGBTs, Silicon (Si) or SiC MOSFETs. The test bench provides slots to test up to six DUTs in parallel. The authors introduce a new concept to generate and inject switching losses in

addition to conduction losses into the DUTs. This test bench has a couple of features similar to those of the MTS presented in this work. However, it lacks properties such as modularity and scalability of the test system architecture.

Chapter 3

Architecture of the Modular Test System

This chapter comprehensively explains the novel architecture of the proposed Modular Test System. It reviews the traditional *centralized* test system architecture and compares it to the proposed *modular* and *distributed* architecture approach. Moreover, the control and the application modules, which are the essential building blocks of the MTS, are described in detail.[1]

3.1 Centralized versus Modular Architecture

3.1.1 Centralized Test System Architecture

Figure 3.1 shows the block diagram of a test system for repetitive short circuit testing, such as the one proposed in [36], which is designed in a *centralized* test architecture. One central host entity controls the full test sequence. It consists of a central computer which is linked to a National Instruments PCI eXtensions for Instrumentation (PXI) bus system holding four FPGA-based digital I/O control units, as shown at left in Figure 3.1. Next to the central host entity, control and measurement interfaces are implemented which distribute the control signals from the host to all test circuits via several multiplexers. The acquired measurement data is read back over these interfaces in the same way. The next part consists of power and protection drivers which monitor the input current to the DUTs and may shut down the main power line in case a defined current level is exceeded. The test circuits and actual tested devices are the only parts which are placed within the environmental chamber.

[1] Parts of the content of this chapter have also been presented in [18].

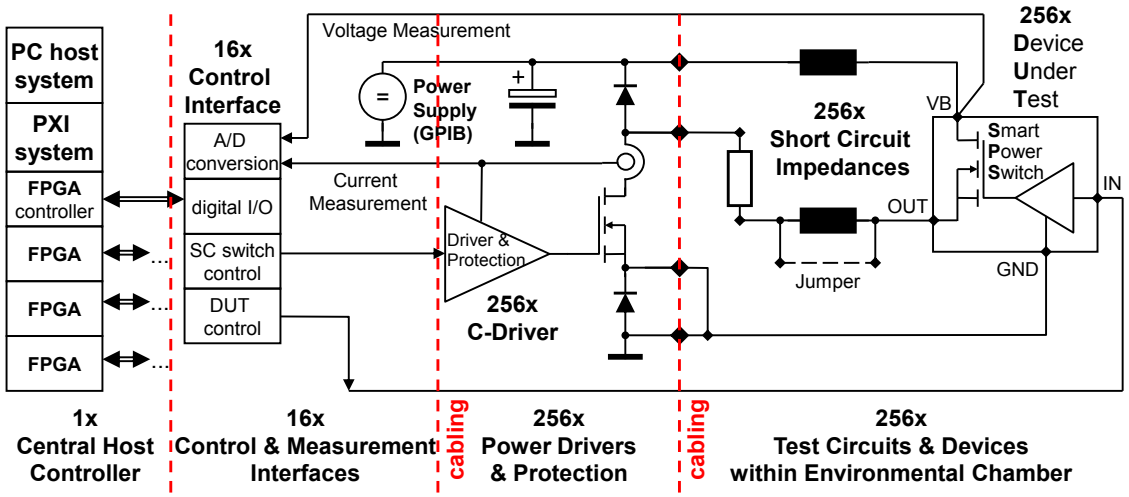


Figure 3.1: Block diagram of the centralized architecture used for the test system presented in [36]. One central host must control and measure all 256 connected DUTs within the test setup.

In Figure 3.1, the massive cabling effort needed for interfacing between control, measurement, and power drivers, as well as between power drivers and test circuits, is depicted. This massive cabling is required because all control and measurement sensing functions can only be performed by the central host. At the proposed MTS, this issue is overcome by placing the control module into the environmental chamber next to the application module. The control and measurement functions are performed by the control module autonomously and the communication to the central host computer is conducted via Ethernet only. Hence, the massive cabling in the *centralized* architecture is replaced by the slim Ethernet cabling in the MTS architecture. Furthermore, a change in the test circuit configuration will not change the Ethernet cabling from control module to the host computer. As the control and application modules are placed close to each other, sensing lines can be kept very short. As a consequence, the analog signal quality is improved in comparison to the centralized approach.

Furthermore, the *centralized* system cannot be easily adapted to new requirements. For example, if one further analog or digital signal is desired to be monitored, the central host must be adapted to acquire the new signal from all 256 DUTs and also the cabling and the interface units must be extended. With the MTS, the change for further acquired signals is less complicated. In the worst case, only the application module needs to be redesigned. In many cases, optional measurement functions are

implemented in the application module at the time of design and only need to be activated by software. The control module hardware as well as the central host function remain unchanged, as several sense channels are optionally available on the control module.

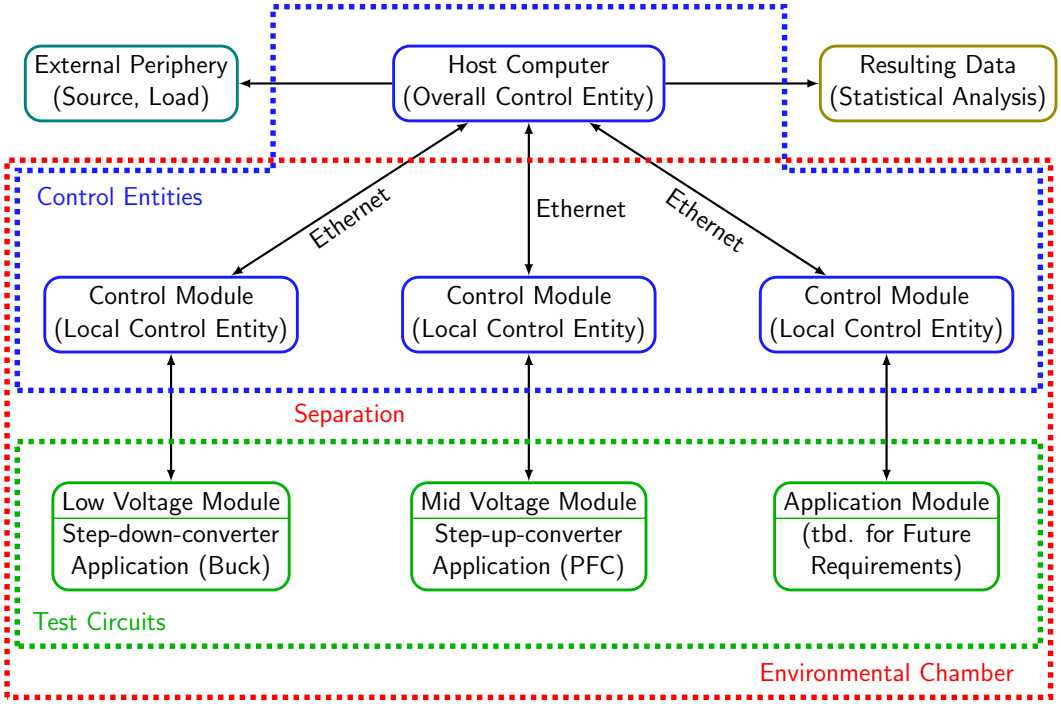


Figure 3.2: The key novelty of the MTS architecture depicted here, is the clear *separation* of the control and measurement part of the test system from the actual test circuits. Furthermore, the control is divided into *one* overall control entity (host computer) and *multiple* local control modules (details in Section 3.2) which are directly connected to the test circuit within an environmental chamber. The local control modules execute the set test pattern on the application modules (details in Section 3.3) and acquire vital parameters from the DUTs which are transferred via Ethernet to the central host computer.

3.1.2 Modular Test System Architecture

The proposed Modular Test System architecture is shown in Figure 3.2. The test control is split into two instances (hence, it is *distributed)*, namely the host computer and the control module. The host computer is *one* unit which controls the overall test flow and

communicates with the control modules. It also controls the external periphery, such as power supplies and electronic loads, as well as stores the measured data to the file system. The control modules may be *many* units (typically 8 to 24 for one test system) and are connected to the host computer via Ethernet. The host computer forwards the stress pattern to the control modules and receives preprocessed (digitized and filtered) measurement data and status information. Each application module is connected to one control module which controls the application test, performs measurement data acquisition and logs device status information. This information is sent back to the host computer which stores the data. The application modules are tailored to individual types of tests. Both the control and the application modules are placed within an environmental chamber. Only the host and the external periphery are placed outside.

The essential advantage of this test system architecture is the *separation* of the control and data acquisition parts from the actual test circuit. With this architecture, the same control and data acquisition parts can be used for different types of tests. Only the test circuits (depicted in Figure 3.2) need to be redesigned. This saves development effort, design time and provides a unified data acquisition and control methodology. In the following, the test circuit will be referred to as "application module." More comprehensive details concerning the MTS architecture are given in the subsequent sections.

3.2 Control Module of the MTS

The control module (Figure 3.3) is the core control element for the test. It consists of the following circuit blocks:

- Infineon XMC4500 microcontroller [73], [74].
- 8 MB SDRAM memory.
- 10 digital input / output channels.
- 2 Serial Peripheral Interface (SPI) interfaces, 6 Pulse Width Modulation (PWM) output channels.
- 1 Universal Asynchronous Receiver Transmitter (UART) interface.
- 1 Inter-Integrated Circuit (I^2C) interface.
- 4 Digital-to-Analog (D/A) converter channels.

- 8 differential and 12 single-ended Analog-to-Digital (A/D) converter channels.
- Overvoltage protection on all signals on the module connector.
- Available interfaces: 100 Mbit Ethernet, Universal Serial Bus (USB), programming.

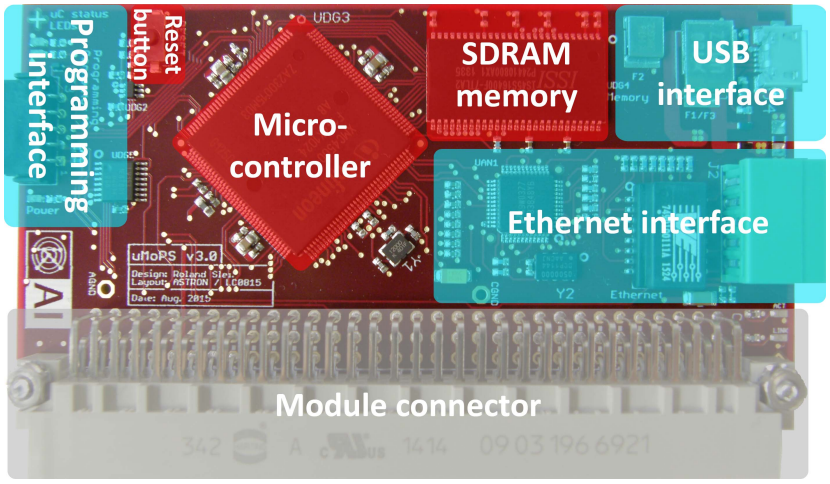


Figure 3.3: The finally manufactured PCB of the control module. The different circuit blocks are highlighted and described. The Infineon XMC4500 [73] micro-controller is located in the center left area. On the bottom, the module connector is depicted which is the interface to an application module.

This module is plugged onto an application module and controls the running test sequence; on a synchronous boost converter application, it provides the PWM-signal via a driver circuit to the half-bridge switching transistors. It senses the output voltage and closes the control loop by a digitally implemented Proportional-Integral (PI)-controller. The control module automatically monitors vital status signals (both digital and analog) from the DUT throughout the entire test time. These signals are, e.g., V_{in}, V_{out}, I_{in}, I_{out}, T_{c}.

All data are digitized on the module and sent to the host computer via the Ethernet network. The major advantage of this concept is that the measurements are directly performed on the application module. No long and complicated sense wiring to a data logger outside of the environmental chamber is required. Altogether, 20 analog measurement channels are available on the control module. This ensures expandability for future applications or extensions to existing ones.

On the control module, the implemented differential Operational Amplifiers (Op-Amps) are provided with different input voltage dividers to offer several voltage ranges.

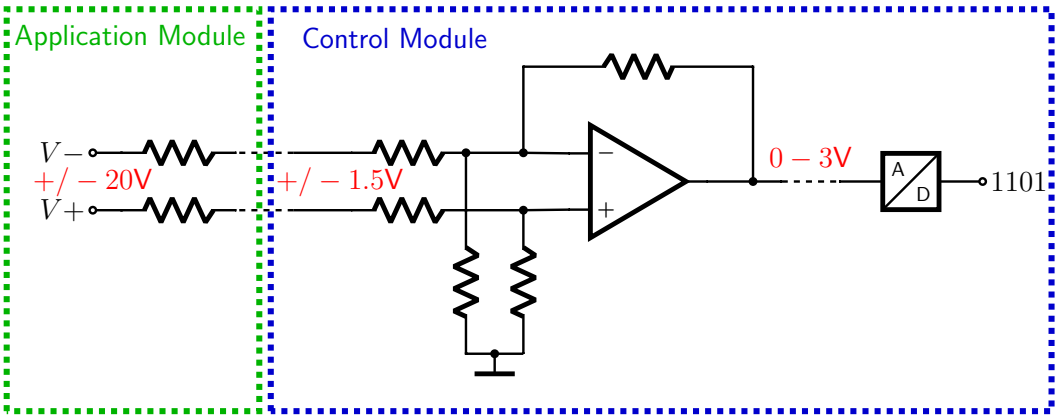


Figure 3.4: The stacked concept of the analog measurements performed by the MTS is depicted. On the control module, the input voltage range of the measurement channels is set to ±1.5 V and by choosing an appropriate series resistor down on the application board, the voltage range can be extended.

For the whole system, the voltage attenuation of analog measurements is implemented as a stacked concept. Thus, the input ranges provided on the control module can be used directly. Another possibility is (referring to Figure 3.4) to change the series resistor values on the application board in order to adapt the input voltage range. This stacked topology provides, where needed, flexibility in adapting the input voltage range to an appropriate value for the target application.

3.2.1 Software Architecture

The firmware implemented on the control module, together with a dedicated software environment on the host computer, allows an arbitrary stress pattern description. The test can be entered in the high level script language Lua [75], [76]. No low-level microcontroller-specific code is needed for programming (new) test scenarios.

The software architecture, depicted in Figure 3.5, follows a top-down approach. The test procedure on the host computer and the control modules is described by using multiple FSMs, in which each depicted circle represents a single FSM. The test procedure is described by the FSM-structure in which each single state can hold a block of Lua code. A state transition can be triggered by internal or external events as well as by a special command invoked from the upper FSM.

The uppermost circular node, named test-FSM, controls the execution of multiple node-FSMs where each node subsequently controls a single control module FSM.

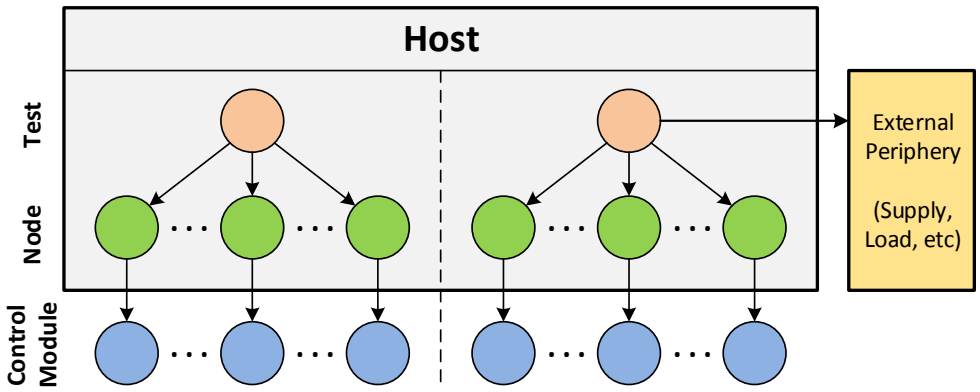


Figure 3.5: Block diagram of the software architecture: Each depicted circle represents a single FSM which holds a block of the high level script language Lua.

Additionally, the test-FSM is capable of controlling the external periphery, e.g., power supplies or electronic loads, to set voltage levels, current limits and cover automated power-up and shut down procedures. Based on this system approach, various test scenarios can be driven at the same time by simply modifying the Lua-script or FSM-structure, or both. A detailed description of the software architecture used with the proposed test system can be found in [24]–[26].

3.3 Application Modules of the MTS

An application module (green boxes in Figure 3.2) implements the main test circuit and is designed for one specific type of test. (For example, for "power cycling," the main test circuit may be a step-down or step-up converter.) Although they have different functions, some circuit blocks are common for all application modules. The most relevant ones are:

3.3.1 Guard Block

An essential function for a stress test system is to ensure that the test setup is protected from catastrophic failure. When performing long-term tests on power semiconductors, the DUT may fail in short circuit. Under any circumstances, the test system must be preserved in case of DUT damage. Preserving the DUT from further destruction

immediately after failure also supports later physical analysis of the failure's root cause. The input current to the power circuit is monitored and an overcurrent limit is defined for each DUT. In case of a short circuit, this limit is exceeded and the application module shuts down the power input immediately. This feature is implemented in hardware with a current sensor and an analog comparator to guarantee a fast response time (typical value: less than 2 µs). The failure event is then stored in an error latch and can only be reset by a test engineer intervention. Depending on the test circuit, it may be necessary to monitor additional parameters. If that is the case, a second parameter, such as the input voltage, is monitored which can trigger a power shut down as well.

3.3.2 Device Monitoring and Control

All application modules incorporate voltage and current measurements (V_{in}, V_{out}, I_{in}, I_{out}) for input and output of the power circuit. Further voltage measurements can be analog status signals from the DUT and temperature signals (e.g., DUT case temperature T_{c}). Moreover, the control module provides several digital I/O channels to log digital status signals from the DUT or send digital stimuli to the DUT.

3.3.3 DUT Board

In the MTS, the DUT is separated from the application module. This simplifies the task of replacing a failed DUT, while the application module can be reused. The DUT board is connected to the application module by a special connector, which may differ on various application boards. The connector's type depends on the voltage and current ratings and the number of needed sense signals.

On the DUT board, typically passive components are located, as well. For example, in a step-down converter application the passive components, like the input/output capacitors and the filter inductor, need to be placed as near as possible to the switching transistors to keep the stray inductances low. Thus, these components are soldered onto the DUT board. Another device which is typically placed onto the DUT board is a Unique Identification (UID) IC (see Section 3.3.5 for further explanation).

3.3.4 Module Connector

As the control module is used on several application modules, all the application modules share the same type of connector [77].

3.3.5 Board Identification

All application modules and DUT boards are equipped with a UID IC. This enables auto-detection of the connected boards by the host computer. The host can then decide which test procedures are eligible for each connected board. Furthermore, it can store the UID number of each DUT board to make it traceable after the test has been finished. To read the UID number, the I^2C interface which is available on the control module Section 3.2, is used.

3.3.6 Analog Signal Conditioning

As stated in Section 3.2, Op-Amps are provided on the control module to attenuate analog differential voltage signals to the single-ended voltage range of the microcontroller's A/D converters. Additionally, all application modules have an analog signal conditioning block for performing further signal translations. For example, a precision current source is implemented on an application module supporting high accuracy measurements of resistive temperature sensors. The voltage signal is amplified on the application module and then fed to the control module.

Chapter 4

Implementation of Test Systems Based on the MTS Architecture

To illustrate the capability of the Modular Test System architecture, this chapter discusses the realization of test systems in an exemplary approach, most notably by the comprehensive explanation of the Low Voltage (Section 4.1) test system. This work focuses on the system architecture as such. The analysis and discussion of measurement results are not within the scope of this work. However, for the sake of comprehensiveness, selected results are shown. In Section 4.2.1, another realized test system, namely the Mid Voltage test system which is based on the MTS architecture, is presented.[1]

4.1 Low Voltage Test System

4.1.1 Target Device Under Test

The target device is a DC-DC power stage which integrates two power MOSFET transistors in synchronous buck converter configuration, shown as the blue dashed box "DUT board" in Figure 4.2. It has built in gate drivers and sensing circuitry for current and temperature monitoring and implements a temperature protection feature to shut down itself in improper operating conditions. It requires merely one PWM-signal input for operation. Interlocking and generation of correct turn on signals for the high- and low-side transistor are generated internally.

[1] Parts of the content of this chapter have also been presented in [18].

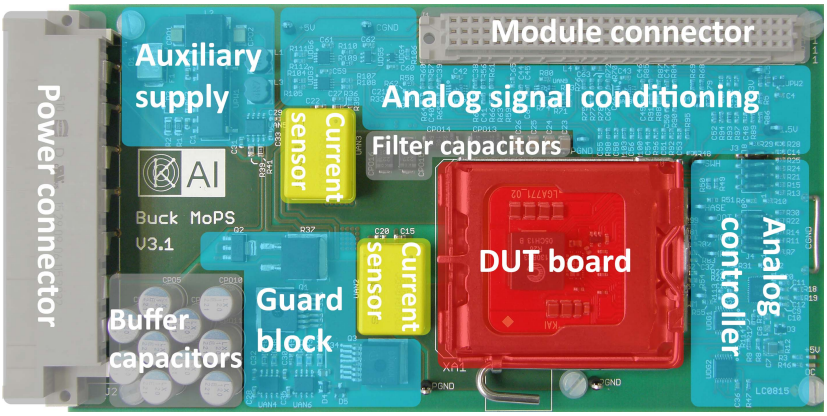


Figure 4.1: The finally manufactured PCB of the LV application module. The different circuit blocks are highlighted and described. The separate DUT board (red) is plugged onto the LV application board approximately in the center. On the top right, the module connector is shown onto which the control module needs to be plugged. The main power connector to the supplies and the electronic load is situated to the left. (In this picture, the DUT was removed from the DUT board for failure analysis.)

4.1.2 Low Voltage Application Module

The Low Voltage application module (Figure 4.1) submits the DUT to power cycling. It comprises a step-down converter circuit designed for integrated power devices. The control loop of the DUT is closed by a dedicated analog controller from Linear Technologies [78]. This analog controller senses the output voltage and provides an appropriate PWM-signal to the DUT. In the case of the LV application module, the connected control module executes only the test sequence and recording of measurement data. The control loop of the step-down converter is closed by the aforementioned analog controller, because the converter runs at high switching frequencies (250 kHz to 2 MHz). Moreover, the microcontroller on the control module is not powerful enough to handle both the control loop and test sequence control, plus measurement data acquisition at this speed.

The DUT is available on a DUT board, shown in red in Figure 4.1. To achieve an application-equivalent circuit behavior, the passive components (such as input and output capacitors and the filter inductor) must also be placed on the DUT board. This especially holds true for the input capacitance, as it influences the commutation loop inductance.

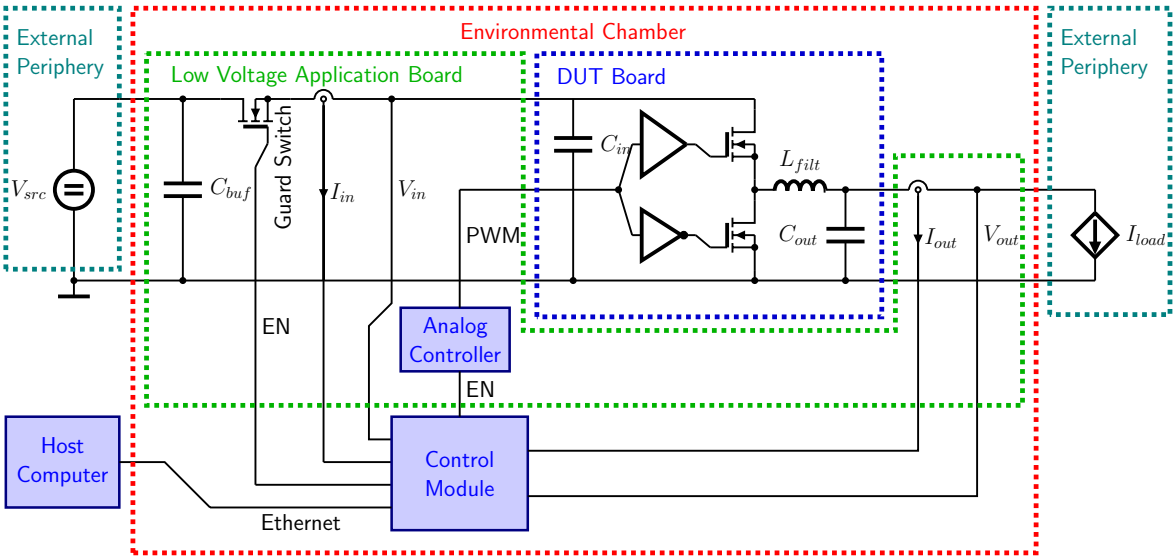


Figure 4.2: In this picture, a simplified circuit of the step-down converter including other essential parts of the LV MTS is depicted. In the center blue dashed rectangle, the switching transistors, their drivers, input and output buffers, and filter is shown which are all placed on a separate DUT board. Within the green dashed area, the measurement paths, the guard protection and control elements are shown which are all placed on the LV application module. Within the environmental chamber, also the control module is located and outside of it, there are the external periphery devices and the host computer.

The LV application module holds the DUT board in a specialized socket with a high current carrying capability and low insertion impedances. It provides additional input and output capacitors (referred to as buffer and filter capacitors in Figure 4.1) to support the power supply.

It is equipped with two current transducers (yellow boxes in Figure 4.1) for input and output current measurement. Conditioning for the logged current signals is achieved by Op-Amps placed on the application module (block “analog signal conditioning” in Figure 4.1) and fed directly to Analog-to-Digital Converters (ADCs) of the control module.

The Op-Amps for the input and output voltage measurement are placed on the control module; by choosing a suitable series resistor, as shown in Figure 3.4, the input

voltage range is set. Signal conditioning for analog monitoring signals (such as T_{mon}, I_{mon}) is implemented in a similar manner.

For the case temperature measurement T_{c}, the resistive temperature sensor is supplied from a constant current source and a voltage signal amplification is provided. The control module and the DUT board are plugged onto the application module and then placed in an environmental chamber. Figure A.1 (provided in the appendix) shows all three boards plugged together. Table 4.1 lists all measurement signals acquired by the low voltage MTS.

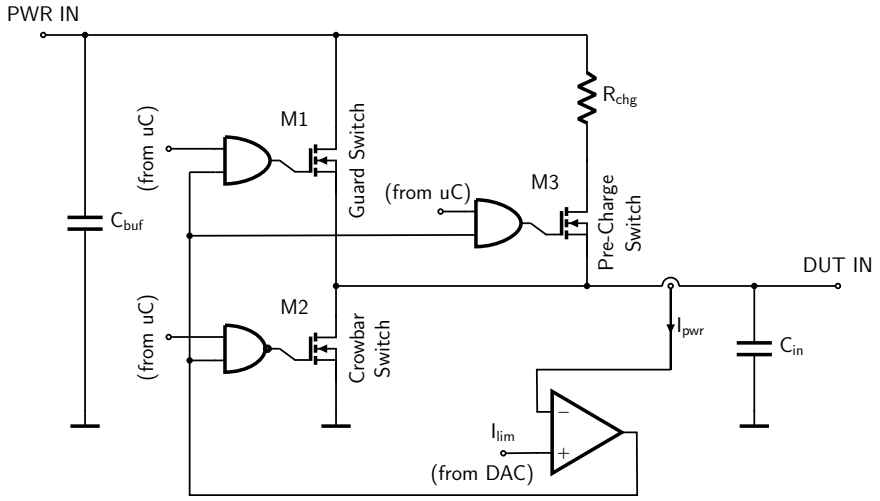


Figure 4.3: Detailed schematic of the three-transistor-solution for the guard block at the LV application module. The two transistors M1, M2 shut down and discharge C_{buf} in case of failure. M3 is used for start-up to avoid inrush current peaks which may accidentally trigger the overcurrent shut down.

4.1.3 Guard Block Realization

A guard block is likewise implemented on the low voltage application module (Figure 4.1) and is described in detail here. To implement the guard function, a solution with three protection transistors is chosen.

In Figure 4.3, the main power input line, beginning at the top left, is supplied with a high power supply. To support this power supply in high transient events, a large bank of buffer capacitors (C_{buf}) is implemented. These capacitors are placed before the protection switches and the current sensor, because the charging current of this buffer bank (C_{buf}) shall not be seen in the current measurement.

However, the input structure at the DUT also needs input capacitors in close proximity to the switching half bridge to have a short path in the commutation loop. Thus, the input capacitors (C_{in}) after the current sensor cannot be avoided.

The guard function continuously measures the power input current at the current sensor. This measurement is compared with an overcurrent limit value which is set by the control module and the guard switch will immediately shut down in case this limit is exceeded.

During start-up, when C_{in} is not charged and the guard switch is turned on, a high inrush current will charge C_{in}. This high inrush current may trigger the overcurrent limit and immediately shut down the guard switch again. To overcome this issue, a second pre-charge path was implemented. With the charging resistor R_{chg}, the current to C_{in} is limited.

Thus, the start-up procedure which is operated by the control module is to first turn off the crowbar switch and then turn on the pre-charge switch. After a wait cycle for the input capacitors (C_{in}) to be fully charged, the main guard switch can be turned on and the pre-charge path is disabled. Then, the power input current is continuously monitored and the guard switches will shut down in an overcurrent event.

The operation of the crowbar switch is complementary to that of the guard switch. It is intended to turn on in the shut down case and discharge the input capacitors (C_{in}) in order to not have the stored energy dissipated over the broken DUT which would further damage the latter.

4.1.4 Measurement Accuracy Investigations

Commercially available measurement devices typically exhibit a high accuracy. For example, the Hioki Power Analyzer PW3336 [79], used in the following investigation, has a specified accuracy for the DC voltage and current measurement of ±0.1 % of reading and ±0.1 % of full scale [80, p.140]. To achieve this high accuracy, the measurement device must be annually calibrated by a dedicated service provider. The strategy for the developed MTS application boards is to determine their accuracy once and to perform an automatic zero adjustment before every test start. In the following, the procedure of determining the accuracy is exemplarily explained by the measurement channels at the LV application module. The same procedure is also used to determine the accuracy of the FPGA-embedded control module which is introduced in Chapter 5.

In Figure 4.4, the available measurement paths are depicted. The *voltage measurement* is fed through a series resistor on the LV application module and an Op-Amp on the

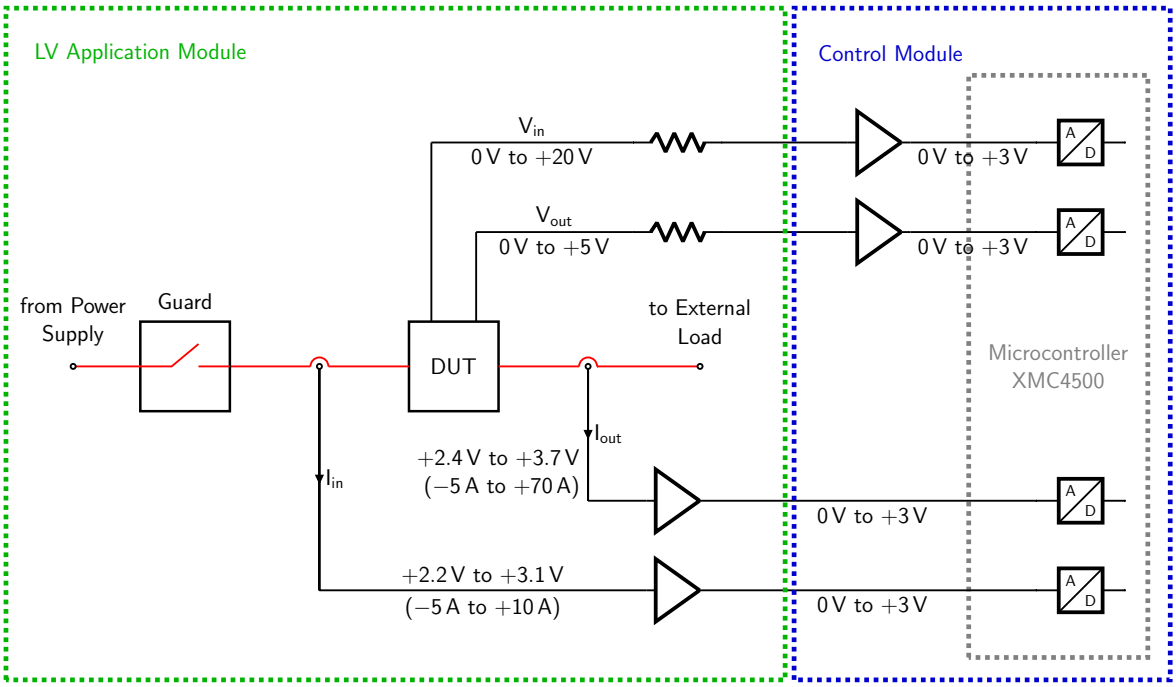


Figure 4.4: Detailed schematic of the current and voltage measurements implementation at the LV application module. All input measurement paths are attenuated to the ADC input range of 0 V to +3 V. The main power path through the LV application module is drawn in red.

control module to attenuate to the proper input voltage range of 0 V to +3 V at the ADC. Hence, the voltage is attenuated in a manner to map the interesting range of the source signal to utilize the full input voltage range of the ADC.

For the *current measurement*, current sensors from Sensitec (e.g., for output current measurement [81]) are used and their output signal is also scaled to fit to the ADC's input range. In Tables B.1 and B.2, the current sensors output voltage range and their corresponding range in ampere are listed. By considering the gain of the current sensor and the Op-Amp's attenuation, the following linear equations can be derived for calculation of the real current values from the current sensors signals.

$$V_{\mathrm{ADC,in}} = 0.21 I_{\mathrm{in}} + V_{\mathrm{ofs}} \tag{4.1}$$

$$I_{\mathrm{in}} = \frac{V_{\mathrm{ADC,in}} - 1}{0.21} \tag{4.2}$$

$$V_{\text{ADC,in}} = 0.0415 I_{\text{out}} + V_{\text{ofs}} \tag{4.3}$$

$$I_{\text{out}} = \frac{V_{\text{ADC,in}} - 0.2}{0.0415} \tag{4.4}$$

In Equations (4.1) to (4.4), I_{in} and I_{out} are the input and output current, $V_{\text{ADC,in}}$ is voltage present at the input of the ADC, and V_{ofs} is the input voltage of the ADC at zero current.

Equations (4.2) and (4.4) represent the ideal case. However, to achieve a high accuracy measurement, the errors introduced by the components in the measurement path must be considered. These components are: the current sensor, the Op-Amp, the ADC and passive components. Table B.5 lists all errors of these components which are defined in the datasheet and the total calculated (predicted) error.

Errors on the measurement signal can be of systematic or random nature (e.g., noise) [82, p.32]. Systematic errors have a deterministic cause and are reproducible by repeated measurements. Hence, these type of errors can be corrected in order to improve the measurement accuracy. This is demonstrated by the example of the output current measurement on the LV application module below.

To calibrate a measurement system, a comparison device is necessary (in literature denoted as *the normal* [82]) with a significantly higher accuracy specification. For the comparison described here, the Hioki Power Analyzer PW3336 [79] is used. The procedure is executed as follows.

The LV application module must be operated in order to stimulate voltage and current values over the entire available measurement range. Table B.3 lists the respective measurement range of each parameter in column two. In columns three and four, two possibilities to stimulate the parameter values are given. In column three, the LV module operates in power conversion, whereas in column four, the LV module power conversion is turned off and the parameters are injected from external laboratory devices. The variant in column four was neglected for current measurements, because the achievable output current would be too low and thus, outside the range of the targeted life test (as in the latter, currents of up to 50 A occur). Hence, the calibration measurement was executed with the LV application module in normal power conversion operation. Possible noise from the power conversion may be seen in this variant which is of interest in the case described here.

The calibration procedure is conducted in the way that each measurement parameter is stepwise set and increased for the whole possible range (as in column three of Table B.3) and measured at each step by both, the LV application module and the reference device (i.e., the Hioki Power Analyzer). The Hioki power analyzer conducts the measurements with a sampling frequency of 700 kHz and the detailed settings of the LV application module and its control module during the calibration procedure are listed in Table B.4.

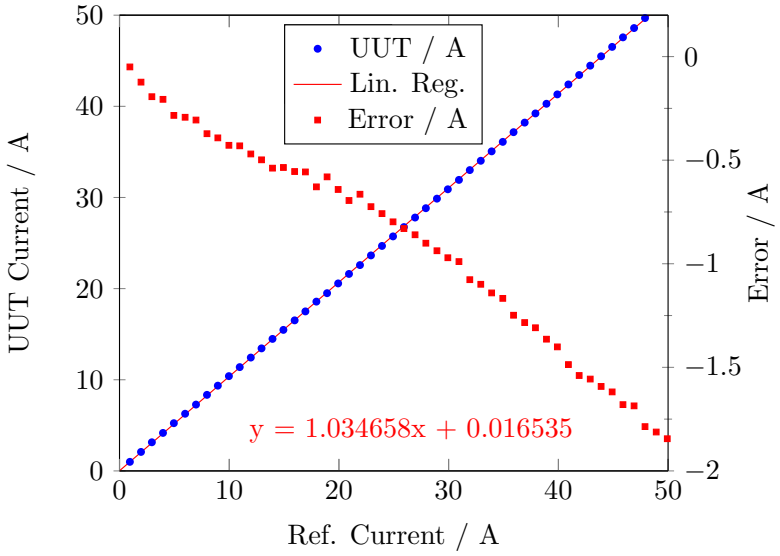
The resulting measurements are plotted in Figure 4.5a, where the current measurement of the reference device is applied on the x-axis and the measurement of the LV application module is applied on the y-axis. A linear regression is calculated onto these two data sets. The current value of the LV application module is calculated by Equation (4.4) which was derived on the assumption of ideal circuit components. For this procedure, the measurement values from the reference device are assumed to be error-free, although it specifies a small error of 0.1 %. If now the circuit components on the LV application module would have an (almost) error-free signal, the slope of the linear equation should have an exact slope of 1 and zero offset. Figure 4.5a reveals that the slope is not 1 as it rises too steeply. Here the systematic error of the not exactly calibrated gain of the slope is unveiled, as with higher current value, the error increases. This systematic error can be corrected (in metrology literature this is denoted as *adjustment* [82]) by adjusting the calculation formula with the results gained by the linear regression. E.g. the values in the formula for calculating the I_{out} change from Equation (4.4) to the following corrected values:

$$I_{\text{out}} = \frac{V_{\text{ADC,in}} - 0.167581}{0.042938} \tag{4.5}$$

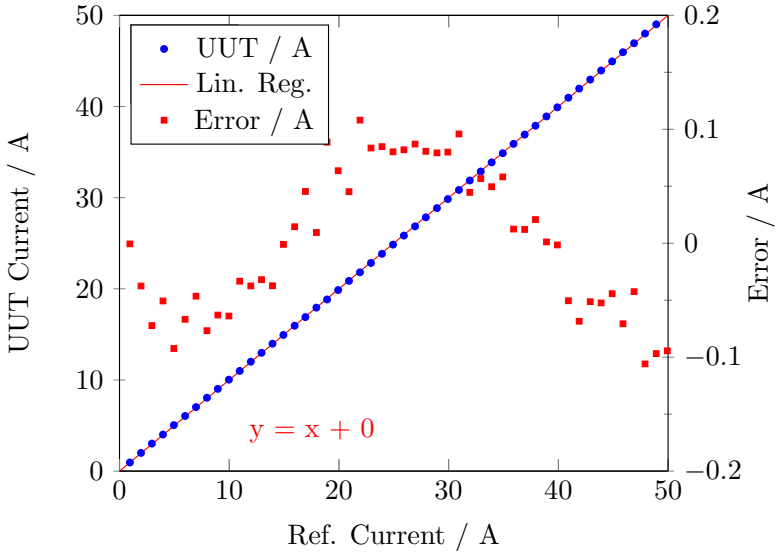
In Equation (4.5), I_{out} is the output current and $V_{\text{ADC,in}}$ is voltage present at the input of the ADC. In Figure 4.5b, the raw values from the LV application module are recalculated with the corrected values as in Equation (4.5) and thus an exact slope of 1 and zero offset are achieved.

For the life tests executed with the LV application module, the accuracy was determined once for four different boards. It was found that the slope deviation between the four boards is low. Thus, an averaged slope for all boards can be used for calculation of the real values.

However, the offset differs more significantly between the boards and may also drift over time and temperature. Hence, the offset is measured and logged automatically



(a) Linear Regression of the I_{out} measurement before adjustment.



(b) Linear Regression of the I_{out} measurement after adjustment.

Figure 4.5: The two pictures show the comparison of the I_{out} measurement between the LV application module and the reference device (Hioki Power Analyzer). In picture (b), the improvement of the measurement accuracy after adjustment of the conversion coefficients is demonstrated. In the bottom of each diagram, the slope and offset of the current measurement comparison is printed.

at every test start and later used to calculate the real values. By this method, a high accuracy is achieved for the LV MTS system which is important to validate the final life test results.

Tables B.6 and B.7 present the detailed results of the investigation of the four LV application boards and the eventually achievable current and voltage accuracy is listed. These achieved accuracy values can be compared to Table B.5 which lists the calculated values taken from the datasheets of the circuit components. This comparison shows that by the here described calibration method the current measurement accuracy can be improved by a factor of 2 compared to the calculated values (e.g. $I_{\text{out,calibrated}} = \pm 0.65\,\%$ versus $I_{\text{out,calculated}} = \pm 1.325\,\%$). For the voltage accuracy the difference between calibration and calculation is small. Thus it shows that the estimation by the calculation is exact. Furthermore, it reveals that the circuit component which is inducing the largest error is the current sensor. In contrast, the components which are realizing the voltage measurement contribute a significant lower error to the final value.

4.1.5 Low Voltage MTS Setup

Table 4.1: List of all available measurement parameters on the LV MTS, stating their measurement ranges and typical values.

Symbol	Description	Measurement Range	Typical Value
I_{in}	Converter input current	−5 A to +10 A	6 A
I_{out}	Converter output current	−5 A to +70 A	40 A
V_{in}	Converter input voltage	0 V to 20 V	12 V
V_{out}	Converter output voltage	0 V to 5 V	1.5 V
T_{c}	DUT case temperature	−50 °C to +200 °C	100 °C
T_{brd}	DUT board temperature	−40 °C to +150 °C	50 °C
I_{drv}	Driver current	0 mA to 63 mA	5 mA
V_{drv}	Driver voltage	0 V to 6 V	5 V
I_{mon}	IC current monitor	0 mV to 300 mV	200 mV
T_{mon}	IC temperature monitor	0.8 V to 1.8 V	1.4 V

An LV MTS in power cycling configuration has been completed [17], [18] and has proven a valuable tool for chip development. Figure 4.6 shows how this system is built

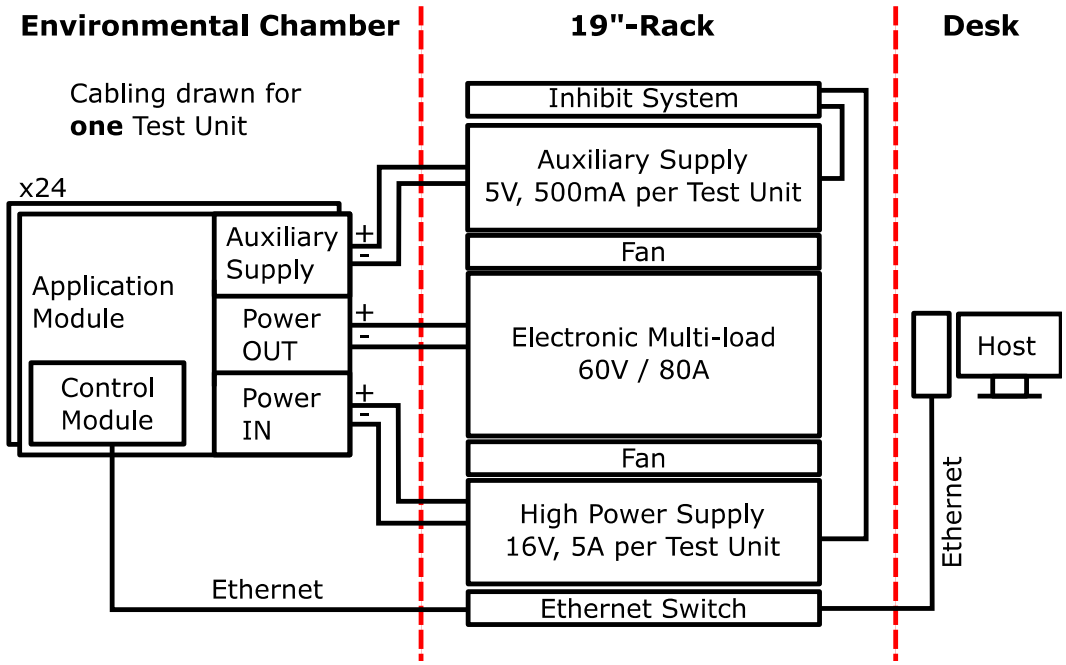


Figure 4.6: In this block diagram, all additionally necessary devices to build up an LV MTS are depicted. In the left area, the LV application modules are shown within the environmental chamber along with their connections to the outside. In the center, the peripheral devices which are the power supplies, the electronic multi-load, the inhibit system, and an Ethernet switch are mounted within a standard 19" rack. The central controlling host computer is symbolized to the right.

up. 24 test units are placed within the environmental chamber, each consisting of an application and a control module as well as a DUT board. Outside the environmental chamber, the power signals are routed to a high power supply for power input and an electronic multi-load for power output of the power converter application. For supply of the control and application module, an auxiliary supply is required. All control modules are wired with Ethernet cables which link to a common Ethernet switch. The host computer with the control software environment connects to this switch and maintains the whole stress test. The inhibit system monitors the auxiliary supply voltage and may shut down the high power supply in an undervoltage condition. Hence, it works as an independent instance and monitors the health status of the auxiliary supply as well as the temperature within the environmental chamber.

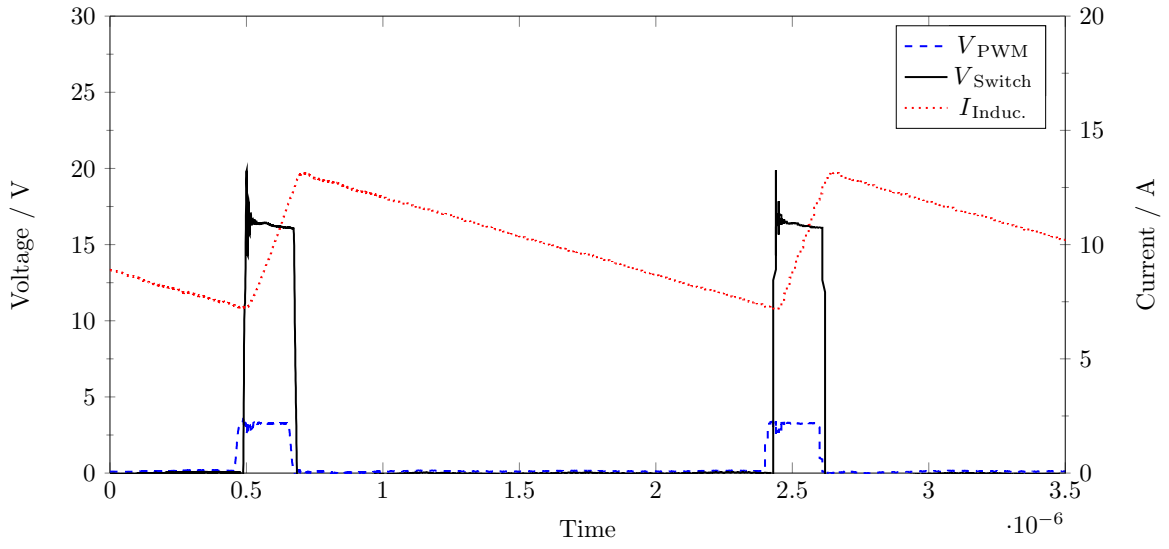


Figure 4.7: Measurement shot of important parameters of an LV application module while the converter is running. The blue dashed curve shows the PWM-signal coming from the analog controller. The red dotted and the black curve indicate the current through the inductor and the voltage at the node between the switching transistors, respectively.

4.1.6 Exemplary Test Result Data

The following results have been obtained with the aforementioned LV MTS. Figure 4.7 depicts typical waveforms of the step-down converter application. The input voltage of 16 V is converted down to 1.5 V at an average load current of 10 A. The control PWM input signal in the figure shows a duty cycle of approximately 10 %. This PWM signal is generated by a control loop which is adjusting exactly to the desired output voltage of V_{out}=1.5 V. Furthermore, the voltage at the switching node of the power transistors and the inductor current are given. Figure 4.8 presents lifetime results of two stress tests. First, "Design 1" was tested and DUT failures were monitored. Subsequently, the design of the DUT was improved and the same test was repeated. The test results of "Design 2" show that all DUTs now survive the stress test. The blue triangles of this test are all on one line because the stress test was stopped after the full test time was reached, at which time all DUTs were still operable. As with the proposed MTS, measurements are performed in situ during the running test, the exact failure times (rectangles and triangles) can be determined. Moreover, drift data of the voltages

and currents, as in Figure 4.7, are continuously recorded and possible deviations are unveiled.

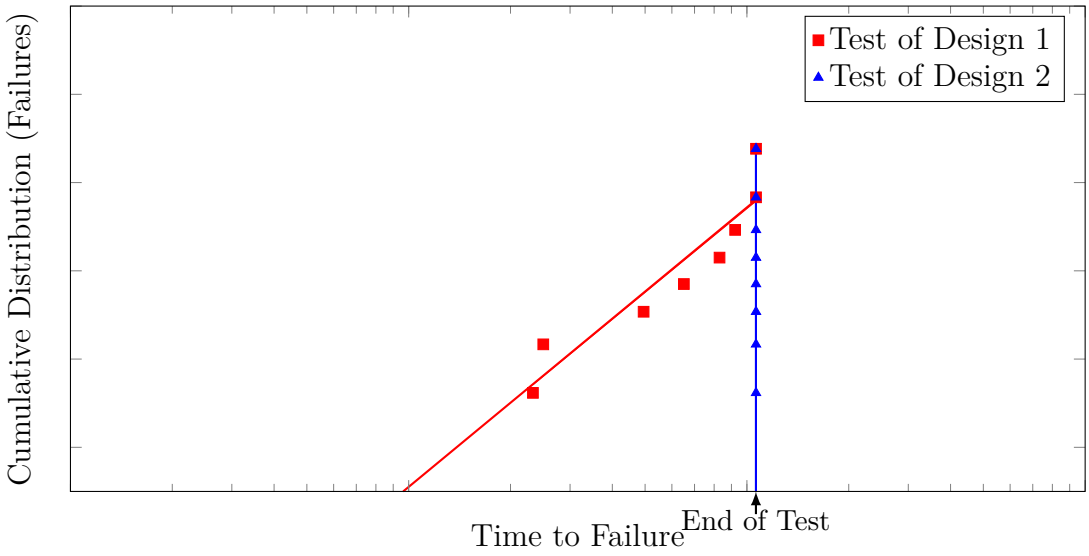


Figure 4.8: Lifetime results of two life tests conducted with the LV MTS.[2] On the x-axis, the run time of the test and on the y-axis the failure distribution are plotted. First, test 1 (red) was executed and device failures occurred. After improving the design of the DUT, the test was repeated (blue) and all DUTs survived the test until test termination.

4.1.7 Arbitrary Load Quantities for Mission Profiles

Usually life testing is performed for a specific, commonly worst case, stress condition. This implies that a fixed ambient temperature and the maximum load current are applied to the test application. However, significant lifetime discrepancies may be observed in field operations due to the varying operation and environmental conditions during the entire service time (compare "mission profiles" [43]). To overcome this challenge, the herein proposed test system provides, thanks to its modular approach with its flexible control module, the possibility to drive arbitrary load profiles. Consider the application of a Point-of-Load (PoL) converter for providing the supply to a server processor. Here, the input voltage is 12 V DC and it is converted to the core voltage of typically 1.2 V DC. However, the load to the processor is hardly constant, but changes

[2] Unfortunately, for reasons of confidentiality, the exact quantities cannot be shown in this figure.

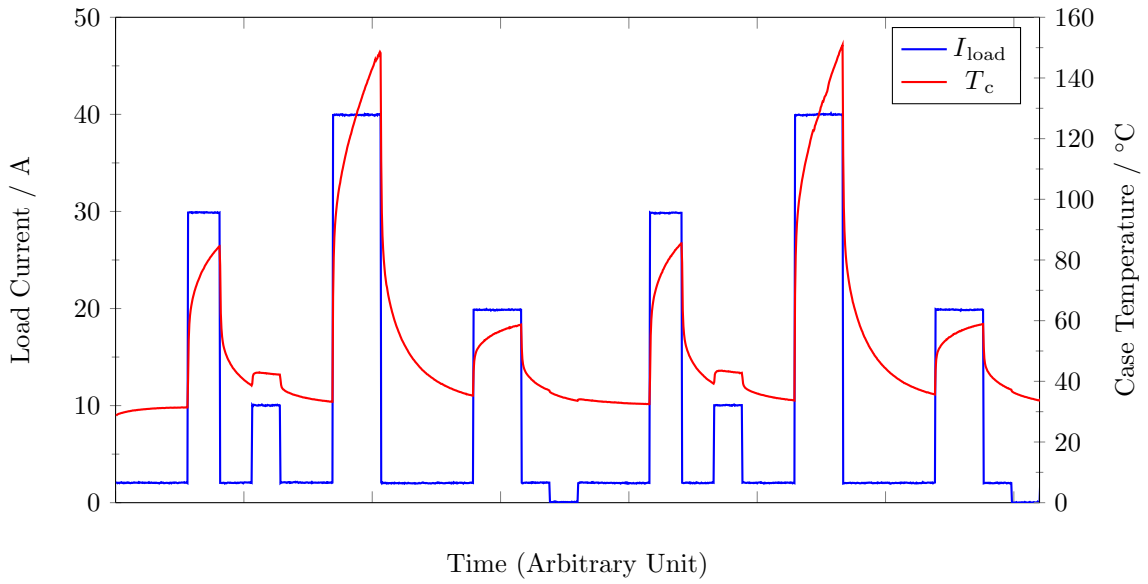


Figure 4.9: This diagram shows two load cycles applied onto an LV MTS which is configured according to Table 4.2. The load current I_{load} (blue) is set for the appropriate time span and the temperature increase of the DUT's case is measured simultaneously (red).

Table 4.2: This table lists an exemplarily configuration of an arbitrary load profile. In column one, the amount of impressed load current and in column two the time span for each load current within one load cycle is given.

Load Current	Time Duration
100 %	11 %
75 %	7 %
50 %	11 %
25 %	6 %
5 %	58 %
0 %	7 %
Total time for load cycle	1 h

rather frequently to various load levels in operation. This implies that also the supplied currents provided by the PoL converter follow these different load levels.

Figure 4.9 shows an application-equivalent arbitrary load profile for a typical server PoL converter application. The processor is at high load condition for a short time

span, e.g., when a request is received. However, it is at low (idle) level for the majority of the operation time. Table 4.2 shows these time durations in more detail.

The test system proposed in this work is designed to support tests with such arbitrary load conditions. This is easily realized by configuring the test pattern in the software environment. It is even possible to drive different load profiles on various control modules within the same test. Figure 4.9 shows real measurement data acquired by the LV MTS. In this test case, two consecutive load cycles are shown which were conducted over two hours test time. Again, the duration of this profile sequence may be set arbitrarily. The blue line indicates the load current I_{load} at the output of the PoL converter. The red solid line shows the case temperature (T_{c}) behavior of the power stage semiconductor. It is measured by a PT100 temperature sensor which is directly glued onto the package of the power stage semiconductor. This temperature measurement information is used to determine the load current (I_{load}) value and on-time to reach a temperature peak of up to 125 °C.

4.1.8 In Situ Voltage Monitoring Evolution

In Figure 4.10, the input voltage V_{in} evolution of a power cycle test performed with the LV MTS is shown. Again, the DUT in this life test was an integrated power stage which conducts a step-down conversion.

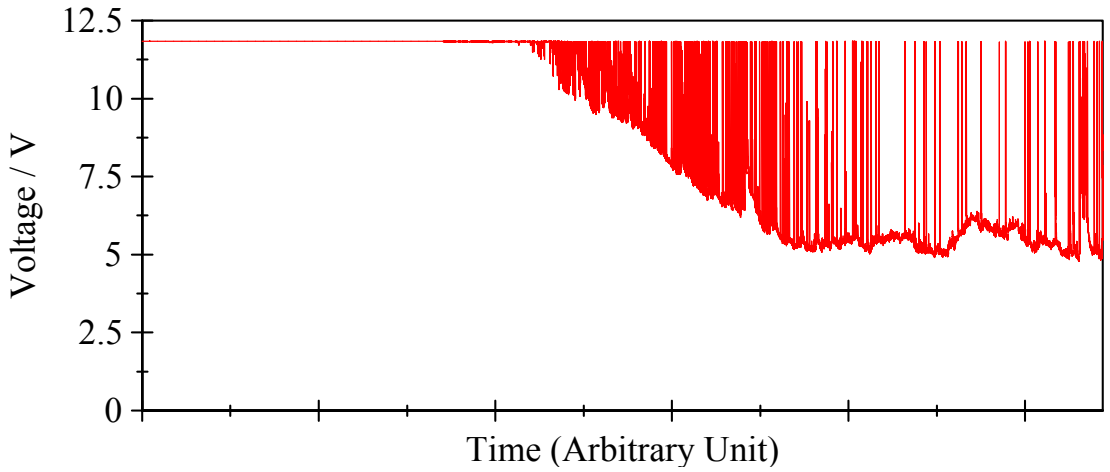


Figure 4.10: The input voltage V_{in} was continuously recorded during a power cycle test executed by the LV MTS. An interconnect problem occurred at the solder joint of the sense pin. The measurement at this defective contact had been toggling between the input voltage of 12 V and lower values.

During the life test, the input voltage was continuously recorded from one dedicated sense pin of the DUT. Figure 4.10 shows that an interconnect problem occurred at the solder joint after the first third of the test time. Through the further ongoing test, the measurement at this defective contact had been toggling between the input voltage of 12 V and lower values. Analysis showed that this was due to a second level interconnect problem as a result of a bad pad layout of the sense pin connection on the DUT board.

4.2 Further Test Systems based on the MTS architecture

Besides the LV MTS, there are further test systems which are based on the MTS architecture. Table 4.3 shows an overview of available and planned test systems at KAI. The first three listed systems are operated by the same control module (as described in Section 3.2), whereas the last test system (FPGA-based MTS) has a different test target, as a significantly higher amount of DUTs needs to be tested. Hence, a different control module was designed which is comprehensively covered in Chapter 5. However, first, the Mid Voltage MTS is presented in the following subsection (Section 4.2.1). The development of the High Voltage MTS is currently ongoing at KAI within another project. Design details will be treated in a separate thesis and an outlook on the topic is given in Chapter 7.

Table 4.3: Voltage and power rating of the different MTS test system variants.

Type	Max. Voltage	Power Rating	Status
Low Voltage MTS	16 V	300 W	in operation
Mid Voltage MTS	700 V	3 kW	in operation
High Voltage MTS	1.2 kV	40 kVA	in development phase
FPGA-based MTS	120 V	600 W	prototype available

4.2.1 Mid Voltage Test System

GaN High Electron Mobility Transistors (HEMTs) offer major advantages in half bridge applications, due to their low switching losses and missing reverse recovery effects, such as a bridgeless power factor correction stage, as presented in [83]. Consequently, an

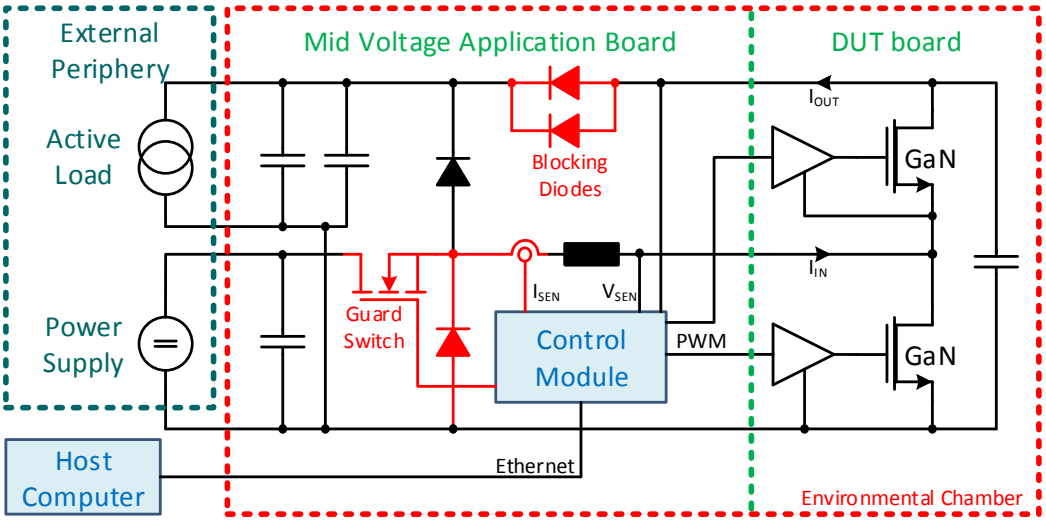


Figure 4.11: This picture shows the main circuit of the MV MTS and its essential parts. To the right, the half bridge circuit with the tested GaN transistors which are all placed on a separate DUT board are depicted. On the MV application board, the protective circuit elements (in red), the control module and buffer capacitors are placed. At the outside of the environmental chamber, the external peripheral devices and the host computer are located. The black diode in the center is used at start-up to directly charge the capacitors at the output rail next to the active load [23].

application-specific reliability test setup needs to combine two GaN devices in series with a low impedance commutation loop providing forward and reverse conduction and drive conditions, as well as dynamic start-up control and continuous load operation. The Mid Voltage MTS[3] is designed to provide all these requirements and executes life tests on multiple GaN transistors in *application-specific* configuration in parallel and under accelerated stress conditions. In particular, this system allows testing of GaN transistors which are arranged in half-bridge configuration and perform a boost-converter operation.

[3]Parts of the content of this section have also been presented in [22], [23].

Hardware Implementation

The block diagram of this system is illustrated in Figure 4.11 which shows that the system is composed of familiar elements in its architecture compared to the previously described LV system.

First of all, the external periphery devices, a high power supply and an electronic load, are depicted to the left on Figure 4.11. These are wired to supply multiple (typically 8) MV application boards in parallel.

A guard block is also realized within the MV MTS and its components are depicted in red in Figure 4.11, where they conduct the following functions:

In the input line, a fast active protection to avoid DUT destruction in case of a failure is realized by a protection switch which is operated by comparators monitoring the input current (via AMR sensor) and output voltage of the half bridge. A hardware implemented digital logic will shut down the PWM signals and the protection switch when the software programmed current and/or voltage limits are exceeded.

In the output line, blocking diodes are implemented to stop the current from flowing back from the output capacitors through the possibly damaged DUT in case of shut down. As all MV application boards within a test setup are connected in parallel at the output rail, the back-flowing current may be considerably high. By means of this protection, the remaining application boards can continue their test operation although they are connected to the same supply-load rails. Furthermore, the failed DUT's micro-structures are preserved to facilitate the physical analysis of damage mechanisms.

In Figure 4.12, a Spice simulation of an overcurrent shut down caused by a short circuit failure of the low-side GaN transistor at time = 100 µs is shown. The overcurrent is detected at 30 A after 10 µs, the input voltage is removed by the protection switch and the output voltage decays earlier due to the blocking diode. The load current I_{load} decays within 100 µs due to the losses in the freewheeling path which removes the power from the GaN transistors and preserves them with only minor local damage for physical analysis. An example of a damage picture resulting from the described protective shut down is given in Figure 4.13.

The MV application board provides a module connector to interface the previously described (in Section 3.2) control module which is connected to a host computer and executes the programmed test pattern. In contrast to the LV MTS, in this test system implementation, the control loop for the boost conversion it realized in software and fully operated by the control module. Hence, the latter is controls *and* measures the

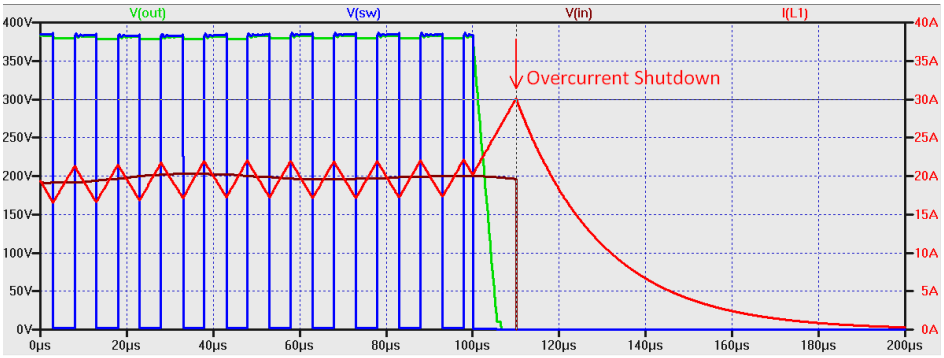


Figure 4.12: Spice simulation of protective system shut down in case of active (low-side) GaN failure by short circuit [23].

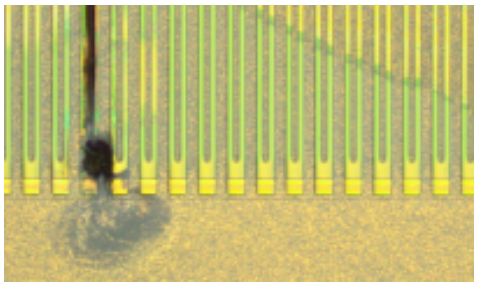


Figure 4.13: Optical micrograph of GaN device failed in short circuit, showing only local damage due to fast protective shut down [23].

application under test. The microcontroller of the control module enables a switching frequency of up to 200 kHz. This frequency range corresponds with the application under consideration which is used as a single phase grid rectifier, where 100 kHz is a typical value.

On the right side in Figure 4.11, the DUT board is depicted which is separated from the MV application board as indicated by the green dotted line. As the power rating of the MV MTS is higher by a factor of 10 (compared to the LV MTS), the inductor and main input and output capacitors of the boost circuit cannot be placed onto the DUT board, because of their dimensions (i.e., the inductor has a diameter of 72.4 mm and a height of 38.5 mm).

The two GaN transistors and their drivers, which are powered by isolated supplies, are implemented in close proximity to each other on the DUT board. Temperature sensors mounted on the transistors' cases and sensing of the low-side transistor's drain source voltage V_{DS} are also realized on the DUT board.

Table 4.4: Settings of the executed MV MTS life test run.

Test Type	V_{in}	V_{out}	I_{in}	f_{sw}	Max. T_c
Nominal	200 V	400 V	8 A	100 kHz	105 °C
Accelerated	300 V	700 V	10 A	200 kHz	150 °C

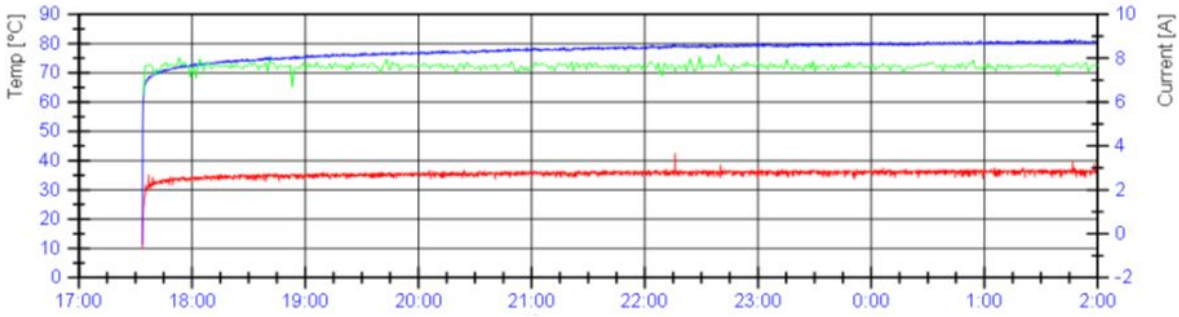


Figure 4.14: In this figure, the case temperatures of the high-side ($T_{c,hs}$=red) and low-side ($T_{c,ls}$=blue) GaN-transistor which are comprising the half-bridge circuit, are depicted. Furthermore, the input current (I_{in}=green) to the power converter is monitored during life testing [23].

Figure A.3 shows four mounted MV MTS test circuits (application and control boards) placed within an environmental chamber which were used for the life test described in the following subsection.

Exemplary Life Test Results

Life tests with the MV MTS have been executed with Infineon 600 V, 70 mΩ normally-off GaN transistors. In the first setup, four test units (comprised of altogether eight GaN DUTs) were operated in parallel at nominal and accelerated conditions.

Detailed test settings are listed in Table 4.4. Due to the developed protection circuit, device destruction in case of failure could actually be prevented. Thus, physical analysis of single failure locations and causes on the chip are possible. While in situ test system voltage and current monitoring delivers information on control quality, and thereby test stability, observation of GaN device temperatures may reveal possible drift and degradation phenomena. Measurements, recorded by the host computer, show stable values of all parameters after start-up and reaching thermal equilibrium, as illustrated in Figure 4.14.

Chapter 5

Performance Enhancement of the MTS by Use of an Embedded System

USING the proposed Modular Test System, *application-specific* life testing is realized with an Infineon XMC4500 [73], [74] microcontroller. In this case, the microcontroller module has a medium complexity level, as *one* module operates *one* DUT within an *application-specific* test circuit. For High Temperature Operating Life testing, however, a higher level of control module complexity is required.

In the following, a test system realization for HTOL testing is comprehensively illustrated. Here, *one* control module drives *several* (typically 4 to 16) individual DUTs in parallel. Furthermore, as the number of DUTs required for HTOL tests (at least 231 devices) is much higher compared to *application-specific* tests, it is reasonable to operate several DUTs with one control entity. Thus, the requirements and complexity of the control entity are higher.

In this HTOL test system concept, the control module is connected to a stress board which holds several DUTs (up to 16 [19]). In fact, the DUTs are soldered onto small PCBs and the stress board provides slots onto which these DUT boards are plugged. Here, the reusability within the MTS becomes an obvious advantage as only the control module needs to be redesigned. The modular software framework, however, can be reused. E.g., smart low- and high-side switches, multichannel switches, Light Emitting Diode (LED) driver ICs, automotive ICs and airbag ICs can be target devices for HTOL tests.[1]

[1]Parts of the content of this chapter have also been presented in [21].

5.1 Discussion of Different Core Units for the Control Entity

In Table 5.1, three different core units are compared. In column two, the XMC4500 microcontroller is listed which is used as the core unit for the *application-specific* MTS which is described in Section 3.2 and published in [18]. As stated above, the computational performance of this microcontroller is not sufficient to control *and* monitor several DUTs in parallel. In column three, the microcontroller which was used in the available *legacy test system* is listed. Here, *legacy test system* refers to previously available test hardware which was used for the execution of HTOL tests.

A comprehensive explanation of the control board used in the *legacy test system* is covered in [20]. In contrast to the systems listed in columns one and two (Table 5.1), the microcontroller within the legacy test system only *controls* multiple DUTs. However, measurements of the DUTs' states are performed either outside the test system or with a separate, and thus non-synchronized, measurement system from National Instruments (a PXI-system). Furthermore, smart protection functions, such as the aforementioned guard blocks, are not available within the *legacy test system*. Only safety fuses are used in the latter system.

Thus, the main required functions for the novel control module described herein are to fulfill the known functions of the *legacy test system* and to add the functions of online DUT status monitoring and circuit protection. Hence, the NI sbRIO-9651 [84] was chosen as the new core unit. It is an embedded system which combines a microcontroller and a reconfigurable FPGA in one module which runs a full operating system (NI Real-Time Linux). Thus, it offers more benefits than using a microcontroller alone, notably the capability to operate, protect and monitor multiple DUTs in parallel in real-time. The functionality in the embedded system needed to act as an advanced control module for the MTS is programmed by NI LabVIEW.

The comparison in Table 5.1 clearly reveals the superior performance of the FPGA-based embedded system over the microcontroller-based approaches, except for the rated ambient temperature range which is higher for the MTS system's microcontroller. This drawback is compensated for as follows: In the former MTS test system [18], the control module is mounted jointly with the application module into an environmental chamber, while in the new HTOL test system, the signals, interfacing between the two units, pass through the chamber enclosure. Thus, the control module is located outside and the stress board, which holds the DUTs, is located inside the environmental

Table 5.1: Comparison between different core units for control modules used in life test systems.

	Novel FPGA-Based Embedded System	MTS System Microcontroller	Legacy Test System Microcontroller
Manufacturer	NI	Infineon	Silicon Labs
Type	sbRIO-9651 [84]	XMC4500 [73]	C8051F120 [85]
CPU	ARM Cortex™-A9	ARM Cortex™-M4	CIP-51™
FPGA	Xilinx Zynq XC7020, Artix-7	n.a.	n.a.
Cores	2 cores	1 core	1 core
Bit width	32-bit	32-bit	8-bit
Speed	667 MHz	120 MHz	100 MHz
Temperature	−40 °C to +85 °C	−40 °C to +125 °C	−40 °C to +85 °C
ADC	n.a.	4x 12-bit, 8x multiplexed (each)	1x 12-bit & 1x 8-bit, 8x multiplexed (each)
DAC	n.a.	2x 12-bit	2x 12-bit

chamber. This configuration is depicted in Figure 5.2: The stress boards are within the environmental chamber which is illustrated by the red dotted line. All other components, namely the host computer, the FPGA-based control module and the load boards are outside. The other disadvantage of the FPGA-based embedded system is that it offers no integrated ADCs and Digital-to-Analog Converters (DACs). This is mitigated by the implementation of multiple external converter ICs, driven by SPI-interfaces, into the new FPGA-based control module.

5.2 Determination of FPGA-Based Control Module Specification

The specification of the FPGA-based control module was defined within the context of the master's thesis in [19]. This thesis performed a concept study by investigating 51 distinct HTOL tests which were previously conducted by the *legacy test system*. A different set of test hardware and software was required for each of these 51 legacy tests. The goal of this concept elaboration was to design an FPGA-based control module

which allows substituting as many of these hardware and software sets as possible with one new control module. An important finding from the concept study is that the majority of devices to be tested operate at a voltage of V_{max}=100 V and currents of I_{rms}=1 A and I_{max}=5 A. Thus, the FPGA-based control module is designed for these ratings. With the chosen concept, 44 of the 51 *legacy tests* can now be covered by one FPGA-based control module.

5.3 Realization of the FPGA-Based Control Module

In this section, the newly developed control entity of the HTOL test system is described. This entity consists of two main sub-modules: The *core sub-module* is the sbRIO-9651 [84] which is a circuit board developed and sold by NI. This board contains the FPGA and microcontroller. NI LabVIEW is used to program the firmware on this board to realize the functionality of the test system. The *peripheral sub-module* is the self-developed board, interfacing between the sbRIO-9651 board and the other components of the test system (i.e., the host computer, the DUTs, the supply line, and the Ethernet connection). This board provides a connector onto which the sbRIO-9651 board is plugged. All connections leading to the rest of the test system are routed from the sbRIO-9651 over the *peripheral sub-module*. Thus, additional circuitry is implemented protecting the FPGA or microcontroller signal I/Os. All further information below refers to both of these sub-modules plugged together when the term *FPGA-based control module* is given.

Figure 5.1 shows the block diagram of the *FPGA-based control module*. At the top left, the sbRIO-9651 is depicted. It communicates via Ethernet with the host computer, receiving the information pertaining to which test pattern is to execute and transmitting measurement data for DUT status documentation. In an HTOL test system, one host computer is used to operate multiple FPGA-based control modules.

The supply concept for the FPGA-based control module comprises five individual supply voltages referred to three different ground potentials. This was realized by dedicated isolated step-down converter and voltage regulator circuits on the *peripheral sub-module*. The FPGA-based control module supports 16 parallel digital I/O lines [namely, the General Purpose Input Output (GPIO) lines] and three communication interfaces (these are: 2 x I^2C, SPI) which are depicted at the top right in Figure 5.1. Since different DUTs will be investigated on the stress board, the system must be

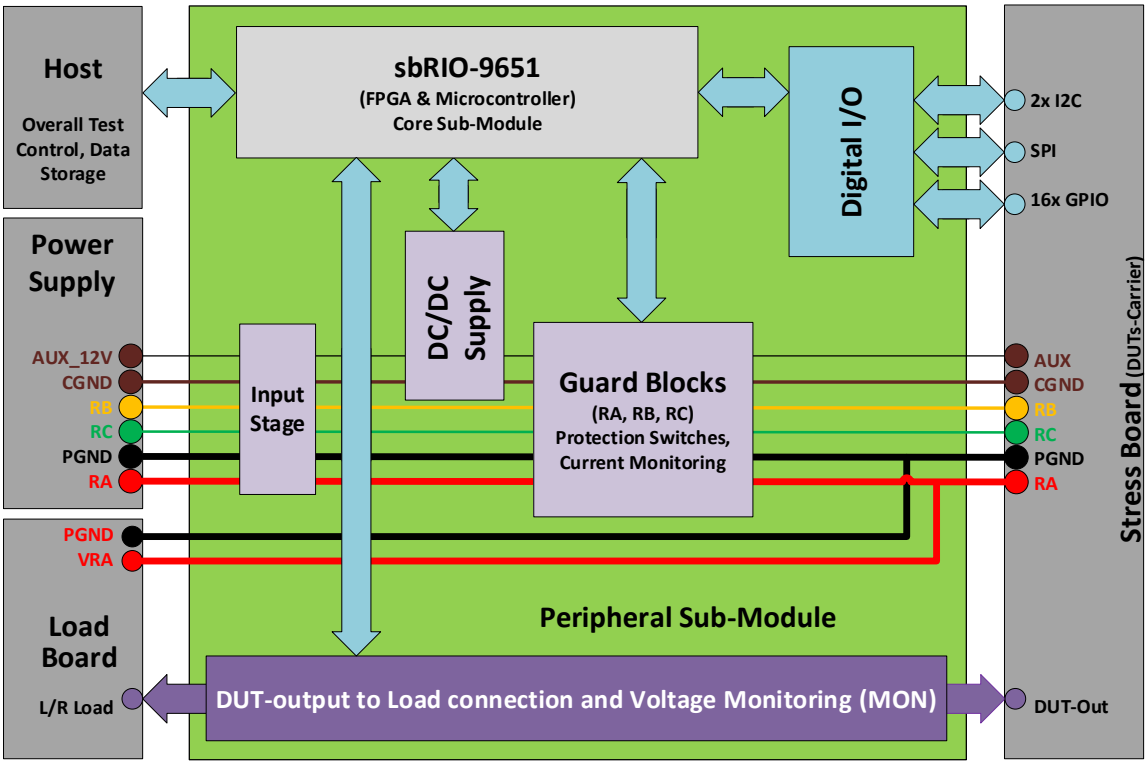


Figure 5.1: Block diagram of the FPGA-based control module. In the top left area, the core sub-module, the sbRIO-9651 from NI, is shown which is plugged onto the *peripheral sub-module*. The latter is depicted as the green rectangle on which all implemented circuit blocks and their connections are shown. In the gray rectangles left and right of the figure, additionally necessary test system components are depicted [19].

capable of supplying various voltage levels to these DUTs. For this reason, the supply of all of these digital functions (GPIO, I^2C, SPI) is adjustable between 1 V and 5.5 V. Thus, the FPGA-based control module is capable of executing tests on DUTs with different supply voltage specifications.

An essential feature of the FPGA-based control module is that it provides guard blocks (shown in the middle of Figure 5.1) to shut down the main power line to the DUTs. It incorporates twelve such guard blocks structured in three groups [4 x rail A (RA), 4 x rail B (RB) and 4 x rail C (RC)], each of which protects one input power rail. The three groups are supplied by external power supplies which are controlled by the host computer of the MTS. Each of the twelve guard blocks incorporates a current sensor and a protection switch function. The current sensor on each power rail is used

for two tasks: The first function is to monitor the input current and shut down in case of an overcurrent event. For this purpose, an analog current limit signal is generated by a DAC channel which is controlled by the sbRIO-9651 and compared to the input current. The second function is the current measurement, where the output of the current sensors is digitized by ADCs and stored as analysis data for the DUT status on the host.

Furthermore, the FPGA-based control module offers 64 voltage measurement channels (described as MON on the bottom of Figure 5.1) realized by multiple ADCs which are controlled by the sbRIO-9651. These voltage measurement channels derive their signals from the connections between the DUTs and the load boards which are routed through the FPGA-based control board. In a hardware setup for an HTOL test, one input power rail supplies multiple DUTs. The DUTs output voltages are routed to individual MON monitoring lines. Hence, the output voltage of each DUT is measured separately, but for the current measurement, the current through multiple DUTs is combined. The reason for this design decision was to not further increase the complexity and cost of the FPGA-based control board. One guard block rail requires a greater amount of components (these are: power transistor, current sensor, comparator, ADC, DAC) compared to the MON voltage measurement (ADC, Op-Amp). Supplying several DUTs from one supply rail via one guard block only, still enables the recognition of a single DUT failure by setting an appropriate current limit.

Table B.8 gives a detailed specification on measurement ranges, resolutions and maximum ratings of the input power rails (RA, RB, RC) and the voltage measurement channels (MON). The measurement accuracy of the power rails was determined by the same method as described for the LV application module in Section 4.1.4. The thereby ascertained measurement accuracy is also listed in Table B.8.

Figure 5.2 illustrates the block diagram of a test system for operating HTOL tests by use of the FPGA-based control modules. On the left side of the figure, the stress board which holds the DUTs is placed within an environmental chamber to stress the DUTs at elevated temperatures. The DUTs themselves are soldered on small DUT boards and are plugged onto the stress boards. In this way, stress boards can be reused for different DUTs. The backplane connector is the connection between the stress board and the FPGA-based control module. One FPGA-based control module is needed per stress board. The FPGA-based control module communicates to the host computer via Ethernet. The host computer is the overall test control entity. DUTs may be power semiconductors which need to be stimulated by a high load current. To achieve this,

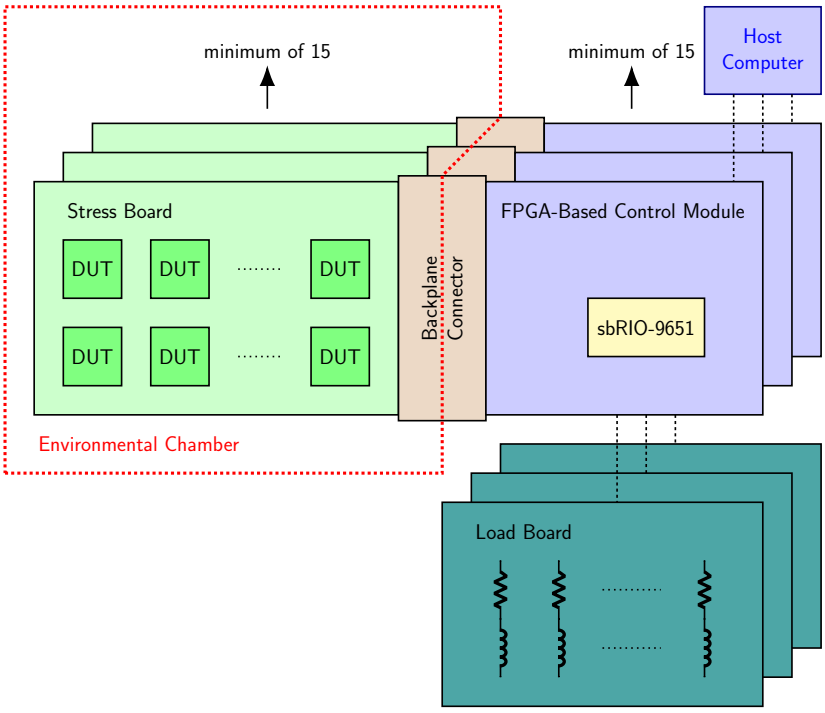


Figure 5.2: Schematic illustration of the necessary elements to establish a test system with FPGA-based control modules. To the left, the stress boards which hold the DUTs within the environmental chamber are depicted. To their right, the connection via the backplane to the FPGA-based control modules is shown. The optionally needed load boards which are connected via the control modules are on the bottom of the picture.

external load boards are used which are depicted in Figure 5.2, to the bottom right. The connection between the DUTs and the load boards is routed through the *peripheral sub-module* to enable monitoring. As the JEDEC-standard [16] defines at least 231 DUTs to be stressed for one full HTOL test, a *minimum of 15* stress boards and control modules is needed if each stress board can carry 16 DUTs. With increasing complexity of the DUTs, a lower number can be controlled by each of the control modules, thus increasing the necessary number of stress boards and control modules (e.g., for 8 DUTs 29 stress boards and control modules are needed).

Figure 5.3 shows the finished FPGA-based control module and the different function blocks are highlighted. Close to the center of the board, and highlighted in red, the sbRIO-9651 *core sub-module* from NI is plugged onto the *peripheral sub-module*. The protection, current and voltage measurement functions are depicted in green and blue.

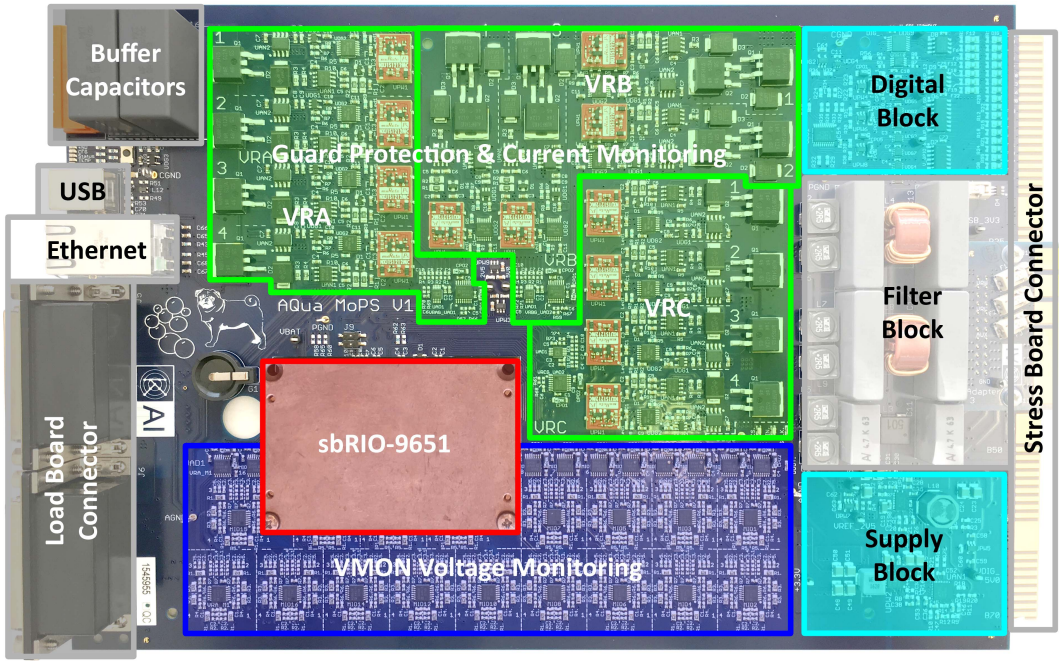


Figure 5.3: The finally manufactured PCB of the FPGA-based control module. The different circuit blocks are highlighted and described.

The connections to host, load board and stress board are highlighted to the left and right of the board.

In right area of Figure 5.3 the filter block is marked. The purpose of this block is to filter the voltage coming from external power supplies by common mode chokes and low pass filters. For each of the three supply rails (RA, RB, RC) one such filter circuit is realized.

In Figure A.4, also a perspective view of this board is depicted.

5.4 Prototype HTOL Test System

Figure A.5 shows the prototype HTOL test system which is based on the novel FPGA-based control modules. In Figure A.5a and Figure A.5b, the plugged stress boards within the environmental chamber and the plugged FPGA-based control modules on the backside are shown, respectively. In both pictures, the long backplane connectors which connect the stress and control boards can be identified. At the bottom right of Figure A.5b, all cabling leading to the main power supplies, the load boards and the host via Ethernet are depicted. The auxiliary supply for the FPGA-based control modules is located at the top of Figure A.5b. Figure A.5c shows the host computer

Table 5.2: Specification of the HTOL Test Setup Frequencies, Timing and Load Configurations.

Setup	Frequency	Period	Duty Cycle	Load Configuration	Free-Wheeling Diode
Setup 1	2 kHz	500 µs	41 %	3.3 Ω + 10 mH	Yes
Setup 2	1 kHz	1 ms	36 %	3.3 Ω + 10 mH	Yes
Setup 3	100 Hz	10 ms	43 %	3.3 Ω + 10 mH	Yes
Setup 4	28 Hz	35.7 ms	2 %	4.7 Ω + 3.3 mH	No

with a screen shot of the fully automated control software and the main power supplies at the bottom. Figure A.5d shows the rack to hold the load boards which are necessary for the prototype HTOL test.

5.5 HTOL Qualification Test and Resulting Data

This section describes a qualification test that has been conducted using this prototype HTOL test system. The DUT is an automotive IC, integrating four low-side switches, which is controlled by an SPI interface. Thus, the task for the FPGA-based control module in this test is to turn on/off the DUTs in a defined pattern and to measure the drain source voltage V_{DS} of each of the four integrated switches.

The detailed test setup is listed in Table 5.2 and the sequence of these setup patterns for the individual switches is shown in Figure 5.4. Each low-side switch from a DUT is subsequently referred to as a *channel* and each of the latter is stimulated by a different setup pattern. Three channels (namely channels 1, 3 and 4) have the same circuit configuration in which their inductive load is connected to a free-wheeling diode in parallel. The setup patterns 1 to 3 are impressed onto channels 1, 3 and 4 and each pattern is rotated after one second as depicted in Figure 5.4. Channel 2 is configured differently. In fact, the output load is realized without a free-wheeling diode in order to force this channel into voltage clamping after every turn off. The voltage is limited at this channel by an integrated clamping structure within the DUT. Hence, channel 2 is always stimulated by the same setup 4. These patterns are repeated for 71 s and after a 1 s break, the loop starts again.

Figure 5.5 shows typical measurement curves of the drain source voltages V_{DS} from every channel/setup configuration. As listed in Table 5.2, each setup pattern has a

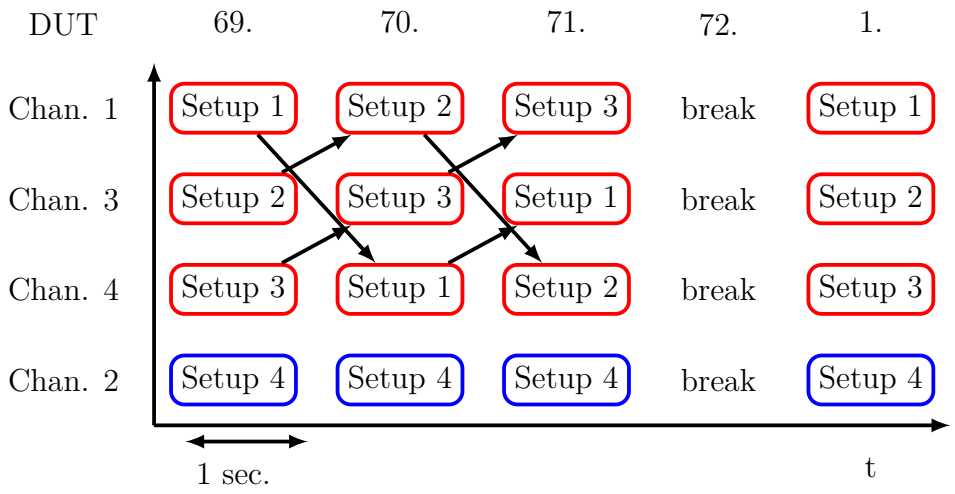
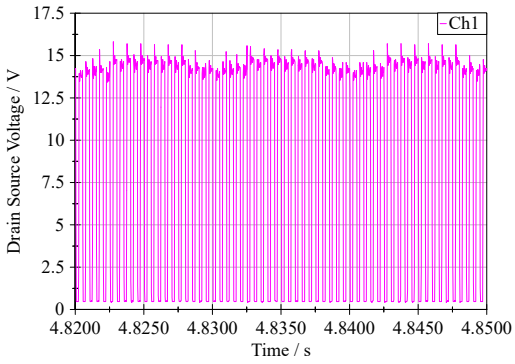


Figure 5.4: HTOL test setup timing: The setup patterns 1 to 3 are impressed onto channels 1, 3, and 4 and each pattern is rotated after one second. Channel 2 is always stimulated by the same setup 4 as it has a differently configured output load.

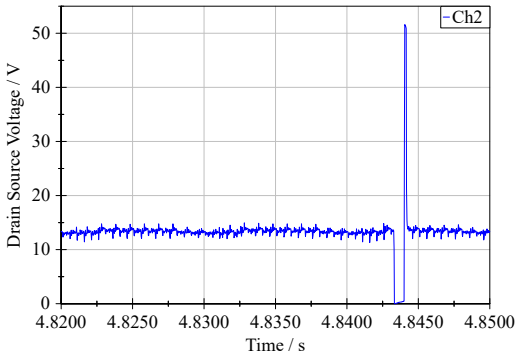
different duty cycle. The latter was defined to set the junction temperature T_j of the DUTs to 125 °C (as demanded by JEDEC [16, p.3]) while considering self heating and the set ambient temperature of 65 °C. Figures 5.5a, 5.5c, and 5.5d show the outputs of the channels with the enabled free-wheeling path at different frequencies. Figure 5.5b shows the measurement curve of the channels which had been operating in voltage clamping.

In this prototype test, five stress boards with four DUTs each were used. All channels of all DUTs are monitored and recorded directly by the new FPGA-based test system, while in legacy test systems this task was realized by separate measurement devices. Thus, the exact synchronization of control and measurement is now possible with the new system. All DUTs and their channels can be driven with independent and individually adjustable setup patterns. The acquisition of one measurement record is performed at a rate of 40 kS/s in these example curves. Hence, the data rate of the FPGA-based control module is fast enough to acquire all stimulated device channels in reasonable quality.

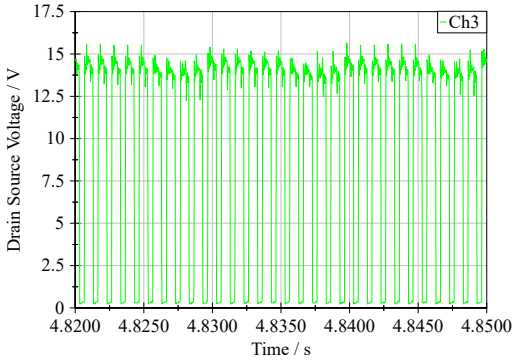
Referring to the resulting measurement curves in Figure 5.5, signal distortion occurs when the high voltage level of approximately 15 V is present. The reason for this issue is illustrated by Figure 5.6, where the circuit details of two adjacent test channels are depicted and explained in the following. If the DUT is in off-state, the ADC measures



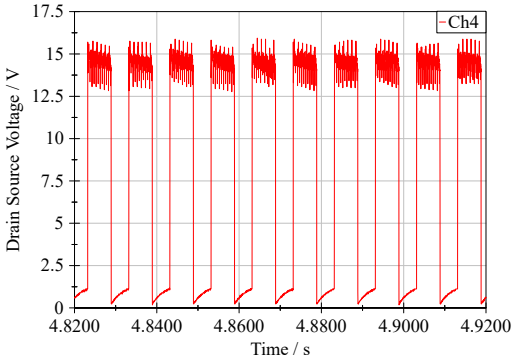
(a) V_{DS} measurement of load channel 1 from one DUT.



(b) V_{DS} measurement of load channel 2 from one DUT.



(c) V_{DS} measurement of load channel 3 from one DUT.



(d) V_{DS} measurement of load channel 4 from one DUT.

Figure 5.5: Measurement records of an HTOL-test conducted with novel FPGA-based control modules. The drain-source voltage V_{DS} of each channel on each DUT was logged over the whole 1000 h test time.

the high voltage level of approximately 15 V which is influenced by noise from adjacent operating test channels.

Figure 5.6 shows that the signal path leads over a long cabling harness to the external load and back to the FPGA-based control module where it is supplied by power rail VRA. Due to the hardware setup of this MTS variant, the long cabling run cannot be avoided, as the load boards must be mounted outside the environmental chamber because of their size and heat loss. Due to this cabling run, it is unavoidable that the measurement signal picks up noise in the DUT's off-state, as visible by the ringing in Figure 5.5. The noise is transmitted due to Electromagnetic Interference (EMI) between

the cables which are unfortunately not twisted paired and over the FPGA-based control module's common ground potential.

However, in the DUT's on-state, the measurement results are noiseless (compare the low voltage levels of approximately 0.5 V in Figure 5.5) and hence valid, as in this case the measurement path is low ohmic. Thus, the noise from the external cabling does not interfere the measurement as also the ADCs are located nearer to the DUTs in this case.

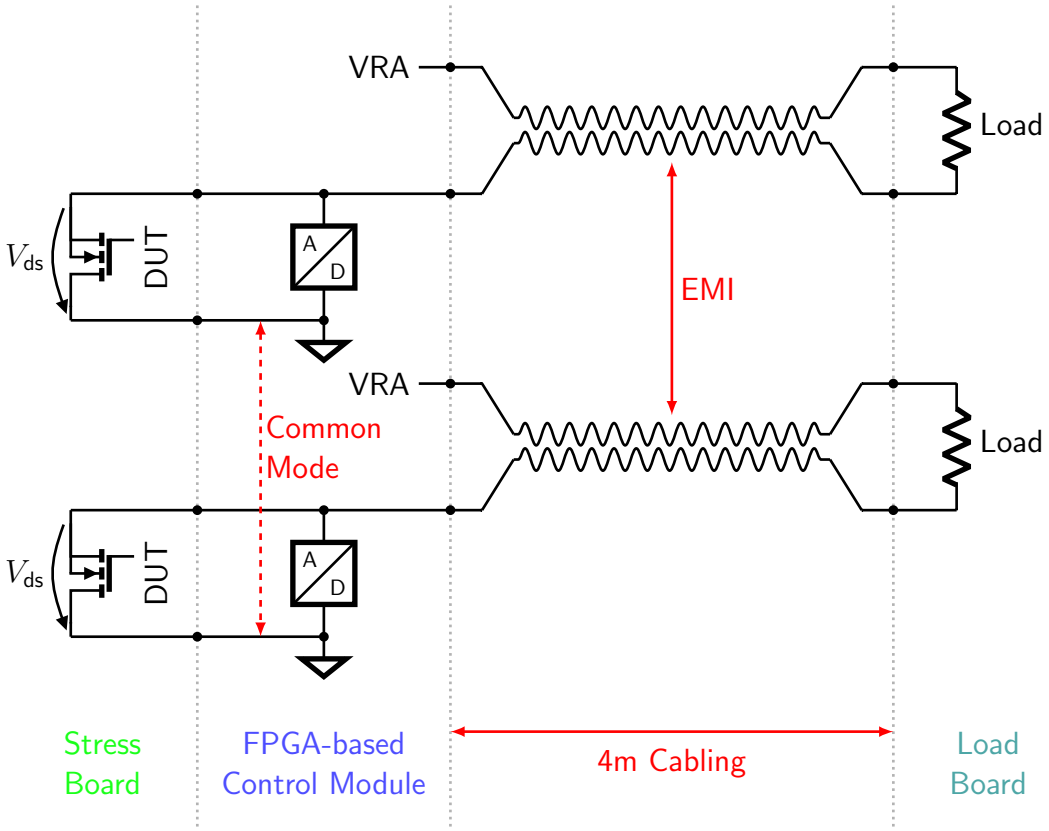


Figure 5.6: In this figure, two adjacent test channels of the MTS variant with FPGA-based control modules are illustrated. The problem of the injected noise can be seen at the cabling. Due to the hardware setup, the cabling run needs to be 4 m long and the wires are not assembled in twisted pair configuration. Hence, in the DUT's off-state, the noise picked up via the cabling from adjacent operating channels deteriorates the measurement results.

Chapter 6

Data Processing and Reduction

The continuous acquisition of digitized measurement data of analog sources is a common task in life test systems. A vast amount of data is produced and stored for later analysis. Life test data commonly comprise long periods of time during which the monitored signals are constant. Such characteristics suggest the use of data reduction techniques so as to reduce storage requirements and facilitate later data processing.

A further common characteristic of life test data is that values increase rather slowly but steadily. In this case, it may be reasonable to store only differences between two adjacent data sets. In this chapter, three approaches are proposed to reduce the size of measured data and to filter for relevant information. These approaches are: (Section 6.1) real-time measurement data compression, (Section 6.2) significant sample point selection, and (Section 6.3) failure event triggering.

6.1 Real-Time Measurement Data Compression

To monitor measurements executed by a short circuit test system [36], 14 bit-wide current and voltage waveform data are continuously acquired [86]. Usually, word size is in multiples of 8 bit and thus, the 14 bit data must be stored in a 16 bit-wide variable, wasting about 12.5 % of the available space. Data compression techniques can be utilized to improve the storage ratio.

In a waveform record, consecutive data samples only differ slightly. Hence, storing the difference can significantly reduce the required amount of bits. To encode smaller values with fewer bits, flexible data coding schemes are desired. Several possible coding candidates are already known [87] and explained in the following paragraphs. However, few of them can be implemented efficiently within a real-time capable setup.

On the whole, two methods for lossless compression are distinguished between, namely, *entropy based* and *dictionary based*. *Dictionary based* methods search for repeating patterns in the input and replace them with shorter symbols (e.g., the index in the dictionary). Examples for *dictionary based* compression are DEFLATE and many variants of the so-called "Lempel-Ziv" algorithms (LZ77, LZ78, LZMA, etc.) As a drawback, the dictionary must be created, stored and transmitted in addition to the compressed data, increasing the resource utilization.

In contrast to the *dictionary based* algorithms, *entropy coding* methods assign symbols with a variable length to the input words, thus reducing the overall number of bits. Well-known representatives of this methods are Huffman coding, arithmetic coding and the so-called *universal codes*. The two first coding schemes are based on the fact that the probability distribution of the input data is known. This is not the case when analog data is sampled. Further, the created probability table again needs to be stored and transmitted so as to decode the data.

Among the entropy coding, *universal coding* schemes assume a monotonic probability distribution of the input samples, thereby coding smaller positive numbers by shorter symbols. To demonstrate real-time measurement data compression, we have chosen *Fibonacci coding* because it can be efficiently implemented on both embedded microcontrollers as well as FPGAs.

$$\Delta V = V_{\mathrm{n}} - V_{\mathrm{n-1}} \tag{6.1}$$

$$S = 2 \cdot |\Delta V| + \begin{cases} 1 & \Delta V < 1 \\ 0 & \text{otherwise} \end{cases} \tag{6.2}$$

In Equations (6.1) and (6.2) V_{n} are the sampled measurement values and S stands for the symbols.

Our proposed solution consists of three stages: first, the difference of consecutive samples is computed (6.1). These values need to be converted into positive integers for further encoding. To map the smallest differences to the shorter symbols, (6.2) is used. Thus, differences of (0, 1, -1, 2, -2, ...) are converted into the symbols (1, 2, 3, 4, 5, ...).

Next, the integers are encoded using Fibonacci coding. The resulting symbols have variable lengths, but they can be glued together into a continuous stream by adding a

stop bit. This is possible due to Zeckendorf's theorem [88], in which encoded symbols are not allowed to be encoded with successive bits which are 1. Finally, the values can be stored in 32 bit data locations (because both microcontroller architecture and Peripheral Component Interconnect (PCI) bus width are 32 bit wide) to be transmitted to the host and storage location.

On the host, the stop bits decode the received data and split them. Then, individual symbols can be decoded into the original absolute samples.

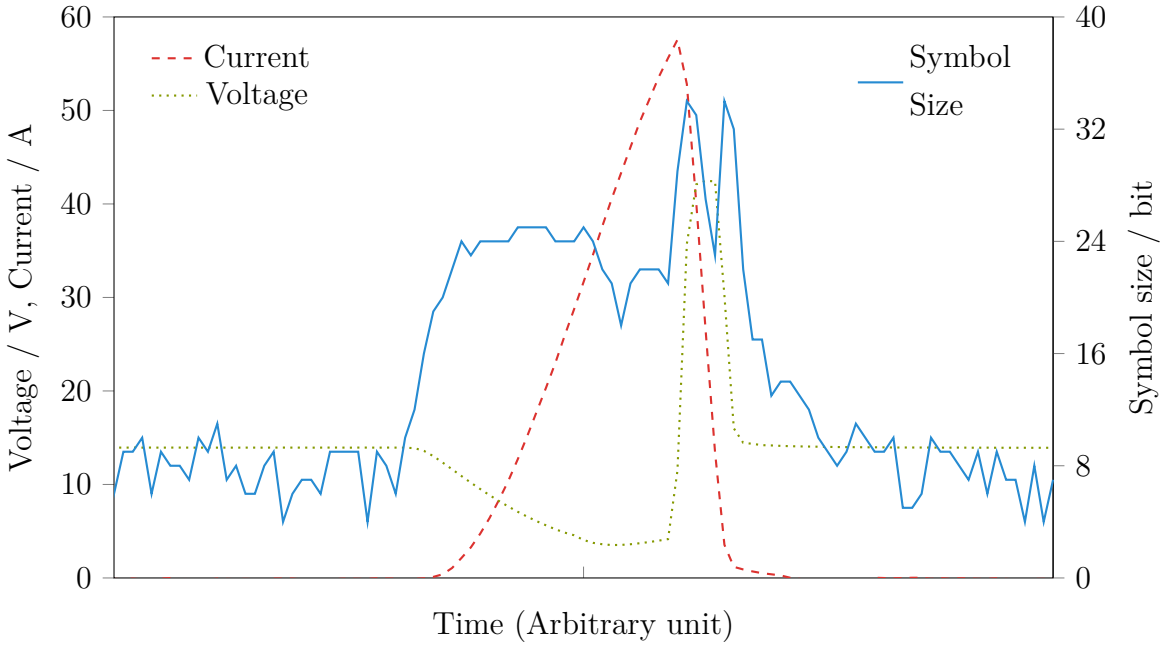


Figure 6.1: Typical symbol size for the samples within a waveform record.[1]

Figure 6.1 shows a typical data set. Acquired voltage and current as well as the required number of bits per symbol, can be seen. To encode our 2 × 14 bit samples, we need between 4 bit and 46 bit per sample. The complete waveform of 12,288 samples can be stored in about 3,000 32 bit words. Hence, a sample takes up an average of 7.8 bit. Typically, compression ratios close to 25 % (of the uncompressed data) are possible. In comparison, the same data compressed on a desktop machine using DEFLATE [87] yields a slightly better compression ratio of 23 %.

[1] Unfortunately, for reasons of confidentiality, not all quantities can be shown in this figure.

6.2 Significant Sample Point Selection

As shown in Section 6.1, a lossless compression of the raw measurement data leads to ratios of approximately 25 %. In order to obtain significantly better ratios, some data must be discarded. Using another particular method, measurement data can be drastically reduced while retaining the significant information. Figure 6.2 shows an example of a measurement record taken periodically by a short circuit test system [36]. 10,000 samples per record are acquired for each measurement channel. Merely a fraction of the original number of samples is sufficient to reproduce the pulse shape of the curves.

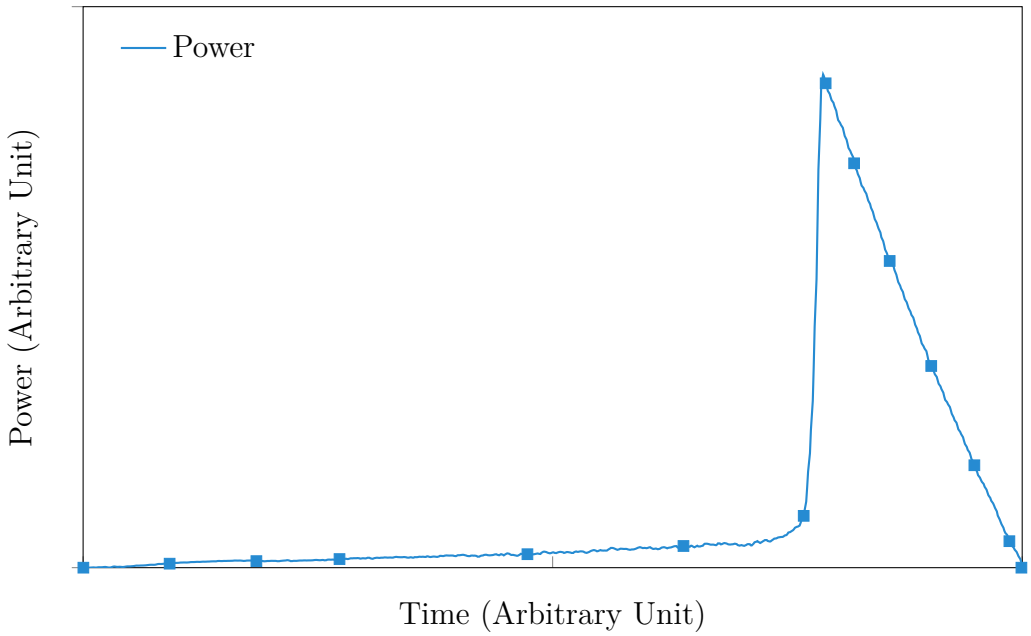


Figure 6.2: Example of a sample point extraction from a power waveform with 10,000 samples.[2]

This method only applies to measurements where the curve shape is known. In the described case here, the curve has only *one* maximum value, as shown in Figure 6.2. First, by looping through one waveform record, this maximum value is determined. Then, the waveform is split into two segments left and right of its maximum value. A sample point is identified and stored when either the time or the value drop exceeds a relative limit. Figure 6.2 shows a typical data set, consisting of the acquired power dissipation (——), and the selected significant sampling points (■) thereof. These sample

[2]Unfortunately, for reasons of confidentiality, not all quantities can be shown in this figure.

points may be stored and can also be used as a Piece-Wise Linear (PWL) description for a circuit simulator. Using this method, the amount of stored data can greatly be reduced (by about 650 times in this example) with only minor information loss.

Certainly, previous knowledge of the pulse shape of the measurement data is necessary to apply this method. As in general, life test systems periodically record similar measurement data for each pulse, and this method is suitable for such systems.

6.3 Failure Event Triggering

To further reduce the amount of stored data, we introduce failure event detection and triggered data storage. In this method, the test pulses are continuously sampled and stored in a circular buffer. The recorded data in this buffer is overwritten every test cycle.

Since the typical response of the DUT is known, we can define a set of parameters that must not be violated, e.g., peak amplitude or maximum pulse width. The parameters can be computed directly on the embedded control module with a small overhead. When a parametric violation triggers this in situ diagnosis, the most recent waveform stored in the circular buffer is tagged with the event and transferred to the host for long term storage and possible manual or automated inspection. In addition, the extracted waveform parameters are smaller in size and can be stored once every measurement cycle.

Furthermore, as the test application is protected with a guard module as mentioned in Section 1.4.2, the trigger signal of the guard can also be used as an event to store the acquired measurement data. This feature allows us to greatly increase the probability of capturing the waveform of the DUT's destruction (i.e., *failure waveform*) while reducing the overall amount of stored data.

This method can also be denoted as measurement data reduction because it is neither reasonable to store *each* acquired waveform record nor is it possible due to limited storage. However, it is of particular interest to store the waveform at the exact point in time when the device fails within a long term life test.

Chapter 7

Conclusion

7.1 Summary

In this work, the topic of life testing of power semiconductor devices is comprehensively covered. After an introduction to the topic, various compulsory tests are discussed which are required when bringing new devices to the market. Previous literature on this topic typically focuses on the DUT and how to improve it. However, in this work the test system itself is in central focus and the question of how to establish efficiently reusable test hardware and software is explored.

Hence, the Modular Test System architecture is introduced which provides numerous benefits, listed hereafter, compared to a legacy centralized approach:

- Reuse of hardware and software
- In situ device status logging; condition monitoring
- Circuit protection
- Failure event detection
- Load profiles; mission profiles
- Control of external periphery

In Table 7.1, an overview is given of the different currently available tests systems developed at KAI and described within this work. The upper four rows of the table list all test systems that are based on the MTS architecture and explained in this work. The LV and MV MTS are comprehensively described in Chapter 4 and the FPGA-enabled MTS is discussed in Chapter 5. The High Voltage (HV) MTS is currently under

development at KAI and is included in the list for the sake of completeness. It will enable life tests for high voltage SiC transistors and will be controlled by the control module introduced in Section 3.2. Deeper design details on this system will be treated in a separate future thesis.

Regarding the technology of the DUTs, thus far MTS variants for testing Si MOSFETs and GaN transistors have been realized. However, none are available yet for testing IGBT devices or modules, even though the MTS would certainly allow the implementation of such MTS variants. Currently, as the focus of our research is on the emerging wide band gap semiconductors, test systems are mainly developed for this technology.

In the lower three rows of Table 7.1, legacy test systems which were developed within former projects at KAI are listed for comparison. All three systems have a *centralized* architecture and are thus limited in their ability to be adapted for different DUTs or to provide additional measurement parameters.

Table 7.1 also reveals that previously *device-specific* test system types were demanded, whereas the current systems are designed for *application-specific* tests. Hence, a major advantage of the MTS architecture is that it can flexibly be used for both of these test types.

Column four of Table 7.1 shows how many test systems have already been established in a productive setup at the key customer of KAI which is Infineon Technologies AG. Column five provides one significant difference between *application* and *device-specific* tests, namely the amount of available test channels of the respective test system.

Regarding the possible measurable parameters, Table 7.1 reveals the clear advantage of the MTS architecture, namely, that significantly more parameters can be logged. The rightmost four columns describe the elements which the listed test systems have in common. It shows that the first three systems are based on the MTS architecture and have an abundance of similar and consequently reusable building blocks in common. For the FPGA-based MTS, the control module needed to be adapted due to the much higher DUT count. Nevertheless, it still shares many elements of the MTS architecture.

For the previously developed test systems at KAI, listed in the last two rows of Table 7.1, the sharing of system elements was also considered, but not for the main hardware setup of the test systems. Thus, this shows the clear progress introduced by use of the MTS architecture: Here, the hardware parts are also split into modules to foster their reusability.

Table 7.1: In this table, the currently available test systems are listed. The systems marked in red are all based on the MTS architecture. The last three are legacy test systems with centralized architecture and given for comparison. In the rightmost four columns, the elements which are in common for the test systems are depicted.

Description	Type	Purpose	Systems	Capacity	Voltage Rating	Current Rating	Measurement Parameters	Compatibility			
								control module	software framework	guard block IP	V & I measurements IP
LV MTS [18]	application-specific	step-down converter (PoL)	3	24	16 V	20 A[1] 60 A[2]	V_{in}, V_{out}, I_{in}, I_{out}, T_c, I_{mon}, T_{mon}				
MV MTS [23]	application-specific	step-up converter (PFC)	1	24	700 V	20 A[1]	V_{in}, V_{out}, $V_{DS,ls}$, I_L, $T_{c,ls}$, $T_{c,hs}$				
HV MTS	application-specific	solar inverter	1[3]	9[3]	1.2 kV	40 A	V_{in}, V_{out}, I_L, 2·V_{DS}, 2·V_{GS}, 2·I_S, 2·T_c,				
FPGA-enabled MTS [21]	device-specific	HTOL qualification	1[4]	231[4]	120 V	6 A[1]	4·I_{RA}, 4·I_{RB}, 4·I_{RC}, 64·V_{MON}				
HTOL legacy system [20]	device-specific	HTOL qualification	15	231	120 V	6 A[1]	with separate equipment only				
Short circuit system [36]	device-specific	short circuit of automotive devices	10	256	60 V	500 A[2]	V_{DS}, I_D, $R_{DS,on}$	software	DUT boards		
Repetitive [62] clamping system	device-specific	inductive load switching	4	256	100 V	20 A[2]	V_{DS}, I_D				

[1]continuous, [2]pulsed, [3]planned to be realized in fall 2018, [4]available prototype system with 20 test slots

7.2 Discussion

The boundaries of designing modular test systems shall be illustrated by the following two selected examples.

Table B.9 lists all 20 analog input channels which are available on the control module. In this table, the large variation in the input voltage ranges of each channel is recognizable. The voltage ranges of the first 8 channels in the list are attenuated by Op-Amps which are implemented on the control module; as opposed to the remaining 12 channels which are directly connected – besides a line protection – to the ADC inputs of the XMC4500 microcontroller. Thus, the latter 12 channels provide the native voltage range from 0 V to +3 V of the ADCs.

In Figure 4.4, this difference in the provided analog input channels is graphically illustrated. In this figure, the current measurement signals coming from the current sensors are attenuated by Op-Amps which are implemented on the application module, whereas for the voltage measurement, the Op-Amps are located on the control module and one of first 8 channels from Table B.9 is used to measure the voltage.

Based on the realized control and application modules (i.e., used in LV and MV MTS), it was learned through practice that this inconsistency of providing different voltage ranges on the control module is not a favorable solution. By considering this example, it can be stated where it is preferable to define the boundary between the modules: Namely, directly after the ADC inputs on the control module. Hence, it is proposed for future designs to implement all circuitry needed to attenuate the measurement signals on the application modules.

The explanation for this proposal is that it does not bear a big advantage to provide different uni- or bipolar input channels before the actual application board is realized. Naturally, no one can anticipate the wide range of future application requirements in advance. It is more reasonable and flexible to implement the analog signal conditioning on the application board at the time, when the target voltage range is known. Thus, the whole measurement range of the ADC is utilized and this is essential to achieve a high measurement accuracy in the final test system.

In the realized FPGA-based control module (Chapter 5) the aforementioned approach is already followed. The attenuation of all measurement channels (VMON, VRx) is implemented on the *peripheral sub-module*. The *core sub-module* executes only the communication per SPI-interface to the ADCs which are all implemented on the *peripheral sub-module*.

For the already realized test systems with the control module described in Section 3.2, this design change cannot be easily introduced in a redesign, as the compatibility with the available application modules would be violated. However, for a new MTS based test system design, this approach of separating signal conditioning and A/D conversion between control and application modules is recommended.

In fact, there is an advantage to use differential signal paths until the ADC-inputs in favor of single-ended signal routing: Transmitting signals over a long distance and connectors provokes noise injection. Differential signals with higher amplitude have a better Signal-to-Noise Ratio (SNR) compared to single-ended routing. In a modular system this is the trade off between flexibility and high signal quality. As in the MTS architecture the control module is connected closely to the application module, the noise injection is not significantly disturbing. Thus, for the MTS the flexibility has the higher benefit.

A further possible area of improvement concerns the investigation and adjustment of the test systems' measurement accuracy, as described in Section 4.1.4. All accuracy investigations described in this work were only conducted at an ambient temperature of 25 °C. As ICs typically have a temperature dependent behavior, it is strongly advisable to perform accuracy investigations also at high and low temperatures. For the life test systems this is also a relevant issue, as DUTs are typically tested at a high ambient temperature and thus also the test circuits are exposed to the same environment.

7.3 Outlook

In the future, further types of test systems based on the MTS architecture will be developed.

For the previously mentioned HV MTS, the degree of modularity will be further increased. It is designed for life testing of SiC transistors and emulates the application of a solar inverter. Thus, the voltage/power class is significantly higher compared to the test systems introduced in this work. As shown in Table 7.1, the SiC transistors need to be stressed at voltages up to 1.2 kV and at a maximum current of I_{rms}=40 A. Due to this voltage requirement, a galvanic isolation between the control module and the power circuit is necessary. As of the higher physical dimensions, the filter elements are placed on the base board in contrast to the LV MTS, where the filter inductor is soldered directly onto the DUT board. The driver circuit for the SiC transistors is realized on separate boards and hence, the modularity is further increased in this test

system variant. A prototype of this system is currently under development at KAI within another project group. This system is based on the MTS architecture and uses the same control module as introduced in Section 3.2. A productive test system is scheduled to be established by fall 2018.

Another project will be based on the MV MTS: The goal of this project is to develop stress test concepts for GaN transistors which are operated at switching frequencies in the range of 1 MHz to 10 MHz. For comparison, the MV MTS described in Section 4.2.1 runs at a maximum switching frequency of 100 kHz. Thus, new concepts are needed to achieve this frequency increase. This project will be realized and published within a future dissertation.

A third project will focus on the development of a test system which is compliant to JEDEC-standards [16], [45]. The control concept for this test system will be similar to the FPGA-based control module introduced in Chapter 5. Thus, the test system should be able to stress at least 231 DUTs. However, the target devices require a higher voltage class of 1.5 kV and hence, new concepts to handle both the high amount of DUTs and the high voltage are the key challenges of this project.

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Glossary

AEC The Automotive Electronics Council (AEC) was originally established by Chrysler, Ford, and GM for the purpose of establishing common part-qualification and quality-system standards. From its inception, the AEC has consisted of two Committees: the Quality Systems Committee and the Component Technical Committee. The AEC Component Technical Committee is the standardization body for establishing standards for reliable, high quality electronic components. Components meeting these specifications are suitable for use in the harsh automotive environment without additional component-level qualification testing. See http://www.aecouncil.com

JEDEC (Joint Electron Device Engineering Council) is the global leader in developing open standards for the microelectronics industry. JEDEC brings manufacturers and suppliers together with the mission to create standards to meet the diverse technical and developmental needs of the industry. JEDEC's collaborative efforts ensure product interoperability, benefiting the industry and ultimately consumers by decreasing time-to-market and reducing product development costs. JEDEC publications and standards are accepted throughout the world, and are free and open to all. See https://www.jedec.org/

LabVIEW LabVIEW (Laboratory Virtual Instrument Engineering Workbench) is a development environment used for instrument control and data acquisition using a graphical programming language. See http://ni.com/labview

National Instruments A United States company producing test and measurement equipment and developing the LabVIEW software platform. See http://ni.com

Acronyms

A/D Analog-to-Digital

ADC Analog-to-Digital Converter

ATE Automated Test Equipment

CPU Central Processing Unit

D/A Digital-to-Analog

DAC Digital-to-Analog Converter

DC Direct Current

DUT Device Under Test

EAM Institut für Elektrische Antriebstechnik und Maschinen an der TU Graz

EMI Electromagnetic Interference

EOL End of Life

FPGA Field Programmable Gate Array

FSM Finite-State Machine

GaN Gallium Nitride

GPIO General Purpose Input Output

HEMT High Electron Mobility Transistor

HTOL High Temperature Operating Life

HV High Voltage

I²C Inter-Integrated Circuit

IC Integrated Circuit

IGBT Insulated Gate Bipolar Transistor

IP Intellectual Property

KAI Kompetenzzentrum Automobil- und Industrie-Elektronik

LED Light Emitting Diode

LV Low Voltage

MOS Metal Oxide Semiconductor

MOSFET Metal-Oxide Semiconductor Field Effect Transistor

MTS Modular Test System

MTTF Mean Time To Failure

MV Mid Voltage

Op-Amp Operational Amplifier

PCB Printed Circuit Board

PCI Peripheral Component Interconnect

PFC Power Factor Correction

PI Proportional-Integral

PoL Point-of-Load

PWL Piece-Wise Linear

PWM Pulse Width Modulation

PXI PCI eXtensions for Instrumentation

Si Silicon

SiC Silicon Carbide

SNR Signal-to-Noise Ratio

SOA Safe Operating Area

SPI Serial Peripheral Interface

SPS Smart Power Switch

UART Universal Asynchronous Receiver Transmitter

UID Unique Identification

USB Universal Serial Bus

UUT Unit Under Test

List of Symbols

C_{buf} Buffer capacitance

C_{in} Input capacitance

I_{D} Drain current of a MOS transistor

I_{L} Current through the inductor of a power converter circuit

I_{RA} Current through power rail A

I_{RB} Current through power rail B

I_{RC} Current through power rail C

I_{S} Source current

I_{drv} Driver current

I_{in} Input current

I_{load} Load current at the output of a power converter

I_{max} Maximum current rating

I_{mon} Current monitor signal produced by an IC

I_{out} Output current

I_{rms} Root-mean-square current rating

$R_{\mathsf{DS,on}}$ On-state resistance of a MOS transistor

R_{chg} Charge resistance

T_{amb} Ambient temperature

T_{brd} PCB temperature at a defined location

$T_{\mathsf{c,hs}}$ Case temperature of the high-side transistor in a half-bride circuit

$T_{\mathsf{c,ls}}$ Case temperature of the low-side transistor in a half-bride circuit

T_{c} Case temperature of a semiconductor device

T_{j} Temperature at the junction of a power semiconductor device

T_{mon} Temperature monitor signal produced by an IC

V_{CE} Collector-emitter voltage of an IGBT

$V_{\mathsf{DS,ls}}$ Drain-source voltage of the low-side transistor in a half-bride circuit

V_{DS} Drain-source voltage of a transistor

V_{F} Forward voltage

V_{GS} Gate-source voltage of a transistor

V_{MON} Voltage monitoring channels

V_{drv} Driver voltage

V_{in} Input voltage

V_{max} Maximum voltage rating

V_{out} Output voltage

λ Failure rate

τ Failure-free operating time

f_{sw} Switching frequency

Appendix A

Test System Hardware Pictures

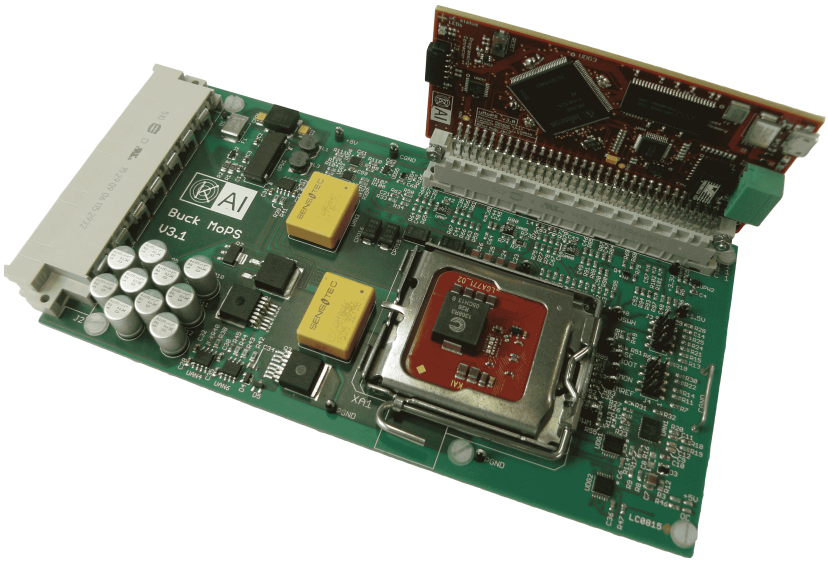

Figure A.1: One test unit of the LV MTS is depicted. In the center, the red DUT board is shown which is a separate PCB holding the DUT. In the top right area, the control module PCB is connected which is equipped with an Infineon XMC4500 microcontroller. Several monitoring functions are provided on the base board. E.g., the yellow components are the current sensors and the black large ICs to the left are the guard transistors.

Figure A.2: In this picture, a completely established LV MTS is shown. The test units (which are shown in Figure A.1) are mounted within the climate chamber and the peripheral devices, like power supplies, electronic multi-load, host computer and an additional high voltage safety protection system are located in the 19" rack to the left.

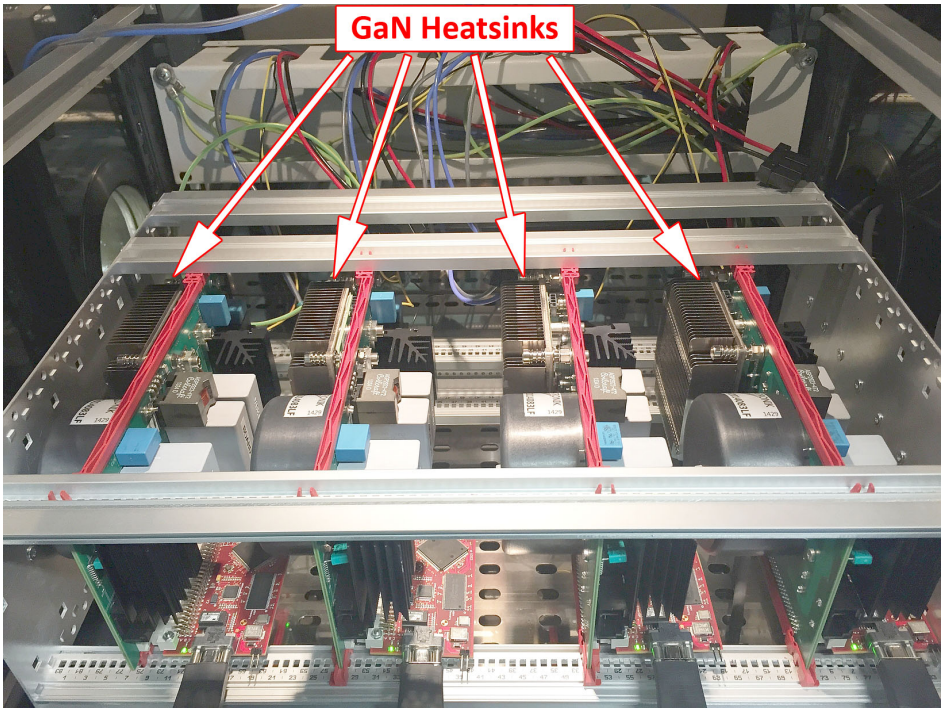

Figure A.3: Four MV MTS application boards are mounted in a 19” rack case which is placed within an environmental chamber. In the center of the figure, the heat sinks can be seen which cover the GaN transistors. At the bottom and in red PCB color the connected control modules are situated. The black inductors for the boost conversion in the center-bottom area are also distinctly visible [23].

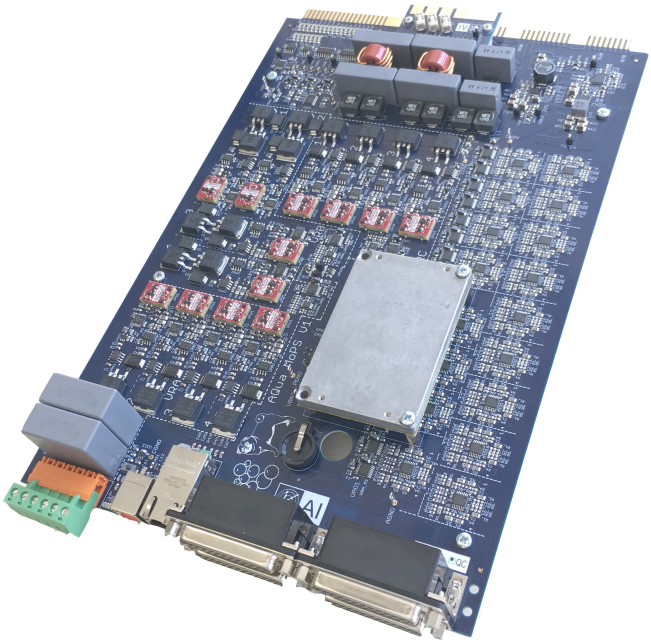

Figure A.4: Aspect view of the final manufactured PCB of the FPGA-based control module. The core sub-module sbRIO-9651 is located approximately in the center which is the solid light gray block. In the top area, the long PCB edge connector which interfaces the backplane connector in the test system can be seen. On the bottom, the black sub-D connectors are the interface to the load boards and next to them on the left, the Ethernet connector is located.

(a) Stress boards within the environmental chamber.

(b) At the backside of (a): FPGA-based control modules with cabling.

(c) Host computer and main power supplies.

(d) The load boards are mounted within a separate rack which is located beside (a) and below (c).

Figure A.5: Essential elements of a completely established MTS to perform HTOL-tests with the novel FPGA-based control modules, are illustrated.

Appendix B

Test System Specification Tables

Table B.1: Input current measurement mapping of the LV MTS.

I_{in} / A	Current Sensor / V	ADC input / V
−5 A	+2.2 V	0 V
0 A	+2.5 V	+1 V
+10 A	+3.1 V	+3 V

Table B.2: Output current measurement mapping of the LV MTS.

I_{out} / A	Current Sensor / V	ADC input / V
−5 A	+2.41 V	0 V
0 A	+2.50 V	+0.2 V
+70 A	+3.76 V	+3 V

Table B.3: This table lists the ranges of the measurement channels at the LV application module. It furthermore states the maximum possible values once the module is in operation or if the DUT is shorted and turned off. The red colored text in column four means that this is the crucial reason why this test variant was neglected: The possible I_{out} range is too low in this case. The blue marked lines in column three mean that for these parameters not the full designed range is achievable, but this variant is still in favor of column four, because of the larger I_{out} range.

Parameter	Measurement Range by Design	With DUT Conversion running	Short instead of DUT Conversion off
I_{in}	−5 A to 10 A	0 A to 6 A	0 A to 10 A
I_{out}	−5 A to 70 A	0 A to 50 A	0 A to 10 A
V_{in}	0 V to 20 V	2 V to 16 V	0 V to 20 V
V_{out}	0 V to 5 V	0.6 V to 3.6 V	0 V to 5 V

Table B.4: This table lists settings which were used for the calibration procedure (Section 4.1.4) of the LV application module.

Description	Set Value
Switching Frequency	500 kHz
Sampling Frequency	100 kS/s
Cutoff Frequency	10 kHz
Averaged Values n	256

Table B.5: This table lists the calculated accuracy of the LV application module. All components contributing to the error are listed and the resulting total error.

Component	V_{in}	V_{out}	I_{in}	I_{out}
Resistors tolerance	±0.24 %	±0.24 %	±0.24 %	±0.24 %
Op-Amp [89] offset error	±0.0021 %	±0.0021 %	±0.0021 %	±0.0021 %
ADC [73] total error	±0.098 %	±0.098 %	±0.098 %	±0.098 %
Current sensor total error [81], [90]			±1.3 %	±1.3 %
Total error	±0.259 %	±0.259 %	±1.325 %	±1.325 %

All values are valid for T_{amb}=25 °C

Table B.6: This table summarizes the current accuracy investigations executed on the LV application modules. Four different boards were tested. While the slopes of the boards only differ slightly, the offset values show a higher difference. In the last row, the final accuracy is stated, including the accuracy of the reference device. All values are valid for T_{amb}=25 °C.

Board Number	I_{in} Slope	I_{in} Offset	I_{in} Error rdg.[1]	I_{in} Error f.s.[2]	I_{out} Slope	I_{out} Offset	I_{out} Error rdg.[1]	I_{out} Error f.s.[2]
by Design	0.21	−5 A			0.0415	−5 A		
1411218	0.213351	−4.610 32 A	±0.40 %	±0.07 %	0.043228	−4.377 91 A	±0.41 %	±0.09 %
1411219	0.211366	−4.674 26 A	±0.60 %	±0.09 %	0.042715	−4.339 75 A	±0.34 %	±0.08 %
1468402	0.211552	−4.650 41 A	±0.56 %	±0.13 %	0.043135	−4.003 17 A	±0.73 %	±0.15 %
1468407	0.21178	−4.659 87 A	±0.43 %	±0.09 %	0.042939	−3.902 31 A	±0.40 %	±0.00 %
Average	0.212012	−4.648 71 A	±0.50 %	±0.10 %	0.043004	−4.155 78 A	±0.47 %	±0.08 %
Including Reference [80, p.140]			±0.51 %	±0.14 %			±0.48 %	±0.13 %

[1]Relative error of reading

[2]Relative error of full scale

Table B.7: This table presents the voltage measurement accuracy of the LV application module. It reveals that the slope can be accurately determined by calculation, as the measurement path consists of only an Op-Amp and the ADC. Furthermore, the offset values are small, thus the voltage measurement on the LV application module exhibits a high accuracy. All values are valid for T_{amb}=25 °C.

Board Number	V_{in} Slope	V_{in} Offset	V_{in} Error rdg.[1]	V_{in} Error f.s.[2]	V_{out} Slope	V_{out} Offset	V_{out} Error rdg.[1]	V_{out} Error f.s.[2]
Calculated	4.883E-3	0 V			1.221E-3	0 V		
1411218	4.896E-3	4.525E-3 V	±0.009 %	±0.004 %	1.220E-3	-4.290E-3 V	±0.028 %	±0.012 %
1411219	4.896E-3	4.895E-3 V	±0.012 %	±0.005 %	1.220E-3	-4.692E-3 V	±0.022 %	±0.009 %
1468402	4.895E-3	8.924E-3 V	±0.015 %	±0.006 %	1.220E-3	-2.467E-3 V	±0.017 %	±0.008 %
1468407	4.896E-3	7.256E-3 V	±0.013 %	±0.005 %	1.220E-3	-3.174E-3 V	±0.023 %	±0.011 %
Average	4.896E-3	6.400E-3 V	±0.012 %	±0.005 %	1.220E-3	-3.656E-3 V	±0.023 %	±0.010 %
Including Reference [80, p.140]			±0.101 %	±0.100 %			±0.103 %	±0.100 %

[1]Relative error of reading

[2]Relative error of full scale

Table B.8: Measurement ranges, resolutions and maximum ratings of the FPGA-based control module. This module is described in Chapter 5.

Parameter	Symbol	No. of Chan.	Min.	Typ.	Max.
MON voltage measurement range	VMON	64	−120 V		+120 V
Rail A current measurement range	IRA	4	0 A		+24 A
Rail B current measurement range	IRB	4	−6 A		+6 A
Rail C current measurement range	IRC	4	0 A		+6 A
MON RMS current rating	$IMON_{RMS}$	64			+5 A
Rail A voltage rating	VRA	4	0 V		+100 V
Rail B voltage rating	VRB	4	−100 V		+100 V
Rail C voltage rating	VRC	4	0 V		+100 V
MON measurement resolution	MON_{res}	64		58.6 mV/LSB[1]	
Rail A measurement resolution	RA_{res}	4		12.2 mA/LSB[1]	
Rail B,C measurement resolution	RB_{res}, RC_{res}	4		6.6 mA/LSB[1]	
Rail A measurement accuracy	RA_{acc}	4		0.5 %[2]	
Rail B measurement accuracy	RB_{acc}	4		3.5 %[2]	
Rail C measurement accuracy	RC_{acc}	4		1.4 %[2]	

[1]Measured by 12-bit ADCs

[2]Valid for T_{amb}=25 °C

Table B.9: In this table, all available analog input channels of the control module are listed. The voltage ranges of the first eight channels in the list are attenuated by Op-Amps implemented on the control board. The remaining channels connect, after a line protection, directly to the ADC inputs of the XMC4500 microcontroller and thus provide the native voltage range of 0 V to 3 V.

Channel	Group	Port.Pin	Voltage Range		Type
ASY00A	0	P14.00	−61.0 V	+61.0 V	differential
ASY01A	0	P14.01	−61.0 V	+61.0 V	differential
ASY02A	3	P15.14	0.0 V	+61.0 V	differential
ASY03A	3	P15.15	0.0 V	+61.0 V	differential
ASY10A	1	P14.12	−1.5 V	+1.5 V	differential
ASY11A	1	P14.13	−1.5 V	+1.5 V	differential
ASY12A	2	P15.06	0.0 V	+1.5 V	differential
ASY13A	2	P15.07	0.0 V	+1.5 V	differential
ASY00B	3	P15.08	0.0 V	+3.0 V	single-ended
ASY01B	3	P15.09	0.0 V	+3.0 V	single-ended
ASY02B	0	P14.06	0.0 V	+3.0 V	single-ended
ASY03B	0	P14.07	0.0 V	+3.0 V	single-ended
ASY10B	2	P15.04	0.0 V	+3.0 V	single-ended
ASY11B	2	P15.05	0.0 V	+3.0 V	single-ended
ASY12B	1	P14.14	0.0 V	+3.0 V	single-ended
ASY13B	1	P14.15	0.0 V	+3.0 V	single-ended
ASC00	0	P14.04	0.0 V	+3.0 V	single-ended
ASC01	0	P14.05	0.0 V	+3.0 V	single-ended
ASC10	3	P15.12	0.0 V	+3.0 V	single-ended
ASC11	3	P15.13	0.0 V	+3.0 V	single-ended

Appendix C

List of Publications

The work presented in this thesis has resulted in the following journal and conference publications. These papers are subjected to copyright by the particular journal or conference organizer. The journal publication is an extended version of a conference publication (J1/C1).

Journal Publication

J1 **R. Sleik**, M. Glavanovics, S. Einspieler, A. Muetze, and K. Krischan, "Modular Test System Architecture for Device, Circuit and System Level Reliability Testing and Condition Monitoring," *IEEE Transactions on Industry Applications*, vol. 53, pp. 5698–5708, Nov. 2017, ISSN: 0093-9994
DOI: 10.1109/TIA.2017.2724501

Conference Publications

C1 **R. Sleik**, M. Glavanovics, S. Einspieler, A. Muetze, and K. Krischan, "Modular Test System Architecture for Device, Circuit and System Level Reliability Testing," *Proceedings of the 31st annual IEEE Applied Power Electronics Conference and Exposition (APEC 2016)*, IEEE, Apr. 2016, pp. 759-765
DOI: 10.1109/APEC.2016.7467957

C1 **R. Sleik**, M. Glavanovics, Y. Nikitin, M. Di Bernardo, A. Muetze, and K. Krischan, "Performance Enhancement of a Modular Test System for Power Semiconductors for HTOL Testing by Use of an Embedded System," *Proceedings of EPE'17 ECCE Europe*, IEEE, Sep. 2017
DOI: 10.23919/EPE17ECCEEurope.2017.8098933