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Low Power Delta-Sigma Modulator for Smart Temperature Sensors in a 40nm CMOS Technology

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Affidavit

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Abstract

Advanced CMOS processes in deep sub-micron technologies are faced with increasing temperatures due to the growing component densities, which makes on-chip thermal monitoring unavoidable for today's integrated circuits. Smart temperature sensors are therefore used to prevent malfunctions or self-destruction of the chip. To detect temperature hotspots appearing on a chip, a supervision of the whole die by embedding several of these smart temperature sensors is necessary. This puts strict constraints on these devices.

This master's thesis addresses the question of a power and area efficient implementation of the analog-to-digital converter of such smart temperature sensors for the use in battery-less RFID products. A survey of converters which are worthy of consideration is given in this thesis. The design process of the most convenient converter from system-level considerations up to a transistor-level implementation in a $40nm$, triple well CMOS process with high threshold devices to reduce leakage currents is shown.

Schematic-level characterization of the implemented second-order delta-sigma modulator shows a peak SNDR of $86.9dB$ for a $1kHz$ bandwidth, while consuming $2.98\mu W$ from a $1.3V$ supply. The modulator operates with a single on-chip reference voltage. In the temperature range of $-40°C$ to $+125°C$ the ENOB of 14.1-bits provides a temperature resolution of $10mK$. A FOM of $0.082\frac{pJ}{conv}$, achieved in simulation, makes the delta-sigma modulator to one of the most efficient among published implementations. The modulator is therefore perfectly convenient for the application in smart temperature sensors.

Kurzfassung

Fortschrittliche CMOS Prozesse in Deep Sub-Mikrometer Technologien sind aufgrund wachsender Bauteildichten steigenden Temperaturen ausgesetzt. Daher ist eine on-chip Temperaturüberwachung mittels smarter Temperatursensoren zur Vermeidung von Ausfällen oder der Selbstzerstörung des Chips für moderne integrierte Schaltungen unabdingbar. Um auftretende Temperaturhotspots zu erkennen, ist eine Überwachung des gesamten Chips durch die Platzierung von mehreren smarten Temperatursensoren nötig. Dies bringt strenge Anforderungen an diese Schaltungsblöcke mit sich.

Diese Masterarbeit behandelt die Frage nach einer leistungs- und flächeneffizienten Implementierung des Analog-zu-Digital Umsetzers solcher smarten Temperatursensoren, um diese in batterielosen RFID Systemen verwenden zu können. Ein Überblick über die dafür in Frage kommenden Konverter wird in dieser Arbeit gegeben. Danach wird jener Umsetzer ausgewählt, der sich für die Anforderungen der vorliegenden Masterarbeit am besten eignet. Der Design-Prozess des ausgewählten Konverters von System-Level Überlegungen bis zu einer Transistor-Level Implementierung in einem $40nm$, drei Wannen CMOS Prozess mit Bauteilen mit hoher Schwellspannung zur Vermeidung von Leckströmen, wird gezeigt.

Die Charakterisierung des implementierten Delta-Sigma Modulators zweiter Ordnung auf Schaltungsebene zeigt einen maximalen SNDR von $86.9dB$ bei einer Bandbreite von $1kHz$, wobei ein Leistungsverbrauch von $2.98\mu W$ an einer Versorgungsspannung von $1.3V$ auftritt. Der Modulator wird mit einer einzigen on-chip Referenzspannung betrieben. Die ENOB von 14.1-Bits ermöglicht im Temperaturbereich von $-40°C$ bis $+125°C$ eine Temperaturauflösung von $10mK$. Eine in der Simulation erzielte FOM von $0.082\frac{pJ}{conv}$ macht den Delta-Sigma Modulator zu einem der effizientesten unter den publizierten Implementierungen. Der Modulator ist daher für die Anwendung in smarten Temperatursensoren optimal geeignet.

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List of Abbreviations

Abbreviation	Explanation
ADC	Analog-to-digital converter
BJT	Bipolar junction transistor
CIFB	Cascade of integrators with distributed feedback
CIFF	Cascade of integrators with distributed feedforward
CMOS	Complementary metal-oxide-semiconductor
CTAT	Complementary to absolute temperature
DAC	Digital-to-analog converter
DFT	Discrete Fourier transform
EDA	Electronic design automation
ENOB	Effective number of bits
FOM	Figure-of-merit
IC	Integrated circuit
MOSFET	Metal-oxide-semiconductor field-effect transistor
NTF	Noise transfer function
OSR	Oversampling ratio
OTA	Operational transconductance amplifier
PDF	Probability density function
PM	Phase margin
PSD	Power spectral density
PSRR	Power supply rejection ratio
PVT	Process-voltage-temperature

Abbreviation	Explanation
RFID	Radio-frequency identification
SAR	Successive-approximation-register
SFR	Special function register
SNDR	Signal-to-noise and distortion ratio
SNR	Signal-to-noise ratio
SQNR	Signal-to-quantization-noise ratio
SR	Slew rate
STF	Signal transfer function
TDC	Time-to-digital converter
UGF	Unity-gain-frequency
VLSI	Very-large-scale integration

Chapter 1

Introduction

In this introductory chapter, the need for on-chip temperature measurements will be discussed. The concept of a smart temperature sensor used for thermal monitoring will be described. Furthermore, the given project specifications will be presented and an overview of recently published implementations will be given.

1.1 Why On-Chip Temperature Measurements?

Constantly ongoing technology scaling leads to increasing component densities in today's very-large-scale integration (VLSI) systems. Following Moore's law, which indicates that the number of transistors in integrated circuits doubles approximately every two years, leads to upcoming problems about which were not considered in the past. One of those problems is the rising temperature due to the increased power density, which makes on-chip thermal monitoring unavoidable. Integrated smart temperature sensors consisting of a temperature sensor and an analog-to-digital converter (ADC) are therefore used, to prevent malfunctions or self-destruction of the chip due to overheating, by sending related information to the power and thermal management. This information can then be exploited to regulate the temperature on the die by a temporary throttling of the performance i.e. in reduction of the clock frequency of the chip [1].

To provide a measure of the absolute temperature as well as temperature gradients on the chip, several of those smart sensors need to be placed on the die [2], which puts strong constraints to these thermal monitoring circuits. The sensors need to be very compact as well as power efficient, to do not waste unnecessary huge areas and to do not consume excessive high currents. Furthermore, the sensing speed must be high enough to detect occurring temperature gradients. Lastly, the resolution and accuracy of the temperature measurement must be appropriate to grantee optimal performance.

1.1.1 Sensing Mechanism

Several sensing mechanisms are used in recently published papers, including mechanisms based on temperature dependence of metal-oxide-semiconductor field-effect transistor (MOSFET) leakage currents, complementary metal-oxide-semiconductor (CMOS) inverter prop-

agation delays and thermal diffusivity of silicon [3]. However, with respect to reliability and accuracy, these mechanisms are still inferior to the bipolar junction transistor (BJT) based sensors [4]. For this thesis, the complementary to absolute temperature (CTAT) voltage of a bipolar based bandgap reference was used. Since the focus of this thesis lies in the processing of the sensor signal, the sensing mechanisms will not be discussed in more detail.

1.1.2 Processing of the Sensor Signal

To process the analog output signal of the sensor in the digital circuitry of the chip, a conversion of the signal is required. The focus of this master's thesis lies on a power and area efficient implementation of those ADCs. In the remaining sections of this chapter, an overview of recently published implementations of such converters in smart temperature sensors will be given. Advantages and disadvantages of the used types will be discussed to find the most convenient ADC for the implementation of this thesis. Since the ADC to be implemented will be used for smart temperature sensors in future NXP Semiconductors[1] products, an overview of project related specifications will be given. Chapter 2 provides theoretical details about the chosen converter type, which are necessary to understand the topics discussed in later chapters of this thesis. Chapter 3 to 6 deal with the implementation process of the ADC. In the last chapter, a performance characterization as well as a comparison with state-of-the-art implementations will be done.

1.2 Recently Published Implementations

There were several publications of smart temperature sensors done in the last years. This section gives a survey of some of those implementations. Particular attention is paid to a power and area efficient implementation of the sensor signal processing ADC, since the design of this is the main task of this thesis. Properties of the chosen ADC types will be discussed and the most advantageous converter type for this thesis will be determined.

A literature study about low power and low area smart temperature sensors showed that there are several different converter architectures commonly used. As a sensing mechanism, most of the available publications use the temperature dependency of bipolar devices as a measure for the temperature. To process the temperature sensor signal, different methods are used to get a digital representation of the analog signal. An all-digital variant using a time-to-digital converter (TDC), which is based on temperature dependent charging of a capacitor followed by a comparator and a counter, was used in [5]. Such implementations of the ADC are extremely simple, but show lower accuracy compared to voltage domain ADCs and are therefore not used that often [6]. For the implementation of voltage domain ADCs, the most common choices are successive-approximation-register (SAR) ADCs and delta-sigma ADCs. Implementations of the former were found in [7] and [8]. Near-Nyquist ADCs like the SAR-ADC are known as the most power efficient implementations. But the accuracy of SAR ADCs is strongly dependent on the matching accuracy between the used components. Thus, higher resolutions lead to larger devices and therefore increased

[1] `https://www.nxp.com`

area and power consumption. If the application of the ADC in smart temperature sensor is considered, the total power consumption of SAR based architectures may not be smaller compared to implementations using oversampled ADCs [9]. Therefore, the most commonly used converter architecture for resolutions in the range of 10-bits and higher is the delta-sigma ADC. Published implementations of smart temperature sensors using this type of ADC were found in [10–12]. This oversampled ADC can achieve high resolutions, without the requirement of exactly matched components [13]. It trades accuracy with speed, which is convenient for monitoring temperature changes on a chip. Thus, this type of ADC seems to be the most advantageous type for the implementation of the sensor signal processing unit and was therefore chosen as converter for this thesis. A delta-sigma ADC consists of an analog delta-sigma modulator followed by a digital post-processing unit. Additional information about delta-sigma ADCs will be provided in chapter 2.

In the following, an overview of published implementations of power efficient delta-sigma modulators will be given. The implementations will be compared against each other with a common measure called figure-of-merit (FOM). As will be discussed in the next section, the ADC to be designed should provide a resolution of 10-bits and an input bandwidth of $1kHz$. Thus, publications with similar specifications, which are not necessarily designed for smart temperature sensors, were chosen for the comparison. Table 1.1 lists published state-of-the-art delta-sigma modulators. The FOM of those implementations was calculated with the commonly used formula

$$\text{FOM} = \frac{P}{2^{\frac{\text{SNDR}-1.76dB}{6.02dB}} \cdot 2 \cdot BW} \qquad \left[\frac{pJ}{conv}\right], \tag{1.1}$$

where P is the total power consumption of the modulator in Watts, SNDR is the signal-to-noise and distortion ratio of the modulator output signal and BW the input bandwidth in Hz. A low FOM in this case indicates an efficient implementation of the delta-sigma modulator. Additional information about the used oversampling ratio (OSR), the order of the modulator, details if either a single-ended, a fully-differential or a pseudo-differential implementation of the modulator was used and information about the used process in terms of minimum channel length L are also provided in this table. At this point of time, the information regarding the OSR and the order of the modulator are just for completeness, theoretical background will be given in chapter 2.

Ref.	peak SNDR dB	BW kHz	Order 1	OSR 1	Impl. -	L nm	P μW	FOM $\frac{pJ}{conv}$
[14]	80.5	1	5	16	FD	350	9	0.52
[15]	76	0.5	2	250	FD	65	2.1	0.407
[16]	68	0.2	2	200	FD	180	1.3	1.583
[17](1)	63	8	2	125	SE	350	6.72	0.364
[18]	61	10	3	70	PD	130	7.5	0.409

(1) Clock generator excluded SE ... Single-ended FD ... Fully-differential PD ... Pseudo-differential

Table 1.1: Comparison of state-of-the-art delta-sigma modulators.

1.3 Project Specifications

The smart temperature sensor will be used in future NXP Semiconductors products, where it will replace currently used blocks for on-chip temperature measurements. Furthermore, the ADC associated with the smart temperature sensor should provide additional testing possibilities on the chip. This section lists the most important design constraints as well as the desired modes of operation of the ADC. The system integration of the delta-sigma ADC will be explained. Available blocks which will be interconnected with the converter will be mentioned. The conclusion of this section will be the derivation of the specifications for the delta-sigma modulator.

1.3.1 Design Constraints

There are several design constraints which need to be fulfilled that the developed converter can be used in a future product. Since the ADC to be implemented will be used in radio-frequency identification (RFID) products and thus powered by the field devices, the current consumption is severely limited. The total current consumption of the delta-sigma modulator is therefore specified to a maximum value of $2.2\mu A$, which leads to a maximum power consumption of $2.86\mu W$ at a $1.3V$ supply. Furthermore, since RFID products are low-cost products, the area provided for the ADC is limited to $0.008mm^2$. To achieve appropriate accuracy in all modes of operation, the desired effective resolution of the ADC is specified to 10-bits. Comparing these constraints with the specifications of the published delta-sigma modulator designs in Tab. 1.1, it can be concluded that the desired resolution should be achievable with this type of converter. The main constraints for the design will therefore be the low power and area consumption.

1.3.2 Modes of Operation

There are two main modes in which the ADC will be operated. These modes are called *tempsens* and *testmode*. The following subsections will provide information about the desired behavior in these modes.

Mode *tempsens*

The default mode is called *tempsens*. In this mode the converter operates as a part of a smart temperature sensor, where a CTAT voltage, provided by the existing bandgap reference circuit of the chip, is processed. Measurements of this voltage in a temperature range of $-40°C$ to $+125°C$ with the desired resolution of 10-bits leads to a resolution in temperature of approximately $0.2°C$. The CTAT voltage to be processed is in a range of $400mV$ to $800mV$ for the mentioned temperature range.

Mode *testmode*

The second mode of operation is called *testmode* and will be used at wafer test. In this mode, the ADC is disconnected from the temperature sensor. The goal is to provide volt-

age measurements of either internal or external signals. The measured voltages can then be used for post-processing, e.g. for trimming.

Actually, there is a third desired mode of operation which is called *power-down*. In this mode, the ADC should be switched off and should only consume leakage currents.

1.3.3 System Integration

As mentioned, the delta-sigma ADC should be used in future products. This section deals with the integration of the converter to existing circuitry. Fig. 1.1 gives an overview of the system integration of the delta-sigma ADC in NXP Semiconductors products. An explanation of this picture will be given in this section.

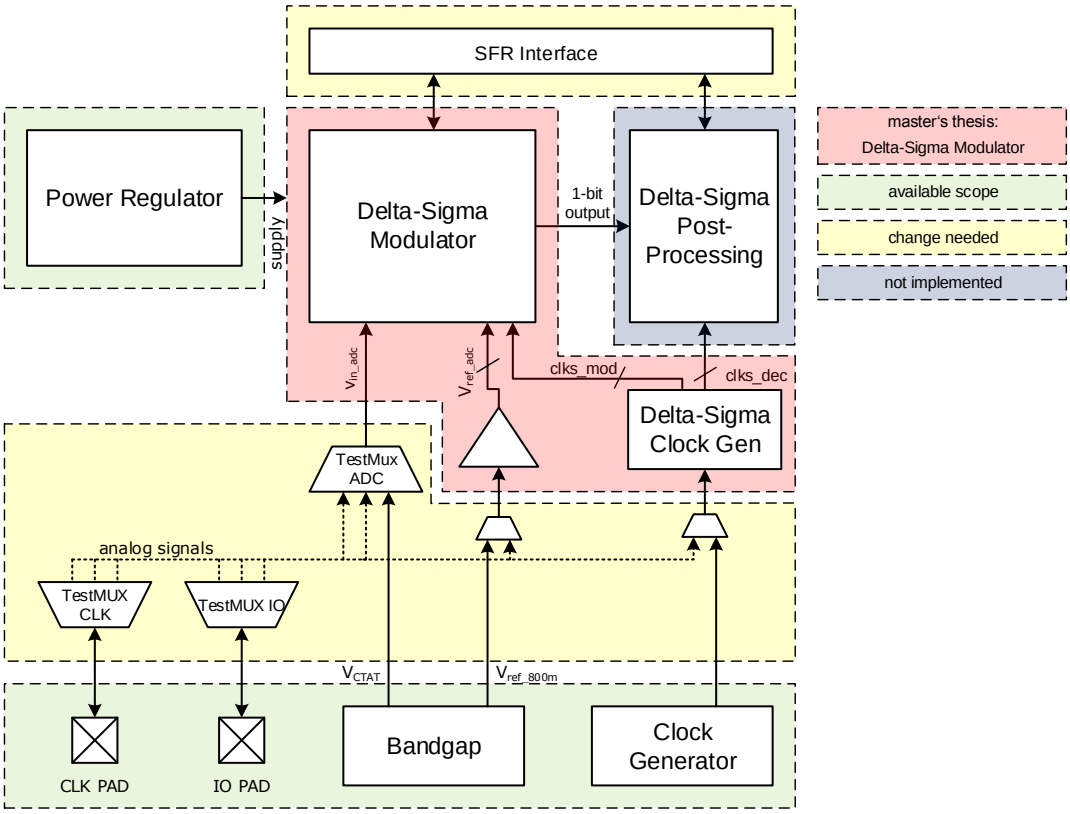

Figure 1.1: System integration of the delta-sigma ADC. The implementation of the blocks within the red box is a task of this master's thesis. The blocks within the green and yellow boxes are available, whereas application-oriented changes might be necessary in the yellow area. The grey box indicates tasks for future works.

As explained in section 1.3.2, depending on the mode of operation, the input signal to be processed with the delta-sigma ADC is either the CTAT voltage V_{CTAT} of the bandgap reference or a certain internal or external signal. Thus, a multiplexer is needed to assign the desired input signal to the ADC regarding the chosen operating mode. The output of

the ADC will be processed in the Special Function Register (SFR). For the operation of the delta-sigma modulator, at least one reference voltage V_{ref_adc} is needed. The already implemented bandgap circuit provides a process-voltage-temperature (PVT) stable, trimmed reference voltage of $V_{ref\_800m} = 800mV$, which can be used. To utilize this voltage and to generate additional required reference voltages, a voltage buffer must be interposed. Since it is also desired to operate the delta-sigma ADC with an external reference voltage, again a multiplexer is needed. As a clock source the available on-chip clock generator, which provides a PVT stable, trimmed base clock with a frequency of $96MHz$, can be used. Furthermore, reduced clock rates with division factors of 2, 4, 8, 16, 32, 64, 128 and 192 referred to the base clock are directly available. To generate the required clock signals for the delta-sigma ADC, a clock generator will be needed. For the operation of the converter with an external clock signal, again a multiplexer is added. The delta-sigma ADC will be powered with voltages provided by the existing power regulator block. If necessary, a reference current of $50nA$ and multiple of this value can be provided by the bandgap circuit.

The goal for this master's thesis is the implementation of the delta-sigma modulator and the generation of all its required reference voltages as well as clock signals on schematic-level. The post-processing of the modulator output signal as well as the implementation of the required multiplexer for the different modes of operations are not part of this thesis, and won't be discussed in detail, therefore.

The mentioned power regulator of the chip provides three supply voltages. Since the product is a mixed-signal integrated circuit (IC), a digital as well as an analog supply is available. The digital supply V_{ddd} provides a voltage between $0.99V$ and $1.26V$ and the analog supply V_{dda} provides a voltage between $1.2V$ and $1.47V$. Additionally, the chip contains a non-volatile memory, therefore a third supply called V_{ddee} is available which provides a voltage between $1.5V$ and $2V$. Since the delta-sigma modulator to be designed is a mainly analog block, the analog supply V_{dda} will be the most interesting of those three and will therefore be used. The nominal voltage of the analog supply is equal to $1.3V$. Nevertheless, the implemented ADC must operate properly in the complete specified voltage range of the analog supply.

The used technology for the implementation of the delta-sigma ADC is a $40nm$, triple-well CMOS process from GlobalFoundries[2]. For further information about the used process the author refers to the Technology Design Manual provided by GlobalFoundries.

1.3.4 Determined Block-Level Specifications

With the given constraints and the different modes of operation, specifications for the modulator can be created. The input signal bandwidth of the ADC was determined to $1kHz$, which should be appropriate to follow appearing temperature changes. The input voltage range was determined to $0 - 800mV$, which is an appropriate range to directly process the provided CTAT voltage. Nevertheless, to achieve maximum resolution in the temperature measurement, a scaling of the CTAT voltage is necessary. To measure voltages outside of this range, which might be useful in the *testmode*, again a preprocessing of these voltages is necessary. The desired temperature range where all the given constraints

[2] `https://www.globalfoundries.com/`

must be fulfilled is predetermined to a junction temperature range of $-40°C$ to $+125°C$. Table 1.2 summarizes the mentioned constraints and specifications. Additional information is also provided in this table. These specifications will guide through the design and verification process of the delta-sigma modulator.

Parameter	Symbol	Value	Unit
Input voltage range	V_{in_adc}	$0 - 800$	mV
Input signal bandwidth	f_B	1	kHz
Current consumption	I	< 2.2	μA
Area	A	< 0.008	mm^2
Effective resolution	ENOB	10	bits
Supply voltage	V_{dda}	1.2 ... 1.47	V
Temperature range	T	-40 ... $+125$	$°C$
Technology	-	CMOS 40nm	-

Table 1.2: Specifications for the delta-sigma modulator.

Chapter 2

Delta-Sigma ADC Based Processing

Investigations done in the previous chapter showed that a delta-sigma ADC based processing tends to be the best choice for the desired application. This chapter provides the required information regarding this type of ADC to understand topics discussed in later chapters.

2.1 Basics of Delta-Sigma ADCs

The delta-sigma ADC consists of two main building blocks, an analog delta-sigma modulator and a digital post-processing unit for the modulator output signal. It thereby uses two key techniques called oversampling and noise-shaping. This section shows how these techniques are applied to an analog input signal to achieve a high resolution digital representation of the input signal.

2.1.1 Block Diagram of a Delta-Sigma ADC

As mentioned, a delta-sigma ADC consists of two main elements. The first part is the delta-sigma modulator, which generates an oversampled, quantization noise-shaped, but low resolution digital representation of an analog input signal. The modulator output signal is afterwards digitally processed, where the shaped quantization noise is removed, the resolution of the signal is increased and the signal is downsampled. This part of the ADC is often referred as the decimator. Fig. 2.1 shows the block diagram of a delta-sigma ADC, where the purpose of the shown elements, as defined in [19], are:

- *Modulator:* The analog input signal $x_c(t)$ is sampled and quantized at a rate much higher than the Nyquist rate, leading to the signal $y_m[n]$. Additionally, after a conversion to the analog domain, this output signal is feed back to the input of the modulator, which provides in case of a suitable choice of the loop filter transfer function $H(z)$ the noise-shaping property of the delta-sigma modulator.

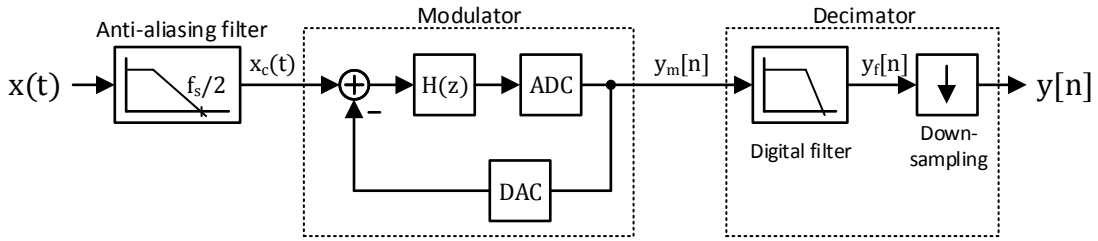

Figure 2.1: Block diagram of a delta-sigma ADC. The delta-sigma ADC consists of a delta-sigma modulator followed by a decimator. To avoid aliasing due to the sampling process performed in the modulator, an anti-aliasing filter is required to bandlimit the input signal. (Own compilation, adapted from [19]).

- *Decimator:* Signal components out of the band of interest, which includes the shaped quantization noise, are removed by a digital filter and the resolution of the signal is thereby increased. Downsampling is performed to reduce the output signal rate back to Nyquist rage.

Additionally, an anti-aliasing filter is usually placed at the input of the modulator, which bandlimits the input signal to avoid aliasing due to the sampling process. Since sampling at much higher rate than the Nyquist rate is performed, the requirements for this filter are quite relaxed and it can therefore be implemented using a low-order analog filter [20].

2.1.2 Oversampling and Noise Shaping

Data Converters are usually separated into two categories depending on the rate of operation compared to the input signal frequency range. The first type of ADCs samples the input signal close to the Nyquist rate. For these type of converters, the accuracy is determined by the matching accuracy of analog components [21]. The other type of converters uses sampling frequencies which are much higher than the signal bandwidth and are therefore known as oversampling converters. These oversampling converters can achieve a much higher resolution than Nyquist rate converters, since they do not rely on precisely matched analog components [22]. The OSR, which is defined as

$$\mathrm{OSR} = \frac{f_s}{f_N} = \frac{f_s}{2f_B}, \tag{2.1}$$

where f_s is the sampling frequency, f_N the Nyquist frequency and f_B the input signal bandwidth, is usually in the range of 8 to 256 [20].

To analyze the impact of oversampling and noise shaping, first the properties of quantization noise need to be understood. Due to quantization of the analog signal to a certain number of digital values, a non-restorable error may occur. With some assumptions, this quantization error e can be treated as quantization noise, uniformly distributed between $-\mathrm{LSB}/2$ and $+\mathrm{LSB}/2$ with a white power spectrum and a total power of

$$\sigma_e^2 = \int_{-\infty}^{\infty} P_e(e)\ e^2\ de = \frac{1}{\mathrm{LSB}} \int_{-\mathrm{LSB}/2}^{\mathrm{LSB}/2} e^2\ de = \frac{\mathrm{LSB}^2}{12}, \tag{2.2}$$

where $P_e(e)$ is the probability density function (PDF) of the quantization error e and LSB is the size of a quantization step [23]. Since the quantization noise power σ_e^2 is uniformly distributed in the frequency range $[-f_s/2, f_s/2]$, the one-sided power spectral density (PSD) of the quantization noise equals

$$S_E(f) = \frac{\sigma_e^2}{\frac{f_s}{2}} = \frac{\text{LSB}^2}{6f_s}. \tag{2.3}$$

For Nyquist rate converters where the sampling frequency f_s equals the Nyquist frequency f_N, the power of the quantization noise in the signal band f_B equals

$$P_Q = \int_0^{f_B} S_E(f)\ df = \int_0^{f_s/2} S_E(f)\ df = \frac{\text{LSB}^2}{12}, \tag{2.4}$$

hence, the whole quantization noise power is within in the signal band.

To determine the performance of data converters, the measures of signal-to-noise ratio (SNR) and signal-to-noise and distortion ratio (SNDR) are commonly used. For a converter, the SNR is calculated using

$$\text{SNR} = 10\ log\left(\frac{P_S}{P_N}\right), \tag{2.5}$$

where P_S is the signal power and P_N is the total noise power, whereas the SNDR is calculated using

$$\text{SNDR} = 10\ log\left(\frac{P_S}{P_N + P_D}\right), \tag{2.6}$$

where P_D is the total power of all distortions, including harmonics. In many publications, there is no strict distinction between the SNR and the SNDR since they refer both to the latter. In this thesis there is a distinction between those two. The measure of SNR will be used in the theoretical part of this thesis, where no distortions are considered. The term SNDR will be used to characterize circuit level simulation results.

For an ideal converter, the only source of error arises from the quantization of the signal, thus the total noise power P_N equals the quantization noise power P_Q. Mathematical derivations which will be done in this thesis refer to ideal converters, leading to the measure of signal-to-quantization-noise ratio (SQNR). The SQNR of a converter is defined as

$$\text{SQNR} = 10\ log\left(\frac{P_S}{P_Q}\right), \tag{2.7}$$

where P_S is the signal power and P_Q is the quantization noise power. Assuming a sinusoidal signal between 0 and V_{ref}, where $V_{ref} = \text{LSB} \cdot 2^N$ and N is the resolution of the ideal converter in bits, the very common relationship between the SQNR and the resolution N of a Nyquist rate converter,

$$\begin{aligned}
\text{SQNR} &= 10\ log\left(\frac{P_S}{P_Q}\right) \\
&= 10\ log\left(\frac{\left(\frac{V_{ref}/2}{\sqrt{2}}\right)^2}{\frac{\text{LSB}^2}{12}}\right) \\
&= 10\ log\left(\frac{3}{2}\ 2^{2N}\right) \\
&= 6.02\ N + 1.76\ dB,
\end{aligned} \tag{2.8}$$

can be derived.

If the sampling frequency f_s is much higher than the Nyquist frequency, thus oversampling is used, the total in-band quantization noise power equals

$$P_Q = \int_0^{f_B} S_E(f)\ df = \frac{\mathrm{LSB}^2}{6f_s} f_B = \frac{\mathrm{LSB}^2}{12} \frac{1}{\mathrm{OSR}}. \tag{2.9}$$

Thus, the quantization noise power in the band of interest is inversely proportional to the used OSR. It is worth to mention that the total quantization noise power stays the same, it just gets spread over a wider frequency range. Using oversampling, equation (2.8) gets therefore modified to

$$\mathrm{SQNR} = 6.02\ N + 1.76\ dB + 10\ log\,(\mathrm{OSR}) \tag{2.10}$$

for an oversampled converter. Thus, every two times oversampling leads to an increase of approximately $3dB$ in SQNR. Oversampling converters are therefore useful, when speed can be exchanged with accuracy and are therefore a good solution to achieve a high resolution representation of relatively low frequency signals [13, 24].

Oversampling ADCs can be further classified into straight oversampling ADCs and noise-shaping ADCs. The further use just the improvement in SQNR due to oversampling as shown in equation (2.10). A well-known converter of this type is the delta-modulator. The delta-sigma modulator on the other hand additionally uses the noise-shaping property to further increase the SQNR in the band of interest. Due to the placement of the loop filter $H(z)$ and the quantizer as shown in Fig. 2.1, two different transfer functions for the input signal and the quantization noise can be achieved. As will be discussed in section 2.2, the input signal will not be changed due to the modulation process, whereas the quantization noise gets attenuated in the band of interest and shaped to higher frequencies, thereby increasing the in-band SQNR.

2.1.3 Signal Processing in Delta-Sigma ADCs

To visualize the points discussed in the previous sections, the signal processing performed by the individual elements of the block diagram in Fig. 2.1 will be investigated in this section. Fig. 2.2 shows the processing steps of an analog input signal in the time and frequency domain. To better understand the impact of sampling to the spectrum, the sampling and quantization process performed by the modulator are split up in two separated blocks.

The anti-aliasing filter at the input of the delta-sigma ADC eliminates frequency components of the input signal $x(t)$, which would lead to aliasing due to the sampling process. The delta-sigma modulator, which performs the sampling and quantization process of the bandlimited signal $x_c(t)$, provides a low resolution (in this case 1-bit) digital output signal $y_m[n]$ with a bit-rate equal to the sampling frequency f_s. Due to sampling process, replicas of the spectrum appear in the frequency domain. The noise-shaping property of the delta-sigma modulator shapes the quantization noise, which occurs due to the quantization of the signal, to frequencies close to $f_s/2$, thereby increasing the in-band SNR.

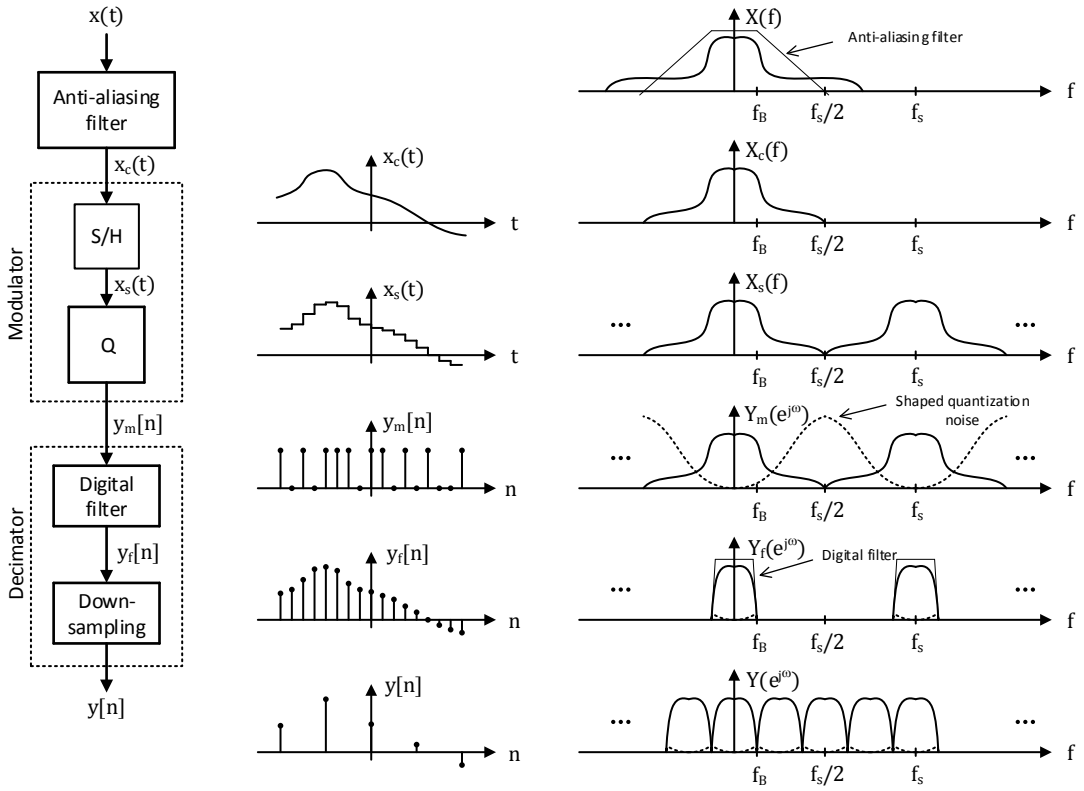

Figure 2.2: Signals and spectra in delta-sigma ADCs. Visualization of the signal processing in delta-sigma ADCs. For simplicity, the sampling and quantization process performed by the 1-bit modulator are split up. (Own compilation, adapted from [19]).

The digital filter, which generates the local average of samples, increases the resolution of the modulator output stream and cuts off out-of-band frequency components. The final decimation stage, reduces the rate of the signal $y_f[n]$ back to the Nyquist rate without introducing information loss, since only redundant parts of information are removed [19]. A high resolution digital representation $y[n]$ of the analog input signal is achieved.

2.2 The Delta-Sigma Modulator

With the knowledge of the basic operating principle of delta-sigma ADCs, the delta-sigma modulator can be discussed in more detail. As mentioned, the delta-sigma modulator provides different transfer functions for the input signal and the occurring quantization error to achieve a high SNR in the band of interest. Since the quantization error can be treated as additive white noise, the block diagram of the modulator in Fig. 2.1 can be simplified to the linear model shown in Fig. 2.3 [21], where $e[n]$ indicates the appearing quantization error. The modulator output $y_m[n]$ can therefore be represented by the z-domain equation

$$Y_m(z) = \frac{H(z)}{1 + H(z)} X_c(z) + \frac{1}{1 + H(z)} E(z), \tag{2.11}$$

where $X_c(z)$ and $Y_m(z)$ are the z-transform of the input and output signal of the modulator, $E(z)$ is the z-transform of the quantization error $e[n]$ and $H(z)$ is the discrete-time loop filter.

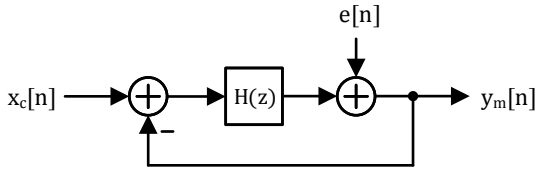

Figure 2.3: Linear model of the first-order delta-sigma modulator. The quantization error is treated as additive white noise $e[n]$.

Thus, two transfer functions are achieved, the signal transfer function

$$STF(z) = \frac{H(z)}{1 + H(z)} \tag{2.12}$$

and the noise transfer function

$$NTF(z) = \frac{1}{1 + H(z)}. \tag{2.13}$$

To achieve a suppression of the quantization noise for low frequencies, a

$$NTF(z) \to 0 \quad \text{for} \quad z \to 1 \tag{2.14}$$

is required, which indicates that the transfer function of the discrete-time filter must fulfill

$$H(z) \to \infty \quad \text{for} \quad z \to 1. \tag{2.15}$$

A discrete-time integrator with a transfer function

$$H(z) = \frac{1}{z - 1} \tag{2.16}$$

is the simplest block that implements such a noise transfer function [19]. Inserting this transfer function into equation (2.11) yields the modulator output in the z-domain to

$$Y_m(z) = z^{-1}X_c(z) + (1 - z^{-1})E(z). \tag{2.17}$$

Thus, the digital output of the modulator contains a delayed but else unchanged version of the input signal and a differentiated version of the quantization error and therefore suppresses the quantization noise in the band of interest [21].

To calculate the in-band quantization noise power, the PSD of the quantization noise, $S_Q(f)$, at the output of the modulator needs to be calculated. This can be done using the Wiener-Lee relation

$$S_Q(f) = |NTF(f)|^2 \; S_E(f), \tag{2.18}$$

where $S_E(f)$ is the PSD of the quantization noise without noise shaping derived in equation (2.3). The quantization noise transfer function NTF, which is in the z-domain $NTF(z) = 1 - z^{-1}$, equals, after replacing z by $e^{j2\pi\frac{f}{f_s}}$,

$$|NTF(f)| = 2 \ \sin\left(\frac{\pi f}{f_s}\right) \tag{2.19}$$

in the frequency domain [21]. Thus, the PSD of the quantization noise at the output of the modulator equals

$$S_Q(f) = 4 \ \sin\left(\frac{\pi f}{f_s}\right)^2 \cdot S_E(f). \tag{2.20}$$

Using the approximation of $\sin\left(\frac{\pi f}{f_s}\right) \approx \frac{\pi f}{f_s}$ [21], the in-band quantization noise power at the output of the delta-sigma modulator can be approximated to

$$P_Q = \int_0^{f_B} S_Q(f)df \approx \frac{\pi^2\sigma_e^2}{3 \ (\mathrm{OSR})^3}. \tag{2.21}$$

Thus, the in-band quantization noise power P_Q at the output of the first-order modulator is inversely proportional to the OSR to the power of three, thus every doubling of the OSR leads to an increase in SQNR of approximately $9dB$ and is therefore much higher than the increase of $3dB$ for oversampling converters only.

A further improvement can be achieved by increasing the order of the modulator by adding additional integrators to the loop as it is shown for a second-order modulator in Fig. 2.4. Doing again the steps as for the first-order modulator, the $NTF(z)$ can be found to $(1-z^{-1})^2$, in case a gain factor of 2 is added to the feedback path of the second integrator as shown in the figure. Solving equations (2.18)-(2.21) for this NTF leads to an in-band quantization noise power of

$$P_Q \approx \frac{\pi^4\sigma_e^2}{5 \ (\mathrm{OSR})^5} \tag{2.22}$$

for the second-order delta-sigma modulator, which indicates an increase in SQNR by approximately $15dB$ for every doubling of the OSR. Thus, the second-order modulator achieves the same performance as the first-order modulator with a lower sampling rate.

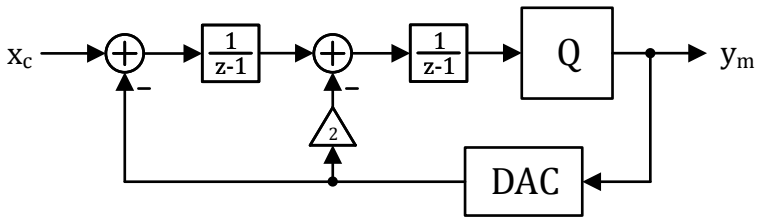

Figure 2.4: Block diagram of a second-order delta-sigma modulator. The gain block in the feedback loop provides a NTF of $(1 - z^{-1})^2$. (Own compilation, adapted from [25]).

A further increase of the order of the modulator would again give a reduction of the in-band quantization noise power. Thus, equation (2.22) can be generalized to

$$P_Q \approx \frac{\pi^{2L} \ \sigma_e^2}{(2L+1) \ (\mathrm{OSR})^{2L+1}} \tag{2.23}$$

for a L-th order delta-sigma modulator. The improvement in SQNR for every doubling of the sampling rate is equal to $(6L + 3)dB$ for a L-th order delta-sigma modulator.

Increasing the order of the modulator to achieve a better SNR will soon lead to stability problems, which can be avoided by using so called MASH structures [21]. These MASH structures will be discussed in section 3.3.

As explained in section 2.1, the delta-sigma ADC achieves its high resolution in the digital post-processing of the oversampled modulator output stream. In most of the cases, the resolution of the modulator output is as low as 1-bit. The big advantage of a 1-bit quantization is the inherent linearity of the digital-to-analog converter (DAC) needed in the feedback loop of the modulator, since it provides only two possible output values [23]. Therefore, the DAC does not require precise component matching as it is the case for multi-bit DACs [13]. One the other hand, multi-bit internal quantizer can achieve a higher SNR compared to 1-bit quantizer. The increase in SQNR is typically $6dB$ per additional bit [13]. Since the desired ADC resolution of 10-bits should be achievable with a single-bit quantization, the advantages outweigh, therefore a 1-bit modulator will be used in this thesis.

To conclude this section, it can be said that the delta-sigma modulator provides a low resolution but high SNR digital representation of an analog input signal. An improvement in SNR can be achieved by increasing the OSR or the order of the modulator.

2.3 Digital Post-Processing

To cut-off the shaped quantization noise and to reduce the rate of the oversampled output stream while increasing its resolution, digital post-processing is performed. Since the implementation of the decimator is not a task of the master's thesis, the theory behind it will be put in a nutshell.

There are several techniques available to implement the digital post-processing for delta-sigma ADCs. For this thesis, a very common approach, the so called multi-stage approach, will be discussed.

The digital post-processing, which is often noted as decimation filtering, consists of an initial lowpass filter followed by a downsampling unit as can be seen in the block diagram of a delta-sigma ADC in Fig. 2.1. Thus, it removes out-of-band quantization noise produced by the modulator and additionally resamples the output signal to a more convenient rate, e.g. to the Nyquist rate. Since a linear phase characteristic in the decimation filters for delta-sigma ADCs is desired, FIR filter implementations are widely used [21]. Since these filters should provide an abrupt cut-off, the number of required filter coefficients can therefore rise quite fast. Thus, decimation filter for delta-sigma ADCs are usually implemented in several stages, which reduces the total number of filter coefficients and hence, reduces the hardware complexity and power consumption [20].

The first stage of a decimation filter for delta-sigma ADCs, as can be seen in Fig. 2.5, is usually a $sinc^{L+1}$ filter, which consists of a cascade of $L+1$ averaging filters with transfer functions

$$T_{avg}(z) = \frac{1}{M} \sum_{i=0}^{M-1} z^{-i}, \tag{2.24}$$

where L is the order of the delta-sigma modulator and M the downsampling ratio performed by this stage. Usually the modulator output signal gets downsampled to a rate of $8f_B$ by this first stage [23]. Cascading these $L+1$ averaging filters and doing some mathematical rewritings as shown in [23], the total transfer function of the first stage can be derived to

$$T_{sinc}(z) = \frac{1}{M^{L+1}} \left(\frac{1 - z^{-M}}{1 - z^{-1}} \right)^{L+1}, \tag{2.25}$$

which gives a sinc frequency response of this filter. The reason for choosing a filter with an order of $L+1$ is to achieve a greater slope of attenuation provided by this low-pass filter compared to the rising quantization noise [23]. This keeps the total noise at the output of the ADC low.

The filters following the $T_{sinc}(z)$ filter act as a sharp anti-aliasing filter, which remove input signal frequency components greater than f_B and additionally downsample the signal to $2f_B$ [23]. If needed, these halfband filters are followed by a correction filter, which compensates the in-band attenuation caused by the $T_{sinc}(z)$ filter [20].

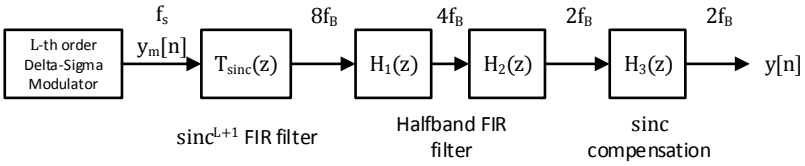

Figure 2.5: Multi-stage decimation filter for delta-sigma ADCs consisting of a sinc filter, halfband filters and a correction filter. (Own compilation, adapted from [23]).

Chapter 3

Design Considerations for the Delta-Sigma Modulator

The basic theory about delta-sigma modulators has been presented in the previous chapter, thus considerations about the implementation of the modulator can be made. This chapter gives details about the process to determine the most advantageous implementation of the modulator with respect to the given project specifications. The decision between a continuous-time and a discrete-time implementation will be explained. Furthermore, a convenient order of the modulator to fulfill the specifications will be determined. Additionally, different topologies of the modulator will be investigated with the help of high level simulations performed in MATLAB.

3.1 Continuous-Time vs. Discrete-Time Implementation

The first decision that must be made when doing the design of a delta-sigma modulator is the choice between a continuous-time and a discrete-time implementation. The loop filter of a continuous-time delta-sigma modulator is implemented with either RC- or g_m/C-integrators. The sampling of the signal takes place just before the quantizer. The loop filter of continuous-time implementations provides inherent anti-aliasing, therefore no additional anti-aliasing filter is required. To provide an analog feedback signal, a DAC is needed in the feedback path. These DACs can be implemented in either discrete-time or continuous-time circuits. Since there are many trade-off's in selecting the DAC architecture, the choice between them is quite critical [26].
For discrete-time implementations of delta-sigma modulators, the sampling of the input signal takes place before the loop filter. Thus, the loop filter is a discrete-time circuit implemented using switched-capacitor integrators. These switched-capacitor integrators provide a high accuracy, since the matching between the capacitors is usually quite accurate. Furthermore, the difference equations which describe the discrete-time modulator are independent of the clock frequency [21]. Since the loop filter operates in the discrete-time domain, the "DAC" of a single-bit discrete-time delta-sigma modulator is just a selector between two feedback levels and can therefore be implemented using logic gates which control switches of the integrators. Thus, no accurately matched components are required

in the DAC. Table 3.1 summarizes advantages and disadvantages of the two types as stated in [13, 21, 26, 27], which may be of interest for the given project specifications.

Continuous-time implementation	Discrete-time implementation
Consumes (slightly) less power	Good accuracy and good linearity
Can operate at higher clock frequencies	Transfer function scales with the sampling frequency
RC-time constants are inversely proportional to the sampling frequency	Less sensitive to timing variations
DAC needed $\rightarrow$ architecture choice critical	Anti-aliasing filter needed

Table 3.1: Advantages and disadvantages of continuous-time and discrete-time loop filter implementations in delta-sigma modulators.

Since the RC-time constants of continuous-time loop filters are inversely proportional to the sampling frequency, there is a trade-off between two important design constraints. A lower sampling rate, which would reduce the requirements and hence the power consumption of blocks like the integrator amplifier, would on the other hand lead to greater resistor and capacitor values and thus require a larger area. That also means, that an implemented continuous-time loop filter can only operate at a specified sampling frequency. As mentioned before, in discrete-time implementations the transfer function of the loop filter is independent of the sampling frequency. This opens a great possibility to reduce the power consumption by a reduction of the sampling frequency, if a lower resolution is appropriate. Furthermore, this increases the reusability of the implemented data converter. To conclude, the discrete-time approach provides the most advantageous trade-offs for the given project specifications, therefore this implementation type was chosen.

3.2 Order of the Modulator

The next design consideration is about the selection of the order of the modulator. The order of the modulator is equivalent to the number of integrators in the loop. As shown in section 2.2, increasing the order of the modulator leads to a lower quantization noise power P_Q in the band of interest and thus increases the SQNR of the modulator for a given OSR. But, increasing the order to achieve a higher SQNR will soon lead to stability issues, thus to further increase the SQNR the OSR needs to be increased. This section shows the procedure to find the most convenient compound of the order and the OSR of the modulator, to fulfill the two most important constraints of the low power and area consumption.

To approximately estimate the required order of the delta-sigma modulator to satisfy the given project specification regarding the resolution, Fig. 3.1 presented by Schreier and Temes in [21] was used, which shows empirically investigated SQNR limits that can be achieved with a 1-bit modulator of order L.

Since quantization noise should only take up a part of the total noise budget, a SQNR design margin of approximately $20dB$ to the desired SNDR is proposed by the publisher of the figure. According to equation (2.8), in case of an ideal converter, a SQNR of $61.96dB$ is required to achieve the desired resolution of 10-bits. Adding $20dB$ of margin

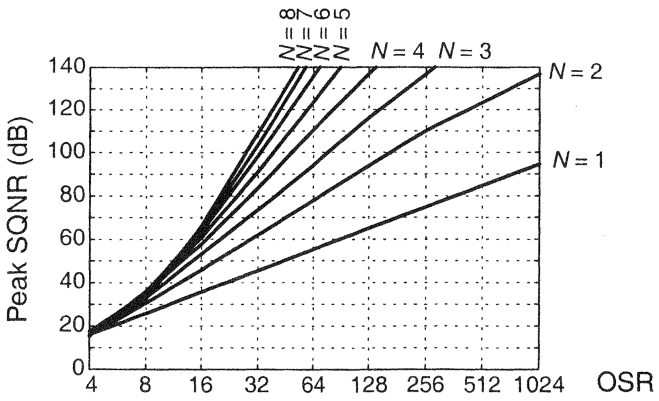

Figure 3.1: Empirical SQNR limits for 1-bit delta-sigma modulators of order N [21]. The variable N of this figure corresponds to the used variable L in the text.

to this SQNR, either a first-order modulator with an OSR of roughly 500, a second-order modulator with an OSR of 100 or a third-order modulator with an OSR of 50 is needed. Higher order modulators would require even lower OSRs, but stability considerations are much more critical for those modulators [21]. Paper studies showed, that due to the area requirement, either first- or second-order modulators are most likely used for similar specifications [2, 15–17, 28–32], therefore these modulator orders were investigated in more detail.

The first-order modulator, consisting of an integrator, a quantizer and a DAC as shown in the block diagram of Fig. 2.1, tends to be the most area efficient implementation, since just one integrator is used. But it requires a much higher OSR to achieve a comparable SQNR as the second-order modulator. The higher sampling rate, which would in the case of a first-order modulator be approximately $1MHz$, leads to increased circuit block requirements, especially for the integrator amplifier, and thus a higher power consumption compared to blocks of the second-order modulator. Furthermore, it is susceptible to finite integrator amplifier gain, which leads to dead bands and degraded noise shaping [13]. The latter reduces the achievable SQNR, since the leaky amplifier does not implement its ideal desired transfer function. Dead bands lead to an unchanged output of the modulator for small variations of the modulator input. For the first-order modulator, this dead bands can be as big as $\pm\frac{1}{2A} \cdot V_{in_{FS}}$ [21], where A is the dc-gain of the integrator amplifier and $V_{in_{FS}}$ the full-scale input range, which leads to a reduced dynamic range of the data converter. Another drawback of the first-order modulator is the possible pattern noise generation for dc inputs. A static input can thereby lead to a periodic modulator output signal with a frequency that can be in the band of interest [19]. This signal can thus reduce the SNDR of the modulator. Investigations done by Gonzalez and Reiss in [33] showed that these periodic patterns appear in low order modulators, especially in the first-order modulator.

The second-order modulator with its z-domain block diagram shown in Fig. 2.4 overcomes disadvantages of the first-order modulator with more hardware by adding a second integrator to the loop. This leads to an increased area consumption. Compared to the first-order modulator, a much lower sampling rate can be used. This especially reduces the speed requirements of the amplifiers used in the integrators, but also reduces the requirements of other circuit blocks like the switches as will be shown in a later chapter. Furthermore, the

second-order modulator is much more robust to finite amplifier gain, since the open loop gain of the modulator is equal to A^2 [21], where A^2 is the total gain of both integrator amplifiers. Thus, the gain requirement of each amplifier is also reduced. Nevertheless, the impact on the total power consumption compared to the first-order modulator is difficult to determine at this point of time.

To get more insight in the selection of the most advantageous order of the modulator, MATLAB simulations were performed. A MATLAB toolbox called *Delta-Sigma Toolbox* provided by Schreier was used for that. This toolbox can be found on the MATLAB homepage[1]. For further information about the toolbox, the author refers to the documentation of the toolbox which can also be found on the mentioned homepage.

Investigations regarding the most advantageous order of the modulator were done for the first- and second-order modulator as they are shown in Fig. 2.1 and 2.4. For the first-order modulator an OSR of 500 and for the second-order modulator an OSR of 125 were chosen. The input bandwidth of the modulators was determined to $1kHz$, as it is specified for the converter to be implemented. To estimate the achievable performance of both modulator orders, the SQNR for changing input signal amplitude was simulated using the provided function $simulateSNR()$. Within this function, the amplitude of a sinusoidal input signal is swept between $-80dBFS$ and $0dBFS$, referred to the default input range of the *Delta-Sigma Toolbox*. The MATLAB simulation results for a first-order modulator with an OSR of 500 and a second-order modulator with an OSR of 125 are shown in Fig. 3.2. This figure shows the maximum achievable SQNR for the selected delta-sigma modulator topologies. As can be seen, both modulators with their chosen OSRs should be able to fulfill the SNDR specification, which is additionally plotted in black. Overall, the SQNRs of the second-order modulator are higher than that of the first-order modulator. Furthermore, the simulated SQNR values of second-order modulator are more regular for changing input signal amplitude. The overload level of both modulators seems to be $-1dB$ below the full-scale input range. Above this value, the achievable SQNR drops because of nonlinear effects due to quantizer overload [21, 34]. The achievable SQNR values of the first-order modulator are quite close to the desired SNDR values for small input signal amplitudes, thus the quantization noise already fills up the complete noise budget, which is not desired. Very small signal amplitudes are even not visible in the output spectrum of the first-order modulator. Thus, the dynamic range of the first-order modulator is severely limited. Simulations showed that an increase of the OSR to 1000 for the first-order modulator would improve the performance with the drawback of even higher circuit block requirements.

At this point of time, the second-order modulator seems to be the better choice for the implementation, since it shows superior performance. Nevertheless, no estimations about differences in power and area consumption were made so far. Since the very low specified current consumption might not be achievable with the second-order modulator, the final selection of the order was shifted to a later point in the design process, where block requirements were derived and first behavioral simulations were performed. All steps described in the following chapters were done for both discussed orders. Finally, the second-order modulator was chosen for the transistor-level implementation, since behavioral simulations showed also a better performance for this order, while the total current consumption of both was estimated to be in a similar range. The following chapters just deal with the

[1] `http://de.mathworks.com/matlabcentral/fileexchange/19-delta-sigma-toolbox`

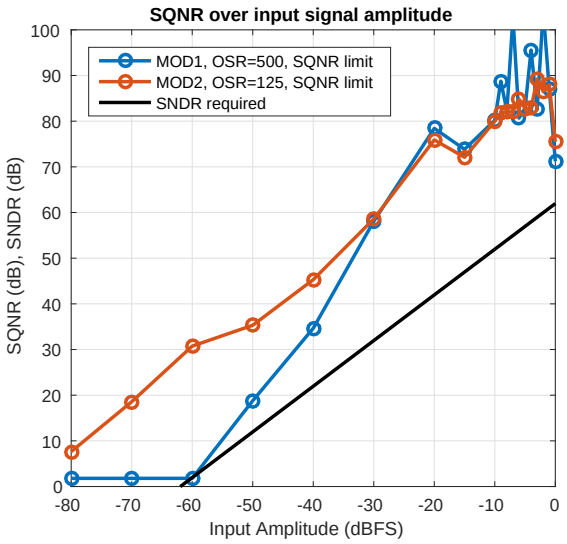

Figure 3.2: SQNR for changing input signal amplitude for first-order (MOD1) and second-order (MOD2) modulators. The black trace indicates the project specified SNDR.

finally implemented second-order modulator. The procedure for the first-order modulator would be similar but will not be discussed in this thesis.

3.3 Topology of the Modulator

Till now, only the basic topology of a second-order delta-sigma modulator as shown in Fig. 2.4 was investigated. As discussed in section 2.2, the zeros of the NTF of this topology are at $z = 1$, which corresponds to a frequency of $f = 0$. There are several more topologies available, which achieve different NTFs. This section shows the considerations made to find the most convenient topology of the second-order modulator for the given project related specifications and modes of operation.

A second-order modulator can either be implemented using a single, second-order loop, or using a so called multi-stage or MASH structure, a cascade of two first-order modulators. The advantage of MASH structures is that they avoid stability issues of higher order modulators by cascading low order modulators [35]. They usually need more power and a greater area than single stage modulators, since the quantizer and the DAC need to be implemented for every modulator in the cascade. Single stage modulators on the other hand are more tolerant to finite dc gain of the amplifiers and they are also more tolerant to capacitor mismatch in the switched-capacitor integrators [13]. Since the order of the modulator under consideration is quite low and the required area and power consumption are important specifications, a single loop implementation is the preferred choice for the design of the modulator.

Several architectures are available to implement the loop filter of a single-stage delta-sigma modulator. In this thesis, the most common ones will be discussed. Advantages and disadvantages of these architectures will be listed. Results of MATLAB simulations

will be shown. These simulations helped to determine the transfer functions of the discussed topologies and to find the gain factors required for signal scaling. Finally, the most convenient of these topologies will be selected for the implementation of the delta-sigma modulator for this thesis. For information to further topologies, the author refers to [13] and [21], where the information described in this section are gathered.

3.3.1 Loop Filters with Distributed Feedback and Input Coupling (CIFB)

A topology which can be seen as a direct implementation of the second-order modulator shown in Fig. 2.4 is the so called CIFB structure, the cascade of integrators with distributed feedback structure. Fig. 3.3 shows a more general structure of this architecture, which additionally includes distributed input coupling.

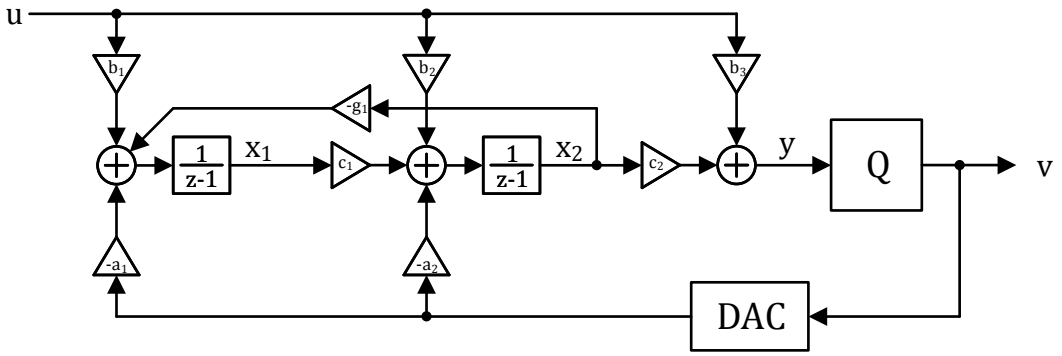

Figure 3.3: Second-order cascade of integrators with distributed feedback and input coupling (CIFB) topology. (Own compilation, adapted from [21]).

A common configuration, which is in the following referred as the general CIFB topology, can be achieved by choosing the gain coefficients to $a_i = b_i$ for $i \leq L$, $b_{L+1} = 1$ and $g_1 = 0$, where L is the order of the modulator. This configuration leads to a STF magnitude response which is equal to 1 in the frequency band from 0 to $f_s/2$ [21]. Furthermore, due to the distributed input coupling, the input signal $u[n]$ is not present at any integrator input. Thus, the loop filter only needs to process the quantization error, which leads to appropriate capacitor ratios to scale the integrator input signal to a convenient output swing [21]. This process of scaling is commonly refereed as dynamic range scaling. Using the MATLAB toolbox, the STF and the NTF of the described modulator topology were simulated. Furthermore, the root-mean-square gain of the NTF in the passband was determined. Using an OSR of 125 for the configuration described above and plotting the magnitude response of the NTF and the STF gives the results shown in Fig. 3.4. Additionally, the pole-zero diagram of the NTF was plotted. The magnitude of the STF is indeed 1 over the whole frequency range, thus the magnitude of the input signal gets not changed by this topology. The NTF has its zeros at dc ($z = 1$) and approaches, as specified in the simulation, $1.5 \approx 3.5dB$ for increasing frequency. The reader may wonder why this value of 1.5 was chosen as a maximum for the NTF. The properties of the NTF determine the stability of 1-bit modulators. Unfortunately, the properties which are necessary for a stable operation are not well known, since there is no simple derivation possible. Several approximations are available, whereas the modified *Lee criterion* [21,

36, 37], which postulates that a binary delta-sigma modulator is likely to be stable if $max|NTF(e^{j\omega})| < 1.5$, is the most used one. Thus, this approximation was used for the implementation of the delta-sigma modulator. The coefficients gained from simulation to implement these magnitude responses are $a_1 = b_1 = 0.55,\ a_2 = b_2 = 0.11,\ b_3 = 1,\ c_1 = 0.06,\ c_2 = 6.96$ and $g_1 = 0$, whereas a dynamic range scaling of 0.7 is assumed for the determination of the coefficients. For an input signal range of $800mV$ this would lead to a maximum output swing of $560mV$ at the integrators, which seems to be an appropriate value for the amplifiers to be implemented. The average value of the NTF gain in the signal bandwidth is equal to $-58dB$.

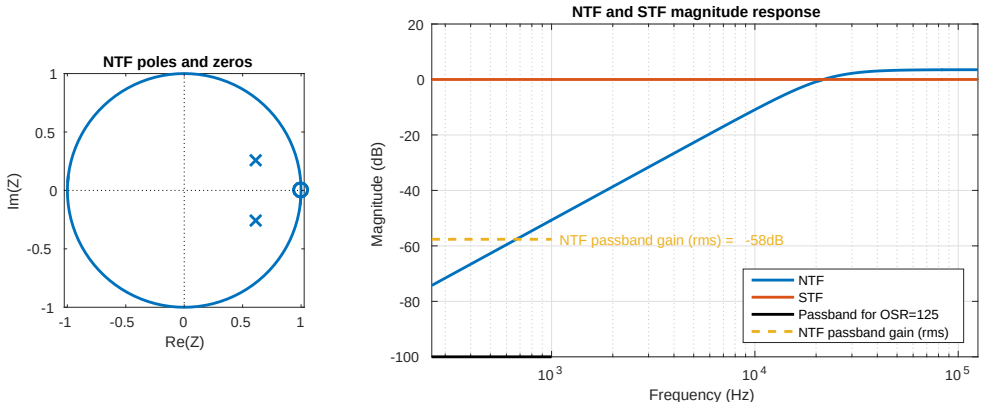

Figure 3.4: NTF pole-zero map and magnitude responses of the NTF and the STF of the general CIFB topology with coefficients $a_1 = b_1 = 0.55,\ a_2 = b_2 = 0.11,\ b_3 = 1,\ c_1 = 0.06,\ c_2 = 6.96$ and $g_1 = 0$.

A simplification of the topology shown in Fig. 3.3 can be achieved by setting the coefficients $b_i = 0$ for $i > 1$, leading to the topology discussed in chapter 2. This configuration, where the input signal is just feed in once, cancels the independence of the STF from the NTF [13]. This leads to a STF which changes its magnitude over the frequency. Fortunately, the magnitude of the STF is approximately 1 in the input signal frequency range and therefore the lowpass behavior has a low impact to the processed input signal. As discussed earlier, the zero of the NTF for this topology is again at dc. The timing for implementations of this topology is easier compared to the general architecture, since the input signal is not directly present at the quantizer [13]. A plot of the simulation results of the NTF and the STF magnitude responses as well as the pole-zero diagram of the NTF are shown in Fig. 3.5. Compared to the general CIFB structure shown before, the integrators now have to process the input signal, which requires greater scaling. This leads to coefficients $a_1 = b_1 = 0.15,\ a_2 = 0.09,\ b_2 = b_3 = 0,\ c_1 = 0.16,\ c_2 = 9.03$ and $g_1 = 0$ to implement this topology, where again a dynamic range scaling of 0.7 was assumed for the determination of the coefficients. An advantage of these simplified implementation is, that the coefficient c_2 does not need to be implemented, since the output signal of the second integrator is the only signal at the input of the 1-bit quantizer, which additionally saves area. The average value of the NTF gain in the signal bandwidth is $-58dB$, which is equal to that of the general CIFB topology.

Another modification can be achieved by using the coefficient g_1 to implement internal feedback from the output of the second integrator to the summing junction at the input of the first integrator. This opens the possibility to shift the zero of the NTF from dc to

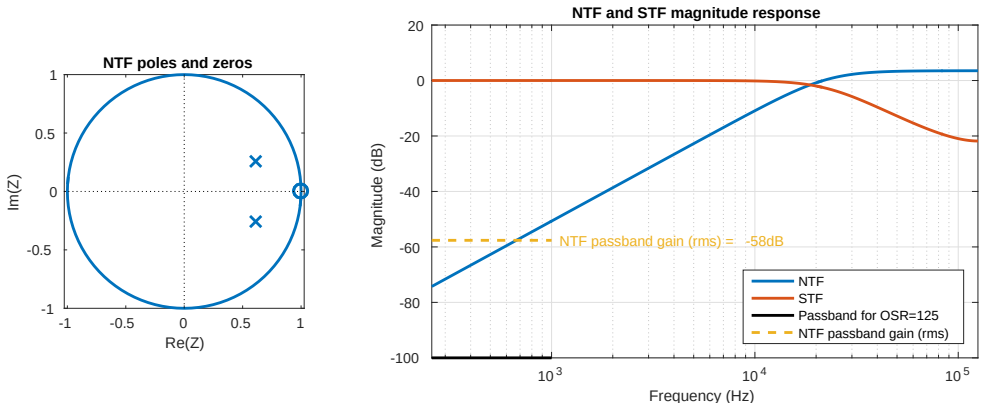

Figure 3.5: NTF pole-zero map and magnitude responses of the NTF and the STF of the simplified CIFB topology with coefficients $a_1 = b_1 = 0.15,\ a_2 = 0.09,\ b_2 = b_3 = 0,\ c_1 = 0.16,\ c_2 = 9.03$ and $g_1 = 0$.

some frequency greater than zero, to increase the attenuation in the band of interest [21]. Simulation of the transfer functions of such a topology gives the magnitude responses of the NTF and the STF as shown in Fig. 3.6. The coefficients to implement these magnitude responses are $a_1 = b_1 = 0.54,\ a_2 = b_2 = 0.12,\ b_3 = 1,\ c_1 = 0.06,\ c_2 = 6.69$ and $g_1 = 0.003$. The in-band attenuation for this configuration is increased to $61dB$.

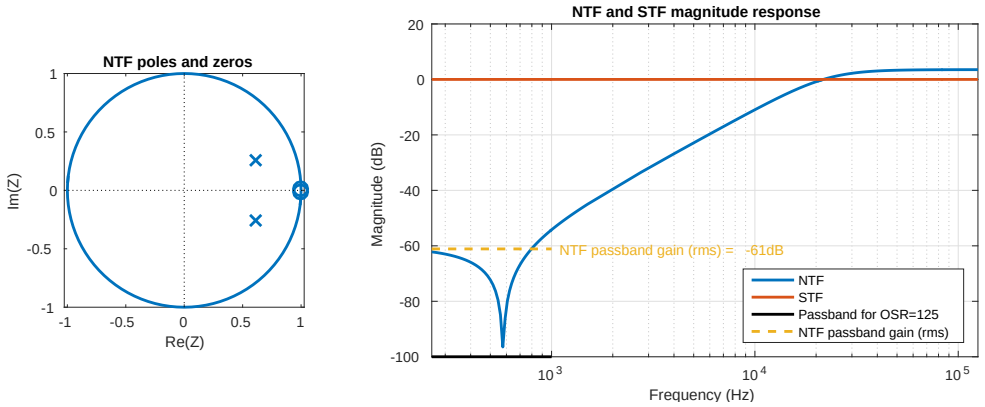

Figure 3.6: NTF pole-zero map and magnitude responses of the NTF and the STF of the CIFB topology with internal feedback using the coefficients $a_1 = b_1 = 0.54,\ a_2 = b_2 = 0.12,\ b_3 = 1,\ c_1 = 0.06,\ c_2 = 6.69$ and $g_1 = 0.003$.

The coefficients c_1 and g_1 are quite small, which would lead to big capacitor values at the integrators. The implementation of this configuration would consume much more area than the simplest architecture, where the coefficients b_2 and b_3 are set to zero and hence do not need to be implemented. Therefore, the disadvantage of the increased hardware complexity outweighs the advantage of higher attenuation in the band of interest, which makes this architecture inconvenient for the given project specifications.

3.3.2 Loop Filters with Distributed Feedforward and Input Coupling (CIFF)

Different topologies to implement the delta-sigma modulator are the cascade of integrators with distributed feedforward structures, short CIFF structures. As the name already suggests, they use feedforward paths instead of feedback paths. Fig. 3.7 shows the general architecture of such feedforward topologies for a second-order modulator.

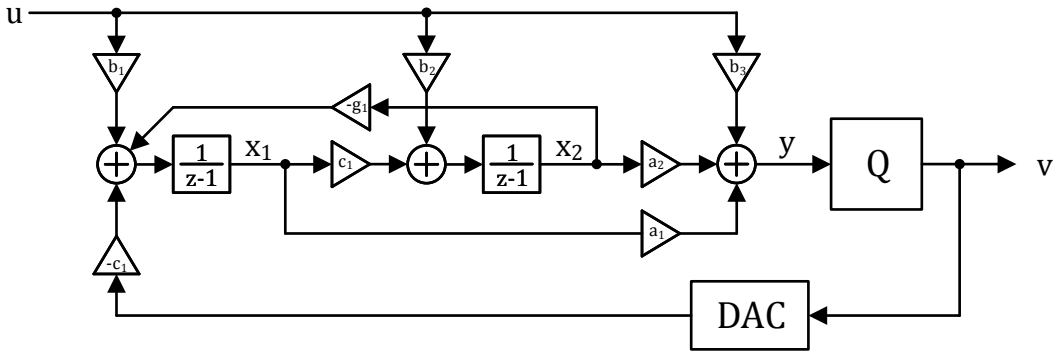

Figure 3.7: Second-order cascade of integrators with distributed feedforward and input coupling (CIFF) topology. (Own compilation, adapted from [21]).

Again, several implementations can be derived from this general architecture. As in the CIFB structures, implementations with and without multiple input feed-in can be considered which has again an impact to the swings occurring at the output of the integrators [38]. Furthermore, internal feedback using the g_1 coefficient can be implemented to perform optimal zero-placement in the NTF. An advantage of CIFF structures is, that they usually have relaxed dynamic range requirements, since they have a lower output swings due to the feedforward paths, which leads to smaller capacitor ratios [39]. This circuits therefore tend to be smaller and less power hungry than feedback topologies [13]. A drawback of feedforward topologies is, that analog signal summation needs to be performed before the quantizer, which requires additional hardware effort and therefore additional area. Another drawback is, that they often show a peaking in the STF which can lead to instabilities [13]. This peaking can be removed by multiple input feed-in, which on the other hand again makes the timing tricky, since the circuit needs to quantize the input signal and feed it back in "zero" time [38].

Different implementations of CIFF structures were investigated using the MATLAB toolbox. The best results with respect to the given specifications were achieved with the configuration where $b_i = 0$ for $i > 1$ and without optimized zero-placement ($g_1 = 0$). To implement this structure, the coefficients $a_1 = 1.59,\ a_2 = 9.5,\ b_1 = c_1 = 0.49,\ b_2 = b_3 = 0,\ c_2 = 0.05$ and $g_1 = 0$ have to be used. Simulation of the transfer functions yields magnitude responses of the NTF and the STF as shown in Fig. 3.8. This configuration provides a NTF in-band gain of $-58dB$, which is equal to that of the simplified CIFB structure. The peaking in the STF can clearly be seen. Fortunately, the peaking is outside the signal band, but it can still lead to stability issues [13].

Investigations on the presented architectures showed, that either the simplified CIFB structure or the simplified CIFF structure are the most convenient topologies for the

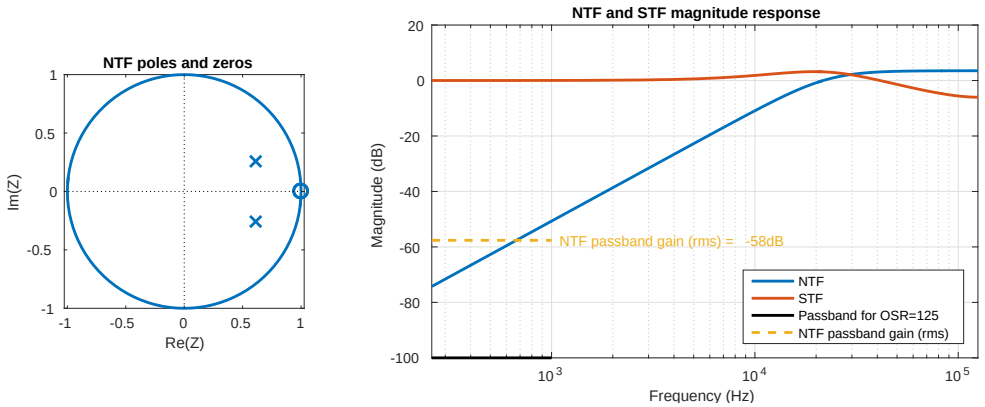

Figure 3.8: NTF pole-zero map and magnitude responses of the NTF and the STF of the simplified CIFF topology with coefficients $a_1 = 1.59$, $a_2 = 9.5$, $b_1 = c_1 = 0.49$, $b_2 = b_3 = 0$, $c_2 = 0.05$ and $g_1 = 0$.

implementation of the delta-sigma modulator for this thesis. The term simplified thereby refers to the topologies without multiple input feed-in and without internal feedback. Both topologies achieve the same in-band attenuation of the quantization noise. Capacitors in the CIFB structure will be somewhat bigger than the capacitors of the CIFF structure, but less capacitors are needed to implement the feedback architecture. The used CMOS process offers a highly linear poly-poly capacitor with a comparable high capacitance per unit area. As will be shown in chapter 4, a kT/C-noise limited design leads to capacitor values in lower fF range, thus they can be implemented very area efficient. Due to this reason, the feedback topology seems to be the better choice for the implementation of the modulator and was therefore selected for this thesis.

3.4 Conclusion

The considerations described in the previous sections showed, that the discrete-time, second-order delta-sigma modulator implemented using a feedback structure and an OSR of 125 seems to be the best choice for the implementation to fulfill the project specifications listed in section 1.3. Fig. 3.9 shows the gained topology which will be used for the implementation. Using the coefficients $a_1 = b_1 = 0.15$, $a_2 = 0.09$ and $c_1 = 0.16$ ensures appropriate dynamic range scaling. In case of ideal components, the magnitude responses as shown in Fig. 3.5 can be achieved.

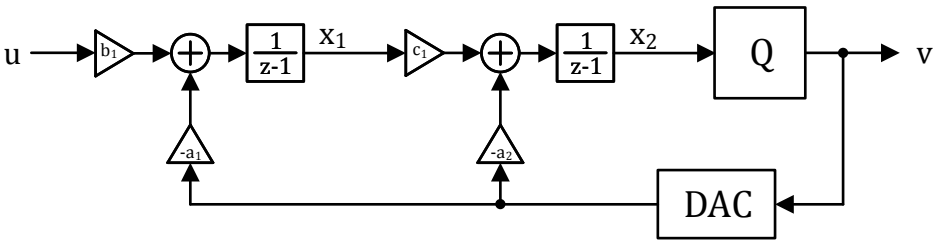

Figure 3.9: Topology of the implemented delta-sigma modulator with coefficients $a_1 = b_1 = 0.15,\ a_2 = 0.09$ and $c_1 = 0.16$.

Chapter 4

System-Level Implementation

With the help of MATLAB simulations, the most advantageous order and topology for the delta-sigma modulator regarding the given specifications were found. Thus, considerations about the circuit level implementation of the modulator can be made. First, the difference equations for the chosen topology will be derived. Using the obtained coefficients of chapter 3.3, the required capacitor ratios for the implementation of the switched-capacitor integrators will be determined. Afterwards, absolute values of the capacitors will be derived assuming a kT/C-noise limited design. With the results of the previous steps, a behavioral circuit will be implemented. The top-down design approach will then help to find the most advantageous circuit block requirements regarding modulator performance, power and area consumption, which will then be used for the transistor-level implementation of the modulator.

4.1 Derivation of the Difference Equations

The discrete-time integrators, which are often referred as switched-capacitor integrators, can either be implemented using delaying or non-delaying integrators. The difference between delaying and non-delaying integrators is basically just the arrangement of the switches in the switched-capacitor network. Fig. 4.1 shows the principle circuits of these two implementation types for a single-ended circuit, where ϕ_1 and ϕ_2 refer to the two phases of a non-overlapping clock signal. Both circuits actually perform the same, they integrate the input voltage V_{in}. Every clock cycle, the output of the integrators changes by $\Delta V_{out} = \frac{C_1}{C_2} V_{in}$. The difference between them is the time of sampling and integration. The delaying integrator samples the signal in one phase and performs the integration in the other phase, while the non-delaying integrator does both in the same phase. Thus, the transfer function of the delaying integrator is equal to $H(z) = \frac{C_1}{C_2} \frac{1}{z-1}$, while it is $H(z) = \frac{C_1}{C_2} \frac{z}{z-1}$ for the non-delaying integrator. Since the delaying integrator decouples the sampling phase from the integration phase, it does not see the load of the following circuit attached to it. That means, the first integrator just sees its capacitor in the feedback path during integration, but does not see the sampling capacitor of the second integrator. Thus, a delaying integrator design usually consumes less power compared to the non-delaying integrator design, since the requirements of the amplifier are lower [40].

Therefore, delaying integrators will be used for the implementation of the delta-sigma modulator for this thesis.

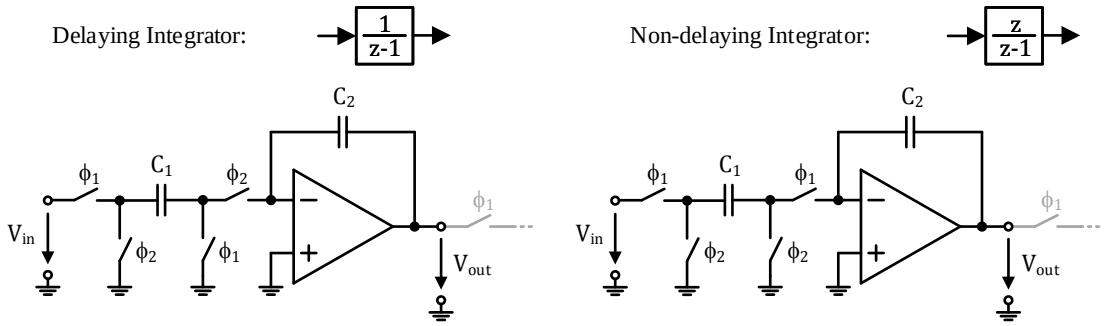

Figure 4.1: Delaying and non-delaying switched-capacitor integrator. The grey switch at the output of the integrators indicates the sampling switch of the next discrete-time integrator in the loop of the delta-sigma modulator.

Using the knowledge of the switched-capacitor integrator type, the difference equations of the topology to be implemented can be derived. The delaying integrators of Fig. 3.9 can be redrawn, leading to the block diagram shown in Fig. 4.2. Using this diagram, it is easier to determine the difference equations implemented by this topology. Since the DAC of a 1-bit, discrete-time delta-sigma modulator just selects the reference voltage which is feed back to the inputs of the integrators without introducing an additional delay, it can be neglected for the derivation of the difference equations. The following difference equations can be found from the block diagram of Fig. 4.2:

$$x_1[n+1] = x_1[n] + b_1 \cdot u[n] - a_1 \cdot v[n] \tag{4.1}$$

$$x_2[n+1] = x_2[n] + c_1 \cdot x_1[n] - a_2 \cdot v[n] \tag{4.2}$$

$$v[n] = Q\left(x_2[n]\right) \tag{4.3}$$

To implement these difference equations, first a simplified switched-capacitor circuit was created. The used realization for this thesis is shown in Fig. 4.3. To ensure that the circuit

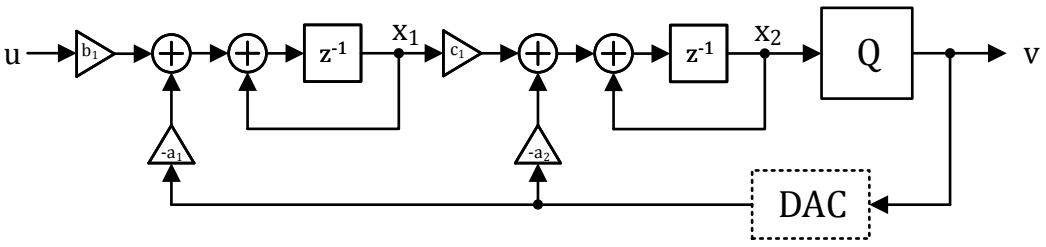

Figure 4.2: Rearranged z-domain block diagram of the delta-sigma modulator. The blocks for the delaying integrators are replaced with a delay element and a local feedback loop, which is an equivalent representation, but simplifies the derivation of the difference equations implemented by this topology. The DAC in the feedback loop of the modulator is drawn in dashed lines, since it does not introduce a delay.

indeed implements the desired difference equations, a timing diagram of the realization was generated as shown in Fig. 4.4. As can be seen, the timing seems to be correct and possible to achieve with blocks on circuit level. Due to the usage of delaying integrators, the first discrete-time integrator has a complete clock cycle to settle and the second integrator has roughly half a clock cycle to settle, which will be appropriate since the 1-bit quantizer does not need a fully settled input signal to achieve a valid logic level. Thus, a very power efficient implementation of the delta-sigma modulator with respect to the timing was found.

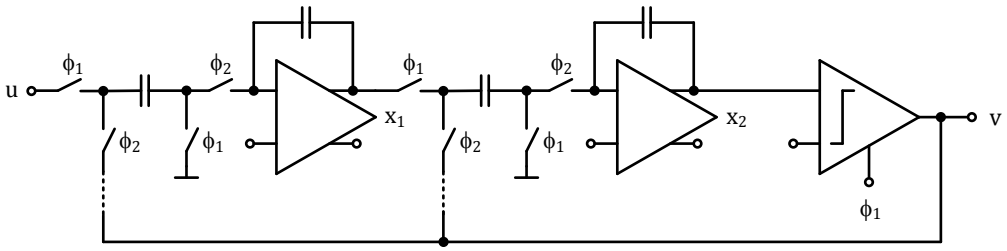

Figure 4.3: Simplified switched-capacitor realization of the modulator. The dashed lines indicate the DAC in the feedback loop.

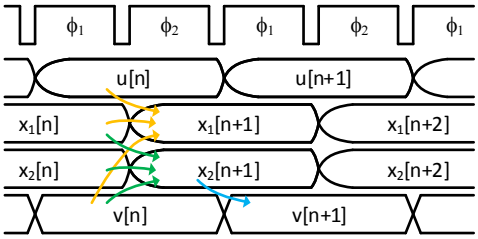

Figure 4.4: Timing diagram of the switched-capacitor realization of Fig 4.3.

4.2 Single-Ended vs. Fully-Differential Implementation

The last decision before the behavioral model of the delta-sigma modulator can be generated is the decision between a single-ended and a fully-differential implementation of the modulator. Advantages and disadvantages of those with respect to the project specifications will be listed in this section. Used implementations in published papers will be discussed. With the gained information, the most convenient type for this thesis will be selected.

A fully-differential implementation of the integrator amplifiers provides double the output swing at each integrator output compared to a single ended implementation. Due to the differential signal provided by them, they have a better noise behavior since they suppress common-mode noise captured from the environment. Furthermore, nonidealities of the switches like charge injection and clock feedthrough appear as common mode disturbances at the input of the amplifiers and get suppressed by them, therefore [41]. Another advantage is that they avoid mirror poles in the integrator amplifiers, which lead to increased stability and higher closed loop speed. Using a fully-differential scheme doubles

the number of capacitors needed for the implementation of the switched-capacitor integrators. But, in a kT/C-noise limited design, each sampling capacitor would have half the value compared to the capacitors of a single-ended implementation, while still achieving the same SNR [42]. Thus, the area consumption of the capacitors would be similar for both implementation types. A drawback of fully-differential implementations is that the amplifier circuits need a common-mode feedback to set the operating point, which leads to increased hardware complexity, area consumption and power consumption. Additionally, a single-ended to differential conversion would be needed, since the input signal for the delta-sigma modulator is given as a single-ended signal. Thus, further amplifier stages would be needed. A literature study showed that fully-differential implementations are heavily used in delta-sigma ADCs with resolutions of 15-bits and more, but there are also several implementations as found in [15] and [16], where a fully-differential circuit was used for similar specifications as for this thesis. Nevertheless, there are publications using single-ended implementations as in [2, 17] and [28]. Additionally, some implementations using pseudo-differential schemes were found, but they are in the minority. For the implementation of the modulator for this thesis, a single-ended scheme was selected, since it should be appropriate for the desired resolution. Furthermore, it is assumed that the single-ended implementation consumes less power and area, therefore it seems to be the better choice for the given project specifications.

4.3 Behavioral Model of the Modulator

Using the information of the previous sections, a behavioral model of the delta-sigma modulator can be created. With this model, impacts of nonidealities associated with the amplifiers like finite amplifier gain, limited bandwidth and slew rate or nonidealities of the switches like the on-resistance can be investigated. The simplified switched-capacitor circuit shown in Fig. 4.3 will therefore be adapted and a SPICE-simulatable schematic will be generated. Capacitor values as well as the theoretical requirements for the individual circuit blocks to fulfill the given project specifications will be calculated.

The translation of the block diagram of Fig. 3.9 into a behavioral schematic was done by replacing the individual blocks by their behavioral models. Fig. 4.5 shows the finally generated circuit. The way of proceeding to design this model as well as the selection of the reference voltages will be discussed in the following.

The delaying integrators of the block diagram can be replaced by the switched-capacitor implementations discussed in section 4.1. Since the modulator will be operated with a single-ended supply, the reference voltage levels of the integrators need to be adapted. Since the gain coefficients a_1 and b_1 of the block-diagram are equal, the same physical sampling capacitor C_1 can be used for the first integrator to implement the desired difference equation [21], which fortunately reduces the required area. For the second integrator, two separated capacitors C_3 and C_4 must be used to process the output signal of the first integrator and the feedback signal of the modulator output, since the gain coefficients a_2 and c_1 are different.

Since the output signal of the delta-sigma modulator is a 1-bit output stream, the quantizer can simply be replaced by a comparator. The reference voltage for the comparator must be equal to the common-mode voltage of the second integrator.

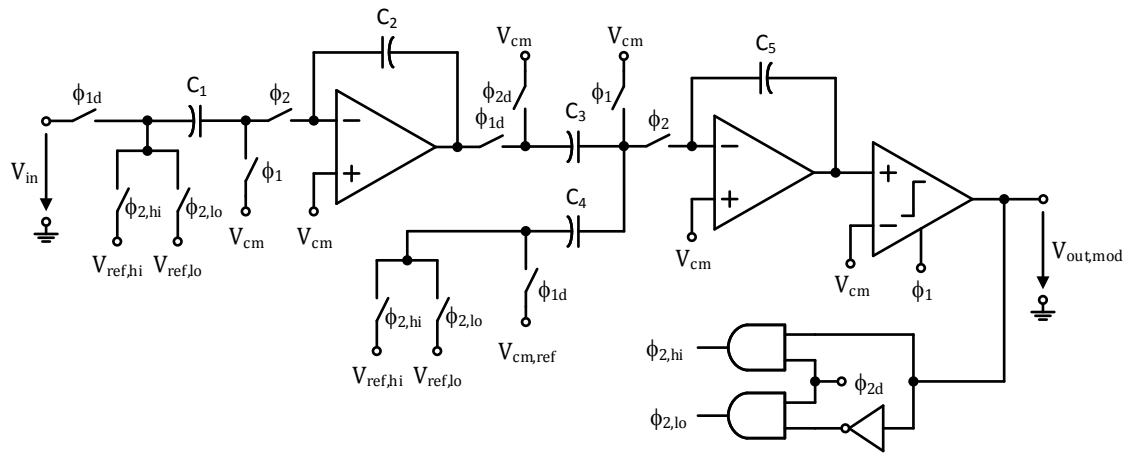

Figure 4.5: Behavioral model of the second-order delta-sigma modulator. The same physical capacitor C_1 is used to process the input and the feedback signal in the first integrator. Two separated capacitors C_3 and C_4 are used to process the output signal of the first integrator and the feedback signal in the second integrator. The 1-bit quantizer is implemented using a latched comparator. The DAC consists of logic gates which control the switches in the feedback path.

As discussed, the feedback DAC shown in Fig. 3.9 is simply a selector between two feedback voltage levels and can therefore be implemented using logic gates. Depending on the logic level at the output of the modulator, either the "positive" or the "negative" feedback voltage will be selected. Since the modulator is operated at a single ended supply and a specified input voltage range of $0V$ to $800mV$, the common mode level of the feedback signal $V_{cm,ref}$ was selected to same common mode level as the input signal. This leads to a "negative" reference voltage of $V_{ref,lo} = 0V$ and a "positive" reference voltage of $V_{ref,hi} = 800mV$ for a chosen reference voltage range equal to the input signal range.

The common-mode level of both discrete-time integrators was chosen to $V_{cm} = 550mV$, since this voltage level leads to a maximum symmetrical output swing of the designed amplifiers as will be shown in section 6.1.1. It is worth to mention that usually the most convenient common-mode level is not well-known at this point of time. Therefore, a convenient value to do the calculations of the circuit block requirements is to use a common-mode level equal to half the supply voltage. Changes at a later point of time usually just lead to minor changes in the calculated capacitor ratios, thus only the capacitor sizing, which will be shown in section 4.3.1, needs to be redone.

The non-overlapping clock signals ϕ_1 and ϕ_2 required for the switched-capacitor integrators were generated using pulse sources in the behavioral model. To reduce nonlinearities due to signal dependent charge injection, which will be necessary for the transistor-level implementation of the modulator, additional clock signals ϕ_{1d} and ϕ_{2d} were used at the driven side of the switched-capacitor networks. These clock signals are identical to the non-overlapping clock signals ϕ_1 and ϕ_2, but they have an additional delay in the falling edge as will be shown in section 6.1.6. Thus, the switches at the summing junction of the amplifier open slightly earlier than the switches on the signal conducting side. Therefore, signal dependent charge from the driven side cannot be injected to the sampling capacitors,

since there is no contacting path to the second plate of the capacitor any more [13].

The capacitors were already implemented using real components, whereas highly linear poly-poly capacitors were used for that. Since the plates of integrated capacitors are usually arranged in parallel to the substrate, non negligible parasitic capacitances against the substrate exist. The parasitic capacitance of the plate closer to the substrate, which is called bottom plate, can be as big as 20% of the actual desired capacitance [23]. The parasitic capacitance of the top plate is smaller compared to that of the bottom plate. Since the parasitic capacitance on the summing junction of the switched-capacitor integrators degrades the effectiveness of the delayed clocking, the top plate of the capacitors was connected to the summing junction of the integrators [38].

The following sections discuss the selection of appropriate parameters for the individual circuit blocks of the behavioral model. Using simplified models, specifications of the blocks will be derived. Nevertheless, the finalized specifications of the circuit blocks will be determined by simulation of the created behavioral model.

4.3.1 Capacitor Sizing

The first step in finding appropriate block parameters for the behavioral model is the determination of absolute capacitor values, since these determine the requirements of other circuit blocks like the switches and the amplifiers of the integrators. For the determination of the capacitor values, first the required capacitor ratios need to be determined. The capacitor ratios depend on the chosen reference voltages of the modulator. With the gained information, convenient absolute values for the capacitors can be determined afterwards.

To determine the capacitor ratios of the switched-capacitor integrators, the difference equations (4.1), (4.2) and (4.3) of the block diagram shown in Fig. 4.2 need to be adjusted, to translate the coefficients a_1, a_2, b_1 and c_1 to capacitor ratios for the behavioral circuit. The *Delta-Sigma Toolbox* used for MATLAB simulations to determine the required gain coefficients assumes by default that the input and the output of the integrators occupy values in the range from -1 to $+1$. As mentioned in section 3.3, the scaling of the modulator was determined to 0.7, since this leads to a reasonable swing at the output of the integrator amplifiers. Thus, the integrator output states occupy the range from -0.7 to $+0.7$. The output of the binary modulator is by default determined to either -1 or $+1$. To map the ranges of the block diagram to the behavioral circuit, a translation of the unit-less ranges to the desired signal ranges is required. Starting with the first integrator of the modulator, which is implemented as shown in Fig. 4.6. To map the specified input signal range V_{in} of $0V$ to $800mV$ to the toolbox default range of $[-1, +1]$, the input signal $u[n]$ in the difference equations needs to be replaced with

$$u[n] = \frac{V_{in}[n] - 0.4V}{0.4V}. \tag{4.4}$$

The same must be performed for the output of the integrator. Due to scaling, the output signal of the integrator will be in a range from $270mV$ to $830mV$ at a common-mode level of $V_{cm} = 550mV$. To map these voltage range to the toolbox range $[-0.7, 0.7]$, equation

$$x_1[n] = \frac{V_{x_1}[n] - 0.55V}{0.4V} \tag{4.5}$$

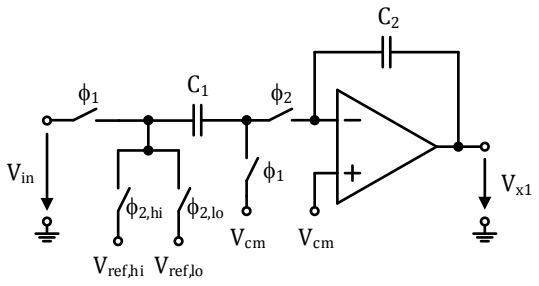

Figure 4.6: First integrator of the second-order modulator. Since the gain coefficients a_1 and b_1 are equal, the same physical capacitor C_1 is used to process the input and the feedback signal.

must be inserted to the difference equations. The output of the implemented single-bit modulator $V_{mod}[n]$ will be either the positive supply V_{dda} or $0V$, which is interpreted as either a logic high ($V_{mod}[n] = 1$) or logic low ($V_{mod}[n] = 0$) signal that selects the level of the feedback signal. Thus,

$$v[n] = 2 \cdot V_{mod}[n] - 1 \tag{4.6}$$

must be used to map the output to the toolbox default of $[-1, +1]$.

Inserting these mapping equations to the block diagram difference equation (4.1) leads to

$$\frac{V_{x_1}[n+1] - 0.55V}{0.4V} = \frac{V_{x_1}[n] - 0.55V}{0.4V} + b_1 \cdot \frac{V_{in}[n] - 0.4V}{0.4V} - a_1 \cdot (2 \cdot V_{mod}[n] - 1). \tag{4.7}$$

Performing simplifications and inserting $a_1 = b_1 = 0.15$ gives

$$V_{x_1}[n+1] = V_{x_1}[n] + 0.15 \cdot V_{in}[n] - 0.12 \cdot V_{mod}[n]. \tag{4.8}$$

Analysis of the circuit of the first integrator of the modulator in Fig. 4.6 shows, that the discrete-time integrator performs the difference equation given by

$$V_{x_1}[n+1] = V_{x_1}[n] + \frac{C_1}{C_2} \cdot V_{in}[n] - \frac{C_1}{C_2} \cdot V_{ref} \cdot V_{mod}[n], \tag{4.9}$$

where the value of V_{ref} is equal to $V_{ref,hi}$.

Solving equation (4.8) and (4.9) for C_1/C_2, leads to the desired capacitor ratio of

$$\frac{C_1}{C_2} = 0.15. \tag{4.10}$$

For the second integrator, the sampling capacitor is split up, since the coefficients c_1 and a_2 of Fig. 3.9 are unequal, leading to the circuit shown in Fig. 4.7. Again, the mapping between the *Delta-Sigma Toolbox* ranges and the real voltage ranges must be done. Doing the same steps as for the first integrator leads to the mapping equations

$$x_1[n] = \frac{V_{x_1}[n] - 0.55V}{0.4V}, \tag{4.11}$$

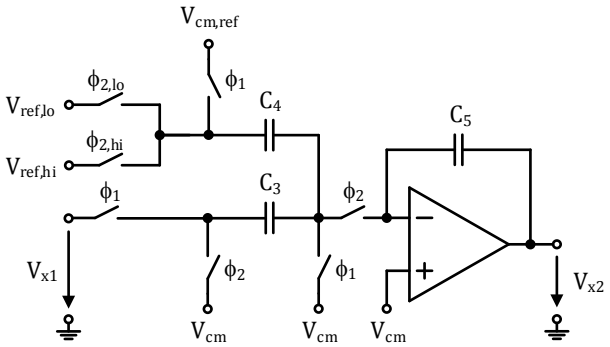

Figure 4.7: Second integrator of the second-order modulator. Since the coefficients a_2 and c_1 are unequal, two separated capacitors C_3 and C_4 are used to process the output signal of the first integrator and the feedback signal.

$$x_2[n] = \frac{V_{x_2}[n] - 0.55V}{0.4V} \tag{4.12}$$

and

$$v[n] = 2 \cdot V_{mod}[n] - 1 \tag{4.13}$$

for the second integrator. Inserting these equations to the difference equation (4.2) and performing simplifications results in

$$V_{x_2}[n+1] = V_{x_2}[n] + 0.16 \cdot V_{x_1}[n] - 0.072 \cdot V_{mod}[n] - 0.052V, \tag{4.14}$$

if the coefficients $c_1 = 0.16$ and $a_2 = 0.09$ are used.

Inspection of the switched-capacitor integrator in Fig. 4.7 gives the difference equation implemented by this circuit to

$$V_{x_2}[n+1] = V_{x_2}[n] + \frac{C_3}{C_5} \cdot V_{x_1}[n] - \frac{C_4}{C_5} \cdot V_{ref} \cdot V_{mod} - \frac{C_3}{C_5} \cdot V_{cm} + \frac{C_4}{C_5} \cdot V_{cm,ref}, \tag{4.15}$$

where again the value of V_{ref} is equal to $V_{ref,hi}$, the value of V_{cm} is equal to $550mV$ and the value of $V_{cm,ref}$ is equal to $400mV$.

Solving equation (4.14) and (4.15) for the capacitor ratios C_3/C_5 and C_4/C_5 leads to

$$\frac{C_3}{C_5} = 0.16 \tag{4.16}$$

and

$$\frac{C_4}{C_5} = 0.09. \tag{4.17}$$

Since all the ratios of the capacitors are now determined, arbitrary capacitor values that fulfill the desired ratios could be used for the implementation of the delta-sigma modulator. This might be the fastest and easiest possibility to find absolute values of the capacitors, but with respect to power and area consumption it will for sure not be the best choice. State-of-the-art low power and high performance circuits use the different concept of a

kT/C-noise limited determination of the absolute capacitor values. In such designs, the total performance of the modulator is limited by the chosen capacitor values, while the most power and area efficient implementation of the capacitors is ensured. This concept was chosen for the determination of the capacitor values for the modulator of this thesis.

Starting again with the first integrator of the delta-sigma modulator shown in Fig. 4.6. If the noise of the amplifier is neglected as done in [42], the total mean square noise voltage of the sampling capacitor C_1 over both phases ϕ_1 and ϕ_2 is given by

$$\overline{v_n^2} = \frac{2kT}{C_1}, \tag{4.18}$$

where k is the Boltzmann's constant and T the temperature in Kelvin. This stored thermal noise is uniformly spread over the frequency band from 0 to $f_s/2$, thus the total in-band kT/C-noise power is given by

$$\overline{v_{n_{in}}^2} = \frac{\overline{v_n^2}}{\mathrm{OSR}}, \tag{4.19}$$

which again shows a big advantage of oversampling ADCs.

Assuming the specified input signal range of $0V$ to $800mV$, assuming further the common-mode level of this signal to $400mV$ and a sinusoidal input signal with an input amplitude A of $-3dBFS$, where $0dBFS$ is equal of $400mV$, the signal power can be calculated to

$$\overline{v_s^2} = \left(\frac{A}{\sqrt{2}}\right)^2 = \frac{\left(\frac{0.4V}{\sqrt{2}}\right)^2}{2} = 0.04V^2. \tag{4.20}$$

The kT/C-noise determined SNR in the band of interest can be calculated using

$$\mathrm{SNR} = 10\ log\left(\frac{\overline{v_s^2}}{\overline{v_{n_{in}}^2}}\right). \tag{4.21}$$

The desired SNDR for a $-3dBFS$ sine wave input signal to achieve a resolution of 10-bits is equal to $58.96dB$. Since the input referred noise of the amplifier and harmonic distortions were neglected, it is advisable to add a margin to this determined SNR value. Assuming a kT/C-noise limited SNR of $70dB$ leads to a maximum allowed in-band noise power of

$$\overline{v_{n_{in}}^2} = \frac{\overline{v_s^2}}{10^{\frac{\mathrm{SNR}}{10}}} = \frac{0.04V^2}{10^{\frac{70}{10}}} = 4nV^2. \tag{4.22}$$

Using equation (4.18) and (4.19) and the maximum allowed in-band noise power calculated in equation (4.22), the minimum capacitor value of the sampling capacitor C_1 at a temperature of $T = 300K$ can be calculated to

$$C_1 = \frac{2kT}{\mathrm{OSR} \cdot \overline{v_{n_{in}}^2}} = \frac{2 \cdot 1.38 \cdot 10^{-23}\ \frac{m^2kg}{s^2K} \cdot 300K}{125 \cdot 4nV^2} \approx 16.56fF. \tag{4.23}$$

Choosing a capacitor value of $C_1 = 17fF$, leads to a convenient SNR margin even for higher temperatures in the specified temperature range. The value of the capacitor C_2 can be calculated to $C_2 = 113.3fF$ using equation (4.10). Since the two capacitors C_1 and C_2

should match for optimal performance, unit capacitors were used for the implementation. Choosing the size of the unit capacitor to $17fF$ and using one of these for C_1 and seven of these in parallel for C_2, the implemented capacitor ratio C_1/C_2 is equal to 0.1429.

The thermal noise contribution of the second integrator is negligible, since the noise at the input of the second integrator is shaped by the inverse transfer function of the first integrator [21]. Thus, the used capacitors at the second integrator can be much smaller, than the capacitors of the first integrator. These capacitors are usually dictated by charge injection of the switches rather than thermal noise [42]. Investigations on switches showed, that the error of charge injection is even for capacitors in the very low fF range negligible, since the used transistor sizes of the switches are quite small. Thus, the value of the capacitor C_4 was chosen to the minimum available value of the used process, which promises an accurate capacitance. This leads to a value of $9.25fF$ for this capacitor, which defines the size of a unit capacitor for the second integrator. Using equation (4.16) and (4.17), the ideal capacitor values of C_3 and C_5 could be calculated to $16.4fF$ and $102.8fF$ respectively. Using two unit capacitors for C_3 and twelve unit capacitors for C_5 leads finally to values of $18.5fF$ and $111fF$ for C_3 and C_5.

4.3.2 Integrator Amplifier Requirements

With the knowledge of the absolute capacitor values, specifications for the amplifiers of the integrators can be determined. The most important constraints of the amplifiers in discrete-time delta-sigma modulators are the dc-gain, the unity-gain-frequency (UGF) and the slew rate (SR). As discussed in section 3.2, finite amplifier dc-gain leads to a leaky integrator, which causes a nonideal transfer function of the integrator and hence a lower attenuation of the in-band quantization noise. Boser and Wooley showed in [43], that a dc-gain as low as the OSR of the modulator should be appropriate to limit the decrease of the in-band SNR to less than $1dB$. For the OSR of 125, this would lead to a minimum required gain of approximately $42dB$. Schreier and Caldwell on the other hand propose in [38] that a dc-gain of

$$A_1 > \frac{C_1}{C_2} \cdot \frac{\mathrm{OSR}}{\pi} \tag{4.24}$$

for the amplifier of the first integrator is appropriate to do not degrade the noise shaping performance significantly. For the design of this thesis, this would lead to an even lower minimum required gain of roughly $16dB$. Typical operational transconductance amplifier (OTA) implementations provide dc-gains which are greater than both above derived values. Nevertheless, for first simulations a very conservative dc-gain of $40dB$ was assumed. The impact on the dead-band behavior of the modulator regarding the chosen dc-gain will be checked with simulations. The UGF determines the speed of the amplifier. This constraint is not that stringent, but common implementations use a UGF of the amplifier which is approximately 5-times the sampling frequency f_s of the switched-capacitor integrator [34]. Thus, the UGF was determined to

$$UGF = 5 \cdot f_s = 5 \cdot 250kHz = 1.25MHz. \tag{4.25}$$

The SR of the amplifier must be high enough to provide linear settling [43]. If the worst case is assumed, where the input voltage of the first integrator is $0V$ and the feedback

level is at $800mV$, initially a voltage difference of $V_d = 800mV$ is present between the two input nodes of the amplifier. If it is further assumed that slewing should just take 1/4-th of the sampling period, a minimum slew rate of

$$SR = \frac{\Delta V}{\Delta t} = \frac{V_d \cdot \frac{C_1}{C_2}}{\frac{T}{4}} = \frac{0.8V \cdot 0.1429}{\frac{1}{4 \cdot 250kHz}} \approx 0.114 \frac{V}{\mu s} \tag{4.26}$$

is required. For first behavioral simulations, a SR of $0.15V/\mu s$ was assumed. The desired phase margin (PM) was determined to roughly 65°, since from experience this value provides a good trade-off between appropriate speed and overshoot.

4.3.3 Comparator Requirements

For the implementation of the 1-bit quantizer, a comparator is used. Nonidealities of the comparator like offset and noise are treated similar as quantization noise and are therefore suppressed by the noise shaping property of the delta-sigma modulator. For example, if the offset of the comparator is given by $v_{os,comp}$, then the input referred offset of the comparator in the second-order modulator is equal to $v_{os,input} = \frac{v_{os,comp}}{A_1 \cdot A_2}$, where A_1 and A_2 are the dc-gains of the two integrators in the loop [13]. Thus, the requirements for the comparator are quite relaxed.

But there are still some topics which are of importance for the performance of the modulator. An important constraint for the comparator used in the modulator is the generation of a valid logic level at a certain point of time [13]. Thus, latched comparators which provide an update of the output voltage once every clock cycle, are perfectly convenient for the desired application in delta-sigma modulators.

There are some other points which are of interest. One of those is the comparator metastability. Since the output of the comparator controls the feedback network of the delta-sigma modulator consisting of logic gates, a valid logic level is required. In case of metastability, it is not that important if the comparator puts out a 0 or a 1, it is only important to deliver a valid logic level [13]. Nevertheless, the goal is to hold the metastability range as small as possible by providing high enough gain in the comparator. Another important constraint is the hysteresis of the comparator. Comparator hysteresis leads to decisions, which depend on previously made decisions. This can create unwanted system poles which can lead to errors in the transfer functions and thus degraded performance of the delta-sigma modulator [13]. Investigation done by Boser and Wooley showed, that comparator hysteresis up to 5% of the full-scale input range has a negligible impact on the performance of the ADC [43]. For the specified input range of $800mV$, this would lead to an allowable hysteresis range of $40mV$. A very important, project specific requirement for the comparator is a low kickback property, since kickback would lead to distortions of the reference voltages of the delta-sigma modulator, as will be further discussed in chapter 6.

Since it is difficult to provide certain values for the mentioned comparator constraints at this point of time, the impact of those was analyzed by simulations of the transistor-level implementation of the delta-sigma modulator. For the behavioral model, the comparator was therefore assumed to be ideal.

4.3.4 Further Circuit Blocks

To implement the switched-capacitor circuits needed for the discrete-time integrators, switches are necessary. Since real switches show a finite on-resistance, it is important to investigate nonidealities associated with them.

Switches in CMOS integrated circuits are implemented using transistors in the linear region. Unfortunately, the on-resistance of such MOSFET switches varies with changing gate to source voltage V_{gs} and is hence dependent on the input level. Thus, the switches cannot simply be treated as a R-C network, given by the on-resistance of the switch and the capacitance of the sampling capacitor, acting as a linear filter with a certain cut-off frequency and time constant [38]. Thus, the on-resistance of the switches needs to be kept low enough, to achieve an adequate settling time for any arising input voltage level. Furthermore, a low on-resistance of the switches is desired with respect to noise produced by them. To reduce the on-resistance of a MOSFET switch, the aspect ratio W/L of the corresponding transistor needs to be increased. On the other hand, a large transistor leads to other nonidealities like charge injection and clock feedthrough. Thus, there are trade-offs between the mentioned properties, which will be discussed in more detail in section 6.1.4, where the transistor-level implementation of the switches will be explained. In this subsection, only the impact of the on-resistance with respect to the settling behavior will be treated.

As shown by Schreier and Caldwell in [38], the on-resistance of the switches increases the settling time τ of the switched-capacitor integrators by a factor of $(1 + g_m \cdot R_{on,tot})$, where g_m is the transconductance of each input transistor of the integrator amplifier and $R_{on,tot}$ is the total on-resistance in the integration phase. To make the increase in τ appropriate, a total on-resistance of

$$R_{on,tot} \leq \frac{1}{40\ g_m} \tag{4.27}$$

is proposed in [38]. Thus, to determine the maximum allowed on-resistance of the switches, first the required transconductances g_m of the input transistors of the amplifiers must be estimated. For this estimation, single stage OTAs were assumed as amplifiers of the integrators. Furthermore, it was assumed that these amplifiers behave like first-order systems till the UGF, thus the required g_m can be estimated by transforming

$$UGF = A_0\ \omega_{pd} = \frac{g_m\ R_{out}}{R_{out}\ C_L} = \frac{g_m}{C_L} \tag{4.28}$$

to

$$g_m = UGF \cdot C_L, \tag{4.29}$$

where A_0 is the dc-gain of the amplifier, $\omega_{pd} = \frac{1}{R_{out}\ C_L}$ is the dominating pole of the amplifier, R_{out} is the output resistance of the amplifier and C_L is the load capacitance in the integration phase. Since delaying integrators are used, the load capacitance of the amplifiers is approximately equal to the capacitances in the feedback loop of the integrator. Using equation (4.29), the required transconductance g_m of each input transistor of the first integrator for the UGF of $1.25MHz$ determined in (4.25) can be calculated to

$$g_m = 2\pi \cdot 1.25MHz \cdot 119fF \approx 1\frac{\mu A}{V}. \tag{4.30}$$

Using equation (4.27), the maximum allowed total on-resistance can therefore be calculated to

$$R_{on,tot} \leq \frac{1}{40 \cdot 1\frac{\mu A}{V}} = 25k\Omega. \tag{4.31}$$

Since the load capacitance of the second integrator of the delta-sigma modulator is roughly equal to the load capacitance of the first integrator, the same total on-resistance is allowed for this integrator. In the integration phase, the total on-resistance of each of the two integrators comprises from two closed switches in series to the integration path [38]. Thus, the on-resistance of each switch is limited to $R_{on} = R_{on,tot}/2 = 12.5k\Omega$. Since parasitic capacitances were neglected in this calculation, it is desired to achieve a somewhat lower total on-resistance as stated in (4.31). A conservative but adequate value with respect to the upcoming transistor-level implementation is an on-resistance of $5k\Omega$ for each switch. Therefore, this value was chosen for the switches in the behavioral model of the delta-sigma modulator.

To implement the DAC in the feedback path of the modulator, a simple inverter and AND-gates were used. There are no specific requirements for these gates.

With the findings of this chapter the implementation of the behavioral model of the delta-sigma modulator in an electronic design automation (EDA) tool is possible. For this thesis, the Cadence[1] Virtuoso platform was used. For the implementation of the behavioral model shown in Fig. 4.5, Verilog-A models for the amplifiers, the comparator and the logic gates of the feedback network were used. The switches were implemented using models where the on-resistance could be determined. The required reference voltages as well as the non-overlapping clock signals ϕ_1 and ϕ_2 were generated with ideal voltage sources. The determined block parameters allow a first simulation of the implemented system-level model. Nevertheless, to ensure that the result of this simulation is as intended, a verification of the delta-sigma modulator is required, which will be discussed in the next chapter.

[1] https://www.cadence.com/

Chapter 5

System-Level Verification and Characterization

To check that the modulator performs as desired, a verification and characterization of the created behavioral model is required. The first part of this chapter focuses on proposed verification steps for delta-sigma modulator implementations. In the second part, a characterization of the verified delta-sigma modulator will be done. Different performance characterization tests will be presented, which check the modulator against the given project specifications. In case of violations of the specifications, the block requirements determined in the previous chapter will be adapted. At the end of this chapter, a fully verified and characterized delta-sigma modulator in behavioral form will be available.

5.1 Verification of the Behavioral Model

To verify that the modulator behaves as desired, or in other words, that it really implements the desired difference equations determined in chapter 4, several steps are proposed to check by Schreier, Temes and Caldwell in [21] and [42]. This section deals with those steps, which check the behavior of the loop filter, the swing of the integrators and the output spectrum of the modulator.

5.1.1 Loop Filter

To verify the correct behavior of the loop filter and thus the correct translation of the block diagram gain coefficients to capacitor ratios on circuit level, the impulse response of the loop filter is checked against the ideal response of the difference equations. Therefore, the feedback loop of the modulator is opened, the outputs of the integrators are initialized to their common-mode level of $550mV$ and an impulse $\delta[n]$ is fed into the input of the feedback DAC, while the real input of the modulator is set to zero, as can be seen in Fig. 5.1. Since the switched-capacitor realization of the modulator is designed for a unipolar input range and supply voltage, an input of zero for the block diagram can be achieved by applying $V_{in_{max}}/2 = 400mV$ at the input of the behavioral model. Furthermore, a zero at the output of the block diagram corresponds to a voltage level of $V_{dda}/2$ at

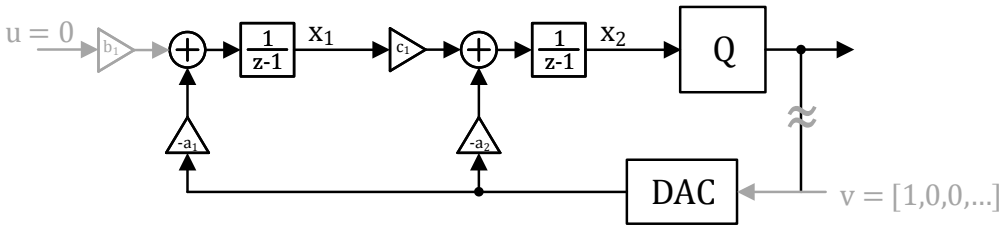

Figure 5.1: Configuration to verify the loop filter. The input of the modulator is set to zero and an impulse is applied to the DAC in open loop configuration.

the output of the comparator in the behavioral model, which is not a valid output level of a binary comparator. Thus, the loop filter check has to be modified. As described in [21], the solution is to perform two simulations, one with an input stream of $v = [+1, -1, +1, -1, +1, ...]$ and one with $v = [-1, -1, +1, -1, +1, ...]$, where a $+1$ in the block diagram is equal to a voltage level of V_{dda} in the behavioral model and a -1 is equal to $0V$ in the behavioral model. Taking the difference between the gained output signals of the two simulations, the response to the impulse train $v = 2\delta[n] = [2, 0, 0, 0, 0, ...]$ can be determined. Thus, the gained result just needs to be divided by 2 to get the desired impulse response. Fig. 5.2 shows the results of the loop filter verification, where the ideal values of the difference equations and the simulated values of the behavioral model are plotted. Additionally, the non-overlapping clock signals and the applied impulse are shown in this figure. As can be seen in the plots of the output signals of the two integrators, the impulse response results of the difference equations and the results of the behavioral schematic are nearly identical and thus, the correct behavior of the loop filter is verified. It should be noted that the coefficients in the difference equations were thereby recalculated to match with the implemented capacitor ratios of the behavioral circuit.

5.1.2 Swing of Internal States

To check that the scaling of the delta-sigma modulator acts as intended, investigations regarding maximum occurring state swings must be done. The maximum values at the output of the integrators should be within the specified amplifier output swings to avoid an overload of the integrators. To check this, the modulator loop needs to be closed and different signals need to be applied at the input of the delta-sigma modulator, while the output signals of the two integrators are captured. The behavioral model was checked for sinusoidal as well as for dc input signals close to the input range maximum and minimum. In all cases, the maximum output levels of the two integrators were within the determined output swing range. Thus, the dynamic range scaling behaves as intended.

5.1.3 Output Spectrum

To conclude the verification section of the delta-sigma modulator, one more closed loop test needs to be done. This check determines the correct generation of the 1-bit output stream regarding the applied input signal. Furthermore, the noise shaping property of the delta-sigma modulator in behavioral form is checked. Therefore, the output stream of

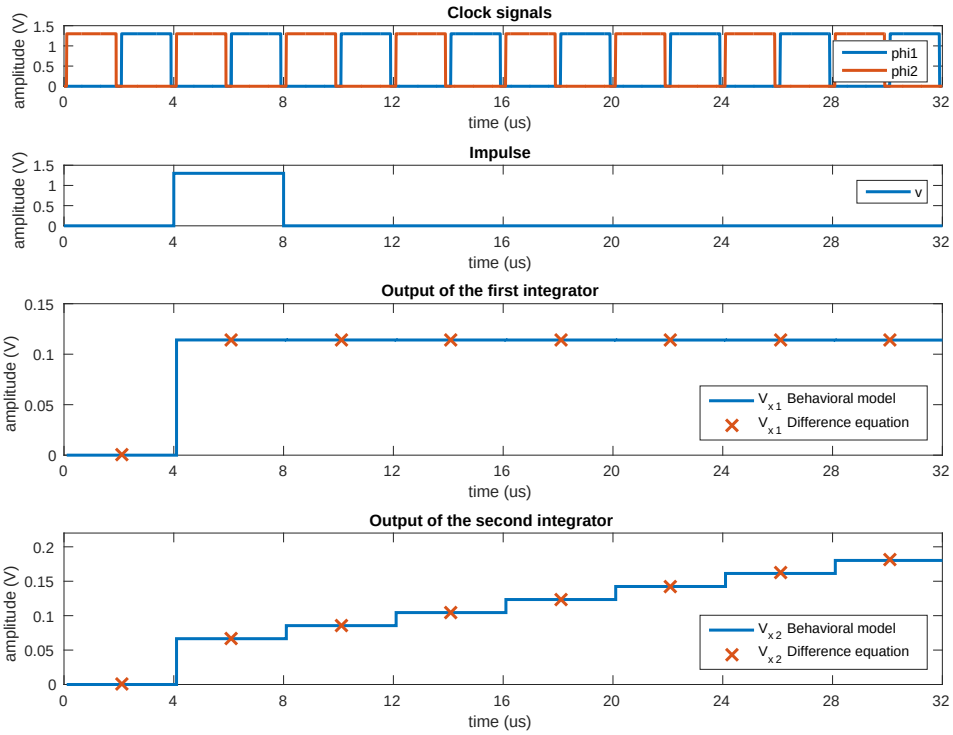

Figure 5.2: Visualization of the loop filter verification results. The upper two plots show the non-overlapping clock signals and the applied impulse. The lower two plots show the output signals of the first and second integrator, where the blue trace presents the result gained form behavioral simulation and the red markers show the values achieved with the difference equations.

the modulator is captured and its discrete Fourier transform (DFT) is determined, which leads to the output spectrum of the modulator.

To achieve accurate results from the DFT, proposals made by Schreier and Temes in [21] were followed. Thus, the number of DFT bins was chosen to $N = 64 \cdot \mathrm{OSR} = 8000$, which leads for the sampling frequency of $f_s = 250kHz$ to a frequency resolution of $31.25Hz$ in the spectrum. To achieve coherent sampling with uniformly distributed quantization noise in the DFT, two conditions must be fulfilled as defined in [44]. The first condition, which is given by

$$f_{in} \stackrel{!}{=} \frac{N_c}{N} \, f_s, \tag{5.1}$$

where N_c is an integer number of captured periods of the sinusoidal input signal, ensures that the input signal with the frequency of f_{in} is exactly located on a frequency bin of the DFT. This condition ensures coherent sampling and thus avoids signal leakage. To ensure a distribution of the quantization noise over all frequency bins of the DFT, condition two given by

$$gcd(N_c, N) \stackrel{!}{=} 1, \tag{5.2}$$

where $gcd(N_c, N)$ stands for greatest common divisor of N_c and N, must be fulfilled. To satisfy this condition, an appropriate number of captured periods of the input signal must be determined. Using $N_c = 17$ periods of the input signal ensures that N_c and N

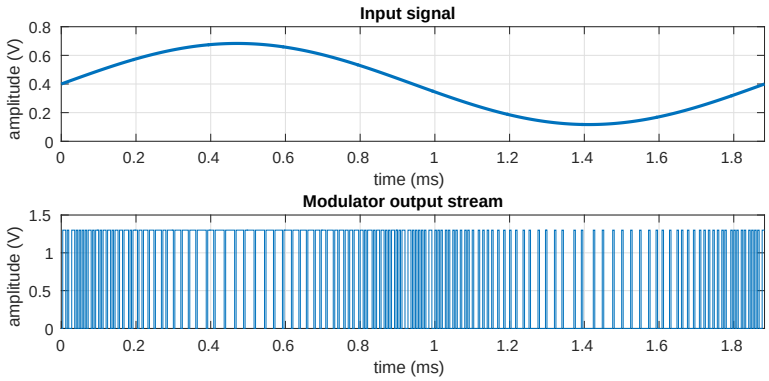

Figure 5.3: One period of the input signal and the delta-sigma modulator output stream for a sinusoidal input signal with an amplitude of $-3dBFS$ and a frequency of $531.25Hz$.

are coprime and hence, fulfill the condition given in (5.2). With the knowledge of the number of periods to be captured, a convenient input signal frequency can be determined. Solving condition (5.1) thus leads to a suitable input signal frequency of $531.25Hz$. To truncate the output stream to the length of 8000 samples, a Hann windowing function was used as proposed in [21], since this windowing function introduces sufficiently low errors through spectral convolution and therefore leads to an accurate spectrum of the delta-sigma modulator output stream.

For the analysis of the output stream, a sinusoidal input signal with an amplitude of $-3dBFS$ and the determined frequency of $f_{in} = 531.25Hz$ was chosen. Fig 5.3 shows the chosen input signal and the gained output stream of the modulator for one period. A first visual inspection of the output stream looks plausible, since for input amplitudes greater than the common-mode input level of $400mV$, the output stream contains more ones than zeros, the opposite is valid for input amplitudes smaller than the common-mode level. Nevertheless, to exactly investigate the output stream, the frequency spectrum of the signal needs to be calculated. Fig. 5.4 shows the determined output spectrum of the modulator output stream. As can be seen in this figure, the input signal is indeed visible at the desired frequency of $531.25Hz$. Using the Cadence calculator, the SNDR of the output stream in the band of interest was determined to $83.2dB$ and hence, the desired SNDR is achieved. In comparing the achieved SNDR with the MATLAB based SQNR simulation results of the block diagram shown in Fig. 3.2, it can be seen that the achieved SNDR is close to the simulated SQNR limit. Thus, it can be postulated that the implemented delta-sigma modulator works as intended.

5.2 Performance Characterization of the Behavioral Model

Since the modulator is now verified against the desired functionality, as a next step the performance characterization needs to be done to ensure that the given specifications for the delta-sigma modulator are fulfilled. Therefore, several tasks will be performed with the behavioral model. The first task is a simulation of the SNDR over changing input signal amplitude, similar as it was done in MATLAB simulations presented in chapter 3. This

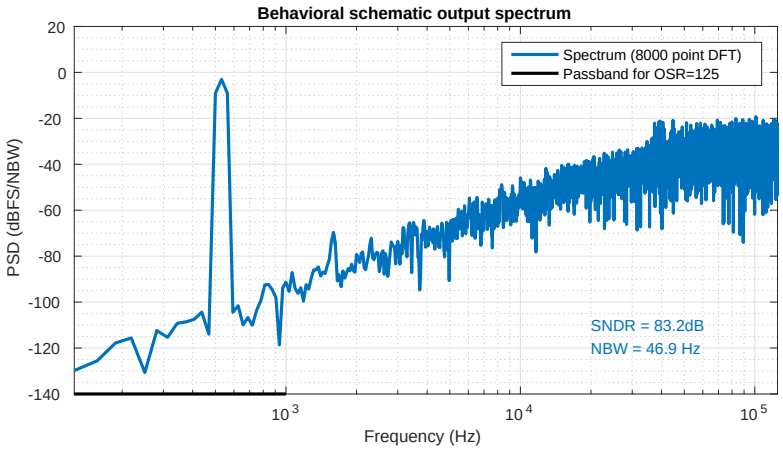

Figure 5.4: Spectrum of the modulator output stream of Fig. 5.3.

characterization test determines the maximum achieved SNDR as well as the dynamic range of the modulator. Afterwards, the SNDR for changing input signal frequency will be investigated. Finally, the offset of the modulator for dc input signals will be simulated. To find the most advantageous configuration as well to find important parameters which determine or limit the performance of the modulator, each test was performed several times with somewhat varied block parameters. The outcome of these characterization tests is a list of finalized specifications for the individual circuit blocks, which lead to a comparable good performance of the modulator while still achieving adequate power consumption.

5.2.1 SNDR for Changing Input Signal Amplitude

The first performance characterization test is the simulation of the SNDR of the delta-sigma modulator for varying input signal amplitude. Therefore, the amplitude of a sinusoidal signal was swept from $-80dBFS$ to $0dBFS$, where a full-scale amplitude is equal to $V_{in_{max}}/2 = 400mV$. For every investigated input signal amplitude, the SNDR of the output stream was calculated using the same settings for the DFT as discussed in section 5.1.3. Thus, the input signal frequency was fixed to $531.25Hz$. The results of this investigation are visualized in Fig. 5.5. Additionally, the required SNDR to fulfill the project specification is plotted in this figure. The results show that the specifications are fulfilled up to the overload level of $-1dBFS$. Compared to the SQNR results determined by MATLAB simulation in Fig. 3.2, the SNDR of the behavioral model is roughly $5dB$ less at every input signal amplitude. Thus, quantization noise is not the only source which limits the achieved SNDR. This indicates that an economical implementation of the modulator was found. Furthermore, the chosen amplifier gain of $40dB$ for each integrator amplifier seems to be high enough with respect to dead bands appearing in the delta-sigma modulator. According to Schreier and Caldwell in [38], the dead band width of a second-order delta-sigma modulator is approximately equal to $\frac{1}{6 \cdot A_1 \cdot A_2} \cdot V_{in,FS}$, where A_1 and A_2 are the dc-gains of the two integrator amplifiers and $V_{in,FS}$ is the full-scale range of the input signal. With a gain of $40dB$ and a full-scale range of $800mV$, this results in a dead band size of $\pm 6.67uV$, which is much less than 1 LSB for the desired

resolution of 10-bits. This leads to a dynamic range of the modulator which is greater than $80dB$. Furthermore, with respect to the required SNDR there is still a margin of roughly $20dB$ in the behavioral simulations, which provides some room for nonidealities in the transistor-level implementation of the behavioral models.

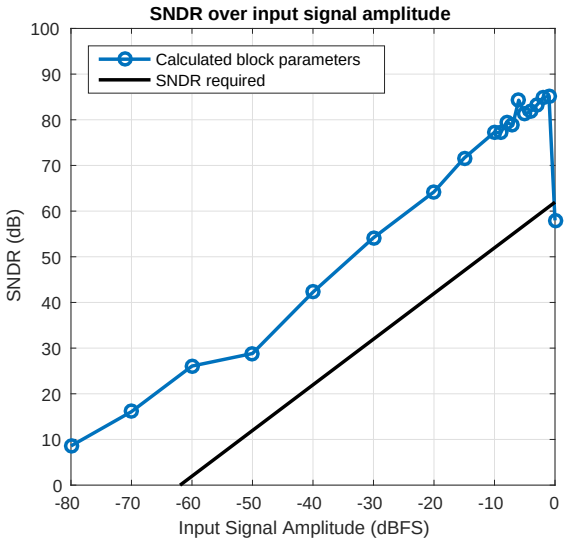

Figure 5.5: SNDR of the behavioral model for changing input signal amplitude. The black trace indicates the project specified SNDR.

5.2.2 SNDR for Changing Input Signal Frequency

A further performance measure for the delta-sigma modulator is the achieved SNDR for changing input signal frequencies in the specified input bandwidth. For this test, the input signal amplitude was fixed to $300mV$ and the input signal frequency was varied from $100Hz$ to $1kHz$. Using the Cadence calculator, the DFT of the output streams was determined and the SNDR for each frequency was calculated. The result is shown in Fig. 5.6. The requirements are exceeded at all frequencies, which again gives some margin for nonidealities in the transistor-level implementation. The attentive reader will have noticed that the achieved SNDR for frequencies less than $500Hz$ is lower than for frequencies greater than $500Hz$. The reason for that are the appearing harmonics of the signal in the modulator output stream. For signals with frequencies less than $500Hz$, the harmonics are located within the band of interest and thus reduce the achieved SNDR. Since the amplitude of the harmonics in the output stream of the modulator are quite small, they do not degrade the performance significantly.

5.2.3 Offset for Dc Input Signals

Since the measurement of static signals is quite important in case the delta-sigma ADC is operated in the *testmode*, the offset of the delta-sigma modulator regarding such input signals was investigated. Therefore, dc signals within the stable input signal range were applied to the delta-sigma modulator and the 1-bit output streams were averaged using

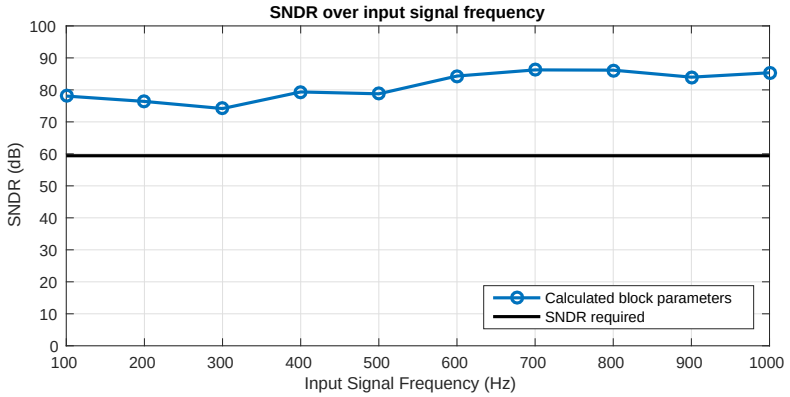

Figure 5.6: SNDR of the behavioral model for changing input signal frequency. The black trace indicates the project specified SNDR.

MATLAB post-processing. Simulations in section 5.2.1 showed that the stable input range of the modulator should be limited to voltage levels less than $-1dBFS$. The simulations performed in this chapter even showed a stable input range up to $15mV$ below full-scale. The result of these simulations is visualized in the blue trace of Fig. 5.7, where the average of the modulator output subtracted with its ideal value is plotted. As can be seen, the offset at the input ranges minimum and maximum is roughly equal to 3 LSB for an assumed resolution of 10-bits, which is a quite huge value. Simulations with varied block parameters showed, that the dc-gain of the integrator amplifiers, which was assumed to $40dB$ for first simulations, causes this offset. Increasing the gain of the amplifiers to $60dB$ leads to the red trace shown in Fig. 5.7. The offset is reduced to roughly one-fourth of the value which was achieved before, thus the offset for dc input signals over the complete input signal range is now less than 1 LSB, which is seen as an acceptable value.

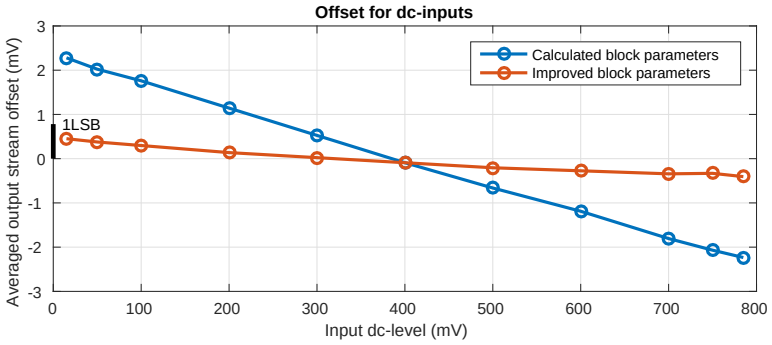

Figure 5.7: Offset of the behavioral model for changing dc input levels. The blue trace shows the result achieved with the calculated block requirements and the red trace shows the result achieved with increased gain in the integrator amplifiers. The marked size of 1 LSB corresponds to an assumed resolution of 10-bits.

The simulations performed in the previous subsections where repeated with the new integrator amplifier gain values, but the changes in the results were negligible, therefore they were not plotted again. Furthermore, simulations showed that the UGF specification of the integrator amplifiers is not that stringed. Even for $UGFs$ as low as $700kHz$, the impact on the performance of the modulator is negligible. Since the calculated value of

$1.25MHz$ seems to be achievable with appropriate current consumption, the specifications for the UGF were not lowered.

After verification and characterization of the delta-sigma modulator on system-level, it can be assumed that the modulator is fully functional for the applications in all the desired modes of operation, while still an appropriate margin to the specified performance is achieved.

5.2.4 Summary of the Circuit Block Specifications

In the previous subsections it was shown that the delta-sigma modulator should fulfill the given project specifications. Thus, this section of behavioral simulations can be concluded in summarizing the finalized parameters and requirements of the individual circuit blocks as well as required reference voltages as shown in Tab. 5.1. The used symbol names are thereby referred to the behavioral schematic shown in Fig. 4.5. The requirements of the comparator are not listed in this table, since these cannot be put into absolute values, as discussed in section 4.3.3.

Block/Component	Parameter	Symbol	Value	Unit
Integrator OTA's ($@C_L = 120fF$)	Dc-gain	A_0	60	dB
	Unity-gain-frequency	UGF	1.25	MHz
	Slew rate	SR	0.15	$V/\mu s$
	Phase margin	PM	≈ 65	deg
	Output swing	–	> 560	mV
Switches	On-resistance	R_{on}	< 5	$k\Omega$
Capacitors	Capacitance	C_1	17	fF
		C_2	119	fF
		C_3	18.5	fF
		C_4	9.25	fF
		C_5	111	fF
Reference Voltages	Voltage	V_{cm}	550	mV
		$V_{ref,hi}$	800	mV
		$V_{ref,lo}$	0	mV
		$V_{cm,ref}$	400	mV

Table 5.1: Determined block and component specifications for the delta-sigma modulator.

Chapter 6

Transistor-Level Implementation

Since a fully characterized and verified behavioral model of the delta-sigma modulator is available, considerations about the implementation using circuit blocks on transistor-level can be made. The idea in the used top-down design approach is to design the blocks one after each other and verify them against their individual specifications. If an individual block got designed and verified against these specifications, it afterwards will be inserted to the behavioral schematic of the delta-sigma modulator, where the functionality of the block will be checked as a part of the modulator. At the end of this chapter, the delta-sigma modulator and all its required additional circuitry will be designed on transistor-level and the complete schematic of the implementation will be shown.

6.1 Implementation of the Circuit Blocks

The design of the circuit blocks on transistor-level will be started with the amplifiers of the two integrators. Beside the basic blocks of a second-order delta-sigma modulator described in section 4.3, there are several more blocks needed. One of those is a circuit to generate the required reference voltages of the modulator. The implementation of this block will be the next task, since it is important to investigate influences produced by the circuits attached to it. Using the designed reference voltage generation circuit, a suitable implementation of the comparator with respect to kickback to the reference generator will be found. If this block is designed, the switches as well as the feedback DAC will be treated. Finally, a circuit which generates the non-overlapping clock signals will be implemented.

Since the delta-sigma modulator should work properly in the specified supply voltage range of $V_{dda} = 1.2 - 1.47V$ and a temperature range of $-40°C$ to $+125°C$, the specification of each circuit block must be fulfilled in these ranges. To check this, corner and Monte Carlo simulations within these ranges will be performed for the designed blocks to guarantee correct functionality in all desired operating conditions.

6.1.1 Integrator Amplifier

The most important block of a delta-sigma modulator is the amplifier of the input integrator, since it determines the noise and distortion performance of the modulator [13]. There are several constraints for this amplifier, which were discussed in detail in section 4.3.2. A main requirement is the amplifier dc-gain in order to provide a good noise shaping property and, as shown in section 5.2.3, a good offset behavior for dc input signals. Characterizations of the transistors in the used CMOS process showed, that a single transistor can provide a gain of roughly $30dB$. Thus, at least two amplifying transistors are needed to achieve the desired dc-gain of $60dB$. Furthermore, the required output swing of $560mV$, determined by the chosen dynamic range scaling, must be provided by the amplifier. Since a low power consumption is a major constraint of the modulator, inverter based amplifiers were investigated. Publications of such amplifiers used in delta-sigma modulators were found in [2] and [17], but it turned out that it is quite difficult to design a PVT stable, inverter based amplifier. Several methods like semi constant current biasing and constant g_m biasing are discussed in [45] to improve the PVT stability of these circuits. Nevertheless, traditional OTA implementations seem to be more stable with respect to PVT variations. Since the delta-sigma ADC should be used for temperature measurements, the advantage of the higher PVT stability outweighs the drawback of the higher current consumption and therefore, an OTA implementation of the integrator amplifier was chosen. Literature studies showed, that a folded-cascode OTA is a quite common choice for those amplifiers in discrete-time integrators, since it achieves similar gain as two stage amplifiers and additionally provides a larger output swing as other single stage amplifiers with comparable gain [13, 20]. Thus, a folded-cascode OTA was chosen for the implementation of the integrator amplifiers. The schematic of the designed OTA is shown in Fig. 6.1.

To minimize the flicker noise of the amplifier, a structure with a PMOS input pair M_1 and M_2 was chosen, since PMOS transistors typically produce less flicker noise than their NMOS counterparts [23]. The drawback of the higher current consumption of this structure was minimized by using the amplifying transistors in the sub-threshold region. Since the transconductance of transistors in this operating region is directly proportional to the current flowing through their channel, the UGF could easily be set to the desired value by adjusting the bias current. The dc-gain of the amplifier, which is given by

$$A_0 = g_{m_{1,2}} \cdot R_{out} \tag{6.1}$$

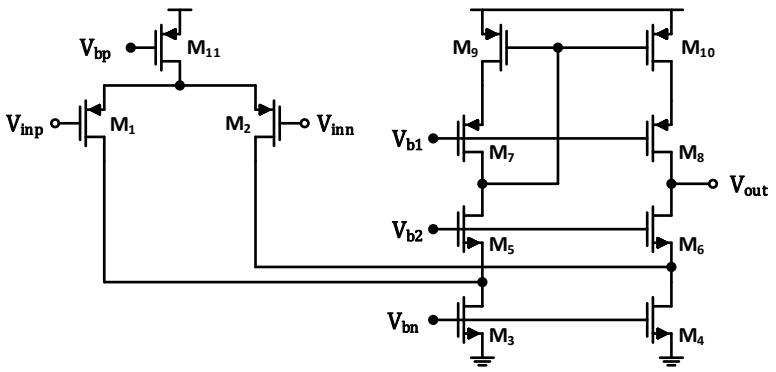

Figure 6.1: Folded-cascode OTA used for the discrete-time integrators.

could afterwards be set by adjusting R_{out} to an appropriate value. R_{out} is thereby referred as the output resistance of the folded-cascode OTA. With this design approach, the optimum performance regarding dc-gain and UGF with respect to minimum power consumption could be found. Using the cascode transistors $M_5 - M_8$ in weak inversion, provides a high output resistance and additionally maximizes the available output swing of the amplifier, in case the bias voltages V_{b1} and V_{b2} are chosen appropriate. To provide good matching and hence low offset in the amplifier, the current sources M_3, M_4 and M_{11} as well as the current mirror M_9/M_{10} are operated in strong inversion with a convenient gate overdrive. To generate the required bias voltages of the amplifier, a bias circuit as shown in Fig. 6.2, was designed. Using this configuration of the bias generator ensures proper operation of the amplifier within the specified supply voltage range and an appropriate rejection of power supply noise in the amplifying circuit. The generation of the required reference current I_{ref} will be discussed in section 6.2.

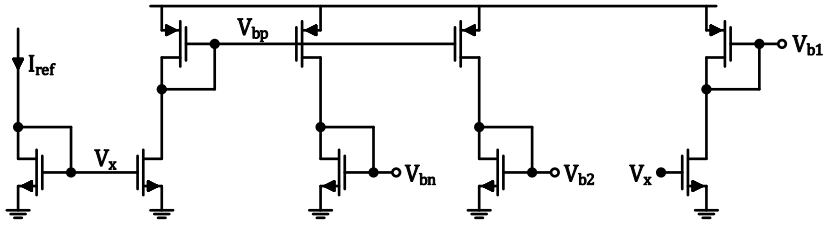

Figure 6.2: Integrator amplifier bias circuit.

Nominal simulations of the designed amplifier showed a dc-gain of $67.8dB$, a UGF of $1.6MHz$ and a PM of $73.7°$ at a load capacitance of $120fF$, while just consuming $380nA$ from a $1.3V$ supply. Corner and Monte Carlo simulations showed, that the required specifications listed in table 5.1 should be fulfilled in all project mandatory corners, even if process and mismatch variations are considered. The minimum available output swing was determined to $600mV$, reaching from $250mV$ to $850mV$ at the minimum specified supply voltage. Out of these simulations, the most advantageous common-mode level of the amplifier was therefore determined to $V_{cm} = 550mV$, as betrayed earlier. The SR of the implemented amplifier is approximately $0.7V/\mu s$ at a load capacitance of $120fF$.

The requirements for the second integrator of the delta-sigma modulator are not that stringed compared to the first integrator, since nonidealities associated with it are already suppressed by the gain of the first integrator. Thus, the requirements of this amplifier could be reduced [21]. Since the current consumption of the designed integrator is already quite low, this shrinking of the requirements was not done, since the greater effort in doing two different layouts outweighs the marginal reduction of the current consumption. Furthermore, the same physical bias circuit can be used for both integrator amplifiers, which reduces the required area consumption.

As discussed, the designed amplifier satisfies the derived specifications listed in table 5.1. As a next step, the amplifier was inserted to the behavioral circuit of the delta-sigma modulator, where it replaced the two ideal amplifiers of the integrators. To verify that the delta-sigma modulator even operates properly with these real amplifiers, the three performance characterization tests described in section 5.2 were done. These simulations showed that the delta-sigma modulator using the designed folded-cascode OTAs for the two integrators behaves similar as the circuit with the ideal amplifiers. Thus, the implemented

OTA seems to be convenient for the discrete-time integrators of the delta-sigma modulator.

6.1.2 Reference Voltage Generation

The next block which was implemented is the circuit which provides the required reference voltages for the delta-sigma modulator. The available bandgap reference of the chip offers a trimmed reference voltage of $800mV$, as well as voltages in $10mV$ steps below this reference voltage, generated by a resistor ladder. As shown in Tab. 5.1, beside the available reference level of $0V$, reference voltages of $400mV$, $550mV$ and $800mV$ are needed for the operation of the delta-sigma modulator. To use a voltage from the bandgap reference, the voltage needs to be buffered to avoid a loading of the bandgap circuit. Thus, there are several important requirements for a unity-gain buffer attached to the bandgap circuit to provide a reference voltage. First, it should have high enough dc-gain to keep the error due to the feedback configuration of the amplifier in an acceptable range for the delta-sigma modulator. Furthermore, it must withstand kickback from circuits attached to it. That means, it must be fast enough and has to provide high enough slew rate, to do not excessively disturb the performance of circuits attached to it. A third very important constraint for the buffer is a low kickback property to its input, since the input is directly attached to the resistor ladder of the bandgap circuit and a kickback to the last is strictly forbidden. Two possibilities were investigated to provide the reference voltages for the delta-sigma modulator. The first possibility is shown on the left side of Fig. 6.3, where three separated unity-gain buffers are used to provide the required reference voltages for the delta-sigma modulator. The second possibility which was investigated is shown on the right side of Fig. 6.3, where just one reference voltage is taken from the bandgap resistor ladder and all other required reference voltages for the delta-sigma modulator are generated locally.

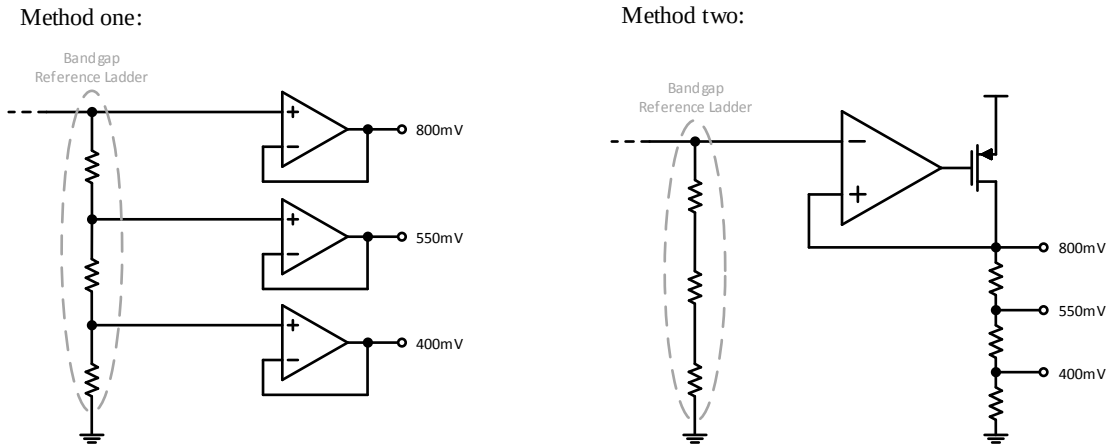

Figure 6.3: Investigated methods to generate the required reference voltages. In the method shown on the left side of the picture, each required reference voltage is taken from the available bandgap reference ladder. The method on the right side just uses one reference voltage from the bandgap reference ladder and generates the required reference voltages locally.

Since it was not clear in the beginning which one the better method witch respect to the

above mentioned requirements will be, both of them were treated in further investigations. As an amplifier for both of these methods, a folded-cascode OTA was used due to its high achievable dc-gain and its comparable good resistance against kickback to the input transistors, provided by the cascode stages. Investigation of the first method showed, that either a rail-to-rail input structure of the folded-cascode OTA or two different folded-cascode OTAs, one with an NMOS input pair and one with an PMOS input pair, would be needed to process the desired reference voltages. Using a rail-to-rail input structure would lead to a higher current consumption and additionally to a variable open loop gain for the different input voltages [41]. Using two different amplifiers for the generation of the desired reference voltages would lead to a higher effort in doing the layout of the modulator. The second method, which locally generates the required reference voltages, uses just one reference voltage from the bandgap circuit. With an additional stage at the output of the folded-cascode OTA, the desired reference voltages are generated on a local reference ladder. The big advantage of this method is that just one connection to the bandgap circuit is required, which makes the top-level layout design easier and additionally increases the reusability and adoption of the reference voltage generation circuit. The drawback of this method is, that either a high current or a high ohmic resistor ladder is required to generate the reference voltages. For example, a chosen total resistance of $800k\Omega$ would lead to a current of $1\mu A$ flowing through the output branch of this implementation to generate the reference voltage of $800mV$.

Investigations on the rail-to-rail input circuit of method one and the circuit of method two showed, that the total current consumption of both methods are nearly identical, since each buffer of method one requires a quite high bias current to provide an appropriate SR to withstand kickback from circuits attached to it. Furthermore, the achievable dc-gain of method two is higher due to the second stage of the amplifier. The second stage additionally reduces the kickback to the input transistors, which is another big advantage. Moreover, the second stage provides the possibility to implement buffer capacitors at the output nodes of the reference ladder very are efficient using well-capacitances. Thus, quite high capacitances can be used for method two to stabilize the generated reference voltages, which further reduces the kickback to the input. The use of well-capacitances for method one is not possible, since the ohmic component of those capacitors would eliminate the gain of the single stage amplifier. Summarizing all the mentioned points, method two seems to be the better choice for the generation of the required reference voltages and was therefore chosen for the implementation in this thesis.

The implemented amplifier for the generation of the reference voltages is shown in Fig 6.4. As already mentioned, the amplifier consists of a folded-cascade OTA ($M_1 - M_{11}$) with a second stage provided by the transistor M_{14} and a resistive reference ladder. The purpose of the stage generated by the transistors M_{12}/M_{13} and capacitor C_c will be explained in a few lines. Since the input level of the amplifier in unity-gain configuration is $800mV$, a NMOS input pair consisting of transistors M_1 and M_2 was chosen. To provide high gain in the first stage, the input pair as well as the cascode transistors $M_5 - M_8$ are operated in weak inversion. The transistors operating as current sources or current mirrors are operated in strong inversion to improve accuracy. The total resistance of the output ladder was chosen to $800k\Omega$. Operating the circuit in unity-gain configuration, which forces the output node to the input level of $800mV$, leads to a current of $1\mu A$ flowing through the output stage of the amplifier. The choice of this resistor value provides an acceptable compromise between arising area and current consumption. Due to a series connection

of 80 equally sized unit resistors, reference voltages in $10mV$ steps are provided by the circuit. Nevertheless, the buffer consumes roughly half of the allowed current for the delta-sigma modulator. Due to the possible reusability and usability of the reference voltage generator for other blocks on the chip, this high value was accepted. Since the amplifier has two stages, a compensation of the circuit is required to provide unity-gain stability. Inserting a Miller-Capacitor between the output node of the first stage and the output node of the second stage showed a very low power supply rejection ratio (PSRR) of the amplifier, which is not acceptable for a reference voltage generator. Thus, a method to improve the PSRR published by Blakiewicz in [46] was used. This approach compensates the amplifier by adding an additional stage, provided by the transistors M_{12} and M_{13} and using the Miller effect with the amplifying transistor of this stage. Noise from the power supply coupled via the compensation capacitor C_c thus disturbs only the node of this additional stage rather than the output node of the reference voltage generator. The required bias voltages for this circuit were again generated using diode connected loads, similar as it was done for the integrator amplifiers.

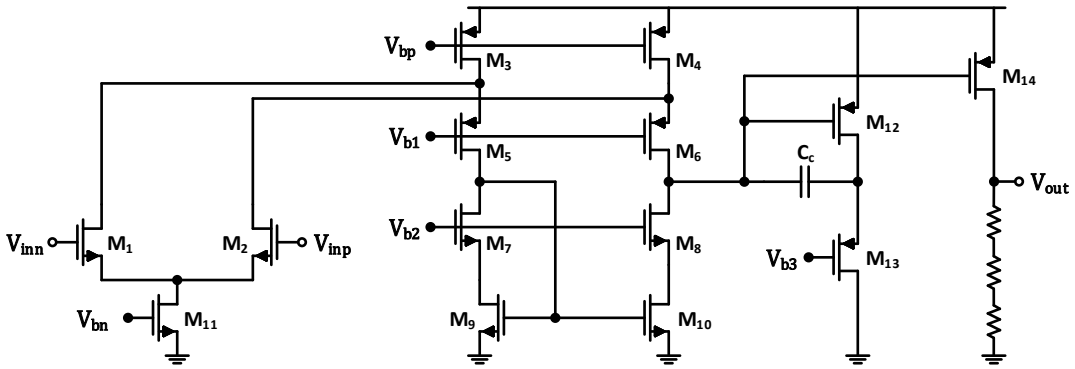

Figure 6.4: Transistor-level implementation of the reference voltage generator.

Simulation results of the amplifier at the nominal corner showed an open-loop gain of $91.9dB$, a UGF of $793kHz$ and a phase margin of 72.1° for n-well load capacitances of $750fF$ at each of the used reference voltages nodes. The total current consumption of the voltage buffer was simulated to $1.07\mu A$. Corner and Monte Carlo simulations showed, that the implemented voltage buffer should operate as desired in all predictable operating conditions. The maximum occurring deviation of the generated reference voltages from their ideal values was determined to less than 3% using a 1800 point Monte Carlo simulation. To check if this variance is acceptable, the designed reference voltage generator was inserted to the behavioral model of the delta-sigma modulator. Simulations performed on the behavioral model showed a negligible impact on the performance of the modulator due to the replacement of the ideal reference voltage sources with the designed reference voltage generator, hence this occurring deviation was treated as acceptable.

6.1.3 Comparator

The transistor-level implementation of the delta-sigma modulator was continued with the latched comparator. As discussed in section 4.3.3, the requirements for the comparator are not that stringed since most nonidealities are suppressed by the noise shaping property of the delta-sigma modulator.

There are several possibilities to implement the latched comparator in discrete-time delta-sigma modulators. The fundamental operation of latched comparators can be subdivided into two phases. One phase is called the reset phase, where both outputs of the comparator are pulled to a certain voltage, regardless of the input voltages applied to the comparator. In the second phase, which is called regeneration phase, the circuit actually operates as comparator and pushes its outputs in a certain direction, depending on the voltages applied to the input transistors of the comparator. Usually, such latched comparators use a cross-coupled pair and the positive feedback associated with it, to achieve a high gain in this phase. A very simple circuit with one cross-coupled pair was used by Lopez-Morillo et al. for a second-order delta-sigma modulator presented in [31]. An additional preamplifier to minimize the offset of the comparator was used by Sandhya in [47]. Both referred implementations operate with a constant bias current. Since a current in latched comparators is just needed at the point of time where a decision has to be made, most of the current flowing through such comparators is wasted. Therefore, Chae and Han used a different kind of a latched comparator in [17], the so called StrongArm latch, which does not require a static current consumption for its operation. A current is only flowing in case a comparison has to be made. A drawback of such circuits is the occurring current peak at the transition between the two phases, which can be quite distinctive, since the current is not controlled by a constant bias source [48].

All the previously mentioned comparator implementations fulfill the requirement of a low hysteresis, since in the reset phase both output nodes are either pulled to the positive or negative supply rail. Investigations showed, that a preamplifier is not required for the implementation of the comparator for this thesis, since the disadvantage of an increased current consumption outweighs the advantage of a lower offset. Furthermore, a circuit without static current consumption is preferred to an implementation with a static current flowing through the comparator, since a low power consumption is a main constraint for the delta-sigma modulator to be implemented. Nevertheless, simulations showed that the StrongArm latch used in [17] produces a high kickback to the inputs of the comparator and hence a not negligible distortion of the generated reference voltages, which leads to a performance reduction of the delta-sigma modulator. To improve this situation, a lower kickback configuration of the StrongArm latch was used by Roy and Barker in [30]. Simulations showed that this configuration reduces the kickback by roughly 60% compared to the original version of the StrongArm latch, with the drawback of a somewhat lower gain and increased offset. Since the gain of this structure is still high enough for an appropriate metastability range, this is no problem for the desired application of the comparator in the delta-sigma modulator. Furthermore, since offset of the comparator is of minor concern, the StrongArm latch in lower kickback configuration, which is shown in Fig. 6.5, seems to be the best choice for this thesis and was therefore selected for the implementation of the comparator. To get a valid output signal even in the reset phase, the latched comparator is followed by a SR latch, which is also shown in this figure.

To optimize such comparator designs, small transistor dimensions are used to achieve fast decisions. But small transistors tend to mismatch and hence nonideal effects like an increased offset of the comparator. Furthermore, to achieve a high gain in the regeneration phase, the amplifying input transistors as well as the cross-coupled transistors should be designed properly to achieve high g_m. Since the input pair of the StrongArm comparator in lower kickback configuration is operating in triode region while amplification [48], there is a trade-off in increasing the size of the input transistors, because the gate drain

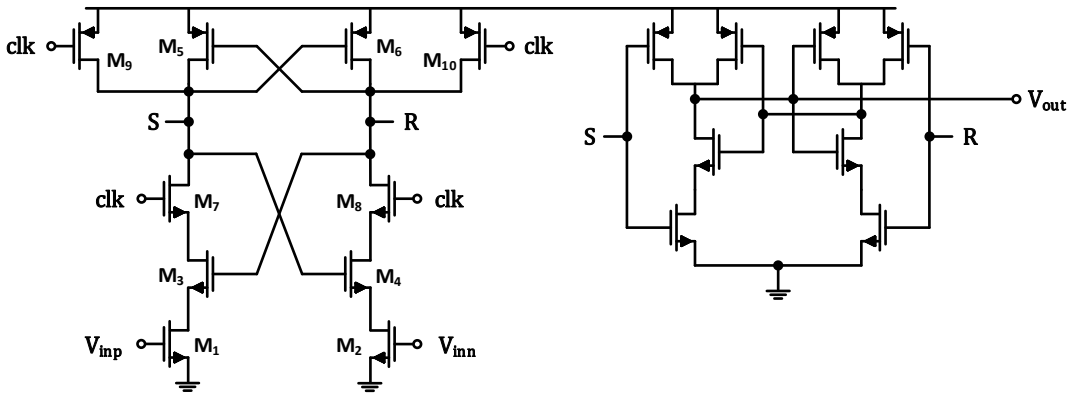

Figure 6.5: StrongArm latch in lower kickback configuration followed by a SR latch.

capacitance C_{gd} in the triode region is proportional to the area of the transistor [22] and hence, increasing the size of those transistors lead to an increased susceptibility to kickback. Furthermore, wide transistors M_3/M_4 and M_7/M_8 are of advantage to reduce the increased offset due to the input pair operating in triode region [48]. As can be seen, there are a lot of compromises to deal with in the design of the comparator. With the help of circuit simulations, a suitable configuration of the comparator could be found. The implemented comparator can resolve input voltage differences as small as $1mV$ within $15ns$ at the nominal corner, while just consuming an average current of $70nA$ per decision for a load capacitance of $100fF$. A 1800 point Monte Carlo simulation showed a maximum input referred offset of the comparator equal to $\pm 8mV$. To verify the functionality of the implemented comparator as part of the modulator, the circuit was inserted to the behavioral model. Simulations showed similar performance of the modulator as for the circuit with the comparator in behavioral form. The kickback of the comparator to the resistor ladder of the reference voltage generator was determined to $8mV$, which is an acceptable value verified by the performance characterization tests of the modulator. Corner and Monte Carlo simulations of the modulator confirmed adequate performance of the implemented comparator in all desired operating conditions, thus a convenient implementation was found.

6.1.4 Switches

To conclude the transistor-level implementation of the discrete-time integrators, the switches need to be implemented. As determined in section 4.3.4, the on-resistance of the switches should be less than $5k\Omega$ and ideally constant over the complete input voltage range. Switches in a CMOS process are usually implemented using transistors in the linear region. Referred to a certain gate level of the transistor, a NMOS transistor is a good switch for low input voltages, whereas the PMOS transistor is a good switch for high input voltages. Since for the implemented delta-sigma modulator voltages close to the complete supply voltage range can appear at the input of the switches, a single transistor is not convenient for their implementation. Thus, transmission gates must be used.

A transmission gate consists of a parallel connection of a NMOS and a PMOS transistor, thereby providing a relatively constant on-resistance over the complete input voltage

range. To reduce the on-resistance of MOSFET switches, the aspect ratios W/L of the used transistors need to be increased. Unfortunately, there are also nonideal effects associated with MOSFET switches. A first nonideal effect which appears in switched-capacitor networks is the kT/C-noise, which is held in the sampling capacitors when the switch opens. This nonideal effect, which does not dependent of the on-resistance of the switch, was already discussed in section 4.3.1 and appropriate values for the sampling capacitors were calculated therefore. Another nonideal effect is called clock feedthrough, where the control signal of the switch couples through the gate-drain and gate-source overlap capacitance to the sampling capacitor, thereby introducing an error voltage to the sampling capacitor [49]. A further nonideality of a MOS switch is called charge injection. When the switch turns off, the charge stored in the channel splits up equally and gets pushed out through the drain and source terminals of the switch, thereby introducing an error voltage to the attached sampling capacitor [41]. The error voltage introduced to the capacitor is directly proportional to the area of the transistor [41]. Thus, there are trade-offs in choosing an appropriate W/L ratio to achieve the desired on-resistance, while holding errors associated with it small. The effect of charge injection can be reduced by adding dummy transistors, which are clocked inversely to the real switch, at the two channel terminals of the switch. Thus, the charge flowing out of the switch terminals gets absorbed by these dummy transistors, which reduces the charge injected to the sampling capacitor. Fig. 6.6 shows such an implementation of the transmission gate, which correspond to the implemented switches for this thesis.

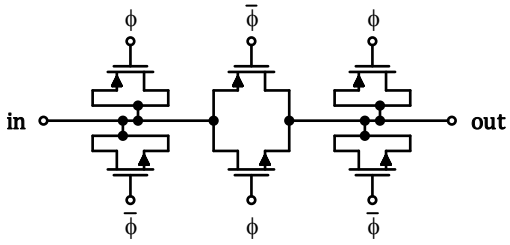

Figure 6.6: Transmission gates with dummy transistors.

Simulations showed, that an aspect ratio W/L of approximately 5 for the NMOS transistor and 7 for the PMOS transistor are needed to generate an on-resistance which is lower than $5k\Omega$ over all corners. The channel length L of the transistors was thereby chosen to an appropriate value to achieve a good trade-off between nonidealities associated with the area of the transistor and nonidealities appearing due to leakage currents of short channel devices. Since the charge stored in the channel splits up approximately equal at switch-off, the width of the dummy transistors was chosen to half the value compared to the width of the switching transistors. Corner simulations of the implemented switch showed a worst-case error voltage of $10mV$ injected into a $20fF$ capacitor when the transmission gate is switched off. Verification in the system-level model of the modulator showed that this error voltage is acceptable and does not degrade the performance of the delta-sigma modulator excessively.

6.1.5 Feedback DAC

To close the loop of the delta-sigma modulator, the transistor-level implementation of the feedback DAC needs to be done. As discussed in section 4.3, since the output of the modulator is just a 1-bit signal, the feedback signal also has just two levels. Therefore, logic gates can be used to implement the DAC, which control the switches in the feedback path. Since the switches are realized as transmission gates, also the inverse of the control signals need to be generated. This was done by adding two additional NAND gates to the feedback DAC, which generate the complementary signal as can be seen in Fig. 6.7. To avoid distortions due to delays between the complementary control signals of the switches, all used gates are custom designs rather than components from a digital library. Thus, the propagation delays of the AND and NAND gates were adjusted to be similar. Again, after individual verification, the behavioral model DAC was replaced with the designed transistor-level DAC, where the performance as part of the modulator was checked.

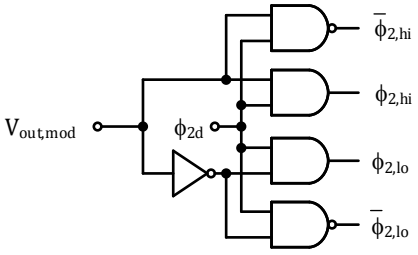

Figure 6.7: Feedback DAC.

6.1.6 Non-Overlapping Clock Generator

To complete the transistor-level implementation of the delta-sigma modulator, a circuit which generates the required clock signals needs to be designed. As explained in section 4.3, a two-phase non-overlapping clock signal (ϕ_1, ϕ_2) as well as the inverse of this clock ($\overline{\phi}_1$, $\overline{\phi}_2$) are needed for the operation of the switched-capacitor integrators. For further reduction of the signal dependent charge injection, the delayed clock signals (ϕ_{1d}, ϕ_{2d}) and again their inverse ($\overline{\phi}_{1d}$, $\overline{\phi}_{2d}$) are needed, to control the transmission gates on the signal conducting side of the switched-capacitor networks. For the implementation of the clock generator of the delta-sigma modulator, a circuit proposed by Schreier and Temes in [21] was modified to additionally create the complementary control signals for the transmission gates. A schematic of the implemented circuit is shown in Fig. 6.8. All used gates are again custom designs, which provides independence of the delta-sigma modulator to upcoming changes in the digital process data and further increases the reusability of the modulator. Applying a clock signal with a duty cycle of 50%, the designed circuit generates signals as shown in Fig. 6.9. Additionally, the inverse of all those signals is generated. The implemented clock generator was then added to the system-level model, where correct functionality of the delta-sigma modulator including the clock generator was checked.

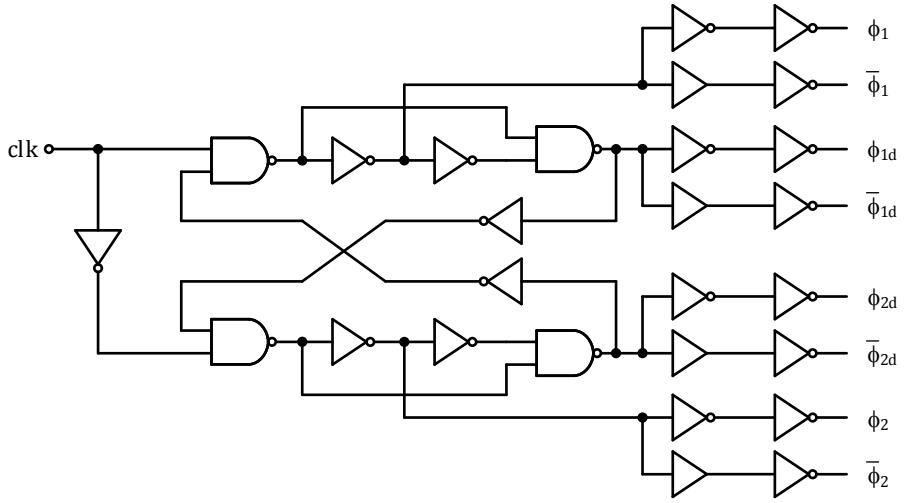

Figure 6.8: Non-overlapping clock generator.

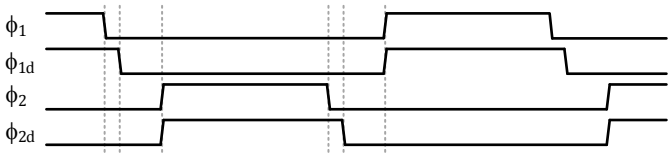

Figure 6.9: Clock signals provided by the implemented clock generator. Additionally, the inverse of all these signals is generated to control the transmission gates.

6.2 Block-Level Schematic of the Delta-Sigma Modulator

Since all the main blocks of the delta-sigma modulator are designed and verified against their individual specifications as well as a part of the modulator, considerations about required additional circuitry for the system integration can be made. This includes the adoption of an available clock signal on the chip to the desired frequency of $250kHz$ and the generation of the required reference currents for the modulator. Fig. 6.10 shows the complete block-level schematic of the delta-sigma modulator, where the implemented circuit blocks discussed in the previous section as well as the additional circuitry, which will be discussed in this section, are combined.

As mentioned in section 6.1.1, reference currents are necessary to generate the required bias voltages of the implemented amplifiers. The existing bias generator of the chip provides a trimmed reference current of $50nA$. This reference current was used in a local biasing scheme, to generate the required currents for the amplifier biasing circuits. To provide high accuracy, comparable big transistors as well as a high gate overdrive was used for the current mirrors. This local biasing scheme, which uses the current rather than the gate to source voltage as an information parameter, provides a very accurate reference current for the delta-sigma modulator, regardless of the distance between the on-chip bias generator and the delta-sigma modulator in future silicon implementations of the design. Furthermore, this scheme is much less susceptible to coupling of disturbances to the gate-source voltage of the on-chip bias generator, since a long routing of the bias generator gate trace is avoided. Thus, the advantages associated with it outweighs the

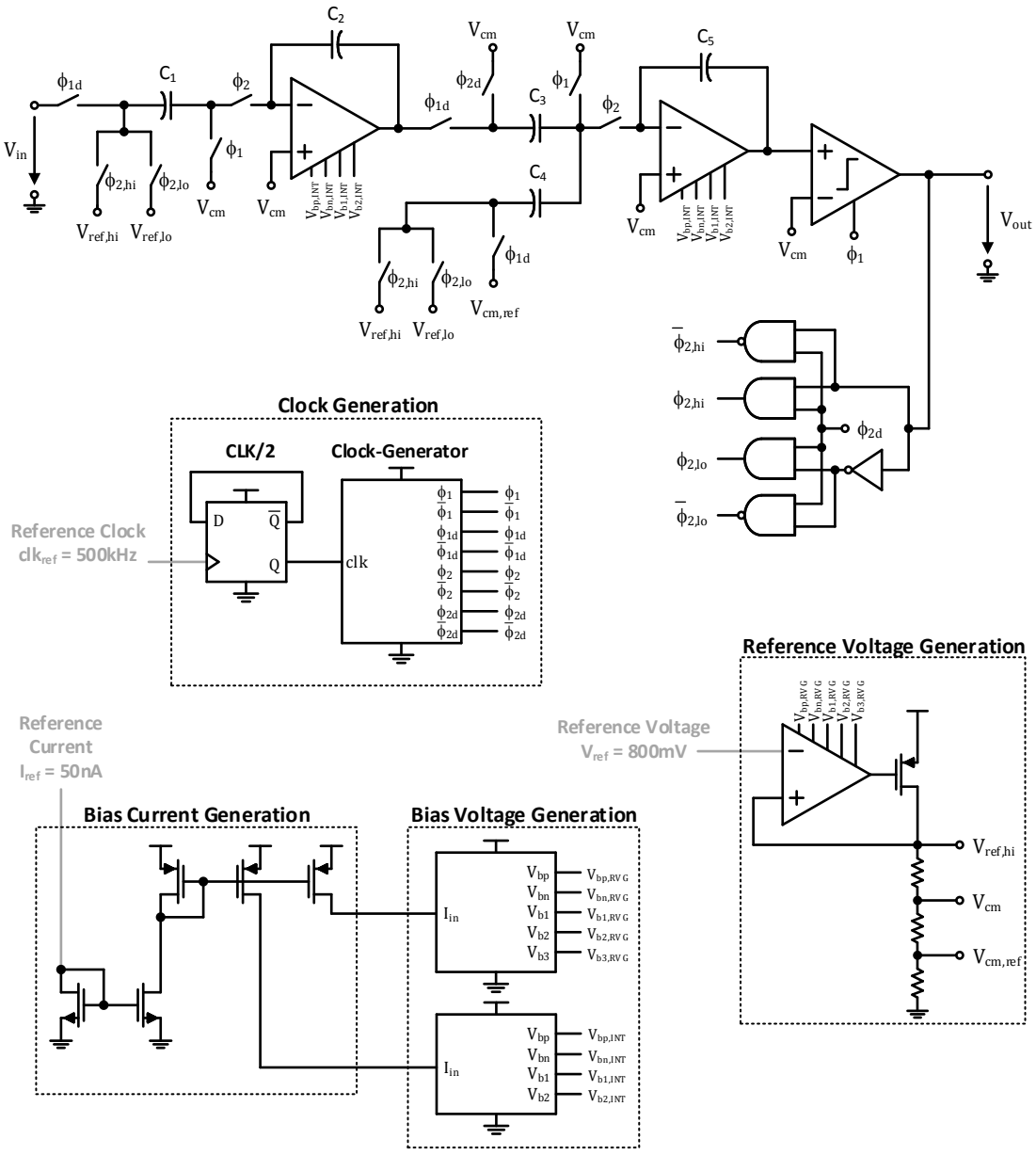

Figure 6.10: Schematic of the delta-sigma modulator. For simplicity, circuit blocks discussed in section 6.1 are represented as black boxes.

disadvantage of a somewhat higher current consumption. As shown in the schematic of the delta-sigma modulator in Fig. 6.10, the generated currents are then connected to the bias voltage generation circuits discussed in section 6.1.1, which are for simplicity drawn as black boxes in this figure.

To generate the non-overlapping clock signals using the implemented clock generator, a reference clock signal with a frequency of $250kHz$ is required. The existing circuitry of the chip provides a clock signal with a frequency of $500kHz$ and a duty cycle of 50%. To generate the required $250kHz$ clock signal for the delta-sigma modulator, this reference clock simply needs to be divided by a factor of two. This can be done by using a D-

flip-flop, where the negated output is connected to its data input and the reference clock signal with the frequency of $500kHz$ is applied to the clock input of the flip-flop. This configuration provides a clock signal with a frequency of $250kHz$ and a duty cycle of 50% at the output of the flip-flop. Since a D-flip-flop especially designed for this purpose is already available for the used process, this circuit was reused.

For completeness it should be mentioned that the two amplifiers of the integrators drawn in Fig. 6.10 contain the circuit discussed in section 6.1.1, the simplified symbols for the switches represent the implemented transmission gates of section 6.1.4 and the symbol of the comparator stands for the circuit of Fig. 6.5. Furthermore, the used symbol for the reference voltage generation block actually depict the circuit shown in Fig. 6.4. To minimize the current consumption in power-down mode, appropriate power down control circuits were implemented, which are not shown in Fig. 6.10.

To conclude this section, the interfaces of the delta-sigma modulator are summarized in Tab. 6.1, since they are important for the system integration. This table lists up all the inputs and outputs of the delta-sigma modulator as well as their required signals.

Name	Symbol	Direction	Value	Unit
Modulator input	V_{in}	in	$15 - 785$	mV
Reference voltage	V_{ref}	in	800	mV
Reference current	I_{ref}	in	50	nA
Clock signal	clk_{ref}	in	500	kHz
Power-down	PD	in	0 or V_{dda}	V
Modulator output	V_{out}	out	0 or V_{dda}	V

Table 6.1: Interfaces of the delta-sigma modulator.

Chapter 7

Performance Characterization and Comparison

All blocks of the second-order delta-sigma modulator are implemented on transistor-level and additional circuitry are designed that the modulator can be used in future NXP Semiconductors products. To ensure that the implemented modulator fulfills project related requirements, a performance characterization must be done. The results of the characterization will be compared to the results gained from the behavioral model. Furthermore, a comparison of the implementation with recently reported designs based on a FOM will be done in this chapter. The required area of the delta-sigma modulator will be estimated. Finally, an overview of the implemented delta-sigma modulator will be given and the convenience for the application in smart temperature sensors will be discussed.

7.1 Performance Characterization of the Implementation

To compare the performance of the transistor-level circuit with the behavioral model of the delta-sigma modulator, the same performance characterization tests were done as discussed in chapter 5. Only results of nominal simulations will be shown, since these can be compared with the simulation results of the behavioral model. Since the modulator needs to be fully functional in all specified operating conditions, corner and Monte Carlo simulations were additionally performed, to ensure a high yield in future silicon implementations of the modulator. These simulations, which ensure proper performance in all operating conditions, will be discussed at the end of this section.

7.1.1 Output Spectrum

To ensure that the loop filter and hence the noise shaping of the implemented delta-sigma modulator performs as intended, the output spectrum of the modulator for sinusoidal input signal with an amplitude of $-3dBFS$ and a frequency of $531.25Hz$ was simulated and compared to the results gained form the behavioral model. Fig. 7.1 shows both gained spectra. As can be seen, the spectrum of the transistor-level implementation looks similar to the spectrum of the behavioral model. Nevertheless, to ensure proper operation of the

modulator, performance characterizations for other input signals must be done, which will be treated in the following sections.

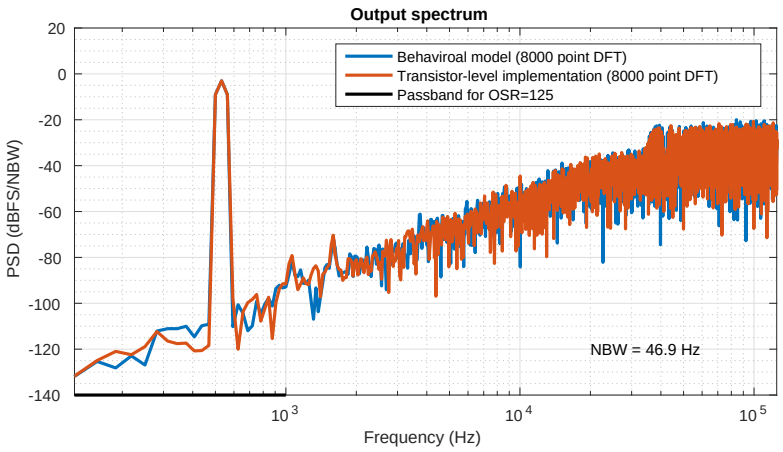

Figure 7.1: Comparison of the output spectra of the behavioral model and the transistor-level implementation for a sinusoidal input signal with an amplitude of $-3dBFS$ and a frequency of $531.25Hz$.

7.1.2 SNDR for Changing Input Signal Amplitude

The first performance measure is the determination of the SNDR for varying input signal amplitudes. The simulation of the delta-sigma modulator and post-processing of the 1-bit output stream to determine the achieved SNDR gave the result shown in Fig. 7.2, where the gained SNDRs for both, the behavioral model and the transistor-level implementation are plotted. In both cases, the input signal frequency was fixed to $531.25Hz$. As can be seen, the performance achieved with the transistor-level implementation is comparable to the results of the behavioral model simulations. The peak value of the SNDR is equal to $86.9dB$, achieved at an input signal amplitude of $-2dBFS$. The maximum stable input signal amplitude is equal to $-1dBFS$. With linear extrapolation of the plotted trace, the dynamic range of the implemented modulator can be estimated to $88dB$.

7.1.3 SNDR for Changing Input Signal Frequency

As a next performance measure, the SNDR of the implemented delta-sigma modulator for changing input signal frequency was determined and compared to the achieved values of the behavioral model. As visible in Fig. 7.3, there is roughly no difference in the achieved SNDR ratios between the behavioral model and the transistor-level implementation of the modulator. For low input signal frequencies, the achieved SNDR is again somewhat lower as for higher input signal frequencies, since harmonics appear in the band of interest. But, the achieved SNDR exceeds its desired values at all treated input signal frequencies.

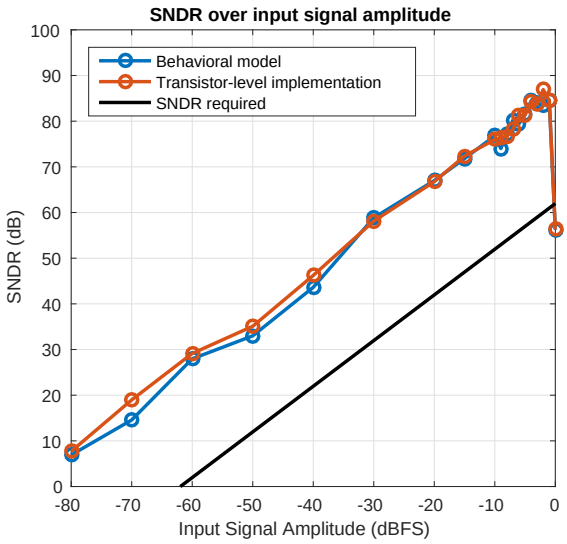

Figure 7.2: Comparison of the achieved SNDR for changing input signal amplitude in the behavioral model and the transistor-level implementation of the modulator. The black trace indicates the project specified SNDR.

7.1.4 Offset for Dc Input Signals

To compare the offset of the transistor-level implementation with the offset of the behavioral model, the same performance characterization test was done as described in section 5.2.3. The result of this investigation is shown in Fig. 7.4. As can be seen, there is a deviation between the result of the behavioral model and the result of the transistor-level implementation. For a desired resolution of 10-bits, the maximum appearing offset for both is within 1 LSB. The transistor-level implementation shows a roughly constant offset over the allowed input signal range. This is a huge advantage in case of trimming is performed, since a 1-point trimming would be enough to remove the offset over the complete input signal range, which would save time and hence costs at wafer test.

7.1.5 Worst-Case Performance Characterization

The results discussed in the previous subsections were gained from nominal simulations. Thus, the supply voltage was assumed to $1.3V$ and the temperature was determined to be room temperature. Since the specifications should be fulfilled in the complete specified supply voltage range of $1.2V$ to $1.47V$ as well as in the specified temperature range of $-40°C$ to $+125°C$, simulations in these ranges need to be done. Furthermore, the modulator should fulfill the specifications even if process and mismatch variations are taken into account. Thus, corner and Monte Carlo simulations in the specified supply and temperature ranges were performed, to treat all conceivable compositions occurring on a chip.

Since simulations of the transistor-level implementation are very time consuming, not all of the previously discussed performance characterization tests could be treated. As a good measure for the behavior of the implementation, a performance characterization using a

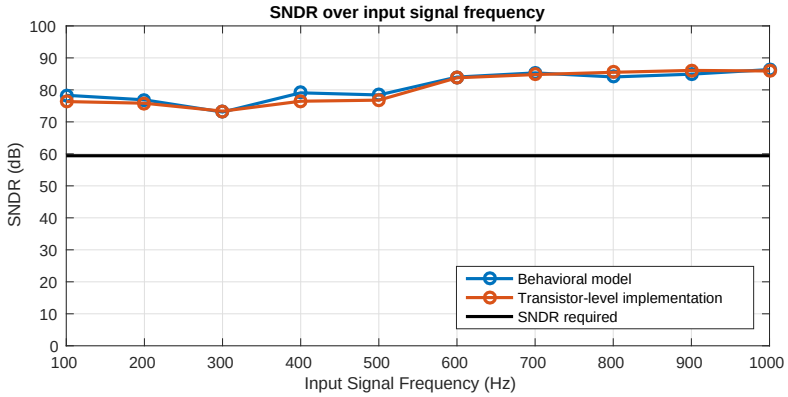

Figure 7.3: Comparison of the achieved SNDR for changing input signal frequency in the behavioral model and the transistor-level implementation of the modulator. The black trace indicates the project specified SNDR.

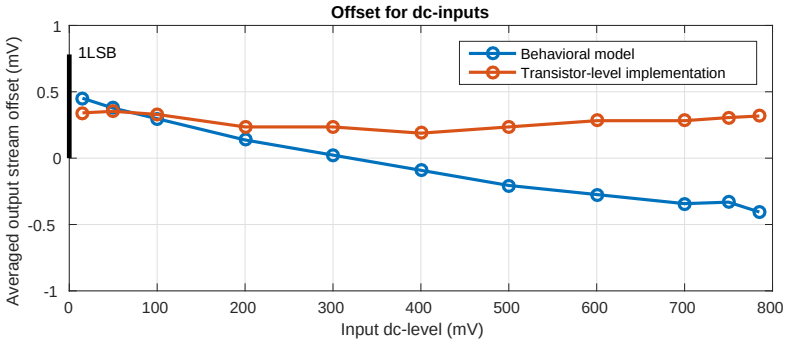

Figure 7.4: Comparison of the occurring offset for changing dc input levels in the behavioral model and the transistor-level implementation of the modulator. The marked size of 1 LSB corresponds to an assumed resolution of 10-bits.

sinusoidal input signal with an amplitude of $-3dBFS$ and a frequency of $531.25Hz$ was chosen by the author. For this input signal, the desired SNDR is equal to $58.96dB$. Corner simulations within the specified supply voltage and temperature range showed thereby a minimum achieved SNDR of $80.5dB$, which is roughly $3dB$ lower as the SNDR achieved at the nominal corner for the same input signal, but still more than $20dB$ above the desired value. To estimate the impact of process and mismatch variations, Monte Carlo simulations within the specified operating regions were performed. These simulations showed a minimum SNDR of $79.1dB$, while the mean value was determined to $84.1dB$, which is comparable to the result gained from nominal simulations. Thus, with these results it can be assumed that the delta-sigma modulator satisfies the specifications in all desired operation conditions. Furthermore, there is still a margin in SNDR for occurring nonidealities in the layout design of the delta-sigma modulator. Tab. 7.1 summarizes the gained results of these simulations. To increase the probability of a first-time-right design, simulations somewhat outside the specified corners were done. These simulations showed that the specifications are even fulfilled for supply voltages of $1.1V$ and $1.55V$, as well as for temperatures of $-50°C$ and $+140°C$.

Name	Target SNDR dB	Min. SNDR dB	Max. SNDR dB	Mean SNDR dB
Corner simulation	58.96	80.5	88.4	84.2
Monte Carlo simulation	58.96	79.1	90.3	84.1

Table 7.1: Results of corner and Monte Carlo simulations for a sinusoidal input signal with an amplitude of $-3dBFS$ and a frequency of $531.25Hz$.

7.2 Estimation of the Area

The estimation of the required area from a schematic-level design is quite difficult. Several proposed rules of thumb for an estimation were found, but they differ quite strongly. Thus, to determine the required area for the delta-sigma modulator, the layout of the schematic-level circuit is required. Since the design of the layout was not a topic for this thesis, just an estimation of the area was done. For this, a simplified and not optimized layout of the modulator was generated. It should be mentioned that this layout was not verified and will not be used for future products, nevertheless to roughly estimate the area it should be appropriate. The designed layout of the delta-sigma modulator requires an area of approximately $0.0075mm^2$ and thus fulfills the specification of $0.008mm^2$. From experience, in an optimized design the area can be reduced by further 10%, thus an area less than $0.007mm^2$ should be reachable.

7.3 Summary of the Implemented Delta-Sigma Modulator

To summarize the implementation of the delta-sigma modulator, a comparison of the achieved performance measures with the given specifications will be done in the first part of this section. In the second part, a comparison with recently published works will be shown.

7.3.1 Comparison with Given Specifications

As shown in section 7.1.5, the implemented modulator should satisfy the desired SNDR in all intended operating conditions. Thus, the specification for the SNDR and hence the specification for the resolution of the delta-sigma modulator is met. The achieved peak SNDR of $86.9dB$, determined at nominal conditions, leads to a resolution of 14.1-bits and thus provides, in case of an ideal scaling of the CTAT voltage is assumed, a temperature resolution of approximately $10mK$ in the given temperature range. The total current consumption of the design is equal to $2.29\mu A$, determined by schematic-level simulations at the nominal corner. Since more than $1\mu A$ is consumed by the reference voltage generation circuit, which was designed to be usable as a reference voltage source for other blocks of the chip at the same time, this somewhat specification violating value was accepted. As discussed in the previous section, the required area was estimated to $0.0075mm^2$ and thus fulfills the given project requirements. Tab. 7.2 compares the desired with the achieved specifications of the delta-sigma modulator. Additionally, further performance measures were added for the implemented delta-sigma modulator.

Parameter	Symbol	Specified value	Achieved value	Unit
Peak SNDR	$SNDR_{peak}$	61.96	86.9	dB
Effective resolution	ENOB	10	14.1	bits
Current consumption	I	2.2	$1.22^{(1)}$ / $2.29^{(2)}$	μA
Area	A	0.008	0.0075	mm^2
Dynamic range	DR	-	88	dB

(1) Reference voltage generator excluded

(2) Reference voltage generator included

Table 7.2: Summary of the performance of the implemented delta-sigma modulator achieved in simulation.

7.3.2 Comparison with Previous Works

In this section, a comparison of the implemented design with recently published works will be made. As discussed in section 1.2, the determination of the figure-of-merit of a design is a commonly used method, to compare state-of-the-art implementations. For the determination of the FOM, the maximum achieved SNDR of $86.9dB$, gained in the characterization test discussed in section 7.1.2, was used. The simulated average current consumption of the delta-sigma modulator was determined to $2.29\mu A$. Thus, at the supply voltage of $1.3V$, the total power consumption of the modulator is equal to $2.98\mu W$. Using all these information, the FOM of the modulator using equation (1.1) can be calculated to

$$\text{FOM} = \frac{2.98\mu W}{2^{\frac{86.9dB-1.76dB}{6.02dB}} \cdot 2 \cdot 1kHz} = 0.082\frac{pJ}{conv}. \tag{7.1}$$

In Tab. 7.3, the discussed publications of section 1.2 are compared with the implementation of this thesis. It should be mentioned, that the achieved values for this work are from schematic-level simulations, while the results of the publications are either determined from extracted layout simulations or measurements performed on a fabricated chip. Nevertheless, it can be claimed that the design of this thesis can be compared with state-of-the-art designs and is thus a perfectly convenient implementation for the application in smart temperature sensors.

Ref.	peak SNDR dB	BW kHz	Order 1	OSR 1	Impl. -	L nm	P μW	FOM $\frac{pJ}{conv}$
[14]	80.5	1	5	16	FD	350	9	0.52
[15]	76	0.5	2	250	FD	65	2.1	0.407
[16]	68	0.2	2	200	FD	180	1.3	1.583
[17](1)	63	8	2	125	SE	350	6.72	0.364
[18]	61	10	3	70	PD	130	7.5	0.409
This work(2)	**86.9**	**1**	**2**	**125**	**SE**	**40**	**2.98**	**0.082**

(1) Clock generator excluded

(2) Schematic-level simulation

SE ... Single-ended

PD ... Pseudo-differential

FD ... Fully-differential

Table 7.3: Comparison of this work with state-of-the-art delta-sigma modulator implementations.

7.4 Conclusion

This thesis showed the design process of a power and area efficient implementation of a delta-sigma modulator. The procedure to find the most convenient implementation regarding given specifications was shown. Design considerations were described and MATLAB simulations were performed. The design of a behavioral model, which was used to optimize the design regarding theoretically determined circuit block specifications and to estimate the impact of nonidealities associated with these blocks, was explained. Proposed verification tests were discussed. With the gained specifications of behavioral simulations, the implementation of the delta-sigma modulator on transistor-level was done.

A low power and low area second-order discrete-time delta-sigma modulator in feedback configuration was designed in a $40nm$ CMOS process. The implemented modulator achieves a peak SNDR of $86.9dB$ in a signal bandwidth of $1kHz$, while just consuming $2.98\mu W$ from a nominal $1.3V$ supply. This performance is achieved with an OSR of 125. The occurring power consumption includes a reference voltage generation circuit, which enables the operation of the modulator with a single on-chip reference voltage. The properties of oversampled converters regarding matching accuracy of analog components was exploited to minimize the area consumption, while the low power consumption was achieved by using devices of the amplifying stages in the sub-threshold region, using a comparator without static current consumption and determining the most efficient capacitor values for the desired resolution. The occupied die area of the delta-sigma modulator is equal to $0.0075mm^2$. The modulator maintains its performance in a supply range of $1.2V$ to $1.47V$ and a temperature range from $-40°C$ to $+125°C$ and is thus perfectly convenient for the application in smart temperature sensors. The low power consumption makes it possible to use the modulator in battery powered or even powered-by-the-field applications. Compared to recently reported delta-sigma modulators with similar input bandwidths, this work shows one of the best FOMs, where it should be noted that the implementation was characterized with schematic-level simulations.

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