Diploma Thesis

Low Power 12 Bit Pipeline ADC with Analog Error Compensation in 40 nm

DT 745

by

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Abstract

Pipeline Analog-to-Digital Converters (ADCs) cover a wide field of broadband communication. They combine both high resolution and high sampling rate with low power consumption. This type of ADC is among the most attractive approaches for medium-high resolution (8-14 bits) and medium-high speed (10-200 MHz) applications. Different error compensation techniques are used to increase the resolution of pipeline ADCs or to relax the requirements for precision in order to save power. An attractive approach to compensate for the errors introduced by a finite DC gain is the use of analog error compensation techniques such as *dual path amplification*. In *dual path amplification*, each pipeline stage is split into a coarse stage and a fine stage. The DC gain that is required for a pipeline stage can be split over two Operational Amplifiers (op-amps). This thesis investigates *dual path amplification* for 40 nm technology both analytically and in Matlab simulations. Error sources are considered separately for the Dual Path Amplification (DPA) Multiplying Digital-to-Analog-Converter (MDAC) with 1.5 bits and the DPA MDAC with 2.5 bits. The residue error of a single pipeline stage is compared with linearity considerations for the pipeline ADC using the *dual path amplification* technique. The DPA approach makes it possible to reach the needed equivalent *DC gain* with two simple Miller op-amps in 40 nm technology. The *noise performance* and the error due to *capacitor mismatch* of an ADC built of DPA MDAC stages are similar to the noise performance of an ADC built of Single Path Amplification (SPA) MDAC stages. Errors of the coarse stage can be compensated by the fine stage but errors of the fine stage cannot be compensated. The fine stage is the dominant error source for noise and errors due to capacitor mismatch. The *chip size* is increased with respect to SPA MDACs, because of additional capacitors and switches. Moreover, two op-amps are used instead of one. *Digital calibration* can be avoided unless capacitor mismatch of the technology used limits the resolution. *Resolution limits* for the pipeline ADC using DPA can be increased with 2.5 bit MDAC stages instead of 1.5 bit MDAC stages. DPA pipeline ADCs built of 2.5 bit MDACs have, with respect to 1.5 bit, relaxed requirements for capacitor mismatch, DC gain and noise sources. Furthermore power can be saved because fewer pipeline stages are required.

Kurzfassung

Pipeline Analog/Digital-Umsetzer (A/D-Umsetzer) decken ein weites Feld von Breitbandkommunikation ab. Sie verbinden hohe Auflösungen und Abtastraten mit niedrigem Energieverbrauch. Dieser Umsetzertyp ist eine der attraktivsten Lösungen für Anwendungen mit mittelhohen Auflösungen (8-14 Bit) und mittelhohen Abtastraten (10-200 MHz). Um die Auflösung von Pipeline A/D-Umsetzern zu erhöhen oder die Anforderungen an Fehler zu relaxen um Energie zu sparen, werden verschiedene Fehler-Kompensation Techniken eingesetzt. Analoge Fehler Kompensation, wie die Dual Path Amplification Technik, ist ein vielversprechender Ansatz um den Fehler zu kompensieren der durch endliche Gleichspannungsverstärkung entsteht. Bei der Dual Path Amplification Technik wird jede Pipeline-Stufe in eine Grob- und in eine Fein-Stufe aufgeteilt. Die benötigte Gleichspannungsverstärkung der Pipeline-Stufe kann dadurch auf zwei Operationsverstärker (OPVs) aufgeteilt werden. Diese Arbeit untersucht Dual Path Amplification für die 40 nm Technologie einerseits analytisch und andererseits mit Matlab Simulationen. Die Fehlerquellen werden getrennt für Dual-Path-Amplification (DPA) Multiplying Digital to Analog Converters (MDACs) mit 1,5 Bit und 2,5 Bit analysiert. Der Residuum Fehler einer Pipeline-Stufe wird mittels Linearitätsbetrachtungen des gesamten Pipeline ADCs mit DPA verglichen. Die DPA Technik macht es möglich, die benötigte Gleichspannungsverstärkung mit zwei einfachen Miller OPVs in der 40 nm Technologie zu erreichen. Die Rauscheigenschaften und die Eigenschaften bezüglich Kapazitäts-Fehlanpassung von DPA A/D-Umsetzern und Single-Path-Amplification (SPA) A/D-Umsetzern sind ähnlich. Fehler der Grob-Stufe können durch die Fein-Stufe kompensiert werden, während Fehler der Fein-Stufe nicht kompensiert werden können. Die Fein-Stufe ist die dominante Fehlerquelle. Die Chipfläche ist im Vergleich zu SPA MDACs größer, da zusätzliche Kondensatoren und Metal Oxide Semiconductor (MOS) Schalter benötigt werden. Außerdem werden zwei Operationsverstärker anstelle von einem verwendet. Digitale Fehlerkorrektur kann vermieden werden solange die, der Technologie inhärente, Fehlanpassung der Kondensatoren die Auflösung nicht begrenzt. Die Auflösung von DPA Pipeline A/D-Umsetzern kann durch die Verwendung von 2,5 Bit MDACs anstelle von 1,5 Bit MDACs verbessert werden. DPA Pipeline A/D-Umsetzer mit 2,5 Bit haben im Vergleich zu 1,5 Bit geringere Anforderungen in Bezug auf die Fehlanpassung von Kapazitäten, die Gleichspannungsverstärkung und in Bezug auf Rauschquellen. Außerdem kann Energie eingespart werden, da weniger Pipeline-Stufen zum Einsatz kommen.

Acknowledgement

This diploma thesis was started 6 months before the last option to finish my Dipl.-Ing. studies. Therefore, time was tight and the pressure to finish the thesis on time was high. I would like to thank my supervisor at the Technical University Graz, Peter Söser, who supported me as much as possible in order that the deadline could be met.

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My special thanks go to my family who supported me throughout my studies. First of all, I would like to express my gratitude to my parents Anna and Gregor and then to my brothers and sisters, especially to Nikolaus, who supported me with his rich academic experience.

Last, but not least, I want to thank my girlfriend Lisi for her encouragement, patience and understanding.

Statutory Declaration

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

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1 Introduction

1.1 Motivation

The importance of digital signal processing is continuously increasing and most communication systems today use digital signal processing techniques. These techniques can typically better deal with variations in the power supply and are less sensitive to noise than their analog counterparts. Further, variations in the production process are tolerated well and scaling the systems to more compact technologies (e.g., from 65 nm to 40 nm) has less impact on the design of digital circuits than for analog circuits. [2]

Nevertheless, physical signals are analog and are typically measured by sensors that produce an analog signal. In order to digitally process the signal it must be translated, i.e., an interface between the analog circuits and the digital circuits is required. One of these interfaces is the Analog to Digital Converter (ADC) . The design of ADCs is a major challenge for designers due to rapidly evolving digital systems that require increasingly accurate and fast converters. The current trend to integrate ADCs into digital technologies makes the design even more sophisticated. [2]

An important representative of ADCs is the so-called *pipelined ADC*. Pipelined ADCs cover a wide range of broadband applications such as Digital Video Broadcasting (DVB), Power Line Communications (PLC), or Very high-bit rate Digital Subscriber Line (VDSL). They combine both high resolution and high sampling rate with low power consumption and are among the most attractive approaches for medium-high resolution (8-14 bits) and medium-high speed (10-200 MHz) applications. [2]

At the same time, pipeline ADCs are also very complex structures that depend on highly accurate switched capacitors, other sub-ADC architectures, and precise timing. One source of imprecision that must be dealt with is linearity errors. To compensate for linearity errors, digital and analog calibration techniques have been developed. One promising analog compensation technique is *dual path amplification (DPA)*. Recently, a new high-performance low-power pipelined ADC based on DPA was proposed. This ADC uses standard 65 nm technology and reaches 10 bit resolution and a sampling rate of 200 MS/s at a low power consumption of only 5.37 mW [1].

The scope of this thesis is to investigate the DPA architecture for pipelined ADCs for the newer 40 nm technology, which is gaining importance for logic circuits and is expected to supersede the older 65 nm technology in many applications.

1.2 Analog Error Compensation Approach

To achieve high resolutions for ADCs, various error compensation approaches have been applied. A powerful approach that is able to compensate for a wide range of errors is based on complex digital calibration techniques [3]. However, digital calibration comes at the cost of additionally required chip area and higher power consumption, which makes this approach less attractive for some applications.

One important error source is caused by the finite DC gain of the operational Amplifiers (op-amps). The problem is only partially solved by using complex op-amps with high DC gain such as cascaded op-amps or op-amps with feedback loop, since these op-amps have higher power consumption and worse noise behavior than a simple Miller op-amp.

An attractive alternative to compensate for the errors introduced by a finite DC gain is the use of analog error compensation such as *dual path amplification* [1]. In dual path amplification, each pipeline stage is split into a coarse stage and a fine stage. Both perform the same operation and calculate the residue voltage. The fine stage also has, in addition to the common inputs with the coarse stage, the inverted output of the coarse stage as an input. The fine stage calculates the error caused by the coarse stage. The overall residue of the pipeline stage is the sum of the coarse output and the fine output. A key feature of this approach is that the op-amps of the coarse and the fine stage have different requirements and can be optimized separately. The coarse op-amp has a wide swing output signal and can be relaxed regarding noise and capacitor mismatch. The fine op-amp, on the other hand, must have good noise performance and low mismatch error, but only needs to perform a small swing output. The DC gain required for the MDAC can be split across both op-amps, which allows simple op-amps with low power consumption to be used.

1.3 Research Contribution

The scope of this thesis is to investigate the DPA architecture for use with 40 nm technology. Previously, DPA had only been discussed for the older 65 nm technology [1] and it was not obvious whether this technique would also prove to be useful for the 40 nm technology. Due to the changed physical properties of the electronic modules, moving from 65 nm to 40 nm is not straightforward and essentially requires redesigning the circuit.

This thesis investigates DPA for 40 nm technology both analytically and in Matlab simulations. The following error sources are considered separately for 1.5 bit and 2.5 bit bit DPA MDACs:

finite DC gain

capacitor mismatch

noise sources

offset voltage

The analytic approximations of the error sources are verified in Matlab simulations, which meant that the corresponding transfer functions had to be derived

For the simulations, the Matlab model of a 1.5 bit DPA MDAC with flip around architecture, which had been developed as part of a previous project, was extended to a 1.5 bit DPA MDAC with non-flip around architecture and to a 2.5 bit DPA MDAC. A Matlab model of the overall pipelined ADC was constructed based on the individual MDAC model stages, which were cascaded, and the ADC performance was analyzed in the frequency domain. The SPA structure with 1.5 bits and 2.5 bits was compared to the DPA approach, and requirements for the mentioned error sources were determined.

The goal of dual path amplification is to reach a high resolution without digital calibration or complex op-amps, i.e., to save chip area and keep the power consumption low. The main findings of this thesis with respect to this goal as follows:

1. *DC gain:* It is possible to achieve the needed equivalent DC gain with two simple op-amps of about 45 dB. The sum of the coarse DC gain and the fine DC gain is higher than the DC gain required for the SPA approach.

2. *Noise performance and capacitor mismatch:* The noise performance and the error due to capacitor mismatch of an ADC using DPA MDAC stages is similar to the noise performance of an ADC built of SPA MDAC stages.

3. *Chip area:* Additional capacitors and switches are needed, which increases the chip size with respect to SPA MDACs.

4. *Digital calibration:* No digital calibration is needed for resolutions covered by the capacitor mismatch of the technology used.

5. *Resolution limits:* In 40 nm technology, the resolution using DPA is limited to an absolute maximum of 10.7 bits for 1.5 bit MDACs and of 11.2 bits for 2.5 bit MDACs.

The thesis is organized as follows: Chapter 2 introduces the basics of analog to digital converters and of pipelined ADCs. Chapter 3 derives error approximations and transfer functions for a single 1.5 bit MDAC stage and verifies the approximations in Matlab simulations, Chapter 4 extends the results to 2.5 bit MDAC stages. 1.5 bit and 2.5 bit MDAC are compared. The cascading of multiple MDAC stages to an overall pipelined ADC is discussed in Chapter 5 based on Matlab simulation results. The digital output of the ADC is analyzed in the frequency domain. The key findings are summarized in Chapter 6 and final conclusions are drawn.

2 Basics

This chapter contains important basics about analog to digital conversion, and about the pipelined ADC and its error sources. First the discretization in time and amplitude is shown in time and frequency domain and noise occurring while sampling, kT/C Noise, is explained. Then the impact of jitter on the analog to digital conversion is discussed. The last section of this chapter deals with error sources of the pipelined ADC and performance metrics. The entire chapter is taken from the dissertation 'Low Noise High Speed Analog Video Frontends for PC and HDTV Applications in 90nm and 65nm' [4] written by Dr. Martin Trojer. It contains no research contributions but theoretical basics to the topic. It was carried over because of time reasons, with friendly permission of the author.

2.1 Sampling and Quantization

Sampling and quantization are the basics for the analog to digital conversion which is a key function in modern systems. This is valid for each converter topology.

2.1.1 Sampling Function

The sampling function represents a sequence of equidistant Dirac impulses.

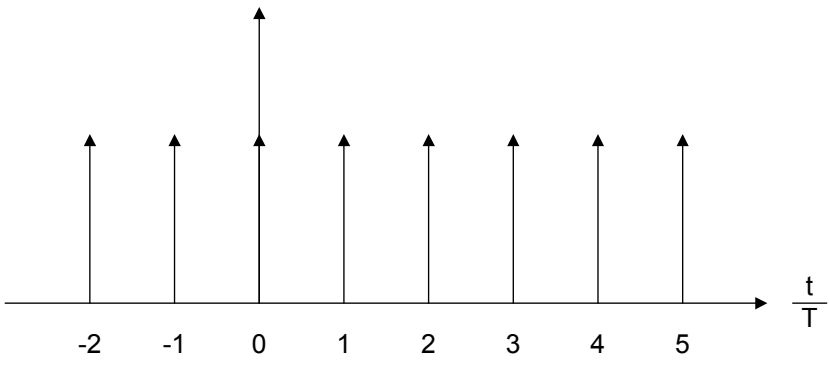

Figure 2.1: Sampling function

$$\triangle(t) = \sum_{n=-\infty}^{+\infty} \delta(t - n \cdot T) \tag{2.1}$$

The sampling function can be evaluated in the frequency domain, where a Fourier series expansion is performed. Hence the sampling function is interpreted by the sum of fundamental wave and harmonics. (fs = sampling frequency)

$$\triangle(t) = \sum_{n=-\infty}^{+\infty} Cn \cdot e^{j \cdot \omega s \cdot n \cdot t} \Longrightarrow t = \frac{2 \cdot \pi}{\omega s} \tag{2.2}$$

$$Cn = \frac{1}{T} \cdot \int_{-\frac{T}{2}}^{+\frac{T}{2}} \triangle(t) \cdot e^{-j \cdot \omega s \cdot n \cdot t} \cdot dt = \frac{1}{T} \cdot \int_{-0}^{+0} \delta(t) \cdot e^{0} \cdot dt = \frac{1}{T} \tag{2.3}$$

δ(t) is a Dirac pulse with infinitely short duration impulse and amplitude.

$$\triangle(t) = \frac{1}{T} \sum_{n=-\infty}^{+\infty} e^{j \cdot \omega s \cdot n \cdot t} \tag{2.4}$$

In equation 2.4 an infinite series of sine waves is shown. In the frequency domain it is given as:

$$\triangle(f) = \frac{1}{T} \sum_{n=-\infty}^{+\infty} \delta(f - n \cdot fs) \tag{2.5}$$

Next a transformation pair between time and frequency domain is obtained.

$$\triangle(t) = \sum_{n=-\infty}^{+\infty} \delta(t - n \cdot T) \Leftrightarrow \triangle(f) = \frac{1}{T} \sum_{n=-\infty}^{+\infty} \delta(f - n \cdot fs) \tag{2.6}$$

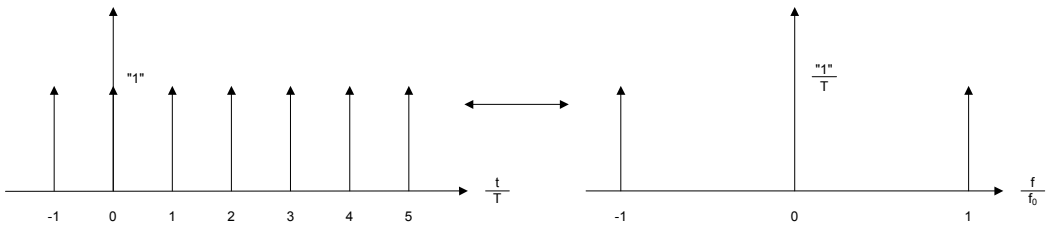

Figure 2.2: Transformation between time and frequency domain for the sampling function

Sampling means multiplication of the continuous time input signal x(t) with the sampling function $\triangle$(t). In time domain an impulse series is obtained which is weighted by the input signal amplitude. A multiplication in time domain corresponds to a convolution in frequency domain, which results in a reproduction of X(f) at integer multiples of the sampling frequency. Therefore, a periodical spectrum is obtained illustrated in figure 2.3. In the frequency domain a convolution of the analog signal spectrum and the spectrum of the sampling function is obtained. In equation 2.7 the sampling theorem is shown. If the bandwidth of X(f) increases then overlapping of the

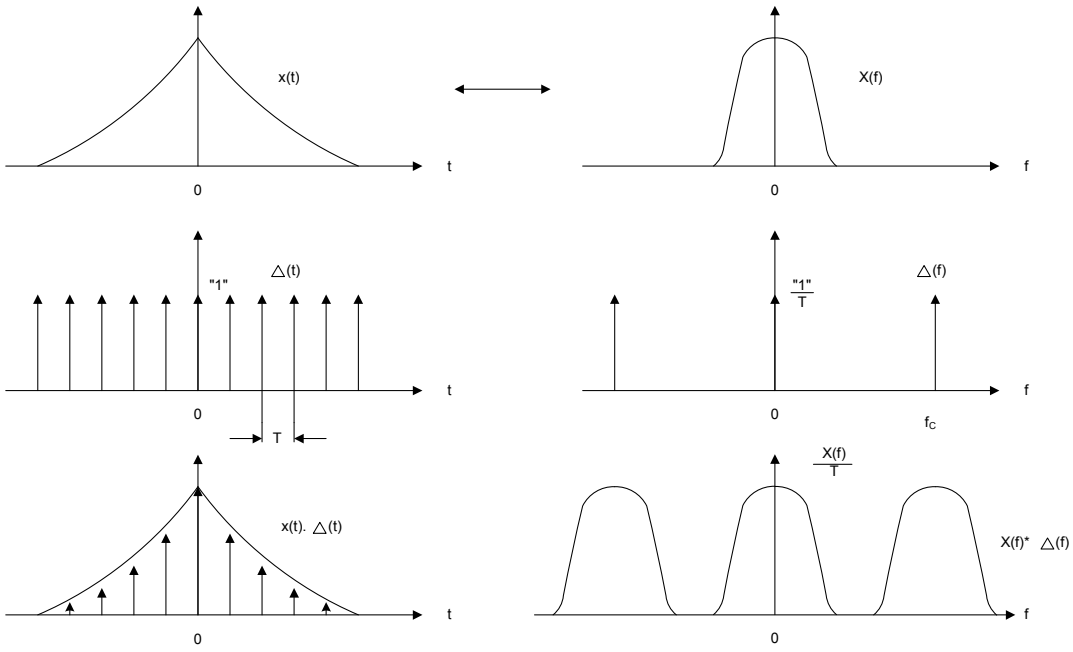

Figure 2.3: Sampling in time and frequency domain

baseband and images occurs, which is called aliasing. Consequently, frequencies larger than half the sampling frequency must not be present in the input signal, which can be realized by a low-pass filter.

$$X(f) * \triangle(f) = \frac{1}{T} \sum_{n=-\infty}^{+\infty} X\left(f - n \cdot fs\right) \tag{2.7}$$

2.1.2 Amplitude Quantization

The analog input samples are rounded to discrete values corresponding to a set of limited numbers, suitable for further digital modification. Although the quantization is non-linear, it can be approximated by a linear model. In many cases the rounding error is represented by a random signal, which is added to the ideal not quantized signal. The rounding error is assumed to be white and uncorrelated with the input signal. To meet these assumptions of the linear model, the input signal must be "busy" and many quantization intervals must be occupied by the signal. In contrast, constant input signals result in non-zero correlation of the rounding error, and the white noise model is obviously not valid.
The noise signal has a constant probability density from -q/2 to +q/2. It is uncorrelated with the signal s(t) and has a wideband noise spectrum. From the difference of the quantization noise

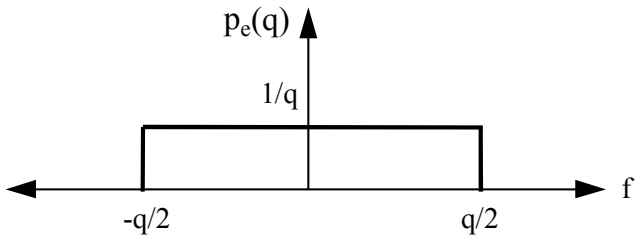

Figure 2.4: Equally distributed quantization noise

power before quantization and after quantization the quantization noise power is obtained.

$$Pq = \frac{q^2}{12} \tag{2.8}$$

By sampling the power density spectrum the noise is concentrated to the range of 0 to fs/2. Consequently, the noise power is equally distributed shown in figure 2.5.

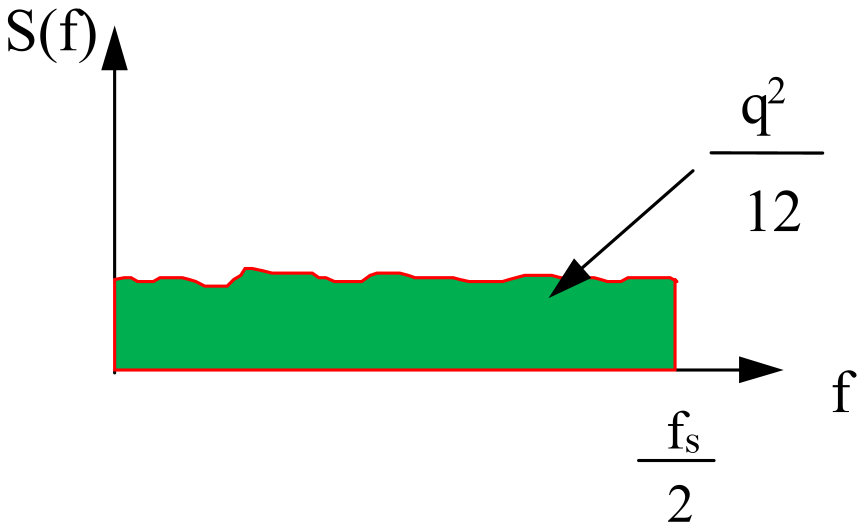

Figure 2.5: Noise density spectrum of the quantization noise

2.1.3 kT/C Noise

Every switch action contains resistive elements with thermal noise: This thermal noise is sampled on the capacitor each cycle. The overall noise power of the switch depends on the temperature,

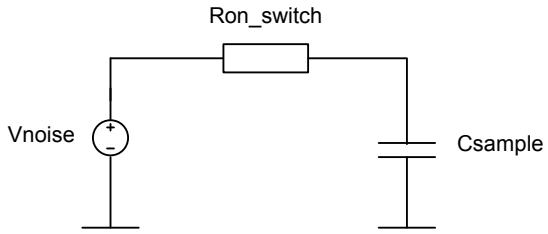

Figure 2.6: The equivalent circuit of a sample switch and capacitor

the Boltzmann constant k and the considered bandwidth.

$$Pnoise_{sw} = 4 \cdot k \cdot T \cdot R \cdot BW \tag{2.9}$$

For calculating the noise power of the sampling circuit the noise power of the resistor can be multiplied by the square of the low pass transfer function.

$$Pnoise = \int_{f=0}^{f=\infty} \frac{4 \cdot k \cdot T \cdot R \cdot \delta f}{1 + (2 \cdot \pi \cdot f)^2 \cdot R^2 \cdot C^2} = \frac{k \cdot T}{C} \tag{2.10}$$

2.2 SNR due to Jitter

The influence of the uncertainty of the sampling clock leads to a decreasing of the SNR. In figure 2.7 this uncertainty results in an error in the voltage amplitude du.

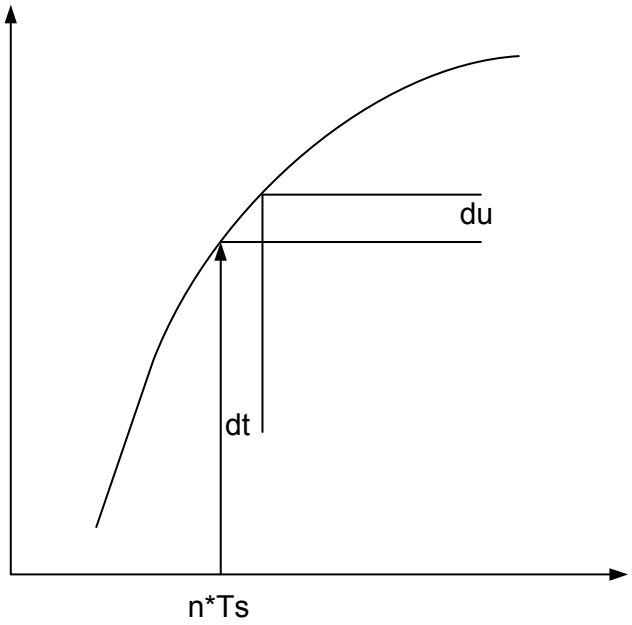

Figure 2.7: Jitter at the sampling process

$$dt = \frac{dV}{SRmax} = \frac{2 \cdot Vinp}{Vinp \cdot 2 \cdot \pi \cdot f \cdot 2^{N+1}} = \frac{1}{\pi \cdot f \cdot 2^{N+1}} \tag{2.11}$$

If dt is an event from a Gaussian distributed jitter then equation 2.12 is valid. Moreover it can be seen that the signal amplitude doesn't influence the signal to noise ratio (cf. 2.8).

$$SNR = \frac{\int \left(Vinp \cdot sin\left(\omega \cdot t\right)\right)^2 \cdot dt}{\int \sigma_{dV}^2 dt} = \frac{1}{\left(\omega \cdot \sigma_{dt}\right)^2} \tag{2.12}$$

2.3 Pipeline ADC and Error Sources

A pipeline ADC consists of similar ADC stages which are connected in a pipeline [5]. Each stage has a resolution of n-bit where a redundancy is used for error correction. The overall resolution of this ADC depends on the amount of stages and input reflected noise at the first stage. A maximum resolution of 16 bit at medium sample rates like 100 MS/s can be achieved by calibration. Figure 2.9 shows the principle topology of a pipeline stage. First the input is sampled and amplified by 2 for 1.5 bit per stage architecture. The comparator which performs the analog to digital conversion can be connected in front or behind the sample and hold.

After the amplification the reference voltage must be subtracted or added depending on the result of the comparator. The analog output is led to the next pipeline stage where the same process is started again. Each stage works with the same sample rate. So the conversion speed is the same as for a Flash ADC but a delay is generated depending on the amount of pipeline

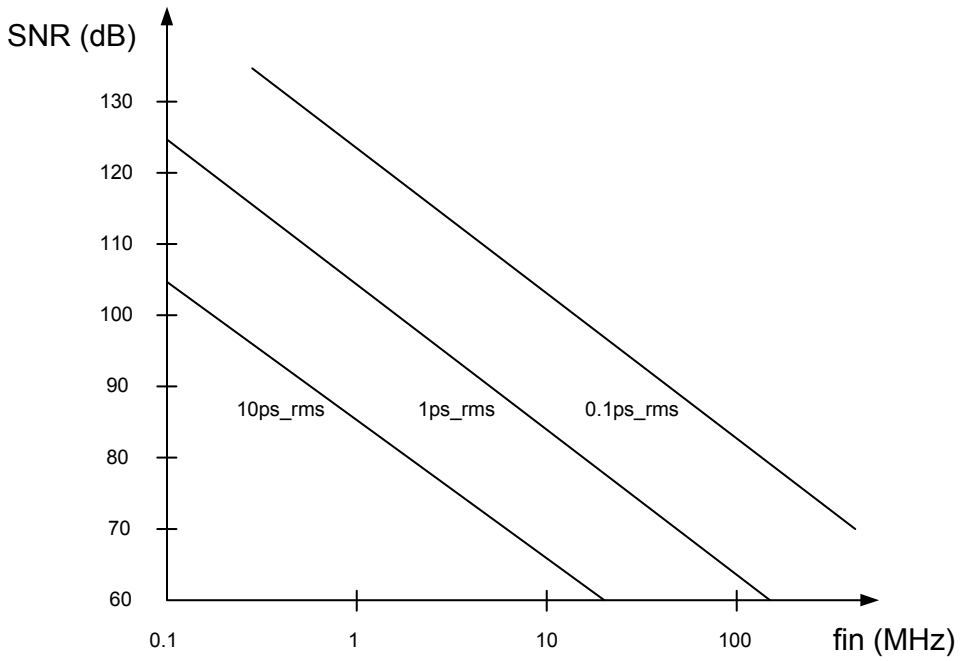

Figure 2.8: SNR due to jitter

stages. Compared to a two step Flash ADC the power consumption and the amount of comparators is smaller. Also from the design point of view only one stage has to be developed and scaled for the following pipeline stages.

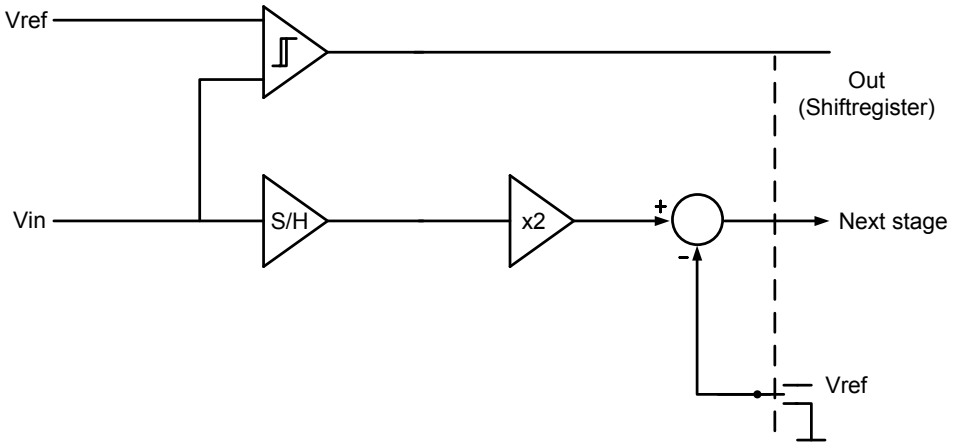

Figure 2.9: Pipeline ADC principle

The residue (analog output) of a 1 bit and 1.5 bit stage is demonstrated in figure 2.10. The 1.5 bit stage reduces the headroom by a factor of 2 for the output to use it for the correction of an error of the comparator. Therefore saturation of the multiplying DAC (MDAC) amplifier is avoided. The principle transfer function of the MDAC can be seen in equation 2.13 where D depends on the decision of the comparator and corresponds to -1, 0 or 1.

$$Vout = Vin \cdot 2 - D \cdot Vref \tag{2.13}$$

2.3.1 Offset in a Pipeline ADC

The maximum correctable offset Voff_{1st} of the first stage followed by an ideal stage corresponds to 1/8*vref. This can be explained by the comparator levels of +/- 0.25*vref of the second stage divided by 2. The maximum correctable offset of an N-bit ADC is calculated in equation 2.14. For a 10 bit ADC this formula yields a maximum correctable offset of 0.25*vref. An increase of the bit count of the stages per one decreases the correction range by a factor of two. Figure 2.11 shows the residue of the first stage if the comparator performs a wrong decision.

$$Voff_{corr}(N) = \sum_{i=2}^{N} \frac{Voff_{1st}}{2^{i-2}} \tag{2.14}$$

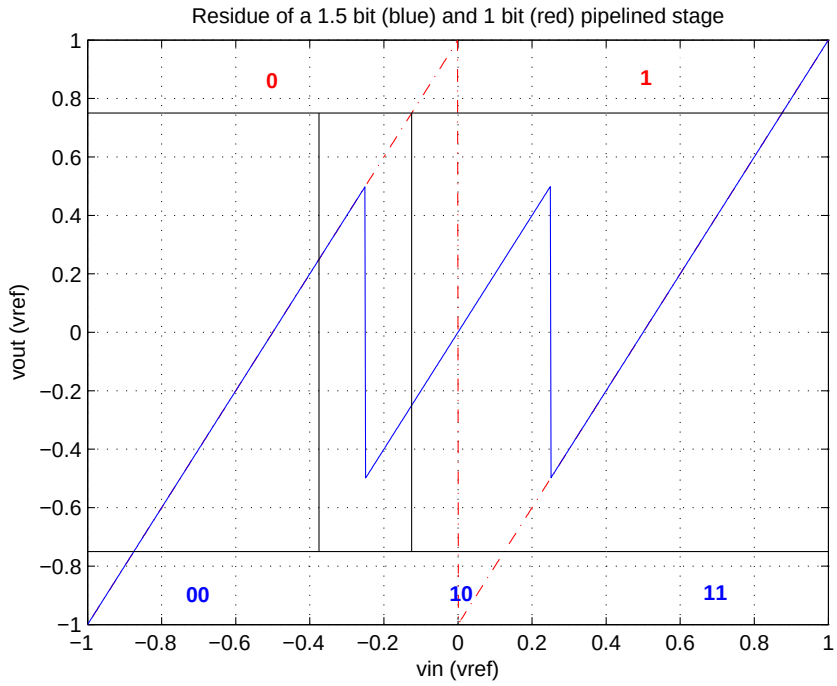

Figure 2.10: Residue of 1 bit and 1.5 bit stage

2.3.2 DNL and INL

The DNL stands for the differential non-linearity and corresponds to the deviation of the real to the ideal step width related on the ideal step width. For the evaluation of the ADC a ramp must be applied where the received characteristics are shown in figure 2.12. A DNL larger than 1 LSB leads to a missing code which degrades the linearity very much.

$$DNL_i = \frac{LSB_{real} - LSB_{ideal}}{LSB_{ideal}} \tag{2.15}$$

The integral non-linearity (INL) equals to the distance of the measured to ideal stepcurve related on the ideal step width. Additionally the INL is the integration of the DNL.

$$INL_i = \frac{x_{real} - x_{ideal}}{LSB_{ideal}} \tag{2.16}$$

In figure 2.12 the INL is demonstrated as the green difference of x_{real}-x_{ideal}. The difference can

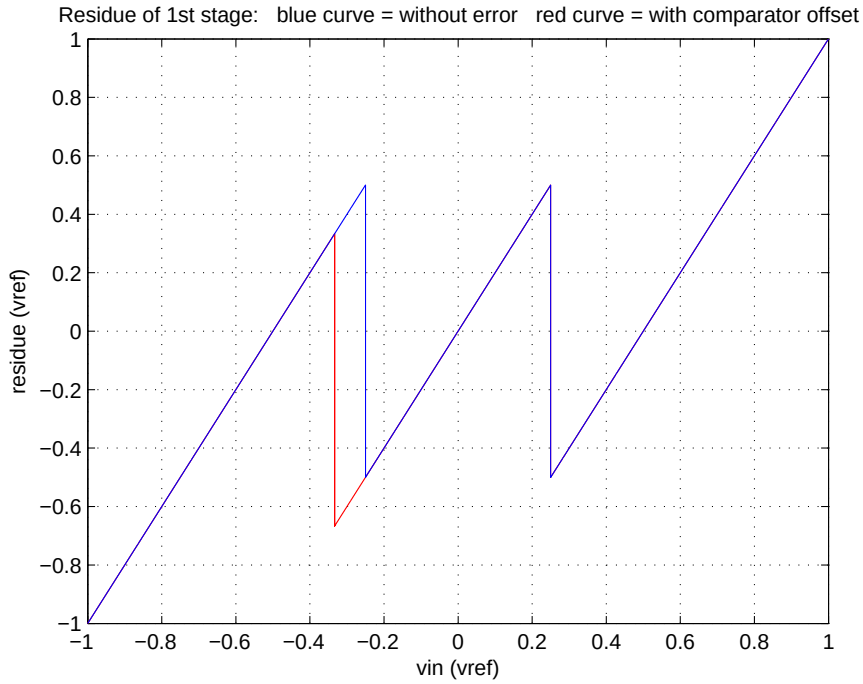

Figure 2.11: Residue of a 1.5 bit stage with comparator offset

be calculated by measuring the center of each quantization step of the ideal and real step-curve.

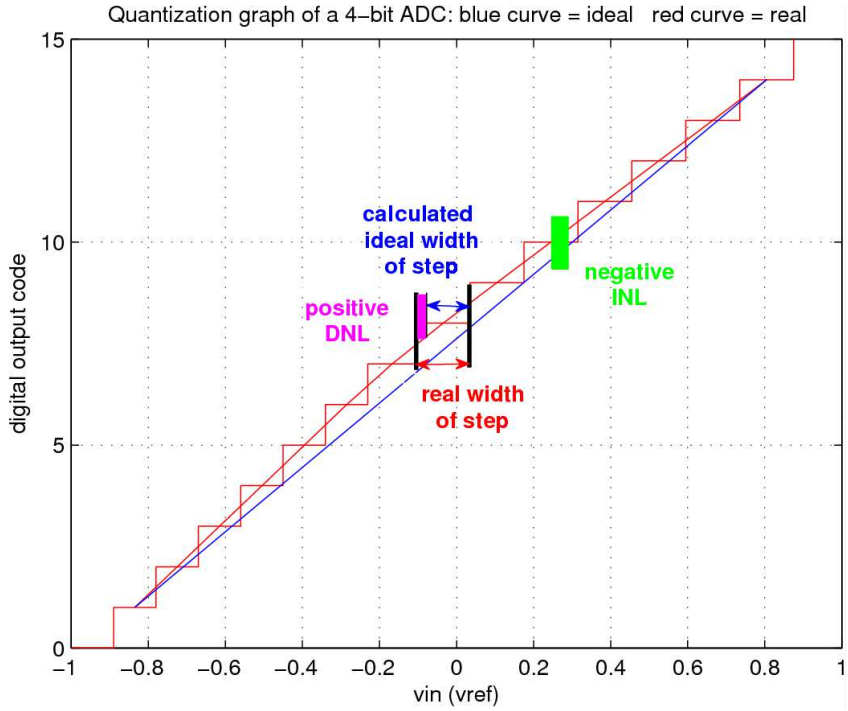

Figure 2.12: 4 bit ADC characteristics with DNL and INL

2.3.3 Gain Error

The output voltage of an MDAC is calculated in equation 2.17 where the feedback capacitor of the inverting amplifier is C1. Figure 2.13 illustrates the bottom plate sampling process with a two phase non-overlapping clock signal where the input is disconnected after the sampling switch is opened. Hence the influence of clock feedthrough and charge redistribution of the input switch can be reduced. After sampling is finished the op-amp is used as inverting amplifier with gain one. There the charge from C2 is transferred to C1. Consequently the gain of two for the 1.5 bit stage is realized. For a 2.5 bit stage a gain of 4 will be get during amplification by one unity capacitor in the feedback and 3 at the input branch.

$$V_{out} = V_{in} \cdot \frac{C_1 + C_2}{C_1} - V_{ref} \cdot \frac{C_2}{C_1} \tag{2.17}$$

The gain error is caused by capacitor mismatch and low op-amp gain. Due to a very large gain

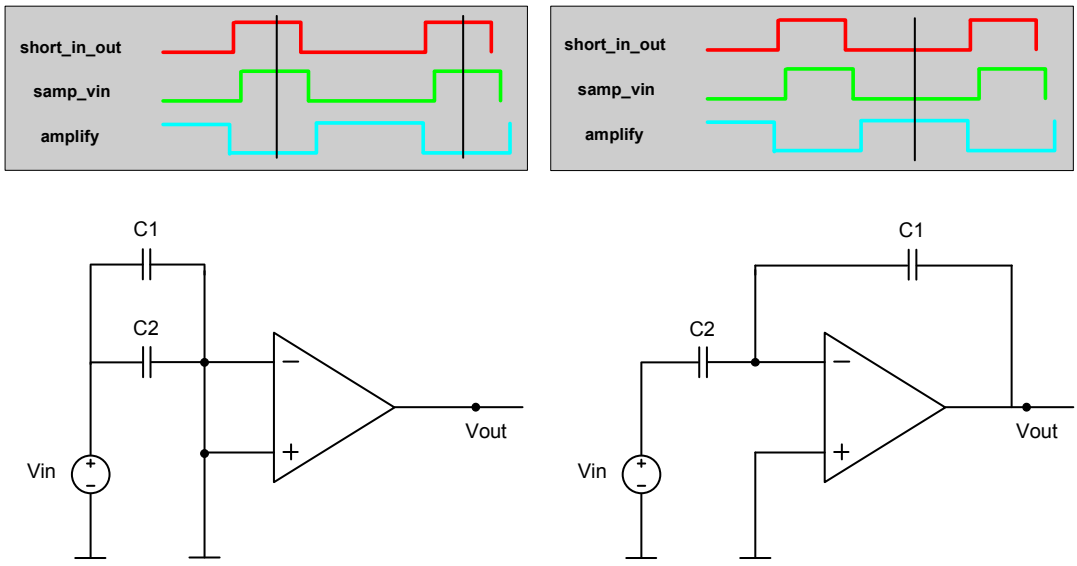

Figure 2.13: MDAC op-amp in sampling and amplification mode

error the output of the first stage is smaller than the ideal value shown in figure 2.14. Therefore a shift of the comparator levels of the first stage in the overall ADC transfer characteristics occurs which is demonstrated in figure 2.15. Specially the accuracy of the first stage is essential for the overall converter performance.

The gain error of the first and second stage of a pipeline ADC is shown in figure 2.16. Inspecting this figure it can be seen that a gain error in the first stage has a large impact on the residue of the second stage. Alternating gain errors of the pipeline stages lead to a larger decrease of the linearity than the same gain error in each stage [6]. The shown gain errors are not realistic and were chosen very large for demonstration.

2.3.4 Total Harmonic Distortion

The total harmonic distortion (THD) 2.18 and the signal-to-noise ratio (SNR) are used to characterize an ADC. The THD is the ratio between the squared voltages of the signal and the tones. It measures the linearity which influences the picture quality. 5 to 10 harmonics are included in the THD and the rest is considered as noise.

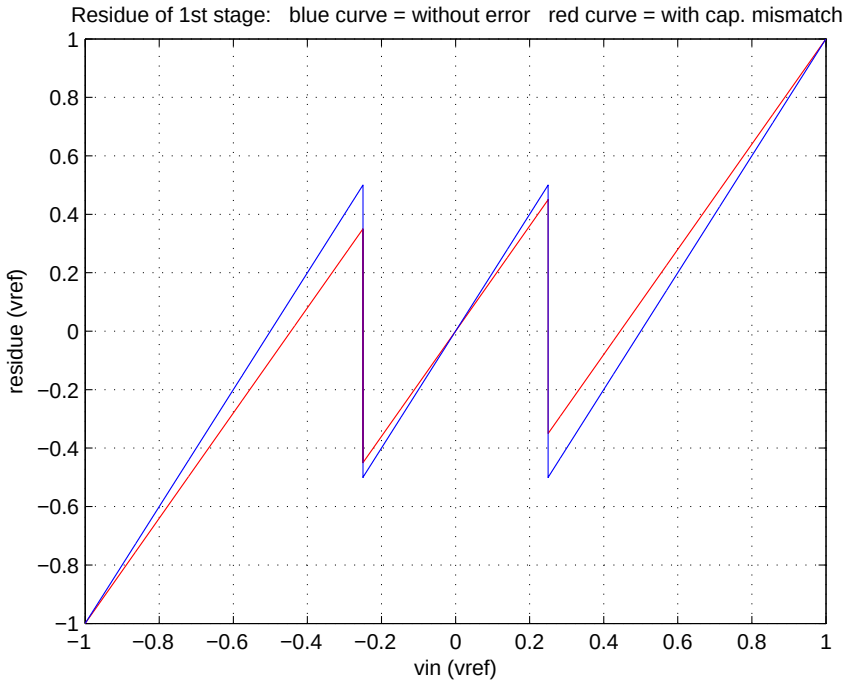

Figure 2.14: Residue of a 1.5 bit stage with capacitor mismatch

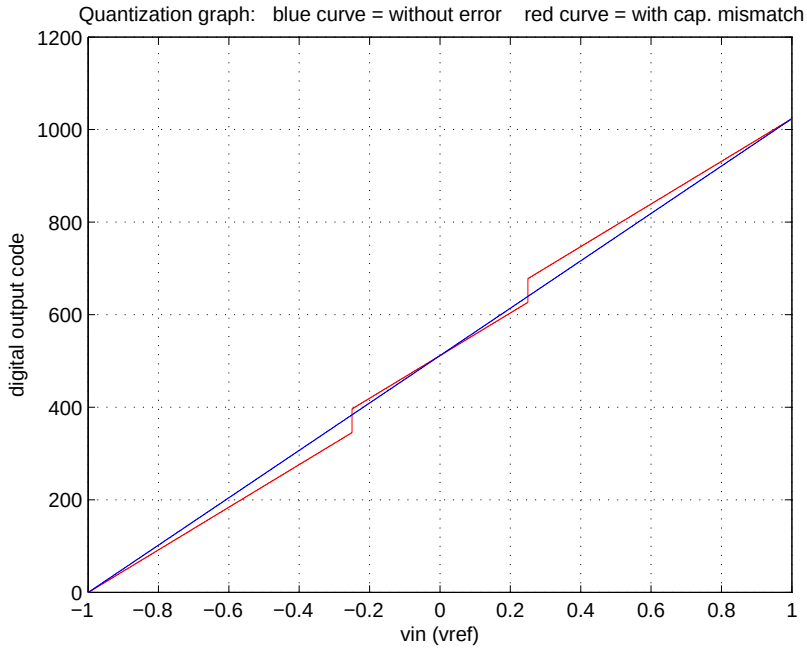

Figure 2.15: Residue of the first and second 1.5 bit stage with capacitor mismatch

$$THD(dB) = 10 \cdot log\left(\frac{V1^2}{V2^2 + V3^2 + V4^2..}\right) \tag{2.18}$$

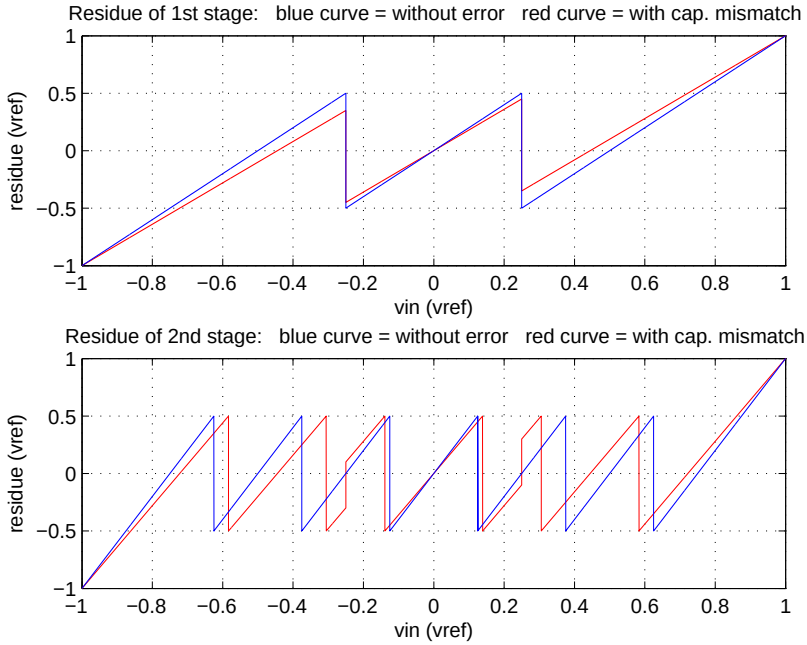

Figure 2.16: Residue of the first and second 1.5 bit stage with capacitor mismatch

2.3.5 Signal–to–Noise Ratio

The signal to noise ratio in dB corresponds for an ADC:

$$SNR(dB) = 1.76 + 6.02 \cdot N \tag{2.19}$$

N is the resolution of the ADC.

2.3.6 Signal–to–Noise and Distortion Ratio

Another important specific value is the signal-to-noise and distortion ratio (SNDR) which contains the distortion and thermal noise of a system. There the signal is referred to all unwanted components up to fs/2.

$$SNDR(dB) = 10 \cdot log\left(\frac{V1^2}{V2^2 + V3^2 + V4^2.. + \frac{V_{LSB}^2}{12} + thermalnoise}\right) \tag{2.20}$$

2.4 Summary of Basics

In this chapter the discretisation of signals in time and amplitude was explained. Moreover the pipeline ADC and its error sources were discussed where the first stage is the most critical part of this ADC.

3

MDAC 1.5 Bit with Dual Path Amplification

This chapter introduces and analyzes *dual path amplification (DPA)*, an analog error compensation technique for MDAC stages. After introducing the DPA technique, the transfer functions are derived, and the following error sources are discussed:

finite DC gain,

capacitor mismatch,

noise sources, and

offset voltage.

The precision of the analog output voltage, the residue V_2, and the compensation for the error caused by *finite DC gain* are analyzed. With DPA it is possible to use a simple miller op-amp with low DC gain instead of a cascaded op-amp or feedback loop, and complex digital compensation is not required. It is also shown that the DPA MDAC behaves similarly to a SPA MDAC regarding *capacitor mismatch, noise sources*, and *offset voltage* on op-amps.

The analytical considerations use approximations. The results are verified in a Matlab simulation.

The focus in this chapter is on a single stage of a pipeline ADC, on the 1.5 bit MDAC; the 2.5 bit DPA MDAC is discussed in Chapter 4.

3.1 Dual Path Amplification Technique and Topology

This section introduces the *dual path amplification* technique.

Figure 3.1 shows a 1.5 bit MDAC using DPA [1]. DPA uses two op-amps instead of one for the calculation of the residue: the *coarse* and the *fine* op-amp. The coarse op-amp produces a residue V_{2C} that is different from $V_{2C,ideal}$ because of a non-ideal op-amp. The fine op-amp is used to compensate for the error of the coarse op-amp. It performs the same operation as the coarse op-amp, and in addition subtracts the output V_{2C} of the coarse op-amp. The output of the fine op-amp V_{2F} is the negative error of the coarse op-amp. The desired *residue voltage*, V_2, is obtained by the sum of coarse and fine outputs.

$$V_2 = V_{2C} + V_{2F} \tag{3.1}$$

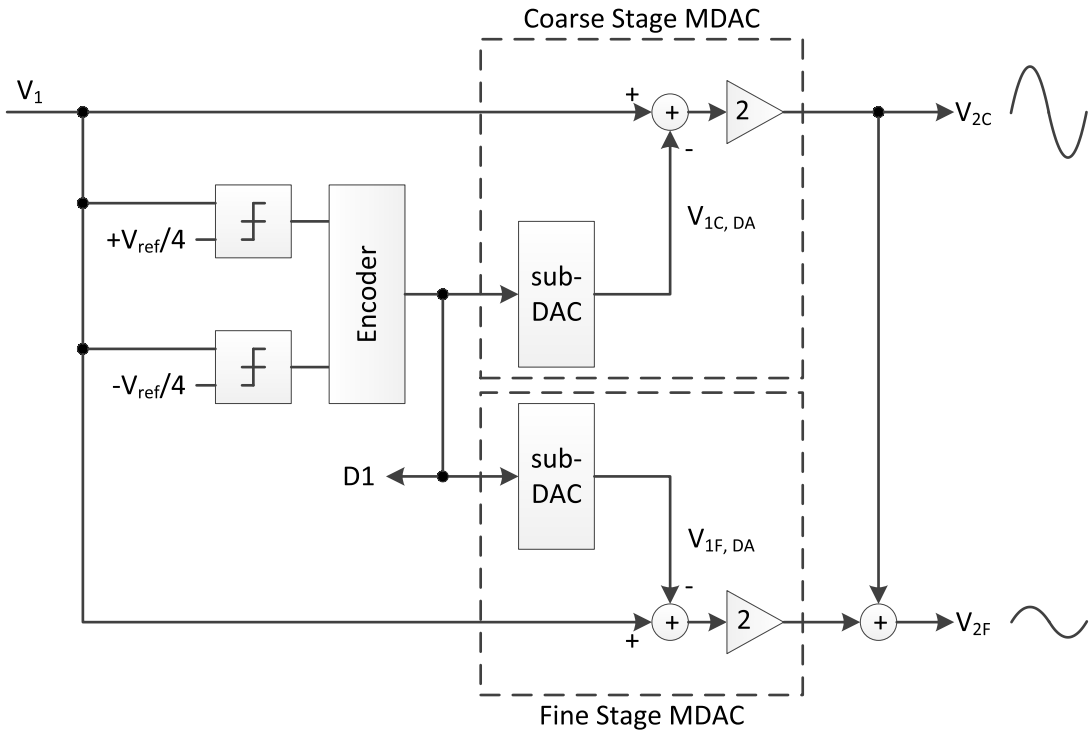

Figure 3.1: MDAC stage with dual path amplification architecture

Thus, the errors of the coarse op-amp are compensated for by the fine op-amp. The fine op-amp determines the accuracy and noise performance of the MDAC, but only needs to generate a small-swing signal.

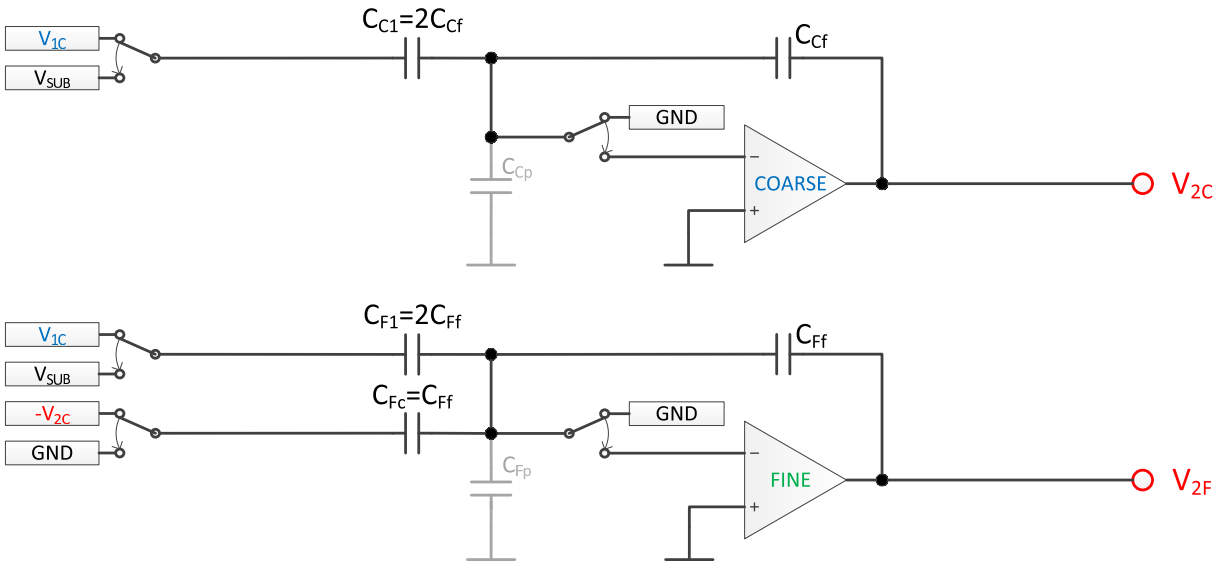

Figure 3.2: Schematic of the 1st pipeline stage of dual path amplification in sampling mode, 1.5 bit MDAC

The MDAC in the 1*st* pipeline stage must be treated differently from the 2*nd* stage MDAC (and all following stages).

First stage. Figure 3.2 shows the schematic of a 1*st* stage MDAC with DPA in sampling mode. The architecture investigated in this thesis is *non-flip around*, i.e., the feedback capacitor is fixed. This brings advantages for the settling behavior of the MDAC. In sampling mode, the

input voltage V_{1C} is loaded on capacitors C_{C1} and C_{F1}. The coarse output voltage V_{2C} is loaded to C_{Fc}. In amplification mode, the op-amp loop is closed. The inputs at C_{C1} and C_{F1} are connected with V_{sub}; the input at C_{Fc} is connected with ground. V_{sub} is the output of sub-DAC realized by a multiplexer, it is calculated by

$$V_{sub} = D_{out} \cdot \frac{V_{ref}}{2} \tag{3.2}$$

for this architecture.

Note that the capacitors C_{C1} and C_{F1} are two times larger than the feedback capacitance, i.e., $C_{C1} = 2C_{F1}$, $C_{F1} = 2C_{Ff}$. This causes a gain of 2 for V_{1C} and V_{1F} sampled on the capacitors as well as for V_{sub} connected to the capacitors during the amplification phase. The coarse output voltage -V_{2C} is transferred with gain 1 to the fine output V_{2F}. The coarse output yields

$$V_{2C} = 2\,(V_{1C} - V_{sub}) + V_{err,C} \tag{3.3}$$

where $V_{err,C}$ is the deviation from the ideal residue $V_{2,ideal}$:

$$V_{err,C} = V_{2C} - V_{2,ideal} \tag{3.4}$$

Also the fine stage is not ideal and produces an error $V_{err,F}$. The fine output is calculated by

$$\begin{aligned} V_{2F} &= 2\,(V_{1C} - V_{sub}) - V_{2C} + V_{err,F} \\ &= 2\,(V_{1C} - V_{sub}) - \{2\,(V_{1C} - V_{sub}) + V_{err,C}\} + V_{err,F} \\ &= -V_{err,C} + V_{err,F} \end{aligned} \tag{3.5}$$

With (3.1) the residue voltage of the 1*st* stage is obtained as:

$$V_2 = V_{2C} + V_{2F} = 2\,(V_{1C} - V_{sub}) + V_{err,F} = V_{2,ideal} + V_{err,F} \tag{3.6}$$

Second stage. The 2*nd* MDAC stage has two inputs, V_{2C} and V_{2F}, which are added in the MDAC. The schematic of the 2*nd* MDAC stage is depicted in Figure 3.3. Note that capacitors

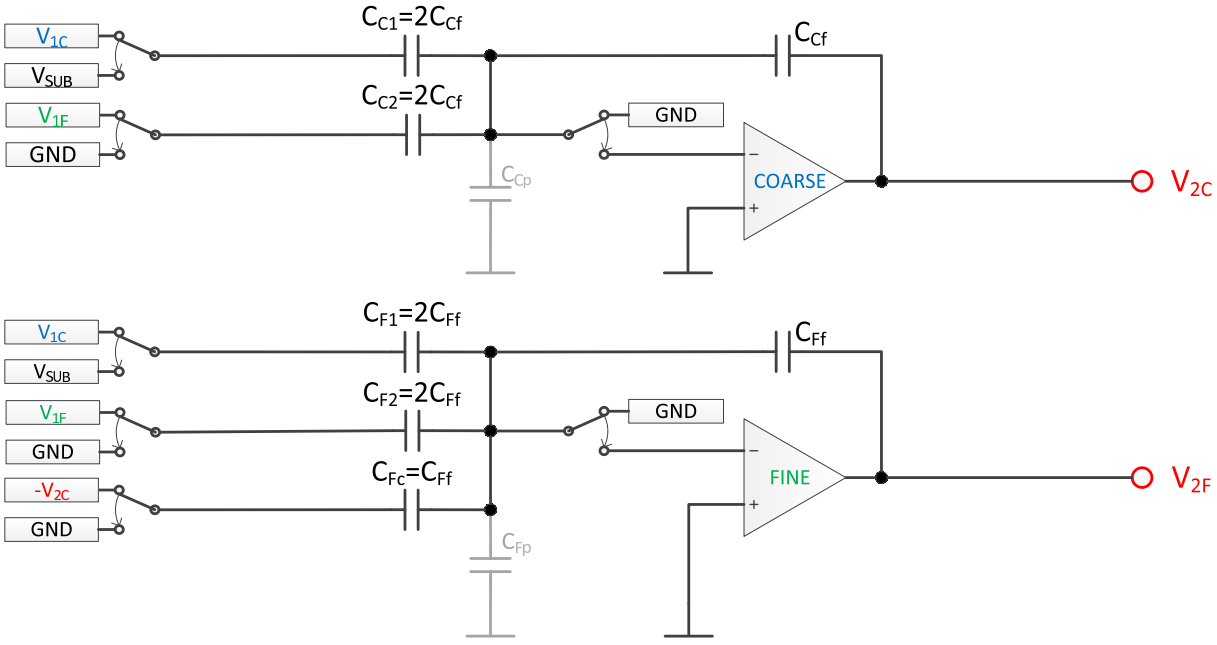

Figure 3.3: Schematic of the 2nd pipeline stage of dual path amplification in sampling mode, 1.5 bit MDAC

C_{C1}, C_{C2}, C_{F1}, and C_{F2} have twice the capacitance of the feedback capacitor, and $C_{Fc} = C_{Ff}$ are the same size. The coarse output of the $2nd$ MDAC stage can be calculated by

$$V_{2C} = 2\,(V_{1C} + V_{1F} - V_{sub}) + V_{err,C} \tag{3.7}$$

the fine output is obtained by

$$V_{2F} = 2\,(V_{1C} + V_{1F} - V_{sub}) - V_{2C} + V_{err,F} \tag{3.8}$$

The residue voltage of the $2nd$ stage is computed as:

$$V_2 = V_{2C} + V_{2F} = V_{2,ideal} + V_{err,F} \tag{3.9}$$

Note that the output of the $2nd$ coarse stage and the output of the $1st$ coarse stage are required for the fine stage and are sampled on the capacitors C_{Fc} and C_{F1}. As a consequence, the capacitor C_{F1} must be sampled during the amplification phase of the fine stage. Two capacitor sets are required.

3.2 Transfer Functions

The Matlab model is based on *transfer functions* describing the input-output behavior of MDAC stages. In this section the transfer functions are derived. Assuming the MDAC is a linear system, the impact of inputs on the system can be considered in isolation, and the outputs added together (additivity property). As the MDAC with DPA is a Multiple Input Multiple Output (MIMO) system, it has a transfer function from each input to each output.

3.2.1 Derivation of Basic Relations

This section shows the basic equations for calculating the transfer functions of MDAC. First the transfer function of a voltage V_{1C} is calculated; second the transfer function of a voltage V_{sub} applied during the amplification phase on the MDAC is treated. In the following sections the transfer functions of the $1st$ stage and the $2nd$ stage DPA MDAC are discussed.

To obtain the transfer function from a voltage sampled on capacitor C_{C1} to the output of the MDAC, consider the coarse stage of the $1st$ MDAC depicted in Figure 3.2. When the transfer function from the sampled voltage V_{1C} to the output V_{2C} is derived, V_{sub} is assumed to be zero. Figure 3.4 illustrates the calculation on a schematic. The input voltage V_{1C} is sampled on

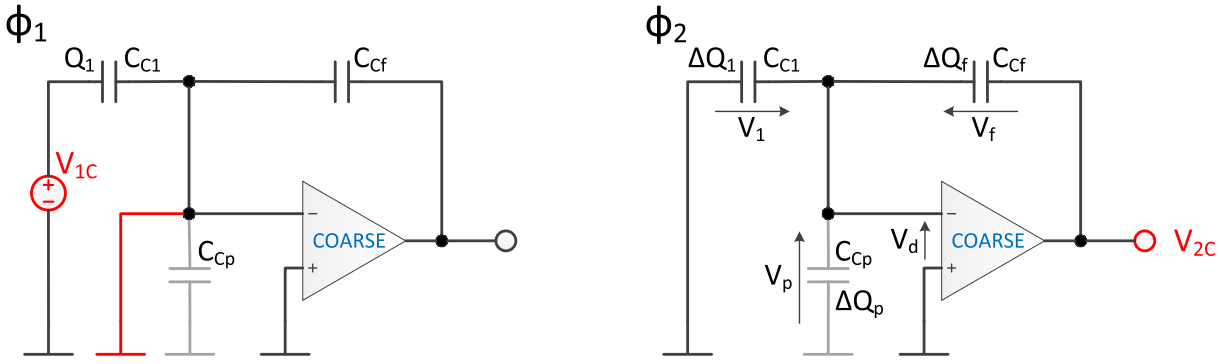

Figure 3.4: Right: sampling phase Φ_1, left: amplifying phase Φ_2

capacitor C_{C1} during Φ_1. The charge on C_{C1} during Φ_1 is:

$$Q_1 = V_{1C} C_{C1} \tag{3.10}$$

The ground connection is removed from the negative op-amp input and C_{C1} is connected to ground during the amplification phase Φ_2. This causes a difference V_d between positive and negative op-amp inputs and results in the output voltage

$$V_{2C} = V_d G_C \tag{3.11}$$

where G_C describes the transfer function of the op-amp. The charge Q_1 is now shifted to C_{Cf}. The op-amp has finite open loop gain and V_d is not equal to zero. Therefore some charge is also on C_{Cp} and C_{C1}. The sum of the charges on the capacitors C_{C1}, C_{Cf}, and C_{Cp} is:

$$Q_1 = \Delta Q_1 + \Delta Q_f + \Delta Q_p \tag{3.12}$$

The charges on the capacitors are

$$\Delta Q_1 = C_{C1} V_d, \qquad \Delta Q_f = C_{Cf}(V_{2C} + V_d), \qquad \Delta Q_p = C_{Cp} V_d. \tag{3.13}$$

Using (3.11) and summing up equations (3.13) yields:

$$\Delta Q_1 + \Delta Q_f + \Delta Q_p = \frac{V_{2C} C_{C1} + V_{2C} C_{Cp} + V_{2C} C_{Cf}}{G_C} + V_{2C} C_{Cf} \tag{3.14}$$

Using (3.12) and (3.10) yields:

$$V_{C1} C_{C1} = V_{2C} \frac{C_{C1} + V_{2C} C_{Cp} + V_{2C} C_{Cf}}{G_C} + C_{Cf} \tag{3.15}$$

After a few conversions the desired transfer function is obtained:

$$\frac{V_{2C}}{V_{1C}} = T_{CC} = \frac{C_{C1}}{\frac{C_{C1} + C_{Cf} + C_{Cp}}{G_C} + C_{Cf}} \tag{3.16}$$

Lets move on to the transfer function of a subtraction voltage V_{sub} applied during the amplification phase Φ_2 on the MDAC input. It is $V_{sub} = V_{ref}/2$ because $C_{C1} = 2C_{Cf}$. Figure 3.5 shows the schematic of the coarse stage of a 1.5 bit MDAC. Only the subtraction voltage V_{sub} is considered as an input. All capacitors are assumed to have zero charge at the beginning of the amplification phase, thus

$$\Delta Q_1 + \Delta Q_f + \Delta Q_p = 0. \tag{3.17}$$

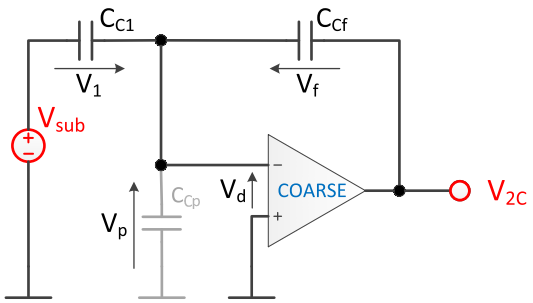

Figure 3.5: Transfer of V_{sub} to the coarse output, amplifying phase Φ_2

The op-amp now tries to balance its positive and negative inputs according to (3.11). The

charges on the capacitors are given by

$$\Delta Q_f = C_{Cf}(V_{2C} + V_d), \qquad \Delta Q_1 = C_{C1}(V_{sub} + V_d), \qquad \Delta Q_p = C_{Cp}V_d. \tag{3.18}$$

According to (3.17) the sum of all charges must be zero, and V_d can be substituted using (3.11). We obtain now the equation between V_{sub} and V_{2C} :

$$\frac{V_{2C}C_{C1} + V_{2C}C_{Cp} + V_{2C}C_{Cf}}{G_C} + V_{2C}C_{Cf} + V_{sub} = 0 \tag{3.19}$$

After a few conversions the transfer function is obtained:

$$\frac{V_{2C}}{V_{sub}} = T_{subC} = \frac{-C_{C1}}{\frac{C_{C1}+C_{Cf}+C_{Cp}}{G_C} + C_{Cf}} \tag{3.20}$$

Compared to the transfer function of the sampled voltage it can be seen that T_{CC} and T_{subC} differ only in the sign. The finite open loop gain and the parasitic capacitance are considered with a disruptive term added in the denominator of the transfer functions. It is the sum of all involved capacitors in the wiring of the op-amp divided by the transfer function G of the op-amp. This term vanishes if the open loop gain of the op-amp is driven towards infinity.

3.2.2 1st MDAC stage

The disruptive term for the coarse stage is according to (3.16) and (3.20):

$$H_{C,1st} = \frac{\Sigma C_{C,1st}}{G_C} = \frac{C_{C1} + C_{Cp} + C_{Cf}}{G_C} \tag{3.21}$$

The fine stage has one additional capacitor. The disruptive term yields:

$$H_{F,1st} = \frac{\Sigma C_{F,1st}}{G_F} = \frac{C_{F1} + C_{Fc} + C_{Fp} + C_{Ff}}{G_F} \tag{3.22}$$

The transfer functions of the coarse stage describe the impact of input signals on the coarse output. The transfer function of the coarse input voltage V_{1C} is:

$$T_{CC} = \frac{V_{2C}}{V_{1C}} = \frac{C_{C1}}{\frac{\Sigma C_{C,1st}}{G_C} + C_{Cf}} \tag{3.23}$$

The transfer function of subtraction voltage V_{sub} is:

$$T_{subC} = \frac{V_{2C}}{V_{sub}} = \frac{-C_{C1}}{\frac{\Sigma C_{C,1st}}{G_C} + C_{Cf}} \tag{3.24}$$

The transfer functions of the fine stage describe the impact of input signals on the fine output. The transfer function of the coarse input voltage V_{1C} is:

$$T_{CF} = \frac{V_{2F}}{V_{1C}} = \frac{C_{F1}}{\frac{\Sigma C_{F,1st}}{G_F} + C_{Cf}} \tag{3.25}$$

The transfer function of subtraction voltage V_{sub} is:

$$T_{subF} = \frac{V_{2F}}{V_{sub}} = \frac{-C_{F1}}{\frac{\Sigma C_{F,1st}}{G_F} + C_{Cf}} \tag{3.26}$$

The transfer function of the coarse output voltage V_{2C} to the fine output is:

$$T_{2CF} = \frac{V_{2F}}{V_{2C}} = \frac{-C_{F2}}{\frac{\Sigma C_{F,1st}}{G_F} + C_{Cf}} \tag{3.27}$$

All partial outputs of the coarse MDAC stage can be superposed to obtain V_{2C} :

$$V_{2C} = \frac{C_{C1}(V_{1C} - V_{sub})}{\frac{\Sigma C_{C,1st}}{G_C} + C_{Cf}} \tag{3.28}$$

The output of fine MDAC stage is obtained by:

$$V_{2F} = \frac{C_{F1}(V_{1C} - V_{sub}) - C_{Fc}V_{2C}}{\frac{\Sigma C_{F,1st}}{G_F} + C_{Ff}} \tag{3.29}$$

Assuming an ideal MDAC with $G = \infty$ and $C_{C1} = C_{Cf}$ we get the following simple equation:

$$V_{2C} = 2(V_{1C} - V_{sub}) \tag{3.30}$$

$$V_{2F} = 2(V_{1C} - V_{sub}) - V_{2C} \tag{3.31}$$

3.2.3 2nd MDAC stage

At the $2nd$ MDAC, coarse and fine stage have additional capacitors C_{C2} and C_{2F} for the fine input V_{1F}. The schematic is shown in Figure 3.3. The disruptive terms are given by:

$$H_{C,2nd} = \frac{\Sigma C_{C,2nd}}{G_C} = \frac{C_{C1} + C_{C2} + C_{Cp} + C_{Cf}}{G_C} \tag{3.32}$$

$$H_{F,2nd} = \frac{\Sigma C_{F,2nd}}{G_F} = \frac{C_{F1} + C_{C2} + C_{Fc} + C_{Fp} + C_{Ff}}{G_F} \tag{3.33}$$

In the following, the transfer functions of the $2nd$ 1.5 bit MDAC stage are introduced. The transfer functions of the coarse stage describe the relationship between the input signals and the coarse output. The transfer function of the coarse input voltage V_{1C} is:

$$T_{CC} = \frac{V_{2C}}{V_{1C}} = \frac{C_{C1}}{\frac{\Sigma C_{C,2nd}}{G_C} + C_{Cf}} \tag{3.34}$$

The transfer function of subtraction voltage V_{sub} is:

$$T_{subC} = \frac{V_{2C}}{V_{sub}} = \frac{-C_{C1}}{\frac{\Sigma C_{C,2nd}}{G_C} + C_{Cf}} \tag{3.35}$$

The transfer function of the fine input voltage V_{1F} is:

$$T_{FC} = \frac{V_{2C}}{V_{1F}} = \frac{C_{C3}}{\frac{\Sigma C_{C,2nd}}{G_C} + C_{Cf}} \tag{3.36}$$

The transfer functions of the fine stage describe the relationship between the input signals and the fine output. The transfer function of the coarse input voltage V_{1C} is:

$$T_{CF} = \frac{V_{2F}}{V_{1C}} = \frac{C_{F1}}{\frac{\Sigma C_{F,2nd}}{G_F} + C_{Ff}} \tag{3.37}$$

The transfer function of subtraction voltage V_{sub} is:

$$T_{subF} = \frac{V_{2F}}{V_{sub}} = \frac{-C_{F1}}{\frac{\Sigma C_{F,2nd}}{G_F} + C_{Ff}} \tag{3.38}$$

The transfer function of the coarse input voltage V_{1F} is:

$$T_{FF} = \frac{V_{2F}}{V_{1F}} = \frac{C_{F3}}{\frac{\Sigma C_{F,2nd}}{G_F} + C_{Ff}} \tag{3.39}$$

The transfer function of the coarse output voltage V_{2C} to the fine output is:

$$T_{2CF} = \frac{V_{2F}}{V_{2C}} = \frac{-C_{F2}}{\frac{\Sigma C_{F,2nd}}{G_F} + C_{Ff}} \tag{3.40}$$

The output as a function of the inputs of the MDAC is

$$V_{2C} = \frac{C_{C1}(V_{1C} - V_{sub} + C_{C2}V_{1F}}{\frac{\Sigma C_{C,2nd}}{G_C} + C_{Cf}} \tag{3.41}$$

for the coarse state, and

$$V_{2F} = \frac{C_{F1}(V_{1C} - V_{sub}) + C_{C2}V_{1F} - C_{Fc}V_{2C}}{\frac{\Sigma C_{F,2nd}}{G_F} + C_{Ff}} \tag{3.42}$$

for the fine state. These equations are the basis of the Matlab simulations in this thesis performed for MDAC stages and for the pipeline ADC. Assuming an ideal MDAC, the functions can be simplified to:

$$V_{2C} = 2(V_{1C} + V_{1F} - V_{sub}) \tag{3.43}$$

$$V_{2F} = 2(V_{1C} + V_{1F} - V_{sub}) - V_{2C} \tag{3.44}$$

3.3 Finite DC Gain

The *finite DC gain* of the op-amps, as described in Section 2.3.3, causes a gain error at the MDAC. The error is proportional to the output of the MDAC. This will be shown in the following for the SPA and for the DPA MDAC. Furthermore, the relationship between the errors resulting from the finite DC gain and the loop gain will be investigated. The analytical considerations will be completed with simulation results.

3.3.1 Analytical Considerations

The transfer functions of a 1.5 bit SPA MDAC are shown in (3.23) and (3.24), they correspond to the coarse stage of the DPA MDAC. The settling behavior is ignored for these considerations, and the transfer function of the op-amp is assumed to be a constant $G_{op} = A_0$. The ideal gain of the MDAC is corrupted by the additional disruptive term (3.21) in the denominator. This causes a gain error that is the same for all inputs. The residue error is shown in Figure 3.6.

Assuming an ideal matching $C_{C1} = 2C_{Cf}$, the input to output equation shown in (3.28) can

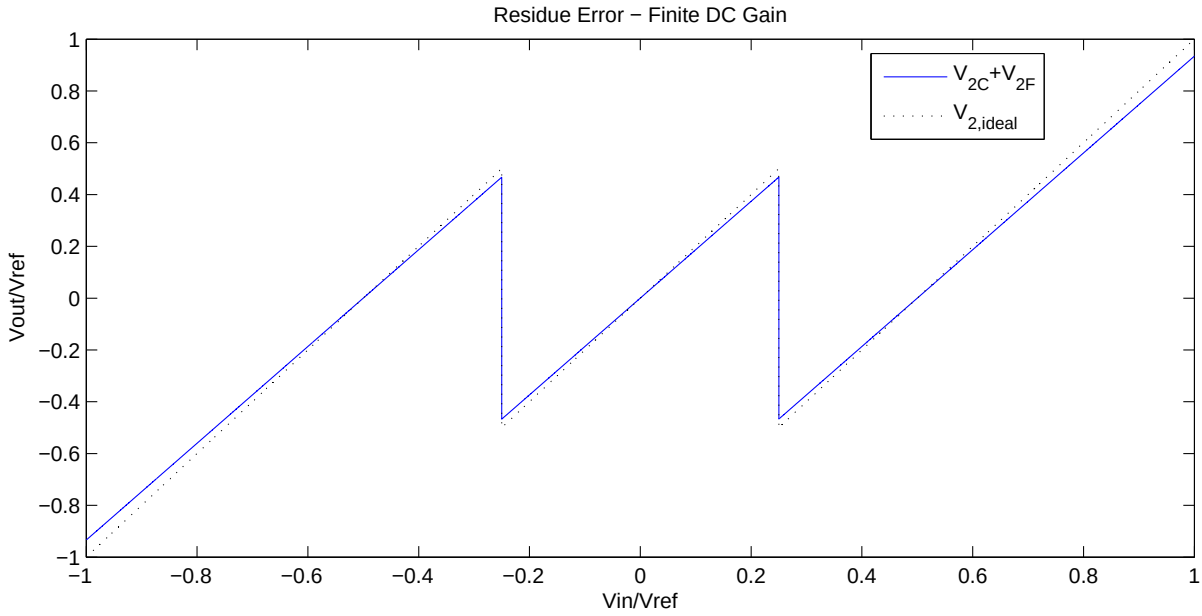

Figure 3.6: Ideal residue (gray dashed) and residue with error (blue) of 1st stage, 1.5 bit MDAC with DPA

be written as:

$$V_{2C} = 2V_{1C}(1-\alpha) - 2V_{sub}(1-\alpha) = V_{2,ideal}(1-\alpha) \tag{3.45}$$

where α is the gain error of the MDAC and

$$(1-\alpha) = \frac{C_{Cf}}{\frac{\Sigma C_{C,1st}}{A_{0C}} + C_{Cf}} \tag{3.46}$$

Considering the MDAC with DPA of Figure 3.2, the fine stage also has the same gain error for all inputs,

$$V_{2F} = 2V_{1C}(1-\beta) - 2V_{sub}(1-\beta) - V_{C2}(1-\beta) = (V_{2,ideal} - V_{2C})(1-\beta), \tag{3.47}$$

where β is the gain error of the fine MDAC stage. The factor $(1-\beta)$ can be expressed by:

$$(1-\beta) = \frac{C_{Ff}}{\frac{\Sigma C_{F,1st}}{A_{0F}} + C_{Ff}} \tag{3.48}$$

The sum of coarse and fine output yields:

$$\begin{aligned} V_{2C} + V_{2F} &= (V_{2,ideal} - V_{2,ideal}(1-\alpha))(1-\beta) + V_{2,ideal}(1-\alpha) \\ &\quad ... \\ &= V_{2,ideal}(1-\alpha\beta) \end{aligned} \tag{3.49}$$

Figure 3.7 illustrates the MDAC as a system with feed forward amplification A_0. The transfer

function (3.23) can be written as:

$$T_{CC} = \frac{V_{2C}}{V_{1C}} = \frac{C_{C1}}{C_{C1} + C_{Cp} + C_{Cf}} \quad \frac{A_{0C}}{1 + \frac{C_{Cf}}{C_{C1}+C_{Cp}+C_{Cf}} A_0}$$
$$= \frac{C_{C1}}{\Sigma C_{C,1st}} \quad \frac{A_{0C}}{1 + \frac{C_{Cf}}{\Sigma C_{C,1st}} A_{0C}} \tag{3.50}$$

Introducing loop gain L_C, the transfer function T_{CC} is:

$$T_{CC} = \frac{C_{C1}}{\Sigma C_{C,1st}} \quad \frac{A_{0C}}{1 + L_C} \tag{3.51}$$

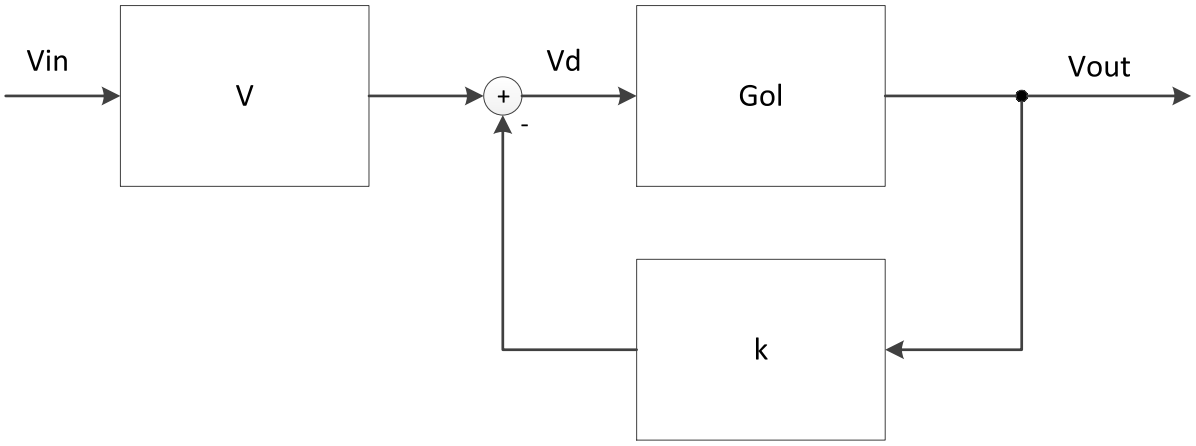

Figure 3.7: MDAC as a system: 1.5 bit 1st stage, SPA

There is a connection between loop gain L_C and gain error α:

$$(1 - \alpha) = \frac{C_{Cf}}{\frac{\Sigma C_{C,1st}}{A_{0C}} + C_{Cf}} = \frac{\Sigma C_{C,1st} + C_{Cf} A_{0C}}{\Sigma C_{C,1st} + C_{Cf} A_{0C}} + \frac{-\Sigma C_{C,1st}}{\Sigma C_{C,1st} + C_{Cf} A_{0C}}$$
$$\approx 1 - \frac{\Sigma C_{C,1st}}{C_{Cf} A_{0C}} = 1 - \frac{1}{L_C} \tag{3.52}$$

The gain errors α and β can be approximated with:

$$\alpha \approx \frac{1}{L_C} \qquad \beta \approx \frac{1}{L_F} \tag{3.53}$$

Consequently, the gain error of the overall MDAC output $V_{2C} + V_{2F}$ yields [1]:

$$\alpha\beta \approx \frac{1}{L_C L_F} \tag{3.54}$$

The output of the coarse stage can then be expressed as:

$$V_{2C} \approx V_{2,ideal}(1 - \frac{1}{L_C}) \tag{3.55}$$

Using (3.49) the overall output of the MDAC yields:

$$V_2 = V_{2C} + V_{2F} \approx V_{2,ideal}(1 - \frac{1}{L_C L_F}) \tag{3.56}$$

3.3.2 Simulation Results

To evaluate the performance of the MDAC corrupted by *finite DC gain*, a Matlab model was implemented using the transfer functions introduced in Section 3.2. Capacitor mismatch and other error sources were ignored. The model of the MDAC shown in Figure 3.2 contains parasitic capacitors C_{Cp} and C_{Fp} at the input of the op-amp. This is because the parasitic capacitor influences the loop gain of the MDAC, as shown in Section 3.3.1. Moreover there are also errors such as noise and offset, not only the error caused by finite DC gain. All errors should be below $\pm LSB_{12}/4$ to get 12 bit resolution but in our case a larger error is allowed. Table 3.1 shows the contribution of pipeline stages to the input referred residual error and requirement for the error on the output of the MDAC stage. The sum of all residual errors (3.57) converges to $LSB/2$.

$$\frac{LSB}{2} = \sum_{i=1}^{N} \frac{LSB}{2 \cdot 2^i} \tag{3.57}$$

Table 3.1: Accumulation of residue errors

Stage number	1	2	3	4	5	...
Input referred error	$\frac{LSB}{4}$	$\frac{LSB}{8}$	$\frac{LSB}{16}$	$\frac{LSB}{32}$	$\frac{LSB}{64}$	...
Error at MDAC output	$\frac{LSB}{2}$	$\frac{LSB}{2}$	$\frac{LSB}{2}$	$\frac{LSB}{2}$	$\frac{LSB}{2}$	...

According to (3.57) only the last stage can be scaled for a residual error within $LSB/2$. The allowed residue error at the output of the MDAC was assumed to be $LSB_{12}/2$ according to Table 3.1. The simulation algorithm looked for $\{A_{0C}, A_{0F}\}$ pairs to get a maximum residue error of exactly $\pm LSB/2$.

$$|V_{2,ideal} - (V_{2C} + V_{2F})|_{max} = \frac{LSB}{2} \tag{3.58}$$

Figure 3.8 shows the DC gain of the coarse op-amp versus on the DC gain of the fine op-amp for different resolutions to meet constraint (3.58). The parasitic capacitor is assumed to be equal to the feedback capacitor for both coarse and fine stage:

$$C_{Cp} = C_{Cf}$$
$$C_{Fp} = C_{Ff}$$

Using the same DC gain for coarse and fine op-amp, with 12 bit resolution the DC gain is:

$$A_{0C} = A_{0F} = 49\,\text{dB} \tag{3.59}$$

7 The sum of both is 98 dB. An SPA MDAC requires DC gain $A_0 = 84.3$ dB for the same residue error. Moving on the black continuous curve of Figure 3.8 by 10 dB to the left or to the right, the sum of DC gains keeps nearly constant. For $A_{0F} = 60$ dB, coarse DC gain $A_{0C} = 37.2$ is needed. It yields a sum of 97.2 dB. Moving further, the sum decreases. The distance between the curves is approximately 6 dB. This is because of the factor of 2 for the LSB of different resolutions. Figure 3.8 (below) shows the linear dependency of DC gain on the resolution for an SPA MDAC.

The dependency of the DC gain on the parasitic capacitor can be seen in Figure 3.9. The parasitic capacitor of coarse and fine stage are assumed to be the same related to the respective feedback capacitor. A parasitic capacitor of C_{xf} costs 4.4 dB if $A_{0C} \approx A_{0F}$. A parasitic capacitor of $2C_{xf}$ costs only 7.9 dB. This is due to loop gain L, which is not proportional to C_{xp}, but to $(C_{xp} + C_{x1} + C_{xf})^{-1}$.

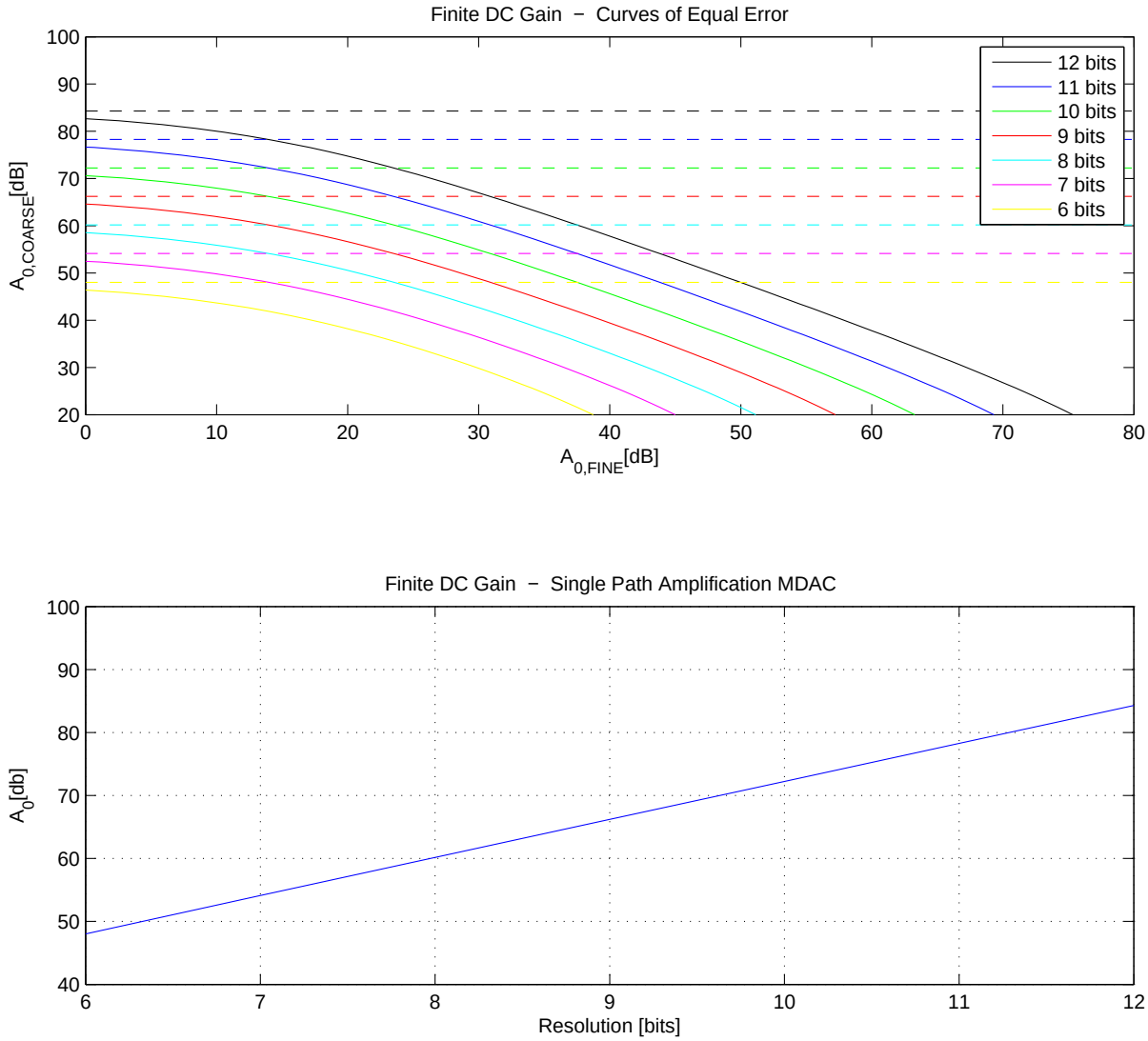

Figure 3.8: Above: Constant error LSB/2 on MDAC output, 1.5 bit MDAC, 1st stage. Continuous lines: DPA MDAC, dashed lines: SPA MDAC. Below: Open-loop gain that produces LSB/2 on MDAC output, dependent on ADC resolution. 1.5 bit SPA MDAC, 1st stage

In Figure 3.10, the impact of the parasitic capacitance on the coarse and fine stage are illustrated separately. It can be seen that parasitic capacitor of $C_{Cp} = 2C_{Cf}$ on the coarse stage has more impact on the residue error than $C_{Fp} = 2C_{Ff}$ on the fine stage. The reason is again the relationship between parasitic capacitor and the sum of input capacitors that appear in loop gain L.

Remember that in Section 3.3.1 the gain error was approximated to show the relationship between gain error and loop gain (3.56). Figure 3.11 compares the approximation with the simulation using exact transfer functions. It can be seen that the approximation features the worst case: the blue curve is always above the magenta curve. Furthermore it can be seen that it is a linearization for the exact behavior at $A_{0C} \approx A_{0F}$.

Figure 3.12 compares the topology of the $1st$ MDAC stage with the topology of the $2nd$ or a following MDAC stage. The output of each MDAC stage was forced to be $LSB/2$. The $2nd$ MDAC stage has additional capacitors C_{C2} and C_{F2} for the input of the fine signal V_{1F}. This decreases the feedback factor k and thus open-loop gain L. With $C_{xp} = C_{xf}$ and $A_{0C} \approx A_{0F}$, the distance between the curves on the x-axis is 6.4 dB. This means that the $2nd$ MDAC stage has stronger requirements regarding DC gain because of its different topology.

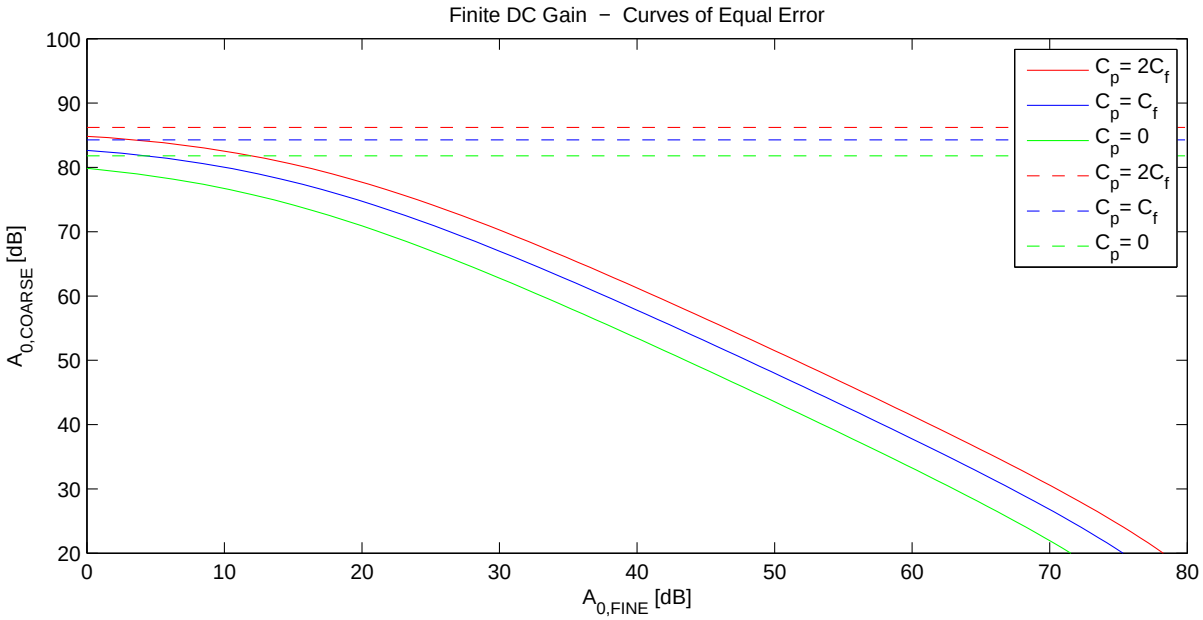

Figure 3.9: Impact of parasitic capacitor, coarse and fine stage have the same parasitic capacitor related to their feedback capacitor. 1.5 bit MDAC, 1st stage

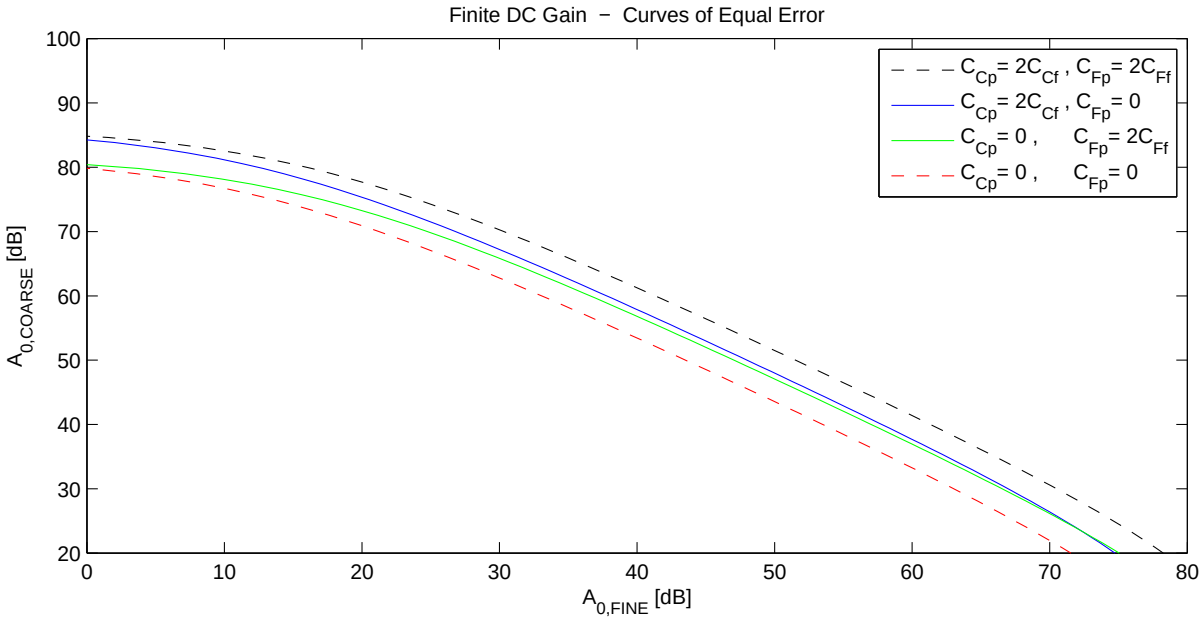

Figure 3.10: Parasitic capacitor at coarse stage vs. parasitic capacitor at fine stage, 1.5 bit MDAC, 1st stage

The most important findings about the error introduced by the finite DC gain are:

The error is proportional to the MDAC output for both SPA and DPA MDAC. This means that the greatest absolute error is always obtained for the inputs $\pm V_{ref}$.

The error is approximately proportional to the loop gain of the MDAC for SPA and to the product of both loop gains for DPA. Thus also the product $A_{0C} \cdot A_{0F}$ is proportional to the error. It must be higher than 98 dB to keep the error below $LSB/2$ for the $1st$ stage DPA MDAC of a 12 bit ADC.

The error decreases with increasing feedback factor k_X and with increasing DC gain A_0X.

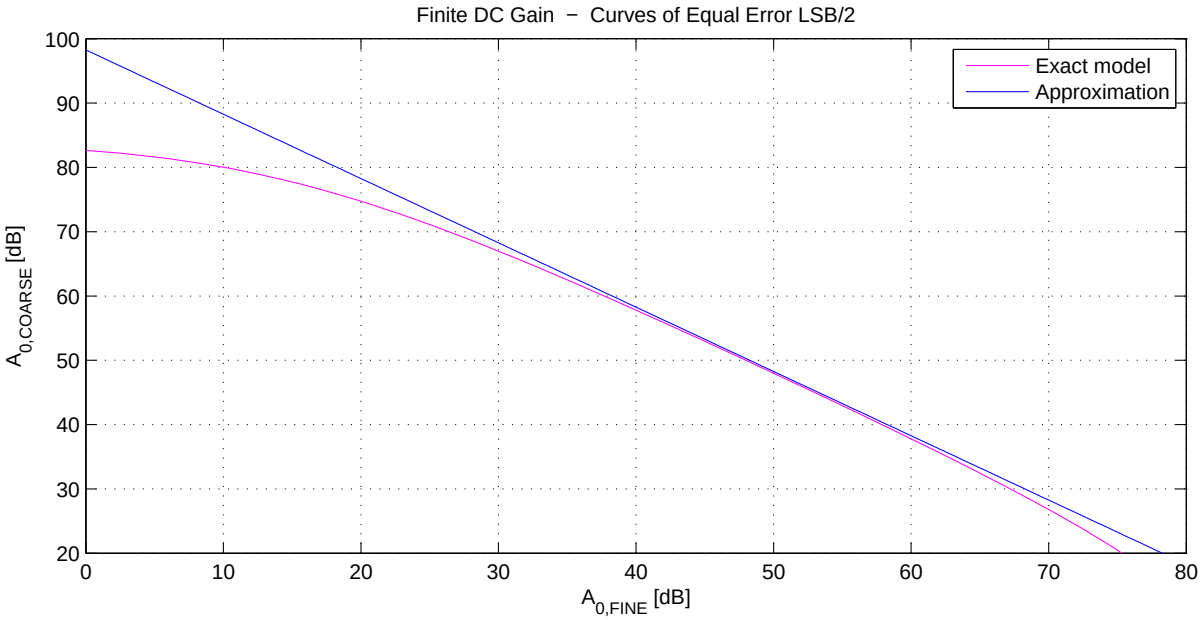

Figure 3.11: Open loop gain for constant error LSB/2 calculated with transfer function (magenta) and with the approximation: $\alpha = 1/(L_C L_F)$ [1](blue).

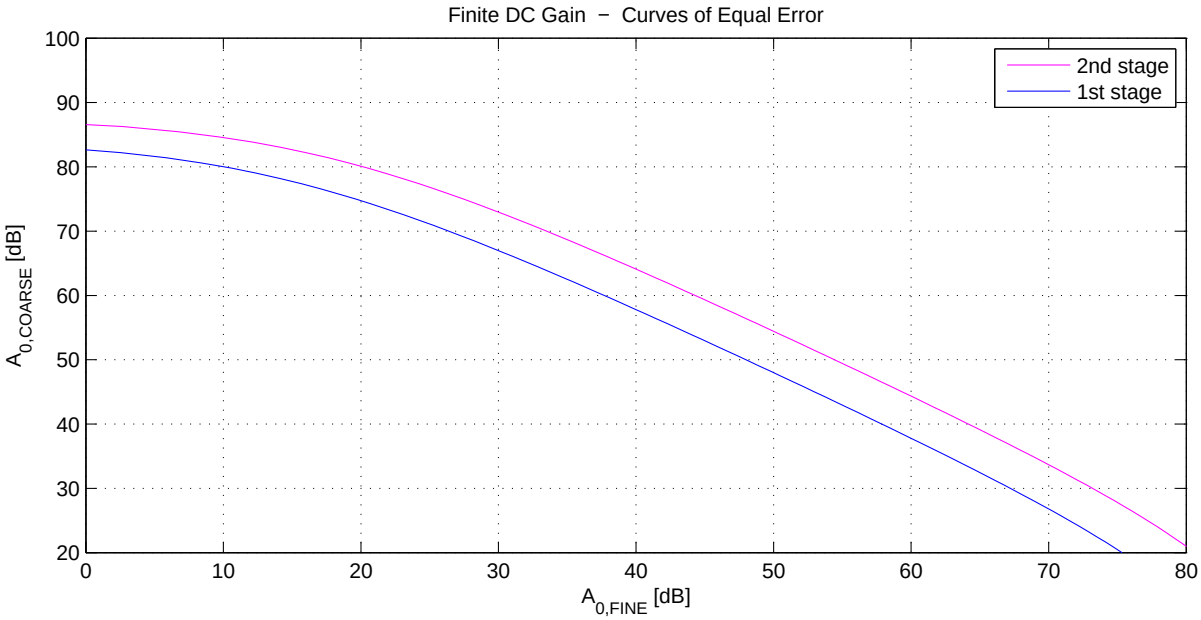

Figure 3.12: Comparison of 1st and 2nd MDAC stage, 1.5 bit MADC

The feedback factor is the ratio of feedback capacitor C_{xf} and all capacitors involved in the op-amp wiring. More capacitors involved in relation to C_{xf} yield a larger error.

3.4 Capacitor Mismatch

The capacitor mismatch affects the precision of the MDAC residue. The gain for each single input signal is adjusted by capacitor ratios. The capacitor mismatch of the 40 nm technology has a minimum at about 200 fF and cannot be improved by increasing the capacitance. This is

visible from the simulation result in Figure 3.13, there is a minimum for mismatch. The residue error caused in the fine stage cannot be compensated by DPA. The mismatch error is depending on the used topology, which is shown in this section.

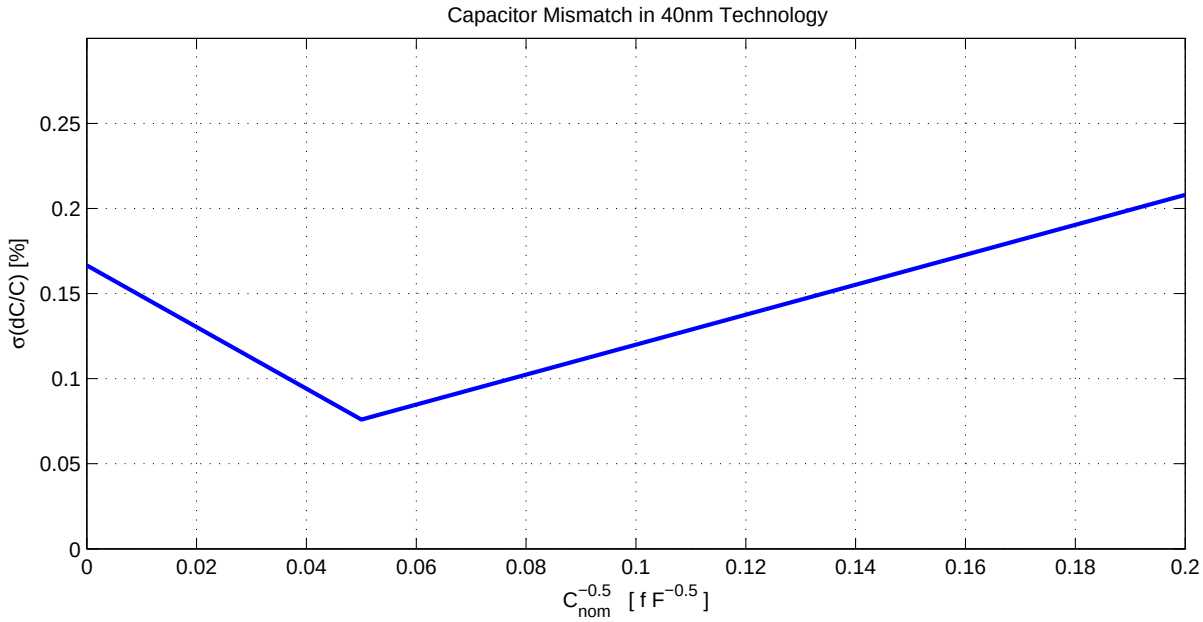

Figure 3.13: Capacitor mismatch for CMOS 40 nm technology, Spice simulation

In the following analytical part the residue error caused by capacitor mismatch will be approximated. The analytic approximation will be evaluated with a simulation using a Matlab model.

3.4.1 Analytical Considerations

Capacitor mismatch σ_c is the relative deviation of two capacitors from each other:

$$\sigma_c = \sigma \left\{ \frac{2(C_1 - C_2)}{C_1 + C_2} \right\} \tag{3.60}$$

The capacitor mismatch is Gaussian distributed, and capacitors vary statistically independent from each other. The capacitor mismatch can be written as the squared sum of the deviations σ_{abs} from the nominal values of C_1 and C_2:

$$\sigma_c = \sqrt{\sigma_{abs}^2 + \sigma_{abs}^2} = \sqrt{2}\,\sigma_{abs} \tag{3.61}$$

The deviation σ_{abs} from the nominal value is:

$$\sigma_{abs} = \frac{1}{\sqrt{2}} \cdot \sigma_c \tag{3.62}$$

This value is suitable for analytical considerations and for introducing the capacitor mismatch into the Matlab model.

Consider the schematic of a 1.5 bit SPA MDAC stage shown in Figure 3.14. Each capacitor is normally distributed around its nominal value C_{nom} with the standard deviation $C_{nom} \cdot \sigma_{abs}$. It can be written as:

$$C = C_{nom}\,(1 + \epsilon), \tag{3.63}$$

where ϵ is a Gaussian distributed random variable with zero mean and standard deviation σ_{abs}. Assuming an ideal op-amp, the MDAC output can be approximated by:

$$V_2 = \frac{V_1 \cdot C_1(1+\epsilon_1) - V_{sub} \cdot C_1(1+\epsilon_1)}{C_f(1+\epsilon_f)} = \frac{2\,(V_1 - V_{sub})\,(1+\epsilon_1)}{(1+\epsilon_f)}$$
$$\approx 2(V_1 - V_{sub}) \cdot (1 + \epsilon_1 - \epsilon_f - \epsilon_1\epsilon_f) \approx 2(V_1 - V_{sub}) \cdot (1 + \epsilon_1 - \epsilon_f)$$

$$V_2 \approx V_{2,ideal} \cdot (1 - (\epsilon_f - \epsilon_1)) \tag{3.64}$$

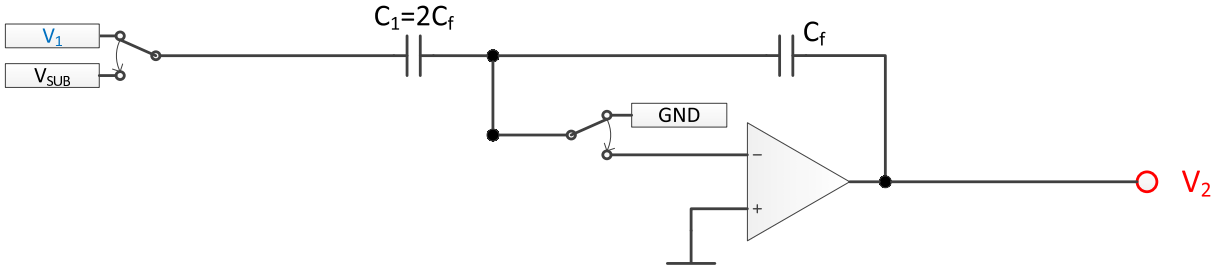

Figure 3.14: Schematic of 1st pipeline stage, 1.5 bit MDAC, with single path amplification (SPA)

The resulting error can be approximated as gain error $(\epsilon_f - \epsilon_1)$. This gain error is also Gaussian distributed with standard deviation

$$\sigma\{\epsilon_1 - \epsilon_f\} = \sqrt{\sigma_{abs}^2 + \sigma_{abs}^2} = \sqrt{2} \cdot \sigma_{abs}. \tag{3.65}$$

The residue of an MDAC with capacitor mismatch is depicted in Figure 3.15. The deviation of the capacitors is overdrawn to make the effect visible. The ideal residue is denoted by the dashed line. The largest error occurs at $V_1 = 1$. Assuming a 12 bit ADC and a mismatch $\sigma_c = 0.1\,\%$, the residue error has a standard deviation

$$\sigma\{V_2 - V_{2,ideal}\} = 1 \cdot \sqrt{2}\,\frac{1}{\sqrt{2}}\sigma_c = 0.001 = 2.0\,LSB_{12}. \tag{3.66}$$

Lets look at the error made by the 1.5 bit DPA MDAC depicted in Figure 3.2. The residue error of the coarse stage is compensated, while the errors made by the fine stage are affecting the residue. To keep calculations simple, the coarse stage is assumed to be ideal:

$$V_{2C} = V_{2,ideal} = 2\,(V_{1C} - V_{sub}) \tag{3.67}$$

The fine stage would then produce zero output if it was ideal. Since the fine stage suffers from mismatch, the output of the fine stage is equal to the residue error. No parasitic capacitor appears since ideal op-amps are assumed.

$$V_{2F} = (V_{1C} - V_{sub}) \cdot \frac{C_{F1}(1+\epsilon_{F1})}{C_{Ff}(1+\epsilon_{Ff})} - V_{2C} \cdot \frac{C_{Fc}(1+\epsilon_{Fc})}{C_{Ff}(1+\epsilon_{Ff})}$$

$$= 2\,(V_{1C} - V_{sub}) \left(\frac{(1+\epsilon_{F1})}{(1+\epsilon_{Ff})} - \frac{(1+\epsilon_{Fc})}{(1+\epsilon_{Ff})} \right)$$

$$V_{2F} \approx V_{2,ideal}(\epsilon_{F1} - \epsilon_{FC}) \tag{3.68}$$

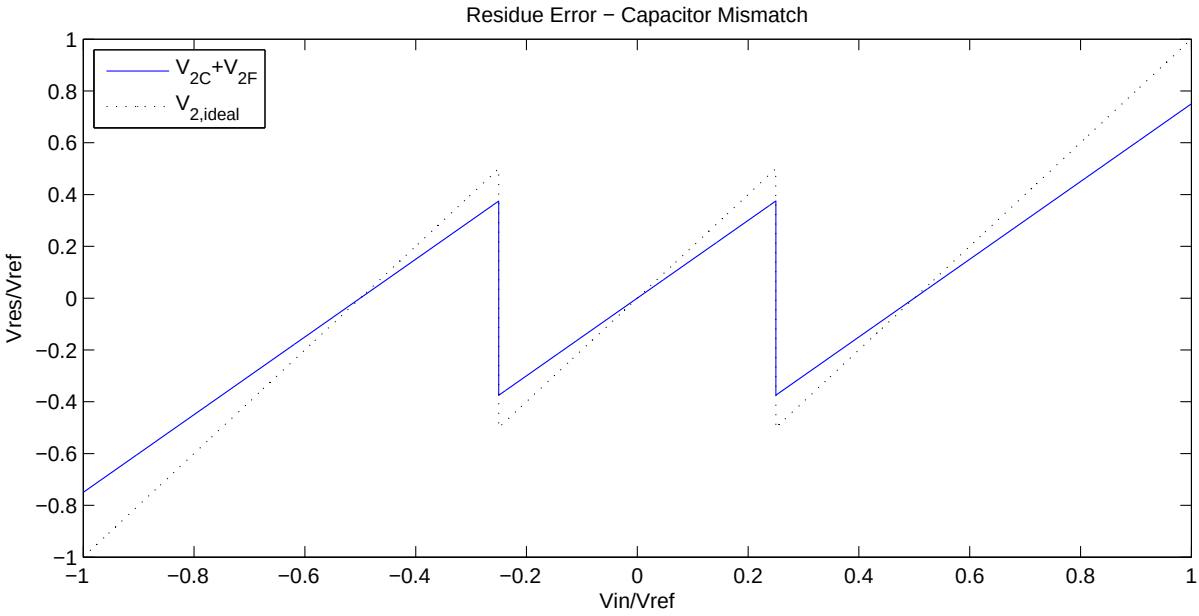

Figure 3.15: Residue of 1.5 bit DPA MDAC with capacitor mismatch (continuous line), ideal residue (dashed line)

The overall residue is calculated by:

$$V_2 = F_{2F} + V_{2C} \approx V_{2,ideal}(1 - (\epsilon_{FC} - \epsilon_{F1})) \tag{3.69}$$

It can be seen that the *gain error* $(\epsilon_{Fc} - \epsilon_{F1})$ is constant, because the residue error is proportional to $V_{2,ideal}$. It has a standard deviation of:

$$\sigma\{\epsilon_{FC} - \epsilon_{F1}\} = \sqrt{\sigma_{abs}^2 + \sigma_{abs}^2} = \sqrt{2}\,\sigma_{abs} \tag{3.70}$$

This corresponds to the result obtained for the SPA MDAC.

3.4.2 Simulation Results

To evaluate the analytical results and to get more details, the DPA MDAC is simulated in Matlab. All capacitors of the MDAC are deviated randomly with Gaussian distribution and standard deviation $\sigma_{abs} = \frac{1}{\sqrt{2}}\sigma_c$, according to the mismatch σ_c. The simulation is performed with 10^3 different capacitor sets and with 10^3 input samples. It yields a distribution of 10^6 residue values. As shown in Section 3.4.1, residue errors are approximately Gaussian distributed. For plotting the results, the standard deviation of the residue errors is calculated.

Figure 3.16 shows the residue error at the output of an SPA MDAC with the black dashed line. It is depicted dependent on input voltage V_{1C} that is normalized by the reference voltage V_{ref}. The shape of the error is piecewise linear. It has kinks at the thresholds of the comparator at ± 0.25 and at the points where the error is crossing zero at ± 0.5 and 0. This is in line with the analytic result (3.64) that claims constant gain error. The magenta curve shows the residue error of a DPA MDAC with the topology of a $1st$ pipeline stage. The topology of a $2nd$ pipeline stage is shown with a dashed, magenta line. The two curves match exactly. This result is not surprising because the simulation assumes that the fine input of the $2nd$ stage is zero. The additional capacitors C_{2C} and C_{2F} of the $2nd$ pipeline stage produce errors due to a finite DC gain (cf. Section 3.3.2). However, with the assumption of an ideal op-amp and

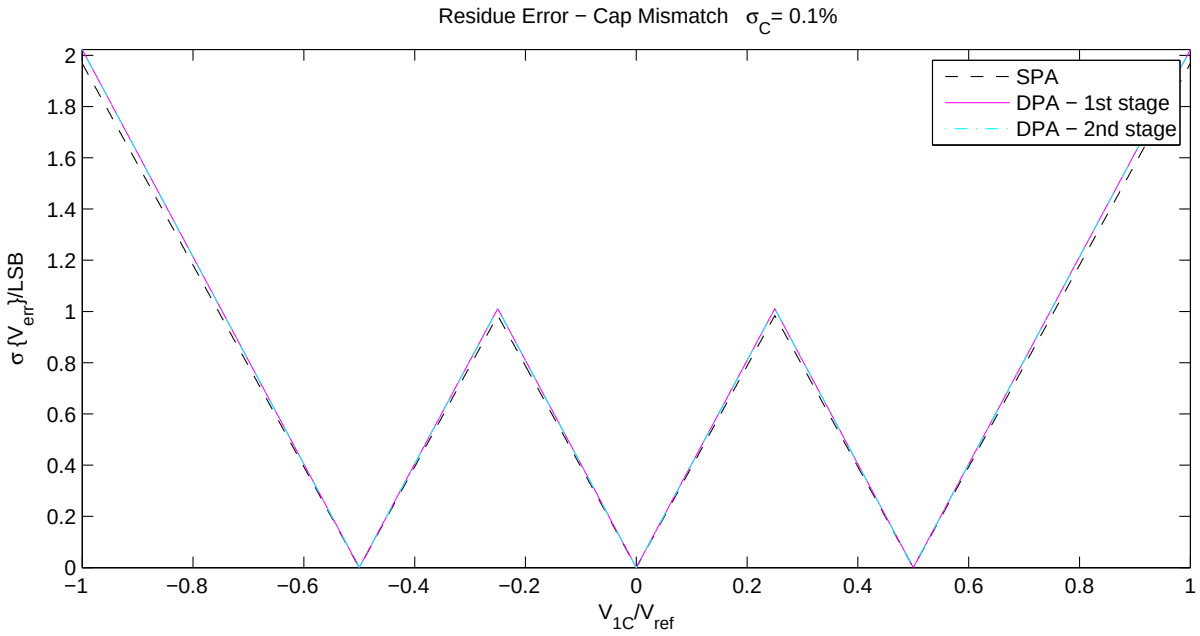

Figure 3.16: Residue Error of 1.5 bit MDAC. Black dashed line: SPA MDAC, magenta line: 1st stage DPA MDAC, cyan line: 2nd stage DPA MDAC. Standard deviation of the error is shown versus input of MDAC

no inputs applied to C_{2C} and C_{2F}, they do not influence the residue error. Fine input V_{1F} can be assumed to be small compared to coarse input V_{1C}, therefore it is ignored. Looking at the maximum values for the residue error at $V_{1C}/V_{ref} = \pm 1$, it can be seen that the standard deviation of the error is about $2\,LSB$ for 12 bit ADC resolution. This matches well the analytic approximation (3.66). Some simplifications are performed in the analytical approximation SPA MDAC and DPA MDAC show the same standard deviation of gain error in (3.70) and (3.65). Looking at the simulation results in Figure 3.16, the largest difference between SPA MDAC and DPA MDAC occurs at $V_{1C}/V_{ref} = \pm 1$ and is only $0.05\,LSB$. Considering the gain of 2 of the 1.5 bit MDAC, the standard deviation of the input referred error e_{in} for a 12 bit ADC with 0.1 % mismatch is $\sigma\{e_{in}\} = 1\,LSB$.

Figure 3.17 shows the impact of the coarse and the fine stage to the residue error. The standard deviation of the residue error is normalized with LSB_{12} and is plotted versus the normalized input voltage of the MDAC. The blue line displays that the residue error is zero, if a mismatch appears only in the coarse stage and the fine stage is ideal. This is obviously taking into account that the fine stage corrects errors of the coarse stage. If the fine stage is assumed to be ideal, all errors can be corrected. The green curve and the dashed black curve show that the MDAC produces the same residue error when the mismatch is only at the fine stage and when the mismatch is on each side, the fine and the coarse stage. This result is very interesting. It shows a very good error rejection for mismatch errors of the coarse stage, even if the fine stage is affected by capacitor mismatch. It also confirms the assumption of the ideal coarse stage made for the analytical calculations in Section 3.4.1 about the mismatch errors of the DPA MDAC.

Figure 3.18 shows the residue error of the DPA MDAC versus the capacitor mismatch σ_c. The simulation was performed with 10^3 uniformly distributed input samples $V_{1C} \sim \mathcal{U}[-1, 1]$ and 10^3 capacitor sets, where each capacitor is independently varied with $C \sim \mathcal{N}(C_{nom}, \sigma^2_{abs})$. The standard deviation of all residue errors iss calculated. Other than Figure 3.17 and Figure 3.16, Figure 3.18 shows the $3\,\sigma$ value of the residue error. Assuming Gaussian distribution of the residue error, 99.7 % of the residue errors are inside the $3\,\sigma$ limits. This is a representative value for the worst case. The blue continuous line in Figure 3.18 shows the residue error for

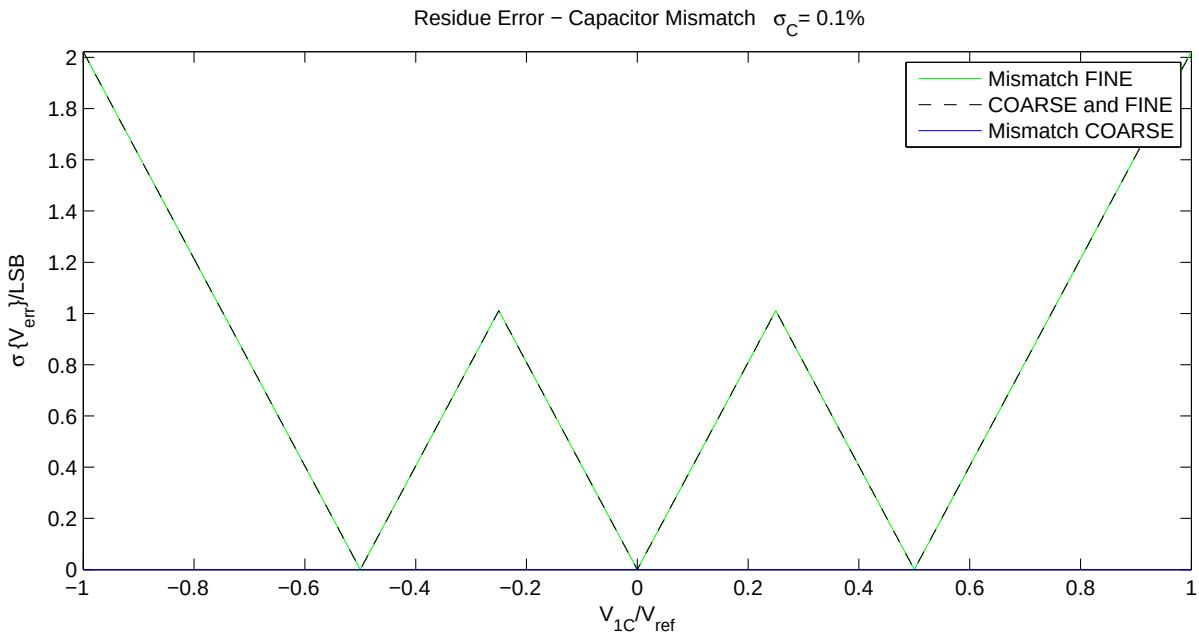

Figure 3.17: Residue Error of 1.5 bit DPA MDAC. Green line: Mismatch only on capacitors of fine stage, coarse stage is ideal. Black dashed line: Mismatch on all capacitors of the MDAC. Blue line (on x-axis): Mismatch only on coarse stage, fine stage is ideal

a DPA MDAC normalized by LSB_{12}. It is very close to the black dashed curve for the SPA MDAC. The two curves differ only by 2.6 %. The DPA MDAC with $\sigma_c = 0.1\,\%$ mismatch has a residue error of $2.8\,LSB$. This corresponds to $1.4\,LSB$ referred to the input of the MDAC. With this error in the $1st$ stage, it is not possible to achieve an effective resolution of 12 bits for the ADC. Assuming the best possible mismatch value of $\sigma_c = 0.076\,\%$ for this 40 nm technology (cf. Figure 3.13), the input referred residue error is given by $1.06\,LSB$. According to Table 3.1, each MDAC stage must have a residue error of less than $\pm LSB/2$ at the output to reach an input referred residue error of $\pm LSB/2$ for the overall ADC. This constraint would only be fulfilled for a 12 bit ADC with mismatch as low as $\sigma_c = 0.036\,\%$.

These results show that the capacitor mismatch is limiting the resolution of the 1.5 bit MDAC to approximately 10.5 bits. This is valid for MDACs with DPA as well as with SPA. The DPA technique cannot compensate for the capacitor mismatch of the fine stage. To reach higher resolutions, it is necessary to choose other topologies. This is the main reason why the 2.5 bit MDAC is investigated in this thesis. The 2.5 bit MDAC has gain 4. The requirements for the residue error are relaxed by a factor 2 compared to the 1.5 bit MDAC. It will be shown that the mismatch requirements are relaxed for the 2.5 bit MDAC.

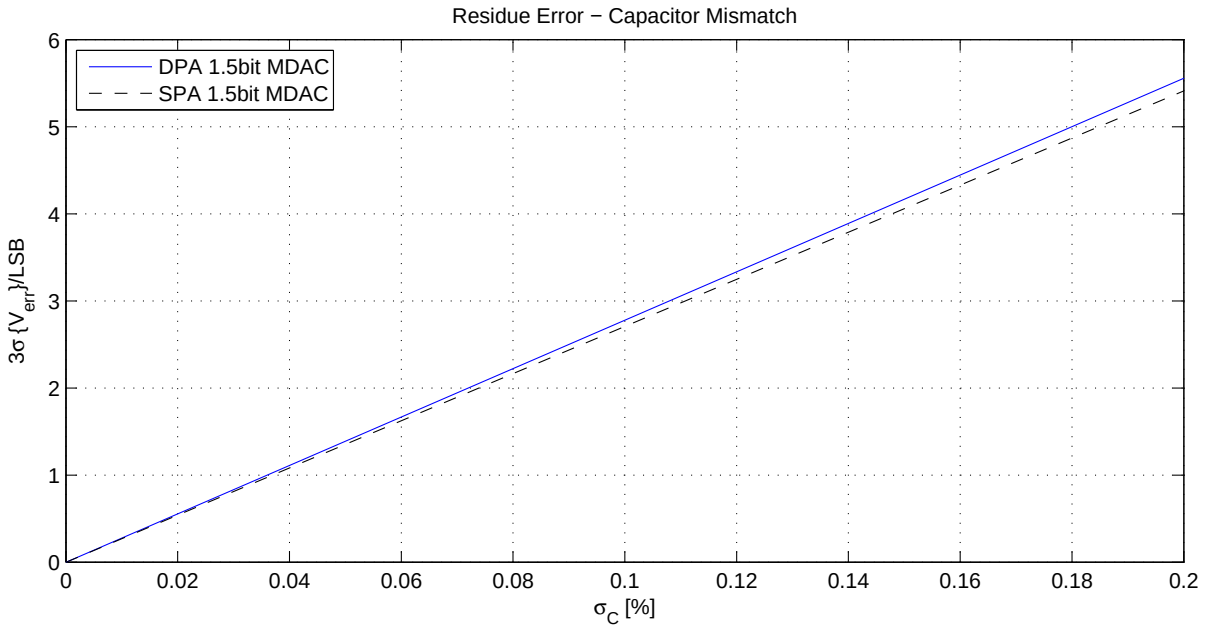

Figure 3.18: Residue Error of 1.5 bit MDAC with $\sigma_C = 0.1\,\%$ mismatch. Blue line: DPA MDAC 1st stage. Black dashed line: SPA MDAC. $3\,\sigma$ value of error distribution is depicted dependent on capacitor mismatch σ_c

3.5 Noise Sources

Noise is a random error. It is not systematic like capacitor mismatch and finite DC gain. Noise sources decrease the signal-to-noise ratio and the effective resolution of the ADC. In this section the following noise sources are discussed:

Noise produced by the switches is sampled on capacitors during each sampling phase. It is called kT/C noise.

The reference voltage V_{ref} is corrupted by noise.

The output of an op-amp is a noise source.

Analytical considerations are presented for the 1.5 bit DPA MDAC and compared to the SPA MDAC. Simulations were only performed for the overall ADC, the results are shown in Section 5.4.

3.5.1 Noise in the Coarse Stage of an MDAC

This section discusses the impact that noise on the coarse output V_{2C} has on the residue $V_2 = V_{2C} + V_{2F}$. It is shown analytically that the noise of the coarse stage can be ignored.

For a zero mean signal, the signal power corresponds to the variance σ^2. For linear systems with transfer function H, the output power of a signal is calculated by integrating its *spectral power density* multiplied with the square of the transfer function:

$$\nu_y^2 = \int_0^\infty S_{xy}(f) \cdot |H(f)|^2 df \tag{3.71}$$

For white noise, the spectral power density is not dependent on the frequency. Since the transfer function is not a function of the frequency, the equation can be simplified to:

$$\nu_y^2 = \sigma^2 \cdot |H|^2 \tag{3.72}$$

This equation will be used to represent noise considerations in the following discussion.

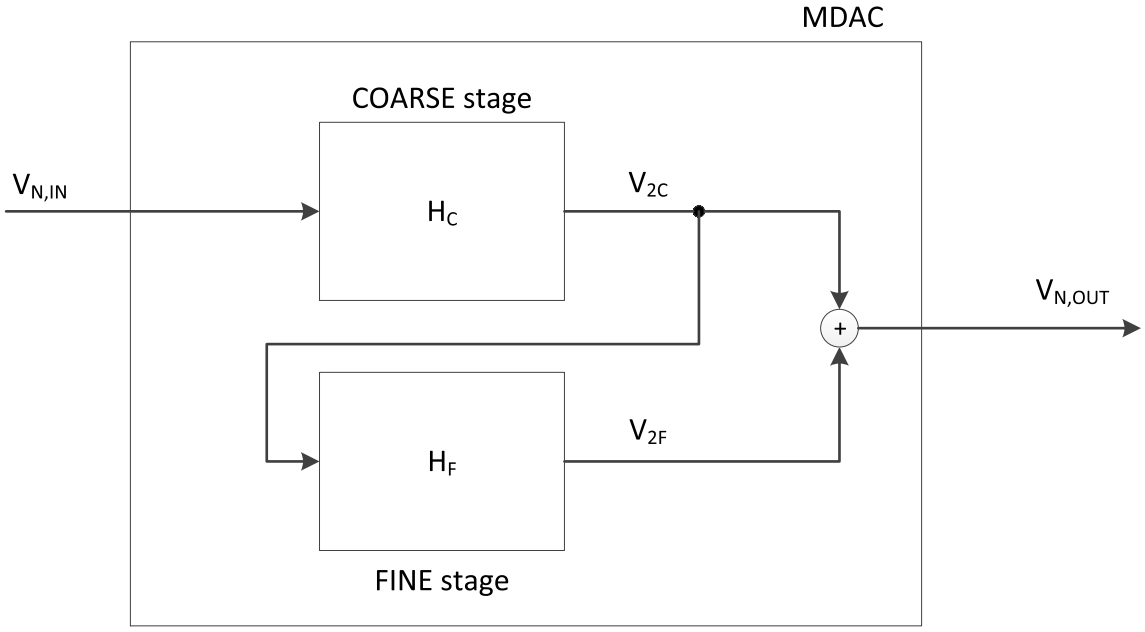

Figure 3.19: Block diagram of a DPA MDAC to analyze noise behavior of the coarse stage

Figure 3.19 shows a DPA MDAC with noise source $V_{N,IN}$ at the input of the coarse stage. H_C is the transfer function from the noise source to the coarse output V_{2C}. H_F is the transfer function from the input of the fine stage on capacitor C_{Fc} to the output of the fine stage V_{2F}. To get the impact of noise on the residue voltage $V_{N,OUT}$, outputs V_{2F} and V_{2C} are summed together. Now, the impact of noise V_{2C} produced by the coarse stage is investigated. V_{2C} is assumed to be Gaussian distributed with zero mean and standard deviation σ_{2C}.

$$V_{2C} \sim \mathcal{N}(0, \sigma_{2C}^2) \tag{3.73}$$

The transfer function from V_{2C} to $V_{N,OUT}$ is the sum of V_{2C} and V_{2F} divided by V_{2C}:

$$\frac{V_{N,OUT}}{V_{2C}} = 1 + H_F \tag{3.74}$$

The noise power ν_N^2 at the output of the MDAC is obtained by combining (3.72) and (3.74):

$$\nu_N^2 = \sigma_{2C}^2 \cdot |1 + H_F|^2 = \sigma_{2C}^2 \cdot (1 + 2H_F + H_F^2) \tag{3.75}$$

The gain error of the fine stage can be approximated according to (3.53) with $1/L_F$. The transfer function H_F can be written as ideal gain multiplied by one minus the gain error.

$$H_F \approx -1 \cdot \left(1 - \frac{1}{L_F}\right) \tag{3.76}$$

Combining (3.75) and (3.76), the noise power μ_N^2 yields:

$$\nu_N^2 = \sigma_{2C}^2 \cdot \left|1 - \left(1 - \frac{1}{L_F}\right)\right|^2 = \sigma_{2C}^2 \cdot \left|\frac{1}{L_F}\right|^2 = \sigma_{2C}^2 \cdot \frac{1}{L_F^2} \tag{3.77}$$

Noise sources in the coarse stage are reduced by a factor of $1/L_F$. Thus, the fine stage is the dominant noise source [1]. The following considerations will ignore noise from the coarse stage and focus on the noise from the fine stage.

3.5.2 kT/C Noise

In Section 2.1.3 the noise occurring in the sampling phase is described. In the sampling phase, shown in Figure 3.2, capacitors C_{F1} and C_{Fc} are loaded through a switch with resistance R_{ON}. This resistor produces thermal noise [7]:

$$\nu^2 = 4 \cdot k \cdot T \cdot R_{ON} \cdot \Delta f \tag{3.78}$$

Where k is the Boltzmann constant $1.38 \cdot 10^{-23} \frac{J}{K}$, T is temperature in Kelvin and Δf is the bandwidth of noise. The resistance of the switch and the capacitor build a lowpass filter with transfer function H_{LP}. The power density of the noise on the capacitor is the product of the squared absolute value of transfer function $|H_{LP}|^2$ and the squared absolute value of spectral density of noise $\nu^2/\Delta f$. The noise power σ_N is obtained by the integral of power density over frequency [8]:

$$\begin{aligned}
\nu_N^2 &= 4 \cdot k \cdot T \cdot R_{ON} \cdot \int_0^\infty \frac{1}{1 + (2\pi \cdot f \cdot R_{ON} \cdot C)^2}\, df \\
&= 4 \cdot k \cdot T \cdot R_{ON} \cdot \frac{1}{2\pi \cdot R_{ON} \cdot C} \cdot \frac{\pi}{2} \\
\nu_N^2 &= \frac{k \cdot T}{C}
\end{aligned} \tag{3.79}$$

The resistance cancels out in the calculation, the noise power is only dependent on capacitor C and on the temperature T.

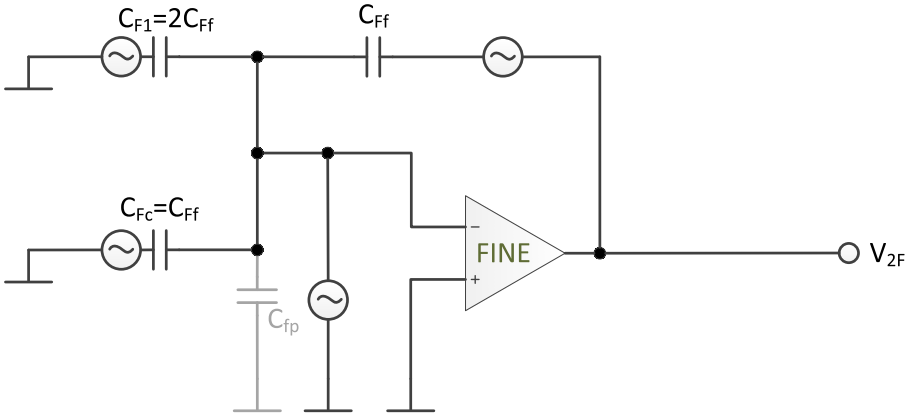

Figure 3.20: 1st fine MDAC stage. Noise sampled on the capacitors is denoted as voltage source

First stage. Figure 3.20 shows the fine stage of a 1*st* stage MDAC. The noise sampled on the capacitors is denoted as voltage source. It can be seen that each capacitor is connected with a noise source. The noise power at the MDAC output equals the noise power of the fine stage, as calculated in (3.80) [9].

$$\sigma_{2F}^2 = \frac{kT\,(C_{F1} + C_{Fc} + C_{Fp} + C_{Ff})}{C_{Ff}^2} = \frac{k\,T\,(4 + C_{Fp}/C_{Ff})}{C_{Ff}} \tag{3.80}$$

With the assumption that $C_{Fp} = C_{Ff}$ follows (3.81).

$$\sigma_{2F}^2 = \frac{5\,kT}{C_{Ff}} \tag{3.81}$$

The noise power is referred to the input of the ADC in (3.82).

$$\sigma_{in}^2 = \frac{5\,kT}{C_{Ff}} \cdot \left|\frac{1}{2}\right|^2 = \frac{5}{4}\,\frac{kT}{C_{Ff}} \tag{3.82}$$

Assuming the feedback capacitor to be 250 fF, and a temperature of $T = 20\,°C$, noise σ_{in} of the $1st$ stage yields:

$$\sigma_{in} = \sqrt{\frac{5 \cdot 1.38 \cdot 10^{-23}\,\frac{J}{K} \cdot 293.15\,K}{4 \cdot 250fF}} = 140\,\mu V \tag{3.83}$$

The input referred effective noise voltage is normalized by LSB_{12} in (3.84).

$$\frac{\sigma_{in}}{LSB_{12}} = \frac{0.14\,mV}{0.49 \cdot 10^{-3} \cdot V_{ref}} = \frac{0.29}{V_{ref}} \tag{3.84}$$

σ_{in} corresponds to $LSB_{12}/4$ if $V_{ref} = 1.16\,V$.

Second stage. The second fine stage is depicted in Figure 3.3. The second and all following fine stages have the capacitor C_{F2} in addition toC_{F1}, C_{Fc} and C_{Ff}, where C_{F2} is twice the size of the feedback capacitor C_{Ff}.

$$C_{F2} = 2 \cdot C_{Ff} \tag{3.85}$$

$\frac{kT}{C}$-noise power σ_{2F}^2 at the output of the $2nd$ stage is calculated in (3.86).

$$\sigma_{2F}^2 = \frac{kT\,(C_{F1} + C_{F2} + C_{Fc} + C_{Fp} + C_{Ff})}{C_{Ff}^2} = \frac{k\,T\,(6 + C_{Fp}/C_{Ff})}{C_{Ff}} \tag{3.86}$$

The noise power is referred to the input of the ADC in (3.87). The gain from the input of the ADC to the output of the $2nd$ MDAC stage is a factor of 4.

$$\sigma_{in}^2 = \frac{7\,kT}{C_f} \cdot \left|\frac{1}{4}\right|^2 = \frac{7}{4}\,\frac{kT}{C_{Ff}} \tag{3.87}$$

Assuming the feedback capacitor to be 250 fF, and a temperature of $T = 20\,°C$, noise σ_{in} of the $2nd$ fine stage yields:

$$\sigma_{in} = \sqrt{\frac{7 \cdot 1.38 \cdot 10^{-23}\,\frac{J}{K} \cdot 293.15\,K}{16 \cdot 250fF}} = 84\,\mu V \tag{3.88}$$

The input referred effective noise voltage is normalized by LSB_{12} in (3.89).

$$\frac{\sigma_{in}}{LSB_{12}} = \frac{84\,\mu V}{0.49 \cdot 10^{-3} \cdot V_{ref}} = \frac{0.17}{V_{ref}} \tag{3.89}$$

σ_{in} of the $2nd$ MDAC stage corresponds to $LSB_{12}/4$ if $V_{ref} = 0.68\,V$.

Single path amplification MDAC. The kT/C noise power of an SPA MDAC is given by [5]:

$$\sigma_{2C}^2 = \frac{kT\,(C_{C1} + C_{Cp} + C_{Cf})}{C_{Ff}^2} = \frac{k\,T\,(3 + C_{Fp}/C_{Ff})}{C_{F}f} \tag{3.90}$$

The same assumptions are made as in the DPA case. The feedback capacitor and the parasitic capacitor are assumed to be $C_{Cp} = C_{Cf} = 250\,\text{fF}$. The temperature is assumed to be $T = 20\,°C$. The noise power of the $1st$ SPA MDAC stage is referred to the input of the ADC in (3.91).

$$\sigma_{in} = \sqrt{\frac{4\,kT}{C_f} \cdot \left|\frac{1}{2}\right|^2} = \sqrt{\frac{1.38 \cdot 10^{-23}\,\frac{J}{K} \cdot 293.15\,K}{250fF}} = 127\,\mu V \tag{3.91}$$

σ_{in} corresponds to $LSB_{12}/4$ if $V_{ref} = 1.04\,V$.

It can be seen that the $1st$ stage of an SPA MDAC has a slightly better noise performance than the $1st$ stage of a DPA MDAC. This is because of the additional capacitor C_{Fc}.

3.5.3 Noise on Reference Voltage and Op-Amp Noise

V_{sub}, applied during the amplification mode, is not ideal. There is noise on it. The absolute value of the gain factor of the input voltage $V_{2C} + V_{2F}$ is the same as for the subtraction voltage V_{sub}. Therefore the noise power σ^2_{sub} of V_{sub} to the input referred noise power σ^2_{in} is:

$$\sigma^2_{in} = \sigma^2_{sub} \tag{3.92}$$

The dominant noise source of the op-amp is the transconductance g_m. It is calculated by the ratio of output current I_{ds} to input voltage V_{gs} [5].

$$g_m = \frac{\partial I_{ds}}{\partial V_{GS}} \tag{3.93}$$

The noise power ν caused by the op-amp is calculated by:

$$\nu = 4 \cdot k \cdot T \cdot \frac{2}{3} \cdot \frac{1}{g_m} \tag{3.94}$$

The transconductance g_m together with the capacitive load C_L on the output of the op-amp build a low pass filter. The calculation of the input referred noise power is the same as for kT/C-noise (cf. Section 3.5.2). The noise power σ^2_{out} at the output of the fine stage is:

$$\sigma^2_{out} = \frac{2}{3} \cdot \frac{k\,T}{C_L} \tag{3.95}$$

When referred to the MDAC input, the noise power σ^2_{out} is divided by the squared gain of the MDAC:

$$\sigma^2_{in} = \frac{2}{3} \cdot \frac{k\,T}{C_L} \cdot \left|\frac{1}{G}\right|^2 = \frac{1}{6} \cdot \frac{k\,T}{C_L} \tag{3.96}$$

Where C_L is the capacitive load of the op-amp and G is the gain of the op-amp. Note that the capacitive parasitic capacitor at the output of the op-amp is not considered in this consideration.

The capacitive load of the op-amp in the SPA MDAC consists of the feedback capacitor C_f and the input capacitor C_1 of the next MDAC stage. For simplicity there is no scaling of capacitors assumed. The capacitor C_1 of the next stage is twice the size of C_f. The capacitive load of the op-amp is:

$$C_L = C_f + C_1 = 3\,C_f \tag{3.97}$$

Input referred noise voltage σ_{in} is calculated in (3.98) using (3.97). It is dependent on the

feedback capacitor C_f.

$$\sigma_{in} = \sqrt{\frac{1}{6} \cdot \frac{k\,T}{3\,C_f}} = 0.24 \sqrt{\frac{k\,T}{C_f}} \tag{3.98}$$

The DPA MDAC has more capacitive load C_L on the fine op-amp compared to the capacitive load of the SPA MDAC. The capacitive load of the fine stage of the DPA MDAC is:

$$C_L = C_{Ff} + C_{C2} + C_{F2} = 5\,C_f \tag{3.99}$$

Note that the capacitive parasitic capacitor at the output of the op-amp is not considered in this consideration. Input referred noise voltage σ_{in} is calculated in (3.100).

$$\sigma_{in} = \sqrt{\frac{1}{6} \cdot \frac{k\,T}{5\,C_f}} = 0.18 \sqrt{\frac{k\,T}{C_f}} \tag{3.100}$$

If capacitors are not scaled, the first stage of a DPA ADC has the same capacitive load as the second stage and further stages. The results of (3.100) and (3.98) are valid for each MDAC input. To obtain the noise contribution to the input of the ADC it is necessary to scale the noise voltage σ_{in} according to the gain factor from the ADC input to the considered MDAC stage.

For the noise behavior of single MDAC stages, no simulations were performed due to time reasons. The noise behavior of the pipeline ADC using DPA MDAC was simulated with the Matlab model and is discussed in Section 5.4.

3.6 Offset Voltage

The real op-amp produces a voltage different from zero if both inputs of the op-amp are set to ground. The output of the op-amp can be forced to be zero by applying an offset voltage V_{offs} to the input of the op-amp. The offset voltage is a systematic error. It will be shown that the offset error of the coarse stage can be ignored. The amplification of the offset error for the fine stage and for the single path amplification MDAC will be derived. The error will be referred to the ADC input to show the requirements regarding the offset voltage.

The coarse stage amplifies the offset voltage by a factor of G_C. The output of the DPA MDAC yields:

$$\begin{aligned} V_2 &= V_{2C} + V_{2F} \\ &= V_{Offs} \cdot G_C + V_{Offs} \cdot G_C \cdot (-1) \cdot (1 - \frac{1}{L_F}) \\ &= V_{Offs} \cdot G_C \cdot (1 - 1 + \frac{1}{L_F}) \end{aligned} \tag{3.101}$$

$$V_2 = \frac{V_{Offs} \cdot G_C}{L_F} \tag{3.102}$$

Whereat L_F is the loop gain of the fine stage. The offset voltage at the output of the coarse stage is reduced by the fine stage. Therefore the offset error of the coarse op-amp can be ignored.

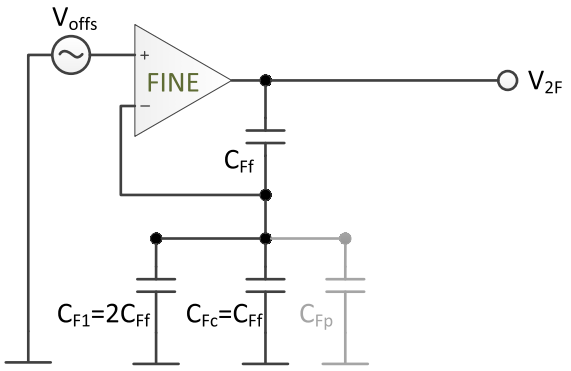

Figure 3.21: Schematic of the 1st fine stage with offset voltage V_{offs} as input. The topology yields a non-inverting amplifier.

1.5 bit DPA MDAC. Figure 3.21 shows the 1*st* fine stage with offset voltage as input. The op-amp is wired as a non-inverting amplifier. Its transfer function is:

$$\frac{V_{2F}}{V_{Offs}} = \frac{C_{F1} + C_{FC} + C_{Ff} + C_{Fp}}{C_{Ff}} = 4 + \frac{C_{Fp}}{C_{Ff}} \tag{3.103}$$

The offset voltage is amplified by a factor of 5 if the parasitic capacitor is assumed to be $C_{Fp} = C_{Ff}$. The amplification depends on the feedback factor k.

A 2*nd* fine stage amplifies the offset voltage by a factor of 7 if $C_{Fp} = C_{Ff}$. This is because of the fine input capacitor C_{F2}. The transfer function is given in (3.104).

$$\frac{V_{2F}}{V_{Offs}} = \frac{C_{F1} + C_{F2} + C_{FC} + C_{Ff} + C_{Fp}}{C_{Ff}} = 6 + \frac{C_{Fp}}{C_{Ff}} \tag{3.104}$$

1.5 bit SPA MDAC. The SPA MDAC amplifies the offset voltage of the op-amp less. It has only one input capacitor C_1. The transfer function yields:

$$\frac{V_2}{V_{Offs}} = \frac{C_1 + C_f + C_P}{C_f} = 3 + \frac{C_P}{C_f} \tag{3.105}$$

The offset voltage is amplified by a factor of 4 if $C_{Fp} = C_{Ff}$.

Table 3.2: Gain of the offset voltage V_{offs} relative to the input of the ADC. Comparison of 1st and 2nd stage DPA MDAC to SPA MDAC.

	Gain: $\frac{V_{in}}{V_{offs}}$
SPA 1*st* stage	2
DPA 1*st* stage	2.5
DPA 2*nd* stage	1.75

Table 3.2 shows the gain factor of the offset error referred to the input of the ADC. The DPA MDAC is more critical regarding offset voltage than the SPA MDAC. The fine stage must have a small offset voltage, in order to compensate for the offset voltage of the coarse stage. Matlab simulations were performed for the overall ADC, as discussed in Section 5.5.

4

MDAC 2.5 Bit with Dual Path Amplification

The capacitor mismatch and the kT/C noise are hard limitations of the 1.5 bit MDAC. Although the DPA approach can improve the error resulting from *finite open loop gain* and compensate for the errors of the coarse stage, the error sources of the fine stage cannot be compensated. To improve the error, a 2.5 bit MDAC must be used, which provides a gain of 4. The precision and noise requirements of the residue on the output of the $1st$ stage are relaxed by a factor of 2 compared to the 1.5 bit architecture. Furthermore, with the 2.5 bit MDAC the number of stages is reduced, i.e., less power is consumed by the ADC. On the other hand, the number of capacitors increases. This results in a slowdown of the settling, a larger gain error, and more kT/C noise.

This chapter discusses the 2.5 bit MDAC with *dual path amplification*. The outline of the chapter follows the outline of the previous chapter for the 1.5 bit MDAC with DPA; after introducing the DPA technique for the 2.5 bit MDAC, the transfer functions are derived, finite DC gain, capacitor mismatch, noise sources, and offset voltage are discussed and analytically approximated. All analytic results are verified using Matlab simulations and are contrasted with the results for the 1.5 bit MDAC in Chapter 3.

4.1 Topology

DPA for the 2.5 bit MDAC follows the same principle as for the 1.5 bit MDAC (cf. Section 3.1).

Figure 4.1 shows the signal path of a 2.5 bit MDAC with DPA [1]. The schematic of a 2.5 bit MDAC with DPA is depicted in Figure 4.2. The coarse stage and the fine stage are identical to an SPA MDAC. But the fine stage has additionally a capacitor C_{Fc}, which allows to subtract the coarse output V_{2C} in the fine stage. Figure 4.3 shows the schematic of the $2nd$ pipelined stage. Note that C_{C5} and C_{F5} are 4 times larger than the feedback capacitor of their stage. This is necessary to obtain gain 4 for fine input V_{1F} to the MDAC output.

The coarse output is calculated by

$$V_{2C} = (4V_{1C} - V_{sub1} - V_{sub2} - V_{sub3}) + V_{err,C}, \tag{4.1}$$

the fine output is

$$V_{2F} = (4V_{1C} - V_{sub1} - V_{sub2} - V_{sub3}) - V_{2C} + V_{err,F} = -V_{err,C} + V_{err,F}, \tag{4.2}$$

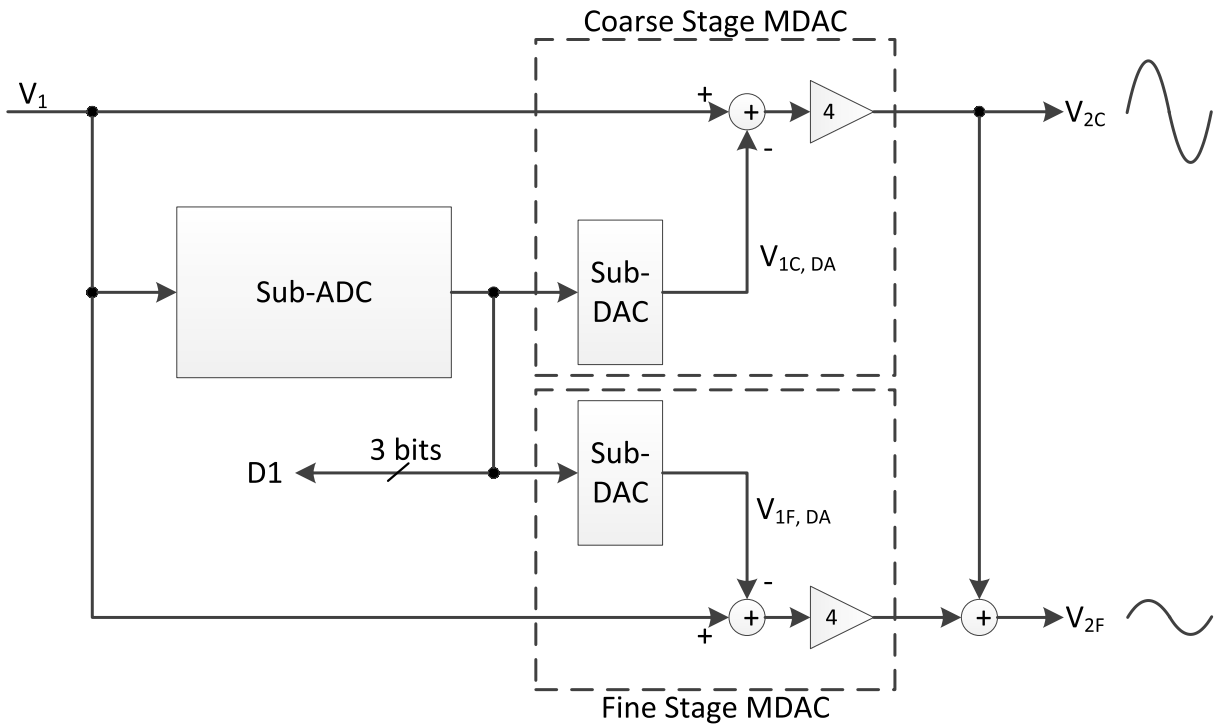

Figure 4.1: Principle of dual path amplification architecture with 2.5 bit per stage

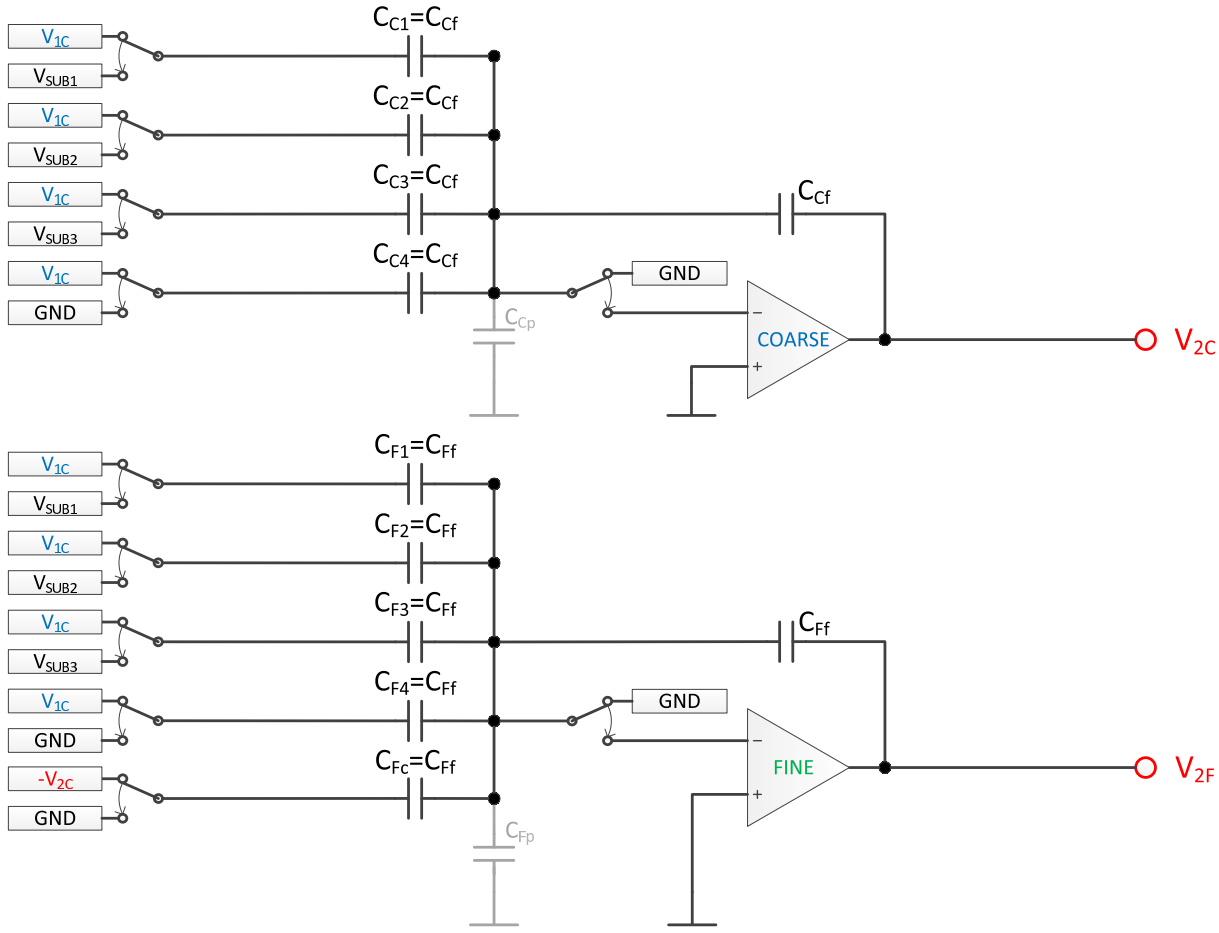

Figure 4.2: Schematic of the 1st pipeline stage, 2.5 bit MDAC, with dual path amplification - sampling mode

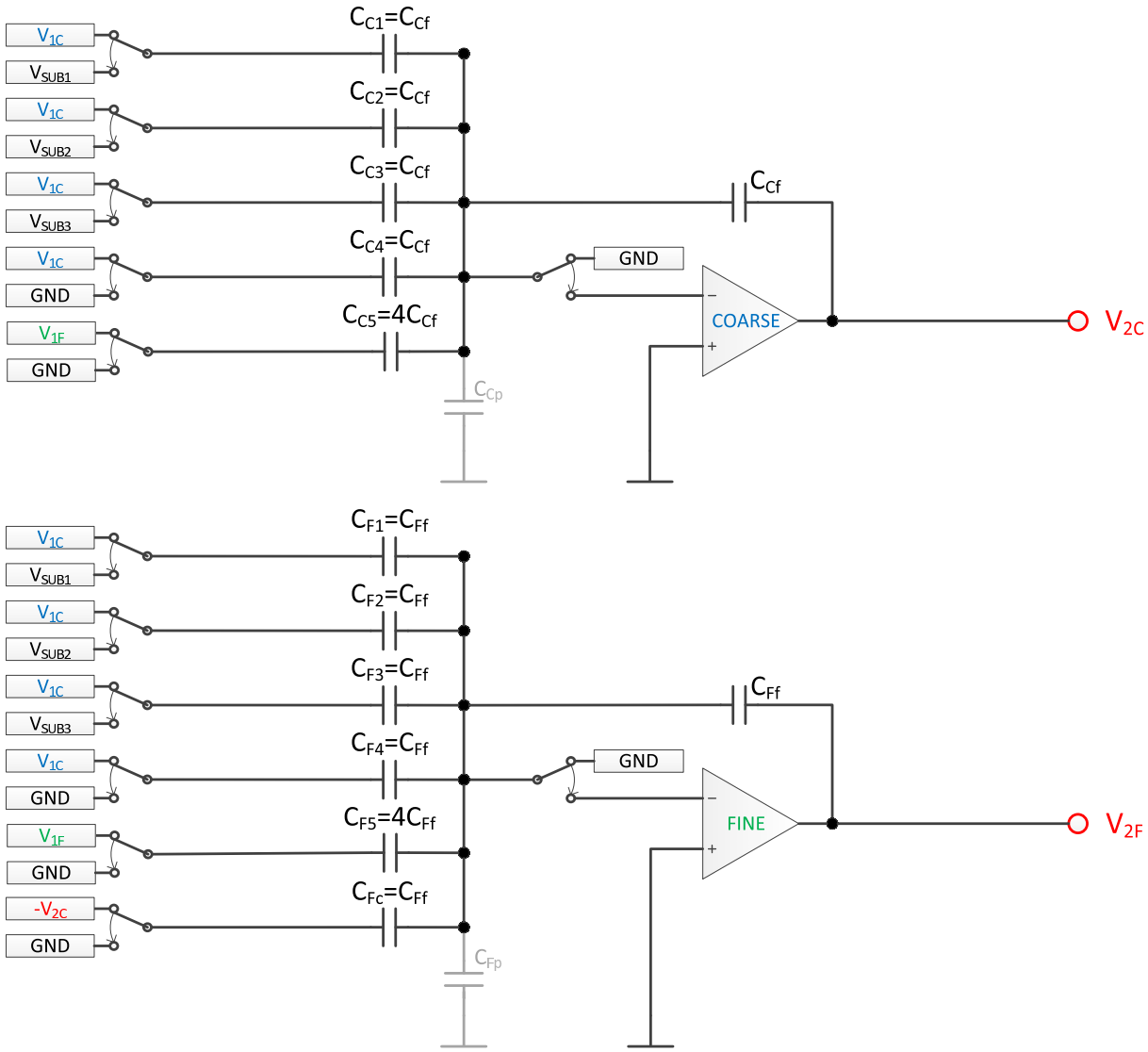

Figure 4.3: Schematic of the 2nd pipeline stage, 2.5 bit MDAC, with dual path amplification - sampling mode

and the overall residue yields

$$V_2 = V_{2C} + V_{2F} = V_{2,ideal} + V_{err,F}. \tag{4.3}$$

Similar to the 1.5 bit MDAC, error $V_{err,F}$ of the fine stage cannot be compensated. But due to the small-swing output and the separate design it might be smaller than the error $V_{err,C}$ of the coarse stage.

4.2 Transfer Functions

The MDAC is a linear MIMO system. Outputs resulting from different inputs can be superposed to get the physical outputs. The rationale behind the transfer functions of the 2.5 bit MDAC is similar to the 1.5 bit case (cf. Section 3.2). The main difference is that more capacitors and more input voltages are involved. Finite DC gain and the impact of the parasitic capacitance are considered by adding a disruptive term in the nominator. The disruptive term is the sum of all involved capacitors in the wiring of the op-amp divided by the transfer function G of the op-amp.

4.2.1 1st MDAC Stage

Refer to Figure 4.2 for the schematic of the the 1*st* MDAC stage. The corresponding disruptive term is obtained by:

$$H_{C,1st} = \frac{\Sigma C_{C,1st}}{G_C} = \frac{C_{C1} + C_{C2} + C_{C3} + C_{C4} + C_{Cp} + C_{Cf}}{G_C} \tag{4.4}$$

The input voltage V_{1C} is sampled on capacitors C_{C1}, C_{C2}, C_{C3}, and C_{C4}. Its transfer function to the coarse output is:

$$\frac{V_{2C}}{V_{1C}} = T_{CC} = \frac{C_{C1} + C_{C2} + C_{C3} + C_{C4}}{\frac{\Sigma C_{C,1st}}{G_C} + C_{Cf}} \tag{4.5}$$

Transfer functions for the subtraction voltages V_{sub1}, V_{sub2}, and V_{sub3} are:

$$\frac{V_{2C}}{V_{subi}} = T_{subiC} = \frac{-C_{Ci}}{\frac{\Sigma C_{C,1st}}{G_C} + C_{Cf}}\,, \qquad i \in \{1, 2, 3\} \tag{4.6}$$

The fine stage has one additional capacitor C_{Fc} and one additional input V_{2C}. Its disruptive term is built by:

$$H_{F,1st} = \frac{\Sigma C_{F,1st}}{G_F} = \frac{C_{F1} + C_{F2} + C_{F3} + C_{F4} + C_{Fc} + C_{Fp} + C_{Ff}}{G_F} \tag{4.7}$$

The corresponding transfer functions of the 1*st* 2.5 bit MDAC stage follow as:

$$T_{CF} = \frac{V_{2F}}{V_{1C}} = \frac{C_{F1} + C_{F2} + C_{F3} + C_{F4}}{\frac{\Sigma C_{F,1st}}{G_F} + C_{Ff}} \tag{4.8}$$

$$T_{subiF} = \frac{V_{2F}}{V_{subiC}} = \frac{-C_{Fi}}{\frac{\Sigma C_{F,1st}}{G_F} + C_{Ff}} \tag{4.9}$$

$$T_{2CF} = \frac{V_{2F}}{V_{2C}} = \frac{-C_{2C}}{\frac{\Sigma C_{F,1st}}{G_F} + C_{Ff}} \tag{4.10}$$

The overall outputs of coarse and fine stage are given by:

$$V_{2C} = \frac{(C_{C1} + C_{C2} + C_{C3} + C_{C4})V_{1C} - C_{C1}V_{sub1} - C_{C2}V_{sub2} - C_{C3}V_{sub3}}{\frac{\Sigma C_{C,1st}}{G_C} + C_{Cf}} \tag{4.11}$$

$$[-0.9em]V_{2F} = \frac{(C_{F1} + C_{F2} + C_{F3} + C_{F4})V_{1C} - C_{F1}V_{sub1} - C_{F2}V_{sub2} - C_{F3}V_{sub3} - C_{Fc}V_{2C}}{\frac{\Sigma C_{F,1st}}{G_F} + C_{Cf}} \tag{4.12}$$

For infinite open loop gain of the op-amps, the disruptive terms vanish. Assuming also perfect matching of capacitors yields the following simple input-output relations:

$$V_{2C} = 4V_{1C} - V_{sub1} - V_{sub2} - V_{sub3} \tag{4.13}$$

$$V_{2F} = 4V_{1C} - V_{sub1} - V_{sub2} - V_{sub3} - V_{2C} \tag{4.14}$$

4.2.2 2nd MDAC Stage

The transfer functions of the $2nd$ 2.5 bit MDAC stage differ from the $1st$ stage only in the disruptive term. This is because of the additional capacitors C_{C5} and C_{F5} (cf. Figure 4.3). The disruptive terms for the $2nd$ coarse and fine stage are:

$$H_{C,2nd} = \frac{\Sigma C_{C,2nd}}{G_C} = \frac{C_{C1} + C_{C2} + C_{C3} + C_{C4} + C_{C5} + C_{Cp} + C_{Cf}}{G_C} \tag{4.15}$$

$$H_{F,2nd} = \frac{\Sigma C_{F,2nd}}{G_F} = \frac{C_{F1} + C_{F2} + C_{F3} + C_{F4} + C_{F5} + C_{Fc} + C_{Fp} + C_{Ff}}{G_F} \tag{4.16}$$

The corresponding transfer functions for the fine input signal V_{1F} are given by:

$$T_{FC} = \frac{V_{2C}}{V_{1F}} = \frac{C_{C5}}{\frac{\Sigma C_{C,2nd}}{G_C} + C_{Cf}} \tag{4.17}$$

$$T_{FF} = \frac{V_{2F}}{V_{1F}} = \frac{C_{F5}}{\frac{\Sigma C_{F,2nd}}{G_F} + C_{Ff}} \tag{4.18}$$

Note that the size of capacitor C_{X5} for fine input V_{1F} is 4 times the size of the feedback capacitor C_{Xf}. This means that V_{1C} and V_{1F} are transmitted both with a gain of 4 to the outputs. The overall outputs of coarse and fine stage yield:

$$V_{2C} = \frac{(C_{C1}+C_{C2}+C_{C3}+C_{C4})V_{1C}+C_{C5}V_{1F}-C_{C1}V_{sub1}-C_{C2}V_{sub2}-C_{C3}V_{sub3}}{\frac{\Sigma C_{F,2nd}}{G_F}+C_{Cf}} \tag{4.19}$$

$$V_{2F} = \frac{(C_{F1}+C_{F2}+C_{F3}+C_{F4})V_{1C}+C_{C5}V_{1F}-C_{F1}V_{sub1}-C_{F2}V_{sub2}-C_{F3}V_{sub3}-C_{Fc}V_{2C}}{\frac{\Sigma C_{F,2nd}}{G_F}+C_{Cf}} \tag{4.20}$$

For infinite open loop gain and by ignoring the capacitor mismatch we get:

$$V_{2C} = 4V_{1C} + 4V_{1F} - V_{sub1} - V_{sub2} - V_{sub3} \tag{4.21}$$

$$V_{2F} = 4V_{1C} + 4V_{1F} - V_{sub1} - V_{sub2} - V_{sub3} - V_{2C} \tag{4.22}$$

4.3 Finite DC Gain

The big advantage of the 2.5 bit structure over the 1.5 bit structure is the relaxed residual error at the MDAC output. On the other hand, the wiring of op-amps increases because of gain 4. This affects also the open-loop gain of the MDAC and increases the residue error caused by *finite DC gain*. In this section the 2.5 bit structure will be compared to the 1.5 bit structure in terms of finite DC gain. The goal is to understand if it is possible and reasonable in term of finite DC gain to use a 2.5 bit MDAC.

4.3.1 Analytical Considerations

Like for the 1.5 bit MDAC (cf. Section 3.3), the finite DC gain introduces a gain error also for the 2.5 bit MDAC. Figure 4.4 shows the residue error due to finite DC gain. Other error sources, in particular the capacitor mismatch, are ignored in this section to isolate the impact of the finite DC gain. From the input-output relations (4.11) and (4.12) a common multiplier is singled out;

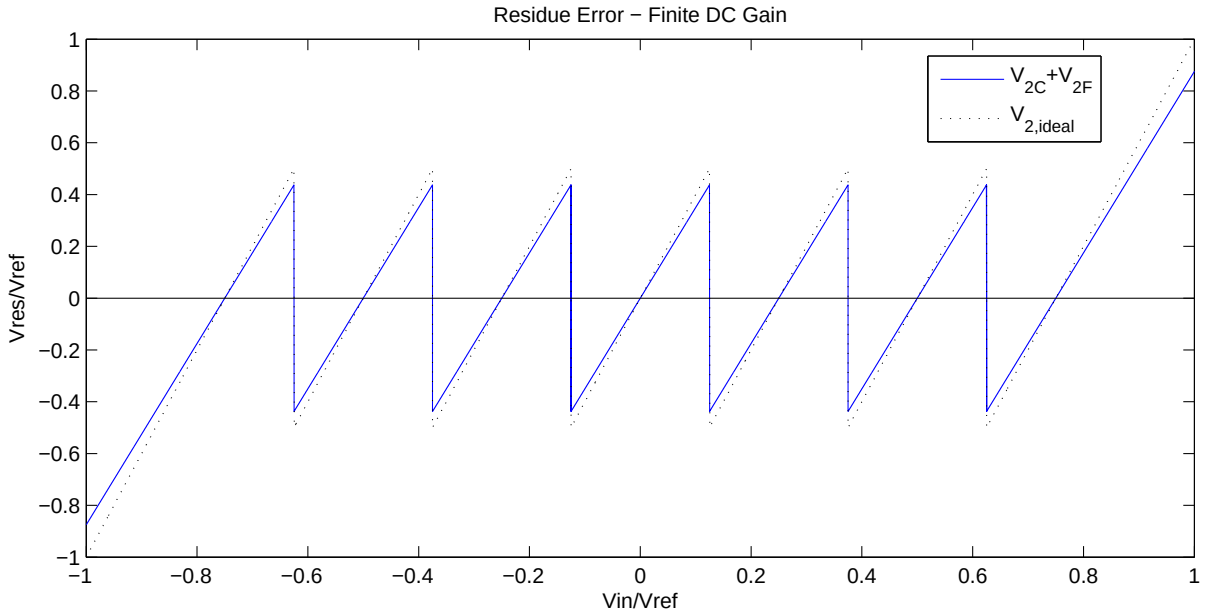

Figure 4.4: 2.5bit DPA MDAC, residue with gain error (blue continuous) and ideal residue (black, dashed)

the common multiplier contains the error source.

$$V_{2C} = \frac{C_{Cf}}{\frac{\Sigma C_C}{A_{0C}} + C_{Cf}}(4V_{1C} - V_{sub1} - V_{sub2} - V_{sub3}) \tag{4.23}$$

$$V_{2F} = \frac{C_{Cf}}{\frac{\Sigma C_F}{A_{0F}} + C_{Cf}}(4V_{1C} - V_{sub1} - V_{sub2} - V_{sub3} - V_{2C}) \tag{4.24}$$

The MDAC output can be expressed as the desired residue voltage multiplied with a gain error. The gain error can be approximated with loop gain L_C and L_F of the 2.5 bit MDAC.

$$V_{2C} = V_{2,ideal}(1-\alpha) \approx V_{2,ideal}(1 - \frac{1}{L_C}) \tag{4.25}$$

$$V_{2F} = (V_{2,ideal} - V_{2C})(1-\beta) \approx (V_{2,ideal} - V_{2C})(1 - (\frac{1}{L_F}) \tag{4.26}$$

With the assumption of $C_{xp} = C_{xf}$, the loop gains $L_{C,1st}$ and $L_{F,1st}$ of the $1st$ MDAC stage (Figure 4.2) can be calculated by:

$$L_{C,1st} = \frac{C_{Cf}}{\Sigma C_{C,1st}} A_{0C} = \frac{1}{6} A_{0C} \tag{4.27}$$

$$L_{F,1st} = \frac{C_{Ff}}{\Sigma C_{F,1st}} A_{0F} = \frac{1}{7} A_{0F} \tag{4.28}$$

This yields the following estimation for the gain-error $\alpha\beta$ of the $1st$ stage 2.5 bit DPA MDAC:

$$\alpha\beta \approx \frac{1}{L_{C,1st} L_{F,1st}} = \frac{42}{A_{0C} A_{0F}} \tag{4.29}$$

At the $2nd$ stage (Figure 4.3), the input capacitors C_{C5} and C_{F5} for the fine signal V_{1F} are added to the op-amp wiring. To achieve gain 4, they are 4 times larger than the feedback capacitors.

Assuming $C_{xp} = C_{xf}$, the loop gain can be computed as:

$$L_{C,2nd} = \frac{C_{Cf}}{\Sigma C_{C,2nd}} A_{0C} = \frac{1}{10} A_{0C} \tag{4.30}$$

$$L_{F,2nd} = \frac{C_{Ff}}{\Sigma C_{F,2nd}} A_{0F} = \frac{1}{11} A_{0F} \tag{4.31}$$

The gain-error $\alpha\beta$ of the $2nd$ stage 2.5 bit DPA MDAC can be estimated as:

$$\alpha\beta \approx \frac{1}{L_{C,2nd} L_{F,2nd}} = \frac{110}{A_{0C} A_{0F}} \tag{4.32}$$

In the $2nd$ stage, the gain-error is 2.6 times larger than in the $1st$ stage. Considering gain 4 of the MDAC, the $2nd$ stage can be relaxed regarding the residue error at the MDAC output as shown in Table 4.1. According to (3.58), the requirement for the input referred residue error increases by a factor of 2 for each stage. Taking gain 4 of the MDAC into account, it yields a relaxation by a factor of 2 of the residue error at the MDAC output. The requirements regarding DC gain of the $1st$ and the $2nd$ stage are compared in (4.33).

$$A_{0C,2nd} A_{0F,2nd} = \frac{2.6}{2} A_{0C,1st} A_{0F,1st} = 1.3\, A_{0C,1st} A_{0F,1st} \tag{4.33}$$

The $2nd$ pipelined stage needs 2.3 dB more DC gain than the $1st$ stage.

Table 4.1: Requirement for residue error referred to ADC input and to MDAC output. The accumulation of all residue errors converges to $LSB/2$.

Stage number	1	2	3	4	5	...
Input referred error	$\frac{LSB}{4}$	$\frac{LSB}{8}$	$\frac{LSB}{16}$	$\frac{LSB}{32}$	$\frac{LSB}{64}$	...
Error at MDAC output	$1\,LSB$	$2\,LSB$	$4\,LSB$	$8\,LSB$	$16\,LSB$	...

When comparing the 2.5 bit MDAC with the 1.5 bit MDAC, the different gain and hence the different requirements regarding the residue error must be considered. In the following comparison, the parasitic capacitors are again assumed to be $C_{xp} = C_{xf}$. The gain error $\alpha\beta$ of the $1st$ 1.5 bit MDAC yields:

$$\alpha\beta \approx \frac{1}{L_{C,1st} L_{F,1st}} = \frac{4 \cdot 5}{A_{0C} A_{0F}} = \frac{20}{A_{0C} A_{0F}} \tag{4.34}$$

The residue error of the 2.5 bit MDAC can be 2 times larger:

$$\alpha_{2.5}\beta_{2.5} = 2\,\alpha_{1.5}\beta_{1.5} \approx \frac{40}{A_{0C} A_{0F}} \tag{4.35}$$

Comparing with (4.29) gives a surprising result: 2.5 bit and 1.5 bit MDACs have similar requirements for DC gain. The 2.5 bit MDAC requires 5 % more DC gain to meet the same constraint of input referred residue error. Note that the 1.5 bit structure requires 2 MDAC stages to convert 2 bits, which requires additional energy and chip area. This observation makes the 2.5 bit stage with the same DC gain requirements more attractive.

Consider the $2nd$ pipeline stage of the 2.5 bit and the 1.5 bit MDAC. Both stages have the same requirements for the input referred residue error of $LSB/8$. According to Table 4.1, the residue error at the input of the $2nd$ 2.5 bit stage can be $\pm 2\,LSB$, and according to Table 3.1 the residue error of the $2nd$ 1.5 bit stage can be $\pm LSB/2$. The $2nd$ pipeline stage of the 1.5 bit

MDAC has loop gain:

$$\alpha_{1.5}\beta_{1.5} \approx \frac{1}{L_{C,2nd}\, L_{F,2nd}} = \frac{6 \cdot 7}{A_{0C}\, A_{0F}} = \frac{42}{A_{0C}\, A_{0F}} \tag{4.36}$$

If this gain error meets the constraint for the 1.5 bit MDAC, the gain error of the 2.5 bit MDAC is allowed to be

$$\alpha_{2.5}\, \beta_{2.5} = 4\, \alpha_{1.5}\, \beta_{1.5} \approx \frac{168}{A_{0C}\, A_{0F}}, \tag{4.37}$$

assuming the same DC gain for the 1.5 bit and the 2.5 bit MDAC. Comparing (4.37) with (4.32) shows that the $2nd$ 2.5 bit pipeline stage has relaxed requirements for DC gain compared to the $2nd$ 1.5 bit stage. This result is expected since the DC gain of the $2nd$ 2.5 bit stage can be scaled, while the DC gain of the $2nd$ 1.5 bit stage can not. The $2nd$ 2.5 bit MDAC needs 3.7 dB less DC gain $A_{0C}\, A_{0F}$. Furthermore, the 2.5 bit structure can convert 4 bits with 2 stages, while the 1.5 bit structure needs 4 stages to convert 4 bits.

The scaling of DC gain to further stages depends on the error requirement at the output of the MDAC. This is true for both 1.5 bit and 2.5 bit DPA MDAC stages. The scaling factor is 2 for the 2.5 bit MDAC; in the 1.5 bit MDAC structure only the last stage can be scaled according to Table 3.1. All MDACs behind the $2nd$ stage have the same schematic and the same feedback factor. This means, the loop gain and thus the gain error is linearly dependent on overall DC gain $A_{0C}A_{0F}$ of the MDAC. Table 4.2 provides an overview over DC gain requirements for 1.5 bit and 2.5 bit MDAC stages according to the simulations in Section 4.3.2.

4.3.2 Simulation Results

The simulations for the 2.5 bit MDAC were performed with the same assumptions as for the 1.5 bit MDAC in Section 3.3.2. The Matlab model uses the transfer functions introduced in Section 4.2, assuming that the transfer function of the op-amps is constant. Also the capacitor mismatch is ignored; all capacitors have nominal values. The simulation algorithm looks for $\{A_{0C}, A_{0F}\}$ pairs to get a maximum residue error of exactly $\pm 1\, LSB$ at the MDAC output, which corresponds to $LSB/4$ at the input.

$$|V_{2,ideal} - (V_{2C} + V_{2F})|_{max} = 1\, LSB \tag{4.38}$$

Figure 4.5 shows coarse over fine DC gain such that the error constraint mentioned above is met. The continuous lines show the results for the $1st$ stage of a DPA MDAC with 2.5 bit structure. The ADC resolution varies between the lines. The lines are bent since the DPA MDAC dependents on both A_{0C} and A_{0F}. The dashed lines in the respective colors show the DC gain for an SPA MDAC with the respective ADC resolution. The SPA MDAC has only one op-amp, therefore it only dependents on one DC gain, A_{0C}. The distance between neighboring curves (dashed or continuous) is about 6 dB. This is because of the scaling of LSB by a factor of 2 with every bit of the ADC resolution.

Consider the black continuous curve for the 12 bit ADC; there is a point where A_{0C} and A_{0F} have the same value of 49.1 dB. Summing up both values yields

$$|A_{0C}|_{\mathrm{dB}} + |A_{0F}|_{\mathrm{dB}} = 98.2\,\mathrm{dB},$$

where the SPA MDAC (dashed black line) needs 81 dB. This is because the loop gain of the DPA MDAC is the product of DC gain $A_{0C}A_{0F}$ and feedback factors $k_C k_F$. This results in k_F additional DC gain for the DPA MDAC to obtain the same gain error. The gain error for the

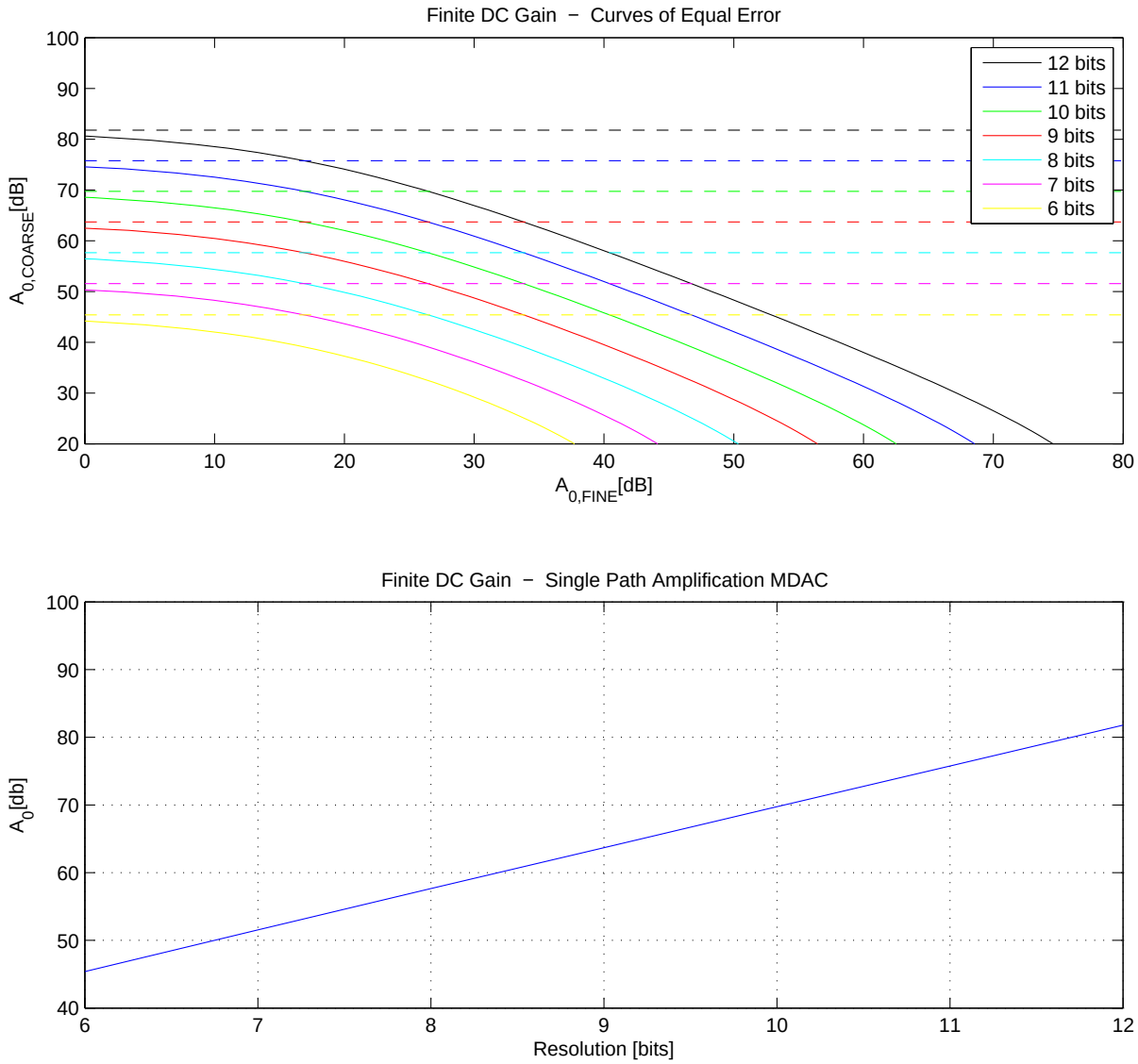

Figure 4.5: Above: Constant error 1 LSB on MDAC output, 2.5 bit MDAC, 1st stage. Continuous lines: DPA MDAC, dashed lines: SPA MDAC. Below: DC gain that produces LSB on MDAC output, dependent on ADC resolution. 2.5 bit SPA MDAC, 1st stage

1*st* stage DPA MDAC and the 1*st* stage SPA MDAC are:

$$\alpha\beta \approx \frac{k_C k_F}{A_{0C} A_{0F}} \qquad \alpha_{SPA} = \frac{k_C}{A_0} \tag{4.39}$$

Equalizing gain error of DPA MDAC and SPA MDAC yields:

$$\frac{k_C k_F}{A_{0C} A_{0F}} = \frac{k_C}{A_0} \qquad \Rightarrow \qquad A_{0C} A_{0F} = k_F A_0 \tag{4.40}$$

The plot in Figure 4.5 below shows the linear relation between ADC resolution and DC gain A_0 for the SPA MDAC.

Figure 4.6 compares the 1*st* MDAC stages for 1.5 bit and 2.5 bit. Both continuous curves show A_{0C} over A_{0F} such that an input referred error of $LSB/4$ is obtained. The plot confirms the analytical considerations that yield similar gain error for both stages in (4.35) and (4.29). Dashed lines of corresponding color show SPA MDAC results. It can be seen that the 1.5 bit

SPA MDAC outplays the 2.5 bit SPA MDAC by about 2.6 dB.

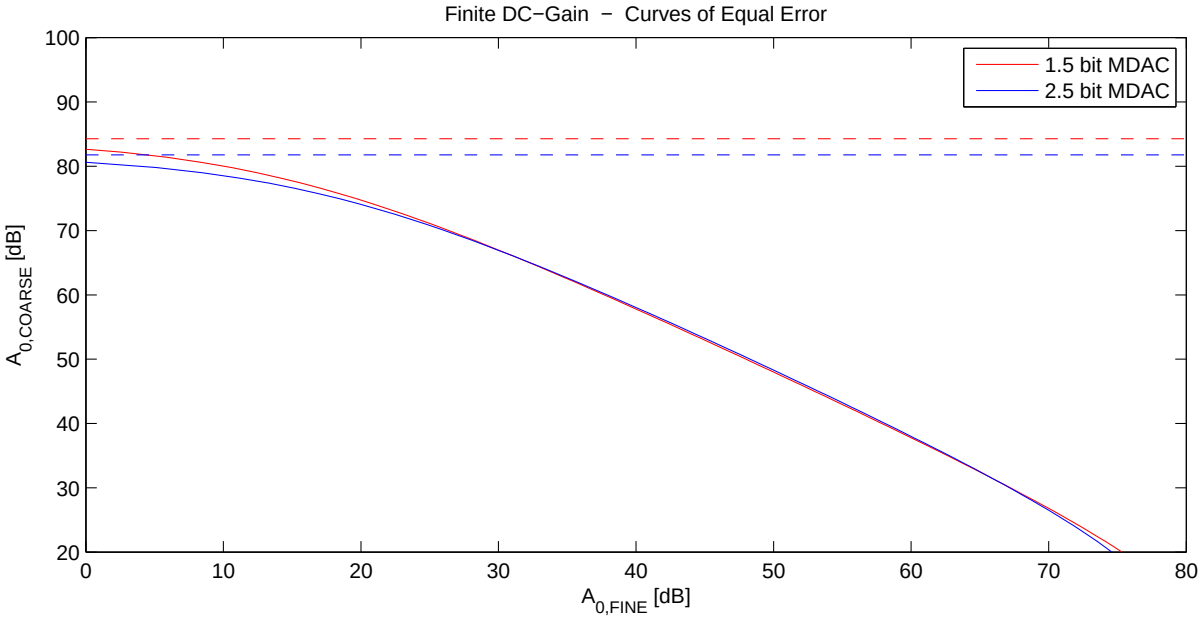

Figure 4.6: 1.5 bit vs. 2.5 bit MDAC, curves of equal input referred error $\pm LSB/4$, 1st stage

According to the considerations in Section 4.3.1, the $2nd$ pipeline stage with 1.5 bit is compared to the $2nd$ pipeline stage with 2.5 bit. As shown in Table 4.1 and Table 3.1, both stages require an input referred residue error $\pm LSB/8$. The tables mentioned above show that considering the gain of the MDAC yields a residue error of $2\,LSB$ on the output of the $2nd$ 2.5 bit MDAC and $LSB/2$ on the output of $2nd$ 1.5 bit MDAC.

Figure 4.7 shows curves of equal residue errors for the $2nd$ stages of 1.5 bit and 2.5 bit MDACs, respectively. To facilitate the comparison with the analytic results of (4.37) and (4.32), this simulation assumes the same requirement of $LSB/4$ for the input of both stages. It corresponds to the $1st$ pipeline stage. This yields a residue error of $1\,LSB$ for the 2.5 bit MDAC and of $LSB/2$ for the 1.5 bit MDAC. The analytic result of 2.5 dB between DC gain of 1.5 bit and 2.5 bit are confirmed by the simulation of Figure 4.7. The dashed lines show the DC gain required by the corresponding SPA MDAC.

Figure 4.8 shows curves of equal input gain error using the approximation (3.54) (green) and calculating the simulation with transfer functions. The approximation was used for analytic considerations. The approximated gain error leads to useful results in a range where $A_{0C} \approx A_{0F}$. If A_{0C} and A_{0F} are very different from each other, the system converges to the behavior of an SPA MDAC. However, the goal of the DPA MDAC is to distribute DC gain on two simple op-amps, therefore the approximation yields useful results.

Table 4.2: Requirement for DC gain assuming 12 bit ADC. The accumulation of all residue errors converges to $LSB/2$ referred to the ADC input.

Stage number	1	2	3	4	5	...
1.5 bit SPA MDAC	84.3 dB	87.8 dB	87.8 dB	87.8 dB	87.8 dB	...
1.5 bit DPA MDAC	97.2 dB	104.4 dB	104.4 dB	104.4 dB	104.4 dB	...
2.5 bit SPA MDAC	81.8 dB	80.2 dB	74.2 dB	68.2 dB	62.2 dB	...
2.5 bit DPA MDAC	98.3 dB	100.6 dB	94.6 dB	88.6 dB	82.6 dB	...

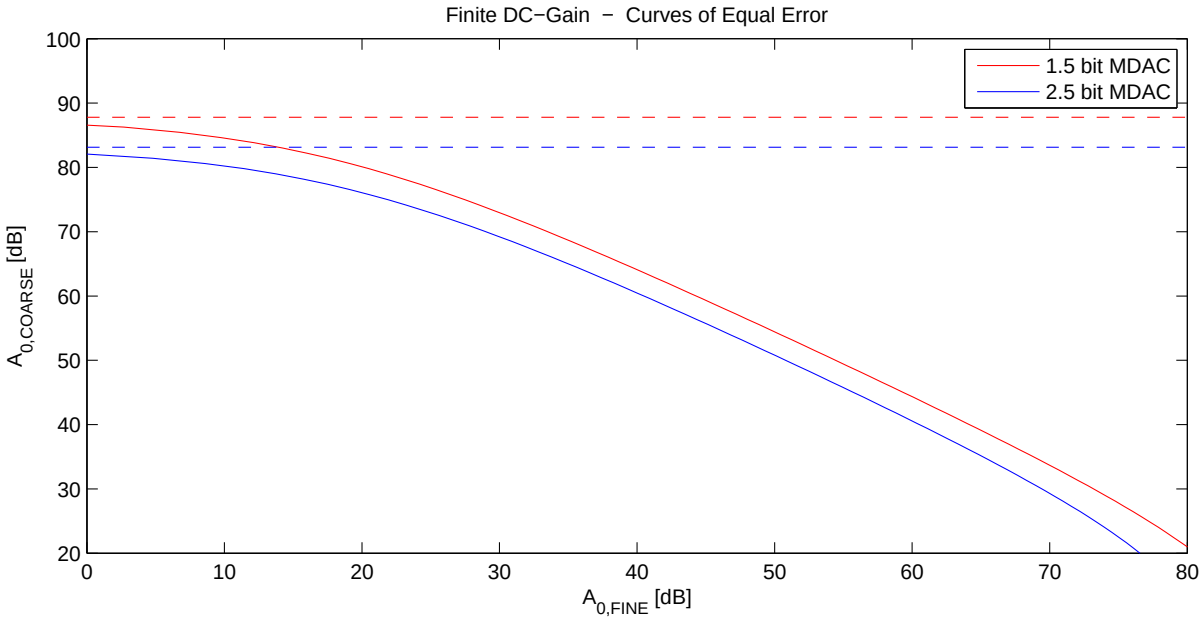

Figure 4.7: 1.5 bit 3th stage vs. 2.5 bit 2nd stage MDAC, curves of equal input referred error $\pm LSB/4$

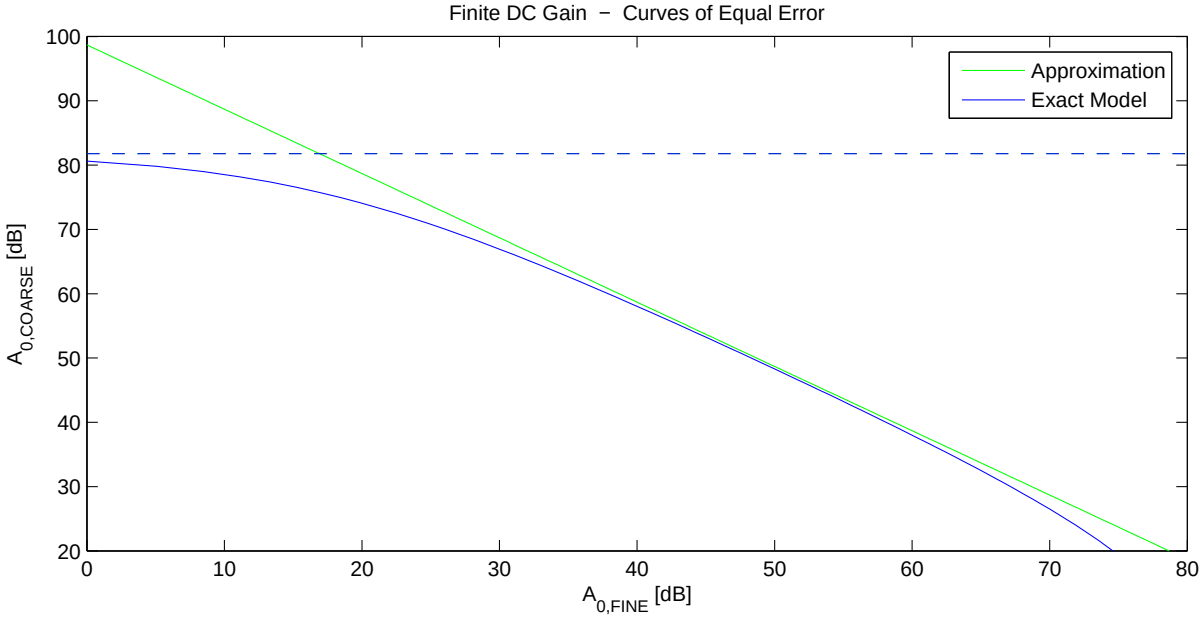

Figure 4.8: Approximation of gain error using loop gain (green) compared with simulation using transfer functions (blue). 2.5 bit MDAC, 1st pipeline stage. Continuous lines: DPA MDAC, dashed lines: SPA MDAC

Summarizing, the most important findings are:

The error caused by finite DC gain is proportional to the MDAC output; this holds also for the 2.5 bit MDAC with DPA. Also the connection between gain error $\alpha\beta$ and loop gain can be approximated with a linear relation like for the 1.5 bit structure.

The required DC gain can be split into two op-amps with low DC gain. This makes it possible to use simple Miller op-amps instead of complicated op-amps with feedback structure or cascaded structures.

The DC gain of the $2nd$ 2.5 bit DPA MDAC stage cannot be relaxed with respect to the $1st$ stage. This is due to a different topology and additional capacitors.

Each stage causes $LSB/4$ referred to the input of the MDAC for simplification. For the implementation, all following 2.5 bit stages can be relaxed by 6 dB due to the linear relation between overall DC gain $A_{0C}A_{0F}$ and gain error $\alpha\beta$. All stages after the $1st$ pipeline stage have the same schematic and therefore the same relation between DC gain and gain error.

Table 4.2 shows an overview of requirements for DC gain considering $LSB_{12}/2$ overall residue error referred to the ADC input.

1.5 bit and 2.5 bit MDACs have the same DC gain requirements for the $1st$ stage. The 1.5 bit structure needs two MDAC stages to convert 2 bits, the 2.5 bit structure needs only one stage. $2nd$ 2.5 bit MDAC and $3th$ 1.5 bit MDAC have the same requirements for the input referred residue error. The 2.5 bit stage requires 2.3 dB more DC gain $A_{0C}A_{0F}$.

4.4 Capacitor Mismatch

The results of Section 3.4 show that the capacitor mismatch limits the resolution of the 1.5 bit MDAC to about 10.5 bits. It was also shown that the DPA technique cannot compensate the capacitor mismatch of the fine stage. To reach higher resolutions, the 2.5 bit MDAC is investigated in this chapter. The 1.5 bit MDAC has gain 2, the 2.5 bit MDAC has gain 4. The requirements on the residue error of the 2.5 bit MDAC are relaxed by a factor of 2 compared to the 1.5 bit MDAC. In this section we show that the mismatch requirements are relaxed for the 2.5 bit MDAC as well.

The mismatch error for the 2.5 bit DPA MDAC is calculated analytically in Section 4.4.1. To get crisp results, some simplifying assumptions were taken. The calculations rely on the considerations in Section 3.4.1. In Section 4.4.2, the analytic results of Section 4.4.1 are compared to the Matlab simulation results. The simulation also provides more insight into the behavior of 2.5 bit DPA and the SPA MDAC concerning capacitor mismatch.

4.4.1 Analytic Considerations

The schematic of the 2.5 bit SPA MDAC corresponds to the coarse stage of the DPA MDAC (cf. Figure 4.2). The residue affected by the capacitor mismatch is calculated according to (3.62). All capacitors are assumed to be Gaussian distributed with standard deviation $C_{nom}\sigma_{abs}$. Op-amps are assumed to be ideal. The MDAC output is calculated by:

$$\begin{aligned} V_2 &= \frac{(V_1 - V_{sub1})(1+\epsilon_1) + (V_1 - V_{sub2})(1+\epsilon_2) + (V_1 - V_{sub3})(1+\epsilon_3) + V_1(1+\epsilon_4)}{1+\epsilon_f} \\ &\approx (V_1 - V_{sub1})(1+\epsilon_1)(1-\epsilon_f) + \cdots + V_1(1+\epsilon_4)(1-\epsilon_f) \\ &\approx (V_1 - V_{sub1})(1+\epsilon_1-\epsilon_f) + \cdots + V_1(1+\epsilon_1)(1-\epsilon_f) \end{aligned} \tag{4.41}$$

$$\begin{aligned} V_2 \approx V_{2,ideal} &- \epsilon_f(V_{2,ideal}) + \epsilon_1(V_1 - V_{sub1}) + \epsilon_2(V_1 - V_{sub2}) + \\ &+ \epsilon_3(V_1 - V_{sub3}) + \epsilon_4(V_1) \end{aligned} \tag{4.42}$$

The residue error $V_{err} = V_2 - V_{2,ideal}$ can be identified as:

$$V_{err} \approx -\epsilon_f(V_{2,ideal}) + \epsilon_1(V_1 - V_{sub1}) + \epsilon_2(V_1 - V_{sub2}) + \epsilon_3(V_1 - V_{sub3}) + \epsilon_4(V_1) \tag{4.43}$$

This result is not as simple as in the 1.5 bit case. It is not proportional to $V_{2,ideal}$ because the inputs are applied on different capacitors. Hence they are amplified with different gain-deviation due to statistically independent random variables ϵ_i. The residue of the 2.5 bit DPA MDAC with capacitor mismatch is depicted in Figure 4.9. The capacitor mismatch is overdrawn to better emphasize its effect. The dashed line denotes ideal residue.

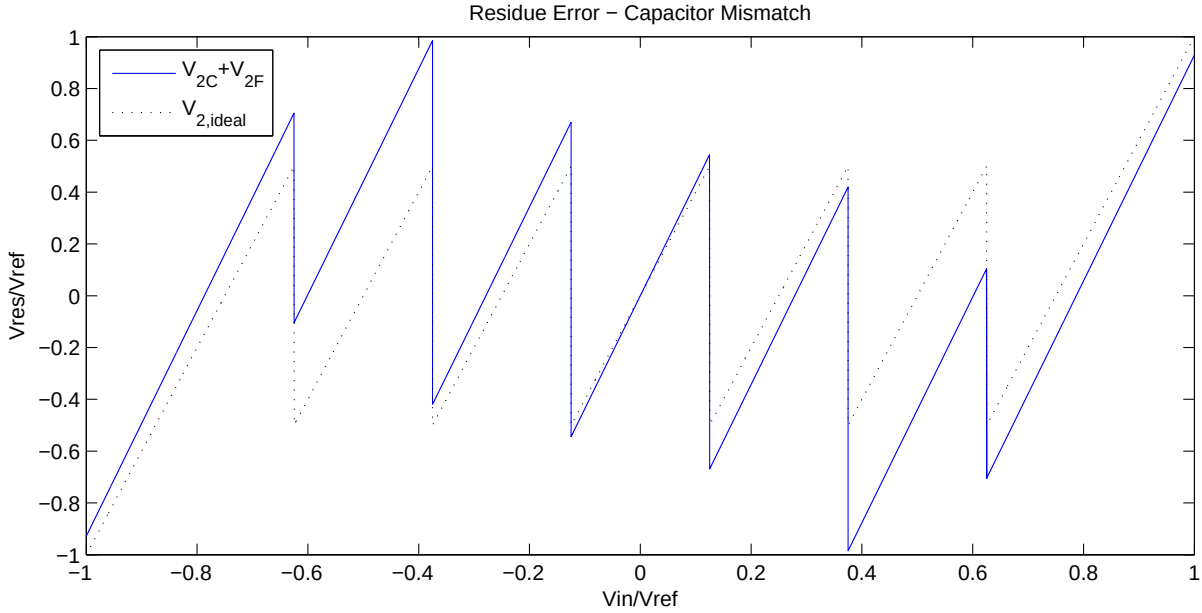

Figure 4.9: Residue of 2.5 bit DPA MDAC with capacitor mismatch (continuous line), ideal residue (dashed line)

The standard deviation of the residue error can be calculated by:

$$\sigma\{V_{err}\} = \sqrt{V_{2,ideal}^2 + (V_1 - V_{sub1})^2 + (V_1 - V_{sub2})^2 + (V_1 - V_{sub3})^2 + V_1^2} \cdot \frac{1}{\sqrt{2}}\,\sigma_c \qquad (4.44)$$

The largest error is produced with $V_1 = \pm V_{ref}$. Assuming a 12 bit ADC and capacitor mismatch $\sigma_c = 0.1\,\%$, the residue error is:

$$\sigma\{V_{err}\} = \sqrt{1+1} \cdot \frac{1}{\sqrt{2}} \cdot \sigma_c = 0.001 = 2.0\,LSB_{12} \qquad (4.45)$$

It is surprising that (4.45) and (3.66) for the 1.5 bit MDAC lead to the same result. Taking the different gain of the 1.5 bit and the 2.5 bit MDAC into account, this result means that the input referred error of the 2.5 bit MDAC is half as large. This is valid for the largest error occurring with input $V_1 = \pm V_{ref}$.

Next the behavior of an MDAC with *dual path amplification* will be discussed. The 2.5 bit DPA MDAC is shown in Figure 4.2. The coarse stage is assumed to be ideal to simplify the calculation. This is acceptable since the error produced by the coarse stage is mostly compensated by the fine stage. With the assumption of an ideal coarse stage, the fine output V_{2F} corresponds to a residue error:

$$V_{err} = V_{2C} + V_{2F} - V_{2,ideal} \qquad (4.46)$$

It can be approximated by:

$$
\begin{aligned}
V_{2F} &= (V_1 - V_{sub1}) \cdot \frac{C(1+\epsilon_1)}{C(1+\epsilon_f)} + \cdots - V_{2C} \cdot \frac{C(1+\epsilon_5)}{C(1+\epsilon_f)} = \\
&= \frac{(V_1 - V_{sub1})(1+\epsilon_1) + \cdots + (V_1 - V_{sub3})(1+\epsilon_3) + V_1(1+\epsilon_4) - V_{2C}(1+\epsilon_5)}{1+\epsilon_f} = \\
&= \frac{(V_1 - V_{sub1})(1+\epsilon_1) + \cdots - [(V_1 - V_{sub1})(1+\epsilon_5) + \cdots + V_1(1+\epsilon_5)]}{1+\epsilon_f} \approx \\
&\approx \frac{(V_1 - V_{sub1})(\epsilon_1 - \epsilon_5) + (V_1 - V_{sub2})(\epsilon_2 - \epsilon_5) + (V_1 - V_{sub3})(\epsilon_3 - \epsilon_5) + V_{in}(\epsilon_4 - \epsilon_5)}{1}
\end{aligned}
\tag{4.47}
$$

$$
\begin{aligned}
V_{2F} &= V_{2C} + V_{2F} - V_{ideal} = V_{err} \\
V_{err} &\approx \epsilon_1(V_1 - V_{sub1}) + \epsilon_2(V_1 - V_{sub2}) + \epsilon_3(V_1 - V_{sub3}) + \epsilon_4(V_1) - \epsilon_5(V_{2,ideal})
\end{aligned}
\tag{4.48}
$$

The result of (4.47) corresponds to the result in (4.42) for the SPA MDAC. The DPA technique cannot compensate errors caused by the fine stage. The largest residue error is produced with input $\pm V_{ref}$. Assuming a capacitor mismatch of $\sigma_c = 0.1\,\%$, the standard deviation of the residue error for $V_1 C = \pm V_{ref}$ yields:

$$
\sigma\{V_{err}\} = 2\,\mathrm{LSB}_{12} \tag{4.49}
$$

The analytical results are verified by the Matlab simulations presented below.

4.4.2 Simulation Results

2.5 bit MDACs using DPA vs. SPA were simulated in Matlab. All capacitors of the MDAC were deviated randomly with Gaussian distribution and standard deviation $\sigma_{abs} = \frac{1}{\sqrt{2}}\,\sigma_c$, where σ_c is the capacitor mismatch. The simulation was performed with 10^3 different capacitor sets and with 10^3 input samples. It yields a distribution of 10^6 residue values. As shown in Section 4.4.1, the residue errors caused by capacitor mismatch can be approximated by a sum of Gaussian distributed random variables. Therefore also the residue error can be assumed to be nearly Gaussian distributed. For plotting the results, the standard deviation of the residue error distribution was calculated.

Figure 4.10 compares the residue errors of 2.5 bit SPA MDAC (black dashed line) and 2.5 bit DPA MDAC (magenta and cyan lines). The standard deviation of the residue errors is shown over the input voltage V_{1C} normalized by V_{ref}. The magenta curve and the cyan curve are identical. They show the residue error of the 2.5 bit DPA MDAC with the topology of a $1st$ pipeline stage (dashed cyan) and the topology of a $2nd$ pipeline stage (magenta). This result is not surprising because the simulation assumed fine input V_{1F} of the $2nd$ stage to be zero. Therefore C_{2C} and C_{2F} of the $2nd$ pipeline stage produce no mismatch error. Fine input V_{1F} can be assumed to be small compared to coarse input V_{1C}, therefore it is ignored. The same behavior can be observed for the 1.5 bit MDAC (cf. Figure 3.16). Looking at the maximum values for the residue error at $V_{1C}/V_{ref} = \pm 1$, it can be seen that standard deviation of the error is about $2\,\mathrm{LSB}_{12}$. This corresponds to the example calculated in (4.45). In the analytical calculation, simplifications were made. The residue error of the SPA MDAC (4.45) and of the DPA MDAC (4.48) show the the same standard deviation. The simulation in Figure 4.10 shows good matching of the curves in the linear range $[-0.125, +0.125]$. For larger inputs the curves of SPA and DPA MDAC deviate from each other. Looking at the upper corners where $V_{1C} = \pm V_{ref}$, the

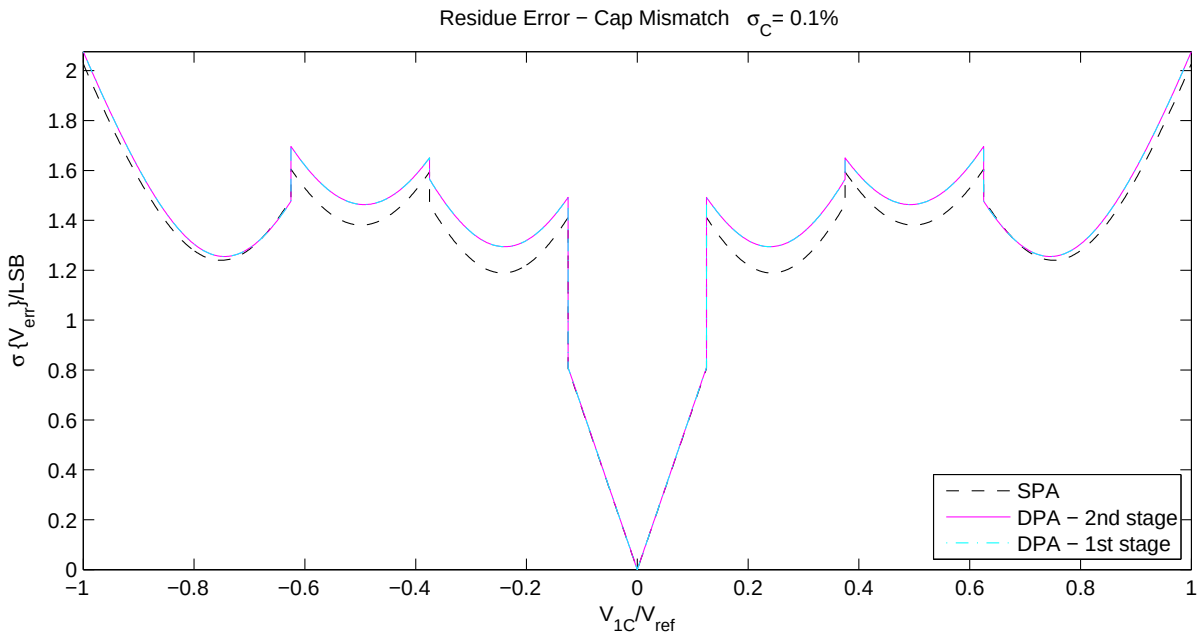

Figure 4.10: Residue error of a 2.5 bit MDAC with capacitor mismatch $\sigma_c = 0.1\,\%$

curves for SPA and DPA MDAC match again. The standard deviation of the curves deviates only 0.8 % from the analytical result of $2\,LSB_{12}$.

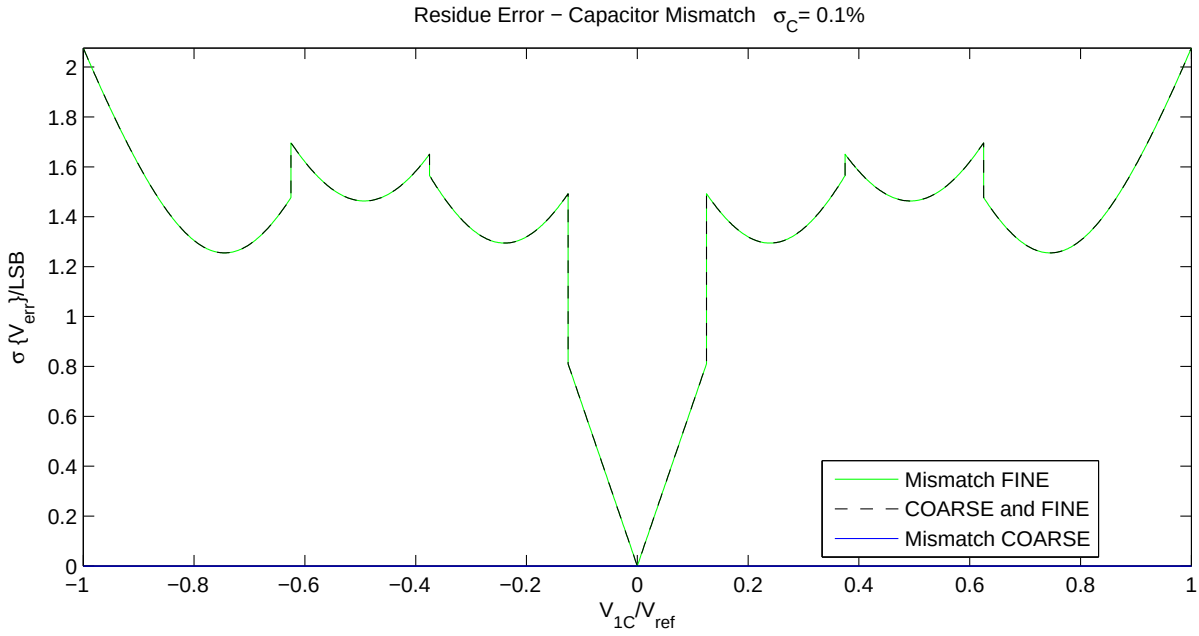

Figure 4.11: Residue error of 2.5 bit MDAC. Green line: Mismatch only on capacitors of fine stage, coarse stage is ideal. Black dashed line: Mismatch on all capacitors of the MDAC. Blue line (on x-axis): Mismatch only on coarse stage, fine stage is ideal

Figure 4.11 shows the impact of coarse and fine stage to the residue error. The standard deviation of the residue error was normalized by LSB_{12} and is plotted over the input voltage of the MDAC. The findings correspond to the 1.5 bit case. The blue line along the x-axis shows the residue error for mismatch only at the coarse stage. All errors are corrected by the ideal fine stage. The green curve and the dashed black curve show residue error only on the fine stage and

on all capacitors of the MDAC. These two cases result in the same residue error, which shows a very good rejection for mismatch errors of the coarse stage, even if the fine stage is affected by capacitor mismatch. Thus the simulation supports the assumption of an ideal coarse stage taken for the analytical considerations in Section 4.4.1.

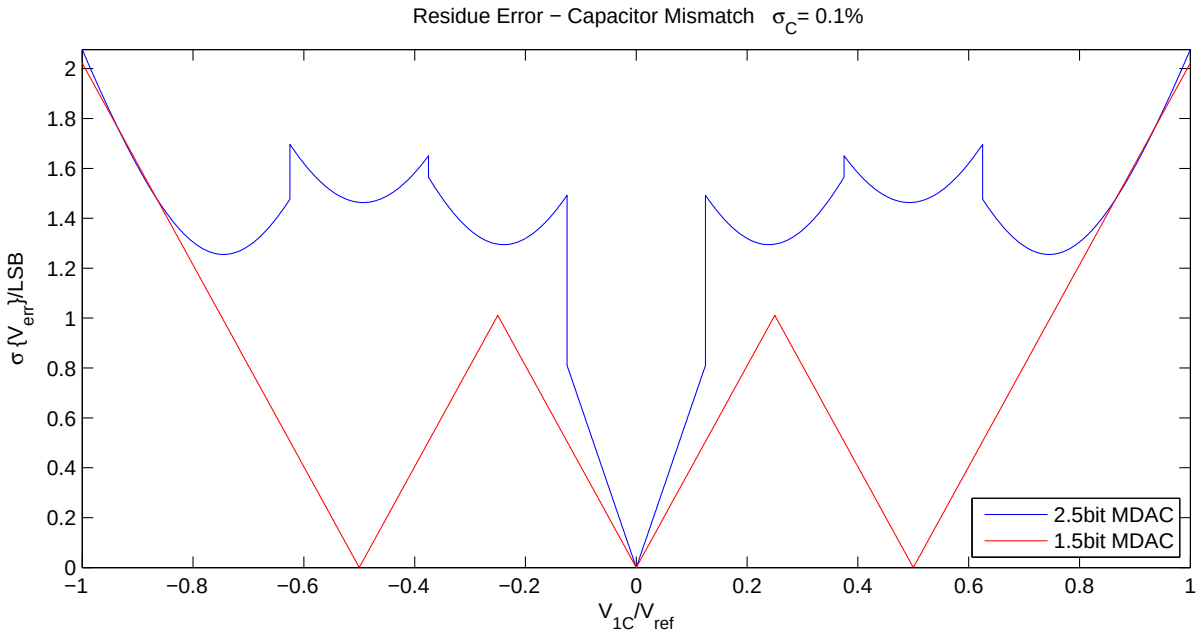

Figure 4.12: Residue error of a 1.5 bit (red) and a 2.5 bit (blue) MDAC 1st stage. Capacitor mismatch is $\sigma_c = 0.1\,\%$

Figure 4.12 shows the standard deviation of residue errors for 1.5 bit (red) and 2.5 bit (blue) DPA MDACs. The blue curve shows more kinks due to the 6 comparators in the sub-ADC of the 2.5 bit MDAC compared to the 2 comparators in the sub-ADC of the 1.5 bit MDAC. Furthermore, the blue curve shows linear behavior only between -0.125 and $+0.125$, while the full red curve is piecewise linear. At the 2.5 bit MDAC all subtraction voltages are $V_{sub1} = V_{sub2} = V_{sub3} = 0$ in the range of $V_1 = [-0.125, +0.125]$. Thus the MDAC depends only on the input V_{1C} in this range. Considering (4.48) and (4.43), the residue error can be written as:

$$\begin{aligned} V_{err} &\approx \epsilon_1(V_1) + \epsilon_2(V_1) + \epsilon_3(V_1) + \epsilon_4(V_1) - \epsilon_5(4\,V_1) = \\ &= V_1(\epsilon_1 + \epsilon_2 + \epsilon_3 + \epsilon_4 - 4\,\epsilon_5) \end{aligned} \tag{4.50}$$

The linear dependency of the residue error on input V_1 can be seen in (4.50). If $\|V_1\| > 0.125$, the residue error depends on more than one input applied on different capacitors. The standard deviation calculated in (4.44) contains a squared sum of different inputs. This is the reason for the bent curves of the 2.5 bit MDAC. The 1.5 bit MDAC has a smaller residue error for most input values. The error for $V_{1C}/V_{ref} = 1$ is approximately $2\,\mathrm{LSB}_{12}$ for both 1.5 bit and 2.5 bit MDAC. Considering gain 4 of the 2.5 bit MDAC, the standard deviation of the input referred error $e_{2.5,max}$ is:

$$\sigma\{e_{2.5,max}\} \approx \frac{1}{2}\,\mathrm{LSB}_{12} \qquad \text{with} \qquad V_{1C}/V_{ref} = 1, \qquad \sigma_c = 0.1\,\% \tag{4.51}$$

The 1.5 bit stage has only gain 2, and the standard deviation of the input referred error yields:

$$\sigma\{e_{1.5,max}\} \approx 1\,\mathrm{LSB}_{12} \qquad \text{with} \qquad V_{1C}/V_{ref} = 1, \qquad \sigma_c = 0.1\,\% \tag{4.52}$$

This comparison, however, considers only two values for the input V_{1C}. A more informative comparison is shown in Figure 4.13.

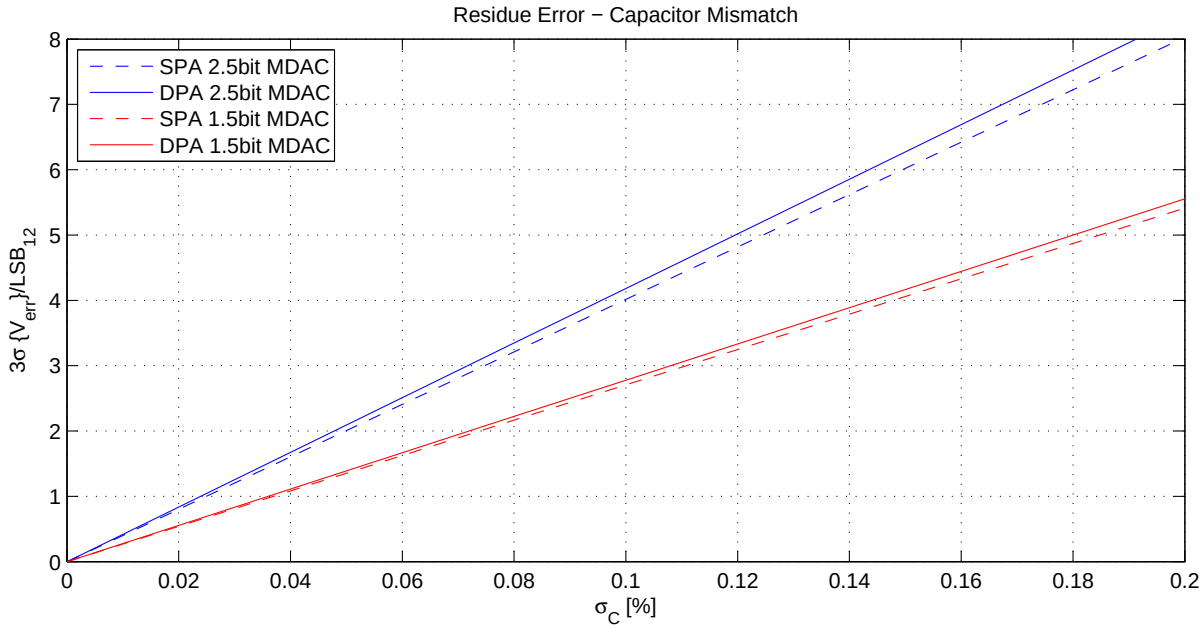

Figure 4.13: Residue Error of 1.5 bit and 1.5 bit MDAC with mismatch $\sigma_c = 0.1\,\%$. $3\,\sigma$ value of error distribution is depicted dependent on capacitor mismatch σ_c

Figure 4.13 shows the $3\,\sigma$ value of residue errors over capacitor mismatch σ_c. The simulation was performed with 10^3 uniformly distributed input samples $V_{1C} \sim \mathcal{U}[-1, 1]$ and 10^3 capacitor sets, where each capacitor is independently varied with $C \sim \mathcal{N}(C_{nom}, \sigma^2_{abs})$. $3\,\sigma$ contains 99.7 % of all errors, assuming Gaussian distribution of the residue error. This is a representative value for the worst error. The blue continuous and the blue dashed lines show the residue error for a 2.5 bit DPA and SPA MDAC normalized by LSB_{12}, respectively. The red continuous and the red dashed lines show the residue error for a 1.5 bit DPA and SPA MDAC normalized by LSB_{12}, respectively. When comparing the mismatch errors of 1.5 bit and 2.5 bit DPA MDACs, it is necessary to consider their gain. Referring the error to the MDAC input, for 2.5 bit we need to divide by 4. The $3\,\sigma$ value of the error $V_{err,2.5}$ for DPA with 0.1 % mismatch is:

$$3\,\sigma\,\{V_{err,2.5}\} = \frac{4.18\,LSB_{12}}{4} = 1.05\,LSB_{12} \tag{4.53}$$

The 1.5 bit MDAC has gain 2. The $3\,\sigma$ value for the input referred error of 1.5 bit yields:

$$3\,\sigma\,\{V_{err,1.5}\} = \frac{2.78\,LSB_{12}}{2} = 1.39\,LSB_{12} \tag{4.54}$$

The 2.5 bit DPA MDAC is 32 % better than the 1.5 bit DPA MDAC. Nevertheless, for a $3\,\sigma$ value of $\mathrm{LSB}_{12}/2$, only 0.048 % mismatch are acceptable. The minimum mismatch achievable in 40 nm technology of 0.076 % yields for the 2.5 bit DPA MDAC:

$$3\,\sigma\,\{V_{err,2.5}\} = \frac{3.18\,LSB_{12}}{4} = 0.8\,LSB_{12} \tag{4.55}$$

The single stage performs 4 % better than the DPA stage.

The most important findings regarding capacitor mismatch are:

1*st* stage DPA MDAC and 2*nd* stages DPA MDAC have the same performance when the fine input signal V_{1F} is assumed to be small.

Mismatch on the coarse stage is compensated by the fine stage of the DPA MDAC. It does not affect the residue error.

Mismatch on the fine stage cannot be compensated. It causes a residue error of the DPA MDAC that is about 4 % larger than the residue error of the SPA MDAC.

The 2.5 bit MDAC is about 1/3 better than the 1.5 bit MDAC, comparing the residue errors referred to the MDAC input. This is because of the increased gain by a factor of 2.

Considering mismatch limits of a Complementary Metal Oxide Semiconductor (CMOS) 40 nm technology, the capacitor mismatch limits the $3\,\sigma$ value of the residue error of the 2.5 bit MDAC to $0.8\,LSB_{12}$.

4.5 Noise Sources

In this section the following noise sources are discussed for the 2.5 bit MDAC and compared with the 1.5 bit MDAC:

Noise produced by the switches is sampled on capacitors during each sampling phase. It is called kT/C noise.

The reference voltage V_{ref} is corrupted by noise.

The output of an op-amp is a noise source.

Simulations were only performed for the overall ADC, the results are shown in Section 5.4.

The impact of noise sources in the coarse stage is discussed in Section 3.5.1 for the 1.5 bit MDAC. Since the DPA structure is the same for 1.5 bit and 2.5 bit MDACs, conclusions is also valid for the 2.5 bit DPA MDAC. Noise sources in the coarse stage are reduced by a factor of $1/L_F$. Thus, the fine stage is the dominant noise source [1]. The following considerations ignore noise from the coarse stage and focus on the noise from the fine stage.

4.5.1 kT/C Noise

kT/C noise is discussed in Section 3.5.2 for the 1.5 bit MDAC. This section extends the results to the 2.5 bit MDAC.

In the sampling phase, shown in Figure 4.2, capacitors $C_{F1}, C_{F2}, C_{F3}, C_{F4}$ and C_{Fc} are loaded via a switch with the resistance R_{ON}. However, C_{Fp} and C_{Ff} are also connected through switches to ground. The thermal noise of resistors (3.78) is sampled onto the capacitors. Calculating the noise power sampled on a capacitor shows that the size of the resistor does not show up in the result.

First stage: Figure 4.14 shows the fine stage of a 1*st* stage 2.5 bit MDAC. The noise sampled on the capacitors is defined as a voltage source. It can be seen that each capacitor is connected with a noise source. The noise power at the MDAC output is calculated in (4.56) [9].

$$\sigma_{2F}^2 = \frac{kT\,(C_{F1} + C_{F2} + C_{F3} + C_{F4} + C_{Fc} + C_{Fp} + C_{Ff})}{C_{Ff}^2} = \frac{k\,T\,(6 + C_{Fp}/C_{Ff})}{C_{Ff}} \qquad (4.56)$$

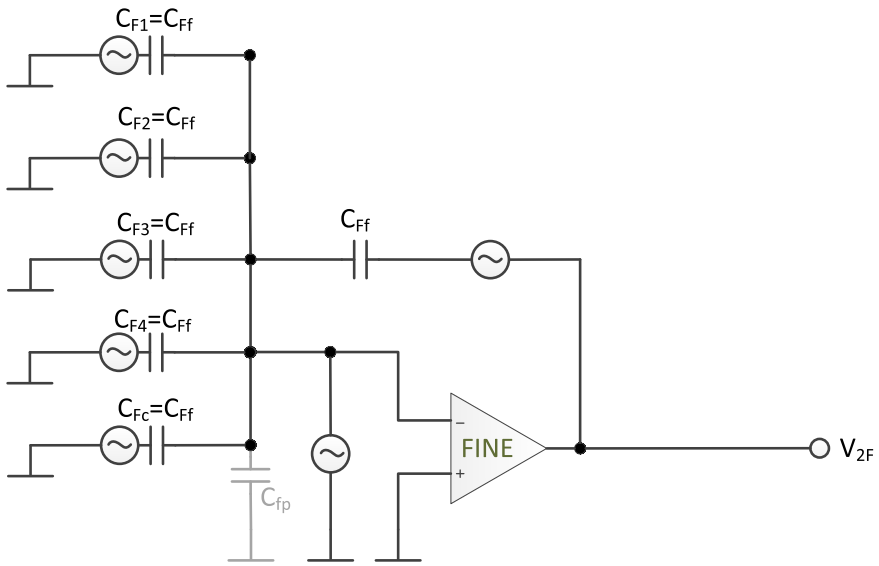

Figure 4.14: 1st fine stage of 2.5 bit DPA MDAC. Noise sampled on capacitors is defined as voltage source

With the assumption that $C_{Fp} = C_{Ff}$ follows (4.57).

$$\sigma_{2F}^2 = \frac{7\,kT}{C_{Ff}} \tag{4.57}$$

The noise power is referred to the input of the ADC in (4.58).

$$\sigma_{in}^2 = \frac{7\,kT}{C_{Ff}} \cdot \left|\frac{1}{4}\right|^2 = \frac{7}{16}\,\frac{kT}{C_{Ff}} \tag{4.58}$$

This result corresponds to the result of the $2nd$ stage of an 1.5 bit DPA MDAC. Assuming the feedback capacitor to be 250 fF, and a temperature of $T = 20\,°C$, the effective noise voltage σ_{in} of the $1st$ stage yields:

$$\sigma_{in} = \sqrt{\frac{7}{16}\,\frac{1.38 \cdot 10^{-23}\,\frac{J}{K} \cdot 293.15\,K}{4 \cdot 250 fF}} = 84\,\mu V \tag{4.59}$$

The input referred effective noise voltage is normalized by LSB_{12} in (3.84).

$$\frac{\sigma_{in}}{LSB_{12}} = \frac{84\,\mu V}{0.49 \cdot 10^{-3} \cdot V_{ref}} = \frac{0.17}{V_{ref}} \tag{4.60}$$

The effective noise voltage σ_{in} corresponds to $LSB_{12}/4$ if $V_{ref} = 0.68\,V$.

Second stage: The second fine stage is depicted in Figure 4.3. The second and all following fine stages have the capacitor C_{F5} in addition to the capacitors of the $1st$ stage , where C_{F5} is four times the size of the feedback capacitor C_{Ff}.

$$C_{F5} = 5 \cdot C_{Ff} \tag{4.61}$$

kT/C noise power σ_{2F}^2 at the output of the $2nd$ stage is calculated in (4.62).

$$\begin{aligned}\sigma_{2F}^2 &= \frac{kT\,(C_{F1}+C_{F2}+C_{F3}+C_{F4}+C_{F5}+C_{Fc}+C_{Fp}+C_{Ff})}{C_{Ff}^2} \\ &= \frac{k\,T\,(10+C_{Fp}/C_{Ff})}{C_{Ff}}\end{aligned} \tag{4.62}$$

The noise power is referred to the input of the ADC in (4.63). The parasitic capacitor is assumed to be $C_{Fp} = C_{Ff}$. The gain from the input of the ADC to the output of the $2nd$ MDAC stage is a factor of 16.

$$\sigma_{in}^2 = \frac{11\,kT}{C_f} \cdot \left|\frac{1}{16}\right|^2 = \frac{11}{16^2}\,\frac{kT}{C_{Ff}} \tag{4.63}$$

Assuming the feedback capacitor to be 250 fF, and a temperature of $T = 20\,°C$, the effective noise voltage σ_{in} of the $2nd$ fine stage yields:

$$\sigma_{in} = \sqrt{\frac{11}{16^2}\,\frac{1.38\cdot 10^{-23}\,\frac{J}{K}\cdot 293.15\,K}{250fF}} = 26\,\mu V \tag{4.64}$$

The input referred effective noise voltage is normalized by LSB_{12} in (4.65).

$$\frac{\sigma_{in}}{LSB_{12}} = \frac{26\,\mu V}{0.49\cdot 10^{-3}\cdot V_{ref}} = \frac{0.054}{V_{ref}} \tag{4.65}$$

The reference voltage must only be $V_{ref} = 0.22\,V$ to obtain an effective noise σ_{in} of $LSB_{12}/4$ referred to the ADC input.

Single path amplification MDAC. The kT/C noise power of an SPA MDAC is given by:

$$\sigma_{2F}^2 = \frac{kT\,(C_{F1}+C_{F2}+C_{F3}+C_{F4}+C_{Fp}+C_{Ff})}{C_{Ff}^2} = \frac{k\,T\,(5+C_{Fp}/C_{Ff})}{C_{Ff}} \tag{4.66}$$

The same assumptions are made as for the DPA MDAC. The feedback capacitor and the parasitic capacitor are assumed to be $C_{Cp} = C_{Cf} = 250$ fF. The temperature is assumed to be $T = 20\,°C$. The noise power of the $1st$ SPA MDAC stage is referred to the input of the ADC in (4.67).

$$\sigma_{in} = \sqrt{\frac{6\,kT}{C_f}\cdot\left|\frac{1}{4}\right|^2} = \sqrt{\frac{6}{16}\,\frac{1.38\cdot 10^{-23}\,\frac{J}{K}\cdot 293.15\,K}{250fF}} = 78\,\mu V \tag{4.67}$$

σ_{in} corresponds to $LSB_{12}/4$ if $V_{ref} = 0.64\,V$.

It can be seen that the $1st$ stage of an SPA MDAC has a slightly better noise performance than the $1st$ stage of a DPA MDAC. This is because of the additional capacitor C_{Fc}.

1.5 Bit vs. 2.5 Bit MDAC: Effective noise voltages referred to the ADC input are used for the following considerations. Comparing the $1st$ stage of an SPA ADC using 1.5 bit MDACs to the $1st$ stage of a DPA ADC using 2.5 bit MDACs, it can be seen that the 2.5 bit structure has relaxed requirements on kT/C noise. If the feedback capacitors C_{Cf} of both $1st$ stages are of the same size and the parasitic capacitors are $C_{Cp} = C_{Cf}$, the 2.5 bit MDAC produces 38.6 % less noise than the 1.5 bit MDAC.

The same tendency can be observed in the DPA structure. Consider the $1st$ stage of a DPA ADC. A 2.5 bit MDAC produces 40 % less noise than an 1.5 bit MDAC. The difference is even

larger for the 2*nd* stage. The 2*nd* 2.5 bit MDAC stage produces 69 % less noise than a 2*nd* 1.5 bit MDAC stage.

4.5.2 Noise on Reference Voltage

V_{sub}, applied during the amplification mode, is corrupted by noise. For the 1.5 bit MDAC with non-flip around architecture, the noise σ^2_{sub} of the reference voltage has a gain of 1 to the input of the MDAC. Input voltage V_{1C} subtraction voltage V_{sub} are applied to the same capacitor C_C1. The 2.5 bit MDAC has a more complex structure. Three of the four input capacitors are used to build the subtraction voltage, depending on the decision of the sub-ADC.

In the range of $V_{1C} \in [-0.125\,V_{ref}, +0.125\,V_{ref}]$, the subtraction voltages are $V_{sub1} = V_{sub2} = V_{sub3} = 0$. Therefore the noise σ^2_{in} is also zero.

In the range of $|V_{1C}| \in [0.125\,V_{ref}, 0.375\,V_{ref}]$, the subtraction voltages are $V_{sub1} = V_{ref}$ and $V_{sub2} = V_{sub3} = 0$. The resulting noise power at the output of the MDAC is:

$$\sigma^2_{out} = \sigma^2_{sub} \cdot 1^2 = \sigma^2_{sub} \tag{4.68}$$

Referring the noise power to the input of the ADC yields:

$$\sigma^2_{in} = \sigma^2_{out} \cdot \left|\frac{1}{4}\right|^2 \tag{4.69}$$

The effective noise voltage at the input of the ADC is shown in (4.70).

$$\sigma_{in} = \sqrt{\sigma^2_{in}} = \sqrt{\sigma^2_{sub} \cdot \left|\frac{1}{4}\right|^2} = \frac{1}{4}\,\sigma_{sub} \tag{4.70}$$

In the range of $|V_{1C}| \in [0.375\,V_{ref}, 0.625\,V_{ref}]$, the subtraction voltages are $V_{sub1} = V_{sub2} = V_{ref}$ and $V_{sub3} = 0$. The effective noise voltage σ_{in} referred to the input of the ADC is calculated in (4.71):

$$\sigma_{in} = \sqrt{\sigma^2_{sub} \cdot \left|\frac{2}{4}\right|^2} = \frac{1}{2}\,\sigma_{sub} \tag{4.71}$$

In the range of $|V_{1C}| \in [0.625\,V_{ref}, V_{ref}]$, all subtraction voltages are equal to the reference voltage $V_{sub1} = V_{sub2} = V_{sub3} = V_{ref}$. The corresponding effective noise voltage σ_{in} referred to the input of the ADC is calculated in (4.72):

$$\sigma_{in} = \sqrt{\sigma^2_{sub} \cdot \left|\frac{3}{4}\right|^2} = \frac{3}{4}\,\sigma_{sub} \tag{4.72}$$

Because of the assumption made in Section 3.5.1, that the noise of the coarse stage can be ignored, the results for a SPA MDAC are also valid for DPA MDACs. The fine stage is the dominant noise source. It has the same gain for the subtraction voltages as a SPA MDAC. The 1*st* and 2*nd* stages of a DPA MDAC also have the same properties regarding noise on the subtraction voltage. Therefore the noise contribution of the 1*st* stage is the largest. Each further stage produces 1/4 less noise referred to the ADC input.

The gain of the subtraction voltage relative to the input is higher for the 1.5 bit MDAC than for the 2.5 bit MDAC. This is due to the lower MDAC-gain of the 1.5 bit MDAC.

4.5.3 Op-Amp Noise

The dominant noise source of the op-amp is the transconductance g_m. In Section 3.5.3,(3.95) the noise power at the output of the MDAC is calculated. The noise power σ_{out} at the output of the op-amp is dependent on the capacitive load C_L of the op-amp. The 2.5 bit MDAC has more capacitive load C_L than the 1.5 bit MDAC, because the input capacitors of the next 2.5 bit MDAC are twice as large. This results in a smaller noise on the output of the 2.5 bit MDAC. Also the capacitive load of a DPA MDAC is larger than the capacitive load of a SPA MDAC. The noise power σ_{in}^2 referred to the input of the ADC is calculated by:

$$\sigma_{in}^2 = \frac{2}{3} \cdot \frac{kT}{C_L} \cdot \left| \frac{1}{G} \right|^2 \tag{4.73}$$

Where C_L is the capacitive load of the op-amp and G is the gain of the MDAC.Table 4.3 shows input referred noise voltage σ_{in} for SPA and DPA MDACs with 1.5 bit and 2.5 bit structures. If capacitors are not scaled, the $1st$ stage of a DPA ADC has the same capacitive load as the $2nd$ stage. Therefore the noise contribution to the input of the MDAC is scaled by a factor of 2 for SPA ADCs and DPA ADCs. Note that the capacitive parasitic capacitor at the output of the op-amp is not considered in this consideration. caused by the op-amp of the MDAC

Table 4.3: Input referred noise voltage σ_{in} caused by the op-amp of the MDAC.

$\sigma_{in}\ [\mu V]$	1.5 bit MDAC	2.5 bit MDAC
SPA	$0.24\sqrt{\frac{kT}{C_f}}$	$0.18\sqrt{\frac{kT}{C_f}}$
DPA	$0.18\sqrt{\frac{kT}{C_f}}$	$0.14\sqrt{\frac{kT}{C_f}}$

It can be seen that the 2.5 bit MDAC produces less noise referred to the input. Furthermore, it turns out that the DPA structure is better than the SPA structure due to the higher capacitive load

No simulations were performed for the noise behavior of single MDAC stages due to time constraints. The noise behavior of the pipeline ADC using DPA MDAC was simulated with the Matlab model and is discussed in Section 5.4.

4.6 Offset Voltage

The impact of the offset voltage on the 1.5 bit structure is discussed in Section 3.6. The 2.5 bit structure differs in the feedback factor k and in the MDAC gain G. The offset error of the coarse stage is ignored because it is reduced by the fine stage. For DPA MDACs only the fine stage is considered.

In this section, the amplification of the offset error for the fine stage and for the single path amplification MDAC is derived and referred to the input. Finally the 2.5 bit structure is compared with the 1.5 bit structure using Table 4.4.

2.5 bit DPA MDAC. Figure 4.15 shows the $1st$ fine stage with offset voltage V_{offs} as input. The op-amp is wired as a non-inverting amplifier. Its transfer function is:

$$\frac{V_{2F}}{V_{Offs}} = \frac{\sum_{i=1}^{4} C_{Fi} + C_{FC} + C_{Ff} + C_{Fp}}{C_{Ff}} = 7 + \frac{C_{Fp}}{C_{Ff}} \tag{4.74}$$

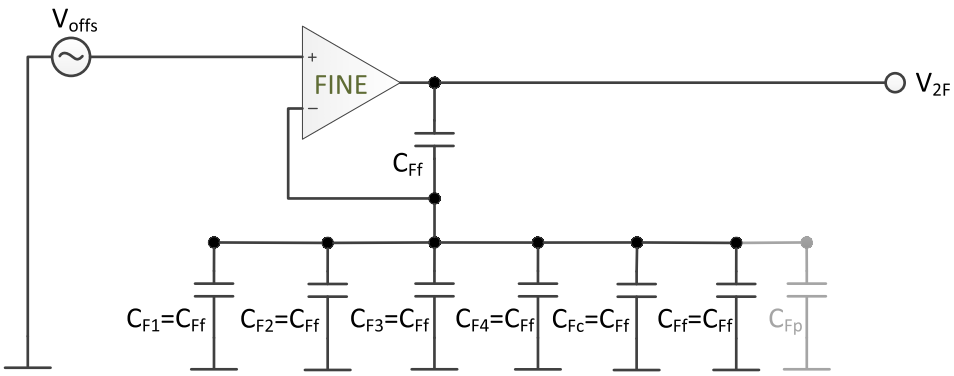

Figure 4.15: Schematic of the 1st fine stage with offset voltage V_{offs} as input. The topology yields a non inverting amplifier

The offset voltage is amplified by a factor of 8 if the parasitic capacitor is assumed to be $C_{Fp} = C_{Ff}$.

A $2nd$ fine stage amplifies the offset voltage with a factor of 12 if $C_{Fp} = C_{Ff}$. This is because of the fine input capacitor C_{F2}. The transfer function is shown in (4.75).

$$\frac{V_{2F}}{V_{Offs}} = \frac{\sum_{i=1}^{5} C_{Fi} + C_{Fc} + C_{Ff} + C_{Fp}}{C_{Ff}} = 11 + \frac{C_{Fp}}{C_{Ff}} \tag{4.75}$$

2.5 bit SPA MDAC. The SPA MDAC has less capacitors than to the DPA MDAC. The transfer function yields:

$$\frac{V_{2F}}{V_{Offs}} = \frac{\sum_{i=1}^{4} C_{Fi} + C_{Ff} + C_{Fc}}{C_{Ff}} = 5 + \frac{C_{Fp}}{C_{Ff}} \tag{4.76}$$

The offset voltage is amplified by a factor of 6 if $C_{Fp} = C_{Ff}$.

Table 4.4: Gain of the offset voltage V_{offs} referred to the ADC input. The parasitic capacitor is assumed to be $C_{Fp} = C_{Ff}$.

Gain: $\frac{V_{in}}{V_{offs}}$	1.5 bit MDAC	2.5 bit MDAC
SPA $1st$ stage	2	1.5
DPA $1st$ stage	2.5	2
DPA $2nd$ stage	1.5	1.75

1.5 bit vs. 2.5 bit MDAC. In order to compare 1.5 bit to 2.5 bit MDACs, it is reasonable to refer the gain of the offset voltage to the ADC input. Table 4.4 shows the gain factor of the offset error referred to the input of the ADC. The DPA MDAC is more critical regarding offset voltage than the SPA MDAC.

Matlab simulations were performed for the overall ADC and are discussed in Section 5.5.

5 Overall Error Compensated Pipelined ADC

The MDAC stage using DPA technique is discussed in Chapters 3 and 4, precision and errors of the analog residue voltage are evaluated. This chapter is about the overall pipelined ADC. The digital output of the ADC is investigated using spectral analysis and the following errors are discussed on the basis of the results of the Matlab simulation:

finite DC gain

capacitor mismatch

noise sources

offset voltage

First the topology of the overall pipelined ADC is introduced, after which the errors are discussed by comparing ADCs with 1.5 bit MDACs to ADCs with 2.5 bit MDACs.

5.1 Topology

The pipelined ADC is composed of several cascaded stages, each pipeline stage consists of a *sub-ADC* and an *MDAC*. The MDAC is described in Section 3.1 and Section 4.1. The digital output of a stage D_i consists of 2 bits for a 1.5 bit stage or 3 bits for a 2.5 bit stage. One bit of each stage is used for the digital correction, taking into account the digital output of the following stage. The last stage is a flash converter and does not need Digital Error Correction (DEC) , its output is 1 bit only. The structure of the error compensated pipelined ADC is shown in figure 5.1.

The digital output D_i is obtained by converting the coarse output of the MDAC_{i-1} to a digital value. The analog input of stage i is built in MDAC_i, summing up the coarse and the fine output voltage of MDAC_{i-1} in both fine and coarse stage. The signal path from one pipeline stage to the next is shown in Figure 5.2

The *digital correction logic* block builds the digital output of the overall ADC, i.e. a weighted sum of D_i. The digital output D_{N+1} of the *flash converter* is weighted with 1, the digital output of the first pipeline stage is weighted with the highest factor. For a 12 bit pipelined ADC with

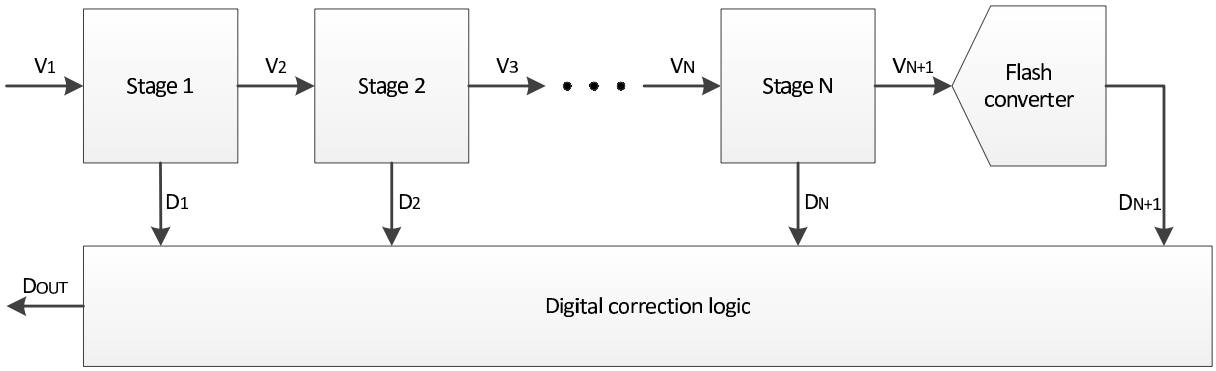

Figure 5.1: Structure of a pipelined ADC

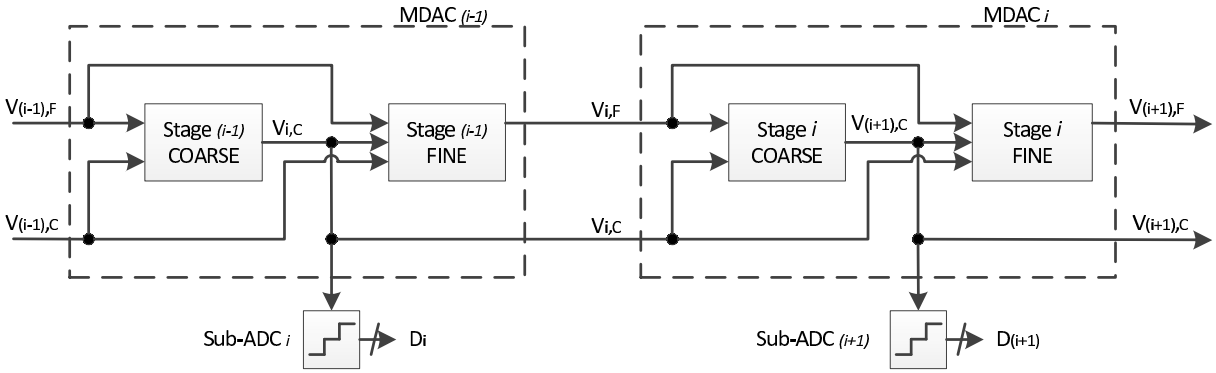

Figure 5.2: Signal path between pipeline stages

eleven 1.5 bit stages and one 1 bit flash converter at the end, the sum yields:

$$D_{OUT} = \sum_{i=1}^{11} 2^{11-i} D_i + D_{12} \tag{5.1}$$

For a 12 bit pipelined ADC with five 2.5 bit stages and one 2 bit flash converter:

$$D_{OUT} = \sum_{i=1}^{5} 2 \cdot 4^{5-i} D_i + D_6 \tag{5.2}$$

Pipeline stages do not all have the same requirements with regard to the residue error. The first stage has the strongest requirements, following stages can be relaxed. This topic was discussed in Sections 3.3.2 and 4.3.1. The Matlab simulations were performed without scaling for simplicity. Therefore the first pipeline stage is the dominant error source.

An overall pipeline ADC built of 2.5 bit MDACs has less pipeline stages than an ADC built of 1.5 bit MDACs. Each 2.5 bit MDAC converts 2 bits, whereas an 1.5 bit MDAC converts only 1 bit. Incidentally, ADCs built of 1.5 bit MDACs and ADCs built of 2.5 bit MDACs have the same structure. Differences between the topologies of 1.5 bit MDACs and 2.5 bit MDACs are shown in Section 4.1.

5.2 Finite DC Gain

The finite *DC gain* of the op-amp used in MDACs introduces a systematic error. The DC gain of the op-amp is limited by g_m and g_{ds} of the input and output stages. There is a deviation

in the DC gain due to mismatch in the op-amp, which cannot be compensated for by simply adapting the loop gain of the MDAC via the feedback capacitor. The impact of finite DC gain on the residue error is discussed in detail in Sections 3.3 and 4.3. This section is focused on how finite DC gain affects the digital output of the overall ADC.

5.2.1 Linearity Considerations for 1.5 Bit MDAC

The DPA structure contains two op-amps, each of them has finite DC gain $A_{0,C}$ and $A_{0,F}$. To better describe the MDAC as one unit, the sum $A_{0,sum} = A_{0,C} + A_{0,F}$ and the difference $\Delta A_0 = A_{0,C} - A_{0,F}$ are introduced. Capacitor mismatch in the MDAC is ignored for these considerations on the effect of finite DC gain.

The sum of DC gains $A_{0,sum}$ is important for the *effective resolution* achievable for the ADC. It is dependent on the sum of $A_{0,C}$ and $A_{0,F}$, as can be seen in Figure 5.3. The difference ΔA_0 is constant for every curve. Considering the red curve with $\Delta A_0 = 20\,\text{dB}$, at the value $A_{0,sum} = 90\,\text{dB}$ on the x-coordinate, the coarse DC gain is $A_{0,C} = 60\,\text{dB}$ and the fine DC gain is $A_{0,F} = 40\,\text{dB}$. The red curve shows the best result, where decreasing the difference also decreases the effective resolution achievable. In Table 5.1 you can see the necessary sum of DC gains for effective resolutions, referring to the red curve.

ENOB	$A_{0,sum}$
10 bit	75 dB
11 bit	82 dB
12 bit	89 dB

Table 5.1: DC gain needed for the effective resolution

The worst result is given by $\Delta A_0 = -10\,\text{dB}$ (black curve), further decreasing of ΔA_0 slightly improves the result again. However the difference between the curves gets smaller with higher overall DC gain. It is 0.2 bits for $A_{0,sum} = 70\,\text{dB}$, and only 0.06 bits for $A_{0,sum} = 90\,\text{dB}$ and 12 bits effective resolution.

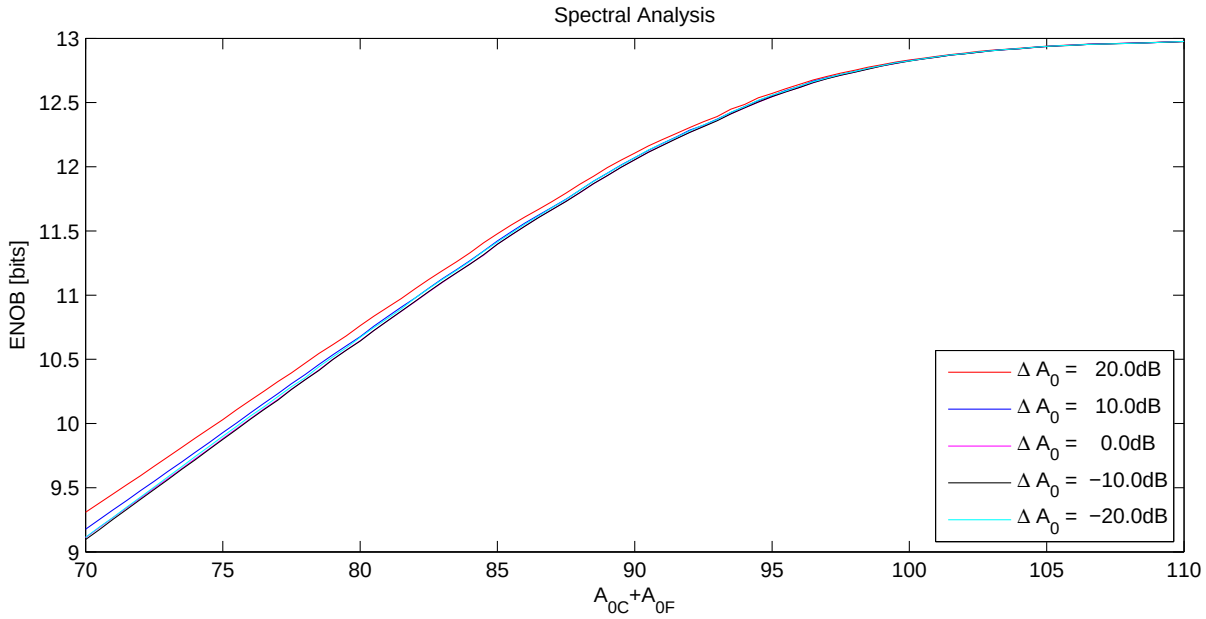

Figure 5.3: Gain Error: 1.5 bit MADC - 13 bitADC - Dual Path Amplification

5.2.2 Linearity Considerations for 2.5 Bit MDAC

Figure 5.4 shows the behavior of a 13 bit ADC with 2.5 bit MDAC related to finite *DC gain*. The same range of $A_{0,sum}$ and the same values for ΔA_0 as in Figure 5.3 are used. Comparing the two plots, it can be observed that 2.5 bit MDAC stages cause a wider spread of the curves. In particular, the cyan curve with $\Delta A_0 = -20\,\text{dB}$ has a kink and drops down faster for $A_{0,sum} < 85\,\text{dB}$. Looking at Figure 5.3, the corresponding curve shows a similar performance to the magenta and black curves ($\Delta A_0 = 0\,\text{dB}$, $-10\,\text{dB}$), it is even slightly better. According to these results $A_{0,C}$ greater than $A_{0,F}$ should be chosen for the 2.5 bit MDAC structure to get the best result for a given sum of DC gains. On the other hand, reducing $A_{0,C}$ cannot be compensated for by adding the same DC gain at $A_{0,F}$.

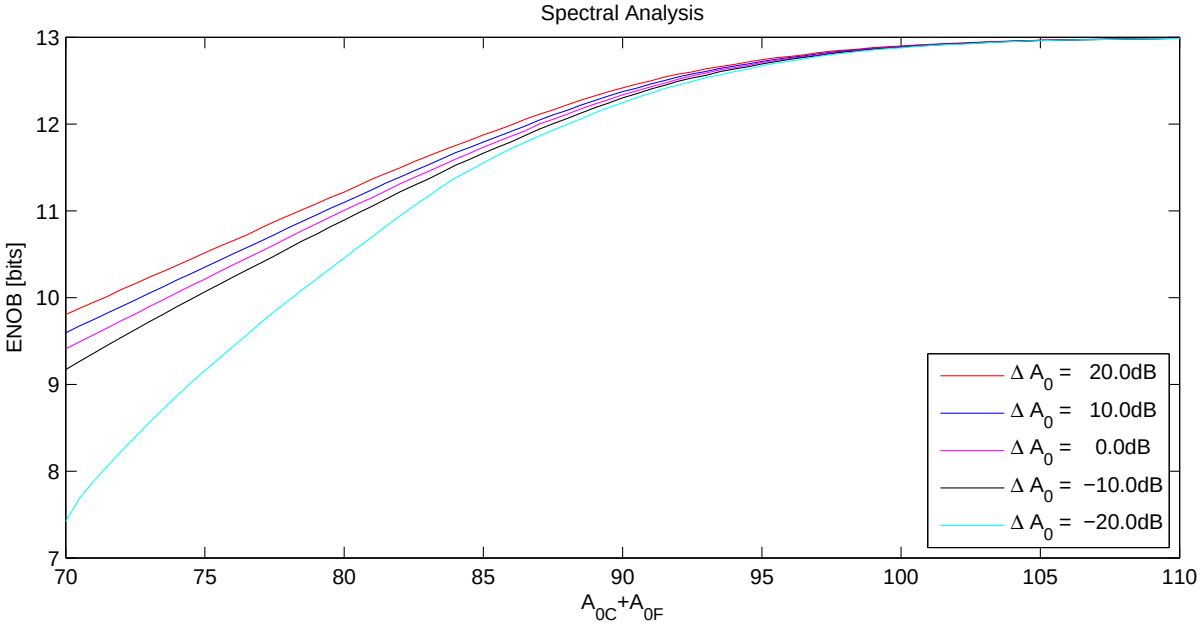

Figure 5.4: Finite DC gain: 2.5 bit MDAC - 13 bit ADC - Dual Path Amplification

Table 5.2 lists the requirements for $A_{0,sum}$ assuming $\Delta A_0 = 20\,\text{dB}$.

ENOB	$A_{0,sum}$
10 bit	71 dB
11 bit	78.6 dB
12 bit	86 dB

Table 5.2: DC gain needed for the effective resolution

In Figure 5.5 ADCs with 2.5 bit and 1.5 bit MDAC structures are compared, ΔA_0 is assumed to be 0. According to the investigations of MDAC stages in Sections 3.3 and 4.3, the performance of the 2.5 bit MDAC ADC is better for the same overall DC gain. The effective resolution of the ADC with 2.5 bit per stage is 0.33 bits higher at $A_{0,sum} = 90\,\text{dB}$.

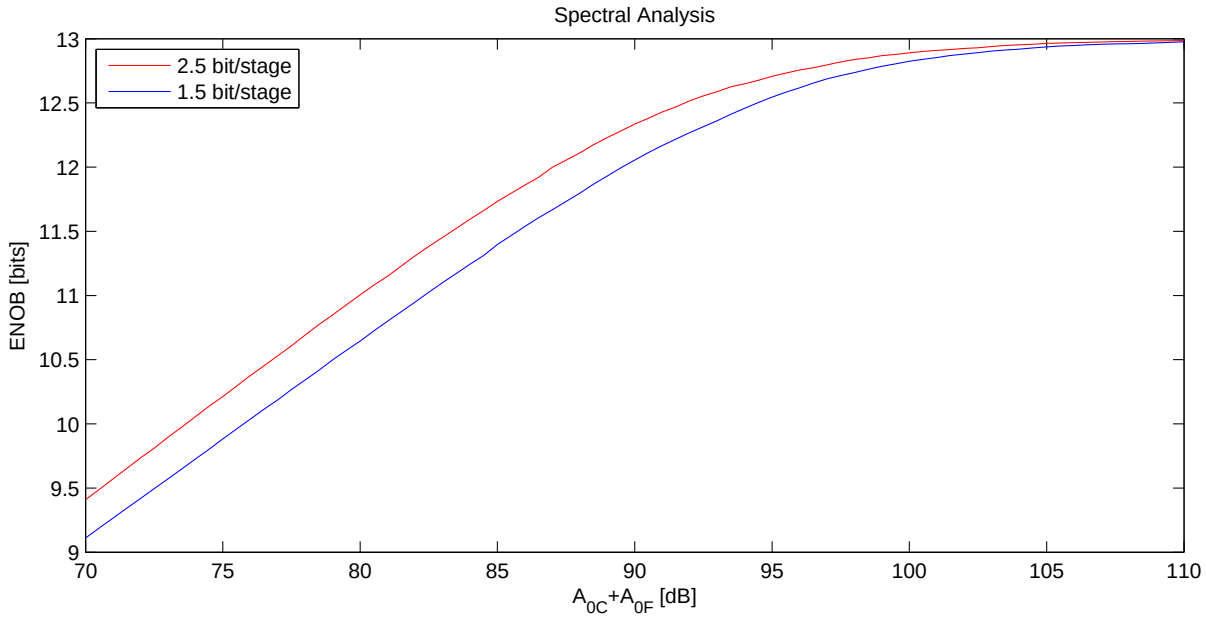

Figure 5.5: Finite DC gain: 13 bit - ADC with Dual Path Amplification

5.3 Capacitor Mismatch

As we saw in chapters 3 and 4, *capacitor mismatch* is a critical point of the pipelined ADC with 12 bits or more, because the technology used limits the accuracy achievable of the *analog error compensated* MDAC. The criteria expressed in chapters 3 and 4 give information about the performance and errors of the residue generating MDAC, however finally the quality of digital ADC output is of interest. Consider the signal path of the error compensated pipelined ADC in Figure 5.2, The $sub-ADC_i$ converts the output of the i-th coarse stage. The error compensated residue is only built in the next stage $MDAC_i$, where subtraction and multiplication operation are also performed at the same time. Hence the error compensated residue is not available as a voltage. The simulation of the pipelined ADC show that the investigations made on one MDAC stage are also meaningful for the performance of the overall ADC. This chapter deals with the effect of *capacitor mismatch* on the ADC linearity. For this purpose, op-amps in the MDAC are assumed to be ideal.

5.3.1 Linearity Considerations for 1.5 Bit MDAC

The Matlab model for the 1.5 bit ADC contains 11 MDAC stages, where the capacitors of each stage display an independent variation from the nominal values. The variation σ_{abs} of each capacitor from its nominal value is Gaussian distributed, the pairwise capacitor mismatch σ_c is obtained by [5]:

$$\sigma_c = \sqrt{\sigma_{abs}^2 + \sigma_{abs}^2} = \sqrt{2\sigma_{abs}^2} = \sqrt{2} \cdot \sigma_{abs} \tag{5.3}$$

The last stage is a flash converter with 1 bit resolution. It is considered to be an ideal comparator. In practice it is common to choose a higher resolution for the flash converter such as 2 bits or 3 bits to save energy and chip area, thus reducing the number of stages. However in this thesis the flash converter is not the subject of investigation. For an ideal flash converter the 1 bit configuration represents the worst case for the ADC errors, because more non ideal stages are involved.

In Figure 5.6 you can see three distributions of Effective Number of Bits (ENOB), for a

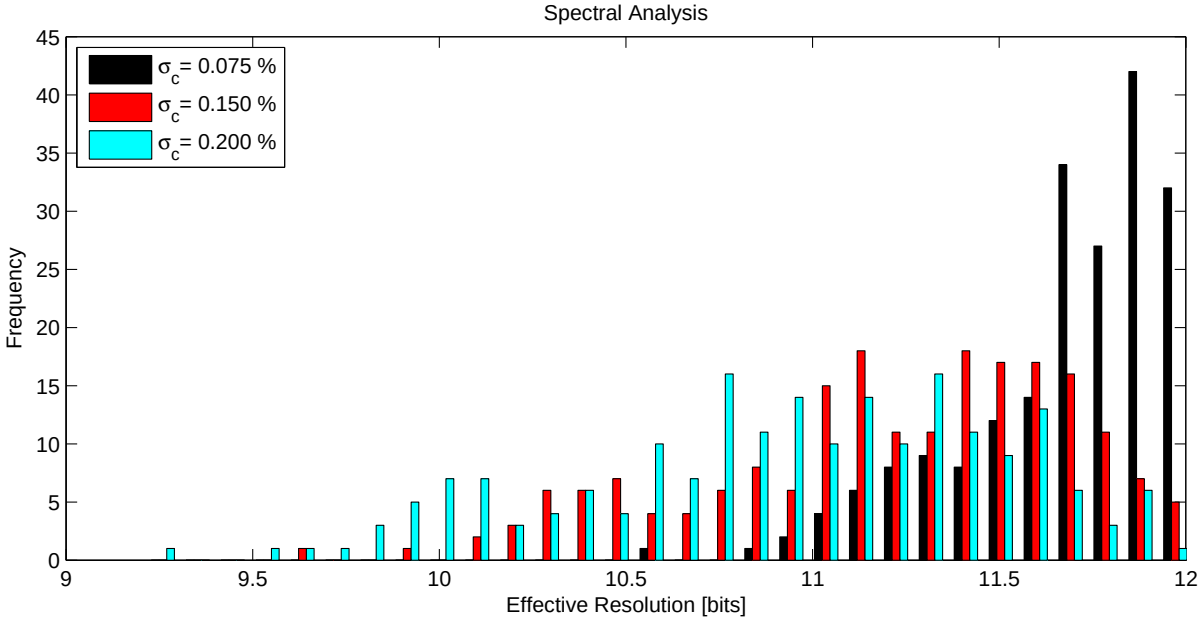

Figure 5.6: Capacitor mismatch: 12 bit - ADC with Single Path Amplification

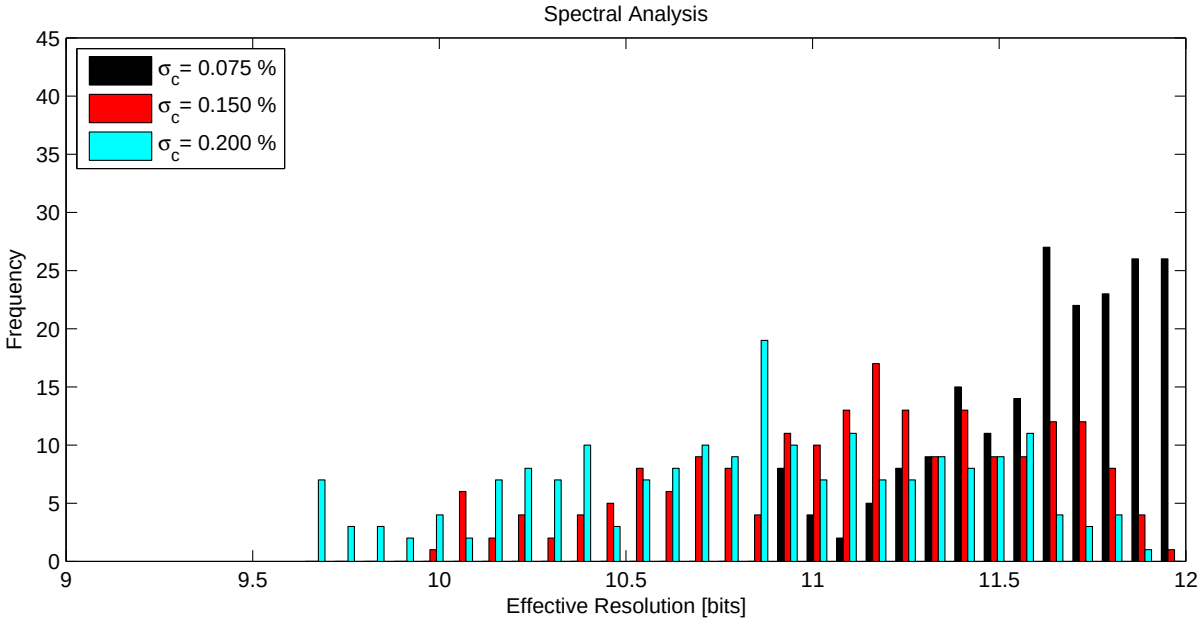

Figure 5.7: Capacitor mismatch: 12 bit - ADC with Dual Path Amplification

12 bit ADC built of 1.5 bit SPA MDACs. The black distribution shows the best case for 40 nm technology with a capacitor mismatch of 0.076%. This minimum capacitor mismatch is the result of a Spice simulation as depicted in Figure 3.13. When the mismatch is increased, the distribution is spread over a wider range of values and the center of the distributions moves to a lower ENOB. The shape of each distribution is similar, this is because the same random numbers are used for capacitor deviation in all the simulations. They were just scaled to obtain the desired standard deviation.

Figure 5.7 shows the same simulation performed for the ADC with DPA. It can be observed, that the distributions resulting from the DPA are more compact than in the SPA case. This is desirable and makes it more easy to evaluate the performance of the ADC. Consider the black

distribution, the lowest ENOB value at 10.91 bits appears 8 times, while the distribution for SPA for the same mismatch in Figure 5.6 is continuous and slower decreasing with an outlier at 10.56 bits.

Figure 3.18 depicts the $3\,\sigma$ value of the residue error of a 1.5 bit MDAC, dependent on capacitor mismatch σ_c. The residue error for a mismatch of $\sigma_c = 0.076\,\%$ is about $2\,LSB_{12}$ for the DPA MDAC and for the SPA MDAC. This corresponds to an input referred mismatch error of $1\,LSB_{12}$, or $\mathrm{LSB}_{10}/4$. The simulation of the overall ADC shows an effective resolution of more than 10.5 bits for a residue error of $\mathrm{LSB}_{10}/2$ on the output of each MDAC stage.

5.3.2 Linearity Considerations for 2.5 Bit MDAC

The Matlab model for the ADC with 2.5 bit per MDAC consists of 5 MDAC stages, each contributing 2 bits to the 12 bit resolution. The $6th$ pipeline stage is a 2 bit flash converter. As in the 1.5 bit case, each capacitor of the ADC has a Gaussian distributed deviation σ_{abs} from the nominal value. Capacitors are deviated independently, which causes a pairwise mismatch σ_c between the capacitors. In the simulation only the last two bits are converted ideally from the flash converter. Nevertheless the first pipeline stage is the dominant error source because no scaling is included.

Figure 5.8 and Figure 5.9 show distributions of effective resolutions for ADCs built of SPA MDACs and DPA MDACs. The lowest values of the black distributions are at 11.2 bits. When only considering mismatch, an ADC built of 2.5 bit MDAC stages reaches a similar effective resolution regardless of whether it uses SPA or DPA.

Figure 5.10 and Figure 5.11 shows a quantile of the distribution of effective resolution which has a 99.73 % probability to exceed the resolution depicted. With this representation it is more easy to compare the effective resolution of the ADCs. Figure 5.11 compares an ADC built of 2.5 bit SPA MDACs (black dashed) to an ADC built of 2.5 bit DPA MDACs (red continuous). The two graphs differ only very slightly. Figure 5.10 campares an ADC built of 1.5 bit DPA MDACs (blue) to an ADC built of 2.5 bit DPA MDACs (red). For a mismatch of 0.076 %, it can be achieved an effective resolution that is 0.5 bits higher using the 2.5 bit approach, with respect to 1.5 bit. This corresponds to a factor of $\sqrt{2}$.

Figure 4.13 depicts the $3\,\sigma$ value of the residue error of the 1.5 bit MDAC compared to the 2.5 bit MDAC, dependent on capacitor mismatch σ_c. It can be observed that the residue errors of SPA MDACs and DPA MDACs only differ slightly. This corresponds to the results of Figure 5.11 for the overall ADC. When considering the gain of the MDACs, the residue error of the 2.5 bit MDAC and the residue error of the 1.5 bit MDAC differ by a factor of 1.5. It can be seen that the residue error of the MDAC stages is closely related to the effective resolution of the ADC.

The most important findings are:

Considering only capacitor mismatch, ADCs built of DPA MDACs and ADCs built of SPA MDACs have similar effective resolution. Capacitor mismatch in the coarse stage of and MDAC can be compensated for of the fine stage. Mismatch of the fine stage cannot be compensated for.

ADCs built of 2.5 bit MDAC stages can achieve 0.5 bit more effective resolution than ADCs built of 1.5 bit MDAC stages. ADCs built of 2.5 bit MDAC stages have gain 4 and the residue error is relaxed compared to ADCs built of 1.5 bit MDAC stages. The residue error cannot be relaxed by factor 2 because of topology differences, as identified in Section 4.4.

ADCs built of 1.5 bit MDAC stages integrated in CMOS 40 nm technology are limited to about 10.7 bits due to capacitor mismatch, unless mismatch errors are compensated for with digital calibration. ADCs built of 2.5 bit MDAC stages integrated in CMOS 40 nm

technology can achieve 11.2 bits effective resolution. All other error sources are ignored and the ADC contains no scaling for this consideration.

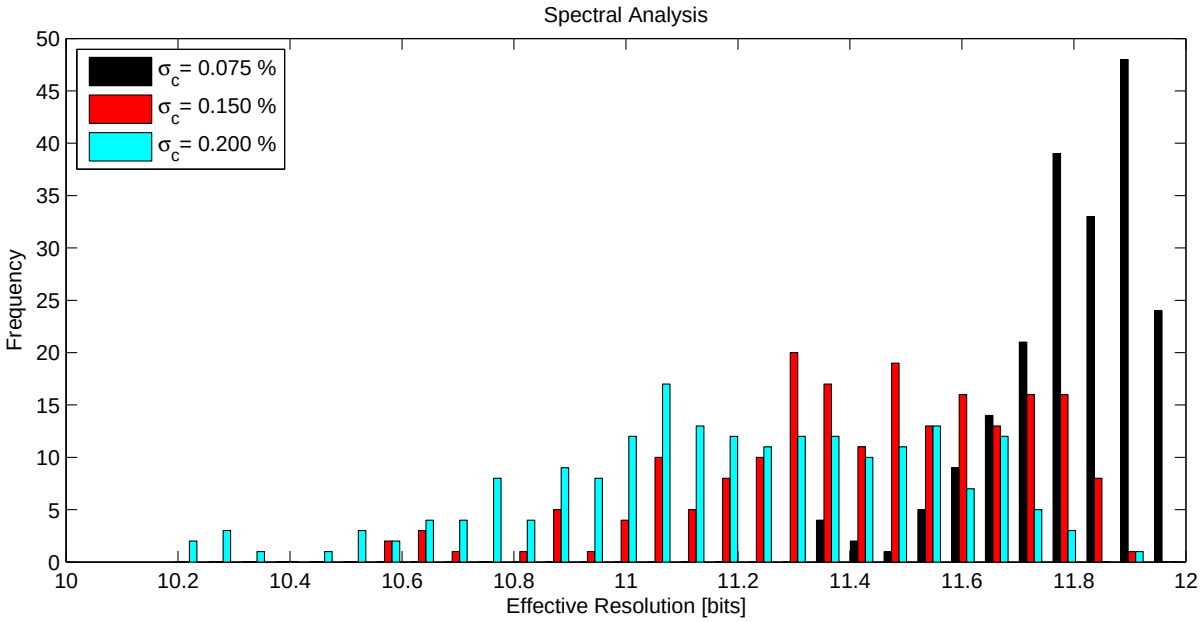

Figure 5.8: Capacitor mismatch: 12 bit - ADC with Single Path Amplification

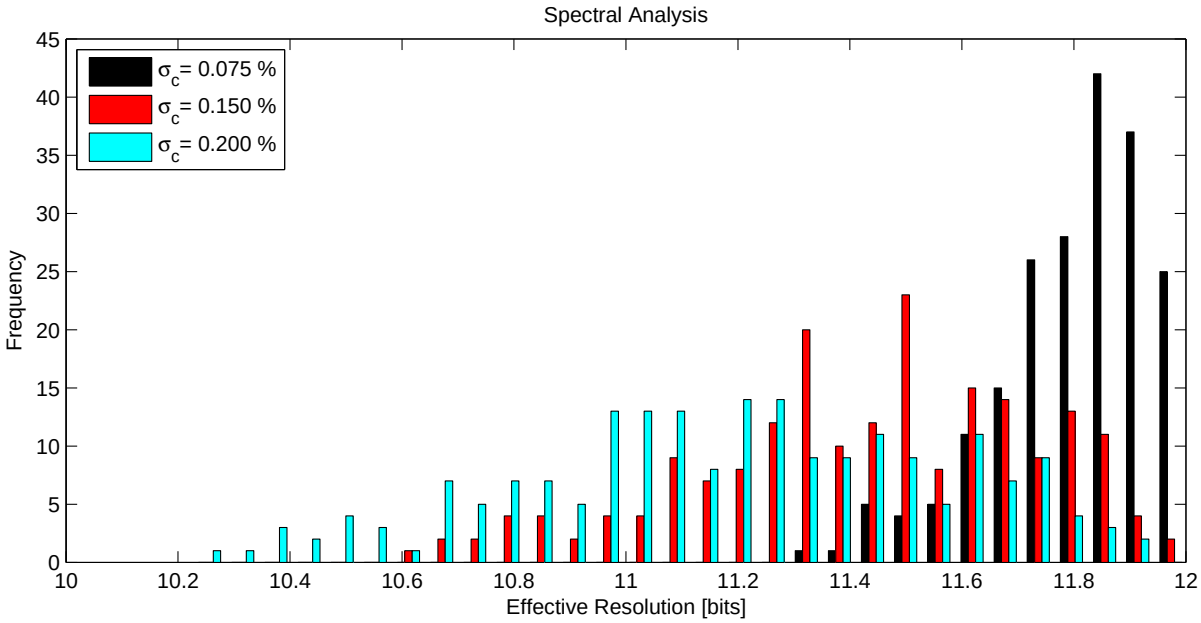

Figure 5.9: Capacitor mismatch: 12 bit - ADC with Dual Path Amplification

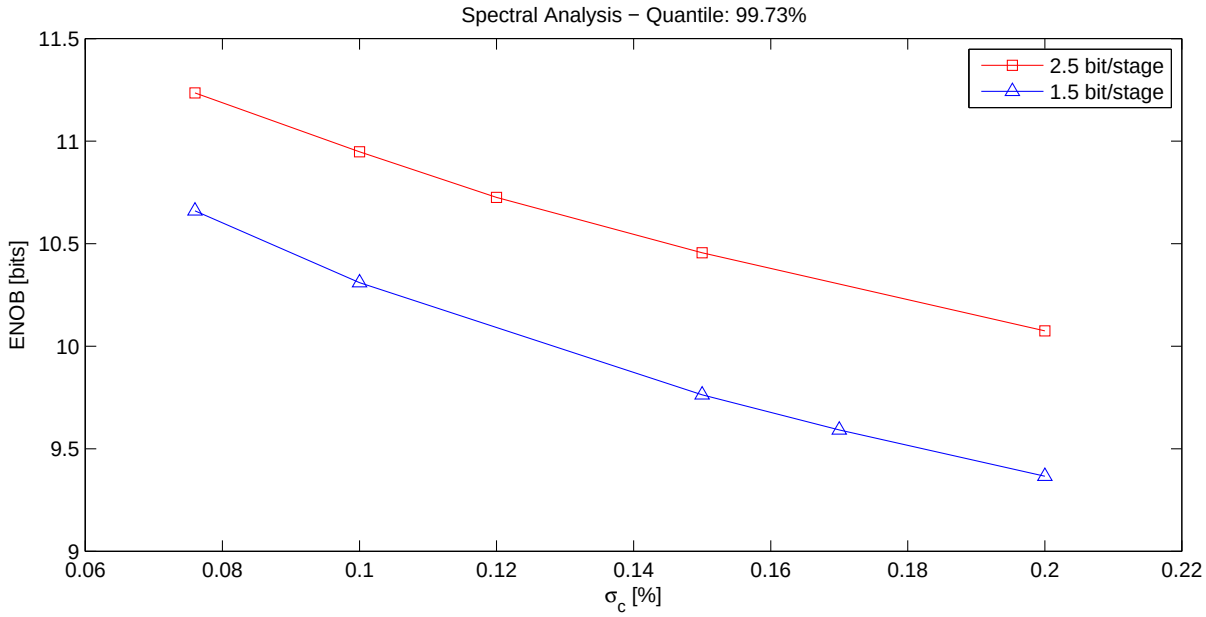

Figure 5.10: Capacitor mismatch: 12 bit - ADC with Single Path Amplification. Quantile of the distribution which has a 99.73 % probability to exceed the resolution depicted

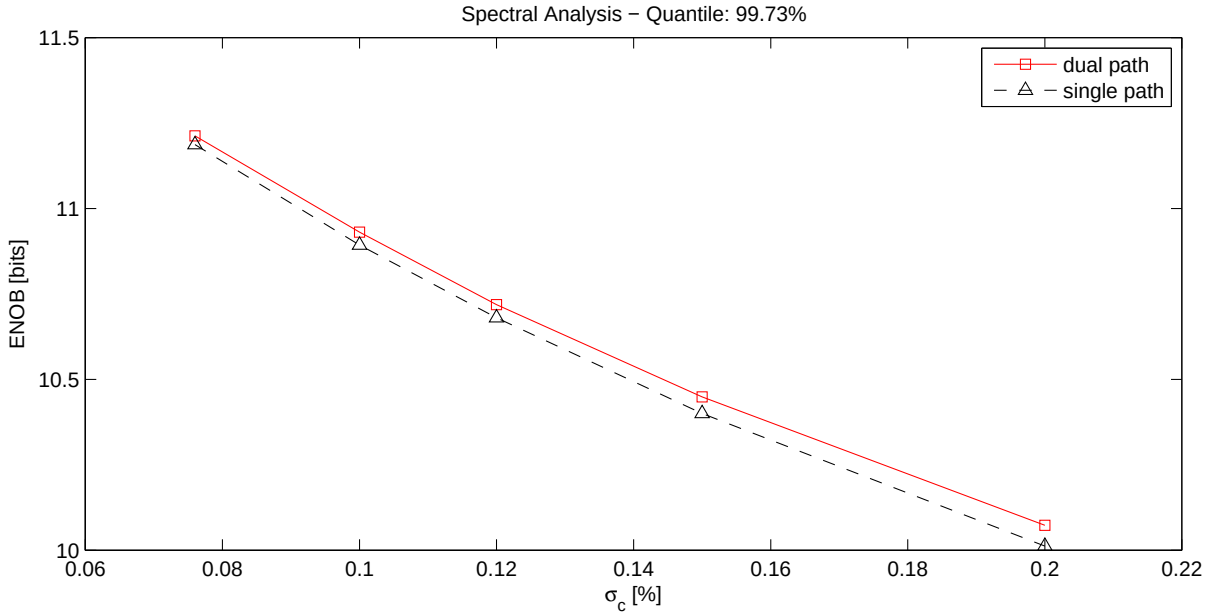

Figure 5.11: Capacitor mismatch: 12 bit - ADC with Dual Path Amplification. Quantile of the distribution which has a 99.73 % probability to exceed the resolution depicted

5.4 Noise Sources

The impact of different noise sources is discussed in Sections 3.5 and 4.5 for a single MDAC stage, where the results are referred to the input of the MDAC stage. Now the previous results will be compared to simulations of the overall pipelined ADC. The Simulation were performed with a sinusoidal input signal of 2^{18} samples. To see the behavior of an ADC built of DPA containing noise sources, a Gaussian distributed noise signal was applied to the input of a 13 bit ADC

5.4.1 Input Referred Noise

Gaussian noise was added to the sinusoidal input signal of the ADC. Figure 5.12 shows the effective resolution of the ADC depending on the standard deviation of input referred noise. This curve shows a *dual path amplification* ADC with 2.5 bit MDAC. The simulation with the *single paht amplification* ADC and with 1.5 bit MDACs shows exactly the same behavior, therefore the curve for one case is sufficient. For an effective resolution of 12 bits, an input referred noise of $\sigma_{Vin} = 120 \cdot 10^{-6} \cdot V_{ref}$ is tolerable. The influence on the design is not the same for all structures, because the noise requirements on the output of the first 2.5 bit MDAC is half compared with the 1.5 bit structure. This is due to the different loop gain of the MDACs.

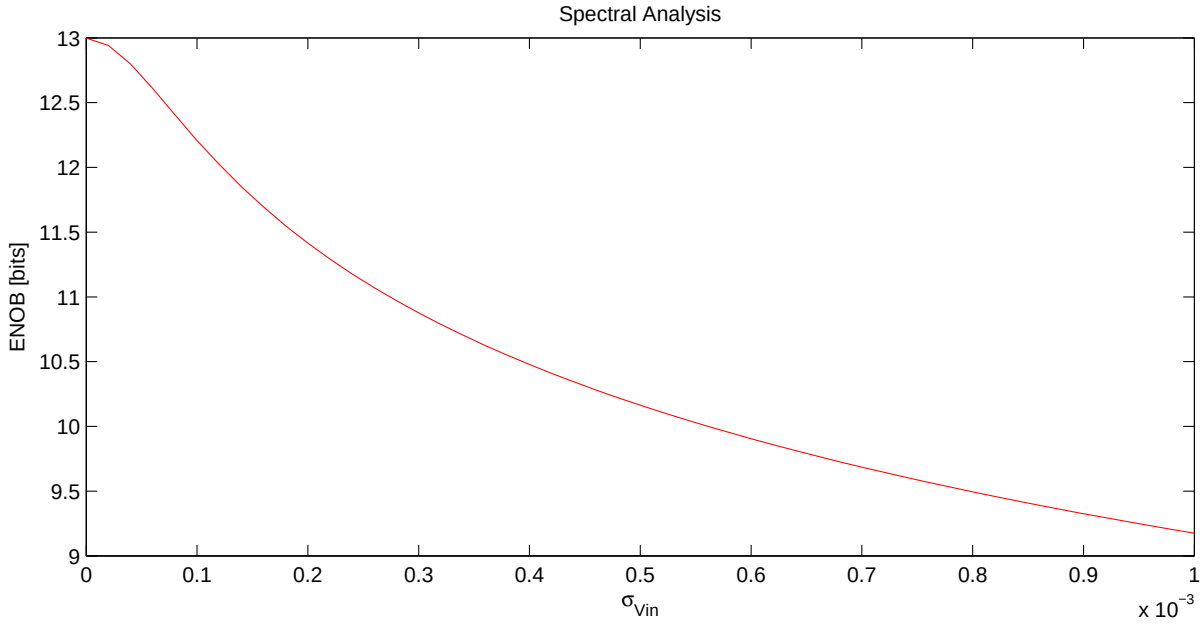

Figure 5.12: 13 bit ADC - noise on Vin - DAP

5.4.2 Noise on the Reference Voltage

The reference voltage of the digital to analog conversion in the MDAC is noise corrupted. The simulation provides a noise source for every reference voltage. Figure 5.13 shows the effective resolution of the MDAC depending on the standard deviation of noise on all reference voltages used in the ADC with DPA MDACs. It can be seen that the 2.5 bit structure allows more noise on the *reference voltage* than the 1.5 bit structure. The curves for ADCs with SPA show the same trend as the corresponding curves for DPA ADCs. Assuming an ADC with 12 bits effective resolution, the noise on thr *reference voltage* can be $\sigma_{Vref} = 200 \cdot 10^{-6} V_{ref}$ for the 1.5 bit MDAC structure and $\sigma_{Vref} = 260 \cdot 10^{-6} V_{ref}$ for the 2.5 bit structure. Thus the 2.5 bit structure can tolerate 1.3 times more noise in this case. Comparing it with the input referred noise, the 2.5 bit structure is relaxed by a factor of 2.

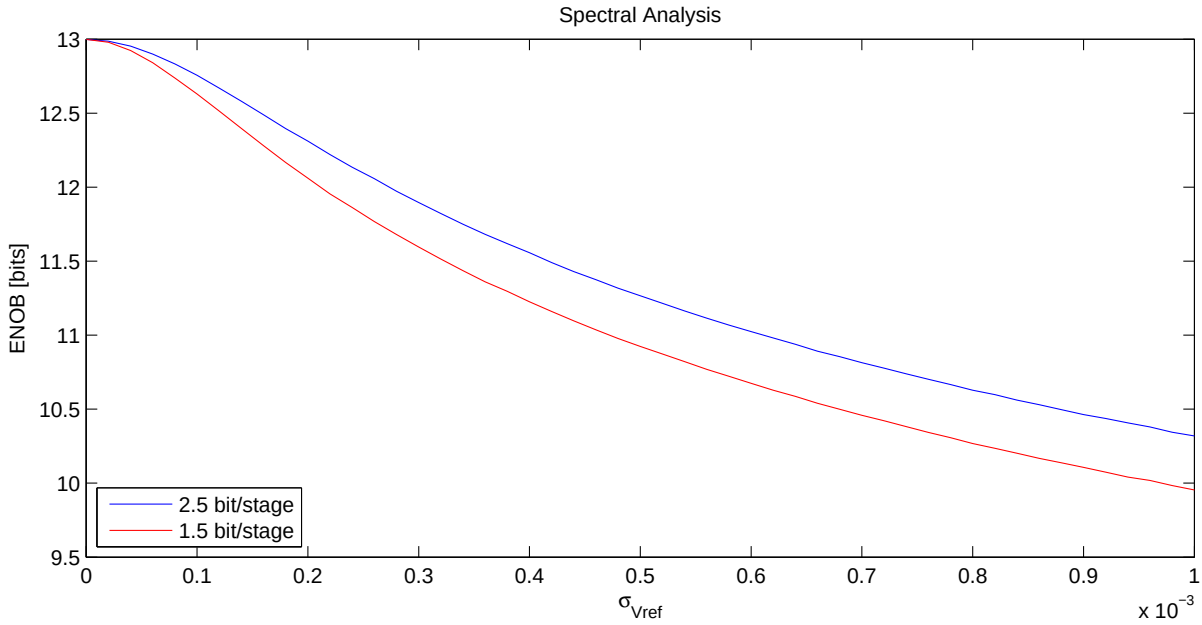

Figure 5.13: 13 bit ADC - noise on Vref - DAP

5.5 Offset Voltage

The offset error of an op-amp is dealt with in Chapters 3 and 4 for a single MDAC stage. In this section the simulation results for the overall pipelined ADC are presented.

5.5.1 Linearity Considerations for 1.5 Bit MDAC

The offset error of op-amps introduces a systematic constant error in each MDAC that is added to the residual voltage. The impact on the residual is discussed in Section 3.6 and Section 4.6. Now we will look at the simulation results for the pipelined ADC and compare the results.

The spectral analysis shows non-linearity errors of the pipelined ADC excluding offset error. The offset of the output waveform is removed from the spectrum before analyzing it. The simulation is performed with a 13 bit pipelined ADC of 12 pipelined stages and one 1 bit flash-converter. An offset voltage is introduced in the op-amps of the 1*st* pipeline stage. The offset voltage is added to the coarse input signal. The input referred offset voltage of the op-amps is investigated.

Sooner or later, the propagation of the offset voltage through pipeline stages causes the residual to leave the interval of ±1. If this happens, the *effective resolution* goes down. For a full scale input voltage, every small offset voltage causes a decrease of the effective resolution. Decreasing the input voltage, the ADC can tolerate a certain amount of offset voltage. The curve goes down where the residue voltage of the MDAC stages leaves the interval of $\pm FS/V_{ref}$(i.e. ±1).

Figure 5.14 shows the effective resolution of a pipeline ADC with offset voltage on the op-amps of the first stage. The curve is a function of the offset voltage. The input voltage is a sine wave with the amplitude of 95 % FS. The blue curve shows an offset only at the coarse op-amp, the red curve only at the fine op-amp.

In the 1.5 bit case it does not matter if the signs of both offset voltages at the coarse and fine op-amp are the same, it leads to the same result. The same offset on both op-amps of the first pipeline stage is shown in Figure 5.15 with the red curve. The blue dashed curve shows an offset on the coarse and fine op-amp with same absolute value but with opposite signs. On the X-Axis you can see absolute values of the offset voltage normalized by the reference voltage.

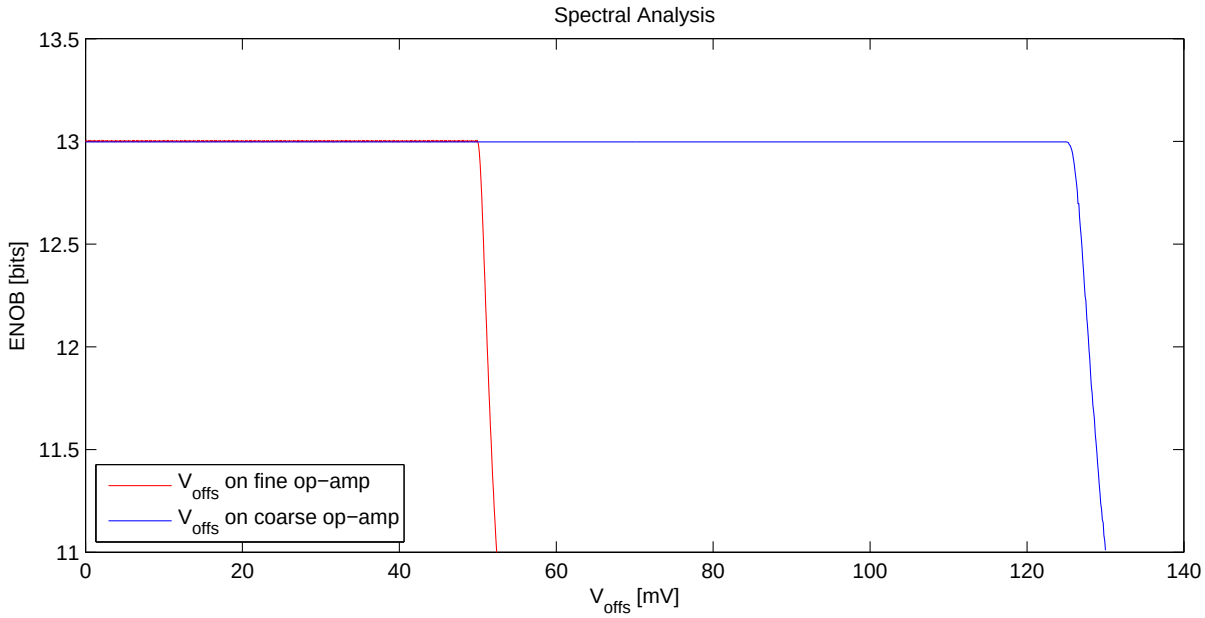

Figure 5.14: Offset Voltage on fine op-amp or coarse op-amp, 1.5 bit MDAC

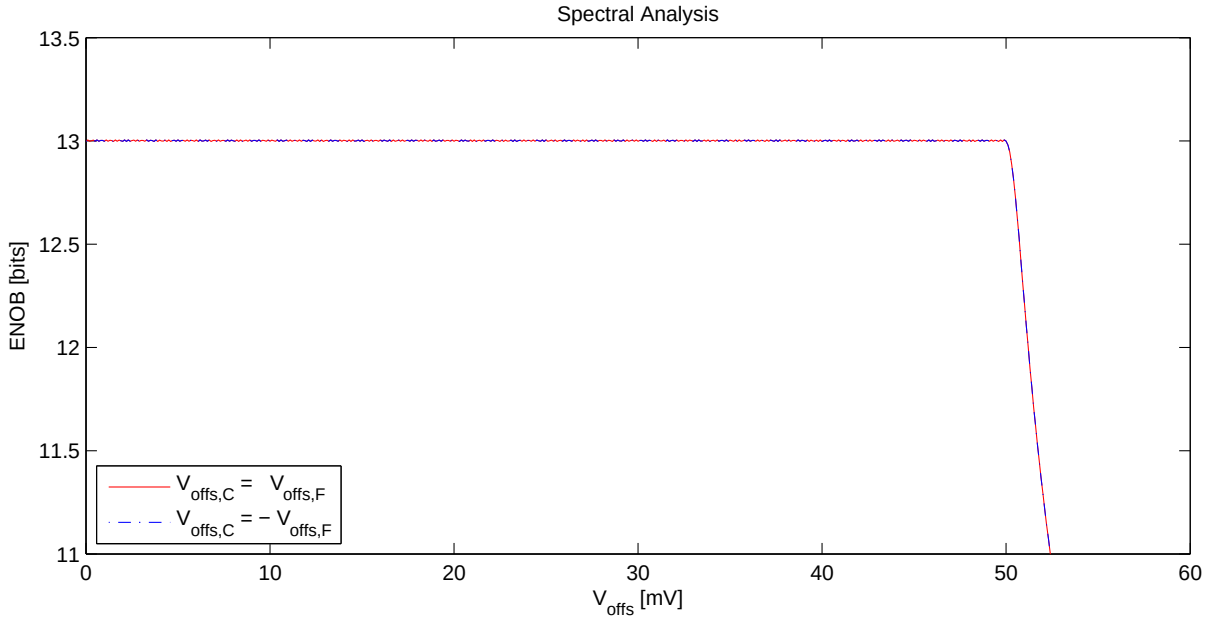

Figure 5.15: Offset voltage on fine op-amp and coarse op-amp, 1.5 bit MDAC

Figure 5.16 shows the impact of the input signal amplitude. The amplitude of the input signal is taken into account when calculating the effective resolution. It is calculated by

$$ENOB = \frac{SINAD - 1.76dB + 20\log\left(\frac{FS}{A_{signal}}\right)}{6.02} \tag{5.4}$$

It can be seen that a smaller input voltage does not cause saturation easily. Decreasing the input signal further, no longer improves the result. This can be seen in Figure 5.17.

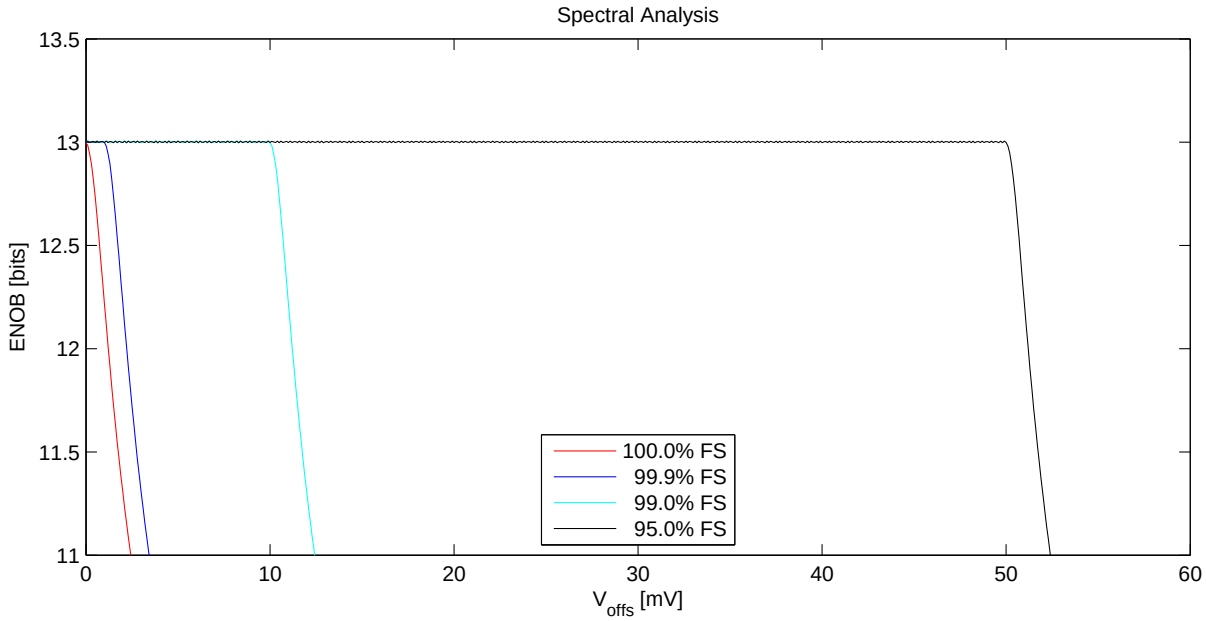

Figure 5.16: 13 bit pipeline ADC, offset voltage on MDAC op-amps, different input amplitudes

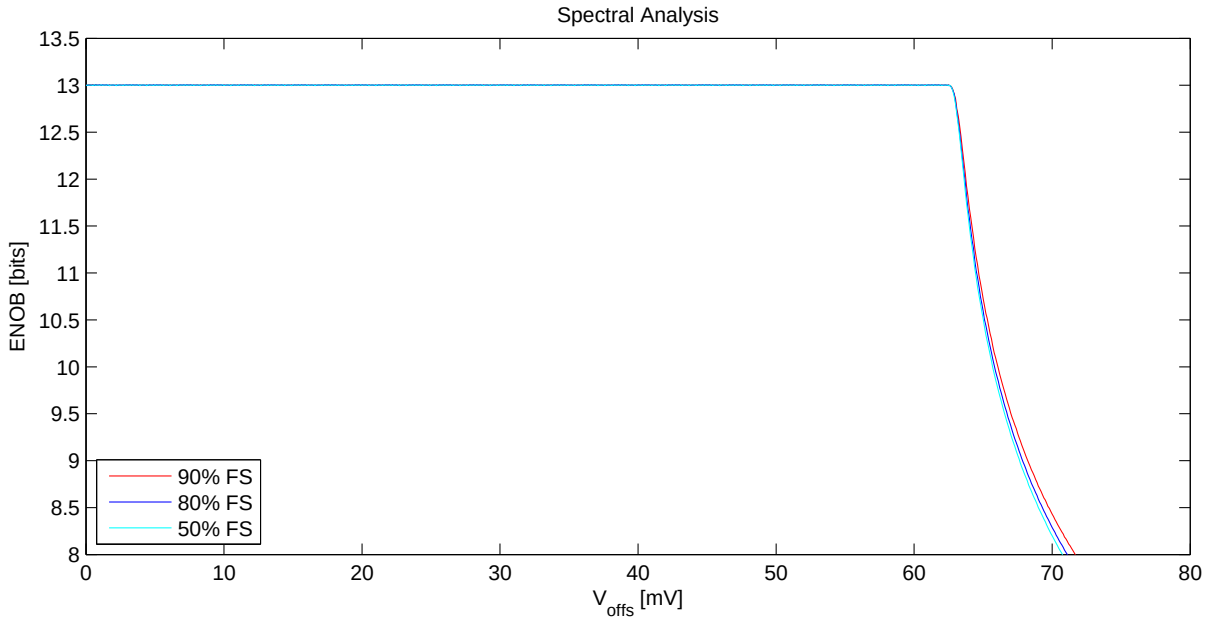

Figure 5.17: 13 bit pipelined ADC, offset voltage on MDAC op-amps, different input amplitudes

5.5.2 Linearity Considerations for 2.5 Bit MDAC

The 2.5 bit structure reacts slightly differently to the offset error than the 1.5 bit structure. In Figure 5.18 it can be seen that the ADC reacts in the same way to an offset voltage on the coarse and on the fine op-amp. Compared to the 1.5 bit case, the offset voltages with different signs have different impact on the linearity of the ADC. This can be observed in Figure 5.19. The 2.5 bit structure behaves similarly to a decreasing input signal amplitude as the 1.5 bit structure. The effective resolution increases with decreasing input signal according to Figure 5.20. A further decrease of the input signal amplitude brings no improvement. This is shown in Figure 5.21. The worst case is given by offset voltages with different signs on the coarse and fine stage. Assume the input signal amplitude to be 95 % FS. The 1.5 bit structure can tolerate an input referred

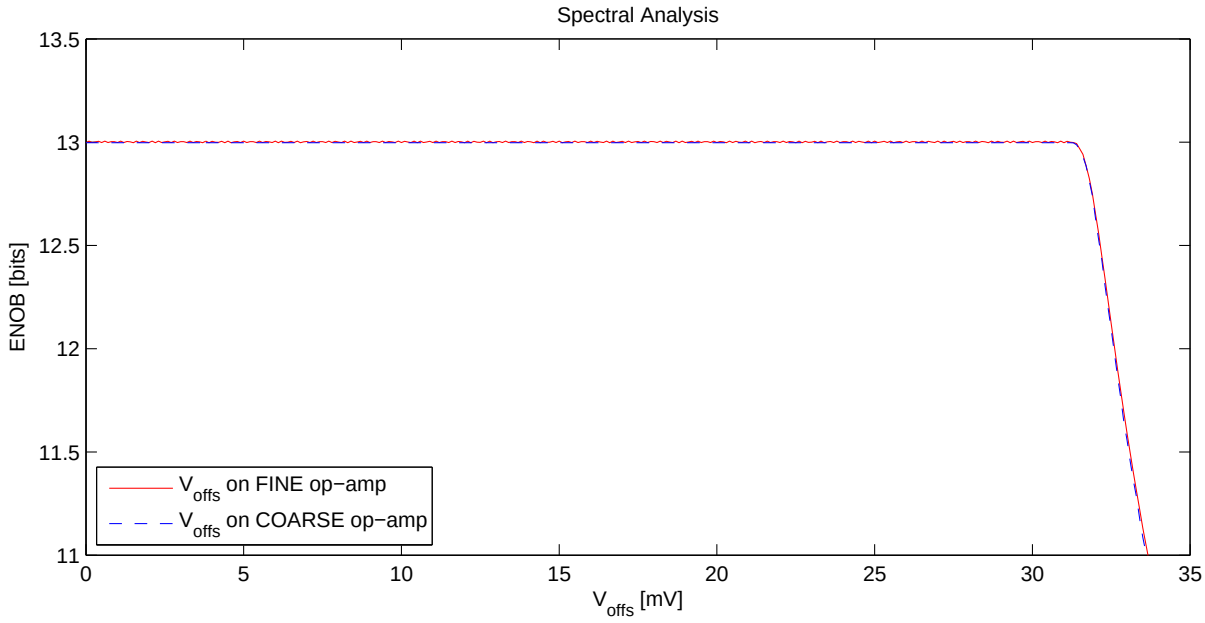

Figure 5.18: Offset voltage on fine op-amp or coarse op-amp, 2.5 bit MDAC

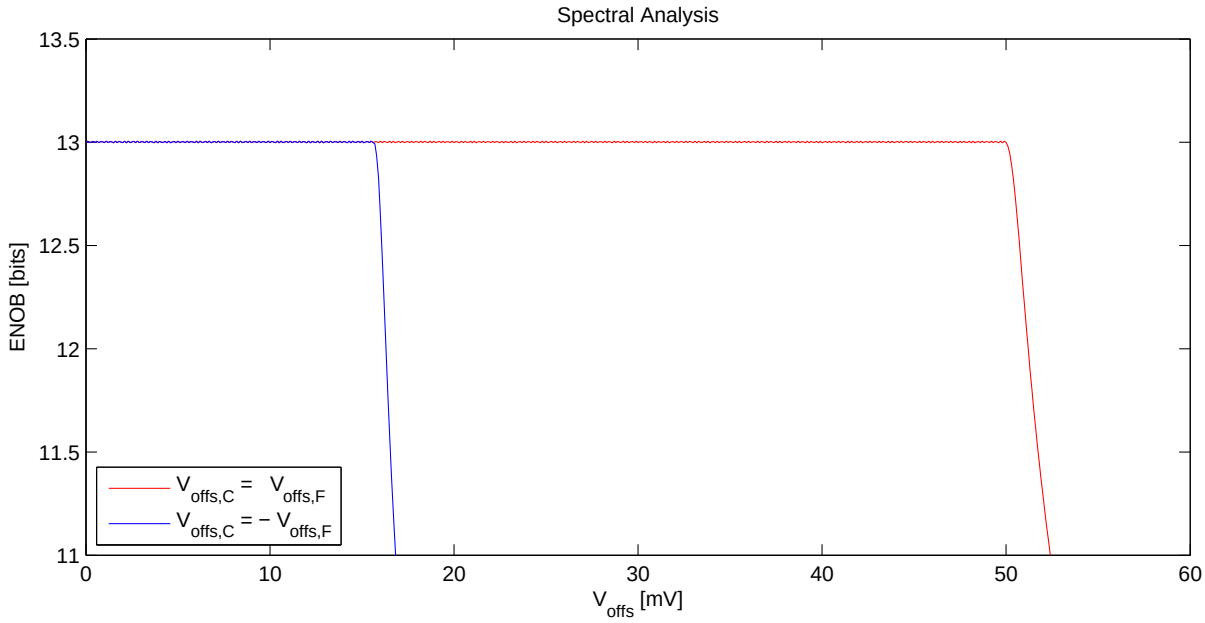

Figure 5.19: Offset voltage on fine op-amp and coarse op-amp, 2.5 bit MDAC

offset voltage of $0.05 \cdot V_{ref}$. The 2.5 bit structure can tolerate only $0.016 \cdot V_{ref}$ to obtain 12 bit effective resolution.

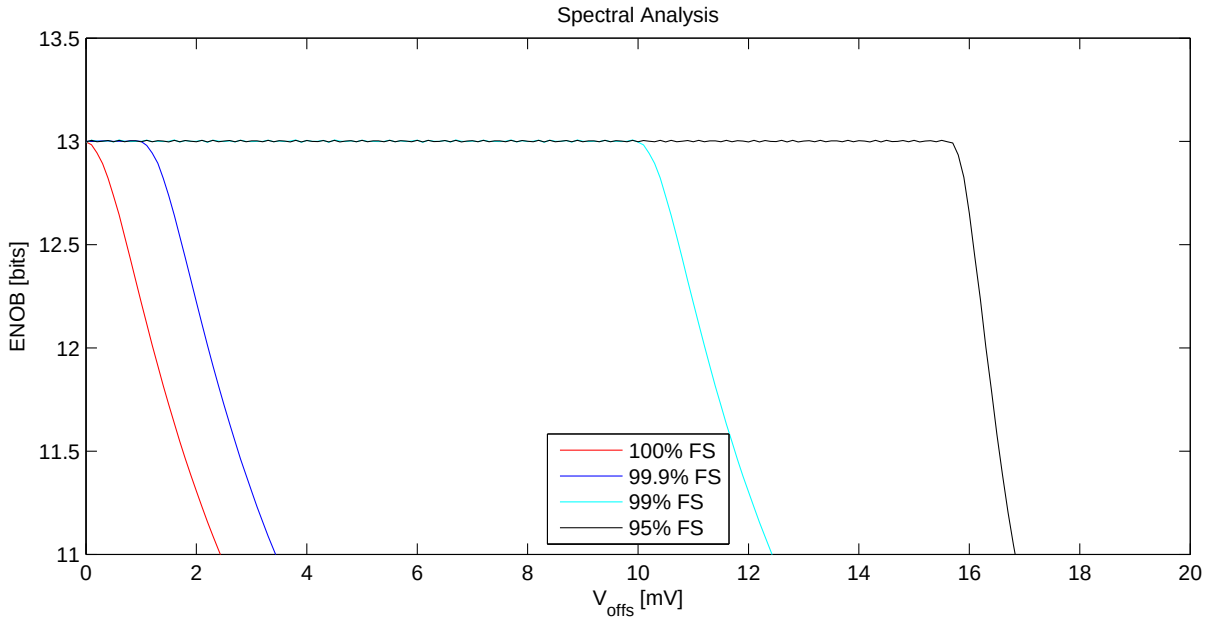

Figure 5.20: Offset voltage with high input amplitudes, 2.5 bit MDAC

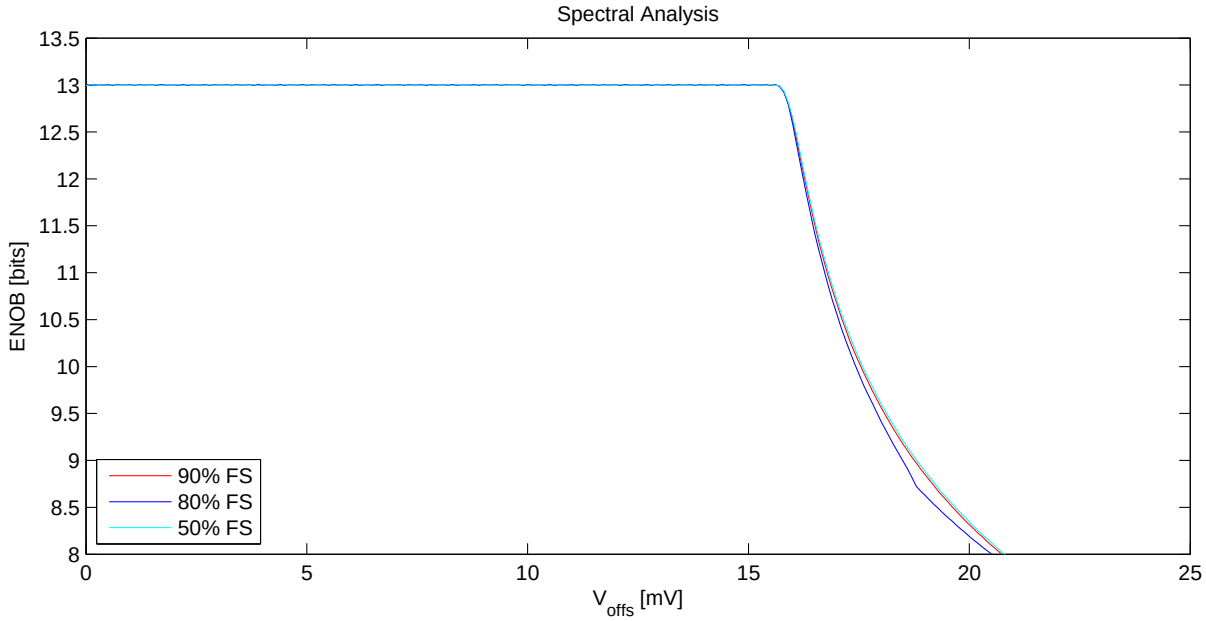

Figure 5.21: Offset voltage with lower input amplitudes, 2.5 bit MDAC

6 Conclusions

6.1 Conclusions

6.1.1 Overview and Important Results

This thesis investigated DPA for use in 40 nm technology both analytically and in Matlab simulations. It is summarized in the following:

Chapter 2 introduced the basics of analog to digital converters and of pipelined ADCs.

Chapter 3 derived transfer functions for a single 1.5 bit MDAC stage. The following error sources were considered separately with analytical approximations and Matlab simulations. The op-amps performing the analog residue generation in the MDAC were modeled with *Finite DC gain* and *Offset voltage*. *Capacitor mismatch* of the capacitors determining the precision of subtraction and multiplication operations in the MDAC was investigated. *Noise sources* during the sampling process, in the op-amp and on the reference voltage were considered. The analytic approximations of the error sources were verified in Matlab simulations.

It turned out that the capacitor mismatch of this 40 nm process limits the ADC resolution of the pipelined ADC using 1.5 bit MDAC stages. Therefore the 2.5 bit MDAC was considered, which has higher MDAC gain and thus relaxed requirements on the residue error. Chapter 4 extended the results of Chapter 3 to 2.5 bit MDAC stages. 1.5 bit and 2.5 bit MDACs were compared.

The cascading of multiple MDAC stages to an overall pipelined ADC was discussed in Chapter 5 on basis of Matlab simulation results. The digital output of the ADC was analyzed in the frequency domain.

For the simulations, the Matlab model of a 1.5 bit DPA MDAC with flip around architecture, which has been developed as part of a previous project, was extended to a 1.5 bit DPA MDAC with non-flip around architecture and to a 2.5 bit DPA MDAC. A Matlab model of the overall pipelined ADC was constructed based on the individual MDAC model stages, which were

cascaded, and the ADC performance was analyzed in the frequency domain. The SPA structures with 1.5 bits and 2.5 bits were compared to the DPA approach, and requirements for the mentioned error sources were determined.

The goal of the dual path amplification technique is to achieve a high resolution without digital calibration or complex op-amps, i.e., to save chip area and keep the power consumption low. The main findings of this thesis with respect to this goal can be summarized as follows.

1. *DC gain:* For a resolution of 12 bits, considering only finite DC gain, it is possible to achieve the needed equivalent DC gain with two simple op-amps of about 45 dB. The sum of the coarse DC gain and the fine DC gain is higher than the DC gain required for the SPA approach. The additional DC gain needed for the DPA approach is proportional to the feedback factor k_f of the fine op-amp.

2. *Noise performance:* The noise performance of an ADC using DPA MDAC stages is similar to the noise performance of an ADC built of SPA MDAC stages. The fine stage is the dominant noise source and has to fulfill similar noise requirements to an SPA MDAC. However, it has less requirements on DC gain than an SPA MDAC, and only a small output swing.

3. *Capacitor mismatch:* The error caused by capacitor mismatch is not proportional to the output of the MDAC. Similar to the noise error, the fine stage determines the precision of the residue. The DPA MDAC has similar performance to the DPA MDAC. The capacitor mismatch of the coarse stage can be relaxed.

4. *Chip area:* Additional capacitors and switches are needed, which increases the chip size compared to SPA MDACs. Furthermore, a second op-amp is required for the fine stage of the MDAC.

5. *Digital calibration:* No digital calibration is needed for resolutions covered by the capacitor mismatch of the technology used.

6. *Resolution limits:* In 40 nm technology, the resolution using DPA is limited to an absolute maximum of 10.7 bits for 1.5 bit MDACs and 11.2 bits for 2.5 bit MDACs. These limits only take capacitor mismatch into consideration but no scaling of the stages. These limits are reduced to lower resolutions by the effects of other error sources.

7. *2.5 bit stage:* The 2.5 bit MDAC shows better results than the 1.5 bit stage for all the error sources investigated, except for the offset error. The offset error of the 2.5 bit MDAC has a higher gain to the input of the MDAC due to the larger feedback factor k.

8. *Coarse stage:* The requirements for all the noise sources and the capacitor mismatch of the coarse stage can be relaxed. The errors are reduced by the fine stage. The DC gain of the coarse op-amp is added to the DC gain of the fine op-amp to achieve the required DC gain.

The scope of this thesis was to investigate the DPA architecture for use with 40 nm technology. The simplifying results of the analytical considerations and the more detailed simulation results give a good overview of the impact of errors on the residue generation and on the limitations of the overall pipeline ADC performance. By contrast, in SPICE simulations the contributions of all the investigated error sources are mixed together, which makes it difficult to extract the impact of one error source. On the other hand, the SPICE simulation allows more effects to be considered, such as charge injection because of non-ideal switches and more complex op-amps models, and is very close to the chip. The thesis, results build a good basis for circuit design

using SPICE simulations. Bottle necks were identified and so optimizations can be done more easily.

6.1.2 Outlook

The ADC built of 2.5 bit DPA MDAC stages shows promising results regarding the investigated effects. Nevertheless, some aspects could not be dealt with in this thesis because of time constraints, for example the settling behavior of the DPA structure and the requirements on the Gain-Bandwidth product (GBW). In addition the scaling of MDAC stages could not be discussed extensively and the impact of the offset voltage on the op-amps needs further simulations. These steps are planed for the near future. The topology could be further optimized by finding a smart way to apply the input signals using parallel or serial capacitors with the goal of reducing the errors due to capacitor mismatch. Simultaneous amplification and sampling of the coarse and fine stages is feasible. However, this would result in a structure that is more complex and more difficult to investigate, because the output of the coarse stage is not sampled and varies during the amplification phase of the fine stage.

Once Matlab simulations have been completed, the most promising approach will be implemented in a SPICE simulation in order to verify the Matlab model. This will allow further parasitic effects to be considered and allow the interaction between the different error sources to be identified. If the SPICE simulation yields good results, the next step would be to implement the architecture in silicon and verify the simulation results on a test chip.

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