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A PVT tolerant 16 MHz RC-Oscillator for Automotive Applications

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Abstract

In this thesis, I designed and implemented a RC-Oscillator which is optimized for a high frequency accuracy over PVT variations. The oscillator uses a voltage averaging feedback concept, which fully compensates the comparator delay. A test-chip with a typical frequency of 16 MHz was fabricated in a $0.14\mu m$ CMOS ABCD9-Power SOI process. The results of the test chips aren't available yet. However, the simulation results show that there is a $\pm 6\sigma$ frequency stability of $\pm 1.65\%$ over a temperature and supply voltage range of $-40°C$ to $150°C$ and $1.7V$ to $1.9V$ respectively.

Kurzfassung

In der folgenden Diplomarbeit entwickelte ich einen RC-Oszillator, welcher für eine hohe Frequenzstabilität über PVT-Variationen optimiert wurde. Das Grundkonzept des Oszillators nützt eine mittelwertbildende Rückkopplung, wodurch das Komparator Delay vollständig kompensiert wird. Nach der Entwicklung des 16 MHz Oszillators wurde dieser in einem Test Chip ($0.14\mu m$ CMOS ABCD9-Power SOI Prozess) verifiziert. Diese Daten sind jedoch noch ausständig. Die Simulationsergebnisse ergaben eine $\pm 6\sigma$ Frequenzstabilität von $\pm 1.65\%$ bei einer Temperatur und Versorgungspannungsvariation von $-40°C$ - $150°C$, und $1.7V$ - $1.9V$.

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I dedicate this thesis to my dear friend Jürgen Karner, who died far too young in an avalanche accident.

About NXP Semiconductors

NXP (which stands for Next eXPerience) Semiconductors is a Dutch semiconductor manufacturer with the headquarter in Eindhoven, the Netherlands. Originally NXP arose from the Philips internal semiconductor group, also known as "Philips Semiconductors". NXP was founded in 2006 as Philips sold its semiconductor group to private investors. In the meantime, NXP has become one of the world's leading semiconductor manufacturers with operations in more than 25 countries and sales of 4.36 billion dollars in 2012 [60] [61].

NXP Semiconductors has over 55 years of experience in different business areas such as High Performance Mixed Signal, Automotive, Identification, Infrastructure and Industrial and Computing [42].

This thesis is done in collaboration with NXP.

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List of Abbreviations

RC	Resistor-Capacitor
PVT	Process-Voltage-Temperature
CMOS	Complementary Metal Oxide Semiconductor
ABCD	Advanced Bipolar CMOS DMOS
SOI	Silicon On Insulator
NXP	Next eXPerience
OTA	Operational Transconductance Amplifier
USB	Universal Serial Bus
GPS	Global Positioning System
XO	Xtal (crystal) Oscillator
VCXO	Voltage Compensated Xtal (crystal) Oscillator
TCXO	Temperature Compensated Xtal (crystal) Oscillator
OCXO	Oven Controlled Xtal (crystal) Oscillator
MEMS	Micro Electro Mechanical Systems
LC	Inductor-Capacitor
PLL	Phase Locked Loop
CPU	Central Processing Unit
FOM	Figure Of Merit
NAND	Negated AND
RS-FF	Reset Set Flip Flop
HI	High

LO	Low
PMOS	P-type Metal Oxide Semiconductor
NMOS	N-type Metal Oxide Semiconductor
MOS	Metal Oxide Semiconductor
BTI	Bias Temperature Instability
NBTI	Negative Bias Temperature Instability
PBTI	Positive Bias Temperature Instability
CHE	Channel Hot-Electron
SGHE	Secondarily Generated Hot-Electron
SHE	Substrate Hot-Electron
PD	Power Down
BW	Band width
GBW	Gain Band Width
PM	Phase Margin
ICM	Input Common Mode
AC	Alternate Current
Gm	Transconductance
PSRR	Power Supply Rejection Ratio
CMRR	Common Mode Rejection Ratio
LSB	Least Significant Bit
CLK	Clock
TMG	Transmission Gate
TCR_1	Temperature Coefficient of Resistance, 1^{st} order
TCR_2	Temperature Coefficient of Resistance, 2^{nd} order
TCC_1	Temperature Coefficient of Capacitance, 1^{st} order
TCF_1	Temperature Coefficient of Frequency, 1^{st} order
TCF_2	Temperature Coefficient of Frequency, 2^{nd} order

Chapter 1

Introduction

"Strictly speaking, an oscillator (from the latin verb, "oscillo," to swing) produces sinusoids. A clock has rectangular or square wave output." The terms have come to be used interchangeably and this thesis bends to that convention [56]. In an age of increasing integration, external frequency references are also becoming more and more integrated on a chip. The main reasons for the integration of frequency references are costs, area and reliability. The following chapter provides an overview of silicon-based frequency references. It studies various state-of-the-art implementations of silicon based frequency references in detail. However, the main aim of this chapter is a comparison of the frequency references currently available in the literature. Finally, a comparison between these references will be provided [28].

First, a word about frequency stability. The stability of a frequency reference is a measure of the amount of change in the output frequency as a function of environmental parameters. These include temperature, supply voltage, process tolerances, noise, etc. But the main factors which influence output frequency are variations in process, voltage and temperature (PVT). The indication of stability can be done in ppm (part per million) or percent [21] [3] [22] [33] [24]. The frequency stability tells us about the deviation of the output frequency Δf from the nominal frequency f_0 caused by environmental parameters [28].

$$f_{error}\,(\%) = \frac{\Delta f}{f_0}10^2 \tag{1.1}$$

$$f_{error}\,(ppm) = \frac{\Delta f}{f_0}10^6 \tag{1.2}$$

It should be noted that f_{error} is only meaningful if information about the environmental parameters is given.

Environmental parameters are:

- The measurement set-up: Temperature range, supply voltage range, trim, number of samples reported, standard deviation...
- Simulation set-up: Temperature range, supply voltage range, trim, corner, Monte-Carlo, standard deviation...

Frequency references are present in almost any electronic device. Therefore, it is understandable that, depending on the application of the device, different levels of accuracy are required. For instance, in some microcontroller applications, stable references ranging from 0.01% (100ppm) to 1% (10000ppm) [10] are needed, while USB 2.0 needs a clock accuracy of around 500ppm [11]. In wireless communication channels, much higher accuracies are required for the operation. For example, in mobile handset application, frequency references should have an accuracy of up to 2.5ppm [12], while a GPS receiver or mobile base station system requires an accuracy of sub ppm [28] [22] [2].

Now some words about quartz oscillators, as they are one of the reasons for the integration of frequency references. Crystal oscillators have been the only means of production of stable frequencies in the last decades. Their advantages are simple and include their low temperature dependence and "relatively low" cost with a small form factor. Therefore, they also have a dominant share in the frequency control market (more than 90%, equivalent to more than 4.5 billion U.S. dollars). To get a brief overview of some of the quartz oscillator technologies available on the market, some of them are listed below with the corresponding accuracy [28] [22].

- Non compensated (XO) and voltage compensated (VCXO) quartz oscillators achieve stability in the range of 20ppm to 100ppm.
- Temperature compensated (TCXO) quartz oscillators achieve stability in the range of 0.1ppm to 5ppm.
- Oven controlled (OCXO) quartz oscillators achieve stability in the range of 1ppb (parts per billion).

On the other hand, quartz oscillators also have some drawbacks. One of these drawbacks is the amount of space required on the circuit board when a particular number of frequency sources are required by the system. Another drawback is their sensitivity to mechanical shock and vibration. As a consequence, any mechanical stress, acceleration or vibration leads to frequency changes [22]. This series of drawbacks is what drives the search for integrated frequency references with similar frequency stability. Such references are made of silicon, which is why they are also referred to as silicon-based frequency references [35].

1.1 Motivation and target specification

In the modern world of communication RC-oscillators gain more and more on influence. Due to the developing of modern CMOS processes, passive elements such as resistors and capacitors can be produced with a low spread. This allows a further reliable process integration of external components. The necessary frequency stability, such as within 1% can be thoroughly achieved with some constraints (temperature range, voltage range, multi point trim) and more or less sophisticated concepts. This results in a considerable variety of application for RC-oscillators. The biggest challenge of these concepts consists mostly of achieving very good frequency stability at low power and a small area. As mentioned above, the future request for RC-oscillators is to achieve a similar frequency stability of quartz oscillators. This desire is triggered from many advantages of the integrated RC-oscillators.

These advantages are:

- Very good to integrate
- Very fast start-up times
- Suitable for low power applications
- Small area
- Trimable
- Require no external components
- Less costs compared to crystal oscillator
- Less susceptible to mechanical shock and vibrations

In large systems more than one system clocks are usually necessary to provide clocks for different sub systems. Depending on the operating mode of the system different clocks are also necessary. For instance, in sleep mode a low power oscillator will be used, but during the transmitting of signals, an RC- or crystal oscillator has to be used. It is also conceivable that an RC-oscillator is only used for the start-up phase until the crystal oscillator frequency is settled. A fast RC-oscillator for wake-up, could load the application code from the flash before the crystal oscillator is prepared. For these requirements, it is clear that this is not feasible with external crystal oscillators due to a long start-up time, space and cost reasons. However, disadvantages result due to the process variations of integrated passive components. To be able to use these oscillator technologies useful as a time source, usually a frequency trim has to be performed. Due to the above mentioned application aspects NXP decided to design an oscillator with a low PVT variation.

1.1.1 Target specification of the oscillator

Table 1.1: Oscillator target specification

Specification	Data
Principle of operation	Best should be chosen
Frequency range in MHz	16
Supply voltage in Volt	1.7 to 1.9
Temperature range in °C	-40 to 150, up to 175 functional behavior
Supply current in μA	< 200
Process	0.14μm SOI ABCD9-Power
Accuracy in %	± 0.5 over $\pm 6\sigma$, PVT and trimmed
Area in mm^2	< 0.1
Power-down mode	yes
Duty-cycle in %	45 to 55
Settling time in μs	< 250
Settling behavior	spike free
Trim	yes
Trim behavior	The frequency change due to the trim signal has to be spike free
Clock output	Enable/disable possibility with a spike free behavior
Start-up behavior	From a low frequency with no frequency overshoot higher than $16MHz + 5\%$

Chapter 2

Oscillator topologies

In the following sections, several silicon-based frequency references are examined for their advantages and disadvantages.

2.1 MEMS-oscillators

Quartz resonators are excited by an electrical oscillating circuit. The oscillation is due to the piezoelectric properties of the quartz. But these piezoelectric properties cannot be integrated on silicon. Therefore, a lot of effort was spent on the research and development of silicon MEMS (Micro Electro Mechanical Systems) oscillators, which, like LC-oscillators, also have self-oscillation properties. In contrast, RC-oscillators have no self-oscillation properties. Thus, they always need additional components such as comparators or Schmitt-triggers to maintain their oscillation. The main aim of the extensive research surrounding the MEMS-oscillators was the replacement of expensive external crystals [31]. MEMS-resonators are structures with sizes in the micrometer to nanometer range which can be excited electrostatically, electromagnetically or piezoelectrically [51] [55]. Their frequency ranges from a few kHz up to one/several MHz with quality factors of 50000 up to 300000 which are comparable to quartz oscillators. The quality factor of the resonator determines the stability of the frequency reference and is equal to the ratio between the resonance frequency and the bandwidth of the LC-circuit. For MEMS-resonators, the shape and geometry

determines this factor. This frequency stability is comparable with that of quartz oscillators. However, the jitter (phase noise) performance for mobile applications is still too low in MEMS technologies. For a better jitter performance with low noise and a high quality factor, LC-oscillators are a good alternative to MEMS-oscillators [51] [45]. Due to the special manufacturing process, it is not possible to manufacture MEMS structures and electronic circuits on the same die. That is also one of the biggest drawbacks of this technology [55] [30]. Furthermore, a big challenge in this technology is ensuring long term frequency stability with a protection against vibration, shock sensitivity and temperature drift [30]. However due to their very small dimensions and very low weight, MEMS-resonators have a better shock resistance than quartz crystals [20]. Compared to quartz oscillators, MEMS-oscillators are more area efficient and, due to mass production, more cost effective. Commercially available MEMS frequency references manufactured by Discera use the technique of combining a MEMS-resonator with a PLL [12]. The lower limit for the frequency stability is about 50ppm, at supply voltages from 1.8V to 3.3V. The output frequencies lie between 1-150MHz and the supply current is about 3mA.

2.2 LC-oscillators

As previously mentioned, LC-oscillators can be manufactured on silicon. These oscillators have various advantages and disadvantages compared to quartz or MEMS-oscillators. Depending on the requirements, LC-oscillators can be preferred over quartz oscillators. They are mostly used in phase locked loops (PLLs) as voltage controlled oscillators. Due to their better phase noise properties, LC-oscillators are also used in RF applications. They have two energy storing elements, L and C, which therefore allow a free oscillation to be generated. As in other oscillator topologies, their frequency stability across a range of temperatures, voltages and process variations has to be considered. The output frequency is usually a function of temperature with a negative concave temperature coefficient whose sensitivity increases at high temperatures, see equation 2.2 [34]. With a positive linear dependency of the re-

sistance r_L of the inductance on temperature, the LC-oscillator exhibits a negative temperature coefficient with a large quadratic frequency variation across temperatures [47]. The resistive losses of the coil limits the possible temperature range from $20°C$ to $70°C$. Another disadvantage is the sensitivity of the output frequency due to conductive materials and eddy currents in the vicinity of the oscillator. Considering the many process and temperature dependent variables, one single point temperature trim is not practical for a definite temperature response as too many unknown variables can still influence the temperature response. For a well defined temperature response, a trim of the temperature coefficients of the frequency is necessary, but this causes an increase in production costs. The frequency ω of an LC-oscillator is defined as per equation 2.1.

$$\omega = \omega_0 \sqrt{\frac{1-\frac{{r_L}^2 C}{L}}{1-\frac{{r_C}^2 C}{L}}} = \frac{1}{\sqrt{LC}} \sqrt{\frac{1-\frac{{r_L}^2 C}{L}}{1-\frac{{r_C}^2 C}{L}}} \tag{2.1}$$

$$f_{TC} = \frac{\partial \omega}{\partial T}\frac{1}{\omega} \approx -\frac{C{r_L}^2}{L}\frac{\omega_0^2}{\omega^2}\frac{\partial r_L}{\partial T} \tag{2.2}$$

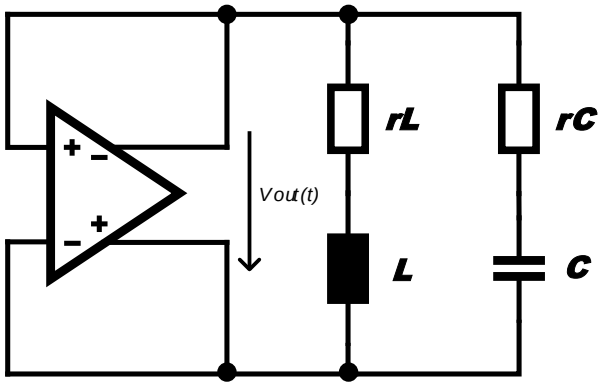

Figure 2-1: Conventional LC-oscillator with output voltage $v_{out}(t)$

2.3 RC-harmonic oscillator

This type of oscillator uses resistors and capacitors to generate an oscillating signal. As known from integrated circuits, these passive elements have a large variation around their nominal value. This variation is in the order of 10 to 20 percent. Due to this large dependency on the absolute values and on temperature, an accurate prediction of the frequency without trimming is not possible. However, RC-oscillators have some advantages which make them very interesting for industrial applications. They can be used as a low-power, sleep or CPU oscillator. In these applications, a high accuracy is usually not necessary. Secondly, they require only a fraction of the power (micro-watts) and area compared to LC, MEMS or quartz oscillators. A state-of-the-art RC-oscillator can reach a frequency stability of up to 1% by trimming and temperature compensation. However, this depends on some details such as supply voltage range or temperature range. Harmonic RC-oscillators operate in a frequency range from one kHz to a few MHz. The output signal of an RC-oscillator depends on the topology of the oscillator. We can distinguish between clock RC-oscillators and harmonic RC-oscillators. Harmonic oscillators have a sinusoidal output voltage whereas clock oscillators have a rectangular one. A commonly known type of harmonic RC-oscillator is the Wien-Bridge-oscillator [15]. This oscillator combines an RC-network with an amplifier. The RC-network basically combines a high pass filter with a low pass filter, producing a very selective second-order frequency dependent band pass filter. At the resonant frequency, the reactance of the circuits equals its resistance R as the phase shift between the input and output equals zero degrees. The magnitude of the output voltage is at its maximum and is therefore equal to one third $\frac{1}{3}$ of the input voltage. So if there is an amplification by 3, then the circuit oscillates [15]. In the first order, the frequency stability of the oscillator is determined by the process and temperature stability of the passive elements R and C. Other non-ideal effects which can lead to additional inaccuracies in the output frequency include the finite gain, output impedance and the phase shift introduced by the amplifier. To mitigate these effects, a fully differential and modified Wien-Bridge-oscillator is

proposed in [58] [44].

2.4 Relaxation-oscillators

Another type of RC-oscillator is a relaxation-oscillator. The oscillator is called relaxation-oscillator due to the relaxation time $\tau = RC$ of the RC-network. This topology produces a digital (square wave) output signal also called clock [25]. Its output frequency lies between a few hundreds kHz to tens of MHz. Relaxation-oscillators are often used primarily because of their low power consumption and CMOS compatibility. These properties make them attractive for battery-powered applications such as wake-up timers or implantable biomedical systems [43] [26] [7]. Like in harmonic RC-oscillators, the time-giving element is a RC-network. This results again in the main disadvantages discussed above [43] [7]. By means of temperature compensation and trimming, a frequency stability of 2% [7] [26] [7] can realistically be obtained. The conventional relaxation-oscillator has the disadvantage that its comparator delay influences the frequency. For an exact description of the operation of conventional relaxation-oscillators please refer to the literature in [50]. However, this delay is subject to strong variations due to PVT. This leads to an additional error due the variation of the comparator delay. Various approaches are suggested in the literature in order to minimize this error. One obvious possible approach is to minimize the variation of the comparator delay is to increase the power of the comparator. This is usually not possible because this cannot be reconciled with the requirement of a low-power oscillator. As part of the literature research, some relaxation-oscillators were investigated. However, not all of them are represented in the table 2.1 at the end of the chapter. The relaxation-oscillator in paper [63] was chosen for the implementation due to its close match of the requirements laid down by NXP. This oscillator will be discussed in detail in the following chapters. However some details are noted here. The oscillator has a novel voltage averaging feedback which has the big advantage that oscillation depends only on the RC-product. So its frequency is independent of the comparator delay. Therefore, it is possible to provide the comparator with lower

power because the delay variation can be compensated. This meets the requirements for low power and frequency stability precisely.

2.5 Ring-oscillators

Another class of clock oscillators are ring-oscillators. They are often used as voltage-controlled oscillators in jitter sensitive applications. Examples of such applications include PLLs or clock recovery circuits. An advantage of ring-oscillators is the high achievable frequency and the easy CMOS integration. There are a variety of topologies (also cross-coupled oscillators) which are explained in detail in [32]. The simplest topology of a ring-oscillator consists of a cascade of inverters with an odd number. However, ring-oscillators can be accomplished with analog differential delay stages too. This topology has the advantage that the frequency can be controlled with the output swing of the differential pair. Thus, for instance, the frequency variation can be partially compensated. More details on this implementation can be found in [6] and [29]. An analytic and exact calculation of the frequency for representatives of ring-oscillators is not straight forward . There are two analyses which are relevant to the calculation of the frequency. Firstly, a small signal analysis for the start-up behavior, and secondly, a large signal analysis for the settled case. In summary, the loop gain of a negative feedback circuit has to satisfy two conditions:

$$|H(j\omega_0)| \geq 1 \text{ and } \angle H(j\omega_0) = 180^\circ, \tag{2.3}$$

then the circuit may oscillate at ω_0. These two conditions are called the Barkhausen Criteria. For a detailed description of the calculation of the frequency see [49].

As noted above two considerations (small and large signal analysis) are necessary. However, the results of the two considerations do not necessarily match. The reason of the frequency mismatch is conceivable. For ring-oscillators, the amplitude grows very rapidly, leading to a saturation phenomenon which results in the limitation of the maximum amplitude. This leads to non-linearities which can be treated only

by a large-signal analysis. A large signal analysis for the propagation delay does not necessarily match the small-signal analysis, since in this case the output resistance and capacitance in the trip point are used whereas the propagation delay is calculated by non-linear currents and capacitances. It should be noted that, if the small signal loop gain is greater than one, then the circuit must spend also enough time in saturation (higher gain than in the triode region) so that the average loop gain is still equal to one. The trip point of an inverter is the point where $v_{in} = v_{out}$ [49].

2.6 Conclusion and design choice

As mentioned in chapter 1, frequency stability can only be compared between publications if the data on the measurement or simulation set-up are known. For instance, 200 measurements of a published oscillator cannot be compared with two measurements of another published oscillator. The same applies to the simulation results. Although if a Monte-Carlo analysis was performed, it is still mostly unknown which parameters were varied by the Monte-Carlo analysis. In RC-oscillators for example, the temperature coefficient of a resistor (TCR) has to be changed since it is dependent on the doping concentration [46] [57]. A statement about the frequency spread is simply not meaningful if there is no variation on the temperature coefficient of a resistor. A comparison between the topologies can therefore only be made based on a rough estimation. The most interesting requirements for integrated oscillators are area, power consumption, frequency stability, jitter and the temperature range. Due to the two die solution, MEMS-oscillators need the largest surface of all integrated oscillators. In other words, a MEMS-oscillator is not CMOS compatible because it cannot be manufactured with a conventional CMOS circuit on a chip. This big disadvantage leads to higher packaging and production costs, as well as an increase in complexity. Its power consumption is similar to the LC-oscillator, and thus larger than in other topologies. However, MEMS and LC-oscillators are the only solutions to achieve better than 0.1% accuracy at a reasonable jitter level. For integrated circuits, the LC-oscillator provides the best performance across process and temperature

variations. However, LC-oscillators need more area and power than all other oscillators. A further disadvantage of LC-oscillators is their limited temperature range. For less precise frequency stability requirements, RC, Ring, mobility or relaxation-oscillators may offer interesting advantages. These oscillators can reach a frequency stability of up to 1%, depending on the topology. The great advantages of these oscillators are the small required area and the low power consumption ($\mu Watt$ range). This makes them very interesting for low power applications. A very short summary of these studies can be found in the table 2.1 at the end of the chapter. Because of area and cost requirements, LC and MEMS-oscillator cannot be chosen for the design. RC-oscillators match the requirements of NXP very well. As seen in table 2.1 the relaxation-oscillator [63] has a good figure of merit as well as a conclusive design. Therefore this oscillator was chosen for the further design. This oscillator will be discussed in the following chapters in detail. For further information on the specification see chapter 1.1 "Motivation and target specification".

Figure of merit

A figure of merit (FOM) [48] can be defined as follows:

$$FOM = \frac{\Delta\omega}{\omega_{T_0}\Delta T}\frac{ppm}{^\circ C} \tag{2.4}$$

Where $\Delta\omega$ is the frequency deviation across the temperature range ΔT, and ω_{T_0} is the nominal frequency at T_0. This FOM addresses the frequency temperature coefficient.

Table 2.1: State-of-the-art oscillator overview [50]

Reference number	[63]	[29]	[37]	[52]
Principle of operation	Relaxation with feedback	Ring	LC	RC-harmonic
Frequency range in MHz	14	10	24	6
Supply voltage in Volt	1.7 to 1.9	1.2 to 3	1.8	1.2
Temperature range in °C	-40 to 125	-20 to 100	0 to 70	0 to 120
Supply current or power consumption	25μA	80μA	4mW	66μA
Process in μm	0.18	0.18	0.13	0.065
Accuracy in ppm	$\pm$3500	$\pm$4500	$\pm$300	$\pm$9000
Voltage coefficient in ppm/V	8000	2500	not available	not available
Temperature coefficient in ppm/°C	$\pm$11.51	$\pm$33.33	$\pm$8.6	$\pm$86
Area in mm^2	0.04	0.22	0.8	0.03
Number of samples reported	1	not available	commercial	6
Figure of merit (FOM)	21.2	32.5	4.3	75

Chapter 3

Theoretical design considerations

3.1 Start-up and oscillation mechanism

The start-up behavior should be well defined and known. According to the specification (see chapter 1.1) of the start-up, the frequency has to settle within 250μs from a low frequency to the higher target frequency. An overshoot of the frequency should be avoided as subsequent blocks could cause a system failure due to higher frequencies. Second, the default trim value for the very first start-up has to be chosen so that the frequency is always less than 16MHz + 5%. This specification can only be achieved through a well-defined starting procedure of the individual blocks and a large enough phase margin of the active filter.

The main building blocks which have an influence on the start-up process are:

- The resistive voltage divider (reference voltage settling behavior)
- The current bias cell (current settling behavior)
- The delay elements (inverters chain) between the NANDs
- The active filter (sets the comparator threshold)

The resistor voltage divider and the current bias cell are very important, because the OTA and the comparator need a constant and well defined bias current for op-

eration. Only then, the OTA and comparator can work properly. Furthermore, the resistive voltage divider has a buffer capacitor and parasitic capacitances depending on the size of the resistors. That changes the start-up behavior in such a way, that the voltage at the reference node is not immediately present due to an RC-charging behavior. Therefore, we must now distinguish between two start signals, the externally applied $enable_{osc}$ and the delayed internally generated $start_{osc}$. The external $enable_{osc}$ first enables the resistive voltage divider and the current bias-cell. After the correct bias current and reference voltage have settled, the bias cell block creates a $start_{osc}$ signal which starts the oscillator immediately. If the reference voltage and the bias current are not settled at a positive $start_{osc}$ signal, than the integrator would integrate to a smaller average voltage which could lead to a significant higher frequency during the starting phase. For further information on the current bias block see chapter 4.4. A further problem during the start-up can be a simultaneous set of the $start_{osc}$ signal of the NANDs at the RS-FF. This can be prevented with a short propagation delay between the two NANDs. As with conventional relaxation oscillators, the level of the comparator threshold also has a big influence on the starting frequency. To avoid a high frequency in the start phase, the comparator threshold has to be set to a high voltage. In our case, this can be easily done by forcing the integrator capacitor to the supply voltage V_{dda}. For a detailed description of the transient profile of this voltage see chapter 3.1.1 and figure 3-1.

The following requirements are also necessary for a proper start-up:

- $t_{VrefSettling} < t_{iSettling}$
- $t_{pdhlNAND} < 4 \cdot t_{pdInv}$
- $V_{CompThresh_{t=0}} = V_{dda}$

The first two statements above have to be checked in all supply and temperature corners with a Monte-Carlo analysis, in order to determine a proper safety margin.

- $t_{pdhlNAND} < 4 \cdot t_{pdInv}$:

  This requirement is necessary to ensure that only the left RC-cell is charged during the start-up. The worst case value for the difference delay $4 \cdot t_{pdInv} -$

$t_{pdhlNAND}$ is as aspect at $V_{dda} = 1.9V$ and $-40°C$. There is a safety margin of $(\mu - 6 \cdot \sigma) = 545ps - 19ps \cdot 6 = 431ps$, which is sufficient.

- $t_{VrefSettling} < t_{iSettling}$:

  This requirement is necessary to ensure a safe start-up from a low frequency. $t_{iSettling}$ is the time between a HI from $enable_{osc}$ until $start_{osc}$ becomes HI.

  $t_{iSettlingMIN} = (\mu - 6 \cdot \sigma) = 15.67\mu s - 0.56\mu s \cdot 6 = 12.3\mu s$. The current of the bias cell is settled up to 0.4% of its end value after this time.

  $t_{VrefSettlingMAX} = (\mu + 6 \cdot \sigma) = 9.16\mu s + 0.46\mu s \cdot 6 = 11.9\mu s$.

  $t_{VrefSettlingMAX}$ is the maximum time for a 0.05% settling of the reference voltage. Therefore, the requirement $t_{VrefSettling} < t_{iSettling}$ is also satisfied. Note: These are very stable assumptions, because the $t_{VrefSettling}$ has its worst case at 1.7V and $-40°C$ and $t_{iSettling}$ at 1.9V and $-40°C$

3.1.1 Start-up sequence

1. Let us assume that a start signal $enable_{osc}$ is applied to the oscillator

2. The resistive voltage divider and the current bias cell will be enabled immediately

3. After the bias current is settled the $start_{osc}$ signal goes to HI

   - If $t_{pdhlNAND} < 4 \cdot t_{pdhlInverter}$ then the right NAND will remain in the same state as before until the comparator switches to LO

4. The left NAND will switch to LO and the load capacitor of the left RC-cell will be charged

   - $V_{CompThresh}$ is at this time forced to the supply voltage (V_{dda}). If a voltage is applied to the active filter, the $V_{CompThrehs}$ voltage rises short-term above V_{dda}, due to a bootstrap effect! However, due to the parasitic diode of the PMOS, in the output stage, the voltage is limited to $V_{dda} + v_{diode}$.

     Stress check of the comparator input differential pair:

$Vdda + v_{diode} < V_{gs,Nmos,MAX} + V_{bs,Nmos}$. Where $V_{gs,Nmos,MAX} = 2.5$V. So for a correctly biased comparator, there is no danger for the input differential pair due to the short-term stress.

- Due to the rising voltage V_{RCleft} at load capacitor of the left RC-cell, the negative input V_{inn} at the active filter also rises.
- If V_{inn} rises above $V_{inp} = V_{ref}$, then the OTA discharges its integrator capacitor C_{int} and $V_{CompThresh}$ decreases.

5. $V_{CompThresh}$ decreases due to the discharging of the OTA
6. If $V_{CompThresh} < V_{RCleft}$ then the comparator switches to LO
7. The left NAND will therefore switch to HI and the right NAND to LO
8. Therefore, the right RC-cell begins to load the capacitor whereas the left RC-cell will be discharged
9. When $V_{RCright} > V_{CompThresh}$ the compactor switches to LO again and the oscillation mechanism begins at step 7 with the other NAND
    - So the waveforms $V_{RCright}, V_{RCleft}$ are transmitted alternately to the active filter
    - The oscillator settles in to its target frequency if the average voltage of $V_{RCright} + V_{RCleft} = V_{osc}$ is equal to V_{ref}.

Nevertheless, there are more requirements for a proper operation of the oscillator.

- The inverter to the transmission gate has to have a shorter propagation delay than the NAND. Otherwise both sides are shortened $t_{pdhlNAND} > t_{pdhlInvTMG}$.
- When neglecting parasitic effects, the comparator delay has to be greater than twice the propagation delay of the NANDs. This condition is easy to achieve at a frequency of 16MHz.

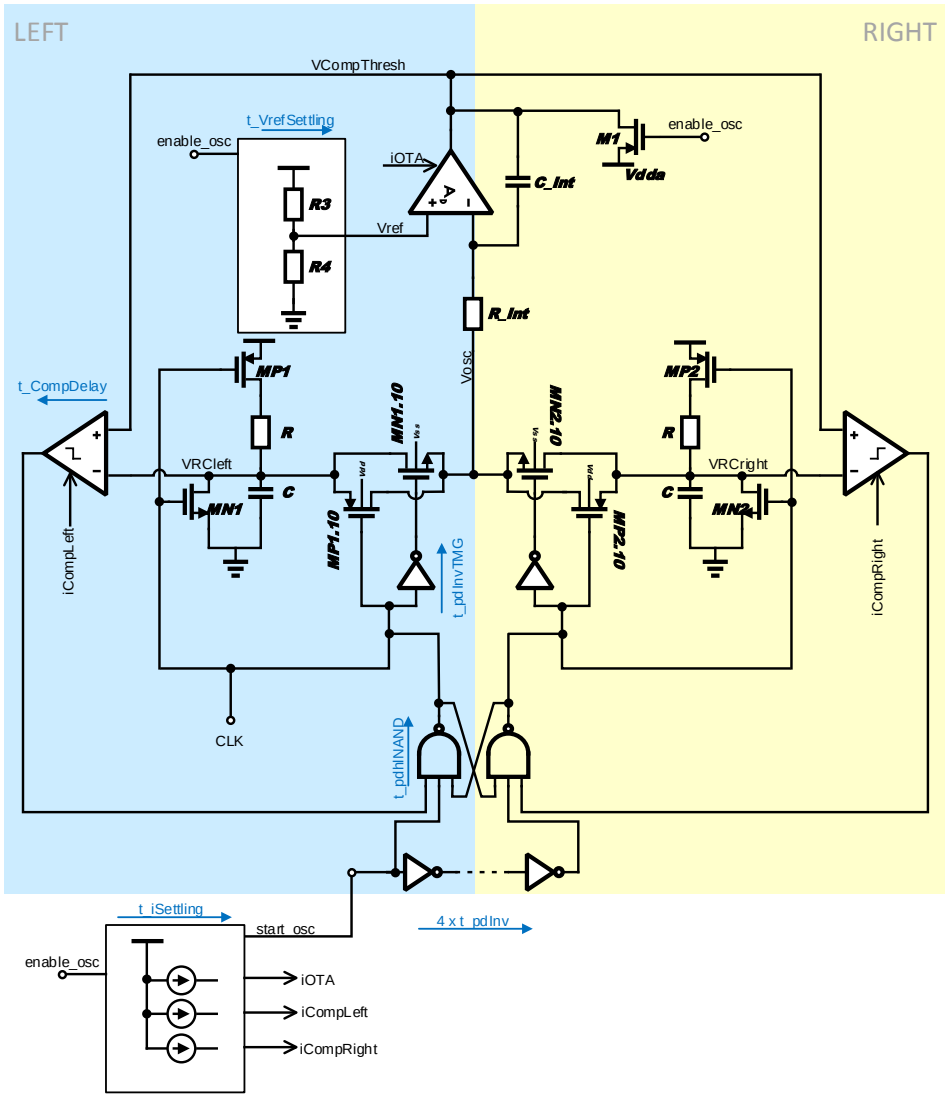

Figure 3-1: RC-oscillator with voltage averaging feedback

3.2 Power-down mode

A power-down mode is a necessary criterion to decrease the power consumption during unneeded phases. Due to aging effects of MOS transistors in power-down mode, a biasing of source, drain, gate and bulk at different voltage levels has to be avoided. Some precautions have to be taken to avoid an adverse shift in parameters due to this asymmetric bias. This shift in parameters can lead, for instance, to a higher offset or an higher offset drift, and therefore to a bad long-term performance. The long-term frequency stability is mainly influenced by aging of the circuit, whereas short-term frequency stability (jitter, phase noise) is influenced by thermal or $\frac{1}{f}$ noise.

MOS transistor aging effects include:

- Negative bias temperature instability (NBTI) of a PMOS
- Positive bias temperature instability (PBTI) of a NMOS
- Hot carrier injection

3.2.1 Bias temperature instability

Bias temperature instability (BTI) is a degradation effect in MOS transistors which causes parameter shifts when a high gate bias with respect to well, source, or drain is applied at relatively high temperatures. Depending on the sign of the gate bias with respect to well, source, or drain, the BTI is usually referred to as a negative BTI (NBTI) or a positive BTI (PBTI). PBTI of an NMOS is far less common than NBTI of a PMOS because PMOSs almost always operate with a negative gate to source voltage (NBTI) [40] [53]. See figure 3.2.1.

The typical setup for a NBTI stress of a PMOS is as follows:

- High temperature, $100°C$ to $200°C$
- The gate is negatively biased, whereas source and drain and substrate are grounded. Therefore the transistor is conductive, $V_{DS} \approx 0V$

The electrical field over the gate oxide in this setup causes damage to the gate oxide and at the oxide-silicon interface. The parameter most affected is the threshold

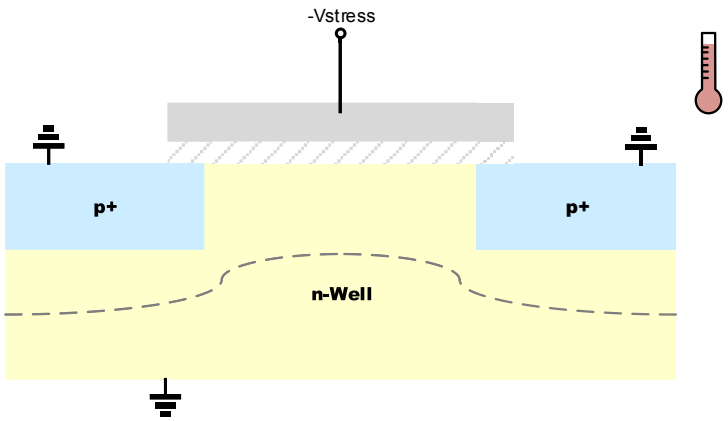

Figure 3-2: NBTI stress of a PMOS

Fig. 3.2.1 shows the set-up for a NBTI stress. The source, drain, and substrate are grounded whereas the gate is negatively biased. These conditions are applied at higher temperatures and for a certain period of time. Due to the symmetry of source and drain no channel hot carriers are generated [53].

voltage V_T (increase in V_T, resulting in a slower transistor). As mentioned above, modes which are susceptible to BTI are the power-down mode or a mode with an asymmetrical bias of the transistors.

Susceptible circuit parts include:

- The matched differential pair
- Voltage dividers with transistors
- Voltage comparators

To prevent lifetime reduction due to BTI, it is important to avoid asymmetrical stress of the MOS transistors in matched pair configurations. Therefore, it is better, if possible, to always use NMOS matched configurations. In power-down mode, PMOS transistors should always remain switched off [40]. This generally requires a gate

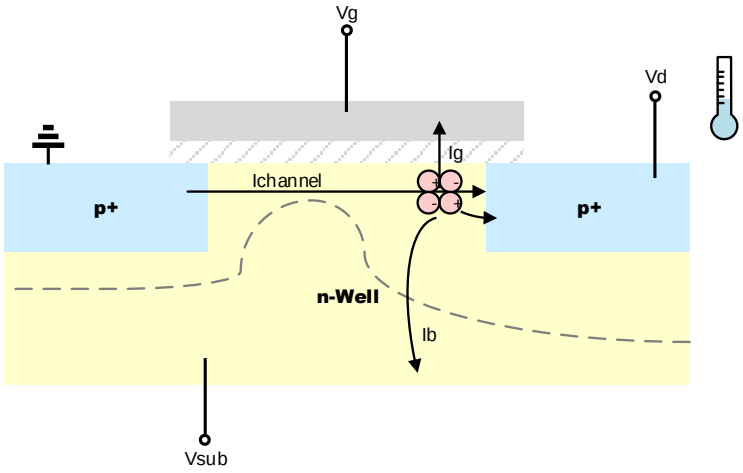

Figure 3-3: Drain avalanche hot carrier injection (DAHC) in a PMOS

Fig. 3-3 shows the set-up for a DAHC stress. Stress conditions: $V_{gs} < V_{ds}$. Hot carriers lead to generating electron-hole pairs. Hot electrons and hot holes are injected into the dielectric. Furthermore some of the carriers form a bulk current [16].

bias respective to the well so that the transistor is actively closed.

3.2.2 Hot carrier injection

Hot carrier injection is a reliability issue due to "hot carriers" that attain a very high kinetic energy from being accelerated by a high electric field. These energetic carriers can be injected into normally forbidden regions of the device, such as the gate dielectric, where they can get trapped or cause interface states to be generated. These defects in the dielectric lead to shifts in the threshold voltage V_T and transconductance degradation in MOS devices. To prevent lifetime reduction due to hot carrier injection, some design modifications can be made. These include, for example, a larger channel length, a doubled diffusion of source and drain or a graded drain junction. Four injection mechanisms can be distinguished when it comes to hot carrier injection into the dielectric [16].

- Channel hot-electron (CHE) injection $V_{gs} \approx V_{ds}$
- Drain avalanche hot-carrier (DAHC) injection $V_{gs} < V_{ds}$
- Secondarily generated hot-electron (SGHE) injection
- Substrate hot-electron (SHE) injection

For further information about the different conditions see [16]. In general, due to a higher V_{DS}, hot carriers can be injected into the dielectric, therefore, a higher R_{on} (low V_{GS}) leads to an high electric field $\Longrightarrow$ high V_{DS}. For instance: The stress conditions with high V_{DS} and lower V_{GS} are called the drain avalanche hot-carrier (DAHC) injection see figure 3-3.

3.2.3 Design considerations

The power-down mode (PD-mode) is a possible start scenario for the oscillator. For start-up, some voltage nodes have to be forced to a certain voltage in order to ensure that there is no overshoot of the frequency during start-up. Thus, the PBTI specifications of the comparator differential pair cannot be met because the comparator threshold has to be forced to V_{dda}. In order to meet the condition again, a transmission gate has to separate V_{inp} from V_{dda}. This problem does not occur for the OTA differential pair in the power-down mode because the reference voltage divider is switched off and thus V_{inn} can be easily connected to ground. V_{inp} of the OTA is also connected to ground so the PBTI condition is satisfied. Secondly, the integrator capacitor can be forced to V_{dda} without a problem so that a start with a low frequency is ensured. To minimize power consumption in power-down mode, low leakage transistors have sometimes been used in logic gates.

3.3 Frequency error due to a supply ripple

As observed in simulations, it makes a significant difference to the frequency when the supply voltage source is no longer assumed to be ideal. A ripple in the supply voltage can be caused by a high current load due to switching components and the finite internal resistance of the voltage regulator.

Solutions include:

- Optimizing of the current in switching components
- Buffer capacitors at peak current components
- Separate supply domains for analog and digital supply voltages
- A low-impedance voltage regulator
- A low-impedance layout

The frequency error caused by a ripple in the supply voltage arises because of the functional concept of an oscillator. The circuit concept tries to keep the average charge constant. So seen from a system point of view the RC-product behaves like a time depending RC-product.

This can be seen in the following derivation:

$$V_{ref} = \frac{1}{\tilde{T}} \int_0^{\tilde{T}} V_{osc}\, dt \tag{3.1}$$

$$V_{osc} = v_c \;\; for \ldots t = \{0 \rightarrow \tilde{T}\} \tag{3.2}$$

$$\text{where, } \tilde{T} = T/2 \tag{3.3}$$

$$v_c = \int_0^t \frac{i_c(\tilde{t})}{C}\, d\tilde{t} = \frac{1}{C} \cdot Q\,(t) \tag{3.4}$$

$$V_{ref} = \frac{1}{\tilde{T}} \int_0^{\tilde{T}} v_c\, dt = \frac{1}{\tilde{T}} \int_0^{\tilde{T}} \int_0^t \frac{i_c(\tilde{t})}{C}\, d\tilde{t}\, dt = \underbrace{\frac{1}{C} \frac{1}{\tilde{T}} \int_0^{\tilde{T}} Q\,(t)\; dt}_{average\ charge} \tag{3.5}$$

3.4 Study of frequency spread determining factors

The frequency is based on an RC-product, so its very important which resistors and capacitors are chosen in order to achieve an accurate frequency across temperature or voltage variations. Thus, a study of the process and its devices is necessary to

determine the depending voltage and temperature coefficients of the devices. As mentioned before, the period time is proportional to the RC-product. This means, that any spread of the temperature coefficient of the RC-product leads to a spread of the temperature behavior of the frequency.

The main factors leading to instability in the frequency across temperatures include:

- The offset voltage drift of the OTA
- Spread in the reference voltage temperature coefficient
- The differential offset voltage drift in comparators
- The spread in the temperature coefficient of the RC-product

Beside these points, the strong spread of the temperature coefficients of the poly-resistor is the limiting factor for the mass production of precisely integrated RC-oscillators. Because of this, it is absolutely necessary to implement a spread of temperature coefficients in simulation models. Otherwise, we cannot draw a useful conclusion about a behavior with real process variations. A compensation for this spread is only possible through a trimming process across two or more temperatures. Because of the fact that this comes with long testing times and therefore with high testing costs, such trimming processes are not useful.

3.4.1 Charge resistor R

Because of the problems laid out above, we can only choose an N^+ poly-resistor as a charging resistor. This resistor has the following advantages and disadvantages over other resistors:

- High temperature range: $-40°C$ to $150°C$

  Thus poly-resistor can be used for automotive applications without any restrictions
- Very low leakage currents
- Temperature coefficients are very low for poly-resistors
- Self-heating N^+ poly: Beware, the poly-resistor has self-heating (since it is on STI-oxide) $\Rightarrow$ Self-heating active-N^+: No issue

- Voltage dependency is very low
- Sheet resistance is low compared to others

As known from the literature [36], the spread of TCR_1 and TCR_2 takes place due to different doping concentrations within the process variations. The resistors have a very low temperature dependency. Therefore, the temperature coefficient TCR_1 can easily flip sign and is clearly a function of resistor width. As a consequence, the temperature behavior can change. For the thermal behavior of a resistor it should be kept in mind that a resistor can be split up into several resistive components: $R = R_{contact} + R_{silicided} + R_{bulk} + R_{interface} \cdot \frac{W_0}{W}$. Every one of these resistors has its own temperature coefficient. However, total TCR is dominated by the TCR value of R_{bulk} and $R_{interface}$ [57].

3.4.2 Charge capacitor C

The capacitor in combination with the resistor is what determines period time. Thus, an appropriate choice of capacitor is also incredibly important. For this reason, we can only consider a fringe capacitor, because it possesses very small voltage and temperature dependence. The metal fringe capacitor is based on the capacitance between parallel metal lines (optionally connected with vias) and separated by the intra level dielectric. The capacitor is made of two inter-digitated combs at each metal level, which are stacked and aligned on the METAL1, METAL2, METAL3, METAL4 and METAL5 levels. A bus connects the fingers of both combs at each level. The capacitor is used without shielding because of the parasitic capacitance of the shield. Due to the insufficient capacitance-to-area ratio, the capacitance value could be increased at the fingers through vias. This option was not chosen due to possible reliability problems and the ensuing demands on the voltage screening circuitry.

3.5 Maximum frequency spread across temperatures

In order to estimate the real performance of the oscillator, the maximum frequency deviation in the trimmed state should be evaluated. Analytically, this calculation is not useful via an error calculation, because the variation in reference voltage is expressed with a complex superfunction and the large temperature range calls for at least a Taylor-approximation of the second order. This is why an estimation of the maximum frequency spread across temperatures was carried out via MATLAB ®. To do this, the spread of temperature coefficients was used in equation 3.43 and evaluated across temperatures. The result of this analysis possesses a frequency spread over temperature of $\approx \pm 1.1\%$ in frequency.

3.6 Influence of the offset of the OTA

Ideally, the output of the operation amplifier should be at zero volts when the inputs are grounded. In practice, a small differential voltage must be applied to the inputs to force the output to zero. This is known as the input offset voltage V_{OS}. The input offset voltage is modeled as a voltage source V_{OS}, switched in series with the inverting or non-inverting input terminal of the operation amplifier [11].

See the following literature: Gray and Meyer [17], and Dostal [13] for more details concerning V_{OS} and the V_{OS} drift over temperature.

Typical CMOS operation amplifiers have offset voltages of around $200\mu V$ to $10000\mu V$ and offset voltage drifts of $0.4\frac{\mu V}{K}$ to $10\frac{\mu V}{K}$, respectively [23].

3.6.1 Frequency changes due to offset voltage

Because the offset voltage can be switched in series to the non-inverting input like a voltage source, a change in offset voltage is equivalent to a change in the reference voltage V_{ref} of the oscillator. Therefore, the frequency sensitivity is equivalent to: $186.1\frac{\%}{V} = 0.1861\frac{\%}{mV}$. For further information see chapter 3.8.1. As with a reference voltage offset, the static offset voltage can easily be compensated for during the

trimming process. It is more difficult to compensate for the offset voltage drift. An offset voltage drift can only be compensated for with a multi-point trimming process. However, such trimming processes are very costly and therefore not usable. See also chapter 6.3, concerning the aging effects of the offset voltage. The design criteria for the input-pair area were specified according to the maximum offset voltage drift. Frequency errors due to the offset voltage drift should reach at most ±0.1%.

This results in a maximum offset voltage drift of:

$$\pm 0.1\% = 0.1861 \frac{\%}{mV} \cdot \pm V_{OS} \tag{3.6}$$

$$\pm TC_{V_{OS}} \cdot \Delta T = \pm V_{OS} \tag{3.7}$$

$$\frac{\pm 0.1\%}{0.1861 \frac{\%}{mV} \cdot 190°C} = \pm TC_{V_{OS}} = \pm 2.8 \frac{\mu V}{K} \tag{3.8}$$

V_{OS} ... Offset voltage

$TC_{V_{OS}}$ ... Temperature coefficient of the offset voltage

ΔT ... Temperature range

3.7 Influence of the comparator offset voltage

As mentioned in chapter 3.6, the offset voltage also displays temperature-dependent behavior. The offset voltage of the comparators is an uncritical factor for our oscillator. However, we need to distinguish two separate cases:

- Both comparators possess the same offset voltage and the same offset voltage drift.
- The offset voltage and the offset voltage drift are different in the two comparators.

The first case is insignificant because the offset voltage and the offset voltage drift are the same for both comparators. In the functional concept of the oscillator, this acts as an additional comparator delay, which is compensated for wholly through the circuitry. The second case is more critical. In this case, the duty-cycle of the clock frequency changes. Furthermore, a change in frequency takes place because assuming

differential drift behavior in the offset voltages. In that case the integrated voltages V_{RCleft} and $V_{RCright}$ have different areas. Therefore, differential drift behavior in offset voltage can only be compensated for by circuitry on average. That means, the specification value to be determined is the differential offset voltage drift of the comparators, since this causes a duty-cycle variation and a change in frequency.
Note: The frequency change due the the static offset voltage and the mismatch in the RC-products are compensated due to the trim procedure in the test phase.

3.7.1 Duty-cycle variation due to mismatch

The symmetry of an oscillating clock voltage is defined by the duty-cycle. This parameter is determined by differential offset voltage, differential offset voltage drift of the comparators and mismatch of the RC-product. Therefore its necessary to specify the maximum differential offset voltage drift and the mismatch. From these results, the required offset voltage behavior and the required mismatch can be achieved by adding to the area. However, the proposed oscillator can achieve a good accuracy for the following reasons. Passive devices as the charge resistor R and the charge capacitor C are well matched in CMOS processes. As discussed before, a limiting factor is the mismatch of differential pairs of comparators. However, this is not a critical issue because a reasonable design will keep the mismatch small, which results in duty-cycle degradation by less than 1% which is negligible for the application [63].
The duty-cycle D is defined as: $D = \frac{T_{ON}}{T} = \frac{T_{ON}}{T_{ON}+T_{OFF}} = \frac{1}{1+\frac{T_{OFF}}{T_{ON}}}$

Passive duty-cycle variation

Because period time results from the two RC-charging curves (V_{RCleft} and $V_{RCright}$), we can assume that T_{ON} and T_{OFF} are proportional to the two RC-products. The mismatch of fringe capacitors is much lower than that of poly-silicon resistors. Therefore, it can be said that the whole passive mismatch is dominated by the poly-silicon resistors [63]. From the mismatch parameters of the resistor, we can deduce (see data sheet [39]):

$$6 \cdot \sigma \left(\frac{R_\Delta}{\bar{R}} \right) = 0.15 \tag{3.9}$$

$$6 \cdot \sigma \left(\frac{C_\Delta}{\bar{C}} \right) = \text{negligible, see [4]} \tag{3.10}$$

$$T_{ON} \propto R_{right} C_{right} \tag{3.11}$$

$$T_{OFF} \propto R_{left} C_{left} \tag{3.12}$$

$$D_{min} = \frac{1}{1 + \frac{R_{left} C_{left} \cdot 1.15}{R_{right} C_{right}}} = \frac{1}{1 + \frac{1.15}{1}} = 0.465 \tag{3.13}$$

$$D_{max} = \frac{1}{1 + \frac{R_{left} C_{left}}{R_{right} C_{right} \cdot 1.15}} = \frac{1}{1 + \frac{1}{1.15}} = 0.534 \tag{3.14}$$

Where $R_{left}C_{left}$ and $R_{right}C_{right}$ are assumed as a ideal RC. Assuming a symmetrical distribution, this signifies a duty-cycle variation of $\pm 3.5\%$.

Active duty-cycle variation due to ΔV_{os} of the comparators

A static differential offset voltage of the two comparators leads, as mentioned before, to a duty-cycle variation, because the threshold of the comparator changes. The maximum offset voltage variation can be calculated as follows.
Assuming $t_{CompDelay}$=0s, maximum duty-cycle variation of $\pm 1\%$, and the period time T changes due to the duty-cycle variation:

$$t = \frac{T}{2} = t_{th} \tag{3.15}$$

$$V_{RCleft}(t) = V_{CompThresh} = Vdd \left(1 - e^{\frac{-t_{th}}{RC}} \right) \tag{3.16}$$

$$V_{RCright}(t) = V_{RCleft}(t) + V_{OS} = Vdd \left(1 - e^{\frac{-(t_{th} + t_{OS})}{RC}} \right) \tag{3.17}$$

$$D = \frac{T_{ON} + t_{OS}}{T} \tag{3.18}$$

$$t_{OS} = D \cdot T - T_{ON} \tag{3.19}$$

$$V_{OS}(D) = V_{RCright} - V_{RCleft} = Vdd \cdot e^{\frac{-t_{th}}{RC}} \left(1 - e^{\frac{-(D \cdot T - T_{ON})}{RC}} \right) \tag{3.20}$$

So if we assume a duty-cycle of D=0.5 $\pm 1\%$ with Vdd=1.8V, T=62.5ns and

$T_{ON} = \frac{T}{2}$ than the ΔV_{OS} has to be less then 11mV.

As the formulas make apparent, the variation of duty-cycle is also a function of the comparator threshold because the threshold time t_{th} (in our case $t_{th} = T/2$ with $t_{CompDelay} = 0s$) is still in the equation 3.20.

3.8 Period time equation and sensitivity analyses

In order to derive a frequency equation, the oscillating voltage node V_{osc} at the active filter has to be considered. As described in the section "Start-up and oscillation mechanism", the oscillating RC-voltage V_{RCleft} and $V_{RCright}$ are alternately applied to the active filter. Due to the large time constant of the active filter, an averaging of this signal takes place. That means, $V_{osc} = V_{RCleft} + V_{RCright}$ is virtually shortened in a low frequency domain defined by the time constant and the amplification of the integrator (active filter), see equation 3.23 [10].

The derivation is as follows:

Assume a constant gain-bandwidth product.

$$1 \cdot f_{A=1,CL} = f_{3dB} \cdot A_0 \tag{3.21}$$

$$f_{A=1,CL} = \frac{1}{2\pi R_{int} C_{int}} \longrightarrow |A(s = j2\pi f_{A=1,CL})| = 1 \tag{3.22}$$

$$f_{3dB} = \frac{1}{2\pi R_{int} C_{int} A_0} \tag{3.23}$$

$f_{A=1,CL}$ ... Unity frequency closed loop

A_0 ... DC-gain of the integrator

f_{3dB} ... Cut-off frequency of the integrator

$A(s)$ ... Frequency response of the integrator

The integrator controls the average value of V_{osc}, that it corresponds exactly to that of V_{ref}, see equation 3.24. That is, the oscillator behaves like a voltage controlled oscillator, controlled by the output voltage $V_{CompThresh}$ of the active filter. Assuming an ideal amplifier, $R << R_{int}$ and $\tilde{T} = \frac{T}{2}$, an equation can be derived as follows.

$$V_{ref} = \frac{1}{\tilde{T}} \int_0^{\tilde{T}} V_{osc}\, dt \tag{3.24}$$

V_{osc} is the voltage at the charging capacitor C,

$$V_{ref} = \frac{1}{\tilde{T}} \int_0^{\tilde{T}} V_{dda} \left(1 - e^{\frac{-t}{RC}}\right) dt \tag{3.25}$$

Now the limits of the integral are used,

$$V_{ref} = \frac{V_{dda}}{\tilde{T}} \left(\tilde{T} - \left(RC - RC\, e^{\frac{-\tilde{T}}{RC}}\right)\right) \tag{3.26}$$

Separation of the T dep. equations,

$$\frac{\left(1 - \frac{V_{ref}}{V_{dda}}\right) \tilde{T}}{RC} = 1 - e^{\frac{-\tilde{T}}{RC}} \tag{3.27}$$

$$\alpha = \frac{V_{ref}}{V_{dda}} \tag{3.28}$$

It follows that,

$$\frac{(1-\alpha)\, \tilde{T}}{RC} = 1 - e^{\frac{-\tilde{T}}{RC}} \tag{3.29}$$

An important characteristic of this equation is that there is no dependency on V_{dda} if V_{ref} is derived from V_{dda}, see equation 3.29 and 3.28. Therefore, in the ideal case, frequency does not depend on supply. However, due to non-ideal factors, the supplies have an influence on the frequency. Furthermore, as shown in the equation 3.29, the oscillation is fully independent of the comparator delay. That is, the comparator variation delay will be fully compensated. Due to the type of the equation (superfunction) a closed solution to the frequency cannot be easily given [62]. In our case such an equation can only be solved with the lambert-W function, also called the omega function or product logarithm [59]. To find a closed solution for the half period $\tilde{T}$

of the oscillation, the equation has to be converted to a similar shape as that of the function $f(w) := w \cdot e^w$. Where e^w is the exponential function and w is any complex number. The lambert-W function gives the principal solution for w in $z = w \cdot e^w$.

Equation 3.29 has to be solved for T,

$$\frac{(1-\alpha)\,\tilde{T}}{RC} = 1 - e^{\frac{-\tilde{T}}{RC}} \tag{3.30}$$

$$e^{\frac{-\tilde{T}}{RC}} = \frac{\tilde{T}\,(\alpha-1)}{RC} + 1 \tag{3.31}$$

It follows that,

$$-\tilde{T}/RC = \ln\left(\frac{\tilde{T}\,(\alpha-1)}{RC} + 1)\right) \tag{3.32}$$

$$0 = \ln\left(\frac{\tilde{T}\,(\alpha-1)}{RC} + 1\right) + \tilde{T}/RC \tag{3.33}$$

Multiply by $(\alpha - 1)$,

$$0 = \ln\left(\frac{\tilde{T}\,(\alpha-1)}{RC} + 1\right)(\alpha-1) + \frac{\tilde{T}}{RC}(\alpha-1) \tag{3.34}$$

Add one,

$$1 = \ln\left(\frac{\tilde{T}\,(\alpha-1)}{RC} + 1\right)(\alpha-1) + \frac{\tilde{T}\,(\alpha-1)}{RC} + 1 \tag{3.35}$$

Divide by $(\alpha - 1)$,

$$\frac{1}{(\alpha-1)} = \ln\left(\frac{\tilde{T}\,(\alpha-1)}{RC} + 1\right) + \frac{\frac{\tilde{T}(\alpha-1)}{RC} + 1}{(\alpha-1)} \tag{3.36}$$

Note: $\ln(xe^y) \Rightarrow \ln(x) + \ln(e^y) \Rightarrow \ln(x) + y$,

$$\frac{1}{(\alpha-1)} = \ln\left(\left(\frac{\tilde{T}(\alpha-1)}{RC}+1\right)e^{\frac{\frac{\tilde{T}(\alpha-1)}{RC}+1}{(\alpha-1)}}\right) \tag{3.37}$$

Thus,

$$e^{\frac{1}{(\alpha-1)}} = e^{\ln\left(\left(\frac{\tilde{T}(\alpha-1)}{RC}+1\right)e^{\frac{\frac{\tilde{T}(\alpha-1)}{RC}+1}{(\alpha-1)}}\right)} \tag{3.38}$$

It follows that,

$$e^{\frac{1}{(\alpha-1)}} = \left(\frac{\tilde{T}(\alpha-1)}{RC}+1\right)e^{\frac{\frac{\tilde{T}(\alpha-1)}{RC}+1}{(\alpha-1)}} \tag{3.39}$$

Divide by $(\alpha-1)$,

$$\frac{e^{\frac{1}{(\alpha-1)}}}{(\alpha-1)} = \frac{\left(\frac{\tilde{T}(\alpha-1)}{RC}+1\right)}{(\alpha-1)}e^{\frac{\frac{\tilde{T}(\alpha-1)}{RC}+1}{(\alpha-1)}} \tag{3.40}$$

Note: $z = we^w \Rightarrow W(z) = W(we^w) \longrightarrow W(z) = w$,

$$W\left(\frac{e^{\frac{1}{(\alpha-1)}}}{(\alpha-1)}\right) = W\left(\frac{\left(\frac{\tilde{T}(\alpha-1)}{RC}+1\right)}{(\alpha-1)}\cdot e^{\frac{\frac{\tilde{T}(\alpha-1)}{RC}+1}{(\alpha-1)}}\right) \tag{3.41}$$

and hence,

$$\tilde{T} = \frac{RC\left(W\left(\frac{e^{\frac{1}{(\alpha-1)}}}{(\alpha-1)}\right)(\alpha-1)-1\right)}{(\alpha-1)} \tag{3.42}$$

Therefore, the period time T of the oscillator is,

Assumption: $\tilde{T} = \frac{T}{2} \longrightarrow T = 2 \cdot \tilde{T}$,

$$T = 2\frac{RC\left(W\left(\frac{e^{\frac{1}{(\alpha-1)}}}{(\alpha-1)}\right)(\alpha-1)-1\right)}{(\alpha-1)} \tag{3.43}$$

3.8.1 Sensitivity of T to α

As shown in equation 3.43, the length of one period and therefore also the frequency is a function of α. An analysis of the sensitivity of the period time T to α is therefore very important for frequency stability.

Some facts about the period time equation 3.29

- The equation 3.29 consists of a linear and an exponential function.
- The intersection point of the linear and the exponential function in equation 3.29 gives the length of one half period of the oscillation. Therefore, if there is a variation of $\Delta\alpha$ then the length of a period also changes by ΔT.

To make the circuit stable in the case of short or long term parameter shifts of α, it is necessary to find the minimum frequency sensitivity. Therefore, we define the sensitivity of the oscillation to α as, $S_\alpha = \frac{1}{T}\frac{\partial T}{\partial \alpha}$ and estimate its behavior.
Note: The following relation was used for the derivation $\frac{d}{du}(W(u)) = \frac{W(u)}{u(W(u)+1)}$.

Derivation without proof:

$$S_\alpha = \frac{1}{T}\frac{\partial T}{\partial \alpha} = \left(2\frac{RC(W\left(\frac{e^{\frac{1}{(\alpha-1)}}}{(\alpha-1)}\right)(\alpha-1)-1)}{(\alpha-1)} \right)^{-1} \cdot \frac{\partial}{\partial \alpha}\left(2\frac{RC(W\left(\frac{e^{\frac{1}{(\alpha-1)}}}{(\alpha-1)}\right)(\alpha-1)-1)}{(\alpha-1)} \right) \tag{3.44}$$

$$S_\alpha = \frac{\alpha-1}{2RC\left((\alpha-1)W\left(\frac{e^{\frac{1}{\alpha-1}}}{\alpha-1}\right)-1\right)} \cdot \frac{-2RC\left((\alpha-1)W\left(\frac{e^{\frac{1}{\alpha-1}}}{\alpha-1}\right)-1\right)}{(\alpha-1)^2\left(W\left(\frac{e^{\frac{1}{\alpha-1}}}{\alpha-1}\right)+1\right)} \tag{3.45}$$

$$S_\alpha = \frac{-1}{(\alpha-1)\left(W\left(\frac{e^{\frac{1}{\alpha-1}}}{\alpha-1}\right)+1\right)} \tag{3.46}$$

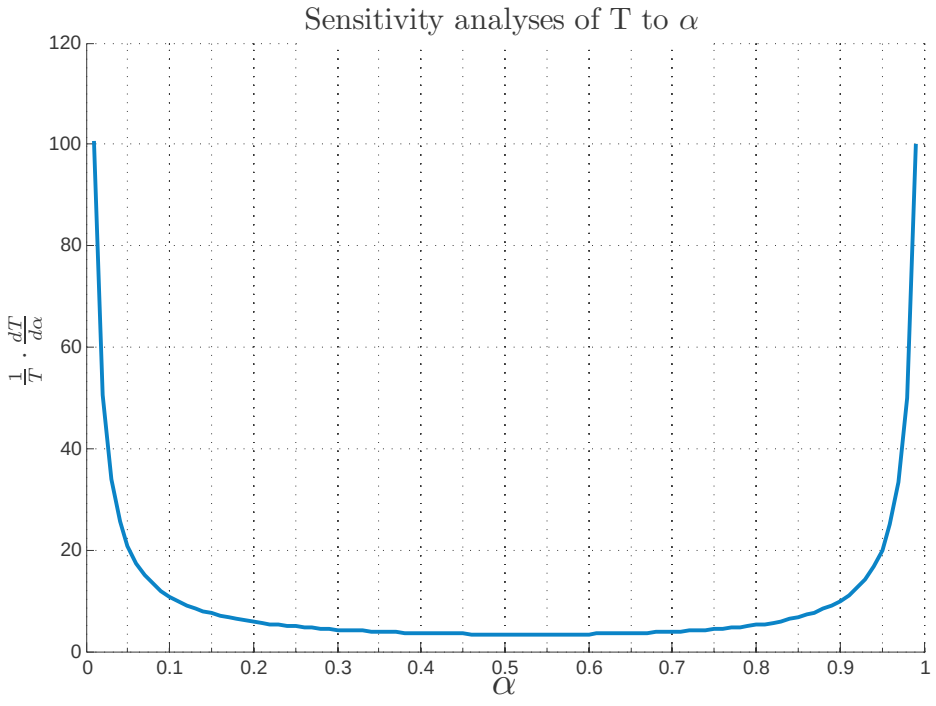

Figure 3-4: Sensitivity of the period time to α

The result shows an interesting characteristic of the sensitivity with a minimum sensitivity of 3.351 at 0.535. As depicted in figure 3-4, the curve has a flat minimum

so that a variation of α within a small range does not have a large effect on the sensitivity. However, the most important fact is that the sensitivity to α is independent of RC. That means the sensitivity is the same for different frequencies. For better interpretation, the results can be converted to a sensitivity in % per mV.

$$S(\alpha) = \frac{1}{T}\frac{\partial T}{\partial \alpha} \tag{3.47}$$

$$[S(\alpha)] = \left[\frac{\frac{\partial T}{T}}{\frac{\partial V_{ref}}{Vdda}}\right] \longleftrightarrow \frac{\frac{s}{s}}{\frac{V}{V}} \tag{3.48}$$

$$\left[\frac{S(\alpha)}{V_{dda}}\right] = \left[\frac{\frac{\partial T}{T}}{\partial V_{ref}}\right] \longleftrightarrow \frac{\frac{s}{s}}{V} \tag{3.49}$$

$$\left[\frac{S(\alpha)\cdot 100}{V_{dda}}\right] = \left[\frac{\frac{\partial T}{T}\cdot 100}{\partial V_{ref}}\right] \longleftrightarrow \frac{\%}{V} \tag{3.50}$$

For instance, with $V_{dda} = 1.8$V, the period length changes with 0.186% per mV variation of V_{ref}.

$$\frac{S(0.535)\cdot 100}{1.8V} = \frac{3.531\cdot 100}{1.8V} \Longrightarrow 186.1\frac{\%}{V} \tag{3.51}$$

$$186.1\frac{\%}{V} = 0.1861\frac{\%}{mV} \tag{3.52}$$

3.8.2 Sensitivity of T to the comparator threshold

This sensitivity is important for phase noise considerations, because noise at $V_{CompThresh}$ leads to a short term variation in frequency if a constant comparator delay is assumed. Note: A long term $V_{CompThresh}$ variation will be compensated due to the averaging behavior of the circuit. $V_{CompThresh} = V_{dda}\left(1 - e^{\frac{-(\tilde{T}-t_{CompDelay})}{RC}}\right)$ where $\tilde{T} = \frac{T}{2}$ is a function of α. Therefore, the comparator threshold $V_{CompThresh}$ is determined by α and the comparator delay. Intuitively, it can be said that the greater the slope in the intersection point of the compare, the less sensitive is the change in period time.

Assume: $t_{CompDelay}$, α are constant and the averaging behavior is to slow for a noise event.

$$V_{CompThresh} = V_{dda}\left(1 - e^{\frac{-(\tilde{T}-t_{CompDelay})}{RC}}\right) \quad (3.53)$$

$$t_{CompDelay} - \ln\left(1 - \frac{V_{CompThresh}}{V_{dda}}\right)RC = \tilde{T} \quad (3.54)$$

$$t_{CompDelay} - \ln\left(1 - \frac{\Delta V_{CompThresh}}{V_{dda}}\right)RC = \Delta\tilde{T} = \frac{\Delta T}{2} \quad (3.55)$$

$$S(V_{CompThresh}) = \frac{1}{T}\frac{\partial \tilde{T}}{\partial V_{CompThresh}} \quad (3.56)$$

$$S(V_{CompThresh}) = \frac{RC}{2 \cdot (V_{dda} - V_{CompThresh})\left(t_{CompDelay} - RC \cdot ln(1 - \frac{V_{CompThresh}}{V_{dda}})\right)} \quad (3.57)$$

As expected the sensitivity to the comparator threshold depends on many factors. Thus, the slope in the intersection point determines the variation of the period time. That is, that the RC-product, the supply voltage and the comparator threshold determines the sensitivity. Therefore, a NMOS differential input pair has to be used in the comparator, because the input common mode (ICM) can be lower compared to a PMOS one. The slope in the RC-curve is higher for a low ICM (low $V_{CompThresh}$) and this leads to a smaller variation in the period time as mentioned above.

3.9 Ideal temperature compensation

Another important topic is the theoretical determination of the best possible frequency accuracy across temperature for a given set of variables. Such problems are called optimization problems. A optimization problem is the selection of a best variable combination (with regard to some criteria) from some set of available alternatives. Because of the high precision requirements, it is necessary to examine all parasitic effects and their sensitivity to frequency. The frequency determining blocks include the charging resistor R, the charging capacitor C and the reference voltage V_{ref}. To examine frequency stability across PVT-variations, we need to identify all effects that change frequency.

Frequency-changing PVT effects include:

- PVT dependence in the charging resistor R
- The process-dependent distribution of resistor temperature coefficients
- PVT dependence in the charging capacitor C
- The process-dependent distribution of capacitance temperature coefficients
- PVT dependence of the R_{on} in the NMOS trim-circuit switching transistor
- PVT dependence of parasitic capacitances in the NMOS trim-circuit switching transistor
- PVT dependence of parasitic capacitances in the discharge NMOS MN_1 and MN_2
- Current leakage through the switched off discharge NMOS
- PVT dependence of the parasitic input capacitance in the comparator
- Kick-back noise at the comparator threshold due to the comparator
- PVT dependence of the R_{on} in the PMOS MP_1 and MP_2 switching transistor
- PVT dependence of the input capacitance of the transmission gate (TMG)
- Current leakage through the switched-off TMG
- PVT dependence of the TMG R_{on} combined with the parasitic capacitance of

the integrator resistor R_{int} causes a voltage drop at V_{osc} by $R_{on,TMG} \cdot C_{para} \frac{\partial U_{Cpara}}{\partial t}$

- Ripple on the supply voltage because of the influence of a real supply voltage source
- Unwanted spread of the temperature dependence at the reference node V_{ref}
- Influence through the active filter (if the chosen integrator resistor R_{int} is too small)
- PVT dependence of the charge injection

In order to get an analytic description of the frequency behavior over temperature, only the main dependencies were observed. The frequency temperature behavior is equal to:

Assumption: C, R depend on the temperature T, α is independent of T.

$$F(T) = 2\frac{(\alpha-1)}{R(T)\cdot C(T)\left(W(\frac{1}{e^{\frac{1}{(\alpha-1)}}(\alpha-1)})(\alpha-1)-1\right)} \tag{3.58}$$

$$\text{where, } R(T) = R_{27}(1+TCR_1(T-27)+TCR_2(T-27)^2) \tag{3.59}$$

$$\text{and, };C(T) = C_{27}(1+TCC_1(T-27)) \tag{3.60}$$

So if α depends in the right way to the temperature T, the frequency temperature behavior can be compensated.

3.9.1 Theoretical, non-linear optimization approach

As shown in equations 3.60, frequency dependency can be compensated via a temperature-dependent reference voltage. The following equations represent a possible approach to the compensation of frequency behavior.

$$F\,(T) = 2\frac{(\alpha-1)}{R(T)\cdot C(T)\left(W\left(\frac{1}{e^{\frac{1}{(\alpha-1)}}}\right)(\alpha-1)-1\right)} \tag{3.61}$$

Where $\alpha = \alpha_0\left(1+\alpha_1\left(T-27\right)+\alpha_2\left(T-27\right)^2\right)$

$$F\left(T\right) = F_{27}\left(1+TCF_1\left(T-27\right)+TCF_2\left(T-27\right)^2\right) \tag{3.62}$$

$$F_{27} = F\left(T=27°C\right) = 2\frac{\left(\alpha_{27}-1\right)}{R_{27}C_{27}\left(W\left(\frac{e^{\frac{1}{\left(\alpha_{27}-1\right)}}}{\left(\alpha_{27}-1\right)}\right)\left(\alpha_{27}-1\right)-1\right)} \tag{3.63}$$

$$\frac{F\left(T\right)}{F_{27}} = \frac{\left(\alpha-1\right)R_{27}C_{27}\left(W\left(\frac{e^{\frac{1}{\left(\alpha_{27}-1\right)}}}{\left(\alpha_{27}-1\right)}\right)\left(\alpha_{27}-1\right)-1\right)}{\left(\alpha_{27}-1\right)RC\left(W\left(\frac{e^{\frac{1}{\left(\alpha-1\right)}}}{\left(\alpha-1\right)}\right)\left(\alpha-1\right)-1\right)} \tag{3.64}$$

$$= \left(1+TCF_1\left(T-27\right)+TCF_2\left(T-27\right)^2\right) \tag{3.65}$$

If α is independent of T, $\alpha = \alpha_{27}$

$$\frac{F\left(T\right)}{F_{27}} = \frac{R_{27}C_{27}}{RC} = \left(1+TCF_1\left(T-27\right)+TCF_2\left(T-27\right)^2\right) \tag{3.66}$$

So if the α depending term performs like $\frac{1}{\left(1+TCF_1(T-27)+TCF_2(T-27)^2\right)}$ then the frequency is independent of T.

$$\frac{F\left(T\right)}{F_{27}} = \underbrace{\frac{R_{27}C_{27}}{RC}}_{\left(1+TCF_1(T-27)+TCF_2(T-27)^2\right)}\underbrace{\frac{\left(\alpha-1\right)\left(W\left(\frac{e^{\frac{1}{\left(\alpha_{27}-1\right)}}}{\left(\alpha_{27}-1\right)}\right)\left(\alpha_{27}-1\right)-1\right)}{\left(\alpha_{27}-1\right)\left(W\left(\frac{e^{\frac{1}{\left(\alpha-1\right)}}}{\left(\alpha-1\right)}\right)\left(\alpha-1\right)-1\right)}}_{if\ \propto 1/\left(1+TCF_1(T-27)+TCF_2(T-27)^2\right)\rightarrow\frac{F(T)}{F_{27}}=const.} \tag{3.67}$$

Since α is part of the lambert-W function, this equation can be viewed as non-linear. Such equations are difficult to solve analytically. Therefore we need to use a non-linear least-square algorithm to solve the optimization problem [9].

The equation to be solved is:

$$\frac{\left(\alpha-1\right)\left(W\left(\frac{e^{\frac{1}{\left(\alpha_{27}-1\right)}}}{\left(\alpha_{27}-1\right)}\right)\left(\alpha_{27}-1\right)-1\right)}{\left(\alpha_{27}-1\right)\left(W\left(\frac{e^{\frac{1}{\left(\alpha-1\right)}}}{\left(\alpha-1\right)}\right)\left(\alpha-1\right)-1\right)} = \frac{1}{\left(1+TCF_1\left(T-27\right)+TCF_2\left(T-27\right)^2\right)} \tag{3.68}$$

where $\alpha = \alpha_0\big(1 + \alpha_1 (T - 27) + \alpha_2 (T - 27)^2\big)$

This equation should now be solved for α_1 and α_2. The results of α_1 and α_2 represents the temperature coefficients of α to compensate completely the frequency behavior over temperature. Nevertheless the coefficient α_2 is not really easy to implement with a common resistant voltage divider. Therefore, also a non-linear optimization can be used do get the best fit to α. Via the expression $\alpha = V_{ref}/V_{dda}$, the temperature coefficient of the reference voltage can be calculated. With this non-linear optimization approach, we can also find the ideal resistor relation for the reference voltage divider. The non-linear optimization equation was solved using MATLAB ® and the **lsqnonlin()** algorithm, which minimizes the error to α.

Chapter 4

Circuit Design

4.1 Active filter, Integrator

Depending on the application of the oscillator, the active low pass filter (integrator) can be designed using different topologies.

Important design specifications of the OTA include:

- Input common mode range
- Output swing
- Offset voltage and offset voltage drift
- Power consumption
- Bandwidth (BW)
- Phase margin (PM) (settling behavior at start-up)

In our case, low power consumption, low offset drift and a defined settling behavior are required. An offset drift acts like a V_{ref} change which leads to a frequency change of 0.19% per mV. Therefore, a low offset drift over temperature is required. For a maximum acceptable frequency error of 0.1%, the drift has to be below 530uV across a 190°C temperature range. Since the frequency trim in our design is not done via α, a rail-to-rail input is not necessary. This restriction and a high gain improve the offset and also the offset drift of the OTA.

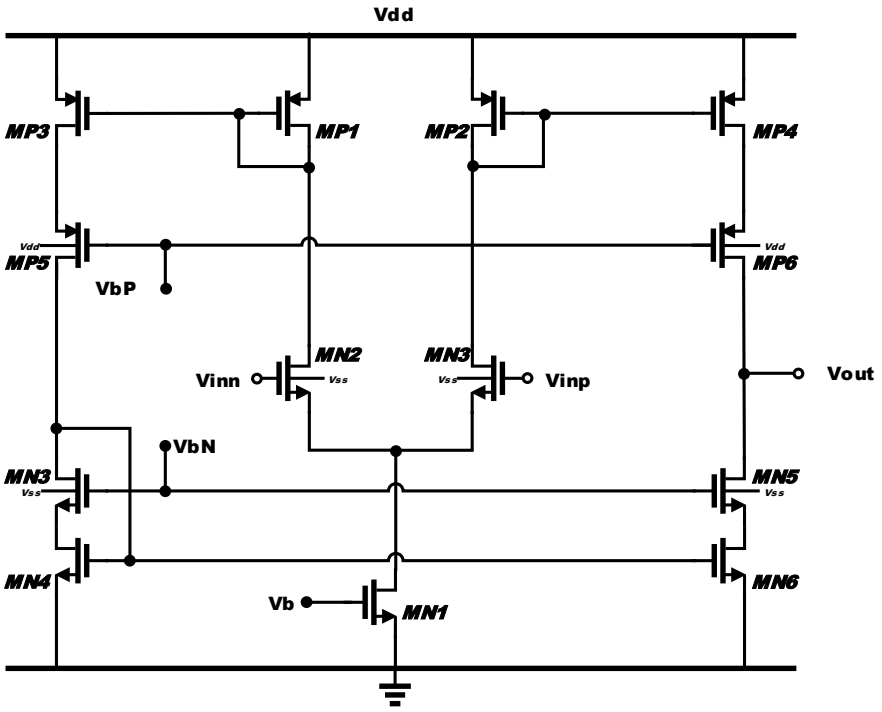

Figure 4-1: Current mirror OTA

4.1.1 Calculations and sizing

Some design aspects:

- A 20% safety margin for the saturation voltage, $(\frac{V_{DS}}{V_{sat}} - 1) \cdot 100\%$ has to be considered for a robust design
- Check of the design with a $\pm 20\%$ bias current variation
- Verification with corner and Monte-Carlo simulation ($\pm 6 \cdot \sigma$ requirement)

Input common mode range

A high input common mode range is not necessary due to the "fixed" input common mode voltage.

$$V_{ICM-} = V_{satMN1} \cdot 1.2 + V_{gsMN2} \tag{4.1}$$

$$with\ V_{bsMN2} = V_{satMN1} \cdot 1.2 \tag{4.2}$$

$$V_{ICM+} = V_{dda} - V_{gsMP1} - V_{satMN2} \cdot 1.2 + V_{gsMN2} \tag{4.3}$$

$$with\ V_{bsMN2} = V_{dda} - V_{gsMP1} - V_{satMN2} \cdot 1.2 \tag{4.4}$$

Due to the more or less fixed voltage at the positive input the V_{ICM} has to be:

$$V_{ICM_+} \approx V_{ddaMAX} \cdot 0.55 \tag{4.5}$$

$$V_{ICM_-} \approx V_{ddaMIN} \cdot 0.55 \tag{4.6}$$

$$where:\ 0.55 = \alpha = \frac{V_{ref}}{V_{dda}} \tag{4.7}$$

V_{ICM+} ... Maximum ICM voltage

V_{ICM-} ... Minimum ICM voltage

V_{ddaMAX} ... Maximum supply voltage, 1.9V

V_{ddaMIN} ... Minimum supply voltage, 1.7V

V_{satMXy} ... Saturation voltage of transistor MXy

V_{gsMXy} ... Gate source voltage of transistor MXy

V_{bsMXy} ... Bulk source voltage of transistor MXy

Output swing

$$V_{Out+} : V_{bP} + |V_{thMP6}| = V_{ddaMIN} - V_{satMP4} \cdot 1.2 - V_{satMP6} \cdot 1.2 \tag{4.8}$$

$$V_{Out-} : V_{bN} - V_{thMN5} = V_{satMN6} \cdot 1.2 + V_{satMN5} \cdot 1.2 \tag{4.9}$$

$$V_{Out-} = V_{ddaMIN}\left(1 - e^{\frac{-(T-t_{CompDelayMAX})}{RC}}\right) \quad (4.10)$$

$$V_{Out+} = V_{ddaMAX}\left(1 - e^{\frac{-(T-t_{CompDelayMIN})}{RC}}\right) \quad (4.11)$$

Where, R=11410Ω, C=1.5pF, $t_{CompDelayMIN} = 7.46ns$ and $t_{CompDelayMAX} = 18.8ns$

V_{Out+} ... Maximum output swing

V_{Out-} ... Minimum output swing

V_{ddaMIN} ... Minimum supply voltage, 1.7V

V_{thMXy} ... Threshold voltage of transistor MXy

V_{satMXy} ... Saturation voltage of transistor MXy

V_{bP} ... Bias voltage for PMOS

V_{bN} ... Bias voltage for NMOS

The OTA has an output voltage swing of 0.6V to 1.2V over process corners and a $\pm 6\sigma$ consideration. This means the range seems to be too small. Although this worst case (w.c.) V_{Out+}=1.2V at 1.7V and 175°C correlates with the high comparator delay at 1.7V and 175°C. In this case, the comparator also displays slow behavior ($13.11ns \pm 6 \cdot 0.4ns$) so that the propagation delay is larger. From this, it follows that the output voltage of the active filter $V_{CompThresh}$ is low in order to compensate the comparator delay.

- Saturation check V_{Out+} by calculation: Propagation delay of the NAND is neglected $V_{Out} = V_{CompThresh}$=$1.7V(1-e^{\frac{-(31.25ns-(13.11ns-6\cdot 0.4ns))}{(11410\Omega \cdot 1.5pF)}}) \approx 1.19V < 1.2V = V_{out+}$ which fulfills the strict assumption of a $\pm 6 \cdot \sigma$ safety margin.

- Saturation check V_{Out+} by simulation: The saturation safety margin has to be larger than 20% under the conditions for the fastest comparator ($-40°C$ and V_{dda}=1.9V). By simulation, a safety margin of 150% of the saturation voltage was observed, which proved to be sufficient.

Offset voltage

The offset voltage does not lead to an accuracy problem because it will be compensated by a trim process. The offset can be adjusted through the area $W \cdot L$ of the current mirrors and differential pair transistors. The offset voltage is under nominal conditions approximately equal to:

$$\sigma_{V_{OS}} \approx \sqrt{\sigma^2_{Vth,Diffp} + \left(\frac{\sigma_{I_{dsMP2}}}{Gm}\right)^2 + \left(\frac{\sigma_{I_{dsMP1}}}{Gm}\right)^2} \tag{4.12}$$

$$V_{OS} : -35uV \pm 6 \cdot 0.8mV \approx \pm 4.8mV \tag{4.13}$$

Offset voltage drift

Linear offset voltage temperature coefficient is: $\pm 528\frac{nV}{K} \pm 6 \cdot 315\frac{nV}{K}$ from $-40°C$ to $150°C$. This leads to $\pm 2.63\frac{uV}{K} \cdot 150°C \approx 500uV$ which corresponds to a frequency variation of max. $\pm 0.1\%$.

Settling time and behavior

The dominant pole of the integrator is defined by the time constant of the active filter so that the start-up time of the oscillator is also dominated by $R_{int} \cdot C_{int}$ [63]. For a time constant τ of $R_{int} \cdot C_{int}$=1M$\Omega \cdot 1pF = 1\mu s$ the frequency has settled up to a negligible error after $10 \cdot \tau$.

AC-behavior

As noted above, a high gain and a big phase margin are necessary for the correct operation of the oscillator. An overshoot of the frequency is not allowed. That is, the OTA should have a large enough phase margin to avoid a frequency overshoot.

Assumption: First order low pass behavior and a closed loop unity frequency (integrator) of $f_{A=1,CL} = \frac{1}{2\pi R_{int} \cdot C_{int}}$. Thus an at least 10 time higher $f_{A=1,OL}$ is necessary, see figure 4-2 and 4-3.

$$GBW = f_{A=1} = A_0 \cdot BW = \frac{Gm}{C_{load}} \tag{4.14}$$

$$f_{A=1,OL} = f_{A=1,CL} \cdot 10 = 10 \cdot \frac{1}{1M\Omega \cdot 1pF} = 10\frac{Mrad}{s} \widehat{=} 1.59MHz \tag{4.15}$$

$$C_{load} = C_{buffer} + C_{inComp} = 9.6pF + 90fF = 9.69pF \tag{4.16}$$

$$Gm = GBW \cdot C_{load} = 10\frac{Mrad}{s} \cdot 9.69pF \approx 96.9uS \tag{4.17}$$

$$A_0 = r_{out} \cdot Gm = 10000 \leftrightarrow 80dB \tag{4.18}$$

$$r_{out} = \frac{10000}{96.9uS} \approx 103M\Omega \tag{4.19}$$

A_0 ... DC-gain open loop

GBW ... Gain-bandwidth open loop

BW ... Bandwidth open loop

Gm ... Transconductance of the differential pair

C_{load} ... Load capacitor

C_{buffer} ... Buffer capacitor

C_{inComp} ... Input capacitance of comparator

$f_{A=1,OL}$ ... Unity frequency open loop

$f_{A=1,CL}$ ... Unity frequency closed loop

However, a lower $R_{int} \cdot C_{int}$ product leads to a larger ripple of the comparator threshold. This should not have an effect on frequency variation, according to [19]. The switching operation of the comparator injects a charge into the threshold node. Therefore, an inharmonic glitch can be observed. This phenomenon is called kick-back noise. It is basically the noise of the switching operation of the first stage back to the input of the comparator. For this reason, and to improve jitter performance, the output of the OTA was buffered by an additional capacitor of about 9.6pF.

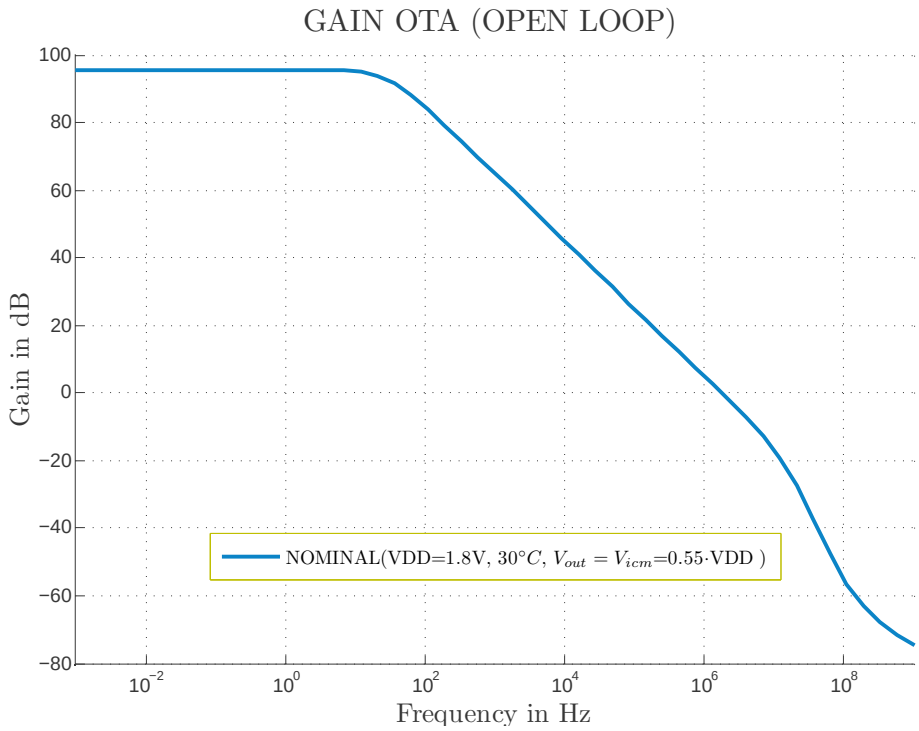

Figure 4-2: Gain of the OTA

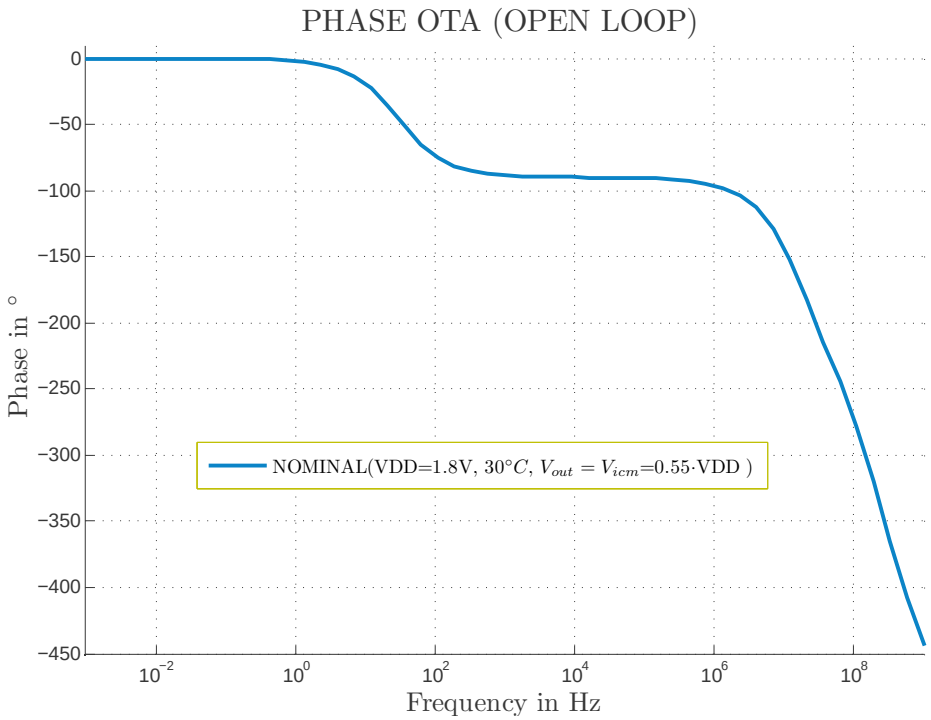

Figure 4-3: Phase of the OTA

Integrator behavior

A conventional low pass filter acts as an integrator if the frequency applied is higher than the cut-off frequency of the filter.

$$A_{lowPass}(s) = \frac{1}{1+sRC} = \frac{1}{1+j\omega RC} \tag{4.20}$$

$$f_{3dBlowPass} = \frac{1}{2\pi RC} \tag{4.21}$$

If $\omega RC \gg 1$ then it follows that $\overbrace{1+j\omega RC}^{j\omega RC}$. So the low pass filter behaves like an ideal integrator $\frac{1}{j\omega RC} \approx \frac{1}{1+sRC}$ if $\omega RC \gg 1$. This result can be transformed from the laplace domain to the time domain which shows the a $\frac{1}{s}$ behavior is an integration in the time domain. The same behavior also applies to an active low pass filter with

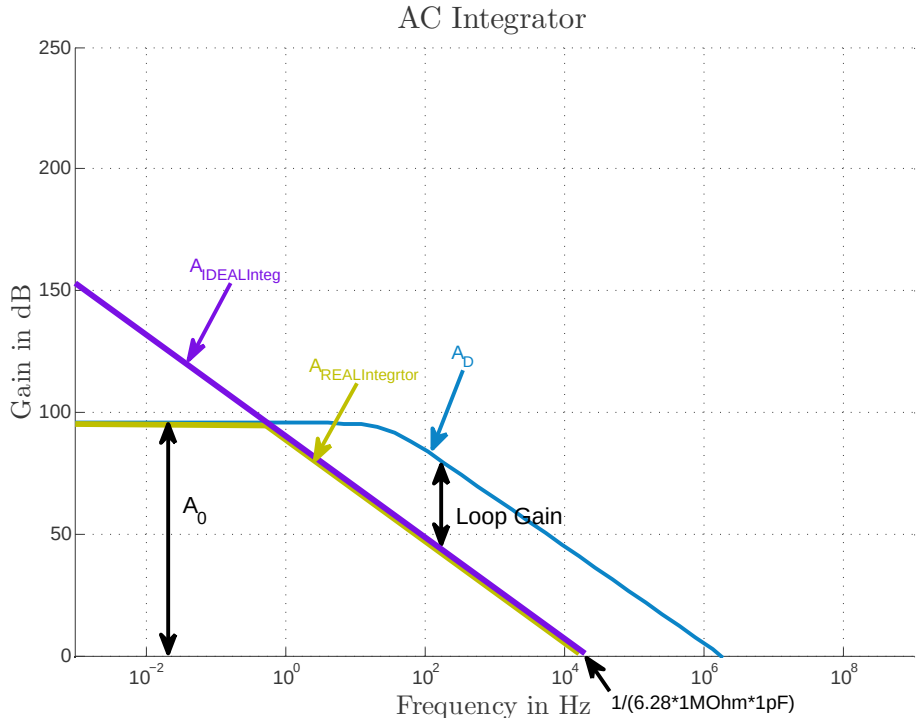

Figure 4-4: AC behavior of the integrator and the differential amplification

the transfer function:

$$A_{activeLPF}(s) = \frac{-A_D(s)}{1 + sR_{int}C_{int}\left(1 + A_D(s)\right)} \tag{4.22}$$

Note: V_{ref} is a static signal (AC-Ground). If the differential amplification of the OTA is $A_D(s) \gg 1$ and the 3dB cut-off frequency $f_{3dB,OL}$ is higher than ≈ 10 times the cut-off frequency $f_{3dB,CL}$ of the closed loop transfer function, then the transfer function can be simplified to that of an ideal integrator [19]:

$$A_{activeLPF}(s) = \frac{-A_D}{1 + sR_{int}C_{int}} \tag{4.23}$$

However, the active filter is used as an integrator which has a very high gain for low frequencies and the $\frac{1}{s}$ behavior after the 3dB cut-off frequency. The critical point about the AC behavior is the 3dB cut-off frequency of the closed loop. Due to the

active filter, the 3dB cut-off frequency is shifted to a lower frequency because the unity gain frequency is $f_{A=1,CL} = \frac{1}{2\pi R_{int} C_{int}}$ and the gain is A_0, see figure 4-4. The active filter behaves in such a way that it has a very high gain for low frequencies, which leads to the average voltage at the input V_{inn} being equal to V_{ref}. So dimensioning as integrator is not really true , because the correct integration is not necessary, but correct averaging is necessary, therefore the 3dB cut-off frequency is the critical point. Note: The integrator only behaves well as an integrator between $f_{3dB,OL}$ and unity frequency $f_{A=1,CL}$. But this fact is not important for our design because we need a low pass filter characteristic with a high gain.

Loop-gain

The loop gain was checked using the stability analysis "stb" form Spectre. A manual setup of the loop gain is depicted in figure 4-5. As depicted in figure 4-5, the loop gain consists of a low pass and a high pass. With no parasitic poles, the system cannot be instable because the phase margin is at least 90 degrees, since in a real system there are some parasitic poles which lead to a phase margin smaller than 90 degrees, see figure 4-7. As noted above, the phase margin has to be large in order to ensure a correct start-up behavior. With a phase margin greater than 60°, the frequency overshoot in the start up phase is very small. For further details and simulation results see table 4.2.

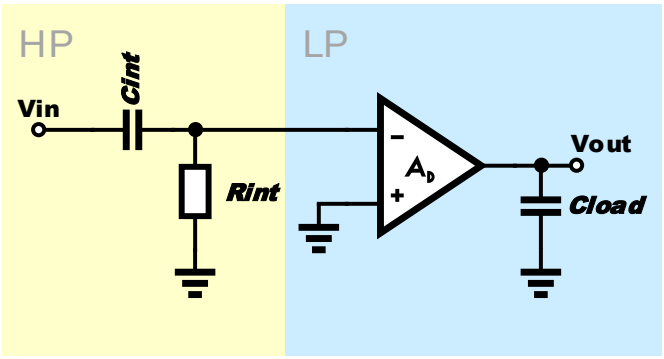

Figure 4-5: Loop-gain setup

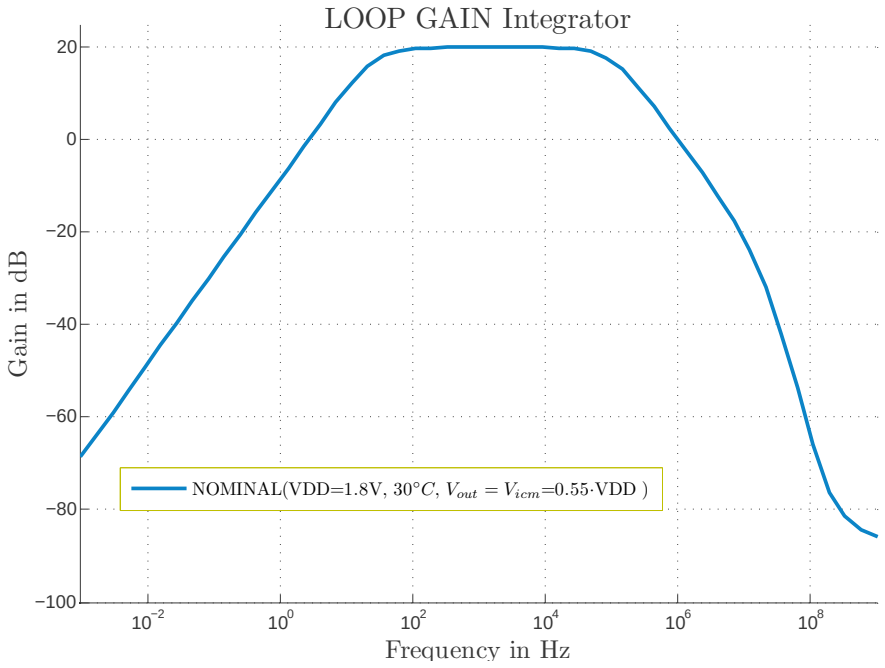

Figure 4-6: Loop-gain of the integrator

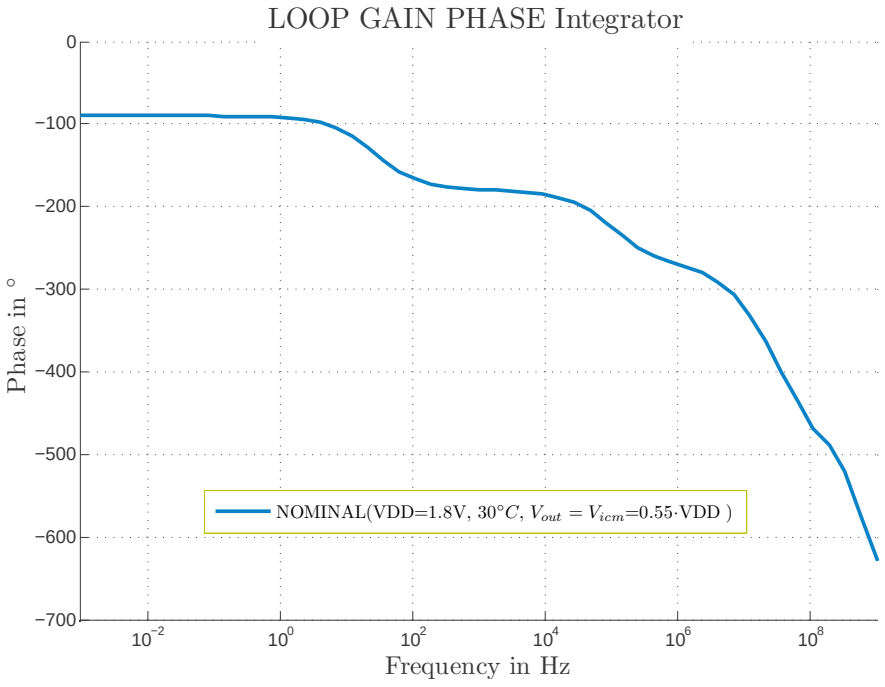

Figure 4-7: Loop-gain phase of the integrator

Table 4.1: OTA-integrator specification table 1 of 2

Symbol	**Parameter**	**Conditions**	6σ **Min**	6σ **Max**	**S. Min**	**S. Max**	**Unit**
V_{dda}	Supply voltage				1.7	1.9	V
T	Temperature				-40	175	°C
V_{ICM}	Input common mode range	MIN: V_{dda}=1.9V, T=−40°C and V_{Out}=0.6V. MAX: V_{dda}=1.7V, T=175°C and V_{Out}=0.6V.	0.87	1.42	0.935	1.045	V
V_{Out}	Output swing	MIN:V_{dda}=1.7V, T=175°C and $V_{ICM} = 0.55 \cdot V_{dda}$ MAX: V_{dda}=1.9V, T=175°C $V_{ICM} = 0.55 \cdot V_{dda}$	0.6	1.2	0.87	1.43	V
$f_{3dB,OL}$	3dB Bandwidth OTA	MIN: V_{dda}=1.9V, T=175°C V_{Out}=1.2V with V_{ICM}=0.87V MAX: V_{dda}=1.7V, T=175°C V_{Out}=1.2V, with V_{ICM}=1.42V $C_{load} = 9.6pF + 90fF = 9.67pF$	22.07	76.73	60		Hz
$f_{A=1,OL}$	Unity gain frequency OTA	MIN: V_{dda}=1.7V, T=175°C V_{Out}=1.2V and V_{ICM}=0.87V MAX: V_{dda}=1.9V, T=−40°C V_{Out}=1.2V and V_{ICM}=1.42V C_{load}=9.67pF	0.77298	3.034	$f_{A=1,CL} \gg f_{A=1}$		MHz
A_0	DC-Gain, OTA	MIN: V_{dda}=1.7V, T=175°C V_{Out}=1.2V and V_{ICM}=0.87V MAX: V_{dda}=1.9V, T=−40°C V_{Out}=1.2V and V_{ICM}=1.42V C_{load}=9.67pF	84.84	99.058	>80		dB

Table 4.2: OTA-integrator specification table 2 of 2

Symbol	Parameter	Conditions	6σ Min	6σ Max	S. Min	S. Max	Unit
PM	Phase margin	MIN:V_{dda}=1.9V, T=$-40°$C V_{Out}=1.2V and V_{ICM}=1.42V MAX: V_{dda}=1.9V, T=175°C V_{Out}=1.2V and V_{ICM}=0.87V C_{load}=9.67pF	77.012	83.284	>70		°
V_{OS}	Offset voltage	V_{dda}=1.8V, T=25°C		±4.8		<5	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Offset voltage drift coefficient	V_{dda}=1.8V, T=$-40°$C to 175°C Eval. at 4σ and approx. to 6σ		± 2.7		< ± 2.6	$\frac{uV}{K}$
PM_{LG}	Phase margin of loop gain	MIN: V_{dda}=1.9V, T=$-40°$C $V_{Out} = V_{ICM} = 0.55 \cdot V_{dda}$ MAX: V_{dda}=1.7V, T=175°C $V_{Out} = V_{ICM} = 0.55 \cdot V_{dda}$ C_{load}=9.67pF, $R_{int} = 1M\Omega$, C_{int}=1pF	85.516	99.204	>80		°
$f_{3dB,CL}$	3dB Bandwidth close loop	MIN:V_{dda}=1.9V, T=$-40°$C V_{Out}=$V_{ICM} = 0.55 \cdot V_{dda}$ MAX:V_{dda}=1.7V, T=175°C $V_{Out} = V_{ICM} = 0.55 \cdot V_{dda}$ C_{load}=9.67pF, $R_{int} = 1M\Omega$, C_{int}=1pF	1.114	5.966		6	Hz
$f_{A=1,CL}$	Unity gain frequency closed loop	MIN: V_{dda}=1.7V, T=175°C $V_{Out} = V_{ICM} = 0.55 \cdot V_{dda}$ MAX: V_{dda}=1.9V, T=$-40°$C $V_{Out} = V_{ICM} = 0.55 \cdot V_{dda}$ C_{load}=9.67pF, $R_{int} = 1M\Omega$, C_{int}=1pF	0.096556	0.2183	$f_{A=1,OL} \gg f_{A=1,CL}$		MHz

4.2 Comparator

In contrast to the OTA design, a time continuous comparator operates without any feedback, thus a consideration of the phase margin is not necessary since there are no stability problems without any feedback.

The key parameters of a comparator are as follows:

- Gain (resolution) $\frac{\Delta V}{V_{dda}}$
- Power dissipation
- Input capacitance
- Kick-back noise
- Offset voltage and offset voltage drift
- Power supply rejection ratio (PSRR)
- Common mode rejection ratio (CMRR)
- Propagation delay for small and high input steps
- Propagation delay when a high input step becomes a low input step (restoring)

In our design, the offset voltage variation between the two comparators lead to an unwanted duty-cycle variation. However, the most important parameter is the comparator delay. This delay determines the output swing of the OTA and the input common mode range of the comparator. Due to this aforementioned unwanted duty-cycle variation, no rail-to-rail input stage was used since this design leads to an undesired high offset. On the other hand, there is a benefit to using a rail-to-rail input stage. If the output swing of the OTA is large, then a very wide range of comparator delays can be compensated. That makes it possible to make the design more energy-efficient because the comparator can be designed as a low power comparator. However a rail-to-rail design leads to a higher offset voltage variation and drift.

Note about the offset voltage: An offset voltage acts more or less like a delay in this design, which is compensated for by the circuit. Only if the two comparators have different offset voltage drifts, then this leads to a change in frequency as the difference between the two drifts cannot be compensated for due to the circuit.

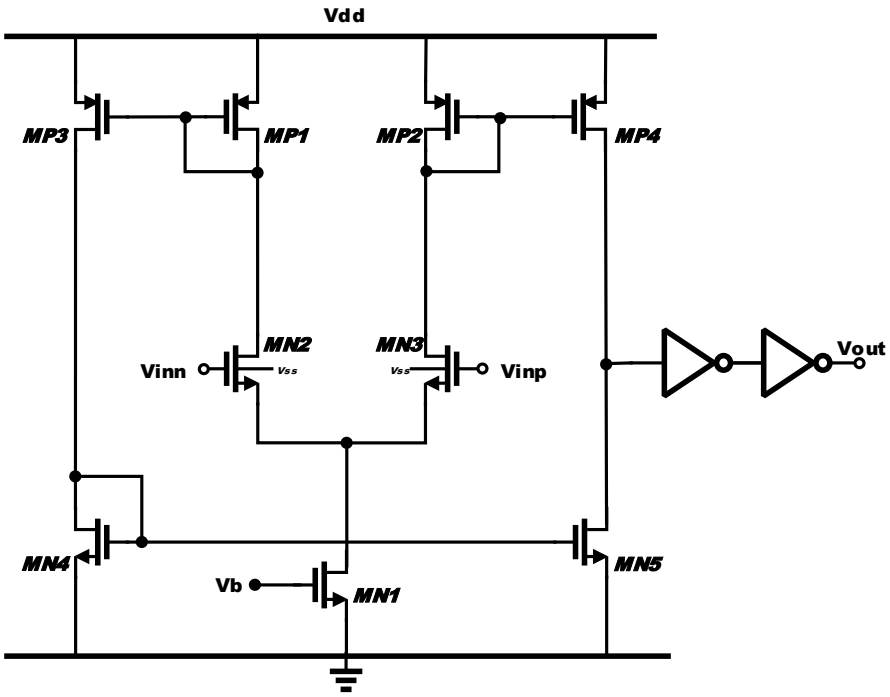

Figure 4-8: Current mirror comparator

4.2.1 Calculations and sizing

Since, as mentioned before, no ultra-low power comparator is necessary. That means that also a rail-to-rail input is not necessary. This leads to the conclusion that an NMOS-input differential pair can be used. With an NMOS-input differential pair, the jitter performance is also better, see chapter 3.8.2. By assuming a minimum and maximum comparator delay, the minimum output swing of the OTA can be calculated. This output swing also represents the minimum input voltage range (input common mode) of the comparator. Due to the fact, that the input of the comparator is directly connected to the charge capacitor, some drawbacks arise. One of these drawbacks is, that the parasitic input capacitance is added to the charge capacitor of the RC-cell. This fact causes the drawback that the voltage dependence of the frequency increases because of the voltage dependence of the parasitic input capacitance. Furthermore, there are glitches due to the kick-back noise at the input of the

comparator, which can be attenuated only through a higher capacitance at the (positive) input. Due to these facts, the requirement of an input capacitance - optimized comparator becomes apparent. The design of the comparator with a certain delay can be done using the GBW-product of the comparator when the frequency response shows a low-pass first-order behavior [5]. Another possibility can be done due to a rough estimation of RC-product of the output node and a following simulation and adaptation of the necessary device values. We used the second approach because of the large signal behavior and a recognizable second pole of the current mirrors.
Now a few words about the comparator design.
As a continuous-time comparator, a current mirror OTA was selected. This is buffered with two inverters at the output. A current mirror OTA has sufficiently large voltage headroom at the input stage and a sufficiently good offset performance. The control of the OTA at the negative input is slower, since the current has to be mirrored about twice at the output node, while the current is mirrored only once if positive input is to be controlled. A further time delay is caused by charge injection due to the transient input voltage. Since the second pole is becoming noticeable due to the current mirror area, a design over a first order low pass characteristic is not possible. The positions of the first and second pole are of importance anyway, as these are also related to the delay. The resolution voltage ΔV is the voltage at which the comparator has to switch to at least V_{dda}. This is approximately equal to the gain $\frac{\Delta V}{V_{dda}}$ of the comparator. With large input amplitude, the delay basically depends on the output resistance and its output capacity. The output node of the OTA is connected to a small inverter. This improves the slew rate of the OTA in order to avoid excessive switching losses on the following NAND. So an adequate rise and fall time can be achieved at the output of the comparator.

Voltage dependency due to the input capacitance

Due to a supply voltage change of about 200mV, the input capacitance of the comparator changes by about 2fF, which leads to a frequency change of about 0.14%. Therefore, there is a trade-off between offset voltage, input capacitance and kick-

back noise.

Input common mode range

In many cases, comparators have to be able to handle a large common mode range. Since for a one-stage amplifier, we have a trade-off between gain and voltage headroom. In contrast to the design of the OTA, a comparator with differential pairs has to be completely in saturation when the comparator switches. The necessary input common mode range is connected to the maximum and minimum comparator delay.

$$V_{ICM-} = V_{Out-} = V_{ddaMIN}\left(1 - e^{\frac{-(T-t_{CompDelayMAX})}{RC}}\right) \quad (4.24)$$

$$V_{ICM+} = V_{Out+} = V_{ddaMAX}\left(1 - e^{\frac{-(T-t_{CompDelayMIN})}{RC}}\right) \quad (4.25)$$

Where, $R = 11410\Omega$, $C_{ges} = 1.5pF$, $t_{CompDelayMIN} = 7.46ns$ and $t_{CompDelayMAX} = 18.8ns$

V_{ICM+} ... Maximum ICM voltage
V_{ICM-} ... Minimum ICM voltage
V_{Out+} ... Maximum output swing
V_{Out-} ... Minimum output swing
V_{ddaMAX} ... Maximum supply voltage, 1.9V
V_{ddaMIN} ... Minimum supply voltage, 1.7V

This means, that the output swing of the OTA has to be equal to at least the necessary input common mode range of the comparator.

Output current

Assumption: The pole at the output is dominant. If the second pole at the current mirror is near the dominate pole some side effects can be observed. A second pole delays the signal due to a higher capacitance load at the current mirrors.

Rough calculation see [14]:

$$\frac{I_{MP4}}{C_L} = S_R \tag{4.26}$$

$$I_{MP4} = S_R \cdot C_L \tag{4.27}$$

$$t_p = \frac{V_{OH} - V_{OL}}{2 \cdot S_R} \rightarrow S_R = \frac{1440mV}{9ns \cdot 2} = 80\frac{V}{\mu s} \tag{4.28}$$

$$I_{MP4} = 80\frac{V}{\mu s} \cdot C_L \tag{4.29}$$

I_{MP4} ... Output current of the output stage.

S_R ... Slew rate.

C_L ... Load capacitor at the output of the amplifier. Input capacitance of inverter plus output capacitance from the output stage MP4, MP5.

t_p ... Propagation delay, 9ns.

V_{OH} ... Output high 90%, 1.62V.

V_{OL} ... Output low 10%, 180mV.

Further information are given in [5], [27] and [14].

Comparator gain and phase

In the figure 4-9 and 4-10 the comparator gain and phase can be seen for different conditions.

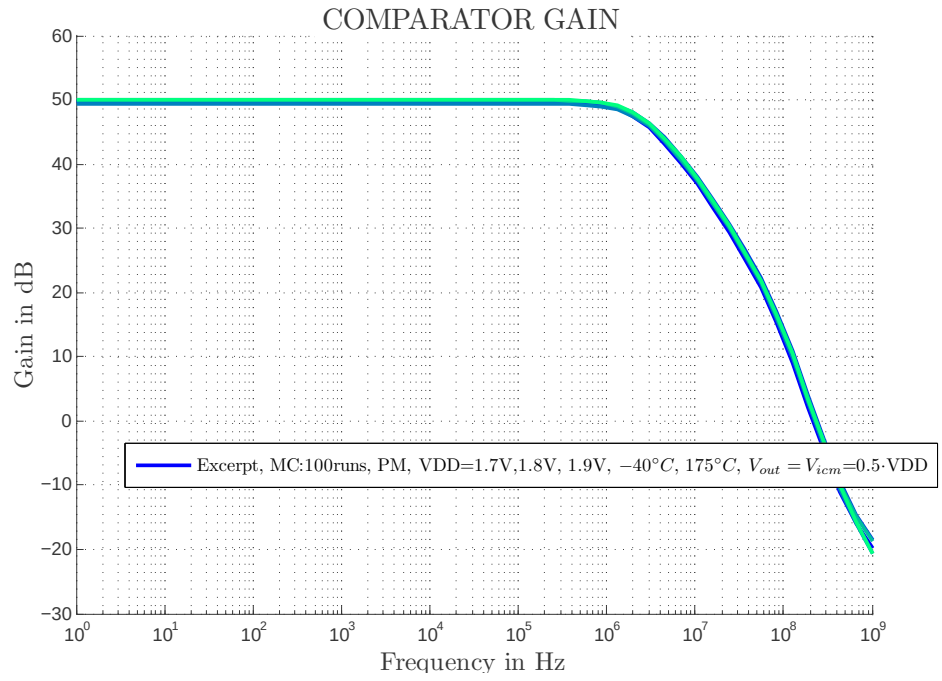

Figure 4-9: Gain of the comparator

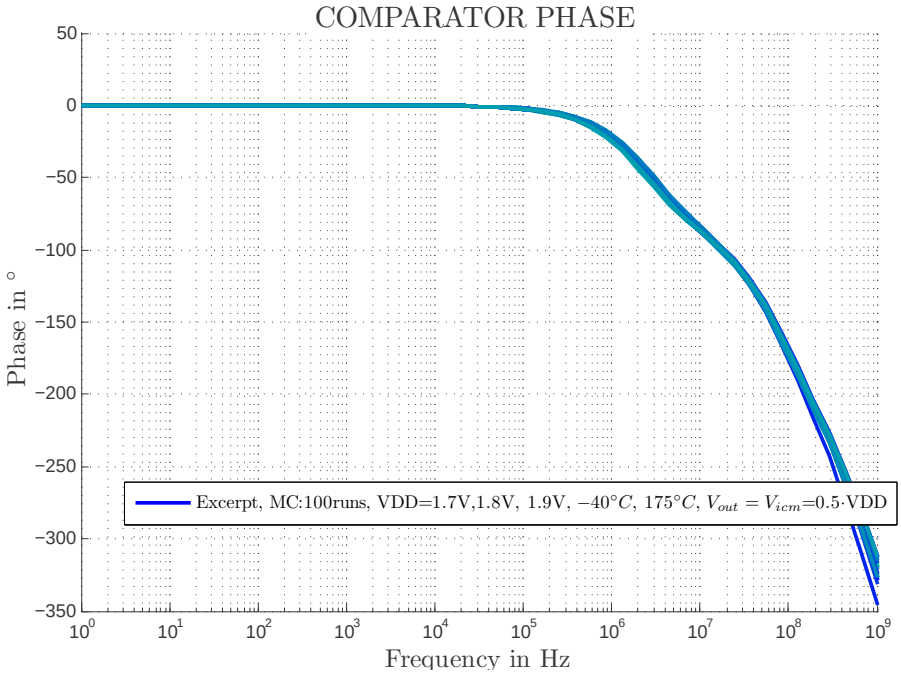

Figure 4-10: Phase of the comparator

4.3 Output driver

The output driver is only necessary for the test chip. Consequently this power consumption shall not add to the RC-oscillator power consumption. For this reason and because of the higher voltage ripple at the supply voltage due to the driver, the supply of this driver has to be forced externally.

4.3.1 Calculations and sizing

The output of the driver was sized in that way, that the 7^{th}-harmonic frequency of the fundamental frequency (16MHz) can be provided. Due to the high peak current flowing through the resistor, we also need to check the reliability here. See chapter 5.2.

$$F_{0H7} = 16MHz \cdot 7 \approx 100MHz \tag{4.30}$$

$$F_g = F_{0H7} = \frac{1}{2 \cdot \pi \cdot R_{out} \cdot C_L} \tag{4.31}$$

$$R_{out} = \frac{1}{2 \cdot \pi \cdot F_{0H7} \cdot C_L} \approx 1k\Omega \tag{4.32}$$

$C_L = 20pF \ldots$ Load capacitor of the driver

$F_{0H7} \ldots$ 7^{th}-harmonic frequency

$F_g \ldots$ Cut-off frequency

$R_{out} \ldots$ Output resistance

4.4 Current bias cell

The current bias cell is amongst the least critical cells in the RC-oscillator. Its most important parameter related to frequency stability is the matching of currents in both comparators. A bad matching of currents leads to alterations in frequency and duty-cycle in cases where the current displays differential drift behavior. Since the current is directly linked to the delay of the comparator, a "well defined" current is necessary. The topology used was a typical bias-cell in weak-inversion. This topology

shows better process stability compared to the topology in current saturation.

$$I_D = I_{D,MN_{CM}} = I_{D,MN_{CM1}} \tag{4.33}$$

$$U_R = V_{gsMN_{CM}} - V_{gsMN_{CM1}} \tag{4.34}$$

$$I_D = I_{D0}\frac{W}{L}e^{\frac{V_{gsMXy}}{nV_T}} \tag{4.35}$$

$$V_{gsMN_{CM}} = \ln\left(\frac{I_D}{I_{D0}}\frac{L}{W}\right)nV_T \tag{4.36}$$

$$V_{gsMN_{CM1}} = \ln\left(\frac{I_D}{I_{D0}}\frac{L}{W\cdot N}\right)nV_T \tag{4.37}$$

$$V_{gsMN_{CM}} - V_{gsMN_{CM1}} = \left(\ln\left(\frac{I_D}{I_{D0}}\frac{L}{W}\right) - \ln\left(\frac{I_D}{I_{D0}}\frac{L}{W\cdot N}\right)\right)nV_T = U_R = I_D\cdot R \tag{4.38}$$

$$I_D = \frac{\ln(N)nV_T}{R} \tag{4.39}$$

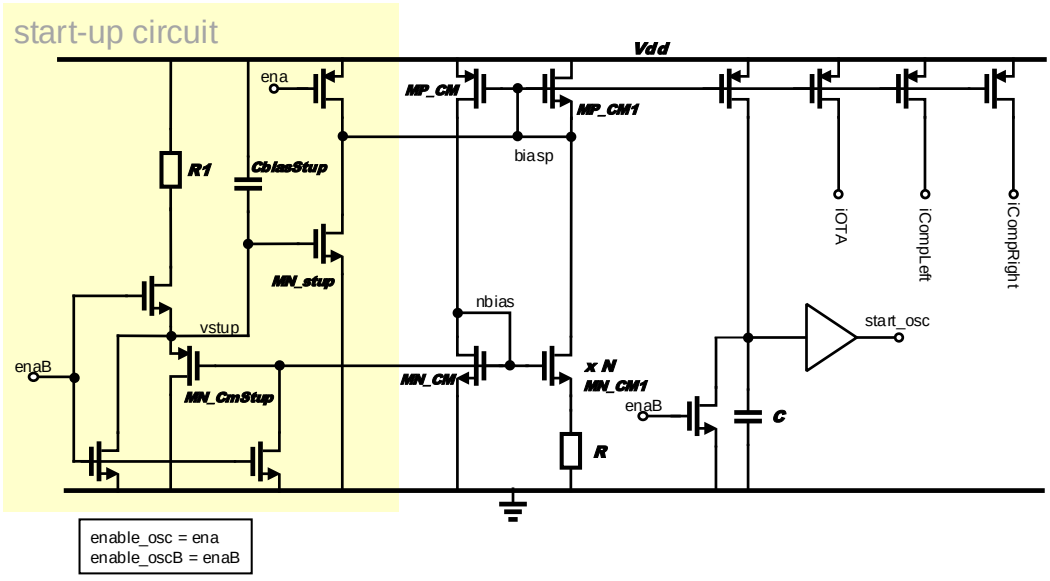

Figure 4-11: Topology of the current bias cell

As apparent from equation 4.39, the current is determined by the resistor. Knowing the strong process variation in resistors, it becomes clear that the NMOS current

mirror does not place very high demands on current matching. However, the PMOS current mirrors need to possess a much better current matching, so that the current difference between the comparators is kept to a minimum. Temperature compensation can therefore also be achieved through a series connection of two resistors with different temperature coefficients. In our case, a poly-resistor was connected in series with a nwell-resistor. **Note:** The nwell-resistor has high voltage dependency, which means it should be connected as close to ground as possible (nwell-resistor back bias dependence).

4.4.1 Start-up behavior

Generally, a start-up circuitry is necessary, since this circuitry has two operation points. The difficulty with this cell lies not in the design of the normal circuitry components, but in the design of the static and dynamic start-ups. First, we should differentiate between dynamic and static start-up behavior.

Static start-up behavior is defined as follows:

- Static supply voltage V_{dd}
- Sequence:
  1. $enable_{osc}$ rises ↑ from 0V to V_{dd}.
  2. *nbias* is first at a low potential when the enable signal goes to high
  3. *vstup* rises ↑ steeply to a high level because of the resistive load (R1)
  4. *biasp* to go down ↓
  5. Bias current starts to flow

Dynamic start-up behavior is defined as follows:

- Supply voltage rises ↑ from 0V to V_{dd} and $enable_{osc} = V_{dd}$
- $i_{CbiasStup} = C_{biasStup} \cdot \frac{\partial U_{C_{biasStup}}}{\partial t}$, so if $C_{biasStup}$ is larger, more current flows through $MN_{Cm,stup}$ in a short term, which leads to a higher *vstup* voltage because the parasitic capacitance can be charged faster.

- $MN_{Cm,stup}$ MOS is critical for the dynamic start-up. If $MN_{Cm,stup}$ is too weak, then $vstup$ is too high. This causes a current to flow through MN_{stup} constantly. If $MN_{Cm,stup}$ is too large, then $vstup$ is too low and this leads to a very low current flowing through the MOS MN_{stup}, $\Rightarrow$ so the start-up is very slow. Also $vstup$ can stick to ground due to leakage currents.

Other design considerations of the start-up include:

- The bias cell forms a control loop which can oscillate due to a wrong sizing of $C_{biasStup}$.

  Assume: V_{dd} rise and a current flows through $R1 \rightarrow C_{biasStup}$ pulls $vstup$ to a higher voltage $\rightarrow$ current flows through $MP_{Cm1} \rightarrow nbias$ goes up $\rightarrow$ current flows through $MN_{Cm} \rightarrow nbias$ increases $\rightarrow vstup$ decreases $\rightarrow biasp$ increases $\rightarrow$ current through MN_{Cm} decreases $\rightarrow nbias$ decreases $\rightarrow vstup$ increases $\rightarrow$ current through $MN_{Cm} \rightarrow$ oscillation.

  Therefore, the sizing of $C_{biasStup}$ is critical to ensure no oscillation.
- Oscillation of the current leads to oscillation in the comparator delay. This leads to temporary changes in frequency (periodic jitter).
- Power supply rejection ratio (PSRR).

  An excessive voltage ripple in V_{dd} directly influences the gate of MN_{stup}. Therefore, if the MN_{stup} is too large or the ripple too strong, current is discharged from the cell through this transistor. This could lead to a current modulation with the ripple frequency, which in turn worsens the jitter performance.

4.4.2 Signal $start_{osc}$

As mentioned previously in chapter 3.1, we need two start-up signals in order to ensure a safe start-up of the oscillator. The current bias cell produces the delayed start signal $start_{osc}$. This signal indicates that the bias current is correct and that the current settling phase is over. This ensures correct functioning of the comparator and the integrator. The chosen circuit design concept to generate the delayed $start_{osc}$

signal was a simple voltage level detection through a Schmitt-trigger. Through the charge of the capacitor C, we can deduce the state of the bias current from the total charge present in the capacitor. The Schmitt-trigger is necessary to avoid oscillation at the switching point.

4.5 Trim-circuit

A trim-circuit is an essential component of almost every integrated RC-oscillator. Trimming procedures of a chip, however, are also linked to unwanted test time and costs. Therefore, the requirement for a quick, linear and robust trimming process arises. A trim is necessary in RC-oscillators, because the timer-related building blocks are subjected to very large process fluctuations. In our design, we have the possibility of a trim of the charging resistor R, the charging capacitor C, or the reference voltage V_{ref}. However, not all of these possibilities are ideal for the system. A trim of the reference voltage is, firstly, non-linear, and secondly, it changes the operation points of the comparator and of the active filter. As a consequence, the process reliability of the functionality becomes dependent of the trim value. To circumvent this problem, we would need a rail-to-rail design in the comparator as well as a large output swing of the OTA. A trim of the charging resistor R would also be possible, but because the necessary switches should possess a minimal R_{on} value, the resulting voltage-dependent parasitic capacitance would be too large. A further disadvantage of this approach is the resulting change in peak current due to the trimming process. Because of these disadvantages, a trim procedure of binarily weighted capacitors is much more linear and easier to carry out. This is firstly more advantageous for linearity and power consumption because this values are not determined by the trim value [8]. To ensure linearity in the trimming process, another important step to consider is the scaling of the R_{on} of connected switches. Because less charge flows through smaller capacitors, the R_{on} in question can be larger than with larger capacitors. It therefore becomes apparent that the R_{on} of the switches should also be weighted binarily.

4.5.1 Design aspects

Depending on the desired precision and on the frequency behavior across temperatures, voltages etc., we can determine the suitable precision for the trim. Important parameters for the design of the trim-circuit include:

- Behavior of the curve to trim

- Trimming points (multi point or single point)
- Trimming voltage and temperature
- Symmetrical distribution of w.c. trim-corners around the target frequency
- Trim step (LSB)
- Trim range
- Safety margin of the trim range
- Number of trim bits necessary
- Topology of the trim-circuit
- Linearity of the trimming process
- Trade-off at the NMOS-switch: Leakage current at $V_{GS} = 0V$, parasitic capacitance and ΔR_{on} by $\Delta V_{GS} = \Delta V_{dd}$
- The LSB capacitor of $1.68fF$ is of the same order of capacitance as parasitic elements such as the wire-capacitance and the C_{jdb} capacitors
- Errors in monotony through switching of parasitic NMOS-capacitances (if NMOS is ON, C_{para} is shorted, otherwise switched in series to the capacitor)
- Errors in monotony through switching of parasitic wire-capacitances between NMOS and the capacitor (if NMOS is ON, C_{wire} is shorted, otherwise switched in series to the capacitor)
- Wire-capacitances between the poly-resistor and the capacitor do not contribute to monotony errors, because they constantly connected on the node
- Non-linearities in the characteristic trim line through the matching of trim capacitors. Matching is dependent on area, which means, that the matching of small trim capacitors is less good than that of larger trim capacitors.

To determine the largest possible trim steps capacitor C_{LSB}, the frequency behavior across voltages and temperatures must be known approximately. Under the assumption of an ideal oscillator without voltage or temperature dependency, and with a necessary frequency stability of $\pm 0.5\%$, a maximum trim step of 1% can be chosen in order to reach the required frequency band. It therefore becomes apparent that the largest trim step can equal, at most, the absolute precision requirement. In a real oscillator, however, there is also the possibility of drifting behavior across

temperatures or voltages. Because of this behavior, the trim step needs to be reduced so that despite this variation, a trim in the specified frequency band is possible. This means that the higher the variation because of the frequency drift, the smaller the trim step should be in order to remain within the frequency band. This, however, is only valid under the condition that the variation due to frequency drift is smaller than the maximum absolute precision requirement in the specifications.

4.5.2 Calculations and sizing

Through corner simulations, we can establish a frequency trim range, which establishes a capacitance value for the necessary trim-circuit. Another important factor is the minimum required width of one trim step. The smallest trim step is defined at $\approx 0.01\%$ of the variation in period time, because of the strong frequency drift behavior. Because the trim capacitors are subject to process variations, just like the charge capacitor C, we cannot determine a fixed trim step.

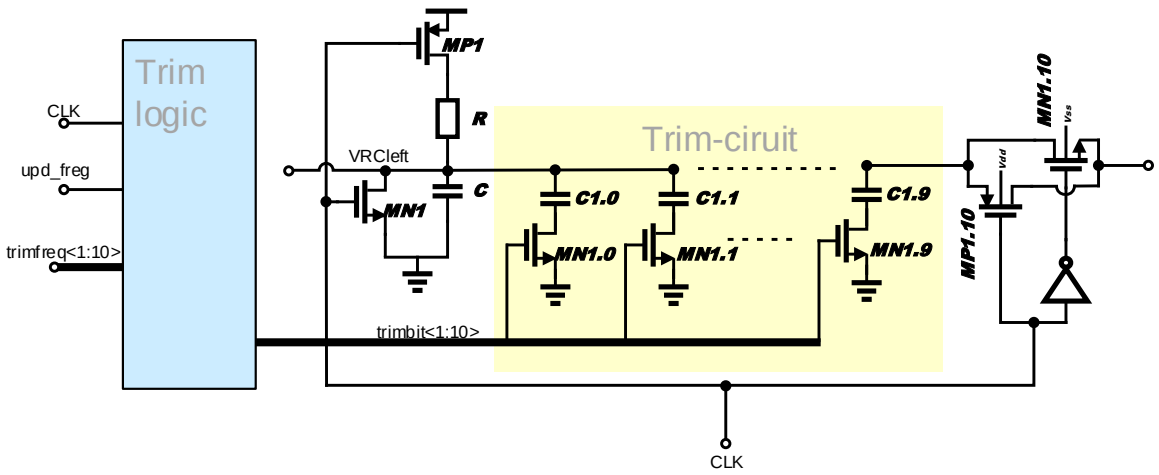

Figure 4-12: Trim-circuit

Trim range

Assumption: Only the R and C of the RC-cell vary and V_{ref} is constant. As noted in [39] and [4], the variation of R is $\pm 16\%$ and the variation of C is $\pm 4\%$. This means that the maximum period time variation respective to the target frequency F_0 is: $|(1 \pm 0.16) \cdot (1 \pm 0.04)| \approx |1 \pm 0.21| \rightarrow \pm 21\%$. From this result, we need to derive a trim-circuit with a trim range of at least $\pm 21\%$ possible period time variation. However, the simulation including extracted parasitics has shown that a much larger trim range is necessary, because monotony errors in the corners (Slow 1023) and (Fast 0) lead to large differences in capacitance.

Note:

- Slow 1023: All parasitic capacitances are short-circuited
- Fast 0: All parasitic capacitances are in parallel to the charge capacitor C

To lend additional robustness against process variation to the trim range, the w.c. trim limits ***Slow 1023*** and ***Fast 0*** should be sized symmetrically around the target frequency. This ensures that the safety-margin is laid out symmetrically around the target frequency.

$$C_{LSB} = 1.68fF \tag{4.40}$$

$$N = 10 \tag{4.41}$$

$$\Delta C(N) = C_{LSB} \cdot (2^0 + ... + 2^{N-1}) \tag{4.42}$$

$$\Delta C(N) = C_{LSB} \cdot \left(2^N - 1\right) = C_{LSB} \cdot 1023 = 1465.95fF \tag{4.43}$$

$$T(T_v) = 2R(C_0 + ((2^N - 1 - T_v) \cdot C_{LSB})) \cdot k \tag{4.44}$$

$$T(T_{default}) = 2R \cdot C(T_{default}) \cdot k = 62.5ns \tag{4.45}$$

C_{LSB} ... Smallest trim step capacitor

N ... Number of trim bits

$T(T_v)$ ... Period time T as function of the decimal trim number

T_v ... Decimal trim number {0 ... 1023}

$$k \ldots \frac{W\left(\frac{\frac{1}{e}}{(\alpha-1)}\right)(\alpha-1)-1}{(\alpha-1)}$$

The frequency variation due to a capacitance change follows an $\frac{1}{x}$ behavior. Thus, the percentage change for a positive or negative change in the capacitance is not the same. The evaluation of the necessary number of trim bits was done by simulation. This was necessary because of the unknown parasitic capacitances.

Spike-free trimming

Spike-free trimming is necessary because in the case of unwanted spikes in the CLK-signal, system failures can happen. A special circuit block was therefore developed. This drastically reduces the probability of spikes occurring during the trimming process. Spike-free trimming can take place in two operating modes:

- upd_{freq}= High

  In this operating mode, an incoming change in a trim bit is immediately transmitted to the oscillator. The trim-circuit carries out the trimming process while taking into account the spike-free trimming. However, in this operating mode, a small probability of a possible spike in the CLK-signal remains.

- upd_{freq}=Low to High

  This operating mode guarantees an absolutely spike-free change in frequency. Through a low-signal at the upd_{freq}, trim bits can be put in place without a simultaneous change in frequency. Only when the upd_{freq} signal is set to high, a frequency change takes place in the next one or two CLK-cycles (depending on the setup-time at flip-flip).

4.6 RC-delay-cell

The RC-cell is the cell which controls the period time in the oscillator. It creates an RC-delay which is used to produce oscillation between the two comparators. The following points are important for the design of the RC-delay-cell:

- The PVT dependence of the charging capacitor C
- The PVT dependence of the charging resistor R
- The PVT dependence of the R_{on} of the PMOS switching transistor
- The PVT dependence of the parasitic input capacitance of the comparator
- The PVT dependence of the parasitic drain capacitance of the discharging NMOS
- Leakage current through the switched-off discharging NMOS
- Leakage current through the switched-off transmission gate (TMG)
- The PVT dependence of the input capacitance of the transmission gate
- Charge injection due to the switching operation
- Influence of the active filter, if the chosen resistor R_{int} is too small
- The PVT dependence of the TMG $R_{on,TMG}$, along with the parasitic capacitance of the integrator resistance, cause a voltage drop of $R_{on,TMG} \cdot C_{para} \frac{\partial UC_{para}}{\partial t}$ at the voltage to be integrated (this leads to a strong voltage dependence in the frequency)
- The unwanted spread of the first and second order temperature coefficients of the poly-resistor
- The mismatch of the RC-products
- The PVT dependence of the trim network

The problem with the production of an exact and temperature stable RC-product is, for one, the large variation of the absolute values of the passive components R and C. Due to process variations, the doping concentrations in the poly-resistor are different. Doping effects on the thermal behavior of a silicon resistor are based on the hole mobility. The two thermal coefficients of the resistor are strongly dependent on doping concentration. The first-order coefficient shows a parabolic behavior with

a minimal value for a particular doping concentration. The second-order coefficient decreases monotonously in accordance with doping concentration, until it reaches zero. So there is a trade-off between the second-order coefficient and the first-order coefficient depending on doping concentration [1].

4.6.1 Design aspects of the RC-cell

As explained in the chapter 3.4, we use a fringe capacitor and a poly-resistor as the charging capacitor and the charging resistor, respectively. When choosing the ratio of R to C, there was a trade-off between power consumption and voltage and temperature dependence. The next important circuit element in this cell is the PMOS charging transistor MP_1 , see figure 3-1. To minimize the error due to the R_{on} of the PMOS charging transistor, the PMOS switch was sized so that he influences the total charging resistor R only per (0.05%) over all PVT variations. On the other hand, the NMOS discharging transistor is easy to dimension, because the discharging curve is irrelevant to the integration. The only possible sources of error are a dimensioning that is too large due to a higher voltage-dependent capacitance, and a dimensioning that is too small, which would prevent a full discharging of the charge capacitor. For the full discharging of the capacitor by the NMOS discharging transistor, we assumed $\tau = R_{onNmos} \cdot C$. This means, for a charging capacitor C of $C = 1.5pF$, the discharging resistor R_{onNmos} has equal to:

$$10 \cdot \tau < \frac{T}{2} \tag{4.46}$$

$$10 \cdot \tau = 10 \cdot R_{onNmos} \cdot 1.5pF \tag{4.47}$$

$$10 \cdot R_{onNmos} \cdot 1.5pF < \frac{T}{2} \tag{4.48}$$

$$R_{onNmos} < \frac{62.5n}{2} \frac{1}{1.5pF \cdot 10} \approx 2k\Omega \tag{4.49}$$

$\tau \ldots$ RC-product $\tau = R_{onNmos} \cdot C$

$T \ldots$ Period time of oscillation

$R_{onNmos} \ldots R_{on}$ of the discharging NMOS MN_1 or MN_2

4.7 Resistive voltage divider

Just like the RC-delay-cell, this cell is critical, because every change in reference voltage results in a change in frequency.

The most critical points surrounding the resistive voltage divider include:

- Unwanted spread of the temperature behavior of the reference voltage V_{ref}
- Unwanted leakage current through the switched-off transmission gate in the resistive voltage divider
- PVT dependence of ΔR_{on} between P/NMOS due to a mismatch

4.7.1 Start-up behavior of the reference voltage

The reference voltage was set to $0.55 \cdot V_{dda}$ instead of $0.535 \cdot V_{dda}$ for reasons relating to the layout. For further information see chapter 3.8.1 "Sensitivity of T to α". In the current test chip design, there is a choice between two reference voltage temperature coefficients ($0\frac{\mu V}{K}$) and ($13\frac{\mu V}{K}$). This allows on the one hand, to determine the overall circuit temperature coefficient, and on the other hand, the compensation for the linear frequency behavior across temperature. The temperature compensation was carried out using poly-resistors with different widths. Further details concerning design aspects can be found in the following literature [1] [38] [57] [18].

Chapter 5

Reliability

5.1 Charging resistor R

Because of the high peak currents, the reliability of the charging resistor R should also be considered. For reasons of matching and reliability, we used a resistor array for the charging resistors. Width of the charge poly-resistor R: $W = 0.2\mu m$.

5.1.1 Unsilicided polysilicon

The maximum equivalent current is proportional to the width W of the resistor. In unsilicided polysilicon, the maximum current is determined by joule heating and independent of temperature. Thus, the required lifetime of $\sqrt{\frac{10}{t_{life}}}$ does not apply to polysilicon [41]!
Simulation result gives at $-40°C$, fast, $1.9V$ a peak current of $I_{peakR} = \frac{Umax}{R_{min}} \approx 115\mu A$. With the equation $1\frac{mA}{\mu m} \cdot W$ the minimum width for a given current can be calculated [41].

$$1\frac{mA}{\mu m} \cdot W \quad = \quad 0.115mA \tag{5.1}$$

Thus, a minimum width of $115\mu m$ has to be chosen for a reliable design. The chosen is width $0.2\mu m$. This means there is a safety margin of about 58%.

5.2 CLK output driver

Due to the high peak current flowing through the poly-resistor, we also need to check the reliability here. $I_{peakR} = \frac{Umax}{R_{min}} = \frac{1.9V}{860\Omega} \approx 2.2mA$. Assume an average current of $0.5mA$ and a life time of about $t_{life} = 1$ year.

5.2.1 Contacts

The maximum equivalent current per contact is $0.09\frac{mA}{contact}$. Thus, the minimum number of contact in the high current line can be determined as follows.

$$0.09\frac{mA}{contact} \cdot \sqrt{\frac{10y}{1y}} \approx 0.3\frac{mA}{contact} \tag{5.2}$$

$$0.3\frac{mA}{contact} \cdot N_c = 0.5mA \tag{5.3}$$

$\longrightarrow N_c = 1.6$, therefore at least two contacts have to be chosen for a reliable design.

5.2.2 VIAx on METALxS

The maximum equivalent current per VIAx is $0.08\frac{mA}{VIAx}$. Thus, the minimum number of VIAx in the high current line can be determined as follows.

$$0.08\frac{mA}{VIAx} \cdot \sqrt{\frac{10y}{1y}} \approx 0.27\frac{mA}{VIAx} \tag{5.4}$$

$$0.27\frac{mA}{VIAx} \cdot N_v = 0.5mA \tag{5.5}$$

$\longrightarrow N_v = 1.8$, therefore at least two VIAxs have to be chosen for a reliable design.

5.2.3 METALxS

Maximum current in METALxS can be determined as follows. $i_{METALxSmax} = 0.65\frac{mA}{\mu m} \cdot (W - 0.02) \approx 0.65\frac{mA}{\mu m} \cdot W$. Thus, the minimum width of METALxS in

the high current line can be determined as follows.

$$0.65\frac{mA}{\mu m} \cdot W \cdot \sqrt{\frac{10y}{1y}} \quad = \quad 0.5mA \tag{5.6}$$

$\longrightarrow W = 0.23\mu m$, therefore a minimum width W of $0.23\mu m$ has to be chosen for a reliable design.

5.2.4 Unsilicided polysilicon

See also chapter 5.1.1.

$$0.5\frac{mA}{\mu m} \cdot W \cdot \quad = \quad 0.5mA \tag{5.7}$$

Thus a minimum width of $0.5\mu m$ has to be chosen for a reliable design.

5.3 Electromigration

Electromigration refers to the gradual displacement of the metal atoms of a conductor as a result of the momentum exchange between the flowing electrons and the metal atoms. Because of the mass transport of metal atoms from one point to another, electromigration leads to the formation of voids at some points in the metal line and hillocks or extrusions at other points. It can therefore result in either an open circuit if the void formed in the metal line becomes big enough, or a short circuit if the extrusions become long enough to serve as a bridge between the affected metals. Electromigration is accelerated by temperature and current density. Due to the reasons mentioned above, the current paths were examined for their failure safety. For further information see 5.1 and 5.2.

Chapter 6

Simulation results

A drawback of this RC-oscillator is the spread of the frequency due to the spread in temperature coefficients, offset voltages and offset voltage drifts. To determine the performance of the trimmed oscillator a test bench with a trim procedure is necessary. Therefore, the test bench should imitate process variation and the trim procedure to $16MHz$. After the determination of the trim value, a characterization run can be started to verify the voltage and temperature behavior of the oscillator. The implementation of the test bench was done with OCEAN. In other words, the OCEAN-script controlled test bench evaluates the mean value and the spread of the frequency error in percent over process, voltage and temperature variations.

6.1 Characterization over PVT, OCEAN-script

A preliminary approximation of the frequency spread via a simplified MATLAB ® model was discussed in chapter 3.4. A much more accurate simulation was carried out via an automatized OCEAN-script, which includes the real trimming process of a test machine.

Some important design aspects of the simulation test bench include:

- Reproduceability (OCEAN-script)
- Computation effort (verification time)

- Necessary memory
- Number of simulations (network traffic)
- The resolution of design parameters and the simulation error involved (design parameters such as temperature, voltages, currents...)
- Simulation time (possible settling behavior)
- Convergence aids to shorten possible settling behavior
- Time resolution and computation accuracy of the transient simulation
- Results of the simulation: Statistical error verification, clear representation of error
- Real-life validity: Errors caused by the testing machine (limited measuring time, frequency settling etc.)
- Structure of the OCEAN-script
- Trim routine: Best-guess, linear-approximation
- Testing conditions: Room temperature, nominal supply voltage...

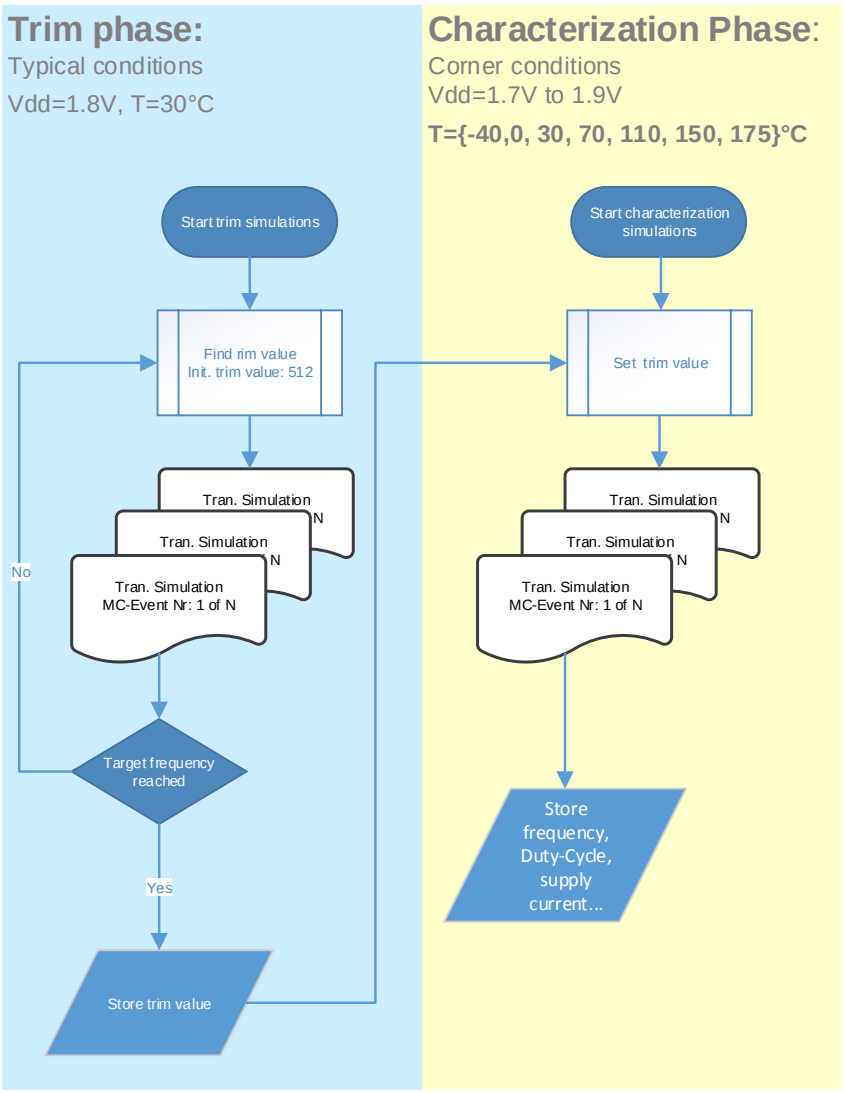

Figure 6-1: Simplified OCEAN simulation sequence

The number of simulations and the computation effort and memory involved cannot be neglected when it comes to automatized simulation scripts. For this reason, a trade-off has to be created between the simulation error and the computation effort. In order to reduce the number of simulations, simulations only take place across a limited range of temperatures and voltages. As such, a small error is added to the error, because it is not possible to always capture the maximum of the frequency error through a simulation. In order to keep this error minimal, the frequency variation across temperatures must be known. The minimum frequency extreme occurs at $-40°C$ or at $175°C$, depending on the linear and the quadratic temperature coefficient of the RC-product. The maximum frequency extreme is much more difficult to predict with accuracy. Depending on linear and quadratic temperature coefficients, maximum frequency extremes can be expected to occur between $60°C$ and $175°C$. However, we can expect a flat maximum between $60°C$ and $90°C$. Therefore, a temperature set of $-40°C$, $0°C$ $30°C$, $70°C$, $110°C$, $150°C$, $175°C$ was chosen. This matches the actual frequency extreme with an accuracy of $\pm 0.025\%$. Another important point is simulation time. To achieve minimal simulation time, several voltage nodes were forced into their correct steady state at the beginning of the transient analysis. However, also a simulation time has to be specified in order to allow a leftover frequency settling behavior. By simulation through the process corners, a simulation time of $40 - 50\mu s$ was verified, which means a frequency error through settling of 0.001%. As the end result, the standard deviation and the mean of the frequency error were calculated for each combination of design variables. From these results, we can draw an enveloping curve, from which a maximum variation can be deduced, see figure 6-2. An important point is that changing design variables such as temperature, current and voltage of an ideal source does not change the mismatch parameters of the Monte-Carlo analysis [54]. Using the OCEAN-script, the following specification parameters were verified across temperature and voltage variation:

- Minimum and maximum frequency deviation
- Minimum, maximum and average power consumption
- Minimum, maximum and average duty-cycle variation

- Voltage dependence of the frequency
- Temperature dependence of the frequency
- Field trim precision (max. ΔF over the temperature + $\frac{1}{2}LSB$)

6.2 Functional analysis

In order to ensure the functionality of the oscillator with external wiring, a functional analysis of the entire test chip during normal operation was carried out.

6.3 Aging and reliability analysis

As mentioned before, due to time effects, the frequency changes across the lifetime of the oscillator.

Time-related frequency changing mechanisms include:

- Jitter
- Aging effects of the active and passive building blocks

Jitter occurs immediately and periodically within a very short time window, deterministically or randomly. Therefore, jitter can include a periodical and deterministic and a random component. In contrast, a long-term change in frequency can be attributed to the aging of active and passive building blocks. In those cases the reliability limitations of a device must be taken into account and lifetime models should be used to determine if an application has a reliability risk. This especially applies to NBTI and PBTI degradation of N/PMOS transistors, which is the dominant failure mechanism of these devices. For further information about NBTI see chapter 3.2.1.

NBTI stress condition of a PMOS is:

- High temperature $175°C$
- $V_{gs} = 0V$ therefore $V_{ds} \approx 0V$

- V_{bs} has a negligible influence

The negative bias instability NBTI of a PMOS transistor is more relevant than the PBTI of NMOS. The aging of MOS transistors is a non-negligible issue for reference oscillators. In our design, the offset voltage of the OTA has an influence on the frequency. Due to aging, the transistors in the ***systematic*** offset vary over the lifetime. However, if the gain is high enough, the amplifier will minimize this issue. The ***random*** offset of the OTA will not change from the time of production until the end of the lifetime (because the same aging effect will occur to transistors). Compared to other oscillator topologies, aging is much better because the oscillator uses passive devices for the oscillation so that its accuracy lasts until the end of its lifetime. **Remark:** Ring or IC oscillator suffer over their lifetime because they hardly depend on the transistor parameters.

The reliability simulation was done with PRESTO. PRESTO is a reliability simulation tool which was developed from NXP-Semiconductor. PRESTO is implemented as a shell around an analog simulator. It allows the user to run a reliability simulation based on an existing transient simulation setup with a single command. With Circuit-Level reliability simulation, it is important to consider the conditions of the circuit stress. For our particular case, we used a situation where we apply a high temperature of $175°C$ and a high supply voltage of $1.9V$ to the circuit for an extended period (1 year), while the oscillator runs on its oscillation frequency. This would be a reasonable setup to replay a HTOL (High Temperature Operating Life) experiment.

Result: 0.027% **over 1 year stress (life time)**

6.4 Total frequency error

The total error E_{Ftot} includes the following:

$$E_{Ftot} = E_{ResultSim} + E_{TestM} + E_{DueSim} + E_{Aging} \tag{6.1}$$

$$E_{Ftot} = \pm 1.6\% + E_{TestM} + 0.001\% + 0.025\% + 0.27\% \tag{6.2}$$

$$E_{Ftot} \approx \pm 1.65\% + E_{TestM} \tag{6.3}$$

$E_{ResultSim}$ ... is the verified error due to the simulation. This error include $E_{\frac{1}{2}LSB}$

E_{TestM} ... is the error due to the testing machine during the testing procedure

E_{DueSim} ... is the error due to the limited resolution of the design parameters and limited setting time

E_{Aging} ... is the error due to aging across the oscillators lifetime.

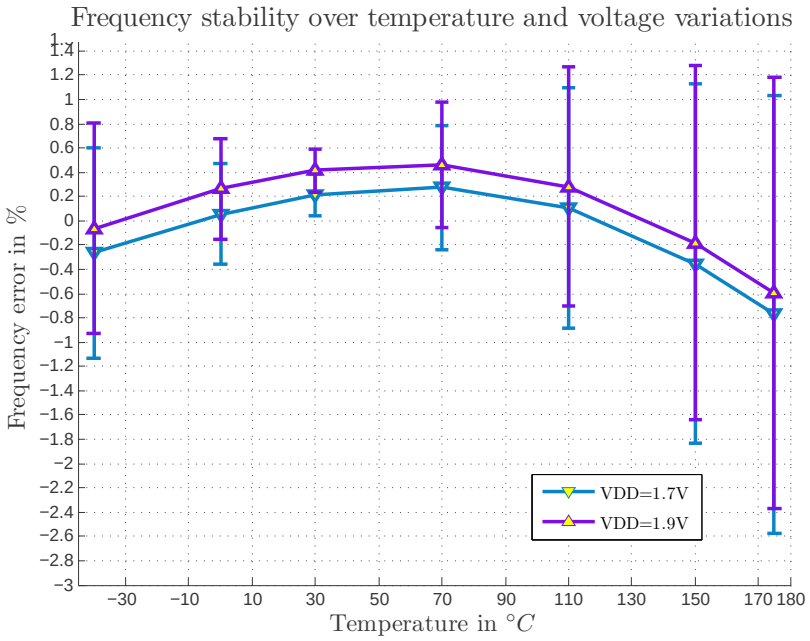

Figure 6-2: Oscillator $\pm 6\sigma$ frequency stability over PVT variations

Note: The frequency error can be shifted to $\pm 1.65\%$ due to a shift of the trim frequency ($+0.25\%$). Trim frequency used for figure 6-2 was 16.0506MHz.

Chapter 7

Conclusion

An oscillator was developed for a high frequency accuracy over PVT variations. The oscillator presented was tested for its stability against PVT variations and aging using Monte-Carlo, corner and aging simulations. Through optimization steps, certain results are comparable to those in the paper [63]. However, these results are irrelevant in terms of suitability for mass production. The oscillator has an area of $0.08mm^2$ and its power usage lies between $180\mu A$ and 220μA. The supply voltage and temperature range between $1.7V - 1.9V$ and $-40°C$ and $150°C$ respectively. Under these conditions, and using a $\pm 6 \cdot \sigma$ range, we can specify a maximum frequency stability of $\approx \pm 1.65\%$. To verify the frequency stability across temperatures and supply voltage, an OCEAN-script, which simulates a real trimming process and then provides a characterization across temperatures and supply voltage, was implemented. This allowed for a simulation of statistical analysis of process variations in a trimmed oscillator. The results of this simulation showed that the spread of the temperature coefficient of the charging resistor and the temperature coefficient of the second degree were the limiting factors. Due to this strong spread of the temperature coefficient, an implementation of this spread in the simulation models is absolutely necessary in characterization stimulation. Otherwise, no conclusion about the real performance can be drawn. Furthermore, frequency stabilities below $\pm 0.5\%$ are very difficult to reach because the spread of the temperature coefficient would need to be compensated for. Such a compensation using conventional approaches

would, amongst other things, raise the voltage dependence of the circuit. A possible solution could be trimming the temperature coefficient of the circuit. However, in terms of mass production suitability, this solution is not useable due to enormous testing costs. The advantage of the RC-oscillator presented here is that the time constant of the oscillator is determined by passive components R and C. This makes the oscillator much more robust against to aging when compared to, for instance, ring oscillators, which are based on transistor parameters. A full immunity toward voltage variation cannot be confirmed. This voltage immunity is hard to realize due to parasitic capacitances of the comparator and the voltage dependent R_{on} of the trimmed network. As mentioned in chapter 2.6, a comparison to other published oscillators is difficult, because there is generally no information about models used in the simulation, standard deviations etc. in these publications. Furthermore, an extracted simulation showed that the parasitic capacitances between the drain and the trim capacitors reduce the trimming range drastically. Therefore, the trimming range needs to be enlarged later on. The published version of the oscillator [63] posits a low-power oscillator with a minimal area. These characteristics could only partly be confirmed in our design. Using a robust $\pm 6 \cdot \sigma$ design for the oscillator that is also suitable for mass production, minimal area and low power can only partly be reached.

This is due to the following trade-offs:

- A larger charging resistor causes the charging capacitor to be smaller at a given frequency. Therefore, the proportion of parasitic capacitance to charging capacitors becomes small, and a larger voltage and temperature dependence of the circuit ensues. Therefore, a smaller resistor and a larger charging capacitor need to be chosen, which causes a rise in power consumption and area.
- Because of the small charging resistor, the PMOS R_{on} of the RC-charging path needs to remain negligibly small across all corners. Therefore, the PMOS needs to be large and the related NANDs needs to be strong, as the driver of the gate. This again contradicts a low power consumption and minimal area usage.

- Because of the large tolerances of the passive building blocks R and C, a large trimming range is necessary. This means a larger area.
- Ripple dependency of the supply voltage: Because the concept of the oscillator is based on the mean calculation of the charge, the supply voltage needs to be buffered with enough capacitance to keep the voltage ripple small.
- Because of the kick-back noise of the comparator, the threshold of the comparator needs to be buffered. This leads to a larger area due to the additional buffer capacitor.

Despite this, using this design, a good reduction in the influence of temperature and voltage can be obtained, because of the excellent compensation for the comparator delay. A test chip was produced in a $0.14\mu m$ ABCD9-Power SOI-CMOS-Process. Unfortunately, the performance results of the test chip regarding jitter, temperature and voltage dependence are still missing. Considering the verified results, the challenge remains to stay under a $\pm 6 \cdot \sigma$ limit of $\pm 0.5\%$ frequency deviation across a large voltage and temperature range.

Table 7.1: Oscillator simulation results and features

Specification	Data
Principle of operation	RC-Relaxation with feedback
Frequency range in MHz	16
Supply voltage in Volt	1.7 to 1.9
Temperature range in °C	-40 to 150, up to 175 functional behavior
Supply current in μA	180 to 220
Process	0.14μm SOI ABCD9-Power
Accuracy in %	-1.3 to $+1.8$ over $\pm 6\sigma$, PVT-Variations and trimmed at 16.0506MHz ± 1.65 see note figure 6-2
Area in mm^2	0.08
Power-down mode	yes
Duty-cycle in %	51 to 49
0.1% Settling time in μs	$180\mu s$
Settling behavior	spike free
Trim	yes
Trim behavior	spike free
Clock output	Enable/disable possibility, spike free
Start-up behavior	From a low frequency with no frequency overshoot higher than $16MHz + 5\%$
Number of samples reported	Simulation TCR spread considered
FOM	86

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