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Feasibility Study of a Cross Cell Measurement System in a Standard CMOS Process

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Graz, October 2017

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Abstract

To maximize the performance of battery cells in a system, they are typically operated close to their *save operating area* (SOA) limits. This raises the need for comprehensive monitoring systems to prevent damage of the cells and in turn the system and therefore battery monitoring systems have to be employed to be able to safely use high power density cell technologies like Li-Ion.

The goal of this thesis was to develop a suitable input stage, to be used in a cell voltage monitoring system as part of a battery management system. This thesis demonstrates that cell voltage monitoring systems can be implemented in a low cost 130 nm CMOS process and that there is no need to design in far more expensive processes as *bipolar CMOS DMOS* (BCD) or *silicon on isolator* (SOI).
The developed systems use the cross cell measurement approach and therefore have to have an input range outside the supply rails of the monitoring IC. Current publications in this field, only present methods to monitor multiple cells above circuit ground and are often of limited accuracy.

In this thesis multiple multiplexed and synchronous sampling systems have been developed and discussed. They can be employed based on system requirements.
Additionally a novel approach for an input stage is presented in this thesis. The design is based on a switched capacitor divider and is very flexible in terms of gain and number of channels. It is also independent of bias currents and voltages and does not use an amplifier and is therefore simpler to design and more robust against stability problems. Due to the reduction in complexity, the sources of errors and faults have been reduced as well, which enables the development of a more accurate system.
All of the designs have been designed with respect to manufacturability and have been optimized in terms of area and therefore cost. The presented designs are able to operate with low supply voltages and compared to previous designs, the power consumption has been reduced drastically.

Keywords: cell voltage monitoring, BMS, analog circuits, CMOS, switched capacitor circuits, class AB amplifier

Kurzfassung

Um die Leistung von Batteriezellen in einem System zu maximieren, werden diese typischerweise in der Nähe ihrer *save operating area* (SOA) Grenzwerte betrieben. Um eine Beschädigung der Zellen und des Systems zu vermeiden und um Zelltechnologien mit hoher Leistungsdichte, wie Li-Ionen einsetzen zu können, müssen somit Batterieüberwachungssysteme eingesetzt werden.

Ziel dieser Arbeit war es, eine geeignete Eingangsstufe zu entwickeln, welche in einem Zellenspannungsüberwachungssystem als Teil eines Batteriemanagementsystems eingesetzt wird. Diese Arbeit zeigt, dass Zellenspannungsüberwachungssysteme in einem kostengünstigen $130\,nm$ CMOS-Prozess implementiert werden können und dass es keine Notwendigkeit gibt, weitaus teurere Prozesse wie *bipolar CMOS DMOS* (BCD) oder *silicon on isolator* (SOI) zu nutzen.
Die entwickelten Systeme nutzen das Cross Cell Measurement Verfahren und müssen daher einen zulässigen Eingangsspannungsbereich außerhalb der Versorgungsspannung des Überwachungs-ICs besitzen. Aktuelle Publikationen in diesem Bereich demonstrieren Systeme, welche mehrere Zellen überwachen. Der Eingangsspannungsbereich ist jedoch auf positive Spannungen eingeschränkt und die vorgestellten Systeme besitzen oft nur eine unzureichende Genauigkeit.

In dieser Arbeit werden mehrere gemultiplexte und synchrone System erarbeitet und vorgestellt. Diese können entsprechend den Systemanforderungen ausgewählt und eingesetzt werden. Des Weiteren wird in dieser Arbeit ein neuartiger Ansatz für eine Eingangsstufe vorgestellt, welcher auf einem kapazitiven Teiler basiert. Das vorgestellte System ist sehr flexibel in Bezug auf Verstärkung und Anzahl der Kanäle. Es ist unabhängig von Referenzströmen und -spannungen. Es nutzt keinen Verstärker und ist somit robust gegen Stabilitätsprobleme. Durch die Verringerung der Komplexität werden auch die möglichen Fehlerquellen reduziert und somit eine höhere Genauigkeit des Systems ermöglicht.
Alle vorgestellten Lösungen wurden mit Rücksicht auf die Herstellbarkeit entworfen und sowohl flächen- als auch kostenoptimiert. Die vorgestellten Systeme benötigen nur niedrige Versorgungsspannungen und im Vergleich zu bereits publizierten Systemen konnte der Leistungsverbrauch drastisch reduziert werden.

Stichwörter: cell voltage monitoring, BMS, analog circuits, CMOS, switched capacitor circuits, class AB amplifier

Contents

Chapter 1

Introduction

1.1 Motivation

The *save operating area* (SOA) of any battery cell is mainly defined by three parameters: voltage, current and temperature. Any violation of the acceptable limits of these parameters can cause a decrease in lifetime, lead to damage of the cell or in the worst case lead to an uncontrolled state of the system.
The most popular type of cell technology are Li-Ion cells, due to their high power density. Unfortunately, Li-Ion cells are especially vulnerable to violations of the SOA. Therefore comprehensive cell monitoring functions are needed to ensure a reliable system.

A system whose main task is to monitor and manage a cell or cell stack is called *battery management system* (BMS) and typically contains cell measurement, cell management and analysis functions [1], as shown in figure 1.1.1. Data logging and communication are also important parts of a BMS for interaction with external systems.

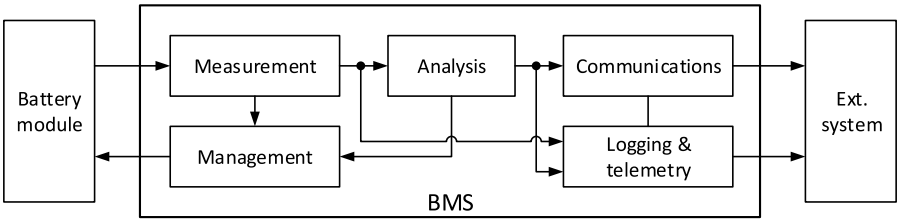


Figure 1.1.1: Typical BMS functions [1].

The overall goal of a BMS is to maximize performance of the cell. This leads to the requirement that the cell is used close to its operating limits. To do so, cell monitoring has to be employed, to protect the cell and in consequence the system from safety risks. More advanced BMSs are often able to estimate the life time and performance of the cell, by determining the *state of health* (SOH) and *state of charge* (SOC) of the cell.

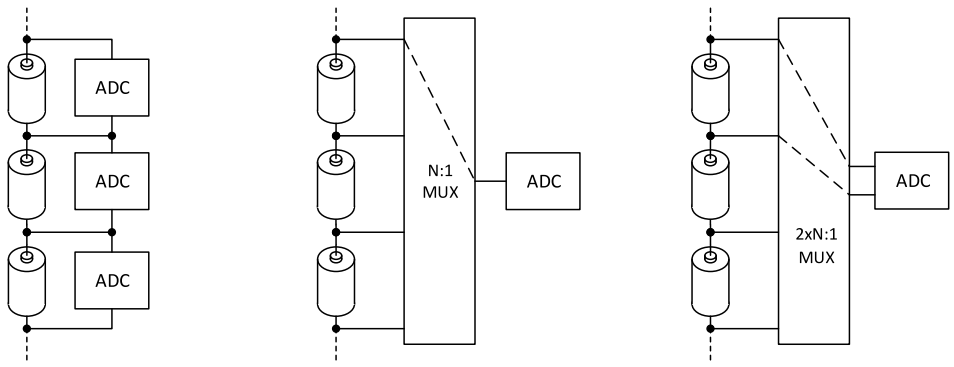
The focus of this thesis is to develop a cell voltage monitoring system in a standard $130\,nm$ CMOS process [5], as part of a BMS.
The system this BMS will be employed in, uses a large series connection of cells to form a high voltage cell stack. Because of the series connection and the large number of cells, these types of cell stacks are prone to unbalanced charging and discharging [1]. Every cell in the stack will therefore be monitored and controlled by a local BMS.

Chapter 2

Preliminary Considerations

2.1 Cell Voltage Measurement

Cell voltage measurement methods can be categorized into three types [1], as shown in figure 2.1.1.



(a) discrete

(b) single-end multiplexed

(c) differential multiplexed

Figure 2.1.1: Different cell voltage measurement methods [1].

Discrete

The discrete approach (a) uses one ADC for each monitored cell. This offers the benefit of a synchronous measurement of all cell voltages. On the downside the approach uses many ADCs which have to be matched. This would be difficult to accomplish for separate ICs. The approach is also more cost intensive due to the large number of ADCs and the required die area. One benefit of the design is, that the ADC does not need to handle higher voltages than one cell voltage.

Single-End Multiplexed

The single-end multiplexed approach (b) uses only one ADC to monitor multiple cell voltages indirectly. The respective cell voltage has then to be determined by calculation from the different measurement results. This leads to the requirement that the ADC needs to have a higher resolution to achieve the same accuracy as in the discrete approach. The design uses a multiplexer to select one tap in the series connection of the battery cells. The reference for the cell voltage

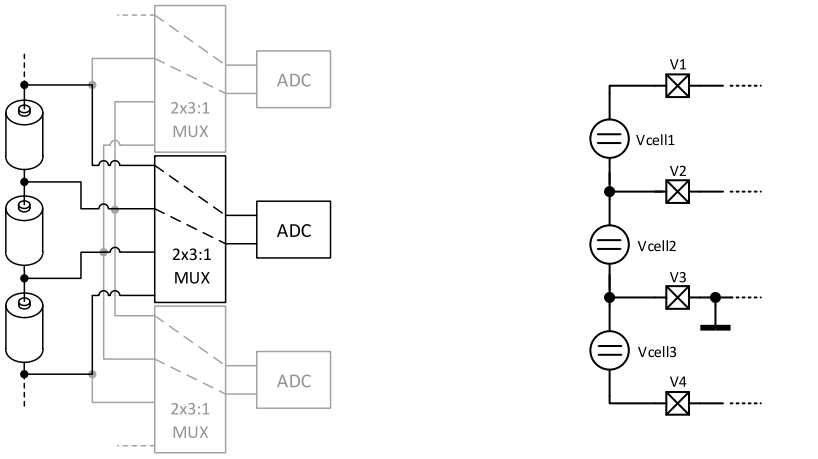
measurement is always the first tap in the series connection. For this design, the multiplexer and the ADC have to withstand input voltages equal to the voltage of the whole battery stack.

Differential Multiplexed

The differential multiplexed approach (c) uses almost the same approach as the single-ended one, with the difference that for this design the voltage is measured across each cell. This offers the benefit of increased accuracy, because in contrast to the single-ended design, the ADC only experiences input voltages of up to one cell voltage.

For this thesis the discrete approach has been chosen as the basis of the design for a cell voltage measurement system in a BMS. Because the developed system has to comply with the automotive safety standard ISO 26262, a short description of the design procedure with respect to functional safety is given.

The safety standard defines different safety levels for systems, based on the required failure rates. The highest level in this classification is the so called ASIL D standard. To design a system with a rating of ASIL D, all subsystems have to be either ASIL D as well or some other approach has to be taken.
The standard defines a procedure to reduce the required safety standard for subsystems by applying decomposition to a subsystem. Decomposition is the process of splitting the subsystem into parts, which in itself do not reach the required safety goal, but the combination of the parts complies with the safety standard. The described process was used to simplify the development of the cell voltage measurement system.



(a) Simplified overview.

(b) Local ground connection and voltage naming convention.

Figure 2.1.2: Cross cell measurement topology.

The result of the decomposition is presented in [7] and depicted in figure 2.1.2.(a). By monitoring not only the cell voltage of the cell the local BMS is managing, but also the voltage of the adjacent cells, the cell voltage monitoring becomes a redundant system. Because of this the cell voltage measurement in itself has to comply only with a lower safety standard and can be designed simpler, cheaper and with fewer development time. The topology has been named "cross cell measurement" in [7] and associated with it is the need for extending the input voltage range above and below the supply voltage.

All approaches have in common that an additional attenuator may be needed in front of the ADC to increase the input range, depending on the voltage of the monitored cell type and the full scale range of the ADC.

2.1.1 Distributed and Non Distributed Topologies

The presented voltage measurement systems can be classified as distributed and non distributed topologies [1]. Where distributed refers to the fact that each cell is monitored by a separate device placed directly at the cell. Such a system needs some kind of master that controls the distributed devices and handles the communication with the top level systems.
When a device is monitoring multiple cells at once it can be referred to as non distributed. This classification does not exclude the possibility that the system is modularized and cells form groups, each with a separate monitoring device.

In the following section a brief comparison of the topologies is made and some of the key differences are presented.

Cost

Distributed topologies are generally more cost intensive because more electronic components are needed. They are typically directly mounted onto the cell and do not need any additional connections, not considering wired communication. The installation cost of non distributed topologies is on the other hand higher because multiple connections to one system have to be made.

Reliability

Multiple connections have to be made to a non distributed topology. This leads to an increase in possible failure modes for a single system. Additionally the risk of a short is increased due to the possibility of a wiring fault.

Accuracy

The direct connection of a non distributed topology enables higher accuracy due to the short connection.

2.2 Concept

2.2.1 Requirements

To design the system that realizes the presented cross cell measurement system, the system requirements have to be defined first.

The first important requirement is the measurement accuracy. The cell voltage monitoring has to be able to accurately measure the cell voltage of the cells which it is monitoring with an absolute accuracy of $\pm 15\,mV$. This includes errors introduced in the input stage, the ADC and the reference of the system. To leave most of the error margin to the highly critical reference, the input stage has been designed with much tighter error tolerances.

To define the required input voltage range of the measurement system, different factors have to

be taken into consideration. The voltage range of a single cell is depicted in figure 2.2.1. The nominal operating range of the cell voltage is between $2\,V$ and $5\,V$. In this range the system has to be able to perform with the required accuracy. To enable fault and short detection of the cell, the input range is extended down, close to $0\,V$. The range extension is obviously only possible for secondary cells and not for the main cell suppling the system.

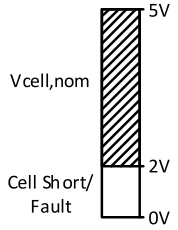


Figure 2.2.1: Channel input voltage range.

The cell stack is organized in such a way that multiple cells are directly connected via short low impedance connectors to form a cell module. The connections between different cell modules are then made with *high voltage* (HV) cables, as depicted in figure 2.2.2.
Due to the impedance of the module connector of around $R_{mod} = 400\,\mu\Omega$, a voltage drop occurs depending on the different operating conditions of the cell stack.

1. If the nominal load current is drawn from the cell stack, the voltage drop across the module connectors will be negative and is given by

$$V_{mod,load} = -400\,A \cdot R_{mod} = -0.16\,V. \tag{2.2.1}$$

2. If the cell stack is being charged, the current direction is reversed and the voltage drop across the module connector will be positive and is given by

$$V_{mod,charge} = 1000\,A \cdot R_{mod} = 0.4\,V. \tag{2.2.2}$$

3. If the load is shorted due to a wiring fault, a temporary over current condition will occur until the system disconnects the cell stack. The voltage across the module connector in this failure mode is given by

$$V_{mod,short} = -4000\,A \cdot R_{mod} = -1.6\,V. \tag{2.2.3}$$

To connect the BMS across a module boundary, two connection schemes are possible as depicted in figure 2.2.2 (a) and (b).

If the voltage monitoring channel measures only the voltage drop across the connector V_{mod} (a), it could be used to monitor the integrity of the module connector itself. But as calculated above, the channel input voltage range would need to be extended below ground. This would increase development effort drastically and is therefore not desirable.

If the voltage monitoring channel measures the voltage drop across the connector V_{mod} plus the first cell voltage $V_{cell,i}$ in the neighboring module (b), it could also be used to indirectly monitor the integrity of the module connector. The voltage across the module connector can be calculated by subtracting the measurement taken by the next voltage monitoring channel. The sum of the cell voltage and the voltage drop across the module connector is always greater than

zero, so there is no need to extend the channel input voltage range below ground. For high cell voltages the input range would have to be extended above $5\,V$. This can be achieved simply by lowering the gain of the designed input attenuator and consumes no additional design effort.

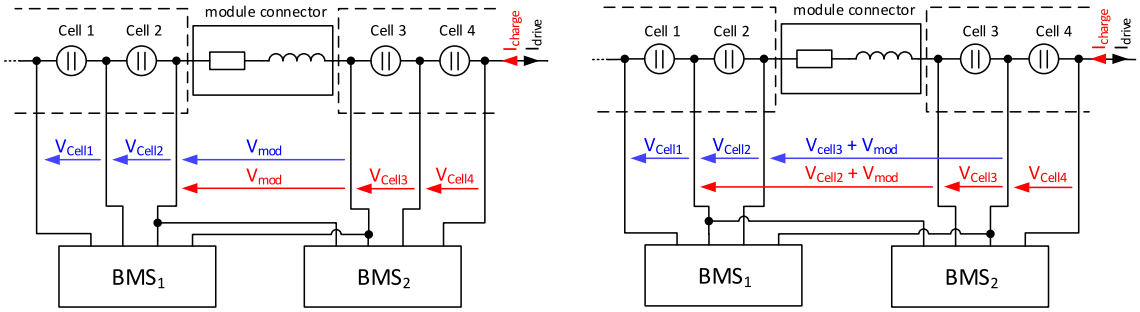


Figure 2.2.2: Different intermodule connection possibilities.

Additionally, the design should operate within the temperature range of $-40\,°C$ to $125\,°C$ and should have no current consumption in the power down state. All relevant system requirements have been listed in table 2.2.1.

	min	**typ**	**max**	**unit**
Temperature Range	-40		125	$°C$
Supply Voltage	1.4	1.5	1.6	V
Measurement Interval: all channels			200	ms
Cell Voltage Range	2		5	V
Input Voltage Range	-5.5		11	V
Aperture Time			10	ms
Absolute Measurement Error: including ADC			15	mV

Table 2.2.1: Requirements on the measurement system developed in this thesis.

2.2.2 Current publications

Different multi cell voltage monitoring systems for a BMS with HV multiplexer and HV switches have been reported in recent time. One of the most recent designs is presented in [13]. The HV switch used in the system is depicted in figure 2.2.3.

The design uses the devices $P1$ and $P2$ as the main conducting devices, because the PMOS devices can be simply switched on by pulling down the gate [13]. To generate a negative gate-source voltage V_{GS}, a current is switched on to cause a voltage drop across the resistors $R1$ and $R2$. The input $V[i]$ represents a low impedance source and the resistor $R1$ is connected directly, without causing a measurement error. The resistor $R2$ can not be connected directly to the output of the HV switch $V_{out}[i]$, because in on-state the current through $R2$ would cause a voltage drop across the on-resistance of the HV switch and therefore a measurement error. To mitigate that source of error, a simple source follower $P3$ is used to buffer the output voltage.
With the presented design it is only possible to switch on the PMOS devices if the input voltage $V[i]$ is higher than one V_{th} plus the voltage headroom for the current sources. For input voltages below that, the NMOS devices $N1$ and $N2$ are the main conducting devices.
Through the series connection of the two devices, at the PMOS and the NMOS side, the HV switch is always non conducting in the off-state.

The design has two main limitations. First, the HV switch cannot switch input voltages below ground. Which makes the design not usable in the cross cell measurement configuration as described in section 2.1. Second, the bias current for the voltage buffer cannot be switched off in power down. For a BMS this has to be considered as a severe disadvantage because it implies a constant current draw from every cell.

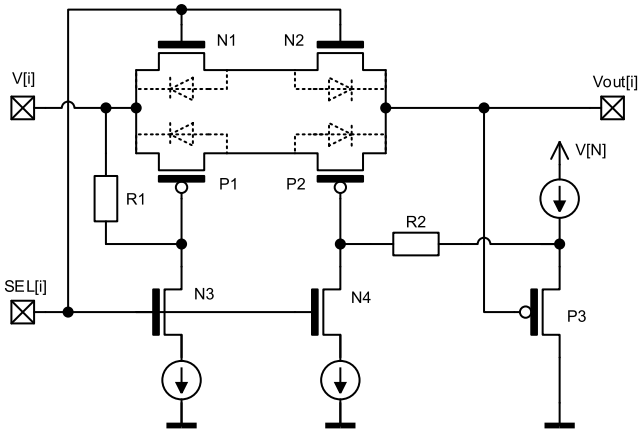


Figure 2.2.3: HV switch presented in [13].

Another design of an HV multiplexer to be used in a BMS has been presented in [3]. The HV switch used in the system is depicted in figure 2.2.4.
The design uses basically the same principle to turn on the HV switch as presented in [13], with the modification of the connection of the resistor R.
To switch on the PMOS devices $P1$ and $P2$, again a current source is switched on and the current causes a voltage drop across the resistor R, therefore generating a negative V_{GS} for both PMOS devices. If both devices are assumed to be non conducting, the current initially has to flow through one of the parasitic bulk diodes. With increasing V_{GS} the current will start to flow through the channel of the switched on PMOS devices.
To switch off the devices, the current source is switched off, causing both gates to be discharged over the resistor R. Through the series connection of the two PMOS devices, the HV switch is always non conducting in the off-state.

This design again has some limitations. First, the HV switch cannot switch input voltages below ground, which makes the design again not usable in the cross cell measurement configuration as described in section 2.1. In contrast to the design presented in [13], the HV switch does not consume any current in the off-state. A third limitation of the design is the lack of NMOS pass devices. Without the complementary devices, the HV switch is limited to input voltages above one V_{th} plus the voltage headroom for the current source. The last limitation of the design is, that in the on-state the pull down current causes a voltage drop across the on-resistance of P1 and therefore a measurement error.

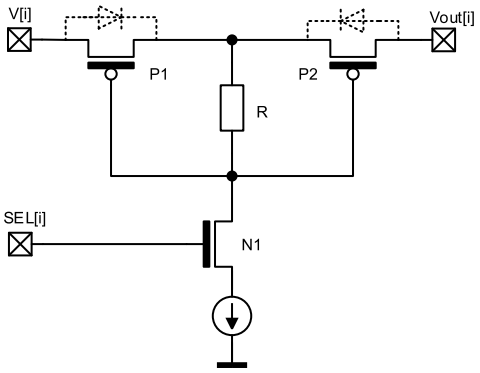


Figure 2.2.4: HV switch presented in [3].

A second important part to consider is the subsequent input attenuator to attenuate the cell voltage and transform it into the measurement range of the used ADC.

In [3] a resistive voltage subtractor has been used as the core of the HV multiplexer as depicted in figure 2.2.5. The report claims a measurement accuracy of 2.54 %. This is to be accepted and can be explained by the matching accuracy of resistors in a typical CMOS process. Due to the requirements on the measurement system stated in 2.2.1, a resistive based input attenuator cannot be used.

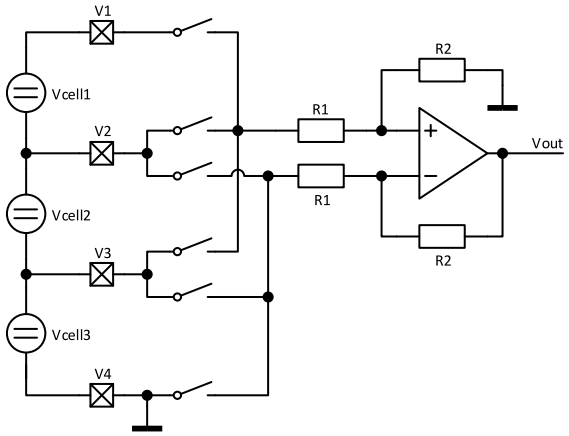


Figure 2.2.5: HV multiplexer presented in [3].

An important drawback that has to be considered when employing a resistive feedback system is, that the on-resistance of the switches in the feedback circuit causes a measurement error due to the voltage drop from the currents in steady state. The only way to mitigate this source of error, is to reduce the on-resistance by making the switches large. This leads to an area intensive design and should be avoided.

The system presented in [13] uses capacitive attenuation and claims a measurement accuracy of $0.3\,mV$ determined through simulation. At a reference voltage of $3\,V$, the reported accuracy is equivalent to a resolution of more than $13\,bit$. Again this is to be accepted and can be explained by the much higher matching accuracy of capacitors in a CMOS process [18]. Another benefit of a charge based design is that in steady state no current is flowing and therefore no voltage drop is occurring, making the design insensitive to large on-resistances and therefore more area efficient.

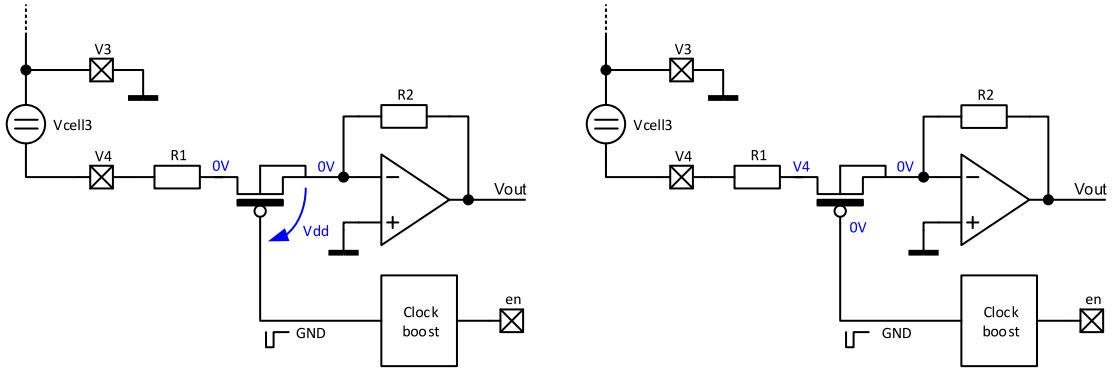
2.3 Design Reuse

To reuse one of the recently published designs [3] [13], the input voltage range has to be extended below ground, because none of the analyzed designs have this capability.

One possibility to design an input multiplexer which is able to work with input voltages below ground is depicted in figure 2.3.1. The circuit essentially works like a simple inverting amplifier, with its output voltage V_{out} given by

$$V_{out} = (V_3 - V_4)\frac{R_2}{R_1}. \tag{2.3.1}$$

To switch off the input channel and reduce the current draw, an HV PMOS transistor is used. It is controlled via a clock boosting circuit, which inverts the control signal. A benefit of the design is, that due to the fact that the common mode input voltage of the amplifier is at $0\,V$ no rail-to-rail input capability is needed.
Unfortunately the circuit is still suffering from the same disadvantages as the circuit presented in [3]. The main issue is still the limited matching accuracy of resistors in a CMOS process and the gain error resulting from it. To be able to reduce the systematic gain error caused by the on-resistance of the HV PMOS transistor, the ratio of R_1 to R_{on} of the transistor has to be made as big as possible. This directly translates into an increase in area.



(a) on-state (b) off-state

Figure 2.3.1: Simplified circuit of an input attenuator for operation below ground.

2.4 Conclusion

From the analysis of current publications, the conclusion has been reached that, to employ the described cross cell measurement system, a new design for an HV input multiplexer and attenuator has to be developed. Additionally the conclusion has been reached that a capacitor based attenuator is most suited for the design developed in this thesis.

Chapter 3

Switched Capacitor Amplifier

The goal of this chapter is to design a circuit that fulfills the stated requirements for the measurement system. To be able to design an accurate system, two main sources of error have to be considered: gain and offset error. Both types of error have to be minimized by design as good as possible. This ensures a high measurement accuracy over a wide range of operating conditions and makes the system robust against manufacturing variations.

The first considerations are made to minimize the gain error of the system. The gain of most measurement systems is defined ratio metric. It can be therefore stated that matching is the most important parameter that determines the gain error. From this a capacitance based measurement system has been selected, due to the fact that capacitors are typically the best matched devices in a CMOS process [18].

Offset errors are minimized by utilizing a design which inherently compensates any arising offset voltage. The circuit presented in [15] and shown in figure 3.0.1 implements such a design. A factor influencing the offset error of the system is the fact that in order to minimize the steady state error of any system with feedback, the system would need infinite gain. From this the requirement for the amplifier can be derived to have high gain.

From the circuit depicted in figure 3.0.1, three major sub circuits can be identified: the operational amplifier (1), the HV tolerable input switch (2) and the *low voltage* (LV) switches in the feedback network (3). For every sub circuit, requirements have to be derived and circuits have to be found and optimized to meet those requirements.

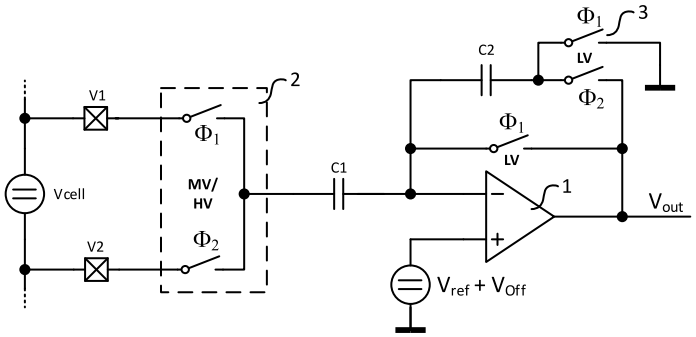


Figure 3.0.1: Switched capacitor amplifier with offset compensation [15]

Additionally an appropriate reference voltage V_{ref} as the common mode input voltage has to be

chosen. One disadvantage of using a reference voltage is the fact, that the circuit has per definition no *power supply rejection* (PSR) towards the voltage reference. The only stable reference voltage would be therefore per definition the circuit ground. Unfortunately it is not possible to use ground as the reference for the SC amplifier. The reason for this is, that during the sampling phase Φ_1 the output voltage V_{out} should settle at the common mode input voltage plus the offset voltage V_{off} of the amplifier. If now the offset voltage is negative and the common mode input voltage is at $0\,V$, the output can not reach the required voltage due to the single supply design. Therefore it is not possible to compensate the offset voltage in this configuration. By choosing the reference voltage at $\frac{V_{dd}}{2}$ the offset voltage is compensable.

3.1 Principle of Operation

To analyze the function of the SC amplifier, each phase has to be considered separately and the steady state of the circuit has to be determined with respect to charge conservation.
In the sample phase Φ_1, the SC amplifier can be represented as shown in figure 3.1.1.(a). The charge in each capacitor is given by

$$\begin{aligned} Q_1^{'} &= C_1(V_1 - V_{off}) \\ Q_2^{'} &= C_2 V_{off}. \end{aligned} \tag{3.1.1}$$

In the amplification phase Φ_2, the SC amplifier can be represented as shown in figure 3.1.1.(b). Again, the charge in each capacitor is given by

$$\begin{aligned} Q_1^{''} &= C_1(V_2 - V_{off}) \\ Q_2^{''} &= C_2(V_{off} - V_{out}). \end{aligned} \tag{3.1.2}$$

By applying charge conservation the following condition can be stated

$$\begin{aligned} \Delta Q_1 &= \Delta Q_2 \\ C_1(V_1 - V_{off} - V_2 + V_{off}) &= C_2(V_{off} - V_{off} + V_{out}) \end{aligned} \tag{3.1.3}$$

where $\Delta Q = Q^{'} - Q^{''}$. From (3.1.3) the gain of the SC amplifier can be found to be

$$V_{out} = (V_1 - V_2)\frac{C_1}{C_2} \tag{3.1.4}$$

therefore compensating the offset voltage V_{off} and amplifying the voltage difference at the input of the circuit.

(a) sample phase Φ_1 (b) amplification phase Φ_2

Figure 3.1.1: Representation of the SC amplifier in different phases.

3.1.1 Parasitics

In order to minimize the gain error, careful considerations have been made with respect to parasitic capacitances in the circuit. From figure 3.0.1 it can be observed that on one hand both

feedback capacitors are always connected to a low impedance source on one side. Given by the input voltages V_1 and V_2 or the output of the amplifier V_{out}. Therefore any parasitic capacitances from these nodes to ground are charged by the described sources and do not lead to an error in the system. Additionally both capacitors are connected to the node at the inverting input of the amplifier, which is at a constant voltage and therefore no charge is flowing into parasitic capacitances from this node to ground.
It can be concluded, that parasitic capacitances of $C1$ and $C2$ towards ground do not cause any measurement error. The selection of the type of capacitor for the SC amplifier can be therefore made without considering parasitic capacitance and purely on other requirements like, consumed area and voltage capability.

On the other hand, parasitic capacitances which change the values of the feedback capacitors C_1 and C_2 do cause an error and have to be minimized. These are the parasitic capacitances across the feedback capacitors and the parasitic capacitance across the LV switches. By shielding the node at the inverting input of the amplifier, all parasitic capacitances across the feedback capacitors are converted into parasitic capacitances towards ground, mitigating their effect. By using a grounded shield at one of the inputs of the LV switch, the same effect can be accomplished for the switches.

The principle of the described shielding technique is depicted in figure 3.1.2. The line L_2 is completely surrounded by a conductor, which is connected to ground. Therefore eliminating all parasitic capacitance between lines L_1 and L_2 and converting them to capacitances towards ground.

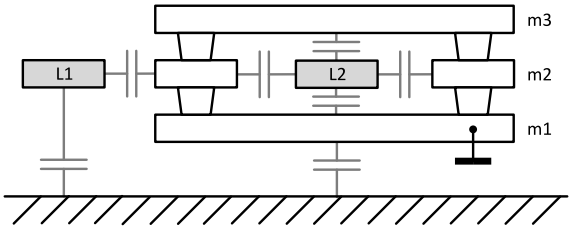


Figure 3.1.2: Principle of shielding a line

3.2 Operational Amplifier

In this section the design of a low voltage *operational amplifier* (OPA) in a $130\,nm$ technology [5] is described, to be used in the proposed SC amplifier (figure 3.0.1).
By using an SC scheme, the requirements on the OPA can be relaxed with respect to certain aspects. First, because of the inherent offset compensation of the circuit, no complex offset reduction techniques are needed. Second, the offset compensation can be exploited to make use of a simpler input structure.

To efficiently use the input range of the ADC in the later stage, the OPA has been designed with rail-to-rail output capability. This presents a difficult design challenge because of the low supply voltage of $1.5\,V$.

3.2.1 AB Output Stage

A low voltage output stage should satisfy the following set of requirements [8] [12] [2]:

1. The output voltage range should be rail-to-rail, to efficiently use the supply voltage.
2. The biasing has to be in class-AB to efficiently use the supply current. The class-AB biasing should have:
   (a) a high ratio of maximum to quiescent current
   (b) smooth AB transition for avoiding distortion
3. The output stage should have a large small-signal transconductance to shift the capacitive load-dependent pole towards higher frequencies.

$$p_{nd} \propto \frac{g_{m2}}{C_L} \tag{3.2.1}$$

4. The output stage should not degrade stability and DC gain of the amplifier.
5. The output stage should be simple and area efficient.

The control principle for an AB output stage is shown in figure 3.2.1 [4]. The floating voltage source V_{AB} ensures that both output devices $P1$ and $N1$ are biased with a small quiescent current. The voltage V_{AB} is given by

$$V_{AB} = V_{dd} - V_{gs,P1} - V_{gs,N1} - V_{ss} \tag{3.2.2}$$

where $V_{gs,P1}$ and $V_{gs,N1}$ are the gate-source voltages of the output devices. Because the output current is potentially large, the gate-source voltages are also large and therefore it is possible that V_{AB} is negative. This is especially true for systems with low supply voltage. It is important that a smooth switchover of the output devices is ensured to avoid crossover distortion. To avoid instability, sufficient quiescent current has to flow, even if no output current is drawn [4].

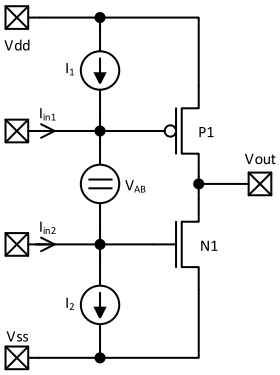


Figure 3.2.1: Principle of an AB output stage.

A common implementation of the principle shown in figure 3.2.1 is the circuit depicted in figure 3.2.2 [4]. The floating voltage source is implemented by the complementary transistors $N4$ and $P4$, together with the biasing transistors $N2-3$ and $P2-3$. The minimum current of the output devices is well controlled by the floating voltage source. The gate-source voltage of $P1$ and $N1$ is given by

$$V_{gs,N1} = V_{gs,N2} + V_{gs,N3} - V_{gs,N4} \approx V_{gs,N} \tag{3.2.3}$$

$$V_{gs,P1} = V_{gs,P2} + V_{gs,P3} - V_{gs,P4} \approx V_{gs,P}, \tag{3.2.4}$$

therefore leaving one gate-source voltage for the output devices and ensuring a minimum quiescent current in the output devices.

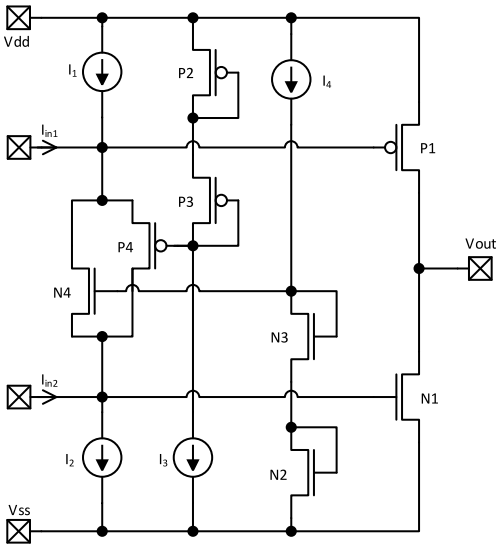


Figure 3.2.2: Implementation of an AB output control with floating voltage source.

One disadvantage of the AB control scheme shown in figure 3.2.2 is, that it needs a minimum supply voltage of two gate-source voltages and one saturation voltage. For example the biasing branch with $P2$ and $P3$ needs two gate-source voltages and enough voltage headroom for the current source I_3. For the used process this is around $1.2\,V$ and therefore not desirable as an amplifier design.

The AB control architecture presented in [4, p.7] and depicted in figure 3.2.3 demonstrates a robust and simple implementation of an AB control scheme, named "folded mesh" by the author. The design controls the minimum current in the output devices $P13$ and $N16$ via a regulation loop, composed of the differential amplifier $P6$ and $P8$, the reference voltage V_{ref} and a minimum selector with load impedance Z. The minimum selector senses the current in the output devices and causes a voltage drop across the load impedance Z, proportional to the minimum current in the output devices. The amplifier controls the output devices in such a way that the voltages across Z and V_{ref} are equal. Therefore it is controlling the minimum current. The input currents I_{in} to the system shift the output common mode voltage of the amplifier, therefore controlling V_{out}. The output stage design is able to operate with supply voltages as low as one gate-source voltage and two saturation voltages.

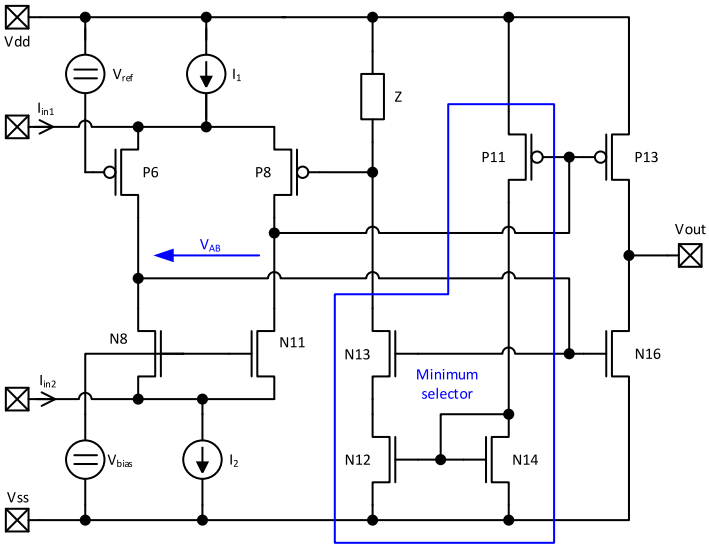


Figure 3.2.3: Implementation of an AB output control with minimum selector.

3.2.2 Input Stage

For the circuit presented in figure 3.0.1, the input common mode voltage was chosen at $\frac{V_{dd}}{2}$. This has two positive effects. First, a simple five transistor *operational transconductance amplifier* (OTA) as depicted in figure 3.2.4 can be used as the first stage of the amplifier. Second, the output of the amplifier is at $\frac{V_{dd}}{2}$ during the sampling phase Φ_1 and has to slew maximally $\frac{V_{dd}}{2}$, during the amplification phase Φ_2. This reduces design effort and enables an increased switching frequency. Because the input common mode voltage is constant, there is no need for rail-to-rail input capability and no design effort has to be put into increasing the *common mode rejection* (CMR).

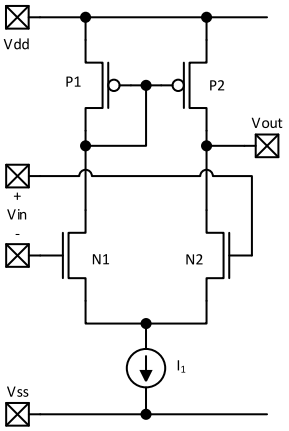


Figure 3.2.4: Simple OTA to be used as the first stage.

3.2.3 Operational Amplifier Design

The amplifier depicted in figure 3.2.5 has been designed to be used as the core of the SC amplifier circuit presented in this chapter. To implement the AB output stage, the architecture presented in [4, p.7] has been used. The presented circuit is a simple and robust implementation of an AB class control principle, which is able to operate with very low supply voltages. The control mesh

consisting of the transistors $N8$, $N11$, $P6$ and $P8$ drives the output transistors $N16$ and $P13$ in such a way, that the minimum current in the output transistor is regulated. The transistors $P11$ and $N12 - N14$ form a CMOS minimum current selector. The current in the output transistors is measured by the transistors $N13$ and $P11$. The transistors $P6$ and $P8$ form a differential pair, which regulates the current in $P4$ and $P10$ to be equal. The control mesh is biased with a constant current from $P7$ and $N9$. The second stage is controlled by the output current from the first stage, which flows into the top node of the folded mesh.

The quiescent current in the output stage is determined by analyzing the case in which no output current is flowing and therefore equal current in the output transistors $P13$ and $N16$ flows. If the ratio between $P13$, $P11$ and $N16$, $N13$ is equal, the current in $P11$ and $N13$ is also equal. The current from $P11$ flows into $N14$ and leads to the same gate-source voltage $V_{GS,N12}$ as at the gate of $N13$. If the transistors $N12 - N14$ are all sized equally, the combination of $N13$ and $N12$ can be considered as a single transistor, with double the gate length of $N14$ and at the same gate voltage. The current mirror formed by $N12 - N14$ therefore mirrors the current from $P11$ into $P10$ with a ratio of two. The quiescent current is therefore given by [4]

$$I_q = 2\frac{W_{P13}L_{P11}}{L_{P13}W_{P11}}I_{ref} \tag{3.2.5}$$

where I_{ref} is the current in $P4$.
To determine the respective minimum currents in the output transistors two cases have to be considered. If $N16$ drives the output current, the minimum current of $P13$ should be controlled. If the drain current of $N16$ is large, also its gate-source voltage will be high. Therefore the gate voltage of $N13$ is high enough to enable $N12$ to operate in saturation. The cascoded current mirror, formed by $N12 - N14$ now mirrors the current from $P11$ into $P10$.
If $P13$ drives the output current, the minimum current of $N16$ should be controlled. Due to the high current in $P13$, a large current will flow through $P11$ and $N14$. Now $N14$ and $N12$ again act as current mirror and $N12$ is therefore pulling the drain of $N13$ towards the supply rail. $N13$ now mirrors the current of $N16$ into $P10$. For both cases the minimum current is given by [4]

$$I_{min} = \frac{W_{P13}L_{P11}}{L_{P13}W_{P11}}I_{ref} = \frac{1}{2}I_q. \tag{3.2.6}$$

Because the AB control uses feedback, stability of the AB loop has to be considered. The loop is formed by the measurement transistors $N13$ and $P11$, the amplifier formed by $P6$ and $P8$ and the minimum selector described above. To ensure stability, the class AB control loop has to have sufficient phase margin at its unity gain frequency. In addition, to ensure proper biasing of the output transistors, the control loop has to have a higher unity gain frequency as the main amplifier [4].

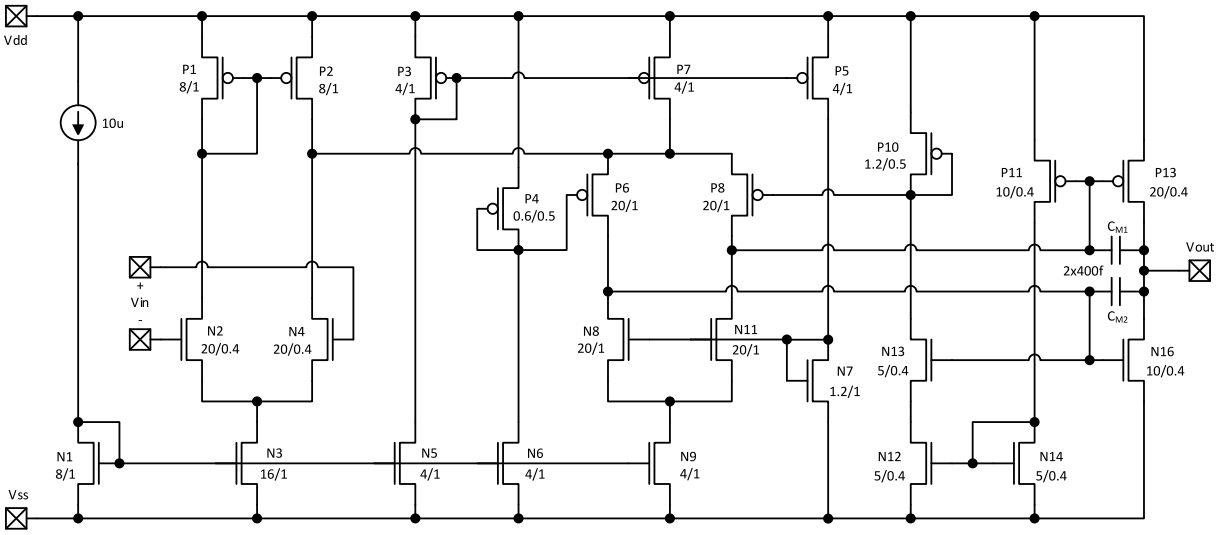


Figure 3.2.5: OPA with folded mesh AB output stage [4].

3.2.4 Operational Amplifier Analysis

Small Signal Parameter

In order to determine the small signal parameters of the amplifier presented in 3.2.5, it is best to redraw the transistor level circuit into a simplified small signal model. For the presented amplifier this small signal model is depicted in figure 3.2.6.

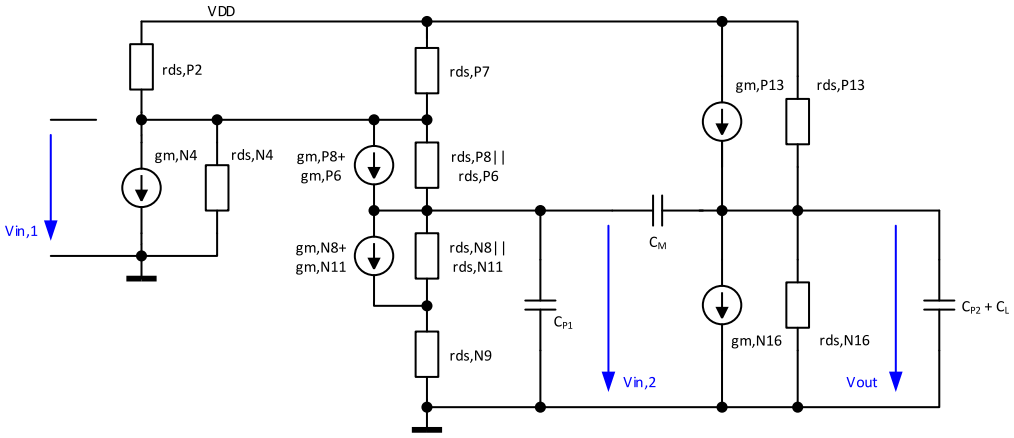


Figure 3.2.6: Small signal model of the OPA presented in figure 3.2.5

The first important parameter of an amplifier is the DC voltage gain A_0. For a multi stage design, the overall gain is simply the product of all voltage gains A_i of the individual stages. The voltage gain of the amplifier is therefore given by

$$A_0 = A_1 A_2 = g_{m1} r_{out1} g_{m2} r_{out2} \tag{3.2.7}$$

where g_m is the transconductance and r_{out} the output impedance of the corresponding amplifier stage.

The voltage gain of the output stage is given by

$$A_2 = \frac{g_{m,P13} + g_{m,N16}}{g_{ds,P13} + g_{ds,N16}} \tag{3.2.8}$$

which is the voltage gain of the two parallel *common source* (CS) stages at the output, formed by transistors $P13$ and $N16$. The output devices have to be scaled to have equal transconductance.

In order to calculate the voltage gain of the first stage, the output resistance of the first stage r_{out1} has to be found. The folded mesh $P6$, $P8$, $N8$ and $N11$ is only connected to high impedance nodes [4]. Therefore $N11$ functions as a cascode with an output impedance of $r_{ds,N9}$ multiplied by the voltage gain of $N11$. The same is true for the other devices in the mesh. The impedance seen by $P13$ and $N16$ can be assumed to be equal and is given by

$$\begin{aligned} r_{up} &= \left((r_{ds,P7} || r_{ds,P2} || r_{ds,N4}) \left(g_{m,P6} + g_{m,P8} \right) \left(r_{ds,P6} + r_{ds,P8} \right) \right) \\ r_{down} &= \left(r_{ds,N9} \left(g_{m,N8} + g_{m,N11} \right) \left(r_{ds,N8} + r_{ds,N11} \right) \right) \\ r_{out1} &= r_{up} || r_{down}. \end{aligned} \tag{3.2.9}$$

The voltage gain of the first stage is then given by

$$A_1 = g_{m,N4} r_{out1}. \tag{3.2.10}$$

The amplifier is a two stage design and each gain stage is contributing at least one pole to the system. Therefore appropriate frequency compensation has to be ensured. In the design, simple Miller compensation has been used. To determine the *gain bandwidth product* (GBWP) one has to determine the dominant pole frequency p_d and the DC gain A_0 of the amplifier first.

The pole p_i associated with a node in a circuit is given by

$$p_i = \frac{1}{r_i C_i} \tag{3.2.11}$$

where r_i is the impedance towards ground from this node and C_i is the effective capacitance at this node.

Due to the used compensation method, the dominate pole p_d is placed at the output of the first stage and is given by

$$p_d = \frac{1}{r_{out1} C_1} \tag{3.2.12}$$

where r_{out1} is the output impedance of the first amplifier stage and C_1 is the effective capacitance at the node. C_1 also contains the parasitic capacitance C_{p1} but is mainly determined by the miller capacitance C_M. Due to the Miller effect the capacitance is increased by the voltage gain of the second stage A_2. Including this in the equation of the dominant pole leads to

$$p_d = \frac{1}{r_{out1} C_M A_2} = \frac{1}{r_{out1} C_M g_{m2} r_{out2}}. \tag{3.2.13}$$

With the previously determined DC gain A_0 the GBWP of the amplifier can now be expressed by

$$GBWP = A_0 p_d = \frac{g_{m1} r_{out1} g_{m2} r_{out2}}{r_{out1} C_M g_{m2} r_{out2}} = \frac{g_{m1}}{C_M} \tag{3.2.14}$$

where C_M is the total Miller capacitance and g_{m1} the transconductance of the first stage, given by the input differential pair $N2$ and $N4$.

The non dominant pole p_{nd} is shifted to [4]

$$p_{nd} = \frac{g_{m2}}{C_{GS} + C_L + \frac{C_{GS}}{C_M} C_L} \tag{3.2.15}$$

where C_{GS} is the gate-source capacitance of the output stage and C_L is the load capacitance.

By approximating the amplifier with a simple two pole system, a relationship with the *phase margin* (PM) can be stated with

$$PM = 180° - atan\left(\frac{GBWP}{p_d}\right) - atan\left(\frac{GBWP}{p_{nd}}\right) \approx atan\left(\frac{p_{nd}}{p_d}\right). \tag{3.2.16}$$

By knowing the phase margin, the damping factor ζ of the system can be estimated with [17]

$$\zeta \approx \frac{1}{2}\sqrt{tan(PM)} \tag{3.2.17}$$

and with [17]

$$overshoot = e^{\frac{-\pi\zeta}{\sqrt{1-\zeta^2}}} \tag{3.2.18}$$

the overshoot of the system step response can be calculated.

The simulated frequency response of the amplifier is shown in figure 3.2.7. The response shows a very high phase margin of more than 70 ° and also a substantial DC gain of approximately 110 dB.

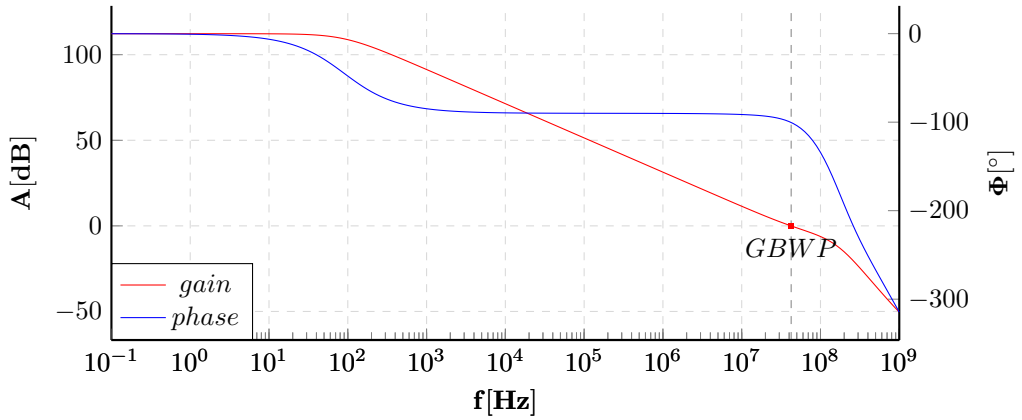


Figure 3.2.7: Frequency response of the designed amplifier for nominal operating conditions

Slew rate

Because of the class AB stage at the output, the maximum output current is very high, the *slew rate* (SR) is therefore not limited by the load capacitance and the output current, but by the Miller capacitances and the corresponding charging current.
The only part that is able to supply the charging current is the first stage. The transistors $P7$ and $N9$ act as constant current source and supply the bias current for the folded mesh. Any additional current supplied by the first stage, which is flowing into the top node of the mesh, has to flow into the capacitors C_{M1} and C_{M2}. Due to the symmetrical nature of the output

stage the charging current is split equally between C_{M1} and C_{M2}.

From figure 3.2.8 it is obvious that the low to high SR and the high to low SR are not equal. This is because on one hand, the maximum current the first stage is able to sink is equal to the current $P7$ provides. For this design this is $5\,\mu A$. The low to high SR is therefore given by

$$SR_{LH} = \frac{I_{P7}}{C_{M1}}. \tag{3.2.19}$$

On the other hand, the high to low SR is determined by the maximum current the first stage is able to source. If one side of the input differential pair is completely cutoff, the tail current provided by $N3$ flows into the top node of the AB control mesh. For this design the tail current is set to $20\,\mu A$. The SR for the high to low transition is therefore given by

$$SR_{HL} = \frac{I_{N3}}{C_{M1}}. \tag{3.2.20}$$

From figure 3.2.8 one can also see that there is almost no over- and undershoot. This is due to the high PM the amplifier has been designed with. Also visible in figure 3.2.8 is the present offset voltage. Due to the requirements derived for the amplifier design, no additional design effort has been put into minimizing the offset voltage.

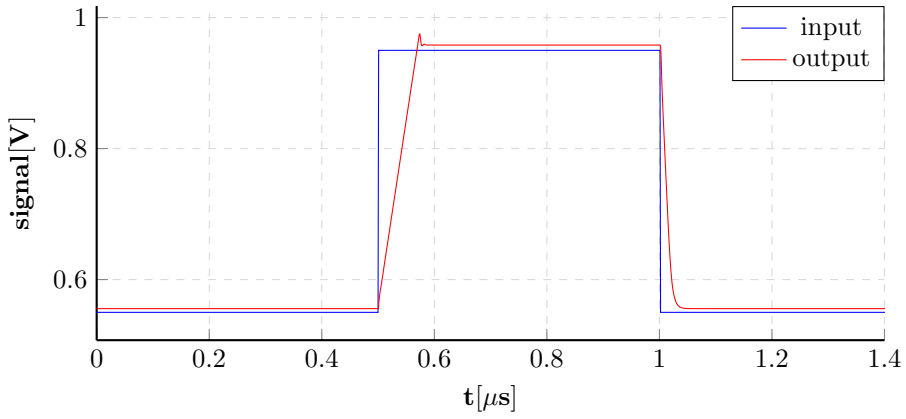


Figure 3.2.8: Step response of the designed amplifier

Through simulation of the presented design over the whole operating range, the worst case values of the described amplifier parameters have been determined and are presented in table 3.2.1.

	min	**max**	**unit**
A_0	98.04	116.4	dB
PM	67.46	89.48	°
GBWP	23.33	51.84	MHz
V_{offset}	2.78	11.48	mV
SR_{LH}	4.264	7.621	$V/\mu s$
SR_{HL}	−6.847	−21.43	$V/\mu s$
I_{sup}	114.5	183.4	μA

Table 3.2.1: Worst case OPA parameters for: $1.4\,V < Vdd < 1.6\,V, 8\,\mu A < I_{bias} < 12\,\mu A, -40\,°C < \vartheta < 125\,°C$, all 6σ process corners

3.3 Low Voltage Switch

In an SC circuit, leakage is a critical issue and has to be minimized. The first task to reduce the error introduced by leakage is to identify the switches which are most critical in terms of leakage.
A simplified view of the SC amplifier is shown in figure 3.3.1. Due to the used switching scheme described in section 3.1, always one of the switches S_2 or S_3 is connecting C_2 to a low impedance source, either V_{out} or ground. Leakage in S_2 and S_3 is therefore not critical for circuit performance.
S_1 on the other hand is connected to the high impedance node at the non inverting input of the amplifier. Any current flowing out of that node will discharge C_1 and C_2, therefore causing a measurement error.

Because the design of S_1 has to be optimized for low leakage and to reduce design effort, the same design is used for all LV switches in the system.

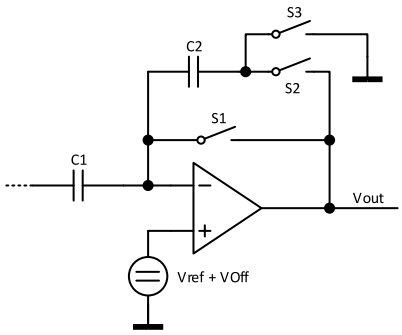


Figure 3.3.1: Simplified view of the SC amplifier.

3.3.1 Leakage Mechanisms

To reduce leakage currents by design, one has to understand the relevant leakage mechanisms and how to influence them.
In general, there are three main contributions to the leakage current: PN junction reverse bias current from drain and source to the well, subthreshold leakage in weak inversion between source and drain and gate oxide leakage.

PN Junction Reverse Bias Current

Drain well and source well junctions are always reverse biased and contribute a leakage current in the off- and on-state of the transistor. The current largely depends on the used doping profile, which can not be influenced by the designer and the size of the diffusion area and temperature. The equation describing the reverse junction leakage current I_r is given by [23]

$$I_r \propto A_j \left(\frac{qD_n n_{p0}}{L_n} + \frac{qD_p p_{n0}}{L_p} \right) \tag{3.3.1}$$

Where A_j is the area, D is the diffusion coefficient, L is the diffusion length, n and p are the respective thermal-equilibrium concentrations of minority carriers. It is therefore beneficial to reduce the area of the drain and source diffusion area. This is in accordance with the need to reduce the effect of charge injection, which is also area dependent.

Subthreshold Current

The equation for the subthreshold current is given by [20]

$$I_{ds} \propto \kappa \frac{W}{L} e^{\frac{V_{gs}-V_{th}}{m v_T}} \left(1 - e^{\frac{V_{ds}}{v_T}}\right) \tag{3.3.2}$$

where v_T is the thermal voltage $v_T = \frac{kT}{q}$. From the equation it is obvious that the biggest influence on the subthreshold current is coming from the exponential dependencies on V_{gs}, V_{th} and V_{ds}.

Gate Oxide Leakage

Gate oxide leakage is mostly dependent on the oxide thickness, which also can not be influenced by the designer.

3.3.2 Low Voltage Switch Design

Now that the critical design parameters for leakage current reduction have been found, ideally an architecture for an analog switch has to be found which reduces both V_{gs} and V_{ds} in the off-state and is minimally sized.
The circuit presented in [9] and shown in figure 3.3.2 proposes a modified transmission gate named "AT-switch" by the author, which minimizes leakage by biasing the pass devices with a negative gate source voltage in the off-state. This ensures that the pass devices are deeply cutoff.

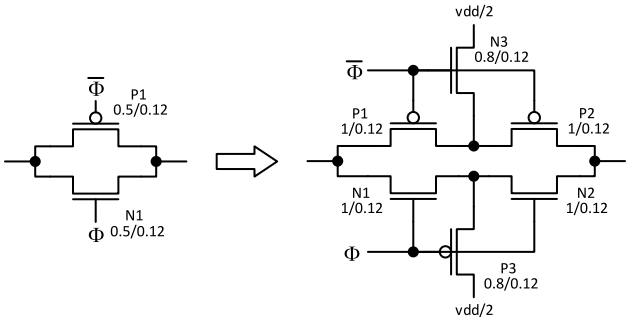


Figure 3.3.2: Leakage suppressed analog switch [9]

The negative gate source voltage is generated by pulling the sources of the corresponding transistors to $\frac{V_{dd}}{2}$ and the gates of the NMOS transistors to $0\,V$ and the gates of the PMOS transistors to V_{dd}.
This also reduces the maximal drain source voltage V_{ds} in the off-state to $\frac{V_{dd}}{2}$.
Additionally the circuit has been implemented with high threshold devices, which further reduces the leakage current.

To make a comparison between a simple analog switch and the improved AT-switch, both switches in figure 3.3.2 have been designed to have similar on-resistances. For small drain-source voltages V_{DS}, the drain current I_D of a MOS transistor is given by

$$I_D = \kappa \frac{W}{L} \left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right) \approx \kappa \frac{W}{L}(V_{GS} - V_{th})V_{DS} \tag{3.3.3}$$

where κ is the process constant. With (3.3.3) an approximation for the on-resistance R_{ON} can be found to be

$$R_{ON} \approx \frac{V_{DS}}{I_{DS}} = \frac{1}{\kappa \frac{W}{L}(V_{GS} - V_{th})}. \tag{3.3.4}$$

From (3.3.4) one can see that for devices of the same type and with the the same biasing conditions, the on-resistance depends only on the $\frac{W}{L}$ ratio. To match the on-resistance, the two switches depicted in figure 3.3.2 have therefore been designed with an equivalent $\frac{W}{L}$ ratio.

The results of a simulation over the whole temperature range for the on- and off-resistances of the two switches is shown in figure 3.3.3. From the graph shown one can see that the on-resistances are very similar, but the off-resistances are vastly different. On one hand, the off-resistance of the leakage suppressed AT-switch is in the $G\Omega$ range over the whole temperature range. On the other hand, the off-resistance of the simple analog switch is not even visible at the scale of the graph, due to the fact that it is only in the $M\Omega$ range.

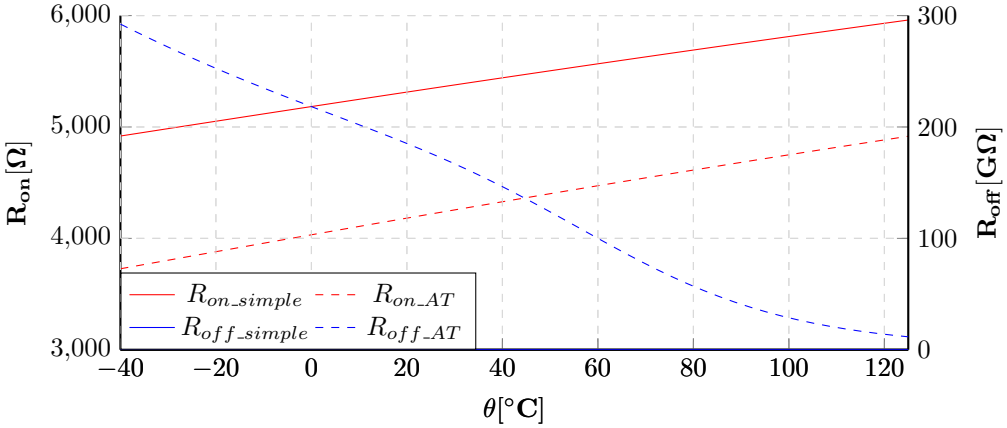


Figure 3.3.3: Comparison of the on- and off-resistance of the simple analog switch and the AT-switch

3.3.3 Low Voltage Switch Analysis

To explain the improvement achieved by the presented leakage suppressed switch, one has to analyze the effect on a single transistor. From figure 3.3.4 it can be seen that the reduction of the maximally occurring V_{ds} to $\frac{V_{dd}}{2}$ reduces the subthreshold current due to the *drain induced barrier lowering* (DIBL) effect. With an additional negative V_{gs} of $-\frac{V_{dd}}{2}$ the subthreshold current has been reduced by an order of two magnitudes.

Unfortunately, all discussed measures to reduce the leakage current, have the effect of increasing the on-resistance as well. But because the switch is used in an SC circuit, the on-resistance is not critical. A high on-resistance is only causing a larger delay but no voltage error. Unlike in a resistive feedback circuit, the static current is zero. Therefore there is no voltage drop across the switches.
It should be also mentioned that the used circuit introduces an area overhead, compared to the simple analog switch. But the alternative solution to minimize the error in an SC circuit due to leakage is to increase the size of the feedback capacitors, which would increase the area significantly. It can be concluded that the presented circuit offers overall area savings.

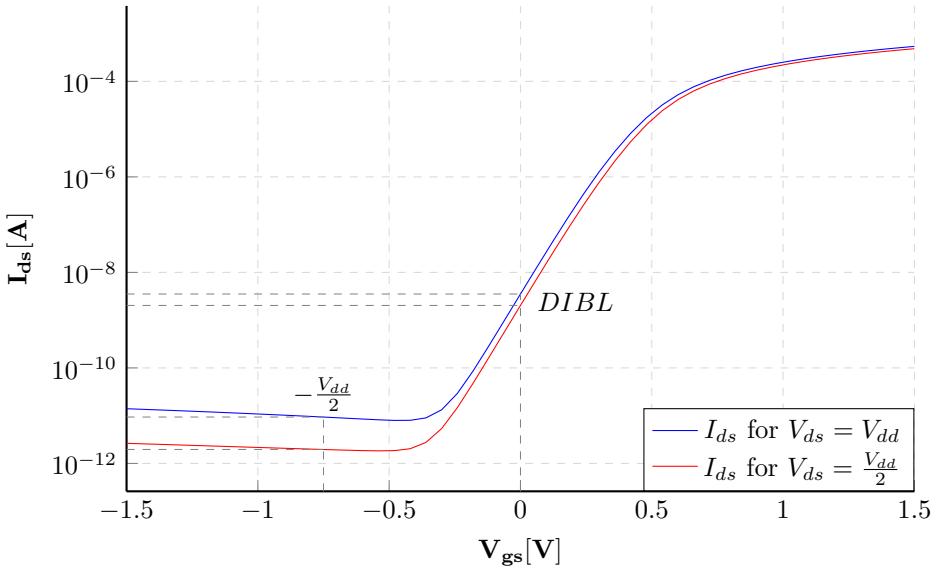
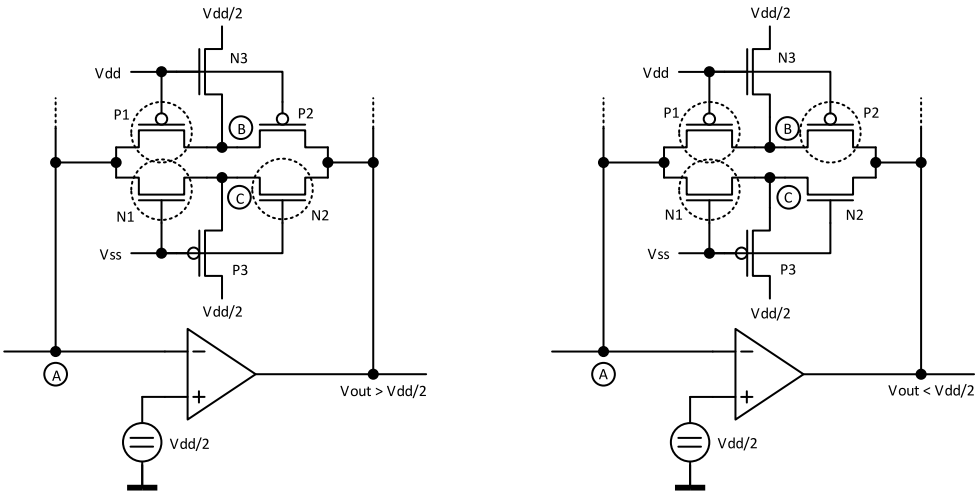


Figure 3.3.4: Subthreshold current for different V_{ds} over V_{gs} of a single transistor.

To show the leakage suppression achieved by the presented LV switch design, a detailed analysis at transistor level of S_1 has been made, as presented in [9] and depicted in figure 3.3.5.
The voltage at node A is always held at the common mode input voltage which is $\frac{V_{dd}}{2}$. In the off-state both nodes B and C are also held at $\frac{V_{dd}}{2}$ by $N3$ and $P3$ respectively. The drain and source of $N1$ and $P1$ are therefore at $\frac{V_{dd}}{2}$. In off-state the gate of $P1$ is at V_{dd} and the gate-source voltage is therefore positive. $P1$ is cutoff deeply and the sub threshold current is reduced. $N1$ has a negative gate source voltage and is also cutoff deeply.
Depending on the voltage at V_{out}, either $P2$ or $N2$ is again biased with a reversed gate-source voltage and therefore in deep cutoff.



(a) V_{out} is higher than $\frac{V_{dd}}{2}$

(b) V_{out} is lower than $\frac{V_{dd}}{2}$

Figure 3.3.5: Detailed view of the transistor level circuit of S_1 in off-state. Encircled devices are in deep cutoff.

3.3.4 Bias Voltage Generator

The needed bias voltage of $\frac{V_{dd}}{2}$ does not have to be very accurate or low impedance. The main goals are simplicity, low area and power consumption.

The simplest solution would be to use a resistive voltage divider with an additional transistor to switch off the current through the divider, to minimize power consumption. A rough estimate, for a current draw of around $10\,\mu A$, leads to approximately $75\,\mu m^2$ of area consumption. The circuit proposed in [10] and shown in figure 3.3.6.(a) presents an interesting alternative.

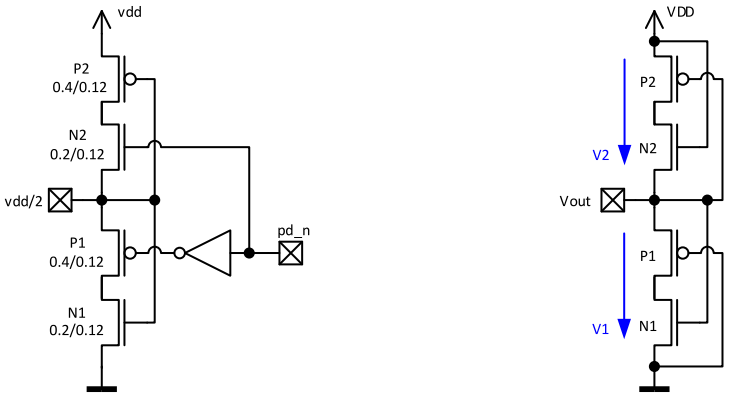


Figure 3.3.6: CMOS voltage divider [10].

Minimally sized transistors can be used, due to the requirements stated earlier, therefore the circuit can be built much smaller than a resistive voltage divider. A layout has been designed and the area consumed is only $24\,\mu m^2$.
Additionally the bias voltage generator can be powered down without additional switching transistors, therefore minimizing current consumption.

To understand the principle of operation of the presented circuit, the operating point has been calculated. The first observation made is, that per design the current through all devices has to be equal. All NMOS devices and respectively all PMOS devices are sized equally. Additionally, the transistors $N1$, $P1$ and $N2$, $P2$ have the same gate-source voltage of V_1 and V_2 respectively. Therefore the following condition can be stated

$$\begin{aligned} I_{d1} &= I_{d2} \\ \beta_P(V_1 - V_{th,P}) &= \beta_P(V_2 - V_{th,P}) \\ V_1 &= V_2 \end{aligned} \tag{3.3.5}$$

where $\beta_P = \kappa_P \frac{W_P}{L_P}$.
With the condition $V_{DD} = V_1 + V_2$ it can be stated that

$$V_1 = \frac{V_{DD}}{2}. \tag{3.3.6}$$

The lowest supply voltage V_{DD} the circuit is able to operate with is given by: two times the highest threshold voltage of the two device types [10].

The worst case circuit parameters have been determined through simulation and are presented in table 3.3.1.

	min	max	unit
V_{error}	-46.16	12.04	mV
I_{sup}	3.26	17.63	μA
I_{pd}	3.239	10.09	pA

Table 3.3.1: Worst case parameters for the CMOS voltage divider[10]: $Vdd = 1.5\,V, -40\,°C < \vartheta < 125\,°C$, all 6σ process corners

3.4 Input Voltage Switch

From figure 3.0.1 it is clear that the only sub circuit that is exposed to the high input voltage is the HV switch (2). To keep the design as simple and robust as possible, the best solution would be to develop an input switch which is capable of switching the whole input range. From this the requirement for the input voltage range has been derived to be $-5\,V$ to $10\,V$. A design with *medium voltage* (MV) devices, which can tolerate gate-source and drain-source voltages up to $10V$ [5], would therefore be possible. If the input voltage range should be increased or the design should have more safety margin, HV devices have to be used. The device parameters are very similar and therefore the device types can be interchanged without modifying the circuit or the dimensions. One advantage of using MV devices would be the smaller overall area of the input switch. Due to the main goal of designing a robust input switch, HV devices have been used.

Due to the charge based nature of the SC circuit, the on-resistance of the input switches do not cause a measurement error and only affects the time constant of the input switch. A small overdrive voltage for the pass devices $P1$ and $N1$ is therefore sufficient and the whole design effort can be targeted towards reducing measurement errors caused by charge injection and leakage currents.

Due to the fact that one high voltage device is always conducting and therefore connecting the output node of the input switch to one of the low impedance sources V_1 and V_2, the leakage current from the non conductive device does not flow through the connected capacitor and does not cause an error in the SC amplifier.

To minimize the effect of charge injection, the high and low side pass devices are sized equally. The injected charges therefore cancel each other at the output node of the input voltage switch.

Special care has to be taken with respect to parasitic junctions. In order to keep the structure of the high voltage switch simple, the circuit has been designed with the assumption that V_{in_p} is always greater than V_{in_n}. Because of this restriction the P-well of the triple well HV NMOS device $N1$ has been directly connected to V_{in_p} and the common N-well has been directly connected to V_{in_n}, ensuring that all parasitic junctions are reverse biased.

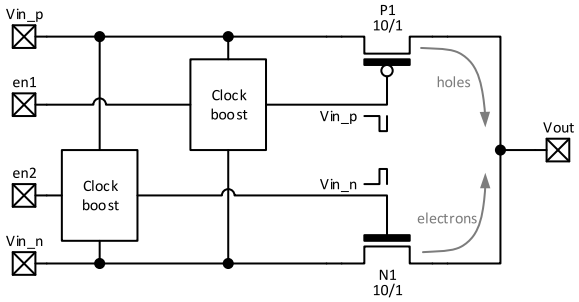


Figure 3.4.1: HV switch

To switch on the pass devices $P1$ and $N1$ with an input voltage independent on-resistance, a clock boosting circuit is used, which generates the corresponding drive voltages.
To turn on the high side PMOS transistor $P1$ the gate has to be at least one V_{th} lower than the input voltage V_{in_p} and to turn on the low side NMOS transistor $N1$ the gate has to be at least one V_{th} higher than the input voltage V_{in_n}. To generate these signals, the cross coupled charge pump presented in [16] and shown in figure 3.4.2 is used.

In order to derive the requirements for the charge pump, the worst case threshold voltage for both devices have to be considered.
For a HV NMOS transistor with a $\frac{W}{L}$ of at least 10, the threshold voltage is smaller than $0.9\,V$ [5].
For a HV PMOS transistor with a $\frac{W}{L}$ of at least 10, the threshold voltage is smaller than $0.95\,V$ [5].

By assuming a supply voltage of $1.5\,V$, a minimum boosting ratio of around 0.75 has to be achieved. Additionally the design of the clock boosting circuit has to operate from $-40\,°C$ to $125\,°C$. Therefore the cross coupled devices have to be optimized with respect to leakage.

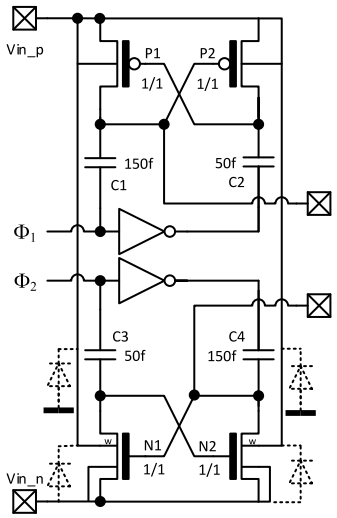


Figure 3.4.2: Clock boosting circuit

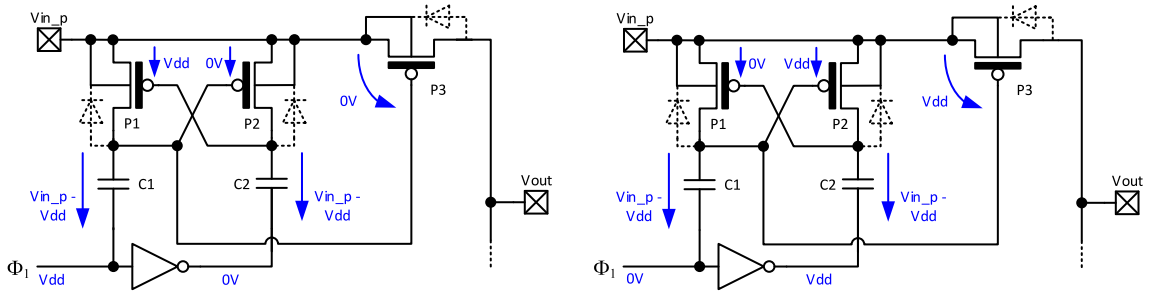
3.4.1 Principle of Operation

To describe the operating principle of the cross coupled charge pump, both phases the circuit operates in have been analyzed separately. The respective voltage levels at each node are shown

in figure 3.4.3.
At power on, both capacitors C_1 and C_2 are discharged and depending on the input voltage $V_{in,p}$, C_1 and C_2 are being charged over the parasitic bulk diodes of P_1 and P_2.
If we assume $V_{in,p} = 0V$ and $\Phi_1 = V_{dd}$, C_1 gets charged over the forward biased bulk diode of P_1. The steady state is reached when $V_{C_1} = V_{in,p} - V_{dd} + V_f$, where V_f is the forward voltage of the bulk diode. P_1, P_2 as well as P_3 are in cutoff.

If Φ_1 transitions from V_{dd} to $0\,V$, the gate of P_2 gets pulled down by C_1. The gate-source voltage V_{GS} of P_2 and P_3 is now sufficiently high to turn on P_2 and P_3, which in turn charges C_2 to $V_{in,p} - V_{dd}$. The high side pass device P_3 is now conducting and the circuit is in the on-state, as depicted in figure 3.4.3.(b).

If Φ_1 transitions from $0V$ to V_{dd}, the gate of P_2 gets pulled up by C_1. V_{GS} of P_2 and P_3 is now approximately $0\,V$. At the transition of Φ_1, the bottom plate of C_2 transitions from V_{dd} to $0\,V$ and pulls down the gate of P_1, which switches on $P1$ and in turn charges C_1 to $V_{in,p} - V_{dd}$. Both devices P_2 and P_3 are now in cutoff and the circuit is in the off-state, as depicted in figure 3.4.3.(a).



(a) off-state (b) on-state

Figure 3.4.3: Different states of the high side HV input switch.

The same considerations made, apply to the low side HV input switch as well.

3.4.2 Design

The circuit presented in [16] has been optimized with respect to area by taking into consideration how the load is connected to the clock boosting circuit. The output nodes of the clock boosting circuits have to drive the pass devices with an area of $10\,\mu m^2$ in addition to one of the cross coupled devices with an area of $1\,\mu m^2$. The load capacitance is therefore given by

$$C_{load} = (A_{pass} + A_{cross})C_{Area,HV} \approx (10\,\mu m^2 + 1\,\mu m^2)1.4\,\frac{fF}{\mu m^2}[5] \approx 15\,fF \tag{3.4.1}$$

The drive capacitors $C1$ and $C4$ have been selected to be ten times the size of the load capacitance and are therefore designed to be $150\,fF$. The drive capacitors $C2$ and $C3$ only have to drive one of the cross coupled devices and can be designed relatively small. They have been selected with $50\,fF$.

3.4.3 High Voltage Capacitor Selection

From the analysis made in section 3.4.1 it is clear that the drive capacitors of the clock boosting circuit depicted in figure 3.4.2 have to withstand voltages of up to $V_{in\_p} - V_{dd}$ for the PMOS side

and $V_{in\_n} - V_{dd}$ for the NMOS side. Therefore the largest voltage difference appears for the high side driver of the $10V$ channel. See figure 2.1.2 for orientation. The largest nominally appearing voltage is therefore $8.5V$. The used process [5] only offers few capacitors capable of handling such high voltages. In table 3.4.1 a comparison is made with respect to process parameters.

	$\mathbf{C_{area}}$	**SOA**	
	normalized	value	unit
cp2p1	2	± 8	V
cp2psw	6	± 8	V
cvppm4m1pw	1	± 60	V

Table 3.4.1: Parametric comparison of different HV capacitors available in the used CMOS process [5].

The *cp*2*p*1 type is a poly-poly capacitor which uses the floating gate of the available flash memory transistors and the standard poly. Capacitors available in a CMOS process are always non ideal and have a parasitic capacitance to the substrate. A typical cross section of a CMOS capacitor is depicted in figure 3.4.4. From the drawing it is clear that the bottom plate is closer to the substrate and therefore has a higher parasitic capacitance.

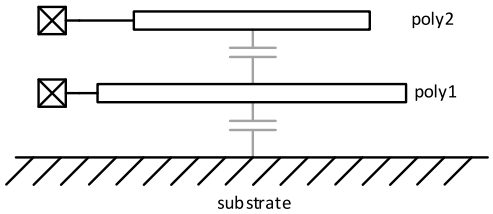


Figure 3.4.4: Simplified cross section of the *cp*2*p*1

The *cp*2*psw* type is constructed from the floating gate capacitance of a flash transistor in a triple well. A simplified cross section is shown in figure 3.4.5. Due to the parasitic P-well to N-well junction, the capacitor has constraints on the applied voltages and is therefore disadvantageous to use.
The *cp*2*psw* has a much higher area capacitance, but the need for a triple well increases the area consumption drastically, especially for small capacitances. For the design the capacitors are selected to be as small as possible and therefore the overall area savings of the *cp*2*psw* are relatively small.
Both described capacitors could be used as the driving capacitor, but because the voltage limit is slightly exceeded a lower life time has to be expected.

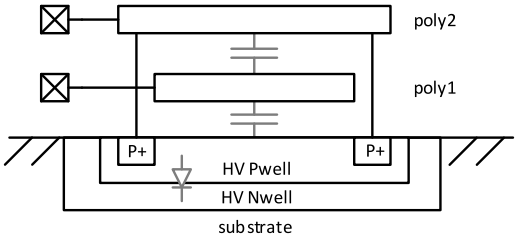


Figure 3.4.5: Simplified cross section of the *cvppm*4*m*1*pw*

The *cvppm*4*m*1*pw* is a *vertical parallel plate* (VPP) capacitor, which is constructed from the metal layers used for routing and the corresponding isolation oxide, as depicted in figure 3.4.6.

This type of capacitor has been qualified to be used in $60\,V$ HV processes and is therefore the one with the highest operating range. Although the oxide thickness is high compared to the other types, the fact that the capacitor is constructed vertically, keeps the area capacitance in a usable range. The *cvppm4m1pw* capacitor has no restrictions on polarity and is almost symmetric with respect to parasitic capacitance towards substrate.

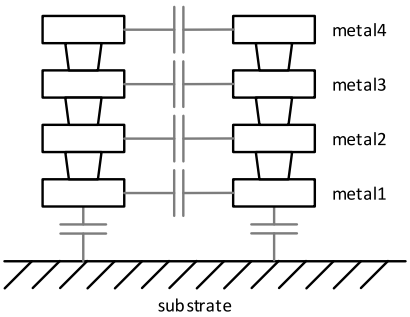


Figure 3.4.6: Simplified cross section of the *cvppm4m1pw*

From the considerations made, the *cvppm4m1pw* has been selected as the driving capacitor for the input switch.

3.4.4 Input Voltage Limitation

The maximum input voltage of the switch is limited by three breakdown conditions. First, the HV P-well is directly connected to the input V_{in_p}. Therefore a first condition 3.4.2 for the input voltage can be derived with

$$0V < V_{in\_p} < 18V[5]. \tag{3.4.2}$$

Second, the HV triple N well is directly connected to the input V_{in_n}. A second input voltage condition 3.4.3 can be derived with

$$-18V[5] < V_{in\_n} < V_{in\_p} \tag{3.4.3}$$

The third limitation is derived from the breakdown of the driving capacitors $C1$ to $C4$ of the clock boosting circuit. The capacitors $C1$ and $C2$ of the high side driver experience a maximum voltage

$$V_{in\_p} - V_{dd} < V_{C\_breakdown}. \tag{3.4.4}$$

The capacitors $C3$ and $C4$ of the low side driver experience a maximum voltage of

$$V_{dd} - V_{in\_n} < V_{C\_breakdown}. \tag{3.4.5}$$

From these conditions and the considerations made in section 3.4.3 one can conclude that the final limitation on the input voltage of the HV switch is given by (3.4.2) and (3.4.3).

3.4.5 Safety Considerations

Because the HV input switch is directly connected across the battery cell, some safety considerations have been made in terms of short circuit and other failure modes. The best solution in terms of safety is to make the design intrinsically safe.
In figure 3.4.7 the equivalent circuit of the HV input switch is depicted. Directly at the input, an external filter structure is used to block off any high transients.
Although the input switch is controlled by break before make signals, one can think of a failure

mode where both input pass devices are switched on simultaneously, shorting the battery cell. In this failure mode the current is limited by an external resistance in addition to the on-resistance of the pass devices. As described in section 3.4, a low on-resistance is not a design goal and therefore helping to reduce the short circuit current and making the design intrinsically safe.

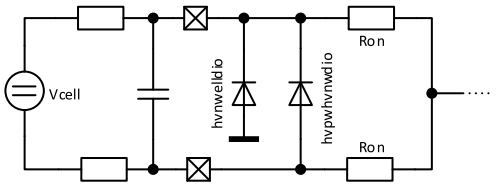


Figure 3.4.7: Equivalent circuit of HV switch failure mode

3.5 Feedback Capacitors

The feedback capacitors directly determine the gain of the system and therefore have to be matched precisely.
From 3.0.1 it is clear that the voltage across C_1 is in the range of the input voltage and therefore potentially much higher than the voltage across C_2, which is always smaller than $\frac{V_{dd}}{2}$. This not only causes a voltage dependent gain error, but because both capacitors have to be matched, both have to be HV capacitors. From the considerations made in 3.4.3, the feedback capacitors have been selected as *cvppm4m1pw* type devices.

3.5.1 Voltage and Temperature Dependencies

The voltage and temperature dependencies of any capacitor can be described by

$$C = C\left(1 + vc_1 \cdot V + vc_2 \cdot V^2\right)\left(1 + tc_1(T - T_0) + tc_2(T - T_0)^2\right) \tag{3.5.1}$$

where C_0 is the nominal capacitance, $vc_{1,2}$ are voltage coefficients and $tc_{1,2}$ are temperature coefficients.

Voltage Dependent Error

To calculate the worst case error caused by the voltage dependency the cell voltages V_{cell} are assumed to be $5\,V$. The voltage at the capacitor C_1 of the top channel is therefore $10\,V$. See figure 3.5.1 for orientation. The output voltage including the first order voltage dependency is given by

$$V_{out} = (V_p - V_n)\frac{C_1(1 + vc_1 \cdot V_p)}{C2(1 + vc_1 \cdot V_{dd})}. \tag{3.5.2}$$

With the values from the design manual [21] the worst case error is approximately $0.4\,mV$. This is well within acceptable limits. It is not possible to reduce the error by putting multiple capacitors in series, because the system would lose the benefit of insensitivity to parasitic capacitance towards ground as described in section 3.1.1.

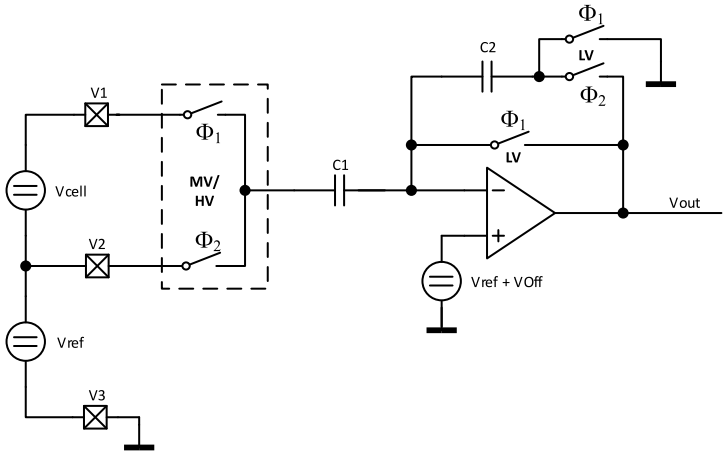


Figure 3.5.1: Top cell measurement system.

As stated above, the voltage dependent gain error is expected to be in the range of one millivolt. By simulating the circuit shown in figure 3.5.1 the voltage dependent measurement error has been determined. The result of the simulation is depicted in the diagram shown in figure 3.5.2. A clear voltage dependency is visible and the maximal measurement error reflects the expected values from the previously made estimation.

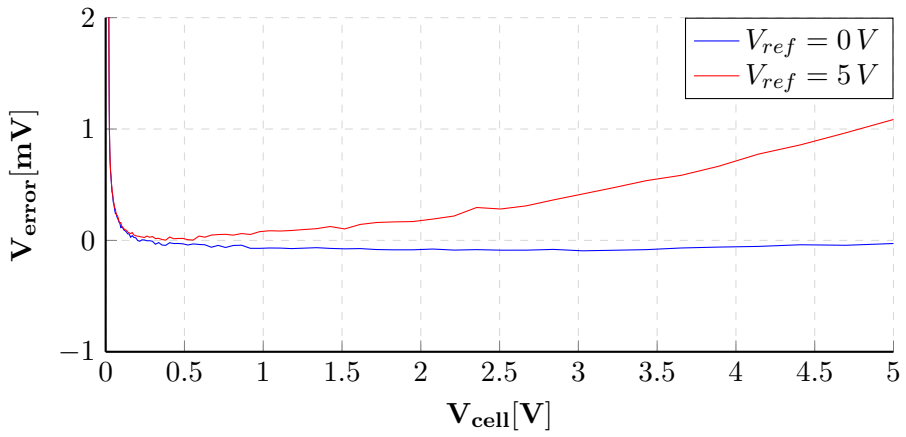


Figure 3.5.2: Simulation results for the voltage dependent gain error of the SC amplifier.

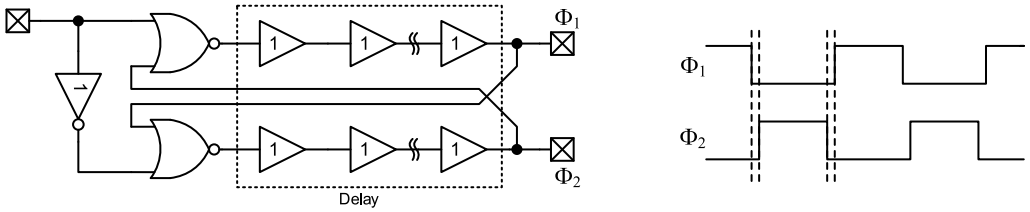
Temperature Dependent Error

Temperature differences across the feedback capacitors can be seen as first order gradient and are therefore compensated by the common centroid layout of the capacitor array and are no source of measurement error.

3.5.2 Control Signals

To control the two phases of the circuit depicted in figure 3.0.1, two control signals Φ_1 and Φ_2 are needed. The active state of both signals has to be non overlapping to ensure that the charge transfer during the phases happens as designed. A common way to generate such non overlapping control signals is by means of the circuit presented in [24, 5.4.5] and depicted in figure 3.5.3.
The circuit uses two NOR gates which are connected to form an SR latch. Through the addition

of delay elements in each signal path, the transition between the two states of the latch gets separated by the sum of delays of all delay elements.



(a) schematic (b) generated signals

Figure 3.5.3: Generation of two non overlapping signals.

The chain of delay elements in each signal path has to be non inverting, so that the function of the circuit is not altered. A typical delay element used consists of two inverters connected in series with an additional capacitive load to increase the time constant, as depicted in figure 3.5.4. The inverter charging the capacitive load is additionally weaker compared to the inverter at the output to further increase the delay per area. Unfortunately the delay achieved with this design is parameter and process sensitive.

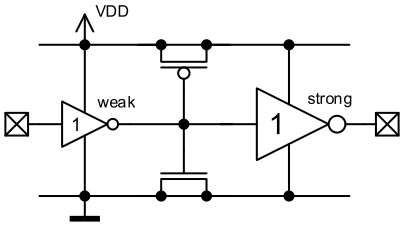


Figure 3.5.4: Typical delay element in a CMOS process.

3.6 Measurement System

3.6.1 Synchronous Single Input SC Amplifier

From the described switched capacitor amplifier it is now possible to construct the required cross cell measurement system. The only subsystem, that is exposed to the input voltage is the HV input switch. Due to the use of the clock boosting technique, the switch is input voltage independent.
One possible measurement system is therefore to use three identical channels in parallel as shown in figure 3.6.1. Such a system would enable synchronous sampling of all input channels by the SC amplifiers. Now the subsequent ADC can be much slower, because the input voltages cannot get out of sync any more.

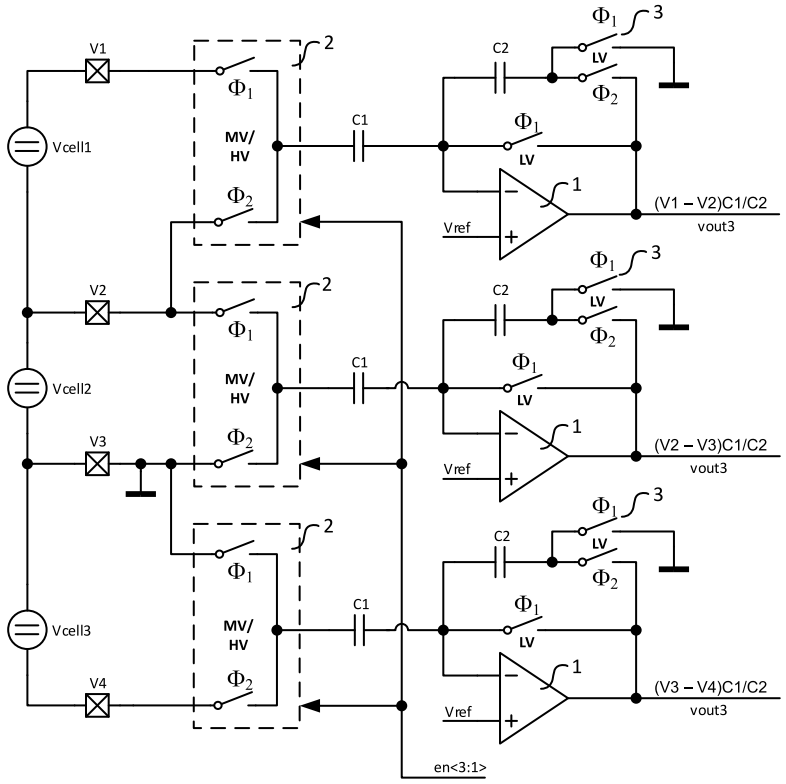


Figure 3.6.1: Synchronous single input SC amplifier.

3.6.2 Multiplexed Multiple Input SC Amplifier

A second measurement system can be derived by combining all input channels into a single SC amplifier as depicted in figure 3.6.2. The input structure is the same as in the synchronous implementation described above. To reduce the complexity of the system and to reduce the sources of error, the following scheme is used. A channel gets selected by setting the corresponding $en<i>$ signal to high. If a channel is inactive, the HV input switch is connected to the upper input voltage of the channel. Only the active channel switches between the upper and lower input voltage. The output voltage of the circuit is given by

$$V_{out} = \frac{C_1}{C_2} \sum V_{\Phi_1} - V_{\Phi_2} \tag{3.6.1}$$

where V_{Φ_1} and V_{Φ_2} are the voltages the respective input capacitor is connected to in clock phase Φ_1 and Φ_2 respectively. It is therefore possible to leave all inactive channels connected and sample the same input voltage in both phases and cancel the influence.
The advantage of this method is that the additional channels do not cause any error due to leakage currents, because of the effect described in section 3.4. The main benefit of the presented solution is, that by reducing the number of used amplifiers, the current and area consumption can be reduced. One disadvantage of the presented measurement system is the cross coupling of the channels. This could limit the measurement accuracy of the system.

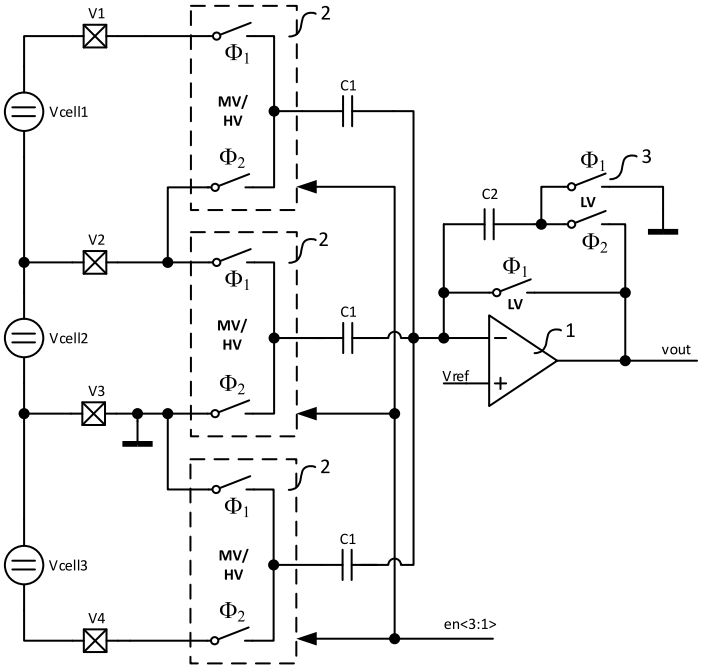


Figure 3.6.2: Multiplexed multiple input SC amplifier.

3.7 Layout

3.7.1 Matching

Deviations due to geometry and process parameter variation can be mitigated by careful layout of the design. The standard technique to compensate process gradients is to layout the matched devices as a common centroid structure. Meaning all geometric centers, of the sum of all unit elements comprising each of the matched elements, are in the same point. With this technique, all first order gradients across the structure are compensated.

The equation describing statistical mismatch of a device parameter X is presented in [19] and is given by

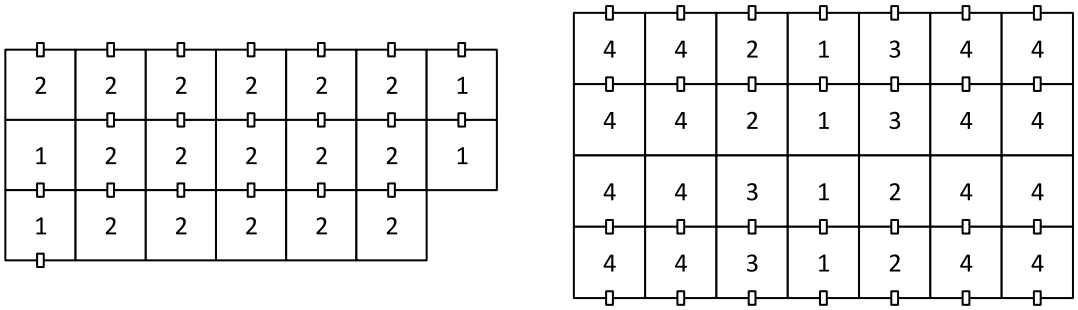
$$\sigma^2_{\Delta X/X} = \frac{A^2_{\Delta X/X}}{WL} + S^2_{\Delta X/X} D^2 \tag{3.7.1}$$

where A is the area matching parameter, S the spacing parameter. WL denotes the area of the device and D the distance between the matched devices.
It is thereof beneficial to use large devices and to put them in close proximity.

Another influence on device matching is the surrounding of the matched devices. It is best to design highly symmetrical layouts with identical surroundings by using dummy devices at the edges.
For relatively large technologies like the used $130\,nm$ process, the most critical *layout dependent effect* (LDE) as presented by [14] is the *well proximity effect* (WPE). For matched devices the distance to the edge of the well should be therefore equal or relatively large [14] [21]. Due to the use of dummy devices, the distance from the critical diffusion areas to the well edge is increased without additional area usage, therefore reducing the WPE and improving matching further.
Additionally the device orientation and direction of the current flow should be equal for matched devices [21].

3.7.2 Feedback Capacitor

In terms of accuracy, the feedback capacitors are the most critical part in the layout. They solely determine the gain of the system. The capacitors C_1 and C_2 therefore have to be matched closely.
The feedback capacitors are constructed from multiple unit capacitors connected in parallel and from a capacitor array. To ensure good matching, together with a common centroid layout, a floor plan for each capacitor array has been designed before the implementation in layout. The floor plan of the capacitor array of the synchronous sampling system is depicted in figure 3.7.1.(a). Each unit capacitor is drawn and marked with a number to group them. The most convenient and area efficient way to group them is in columns of three unit capacitors. This causes a slight mismatch in symmetry of the layout.
To ensure matching with respect to the connections made between the unit capacitors, the number of connections and the number of unit capacitors in a group are equal.
The same considerations have been made for the multiplexed sampling system and resulted in the floor plan of the capacitor array depicted in figure 3.7.1.(b).



(a) Capacitor array of the synchronous sampling system.

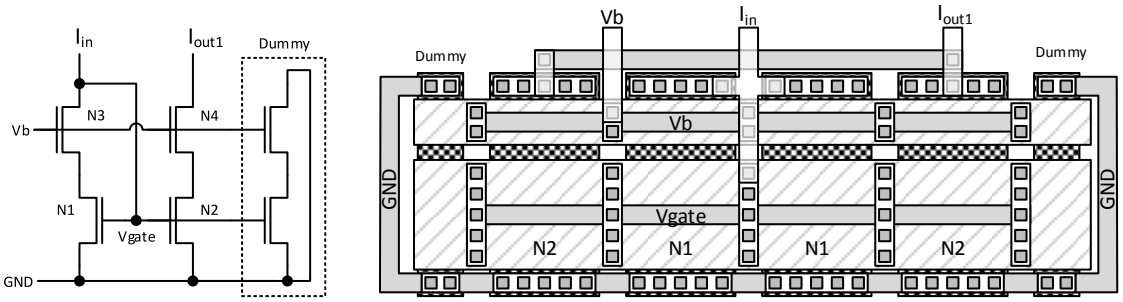
(b) Capacitor array of the multiplexed sampling system.

Figure 3.7.1: Floor plan of the different capacitor arrays.

With respect to surrounding symmetry, the selected capacitor type *cvppm4m1pw* used as the feedback capacitor is inherently matched, due to the fact that it is always used with a guard ring surrounding it. Therefore no dummy devices have to be used and a compact layout is achieved.

3.7.3 Current Mirror

A closely matched implementation of a cascode current mirror is depicted in figure 3.7.2.(b). The layout is highly symmetrical and consumes minimal area. As demonstrated in the layout, a common centroid design can be achieved for current mirrors as well. This again compensates all linear gradients, like temperature or process variation. Not shown in the layout is the surrounding guard ring. It ensures good substrate contact and provides the bulk connection to the current mirror. The same layout principle applies to current mirrors without cascode devices.

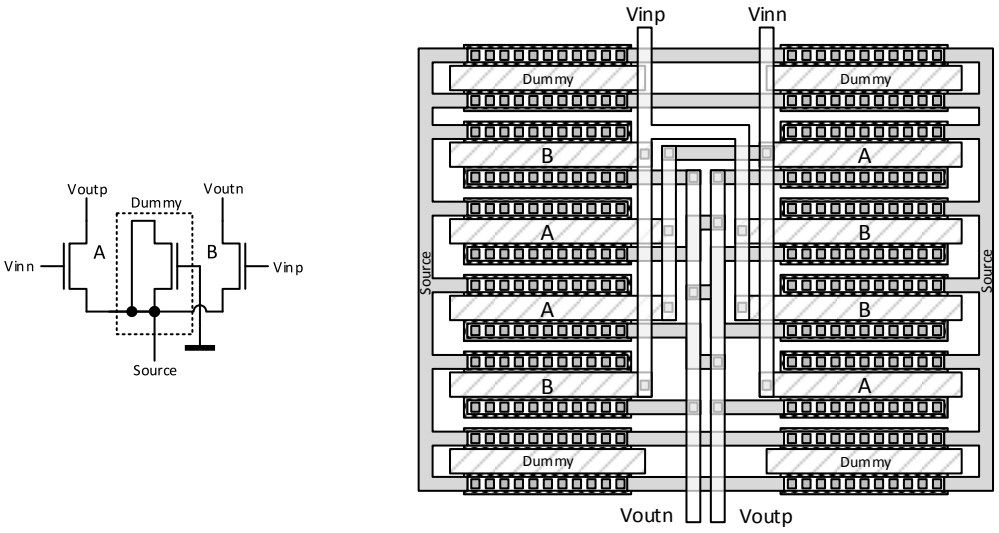


(a) schematic (b) layout

Figure 3.7.2: Cascode current mirror.

3.7.4 Differential Pair

Another critical block in layout is the input differential pair of the first amplifier stage. In general, matching of these devices is crucial for minimizing input offset voltage. For this design in particular, the input offset voltage is not relevant. But to create a reusable design and keep design effort low, some matching techniques have been still followed.
As described in section 3.7.1, one of the most important constraints to follow is the use of surrounding symmetry. Dummy devices have been therefore included at the boundaries of each column of devices. The devices themselves have been arranged as common centroid structure. The resulting layout is depicted in figure 3.7.3.(b). Not shown in the layout is the surrounding guard ring. It ensures good substrate contact and provides the bulk connection to the differential pair. It also reduces cross coupling with other sub circuits and reduces substrate noise [25] [22].



(a) schematic (b) layout

Figure 3.7.3: Differential pair.

3.7.5 Amplifier

The resulting layout of the amplifier designed in section 3.2 is shown in figure 3.7.4. Every sub circuit block has been designed separately and surrounded with an appropriate guard ring. In order to create a flexible design, only the first two metal layers have been used for connections.

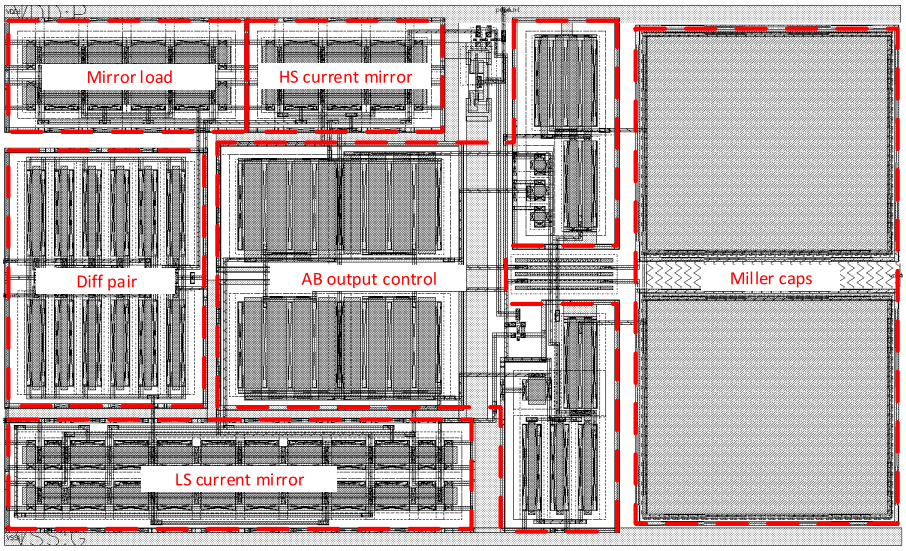


Figure 3.7.4: Layout of the AB output amplifier

3.7.6 Synchronous Single Input SC Amplifier

The complete layout of one channel of the synchronous sampling system presented in section 3.6.1 is depicted in figure 3.7.5. A compact layout has been achieved, demonstrating the feasibility of the selected architecture.

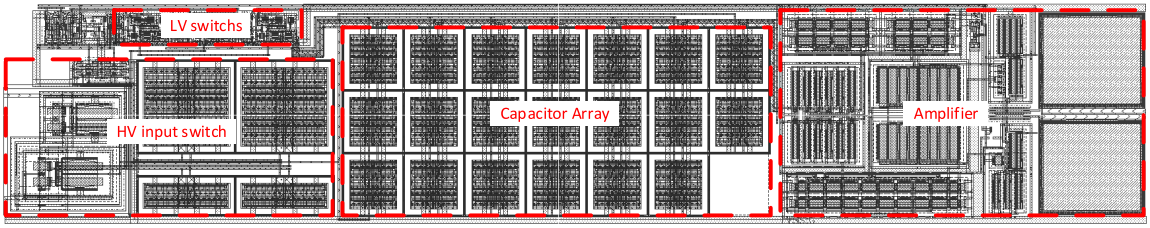


Figure 3.7.5: Layout of one channel of the synchronous sampling circuit

3.7.7 Multiplexed Multiple Input SC Amplifier

The complete layout of the multiplexed sampling system presented in section 3.6.2 is depicted in figure 3.7.6. Again a compact layout has been achieved, which demonstrates the feasibility of the selected architecture.

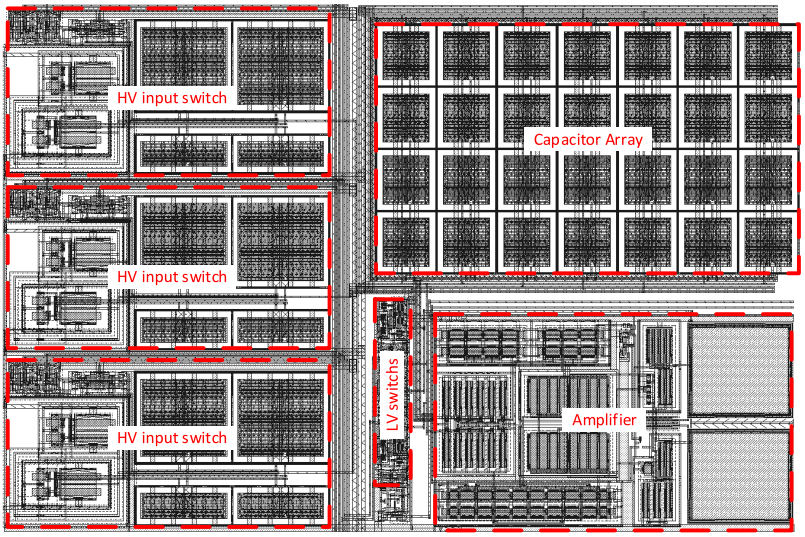
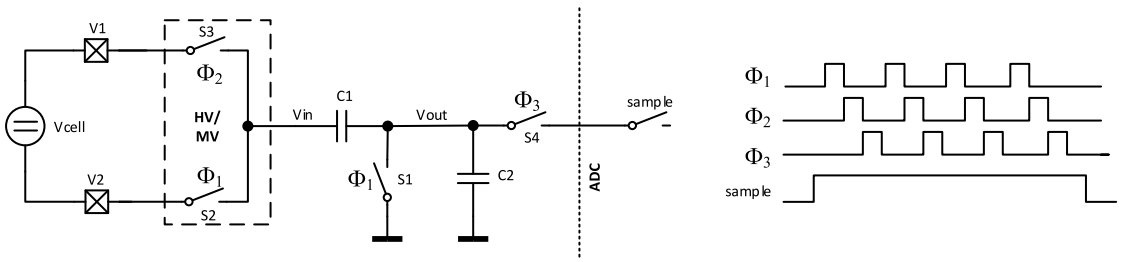


Figure 3.7.6: Layout of the multiplexed sampling circuit

Chapter 4

Switched Capacitor Divider

The circuit presented in chapter 3 is very flexible in terms of input voltage and gain. It is also very accurate but has the disadvantage of using an operational amplifier, therefore consuming additional area and power. The goal of this chapter is to come up with a simplified circuit that does not need an amplifier nor rely on any bias voltages or currents and which does not consume any power other than during the sampling phase.
One possible design that fulfills these requirements is the SC divider circuit depicted in figure 4.0.1. The circuit essentially works like a charge pump, charging the sampling capacitor of the subsequent ADC. Because of this, the problem arises that the settling time of the system depends on the sizes of the sampling capacitor and the size of the capacitors in the SC divider. This leads to one disadvantage of the presented system, which is the need for a long sampling time.



(a) schematic (b) control signals

Figure 4.0.1: Switched capacitor divider circuit.

4.1 Principle of Operation

To analyze the function of the SC divider, each phase has to be considered separately and the steady state of the circuit has to be determined with respect to charge conservation.
In phase Φ_1, the SC divider can be represented as shown in figure 4.1.1.(a). The charge in each capacitor is given by

$$\begin{aligned} Q_1^{'} &= C_1 V_2 \\ Q_2^{'} &= 0. \end{aligned} \tag{4.1.1}$$

In phase Φ_2, the SC divider can be represented as shown in figure 4.1.1.(b). The charge in each capacitor is given by

$$\begin{aligned} Q_1^{''} &= C_1(V_1 - V_{out}) \\ Q_2^{''} &= C_2 V_{out}. \end{aligned} \tag{4.1.2}$$

By applying charge conservation, the following condition can be stated

$$\begin{aligned} \Delta Q_1 &= \Delta Q_2 \\ C_1(V_2 - V_1 + V_{out}) &= C_2 V_{out} \end{aligned} \tag{4.1.3}$$

where $\Delta Q = Q^{'} - Q^{''}$. From (4.1.3) the gain of the SC divider can be found to be

$$V_{out} = (V_1 - V_2)\frac{C_1}{C_1 + C_2} \tag{4.1.4}$$

therefore dividing the voltage difference at the input of the circuit.

(a) sample phase Φ_1 (b) amplification phase Φ_2

Figure 4.1.1: Representation of the SC divider in different phases.

In phase Φ_3, C_2 charges the sampling capacitor of the subsequent ADC. The steady state of the system is reached when the voltage at the sampling capacitor equals V_{out}.

With the transition from phase Φ_3 to Φ_1, C_2 has to be discharged to $0\,V$ and C_1 has to be charged to V_2. If the system is in steady state, it is unnecessary to discharge C_2 over S_1. By introducing an additional phase Φ_4, in which the node V_{in} is connected to V_2, C_1 gets charged over C_2 and will cause V_{out} to drop to $0\,V$. This can be concluded by realizing that this transition is the same as the transition from Φ_1 to Φ_2, only in reverse order. The resulting system with the additional phase is depicted in figure 4.1.2.

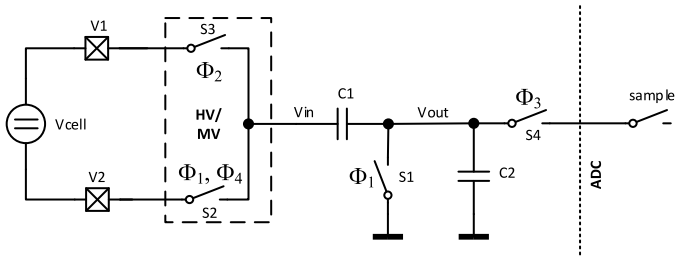


Figure 4.1.2: Switched capacitor divider circuit with modified switching.

To elaborate on the discussion, simulations with ideal components have been made, to compare the two presented switching schemes. The result is shown in figure 4.1.3.
The only difference between the simulations is that for case one, S_1 and S_2 are conducting during phase Φ_1 and Φ_4 and in case two, S_1 is conducting during phase Φ_1 and S_2 is conducting during phase Φ_1 and Φ_4.
Case two shows a clear improvement in settling time and by switching the system as described, no unnecessary charge transfer has to happen and the system can be clocked at a higher clock speed.

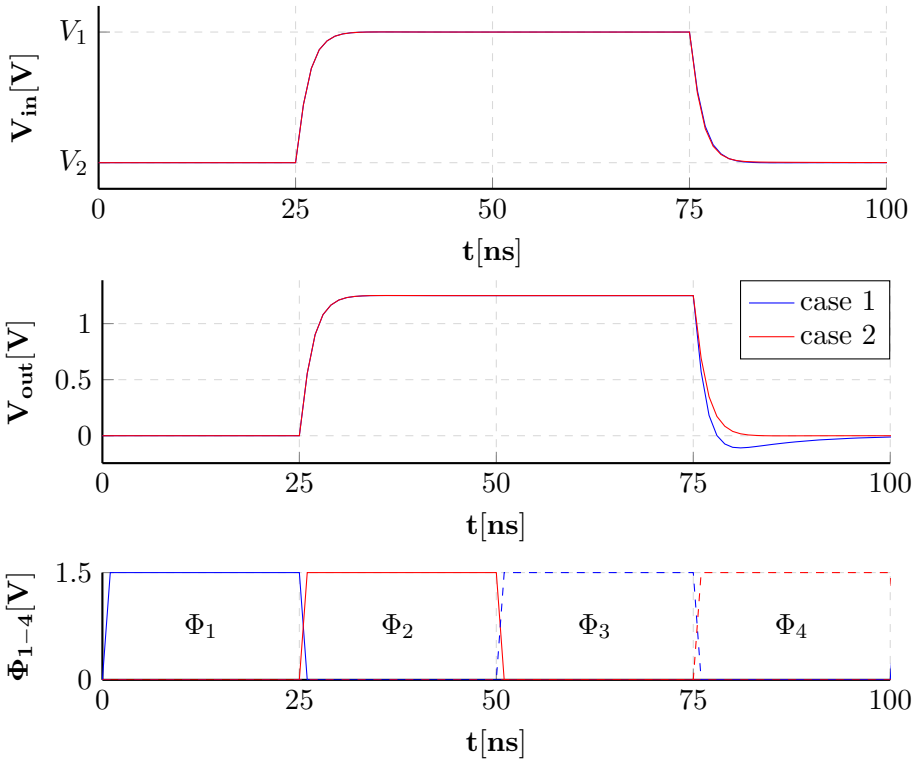
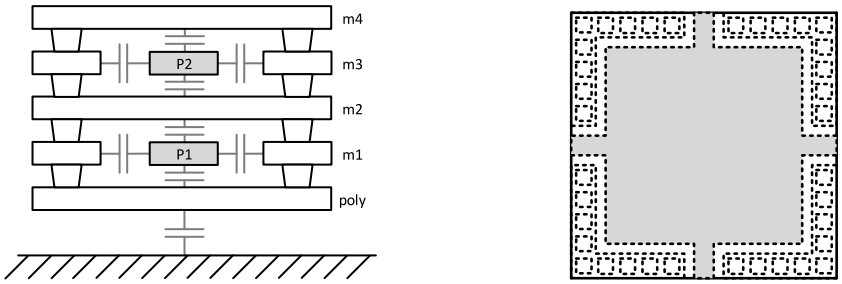


Figure 4.1.3: Comparison of the two switching schemes.

4.2 Parasitics

To minimize the gain error of the system, a careful analysis of the parasitic capacitances in the circuit has been made.
Any parasitic capacitance from node V_{in} towards ground does not cause an error, because it is always charged by one of the low impedance sources V_1 or V_2 depending on the phase of the circuit. Unfortunately any parasitic capacitance from node V_{out} towards ground is in parallel to C_2 and causes a gain error.

One design approach, to minimize the parasitic capacitance connected to the node V_{out}, is to use a capacitor that has inherently no parasitic capacitance associated with one of its plates. By connecting both capacitors C_1 and C_2 with this low parasitic plate to the node V_{out}, the gain error is minimized.
A possible implementation of this concept is depicted in figure 4.2.1. The inner plates P_1 and P_2 are surrounded by conductors as shown in the side view (a) and the top view (b). The outer shell, which has all remaining parasitic capacitance attached to it, is used as the bottom plate and the two inner plates, connected together are used as the low parasitic top plate.



(a) Side view. (b) Top view.

Figure 4.2.1: Unit capacitor with parasitic suppressed top plate.

Due to the parasitic wiring capacitance, a residual gain error is going to occur and further compensation will be necessary. To compensate any arising gain error, a compensation capacitor C_{comp} in parallel to C_1 could be used, as shown in figure 4.2.2. Unfortunately the value of this compensation capacitor can only be determined after layout extraction.

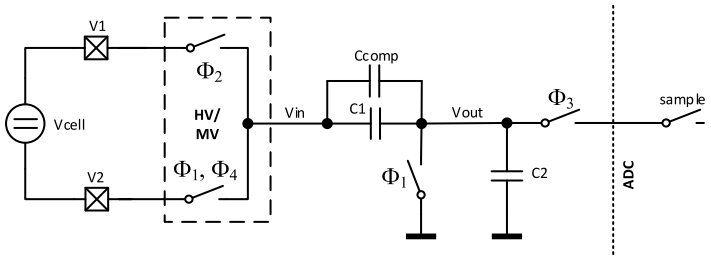


Figure 4.2.2: Switched capacitor divider circuit with gain compensation.

If a compensation capacitor has to be used anyway, the most effective solution would be to use the most suitable and area effective capacitor, without considering parasitic capacitance and to size the compensation capacitor after the layout is finished and an extraction has been performed.
Now the overall gain of the system is then given by

$$V_{out} = (V_1 - V_2)\frac{C_1 + C_{comp}}{C_1 + C_{comp} + C_2}. \tag{4.2.1}$$

4.3 Precharging

To reduce the settling time of the system, without increasing the capacitance of C_1 and C_2 and without increasing the switching frequency, a precharging phase rst has been introduced. During this phase the sampling capacitor of the subsequent ADC is charged to $\frac{V_{dd}}{2}$, therefore reducing the maximum settling time needed.
The alternative way to reduce the settling by increasing the capacitor sizes directly increases the consumed area, but also increasing the switching frequency increases the consumed area indirectly. To make use of the higher switching frequency, shorter time constants for charging and discharging are needed. This implies larger switches and again higher area consumption.

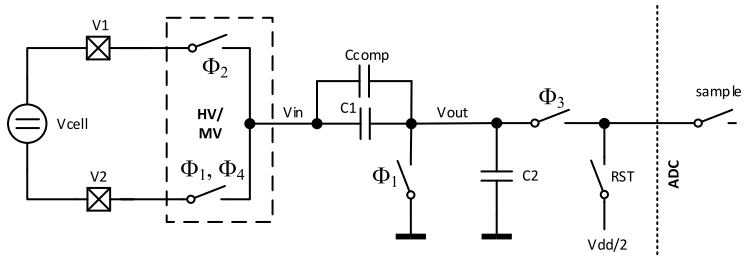


Figure 4.3.1: Switched capacitor divider circuit with precharging.

To compare the system with precharging phase to a system without it, simulations with ideal components have been made and the result is depicted in figure 4.3.2. During the *rst* phase the sampling capacitor of the subsequent ADC is charged to $\frac{V_{dd}}{2}$. This reduces the settling time for all cell voltages where the resulting output voltage is higher than $\frac{V_{dd}}{4}$. For cell voltages where the resulting output voltage is below $\frac{V_{dd}}{4}$, the settling time is increased. The overall reduction in settling time can be stated by analyzing the worst case condition, which appears for the maximum output voltage. By precharging the sampling capacitor, only half of the charge has to be transfered in the later phases. This effectively reduces the settling time by a factor of two. By closing the precharging switch only during the first two clock phases Φ_1 and Φ_2, no additional time is consumed by the precharging phase.

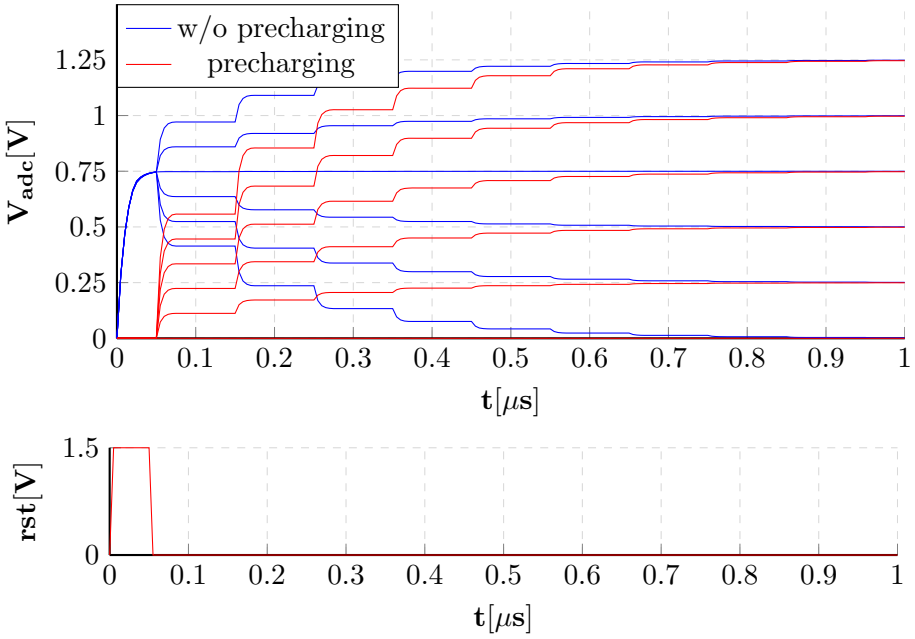


Figure 4.3.2: Comparison of the switching scheme with and without precharging.

4.4 Charge Injection

Due to the fact that almost all nodes of the circuit are high impedance nodes, charge injection has to be considered and minimized in all used switches.
A typical way to compensate charge injection in an NMOS switch is presented in [6] and depicted in figure 4.4.1. To switch off the pass device $N1$, the accumulated charge in the inversion layer has to leave the channel. For symmetrical impedances at source and drain, the charge is assumed

to split equally [6]. Therefore a symmetrical compensation is assumed to be most effective. The charge is proportional to the area of the device and is compensated with two dummy devices $N2$ and $N3$ of the same type and half the area of the pass device. The compensating devices are controlled with the inverse of the control signal of the pass device.

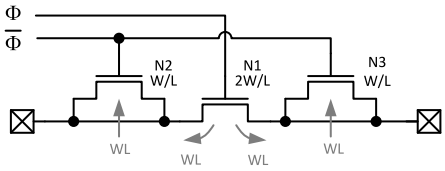


Figure 4.4.1: Charge injection compensation of an NMOS pass device [6].

The same design concept also applies to charge injection compensation for PMOS devices.

The precharging switch does not need to be charge injection compensated, because it is only injecting charge at the start of the sampling phase and has no effect on the steady state value of the system. Instead the design effort can be invested into other optimizations of the switch, like leakage current reduction.

4.5 Leakage

Due to the similarities in the designs, the considerations made in section 3.3 about the LV switches are still valid. The precharging switch is only closed during the phase rst and opened the rest of the sample time. Any leakage from this switch has therefore the biggest impact on the system. To accomplish a high off-resistance the AT-switch presented in [9] and described in section 3.3 is again used in the design.

The system reaches the steady state when the voltage at the sampling capacitor and the voltage at the node V_{out} are equal. It can be concluded that for the steady state, the voltage at the node V_{out} does not change between phases Φ_2 and Φ_3. This implies that no charge is flowing out of C_1 during the transition from phase Φ_2 to Φ_3 and that the top switch of the HV input switch can be switched on during phase Φ_2 and Φ_3. Resulting in the switching sequence depicted in figure 4.5.1. The node V_{in} is therefore always connected to one of the low impedance nodes V_1 or V_2 and the same principle as described in section 3.4 applies. Effectively canceling the effect of leakage from the HV input switch.

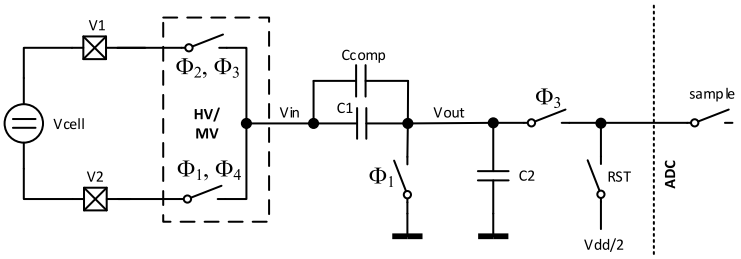
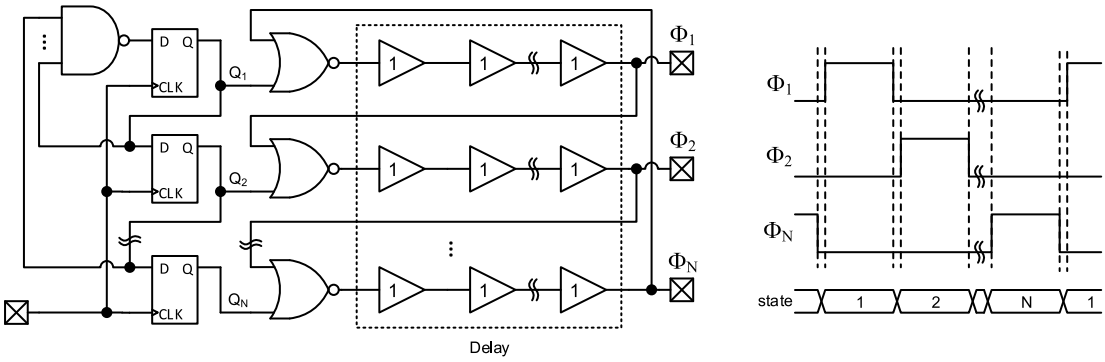


Figure 4.5.1: Switched capacitor divider circuit with modified switching to reduce leakage.

4.6 Control Signals

To generate the multiphase signal needed to control the circuit presented in this chapter, multiple control signals Φ_i are needed. The active state of the signals has to be non overlapping to ensure that the charge transfer during the phases happens as designed. The circuit depicted in figure 4.6.1 uses the same principle as the circuit presented in [24, 5.4.5], which has been described in section 3.5.2.
A state machine is formed by a shift register composed of multiple D-FFs. Only one of the shift register outputs Q_i is high at a time. The last state of the state machine is therefore reached when all outputs but the last are zero. This state is detected and the first FF is set to one on the subsequent positive clock edge, restarting the sequence.
To generate the non overlapping signals Φ_i from the signals Q_i, the same circuit as in section 3.5.2 is used. Again the signal path is blocked by NOR gates until the new state has propagated through the delay elements. The timing difference between subsequent phases is therefore two times the number of delay elements per signal path.



(a) schematic (b) generated signals

Figure 4.6.1: Generation of multiple non overlapping signals.

4.7 System Design

To design the system and to find suitable values for the capacitors C_1 and C_2 as well as to decide the sizes of the switches, multiple influences have to be considered.
To estimate the size of C_2 the condition for the number of needed charge transfers N can be used which is given by

$$N = \frac{C_s}{C_2} m \tag{4.7.1}$$

where C_s is the size of the sampling capacitor of the ADC and m is the required accuracy in bits. To keep both the sample time $t_s = \frac{N}{f}$ and the size of C_2 small, N should be large and a high switching frequency f should be used.
Unfortunately, the maximum switching frequency is limited by time constants determined by the on-resistance of the switches and the size of C_1 and C_2. Increasing the size of the switches would reduce their on-resistance but also the effects of charge injection and leakage would get more prominent.
A tradeoff has to be found between capacitor size, switch size, switching frequency and number of cycles.

4.8 Measurement System

4.8.1 Multiplexed Single Input SC Divider

From the sub circuit described in this chapter, a complete measurement system can be put together. One possible system is depicted in figure 4.8.1. Due to the fact that the system uses the ADC's internal sampling capacitor, it is not possible to construct a synchronous sampling system as presented in section 3.6.1. The design uses three identical and independent channels, which are multiplexed onto the input of the subsequent ADC. The circuit depicted in figure 4.8.1 is a simplified version, which does not show the modified switching scheme or other enhancement presented in this chapter. The independent channels make it simple to apply gain compensation as described in section 4.2. Of course precharging as described in section 4.3 can be applied to the system as well.

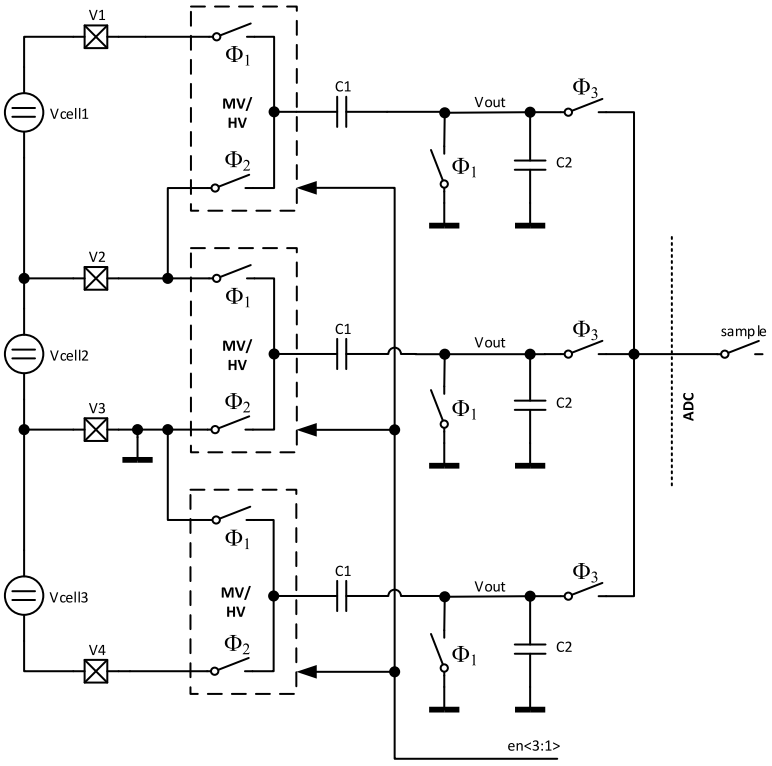


Figure 4.8.1: Multiplexed single input SC divider.

4.8.2 Multiplexed Multiple Input SC Divider

A second measurement system can be derived by combining all input channels into a single SC divider as depicted in figure 4.8.2. The input structure is the same as in the implementation described in section 4.8.1. To reduce the complexity of the system and to reduce the sources of error, the following scheme is used.
A channel gets selected by setting the corresponding $en < i >$ signal to high. If a channel is inactive, the HV input switch is connected to the lower input voltage of the channel. Only the active channel switches between the upper and lower input voltage.

The advantage of this method is that the additional channels do not cause any error due to leakage currents, because of the effect described in section 3.4.
The main benefit of the presented system is the reduced area consumption. One disadvantage

of the presented system is the cross coupling of the channels. This could limit the measurement accuracy of the system.

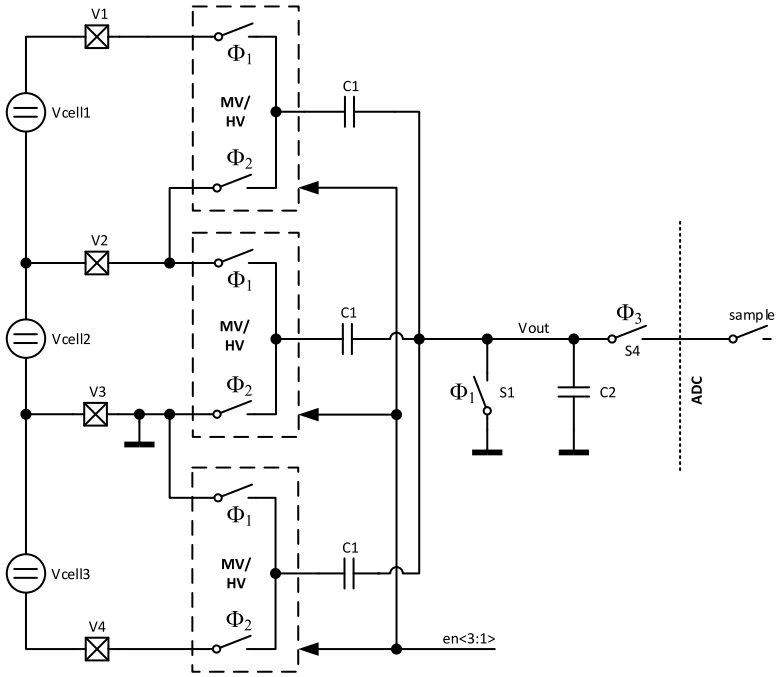


Figure 4.8.2: Multiplexed multiple input SC divider.

The circuit depicted in figure 4.8.2 is a simplified version, which does not show the modified switching scheme or other enhancements presented in this chapter. The implementation of precharging as described in section 4.3 is straightforward, but gain error correction as described in section 4.2 has to be applied individually to each channel. Matching the gain of all channels could be difficult and could proof to be a limiting factor of measurement accuracy.

Principle of Operation

To analyze the function of the multiple input SC divider presented in figure 4.8.2, each phase has to be considered separately and the steady state of the circuit has to be determined with respect to charge conservation.
For the derivation it has been assumed that the bottom channel is active and the other two channels are inactive.
In phase Φ_1, the SC divider can be represented as shown in figure 4.8.3.(a). The charge in each capacitor is given by

$$\begin{aligned} Q_2^{'} &= 0 \\ Q_1^{'} &= C_1 V_2 \\ Q_3^{'} &= C_3 V_3 \\ Q_4^{'} &= C_4 V_4 \end{aligned} \tag{4.8.1}$$

In phase Φ_2, the multiple input SC divider can be represented as shown in figure 4.8.3.(b). The charge in each capacitor is given by

$$\begin{aligned} Q_2^{''} &= C_2 V_{out} \\ Q_1^{''} &= C_1(V_2 - V_{out}) \\ Q_3^{''} &= C_3(V_3 - V_{out}) \\ Q_4^{''} &= C_4(V_3 - V_{out}) \end{aligned} \tag{4.8.2}$$

By applying charge conservation the following condition can be stated

$$\begin{array}{llll} \Delta Q_1 + & \Delta Q_3 + & \Delta Q_4 & = \Delta Q_2 \\ C_1(V_2 - V_2 + V_{out}) + & C_3(V_3 - V_3 + V_{out}) + & C_4(V_4 - V_3 + V_{out}) & = C_2 V_{out} \end{array} \tag{4.8.3}$$

where $\Delta Q_i = Q_i^{'} - Q_i^{''}$. From (4.8.3) the gain of the SC divider can be found to be

$$V_{out} = (V_3 - V_4)\frac{C_4}{C_1 + C_2 + C_3 + C_4} \tag{4.8.4}$$

therefore dividing the voltage difference at the input of the channel.

(a) sample phase Φ_1 (b) amplification phase Φ_2

Figure 4.8.3: Representation of the multiple input SC divider in different phases.

By assuming $C_1 = C_3 = C_4$ (4.8.4) can be rewritten to

$$V_{out} = (V_3 - V_4)\frac{C_1}{C_2 + 3C_1}. \tag{4.8.5}$$

To design the circuit with equal gain as the circuit described in section 4.8.1, the capacitance of C_2 has to be reduced by $C_1(N-1)$, where N represents the number of inputs. It can be concluded that the overall number of unit capacitors used is equal to the number of unit capacitors for one channel of the system presented in section 4.8.1.

4.9 Layout

Due to the reason stated in section 4.2, both systems described in section 4.8 are presented without a layout. As stated, a complete layout would need at least two redesigns and is therefore outside of the scope of this thesis. Because the design uses similar or even the same sub circuit blocks, as the designs presented in chapter 3, the implementation feasibility of the designs has been already demonstrated.

Chapter 5

Results and Discussion

In this chapter the simulation results of all presented designs are discussed and compared.

To evaluate the performance of the presented designs, the true measurement error has to be calculated. The input refereed measurement error V_{error} of the cell voltage measurement system is calculated with

$$V_{error} = V_{cell} - V_{out} \cdot gain \tag{5.0.1}$$

where $gain$ is the ideal gain of the system.

5.1 Synchronous Single Input SC Amplifier

The most relevant parameters of the extracted and simulated single input SC amplifier system presented in section 3.6.1, are listed in table 5.1.1.

	area		**gain**	$\mathbf{I_{sup,avg}}$		$\mathbf{V_{error}}$	
	value	unit		value	unit	value	unit
max	$3 \cdot 5245$	μm^2	$\frac{4}{16}$	589	μA	1.75	mV

Table 5.1.1: Characteristic parameters for the single input SC amplifier system for: 3 channels, $0.1\,V < V_{cell} < 5\,V$, $1.4\,V < Vdd < 1.6\,V, 8\,\mu A < I_{bias} < 12\,\mu A, -40\,°C < \vartheta < 125\,°C$, all 6σ process corners

From the simulation results for nominal operating conditions and process corners, depicted in figure 5.1.1 one can see how the control signals Φ_1 and Φ_2 relate to the generated output voltage V_{out}. Two subsequent sampling cycles of the same channel have been simulated and one can see that the circuit is able to operate with its full accuracy directly after startup. There are no preconditioning phases needed. The plot showing the output voltage clearly demonstrates the need for rail-to-rail output capability, to be able to convert the whole input voltage range. From the plot showing V_{error}, one can see that the requirements stated in section 2.2.1 are easily met in terms of accuracy and aperture time.

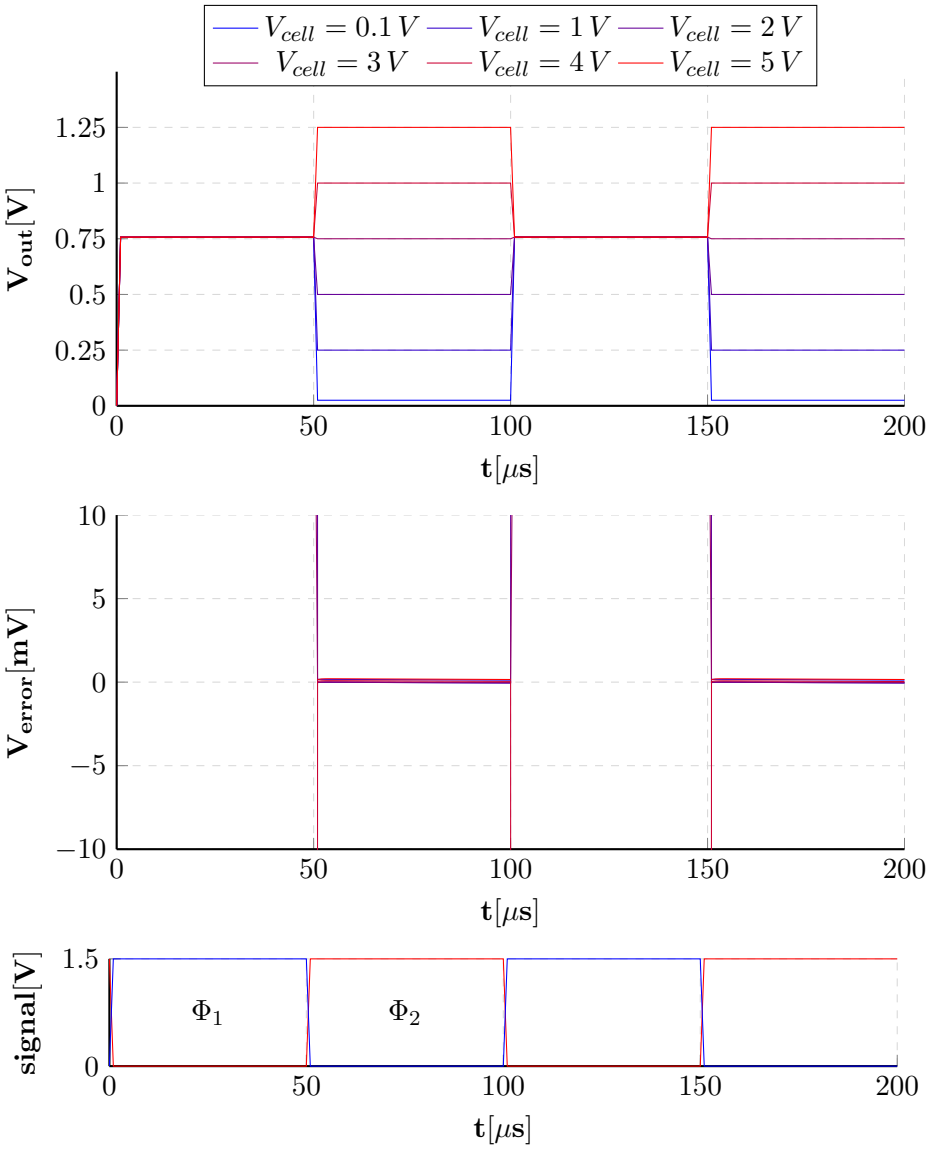


Figure 5.1.1: Simulation results for one channel of the synchronized sampling system, for different cell voltages.

5.2 Multiplexed Multiple Input SC Amplifier

The most relevant parameters of the extracted and simulated multiple input SC amplifier system presented in section 3.6.2, are listed in table 5.2.1.

	area		**gain**	$\mathbf{I_{sup,avg}}$		$\mathbf{V_{error}}$	
	value	unit		value	unit	value	unit
max	8840	μm^2	$\frac{4}{16}$	265	μA	1.62	mV

Table 5.2.1: Characteristic parameters for the multiple input SC amplifier system for: 3 channels, $0.1\,V < V_{cell} < 5\,V$, $1.4\,V < Vdd < 1.6\,V, 8\,\mu A < I_{bias} < 12\,\mu A, -40\,^{\circ}C < \vartheta < 125\,^{\circ}C$, all 6σ process corners

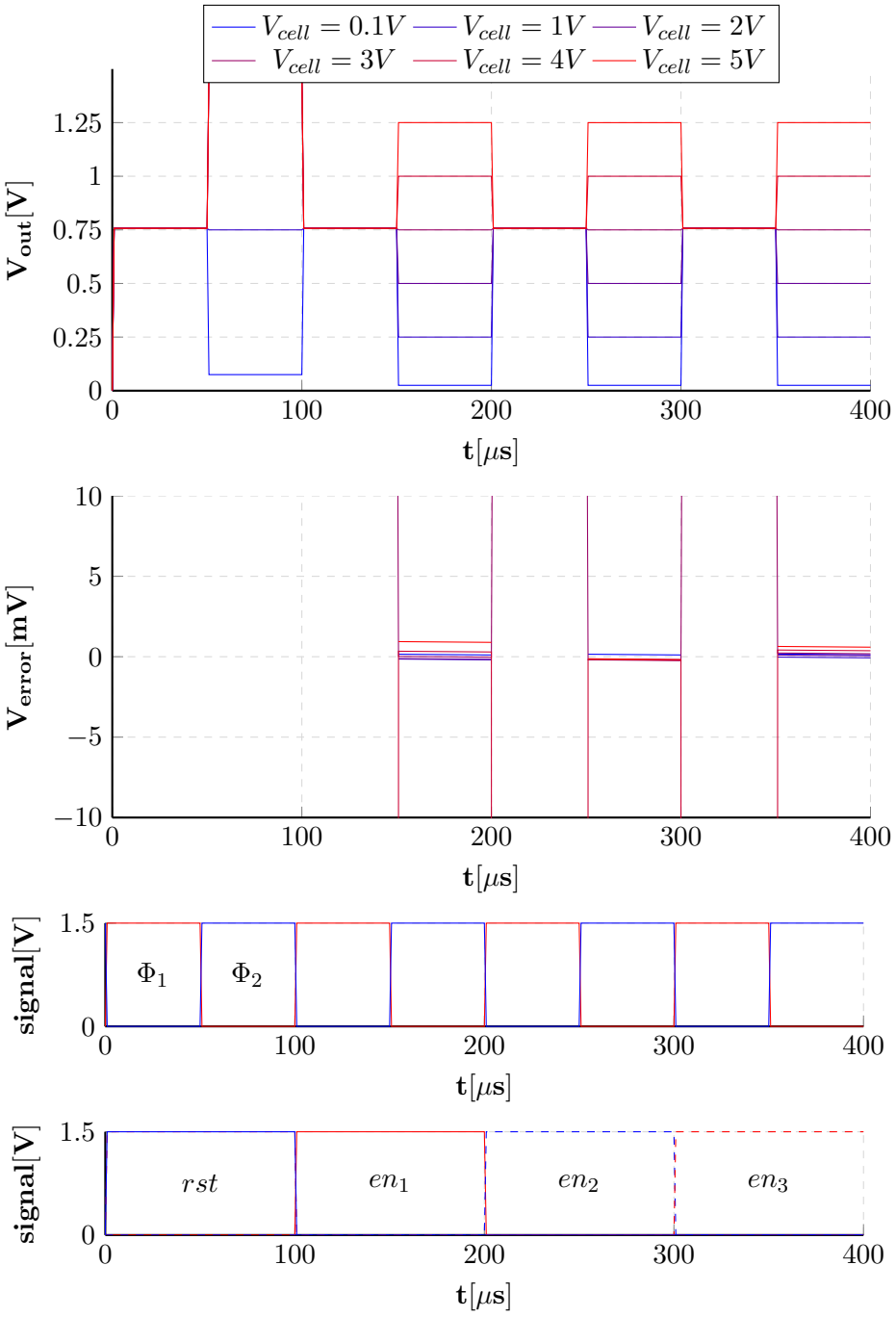


Figure 5.2.1: Simulation results for the multiple input SC amplifier system, for different cell voltages.

In section 3.6.2 the claim has been made that for the multiple input SC amplifier system, the inactive channels have no influence on the active channel which is currently sampled. From simulations made, the conclusion has been reached that this claim is only true after all channels have been sampled at least once. This is due to the fact that the respective capacitor C_1 of the channel has to be charged first. To eliminate this behavior an additional phase rst has been introduced to activate all channels simultaneously and charge all capacitors C_1. This reduces the needed preconditioning time to one sample cycle and makes it independent of the number of channels.

The result of the simulation with the modified phasing is shown in figure 5.2.1 and has been generated for nominal operating conditions and process corners. The plots show the introduced rst phase after startup and the subsequent sampling of all input channels. As for the synchronous sampling system, one can see that the requirements stated in section 2.2.1 are easily met in terms of accuracy and aperture time.

5.3 Multiplexed Single Input SC Divider

The single input SC divider system presented in section 4.8.1 has been simulated and the results are presented in table 5.3.1 and figure 5.3.1.
Due to the fact that for the single input SC divider no layout has been designed, the area consumption is only estimated.

	area		**gain**	$\mathbf{I_{sup,avg}}$		$\mathbf{V_{error}}$	
	value	unit		value	unit	value	unit
max	$3 \cdot 6000$	μm^2	$\frac{4}{16}$	77.6	μA	2.29	mV

Table 5.3.1: Characteristic parameters for the single input SC divider system for: 3 channels, $0\,V < V_{cell} < 5\,V$, $1.4\,V < Vdd < 1.6\,V$, $-40\,°C < \vartheta < 125\,°C$, all 6σ process corners

The simulation results depicted in figure 5.3.1 have been generated by using a clock frequency of $20\,MHz$ and the input sampling capacitance of the ADC has been assumed to be $1\,pF$. From the result shown, it is clear that the high frequency switching causes a substantial amount of noise at the input of the ADC and that the generated noise has to be considered as a source of *electro magnetic emission* (EME).
From the plot showing V_{out}, one can see that with this system it is possible to process input voltages equal to $0\,V$. Again, from the plots shown one can see that the requirements stated in section 2.2.1 are easily met in terms of accuracy and aperture time.

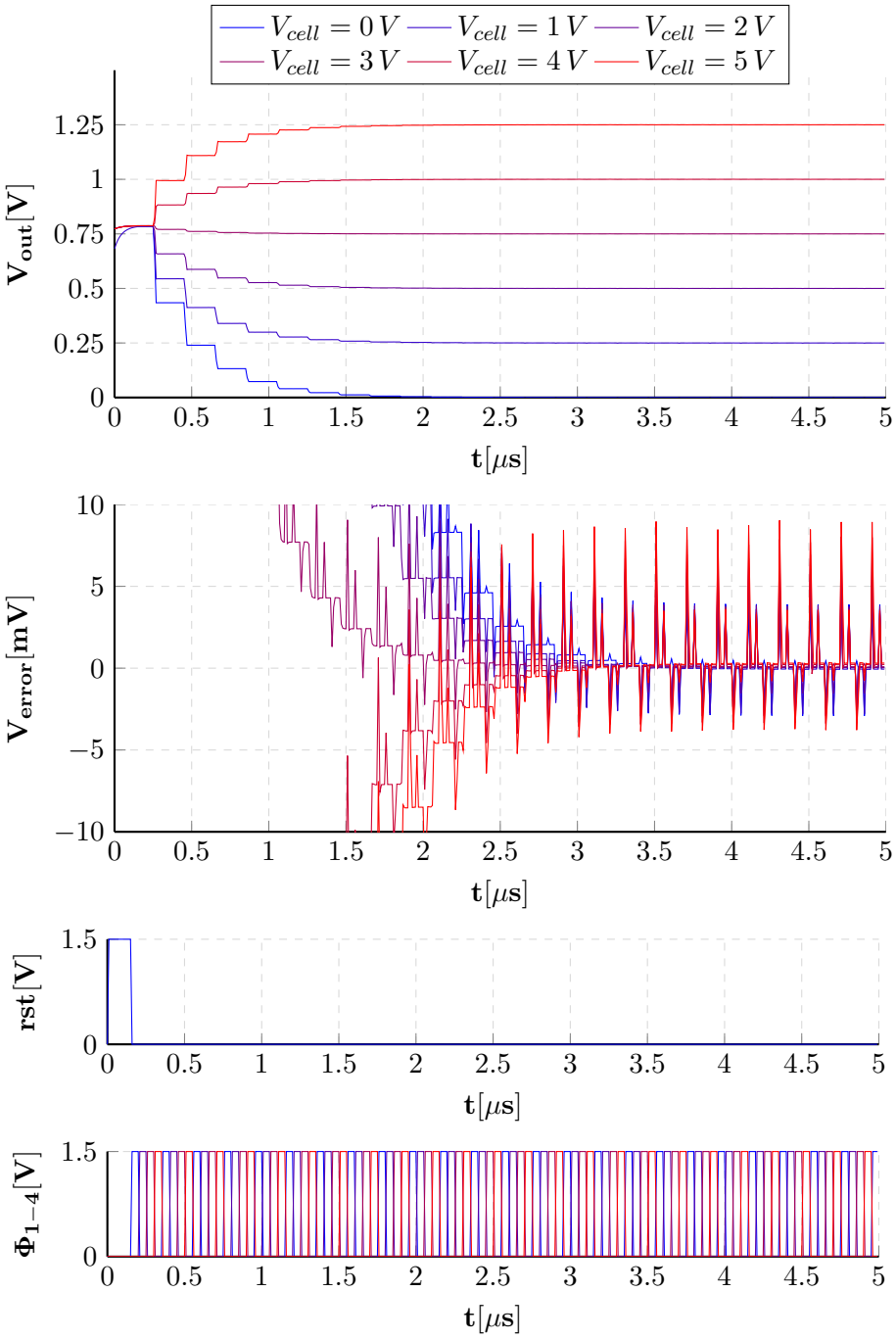


Figure 5.3.1: Simulation results for one channel of the single input SC divider system, for different cell voltages.

5.4 Multiplexed Multiple Input SC Divider

The multiple input SC divider system presented in section 4.8.2 has been simulated and the results are presented in table 5.4.1 and figure 5.4.1. Due to the fact that for the multiple input SC divider no layout has been designed, the area consumption is only estimated to be smaller by a factor of two compared the single input SC divider.

	area		gain	$\mathbf{I_{sup,avg}}$		$\mathbf{V_{error}}$	
	value	unit		value	unit	value	unit
max	9000	μm^2	$\frac{4}{16}$	48.08	μA	2.43	mV

Table 5.4.1: Characteristic parameters for the multiple input SC divider system for: 3 channels, $0\,V < V_{cell} < 5\,V$, $1.4\,V < Vdd < 1.6\,V$, $-40\,°C < \vartheta < 125\,°C$, all 6σ process corners

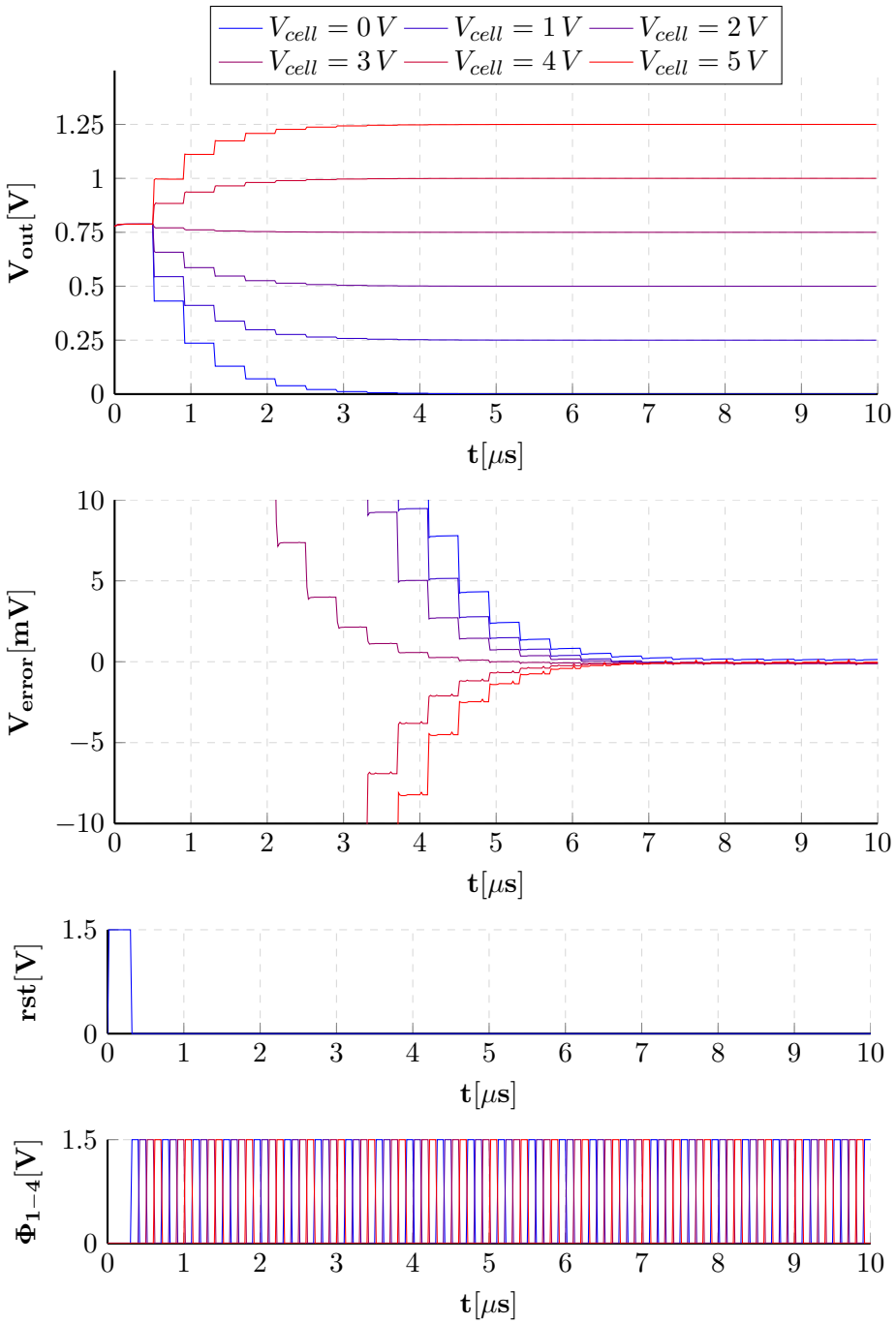


Figure 5.4.1: Simulation results for the multiple input SC divider system, for different cell voltages.

The simulation results depicted in figure 5.4.1 have been generated by using a clock frequency

of $10\,MHz$ and the input sampling capacitance of the ADC has been assumed to be $1\,pF$. The plots depicted are very similar to the plots generated for the single input SC divider, shown in figure 5.3.1. The reasons that the switching noise is reduced, compared to the single input SC divider, is the reduced switching frequency and size of capacitor C_2 as described in section 4.8.2.

5.5 Discussion

To enable a comparison of the different designs, a *figure of merit* (FOM) has been introduced as a parameter to characterize the designs without considering functional differences. The parameter is given by

$$FOM = P \cdot area \cdot V_{error}. \tag{5.5.1}$$

where P is the consumed power. An ideal system would therefore have a FOM of zero.

A brief parametric comparison of the presented designs has been made in table 5.5.1, where the FOM has been normalized.

	sampling type	**area**		**P**		**V_{error}**		**FOM**
		value	unit	value	unit	value	unit	
single input SC amplifier	synchronous	15735	μm^2	942	μW	1.75	mV	1
multiple input SC amplifier	multiplexed	8840	μm^2	424	μW	1.62	mV	0.234
single input SC divider	multiplexed	18000	μm^2	124	μW	2.29	mV	0.197
multiple input SC divider	multiplexed	9000	μm^2	72	μW	2.43	mV	0.061

Table 5.5.1: Parametric comparison of the presented measurement systems.

From the requirements stated in section 2.2.1, the conclusion has been reached that due to relatively large required aperture time of $10\,ms$, there is no need to employ synchronized sampling. Because the achievable measurement accuracy of all developed systems is in the same range, the selection should be based on power and area requirements.

The presented multiplexed designs are similar in terms of FOM, but the functional differences have to be considered carefully.
On one hand, the SC amplifier provides a low impedance source and therefore makes the measurement system independent from the subsequent ADC. On the other hand, it depends on bias voltages and currents and makes the measurement system less flexible and robust.
The SC divider does not use an amplifier and therefore is not dependent on any reference voltages or currents and consumes very little power. One disadvantage of the SC divider is the dependency on the size of the sampling capacitor of the subsequent ADC and the need for at least one design iteration due to the necessary gain error correction after layout extraction.

Chapter 6

Conclusion

6.1 Summary

The goal of this thesis was to develop a suitable input multiplexer and attenuator to be used in a battery cell voltage monitoring system.
The system uses the cross cell measurement approach proposed in [7] and therefore has to have an input range well below and above the supply rail of the monitoring IC. Current publications in this field only present methods to monitor multiple cells above circuit ground and are often of limited accuracy.

Multiple types of HV input multiplexers with attenuation have been developed and their implementation feasibility has been demonstrated.
It has been shown that the system requirements can be met by using a simple and cheap 130 nm CMOS process with a basic HV extension and that there is no need for *shallow trench isolation* (STI) or junction isolated areas as available in a typical *bipolar CMOS DMOS* (BCD) process or by designing in a *silicon on isolator* (SOI) process, as in [3] [13].

This thesis demonstrates multiple multiplexed and synchronous sampling systems which can be employed based on system requirements. All of the designs have been designed with respect to manufacturability and have been optimized in terms of area and therefore cost. The presented designs are able to operate with low supply voltages and compared to previous designs [3] [13], the power consumption has been reduced drastically.
To develop a system, which is independent of bias currents and voltages, a new approach to an HV input multiplexer has been proposed. The resulting design is based on an SC divider and is very flexible in terms of gain and number of channels. It does not use an amplifier and is therefore simpler and more robust against stability problems. Due to the reduction in complexity, the sources of errors and faults have been reduced as well.

6.2 Outlook

To implement the presented designs and concepts in future projects, more design effort has to be invested into finding applicable input protection structures. Standard *electro static discharge* (ESD) protection elements and concepts, available in the used CMOS process, are not suitable and cannot handle the required input voltage range of the system. A promising solution is presented in [11], which demonstrates a bi-directional anti-series ggNMOS ESD clamp.
Additionally, a layout for the SC divider based design has to be designed to show that the area estimation made is valid.

The designs presented in this thesis are intended as part of a BMS, therefore much attention will be required in terms of system integration and influence on other precision measurement systems of the BMS, like cell impedance spectroscopy.
Due to the fact that the intended use of the presented designs is in a distributed BMS systems, the need for inter module communication arises. This leads to noise and *electromagnetic compatibility* (EMC) requirements for the system, which have to be considered in this work.

Acronyms

BCD	bipolar CMOS DMOS
BMS	battery management system
CMR	common mode rejection
CS	common source
DIBL	drain induced barrier lowering
EMC	electromagnetic compatibility
EME	electro magnetic emission
ESD	electro static discharge
FOM	figure of merit
GBWP	gain bandwidth product
HV	high voltage
LDE	layout dependent effect
LV	low voltage
MV	medium voltage
OPA	operational amplifier
OTA	operational transconductance amplifier
PM	phase margin
PSR	power supply rejection
SC	switched capacitor
SOA	save operating area
SOC	state of charge
SOH	state of health
SOI	silicon on isolator
SR	slew rate
STI	shallow trench isolation
VPP	vertical parallel plate
WPE	well proximity effect

List of Figures

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