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Characterization and Evaluation of Multi-Layer Ceramic Capacitors

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Affidavit

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Abstract

This master thesis is paying attention to the characterization of multi-layer ceramic capacitors.

Influences of different manufacturers or dielectric material are observed. These results are getting compared to the, from the manufacturer, provided characteristics.

Next step is to connect different capacitors as a parallel circuit and evaluate which connections are productive and which connections should be avoided regarding the overall impedance characteristic.

Based on these preliminary findings, a whole printed circuit board is examined. Furthermore the possible influence of board modifications (adding or bridging capacitors) is observed.

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1 Preface

1.1 Introduction

The idea for this master thesis arose right after completion of the so called electronic project [1], which is mandatory for the masters degree course. In this project, the research concept was to examine the propagation of electrostatic pulses (based on the human body model) and their impact on different (protection) structures.

This lead to the idea of examining multi-layer ceramic capacitors. Those (filter and protection) components are often chosen to complete the equipping of the printed circuit board.

The examination of the capacitors is planned to be in several steps build on each other.

But before the measurement sections, there is a section with a lot of background theory, which will be needed in the following sections.

The first analysis step is to characterize single capacitors.

This is done by measuring the characterization of the capacitor via a vector network analyzer and comparing it to the provided characteristic by the manufacturer of the capacitor. In this context, it was also analyzed, how realistic the provided equivalent circuit diagram of this capacitor is and how to create a specific one in the advanced design system (ADS) software.

Next discussion point is the comparison of "similar" capacitors. There will be a comparison between two 1nF capacitors of the same manufacturer, but with different dielectric material, which means, they are assigned in different classes. Another comparison will be between two identically constructed capacitors with the same value (100nF), but provided by different manufacturers. The third comparison will be between a standard X7R capacitor and a LLL capacitor, both 100nF and provided by the same manufacturer.

1 Preface

The next part of the thesis is build up from the previous described section.

The first part of this section is dominated by various combinations of connecting two capacitors parallel.

As first measurement two similar capacitors are connected parallel. Then, there will be two comparisons between a 100nF and a 1nF capacitor. First the two capacitors are X7R types. In the second measurement, the 100nF capacitor will be the same X7R type and the 1nF capacitor will be a C0G type.

The second part of this section is composed of parallel circuits of four different capacitors.

In the previous mentioned electronic project, the wiring related to an integrated circuit also was a topic. There the idea was to chose four capacitors (1 μ F, 100nF, 1nF and 100pF) and slot them in ahead of the integrated circuit. This idea was picked up to analyze the characteristic of such a circuit. The 100pF capacitor is of a C0G type, the 1 μ F and the 100nF capacitors are of X7R types and the 1nF capacitor is a X7R type for the first and a C0G type for a second comparison measurement.

In the last measurement section, the idea is, to analyze a complete printed circuit board.

With bridging or adding capacitors it should be possible to influence the characterisitc of the board. This will be observed and discussed in this last measurement section.

1.2 Literature research

There are a lot of papers analysing capacitors one way or another.

The deration of ceramic capacitors under ESD stress is discussed in a paper from Germany [2]. In this paper, the verifying measurement is just composed of a measurement of the capacitors value.

Another paper [3] discusses the description of 0603 capacitors based on there impedance characteristics. One of the conclusions of this paper is, that capacitors with 0603 dimensions are not recommended as an ESD bypass

1.2 Literature research

mechanism and that a 0805 dimensioned capacitor will respond better to stressing by an ESD pulse. This paper also shows an equivalent circuit diagram for a capacitor, which will be used later in this thesis.

Further analysis of capacitors for ESD protection [4] is given by D. Pommerenke (among others). D. Pommerenke is one of the world-wide experts regarding EMC (in the broadest sense). In this given paper he compares two multi-layer ceramic capacitors (MLCC) with different dielectric materials, means with different characteristics. The comparison is between X7R (which will also be discussed in this thesis) and AEF capacitors.

But there are a lot more papers with valuable information regarding the characterisation, measurement and modelling of capacitors [5],[6],[7], [8], [9].

Two german publications [10], [11] are concentrating on parallel circuits of capacitors, a topic, which is also investigated in this thesis. English informations regarding parallel connected capacitors could be found in [12]

Information on the influence of the printed circuit board to the impedance characteristic is found in [13]. [14] discusses an experiment similiar like the approach in chapter 5.

Further information, which was valueable when writing this thesis, is found in [15], [16] and [17].

2 General information

This section serves as a short theoretical information resource, before starting with measurements and analyses.

2.1 Principles of a capacitor

There are a few different kinds of capacitors. Some of the, for this thesis relevant, distinguishing characteristics are discussed in the sections [2.1.1](#) - [2.1.3](#).

2.1.1 Different design

There are many different types of capacitors. A short description of the three big types is quoted in the following listing.

- Electrolytic capacitor
These capacitor types are polarized. A more precise description of the capacitors is depending on the type of metal, which is used as material for the anode. A big advantage of electrolytic capacitors against others is the possibility of quite big values of capacity in relation to their size.
- Film capacitor
The dielectric material of film capacitors are isolated plastic films. Those films get either reeled or layered. Due to the usage of different plastic materials, almost every characteristic is possible. But the disadvantages towards electrolytic and

2 General information

ceramic capacitors is a relatively large-sized design, high costs and the opportunity of self ignition.

- Ceramic capacitor

The dielectric material of these capacitors is made of ceramic. The exact composition of the isolating material defines the electrical properties and therefore the classification in the different categories, mentioned in section 2.1.2. Designed as multi-layer ceramic capacitors (MLCC), these capacitors are used most in electronics. This is the reason, why they have been chosen to be analyzed.

But all in all, all three mentioned capacitor types are developed in a way, in which they all show more or less similar properties and characteristics.

Multi-layer ceramic capacitors are the most spreaded capacitors yet and their structure is shown in figure 2.1. It is seen, that such a capacitor is build of several electrodes surrounded by a dielectric medium. This means, that a MLCC basically consists of various single ceramic capacitors.

This is a not to be scoffed advanted over other designs. Through the

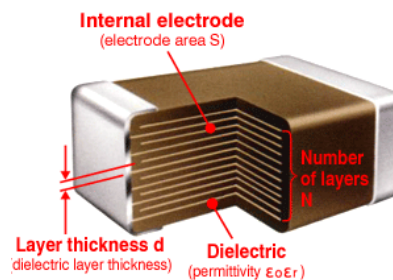


Figure 2.1: General structure of a MLCC [18]

multi-layer structure it is possible to get higher capacitance values without growing in size.

2.1.2 Different classes

As already mentioned in the listing before, the electrical characteristic is defined by the dielectric material. Depending on the material (therefore on

2.1 Principles of a capacitor

the properties), capacitors are assigned to different classes.

According to IEC 60384 – 8/9/21/22 [19] are there two (respectively three, but the third one is obsolete) different classes.

When considering EIA RS-198 [20], there are four different classes.

The only difference in the separation between the classes is, that class two of the IEC standard is separated into class two and class three in the EIA standard. Each last of the classes is describing barrier layer capacitances and these are not relevant any more.

Besides this extra separation of the second class, the two standards are similar.

For this paper, the IEC 60384 standard is used.

In general it is to say, the lower the class number, the better the overall characteristic, but the larger the package of a given capacitor. A few more comparison details are noted in the following listing:

- Class 1:
 - For example C0G capacitors, in industry they are called NP0 capacitors
 - Low temperature drift
 - Low aging, voltage coefficient, frequency coefficient, leakage, dissipation factor
 - Problem:
 - * Size (strong increasing at values greater than $0,01\mu\text{F}$)
 - * Lower voltage breakdown by higher dielectric constants
- Class 2/3:
 - For example the examined X7R
 - Poor temperature drift
 - High voltage coefficient, frequency coefficient, dissipation factor, aging rate
 - Not that good high frequency characteristic: if above 1MHz, there is a drop in the capacitance value and a rise in dissipation
 - Advantage in size and costs

2 General information

2.1.3 Different package sizes

There are all kinds of different sizes for capacitors.

The one big differentiation is between wired components and components in SMD technology.

SMD components are also available in all sorts of dimensions.

The package size of the capacitors is expected to influence the impedance characteristic.

In figure 2.2 is an exemplary waveform of a 100nF capacitor illustrated. In theory the first part of the waveform until the resonance frequency f_r is defined by the value of the capacitor. The part of the waveform after the resonance frequency is determined by the parasitic inductance. The smaller the value of this parasitic inductance, the higher the resonance frequency. To get a smaller parasitic inductance, a smaller package is helpful.

Another reduction of the inductivity value should be possible by placing the contacts on the long side of the SMD component. This possibility is examined with the LLL capacitor by Murata.

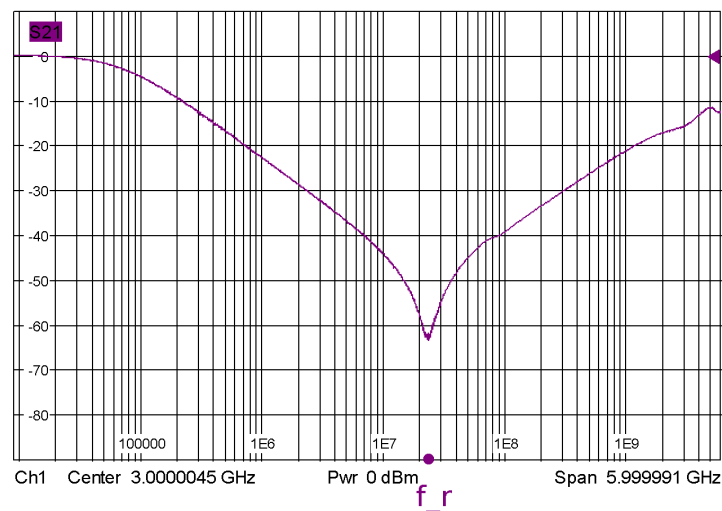


Figure 2.2: Exemplary characteristic of a 100nF ceramic capacitor

The dimension of the capacitors was almost mandatory to be chosen with

2.2 Series resonance vs. parallel resonance

0805, because of the conclusions of the already mentioned paper (see section 1.2) from Germany [2].

2.2 Series resonance vs. parallel resonance

When considering the impedance characteristic of a capacitor, an inductance and a resistor are also always to consider (as seen later in figure 3.5) and so the situation of a series resonance of those three components is given.

This means, the impedance characteristic of a single ceramic capacitor shows not just the characteristic of a capacitor, but also, starting at the resonance frequency, the characteristic of an inductance, as seen in figure 2.2. When neglecting the pure ohmic resistance, the impedance is calculated with following equation, where R_C and R_L describes the real parts of the components and X_C and X_L the imaginary parts:

$$\underline{Z} = (R_C + R_L) + j(X_C + X_L) \quad (2.1)$$

At the resonance frequency, the imaginary part should be zero (capacitor influence is decreasing, inductance part just rising):

$$\text{Im}\{\underline{Z}\} = 0 \quad (2.2)$$

That implies an impedance at resonance frequency, which is very low:

$$\underline{Z}_{R_s} = \text{Re}\{\underline{Z}\} = R_C + R_L \quad (2.3)$$

Usually, the low-impedance scope is not wanted to be concentrated at one (resonance) frequency, but rather be spread over a wider frequency range. This is realized by connecting more capacitors in parallel, which leads to parallel resonances.

The characteristics of the single capacitors all look quite similar (of course, with little deviations regarding resonance frequency or exact course of the curve). By arranging the components in parallel the characteristic curves are multiplied with each other, as seen in the example figure 2.3.

It is obvious, that there is a peak in the purple waveform between the two series resonance frequencies of the single capacitors. This, not wanted, peak

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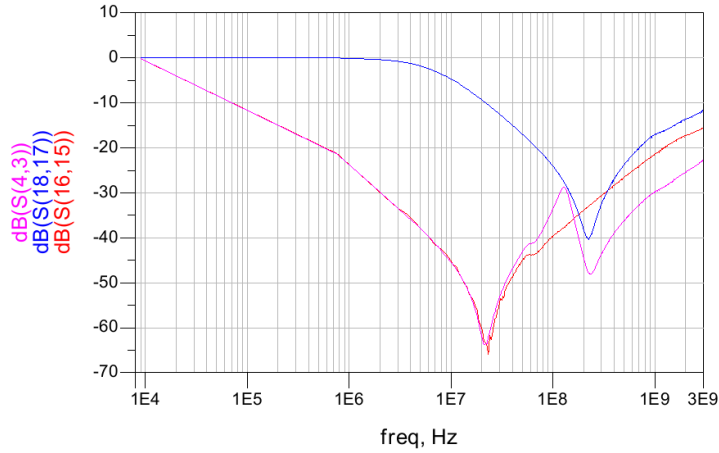


Figure 2.3: Example of a parallel resonance

is developed because one capacitor is already working as an inductance (at a frequency, which is higher than its own resonance frequency) and the second capacitor is still working as a capacitor. That is also reflected in following equations (2.4 and 2.5).

The frequency that shows this effect is the resonance frequency of the parallel circuit. The impedance of a parallel circuit is calculated slightly different and with simplification (R_C is very small and therefore neglected) it is calculated like:

$$\underline{Z} = \frac{(R_L X_C^2) + j(R_L^2 X_C + X_C X_L (X_L + X_C))}{R_L^2 + (X_L + X_C)^2} \quad (2.4)$$

Equation 2.2 of the series circuit is also valid for the resonance frequency of the parallel circuit.

That is given, when the numerator of the fraction is zero and the denominator of the fraction is unequal zero. This leads to a very high impedance at the resonance frequency:

$$\underline{Z}_{Rp} = Re\{\underline{Z}\} = \frac{R_C^2 R_L + R_C R_L^2 + R_C X_L^2 + R_L X_C^2}{(R_C + R_L)^2 + X_L + X_C^2} \quad (2.5)$$

The two equations 2.3 and 2.5 at the resonance frequencies explain the course of the characteristic curve.

2.3 Measurement preparation work

The general goal when using capacitors in parallel as filter or decoupling elements is, to keep the impedance Z_{Rp} as low as possible.

2.3 Measurement preparation work

To measure the characteristic of a capacitor, besides the correct equipment, a fitting wiring of the capacitor is needed.

In reference of Power Integrity, written by Steven M. Sandler [21], the chosen measurement method is the two-port shunt measurement method, as seen in figure 2.4.

On the left and on the right end of the circuit are the 50Ω terminating resistors. In between, the DUT (device under test) is pictured. This stands for the capacitor, which should get characterized.

To measure the characteristic of a capacitor, a Network Analyzer (described

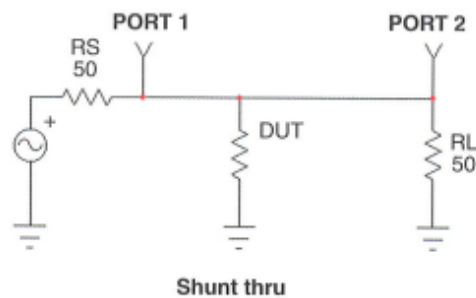


Figure 2.4: Circuit diagram by Steven M. Sandler [21]

in section 2.4) is needed. At the measurements for this thesis, the Network Analyzer measures with a SMA connector. But there are all connectors possible, which exists as an adapter to a N-connector. To measure based on the two-port shunt measurement method, two SMA connectors are needed (one for each terminal). The SMA connectors are build right-angled. That is reasonable due to strain relief during the measurement process. When using straight connectors, it is very likely that one of the solder joints, which

2 General information

connect the two plugs, and/or even the capacitor itself will break. To measure the capacitor, it needs to get soldered in the correct way to measure based on the two-port shunt measurement method. This is seen in figure 2.5. The capacitor is seen in the green circle and is soldered between the signal path and the GND path.



Figure 2.5: Example DUT mounted on two SMA connectors

2.4 Hardware in use

The easiest way to consider the usability of a capacitor for a certain purpose, is to analyse the impedance characteristic of the contemplable capacitor. There are more possible ways to get such a characteristic for a capacitor. The measurement could be done with a vector voltmeter, for example. A member of the Institute of Electronics already worked with this technique to analyze capacitors [22]. Now, for internal comparison reasons, a Rohde & Schwarz Network Analyzer (R&S ZVL Network Analyzer 9kHz...6GHz) is used to get the impedance characteristics. A little howto to the Network Analyzer is written in the following section.

2.4.1 Measurement HOW TO

The most important part of the whole measurement is the calibration of the measuring cables. Due to the decision of measuring with the two-port

2.4 Hardware in use

methode, both possible measurement cables have to be calibrated.
But before starting the calibration, some preferences need to be set:

- Mode button
To set the measurement device as a Network Analyzer (Signal Analyzer would also be possible).
- Center button
To enter the start and stop frequency and the power.
With the upcoming measurements, the frequency range is 9kHz - 3GHz and for the power -10dBm is chosen.
- Sweep button
To enter sweep type and number of points, as also to turn on averaging and set the average factor.
The sweep type is set to logarithmical and number of points is set to the maximum value, which is 4001. The turned on averaging should calculate over 10 single measurements.

If one of these settings is forgotten or changes during the measurement, the whole calibration needs to be done again.

To perform a calibration, the so-called "R&S TOSM Calibration Kit" (see figure 2.6) is needed.

There are ways to accomplish a calibration, all with a difference in time-



Figure 2.6: Calibration kit belonging to the Institute of Electronics

consumption and accuracy.

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To start the most precise calibration (which should always be chosen), the Cal button has to be pushed. Then the "Two-Port P1 P2" selection and afterwards the TOSM possibility should be chosen. To finish the basic calibration the commands on the screen needs to be followed. Therefore the extensions of the calibration kit are needed. The screen of this process is illustrated in figure 2.7. After connecting the correct port of the kit to the currently active cable, a click on the corresponding spot at the screen starts the calibration process. As seen in figure 2.7, this has to be done seven times. Three times per terminal (Open, Short and Match) and once as a connection (Through) of both cables.

After finishing this basic calibration, the measurement extensions need to

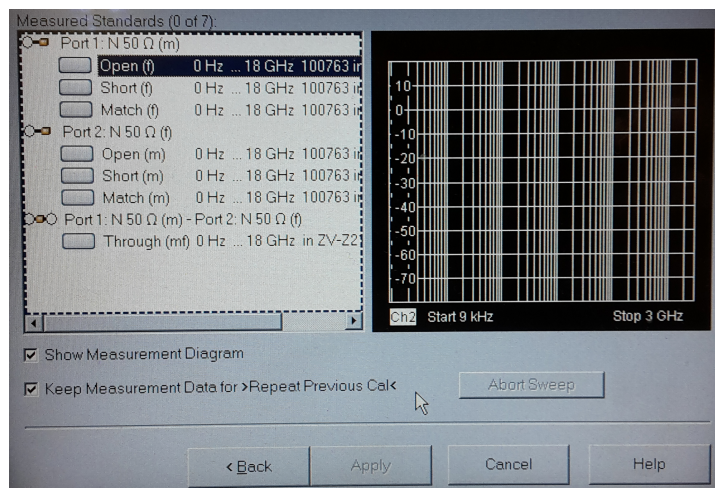


Figure 2.7: Calibration screen of the Network Analyzer

screw into the measurement cables. These extensions are seen in figure 2.8 and are needed to guarantee that just the capacitor is measured and that there are no distortion of the measurement cables or the extensions or the SMA connectors (zero adjustment). This offset calibration (to be found in the Cal settings, at "Port extensions") has to be done for both measurement cables. After pressing the Meas button, it's possible to switch between the different ports via a selection at "traces".

After that, the calibration is finished.

To verify the calibration the smith chart display is recommended.



Figure 2.8: Required extensions for measurement (left) and calibration (right)

With the File button it is possible to save the calibration. For the measurement itself it is important, to guarantee, that the measurement setup is unmoved during the whole measurement. There are two ways to save the results of the measurement. First the possibility of saving the resulting waveform as a screenshot. This is realized with the "Print screen" option after pushing the Print button. The second saving technique is to use the export data option, which could be found in the import/export data setting after pushing the traces button. The file with the data could be saved in different types, for example as *.csv (comma-separated-value file) or as *.s2p (touchstone file). In this thesis the latter file type will be used, because of the reusability in the analyzer software.

2.4.2 Measurement theory

In the context of this thesis, the measured capacitors are treated as a two-port network.

An example image for such a network is illustrated in figure 2.9. Figure 2.10 shows the two possible connectivities inside the black box of figure 2.9. Either the capacitor is connected in series (C1) or the capacitor is connected against ground (C2). The latter one is chosen for the measurements in this thesis.

All voltages and currents are described by a forerunning respectively reflected wave. The context of these waves is depending on the wiring of the two-port network. In this case, it is depending on the capacitor.

2 General information

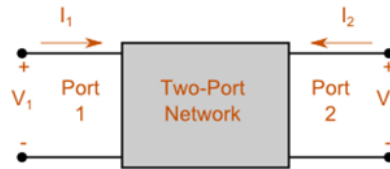


Figure 2.9: Example of a two-port network [23]



Figure 2.10: Two possibilities for the blackbox

Such correlation allows a consistent description of components. The relations between forerunning respectively reflected wave defines the characterization by S-parameters. One advantage from S-parameters towards Y- or Z-parameters is, that the other parameters need an idling oder a short at the input or the output for measurement. That is not necessary for measuring the S-parameters. Another advantage is, that S-parameters are measured considering the terminating resistance, which is also there in the usual mode of operation.

The measured S-parameter waveforms are used to the purpose of comparison to the S-parameter waveforms provided by the manufacturers. In the used software (see section 2.5), the conversion of S-parameters to Z-parameters is made automatically. Without this software, the conversion is done by calculations based on following formula:

$$\mathbf{Z} = \mathbf{Z}_0 \cdot (\mathbf{E} - \mathbf{S})^{-1} \cdot (\mathbf{E} + \mathbf{S}) \quad (2.6)$$

Where Z_0 is the 50Ω termination resistance, \mathbf{E} describes the identity matrix and \mathbf{S} stands for the matrix with the S-parameters.

2.5 Software in use

Another possibility is, to measure the Z-parameters directly. The used Network Analyzer of Rhode & Schwarz is capable of a measurement like that, but because of already discussed reasons the S-parameters measurement was chosen.

The impedance characteristic is adequate to the Z_{21} waveform. When re-converted to S-parameters, Z_{21} corresponds with S_{21} . As the online systems of the capacitor manufacturing companies, Kemet and Murata, provides characteristics based on S-parameters, these parameters will be compared in this thesis.

2.5 Software in use

To extract all the needed information of the performed measurements, the result data has to be examined with a software.

There are more possible software solutions available.

MathCad is one of these possible software solutions, with the great advantage of an easy usability. But the usage is also limited.

So the analysis of the measurements for this thesis is getting done by a software named Advanced design system by keysight.

How to move on, after getting the measurement result files of the network analyzer is described in the measurement example in section [3.1](#).

3 Analysis of a single capacitor

This chapter contains a detailed description of the performed measurements, as well as a summary of the results of all 5 analyzed capacitors.

The examined capacitors of this thesis are manufactured by Kemet and Murata. Murata is one of the biggest manufacturer worldwide and Kemet is a big US company. Both provide datasheets of their products and possibilities to simulate them online.

First the impedance progress over a specified frequency will be measured and compared to the data provided by the manufacturer of the capacitor. Based on the measurement results, the real equivalent circuit diagram could be determined. For comparison, this equivalent circuit diagram should be used to simulate an impedance characteristic.

Furthermore it's planned to compare "similar" capacitors against each other.

In theorie a 100nF capacitor compared to another 100nF capacitor should have almost no deviation of each other (considering the same tolerance range, which is up to 20%), independent of the manufacturer or design. But as it is common knowledge, that not even two capacitors have the exact same value or characteristic, it is also consistent, that different manufacturers have got slightly different production processes.

Another point of interest is the comparison of two 100nF capacitors manufactured in different packages. If any, what are the differences between such packages?

Moreover, the possible differences between capacitors with the same value but different dielectric materials are considered.

The procedure of analysing a capacitor is described in section 3.1. A summary of all measurement is given in section 3.2 and discussed in section 3.3.

3 Analysis of a single capacitor

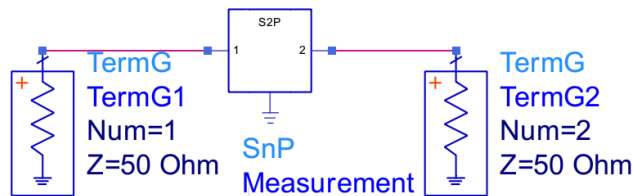


Figure 3.1: Data item to load datasets

First, the characteristic of the S-parameters of the chosen capacitor (in this example, it's a 1nF capacitor by Kemet) is to be measured. The thereby gained *.s2p file is loaded in the ADS software. In this software the measured dataset can be processed further or just be plotted.

3.1 Evaluation sequence on the basis of one example capacitor

This section represents a detailed description on how the analysis of all 5 capacitors was realised.

As example serves one of the 1nF multi-layer ceramic capacitor of Kemet.

At first, the wished parameters need to get measured with the Network Analyzer as described before in section 2.4.1.

For the planned analyses it is necessary to start with the measurement of the S-parameters. The theory behind this measurement is explained in section 2.4.2. The result of the measurements (the S-parameters) can be loaded into the ADS software. This is done with the setup shown in figures 3.1 and 3.2. The parameters which need to be specified are also illustrated in this figure. It is essential to give the *.s2p which holds the measured data and to specify the number of ports and their arrangement.

3.1 Evaluation sequence on the basis of one example capacitor

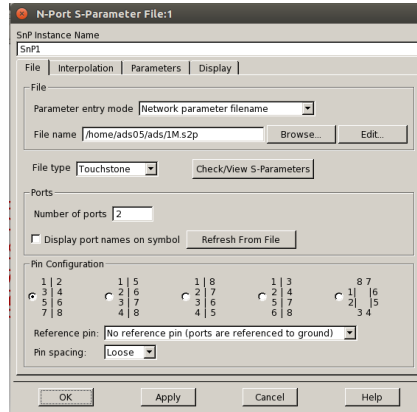
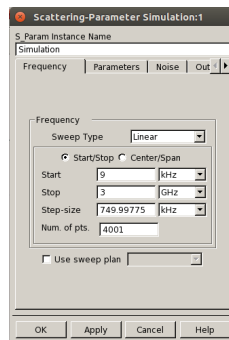


Figure 3.2: Parameter settings

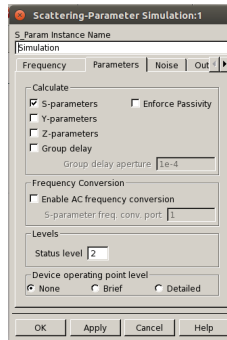


S_Param
Simulation
Start=9 kHz
Stop=3 GHz
Step=

(a) Chosen data item in ADS



(b) Frequency settings



(c) Parameter settings

Figure 3.3: Simulation of S-parameters

3 Analysis of a single capacitor

After feeding the measurement results into the software, it is possible to graphically visualize the loaded dataset and compare the measured S_{21} parameter to the S_{21} parameter provided by the manufacturer.

The data item and the attendant settings which are needed for a simulation run is seen in figure 3.3 and a first result is shown in figure 3.4.

The representation of the data in figure 3.4 takes place with two different plots, which show the same data. On the left is a representation as a xy plot with a logarithmic frequency axis and on the right side is a Smith chart displayed.

In ADS it's also possible to develop the equivalent circuit diagram. This is

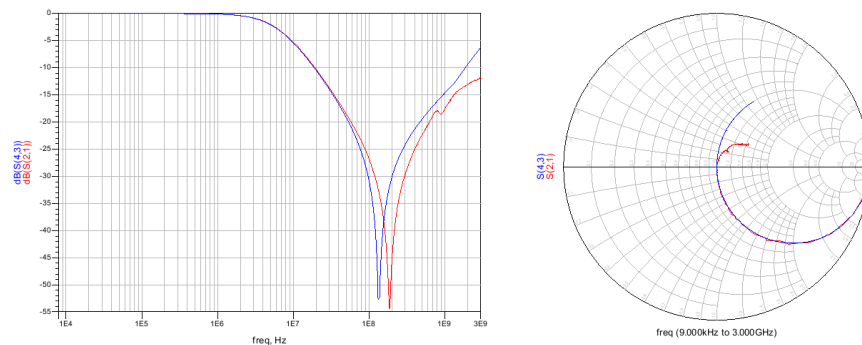


Figure 3.4: Comparison of measured S_{21} parameters (red) and the parameters provided by kemet (blue)

done by building and simulating an "guessed" equivalent circuit diagram and tuning the values of the single components until the plotted result matches the measured or provided plot.

It is possible to use both, a smith chart or an ordinary xy chart for adjusting the waveform of the equivalent circuit diagram to the wished waveform. Experience shows, that it is good to use a representation with a smith chart for the first rough approximation. For precision tuning it is easier to use the xy chart.

The first guess of an equivalent circuit diagram was the standard one, learned in education (for example in [24]). This circuit is seen in figure 3.5 and leads to to the plots in figure 3.6. On the left and the right end of the circuit shown in figure 3.5 are 50Ω termination resistors placed. The

3.1 Evaluation sequence on the basis of one example capacitor

capacitor C2 maps the capacitance of the capacitor. The resistor R1 represents the Equivalent Series Resistance (ESR). It summarizes the ohmic lead resistance and the dielectric reversal losses. The inductivity L1 stands for the Equivalent Series Inductivity (ESL) and it summarizes the parasitic inductance of the component. The resistor R2 in parallel to the capacitor shows the insulation resistance.

As seen in the graphic representation in figure 3.6, the equivalent circuit diagram is not quite accurate.

The first improvement of the circuit, is the adaption by a found paper [3] respectively the circuit also provided from Kemet (same construction), see figure 3.7. In this figure, the circuit is a further development of the equivalent circuit diagram in figure 3.5. The ESL is splitted up. Next to the parallel resistor is another capacitance, which forms together with the upper part of the splitted inductance another real capacitor. And the resistor R3 is parallel to the whole circuit to summarize the ohmic losses.

The values for the components in this equivalent circuit are specified for the resonance frequency.

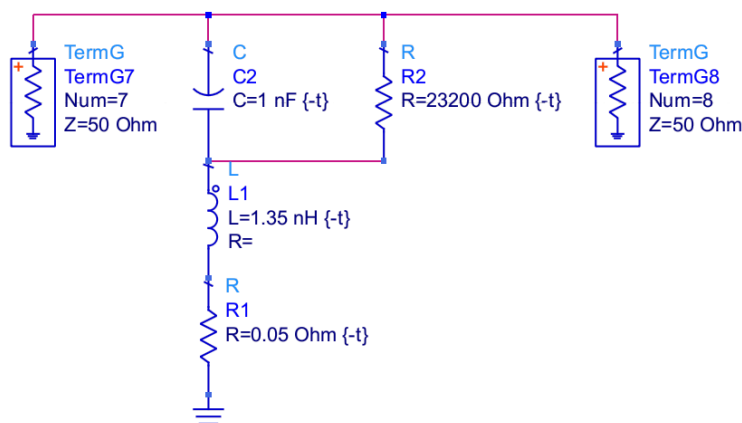


Figure 3.5: Standard equivalent circuit diagram

This leads to figure 3.8. It shows the comparison of the S_{21} parameter of the

3 Analysis of a single capacitor

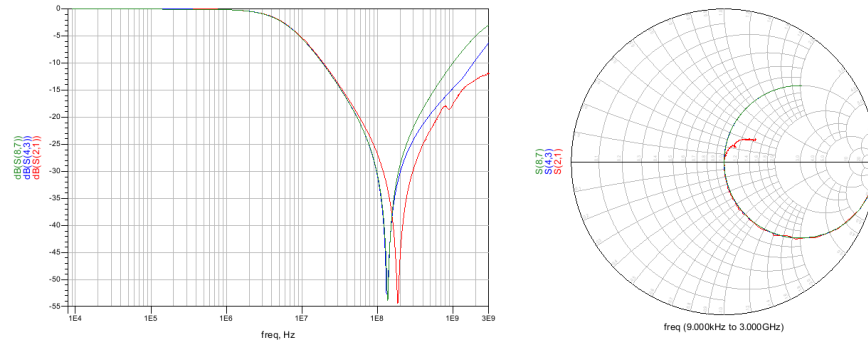


Figure 3.6: Waveform comparisons of S_{21} parameter, where $S(2,1)$ is the measured waveform, $S(4,3)$ the provided one and $S(8,7)$ the simulated one

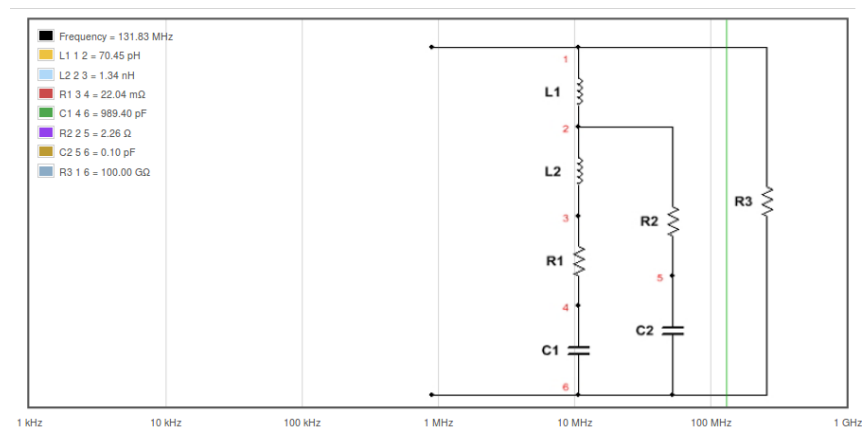


Figure 3.7: Equivalent circuit diagram of the 1nF C0G capacitor provided by Kemet

capacitor simulated with the equivalent circuit diagram from Kemet with the provided S_{21} parameter curve. The comparison shows, that these two curves match quite accurately.

The next step is, to figure out an fitting equivalent circuit diagram for the characteristic measured with the network analyzer. This circuit and the resulting plots are shown in figures 3.9 and 3.10.

This paragraph is to get a little impression, which component of the equiva-

3.1 Evaluation sequence on the basis of one example capacitor

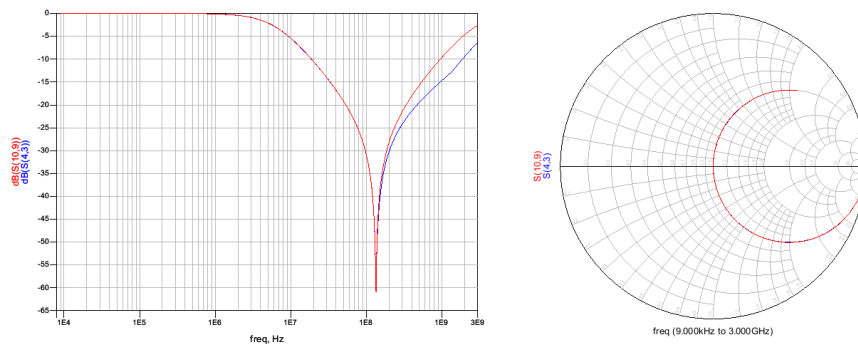


Figure 3.8: Simulated S_{21} parameter ($S(10,9)$) based on figure 3.7 compared to the characteristic of the capacitor ($S(4,3)$), which are both provided by Kemet

lent circuit diagram maps which real properties. The previous existing ESR is now not present anymore due to its small size. R9 and C11 are simulating the solder joint to the SMA connector in the measurement setup. That is reasonable, because all of the measured waveforms (and just the measured ones, not the provided characteristics) show such a deviation. And the three components (R7, L6, C10) which are connected in parallel to the whole circuit are mapping the capacitor which is formed by the connection areas of the capacitor. That means they are a result of the manufacturing process. The waveforms in figure 3.10 are quiet a good match. To get this result, the final equivalent circuit diagram is much costlier, than the equivalent circuit diagram looked at before (in figure 3.7). Making the correct adaptations is requiring a lot of experience and is very time-consuming.

To perform such an adaption to the provided equivalent circuit diagram, it is necessary to, at least roughly, know which component placed at which position creates what effect in the waveforms.

The most important discovery while adapting the circuit is to realize, that the bottom half of the smith diagram is mostly described by capacitors. The upper half on the other hand is dominated by the inductance in the capacitor. This insight is a good start, but it is not an absolut solution.

The more complex the equivalent circuit gets, the more influences the components each other.

For example the capacitor C11 in figure 3.9 creates the little loop almost

3 Analysis of a single capacitor

at the end of the waveform in the smith chart. The value of the capacitor defines the size of the loop.

More detailed considerations regarding the course of all waveforms are following in section 3.3.

Furthermore the ratio between the component values influences the waveforms. For that, the tuning function in ADS is very useful. With this function, it is possible to change the value of specified components and watch the consequences directly at the plot.

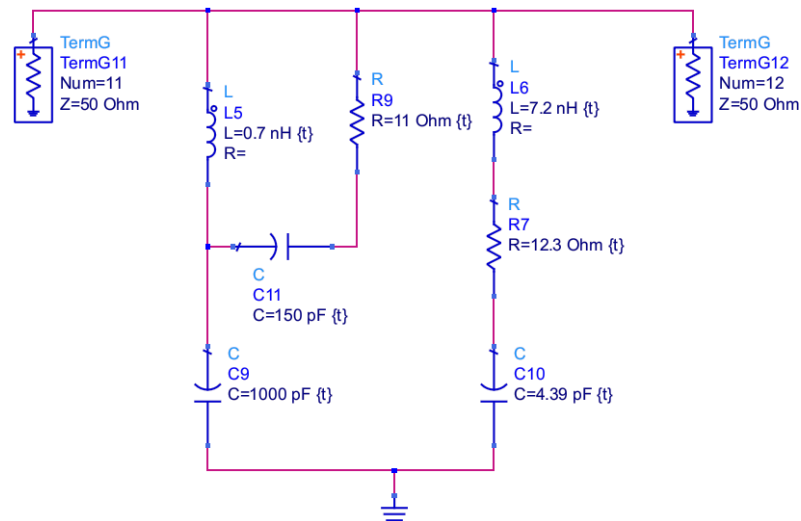


Figure 3.9: Adjusted equivalent circuit diagram of the 1nF COG capacitor

3.2 Comparison of the characteristics

All the results shown in this section are obtained as described in section 3.1. First there are the comparisons between the characteristics, provided by the manufacturers, and the measured characteristic in section 3.2.1.

In section 3.2.2 the capacitors will be compared against each other.

3.2 Comparison of the characteristics

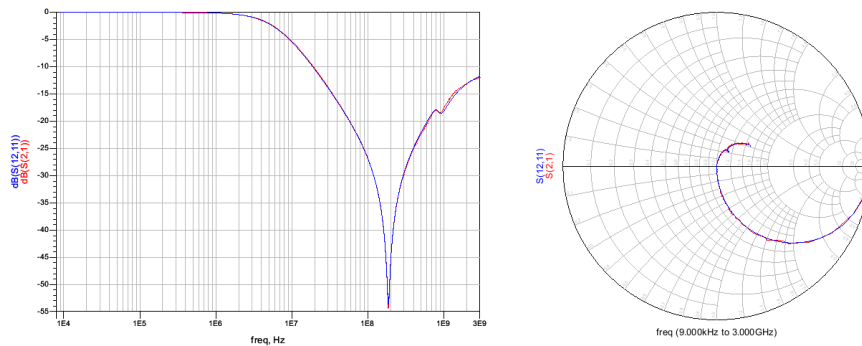


Figure 3.10: Comparison of measured (S(2,1) in red) and simulated (S(12,11) in blue) S_{21} waveform

The subsequent sections are a listing of the resulting waveforms, the analysis of these comparisons is quoted in section 3.3.

3.2.1 Capacitor characteristic compared to each other

The following sections are a summary of the comparisons of all five measured capacitors. Compared got the measurement S_{21} characteristic with the S_{21} characteristic provided by the particular manufacturer.

In the following plots, the measured waveform will be plotted in red (each S(2,1) waveform) and the provided waveform will be illustrated in blue (as S(4,3) curve).

1nF COG Kemet

The waveform illustrated in figure 3.11 shows the comparison of the measured and the provided S_{21} characteristics of the C0805C102J5GACTU manufactured by Kemet.

Until around 13MHz, the measured and the provided waveform matches. With higher frequencies the deviates in the direction of a slightly higher resonance frequency.

3 Analysis of a single capacitor

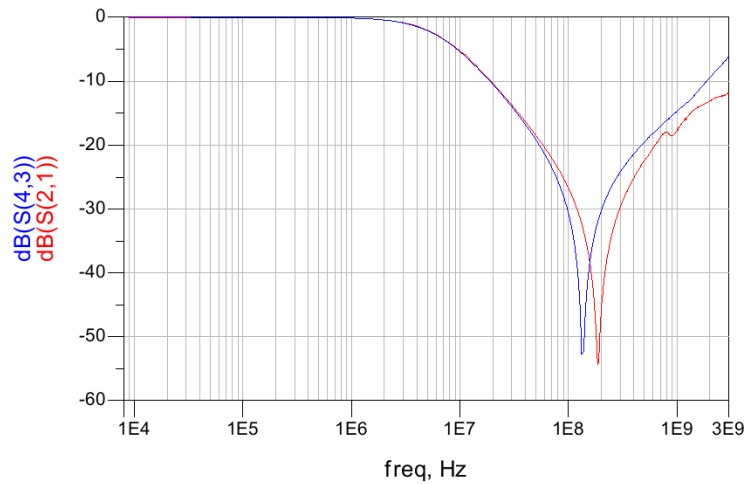


Figure 3.11: Comparison of 1nF C0G characteristics

1nF X7R Kemet

In figure 3.12 the comparison between the measured and the provided S_{21} characteristics of the C0805C102J5RACTU capacitor by Kemet is illustrated. Both of the waveforms concur quite good until the resonance frequency. After that point, the measured waveform strays regarding a little higher resonance frequency with a slightly lower impedance value.

100nF X7R Kemet

The measured and the provided S_{21} characteristics of C0805C104K3RACTU by Kemet are shown in figure 3.13.

Up from around 3MHz the measured waveform deviates quite obvious to the provided characteristic.

3.2 Comparison of the characteristics

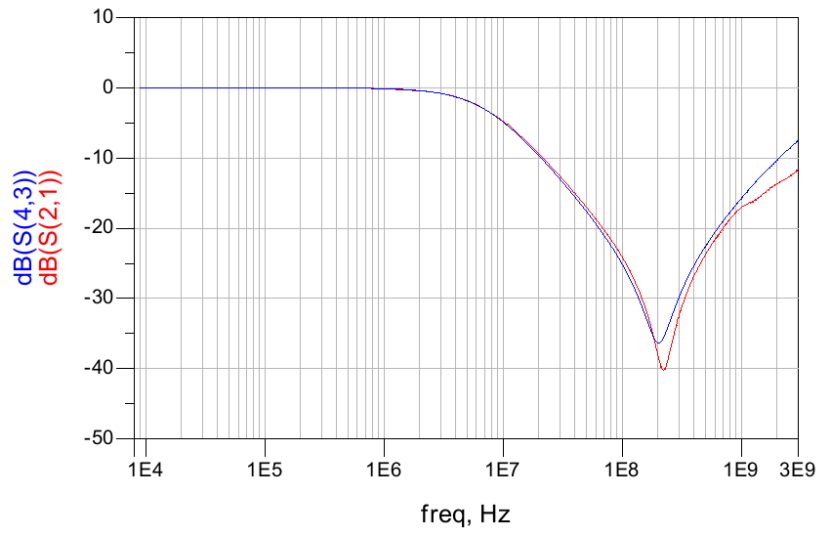


Figure 3.12: Comparison of 1nF X7R characteristics

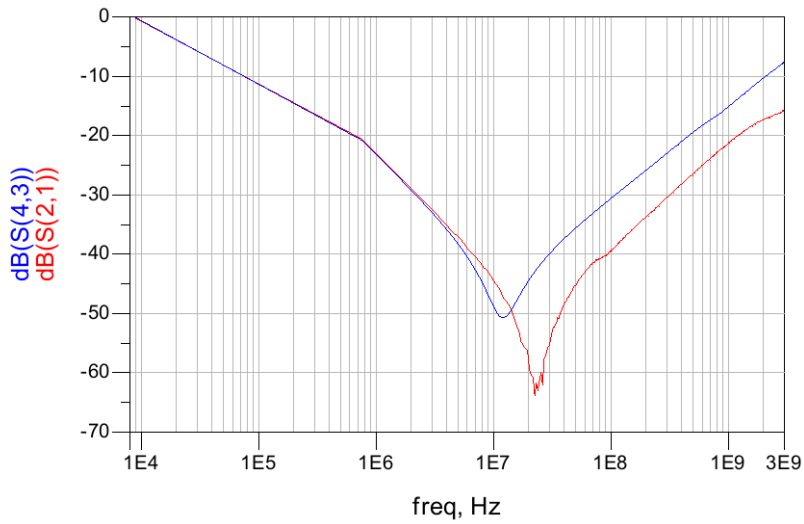


Figure 3.13: Comparison of 100nF X7R characteristics

3 Analysis of a single capacitor

100nF X7R Murata

Murata is the manufacturer of the GRM21BR71E104KA01L, which is also a 100nF capacitor. The comparison of the S_{21} characteristics is shown in figure 3.14.

There are not as much deviations around the resonance frequency as with the capacitors before. Although the beginning of the waveforms match not as good as in the previous plots.

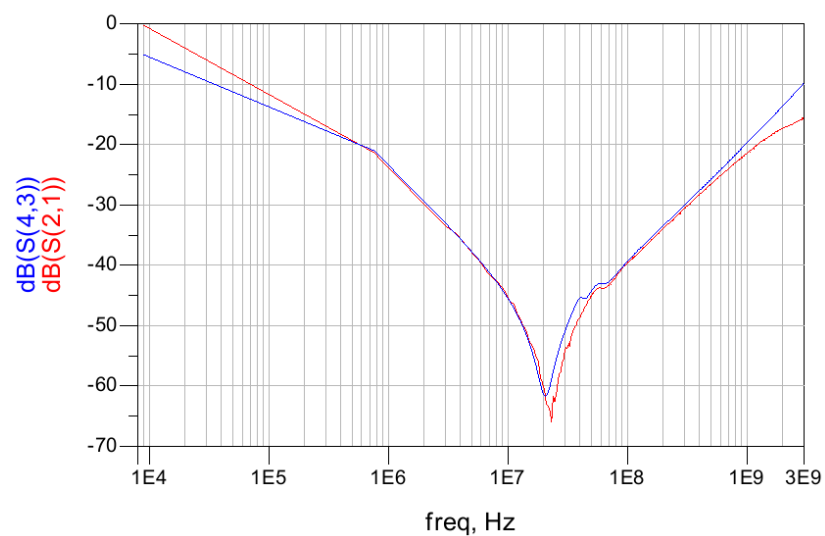


Figure 3.14: Comparison of 100nF X7R characteristics

100nF LLL Murata

The 100nF capacitor in this section is produced also by Murata, but in another package form. The comparison of the S_{21} characteristics of the LLL216R71E104MA01L is illustrated in figure 3.15.

At the beginning of the two waveforms is, like at the other Murata capacitor, a recognizable difference. Until the resonance frequency, they match quite good and afterwards they deviate again.

3.2 Comparison of the characteristics

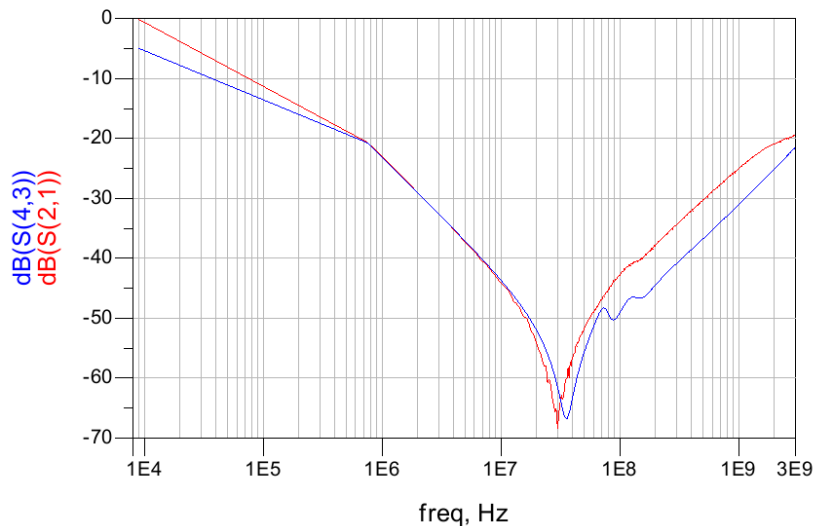


Figure 3.15: Comparison of 100nF LLL characteristics

3.2.2 Capacitors compared with/against each other

There are three different comparisons following. The comparisons between the characteristics specified by the manufacturer and also the comparisons between the first-hand measurements of the S-parameters characteristic.

1nF vs 1nF

In this section, two 1nF capacitors made by Kemet are compared. One of the capacitors is a X7R type and the other one is a COG type. These two different classes (explanation in section 2.1) are going to be compared, although the expectation is, that there will not be much difference, since both of the capacitors have got the same component value and just some differences at the isolating material.

Figure 3.16a shows the two capacitor waveforms as provided by Kemet.

3 Analysis of a single capacitor

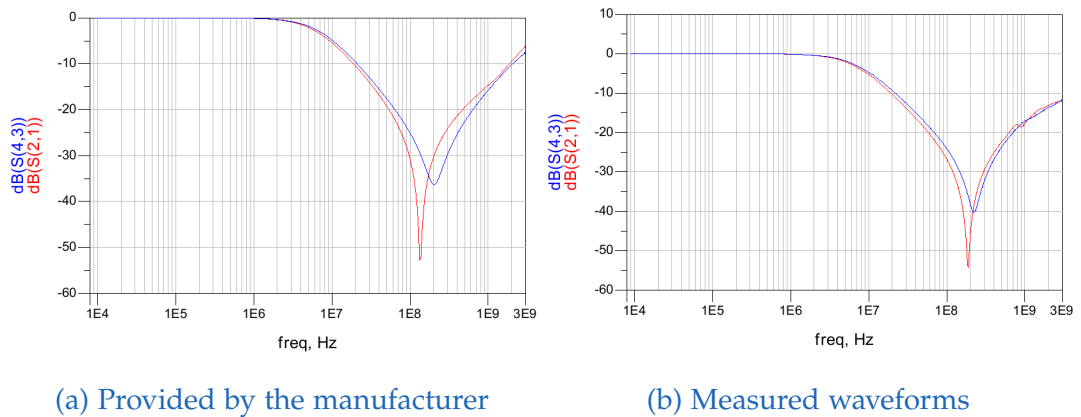


Figure 3.16: The S(2,1) waveforms are from the C0G capacitor, the S(4,3) waveforms illustrate the characteristic of the X7R capacitor

In figure 3.16b the same two capacitors are compared. But this time the waveforms are measured.

100nF vs 100nF

Two 100nF capacitors made by Murata are compared in this section. The difference between these two capacitors is in the design. One capacitor is a LLL type (for explanation see conclusion section 3.3) and the other one capacitor is a standard X7R type, as also one of the 1nF capacitors.

The comparison between the by Murata provided characteristics is shown in figure 3.17a. The same capacitors with measured waveforms are illustrated in figure 3.17b.

100nF vs 100nF

In this section also two 100nF capacitors are under review. This time both capacitors are made at X7R type, so the resulting plots should be overlapping. The only difference between them, are the different

3.2 Comparison of the characteristics

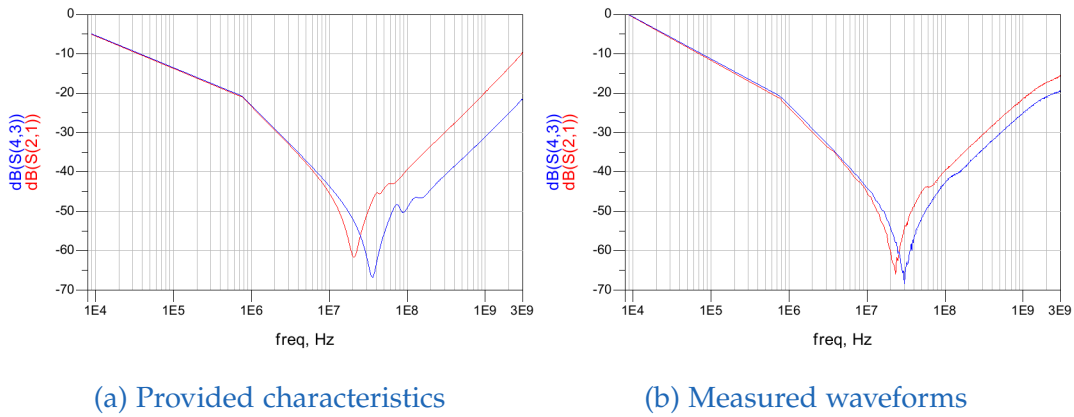


Figure 3.17: Comparison of the both capacitors, compounded by Murata. The S(2,1) waveforms illustrate the standard X7R 100nF capacitors, the S(4,3) curves show the characteristics of the LLL type.

manufacturers. One capacitor is made by Kemet, the other one is made by Murata.

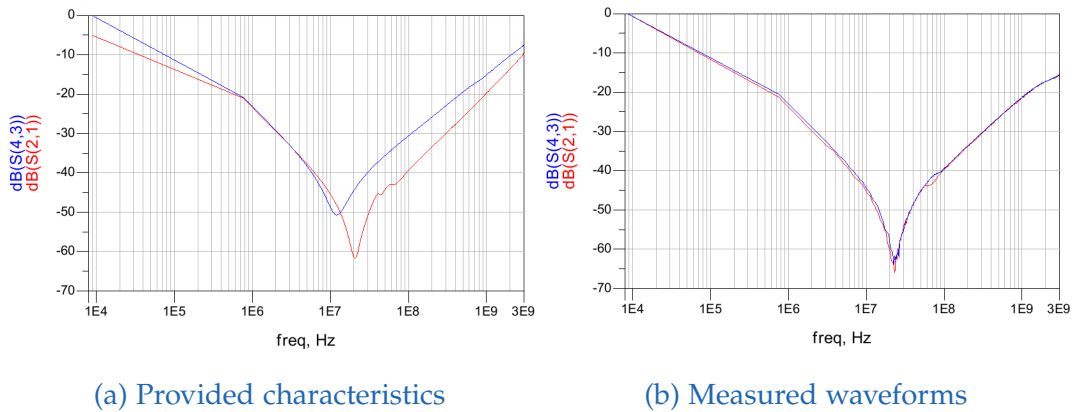


Figure 3.18: Comparison of 100nF capacitor of Murata (S(2,1)) and Kemet (S(4,3))

The plot in figure 3.18a shows the provided S_{21} characteristics. In figure 3.18b the same characteristic based on a measurement is shown.

3.3 Conclusion

The results of the previous measurements are going to be discussed in the following two sections.

The plots from section 3.2.1, the section where the measured characteristics of capacitors is compared with the provided one, will be discussed in section 3.3.1. The results illustrated in section 3.2.2, where the capacitors are compared against each other, will be discussed in section 3.3.2.

But beforehand one generic realization:

The generalized equivalent circuit diagram which is taught during education is way to inaccurate.

Kemet also provides an equivalent circuit diagram (which is already more complex than the "standard" equivalent circuit diagram) for their capacitors. The characteristic of this equivalent circuit and the provided characteristic are quite a good match.

But as already learned in section 3.2, to develop a fitting equivalent circuit diagram is rather time-consuming.

While trying to develop a equivalent circuit diagram, which results in a characteristic that matches the measured one, there emerged several insights.

The most serious one is probably the deviation of the red waveform to the inside of the smith chart in figure 3.4. While designing the equivalent circuit diagram, it was revealed, that this divergence could be recreated by adding an extra resistance to the circuit. This also means, that the real capacitor has an additional resistance in contrast to the capacitor, which is delivered according to the Kemet.

The second difference to the provided characteristic is that the measured one shows a loop in the before discussed deviation part. In the equivalent circuit diagram this could be realized by adding a capacitor in parallel to the inductor.

In reality those two deviations most likely was formed because of the measurement setup. That means, the solder joint respectively the SMA connector itself are responsible for the deviation of the provided characteristics. This also means, that the provided characteristic have to be treat with caution. Because every bought component needs to get soldered or mounted in some way.

The values of the components are chosen due to fitting reasons.

3.3.1 Conclusions regarding the comparison between datasheet and measurement characteristics

When comparing the measured characteristics with the provided waveforms, it is clearly evident, that these graphics are similar-looking, but definitely not an exact match.

In theory, both of these waveforms of the respective capacitors should be an exact match.

In practical experience there are many factors, which influences the characteristics and affect the course of the curve.

In general terms, it can be said that the deviations of the capacitors by Kemet starts at latest at the resonance frequency.

With the two Murata capacitors, the deviations already starts at the beginning, until around 1MHz. Then there is quite an exact match between the waveforms. Around the resonance frequency a more or less obvious deviation starts again.

Following is a more detailed conclusion:

- 1nF COG by Kemet in figure 3.11
Until 13MHz the two waveforms match exactly. Then the deviation is growing quite fast and leads to a dissonant resonance frequency. After that frequency, the traces run parallel (but with a distance to each other) until around 140MHz. Then there is kind of a hook in the measured waveform and the two traces doesn't fit no longer at all. For this capacitor an equivalent circuit diagram was created, so it is easy to recognize the differences between the capacitor as planned by the manufacturer (see figure 3.5) and the capacitor which it is in real (see figure 3.9). While developing the equivalent circuit diagram, it became clear, that this little hook is created by the part in the upper left corner in figure 3.9.
The general deviation after the resonance frequency is to blame on a too little parasitic inductance, which is determined by the package

3 Analysis of a single capacitor

size. These variance happened possible through the manufacturing process.

- 1nF X7R by Kemet in figure 3.12

These two waveforms show already at around 10MHz a slight deviation. The resonance frequencies almost match, but apparently the parasitic resistance changes the impedance value at this frequency. Furthermore there is also a deviation at the inductance part of the waveform. This means, there is a variance in the inductance respectively the package size as well as at the C0G capacitor.

There is also, as already seen at the C0G capacitor, a little hook at around 190MHz. But it is not as distinctive as at the C0G capacitor.

- 100nF X7R by Kemet in figure 3.13

This capacitor is the one with the biggest deviation. Until almost 2MHz the both waveforms match fine. After that, until the resonance frequency, the measured waveform is deviation quite obvious. The resonance frequency itself and the related impedance value don't match at all. The frequency is too high and the impedance value too low compared to the provided characteristic.

The measured characteristic after the resonance frequency has a distinctly deviation of the provided curve, obviously due to the variance beforehand, but the course of the curve matches the provided curve moderately well.

- 100nF X7R by Murata in figure 3.14

At first sight the waveforms are almost consistent with each other. Closer examination shows that the initial impression was misleading. In the range of around 500kHz until around the resonance frequency the deviations are minimal. In the remaining frequency range, the course of the measured curve is similar-looking, but not the same as the provided characteristic. Below 500kHz and above around 500MHz the deviations grow clearly.

The hook around 15MHz is in the measured waveform not as distinctive as it should be, according to the provided characteristic.

- 100nF LLL by Murata in figure 3.15

The first part of the characteristics, until the resonance frequency, shows quite similar deviations as the other capacitor provided by Murata. After that, in the range of around 80 to 100MHz, the capacitor characteristic should also show a hook, again, like the other capacitor

3.3 Conclusion

of Murata. This hook is even less distinctive as at the other 100MHz capacitor by Murata. That is interesting, because all measured characteristics show a hook in this range. All but this one, where it is claimed by the provided characteristic.

After considering all graphs, there are some obvious insights:

Every measured waveform shows this already mentioned hook in a certain frequency range. This hook in the xy plot corresponds to the also already discovered deviation of the graph to the inside of the smith chart. As a consequence this has to be something external. Most likely this deviation comes from the solder joints of the capacitor with the SMA connectors, as seen in figure 2.5.

Another detail, which attracts attention, is the loop discovered at the 1nF C0G capacitor while developing the equivalent circuit diagram. As the 1nF X7R capacitor also shows this effect, but no one of the 100nF capacitors, it seems to trace back to different manufacturing processes, used materials or internal structures between the 1nF and the 100nF capacitors.

The 100nF capacitors instead shows the faster drop of the impedance right from the beginning of the graphical illustration and not just after approximately 1MHz. This also suggests a different internal structure between the different values of the capacitors.

3.3.2 Conclusions regarding the comparison between the capacitors against each other

In this second conclusion section, the really interesting part is discussed.

When comparing two capacitors with the same value to each other, the first thought is, to expect the same properties.

But literature research and the results of the measurements so far suggest that this first thought has to be reconsidered.

- 1nF vs 1nF in figure 3.16

The intention of this comparison is, to show differences between the different classes of capacitors, which are both manufactured by Kemet. The differentiation of the classes is explained in section 2.1.2.

The plot shows, that, in comparison with the X7R capacitor, the C0G

3 Analysis of a single capacitor

capacitor provides a lower impedance around the resonance frequency, as already expected. The impedance range which is lower than the one of the X7R capacitor is also narrower than the higher impedance characteristic.

This is not just in theory, means, in the provided waveforms, but also the measured waveforms confirm this.

Apart from the impedance value, the resonance frequencies themselves are consimilar. The little deviation is explainable with divergences in the manufacturing process.

- 100nF vs 100nF in figure 3.17

These two capacitors are produced by Murata. Both have the same capacitance value and are of the X7R type. The only difference lies in the package.

The capacitor described as X7R is a standard 0805 component. The part called LLL is build as 0508.

This difference is also visible in the plots. In the plot with the provided waveforms the deviation due to the lower parasitic inductance is obvious. The difference is not that obvious in the plot with the measured waveforms, but it is still evident.

- 100nF vs 100nF in figure 3.18

When considering the plot with the provided waveforms, besides the derivation at very low frequencies, a significant variance in the area around the resonance frequencies and afterwards is seen. That means, that there has to be quite a difference regarding the parasitic inductance. Since the two capacitors are produced by different manufacturers (one is by Kemet, one by Murata), this seems to be because of their production process or their different inner structure.

But then, when considering the plot with the measured waveforms, the two capacitors look quite similar. This means, a 100nF capacitor is exchangeable with an identically constructed 100nF capacitor manufactured by a different company.

Summarizing is to say, that the comparisons fit better than first (after the first measurements and researches) expected.

When looking at the provided characteristics, the results are as expected. Clear differences between different classes of capacitors, an obvious deviation at capacitors with different designs and also a manufacturer-specific

3.3 Conclusion

variance between to capacitors with the same value.

When looking at the measurement results, there forms a different picture. The differences between different classes of capacitors are not as clear as expected. The deviation at capacitors with different designs are not as obvious as in the graph with the provided characteristics and the manufacturer-specific variance between two capacitors with the same value does not really exist.

4 Parallel circuit of capacitors

The reason for connecting capacitors parallel is the requirement for an impedance characteristic as low as possible across a frequency range as wide as possible. The corresponding theory is explained in section 2.2.

Sometimes parallel circuits in the design are created by accident. Chances therefor increase with the size of the printed circuit board.

Such a board itself could also appear to be a problem. A stand-alone board (even without equipping) is building a parasitic capacity between the GND and the VDD plane.

Such effects, if not considered, could seriously influence the characteristics. The existence of additional (parasitic) capacitors is a problem. Due to unspecified and uncorrected values of these capacitors they promote parallel resonances.

In this section of this thesis, the main focus lies at planned parallel circuits.

In section 4.1, the impact of two parallel capacitors with the same value is discussed. Furthermore, the differences of a parallel circuit of 100nF and 1nF (both X7R) and a parallel circuit where the 1nF capacitors is a C0G type are analyzed.

In section 4.2 there will be four capacitors connected in parallel. First with the capacitor values considered during the electronic project [1]. After that, possible improvements will be discussed.

The planned measurements respectively analyses of this section corresponds with the measurements from section 3.

Therefore there is no explanation of the measurement setup or the measurement itself in the following sections. It will be just a summary of the measurement results and the corresponding discussions.

4 Parallel circuit of capacitors

4.1 Parallel circuit of two capacitors

In the following three subsections considerations of different parallel circuits of two capacitors per circuit takes place.

First, two equally designed capacitors with the same value (in this case 100nF) will be connected in parallel and observed.

Then there will be two parallel circuits with a 100nF and a 1nF capacitor. At the first of these two parallel circuits, the 1nF capacitor is a X7R type, same as the 100nF capacitor. The second parallel circuit is build with a 100nF (type X7R as before) and the 1nF capacitor is a C0G type.

4.1.1 Parallel circuit of two 100nF of Murata

The question of this section is, if there is any effect, if two identically constructed capacitors with the same value are connected in parallel?

As learned in section 2.2 a parallel resonance (the unwanted peak in the characteristics of parallel circuits) is evolved when the capacitor with the lower resonance frequency is already working as an inductance and the capacitor with the higher resonance frequency is still working as a capacitor. So, at a parallel circuit with two capacitors with the same resonance frequency this should not happen.

As shown in figure 4.1, the before made assumption is correct: there is no parallel resonance.

The curve shape of the characteristic of the parallel circuit of two capacitors with 100nF each is looking almost the same as the curve shape of the characteristic of the single 100nF capacitor. The characteristic is just shifted in a way, that this results in a lower impedance over the entire range of the measurement. Measured at the resonance frequency, the characteristic of the parallel circuit is 6dB lower, than the characteristic of the single capacitor. This value is formed because of a simple fact: when doubling the capacitors with the same capacitance value, the total capacity is decreasing by half. As seen in formula 4.1, this leads to a increasing of the impedance characteristic by approximately 6dB.

4.1 Parallel circuit of two capacitors

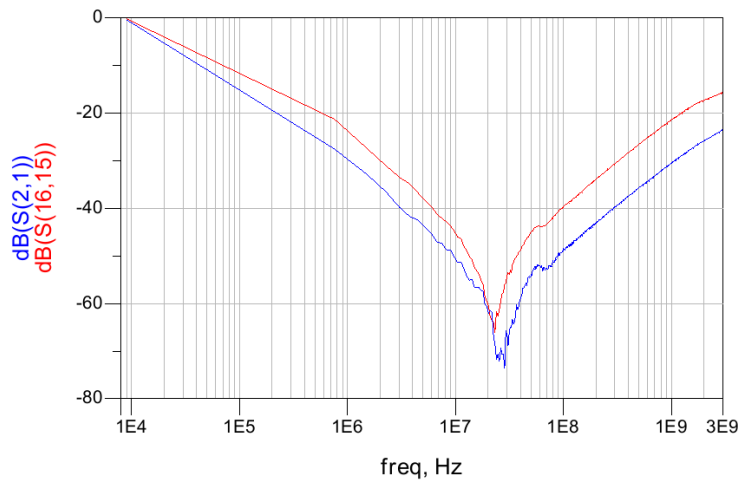


Figure 4.1: Parallel circuit of two 100nF capacitors (blue) compared to the characteristic of the single capacitor (red)

$$20 \cdot \log \frac{1}{2} = -6,0206dB \quad (4.1)$$

4.1.2 Parallel circuit of 100nF and 1nF (both X7R)

In this section, a parallel circuit of two capacitors of the X7R type are analyzed. Two similar capacitors with the same value were already looked at in the section before. Now there will be a 100nF and a 1nF capacitor with the same dielectric material under review.

The characteristic of this capacitor combination is shown in figure 4.2.

The overall characteristic of the parallel circuit is shown in pink as the S(4, 3) curve. The characteristic with the lower resonance frequency is related to the 100nF capacitor, the higher resonance frequency characteristic to the 1nF component.

4 Parallel circuit of capacitors

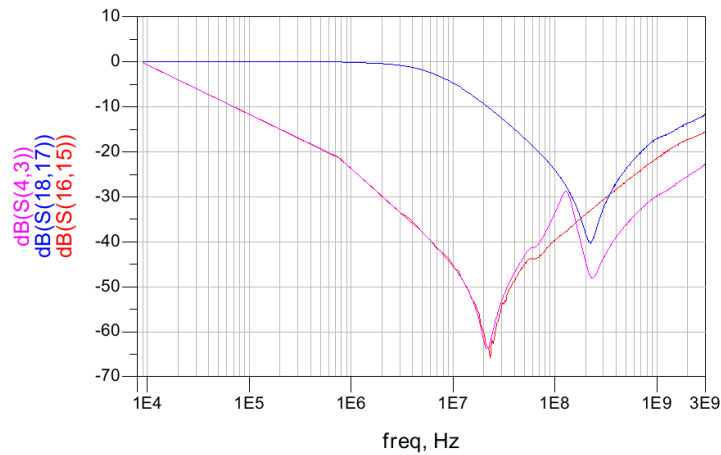


Figure 4.2: Parallel circuit (pink) of 100nF (red) and 1nF (blue), both X7R

4.1.3 Parallel circuit of 100nF (X7R) and 1nF (C0G)

For comparison reasons, the standard 100nF capacitor, like in the two measurements before, is combined with a 1nF capacitor of the C0G type this time.

The C0G capacitor shows a lower impedance at the resonance frequency as the same-valued X7R type, so it should make a better overall characteristic.

That this assumption was wrong, is seen in figure 4.3. The parallel resonance of the overall curve is 7,4dB higher then the parallel resonance when using two capacitors of the X7R type.

A more detailed analysis is performed in section 4.3.

4.2 Parallel circuit of four capacitors

As already planned during an previous electronic project [1], a parallel protection circuit (for example for an integrated circuit) with four capacitors is analyzed in this section.

The smallest capacitor (100pF) is a C0G type. The reason therefor is, that the C0G type is more low-loss than the X7R type. The capacitor next to

4.2 Parallel circuit of four capacitors

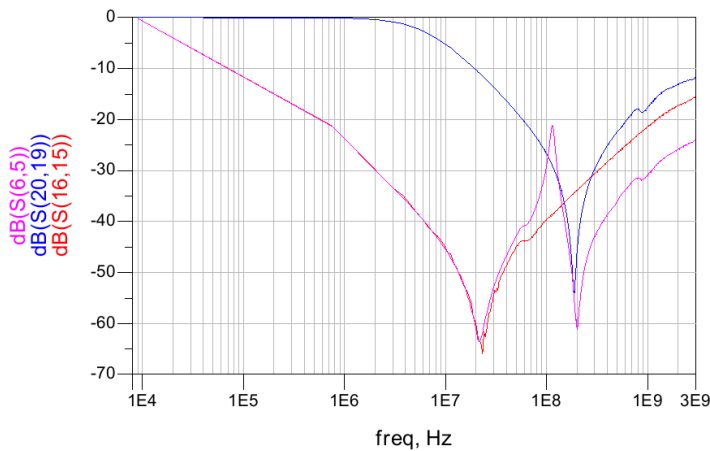


Figure 4.3: Parallel circuit (pink) of 100nF (red, X7R) and 1nF (blue, C0G)

the 100pF is the 1nF capacitor, which will be build in as a X7R type at first. The second measurement is with the C0G type, for comparison. For both measurements, the other two capacitors are similar: 100nF and $1\mu\text{F}$, both designed as X7R type.

The used component values were choosen during the already mentioned electronic project without any research or basic knowledge (what often is the strategy of unexperienced designer).

Regarding the previously done literature research, there exists an ideal ratio of the capacitor values, if they should be structured in parallel [10], [11].

But for research reasons, the already mentioned capacitor values will be used, analyzed and possibly improved.

Afterwards a conclusion of the results is following.

4.2.1 Parallel circuit of $1\mu\text{F}$ (X7R), 100nF (X7R), 1nF (X7R) and 100pF (C0G)

In figure 4.4 the first attempt of a parallel circuit with four capacitors is illustrated.

The characteristics of the single capacitors are also shown. The higher the

4 Parallel circuit of capacitors

value of the capacitor, the lower the resonance frequency of the characteristic and the flatter the reduction of the curve to the absolute minimum. The blue, slightly broader curve is the resulting characteristic of the parallel circuit.

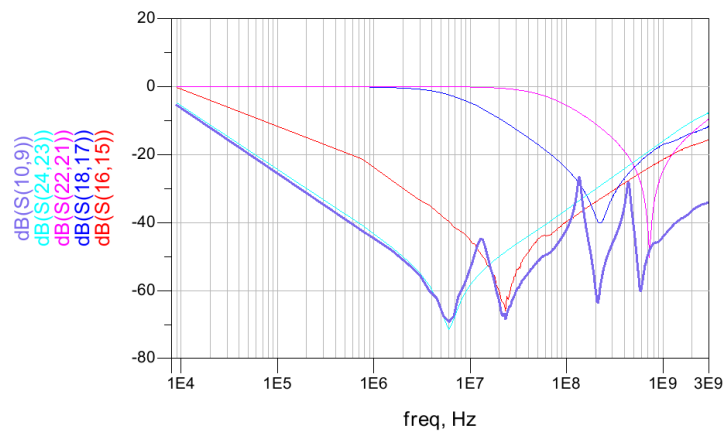


Figure 4.4: Parallel circuit (light blue) of 1 μ F (X7R, green), 100nF (red, X7R), 1nF (blue, X7R) and 100pF (pink, C0G)

4.2.2 Parallel circuit of 1 μ F (X7R), 100nF (X7R), 1nF (C0G) and 100pF (C0G)

For comparison reasons, the same parallel circuit as in the section before was evaluated. The only difference is the switched 1nF capacitor. Instead of a X7R, a C0G was used. In figure 4.5 this switched capacitor characteristic is illustrated by the thin blue line with the second highest resonance frequency. Like in figure 4.4, the resulting graph is drawn in blue and slightly broader than the other curves.

4.2 Parallel circuit of four capacitors

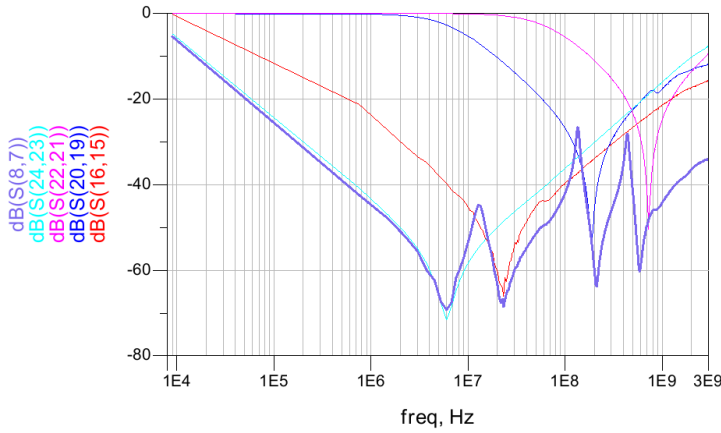


Figure 4.5: Parallel circuit (light blue) of $1\mu\text{F}$ (X7R, green), 100nF (red, X7R), 1nF (blue, C0G) and 100pF (pink, C0G)

	Cap 1	Cap 2	Cap 3	Cap 4
Theory	1	5	25	125
Values by e-series	1	4,7	22	100

Table 4.1: Capacitor values in ration of 5:1, all values in nF.

4.2.3 Improvements

The resulting characteristics shown in figures 4.4 and 4.5, when choosing the capacitor values without experience or research, are a step in the right direction. However, the peaks in the graph are definitely too high for a functional usage. Therefore an improvement is indispensable.

As already discovered while the literature research, the ideal ratio of the parallel capacitors to each other is 5:1 [11].

When starting the values at 1nF , the calculated values and the values according to the e-series are listed in table 4.1.

Figure 4.6 shows two characteristics, where the capacitor values were selected by the 5:1 theory. The red characteristic shows the parallel circuit, which was built with three X7R and one C0G capacitors, the blue characteristic shows the parallel circuit built just with X7R type capacitors.

4 Parallel circuit of capacitors

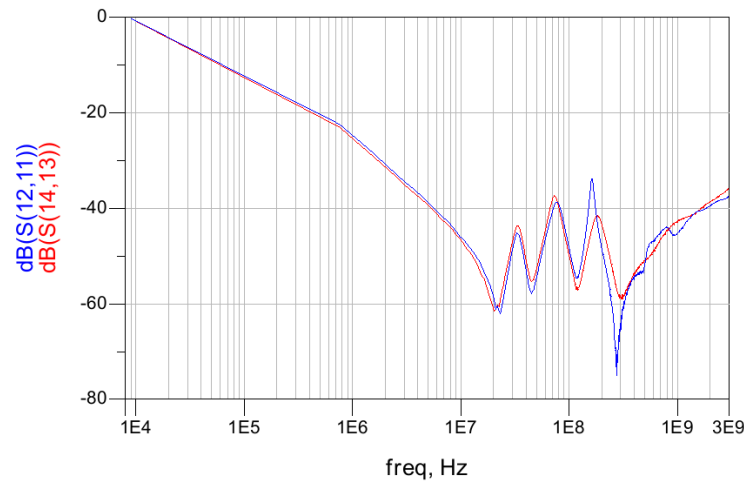


Figure 4.6: Characteristic comparison of both improved parallel circuits with four capacitors (blue: all capacitors X7R, red: smallest capacitor as C0G type)

4.3 Conclusion

The measurements of this section reveal a few effects.

Starting with section 4.1, there are two big insights:

The use of two capacitors with the same value, or more specifically the same resonance frequency, for a parallel circuit does not lead to a peak in the resulting characteristic waveform as usually when connecting capacitors in parallel. The effect with two equal capacitors is a shift of -6dB of the impedance at resonance frequency. A 6dB decreasing is equivalent to a reduction by factor 2. This happens every time, the number of capacitors connected in parallel is doubled [10]. If the additional costs and the extra space are irrelevant, such an effect is quite useful for a selective reduction of the impedance at the resonance frequency of the used capacitors.

Comparing the two measurements of the parallel circuits with 100nF and

4.3 Conclusion

1nF, where the two 1nF capacitors are from a different type, leads to following conclusion:

The parallel circuit with the C0G capacitor results, against first assumptions, in the worse waveform. That is because the C0G capacitor shows an abrupt drop of the curve towards the resonance frequency. This steep course of the curve is responsible for the high peak at the resonance frequency of the parallel circuit. This leads to the conclusion, that, for parallel circuits, it is better to accept a higher impedance with a more shallow waveform, than to insist for an impedance as low as possible and earn a high parallel resonance.

The overall characteristics of the two parallel circuits with four capacitors are compared in figure 4.7.

It was not clearly seen in the two plots before, but in this graph it is getting obvious, that those curves are exactly the same.

In section 4.1 the measurements leads to the conclusion, that the usage of

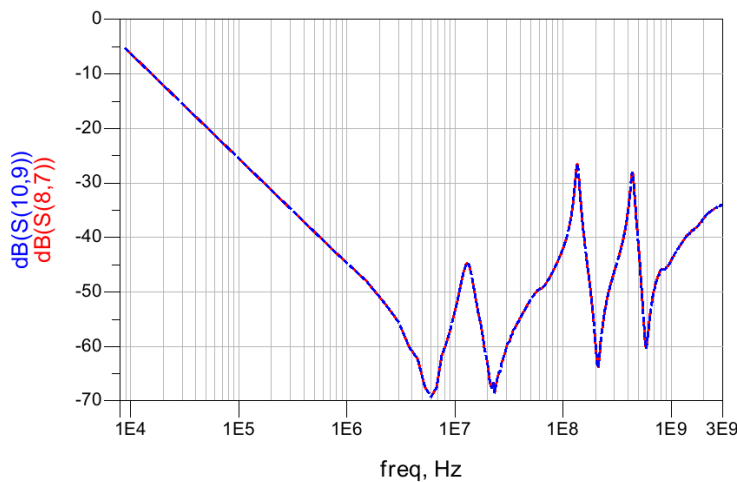


Figure 4.7: Characteristic comparison of both parallel circuits with four capacitors, with values chosen without experience

capacitors of the C0G type leads to higher peaks in the characteristic of the parallel circuit, as the usage of type X7R capacitors.

But in this case, in figure 4.7, there is no impact of the substitution of the 1nF capacitors.

4 Parallel circuit of capacitors

This leads to the conclusion, that it is not relevant for the characteristic if the type of one capacitor is changed, as long as there is still a smaller one, to compensate a possible change of course.

Another important observation was, that it is better to connect capacitors together which show not such a big range of value as in the first measurement.

Also the assumption, that a ratio of 5:1 of the capacitor values [11] was confirmed.

The last measurement, results seen in figure 4.6, confirmed the before stated conclusion, that the position within the value range of a capacitor which should be switched against a same-valued capacitor from another type is crucial.

It also confirms the 5:1 ratio theory. Such a ratio of capacitor values to each other leads not necessarily to a lower overall impedance characteristic, but to a parallel resonance without unwanted high peaks.

As an overall conclusion, it could be said, that for parallel circuits in practice the value-ratio of the capacitors to each other is more important than the types of the capacitors.

Furthermore the ratio between the different capacitors is not neglectable. Considering that in practice, there are a lot more effect influencing the characteristic waveform, this is not an irrelevant conclusion. More of a possible practical usage is discussed in chapter 5.

5 Final measurement

This chapter is build on the measurements so far.

Up to this point, this thesis is about the impedance characteristic of single capacitors and how such a characteristic is changing, when capacitors are connected in parallel. Which was a good way of getting started with this topic and to understand how different capacitors could be influencing the impedance characterisitc.

But in reality, neither capacitors are connected to the next capacitor or whatever component directly, nor are the components levitating.

In reality, the capacitors are connected to other components via traces and are mounted on a printed circuit board (PCB).

This was not considered until now.

The idea of this chapter is to observe the impedance characteristic over the whole PCB and to watch the influence of individual capacitors.

5.1 Used printed circuit board

It would be easier to design a simple demonstration board for a first look into the overall impedance characteristic.

But in reality, it is possible, that the layouter/designer gets the completed board with a way too high impedance on a certain frequency or even overall.

To simulate an realistic case, a random PCB was chosen to realize the previous made measurement ideas.

The chosen board is designed by two members of the Insititute of Electronics (Prof. Winkler and Prof. Deutschmann).

It is called skewing demonstration board and is designed to determine ground bouncing of integrated circuits. Such an effect is often a big part

5 Final measurement

of interference emission. To reduce this influence it is possible to shift the switching times chronological (which is called skewing). This is possible with the outputs of the driver integrated circuits.

But there is no need for a more detailed description, as the functionality of the printed circuit board is of secondary importance.

What is important, is that a lot of capacitors are placed on the board, access to the schematic is available and it is possible to analyze the impedance characteristic.

As the board was planned by members of the Institute of Electronics, all those factors apply.

5.2 Measurement preparation

In this measurement case, the preparation and calibration is not as easy as at the measurements before.

The measurement setup needs to be chosen wisely, since the PCB features no SMA connector.

This means that there is need for an alternative connection, which will be suitable for measurements with the vector network analyzer.

The easiest way to get the required 50Ω system is to use a coaxial cable, cut it and use this open end as connectors to the measurement point.

An example of such a coaxial cable is illustrated in figure 5.1. This is not the originally used cable, but the first version. It was made out of a broken cable in hopes of reusability. But unfortunately this cable was too corrupt. Also the loop, which is formed by the shield and the conductor is too big at this first try.

The calibration of this cable is rather easy made with the help of the already described "Port extension" function at the Network analyzer.

Additionally it is important to verify the idle and the short case. Furthermore it is necessary to test if the calibration was done correctly. This is possible with the usage of a known resistance. Optimally, the value of the resistance should be constant over the whole frequency range.

The chosen test resistor in this case is a 51Ω MiniMelf (Mini-Metal electrode faces). The resistor value over the whole frequency range without performing an "Auto offset" (via "Port extension") is seen in figure 5.2.

5.2 Measurement preparation



Figure 5.1: Example of a self constructed measurement connection

The impedance progress of the resistor after a successful adjustment is illustrated in figure 5.3.

The marked point corresponds to the frequency, at which the resistor value

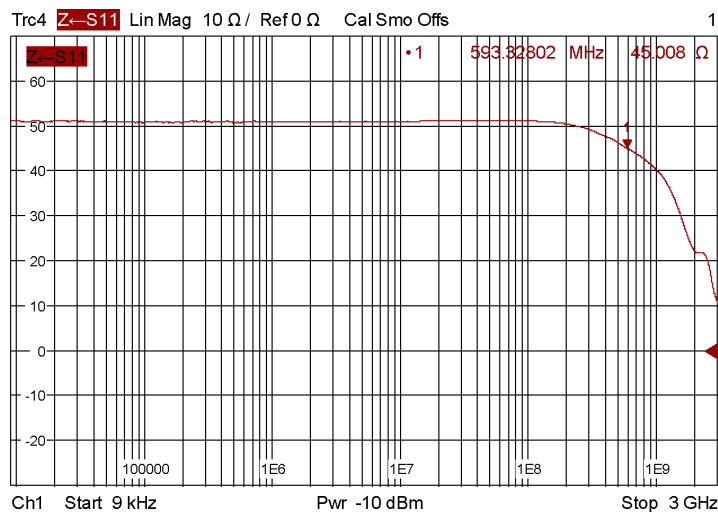


Figure 5.2: Measurement of a 51Ω MiniMelf without correction

is deviating up to 10% of the original value. This frequency is just under 2GHz, which is the reason, why the upcoming measurements are performed up to this frequency limit.

Another point at the calibration was clearly recognizable: the size of the loop, which is formed by the two wires (conductor and shielding) is influencing

5 Final measurement

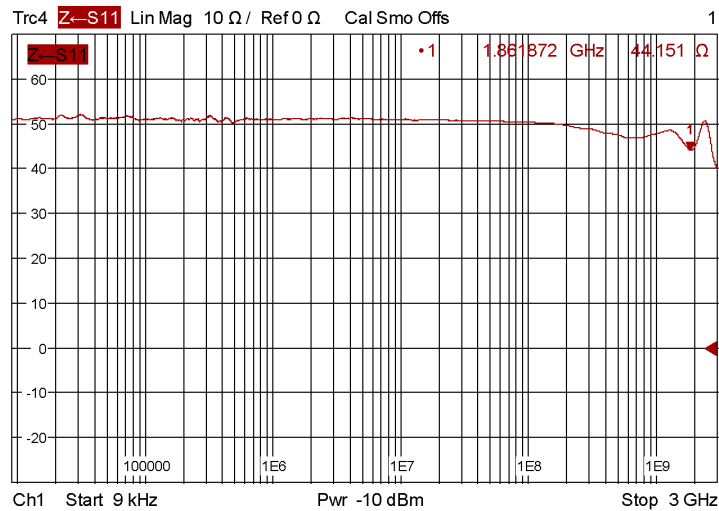


Figure 5.3: Measurement of a 51Ω MiniMelf after successful calibration

the waveform big-time. More to that in the conclusion section 5.4.

After finishing the calibration, the wires could be soldered at a wished solder joint at the printed circuit board.

The first approach was to measure the impedance characteristic directly at the batterie clip. But as attention should be paid to the dimensions of the constructed wire loop the LP2950 (a voltage regulator) is a better choice, due to its physical dimensions.

As a consequence, there will be two kinds of measurements. One up to the front (the batterie) and one to back, into the whole circuit. This leads to two observation courses of the PCB, which will be discussed with the measurement results, which will be illustrated in section 5.3. In figures 5.4 and 5.5 the chosen measurement points are marked. The voltage regulator as measurement point for port 1 of the network analyzer is marked in green. The measurement for port 2 for the measurement in the direction of the batterie is marked in yellow. The measurement point for port 2 for the second measurement (in direction of the whole port) is marked in red.

Figure 5.4 shows the schematic plan of the printed circuit board and figure 5.5 shows the manufactured board itself.

5.3 Measurement results

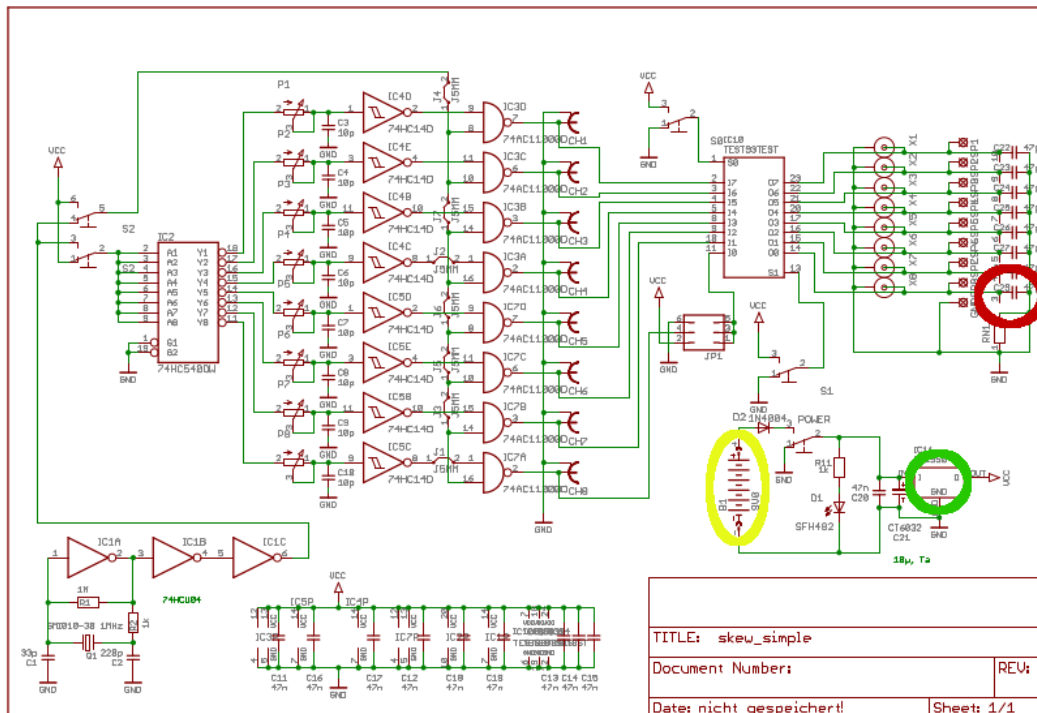


Figure 5.4: Schematic view of the analyzed printed circuit board

5.3 Measurement results

In the following three figures (5.6, 5.7 and 5.8), the results of the measurements are illustrated.

In figure 5.6, the impedance characteristics of the original, unmodified printed circuit board are illustrated. The red waveform reflects the view from the voltage regulator to the supply (further called batterie view). The blue waveform maps the view from the voltage regulator into the rest of the board (further called pcb view).

Figure 5.7 shows different traces of the batterie view.

The red curve is the original impedance characteristic. The blue-colored waveform illustrates the characteristic without the capacitor C21, which is a electrolytic tantalum capacitor with $10\mu\text{F}$.

5 Final measurement

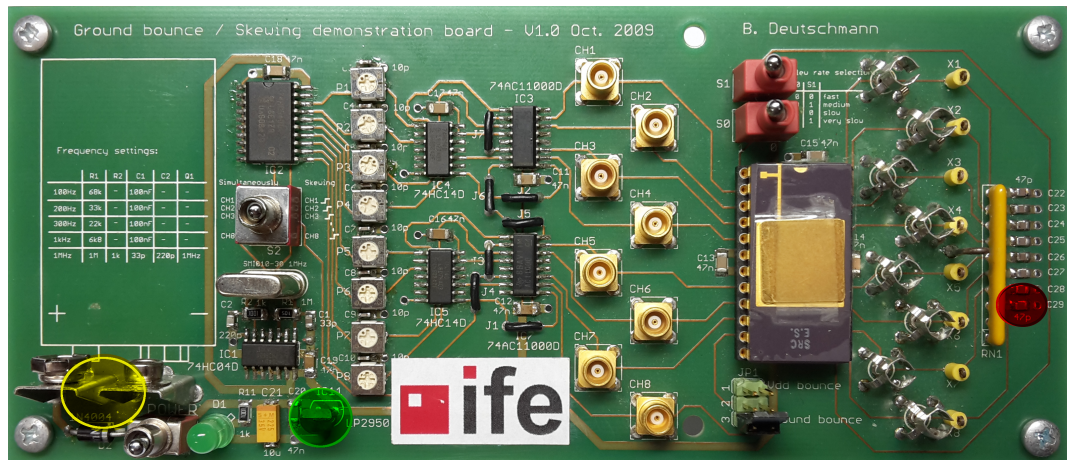


Figure 5.5: Original measurement board

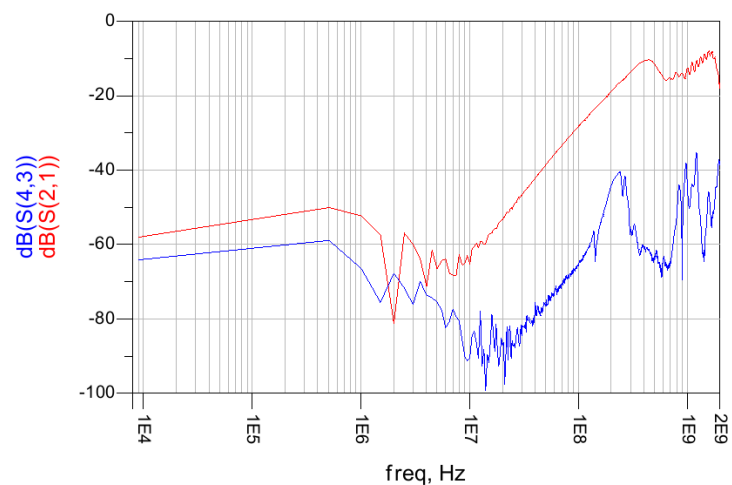


Figure 5.6: Characteristics of the printed circuit board in two different views

In figure 5.8 the measurements of the pcb view are displayed. The original characteristic is illustrated by the red trace. The green waveform is without one of the 9 47nF capacitors (C12), which serves as decoupling capacitors for the integrated circuits that are all parallel connected. For the blue trace, none of the planned capacitors is bridged. But a 1 μ F capacitor is

5.3 Measurement results

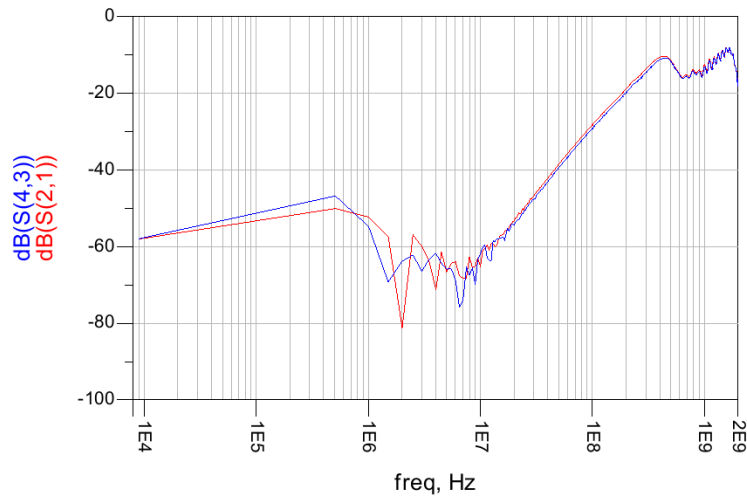


Figure 5.7: Characteristics of the original and modified board (batterie view)

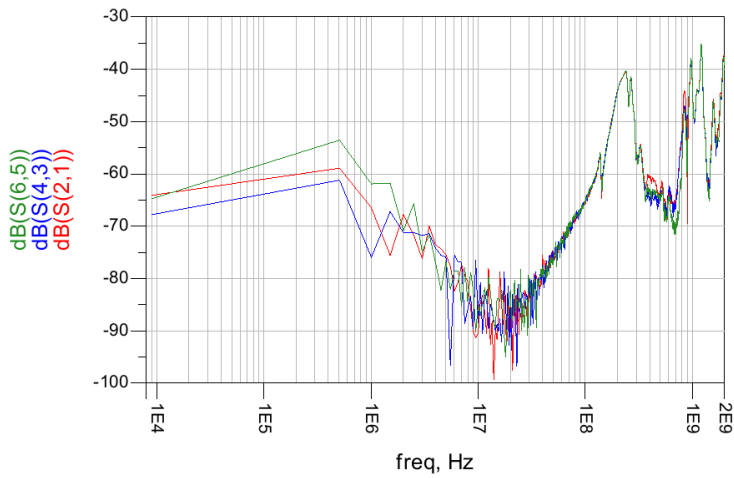


Figure 5.8: Characteristics of the original and modified board (pcb view)

connected parallel to the previous bridged C12 (and therefore also parallel to the other 8 47nF capacitors).

5.4 Final conclusion

These final measurements brought many valuable insights.

Already during the setup and the calibration it became obvious, that the measurement would not be as easy and straight forward as assumed.

Basically the calibration with an vector network analyzer is quite simple. If the measurement point is at a N- oder SMA-connector. But for the measurement on a completed board, which was not planned to be measured like this, this was not an option. So, the idea was to take an old SMA wire, chop it after a few centimeters and solder the conductor and the shield to the measuring point.

But during the calibration of the chopped wire, the problem manifested. Principally it is easy to shift the point of calibration (means the point from which the measurement is starting). But due to the fact, that the end of the measurement wire is chopped off (means, that there are just two wires, which aren't a 50Ω system), the calibration is to treat with caution. The slightest change of the wires and their formed loop leads to the necessity of a new calibration.

Another important point was seen during the reference measurement in figure 5.3. Despite the calibration, the frequency range, where the results concurs with the expactations, stops at approximately 2GHz.

Another reference measurement was made with two capacitors. By calculating the impedance of a capacitor at a specific frequency and comparing this value to the impedance measurement of the network analyzer, the calibration could be verified. The choosen capacitor values were $1\mu\text{F}$ and $2,2\mu\text{F}$ and the choosen frequency was 10kHz. The following calculations were performed:

$$Z = \frac{1}{2\pi fC} = \frac{1}{2 \cdot 3,14 \cdot 10 \cdot 10^3 \cdot 1 \cdot 10^{-6}} = 15,9\Omega \quad (5.1)$$

$$Z = \frac{1}{2\pi fC} = \frac{1}{2 \cdot 3,14 \cdot 10 \cdot 10^3 \cdot 2,2 \cdot 10^{-6}} = 7,2\Omega \quad (5.2)$$

That means, with a $1\mu\text{F}$ capacitor, the network analyzer should show $15,9\Omega$ at a frequency of 10kHz. With a $2,2\mu\text{F}$ capacitor it should show $7,2\Omega$ at the same frequency.

5.4 Final conclusion

This was achieved, so that was another confirmation of the performed calibration.

Regarding the measurement itself:

Figure 5.6 shows the characteristics of both views. The red waveform illustrates the characteristic of the batterie view and the blue one of the pcb view and both look reasonable.

With increasing frequency, the characteristic stays not as low as wished. The waveform of the pcb view is better than the waveform of the batterie view regarding the lowness of the characteristics.

When viewing figure 5.7, there is quite a difference expected, though for the blue waveform the $10\mu\text{F}$ capacitor is bridged.

But when observing figure 5.9, it becomes clear, why there is no consequence, when bridging C21. It simple has to less influence on the course of the characteristic.

When considering the characteristics of the pcb view, seen in figure 5.8, it

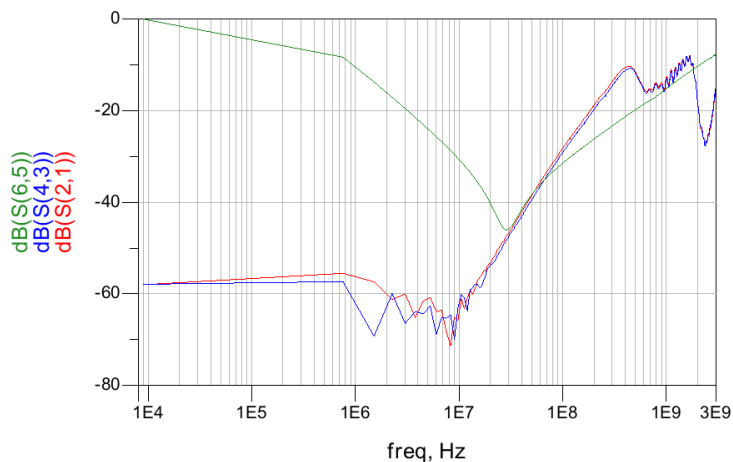


Figure 5.9: Impact of the bridged $10\mu\text{F}$ capacitor for the batterie view

is a similar situation as for the batterie view.

There is no noteworthy change, when modifying the printed circuit board. Neither the bridging of one of the many parallel capacitors (which should

5 Final measurement

bring an increasing at a resonance frequency), nor the adding of a $1\mu\text{F}$ capacitor is leading to a change in the waveforms. The slight differences seen between the measurements are explainable with the delicate measurement setup.

But as discussed before for the batterie view, the impacts for the whole printed circuit board is to little to see in the characteristics. Figure 5.10 shows the visual explanation, why the modifications did not change the characteristics as wished for.

The red waveform is the characteristic of the original, not modified, pcb.

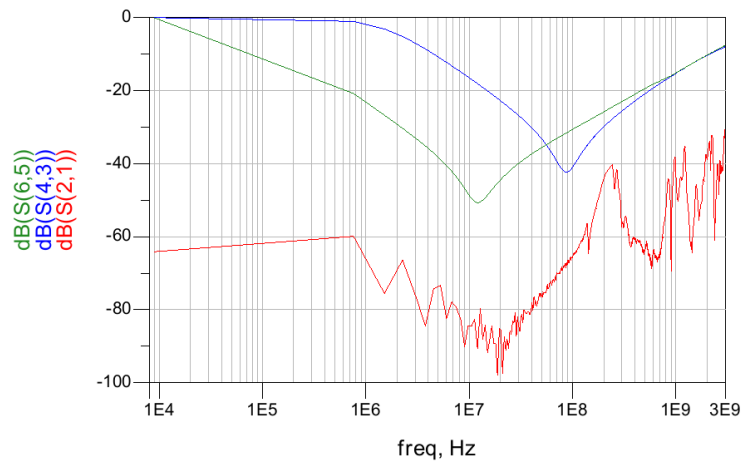


Figure 5.10: Impact of the bridged and added capacitor for the pcb view

The green curve shows the characteristic of a single $1\mu\text{F}$ capacitor and the blue one illustrates the characteristic of one 47nF capacitor. The two characteristics of the single capacitors both show a too high impedance to influence the overall characteristic.

First, the measurements of this chapter were performed with a one port measurement, regarding the fact, that there are just differences in the accuracy of the impedance ranges when measuring [21]. Another reason for measuring with just one port is the minimization of error sources, when just having one self-made measurement probe instead of two. But there is one other thing to bear in mind.

5.4 Final conclusion

The comparison of a S11 characteristic to a S21 characteristic is like comparing apples and pears.

So the first done one-port measurements was not really informative when trying to compare it to the measurements made before.

As a final summary could be said, that the considerations so far could not be turned into real measurement results.

This leads to the assumption, that the approaches so far still were to simple.

6 Summary and outlook

Summarizing is to say, that not all measurement results were as expected. In the first of the four relevant chapters some background information was listed. These information were gathered in a combination of literature research and the study of Telematics.

In the first practical chapter, a detailed description of the upcoming measurements on the basis of an example measurement is given. During this example measurement, a side issue was the development of a real equivalent circuit diagram. This was quite elaborating, because this equivalent circuit diagram also images the deviations because of soldering and the measurement setup.

Also a comparison between all measured capacitor characteristic and their characteristics provided by the capacitors manufacturer is noted.

In the second measurement chapter, the procedure is guided by an idea during a previous project [1].

The capacitor values are chosen, like thought of during that mentioned project, without any background knowledge. First experiments by connecting two capacitors parallel and afterwards, as underlying objective, a parallel circuit with four capacitors. As a consequence, the overall characteristic was not as low as wished for. Therefore improvements regarding the selection of capacitor values had to be made. Due to the results of the literature research the first improvement steps exposed a overall characteristic as expected.

In the last practical chapter, the insights of the previous experiments was used.

A given printed circuit board was characterized and the idea was to show, how bridging or adding of designated capacitors influence the characteristic. It was not possible to confirm this assumption within this thesis. But this

6 Summary and outlook

leads to the conclusion, that the characteristic is possible not just influenced by the capacitors itself (with value and construction), but also by the placement of them on the board in relation to the other components.

Furthermore this topic is also present at the Insitute of Electronics. It is planned to build up a summary of characterisation of all kinds of capacitors. The measurements of this thesis will also be found in this summary. Moreover it would be interesting to pursue the idea of measuring the characteristic of a whole PCB. The calibration and the measurement itself should be developed alright, but the modifications of the board deserve another view.

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