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A Low Quiescent Current LDO Regulator Operating at High Temperature

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Abstract

In this thesis a low-drop-out regulator for a high temperature region of −40 °C up to 200 °C was designed. The output voltage can be set either to 2.65 V or 2.95 V. A drop-out voltage of 100 mV had to be achieved while sourcing a load current up to 50 mA.

A comparison between NMOS and PMOS as pass device showed that using a PMOS transistor is the more suitable choice for this application. Due to the high supply voltage up to 8 V, the pass device had to be a high voltage transistor. The smaller current gain compared with low voltage transistors leads to a large pass device. For driving this large pass device an adaptive biasing stage was introduced. For the error amplifier the concept of a reversed nested Miller compensation with current buffers was applied.

This regulator was designed in a 0.35 µm high voltage CMOS process. Also, a test-chip was manufactured and evaluated. The current consumption of the measured LDO is about 70 µA under low load condition and increases up to about 150 µA at high load currents. For the minimum input voltage and high temperatures the quiescent current can reach values up to 1.6 mA. Over the whole temperature region, the output voltage varies about 9 mV for an output current of 250 µA and about 30 mV for an output current of 50 mA.

Contents

1 Introduction

With the trend to smaller supply voltages, low-drop-out (LDO) regulators are widely used. An LDO is a voltage regulator with the ability to hold the output voltage constant, even if the difference between the supply and the output voltage gets small. With the increasing complexity of integrated circuits the LDO has also to be able to deliver high load currents. In battery powered devices it is very important to hold the quiescent current as low as possible in order to achieve a long battery runtime. Also critical are overshoots and undershoots, caused by fast changes of the load current, which could cause a reset or turning off of the device [1].

In order to source high load currents at low supply voltages the pass device has to be large. This introduces a high gate capacitance which causes the non-dominant pole to get down to lower frequencies. The unity gain frequency (UGF) increases with the load current to a higher frequency than the non-dominant pole. This introduces instability. By applying an adaptive biasing stage the non-dominant pole gets pushed up to higher frequencies for higher load currents and the LDO stays stable [2].

In this work an LDO has to be designed with a drop-out voltage of 100 mV and a quiescent current of less then 100 µA. The challenge is the high temperature region of −40 °C to 200 °C. At higher temperatures the leakage currents are strongly increasing. A rule of thumb says, with every 10 °C increase of temperature the leakage current gets multiplied by two [3]. Thus, it will be hard to achieve a low quiescent current consumption at high temperature.

The LDO was implemented on a test-chip to test the functionality and compare its behaviour with the simulation results. For the evaluation over the temperature region a thermostream is used.

Section 2 explains the functionality and important properties of LDOs. Section 3 shows the given specification for the LDO which have to be achieved. Important error sources and their calculation are presented in section 4. The comparison between NMOS and PMOS transistor as pass device is made in section 5.

Section 6 shows the pole/zero analysis for a one stage error amplifier and an error amplifier with reverse nested Miller compensation. The final design and the simulation results are discussed in section 7. In section 8 the structure of the designed test-chip is explained. The evaluation results for the test-chip are shown in section 9.

2 Low-Drop-Out Voltage Regulators

Figure 2.1 shows the block diagram of a low-drop-out linear voltage regulator (LDO) [4]. To the left hand side the input voltage v_{in} is applied. The pass device can be seen as a current source, which always sources as much current as needed to hold the output voltage constant at a specific level. The output voltage is sensed by the resistors $R1$ and $R2$ and compared to an accurate reference voltage *Vref*. The comparison is done by an amplifier which controls the pass device.

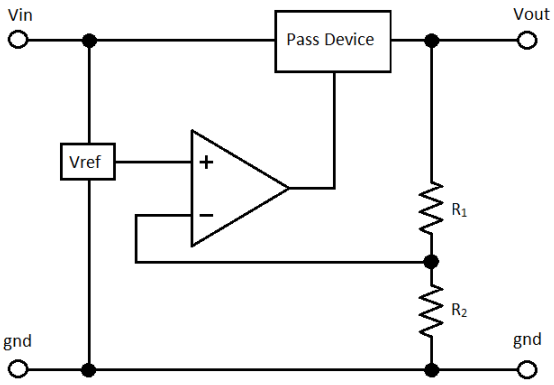

Figure 2.1: Block diagram of an LDO. The amplifier compares the sensed output voltage with a reference voltage and controls the pass device.

The pass device can be either a bipolar transistor or a MOS transistor. The bipolar transistor has the advantage of a higher current source capability but the MOS transistor needs less quiescent current [4]. In this thesis a MOS transistor was used as pass device because the LDO was produced in a high voltage CMOS process where the necessary bipolar devices were not available.

The drain current of a MOS transistor in saturation can be approximated [5] to

$$I_D = \frac{K'}{2}\frac{W}{L}(V_{gs} - V_{th})^2, \tag{2.1}$$

where K' is a process dependent parameter, W and L are the width and length of the transistor respectively, V_{gs} is the gate-source voltage and V_{th} the threshold voltage of the transistor. This shows that the drain current depends quadratically on the gate-source voltage. Therefore, the transistor can be seen as a voltage controlled current source.

The drop-out voltage is the minimum voltage between input and output, or rather the drain-source voltage of the pass device, which is needed for the regulator to work properly. If the input voltage gets smaller than the drop-out voltage, then the regulator is not able to source enough current to the load any more and the output voltage decreases. With further reducing the input voltage, also the voltage controlling the pass device (V_{gs}) is decreasing until the regulator shuts off. This behaviour is illustrated in figure 2.2 [4]. Thus, a low-drop-out regulator is a voltage regulator which can handle small voltage differences between input and output voltage.

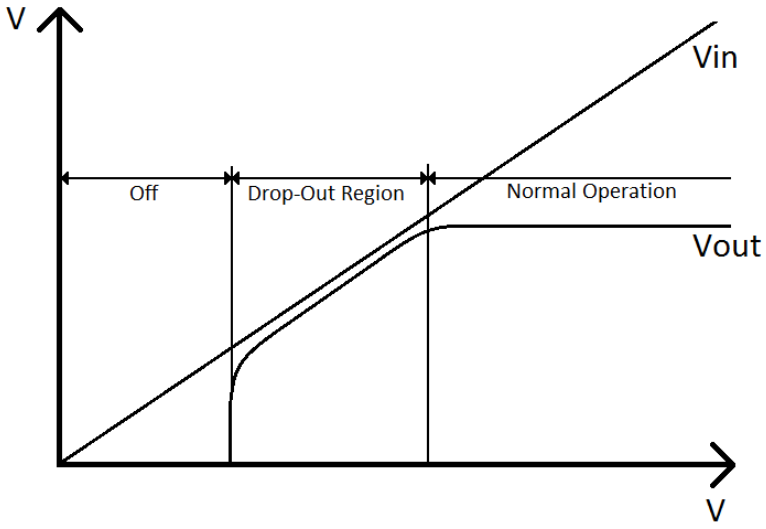

Figure 2.2: Input/output characteristic of an LDO. For lower input voltages than the drop-out voltage the output voltage decreases. At some point the LDO shuts off.

The load regulation parameter determines the dependency of the output voltage on the load current. Increasing the load current leads to a reduction of the

output voltage. The load regulation [4] is defined as

$$\text{Load Regulation} = \frac{\Delta V_{out}}{\Delta I_{Load}}, \tag{2.2}$$

where ΔV_{out} is the variation of the output and ΔI_{Load} is the variation of the load current.

The ability to maintain the output voltage constant with a varying input voltage is called line regulation [4] and is defined as

$$\text{Line Regulation} = \frac{\Delta V_{out}}{\Delta V_{in}}, \tag{2.3}$$

where again, ΔV_{out} is the variation of the output voltage and ΔV_{in} is the variation of the input voltage. This variation of the input voltage could be caused by a discharging battery. Ideally, the regulator holds the output voltage constant, until the input voltage gets lower than the drop-out voltage and the regulation begins to fail. In reality, the finite open loop gain causes a variation of the output voltage.

3 Specification of the LDO

The specification for the LDO is shown in table 3.1. The maximum deviation of the output voltage (150 mV) includes the error induced by inaccuracies of the bandgap and the output error of the LDO. The LDO should be able to switch between two output voltages (2.65 V and 2.95 V) and source a load current up to 50 mA. The minimum supply voltage is 2.75 V, therefore the drop-out voltage has to be 100 mV. The external output capacitor is given with 1 µF and its equivalent series resistor of 10 mΩ to 100 mΩ.

Specifications	
Temperature	−40 °C to 200 °C
Supply voltage	2.75 V to 8 V
Quiescent current consumption	$<$100 µA
External output capacitance	1 µF +20 % / −50 %
Equivalent series resistor	10 mΩ to 100 mΩ
Output voltage	2.65 V or 2.95 V
Output error*	±150 mV
Load current	250 µA to 50 mA

*Including load- and line regulation, over- and undershoots and bandgap error.

Table 3.1: Specification of the LDO.

4 Error Calculation

The maximum output error is split into two parts: The output error of the bandgap and the output error of the LDO.

The maximum error in percent can be calculated as:

$$E_{out} = \frac{V_{err}}{V_{out}} 100\,\% \tag{4.1}$$

Where V_{err} is the maximum output deviation and V_{out} is the desired output voltage.

For an output voltage of 2.65 V this gives an error of

$$E_{out,2.65} = \frac{V_{err}}{V_{out}} 100\,\% = \frac{0.15\,\mathrm{V}}{2.65\,\mathrm{V}} 100\,\% = 5.66\,\% \tag{4.2}$$

and for an output voltage of 2.95 V

$$E_{out,2.95} = \frac{V_{err}}{V_{out}} 100\,\% = \frac{0.15\,\mathrm{V}}{2.95\,\mathrm{V}} 100\,\% = 5.08\,\%. \tag{4.3}$$

By having a look at an existing bandgap with 6-bit trimming, an accuracy of 1.563 mV can be achieved. For the nominal output voltage of this bandgap of 1.237 V this would be 0.12 %. This bandgap also has a temperature coefficient of 30 ppm, which means a tolerance of about 0.3 % in its temperature region up to 125 °C. Together, this gives an error of about 0.42 %. At higher temperatures this accuracy will be much harder to achieve, therefore the maximum allowed error of the bandgap is set to 2 %. Now, at 2.65 V output voltage the maximum deviation of the LDO output is $E_{LDO,2.65} = 3.66\,\%$ and at 2.95 V the maximum deviation is $E_{LDO,2.95} = 3.08\,\%$.

This means, the absolute error for the 2.65 V output voltage is

$$E_{abs,2.65} = V_{out} \cdot E_{LDO,2.65} = 2.65\,\mathrm{V} \cdot 0.0366 = 96.99\,\mathrm{mV} \tag{4.4}$$

and for the 2.95 V output voltage

$$E_{abs,2.95} = V_{out} \cdot E_{LDO,2.95} = 2.95\,\text{V} \cdot 0.0308 = 90.86\,\text{mV}. \tag{4.5}$$

The main error sources are the gain error due to the finite open loop gain of the error amplifier, the mismatch error of the feedback resistors, the offset error of the error amplifier, over- and undershoots and load regulation.

Figure 4.1 shows the error budget for the output voltage of 2.95 V. The borders of 3.1 V and 2.8 V are given by the maximum error of 150 mV. The minimum and maximum bandgap voltages, which are $1.2\,\text{V} - 2\,\% = 1.176\,\text{V}$ and $1.2\,\text{V} + 2\,\% = 1.224\,\text{V}$ are introducing an error of $2.95\,\text{V} \cdot (\pm)2\,\% = \pm 59\,\text{mV}$. The remaining 91 mV for the LDO are split in 2 parts. One part with 71 mV for over- and undershoots and one part with 20 mV for the other error sources.

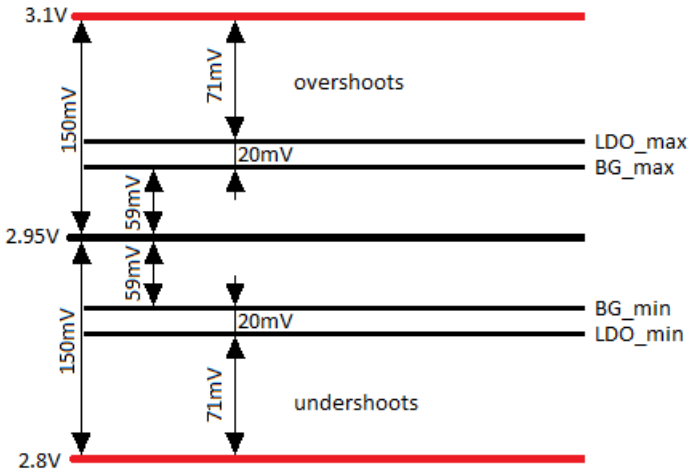

Figure 4.1: Error budget of the LDO. The ±150 mV error budget are split into the error caused by the bandgap (±59 mV), the error caused by over- and undershoots (±71 mV) and the other error sources like offset error, load regulation and line regulation (±20 mV).

4.1 Gain error

Figure 4.2 shows a non-inverting amplifier with finite open loop gain A and the feedback resistors R_1 and R_2. The current through R_2 can be determined to

$$I_{R2} = \frac{V_{in} - V_d}{R_2}. \tag{4.6}$$

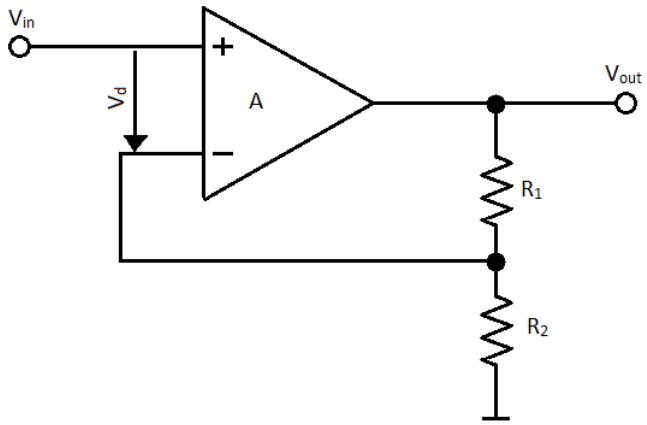

Figure 4.2: Schematic of a non-inverting amplifier

Due to the high input resistance of the amplifier there is no current flowing into the negative input, therefore the same current is flowing through R_1, which can be calculated to

$$I_{R1} = \frac{V_{out} - (V_{in} - V_d)}{R_1}. \tag{4.7}$$

The output voltage is given by the product of the open loop gain and the input differential voltage:

$$V_{out} = A \cdot V_d. \tag{4.8}$$

With $I_{R_1} = I_{R_2}$ and eliminating V_d through equation 4.8 the closed loop gain A_{CL} can be determined to

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{1}{\frac{R_2}{R_1+R_2} - \frac{1}{A}}. \tag{4.9}$$

For infinite open loop gain A the closed loop gain can be rewritten as

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{R_1 + R_2}{R_2}. \tag{4.10}$$

By subtracting the maximum deviation of the output (V_{Gain_Err}) caused by the gain error, equation 4.9 can be rewritten to

$$A_{min} = \frac{1}{\frac{V_{in}}{V_{out} - V_{Gain\_Err}} - \frac{R_2}{R_1+R_2}}, \tag{4.11}$$

which is the minimum necessary gain, in order to get a certain gain error.

4.2 Resistor matching error

In order to save area, resistors should be as small as possible. The matching error of two equal resistors [6] can be calculated by

$$\sigma^2 = \frac{A_R^2}{W \cdot L} \tag{4.12}$$

Where σ is the standard deviation, A_R is the mismatch parameter which is process dependent and W and L are the width and length of the resistor respectively. By rearranging this equation the required minimum area can be calculated to

$$Area = W \cdot L = \left(\frac{A_R}{\sigma}\right)^2. \tag{4.13}$$

5 Comparison of Possible Pass Devices

The pass device can either be an NMOS or a PMOS transistor. The NMOS transistor would be used in common drain configuration, also known as source-follower [5], and the PMOS would be used in common source configuration. Both concepts have their advantages and disadvantages.

5.1 NMOS Transistor as Pass Device

The NMOS pass device is operating in common drain configuration. In figure 5.1 the schematic of an LDO with an NMOS pass device is shown. The drain is connected to the supply voltage V_{DD}, the source is connected to the output and the gate is connected to the output of the error amplifier. The gate-source voltage has to be higher than the threshold voltage of the pass device in order to source the output current. If the error amplifier is supplied with V_{DD}, then the maximum output voltage of the error amplifier is limited to this supply voltage. Therefore the gate voltage of the pass device cannot get higher than the supply voltage. For supply voltages smaller than the output voltage plus the gate-source voltage, the gate voltage gets decreased and the pass device is not able to source the output current any more. By supplying the error amplifier with a higher voltage than the supply voltage, the gate voltage can be held, even if the supply voltage gets smaller than the gate voltage. This higher voltage for the error amplifier can be achieved by using a charge pump [7, 8].

Due to the source follower configuration, the NMOS has a gain of about one [9]. This makes it much easier to get the LDO stable because the gain does not change with the load current and the pass device does not introduce an additional phase shift.

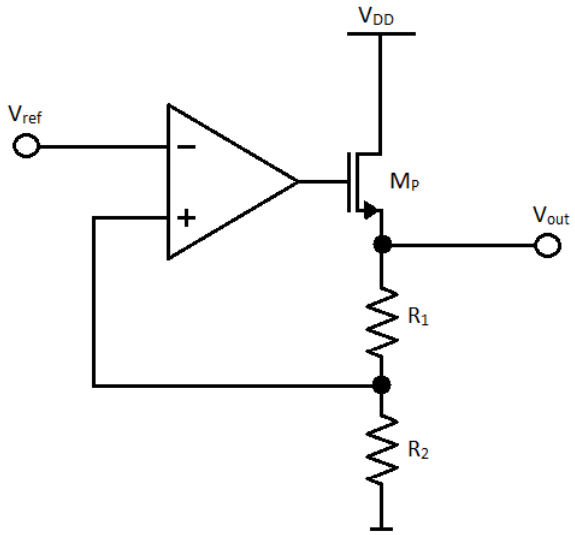

Figure 5.1: Schematic of an LDO with NMOS pass device. The pass device is operating in common-drain configuration.

Another advantage of the NMOS over the PMOS pass device is the higher mobility of the charge carriers which leads to a smaller transistor size [7]. This reduces the necessary chip area and decreases the gate-source capacitance.

The main issues of charge pump circuits are area efficiency, power efficiency and output voltage ripple. The charge pump has to be able to deliver high output currents and have a fast ramp-up time. The NMOS LDO with charge pump basically only makes sense if the area required by the charge pump plus the area required by the pass device is smaller than an equivalent PMOS pass device. The clock frequency has to be chosen so, as to avoid electro magnetic interference [10, 11].

The line regulation [12] can be calculated to

$$\frac{\Delta V_{out}}{\Delta V_{DD}} \approx \frac{1}{g_{mP}\, r_{outP} \left(A \, \frac{R_2}{R_1+R_2} \right)}, \tag{5.1}$$

where g_{mP} is the transconductance of the pass device, r_{outP} is the output resistance of the pass device, A is the open loop gain of the error amplifier and R_1 and R_2 are the feedback resistors. Therefore the intrinsic gain of M_P and the loop gain $A \cdot R_2/(R_1 + R_2)$ are determining the line regulation of the voltage regulator with an NMOS pass device. In order to achieve a high line regulation, a high open loop gain of the error amplifier is necessary.

The load regulation [12] of a regulator with NMOS pass device is given by

$$\frac{\Delta V_{out}}{\Delta I_{load}} \approx -\frac{1}{g_{mP}\, A\, \frac{R_2}{R_1+R_2}}, \tag{5.2}$$

with the transconductance of the pass device g_{mP}, the open loop gain of the error amplifier A and the feedback resistors R_1 and R_2. The load regulation is dependent on the open loop gain. Therefore the error amplifier should have a high open loop gain.

5.2 PMOS Transistor as Pass Device

The PMOS pass device is operating in common source configuration and has therefore much more gain than unity. This introduces another gain stage which changes its gain depending on the output current. Another disadvantage of a PMOS pass device is that the mobility of the charge carriers is much lower than with an NMOS and therefore the device has to be larger than an NMOS pass device under the same conditions [7].

The advantage of the PMOS pass device is that there is no need for a charge pump to work properly. A charge pump would introduce an additional current consumption and increase the chip area due to its switches and capacitors [13]. Also an oscillator is necessary to drive the charge pump. This again, results in a higher current consumption and chip area. Therefore, using a PMOS transistor as pass device needs much less effort for realisation.

In figure 5.2 an LDO with a PMOS pass device is illustrated. The source of the PMOS is connected to the supply voltage, which means in order to turn the output current off, the gate voltage only needs to be higher than the supply voltage minus the threshold voltage.

The line regulation [12] is given by

$$\frac{V_{out}}{V_{DD}} \approx \frac{1}{A\, \frac{R_2}{R_1+R_2}}, \tag{5.3}$$

where A is the open loop gain of the error amplifier and R_1 and R_2 are the feedback resistors. Compared with the line regulation of an LDO with NMOS pass device (equation 5.3) the line regulation is inferior by the factor $g_{mP}\, r_{outP}$. Thus, the open loop gain is even more important in order to achieve a good line regulation.

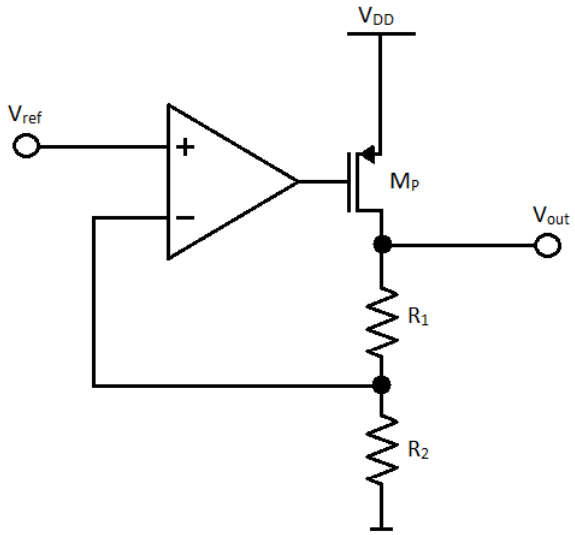

Figure 5.2: Schematic of an LDO with PMOS pass device. The pass device is operating in common-source configuration.

The load regulation [12] is given by

$$\frac{\Delta V_{out}}{\Delta I_{load}} \approx -\frac{1}{g_{mP}\, A\, \frac{R_2}{R_1+R_2}} \tag{5.4}$$

Again, A is the open loop gain of the error amplifier, g_{mP} is the transconductance of the pass device and R_1 and R_2 are the feedback resistors. Therefore, the load regulation is determined by A and g_{mP}.

5.3 Selected Pass Device

Using an NMOS as pass device would make it easier to get the LDO stable due to the unity gain and zero phase shift, but the required charge pump introduces another issues like a higher current consumption, additional silicon area, voltage ripple in the supply voltage for the error amplifier and electro magnetic interference. Using a PMOS as pass device introduces an additional phase shift and makes it harder to get the LDO stable. In order to avoid issues through the additional circuitry with the NMOS as pass device, the PMOS pass device was chosen.

Due to the high supply voltage a high voltage PMOS is necessary. In the H35 process there are three different 20 V transistors available. One with a thin gate oxide which has a maximum gate-source voltage of 3.6 V, one with a mid gate oxide which can withstand a gate-source voltage of 5 V and one with a thick gate oxide which has a maximum gate-source voltage of 20 V.

The PMOS with the thick gate oxide, has a threshold voltage of about 2 V and the lowest current gain of these three transistor types. At minimum supply voltage of 2.75 V it is only possible to get the gate-source voltage 0.75 V higher than the threshold voltage. This is not enough in order to source 50 mA. The PMOS transistor with the thin gate oxide has the smallest threshold voltage and the highest current gain. But this transistor has high leakage currents at high temperature, so it would be necessary to have a higher gate voltage than the supply voltage to turn the output current off. The remaining PMOS transistor with mid gate oxide, lies in the middle. The threshold voltage is high enough to turn the output current off and low enough to be able to deliver 50 mA.

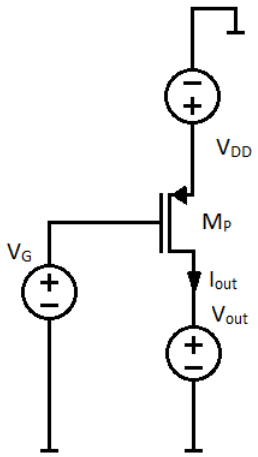

Figure 5.3: Schematic for determining the transistor size. The drain-source current is measured for a fixed drain, source and gate voltage.

Figure 5.3 illustrates the schematic which was used to determine the transistor size. At source, drain and gate an ideal voltage source has been applied. The source voltage V_{DD} was set to the minimum supply voltage and the gate voltage V_G was set to 300 mV, because the error amplifier cannot go further down than a saturation voltage of its output transistors. The drain voltage V_{out} was set to the desired output voltage. After simulating this circuit over all process

corners and the minimum and maximum temperature, the corner with the smallest current I_{out} was picked out. The drain current is proportional to the width and inverse proportional to the length of the transistor (see equation 2.1). By holding the length of the transistor constant the necessary width for a particular current can be calculated to

$$W_{new} = W_{old} \frac{I_{des}}{I_{min}}. \tag{5.5}$$

Where W_{old} is the width of the transistor used for the simulation, I_{des} is the desired maximum output current and I_{min} is the minimum current over the simulated corners.

To simulate the leakage current the gate voltage was set to the supply voltage in order to shut the device off. The maximum leakage current appears at the maximum drain source voltage, therefore the supply voltage of 8 V was applied. After a simulation over all process corners and maximum temperature, the current was measured. Table 5.1 shows the result of the simulation. The leakage current flowing from the source pin to the substrate ($I_{leak,sub}$) is 5.2 µA and the current from source to drain ($I_{leak,sd}$) is 1.4 µA.

$I_{leak,sub}$	$I_{leak,sd}$
5.2 µA	1.4 µA

Table 5.1: Leakage currents of the pass device.

6 Error Amplifier

The error amplifier compares the reference input voltage with the output voltage and controls the gate voltage of the pass device.

6.1 Pole/Zero Analysis with an Ideal One Stage Error Amplifier

The ideal error amplifier was modelled by a voltage controlled current source with a transconductance g_{m1} and an output resistor R_1. The small signal model of the ideal error amplifier and the pass device is presented in figure 6.1. The pass device has a parasitic capacitance C_{GS} between the gate and source pin and a parasitic capacitance C_{GD} between gate and drain.

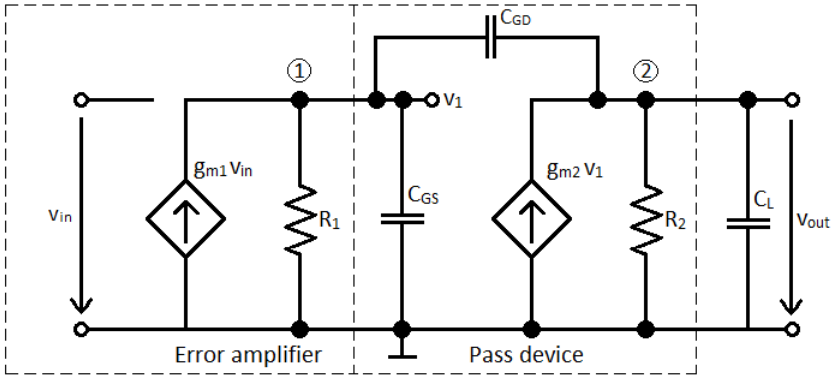

Figure 6.1: Small signal model of an ideal error amplifier and pass device. The error amplifier is modelled by an ideal current source and an output resistor. The pass device is modelled by an ideal current source, an output resistor, a gate-drain capacitance and a gate-source capacitance. C_L is the external output capacitor.

The equations for the currents of nodes 1 and 2 are given by

$$-\mathrm{v}_{in}\, g_{m1} + \frac{\mathrm{v}_1}{R_1} + \mathrm{v}_1\, s\, C_{GS} + (\mathrm{v}_1 - \mathrm{v}_{out})\, s\, C_{GD} = 0 \tag{6.1}$$

and

$$g_{m2}\, \mathrm{v}_1 + (\mathrm{v}_{out} - \mathrm{v}_1)\, s\, C_{GD} + \frac{\mathrm{v}_{out}}{R_2} + \frac{\mathrm{v}_{out}}{\frac{1}{s\, C_L}} = 0. \tag{6.2}$$

By solving this system of equations the numerator and denominator of the transfer function $T(s) = \mathrm{v}_{out}/\mathrm{v}_{in}$ can be determined to

$$Numerator(T(s)) = g_{m1}\, R_1\, g_{m2}\, R_2 \left(1 - \frac{C_{GD}}{g_{m2}}\, s\right) \tag{6.3}$$

$$Denominator(T(s)) = 1 + (C_{GS}\, R_1 + C_{GD}\, R_1 + C_L\, R_2 + C_{GD}\, R_2 + C_{GD}\, g_{m2}\, R_1\, R_2)\, s$$
$$+ (C_{GS}\, C_{GD}\, R_1\, R_2 + C_L\, C_{GD}\, R_1\, R_2 + C_{GS}\, C_L\, R_1\, R_2)\, s^2 \tag{6.4}$$

From equation 6.3 the open loop gain A_{OL} can be determined to

$$A_{OL} = g_{m1}\, R_1\, g_{m2}\, R_2 \tag{6.5}$$

and a zero, caused by the capacitance C_{GD}, can be found at

$$z_1 = \frac{g_{m2}}{C_{GD}}. \tag{6.6}$$

This zero is located at the right half plane which could cause stability issues. Located at too low frequencies, it would increase the unity gain frequency and decrease the phase margin.

In equation 6.4 the terms $C_{GD}\, R_1$ and $C_{GD}\, R_2$ can be neglected, because these two terms are much smaller than $C_{GD}\, g_{m2}\, R_1\, R_2$. Also the term $C_{GS}\, C_{GD}\, R_1\, R_2$ can be neglected because it is smaller than the other two terms. Now, the denominator of $T(s)$ can be rewritten as

$$Denominator(T(s)) = 1 + a'\, s + b'\, s^2 \tag{6.7}$$

where

$$a' = C_{GS}\, R_1 + C_L\, R_2 + C_{GD}\, g_{m2}\, R_1\, R_2 \tag{6.8}$$

and

$$b' = C_L\, C_{GD}\, R_1\, R_2 + C_{GS}\, C_L\, R_1\, R_2. \tag{6.9}$$

By comparing equation 6.7 with

$$(1 + a\,s)(1 + b\,s) = 1 + (a + b)\,s + (a\,b)\,s^2, \tag{6.10}$$

and assuming that the dominant pole lies at much lower frequencies than the second pole ($a \gg b$), the dominant pole can be approximated [5] to

$$p_1 = -\frac{1}{a} \approx -\frac{1}{a'} = -\frac{1}{C_{GS}\,R_1 + C_L\,R_2 + C_{GD}\,g_{m2}\,R_1\,R_2} \tag{6.11}$$

and the non-dominant pole to

$$p_2 = -\frac{1}{b} \approx -\frac{a'}{b'} = -\frac{C_{GS}\,R_1 + C_L\,R_2 + C_{GD}\,g_{m2}\,R_1\,R_2}{C_L\,C_{GD}\,R_1\,R_2 + C_{GS}\,C_L\,R_1\,R_2}. \tag{6.12}$$

Due to the Miller effect C_{GD} appears $g_{m2}\,R_2$ times larger than its real value [5]. This pushes the dominant pole to lower frequencies. The second pole has the Miller capacitance in the numerator, which means that this pole will be pushed to higher frequencies.

Due to the equivalent series resistance (ESR) of the output capacitor a second zero [14] appears at

$$z_2 = -\frac{1}{R_{ESR}\,C_L}. \tag{6.13}$$

This zero is located on the left half plane and can be used to compensate the second pole in order to gain stability [2].

Now, the transfer function of this model can be written as

$$T(s) = \frac{\mathrm{v}_{out}}{\mathrm{v}_{in}} \approx A_{OL}\,\frac{(1 - \frac{C_{GD}}{g_{m2}}\,s)(1 + R_{ESR}\,C_L\,s)}{(1 + \frac{1}{p1}\,s)(1 + \frac{1}{p2}\,s)}. \tag{6.14}$$

By setting $p_2 = m \cdot p_1$, the necessary capacitance, in order to split the poles by the factor m, can be determined:

$$C_{GD} \approx 0.5\,\frac{\sqrt{4\,m\,C_L\,C_{GS}\,R_1\,R_2}}{g_{m2}\,R_1\,R_2} \tag{6.15}$$

The load capacitance C_L can vary from 500 nF to 1.2 µF and the equivalent series resistor from 10 mΩ to 100 mΩ. Therefore, the zero z_2 can be located between

$$f_{z,min} = \frac{1}{2\pi\,R_{ESR,max}\,C_{L,max}} = \frac{1}{2\pi \cdot 100\,\mathrm{m\Omega} \cdot 1.2\,\mu\mathrm{F}} = 1.33\,\mathrm{MHz} \tag{6.16}$$

and

$$f_{z,max} = \frac{1}{2\pi\, R_{ESR,min}\, C_{L,min}} = \frac{1}{2\pi \cdot 10\,\mathrm{m\Omega} \cdot 500\,\mathrm{nF}} = 31.83\,\mathrm{MHz}. \tag{6.17}$$

By setting the transconductance g_{m1} of the error amplifier to 10 µS and its output resistance R_1 to 100 MΩ, the small-signal parameters of the pass device can be determined by simulation. Figure 6.2 shows the schematic used to get the small-signal parameters and the pole frequencies. The current through the feedback-resistors was set to 5 µA in order to hold the current consumption low. To archive an output voltage of 2.65 V the closed-loop gain has to be

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{2.65\,\mathrm{V}}{1.2\,\mathrm{V}} = 2.20833. \tag{6.18}$$

By rewriting equation 4.10, the necessary ratio of the feedback resistors can be calculated to

$$\frac{R_{f1}}{R_{f2}} = A_{CL} - 1 = 2.20833 - 1 = 1.20833. \tag{6.19}$$

Now, with the current through the feedback resistors and the voltage over R_{f2}, which is equal to the input voltage, R_{f2} can be calculated:

$$R_{f2} = \frac{V_{Rf2}}{I_{Rf2}} = \frac{1.2\,\mathrm{V}}{5\,\mathrm{\mu A}} = 240\,\mathrm{k\Omega} \tag{6.20}$$

By rearranging equation 6.19 R_{f1} can be determined to

$$R_{f1} = R_{f2}\,(A_{CL} - 1) = 240\,\mathrm{k\Omega}\,(2.20833 - 1) = 290\,\mathrm{k\Omega} \tag{6.21}$$

Table 6.1 shows the DC simulation results and the pole frequencies for minimum and maximum supply voltage and for minimum and maximum load current. In figure 6.3 the AC response of the LDO is shown. The upper figure shows the gain and phase for no load current and full load current of the LDO with a supply voltage of 2.75 V and the lower figure with the maximum supply voltage of 8 V.

By increasing the output current, the output resistance gets decreased. Thus, the pole at the output moves up to higher frequencies and the inner pole gets dominant. At low output currents the output resistance gets very high and the output pole is coming down to very low frequencies and gets dominant. Due to the pole movement over several decades it is very hard to gain stability.

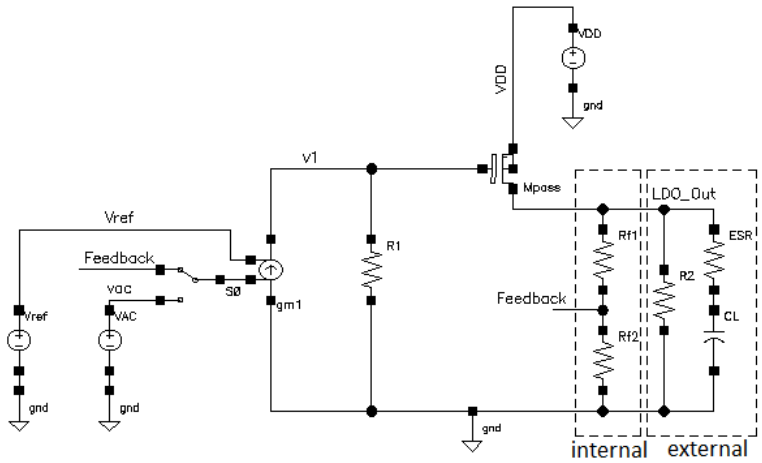

Figure 6.2: Schematic for the simulation of an one stage error amplifier. R_{f1} and R_{f2} are building the feedback network. With $S0$ the input can be connected to the feedback node for the DC-simulation or to the AC-source for the AC-simulation. R_2 and C_L with its equivalent series resistor (ESR) are representing the external load.

One approach would be using the Miller effect. By putting the small signal values of the point where the poles are closest to each other into equation 6.5 the open loop gain can be calculated:

$$A_{OL,LDO} = g_{m1}\, R_1\, g_{m2}\, R_2$$

$$= 10\,\mu\text{A} \cdot 100\,\text{M}\Omega \cdot 138.5\,\mu\text{S} \cdot 46.8\,\text{k}\Omega = 6482 \mathrel{\widehat{=}} 76.2\,\text{dB}. \tag{6.22}$$

Because the feedback loop is opened at the feedback node, the phase margin also has to be measured there. Therefore, the open loop gain is damped by the

V_{DD}	8 V		2.75 V	
I_L	0 mA	50 mA	0 mA	50 mA
g_{m2}	139.7 µS	346 mS	138.5 µS	87.46 mS
R_{out}	530 kΩ	53 Ω	46.8 kΩ	1.7 Ω
C_{GS}	22.82 pF	44.75 pF	32.12 pF	67.9 pF
$p1$	268 mHz	12 Hz	2.4 Hz	21.2 Hz
$p2$	63.9 Hz	7.4 kHz	58.1 Hz	71.7 kHz

Table 6.1: Simulation results for an one stage error amplifier.

voltage divider build of R_{f1} and R_{f2}. The open loop gain at the feedback node can be calculated to

$$A_{OL,fb} = A_{OL,LDO}\,\frac{R_{f2}}{R_{f1}+R_{f2}} = 6482\,\frac{240\,\mathrm{k\Omega}}{240\,\mathrm{k\Omega}+290\,\mathrm{k\Omega}} = 2935 \mathrel{\widehat{=}} 69.3\,\mathrm{dB} \tag{6.23}$$

To get a phase margin of more than 45° the second pole has to be located at a higher frequency than the gain-bandwidth-product. The gain-bandwidth-product lies at

$$GBW = A_{OL}\,p_1 = 2935 \cdot 2.4\,\mathrm{Hz} = 7.04\,\mathrm{kHz}. \tag{6.24}$$

Therefore, the second pole has to be located at an $m = 2935$ times higher frequency then the dominant pole. Now, with equation 6.15 the necessary capacitance C_{GD} to split the poles can be determined:

$$C_{GD} \approx 0.5\,\frac{\sqrt{4\,m\,C_L\,C_{GS}\,R_1\,R_2}}{g_{m2}\,R_1\,R_2} =$$

$$= 0.5\,\frac{\sqrt{4 \cdot 2935 \cdot 1.2\,\mathrm{\mu F} \cdot 32.12\,\mathrm{pF} \cdot 100\,\mathrm{M\Omega} \cdot 46.8\,\mathrm{k\Omega}}}{138.5\,\mathrm{\mu S} \cdot 100\,\mathrm{M\Omega} \cdot 46.8\,\mathrm{k\Omega}} = 1.12\,\mathrm{nF} \tag{6.25}$$

A capacitor of this size would be far to large to be produced on a chip. Therefore, this concept cannot be realized.

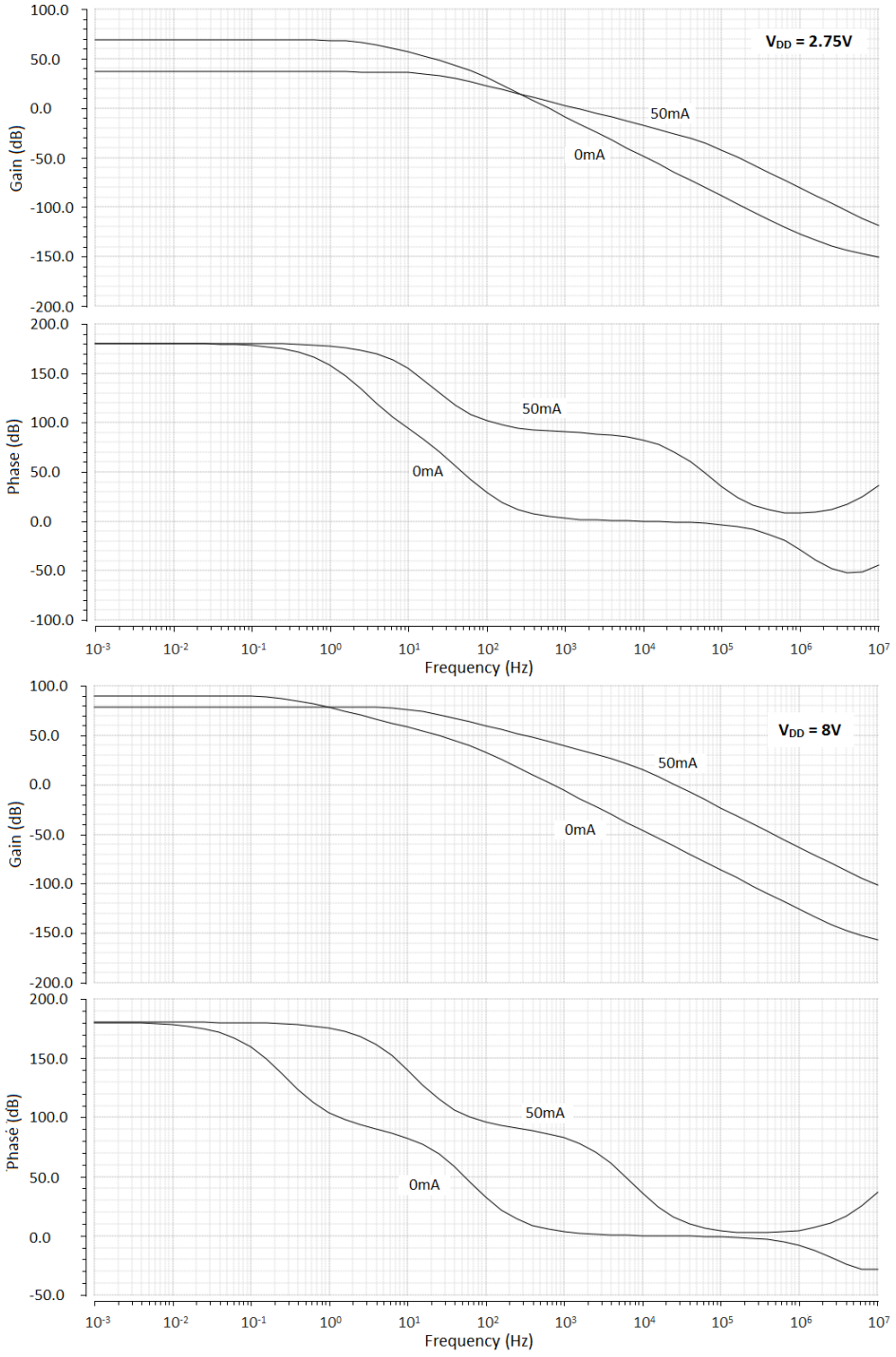

Figure 6.3: AC-response of an LDO with an one stage error amplifier for a supply voltage of 2.75 V (upper diagram) and 8 V (lower diagram). For low load currents the output pole is dominant and for high load currents the inner pole is dominant.

6.2 Error Amplifier with Reverse Nested Miller Compensation

For the reverse nested Miller compensation a three stage amplifier with an inverting second stage and a non-inverting third stage is needed [15]. The principle of the reverse nested Miller compensation is shown in figure 6.4. The capacitors C_{C1} and C_{C2} are connected from the outputs of the second and third stage to the output of the first stage and are performing the Miller compensation. The parameters g_{m1}, g_{m2} and g_{m3} are the transconductance of the first, second and third stage respectively. Also $R1$ and $C1$, $R2$ and $C2$ and $R3$ and $C3$ are the output resistances and capacitances of their particular stage.

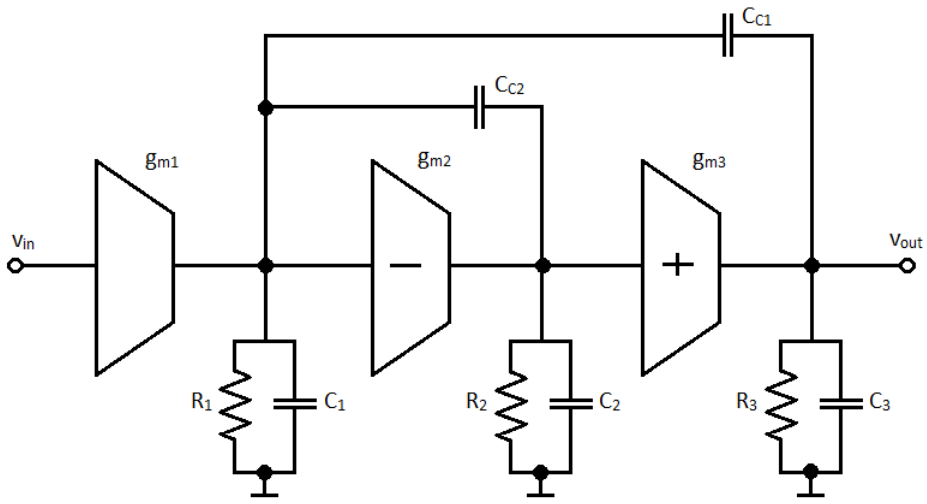

Figure 6.4: Reverse nested Miller compensation. A three stage amplifier where the compensation capacitors are connected between the outputs of the first stage and the second stage and between the first stage and the third stage. The second stage has to be inverting and the third stage non-inverting.

The advantage of the reverse nested Miller compensation is the ability to drive heavy capacitive loads and achieve a high bandwidth since the inner compensation capacitor is not loading the output node [16].

Referring to [15], the transfer function can be approximated to

$$T(s) = \frac{\mathrm{v}_{out}}{\mathrm{v}_{in}} = A_{OL} \frac{1 - \left(\frac{C_{C2}}{g_{m2}} + \frac{C_{C1}}{g_{m2}\, g_{m3}\, R_2}\right) s - \frac{C_{C1}\, C_{C2}}{g_{m2}\, g_{m3}}\, s^2}{\left(1 + \frac{s}{p_1}\right)\left[1 + \left(\frac{C_{C2}\, C_3}{g_{m3}\, C_{C1}} - \frac{C_{C2}}{g_{m2}} + \frac{C_{C2}}{g_{m3}}\right) s + \frac{C_{C2}\, C_3}{g_{m2}\, g_{m3}}\, s^2\right]}. \tag{6.26}$$

The open-loop gain is given by

$$A_{OL} = g_{m1}\, R_1\, g_{m2}\, R_2\, g_{m3}\, R_3 \tag{6.27}$$

and the dominant pole p_1 is determined by

$$p_1 = -\frac{1}{R_1\, C_{C1}\, g_{m2}\, R_2\, g_{m3}\, R_3}. \tag{6.28}$$

Therefore the gain-bandwidth product can be calculated to

$$GBW = A_{OL}\, p_1 = \frac{g_{m1}}{C_{C1}}. \tag{6.29}$$

The other two poles are usually building a conjugate-complex pole pair. Also two zeros can be found. The lower one on the right half plane and the higher one on the left half plane. The zero on the right half plane can be critical for stability. To avoid this right half plane zero, the feed forward path has to be eliminated. This can be done by adding a current or voltage buffer into the feedback path.

By adding one inverting and one non-inverting current buffer into the feedback paths, the feed-forward paths can be eliminated and the output stage does not have to be non-inverting. This is presented and analysed in [17]. The concept of this reverse nested Miller compensation with current buffers is shown in figure 6.5.

Figure 6.6 shows how the second and third stage can be implemented. The transistor M_1 builds a common source stage with current mirror load. M_2 mirrors the current with a ratio of 1:M to the pass device and therefore to the output. Increasing v_{in} leads to a higher current through M_2 and therefore through M_p and the output voltage goes up.

The inverting current buffer is realized by connecting the compensation capacitor to the input of a current mirror. This is illustrated in figure 6.7. A left half plane zero appears at

$$z_1 = -\frac{g_{mC1}}{C_{C1}}. \tag{6.30}$$

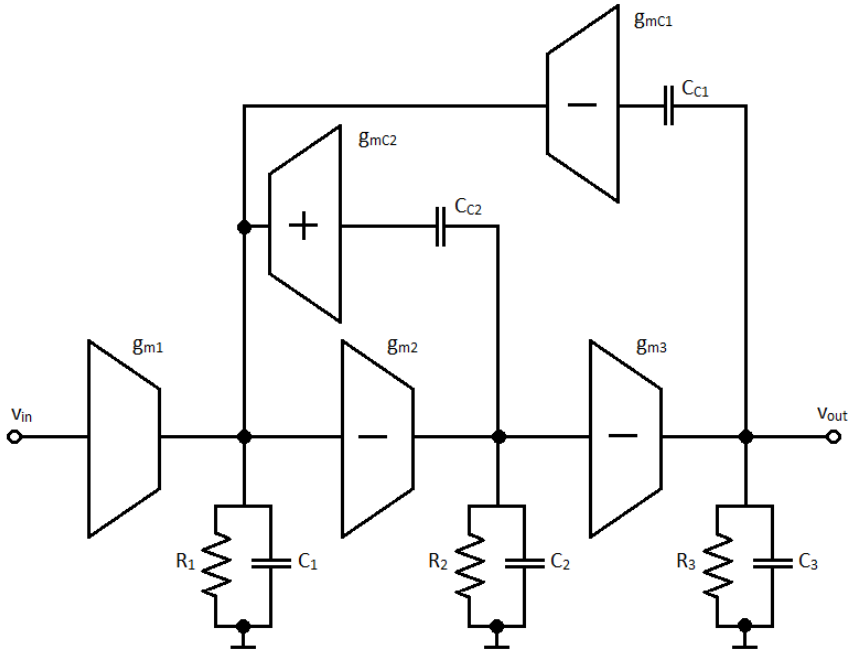

Figure 6.5: Concept of an LDO with reverse nested Miller compensation with current buffers. Current buffers are added to eliminate the feed forward paths.

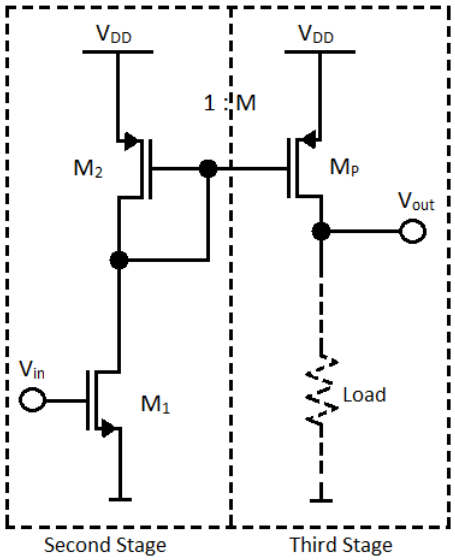

Figure 6.6: Implementation of the second and third stage. Increasing V_{in} increases the current through M_1. M_2 mirrors this current with a ratio of 1:M to the pass device M_p, therefore the output voltage increases too.

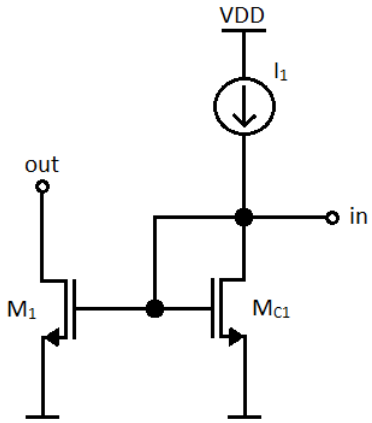

Figure 6.7: Concept of an inverting current buffer. The input is connected to the input of a current mirror.

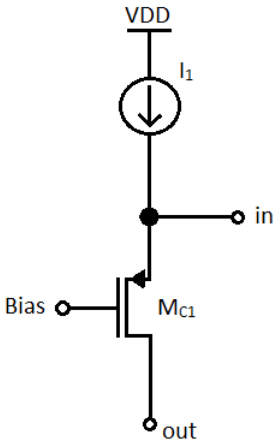

Figure 6.8: Concept of a non-inverting current buffer. The input is connected to the source pin of a transistor in common gate configuration.

For the non-inverting current buffer the compensation capacitor is connected to a transistor in common gate configuration. This is also known as cascode compensation. Figure 6.8 shows this concept. This introduces also a left half plain zero at

$$z_2 = -\frac{g_{mC2}}{C_{C2}}. \tag{6.31}$$

The transfer function of the reversed nested Miller compensated amplifier with current buffer can be approximated [17] to

$$T(s) = \frac{\mathrm{v}_{out}}{\mathrm{v}_{in}} \approx A_{OL} \frac{(1 + \frac{C_{C2}}{g_{mC2}}\, s)(1 + \frac{C_{C1}}{g_{mC1}}\, s)}{(1 + C_{C1}\, R_1\, g_{m2}\, R_2\, g_{m3}\, R_3\, s)(1 + \frac{C_{C2}\, C_3}{C_{C1}\, g_{m3}}\, s)(1 + \frac{C_{C1}}{g_{mC1}}\, s)}. \tag{6.32}$$

Due to the Miller effect the capacitance C_{C1} appears amplified with the gain of the second and third stage. Therefore the dominant pole can be found at the output of the first stage and lies at the same frequency as without the current buffers (equation 6.28). The open loop gain is given by

$$A_{OL} = R_1\, g_{m1}\, R_2\, g_{m2}\, R_3\, g_{m3}. \tag{6.33}$$

The gain bandwidth product can be calculated to

$$GBW = A_{OL}\, p_1 = \frac{g_{m1}}{C_{C1}}. \tag{6.34}$$

From the transfer function (equation 6.32) the second pole can be determined to

$$p_2 = -\frac{g_{m3}\, C_{C1}}{C_{C2}\, C_3}. \tag{6.35}$$

The third pole

$$p_3 = -\frac{g_{mC1}}{C_{C1}} \tag{6.36}$$

is compensated by the zero z_1. Thus, the transfer function has one zero and two poles. The phase margin can be approximated to

$$PM \approx 90^\circ - arctan\left(\frac{GBW}{p_2}\right) + arctan\left(\frac{GBW}{z_2}\right). \tag{6.37}$$

By adding a series resistor much larger than $1/g_{mC2}$ into the feedback path of C_{C2}, the zero can be moved down to a certain frequency

$$z_2 = -\frac{1}{R_{C2}\, C_{C2}}. \tag{6.38}$$

The proposed LDO with the error amplifier using reverse nested Miller compensation with current buffers is presented in figure 6.9. As input stage a folded cascode differential amplifier is used. This folded cascode amplifier consists of the input differential pair M_1 and M_2, the cascodes M_4/M_6 and M_5/M_7 and the current mirror M_8/M_9. The second stage is build by the transistor M_{11} in common source configuration and a diode connected load (M_{10}). The output stage is build by the pass-device M_{pass}, also in common source configuration.

R_{f1} and R_{f2} are the feedback resistors and are determining the closed loop gain of the LDO. The compensation capacitor C_{C1} is connected between the output and the input of the current mirror M_8/M_9. C_{C2} and R_{C2} are connected from the output of the second stage into the cascode M_5/M_7. The capacitor C_{C3} and the resistor R_{C3} between the outputs of the first and second stage are applied to create an additional zero. Together with C_{C2} and R_{C2} the zeros z_2 and z_3 will appear[17] at:

$$z_2 \approx -\frac{1}{R_{C2}\,C_{C2} + R_{C3}\,C_{C3}} \tag{6.39}$$

$$z_3 \approx -\left(\frac{1}{R_{C2}\,C_{C2}} + \frac{1}{R_{C3}\,C_{C3}}\right) \tag{6.40}$$

This is also influencing the second pole which can now be found at:

$$p_2 \approx -\frac{1}{R_{C2}\,C_{C2} + R_{C3}\,C_{C3} + \frac{C_{C2}}{g_{mC2}} + \frac{C_{C2}}{g_{mC1}\,g_{m3}\,R_3} + \frac{C_{C2}\,C_3}{C_{C1}\,g_{m3}}} \tag{6.41}$$

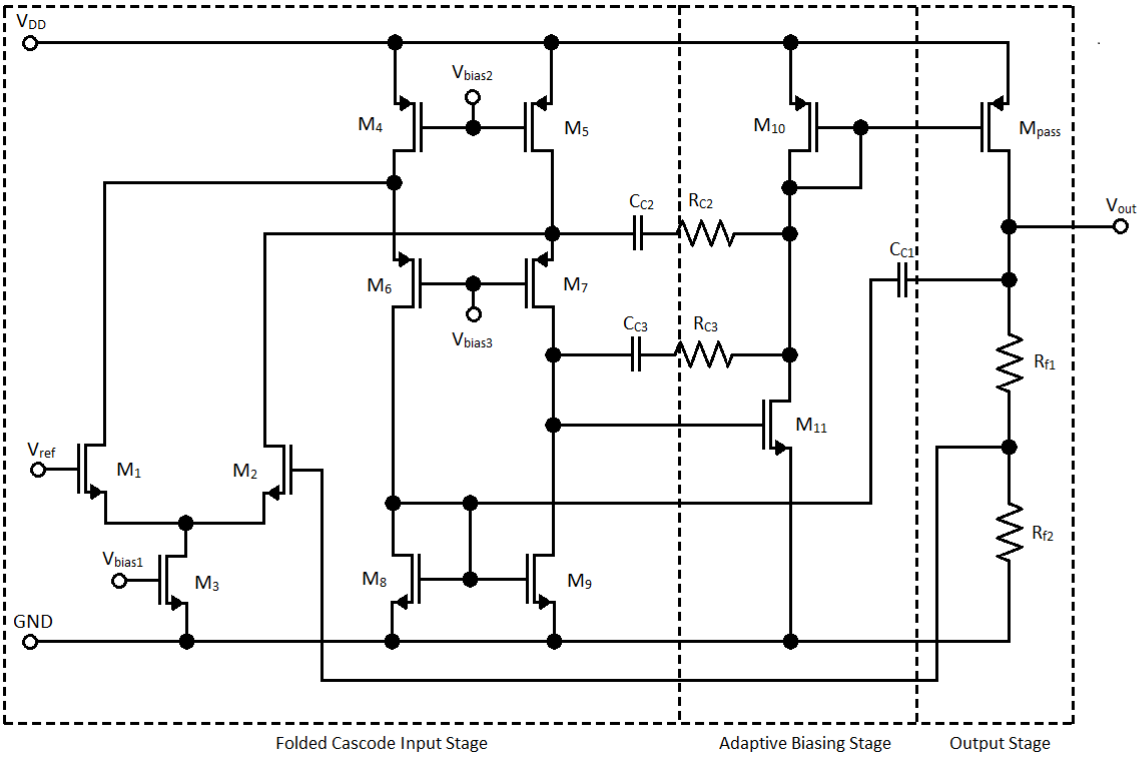

Figure 6.9: Schematic of the proposed error amplifier with reverse nested Miller compensation with current buffers. The input stage is a folded cascode OTA, the second stage is the adaptive biasing stage and the output stage consists of the pass device in common source configuration.

6.3 Discussion of the Presented Error Amplifiers

The concept of the single stage error amplifier with Miller compensation is the simplest approach for the LDO. Due to the large output capacitance of 1 µF and the gate capacitance of the pass device up to 70 pF, the compensation capacitor would have to be in the range of 1 nF in order to stabilize the LDO. A capacitor of this size is too large to be manufactured on-chip. Therefore this concept can not be realized.

The reverse nested Miller compensation has the ability to drive high load capacitances and achieve a high bandwidth because the output node is not loaded by the inner compensation capacitor. But this concept introduces a low frequency, right half plane zero which leads to a reduction of the phase margin and therefore introduces stability issues. By adding current buffers into the feedback paths, the right half plane zero changes to a left half plane zero. This can be used to compensate a pole and gain stability. This concept is called reversed nested Miller compensation with current buffers.

The ability to achieve a high bandwidth, even for a high load capacitance is the reason for choosing the concept of the reversed nested Miller compensation with current buffers for this project.

7 Design and Simulation of the LDO Regulator

7.1 Design

The reversed Miller compensation with current buffers, as discussed in the previous section, has the ability to achieve a high bandwidth even at heavy capacitive loads. Therefore this concept was implemented. The process used for this device is the H35 CMOS process from ams AG. Figure 7.1 illustrates the final schematic of the LDO. The pass device M_{pass} is a PMOS with mid gate oxide. This means, the pass device can withstand a higher voltage at its gate and also has a higher threshold voltage. In this application the higher threshold voltage is the reason for using the mid oxide transistor. This makes it possible to turn off the output current at 200 °C (see section 5.3).

Due to the current mirror driving the output stage, M_{10} has to be the same type of transistor as the pass device. Therefore M_{10} is also a PMOS transistor with mid gate oxide. In order to hold the current consumption of the LDO as small as possible the ratio of the current mirror M_{10} and M_{pass} has to be very large. This leads to the effect that for small output currents the transistor M_{10} reaches the sub-threshold region, where only several nano ampere are flowing. To make sure that M_{11} stays in a reasonable biasing condition the resistor R_1 was added.

To generate the bias voltages for the current mirrors a reference current is needed. This bias current was set to 1 µA and mirrored to M_{13}, M_{14} and M_3. M_{15} and M_{16} are generating the gate voltage for the cascode transistors M_{18}, M_6 and M_7. M_{17} mirrors the bias current to M_4 and M_5.

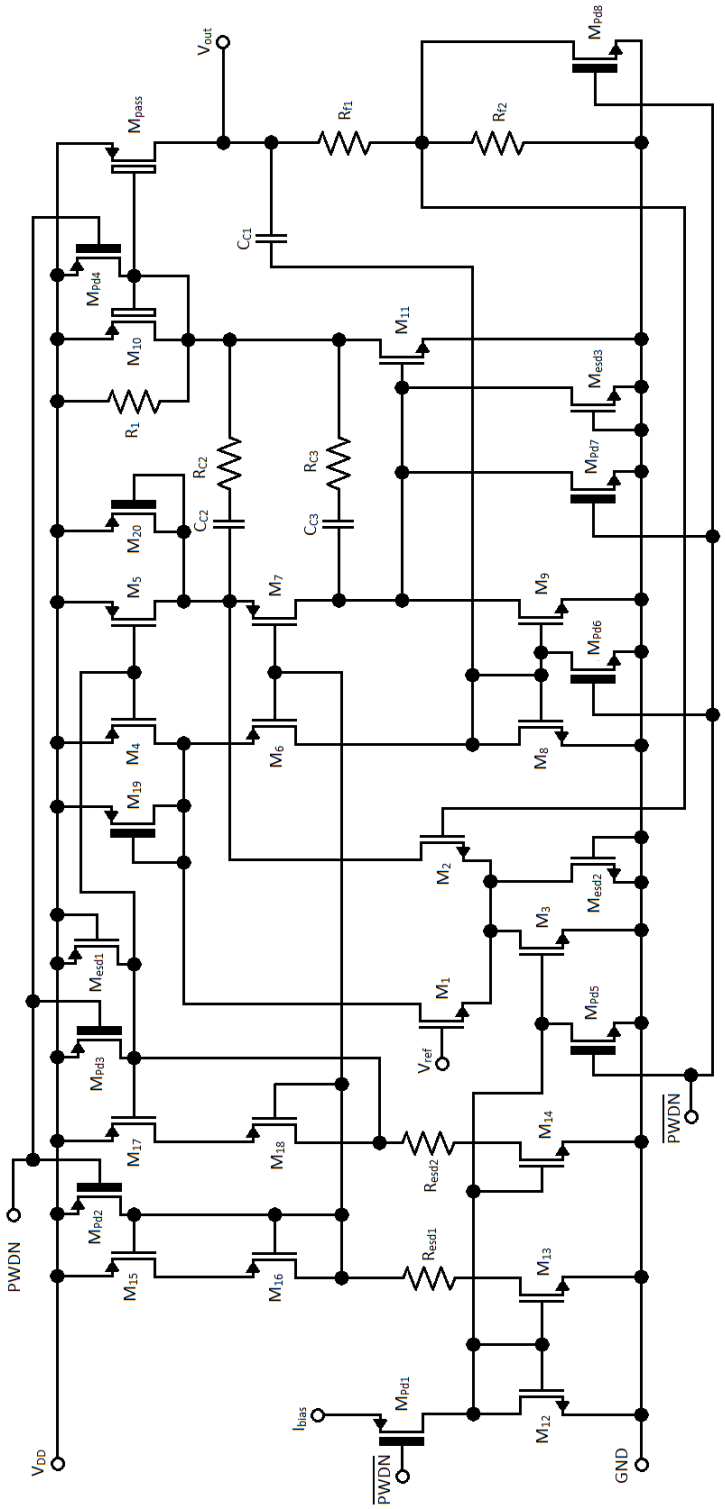

Figure 7.1: Final schematic of the LDO, including biasing blocks, power down mechanism and protection circuitry.

A power-down mechanism has been implemented with the transistors M_{pd1}, M_{pd2}, M_{pd3}, M_{pd4}, M_{pd5}, M_{pd6}, M_{pd7} and M_{pd8}. The power-down signal is an external signal with the values 0 V or V_{DD}, therefore it can reach a voltage up to 8 V. Since this voltage is applied at the gates of the power down transistors, the gate-source voltage can also reach 8 V. Thus, these transistors are designed as thick gate oxide transistors. The thin and mid oxide transistors would be destroyed by such a gate-source voltage. The power-down mode is implemented as active-low, which means, if the power-down signal has 0 V, the LDO is switched off. M_{pd1} cuts off the bias current of the LDO. If this would be a NMOS, its source voltage would be about the threshold voltage of M_{12}. Thus, in order to source current, the gate-voltage of M_{Pd1} has to be larger then the threshold voltage of M_{12} plus the threshold voltage of M_{Pd1}. At minimum supply voltage the sum of these two threshold voltages is higher than the supply voltage, hence, the transistor would not be able to turn on the bias current. This is the reason for using a PMOS at this place. M_{Pd2}, M_{Pd3} and M_{Pd4} are pulling the gates of the PMOS current mirrors up to the supply voltage. Thus, the gate-source voltages of the current mirror transistors are going to be zero and the current mirrors are turned off. The transistors M_{Pd5}, M_{Pd6} and M_{Pd7} are turning of the NMOS current mirrors by pulling the gate voltages down to the ground potential. M_{Pd8} is used to pull down the output. If it would be applied directly at the output it shorts the load capacitance and a high current would flow through the transistor which could destroy it. By connecting the drain between the feedback resistors, this current is limited through R_{f1}.

The $\overline{\text{PWDN}}$ signal is generated by an inverter consisting of two high voltage transistors with thick gate oxide. This is illustrated in figure 7.2.

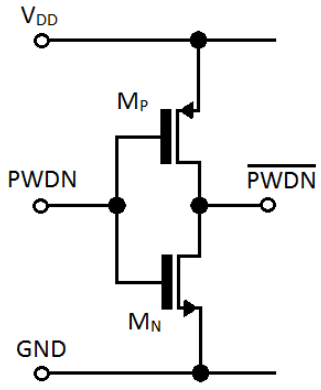

Figure 7.2: High voltage inverter to generate the $\overline{\text{PWDN}}$ signal

The transistors M_{esd1}, M_{esd2} and M_{esd3} are special ESD-MOSFETs to protect the circuit at critical points. M_{esd1} protects the gates of the PMOS current mirrors. M_{esd2} makes sure that the potential at the source pins of the differential input pair cannot reach the gate-source breakdown voltage. The gate of M_{11} is protected by M_{esd3}. The resistors R_{esd1} and R_{esd2} are protecting the gates of the current mirror transistors M_{15} to M_{18}. If the drain of M_{13} or M_{14} is being pulled down, the current through the resistor introduces a voltage drop. This voltage drop holds the gate voltages of the PMOS current mirror transistors at higher voltages.

The transistors M_4, M_5, M_{15} and M_{17} are low voltage transistors. In the layout they can be placed much closer to each other than the high voltage devices, therefore a better matching can be achieved.

If the supply voltage goes up without applying a bias current – this could be if the LDO is in power-down mode – than the transistors M_4 and M_5 are sourcing no current too. Therefore, the drains of M_4 and M_5 are not going to change their potential. Because M_4 and M_5 are low-voltage devices, the drain-source breakdown voltage will be reached for high input voltages. To avoid this, M_{19} and M_{20} are implemented. These are thick-oxide transistors in diode configuration. The threshold voltage is much higher than the voltage drop over M_4 and M_5 at normal operating condition. Thus, this transistors are sourcing no current and are not influencing the function of the circuit. But if the voltage drop would get higher than the threshold voltage of M_{19} and M_{20}, then they are limiting the maximum drain source voltage of M_4 and M_5.

The gain-bandwidth product should be as small as possible in order to hold the unity gain frequency lower than the non-dominant poles. Referring to equation 6.34 this means the compensation capacitor has to be large and g_{m1} has to be small.

7.2 Simulation

Figure 7.3 shows the testbench used to simulate the LDO. For the AC-analysis the feedback path is cut open and led out to the testbench through the two pins feedback out ("FBO") and feedback in ("FBI"). The switch S0 connects either the "FBO" pin directly to the "FBI" pin (DC-analysis) or the AC-source to the "FBI" pin (AC-analysis). The signal "Select" is for setting the output

voltage to 2.65 V or 2.95 V. "VDD" is the supply voltage, "Vref" the reference voltage and the bias current for the LDO is applied through the "bias" pin.

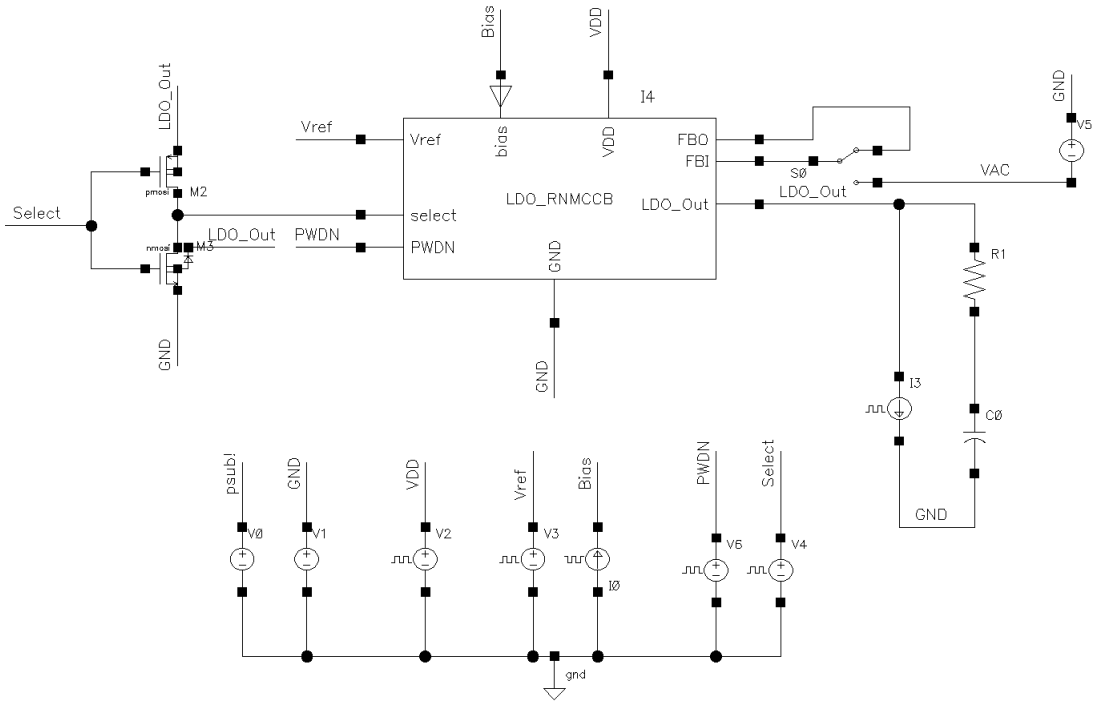

Figure 7.3: Schematic of the testbench for the simulation of the LDO. With the "select" pin the output voltage can be chosen (2.65 V or 2.95 V), "Vref" and "Bias" are the 1.2 V reference voltage and the 1 µA bias current respectively and "VDD" is the supply voltage for the LDO. With the pins "FBO" and "FBI" the feedback loop can be opened and the AC-source can be added through the switch "S0". With the "PWDN" pin the LDO can be set into the power-down mode. C_0 and R_1 are modelling the external output capacitor and its ESR respectively. I_3 is a current source to sink the load current.

7.2.1 DC Analysis

The results of the DC-analysis for the typical mean point of the process corners at room temperature (27 °C) are shown in table 7.1. The output voltage was set to 2.65 V through the "Select" signal, the load current (I_{Load}) was set to 50 mA and 250 µA and the supply voltage (V_{DD}) was set to minimum (2.75 V) and maximum (8 V) voltage. V_{LDO_Out} is the output voltage of the regulator

and I_{LDO} is the current amount of the LDO itself. Due to the adaptive gain stage the current amount increases with higher load currents. In standby I_{LDO} goes down to about 45 µA.

V_{DD}	2.75 V		8 V	
I_{Load}	250 µA	50 mA	250 µA	50 mA
V_{LDO_Out}	2.634 V	2.634 V	2.634 V	2.634 V
I_{LDO}	45.4 µA	309.5 µA	44.9 µA	117.4 µA

Table 7.1: DC-simulation results for 2.65 V output voltage.

Table 7.2 shows the results for the same simulation, but with the 2.95 V output voltage selected. The minimum supply voltage was set to 3.05 V in order to have 100 mV more than the output voltage.

V_{DD}	3.05 V		8 V	
I_{Load}	250 µA	50 mA	250 µA	50 mA
V_{LDO_Out}	2.94 V	2.94 V	2.94 V	2.94 V
I_{LDO}	50.7 µA	337.6 µA	50.2 µA	123 µA

Table 7.2: DC-simulation results for 2.95 V output voltage.

For the corner simulation the worst case (WC) models for the transistors, the resistors and the capacitors were used. Furthermore, the minimum and maximum values of the temperature, the load capacitance, the load current and the supply voltage were taken account for this simulation. Table 7.3 presents the used worst case parameters.

Transistor	Resistor	Capacitor	C_L	I_{Load}	V_{DD}	Temperature
WC Speed	WC Speed	WC Speed	500 nF	250 µA	2.75 V	−40 °C
WC Power	WC Power	WC Power	1.2 µF	50 mA	8 V	200 °C
WC One	-	-	-	-	-	-
WC Zero	-	-	-	-	-	-

Table 7.3: Input parameters for the corner simulation.

The minimum and maximum outputs of the corner simulation for 2.65 V output voltage is shown in table 7.4. The variation of the output voltage is 13 mV and the current amount can raise up to 751.2 µA at full load condition.

	Minimum	Maximum
V_{LDO_Out}	2.629 V	2.642 V
I_{LDO}	36.1 µA	751.2 µA

Table 7.4: Corner simulation results.

7.2.2 AC Analysis

The typical mean simulation was done with the typical mean models of the transistors, the resistors and the capacitors. The load capacitance was set to 1 µF and the Equivalent Series Resistor (ESR) of the load capacitor (R_1 in figure 7.3) was set to 10 mΩ. Figure 7.4 shows the frequency response of the LDO with 2.65 V output voltage. In the upper diagram the supply voltage was set to 2.75 V and for the lower diagram it was set to 8 V. For both supply voltages the simulation was done with 50 mA and 250 µA load current.

With higher input voltages the output resistance, dominated by the drain source resistance of the pass device, increases. Thus, referring to equation 6.33 the open loop gain also has to increase. The dominant pole, given by equation 6.28, is pulled to lower frequencies due to the higher output resistance. The zero z_2 (equation 6.39) was designed to cancel the second pole p_2 (equation 6.41). The zero z_3 (equation 6.40) was placed to cancel one of two high frequency poles which would generate a conjugate complex pole pair and cause instability.

Increasing the load current leads to a higher transconductance and a lower drain-source resistance of the pass device, thus the dominant pole moves to higher frequencies and the gain gets decreased. This effect is much stronger at low supply voltages because the low voltage drop between input and output causes the pass device to go near the linear region. Therefore, the drain-source resistance decreases stronger, which reduces the gain even more and pushes the dominant pole up to higher frequencies. The second pole frequency (equation 6.41) is also affected by increasing the load current, because it is also proportional to the transconductance of the pass device and therefore is pushed to higher frequencies.

Table 7.5 shows the phase margin and gain margin for these operating conditions. By increasing the load current the poles are pushed to higher frequencies, but the gain bandwidth product, given by equation 6.34, stays nearly constant. Therefore, the phase margin increases. Figure 7.5 presents the dependency of the phase margin on the load current.

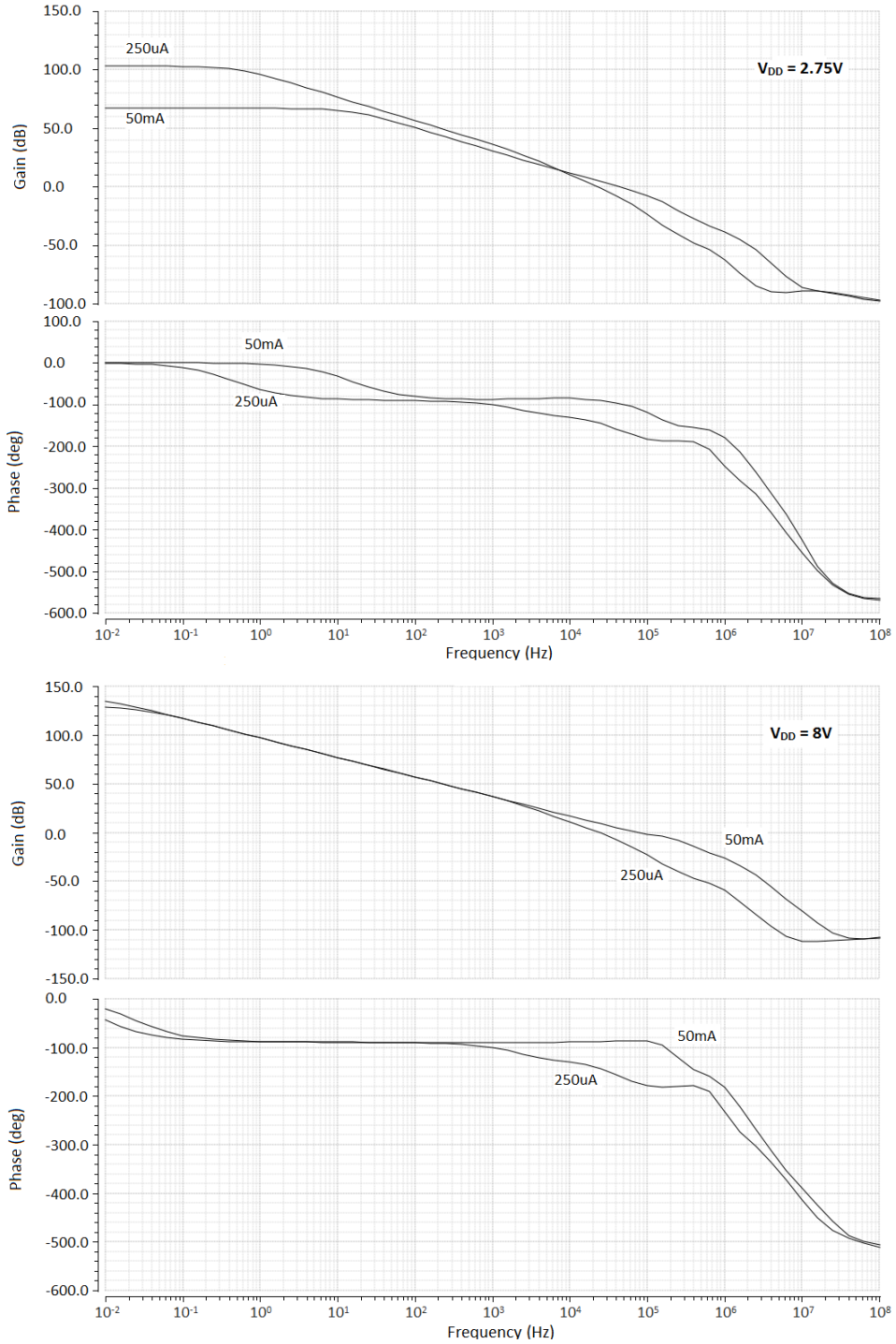

Figure 7.4: AC-response of the LDO for 2.75 V and 8 V supply voltage with 250 µA and 50 mA load current at 2.65 V output voltage. The dominant pole frequency increases and the open loop gain decreases with the load current.

V_{DD}	2.75 V		8 V	
I_{Load}	250 µA	50 mA	250 µA	50 mA
Phase Margin	36.6°	82.2°	37.3°	92.9°
Gain Margin	20.8 dB	38.9 dB	23.5 dB	25.8 dB

Table 7.5: Typical mean phase margin and gain margin for 2.65 V output voltage.

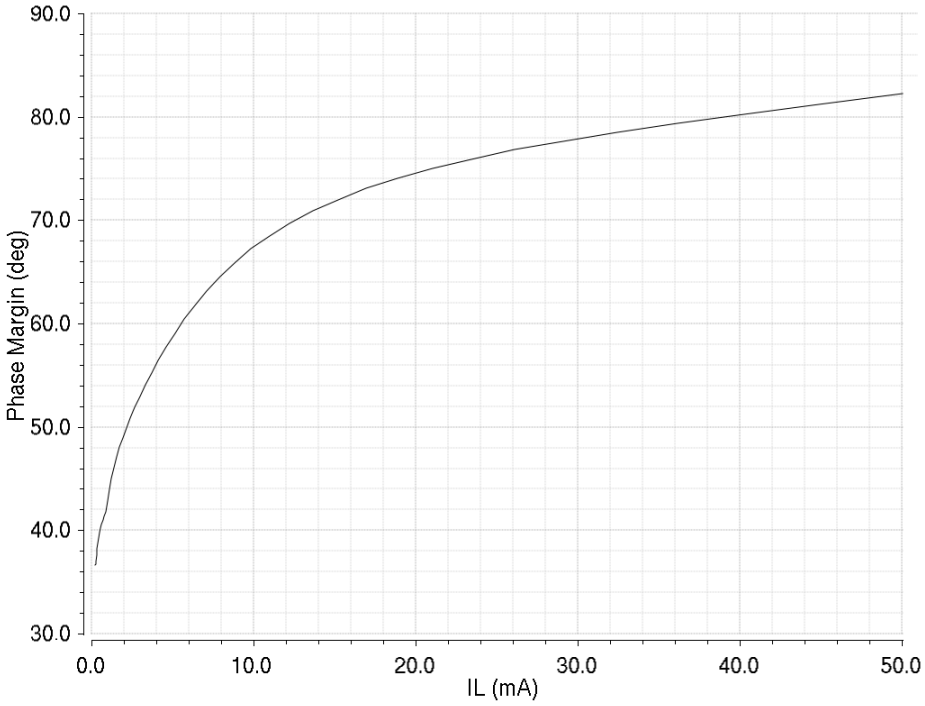

Figure 7.5: Phase margin depending on the load current. The phase margin increases with increasing the load current, beginning at about 36° up to 82°.

The frequency response of the 2.95 V output voltage for the typical mean simulation is illustrated in figure 7.6. As expected, it does not look much different to the 2.65 V output, because the only thing changed is the ratio of the feedback resistors in order to get a higher closed loop gain. The phase margin and gain margin are presented in table 7.6.

Again, the corner analysis was done with the parameters listed in table 7.3. The maximum and minimum values of the phase margin and gain margin over all corners are illustrated in table 7.7.

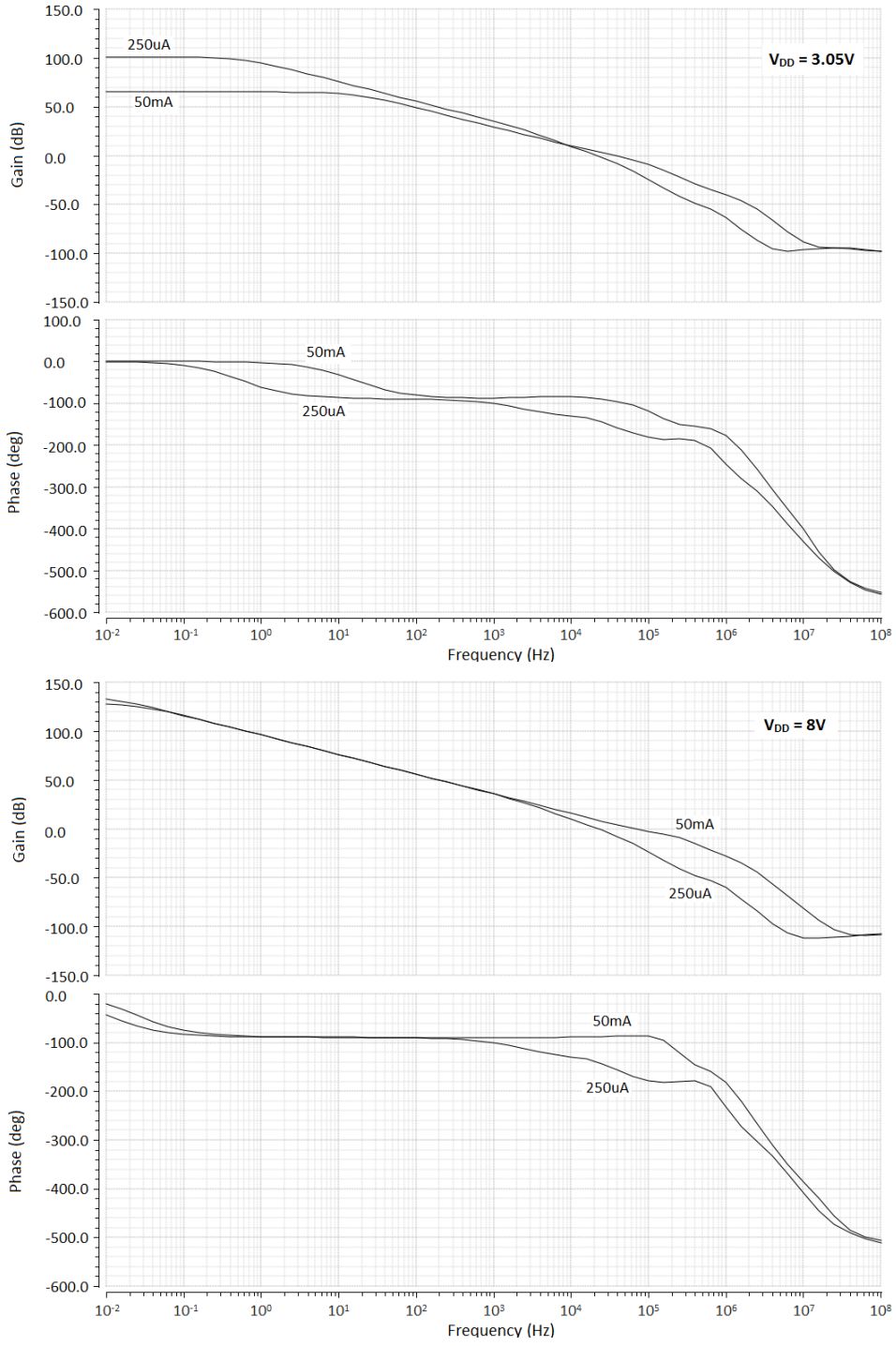

Figure 7.6: AC-response of the LDO for 3.05 V and 8 V supply voltage with 250 µA and 50 mA load current at 2.95 V output voltage. The frequency behaviour with 2.95 V output voltage is nearly the same as with the 2.65 V output voltage.

V_{DD}	3.05 V		8 V	
I_{Load}	250 µA	50 mA	250 µA	50 mA
Phase Margin	38.6°	84.4°	39.2°	93.2°
Gain Margin	21.8 dB	40.7 dB	24.6 dB	27.0 dB

Table 7.6: Typical mean phase margin and gain margin for 2.95 V output voltage.

V_{Out}	2.65 V		2.95 V	
	Minimum	Maximum	Minimum	Maximum
Phase Margin	29.2°	104.6°	29.9°	103.1°
Gain Margin	9.8 dB	56.6 dB	10.9 dB	58.1 dB

Table 7.7: Minimum and maximum results for the phase margin and gain margin of the corner analysis.

For the power supply rejection (PSR) simulation the control loop was closed and the AC source applied to V_{DD}. The output was measured in decibel by applying a 1 V AC signal. The results for the 2.65 V output under different load and supply voltage conditions are presented in figure 7.7. Due to equation 5.3 the line regulation and therefore also the PSR is mainly dependent on the open loop gain A. As mentioned before, the open loop gain decreases with increasing the load current, thus the PSR gets worse. At the 8 V supply voltage the PSR is higher and less depending on the load current compared to the 3.05 V.

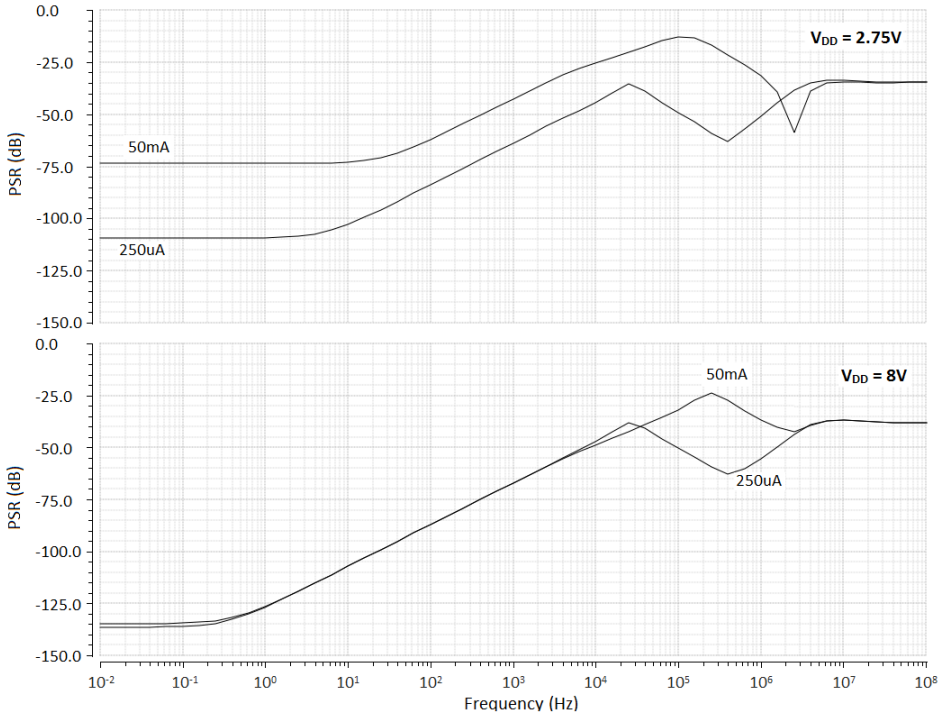

Figure 7.7: Power supply rejection of the LDO at 2.65 V output voltage. The PSR is higher with 8 V supply voltage than with 2.75 V supply voltage. At 2.75 V supply voltage the pass device reaches the linear region and the PSR decreases.

7.2.3 Transient Analysis

For the transient analysis a load step was applied from 250 µA to 50 mA with a rise time of 10 µs. The response of the output with the 2.65 V output voltage selected and 2.75 V supply voltage is shown in figure 7.8.

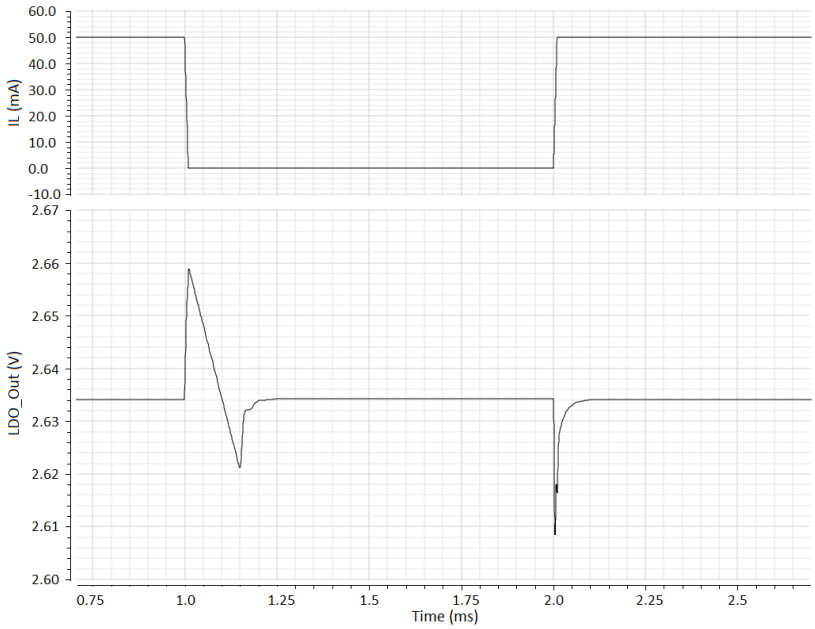

Figure 7.8: Transient response to a load step at typical mean condition with 2.65 V output voltage. The over- and undershoots are smaller than 30 mV.

To get the worst case of the over- and undershoots a corner analysis was done. The over- and undershoots are highest if the supply voltage is at its minimum. For the worst case overshoot the highest possible reference voltage V_{ref} with 1.224 V was applied. Due to the maximum allowed output voltage of 2.8 V the supply voltage needs to be higher than 2.8 V. Therefore it was set to 2.83 V to see if the output voltage gets higher than the allowed voltage. For the worst case undershoot, the smallest supply voltage of 2.75 V and the smallest reference voltage was applied. The result of this two cases is illustrated in figure 7.9. The minimum allowed voltage of 2.5 V and the maximum allowed voltage of 2.8 V have not been crossed.

Figures 7.10 and 7.11 are showing the step response under typical mean condition and the worst case over- and undershoot for the 2.95 V output voltage. Here too, the specified tolerance of ±150 mV has been achieved.

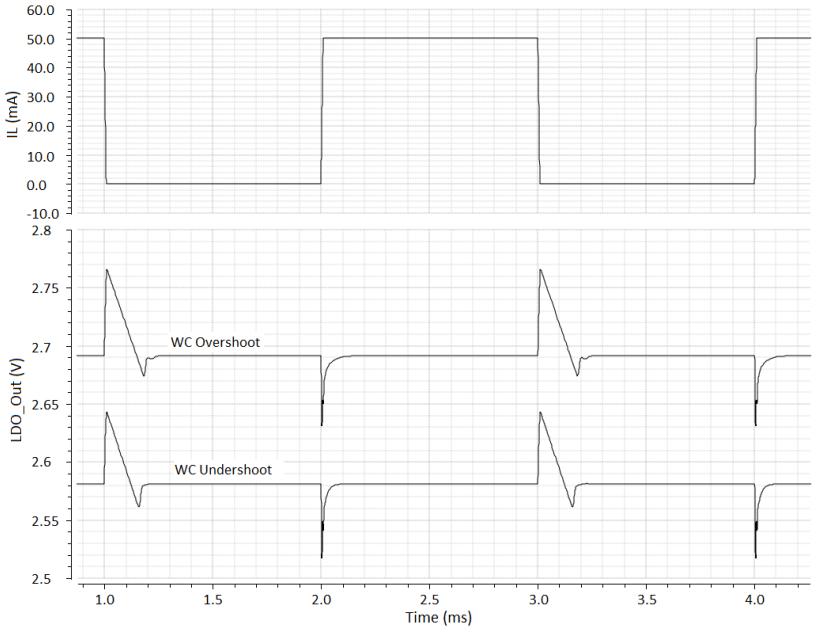

Figure 7.9: Worst case over- and undershoot by applying a load step from 250 µA to 50 mA in 10 µs at 2.65 V output voltage. The highest and the lowest peak are in the range of the ±150 mV.

The transient response to a 1 V step in the supply voltage is presented in figure 7.12. The rise and fall time for the line step was set to 10 µs. With decreasing the supply voltage to the minimum of 3.05 V at the 2.95 V output, the pass device enters the linear region and the LDO will not be able to suppress the peak as good as with higher supply voltages.

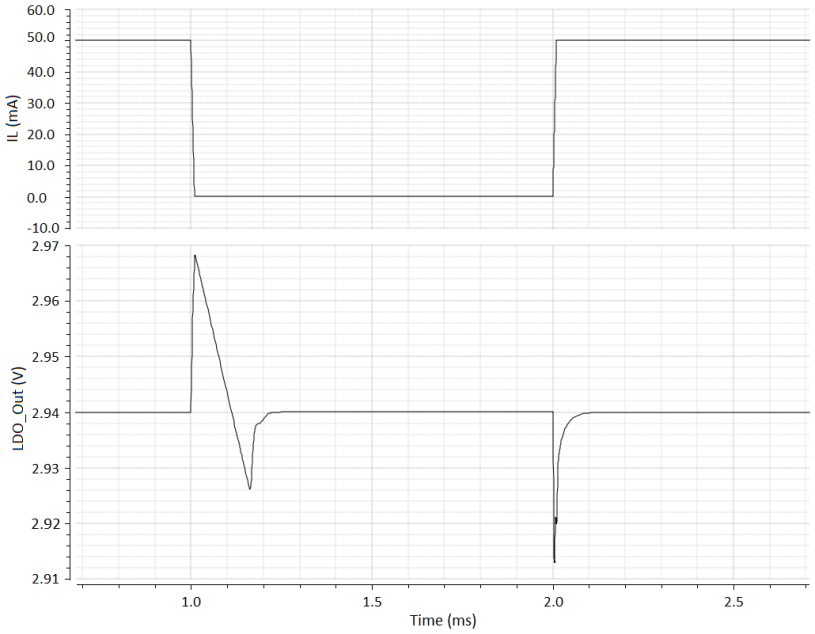

Figure 7.10: Transient response to a load step from 250 µA to 50 mA in 10 µs at typical mean condition with 2.95 V output voltage. The over- and undershoots are smaller than 30 mV.

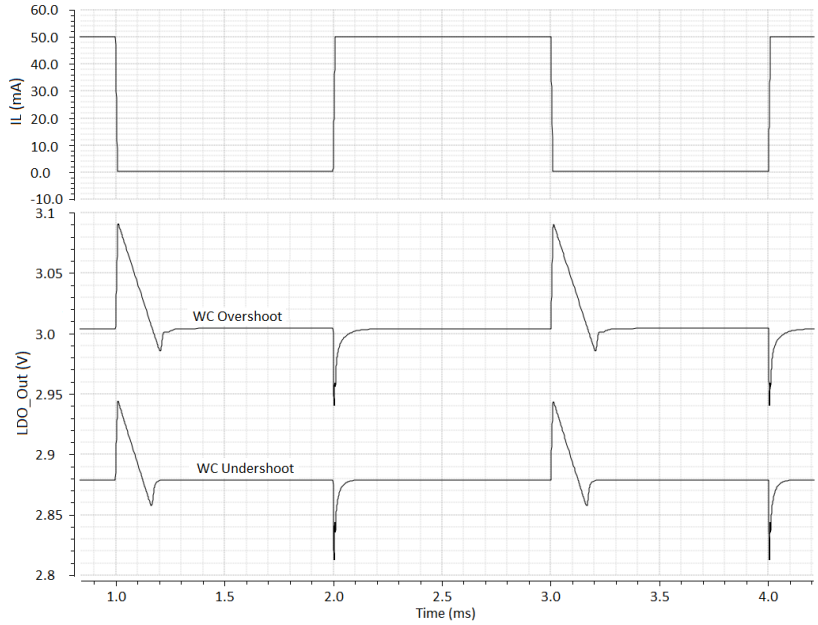

Figure 7.11: Worst case over- and undershoot by applying a load step at 2.95 V output voltage. The peaks of the over- and undershoots are not crossing the ±150 mV.

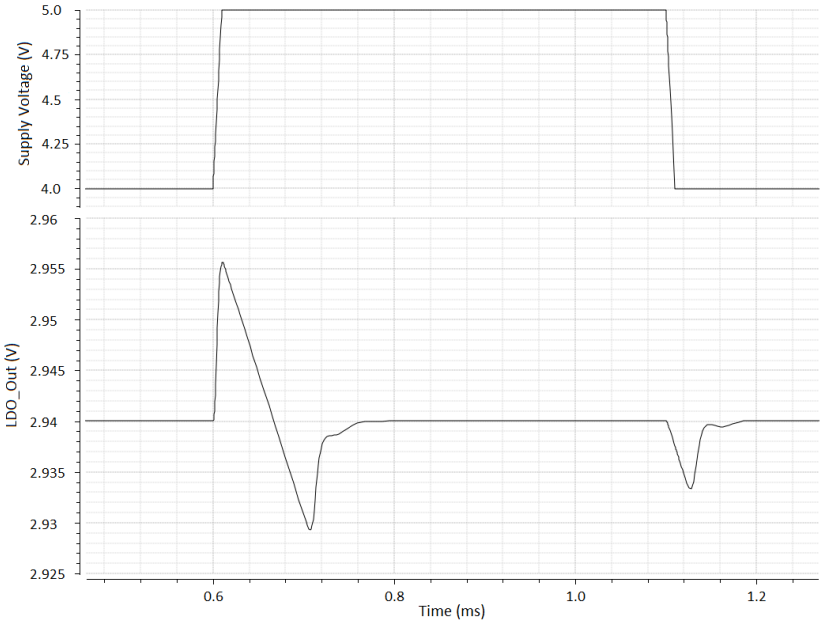

Figure 7.12: Transient response to a 1 V step in the supply voltage with 2.95 V output voltage. The over- and undershoots are in the range of 15 mV.

7.2.4 Discussion of the Simulation Results

The DC-simulation shows that the output voltage in the typical mean simulation stays constant over the whole load current and supply voltage range. Therefore, the load- and line regulation is negligible small. The quiescent current at 250 µA load current lies at about 50 µA. This is the half of the specified maximum quiescent current. At 50 mA load current the current consumption of the LDO increases to about 340 µA. This high current consumption at high loads is caused by the adaptive biasing stage, especially at minimum supply voltage, because the pass device reaches the linear region. The worst case simulation gives a variation of the output of 13 mV, which is in the range of the targeted 20 mV (see section 4). The current consumption can raise up to about 750 µA. This is much higher than the targeted 100 µA and could be a task for the future to get reduced.

The AC-simulation results for the typical mean simulation gives a phase margin of about 37° for minimum load current and increases with the load current up to about 90°. This is much lower then expected from [17], where phase margins were achieved of over 100° over the whole range of the output current. In the worst case simulation, the phase margin decreases to about 29°.

The transient analysis gives for a load transient at minimum supply voltage from minimum to maximum load current in 10 µs over- and undershoots in the range of 30 mV. Together with the deviation of the bandgap, the over- and undershoots are not reaching the ±150 mV.

The designed LDO meets the specification, but the phase margin and the current consumption are leaving place for improvement.

8 Testchip

In order to evaluate the behaviour of the regulator, a test chip was manufactured. On the test chip additionally an already existing bandgap reference and current reference were implemented. These two blocks were used to generate the 1.2 V reference voltage and the 1 µA bias current for the LDO. With an input pin ("ext_en") it can be chosen if this internal reference and bias or an externally applied reference voltage ("Vref_ext" pin) and current ("bias_ext" pin) source are used. To be able to measure the internal bandgap reference and current reference they have to be connected to output pins ("Vref_out" and "Ibias_out"). With an input pin ("ref_out_en") these references can be switched to their output pins. The bandgap reference has six trim bits (v_trim0 to v_trim5) and the current reference has five trim bits ("i_trim0" to "i_trim4") in order to set the desired output values. Also a power-down pin ("pd_vref_bias") for the two blocks was implemented. The LDO and the reference circuits have different supply pins because the reference circuits are built with low voltage devices which cannot withstand the maximum supply voltage of 8 V. With the "select" input pin the output voltage (2.65 V or 2.95 V) can be chosen. To shut the LDO down, the "PWDN" pin is used. "LDO_Out" is the output pin of the LDO regulator, "VDD" is the supply voltage for the LDO (up to 8 V) and "vdda" is the supply voltage for the bandgap reference and the current reference (3 V).

8.1 ESD Concept

In order to avoid the destruction of the test chip due to an electrostatic discharge (ESD), an ESD protection circuitry has to be applied. The concept of this circuitry is presented in figure 8.1. The test-chip is split in three voltage domains: The "vdda" domain, the "VDD" domain and the "LDO_Out" domain. Every domain has two current paths, one for the primary protection, where the main part of the ESD current is flowing and one for the secondary protection.

Every signal pad has diodes to protect the gates of the transistors from voltages higher than the supply voltage and lower than the ground potential. To protect

the supply voltage against to high voltages in case of an ESD impulse a clamping diode is applied. The digital inputs have an additional Schmitt trigger stage in order to get clear defined states.

In the "vdda" domain two analogue pads, for the bandgap reference and the current reference output and thirteen digital pads, for the trim bits, the power down signal and the clock signal are applied. In the "LDO_Out" domain two analogue input pads for the external references and two digital input pads for the "select" signal and the "ext_en" signal are applied. The "VDD" domain consists of a 15 V clamp and the "PWDN" pad.

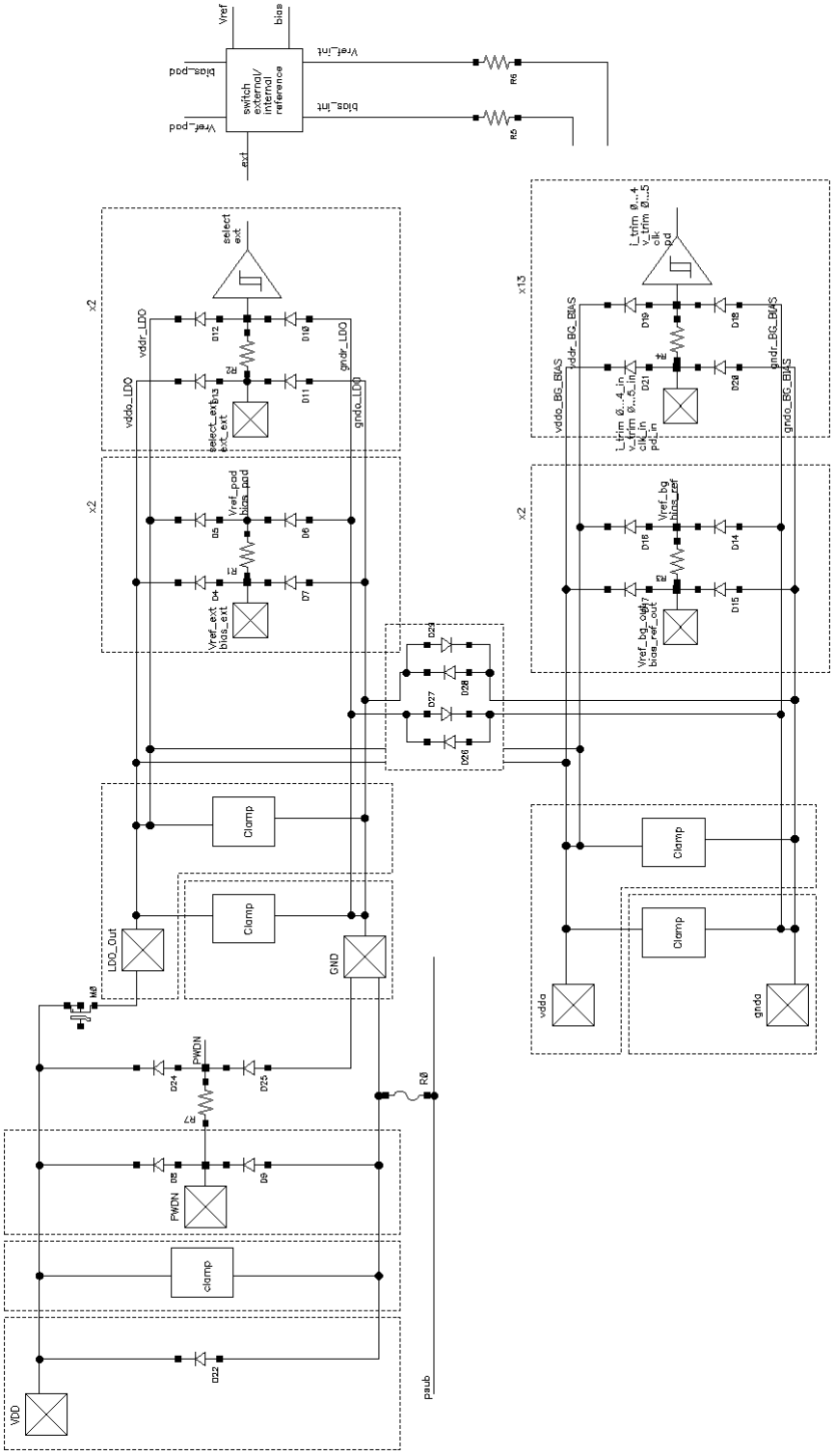

Figure 8.1: ESD concept for the testchip. Three different voltage domains are used.

9 Evaluation

Figure 9.1 shows the layout of the LDO. The main part of the silicon area is used by the pass device and the compensation capacitors. In order to hold the parasitic resistance at the output as small as possible, the drain of the pass device is connected with as much vias as possible to the metal layer.

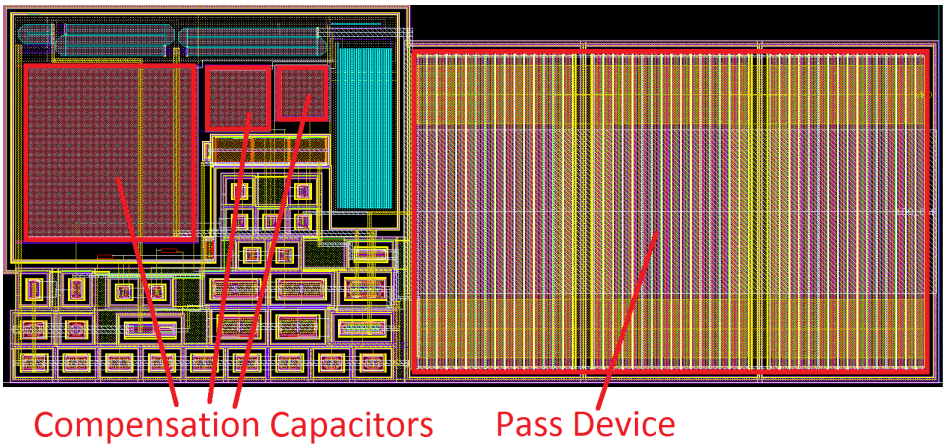

Figure 9.1: Layout of the LDO. The area of the pass device is as large as the rest of the circuitry

The testchip was directly bonded to a printed circuit board (PCB) and measured under a thermostream. The measurement setup is shown in figure 9.2. The supply voltage for the LDO is generated by an Agilent E3631A and the reference voltage and the bias current are applied by a Keithley 2602B source meter. The switches for the "Select" and the "ext_en" signals are supplied with 2.5 V in order to have always a lower voltage than the output. Would the voltage on this input pins get higher than the output voltage, then a current would flow through the ESD diodes to the output. Due to the voltage drop over the ampere meter, the supply voltage is measured after the ampere meter.

First, the leakage current of the LDO was measured. The LDO was set to the power-down mode and the supply voltage was set to 8 V. Beginning at 100 °C

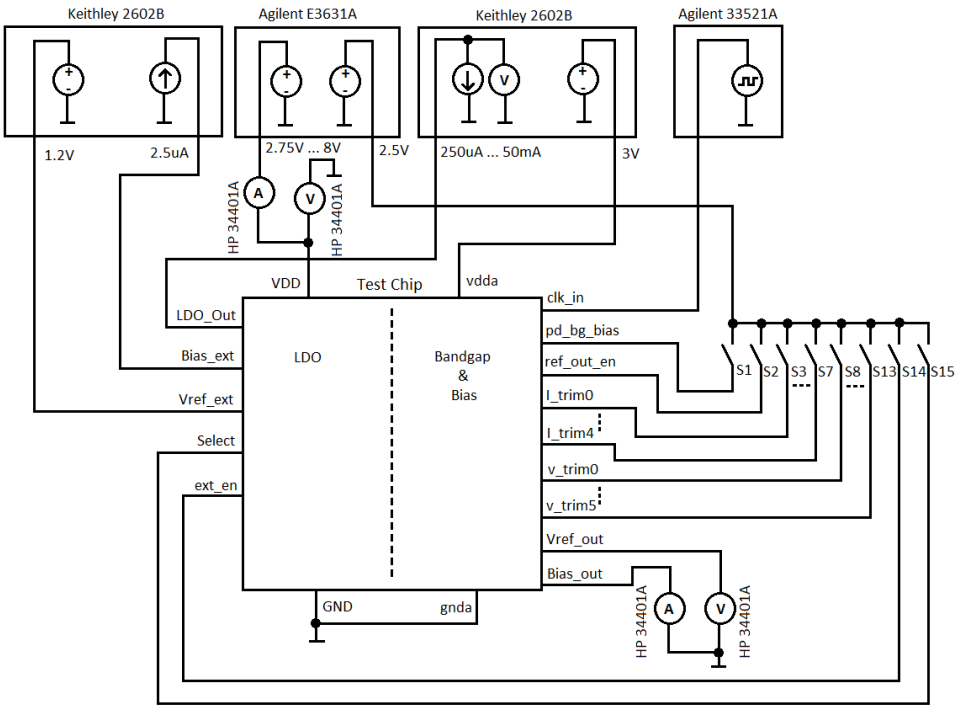

Figure 9.2: Measurement setup for the LDO. The supply current is measured with an ampere meter. The supply voltage is measured after the ampere meter due to the voltage drop over the ampere meter. The digital pins are supplied with 2.5 V and can be turned off and on with the switches S1 to S15. The reference voltage and bias current are applied through a Keithley 2602B source meter.

the temperature was increased in 10 °C steps up to 220 °C. The results of this measurement is presented in figure 9.3. The leakage current grows exponential with the temperature. The main part of the leakage current is introduced by the diode from the VDD pad to ground.

The LDO was designed for a bias current of 1 µA. By applying this bias current the output voltage breaks down and the LDO gets unstable at 200 °C and high load currents. Increasing the bias current leads to higher stability in this operating point and the LDO works properly again. The reason for this behaviour could be the increasing leakage currents and the additional heating of the pass device through the high load currents. Therefore, all following measurements were done with a bias current of 2.5 µA. Using this higher bias current decreases the phase margin at lower temperatures and increases the maximum deviation of the output voltage.

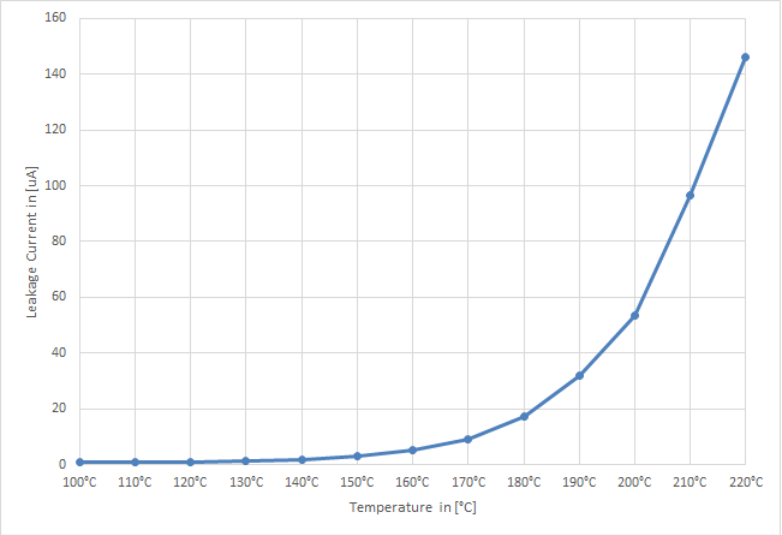

Figure 9.3: Measurement of the leakage current at 8 V supply voltage in power down mode. The leakage current increases exponential with the temperature. At 200 °C the leakage current is about 55 µA.

Now, a supply voltage sweep over the whole temperature region was done, where the supply voltage was increased from 3.05 V to 8 V. From 3.05 V to 3.2 V the step size was set to 50 mV and beginning with 3.5 V to 8 V the step size was set to 0.5 V. The supply voltage sweep was done over the whole temperature region of −40 °C to 200 °C in 20 °C steps. This measurement was done for a load current of 250 µA (figure 9.4) and for a load current of 50 mA (figure 9.5). At low output currents the output voltage stays nearly constant over the whole region of the supply voltage. For high load currents and small supply voltages the output voltage breaks down, especially at high temperatures.

To determine the quiescent current, the load current was subtracted from the measured supply current. The dependency of the quiescent current on the supply voltage is presented in figure 9.6 for the minimum load current of 250 µA and in figure 9.7 for the maximum load current of 50 mA. At low input voltages the current consumption of the LDO increases due to the adaptive biasing and the low difference between the supply voltage and the output voltage. Under low load current condition the quiescent current increases with the temperature. The main part of this effect is caused by the leakage current of the diode at the VDD pad.

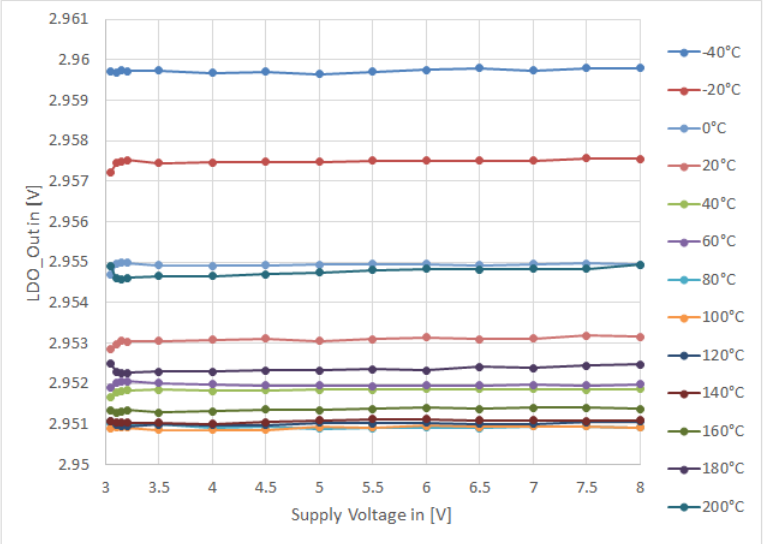

Figure 9.4: Measurement results of supply voltage sweeps under different temperatures for a load current of 250 µA. The output voltage stays constant over the whole supply voltage region and increases about 9 mV over the temperature region.

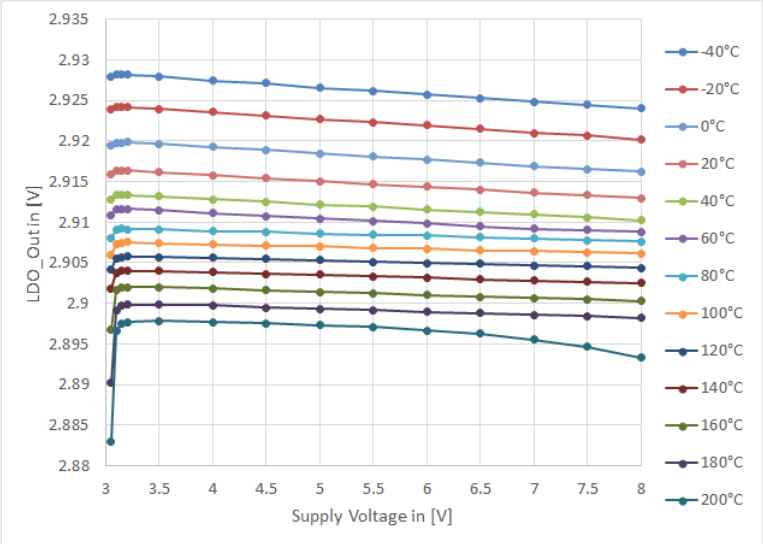

Figure 9.5: Measurement results of supply voltage sweeps under different temperatures for a load current of 50 mA. For the minimum supply voltage the output voltage gets decreased at high temperatures. For higher supply voltages the temperature dependency lies at about 30 mV over the whole temperature region.

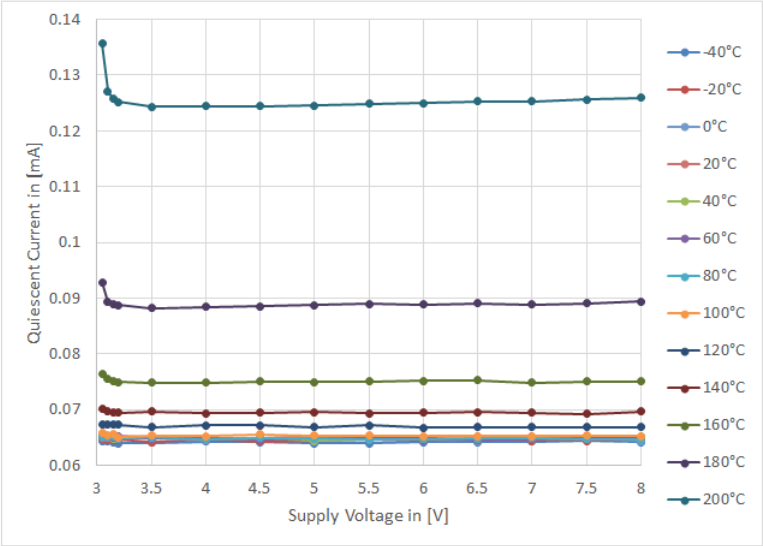

Figure 9.6: Dependency of the quiescent current on the supply voltage for a load current of 250 µA. The quiescent current stays nearly constant over the whole supply voltage region and increases with the temperature.

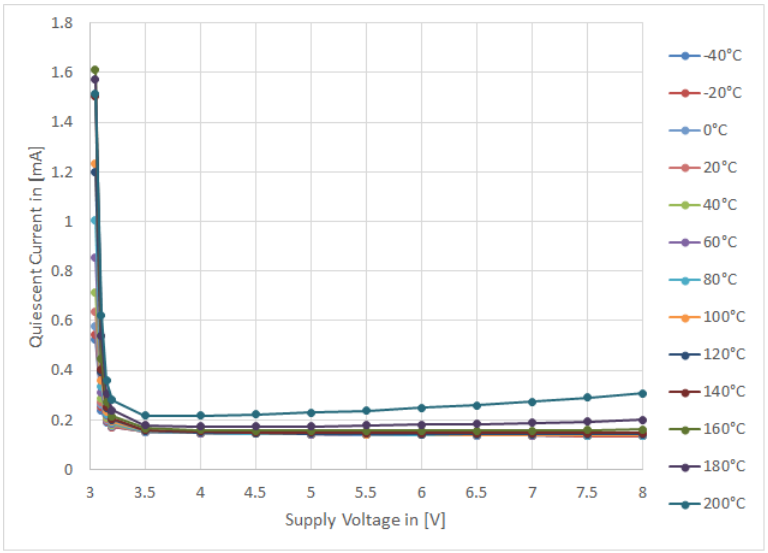

Figure 9.7: Dependency of the quiescent current on the supply voltage for a load current of 50 mA. For the minimum supply voltage the current consumption of the LDO increases to 1.6 mA. At higher supply voltages the current consumption stays at about 150 µA.

Also a load current sweep was done over the whole temperature region. The load current was increased from 250 µA to 50 mA. Here too, the step size at the beginning was chosen smaller (250 µA) until a current of 1 mA. Starting with 2 mA to 50 mA the load current was increased in 4 mA steps. Again, this was done over the whole temperature region with 20 °C steps. Figures 9.8 and 9.9 are presenting the results of this measurement for a supply voltage of 3.05 V and a supply voltage of 8 V respectively. The output voltage is approximately linear decreasing with the increasing load current. This behaviour could be introduced by the resistance of the bonding wire from the chip to the printed circuit board. This parasitic resistance increases with the temperature.

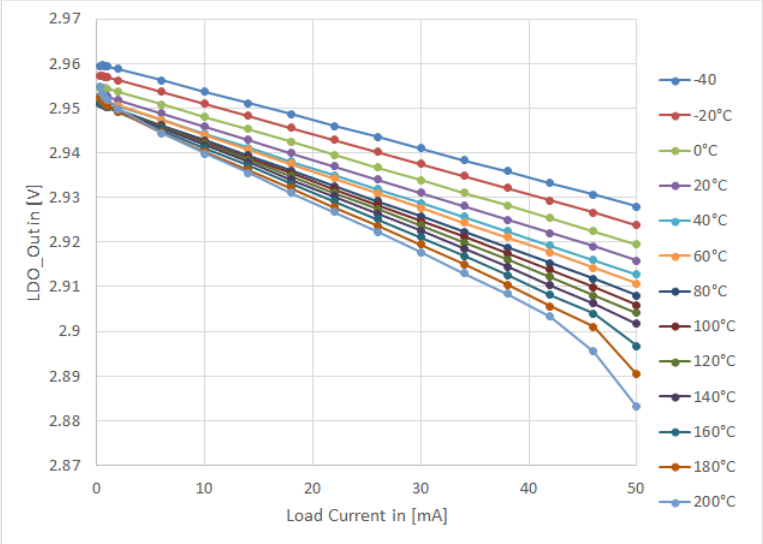

Figure 9.8: Measurement results of load current sweeps under different temperatures for a supply voltage of 3.05 V. The output voltage decreases linearly with the load current, which suggests parasitic resistors in the output path.

The dependency of the quiescent current on the load current is presented in figures 9.10 and 9.11 for the minimum and maximum supply voltage respectively. At the low supply voltage the quiescent current starts very low and increases with the load current. Due to the adaptive biasing stage and the low voltage drop over the pass device, the quiescent current can increase to 1.6 mA. At the high input voltage the quiescent current increases too, but the pass device always stays in saturation and the quiescent current does not reach this high values as with the low supply voltage.

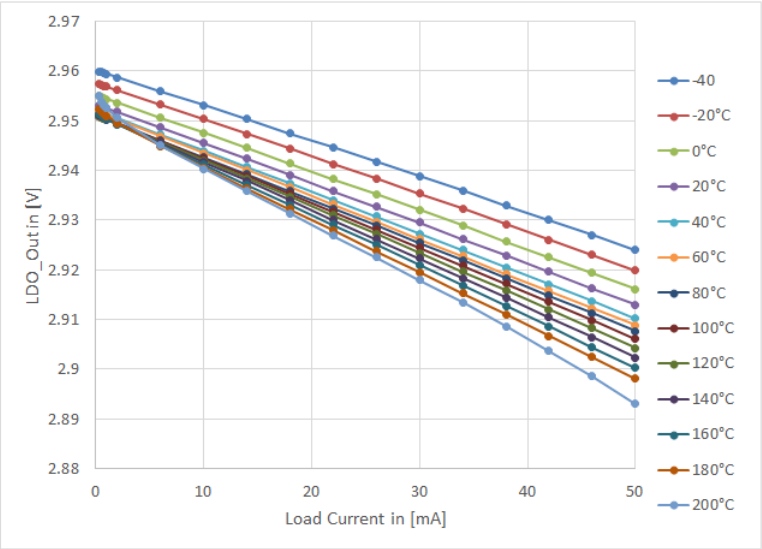

Figure 9.9: Measurement results of load current sweeps under different temperatures for a supply voltage of 8 V. The load current decreases linearly with the output voltage.

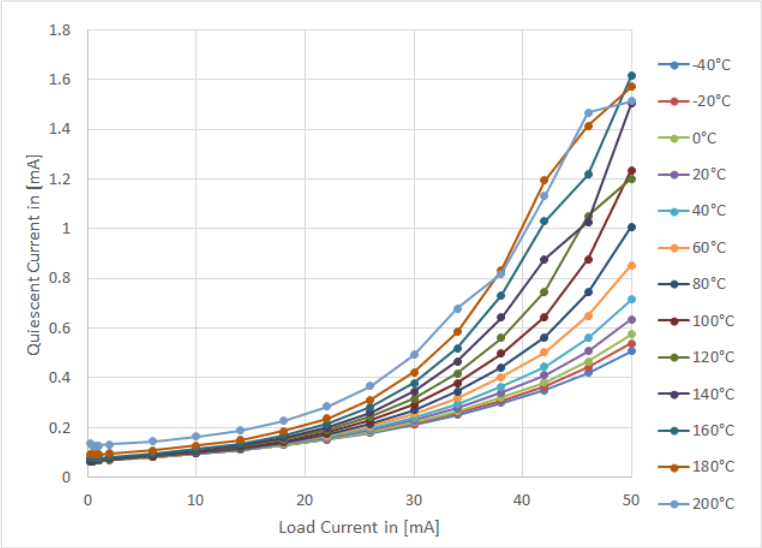

Figure 9.10: Dependency of the quiescent current on the load current for a supply voltage of 3.05 V. The current consumption increases with the load current.

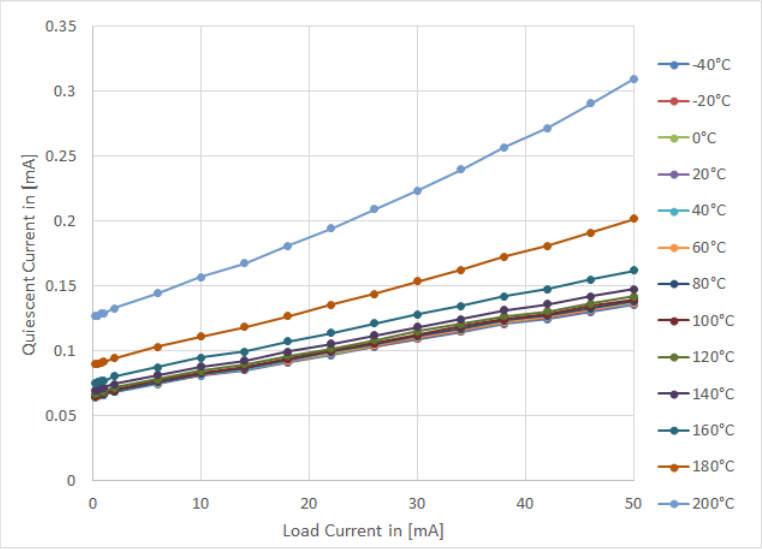

Figure 9.11: Dependency of the quiescent current on the load current for a supply voltage of 8 V. The current consumption of the LDO increases with the load current, but not so strong as with the minimum supply voltage.

Figures 9.12 and 9.13 are showing the relation between the output voltage and the temperature under minimum and maximum load condition respectively. At the low load current the output voltage varies only about 9 mV. Under high load condition the variation of the output voltage is much higher.

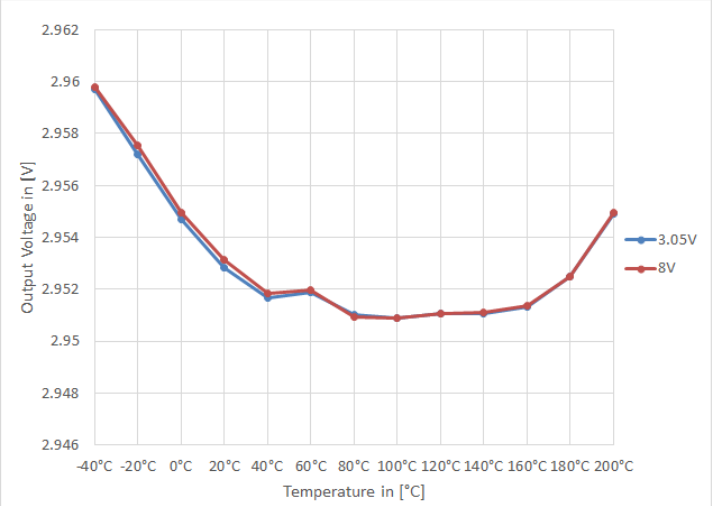

Figure 9.12: Output voltage over temperature for 250 µA load current. The deviation of the output is about 9 mV.

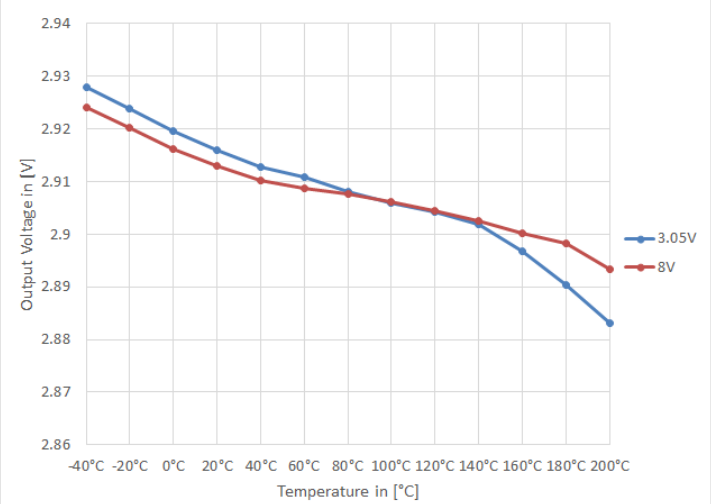

Figure 9.13: Output voltage over temperature for 50 mA load current. The deviation of the output voltage is higher with the minimum supply voltage (3.05 V) than with the maximum supply voltage (8 V).

9.1 Discussion of the Evaluation Results

The leakage current of the diode on the VDD pad increases at 200 °C to about 55 µA. This would be more than the half of the maximum allowed quiescent current, therefore, for applications in this temperature region standard protection pads are not sufficient and special low leakage pads should be used.

Through the self heating of the pass device, due to the high load current and voltage drop over the pass device, the bias current had to be increased to 2.5 µA. This reduces the worst case phase margin to about 26°.

Under low load condition (250 µA) the output voltage varies about 9 mV over the whole temperature region and stays nearly constant over the whole range of the supply voltage. With increasing the load current, the output voltage decreases. The reason for this can be parasitic resistances like the bond wire or the path from the pass device to the output pin.

Neglecting the leakage current of the diode on the VDD pad, the quiescent current of the LDO for a low load current is about 70 µA, which is a bit higher than the simulation results. This could be caused by the higher used bias current. At high load currents and minimum supply voltage the current consumption can increase up to 1.6 mA, which is much higher than the simulation results. A possible reason for this behaviour could be a voltage drop in the supply voltage over parasitic resistances, introduced by the bonding wire and the path from the supply pad to the LDO. This voltage drop causes a smaller voltage as the drop-out voltage over the pass device. With this too low voltage over the pass device, the current consumption of the adaptive biasing stage increases.

This LDO leaves yet room for improvement, especially at high load currents, but it is a working solution and delivers a nearly constant output voltage up to 200 °C.

10 Conclusions and Future Work

In this work a high temperature LDO was designed. As pass-device a PMOS transistor is used. The advantage of using a PMOS pass-device is that there is no charge pump necessary to get low drop-out voltages. The disadvantages of the PMOS, compared to an NMOS, are the larger device size due to the smaller mobility of the charge carriers and the load current depending gain.

As error amplifier, first an ideal one stage error amplifier was analysed together with using the Miller effect to stabilize the circuit. With this concept the additional necessary capacitance would be to large to be realized on-chip. The reason for this is the large output capacitor which causes the non-dominant pole to get to low frequencies near the dominant pole. Therefore, the LDO is realized with the concept of the reverse nested Miller compensation with current buffers. This is a three stage design where the stage driving the pass device is an adaptive biasing stage. This means, the quiescent current increases with the load current and pushes the non-dominant pole to higher frequencies.

This LDO was implemented on a test-chip and evaluated. Due to high leakage currents and heating through the high current and the high supply voltage the LDO was not working properly at 200 °C. Increasing the bias current solved this problem but introduces a smaller phase margin and a higher variation of the output.

The hardest part at working at this thesis was to get a reasonable phase margin over the whole temperature region, due to the big differences of the threshold voltage and the leakage currents between minimum and maximum temperature.

The figure of merit (FOM) is used to compare the transient behaviour of LDOs [1] and is defined by

$$FOM = \frac{C_{Out}\,\Delta V_{Out}\,I_Q}{I^2_{Load\_max}}. \tag{10.1}$$

The lower the value of the FOM the better the transient behaviour.

The current efficiency is the ratio between the quiescent current and the load current:

$$\text{Current efficiency} = \frac{I_{Load\_max} - I_Q}{I_{Load\_max}} 100\%. \tag{10.2}$$

A high current efficiency means, the LDO is able to source high currents by having a small current consumption. Therefore, the higher the current efficiency the better.

Table 10.1 compares this LDO with previously reported LDOs. This LDO has the highest supply voltage range and compared to [1] [2] and [17] a lower drop-out voltage. The high current consumption together with the smaller load current are resulting in a high figure of merit. But the main reason for this high current consumption is the ability to operate at temperatures up to 200 °C, where the other LDOs are only able to operate up to 80 °C or 125 °C.

	[1]	[2]	[17]	[18]	This Work
Year	2007	2009	2010	2014	2014
Technology	0.35	0.6	0.5	0.35	0.35
V_{DD} [V]	2 - 5.5	3.5 - 5	1.4 - 4.2	3.32 - 5	2.75 - 8
V_{Out} [V]	1.8	3.3	1.21	3.3	2.65, 2.95
$V_{Drop-Out}$ [mV]	200	200	200	20	100
I_{Load_max} [mA]	200	220	100	220	50
I_Q @ I_{Load_max} [µA]	340	400	45	120	300
ΔV_{Out} mV	54	N.A.	120	137	90
FOM [ps]	27	N.A.	59	340	10800
Current efficiency [%]	99.8	99.82.	99.95	99.85	99.4
C_{Out} [µF]	1	4.7	0.1	1	1
Temperature [°C]	N.A.	N.A.	-40 - 80	-40 125	-40 - 200

Table 10.1: Comparison of this work with previously reported LDOs.

This LDO meets the given specification by using a higher bias current, but this decreases the phase margin and increases the output deviation. Therefore, future work could be to investigate and solve this problem.

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