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100 MHz Voltage Averaging Feedback Relaxation Oscillator

DIPLOMA THESIS

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Statutory Declaration

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Abstract

Integration of complete systems on a single chip is state of the art. Modern integrated circuits include analogue and digital circuits and are necessary to obtain high performance and power-efficient systems. The integration of synchronous digital circuits requires a stable and accurate clock reference.

Oscillators generate a clock reference. There are different types of oscillators, like external crystal, on chip relaxation oscillators or on chip LC oscillators.

A voltage averaging feedback concept for higher frequencies is proposed to overcome problems with conventional relaxation oscillators such as sensitivity to comparator delay. Based on the voltage averaging feedback concept by Yusuke Tokunaga [1] a new circuit topology was developed. The original topology does not achieve accuracy less than ±2% for an output frequency of 100MHz. Therefore the topology was modified.

The new topology compensates variations of the supply voltage, the comparator delay and the delay times of the used digital gates have no influence on the output frequency, as long as the voltage reference is proportional to the supply voltage.

Two 100 MHz relaxation oscillators were designed with this topology. The main difference between them, are the amplifiers used in the control loop. The different amplifiers have different current consumptions and gain. Both are fabricated in a 0.35 µm CMOS process as test chip. The test chip evaluation in the laboratory is out of scope of this diploma thesis.

The oscillators were simulated over temperature. The output frequency varies less than ±1.5% over a temperature range from -40°C to +125°C.

Kurzfassung

Die Integration von kompletten Systemen auf einen Chip ist der aktuelle Stand der Technik. In modernen integrierten Schaltungen werden analoge und digitale Schaltungen gemeinsam verwendet. Das ist die Voraussetzung für ein leistungsfähiges und Energie effizientes System. Die Integration von synchronen digitalen Schaltungen erfordert eine stabile und genaue Zeitbasis.

Oszillatoren erzeugen diese Zeitbasis. Es gibt verschiedene Arten von Oszillatoren wie externe Quarzoszillatoren, auf den Chip integrierte Relaxationoszillatoren oder auch auf den Chip integrierte LC Oszillatoren.

Ein neues *voltage averaging feedback* Schaltungskonzept wird vorgestellt, welches dazu dient, die Probleme von gewöhnlichen Relaxationsoszillatoren, wie Abhängigkeit von der Komparator Verzögerungszeit, zu minimieren. Basierend auf dem *voltage averaging feedback* Konzept von Yusuke Tokunaga [1] wurde eine neue Schaltungstopologie entwickelt. Die ursprüngliche Schaltung konnte keine höhere Genauigkeit als ±2% für die Frequenz von 100 MHz erreichen. Darum wurde die Schaltung modifiziert.

Die neue Schaltung kompensiert die Variationen der Versorgungsspannung. Die Verzögerungszeiten der Komparatoren und der digitalen Schaltungsteile haben keinen Einfluss auf die Ausgangsfrequenz, solange die Referenzspannung proportional zur Versorgungsspannung ist.

Zwei 100 MHz Relaxationoszillatoren wurden mit dieser Topologie gebaut. Der Unterschied zwischen ihnen ist der verwendete Verstärker in der Regelschleife. Die beiden Verstärker haben unterschiedliche Stromaufnahmen und Verstärkungen. Beide Oszillatoren wurden in einem 0,35µm Prozess als Testchip gefertigt. Die Evaluierung des Testchips ist nicht Teil dieser Diplomarbeit.

Die Oszillatoren wurden über Temperatur simuliert und die Ausgangsfrequenz schwankt weniger als ±1,5% über den Temperaturbereich von -40°C bis 125°C.

Contents

Glossary

Symbol	Declaration	Unit
A_0	Open loop gain	$[dB]$
C	Charge capacitor	$[F]$
C_{int}	Capacitor of the integrator	$[F]$
C_L	Load capacitance	$[F]$
C_{OX}	Capacitance of the gate oxide per unit area	$\left[\frac{F}{m^2}\right]$
f_{int}	Unity gain frequency of the integrator	$[Hz]$
f_T	Unity fain frequency	$[Hz]$
GBW	Gain bandwidth product	$[Hz]$
g_m	Small signal transconductance	$\left[\frac{A}{V}\right]$
I_{NTC}	Current with a negative temperature coefficient	$[A]$
I_{PTC}	Current with a positive temperature coefficient	$[A]$
k’	Transconductance parameter	$\left[\frac{A}{V^2}\right]$
L	Length of transistor	$[m]$
n	Ratio charge to discharge time	$[1]$
PM	Phase margin	$[°]$
R_1	Charge and discharge resistor	$[\Omega]$
R_2	Charge resistor	$[\Omega]$
R_{int}	Resistor of the integrator	$[\Omega]$
R_{NTC}	Resistance with a negative temperature coefficient	$[\Omega]$
R_{PTC}	Resistance with a positive temperature coefficient	$[\Omega]$
slope	Slope of the input voltage of the OTA based comparator	$\left[\frac{V}{s}\right]$

SR	Slew Rate	$\left[\frac{V}{s}\right]$
T	Period time 1/f	$[s]$
t_{charge}	Time to charge capacitor	$[s]$
TCR1	First order temperature coefficient	$\left[\frac{ppm}{K}\right]$
TCR2	Second order temperature coefficient	$\left[\frac{ppm}{K}\right]$
t_d	Delay time of the comparator	$[s]$
$t_{discharge}$	Time to discharge capacitor	$[s]$
u(s)	Input signal of the OTA based comparator in s-domain	$[V]$
u(t)	Input signal of the OTA based comparator in time-domain	$[V]$
u_a(s)	Output signal of the OTA based comparator in s-domain	$[V]$
u_a(t)	Output signal of the OTA based comparator in time-domain	$[V]$
v_c	Control voltage	$[V]$
v_d	Voltage differences between the inputs of the OTA	$[V]$
v_{dd}	Supply	$[V]$
v_{ref}	Voltage reference	$[V]$
v_{ss}	Ground	$[V]$
v_{TH}	Threshold voltage of transistor	$[V]$
W	Width of transistor	$[m]$
α	Ratio voltage reference to supply	$[1]$
ω_T	Unity gain frequency	$\left[\frac{rad}{s}\right]$

1 Introduction

1.1 Motivation

Integration of complete systems on a single chip is state of the art. Modern integrated circuits include analogue and digital blocks which are necessary to obtain high performance and power-efficient systems. Synchronous digital circuits always need a clock reference. This clock reference has to be stable over temperature. External crystal oscillators achieve high performance and are stable over temperature, but they are sensitive to mechanical stress, need additional components, are expensive, need more area and the chip needs additional pins. In modern circuit design, external components are undesirable.

Modern integrated systems need fully integrated, temperature stable, accurate and low-power clock references. The frequency of the clock reference is determined by passive devices like resistors, capacitors or inductors. The on-resistance of MOS devices is not stable over the voltage range. This is the reason why the influences of the MOS devices to the output frequency have to be minimized. The problem of integrated oscillators is that the passive devices have tolerances over process and temperature, which affect the accuracy of the output frequency.

The required 100 MHz frequency is hard to achieve in the used CMOS process because the parasitic capacitances and resistances have effect on the output frequency. These effects are undesired.

1.2 Specification of the project

A 100 MHz voltage averaging feedback relaxation oscillator has to be developed in a 0.35 µm CMOS process for this diploma thesis. The oscillator has to achieve an accuracy of ±1% over the temperature range from -40°C to +125°C. The available 3.3 V supply voltage has an accuracy of ±100 mV and ±1.5% accuracy over temperature.

The oscillator current consumption must be less than 1mA and the oscillator has to drive a 500fF capacitive load. The CMOS process offers 4 metal layers, poly-poly-capacitors, poly-resistors, high-resistance-poly-resistors and logic devices.

The oscillator will be manufactured as a test chip. The layout will be done at Dialog Semiconductor. The test chip measurements are out of scope of the diploma thesis.

2 Theoretical background

2.1 Generation of an electrical frequency on a chip

Oscillators are used to generate an electrical frequency. Oscillator contains one or more energy tanks [2]. Energy tanks are able to exchange energy with another energy tank or a resistive component. A look at the units (1) of passive devices in integrated circuits shows, that a combination of passive devices generates a time domain, shown in (2).

$$[L] = \frac{Nm}{A^2} = \Omega s$$
$$[C] = \frac{A^2 s^2}{Nm} = \frac{s}{\Omega} \quad (1)$$
$$[R] = \frac{Nm}{A^2 s} = \Omega$$

When two different energy tanks are used, energy transformation during the energy exchange occurs. This conversion happens in a certain time, depending on the properties of the two energy tanks. When just one energy reservoir and one resistor are used a time constant is provided.

$$\left[\frac{1}{RC}\right] = \frac{1}{\frac{A^2 s^2}{Nm}} \cdot \frac{1}{\frac{Nm}{A^2 s}} = \frac{1}{s}$$
$$\left[\frac{1}{\sqrt{LC}}\right] = \frac{1}{\sqrt{\frac{Nm}{A^2} \cdot \frac{A^2 s^2}{Nm}}} = \frac{1}{s} \quad (2)$$

The most commonly used oscillators in modern integrated circuits use a combination of these passive devices (2). The oscillator topology depends on the required output frequency. For frequencies lower than a few MHz, inductors get very large and hard to integrate on a chip. RC oscillators are ideal for lower frequencies, because they are much smaller than LC oscillators for the same output frequency.

Passive devices vary over process and temperature. This variation, depicted in Table 1, affects the accuracy of the output frequency. Most chips have a voltage which achieves accuracy of less than ± 1.5%, which is the most accurate parameter achievable on a chip. An inductor achieves a better accuracy than resistors or capacitors, because the inductance depends on the area needed for the inductor and the area is normally huge. Inductors exhibit a poor quality factor between 10 and 20 and need a huge area which leads to more costs. Inductors are hard to integrate because they need a certain toolkit. The toolkit is normally not

available in a standard CMOS process. Tiling is not possible in the layout. As a result on-chip LC oscillators are hardly used for low frequencies. RC oscillators are difficult to implement for frequencies higher than 40 MHz, because the resistors and capacitors become too small compared to the parasitic capacitors and resistors on the chip.

A ring oscillator is a device composed of an odd number of inverters and is often used in integrated circuits. Its frequency depends on the delay time of the inverters. The delay time can be controlled with the current through the inverter, but currents have a spread over the process. A ring oscillator covers a large frequency range, depending on the current through the inverters, the supply voltage and the size of the inverters. The ring oscillator is an RC oscillator and often used in integrated circuits.

Parameter	**tolerance** $[\%]$
Voltage	± 1.5
Current	± 30
Resistance	± 30
Capacitance	± 20
Inductance	± 5

Table 1: Tolerances of parameter and devices over process [3][4]

All the oscillator types which depend on passive devices, can not achieve accuracy better than the spread of the passive device. These spreads are the reasons why accurate oscillators need a compensation of the tolerance for the process. This compensation is called trimming. There are different methods to trim an oscillator, for example the addition of resistors to the circuit.

Trimming circuits always consume additional area, but without trimming no accurate oscillator frequencies are achievable.

2.2 Types of on-chip oscillators

In technical literature, a difference is made between harmonic oscillators and relaxation oscillators [2].

Relaxation oscillators need only one energy tank in combination with a resistive device and a nonlinear device, like a transistor. A typical property of a relaxation oscillator is the voltage over the energy tank or the current through the energy tank, which is switched at a certain reference level. Relaxation oscillators generate discontinuous waveforms or waveforms with a discontinuous first derivative. A typical type of a relaxation oscillator is a multi-vibrator.

Harmonic oscillators require more than one energy tank. The energy tanks can either be of the same or of different type and they can be combined with a resistive device. Harmonic oscillators can be built by using just linear components and harmonic oscillators produce sine waveforms.

The typical form of a harmonic oscillator is an amplifier with a connection of its own output with a positive feedback loop to its input, depicted in Figure 1. The oscillator needs an initial input signal v_{in} for starting [5]. This initial signal can also be noise. After the start, the input signal is not necessary any more and the switch closes the feedback loop.

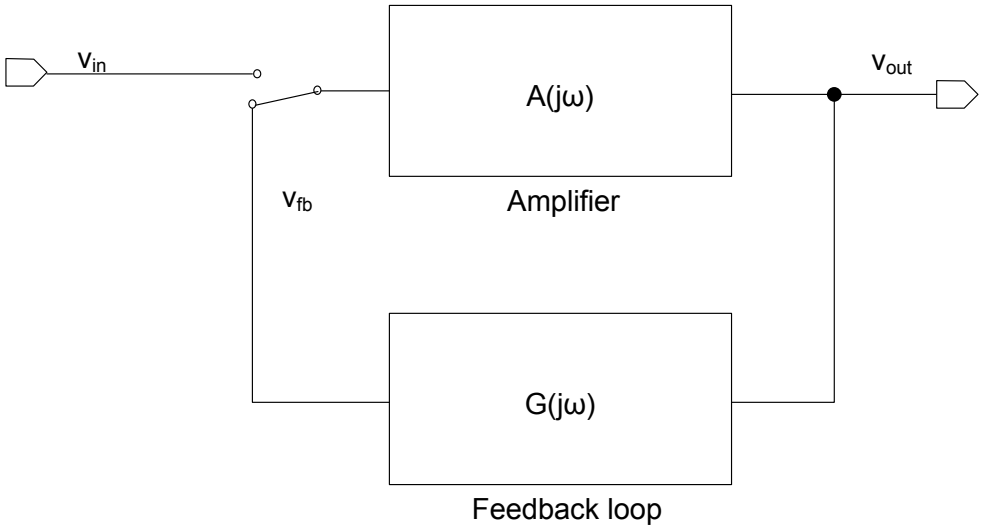

Figure 1: Basic form of a harmonic oscillator

The Barkhausen criterion (3) defines the condition for stable oscillation. The loop gain of the system has to be equal to 1 and the phase shift has to be a multiple of 360°. A typical type of a harmonic oscillator is the Wien bridge oscillator.

$$A(j\omega)\cdot G(j\omega)=1 \quad (3)$$

Relaxation oscillators can not be described by using a transfer function, and it is not possible to use the Barkhausen criterion to describe the output frequency.

2.3 Conventional relaxation oscillator

A commonly known, conventional relaxation oscillator consists of an energy tank, like a capacitor or inductor, and a nonlinear trigger circuit, like a latch or Schmitt trigger. The nonlinear trigger circuit control switches. The switches periodically switch on and off the current sources. The current sources periodically charge and discharge the energy tank. A typical implementation is depicted in Figure 2.

The capacitor C is charged with the current source I_1 till the voltage reaches the voltage v_{high}. Then the comparator $Comp_1$ changes its output and resets the RS-flip-flop. The switch S_1 disconnects the current source I_1 from the capacitor. The switch S_2 connects the current source I_2 to the capacitor C. The capacitor gets discharged by I_2 till the voltage v_{osc} reaches the voltage v_{low}. Afterwards the output of $Comp_2$ sets the flip-flop and the switch S_2 disconnects I_2 and the capacitor C. The switch S_1 connects the current source I_1 with the capacitor. The capacitor gets charged till the voltage v_{osc} again reaches the voltage v_{high}.

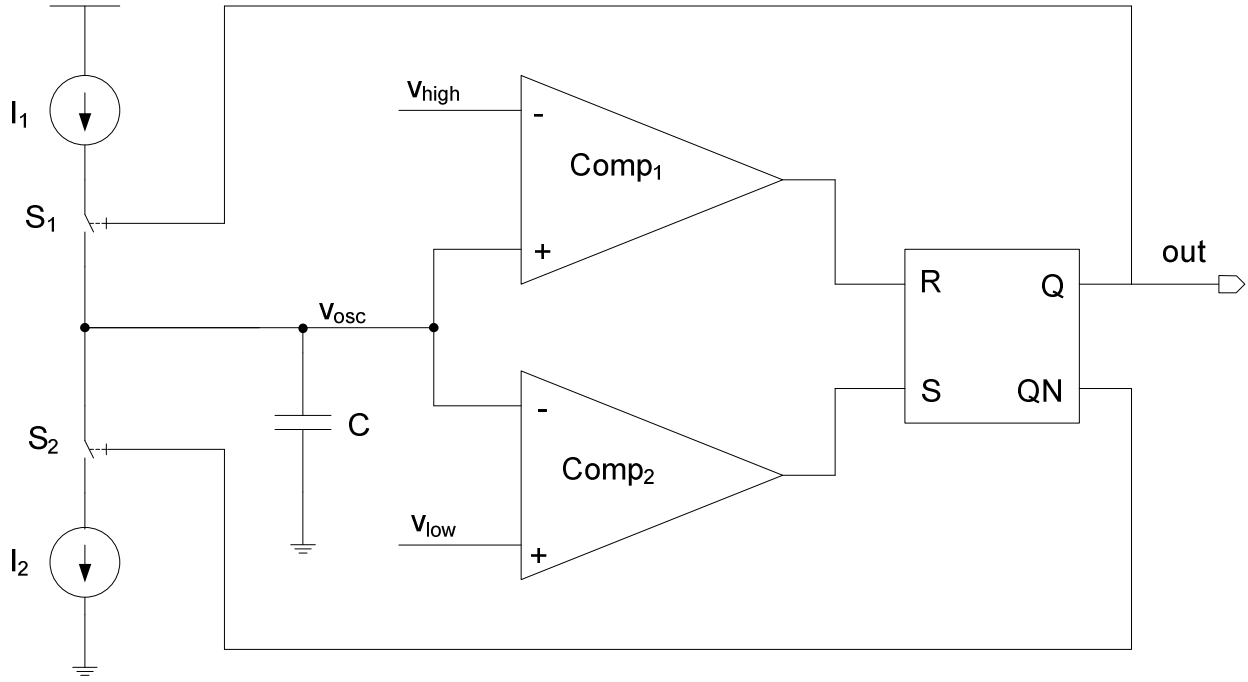

Figure 2: Conventional relaxation oscillator

In this manner a periodic square output signal is generated, depicted in Figure 3. The frequency of this output signal is defined by the charge, the discharge times and the delay time of the comparators, shown in equation (4).

$$f_{osc} = \frac{1}{T} = \frac{1}{t_{charge} + t_{dComp1} + t_{discharge} + t_{dComp2}} \quad (4)$$

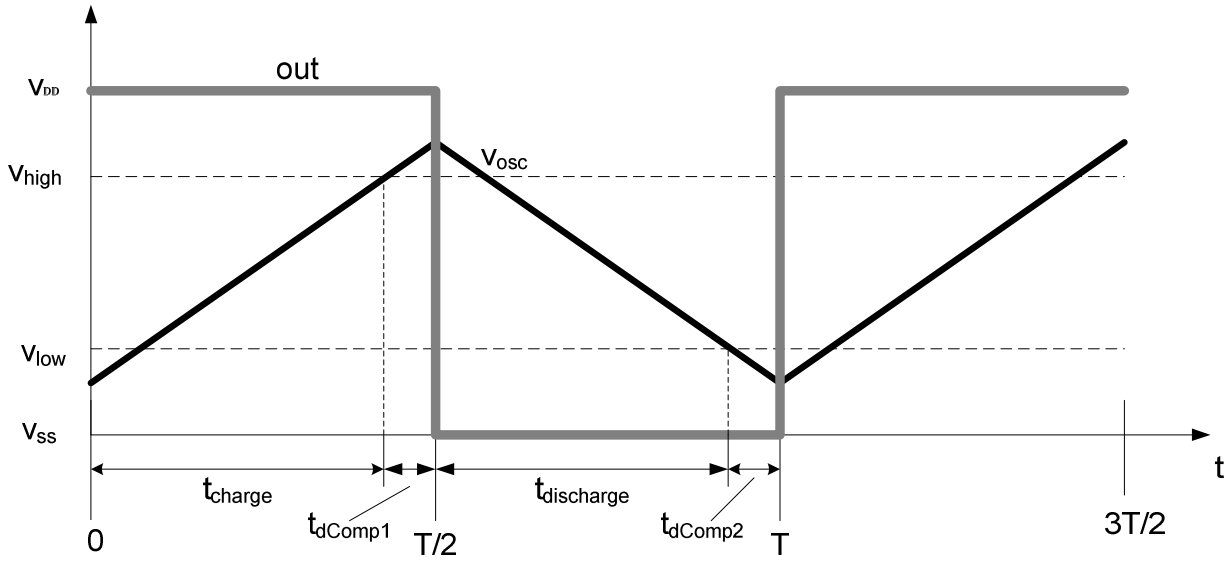

Figure 3: Waveform of the oscillating signal a relaxation oscillator

A general issue for that kind of oscillation circuits is the variation of the delay time of the comparator over temperature and process. A simple solution to reach higher accuracy is to shorten the delay time so that it can be neglected. However this approach increases the current consumption of the comparators and that does not fit in with a low power design. The delay of the comparators has to be below one percent of t_{charge} and $t_{discharge}$ to reach an overall accuracy of less than ± 1%.

Other issues of that circuit are the aging of the current sources and flicker noise. Those issues can be reduced by using resistors instead of current sources. The use of resistors has the disadvantage that resistors have a spread over the process of ±30%. Not only the resistors also the used capacitors have ±20% spread. The spread can be compensated with a trimming circuit.

While spread of resistors and capacitors can be compensated, the variation of the delay time is hard to compensate. The frequency accuracy of that oscillator depends on the variation of the delay time, on the comparators and on the spread of resistors and capacitors as well as the aging of current sources. It is hard to achieve a highly accurate frequency with low power and small area.

2.4 Concept of a relaxation oscillator with voltage averaging feedback

This part of the diploma thesis refers to the IEEE-paper from Yusuke Tokunaga, Shiro Sakiyama, Akinori Matsumoto and Shiro Dosho [1].

The voltage averaging feedback concept, depicted in Figure 4, offers a solution to overcome conventional relaxation oscillator problems as sensitivity to comparator delay. This concept consists of a complementary relaxation oscillator and an active integrator as a voltage averaging feedback. The oscillator can be seen as a voltage controlled oscillator with v_c as the control voltage.

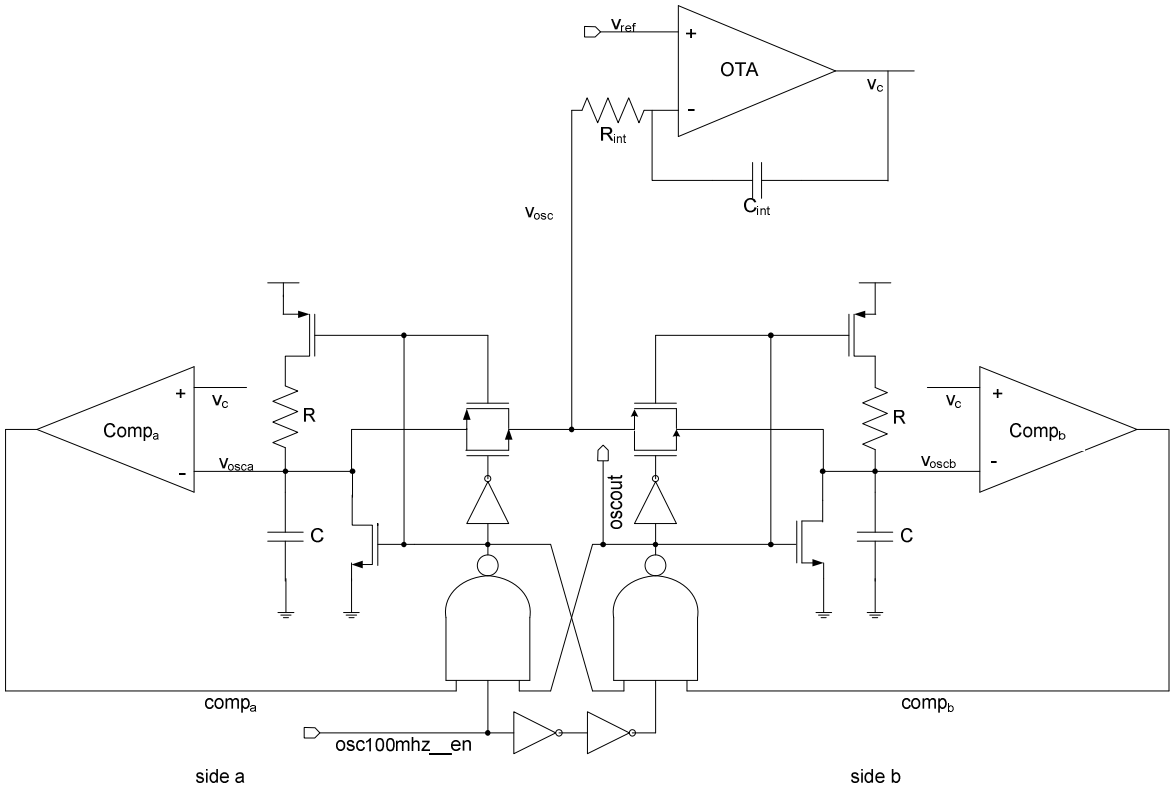

Figure 4: Relaxation oscillator with voltage averaging feedback

The oscillating signals $v_{osca,b}$, are shown in Figure 5 and can be described with equation (5). The voltage averaging feedback uses a reference voltage v_{ref}, which is proportional to the supply. The voltage averaging feedback compares the dc part of the oscillating signal with the reference v_{ref}, depicted in equation (6) and determines the threshold v_c for the comparators.

$$v_{osca,b}(t) = v_{dd}\left(1 - e^{-\frac{t}{RC}}\right) \quad (5)$$

$$\frac{1}{T}\int_0^T v_{osca,b}(t)dt = v_{ref} \quad (6)$$

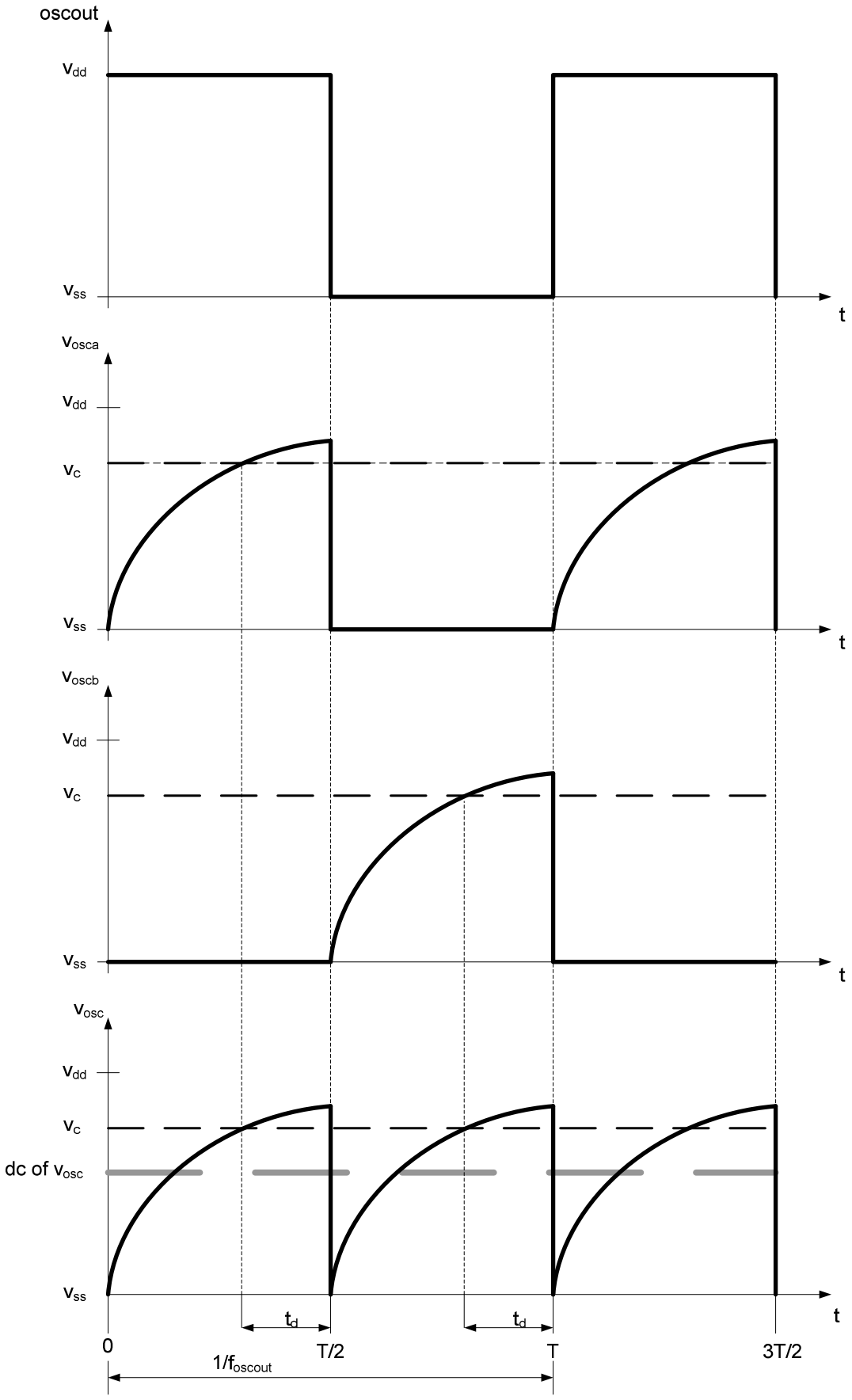

Figure 5: Waveforms of the oscillating signals

Equation (7) is the result of formula (6) and means that the output frequency is just defined by the time constant *RC* and the proportional factor v_{ref}/v_{dd}. The variation of the delay time t_d has theoretically no effect on the output frequency, because the active integrator automatically adjusts its output v_c to keep the equation (6) true. In this matter the required stable frequency is generated.

$$\frac{\left(1-\frac{v_{ref}}{v_{dd}}\right)T}{RC} = 1 - e^{-\frac{T}{RC}} \quad (7)$$

This fact allows a low power comparator design. The comparators must be fast enough for the desired output frequency, but the variation of the comparator delay time and it offset do not affect the output frequency. The delay time of the comparators have to be less than a fourth or a third of the desired time domain.

The active integrator consists of a resistor, a capacitor and an operational transconductance amplifier OTA with a high gain and a high unity gain frequency.

Equation (7) also shows that the oscillator frequency does not have any sensitivity to the supply voltage v_{dd}, because the ratio v_{ref}/v_{dd} has to be constant. The ratio can be fixed for example by a simple resistive divider.

The time determining part is the time constant *RC*, but this time constant is affected by the finite size of integrator resistor R_{int}. This time determining system is depicted in Figure 6, the on-resistance and capacitance of the transmission gate are neglected.

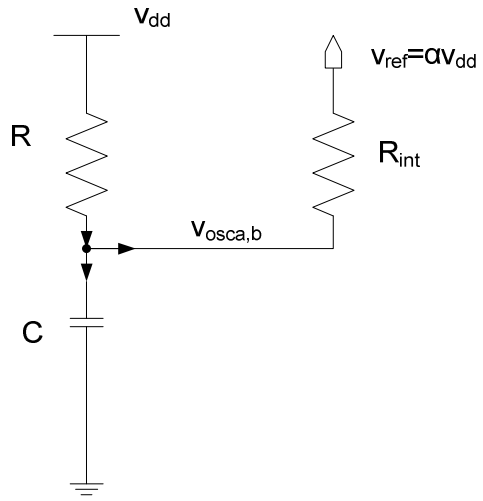

Figure 6: Simplification of time determining system

Equation (8) describes the circuit with the Kirchhoff's current law. Now the oscillating signal v_{osc} is calculated. Equation (9) depicts the effects of R_{int} to the oscillating signal v_{osc}.

$$\frac{v_{dd} - v_{osca,b}(t)}{R} = C\frac{dv_{osca,b}(t)}{dt} + \frac{v_{osca,b}(t) - v_{ref}}{R_{\text{int}}} \quad (8)$$

$$v_{osca,b}(t) = v_{dd}\frac{1+\alpha\dfrac{R}{R_{\text{int}}}}{1+\dfrac{R}{R_{\text{int}}}}\left(1 - e^{-\frac{1}{RC}\left(1+\frac{R}{R_{\text{int}}}\right)t}\right) \quad (9)$$

It is not a problem to consider the integrator resistor in the calculation of the output frequency, since it is constant over the needed voltage range. As a result of equation (9) the effects of R_{int} to the signal v_{osc} can be neglected if R_{int} is much larger than R.

The other issues of typical relaxation oscillators, like aging of the current sources und flicker noise, are reduced in this circuit topology. Here, passive devices are used instead of current sources. Other noise sources are comparators. The noise of the two comparators is suppressed by the high pass filter like transfer function of the voltage averaging feedback. The symmetry of the circuit defines the duty cycle. Passive devices have a large spread over process, but they match well. The matching of devices depends on the size of the device and the surroundings on the chip. Layout methods for best matching, like common centroid layout, have to be applied.

A certain start-up sequence is important for this oscillator. In the reset state, all signals have a defined state, the enable signal *osc100mhz_en* is LOW, the threshold of the comparators v_c has to be pushed up to supply and the oscillating signals $v_{osca,b}$ are pulled down by the NMOS transistors by a HIGH at the outputs of the two cross coupled NAND gates.

When the enable signal *osc100mhz_en* becomes HIGH, *side a* starts first and blocks *side b*, because of the delay of the two inverters between the both NANDS. It is very important for the start-up to be defined, because otherwise the oscillator can get stuck if both sides start at the same time. The output of the NAND at *side a* changes its output to LOW and the capacitor at *side a* is charged over the resistor. When the voltage of the capacitor reaches the threshold of the comparator $Comp_a$, the comparator changes its output and the NAND on *side a* changes its output. Now all inputs of the NAND at *side b* are HIGH and the NAND switches its output to LOW. The capacitor at *side b* is charged till the voltage reaches the threshold of the comparator. The capacitor on *side a* is discharged. In this matter a stable frequency is generated.

3 Implementation of a 100 MHz voltage averaging feedback relaxation oscillator

3.1 Specification of the oscillator sub-blocks

For the specification of the sub-blocks of the most suitable topology, a top-down design strategy was chosen. With this top-down the specification of each block was approach. The comparators and OTAs were formulated in Verilog-AMS models [6].

At the beginning this top-down design needs more time, but it is easier to detect the real requirements. When the specification is changed later, the same models can be used to detect the new requirements.

The circuit topology was analysed, and only after that the sub blocks were specified exactly. When a topology met the requirements of the oscillator specification, the Verilog-AMS models were replaced step by step with schematic circuits.

In this matter, the blocks were exactly specified. An accurate topology for the required frequency is developed.

It is possible to reduce the simulation time by using the Verilog-AMS models and the schematic in one and the same simulation. Only the new designed block is simulated as a schematic and the other blocks are simulated as Verilog-AMS models. For this simulation mode, the models have to describe the behaviour of the schematic exactly.

At the end of the design all blocks are simulated as schematic.

With this approach, the original concept of the relaxation oscillator with voltage averaging feedback was adapted several times, as shown in the following subsections.

3.1.1 Original topology with one integrator and two integrator resistors

First the topology of [1] was realized. The detailed circuit is depicted in Figure 4. A switch control was added to ensure a stable output frequency. It is important that the switches always switch in the same controlled sequence with break-before-make to prevent shorts.

It was found that the original circuit topology is not suitable for the required frequency of 100 MHz in this technology. The output frequency is not defined by $R_{a,b}$ and $C_{a,b}$, any more, because the on-resistance and capacitance of the transmission gates affect the output tolerance. That is undesirable because the on-resistance and capacitance of the transmission gates are not constant over the voltage and temperature range.

To avoid these negative effects, the circuit topology was changed. The modified circuit, shown in Figure 7, has two integrator resistors and in this matter the on-resistance of the switch has no effect on the time constant, since the integrator resistor is much larger than the on-resistance of the transmission gate. The integrator resistor affects the time constant, but it can be considered in the calculation of the time constant, because it is constant over the voltage range. When the integrator resistor is more than 10 times larger as the charge resistor, then the effects to the output frequency can be neglected.

The modified topology has a lot of switches. This switches are needed, to ensure a break-before-make sequence. The sequence is shown in the next subsection.

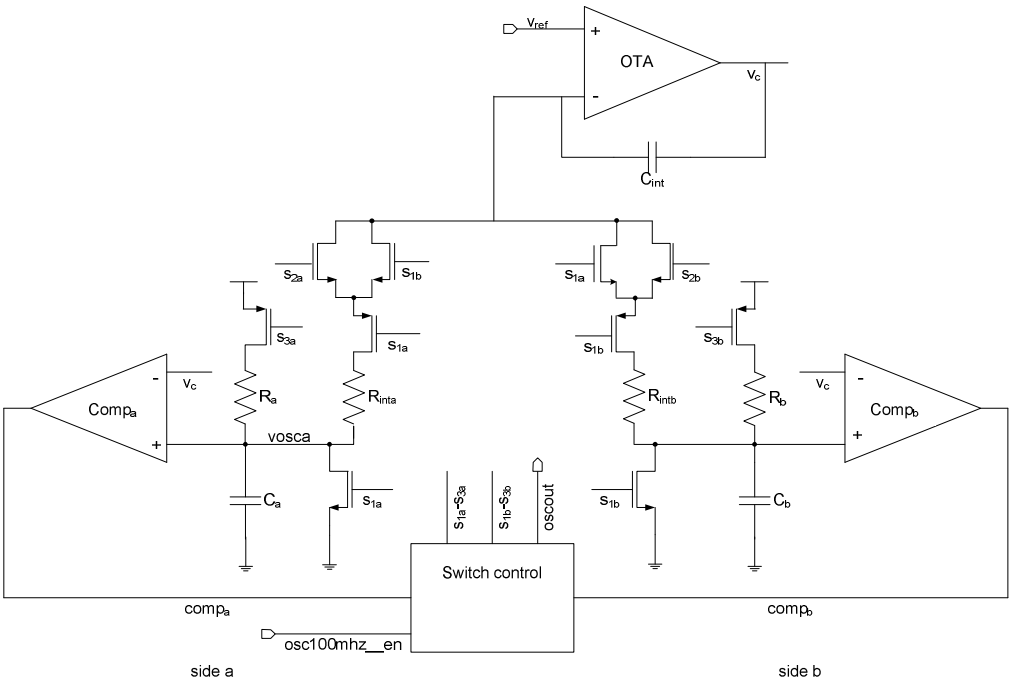

Figure 7: Original topology with one integrator and two integrator resistors

3.1.1.1 Generation of switch signals

To ensure that the oscillator works, a defined start and switching sequence is needed. This sequence prevents shorts. The switch control, depicted in Figure 8, generates a make-before-break sequence, shown in Figure 9, which prevents shorts and assures a defined oscillation.

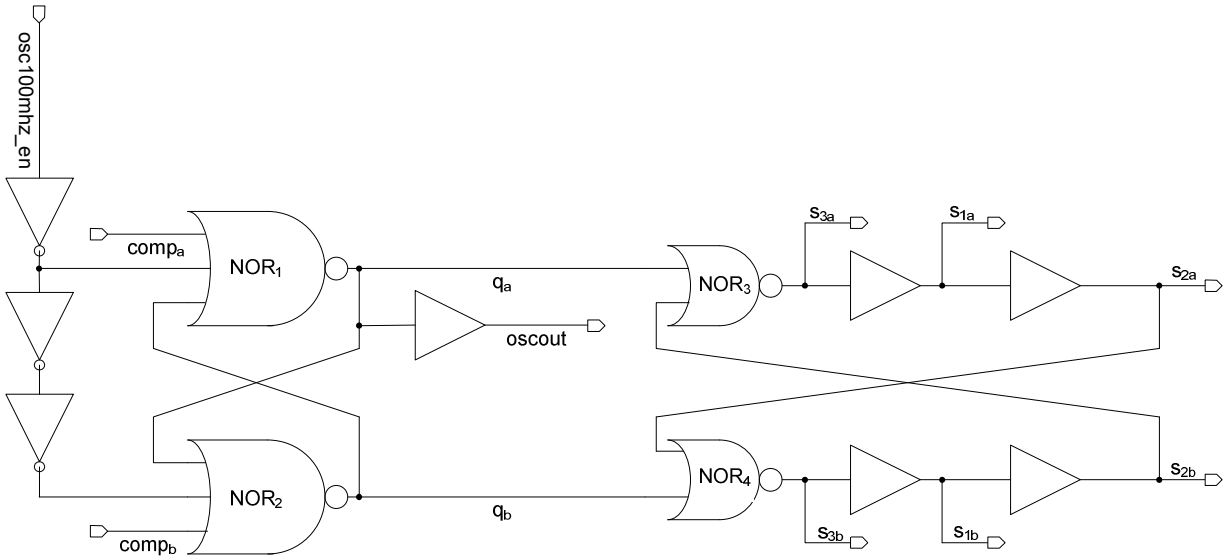

Figure 8: Switch control

In the reset state, all signals have to be defined. The enable signal signal *osc100mhz_en* is LOW, $v_{osca,b}$ are pulled down with the NMOS switches controlled by the signals $s_{1a,b}$, $comp_a$ and $comp_b$ are LOW, the OTA output v_c is pushed up to supply v_{dd}.

When the enable signal *osc100mhz_en* is HIGH, all inputs of the NOR gate are LOW and the cross coupled $NOR_{1,2}$ gates change their outputs and cause s_{3a} to connect the charge resistor and capacitor with the supply.

Afterwards s_{1a} opens the short of the charge capacitor C_a, which is charged now and *side b* is disconnected from the active low pass filter. Now s_{2a} connects *side a* to the integrator. After that all s_{3b} split the charge resistor of *side b* from the supply. Then s_{1b} shorts the capacitor C_b and discharges it.

When the signal v_{osca} reaches the threshold of comparator $Comp_a$, the comparator will change its output. That causes the same effects before, but on the other side.

The switch control consists of a very useful feature. The output of the both $NOR_{1,2}$ gates can not have the state, that both are HIGH. That state is impossible. That guarantees that the signals s_{1a} and s_{1b} are not LOW at the same time which further ensures that these two signals do not start charging capacitance at the same time. This ensures that the oscillator can not get stuck.

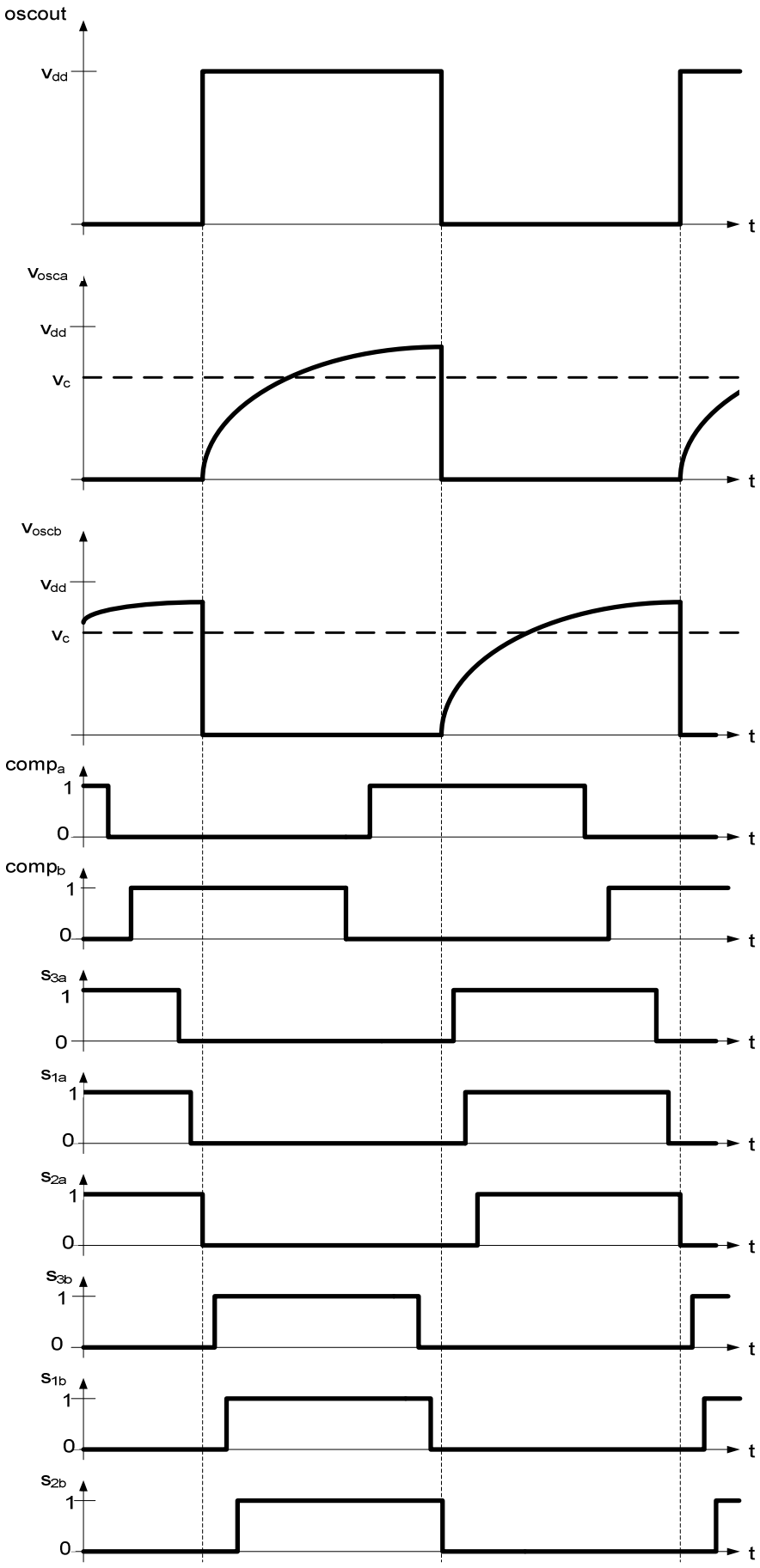

Figure 9: Waveforms of the switch signals of original topology with one integrator

3.1.1.2 Temperature behaviour

The circuit was simulated over the temperature range. The output frequency varied more than ± 4% with Verilog-AMS models for the OTA and comparator.

One reason for that is charge injection, which affects the input signal of the active integrator. Charge injections are unwanted effects of analogue switches. The MOS transistors inject a small electrical charge into the signal when it is switched off [7][8]. A simple switch circuit with a detailed model of a MOS transistor is depicted in Figure 10. The total charge in the channel is described by equation (10).

$$Q_{channel} = WLC_{OX}\left(v_{dd} - v_{in} - v_{TH}\right) \quad (10)$$

The charge injected to the left side of Figure 10 is absorbed by the input source and does not create an error. The charge injected to the right side introduces an error to the voltage stored in the load capacitor C_{load}. If the half of $Q_{channel}$ is injected onto the capacitor C_{load}, the resulting error of the voltage is described by equation (11).

$$v_{error} = \frac{WLC_{OX}\left(v_{dd} - v_{in} - v_{TH}\right)}{2C_{load}} \quad (11)$$

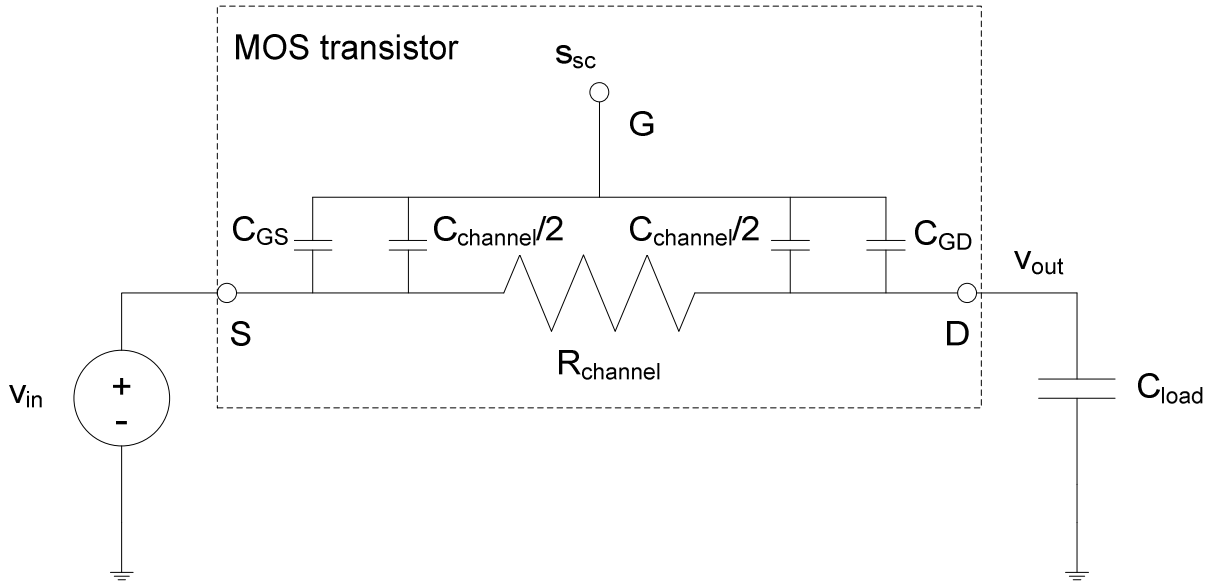

Figure 10: Simple switch circuit with a MOS transistor as switch

That causes a small spike or glitch at the signal. The output signal of an ideal switch is the same as the input signal. The output of a MOS transistor as a switch can be described by equation (12).

$$v_{out} \approx v_{in} - \frac{WLC_{OX}\left(v_{dd} - v_{in} - v_{TH}\right)}{C_{load}} \quad (12)$$

The input/output characteristic of a MOS switch is depicted in Figure 11.

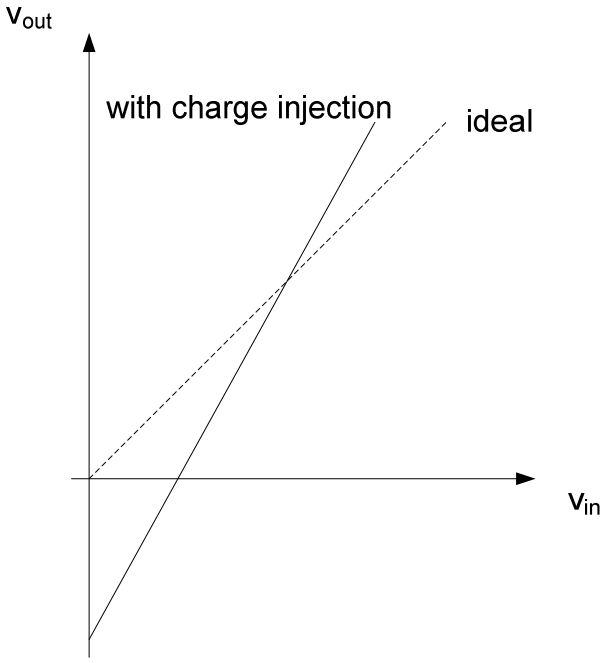

Figure 11: Input/output characteristic of MOS switch

Charge injections cause three types of errors in a switched circuited. These are gain error, DC offsets and nonlinearity.

Another reason is the variation of the delay times of the digital gates, of the switch control. Every delay time of each single digital block varies a little bit, added together more than one percent of the required periodic time of the output frequency.

As a result, the required accuracy of ± 1% over the temperature range of -40°C ot +125°C can not be achieved with this circuit topology in this technology.

3.1.2 Modified topology with two integrators

Another topology was developed, shown in Figure 12. This new circuit is proposed to overcome the issues of the original topology such as charge injections and time delays of the digital blocks. This oscillator is completely symmetric and has a second integrator with the same reference. The two symmetric sides are connected by two cross-coupled NAND gates. The two NAND gates make the switch-over between the two sides.

A big advantage of this topology is that the integrator is always connected to the oscillating signal and has not to switch between the two oscillating signals.

A disadvantage is that the discharging period is also time determining and has to be defined. The capacitor is charged via R_1 and R_2 and is discharged via R_1. The discharging time has to be smaller than the charging time.

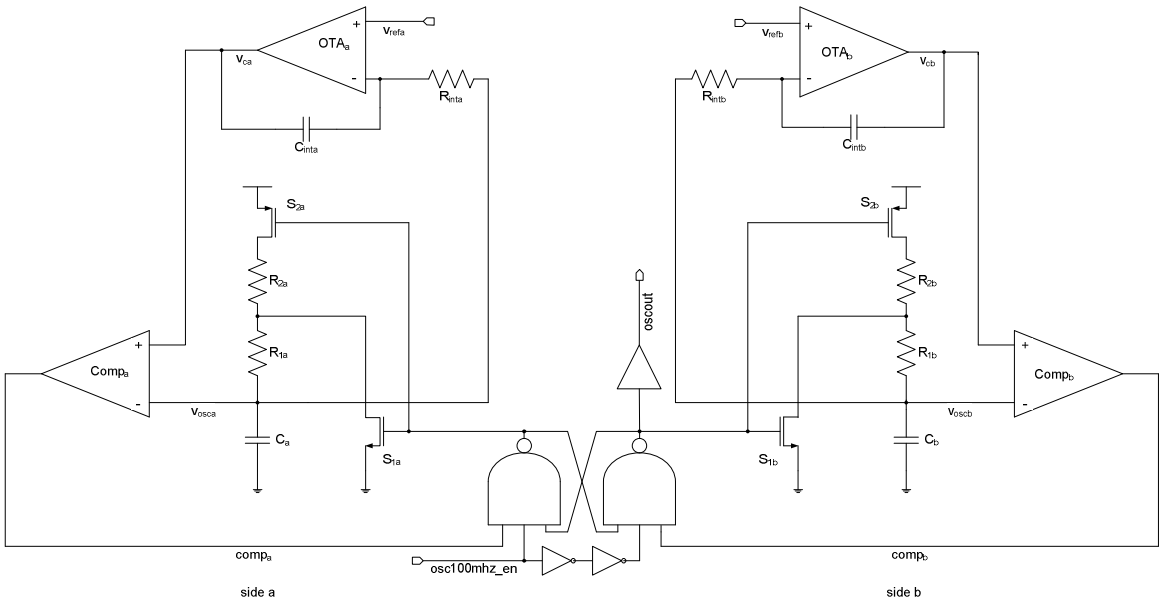

Figure 12: Modified topology with two integrators

3.1.2.1 Generation of the switch signals

The two cross-coupled NAND gates generate the control signals for the switches. All switches of one side of the circuit need only one control signal. The switches $S_{2a,b}$ are just to save power. Note that the PMOS is always switched on before the NMOS switches off at a single steep falling edge of the control signal. The rising edge always switches on the NMOS before the PMOS switches off.

An advantage of the cross-coupled NAND gates is, that both outputs can never be LOW at the same time. Again, this would cause the oscillator to get stuck.

The start-up sequence is very important. In the reset state all signal have to be defined, the enable signal *osc100mhz_en* is LOW, $v_{osca,b}$ are pulled down to ground by the NMOS transistors, $comp_{a,b}$ are HIGH and the OTA outputs $v_{ca,b}$ are pushed up to supply v_{dd}.

When *osc100mhz_en* switches to HIGH all the inputs of the NAND gate at *side a* are HIGH so S_{1a} switches off and S_{2a} switch on. The capacitor C_a is charged over the resistors R_{1a} and R_{2a}. *Side a* always start first, because there is a delay between the two NAND gates, implemented with two inverters. When the voltage v_{osca} exceeds the threshold of the comparator $Comp_a$ the comparator output $comp_a$ gets LOW. Now the output of the *side a* NAND gate goes to HIGH again and the capacitor C_a is discharged over the resistor R_{1a}.

When the output of the *side a* NAND is HIGH, the *side b* NAND pulls down its output and the capacitor C_b gets charged. When v_{oscb} exceeds the threshold of the comparator $Comp_b$, its output gets LOW and the *side b* NAND rises up its output to HIGH again.

In this manner an oscillation is generated. The duty cycle depends on the symmetry of the topology and is typically 50%. The resulting waveforms are depicted in Figure 13.

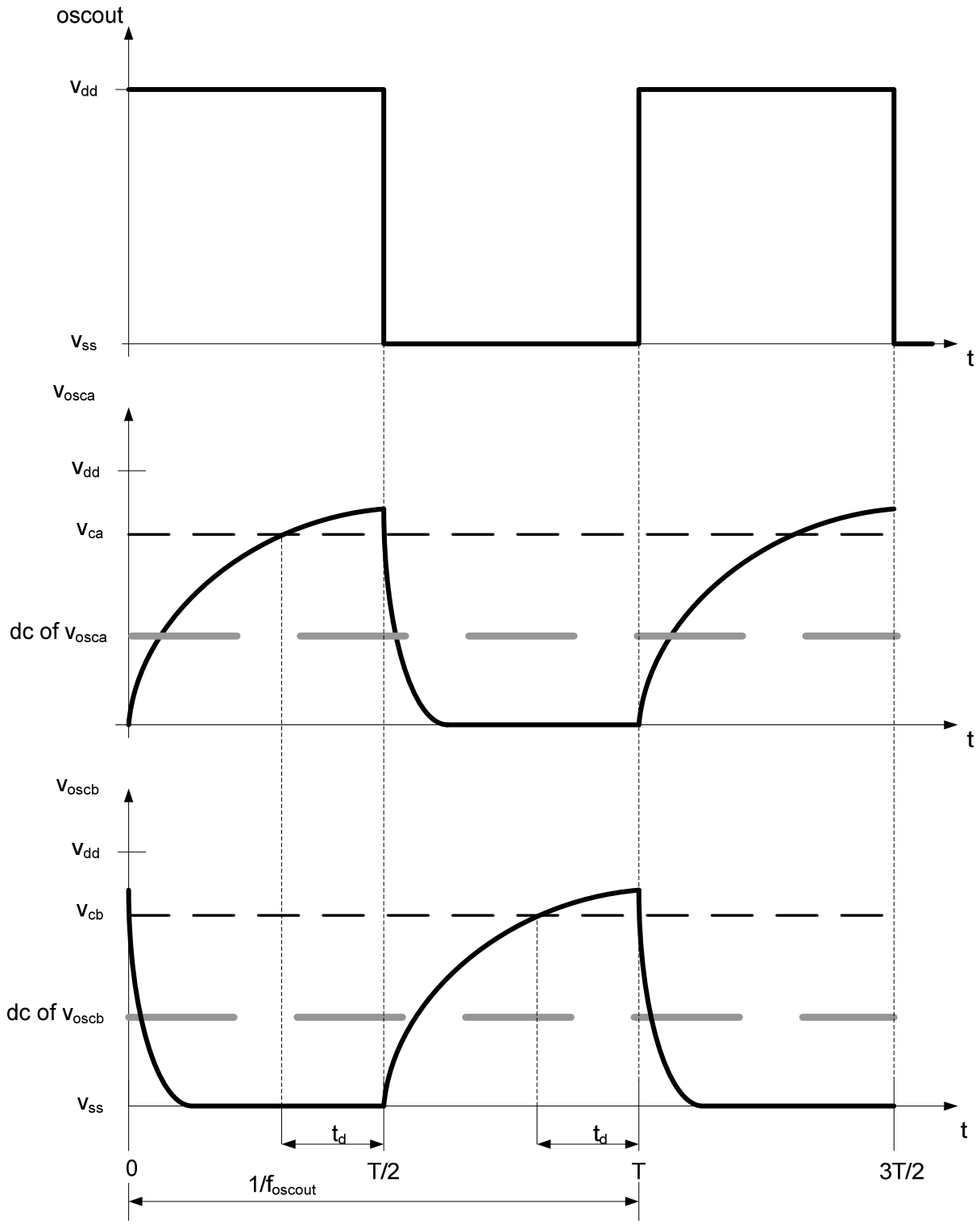

Figure 13: Waveforms of the modified topology with two integrators

3.1.2.2 Temperature behaviour

The circuit was simulated over the temperature range. The output frequency varied by ±2% with Verilog-AMS models for OTA and comparator. The modified topology has a better accuracy than the original one, but not good enough for the specification.

The reason is the variation of the delay times of the cross-coupled NAND. It is more than one percent of the required period time of the output frequency. The problem is that cross-coupled NAND gates are outside of the control loop and therefore the control loop can not compensate the variation.

As a result, the required accuracy of ± 1% over the temperature range of -40°C ot +125°C can not be achieved with this circuit topology.

3.1.3 Final topology with single edge switching

The new topology is a solution to solve the issue of the variation of delay time of the cross-coupled NAND gates. The idea is to use just one of the two outputs of them. This is possible, when *side b* is upside down of *side a*. That means that *side a* refers to ground and side b refers to supply. An advantage of this topology is that the delay time of the two cross-coupled NAND gates is eliminated. The final topology, depicted in Figure 14, requires two different references, where both need to be proportional to the supply voltage.

Both sides have different common mode ranges and that requires two different OTAs and comparators. The reference of *side a* (i.e. v_{refa}) is smaller than $v_{dd}/2$ and the reference of *side b* (i.e. v_{refb}) is always larger than $v_{dd}/2$.

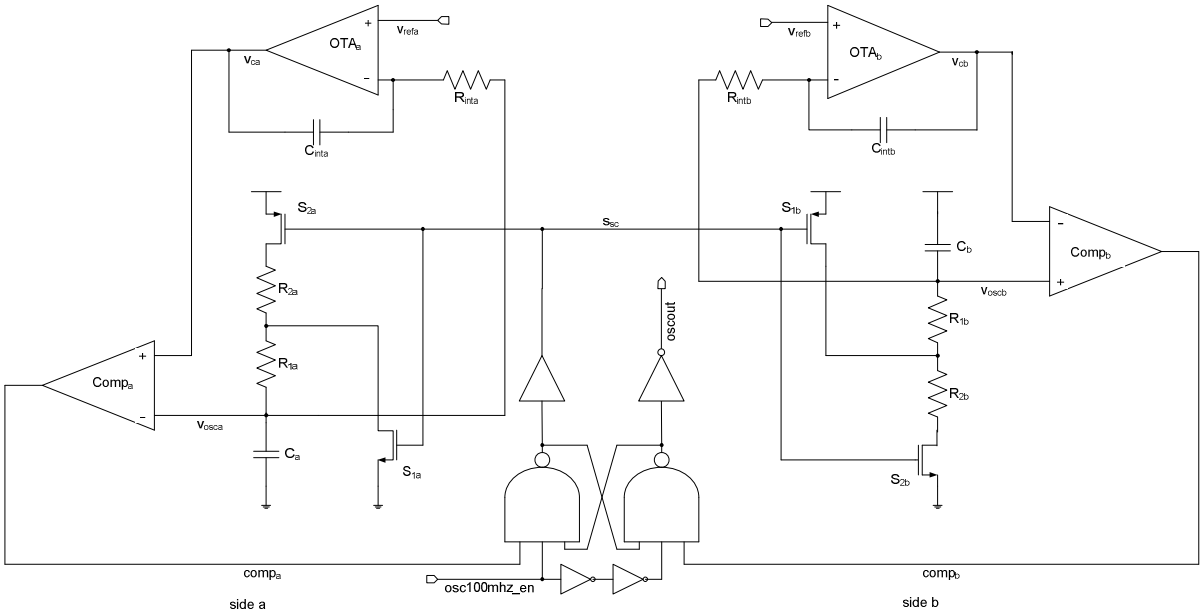

Figure 14: Final topology with single edge switching

The references of each side are related with equation (13).

$$v_{refb} = v_{dd} - v_{refa} \quad (13)$$

Side a uses an OTA and a comparator with PMOS input stages and the *side b* uses an OTA and a comparator with NMOS input stages. The active integrators compensate the time delays of the comparators and determine the thresholds $v_{ca,b}$ of both comparators.

3.1.3.1 Generating of the switch signals

The two cross-coupled NAND gates generate the control signal s_{sc} for the switches. A big advantage of this topology is that the delay time of the cross-coupled NAND gates is eliminated. That is because only one of the outputs of the cross-coupled NAND gates controls all the switches. Hence all the switches are operated with one single edge. Note that the PMOS is always switched on before the NMOS is switched off at a single steep falling edge of the control signal. The rising edge always switches on the NMOS on before the PMOS is switched off.

The start-up sequence is important. In the reset state all signals have to be defined. The enable signal *osc100mhz_en* is LOW, v_{osca} is pulled down to ground, v_{oscb} and v_{ca} is pushed up to supply, $comp_{a,b}$ are HIGH and v_{cb} is pulled down to ground.

When osc100mhz_en switches to HIGH, all the inputs of the NAND gate at *side a* are HIGH and the output of the NAND is pulled down to ground. The signal s_{sc} controls all the switches in the circuit. The capacitor C_a is charged via the two resistors R_{1a} and R_{2a}, at the same time the capacitor C_b is discharged via the resistor R_{1b}. The waveforms of the signals is depicted in Figure 15.

When the voltage v_{osca} exceeds the comparator threshold v_{ca}, the comparator goes to LOW and the cross-coupled NAND gates change their outputs. The capacitor C_b starts getting charged via the resistors R_{1b} and R_{2b}. At the same time the capacitor C_a is discharged via R_{1a}. When the voltage v_{oscb} reaches the threshold of comparator $Comp_b$, the cross-coupled NAND gates change their output again and the capacitors are charged again.

In this matter a stable oscillation is generated. The duty cycle depends on the symmetry of the circuit. The topology is point symmetric, but the differences between the PMOS transistors and the NMOS transistors affects the duty cycle.

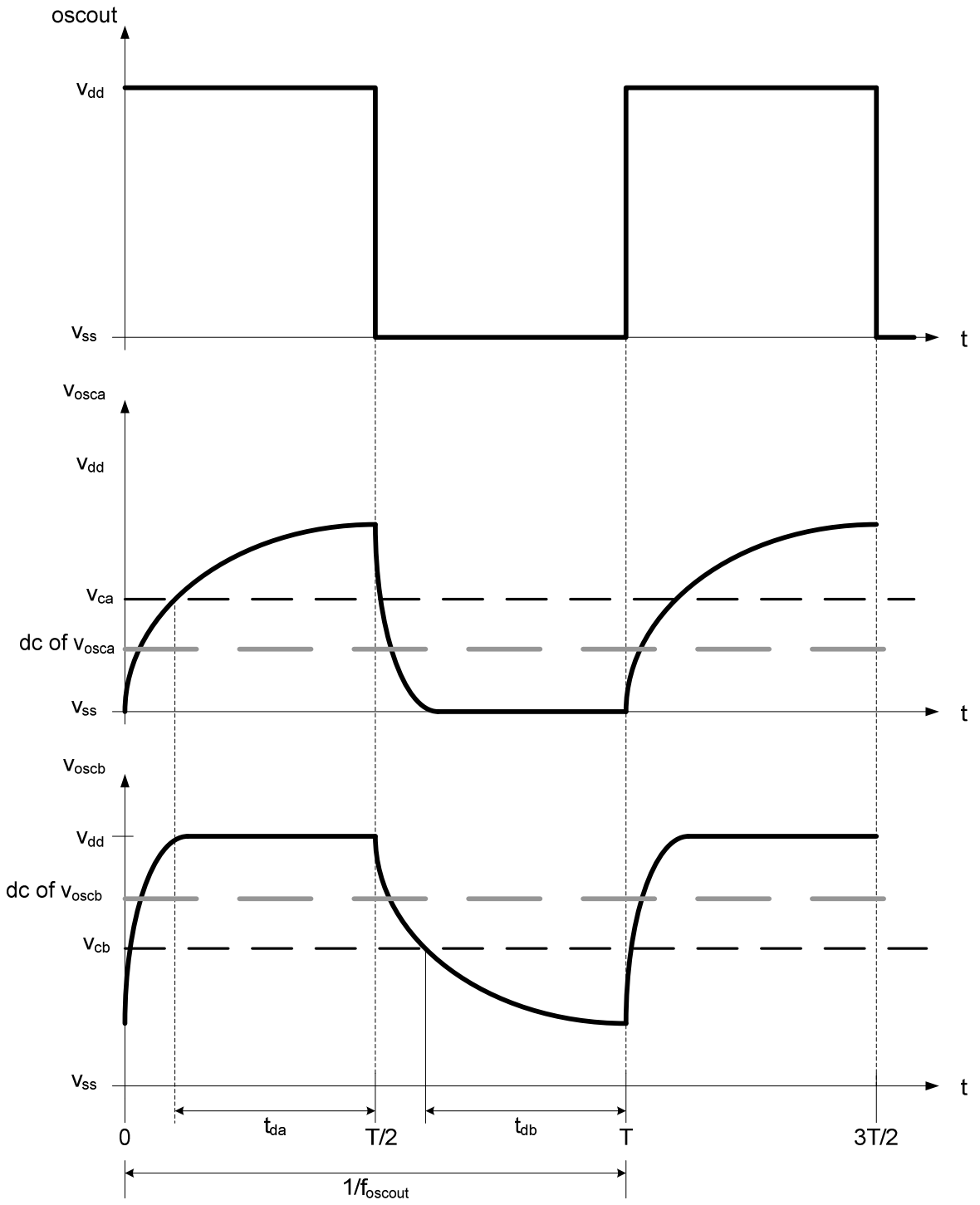

Figure 15: Waveforms of the oscillating signals

3.1.3.2 Temperature behaviour

The output frequency variation is smaller than ±0.1% over the temperature range from -40℃ to +125℃ with ideal comparators, ideal OTAs, ideal resistors, ideal capacitors and ideal switches. The gate delays do not affect the output frequency. The output frequency is defined by the time constant $(R_1+R_2)C$. As the resistance varies over temperature, two different resistors with different resistive material (*rp0h, rp1n*) are used to compensate that variation. In this matter the first order temperature dependence of the resistors is compensated. The second order temperature coefficient still causes a variation of the resistor value.

Table 2 depicted the used resistance materials and their temperature coefficients [9].

resistance material	**Mean TCR1**	**Standard deviation of TCR1**	**Mean TCR2**	**Standard deviation of TCR2**
	[ppm/K]	[ppm/K^2]	[ppm/K]	[ppm/K^2]
rp1n	438	98.9	1.7	3.7
rp0h	-2144	160	7.39	2.48

Table 2: Resistance materials and them temperature coefficients

Figure 16 shows the temperature drift of R_1, the orange one and R_2, the brown one, over the temperature range from -40℃ to +125℃. The resistors have a variation of ±1%. Figure 16 also shows the temperature drift of the used resistor. The green curve is rp0h and the violet curve is rp1n.

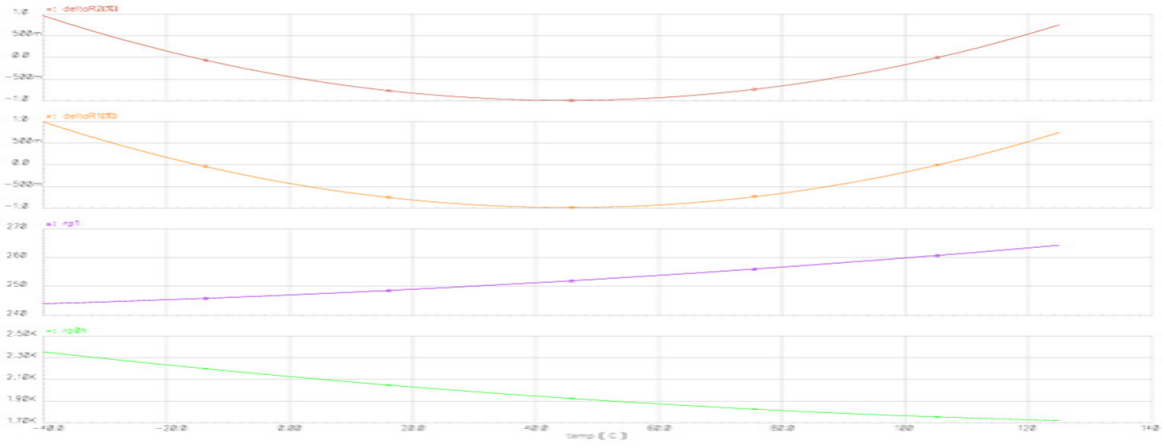

Figure 16: Compensation of the temperature variation of the resistors R_1 and R_2

The output frequency variation is less than ±1.5% over temperature with real comparators, real OTAs, real switches, real resistors and real capacitors.

3.1.3.3 Calculation of R_1, R_2 and C

The output frequency of the relaxation oscillator at a certain voltage reference v_{ref} is defined by the resistors R_1, R_2 and the capacitance C. The parasitic resistance and the parasitic capacitance are neglected to simplify the following calculations.

All the following calculations are shown for *side a*. They are the same for *side b*, except the constant terms.

The capacitor C_a gets charged by the resistors R_{1a} and R_{2a} as described in equation (14). The discharging of the capacitance C_a is done by resistor R_{1a} and is depicted in formula (15).

$$v_{osca1}(t) = v_{dd}\left(1 - e^{-\frac{1}{(R_{1a}+R_{2a})C_a}t}\right) \quad (14)$$

$$v_{osca2}(t) = v_{dd}\left(1 - e^{-\frac{1}{(R_{1a}+R_{2a})C_a}\frac{T}{2}}\right)e^{-\frac{1}{R_{1a}C_a}t} \quad (15)$$

The active integrator of the voltage averaging feedback compares the dc part of the oscillating signal v_{osca} with the voltage reference v_{refa}, shown in formula (16) with $R_1=R_{1a}=R_{1b}$, $R_2=R_{2a}=R_{2b}$ and $C=C_a=C_b$. The factor α is defined in (17). Equation (18) is the result of (16) and shows that the periodic time of the signal is just defined by the resistors R_{1a}, R_{2a}, C_a and the factor

$$\int_0^{\frac{T}{2}} v_{osca1}(t)dt + \int_0^{\frac{T}{2}} v_{osca2}(t)dt = \alpha v_{dd} T \quad (16)$$

$$\alpha = \frac{v_{ref}}{v_{dd}} \quad (17)$$

$$\underbrace{1 - e^{-\frac{1}{(R_1+R_2)C}\frac{T}{2}} + \frac{R_1}{R_1+R_2}\left(1 - e^{-\frac{1}{(R_1+R_2)C}\frac{T}{2}}\right)\cdot\left(e^{-\frac{1}{R_1 C}\frac{T}{2}} - 1\right)}_{Y2} = \underbrace{\frac{T\left(\frac{1}{2}-\alpha\right)}{(R_1+R_2)C}}_{Y1} \quad (18)$$

The easiest way to solve the implicit equation (18) is the graphical way, depicted in Figure 17. The intersection of the two curves delivers the solution of the time constant $(R_1+R_2)C$. The value of the capacitor C can be chosen. There is a lower limit due to parasitic capacitances on a chip that affect the output frequency and the accuracy. The resistance of (R_2+R_1) has to be larger than the resistance of R_1, because the discharging time of the capacitor C has to be shorter than the charging time. The value of resistor R_1 has to be much larger than the on-resistance of the NMOS switch.

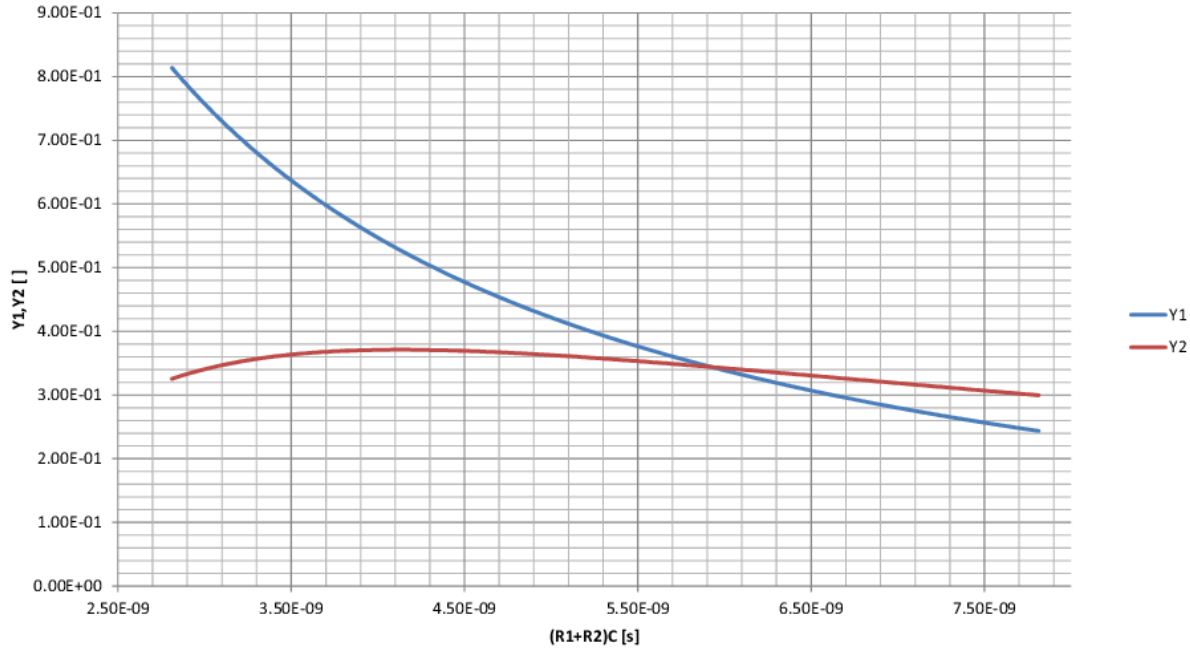

Figure 17: Graphic calculation of $(R_1+R_2)C$ for T=1/100MHz and α=0.25

$$\alpha = \frac{1}{2} - \frac{(R_1+R_2)C}{T}\left[1 - e^{-\frac{T}{2(R_1+R_2)C}} + \frac{R_1}{R_1+R_2}\left(1 - e^{-\frac{T}{2(R_1+R_2)C}}\right)\cdot\left(e^{-\frac{\frac{R_1+R_2}{R_1}T}{2(R_1+R_2)C}} - 1\right)\right] \quad (19)$$

The required divider ratio *α* for a constant *$(R_1+R_2)C$* is calculated in equation (19). The equation (19) is calculated by equation (18). The behaviour of *α* over the frequency is depicted in Figure 18.

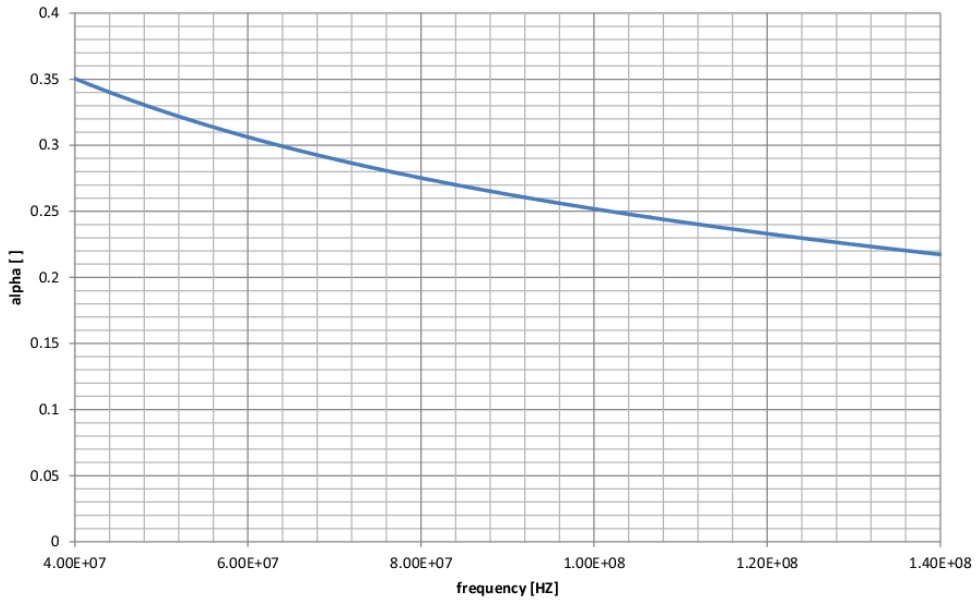

Figure 18: Divider ratio α over the output frequency with constant *$(R_1+R_2)C$*

3.1.3.4 Sizing of the switches

MOS switches are not ideal switches. Their on-resistance and capacitance have a large variation over the voltage range and over temperature.

The size of the switches $S_{2a,b}$ is easy to determine via parametric simulation, their on-resistance has to be smaller than 1% of the sum of the resistors $R_{1a,b}$ and $R_{2a,b}$. The variation of the on-resistance of the switch has just a small effect on the output frequency.

The size of the switches $S_{1a,b}$ is a compromise between a small resistance and a small capacitance. A large parasitic capacitance affects the time determining capacitances $C_{a,b}$, a large on-resistance affects the discharging time, which in turn affects the output frequency. The sizes of the switches are determined by a parametric analysis. The sizes with the smallest effects to the output frequency over the temperature range from -40°C to +125°C were chosen.

3.1.3.5 Sensitivity to reference

It is very important to know how a variation of the reference affects the output frequency. In [1] the sensitivity to reference is defined as equation (20). This describes the effects of a variation of the divider ratio on the output frequency. For the new topology this sensitivity is shown in equation (21). The definitions of the variables *n*, τ and α are shown in (22), (23) and (19), respectively.

$$\left(\partial T \middle/ T\right) \middle/ \partial \alpha \quad (20)$$

$$\frac{\partial T}{T} = \frac{1}{\frac{1}{2}\left(1-e^{-\frac{T}{2\tau}}\right)e^{-\frac{nT}{2\tau}} + \frac{1}{2n}\left(1-e^{-\frac{nT}{2\tau}}\right)e^{-\frac{T}{2\tau}} - \frac{1}{2}e^{-\frac{nT}{2\tau}} + \left(\frac{1}{2}-\alpha\right)} \quad (21)$$

$$n = \frac{R_1 + R_2}{R_1} \quad (22)$$

$$\tau = (R_1 + R_2)C \quad (23)$$

The equation (21) is plotted in Figure 19. The sensitivity is a bath tube curve with a minimum of 9.04 detected at α=0.324.

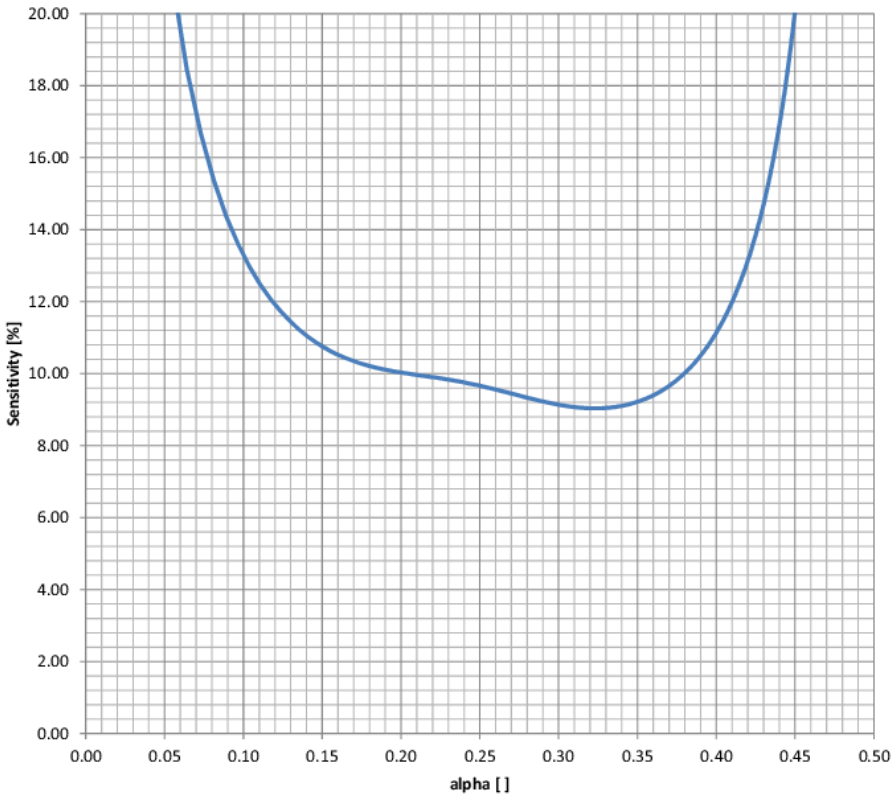

Figure 19: Sensitivity to reference

This means that a variation of the ratio *α* has the smallest effect on the output frequency when α=0.324.

Since the topology has a high sensitivity to *α, α* has to be constant over the temperature range from -40°C to +125°C. Otherwise the output frequency will vary by 9,04% if *α* varies by 1% at a nominal *α*=0.324. A stable output frequency requires a constant *α*.

For the implementation *α=0.25* was chosen. This divider ratio is not the one where the circuit is least sensitive to the divider ratio but there is just a little difference in sensitivity between a divider ratio *α=0.2 and α=0.37.*

3.1.3.6 Trimming

Resistors and capacitors have a large spread of about ±20% over the process. To reach an accuracy of ±1%, these tolerances must be compensated with trimming. The trimming circuit is not implemented because it is out of scope.

For the chosen topology, the trimming can be done via the voltage references v_{refa} and v_{refb}. The easiest solution for a trimming circuit is a variable voltage divider. But this does not take into consideration the temperature coefficient of the oscillator which also has to be trimmed.

A possible circuit is shown in Figure 20. The trim stage delivers a stable voltage proportional to supply. That circuit also considers a first order temperature compensation.

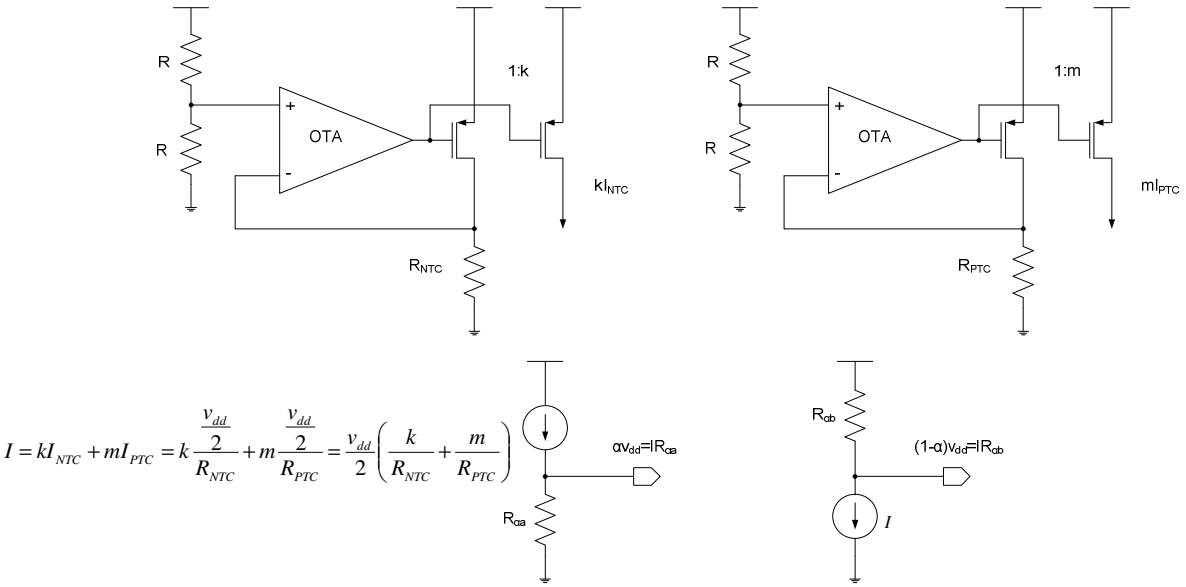

Figure 20: Concept of a possible circuit to trim the oscillator

The currents are dependent to the supply. Now the voltage reference is dependent on the supply. The oscillator topology is independent to the supply when the voltage reference is a proportional ratio of the supply. That means that a variation of the supply does not affect the output frequency.

To compensate the temperature drift of the oscillator circuit, a first order temperature compensation is possible. That is possible through a combination of the NTC current and the PTC current.

3.2 Sub blocks circuit design

3.2.1 Comparator

The chosen topology needs two different comparators. One with a PMOS input stage and one with an NMOS input stage, because *side a* and *side b* have different operation points. *Side a* refers to ground and *side* b refers to the supply.

The comparator has to change its output in a certain time. This is specified as the propagation delay. A parametric simulation detects the required propagation delay. The chosen topology needs comparators, which change their outputs in a fourth of the desirable time reference. A variation of the delay time is compensated by the control loop. The offset of the comparator is also compensated by the control loop. These two facts relax the comparator design.

To detect the requirements of the comparator the following calculations are made. The required unity gain frequency of the comparator is detected on the following sides.

3.2.1.1 Definition of requirements of a OTA based comparator

A comparator can be interpreted as a linear time invariant system and can be described with a transfer function. A model of a transmission scheme is depicted in Figure 21. The input signal is a slope and is described with equation (24) at the time domain and with (25) at the frequency domain [10][11]. The transfer function of the comparator is defined in formula (26).

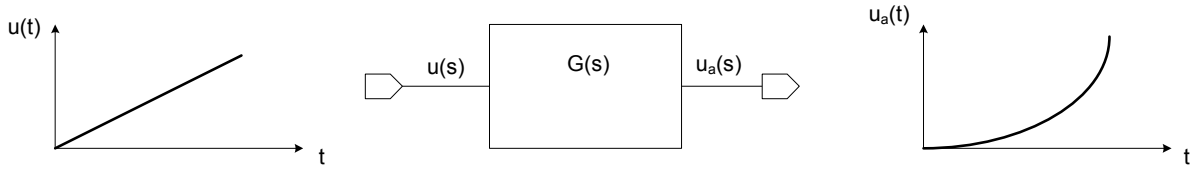

Figure 21: Model of transmission scheme

$$u(t) = slope \cdot t \quad (24)$$

$$u(s) = \frac{slope}{s^2} \quad (25)$$

$$G(s) = \frac{A_0}{1 + \frac{sA_0}{\omega_T}} \quad (26)$$

The output of the comparator is calculated with equation (27) in the s-domain. This form of the equation is not well suited for the inverse Laplace transform. With a partial fraction expansion the equation (27) is extended to equation (28).

$$u_a(s) = u(s) \cdot G(s) = slope \cdot A_0 \left(\frac{1}{s^2} \frac{1}{1 + \frac{sA_0}{\omega_T}} \right) \quad (27)$$

$$u_a(s) = slope \cdot A_0 \left[\frac{1}{s^2} - \frac{\frac{A_0}{\omega_T}}{s} + \frac{\left(\frac{A_0}{\omega_T} \right)^2}{1 + \frac{A_0 s}{\omega_T}} \right] \quad (28)$$

Equation (28) is transformed with the inverse Laplace transform in the time domain. The inverse Laplace transform delivers the equation (29).

The equation (29) is hard to solve analytically because there is a linear term and an exponential term. The exponential term is approximated with a Taylor series, depicted in equation (30). The result of this approximation is depicted in equation (31) and in Figure 22.

$$u_a(t) = slope \cdot A_0 \left[t + \frac{A_0}{\omega_T} \left(e^{-\frac{\omega_T}{A_0} t} - 1 \right) \right] \quad (29)$$

$$e^x = 1 + \frac{x}{1!} + \frac{x^2}{2!} \quad (30)$$

$$u_a(t) = slope \cdot \frac{t^2}{2} \omega_T \quad (31)$$

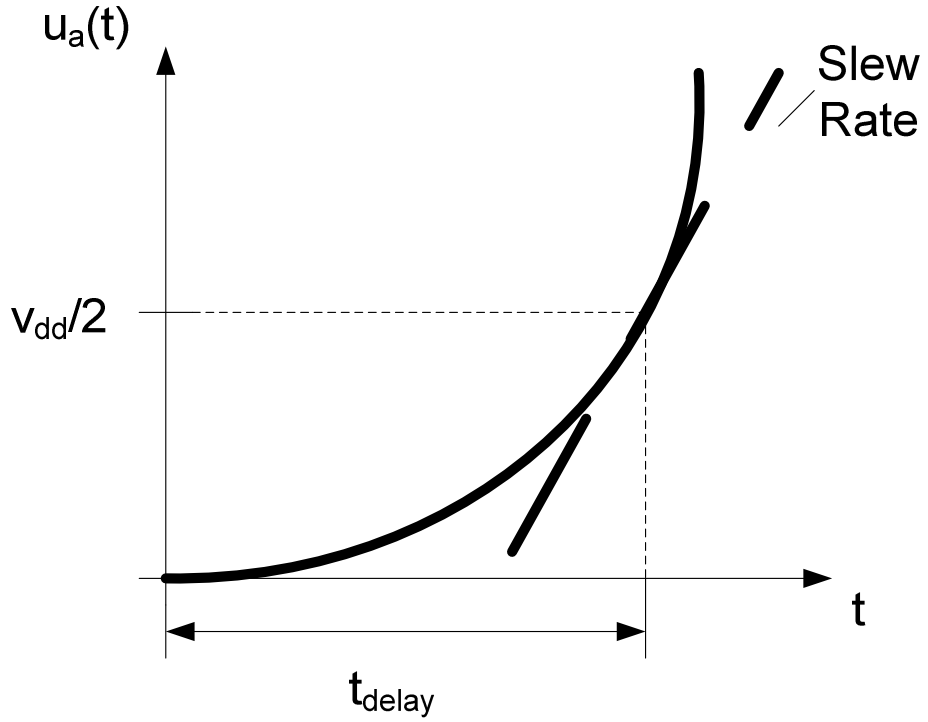

Figure 22: Output signal $u_a(t)$ of the comparator

The output signal is proportional to the input slope and the unity gain. The necessary unity gain frequency, to move the output to a certain voltage within a required time, is calculated by equation (32).

$$\omega_T = \frac{2u_a(t)}{slope \cdot t^2} \quad (32)$$

As shown in Figure 22, the interesting voltage is the half of the supply. The comparator needs the time t_{delay} to reach this voltage. Equation (33) and equation (34) define the needed unity gain frequency ω_T or f_T to reach $v_{dd}/2$ in the required time t_{delay}.

$$\omega_T = \frac{v_{dd}}{slope \cdot t^2_{delay}} \quad (33)$$

$$f_T = \frac{v_{dd}}{slope \cdot 2\pi t^2_{delay}} \quad (34)$$

The needed unity gain frequency is proportional to $1/t^2$ and proportional to *1/slope*, this relation is depicted in Figure 23.

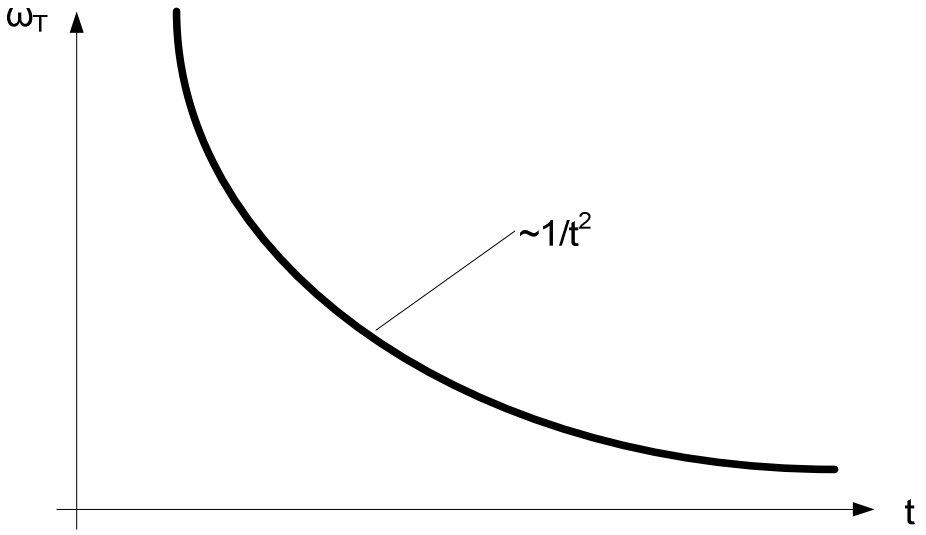

Figure 23: Unity gain frequency over time

The needed Slew Rate *SR of the OTA was to be larger than* SR_{min} *defined in* (35).

$$SR_{\min} = \sqrt{v_{dd} \cdot slope \cdot \omega_T} \quad (35)$$

The unity gain frequency also is defined by equation (36) and shows that the *unity gain frequency* f_T is the same as the *gain bandwidth product GBW* and this is proportional to the square root of the current.

$$f_T = GBW = \frac{g_m}{C_L} = \frac{\sqrt{2I_D k' \frac{W}{L}}}{C_L} \quad (36)$$

A result of that calculations is, that to halve the delay time t_{delay} of the OTA based comparator a four times larger gain bandwidth product is required and that further requires a 16 times larger current consumption of the OTA based comparator.

OTA based comparators achieve short delay times just with steep slopes or a huge current consumption.

Equation (37) shows the required unity gain frequency for the oscillator.

$$f_T = \frac{v_{dd}}{2\pi \cdot slope \cdot t^2{}_{delay}} = \frac{3.3V}{2\pi \cdot 500M\frac{V}{s} \cdot (1.5\ ns)^2} = 467MHz \quad (37)$$

3.2.1.2 Implementation

The design of the two comparators is relaxed, because the input signals have a very steep slope, shown in equation (34). This is the reason, why a low power design is possible. The comparator delay must be less than about a fourth of the periodic time *T* over all process and temperature corners. This specification is a result of the parametric simulations with the Verilog-AMS models. The offset will be compensated by the control loop. With this specification, it is shown that a standard comparator topology is sufficient. The PMOS input comparator is depicted in Figure 24.

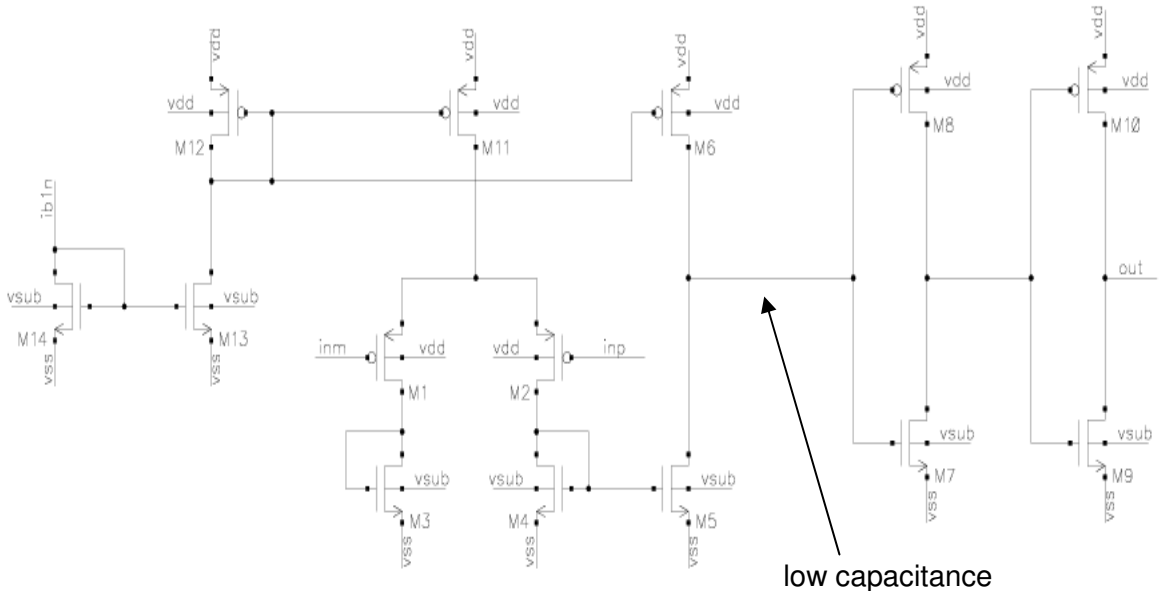

Figure 24: Comparator with PMOS input stage

The comparator consists of a differential input pair, which works against a current source. The transistors M_1 and M_2 compose the differential input pair. Transistor M_6 is the current source, M_4 and M_5 compose a current mirror and the transistors M_7 to M_{10} compose an output buffer. Transistor M_3 is needed so that M_1 and M_2 both see the same load. The other transistors are responsible for the biasing of the circuit.

As long as the voltage at in_m is less than the voltage at in_p, the whole tail current flows through transistor M_1, and M_2 is blocked. That causes that M_5 is also blocked and furthermore a HIGH output signal.

When the voltage at in_m is greater than the voltage at in_p, the whole current flows through transistor M_2 and the transistor M_5 pulls the output of the comparator to ground and the output signal changes to LOW.

The reason to use a current source at the output stage is, that the comparator also works when $v_{ca}(in_m)$ is pushed up to supply voltage v_{dd}. If $v_{ca}(in_m)$ is pushed up to v_{dd} the oscillating

signal $v_{osca}(in_p)$ rises up to v_{dd} and if the input in_m rises up to supply voltage minus a transistor threshold v_{th}, the current source pushes up the output of the comparator *out* to HIGH, depicted in Figure 25.

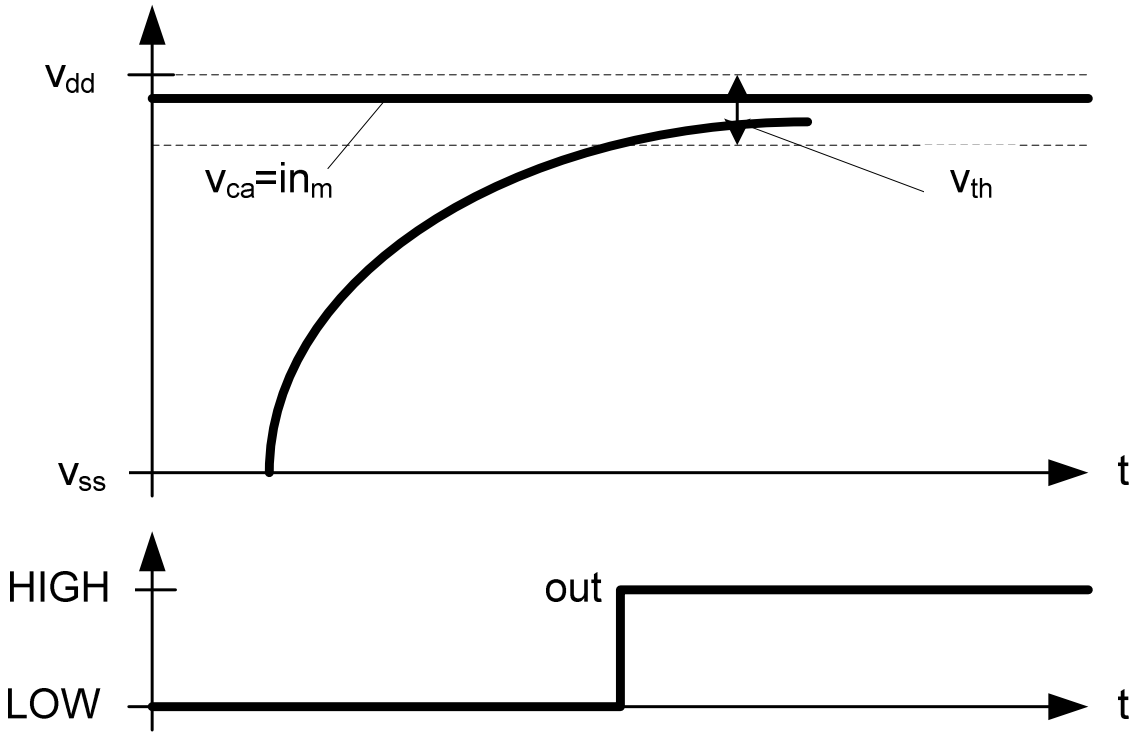

Figure 25: Waveform of the signal of the comparator with PMOS input stage

The NMOS input comparator works the same way but certainly in the other direction. This is the reason that the NMOS input comparator has an inverter as output stage. The comparator with NMOS input stage is shown in Figure 26.

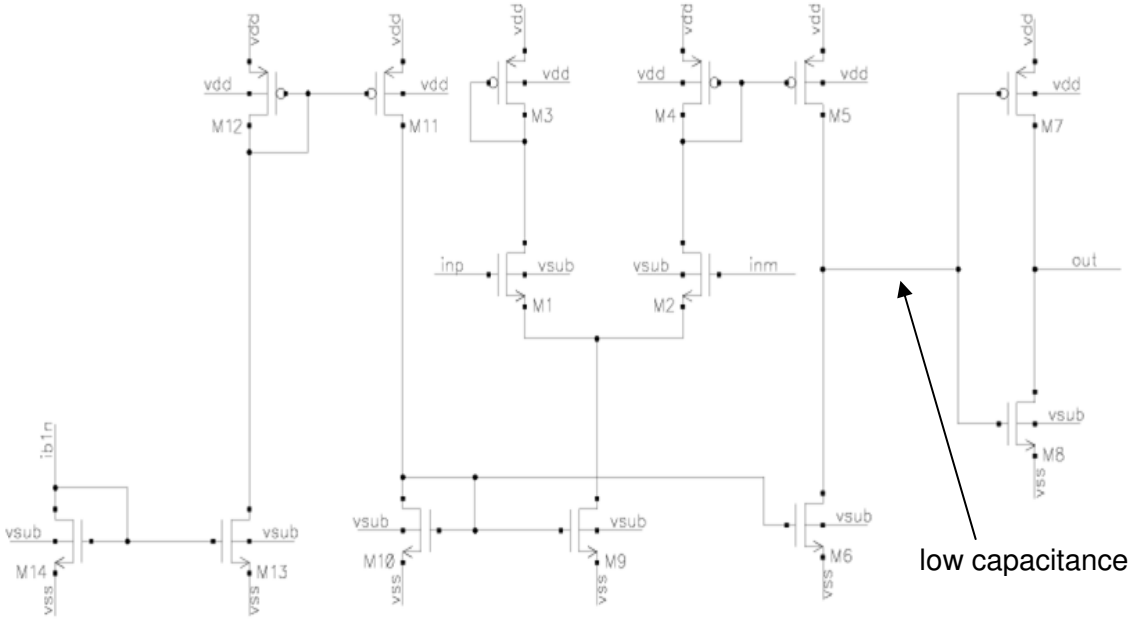

Figure 26: Comparator with NMOS input stage

Both comparators together consume less than 100µA and have a propagation delay of about 1.5ns.

3.2.2 OTA

The chosen topology needs two different OTAs, one with a PMOS input stage and one with an NMOS input stage, because the voltage reference at the input of the OTA at *side a* is always smaller than $v_{dd}/2$ and the voltage reference at side b is always larger than $v_{dd}/2$. That causes different input common mode ranges.

3.2.2.1 Definition of requirements

The OTA is used as a continuous time, active integrator in the control loop. The control loop is shown in Figure 27. Two conditions have to be fulfilled. These conditions are depicted in equation (38) and equation (39).

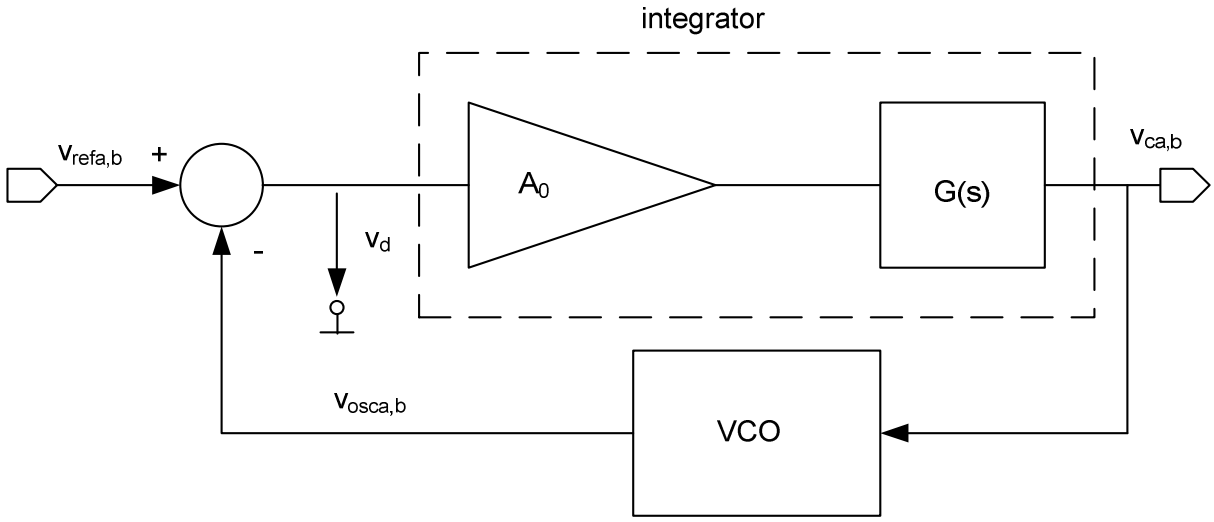

Figure 27: Control loop

$$v_d(f) = 0 \quad for\ f \leq f_{vosca,b} \quad (38)$$

$$v_c(f) = 0\ for\ f \geq f_{vosca,b} \quad (39)$$

The integrator is depicted in Figure 28. The active integrator generates the threshold of a comparator. The threshold v_c of the comparator has to be constant. This is the reason why the oscillator frequency and its harmonics have to be attenuated. These input signals must not to affect the output signal.

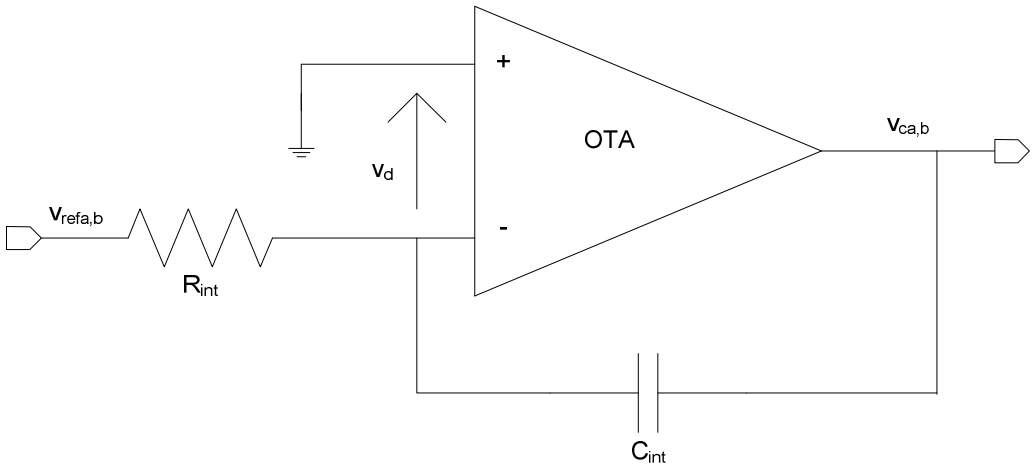

Figure 28: Continuous time integrator

The positive input of the OTA is always the stable voltage reference and is considered to be at AC ground in the following frequency domain stability considerations. At the negative input of the OTA is a 100MHz input signal. The active integrator works like a low pass filter and attenuates the disturbances.

Equation (40) describes the circuit with the Kirchhoff's current law [12]. An ideal integrator exhibits an infinite gain and its unity gain frequency is defined by the integrator resistor R_{int} and the integrator capacitance C_{int}. The integrator resistance of R_{int} is 300kΩ and the capacitance of C_{int} is 500fF large. The used OTA has a finite gain. Hence the voltage difference v_d between its two inputs is not equal to zero. The voltage difference is defined in equation (41).

$$\frac{v_{osca,b} - v_d}{R_{\text{int}}} = -\frac{v_{ca,b} - v_d}{\frac{1}{sC_{\text{int}}}} \quad (40)$$

$$v_d = -v_{ca,b}\frac{1 + \frac{A_0 s}{2\pi\omega_T}}{A_0} \quad (41)$$

The transfer function of the integrator (42) was calculated. The simulated bode plot is shown in Figure 29. It is not easy to bring the transfer function in a standard form to get the poles and zeros by a comparison of coefficients. This is the reason to analyse it in two cases; case one $A_0 \to \infty$ and case two $\omega_T \to \infty$.

$$\frac{v_{ca,b}}{v_{osca,b}} = \frac{-A_0}{s^2\frac{C_{\text{int}}R_{\text{int}}A_0}{2\pi\omega_T} + s\left(C_{\text{int}}R_{\text{int}}A_0 + C_{\text{int}}R_{\text{int}} + \frac{A_0}{2\pi\omega_T}\right) + 1} \quad (42)$$

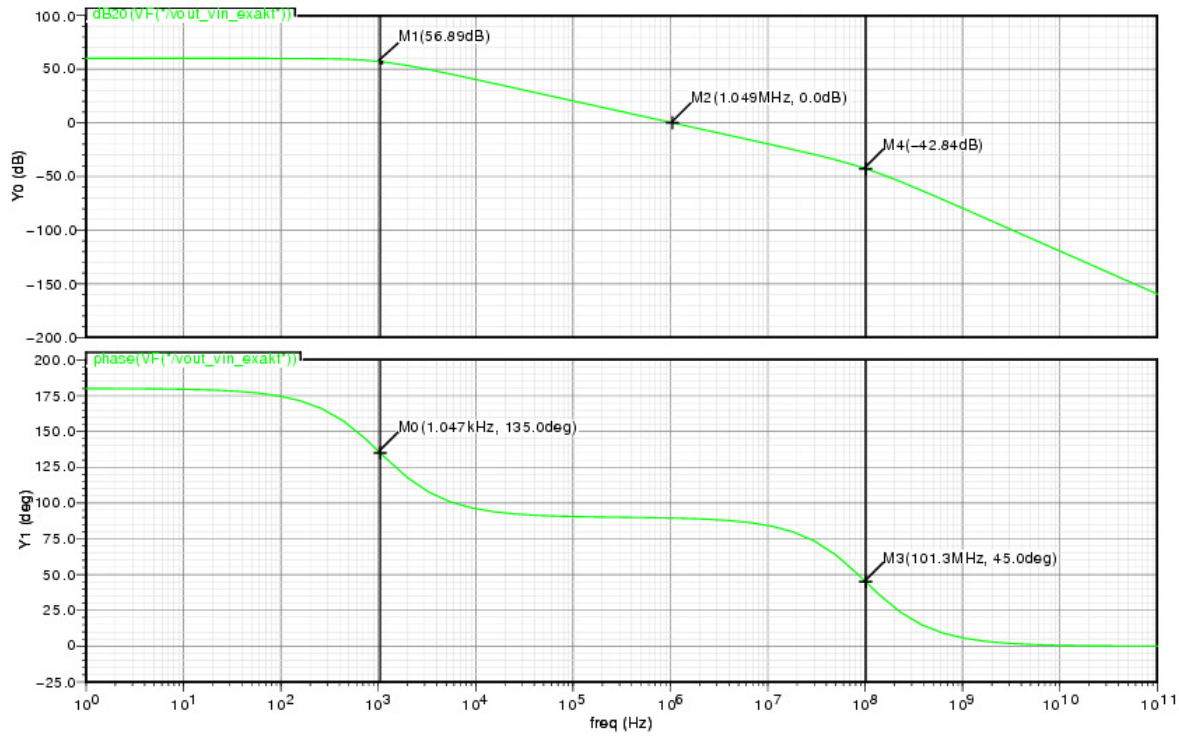

Figure 29: Simulated bode plot of the transfer function $v_{ca,b}/v_{osca,b}$ (42)

In case one, the integrator is like an ideal integrator at low frequencies with a unity gain frequency inverse of $R_{int}C_{int}$. This ideal integrator causes a phase shift of 90°. At the unity gain frequency $2\pi\omega_T$ of the OTA is a pole, which causes another phase shift of 90°. Equation (43) shows the transfer function of case 1, and Figure 30 depicts the bode plot of this case. This case describes the behaviour of the integrator at high frequency. The pole at the unity gain frequency causes of the finite bandwidth of the OTA.

$$\frac{v_{ca,b}}{v_{osca,b}} = -\frac{1}{sR_{\text{int}}C_{\text{int}}} \cdot \frac{1}{1+\frac{s}{2\pi\omega_T}} \; for\; A_0 \to \infty \quad (43)$$

In case two, the integrator is like an active low-pass filter with a cut-off frequency defined by the time constant $R_{int}C_{int}$. This case describes the behaviour for low frequency, shown in Figure 31 and equation (44).

$$\frac{v_{ca,b}}{v_{osca,b}} = -\frac{A_0}{sR_{\text{int}}C_{\text{int}}+1} for\; \omega_T \to \infty \quad (44)$$

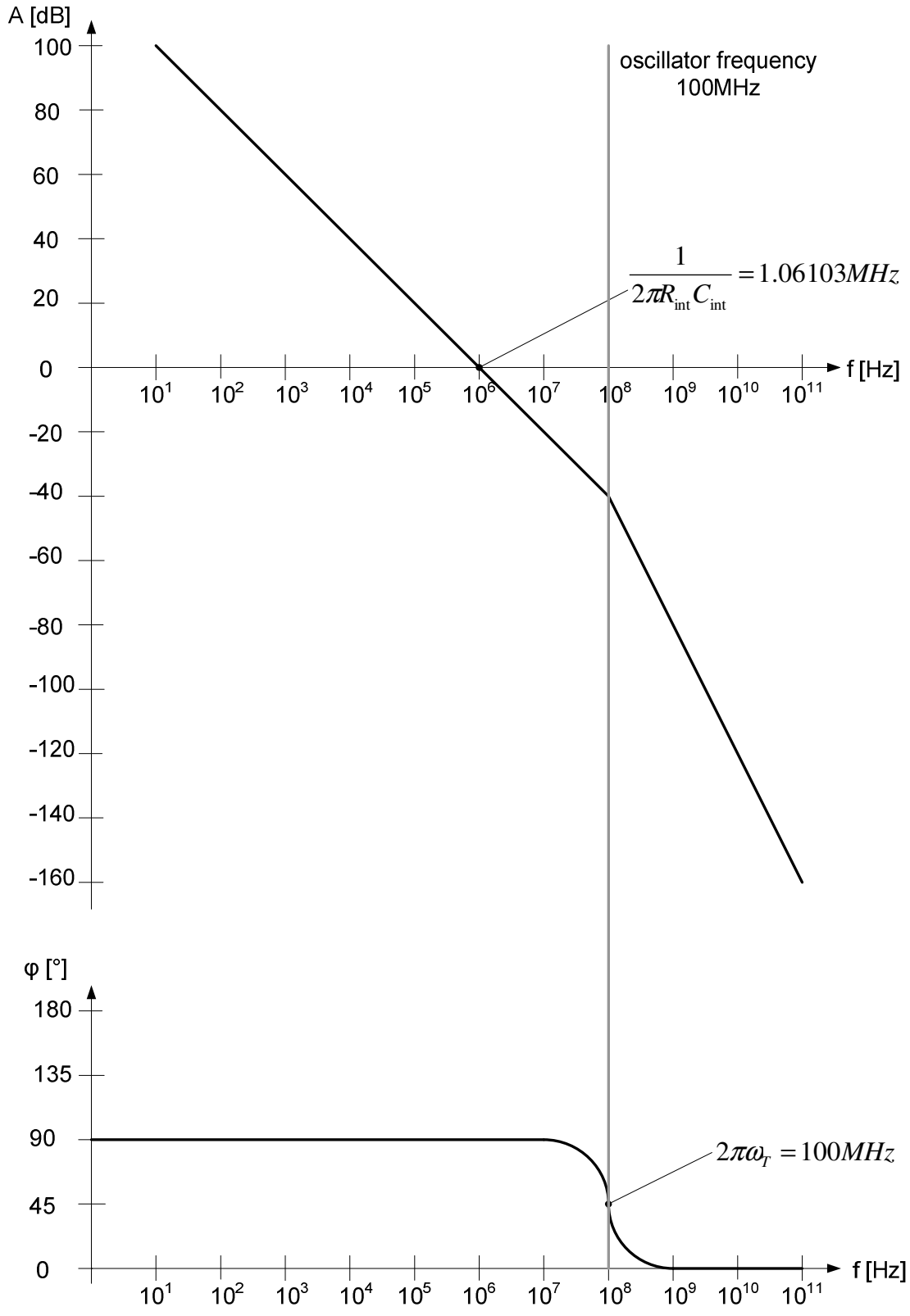

Figure 30: Bode plot of the transfer function $v_{ca,b}/v_{osca,b}$ with $A_0 \rightarrow \infty$ (43)

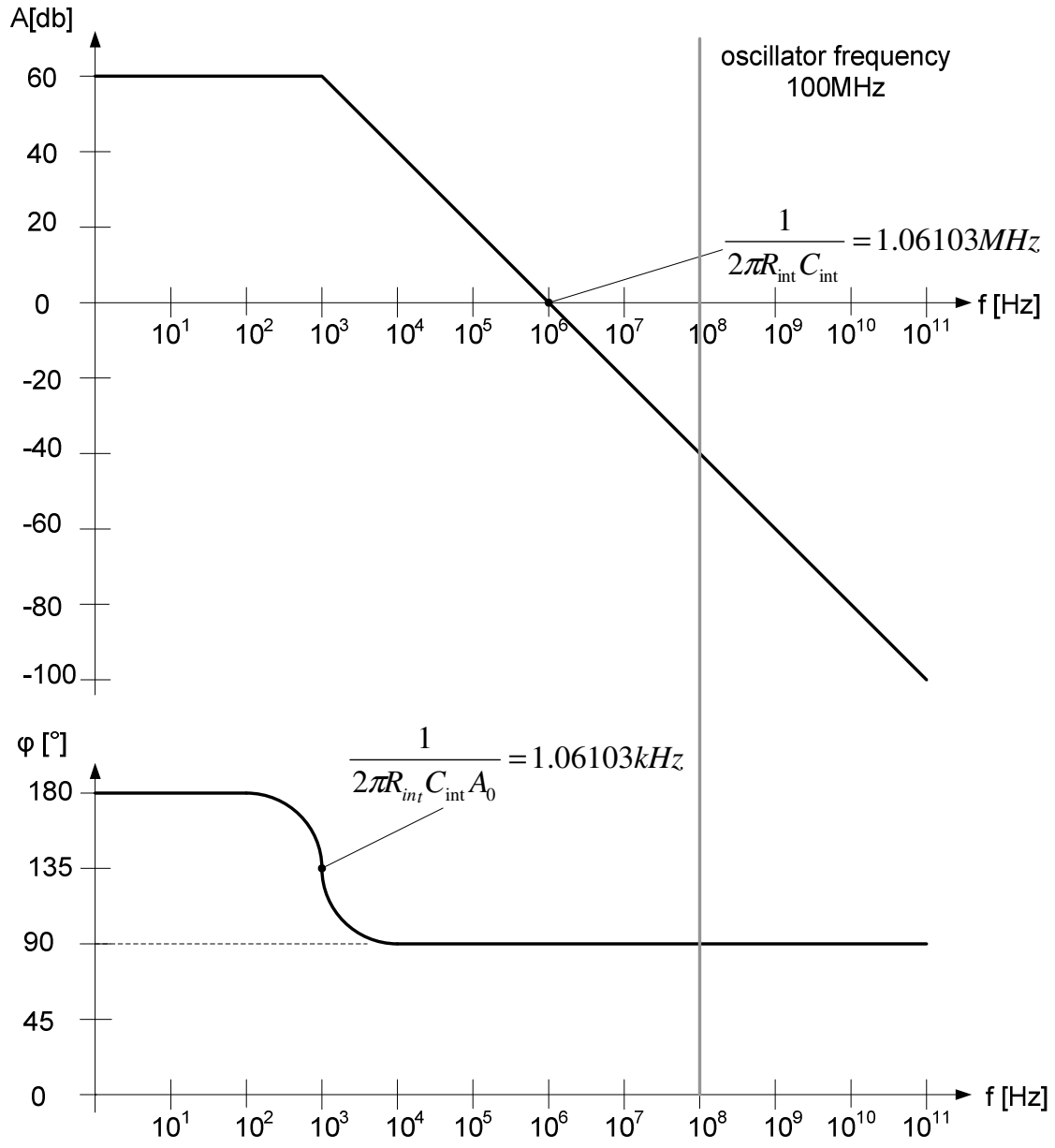

Figure 31: Bode plot of the transfer function $v_{ca,b}/v_{osca,b}$ with $\omega_T \rightarrow \infty$ (44)

The transfer function (42) can be described with these two cases. For low frequencies the integrator can be described with (44) and for high frequency with second part of (43), described in (45) and depicted in the bode plots in Figure 32 and Figure 33.

$$\frac{v_{ca,b}}{v_{osca,b}} = -\frac{A_0}{sR_{\text{int}}C_{\text{int}} + 1} \cdot \frac{1}{1 + \frac{s}{2\pi\omega_T}} \quad (45)$$

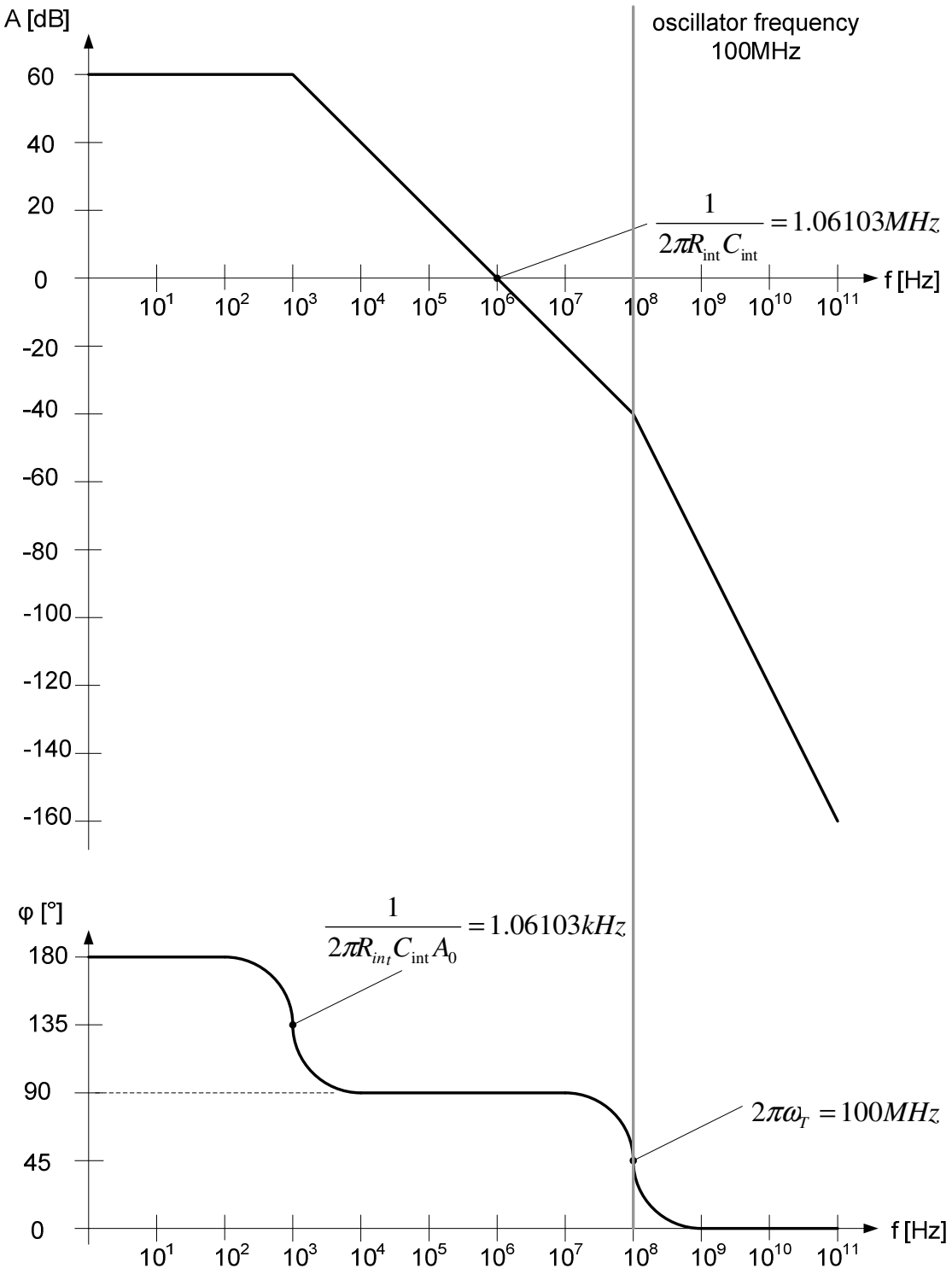

Figure 32: Bode plot of simplification of the transfer function $v_{ca,b}/v_{osca,b}$ (45)

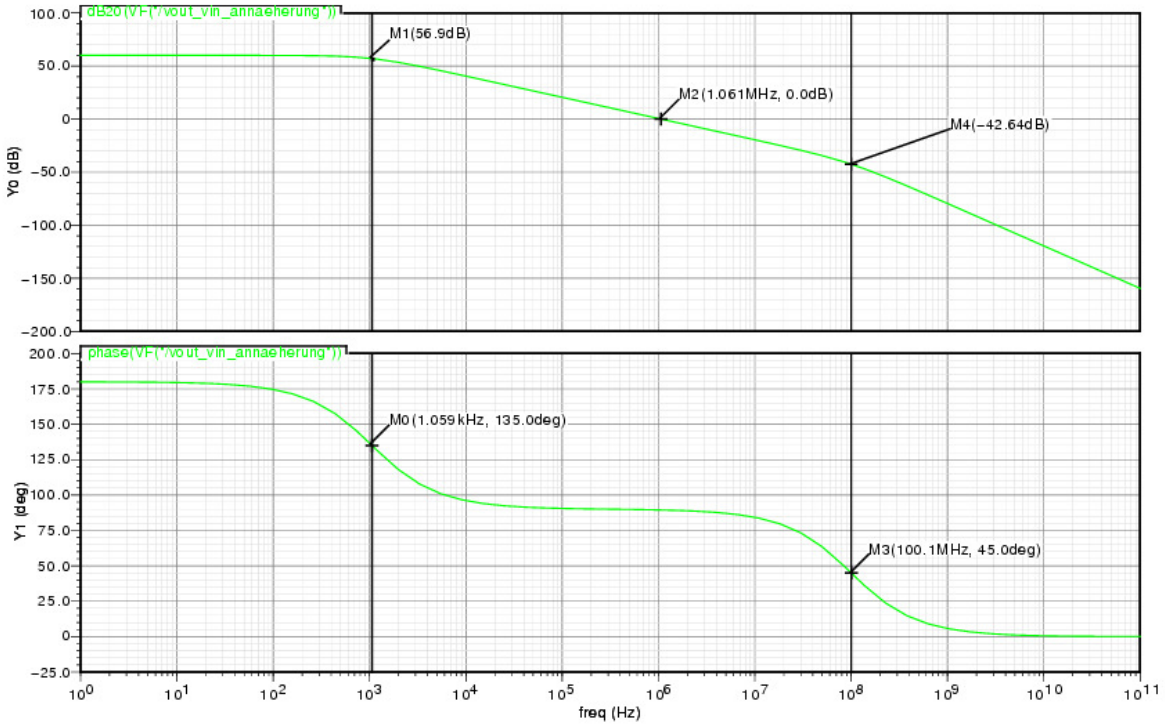

Figure 33: Simulated bode plot of simplification of the transfer function $v_{ca,b}/v_{osca,b}$ (45)

The behaviour of the voltage difference v_d between the inputs has to be analysed in order to ensure that equation (41) is satisfied. The transfer function $v_d/v_{osca,b}$ gets defined by formula (46) and the bode plot depicted in Figure 34 and Figure 35.

$$\frac{v_d}{v_{osca,b}} = -\frac{1}{1+sA_0R_{\text{int}}C_{\text{int}}} \cdot \frac{1+\frac{A_0 s}{2\pi\omega_T}}{1+\frac{s}{2\pi\omega_T}} \quad (46)$$

The bode plot shows the requirements of the OTA to attenuate the oscillator frequency and its harmonics of the input signal. Up to the first pole $1/(2\pi A_0 R_{int} C_{int})$ no suppression of the input noise is achieved, then the input signal attenuates with 20dB/decade up to the zero at $(2\pi\omega_T)/A_0$, defined by ω_T and A_0. The attenuation does not increase up to ω_T. For higher frequency than ω_T the attenuation increases with 20dB/decade.

High output ripple attenuation needs a large time constant $R_{int}C_{int}$, a high gain, larger than 60 dB and a high unity gain frequency like 100 MHz. The OTA has to be stable, which requires a phase margin of greater than 55°.

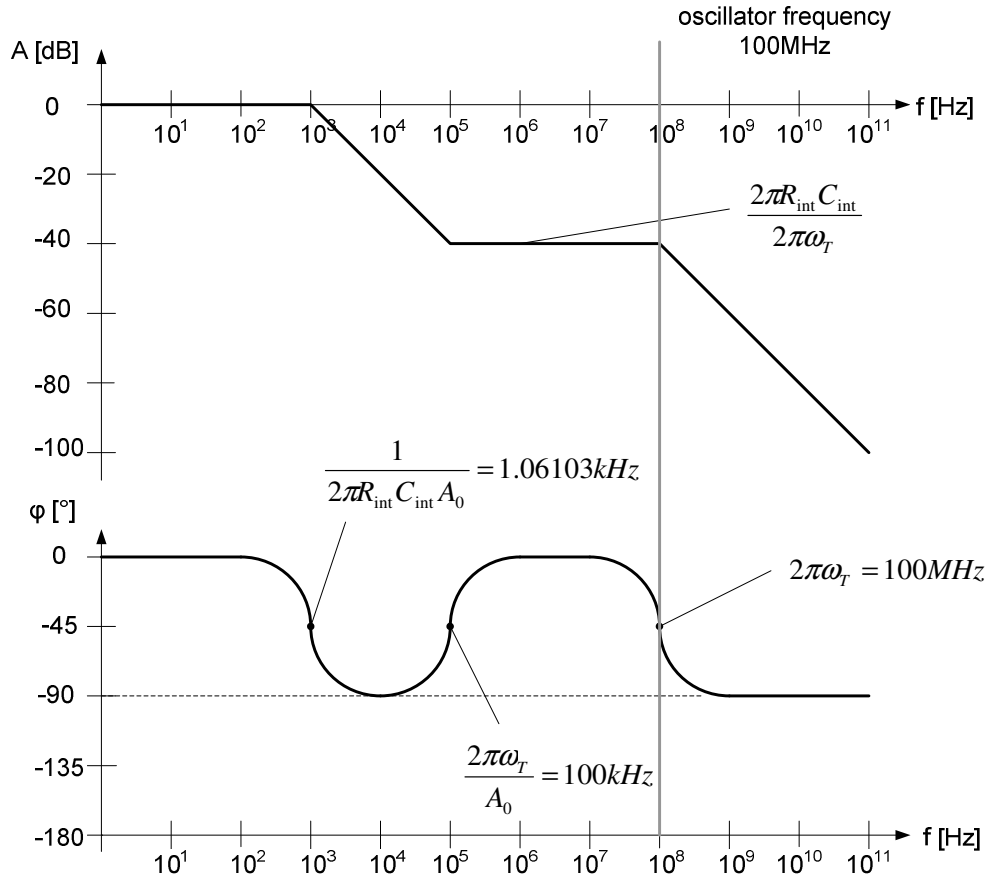

Figure 34: Bode plot of the transfer function $v_d/v_{osca,b}$ (46)

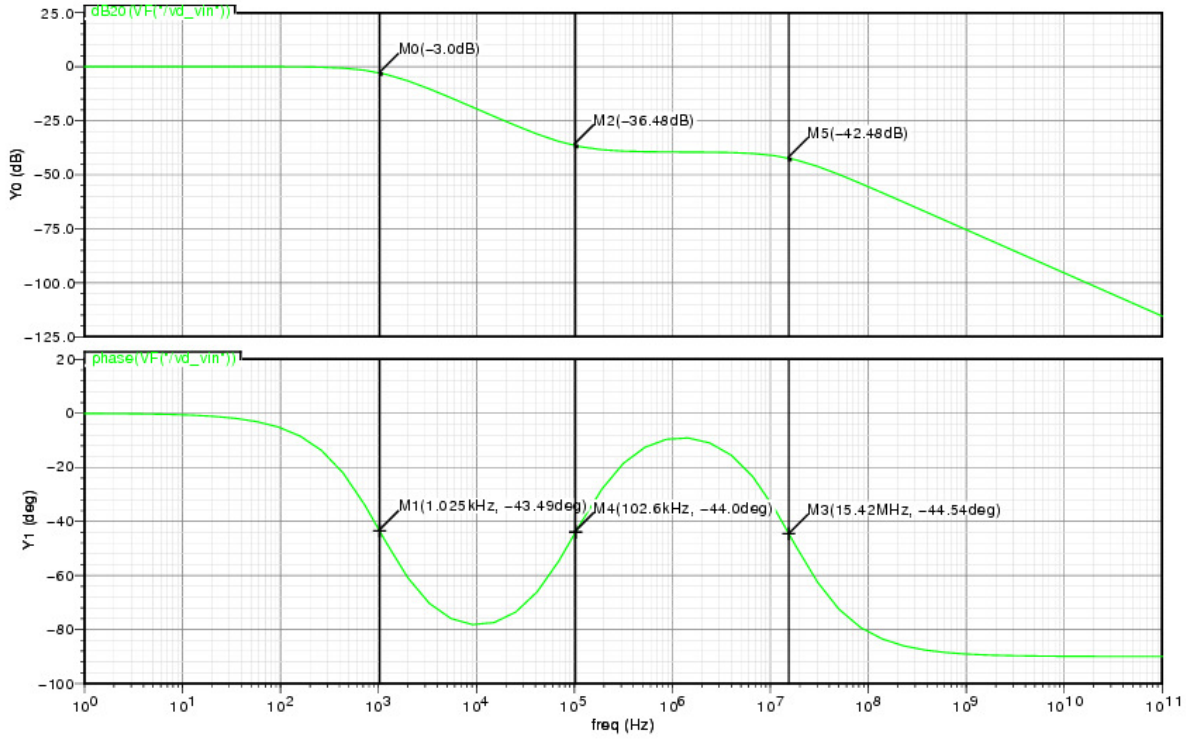

Figure 35: Simulated bode plot of the transfer function $v_d/v_{osca,b}$ (46)

3.2.2.2 Implementation as folded cascode OTA

On the test chip, two different oscillators are placed. The only difference between them lies in the OTA topologies of the integrators. The first comprises two folded cascode OTAs and the second comprises two two-stage amplifiers with a telescopic OTA as first stage and a common source stage at the output stage [7][8].

The current gain OTA, the telescopic OTA and the Miller OTA do not reach a phase margin of 40° at unity gain frequency of 100 MHz. The telescopic OTA has a too small output range for the needed operation point. So a folded cascode circuit was chosen. The PMOS input folded cascode OTA is depicted in Figure 36.

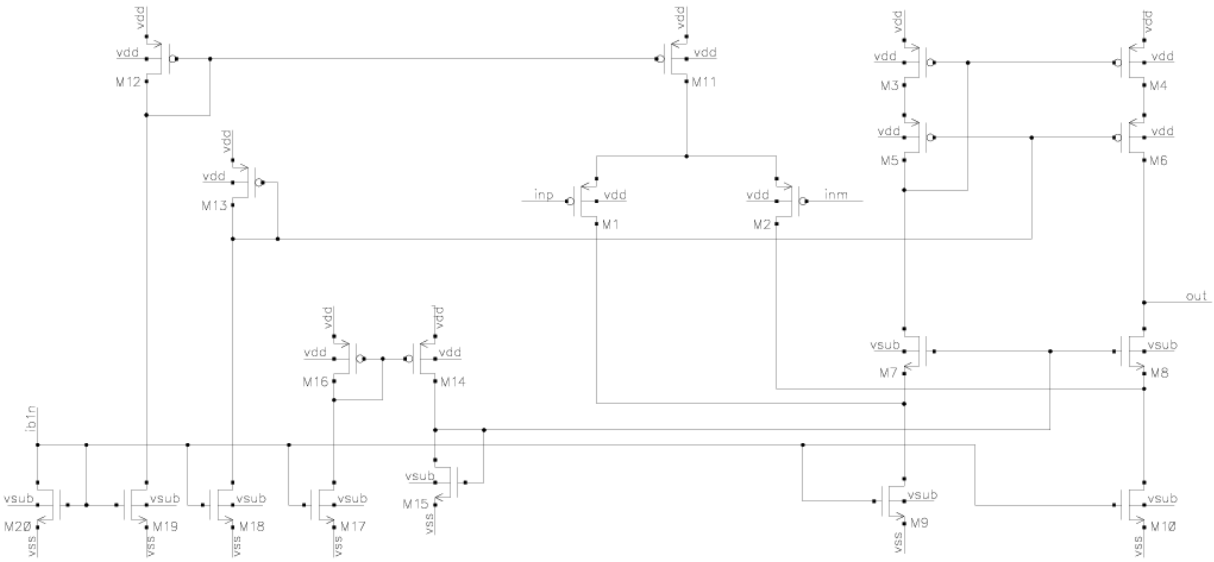

Figure 36: Folded cascode OTA with PMOS input

The folded cascode OTA consists of an input differential pair, transistors M_1 and M_2 in Figure 36, two cascode transistors M_7 and M_8 and a high-swing current mirror, M_3 to M_6. The circuit is completely symmetric, and both inputs see the exact same DC voltage and impedance. The output is the only high resistive point of the circuit.

The advantages of the folded cascode OTA are high unity gain frequency, high phase margin and the input transistors can operate to the supply rail.

The disadvantage of this topology is a high current consumption, i.e. about twice as much as that of a telescopic OTA.

The both folded cascode OTAs consume together 280µA and this is more than a third of the current consumption of 730µA of the whole oscillator.

The implemented NMOS input folded cascode OTA is depicted in Figure 37.

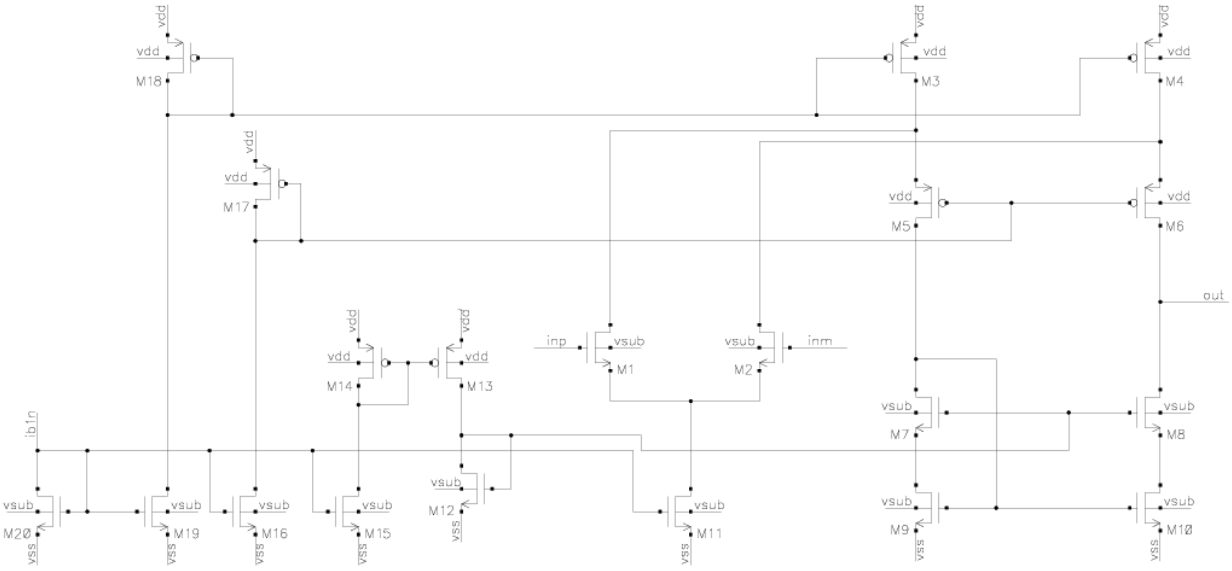

Figure 37: Folded cascode OTA with NMOS input

3.2.2.3 Implementation as two stage OTA

A higher DC gain is achieved with a two stage OTA. The unity gain frequency is defined by the compensation capacitance and the stability is determined by the load capacitor [13]. The current consumption of the implemented two stage amplifier is less than the consumption of the folded cascode OTA. The current consumption is about half of the folded cascode OTAs.

A telescopic OTA is used as first stage and a common source stage is used as a second stage. The PMOS input OTA is shown in Figure 38.

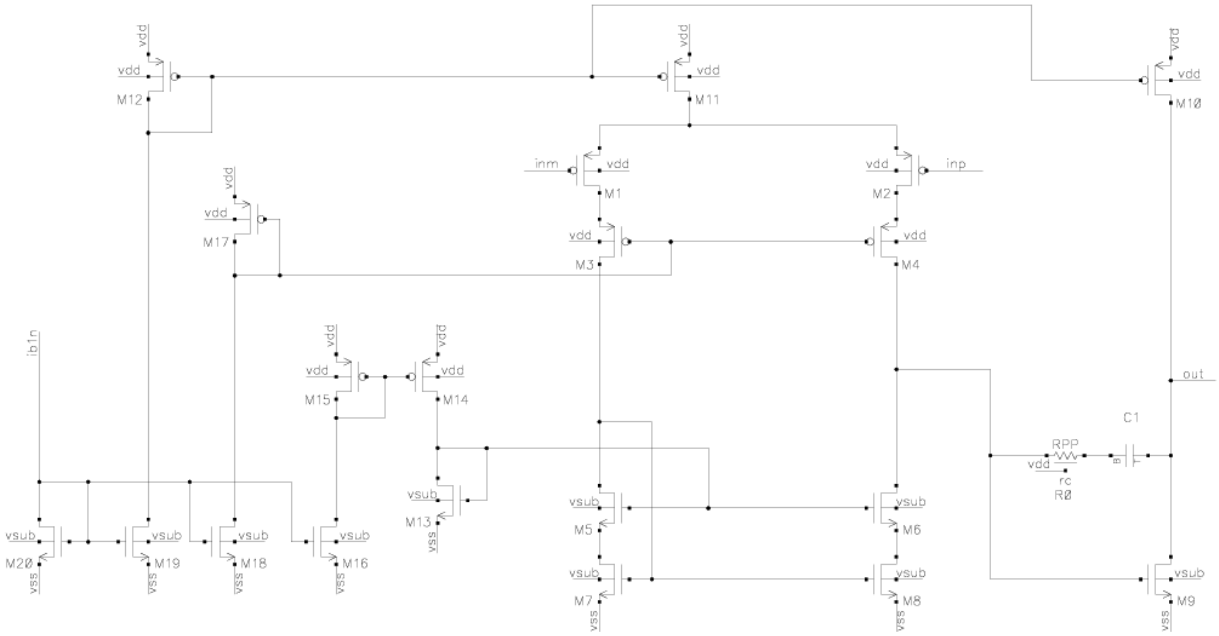

Figure 38: PMOS input two stage amplifier with a telescopic OTA and a common source stage

The telescopic OTA consists of one differential input pair, transistor M_1 and M_2 in Figure 38, two cascode transistors, M_3 and M_4, and one high-swing current mirror, transistors M_5 to M_8.

Between the first stage, the telescopic OTA, and the second stage, the common source stage, a pole-zero compensation is placed. This compensation is needed to ensure stability.

Telescopic OTAs are not as frequently used as folded cascode amplifiers, because the output swing of the telescopic OTAs is reduced by the overdrive voltages of the cascode transistors. The input common mode range is limited by the bias voltage of the cascode transistors. The OTA is not symmetric, i.e. the input transistors see different loads. The current consumption is acceptable and less than a folded cascode OTA.

Both two stage OTAs consume together 150µA and this is less than a third of the current consumption of 540µA of the whole oscillator.

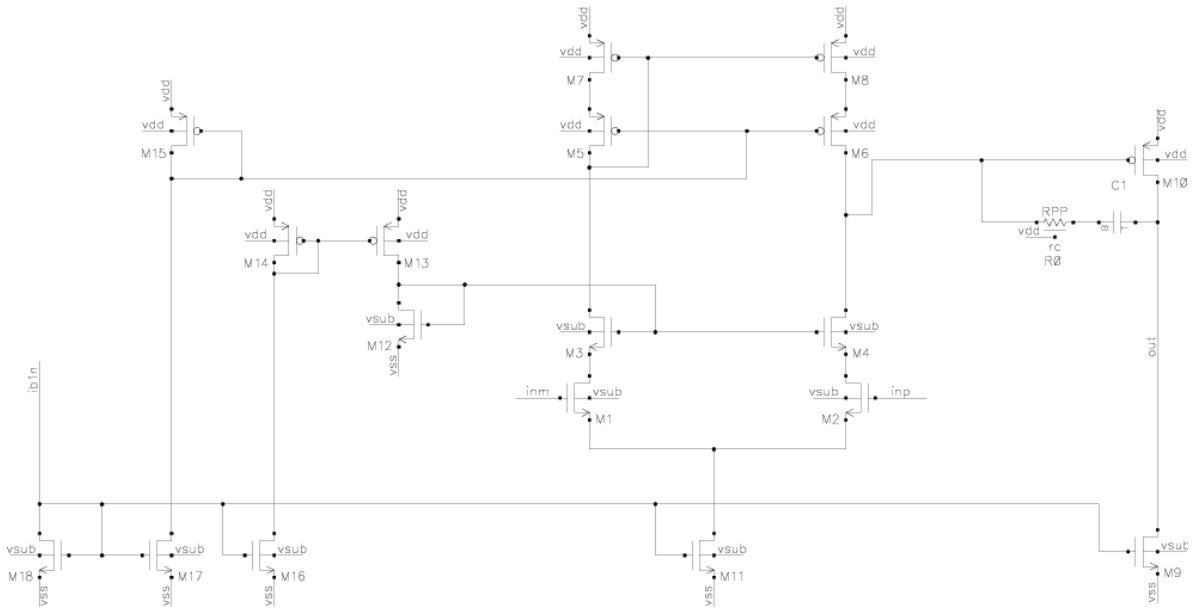

Figure 39: PMOS input two stage amplifier with a telescopic OTA and a common source stage

3.3 Layout

The layout was done by an employee at Dialog Semiconductors.

The layout of integrated circuits requires a precise planning. And therefore the layout planning has to be considered thoroughly [14]. Every block needs a certain area. This area has to be optimized to a minimum to reduce the costs. The layout adds parasitic capacitances and resistances to the designed circuits. The added parasitic capacitances and resistances have to be minimized in order not to affect the functionality of the designed circuit. The interconnections have to be optimized to minimize the parasitic capacitances and resistances.

The layout also contains the ring of bond pads. The pads are required to connect the circuit with external parts and external signals, like supply, ground, bias currents and references.

The first step in layout of integrated circuits is to estimate the die area. The area of each circuit block has to be computed separately. The total area of an integrated circuit is the sum of the areas of all circuit blocks plus the required area for wiring, bond pads, scribe seals and scribe streets.

After that a floor plan has to be constructed. When the first layout is finished, a simulation file is generated and a back annotation is started. The layout can be modified several times.

The following subsections describe the floor plan, the layout considerations and the back annotations.

3.3.1 Floor plan

A floor plan is a sketch of the layout. It shows the placement and shapes of all the different cells. During the layout the floor plan is used as a guide to design the pad ring. When a cell needs significantly more or less area than estimated, the floor plan has to be modified.

In the floor plan the placement gets optimized for matching and packaging. Each cell requires resistors, capacitors or diodes. In the floor plan the placement of each cell gets optimized. The area is minimized. The interconnections get optimized, to minimize the parasitic capacitances and resistances. The parasitic capacitances of wires are smaller at higher metal layers. The floor plan of the oscillator is depicted in Figure 40.

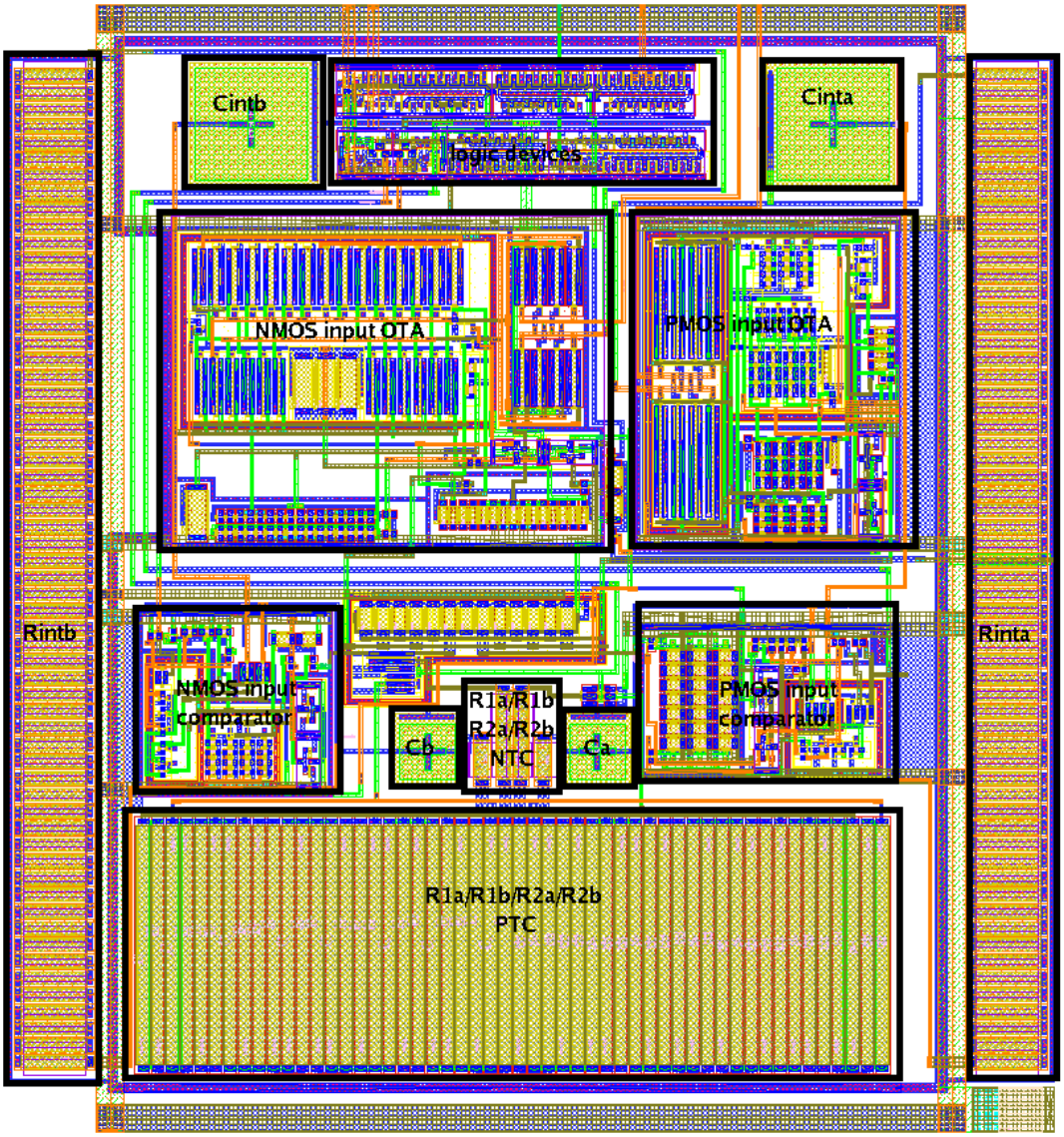

Figure 40: Floor plan of the oscillator

The placements take care of sensitive cells and nets. The used circuit topology contains some sensitive point. The nets $v_{osca,b}$ has to be as short as possible and has to have small parasitic capacitances, because at this net the time determined passive devices are placed.

3.3.2 Layout considerations

There are some things and techniques to consider before to start with a layout [14].

The sensitive devices have to be placed in the middle of the layout. The later surroundings of the block are unknown. Sensitive signals, like bias currents or references, have to be far away from signals, like clock signals. The sensitive signals have to be placed in the middle of the layout, because the later surroundings of the block are unknown. Nets sensitive to parasitic capacitances have to be placed at a higher metal layer to keep the parasitic capacitance small. Signals which are not sensitive to parasitic capacitances have to be placed on lower metal layers.

The use of unit elements is helpful to use layout strategies like common centroid layout. A big device is split in certain unit elements. The matching of devices is easier to optimize with unit elements. Dummy elements are needed to assure a steady surrounding of all the unit elements. The unit elements are placed in a common centroid layout scheme to improve the matching of the two transistors. A possible common centroid layout scheme with dummies of two devices which have to match is depicted in Figure 41. A disadvantage of using dummy devices is the additional area needed for the devices. As a result dummy devices are used, when absolutely necessary.

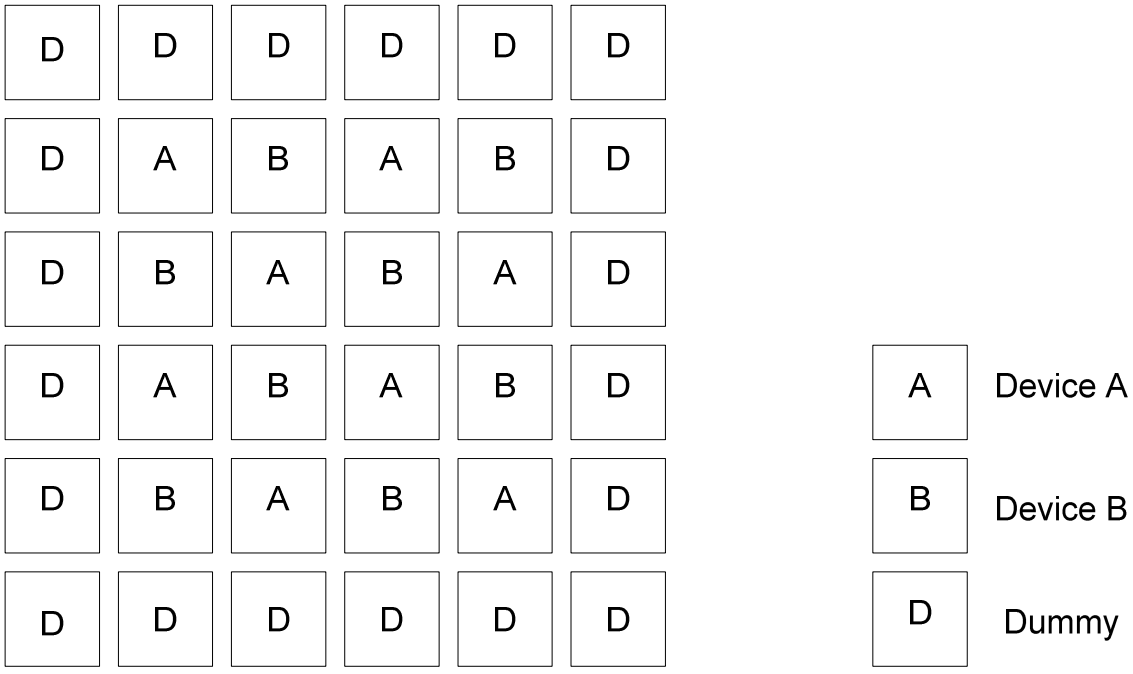

Figure 41: Common centroid layout with dummy devices for two matching devises

The diode at the current mirror has to be in the middle of the other mirror transistors to improve the matching. The matching parts have to be placed as close as possible together, to improve the matching, because the surroundings have to be equal. The current through the matching transistors has to flow in the same direction.

The transistors of the large differential input pairs have to be split in several unit transistors. The unit transistors have to be placed in a common centroid layout scheme. The wires to the load of the differential pair have to be symmetric. When the wires are symmetric, the parasitic capacitance and resistance have to be nearly the same and no offset is added. A possible common centroid layout scheme for a differential input pair is depicted in Figure 42.

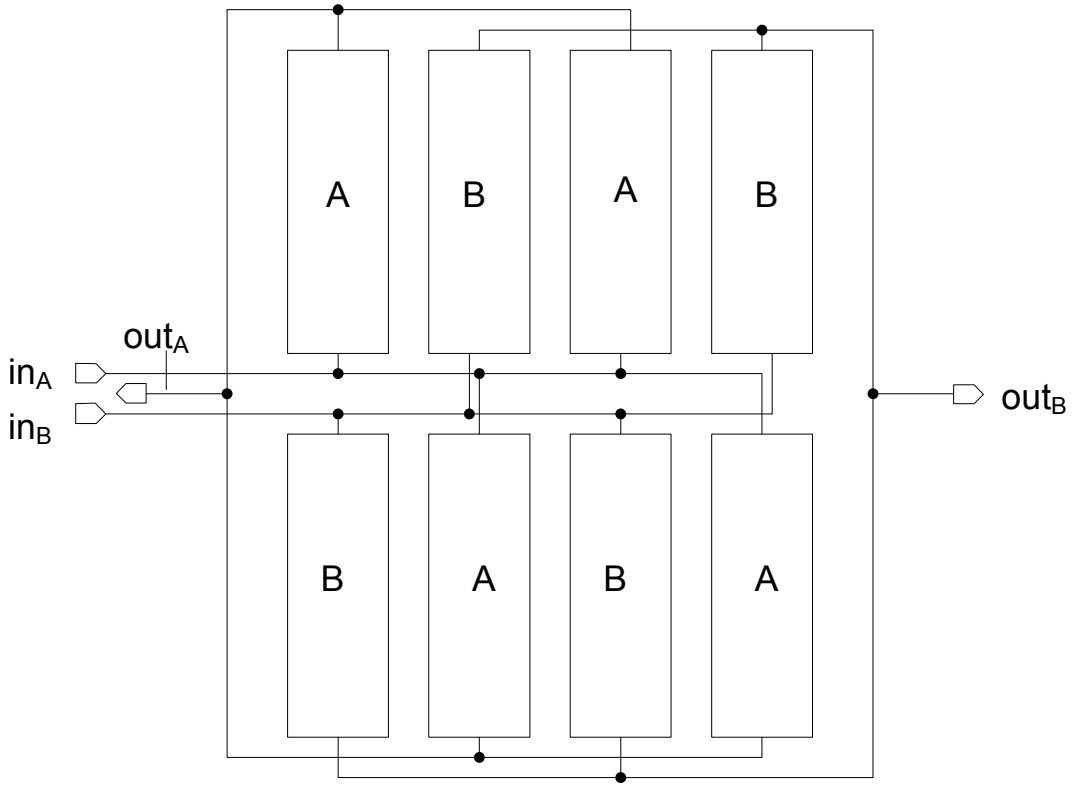

Figure 42: Common centroid layout scheme of a differential input pair

3.3.3 Back annotation

The oscillator layouts are extracted and simulated. These simulations show issues.

One issue is the parasitic capacitance of the resistor array, which affects the output frequency enormously. The charge and discharge resistors are decreased to achieve an output frequency of 100 MHz. The final schematic of the oscillator with two stage OTAs is depicted in Figure 43.

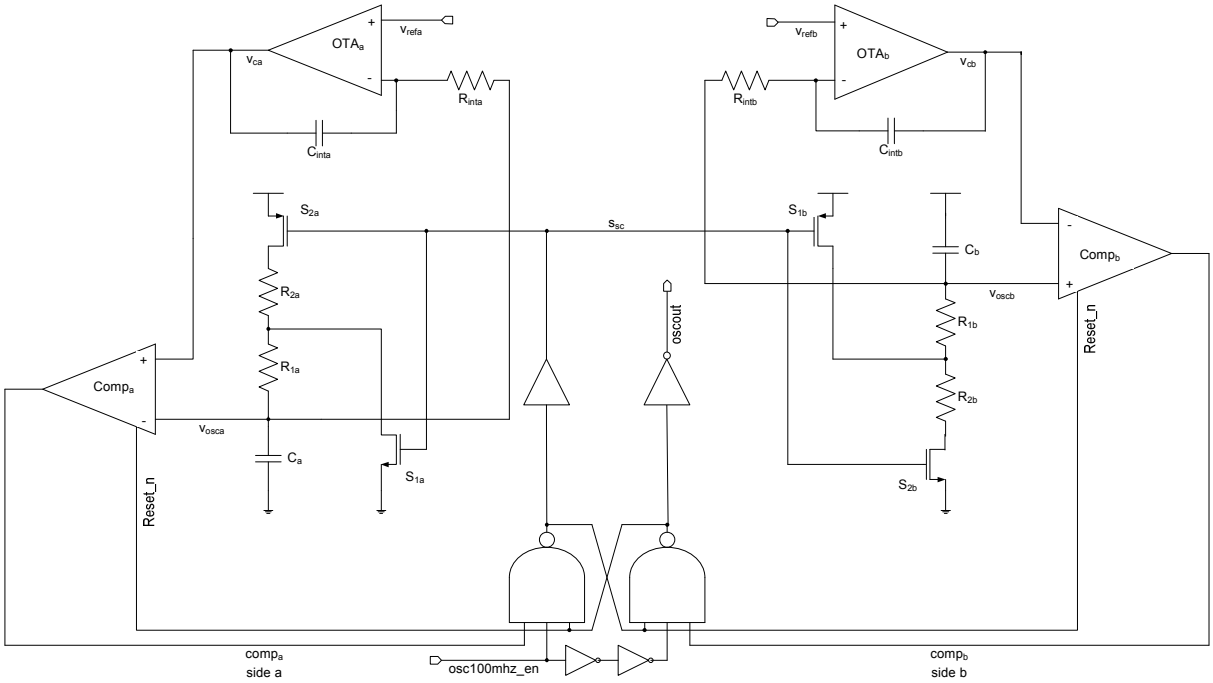

Figure 43: Final Schematic of the oscillator with the two stage OTAs

Another issue is that the comparators are slower, because of the internal parasitic capacitance at the input of the output drivers.

The comparators are modified with a reset function. The reset function helps the comparators to push up their outputs. The comparators change their outputs to LOW. This LOW controls the cross-coupled NAND gates. The cross-coupled NAND gates control the switches and the added reset function of the comparators. At the same time only one comparator is in the reset mode except at start up. The modified comparator with NMOS input stage is shown in Figure 44.

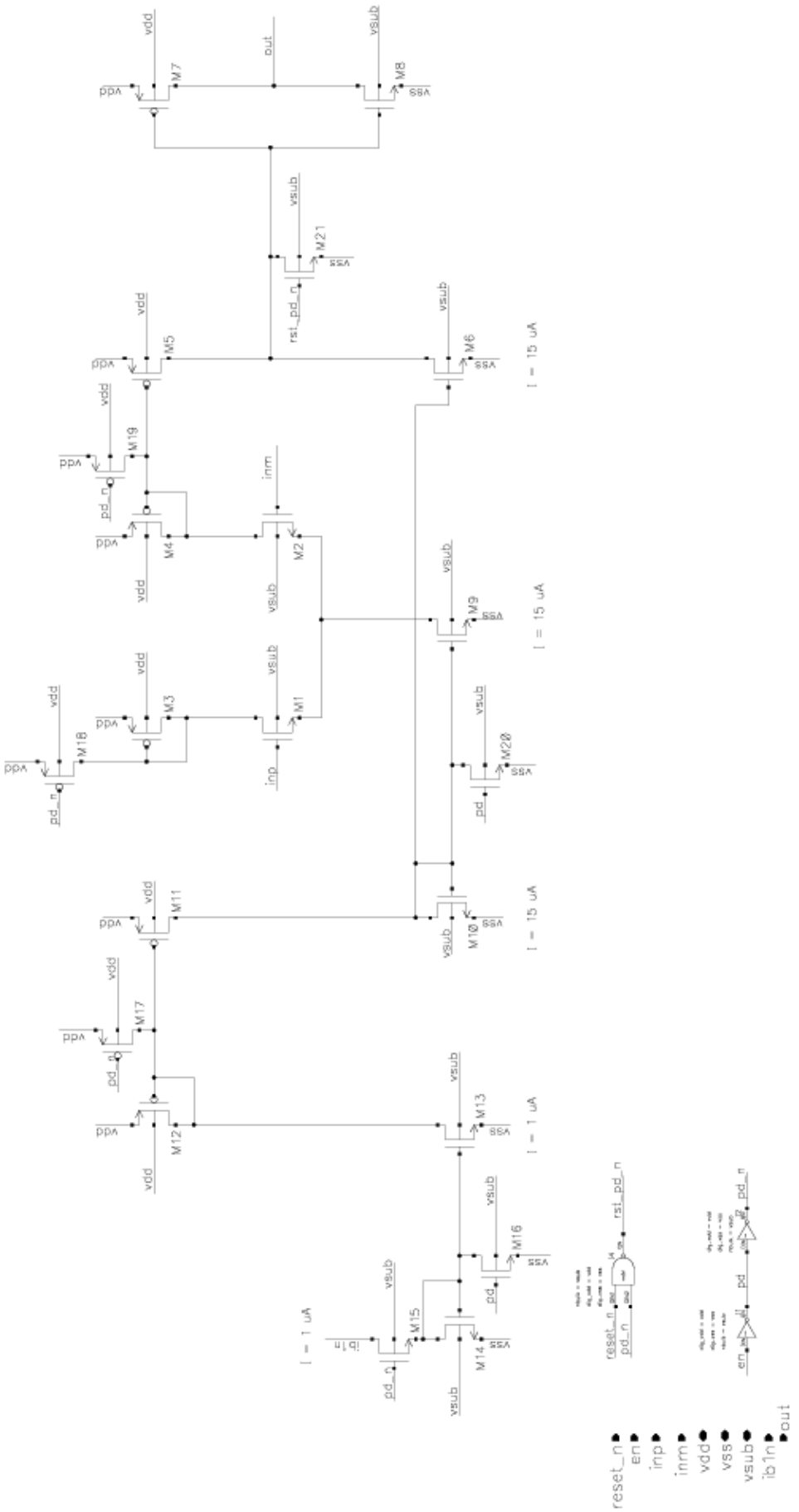

Figure 44: Modified comparator with NMOS input stage

The modified PMOS comparator is depicted in Figure 45.

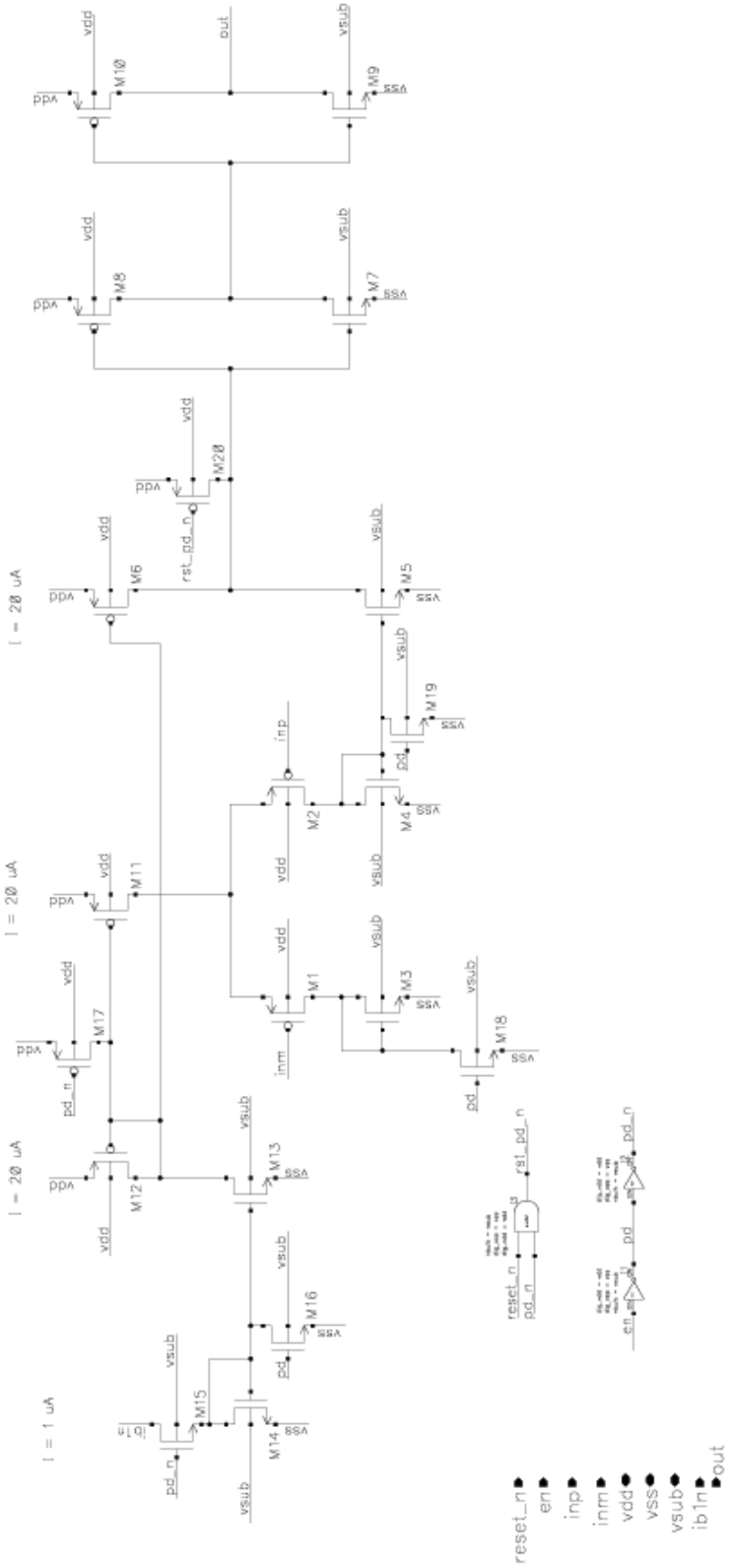

Figure 45: Modified comparator with PMOS input stage

The phase margin of the OTAs is reduced by the layout, but it is always larger than 50° and the integrator is stable.

3.3.4 Final layouts of the oscillator

The layouts have changed several times and the final layouts for the two different oscillators are depicted in Figure 46 and Figure 47. There are some empty areas which result from the modification caused by the back annotations. The sensitive blocks and nets are placed in the middle of the layout.

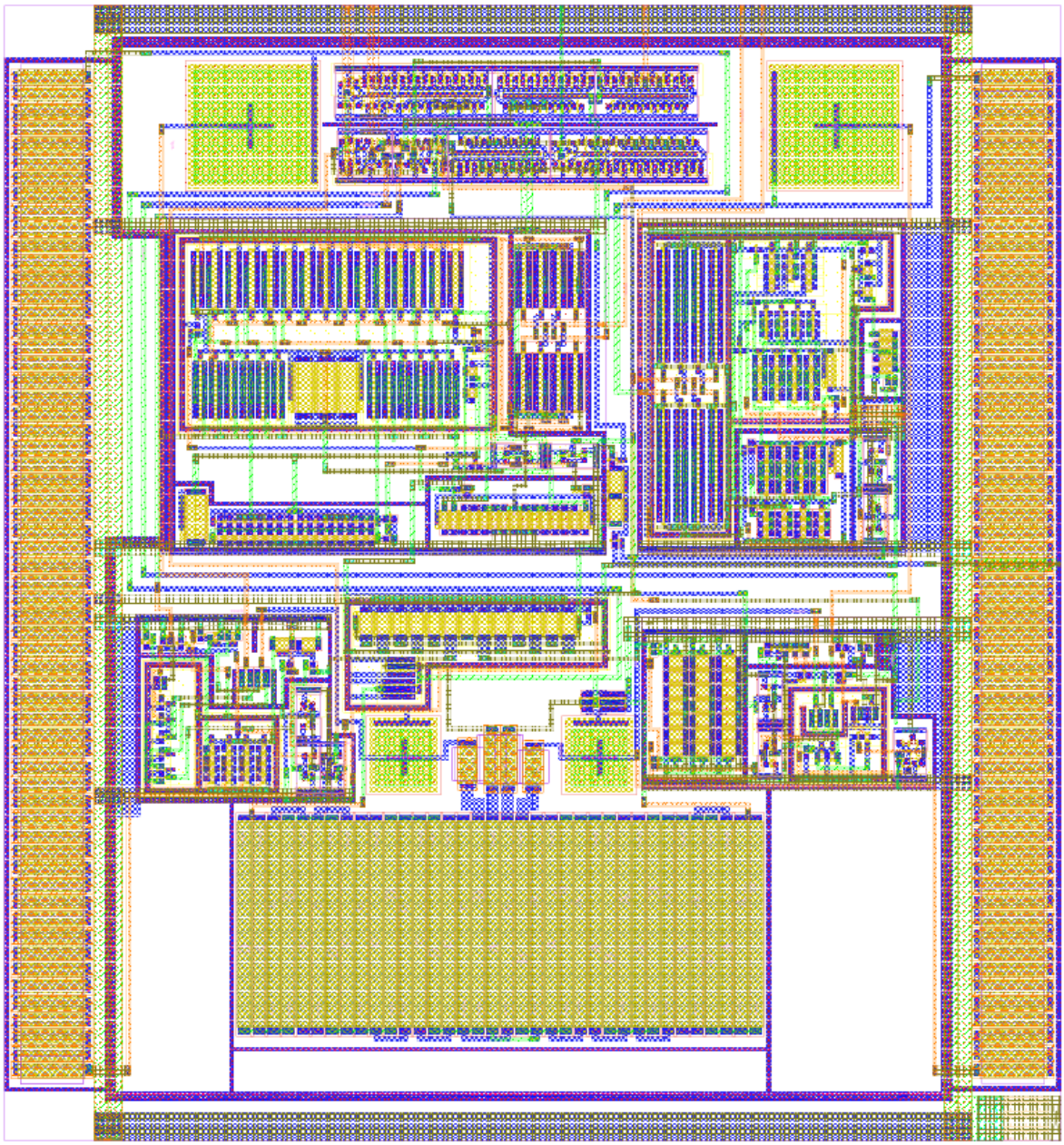

Figure 46: Final layout of the oscillator with the folded cascode OTAs

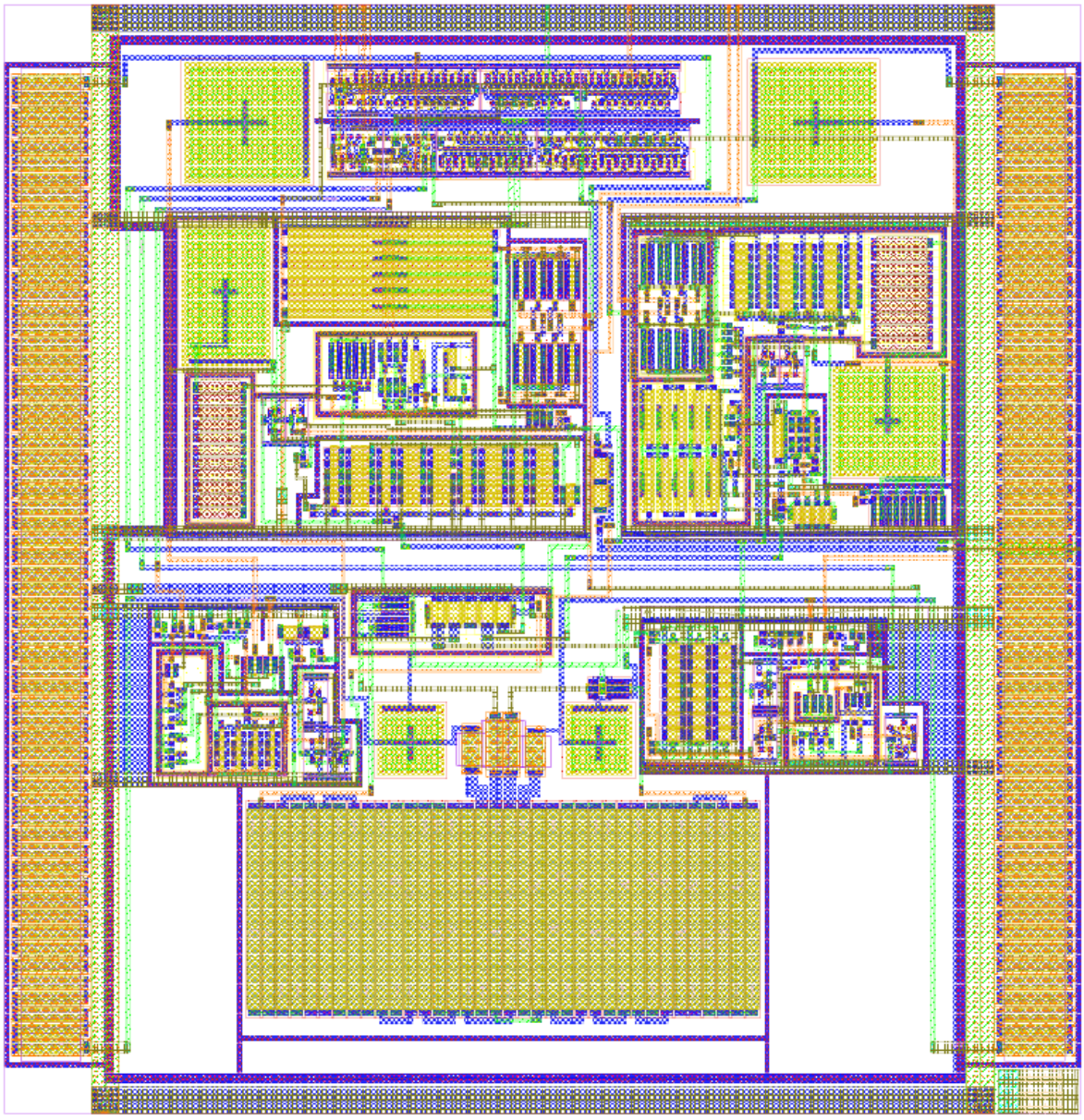

Figure 47: Final layout of oscillator with the two stage OTAs

3.3.5 Test chip layout

The two oscillators are fabricated in a 0.35µm CMOS process and are packaged in a SOIC28 300mil package. The test chip schematic is depicted in Figure 48. The two oscillators have separate voltage references, separate bias currents, separate enable signals and separate output buffers.

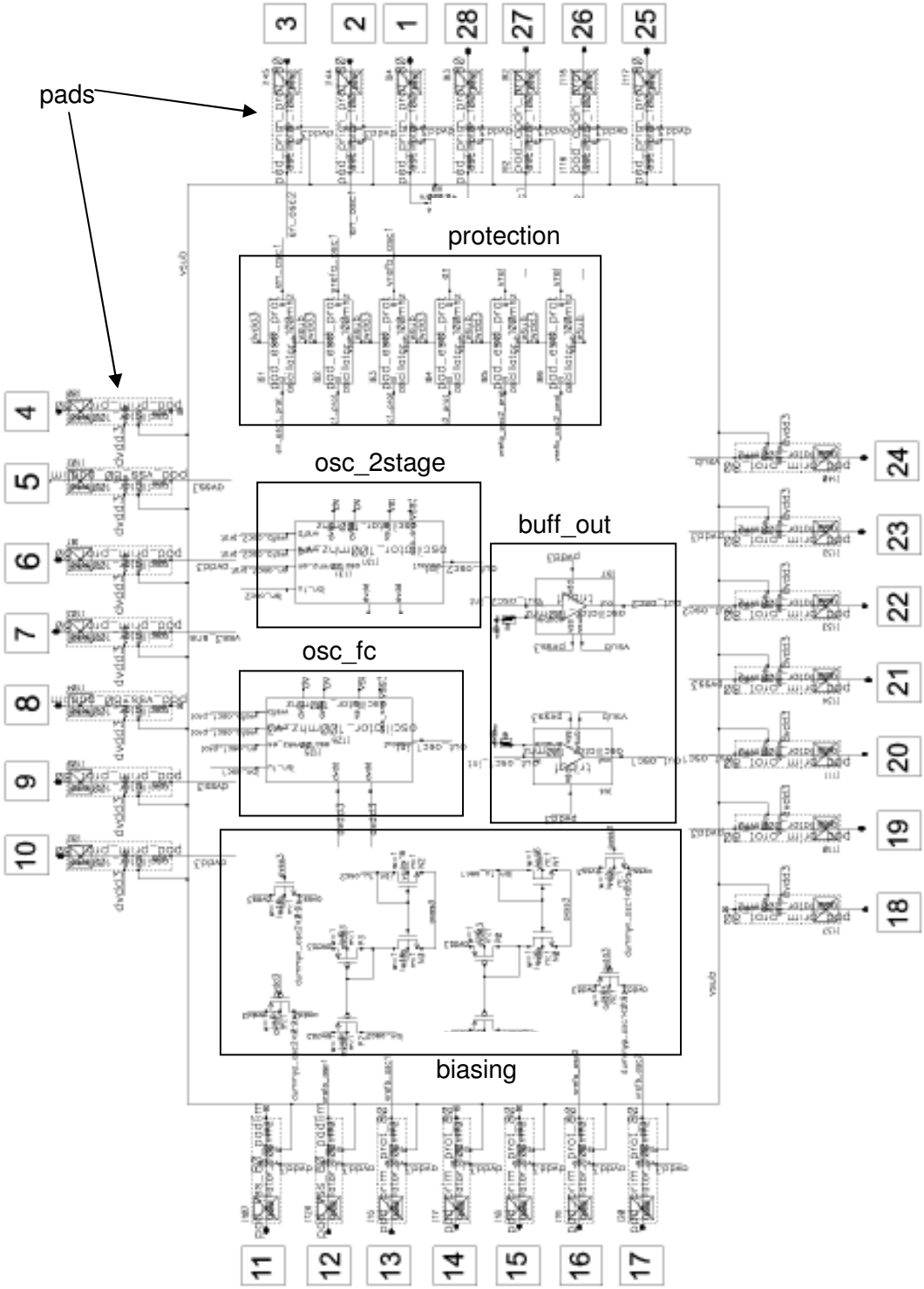

Figure 48: Schematic of the test chip

The output buffers are placed as near as possible to the output pads. The supply of the output buffers is also close to the pads. The current consumption of the output buffers are high. The sensitive supplies of the analogue parts are separate from the digital supply and between these supplies no connect pad is inserted. The four pads at the corners are also not connected. All signals that drive a gate are protected with an additional protection. The pin allocation is depicted in Table 3.Table 3: Pin allocation

	pin name		**pin name**
1	NC1	15	NC15
2	en_osc1	16	vrefa_osc2
3	en_osc2	17	vrefb_osc2
4	NC4	18	NC18
5	avss3	19	pvdd3
6	avdd3	20	out_osc1
7	vss3_sns	21	pvss3
8	NC8	22	out_osc2
9	dvss3	23	pvdd3
10	dvdd3	24	vsub
11	NC11	25	vsub
12	vrefa_osc1	26	ibn_1u_osc2
13	vrefb_osc1	27	ibn_1u_osc1
14	NC14	28	NC28

Table 3: Pin allocation

The layout of the test chip is depicted in Figure 49. The two oscillators are placed in the middle of the test chip. The output buffers are close to the output pads.

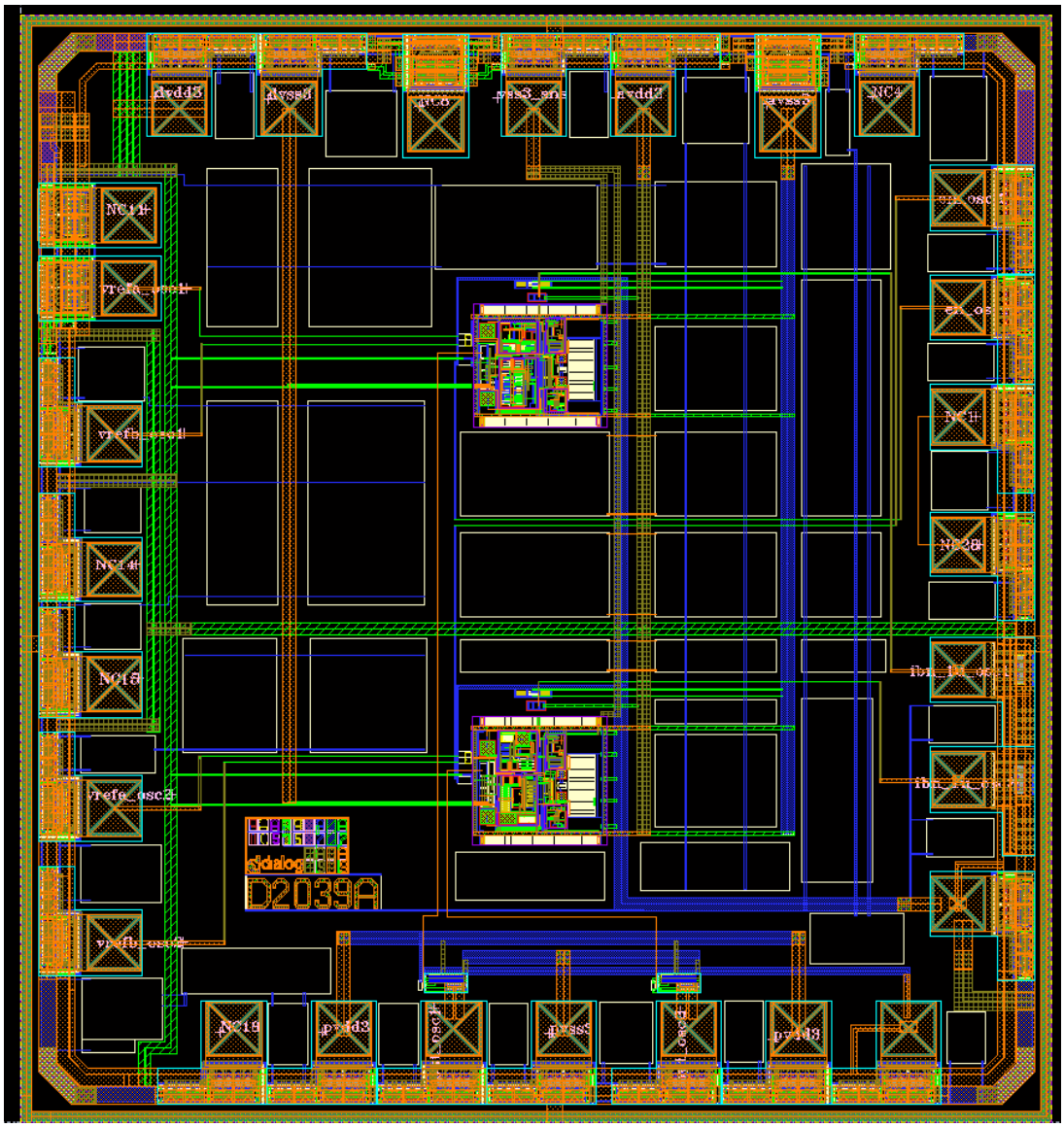

Figure 49: Final layout of the test chip

4 Conclusion

A new voltage averaging feedback topology was designed for a nominal frequency of 100 MHz. Variation of the supply does not affect the output frequency as long as the voltage reference is a constant proportional of the supply voltage. The temperature range is from -40°C to +125°C. The delay time of the comparators are internally compensated by the voltage averaging feedback. The delay times of the digital gates do not affect the output frequency. The new topology achieves an accuracy of ±1.5% over temperature. The oscillator failed in three corners. In these three corners the control loop is not able to compensate the too slow comparator and the oscillator frequency sinks at the worst case to 83 MHz. The used comparator is too sensitive to the parasitic capacitances of the layout.

Two different oscillators are fabricated on a test chip in a 0.35µm CMOS process. The difference between the two circuits lies in the OTAs used for the control loop. It needs to be analysed which OTA topology has higher performance at the test chip. One of them is a folded cascode OTA, the other one is a two stage amplifier with a telescopic OTA as first stage and a current source stage as an output stage. The two stage amplifiers consume less current and reach a higher gain.

The electrical characteristics of the two oscillators are shown in Table 4. All the simulations are done over the temperature range from -40°C to +125°C.

A trim circuit to compensate the spread of the passive devices over the process was proposed but not implemented, because it was out of scope. The circuit proposed in this diploma thesis was a circuit with a variable current. This circuit makes first order temperature compensation possible.

The test chip has to be evaluated in the laboratory to analyse the temperature behaviour of the two fabricated oscillators on the test chip.

Parameter	**Condition**	**Oscillator with folded casccode OTAs**			**Oscillator with two stage OTA**			**Unit**
		min	typ	max	min	typ	max	
output frequency	over active corners and temperature	83[1]	100.7	101	85[2]	100.6	102	[MHz]
output frequency	over temperature (tt)	97.0	100.7	100.7	98.75	100.6	100.6	[MHz]
current consumption	Enable LOW (power down)		0.1			0.1		[µA]
current consumption	Enable HIGH; C_{load}=0fF		931			748		[µA]
current consumption	Enable HIGH; C_{load}=500fF		1000			872		[µA]
Y dimension			203			204		[µm]
X dimension			189			197		[µm]
area			38367			40188		[µm^2]

Table 4: Electrical characteristics

[1] The control loop is not able to compensate the comparator delay in the corners: ss 125°C, ss 27°C and fnsp 125°C

[2] The control loop is not able to compensate the comparator delay in the corners: ss 125°C, ss 27°C and fnsp 125°C

5 Registers

5.1 Table of figures

5.2 List of tables

5.3 Bibliography

[1]. **Yusuke Tokunaga, Shiro Sakiyama, Akinori Matsumoto, Shiro Dosho.** An On-Chip CMOS Relaxation Oscillator With Voltage Averaging Feedback. *IEEE Journal of Solid-State Circuits, Vol. 45, No.6.* Juni 2010.

[2]. **Valentijn De Smedt, Pieter De Wit, Wim Vereecken, Michiel S. J. Steyaert.** A 66 µW 86 ppm/°C Fully-Integrated 6 MHz Wienbridge Oscillator With a 172 dB Phase Noise FOM. *IEEE Journal of Solid State Circuits.* July 2009.

[3]. **Auer, Mario.** Passive Bauelemente in CMOS. 2010.

[4]. **Long, John.** Advanced Engineering Course on "RF Analog IC Design". June 2011.

[5]. **Harald Hartl, Edwin Krasser, Wolfgang Pribyl, Peter Söser, Gunter Winkler.** *Elektronische Schaltungstechnik.* 2008.

[6]. **Kenneth S. Kundert, Olaf Zinke.** *The Designer's Guide to Verilog AMS.* 2004.

[7]. **Phillip E. Allen, Douglas R. Holberg.** *CMOS Analog Circuit Design.* 2002.

[8]. **Razavi, Behzad.** *Design of Analog CMOS Integrated Circuits.* 2001.

[9]. **Johnny Chew, Zhang ShaoQiang, P.R. Verma, Sanford Chu.** Resistor Characterication Report.

[10]. **Bartsch, Hans-Jochen.** *Taschenbuch Mathematischer Formeln.* 2004.

[11]. **Bronstein, Semendjajew, Musiol, Mühlig.** *Taschenbuch der Mathematik.* 2000.

[12]. **Ulrich Tietze, Christoph Schenk.** *Halbleiter-Schaltungstechnik.* 2009.

[13]. **Sansen, Willy M. C.** *Analog Design Essential.* 2006.

[14]. **Hastings, Alan.** *The Art of Analog Layout.* 2005.