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Switched Mode Transmitter Architectures for Efficient Wireless Communication Systems

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Abstract

With the increasing number of wireless services and users, the required bandwidth is ever increasing. To use the available spectrum efficiently modern communication standards, such as LTE, employ sophisticated modulation schemes with high crest factors. As a result, the power amplifier (PA) spends most of its time providing for less than its maximum output power, leading to low average efficiency in traditional designs. Therefore, PA concepts providing efficiency enhancement in back off are key for efficient transmitters.

Base Band PWM (BB PWM) is a promising concept to provide high efficiency over a wide output power range. Conventional BB PWM transmitters use an isolator before the band pass filter to prevent its reflections interfering with the PA operation. This causes a loss of energy in the modulation sidebands and limits the achievable efficiency. By removing the isolator and by connecting the filter directly, while accounting for the filters reflections, these losses can be mitigated. Such designs require multilevel PA structures that can deal efficiently with the resulting continuous load current. The concept of direct filter connection results in dynamic load modulation of the PA, enabling efficient operation. As the load modulation trajectories are of importance for successful designs, generalized analytical equations are presented. A design methodology based on both, the load pull contours of the PA and the load modulation trajectories, has been developed and applied to the presented designs. The band pass filter is the starting point for the design of the matching network as the phase of the reflections caused by the matching network have a significant influence on the design. The impact of the coupling to a cavity resonator and its reflections is studied. It was found that for best performance, a short connection between PA and band pass filter is vital. Thus requires a co-design of the output matching network on printed circuit board level and the cavity band pass filter. Based on the derived design requirements, an implementation study of four integrated multi level PA structures designed on a GaN MMIC process has been carried out. Two of the presented structures are based on a parallel concept, while the other two rely on series concepts. All four proposed PA structures can be combined with direct filter connection and outperform conventional BB PWM operation.

For an efficient transmitter system, the power consumption of the modulator also plays an important role. In that context the use of RF PWM modulators shows promising results, but they still lag behind conventional state of the art modulators in terms of spectral quality. As a result this work focused on the required signal processing to correct for digital, as well as analog imperfections. Aliasing effects of digital RF PWM, which are due to its discrete time nature, could be reduced by introducing cross point estimation. With a special predistortion scheme tailored to the properties of RF PWM modulation, the spectral limitations due to the driver nonlinearity could be overcome. Additionally, a concept for digitally correcting the device mismatch is presented. It can optionally be combined with delta sigma modulation to improve the inband signal quality. The proposed signal processing chain is verified by extensive simulations and supported by measurements. By using the applied corrections mismatch, driver nonlinearity and aliasing due to the discrete time nature can be compensated and high signal quality can be maintained.

Kurzfassung

Durch die ständig steigende Anzahl an Nutzern von mobilen Breitbanddiensten wurde das verfügbare Spektrum zu einer wertvollen Ressource. Moderne Kommunikationsstandards, wie LTE, verwenden zur effizienten Nutzung des Spektrums aufwändige Kodierverfahren, wodurch die Leistung des zu sendenden Signals stark variiert. Dadurch wird der Leistungsverstärker meist mit verringerter Leistung betrieben, was bei konventionellen Verstärkern zu einer starken Reduktion des Wirkungsgrades führt. Konzepte zur Effizienzsteigerung des Leistungsverstärkers von Sendern bei niederen Ausgangsleistungen sind daher extrem wichtig.

Basis Band Pulsweitenmodulation (BB PWM) hat sich als vielversprechende Maßnahme herausgestellt. Üblicherweise wird bei BB PWM Sendern ein Isolator eingesetzt um zu verhindern, dass die Reflektionen des zur Demodulation erforderlichen Bandpassfilters (BPF) Einfluss auf die korrekte Funktion des Leistungsverstärkers haben. Dies führt jedoch zu Verlusten, da die Energie der Modulationsseitenbänder verloren geht. Durch den direkten Anschluss des BPF an den Leistungsverstärker können diese Verluste minimiert und die Effizienz des Senders gesteigert werden. Dazu werden Verstärker benötigt, die mehrere Ausgangsleistungen erzeugen und mit dem entstehenden, konstanten, Laststrom des Filters und der daraus resultierenden Lastmodulation effizient umgehen können. Um die bestmögliche Effizienz zu erreichen, ist die Berücksichtigung der Lastmodulationskennlinien erforderlich. Daher werden allgemeine analytische Gleichungen zu deren Berechnung präsentiert, welche die Grundlage der angewendeten Entwicklungsmethode unter Berücksichtigung der Effizienzkontouren des Verstärkers für verschiedene Lastimpedanzen bilden. Den Startpunkt für die Entwicklung des Anpassungsnetzwerkes bilden die Reflektionen des verwendeten BPF, in diesem Fall eines Hohlraumresonators. Da diese Reflektionen, vor allem deren Phase, stark von der Art und Stärke der Koppelung abhängen, wurde ihr Einfluss analysiert und die Ergebnisse in die Entwicklung des Anpassungsnetzwerkes mit einbezogen. Des Weiteren wurde herausgefunden, dass für den breitbandigen Betrieb eine kurze Verbindung zwischen Verstärker und Filter unabdingbar ist, was zur Folge hat, dass das Anpassungsnetzwerk auf Leiterplattenebene zusammen mit dem BPF entworfen werden muss. Anhand der aufgestellten Anforderungen wurden vier integrierte Schaltungen in einem GaN MMIC Prozess entwickelt, welche den direkten Filteranschluss unterstützen und bessere Effizienzen als konventionelle BB PWM erzielen.

Neben der Effizienz des Verstärkers spielt auch der Leistungsverbrauch des Modulators eine wichtige Rolle. In diesem Zusammenhang hat sich die Verwendung von auf RF PWM basierenden Modulatoren als eine besonders energieeffiziente Implementierungsvariante erwiesen, welche jedoch die erforderliche spektrale Qualität noch nicht bieten. Daher wurde hier der Fokus auf die erforderliche Signalverarbeitung zur Korrektur von analogen, sowie digitalen Effekten gelegt. Zur Kompensation von Aliasingeffekten, resultierend aus der zeitdiskreten Ansteuerung des RF PWM Modulators, wurde eine Methode zur Berechnung der korrekten Signalübergange vorgeschlagen. Im analogen Bereich begrenzt vor allem die Nichtlinearität der verwendeten Treiberschaltungen die Signalqualität. Dieser Effekt kann mittels einer speziell auf die Eigenschaften digitaler RF PWM zugeschnittenden Vorverz-

errung bestmöglich kompensiert werden. Zudem wird ein Konzept zur Kompensation der Fertigungstoleranzen des Modulators auf der digitalen Ebene vorgestellt, welches optional mit einem $\Delta\Sigma$ Modulator kombiniert werden kann, um die Signalqualität bei limitierter Auflösung zu erhöhen. Die vorgeschlagene Signalverarbeitungskette wurde anhand von Simulationen und Messungen verifiziert. Durch die Anwendung der entsprechenden Korrekturmaßnahmen können die vorhandenen Fehler kompensiert und beste Signalqualität erreicht werden.

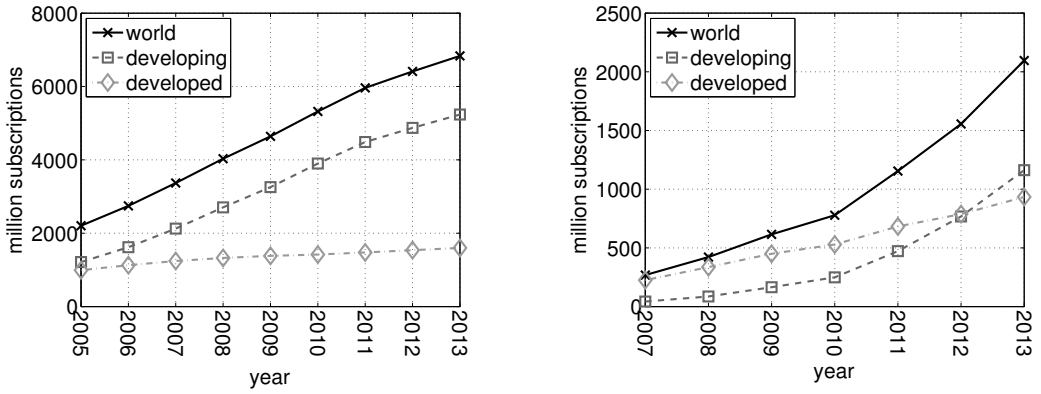
Acknowledgment

A number of people deserve thanks for their support and help with my PhD thesis. It is therefore my greatest pleasure to express my gratitude to them all in this acknowledgment. First of all, I would like to thank Peter Singerl for the industrial supervision of this thesis as well as for sharing his expertise and for his continuous support in various matters. Thanks to Christian Schuberth for sharing his rich experience in PA design with me, as well as for his patient explanations and the support during the writing of many papers. I am also grateful to Franz Dielacher for his continuous encouragement and belief in the switched mode transmitter project. The support of Martin Mataln when it came to predistortion topics and the FPGA implementation/measurements was much appreciated. I would also like to thank Marc Tibout and Koen Mertens for the review of the designs as well as for their help with various other problems regarding the UNIX system. Important to mention are also Bittolo Alberto, who investigated different matching structures during his master thesis, and Stefano Lenuzza, who offered me support with various measurement topics. Furthermore I would like to thank Wolfgang Bösch for the academic supervision and his guidance. Michael Gadringer's comments on various technical problems, as well as on many of the published papers, shall also be acknowledged. I am furthermore grateful to Patrick Reynaert for spending the effort to be my second examiner. I would also like to thank Matthias Thorsell and Christian Fager for their support and discussion regarding the GaN MMIC process. The discussions with Shailesh Kulkarni and Wim Dehane on the digital implementation of the RF PWM modulator provided valuable input for the development of the compensation algorithms. Also Yannis Papananos and Nikolaos Alexiou for providing me insights in the analysis and design of the analog RF PWM modulator shall not remain unmentioned. Last but not least I want to mention family and friends, who accepted my occasional absence and supported me in various ways during these years.

Contents

1. Introduction

Mobile communications have become an indispensable commodity of today's society. The rapid growth of this market sector can be seen best when observing the number of mobile subscriptions over the recent years. From 2005 to 2013 world wide mobile cellular subscriptions have more than tripled (see Fig. 1.1(a)). With the advances in technology and the resulting commercialization of broadband data services, this user group increased even more rapidly. Fig. 1.1(b) shows that the number of mobile-broadband subscriptions from 2007 to 2013 have even more than seven folded. This growth imposes a challenge for the infrastructure providers in terms of bandwidth, but also in terms of energy consumption.



(a) Mobile cellular subscriptions

(b) Active mobile-broadband subscriptions

Figure 1.1: Number of mobile subscriptions using broadband services and total number of subscriptions, data retrieved from [1].

To account for this development new standards are continuously developed leading from UMTS[1] [2,3] towards LTE[2] [4,5] and LTE Advanced [6]. To increase the spectral efficiency in order to provide high data throughput these standards employ sophisticated modulation schemes. As a result the Peak to Average Power Ratio (PAPR) of these signals becomes very large. This means that the average signal is far below its maximum value. For the design of the Power Amplifier (PA) this imposes a great challenge, as it has to be designed to provide the maximum output power, although being operated at far lower output powers for most of the time. In traditional PA designs the efficiency is significantly reduced when operating the PA at lower output powers, which leads to a rather low overall efficiency. As a consequence the PA is a major contributor to the energy consumption of a radio base station, as can be seen in Fig. 1.2. Therefore, its efficiency, especially at low output powers, is an important parameter for the total efficiency of a transmitter [7, 8].

Besides the use of spectrally efficient modulation schemes the trend goes towards smaller (pico cells) and smaller cell sizes (femto cells) to increase the network capacity [9]. This results in a larger number of base stations with their related energy consumption. Due to the rather inefficient PA and the large number of transmitters, there is a large potential for energy savings by improving the PA efficiency.

Therefore, this thesis is dedicated to the development of efficient transmitter architectures. A main focus is set on switched mode architectures, which are known for their high peak

[1] 3rd generation mobile cellular standard
[2] 4th generation mobile cellular standard

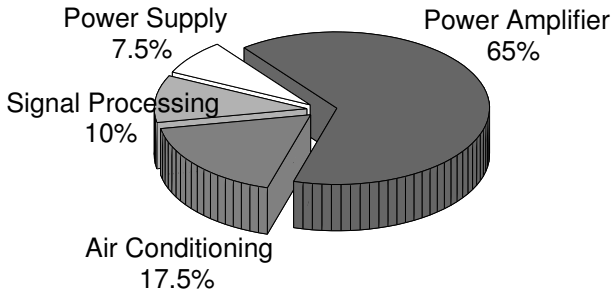


Figure 1.2: Power consumption radio base station, data retrieved from [8].

efficiency [10], as they reduce the overlap between current and voltage waveforms and thus their losses. In that context two different methods, namely Base Band Pulse Width Modulation (BB PWM) and Radio Frequency Pulse Width Modulation (RF PWM), are investigated. Their properties and prospects in terms of energy efficiency are presented. In the context of BB PWM operation the concept of direct filter connection is a very promising solution for highly efficient operation. Different integrated circuit implementations capable of supporting direct filter connection are investigated.

Additionally, aspects like flexibility, reconfigurability, multi band and multi standard operation are of importance. The use of RF PWM goes hand in hand with the trend towards purely digital solutions moving the digital domain closer towards the antenna enabling Software Defined Radio (SDR). The required signal processing for compensating digital and analog effects to achieve best signal quality in RF PWM transmitters is analyzed and corresponding solutions are proposed.

The second chapter provides an introduction on the different PA classes and discusses their properties under rectifier operation. In addition, the requirements on the static efficiency curve for good average efficiency are derived and the loss mechanisms of RF power transistors with a focus on load modulation aspects are discussed.

The third chapter introduces well established as well as recently developed methods for efficiency enhancement in the low power region. A main focus is set on BB PWM operation of the PA, which means that the PA is either operated at maximum power or switched off, being highly efficient under both conditions. The theoretical concept of BB PWM is introduced and further efficiency enhancement by direct filter connection is discussed. Additionally, different energy recovery methods are presented. Also the concept of RF PWM operation, which means that the PWM encoding is applied on the carrier pulse length itself and not on the signal envelope, is covered.

Chapter 4 is dedicated to the development of integrated PA circuits suitable for BB PWM operation in combination with direct filter connection. First, modulation aspects regarding the signal quality are covered. In a next step the load modulation properties of direct filter connection under BB PWM are derived. Based on them, the requirements for the matching network design are determined. In order to provide an optimum design the orientation of the resonance locus is a very important parameter. A design methodology for the direct filter connection based on the load modulation trajectories considering the orientation of the resonance locus is developed. The starting point for the matching network design is the input impedance, respectively resonance locus, of the Band Pass Filter (BPF). Therefore, the impact of the coupling on the reflections of a cavity filter is investigated and considered in the final designs. Four different integrated PA designs are presented. Two of them rely on a parallel concept, while the other two are based on series concepts in order to provide an efficient multilevel PA structure capable of supporting

direct filter connection. In addition, an implementation study of a biphase energy recovery transmitter, as well as a Doherty PA designed for isolated BB PWM operation is presented. Finally, different spectral considerations, such as predistortion and achievable bandwidth, are considered.

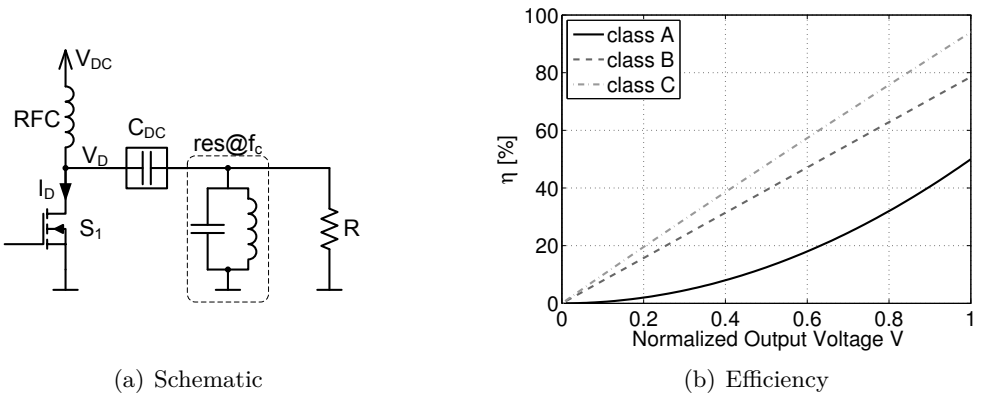
The focus of chapter 5 is on RF PWM operation. First the properties of the different PA classes under RF PWM excitation are discussed. Besides the PA efficiency, flexibility and reconfigurability of the modulator are very important parameters. Therefore, the properties of the RF PWM modulator itself are investigated in detail. In order to provide high spectral quality non ideal effects of the modulator have to be compensated. Thus, a main focus is set on the required signal processing. The impact of the discrete time nature of the achievable signal quality due to aliasing effects is covered and a method to mitigate this limitation is presented. Additionally, the properties of real driver circuits, which show nonlinear behavior, are studied. In order to compensate the driver nonlinearity under broadband signal excitation a special predistortion scheme is proposed. Finally, the aspects of digital mismatch compensation and the use of $\Delta\Sigma$ modulators for resolution enhancement are presented.

2. Amplifier Fundamentals

This chapter is dedicated to provide the basics of RF Power Amplifiers. The different amplifier classes and their properties are discussed in detail. Additionally, RF rectifiers are covered, as they are of importance for efficiency enhancement methods using energy recovery. In addition, the loss mechanisms of RF power transistors and their impact on the load pull contours are presented. Finally, the impact of the amplitude distribution on the average efficiency and the resulting requirements for static efficiency behavior is covered.

2.1 Linear Amplifiers

This section provides an introduction to the basic PA classes as A, B and C respectively. The schematic for this three PA classes is the same and provided in Fig. 2.1(a). The transistor S_1 is biased by means of an RF Choke (RFC), which provides the DC bias current and an open circuit at the carrier frequency. To avoid any DC current flowing to the load R, leading to unnecessary power dissipation, a series decoupling capacitor C_{DC} is required. The higher order harmonics of the drain voltage are short circuited by the parallel shunt resonator, which is high ohmic for the carrier frequency.



(a) Schematic (b) Efficiency

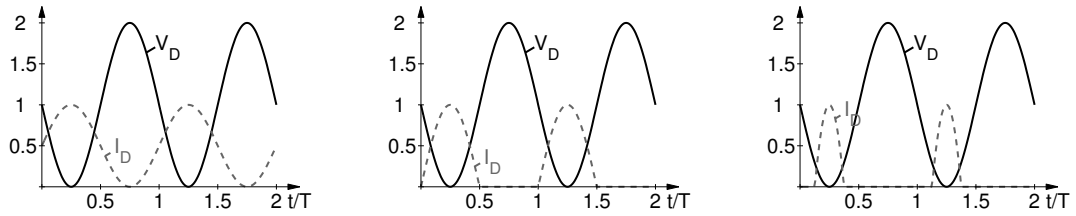
Figure 2.1: Class A schematic and efficiency.

The difference between the amplifier classes is in the biasing condition for the drain current of the transistor, which can be written as

$$I_D(\theta) = \max(I_{D,MAX}\left((1-k)\ m\ \sin(\theta) + k\right); 0), \tag{2.1}$$

where $I_{D,MAX}$ denotes the maximum drain current of the transistor, k is the normalized bias current. The parameter m denotes the normalized drain current amplitude, respectively the normalized gate voltage amplitude, and θ is the normalized (angular) time variable. The normalized drain current factor k basically defines the class of operation and n controls the output power by varying the drive level. For class A operation the drain bias current is set to half of its maximum value ($k = 0.5$). The resulting drain current and voltage time domain waveforms for class A operation and maximum output power are depicted in Fig. 2.2(a). It can be seen that the drain current varies in a sinusoidal way around the bias value of 0.5. This class of operation has a significant overlap of voltage and current and thus power dissipation in the transistor, which leads to rather poor efficiency. The DC current consumption remains constant independently of the drive level, as

the current never becomes zero. Therefore the DC power consumption remains constant regardless of the output power and the efficiency is directly related to the output power as $\eta_A = V^2/2$ [10], as depicted in Fig. 2.1(b). The general derivation of the efficiency is provided in section 7.1.

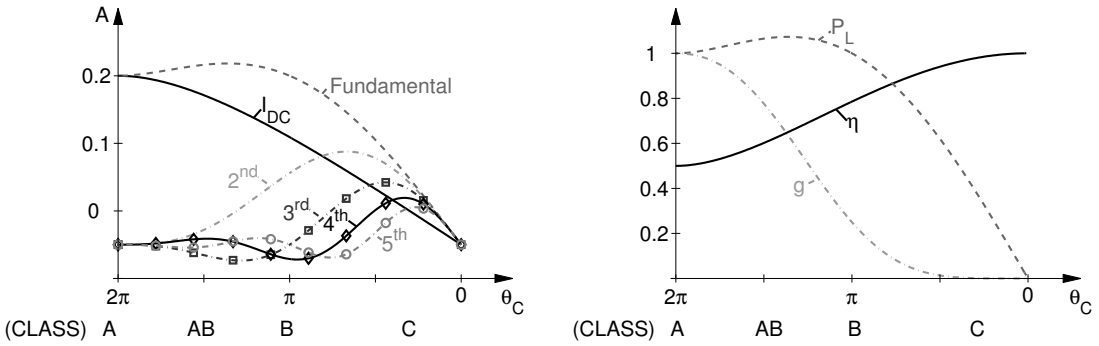


(a) Class A (b) Class B (c) Class C

Figure 2.2: Drain voltage and current time domain waveforms for class A, B and C.

A way to improve the efficiency is to reduce the drain current biasing to the threshold of the transistor ($k = 0$), which is defined as class B [10]. The sinusoidal gate drive is now translated into a half sinusoidal drain current, which leads to a reduced overlap of current and voltage, as can be seen in Fig. 2.2(b). As the DC current consumption linearly depends on the drain current for this operational mode, the efficiency is improved to $\eta_B = V\pi/4$, where V denotes the normalized output voltage. The factor $\pi/4$ is a result of the residual overlap of drain voltage and current.

The fundamental drain current for class B operation is the same as for class A operation. This can be seen in Fig. 2.3(a), which depicts, the DC, fundamental and higher order harmonics amplitudes versus the conduction angle. From Fig. 2.3 it can also be seen that the DC current I_{DC} is significantly higher for class A biasing than for class B. This leads to the improvement in efficiency as depicted in trace η in Fig. 2.3(b). It can also be seen that the output power is highest for class AB operation, meaning that the biasing is somewhere inbetween class A and class B.



(a) DC and harmonic content (b) Power, gain and efficiency

Figure 2.3: General harmonic contribution and power, gain and efficiency versus conduction angle.

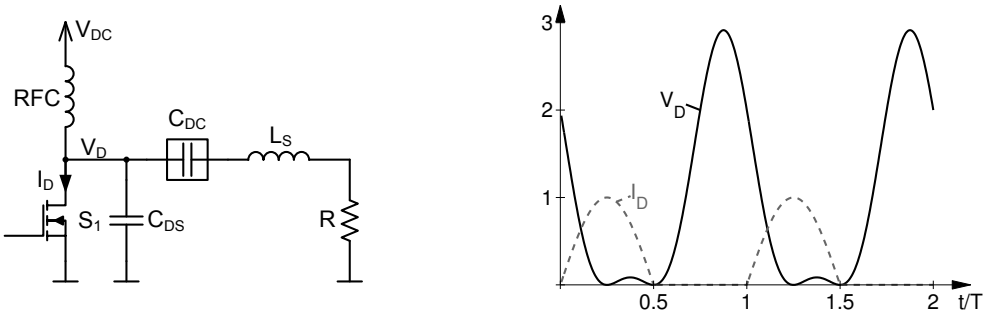
When moving to even smaller conduction angles than class B operation the efficiency is further improved as the overlap current and voltage decreases, as can be seen in Fig. 2.2(c) for a conduction angle of $\pi/2$. This operational region is referred to as class C. Unfortunately, the output power P_L rapidly decreases for short conduction angles as the fundamental component of the drain currents gets very low. On the other hand the required gate drive swing increases, which leads to higher input power, causing a degradation in gain. This

effect in general leads to low Power Added Efficiency (PAE) for class C operation making this mode of operation less attractive for single PAs.

Finally it shall be noted that only the ideal class A and class B circuit show linear behavior over the whole operational range. The gain under class AB bias and especially class C biasing experiences gain expansion before compressing at maximum output powers, which leads to nonlinear behavior.

2.2 Class J

In practice a perfect short circuit of the higher order harmonics can hardly be achieved or may be even undesired. Usually the parasitic drain source capacitance C_{DS} is resonated out at carrier frequency and is supposed to provide the desired short circuit at the carrier harmonics. At the second harmonic this short circuit is normally not very pronounced and one can use this capacitive termination to contribute to the drain voltage waveform. This has led to the class J amplifier [11–17], which essentially provides an inductive reactance at the fundamental and a capacitive termination for the second harmonic. The basic schematic of a class J amplifier can be found in Fig. 2.4(a).



(a) Schematic

(b) Time domain

Figure 2.4: Class J schematic and time domain waveforms.

According to [11] the general drain voltage for maximum voltage swing (N=1) can be defined by

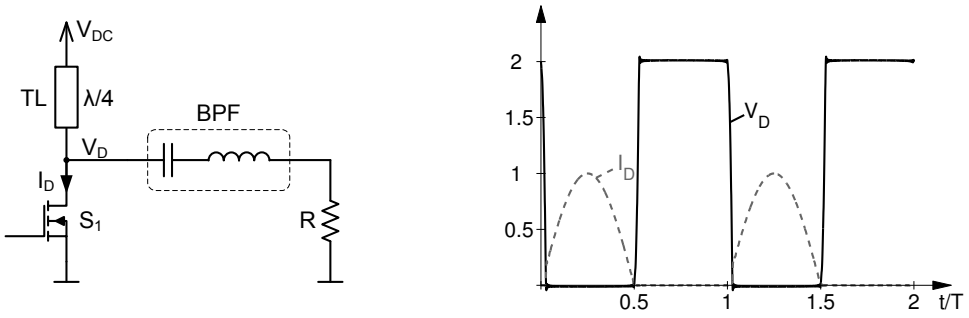
$$V_D = (1 - \beta \cos(\theta))\,(1 - \alpha \sin(\theta))\,, \tag{2.2}$$

while β denotes the maximum voltage swing and the parameter α defines the reactive termination contribution. Fig. 2.4(b) depicts the time domain waveforms for $\beta = 1$ and $\alpha = 1$ as an example. The maximum drain voltage is higher than for the class B operation, where it never exceeds two times the supply voltage. The resulting efficiencies are equivalent to the one of a class B amplifier [11].

2.3 Class F

To achieve higher efficiency than the class B PA the class F circuits use proper higher order terminations to shape the rectangular drain voltage. To achieve this behavior the even order harmonics require a short circuit termination, while the odd order harmonic terminations have to be left open [18–26]. Ideally this is done by means of quarter wave line which can also be used for biasing purposes, as depicted in Fig. 2.5(a). To have an open circuit for the odd order harmonics the load has to be connected by a series resonator. The

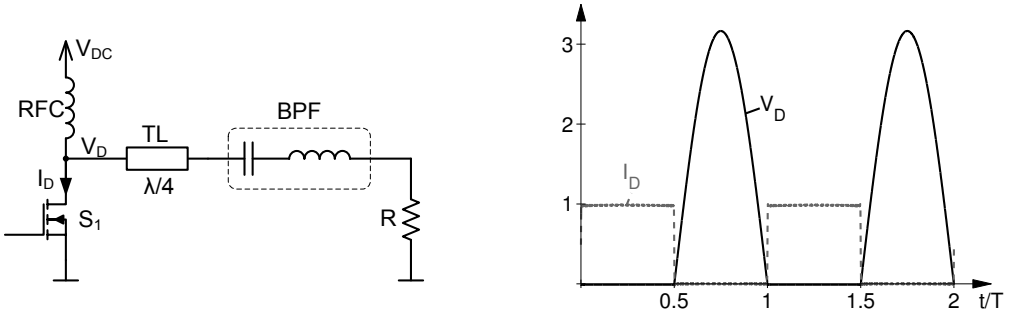
resulting drain current is half sinusoidal, but the drain voltage is rectangular, leading to basically no voltage and current overlap and highly efficient operation. The corresponding time domain waveforms are provided in Fig. 2.5(b).



(a) Schematic (b) Time domain

Figure 2.5: Class F schematic and time domain waveforms.

When exchanging the harmonic terminations and providing an open circuit for all even order harmonics and a short circuit for all odd order harmonics the shape of drain current and voltage are exchanged as well. This leads to the inverse class F amplifier [27–32], whose schematic is depicted in Fig. 2.6(a). The position of the quarter wave line is different compared to the class F PA. The series resonator provides an open circuit at the input of the quarter wave line for all carrier harmonics. This open circuit is transformed to a short circuit for all odd order and remains an open circuit for all even order harmonics. This way the desired harmonic terminations can be achieved. To not interfere with these terminations the biasing is done using an RFC, which provides high impedance for all frequencies except DC. The resulting drain current and voltage waveforms are depicted in Fig. 2.6(b).



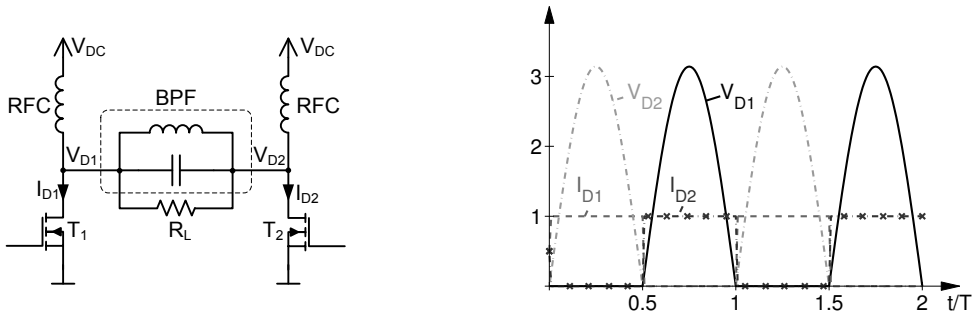
(a) Schematic (b) Time domain

Figure 2.6: Inverse class F schematic and time domain waveforms.

Basically the shapes of drain current and voltage are exchanged compared to the class F PA. The drain current is now rectangular and the drain voltage is half sinusoidal. As there is no overlap of current and voltage also this circuit shows 100 % efficiency in theory. In practice the parasitic capacitance C_{DS} is present and has to be properly compensated for the higher order harmonics to provide the desired terminations and highly efficient operation.

2.4 Class D

Two different versions, namely the current mode and the voltage mode of the class D amplifier exist. The class D amplifier family [33,34] is in general an extension of the class F family to the push-pull configuration. The current mode class D amplifier, whose schematic is depicted in Fig. 2.7(a), basically relates to the inverse class F amplifier. Instead of using a quarter wave line to transform the series resonator of the inverse class F into a parallel resonator, the current mode class D amplifier [35–38] directly uses a parallel resonator located between the two transistors. In practice the load will be connected by a Balanced Unbalanced (BALUN) circuit to provide a single ended output. The even order harmonics of the drain voltage waveform will be canceled out due to the 180 ° out of phase push-pull operation. Therefore no special care about their termination has to be taken.



(a) Schematic

(b) Time domain

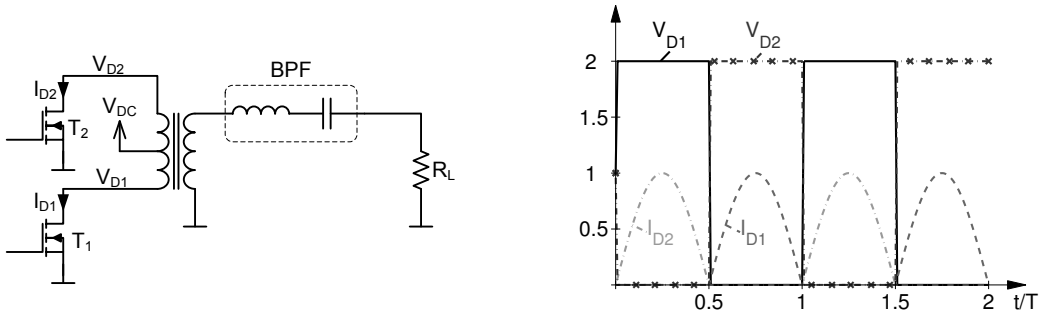
Figure 2.7: Current mode class D schematic and time domain waveforms.

The resulting drain currents are rectangular and the drain voltage waveforms show a half sinusoidal shape, as can be seen in Fig. 2.7(b). The waveforms of a single transistor are essentially the same as for the inverse class F in Fig. 2.6(b) and thus also the current mode class D has a theoretical efficiency of 100 % as ideally there is no overlap of current and voltage on the switch. The general mathematical definition of time domain waveforms can be found in section 7.2. In practice the parasitic drain source capacitance C_{DS}, that would cause switching losses, can be absorbed into the parallel resonator maintaining Zero Voltage Switching (ZVS).

The voltage mode class D amplifier [39–42] uses a series resonator connected via a BALUN instead of the parallel resonator, as depicted in Fig. 2.8(a). The resulting rectangular drain voltage waveform due to the series resonator and the BALUN in push-pull drive can be seen in Fig. 2.8(a). The drain current has a half sinusoidal shape and essentially looks the same as for the class F amplifier.

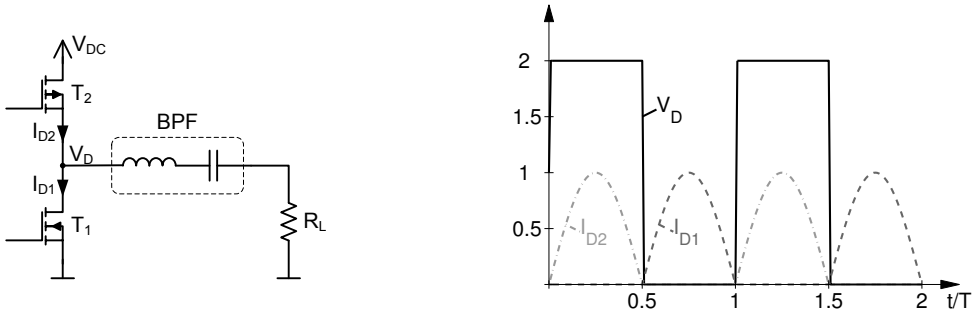
Instead of using a push-pull architecture an inverter based architecture as given in Fig. 2.9(a) can be used [43–50]. The drain voltage is either pulled to ground or to the supply voltage by the transistors forcing a rectangular signal. To not dissipate any energy in the higher order harmonics and to allow for the rectangular drain voltage, the load is decoupled by a series resonator. The resulting drain currents are given in Fig. 2.9(b) and are half sinusoidal and the same as for the conventional voltage mode class D.

The inverter based voltage mode class D has the advantage of directly providing a single ended output signal mitigating the demand for a BALUN. But on the other hand it requires a P-channel high side switch, which is normally avoided due to its worse RF properties compared to N-channel devices. As for RF power transistors usually only the N-channel is available the resulting gate control circuitry for the high side switch will



(a) Schematic (b) Time domain

Figure 2.8: Voltage mode class D schematic and time domain waveforms.



(a) Schematic (b) Time domain

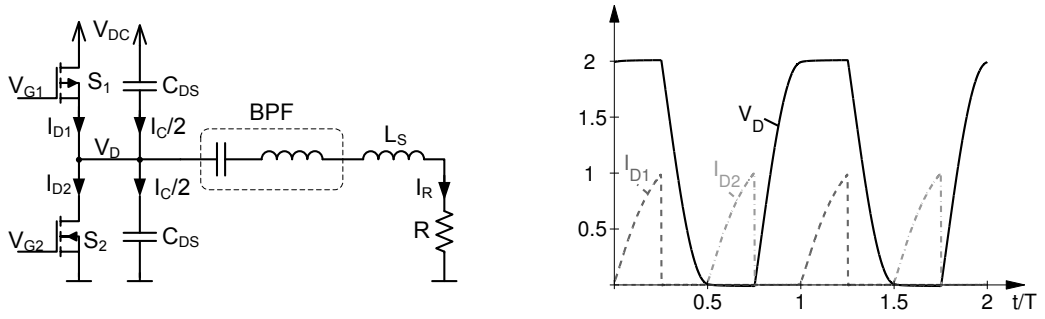
Figure 2.9: Inverter based voltage mode class D schematic and time domain waveforms.

become complex and power consuming. Also the C_{DS} switching losses will degrade the amplifier efficiency in practice.

2.5 Class DE

Instead of charging and discharging the parasitic capacitance C_{DS} actively, which leads to large power dissipation, it can be made an integral part of the operational concept. By introducing a dead time between the two periods and adding a series reactance, as depicted in Fig. 2.10(a), to the load, ZVS can be established. This operational mode is known as the class DE amplifier [51–64]. The parasitic capacitance is now charged and discharged by the load current and not the transistors. Fig 2.10(b) provides the drain currents and voltage waveforms. It can be seen that the drain voltage at the beginning of the ON period already has reached the correct value and ZVS occurs. Also the derivative of the drain voltage is zero at this point in time and thus also Zero Current Switching (ZCS) is possible. Thus no switching losses occur and the circuit allows perfect DC to RF conversion. In section 7.3.2 the derivation of the matching network parameters is provided.

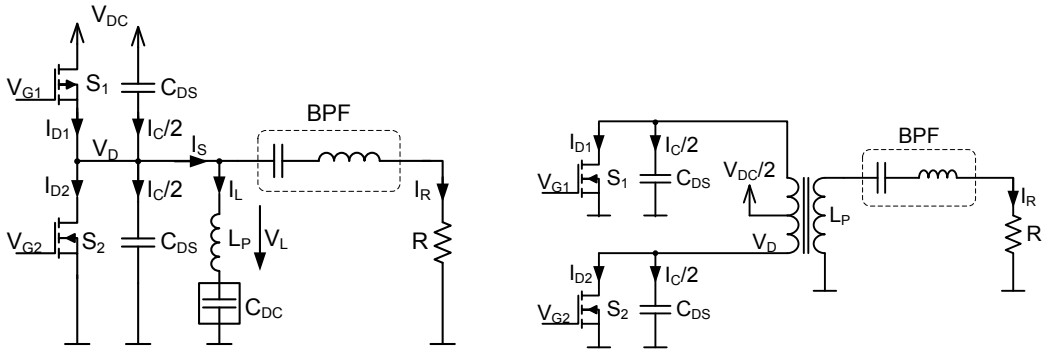
A drawback of the conventional class DE amplifier using a series compensation inductance is its limited load modulation [51] as a certain load current has to flow to charge/discharge the capacitances enabling ZVS. Instead of using a series compensation inductance a parallel inductance as depicted in Fig. 2.11(a) can be used. The corresponding calculation of the parameter values is provided in section 7.3.1. Using the parallel compensation



(a) Schematic (b) Time domain

Figure 2.10: Conventional class DE schematic and time domain waveforms.

inductance offers the possibility of efficient load modulation over a wider dynamic range compared to the conventional class DE amplifier [S1].



(a) Inverter configuration (b) Push-pull configuration

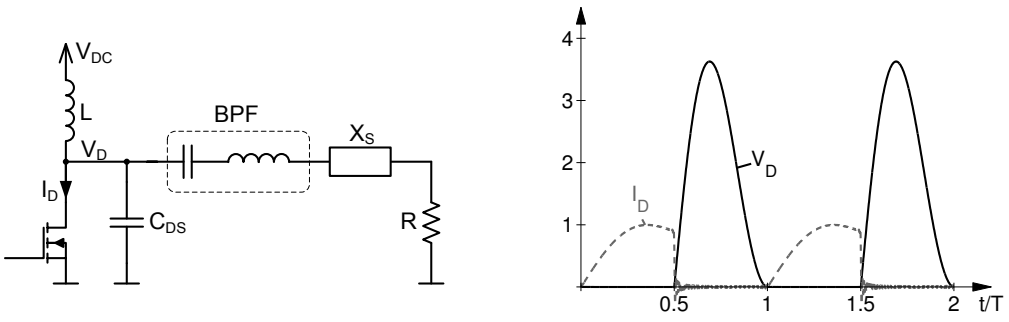
Figure 2.11: Voltage mode class DE using parallel compensation inductance.

The big disadvantage of the circuits in Fig. 2.10(a) and Fig. 2.11(a) is the inverter like structure that requires either complementary transistors or complex and power consuming gate signal generation for the high-side switch. This problem can be solved by using a push-pull variant as depicted in Fig. 2.11(b). It has the advantage of using two low-side switches, which are easier to implement for high frequencies. The disadvantage is that the transformer's parasitic parallel inductance L_P makes the conventional circuit design based on the series compensation inductance more difficult. But this parallel inductance L_P can also be used instead of the series inductance L_S to achieve class DE operation. Therefore the parasitics of the transformer can be absorbed into the matching network and the load modulation properties can be preserved.

2.6 Class E

Since the introduction of the class E amplifier in 1964 [65] its properties and aspects have been studied in numerous papers [66–79]. The basic circuit diagram of the class E PA is given in Fig. 2.12(a). It consists of a biasing inductance L and a shunt capacitance C_{DS}, which may only be the parasitic capacitance of the transistor for high frequency operation. The load R is connected by a series resonator and a series reactance X_S. The values of the elements depend on many design parameters. One of the most important ones is the

q-value, which basically defines the ratio of the resonance frequency of the parallel circuit (L and C_{DS}) to the operational frequency [80–82].



(a) Schematic (b) Time domain

Figure 2.12: Voltage mode class E schematic and time domain waveforms.

The time domain waveforms of the class E amplifier for $q = 1.3$ [81] are depicted in Fig. 2.12(b). When observing the time domain waveforms it can be seen that ZVS and also ZCS occurs, leading to ideally 100 % efficiency. A drawback of the class E amplifier is its relative high peak drain voltage with respect to the DC supply voltage. The maximum drain voltage that occurs is three times larger, or even higher depending on the configuration, than the supply voltage, as can be seen from Fig. 2.12(b).

2.7 Controlled Rectifiers

This section is dedicated to cover the field of circuits for RF rectification [83–89]. Some efficiency enhancement concepts relying on RF energy recovery require efficient rectifiers and therefore it is important to discuss their properties. Several circuit variants will be discussed starting from the basic rectifier circuits and leading to highly efficient switched mode rectifiers.

2.7.1 Class B Rectifier

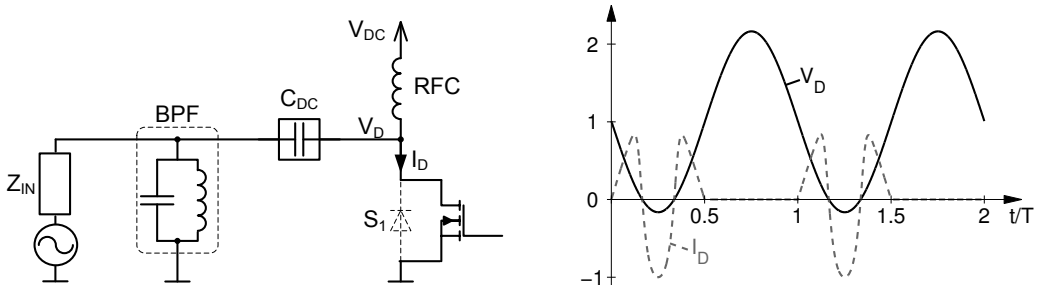
The schematic of the class B rectifier is given in Fig. 2.13. The higher order harmonics are short circuited and the gate is actively controlled in the same manner as for a class B amplifier. The power comes from an RF source showing an input impedance Z_{IN}, which is matched to the transistor properties.

As a result of the active control there is a large overlap of the drain current, especially positive current, which leads to a big power dissipation and low efficiency. Therefore the class B rectifier using active gate control is not a good candidate for efficient RF rectification.

But when using a self aligned diode rectifier, as depicted in Fig. 2.14, the drain current is similar to the one of a class C PA with similar (high) efficiency behavior [88]. This circuit essentially behaves like a common one way rectifier.

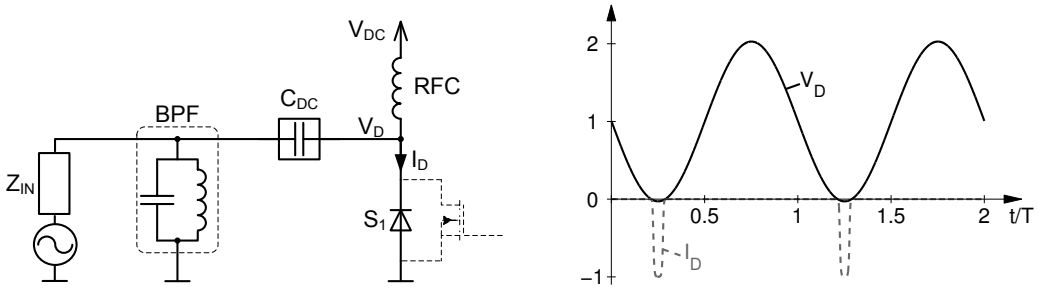
2.7.2 Class D Rectifier

A switched mode PA structure has major advantages in terms of efficiency not only for PAs, but also for rectifier operation. As the drain voltage during the conduction period is



(a) Schematic (b) Time domain waveforms

Figure 2.13: Class B rectifier.



(a) Schematic (b) Time domain waveforms

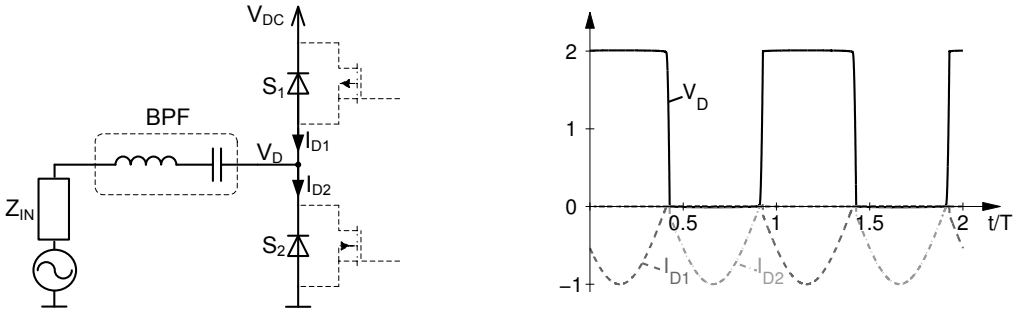
Figure 2.14: Class C rectifier (self aligned diode).

ideally zero, it makes no difference if the drain current is positive or negative. The inverter based class D amplifier is a textbook example of a switched mode PA. Fig. 2.15(a) depicts a class D circuit that can also be used for active or self aligned rectification. From the time domain waveforms in Fig. 2.15(b) it can be seen that the drain currents are negative and thus rectification occurs.

The circuit basically behaves as an ideal full wave rectifier with rectangular drain voltage, which is possible due to the series resonator. As there is no overlap between voltage and current the rectifier is ideally 100 % efficient. In practice the same problems with C_{DS} losses as for the class D PA will occur leading to decreased efficiency. It shall be noted that the current and voltage class D rectifiers are not discussed as they behave similarly to their single ended class F counterparts that will be covered in section 2.7.5.

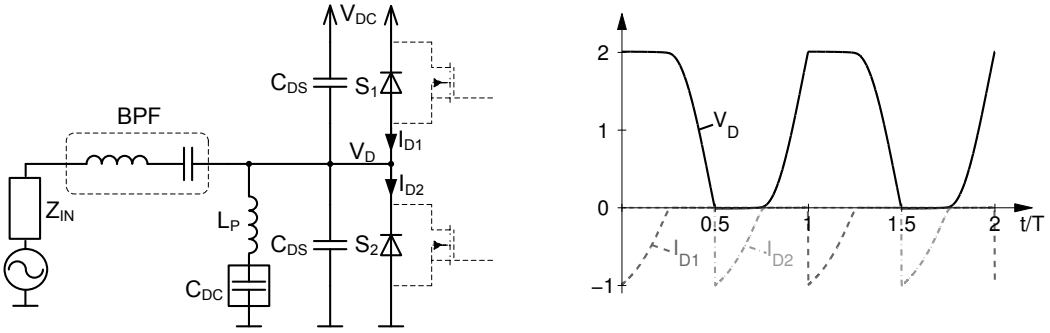
2.7.3 Class DE Rectifier

To overcome the problems with the C_{DS} losses, which impose a major limitation for efficiency, the class DE circuit is a good candidate [90–92]. Its schematic is depicted in Fig. 2.16(a) and its operational principle is already discussed in section 2.5. The main concept is to leave a dead time between the two ON states of the transistor and let the load current charge and discharge the parasitic capacitances. This leads to zero voltage switching and thus no capacitive losses as can be seen in Fig. 2.16(b).



(a) Schematic (b) Time domain waveforms

Figure 2.15: Class D rectifier.



(a) Schematic (b) Time domain waveforms

Figure 2.16: Class DE rectifier.

The time domain waveforms are basically inverted, both in amplitude and time, compared to PA operation (Fig. 2.10(b)) [93, 94]. Only the ON resistance of the switches causes energy dissipation and reduces the theoretical 100 % efficiency.

2.7.4 Class E Rectifier

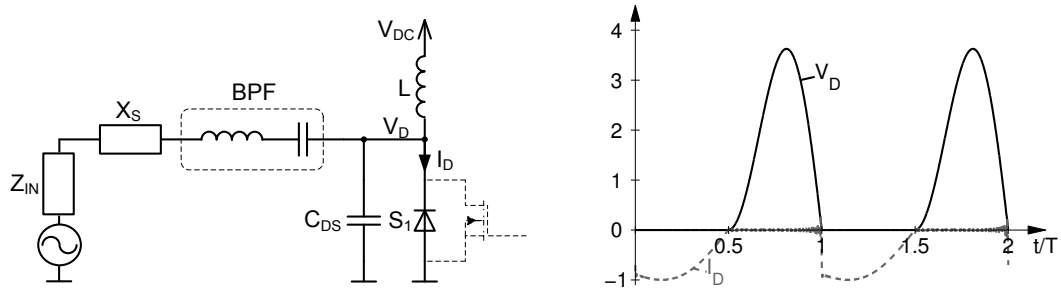
Instead of using two transistors either in push-pull or complementary arrangement it is also possible to achieve perfect RF to DC conversion with a single ended class E circuit [91, 92, 95–98] as depicted in Fig. 2.17(a).

Similar to the class DE rectifier the time domain waveforms are basically inverted both in time and amplitude [93, 94]. Nevertheless there is no overlap between drain current and voltage leading to highly efficient operation.

2.7.5 Class F Rectifier

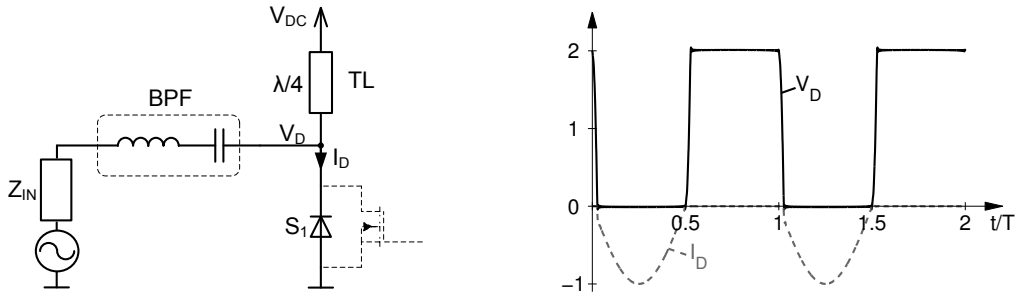
Another single ended circuit besides the class E is the class F circuit family. The schematic of the standard class F rectifier can be found in Fig. 2.18(a). Similar to the class F PA case the time domain waveforms of current and voltage of the class F rectifier are presented in Fig. 2.18(b). These waveforms are similar to the voltage mode class D rectifier.

Beside the class F circuit the inverse class F, as depicted in Fig. 2.19(a), can also be used



(a) Schematic (b) Time domain waveforms

Figure 2.17: Class E rectifier.



(a) Schematic (b) Time domain waveforms

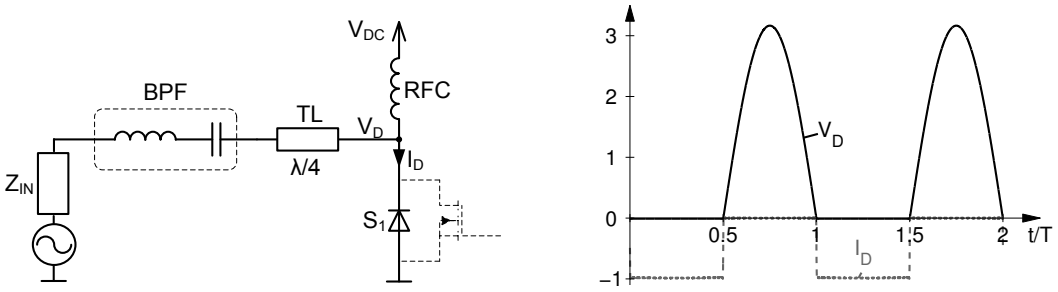
Figure 2.18: Class F rectifier.

[89]. Its harmonic terminations are set to achieve a half sinusoidal drain voltage and a rectangular drain current. This leads to no overlap between drain voltage and current, as depicted in Fig. 2.19(b) and ideally 100 % efficiency.

As the matching network at the fundamental carrier frequency basically behaves like a parallel resonator, which is not desired for some concepts such as BB PWM, it would be beneficial to have a structure that behaves like a series resonator. For inverse class F PAs the matching network can be modified to do so, while maintaining the same drain current waveforms. The resulting PA circuit in Fig. 2.6(a) can also be used in the same way for rectification.

2.8 Comparison

In this section the main circuit parameters of the different PA classes are summarized. They are compared in terms of their maximum efficiency η_{MAX}, maximum drain voltage $V_{D,MAX}$, and their Power Utilization Factor (PUF). The PUF defines the ratio of the output power with respect to the maximum drain current and voltage compared to the class A output power of the same device [10]. In addition the mode of operation (linear or switched) is indicated by the field Switched Mode Power Amplifier (SMPA). The circuits abilities to operate also as rectifier are evaluated as well. The results are summarized in Tab. 2.1 below.



(a) Schematic

(b) Time domain waveforms

Figure 2.19: Inverse class F rectifier.

class	η_{MAX}	SMPA	$V_{D,MAX}$	PUF	rect
A	50 %	no	$2V_{DC}$	1	no
B	78.5 %	no	$2V_{DC}$	1	$\sim$
C	<100 %	no	$2V_{DC}$	«1	yes
J	78.5 %	no	$>2V_{DC}$	1	$\sim$
CM D	100 %	yes	πV_{DC}	$4/\pi$	yes
VM D	100 %	yes	$2V_{DC}$	$4/\pi$	yes
DE	100 %	yes	$2V_{DC}$	$<4/\pi$	yes
E	100 %	yes	$3\text{-}4V_{DC}$	<1	yes
F	100 %	yes	$2V_{DC}$	$4/\pi$	yes
F^{-1}	100 %	yes	πV_{DC}	$4/\pi$	yes

Table 2.1: Overview amplifier classes.

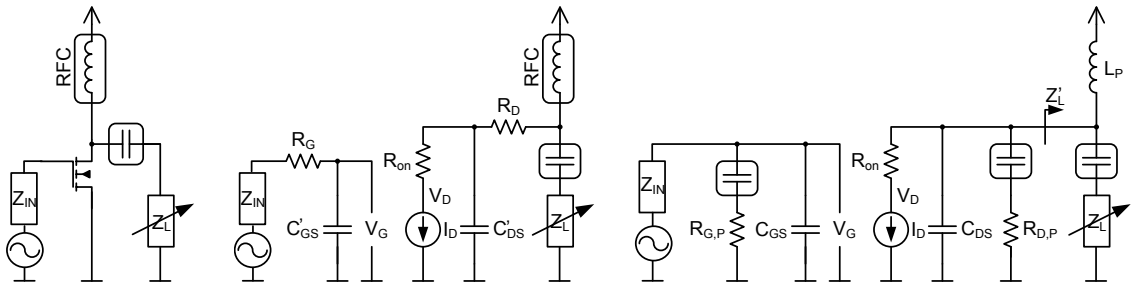
2.9 Loss Mechanisms RF Transistors

In this section the main loss mechanisms and their impact on the load pull contours will be discussed. A particular focus is set on the influence on the load modulation capabilities, as this is an important property for several efficiency enhancement techniques such as Doherty or Chireix PAs. Based on a simplified transistor model the influence of the R_{on}, the biasing current, parasitics Q-factor and parallel losses as well as the gain are presented.

When performing a load pull, amplifier parameters like efficiency output power and gain are evaluated over a range of different load impedances. Therefore, the load impedance is modified as depicted in Fig. 2.20(a). The resulting contours are usually plotted in a smith chart to easily identify the spots of maximum power or efficiency.

For the PA a simple model, as depicted in Fig. 2.20(b) is considered [S2]. It consists of the gate input with its parasitic capacitance C'_{GS} and series resistance R_G. The gate voltage V_G controls the drain current I_D source which forms together with its R_{on} the intrinsic transistor. Additionally, the drain source capacitance C'_{DS} and the drain resistor R_D are considered.

The higher order harmonics are assumed to be short circuited such that class B operation occurs. For the calculation of the intrinsic transistor losses P_T the equations derived in Appendix 7.1 are considered. The corresponding efficiency of the intrinsic transistor can



(a) Load pull (b) Transistor model (c) Modified transistor model

Figure 2.20: Load pull setup and transistor model.

be calculated by

$$\eta_D = \frac{P_L}{P_L + P_T}. \tag{2.3}$$

The effect of R_{on}, respectively the knee voltage can be considered by

$$\eta_{knee} = \frac{R_L}{R_L + R_{on}(k,n)}. \tag{2.4}$$

The effective R_{on} depends on the biasing (k) and the normalized drive level (n). Therefore, it is easier to reduce the normalized drain voltage swing N and current n in (7.6) accordingly to account for the drain efficiency degradation.

The drain resistance $\mathrm{R_D}$ defines the Q-factor of the parasitic drain source capacitance $\mathrm{C_{DS}}$ and will for this analysis be parameterized by it. In order to ease the calculation of the influence of $\mathrm{C_{DS}}$ and the series resistor $\mathrm{R_D}$ on the efficiency, they can be transformed into a parallel circuit as depicted in Fig. 2.20(c). Although mathematically not 100 % correct, it was found to be a good approximation [99]. The resulting parallel shunt resistance is DC wise decoupled to avoid static losses and may also be modified to account for substrate losses [100]. The efficiency degradation due to the equivalent parallel resistor $\mathrm{R_{D,P}}$ of $\mathrm{C_{DS}}$ can be calculated by

$$\eta_P = \frac{R_{D,P}}{R_{D,P} + R_{L,P}}, \tag{2.5}$$

where $\mathrm{R_{L,P}}$ denotes the effective parallel load resistance of $\mathrm{Z_L}$.

The influence of the gain on the PAE can be accounted for by

$$\eta_G = 1 - \frac{1}{G}. \tag{2.6}$$

To discuss the impact of the mentioned parasitics a frequency of 2.65 GHz, a normalized capacitance $\mathrm{C_{DS}}$ per maximum current of 1.65 pF/A and a Q-factor of 40 for $\mathrm{C_{DS}}$ were selected.

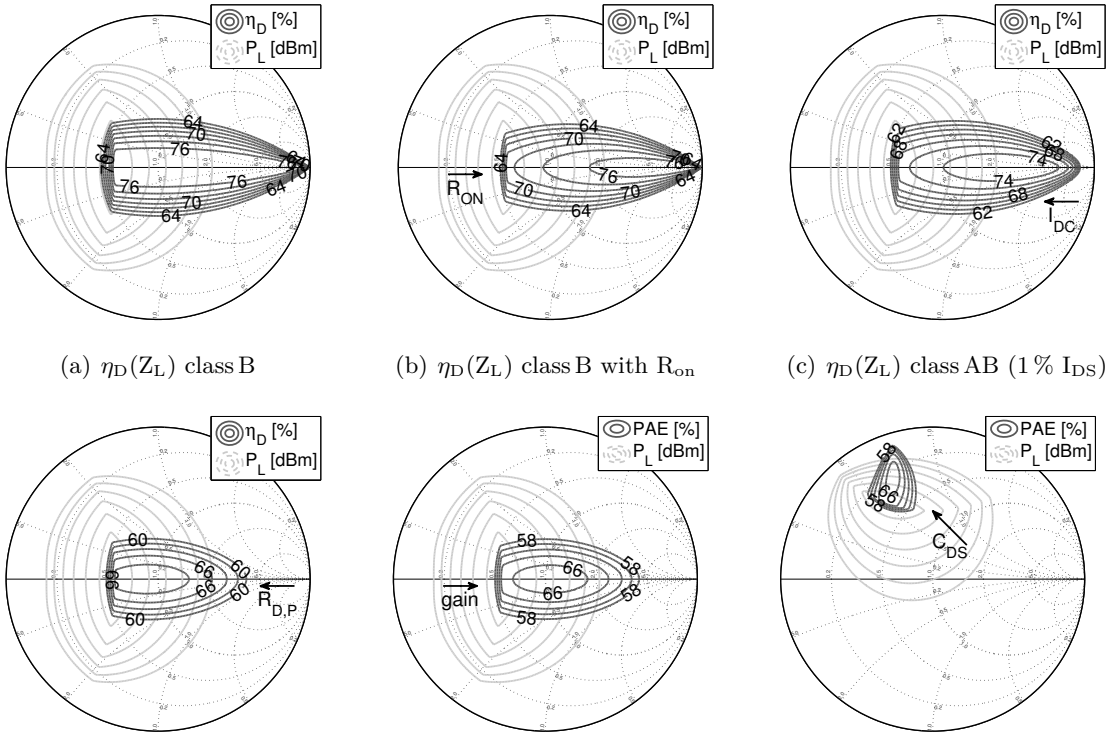
The knee voltage was assumed to have 10 % of the nominal supply voltage (28 V). The biasing inductance $\mathrm{L_P}$ in Fig.2.20(c) is set to resonate $\mathrm{C_{DS}}$ out such that the resulting load pull contours are symmetrical around the real axis.

The influence of the different effects on the load pull contours is depicted in Fig. 2.21. In Fig. 2.21(a) the impact of the ON resistance of the transistor can be seen. Ideally any load resistance large enough to get maximum voltage swing would result in the theoretical class B efficiency of 78.5 % (Fig. 2.21(a)). But the ON resistance of the transistor reduces the efficiency, especially for smaller load resistor values (higher power). Thus the ON

resistance of the transistor moves the points of maximum power and efficiency apart. This can be seen in Fig. 2.21(b), which depicts the drain efficiency for class B biasing considering the ON resistance, respectively knee voltage. It can be seen that for very large resistance values towards the open circuit maximum efficiency is achieved.

Considering a realistic biasing with 1 % quiescent current (or leakage) reduces the efficieny for very high resistance values. Fig. 2.21(c) illustrates this effect.

Beside the biasing, the influence of the parallel resistor $R_{D,P}$, which accounts for the losses due the limited Q-factor of C_{DS}, significantly reduces the range of impedances for high efficiency operation. In Fig. 2.21(d) the influence of this effect is shown. It can be seen that the region of highest efficiency has shrunk and its maximum is reduced. The Q-factor of C_{DS} might in practice be further reduced by any series resistance (eg. bondwires). Also the biasing inductor will have a limited Q in practice. It shall be noted that the Q-factor of 40 was chosen as an example and may vary according to transistor technology, generation and operational frequency.



(a) $\eta_D(Z_L)$ class B (b) $\eta_D(Z_L)$ class B with R_{on} (c) $\eta_D(Z_L)$ class AB (1 % I_{DS})

(d) $\eta_D(Z_L)$ class AB C_{DS} losses (e) PAE(Z_L) class AB (f) PAE(Z_L') class AB (with L_P

Figure 2.21: Theoretical load pull contours and impact of loss mechanisms.

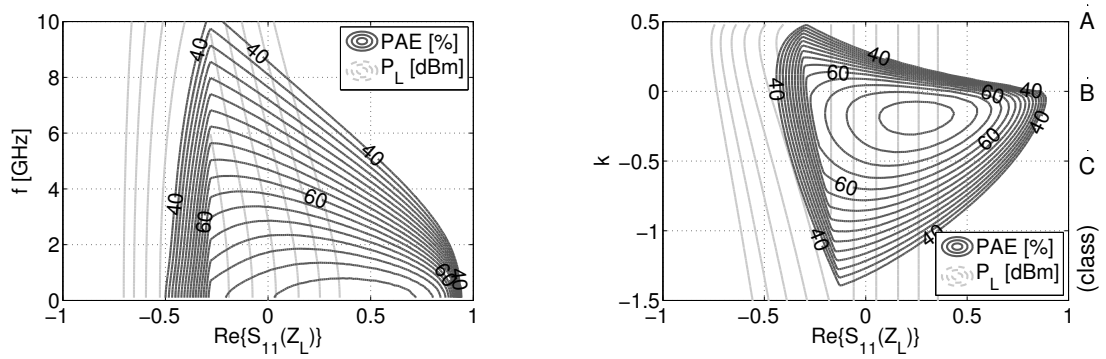
When considering the gain, which has an influence on the PAE, the efficiency contours are shifted again towards higher impedance values, as can be seen in Fig. 2.21(e).

The drain biasing with L_P is in practice ascribed to the matching network and usually considered as a part of the load impedance. Fig. 2.21(f) shows its influence on the position of the load pull contours.

It can be summarized that the ON resistance of the transistor and the gain basically move the point of maximum efficiency towards higher resistance values. This behavior is beneficial for systems that rely on load modulation such as the Doherty amplifier. These systems require high efficiency over a wide range of load impedances to work properly. Unfortunately the biasing current and especially the Q-factor of the parasitic drain capacitance C_{DS} limit this range significantly. Thus it can be said that the Q-factor of the parasitic

capacitance plays an important role for the load modulation capabilities of a transistor and it imposes a limit for the high efficiency region.

Beside the behavior at a single frequency the evolution of the PAE versus frequency is interesting to observe. Therefore, Fig. 2.22(a) depicts the PAE as a function of the real valued axis of the load reflection coefficient and the frequency. It can be seen that for very low frequencies the transistor operates efficiently over a wide range of impedances. In this region the transistor may be oversized to reduce the influence of the knee voltage and to achieve better efficiency. But when moving to higher frequencies the maximum efficiency region is significantly reduced, moving it close to the maximum output power. This trend highlights that using a larger transistor to reduce the impact of R_{ON} becomes ineffective at higher frequencies. The fact that the region of highest efficiency is reduced for higher frequencies reduces the useful load modulation range and thus limits the achievable efficiency enhancement.



(a) PAE versus frequency

(b) PAE versus bias

Figure 2.22: Theoretical efficiency versus sweep parameters.

Reducing the conduction angle from class B to class C is a way to improve the drain efficiency. Fig. 2.22(b) depicts the influence of the biasing on the PAE. It presents the dependency of the efficiency on the real axis of the load reflection coefficient for a carrier frequency of 2.6 GHz versus different biasing conditions. It can be seen that the efficiency maximum occurs for slight class C biasing. For class B operation (k=0) the efficiency is only slightly smaller, while it is significantly reduced for class A (k=0.5) operation. From Fig. 2.22(b) it can be concluded that deep class C biasing is not useful, as the C_{DS} related losses ($R_{D,P}$) and the reduced gain lower the PAE.

2.10 Average Efficiency

In this section the calculation of the average drain efficiency under excitation with modulated signals will be discussed. Additionally the design requirements to achieve good average efficiency will be conducted.

The average efficiency can be calculated according to (2.7) [101].

$$\eta_{\mathrm{AVG}} = \frac{\int_0^{V_{max}} V^2 \mathrm{pdf}(V) dV}{\int_0^{V_{max}} \frac{V^2}{\eta(V)} \mathrm{pdf}(V) dV} = \frac{\int_0^{V_{max}} \mathrm{w}(V) dV}{\int_0^{V_{max}} \frac{\mathrm{w}(V)}{\eta(V)} dV}, \tag{2.7}$$

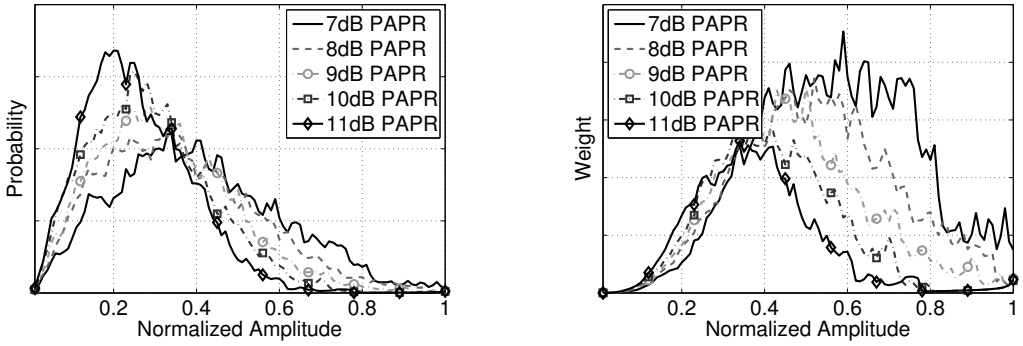
where V_{max} denotes the maximum voltage and pdf(V) the amplitude Probability Density Function (PDF) of the modulation signal. The numerator of the equation normalizes the

result, while the denominator depends on the PDF and the weighting function

$$\mathrm{w}(V) = V^2 \mathrm{pdf}(V). \tag{2.8}$$

A large weighting function indicates the regions which contribute the most to the average efficiency. Therefore high efficiency within this regions is important for the average efficiency.

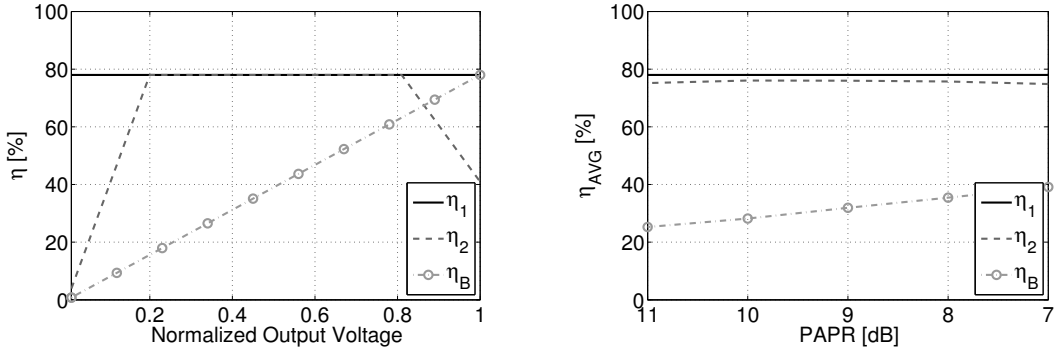
Fig. 2.23(a) provides PDFs with different PAPRs. The corresponding weighting functions for are plotted in Fig. 2.23(b).



(a) PDF (b) Weight

Figure 2.23: Probability density and resulting weighting functions.

From Fig. 2.23(b) it can be seen that the region of intermediate output power is most important for the average efficiency. To show these three different efficiency curves are considered in Fig. 2.24(a). A class B efficiency curve η_{B}, a constant efficiency η_1 and efficiency curve η_2 adapted to the weighting function are considered.



(a) η PA (b) η_{AVG}

Figure 2.24: Example efficiency functions and resulting average efficiency.

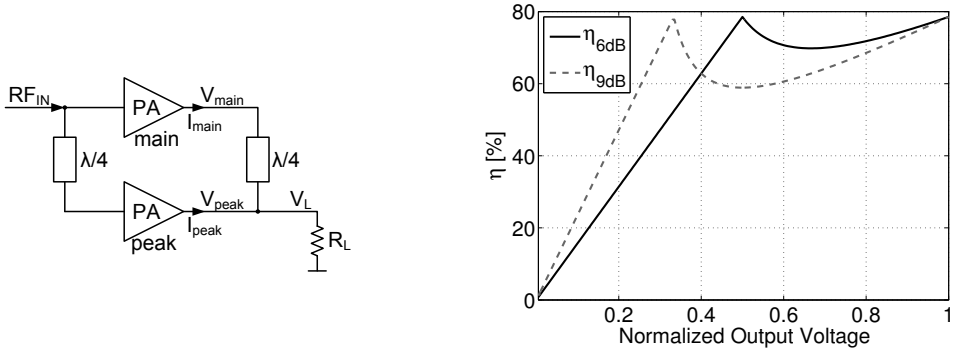
The resulting average efficiencies versus different PAPRs are depicted in Fig. 2.24(b). It can be seen that the average efficiency for the class B amplifier heavily depends on the PAPR, while the constant efficiency curve η_1 is not at all affected by the PAPR of the signal. But also the efficiency curve η_2 optimized for the weighting function barely varies with the PAPR and is only slightly smaller than the maximum efficiency η_1. Thus neither the efficiency at peak power nor for very low output powers have a big impact on the average efficiency. It can be concluded that the intermediate region for a normalized signal magnitude between 0.2 and 0.8 is most important for the average efficiency and should be optimized in amplifier designs.

3. Efficiency Enhancement Concepts

In this chapter several efficiency enhancement concepts will be discussed, briefly touching well established concepts such as Doherty and Chireix but also covering topics like envelope tracking. Emphasis is put on the theory of Base Band Pulse Width Modulation (BB PWM), which is often also referred to as burst mode. In that context a particular focus is set on the effects and perspectives of isolated load and direct filter connection. The properties of multilevel and multiphase structures will also be covered. Additionally, several concepts of energy recovery methods are evaluated. Finally, the theoretical background of RF PWM operation is presented. It shall be noted that for a fair comparison a class B maximum efficiency is assumed for all concepts unless otherwise noted.

3.1 Doherty

The concept of the Doherty amplifier exists for many decades and was introduced by W. H. Doherty in 1936 [102]. Recently the Doherty PA is experiencing a revival [103–107]. Several different variants exist reaching from integrated Doherty PAs [108–113] to highly efficient circuits using class E [114, 115] or class F [116–118] amplifier concepts at high output power levels. Further improvement is made by using separate controlled inputs [119,120] or even going to 3 way [121–123] or 4 way architectures [124]. The basic circuitry is depicted in Fig. 3.1(a) and essentially consists of two amplifiers connected by a quarter wave line.

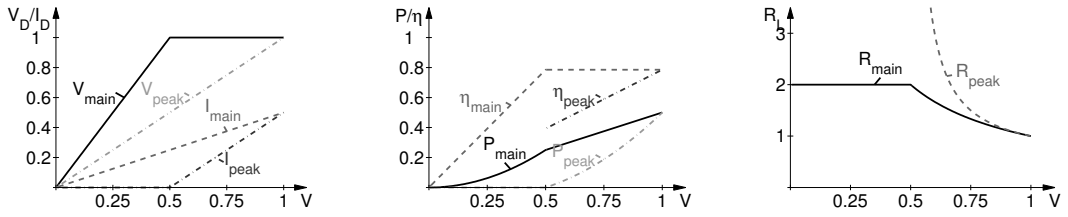


(a) Block diagram

(b) Efficiency

Figure 3.1: Doherty block diagram and efficiency.

The upper main amplifier is constantly active and the peak amplifier is only activated for higher powers and performs load modulation of the main PA enabling efficient operation. For low power only the main PA is active and the peak PA ideally provides an open circuit not influencing the operation. The impedance of the quarter wave line is set such that the main PA sees twice its optimum load impedance for this operational region. When increasing the drive of the main PA its drain current I_{main} continuously increases as depicted in Fig. 3.2(a). The drain voltage V_{main} raises accordingly until the main PA saturates. In this region the PA behaves like a regular class AB amplifier, as its load resistance remains constant (Fig. 3.2(c)).



(a) Block diagram (b) Power and efficiency (c) Load resistance

Figure 3.2: Doherty control, output power and partial efficiency.

Once the main PA is saturated, the peak PA starts operating and provides additional output power. Its current contribution I_{peak} at the summation point increases the total load current and hence the load voltage, respectively the peak amplifier's drain voltage. The load current contribution of the main PA remains constant. Due to the quarter wave line the drain voltage of the main PA stays constant and the saturated operation condition is kept. On the other hand the drain current of the main PA increases with higher load voltage swing, leading to linearly increased power contribution of the main PA, as depicted in Fig. 3.2(b). The efficiency of the main PA remains at its maximum in this region, as the main PA experiences maximum drain voltage swing. When the peak PA starts to operate its efficiency is low, as the voltage swing is limited, but the efficiency linearly increases with the load voltage. In the back off range the power contribution of the peak PA compared to the main PA is small and its lower efficiency has only a limited impact on the overall efficiency curve depicted in Fig. 3.1(b). This way highly efficient operation over a wide power range is possible.

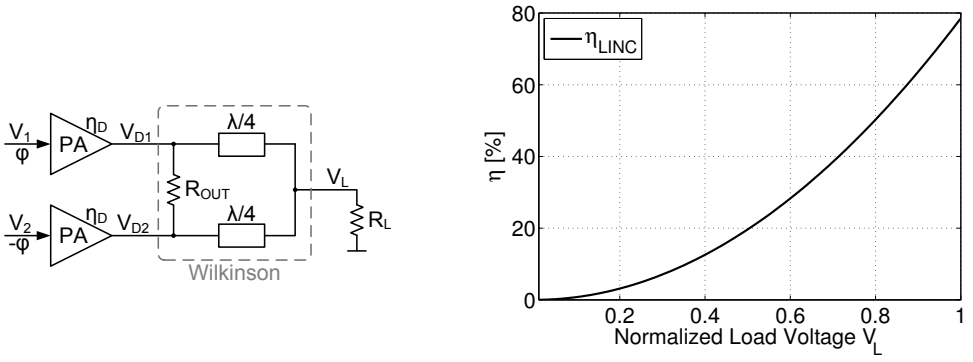
3.2 Linear Amplification Using Nonlinear Components

The concept of Linear Amplification Using Nonlinear Components (LINC) is based on two amplifiers, whose powers are combined using an isolated combiner [125]. The PAs are operated in saturation and the output power is controlled by modifying the phase φ of the two PAs with respect to each other [126]. Fig. 3.3 depicts the block diagram of a LINC transmitter using a Wilkinson combiner to provide isolation. Due to the isolated combining scheme the load impedance for each PA remains constant regardless of the driving conditions. This leads in combination with the saturated drive of the PAs to a constant output power with high drain efficiency. While the in-phase power is transfered to the load, the out of phase components are dissipated in the resistor R_{OUT}. A result of the constant input power is the rather poor efficiency curve that depends in a square relation to the output voltage, as depicted in Fig. 3.3(b).

To improve this efficiency curve several different architectures based on multiple levels for the outphasing operation are known. One way is to reduce the input drive [127], which results in a class B efficiency trend. Using multiple supply levels on the other hand results in high efficiency for the different levels [128]. By also using asymmetric supply combinations [129–132] the number of levels and thus the efficiency can be enhanced.

3.3 Chireix

The Chireix combiner was proposed by H. Chireix in 1935 [133]. Instead of using an isolated combiner structure as for LINC the Chireix combiner uses the interaction of both PAs, which results in load modulation for the single branches. The basic arrangement



(a) Block diagram (b) Efficiency

Figure 3.3: LINC.

[134–140] is shown in Fig. 3.4(a) and consists of two PAs connected to the common load by two quarter wave lines. The PAs are operated in saturation by keeping the drain voltage constant. The output power is controlled by modifying the relative phase φ of the control signals.

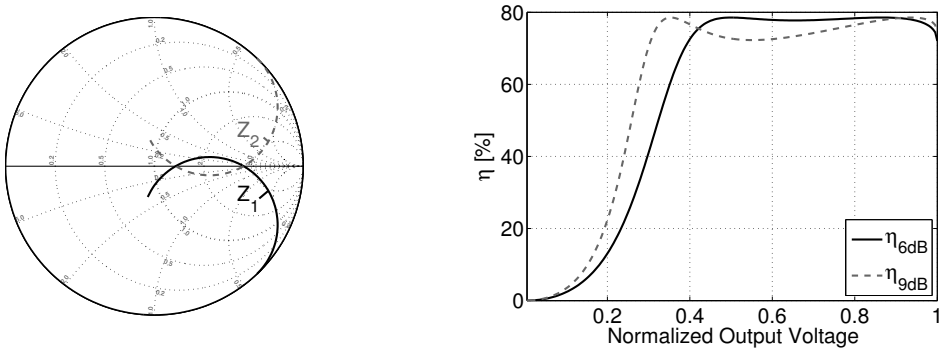
When using only quarter wave lines the resulting impedances for each PA branch shows a significant reactive component causing overlap of drain current and voltage and leading to efficiency degradation. In order to compensate for this reactive components the shunt reactances X_P, as depicted in Fig. 3.4(a), are employed.

(a) Conventional (b) Simplified

Figure 3.4: Chireix block diagram.

The resulting impedance trajectories for the single PA branches exemplified for an efficiency peak at 6 dB back off are provided in Fig. 3.5(a). It can be seen that due to the shunt compensation reactances the load modulation trajectories are close to the real axis, enabling efficient operation [141]. The component values for the efficiency peak at distinct back off values have been determined using the equations derived in section 7.6.1. The corresponding efficiency curve for 6 dB as well as for 9 dB back off are plotted in Fig. 3.5(b).

Instead of using shunt elements X_P, which can be lossy in practice, the Chireix combiner can also be built by using series transmission lines only [142], leading to an architecture as depicted in Fig. 3.4(b). The load modulation behavior for proper dimensioning (see section 7.6.2) is exactly the same as for the conventional Chireix architecture shown in Fig. 3.4(a). A drawback of the Chireix, as well as the LINC, is the fact that the generation of low output signals is based on cancellation and that they are therefore very sensitive to parameter mismatch (supply, TL, phase). This leads to a limited dynamic range (see section 7.6.3). Using the outphasing approach until the maximum efficiency in back off is reached and then lowering the drive level to achieve low output powers has advantages both in terms of dynamic range and efficiency [143].



(a) Load modulation trajectories (b) Efficiency

Figure 3.5: Chireix load modulation trajectories and efficiency.

Practical applications of the Chireix combiner reach from low power CMOS circuits [40, 144] over high power systems using class E PAs [77,145,146] to 4 way combiners [147–149].

3.4 Envelope Tracking / Envelope Elimination and Restoration

Another way to improve amplifier efficiency is to modify the supply voltage according to the output power in order to reduce current and voltage overlap. In general two concepts, namely Envelope Tracking (ET) [150–155] and Envelope Elimination and Restoration (EER) [156–158], exist. EER was suggested by R. Kahn in 1952 [159,160] and is therefore often referred to as Kahn transmitter. Both concepts ET, as depicted in Fig.3.6(a), and EER, as shown in Fig. 3.6(b), essentially rely on the use of an envelope PA, which modifies the supply voltage of the actual PA according to the output of the Envelope Detector (ED). This way the PA is always operated with maximum voltage swing and thus maximum efficiency. The main difference between ET and EER lies in the input signal generation. For envelope tracking the amplitude information is still contained in the PAs driving signal. This leads to a combined control of the output power by the envelope PA and the driving signal. For EER the amplitude information is only controlled by the envelope PA and the driving signal only contains the phase information φ extracted by the limiter.

(a) ET (b) EER

Figure 3.6: Block diagrams of envelope tracking and envelope elimination and restoration.

In practical implementations the required bandwidth of the envelope PA due to bandwidth expansion of the envelope signal imposes a challenge. Also the fact that the system efficiency is the combined efficiency of envelope and regular PA tightens the requirements.

3.5 Load Modulation

Instead of changing the supply voltage it is also possible to modify the load impedance to control the output power. The general block diagram for load modulation is provided in Fig. 3.7. The impedance Z_L provided to the PA is varied by tuning the Output Matching Network (OMN) [17,161–171]. This way the power delivered to the load can be controlled. In practice the variable matching network is mainly implemented using varactors, which require control signals with very high voltage swings and complex control circuitry. Also the synthesis of broadband load modulation networks imposes a big challenge.

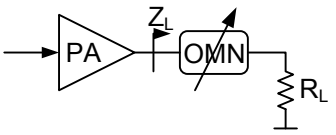


Figure 3.7: Load modulation block diagram.

3.6 Base Band PWM

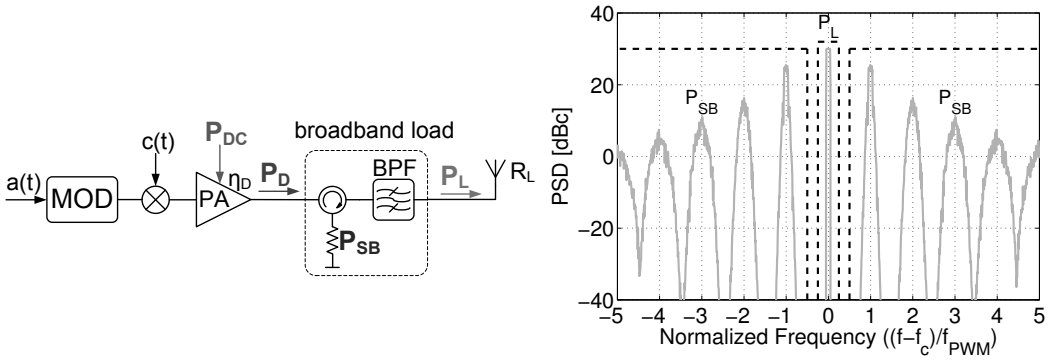
In this section the concept of Base Band Pulse Width Modulation (BB PWM) will be introduced. First the properties of BB PWM using an isolated combiner and single level PA will be discussed. Furthermore, the perspectives of direct filter connection based on a series or parallel resonator will be covered. Different multilevel PA structures and their behavior in combination with BB PWM is treated. In addition the multiphase concept is introduced and compared to the multilevel approach.

3.6.1 Isolated Broadband Load

The efficiency of conventional amplifiers is significantly reduced for lower output powers. One way to overcome this efficiency degradation is to drive the PA only at its most efficient operating points when the transistor is either working close to saturation with maximum voltage swing and thus maximum efficiency or completely switched off, not dissipating any power at all [38, 172–174]. To drive the PA in such a way a special modulator arrangement, as depicted in Fig. 3.8(a) is required. The input amplitude a(t) is encoded in the MODulator (MOD) by means of Pulse Width Modulation (PWM) and upconverted using the Local Oscillator (LO) signal c(t). The phase information is introduced by (phase) modulating the carrier signal c(t).

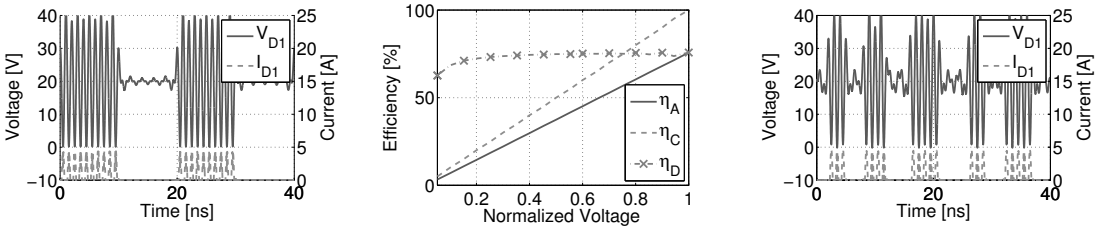
Unfortunately the PWM introduces modulation sidebands close to the desired inband signal, as shown in Fig. 3.8(b) depicting the Power Spectral Density (PSD) versus the normalized modulation frequency. To only transmit the desired information a BPF is used to filter out the inband signal. In order to avoid any feedback of the filter to the PA and to provide a broadband load, a circulator configured as isolator, as depicted in Fig. 3.8(a), can be used. This way a perfect match not only for the inband signal, but also for the modulation sidebands is provided.

Fig. 3.9(a) depicts the drain voltage waveforms for a class B PA with broad band load under PWM excitation with 50 % duty cyle. During the first period (ON) the PA is operated with maximum drain voltage swing and thus maximum power and efficiency. During the second period (OFF) the PA is switched off and no power is dissipated at all, as no drain current is flowing. The information is now encoded in the bursts at the drain of the transistor, therefore this type of operation is also referred to as burst mode operation.



(a) Block diagram (b) Spectrum

Figure 3.8: Block diagram of broadband load operation.



(a) PWM time domain (b) Efficiency (c) ΔΣ time domain

Figure 3.9: Drain voltage and current for PWM and ΔΣ operation for an isolated load and efficiency.

By using this efficient coding scheme high drain efficiency of the PA can be achieved. The drain efficiency η_D is defined as

$$\eta_D = \frac{P_D}{P_{DC}}, \tag{3.1}$$

where P_D denotes the total power delivered from the drain to the (broadband) load and P_{DC} is the total DC power consumption. It shall be noted that the total power delivered from the drain does not only include the inband power delivered to the load, but also the energy of the modulation sidebands dissipated in the termination resistor.

Although the drain efficiency is high, the total efficiency curve of the amplifier η_A, as depicted in Fig. 3.9(b), degrades to the one of a class B amplifier. This is caused by the fact that also the modulation sidebands see the optimum load impedance and thus their power (P_{SB}) is dissipated in the sideband termination resistor. The coding efficiency defined by (3.2) describes this effect by taking the ratio of the power delivered to the load P_L versus the power delivered from the PA P_D into account.

$$\eta_C = \frac{P_L}{P_D} \tag{3.2}$$

As a significant amount of energy is dissipated in the modulation sidebands, the calculation of the coding efficiency, as provided in section 7.4, results in a linear dependence on the generated load voltage. Therefore the overall amplifier efficiency, which is defined as

$$\eta_A = \eta_D \eta_C, \tag{3.3}$$

is significantly reduced. Although the PA itself is operated highly efficient, the class B efficiency trend is not exceeded.

It shall be noted that the above considerations are also valid for $\Delta\Sigma$ noise shaping, if all spectral components see the optimum load impedance. Exemplary time domain waveforms for 50 % relative output voltage and $\Delta\Sigma$ operation are plotted in Fig. 3.9(c).

3.6.2 Direct Filter Connection

To mitigate the losses in the modulation sidebands, the isolator can be removed connecting the filter directly [175–179]. The BPF can either be implemented as a series or parallel resonator, each of them showing different effects. Their properties will be discussed in the following two subsections. In addition, the possible efficiency enhancement by combining the series resonator with a switch is also covered.

3.6.2.1 Parallel Resonator

The use of a parallel resonator results in the block diagram depicted in Fig. 3.10.

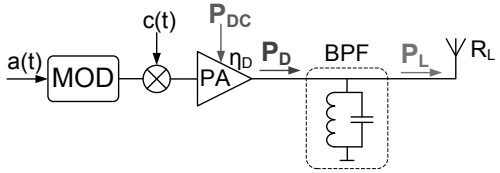
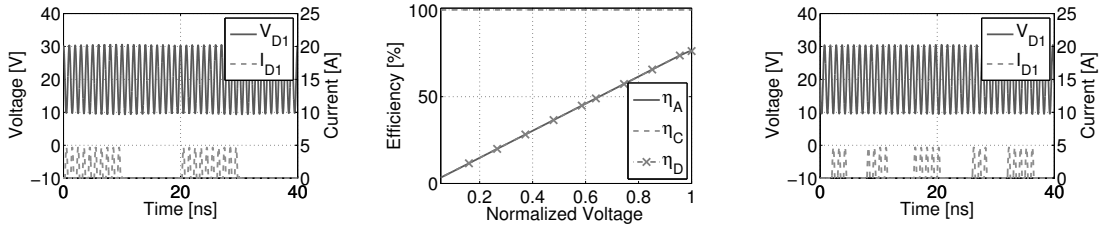


Figure 3.10: Block diagram of direct filter operation.

The parallel resonator provides a short circuit for the modulation sidebands and causes the drain voltage to be demodulated. This can be seen in Fig. 3.11(a), which depicts the drain voltage and current for a 50 % duty cycle signal. The drain current pulses are demodulated by the parallel resonator resulting in a constant drain voltage. This constant drain voltage results in an overlap of voltage and current for lower output powers and degrades the drain efficiency. Fig. 3.11(b) shows the corresponding efficiency curves. The coding efficiency is high, as no energy is dissipated in the modulation sidebands, but the drain efficiency is degraded leading to a class B like overall performance.



(a) PWM time domain (b) Efficiency (c) $\Delta\Sigma$ time domain

Figure 3.11: Drain voltage and current for PWM and $\Delta\Sigma$ operation for a parallel filter and resulting efficiency.

Using $\Delta\Sigma$ envelope coding, as depicted in Fig. 3.11(c), shows essentially equal behavior, leading to the same efficiency performance in Fig. 3.11(b).

3.6.2.2 Series Resonator

Instead of the parallel resonator its series counterpart, as depicted in Fig. 3.12, can be employed.

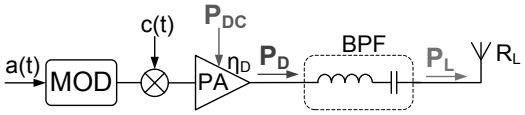
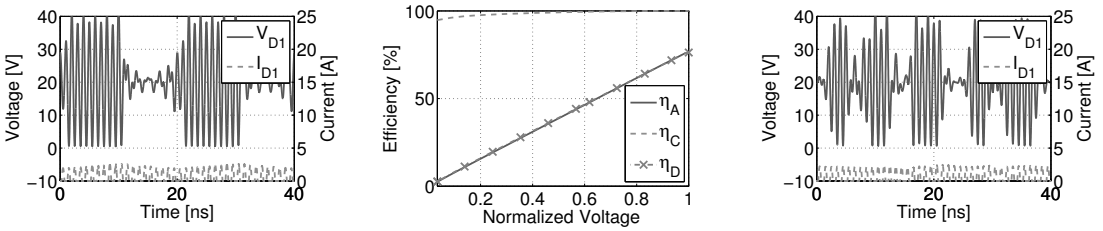


Figure 3.12: Block diagram of direct filter operation.

The series resonator causes the current to be constant within one period, while the drain voltage can be shaped to follow the desired modulation. This can be seen in Fig. 3.13(a), which shows the drain voltage and current for direct filter connection of a series resonator. During the first period the voltage swing is at its maximum enabling highly efficient operation. Due to the series resonator the current also has to flow during the second period. This results in a large overlap of current and voltage and leads to high power dissipation. Although the coding efficiency η_C is theoretically 100 % the overall amplifier efficiency is degraded to the one of a class B amplifier, as can be seen in Fig. 3.13(b).



(a) PWM time domain (b) Efficiency (c) ΔΣ time domain

Figure 3.13: Drain voltage and current for PWM and ΔΣ operation for the series filter and efficiency.

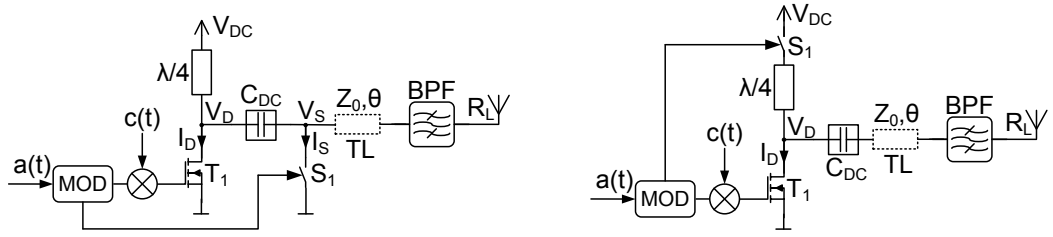
It shall be noted that the presented efficiency considerations are also valid for ΔΣ operation, as depicted in Fig. 3.13(c).

3.6.2.3 Series Resonator with Switch

When observing the drain voltage and current waveforms of the series filter connection in Fig. 3.13(a) it can be seen that during the second period no power is generated as there is no voltage swing. On the other hand the series resonator requires a continuous current. The resulting overlap causes only power dissipation and does not deliver RF power. As the drain voltage swing is basically zero during this period a DC decoupled switch can be placed in parallel to provide current conduction instead of using the PA itself. Fig. 3.14(a) depicts the corresponding schematic, which includes the DC decoupled switch S_1 in parallel to the transistor. The DC decoupled switch is controlled by the modulator and closed during the second period, while during this time no gate signal is generated.

In Fig. 3.15(a) the resulting drain voltage and current for the DC decoupled switch circuit in Fig. 3.14(a) for PWM operation with 50 % duty cycle are given. During the ON period the PA is active and operates with maximum voltage swing and hence maximum efficiency. During the OFF period the PA is inactive and the switch S_1 is closed. Its voltage and current waveforms are depicted in Fig. 3.15(c). A drawback of this arrangement is that the switch has to withstand high positive and negative voltages during the ON period and it has to conduct positive and negative current during the OFF period.

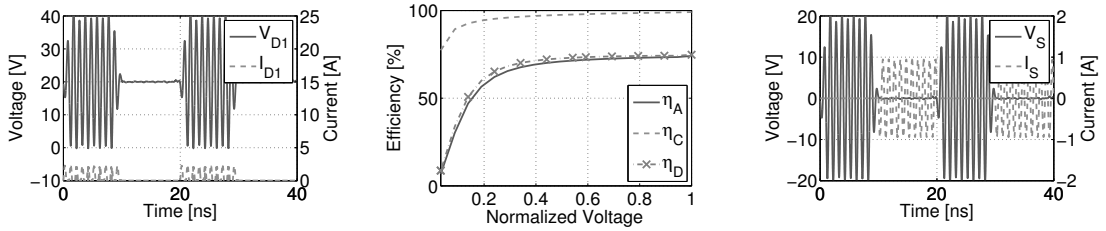
Nevertheless there is no additional power dissipation in the PA during the OFF period. When assuming an ideal switch theoretically constant efficiency can be achieved.



(a) DC decoupled switch

(b) DC feed switch

Figure 3.14: Direct filter connection of class B PA with switch.



(a) Transistor time domain

(b) Efficiency

(c) Switch time domain

Figure 3.15: Drain voltage and current for PWM and series filter with switch and efficiency.

Fig. 3.15(b) depicts the corresponding efficiency curve. It can be seen that the coding efficiency is high over the whole power range as there are only small residual losses in the modulation sidebands. Therefore, the drain and the system efficiency are almost the same. For very low output powers the efficiency degrades due to the influence of finite transition times between the two states leading to additional losses. In reality the switch will not be ideal and its ON resistance will significantly reduce the efficiency in the back off region.

An alternative to the DC decoupled switch is to place the switch in the DC supply, as depicted in Fig. 3.14(b), keeping it closed during the ON period supplying the DC current and opening it during the OFF period. By using a quarter wave line the open circuit is transformed into a short circuit at carrier frequency allowing the continuous current from the series resonator to flow. While with this arrangement the current through the switch is mainly positive, high voltage swings with an amplitude up to twice the supply voltage can occur. In both cases the requirements for the switch are very tough and can not be fulfilled with state of the art device technologies.

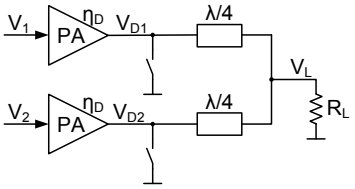
3.6.3 Multilevel

The system efficiency for single level PAs, even under highly efficient BB PWM operation, shows significant efficiency degradation in back off. A way to overcome this problem is the use of multilevel PA structures. Many different architectures for generating a multilevel signal exist and the most prominent ones are provided in Fig. 3.16.

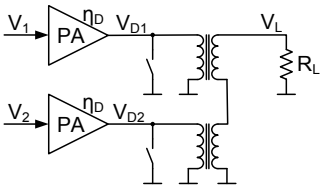
The quarter wave (Fig. 3.16(a)) [171,180–182] and the transformer based combiner (Fig. 3.16(b)) [183–188] are circuits that offer multiple output power levels with high efficiency depending on their input control. At carrier frequency both combiners have the same properties and will therefore be treated as equivalent. A drawback of them is, that they require a (DC decoupled) switch to provide low impedance when the PA is off.

Depending on the ratio of power contribution of the single PAs different efficiency curves

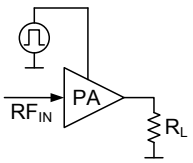
can be achieved. When considering equal power for both PAs, it makes no difference which of the two PAs is active in the low power region. For the highest power both PAs are active. The resulting efficiency curve is depicted in trace '2 level' in Fig. 3.17(a) and is similar to a sawtooth function. But when using uneven power contribution it makes a difference



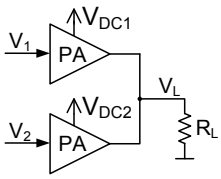
(a) Quarter wave combiner



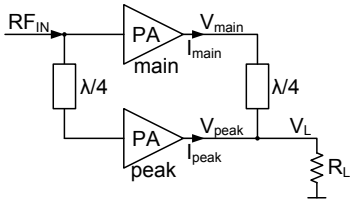
(b) Transformer based combiner



(c) Supply mod. PA



(d) Parallel PA

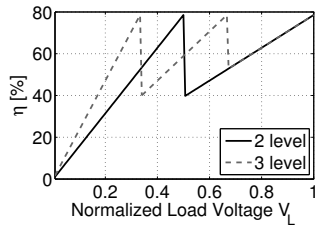


(e) Doherty

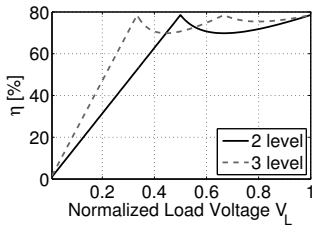
Figure 3.16: Block diagrams for multilevel combining.

which of the PAs is active for lower output powers. For very low output powers only the smallest PA contributes. When the output power exceeds its capabilities the PA with the higher output power is activated and for highest power both are active. This results in an additional efficiency peak, as depicted in trace '3 level' in Fig. 3.17(a). This means that by uneven dimensioning of the PAs an additional efficiency peak can be achieved.

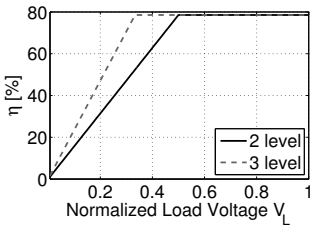
Another possibility to generate multiple efficiency peaks is to switch the DC drain supply [10], as depicted in Fig. 3.16(c), in order to provide (discrete) supply modulation to follow the envelope function. This results in essentially the same sawtooth efficiency behavior. Fig. 3.16(d) provides the schematic of two PAs whose drains are connected in parallel RF wise, but each of them having a different DC supply [189, 190]. Using the smaller PA for lower and the larger one for higher powers shows the same efficiency trend.



(a) Normal Operation



(b) BB PWM

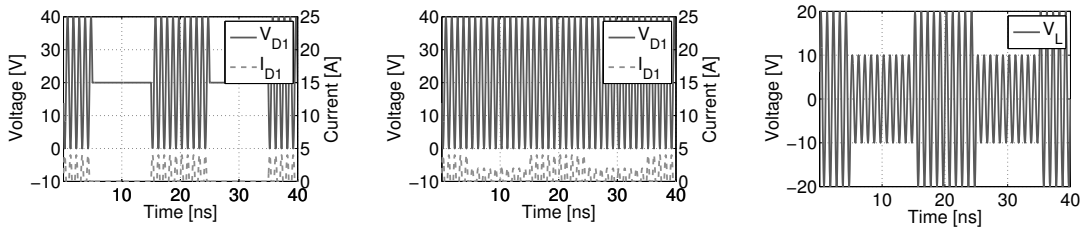


(c) BB PWM direct filter

Figure 3.17: Multi level efficiency for static, BB PWM and direct filter operation.

By applying the BB PWM coding using an isolated load, as covered in section 3.6.1, the sawtooth efficiency curves depicted in Fig. 3.17(a) can be improved in the high power region. The supply levels may be optimized in order to provide best average efficiency [191, 192]. In Fig. 3.18 example time domain waveforms for the quarter wave, respectively the transformer based combiner, for BB PWM operation for 75 % normalized load voltage, are depicted. The second PA is continuously switched on, as can be seen from its drain voltage

and current waveforms in Fig. 3.18(b). This results in a constant (CW) contribution to the load voltage depicted in Fig. 3.18(c). The bursts are provided by the first PA, which is switched on and off accordingly. For this output power range the relative contribution of the PWM is reduced compared to single level PWM coding, as a constant part (CW) is present in the load signal. This leads to reduced modulation sidebands for multilevel coding, as can be seen in Fig. 3.20(a). Exactly this reduced sideband contribution in the higher power regions leads to an improvement by BB PWM operation from the (static) sawtooth efficiency curves in Fig. 3.17(a) to the efficiency trends in Fig. 3.17(b). The theoretical derivation of this efficiency trend is provided in section 7.4.



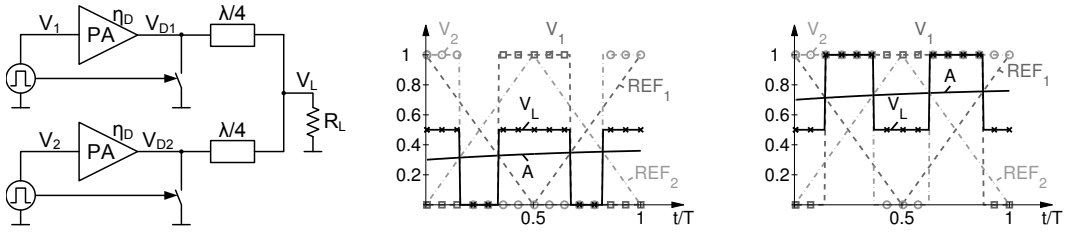
(a) PA 1 (b) PA 2 (c) Load

Figure 3.18: Drain voltage and current for 2 level BB PWM encoding with 75 % output voltage.

An exception to this is the Doherty amplifier (Fig. 3.16(e)), which shows already under static excitation the good efficiency depicted in Fig. 3.17(b). By combining the multilevel PAs with the concept of direct filter connection the efficiency can even be further increased, connecting the efficiency peaks of the Doherty PA directly [176, 177, 193]. This concept is not limited to the Doherty PA, but can be applied to any multilevel structure presented in Fig. 3.16. In the high power regions highly efficient operation, as depicted in Fig. 3.17(c), is possible, as at any time at least one PA is active, providing the required continuous load current. For the low power region, when only one PA is active, the efficiency is degraded to a class B trend due to overlap of voltage and current as described in section 3.6.2.2. Nevertheless highly efficient operation in the intermediate and high power region can be achieved.

3.6.4 Multiphase

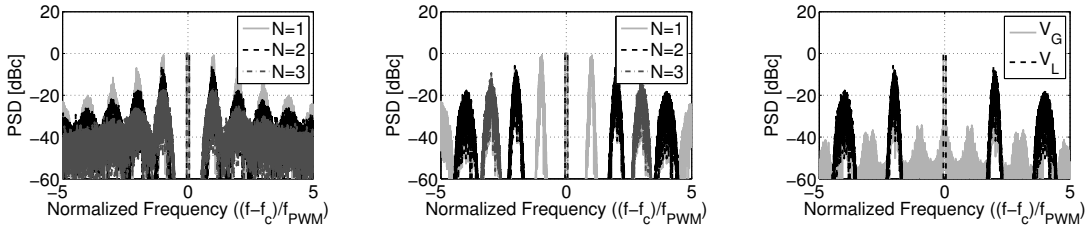
Instead of making use of multiple levels, the signal can be split into multiple phase components. This leads to the concept of multiphase BB PWM transmitters [194, 195]. The corresponding block diagram of a multiphase transmitter based on the quarter wave combiner is given in Fig. 3.19(a). Instead of using offset reference functions for the PWM generation of multilevel signals, the multiphase concept relies on (multi) phase shifted reference functions [195]. In Fig. 3.19(b) and Fig. 3.19(c) the encoding process for a 2 level transmitter with 25 %, respectively 75 %, output signal is depicted. It can be seen, that the bursts for the single branches V_1 and V_2 are generated at different phases. This is achieved by using the phase shifted reference functions REF_1 and REF_2 which are used to encode the amplitude information A. The (normalized) combined signal is composed of both pulses and shows an increased effective number of bursts. The idea is to reduce the actual modulation frequency for the single branches by making use of this increased effective modulation frequency by the multiphase coding. This can be seen in Fig. 3.20(b), which depicts the spectra of different multiphase encodings with the same modulation frequency. By increasing the number of encoding levels the first modulation sideband is moved further away from the carrier and reduced in magnitude. The magnitude reduction



(a) Block diagram (b) Normalized amplitude 0.25 (c) Normalized amplitude 0.75

Figure 3.19: Multiphase block diagram and signal generation for 2 levels.

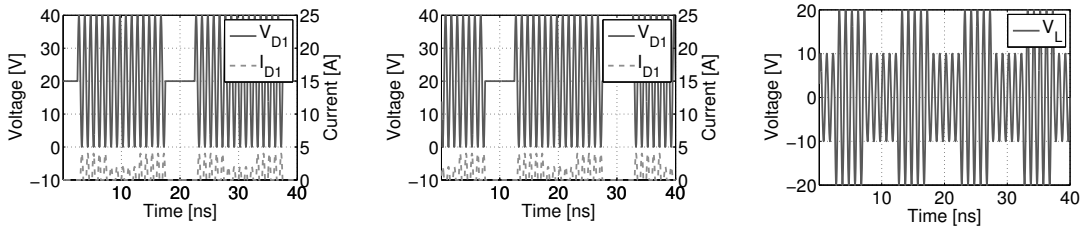
is essentially the same as for the multilevel encoding in Fig. 3.20(a), therefore the resulting efficiency enhancement is also the same as in Fig. 3.17(b).



(a) Multilevel (b) Multiphase (c) Gate/load 2 phase

Figure 3.20: Multilevel and Multiphase spectra.

In Fig. 3.21 the corresponding time domain waveforms for the encoding periods of the example of Fig. 3.19(c) are depicted. It can be seen that the drain voltage for the single PA branches contains only one burst per encoding period, while the combined signal at the load contains two bursts. This is due to the fact that the single branch signals overlaps and adds up twice per modulation period.



(a) PA 1 (b) PA 2 (c) Load

Figure 3.21: Drain voltage and current for 2 phase BB PWM encoding with 75 % output voltage.

This burst at the load, when both PAs are active at the same time, directly defines the drain currents of the single branches. Due to the quarter wave line the drain currents for the single transistors are related to load voltage and are therefore increased during the periods when both PAs are active. Although the effective modulation frequency seems to be increased by the multiphase encoding, the gate signal frequency components to generate the required drain current are increased as well. This can be seen in Fig. 3.21(c), which shows the spectra of the load and the gate signal for 2 phase encoding. It can be recognized that the drain voltage shows the desired doubling of the modulation frequency,

but that also the main modulation components of the gate signal are increased in the same way. The frequency multiplication effect also relies on cancellation of the corresponding frequency components by the single branch PAs, as the signal is multiplexed between them. To provide this cancellation the single branch PAs have to perfectly match in terms of amplitude and phase contribution.

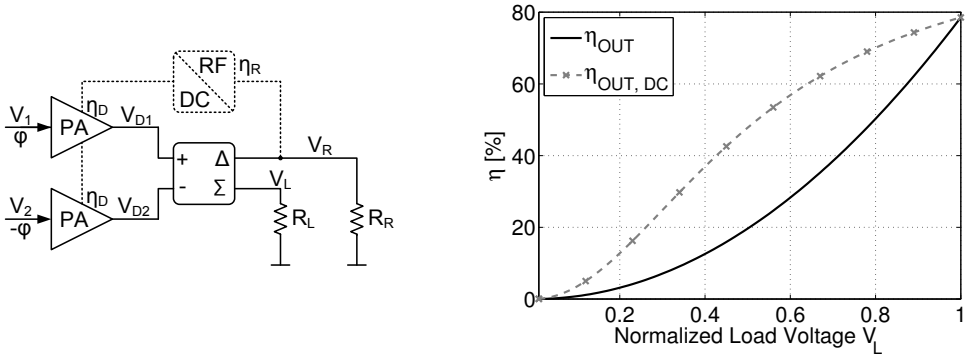
Due to the required increased gate control frequency and the stringent matching requirements the multiphase concept has no significant advantages compared to the multilevel approach. It is also possible to provide an additional efficiency peak by uneven dimensioning of the multilevel encoding, which is not possible using multiple phases, which require exactly equal levels.

3.7 Energy Recovery

In this section various efficiency enhancement concepts involving energy recovery or energy reuse will be introduced. Starting with the DC energy recovery for LINC transmitters, also the aspects of DC energy recovery in the context of BB PWM operation will be covered. Instead of recovering the energy on DC level for the BB PWM operation, a concept capable of directly reusing the energy on RF level is presented. Finally, the idea of BPSK PWM coding and related DC energy recovery operation is discussed.

3.7.1 DC Energy Recovery LINC

The LINC concept presented in section 3.2 uses an isolated combiner to avoid any load modulation effects for the PAs. A result of this isolated combiner is that a significant amount of energy is dissipated in the isolation resistor. Instead of using a Wilkinson combiner, also a 180 ° hybrid, as depicted in Fig 3.22(a), can be used. The output power is controlled by modifying the relative phase φ of the single PAs. The inphase component is transfered to the load R_L, while the out of phase power is dissipated in the termination resistor R_R.



(a) Block diagram

(b) Efficiency

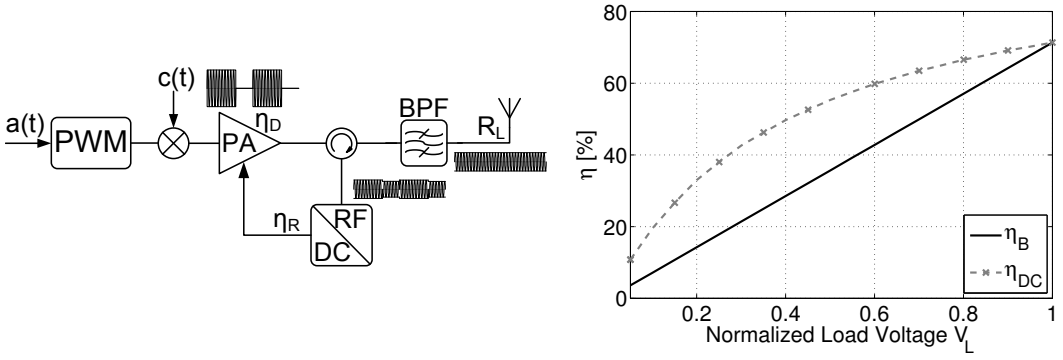
Figure 3.22: DC energy recovery outphasing.

A way to improve the resulting poor efficiency (η_{OUT}) as seen in Fig. 3.22(b) is to rectify the power of the termination resistor R_R and feed it back to the DC supply [87, 196, 197]. Assuming the same rectifier as PA efficiency leads to the improved efficiency curve $\eta_{OUT,\,DC}$ in Fig. 3.22(b). The theoretical derivation of the efficiency is provided in the Appendix 7.5.2.

A drawback of this concept is the limited possible efficiency enhancement in back off, as the recovered energy is already generated with drain efficiency, leading to unavoidable losses. The signal at the rectifier also varies with the load voltage, requiring the rectifier now to be efficient over a wide power range. Thus, the design problem is rather shifted to the rectifier than solved.

3.7.2 DC Energy Recovery BB PWM

The concept of BB PWM operation with an isolated broadband load, as introduced in section 3.6.1, shows reduced efficiency due to the energy dissipated in the isolator. This energy can be reused by replacing the sideband termination resistor with a rectifier, as depicted in Fig. 3.23(a). Instead of dissipating the energy in the sideband termination resistor the signal is now rectified and fed back into the DC power supply [198, 199].



(a) Block diagram (b) Efficiency

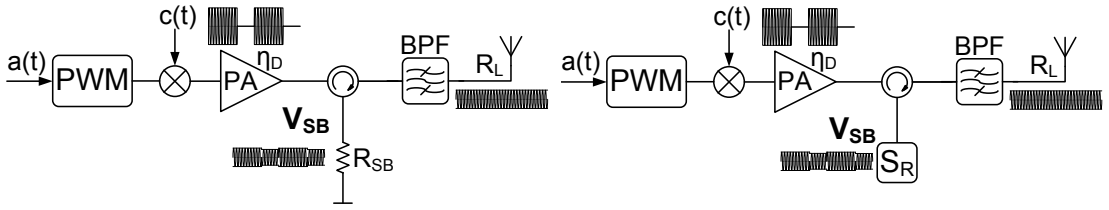
Figure 3.23: DC energy recovery BB PWM.

The derivation of the efficiency enhancement is provided in the Appendix 7.5.1 and the results are represented by the trace η_{DC} in Fig. 3.23(b). Even when assuming a rectifier efficiency of 100 % the resulting efficiency enhancement is limited due to the fact that the recovered energy is generated with the drain efficiency and thus not all of the initial DC power used to generate the sideband components can be recovered. As for the LINC energy recovery concept the signal at the rectifier significantly varies with the output power, but also significantly within one BB PWM period. Thus, the rectifier has to be efficient for varying input power signals. Again, the design problem is rather shifted to the rectifier than solved.

3.7.3 RF Energy Recovery

Instead of rectifying the signal at the termination resistor it can also be directly reused at RF level. Fig. 3.24(a) depicts the block diagram of a conventional BB PWM transmitter [38, 198, 200]. The power dissipated in the modulation sideband termination resistor R_{SB} leads to a significant reduction in efficiency. This power can be reused directly at RF level in order to provide constructive interference at the drain of the PA [S3]. In Fig. 3.24(b) the general block diagram of such a system is provided. To reflect the power in the desired phase the sideband termination resistor is replaced with a variable reflection S_R.

In order to derive the requirements of the variable reflector it is useful to investigate the time domain waveforms at the transistor and the sideband termination resistor. For the simulations presented in this section a Class B PA with a parallel resonator, placed in parallel to the DC decoupled transistor drain, is used [10]. It provides an open circuit for



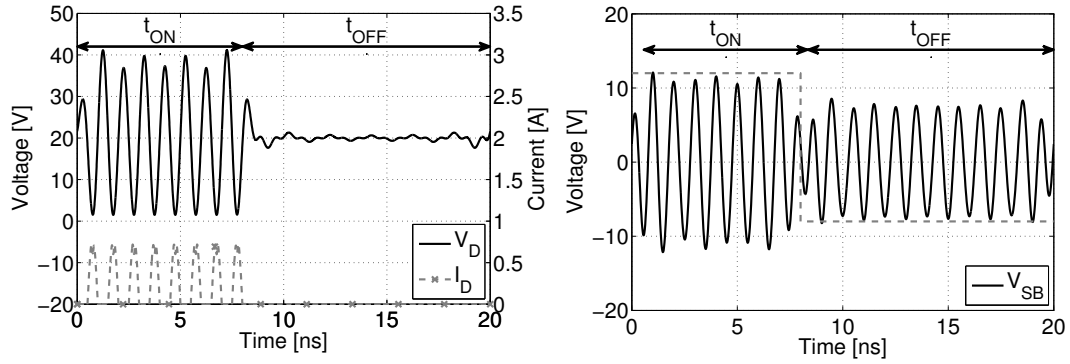
(a) Without energy reuse

(b) General energy reuse

Figure 3.24: Block diagrams of BB PWM transmitters with/without energy reuse.

the carrier and the modulation sidebands and short circuits all the carrier harmonics. The output filter is implemented as a high-Q parallel resonator.

In Fig. 3.25(a) the drain current and drain voltage of a Class B PA in burst mode operation with a duty cycle of 40 %, a supply voltage of 20 V and a carrier frequency of 1 GHz are plotted. It can be seen that the drain voltage is at maximum swing during the first period t_{ON} and zero during the second period t_{OFF}. The drain current is modulated accordingly and hence the amplifier is always efficient. Fig. 3.25(b) depicts the corresponding voltage across R_{SB}. It can be seen that the voltage at the sidebands termination resistor is the difference between the (DC decoupled) drain voltage and the average output voltage. In this case the average output voltage is 8 V due to the 20 V supply voltage and the 40 % duty cycle. This means that the voltage amplitude is 12 V during t_{ON} and -8V during t_{OFF}. This leads to a significant energy dissipation, resulting in poor overall efficiency for lower output powers which is identical to a Class B PA.



(a) Drain voltage and current

(b) Voltage across sidebands termination resistor R_{SB}

Figure 3.25: Duty cycle of 40 % and conventional burst mode PA.

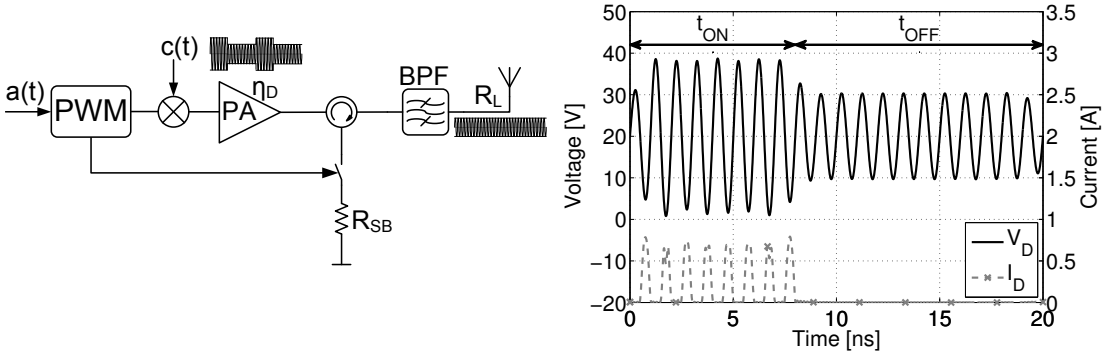
To reuse the energy it is required to reflect the signal from the sidebands termination resistor R_{SB} in the correct phase to the PA in order to have constructive interference [S3]. The required reflections will be derived in the following subsections based on partial energy recovery during t_{OFF} and t_{ON}, leading to full energy recovery in both periods. It shall be noted that for easier reading the mathematical derivation for all methods is provided in the Appendix 7.5.3.

3.7.3.1 Reuse During OFF Period

One possibility to improve efficiency is to recover the energy during t_{OFF}. During the ON period the circulator port is terminated with 50 Ω, but during t_{OFF} the signal is reflected.

The correct phase to achieve constructive interference of the drain voltage depends on the used type of band pass filter. A parallel resonator, as considered in this simulations, provides a short circuit for the modulation sidebands and therefore an open circuit is required to reflect the signal with the correct phase for constructive interference. The series resonator on the other hand provides an open circuit for the modulation sidebands and thus a short circuit at the sideband resistor would be required.

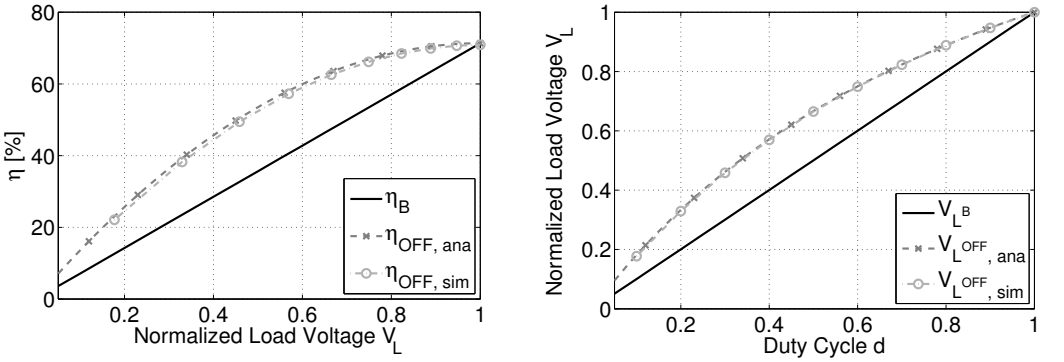
The required reflections for the parallel resonator can be generated by simply using a switch in series to the sideband termination resistor, as depicted in Fig. 3.26(a). During the ON period the switch is closed, resulting in a perfect match, but during the OFF period the switch is open, providing the desired reflection. The resulting drain current and voltage for a duty cycle of 40 % are plotted in Fig. 3.26(b). It can be seen that also during t_{OFF} a drain voltage is present. The amplitude of the drain voltage corresponds to the output voltage, as the signal is fully reflected from the sideband termination and no energy is lost during this time. The drain voltage and current during t_{ON} are the same as for the conventional operation presented in Fig. 3.25(a), meaning the PA effectively sees the load resistor during this time.



(a) Block diagram

(b) Drain voltage and current

Figure 3.26: RF energy recovery block diagram OFF period for a duty cycle of 40 %.



(a) Efficiency versus normalized load voltage

(b) Normalized load voltage versus duty cycle

Figure 3.27: Simulation results energy recovery during OFF period.

The presence of the drain voltage also during the OFF period causes a nonlinear dependence of the output voltage on the duty cycle $d = t_{ON}/(t_{ON} + t_{OFF})$ and results in

$$V_{L^{OFF}} = \frac{2\,d}{1+d}. \tag{3.4}$$

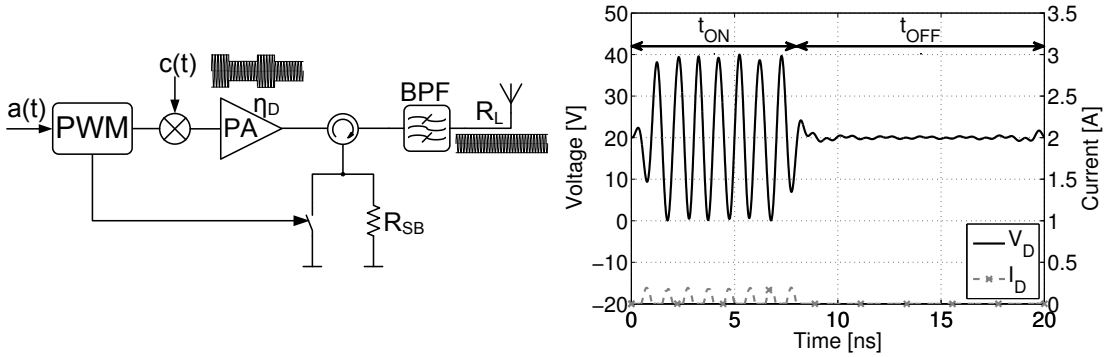
The simulated output voltage dependence curve OFF is plotted in Fig. 3.27(b). It corresponds well to the theoretically calculated output voltage defined in (3.4). As can bee seen in Fig. 3.27(b), the resulting output voltage $V_{L^{OFF}}$ is larger for low duty cycles compared to conventional operation $V_{L^{B}}$. Also the efficiency is higher than for conventional operation and can be calculated by

$$\eta_{OFF} = V_L \left(2 - V_L\right) \eta_D, \tag{3.5}$$

where V_L denotes the normalized load voltage. The efficiency enhancement is caused by the fact that no energy is dissipated in the sideband termination resistor R_{SB} during the OFF period anymore. In Fig. 3.27(a) the corresponding simulated efficiency curve η_{OFF} is plotted. For low output voltages the efficiency enhancement is limited, but for higher output voltages the efficiency can be significantly improved. It shall be noted that all simulations for efficiency and load voltage are performed with a modulation frequency of 5 MHz in order to reduce the influence of band limitation and aliasing effects [201], whereas for time domain plots a modulation frequency of 50 MHz is used for illustrative purposes.

3.7.3.2 Reuse During ON Period

To recover the energy during t_{ON}, the energy from the sidebands termination resistor is reflected back to the PA during the first period, and terminated during t_{OFF}. As for the energy recovery during t_{OFF} the required reflection depends on the used type of band pass filter. For a parallel filter a short circuit is required during t_{ON}, whereas a series filter requires an open circuit. By using a switch in parallel to the sideband termination resistor, as depicted in Fig. 3.28(a), it is possible to generate a short circuit during the ON period and by leaving it open a perfect match is provided during the OFF period. The reflected signal causes constructive interference for the drain voltage and destructive interference for the drain current, as can be seen in Fig. 3.28(b). This means that the equivalent load resistance for the PA is increased, resulting in a lower drain current in comparison to conventional operation (Fig. 3.25(a)) during t_{ON}.



(a) Block diagram

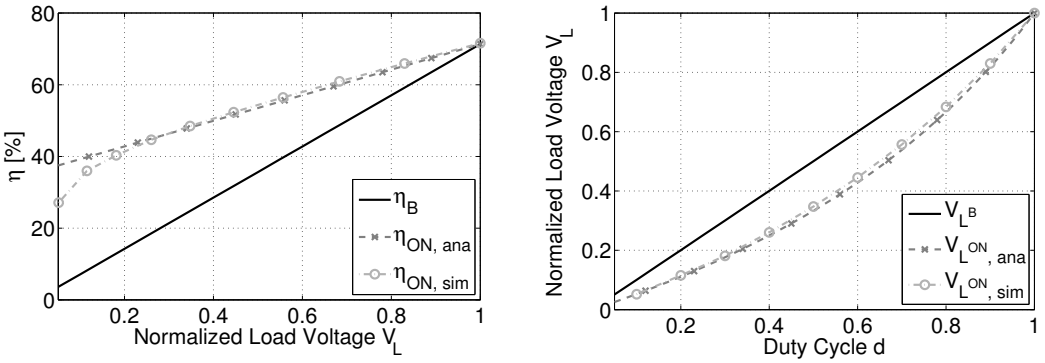
(b) Drain voltage and current

Figure 3.28: RF energy recovery block diagram ON period for a duty cycle of 40 %.

Additionally to the increased equivalent load resistance no energy is dissipated in the sideband's resistor during t_{ON}, which leads to a significant efficiency improvement. The resulting efficiency in dependence of the normalized load voltage V_L is given by

$$\eta_{ON} = \frac{1 + V_L}{2} \eta_D. \tag{3.6}$$

The simulated efficiency curve η_{ON} is depicted in Fig. 3.29(a). A significant efficiency improvement is possible, especially for low output voltages. The efficiency deviates from



(a) Efficiency versus normalized load voltage

(b) Normalized load voltage versus duty cycle

Figure 3.29: Simulation results energy recovery during ON period.

the theoretical limit for very low output voltages due to the finite rise and fall times of the pulses caused by bandwidth constraints.

As well as for the energy recovery during t_{OFF} the output, respectively load voltage, does not depend linearly on the duty cycle d anymore and is given by

$$V_{L^{ON}} = \frac{d}{2-d}. \tag{3.7}$$

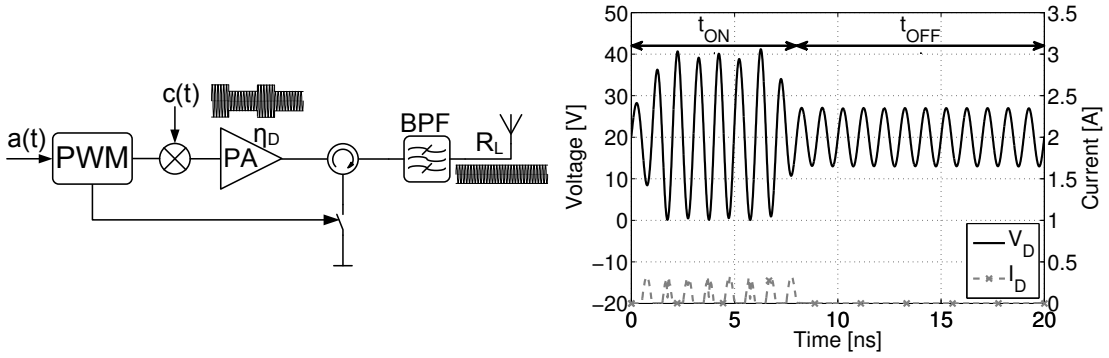
The corresponding control characteristic resulting from simulation can be seen in trace $V_{L^{ON}}$ in Fig. 3.29(b). For low duty cycles the output voltage is smaller than for conventional operation and increases rapidly to its maximum value towards the maximum duty cycle.

3.7.3.3 Full Reuse

Up to now only energy reuse either during the ON or OFF period was considered. Both methods have the drawback of nonlinear output voltage control characteristic and remaining loss in the sidebands termination resistor, which lowers efficiency. By combining both methods the energy in the sidebands can be fully reused and efficiency can be enhanced. This means that recovery takes place during the whole cycle. It is only required to reflect the signal from the sideband's resistor R_{SB} in the correct phase according to the period. By using a single switch, as shown in Fig. 3.30(a) the signal envelope at the sidebands termination resistor (Fig. 3.25(b)) can be rectified and fed back to the drain of the PA. Constructive interference for the drain voltage during t_{ON} and t_{OFF} occurs. The resulting drain voltage and current waveforms for a duty cycle of 40 % can be seen in Fig. 3.30(b).

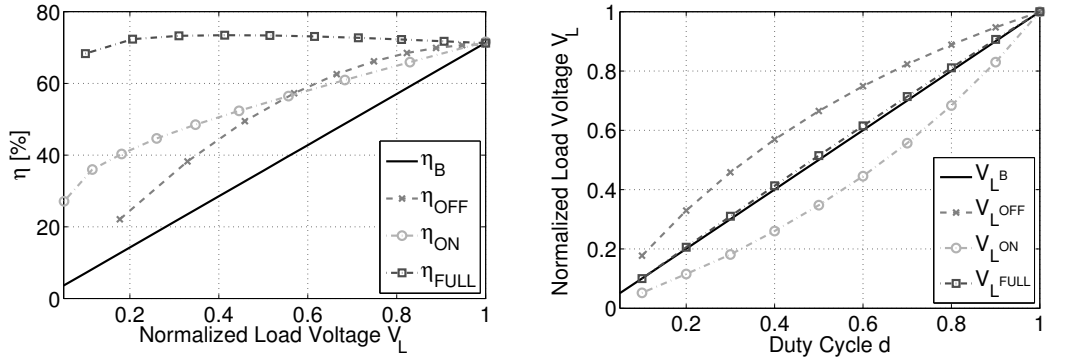
The drain current during t_{ON} is lower than for conventional operation, meaning that the equivalent load resistance for the PA also increases for this type of operation. During t_{OFF} the load voltage is present at the drain of the PA. As no energy is dissipated at all in the sidebands termination resistor anymore, the efficiency η_{FULL} is simply the drain efficiency η_D. The corresponding simulated efficiency curve η_{FULL} is given in Fig. 3.31(a). For lower output voltages the efficiency starts to slightly increase, as the influence of the knee voltage is reduced for higher load resistances, and decreases for very low output voltages. This decrease is also present for the energy recovery during t_{ON}, due to the influence of the signal transitions on the drain efficiency.

In contrast to the nonlinear dependence of the output voltage on the duty cycle for partial energy recovery, the output voltage linearly depends on the duty cycle for full energy recovery. This can be seen in the simulation results in Fig. 3.31(b) in trace $V_{L^{FULL}}$. The slight



(a) Block diagram (b) Drain voltage and current

Figure 3.30: RF energy recovery block diagram full recovery for a duty cycle of 40 %.



(a) Efficiency versus normalized load voltage (b) Normalized load voltage versus duty cycle

Figure 3.31: Comparison of partial and full energy recovery.

increase in comparison to conventional operation is due to the increase of the equivalent load resistance presented to the PA during t_{ON}, resulting in reduced influence of the knee voltage, respectively ON resistance of the transistor, for the same drive level.

For a practical system implementation a very compact solution, minimizing all delays, is desired. A delay in the system will result in a different phase of the reflected signal and impacts constructive interference, which can be overcome by providing the correct reflection coefficients for the sideband termination. In case of a delay, there will also be a short overlap of both recovery phases. This can be solved either by introducing a short dead time between both recovery phases using the general reflection circuitry suggested in Fig. 3.32 or by performing partial energy recovery and selecting the most efficient mode according to the duty cycle.

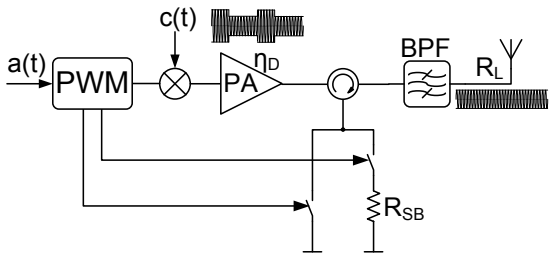
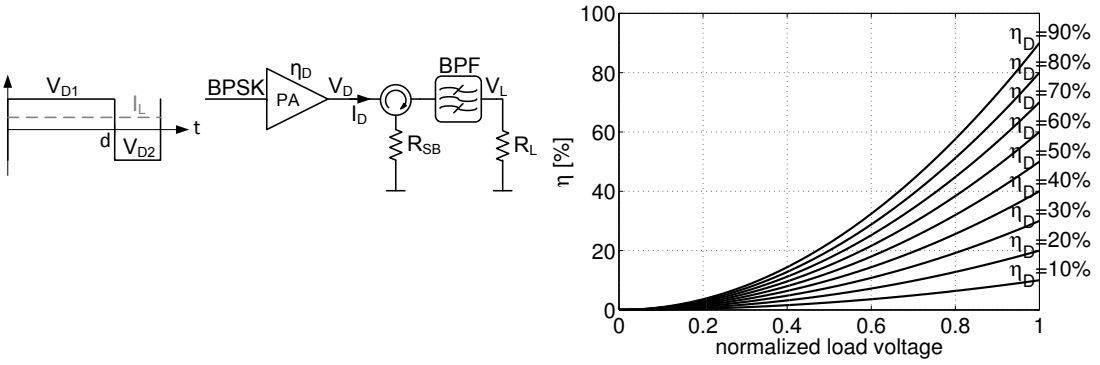


Figure 3.32: General RF energy recovery block diagram.

3.7.4 DC BPSK Energy Recovery

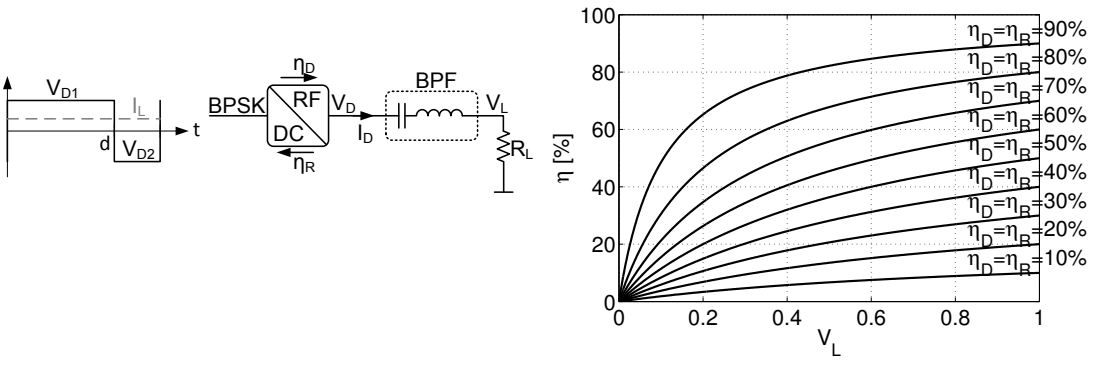
The basic idea of BPSK operation is to drive the PA with a constant envelope signal to achieve high drain efficiency. During the first period the PA is driven in phase and during the second period 180 ° out of phase. The resulting driving signal is encoded as a Binary Phase Shift Keying (BPSK) signal. By changing the duty cycle from 0 % to 50 % (or 50 % to 100 %) the output voltage respectively power can be modified. The corresponding block diagram for isolated operation is given in Fig. 3.33(a). The resulting efficiency trend $\eta_D = \eta_{max} V^2$ is similar to the one of a class A PA with higher peak efficiency, as the input power is constant and the output power increases with the duty cycle. The reflected (out of band) power from the BPF is dissipated in the isolation resistor resulting in a low efficient operation.



(a) Block diagram (b) Efficiency

Figure 3.33: BPSK PWM with isolator.

The concept of DC BPSK energy recovery is, instead of dissipating this energy in the isolation resistor, to rectify and reuse it [202], [S4]. This can be done by removing the isolator as depicted in Fig. 3.34(a). To recover the energy a PA being capable of operating as PA and rectifier is required. Possible architectures are already discussed in section 2.7.



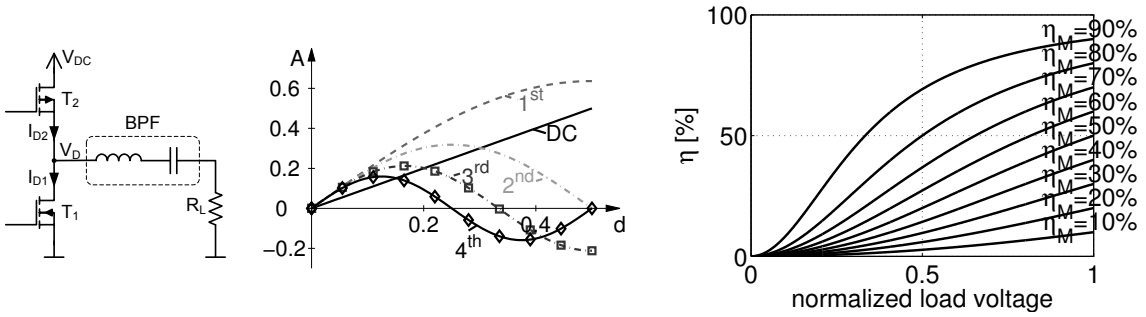
(a) Block diagram (b) Efficiency

Figure 3.34: BPSK PWM with DC energy recovery.

The resulting efficiencies for different maximum drain efficiencies (under the assumption of equal and constant PA and rectifier efficiency) are plotted in Fig. 3.34(b). The theoretical derivation is provided in Appendix 7.5.4.

3.8 RF PWM

The concept of RF PWM is to operate the PA in a saturated mode and to modify the conduction angle to control the output power [171, 203–207]. Some concepts combine the load modulation and the RF PWM approach to get best performance [169, 170]. In this section the properties of an inverter based voltage mode class D amplifier will be discussed to explain the basic principles. The behavior of other amplifier classes under RF PWM excitation is covered in section 5.1. In Fig. 3.35(a) the circuit diagram of the inverter based voltage mode class D amplifier is given. It consists of an inverter pair that forces a rectangular drain voltage. The load is connected by a series resonator to only extract the fundamental frequency component and to provide an open circuit for the higher order harmonics.



(a) Schematic (b) Frequency content vs. d (c) Efficiency

Figure 3.35: Inverter based voltage mode class D.

The resulting spectral contributions versus different duty cycles of the RF PWM signal are depicted in Fig. 3.35(b). Due to the series resonator only the fundamental (1^{st}) component is transferred to the load. Theoretically also a higher order harmonic could be selected as output signal, with the price of reduced maximum output power and higher sensibility to duty cycle variations.

The use of the series resonator enables in theory 100 % efficiency over the whole power range. Unfortunately, the maximum efficiency in practice is limited by constant losses due to the parasitic drain source capacitance or drive signal generation for the gates. These losses are independent of the duty cycle and result in the following efficiency

$$\eta(V) = \frac{V^2 \eta_{MAX}}{\eta_{MAX}(V^2 - 1) + 1} \tag{3.8}$$

with respect the normalized load voltage V. The definition of the maximum efficiency η_{MAX} and the derivation of (3.8) are provided in Appendix 7.2.3.

In Fig. 3.35(c) efficiency plots for different maximum efficiencies are depicted. It can be seen that only for high maximum efficiency the back off efficiency is improved compared to class B performance.

3.9 Summary

In this chapter several efficiency enhancement methods have been introduced, covering well established methods like Doherty, Chireix, LINC or ET/EER. In the context of energy recovery based efficiency enhancement a new method for direct energy reuse on RF level of BB PWM operated transmitters has been presented.

Among the different options of BB PWM the concept of direct filter connection shows high potential for achieving good efficiency in back off. Therefore, a main chapter of this thesis is dedicated to the analysis and development of circuits for the use of BB PWM and direct filter connection.

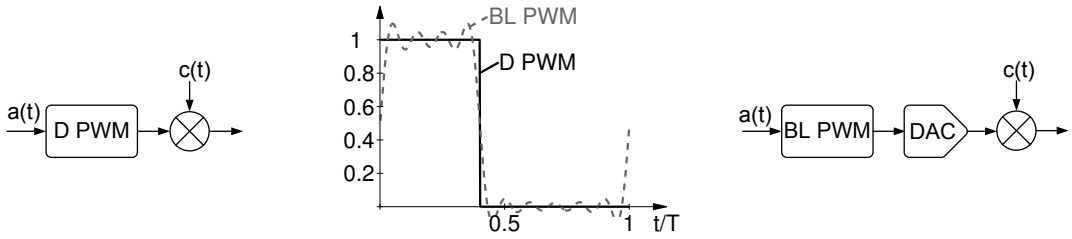
But also the concept of RF PWM is of interest due to its purely digital control signal. The use of RF PWM control enables shifting the digital to analog boundary closer to the PA towards fully digital and reconfigurable transmitters. These aspects are presented and discussed in detail in chapter 5.

4. BB PWM

In this chapter the properties of BB PWM, with a special focus on direct filter connection, will be covered. This provides the foundation for the proposed circuits for direct filter connection. First the differences and advantages of digital PWM and band limited PWM modulation will be discussed. In the subsequent sections the properties of direct filter connection in terms of load modulation, filter requirements and modeling are covered. Additionally a study about the impact of the coupling on the input impedance of the cavity filter included in the output matching network of the PA circuits is presented. The main part of this chapter covers the different circuits developed for direct filter connection. Finally spectral and linearity aspects will be discussed and the properties of the circuits will be compared.

4.1 Modulator

In this section the aspects and properties of two different modulator implementations for the generation of BB PWM signals will be discussed. The PWM modulator can be either implemented in a purely digital way, where the PWM output signal is limited to 0 and 1, or by using a limited number of harmonics, leading to an analog PWM signal with intermediate output levels. Fig. 4.1(a) depicts the block diagram of the digital PWM modulator. The amplitude information a(t) is used to encode the PWM signal, which itself modulates the envelope of the carrier signal c(t). The phase information is introduced by modulating the carrier signal c(t) accordingly. In trace 'D PWM' in Fig. 4.1(b) a digital PWM signal at base band level with 40 % duty cycle is depicted. It can be seen that it is strictly bounded to 0 and 1.

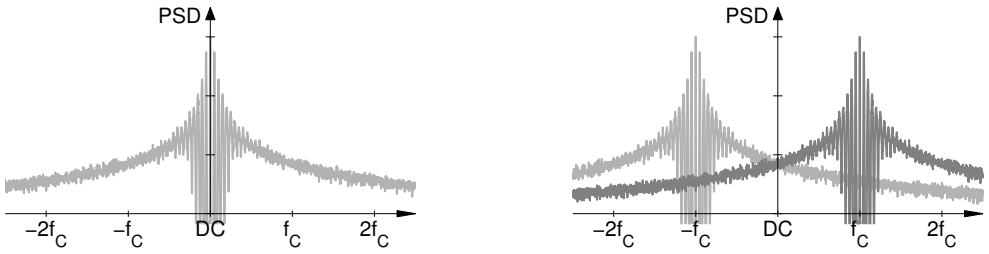


(a) Digital BB PWM (b) Time domain 40 % PWM signal (c) Band limited BB PWM

Figure 4.1: Block diagram of BB PWM modulators.

In Fig. 4.2(a) the base band spectrum of the digital PWM modulator for a modulated signal is depicted. Due to the digital nature of the PWM signal an infinite number of higher order modulation harmonics exist. This can be well seen in the decaying spectral density towards higher frequencies. Upconverting this signal to RF level leads to the spectrum shown in Fig. 4.2(b). It can be seen that the tails of the PWM spectrum continue across DC and still have a significant contribution at the inband signal range around the carrier frequency. The aliasing around DC of the higher order harmonics in the digital PWM signal severely limits the achievable dynamic range of the RF signal [201].

Instead of using all modulation harmonics one can generate the BB PWM signal only with a limited number of harmonics to avoid the aliasing around DC [208,209]. The corresponding block diagram of such a band limited BB PWM modulator is given in Fig. 4.1(c). The

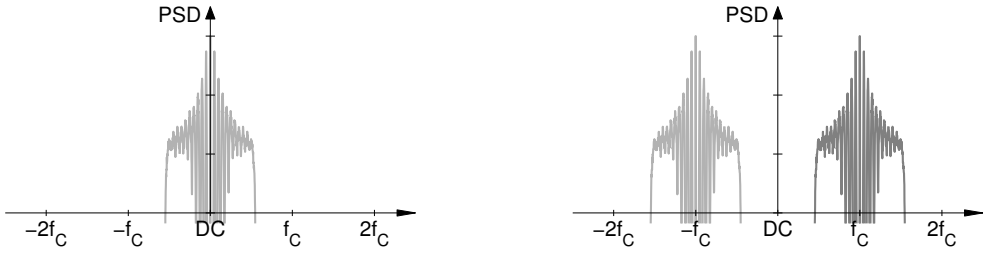


(a) BB (b) RF

Figure 4.2: Aliasing problem digital BB PWM.

resulting output signal of the Band Limited (BL) modulator core for 10 PWM harmonics and a 40 % duty cycle is plotted in trace 'BL PWM' in Fig. 4.1(b). It can be seen that due to the band limitation small ripples are present. Thus the output signal is not purely digital anymore and requires analog signals between 0 and 1 to be generated. Therefore, a D/A converter, as depicted in Fig. 4.1(c), is required after the PWM modulator core. This D/A converter is additional hardware that needs to be implemented compared to the purely digital approach. But on the other hand the band limited PWM signal can be generated with conventional IQ upconversion chains, meaning that simple integration is possible.

The main advantage of the BL PWM signal is its aliasing free output signal. The baseband signal, as depicted in Fig. 4.3(a), now shows only a limited number of harmonics, with no signal components above a certain maximum frequency. During the upconversion of this signal no aliasing occurs, due the band limited nature. The resulting aliasing free spectrum of the BL PWM modulator at RF level is provided in Fig. 4.3(b).



(a) BB (b) RF

Figure 4.3: Aliasing free band limited BB PWM.

It can be seen that the spectrum exhibits a band pass behavior. This matches with the frequency characteristics of the input matching of PAs, which usually also exhibit band pass behavior. This means that for the digital modulator, the signal at the transistor's gate will exhibit a band pass nature, with the difference that the aliasing products due to the upconversion are still present in this case.

Thus by using the band limited modulator approach high signal quality and easy integration into existing modulator setups can be achieved. Therefore, for all following simulations it will be assumed, unless otherwise noted, that a band limited modulator is used for the generation of the BB PWM signals.

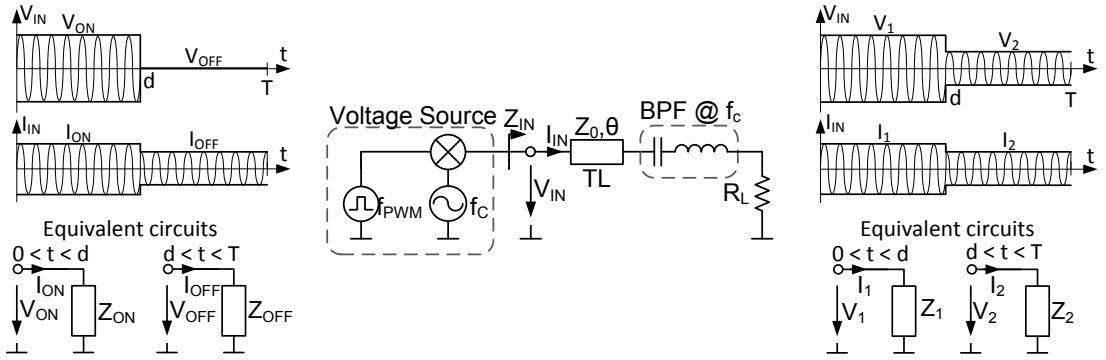
4.2 Direct Filter Connection

In this section the load modulation properties of a Band Pass Filter (BPF) will be discussed and a design methodology based on the equivalent load impedances will be presented. The requirements for the filter and the matching network for optimum performance are covered. Additionally the influence of the coupling on the reflections of cavity filters is analyzed, as they are of great importance to the matching network design. Finally the signal conditioning to achieve best performance of direct filter connection will be presented.

4.2.1 Filter Load Modulation

The use of direct filter connection results in load modulation during the BB PWM periods. As for well established concepts such as Doherty or Chireix, the load modulation trajectories of the direct filter connection are vital for the design of the PA. Therefore, the corresponding theory and the resulting design method are discussed in this chapter.

In Fig. 4.4(b) the circuit used for the derivation of theoretical load modulation is depicted. The series resonator is excited by a BB PWM modulated voltage source, which is used to model the saturated PAs. The existing theory [175] based on a series resonator is expanded by a Transmission Line (TL) to cover arbitrary orientation of the resonance locus. Fig. 4.4(a) depicts exemplary time domain traces for input voltage and current for full PWM operation. As the input voltage is different for the ON and the OFF period, while the current depends on both periods, two equivalent impedances Z_{ON} and Z_{OFF} for each period can be defined [S4].



(a) Full modulation (b) Schematic (c) Partial modulation

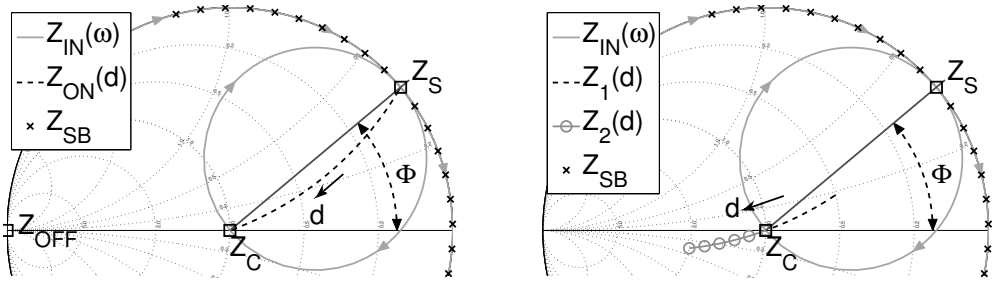
Figure 4.4: Equivalent load impedances for full/partial load modulation.

In order to provide a general solution the PWM signal is allowed to be pulse width modulated between two arbitrary voltages V_1 and V_2, leading to partial PWM modulation, as depicted in Fig. 4.4(c). Similarly to the full modulation, equivalent impedances for both periods (Z_1 and Z_2) can be defined.

The full derivation of the resulting load impedance trajectories for full and partial PWM modulation are provided in Appendix 7.7. Parameterizing the equations with the impedance at carrier frequency Z_C and the symmetry impedance of the resonance locus Z_S makes the calculation independent of the specific filter structure and generally applicable. The definition of Z_C and Z_S can be found in Fig. 4.5.

The resulting load impedances Z_{ON} and Z_{OFF} for full modulation depth and a delay θ of 160 ° are plotted in Fig. 4.5(a). The delay θ of 160 ° results in a detuning from the ideal series resonance locus by $\Phi = 40\,°$. The impedance during the ON period Z_{ON} is very

high (close to the symmetry impedance Z_S) for low duty cycles d and moves towards the carrier impedance Z_C for high duty cycles. As the voltage swing during the OFF period is zero for full PWM modulation the resulting equivalent impedance during that period Z_{OFF} is a short circuit, as can be seen in Fig. 4.5(a).



(a) Full modulation (b) Partial modulation

Figure 4.5: Example resonance locus with impedance definitions of Z_C and Z_S and resulting load impedances for full and partial modulation.

Exciting the same circuit with a partial PWM signal, varying between 0.5 and 1, results in different load modulation trajectories, as depicted in Fig. 4.5(b). The equivalent impedance Z_1 varies along part of the modulation trajectory Z_{ON} for full modulation and shows the same trend with respect to the duty cycle d. As the voltage during the OFF period is nonzero for partial PWM modulation, the equivalent impedance Z_2 during this period is modulated, as can be seen in Fig. 4.5(b).

For the theoretical derivation provided in Appendix 7.7 it is assumed that the band pass filter has infinite Q and that the impedance for all modulation sidebands is exactly the symmetry impedance Z_S. It was found that the theoretical equations are still a good approximation for finite Q resonators [S4] even if the impedances for the modulation sidebands Z_{SB}, as depicted in Fig. 4.5, deviate from the symmetry impedance Z_S. The only requirement is that the most important modulation sidebands (approx. 10) still see a reasonably high reactive impedance.

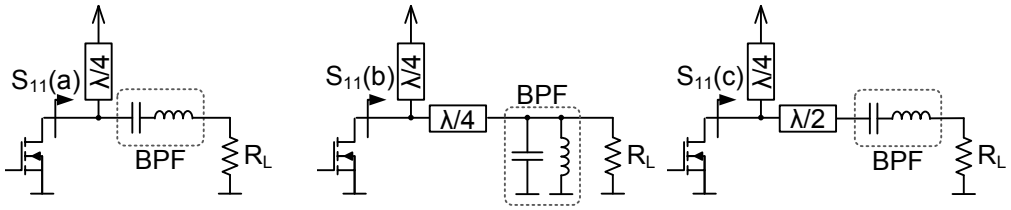
With the knowledge of the modulation trajectories the matching network can be designed in such a way that the load modulation trajectories follow efficient regions of the PA. It is shown that the orientation of the resonance locus, respectively the symmetry impedance Z_S, has a high impact on the modulation trajectories and is therefore an important design parameter. Beside for the design of the matching network the equations can be used to optimize signal generation for high efficient operation when operating the circuit not at the design frequency.

4.2.2 Filter and Matching Network Requirements

For the use of direct filter connection it is desirable to provide a high impedance over the widest range possible for the modulation sidebands above and below the carrier frequency. Also the Q-factor of the band pass filter and the related losses are an important parameter.

Based on the circuits presented in Fig. 4.6 the challenges of designing the matching network will be discussed. The ideal circuit for direct filter connection would be a series resonator with the correct load impedance directly connected to the transistor's drain, as depicted in Fig. 4.6(a). In order to provide the DC biasing of the drain a quarter wave length line is added.

The corresponding resonance locus is provided in Fig. 4.7(a). It can be seen that the resonance locus is ideally centered around the open circuit due to the series resonator. It

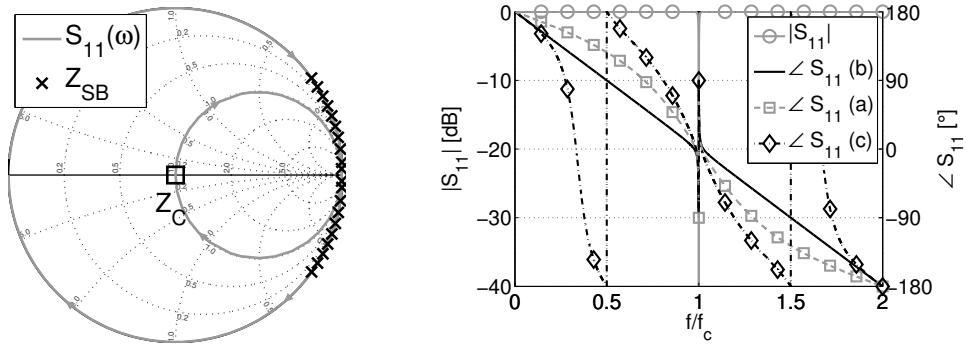


(a) Ideal series resonator (b) Parallel resonator connected by $\lambda/4$ line (c) Series resonator connected by $\lambda/2$ line

Figure 4.6: Different matching networks including high-Q BPF for direct filter connection.

can be observed that the impedances at the modulation sidebands Z_{SB}, which are marked with 'x', deviate from the ideal open circuit. This is caused by the quarter wave length line used for the DC drain biasing. The phase behavior of the reflection coefficient can be seen in trace '$\angle\, S_{11}$ (a)' in Fig. 4.7(b). The impedance, respectively reactance, remains above the carrier impedance for angles between -90° and 90°, which corresponds to $0.5\,f_c$ and $1.5\,f_c$ in this case.

Considering a parallel resonator, as depicted in Fig. 4.6(b), an additional quarter wave is required in order to transform the resonance locus into the trajectory of a series resonator, as depicted in Fig. 4.7(a). The quarter wave line causes a delay between the transistor and the load, reducing the frequency range with high impedance, as can be seen from the phase of trace '$\angle\, S_{11}$ (b)' in Fig. 4.7(b).



(a) Smith chart (b) Amplitude and phase plot

Figure 4.7: Impedance behavior of the circuits in Fig. 4.6.

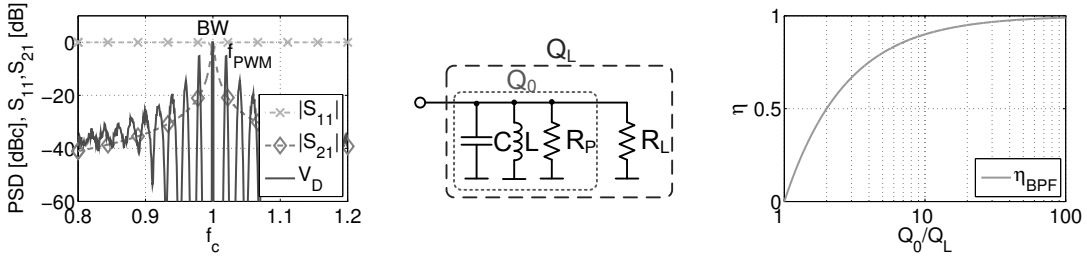
Increasing the delay, as in the circuit in Fig. 4.6(c), leads to a further reduction of the high impedance region. This can be observed in the corresponding trace '$\angle\, S_{11}$ (c)' in Fig. 4.7(b).

The delay on the one hand reduces the region of high impedance around the carrier and thus should be as short as possible. But on the other hand the delay can be used in order to provide fundamental impedance matching. The delay is helpful in providing the correct termination for the higher order harmonics. In practice always a certain shift of the resonance locus due to the coupling itself and a delay due to the connection to the coupling will be present, such that the ideal case in Fig. 4.6(a) is practically not realizable. Also the implementation of the circuit in Fig. 4.6(b) can hardly be implemented with reasonable coupling and therefore the circuit in Fig. 4.6(c), which shows high impedance between $0.8\,f_c$ and $1.2\,f_c$, will be used for the definition of the bandwidth requirements.

The maximum PWM frequency f_{PWM} has to be set in such a way that the most important

sideband harmonics (the first 5-10) fall into the region of high impedance. Fig. 4.8(a) depicts such an example. In order to provide sufficient spectral spacing between the inband signal and the first modulation sidebands the ratio of the PWM frequency f_{PWM} to the signal bandwidth BW has to be at least a factor of 5; This is required to allow for the filter's transition from pass to stop band and to provide some margin for Digital Predistortion (DPD) purposes.

Considering these two requirements results in a factor of 50 between the maximum signal bandwidth and the maximum bandwidth of high impedance. Taking some margin into account, as the matching network with the band pass filter cannot be used efficiently up to its 3 dB points, leads to a factor of 100. The circuit of Fig. 4.6(c) with its 20 % relative bandwidth of high impedance leads to a maximum signal bandwidth of 0.2 % with respect to the carrier frequency. This signal bandwidth, taking the margin to the 3 dB points of the filter into account, leads to the requirement of a loaded Q-factor Q_L in the range of 250-500 in order to fulfill the bandwidth requirements.



(a) Spectrum

(b) Parallel resonator with loss

(c) Efficiency

Figure 4.8: Unloaded/loaded Q-factor requirements of band pass filter.

A real band pass filter will always exhibit some losses, usually characterized by the unloaded Q_0, as depicted in Fig. 4.8(b). The insertion loss of the band pass filter with respect to the loaded/unloaded Q-factor is given by

$$\eta = 1 - \frac{Q_L}{Q_0}. \tag{4.1}$$

Its derivation is provided in Appendix 7.8. Fig. 4.8(c) depicts the corresponding efficiency curve of (4.1). It can be seen that for low insertion loss it is required to have a ratio of the unloaded to the loaded Q-factor Q_0/Q_L of around 10 or even higher. This means that for the design of direct filter connection circuits Q_0 values in the mid 1000 range are required in order to fulfill spectral requirements and to obtain good efficiency.

Some filter implementations, such as lumped element or microstrip, have much lower unloaded Q_0-factors and can therefore not be used. Other filter structures such as dielectric resonators or cavity filters can provide such high Q_0-factors. Cavity filters have the advantage of easy to manufacturing and tuning and where therefore selected for the design of the matching networks for the direct filter connection presented in this chapter. Their properties will be analyzed and discussed in the next section.

4.2.3 Coupling Effects in Cavity Resonators

The location of the resonance locus of the filter and the delay due to the coupling can have a significant impact on the frequency performance of the matching network, as discussed in section 4.2.2. Based on the circular cavity resonator used for the matching network design

the influence of the coupling on the filter's reflections will be discussed. The measurement and the influence of the Q-factor in the presence of coupling is very well described in [210–214], but very little attention is paid to the phase of the reflections of the filters. Therefore, a special focus on the relation of the inductive and capacitive coupling to the phase, respectively location of the resonance locus, will be paid in this section [S5].

In Fig. 4.9(a) the mechanical dimensions of the cavity resonator with a diameter of 85.6 mm and a height of 41 mm, are depicted. Capacitive coupling at the top and the bottom and inductive loop coupling at the cavity's walls was considered. As feedthrough into the cavity an extension of an SMA connector, which yields a 50 Ω coaxial transmission line, was used.

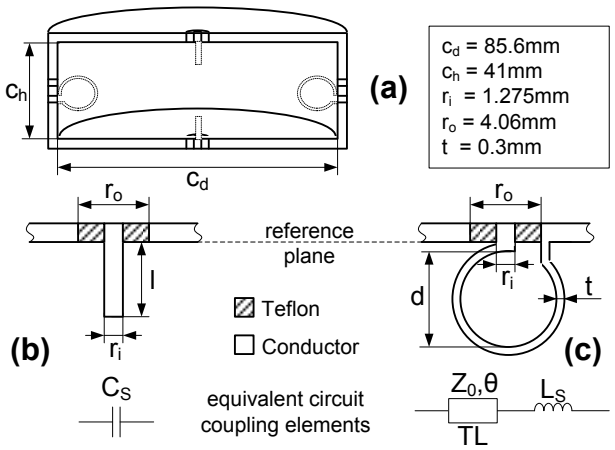


Figure 4.9: Mechanical dimensions of the cavity and coupling equivalent circuit elements.

The measured and simulated data was deembedded to the internal cavity walls, as shown in Fig. 4.9(b) and Fig. 4.9(c) respectively. The results presented in section 4.2.3.1 and section 4.2.3.2 are from finite element simulations performed with HFSS. Additionally the results from simulation have been confirmed by measurements on a coarse grid.

4.2.3.1 Capacitive Coupling

The influence of the coupling on the resonator's properties was studied using the equivalent circuit model in Fig. 4.10 [210]. In addition to the standard model, an ideal transformer is added [S5] to account for the different coupling polarities that can occur, depending on the orientation and location of the coupling, as well as the mode to which it is coupled to.

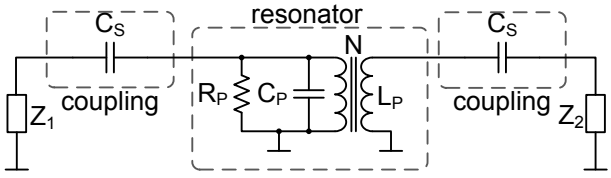


Figure 4.10: Equivalent circuit for capacitive coupling.

For analysis and representation purposes the circuit parameters of the parallel shunt circuit L_P and C_P are expressed in terms of resonance frequency f_0, internal Q-factor Q_0 and

parallel resistance R_P.

$$L_P = \frac{R_P}{2\pi f_0 Q_0};\ C_P = \frac{Q_0}{2\pi f_0 R_P} \tag{4.2}$$

For the capacitive coupling the center conductor of an SMA connector was extended to reach into the cavity, as depicted in Fig. 4.9(b). The coupling length l was swept from 0 to 12 mm during simulation. Additionally 4 different conductivities ($\sigma = \{1.1, 7, 15, 58\}$MS/m) resulting in internal Q-factors ranging from Q_0=2223 to Q_0=16118 were considered. The corresponding results for the transmission coefficient S_{21} are depicted in Fig. 4.11. For illustrative purposes only S_{21} versus frequency of selected values is plotted for the trace with the highest insertion loss ($Q_0 = 2223$) and for all the others only the maximum value max(S_{21}) for each length l and Q_0 are plotted. For stronger capacitive coupling (longer l) the insertion loss and the external resonance frequency f_{EXT}, which defines the maximum of the transmission coefficient max(S_{21}), decrease. At the same time the coupling bandwidth increases. For higher internal Q_0 the insertion loss for the same coupling length is reduced, while the frequency shift and the coupling bandwidth remain the same.

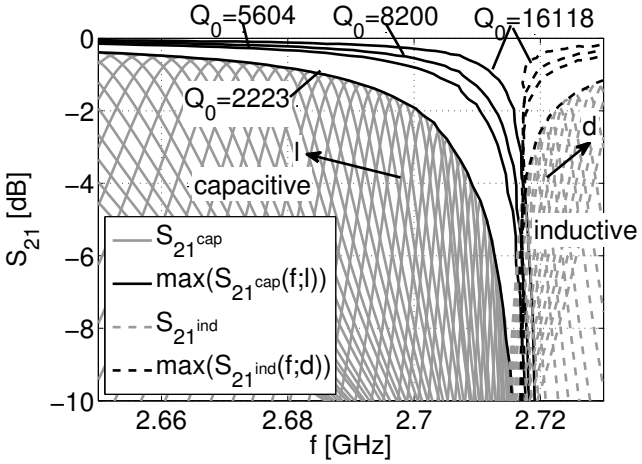
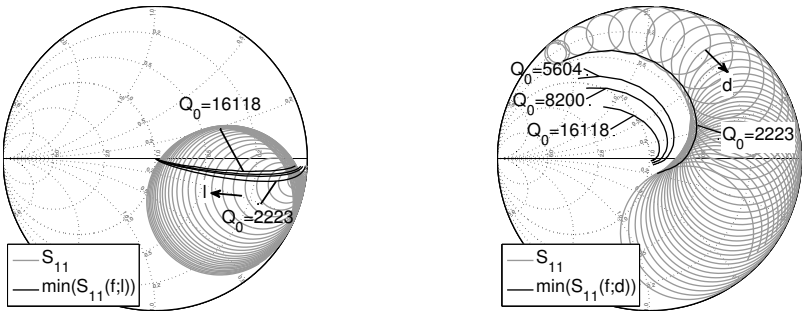


Figure 4.11: Insertion loss (S_{21}) and minimum insertion loss (max(S_{21})) for inductive and capacitive coupling for coupling length, respectively diameter and different Q-factors versus frequency.

The reflections'coefficients of the filter versus frequency and coupling length l are plotted in Fig. 4.12(a). The inner cavity walls as shown in Fig. 4.9 have been selected as reference plane. Only the full data of selected values for the lowest Q-factor are plotted and for higher Q-factors the minimum reflections min(S_{11}(f;l)) for different coupling lengths are depicted. In the smith chart it can be seen that the resonance locus is slightly shifted towards the capacitive region. This is caused by the parasitic capacitance of the coupling element. For higher Q_0 the losses are reduced and thus the reflections for the same coupling length are lower. This means that for the same mismatch the length of the coupling and also the parasitic capacitance for higher Q_0 is lower and the shift towards the capacitive region is smaller. For strong coupling the traces converge towards the same point (perfect match).

To better understand the impact of the coupling, the parameters of the equivalent circuit model of Fig. 4.10 were fitted to the simulation data for each sweep value (length and conductivity). This was done by fitting the S-Parameters using the MATLABs' fminsearch algorithm. During the fitting process the initial parameters for f_0, Q_0, R_P and C_S were estimated and their accuracy was improved using the optimizer. The transformer's ratio N_1 was set to -1 to account for the coupling polarity. The optimizer output was crosschecked by means of a circuit simulator. As the S-Parameters of the equivalent circuit model are in



(a) Capacitive coupling (b) Inductive coupling

Figure 4.12: Reflection S_{11} versus frequency and minimum reflection $\min(S_{11})$ for different coupling lengths, respectively diameter and Q-factors for $Z_0 = 50\Omega$.

good agreement with the data presented in Fig. 4.11 and Fig. 4.12(a) they are considered to be equivalent. Hence only the resulting values of the cavity fit will be discussed.

The values for the parasitic capacitance of the coupling element versus length l are plotted in trace C_S in Fig. 4.14(a). It can be seen that the capacitance increases roughly linearly with some offset for zero coupling length. In addition the fringe capacitance $C_{S^{FR}}$ of the coupling element above an infinite ground plane is evaluated to show that it is equal to the series capacitance C_S of the full model fit. As both values are in good agreement, the values for the series coupling element may be determined by the fringe field only to reduce the degrees of freedom and thus complexity for the fitting of the equivalent circuit. The coupling capacitance is independent of the Q_0 of the cavity, as it is only determined by the geometric dimensions and not by the conductivity of the cavity.

The dependence of the internal $f_{0^{CAP}}$ and external resonance frequency $f_{EXT^{CAP}}$ for capacitive coupling is given in Fig. 4.14(b). It can be seen that also the internal resonance frequency $f_{0^{CAP}}$ of the fitted model decreases with coupling length l, which causes a similar effect as inserting a tuning screw. The external resonance frequency $f_{EXT^{CAP}}$ is even lower than $f_{0^{CAP}}$, as for capacitive coupling the parallel shunt resonator has to be inductive, and thus below the resonance frequency.

The Q-factor is independent of the coupling and also remains constant over different coupling lengths for the fitted model. The parallel resistance R_P increases with stronger coupling due to the resulting lower losses.

4.2.3.2 Inductive Coupling

Round coupling loops located at the cavity side walls, as depicted in Fig. 4.9, were considered for the inductive coupling. For the coupling loop a flat conductor with a thickness t of 0.3 mm and a width of 2 mm was considered. The diameter of the coupling was swept from 1 mm to 12 mm and the used conductivities, and therefore internal Q-factors, were the same as for the capacitive coupling in section 4.2.3.1. It shall be noted that also other shapes have been considered, but the general trend is approximately the same. Similar as for the capacitive coupling an equivalent circuit model, as given in Fig. 4.13, was used to analyze the impact of the inductive coupling.

In Fig. 4.11 the transmission coefficient S_{21} is plotted. As for the capacitive coupling only selected traces for the highest insertion loss ($Q_0 = 2223$) are plotted and for lower insertion loss the maximum $\max(S_{21}(f;d))$ for each parameter sweep is depicted. It can be seen that with increasing coupling the external resonance frequency, which is at the maximum transmission $\max(S_{21})$, and also the coupling bandwidth increase. But the

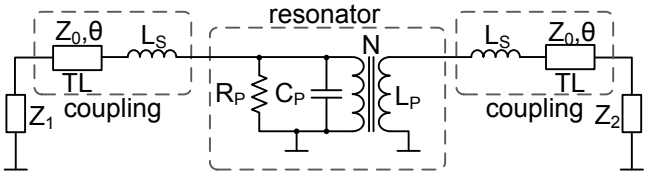
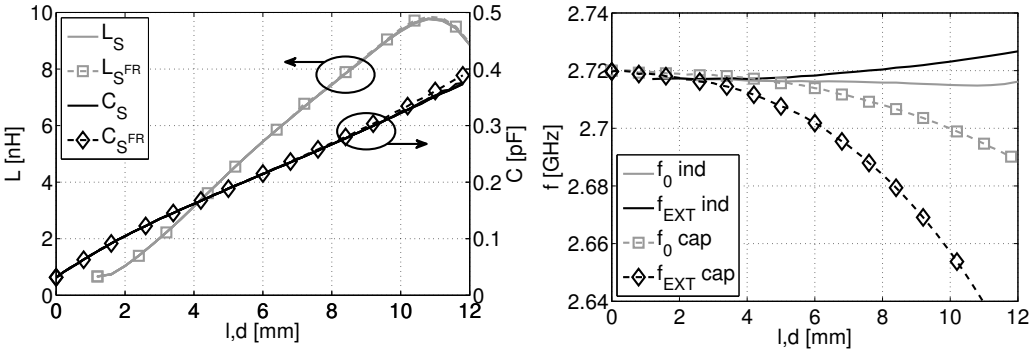


Figure 4.13: Equivalent circuit for inductive coupling.

frequency shift versus coupling strength is not as high as for capacitive coupling and thus a lower insertion loss can be achieved with a smaller frequency shift.

The impact of inductive coupling on the reflection is much more severe compared to capacitive coupling. This can be seen in Fig. 4.12(b), which shows the reflection coefficient S_{11} of the inductive coupling in the same manner as for the capacitive coupling. For small diameter d the series inductance and the coupling are small. But with increasing coupling the resonance locus moves from the inductive region towards the capacitive region of the smith chart. This is due to the fact that the coupling element itself imposes a small delay and that for large diameters d the frequency of interest is already in the vicinity of the self resonance frequency of the inductor. For strong inductive coupling S_{11} is in the same region as for capacitive coupling and can even be shifted further towards the short circuit.

For the coupling element of the equivalent circuit model in Fig. 4.13, an inductor in series with a short transmission line was used. The transmission line was required to model the extended feed of the center conductor and to take into account that the 2 mm wide coupling loop acts in the vicinity of the cavity walls like a short transmission line. For simplicity the impedance of the transmission line was assumed to be 50 Ω. The transformers ratio N was set to 1 and the delay θ of the transmission line was determined to be in the range of 10 ps to 30 ps (strong coupling) by evaluating the parameters of the coupling element only above an infinite ground plane. Beside the delay only the resulting inductance of the coupling element $L_{S^{FR}}$, as depicted in Fig. 4.14(a), was determined. Also for the inductive coupling the parameters for the coupling with (L_S) and without ($L_{S^{FR}}$) resonator are in good agreement, showing that the parameters of the coupling are independent of the cavity. The series inductance L_S increases with the diameter d. For very large diameters the inductance decreases again, as the frequency region of interest is already in the vicinity, respectively above, the self resonance frequency of the coupling element.



(a) Coupling element values

(b) External (f_{ECT}) and internal resonance frequency (f_0)

Figure 4.14: Fitted values for inductive and capacitive coupling versus coupling length, respectively diameter.

The impact of the inductive coupling on the internal resonance frequency $f_{0^{IND}}$ and external resonance frequency $f_{EXT^{IND}}$ can be seen in Fig. 4.14(b). The internal resonance frequency $f_{0^{IND}}$ of the model increases only slightly with the coupling. In contrast to capacitive coupling, the external resonance frequency $f_{EXT^{IND}}$ for inductive coupling is higher than the internal resonance frequency $f_{0^{IND}}$ due to the series inductance. The internal Q-factor and the parallel resistance R_P behave the same as for capacitive coupling.

Other important aspects are the (external) coupling bandwidth and the insertion loss of the resonator. The relation between them is given in Fig. 4.15. It was observed that the insertion loss for the same coupling bandwidth is the same for capacitive and inductive coupling and therefore only one curve is shown. It can be seen that for higher Q_0 the insertion loss for the same coupling bandwidth is significantly reduced.

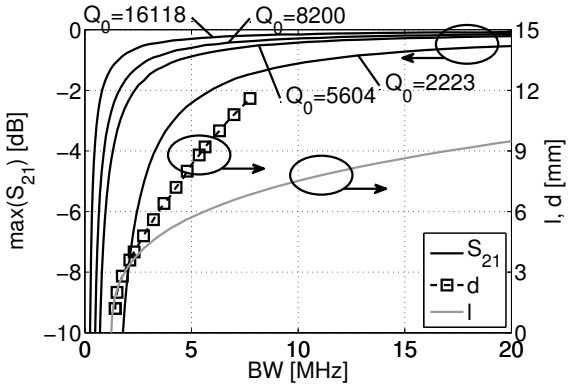


Figure 4.15: Insertion loss (S_{21}) and coupling length and diameter versus coupling bandwidth.

Additionally the required coupling length, respectively diameter, for a certain bandwidth is depicted. As the self resonance of the inductive coupling element causes the coupling to become ineffective for very large diameters, it is not possible to couple as strong as with capacitive coupling.

4.2.3.3 Broadband Modeling

For the design of power amplifiers, not only the impedance at the fundamental, but also at higher order harmonics is important. Therefore, the equivalent circuit model used for inductive/capacitive coupling is expanded to the circuit in Fig. 4.16 to take the higher order resonances, respectively modes, into account. The higher order modes of the cavity resonator can be considered by an extension of the shunt RLC circuit to N-levels [210]. To consider the different polarity of the coupling, due to the location/orientation and the used mode, a transformer for each resonator is added [S5]. The coupling elements are considered in form of a series impedance Z_S with an optional transmission line TL.

To verify the simulation results the cavities shown in Fig. 4.17 have been built and measured. The aluminum cavity shown in Fig. 4.17(a) showed a rather low Q-factor and therefore the copper cavity depicted Fig. 4.17(b) was used for further analysis and the design of the matching network.

To validate the proposed broadband model of Fig. 4.16 it is fitted to the measured data for capacitive coupling to the manufactured cavity depicted in Fig. 4.17(b). The first four resonances of the TE mode with significant coupling are taken into account and the influence of the remaining higher order resonances was considered by using a fifth resonator. To achieve good convergence of the optimizer, the parameters of each peak were determined separately and acted as initial parameters for the full model fit.

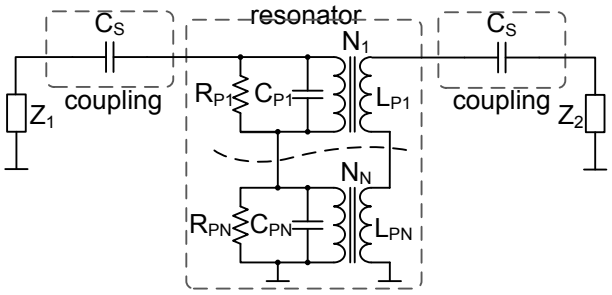
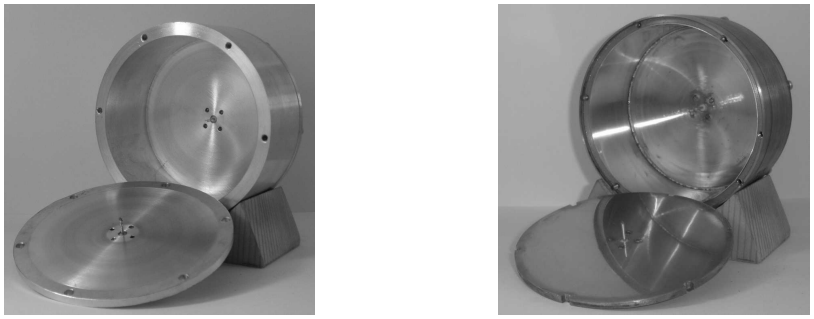


Figure 4.16: Equivalent circuit model for resonators considering the coupling and higher order modes with different coupling polarity.



(a) Aluminum (b) Copper

Figure 4.17: Manufactured aluminum and copper cavity.

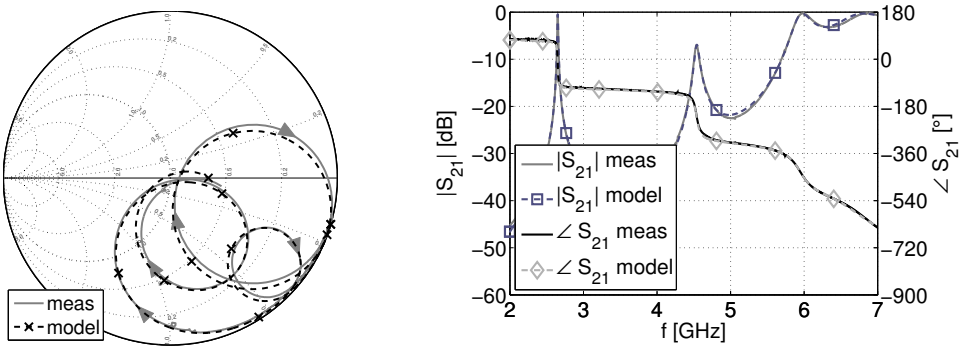
In Tab. 4.1 the resulting parameters are given. For the coupling element a series capacitor C_S with a resulting value of 0.214 pF was used. The low Q-factor for the second resonance is attributed to the fact that multiple modes are excited. The parallel resistance R_P determines the shunt reactances according to (4.2) and thus defines the 'characteristic impedance' of the resonance. In Fig. 4.18 it can be seen that both, magnitude and phase of S_{21} are in good agreement. The magnitude of S_{11} also fits well, but the phase slightly deviates as the real coupling element has a frequency dependence of C_S due to its physical dimensions.

4.2.3.4 Summary

For strong coupling the reflections of capacitive and inductive coupling are in the same region caused by the high inductance of the coupling loop and the operation in the vicinity of the self resonance. Due to that the phase of the reflection for capacitive coupling is less sensitive to the coupling strength than for inductive coupling, as can be seen well in Fig. 4.12. Therefore, capacitive coupling is better suited for the design of the matching networks for direct filter connection. The capacitive coupling has the advantage that it implicitly provides DC decoupling of the load mitigating the demand for a series capacitor

f_0	2.6799 GHz	4.5817 GHz	6.166 GHz	7.7736 GHz	9.2285 GHz
Q_0	4728.8	120.45	1408.6	933.4	31.6
R_P	14148 Ω	161.4 Ω	5319.6 Ω	17191 Ω	747.9 Ω
N	-1	1	-1	1	-1

Table 4.1: Equivalent circuit parameters.



(a) Reflection (b) Transmission

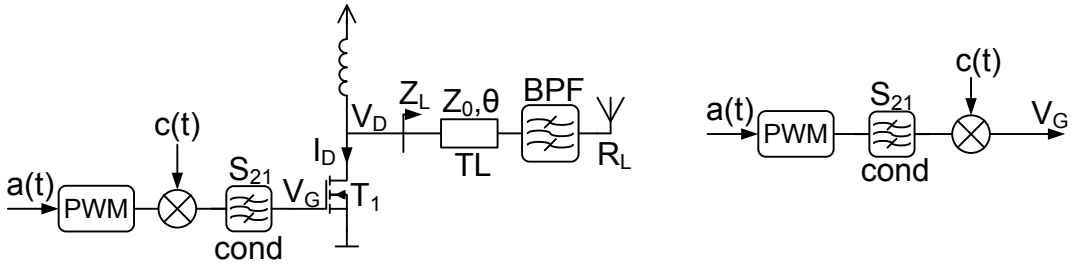
Figure 4.18: Measurement and model fit data (markers) of reflection coefficient S_{11} and insertion loss S_{21} for the first 4 TE-mode resonances.

serving this purpose.

The PA designs involving direct filter connection presented in the section 4.3 will be based on the measured data of the cavity filter shown in Fig. 4.17(b). With its external -3 dB bandwidth of around 11 MHz and its insertion loss of -0.53 dB in an 50 Ω environment it fulfills the requirements derived in section 4.2.2.

4.2.4 Direct Filter Signal Conditioning

For real circuit implementations the filter is not perfect in terms of filter bandwidth and resonance locus orientation. This results in impedances for the modulation sidebands that deviate from the ideal open circuit and eventually lead to some residual modulation of the filter current. In order to cope with that effect and to operate the PA at its optimum operational points, also within one BB PWM period, it is required to modify the applied gate signal. Fig. 4.19(a) shows a circuit for direct filter connection including the gate signal conditioning by the band pass filter. It shall be noted that the position of the band pass filter can be moved into the digital (complex) base band, as indicated in Fig. 4.19(b)



(a) Circuit (b) BB signal conditioning

Figure 4.19: Gate signal conditioning direct filter connection.

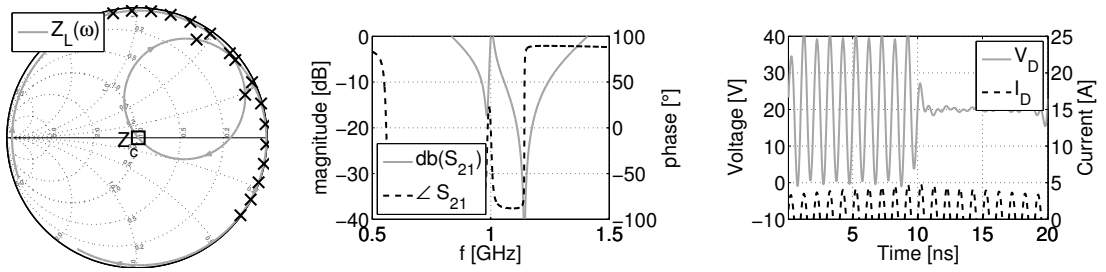
In order to generate the required gate current in terms of phase and amplitude the filter's transfer function S_{21} can be calculated by

$$S_{21}(\omega) = \frac{Z_L(\omega_C)}{Z_L(\omega)}, \tag{4.3}$$

where $Z_L(\omega_C)$ denotes the input impedance at carrier frequency and $Z_L(\omega)$ is the input impedance with respect to frequency. In case of an open circuit for the modulation side-

bands the resulting signal is constant with the amplitude corresponding to the input amplitude a(t). But if the input impedance at the modulation sidebands is finite there is a small residual remainder from the PWM modulation, which is required to provide the optimum load current throughout one BB PWM period.

Fig. 4.20(a) depicts an example for the input impedance of the BPF, where 'x' denotes the impedances at the modulation sideband frequencies.



(a) Reflection filter (b) Transfer function signal conditioning (c) Time domain waveforms

Figure 4.20: Example impedance of direct filter connection and associated signal generation.

The corresponding transfer function S_{21} of the filter, according to (4.3), is provided in Fig. 4.20(b). While for an ideal series resonator the signal at the modulation sidebands would be completely attenuated it can be seen that in this example the PWM signal is still present to some extend and corrected in terms of amplitude and phase in order to generate the desired drain voltage.

Fig. 4.20(c) shows the drain current and voltage time domain waveforms for the circuit in Fig. 4.19(a) considering the predistortion shown in Fig. 4.20(b). It can be seen that the drain current shows some residual amplitude and phase modulation. By correcting the gate signal accordingly the PA is always operated under optimum compression, leading to best efficiency performance.

If the impedance at the modulation sidebands is sufficiently high, meaning that only very small residual modulation of the drain current is present, the signal conditioning might not be required and the gate can be excited by a CW signal.

4.3 BB PWM PA Circuits

This section is dedicated to the development of PA circuits for direct filter connection. To enable the direct filter connection the PA circuits have to provide a multilevel signal and to be capable of dealing with the constant current of the filter. Four different integrated PA circuits designed for direct filter connection under multilevel excitation are presented. Two of them are based on parallel concepts and the other two rely on series concepts in order to provide multilevel PA structures. The properties of a DC BPSK energy recovery circuit, requiring a single transistor only, are evaluated. Additionally the performance of a Doherty amplifier under BB PWM operation with an isolated broadband load is investigated.

4.3.1 Common Source Parallel PA

The main requirement for efficient operation of the direct filter connection is the use of a multilevel excitation. In addition the PA has to be capable of dealing with the resulting

constant drain current efficiently for all output levels. One structure that is capable of doing so is the parallel PA, which is based on two PAs in parallel, each supplied with a different supply voltage and only one operated at a time. The basic operational principle was introduced in section 3.6.3.

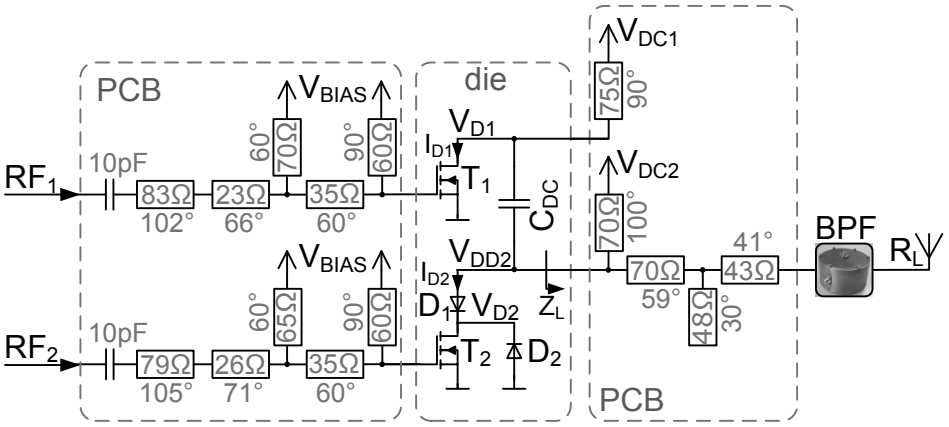
Fig. 4.21 depicts such a design of a parallel PA on a common source basis [S6, S7]. The design is split into 3 main parts. The Input Matching Network (IMN) and the Output Matching Network (OMN) are implemented on Printed Circuit Board (PCB) level using a Rogers 4350B substrate to enable the use of high Q passives and tuning after manufacturing. To provide best performance the connection of the two transistors' drains has to be very close together. The low power transistor requires a series diode for protection and therefore the core of the circuit is designed in an integrated GaN process [215]. The used transistors have a gate periphery of 4x100 μm with a maximum current of around 400 mA, their DC IV curves can be found in Appendix 7.9. It shall be noted that the same transistor size is used for all Monolithic Microwave Integrated Circuit (MMIC) designs presented in this chapter. For the direct filter connection a codesign of the OMN and the cavity BPF was done in order to provide the desired resonance locus and to achieve best performance.

The basic principle of the circuit relies on biasing the two transistors T_1 and T_2 with different DC supply voltages, where $V_{DC1} > V_{DC2}$. To provide the DC decoupling the drain of the two transistors is connected using the series capacitor C_{DC}, whose parasitic self resonance frequency is designed to be at the carrier frequency in order to provide the best connection. For efficient operation only one of the two transistors is active at a time, while each exhibits its maximum voltage swing. This results in two different (non zero) envelope voltage levels, for which high drain efficiency can be achieved. The input signal is encoded and predistorted in order to shape the drain voltage to these two voltage levels, and then multiplexed between the two transistors according to the duty cycle of the PWM signal.

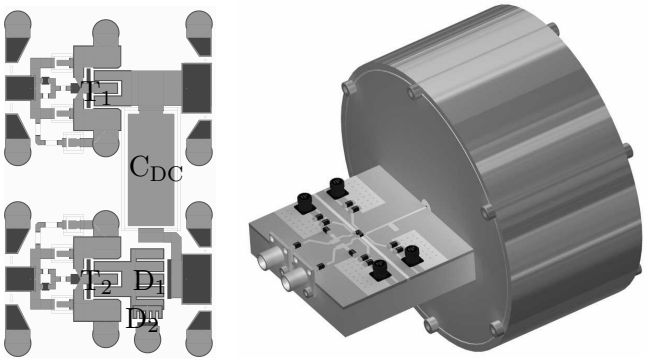
Fig. 4.22 depicts exemplary time domain waveforms of the drain voltages and currents for both transistors and a duty cycle of 50 %. For illustrative purposes a high modulation frequency of 132.5 MHz was selected, while the real circuit is operated at 20.7 MHz ($f_c/128$). Transistor T_1 is biased with 30 V and transistor T_2 with 15 V. In combination with the 50 % duty cycle the resulting load voltage is 22.5 V, which corresponds to a normalized load voltage of 0.75. The drain voltage swing toggles between the two DC supply voltages and the drain current is multiplexed between both transistors according to the duty cycle. It can be seen that the drain voltage has a maximum swing for each transistor during current conduction. Therefore, the drain efficiency is at its maximum. In combination with the high coding efficiency, due to the open circuit for the PWM sidebands, high system efficiency can be achieved.

When the high power transistor T_1 is active (t_{ON}) the drain voltage of the lower power transistor T_2 drops below zero. This would lead to conduction of the parasitic gate-drain diode of the GaN transistor. To prevent negative voltages at transistor T_2's drain a series diode D_1 is added. In order to ensure a positive voltage at the transistor's drain also during signal transitions a small anti parallel diode D_2 is required as well.

For the design of the matching networks of a PA the Load Pull (LP) contours are of importance. Fig. 4.23(a) and Fig. 4.23(b) depict the load pull contours at the reference plane Z_L for low and high power operation respectively. It can be seen that the efficiency maxima are different in terms of resistance due to the two different supply voltages. Also in terms of reactance the efficiency contours deviate. This is due to the fact that for the high power operation the series combination of the parasitic capacitances of D_1 and T_2 load the circuit, while for low power operation the parasitic capacitance of D_1 is effectively short



(a) Schematic



(b) Layout

(c) 3D view

Figure 4.21: Schematic of the common source PA with direct filter connection.

circuited increasing the capacitive loading as only T_2's parasitic capacitance is present. For the design the focus was set on the efficiency of the low power operation, as the efficiency at low powers is more important for the average efficiency than the maximum efficiency of the circuit. Another important parameter for direct filter connection, which was also considered during the matching network design is the orientation of the resonance locus. By properly designing the matching network in Fig. 4.21(a), including the orientation of the resonance locus, the load modulation trajectories Z_{ON} and Z_{OFF} shown in Fig. 4.23(c) follow efficient regions in the smith chart. Additionally the impedances at the modulation sidebands Z_{SIDE} for a modulation frequency of 20.7 MHz are indicated.

In Fig. 4.24 the drain voltage waveforms of the circuit in Fig. 4.21 for low power operation are provided. It can be seen that the low power PA is operated with maximum voltage swing leading to maximum efficiency. The drain voltage V_{DD2} before and V_{D2} after the diode are almost identical as the diode is conductive. The voltage at drain of the high power transistor in Fig. 4.24(b) is simply a DC shifted replica of T_2's drain voltage. The drain current of the high power transistor is essentially zero due to the class C gate biasing, leading to almost no power consumption of T_1. As the drain of T_1 is actively excited there is some feedback to the gate due to the parasitic gate-drain capacitance. This feedback can lead to conduction of the transistor resulting in power consumption and even instability. Therefore, the class C biasing was required not only for the low DC drain current, but also to provide some margin such that the feedback effect doesn't cause any drain current conduction in the OFF state. To ensure stability a resistance network was added to the transistor's gates, which also improves the feedback behavior. These resistance networks

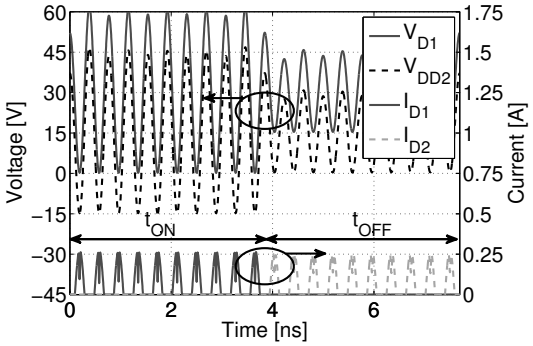
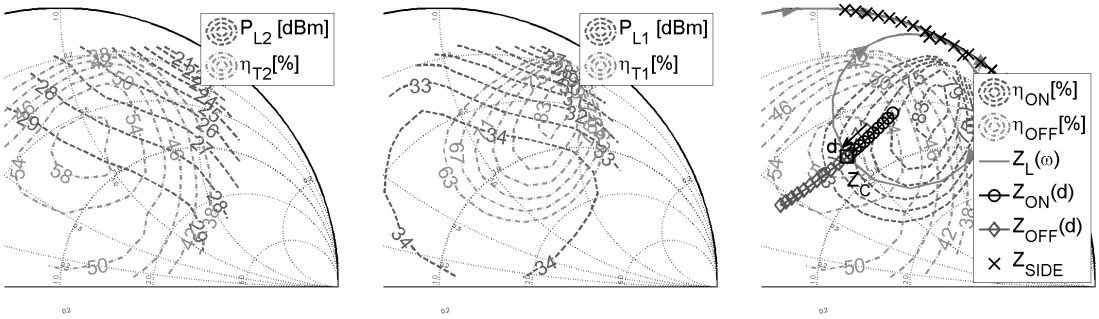


Figure 4.22: Drain voltages and currents for the Class-B parallel PA circuit for a PWM frequency of 132.5 MHz, a carrier frequency of 2.65 GHz and a duty cycle of 50 %.



(a) Low power (T_2) (b) High power (T_1) (c) Both

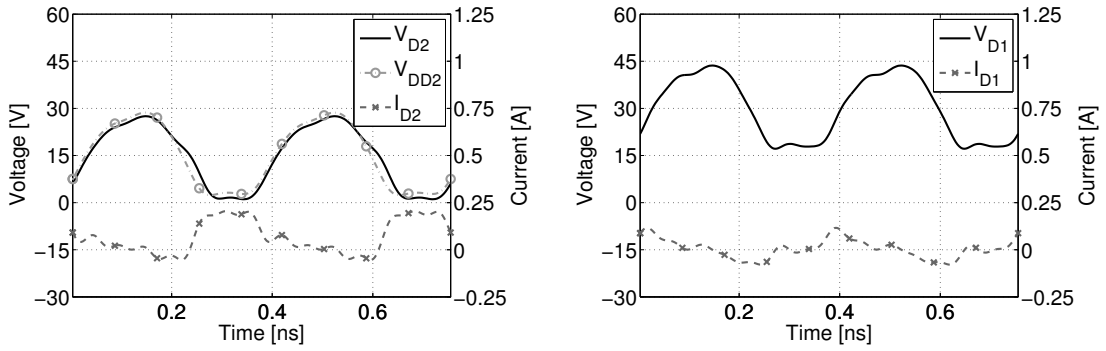
Figure 4.23: Load pull efficiency contours, matching network and load modulation trajectories for a carrier frequency of 2.6515 GHz.

consist of a combination of series and shunt elements and are located between the probe pads and the transistor, as can be seen in the layout in Fig. 4.21(b).

During high power operation the transistor T_1 is excited, resulting in maximum voltage swing, as depicted in Fig. 4.25(b). The low power transistor is inactive during this time. It can be seen that the series diode prevents negative voltage on the transistor's drain such that V_{D2}, given in Fig. 4.25(a), always remains positive. Nevertheless the drain voltage V_{D2} shows still some voltage swing, as the parasitic capacitances of the diode and the transistor form a capacitive voltage divider.

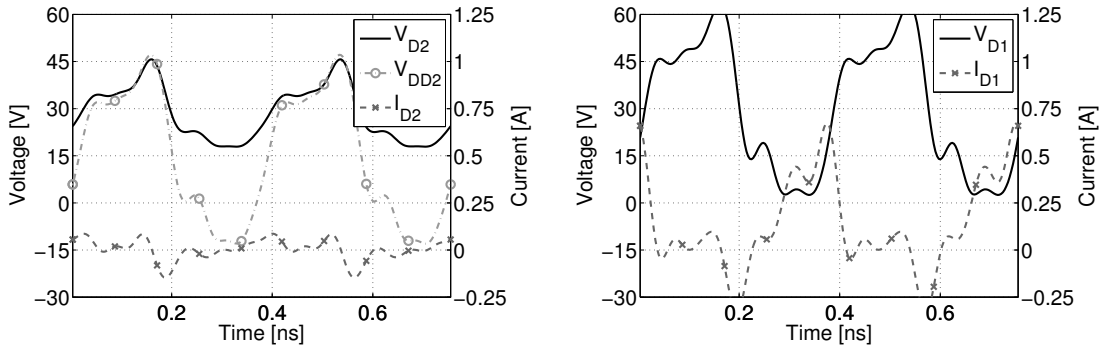
The frequency dependence of the gain, output power and efficiency is plotted in Fig. 4.26. Although the drain efficiency for low power operation, as shown in Fig. 4.26(a) is quite high, the PAE is severely reduced by the low gain of less than 10 dB. The low gain is a result of the class C biasing and the reduced supply voltage for the low power operation. The diode also increases the series resistance of the transistor and thus contributes to the efficiency degradation. Due to the band pass filter required for direct filter connection output power and efficiency degrade quite quickly when deviating from the design frequency of 2.6515 GHz.

For high power operation in Fig. 4.26(b) it can be seen that higher values in terms of gain and efficiency are achieved due to the higher supply voltage. When comparing the efficiency of both operational conditions, as given in Fig. 4.26(c), it can be seen that their maxima are different. This is caused by the different capacitive loading for both operational conditions.



(a) Low power PA (T_2) (b) High power PA (T_1)

Figure 4.24: Drain current of both PAs for low power mode.



(a) Low power PA (T_2) (b) High power PA (T_1)

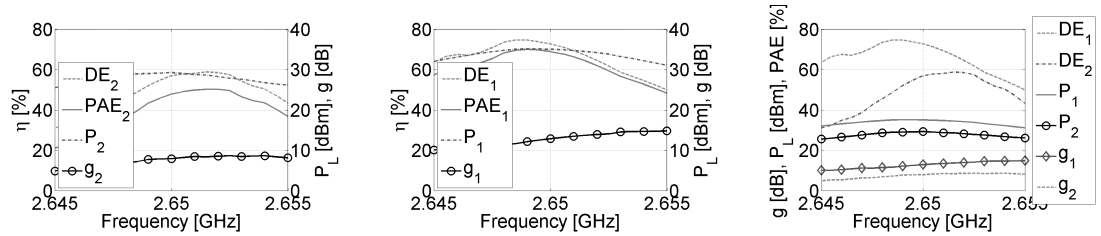
Figure 4.25: Drain current of both PAs for high power mode.

Fig. 4.27 depicts the efficiency curves under static and BB PWM excitation for the design frequency of 2.6515 GHz. From the static efficiency curve in Fig. 4.27(a) it can be seen that the desired efficient multilevel operation is achieved. Two efficiency peaks at 0.65 W (8 V load voltage amplitude) and 2.5 W (15.8 V load voltage amplitude) output power lead to a sawtooth like efficiency curve for CW excitation. By using BB PWM in combination with direct filter connection it is possible to connect the two maximum drain efficiency points leading to the efficiency curve provided in Fig. 4.27(b). It can be seen that for the high power range above the output power of the low power transistor highly efficient operation can be achieved. Due to the rather low gain the corresponding PAE is reduced. Accounting for the insertion loss of 0.54 dB of the band pass filter, the drain efficiency and PAE are further reduced, but still show the highly efficient trend of direct filter connection.

It can be concluded that by combining the common source parallel PA presented in this section with direct filter connection and BB PWM highly efficient operation in the high power region can be achieved.

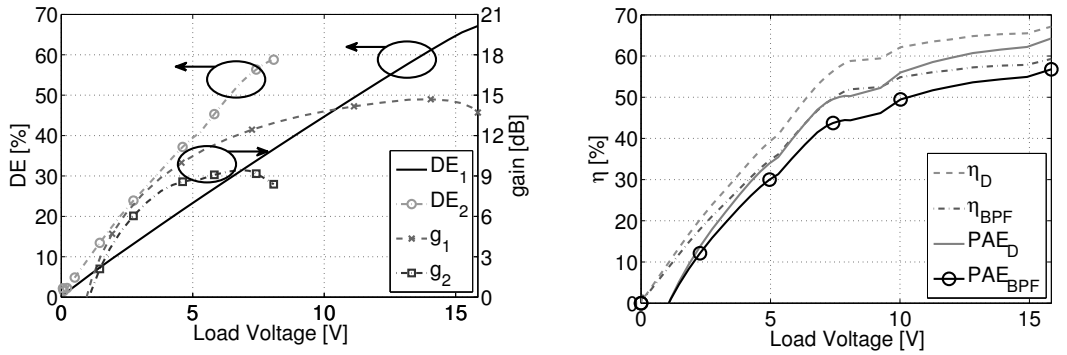
4.3.2 Common Drain Parallel PA

The operational principle of the common drain parallel PA is essentially the same as for the common source parallel PA presented in the previous section. The main difference is that for the common drain parallel PA the drain of the two transistors is connected



(a) Low power (b) High power (c) Both

Figure 4.26: Efficiency, gain and output power versus frequency.



(a) Static CW (b) BB PWM

Figure 4.27: Efficiencies versus load voltage for a carrier frequency of 2.65 GHz and 20.7 MHz modulation frequency.

directly, as can be seen in the schematic provided in Fig. 4.28(a). Its core is designed in a GaN MMIC process [215] to minimize the physical and electrical length of their connection. The corresponding layout is given in Fig. 4.28(b). In order to provide two different supply voltages the DC source potential of T_2 is modified instead of the DC drain supply voltage. Transistor T_1 is supplied with 30 V, while T_2 is biased with 15 V. The biasing for transistor T_2 is done with respect to the supply voltage of transistor T_1, meaning that the source potential of T_2 is shifted to 15 V in this case. To provide a stable source voltage an on chip shunt capacitor C_{DC} is included, which is designed to have its parasitic self resonance frequency close to the carrier frequency. Compared to the common source PA this circuit has the advantage of requiring only one DC bias on the RF domain leading to a reduction of the losses and a compact matching network design [S7, S8].

In combination with the direct filter connection the common drain amplifier can be operated highly efficient between the region of the low power (T_2) and the high power mode (T_1). Fig. 4.29 depicts the drain currents and voltage for the common drain PA and a duty cycle of 50 %. For illustrative purposes the high modulation frequency of 132.5 MHz was chosen. During the ON period the high power transistor T_1 is active, being operated with its maximum voltage swing and thus maximum efficiency.

During the OFF period the low power transistor T_2 is active, being also operated at its maximum voltage swing. Due to the special biasing concept the source potential of T_2 is increased to 15 V resulting in a minimum overlap of the drain-source voltage and the drain current of T_2. This way also T_2 is operated highly efficient during the OFF period. As the source potential of T_2 is higher than the ground potential, transistor T_2 would see a negative drain source voltage, when T_1 is active. To prevent this, the series diode D_1 has been added.

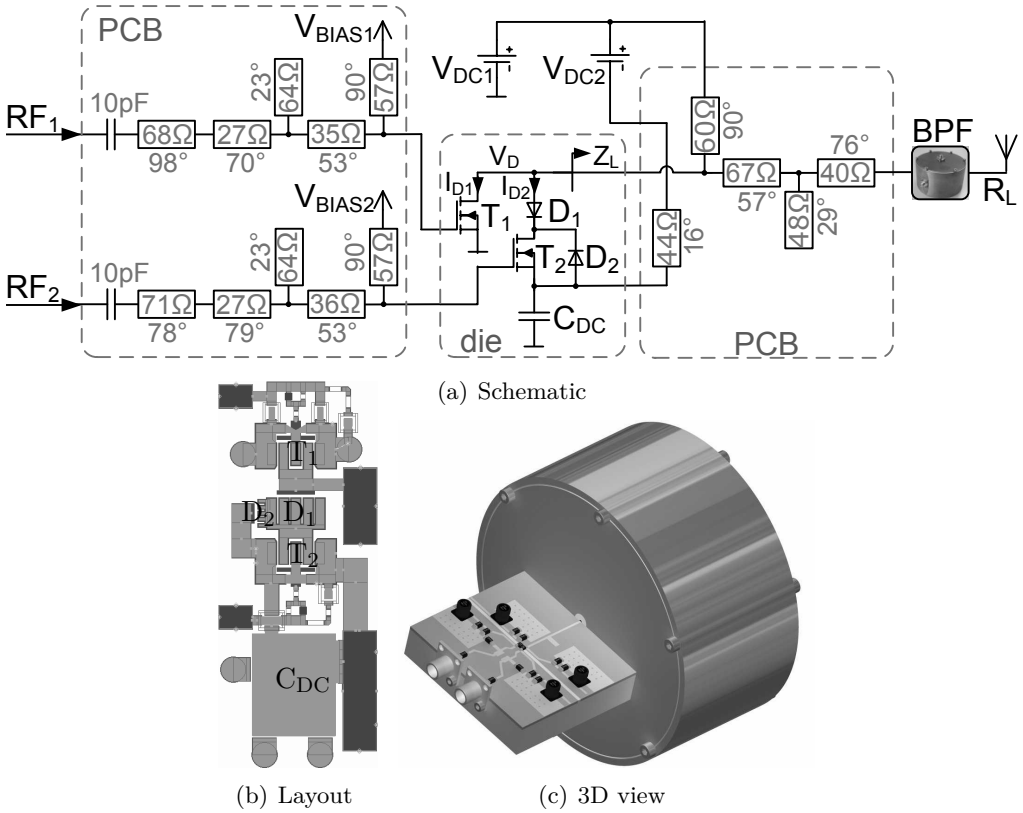


Figure 4.28: Schematic of the common drain PA.

To achieve best performance and enable tuning after manufacturing the input matching network and the output matching network are implemented on PCB level. To achieve the required matching network a codesign of the cavity band pass filter and the PCB output matching was done. For the BPF measured data of the cavity filter presented in section 4.2.3.3 was used, while for the PCB a Rogers 4350B substrate was considered. The resulting arrangement is depicted in Fig. 4.28(c). The transition from the band pass filter to the PCB is essentially the same as the interface of SMA connectors to a PCB and has no major influence.

The LP contours for both operational modes, provided in Fig. 4.30, were used as a starting point for the design of the output matching network. The efficiency maxima η_{T1} and η_{T2} are different in resistance due to different supply voltages and slightly different in reactance. The difference in reactance is due to the fact that the parasitic capacitance of T_2 is different for both operational modes similar to the common source amplifier. Compared to the common source amplifier the efficiency contours of the common drain PA are slightly shifted towards higher inductive regions. This is caused by the fact that the fringe capacitance to ground of C_{DC} does not load the RF part of the common drain circuit. In addition the achievable maximum efficiencies are higher, as only one DC biasing at RF level is required, leading to fewer losses and leaving more degrees of freedom for the higher order harmonics' termination.

Also in the design of the common drain PA the focus was set to the efficiency of the low power PA. During the matching network design the orientation of the resonance locus, the fundamental Z_C and the impedances of the higher order harmonics, were considered. In Fig. 4.30(c) it can be seen that resulting load modulation trajectories Z_{ON} and Z_{OFF} with respect to the duty cycle d run along efficient regions of the LP contours. Additionally the impedances Z_{SIDE} for the first 10 modulation sidebands for a modulation frequency of

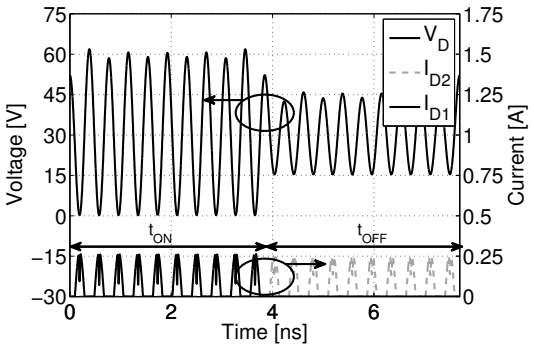
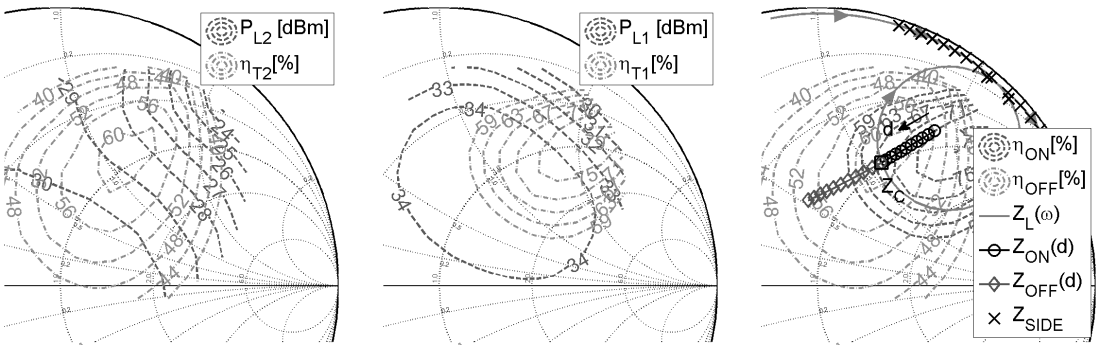


Figure 4.29: Exemplary drain voltages and currents for the common drain PA for a PWM frequency of 132.5 MHz, a carrier frequency of 2.65 GHz and a duty cycle of 50 %.

20.7 MHz are plotted.



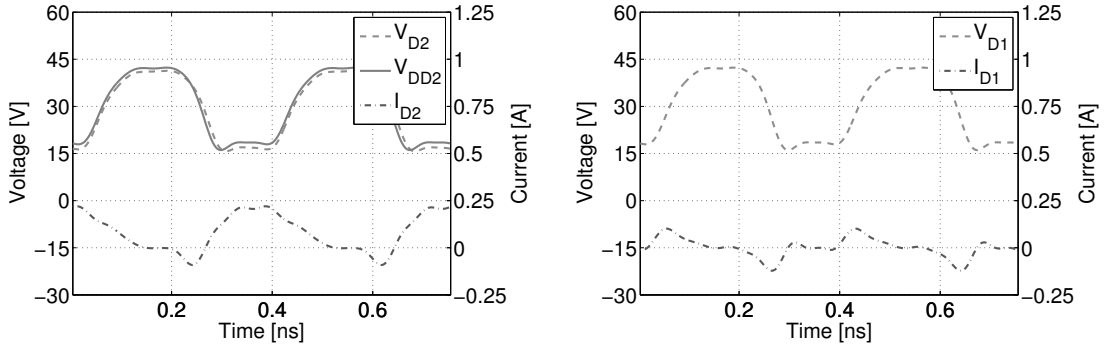
(a) Low power (T_2) (b) High power (T_1) (c) Both

Figure 4.30: Load pull efficiency contours, matching network and load modulation trajectories for a carrier frequency of 2.6495 GHz.

Fig. 4.31 depicts the drain currents and voltages of the final design for low power operation. Only the transistor T_2 is active during that time, being operated with its maximum voltage swing. Its source potential is shifted to 15 V by the biasing concept. It can be seen that the overlap of its drain current and voltage has been minimized, leading to high efficiency. The drain voltage of T_1 is the same as for T_2. Its DC drain current is basically zero, thus T_1 does not consume power in that operational state. As for the common source PA the gates of both transistors are equipped with a resistive network for stability and biased in class C in order to provide some margin for the drain-gate feedback.

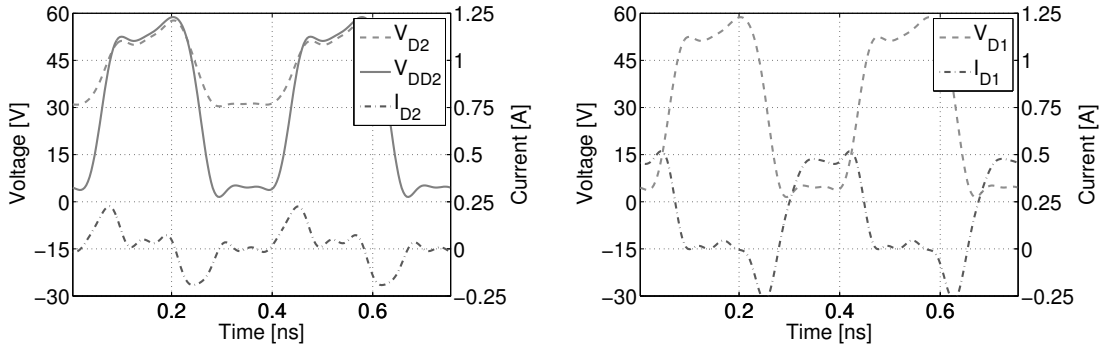
For high power operation, as plotted in Fig. 4.32, the high power transistor T_1 is active. In Fig. 4.32(b) it can be seen that T_1 exhibits its maximum voltage swing and thus is operated highly efficient. The higher order harmonic terminations have been optimized towards class F operation to improve the efficiency. Due to the direct connection of both transistors drains their voltage swing is the same. The series diode D_1 prevents negative drain source voltage for T_2 (with respect to its 15 V source potential). The combination of the parasitic capacitances of D_1 and T_2 acts as a capacitive voltage divider, keeping the drain voltage V_{D2} in Fig. 4.32(a) above 15 V.

Fig. 4.33 provides the frequency trend of gain, output power and efficiency. It can be seen that due to the narrow BPF used in the output matching network the efficiency quickly degrades when deviating from the design frequency of 2.6495 GHz. Due to the low gain the PAE significantly degenerates compared to the Drain Efficiency (DE). The difference



(a) Low power transistor (T_2) (b) High power transistor (T_1)

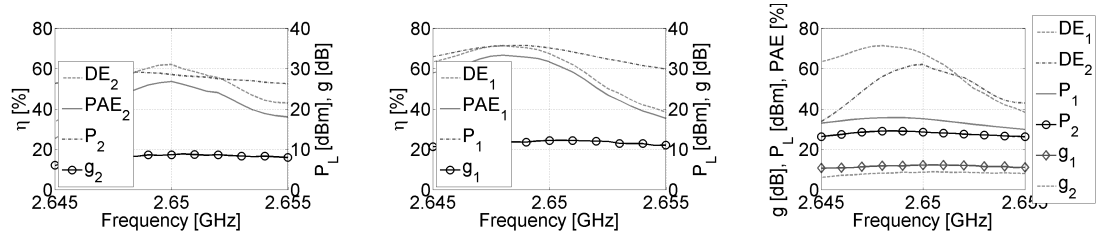
Figure 4.31: Drain current of both transistors for low power mode.



(a) Low power transistor (T_2) (b) High power transistor (T_1)

Figure 4.32: Drain current of both transistors for high power mode.

between the output powers of both operational conditions is roughly 6 dB. In the efficiency traces of both modes in Fig. 4.33(c) it can be seen that their efficiency maxima occur at different frequencies due to the different capacitive loadings of the modes caused by the series diode.



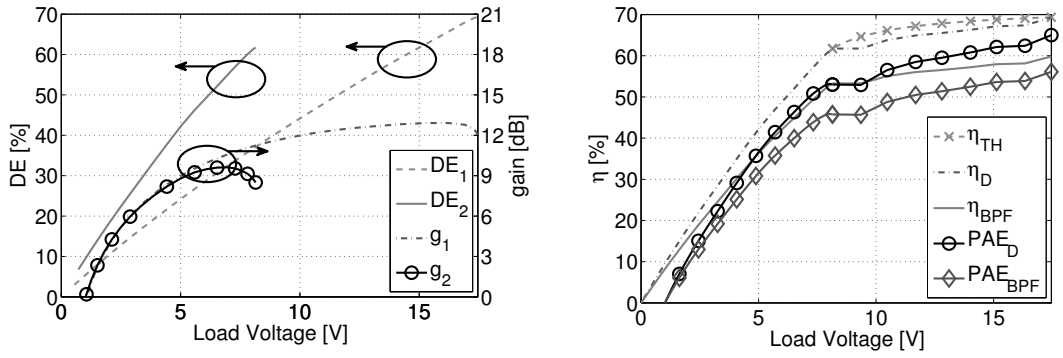
(a) Low power (b) High power (c) Both

Figure 4.33: Efficiency, gain and output power versus frequency.

The efficiency curves for the design frequency of 2.6495 GHz under static excitation are provided in Fig. 4.34(a). It can be seen that for the CW case a sawtooth like efficiency behavior can be achieved. The maximum efficiency is slightly increased compared to the common source PA, as only a single DC biasing at RF level is required allowing for an optimized matching network.

The resulting BB PWM efficiency curves versus the load voltage are given in Fig. 4.34.

Trace η_{TH} depicts the theoretical drain efficiency curve (derived in Appendix 7.4) of the circuit in Fig. 4.28, while trace η_{D} shows the simulation results for a modulation frequency of 20.7 MHz. The difference between the two traces is attributed to the residual losses in the modulation sidebands and due to signal transitions. The gain for the low power region with 8.6 dB is however limited leading to a reduced power added efficiency $\mathrm{PAE_D}$. For the high power operation with 3 W output power, the gain is around 12 dB leading to an improvement in $\mathrm{PAE_D}$. The negative PAE for very low output voltages is caused by the class C gate biasing. When considering the insertion loss of 0.65 dB of the matching network and the filter, the drain efficiency η_{BPF} and the power added efficiency $\mathrm{PAE_{BPF}}$ are further decreased.



(a) Static CW

(b) BB PWM

Figure 4.34: Efficiencies versus load voltage for a carrier frequency of 2.65 GHz and 20.7 MHz modulation frequency.

Nevertheless efficiencies still show the highly efficient operation of the direct filter connection after the BPF. Thus the common drain PA is capable of improving the efficiency significantly compared to a standard class B efficiency implementation.

4.3.3 Switchable Cascode PA

Cascodes are widely used in analog CMOS circuits and power amplifiers to increase gain and voltage swing by distributing the voltage drop among the stacked transistors [216–222]. In all these designs reduced input power, respectively gate drive, reduces the drain voltage swing on the transistors and degrades the efficiency according to the class of operation [10]. This results in general in poor efficiency for low output power. A possible method to regain efficiency in back off is to perform (discrete) supply modulation [223], which is also known as envelope tracking. Traditionally envelope tracking tackles the problem by modifying the drain voltage of the PA and requires therefore a rather broadband envelope tracking PA and special baseband matching to cope with the envelope expansion of the signal. The switched cascode avoids this problem by using a second supply voltage level inherently available in cascode circuits. To do so the source potential of the upper cascode transistor $\mathrm{T_1}$ is modified according to the signal's amplitude. This is done by adding a switch between the intermediate supply level ($\mathrm{V_{DC2}}$) and the two transistors, as depicted in Fig. 4.35 [S9, S10].

When the switch is open the circuit acts like a conventional cascode and the drain voltage ($\mathrm{V_{D1}}$) drops equally across both transistors. Corresponding time domain waveforms for the drain voltages and currents under class B bias and maximum drive for a carrier frequency of 2.65 GHz are given in Fig. 4.36(b).

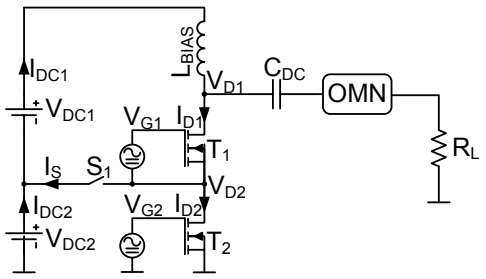
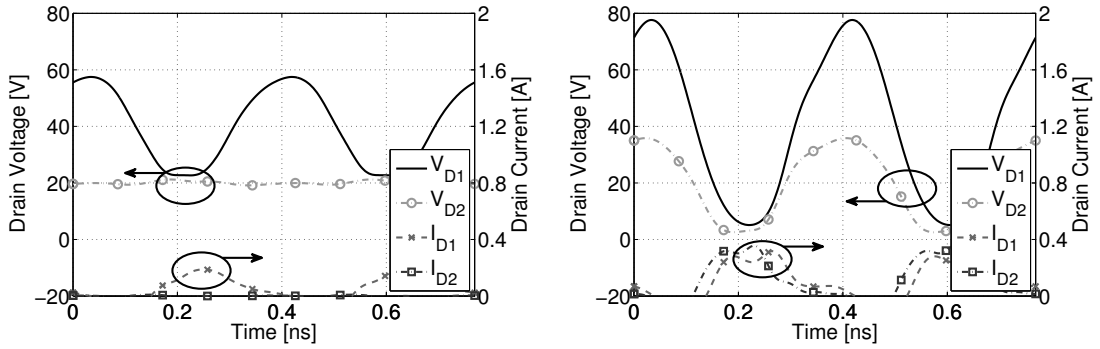


Figure 4.35: Switchable cascode general circuit.



(a) Switch closed (normal PA)

(b) Switch open (cascode)

Figure 4.36: Simulated drain voltages and currents for operation at 2.65 GHz with switch open/closed.

It can be seen that the drain currents of both transistors I_{D1} and I_{D2} are equal, as the switch is open and no current flows through it ($I_S = 0$). The voltage is shared equally among the two transistors enabling a higher voltage swing.

By closing the switch S_1 and applying no gate signal to the lower transistor T_2 it is possible to disable the lower part of the cascode [S9, S10]. Due to the class B bias no drain current I_{D2} flows, although the applied drain voltage is equal to the lower supply voltage as the switch S_1 is closed. This can be seen in the time domain waveforms of the drain voltages and currents in Fig. 4.36(a). As there is no drain current I_{D2} the resulting power consumption of the lower supply is zero, meaning that the lower part of the cascode is completely powered down. The power generation is done by the upper cascode transistor T_1 only, which operates now as a normal PA with some DC voltage offset, which can also be observed in Fig. 4.36(a).

The drain current I_{D1} flows now through the switch I_S and back into the upper power supply V_{DC1}. As the lower supply current I_{DC2} and the input power P_{IN2} are zero, the lower part of the circuit ideally does not consume any power for this type of operation.

For the circuit implementation a GaN MMIC process [215] was chosen, to benefit from the high supply voltages and low parasitics. The high power density of GaN and the use of cascodes allows to easily achieve output powers in the watts range [219–222]. In Fig. 4.40(b) the schematic of the switchable cascode implementation is depicted. The design is split into an integrated part, which contains the cascode circuit and some prematching. The final Input Matching Network (IMN) and Output Matching Network (OMN) are done on board level. This enables the use of high-Q passives and tuning after manufacturing. In Fig. 4.40(b) the layout of the die is depicted. The main circuit consists of the two cascode transistors T_1 and T_2 and the switch S_1. For these transistors 4x100μm HEMTs with

a maximum current of around 400 mA were used. To provide a stable on chip supply voltage V_{DC2} of 20 V when the switch is closed, the shunt capacitor C_B was added. Its parasitic self resonance frequency was designed to match the carrier frequency to provide low impedance. The supply voltages V_{DC1} and V_{DC2} were set to 20 V.

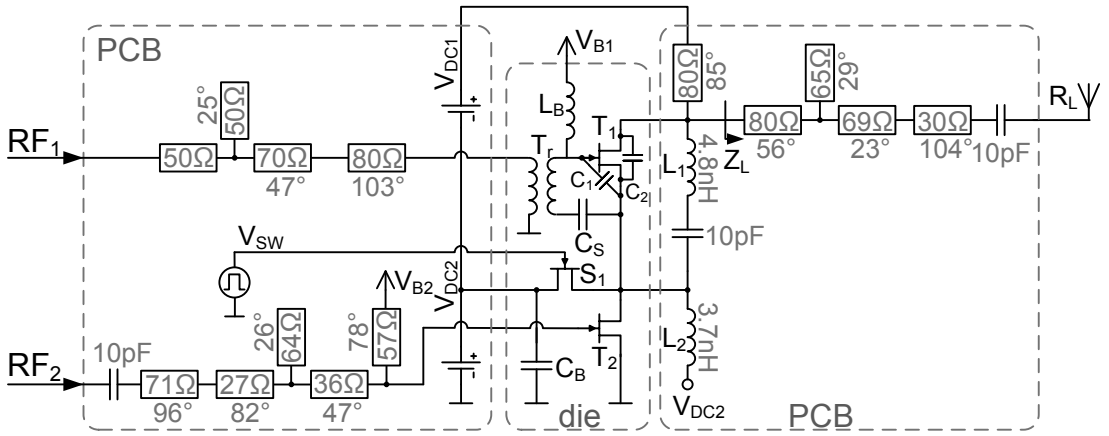


Figure 4.37: Switchable cascode implementation with broadband load.

In conventional cascode structures in GaN technology the gate-source voltage of the upper transistor is controlled by its own source potential. In order to not overdrive the gate, a capacitive voltage divider, consisting of the parasitic gate-source capacitance and a series capacitor, is used. The division ratio is set in such a way that equal voltage and power splitting is achieved [219–221]. This approach would require very large voltage swings (full drain voltage swing) due to the series capacitor for the signal input of the upper transistor when being in normal PA operation (switch closed). Therefore, it was decided to actively drive the upper transistor also during cascode operation. To decouple the required gate signal from the source voltage swing a transformer was used. During the design of the transformer T_r attention was paid to minimizing the parasitic capacitance of the transformer to avoid increased capacitive feedback. This is necessary to provide the same input impedance for both operational conditions as the capacitive feedback results in a kind of load modulation for the gate impedance during cascode operation.

The gate biasing of the transistor T_1 is done with the biasing inductor L_{BIAS}. In order not to short circuit the biasing, the transformer has to be decoupled by the series capacitor C_S. In addition the capacitor C_1 in parallel to the gate and source of T_1 was added to resonate out the transformers inductance and to further reduce the capacitive feedback ratio. When the switch is off, during normal cascode operation, it loads the circuit with its parasitic drain-source capacitance, effectively doubling the drain-source capacitance of T_2. This would result in an unequal voltage division between the two transistors due to the parasitic capacitive voltage divider at the drain of the transistors. To prevent this the drain-source capacitance of T_1 is increased by adding the parallel capacitor C_2 to its drain. The same effect could also be achieved by increasing the width of T_1. But with this architecture the optimum load resistance would differ too much for normal PA operation (switch closed), where T_1 already sees twice optimum the load impedance and doubling its size would mean that it sees four times the optimum load impedance resulting in lower efficiency in back off. To achieve stability, resistors were added to the gate of both transistors, with the major focus on the upper transistor T_1.

For the output matching a combination of microstrip lines based on Rogers 4350B substrate and lumped components was considered. To be capable of providing the correct load impedance for both operational conditions the drain-source capacitance of each cascode

transistor T_1 and T_2 has to be resonated out individually (using L_1 and L_2), such that the remaining required load impedance is purely resistive. This is necessary because when the switch is closed there is no voltage swing on the lower transistor T_2 and the resulting parallel capacitance is only the drain-source capacitance of the upper transistor T_1. Whereas for cascode operation the parallel capacitance consists of both parasitic capacitances. If only a single compensation would be used it would not be possible to compensate the capacitances for both operating conditions leading to non optimum load impedances.

To compensate the drain-source capacitances 0201DS SMD inductors from Coilcraft are placed in parallel to the transistors T_1 and T_2. Instead of being DC-wise decoupled the lower compensation inductance L_2 can be connected to the intermediate supply voltage V_{DC2} as both circuit nodes have the same DC potential. For the DC decoupling of the inductor L_1 and for all other capacitors the ATC600S series from American Technical Ceramics was considered. For the simulation models including not only the first but also higher order self resonances have been used [224].

The resulting drain voltage and current waveforms for the circuit given in Fig. 4.37 for operation at maximum power at 2.65 GHz are depicted in Fig 4.36(b). It can be seen that both drain currents have the same phase and amplitude implying that the two gate signals are well aligned. The voltage drop is shared equally amongst the two transistors due to the above described measures. As the output matching was optimized to provide highest efficiency, thus reduced overlap of voltage and current, the resulting drain voltages are not sinusoidal as for pure class B operation. The voltage at the switch V_{SW} has to be pulled down to 0 V in order to avoid conduction of the parasitic gate-drain diode of the switch S_1. This requires a rather large voltage swing of 20 V to switch between the two operational states.

In Fig. 4.36(a) the drain voltage and current waveforms for normal PA operation and maximum power for the closed switch are given. It can be seen that the lower part is disabled as no drain current I_{D2} flows. Only a small residual drain voltage swing for V_{D2} remains due to the finite ON resistance of the switch.

A graph providing the gain and power added efficiency versus load voltage is shown in Fig. 4.38. For cascode operation, as depicted in Fig. 4.36(b), the resulting 64.1 % power added efficiency is given in trace PAE_H. The corresponding gain g_H is also shown, where trace g_L depicts the gain for normal PA operation. With the switch closed, the gain g_L is lower than for cascode operation, mainly due to the fact that the ON resistance of the switch acts as a source degeneration and lowers the gain. Both gain curves show an expansion, as the actual gate biasing used is in slight class C.

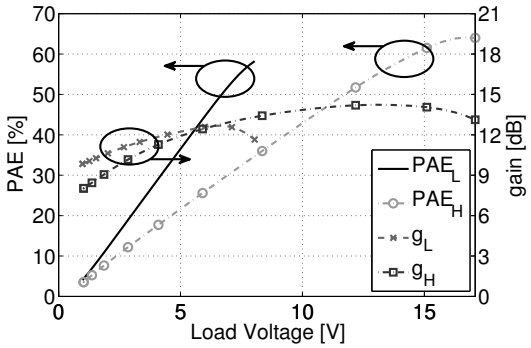
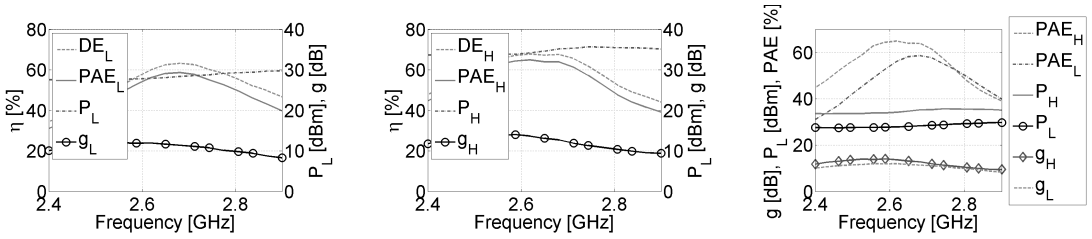


Figure 4.38: Simulated efficiency and gain versus load voltage for both operating conditions at 2.65 GHz for the broadband load circuit in Fig. 4.37.

For normal PA operation an efficiency peak PAE_L (8 V) below half the maximum load

voltage (17.1 V), at 6.5 dB back off can be achieved. Its maximum is with 58.2 % slightly lower than for cascode operation. This is due to the fact that the load impedance is not split between the two transistors, as for cascode operation, resulting in twice the optimum load impedance. Thus the transistor T_1 operates less efficiently. The second contributor to reduced efficiency is the ON resistance of the switch. It shall be noted that the position of the efficiency peak may be changed by modifying the supply voltages.

The frequency behavior of the circuit is also important, as depicted in Fig. 4.39(c). Efficiency is largest for the design frequency of 2.65 GHz and declines moderately when deviating from the center. For higher frequencies the efficiency for cascode operation PAE_H becomes smaller than the efficiency for normal operation PAE_L.



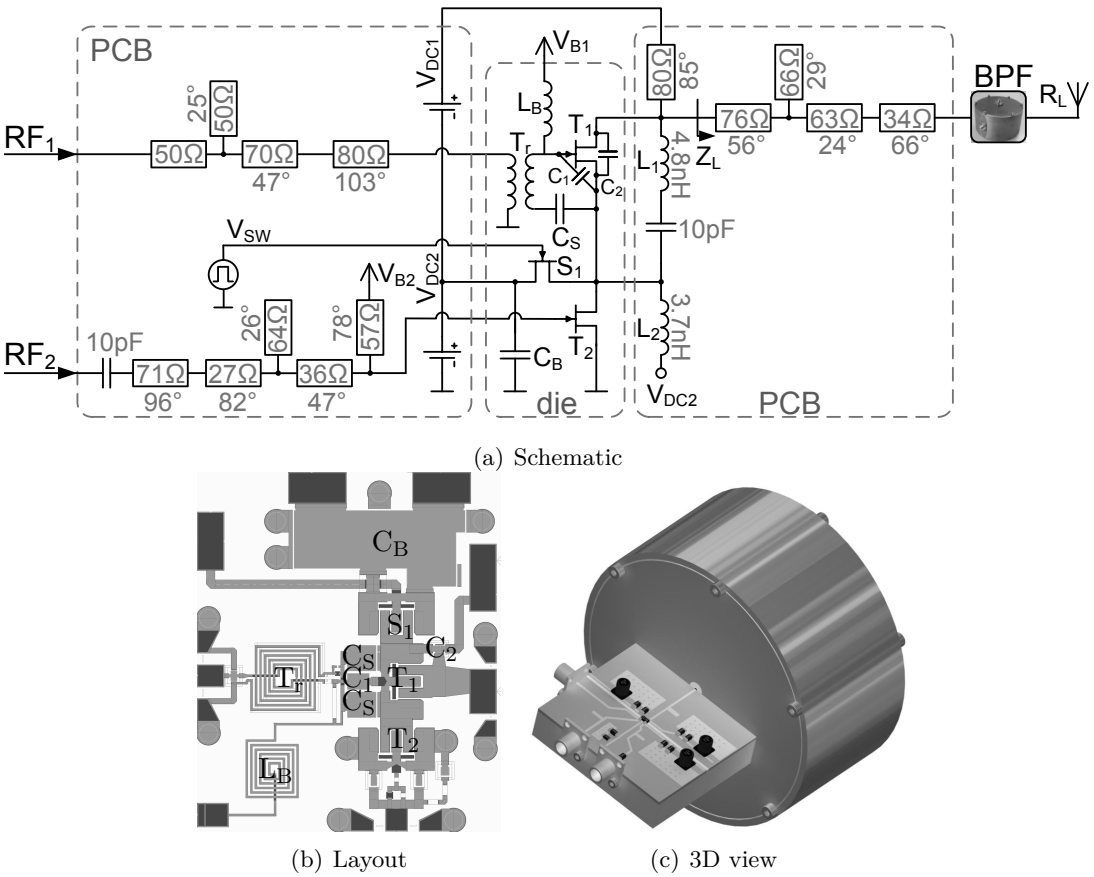
(a) Low power (b) High power (c) Both

Figure 4.39: Efficiency, gain and output power versus frequency for the broadband load circuit in Fig. 4.37.

This is caused by the fact that the resulting impedance for that frequencies is smaller compared to the design frequency and for cascode operation maximum voltage swing cannot be achieved anymore. The peak power for cascode operation P_H increases a bit with frequency and reaches 2.74 W at the center frequency of 2.65 GHz. For normal PA operation the peak power at back off P_L remains around 0.57 W over frequency. The gain g_H and g_L for both operational conditions varies in the same manner due to the frequency dependence of the input matching. It shall be noted that the matching networks have not been optimized for broadband operation leaving margin for improvement.

By using a CW excitation the efficiency trace can be improved from a class B efficiency trace to a sawtooth like curve, as depicted in Fig. 4.38. This efficiency curve can be further improved to a Doherty like efficiency behavior by using BB PWM. Therefore, the load of Fig. 4.37 is connected via a BPF to remove the modulation sidebands. In order to avoid any feedback to the PA an isolator is placed between the PA and BPF. The resulting efficiency enhancement is provided in Fig. 4.43(a). For the high power region the theoretical efficiency η_{TH} derived in Appendix 7.4 corresponds well with the simulated drain efficiency η_D. The gain of around 12 dB, respectively 13 dB, leads to a reduction in PAE_D compared to the drain efficiency η_D. Considering the 0.53 dB insertion loss of the BPF (in a 50 Ω environment) the drain efficiency η_{BPF} and PAE_{BPF} are further reduced. But they still show the good efficiency curve similar to a Doherty PA.

A drawback of the isolated BB PWM operation is that the power in the modulation sidebands is dissipated in the isolator leading to reduced efficiency. Direct filter connection reduces this dissipated power by providing a high impedance for the modulation sidebands and thus improving efficiency. Fig. 4.40 depicts the switchable cascode circuit with the output matching network optimized for direct filter connection. The main difference to the circuit shown in Fig. 4.37 is that the BPF is connected directly to the PA in order to provide high impedance for the modulation sidebands for a wide frequency range. The resulting arrangement of the filter-microstrip line codesign for the output matching network is given in Fig. 4.40.



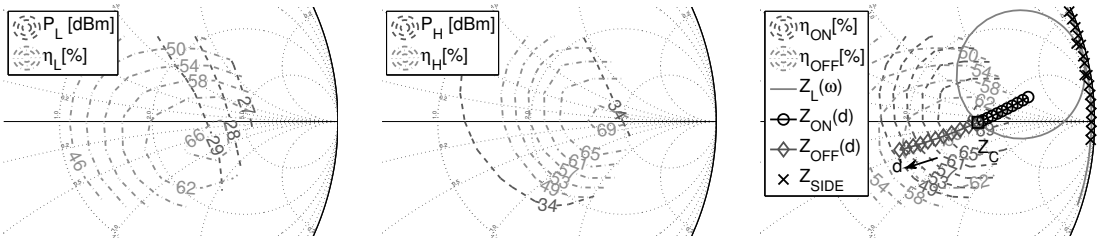
(a) Schematic

(b) Layout

(c) 3D view

Figure 4.40: Switchable cascode implementation with direct filter connection.

For the design of the output matching network the LP contours for both operational states, as provided in Fig. 4.41, are of importance. It can be seen that by individually compensating the parasitic capacitances the efficiency maxima for both operational states are close to the real axis. During the design the orientation of the resonance locus of the load impedance Z_L was set such that the load modulation trajectories for the low power period Z_{OFF} and for the high power period Z_{ON} follow efficient regions. By moving the BPF close to the PA it is possible to provide the desired high impedance Z_{SIDE} for the modulation sidebands considering 20.7 MHz BB PWM frequency.



(a) Low power (S_1 closed)

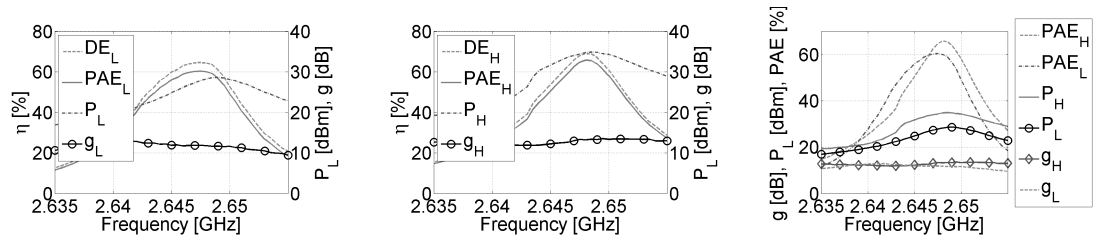
(b) High power (S_1 open)

(c) Both

Figure 4.41: Load pull efficiency contours, matching network and load modulation trajectories for a carrier frequency of 2.648 GHz for the direct filter connection circuit in Fig. 4.40.

The frequency performance of the direct filter connection circuit presented in Fig. 4.40(a) is dominated by the response of the band pass filter, as can be seen in Fig. 4.42. The

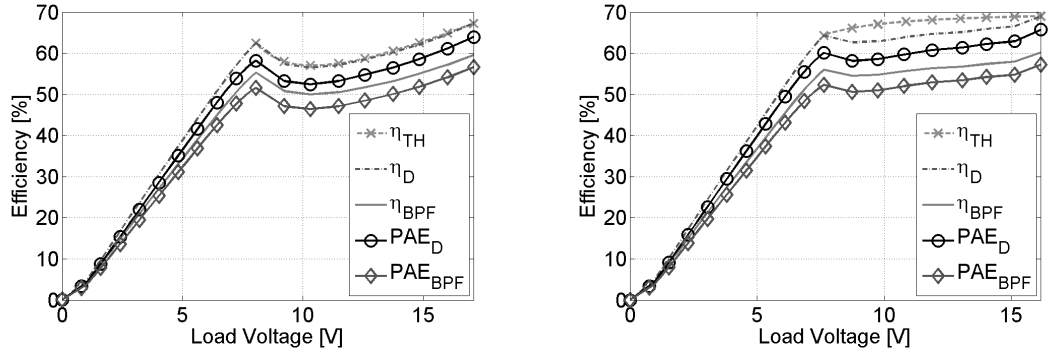
output power, as well as efficiency follow the band pass nature of the filter. Compared to the broad band design of Fig. 4.37 the bandwidth is significantly reduced. But this behavior is a result of the requirement for high impedance at the modulation sidebands and therefore required for the highly efficient BB PWM operation around the design frequency of 2.648 GHz. When comparing the efficiency curves in Fig. 4.42(c) for both operational modes it can be seen that their maxima are well aligned in terms of frequency. This is due to the fact that the parasitic capacitances are almost equally compensated for both operational modes. If only a single compensation inductance (instead of L_1 and L_2) would be used to resonate out the C_{DS} of both transistors it is not possible to achieve a purely resistive load for both operating conditions simultaneously. Thus the efficiency curves would differ significantly in terms of frequency, making efficient operation for both conditions impossible.



(a) Low power (b) High power (c) Both

Figure 4.42: Efficiency, gain and output power versus frequency for the direct filter connection circuit in Fig. 4.40.

Fig. 4.43(b) depicts the efficiency of the direct filter connection circuit versus the load voltage. It can be seen that the drain efficiency η_D is improved compared to the isolated operation depicted in Fig. 4.43(a). But due to residual losses in the modulation sidebands and during the signal transitions the drain efficiency η_D falls behind the theoretical possible efficiency η_{TH} for direct filter connection. The gain of around 13 dB leads to a small reduction of PAE_D compared to the drain efficiency. Accounting for the 0.682 dB insertion loss of the matching network reduces the drain efficiency η_{BPF} and PAE_{BPF} after the BPF accordingly. Nevertheless the efficiency behavior still shows the highly efficient connection of the two efficiency peaks due to the direct filter connection.



(a) Isolator (Fig. 4.37) (b) Direct filter (Fig. 4.40)

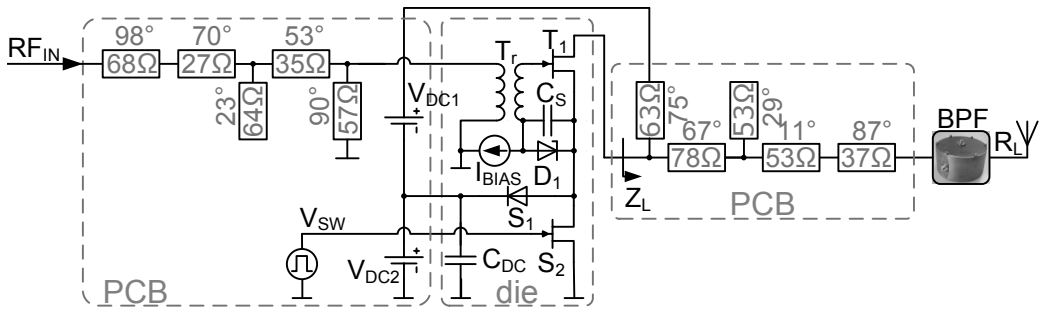
Figure 4.43: Simulated efficiency enhancement by BB PWM with and without direct filter connection.

It can be concluded that the switchable cascode is a PA structure capable of providing an

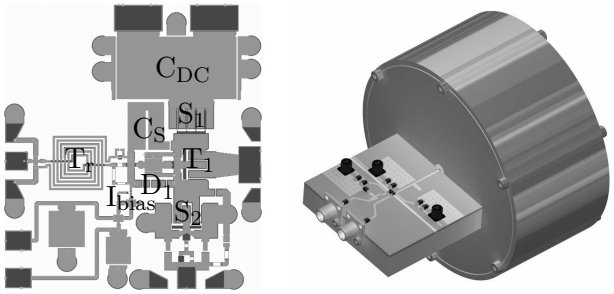
efficiency peak in back off. By combining it with BB PWM the efficiency can be improved to a Doherty behavior trend. Beside that the switchable cascode is perfectly suited for direct filter connection with its constant drain current. With the direct filter connection the two efficiency peaks can be connected in a highly efficient way.

4.3.4 Source Modulated Amplifier

The source modulated amplifier is based on modifying the source potential to provide two operational points with maximum voltage swing and thus maximum efficiency [S11]. By modifying the source potential of the transistor the RF biasing and the DC envelope tracking networks are separated. To simplify the concept only two discrete values were considered. The schematic of the source modulated amplifier is depicted in Fig. 4.44(a) and is similar to the switchable cascode PA circuit. The main difference is that the active switch S_1, with its high control voltage, can be replaced by a diode (S_1). Its core is designed in a GaN MMIC process [215] in order to provide lowest parasitics and compact integration of the source modulation circuitry to ensure proper operation. The corresponding layout is given in Fig. 4.44(b).



(a) Schematic



(b) Layout

(c) 3D view

Figure 4.44: Schematic of the source modulated PA.

The actual PA circuit consists of the transistor T_1 and its input matching. The source modulation is done by the switches S_1 and S_2. By splitting the DC supply and using a special biasing scheme the source potential of T_1 can be switched between 0 V and V_{DC2}. The switch S_1 can be implemented as a diode, requiring only S_2 to be controlled. To provide a stable source voltage an on chip shunt capacitor C_{DC} is included, which has its self resonance frequency close to the carrier frequency.

As the source potential of transistor T_1 is modulated the biasing and the generation of the correct gate signal requires special attention. To decouple the RF signal from the source potential a transformer T_r is used. For the bias generation a series capacitor C_S has to be included. The actual biasing is done with the help of a reference diode and a constant current source I_{bias}. The diode D_1 is implemented as a series connection of 4 diodes to

provide the correct reference voltage for slight class C biasing. For the reference current generation a small transistor with constant gate bias was used.

When combining the source modulated PA with the direct connection of a series resonator highly efficient operation within the region of the low power (V_{DC1}=15 V) and high power mode (V_{DC1}+V_{DC2}=30 V) can be achieved. Fig. 4.45 depicts exemplary drain current and voltage for a duty cycle of 50 %. For illustrative purposes the high modulation frequency of 132.5 MHz was chosen. The source potential is changed according to the duty cycle by a high power digital inverter driving S_2. During the ON period the switch S_2 is closed and the power transistor T_1 is operated with its maximum voltage swing and thus maximum efficiency.

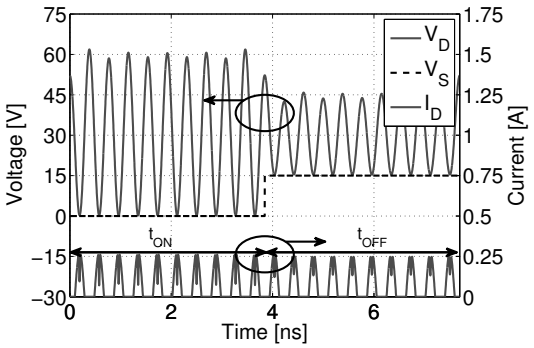
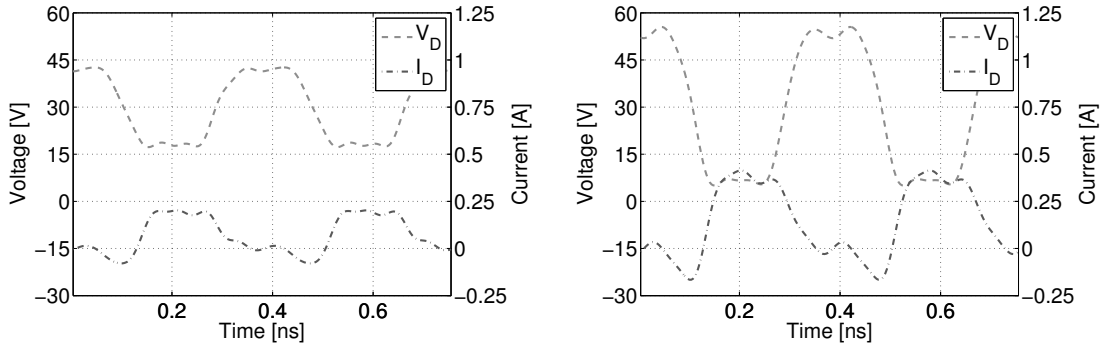


Figure 4.45: Exemplary drain voltage and current for the source modulated PA for a PWM frequency of 132.5 MHz, a carrier frequency of 2.65 GHz and a duty cycle of 50 %.

During the OFF period the switch S_2 is open and S_1 is conductive causing the source potential V_S to be shifted to 15 V. Also in this operational regime the power transistor T_1 is operated at its maximum voltage swing and highest efficiency.

To achieve best performance and to enable tuning after manufacturing the input matching network and the output matching network are implemented on PCB level. For best performance of the direct filter connection a codesign of the cavity band pass filter and the PCB output matching was done. The measured data of the cavity filter presented in section 4.2.3.3 was used for the BPF, while for the PCB a Rogers 4350B substrate was considered. The resulting arrangement is depicted in Fig. 4.44(c).

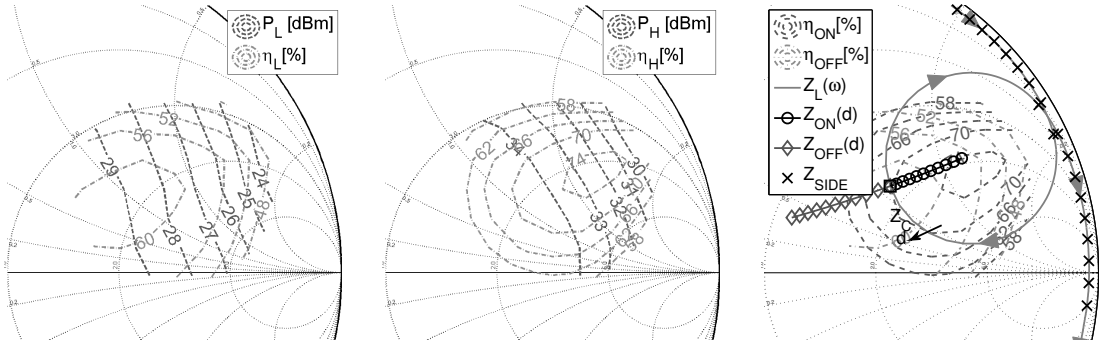


(a) Low power (b) High power

Figure 4.46: Drain current and voltage for both operational modes.

For the design of the output matching network the load pull contours of both transistors, respectively operational modes, are important. The corresponding drain efficiency

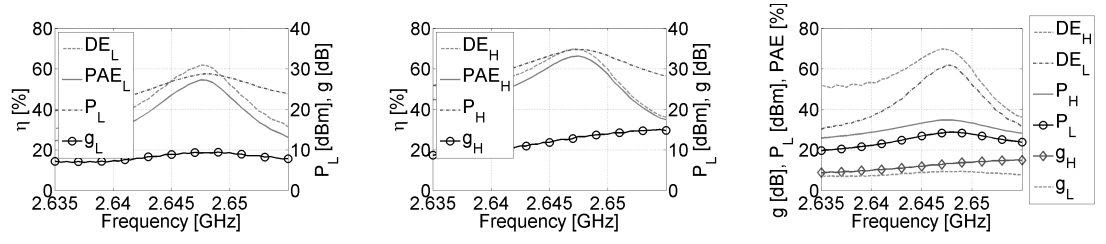
contours η_{ON} and η_{OFF} for both supply voltages are plotted in Fig. 4.47. The efficiency maxima are different in resistance due to different biasing. For best average performance the focus was set on the efficiency for the low power operation. Therefore, the impedance at carrier frequency Z_C and the higher order harmonics' termination were optimized to obtain best efficiency in back off. Beside the impedance Z_C at the carrier frequency the resulting modulation trajectories are important. They depend on the impedance at carrier frequency and the orientation of the resonance locus, as covered in section 4.2.1. Due to the fact that the resulting drain voltage PWM signal for the operation between V_{DC2} and $V_{DC1}+V_{DC2}$ has an offset, the resulting load modulation is limited to a range with good efficiency. The resonance locus was set such that the load modulation trajectories Z_{ON} and Z_{OFF} of both operational modes follow efficient regions. Additionally the impedances Z_{SIDE} for the first 10 modulation sidebands for a modulation frequency of 20.7 MHz are indicated.



(a) Low power (S_2 open) (b) High power (S_2 closed) (c) Both

Figure 4.47: Load pull efficiency contours, matching network and load modulation trajectories for a carrier frequency of 2.648 GHz.

The dependence of the gain, output power and efficiency on the frequency is given in the corresponding plots in Fig. 4.48. The band pass filter dominates the frequency behavior of the circuit and allows for highest efficiency at the design frequency of 2.648 GHz. When comparing the efficiency maxima in Fig. 4.48(c) for both operational modes it can be seen that they fit very well in terms of frequency. This is due to the fact that the same transistor is active for both operational modes and no modification of the parasitic capacitance compared to the parallel PA or the switchable cascode occurs.

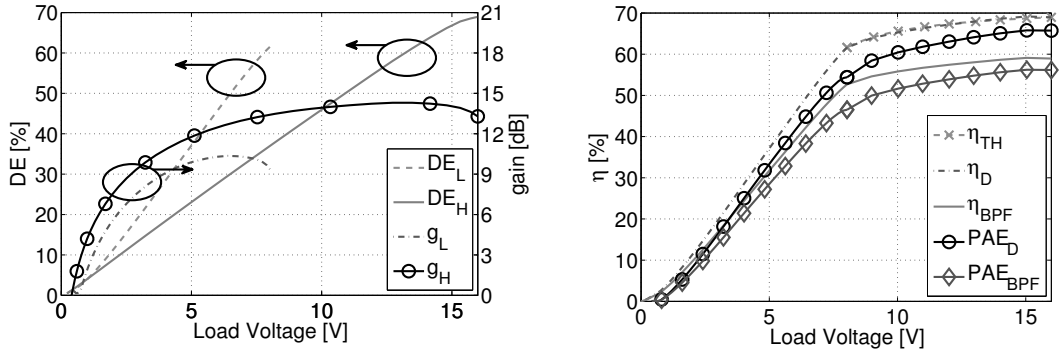


(a) Low power (b) High power (c) Both

Figure 4.48: Efficiency, gain and output power versus frequency.

Fig. 4.49(a) depicts the efficiency of the source modulated PA under CW excitation. It can be seen that the sawtooth like efficiency behavior for a dual supply concept can be achieved. By combining this property with BB PWM and direct filter connection the efficiency can significantly be improved. The resulting efficiency curves versus the load

voltage are given in Fig. 4.49(b). Trace η_{TH} depicts the theoretical drain efficiency curve of the circuit in Fig. 4.44 according to (7.114) derived in Appendix 7.4, while trace η_{D} shows the simulation results for a modulation frequency of 20.7 MHz. It can be seen that both traces are in good agreement. Unfortunately the gain for the low power region with 9.3 dB is rather limited leading to a reduced power added efficiency $\mathrm{PAE_D}$. For the high power operation with 3 W output power, the gain is around 13.4 dB leading to an improvement in $\mathrm{PAE_D}$. When considering the insertion loss of 0.68 dB of the matching network and the filter the drain efficiency η_{BPF} and the power added efficiency $\mathrm{PAE_{BPF}}$ are further decreased.



(a) Static CW

(b) BB PWM

Figure 4.49: Efficiencies versus load voltage for a carrier frequency of 2.648 GHz and 20.7 MHz modulation frequency.

It can be summarized that the source modulated PA is well suited to provide an additional efficiency peak in back off region due to its two source potentials. When combining the source modulated PA with the concept of direct filter connection highly efficient operation can be achieved. Another advantage of the source modulated PA is that only a single transistor is active for both operational conditions, reducing the required control signals compared to the parallel PA or the switchable cascode. A single RF signal and the digital signal for the source modulation are sufficient for proper operation. The use of a single active transistor also allows for a compact and efficient output matching network design. The fact that the RF signal has not to be multiplexed between two transistors and that the source modulation is decoupled from the drain signal leads to reduced transition losses between the two states. This results in a drain efficiency η_{D} close to the theoretical limit.

4.3.5 BPSK DC Energy Recovery

The concept of DC BPSK energy recovery is introduced in [202] and is based on a modified BB PWM and direct filter connection. One of its main advantages is that it can be implemented using a single (discrete) RF transistor. While the general operational principle is considered in section 3.7.4, this section is dedicated to the analysis of its practical applicability.

The block diagram of DC BPSK energy recovery is given in Fig. 4.50. The circuit consists of a PA, being capable of operating in amplifier and rectifier mode and a band pass filter directly connected to it. The band pass filter is designed to emulate the behavior of a series resonator, providing high impedance for the modulation sidebands and requiring a constant current. Instead of switching the PA on and off, the PA is operated continuously, driving the series resonator with opposite phases (biphase) for each period. The resulting driving signal is the same as for Binary Phase Shift Keying (BPSK) but can also be

represented by a PWM signal with amplitude 2 and an offset of -1, as can be seen from the drain voltage envelope V_D in Fig. 4.50.

During the first period the drain voltage V_{D1} and the drain current I_D are positive and the PA is operated as a regular amplifier driving the band pass filter. But during the second period the drain voltage V_{D2} is negative while the drain current I_D is still positive due to the series resonator. This provides a negative resistance to the PA resulting in rectifier operation recovering a part of the generated energy and leading to an improvement in efficiency.

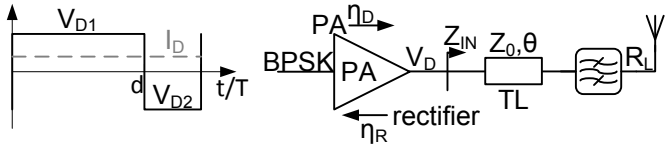


Figure 4.50: Block diagram biphase energy recovery.

An important requirement for the design of a biphase energy recovery transmitter is that the used PA is able to efficiently operate as an amplifier as well as a rectifier. In section 2.7 different PA classes being capable of also serving as rectifier have been presented. Amongst them the class E PA was selected due to its high efficiency and switching nature, suitable for purely digital control signals. Fig. 4.51 depicts the corresponding implementation [S4]. It shows a class E PA design with a GaN transistor (Cree CGH60008D) connected to a BPF with a transmission line (TL) matching network that provides the required impedances at the carrier harmonics and the fundamental frequency. For the gate drive a high power driver [225] was considered providing a rectangular driving signal.

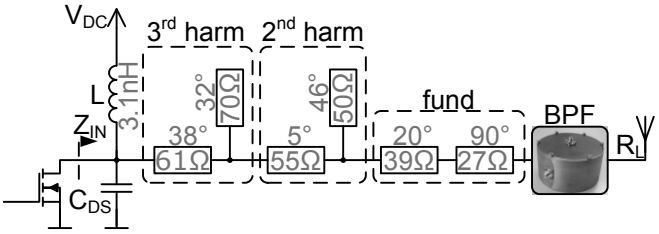
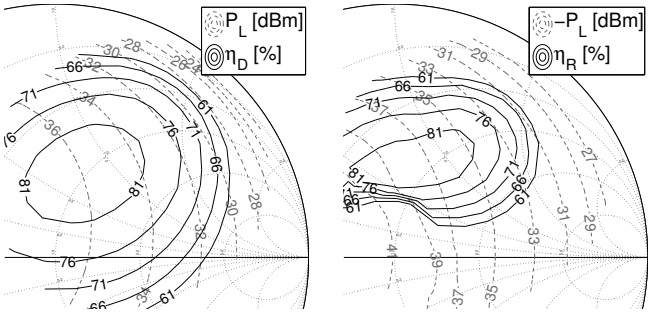


Figure 4.51: Schematic of GaN class E biphase energy recovery transmitter using transmission line matching and a cavity resonator.

To achieve best PA, respectively rectifier, efficiency it is important to provide the correct load impedances. This can be well seen in the LP contours in Fig. 4.52, which provide the data for the class E PA of Fig. 4.51 with a supply voltage of 18 V. Fig. 4.52(a) depicts the LP contours of the drain efficiency η_D in 5 % steps and the power delivered to the load P_L in 2 dBm steps for the amplifier operation mode. In Fig. 4.52(b) the corresponding data for rectifier operation (receiving power) is provided. Here the negative complex conjugate of the applied load impedance Z_{IN} is plotted to achieve contours located within the smith chart.

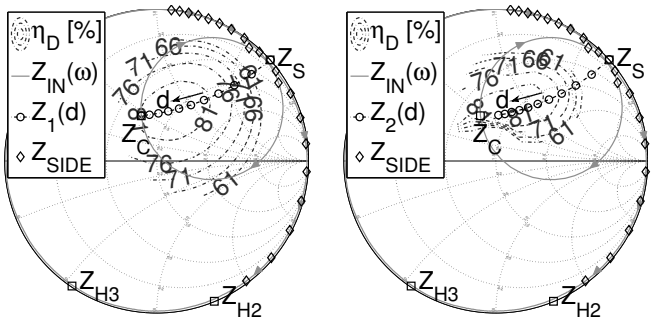
To get best system performance it is important that the load modulation trajectories for PA and rectifier operation follow the efficient regions in Fig. 4.52. To achieve that the matching network including the band pass filter has to be designed in such a way that the orientation of the resonance locus, which defines the load modulation trajectory, allows for efficient operation. The symmetry impedance Z_S was optimized to provide optimum trajectories of the resulting load impedances Z_1 and Z_2 in Fig. 4.53. During the design of the fundamental matching both requirements for Z_C and Z_S were considered to get best



(a) Amplifier ($Z = Z_{IN}$) (b) Rectifier ($Z = -Z_{IN}^*$)

Figure 4.52: Load Pull contours at the intrinsic transistor plane for drain efficiency η_D and output power P_L at a carrier frequency of 2.648 GHz.

performance. The second (Z_{H2}) and third harmonic impedances (Z_{H3}) were tuned to get class E operation. Measured S-Parameters from the filter presented in section 4.2.3.3 were used for simulation.

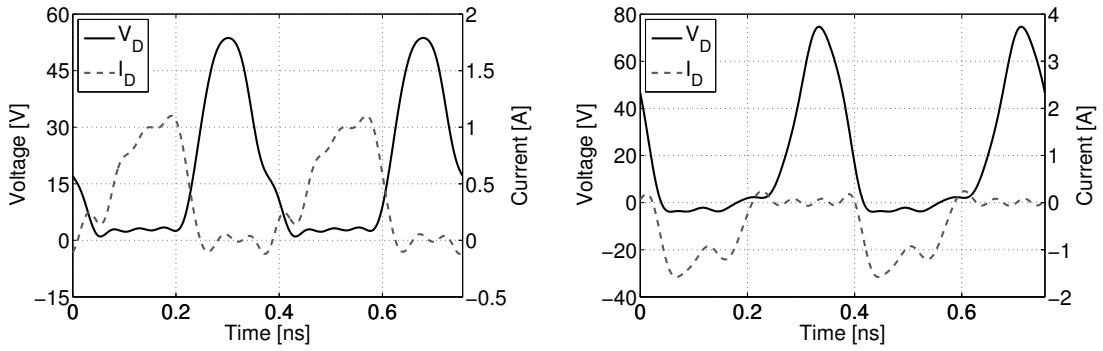


(a) Amplifier ($Z = Z_{IN}$) (b) Rectifier ($Z = -Z_{IN}^*$)

Figure 4.53: Load pull contours at the intrinsic transistor plane for drain efficiency η_D and load modulation trajectories at a carrier frequency of 2.648 GHz.

The resulting time domain waveforms for amplifier and rectifier operation of the class E circuit are provided in Fig. 4.54. It can be seen that the overlap of drain current and voltage for amplifier operation in Fig. 4.54(a) is minimized and that the waveforms approximate class E behavior. For the rectifier operation, as depicted in Fig. 4.54(b) the drain current is negative while the drain voltage remains positive. This allows for the recovery of energy. Thanks to the minimum overlap of voltage and current for both operational conditions high efficiency can be achieved.

In Fig. 4.55 the resulting efficiency versus the load voltage is given. Trace η_D shows the drain efficiency at the intrinsic transistor plane for the desired biphase energy recovery operation. At the maximum output power of 37.1 dBm it reaches a maximum efficiency of 81.9 %. But for lower output power the efficiency is lower than the theoretical efficiency curve η_{LP} derived in Appendix 7.5.4. The difference is attributed to the fact that the losses in the modulation sidebands and the signal transitions are not considered. Considering the losses of the modulation sidebands in the matching network (Z_{SIDE}) for the theoretical calculation delivers $\eta_{LP,M}$, which is close to the efficiency for biphase operation η_D. The residual losses are attributed to the signal transitions. When taking the 0.53 dB insertion loss of the filter into account the efficiency drops as depicted in trace η_{BPF}. It shall be noted that the impedances for the modulation sidebands were not optimized yet, leaving some margin for improvement.



(a) Amplifier (b) Rectifier

Figure 4.54: Drain current and voltage for PA and rectifier operation.

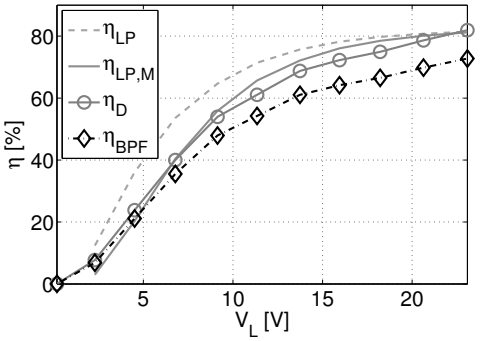


Figure 4.55: Efficiencies vs. load voltage V_L.

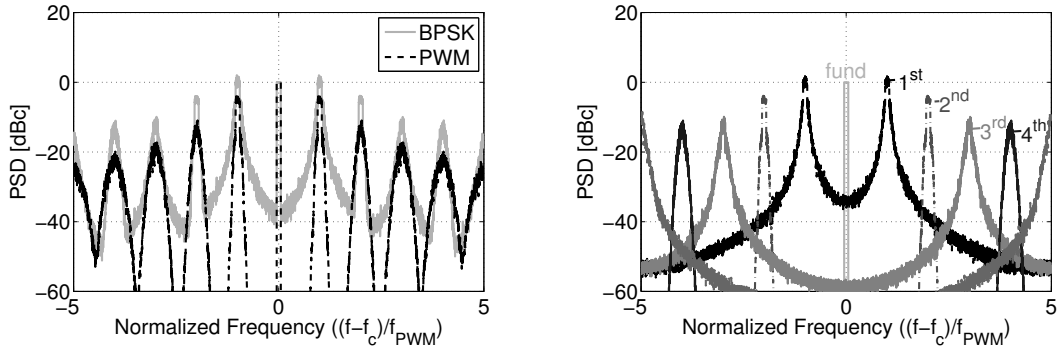
Besides efficiency the achievable spectral purity is of importance. Fig. 4.56(a) shows a comparison between the spectrum of BB PWM and BPSK encoding. It can be seen that the modulation sidebands for BPSK operation are roughly 6 dB higher than for PWM encoding. This is caused by the biphase encoding, resulting in an effective normalized amplitude of 2, which is double the value of PWM encoding. The PSD of the first modulation sideband even exceeds the inband energy, which results in an increased sensibility of the efficiency to the residual losses in the modulation sidebands. Additionally the achievable dynamic range around the inband signal is significantly reduced for the BPSK encoding.

This is due to the fact that the first modulation sideband exhibits a very wide spectrum due to the BPSK encoding, as shown in Fig. 4.56(b). The spectral expansion of the first modulation sideband dominates the achievable inband signal quality. Compared to the PWM encoding only a very small signal bandwidth for the same modulation frequency can be used in order to achieve good signal quality.

Although good efficiency can be achieved with the DC BPSK energy recovery concept, the achievable signal quality is fundamentally limited by the concept itself. As a result the range of possible applications is severely limited.

4.3.6 Switched Doherty

The Doherty PA is a well known structure to provide an efficient multilevel PA and its operational principle was already discussed in section 3.1. Beside of controlling the Doherty PA in the conventional way it is well suited for combination with multilevel BB PWM for highly efficient operation.

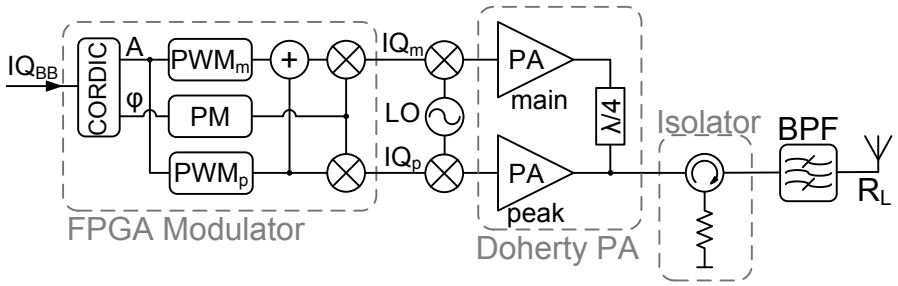


(a) BPSK vs. PWM

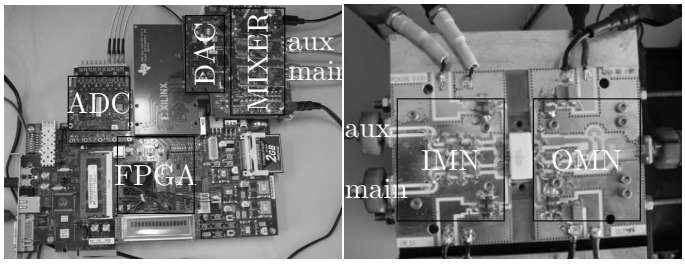
(b) BPSK composition

Figure 4.56: BPSK spectrum.

The block diagram of such a transmitter employing BB PWM on a Doherty PA can be found in Fig. 4.57(a) [226]. It consists of a modulator block, which generates the required control signals, and the Doherty PA itself. The modulator core providing the band limited multi level BB PWM signal is implemented in a Field Programmable Gate Array (FPGA) design[1]. The digital signal of the FPGA is upconverted to the analog RF using an IQ upconversion path consisting of Digital to Analog Converters (DACs) and mixers. The Doherty PA itself is implemented using discrete LDMOS transistors[1]. In order to only feed the inband signal to the antenna a BPF and an isolator are used to connect the load R_L. Pictures of the corresponding FPGA modulator and Doherty PA implementation are provided in Fig. 4.57(b).



(a) Block diagram



(b) Pictures

Figure 4.57: Multi level BB PWM implementation with FPGA and Doherty PA[1].

In the modulator the baseband signal IQ_{BB} is converted into phase φ and amplitude A. The amplitude signal is used to encode the band limited multilevel PWM signal. For the encoding of the PWM_p signal for the peak PA a normalized reference function between

[1]The FPGA design was done by M. Mataln and the PA was designed and built by C. Schuberth.

0.5 and 1 is used. The signal for the main branch PWM_m is encoded using a normalized reference function between 0 and 0.5. Thus for a normalized amplitude above 0.5 the main PA is constantly turned on, as required for Doherty operation. To account for the load modulation effect of the main PA it is required to take the peaking PA signal into account. This is done by adding the PWM_p signal to the main branch control signal to achieve optimum control of the Doherty PA.

In Fig. 4.58 the output spectrum of the FPGA for a single level band limited PWM encoding using 4 PWM harmonics is depicted. The inband signal had a bandwidth of 8 MHz and a PAPR of 7 dB, while the PWM frequency f_{PWM} was set to 25 MHz in order to provide sufficient spacing. It can be seen that around the inband signal in Fig. 4.58 a high dynamic range can be achieved by the band limited PWM approach.

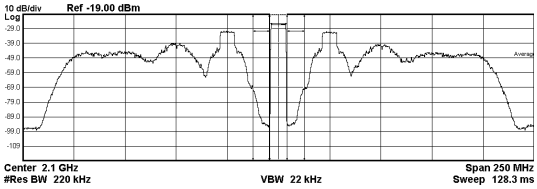


Figure 4.58: Single level FPGA output spectrum for a carrier frequency of 2.1 GHz and a modulation frequency f_{PWM} of 25 MHz with a signal bandwidth of 8 MHz.

The measured efficiency curves for a static sweep of the multi level BB PWM signal are depicted in Fig. 4.59. It can be seen that the total PAE_D at the drain including the output power of the modulation sidebands (before the BPF) remains high over the whole range. For the operation between the main and peak PA levels highest values for drain PAE_D can be held, but for very low duty cycles the efficiency drops as a result of the limited number of harmonics and related rise/fall time of the pulses. Considering the coding efficiency η_C that accounts for the losses in the modulation sidebands leads to the Doherty like efficiency curve PAE_{IN} after the BPF at the load. By mitigating the losses in the modulation sidebands through direct filter connection, PAE_D can theoretically be achieved, improving the efficiency even further.

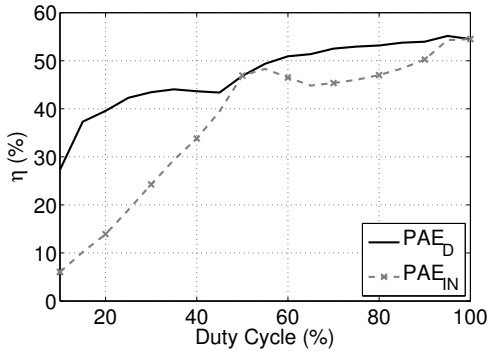
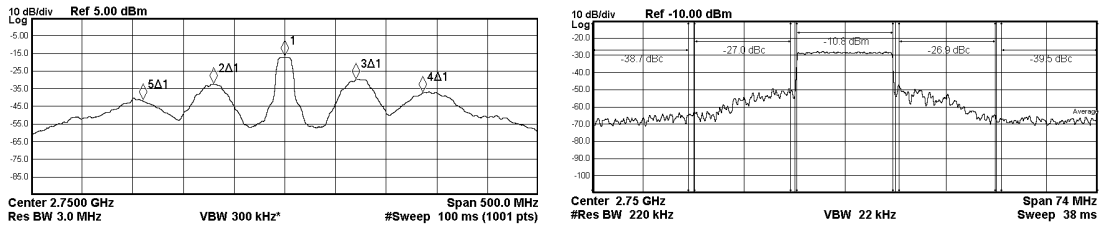


Figure 4.59: Static total PAE_D and inband PAE_{IN} for the Doherty PA and BB PWM operation at 2.75 GHz with a modulation frequency f_{PWM} of 70 MHz.

From the static efficiency measurement PAE_{IN} of the whole transmitter chain high average efficiency also for the modulated case can be predicted. Beside the achievable efficiency the output spectrum of the PA, as provided in Fig. 4.60, is of interest. It shows the output spectrum of the Doherty PA including the three modulation sidebands used to encode the inband signal with a modulation frequency of 70 MHz. The inband signal itself has a bandwidth of 14 MHz with a PAPR of 7 dB.

In Fig. 4.60(a) it can be seen that the power in the modulation sidebands is reduced for the multi level operation compared to the single level signal provided in Fig. 4.58. The achieved Adjacent Channel Leakage Ratio (ACLR) without applying predistortion was -27.0 dBc and -26.9 dBc for the lower and upper signal band respectively, as given in Fig. 4.60(b). For the next bands the ACLR goes down to almost -40 dBc, indicating possible improvements by applying predistortion. Beyond that further improvement by predistortion could be achieved if the noise between the carrier and the first PWM modulation harmonic is caused by a deviation of the intermediate output power level, leading to a discontinuity causing spectral regrowth.



(a) Full spectrum

(b) Zoom

Figure 4.60: Doherty PA output spectrum for a carrier frequency of 2.75 GHz with a modulation frequency f_{PWM} of 70 MHz and a signal bandwidth of 14 MHz.

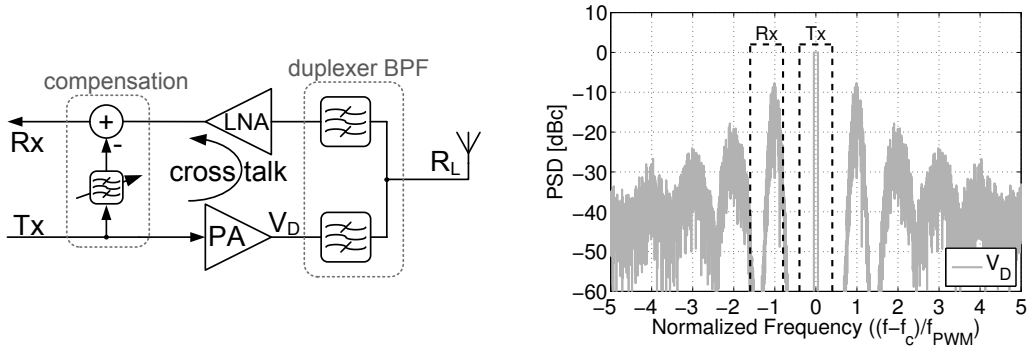
The total wideband average output power for the signal provided in Fig. 4.60 was 38.45 dBm with a coding efficiency η_C of 84.89 %, which results in an average inband power of 37.72 dBm. The average drain PAE including the total output power was 48.5 % for the 7 dB PAPR signal. Even when taking the coding efficiency into account the inband efficiency after the isolator and BPF is still high with 41.17 %.

4.4 Spectral Considerations

Beside the efficiency performance the resulting signal quality is a very important factor. In order to ensure proper communication and not to interfere adjacent channels or the own receive band disturbing proper communication, the spectral requirements have to be fulfilled.

One challenge resulting from the use of BB PWM includes the rather high signal components of the modulation sidebands next to the carrier, as depicted in Fig. 4.61(b). In order not to interfere with the adjacent channels and to fulfill ACLR requirements a BPF after PA, as shown in Fig. 4.61(a) has to be applied. The filter has to provide sufficient attenuation for the modulation sidebands for good ACLR at the load, respectively antenna.

A second effect related to the modulation sidebands is the possible jamming of the own receive band. As the receive power is much lower than the transmit power, the requirements for spectral purity are even far beyond the ACLR requirements for the receive band. For BB PWM this can be problematic as the receive band Rx may be in the vicinity of the transmit band Tx like shown in Fig. 4.61(b). A duplexer filter or a circulator can be used to provide isolation reducing the cross talk from the transmitter Tx to the receiver Rx. Even when using high quality components there will always be some residual cross talk to the receive band. But as the transmitted data interfering with the receive band is well known, the signal quality in the receive band can be improved by canceling the cross talk. This can be done either in the analog or in the digital domain [227–232] and enables proper operation of the receiver.



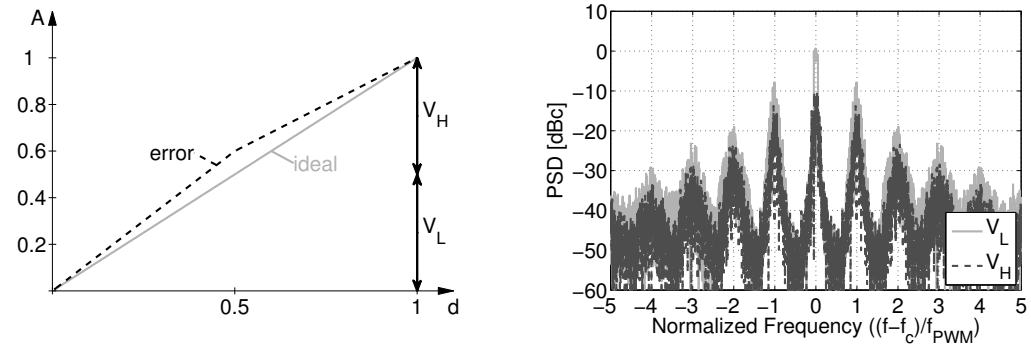
(a) Tx to Rx cross talk

(b) Receive band definition

Figure 4.61: Receive band issue BB PWM.

Another very important property of PAs is their linearity, which directly relates to the ACLR. For the use of multilevel BB PWM it is very important to identify and eventually track the output levels the PA can generate in order to provide a linear response. Fig. 4.62(a) depicts an example, where the intermediate output level has not been properly identified (error), which leads to a difference compared to the ideal curve used for encoding of the low V_L and high level V_H signal.

Fig. 4.62(b) provides the spectra of the low V_L and the high level V_H individually. For proper encoding the sum of both signals will cancel out between the inband signal and the carrier resulting in the ideal spectrum shown in Fig. 4.61(b). But if there is discontinuity in the encoding the two signal components will not cancel out perfectly anymore, leading to reduced signal quality.



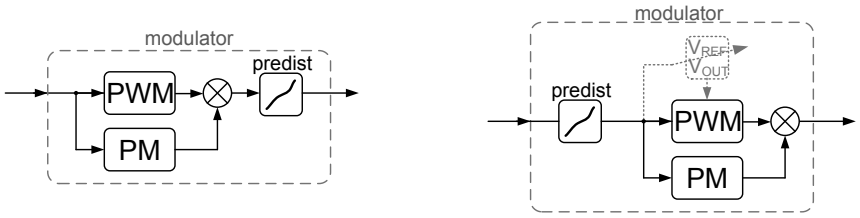
(a) Discontinuity

(b) Multilevel decomposition

Figure 4.62: Multilevel BB PWM decomposition and potential error source.

To avoid this effect and correct the error, the signal has to be predistorted in order to provide the correct signal. This can either be done after the PWM encoding, as depicted in the block diagram in Fig. 4.63(a), or before the PWM encoding. Predistorting the signal after the PWM encoding has the big disadvantage of requiring to correct the wideband PWM signal with all its modulation sidebands. This severely increases the required bandwidth for predistortion compared to the pure band limited PWM encoding. Keeping the high bandwidth of the PWM signal in mind this can hardly be implemented in practice and will therefore not be considered.

The second possibility of correcting the signal is by doing the predistortion before the

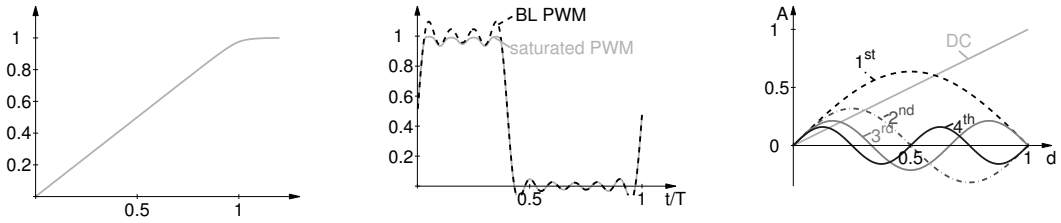


(a) Post modulator (b) Pre modulator

Figure 4.63: Location of the predistorter.

PWM encoding, as depicted in Fig. 4.63(b). Instead of correcting the whole signal, it is sufficient to predistort the inband signal information only, before it is encoded using the PWM. This way the predistortion has to run only at a multiple of the actual signal bandwidth and not the maximum modulation sideband frequency. Beside correcting the signal for the encoder itself, also the output voltages V_{OUT} for the different PWM levels can be modified in order to improve the linearity of the PWM operation of the PA itself. To account for the actual output levels of the PA and to cope with the resulting discontinuities the reference voltages V_{REF} used for the encoding can be corrected instead of leaving the whole correction to the predistorter.

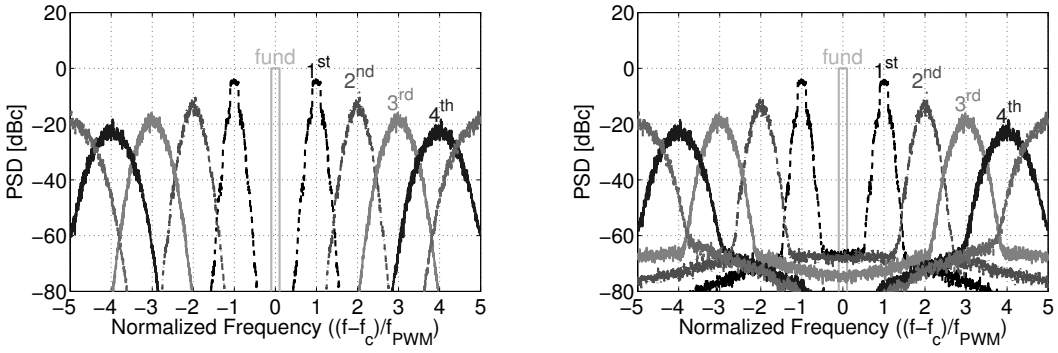
In theory the inband signal linearly depends on the duty cycle, while the harmonics show a sine relationship, as plotted in Fig. 4.64(c). When the ideal BB PWM signal passed through the PA a saturation in terms of amplitude such as in Fig. 4.64(a) occurs. In practice not only the amplitude, but also the phase will be affected. This saturation modifies the applied Band Limited (BL) PWM in a way such that the overshoots of the BL PWM will be severely compressed. In Fig. 4.64(b) a time domain waveform of an ideal BL PWM with 40 % duty cycle signal, as well as the saturated PWM signal are provided.



(a) Saturation (b) 40 % duty cylce (c) Frequency content

Figure 4.64: Ideal BL and saturated PWM signal for a duty cycle of 40 %.

A disadvantage of predistorting the inband signal only is, that the amplitude relation between the inband (DC) content and the higher order harmonics eventually differs from the theoretical behavior. This could lead to spectral expansion of the modulation sidebands after predistortion of the inband signal. In Fig. 4.65(a) the spectrum of an ideal BB PWM signal decomposed into its signal components is plotted. When considering that the higher order harmonics are distorted, as for the saturated PWM signal in Fig. 4.64(b), the contribution of the higher order harmonics eventually expands into inband signal. This could limit the achievable inband signal quality, even when perfect predistortion is possible. As a consequence the bandwidth of the inband signal compared to the PWM frequency has to be reduced in order to provide sufficient spacing for the first harmonic contribution to decay.



(a) Ideal

(b) Saturated

Figure 4.65: BB PWM harmonic decomposition.

It can be concluded that predistortion of the BB PWM signal can either be done after or before the modulator. Predistorting the signal after the PWM encoder results in very large bandwidths and hence tightens the requirement. By predistorting the signal before the PWM encoder the required bandwidth after the PWM encoding remains unaffected. The only requirement is that sufficient spacing between the inband signal and the first PWM harmonic has to be assured. Beside the nonlinearity also the spectral mask and the receive band requirements have to be considered. To fulfill ACLR requirements and to provide low output power next to the band in order not to interfere with adjacent channels, a BPF with sufficient attenuation has to be employed. To ensure proper operation of the receiver digital or analog cancellation of the cross talk can be used.

4.5 Summary BB PWM

In this chapter the properties and prospects of BB PWM have been discussed in detail. Based on the theoretical considerations presented in chapter 3 the requirements for the circuit implementations for direct filter connection have been derived. The influence of the coupling on the input impedance of cavity filters has been studied in detail, as it is the starting point for the matching network design. Based on this, possible matching network architectures have been evaluated. In order to provide high impedance for the modulation sidebands over a wide bandwidth the connection between the filter and the transistor has to be as short as possible. Depending on the orientation of the resonance locus, which is influenced by the coupling, a certain length of transmission line is required to shift the resonance locus towards the open to emulate the behavior of an ideal series resonator. This delay on the one hand reduces the bandwidth with high impedance around the carrier, but on the other hand allows for impedance matching.

Other important aspects are the load modulation trajectories of direct filter connection, for which generalized equations have been derived. Equivalent load impedances for the two different states of the PWM signal have been defined and based on them a design methodology considering the load pull contours and the load modulation trajectories has been developed. During the design a special emphasis was put not only on the carrier impedance matching, but also on the orientation of the resonance locus, as this significantly influences the load modulation trajectories.

The required signal generation chain for optimum operation has been discussed. The difference between digital PWM generation with its aliasing problem and the implemented band limited PWM, which avoids this problem, have been highlighted. A signal condi-

tioning approach to account for residual fluctuation of the filter current in real circuits in order to drive the transistor the optimum way also within the PWM periods has been presented. Two different approaches of correcting the nonlinear behavior of real circuit implementations have been suggested and their difference has been highlighted. In addition a possible solution to avoid the jamming of the own receive band has been discussed.

By analyzing the performance of a switched Doherty PA under BB PWM excitation with isolated load, the possible efficiency improvement by direct filter connection has been highlighted. Based on the derived requirements for direct filter connection four different integrated circuits capable of dealing efficiently with the constant filter current have been developed. Two of the circuits are based on a parallel approach on common source and common drain basis. Both circuits show the highly efficient operation of direct filter connection in the high power region. Due to the required multiplexing between the two transistors the efficiency performance falls slightly behind the theoretical limit. The other two circuits designed are based on series approaches. One of them is the switchable cascode, which makes use of the second voltage level inherently available in cascode structures by adding a switch. This way a discrete supply modulation is possible, leading to a sawtooth like efficiency curve. By combining the switched cascode with BB PWM and direct filter connection highly efficient operation can be achieved. Another promising circuit is the source modulated PA. Its basic concept is to provide (discrete) supply modulation at the source of the PA instead of the drain. This way the RF and BB envelope generation can be separated simplifying the matching network design. The efficiency traces of the source modulated PA for direct filter connection are close to the theoretical limit, as the RF signal is applied to a single transistor, mitigating the demand for switching. The source potential is modulated according to the PWM signal by a purely digital control signal. In addition to the multi level PWM circuits the performance of a biphase direct filter connection concept requiring a single discrete transistor has been evaluated. By using a constant envelope signal and modulating the phase between 0° and 180° it is possible to generate power in one period and recover energy in the other period. Based on a class E circuit design it has been shown that efficiency enhancement in back off by using a single transistor only is possible. One of the drawbacks of this circuit is that the PA and rectifier efficiency have to be very high in order to achieve significant efficiency enhancement in back off. Another disadvantage of the concept is the poor spectral quality as a result of the large spectral expansion of the first modulation sideband. This requires sufficient spacing and a high ratio of the PWM modulation frequency to the signal bandwidth. As a result, good signal quality can only be achieved for very narrowband signals.

For the multilevel PWM circuits this requirement is relaxed, but still sufficient spacing in order to allow for predistortion and to account for filter requirements is necessary. Considering the design limitation for the matching network, which impose a limit for the maximum modulation frequency, the achievable signal bandwidths are limited by the operational principle. Although excellent efficiencies can be achieved, BB PWM can only accommodate for ever rising signal bandwidth up to the limit defined by the operational principle and practical implementation.

5. RF PWM

In this chapter the properties of RF PWM operation with respect to PA efficiency, spectral emissions, modulator implementation and requirements as well as signal processing aspects will be discussed.

Compared to BB PWM the use of RF PWM has significant advantages in terms of spectral emissions close to the carrier. For BB PWM the modulation sidebands of the PWM signal are close to the carrier, as depicted in Fig. 5.1. In order not to interfere with adjacent channels high quality filters are required to remove the modulation sidebands. The first modulation harmonic for RF PWM are simply the second carrier harmonic, thus providing a large spacing to the signal. This drastically simplifies the filtering task compared to BB PWM.

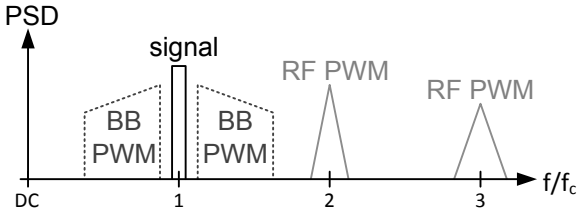
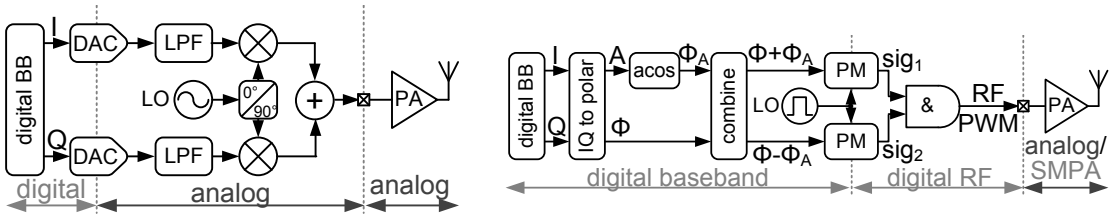


Figure 5.1: Comparison of BB PWM and RF PWM spectrum.

Beside the spectral emission the ever increasing bandwidth is a very important aspect. Hence a higher level of flexibility and reconfigurability of the transmitters, respectively modulators, is required. Thus the trend goes towards digital solutions moving the digital domain closer towards the antenna. Digital circuits can additionally support multi band and multi standard operation leading towards Software Defined Radio (SDR). Another aspect is the low power consumption of digital modulators and their benefit from technology scaling. While for BB PWM a conventional analog IQ modulator is required to avoid the aliasing problem, the RF PWM signal is purely digital up to the PA.

In Fig. 5.2(a) the block diagram of a conventional analog IQ modulator is given. The BB IQ signal undergoes a DAC and is low pass filtered to remove aliasing components. The analog I and Q components are then upconverted using a quadrature mixer and the analog signal is fed to the PA. A drawback of this method is the rather large power consumption of the DACs and the mixer. The circuit also suffers from analog imperfections such as (frequency dependent) IQ imbalance, skew mismatch and DC offset, which lead to images and carrier feedthrough if not properly compensated.



(a) Conventional analog IQ transmitter.

(b) Digital RF PWM transmitter.

Figure 5.2: Block diagram of analog/digital transmitter.

Digital circuits on the other hand do not suffer from such problems. An example of such a digital modulator is provided in Fig. 5.2(b), which depicts the block diagram of a digital

RF PWM transmitter [233–237]. Up to the PA the signal is purely digital and also the PA might be operated purely digital as a Switched Mode Power Amplifier (SMPA) [238]. In this case the amplitude information is introduced by the pulse length, respectively duty cycle, of the signal and the phase is represented by the pulse position.

Similar architectures can be found in [204, 239] and [240]. Other purely digital solutions are for example all digital IQ modulation [241, 242] and all digital Phase Locked Loops (PLLs) [243, 244]. These developments have led to the concept of RFDACs [245, 246] with the possible resolution enhancement in combination with RF PWM [247]. Beside those solutions it is also possible to use $\Delta\Sigma$ modulators either for direct signal generation [248] or to enhance the resolution [249–251] or efficiency [252].

The focus of this chapter is on RF PWM due to its single bit output signal eliminating the demand for any DAC, while high timing resolution in combination with low power consumption [233–237] can be achieved. In the first section the properties of different PA classes under RF PWM operation in terms of efficiency and nonlinear behavior will be discussed. In the subsequent section two different modulator architectures will be compared and their operational principle will be discussed. Additionally the combination with $\Delta\Sigma$ noise shaping for resolution enhancement will be covered.

Due to the discrete time nature of the digital RF PWM generation the achievable spectral quality, especially for broadband signals, is limited by aliasing effects. The effect is described in section 5.2.2 and a method to mitigate this effect is introduced in section 5.2.3.

The properties of driver circuits are covered in section 5.2.4 and lead in general to nonlinear behavior and reduced signal quality. In order to compensate the driver's influence predistortion of the pulses is required. Therefore, a special predistortion scheme dedicated to RF PWM capable of recovering best performance is proposed in section 5.2.5. Finally digital mismatch compensation and its combination with $\Delta\Sigma$ noise shaping is discussed.

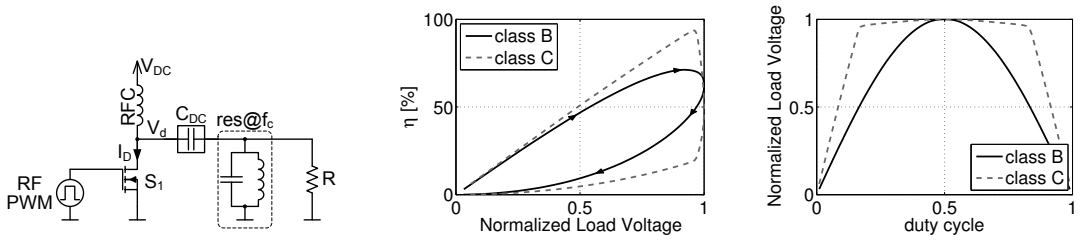
5.1 RF PWM PA Characteristics

Very important aspects are the properties of the PA under RF PWM excitation, which lead to SMPA operation. SMPAs are known for their high efficiency due to the purely switching operation. Therefore, the performance of different PA classes under RF PWM excitation will be discussed in this section. The efficiency behavior, as well as the control characteristic of the circuits is analyzed. The analysis is based on ideal transistor models in order to investigate the influence of the RF PWM operation without experiencing any other efficiency degradation. Nevertheless the limits in terms of maximum voltage and current of real transistors are considered in the discussion.

5.1.1 Class B

In this section the influence of RF PWM operation on linear PAs is presented. The basic circuit of a class B PA for RF PWM operation is depicted in Fig. 5.3(a). Instead of feeding a sine signal to the transistor's gate the RF PWM signal is directly applied, switching the transistor either ON or OFF. The higher order harmonics are short circuited for class B operation and thus the load voltage depends on the fundamental drain current of the RF PWM signal only. To achieve class B operation the load resistor is designed to achieve the maximum voltage swing for a duty cycle of 50 %. The resulting control characteristic for this case follows the theoretical sine curve of the fundamental contribution of the RF PWM signal, as provided in Fig. 5.3(c). A drawback of RF PWM compared to conventional class B operation is the slightly increased overlap of voltage and current in the 50 % duty cycle region. This can be seen in Fig. 5.4(b), which depicts the drain current and voltage

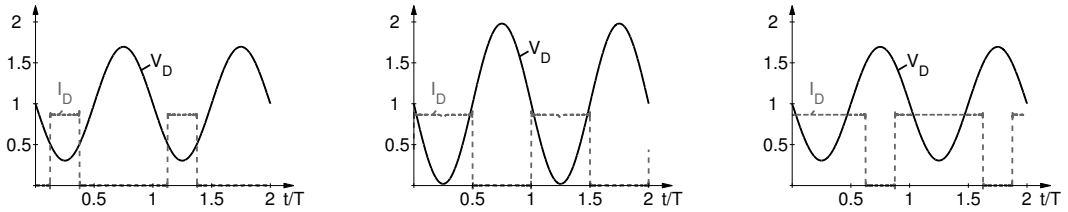
for 50 % duty cycle. As a result the efficiency at maximum output power is lower than the conventional class B performance, as shown in Fig. 5.3(b).



(a) Schematic (b) Efficiency (c) Output voltage

Figure 5.3: RF PWM operation class B and class C.

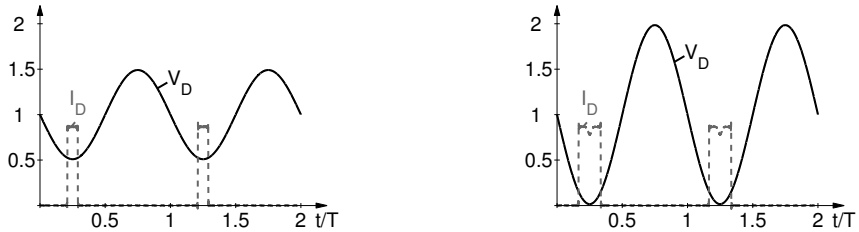
For very low duty cycles the efficiency is similar to the class B performance. Although the drain current amplitude is at its maximum, as given in Fig. 5.4(a), the reduced conduction angle limits the efficiency degradation. In Fig. 5.3(b) it can be seen that the efficiency for the class B design follows a linear trend, while it starts to saturate towards higher output powers. For duty cycles above 50 % the efficiency rapidly drops due to the increased conduction period in combination with the reduced output power. This is caused by the large overlap of voltage and current as depicted in Fig. 5.4(c).



(a) 25 % duty cycle (b) 50 % duty cycle (c) 75 % duty cycle

Figure 5.4: Time domain waveforms RF PWM operation class B.

When increasing the load resistance class C operation can be accomplished. For twice the load resistance of class B operation the output voltage starts to saturate already at a duty cycle of around 17 %. The fundamental current contribution already results in maximum drain voltage swing, as can be seen in Fig. 5.5(b). Due to the reduced conduction angle for maximum output power the efficiency of the class C PA under RF PWM operation is increased compared to the class B behavior, as depicted in Fig. 5.3(b).



(a) 8 % duty cycle (b) 17 % duty cycle

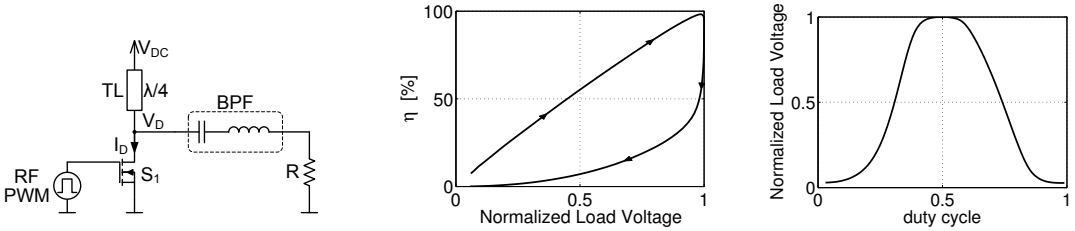
Figure 5.5: Time domain waveforms RF PWM operation class C.

Nevertheless no significant efficiency enhancement in back off is possible by the RF PWM

operation, as the PA is not operated in a purely switched way. This is caused by the fact the the demodulated drain voltage leads to an overlap of current and voltage and thus to a reduced efficiency for lower output powers. The class J PA essentially shows the same trend and is therefore not discussed.

5.1.2 Class F

Compared to the class B PA the class F PA is operated in a true switched mode and achieves ideally 100 % efficiency for maximum output power, as can be seen in Fig. 5.6(b). The basic circuit of the class F amplifier for RF PWM operation is depicted in Fig. 5.6(a). Instead of driving the gate in the conventional way using a sinusoidal drive and class B biasing conditions it is controlled directly by the RF PWM signal. For maximum output

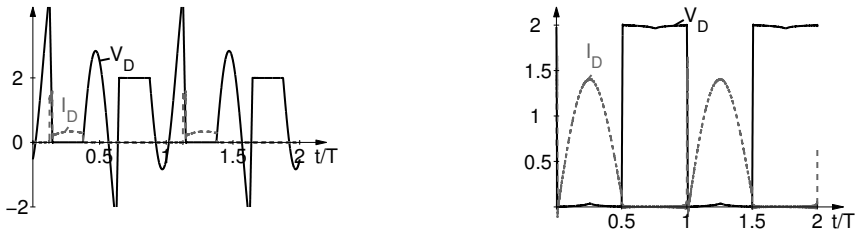


(a) Schematic (b) Efficiency (c) Output voltage

Figure 5.6: RF PWM operation class F.

power with 50 % duty cycle the drain current and voltage correspond to the regular class F operation due to its saturated operation. This can be seen in Fig. 5.7(b), which depicts the half sinusoidal drain current and the rectangular drain voltage waveform. As there is no overlap of drain current and voltage the transistor is operated highly efficient.

Reducing the duty cycle of the signal results in a residual voltage at the beginning of the ON period, preventing Zero Voltage Switching (ZVS), and resulting in capacitive losses. Only for a duty cycle of 50 % the continous current of the series resonator is fully provided by the quarter wave line. A deviation from the 50 % case causes a residual current charging the parasitic capacitance C_{DS} of the transistor resulting in capacitive losses. The drain voltage can reach very large values and can even become negative, as for the 25 % duty cylce example in Fig. 5.7(a).



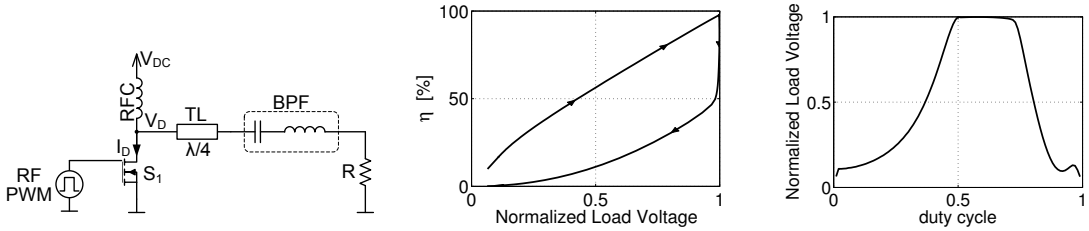
(a) 25 % duty cycle (b) 50 % duty cycle

Figure 5.7: Time domain waveforms RF PWM operation class F.

The capacitive losses lead to an almost linear dependence of the efficiency on the load voltage, as provided in Fig. 5.6(b). The value of the parasitic capacitance has only a minor impact on the overall efficiency trend, although it determines the maximum voltage excursions. But at the same time it influences also the highly nonlinear output voltage

characteristic in Fig. 5.6(c) such that the efficiency with respect to output voltage varies insignificantly. Therefore, only the traces for a single capacitance value are plotted. Similar to the class B PA the efficiency rapidly decreases above 50 % duty cylce due to the reduced output power, while the conduction angle and thus DC power consumption increases.

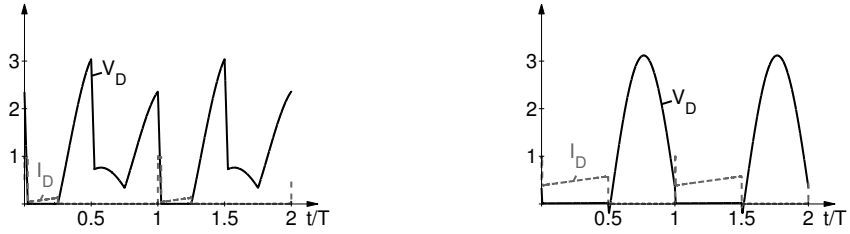
Beside the standard also the inverse class F PA exists. Its schematic is depicted in Fig. 5.8(a). Regular operation with 50 % duty cylce results in a rectangular drain current and a half sinusoidal drain voltage, as plotted in Fig. 5.9(b). As there is ideally no overlap of drain voltage and current a theoretical efficiency of 100 % can be achieved.



(a) Schematic (b) Efficiency (c) Output voltage

Figure 5.8: RF PWM operation inverse class F.

But when deviating from the 50 % duty cyle operation only a part of the constant biasing current of the RFC flows towards the load during the OFF period. Similar to the class F PA this current charges the parasitic capacitance. This effect can be seen in Fig. 5.9(a), which depicts the drain voltage and current for 25 % duty cycle operation. The voltage at the parasitic capacitance during switching ON leads to capacitive losses that reduce the efficiency.



(a) 25 % duty cycle (b) 50 % duty cycle

Figure 5.9: Time domain waveforms RF PWM operation inverse class F.

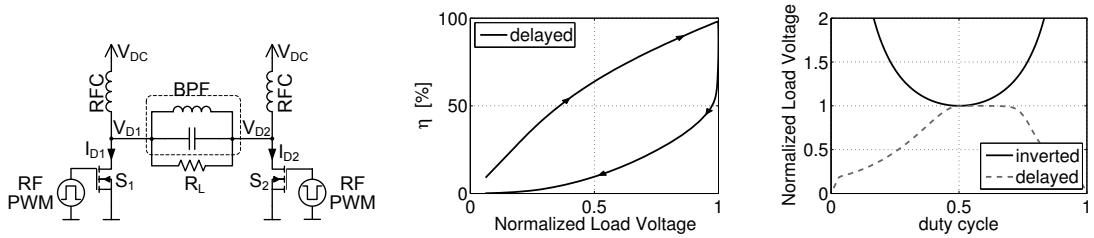
Also for the inverse class F PA the value of the parasitic capacitance mainly influences the maximum voltage, but has only minor impact on the efficiency curve, due to its interdependence with the output voltage control characteristic in Fig. 5.8(c).

It can be summarized that although the class F PA is operated in highly efficient switched mode operation, the capacitive losses degrade the efficiency to a roughly linear behavior, preventing efficiency enhancement in back off.

5.1.3 Class D

The class D PA circuit family is basically an extension of the class F circuits to a push-pull configuration. The schematic of the current mode class D PA can be found in Fig. 5.10(a). It consists of two PA stages, with the load connected between them. For the operation

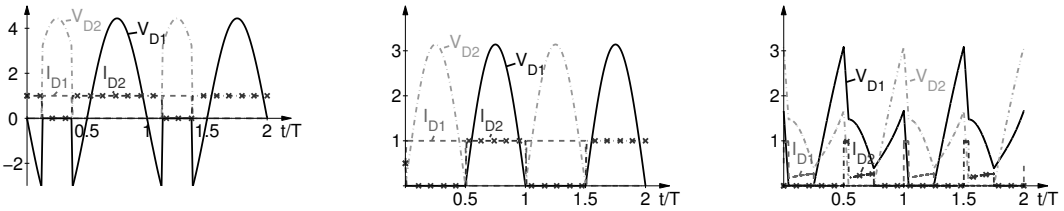
with RF PWM two different operational modes are possible. The second signal can either be the complementary (inverted) signal of the first one or a 180° delayed version of it.



(a) Schematic (b) Efficiency (c) Output voltage

Figure 5.10: RF PWM operation current mode class D.

Both operational modes have different properties, but for 50 % duty cycle the resulting time domain waveforms, as depicted in Fig. 5.11(b), are independent of the signal generation. The drain current and voltage for complementary (inverted) RF PWM control with a duty cycle of 25 % are provided in Fig. 5.11(a). It can be seen that large negative voltages occur at the drain of the first transistor and that the resulting voltage swing is larger than for 50 %. This is caused by the boundary conditions, as shown in Appendix 7.2.1, and leads to an inverse control characteristic of the output voltage as depicted in Fig. 5.10(c). In theory the circuit is 100 % efficient, when neglecting capacitive losses. But due to the inverted control characteristic, the large negative voltages and the increased current for low duty cycles, the practical applicability of this operational mode is limited.



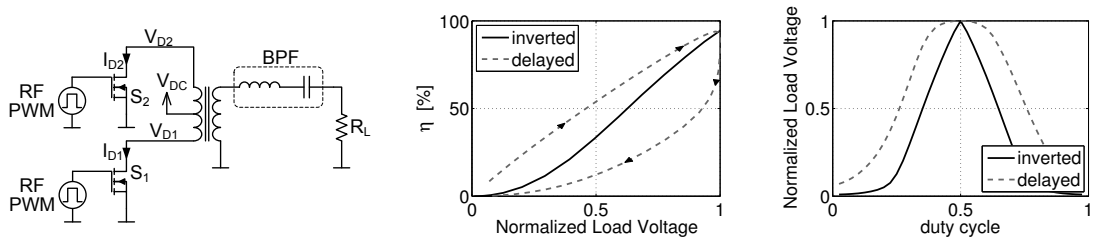
(a) 25 % duty cycle inverted control (b) 50 % duty cycle (c) 25 % duty cycle delayed control

Figure 5.11: Time domain waveforms RF PWM operation current mode class D.

The second operational mode is based on a 180° delayed control signal for the second transistor and is equal to the RF PWM operation of the inverse class F PA. This can be seen well in Fig. 5.11(c), which depicts the time domain waveforms for a duty cycle of 25 % and the delayed control scheme. As for the inverse class F, capacitive losses occur, which lead to a reduced efficiency as depicted in Fig. 5.10(b). Without parasitic capacitances the constant current of the biasing would drive into an open circuit, leading to very large voltage peaks, far beyond the limits of the device and furthermore to a very large voltage during the beginning of the transistor's conduction period. Similar to the inverse class F the efficiency curve of the current mode class D PA with delayed control depends only weakly on the parasitic capacitance.

The voltage mode class D PA, as depicted in Fig. 5.12(a) is the push-pull counterpart of the class F PA.

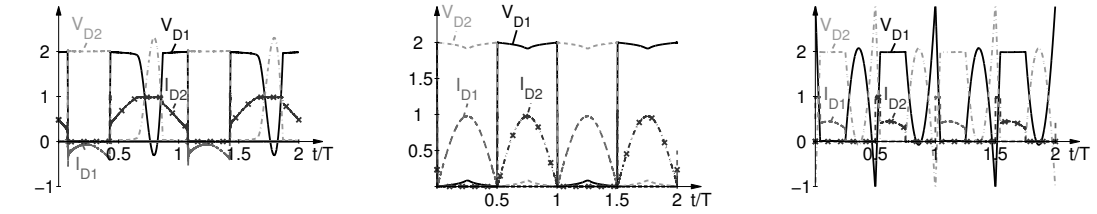
As for the current mode class D PA, two operational modes are possible, which are equal for 50 % duty cycle. The drain current and voltage time domain waveforms for 50 % duty cycle operation are provided in Fig. 5.13(b). It can be seen that the waveforms of a single



(a) Schematic (b) Efficiency (c) Output voltage

Figure 5.12: RF PWM operation voltage mode class D.

transistor correspond to the ones of a class F PA. While for the current mode class D it is possible to operate the circuit efficiently with complementary signal generation, it is shown in Appendix 7.2.2 that this is not possible for the voltage mode class D. The DC biasing determines the DC content of the drain voltage waveforms and results in a large overlap of voltage and current for duty cycles deviating from 50 %. An example for 25 % duty cycle operation is provided in Fig. 5.13(a). It can be seen that the drain current of transistor 1 is negative and the drain current and voltage of transistor 2 have a very large overlap. This overlap results in a rather poor efficiency of this operational mode (inverted), as can be seen in Fig. 5.12(b). Also the control characteristic of the output voltage, as depicted in Fig. 5.12(c), is highly nonlinear.



(a) 35 % duty cycle inverted control (b) 50 % duty cycle (c) 25 % duty cycle delayed control

Figure 5.13: Time domain waveforms RF PWM operation voltage mode class D.

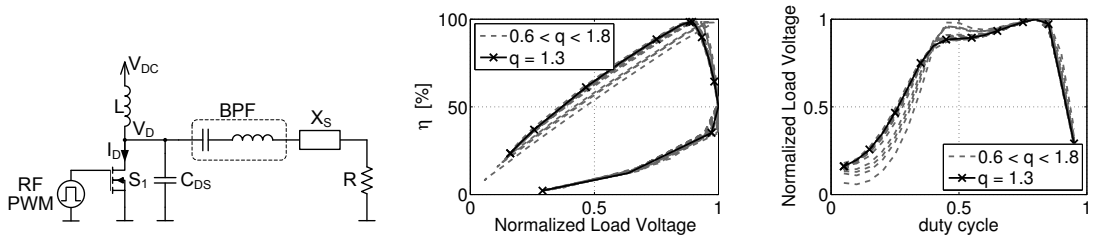
The properties of the operational mode based on a 180° delayed control signal are essentially the same as for the RF PWM control of the class F PA and have already been discussed.

It can be summarized that for the voltage and current mode class D PA no significant efficiency enhancement in back off is possible by RF PWM operation.

5.1.4 Class E

In this section the properties of the class E PA under RF PWM operation will be discussed. The class E PA is a true switched mode PA. Its design offers various degrees of freedom. One of the most important parameters is the q-value, which basically defines the ratio of the resonance frequency of the shunt elements with respect to the operational frequency [80–82]. In addition to that the class E PA can be designed for different duty cycles. Fig. 5.14(a) depicts the schematic of the class E PA for RF PWM operation. For the results presented a range of q-values and a design duty cycle of 50 % is considered. The resulting efficiency curves with respect to maximum load voltage are depicted in Fig. 5.14(b). It can be seen that the efficiency curves show a roughly linear increase until reaching their

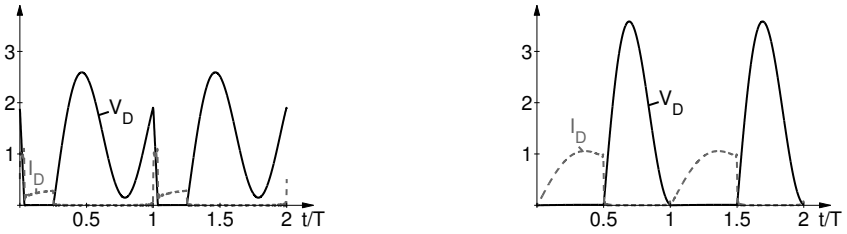
maximum efficiency value, slightly below maximum output power. The corresponding control characteristics of the output voltages provided in Fig. 5.14(c) are highly nonlinear. For duty cycles above the design value of 50 % the output voltage, respectively power, increases only very moderately.



(a) Schematic (b) Efficiency (c) Output voltage

Figure 5.14: Efficiency and control characteristic RF PWM operation of class E designed for 50 % duty cycle.

The time domain waveforms for a class E with a q-value of 1.3, which is designed for and operated at 50 % duty cycle, are provided in Fig. 5.15(b). It can be seen that there is no overlap of voltage and current at any time, enabling highly efficient operation.



(a) 25 % duty cycle (b) 50 % duty cycle

Figure 5.15: Time domain waveforms RF PWM operation class E (q=1.3).

When reducing the duty cycle, deviating from the design duty cycle, the ZVS condition cannot be held anymore and capacitive losses lead to efficiency degradation. This can be seen well when observing the time domain waveforms for 25 % duty cycle operation depicted in Fig. 5.15(a). The residual voltage during switching ON causes capacitive losses that limit the efficiency. The required shunt capacitor value for class E operation is defined by the design equations. Its dependence on the supply voltage and operational frequency makes the efficiency degradation independent of the two parameters. This means that no performance improvement for different supply voltages or operational frequencies is possible.

Another important aspect of class E PAs is their high peak voltage compared to the DC supply voltage. In Fig. 5.16 the maximum drain voltage for different q-values with respect to duty cycle are plotted. For duty cycles above 50 % the maximum drain voltage quickly starts to increase, reaching very high peak values. At the same time the output voltage, respectively output power, increases only slightly in this region.

Considering the large increase of maximum drain voltage for a small benefit only in output power it is not very useful to operate the circuit above the design duty cycle. In Fig. 5.17 the efficiency and control characteristics for operation limited to 50 % duty cycle are depicted.

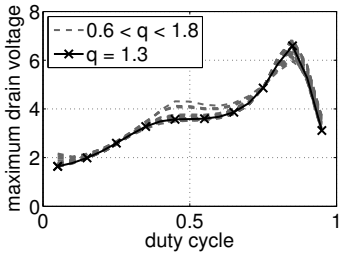
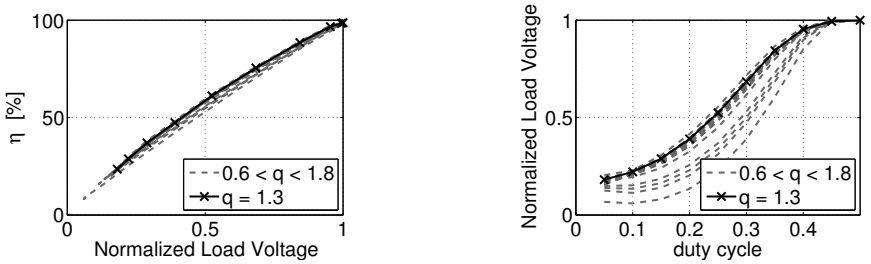


Figure 5.16: Normalized maximum drain voltage RF PWM operation class E designed for 50 % duty cycle and operation until 100 % duty cycle.



(a) Efficiency (b) Output voltage

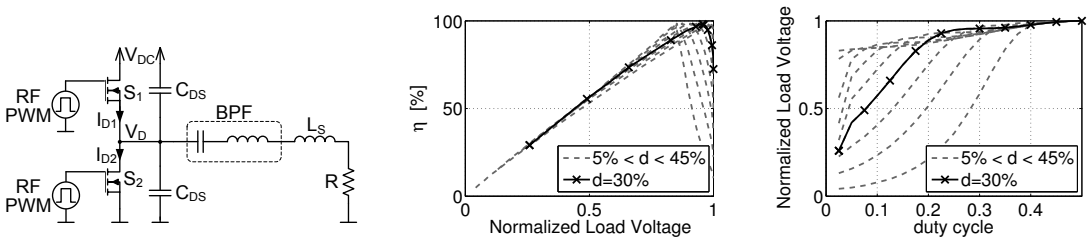
Figure 5.17: Efficiency and control characteristic RF PWM operation class E designed for 50 % duty cycle and operation limited to 50 % duty cycle.

It can be seen that the efficiency curves in Fig. 5.17(a) show an almost linear trend and no significant efficiency enhancement is possible. This means that by simply modifying the duty cycle no efficiency enhancement can be accomplished. The analysis of class E PAs designed for different duty cycles basically delivered the same trends and is therefore not discussed further.

5.1.5 Class DE

In this section the properties of the class DE amplifier depicted in Fig. 5.18(a) with respect to RF PWM will be presented. The operational principle of the class DE amplifier was already covered in section 2.5 and essentially eliminates the capacitive losses of the conventional voltage mode class D by leaving a dead time between the two conduction periods. The load current charges and discharges the parasitic capacitance during this time which results in ZVS and enables highly efficient operation. The class DE amplifier can be designed to operate at different duty cycles, therefore implementations for duty cycles d from 5 % to 45 % in 5 % steps have been considered for this analysis. Fig. 5.18(b) depicts the corresponding efficiency curves with respect to the normalized load voltage. It can be seen that the efficiency peak for some implementation variants is slightly shifted towards lower output voltages, but in general the efficiency shows a roughly linear dependence on the load voltage.

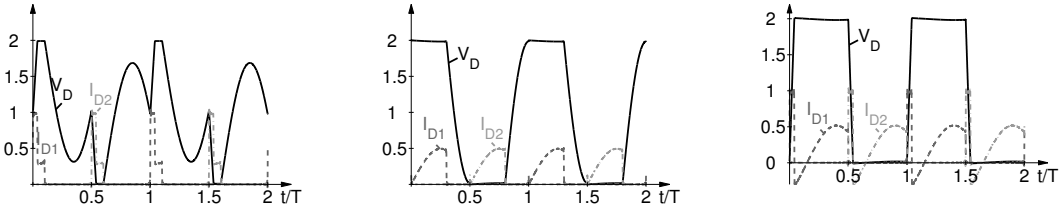
The slight shift of the efficiency peak towards back off dominantly occurs for implementations designed for lower duty cycle operation. These implementations have the drawback that the design duty cycle is already rather low and that controlling the PA with a duty cycle below the design value only results in a minor decrease in output voltage. This can be seen in Fig. 5.18(c), which depicts the relation of the output voltage to the applied duty cycle. Class DE PAs, which are designed to operate at higher duty cycles show a better control characteristic in terms of output voltage coverage.



(a) Schematic (b) Efficiency (c) Output voltage

Figure 5.18: Efficiency and control characteristic RF PWM operation of class DE for designs from 5 % to 45 % duty cycle.

The main contributor to the efficiency degradation are the capacitive losses, when deviating from the design duty cycle. In Fig. 5.19(b) the time domain waveforms of a class DE PA designed and operated at 30 % duty cycle are plotted. Due to the dead time between the two conduction periods ZVS is possible and thus no capacitive losses occur that degrade the efficiency. When controlling the PA with a higher duty cycle, such as 50 % as depicted in Fig. 5.19(c), the dead time between the two conduction periods is not long enough to charge/discharge the parasitic capacitance. This results in capacitive losses, which reduce the efficiency. Another drawback is that the drain current is negative at the beginning of the conduction period. Similar problems occur, when operating the PA with duty cycles below the design value. Fig. 5.19(a) depicts the corresponding waveforms for operation at 10 % duty cycle. Compared to the design value of 30 % the dead time between the two conduction periods is increased, which causes the drain voltage to increase again due to the current of the series resonator. As a result ZVS is not possible and the capacitive losses limit the efficiency.



(a) 10 % duty cycle (b) 30 % duty cycle (c) 50 % duty cycle

Figure 5.19: Time domain waveforms RF PWM operation class DE designed for 30 % duty cycle.

The same trend in terms of efficiency, control characteristic and time domain waveforms has also been observed for the class DE PA with parallel compensation inductance and therefore the results are not shown. Although the class DE PA can be operated highly efficient at the design duty cycle, any deviation from the design value results in capacitive losses, that prevent efficient operation over a wide range. Thus no significant efficiency enhancement in back off by RF PWM operation can be achieved. Supply voltage and operational frequency have, as for the class E PA, no influence on the efficiency behavior, as the required shunt capacitance for class DE operation scales accordingly. As a result the capacitive losses with respect to the output power are independent of supply voltage and frequency.

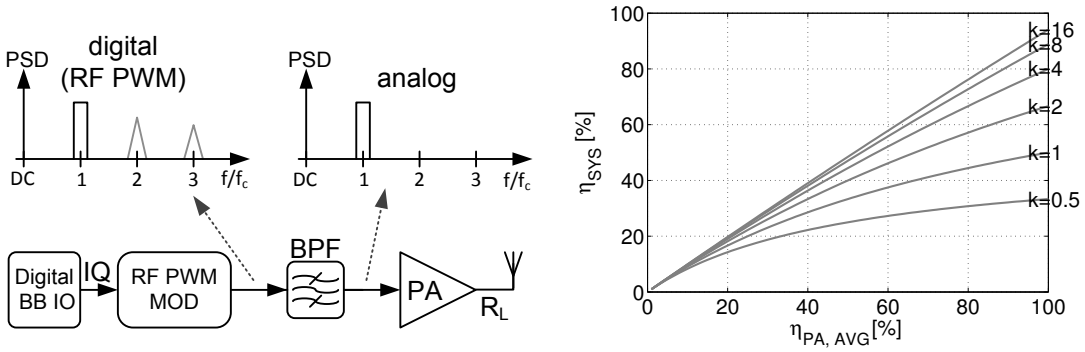
5.1.6 Summary RF PWM PA Characteristics

In this section the properties of different PA classes under RF PWM excitation have been investigated. It has been observed that no significant efficiency enhancement in back off by controlling the PA with RF PWM can be achieved. For linear PAs this is attributed to the fact that the drain voltage is demodulated, which leads to overlap of current and voltage. In the case of SMPAs capacitive losses dominate and cause an almost linear efficiency behavior. Even considering very small parasitics makes no difference, as these result in very large peak voltages which cause the capacitive losses during switching ON to remain roughly constant due to the increased voltage.

It can be summarized that the maximum efficiency can be increased by using SMPAs, but in general no efficiency enhancement in back off compared to the linear (class B) efficiency behavior is possible by simply applying RF PWM control. Only the inverter based voltage mode class D PA, as discussed in section 3.8, is capable of providing good efficiency in back off, if its capacitive losses become negligible. Thus, to enhance the efficiency, the RF PWM control has to be combined with other techniques such as load modulation [169, 170, 238] or multilevel PAs.

5.2 Modulator

This section is dedicated to the properties of the RF PWM modulator itself. Even though no significant improvement of the PA efficiency for single level PAs can be achieved, the use of RF PWM is still appealing due to its digital output signal and the modulator flexibility. As a result of the purely digital output signal the power consumption of the modulator can be reduced. This is an important property for low power transmitters, where the modulator starts having a significant contribution to the total DC power consumption. In Fig. 5.20(b) the impact of the modulator DC power consumption with respect to the average output power and average PA efficiency $\eta_{\mathrm{PA,AVG}}$ is depicted. The traces are parameterized with the parameter $\mathrm{k} = \mathrm{P_{PA,\,AVG}}/\mathrm{P_{MOD}}$, which is the average PA output power with respect to the DC power consumption of the modulator.



(a) Direct digital to RF

(b) Modulator efficiency impact

Figure 5.20: RF PWM for direct digital to RF conversion.

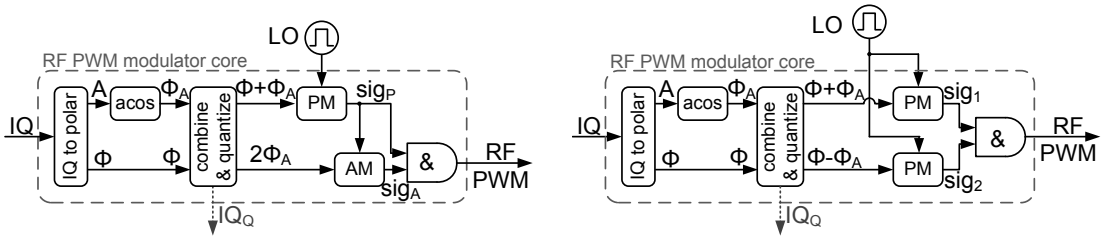
For low average output powers (low k) the PA efficiency becomes less important and the DC power consumption dominates the total system efficiency η_{SYS}. Even for moderate output powers the modulator efficiency has a significant impact on the total system efficiency. In order to benefit from the good modulator efficiency and to introduce an intermediate step towards a fully switched mode transmitter the RF PWM modulator can be used to provide

direct digital to RF conversion. Fig. 5.20(a) depicts such a block diagram. The digital RF PWM signal from the modulator is filtered by the BPF before being fed to the (analog) PA. This operational mode will be considered in this chapter in order to investigate the achievable signal quality. Based on the presented considerations the architecture can be expanded to fully (multilevel) switched mode PAs in a subsequent step.

First the architecture of the modulator and its specific properties will be discussed. Later the aliasing problems of digital discrete time RF PWM will be described and a method based on Cross Point Estimation (CPE) to resolve the problem will be proposed. The properties of digital drivers and their impact on signal quality is covered. In order to compensate the nonlinear effects of the driver a dedicated predistortion scheme will be presented. Finally the digital compensation of device mismatch will be discussed.

5.2.1 Architecture

In this section the architecture and implementation details of the RF PWM modulator will be discussed. The generation of a digital RF PWM signal is usually based on the generation of two outphasing signals with 50 % duty cycle each. The final RF PWM signal is generated by a logical AND operation on the two outphasing signals. Fig. 5.21 depicts the corresponding block diagrams. In general two approaches based on either a series [237,253] or a parallel [240] architecture are possible. For both cases it is necessary to convert the IQ data to polar representation. This can be done by means of a COordinate Rotation DIgital Computer (CORDIC) [254]. The amplitude is then encoded by the inverse cosine to deliver the outphasing angle Φ_A. The inverse cosine function is required in order to account for the sinusoidal relationship between duty cycle and fundamental signal amplitude.



(a) Series architecture

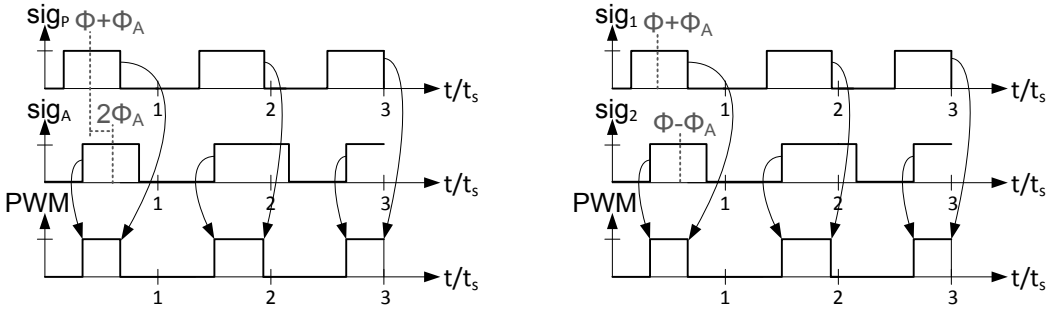
(b) Parallel architecture

Figure 5.21: RF PWM modulator block diagram.

In case of the series architecture in Fig. 5.21(a) the phase information Φ is introduced by the Phase Modulator (PM), with its output signal sig_P. In Fig. 5.22(a) an encoding example for the series architecture is provided. As the phase of the pulse is at its center, the outphasing signal Φ_A has to be considered as well in the control signal generation for the PM. The amplitude information, respectively the PWM signal, is generated by delaying the phase modulated output signal sig_P by twice the outphasing angle $2\Phi_A$. The result is a delayed version sig_A of the phase modulated signal sig_P. The final RF PWM signal is generated by the logical AND operation on sig_P and sig_A.

For the parallel architecture in Fig. 5.21(b) the procedure is similar, with the main difference that two full PMs are used. The outphasing signal for each branch is generated directly in a parallel fashion. In Fig. 5.22(b) an example of the signal generation for the parallel architecture is provided. The two outphasing signals sig_1 and sig_2 are shifted to each other with respect to the outphasing angle Φ_A and the phase Φ is considered by shifting both signals accordingly. The final RF PWM signal is generated by a logical AND

operation on both outphasing signals sig_1 and sig_2.



(a) Series architecture (b) Parallel architecture

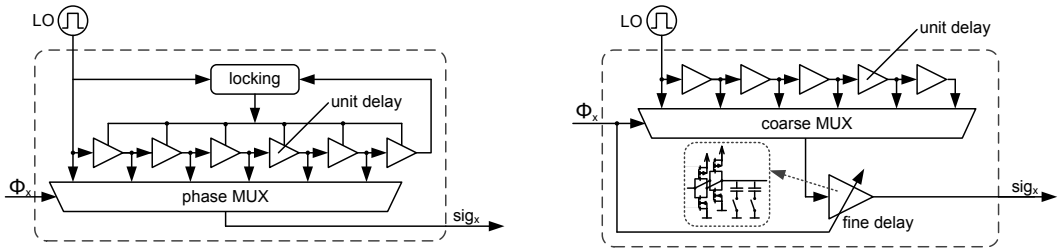
Figure 5.22: RF PWM signal generation.

An advantage of the series approach is that the Amplitude Modulator (AM) has only to cover a 180° shift in order to generate the duty cycle (0-50 %), while the PM has to cover the whole 360°. The AM can be implemented in the same way as the PM, but requires only half of the delay elements. This means that the series architecture results in a smaller implementation with lower power consumption. But the series architecture has some drawbacks compared to the parallel architecture. The fact that the output signal sig_P of the PM travels through the delay elements of the AM, which takes up to 180°, can lead to inconsistent output states during that period, especially for rapidly varying signals.

In Fig. 5.23(a) a possible implementation of the phase modulator is depicted. It consists of a delay line with unit delay elements, which is fed with the rectangular LO signal. As a result the phase shifted copy of the LO signal is present at the output of the unit delay elements. The unit delay can be implemented by an inverter chain with its basic delay including further resolution enhancement by resistive interpolation. The output signal sig_x is selected by a multiplexer, which is controlled by Φ_x. This means that the output signal is a circular shifted version of the LO signal.

In order to compensate temperature drifts of the delay line a locking mechanism, as depicted in Fig. 5.23(a), can be applied [255, 256]. In this aspect the series architecture has another disadvantage in terms of locking of the AM. For the PM the input signal is the constant rectangular LO, which is used as reference for the last output tap of the delay line. But for the AM the input and thus reference signal of the delay line is the phase modulated output signal of the PM, which imposes a challenge for the locking mechanism. The series architecture has also disadvantages in terms of mismatch compensation, as the errors of the PM and AM are not independent, which requires a more sophisticated identification and compensation scheme. For the parallel architecture the impact of the mismatch of both modulators is independent and therefore individual compensation for each modulator branch, as covered in section 5.2.7, is possible. Due to this drawbacks of the series architecture, the parallel architecture will be considered in the further analysis.

Another important property is the achievable resolution of the phase modulator. In case of a digital delay line the resolution is defined by the basic inverter delay. Resolution enhancement by using resistive interpolation is limited to a small factor in practice [237, 257]. To provide even better resolution it is possible to use a cascaded approach as depicted in Fig. 5.23(b). The coarse delay is provided by the delay line and the fine delay done by an adjustable delay element. This can be done by switching the number of inverted cells driving a variable capacitive load [240]. For the separation of coarse and fine delay it

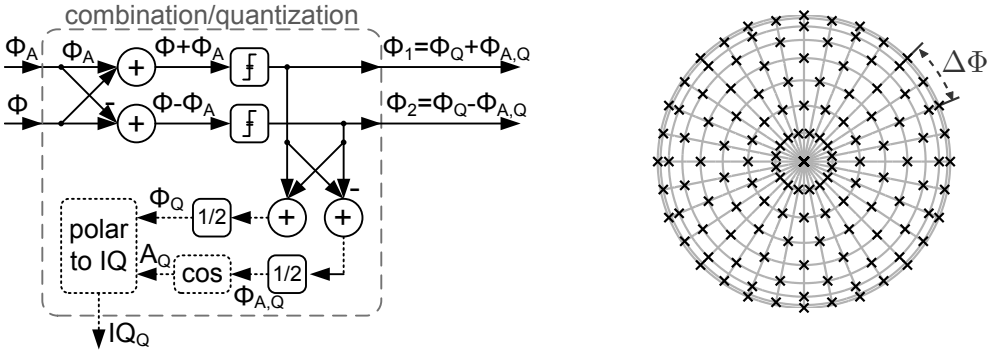


(a) Locking (b) Fine delay

Figure 5.23: Digital phase modulator implementation.

is important to implement only a very short fine delay section in order to minimize the impact of run time effects on the signal quality.

Directly related to the phase resolution of the PMs in Fig. 5.22(b) is the combination/quantization block. A possible implementation is depicted in Fig. 5.24(a). After the decomposition for the single modulator branches the signals Φ_1 and Φ_2 are quantized and fed to the modulator. To provide a feedback signal to enable noise shaping of the quantization error the quantized IQ_Q value is calculated in the reverse manner to the signal decomposition.



(a) Block diagram (b) IQ plane 4 bit

Figure 5.24: Combination and quantization block.

The modulator has an interesting phase relationship, as the phase of the generated IQ signal depends on the pulse length. The phase of a pulse is at exactly half of the pulse length, thus the phase for odd pulse lengths is shifted by half of the phase resolution $\Delta\Phi/2$ compared to even pulse lengths. This can be seen in Fig. 5.24(b), which depicts the possible IQ constellation points for 4 bit resolution. The samples on amplitude circles with odd pulse lengths are shifted in phase by $\Delta\Phi/2$ compared to the IQ samples for even pulse lengths. This effect results in better coverage of the IQ plane. By quantizing the outphasing signals, as shown in Fig. 5.24(a), the sample with the minimum IQ quantization error is selected.

The quantization noise floor is determined by the achievable phase, respectively timing resolution, of the modulator. Fig. 5.26(a) depicts examples for the quantization noise floor of a 40 MHz bandwidth signal generated by an ideal modulator operating at 2.6 GHz with 6 to 9 bit resolution. The desired reference signal as well as the quantization error (generated - reference signal) is plotted. At DC and at twice the carrier frequency the quantization error increases due to the corresponding signal components of the RF PWM. With each bit the quantization noise floor improves by roughly 6 dB. For very low resolution with

6 bit it can be seen that the quantization noise is already partially correlated to the signal, which leads to a small increase of the quantization noise around the inband signal.

In practice the achievable resolution is limited and can possibly be enhanced by using noise shaping. In Fig. 5.25 the block diagram of a RF PWM modulator including $\Delta\Sigma$ noise shaping is depicted [258]. The digital BB signal is upsampled and aliasing effects caused by the Zero Order Hold (ZOH) nature of the modulator are compensated by the CPE block. The detailed function of the CPE block will be presented in section 5.2.3. After the CPE correction the signal is fed to the $\Delta\Sigma$, which works together with the RF PWM modulator block. The quantized signal from the RF PWM modulator is fed back to the $\Delta\Sigma$, which performs the noise shaping to increase the inband signal quality. In order to provide the desired noise shaping, the $\Delta\Sigma$ has to be employed on the IQ data due to their orthogonal nature. Applying the $\Delta\Sigma$ on phase and the amplitude instead of the IQ signal is not possible as due to the nonlinear relation of the RF signal to phase and amplitude the shaped noise folds back into the band.

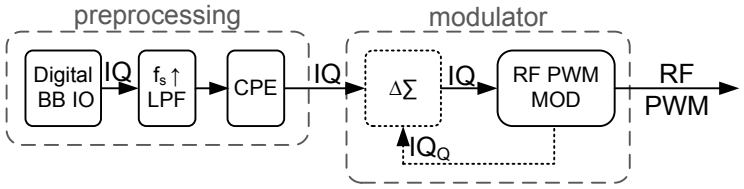
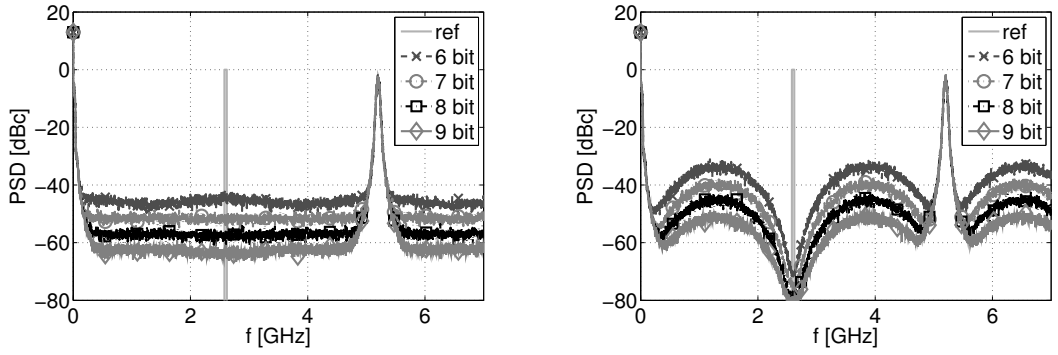


Figure 5.25: Delta Sigma operation for resolution enhancement.

Fig. 5.26(b) depicts the quantization error for 6 to 9 bit resolution while using a second order $\Delta\Sigma$. By employing the noise shaping the inband signal quality around the carrier can be significantly improved and even with low resolution good results can be achieved. The $\Delta\Sigma$ moves the quantization noise to the frequency band between DC and the carrier, respectively between the carrier and the second harmonic. The resolution of the modulator mainly determines the magnitude of the noise floor of the $\Delta\Sigma$ operation.



(a) Normal quantization

(b) 2nd order $\Delta\Sigma$

Figure 5.26: Spectrum of RF PWM signal at 2.6 GHz with 40 MHz bandwidth for limited resolution without and with $\Delta\Sigma$.

5.2.2 Digital RF PWM

The focus of this section is on digital RF PWM and related aliasing problems [259]. Due to the sampled nature of the modulator, aliasing products from higher order harmonics

are generated back into the signal band [259–262]. This aliasing products impose a major limitation for signal quality.

For the analysis presented in this section the parallel modulator architecture of Fig, 5.22(b) will be considered. The IQ input signal is converted into phase Φ and amplitude A. Subsequently the outphasing angle $\Phi_{\mathrm{A}} = \cos^{-1}(A)$ is calculated. The final control signals for the PMs consist of the phase Φ of the signal and the outphasing angle $\pm\Phi_{\mathrm{A}}$. These signals are fed to the PMs, which modulate the 50 % duty cycle LO signal. The actual RF PWM signal is generated by the logical AND combination of the two phase modulated signals. The modulator can only be updated once per carrier period and therefore implicitly performs a ZOH. To understand the effects of the ZOH on the signal quality it is best to start with the base band spectrum resulting from the phase modulation by the outphasing control signal Φ_x, which is given by

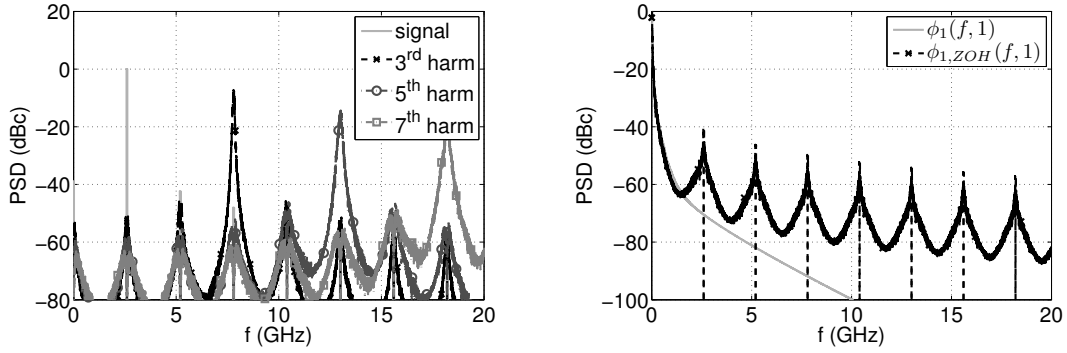
$$\phi_x(f,n) = \mathcal{F}\left\{\mathrm{Re}\left\{\mathrm{e}^{jn\Phi_x(t)}\right\}\right\} \tag{5.1}$$

for the time continuous case. The parameter n denotes a multiplication factor for the higher order harmonics, which is 1 for the fundamental. To account for the sampled nature of the signal the sinc function has to be considered by

$$\phi_{x,ZOH}(f,n) = \mathrm{sinc}\,(f/f_s) \sum_{i=-\infty}^{\infty} \phi_x(f - if_s, n), \tag{5.2}$$

where f_s denotes the sampling frequency, which is the carrier frequency in this case.

The effects of this ZOH on the spectrum of the base band outphasing signal ϕ_1, respectively ϕ_2 are depicted in Fig. 5.27(b). It shows the base band spectra of the phase modulator for the analog case (ϕ_1) and the sampled version ($\phi_{1,ZOH}$) for a carrier frequency of 2.6 GHz. The ZOH operation results in an increase of the PSD at multiples of the signal rate (carrier frequency) due to the sinc function.



(a) Higher order harmonic contribution

(b) Analog and ZOH version of ϕ_x

Figure 5.27: Illustration of aliasing of the higher order harmonics due to ZOH.

The signal for each outphasing branch is generated by modulating the phase of the digital LO signal (50 % duty cycle) with Φ_1 or Φ_2 respectively and may be written as its inverse Fourier Series

$$sig_x\,(t) = \frac{1}{2} + \sum_{n=1}^{\infty} \mathrm{Re}\left\{\frac{2\sin\left(\frac{n\pi}{2}\right)}{n\pi}\mathrm{e}^{jn(\omega t - \frac{\pi}{2})}\mathrm{e}^{jn\Phi_x(t)}\right\}. \tag{5.3}$$

Its frequency domain representation is given by

$$sig_x\,(f) = \frac{1}{2}\phi_{x,ZOH}(f,1) + \sum^{n\neq 0} \frac{2\sin\left(\frac{\pi}{2}\right)}{n\pi}\mathrm{e}^{-j\frac{n\pi}{2}}\phi_{x,ZOH}(f - nf_s, n) \tag{5.4}$$

It can be seen that not only the fundamental of the LO signal but also the higher order harmonics (3^{rd}, 5^{th}, 7^{th}...) exist and are modulated. Due to the ZOH of the modulator and phase signal respectively, the contribution of the higher order harmonics folds back into the signal band lowering the signal quality. This effect is illustrated in Fig. 5.27(a), depicting the spectral contribution of the higher order harmonics for one outphasing signal sig_x and the desired in band signal. The AND operation for the final RF PWM signal generation

$$pwm(t) = sig_1(t) \wedge sig_2(t) \tag{5.5}$$

of the digital signals is equivalent to a mixing process and results in a convolution

$$pwm(f) = sig_1(f) * sig_2(f) \tag{5.6}$$

of the spectra of the two signals sig_1 and sig_2. This convolution results in a contribution of the aliasing products of the higher order harmonics to the inband aliasing effects and increases the aliasing error.

In the time domain the problem manifests itself as an error in the determination of the cross points of the signal. Fig. 5.28 shows an illustration of the error in the time domain. The topmost trace shows the analog (Φ_x) and the sampled version ($\Phi_{x,ZOH}$) of the outphasing control signals. It can be seen that the sampled signal deviates from the desired (analog) signal at the signal transitions as the outphasing signal changes during the sample period. The resulting deviation of the outphasing signals sig_x can be seen in the middle traces of Fig. 5.28. This leads to a difference of the desired (analog) and the generated PWM signal.

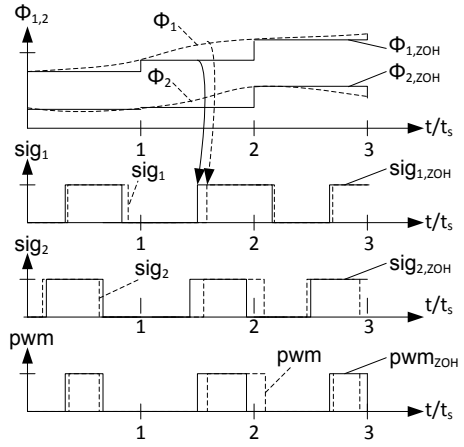


Figure 5.28: ZOH problem in the time domain.

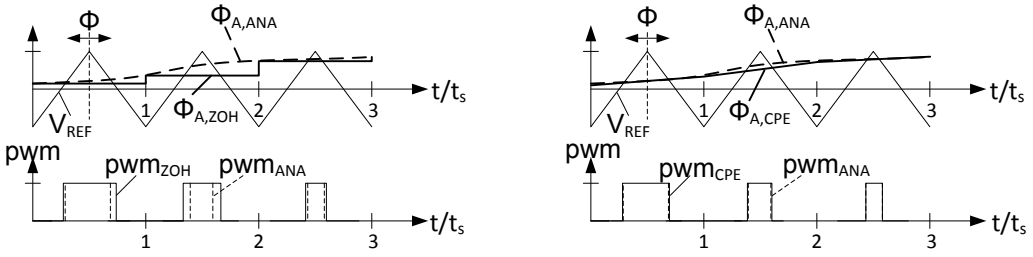
The error caused by this effect is significantly limiting the signal quality of the generated signals, especially for wideband signals or signals with a carrier frequency offset (carrier aggregation).

5.2.3 Cross Point Estimation

In this section the reduction of the signal error by means of cross point estimation will be described. While for conventional CPE [263–265] a linear interpolation and a constant sawtooth reference function are sufficient, the CPE for RF PWM requires a triangular reference function, as depicted in Fig. 5.29. To account for the phase Φ the reference function has to be phase modulated in order to generate the desired modulation signal. The root cause for the error due to the ZOH when using a triangular reference function

V_{REF} is visualized in Fig. 5.29(a). It can be seen that the analog amplitude signal A_{ANA} changes during one symbol and crosses the reference function at different times than the constant ZOH amplitude signal A_{ZOH}. This results in a different signal for the ZOH case and subsequently in reduced signal quality. The same applies for the phase signal Φ, which is modulating the reference function.

The signal quality can be improved by linearly interpolating the amplitude outphasing signal $\Phi_{A,CPE}$ between the samples and using it for the signal generation as depicted in Fig. 5.29(b) [263–265]. The resulting signal is very close to the ideal analog signal and sufficiently accurate to improve the signal quality.



(a) Analog and ZOH

(b) Analog and interpolation

Figure 5.29: CPE using (phase modulated) triangular reference function.

This interpolation can be simplified by performing the cross point estimation for the single branch outphasing signals individually, as depicted in Fig. 5.30, which shows the block diagram of the proposed architecture [S12, S13].

In a first step the signal is separated to get the modulator control signals Φ_1 and Φ_2. The procedure is equal to the control signal generation for the parallel modulator architecture, with the exception that no quantization is involved. Then the signal transitions are detected using CPE, which requires knowledge about the following sample and therefore optional signal prediction. The output of the CPE is the correct normalized edge timing of the outphasing signals. Based on the normalized edge timing the RF PWM signal is calculated. The final signal generation depends on the calculated RF PWM signal and the used mode of operation. The detailed function of each block will be described in the following subsections.

5.2.3.1 Single Branch Cross Point Estimation

For the linear interpolation of the signals, as depicted in Fig. 5.29(b), knowledge of the next sample is required. To get the information about the next sample, signal prediction techniques [266–270] can be used. But when one sample delay can be tolerated ideal signal prediction can be achieved by using the delayed sample for the calculation and considering the current sample as the predicted one. This simplifies the signal prediction block in Fig. 5.30 to a simple one tap delay.

Due to the addition of the outphasing angle Φ_A, Φ_1 determines the falling edges, while Φ_2 is responsible for the rising edges of the RF PWM signal after the AND gate. By using this property the computational effort can be reduced as only information about the rising edges of Φ_1 and the falling edges of Φ_2 is required.

For the calculation of the crossing points the time domain waveform of the modulator signals sig_1 and sig_2 are of importance. Their definition in (5.3) may be rewritten to

$$sig_x(t) = \mathrm{H}\left(\sin\left(\omega t + \Phi_x(t)\right)\right) = \mathrm{sign}\left(\sin\left(\Phi_{Cx}\right)\right), \tag{5.7}$$

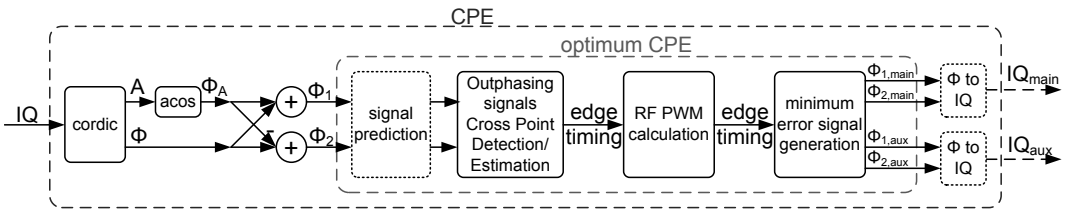


Figure 5.30: CPE block diagram.

with Φ_{Cx} being the argument of the sin function. It is given by

$$\Phi_{\mathrm{Cx}} = \omega t + \Phi_x(t) \tag{5.8}$$

and takes ωt and the interpolated phase modulation signal $\Phi_x(t)$ into account. The function H(x) generates the digital signal and is defined as

$$\mathrm{H}\,(\mathrm{x}) = \begin{cases} 0, & x < 0 \\ 1, & x \geq 0 \end{cases} . \tag{5.9}$$

Considering (5.7) it can be concluded that signal transitions occur when Φ_{Cx} is equal to π and multiples of it. Fig. 5.31 depicts an example for the outphasing signal and the resulting signal calculation. Based on the input signal Φ_{x}, which is plotted for the interpolated $\Phi_{\mathrm{x,CPE}}$ and the ZOH $\Phi_{\mathrm{x,ZOH}}$ case, the argument $\Phi_{\mathrm{Cx}} = \omega \mathrm{t} + \Phi_{\mathrm{x}}$ of the sine is calculated. It can be seen that the negative edge of the resulting signal $\mathrm{sig_x}$ occurs each time the argument Φ_{Cx} crosses π or 3π. While the positive edge occurs when Φ_{Cx} crosses 0 or any cyclic repetition of it (2π, 4π...).

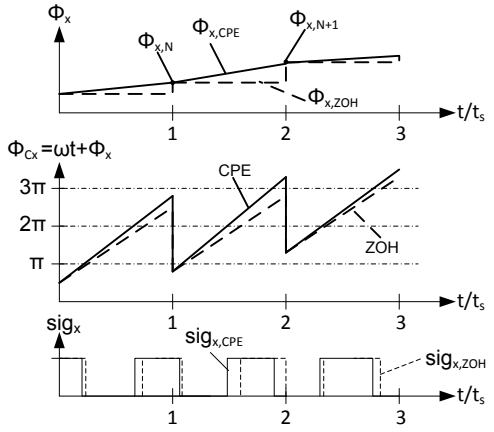


Figure 5.31: CPE calculation for a single branch signal.

The contribution of the carrier ωt is linearly increasing from 0 to 2π within one period. Also the contribution of the interpolated input signal $\Phi_{\mathrm{x,CPE}}$ is linear. Using this property the cross points of the signal can be calculated by interpolation using the state of Φ_{Cx} at the beginning and at the end of the sample, which can be calculated by

$$\Phi_{\mathrm{Cx,N}} = \Phi_{\mathrm{x,N}}, \tag{5.10}$$

$$\Phi_{\mathrm{Cx,N+1}} = 2\pi + \Phi_{\mathrm{x,N+1}}. \tag{5.11}$$

During the calculation of $\Phi_{\mathrm{Cx,N+1}}$ the unwrapped signal of $\Phi_{\mathrm{x,N+1}}$ has to be considered to avoid any error due to the circular nature of the outphasing signals. Based on this

information the cross points (normalized edge timing) of the signals can be calculated using

$$t_{edge} = \frac{\Phi_{REF} - \Phi_{Cx,N}}{\Phi_{Cx,N+1} - \Phi_{Cx,N}}, \tag{5.12}$$

where $\Phi_{Cx,N}$ denotes the current and $\Phi_{Cx,N+1}$ the upcoming (predicted) sample. The edge timing t_{edge} is normalized to one carrier period, such that the calculation is independent of the carrier frequency.

For the calculation of the rising edges the reference vector $\Phi_{REF} = \{0, 2\pi, 4\pi\}$ is used. Only the resulting edge timings that are within the current period [0-1) are of importance and the others are ignored. Using this boundary conditions and the circular nature of the control signal Φ_x [0-2π) the calculation for the reference phase $\Phi_{REF} = 0$ simplifies to a prompting of $\Phi_{Cx,N}$ for zero. To determine the falling edges the reference vector $\Phi_{REF} = \{\pi, 3\pi\}$ is used.

Taking into account that Φ_1 determines the rising and Φ_2 the falling edges mitigates the demand for the calculation of the RF PWM signal, as depicted in Fig. 5.30, as the edge timing calculated by the CPE directly defines the PWM signal. Only for the general case when it is not explicitly known which signal transitions of the outphasing signals sig_x dominate in the signal generation the RF PWM calculation block is required.

It shall be noted that instead of performing the cross point estimation it is possible to perform cross point detection based on the upsampled time domain signals. As this requires a high computational effort and complexity, as the signal has to be oversampled with at least the timing resolution of the phase modulators, this option is not further considered.

For the implementation of the CPE algorithm the required division in (5.12) imposes a challenge and should preferably be avoided. Therefore, the calculation of the edge timings was modified to an iterative approximation approach. The corresponding block diagram is given in Fig. 5.32. In the first step the phase difference $d\Phi_x$ between the current $\Phi_{x,N}$ and the upcoming sample $\Phi_{x,N+1}$ is calculated and normalized to give the edge timing difference dt. The reference phase is considered by subtracting it from the current sample $\Phi_{x,N}$ and the resulting signal is normalized to give the initial estimate for the edge timing t_1. The initial edge timing defines the first normalized error weight e_{t1}. Based on e_{t1} and the total timing difference of the entire sample period dt the error signal e_{tN} is calculated and used to correct the edge timing t_1. The error e_{tN} defines the timing correction of the edge timing and furthermore it is the normalized correction value for the next iteration. In this way the interpolated timing can be calculated to a given accuracy defined by the number of steps required.

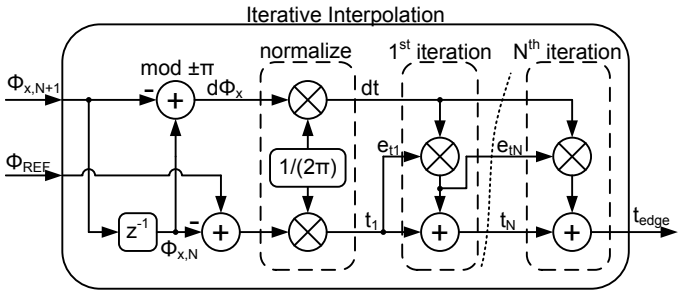


Figure 5.32: CPE iterative interpolation.

By using the iterative interpolation approach the demand for the division involved in the cross point calculation can be mitigated. In Appendix 7.10 detailed block diagrams of a

possible implementation of the CPE are provided.

5.2.3.2 Minimum Error Signal Generation

The last step in the CPE signal calculation is the calculation of the output control signals, respectively the according IQ symbols. Based on the desired RF PWM signal calculated in the previous step the output signals are determined. For modulated signals with rapidly varying phase or signals with a frequency offset (carrier aggregation) up to two RF PWM pulses per carrier period can be required. As the digital RF PWM modulator presented in Fig. 5.21 is only capable of generating one pulse per period special care has to be taken.

To account for this property the signal is separated into a main IQ_{main} and an auxiliary path IQ_{aux}. The separation between main and auxiliary path is based on the decision of the minimum error pulse. If only a single pulse is present it is directed to the main path and the auxiliary path remains zero. In Fig. 5.33 an example of this separation is provided, like during the first two periods where only a single pulse is present.

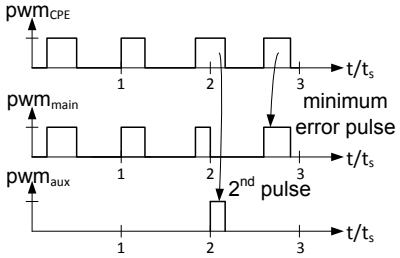


Figure 5.33: Example timing diagram for pulse separation for main and auxiliary path.

In the last period two pulses are present. In such a case the main path holds the pulse which is longer and has hence the smaller error compared to the shorter pulse. The second (missing) pulse is assigned to the auxiliary path. In the following subsections different methods how to handle the auxiliary signal and their impact on signal quality will be discussed.

5.2.3.3 Single and Double Branch Modulator Performance

If no CPE is performed the signal quality is limited by the aliasing effects, as described in section 5.2.2. This can be seen in trace $e_{NO\ CPE}$ in Fig. 5.34, which shows the spectral error signal (generated signal - reference signal) for a carrier frequency of 2.6 GHz and 40 MHz bandwidth when no cross point estimation is performed. The error signal representation is chosen to provide also insight into the inband signal quality. It can be seen that the error reduces the signal quality to slightly above 43 dBc at the signal borders. At the carrier frequency the spectral error gets very small due to the sinc nature of the ZOH.

When using a single modulator (Fig. 5.21) controlled by the main CPE signal (IQ_{main}), as described in section 5.2.3.2, the signal quality (e_{CPE}) can already be improved to ∼65 dBc in the example given in Fig. 5.34. The remaining noise floor is due to the fact that the possible occurrence of a second pulse within one carrier period (IQ_{aux}) is not treated.

To further improve signal quality a second modulator capable of generating the required second pulses might be used. Fig. 5.35 shows the block diagram of such a modulator structure. The IQ output of the CPE depicted in Fig. 5.30 is fed to two RF PWM modulators (Fig. 5.2(b)) and combined by a logical OR. It shall be noted that the second pulse could also be generated by a single modulator, if the control signal is oversampled compared to the carrier frequency.

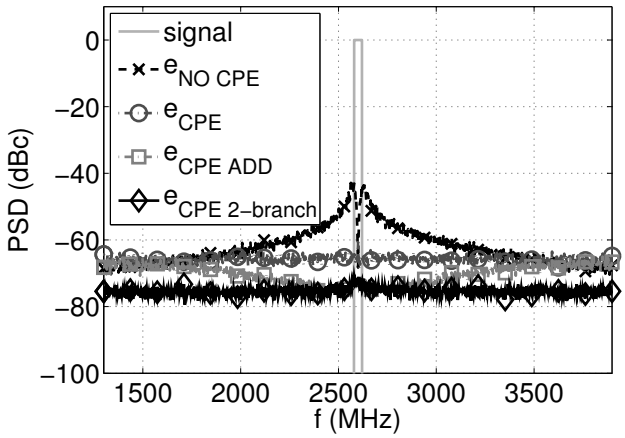


Figure 5.34: Reference and error signal spectra with and without CPE for a carrier frequency of 2.6 GHz, a bandwidth of 40 MHz and a resolution of 11 bit.

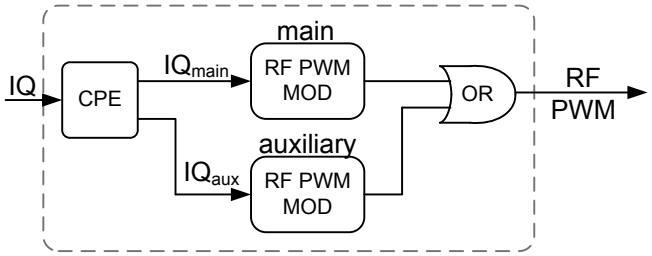


Figure 5.35: Block diagram of main and auxiliary path modulator.

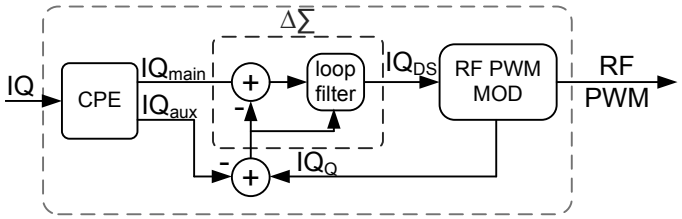
By using this structure it is possible to generate the missing pulses, further decreasing the error signal. This can be seen in trace $e_{\text{CPE 2-branch}}$, which depicts the error signal for the combined main and auxiliary signal. The noise floor with roughly -75 dBc is 10 dB lower than the single modulator option (e_{CPE}). The remaining noise is dominated by the quantization noise caused by the 11 bit resolution of the phase modulator. A drawback of this operation is that the RF PWM modulator components depicted in Fig. 5.21 have to be duplicated, which leads to increased hardware complexity and power consumption.

5.2.3.4 Delta Sigma Cross Point Estimation Noise Shaping

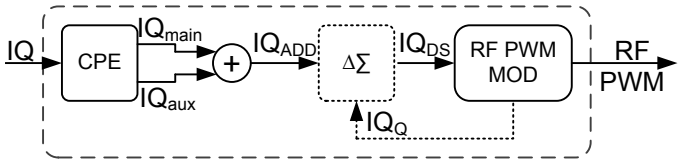
Instead of using a second modulator branch, the remaining error can be spectrally shaped by means of delta sigma noise shaping [248–252]. A delta sigma modulator to shape the quantization noise might already be present in the system to increase the signal quality if limited resolution is available. Fig. 5.36(a) provides a block diagram of such a combined CPE $\Delta\Sigma$ system that allows to also shape the CPE error. The core of the circuit is the delta sigma modulator, which consists of an adder and the loop filter. The input signal of the $\Delta\Sigma$ modulator is the IQ_{main} signal of the CPE. Its output signal IQ_{DS} is fed to the RF PWM modulator, which quantizes and generates the signal. The $\Delta\Sigma$ uses the difference between the desired signal (IQ_{main}) and the quantized signal to shape the quantization error.

In addition to the quantization error a possible error due to the missing second pulse might be present. This error is the signal of the auxiliary path IQ_{aux}, which forms together with the quantized signal IQ_{Q} the error signal for the noise shaping. In order to process the CPE signal, which is calculated at carrier rate, and to provide the highest oversampling

ratio and thus best noise shaping the delta sigma runs also at carrier rate.



(a) ΔΣ with auxiliary signal as error feedback



(b) Additive CPE noise shaping with optional ΔΣ

Figure 5.36: Block diagram for PWM modulator with CPE error noise shaping.

As the error due to the missing pulse is a priori known, no delay is required and it can be directly considered in the feedback path. This makes it possible to move the addition for the feedback signal, as given in Fig. 5.36(a), outside of the ΔΣ loop, as depicted in Fig. 5.36(b). By doing so the ΔΣ is only required to shape the quantization noise and therefore the ΔΣ itself is optional in the CPE context. The spectral shaping of the error due to the second pulse results in a simple implementation, as only an addition of the two signal paths (main and aux) is required.

In Fig. 5.37 an example of the additive CPE operation is given. During the first two periods only one pulse occurs, consequently the output $\mathrm{pwm_{ADD}}$ is the same as the desired signal $\mathrm{pwm_{CPE}}$. But in the third period two pulses occur. These two pulses are split into the modulator paths and the corresponding IQ representation is calculated and added ($\mathrm{IQ_{ADD}}$). This can be seen as a calculation of the corresponding IQ vector of the fundamental signal for the given signal period. The result is that the modulator selects the single pulse signal, whose IQ vector shows the smallest quantization error with respect to $\mathrm{IQ_{ADD}}$. Such an example is depicted in the third period in Fig. 5.37.

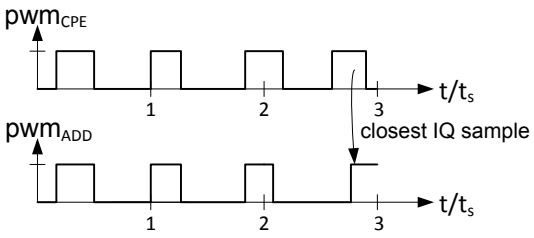


Figure 5.37: Example timing diagram for pulse generation for delta sigma CPE noise shaping.

The resulting spectral improvement can be seen in trace $\mathrm{e_{CPE\ ADD}}$ in Fig. 5.34. The inband signal quality reaches the level of the two branch system and converges towards the single branch noise floor when deviating from the carrier frequency. It can be concluded that by the simple addition of the two branch signals it is possible to shape the error and to mitigate the demand for a second modulator branch or the ΔΣ. The ΔΣ itself can

be optionally included to shape the quantization noise but is not required for the CPE correction. Thus by using the additive CPE correction best inband performance without additional hardware and power consumption in the modulator can be achieved.

5.2.3.5 Measurement Results

To evaluate the proposed signal generation, measurements using an Arbitrary Waveform Generator (AWG) have been carried out. The digital output of an AWG with a maximum sample frequency of 1.2 GHz was used to generate the digital RF PWM signal. In order to emulate a high resolution of 10 bit with the available measurement equipment a carrier frequency of 1 MHz was selected to provide the required oversampling. A Vector Signal Analyzer (VSA) has been used to measure the signal.

The measured spectra for 20 kHz bandwidth, which corresponds roughly to the 40 MHz at 2.6 GHz carrier frequency, are presented in Fig. 5.38. When performing no CPE the signal quality is limited to roughly 40 dBc. The main signal error can be removed by using the single branch CPE calculation, as depicted in trace CPE in Fig. 5.38. By considering the 2 modulator branches ($\text{CPE}_{\text{2-branch}}$) the signal quality can be further improved by 5 dB. The signal is now dominated by the quantization noise and the clock jitter.

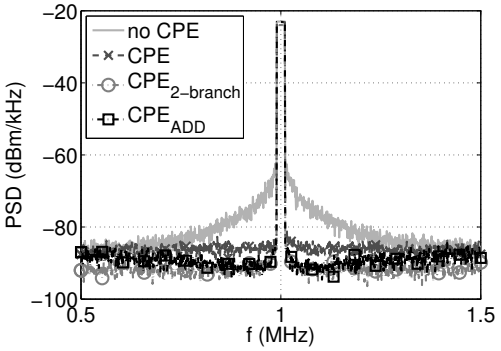


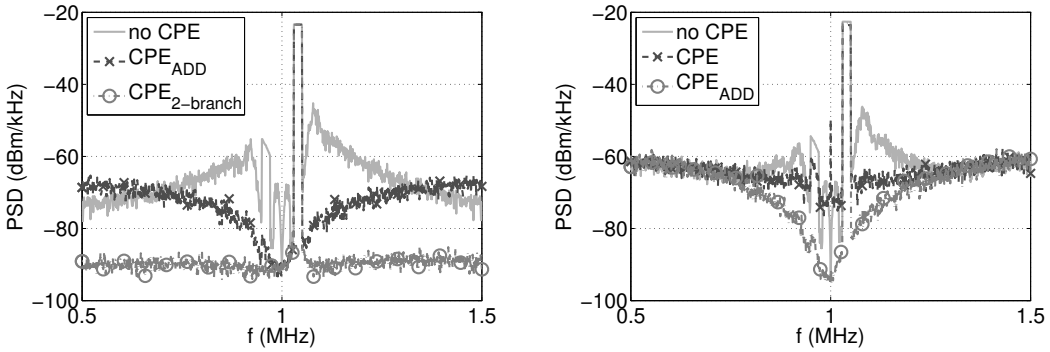
Figure 5.38: Measured signal at 1 MHz carrier frequency, 20 kHz bandwidth and 10 bit resolution.

Additionally the additive noise shaping for the single branch modulator has been measured and is given in trace CPE_{ADD}, which shows that the inband signal quality can be improved.

The effects of the aliasing error are even more pronounced, if the signal has a frequency offset (carrier aggregation). This is due to the fact that the aliasing components do not fall into the zero of the ZOH sinc anymore and significantly impact the signal quality. Trace 'no CPE' in Fig. 5.39(a) shows these effects for a 20 KHz bandwidth with a 40 KHz frequency offset. By using the additive noise shaping (CPE_{ADD}) the signal quality can already be improved. The out of band spectra is dominated by the noise shaping, as a second pulse per carrier period frequently occurs, resulting in a significant error that has to be corrected.

But when considering a second modulator branch to generate the missing pulses ($\text{CPE}_{\text{2-branch}}$ in Fig. 5.39(a)) optimum signal quality can be achieved.

The resulting signal quality for the two branch option with and without frequency offset is the same, showing the capabilities of the CPE and indicating smooth operation. Thus to achieve best signal quality also for signals with frequency offset it is required to use a second modulator branch. When using a single modulator and the additive CPE option to get best signal quality (CPE_{ADD}) the out of band spectra for a frequency offset is significantly increased compared to the quantization noise floor dominated signal ($\text{CPE}_{\text{2-branch}}$).



(a) 10 bit resolution

(b) 7 bit resolution and 2nd order $\Delta\Sigma$

Figure 5.39: Measured signal at 1 MHz carrier frequency, 20 kHz bandwidth and 40 kHz frequency offset (carrier aggregation).

Considering this limitation, it is not required to have a high resolution of 10 bit, as otherwise a similar spectrum can be achieved by noise shaping and a resolution of 7 bit. This is depicted in Fig. 5.39(b), which considers a frequency offset of 40 KHz, 7 bit resolution and a 2nd order delta sigma architecture as given in Fig. 5.36(b).

When comparing trace CPE_{ADD} for the 10 bit resolution in Fig. 5.39(a) and the 7 bit resolution and noise shaping in Fig. 5.39(b) only a minor increase of the out of band spectra can be achieved. The main contributor to the error spectrum is not the shaped quantization error, but the limited signal quality for single pulses as can be seen in trace CPE of Fig. 5.39(b). This means that for this case a resolution of 7 bit in combination with delta sigma is sufficient to achieve almost optimum signal quality. Further enhancements in resolution only marginally improve the out of band spectrum.

5.2.3.6 Summary CPE

Aliasing problems and related signal degradation in digital RF PWM modulators have been described. The root cause has been identified to be related to an error in the calculations of the cross points of the signal. The straight forward approach of calculating the cross points of the amplitude signal with a phase modulated reference function would result in a rather complicated calculation. The proposed method is reduced to two simple linear interpolations based on an outphasing method to generate the desired RF PWM signal. It shall be noted that the compensation is not limited to a specific architecture of the final modulator. To cover also the possible occurrence of two pulses per carrier period several methods have been investigated. With the proposed methods the aliasing problem can be significantly reduced and high signal quality can be ensured.

5.2.4 Driver Properties

In this section the properties of the AND gate and the following driver stages are analyzed. In the case of ideal RF PWM generation infinite rise and fall times are required, which cannot be generated by real world driver circuits. In Fig. 5.40 a high level block diagram of a driver chain is depicted. Each of the driver blocks may be implemented as a complementary inverter circuit loaded with its own parasitic output capacitance and the parasitic input capacitance of the subsequent stages.

The rise and fall times of the circuit are determined by the parasitic capacitances and the maximum current that can be provided by the driver circuit. As a result of the

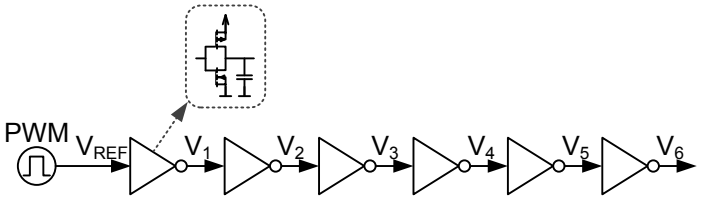
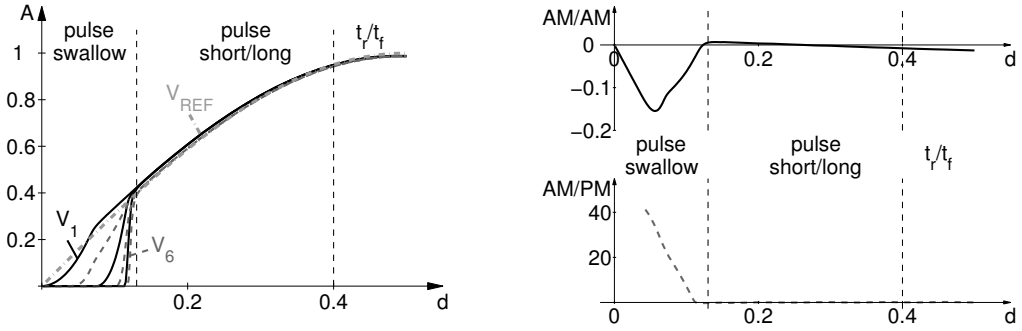


Figure 5.40: Driver block diagram.

finite rise and fall time the real driver response differs from the ideal one. Fig. 5.41(a) depicts the fundamental amplitudes at different stages of the driver chain. The curve can basically be divided into 3 regions. For very low duty cycle signals Pulse Swallowing (PS) can happen, which occurs when the output of one stage is too small to trigger the threshold of the subsequent stage [237]. For the intermediate duty cycle region the effects of pulse shortening/extension caused by different rise and fall times dominates the driver characteristic. The fundamental amplitude for high duty cycles around 50 % for the driver circuit is reduced compared to theory due the impact of limited rise and fall times.



(a) Characteristic

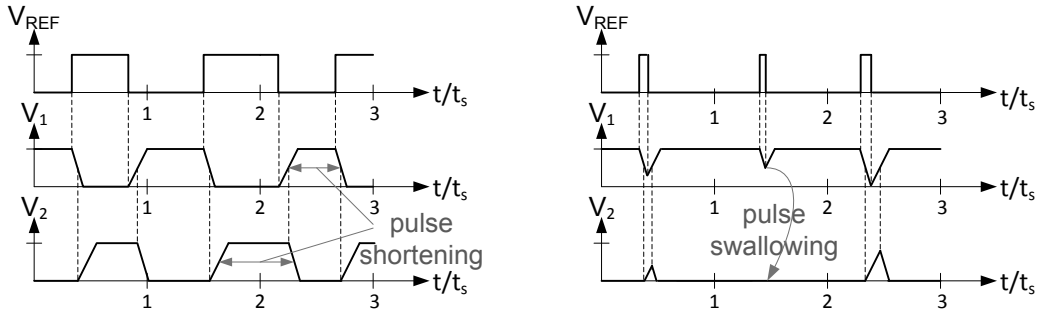
(b) AM/AM and AM/PM

Figure 5.41: Driver errors and AM/AM, AM/PM deviation.

The corresponding AM/AM and AM/PM characteristics for the output V_2 of the second driver stage is plotted in Fig. 5.41(b). It can be seen that for the pulse swallowing region for low duty cycles the highest deviation for the AM/AM characteristic occurs. Also the phase response drifts away in the pulse swallowing region, as can be seen in the AM/PM curve. Above the pulse swallowing region the phase remains unaffected. In the intermediate and high duty cycle region the pulse shortening/extension effect, respectively the finite rise and fall time, dominate the behavior. It shall be noted that for illustrative purposes a worst case scenario is assumed to highlight the impact of the individual effects.

In Fig. 5.42(a) a time domain illustration of the pulse shortening effect is provided. In general the rising edge is slower than the falling edge, as the high side PMOS transistors have lower current density than the low side NMOS transistors. This leads to a reduction of pulse length, as the delay for triggering the next stage is higher for the rising edge than the (faster) falling edge. Ideally this effect is compensated in the next stage, whose input is the inverted signal which experiences effectively a pulse extension. This effect causes the increase of the fundamental voltage in the intermediate duty cycle region for all odd numbered signals in Fig 5.41(a).

Compared to the pulse shortening/extension effect the pulse swallowing effect has a more severe impact. Fig. 5.42(b) provides an illustration in the time domain of this effect. The pulse in the first period is sufficiently long, such that the threshold of the next stage is



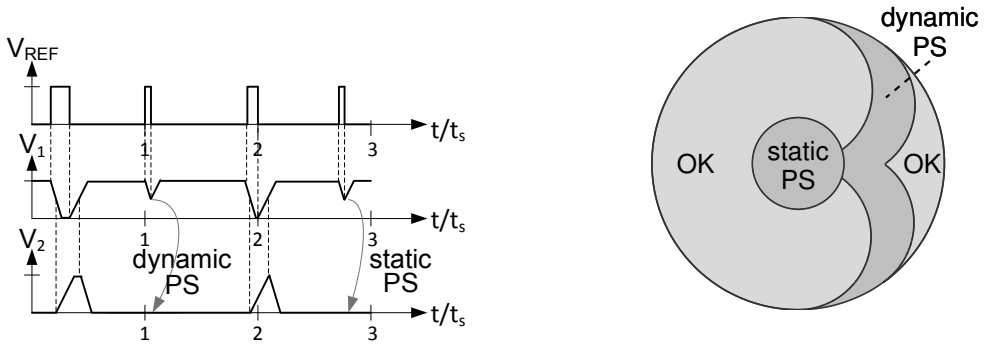
(a) Pulse shortening (b) Pulse swallow

Figure 5.42: Driver effects.

reached. But the effective pulse does not reach a steady state, which results in a reduced output pulse length and height. In the second period the input pulse is very short, such that the output pulse of the first stage is not capable of triggering the next stage. Thus the pulse disappears and is 'swallowed' in the driver chain. The higher the number of elements in the chain, the more pronounced is the effect, leading to a rapid transition as depicted in Fig. 5.41(a).

The PS effect is not limited to the static case but can also appear for dynamic signals with sufficiently long duty cycles. Due to the circular nature of the modulator a pulse can be split into two parts, as in the second period in the example in Fig. 5.43(a). As a result a part of the pulse is too short and swallowed. This is referred to as dynamic PS.

In Fig. 5.43(b) the pulse swallowing regions in the IQ plane of the modulator are depicted. For low duty cycles static PS occurs, independent of the phase. As a result the inner circle of the IQ plane (except zero) cannot be represented.



(a) Time domain (b) IQ plane

Figure 5.43: Static and dynamic pulse swallowing.

The region where dynamic PS can occur is also indicated. It is separated into two main areas, as dynamic PS can either happen at the beginning or the end of the period. For slowly varying signals dynamic PS is no problem as the pulses are extended by the adjacent samples. Thus dynamic PS can only occur for rapidly varying phase signals. In general the CPE will correct this signals accordingly, such that dynamic PS is avoided. But due to the additive error shaping of the CPE dynamic PS cannot be completely excluded.

5.2.5 Predistortion

In this section the required predistortion to compensate for the driver nonlinearity will be presented. The nonlinear effects of the driver lead to significant distortion that imposes a major limitation for the spectral quality [271]. In order to compensate these effects a predistortion scheme specifically targeted to the digital RF PWM modulator has to be applied. In Fig. 5.44 the corresponding block diagram is provided. In the first step the edge timing for the input IQ samples is calculated. This is followed by the signal prediction block, as it is required to know the upcoming sample. As for the CPE implementation this block can consist of a simple one tap delay. In the next step the desired pulses, based on the edge timing of the previous t_{N-1}, current t_N and upcoming sample t_{N+1}, are calculated. The desired pulses are then corrected individually by static predistortion using Look Up Tables (LUTs) for phase and amplitude correction. Based on the predistorted pulses, which fall into the current sample, the control signal is generated. Up to two pulses per sample can occur, which are separately converted into the IQ domain. Finally the IQ values are added to give the final predistortion signal.

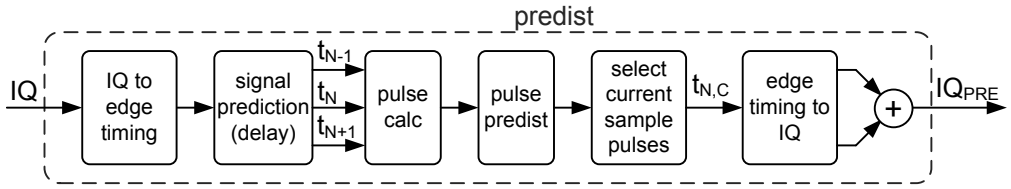
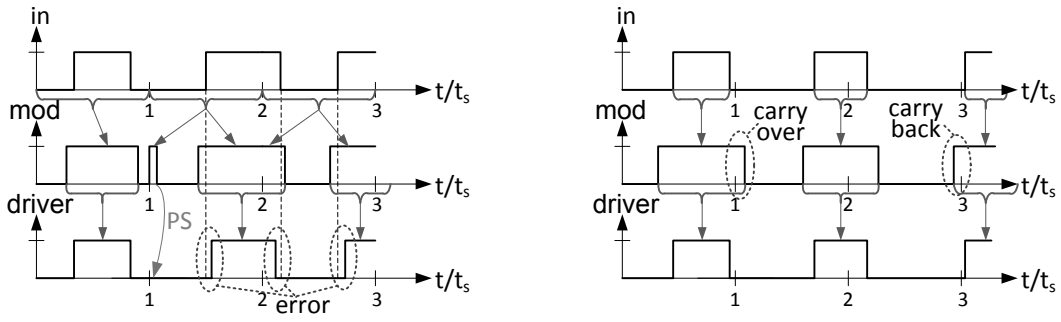


Figure 5.44: Carry over based predistortion block diagram.

For very wideband signals one sample varies significantly from the other and a predistortion that works only on a per sample basis cannot fully correct the signal anymore. In Fig. 5.45 examples highlighting the difference between sample and pulse based predistortion are provided. By applying the predistortion on a per sample basis the relation of the pulses with the adjacent samples is ignored. For the first period in Fig. 5.45(a) the pulse occurs in the middle of the sampling period and thus has no influence on the other samples after predistortion. In this case the sample based predistortion delivers the correct results. But during the second period the predistorted signal results in a circular shifted pulse with only a very short pulse at the beginning of the sample period. After the driver this pulse disappears due to the PS effect. This leads to an error. Also in case of a pulse covering two adjacent sampling periods, such as in the third period the correction applied on a per sample basis delivers a wrong result, as the driver nonlinearity acts on a per pulse basis.



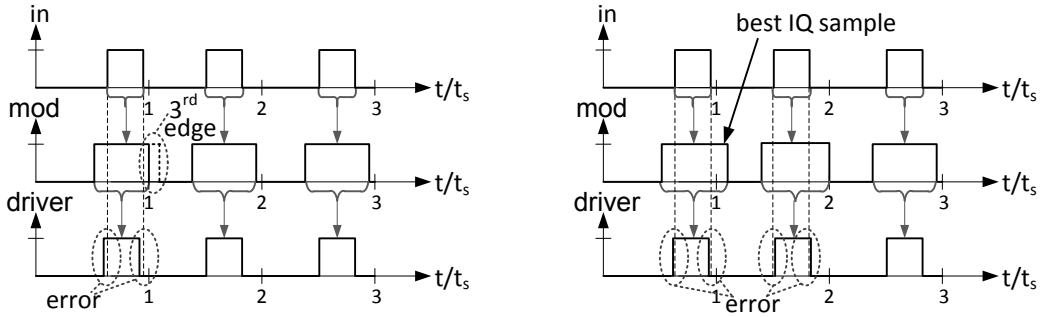
(a) Sample based

(b) Pulse based

Figure 5.45: Sample and pulse based predistortion carry over/back effects.

In order to compensate for the behavior of the driver circuit the predistortion has to be applied on a per pulse basis, as depicted in Fig. 5.45(b). As a result, the nonlinearity of the driver can be perfectly compensated, with the drawback of introducing some special effects. After predistortion the pulse might be extended to reach into the next sample period (carry over) or it might be expanded to the previous sample period (carry back). In both cases interaction with the adjacent samples is given and therefore it is required to take the previous and the upcoming sample, Carry Over (CO) effect, into account for the calculation of the predistortion signal.

Due to CO effects it is possible that three signal edges within one sample period occur. Fig. 5.46(a) provides such an example. The pulse from the first period is extended to the second period, while the second pulse still completely remains within the second period after predistortion. As a result three signal transitions for the second carrier period are desired. But the modulator can only provide a single (circular shifted) pulse and thus cannot generated the desired signal. One option could be to ignore the CO contribution, as depicted in Fig. 5.46(a). As a result the pulses after the driver shows some error in the first period. By simply skipping the CO contribution a single sided error is generated, which is correlated to the signal and leads to raise of the inband noise floor.



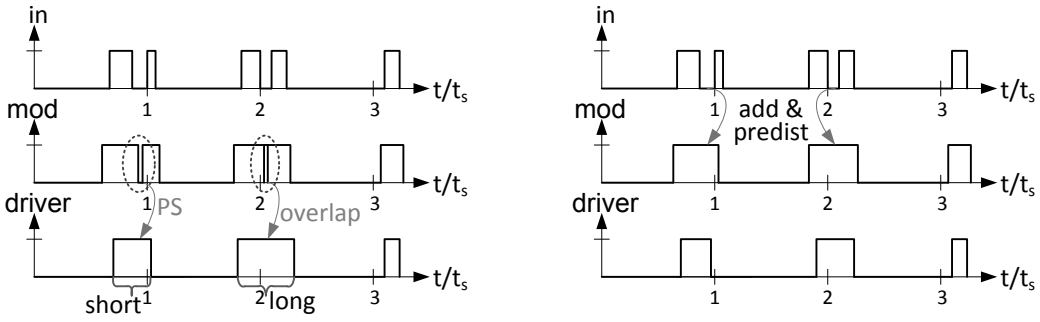
(a) Skip CO (b) Additive approach

Figure 5.46: Pulse predistortion time domain three signal transitions.

Instead of skipping the contribution of the CO pulse it can be considered as an additive manner. Fig. 5.46(b) provides a corresponding example. The IQ values of the predistorted pulses in the second period are calculated and added. The result is a pulse which represents the closest sample in the IQ domain. In this example the resulting pulse in the second period is slightly shifted compared to the CO skipping approach in Fig. 5.46(a) and exhibits circular properties such that it can be represented by the modulator. By using this additive approach the error is distributed among the two pulses involved and does not have a single side preference. The resulting error spectrum exhibits a $\Delta\Sigma$ like behavior, as the error signal energy is shifted out of the band. This way high inband signal quality can be maintained and thus the additive approach is included in the proposed predistortion scheme in Fig. 5.44. By calculating the IQ values of the pulses individually the contribution of the adjacent pulses, as well as the additive handling of the three signal transitions, are implicitly considered.

Another problem that can occur for very rapidly varying signals is the overlap of signals after predistortion. In Fig. 5.47(a) such an example is depicted. After predistortion the signal transitions of the first and the second sample are in very close vicinity. As a result the negative pulse between the two signals cannot be generated due to PS, which leads to the fact that the generated pulse by the driver is too short. If the desired pulses are even closer, as for the transition of the second to the third sample, the required predistortion signal can overlap. This leads to an error during the signal calculation and results in a

pulse after the modulator, that is too long. In both cases involved the final signal after the modulator is erroneous, which leads to a degradation of the signal quality.



(a) Skip CO

(b) Additive approach

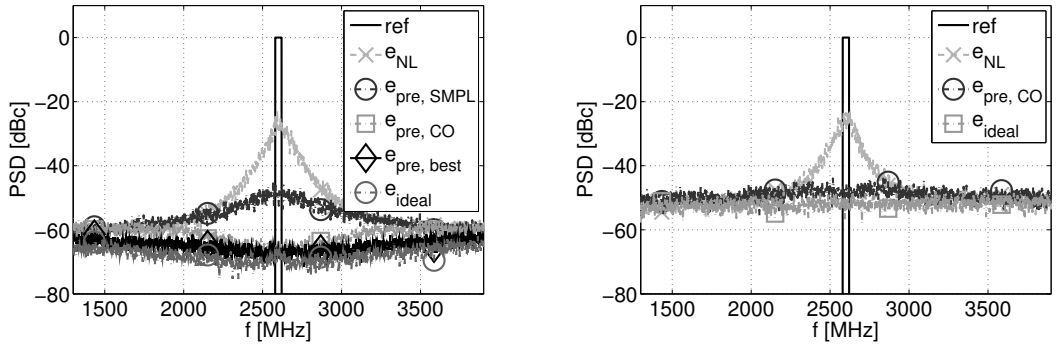
Figure 5.47: Pulse predistortion circular overlap problem.

The problem can be resolved by detecting and handling such a situation. Instead of treating the pulses individually they are 'added' in the IQ domain to give a single pulse that closely represents the signal content of the two pulses. Fig. 5.47(b) provides a corresponding example. The pulses for which the overlap problem would occur are combined in an additive way and predistorted. The result are well controlled pulses of the modulator, as well as after the driver. Still a residual error exists, which experiences $\Delta\Sigma$ like noise shaping due to the addition of the pulses. Nevertheless this situation occurs rarely as it is only caused by very rapidly varying phase signals, which are corrected by the CPE anyways.

In Fig. 5.48(a) the spectra of the CO based predistortion for a modulator with 10 bit resolution are plotted. It depicts the reference signal (ref) and the error signal (e_{NL}) caused by the nonlinearity, if no predistortion is applied. By using the sample based approach for predistortion, the signal quality $e_{pre,SMPL}$ can be improved, but is still limited. This is caused by errors due to the CO effects, which are neglected. Applying the proposed CO based predistortion improves the signal quality $e_{pre,CO}$ significantly, coming close to the noise floor of an ideal driver e_{ideal}. The difference between the ideal and the CO based predistortion spectrum is caused by two effects. Due to the nonlinearity the quantization steps are slightly shifted. This leads to an increase of the noise floor. This can be seen in trace $e_{pre,best}$, which depicts the error signal of the predistortion applied on a per pulse basis, ignoring the limitations of the modulator (3 pulses/period are allowed). Considering the limitations of the driver by applying the IQ addition of the single pulses within one sample period results in the small increase of the out of band spectrum $e_{pre,CO}$ for the CO based predistortion. Nevertheless high inband signal quality can be achieved.

For reduced modulator resolution, as depicted in Fig. 5.48(b), the spectrum after predistortion $e_{pre,CO}$ shows still an increased noise floor around the signal band. This is caused by the modified quantization of the nonlinearity and is not a residual error of the predistortion. Fig. 5.49 provides an example for the influence of the driver nonlinearity on the amplitude quantization. For ideal driver characteristic, as plotted in Fig. 5.49(a), the resulting quantization steps are equally distributed.

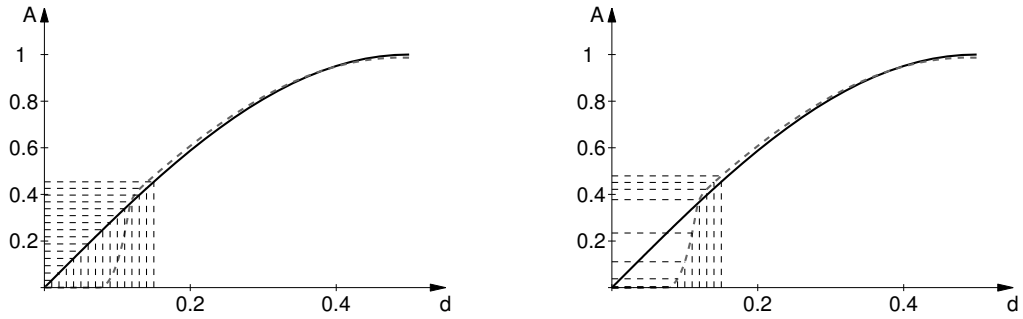
The driver nonlinearity in the pulse swallowing region, such as in Fig. 5.49(b), leads to increased quantization steps due to the step amplitude response with respect to the duty cycle. In the most extreme case for hard pulse swallowing only a single quantization step in the pulse swallowing region is available. The resulting coarse quantizations lead to an increase of the effective amplitude resolution, as well as to a partial correlation with the signal. Therefore, the inband signal quality cannot completely be restored by the predistortion.



(a) 10 bit resolution

(b) 7 bit resolution

Figure 5.48: Spectra for a 40 MHz bandwidth signal at 2.6 GHz with driver nonlinearity corrected by different predistortion schemes.



(a) Ideal

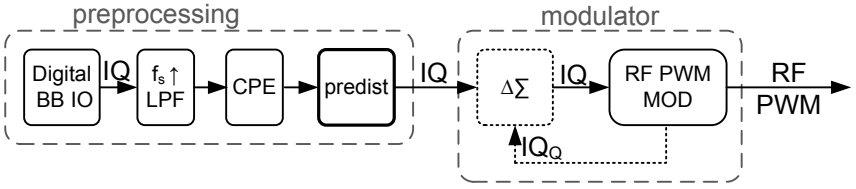
(b) Nonlinear

Figure 5.49: Increased quantization step due to nonlinearity.

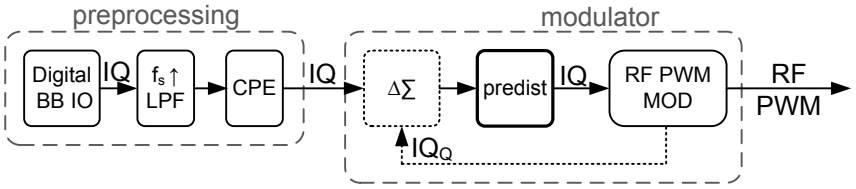
A method to decorrelate and shape the quantization error is the use of a $\Delta\Sigma$ modulator. The predistorter can either be located before the $\Delta\Sigma$, as depicted in Fig. 5.50(a), or the predistorter can be integrated in the $\Delta\Sigma$ loop (Fig. 5.50(b)).

Both predistorter locations have their advantages and drawbacks. When including the predistortion in the $\Delta\Sigma$ loop, as depicted in Fig. 5.50(b), the correct calculation of the CO based predistortion is not possible. Due to the noise shaping of the $\Delta\Sigma$ the next sample cannot be predicted and therefore the CO based predistortion cannot be calculated properly. Therefore, only the sample based predistortion approach can be applied within the $\Delta\Sigma$ loop. As a result the overall signal quality is determined by the limitations of the sample based predistortion approach.

Locating the predistorter before the $\Delta\Sigma$, as done in Fig. 5.50(a), allows for the calculation of the CO based predistortion. A drawback of this combination is that only the inband signal is considered in the predistortion. As a result the out of band quantization noise shifted by the $\Delta\Sigma$ folds back into the signal band due to the driver nonlinearity. This effect can be seen in Fig. 5.51, which depicts the predistortion results for a 7 bit modulator with and without $\Delta\Sigma$ operation. For normal quantization the nonlinearity error e_{NL} can be improved to e_{pre} by applying the CO based predistortion. The inband spectral quality is still limited by the resolution and is further increased by the partial correlation of the quantization noise. By applying a 1^{st} order $\Delta\Sigma$ modulator after the predistortion the spectral quality can be improved to $e_{pre,\,DS}$. The achievable resolution enhancement is



(a) Before $\Delta\Sigma$



(b) Within $\Delta\Sigma$

Figure 5.50: Predistorter location.

limited compared to the ideal case ($e_{ideal,DS}$), as a part of the out of band quantization noise is folded back into the signal band due to the nonlinear driver behavior.

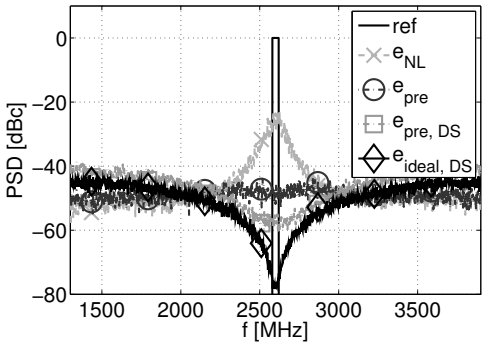
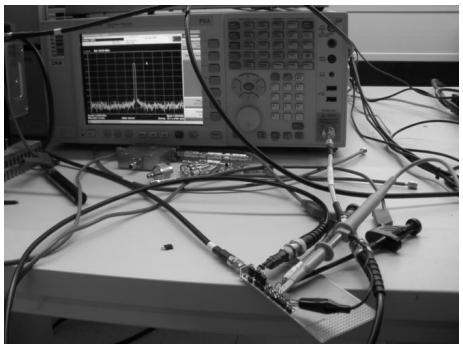


Figure 5.51: Spectra for a 40 MHz bandwidth signal at 2.6 GHz with driver nonlinearity corrected by pre $\Delta\Sigma$ predistortion using 1st order $\Delta\Sigma$.

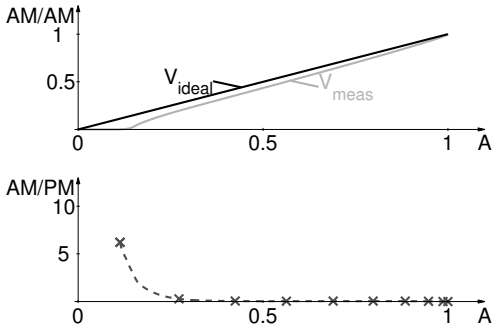
These effects impose a limit for the signal quality of this combined predistortion/noise shaping approach. Although the quantization noise that is folded back into the signal band imposes a limitation, it was found that this approach delivers better results than using the sample based predistorter within the $\Delta\Sigma$ loop.

5.2.6 Predistortion Measurement Results

In order to verify the proposed predistortion scheme a driver model has been built. The same measurement equipment as in section 5.2.3.5 has been used, limiting the operating frequency to 1 MHz in order to provide sufficient resolution. The driver was built using several discrete inverters [272] soldered onto a prototyping board, which were loaded with a shunt capacitance to decrease their rise/fall times to emulate the expected behavior at 2.65 GHz. Fig. 5.52(a) shows a picture of the measurement setup including the driver model. The measured AM/AM and AM/PM distortion of the driver after two inverters is depicted in Fig. 5.52(b).



(a) Measurement setup



(b) Driver AM/AM and AM/PM

Figure 5.52: Measurement setup and driver distortion.

The statically measured distortion behavior is used for the predistortion of the modulated signals after their CPE correction. The signal processing chain provided in Fig. 5.50(a) was used for the measurements. A signal bandwidth of 20 kHz at the carrier frequency of 1 MHz was selected, which roughly corresponds to 40 MHz bandwidth at 2.65 GHz. The corresponding measurement results considering a resolution of 10 bit without noise shaping are provided in Fig. 5.53. It can be seen that without applying any predistortion (no pred) the signal is highly distorted and the spectral quality is rather poor. By applying the sample based predistortion (smpl based) the signal quality can already be improved, but still suffers from errors due to carry over effects. The best results can be achieved by using the proposed carry over based predistortion, as can be seen in trace 'CO based'.

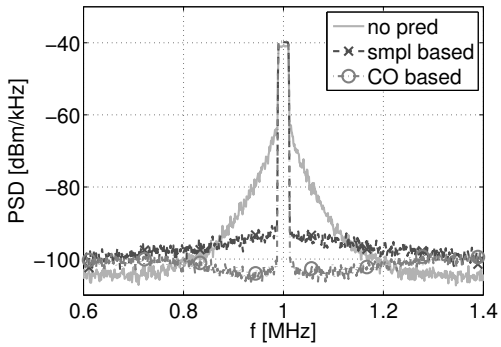
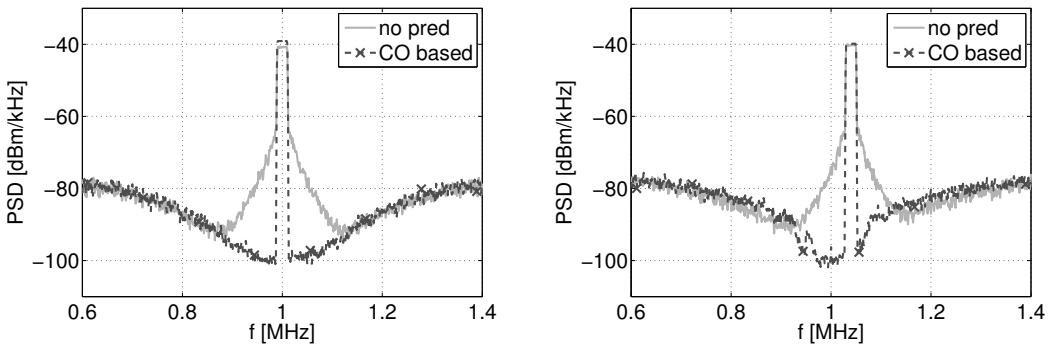


Figure 5.53: Measured signal at the driver output at 1 MHz carrier frequency, 20 kHz bandwidth and 10 bit resolution.

In practice a resolution of around 7 bit is common for carrier frequencies around 2.65 GHz. Therefore, the same measurement using a resolution of 7 bit, while applying 2^{nd} order $\Delta\Sigma$ noise shaping, has been repeated. Fig. 5.54(a) provides the corresponding results. It can be seen that by using the carry over based predistortion approach the signal quality can be significantly increased, but the inband noise floor is limited by the out of band quantization noise that is folded back into the band by the nonlinearity.

In order to support multi band and multi standard operation the capability of generating signals with a frequency offset is a very important functionality. Therefore, a measurement with 40 kHz carrier offset, as depicted in Fig. 5.54(b), has been carried out. It can be seen that the signal quality almost reaches the values without a frequency offset, offering significant improvement by using the carry over based predistortion.



(a) No frequency offset

(b) 40kHz frequency offset

Figure 5.54: Measured signal at the driver output at 1 MHz carrier frequency, 20 kHz bandwidth and 40 kHz frequency offset (carrier aggregation) and 7 bit resolution.

5.2.7 Digital Mismatch Compensation

Beside the driver nonlinearity the device mismatch of the phase modulators can have a significant impact on the overall performance. Due to accuracy limits within the manufacturing process the properties of the single devices deviate from each other. This leads to a deviation between the real phase response of the modulator and the theoretical linear one. The impact of the device mismatch can be reduced by adding hardware tuning elements or by digitally compensating the phase modulator behavior in the signal generation. Fig. 5.55 depicts a block diagram for digital mismatch compensation. In order to correct the mismatch it has to be identified by measuring the phase response of the modulator. This phase response delivers the PM/PM characteristic for each branch. Based on the inverse PM/PM characteristic the outphasing signals for each branch are corrected prior to quantization. The quantization step is followed by an optional Look Up Table (LUT) for scrambling to account for non monotonic phase responses of the modulator.

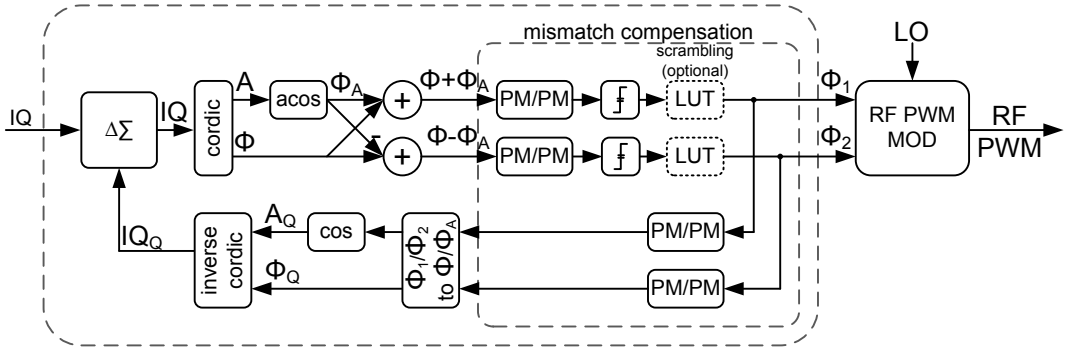


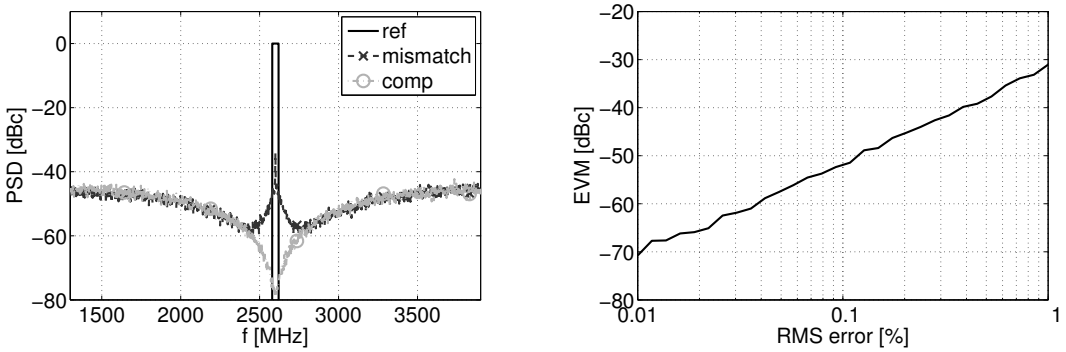
Figure 5.55: ΔΣ and digital mismatch compensation.

The ΔΣ modulator is optional and can be used in order to increase the inband signal quality. In order to provide the correct feedback signal it is required to consider the real modulator behavior by applying the identified PM/PM characteristic to each branch prior to the calculation of the quantized IQ_Q value.

The required LUT size and hence measurement effort for the parallel architecture presented in section 5.2.1 is 2 x N, where N denotes the phase resolution. As the impact of the mismatch of the single branches is independent from each other the mismatch of each output combination (N x N) can be calculated from the 2 x N data. For the series archi-

tecture the influence of the modulator's mismatch is coupled and therefore it is required to identify the full N x N matrix for compensation. Aside from a significant increase in measurement effort, the implementation complexity increases. Thus the series architecture has significant drawbacks in terms of mismatch compensation.

In Fig. 5.56(a) an example for the digital mismatch compensation of a parallel modulator with 7 bit resolution combined with a 1st order $\Delta\Sigma$ is provided. It can be seen that without compensation the noise floor around the inband signal is significantly increased. The mismatch leads to a non uniform quantization and therefore the quantization noise if partially correlated with the signal. This leads to the rise around the signal band. As in this region high signal quality is most important, mismatch compensation is required. By applying the digital mismatch compensation scheme proposed in Fig. 5.55, high signal quality can be recovered.



(a) Spectrum (b) Measurement sensitivity

Figure 5.56: Mismatch compensation and measurement sensitivity for 1st order $\Delta\Sigma$.

A main factor for the mismatch compensation is the accuracy of the mismatch identification. Measuring the response of the phase modulator is only possible up to a certain accuracy when using measurement instruments. The resulting measurement error directly translates to reduced signal quality as the signal in the feedback path, used for noise shaping, and the actually generated signal deviate. This limits the effectiveness of the digital mismatch compensation. Fig. 5.56(b) depicts the sensitivity of the Error Vector Magnitude (EVM), which is defined here as the average inband noise floor, to the measurement accuracy. The EVM directly depends on the measurement accuracy given by the Root Mean Square (RMS) measurement error with respect to the full phase modulator resolution. Thus for highest signal quality it is required to measure the modulator mismatch with an accuracy in the sub picosecond range, which imposes a great challenge for the measurement instrumentation. Another important factor is that the mismatch remains constant over time, temperature or voltage variations. This could be ensured by using a locking mechanism, such as the one proposed in Fig. 5.23(a).

5.3 Summary RF PWM

In this chapter the general difference between BB PWM and RF PWM operation and the advantages of purely digital RF PWM signal generation have been highlighted. The responses of different amplifier classes to RF PWM operation have been investigated. It has been found that for all the amplifiers, except the inverter based voltage mode class D, no significant efficiency enhancement in back off is possible by pure RF PWM operation. Moreover, the relation of the output voltage to the duty cycle is highly nonlinear for most

amplifier classes.

Nevertheless the concept of RF PWM is well suited for providing an efficient modulator implementation with a single bit digital output. In order to achieve highest signal quality, analog and digital effects have to be compensated. Therefore, the second part of this chapter was dedicated to the required signal processing for best spectral quality. Aliasing effects due to the discrete time nature of the digital modulator have been identified and an approach for their mitigation has been developed. The properties of the different variants of the developed compensation scheme based on Cross Point Estimation (CPE) have been evaluated in detail. In addition the properties of driver circuits for the RF PWM signal generations have been studied. The nonlinear behavior of real driver implementations results in reduced signal quality. In order to remove the driver's influence a special predistortion scheme for wideband signals has been developed. By performing the proposed predistortion on a per pulse and not on a per sample basis best performance can be achieved. Finally a concept for the digital compensation of the (device) mismatch of the phase modulators was derived and evaluated.

A big drawback of the signal processing schemes developed is their requirement for running at carrier rate. This imposes a big challenge for the implementation of the signal processing circuitry for transmitters operating in the GHz range. Nevertheless the impact of the specific errors has been highlighted and the demand for their compensation has been shown.

6. Conclusion

In the first chapter the general operational principle of PAs has been discussed and a new circuit variant for the class DE PA based on a parallel compensation inductance [S1] has been proposed. Additionally the requirements on the static efficiency curve for achieving good average efficiency have been derived. Based on a simplified circuit model the different loss mechanisms of RF power transistors and their influence on the efficiency of load modulation have been discussed [S2].

The second chapter deals with different efficiency enhancement concepts, where a main focus was set on BB PWM operation. The properties of BB PWM operation using an isolated load and the prospects of direct filter connection have been highlighted. Beside that different energy recovery methods have been reviewed and a concept for direct reuse of the out of band energy of BB PWM transmitters [S3] has been introduced. With that concept theoretical 100 % efficiency over the whole output power range can be achieved.

A main chapter is dedicated to the design of PAs suitable for the use of BB PWM and direct filter connection. At first the concept of band limited BB PWM to avoid the aliasing problems of digital BB PWM is introduced. For the design of direct filter connection the resulting load modulation trajectories are very important. Therefore, generalized equations [S4] to determine the load modulation trajectories for BB PWM with arbitrary levels have been derived. For the efficient operation of the direct filter connection it is required to provide a high impedance over a wide frequency range for the modulation sidebands [S7]. Therefore, a study of the impact of the coupling on the reflections of cavity filters [S5] has been carried out. The results provide the starting point for the matching network design, which is done as a codesign of microstrips on PCB level and the cavity filter. For best performance it is required to have short connection between filter and PA within the matching network. Four different integrated circuits for direct filter connection have been designed. Two of them are based on a parallel approach, either on a common drain [S6] or a common source design [S8]. The other two PA designs follow a series approach by adding a switch to a cascode [S9, S10] and by source modulation [S11]. Amongst them the source modulation circuit shows the best efficiency performance, while requiring only one RF and one digital input signal.

The second main chapter is dedicated to RF PWM, in that context the PA properties under RF PWM excitation are discussed, but the main focus is set on the required signal processing for highest signal quality. In that context a method for the reduction of aliasing effects of digital RF PWM modulators based on Cross Point Estimation (CPE) has been developed [S12, S13]. Additionally a special predistortion scheme dedicated to the properties of RF PWM has been developed to account for the driver nonlinearity. Finally a digital mismatch compensation scheme that can optionally be combined with $\Delta\Sigma$ modulation, has been introduced.

The concept of BB PWM could possibly be applied to smaller base stations by properly integrating existing BPFs into the matching network and using multilevel MMIC circuits. This includes the use of higher order filter networks and the optimization of the integration into the matching network, with the aim to provide a high impedance for the modulation sidebands over a very wide bandwidth. Further investigations into the digital predistortion of BB PWM signal based on the presented suggestions could result in improved spectral quality.

The presented RF PWM modulator concept could be used to replace conventional RF upconverters in small transceivers, where the power consumption of the DACs and mixers is critical for the system performance. Another benefit is the flexibility and reconfigura-

bility of such a modulator providing a step towards a fully digital transmitter. In order to achieve the best performance of the RF PWM modulator, accounting for the nonidealities of a real modulator, the proposed compensation schemes have to be implemented in hardware together with the RF PWM modulator core, providing a device that features direct base band to RF conversion.

7. Appendix

7.1 Generic Linear PA

In this section the efficiency of a general linear amplifier (class A to class C) as depicted in Fig. 7.1 is derived.

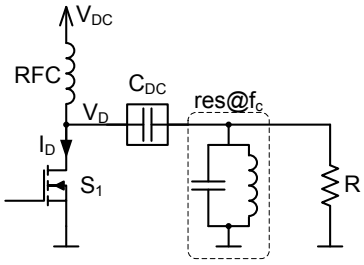


Figure 7.1: General class A, B and C schematic.

Its drain current is defined by

$$I_D(\theta) = \begin{cases} I_{D,MAX}\left((1-k)\ m\ \sin(\theta) + k\right) & -\alpha \leq \theta\ \leq \pi + \alpha \\ 0 & \text{else} \end{cases}, \tag{7.1}$$

where $I_{D,MAX}$ denotes the maximum drain current of the transistor, k is the normalized bias current and m is the normalized current amplitude, respectively normalized gate voltage. In order to generate only a positive drain current the (integration) border α is given by

$$\alpha = \min\left(\sin^{-1}\left(\frac{k}{(1-k)\,m}\right); \frac{\pi}{2}\right). \tag{7.2}$$

The restriction to a maximum of $\pi/2$ is required to also cover the case that the load drain current is never zero (eg. class A operation).

The drain voltage is given by

$$V_D(\theta) = V_{DC}\left(1 - V\ \sin(\theta)\cos(\phi) - V\ \cos(\theta)\sin(\phi)\right), \tag{7.3}$$

where V_{DC} denotes the drain bias voltage, V the normalized drain, voltage swing and ϕ the phase angle of the load in case it is not purely resistive. As all higher order harmonics of the drain voltage are short circuited, only the fundamental of the drain current is of importance. It can be calculated by performing a Fourier analysis of the time domain signal (7.1) and yields

$$I_L = \frac{1}{\pi}\int_{-\alpha}^{\pi+\alpha} I_D(\theta)\sin(\theta)d\theta = \frac{I_{D,MAX}}{\pi}\left((1-k)\,\frac{m}{2}\left(\pi + 2\alpha - \sin(2\alpha)\right) + 2k\cos(\alpha)\right). \tag{7.4}$$

The resulting power dissipation in the transistor depends on the average drain voltage and current overlap and is given as

$$P_T = \frac{1}{2\pi}\int_{-\alpha}^{\pi+\alpha} I_D(\theta)V_D(\theta)d\theta, \tag{7.5}$$

which yields

$$P_T = \frac{I_{D,MAX} V_{DC}}{2\pi} \Big[((1-k)\, m - k\, V \cos(\phi))\, 2\cos(\alpha) + k\,(\pi + 2\alpha) - V\,(1-k)\,\frac{m}{2}\cos(\phi)\,(\pi + 2\alpha - \sin(2\alpha)) \Big]. \tag{7.6}$$

The output power delivered to the load can be calculated by

$$P_L = \frac{I_L V_L \cos(\phi)}{2}, \tag{7.7}$$

where the load voltage V_L is given by

$$V_L = |I_L Z_L| = V_{DC} V. \tag{7.8}$$

The drain efficiency is given by

$$\eta_D = \frac{P_L}{P_L + P_T} \tag{7.9}$$

and depends on the output power and the power dissipated in the transistor.
Considering class A operation ($k = 0.5, \alpha = \pi/2$) the load current I_L can be simplified to

$$I_{L,A} = \frac{I_{D,MAX} m}{2}. \tag{7.10}$$

Assuming a purely resistive load ($\phi = 0$) allowing for maximum voltage swing for the maximum drain current ($m = V$) the power delivered to the load can be rewritten as

$$P_{L,A} = I_{D,MAX} V_{DC} \frac{V^2}{4}. \tag{7.11}$$

The maximum output power ($V = 1$) with respect to the maximum drain voltage ($V_{D,MAX} = 2V_{DC}$) is given by

$$P_{L,A} = \frac{I_{D,MAX} V_{D,MAX}}{8}. \tag{7.12}$$

The power dissipated in the transistor can be calculated by

$$P_{T,A} = I_{D,MAX} V_{DC} \left(\frac{1}{2} - \frac{V^2}{4} \right). \tag{7.13}$$

Furthermore the efficiency for class A operation can be calculated by (7.9) taking (7.11) and (7.13) into account. This delivers

$$\eta_A = \frac{I_{D,MAX} V_{DC} \frac{V^2}{4}}{I_{D,MAX} V_{DC} \frac{V^2}{4} + I_{D,MAX} V_{DC} \left(\frac{1}{2} - \frac{V^2}{4} \right)} = \frac{V^2}{2} \tag{7.14}$$

with respect to the normalized load voltage V.
Performing the same calculations for class B operation ($k = 0, \alpha = 0$) and a purely resistive load ($\phi = 0$), the load current I_L evaluates to

$$I_{L,B} = \frac{I_{D,MAX} m}{2}, \tag{7.15}$$

showing linear behavior. The result is the same as for class A operation and thus the power delivered to the load is also the same as for class A operation (7.13).

The power dissipation in the transistor for class B operation is given by

$$P_{T,B} = I_{D,MAX} V_{DC} \left(\frac{V}{\pi} - \frac{V^2}{4} \right). \tag{7.16}$$

Thus the efficiency for class B operation with respect to normalized load voltage V is given by

$$\eta_B = \frac{I_{D,MAX} V_{DC} \frac{V^2}{4}}{I_{D,MAX} V_{DC} \frac{V^2}{4} + I_{D,MAX} V_{DC} \left(\frac{V}{\pi} - \frac{V^2}{4} \right)} = \frac{V\pi}{4} \tag{7.17}$$

7.2 Class D

7.2.1 Current Mode Class D RF PWM

In this section the control characteristic of the current mode class D PA with respect to RF PWM will be derived. The circuit for the current mode class D PA is given in Fig. 7.2.

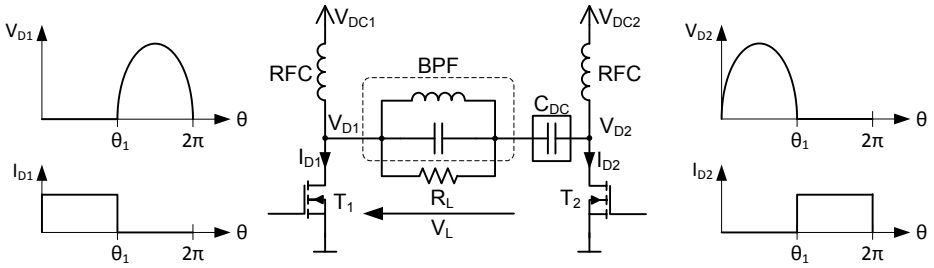


Figure 7.2: Current mode class D.

The load voltage can be set to

$$V_L = N \cos(\theta) + V_{L\,DC} \tag{7.18}$$

to maintain symmetry and to allow for easier integration. The drain voltages during the first period $-\theta_1/2 \leq \theta \leq \theta_1/2$ can be written as

$$V_{D1}^1 = 0;\ V_{D2}^1 = V_L \tag{7.19}$$

and during the second period $\theta_1/2 \leq \theta \leq (2\pi - \theta_1/2)$ as

$$V_{D1}^2 = -V_L;\ V_{D2}^2 = 0. \tag{7.20}$$

It shall be noted that the superscript x^1 denotes the first period, where T_1 is active, and the superscript x^2 denotes the second period, where T_2 is active. The DC content of the drain voltages has to correspond to the supply voltages and can be calculated by the integral over one cycle

$$V_{DC1} = \frac{1}{2\pi} \int_0^{2\pi} V_{D1} d\theta = \frac{1}{2\pi} \int_{\theta_1/2}^{2\pi-\theta_1/2} -(N\cos(\theta) + V_{L\,DC}) d\theta = \frac{N \sin(\frac{\theta_1}{2}) + (\frac{\theta_1}{2} - \pi) V_{L\,DC}}{\pi}. \tag{7.21}$$

$$N = \frac{\pi V_{DC1} - (\frac{\theta_1}{2} - \pi) V_{L\,DC}}{\sin(\frac{\theta_1}{2})} \tag{7.22}$$

Doing the same for the second drain voltage delivers

$$V_{DC2} = \frac{1}{2\pi} \int_{0}^{2\pi} V_{D2} d\theta = \frac{1}{2\pi} \int_{-\theta_1/2}^{\theta_1/2} (N\cos(\theta) + V_{L\,DC}) d\theta = \frac{N\sin(\frac{\theta_1}{2}) + \frac{\theta_1}{2} V_{L\,DC}}{\pi}. \tag{7.23}$$

Resolving for N yields

$$N = \frac{\pi V_{DC2} - \frac{\theta_1}{2} V_{L\,DC}}{\sin(\frac{\theta_1}{2})}. \tag{7.24}$$

Setting (7.22) and (7.24) equal and resolving for $V_{L\,DC}$ delivers

$$V_{L\,DC} = V_{DC2} - V_{DC1}. \tag{7.25}$$

For equal supply voltages $V_{DC} = V_{DC1} = V_{DC2}$ the control characteristic reduces to

$$N = \frac{\pi V_{DC}}{\sin(\frac{\theta_1}{2})}. \tag{7.26}$$

The output power for this case is given by

$$P_L = \frac{N^2}{2R_L} = \frac{\pi^2 V_{DC}^2}{2R_L \sin^2(\frac{\theta_1}{2})}. \tag{7.27}$$

The maximum negative voltage at the drain is given by $V_{D1}(\theta_1)$ and can be calculated using

$$V_{D1\,N} = -N\cos(\frac{\theta_1}{2}) = -\frac{\pi V_{DC}}{\sin(\frac{\theta_1}{2})}\cos(\frac{\theta_1}{2}) = -\pi V_{DC}\cot(\frac{\theta_1}{2}), \tag{7.28}$$

which results in large negative voltages for lower duty cycles.

A modified version of the current mode class D PA with a series resonator load is depicted in Fig. 7.3.

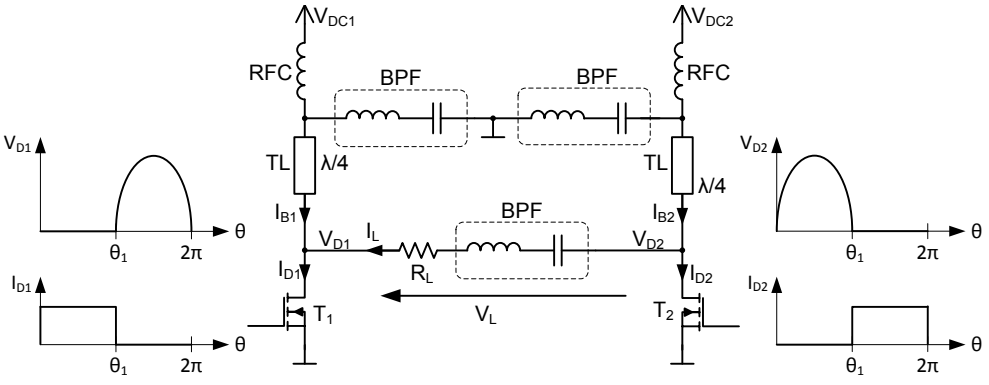


Figure 7.3: Current mode class D with series resonator.

The load current can be set as

$$I_L = \frac{V_{L1}}{R_L}\cos(\theta) \tag{7.29}$$

to maintain symmetry and to allow for easier integration. The drain voltages during the first period $-\theta_1 \leq \theta \leq \theta_1$ can be written as

$$V_{D1}^1 = 0;\ V_{D2}^1 = N_2\left(\cos(\theta) - \cos(\frac{\theta_1}{2})\right) \tag{7.30}$$

and during the second period $\theta_1 \leq \theta \leq (2\pi - \theta_1)$ as

$$V_{D1}^2 = N_1 \left(\cos(\frac{\theta_1}{2}) - \cos(\theta) \right); \; V_{D2}^2 = 0. \tag{7.31}$$

The DC content of the drain voltages has to correspond to the supply voltages and can be calculated by the integral over one cycle.

$$\begin{aligned} V_{DC1} = \frac{1}{2\pi} \int_0^{2\pi} V_{D1} d\theta = \frac{1}{2\pi} \int_{\theta_1/2}^{2\pi-\theta_1/2} N_1 \left(\cos(\frac{\theta_1}{2}) - \cos(\theta) \right) d\theta = \\ = N_1 \frac{\sin(\frac{\theta_1}{2}) + (\pi - \frac{\theta_1}{2}) \cos(\frac{\theta_1}{2})}{\pi} \end{aligned} \tag{7.32}$$

$$N_1 = \frac{\pi V_{DC1}}{\sin(\frac{\theta_1}{2}) + (\pi - \frac{\theta_1}{2}) \cos(\frac{\theta_1}{2})} \tag{7.33}$$

$$V_{DC2} = \frac{1}{2\pi} \int_0^{2\pi} V_{D2} d\theta = \frac{1}{2\pi} \int_{-\theta_1/2}^{\theta_1/2} N_2 \left(\cos(\theta) - \cos(\frac{\theta_1}{2}) \right) = N_2 \frac{\sin(\frac{\theta_1}{2}) - \frac{\theta_1}{2} \cos(\frac{\theta_1}{2})}{\pi} \tag{7.34}$$

$$N_2 = \frac{\pi V_{DC2}}{\sin(\frac{\theta_1}{2}) - \frac{\theta_1}{2} \cos(\frac{\theta_1}{2})} \tag{7.35}$$

The load voltage can be defined as

$$V_L = V_{D2} - V_{D1}. \tag{7.36}$$

The Fourier coefficients of the load voltage can be calculated by the Fourier series, which is given by

$$\begin{aligned} V_{L,FUND} = \frac{1}{\pi} \int_0^{2\pi} V_L \cos(\theta) d\theta = -\frac{N_1}{\pi} \int_{\theta_1/2}^{2\pi-\theta_1/2} \left(\cos(\frac{\theta_1}{2}) - \cos(\theta) \right) \cos(\theta) d\theta + \\ \frac{N_2}{\pi} \int_{-\theta_1/2}^{\theta_1/2} \left(\cos(\theta) - \cos(\frac{\theta_1}{2}) \right) \cos(\theta) d\theta \\ = \frac{N_1}{\pi} \left(\sin(\theta_1) + 2\pi - \theta_1 \right) + \frac{N_2}{\pi} \left(\theta_1 - \sin(\theta_1) \right) \end{aligned} \tag{7.37}$$

$$V_{L,FUND} = \frac{V_{DC1} \left(\sin(\theta_1) + 2\pi - \theta_1 \right)}{2 \sin(\frac{\theta_1}{2}) + 2(\pi - \frac{\theta_1}{2}) \cos(\frac{\theta_1}{2})} + \frac{V_{DC2} \left(\theta_1 - \sin(\theta_1) \right)}{2 \sin(\frac{\theta_1}{2}) - 2 \frac{\theta_1}{2} \cos(\frac{\theta_1}{2})} \tag{7.38}$$

Considering equal supply voltage the load voltage can be approximated by

$$V_{L,FUND} \approx V_{DC} \pi. \tag{7.39}$$

The drain current at the fundamental component does not depend on the biasing current and is defined by

$$I_{D1,FUND} = I_L = \frac{V_{L,FUND}}{R_L} = \frac{1}{\pi} \int_0^{2\pi} I_{D1} \cos(\theta) d\theta = \frac{1}{\pi} \int_{-\theta_1/2}^{\theta_1/2} I_{D1,MAX} \cos(\theta) d\theta. \tag{7.40}$$

Solving the integral and rearranging delivers

$$I_{D1,MAX} = \frac{2\pi V_{L1}}{R_L \sin(\frac{\theta_1}{2})} \approx \frac{2\pi^2 V_{DC}}{R_L \sin(\frac{\theta_1}{2})}. \tag{7.41}$$

The maximum drain voltage can be calculated by

$$V_{D1,MAX} = \frac{\pi V_{DC1}\left(\cos(\frac{\theta_1}{2})+1\right)}{\sin(\frac{\theta_1}{2})+(\pi-\frac{\theta_1}{2})\cos(\frac{\theta_1}{2})}. \tag{7.42}$$

7.2.2 Voltage Mode Class D

The properties of the voltage mode class D will be derived in this section. The circuit of the voltage mode class D PA is given in Fig. 7.4.

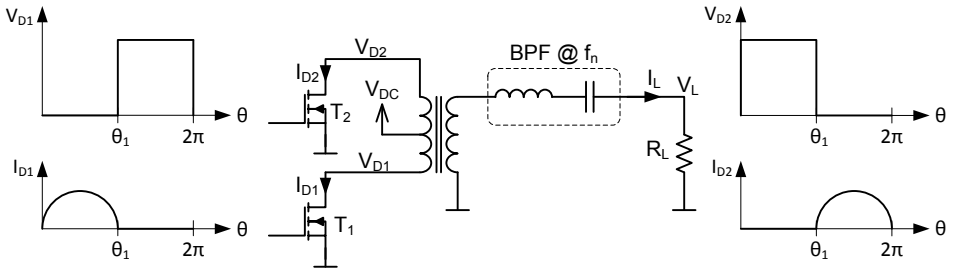


Figure 7.4: Voltage mode class D.

The desired rectangular drain voltages can be written as

$$V_{D1} = K(1-\text{pulse}(\theta)), \tag{7.43}$$

$$V_{D2} = K\,\text{pulse}(\theta), \tag{7.44}$$

with pulse(θ) being

$$\text{pulse}(\theta) = \begin{cases} 1 & 0 \le \theta \le \theta_1 \\ 0 & \text{else} \end{cases}. \tag{7.45}$$

The DC content of the drain voltage of the first transistor can be calculated by

$$V_{DC1} = \frac{1}{2\pi}\int_0^{2\pi} V_{D1}d\theta = \frac{1}{2\pi}\int_{\theta_1}^{2\pi} K\,d\theta = \frac{K(2\pi-\theta_1)}{2\pi}. \tag{7.46}$$

Doing the same for the second transistor results in

$$V_{DC2} = \frac{1}{2\pi}\int_0^{2\pi} V_{D2}d\theta = \frac{1}{2\pi}\int_0^{\theta_1} K\,d\theta = \frac{K\theta_1}{2\pi}. \tag{7.47}$$

Considering the fact that the DC content of both drain signals has to be equal to the supply voltage V_{DC} gives

$$\frac{K(2\pi-\theta_1)}{2\pi} = \frac{K\theta_1}{2\pi}. \tag{7.48}$$

It can be seen that (7.48) can only be held for $\theta_1 = \pi$. Thus the circuit can only be operated in the desired way for equal duty cycles as a result of the fixed DC biasing.

Due to that further derivations will be restricted to $\theta_1 = \pi$. Using (7.46) or (7.47) the scaling factor K can be resolved to $K = 2V_{DC}$.

The fundamental load voltage can be determined by calculating the Fourier transformation of the drain voltage

$$V_L = \frac{1}{\pi}\int_0^{2\pi} V_{D1}\sin(\theta)d\theta = \frac{2V_{DC}}{\pi}\int_0^{\pi}\sin(\theta)d\theta = \frac{4V_{DC}}{\pi}. \tag{7.49}$$

The corresponding load current is given by

$$I_L = \frac{V_L}{R_L} = \frac{4V_{DC}}{\pi R_L}. \tag{7.50}$$

The drain currents are defined as

$$I_{D1} = \begin{cases} I_L\sin(\theta) & 0 \le \theta \le \pi \\ 0 & \text{else} \end{cases} \tag{7.51}$$

and

$$I_{D2} = \begin{cases} 0 & 0 \le \theta \le \pi \\ -I_L\sin(\theta) & \text{else} \end{cases}. \tag{7.52}$$

Considering the maximum drain current $I_{D\,MAX}$ the load resistor can be resolved by

$$R_L = \frac{4V_{DC}}{\pi I_{D\,MAX}}. \tag{7.53}$$

The resulting output power with respect to maximum drain voltage $V_{D\,MAX} = 2V_{DC}$ and maximum drain current is given by

$$P_L = \frac{V_L^2}{2R_L} = \frac{V_{D\,MAX}I_{D\,MAX}}{\pi}. \tag{7.54}$$

Comparing the power per transistor ($P_L/2$) with the output power of a class A PA ($V_{D\,MAX}I_{D\,MAX}/8$) delivers a Power Utilization Factor (PUF) of

$$PUF = \frac{4}{\pi}. \tag{7.55}$$

7.2.3 Inverter Based Voltage Mode Class D

In this section the properties of the inverter based voltage mode class D with respect to RF PWM control will be derived. As efficient control of the output voltage with the push pull configuration is not possible an inverter structure as depicted in Fig. 7.5 can be used.

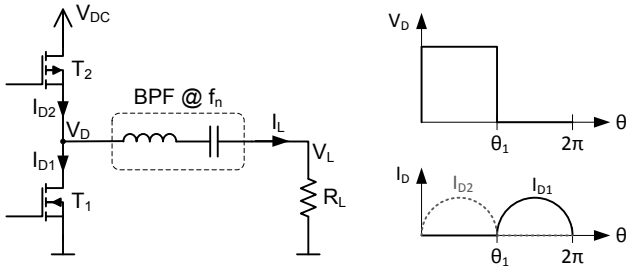


Figure 7.5: Voltage mode class D.

The drain voltage V_D is defined as

$$V_D = V_{DC}\,\mathrm{pulse}(\theta), \tag{7.56}$$

with

$$\mathrm{pulse}(\theta) = \begin{cases} 1 & 0 \le \theta \le \theta_1 \\ 0 & \text{else} \end{cases}. \tag{7.57}$$

The Fourier coefficients of this waveform can be calculated by the Fourier series of the signal, which is given by

$$a_n = \frac{1}{\pi}\int_0^{2\pi} V_D \sin(n\theta)d\theta = \frac{V_{DC}}{\pi}\int_0^{\theta_1} \sin(n\theta)d\theta = V_{DC}\frac{1-\cos(n\theta_1)}{\pi n}, \tag{7.58}$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} V_D \cos(n\theta)d\theta = \frac{V_{DC}}{\pi}\int_0^{\theta_1} \cos(n\theta)d\theta = V_{DC}\frac{\sin(n\theta_1)}{\pi n}. \tag{7.59}$$

The resulting amplitude can be calculated by

$$A_n = \sqrt{a_n^2 + b_n^2} = 2V_{DC}\frac{\sin(n\theta_1/2)}{n\pi}. \tag{7.60}$$

The corresponding phase is given by

$$\phi = \tan^{-1}\left(\frac{a_n}{b_n}\right) = \frac{n\theta_1}{2}. \tag{7.61}$$

The output control characteristic is determined by the amplitude characteristic and it is nonlinear. For predistortion the duty cycle signal has to be generated by $\sin^{-1}$ to generate the desired amplitude signal and to preserve linearity.

A main problem of the voltage mode class D is its capacitive losses due to charging and discharging of the parasitic drain source capacitance C_{DS} of the transistors. To calculate their influence it is required to get the maximum output power of the circuit. The maximum drain amplitude according to (7.60) is

$$V_{MAX} = \frac{2}{\pi}V_{DC}, \tag{7.62}$$

and the maximum load current is simply the maximum transistor current I_{MAX}. Thus the load resistance can be calculated by

$$R_L = \frac{V_{MAX}}{I_{MAX}} = \frac{2V_{DC}}{\pi I_{MAX}} \tag{7.63}$$

and the output power can be written as

$$P_L(V) = V^2 P_{MAX} = V^2\frac{V_{DC}I_{MAX}}{\pi}, \tag{7.64}$$

where V denotes the normalized load voltage.

For the efficiency of the circuit the (constant) capacitive losses have to be taken into account. The capacitive losses have to be considered for both signal transitions and for both transistors, which results in

$$P_{CAP} = 2V_{DC}^2 C_{DS} f_C. \tag{7.65}$$

The resulting maximum efficiency is given by

$$\eta_{MAX} = \frac{P_L(1)}{P_L(1) + P_{CAP}} = \frac{1}{1 + \frac{2\pi V_{DC}C_{DS}f_C}{I_{MAX}}}. \tag{7.66}$$

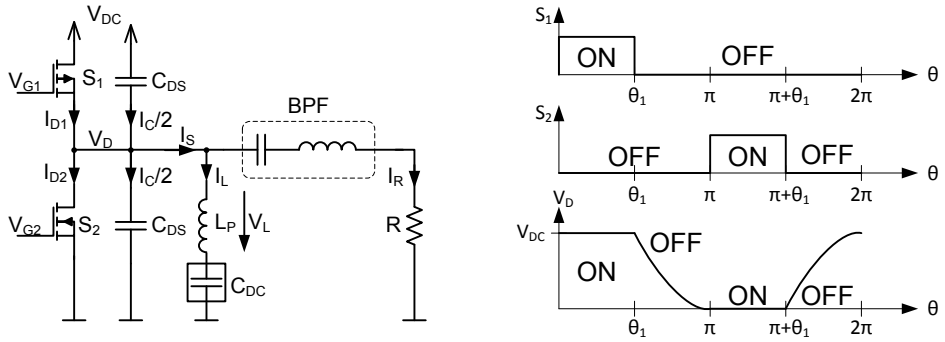
Resolving this equation for P_{CAP} and inserting it into the efficiency calculation delivers

$$\eta(V) = \frac{V^2\eta_{MAX}}{\eta_{MAX}(V^2-1)+1}. \tag{7.67}$$

7.3 Class DE

7.3.1 Class DE With Parallel Compensation Inductance

In this section the properties and design equations for the class DE PA with parallel compensation inductance, as given in Fig. 7.6, will be provided. For the derivation all



(a) Schematic (b) Timing Diagram

Figure 7.6: Voltage mode class DE with parallel compensation inductance.

voltages and currents will be normalized to V_{DC}. Setting up the current and voltage relations for the 1st period (switch S_1 closed) delivers the following relations. Due to the symmetry of the waveform the normalized DC voltage at the drain evaluates to 1/2, hence the inductor voltage during the first period results to

$$V_{L1}(\theta) = \frac{1}{2}, \tag{7.68}$$

The current flow through the capacitor ($I_{C1}(\theta) = 0$) is zero, as the voltage remains constant, while the inductor current is given by

$$I_{L1}(\theta) = \frac{1}{\omega L_P} \int V_{L1}(\theta) d\theta = \frac{1}{2\omega L} \left(\theta + 2I_{L01}\right), \tag{7.69}$$

where I_{L01} denotes the initial inductor current. The load current is defined by

$$I_{R1}(\theta) = \frac{A}{R} \cos\left(\theta\right) + \frac{B}{R} \sin\left(\theta\right) \tag{7.70}$$

and the summation current taking the parallel inductor into account is given as

$$I_{S1}(\theta) = I_{L1} + I_{R1}. \tag{7.71}$$

The voltage at the inductance for the dead time (both switches are open) can be approximated by

$$V_{L2}(\theta) = \left(1 + \cos(\theta)\right) z - \frac{1}{2}. \tag{7.72}$$

The factor n can be resolved by inserting the boundary condition for the beginning of the dead time with $V_{L2}(\theta_1) = 1/2$. This delivers

$$z = \frac{1}{1 + \cos(\theta_1)}. \tag{7.73}$$

The inductance current can be calculated by integrating over the voltage.

$$I_{L2}(\theta) = \frac{1}{\omega L} \int V_{L2}(\theta) d\theta = \frac{1}{\omega L} \left[\left(z - \frac{1}{2} \right) \theta + z \sin(\theta) + I_{L02} \right] \tag{7.74}$$

The load current is the same as during the first period as the series resonant filter forces a sinusoidal current and is defined by

$$I_{R2}(\theta) = I_{R1}(\theta) = \frac{A}{R}\cos(\theta) + \frac{B}{R}\sin(\theta). \tag{7.75}$$

The current through the capacitance is the sum of the load and the inductor current and is given by

$$I_{C2}(\theta) = -I_{L2}(\theta) - I_{R2}(\theta). \tag{7.76}$$

Hence the voltage across the capacitor can be derived by integration.

$$U_{C2}(\theta) = \frac{1}{\omega C}\int I_{C2}(\theta)d\theta \tag{7.77}$$

$$U_{C2}(\theta) = -\frac{1}{\omega^2 LC}\left[\left(z-\frac{1}{2}\right)\frac{\theta^2}{2} - z\cos(\theta) + I_{L02}\,\theta\right] - \frac{1}{\omega RC}\left(A\sin(\theta) - B\cos(\theta)\right) \tag{7.78}$$

By using the requirement that there is a continuous current through the inductance $I_{L1}(\theta_1) = I_{L2}(\theta_1)$ and by taking into account the symmetry of the waveforms $I_{L2}(\pi) = -I_{L1}(0)$ the initial inductor currents can be resolved as

$$I_{L02} = \frac{1}{2}\left[\frac{1}{2}\theta_1 - \left(z-\frac{1}{2}\right)(\pi+\theta_1) - z\sin(\theta_1)\right] \tag{7.79}$$

and the the initial current for period one can be calculated by

$$I_{L01} = \left(\frac{1}{2} - z\right)\pi - I_{L02}. \tag{7.80}$$

By performing a Fourier analysis of the voltage waveform the normalized fundamental voltage components can be determined.

$$A = \frac{2}{\pi}\int_0^{\pi} V_C(\theta)\cos(\theta)d\theta;\;\; B = \frac{2}{\pi}\int_0^{\pi} V_{C1}(\theta)\sin(\theta)d\theta \tag{7.81}$$

$$A = \frac{z}{\pi}\left(\pi - \theta_1 + \frac{\sin(2\theta_1)}{2}\right);\;\; B = \frac{z}{\pi}\left(1 - \cos^2(\theta_1)\right) \tag{7.82}$$

To fulfill class E conditions it is required to have zero current switching.

$$I_{L2}(\pi) + I_{R2}(\pi) = 0 \tag{7.83}$$

When considering (7.74) and (7.75) the inductance can be resolved.

$$L = \frac{R}{\omega A}\left[\left(z-\frac{1}{2}\right)\pi + \frac{\theta_1}{4} - \left(\frac{z}{2}-\frac{1}{4}\right)(\pi+\theta_1) - \frac{z}{2}\sin(\theta_1)\right] \tag{7.84}$$

The equation can be rearranged to calculate the inductance factor K_L as

$$\omega L = R\,K_L, \tag{7.85}$$

which yields

$$K_L = \frac{1}{A}\left[\left(z-\frac{1}{2}\right)\pi + \frac{\theta_1}{4} - \left(\frac{z}{2}-\frac{1}{4}\right)(\pi+\theta_1) - \frac{z}{2}\sin(\theta_1)\right]. \tag{7.86}$$

The voltage difference of the capacitor voltage (7.78) between the two states is exactly the supply voltage $U_{C2}(\theta_1) - U_{C2}(\pi) = V_{DC}$. Taking this into account, inserting (7.79), (7.86) and resolving delivers

$$\omega RC = \frac{1}{K_L}\left[\left(z-\frac{1}{2}\right)\frac{(\pi^2-\theta_1^2)}{2} + 1 + I_{L02}\,(\pi-\theta_1)\right] + B\,(1+\cos(\theta_1)) - A\sin(\theta_1). \quad (7.87)$$

Following that the capacitor factor can be defined as

$$\omega C = \frac{K_C}{R}, \quad (7.88)$$

with

$$K_C(\theta_1) = \frac{1}{K_L}\left[\left(z-\frac{1}{2}\right)\frac{(\pi^2-\theta_1^2)}{2} + 1 + I_{L02}\,(\pi-\theta_1)\right] + B\,(1+\cos(\theta_1)) - A\sin(\theta_1). \quad (7.89)$$

The maximum current through the switch can be determined by using (7.71) and setting its derivative to zero

$$I_{S1}(\theta)\frac{d}{d\theta} = 0. \quad (7.90)$$

Doing so the phase for the maximum current θ'_{MAX} can be resolved.

$$\theta'_{MAX} = \sin^{-1}(arg) + \tan^{-1}\left(\frac{B}{A}\right);\ arg = \frac{1}{2K_L\sqrt{A^2+B^2}} \quad (7.91)$$

The maximum current through the switch occurs either during or at the end of the ON period. The corresponding phase is determined by

$$\theta_{MAX} = \begin{cases} \theta_1 & \theta'_{MAX} > \theta_1 \text{ or } ||arg|| > 1, \\ \theta'_{MAX} & \text{else} \end{cases}. \quad (7.92)$$

The maximum switch current is the normalized switch current times the supply voltage at the maximum current phase $I_{MAX} = V_{DC} I_{S1}(\theta_{MAX})$. Using (7.71) and (7.86) yields

$$I_{MAX} = \frac{V_{DC}}{R}\left[\frac{1}{K_L}\left(\frac{\theta_{MAX}}{2} + I_{L01}\right) + A\cos(\theta_{MAX}) + B\sin(\theta_{MAX})\right]. \quad (7.93)$$

The load resistance can be calculated by

$$R = \frac{V_{DC}}{I_{MAX}} K_R, \quad (7.94)$$

with K_R being the load resistance factor.

$$K_R(\theta_1) = \frac{1}{K_L}\left(\frac{\theta_{MAX}}{2} + I_{L01}\right) + A\cos(\theta_{MAX}) + B\sin(\theta_{MAX}) \quad (7.95)$$

Taking into account that the shunt capacitance is twice the drain source capacitance $C = 2\,C_{DS}$, inserting (7.94) into (7.88) and rearranging the equation results in

$$\omega_{MAX}(\theta_1) = \frac{I_{MAX}\,K_C(\theta_1)}{2C_{DS}V_{DC}\,K_R(\theta_1)}. \quad (7.96)$$

The normalized maximum frequency is defined as

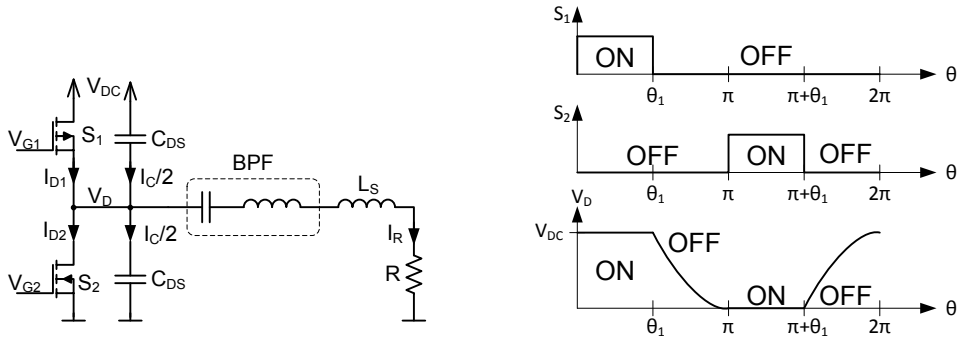
$$\omega_{MAX,N} = \omega_{MAX} C_{DS}\frac{V_{DC}}{I_{MAX}} = \frac{K_C(\theta_1)}{2K_R(\theta_1)}. \quad (7.97)$$

The output power can be calculated using

$$P_L = \frac{{V_{DC}}^2\,(A^2+B^2)}{2R} = \frac{V_{DC} I_{MAX}\,(A^2+B^2)}{2K_R(\theta_1)} \quad (7.98)$$

7.3.2 Class DE Amplifier With Series Inductance

In this section the design parameters for the class DE PA in Fig. 7.7 will be provided. According to [55] the ratio of load resistance R to series inductance L_S is determined by



(a) Schematic (b) Timing Diagram

Figure 7.7: Voltage mode class DE with series compensation inductance.

$$\omega L_S = R\, K_{R,S};\ K_{R,S} = \frac{A}{B}. \tag{7.99}$$

The load current is given by

$$I_R(\theta) = V_{DC} \frac{B}{R} \sin(\theta)\,. \tag{7.100}$$

The voltage across the capacitance can be calculated by integrating the current. The voltage difference during the OFF period has to be the supply voltage and is given by the following relation

$$-V_{DC} = -\frac{1}{\omega C} \int_{\theta_1}^{\pi} I_R(\theta) d\theta. \tag{7.101}$$

Resolving the integral and rearranging the equation delivers

$$\omega RC = K_{C,S};\ K_{C,S} = B\,(1 + \cos(\theta_1))\,. \tag{7.102}$$

The maximum switch current is given by

$$I_{MAX} = V_{DC} \frac{B}{R} \sin(\theta_{MAX})\,, \tag{7.103}$$

with the maximum current phase θ_{MAX} being

$$\theta_{MAX} = \begin{cases} \pi/2 & (\theta_1 > \pi/2)\,, \\ \theta_1 & \text{else} \end{cases}. \tag{7.104}$$

Thus the load resistance can be calculated by

$$R = \frac{V_{DC}}{I_{MAX}} K_{R,S};\ K_{R,S} = B \sin(\theta_{MAX})\,. \tag{7.105}$$

The maximum frequency can be calculated the same way as for the parallel inductance (7.96) and results in

$$\omega_{MAX,S}(\theta_1) = \frac{I_{MAX}\, K_{C,S}(\theta_1)}{2C_{DS} V_{DC}\, K_{R,S}(\theta_1)} = \frac{I_{MAX}\,(1 + \cos(\theta_1))}{2C_{DS} V_{DC} \sin(\theta_{MAX})}, \tag{7.106}$$

with the normalized maximum frequency

$$\omega_{MAX,S,N} = \omega_{MAX,S} C_{DS} \frac{V_{DC}}{I_{MAX}} = \frac{1+\cos(\theta_1)}{2\sin(\theta_{MAX})}. \tag{7.107}$$

The output power for the series compensation inductance can be calculated using

$$P_{L,S} = \frac{{V_{DC}}^2 B^2}{2R} = \frac{V_{DC} I_{MAX} B}{2\sin(\theta_{MAX})}. \tag{7.108}$$

7.4 BB PWM

In this section the average drain efficiency of BB PWM operation between two operational points will be calculated. The load powers for each period with respect to the duty cycle d can be calculated by

$$P_{L1} = \frac{V_{L1}^2 d}{2R_L},\ P_{L2} = \frac{V_{L2}^2 (1-d)}{2R_L}. \tag{7.109}$$

The corresponding DC power consumption is given by

$$P_{DC1} = \frac{V_{L1}^2 d}{2R_L \eta_{D1}},\ P_{DC2} = \frac{V_{L2}^2 (1-d)}{2R_L \eta_{D2}}. \tag{7.110}$$

The average drain efficiency is defined as follows

$$\eta_D = \frac{P_{L1} + P_{L2}}{P_{DC1} + P_{DC2}}. \tag{7.111}$$

Inserting (7.109) and (7.110) into (7.111) and deriving the dependency on the duty cycle d results in

$$\eta_D(d) = \frac{\left(V_{L1}^2 d + V_{L2}^2 (1-d)\right) \eta_{D1}\eta_{D2}}{V_{L1}^2 d\eta_{D2} + V_{L2}^2 (1-d)\eta_{D1}}. \tag{7.112}$$

Considering the relationship of duty cycle and load voltage

$$V = (V_{L1} - V_{L2})d + V_{L2}, \tag{7.113}$$

inserting this into (7.112) and rearranging delivers

$$\eta_D(V) = \frac{\left(V_{L1}^2 (V - V_{L2}) + V_{L2}^2 (V_{L1} - V)\right) \eta_{D1}\eta_{D2}}{V_{L1}^2 (V - V_{L2})\eta_{D2} + V_{L2}^2 (V_{L1} - V)\eta_{D1}}. \tag{7.114}$$

For the system efficiency not only the drain, but also the coding efficiency is important. The coding efficiency is the ratio between the desired in band energy and the total energy generated by the PA.

$$\eta_C = \frac{P_L(V)}{P_{L1} + P_{L2}} \tag{7.115}$$

Taking into account that the inband energy can be calculated by

$$P_L(V) = \frac{V^2}{2R_L} = \frac{\left((V_{L1} - V_{L2})d + V_{L2}\right)^2}{2R_L} \tag{7.116}$$

and inserting into (7.115) and simplifying delivers

$$\eta_C(d) = \frac{\left((V_{L1} - V_{L2})d + V_{L2}\right)^2}{V_{L1}^2 d + V_{L2}^2 (1-d)}. \tag{7.117}$$

Considering (7.113) and rearranging delivers

$$\eta_C(V) = \frac{V^2(V_{L1} - V_{L2})}{V_{L1}^2(V - V_{L2}) + V_{L2}^2(V_{L1} - V)}. \tag{7.118}$$

The system efficiency is the product of drain and coding efficiency and can be calculated by

$$\eta(V) = \eta_D(V)\eta_C(V) = \frac{V^2(V_{L1} - V_{L2})\eta_{D1}\eta_{D2}}{V_{L1}^2(V - V_{L2})\eta_{D2} + V_{L2}^2(V_{L1} - V)\eta_{D1}} \tag{7.119}$$

and is valid for $V_{L2} \leq V \leq V_{L1}$. To cover multilevel operation the calculation has to be done separately for the different levels.

7.5 Energy Recovery

In this section the properties of DC and RF energy recovery systems will be derived. The section deals with DC energy recovery for BB PWM and outphasing and also covers RF energy reuse. Finally the properties of DC BPSK energy recovery are analyzed.

7.5.1 DC Energy Recovery BB PWM

The basic circuit diagram of BB PWM energy recovery is given in Fig. 7.8. Instead of dissipating the energy in the isolator it can be rectified and reused to achieve efficiency enhancement.

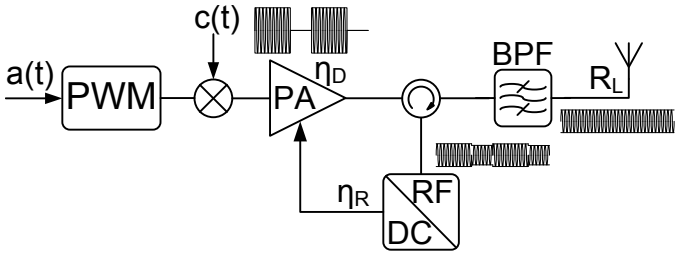


Figure 7.8: DC energy recovery BB PWM.

The power generated by the PA and fed to the circulator with respect to the drain voltage V_D and the duty cycle d is defined as

$$P_D = \frac{V_D^2 d}{2Z_L}. \tag{7.120}$$

The corresponding power at the load is given by

$$P_L = \frac{V_L^2}{2Z_L}. \tag{7.121}$$

Considering $V_L = V_D d$ results in

$$P_L = \frac{V_D^2 d^2}{2Z_L}. \tag{7.122}$$

According to the conservation of energy the sideband power at the rectifier is given by

$$P_{SB} = P_D - P_L = \frac{V_D^2}{2Z_L}(d - d^2). \tag{7.123}$$

The resulting coding efficiency is defined by the ratio of the output power at the load P_L to the total drain power P_D

$$\eta_C(d) = \frac{P_L}{P_D} = \frac{\frac{V_D^2 d^2}{2Z_L}}{\frac{V_D^2 d}{2Z_L}} = d. \tag{7.124}$$

The overall efficiency is given by

$$\eta(d) = \frac{P_L}{P_{DC}} = \eta_C \eta_D = d\eta_D. \tag{7.125}$$

Considering now energy recovery with rectifier efficiency η_R and $P_{DC} = P_D/\eta_d$ gives

$$\eta_{DC}(d) = \frac{P_L}{P_{DC} - P_{SB}\eta_r} = \frac{d^2}{\frac{d}{\eta_D} - (d - d^2)\eta_R} = \frac{d}{1 - (1-d)\eta_R\eta_D}\eta_D. \tag{7.126}$$

Taking into account that the average normalized output voltage is equal to the duty cycle $V = d$ delivers

$$\eta(V) = V\eta_d;\ \eta_{DC}(V) = \frac{V}{1 - (1-V)\eta_R\eta_D}\eta_D \tag{7.127}$$

for the efficiency in dependence to the normalized load voltage.

7.5.2 DC Energy Recovery Outphasing

In this section the theoretical performance of DC energy recovery for outphasing systems will be derived. Fig. 7.9 depicts the block diagram of an outphasing transmitter. Instead of dissipating the out of phase energy (Δ) it can be rectified and reused in order to enhance the efficiency.

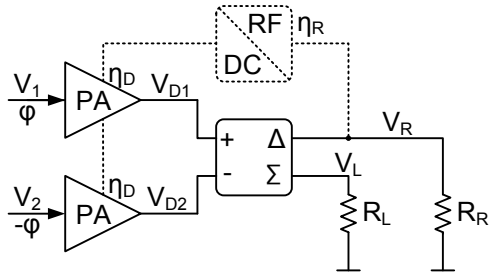


Figure 7.9: DC energy recovery outphasing.

The drain voltages V_{D1} and V_D are defined as

$$V_{D1} = V_D e^{j\phi};\ V_{D2} = V_D e^{-j\phi}. \tag{7.128}$$

The total output power is the sum of the absolute power of both PAs and is given by

$$P_D = \frac{V_{D1}^2 + V_{D2}^2}{2Z_L} = \frac{V_D^2}{Z_L}. \tag{7.129}$$

The voltage at the load resistor and at the out of phase reflection termination is given by

$$V_L = \frac{1}{\sqrt{2}}(V_{D1} + V_{D2});\ V_R = \frac{1}{\sqrt{2}}(V_{D1} - V_{D2}). \tag{7.130}$$

The output power at the load resistor is the inphase combined output power

$$P_L = \frac{V_L^2}{2Z_L} = \frac{V_{D1}^2 + 2V_{D1}V_{D2}\cos(2\phi) + V_{D2}^2}{4Z_L} = \frac{V_D^2(1+\cos(2\phi))}{2Z_L}. \tag{7.131}$$

The power dissipated in the out of phase termination resistor is given by

$$P_R = \frac{V_R^2}{2Z_L} = \frac{V_{D1}^2 - 2V_{D1}V_{D2}\cos(2\phi) + V_{D2}^2}{4Z_L} = \frac{V_D^2(1-\cos(2\phi))}{2Z_L}. \tag{7.132}$$

The efficiency can be calculated using

$$\eta(\phi) = \frac{P_L}{P_D - P_R\eta_D\eta_R}\eta_D = \frac{(1+\cos(2\phi))}{2-(1-\cos(2\phi))\eta_D\eta_R}\eta_D = \frac{\cos^2(\phi)}{1-(1-\cos^2(\phi))\,\eta_D\eta_R}\eta_D, \tag{7.133}$$

where η_R denotes the rectifier efficiency defined in the previous section. Considering that the magnitude of both drain voltages are equal $|V_D| = |V_{D1}| = |V_{D2}|$ the load voltage can be calculated by

$$V_L = \frac{1}{\sqrt{2}}V_D(e^{j\phi} + e^{-j\phi}) = \sqrt{2}V_D\cos\phi. \tag{7.134}$$

Using (7.134) and introducing the normalized voltage $V = V_L/V_D/\sqrt{2}$ yields

$$\eta(V) = \frac{V^2}{1-(1-V^2)\,\eta_D\eta_R}\eta_D. \tag{7.135}$$

This equation simplifies to $\eta(V) = V^2\eta_D$ for the case that no energy recovery is done.

7.5.3 RF Energy Recovery

In this section the properties of RF energy recovery will be derived. The concept is based on reusing the energy in the modulation sidebands for BB PWM operation by employing a variable reflection as depicted in Fig. 7.10. It will be assumed that the BPF is implemented as a parallel resonator. The resulting equations in terms of efficiency and output voltage when using a series resonator are the same and, therefore, only the derivation for the parallel resonator will be provided.

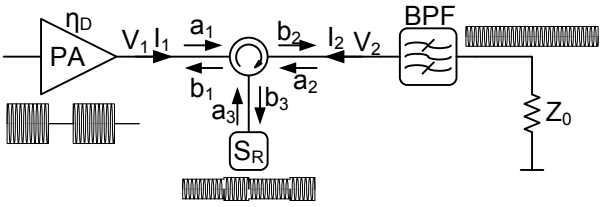


Figure 7.10: RF energy recovery.

Setting up the relationship between PA and load delivers

$$b_1 = a_2 S_R;\ b_2 = a_1, \tag{7.136}$$

with

$$b = \frac{V - Z_0 I}{2\sqrt{Z_0}};\ a = \frac{V + Z_0 I}{2\sqrt{Z_0}}, \tag{7.137}$$

Combining both equations results in

$$V_1 + Z_0 I_1 = V_2 - Z_0 I_2, \tag{7.138}$$

$$V_1 - Z_0 I_1 = (V_2 + Z_0 I_2) S_R. \tag{7.139}$$

Taking this relation for both periods into account results in two equations for the ON period

$$V_1^{ON} + Z_0 I_1^{ON} = V_2^{ON} - Z_0 I_2^{ON}, \tag{7.140}$$

$$V_1^{ON} - Z_0 I_1^{ON} = (V_2^{ON} + Z_0 I_2^{ON}) S_R^{ON} \tag{7.141}$$

and two equations for the OFF period

$$V_1^{OFF} + Z_0 I_1^{OFF} = V_2^{OFF} - Z_0 I_2^{OFF}, \tag{7.142}$$

$$V_1^{OFF} - Z_0 I_1^{OFF} = (V_2^{OFF} + Z_0 I_2^{OFF}) S_R^{OFF}. \tag{7.143}$$

7.5.3.1 Energy Recovery OFF Period

Now, energy recovery during the OFF period under the assumption that a parallel resonator is used will be considered. Setting up the equations for the ON period and assuming $V_1^{ON} = 1$ and $V_2^{ON} = V_2^{OFF} = V_L$ due to the parallel resonator and $S_R^{ON} = 0$ results in the following equations

$$1 + Z_0 I_1^{ON} = V_L - Z_0 I_2^{ON}, \tag{7.144}$$

$$1 - Z_0 I_1^{ON} = (V_L + Z_0 I_2^{ON}) 0. \tag{7.145}$$

These can be resolved to deliver

$$I_1^{ON} = \frac{1}{Z_0}, \tag{7.146}$$

$$I_2^{ON} = \frac{V_L - 2}{Z_0}. \tag{7.147}$$

Setting up the equations for the OFF period considering that the PA provides an open circuit and thus $I_1^{OFF} = 0$ yields

$$V_1^{OFF} + Z_0 0 = V_L - Z_0 I_2^{OFF}, \tag{7.148}$$

$$V_1^{OFF} - Z_0 0 = (V_2 L + Z_0 I_2^{OFF}) S_R^{OFF}. \tag{7.149}$$

As no energy is lost during the OFF period and thus $I_2^{OFF} = 0$ (7.148) simplifies to

$$V_1^{OFF} = V_L. \tag{7.150}$$

Inserting (7.150) into (7.149) delivers

$$V_L = (V_L + Z_0 0) S_R^{OFF};\ S_R^{OFF} = 1. \tag{7.151}$$

Considering the following relation for the parallel resonator

$$\frac{-V_L}{Z_0} = I_2^{ON} d + I_2^{OFF} (1 - d) \tag{7.152}$$

and inserting (7.146) and (7.147) delivers

$$\frac{-V_L}{Z_0} = \frac{V_L - 2}{Z_0} d + 0(1 - d). \tag{7.153}$$

Resolving for V_L yields

$$V_L = \frac{2d}{1 + d}. \tag{7.154}$$

The input power can be calculated by

$$P_1 = \frac{V_1^{ON} I_1^{ON}}{2} \frac{d}{1} = \frac{1}{2Z_0} d \tag{7.155}$$

and the output power by using

$$P_L = \frac{V_L^2}{2Z_0} = \frac{4d^2}{2Z_0(1+d)^2}. \tag{7.156}$$

The corresponding coding efficiency is given by

$$\eta_C(d) = \frac{P_L}{P_1} = \frac{4d}{(1+d)^2}. \tag{7.157}$$

Resolving with respect to output voltage V_L delivers

$$\eta_C(V_L) = V_L(2 - V_L). \tag{7.158}$$

The resulting PA efficiency is determined by the coding efficiency $\eta_C(V_L)$ and the drain efficiency $\eta_D(V_L)$ and is given by

$$\eta(V_L) = \eta_C(V_L)\eta_D(V_L) = V_L(2 - V_L)\,\eta_D(V_L). \tag{7.159}$$

7.5.3.2 Energy Recovery ON Period

Now the same calculation is done for energy recovery during the OFF period. Setting up the current and voltage relationship (7.138) and (7.139) for the ON period yields

$$1 + Z_0 I_1^{ON} = V_L - Z_0 I_2^{ON}, \tag{7.160}$$

$$1 - Z_0 I_1^{ON} = (V_L + Z_0 I_2^{ON}) S_R^{ON}. \tag{7.161}$$

Resolving both equations for $Z_0 I_1^{ON}$ delivers

$$Z_0 I_1^{ON} = V_L - Z_0 I_2^{ON} - 1, \tag{7.162}$$

$$Z_0 I_1^{ON} = -V_L S_R^{ON} - Z_0 I_2^{ON} S_R^{ON} + 1. \tag{7.163}$$

Setting them equal results in

$$V_L - Z_0 I_2^{ON} - 1 = -V_L S_R^{ON} - Z_0 I_2^{ON} S_R^{ON} + 1. \tag{7.164}$$

The equations for the OFF period considering $V_1^{OFF} = 0$ and $S_R^{OFF} = 0$ are defined as

$$0 + Z_0 I_1^{ON} = V_L - Z_0 I_2^{ON} \tag{7.165}$$

$$0 - Z_0 I_1^{ON} = (V_L + Z_0 I_2^{ON}) 0. \tag{7.166}$$

This results in

$$I_1^{OFF} = 0;\ I_2^{OFF} = \frac{V_L}{Z_0}. \tag{7.167}$$

Using this and the condition for the parallel resonator current (7.152) delivers

$$I_2^{ON} = \frac{V_L}{Z_0} \left(1 - \frac{2}{d}\right). \tag{7.168}$$

Inserting this into (7.164) and resolving for V_L yields

$$V_L = \frac{1}{S_R^{ON} + \frac{1-S_R^{ON}}{d}}. \tag{7.169}$$

If $S_R^{ON} = 1$ the resulting output voltage does not depend on the duty cycle anymore and thus

$$S_R^{ON} = -1. \tag{7.170}$$

Resolving (7.169) considering $S_R^{ON} = -1$ results in

$$V_L(d) = \frac{d}{2-d}. \tag{7.171}$$

Taking (7.168) and (7.171) into account and inserting into (7.162) yields

$$I_1^{ON} = \frac{1}{Z_0}\frac{d}{2-d}. \tag{7.172}$$

The input power can can be calculated using

$$P_1 = \frac{V_1^{ON} I_1^{ON}}{2}\frac{d}{1} = \frac{d^2}{2Z_0(2-d)}. \tag{7.173}$$

The output power is given by

$$P_L = \frac{V_L^2}{2Z_0} = \frac{d^2}{2Z_0(2-d)^2}. \tag{7.174}$$

The coding efficiency results in

$$\eta_C(d) = \frac{P_L}{P_1} = \frac{1}{2-d} \tag{7.175}$$

and resolving in terms of output voltage V_L delivers

$$\eta_C(V_L) = \frac{1+V_L}{2}. \tag{7.176}$$

Considering the whole PA efficiency results in

$$\eta(V_L) = \eta_C(V_L)\eta_D(V_L) = \frac{1+V_L}{2}\eta_d(V_L). \tag{7.177}$$

7.5.3.3 Full Energy Recovery

Finally the properties of full energy recovery during both periods are considered. Setting up the equations for the ON period considering $V_1^{ON} = 1$ and (7.170) results in

$$1 + Z_0 I_1^{ON} = V_L - Z_0 I_2^{ON}, \tag{7.178}$$

$$1 - Z_0 I_1^{ON} = -V_L - Z_0 I_2^{ON}. \tag{7.179}$$

Resolving both equations for $Z_0 I_1^{ON}$ yields

$$Z_0 I_1^{ON} = V_L - Z_0 I_2^{ON} - 1, \tag{7.180}$$

$$Z_0 I_1^{ON} = +V_L + Z_0 I_2^{ON} + 1. \tag{7.181}$$

Setting (7.180) and (7.180) equal and resolving for I_2^{ON} delivers

$$I_2^{ON} = \frac{-1}{Z_0}. \tag{7.182}$$

Setting up the equations for the OFF period considering (7.151) and $I_1^{OFF} = 0$ (open circuit) gives

$$V_1^{OFF} = V_L - Z_0 I_2^{OFF}, \tag{7.183}$$

$$V_1^{OFF} = V_L + Z_0 I_2^{OFF}. \tag{7.184}$$

Resolving for I_2^{OFF} yields

$$I_2^{OFF} = 0 \tag{7.185}$$

and thus

$$V_1^{OFF} = V_L. \tag{7.186}$$

Considering (7.182), (7.185) and the parallel resonator (7.152) results in

$$V_L = d. \tag{7.187}$$

Using this and inserting into (7.180) along with (7.182) and resolving for I_1^{ON} yields

$$I_1^{ON} = \frac{d}{Z0}. \tag{7.188}$$

The input power can be calculated using

$$P_1 = \frac{V_1^{ON} I_1^{ON}}{2} \frac{d}{1} = \frac{d^2}{2Z_0} \tag{7.189}$$

and the output power by using

$$P_L = \frac{V_L^2}{2Z_0} = \frac{d^2}{2Z_0}. \tag{7.190}$$

The coding efficiency results in

$$\eta_C(d) = \frac{P_L}{P_1} = 1. \tag{7.191}$$

Thus the PA efficiency is determined only by the drain efficiency η_d.

$$\eta(V_L) = \eta_D(V_L) \tag{7.192}$$

7.5.4 DC BPSK Energy Recovery

In this section the properties of BPSK operation with and without energy recovery will be derived. First BSPK operation with a broadband load (isolator + filter) will be derived. The corresponding block diagram is depicted in Fig. 7.11.

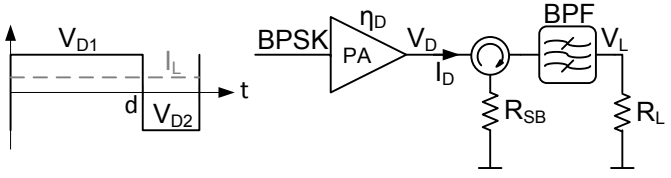


Figure 7.11: BPSK isolated operation.

The normalized drain voltages during the first period V_{D1} and during the second period V_{D2} due to the BPSK coding are given by

$$V_{D1} = 1;\ V_{D2} = -1, \tag{7.193}$$

which results in

$$V_L = V_{D1}d + V_{D2}(1-d) = 2d - 1. \tag{7.194}$$

Resolving (7.194) for the duty cycle d delivers

$$d = \frac{1 + V_L}{2}. \tag{7.195}$$

The output power at the load can be calculated by

$$P_L = \frac{V_L^2}{2R_L}. \tag{7.196}$$

The input power is constant due to the constant envelope in combination with the broadband load and is given by

$$P_D = \frac{V_D^2}{2R_L} = \frac{1}{2R_L}. \tag{7.197}$$

The resulting efficiency is defined by

$$\eta = \frac{P_L}{P_D}\eta_D = V_L^2\eta_D. \tag{7.198}$$

Due to the conservation of energy the power in the sideband termination resistor R_{SB} can be calculated by

$$P_{SB} = P_D - P_L = \frac{1 - V_L^2}{2R_L}. \tag{7.199}$$

In this section DC energy recovery within one BB BPSK period will be discussed. The block diagram is given in Fig. 7.12. A biphase coding is applied and the PA is operated

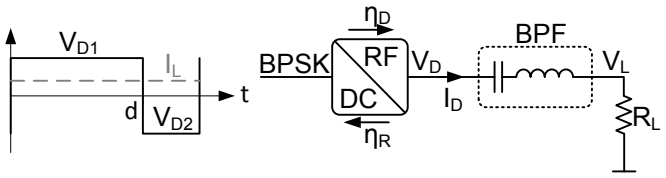


Figure 7.12: DC BPSK energy recovery.

regularly in one period and acts as a rectifier in the other one. The normalized drain voltage is the same as for the broadband load. Also the resulting load voltage is the same and defined by (7.194). The input current I_D differs from the broadband load operation and is defined by

$$I_D = \frac{V_L}{R_L} = \frac{2d-1}{R_L}. \tag{7.200}$$

The input power for both periods is given by

$$P_{D1} = \frac{V_{D1}I_D d}{2};\ P_{D2} = \frac{V_{D2}I_D(1-d)}{2}. \tag{7.201}$$

Considering (7.195) and (7.200) yields

$$P_{D1} = \frac{V_L + V_L^2}{4R_L};\ P_{D2} = \frac{-V_L + V_L^2}{4R_L}. \tag{7.202}$$

The resulting DC power consumptions are defined as

$$P_{DC1} = \begin{cases} P_{D1}/\eta_D & P_{D1} > 0 \\ P_{D1}\eta_R & \text{else} \end{cases}, \; P_{DC2} = \begin{cases} P_{D2}/\eta_D & P_{D2} > 0 \\ P_{D2}\eta_R & \text{else} \end{cases}. \tag{7.203}$$

Calculating the total DC power considering (7.203) and only positive load voltage V_L results in

$$P_{DC} = \frac{P_{D1}}{\eta_D} + P_{D2}\eta_r. \tag{7.204}$$

The resulting efficiency considering (7.196) and (7.202) is given by

$$\eta = \frac{P_L}{P_{DC}} = \frac{P_L}{P_{D1} + P_{D2}\eta_R\eta_D}\eta_D = \frac{2V_L}{1 + V_L - (1 - V_L)\eta_R\eta_D}\eta_D. \tag{7.205}$$

7.6 Chireix

In this section the general properties of the Chireix combiner for arbitrary load voltage and phase relationships will be derived.

7.6.1 Quarterwave Chireix Outphasing

In Fig. 7.13 a general outphasing combiner is depicted.

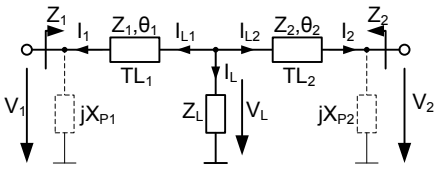


Figure 7.13: Chireix combiner with shunt reactance.

The relation for the currents at the summation point can be defined as

$$I_L = -I_{L1} - I_{L2}. \tag{7.206}$$

Furthermore the load voltage V_L results in

$$V_L = I_L Z_L = -(I_{L1} + I_{L2})Z_L. \tag{7.207}$$

The relations for the transmission lines with their characteristic impedance Z_1, Z_2 and electrical length θ_1, θ_2 are defined by

$$V_L = V_1\cos(\theta_1) + jZ_1 I_1 \sin(\theta_1) \tag{7.208}$$

$$I_{L1} = jV_1\frac{1}{Z_1}\sin(\theta_1) + I_1\cos(\theta_1) \tag{7.209}$$

$$V_L = V_2\cos(\theta_2) + jZ_2 I_2 \sin(\theta_2) \tag{7.210}$$

$$I_{L2} = jV_2\frac{1}{Z_2}\sin(\theta_2) + I_2\cos(\theta_2). \tag{7.211}$$

Setting (7.208) and (7.210) equal and resolving for I_2 delivers

$$I_2 = -j\frac{V_1\cos(\theta_1) - V_2\cos(\theta_2) + jZ_1 I_1\sin(\theta_1)}{Z_2\sin(\theta_2)}. \tag{7.212}$$

Inserting (7.209) and (7.211) into (7.207) yields

$$-V_L = jV_1\frac{Z_L}{Z_1}\sin(\theta_1) + I_1 Z_L\cos(\theta_1) + jV_2\frac{Z_L}{Z_2}\sin(\theta_1) + I_2 Z_L\cos(\theta_2). \tag{7.213}$$

Considering (7.212) results in

$$\begin{aligned} -V_L = I_1 Z_L\left(\cos(\theta_1) + \frac{Z_1\cos(\theta_2)}{Z_2\sin(\theta_2)}\sin(\theta_1)\right) + jV_2\frac{Z_L}{Z_2\sin(\theta_2)} \\ + V_1\left(j\frac{Z_L}{Z_1}\sin(\theta_1) - j\frac{Z_L\cos(\theta_2)}{Z_2\sin(\theta_2)}\cos(\theta_1)\right). \end{aligned} \tag{7.214}$$

Setting (7.208) and (7.214) equal delivers

$$\begin{aligned} -I_1\left(jZ_1\sin(\theta_1) + Z_L\cos(\theta_1) + Z_L\frac{Z_1\cos(\theta_2)}{Z_2\sin(\theta_2)}\sin(\theta_1)\right) \\ = V_1\left(j\frac{Z_L}{Z_1}\sin(\theta_1) - j\frac{Z_L\cos(\theta_2)}{Z_2\sin(\theta_2)}\cos(\theta_1) + \cos(\theta_1)\right) + jV_2\frac{Z_L}{Z_2\sin(\theta_2)} \end{aligned} \tag{7.215}$$

Resolving for $-I_1$ and considering $Z_1 = -V_1/I_1$ yields

$$Z_1 = \frac{V_1\left(Z_L\cos(\theta_1) + \left(jZ_1 + Z_L\frac{Z_1}{Z_2}\cot(\theta_2)\right)\sin(\theta_1)\right)}{V_1\left(j\frac{Z_L}{Z_1}\sin(\theta_1) + \left(1 - j\frac{Z_L}{Z_2}\cot(\theta_2)\right)\cos(\theta_1)\right) + jV_2\frac{Z_L}{Z_2\sin(\theta_2)}}. \tag{7.216}$$

Doing the same for the second branch gives

$$Z_2 = \frac{V_2\left(Z_L\cos(\theta_2) + \left(jZ_2 + Z_L\frac{Z_2}{Z_1}\cot(\theta_1)\right)\sin(\theta_2)\right)}{V_2\left(j\frac{Z_L}{Z_2}\sin(\theta_2) + \left(1 - j\frac{Z_L}{Z_1}\cot(\theta_1)\right)\cos(\theta_2)\right) + jV_1\frac{Z_L}{Z_1\sin(\theta_1)}}. \tag{7.217}$$

Considering equal line impedances $Z_1 = Z_2 = F\,Z_L$ and implying quarterwave lines $\theta_1 = \pi/2, \theta_2 = \pi/2$ and a real load $Z_L = R_L$ results in

$$Z_1 = \frac{F^2 R_L}{1 + \frac{V_2}{V_1}},\ Z_2 = \frac{F^2 R_L}{1 + \frac{V_1}{V_2}}. \tag{7.218}$$

When considering $V_1 = e^{j\phi}$ and $V_2 = e^{-j\phi}$, (7.218) simplifies to

$$Z_{1,2} = R_L\frac{F^2}{2}\left(1 \pm j\tan(\phi)\right). \tag{7.219}$$

For F = 2 the equation further reduces to

$$Z_{1,2} = 2R_L\left(1 \pm j\tan(\phi)\right). \tag{7.220}$$

The parallel resistance is given by

$$R_1 = R_2 = \frac{F^2}{2}R_L\left(1 + \tan^2(\phi)\right). \tag{7.221}$$

The output power can be calculated by

$$P = P_1 + P_2 = \frac{V_1^2}{2R_1} + \frac{V_2^2}{2R_2} = \frac{1}{F^2 R_L\left(1 + \tan^2(\phi)\right)} \tag{7.222}$$

and the power back off ratio p can be calculated by

$$p = \frac{P_{BO}}{P_0} = \frac{\frac{1}{F^2 R_L (1+\tan^2(\phi_{BO}))}}{\frac{1}{F^2 R_L (1+\tan^2(0))}} = \frac{1}{1+\tan^2(\phi_{BO})} = \cos^2(\phi_{BO}). \tag{7.223}$$

Rearranging to get the back off outphasing angle $\tan(\phi_{BO})$ results in

$$\tan(\phi_{BO}) = \sqrt{\frac{1-p}{p}}. \tag{7.224}$$

The parallel reactance at the back off level can be calculated by

$$jX_1(\phi_{BO}) = jF^2 R_L \left(\tan(\phi_{BO}) + \frac{1}{\tan(\phi_{BO})}\right). \tag{7.225}$$

Inserting (7.224) results in

$$jX_1(p) = j\frac{F^2}{2} R_L \left(\sqrt{\frac{1-p}{p}} + \sqrt{\frac{p}{1-p}}\right) = j\frac{F^2 R_L}{2\sqrt{p-p^2}}. \tag{7.226}$$

To compensate this reactance a parallel reactance of the opposite sign is added. These reactances are also known as the Chireix reactances, respectively Chireix combiner. The required parallel compensation reactances result in

$$jX_{P1} = -jX_1(\phi_{BO});\ jX_{P2} = jX_1(\phi_{BO}). \tag{7.227}$$

The final Chireix input impedances Z_1 and Z_2 simplify to a parallel circuit and are given by

$$Z_1 = \frac{F^2}{2} R_L \frac{(\tan(\phi) - j)}{\sqrt{p-p^2}\,(1 + j\tan(\phi)) - j}, \tag{7.228}$$

$$Z_2 = \frac{F^2}{2} R_L \frac{(\tan(\phi) + j)}{\sqrt{p-p^2}\,(1 - j\tan(\phi)) + j}. \tag{7.229}$$

For zero outphasing angle $\phi = 0$ the input impedances Z_1^C and Z_2^C simplify to

$$Z_1^C = \frac{F^2 R_L}{2 + j2\sqrt{p-p^2}};\ Z_2^C = \frac{F^2 R_L}{2 - j2\sqrt{p-p^2}}. \tag{7.230}$$

7.6.2 Asymmetric Chireix Outphasing

A Chireix combiner can also be built by using transmission lines with different lengths according to $\theta_1 = \pi/2 + \theta_c$ and $\theta_2 = \pi/2 - \theta_c$, as depicted in Fig. 7.14.

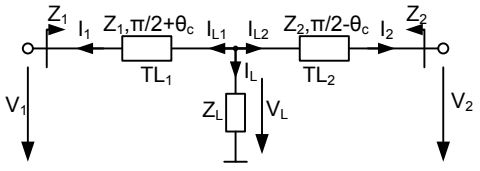


Figure 7.14: Asymmetric transmission line Chireix combiner.

Considering transmission lines with the same characteristic impedance defined by $Z_1 = Z_2 = F_c\,Z_L$ and a real load $Z_L = R_L$ results in

$$Z_1 = R_L \frac{\cos(\theta_1) + (jF_c + \cot(\theta_2))\sin(\theta_1)}{\left(j\frac{1}{F_c}\sin(\theta_1) + \left(1 - j\frac{1}{F_c}\cot(\theta_2)\right)\cos(\theta_1)\right) + j\frac{V_2}{V_1}\frac{1}{F_c\sin(\theta_2)}}. \tag{7.231}$$

Simplification results in

$$Z_1 = R_L \frac{F_c^2\cos^2(\theta_c)}{1 + j\frac{F_c}{2}\sin(2\theta_c) + \frac{V_2}{V_1}};\; Z_2 = R_L \frac{F_c^2\cos^2(\theta_c)}{1 - j\frac{F_c}{2}\sin(2\theta_c) + \frac{V_1}{V_2}}. \tag{7.232}$$

Considering $V_1 = e^{j\phi}, V_2 = e^{-j\phi}$ delivers

$$Z_1 = R_L \frac{F_c^2\cos^2(\theta_c)\left(1 + \cos(2\phi) - j\left(\frac{F_c}{2}\sin(2\theta_c) - \sin(2\phi)\right)\right)}{2 + 2\cos(2\phi) + \frac{F_c^2}{4}\sin^2(2\theta_c) - F_c\sin(2\theta_c)\sin(2\phi)}, \tag{7.233}$$

$$Z_2 = R_L \frac{F_c^2\cos^2(\theta_c)\left(1 + \cos(2\phi) + j\left(\frac{F_c}{2}\sin(2\theta_c) - \sin(2\phi)\right)\right)}{2 + 2\cos(2\phi) + \frac{F_c^2}{4}\sin^2(2\theta_c) - F_c\sin(2\theta_c)\sin(2\phi)}. \tag{7.234}$$

For zero outphasing angle $\phi = 0$ the equations simplify to

$$Z_1 = R_L F_c^2 \frac{\cos^2(\theta_c)}{4 + \frac{F_c^2}{4}\sin^2(2\theta_c)}\left(2 - j\frac{F_c}{2}\sin(2\theta_c)\right). \tag{7.235}$$

To get the same impedances as for the conventional approach with parallel compensation reactances the line impedance $F_c\,R_L$ and the Chireix compensation angle θ_c can be calculated by setting (7.230) and (7.235) equal, which delivers the following two equations

$$\frac{F_c^2\cos^2(\theta_c)}{4 + \frac{F_c^2}{4}\sin^2(2\theta_c)} = \frac{F^2}{4(p - p^2 + 1)}, \tag{7.236}$$

$$\frac{F_c^2\cos^2(\theta_c)}{4 + \frac{F_c^2}{4}\sin^2(2\theta_c)}\left(\frac{F_c}{2}\sin(2\theta_c)\right) = \frac{F^2}{2}\frac{\sqrt{p - p^2}}{p - p^2 + 1}. \tag{7.237}$$

Inserting (7.236) into (7.237) and resolving for θ_c yields

$$\sin(2\theta_c) = \frac{4}{F_c}\sqrt{p - p^2}. \tag{7.238}$$

Considering (7.236) and (7.238) delivers

$$F_c = \frac{F}{\cos(\theta_c)}. \tag{7.239}$$

Inserting this into (7.238) results in

$$\sin(\theta_c) = \frac{2}{F}\sqrt{p - p^2}. \tag{7.240}$$

Inserting now (7.240) into (7.239) yields the design equation for F_c

$$F_c = \frac{F^2}{\sqrt{F^2 - 4\,(p - p^2)}}. \tag{7.241}$$

For $F = 2$ the equation simplifies to

$$F_c = \frac{2}{\sqrt{1 - p + p^2}}. \tag{7.242}$$

7.6.3 Error Analysis

Any imperfection in the supply voltages and/or matching network makes it impossible to achieve low output voltages. The load voltage is defined by (7.207) and thus for zero load voltage the following condition has to be satisfied

$$V_L = -(I_{L1} + I_{L2})Z_L = 0. \tag{7.243}$$

Considering $I_{L1} = I_{M1}e^{j\phi}, I_{L2} = I_{M2}e^{-j\phi}$ and defining $I_{M2} = I_{M1} + \Delta I$ results in

$$V_L = -(2I_{M1}\cos(\phi) + \Delta I e^{-j\phi})Z_L. \tag{7.244}$$

The first part of the equation $I_{M1}\cos(\phi)$ will become zero for an angle of $\phi = \pi/2$, but the second part has a constant amplitude and only changes in phase. Therefore, the resulting minimum and maximum amplitudes are given by

$$V_{L\,MIN} = -j\Delta I\, Z_L;\ \phi = \frac{\pi}{2}, \tag{7.245}$$

$$V_{L\,MAX} = -(2I_{M1} + \Delta I)\, Z_L;\ \phi = 0. \tag{7.246}$$

Normalizing the minimum load voltage by the maximum load voltage delivers

$$V_{MIN} = \frac{V_{L\,MIN}}{V_{L\,MAX}} = j\frac{\Delta I}{2I_{M1} + \Delta I} = j\frac{I_{M2} - I_{M1}}{I_{M1} + I_{M2}}. \tag{7.247}$$

The remaining load voltage phasor is orthogonal to the phasor controlled by the outphasing and can therefore not easily be reduced. Considering an outphasing combiner using two equal quarter wave lines results in the following requirement

$$V_{MIN} = j\frac{\Delta V}{2V_{M1} + \Delta V} \approx j\frac{\Delta V}{2V}. \tag{7.248}$$

The resulting dynamic range for supply voltage mismatch can be approximated by

$$DR = 20\log10\left(\frac{\Delta V}{2V}\right). \tag{7.249}$$

The current mismatch can also be caused by a mismatch of the transmission line impedance or by a phase difference, which will always be the case due to manufacturing tolerances. The impact of different transmission line impedances can be expressed by

$$V_{MIN} = j\frac{Z_{L1} - Z_{L2}}{Z_{L1} + Z_{L2}} = j\frac{\Delta Z}{2Z + \Delta Z} \approx j\frac{\Delta Z}{2Z}, \tag{7.250}$$

$$DR = 20\log10\left(\frac{\Delta Z}{2Z}\right). \tag{7.251}$$

Thus for a single frequency an output matching imperfection might be compensated by modifying the supply voltages accordingly, which is however not desirable in practice. Another possibility is to use a three (or more) way outphasing system. The only constraint for reaching zero output power is the requirement that the sum of the magnitudes of the smallest vectors is larger than the magnitude of the largest vector.

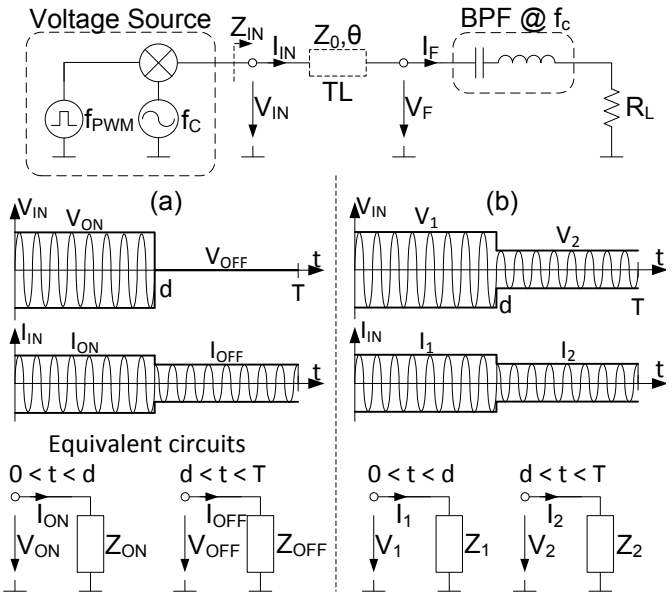


Figure 7.15: Voltage and current waveforms and equivalent circuit for (a) full and (b) partial PWM modulation.

7.7 Equivalent Load Impedance

7.7.1 Full PWM Modulation

In this section the equivalent load impedance for PWM modulation with full modulation depth (between zero and one) will be derived. For the derivation a series resonator connected via a transmission line with a characteristic impedance Z_0 and electrical length θ, as depicted in Fig. 7.15, will be assumed. Later the calculation will be expanded to a general case, without any restriction on circuit topology.

For the derivations it is assumed that the filter has an infinite Q and the ratio f_{PWM}/f_c approaches zero. The ratio of average voltage and current over one cycle is equal to the impedance at carrier frequency

$$Z_c = Z_{IN}(\omega_c) = \frac{V(\omega_c)}{I(\omega_c)}. \tag{7.252}$$

The average voltage $V(\omega_c)$ relates to the duty cycle d as $V(\omega_c) = V_{ON}d$, where the average current is defined by

$$I(\omega_c) = I_{ON}d + I_{OFF}(1-d). \tag{7.253}$$

This results in an impedance at carrier frequency given by

$$Z_c = \frac{V_{ON}d}{I_{ON}d + I_{OFF}(1-d)}. \tag{7.254}$$

The lossless transmission line TL with the properties Z_0 and θ delivers 2 equations for each condition (ON and OFF).

$$V_{ON} = V_{F,ON}\cos(\theta) + jI_{F,ON}Z_0\sin(\theta) \tag{7.255}$$

$$I_{ON} = j\frac{1}{Z_0}V_{F,ON}\sin(\theta) + I_{F,ON}\cos(\theta) \tag{7.256}$$

$$V_{OFF} = V_{F,OFF}\cos(\theta) + jI_{F,OFF}Z_0\sin(\theta) \tag{7.257}$$

$$I_{OFF} = j\frac{1}{Z_0}V_{F,OFF}\sin(\theta) + I_{F,OFF}\cos(\theta) \tag{7.258}$$

Solving (7.255) for $V_{F,ON}$ assuming the normalized voltage V_{ON} being 1 yields

$$V_{F,ON} = \frac{1 - jI_{F,ON}Z_0\sin(\theta)}{\cos(\theta)}. \tag{7.259}$$

Combining this with (7.256) and solving for $I_{F,ON}$ gives

$$I_{F,ON} = I_{ON}\cos(\theta) - j\frac{1}{Z_0}\sin(\theta). \tag{7.260}$$

Resolving (7.257), taking $V_{OFF} = 0$ into account, results in

$$V_{F,OFF} = -jZ_0\frac{\sin(\theta)}{\cos(\theta)}I_{F,OFF}. \tag{7.261}$$

Based on the same assumptions (7.258) is given by

$$I_{F,OFF} = I_{OFF}\cos(\theta). \tag{7.262}$$

The current through the series filter is continuous and thus $I_{F,ON} = I_{F,OFF}$. This property allows solving for I_{OFF}

$$I_{OFF} = I_{ON} - j\frac{\sin(\theta)}{Z_0\cos(\theta)}. \tag{7.263}$$

Now the impedance Z_S is introduced, which can be seen as the input impedance at the carrier frequency, if the series resonator provides an open circuit (low duty cycles). In other words the impedance Z_S also marks the intersection of the unit circle of the smith chart and the symmetry axis of the resonance locus. Its graphical definition is depicted in Fig. 7.16 and its value is given by

$$Z_S = -jZ_0\cot(\theta). \tag{7.264}$$

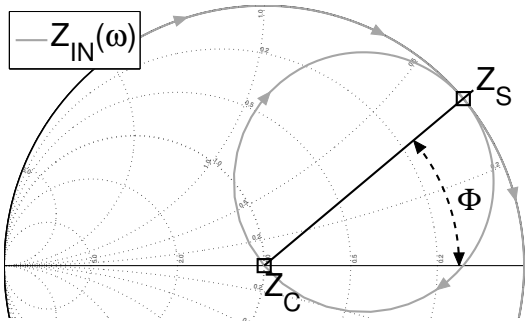


Figure 7.16: Definition of Z_C and Z_S.

The phase angle (θ) relates to the detuning angle from the series resonator locus (Φ) as $\Phi = 180\,^\circ - \theta$. Based on (7.264), (7.263) can be rearranged to

$$I_{OFF} = I_{ON} - \frac{1}{Z_S}. \tag{7.265}$$

Extracting I_{ON} considering (7.254) and $V_{ON} = 1$ yields

$$I_{ON} = \frac{d}{Z_C} + \frac{1-d}{Z_S}. \tag{7.266}$$

Introducing the weighted load impedance

$$Z_P = \frac{Z_C}{d} \tag{7.267}$$

and defining the weighted reactance

$$Z_{PR} = \frac{Z_S}{1-d} \tag{7.268}$$

delivers

$$I_{ON} = \frac{1}{Z_P} + \frac{1}{Z_{PR}}. \tag{7.269}$$

The equivalent load impedance Z_{ON} during the ON period can be calculated by

$$Z_{ON} = \frac{V_{ON}}{I_{ON}} = \frac{Z_P Z_{PR}}{Z_P + Z_{PR}}, \tag{7.270}$$

which is a simple parallel circuit of the weighted load impedance Z_P and the weighted reactance Z_{PR}.

The current during the OFF period can be calculated considering (7.263) and (7.264) and results in

$$I_{OFF} = d\left(\frac{1}{Z_C} - \frac{1}{Z_S}\right). \tag{7.271}$$

The equivalent load impedance during the OFF period depends on the voltage as

$$Z_{OFF} = \frac{V_{OFF}}{I_{OFF}} = 0, \tag{7.272}$$

as the input voltage during the OFF period is zero.

7.7.2 Partial PWM Modulation

In the previous section the load impedances for a fully PWM modulated signal have been derived. In this section the equivalent load impedances of a constant signal (V_2) also during the OFF period imposed by a PWM modulated signal ($V_1 - V_2$) will be calculated.

In Fig. 7.15(b) the definition of voltages and currents for this operation are depicted. To simplify the calculations the normalized reference voltage $V_{REF} = V_2/V_1$ is introduced. The constant part corresponds to V_{REF} and the modulated part to $1 - V_{REF}$. It is important to note that V_1 and V_2 and also V_{REF} are complex numbers in general.

The load current during the first period depends on the constant part (V_{REF}/Z_C) and on a modulated part (7.269).

$$I_1 = \frac{V_{REF}}{Z_C} + \frac{1 - V_{REF}}{Z_{ON}} \tag{7.273}$$

This results in

$$Z_1 = \frac{V_1}{I_1} = \frac{Z_{ON} Z_C}{Z_{ON} V_{REF} + Z_C(1 - V_{REF})} \tag{7.274}$$

for the impedance during the first period. Similarly the current during the second period can be calculated by

$$I_2 = \frac{1 - V_{REF}}{Z_C} + I_{OFF}(1 - V_{REF}). \tag{7.275}$$

The resulting load impedance Z_2 during the second period is given by

$$Z_2 = \frac{V_2}{I_2} = \frac{V_{REF}}{\frac{V_{REF}}{Z_C} + \left(\frac{1}{Z_C} - \frac{1}{Z_S}\right) d\,(1 - V_{REF})} \tag{7.276}$$

7.8 Power Loss Band Pass Filters

In this section the insertion loss of band pass filters with respect to the loaded/unloaded Q factor will be derived. The basic circuit diagrams of a parallel and a series resonator with losses are provided in Fig. 7.17.

(a) Parallel resonator (b) Series resonator

Figure 7.17: Losses in band pass filters.

The internal Q-factor of the parallel resonator depicted in Fig. 7.17(a) can be calculated using

$$Q_0 = R_P\sqrt{\frac{C}{L}}, \tag{7.277}$$

while the external Q-factor Q_L also depends on the load resistor R_L and is given by

$$Q_L = \frac{R_P R_L}{R_P + R_L}\sqrt{\frac{C}{L}}. \tag{7.278}$$

For the calculation of the efficiency of the resonator the power lost in the parallel resistor R_P and the power fed to the load R_L

$$P_P = \frac{V^2}{R_P},\ P_L = \frac{V^2}{R_L} \tag{7.279}$$

are required. The efficiency can be calculated by

$$\eta_P = \frac{P_L}{P_P + P_L} = \frac{R_P}{R_L + R_P}. \tag{7.280}$$

Resolving (7.277) for the parallel resistor R_P delivers

$$R_P = \frac{Q_0}{\sqrt{\frac{C}{L}}}. \tag{7.281}$$

Inserting this into (7.278) and resolving for R_L results in

$$R_L = \frac{Q_0 Q_L}{\sqrt{\frac{C}{L}}(Q_0 - Q_L)}. \tag{7.282}$$

Using (7.281) and (7.282) to express (7.280) in terms of the loaded Q_L and unloaded Q_0 Q-factor yields

$$\eta_P = 1 - \frac{Q_L}{Q_0}. \tag{7.283}$$

Considering the series circuit in Fig. 7.17(b) the loaded and unloaded Q factor can be expressed as

$$Q_0 = \frac{1}{R_S}\sqrt{\frac{L}{C}} \tag{7.284}$$

and

$$Q_L = \frac{1}{R_S + R_L}\sqrt{\frac{L}{C}}. \tag{7.285}$$

The power in the series resistor and the load can be calculated by

$$P_S = I^2 R_S,\ P_L = I^2 R_L. \tag{7.286}$$

The efficiency is given by

$$\eta_S = \frac{P_L}{P_S + P_L} = \frac{R_L}{R_L + R_S}. \tag{7.287}$$

Resolving (7.284) for R_S delivers

$$R_S = \frac{1}{Q_0}\sqrt{\frac{L}{C}}. \tag{7.288}$$

Taking this into consideration when resolving (7.285) results in

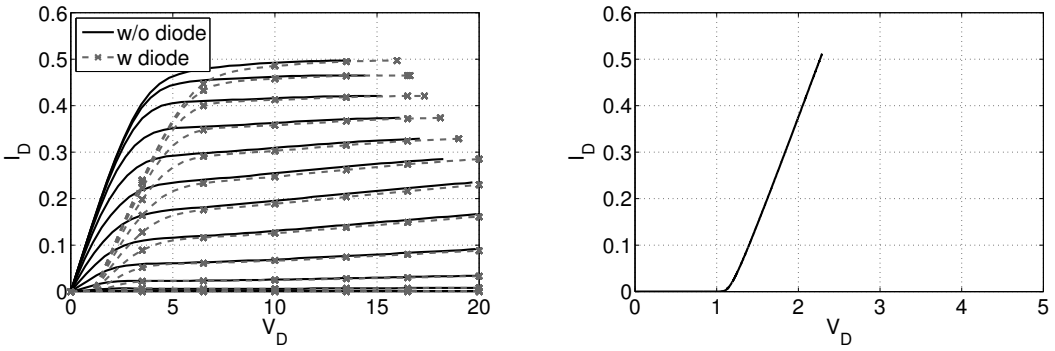
$$R_L = \left(\frac{1}{Q_L} - \frac{1}{Q_0}\right)\sqrt{\frac{L}{C}}. \tag{7.289}$$

Taking (7.288) and (7.289) into account when rearranging (7.280) yields

$$\eta_S = 1 - \frac{Q_L}{Q_0}, \tag{7.290}$$

which is the same result as for the parallel resonator (7.283).

7.9 Transistor Parameters



(a) Transistor (b) Diode

Figure 7.18: GaN transistor and GaN diode IV curves.

7.10 CPE Implementation

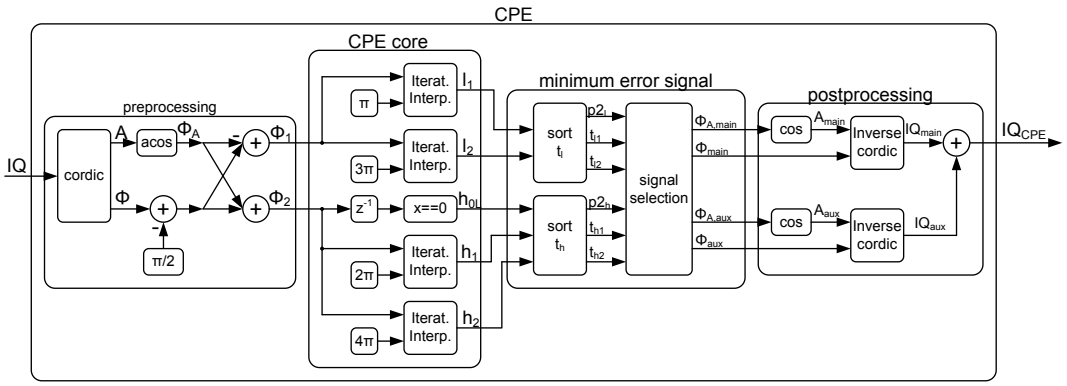


Figure 7.19: CPE overview.

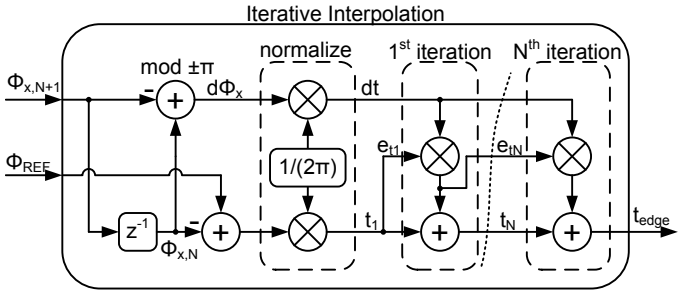


Figure 7.20: CPE iterative interpolation.

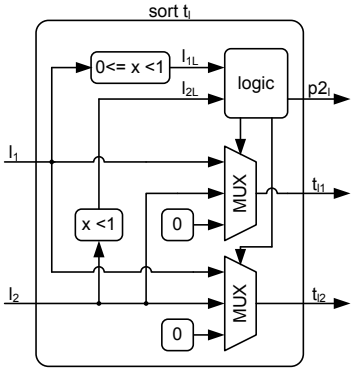
(a) Low edge timing

l_{1L}	l_{0L}	t_{l1}	t_{l2}	p_{2l}
0	0	0	0	0
0	1	0	l_1	0
1	0	l_2	0	0
1	1	l_1	l_2	0

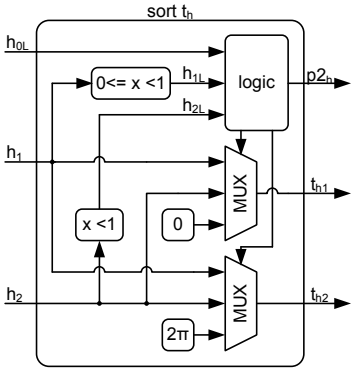
(b) High edge timing

h_{2L}	h_{1L}	h_{0L}	t_{h1}	t_{h2}	p_{2h}
0	0	0	0	2π	0
0	0	1	0	2π	0
0	1	0	h_1	2π	0
0	1	1	0	h_1	1
1	0	0	h_2	2π	0
1	0	1	0	2π	0
1	1	0	h_1	h_2	1
1	1	1	0	h_1	1

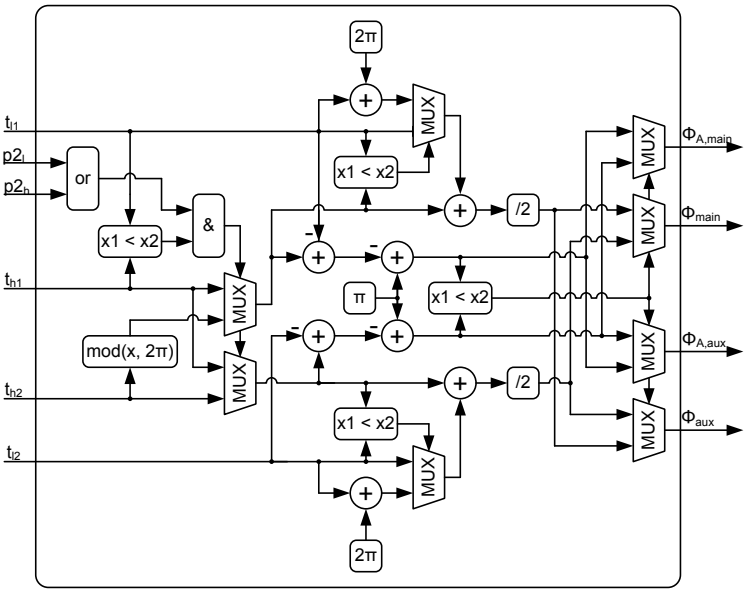
Table 7.1: Logic table edge timing selection.



(a) Low edge timing selection



(b) High edge timing selection



(c) Signal selection

Figure 7.21: CPE minimum error signal selection.

List of Publications

[S1] D. Seebacher, W. Bösch, M. Gadringer, P. Singerl, and C. Schuberth. High Frequency Class-DE Push/Pull Power Amplifier Utilizing a Parallel Compensation Inductance. In *Microelectronic Systems Symposium (MESS)*, May 2014.

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List of Abbreviations

ACLR	Adjacent Channel Leakage Ratio
AM	Amplitude Modulator
AWG	Arbitrary Waveform Generator
BALUN	Balanced Unbalanced
BB PWM	Base Band Pulse Width Modulation
BL	Band Limited
BPF	Band Pass Filter
BPSK	Binary Phase Shift Keying
CO	Carry Over
CORDIC	COordinate Rotation DIgital Computer
CPE	Cross Point Estimation
DAC	Digital to Analog Converter
DE	Drain Efficiency
DPD	Digital Predistortion
ED	Envelope Detector
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
EVM	Error Vector Magnitude
FPGA	Field Programmable Gate Array
IMN	Input Matching Network
LINC	Linear Amplification Using Nonlinear Components
LO	Local Oscillator
LP	Load Pull
LUT	Look Up Table
MMIC	Monolithic Microwave Integrated Circuit
MOD	MODulator

OMN	Output Matching Network
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PCB	Printed Circuit Board
PDF	Probability Density Function
PLL	Phase Locked Loop
PM	Phase Modulator
PS	Pulse Swallowing
PSD	Power Spectral Density
PUF	Power Utilization Factor
PWM	Pulse Width Modulation
RFC	RF Choke
RF PWM	Radio Frequency Pulse Width Modulation
RMS	Root Mean Square
SDR	Software Defined Radio
SMPA	Switched Mode Power Amplifier
TL	Transmission Line
VSA	Vector Signal Analyzer
ZCS	Zero Current Switching
ZOH	Zero Order Hold
ZVS	Zero Voltage Switching