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Capacitive Charge Pump based Low Power Pipeline ADC

MASTER'S THESIS

to achieve the university degree of

Diplom-Ingenieurin

Master's degree programme: Electrical Engineering

submitted to

Graz University of Technology

Supervisor

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Institute of Electronics

AFFIDAVIT

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Abstract

This thesis investigates the low power design for pipelined analog-to-digital converters. The focus is on the multiplying-digital-to-analog converter (MDAC) block, whereof various switched capacitor based principles are presented. It aims to avoid power hungry operational amplifiers which are common in these state of the art solutions. The research question was, whether this is possible while maintaining a high enough gain accuracy for operation without digital calibration. The most important contribution is a new topology which uses only one sampling capacitor per channel. Therefore, the proposed circuit is characterised by a less complex design and requires less area on chip. Additionally, it reaches a better gain accuracy for equally sized sampling capacitors. Simulation results are provided to confirm these statements. The thesis concludes with a discussion of trade-offs between the different presented design approaches.

Kurzfassung

Diese Arbeit untersucht das Design von leistungsarmen *pipeline* analog-zu-digital Umsetzern. Der Fokus liegt dabei auf dem *multiplying-digital-to-analog converter* (MDAC) Block, wovon verschiedene *switched capacitor* basierte Topologien vorgestellt werden. Das Ziel war leistungshungrige Operationsverstärker, welche in bekannten Lösungen häufig Verwendung finden, zu umgehen. Die Frage war, in wie weit dies möglich ist, wenn trotzdem die Verstärkungsgenauigkeit gewahrt bleiben soll, um eine Funktion ohne digitale Kalibrierung zu ermöglichen. Die wichtigste Errungenschaft ist eine neue Topologie, welche nur eine sampling Kapazität pro Kanal aufweist. Die vorgestellte Schaltung ist daher weniger komplex und braucht weniger Platz am Chip. Darüber hinaus erreicht sie bei gleich großen Kapazitätswerten eine bessere Verstärkungsgenauigkeit. Entsprechende Simulationsergebnisse werden bereitgestellt, um diese Behauptungen zu belegen. Die Arbeit schließt mit einer Diskussion der Kompromisse der unterschiedlichen vorgestellten Methoden.

This thesis was carried out at the Institute of Electronics



in cooperation with ams AG



*and is dedicated to my two grandmas,
who never quite knew what I was studying,
but were still proud of me.*

Thanks

On the technical side I want to thank:

Andrzej Gajdardziew, first of all for the topic, which got me hooked on. But more importantly for the numerous inspiring discussions, never killing an idea and his amazing gift to explain.

Mario Manninger, who kept the project alive and made sure that its outcome will hopefully be of use for the ams AG, which was a sponsor of this project.

Peter Söser, for his guidance and providing me a great freedom in the realization of this thesis.

Thanks also goes to John Thompson, who was helping me along with good old-style pen and paper analysis; to Peter Speer, who contributed with his layout skills, but also to Pietro Cipriano, Andreas Haller, Anneliese Moser, Beatriz Olleta, Sudhakar Singamala, Christian Wunderl and Christian Zangl who made coming to work simply more pleasurable.

Further, I want to thank my sister and my mother for their motivation and support. As well as my dad for bringing me in touch with the world of electronics at an early age which was probably why I later even considered studying it.

Finally, a big tribute goes to Andreas Daniel Sinnhofer, who did not only support and encourage me throughout my time at university, but also had to stand me when I was physical at home but my mind still at work.

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1. Introduction

A main goal in the design of consumer products has always been to improve their performance in regards of their primary function and purpose. Yet taking a look at recent developments the challenge is more and more to provide devices able to act in a clever way on their own.

A good example for this clever way of operation are digital cameras equipped with rotary sensors. They are able to save the rotation with which a picture has been taken. This functionality has nothing to do with the basic function of taking high resolution pictures. However, it is convenient for the user when pictures are already rotated correctly when loaded to a PC. Other examples are noise cancellation in head-phones or alert and assistance systems in cars. Robotics and autonomous driving, which are in the focus of research at the moment, carry this idea to the extreme, where devices are meant to operate and take complex decisions with minimal input from the user.

What all these use cases have in common is that devices adjust their behaviour to the circumstances. In order to be responsive to the environment you have to be able to sense it. Since signal processing is almost always done in the digital domain each sensor requires an analog-to-digital converter (ADC). According to this trend the number of ADCs per device can be expected to grow.

The desire to transform analog signals into the digital domain arises from the computational power available there. It turned out that digital signal processing can be done much cheaper than its analog counterpart. As the performance development of ADCs is lacking behind the one of digital circuitry [33] there is need to work on ADC concepts to prevent it of becoming the bottleneck of system performance.

For mobile devices like phones, tablets and smart-watches, but also mobile robots power consumption is essential [18]. However, it also turns out to be an issue for devices where basically enough power is at hand [11]. The reason are packaging costs which diminish when power dissipation and the heating accompanied with it, can be reduced [4]. This explains why power dissipation is a crucial factor in ADC design.

1.1. Structure

The motivation and underlying problem of this thesis is discussed in chapter 2.

Then the first part gives an overview on the fundamentals of the field. The 3rd chapter addresses the used terminology and characteristics of ADC converters and further introduces the non-idealities of an actual ADC. The 4th chapter gives an overview over the basic principles of analog-to-digital conversion and explains the concepts on a common-sense level. Chapter 5 focuses on the pipelined ADC topology, pointing out state of the art approaches and known pitfalls for the design. In chapter 6 some basics design guidelines for switched capacitor circuits are presented.

In the second part new ideas and concepts are discussed. Chapter 7 presents a way to improve the function of the prior art discussed in chapter 5.5.3. A new topology to implement the desired function is introduced in chapter 8. The 9th chapter introduces some ideas for further improvement on a theoretical level. All simulation results comparing and discussing performance are collected in chapter 10. Finally, a conclusion and outlook can be found in chapter 11 where the results of this work are discussed and summarized.

Mathematical derivations for statements made throughout the other chapters are carried out in detail in the appendix A to keep the comprehensibility.

2. Motivation

Pipelined ADCs took over to dominate the area of moderate resolution and conversion speed [25]. Yet they face the problem of high power consumption due to the large number of operational amplifiers (OP-amps).

Different attempts were made to minimize total power consumption of the OP-amps which are part of each stage. There is potential to save power by switching off the OP-amp during idle times. However, since they show long start up times this measure is not suitable for higher frequencies [9]. Likewise, one OP-amp could be used for two stages. Additional switches, long transmission lines and missing resetting are drawbacks of this approach. Another concept tries to reduce the number of stages and with it the number of OP-amps by using multi-bit stages. This shifts the problem to the complexity of the sub-ADC and the sub-digital-to-analog converter (DAC).

Since the main contributor of power consumption is the OP-amp, the simplest solution would be to avoid them at all. This was done by Ahmed in [2] where a charge pump is used to create the gain and a simple source follower to forward the signal. The proposed architecture used digital calibration to overcome circuit imperfections.

The question of this thesis was whether this idea of passive gain creation could be adapted for the use in an existing design, which exactly suffered from too high power consumption. The goal was to find ways to improve the given topology to hopefully make it work without digital calibration. This should lead to a simpler and more efficient design.

2.1. Area and Power Consumption

For system design and production costs the area occupied by a certain topology is a crucial factor. On the one hand costs per chip shrink if more chips can be placed on one wafer. In addition, the size of the chip increases the risk of defects and further may reduce the yield which lowers the profit [12, p.155]. Above all the aim is therefore a small design.

While area has mainly negative effects on the chip manufacturer, power consumption has an even wider impact. Packaging costs can be reduced for low power consumption because of less thermal requirements [4]. Additionally, power consumption has an influence on performance even during operation. Finding the right topology for the given requirements is therefore a tricky task considering the great variety of existing designs in today's literature.

Part I.

Fundamentals

3. Analog-to-Digital Conversion

An analog signal is continuous in time and can reach an infinite amount of possible values. To represent such a signal in a digital system, which has finite possible states and is working at a certain clock rate, it has to be limited by its values in time and amplitude. Otherwise the digital side could never keep track with the real world neither have a chance to represent it. The block performing this task is called analog-to-digital converter (ADC).

Digitalisation in the time domain means that the input is only observed at certain time steps. This process is referred to as sampling. Values between the sampling steps are simply neglected. According to the sampling theorem [30] the original signal can be reconstructed when the sampling frequency is more than twice of the highest signal frequency.

In case that an ADC needs more than one clock cycle to finish the conversion a sample-and-hold (S&H) block is needed. This block samples the input and charges a capacitor to store the value so that it can be provided as constant throughout the conversion process.

To reach a finite amount of states we specify the full scale range (FSR) between the lowest V_N and highest V_P allowed input. The process of digitalisation can then be described as mapping this range to a number of codes (n) with the length of N bits. With more bits the number of possible codes rises and the mapping becomes finer and finer. Therefore, the number of bits is indicating the resolution of an ADC.

The mapping process is also apparent in the transfer curve which is shown in Figure 3.2 (a) for an ideal 3 bit ADC. The quantisation step (V_{LSB}) as defined in Equation 3.3, is describing the size of one step on the analog side. All voltages within that step will be represented by the same code. For higher resolution the steps become smaller and the stair case function is converging towards a straight line. This ideal conversion curve is marked in green in the diagrams. The difference between this ideal curve to the transfer curve of an ideal 3 bit ADC is called quantisation error (Q). It can be interpreted as an information loss and its characteristic is shown below the transfer curve. The mathematical relations between the discussed parameters are given in Equation 3.1 to 3.4.

$$FSR = V_P - V_N \quad (3.1)$$

$$n = 2^N \quad (3.2)$$

$$V_{LSB} = \frac{FSR}{n} = \frac{FSR}{2^N} \quad (3.3)$$

$$|Q_{max}| = \frac{V_{LSB}}{2} = \frac{FSR}{2^{N+1}} \quad (3.4)$$

3. Analog-to-Digital Conversion

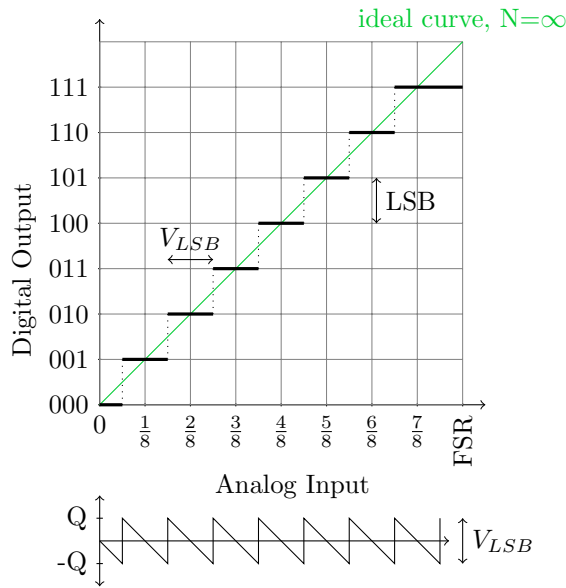


Figure 3.1.: Transfer curve of an ideal 3 bit ADC with resulting quantization error.

3.1. Ideal Characteristics

Accordingly, an ideal ADC is fully specified by the following parameters:

FSR Or V_P and V_N respectively, defines the input range the ADC is able to process.

N the Stated Number of Bits, hence the number of bits of a generated output code. Together with the FSR it determines the resolution.

f_{smp} the sampling frequency, directly implies that the time for conversion is given as $\frac{1}{f_{smp}}$.

Further, it limits the frequency of the input for which the converter can be used as a Nyquist converter to avoid aliasing to $\frac{f_{smp}}{2}$.

3.2. Error Measures of Actual ADCs

The width and location of the steps on the analog side can differ from the ideal curve because of errors in the conversion process in an actual ADC. For the characterisation of actual ADCs certain errors have been defined [28].

3.2.1. Static Errors

Static errors occur even for a constant input signal which has to be digitised. They are caused by non-ideal circuit behaviour due to component mismatch, temperature dependences or process variation. As a first requirement the input must not change more than $\frac{1}{2}V_{LSB}$ during the time of the conversion. Otherwise at the moment when the result is present at the output it will not correspond to the ADCs current input. The now discussed errors are all marked in Figure 3.2 for a better understanding.

3. Analog-to-Digital Conversion

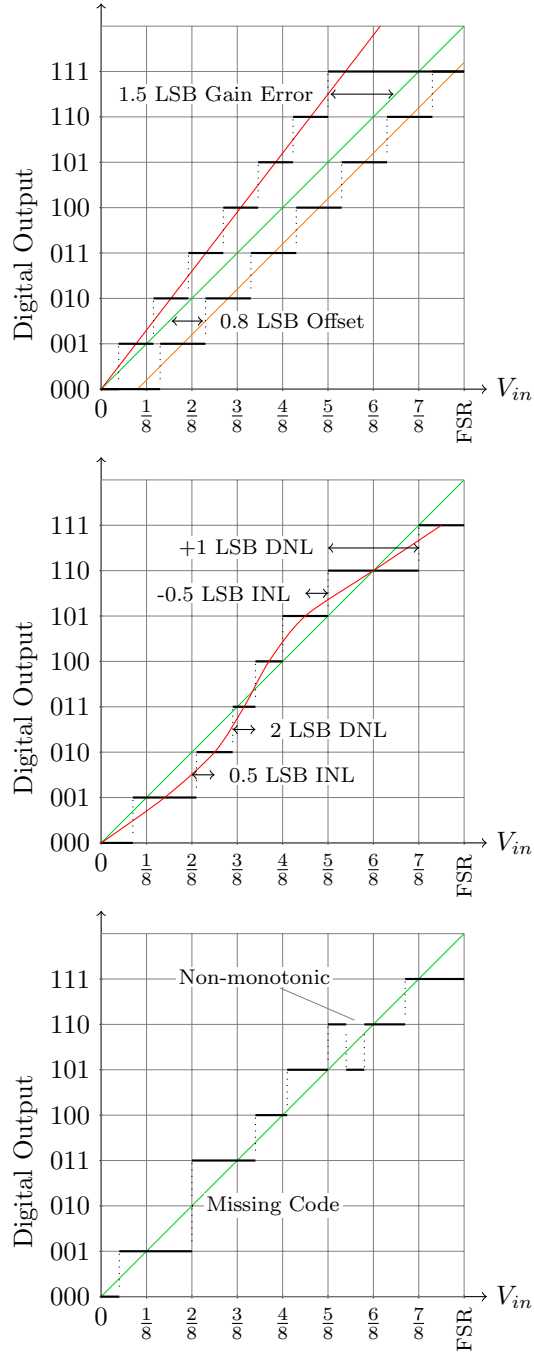


Figure 3.2.: Ideal and non-ideal ADC transfer curves showing the influence of different errors.

3. Analog-to-Digital Conversion

3.2.1.1. Offset Error

The offset error describes the difference of the origin of the transfer curve from the ideal value of $\frac{1}{2}V_{LSB}$. Accordingly, the whole curve is shifted parallel which allows to correct this error externally simply by adding or subtracting the known offset from the digital values.

3.2.1.2. Gain Error

A gain error is present if the slope of the transfer curve deviates from its ideal value. For an unipolar ADC it is measured as the distance between ideal and actual position of the last transition and usually given in parts of least significant bit (LSB) or percent of the FSR. For a bipolar ADC a negative and a positive gain error is equivalently given as the distance from the first and the last jump to their ideal positions. As this error is affecting all values in the same amount it can be eliminated afterwards by multiplying the digital values with the right correction factor.

3.2.1.3. Integral Non Linearity - INL

An integral non-linearity (INL) error is present when the midpoint of the steps of the transfer curve are not placed on a straight line. Therefore this error is often referred to as *Linearity error*. It can not be corrected in the digitised values.

3.2.1.4. Differential Non Linearity - DNL

In case the step width deviates from the ideal value and changes for different steps the ADC has a differential non-linearity (DNL) error. It is given as the maximum deviation occurring between an actual step from the ideal width.

3.2.1.5. Missing Codes and Monotony Errors

Due to the non-idealities mentioned before it can happen that certain codes will never be generated. To guarantee that no missing codes exist the DNL must stay below ± 1 LSB. To be monotone the ADC should produce rising codes for a constantly rising analog input. When the digital value decreases although the analog input was increased (or the other way round) a monotony error is present.

3.2.2. Dynamic Errors

For characterising the dynamic behaviour a sine wave over usually 90% of the FSR is applied as an input signal. The digital code is converted back to a voltage signal with an ideal DAC. The difference between the original and the reconstructed signal minus the ideal quantisation error is defined as noise added by the ADC.

In practice the dynamic errors are measured by performing a spectral analysis on the output signal. It is most common to use a Fast Fourier Transform (FFT) for this purpose. Figure 3.3 shows an exemplary spectrum. The defined dynamic error specifications will now be explained.

3. Analog-to-Digital Conversion

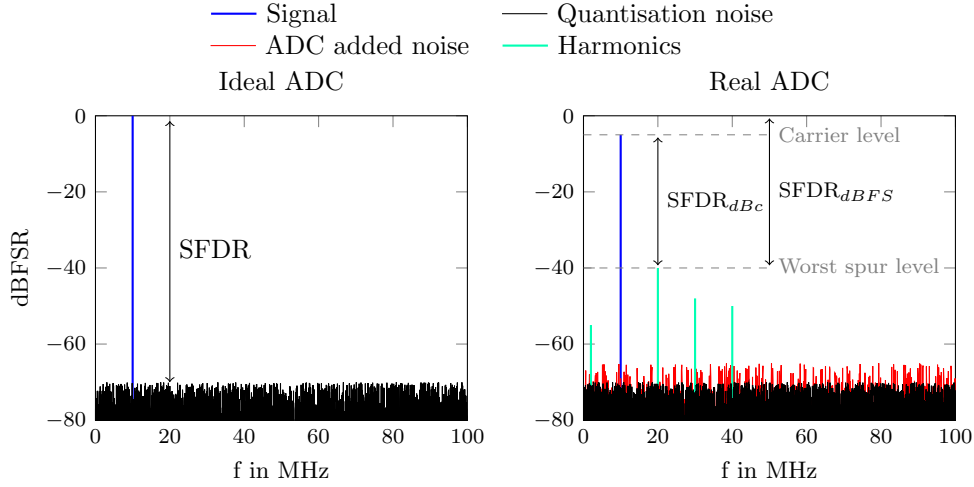


Figure 3.3.: Spectrum of an ideal ADC on the left and exemplary spectrum of a more realistic ADC on the right.

3.2.2.1. Signal-to-Noise Ratio - SNR

The signal-to-noise ratio (SNR) is defined as the ratio of the signal power to the noise power. It can also be written as the root mean square (RMS) of the input signal amplitude to the integral over the square root of the noise power spectrum over the frequency band of interest [33]. It is therefore giving a characterisation how much noise the ADC is adding in the frequency band of interest which reaches from 0 to $\frac{f_{samp}}{2}$ for a Nyquist converter. For an ideal ADC the only added noise is quantisation noise. In real life, the analog input contains many frequency components and noise making it possible to assume the quantization error as random. In this case the correlation between output signal and quantisation noise diminishes and last can be treated like white noise with an RMS noise power amplitude of $\frac{V_{LSB}}{\sqrt{12}}$ [32]. The SNR of an ideal ADC can then be calculated as:

$$\begin{aligned}
 SNR(ideal) &= \frac{P_{signal}}{P_{Noise}} = \frac{RMS(input\ amplitude)^2}{RMS(noise\ power\ amplitude)^2} = \frac{RMS(\frac{FSR}{2})^2}{(\frac{V_{LSB}}{\sqrt{12}})^2} \\
 \sqrt{SNR(ideal)} &= \frac{FSR}{2\sqrt{2}} \frac{\sqrt{12}}{V_{LSB}} = \frac{FSR}{2\sqrt{2}} \frac{\sqrt{12}}{\frac{FSR}{2^N}} = \frac{2^N \sqrt{12}}{2\sqrt{2}} = 2^N \frac{\sqrt{6}}{2} \\
 SNR_{dB}(ideal) &= 20 \cdot \log\left(2^N \frac{\sqrt{6}}{2}\right) = 20 \log(2)N + 20 \log\left(\frac{\sqrt{6}}{2}\right) = 6.02N + 1.76 \quad (3.5)
 \end{aligned}$$

Equation 3.5 stated the maximum SNR for a given resolution and shows that for an ideal ADC the SNR can only be improved by increasing the resolution.

3. Analog-to-Digital Conversion

3.2.2.2. Signal-to-Noise and Distortion Ratio

The signal-to-noise and distortion ratio (SNDR), sometimes also abbreviated as SINAD, includes the distortion of the ADC in the SNR.

$$SNDR_{dB} = 10 \cdot \log \left(\frac{P_{signal}}{P_{Noise} + P_{Distortion}} \right) \quad (3.6)$$

In reality, the achieved SNDR of an ADC will always be lower than the SNR. The difference between these two parameters can then be used to calculate the effective number of bits (ENOB).

3.2.2.3. Effective Number of Bits - ENOB

The ENOB can be derived using the SNDR of an actual ADC to calculate the equivalent resolution in bits of an ideal ADC. It gives a measure about how many of the stated bits can actually be reconstructed. Therefore, it is a more straight forward characterisation for the accuracy of an actual ADC and often used instead of the SNDR.

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \quad (3.7)$$

The difference between the ENOB and the stated number of bits is indicating the lower SNR due to additional noise and distortion in the ADC.

3.2.2.4. Total Harmonic Distortion - THD

The output of a non-linear ADC will contain harmonics of the input frequency. The ratio of the power off the first k harmonics to the power of the signal is defined as the total harmonic distortion (THD) [27]¹. Usually, k is chosen between four up to ten [28].

$$THD_{dB} = 10 \cdot \log \left(\frac{\sum_{i=2}^k A_{harmonics,i}^2}{A_1^2} \right) \quad (3.8)$$

The THD+N includes noise in the above equation. In case the noise is measured over the Nyquist bandwidth (which is not always true for audio) this value is equal to the reciprocal of the SNDR.

3.2.2.5. Spurious Free Dynamic Range - SFDR

The spurious free dynamic range (SFDR) is the ratio between the sine wave signal amplitude and the amplitude of the largest non-signal spur in the spectrum. When the spectrum is plotted in dB, which is the case most of the times, the SFDR is equal to the distance between these two peaks (see Figure 3.3).

$$SFDR_{dB} = 10 \cdot \log \left(\frac{A_1^2}{A_{spur}^2} \right) \quad (3.9)$$

¹Sometimes the THD is defined as the reciprocal value [20].

3.2.2.6. Effective Resolution Bandwidth - ERBW

To fully characterise an ADC the SNDR and SFDR have to be measured for different input signal frequencies f_{sig} . For low input frequencies the SNDR is at a constant value but it starts to drop for higher frequencies. The value of f_{sig} where the SNDR has fallen by -3 dB is defined as the effective resolution bandwidth (ERBW). It indicates until which input signal frequency the converter may be used. For a Nyquist converter this frequency should be larger than half the sampling frequency $ERBW \geq \frac{f_{samp}}{2}$. Otherwise, the ADC loses bandwidth due to its inherent noise as in Figure 3.4. For the ADC with the blue curve the high sampling of $\frac{f_{samp}}{2}$ is futile. It requires an ADC with a better noise performance (drawn in light blue) to exploit the whole sampling speed.

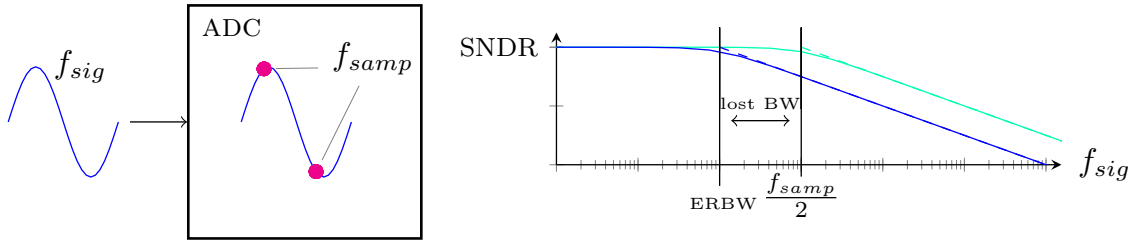


Figure 3.4.: Specification of an ADC over signal frequency. The ERBW should be as high as half the sampling frequency to avoid that bandwidth is lost due to the noise of the ADC.

3.2.3. Figure of Merit - FOM

In order to make different ADCs more comparable to each other, certain figure of merits (FOMs) have been introduced. They should give a classification for operation efficiency. In general they try to set the used resources (area or power) in relation to the produced bit rate and resolution. Unfortunately, different functions are common to bring the ENOB and the sampling frequency into play.

$$FOM_{area} = \frac{Area}{f(ENOB, f_{samp})} \quad (3.10)$$

$$FOM_{power} = \frac{Power}{f(ENOB, f_{samp})} \quad (3.11)$$

Where $f(ENOB, f_{samp})$ is one of the following:

$$f(ENOB, f_{samp}) = 2^{ENOB} f_{samp} \quad (3.12)$$

$$= 2^{2 \cdot ENOB} f_{samp} \quad (3.13)$$

$$= 2^{ENOB} \cdot 2 \cdot ERBW \quad (3.14)$$

Equation 3.12 as set by Walden in [33] is used most commonly. Equation 3.13 takes account that due to thermal noise for twice the resolution four times the power is necessary [24]. Therefore, it credits a higher ENOB with the factor of two, which gives a more meaningful FOM for higher resolution ADCs. Equation 3.14 as in [9] considers the ERBW instead of the sampling frequency. Implying that the converter is operating as a Nyquist converter and where $2 \cdot ERBW \geq f_{samp}$ is valid. Typical values range around $100 \text{ nm}^2/\text{conversion}$ and $1 \text{ pJ}/\text{conversion}$ [27].

4. ADC Topologies

Multiple methods exist for referencing the infinite number of states on the analog side to the limited amount of states on the digital side. The relevant ones will be presented here in detail. Other methods are just mentioned shortly for the sake of completeness and a source for further information is provided.

4.1. Direct ADCs

The group of direct ADCs comprises converters which directly compare the input to one or more references to generate a digital code proportional to the input.

4.1.1. Comparator

A comparator can be seen as the most primitive form of an ADC. Though, it is an indispensable building block for each of the following topologies. Its basic function is deciding which of its two inputs is higher. Accordingly, it is implementing an one bit ADC.

4.1.2. Flash Converter

In principle, a flash converter functions like a ruler. When measuring a distance we apply the scale next to it and literally check until which marker the object of interest reaches.

In the electronic circuit each stroke on the ruler is realized with a comparator able to detect whether the input exceeds its reference or not. Mostly the references are generated by a simple resistive voltage divider as shown in Figure 4.1. Imagining the mm steps on a ruler for one meter it becomes clear that the circuit effort becomes incredible large with rising resolution. Expressed in bits this example would be equal to roughly 10 bits as $2^{10} = 1024$.

Generally, the number of comparators and reference voltages rises exponentially with the number of bits and can be given by $2^N - 1$ ¹. Additionally, for better resolution also accuracy of the components has to increase. In most cases this implies larger devices to suppress process variation. This makes obvious why flash converters are limited to low resolutions.

Since all comparators are clocked in parallel the needed time for conversion is just one clock cycle but this also leads to high power consumption. Summarized, a flash converter is the fastest conversion technique with the drawback of high power consumption as well as area needed on chip. However, flash converters of smaller resolution are often used as sub-blocks in other ADC principles like successive approximation register (SAR) [4.1.3] and pipelined ADCs [4.1.4.2] for multiple bit stages.

¹The -1 originates from the fact that it needs just one cut to receive two pieces out of a whole.

4. ADC Topologies

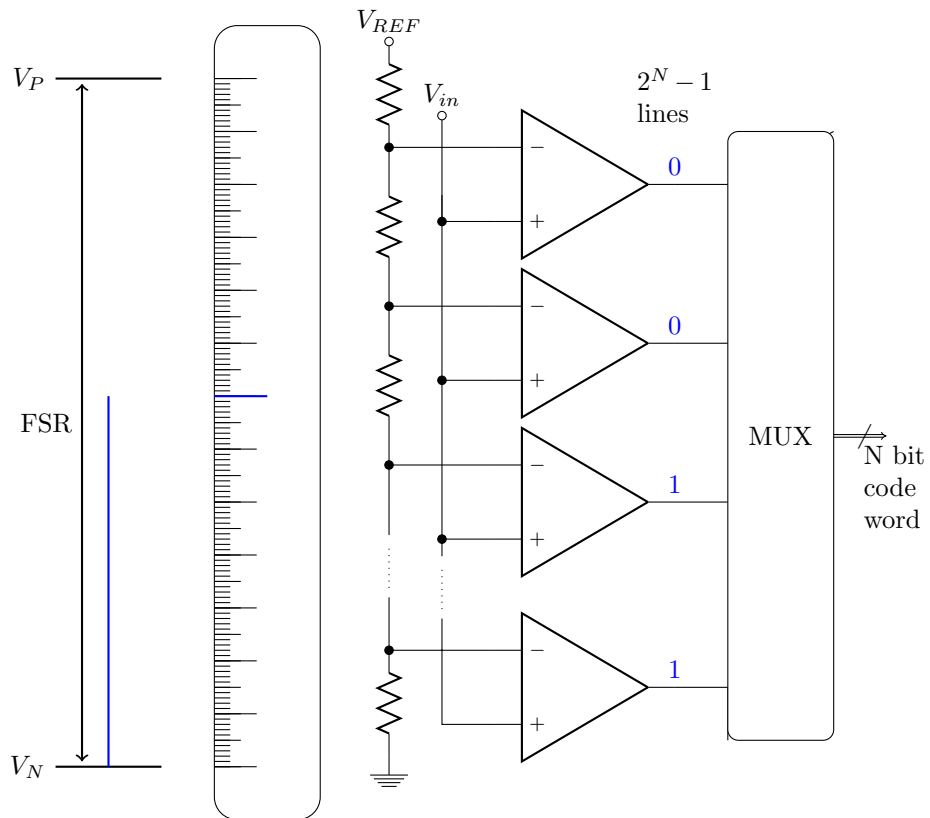


Figure 4.1.: Principle and basic circuit of a Flash-Converter

4.1.3. Successive Approximation Register ADC

An SAR based ADC implies the principle of an old manually operated scale. During each iteration step the unknown mass is compared with a known mass. According to which side is heavier the known mass is adjusted by adding or retrieving a known weight. If an equilibrium state is reached we can assume that both masses equal each other and the value of the unknown mass has been determined.

The according electronic circuit consists of an SAR, a DAC and a comparator connected as in Figure 4.3. The process described above has to follow a strict pattern and is shown for two inputs in Figure 4.2. In the first cycle the SAR sets the most significant bit (MSB) and the DAC generates the corresponding voltage, in particular the middle of the FSR. This voltage is compared to the input by the comparator. Depending whether the input is higher or lower the MSB remains set ("weight stays on the scale") or is reset ("retrieved from the scale") for the next code generation in the SAR.

This algorithm is generally known as binary search. Since the same steps are done for all bits down to the LSB it requires as many clock cycles as bits to acquire the result. During this time the input signal has to remain constant. Additionally, there is a delay until the conversion code is valid at the output. In other words the internal clock has to be higher by the factor of bits converted than the sampling clock. For high resolutions this topology needs very high internal clock frequencies. The corresponding relations are indicated in Figure 4.3.

The advantage of this topology is the small area consumption on chip, as all components (comparator, DAC, ...) are only placed once and are reused for each bit generation.

Instead of a comparator, a flash can be used to convert multiple bits (N_{cc}) per clock cycle. In this case the operation frequency of the block reduces to $\frac{N}{N_{cc}}$.

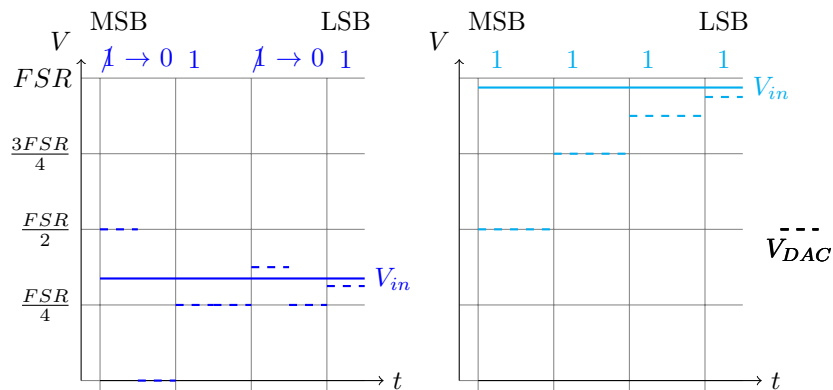


Figure 4.2.: Demonstration of the principle of an SAR-ADC for two input voltages. Where each bit is tentatively set and reset if V_{DAC} turned out to be higher.

4. ADC Topologies

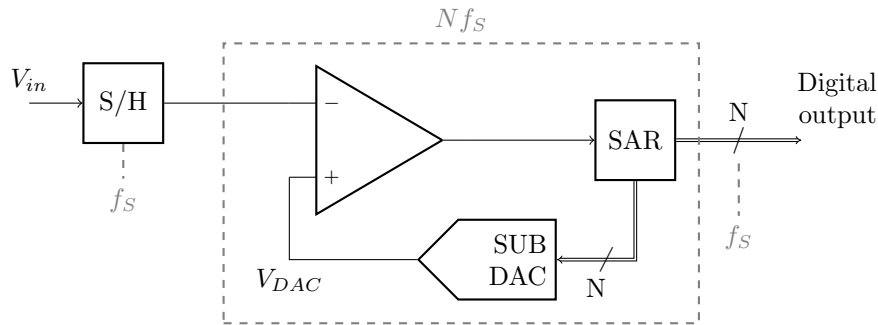


Figure 4.3.: Block diagram of an SAR-ADC showing the different operation frequencies of the parts of the circuit.

4.1.4. Algorithmic ADC

Like an SAR the algorithmic ADC uses the method of binary search. On the contrary, not the reference is changed, comparing it over and over again with the input, but the input voltage itself, which is compared with a constant reference.

In Figure 4.4 the process of code generation is shown for two input voltages (for comparison the same voltages as for the SAR in Figure 4.2). A comparator decides whether the voltage is in the upper or lower half of the FSR. This decision generates the first bit. In the next step the area, where according to the comparator the input is lying, is scaled up to span over the whole FSR again. For the next bit the comparator is again comparing the modified input with the middle of FSR. This process is done N times to determine all bits. The digital code can later be created using the consecutive decisions in which region the input was located.

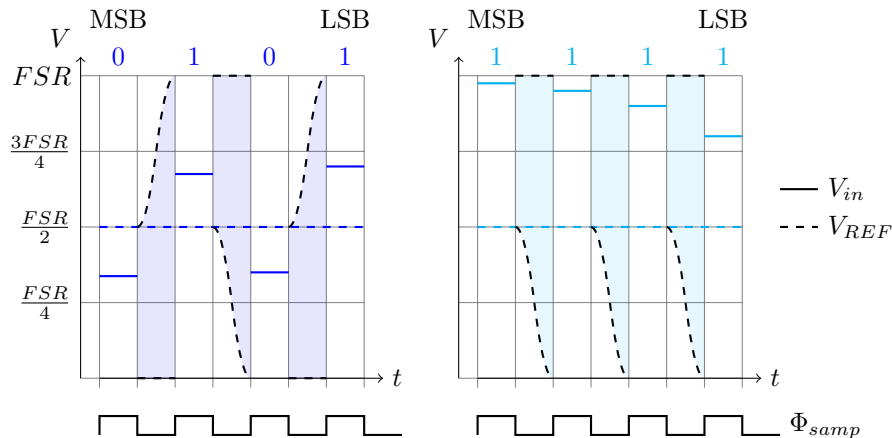


Figure 4.4.: Method of code generation in a pipelined ADC, demonstrating the step where one half is scaled up to the FSR while the reference stays constant.

In circuit realisation the scaling is done by a multiplication by two which is equivalent to a gain function. This works straight forward for the lower region which will then span over the whole area. However, the upper region is thereby moved away from the reference. In this case

4. ADC Topologies

a down shift is needed so that the constant reference is kept in the middle. The residue for the consecutive stage can be described by the following mathematical operations:

$$V_{in}^{i+1} = \begin{cases} 2V_{in}^i - V_P & : \text{ for } V_{in}^i > \frac{FSR}{2} \\ 2V_{in}^i & : \text{ for } V_{in}^i < \frac{FSR}{2} \end{cases}$$

The block diagram to build this functionality is shown in Figure 4.5. It can be used to build two embodiments as explained next.

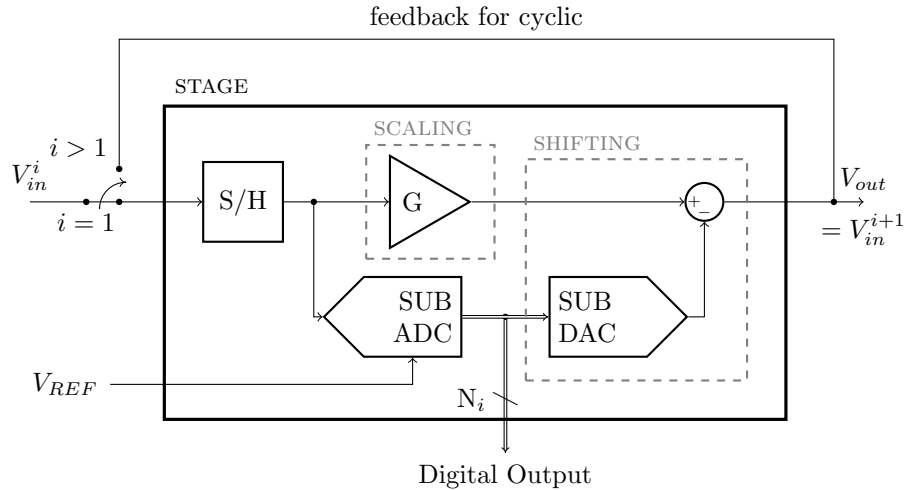


Figure 4.5.: Block diagram of a basic pipelined ADC stage indicating the functions of the individual parts of the circuit.

4.1.4.1. Cyclic ADC

If the residue voltage is fed back to the input to reuse the same stage for the next bit the ADC is called cyclic. During each clock cycle the block will output one bit and the modified input voltage V_{in}^{i+1} . The modified input voltage is feedback and the bits have to be collected.

The cyclic approach is characterized by its minimal required components as they are reused for the different bits. Like for the SAR this leads to a delay of N clock cycles between sampling and finishing the whole N bit code. Since the single stage can only handle one input value at the time it can only take a new sample when the conversion is finished. As a result the internal operation frequency has to be higher than the sampling frequency by the factor of bits to be resolved.

4.1.4.2. Pipelined ADC

In case the residue is passed on to a next stage the ADC is called pipelined.

Since each stage in the pipeline is passing on the modified input signal, it is able to sample the analog input in each clock cycle. The bits generated by each stage have to be delayed until the residue reaches the end of the pipeline. Of course, the whole output code still has a delay regarding its corresponding input since it had to propagate through the pipeline. However, the throughput is equal to one whole code per clock cycle.

4. ADC Topologies

The structure of such a pipeline is shown in Figure 4.6 where the two different phases are indicated. In sampling phase the stage is receiving the output voltage of the previous stage. In the other half of the clock cycle the stage is performing the $2V_{in} + c$ function and forwards the signal. A further possibility in design for a pipeline is stage scaling. Due to the present gain later

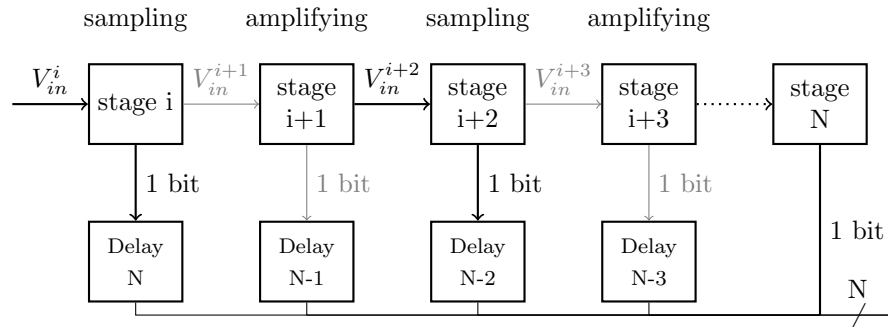


Figure 4.6.: Signal flow and error correction in a pipelined ADC using the basic stage block presented in 4.5.

stages require less accuracy [8]. This allows a reduction in area and power consumption and will be discussed in detail in section 5.2. Stage scaling allows to exploit the benefits of the pipelined approach while investing less than N times the effort.

In general, an arbitrary number of bits can be converted per stage. The upper limit is given by the needed flash converter in the sub-ADC and its inefficiency with higher resolution. Multiple bits per stage mean that one stage is already detecting for more regions (e.g. four which would be equivalent to a two-bit stage). To reuse the same references it is then necessary to realise a larger gain and adjust the shifting. Converting multiple bits per stage is common for the first stages in pipelined ADCs with high resolution. In this case the accuracy requirements for the first stages would otherwise become very demanding as presented in subsection 5.1.1. The optimum stage resolution considering area, power consumption and conversion rate is a pipeline with minimal, hence 1 bit, resolution per stage [21].

4.2. Indirect ADCs

These ADCs create a proportionality between the analog input signal and a time span. This is beneficial because time can be measured and digitised quite simply using high frequency clocks. To do so a counter is connected to the clock which starts counting at a start pulse and stops counting for some end event. An inherent problem for all ADCs in this group is that the time span should not be chosen to short compared to the clock period. The reason is that the final counter number should never be too small in order to reduce the relative error introduced by the ± 1 insecurity in the counter. This error emerges simply by the possible asynchronism between the clocking edges and the start or end pulse.

A Single-Slope Converter or Ramp-Compare Converter is measuring the time a constant ramp signal needs to reach the input voltage [14].

4. ADC Topologies

The Dual-Slope Converter or 2-Ramp Converter tries to overcome component dependencies present in a Single-Slope converter. To do so it operates in two cycles. In the first cycle the input voltage is integrated for a constant time. In the second phase a constant reference voltage is used for reverse integration. With the known reference the proportionality of the two time spans can be used to calculate the input value while component values will cancel out.

ADCs with a high linearity can be built with these topologies.

4.2.1. Sigma-Delta-Converter

A sigma-delta ADC ($\Sigma\Delta$ -ADC) is integrating its constant input voltage and compares the integrated value with a positive and a negative reference. When the positive reference is reached the highest possible input is subtracted from the input. As a result the voltage to be integrated will now be negative and further the integration result is decreasing. Once the negative reference is reached the highest possible input is added again. Accordingly, the integrator's output voltage rises again. The binary signal encoding whether the integrator is in the rising or falling phase is representative for the input value. In case the input is in the middle of FSR the high and low times will have equal widths. If the voltage is closer to one of the edges of the FSR either the high stage or the low stage is dominating in the output code. Although this principle is easy to understand the mathematical post-processing is somewhat cumbersome [19].

4.3. Time Interleaved ADCs

Time interleaved ADCs are not really a type of ADC on their own. Rather time interleaving is a method to relax the requirements on a single ADC, concerning its sampling and conversion speed, by using multiple ADCs processing the same input but staggered in time. As a result each ADC has more time for the conversion until its next turn to take an input sample. However, these quasi-parallel working ADCs can be of whatever type presented so far.

4.4. Range of Operation

The two main aspects for choosing the topology are desired resolution and sampling frequency. Flash converters are limited to high speed and low resolution. The SAR ADC is restricted by its internal operation frequency which is N-times higher than the sampling frequency. Time based methods show the possibility of high accuracy but are restricted to low speed. The pipeline ADC has therefore become popular for medium-high speed and resolution showing a good compromise for area and power consumption [25].

5. Pipelined ADC Design

In subsection 4.1.4.2 the pipelined ADC was introduced at a principle level. We now want to investigate on certain constraints which have to be considered in its practical usage.

5.1. Accuracy Requirements

To derive the necessary accuracy or in other words, the allowed error V_ϵ of an ADC as in Figure 5.1 (a) we use the allowed deviation of the input which will not cause an error in the output of an ideal ADC. The output will not change for an input change in this range as it gets lost in the quantisation noise.

$$|V_\epsilon| \leq Q_{max} = \frac{V_{LSB}}{2} = \frac{FSR}{2^{N+1}} \quad (5.1)$$

The allowed fractional error is then defined as:

$$\epsilon_a \cdot \frac{FSR}{2} = V_\epsilon \leq \frac{FSR}{2^{N+1}} \quad (5.2)$$

$$\epsilon_a \leq \frac{1}{2^N} \quad (5.3)$$

This is what is often referred to as N-bit accuracy which is sufficient specification for a flash or a SAR converter. For the pipeline, however, the input is amplified from stage to stage so that errors which occur later have less relative impact. This changes the necessary specifications in each stage.

To derive the requirements we examine a pipeline with NS stages as in Figure 5.1 (b). Where G_i is the gain in stage i, generally given by 2^{N_i} and N_i is the number of bits converted in stage i. Then the stated number of bits is given by:

$$N = \sum_{i=1}^{NS} N_i \quad \text{where for equal stages: } N = NS \cdot N_i \quad \text{and for } N_i=1: N = NS \quad (5.4)$$

As a first step all possible errors are referred back to the input:

$$\epsilon_{tot} = \frac{\epsilon_i}{G_i} + \frac{\epsilon_{i+1}}{G_i \cdot G_{i+1}} + \dots = \sum_{i=1}^{NS} \frac{\epsilon_i}{\prod_{j=0}^i G_j} \quad (5.5)$$

For all stages converting one bit the gain becomes $G_i = 2$ and $N = NS$ so we further can write:

$$\epsilon_{tot} = \sum_{i=1}^N \frac{\epsilon_i}{2^i} \quad (5.6)$$

5. Pipelined ADC Design

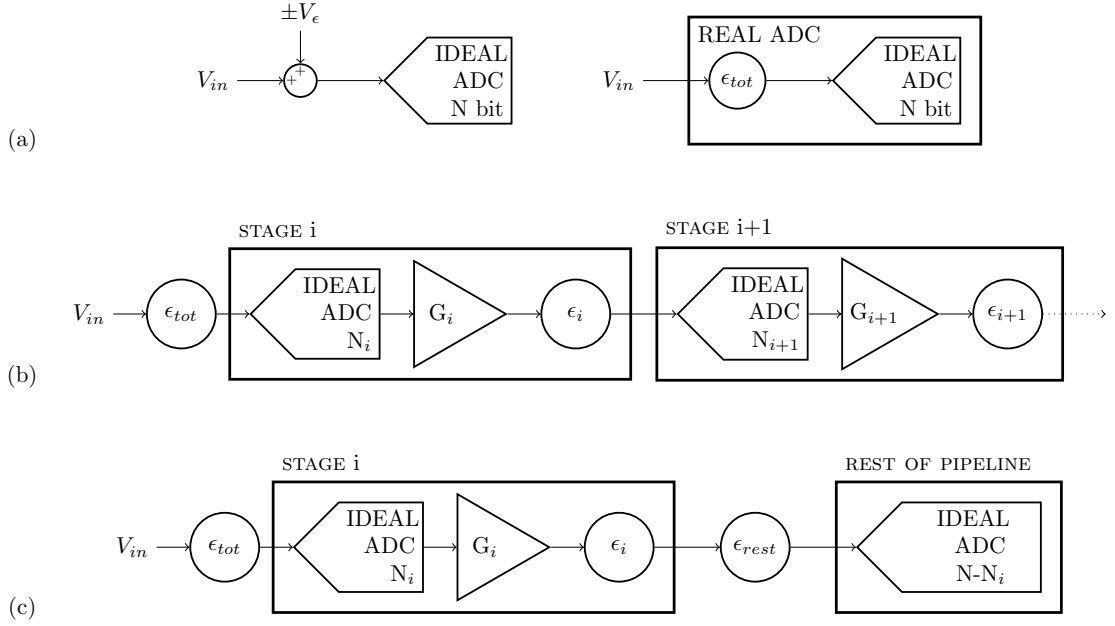


Figure 5.1.: Pipelined ADC block diagrams used to derive the allowed fractional error ϵ_i in each stage.

If the error is uniformly distributed over the stages, meaning each stage contributes the same error, the parts of the sum have to be equal. This is the necessary condition for the needed accuracy to assure that the pipeline has no missing codes. The final condition is derived in Equation 5.7.

$$\begin{aligned}
 \sum_{i=1}^N \epsilon_u &= N \cdot \epsilon_u \leq \epsilon_a \\
 N \cdot \epsilon_u &\leq \frac{1}{2^N} \\
 \epsilon_u &\leq \frac{1}{N \cdot 2^N} \\
 \frac{\epsilon_i}{2^i} &\leq \frac{1}{N \cdot 2^N} \\
 \boxed{\epsilon_i} &\leq \frac{1}{N \cdot 2^{N-i}} \tag{5.7}
 \end{aligned}$$

for the last stage: $\epsilon_N \leq \frac{1}{N}$

Yet for design another specification is more common. Stage i is inserted before an existing ADC which converts the rest of the bits $(N - N_i)$ as in Figure 5.1 (c). The necessary accuracy of the additional stage is then derived using the relation between the total allowed error at the input

5. Pipelined ADC Design

and the allowed error of the rest of the pipeline.

$$\begin{aligned}
 \frac{\epsilon_i}{G_i} + \frac{\epsilon_{rest}}{G_i} &\leq \epsilon_a \\
 \frac{\epsilon_i}{G_i} + \frac{\epsilon_{rest}}{G_i} &\leq \frac{1}{2^N} \\
 \epsilon_i + \epsilon_{rest} &\leq \frac{G_i}{2^N} \\
 \epsilon_i &\leq \frac{G_i}{2^N} - \epsilon_{rest} \\
 \epsilon_i &\leq \frac{2^{N_i}}{2^N} - \frac{1}{2^{N-N_i}} \\
 \epsilon_i &\leq \frac{1}{2^{N-N_i}} - \frac{1}{2^{N-N_i}} = 0
 \end{aligned} \tag{5.8}$$

Equation 5.8 means that for the added stage no error budget would be left if the remaining ADC is just accurate to the number of bits converted from there on. This makes clear why the rest of the pipeline has to be over specified as it can be seen in Equation 5.7, where for the last stage (converting only one bit) a fractional error of $\epsilon_N \leq \frac{1}{N}$ is desired. Usually, a factor of two is chosen, leaving an error budget for the added stage. For design the allowed error is split in half for dynamic and static errors.

$$\begin{aligned}
 \epsilon_i &\leq \frac{1}{2^{N-N_i}} - \frac{1}{2} \frac{1}{2^{N-N_i}} \\
 \epsilon_i &\leq \frac{\frac{1}{2}}{2^{N-N_i}} = \frac{1}{2^{N-N_i+1}} = \frac{1}{2^{N-i+1}} \\
 \boxed{\epsilon_{S,D} &\leq \frac{1}{2^{N-i+2}}}
 \end{aligned} \tag{5.9}$$

Note that the factor was more or less chosen arbitrarily but can be interpreted as keeping the additional error below the RMS of the quantisation error of the rest of the pipeline.

$$\frac{V_{LSB} \text{ (of remaining ADC)}}{\sqrt{12}} \approx \frac{FSR}{2^{N-N_i}} \frac{1}{4} \rightarrow \epsilon_i \frac{FSR}{2} \leq \frac{FSR}{2^{N-N_i}} \frac{1}{4} \rightarrow \epsilon_i \leq \frac{1}{2 \cdot 2^{N-N_i}} \rightarrow \epsilon_i \leq \frac{1}{2^{N-i+1}}$$

Be aware that with this setting the sum of the stage errors will not full-fill the total allowed error in Equation 5.3, because we did not account the rest of the ADC having the error characteristic of a pipeline. This is accepted because the equation sets the lowest mathematical boarder even considering the worst case scenario.

The three equations are plotted in Figure 5.2 on a logarithmic scale for 2, 4, 8, 12, 16, (24) 1-bit stages. Clearly, things become more demanding for higher N but also the common design assumption (○) deviates more and more from the mathematically correct condition (×) for higher N.

5. Pipelined ADC Design

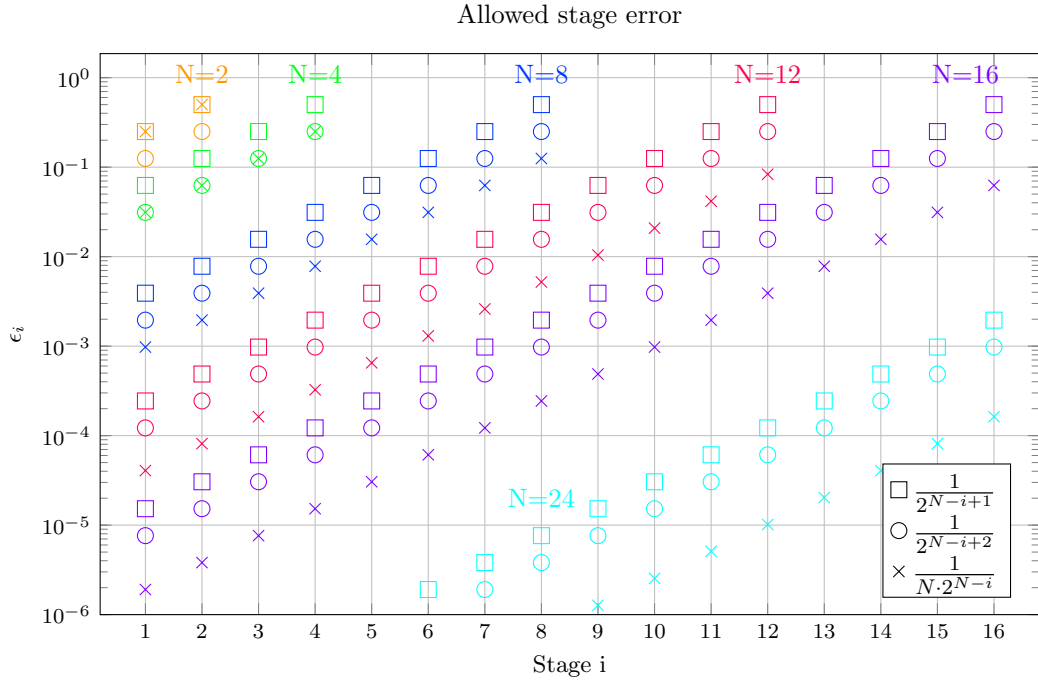


Figure 5.2.: Allowed fractional error ϵ in stage i in a pipelined ADC. Shown for $N = 2, 4, 8, 12, 16, (24)$.

5.1.1. Stage Error

With the calculated desired error figures the residual voltage can be given by

$$V_{out}^i = (G_i \cdot V_{in}^i + V_{ADD}) \cdot (1 \pm \epsilon_i) \quad (5.10)$$

And further the allowed gain variance in stage i can be calculated as:

$$G_i = G_{i,ideal} \cdot (1 \pm \epsilon_i) \quad (5.11)$$

5.2. Stage Scaling

At the beginning of this chapter we laid out that the precision can decrease down the pipeline. This fact can be used to save area and power in the subsequent stages. However, in OP-amp based solutions this option is seldom chosen [22]. Designing and lay-outing the amplifier in different versions, with its high complexity would mean too much effort. Likewise, also the comparator is only designed once for all stages. As a result scaling is only applied to sampling capacitors [8] and OP-amp bias currents [9] to reduce power and area consumption.

5.3. Comparator Offset and Redundancy

An additional problem arises for the error of the comparator. If it is not exactly cutting the FSR in half the larger region will not fit in the allowed FSR after amplification. Once a pipeline stage saturates all following generated bits will not have a correlation to the input any more.

5. Pipelined ADC Design

In order to achieve a certain resilience against comparator offset it is common to implement the pipelined ADC using more comparators than actually needed. This introduces some redundant bits which can be used for error correction. The pipeline is then extended by a correction block which is collecting two bits per stage and calculates the final N bit code as illustrated in Figure 5.3.

In case of a 1-bit stage two comparators are used. This divides the FSR into three regions and leads to a conversion of two bits for three states, so effectively this is 1.5-bit stage.

As we can see in Figure 5.4 (b) the offset of the comparator is now not automatically leading to a saturation of the next stage but the signal stays inside the FSR.

The two thresholds are placed $\frac{FSR}{8}$ below and above the original comparator threshold $\frac{FSR}{2}$, resulting in an output of $V_L = \frac{FSR}{4}$ and $V_H = \frac{3FSR}{4}$. This setting allows the maximum correction of a negative and positive offset error as shown in Figure 5.4 (d).

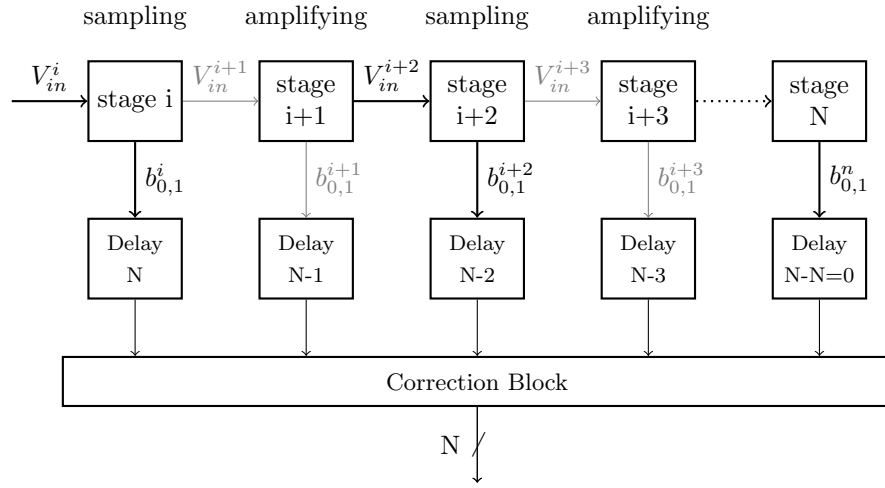


Figure 5.3.: Signal flow and error correction in a pipelined ADC using the basic stage block presented in 4.5.

The residual voltage of such a stage can be given by

$$V_{out}^i = V_{in}^{i+1} = 2V_{in}^i + V_{ADD}$$

and more precisely for the different regions:

$$V_{out}^i = V_{in}^{i+1} = \begin{cases} 2V_{in}^i - V_P & : \text{ for } V_{in}^i > V_{th_P} \\ 2V_{in}^i - V_{CM} & : \text{ for } V_{th_N} < V_{in}^i < V_{th_P} \\ 2V_{in}^i - V_N & : \text{ for } V_{in}^i < V_{th_N} \end{cases}$$

Due to its robustness and minimal hardware effort the 1.5-bit stage is very popular for pipelined ADC design [21].

5. Pipelined ADC Design

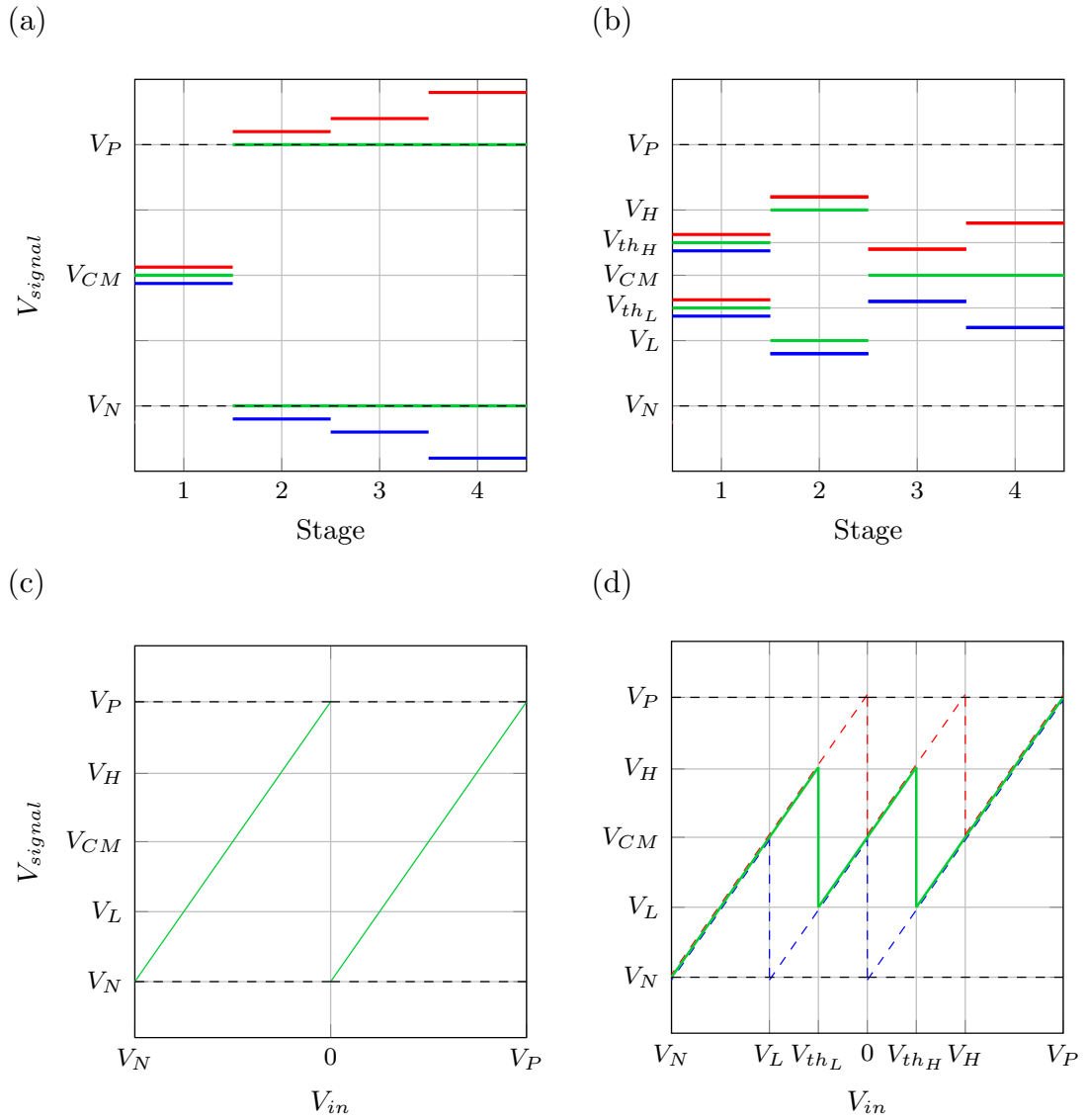


Figure 5.4.: Demonstrating the problem of comparator offset in (a) for a stage with only one comparator. The according transfer curve of the stage is shown in (c). In (b) the situation is shown for a 1.5-bit stage. Now comparator offset not automatically saturates the stage.

5.4. 1.5-bit Differential Stage Realisations

In Figure 5.5 the 1.5-bit pipelined stage is revised in more detail. The DAC reduces to a simple 1-out-of-3 multiplexer (MUX) selecting V_{ADD} . The block in focus of this work is marked in blue. This block is usually implemented as a switched capacitor network (see chapter 6) and realizes a S&H, multiplication by two and shifting the signal to reuse the same references. As discussed beforehand in subsection 5.1.1 this block is therefore highly important to achieve the specified INL and DNL. The following section will introduce possible concepts for this block.

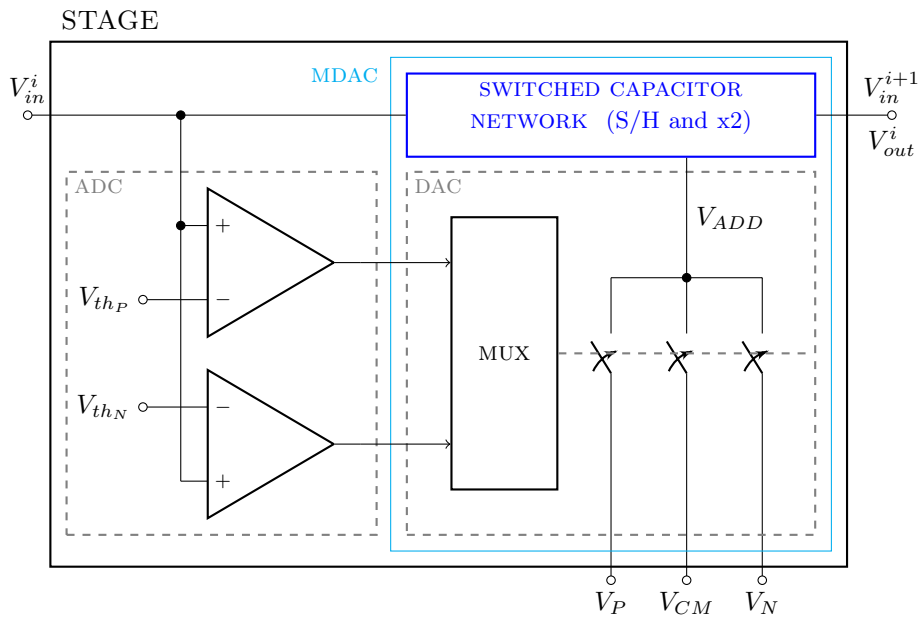


Figure 5.5.: Detailed block diagram of a basic pipelined ADC stage.

5.5. Concepts for MDAC Realisation

We want to focus on the different ways to create the gain in a multiplying digital-to-analog converter (MDAC). To do so, the DAC which is universal for all concepts is not drawn. Instead, V_{ADD} is seen as an input providing the correct shifting voltage.

Concepts for the remaining, labelled switched capacitor network block in Figure 5.5, are summarized in Figure 5.6 in their fully differential implementation. Since the picture is meant to give an overview, switches were spared out. Alternatively, the charging during sampling phase is shown left (for the p channel) while the circuit during amplification is shown in the middle. The orientation of the capacitors is indicated by the node marked in red. On the right, tables with the charging conditions are given for easier comparison.

5. Pipelined ADC Design

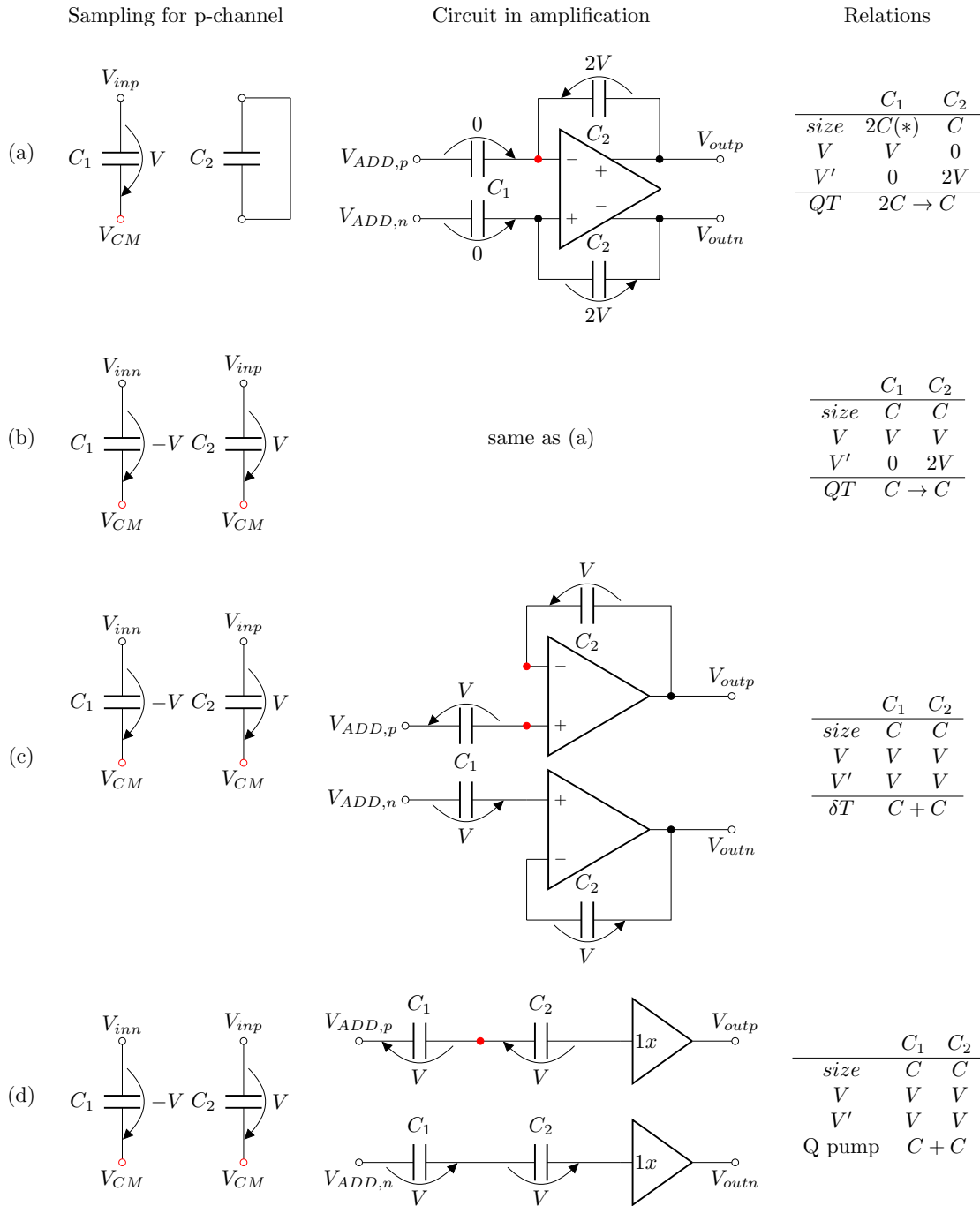


Figure 5.6.: Different MDAC architectures: (a) QT for an arbitrary gain factor for variable C_1 (b) QT for $G=2$ as in a 1.5-bit stage (c) $C+C \delta T$ as in [27] (d) $C+C$ charge pump as in [2]

5.5.1. Charge Transfer Technique QT

The charge transfer technique (QT) technique is by far most commonly used to implement the MDAC [16, 17, 34] as in Figure 5.6 (a) or [13, 1, 26, 35] as in (b). It is characterized by the fact that the OP-amp is transferring all the charge from capacitor C_1 to C_2 . Inherently, the ratio of these two capacitors determines the gain. Equally, matching of (multiples of the) capacitor values is essential for accuracy.

For pipeline stages which convert more than 1 bit and require a gain higher than two, type (a) in Figure 5.6 is used and capacitor C_1 is realised larger by the factor of the necessary gain [9]. For a required gain of two option (b) can be used. In this case both capacitors are preloaded with the same input voltage.

5.5.2. Delta Charge Flow Technique δQ

Whereas in the QT approach all the charge was transferred from one capacitor to the other this technique is only transferring the charge needed to compensate for the existence of parasitic capacitors. In the ideal case, without parasitics, there is no charge moved at all and the OP-amp has the primary function of buffering. Compared to QT a realisation with the delta charge flow technique (δQ) yields a higher feedback factor for the closed loop of the amplifier [27, p. 10]. Further, capacitor matching requirements are relaxed and allow higher accuracy up to four extra bits [27, p.201]. Yet two independent OP-amps are needed.

5.5.3. C+C Charge Pump

This approach tries to avoid the use of OP-amps by creating the gain of two by a simple capacitive adder. To forward the signal in the pipeline only an unity gain buffer is needed. The circuit proposed in [2] is shown in detail for the p-channel in Figure 5.7. The switch S_{mid} is used to implement bottom plate sampling when the switches S_{S1} open shortly before S_{S2} . To keep design complexity low a source follower was used as a buffer. A drawback of this design is that digital calibration is necessary to compensate the low gain of just 1.8. Beside the fact that digital circuitry is needed, the execution of the calibration process also takes time during runtime.

5.5.3.1. Shortcomings

Since this topology creates the gain passively its general issue is charge redistribution. Charge redistribution or charge sharing happens when two capacitors preloaded with different voltages are switched together. More generally, the same effect applies when the common node of two capacitors is loaded to the same voltage in one phase and in the next phase one of the capacitors is driven with an additional voltage at the other node.

In the proposed circuit exactly this problem arises at the middle node due to the existence of the bottom plate capacitors. While in the other two concepts re-charging of these parasitics was done by the OP-amp there is no active circuitry in charge of doing so here. The node is pre-charged to V_{CM} and should jump to $V_{ADD,p} + \frac{V_{in}}{2}$. But due to charge sharing it will reach a voltage lower than this.

5. Pipelined ADC Design

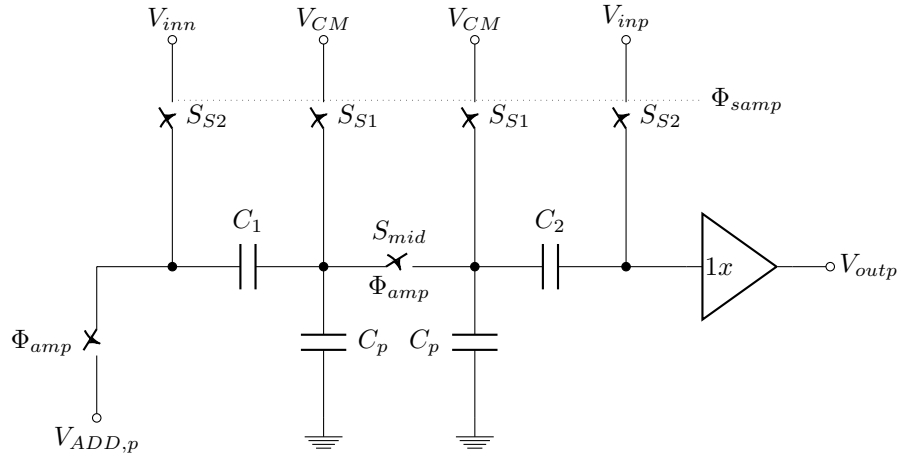


Figure 5.7.: The voltage C+C charge pump based MDAC presented in [2]

The same happens for the node at the output. The buffer node is pre-charged to V_{inp} and is ideally facing a jump to the desired output $2V_{in} + V_{ADD,p}$ when switches for amplification are closed. Since C_1 already lost charge at the middle node, the output node will just try to be lifted to $V_{ADD} + \frac{V_{in}}{2} - V(\text{lost on } C_1) + \frac{V_{in}}{2}$. Again the voltage will not reach this value as well because some charge is lost when charging the parasitic.

In total both effects simply superpose each other. The overall result on the output signal is shown in Figure 5.9. As it can be clearly seen the slope of the real signal output curve is reduced which is equivalent to a constant negative gain error. In [2] this error was handled using digital calibration.

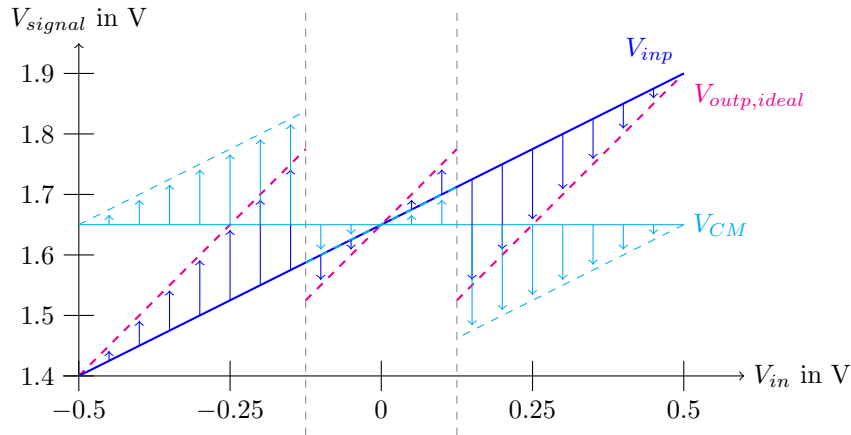


Figure 5.8.: Jumps to be made when the circuit is switching into amplification. Arrows indicate the voltage change at the middle node between the two capacitors in light blue and the voltage change at the output in blue

The parasitic capacitance of the output node is mainly entailed by the buffer, respectively the size of the gate of the source follower transistor. Also this problem was not existent in the previous designs since the buffering was inherently done by the OP-amp.

5. Pipelined ADC Design

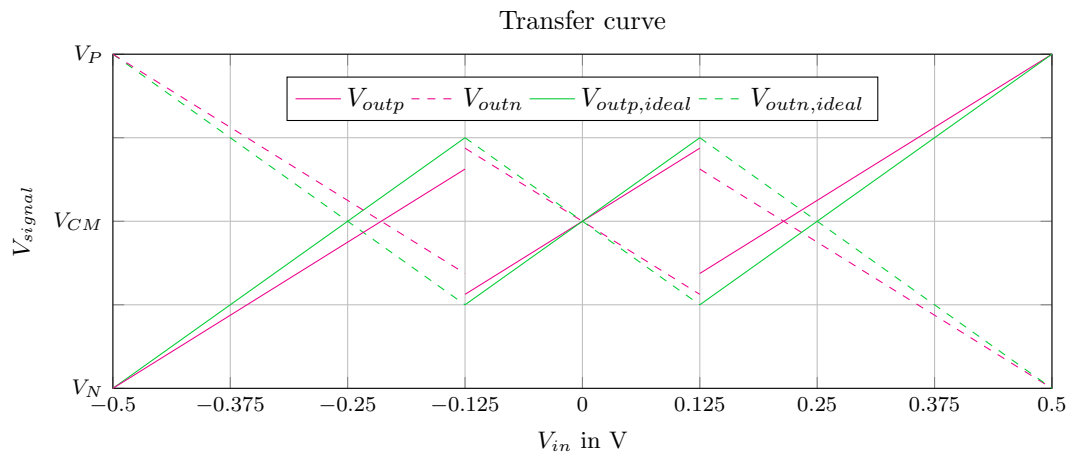


Figure 5.9.: Impact of the parasitic capacitance at the output node for $C_S = 3C_p$.

6. Switched Capacitor Basics

It has to be said that the term switched capacitor circuit is used quite generously for circuits which contain a capacitor and a switch. This quite imprecise definition makes it unclear which are the critical parameters regarding a circuit needs to be optimized. In literature authors often divided into *active* and *passive* yet they have to admit that this classification is lacking since no purely passive switched capacitor (SC) circuits exist due to the nature of the switch itself [23]. Moreover, it is also not helping to indicate the functionality and priorities in a block. To address this issue we want to distinguish between three main fields of SC circuits.

6.1. Charge Pumps

Charge pumps exploit the fact that voltages sampled on a capacitor can be stacked to reach higher values. Historically, they were introduced to generate high voltages in the direct current (DC) domain without the need of transformers and the transformation to alternating current (AC).

In integrated circuit (IC) design they gained importance because of the decrease in supply voltage to keep power consumption low. Due to the fact that the threshold voltage of a transistor is not decreasing along with the lower supply, it becomes harder to switch transistors effectively. Likewise, EEPROMs and Flash memories among other blocks, require a higher voltage than what is usually available on chip for their erase and write functions. Thus, charge pump blocks have been established to provide the necessary high voltage for some circuitry on chip [10].

Ideally, charge pumps should have a fast settling when charging up for the first time. Whereas during operation they should show a low ripple when a load is attached. Basically this means that the time constant at the input is not desired while it should be infinitely large at the output.

The priority here is to reach the desired voltage quickly after start up end then keep it as constant as possible.

6.2. Capacitor Arithmetic

By storing multiple voltage values on capacitors in a first step and connecting them together in the next it is possible to realize some simple mathematical calculations. When switched in series voltages stored on the capacitors sum up while when switched in parallel the mean value weighted with the capacitor sizes will result. With the use of an OP-amp it is further possible to achieve charge transfer from one capacitor to another. This makes division or multiplication by arbitrary factors viable.

For the sampling phase the time constant should be low to achieve a fast settling to the final value. Also in the second phase a fast charge redistribution is desired to obtain the end value of the calculation in a considerable amount of time.

However, in the sense of measuring and forwarding the result it should not be disturbed. Therefore parasitics connected to the node with the voltage potential result are critical. This is directly calling for ideal buffer stages. In contrast to the typical charge pump discussed above, buffers can be used in this case because the result potential lies within the voltage range available on chip.

For realization capacitors ratios and matching are the other factors to perform high accuracy calculation results. Another key aspect are parasitics which have to be handled in a way that their presence is not disturbing the main function too much.

Another distinction to charge pumps is that capacitors need to reach their end value during each clock cycle since in general a new signal is processed during each cycle. The focus lies on the settling accuracy at the end of each half clock cycle as the first half is required for reading in the values and the other half for computing the result.

An in-between of the so far presented concepts is constant V_{GS} -sampling where the controlling voltage for a sampling switch is modified according to the signal. This will later be discussed in 6.5.3.

6.3. Resistor Approximation

The design of operational amplifiers and filters is often calling for large resistor values which are not practically to implement on an IC. For this purpose switched capacitors are used to approximate a resistive behaviour. Another benefit is that circuit functionality becomes dependent on capacitor ratios which can be controlled much better than resistor values improving the accuracy performance [23].

It should be emphasised that this approximation is based on the properties which were undesired for the last two concepts. In case the capacitor would charge up infinitely fast and not discharge when a load is applied its equivalent resistance would always be 0 regardless of its size and the switching frequency.

6.4. Components

6.4.1. Capacitors

Depending on the process various layers and methods exist for the creation of capacitors. In the simplest case capacitors are realised by two plates above each other, a so called parallel plate configuration. The same can be done vertically, though vertical plates are actually build up by lines in different layers. Due to the production circumstances these layers are by nature insulated from each other and therefore need to be explicitly connected. Also multiple fingers interlocking in the same layer - a so called parallel wire configuration - can be used to create high capacitor values.

Since the distances between layers are much larger than the minimal structure lengths on chip it is easier to implement large capacitors placing the plates in one layer. However, when the priority is accuracy rather than size the parallel plate version is the choice.

6. Switched Capacitor Basics

6.4.1.1. Capacitor Parasitics

Since the same area between the two capacitor plates is also facing a structure above and below it, each capacitor comes with a bottom and top plate parasitic capacitance.

Due to the fact that the metal structures are located in the upper layers of the chip the distance to substrate is larger and therefore this type has smaller bottom plate parasitic capacitances. If two plate polysilicon (poly-poly) capacitors are available in the used process they are usually preferred as they show better matching and more exact absolute values.

The top plate capacitance is usually much smaller and is mainly determined by the connections lead above the capacitor. Careful lay-outing can help to keep it small.

Typical poly-poly capacitors inhibit a parasitic bottom plate of around 10-30%. In most cases certain measures have to be taken by circuit design to minimize its impact. However, possible actions are limited since each capacitance simply comes with a capacitance at one contact which is always tied to ground.

To have more possibilities in handling the parasitic plate a deep N-well (DNW) can be used. The DNW is a highly doped n-type region in the p-substrate and placed directly below the cpoly capacitor. This introduces another shielding plate so that the parasitic is not automatically grounded. The DNW introduces another parasitic, a diode to substrate, However, as long as it is kept reverse biased it usually can be neglected and we have gained the freedom to set the potential of the bottom plate capacitor.

6.4.2. Switches

The functionality of a switch is based on the creation of a conducting channel beneath the gate. The gate itself can be seen as a capacitor which is accumulating charges according to $|V_{GS}|$. The higher the voltage difference between gate and source the larger the amount of charges which build up the channel. This makes the non-ideal characteristics of a switch input signal dependent. The fact that the resistance is a function of V_{GS} is leading to distortion and therefore not desired.

On-Resistance Since it is the purpose of switching, both sides of the transistor will finally be at the same potential, respectively the input voltage. The on-resistance of a metal oxide semiconductor (MOS) transistor is then given by:

$$R_{on} = \frac{1}{K'} \frac{L}{W} \frac{1}{V_{GS} - V_T - V_{DS}} \approx \frac{1}{K'} \frac{L}{W} \frac{1}{V_{GS} - V_T} \quad (6.1)$$

As the height of the controlling voltage is limited by the supply voltage and the minimum length is limited by the process, the width is used to adjust the resistance value to meet the requirements.

$$W \geq \frac{1}{K'} \frac{L}{R_{on}} \frac{1}{V_{GS} - V_T} \quad (6.2)$$

6.4.2.1. Transmission Gate

To minimize the on-resistance dependency of the switched voltage n- and p-MOS transistors are used in parallel. Since V_{GS} has to be positive for an n-type metal oxide semiconductor (NMOS) transistor it can be considered a good switch for low voltages as a high is applied on the gate. On

the contrary a p-type metal oxide semiconductor (PMOS) transistor requires a negative V_{GS} and therefore is a good switch for high voltages when a low is applied to the gate.

6.5. Switched Capacitor Circuits in Pipelined ADC Design

As it will be shown in chapter 5 the functionality of a pipelined ADC greatly relies on how accurately a function of multiplication and summation can be performed. SC circuits for this purpose therefore clearly belong to the group of arithmetic SC circuits. Together with general chip design considerations the priorities are: fast and accurate settling, small influence of parasitics, low noise and secondary effects while using low power and area.

6.5.1. Settling Error

As the pipeline can be understood as a sampled-data switched capacitor network only the end value during each cycle has to settle to the desired value. For OP-amp based designs this influences the phase margin settings as described in [36]. Fundamentally, we have to insure that the charging process is completed sufficiently within once clock cycle which is equivalent to half the period. The relevant parameters are the resistance of the connecting path, in most cases R_{on} of the switch and the capacitor size. As last is dictated by the noise requirements we can calculate the necessary width (Equation 6.1) for a desired sampling frequency.

$$\begin{aligned}
 U_C(t) &= U(1 - e^{-\frac{t}{RC}}) \\
 pU &= U(1 - e^{-\frac{t}{RC}}) \\
 R &= \frac{-T}{2C \cdot \ln(1-p)} \\
 W &\geq \frac{1}{K'} \frac{L}{\frac{-T}{2C \cdot \ln(1-p)}} \frac{1}{V_{GS} - V_T}
 \end{aligned} \tag{6.3}$$

Where the necessary percentage p can be derived from the allowed error in stage i using

$$V_{settleerror}^i \leq \epsilon_i \cdot \frac{FSR}{2}. \tag{6.4}$$

Another crucial factor for accurate voltage settling at the end of the sampling phase are non-overlapping clock cycles. Consequently, also the clock generator circuit needs special attention.

6.5.2. Noise Considerations

As shown in [23] the noise sampled on a capacitor is independent of the resistance over which the charging took place. Instead the noise follows equation

$$\overline{V_{noise}^2} = \frac{kT}{C} \tag{6.5}$$

6. Switched Capacitor Basics

why it is often referred to as kTC-Noise. Further, it can be used to find the minimum value for a certain noise voltage.

$$\begin{aligned}
 \frac{kT}{C} &\leq \epsilon_i \cdot \frac{FSR}{2} \\
 \rightarrow C &\geq \frac{2kT}{FSR \cdot \epsilon_i} \\
 \rightarrow C &\geq \frac{2kT}{FSR} 2^{N-i+2} = 2^3 \frac{2^{N-i} kT}{FSR} \quad (6.6)
 \end{aligned}$$

6.5.3. Charge Injection

In a MOS transistor the conducting channel below the gate is build up by charges. Once the switch is turned off this channel has to dissolve and with it the charge has to leave and will mainly flow out of the drain and source. For sampling this means that at the moment when switching off additional charge is transferred, changing the voltage to which the node was previously charged.

Since the amount and polarity of charge is dependent on V_{GS} the error caused by charge injection will also be signal dependent.

Let us consider an NMOS transistor switching a capacitor like in Figure 6.1. In the on state V_{DD} is applied at the gate and the voltage over the gate capacitance is $V_{DD} - V_{in}$. Since the potential at the gate is higher, electrons build the channel. When switched off the electrons leave through the drain and source. As the direction flow of electrons is inverse to the technical current flow the voltage at the capacitor reduces. For the PMOS transistor polarities are interchanged so that the voltage finally sampled will be higher.

Now lets assume an equally sized transmission gate switching the voltage $\frac{V_{DD}}{2}$ as in Figure 6.1 (T-gate). In this case both transistors see the same $|V_{GS}|$ and will, with the same dimensions, accumulate the same amount of charge in the channel. Yet for the NMOS transistor these charges are electrons while the channel in the PMOS transistor is build up by holes. Therefore when switched off they cancel each other.

When the input voltage is higher than $\frac{V_{DD}}{2}$, $|V_{GS}|$ for the NMOS decreases while it increases for the PMOS transistor. Now the number of injected electrons will be lower than the number of holes, resulting in holes being injected and further the voltage will be higher after the switch opened.

Inversely, for an input voltage lower than $\frac{V_{DD}}{2}$, $|V_{GS,p}|$ gets lower than $|V_{GS,n}|$ which is why there are less holes injected when the switch is turned off. As a result in total we see only electrons injected which lowers the sampled voltage.

When the input voltage is plotted versus the voltage finally stored on the capacitance we receive the transfer curve of a switch. All points discussed so far coincide with the simulation shown in Figure 6.2 (a). The ideal case is a proportionality of one and marked in green.

We observe that for a transmission gate the transfer curve between the applied voltage to the voltage which is finally sampled is tilted around the middle point. This corresponds with the consideration made above. For a PMOS transistor the curve is tilted at the starting point and for an NMOS transistor at the endpoint. The pivot points are placed there where the charge injection is not changing the voltage. Either because no channel existed (for N- and PMOS transistor) or because it cancels as for the transmission gate in the middle of V_{DD} . The transfer curve of the

6. Switched Capacitor Basics

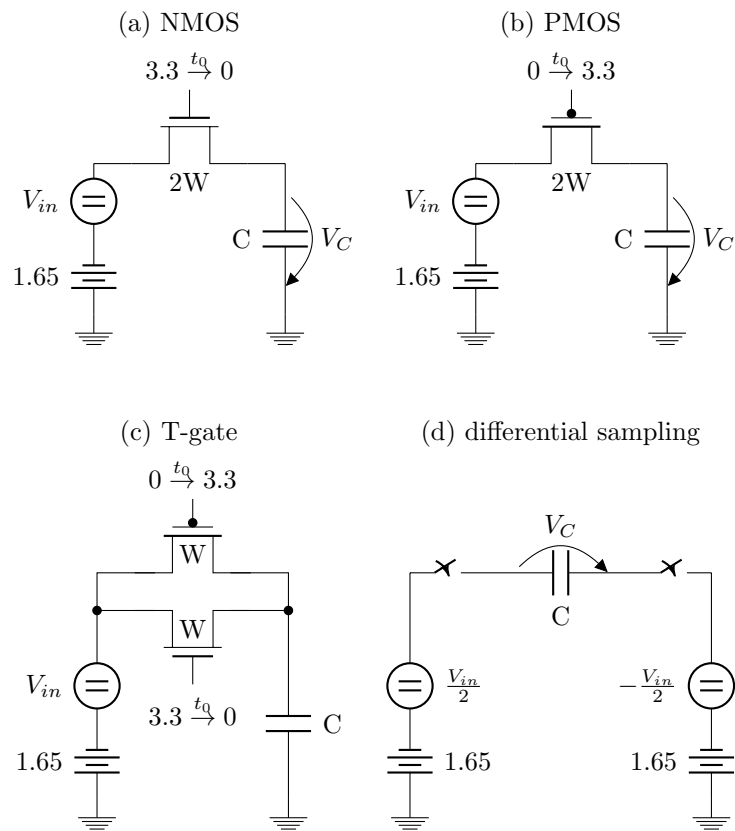


Figure 6.1.: Circuits of different switches and sampling techniques. Note that for single ended sampling the capacitors are charged from 0 to 3.3V. Yet for the differential case the switches see a voltage between 0.825 to 2.475V and the voltage stored on the capacitor ranges from -1.65 to 1.65. The corresponding simulation results can be found in Figure 6.2.

6. Switched Capacitor Basics

single transistors breaks off before reaching the pivot points as no conducting channel can be built up so that charging the capacitor was not possible at all.

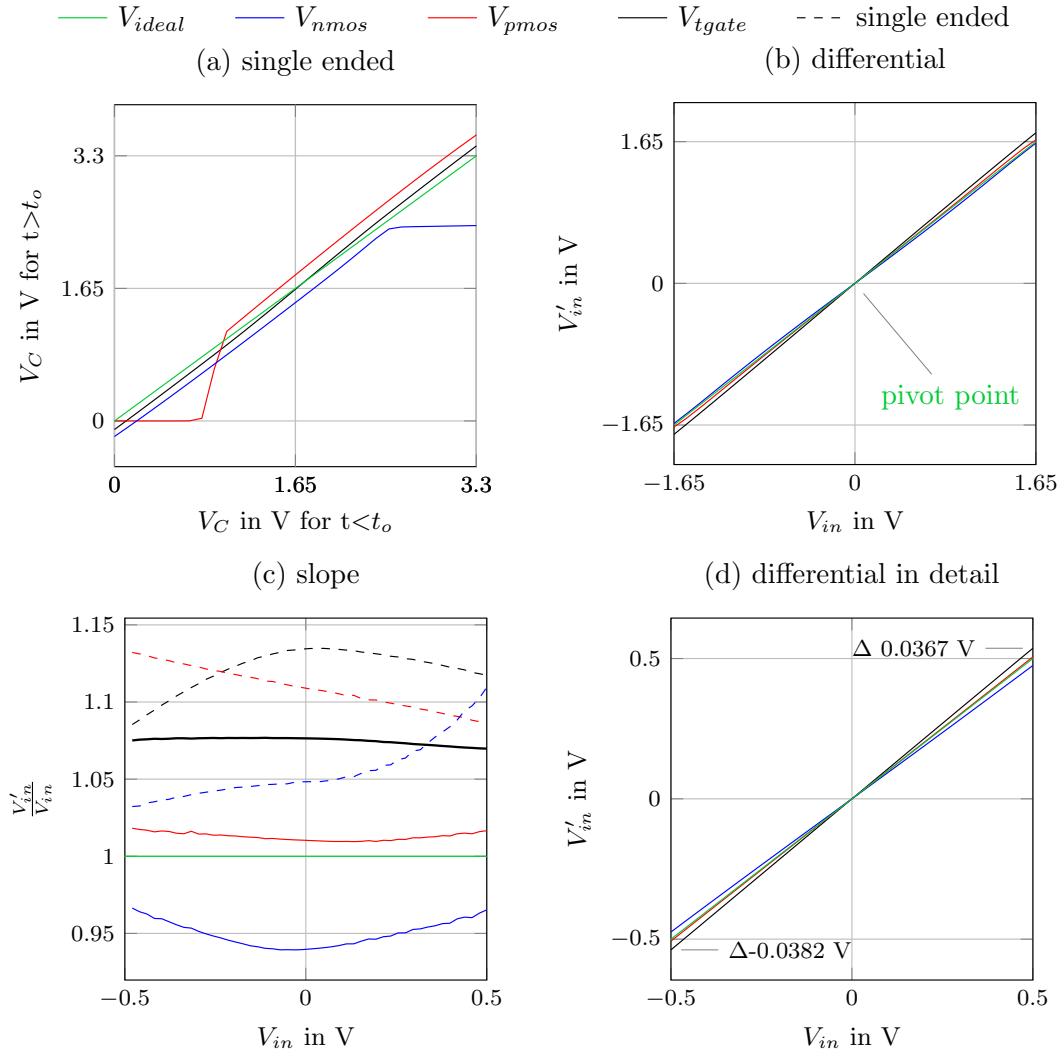


Figure 6.2.: Transfer curves for different switches and sampling techniques shown in Figure 6.1 for $L = 0.35\mu\text{m}$, $W = 10\mu\text{m}$ and $C_S = 100\text{fF}$.

To summarize we can say the better a switch was conducting the more charge will be injected when it is switched off. For single ended sampling an NMOS transistor decreases and a PMOS transistor increases the just sampled voltage. For a transmission gate the better conducting transistor type dominates. So above the middle of the controlling voltage the sampled voltage will be higher, below it lower.

For differential sampling, shown in Figure 6.2 (b), a charge injection cancels regardless of the type of the switch when $V_{inn} = V_{inp}$ (the sampled voltage is zero). In other cases things become a little bit more complex because of the time dependency.

For two NMOS transistors loading a capacitor the transistor switching the higher voltage sees

6. Switched Capacitor Basics

the smaller V_{GS} and therefore switches off first when the voltage at the gate drops. At the time when the electrons of the switch from the other side want to leave there is already no current path through the capacitor and these charges will take another low ohmic path. The overall resulting current is therefore lowering the sampled voltage as indicated in Figure 6.3.

Again the same applied reversely for a PMOS transistor but since the mobility of holes is much less than of electrons the effect is not as pronounced as we can also see in Figure 6.2 (b), and detailed in (d).

For a transmission gate in differential sampling the slow PMOS transistor is keeping up the current path through the capacitor longer than both NMOS transistors need to switch off. Why in this case the charges from both NMOS transistors can pass through the capacitor resulting in a total technical current against the direction of the majority of electrons. The sampled voltage will finally be increased.

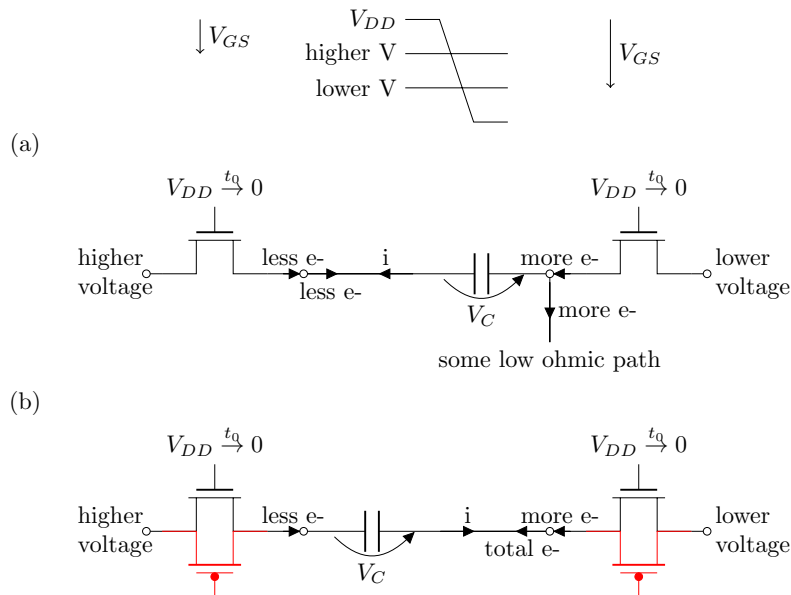


Figure 6.3.: Investigation of charge injection for differential sampling. (a) Due to the fall time of the clock the electrons in the transistor with the higher V_{GS} see no path through the capacitor when they leave the gate channel. (b) The slow PMOS transistor is keeping the path open for longer allowing the electrons from both sides to pass.

6.5.3.1. Bottom Plate Sampling

One way to deal with charge injection is bottom plate sampling. For sampling in a differential circuit the two sampling capacitors are individually connected to the same potential over a second switch. This switch is opened first, injecting the same charge on both capacitors. This error has a common mode character and will further be suppressed in a differential circuit. When disconnecting from the input signal the charge will not flow through the capacitors but through another low ohmic path.

6. Switched Capacitor Basics

6.5.3.2. Constant V_{GS} Sampling

Another method to reduce signal dependency is to modulate the controlling voltage with the signal voltage. To achieve this the input voltage is previously sampled and then either added to VDD or subtracted from the ground level to reach a constant V_{GS} for both transistor types. Also this approach needs either switches on both sides of the sampling capacitor or transmission gates. When the transistors are switched off, the same amount and polarity of charge would be injected from both sides or the different polarity but same amount would be injected from one side. As a result, in both cases they cancel each other leaving the voltage unchanged.

6.5.3.3. Dummy Switch

A shorted dummy switch placed in series to the real switch can be used to absorb the injected charge. To do so it is turned on exactly when the real switch is turned off. To make sure that the dummy is exactly compensating it is usually sized half of the real switch for the model that half of the charge will leave through each side of the transistor. For this assumption to hold it has to be made sure that the main switch is facing same environments on both sides. Immediately this means that the sampling capacitance, which tends to be large, has to be placed once again just for error compensation.

Part II.

Findings

7. Improvements for the C+C Charge Pump MDAC

In the topology used in [2] and presented in subsection 5.5.3, the most severe error is caused by the bottom plate capacitances which appear at the middle node. A simple option for improvement is to turn C_1 so that at least one of the larger bottom plate capacitances is placed at an uncritical node. As this introduces unbalance in the system this is not a first choice.

After the first phase the parasitic capacitors, C_p in Figure 7.1 at the middle node are charged to the common mode of the input. When the circuit goes into the second phase this node is driven over capacitance C_1 . Therefore this capacitance experiences charge redistribution and the voltage sampled on it reduces significantly which causes an error of the multiplication by two.

As explained in subsection 6.4.1.1 DNWs can be used to shield the bottom plate. Yet the question is which voltage V_X and V'_X should be applied for shielding during the two phases.

The idea is to look at the parasitic network attached to the critical node and try to set the voltage of the DNW in a way that this parasitic network leaves the rest of the circuit unchanged. This is reached when the charge inside the parasitic network stays constant throughout the two clocking phases. The according calculations are carried out in section A.1. Here only the results should be discussed.

$$V_X = V_{CM} \qquad V'_X = V_{ADD} - \frac{V_{in}}{2}$$

The first solution is trivial and would mean to set the DNW to the same potential as the critical node. The capacitive coupling would have no effect. Setting V_{CM} during the sampling phase would be no problem. Nevertheless, $V_{ADD} - \frac{V_{in}}{2}$ is a potential which is not present in the system. Actually, it is part of what we are trying to create. It could be realised with another sampling capacitor as C_1 which is just used to drive the DNW in the second phase. This would imply building half of the circuit only to provide the shielding for the parasitics. Indeed, simulation results showed improvement but yet it is an unsatisfactory solution requiring too much effort for what is gained. In addition it has to be considered that this capacitor also suffers from charge sharing and will not really drive the DNW.

The second solution is however more feasible.

$$V_X = V_{CM} - \frac{V_{in}}{2} \qquad V'_X = V_{ADD}$$

Though it might not be clear at first sight, both voltages are present in the circuit. During the amplification phase the comparator has already made its decision and the correct V_{ADD} is available. $V_{CM} - \frac{V_{in}}{2}$ on the other hand is nothing else than V_{inn} in case of the p-channel.

It is interesting to note that to set these voltages just a single additional connection (marked in red) is required. Taking a closer look at this connection it can be understood why it is improving

7. Improvements for the C+C Charge Pump MDAC

the behaviour significantly. In fact it is switching the two bottom plate parasitic capacitors in parallel with C_1 . This is acceptable because as derived in Equation A.11 capacitor sizes and matching have no influence as long as the buffers input impedance is large compared to the sampling capacitance. Actually, the error is reduced as the size of one sampling capacitor is increased.

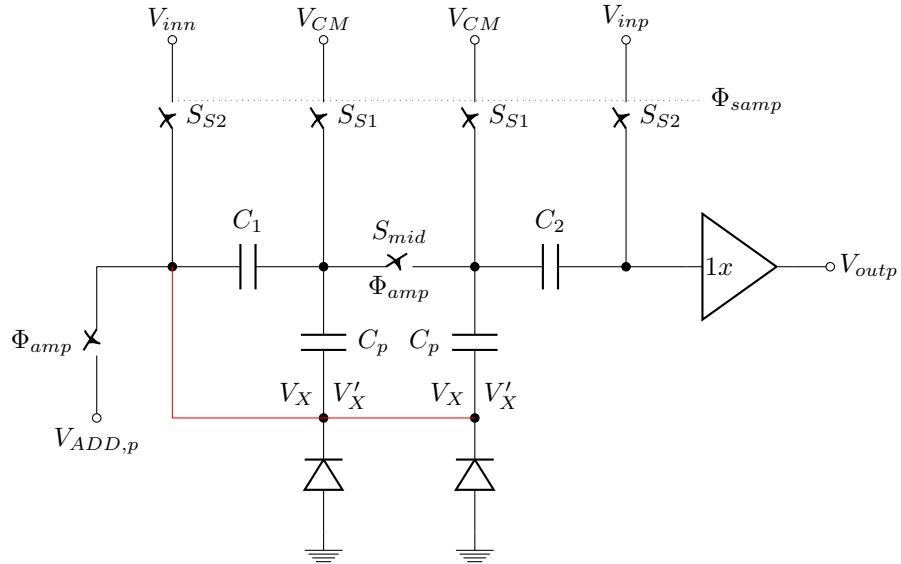


Figure 7.1.: Shielding for the bottom plate capacitors for the C+C MDAC [2]

It has to be mentioned that the DNW creates another parasitic, a diode, with the substrate. However, the diode will be strongly reverse biased during operation so its capacitance will be quite constant and more importantly, small, according to [12].

8. Differential Gain MDAC

Usually most circuit concepts are first created single ended. Later they are adapted to work fully differential to make them more common mode resistant. In a single ended system it is necessary to sample the same voltage on two capacitors to be able to create a multiplication by two when adding these voltages.

In a fully differential system the voltage difference needed for a gain of two is already present. Differential signals are defined as the difference between two single ended signals [29]. The single ended signals are created by either adding or subtracting half of the input from common mode. Therefore, a gain of two can be realised by sampling this voltage difference on one capacitor and use it to generate the differential signal again, but this time with twice the amplitude in regard to V_{in} .

8.1. Functional Description

In Figure 8.2 the circuit is shown for both channels of the differential signal path. The clock signals correspond to Figure 8.1 where the signal generation is illustrated for V_{outp} . During the first phase the capacitors are connected to V_{in} . The voltage stored on the capacitor is indicated by the arrows in Figure 8.1. In amplification phase this voltage is then added to the corresponding reference voltage V_{ADD} which are highlighted by thick black lines. This creates *one* single ended signal for one channel. In doing so the differential signal at the output is then proportional to $2V_{in}$. Hence, a gain of two has been established.

The mathematical equations for the voltage signals are given in the following table distinguishing the three different regions.

		$V_{inp}^{i+1} =$	$V_{inn}^{i+1} =$	$V_{in}^{i+1} =$
for	$V_{in}^i > V_{thp}$	$V_{in}^i + V_N$	$-V_{in}^i + V_P$	$2V_{in}^i - \Delta V$
for	$V_{thN} < V_{in}^i < V_{thp}$	$V_{in}^i + V_{CM}$	$-V_{in}^i + V_{CM}$	$2V_{in}^i$
for	$V_{in}^i < V_{thN}$	$V_{in}^i + V_P$	$-V_{in}^i + V_N$	$2V_{in}^i + \Delta V$

For comparison, the differential gain approach can be attached with Figure 8.3 to the table of possible MDAC solutions (Figure 5.6).

8. Differential Gain MDAC

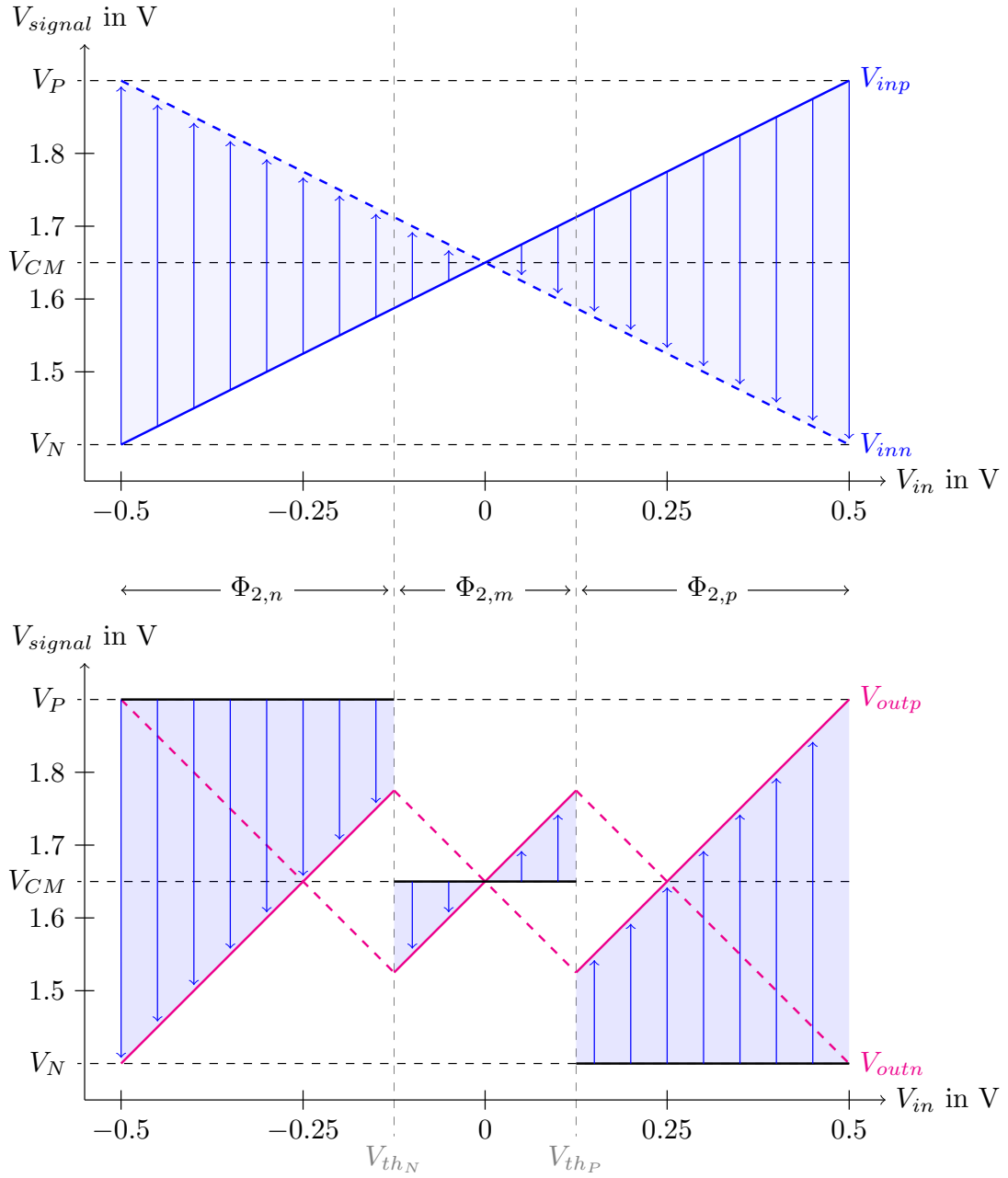


Figure 8.1.: Using the differential inputs to generate a gain of two for the MDAC. Above arrows indicate the voltage sampled on the capacitor. Below shows how the output signal is constructed adding the sampled voltage to the right reference.

8. Differential Gain MDAC

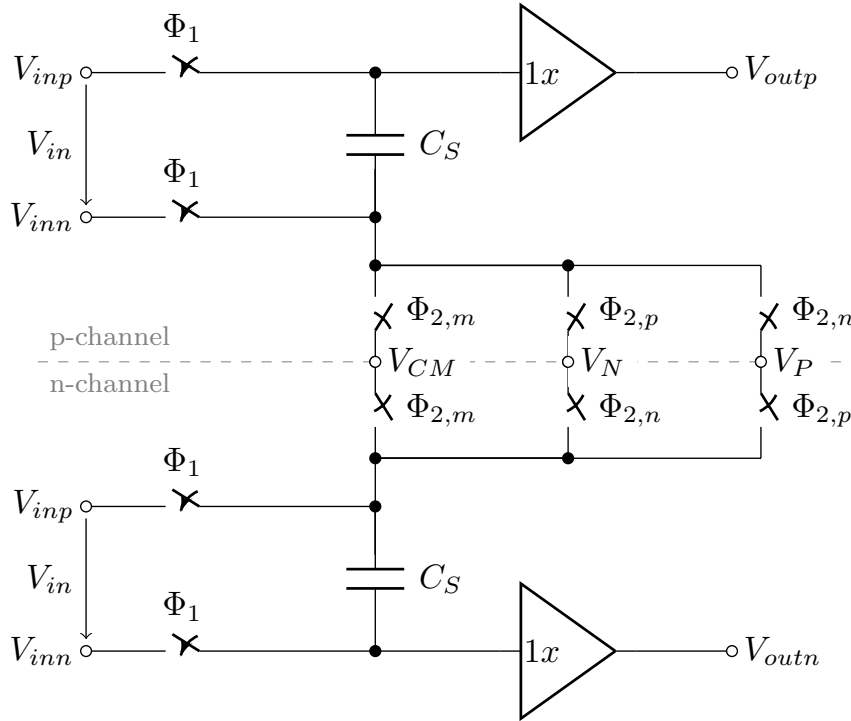


Figure 8.2.: Circuit for the differential gain MDAC

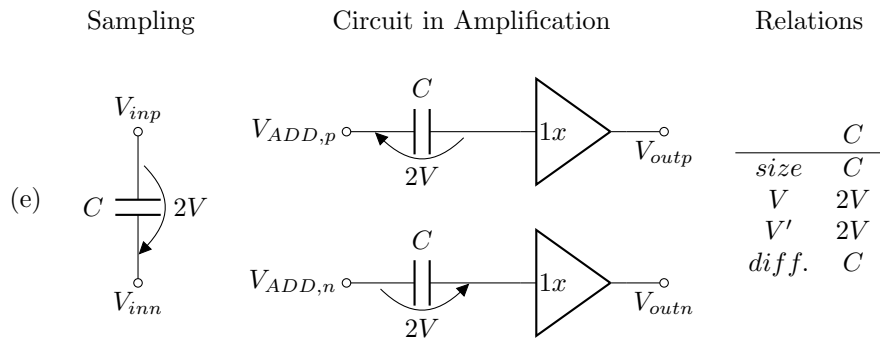


Figure 8.3.: Adding the differential sampling approach to the prior art MDACs summarised in Figure 5.6.

8.2. Advantages

This way to implement the gain has multiple benefits.

First of all the only remaining bottom plate capacitance can be connected to a node which is driven in both clock cycles (V_{in} during sampling and V_{ADD} during amplification). This means that the problems caused by this parasitic literally disappear.

Moreover, the circuit as a whole is reduced in complexity, with just two out of five switches and only one capacitor remaining to realise the same function. There is also no need for the special clocking which was required by bottom plate sampling. The impact of charge injection on this topology will be discussed later. Further, the middle switch is eliminated whose dimensioning was a trade off between settling and gain error [3].

Another significant benefit compared to the adding approach with two capacitors is that the effective capacitor size towards the parasitics of the buffer is larger. This can be explained by the fact that capacitances in series reduce in total size ($X_C + X_C = X_{\frac{C}{2}}$). Consequently, this approach can be realized in a considerably smaller area with better performance. The mathematical derivation is provided in Equation A.15 showing that for the same error only half the capacitor size is needed. Additionally, this capacitance is only placed once. As a result the area occupied by sampling capacitors reduces by a factor of four for the same error compared to the old design.

Like for the approach with two capacitances the gain is created before the buffer which is lowering the buffer noise when referred to the input [3].

Yet another minor advantage is that only one switch on-resistance is in the charging path of the parasitic capacitance when the circuit is in amplification phase.

8.3. Error Analysis

8.3.1. Charge Injection

The approach of bottom plate sampling can not be used any more to handle the error caused by charge injection. An alternative could be constant V_{GS} sampling or the use of dummy switches.

Besides, some theoretical investigations were made on the exact influence charge injection has on this topology. For this purpose we focus on the positive side of V_{in} since the behaviour is symmetric around the zero point. Note that the error is exaggerated here to make the plots more illustrative.

In subsection 6.5.3 it was shown that charge injection is increasing the absolute value of the sampled voltage when sampling differentially. Basically this can be interpreted as a gain greater than one, which was also shown in the according diagram (Figure 6.2) where the transfer curve of the switch showed a slope of 1.08. See Figure 8.4 how this is further influencing the created output signals.

In principle the transfer lines are tilted around the zero point to become steeper. Recalling from before we know that charge sharing has the opposite effect, it is reducing the gain. Indeed it would be nice if one evil could be fixed by another. Unfortunately, this is not working because a larger switch is also adding capacitance at this node and the impact of charge injection is way smaller than that caused by charge sharing.

8. Differential Gain MDAC

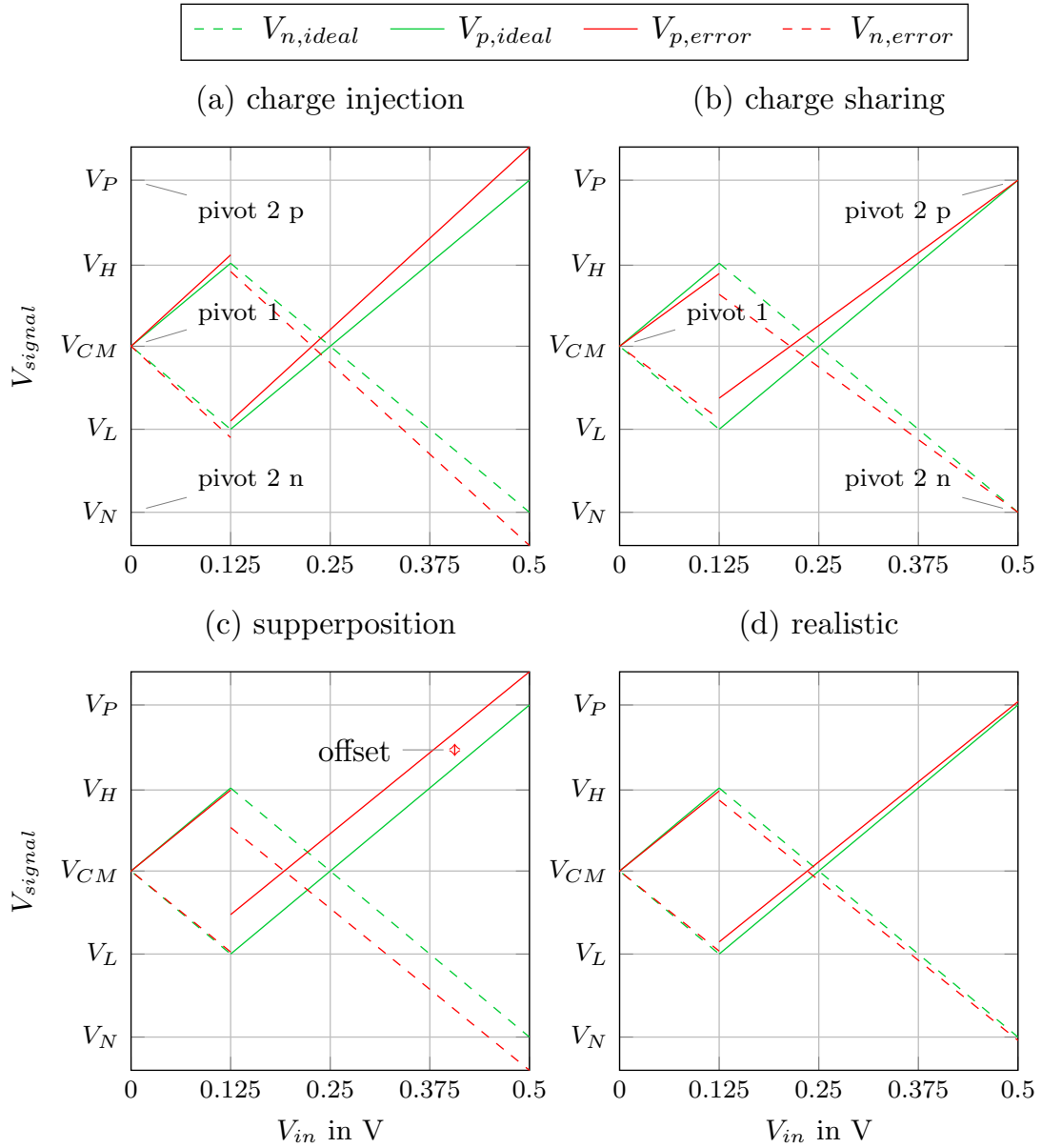


Figure 8.4.: (a) Voltage after sampling phase, due to charge injection the sampled voltage on the capacitor was higher as it should be. (b) Demonstrates only the impact of charge sharing for a proportionality factor of $m=3$. (c) The two effects from a and b superpose in amplification phase. For the chosen values the two effects cancel each other in the middle region and leave a constant offset in the upper region. (d) Same as c but for more realistic values where the effect of charge sharing is dominant $m=20$.

To summarize we now want to conclude which error remains if we already take into consideration that the capacitor will face charge sharing in amplification phase. Since in the middle region the two pivot points fall together charge injection is actually working against the charge sharing error. For the upper and lower region the error functions have different pivot points why as a result additionally a constant error is introduced. Regarding its height we can consider the transfer curve of a switch introduced in subsection 6.5.3. For the corresponding voltage range $V_{in}=\pm 0.5\text{ V}$ the derivation from the ideal curve (even for a poor ratio between capacitor and switch size ($W=10\ \mu\text{m}$, $C_S=100\ \text{fF}$)) is minimal. Finally, we can state that for all regions the input voltage dependent part of the charge injection error should be of no concern and actually has positive effects in reducing the negative gain error. For the upper and lower region an offset will be introduced.

8.3.2. Voltage Divider at the Output Node

The change in circuitry minimized the problem of charge redistribution at the output node. Though the voltage divider is still the main problem in order to reach sufficient gain accuracy.

To reduce the error according to Equation A.14, the sampling capacitance needs to increase. This is immediately calling for larger switches (to have a lower resistance for the same time constant) and a higher g_m for the buffer which has to load the next stage. Even worse, both of these actions will add even more parasitic capacitance to the mentioned node. Additionally, larger switches increase the effect of charge injection so that this action is limited.

The g_m can of course also be increased by spending more current in the stage, but at a certain point this becomes inefficient without increasing the width of the source follower transistor. Likewise this is not in the sense of a low power application.

We can conclude that a certain accuracy for a given technology might only be reached for a limited sampling frequency.

8.3.3. Capacitor Mismatch

As only one capacitor is used to create the gain, mismatch for one channel is no issue at all.

Non-ideal matching between the channels leads to different gain errors in the channel. As the signal is transmitted differentially this is uncritical and can be interpreted still as an overall gain error.

Indeed, it will violate the definition that differential signals are exactly equal and opposite to each other so that we can not assume that currents through ground will cancel [5]. With a return signal through ground electromagnetic interference (EMI) may become an issue.

However, as we anyway aim to kept the gain error small, capacitor mismatch will have minor consequences and is not a primary concern.

8.3.4. Current Mismatch between Channels

Current mismatch between the two channels leads to different voltage shifts in the source followers since:

$$V_{GS} = V_T + \sqrt{\frac{L \cdot I_d}{W \cdot K'}}$$

This would directly influence the differential signal and must be prevented. Matching the buffer circuits of both channels is therefore highly important.

8.4. Dimensioning and Design

8.4.1. Capacitor and Switch Sizes

Capacitor sizes must be set above the kTC-noise limit in Equation 6.6. Together with the wished operating frequency the switches must then be dimensioned for settling using Equation 6.3 and Equation 6.4

For an N bit ADC the R_{on} for sufficient settling can be given by [31]

$$R_{on} \leq \frac{1}{2.5 \cdot (N + 2) \cdot C \cdot \log(2)} \quad (8.1)$$

$$\frac{1}{K'} \frac{L}{W} \frac{1}{V_{GS} - V_T} \leq R_{on} \leq \frac{1}{2.5 \cdot (N + 2) \cdot C \cdot \log(2)} \quad (8.2)$$

$$\frac{L}{K'} \frac{2.5 \cdot (N + 2) \cdot C \cdot \log(2)}{V_{GS} - V_T} \leq W \quad (8.3)$$

8.4.2. Stage Scaling - Unity Gain Cell

To simplify the use of stage scaling the MDAC was designed by small unity cells. In the first stages of the pipelines these unity cells were then placed multiple times while the number decreased until the last stage, which only consisted of one single cell.

For layout the aim is clearly to reach a very symmetric block for both channels while keeping the parasitics at the buffer input as small as possible.

8.4.3. Buffer Design

To dimension the buffer we have to consider the load it has to drive. For this purpose the situation is shown for the two topologies in Figure 8.5. Whereas in the C+C charge pump each buffer has to load two times C_S against V_{CM} , the load capacitance is given by $C_p + 4 \cdot C_S$ in the proposed design. This can be explained by the fact that the capacitance $2C_S$ is mounted between the two outputs. While one channel output tries to increase its output potential, the potential on the other side is lowered by the other buffer. Essentially, this is the same effect as for a Miller capacitance, where the feedback capacitance appears larger because the transistor is lowering its drain potential for a rising input. Since in this case the potential on one side is rising in the same amount as the other side falls, the capacitance is enlarged by a factor of two.

8. Differential Gain MDAC

For verification we use the Miller Theorem [6, p.171]:

$$V_1 = V_{CM} + \frac{V}{2} \qquad V_2 = V_{CM} - \frac{V}{2} \qquad V_2 = -AV_1$$

$$\frac{V}{2} = -A \frac{V}{2} \qquad \rightarrow A = 1$$

$$C_1 = (1 + A)C \qquad C_2 = (1 + \frac{1}{A})C$$

$$C_1 = 2C \qquad C_2 = 2C$$

$$V_X = V_1 + \frac{C_2}{C_1 + C_2}(V_2 + V_1) = V_{CM} + \frac{V}{2} - \frac{1}{2}V = V_{CM}$$

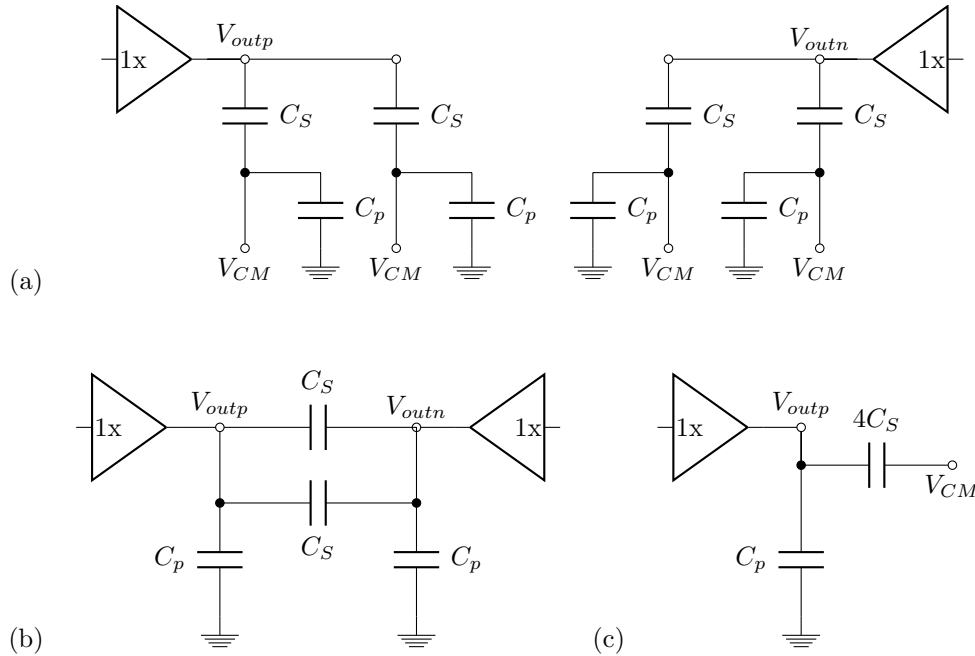


Figure 8.5.: Comparing the load of the two topologies (a) and (b). Further showing the equivalent circuit in (c) the buffer has to drive in the case of (b).

Similarly, we can see in the bode plot in Figure 8.6 that the real circuit shows the same progressive form as the equivalent circuit with four times the load capacitance. With only two times C_S as a load the resulting bandwidth is too high.

From $f=10^9$ Hz onwards, the phase of all three curves is identical because the zero is determined by $\omega_z = \frac{g_m}{C_{gs}}$. Since all circuits inhibit the same source follower transistor the phase change appears at the same frequency. For high frequencies above $f=10^{10}$ Hz the amplitude settles as the transistor is now subjected by its parasitics and the circuit becomes a capacitive divider. This is yet another confirmation for the load capacitor size which has to be expected.

8. Differential Gain MDAC

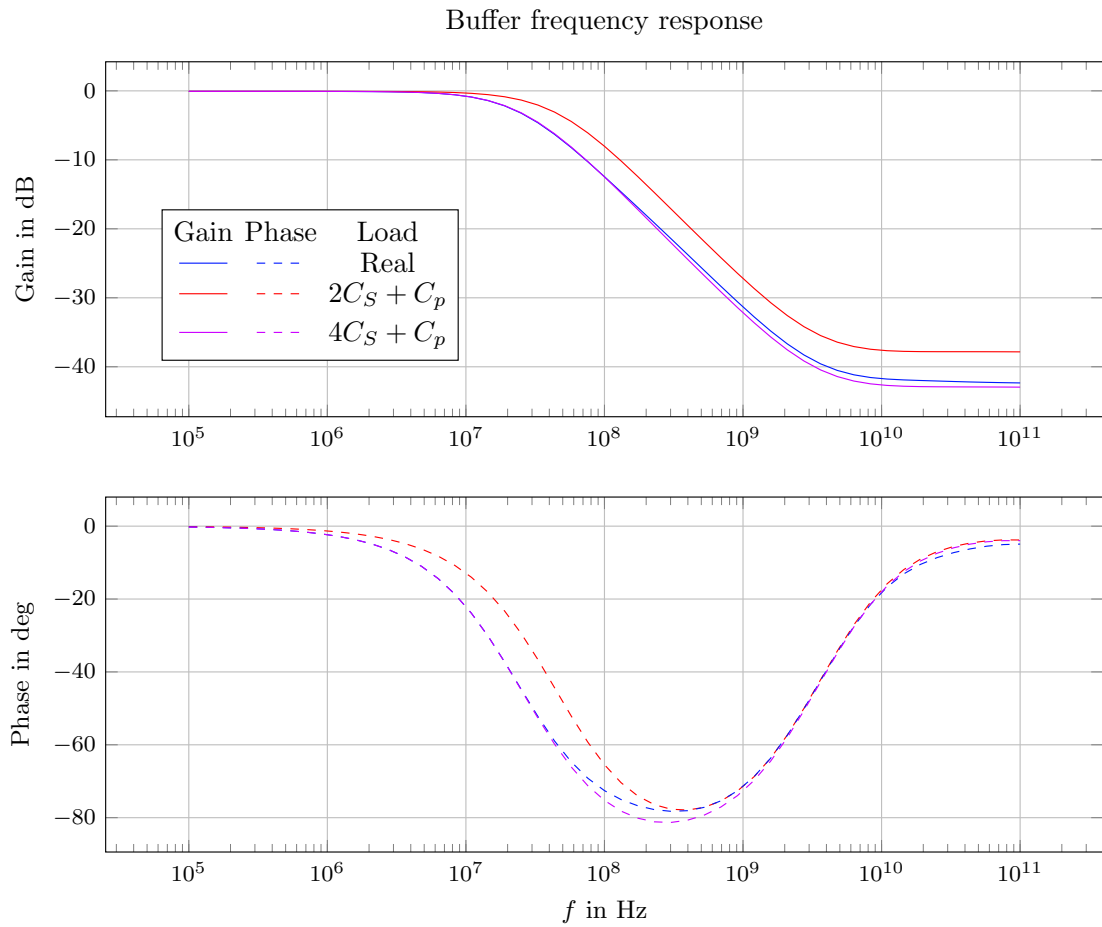


Figure 8.6.: Transfer characteristic of the buffer for different loads. Proving that the buffer indeed sees a capacitance of $4C_S + C_p$ as shown in Figure 8.5 (b)

8.5. Conclusion

To end this chapter we want to summarize the differences between the C+C charge pump and the proposed topology using differential gain. There are three main points where these two approaches differ. First, the capacitor value needed per stage and channel determines how much area is occupied on chip. Second, the capacitor value which forms the voltage divider with the parasitic of the output buffer is relevant for the gain error. And third, the effective capacitor value which has to be loaded by the output buffer. Considering no downscaling these values are summarized in Table 8.1. (Refer to Figure 8.5 for the according schematics.)

Capacitor size: relevant for:	of C_S	total per channel Area on Chip	for Voltage Divider Gain error	of the effective Load Buffer Design/Speed
C+C Charge Pump	C	$2C$	$\frac{C}{2}$	$2C$
Differential Gain	C	C	C	$4C(+C_p)$
Differential Gain	$2C$	$2C$	$2C$	$8C(+C_p)$
Differential Gain	$\frac{C}{2}$	$\frac{C}{2}$	$\frac{C}{2}$	$2C(+C_p)$

Table 8.1.: Comparing the effective capacitor values at different parts in the circuit. Note that C_p is the bottom plate capacitance of the chosen C_S . (See Figure 8.5 for the schematics)

Hence, we can state that the differential gain approach can be built four times smaller for the same gain error and almost same load requirements. Additionally, the parasitic bottom plate has to be loaded which is a reasonable trade-in because we eliminated its negative impact during amplification.

If C_S is chosen the same, the gain error and the area needed on chip reduce by a factor of two while the challenge is moved to the buffer which has to drive twice the load. This means passive component size on chip can be replaced by buffer efficiency. Often this is beneficial considering the fact that active circuitry can be built cheaper on ICs [12, p.170].

Besides, we can conclude that the negative effect of parasitic capacitances was exchange by the error introduced by charge injection.

Overall, the differential gain MDAC could be a good option for lower speed ADCs as a very compact and small solution.

9. Error Compensations

The voltage divider at the output node is limiting the use of capacitor based gain stages with a unity gain buffer to low resolutions due to the achievable accuracy. To overcome this problem systematically rather than just investing progressively more to achieve a fraction of improvement, attempts to correct the error will be explored next.

9.1. Analog Error Correction

The parasitic capacitance is diminishing the gain from its ideal value. In other words the voltage exiting the stage is a fraction too low as it should be. The idea would be to reproduce this missing voltage to be able to add it again in the next stage. It is sufficient to do the summing in the next stage since the high gain accuracy requirements are only necessary for the signal propagation through the pipeline.

Error reproduction could be done by setting up an additional stage with an even worse stage gain. Then the voltage difference between the two non-ideal outputs might be adjusted to equal the voltage difference between the ideal and the non-ideal voltage. In the next stage it would then be possible to add this missing voltage using a capacitive voltage summer like in the old design.

The difference is that now the whole signal and multiplication is accomplished by one capacitor while the other is just repairing the error. Therefore the charge redistribution at the middle node is not so critical. Overall this leads to a better result because at least a part of the error can be emended.

Next various methods and their feasibility will be explored. The question is how this can be achieved and whether it can be controlled. While deriving the dimensioning only half of the transfer curve will be taken into consideration since the other half is mirrored around the y-axis.

In Equation A.13 we derived the output voltage of the stage dependent on the ratio between sampling capacitance and parasitic capacitance where $C_S = mC_p$. For the following conditions we will refer to the voltage exiting the main path as $V(m)$ and the voltage exiting the emending path as $V(e)$. Basically, these voltages are straight lines with a slope dependent on the capacitor ratio.

9. Error Compensations

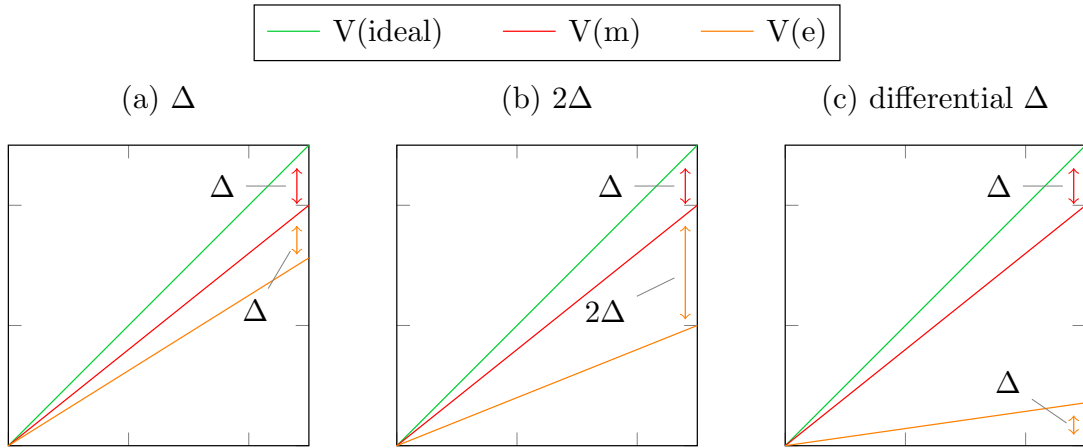


Figure 9.1.: Illustrating ideas to correct the error due to charge sharing with a second, also non-ideal emending path.

9.1.0.1. Δ Emending Path

Probably the most straight forward solution to fix the error in the next stage is to reproduce exactly the same. Or in other words create a voltage which has the same error referred to the "good" main signal than this has to the ideal. With the diagram in 9.1 (a) we can set up the following equations.

$$\begin{aligned} V(\text{ideal}) &\stackrel{!}{=} V(m) + (V(m) - V(e)) \\ V(\text{ideal}) &\stackrel{!}{=} 2V(m) - V(e) \\ V(\text{ideal}) &\stackrel{!}{=} MV(m) - E(e) \text{ for } M = 2, E = 1 \end{aligned}$$

According to A.20 a solution exists and e can be calculated.

$$e = \frac{E}{M} (m + 1) - 1 = \frac{m - 1}{2} \quad \rightarrow e_{m \gg} \approx \frac{1}{2}m$$

The C_S to C_p ratio for the emending path is converging towards one half of the ratio in the main stage if the main stage is almost ideal. Since this is anyway what we want to achieve the result would be reasonable. The proportionality $\frac{e}{m}$ is also plotted in Figure 9.2 along with the derivative which is indicating that this proportionality tends to be constant for a high m. The factor between the two paths could easily be implemented by placing just half the sampling capacitance in the emending path.

The disadvantage of this idea is that three capacitances are required in the next stage to assemble the correct signal. Further three capacitors in series would decrease the effective capacitance in regard to the parasitic by a factor of three. This would make matters worse in the next stage and is therefore not a good option.

9. Error Compensations

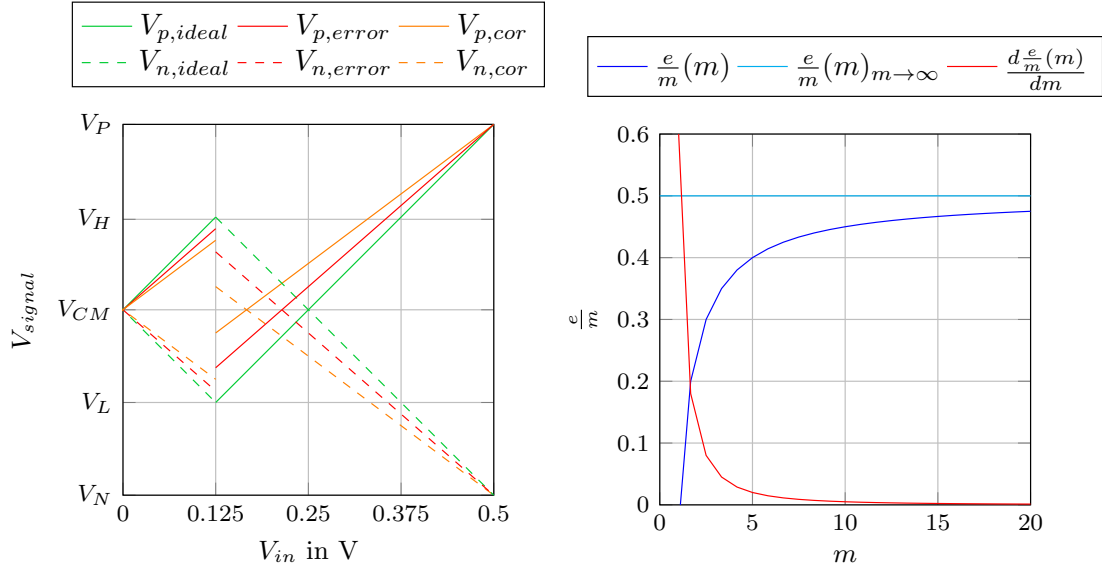


Figure 9.2.: Showing the signals for *Delta* correction on the left and the necessary proportionality between the two paths on the right. For a good main path ($m \gg \frac{e}{m}$) is converging towards 0.5 and the derivative stays constant.

9.1.0.2. 2Δ Emending Path

As we have seen just before it is desirable to create a correcting voltage already twice as large to spare a second correcting capacitor in the next stage. To do so we simply create twice the error because the other differential channel is lacking the same voltage to the ideal output voltage.

$$V(ideal) \stackrel{!}{=} V(m) + \left(\frac{V(m) - V(e)}{2} \right)$$

$$V(ideal) \stackrel{!}{=} \frac{3}{2}V(m) - \frac{1}{2}V(e)$$

$$V(ideal) \stackrel{!}{=} MV(m) - E(e) \text{ for } M = \frac{3}{2}, E = \frac{1}{2}$$

Again according to A.20 a solution exists and e can be calculated.

$$e = \frac{E}{M} (m + 1) - 1 = \frac{m - 1}{3} \rightarrow e_{m \gg} \approx \frac{1}{3}m$$

Now the emending path has to be three times as bad as the main path for the main path being almost ideal. Like before for a good main path the factor between the paths is converging and stays constant. The proportionality between the two paths can be reached most easily by scaling the sampling capacitor with e while everything else stays the same. When implemented it can be considered to choose the factor even smaller than $\frac{1}{3}$ because first of all m is not infinite and secondly the correcting capacitor in the next stage will also loose some charge at the middle node.

9. Error Compensations

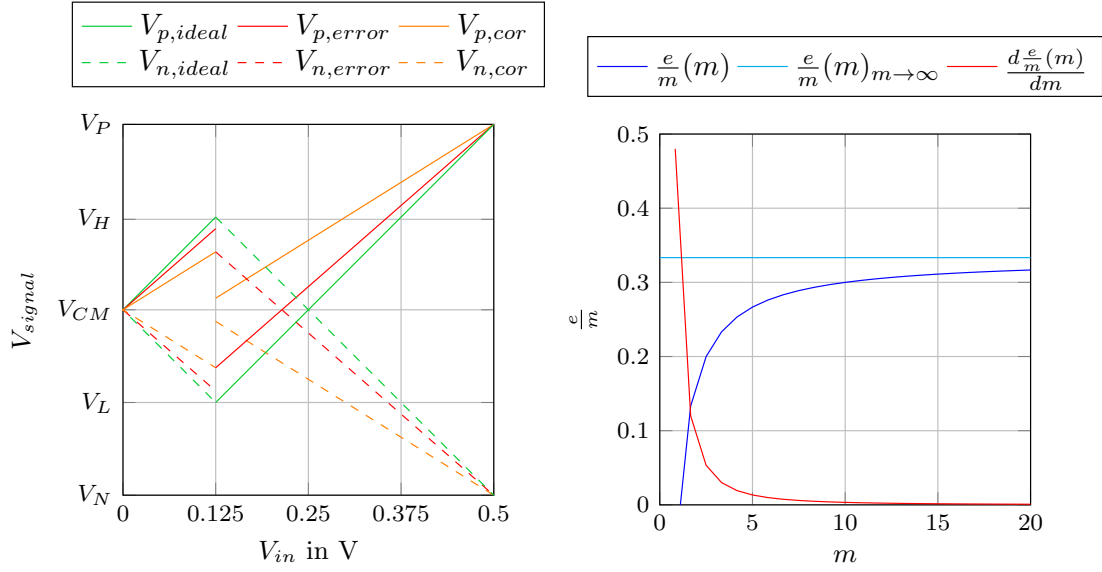


Figure 9.3.: Setting up a second path with the twice the error between the main and emending path.

9.1.0.3. Differential Δ

Here once again we try to exploit the existence of differential signals. For this approach we would like to create a path which is just generating what the other main stage is missing.

$$\begin{aligned}
 V(ideal) &\stackrel{!}{=} V(m) + (V(e) - V_{CM}) \\
 V(ideal) + V_{CM} &\stackrel{!}{=} V(m) + V(e) \\
 2V_{in} + V_{ADD} + V_{CM} &\stackrel{!}{=} V(m) + V(e)
 \end{aligned}$$

Solving the Equation A.19 we have to face the fact that no solution exists as e and m have to stay positive. This can be explained by two misceptions. First in proposing the idea in Figure 9.1 we only considered the conditions in the middle range. In Figure 9.4 we can see that this approach will not work for the upper region.

Even in the middle region there exist just one solution for $e = m, e \rightarrow 0, m \rightarrow 0$. When switching two loaded capacitors in parallel the resulting voltage can never go below the lowest voltage loaded on one of the capacitors. As it is impossible to reach a voltage above $2V_{in} + V_{ADD}$ it is just as well impossible to reach a voltage below V_{inp}

9. Error Compensations

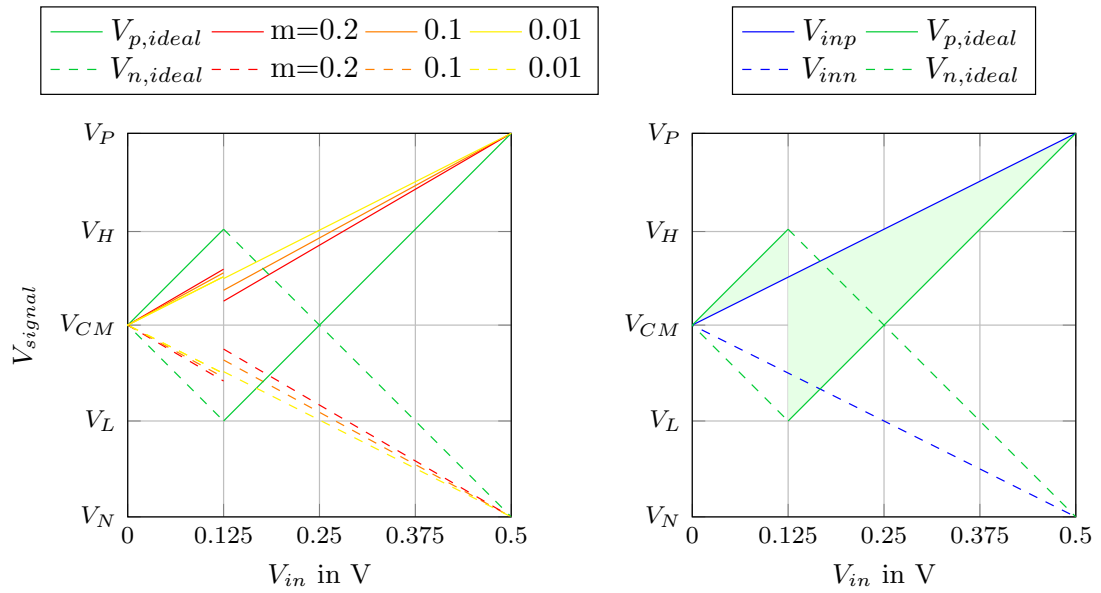


Figure 9.4.: Showing that the output is converging to the input voltage when the sampling to parasitic ratio becomes worse. Left the physical possible range for the output is shaded in green.

10. Results

10.1. Comparison between Different Gain Stages

In Figure 10.1 the different discussed topologies avoiding OP-amps are compared. C+C refers to

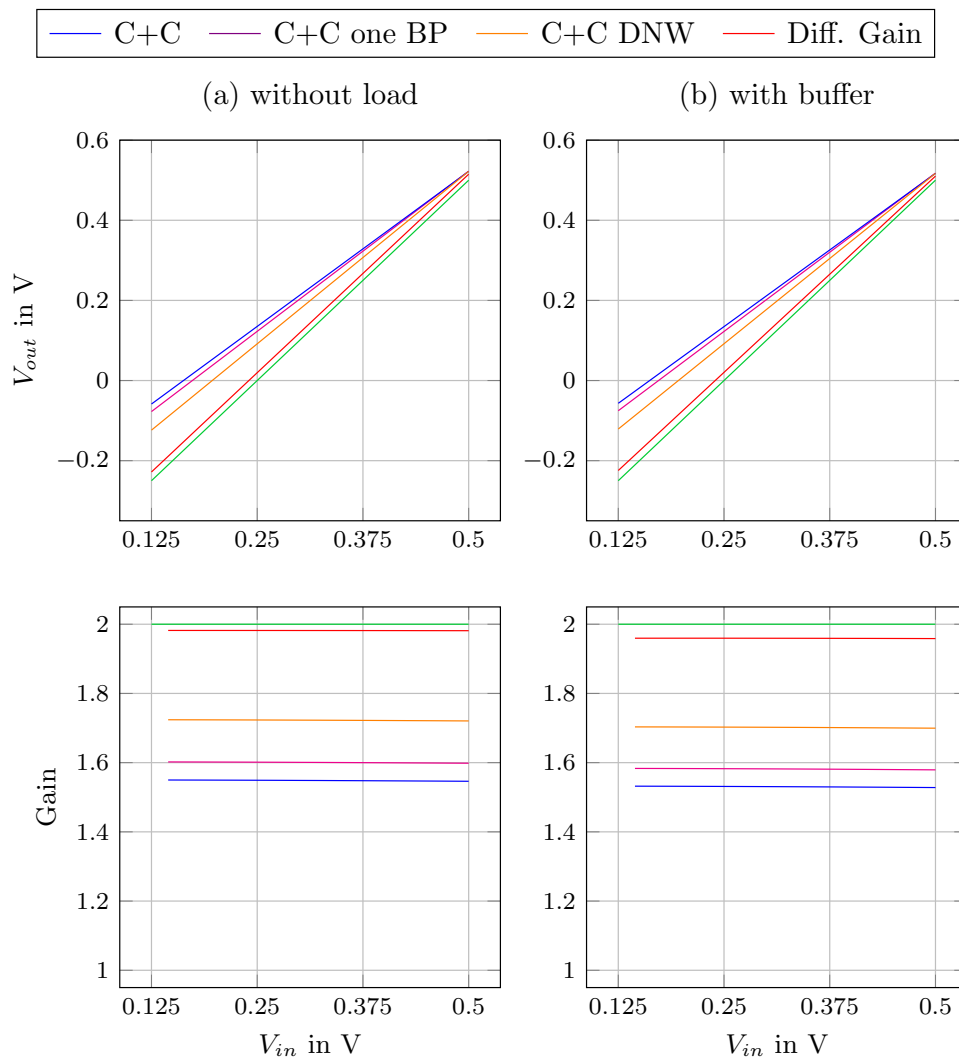


Figure 10.1.: Comparison of the different stages for the upper region. The transfer curve is shown above while the gain is plotted below. On the left (a) without any load, on the right (b) with the buffer.

the charge pump with both bottom plates at the middle node as presented in subsection 5.5.3.

The same topology where one bottom plate is connected to the driven node is named *C+C one BP*. *C+C DNW* shows results for the improvement with DNW shielding discussed in chapter 7. *Diff. Gain* is the new topology introduced in chapter 8.

They were all built with the same unit size capacitance and equally sized switches. The simulation was performed only for the upper region above V_{thp} . This is acceptable as the transfer curve is symmetric and the fact that the charge redistribution error is worst in this area.

At first the different circuits were operated without any load or buffer, see Figure 10.1 (a). This can be understood as ideally measuring the inherent gain of the SC network itself. On the right (b) results are shown for the whole stage with the output buffer. Again the same buffer was used in all cases. Worth mentioning is that the *C+C* solution only achieves a gain of roughly ~ 1.55 which is significantly lower than what is stated in literature for the whole stage [2].

10.1.1. Gain as a Function of Load Capacitance

Figure 10.2 visualizes the dependence of the stage gain on the load capacitance. In this case we attach the load capacitance directly - without the buffer - to the circuit to show the influence of parasitic capacitances.

The attentive reader may notice that the curves show almost identical slopes. This is irritating considering the statement that the *Diff. Gain* should be twice as robust to parasitics. Indeed, according to section A.3 we would expect the *Diff. Gain* curve to fall with only half the steepness for increasing C_L .

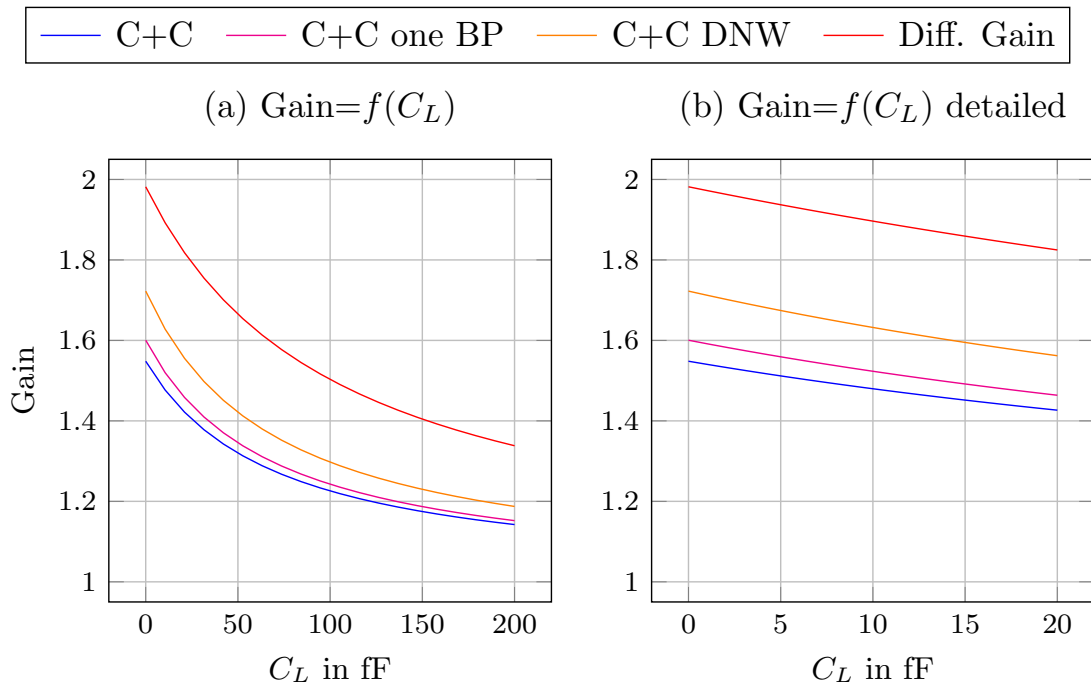


Figure 10.2.: Comparison of the different stages while the load capacitance was changed (a) and detailed in (b).

To approve that the foregoing mathematical derivations are correct, we have to consider that

10. Results

the simulation was carried out with physical device models. At the point where $C_L = 0$ there is still a capacitive load present in the parasitics of the switches.

For this purpose the topologies were simulated again without switches. As this was done only for one channel the results show voltages instead of the gain. In the first row of Figure 10.3 we see the behaviour over a wide span of C_L . For zero load the output voltage is equal to the ideal desired output voltage. With increasing C_L the voltage converges towards the voltage stored on C_L .

Only for very small load capacitor values (in relation to the sampling capacitor) as in the lowest row of the figure, we can observe that the derivatives on the right have a proportionality factor of two. The corresponding lines were calculated and are plotted in dashed style.

For an intuitive understanding we can argue that in both cases for $C_L \rightarrow \infty$ the final voltage has to go to the same value, the voltage previously stored on C_L . This is only possible if the curves exhibit almost the same steepness from some point onwards.

What finally matters is that the lower steepness at the beginning is still showing its benefits of better gain for quite large (up to hundred times the sampling capacitance) load capacitances.

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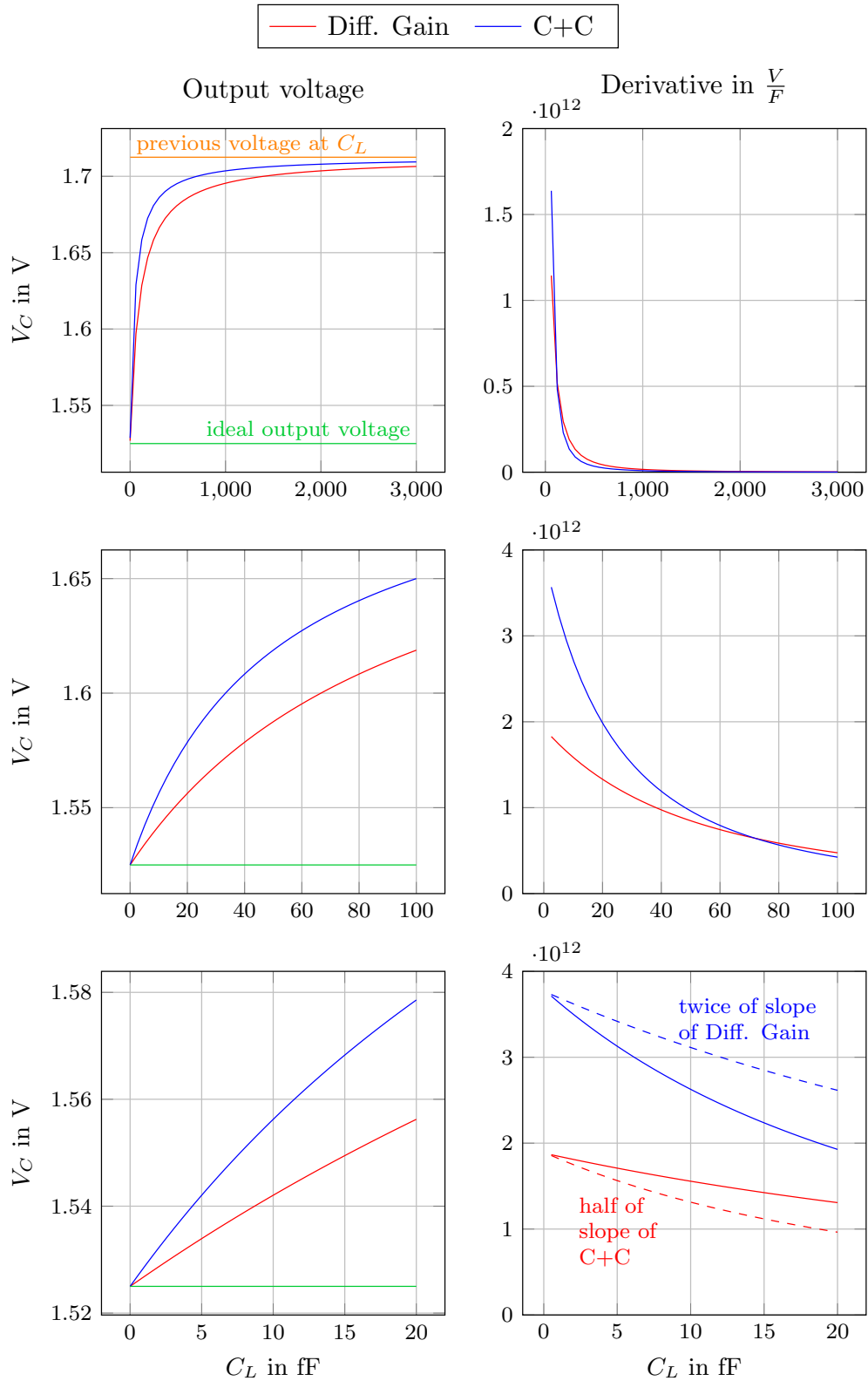


Figure 10.3.: On the left: the final voltage after the switching process for the two different capacitor configurations (C+C and Diff. Gain). On the right: the according derivative. Where in the last plot the dashed lines are calculated as twice or half the other steepness.

10.2. Unity Gain Cell

The designed circuit as in Figure 10.4 achieved a total (for multiplying and buffering) stage gain of ~ 1.96 . Opposed to ~ 1.8 as in [3] this is a significant improvement.

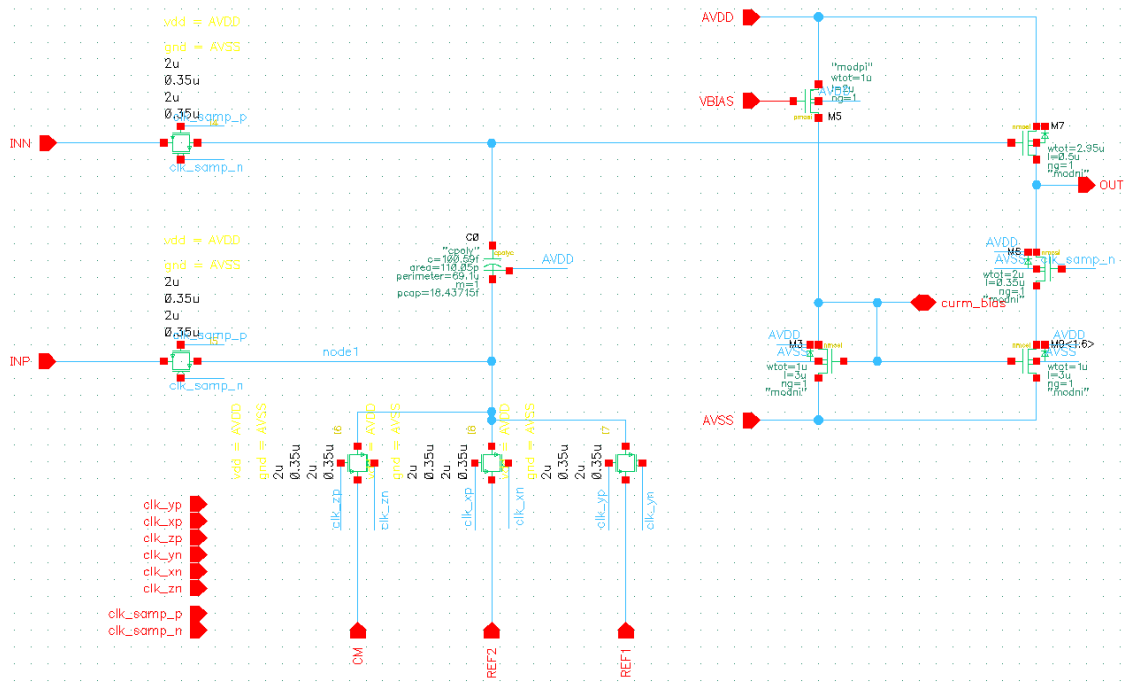


Figure 10.4.: Schematic of the unity gain cell.

The performance of this cell is given over temperature in Figure 10.5. Due to the fact that the gain error is mainly introduced by geometric measures, the gain curves show variation only in the third decimal place over temperature.

The layout of this cell is shown in Figure 10.7 and measures $45 \mu\text{m}$ per $75 \mu\text{m}$. It has to be mentioned that switch sizes were over dimensioned in order to use standard cells to keep layout effort small as this was just a concept approval. Proper dimensioning might further increase the gain.

Simulation results for different operating frequencies and layout parasitics are presented in Figure 10.6.

10. Results

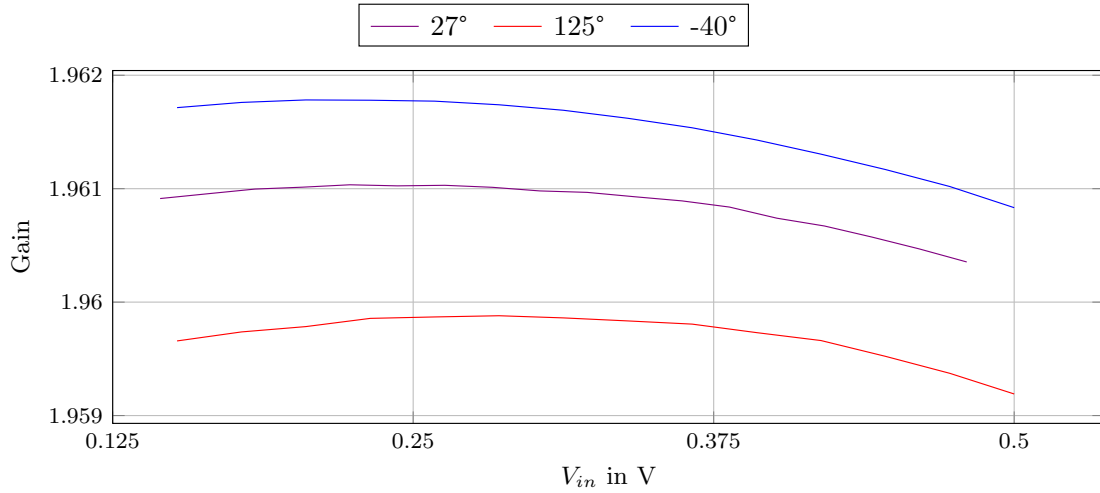


Figure 10.5.: Gain over temperature range

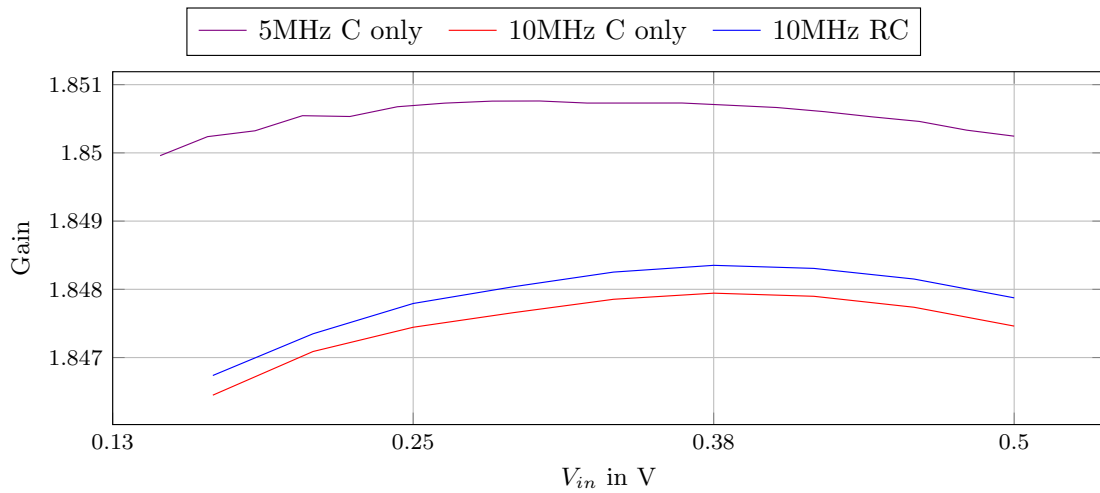


Figure 10.6.: Gain at various operating frequencies and different layout parasitics

10. Results

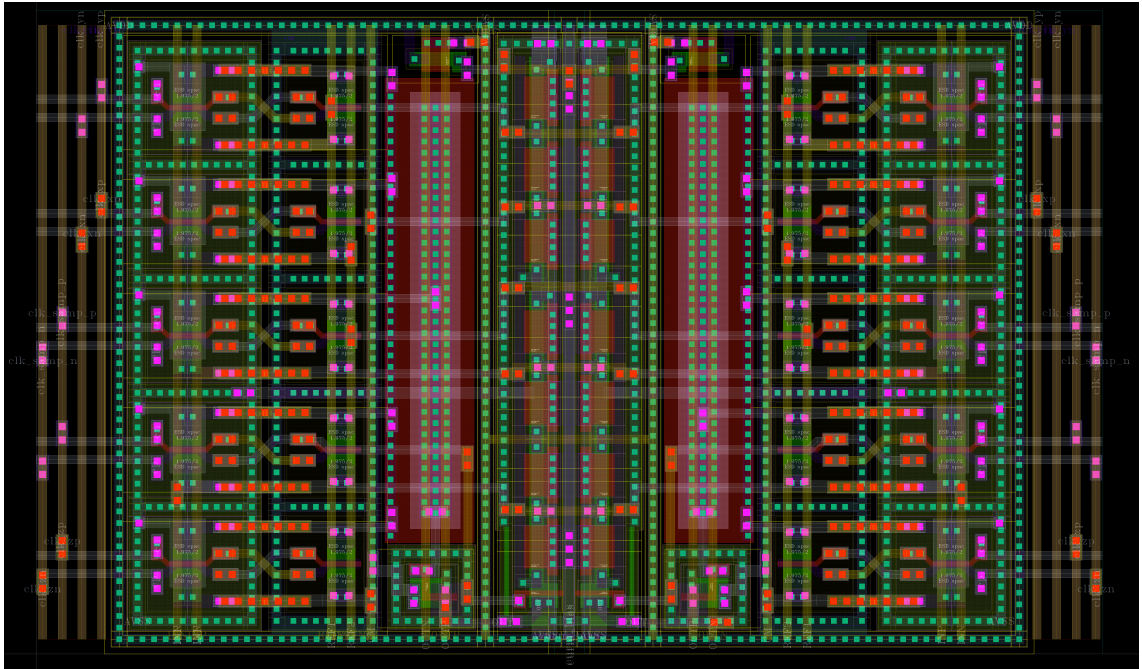


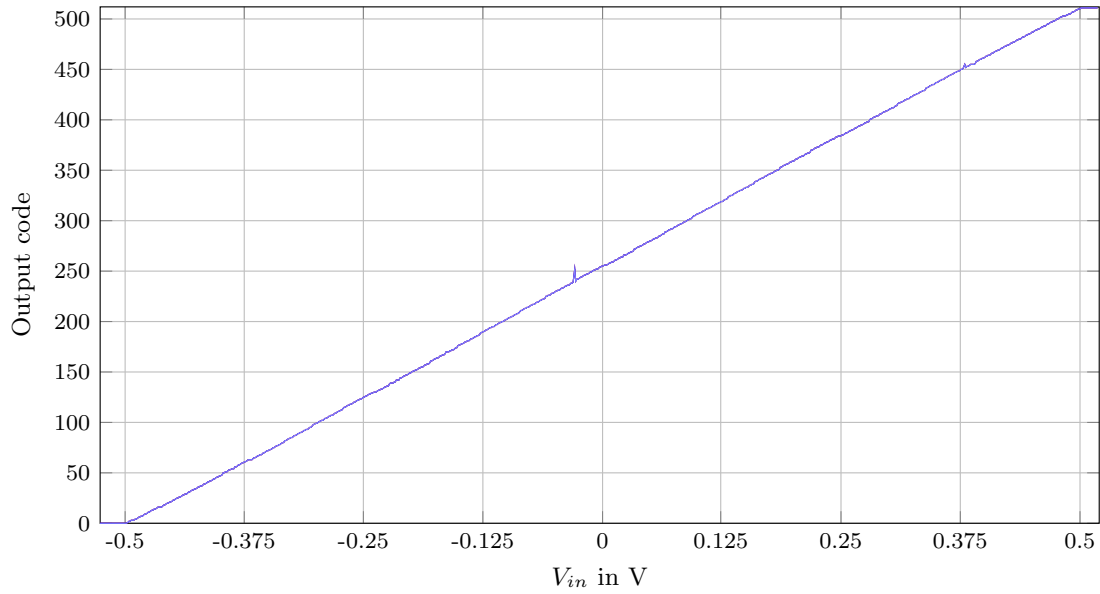
Figure 10.7.: Layout of the unity gain cell

10.3. ADC Performance

For simulation of the whole ADC an input ramp with a slope of one V_{LSB} per conversion step was applied. The transfer curves of the first three stages are shown in Figure 10.9. The whole ADC transfer curve can be found in Figure 10.8 (a). Actually, the curve is plotted for three different temperatures but as desired this lead to no significant derivations. The plots for the stage gains in Figure 10.8 (b) exhibit gaps as they had to be corrected from spikes. These spikes are caused by the region jumps which are not relevant for the plot. The individual stage transfer curves can be found in Figure 10.9 for the first three stages.

10. Results

(a) Output code over input voltage



(b) Stage gain of all stages

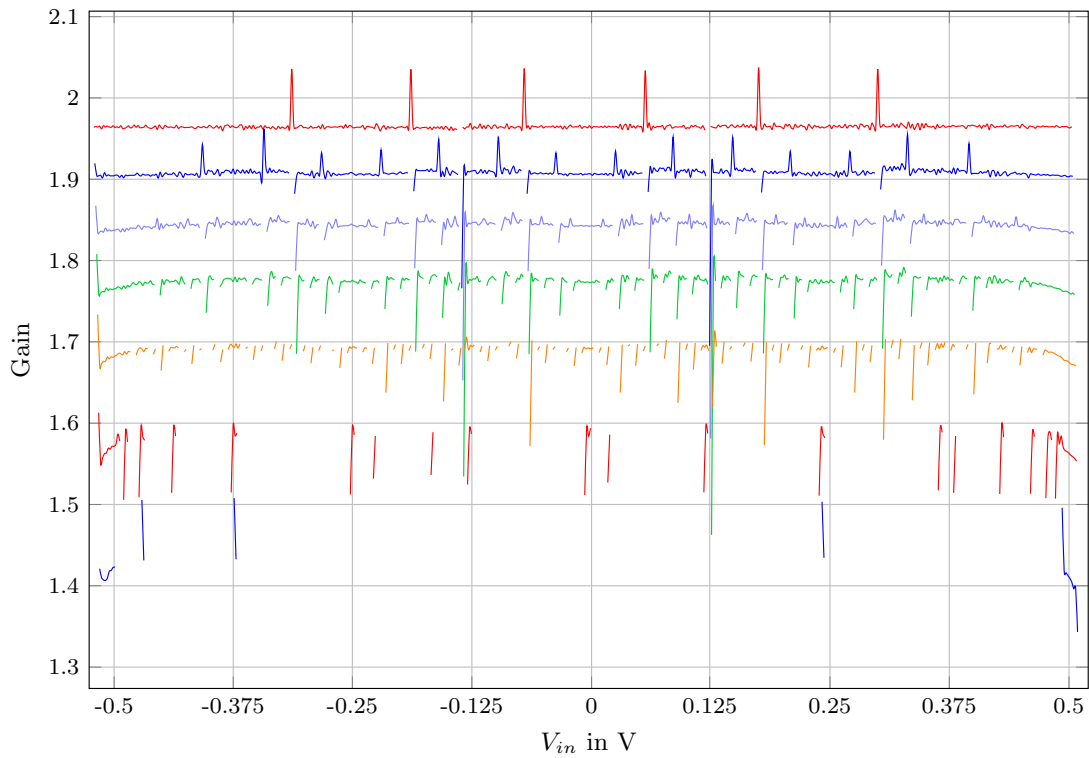


Figure 10.8.: ADC transfer curve (a) and stage gains for all stages (b).

10. Results

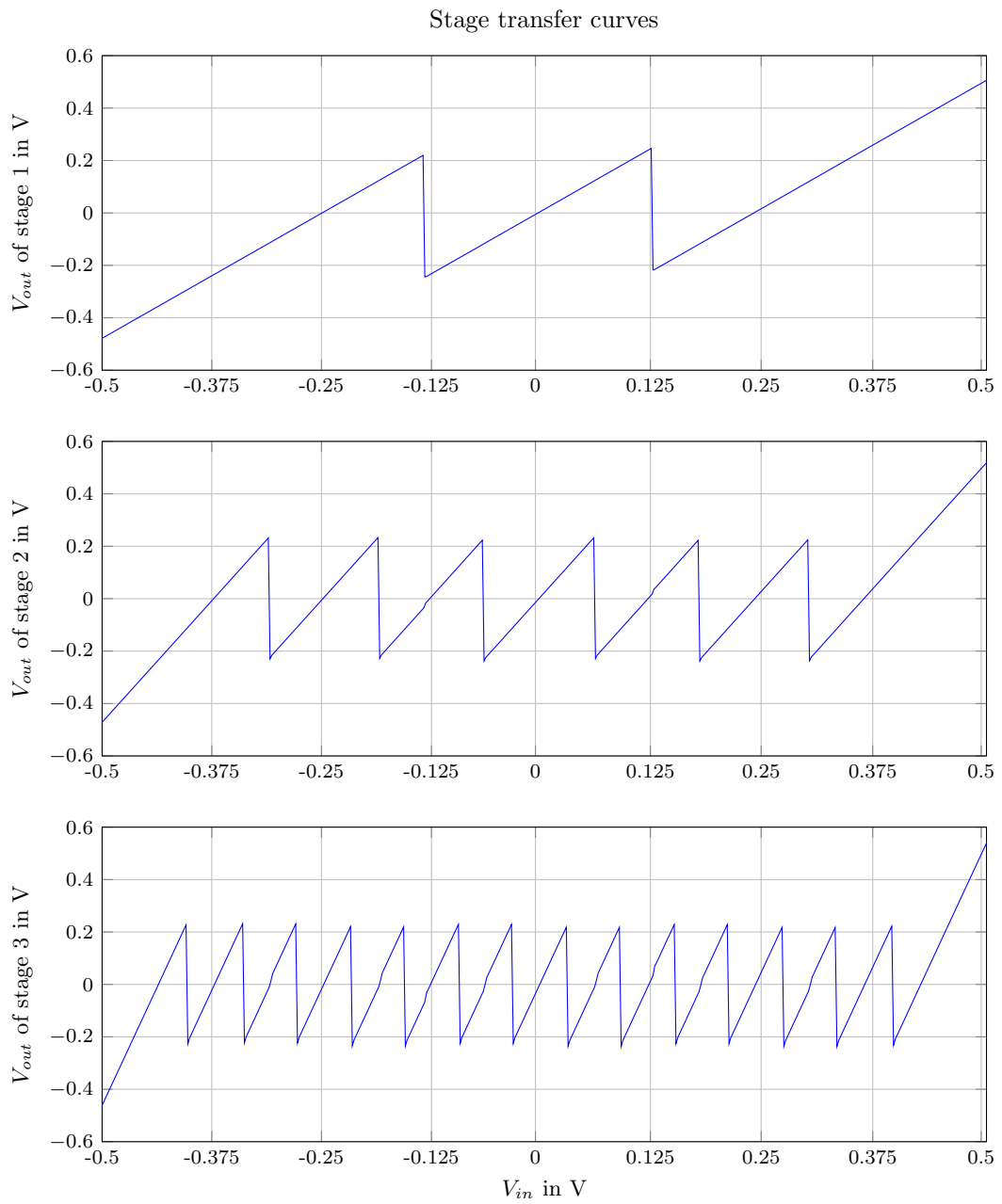


Figure 10.9.: Transfer curves of the first three stages.

10.3.1. INL and DNL

For INL and DNL measurements the slope of the ramp was lowered by a factor of ten so that ten conversions are done for each input code. The results therefore have an accuracy of $\frac{V_{LSB}}{10}$ and can be found in Figure 10.10. Comparing the plot of the DNL error with the stage transfer curves makes obvious that the error is worst for input voltages located close to the jumps of the transfer curve as in this region charge redistribution is more pronounced.

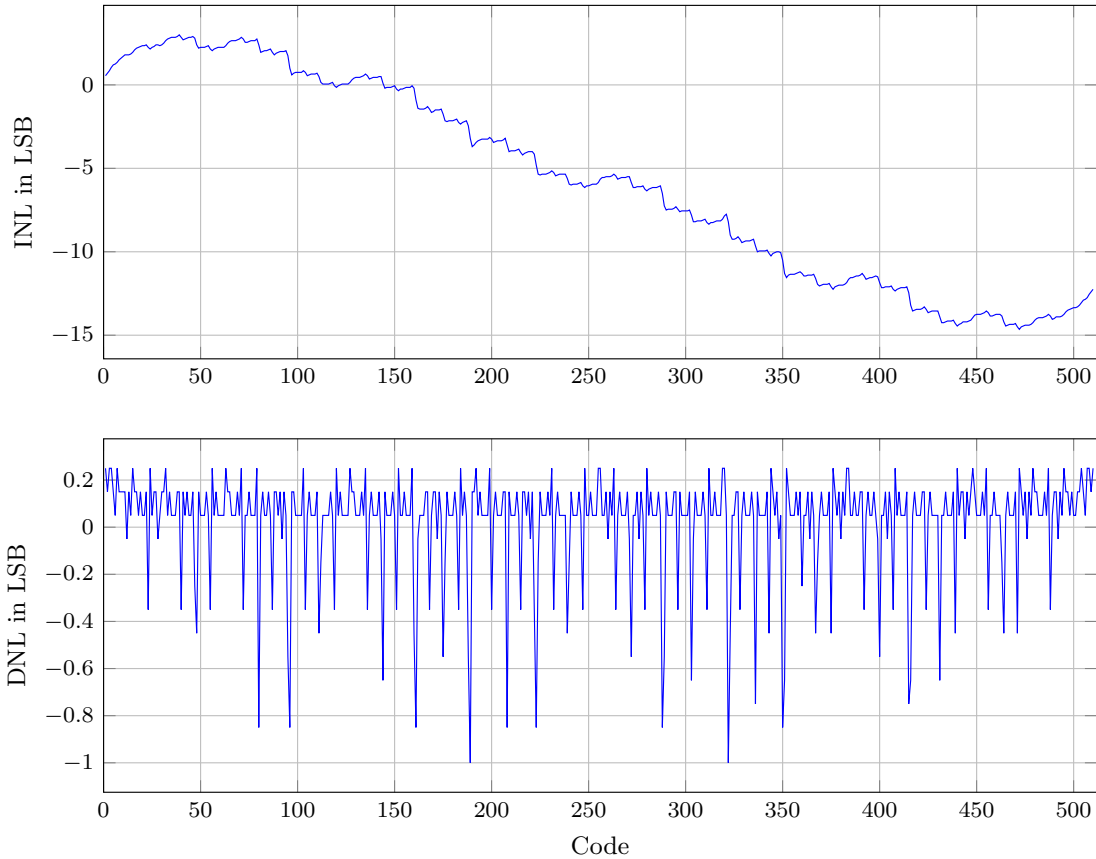


Figure 10.10.: Simulated INL and DNL of the proposed circuit using differential Gain.

10.4. Related Work - Performance Summary

The current consumption was determined to be 7 mA. Note that the original ADC, upon which the design was based, was running at 125 MHz. The S&H was not adapted, so that it is over dimensioned and contributed already 5 mA.

A comparison with ADCs running with comparable conversion rate and resolution is given in Table 10.1. The INL and DNL values are given without the use of digital calibration so that we can state that this work shows improvements in comparison to the C+C topology.

The other decisive improvement is the size of C_S . While the three given designs use capacitances

10. Results

	unit	C+C [3]	[15]	[7]	This work
Technology	μm	0.18	0.18	0.35	0.35
V_{DD}	V	1.8	0.8	1.5	3.3
FSR	V	1	0.8	2	1
N	bit	10	9	10	9
FOM	$\frac{pJ}{\text{conversion}}$	0.3	0.71	-	2.58
FOM	$\frac{pJ}{\text{conversion}}$	0.54	0.57	-	8.5
Conversion Rate	$\frac{MS}{s}$	50	10	10	10
DNL	LSB	-1/+1.6	-0.51/+0.49	-	-1/+0.3
INL	LSB	-17.9/+15.7	-0.49/+0.37	-	-15/+3
total Power	mW	9.9	2.4	28.3	23
C_S per stage & channel	pF	0.65(\cdot 2)	0.8(\cdot 2)	2(\cdot 2)	0.6 - 0.1
MDAC area	μm^2	-	-	-	3375
total area	mm^2	1.4	-	1.59	-
year		2010	2008	2000	2016

Table 10.1.: Comparing ADC performances of the proposed work with other SC pipelined ADCs.

over 0.6 pF in every stage, the new topology is built with a decreasing capacitor size along the pipeline. In addition, it needs only one capacitance per channel leading in total to less than 3 pF compared to 10.4 pF or even over 30 pF.

The lower speed is justified by the Miller Theorem as explained in subsection 8.4.3 and the larger process.

Within this project the proposed design did not quite reach the other FOMs due to the higher V_{DD} and technology. Another reason might be additional circuitry and the discrepancies where to draw the line when calculating the power consumption of the ADC. However, total power consumption is in the range of low power pipelined ADCs in the same technology.

11. Conclusion

Despite the ability to correct comparator offsets a pipelined ADC requires a high level of stage gain accuracy for larger resolutions. Owing to parasitics and many other secondary effects, what you design is not always what you get. To nonetheless make such circuits work certain strategies have been established. We were able to spot some of them throughout this work.

The OP-amp based solutions incorporate the idea of robust design where the price is paid mainly by analog effort. The OP-amp takes care of the parasitics by active recharging but contributes significantly to power consumption.

The C+C charge pump accepts the lower gain and uses digital calibration. This shifts the problem to additional digital circuitry which has to be designed and placed on chip.

The differential gain MDAC is the main achievement of this work. Besides possessing a better gain it uses less components and area. The challenge is moved to the charging process of the sampling capacitor of the next stage, which appears bigger as it physically is, due to the Miller Theorem. In this way, the architecture allows another choice in the trade-off between area, speed and gain accuracy.

Whether it can be used without digital calibration depends mainly on the desired resolution. Additionally, operating frequency and technology play a crucial role.

Especially the bigger technology probably precluded a similar speed performance as in the C+C charge pump presented in literature. Considering the fact that simulation results in our given technology showed even worse values for this topology than in the original, leads to the conclusion that the differential gain stage could reach even better accuracy in a smaller technology.

11.1. Future Work

Since it was not decided to produce a test chip within the master project this would be a top priority. In doing so the proposed circuit could be verified in the lab. Research is also necessary to find a suitable solution to handle charge injection. Dummy switches or constant V_{GS} sampling could be used as already known solutions but the symmetries of the circuit might open other doors. Another point for further investigations might be the fact that the INL and DNL errors show a very dis-balanced form. It would be interesting whether actions could be taken to counteract this phenomena, leading to a more uniform distribution. The concept of analog error correction, which was just truncated in one chapter might also have potential to rise the gain accuracy closer to the ideal value.

Appendix

Appendix A.

Mathematical Derivations

A.1. Setting the Potential of the Bottom Plate Capacitance

The parasitic network of a given circuit is illustrated in figure A.1 where the cut off point to the rest of the circuit is shown in a dashed line. To guarantee that the rest of the circuit stays unchanged during the two clock phases we set the condition that the total charge in the parasitic network should stay constant during the two switching phases.

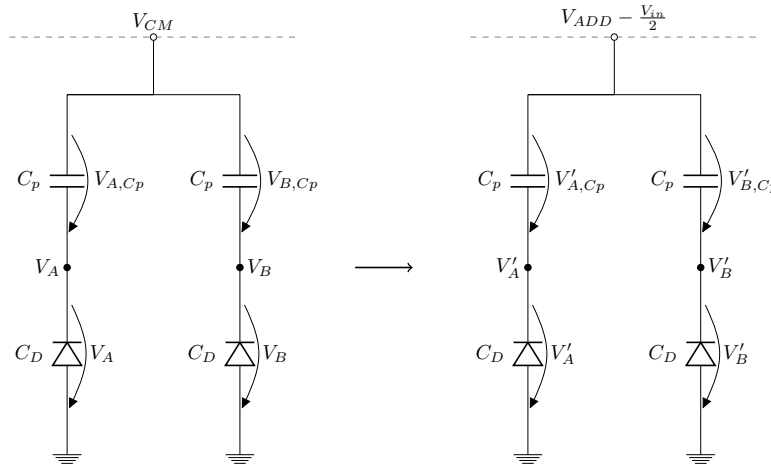


Figure A.1.: The parasitic network formed by the bottom plate capacitances and the N-wells

$$Q \stackrel{!}{=} Q' \quad (\text{A.1})$$

$$C_p \sum_{i=A}^B V_{i,Cp} + C_D \sum_{i=A}^B V_i \stackrel{!}{=} C_p \sum_{i=A}^B V'_{i,Cp} + C_D \sum_{i=A}^B V'_i \quad (\text{A.2})$$

Since C_p and C_D are unknown parameters it is desirable to full fill the equation without them being involved. With the voltages expressed in terms of V_i we therefore yield:

$$\sum_{i=A}^B (V_{CM} - V_i) \stackrel{!}{=} \sum_{i=A}^B (V_{ADD} - \frac{V_{in}}{2} - V'_i) \quad (\text{A.3})$$

$$\sum_{i=A}^B V_i \stackrel{!}{=} \sum_{i=A}^B V'_i \quad (\text{A.4})$$

The second equation states that the voltage over the N-well diode capacitance has to stay constant. However, if we assume that V_i and V'_i will be driven the charge change will be provided by the voltage source and therefore won't influence the rest of the circuit. Under this condition V_i and V'_i can be set differently and we can proceed with A.3.

$$(V_{CM} - V_A) + (V_{CM} - V_B) \stackrel{!}{=} \left(V_{ADD} - \frac{V_{in}}{2} - V'_A \right) + \left(V_{ADD} - \frac{V_{in}}{2} - V'_B \right) \quad (\text{A.5})$$

$$V_A + V_B - (V'_A + V'_B) \stackrel{!}{=} 2V_{CM} - 2 \left(V_{ADD} - \frac{V_{in}}{2} \right) \quad (\text{A.6})$$

for $V_A = V_B = V_X$ and $V'_A = V'_B = V'_X$

$$V_X - V'_X = V_{CM} - \left(V_{ADD} - \frac{V_{in}}{2} \right) \quad (\text{A.7})$$

$$V_X - V'_X = V_{CM} + \frac{V_{in}}{2} - V_{ADD} \quad (\text{A.8})$$

So two possible solutions can be derived.

$$V_X = V_{CM} \quad \text{and} \quad V'_X = V_{ADD} - \frac{V_{in}}{2} \quad (\text{A.9})$$

$$V_X = V_{CM} + \frac{V_{in}}{2} \quad \text{and} \quad V'_X = V_{ADD} \quad (\text{A.10})$$

A.2. The Impact of Capacitor Sizes on a Capacitive Voltage Adder

We assume two capacitors of arbitrary size which are pre-charged to certain voltage values. Once they are switched in series we want to know on which parameters the voltage across them depends. Be aware that in contrary to the parallel case, the total charge after the switching process is not equal to the sum of charges sampled on the two capacitances, $Q'_{tot} \neq Q_1 + Q_2$. When

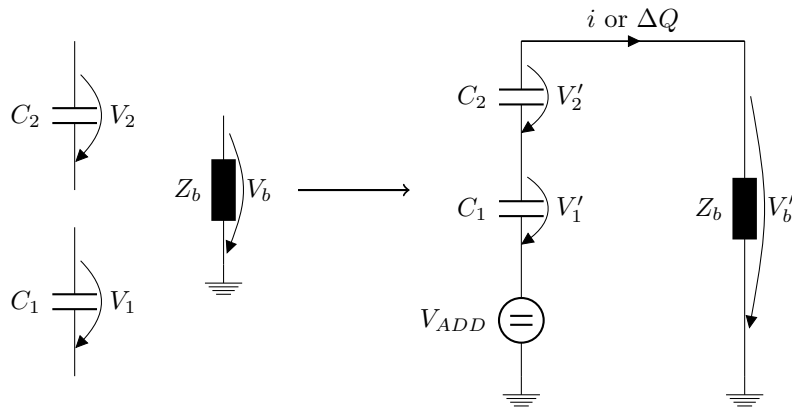


Figure A.2.: Setup to determine the impact of capacitor sizes on the error in a capacitive voltage adder

the input impedance of the buffer has a mainly capacitive characteristic after the two capacitors are switched to the buffer the system will settle meaning no current i will be flowing any more.

Appendix A. Mathematical Derivations

Since $i = \frac{dQ}{dt}$ we can state that due to the buffers input capacitance charge will be lost. As the current has just one path to flow the same amount of charge is lost on both capacitances. For the remaining charge we can set up the following equations and determine the voltages.

$$\begin{aligned} Q'_1 &= Q_1 - \Delta Q & Q'_2 &= Q_2 - \Delta Q \\ C_1 V'_1 &= C_1 V_1 - \Delta Q & C_2 V'_2 &= C_2 V_2 - \Delta Q \\ V'_1 &= V_1 - \frac{\Delta Q}{C_1} & V'_2 &= V_2 - \frac{\Delta Q}{C_2} \end{aligned}$$

The voltage at the buffer will be defined by:

$$\begin{aligned} V'_{buffer} &= V'_1 + V'_2 + V_{ADD} \\ &= V_1 + V_2 - \frac{\Delta Q}{C_1} - \frac{\Delta Q}{C_2} + V_{ADD} \end{aligned}$$

In the ideal case $\Delta Q = 0$, which as expected leads to:

$$V'_b = V_1 + V_2 + V_{ADD}$$

Since ΔQ is dependent on the size of the buffers input capacitance and the voltage jump which this node has to make it can be substituted to reach:

$$\begin{aligned} \Delta Q &= C_p \Delta V \\ V'_b &= V_1 + V_2 + V_{ADD} - \left(\frac{C_p \Delta V}{C_1} + \frac{C_p \Delta V}{C_2} \right) \\ &= V_1 + V_2 + V_{ADD} - \left(\frac{C_p}{C_1} + \frac{C_p}{C_2} \right) \Delta V \end{aligned} \tag{A.11}$$

The voltage jump ΔV can further be expressed as the difference between the voltages on the buffers input node $V'_b - V_b$

$$\begin{aligned} V'_b &= V_1 + V_2 + V_{ADD} - \left(\frac{C_p}{C_1} + \frac{C_p}{C_2} \right) (V'_b - V_b) \\ V'_b \left(\frac{C_p}{C_1} + \frac{C_p}{C_2} + 1 \right) &= V_1 + V_2 + V_{ADD} + \left(\frac{C_p}{C_1} + \frac{C_p}{C_2} \right) V_b \\ V'_b &= \frac{1}{\left(\frac{C_p}{C_1} + \frac{C_p}{C_2} + 1 \right)} (V_1 + V_2 + V_{ADD}) + \frac{\left(\frac{C_p}{C_1} + \frac{C_p}{C_2} \right)}{\left(\frac{C_p}{C_1} + \frac{C_p}{C_2} + 1 \right)} V_b \end{aligned}$$

For only one capacitor :

$$\begin{aligned} V'_b &= \frac{1}{\left(\frac{C_p}{C_1} + 1 \right)} (V_1 + V_{ADD}) + \frac{\left(\frac{C_p}{C_1} \right)}{\left(\frac{C_p}{C_1} + 1 \right)} V_b \\ V'_b &= \frac{C_1}{C_1 + C_p} (V_1 + V_{ADD}) + \frac{C_p}{C_p + C_1} V_b \\ V'_b &= K_1 (V_1 + V_{ADD}) + K_p V_b \end{aligned} \tag{A.12}$$

Which for differential sampling and V_{inp} at the output node leads to

$$\begin{aligned} V'_b &= K_1 (V_{inp} - V_{inn} + V_{ADD}) + K_p V_{inp} \\ V'_b &= K_1 ((V_{CM} + V_{in}) - (V_{CM} - V_{in}) + V_{ADD}) + K_p (V_{CM} + V_{in}) \\ V'_b &= K_1 (2V_{in} + V_{ADD}) + K_p (V_{CM} + V_{in}) \\ V'_b &= K_1 2V_{in} + K_1 V_{ADD} + K_p V_{CM} + K_p V_{in} \\ V'_b &= (2K_1 + K_p)V_{in} + K_1 V_{ADD} + K_p V_{CM} \end{aligned}$$

After introducing the proportionality factor m for $C_S = mC_p$ we receive:

$$V'_b(m) = \frac{2m+1}{m+1} V_{in} + \frac{m}{m+1} V_{ADD} + \frac{1}{m+1} V_{CM} \quad (\text{A.13})$$

A.3. Effective Capacitance

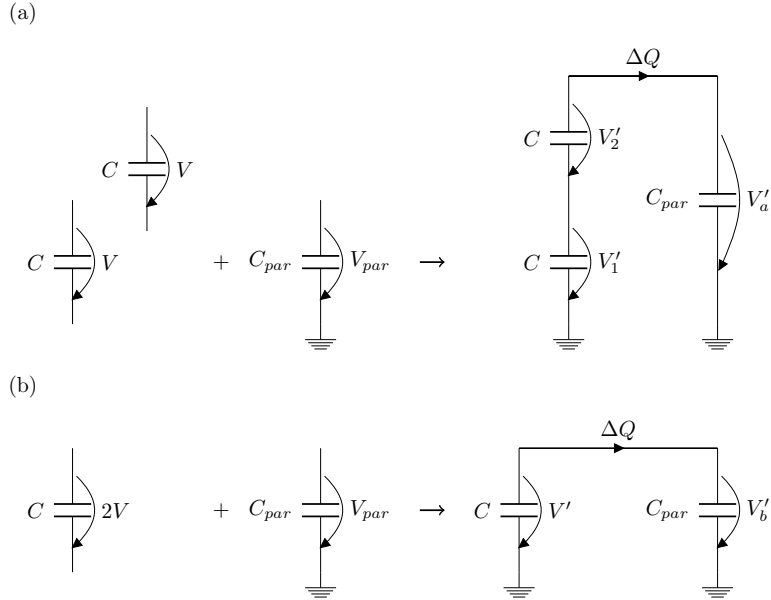


Figure A.3.: Comparison between prior art and the proposed circuit

It should be examined which error emerges for the two different settings (a) and (b) presented in Figure A.3 when they are switched to a node with a parasitic capacitance.

A.3.1. Calculating the Error Using the Charges

$$\begin{array}{ll}
 \text{for (a)} & \text{for (b)} \\
 V'_{1,2}C = Q'_a & V'C = Q'_b \\
 V'_{1,2}C = VC - \Delta Q & V'C = 2VC - \Delta Q \\
 V'_{1,2} = V - \frac{\Delta Q}{C} & V' = 2V - \frac{\Delta Q}{C} \\
 V'_a = V'_1 + V'_2 = 2V - 2\frac{\Delta Q}{C} & V'_b = 2V - \frac{\Delta Q}{C} \quad (\text{A.14})
 \end{array}$$

In Equation A.14 we clearly see that in case (a) the error will be twice as big. To yield the same error the capacitance needs to be doubled. Another approach would have been to calculate the equivalent capacitance of setting (a) over which 2 V are present in the first step.

A.3.2. Calculating the Equivalent Capacitance Value

$$\begin{array}{ll}
 \text{for (a): } X_C + X_C = \frac{1}{j\omega C} + \frac{1}{j\omega C} = \frac{2}{j\omega C} = \frac{1}{j\omega \frac{C}{2}} & C_b = C \\
 C_{a,tot} = \frac{C}{2} & C_b = C \quad (\text{A.15})
 \end{array}$$

Again we come to the conclusion that for case (a) twice the capacitance is needed to reach the same behaviour.

A.4. Emending Proportionality Factor

In the last section we derived the voltage at the buffer which is a function of the factor between the sampling and the parasitic capacitance. Here we now want to construct the desired voltage $2V_{in} + V_{ADD}$ using two different paths with a different proportionality factor. We chose m for main signal path and e for the emending signal path. We use a general equation valid for both cases represented in 9.

$$MV'_b(m) - EV'_b(e) \stackrel{!}{=} 2V_{in} + 1V_{ADD} + 0V_{CM} \quad (\text{A.16})$$

$$V_{in} : 2 \stackrel{!}{=} M \frac{2m+1}{m+1} - E \frac{2e+1}{e+1} \quad (\text{A.17})$$

$$V_{ADD} : 1 \stackrel{!}{=} M \frac{m}{m+1} - E \frac{e}{e+1} \quad (\text{A.18})$$

$$V_{CM} : 0 \stackrel{!}{=} M \frac{1}{m+1} - E \frac{1}{e+1} \quad (\text{A.19})$$

For a solution valid for all input signals all of these three equations have to be fulfilled. Therefore we start solving one of them and then recursively set into the others to find out for which values

Appendix A. Mathematical Derivations

of M and E a solution can be found.

$$\begin{aligned}
 V_{CM} : \quad & M \frac{1}{m+1} = E \frac{1}{e+1} \\
 V_{CM} : \quad & e+1 = \frac{E}{M} (m+1) \\
 V_{CM} : \quad & e = \frac{E}{M} (m+1) - 1 \tag{A.20} \\
 V_{ADD} : \quad & 1 = M \frac{m}{m+1} - E \frac{\frac{E}{M} (m+1) - 1}{\frac{E}{M} (m+1) - 1 + 1} \\
 V_{ADD} : \quad & 1 = M \frac{m}{m+1} - E + \frac{E}{\frac{E}{M} (m+1)} \\
 V_{ADD} : \quad & 1 = M \frac{m}{m+1} - E + \frac{M}{m+1} \\
 V_{ADD} : \quad & E+1 = M \left(\frac{m}{m+1} + \frac{1}{m+1} \right) \\
 V_{ADD} : \quad & M = E+1 \tag{A.21} \\
 V_{in} : \quad & 2 = M \frac{2m+1}{m+1} - E \frac{2e+1}{e+1} \\
 V_{in} : \quad & 2 = (E+1) \frac{2m+1}{m+1} - E \frac{2 \left(\frac{E}{M} (m+1) - 1 \right) + 1}{\frac{E}{M} (m+1) - 1 + 1} \\
 V_{in} : \quad & 2 = (E+1) \frac{2m+1}{m+1} - E \frac{2 \frac{E}{E+1} (m+1) - 2 + 1}{\frac{E}{E+1} (m+1)} \\
 V_{in} : \quad & 2 = (E+1) \frac{2m+1}{m+1} - E \frac{2E(m+1) - 1(E+1)}{E(m+1)} \\
 V_{in} : \quad & 2(m+1) = (E+1)(2m+1) - 2E(m+1) + 1(E+1) \\
 V_{in} : \quad & 2(m+1) = 2Em + E + 2m + 1 - 2Em - 2E + E + 1 \\
 V_{in} : \quad & 2(m+1) = 2m + 2 \quad \text{Q.E.D.}
 \end{aligned}$$

Note that e and m can not be negative since no negative capacitances exist.

$$\begin{aligned}
 e > 0 \rightarrow \quad & \frac{E}{M} (m+1) - 1 > 0 \\
 & \frac{E}{M} (m+1) > 1 \\
 & \frac{E}{M} > \frac{1}{m+1}
 \end{aligned}$$

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