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Development of Adaptive Test Methods for Semiconductors including Devices for Healthcare Applications

Master Thesis

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Abstract: In recent decades, the semiconductor industry managed to produce more complex components with ever-decreasing direct costs of production and this trend also seems to proceed in the future. Unfortunately a consequence of this trend also means that more and more effort is needed to test these advanced circuits. It has been shown that the test costs have become an ever larger share of the production costs and this trend will also continue. Among other things, the increasing test time, which is needed for each integrated circuit, is considered as one of the most critical cost factors. With this thesis, a new test method is presented which falls under the category of "adaptive test" methods. Adaptive test aims to reduce the test time per chip, but affect the quality of the products not, or only as little as possible compared to the conventional test. For that purpose, a simulation software has been developed that performs adaptive test simulations based on real data and test results of conventional production testing. Product analyzes were performed and both the potential at test time savings, and the resulting loss of quality were determined. Finally, the thesis has shown that by the intelligent omission of tests, compared to conventional testing procedures, test time reduction of up to 50% can be achieved with the simulation. In contrast, there are only few unrecognized defective components that are not detected by the adaptive test procedure and which reduce the quality of products. In best case, the fraction of nonconforming units was reduced down to values under 40 parts per million.

Key Words: semiconductor, adaptive test, test simulation, sample testing, outlier method

Zusammenfassung: In den letzten Jahrzehnten ist es der Halbleiterindustrie gelungen, immer komplexere Bauteile mit ständig sinkenden Direktkosten der Herstellung zu produzieren. Dieser Trend scheint sich auch zukünftig fort zu setzen. Die Konsequenz dieses Trends ist aber leider auch, dass immer mehr Aufwand nötig ist, um diese hochentwickelten Schaltungen zu testen. Es hat sich gezeigt, dass sich die Testkosten zu einem immer größer werdenden Anteil der Herstellungskosten entwickeln. Unter anderem wird dabei die steigende Testzeit als Hauptverursacher der Testkosten gesehen. Mit dieser Diplomarbeit wird eine neuartige Testmethode vorgestellt, die unter die Kategorie der „Adaptive Test“ Methoden fällt. Das Ziel ist, die Testzeit pro Chip zu reduzieren, jedoch die Qualität der Produkte im Vergleich zum konventionellen Test nicht, oder so wenig wie möglich zu vermindern. Dazu wurde eine Simulationssoftware erarbeitet, die basierend auf realen Daten und Testergebnissen des konventionellen Herstellungstests Adaptive Test Simulationen durchführt. Es wurden Produktanalysen durchführt und sowohl das Potential an Testzeitersparnis, als auch die resultierenden Qualitätseinbußen ermittelt. Schlussendlich hat die Diplomarbeit gezeigt, dass durch das intelligente Weglassen von Tests, im Verglich zum konventionellen Testverfahren, eine Testzeitreduktion von bis zu 50% mit der Simulation erreicht werden kann. Dem gegenüber treten nur wenig nichterkannte fehlerhafte Bauteilen auf, die vom adaptiven Testverfahren nicht erkannt werden und die Qualität des Produktes vermindern. Im besten Fall wurde dabei ein Anteil von nur 40ppm (parts per million) nicht vom Algorithmus erkannt.

Schlüsselwörter: Halbleiter, Adaptives Testen, Testsimulation, Stichprobentest, Ausreißer Methode

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Glossary

a.u.	arbitrary unit
AC	Alternating Current
ADC	Analog to Digital Converter
AQL	Acceptable Quality Level
ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
ATE	Automated Test Equipment
ATE	Automated Test Equipment
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
Die	A single semiconductor device or individual circuit within a wafer
DLL	Dynamic Link Library
DUT	Device Under Test
IC	Integrated Circuit
ID	Identification, Identification Number
ITRS	International Technology Roadmap for Semiconductors
LSL	Lower Specification Limit
Mixed Signal IC	Circuit processing both analogue and digital signals on one IC
PAT	Part Average Testing
PCB	Printed Circuit Board
ppm	Parts per million
QA	Quality Assurance
RF	Radio Frequency
RMA	Returned Material
SFL	STATS Function Library
SOF	Stop on Fail
STDF	Standard Test Data Format
SPC	Statistical Process Control
TTR	Test Time Reduction
UPH	Units per Hour
USL	Upper Specification Limit
Wafer	Round, thin silicon disc serving as basic material for ICs
WLP	Wafer Level Package

1 Introduction

Overview of Semiconductor Manufacturing Testing

The main competence of ams AG is the design and manufacture of analogue and mixed signal ICs (integrated circuits). Mixed signal ICs are devices which process both analogue and digital signals and combine or integrate these two functionalities into a single device to meet a function or application need. For instance a typical mixed signal IC is a common analogue to digital converter (ADC) which includes digital as well as analogue signal processing capabilities within one unit. Put simply, it can be said that analogue sections of such mixed signal ICs are similar to linear devices like amplifiers and regulators and deal with electrical signals that vary in the time as well as the amplitude domain. In contrast, the digital function blocks process only two binary amplitude states and uses logic state machines, processors and memory blocks to complete tasks. Mixed signal devices have become increasingly widespread in the semiconductor industry and are very common in our everyday lives. [1] Complex digital circuits are now increasingly being combined with analogue circuits as part of the continuing progress to higher levels of system integration in electronic devices. Microcontroller for instance represents a device group which is often combined with analogue units to form so-called "system-on-a-chip" ICs. The reduction of chip to chip interconnections is only one reason why mixed signal devices offer the customer significant application advantages and savings in manufacturing costs. Some examples of products which include mixed signal ICs are cellular telephones, multimedia audio and video devices and medical equipment. [2] ams AG produces semiconductors, including high performance standard products as well as customized solutions also known as ASICs (application specific integrated circuits). An ASIC is a custom chip which implies that only one client orders this circuit for a specific application.

The company has the three main focus areas: power management, sensors & sensor interfaces and mobile infotainment. The markets of ams AG are Consumer & Communications, Industry & Medical and Automotive, complemented by its Full Service Foundry activities. ams AG operates its own leading-edge 200mm (8”) wafer fabrication as well as state of the art IC test centres and has its headquarters located in Unterpremstaetten - Austria. The analogue and mixed-signal process technologies include CMOS, HV-CMOS and SiGe technologies.

The very challenging manufacturing of wafers occurs in many complex process steps and takes about 5 to 6 weeks from raw silicon material to the bare wafer. This is the so-called front-end in the manufacture of integrated circuits which deals with the production of the electrically active devices (transistors, capacitors, etc.) and the associated wiring (metallization). After this front-end production, the finished wafer is composed of many ICs of the same kind which are also called "dies" during these production steps because of their small rectangular plate-like shape. [3]

After the wafer fabrication, many additional production steps remain before a final device can be shipped to the customer. The sum of subsequent steps after the wafer fabrication is termed back-end operations or post-silicon production flow and is detailed in Figure 1.

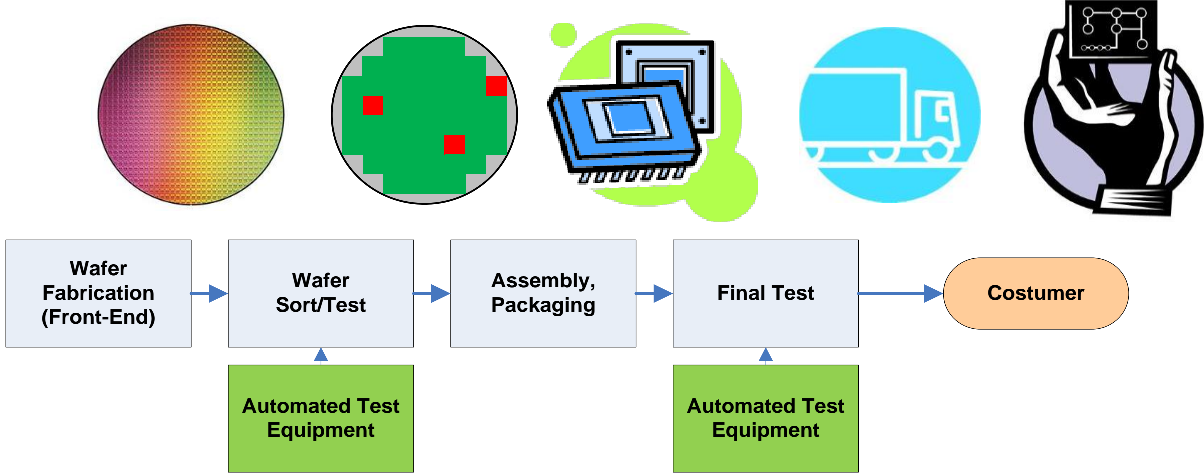

Figure 1: Traditional Semiconductor Back-End Production Flow for packaged parts with the focus on Production Test

Figure 1 represents the simplified back-end production flow with the focus on testing of the ICs produced. Production means high volume manufacturing and because the fabricated chips are tested in the factory these processes are called manufacturing test. After the wafer fabrication, which includes the whole front-end process, the functionality of all ICs is usually tested prior to further processing with an electrical test named the wafer sort or wafer test. The wafer sort is carried out in bare wafer form and the dies are tested for manufacturing defects[1]. Therefore automated test equipment (ATE) is used to prevent faulty dies from continuing on to later production steps, which is the main driver for applying a

[1] "A defect is a physical anomaly within the IC, which can be caused by impurities such as dust or improper manufacturing processes. Defects cause electrical failures on the IC and logical failures or faults. A fault is a model of a defect's effect on the circuit. " [1, H. Geng, 2005, site 300]

manufacturing test at the wafer level. Only those devices which pass all the product specific tests are further assembled. Individual test software and hardware is designed by a test engineer for each product to ensure the testing process on the ATE. Generally, a test program directs the ATE through the process which applies different types of electrical stimuli on the device under test (DUT) and the ATE then observes the responses. Afterwards the ATE's task is to determine whether the device passes or fails the test. [2]

Thus applying test stimuli and evaluate the response of a DUT is the general definition of a test process in electrical semiconductor testing. Typical ams AG mixed signal products must pass hundreds or even thousands of tests before they can be shipped to the customer. In general, dies are subjected to **main two test types**, standardized parametric and functional tests. The purpose of **functional testing** is to provide verification that the DUT performs its intended function. Thus the correct operation of the chip design is checked by testing the internal chip nodes. Only when the output of the DUT accords to the expected function of the circuit, the die passes the test. The primary representative for this category of tests are digital tests, where binary test patterns on the input of a circuit result in a pattern on the output of the same unit. **Parametric tests** represent the second main category of tests. Parametric tests are those that return a measurement value. This value has to be checked afterwards to determine whether it lies between predefined limits. The pass or fail decision is determined by comparing a measurement against his specified test limits. They can be subdivided into AC and DC parametric test. Some examples for these kind of tests are leakage current, amplifier gain, input resistance and output noise. The role of parametric tests can be manifold, ranging from quality control to process control and design verification. [2] [4]

For the wafer sort, each die or a sample of dies per wafer is electrically contacted directly on the semiconductor material. Therefore the ATE uses an array of needlelike probes that descend on the contact pads to make electrical connections to each DUT. After the circuit is tested, the ATE steps to the next one. In principle, functional as well as parametric measurements are applied to ensure that the dies meet the electrical specifications which are predefined in the test specifications. At this stage the specifications are usually not the same as the datasheet specifications which are expected by the customer because the performance may change once the device is assembled. It is often the case that circuits can

develop their full performance only in the package, for example due to thermal or electrical conditions. Another example is that without any casing photons from ambient light may disturb leakage current measurements on the raw semiconductor material. At ams AG it is usually the case that electrical testing in production is done with limits derived from actual chip parameter distributions instead of the specification limits guaranteed to the customer by the data sheet. It is, however, essential that these statistical limits have to be tighter than those specified. The requirements for testing are summarized in separate test specifications. As mentioned before, the main goal is to determine whether the DUT functions correctly and the elimination of non-conforming parts can be very cost effective because these parts are not packaged in the subsequent process step. Thus the wafer sort helps to minimize scrap and material costs. [4] [5]

Inking, which makes it possible to distinguish between good and bad dies at the wafer level, represents the next intermediate step in the processing chain. In the past, defective dies at this stage were often marked by the use of ink dots at the proper position on the wafer surface. In this way it was possible to discard defective devices afterwards. Today, primary wafer mapping is used to track defective dies back. This is done automatically by the ATE and a linked database which provides the tests' pass and fail information and the exact coordinate of every die electronically. Afterwards the wafers can be sawn into separate dies and only faultless devices are then assembled into packages. The wafer sawing procedure is also known as dicing. During the packaging process the individual ICs are usually placed in housing and contacted to external pins. Many different types of packages and packaging technologies are used. Packaging is not just used to provide the electrical connections to the outside of the die, making it possible to mount the ICs on printed circuit boards (PCB). It is also the aim of a package to mechanically and thermally link the IC to its environment. So the package has to protect the IC, support the IC performance, handle the thermal conditions and power dissipation and has to offer a mechanically and electrically reliable interconnection to the printed circuit board (PCB). [1] [6]

After this process, the packaged ICs are ready for the next production step, the final test, which is also carried out with the help of ATEs. Again, functional and parametric testing is performed on the now packaged device under test (DUT). On the one hand, the aim of final testing is to check whether the performance of the dies has changed due to packaging. So

the purpose is to verify if the assembly has been faultless and the ICs that were initially operating properly are still undamaged after the packaging process. On the other hand, as already mentioned above, it may be the case that a measurement with package differs from the wafer sort result. For instance in the case of RF (radio frequency) tests, mostly a measurement with housing differs from the wafer sort value. Since it is the last step in the production flow it is crucial to ensure quality of the products. Final testing is done to make sure that all the products perform within the specifications for which they were designed and which are expected by the customer, based on the product data sheet. Basically, a device specification defines the requirements needed for the part to work properly in the application and is created together with the customer for ASICS. After final testing is complete, the devices can be shipped to the customer, and once the ICs are received they may be tested again. This testing is known as incoming inspection or acceptance sampling and is conducted either by the customer or for the customer by an independent test house. [4]

To sum up, an extensive testing of the ICs is carried out before the products can be shipped to the customer. Every fabricated chip is subjected to production tests with the goal of enforcing the quality requirements by determining whether a device meets its predefined specifications or not. Semiconductor tests, and especially the testing of mixed signal devices, have developed into a highly specialized field of electrical engineering. Unfortunately it is not the case that every fabricated chip is perfect. Some causes of defects are impurities and defects in materials, equipment faults or human error. Defects like these are the reason why each semiconductor product must be investigated and is subjected to production testing. Since they are unavoidable, defects and their consequences, the faults, are the main drivers for testing. Production tests are typically short but verify all the relevant specifications of the device. In addition to the normal sorting function, tests also provides a very valuable feedback loop for understanding the fabrication process of manufactured chips, which is also termed “yield learning”. [4] [7]

It should also be mentioned that there are other possible back-end flows compared to the flow in Figure 1. For instance, it is also possible that the customer purchases the product directly in bare wafer form after wafer sort or as unpacked dies after the sawing process. In both cases only a wafer sort is applied to the product. Another variation to the flow

described above concerns products with modern wafer-level packages (WLP). Wafer-level packaging is a process in which all the integrated circuit packaging and interconnection is performed on the wafer level prior to the sawing process. Thus the final test also takes place directly on the wafer and the sawing process represents the last step in the manufacturing flow. [6]

Conventional Semiconductor Manufacturing Test

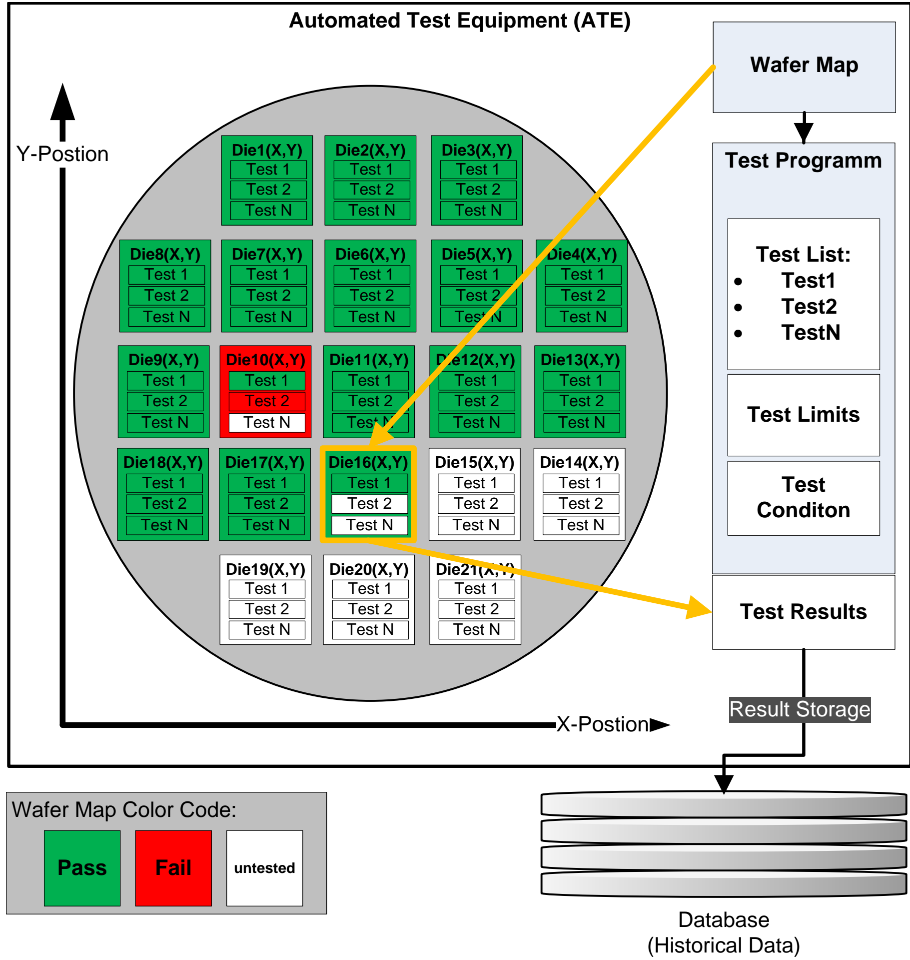

Figure 2: Conventional Semiconductor Manufacturing Test

The simplified operating mode of a conventional manufacturing test is shown in Figure 2 using an example of a wafer sort where the wafer is displayed as a grey round slice. The whole test procedure of one IC is controlled by the automated test equipment (ATE) and the test program which is executed on it. In simple terms it can be said that an ATE is an electrical measurement instrument with three main tasks. The first task is to apply test patterns to a device under test (DUT), the second is that the response of the DUT has to be analysed and finally the DUT is marked as good or bad. Thus the purpose of a tester is to drive the inputs and to monitor the outputs of a DUT afterwards. To be able to do all this,

first the ATE has to know the right positions of the dies integrated on the wafer which are to be tested. This product specific information is shared in the form of coordinates within the so-called wafer map. Afterwards the wafer sort can be started and die after die is tested sequentially. To minimize the time delay in-between the testing of dies, the next DUT should always be the nearest possible neighbour with the shortest distance to the coordinate of the actual die. Commonly this time delay between DUTs is called the index time and for a wafer sort it is also known as the step time. To achieve minimal delays a step sequence corresponding to the numbering from 1 to 21 of the dies in Figure 2 leading to a winding path is common. Once a die is selected, e.g. die 16 in Figure 2, the test program executes the predefined test list including the different types of test. As mentioned above, the two main types are parametric as well as functional tests. [5] Each test result is verified if it lies between predefined limits for parametric tests and if the DUT delivers the right output for functional tests. Only if the DUT passes all tests out of the test list, the part can be marked as a pass (green colour in Figure 2). If only one measurement fails its test requirements, the whole die fails its specification and is marked as a fail (red colour in Figure 2). Additionally, when a fail occurs all the following tests are not executed, if there are any remaining. This is done because it would bring no new information about the condition of the device and only waste test time. This strategy is also known as SOF (stop on fail) testing and die 10 in Figure 2 is representative of this behaviour. A conventional ATE has also the capability to operate with different test conditions. This implies, for example, applying tests at different temperatures to guarantee the customer the specified operating specifications. Additional examples are applying tests at several voltages (e.g., supply voltage, input voltage), testing with different timing conditions (e.g., clock frequency) to verify or grade ICs according to their performance and testing with different chip load conditions. For conventional high volume production testing these test conditions are predefined for worst case situations and never changed during a running production test session. Finally, after the wafer is sorted into faulty and faultless devices, the measurement values and results are typically stored into a database in a standardized data format, the Standard Test Data Format (STDF™, Teradyne Inc., North Reading, USA) and stored there for several months.

In principal the final test procedure is very similar to the wafer sort process. Because the wafer has been separated into single dies before, for the final test no wafer map is present. For a wafer sort, a robotic machine called a “wafer prober” manipulates the wafer, selects

the proper DUT and establishes electrical contact with it. Therefore the wafer prober selects all DUTs based of the wafer map. In contrast to that, at the final test, the packaged devices are picked up automatically by a so called “handler”. [2]

Traditionally, all parts are tested identically during each step and the test list, test limits and test conditions are always the same. Whenever a change or optimization of this conventional test procedure is required it can only done offline, which means it’s not possible during the running production. For example, test time reduction would be interesting because of the good performance or improved yield of the product, it is only possible to adapt the test program by manually excluding tests from a fixed test list. Improving test quality by setting tighter test limits is another example which cannot be carried out during the test session. Despite its advantages, conventional semiconductor testing is a fixed and rigid process and human involvement is needed for any adaption and improvement. Testing produces a huge amount of data, which are often supplied manually to analysis tools. Because they are not fully avoidable, manufacturing drifts do occur, and in worst case scenarios they remain unnoticed as long as they are within the specification limits. Furthermore, every test insertion in the backend-flow is a self-contained process in regard of data analysis and process control. So it is, for instance, not possible to adapt or optimize the final test based on wafer sort data and bridge across the various test insertions.

The Adaptive Test

The adaptive test definition, introduced by ITRS (International Technology Roadmap for Semiconductors), shows the differences between a conventional and adaptive test procedure, or rather the extension from traditional testing to the new approach of adaptive testing. [8]

> *"Adaptive Test is a broad term used to describe methods that change test conditions, test flow, test content and test limits (potentially at the die/unit or subdie level) based on manufacturing data and statistical data analysis. This includes feed-forward data from inline and early test steps to later test steps and feed-back of data from post-test statistical analysis that is used to optimize testing of future products. Adaptive Test also includes real-time data analysis that can perform Statistical Process Control (SPC) and adjust test limits and content during product testing on-the-fly. (e.g., Parts Average Testing algorithms) Although some simple applications have been applied for some time, Adaptive Test will increasingly be applied and will require updated software algorithms and complex statistical analysis methods and database infrastructure." [8 , ITRS, 2006,* site 17]

Adaptive test was added to the ITRS in 2009 and is in the meantime a continuously growing area [8]. One purpose of adaptive testing in general, and especially for ams AG, is to reduce test costs due to test time reduction without any significant losses in quality, which means optimizing the defect detection probability. Adaptive test has also the possibility to improve product quality, for instance by tightening test limits, change test content or aggravating test conditions. Dependent on actual test results from the DUT, results from previously tested DUTs on the same wafer, results from previously tested wafers and results from prior test insertions or manufacturing steps, targeted decisions for the next tests on the same die or for the next devices could be derived. So, with an adaptive setup, tests applied on each die are individually and dynamically adapted for maximum cost effectiveness. Adaptive test will include a combination of parametric measurements and functional tests and its nature depends upon the type of circuit, the customer and their quality expectations, specific device peculiarity or weaknesses and economic considerations like manufacturing and market price. [9]

An approach is offered for an adaptive test environment in the following section of this work which is basically an extension of the conventional setup and can also be seen as the basis for the adaptive test simulation.

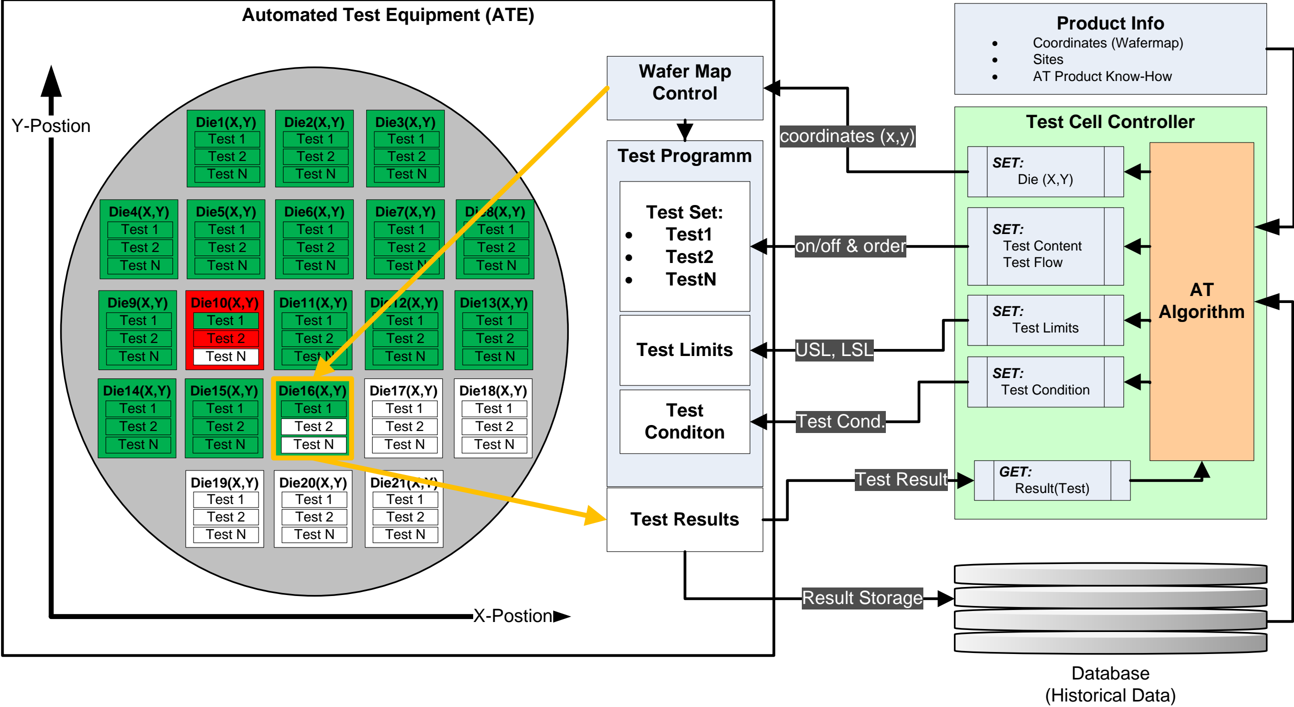

Figure 3: Theoretical Setup for Production Test with Adaptive Test Capability

An ideal, but still theoretical adaptive test setup for electrical testing at the wafer level is presented in Figure 3. The adaptive test setup in Figure 3 is an extension of the conventional semiconductor test setup in Figure 2. The functionality, which makes adaptive test possible, is centralised in a so-called test cell controller. This is an external processing unit with powerful statistical processing capabilities as well as real-time interfaces to a common ATE. The blue function blocks in the figure (set- and get- functions) represent the interface from the viewpoint of the test cell controller. This test setup has the capability to change all the following parameters during a running test session without any significant time delays on the testing process itself, which means it's possible to make these adaptations in real-time:

- **Wafer map control**

  It can decide which DUT will be tested next, due to an implemented wafer map control. Any position on the wafer can be selected by sharing the coordinates between the test cell controller and the ATE. As mentioned in the previous chapter, the stepping sequence through all the devices on the wafer is predefined for conventional testing with respect to minimal stepping time between DUTs. For

instance, due to the wafer map control it can dynamically decide if, instead of 100% testing, only a sample of DUTs is drawn, or vice versa.

- **Test Content**

  The ATE has the capability to change and modify the test content, which means that it is possible to add or skip tests at any time. So even if a device is currently under test, it is possible through the test cell controller to modify or change the test sequence.

- **Test Flow**

  There is also the ability to change the test flow by reordering tests. The order can either be predefined or also be changed during the running IC test. It is, for example, also possible to make any specific test again without contacting the DUT again.

- **Test Limits**

  For parametric tests, the test cell controller is able to dynamically alter the test limits, which leads to individual pass/fail criteria for each DUT. Quality improvement due to tighter specification limits is conceivable. The method of dynamic part average testing (PAT) could, for instance, be implemented with this option. [10]

- **Test Condition**

  The final parameters which can also be altered on the fly are test conditions. For example, supply voltage or operating temperatures can be adapted during testing, which is not offered during a conventional test.

Making meaningful efficient and targeted decision about changing and adapting these intervention options on a running test session is the task of an appropriate AT algorithm. Whatever any algorithm looks like, they have one thing in common. The adaptation algorithm can be based on previous measurements from the same unit (feed-forward), as well as the same measurements on previous units (feed-back) stored in the database (historical data of the same product). Thus the decision making for the adaptive intervention options is based on three inputs:

- **Actual test results** and data from the running testing session. This includes test results from the actual DUTs as well as results from other DUTs before on the same wafer for an adaptive wafer sort.

- **Historical test data** from the same product generated in previous tests session or test stages and stored in a data base. Thus the database stores data from the same product type of other wafers. Other data base entries are data from the same product of other test stages or insertions. Until now it was talked about the adaptive wafer sort but for instance, it is also conceivable that the wafer sort data collected afterwards could be the base for adaptive test decisions in final testing. The database for testing, therefore, differs significantly from that of the conventional tests by including data from all the test insertions over the production process.
- **Product specific knowledge** (Product Information) which the algorithm has to know to be able to work. This includes the information about the positions of the dies on the wafer which is shared by the wafer map. The number of dies which are tested parallel with the same measurement settings (which is termed "sites") also has to be known by the algorithm (sites and parallel testing is explained in section: 2.1.4 Detailed Algorithm Description). Additionally, specific knowledge of tests is necessary which implies, for example, the presence of mandatory tests which must not be skipped any time to make the simulation as realistic as possible (details are illustrated in section 2.1.2 Simulation Rules and Limitations that arise due to the Properties of a real Production Test).

In principal, the adaptive final test procedure is again similar to the adaptive wafer sort process, except that no wafer map is present. Adaptive testing is a dynamic testing approach instead of static optimization which has been carried out at ams AG up to now. The ATE has to be extended by test cell controller and result database external units. The information sharing between these units due to real-time interfaces makes an adaptive approach possible. The adaptive test algorithm is the master of the whole process and aims to dynamically control and change the test program used for testing each specific circuit at the different test stages in the test flow. The aim is to make a trade-off between the overall test cost and defect detection probability. A version of such an algorithm was developed as part of this work and will be presented in section 0.

Quality and Economics of Testing

In 1965, Gordon Moore predicted that the transistor density on semiconductors was going to grow exponentially. Today, almost five decades later we can look back to the incredible growth of the semiconductor and electronics industry, and it has been shown that Gordon Moore and his famous Moore's Law was right. For more than a half of a century we have observed that the transistor density doubles roughly every 24 months. Generally, industry reaches continuously higher levels of component integration due to steadily decreasing the minimum feature sizes, which in turn means shrinking geometries used to fabricate ICs. Other trends which have been observed and still on-going are, increasing functionality as well as complexity, rising performance (clock rates), lower power consumption especially for portable devices and smaller form factors for more compact products. All these continuously improvement trends are sometimes summarized with the term "scaling effect". [7] [11]

Scaling of the wafer fabrication processes and improvements in design drive down the cost per transistor and hence the cost per function dramatically. This is the most significant trend which has led to significant developments in economic productivity in the semiconductor as well as other industries which are connected to it. It can even be argued that the overall quality of life through proliferation of computers, communication, medical electronics and other industrial and consumer electronics has benefitted from these advances. It is remarkable that the industry has steadily developed more complex chips at ever decreasing cost. The semiconductor cost per function has been reduced at the historical rate of approximately 25% per year. This has been enabled mainly by large research and development investments by the vendors. Up to this point it is clear that manufacturing costs in the past as well as in the future play the dominant role of semiconductor manufacturing. [7] [11] [12]

Unfortunately the cost of production testing has not kept pace with the rapid cost reduction in wafer fabrication described above. It has been shown that there has been no significant cost reduction over time. This trend is recognizable in Figure 4, where the ordinate illustrates both the costs for manufacturing as well as costs for testing a transistor in US cents. The main reason is that higher levels of integration on an IC lead to rising test times. Furthermore, this additional test time leads directly to constant or slightly increasing test costs over time. Thus the test time and their costs cannot be similarly reduced as the wafer

fabrication costs. Especially for mixed signal ICs, testing is perhaps the fastest increasing portion of manufacturing costs. The acceptable cost of testing is very market specific and must be determined by balancing the value, and furthermore, the quality of testing with its costs. [7] [11]

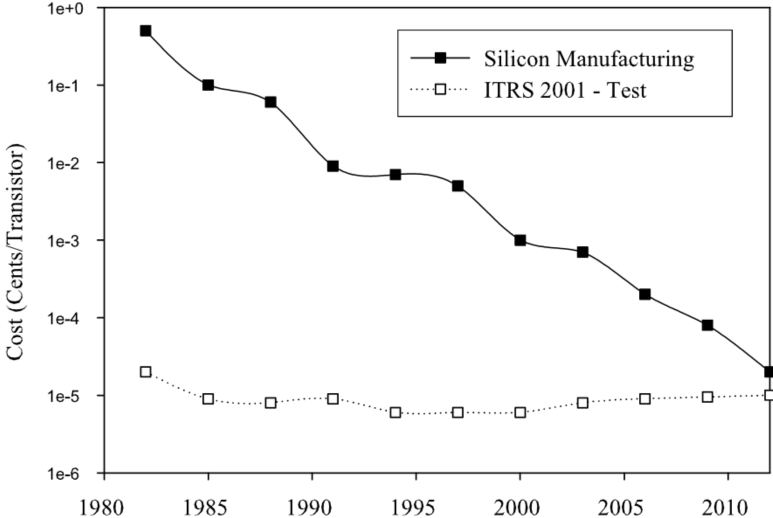

Figure 4: Trend in Test Cost versus Manufacturing Cost per Transistor [7, S. Bahukudumb, Figure 1.1, 2011, site 2]

Generally test costs include the cost of automatic test equipment (ATE) and the cost of test development and depend on yield as well as throughput [4]. However, determining the exact cost of production testing is not a simple task and results in complex cost models, which are not further discussed here. The simplest possible model is shown in equation (1), where C_{Test} are the costs of test, $C_{per\ Sec}$ relates to the test costs per second and t_{Test} represents the test time in seconds. [2]

$$C_{Test} = C_{per\ Sec} \cdot t_{Test} \tag{1}$$

Equation (1) shows that test time reduction is one of the main possibilities to increase profitability. So, “time is money”, especially when it comes to manufacturing testing. The challenge for the test engineer is to perform accurate measurement and, furthermore, to do this as quickly as possible to reduce production costs. [2]

A fact is that the costs of any production process are most impacted by the two factors of yield and throughput. Yield is defined as the percentage of products that meet the required specifications. It is the case that the yield of manufacturing is contrariwise proportional to the costs of it. An increasing yield tends to produce more conforming ICs, which leads

directly to lower costs of the same process. However, if it is the case that too many faulty ICs are being produced, then the manufacturing cost of those bad parts will have to be recovered from the price charged for the faulty devices. Yield is probably the most important index in the semiconductor manufacturer for measuring success in the IC business. [13]

The components of the overall yield ($Y_{overall}$) for a semiconductor manufacturer can be separated into several components over the whole manufacturing process. The yield portions discussed here are related directly to the process steps defined in the introduction (see 1.4) and can be written as in equation (2) [12]:

$$Y_{overall} = Y_{fabrication} \cdot Y_{wafer\ sort} \cdot Y_{assembly} \cdot Y_{final\ test} \tag{2}$$

With regard to the two types of tests described in the introduction, also the yield of any test insertion Y_{test} can be separated into functional yield $Y_{functional}$ and parametric yield $Y_{parametric}$ such that (3):

$$Y_{test} = Y_{functional} \cdot Y_{parametric} \tag{3}$$

Parametric yield $Y_{parametric}$ refers to the quantification of IC performance that is caused by process parameter variations. The designer attempts to increase parametric yield using several tools to check the design for process and parameter variations. Functional yield $Y_{functional}$ is related to manufacturing problems such as dust particles, mechanical damage, and crystalline defects which cause ICs not to function. Therefore, functional yield is a reflection of the quality of the manufacturing process and is often called the manufacturing yield or the catastrophic yield. The last sub-yields are the two portions of a functional yield. So the functional yield can also be further separated into systematic as well as random yield (4). [12]

$$Y_{functional} = Y_{systematic} \cdot Y_{random} \tag{4}$$

Systematic yield is reduced by any kind of process-related non-random defects. $Y_{systematic}$ is usually known and hence controllable, and is often equal to one. On the other hand, the random yield Y_{random} is not known and is controlled due to statistical models based on defect observations and investigations. The random yield typically dominates the functional yield in high-volume productions. Systematic as well as parametric yield losses occur

typically in early process stages for newly defined products. With the help of statistical methods like SPC (statistical process control) it is consequently possible to ramp up these two yield components. This is also the reason why these process development phases are called "yield learning" for "yield ramp-up". For the goal of yield ramp up, electrical manufacturing tests are one of the prime sources for yield learning. [12]

Another economically important factor it the so-called throughput. Throughput is simply defined as the number of conforming products processed per unit time. The testing throughput refers to the average number of passing DUTs per time unit, which is usually declared in terms of UPH (units per hour). High throughput also leads directly to lower production costs. It is clear that test time for a passing DUT is the dominating factor. Semiconductor manufacturers spend a lot of time and money reducing the test times and so increasing the throughput. [2]

Beyond this, the two last fundamental goals for a successful company are high quality as well as high reliability. Testing is mainly responsible for the quality of mixed signal devices and because of process variations it is absolutely necessary. Typical process variations are the main reason for defects on wafer and some examples are: impurities in semiconductor material and chemicals, dust particles and incorrect temperature control. Best quality can only be derived from a stable and well controlled manufacturing process. An effective back-end process aims to remove all nonconforming products before they reach the customer by testing. Beyond the elimination of faulty parts, quality improvement can also be achieved by the reduction of such variability in processes and products and testing delivers direct feedback. Trade-offs are usually necessary to obtain the required quality level at minimal cost, and this is the cardinal goal of testing. [13]

The definition of quality with regard to testing can be specified in terms of test escapes, which is the fraction of faulty chips among the ICs that pass the test. The customer will be only satisfied if faultless ICs are delivered. The number of test escapes are sometimes also called the defect level and are commonly expressed as parts per million (ppm). A common way to determine the defect level is to observe the user's feedback in terms of the field return data. There returned materials (RMAs) are nonconforming ICs, which leave the manufacturing facility, fail at the customer and are returned to the manufacturer. Some scenarios when this could be the case are:

- Failing incoming inspection (discussed in the next section 0 Acceptance Sampling)
- Failing a system test. A PCB fails because of a faulty IC on it, but once the chip is replaced the system works properly. The replaced chips are afterwards returned to the chip supplier.
- A maintenance test is carried out on a system once an operational failure occurs. After the faulty system part is located usually the whole PCB board is replaced, so that the system goes quickly back into operation. If the system is running again, maybe the faulty chips on the board will be found and replaced. The faulty chips are afterwards returned to the chip supplier.

These are some typical examples of RMAs in the semiconductor industry. The returned chips can be very valuable in delivering a quality measurement as well as an insight into the manufacturing process. The aim of the examination of the returned chip is to find the causes of failures. These causes may point to areas of potential improvement in specification, design, fabrication or test. Such improvements can increase the yield as well as reduce the defect level. Depending on the application for mixed signal ICs, a defect level of 500 ppm may be acceptable and 100 ppm or lower represents high quality. [4]

Another very important aspect of quality for semiconductor products is their reliability. “Reliability is a characteristic of a product that is associated with the probability that it will perform its intended function under specified conditions for a stated period of time.” [10] The improvement of reliability is usually accomplished by FMEA (failure-mode and effect analysis), which is aimed at identifying the mechanisms for failure and draw conclusions to the design and manufacturing processes. The reliability of integrated circuits is also directly impacted by the manufacturing process. High reliability also results from the minimization of manufacturing defects and is directly correlated to the overall yield of a production. However, although the reliability of integrated circuits is a very important quality topic, the detailed study of it is beyond the scope of this thesis [12].

The main goal of ams AG is to develop, produce and provide products and services of the highest quality and reliability to the market. The quality management system is designed to satisfy customer needs and expectations. Therefore all the technical, administrative and human factors affecting the quality of products and services are geared towards the reduction, elimination and most importantly, prevention, of deficiencies. The Quality and

Environment Department of ams AG handles all those activities normally defined as quality control, quality assurance, quality and environmental management, as well as reliability. ams AG product assurance and environmental activities are based on ISO 9001 [14], ISO/TS 16949 [15] including semiconductor commodities, as well as ISO 13485 [16] Furthermore, the company is certified according to environmental standards ISO 14001 [17] and the European EMAS scheme. The test related procedures and methods closely follow the requirements of JEDEC and/or MIL-STD-883 [18].

The quality policy has the goal to achieve customer satisfaction by:

- Meeting and exceeding customer expectations
- Achieving a zero defect rate from the start through the application of failure prevention methods in product and technology development and continuous improvement to end-of-life
- Reducing production costs through improvement of process yield as well as reduction and elimination of quality deficiencies
- Ensuring on-time completion of projects, prompt response to offers and enquiries and resolution of problems by the implementation of clearly defined and closely monitored and controlled business processes

[19]

Acceptance Sampling

The purpose of acceptance sampling is quality assurance based on sampling, and afterwards comparing the attributes' adherence to a standard. Thus the aim of acceptance sampling is to make an ultimate decision about the disposition of attributes of a large lot or batch, based on a random sample of units. Attributes are discrete data often taking the form of counts. For semiconductor testing a unit can be understood as a single IC and its proper attribute is faulty or not faulty, based on prior pass or fail decision. In the context of testing, inspection and decision making regarding products is for the purpose of acceptance or rejection. Acceptance Sampling is a common method of quality assurance (QA) for ams AG and is used in different stages of the production flow. Additionally, the customer may also use sampling procedures. [20]

The first example where acceptance sampling is used is the so-called QA test. The purpose is to verify the correctness of production test. Therefore randomly dies are inspected again after they have passed the common production test. This is done at both the wafer sort and final test. The QA test is generally the same as the proper production test for the same product, but in terms of test limits they differ from each other. As already mentioned, in production testing the manufacturing test limits are derived from statistical calculations and are usually tighter than specification limits defined for the customer. For the QA test the limits are the same as the production limits, or might be closer to the customer limits. Single sampling plans according to the MIL-STD-105 [21] and ISO 2859 [22] international standards are used for the whole sampling procedure. For accepting or rejecting a random drawn sample of ICs, a single sampling plan based on AQL (Acceptable Quality Level) values is used. [23]

Another application of acceptance sampling is the following. It is quite common in the industry that after purchasing ICs the customer also performs an incoming inspection before integrating them into a system. Typically this testing is pretty similar to production testing, or even tuned to specific customer requirements. It is also mainly the case that only a random sample with the sample size depending on the product quality (AQL[2] value) and the

[2] Definition: "The AQL represents the poorest level of quality for the supplier's process that the consumer would consider to be acceptable as a process average." [22, Montgomery, 2005, site 654]

system requirement is inspected, instead of testing every single IC. The aim and the most important purpose of this testing is to avoid placing defective devices in a system assembly. The cost of failure diagnosis of later production steps than incoming inspection may far exceed the cost of it. In the electronics industry it is widely accepted that there is an existing "rule of ten" concerning costs of finding a fault in different levels of product integration into a system. If a defective IC is not caught by chip testing it costs ten times as much at the next assembly level, for instance on a circuit board, as at the chip level [4] [24].

If, for example, the customer accepts a certain defect level of the purchased product, which is normally fixed per contract, acceptance sampling is also carried out at ams AG. Normally this goes hand in hand with a price discount. Therefore a certain AQL value is agreed and the manufacturer only applies a sample test instead of a 100% inspection of the delivered ICs. The sampling plan includes the size of the sample which has to be drawn as well as the acceptance number. The acceptance number is the maximum number of nonconforming units that are allowed. This means that once the number of faulty ICs within the drawn sample exceeds this number the whole sample is rejected. The consequence would be a 100% full test of the whole wafer. However, it has to be added that a sampling plan depends on the AQL value as well as on the lot size, which is usually the number of dies on the entire wafer. Usually the sample size is 5 to 50% of the wafer. At ams AG, the so called "monte sort algorithm" is used for this purpose. It has the capability to automatically switch to a 100% wafer sort if the yield is below the expected level. Additionally, the algorithm is able to estimate the yield of the untested dies of the wafer and thus makes it possible to reconstruct the entire wafer map. [25] Again, the sampling plans are derived from the MIL-STD-105 [21] and ISO 2859 [22] standards.

Summary: Problem and Aim of Thesis

The prospects of Adaptive Testing for concrete products from ams AG are analysed in this thesis. The analysed products are selected high volume integrated circuits from all business units, including devices for medical and healthcare applications. The aim of the thesis is to point out the potential of test time reduction and the impact on the quality of the product, based in particular on the quality management system. The challenge was to optimise the test routines without concessions to quality. Therefore algorithms for adaptive test are

derived and implemented for tests in wafer sort and for the final test. The focus is also on the comparison of the adaptive methods developed with common semiconductor tests.

2 Methods

Adaptive Test, State of the Art Recherché

A recherché was conducted at the beginning of this thesis in order to become familiarised with the topical subject of adaptive test and get an overview of the latest developments. Initial research has been shown that there is still very little literature on this subject, and no written books have been found yet. Thus the focus has been mainly reduced to an internet search. Internal company documents as well as the direct contact with the company's tester vendors have been used as additional sources of information, which consist mainly of conference papers and presentation materials. Table 1 displays the detailed method of the main literature review, which took place in July 2011. The search enquiry column shows the logical linked search keywords for the IEEE Xplore search engine, which took place in the "Title", "Abstract" and "Keywords" section of the library. For the Google Advanced Search the search words are by default linked with an logical "AND" operator, and the "-" indicates an exclusion of the word. The double quote sign means that a search for exact group of words is used with both search engines. Furthermore, in the IEEE search the results were refined by choosing an appropriate scientific topic and an actual publication year for the quite young topic of adaptive test since it was first introduced by the ITRS in 2009, as mentioned in the introduction. Finally, the manual reading of abstracts and the web presence of homepages was the last filtering step and has lead to the basic framework of this thesis. The number of selected and afterwards reviewed documents per search engine can be found in Table 1 in the last column. The exact listing of the used and referenced literature can be found in section 6, the Bibliography of this work.

Table 1: Search Enquiry and Method of the Internet Recherché/Literature Review

Search Engine	Search enquiry	Without the terms:	In specific topic	Publication Year:	Result	Reviewed Documents
IEEE Xplore Digital Library	(((Document Title:"adaptive test") OR Abstract:"adaptive test") OR Author Keywords:"adaptive test")	not selected	○ Computing & Processing (Hardware/Software) ○ Components, Circuits, Devices & Systems ○ Signal Processing & Analysis , ○ Power, Energy, & Industry Applications , ○ General Topics for Engineers (Math, Science & Engineering)	2005 - 2011	**56**	**12**
	(Document Title:"adaptive testing") OR Abstract:"adaptive testing") OR Author Keywords:"adaptive testing")	not selected	○ Computing & Processing (Hardware/Software) ○ Components, Circuits, Devices & Systems ○ Signal Processing & Analysis , ○ Power, Energy, & Industry Applications , ○ General Topics for Engineers (Math, Science & Engineering)	2005 - 2011	**66**	
	((((Document Title:"adaptive test") OR Abstract:"adaptive test") OR Author Keywords:"adaptive test") AND semiconductor)	not selected	all topics	no limitation	**13**	
	((((Document Title:"adaptive testing") OR Abstract:"adaptive testing") OR Author Keywords:"adaptive testing") AND semiconductor)	not selected	all topics	no limitation	**3**	
Google Advanced Search	"adaptive test" semiconductor wafer -psychology –exam –education –patent -patents	"psychology" "exam" "education" "patent" "patents"	not available in Google Advanced Search	no limitation	**991**	**9**

Adaptive Test Simulation Tool Development

In the following chapter, the software tool which has been developed for the simulation of adaptive test using real production test data is described. There were basically no precise specification or limitations on the part of the company about the way the software should be implemented. The only thing that the software needed to support was the use of test data arising from the daily chip production. This test data is stored in the standardized data format, the so-called Standard Test Data Format (STDF™). STDF™ (Teradyne Inc., North Reading, USA) in the current version 4 is a flexible and portable data format which provides the compatibility of test result data between test systems of different manufacturers and is the established standard in the semiconductor industry [26]. These data contain all the information and results about the conventional production test and it is specified by ams AG that one closed STDF file should include data from one test session. For the wafer sort this means that the file includes all the test data from one tested wafer. For final test, where the wafer is not present any more, the test data is stored into STDF files after every hour at ams AG.

2.1.1 Development Environment

Because of the already existing interface library to access STDF™ data and the comprehensive mathematical and statistical functions and utilities, the adaptive test simulator was built with the following development environment. The highest abstraction level of the software modules for the simulation tool is illustrated in Figure 5. The core operating system is Windows XP with Service Pack 2 installed (Microsoft Corporation, Redmond, USA).

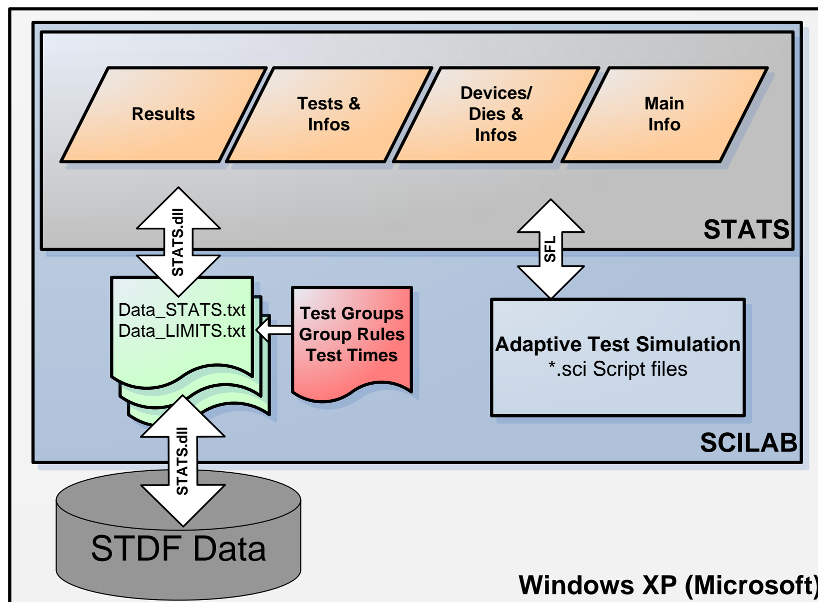

Figure 5: Software Environment and Modules of the Offline AT Simulation Tool

The main development software, including the interpreter for the developed source code, is SCILAB (The Scilab Consortium (Digiteo), Chesnay Cedex, France). SCILAB is a comprehensive, powerful and free software package for applications in numerical programs and can be seen as an alternative to the Matlab (Mathworks Inc., Natick, USA). SCILAB is a high-level language using an interpreted programming environment with matrices as the main data type. [27] STATS (DIAWA-Wawrina KEG, Graz, Austria) is an application for graphical and mathematical analyses of test data specified for microchip production test data and can be seen as an customized extension of SCILAB. The interface from STATS to raw data in STDF™ format is realized with a DLL (dynamic link library) named STATS.dll (see Figure 5). It contains the relevant basic functions like flexible storage of data, fast data access, quick filtering and is realized with attention to the performance. To have a fast, efficient and transparent data management, a proprietary ASCII conform data format has been introduced by STATS. If a STDF™ File is loaded, the converter DLL reads the STDF file and writes the test data into two files in STATS ASCII format. [28]

- *STATS LIMITS File:* *"STATS_Filename_LIMITS.txt"*
  This file includes a table with all the test names, test units, unique test ID's and test limits [28].
- *STATS File:* *"STATS_Filename_STATS.txt"*
  This file shares the information about all measurement values per test as well as of all devices tested [28].

The main application for the adaptive test simulation is also realized with the SCILAB scripting language by using *.sci script files. With the help of an included STATS function library (SFL in Figure 5), STATS offers a very efficient way to access test data in such script files. With these software modules it is consequently possible to load the test data directly into the main memory of the software environment, which is the base on which to develop an adaptive test simulator. In summary, the software environment discussed up to now provides the following data access for arbitrary adaptive test simulation software:

- Main information
    - ATE name
    - Date and time of the test session
    - Unique production lot[3] number
    - Unique wafer number
- Test information
    - Unique test numbers
    - Unique test names
    - Upper and lower test limits
    - Test times
    - Test groups and group rules
- Die information
    - Unique die numbers
    - Coordinates, x and y position on the wafer
- Test results
    - Measurement value for each test of each die

To be able to back close to test times within the simulation, the individual test times for each test are added additionally to the STATS LIMITS file. This is necessary because test times are not logged by default in conventional company's production STDF data. Hence it is only possible to calculate test time reductions within the algorithm if the simulation knows the exact execution times for each test. The STATS LIMITS file is a table, which contains all important information of tests which are available for each DUT. For the purpose of additional test time information for each test, the table is extended by an additional test time column. In the same way, information about test groups and special rules for these groups are added to the simulation. The exact meaning of this additional information is represented in 2.1.2 on page 28. By using the framework described until now, it is possible

[3] In the company it is practice that 25 wafers are grouped into a so-called production lot.

to access all this data with any adaptive algorithm and generate a full adaptive test simulation.

The simplified architecture of the software and the appropriate data interfaces for an adaptive test simulator can be seen in Figure 6 and are described in the following section. Again the wafer sort is used to describe the processes.

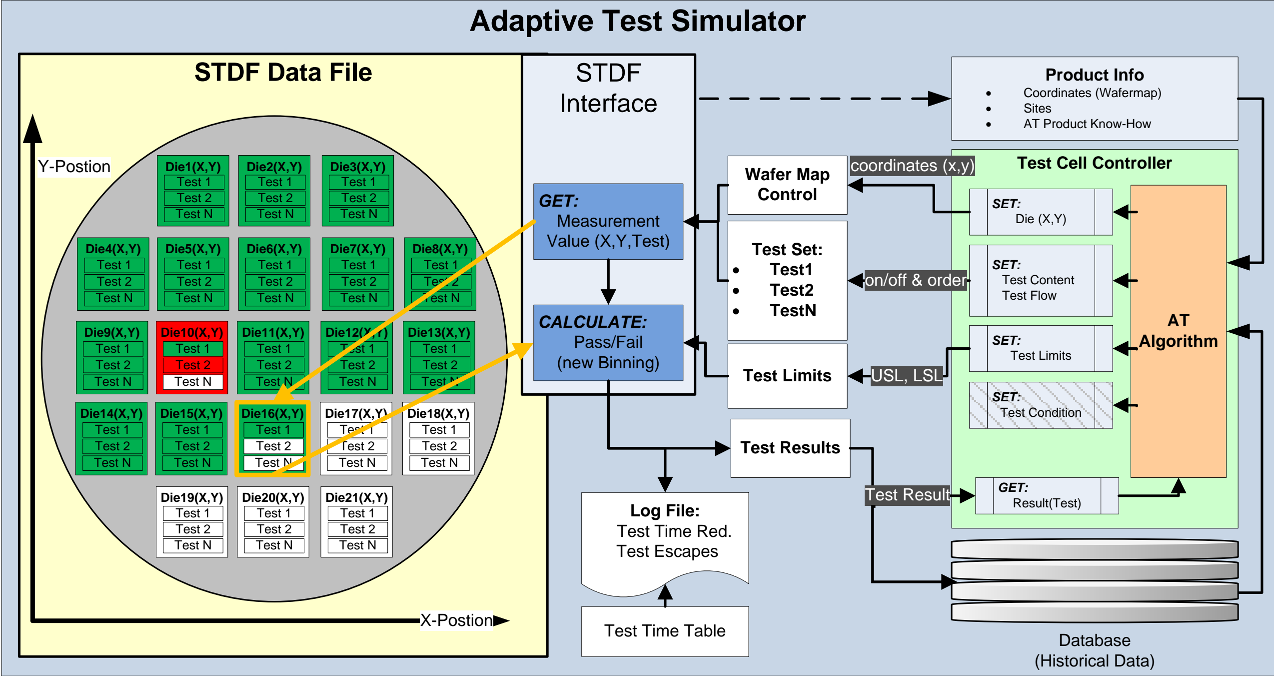

Figure 6: Software Architecture: Interfaces and Functional Blocks of AT Simulation Tool operating with Offline STDF Data

In principle, the AT simulator in Figure 6 differs only marginally from the real AT setup described in the introduction and shown in Figure 3. The main difference to a simulation is that the whole wafer sort has already taken place and measurement results are available in the form of STDF data. Thus, for all tests of each die the test results are stored in the STDF file, which is represented by the yellow block in the figure. By comparing Figure 3 with Figure 6 it can also be seen that, instead of the ATE the test session is controlled by the adaptive test simulator software block, in which no hardware is present. The main concept and framework for the test cell controller, which is displayed in green colour, is basically equivalent to those used in a real AT. It also has the same capability and functionality of making adaptive decisions by a given test set, but with one exception. It is not possible to modify the test conditions afterwards, which usually has an impact on the test results. This is the case because the test has already taken place and the measurement value is already pre-recorded in the data file. The test cell controller in the simulation has no physical presence

and is a fully virtual functional block. This is also the case for the wafer in Figure 6 which includes its virtual occurrence in the form of an STDF file. To get access to the test data an interface must be introduced, which is illustrated by the STDF Interface block in the figure. The functionality of the STDF interface is to provide requested test results to AT algorithm. The STDF interface has to know which measurement value is wanted, thus the request of the test cell controller has to include the information of the wanted X/Y coordinates of the DUT. Furthermore the corresponding test is also needed to get the correct value. This is carried out by the GET function within the STDF interface block. The queries of the AT algorithm to the data is again provided by the GET and SET functions within the test cell controller, as in Figure 3 in the introduction. The STDF data includes the information about the pass/fail information of each DUT, because the test has already taken place. The pass or fail information of DUTs is also known as binning. This binning information of the conventional test may not be the same as for the adaptive test. Because the omission of tests it can, for example, be the case that a test is never performed during the simulation which would have a fail in the conventional procedure. Thus the DUT would be declared as faulty due to conventional testing and on the other hand pass the adaptive test. This is an undesirable scenario and would lead into test escapes but must be considered. Therefore the STDF interface has to do a re-processing of the pass or fail decision. A new binning is made for all tests that were performed and tests that were never executed must be ignored. This represents the second function block within the STDF interface block. Another aspect which must be considered is that if an adaptive method with limit changing abilities is used, it is also necessary to recalculate the binning information. However, the presence of the real results within the STDF data offers also the ability to validate the algorithm. By comparing the simulation results with the real data it is subsequently possible to judge the reliability of the algorithm concerning failure coverage and test escapes. Because the test times are not logged by default at ams AG STDF data, this information is added externally to the simulation (Test Time Table), as described previously. This enables the simulation to calculate the test time savings by reason of skipping tests. After the simulation took place, the software saves the test time reduction as well as the test escape information into a log file.

2.1.2 Simulation Rules and Limitations that arise due to the Properties of a real Production Test

To make the simulation as realistic as possible, it is necessary that the algorithm acquires some IC- or product-specific knowledge concerning its tests. The first point is, that a restriction for the AT algorithm is based on the functionality of a conventional test program. In such a test program it is usually the case that before a test takes place the measurement instruments and modules of the testers (ATE) must be selected and adjusted, or even calibrated, by software. This test setup usually takes a certain time and no test can be executed during this period. Because of this the goal of the test program developer is to execute all the tests which require the same setup immediately afterwards. It may also be the case that one and the same test is performed with different conditions or qualities sequentially. Because of this, it would make no sense to perform such tests on their own since the test setup time plays a significant role. But if the test setup were set once, more measurements could be performed almost without delay. As a result, it makes sense or is necessary to merge single tests into groups of tests (Figure 7). The basic concept of how AT algorithm deals with groups is that the whole group can only be switched on or off. In the simulation, only if the AT decision is that every test within this group can be omitted can the whole group be allowed to be skipped. As soon as one test within this group has to be executed, the whole group has to be switched on, although other tests may be allowed to be omitted by the software. By definition, for the simulation it is also possible that one group consists only of one test, which makes it possible again to represent a single test. It is also defined that tests which belong to the group with the number 0 are ignored by the algorithm. So by setting a test's group number to zero the test will be not part of the simulation.

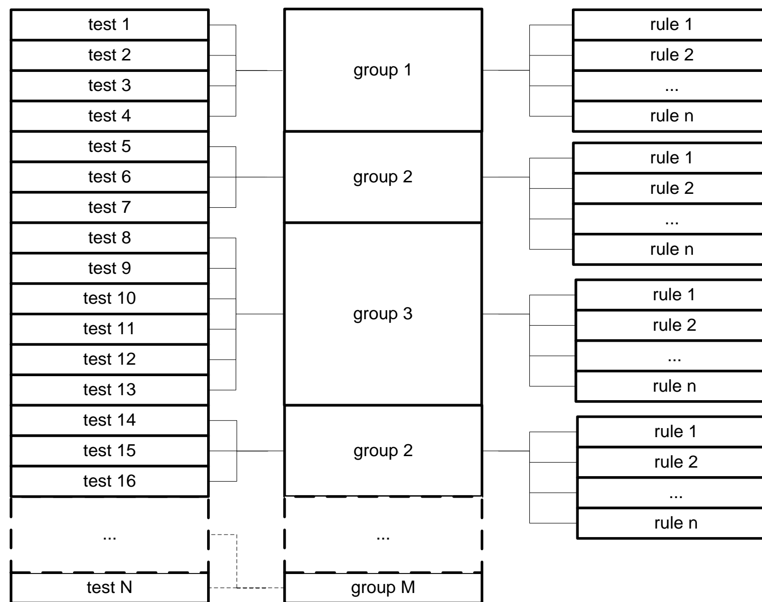

Figure 7: Grouping of Tests for AT Simulation as well as Group Rules and Restrictions for each Group

Moreover, as also displayed in Figure 7, different rules have been defined for any group of tests, which allow the simulation to map the nature of a real test as realistically as possible. This is a kind of special product know-how which has to be implemented offline specifically for each product.The following group rules which guide and restrict the skipping of the tests are defined:

- **Rule 1: Global Execute**
  - The test group must be executed on every die of the wafer
  - It is not allowed to skip any die and let an IC untested on the wafer which indicates that sample testing of dies is prohibited

  Example: The customer wants to have a parametric measurement of each IC; Trimming[4] is another Example.

- **Rule 2: DUT Execute**
  - Once a coordinate is selected and a die is under test, the test group have to be executed
  - Sample test of dies is allowed, but once a DUT is contacted the group has to be executed

  Example: Tests with huge defect coverage; Continuity Tests[5]

[4] Trimming: "Many high-performance mixed-signal devices require, for instance, reference voltages that are trimmed to very exact levels by the ATE tester. DC voltage trimming can be accomplished in a variety of ways. The most common way is to use a programmable reference circuit that can be permanently adjusted to the desired level" [2, M. Burns und G. W. Roberts , 2001, site.55]

- **Rule 3: Depend Group**
  - If the test group should be executed, a dependent group has to be executed before
  - The test group can only be skipped if the depending group before was executed or the dependent group is also allowed to be skipped

  Example: A test needs test result from another test before; for example, the offset voltage of an operational amplifier has to be determined before further circuit measurements

- **Rule 4: Skip to End**
  - The group can only be skipped if all following groups in the test sequence are allowed to be skipped
  - No groups in between executed test groups can be skipped in the sequence

  Example: simulation of a test program abortion

- **Rule 5: Optional Group**
  - Instead of the test group, it is possible to execute an optional test group

  Example: Quality improvement, more exact measurement (e.g. averaging), parameter measurement instead of a pass/fail test based on comparing against a threshold

Table 2 summarizes the rules mentioned above and shows how they are implemented in programming language manner. For each rule, if the value of the rule variable has the value FALSE, the rule does not apply. It is necessary to define this control chart for the algorithm for every product to be analyzed. In the course of this work, this step was carried out for each product individually in cooperation with the appropriate test as well as product engineer.

Table 2: Summary of Rules for each Group of Tests in Programming Language Manner

Rule	**Description**	**Variable**	**Value if rule is** applicable
1	Always execute on every IC	global_execute	TRUE / 1
2	Always execute if IC is tested	die_execute	TRUE / 1
3	Only skip/execute if group *M* skipped/ executed	depend_group	M … group number
4	Only skip if all following groups can be skipped	skip_to_end	TRUE
5	Optional group *M* available	optional_group	M … group number

The information about the test groups and their appropriate group rules are implemented as an extension of the STATS LIMITS file. This is also necessary for the test times of each test as

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[5] "The purpose of the continuity test is to verify that all the electrical contacts between the tester and the DUT have been successfully connected. If a large percentage of devices fail the continuity test, this indicates a probable error in the tester hardware" [6, M. Burns und G. W. Roberts , 2001, site.40]

already described in section 2.1.1. Each test time test group and rule is added to the file by an additional column. A table of such an extended STATS LIMITS file is displayed in Table 3 in the next section, 2.1.3.

There are further additional following restrictions for the algorithm due to the current status of the on-going adaptive test project within the company:

- A wafer map control should not be a part of the simulation because in the near future it is not planned to implement this functionality on real tester equipment. Consequently it is not possible to select arbitrarily any wanted X/Y coordinate on the wafer. The simulation has to select the DUTs in a sequential way, like they are recorded in the STDF data file.
- Only data from the same test session or insertion should be analysed by the algorithm. This restriction is necessary because no access to historical data is yet available on a real production test. As a result, at wafer sort it is not possible to make adaptive decision based on the results of prior tested wafers.
- As already mentioned, condition changing is not possible for a simulation.

Adaptive Test Algorithm

2.1.3 Basic Methods and Framework of the Algorithm

In this section, the algorithm which forms a main part out of this thesis is presented. Making predictions about the behaviour of the devices under test (DUTs) based on statistical data analysis, and afterwards triggering targeted test sets for the DUT is the main concept of adequate adaptive test algorithm. Since at the beginning of this work no specific requirement for the algorithm had pre-existed, the ideas for a realizable program were collected step by step. Thus the algorithm has been further developed during the master thesis. This is the main reason why in the following paper work two algorithms are presented. The first algorithm has the name "**Test- Pareto Algorithm**" and the further development of it is named "**Test- Pareto & PAT- Outlier Algorithm**," both of which are described in detail in the following chapters.

The first concept is realised by adapting the test flow and test content based on all prior measurements of the same test session. To obtain statistics for each test it is necessary to collect data at the beginning of the session by performing all the tests on the first devices. Therefore, initially a control sample has to be drawn. If the information content and the statistical significance are considered to be large enough, the tests which are most likely to fail should be executed. Tests which seem to be under statistical control are allowed to be skipped with the aim of saving test time. Nevertheless, they are not omitted entirely during the further testing process, but sampled sometimes to verify the assumption that they are not likely to fail. The question is now, what are the tests which are likely to fail and which are not? This classification is based on a fail pareto analysis which is updated dynamically during the whole test session. Through a pareto analysis it is possible to identify the most frequently occurring test with fails. So it simply represents a frequency distribution of discrete data arranged by category. The pareto method does not automatically identify the most important tests, but rather only those that fail most frequently [20]. The threshold within the algorithm for the decision of whether or not a test is allowed to be skipped is very strict: Once a test shows an error, it is no longer allowed to skip it in further test session. On the other hand, only tests which never show fails in the prior executions are allowed to be skipped. To sum up, the "Test-Pareto Algorithm" achieves its goal of test time reduction due to a test sampling procedure based on a dynamic test fail pareto analysis. The aim of the

sampling procedure is to improve test efficiency by only testing as much as is required to meet the outgoing quality target given the incoming manufactured quality level [20]. It is clear that two wafers of the same product with two different yields have the same requirements concerning outgoing quality. The algorithm's task is now to increase the test intensity on the wafer with the worse manufacturing quality compared to the other one. A detailed algorithm description is amongst others presented in the next section (2.1.4).

An improvement concerning fault coverage was added by extending the algorithm with a statistical outlier method. The basic concept here is that if a test differs significantly from an expected behaviour but is still inside of the specified test limits, that part is perhaps bad. So when each part originates from the same production process it is assumed that if a device differs from its population a defect may be the reason for its suspicious behaviour.

"Outlier detection offers the benefits of increasing the defect detection sensitivity (to increase the effectiveness) of a measurement without improving how the measurement is made and being able to detect a defect by fewer or easier to make measurements (increasing test efficiency)." [29] [29, P. O'Neill, site 1]

Generally, outlier methods can be applied to parametric measurements as well as counts of pass/ fail results of functional tests, whereby here only parametric measurements have been used. Specifically, the algorithm developed uses a technique based on the so-called dynamic part average testing (PAT) method. The Automotive electronics council (AEC) publishes a guideline on how to implement this statistical method in detail, with the purpose of removing abnormal characteristics from DUTs. The main concept of dynamic part average testing is to derive suitable limits on measurement parameters based on a moving window of most recently tested parts. The test limits are individually adapted for each DUT with the aim to improve the quality and reliability of the part.

> "Meeting the intent of this guideline, either by performing this method or some other similar method, is highly recommended. History has shown that parts with abnormal characteristics significantly contribute to quality and reliability problems. Use of this technique will also flag process shifts and provide a source of rapid feedback that should prevent quality accidents." [10] [10, AEC, site 1]

As generalized in common statistical process control (SPC), the PAT approach is also to declare data that is more than six standard deviations away from the centre or mean of the process to be outlying data. So if a population of parts is produced with a particular design and the same manufacturing process, it is assumed this will yield in a certain consistent set of test results. So it is normally the case that these data are normal distributed with the statistical parameters – mean and standard deviation- of a gaussian curve. Because common mean and variance values are very sensitive to outliers, more robust statistical calculations are used to calculate the characteristics of the main distribution. The median is also termed the robust mean ($\tilde{x}$) in this context and represents the centre of the ranked data which represents the second Quartile (Q_2). Also for the standard deviation, the more insensitive calculation based on the first (Q_1) and third interquartile (Q_3), which is also known as the robust sigma ($\tilde{\sigma}$) calculation, is used (5). Q_1 is the point 1/4 of the way through the ranked data and Q_3 is the point 3/4 the way through the ranked data. [10]

$$\tilde{\sigma} = \frac{Q_3 - Q_1}{1.35} \quad (5)$$

The higher (PAT_{HL}) and lower (PAT_{LL}) PAT limits afterwards are calculated, as mentioned before, based on the assumption of a six sigma process according to (6)(7). [10]

$$PAT_{HL} = \tilde{x} + 6 \cdot \tilde{\sigma} \quad (6)$$

$$PAT_{LL} = \tilde{x} - 6 \cdot \tilde{\sigma} \quad (7)$$

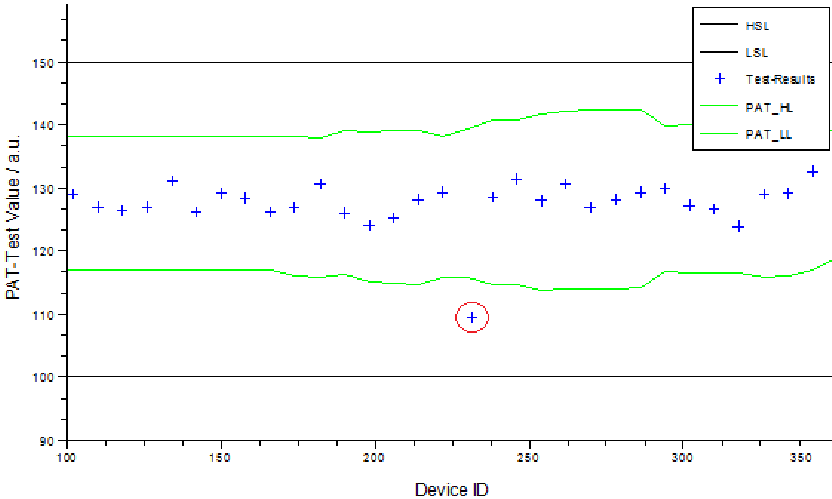

Figure 8: Trend Plot with Example of a Typical Outlier Outside the PAT Limits

Figure 8 now shows how the PAT limits (PAT_HL and PAT_LL) adapt dynamically and individually for each device based on a data set of measured devices from the same production process before. At the beginning of a test, when only a few results are available, instead of the dynamic limits only the common production limits can be used for testing. In Figure 8 the trend plot begins at the hundredths tested DUT, so enough measurements are present do apply the statistical calculations. As shown in the diagram, it is generally the case that the specification limits (HSL and LSL) are looser than the PAT limits. This is the case because specification limits are often established on a huge amount of test data and under different test condition (e.g., temperatures), which results in a higher process variation than looking at the data through a window as the PAT method does. But it should never be the case that PAT limits exceed the specification limits and must be prevented by the algorithm. How many data points are used to calculate, and what the consequence is if a data point exceeds this dynamically calculated PAT limits, like the point within the red circle in Figure 8, is discussed in the course of the next section.

The guideline suggests: "PAT limits should be used for all electrical tests if possible, but shall be established for at least 8 important characteristics …" [10] [10] [10, AEC, site 5]

Important Characteristics are defined as device characteristics that could impact product quality and reliability. They provide the most significant information if a part is working properly. This implies tests with high defect coverage which use PAT limits during the ATE testing. What kind of test is meant in particular is not discussed further here. The detailed list of test types can be reviewed in the PAT guideline [10]. The important characteristics are termed PAT test for the products analysed in this thesis and have been defined and worked out together with the proper test and product engineer. To inform the simulation about the PAT tests which should selected the STATS LIMITS file was again extended by a column. A logical one in the corresponding row of the table indicates a test with PAT limit calculation. Table 3 now shows an example of the entire extended STATS LIMITS which additionally includes the test times, test groups, the 5 group rules, and is completed by the PAT test column.

Table 3: Extended STATS File with Additional Information and Rules for a Proper Adaptive Test Algorithm.

Index	Parameter	testunit	TestNumber	LSL	USL	TestTime (ms)	TestGroup	global_execute	die_execute	depend_group	skip_to_end	optional_test	pat_test
1	CONTINUITY NEG_1	mV	1000	-1000	-300	10.99	1	1	1	0	0	0	1
2	CONTINUITY NEG_2	mV	1000	-1000	-300	0.24	1	1	1	0	0	0	1
3	CONTINUITY NEG_3	mV	1000	-1000	-300	10.99	1	1	1	0	0	0	1
4	CONTINUITY POS_1	mV	1100	300	1000	0.24	1	1	1	0	0	0	1
5	CONTINUITY POS_2	mV	1100	300	1000	10.99	1	1	1	0	0	0	1
6	CONTINUITY POS_3	mV	1100	300	1000	0.24	1	1	1	0	0	0	1
7	VBIAS_AND_CURR.VOLT_VDD_MAX/VBIASA	V	1	9.84	12.1	40.7	2	1	1	0	0	0	1
8	VBIAS_AND_CURR.CURR_VDD_MAX/VSUP	uA	2	100	150	51.86	3	1	1	0	0	0	1
9	VBIAS_AND_CURR.VOLT_VDD_MIN/VBIASA	V	3	9.84	12.1	37.97	4	0	0	0	0	0	1
10	VBIAS_AND_CURR.CURR_VDD_MIN/VSUP	uA	4	90	140	11.85	5	0	0	0	0	0	0
11	LEAKAGE.NEG.TESTEN/TESTEN_VI16	uA	1400	-250.00002	-50	10.07	6	0	0	0	0	0	1
12	LEAKAGE.NEG.FORCEZERO/FORCE0_VI16	uA	1410	-21	-7	0.12	6	0	0	0	0	0	1
13	DC_OUTPUT.VOUT_MIN/OUTP_OVI	V	5	0.43	1.04	10.04	7	0	0	0	0	0	0
14	DC_OUTPUT.VOUT_MAX/OUTP_OVI	V	6	0.43	1.04	6.63	8	0	0	0	0	0	0
15	AMPLIFICATION.GAIN_10KHZ/OUTP_OVI	[%]	7	58.900002		666.07	9	0	0	0	0	0	0
16	AMPLIFICATION.GAIN_100KHZ/OUTP_OVI	[%]	8	70.899994		0.31	9	0	0	0	0	0	0
17	OUT_RES.GAIN_OUT_100OHM/OUTP_OVI	[%]	9	50.799999		0.22	9	0	0	0	0	0	0
18	TDI-Time-Stamp/	s	8000042			0	0	0	0	0	0	0	0
19	NOISE.NOISE_COUNT_INFO/OUT_DIG	-	10			681.43	10	1	1	0	0	0	0
20	NOISE.NOISEVOLT/OUT_DIG	uV	11	2	7	0.3	10	1	1	0	0	0	0

2.1.4 Detailed Algorithm Description

Until now it has been assumed that only one physical device is investigated for each test run. In recent years a common and increasingly used feature in ATE is multisite capability. Multisite testing is also known as parallel testing and is a process in which multiple devices are simultaneously tested with the same contacting unit. This leads to obvious savings in test costs. The number of site refers in general to the number of parallel testable DUTs. Duplicate tester hardware and instruments must be added to the tester for each site to allow simultaneous testing on multiple DUTs [2]. If multiple sites are present, also the test list is executed in parallel on the DUTs, thus it is not possible that any site applies a different test program than others. For the adaptive test algorithm this implies that one test set is executed simultaneously on multiple DUTs, and depending on the number of multiple tested ICs more than one test result per test may be returned. The contacting process of one or multiple DUTs is termed touchdown. So depending on the number of sites, it may be that multiple physical devices are simultaneously tested during one touchdown. Furthermore the test flow and test content has to be identical for each DUT within one touchdown. From this point, it is clear that adaptive decisions concerning executing or skipping of test groups within the simulation can only be applied per touchdown. This is the reason why in the further course this term is used instead of DUT.

In the following flowchart (Figure 9), the software is described in which both algorithms are included. Hence the Test-Pareto as well as the Test-Pareto and Outlier algorithm are shown in the same flow chart. Table 4 summarizes the parameter of both algorithms. The appropriate values for these parameters are discussed in the next section, 0.

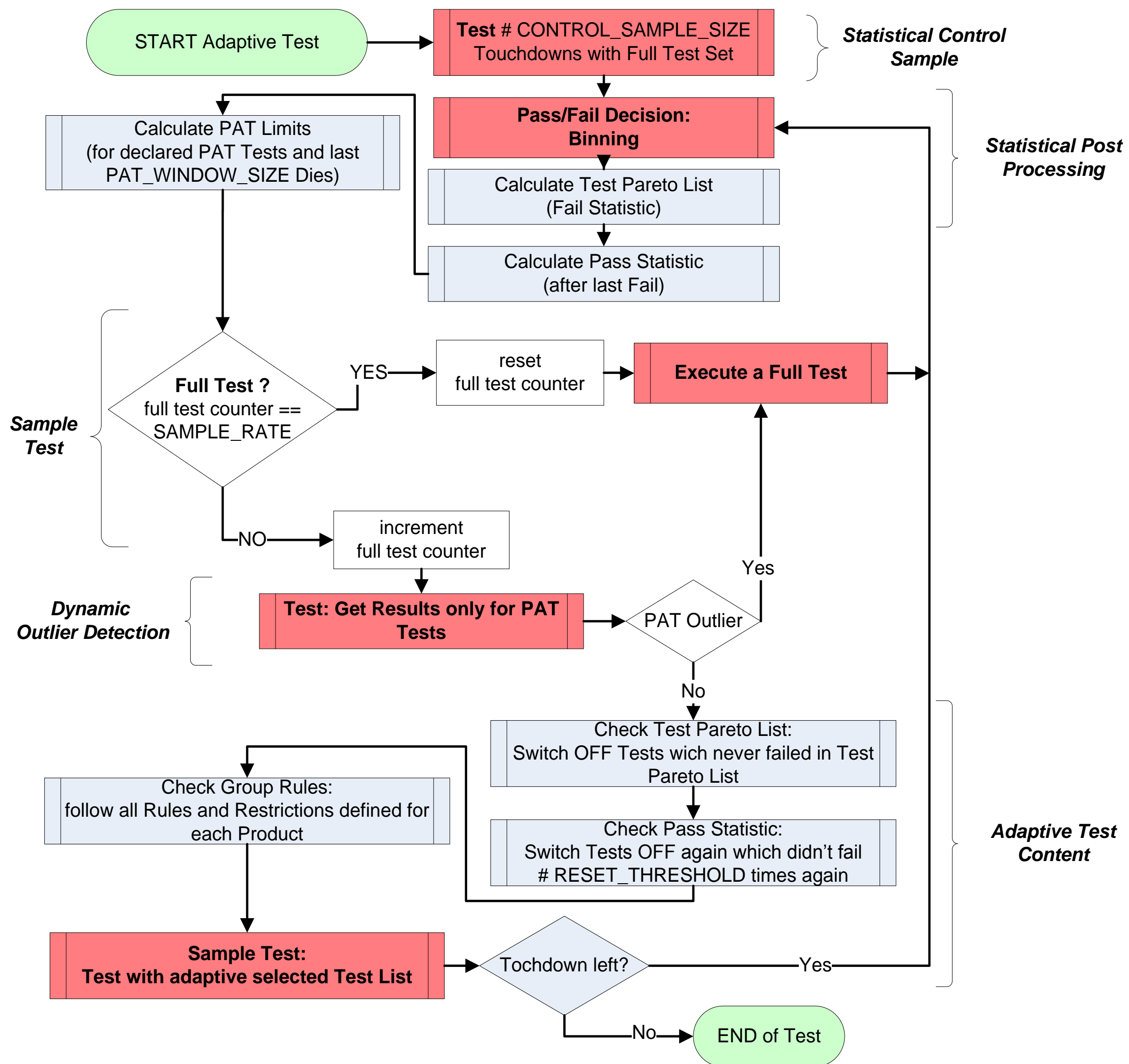

Figure 9: High level Flowchart of the Test Pareto and PAT Outlier Algorithm

Table 4: Parameter Overview

Algorithm Parameter	Description
CONTROL_SAMPLE_SIZE (in % of entire wafer)	Number of touchdowns which are initially tested with full content of test list (full test). Represents the size of the initially drawn control sample.
SAMPLE_RATE (in # Parts)	Number of touchdowns between full tests. Represents the sample rate for full test executions after the initially drawn sample.
RESET_THRESHOLD (in # Parts)	Number of successful results which a test needs which once had a fail, so that it is permitted to be skipped once again. *Example: A test must always be executed because of a fail before (Test-Pareto Algorithm) and now the test hasn't failed the number of (RESET_THRESHOLD) times again. After this the test is reset in the pareto list and is again permitted to be skipped in the following test session.*
PAT_WINDOW_SIZE (in # Parts)	Number of DUTs per touchdown which are used to calculate the PAT limits per site according to equations (5),(6)and (7)

Initially a full test[6] is executed on all the dies within a first number of touchdowns. A red function block within the flow chart indicates a test execution. The number of initially touchdowns is defined by the parameter CONTROL_SAMPLE_SIZE of the algorithm and is the basis for the statistical calculations. The pass/fail decision for the tested DUTs, the binning, is carried out as the next step. Afterwards, the pareto list counts the number of fails for each of the tests performed and is displayed with the Calculate Test Pareto List block. The pass statistic (Calculate Pass Statistic) computes the number of successful results in a row which a test had after it had a fail once before. The meaning of this function will become clear in a broader context. For all PAT tests the outlier limits are calculated, as described in the previous section with the help of the Calculate PAT Limits function. The base for the limit calculation is the last number of devices which are defined by the parameter PAT_WINDOW_SIZE. The PAT limits are calculated separately for each tester site to prevent calculation errors based on variation between the measurement units of the different sites. Subsequently a program counter named the full test counter is used to trigger full test executions in regular steps by comparing the count of this variable with a predefined sample rate (SAMPLE_RATE). As in the first program loop the counter is incremented for each touchdown where no full test is required. Then all the PAT tests are executed and their results are checked to determine if they lie between the calculated individual limits. If it is the case that any test out of all the PAT tests does not pass these limits and the result is thus declared as an Outlier, the DUT is not directly declared as faulty at this point. The algorithm in this case looks in detail at the DUT, switches all the remaining tests on and makes the pass or fail decision based on the specification limits and not as suggested in [10] with PAT limits. So, in the case of a PAT Outlier, the algorithm does not allow the skipping of tests and executes a common full test. If the PAT analysis does not result in an outlier result, the skipping of the remaining tests is, in principle, allowed. The decision, if a particular test is allowed to be skipped afterwards is first based on the test pareto list (Check Test Pareto List). The omitting is only permitted for those tests which have had no fail up to now. On the other hand if a test had only once a fail it would be never allowed to be omitted any more in the remaining test session. Whether a test for example had a fail at the beginning of a wafer

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[6] Full tests means, that the DUT is tested with the full test content. Hence it follows that all the tests within the test list are executed.

sort and afterwards fails never again this would be a very strict decision. To make it possible so reset such a test again, to a test which is allowed to be skipped, the parameter RESET_THRESHOLD is introduced. Thus a test which once had a fail and didn't have afterwards a certain number of executions (size of RESET_THRESHOLD) no new fail again, this test is again allowed to be skipped. The last criterion, whether a test can be left out or not, is decided by the group rule check. This is done to make the simulation as near as possible to a real production test (details see 2.1.2). Finally, all the tests which have to be executed are selected by the algorithm and performed in the next function block (Test with adaptive test set). Since dies or touchdowns are left, the algorithm repeats the same procedure. As a consequence of further program loops the full test counter will increase steadily. Since it is unequal to the SAMPLE_SIZE the omitting of tests will be possible, but if the counter equals the SAMPLE_SIZE, a full test will take place. Once the program is in the branch for full test, the counter is reset to repeat this event periodically. In summary this procedure represents the Test Pareto and PAT Outlier Algorithm. The flowchart without the function blocks dealing with Part average Testing would represent the Test- Pareto Algorithm. This functional blocks are: "Calculate PAT Limits", "Get Results only for PAT Tests" and the if-then-else branch asking for PAT Outliers.

In summary, the algorithm consists of a sample test and a dynamic outlier detection. Based on the different statistical post-processing methods, either targeted adaptive test content or a full test set is executed on the DUT. At the beginning, a statistical control sample is necessary to collect statistical information.

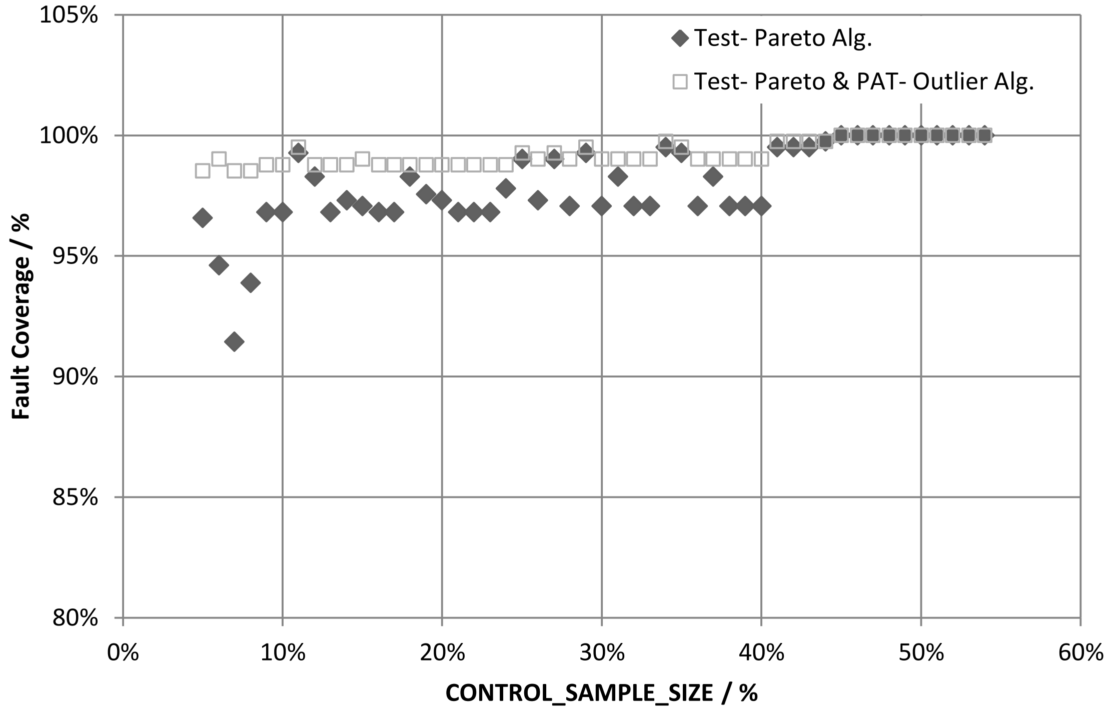
In search of the optimal Parameter Set

To find adequate values for the four parameters of the algorithm described above, an exhaustive search, also known as the brute force method in computer science, is used. In general, the exhaustive search method is a method for optimisation and problem solving. The method is based on the trying of all possible or, at least, of many feasible cases to find a satisfying result to the problem. [30] The best case for the adaptive test simulation would be a big test time reduction without any impacts on the quality of test. This implies the same fault coverage as the conventional test would be desirable. The following diagrams demonstrate that in general a trade-off between fault coverage and test time reduction (TTR) will be needed. In the course of this work five products are going to be analysed with the described AT algorithms. For each of this products' the parameter set was determined in the same way as it now will be described in the following. The listing and details of all products will be presented in the next section 0. For the purpose of explaining the parameter search, the procedure only for the exemplary product E is described in the following. Because of the huge amount of parameter combination possibilities, which would lead into everlasting calculation times, a default parameter set is defined at the beginning of the parameter search (see Table 5).

Table 5: Default Values for each Parameter used for the Parameter Search of the Algorithm in arbitrary units (a.u.)

Algorithm Parameter	Default Value (a.u.)
CONTROL_SAMPLE_SIZE	5%
SAMPLE_RATE	20
RESET_THRESHOLD	4000
PAT_WINDOW_SIZE	40

The following diagrams, from Figure 10 to Figure 13, contain both developed algorithms, giving an insight into how they differ from each other. Each of the diagrams relates to one algorithm parameter and demonstrates its influences on the test time reduction as well as fault coverage. The other parameters, on the other hand, are not varied and set to their constant default values according to Table 4. In all the figures the test time reduction as well as defect coverage is compared to the results of the conventional test in percentage terms. The increasing CONTROL_SAMPLE_SIZE in Figure 10 leads to increasing fault coverage for both algorithms where the Test Pareto and PAT Outlier Algorithm tend to significantly higher Fault coverage. It can be seen that the algorithm inclusive outlier monitoring results in better and more stable fault coverage outcomes than the Test Pareto Algorithm.



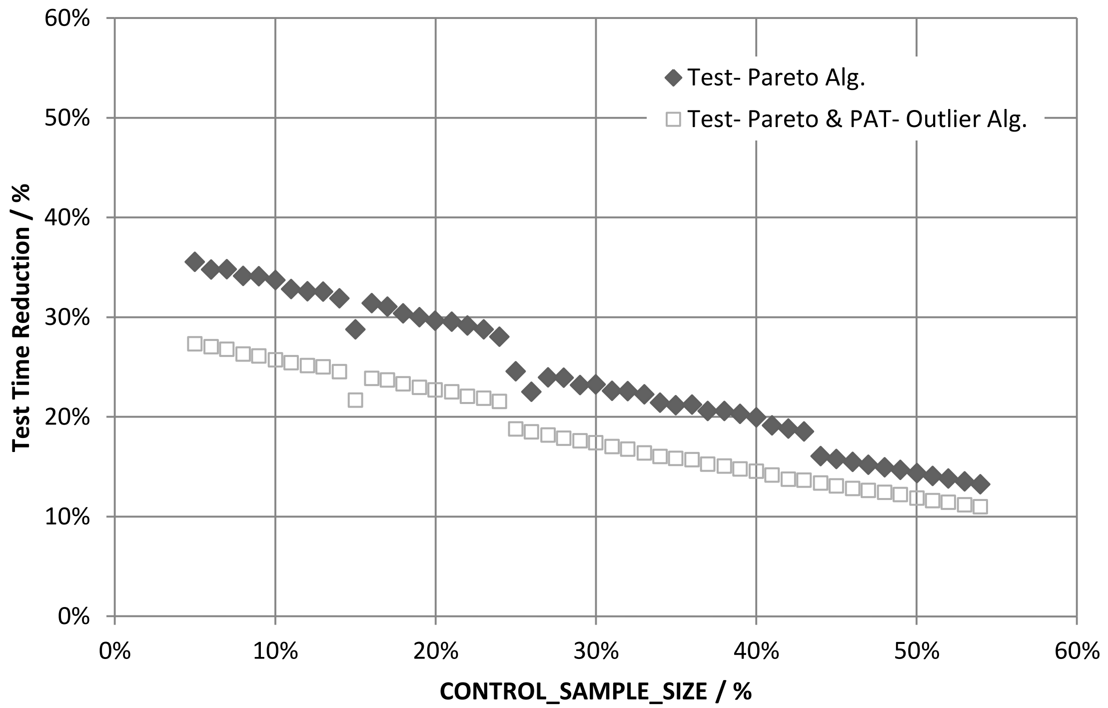


Figure 10: Test Time Reduction and Fault Coverage as a Function of CONTROL_SAMPLE_SIZE

It is clear that if the limit case occurs where the CONTROL_SAMPLE_SIZE is 100%, the fault coverage would be also 100%, since all the dies would be fully tested. Otherwise no test time reduction would be achieved in this case. In order to save test time, the parameter should be decreased. Because of the functionality of the outlier algorithm, which triggers a full test once an outlier occurs, it is clear that less test reduction is possible. This phenomenon is also displayed in the graph by looking on the two test time reduction (TTR) curves. As the following figures also show, on the one hand, the defect coverage tends to be higher and, on the other hand, the TTR is lower for the Test- Pareto and PAT Outlier Algorithm.

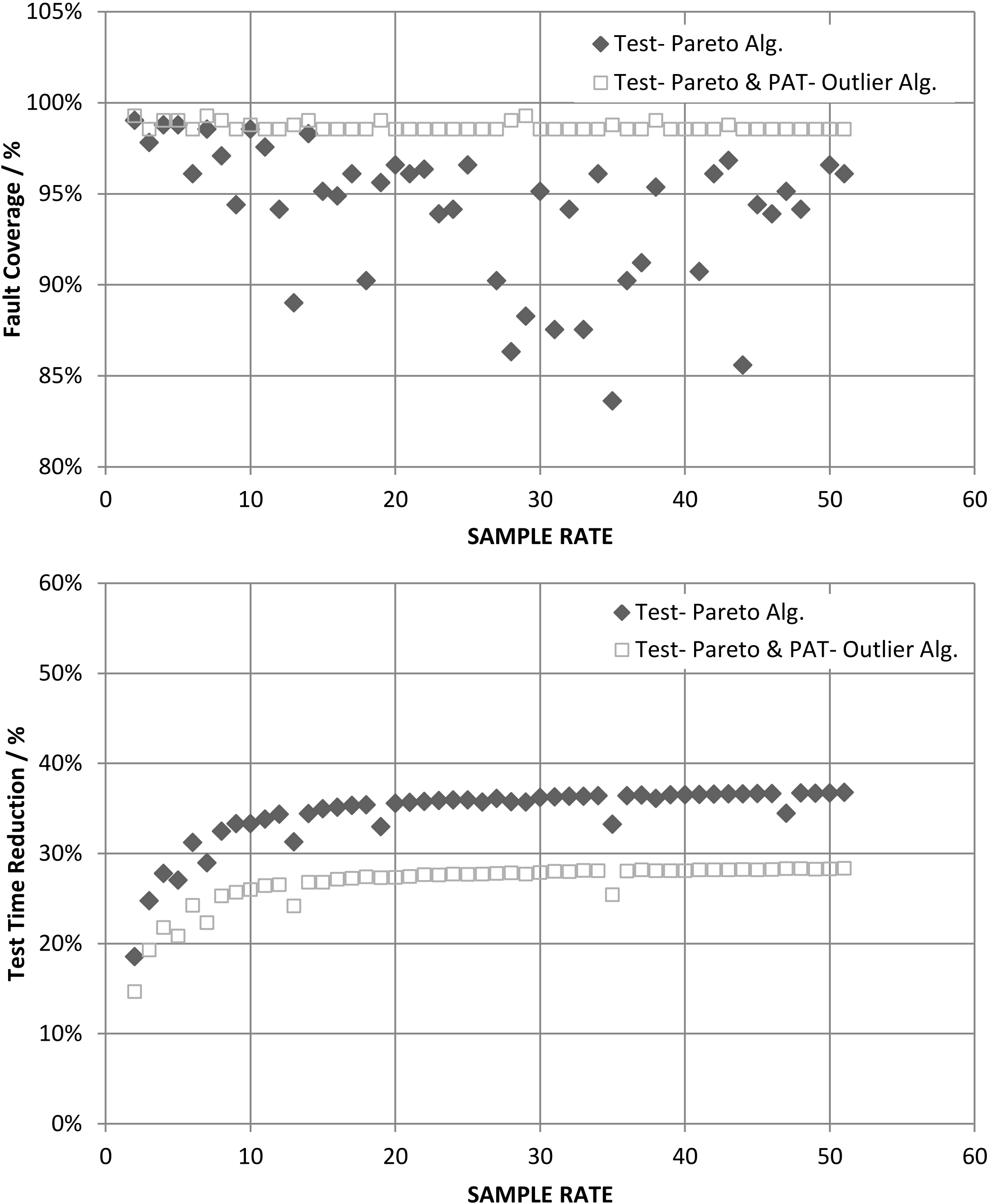


Figure 11: Test Time Reduction and Fault Coverage as a Function of SAMPLE_RATE

Figure 11 shows that the decreasing SAMPLE_RATE converge again to the conventional test. This is the case because the SAMPLE_RATE value 0 would imply that once more a full test has to be executed on every die. For a rising SAMPLE_RATE, less dies are tested, which results in more test escapes and worse fault coverage.

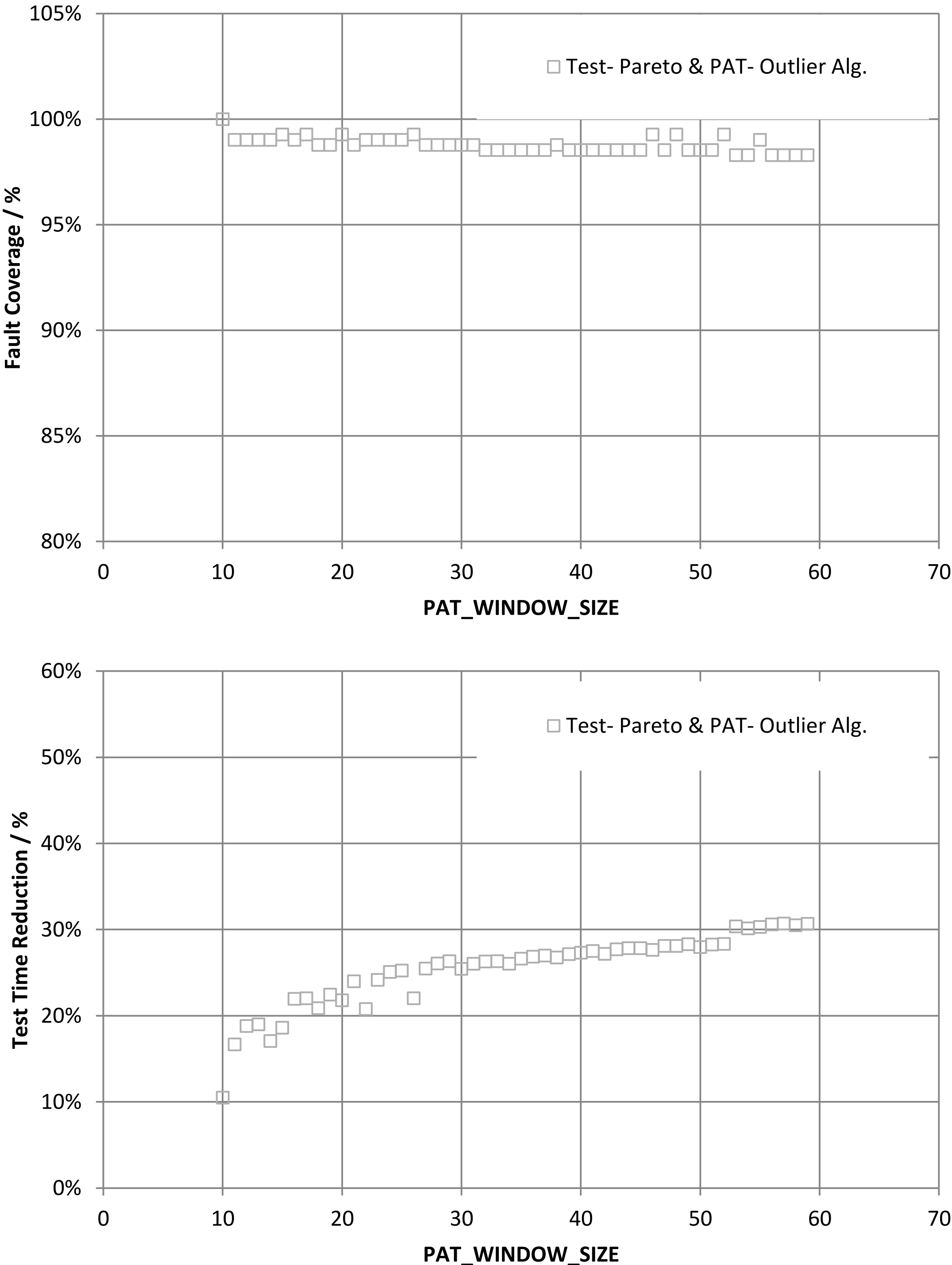


Figure 12: Test Time Reduction and Fault Coverage as a Function PAT_WINDOW_SIZE

Figure 12 illustrates the trend of the PAT_WINDOW_SIZE variable. Since this parameter is not used for the Test-Pareto Algorithm, it is clear that parameter variation has no impact on it and is not displayed. For the other algorithm it can be seen that a decreasing window size shows a similar effect like the SAMPLE_RATE parameter. This is caused by the nature of the outlier calculation. The smaller the window size is, the tighter the PAT outlier limits will be and all the more PAT outlier will occur. These phenomena can also be derived from the calculations represented in the previous chapter, 2.1.3.

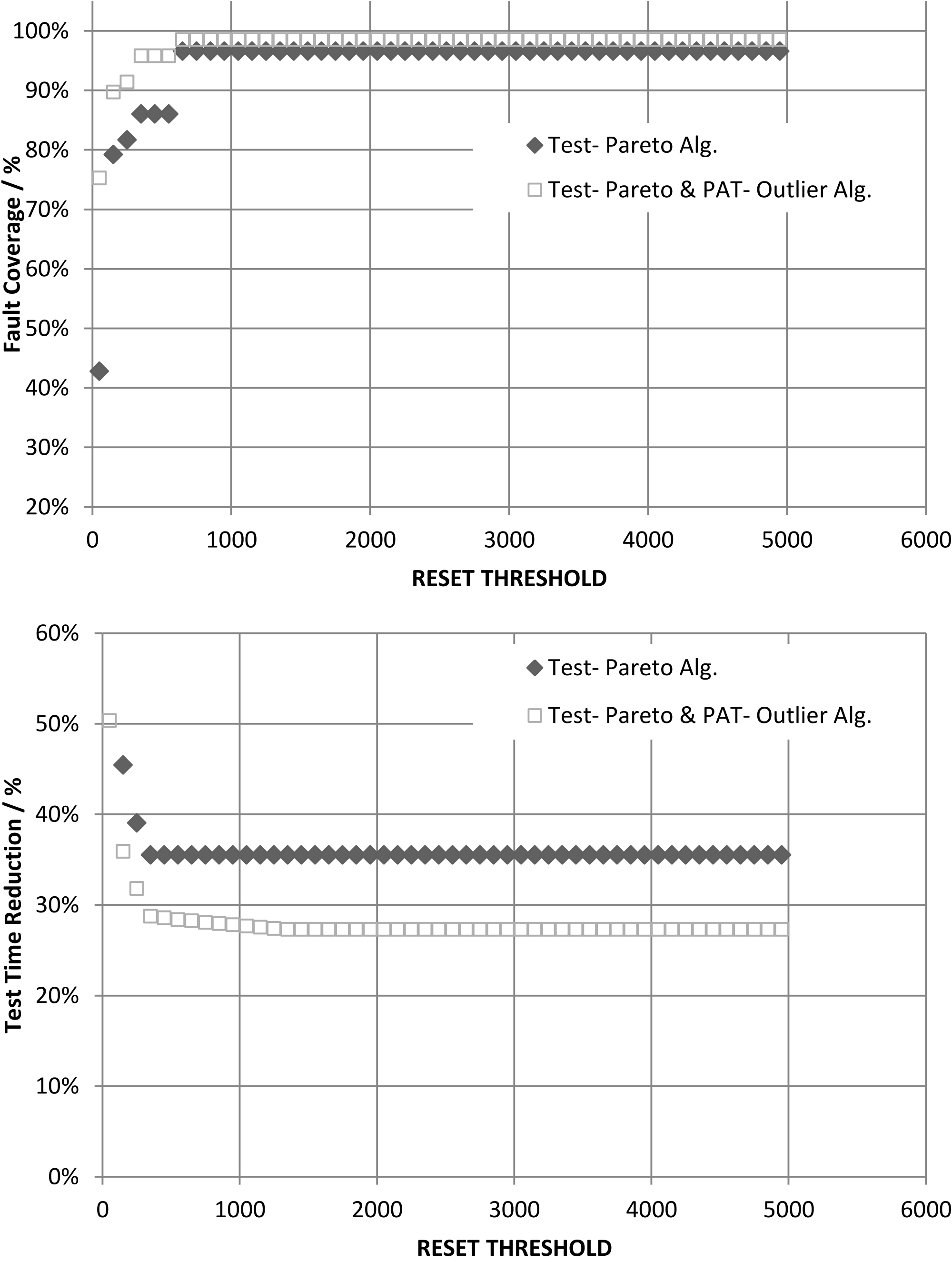


Figure 13: Test Time Reduction and Fault Coverage as a Function RESET_THRESHLD

Figure 13 shows that the decreasing RESET_THRESHOLD can yield higher test time reductions for both algorithms, but in the same way significant fault coverage losses result. Hence it seems to be very risky to allow tests which once had a fail in the past to be skipped again in the upcoming test session.

It is now clear that the choice of parameters results directly in the outcome of the algorithm. Generally, a trade-off between test time reductions and fault coverage has to be made. A general approach on how to derive the "perfect" parameter set cannot be offered. Consequently it is necessary to try several parameters with the algorithms modelled on the diagrams above. Table 6 shows an example parameter set derived from Figure 10 to Figure 13.

Table 6: Derived Parameter Set for AT Algorithm

Algorithm Parameter	Value (a.u.)
CONTROL_SAMPLE_SIZE	5%
SAMPLE_RATE	25
RESET_THRESHOLD	5000
PAT_WINDOW_SIZE	55

Estimation of the Lot Fraction Defective for Adaptive Test Algorithm

In the following chapter an approach for calculating and estimating the lot fraction defective of adaptive testing is introduced. Lot fraction defective is a statistical term and refers to the portion of faulty ICs among all the others. Adaptive testing also represents a type of a statistical sampling procedure. This is the case because with most AT algorithms whose purpose is to save test time, this is always done by simply omitting tests. If a wafer is not tested with all the tests on every die, it is clear that there can be no 100% assurance that all the imperfect parts are detected. But one thing that can be done is to estimate the fraction of defects that may occur in the untested units of the wafer, based on information from the previously tested units. The accuracy of this estimation can be refined by specifying its uncertainty using a proper statistical confidence interval. These on inferential statistics based calculations are then used to specify and derive the lot fraction defective caused by the adaptive test algorithms. In Figure 14, on the left side, a pass/fail wafer map of a conventional full test is shown in which one square represents one DUT for a conventional test. Each DUT is subjected to a test set with four tests which are always executed in sequence, beginning with test 1 and ending with test 4. The detailed considerations for example single DUT results from this testing are shown on the right in Figure 14. In situation A, the die has succeeded in all the tests and is marked as a pass. The next situation, Situation B, shows a die, which has failed the second test after previously passing the first test beforehand. After failing this test 2, the IC is not tested further, and test 3 as well as test 4 will be never executed because of the stop on fail (SOF) method of conventional production testing. The last example, C, again shows a faulty die which has already failed the first test. Testing is stopped after this point. This means that each IC is subjected to the full test set, and once only one test fails in the row is the whole die marked as fail (red colour). Only if an IC passes the entire test set, it can be marked as faultless, which is then displayed in green. To put it more generally, it can be said that an IC consists of a number of subunits which can take three information conditions. These three conditions are pass, fail and untested, whereas an IC only works if all the subunits are free of errors.

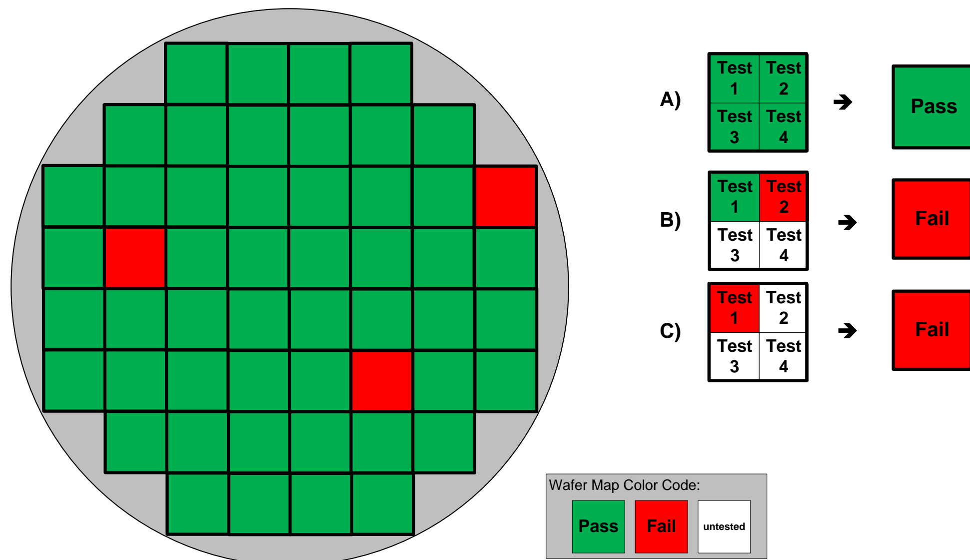


Figure 14: Wafermap with Pass and Fail Information Content based on Stop on Fail (SOF) Strategy of Conventional Test

In contrast, in Figure 15 on the left side of the drawing the same wafer is shown. This time the wafer was tested with an adaptive algorithm. The same dies as in the other wafer map are now divided into four subunits, whereby each subunit refers to a test. Because of the adaptive test algorithm it is now the case that not every die will be tested with all the tests available, so that some subunits of the chip will be left untested. For these kinds of subunits, no pass/ fail information as in the conventional SOF method is available and they are displayed as white squares in the example wafer map. The final decision as to whether a device is faulty or faultless is the same; once a subunit fails the overall die is declared to be faulty. The difference to the conventional test is that untested subunits can also occur between other tests and are not always lined up at the end of the testing sequence as in SOF testing. So it is also possible that an IC is considered as error-free if not every subunit was tested – situation A. C differs from B because test 2 was left out in-between, which is also quite possible. However, both are considered to be faulty because test 3 failed each time. Here it is again clear that untested units may result in undetected faults. Now the basic idea is to use the information about the tested subunits, which includes the corresponding test result, and, based on that, estimate the appearance of defects in the fraction of untested subunits. Afterwards the estimated portion of faulty subunits is used to derive an estimate for the lot fraction defective of ICs resulting due to adaptive testing.

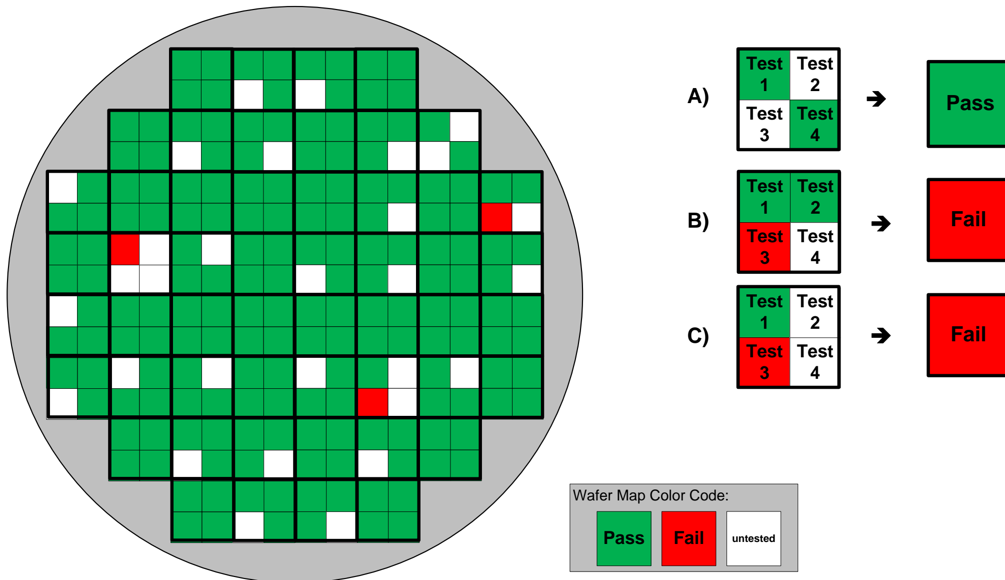


Figure 15: Wafer map with Pass and Fail Information Content based on Stop on Fail (SOF) Strategy of Adaptive Test

The first assumption for this failure estimation model is that every subunit is statistically independent, which means that the outcome of each subunit does not depend in any way on the outcome of another subunit. Every subunit has the same possibility either to be faulty or not. Therefore the tests are also assumed to be independent of each other, and in the example of Figure 15 one die exists of four subunits.

Moreover, the fault distribution is assumed to follow a binomial model. A binomial distribution is a probability model for sampling from an infinitely large population, where p represents the fraction of defective or nonconforming items in the population. In this context, x represents the number of nonconforming items found in a random sample of n items of the population. The binomial distribution function is defined as follows in equation (8):

$$\mathrm{B}_{n,p}(\mathrm{x}) = \sum_{k=0}^{x} \binom{n}{k} p^k (1-p)^{n-k} \qquad (8)$$

After an adaptive test session has been completed, how often each single test was executed by the algorithm can be exactly traced back. Figure 16 represents, for example, a product with 20 tests for each IC and 3200 dies on the wafer. So after the algorithm has finished for each test, the information about its sample size $\mathrm{n_i}$ is available. Furthermore, the exact information how often each test failed during the simulation is also available, the fail pareto list. The number of faults which occurred per test is x_i. Based on this, it is now possible to

estimate the lot fraction defective per test with the so-called point estimator $\hat{p}_i$ for the binomial distribution. See equation (9).

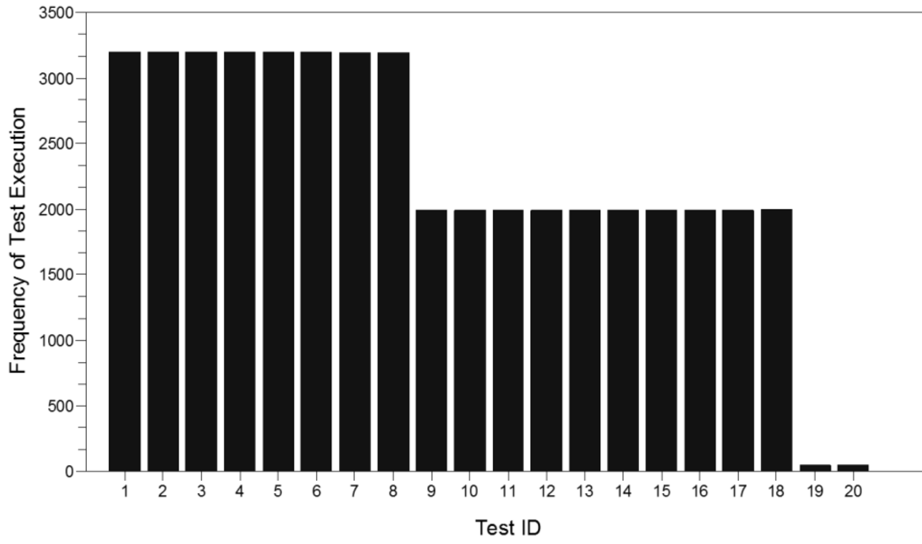


Figure 16: Execution Statistic of all Tests which is Available after AT is Finished

$$\widehat{p}_i = \frac{x_i}{n_i} \quad (9)$$

The assumption is that one test is a binomial model with the parameter $\mathrm{n_i}, \mathrm{p_i}$

$$\mathrm{T_i} \sim \mathrm{B}(\mathrm{n_i}, \mathrm{p_i}) \quad (10)$$

When the number of tests is t, the model of the whole chip test T can be written as (11):

$$\mathrm{T} = \sum_{i=1}^{t} \mathrm{T_i} \quad (11)$$

Because of the initially assumed independency of the tests, the individual defect portions $\mathrm{p_i}$ have to originate from a population with the same lot fraction defective. So every test sample with its size $\mathrm{n_i}$ and faults $\mathrm{x_i}$ must therefore originate from the population of the subunits with the same lot fraction defective p_{sub} – which is the unknown. This leads directly to the next equation (12)

$$\mathrm{T} = \mathrm{B}(\sum_{i=1}^{k} n_i \ , \mathrm{p_{sub}}) \quad (12)$$

The point estimator for the fraction defective in the subunits can now be calculated according to formula (13):

$$\widehat{\mathrm{p}}_{\mathrm{sub}} = \frac{\sum_{i=1}^{t} x_i}{\sum_{i=1}^{t} n_i} \tag{13}$$

The next goal is to estimate the IC fraction defective based on this subunit level estimate $\widehat{\mathrm{p}}_{\mathrm{sub}}$. Like in the SOF method, for the estimation it is also assumed that simply one defect leads to an overall faulty die. When taking in account, that one die exists of t subunits, the point estimator for the lot fraction defective for ICs can be calculated according to equation (14):

$$\hat{p}_{lot} = \frac{\sum_{i=1}^{t} x_i}{\sum_{i=1}^{t} n_i} \cdot t \tag{14}$$

The expected value $E(X)$ for faulty dies out of a sample n of dies would refer to (15):

$$E(X) = n \cdot \widehat{p}_{lot} \tag{15}$$

To derive a worst case scenario for the lot fraction defective which can occur in the untested subunits the confidence interval is used to indicate the reliability of the estimate. A confidence interval specifies a range within the parameter is estimated to lie. The (1-α) confidence interval for an unknown lot fraction defective p is an interval which includes with a (1-α) probability the unknown lot fraction defective p.

The confidence interval is given by Equations (16) to (18):

$$p_l \leq \widehat{p}_{sub} \leq p_u \tag{16}$$

$$P\{x \leq E(X_{sub})\} := \sum_{x_{sub}=0}^{E(X_{sub})} \binom{n_{sub}}{x_{sub}} \cdot p_u^{\ x_{sub}} \cdot (1-p_u)^{n_{sub}-x_{sub}} = \frac{\alpha}{2} \tag{17}$$

$$P\{x \leq E(X_{sub}) - 1\} := \sum_{x_{sub}=0}^{E(X_{sub})-1} \binom{n_{sub}}{x_{sub}} \cdot p_l^{\ x_{sub}} \cdot (1-p_l)^{n_{sub}-x_{sub}} = \left(1 - \frac{\alpha}{2}\right) \tag{18}$$

with $x_{sub} = \sum_{i=1}^{t} x_i$ and $n_{sub} = \sum_{i=1}^{t} n_i$

So the lot fraction defective for the subunits lies in between the boundaries $p_l \leq \hat{p} \leq p_u$ with a probability of (1-α) percent. In the worst case situation the lot fraction defective is expected to be p_u. If a wafer has N dies on it, the number of untested subunits u_i is also known(19):

$$u_i = N - \mathrm{n_i} \tag{19}$$

and the number of defects in the untested can be estimated as $\hat{x}_{wc,usub}$ (20):

$$\hat{x}_{wc,usub} = p_u \cdot \sum_{i=1}^{t} u_i \tag{20}$$

When assuming that every defective subunit results in a faulty die and it is not considered that more than one defective subunit could take place within one IC, the worst case error contribution of dies can be written as in equation(21), which represents the worst case number of estimated test escapes due to adaptive testing.

$$\hat{x}_{wc} = \hat{x}_{wc,usub} = p_u \cdot \sum_{i=1}^{t} u_i \tag{21}$$

The point estimator for test escapes can be written as shown in formula (22):

$$\hat{x} = \hat{p}_{lot} \cdot \sum_{i=1}^{t} u_i \tag{22}$$

Additionally, the worst case lot fraction can also be calculated, as in formula (23)

$$\hat{p}_{wc,lot} = \frac{\hat{x}_{wc}}{N} \tag{23}$$

All the calculations above have been used for the product analysis presented in 0.

Adaptive test product analysis and investigations based on experimental test data for product E

For the subsequent adaptive test simulations and experiments, the standard wafer of the product E was used. The experiments took place on wafer level due to wafer sort. Standard wafer denotes a reference wafer that was fabricated using the typical process flow of the product. This means that a standard wafer represents the “golden” standard also in terms of testing behaviour for the entire products of the same kind. Normally this wafer is only used in exceptional cases as measuring reference or for product verification and is not shipped to any costumer. In Table 7, the manufacturing data for the product E are summarized.

Table 7: Overview and Information of Product E

Product Name:	***E***
Number of Tests per Die:	107
Number of Dies per Wafer:	4694
Number of Test Sites:	2
ATE:	LTX, Fusion EX
Sort Type:	Full Sort
Lot ID:	B44771-1
Wafer Name:	B44771W16PA7 (Standard Wafer)

The sequence of tests, simulations and analyses has been as follows:

- At the beginning of the experiments, the standard wafer was tested in a conventional way on the LTX Fusion EX (LTX-Credence Corporation, Norwood USA) ATE. A full sort was done, which means that 100% of all dies on the wafer have been tested with the full test list.
- Afterwards this data have been used to derive a parameter set for the simulation. The results are exactly those values which have already been presented in the prior chapter 0 in Table 6.
- The test times, test groups, group rules and tests for PAT outlier monitoring have been defined together with the proper test and product engineers.
- As a next step, an adaptive test simulation with both algorithms and the derived parameter set took place.

- Subsequently, a manual retest only of the dies with test escapes was carried out, with the aim to verify the results of the conventional test. On the one hand the simulation (see 0) achieved the desired test time reduction with about 35% compared to the conventional test. Unfortunately, on the other hand, the algorithm resulted in a significant number of undesired test escapes, which was the main driver for the manual retest.
- Since the results (see 0) of the retest have shown that only 2 dies out of the 14 test escapes from the first full sort have again failed the exactly same test program, an entire second full sort of the wafer has been applied. A first assumption was that contact issues of the ATE might have been the reason for this unequal outcomes. To prevent contact issues, the contact force of the wafer prober, which is necessary to provide trustworthy contact to the DUT, was increased. Again the conventional test was carried out and afterwards the simulation with the same parameter set and extended STATS file as before took place.
- Because of still existing result inconsistencies between the two full sorts, a "Pass- Fail Flip Report" was done. With the help of a pass fail flip report it is possible to compare two test sessions and make a statement about the repeatability of the test. Therefore the assignment of parts is done with the X and Y position of the dies, and for a result comparison the so called pass-fail flip map is generated. The detailed results are displayed in Figure 18 in the discussion part of this thesis. Additionally, histograms of tests with the most occurring result flips are plotted (Figure 19 and Figure 20).
- Finally the continuity tests have been additionally added to the PAT test column of the STATS LIMITS file. Two simulations with the Test Pareto and PAT Outlier Algorithm have been initiated afterwards based on both full sort data.

The results of all these experiments are presented in detail in chapter 0.

Offline Adaptive Test Simulations of high-volume Products

Table 8 shares all information about the analysed products selected from high-volume production. For all of these five products, a lot composed of 25 wafers was selected randomly out of the companies' test archive data base.

For the first two products, A and B, the customer accepts a certain defect level of the purchased ICs which is fixed per contract. The acceptance sampling procedure has already been described in section 0 and is based on the MIL-STD-105 as well as the ISO 2859 standard. As a consequence, the ams AG applies only a 10% sample sort instead of a 100% inspection and accepts or rejects the drawn sample depending on the number of faulty dies in the sample – the acceptance number. For instance the acceptance number for the product A is 8 faulty dies out of a sample of 3200 which results in a lot fraction defective of 0.25% (= 8/3200). Once the level of detected faults in the sample exceeds this value, a full sort of the entire wafer is done. For the product B also the same threshold of 0.25% lot fraction defective is given. Because the real percentage of nonconforming units is unknown for adaptive testing, the lot fraction defective estimation method (cp. 2.5) was applied, with the aim to estimate the unknown value produced by AT simulations. The corresponding results for each product can also be found in 3.2. The estimated value can afterwards also be used for deciding whether 100% testing is necessary or not. Because only AT simulations were applied during this thesis, it is also possible to compare the results with the real lot fraction defective of the conventional test.

Table 8: Overview of analyzed high-volume Products

Product Name:	***A***	***B***	***C***	***D***	***E***
Number of Tests per Die:	20	45	662	45	107
Number of Dies per Wafer:	32000	22000	2000	25662	4694
Number of Test Sites:	8	8	1	8	2
Lot ID:	C25972-1	C23401-1	C24133-1	C25208-1	C25357-1
Number of Wafer:	25	25	25	25	25

Out of the wafer lot of each product, a wafer was randomly drawn and the so selected wafer was then used to derive the algorithm's parameter sets. This was done in the same way as

described in 0 and with the focus on test time reduction rather than on fault coverage. The resulting values are represented in Table 9.

Table 9: Parameter Sets for AT Algorithm derived from exhaustive-search method of a randomly selected wafer

Product Name:		***A***	***B***	***C***	***D***	***E***
CONTROL_SAMPLE_SIZE	in %	20	15	20	10	20
SAMPLE_RATE	in #Dies	20	14	4	30	10
RESET_THRESHOLD	in #Dies	3280	2176	1076	25662	4694
PAT_WINDOW_SIZE	in #Dies	30	28	10	40	20

The next step in the workflow were adaptive test simulations, separate for each product. The software is designed in a way that it can handle the simulation of an entire wafer lot. Thus for analysing a whole lot, the simulation has to be started only once. Again the outcomes of the algorithm in form of statistics about test time reduction as well as fault coverage are reported. For that, the Test- Pareto Algorithm and the Test- Pareto and PAT-Outlier Algorithm have been executed. Moreover an additional simulation run with a different set of PAT tests was done. All continuity tests which anyway had to be tested on the DUT due to the group rules have been selected as PAT tests. Therefore the corresponding STATS Limits file has been adapted. The corresponding results are represented in 0.

3 Results

Adaptive test product analysis and investigations based on experimental test data for product E

Table 11 summarizes the most important results of the experiments with real production tests as well as simulated adaptive tests. As already described in the methodology chapter, for the simulations the results of the two different algorithms are documented. Moreover a simulation with a modified extended STATS LIMITS file is shown, which means that in addition to the PAT tests proposed by the test engineer, continuity tests have been added to the PAT outlier algorithm. Although the continuity tests are parametric one, they are not typical for the purpose of part average testing. This is the case, because in general they are applied to verify that the contacting process between the tester and the DUT have been done successfully. However, in the further consequence it has pointed out, that outlier monitoring of these kind of tests results into a significant decreased number of test escapes (see Table 11). Additionally in Table 11, the first as well as the second full sort of the same standard wafer are compared.

Table 10: Result summary of the 1st and 2nd Full Sort of the Standard Wafer from Product E

	Data of Conventional Test		*AT with Test-Pareto Algorithm*		*AT with Test-Pareto and PAT Outlier Algorithm*		*AT with Test-Pareto and PAT Outlier Algorithm with additional Continuity Tests as PAT Outlier Monitor Tests*	
	# Fail Dies	***Yield %***	***Number of Test Escapes***	***Test Time Reduction %***	***Number of Test Escapes***	***Test Time Reduction %***	***Number of Test Escapes***	***Test Time Reduction%***
1st Full Sort	409	91.31	14	36%	12	34%	4	31%
2nd Full Sort	407	91.29	3	36%	3	35%	2	29%

Table 11 compares the test results of the first full sort with the results from the manual retest. Exactly the same coordinates as the DUTs which showed test escapes in the AT with Pareto Algorithm simulation have been manually reselected by its coordinates. The background colour of passing test results is green and red is used for the failing ones.

Table 11: Product E: Result of Test Escapes and corresponding Retest of faulty dies in 1st Full Sort for AT with Pareto Algorithm [green ... test passed, red … test failed, a.u. … arbitrary unit]

index	Test ID	Test Name	Result of 1st Full Sort (a.u.)	Manual Retest (a.u.)	Lower Limit (a.u.)	Upper Limit (a.u.)	X Position	Y Position
1	57	VDD_ALL_DELTA_VREF_VREFS/RIH_DIGHR	46.70	42.1757	25.001	44.999	-58	-19
2	46	VDD_MIN_VREF/RIH_DIGHR	1104.49	1105.11	1127.97	1279.53	-86	-11
3	49	VDD_MAX_VREF/RIH_DIGHR	1156.64	1158.97	1171	1261	-89	-2
4	56	VDD_ALL_DELTA_VREFS/RIH_DIGHR	-2.90	0.0159	-0.8	3.452	1	-2
5	55	VDD_ALL_DELTA_VREF/RIH_DIGHR	0.80023	0.0460	-0.463	0.73	-24	-3
6	55	VDD_ALL_DELTA_VREF/RIH_DIGHR	0.74358	-0.0734	-0.463	0.73	-34	1
7	55	VDD_ALL_DELTA_VREF/RIH_DIGHR	-0.5471	-0.1996	-0.463	0.73	-46	1
8	55	VDD_ALL_DELTA_VREF/RIH_DIGHR	1.0221	0.0192	-0.463	0.73	-14	4
9	55	VDD_ALL_DELTA_VREF/RIH_DIGHR	-0.6438	-0.1966	-0.463	0.73	-40	5
10	55	VDD_ALL_DELTA_VREF/RIH_DIGHR	-0.6122	-0.0546	-0.463	0.73	-82	6
11	55	VDD_ALL_DELTA_VREF/RIH_DIGHR	-0.471	-0.1188	-0.463	0.73	-52	6
12	55	VDD_ALL_DELTA_VREF/RIH_DIGHR	0.85272	-0.0622	-0.463	0.73	-46	6
13	55	VDD_ALL_DELTA_VREF/RIH_DIGHR	0.76925	-0.0213	-0.463	0.73	-40	6
14	55	VDD_ALL_DELTA_VREF/RIH_DIGHR	0.73768	0.2147	-0.463	0.73	-24	9

Table 12 represents the same, but here the Pareto Algorithm and PAT Outlier Algorithm and additional continuity tests have been declared as PAT tests.

Table 12: Product E: Result of Test Escapes and corresponding Retest of faulty dies in 1st Full Sort for AT with Pareto Algorithm and PAT Outlier Alg. incl. Continuity Tests as PAT tests [green ... test passed, red … test failed, a.u. … arbitrary unit]

index	Test ID	Test Name	Result of 1st Full Sort (a.u.)	Manual Retest (a.u.)	Lower Limit (a.u.)	Upper Limit (a.u.)	X Position	Y Position
1	57	VDD_ALL_DELTA_VREF_VREFS/RIH_DIGHR	46.70	42.1757	25.001	44.999	-58	-19
2	46	VDD_MIN_VREF/RIH_DIGHR	1104.49	1105.17	1127.97	1279.53	-86	-11
3	49	VDD_MAX_VREF/RIH_DIGHR	1156.64	1158.977	1171	1261	-89	-2
4	56	VDD_ALL_DELTA_VREFS/RIH_DIGHR	-2.904	0.015893	-0.8	3.452	1	-2

Table 14 finally shows again the detailed tests of the Test Pareto and PAT Outlier Algorithm which resulted in test escapes of the second full sort. On the other hand, these results are compared with the retest results of the manually selected DUTs. It can be seen, that only one failing test remains after the manual retest in Table 14. This phenomena will be discussed in detail in the discussion section 0.

Table 13: Product E: : Result of Test Escapes an of corresponding Retest of faulty dies in 2nd Full Sort for AT with Pareto Algorithm and PAT Outlier Alg. incl. Continuity Tests as PAT tests [green … test passed, red … test failed, a.u. … arbitrary unit]

index	Test ID	Test Name	Result of 2nd Full Sort (a.u.)	Manual Retest (a.u.)	Lower Limit (a.u.)	Upper Limit (a.u.)	X Position	Y Position
1	46	VDD_MIN_VREF/RIH_DIGHR	1105.10	(no Result) Fail Flip[7]	1127.97	1279.537	-86	-11
2	55	VDD_ALL_DELTA_VREF/RIH_DIGHR	-0.487603	-0.173434	-0.463	0.73	-44	27

[7] Fail Flip: The part failed in both measurements at different tests.

Test Time Reduction and Test Escape Results of Offline Adaptive Test Simulations of high-volume Products

In this section, the results of the five high volume product analyses are presented. Mainly the test time reduction, fault coverage and test escape estimation results are offered. In Table 14, only the statistical summaries of the simulation with additional continuity tests as PAT outlier tests are documented. All results out of Table 14 are average values per wafer derived from the entire lot of twenty-five wafers. For all products, the detailed results for each single wafer out of the lot are documented in the appendix chapter of this thesis (7.1 - 7.5). Moreover the results in the appendix include both algorithms with the parameter sets which have been defined with the proper test and product engineer hence without continuity tests as PAT tests.

Table 14: Conventional Test Yield, Test Escapes, Fault Coverage and Test Time Reduction of AT with Pareto and PAT Outlier Algorithm with additional Continuity Tests as PAT Outlier Monitor Tests for all five Products

Product Name:	**A**	**B**	**C**	**D**	**E**
Yield of conventional Test *%*	99.93%	99.78%	81.57%	99.70%	92.97%
Number of Test Escapes *# parts*	0.12	0.44	1.48	1.00	3.52
Number of Test Escapes *ppm*	37.67	201.40	798.00	38.97	749.89
Fault Coverage *%*	97.70%	86.82%	99.64%	98.88%	99.07%
Test Time Reduction *%*	50.10%	51.02%	6.28%	14.49%	17.46%

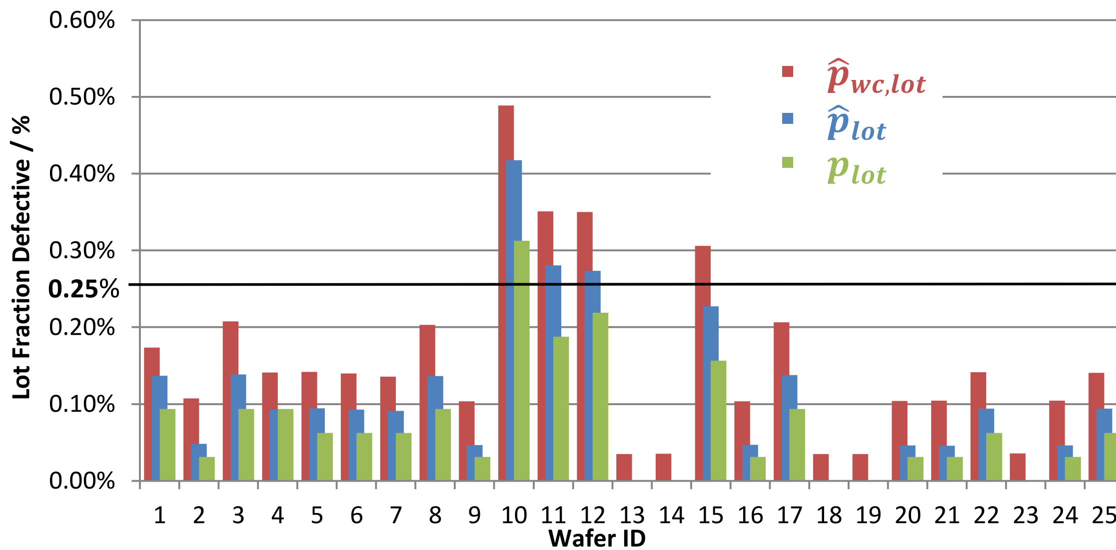


Figure 17: Product A: Validation of the Lot Fraction Defective Estimation for AT with Pareto and PAT Outlier Algorithm and additional Continuity Tests as PAT Outlier Monitor Tests

In Figure 17, the lot fraction defective estimation results for the product A, separate for each wafer, are plotted. The underlying simulation is the Test Pareto and PAT Outlier algorithm with additional continuity tests as PAT outlier monitor tests. In the bar chart, the real fraction defective p_{lot} derived from the conventional test is compared with the point estimation $\hat{p}_{lot}$ as well as the worst case estimation $\hat{p}_{wc,lot}$ from the simulation. The horizontal black line at the lot fraction defective value of 0.25% presents the threshold for lot acceptance. Due to the sampling plan, only values below this threshold are acceptable and once the value is higher, a full sort of the wafer is the consequence. Concerning lot fraction defective estimation of all other products, only the statistical summary of the results are presented in Table 15. Again only the results with additional continuity tests as PAT outlier monitor tests are shown as average value per wafer out of the wafer lot. All other algorithm and parameter set results can be found in the appendix (7.1-7.5). As already mentioned in the methods section, only for the products A and B so far an AQL value and due to this a threshold for the lot acceptance is defined. For the other products no thresholds, which are defined per contract with a customer are available, but applying the lot fraction defective estimation is also a valuable tool for estimating the test escapes produced by AT for them.

Table 15: Statistical Summary of Lot Fraction Defective Estimation as well as Validation of the Results by comparing Test Data from Conventional Test for AT with Pareto and PAT Outlier Algorithm and additional Continuity Tests as PAT Outlier Monitor Tests

Product Name:	A	B	C	D	E
p_{lot}	0.07%	0.21%	17.17%	0.30%	7.03%
$\hat{p}_{lot}$	0.10%	0.31%	20.65%	0.36%	7.97%
$\hat{p}_{wc,lot}$	0.16%	0.44%	20.77%	0.37%	8.06%
threshold for lot acceptance	0.25%	0.25%	-	-	-

4 Discussion

Adaptive test product analysis and investigations based on experimental test data for product E

At first glance the results of the data experiments for the product E seem to be very inconsistent and inapprehensible (compare Table 10). Because the simulation with the two different algorithm of the first full sort yielded significant numbers of test escapes, a retest only of the test escapes has been carried out. The results in Table 11 shows that out of the 14 dies from the first full sort with the Test-Pareto Algorithm, only 2 parts remained faulty after the manual resort. An assumption for that effect was that the first wafer sort had electrical contact issues. During wafer sort, the wafer prober provides the force needed to make electrical contact with the DUT and take up the compliance. The contact force is considered as one of the critical parameters to stabilize the electrical connection and insure low contact resistance [8]. To check this hypothesis of contact issues, a second full sort of the same wafer has been initiated but now with a higher contact force value (also known as “over travel"). It was expected that the overall number of faulty dies was going to be reduced after the second full sort, because the manual resort already figured out that many faulty dies seem to be good after retest. But surprisingly it has been shown that the second full sort delivers roughly the same number of faulty dies (Table 10: 1st full sort: 409, 2nd full sort: 407), so no yield improvement could be achieved with the increased contact force. Moreover after the second full test, a significant number of DUTs have changed their pass or fail result. Initially faulty devices changed their behaviour and passed the second test and vice versa. So some faults occurred at completely different coordinates on the wafer.

A pass fail flip report was generated to compare the two full sorts. An excerpt of this report is displayed on the next page in Figure 18 and delivers a first explanation for these inconsistent results. In that map, the flip types of the parts are plotted in a wafer map. The following types are defined:

- PASS → PASS: The part was “good” in both measurements (light grey)
- FAIL → FAIL: The part failed at the same test in both measurements (dark grey)
- PASS → FAIL: The part was “good” in the first measurement but failed in the second measurement (red)
- FAIL → PASS: The part failed in the first measurement but was “good” in the second measurement (orange)
- FAIL FLIP: The part failed in both measurements at different tests (blue).
- No Value: One of the measurements/parts is not available (white) [28]

The report shows that 264 devices have changed their result, either from an initially passing DUT to faulty device in the second full sort (PASS->FAIL flip) or the other way around from a firstly failing device to a passing one afterwards (FAIL→PASS flip). Elsewhere the report delivers also those tests with the greatest number of counts in any kind of flips.

Assuming this wafer would be shipped to the customer and only the first full sort would have taken place, it is clear that the majority of critical flips are PASS->FAIL ones. Depending on which result is now the right one, either first or second, the customer is going to get a potentially nonconforming part. The tests with the greatest number of this kind of flips are shown in Table 16. The corresponding histograms are displayed in Figure 19 and Figure 20.

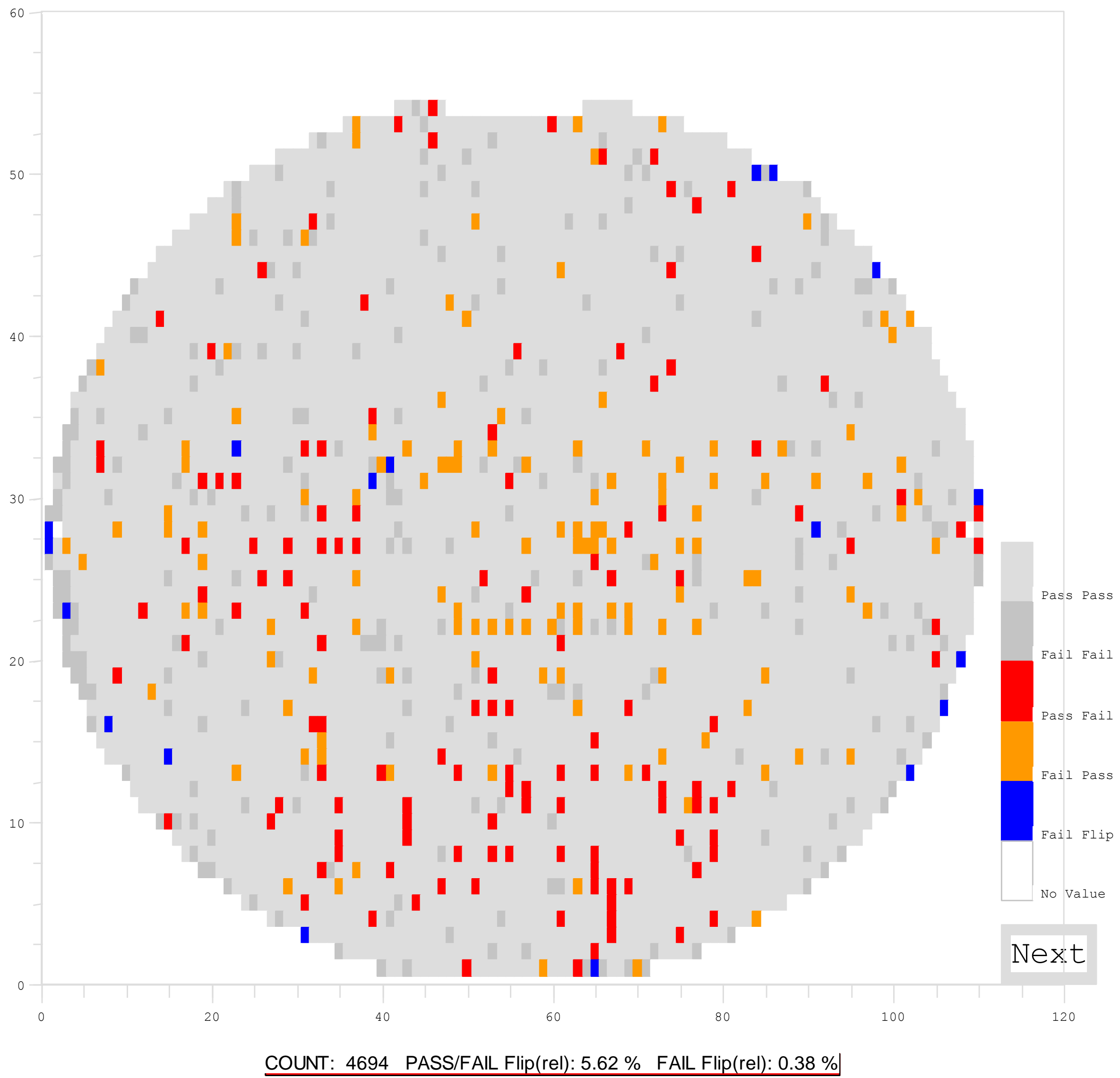


Figure 18: Pass Fail Flip Wafer Map

Table 16: Tests with the greatest number of Pass Fail Flips based on PASS/FAIL Flip Report of 1st and 2nd Full Sort

Test Name	Unit	# Pass Fail Flips
57 VDD_ALL_DELTA_VREF_VREFS/RIH_D	mV	75
106 ADC_FFT_SNRV/MISO_DP	dB	27

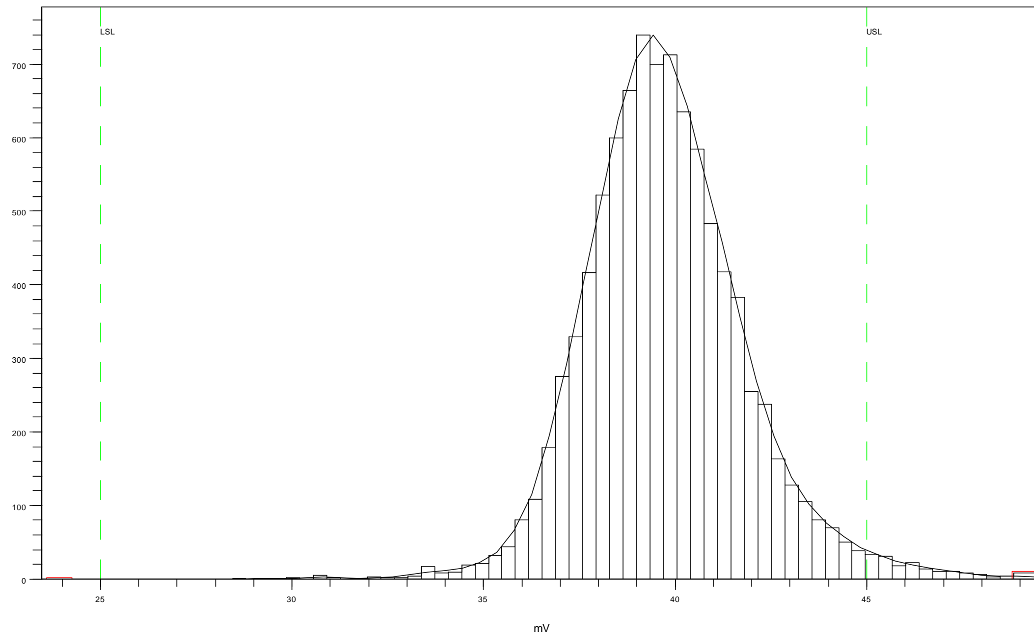


Figure 19: Histogram of Test 57: (VDD_ALL_DELTA_VREF_VREFS/RIH_D) based on data from both Full Sorts

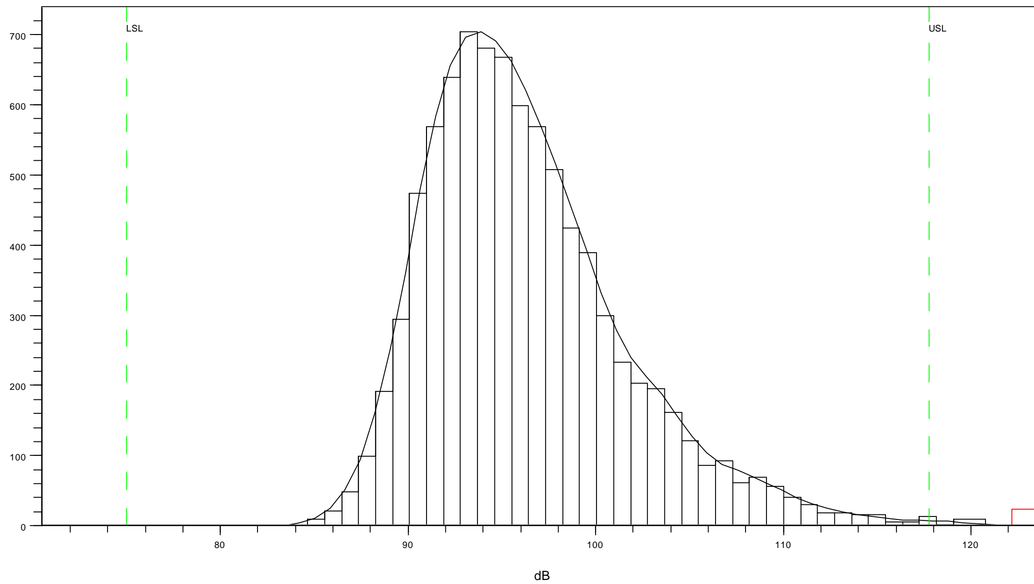


Figure 20: Histogram of Test 106: (ADC_FFT_SNRV/MISO_DP) based on data from both Full Sorts

And now, when looking at the corresponding test histograms of Table 16, the reason for the suspicious results as well as undesirable high flip rates is getting clearer. Both tests in Figure 19 and Figure 20 show potential parametric issues. This is the case because both distributions show tails which exceed the upper specification limits (USL). This variance of the parameter can thus produce test escapes as well as yield losses[8]. Theoretical causes for such issues can be for instance that the test specification has a problem and the limits are not suitable for these two parametric tests. Another reason could be that the test had a problem and leads to the huge measurement variance or uncertainty in the parameter distribution. Because of the implemented SPC (Statistical process control) methods in the company the shown parameter behaviours are not unwanted or even out of control. Rather because of a customer related requirement, the limit has to be as tight as they are. The undesirable yield loss would only be avoidable due to a slimmer parameter distribution with a decreased variance compared to the distribution now. The variance of the parameter distribution, which is based on the chip design, manufacturing process, as well as the uncertainty of the measurement, are the main contributor to the resulting variance it the histograms. When assuming that the measurement accuracy[9] of the ATE between the two wafer sorts didn't change, the repeatability[10] of the measurement can be seen as the main reason for the huge amount of pass/fail flips. This also implies that failing test results close outside the specified limits, are probably only based on the variance of measurement and are not the results of a potentially faulty DUT. If a parameter after repeated retesting passes only once, the parameter of the DUT can most likely be considered as passing the test. On the other hand, the repeated failing results are then based only on the measurement uncertainty. In the subsequent discussion it will be pointed out, that after all retests for this specific product analysis, only one potential DUT would have escape the adaptive test simulation. All other test escapes are origin from result flips. Because the source of the result flips is found and the increased contact force didn't improve the probe yield significantly, the hypothesis of contact issues can be mostly rejected.

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[8] Yield loss: occurs when testing results in the misclassification of correct dies as being faulty

[9] Accuracy: The difference between the average of measurements and a standard sample for which the "true" value is known. [2, M.Burns, 2001, site 87]

[10] Repeatability: "The variation of a measurement system obtained by repeating measurements on the same sample back-to-back using the same measurement conditions." [2, M.Burns, 2001, site 87]

A principal statement for the data experiment is that approximately 30% test time reduction is possible, compared to the two conventional wafer tests due to adaptive testing as well as for both full sorts (Table 10). This is a remarkable value since it would yield into significant direct production cost savings. It can also be said that there is no big difference between the two algorithms with or without outlier monitoring. So also if additional PAT tests are added, it will cost only slightly more test time to switch on all tests in case of a PAT outlier which is the functionality of the Test Pareto and PAT Outlier Algorithm. When comparing both test escape results - one with and the other without PAT outlier monitoring for the first full sort - there is also no big gap between the outcomes. The number of test escapes decreases from 14 to 12 dies for the Test Pareto and PAT Outlier Algorithm.

A remarkable improvement, especially of the first full sort simulation, delivers the modified PAT test set with additional continuity tests as PAT outlier tests. It adds a big value to the simulation if continuity tests are also used as PAT tests because the algorithm reduces the number of test escapes and thus increases fault coverage. For the first full sort of the standard wafer, the test escapes decreased from 14 down to only 4 dies (see Table 10).

The retest in Table 12 indicates that out of the remaining 4 test escapes only 2 devices were probably faulty. In the further course of this work it was pointed out that for each analysed product, the additional definition of continuity tests as PAT outlier tests resulted in substantially higher fault detection probabilities and on the other hand corresponded with a reasonably increasing test time. As already mentioned, the guideline for PAT suggests: “PAT limits should be used for all electrical tests if possible, but shall be established for at least 8 important characteristics …” [10]. To use all tests as PAT outlier monitor tests would make no sense for the adaptive test approaches present in this thesis, because test time reduction can only be achieved due to skipping of tests. Once a test is not executed, no measurement value is available. In the consequence it is clear that it would simply be impossible to check if the result is an outlier or not. The selection of continuity tests that anyway have to be executed is therefore a compromise with very satisfying results in fault coverage as well as test time reduction. The continuity tests are typically executed at the beginning of the test program and should never be skipped which was defined due to the group rules together with the test engineer.

Table 10 also shows that already for the simple Test Pareto Algorithm, the data of the second full sort results in a significant lower level of test escapes compared to the first full sort simulation. At the first full sort, the Test Pareto Algorithm resulted into 14 test escapes whereas in the second full sort only 3 escapes remained. The reason for that can be explained with the help of the pass fail flip analysis. The pass fail flip report indicates that for the test with the ID 55, ten FAIL→PASS flips as well as one FAIL FLIP happened. So in total, this test passed eleven times more often in the second full sort than at the first run. Furthermore during the first full sort this test only had ten faults at the conventional test and every fault resulted in a test escape during the simulation.

In Table 11, the exact test list with the tests that lead into test escapes at the first full sort is documented. At the second full sort, this test 55 had only one fail but on a different DUT coordinate than the ten devices before. So because these fails do not occur in the second full sort, they don't result in test escapes. The one remaining test escape of the first full sort comes from another FAIL→PASS flip of the test with ID 57. For the second full sort, the continuity tests have again been added to the list of PAT tests. The result was that one more test escape has been eliminated. Table 13 illustrates these results and furthermore shows that again after a manual retest in the best case, only one test escape would remain for the simulation with continuity tests as PAT tests. When investigating in detail the failing test with ID 46 of this one test escape, the histogram shows that this test is parametrically under control and the escaping test result was a real outlier of the main distribution. The outlier can be seen in red colour at the left bottom corner of the histogram.

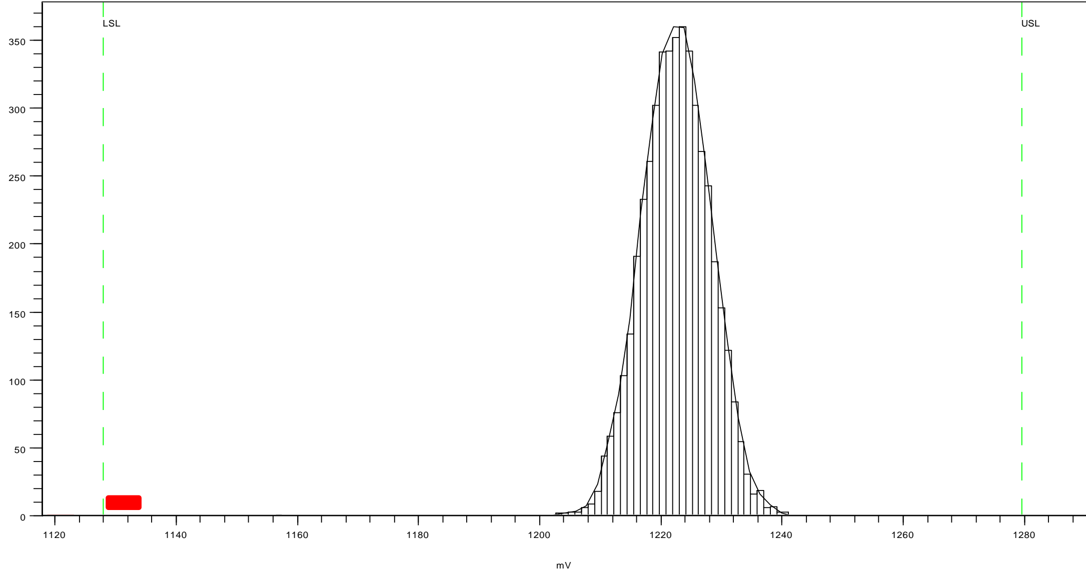

Figure 21: Histogram of Test 46: (ADC_FFT_SNRV/MISO_DP) based on data from both Full Sorts

In summary, after the detailed test escape analysis produced due to AT, it has been shown that only one potential faulty DUT remains. All other test escapes where based on test related issues and their initially nonconforming results has been disproven by retests.

Adaptive offline Test Simulations of high-volume Products

During the analysis of the five products it became apparent that the algorithms with additional outlier monitoring (Test Pareto and PAT Outlier Alg.) consequently lead to a higher fault detection probability. Furthermore the declaration of continuity tests as PAT tests increased once more the fault coverage of the analysed products. In Table 14 it can be seen that except for the product B, the simulations resulted in fault coverage from roughly 97.7 to 99.6% of detected faulty dies out of all nonconforming. For the product B fault coverage of only 87% was reached, but on the other hand a test time reduction of 51% was achieved with the selected parameter set. Another balance or trade-off between test time reduction and fault coverage for this product could be obtained by choosing another parameter set (compare to section 0 In search of the optimal Parameter Set), which is not documented in detail here. Table 14 additionally shows, that for the high fault coverage of about 98%, still approximately 50% test time reduction could be reached for the product A. Test time reductions of around 15% where the results for product D and E, whereupon the fault coverage with circa 99% was very high . Again the balance between fault coverage and test time reduction could be modified by another parameter set. The product C shows the lowest test time reduction and although the fault coverage is with 99.6% very high, this leads into a test escape percentage of about 800ppm. The reason for this is that with only 82%, the product has an initially low yield compared to the others. This is probably also a reason for the low reduction concerning test time, because for a higher failure rate the algorithm increasingly prohibits the omitting of tests.

The purpose of the lot fraction defective estimation is to make statements about the number of potential test escapes which are caused by adaptive testing. Figure 17 shows for the product A that the applied estimation method could be used as a helpful estimation for acceptance sampling. As described in the introduction in point 0, at ams AG the montesort method is used to accept or reject wafers based on their yield with the aim to guarantee AQL values to the customer [25]. Once the fraction defective of conventional testing exceeds a predefined threshold the montesort method switches to a 100% full sort of the wafer. For

the product in Figure 17 this threshold would be a lot fraction defective of 0.25%. It can be seen that the real fraction defective p_{lot} exceeds this threshold only once at wafer 10. The next two wafers of the lot, 11 and 12, also show a remarkably higher lot fraction defective compared to the other wafer. On the other hand, wafers 13, 14, 18 and 19 just have no defects and a yield of 100%. A comparison with the estimated values points out that the estimated values follow the different yields of the wafer very well. The point estimation $\hat{p}_{lot}$ for wafer 11 and 12 results in two additional full sorts compared to the conventional acceptance sampling procedure.

The lot fraction defective estimation in the bar plot as well as in Table 15 also indicates that the point estimation $\hat{p}_{lot}$ of the developed method for each product exceeds the real occurring value p_{lot}. Obviously also the worst case estimation $\hat{p}_{wc,lot}$ based on a 90% confidence interval is always greater than the reality. So it can be said that the lot fraction estimation method consequently overestimates the real fraction of occurring faults. A good fitting estimator would lead to randomly distributed results above as well as below the real values with a very small deviation from reality. The reasons for this overestimating trend can be very manifold. As pointed out in the methodology, there were a lot of assumptions made in order to make the estimation possible. The assumption that each subunit is independent of each other and in further consequence that the tests are statistically independent is probably one of the weakest points of the estimation method. The same point estimator as in the methodology chapter is again shown in equation (24):

$$\hat{p} = \frac{\sum_{i=1}^{t} x_i}{\sum_{i=1}^{t} n_i} \cdot t \qquad (24)$$

In reality it is often the case that tests depend on each other. Thus correlations of tests are common and as a consequence not the whole number of tests is responsible for the real occurring fraction defective. This would lead to a decreased t in equation (24) which further results in a smaller fraction defective estimation. Another reason for the overestimation could be that the tests have a different likelihood to detect a defect, which means they have different test coverage. In the applied method it is assumed that the lot fraction defective of tests is only weighted due to the number of executions as shown by the following proof (25).

$$\hat{p} = \frac{p_1 n_1 + p_2 n_2 + \cdots p_i n_i}{n_1 + n_2 + \cdots n_i} t = \frac{\sum_{i=1}^{t} p_i n_i}{\sum_{i=1}^{t} n_i} t = \frac{\sum_{i=1}^{t} \frac{x_i}{n_i} n_i}{\sum_{i=1}^{t} n_i} t = \frac{\sum_{i=1}^{t} x_i}{\sum_{i=1}^{t} n_i} t \quad (25)$$

It can be seen that the derived weighted average formula is again the same as presented in equation (24). To model the real behavior per test this weighted average calculation also has to be weighted by the test coverage C_i (26):

$$\hat{p} = \frac{\sum_{i=1}^{t} x_i \, C_i}{\sum_{i=1}^{t} n_i} t \quad (26)$$

$$with \sum_{i=1}^{t} C_i = 1$$

To identify the values of the factor C_i separately for each test as well as the correlations of the test can be a very challenging task not only because of the stop-on-fail method of conventional testing. Statistical data analysis, fault modelling and maybe real test coverage experiments on the ATE would be necessary to derive appropriate values.

5 Conclusion

It has been shown that the test costs have become an ever larger share of the production costs and this trend will also continue. Among other things, the increasing test time, which is needed for each integrated circuit, is considered as one of the most critical cost factors. With this thesis, a new test method is presented which falls under the category of "adaptive test" methods. Adaptive test aims to reduce the test time per chip, but affect the quality of the products not, or only as little as possible compared to the conventional test. For that purpose, a simulation software has been developed that performs adaptive test simulations based on real data and test results of the conventional production testing. Product analyzes were performed and both the potential at test time savings, and the resulting loss of quality were determined. The underlying algorithms are based on statistical methods and dynamically decide which tests per chip compared to the conventional test methods can be omitted, or not. Finally, the thesis has shown that by the intelligent omission of tests, compared to conventional testing procedures, test time reduction of up to 50% can be achieved with the simulation. In contrast, there are only few unrecognized defective components (test escapes in ppm) that are not detected by the adaptive test procedure and reduce the quality of manufacture. In best case, the fraction of nonconforming units was reduced down to values under 40ppm (parts per million). A positive outcome of this work is that due to the very satisfactory results, the project will be continued in further consequence in practice of the company. ams AG has planned to proceed the adaptive test project and possibly implement it into real production test in the future.

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A Appendix

A.1 Product A: Summary of AT Results based on Production Data from 25 Wafer

Table 17: : Product A: Overview of AT Results comparing both developed Algorithm and AT with Continuity Tests as PAT Outlier Monitor Tests

Data of Conventional Test					*AT with Pareto Algorithm*			*AT with Pareto and PAT Outlier Algorithm*			*AT with Pareto and PAT Outlier Algorithm with additionally Continuity Tests as PAT Outlier Monitor Tests*		
Wafer ID	*Wafername*	*Dies tested #parts*	*Bad Dies #parts*	*Yield %*	Number of Test Escapes #parts	Fault Coverage %	Test Time Reduction %	Number of Test Escapes #parts	Fault Coverage %	Test Time Reduction %	*Number of Test Escapes #parts*	*Fault Coverage %*	*Test Time Reduction %*
1	C25972W01PA5	3200	3	99.91%	0	100.00%	64.18	0	100.00%	58.84	0	100.00%	48.63
2	C25972W02PD0	3107	1	99.97%	0	100.00%	64.22	0	100.00%	58.44	0	100.00%	52.74
3	C25972W03PF3	3208	3	99.91%	0	100.00%	64.24	0	100.00%	59.09	0	100.00%	50.49
4	C25972W04PA3	3148	3	99.90%	2	33.33%	64.15	2	33.33%	58.79	1	66.67%	51.64
5	C25972W05PC6	3127	2	99.94%	0	100.00%	64.35	0	100.00%	57.78	0	100.00%	49.89
6	C25972W06PF1	3174	2	99.94%	0	100.00%	64.45	0	100.00%	58.68	0	100.00%	49.76
7	C25972W07PA1	3272	2	99.94%	0	100.00%	64.12	0	100.00%	58.81	0	100.00%	51.28
8	C25972W08PC4	3280	3	99.91%	0	100.00%	64.29	0	100.00%	58.96	0	100.00%	51.83
9	C25972W09PE7	3216	1	99.97%	0	100.00%	64.18	0	100.00%	59.04	0	100.00%	52.40
10	C25972W10PC4	3184	10	99.69%	1	90.00%	64.32	1	90.00%	58.37	1	90.00%	50.11
11	C25972W11PE7	3164	6	99.81%	0	100.00%	61.22	0	100.00%	55.45	0	100.00%	48.93
12	C25972W12PH2	3174	7	99.78%	1	85.71%	64.47	1	85.71%	59.09	1	85.71%	46.98
13	C25972W13PC2	3184	0	100.00%	0	100.00%	64.19	0	100.00%	59.04	0	100.00%	51.31
14	C25972W14PE5	3160	0	100.00%	0	100.00%	64.37	0	100.00%	59.40	0	100.00%	50.00
15	C25972W15PH0	3263	5	99.85%	0	100.00%	64.04	0	100.00%	57.66	0	100.00%	50.69
16	C25972W16PC0	3208	1	99.97%	0	100.00%	64.25	0	100.00%	58.91	0	100.00%	52.63
17	C25972W17PE3	3224	3	99.91%	0	100.00%	64.21	0	100.00%	59.07	0	100.00%	50.43
18	C25972W18PG6	3176	0	100.00%	0	100.00%	64.35	0	100.00%	58.59	0	100.00%	46.87
19	C25972W19PB6	3196	0	100.00%	0	100.00%	64.29	0	100.00%	58.94	0	100.00%	49.84
20	C25972W20PG6	3207	1	99.97%	0	100.00%	64.26	0	100.00%	58.94	0	100.00%	50.07
21	C25972W21PB6	3192	1	99.97%	0	100.00%	64.24	0	100.00%	58.69	0	100.00%	48.81
22	C25972W22PE1	3136	2	99.94%	0	100.00%	64.41	0	100.00%	59.03	0	100.00%	49.80
23	C25972W23PG4	3112	0	100.00%	0	100.00%	64.27	0	100.00%	59.09	0	100.00%	47.51
24	C25972W24PB4	3184	1	99.97%	0	100.00%	64.31	0	100.00%	59.35	0	100.00%	49.42
25	C25972W25PD7	3152	2	99.94%	0	100.00%	64.17	0	100.00%	58.24	0	100.00%	50.46
Sum of entire Lot (a.u.)		***79648***	***59***	***-***	***4***	***-***	***-***	***4***	***-***	***-***	***3***	***-***	***-***
Mean of entire Lot (a.u.)		***-***	***2.36***	***99.93%***	***0.16***	***96.36%***	***64.14%***	***0.16***	***96.36%***	***58.65%***	***0.12***	***97.70%***	***50.10%***
Fraction of entire Lot (ppm)		***-***	***740.76 ppm***	***-***	***50.22 ppm***	***-***	***-***	***50.22 ppm***	***93.22%***	***-***	***37.67 ppm***	***-***	***-***

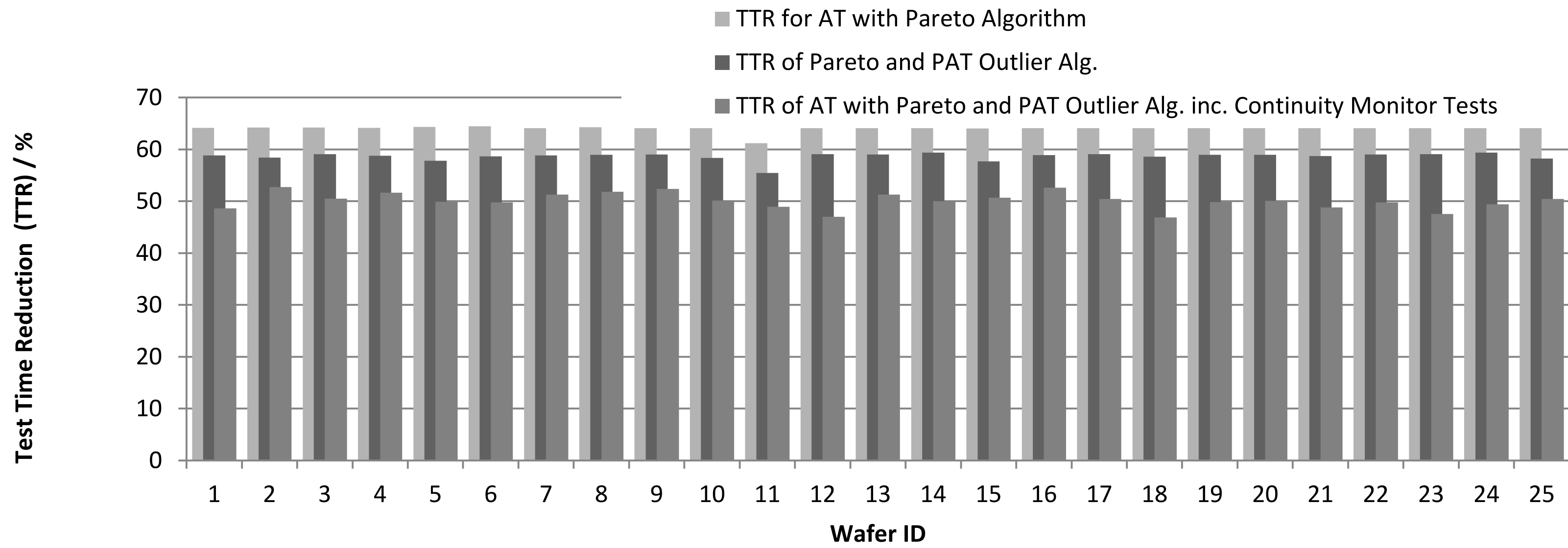

Figure 22: Comparison of Test Time Reductions for each Wafer of Product A for different AT Algorithm as well as AT with additionally Continuity Tests as Outlier Monitor Tests

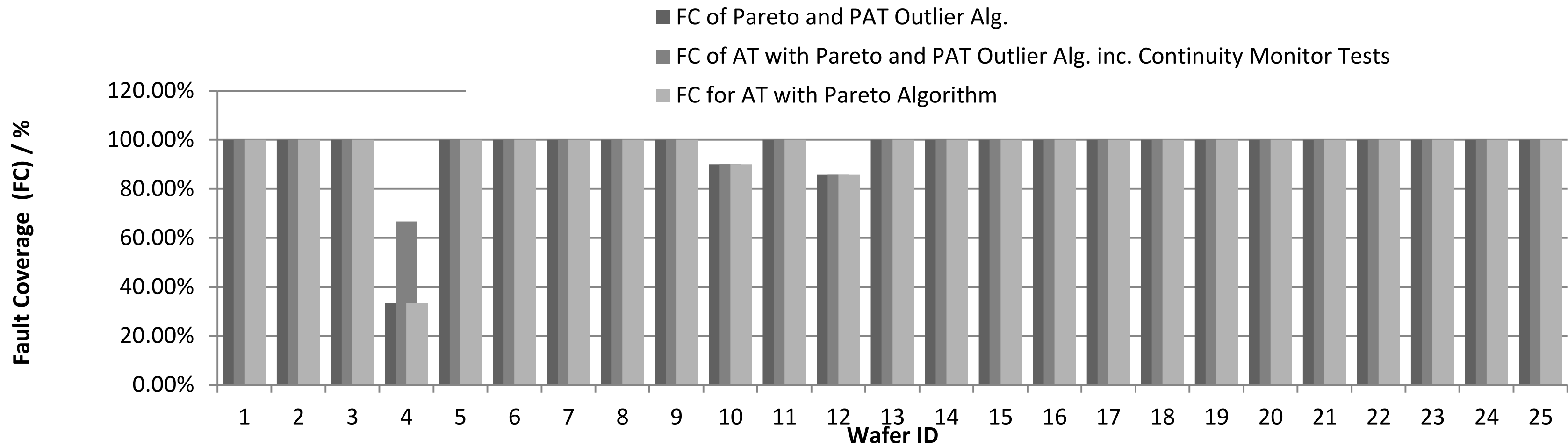

Figure 23: Comparison of Fault Coverage for each Wafer of A for different AT Algorithm as well as AT with additionally Continuity Tests as Outlier Monitor Tests

Table 18: : Product A: Test Escapes and Fraction Defective Estimation as well as Validation of the Results by comparing with Test Data form Conventional Test for AT with Pareto and PAT Outlier Algorithm

WaferID	Wafername	Percentage of Test Executions %	x_{sub}	$\hat{p}$	p_{wc}	$\hat{x}_{usub}$	$x_{wc,usub}$	x_{real}	$\hat{x}_{lot}$	$x_{wc,lot}$	x_{lot}	$\hat{p}_{AQL}$	$p_{AQL,wc}$	p_{AQL}
1	C25972W01PA5	70.87%	3	0.0073%	0.0190%	1	3	0	4	6	3	0.15%	0.21%	0.09%
2	C25972W02PD0	71.07%	1	0.0025%	0.0119%	0	2	0	1	3	1	0.05%	0.11%	0.03%
3	C25972W03PF3	70.75%	3	0.0073%	0.0190%	1	3	0	4	6	3	0.15%	0.21%	0.09%
4	C25972W04PA3	70.86%	1	0.0025%	0.0118%	0	2	2	1	3	3	0.05%	0.11%	0.09%
5	C25972W05PC6	71.39%	2	0.0050%	0.0157%	1	3	0	3	5	2	0.10%	0.18%	0.06%
6	C25972W06PF1	70.96%	2	0.0049%	0.0155%	1	3	0	3	5	2	0.10%	0.17%	0.06%
7	C25972W07PA1	70.85%	2	0.0048%	0.0151%	1	3	0	3	5	2	0.10%	0.17%	0.06%
8	C25972W08PC4	70.82%	3	0.0072%	0.0185%	1	3	0	4	6	3	0.14%	0.20%	0.09%
9	C25972W09PE7	70.74%	1	0.0024%	0.0116%	0	2	0	1	3	1	0.05%	0.10%	0.03%
10	C25972W10PC4	71.13%	9	0.0221%	0.0385%	4	6	1	13	15	10	0.44%	0.52%	0.31%
11	C25972W11PE7	71.68%	6	0.0147%	0.0290%	2	5	0	8	11	6	0.29%	0.39%	0.19%
12	C25972W12PH2	70.76%	6	0.0148%	0.0293%	2	5	1	8	11	7	0.30%	0.38%	0.22%
13	C25972W13PC2	70.74%	0	0.0000%	0.0074%	0	1	0	0	1	0	0.00%	0.03%	0.00%
14	C25972W14PE5	70.61%	0	0.0000%	0.0075%	0	1	0	0	1	0	0.00%	0.04%	0.00%
15	C25972W15PH0	71.43%	5	0.0119%	0.0250%	2	4	0	7	9	5	0.24%	0.31%	0.16%
16	C25972W16PC0	70.84%	1	0.0024%	0.0116%	0	2	0	1	3	1	0.05%	0.10%	0.03%
17	C25972W17PE3	70.77%	3	0.0073%	0.0189%	1	3	0	4	6	3	0.15%	0.21%	0.09%
18	C25972W18PG6	70.95%	0	0.0000%	0.0074%	0	1	0	0	1	0	0.00%	0.03%	0.00%
19	C25972W19PB6	70.82%	0	0.0000%	0.0073%	0	1	0	0	1	0	0.00%	0.03%	0.00%
20	C25972W20PG6	70.84%	1	0.0024%	0.0116%	0	2	0	1	3	1	0.05%	0.10%	0.03%
21	C25972W21PB6	70.92%	1	0.0025%	0.0116%	0	2	0	1	3	1	0.05%	0.10%	0.03%
22	C25972W22PE1	70.78%	2	0.0050%	0.0157%	1	3	0	3	5	2	0.10%	0.18%	0.06%
23	C25972W23PG4	70.74%	0	0.0000%	0.0076%	0	1	0	0	1	0	0.00%	0.04%	0.00%
24	C25972W24PB4	70.64%	1	0.0025%	0.0117%	0	2	0	1	3	1	0.05%	0.10%	0.03%
25	C25972W25PD7	71.12%	2	0.0050%	0.0156%	1	3	0	3	5	2	0.10%	0.18%	0.06%
Sum of entire Lot (a.u.)		***-***	***55***	***-***	***-***	***22***	***66***	***4***	***77***	***121***	***59***	***-***	***-***	***-***
Mean of entire Lot (a.u.)		***70.92%***	***2.2***	***0.01%***	***0.02%***	***0.90***	***2.64***	***0.16***	***3.10***	***4.84***	***2.36***	***0.11%***	***0.17%***	***0.07%***
Fraction of entire Lot (ppm)		***-***	***690.54***	***-***	***-***	***281.41***	***828.65***	***50.22***	***971.95***	***1519.18***	***740.76***	***-***	***-***	***-***

Table 19: : Product A: Test Escapes and Fraction Defective Estimation and Validation of the Results by comparing with Test Data form Conventional Test for AT with Pareto and PAT Outlier Algorithm and additionally Continuity Tests as PAT Outlier Monitor Tests

WaferID	Wafername	Percentage of Test Executions %	x_{sub}	$\hat{p}$	p_{wc}	$\hat{x}_{usub}$	$x_{wc,usub}$	x_{real}	$\hat{x}_{lot}$	$x_{wc,lot}$	x_{lot}	$\hat{p}_{AQL}$	$p_{AQL,wc}$	p_{AQL}
1	C25972W01PA5	75.95%	3	0.0069%	0.0177%	1	2	0	4	5	3	0.14%	0.17%	0.09%
2	C25972W02PD0	73.86%	1	0.0024%	0.0115%	0	2	0	1	3	1	0.05%	0.11%	0.03%
3	C25972W03PF3	75.01%	3	0.0069%	0.0179%	1	3	0	4	6	3	0.14%	0.21%	0.09%
4	C25972W04PA3	75.98%	2	0.0046%	0.0146%	1	2	1	3	4	3	0.09%	0.14%	0.09%
5	C25972W05PC6	75.28%	2	0.0047%	0.0148%	1	2	0	3	4	2	0.09%	0.14%	0.06%
6	C25972W06PF1	75.40%	2	0.0046%	0.0146%	1	2	0	3	4	2	0.09%	0.14%	0.06%
7	C25972W07PA1	74.58%	2	0.0046%	0.0143%	1	2	0	3	4	2	0.09%	0.14%	0.06%
8	C25972W08PC4	74.33%	3	0.0068%	0.0177%	1	3	0	4	6	3	0.14%	0.20%	0.09%
9	C25972W09PE7	74.02%	1	0.0023%	0.0111%	0	2	0	1	3	1	0.05%	0.10%	0.03%
10	C25972W10PC4	75.26%	9	0.0209%	0.0364%	3	5	1	12	14	10	0.42%	0.49%	0.31%
11	C25972W11PE7	75.07%	6	0.0140%	0.0277%	2	4	0	8	10	6	0.28%	0.35%	0.19%
12	C25972W12PH2	76.72%	6	0.0137%	0.0270%	2	4	1	8	10	7	0.27%	0.35%	0.22%
13	C25972W13PC2	74.58%	0	0.0000%	0.0070%	0	1	0	0	1	0	0.00%	0.03%	0.00%
14	C25972W14PE5	75.25%	0	0.0000%	0.0070%	0	1	0	0	1	0	0.00%	0.04%	0.00%
15	C25972W15PH0	74.88%	5	0.0114%	0.0239%	2	4	0	7	9	5	0.23%	0.31%	0.16%
16	C25972W16PC0	73.92%	1	0.0023%	0.0111%	0	2	0	1	3	1	0.05%	0.10%	0.03%
17	C25972W17PE3	75.05%	3	0.0069%	0.0178%	1	3	0	4	6	3	0.14%	0.21%	0.09%
18	C25972W18PG6	76.76%	0	0.0000%	0.0068%	0	1	0	0	1	0	0.00%	0.03%	0.00%
19	C25972W19PB6	75.31%	0	0.0000%	0.0069%	0	1	0	0	1	0	0.00%	0.03%	0.00%
20	C25972W20PG6	75.23%	1	0.0023%	0.0109%	0	2	0	1	3	1	0.05%	0.10%	0.03%
21	C25972W21PB6	75.82%	1	0.0023%	0.0109%	0	2	0	1	3	1	0.05%	0.10%	0.03%
22	C25972W22PE1	75.33%	2	0.0047%	0.0148%	1	2	0	3	4	2	0.09%	0.14%	0.06%
23	C25972W23PG4	76.45%	0	0.0000%	0.0070%	0	1	0	0	1	0	0.00%	0.04%	0.00%
24	C25972W24PB4	75.54%	1	0.0023%	0.0109%	0	2	0	1	3	1	0.05%	0.10%	0.03%
25	C25972W25PD7	74.97%	2	0.0047%	0.0148%	1	2	0	3	4	2	0.09%	0.14%	0.06%
Sum		***-***	***56***	***-***	***-***	***18***	***57***	***3***	***74***	***113***	***59***	***-***	***-***	***-***
Mean		***75.22%***	***2.24***	***0.01%***	***0.01%***	***0.74***	***2.28***	***0.12***	***2.98***	***4.52***	***2.36***	***0.10%***	***0.16%***	***0.07%***
Lot Fraction / ppm		***-***	***703.09***	***-***	***-***	***231.16***	***715.65***	***37.67***	***934.26***	***1418.74***	***740.76***	***-***	***-***	***-***

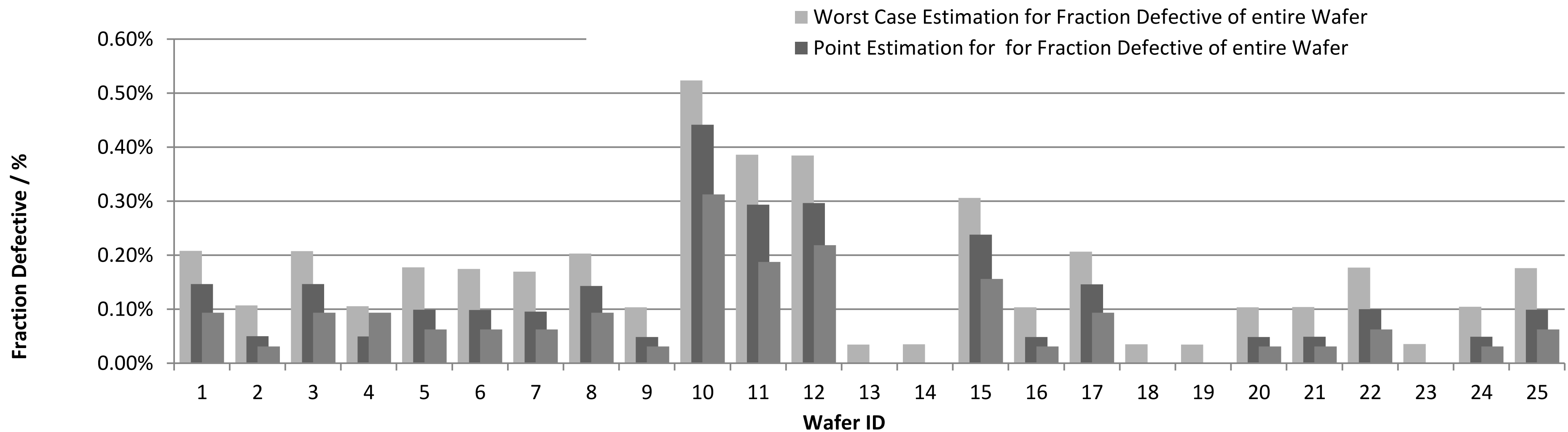

Figure 24: : Product A: Validation of the Lot Fraction Defective Estimation for AT with Pareto and PAT Outlier Algorithm

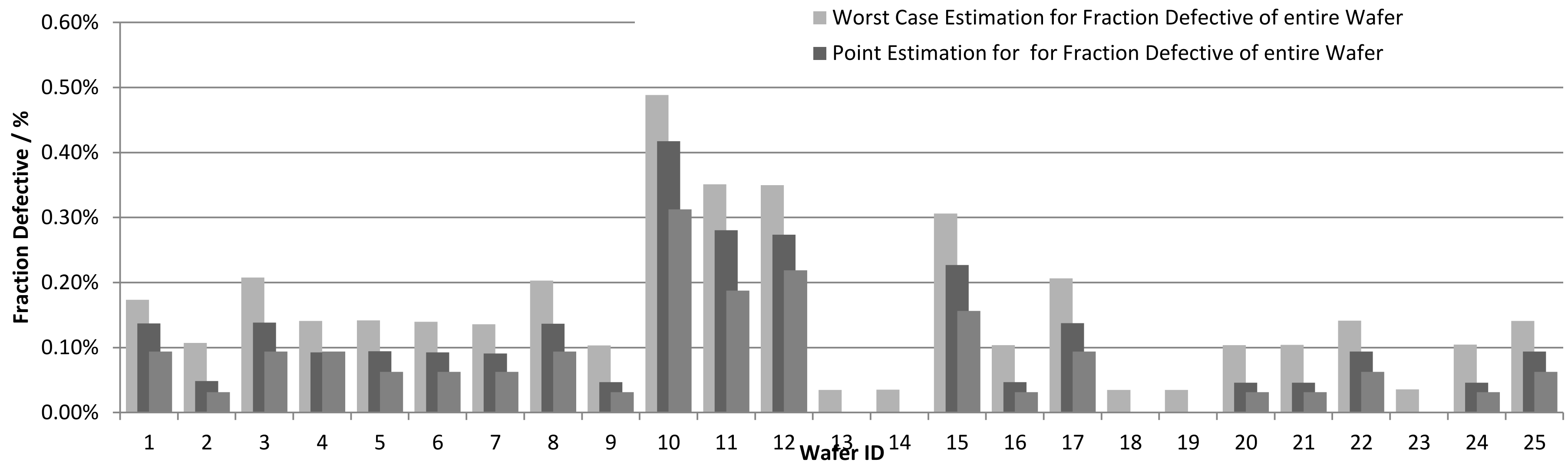

Figure 25: Product A: Validation of the Lot Fraction Defective Estimation for AT with Pareto and PAT Outlier Algorithm and additionally Continuity Tests as PAT Outlier Monitor Tests

B Product B: Summary of AT Results based on Production Data from 25 Wafer

Table 20 Product B:: Overview of AT Results comparing both developed Algorithm and AT with Continuity Tests as PAT Outlier Monitor Tests

Data of Conventional Test					*AT with Pareto Algorithm*			*AT with Pareto and PAT Outlier Algorithm*			*AT with Pareto and PAT Outlier Algorithm with additionally Continuity Tests as PAT Outlier Monitor Tests*		
Wafer ID	*Wafername*	*Dies tested #parts*	*Bad Dies #parts*	*Yield %*	Number of Test Escapes #parts	Fault Coverage %	Test Time Reduction %	Number of Test Escapes #parts	Fault Coverage %	Test Time Reduction %	*Number of Test Escapes #parts*	*Fault Coverage %*	*Test Time Reduction %*
1	C23401W01PC2	2227	5	99.78%	4	20.00%	61.41	3	40.00%	55.84	3	40.00%	44.97
2	C23401W02PE5	2112	2	99.91%	0	100.00%	61.08	0	100.00%	59.65	0	100.00%	49.18
3	C23401W03PH0	2144	3	99.86%	2	33.33%	61.34	2	33.33%	61.05	2	33.33%	49.30
4	C23401W04PC0	2200	6	99.73%	2	66.67%	61.61	2	66.67%	61.05	2	66.67%	52.13
5	C23401W05PE3	2176	4	99.82%	1	75.00%	61.33	0	100.00%	59.05	0	100.00%	46.47
6	C23401W06PG6	2152	3	99.86%	1	66.67%	61.37	1	66.67%	59.94	1	66.67%	50.84
7	C23401W07PB6	2184	8	99.63%	0	100.00%	58.44	0	100.00%	57.63	0	100.00%	50.52
8	C23401W08PE1	2160	2	99.91%	1	50.00%	61.08	0	100.00%	57.68	0	100.00%	51.39
9	C23401W09PG4	2146	1	99.95%	1	0.00%	61.43	1	0.00%	61.14	1	0.00%	53.79
10	C23401W10PE1	2240	4	99.82%	2	50.00%	61.39	2	50.00%	59.50	1	75.00%	49.79
11	C23401W11PG4	2200	3	99.86%	0	100.00%	61.52	0	100.00%	61.24	0	100.00%	52.87
12	C23401W12PB4	2103	8	99.62%	1	87.50%	61.51	1	87.50%	59.92	0	100.00%	50.08
13	C23401W13PD7	2144	10	99.53%	0	100.00%	61.31	0	100.00%	60.32	0	100.00%	52.36
14	C23401W14PG2	2168	3	99.86%	0	100.00%	61.51	0	100.00%	61.22	0	100.00%	53.65
15	C23401W15PB2	2216	3	99.86%	0	100.00%	61.40	0	100.00%	60.87	0	100.00%	52.36
16	C23401W16PD5	2184	9	99.59%	1	88.89%	57.15	0	100.00%	55.58	0	100.00%	49.09
17	C23401W17PG0	2200	9	99.59%	1	88.89%	60.32	1	88.89%	59.83	1	88.89%	51.59
18	C23401W18PB0	2215	12	99.46%	0	100.00%	60.09	0	100.00%	59.61	0	100.00%	52.15
19	C23401W19PD3	2216	3	99.86%	0	100.00%	61.15	0	100.00%	59.55	0	100.00%	54.57
20	C23401W20PB0	2224	3	99.87%	0	100.00%	61.33	0	100.00%	60.50	0	100.00%	53.62
21	C23401W21PD3	2168	9	99.58%	0	100.00%	57.16	0	100.00%	56.16	0	100.00%	50.88
22	C23401W22PF6	2199	2	99.91%	0	100.00%	61.64	0	100.00%	60.52	0	100.00%	51.68
23	C23401W23PA6	2256	4	99.82%	0	100.00%	55.01	0	100.00%	54.06	0	100.00%	48.05
24	C23401W24PD1	2168	0	100.00%	0	100.00%	61.36	0	100.00%	60.79	0	100.00%	50.65
25	C23401W25PF4	2199	2	99.91%	0	100.00%	61.55	0	100.00%	60.74	0	100.00%	53.49
Sum of entire Lot (a.u.)		**54601**	**118**	**-**	**17**	**-**	**-**	**13**	**-**	**-**	**11**	**-**	**-**
Mean of entire Lot (a.u.)		**-**	**4.72**	**99.78%**	**0.68**	**81.08%**	**60.58%**	**0.52**	**85.32%**	**59.34%**	**0.44**	**86.82%**	**51.02%**
Fraction of entire Lot (ppm)		**-**	**2161.13 ppm**	**-**	**311.35 ppm**	**-**	**-**	**238.09 ppm**	**-**	**-**	**201.46 ppm**	**-**	**-**

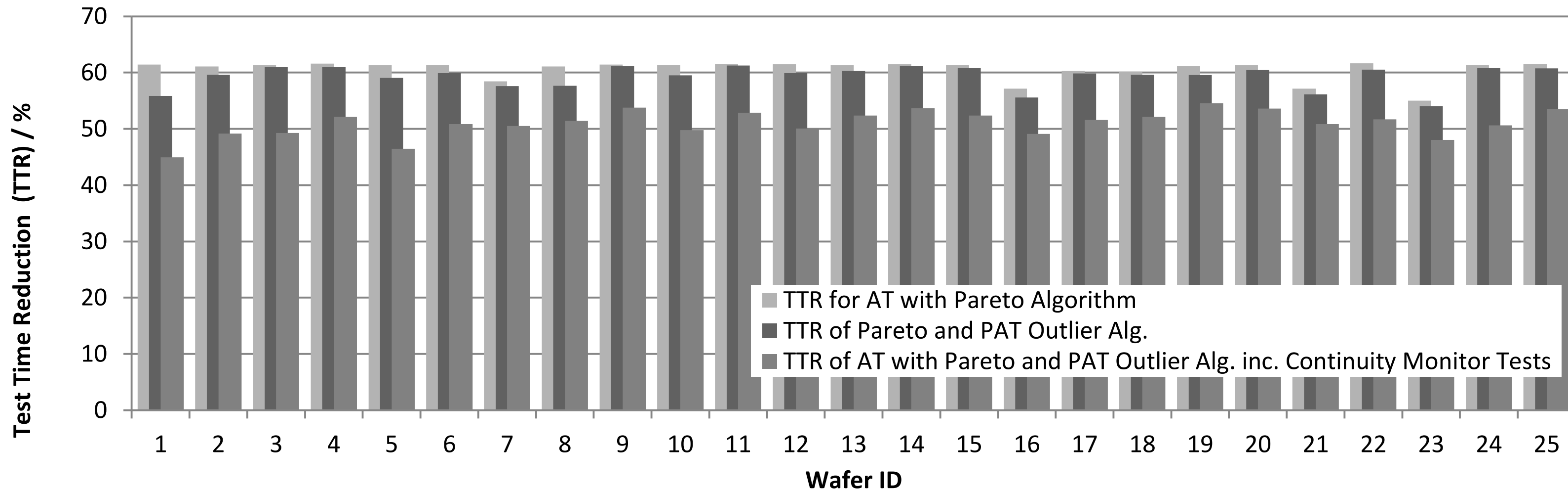

Figure 26: Comparison of Test Time Reductions for each Wafer of Product B for different AT Algorithm as well as AT with additionally Continuity Tests as Outlier Monitor Tests

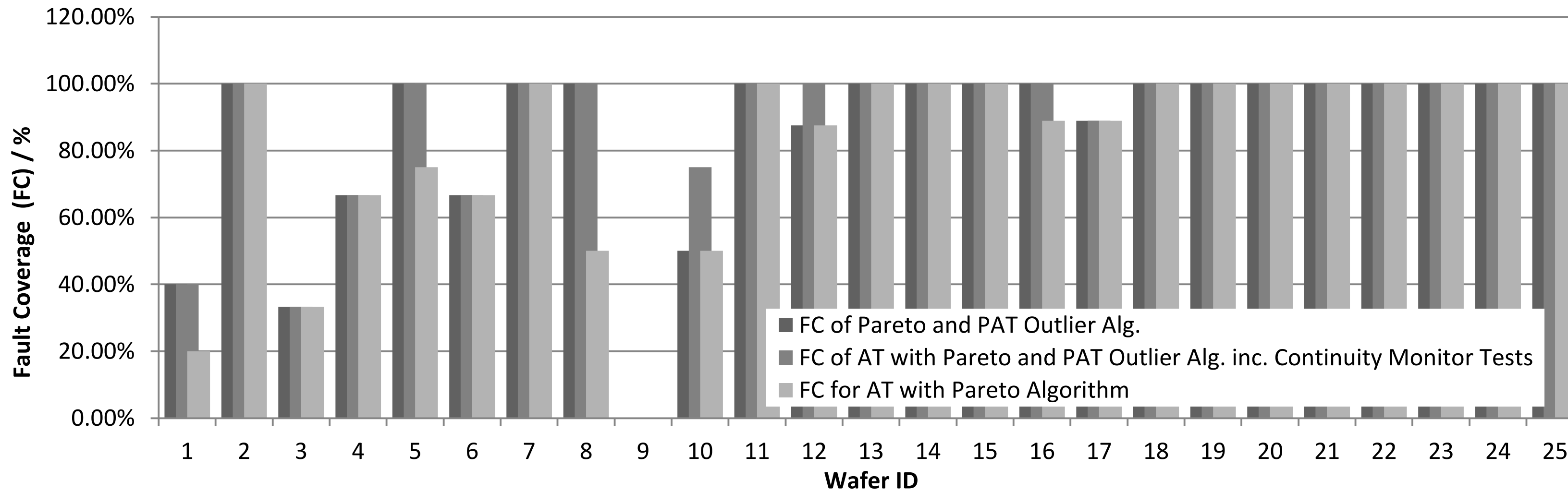

Figure 27: Comparison of Fault Coverage for each Wafer of Product Product B for different AT Algorithm as well as AT with additionally Continuity Tests as Outlier Monitor Tests

Table 21: Product B: Test Escapes and Fraction Defective Estimation and Validation of the Results by comparing with Test Data form Conventional Test for AT with Pareto and PAT Outlier Algorithm

WaferID	Wafername	Percentage of Test Executions %	x_{sub}	$\hat{p}$	p_{wc}	$\hat{x}_{usub}$	$x_{wc,usub}$	x_{real}	$\hat{x}_{lot}$	$x_{wc,lot}$	x_{lot}	$\hat{p}_{AQL}$	$p_{AQL,wc}$	p_{AQL}
1	C23401W01PC2	62.25%	2	0.0034%	0.0106%	1	4	3	3	6	5	0.15%	0.28%	0.23%
2	C23401W02PE5	58.85%	2	0.0037%	0.0118%	1	4	0	3	6	2	0.17%	0.30%	0.09%
3	C23401W03PH0	57.87%	1	0.0019%	0.0089%	1	3	2	2	4	3	0.08%	0.20%	0.14%
4	C23401W04PC0	57.98%	4	0.0073%	0.0167%	3	7	2	7	11	6	0.33%	0.52%	0.27%
5	C23401W05PE3	59.34%	4	0.0072%	0.0165%	3	6	0	7	10	4	0.32%	0.48%	0.18%
6	C23401W06PG6	58.64%	2	0.0037%	0.0116%	1	4	1	3	6	3	0.17%	0.29%	0.14%
7	C23401W07PB6	63.68%	8	0.0134%	0.0242%	5	8	0	13	16	8	0.60%	0.77%	0.36%
8	C23401W08PE1	60.55%	2	0.0036%	0.0112%	1	4	0	3	6	2	0.16%	0.29%	0.09%
9	C23401W09PG4	57.85%	0	0.0000%	0.0056%	0	2	1	0	2	1	0.00%	0.10%	0.05%
10	C23401W10PE1	59.08%	2	0.0035%	0.0111%	1	4	2	3	6	4	0.16%	0.28%	0.18%
11	C23401W11PG4	57.78%	3	0.0055%	0.0142%	2	6	0	5	9	3	0.25%	0.43%	0.14%
12	C23401W12PB4	58.81%	7	0.0132%	0.0248%	5	9	1	12	16	8	0.59%	0.80%	0.36%
13	C23401W13PD7	58.41%	10	0.0186%	0.0316%	7	12	0	17	22	10	0.84%	1.08%	0.45%
14	C23401W14PG2	57.88%	3	0.0056%	0.0144%	2	6	0	5	9	3	0.25%	0.43%	0.14%
15	C23401W15PB2	58.07%	3	0.0054%	0.0140%	2	6	0	5	9	3	0.24%	0.43%	0.14%
16	C23401W16PD5	65.96%	9	0.0146%	0.0254%	5	8	0	14	17	9	0.65%	0.82%	0.41%
17	C23401W17PG0	59.74%	8	0.0142%	0.0256%	5	10	1	13	18	9	0.64%	0.86%	0.41%
18	C23401W18PB0	59.84%	12	0.0211%	0.0342%	8	13	0	20	25	12	0.95%	1.18%	0.55%
19	C23401W19PD3	58.85%	3	0.0054%	0.0138%	2	5	0	5	8	3	0.24%	0.38%	0.14%
20	C23401W20PB0	58.24%	3	0.0054%	0.0139%	2	6	0	5	9	3	0.24%	0.42%	0.14%
21	C23401W21PD3	65.51%	9	0.0148%	0.0258%	5	8	0	14	17	9	0.66%	0.82%	0.41%
22	C23401W22PF6	58.35%	2	0.0036%	0.0114%	1	4	0	3	6	2	0.16%	0.29%	0.09%
23	C23401W23PA6	63.83%	4	0.0065%	0.0148%	2	5	0	6	9	4	0.29%	0.42%	0.18%
24	C23401W24PD1	58.13%	0	0.0000%	0.0055%	0	2	0	0	2	0	0.00%	0.10%	0.00%
25	C23401W25PF4	58.14%	2	0.0036%	0.0115%	1	5	0	3	7	2	0.16%	0.33%	0.09%
Sum of entire Lot (a.u.)		-	**105**	-	-	**68**	**151**	**13**	**173**	**256**	**118**	-	-	-
Mean of entire Lot (a.u.)		**59.74%**	**4.2**	**0.01%**	**0.02%**	**2.74**	**6.04**	**0.52**	**6.94**	**10.24**	**4.72**	**0.33%**	**0.49%**	**0.21%**
Fraction of entire Lot (ppm)		-	**1923.04**	-	-	**1253.26**	**2765.52**	**238.09**	**3176.31**	**4688.56**	**2161.13**	-	-	-

Table 22: Product B: Test Escapes and Fraction Defective Estimation and Validation of the Results by comparing with Test Data form Conventional Test for AT with Pareto and PAT Outlier Algorithm and additionally Continuity Tests as PAT Outlier Monitor Tests

WaferID	Wafername	Percentage of Test Executions %	x_{sub}	$\hat{p}$	p_{wc}	$\hat{x}_{usub}$	$x_{wc,usub}$	x_{real}	$\hat{x}_{lot}$	$x_{wc,lot}$	x_{lot}	$\hat{p}_{AQL}$	$p_{AQL,wc}$	p_{AQL}
1	C23401W01PC2	69.66%	2	0.0030%	0.0094%	1	3	3	3	5	5	0.13%	0.23%	0.23%
2	C23401W02PE5	66.14%	2	0.0033%	0.0105%	1	3	0	3	5	2	0.15%	0.25%	0.09%
3	C23401W03PH0	66.05%	1	0.0016%	0.0078%	1	2	2	2	3	3	0.07%	0.15%	0.14%
4	C23401W04PC0	64.20%	4	0.0066%	0.0151%	2	5	2	6	9	6	0.30%	0.43%	0.27%
5	C23401W05PE3	67.98%	4	0.0063%	0.0144%	2	4	0	6	8	4	0.28%	0.38%	0.18%
6	C23401W06PG6	64.97%	2	0.0033%	0.0105%	1	3	1	3	5	3	0.15%	0.24%	0.14%
7	C23401W07PB6	68.09%	8	0.0125%	0.0226%	4	7	0	12	15	8	0.56%	0.72%	0.36%
8	C23401W08PE1	64.77%	2	0.0033%	0.0105%	1	3	0	3	5	2	0.15%	0.24%	0.09%
9	C23401W09PG4	62.85%	0	0.0000%	0.0052%	0	2	1	0	2	1	0.00%	0.10%	0.05%
10	C23401W10PE1	67.58%	3	0.0046%	0.0119%	1	4	1	4	7	4	0.21%	0.33%	0.18%
11	C23401W11PG4	63.61%	3	0.0050%	0.0129%	2	4	0	5	7	3	0.22%	0.33%	0.14%
12	C23401W12PB4	65.94%	8	0.0134%	0.0242%	4	7	0	12	15	8	0.60%	0.75%	0.36%
13	C23401W13PD7	63.82%	10	0.0170%	0.0289%	6	10	0	16	20	10	0.77%	0.98%	0.45%
14	C23401W14PG2	63.03%	3	0.0051%	0.0132%	2	5	0	5	8	3	0.23%	0.39%	0.14%
15	C23401W15PB2	63.86%	3	0.0049%	0.0127%	2	4	0	5	7	3	0.22%	0.33%	0.14%
16	C23401W16PD5	69.87%	9	0.0137%	0.0240%	4	7	0	13	16	9	0.62%	0.77%	0.41%
17	C23401W17PG0	65.33%	8	0.0130%	0.0234%	4	8	1	12	16	9	0.58%	0.76%	0.41%
18	C23401W18PB0	64.69%	12	0.0195%	0.0316%	7	11	0	19	23	12	0.88%	1.09%	0.55%
19	C23401W19PD3	62.32%	3	0.0051%	0.0131%	2	5	0	5	8	3	0.23%	0.38%	0.14%
20	C23401W20PB0	63.04%	3	0.0050%	0.0129%	2	5	0	5	8	3	0.22%	0.38%	0.14%
21	C23401W21PD3	68.78%	9	0.0141%	0.0245%	4	7	0	13	16	9	0.63%	0.77%	0.41%
22	C23401W22PF6	64.39%	2	0.0033%	0.0103%	1	3	0	3	5	2	0.15%	0.24%	0.09%
23	C23401W23PA6	67.79%	4	0.0061%	0.0139%	2	4	0	6	8	4	0.27%	0.37%	0.18%
24	C23401W24PD1	65.05%	0	0.0000%	0.0049%	0	2	0	0	2	0	0.00%	0.10%	0.00%
25	C23401W25PF4	63.20%	2	0.0034%	0.0105%	1	4	0	3	6	2	0.15%	0.29%	0.09%
Sum of entire Lot (a.u.)		-	**107**	-	-	**55**	**122**	**11**	**162**	**229**	**118**	-	-	-
Mean of entire Lot (a.u.)		**65.48%**	**4.28**	**0.01%**	**0.02%**	**2.21**	**4.88**	**0.44**	**6.49**	**9.16**	**4.72**	**0.31%**	**0.44%**	**0.21%**
Fraction of entire Lot (ppm)		-	**1959.67**	-	-	**1013.94**	**2234.39**	**201.46**	**2973.61**	**4194.06**	**2161.13**	-	-	-

C Product C: Summary of AT Results based on Production Data from 25 Wafer

Table 23: Product C.: Overview of AT Results comparing both developed Algorithm and AT with Continuity Tests as PAT Outlier Monitor Tests

Data of Conventional Test					**AT with Pareto Algorithm**			**AT with Pareto and PAT Outlier Algorithm**			**AT with Pareto and PAT Outlier Algorithm with additionally Continuity Tests as PAT Outlier Monitor Tests**		
Wafer ID	*Wafername*	*Dies tested #parts*	*Bad Dies #parts*	*Yield %*	Number of Test Escapes #parts	Fault Coverage %	Test Time Reduction %	Number of Test Escapes #parts	Fault Coverage %	Test Time Reduction %	*Number of Test Escapes #parts*	*Fault Coverage %*	*Test Time Reduction %*
1	C24133W01PB7	1932	323	83.28%	11	96.59%	38.81	4	98.76%	24.01	1	99.69%	7.72
2	C24133W02PE2	1938	331	82.92%	20	93.96%	39.72	7	97.89%	23.23	0	100.00%	6.79
3	C24133W03PG5	1880	357	81.01%	9	97.48%	40.11	2	99.44%	21.38	0	100.00%	7.61
4	C24133W04PB5	1919	304	84.16%	13	95.72%	38.56	6	98.03%	20.68	2	99.34%	6.99
5	C24133W05PE0	1921	321	83.29%	26	91.90%	36.30	12	96.26%	19.54	2	99.38%	6.49
6	C24133W06PG3	1949	347	82.20%	14	95.97%	35.78	6	98.27%	20.74	3	99.14%	6.85
7	C24133W07PB3	1933	345	82.15%	15	95.65%	36.93	8	97.68%	19.96	4	98.84%	7.55
8	C24133W08PD6	2070	729	64.78%	35	95.20%	24.34	10	98.63%	12.54	1	99.86%	3.63
9	C24133W09PG1	1960	394	79.90%	23	94.16%	35.60	12	96.95%	19.10	4	98.98%	6.16
10	C24133W10PD6	1697	234	86.21%	6	97.44%	38.02	0	100.00%	22.40	0	100.00%	7.80
11	C24133W11PG1	1913	295	84.58%	15	94.92%	41.93	5	98.31%	22.88	3	98.98%	6.86
12	C24133W12PB1	1933	350	81.89%	10	97.14%	33.32	4	98.86%	20.63	0	100.00%	7.11
13	C24133W13PD4	1933	330	82.93%	7	100.00%	32.13	4	100.00%	18.91	2	100.00%	6.82
14	C24133W14PF7	1076	190	82.34%	12	100.00%	38.52	8	100.00%	22.01	0	100.00%	5.62
15	C24133W15PA7	1947	375	80.74%	6	98.40%	37.20	3	99.20%	23.21	0	100.00%	7.29
16	C24133W16PD2	1950	362	81.44%	22	93.92%	34.66	11	96.96%	21.28	2	99.45%	6.74
17	C24133W17PF5	1934	344	82.21%	24	93.02%	37.83	9	97.38%	21.48	3	99.13%	7.93
18	C24133W18PA5	1423	244	82.85%	22	100.00%	34.30	6	100.00%	19.49	3	100.00%	6.76
19	C24133W19PD0	1925	339	82.39%	10	100.00%	30.92	6	100.00%	16.92	0	100.00%	3.73
20	C24133W20PA5	1933	355	81.63%	11	96.90%	36.88	3	99.15%	20.09	1	99.72%	4.62
21	C24133W21PD0	1879	315	83.24%	17	94.60%	31.42	2	99.37%	15.26	0	100.00%	3.98
22	C24133W22PF3	1922	330	82.83%	19	94.24%	39.28	9	97.27%	21.81	1	99.70%	5.81
23	C24133W23PA3	1965	423	78.47%	15	100.00%	41.10	7	100.00%	21.20	1	100.00%	5.14
24	C24133W24PC6	1917	335	82.52%	15	95.52%	36.70	6	98.21%	21.06	1	99.70%	5.86
25	C24133W25PF1	1507	311	79.36%	29	90.68%	40.05	16	94.86%	20.06	3	99.04%	5.14
Sum of entire Lot (a.u.)		***46356***	***8583***	***-***	***406***	***-***	***-***	***166***	***-***	***-***	***37***	***-***	***-***
Mean of entire Lot (a.u.)		***-***	***343.32***	***81.57%***	***16.24***	***96.14%***	***36.42%***	***6.64***	***98.46%***	***20.40%***	***1.48***	***99.64%***	***6.28%***
Fraction of entire Lot (ppm)		***-***	***185154 ppm***	***-***	***8758 ppm***	***-***	***-***	***3581 ppm***	***-***	***-***	***798 ppm***	***-***	***-***

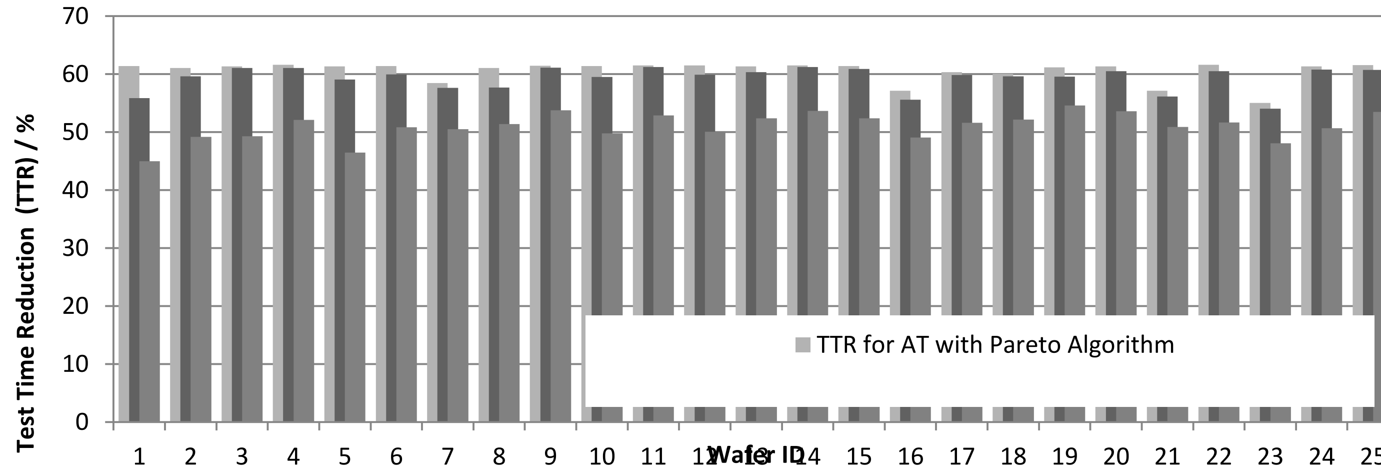

Figure 28: Comparison of Test Time Reductions for each Wafer of Product C for different AT Algorithm as well as AT with additionally Continuity Tests as Outlier Monitor Tests

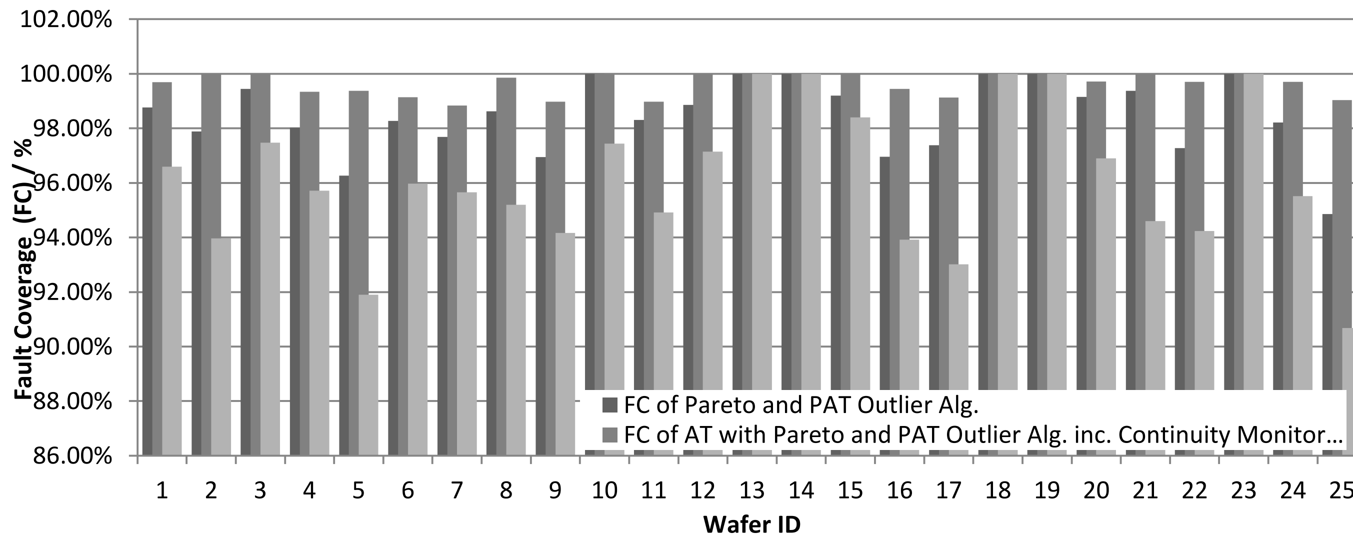

Figure 29: Comparison of Fault Coverage for each Wafer of Product C for different AT Algorithm as well as AT with additionally Continuity Tests as Outlier Monitor Tests

Table 24:Product C.: Test Escapes and Fraction Defective Estimation and Validation of the Results by comparing with Test Data form Conventional Test for AT with Pareto and PAT Outlier Algorithm

WaferID	Wafername	Percentage of Test Executions %	x_{sub}	$\hat{p}$	p_{wc}	$\hat{x}_{usub}$	$x_{wc,usub}$	x_{real}	$\hat{x}_{lot}$	$x_{wc,lot}$	x_{lot}	$\hat{p}_{AQL}$	$p_{AQL,wc}$	p_{AQL}
1	C24133W01PB7	79.36%	319	0.0345%	0.0379%	83	91	4	402	410	323	21.48%	21.91%	16.15%
2	C24133W02PE2	79.18%	324	0.0350%	0.0384%	85	93	7	409	417	331	21.78%	22.19%	16.55%
3	C24133W03PG5	80.31%	355	0.0396%	0.0433%	87	95	2	442	450	357	24.64%	25.09%	17.85%
4	C24133W04PB5	80.14%	298	0.0319%	0.0351%	74	81	6	372	379	304	19.85%	20.23%	15.20%
5	C24133W05PE0	80.85%	309	0.0330%	0.0363%	73	80	12	382	389	321	20.55%	20.91%	16.05%
6	C24133W06PG3	79.74%	341	0.0367%	0.0401%	87	95	6	428	436	347	22.82%	23.27%	17.35%
7	C24133W07PB3	83.23%	337	0.0352%	0.0385%	68	74	8	405	411	345	21.86%	22.19%	17.25%
8	C24133W08PD6	86.78%	719	0.0779%	0.0828%	110	116	10	829	835	729	48.44%	48.82%	36.45%
9	C24133W09PG1	80.75%	382	0.0410%	0.0446%	91	99	12	473	481	394	25.50%	25.93%	19.70%
10	C24133W10PD6	79.83%	234	0.0283%	0.0315%	59	66	0	293	300	234	17.57%	17.98%	11.70%
11	C24133W11PG1	79.18%	290	0.0317%	0.0350%	76	84	5	366	374	295	19.73%	20.14%	14.75%
12	C24133W12PB1	81.12%	346	0.0374%	0.0409%	81	88	4	427	434	350	23.26%	23.67%	17.50%
13	C24133W13PD4	80.64%	326	0.0349%	0.0382%	78	86	4	404	412	330	21.68%	22.09%	16.50%
14	C24133W14PF7	81.01%	182	0.0347%	0.0392%	43	48	8	225	230	190	21.57%	22.08%	9.50%
15	C24133W15PA7	79.11%	372	0.0409%	0.0446%	98	107	3	470	479	375	25.44%	25.92%	18.75%
16	C24133W16PD2	80.16%	351	0.0380%	0.0415%	87	95	11	438	446	362	23.61%	24.05%	18.10%
17	C24133W17PF5	79.99%	335	0.0365%	0.0399%	84	92	9	419	427	344	22.70%	23.14%	17.20%
18	C24133W18PA5	80.58%	238	0.0344%	0.0383%	57	64	6	295	302	244	21.42%	21.90%	12.20%
19	C24133W19PD0	82.30%	333	0.0355%	0.0389%	72	78	6	405	411	339	22.08%	22.43%	16.95%
20	C24133W20PA5	81.71%	352	0.0381%	0.0416%	79	86	3	431	438	355	23.69%	24.08%	17.75%
21	C24133W21PD0	82.76%	313	0.0340%	0.0373%	65	72	2	378	385	315	21.13%	21.51%	15.75%
22	C24133W22PF3	80.71%	321	0.0351%	0.0385%	77	84	9	398	405	330	21.82%	22.22%	16.50%
23	C24133W23PA3	81.88%	416	0.0457%	0.0495%	92	100	7	508	516	423	28.41%	28.86%	21.15%
24	C24133W24PC6	80.26%	329	0.0362%	0.0397%	81	89	6	410	418	335	22.52%	22.97%	16.75%
25	C24133W25PF1	81.05%	295	0.0419%	0.0461%	69	76	16	364	371	311	26.06%	26.56%	15.55%
Sum of entire Lot (a.u.)		**-**	***8417***	**-**	**-**	***1955***	***2139***	***166***	***10372***	***10556***	***8583***	**-**	**-**	**-**
Mean of entire Lot (a.u.)		***80.91%***	***336.68***	***0.04%***	***0.04%***	***78.19***	***85.56***	***6.64***	***414.87***	***422.24***	***343.32***	***23.58%***	***24.01%***	***17.17%***
Fraction of entire Lot (ppm)		**-**	***181573***	**-**	**-**	***42167***	***46143***	***3581***	***223740***	***227716***	***185154***	**-**	**-**	**-**

Table 25: Product C.: Test Escapes and Fraction Defective Estimation and Validation of the Results by comparing with Test Data form Conventional Test for AT with Pareto and PAT Outlier Algorithm and additionally Continuity Tests as PAT Outlier Monitor Tests

WaferID	Wafername	Percentage of Test Executions %	x_{sub}	$\hat{p}$	p_{wc}	$\hat{x}_{usub}$	$x_{wc,usub}$	x_{real}	$\hat{x}_{lot}$	$x_{wc,lot}$	x_{lot}	$\hat{p}_{AQL}$	$p_{AQL,wc}$	p_{AQL}
1	C24133W01PB7	93.34%	322	0.0300%	0.0300%	23	25	1	345	347	323	18.44%	18.54%	16.15%
2	C24133W02PE2	93.69%	331	0.0300%	0.0300%	22	24	0	353	355	331	18.79%	18.89%	16.55%
3	C24133W03PG5	92.97%	357	0.0300%	0.0400%	27	29	0	384	386	357	21.41%	21.52%	17.85%
4	C24133W04PB5	93.30%	302	0.0300%	0.0300%	22	24	2	324	326	304	17.29%	17.40%	15.20%
5	C24133W05PE0	93.41%	319	0.0300%	0.0300%	22	25	2	341	344	321	18.33%	18.49%	16.05%
6	C24133W06PG3	93.11%	344	0.0300%	0.0400%	25	28	3	369	372	347	19.69%	19.85%	17.35%
7	C24133W07PB3	93.75%	341	0.0300%	0.0400%	23	25	4	364	366	345	19.65%	19.76%	17.25%
8	C24133W08PD6	96.23%	728	0.0700%	0.0800%	28	30	1	756	758	729	44.20%	44.31%	36.45%
9	C24133W09PG1	93.48%	390	0.0400%	0.0400%	27	30	4	417	420	394	22.48%	22.64%	19.70%
10	C24133W10PD6	92.97%	234	0.0200%	0.0300%	18	20	0	252	254	234	15.10%	15.22%	11.70%
11	C24133W11PG1	93.75%	292	0.0300%	0.0300%	19	21	3	311	313	295	16.75%	16.86%	14.75%
12	C24133W12PB1	93.38%	350	0.0300%	0.0400%	25	27	0	375	377	350	20.45%	20.56%	17.50%
13	C24133W13PD4	93.07%	328	0.0300%	0.0300%	24	27	2	352	355	330	18.87%	19.03%	16.50%
14	C24133W14PF7	94.76%	190	0.0300%	0.0400%	11	12	0	201	202	190	19.29%	19.39%	9.50%
15	C24133W15PA7	93.11%	375	0.0400%	0.0400%	28	30	0	403	405	375	21.81%	21.91%	18.75%
16	C24133W16PD2	93.71%	360	0.0300%	0.0400%	24	26	2	384	386	362	20.70%	20.81%	18.10%
17	C24133W17PF5	92.60%	341	0.0300%	0.0400%	27	30	3	368	371	344	19.94%	20.11%	17.20%
18	C24133W18PA5	93.30%	241	0.0300%	0.0300%	17	19	3	258	260	244	18.71%	18.85%	12.20%
19	C24133W19PD0	96.04%	339	0.0300%	0.0300%	14	15	0	353	354	339	19.26%	19.32%	16.95%
20	C24133W20PA5	95.71%	354	0.0300%	0.0400%	16	17	1	370	371	355	20.34%	20.40%	17.75%
21	C24133W21PD0	95.68%	315	0.0300%	0.0300%	14	16	0	329	331	315	18.38%	18.49%	15.75%
22	C24133W22PF3	94.70%	329	0.0300%	0.0300%	18	20	1	347	349	330	19.04%	19.15%	16.50%
23	C24133W23PA3	95.28%	422	0.0400%	0.0400%	21	23	1	443	445	423	24.78%	24.89%	21.15%
24	C24133W24PC6	94.40%	334	0.0300%	0.0300%	20	22	1	354	356	335	19.45%	19.56%	16.75%
25	C24133W25PF1	95.00%	308	0.0400%	0.0400%	16	18	3	324	326	311	23.20%	23.34%	15.55%
Sum of entire Lot (a.u.)		***-***	***8546***	***-***	***-***	***531***	***583***	***37***	***9077***	***9129***	***8583***	***-***	***-***	***-***
Mean of entire Lot (a.u.)		***94.03%***	***341.84***	***0.03%***	***0.04%***	***21.24***	***23.32***	***1.48***	***363.08***	***365.16***	***343.32***	***20.65%***	***20.77%***	***17.17%***
Fraction of entire Lot (ppm)		***-***	***184356***	***-***	***-***	***11455***	***12577***	***798***	***195811***	***196932***	***185154***	***-***	***-***	***-***

D Product D: Summary of AT Results based on Production Data from 25 Wafer

Table 26: Pruduct D: Overview of AT Results comparing both developed Algorithm and AT with Continuity Tests as PAT Outlier Monitor Tests

Data of Conventional Test					**AT with Pareto Algorithm**			*AT with Pareto and PAT Outlier Algorithm*			*AT with Pareto and PAT Outlier Algorithm with additionally Continuity Tests as PAT Outlier Monitor Tests*		
Wafer ID	*Wafername*	*Dies tested #parts*	*Bad Dies #parts*	*Yield %*	**Number of Test Escapes #parts**	**Fault Coverage %**	**Test Time Reduction %**	**Number of Test Escapes #parts**	**Fault Coverage %**	**Test Time Reduction %**	*Number of Test Escapes #parts*	*Fault Coverage %*	*Test Time Reduction %*
1	C25208W01PB2	25662	59	99.77%	7	88.14%	30.11	4	93.22%	18.00	1	98.31%	13.34
2	C25208W02PD5	25662	63	99.75%	13	79.37%	28.68	2	96.83%	20.36	1	98.41%	18.03
3	C25208W03PG0	25662	63	99.75%	1	98.41%	25.64	0	100.00%	17.82	0	100.00%	16.40
4	C25208W04PB0	25662	67	99.74%	15	77.61%	30.13	8	88.06%	19.65	1	98.51%	14.85
5	C25208W05PD3	25662	69	99.73%	2	97.10%	25.62	1	98.55%	17.75	1	98.55%	16.11
6	C25208W06PF6	25662	66	99.74%	2	96.97%	25.63	1	98.48%	17.68	1	98.48%	15.93
7	C25208W07PA6	25662	96	99.63%	1	98.96%	25.62	1	98.96%	19.36	1	98.96%	17.24
8	C25208W08PD1	25662	75	99.71%	3	96.00%	25.66	2	97.33%	19.90	0	100.00%	15.53
9	C25208W09PF4	25662	67	99.74%	1	98.51%	19.88	0	100.00%	13.79	0	100.00%	12.77
10	C25208W10PD1	25662	63	99.75%	9	85.71%	25.63	3	95.24%	17.02	1	98.41%	14.30
11	C25208W11PF4	25662	76	99.70%	2	97.37%	25.61	1	98.68%	18.12	1	98.68%	16.44
12	C25208W12PA4	25662	63	99.75%	5	92.06%	24.39	2	96.83%	15.27	2	96.83%	13.60
13	C25208W13PC7	25662	53	99.79%	7	100.00%	30.13	1	100.00%	19.11	0	100.00%	15.98
14	C25208W14PF2	25662	59	99.77%	4	100.00%	17.94	0	100.00%	11.32	0	100.00%	10.04
15	C25208W15PA2	25662	69	99.73%	1	98.55%	20.64	1	98.55%	15.43	1	98.55%	13.72
16	C25208W16PC5	25662	89	99.65%	3	96.63%	20.64	3	96.63%	15.89	3	96.63%	14.45
17	C25208W17PF0	25662	111	99.57%	7	93.69%	25.63	7	93.69%	19.09	2	98.20%	14.62
18	C25208W18PA0	25662	83	99.68%	11	100.00%	25.17	8	100.00%	14.45	0	100.00%	10.33
19	C25208W19PC3	25662	94	99.63%	1	100.00%	20.63	1	100.00%	15.24	1	100.00%	13.59
20	C25208W20PA0	25662	91	99.65%	2	97.80%	20.62	2	97.80%	16.24	2	97.80%	14.52
21	C25208W21PC3	25662	88	99.66%	4	95.45%	25.61	2	97.73%	16.96	0	100.00%	14.22
22	C25208W22PE6	25662	105	99.59%	19	81.90%	30.12	3	97.14%	19.81	2	98.10%	17.91
23	C25208W23PH1	25662	87	99.66%	10	100.00%	25.63	2	100.00%	14.88	2	100.00%	13.16
24	C25208W24PC1	25662	79	99.69%	1	98.73%	19.84	0	100.00%	15.34	0	100.00%	13.89
25	C25208W25PE4	25662	86	99.66%	14	83.72%	30.12	8	90.70%	15.61	2	97.67%	11.34
Sum of entire Lot (a.u.)		**641550**	**1921**	**-**	**145**	**-**	**-**	**63**	**-**	**-**	**25**	**-**	**-**
Mean of entire Lot (a.u.)		**-**	**76.84**	**99.70%**	**5.8**	**94.11%**	**25.01%**	**2.52**	**97.38%**	**16.96%**	**1**	**98.88%**	**14.49%**
Fraction of entire Lot (ppm)		**-**	**2994.31 ppm**	**-**	**226.02 ppm**	**-**	**-**	**98.20 ppm**	**-**	**-**	**38.97 ppm**	**-**	**-**

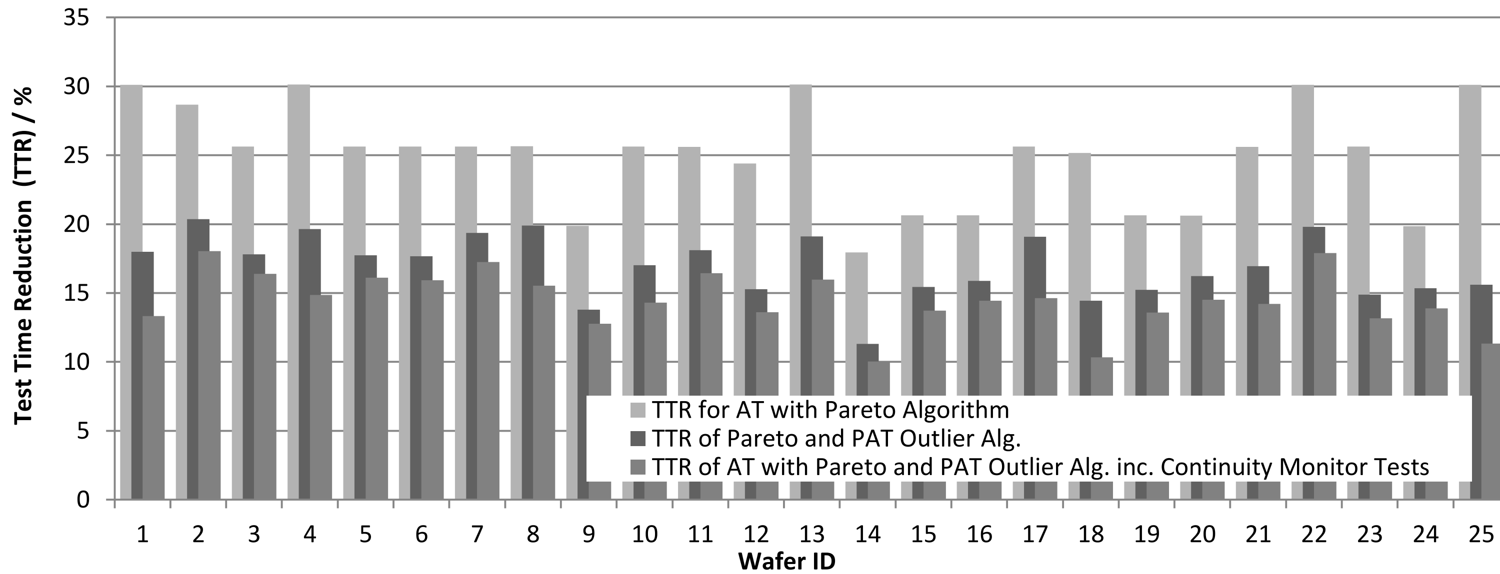

Figure 30: Comparison of Test Time Reductions for each Wafer of Product D for different AT Algorithm as well as AT with additionally Continuity Tests as Outlier Monitor Tests

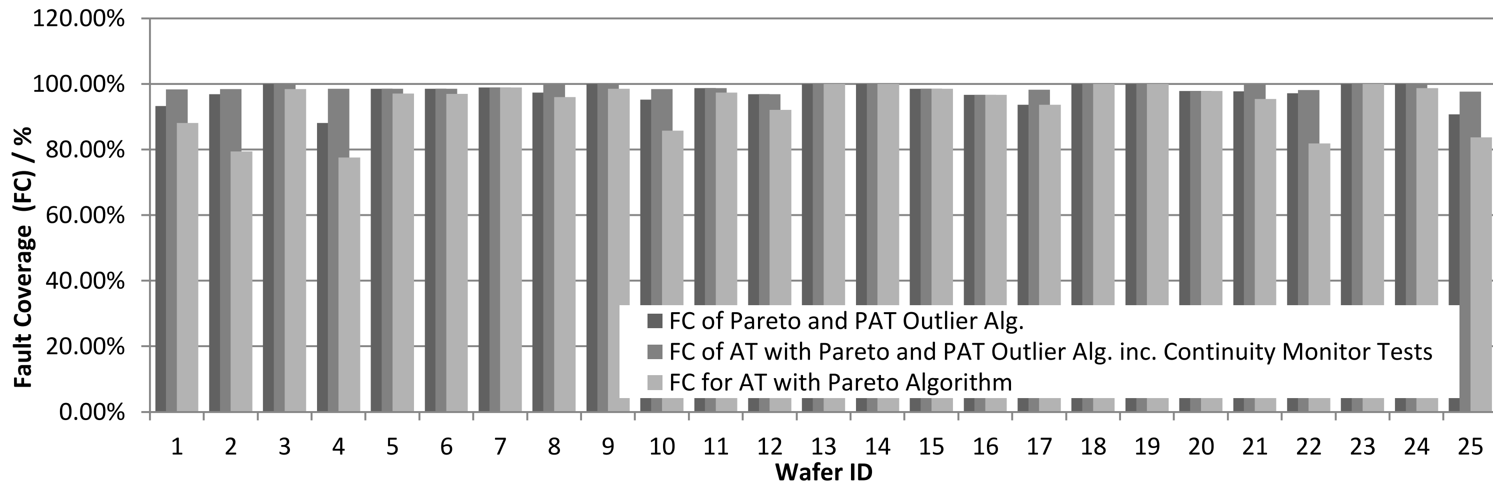

Figure 31: Comparison of Fault Coverage for each Wafer of Product D for different AT Algorithm as well as AT with additionally Continuity Tests as Outlier Monitor Tests

Table 27: Product D: Test Escapes and Fraction Defective Estimation and Validation of the Results by comparing with Test Data form Conventional Test for AT with Pareto and PAT Outlier Algorithm

WaferID	Wafername	Percentage of Test Executions %	x_{sub}	$\hat{p}$	p_{wc}	$\hat{x}_{usub}$	$x_{wc,usub}$	x_{real}	$\hat{x}_{lot}$	$x_{wc,lot}$	x_{lot}	$\hat{p}_{AQL}$	$p_{AQL,wc}$	p_{AQL}
1	C25208W01PB2	78.72%	55	0.0062%	0.0078%	15	19	4	70	74	59	0.28%	0.30%	0.23%
2	C25208W02PD5	78.06%	61	0.0069%	0.0086%	17	21	2	78	82	63	0.31%	0.33%	0.25%
3	C25208W03PG0	80.33%	63	0.0070%	0.0086%	15	19	0	78	82	63	0.31%	0.33%	0.25%
4	C25208W04PB0	77.51%	59	0.0068%	0.0084%	17	21	8	76	80	67	0.30%	0.32%	0.26%
5	C25208W05PD3	80.42%	68	0.0075%	0.0092%	17	20	1	85	88	69	0.34%	0.35%	0.27%
6	C25208W06PF6	80.21%	65	0.0072%	0.0088%	16	20	1	81	85	66	0.32%	0.34%	0.26%
7	C25208W07PA6	79.09%	95	0.0107%	0.0127%	25	30	1	120	125	96	0.48%	0.50%	0.37%
8	C25208W08PD1	78.23%	73	0.0083%	0.0101%	20	25	2	93	98	75	0.37%	0.39%	0.29%
9	C25208W09PF4	84.89%	67	0.0070%	0.0086%	12	15	0	79	82	67	0.32%	0.33%	0.26%
10	C25208W10PD1	81.69%	60	0.0065%	0.0081%	13	17	3	73	77	63	0.29%	0.31%	0.25%
11	C25208W11PF4	80.37%	75	0.0083%	0.0100%	18	22	1	93	97	76	0.37%	0.39%	0.30%
12	C25208W12PA4	83.14%	61	0.0065%	0.0081%	12	15	2	73	76	63	0.29%	0.30%	0.25%
13	C25208W13PC7	78.93%	52	0.0058%	0.0074%	14	17	1	66	69	53	0.26%	0.28%	0.21%
14	C25208W14PF2	86.55%	59	0.0061%	0.0075%	9	11	0	68	70	59	0.27%	0.28%	0.23%
15	C25208W15PA2	82.25%	68	0.0073%	0.0090%	15	18	1	83	86	69	0.33%	0.34%	0.27%
16	C25208W16PC5	81.72%	86	0.0094%	0.0112%	19	23	3	105	109	89	0.42%	0.44%	0.35%
17	C25208W17PF0	79.38%	104	0.0117%	0.0137%	27	32	7	131	136	111	0.52%	0.54%	0.43%
18	C25208W18PA0	79.77%	75	0.0084%	0.0101%	19	23	8	94	98	83	0.38%	0.39%	0.32%
19	C25208W19PC3	82.47%	93	0.0100%	0.0119%	20	23	1	113	116	94	0.45%	0.46%	0.37%
20	C25208W20PA0	81.33%	89	0.0097%	0.0116%	20	24	2	109	113	91	0.44%	0.45%	0.35%
21	C25208W21PC3	80.90%	86	0.0094%	0.0113%	20	24	2	106	110	88	0.42%	0.44%	0.34%
22	C25208W22PE6	78.40%	102	0.0116%	0.0136%	28	33	3	130	135	105	0.52%	0.54%	0.41%
23	C25208W23PH1	82.89%	85	0.0091%	0.0109%	18	21	2	103	106	87	0.41%	0.42%	0.34%
24	C25208W24PC1	83.39%	79	0.0084%	0.0101%	16	19	0	95	98	79	0.38%	0.39%	0.31%
25	C25208W25PE4	83.69%	78	0.0083%	0.0100%	15	18	8	93	96	86	0.37%	0.38%	0.34%
Sum of entire Lot (a.u.)		***-***	***1858***	***-***	***-***	***439***	***530***	***63***	***2297***	***2388***	***1921***	***-***	***-***	***-***
Mean of entire Lot (a.u.)		***80.97%***	***74.32***	***0.01%***	***0.01%***	***17.55***	***21.20***	***2.52***	***91.87***	***95.52***	***76.84***	***0.37%***	***0.38%***	***0.30%***
Fraction of entire Lot (ppm)		***-***	***2896***	***-***	***-***	***684***	***826***	***98***	***3580***	***3722***	***2994***	***-***	***-***	***-***

Table 28: Product D: Test Escapes and Fraction Defective Estimation and Validation of the Results by comparing with Test Data form Conventional Test for AT with Pareto and PAT Outlier Algorithm and additionally Continuity Tests as PAT Outlier Monitor Tests

WaferID	Wafername	Percentage of Test Executions %	x_{sub}	$\hat{p}$	p_{wc}	$\hat{x}_{usub}$	$x_{wc,usub}$	x_{real}	$\hat{x}_{lot}$	$x_{wc,lot}$	x_{lot}	$\hat{p}_{AQL}$	$p_{AQL,wc}$	p_{AQL}
1	C25208W01PB2	84.55%	58	0.0061%	0.0076%	11	13	1	69	71	59	0.27%	0.28%	0.23%
2	C25208W02PD5	80.40%	62	0.0068%	0.0085%	15	19	1	77	81	63	0.31%	0.32%	0.25%
3	C25208W03PG0	81.90%	63	0.0068%	0.0084%	14	17	0	77	80	63	0.31%	0.32%	0.25%
4	C25208W04PB0	83.41%	66	0.0070%	0.0086%	13	16	1	79	82	67	0.32%	0.33%	0.26%
5	C25208W05PD3	82.24%	68	0.0073%	0.0090%	15	18	1	83	86	69	0.33%	0.34%	0.27%
6	C25208W06PF6	82.17%	65	0.0070%	0.0086%	14	17	1	79	82	66	0.32%	0.33%	0.26%
7	C25208W07PA6	81.38%	95	0.0104%	0.0123%	22	26	1	117	121	96	0.47%	0.48%	0.37%
8	C25208W08PD1	82.24%	75	0.0081%	0.0098%	16	20	0	91	95	75	0.36%	0.38%	0.29%
9	C25208W09PF4	86.01%	67	0.0069%	0.0085%	11	13	0	78	80	67	0.31%	0.32%	0.26%
10	C25208W10PD1	84.36%	62	0.0065%	0.0081%	11	14	1	73	76	63	0.29%	0.30%	0.25%
11	C25208W11PF4	82.18%	75	0.0081%	0.0098%	16	20	1	91	95	76	0.36%	0.38%	0.30%
12	C25208W12PA4	84.98%	61	0.0064%	0.0079%	11	13	2	72	74	63	0.29%	0.30%	0.25%
13	C25208W13PC7	82.57%	53	0.0057%	0.0072%	11	14	0	64	67	53	0.26%	0.27%	0.21%
14	C25208W14PF2	88.06%	59	0.0060%	0.0074%	8	10	0	67	69	59	0.27%	0.28%	0.23%
15	C25208W15PA2	84.22%	68	0.0072%	0.0088%	13	16	1	81	84	69	0.32%	0.34%	0.27%
16	C25208W16PC5	83.38%	86	0.0092%	0.0110%	17	21	3	103	107	89	0.41%	0.43%	0.35%
17	C25208W17PF0	83.50%	109	0.0116%	0.0136%	22	25	2	131	134	111	0.52%	0.54%	0.43%
18	C25208W18PA0	85.32%	83	0.0087%	0.0104%	14	17	0	97	100	83	0.39%	0.40%	0.32%
19	C25208W19PC3	84.37%	93	0.0098%	0.0116%	17	20	1	110	113	94	0.44%	0.45%	0.37%
20	C25208W20PA0	83.29%	89	0.0095%	0.0113%	18	21	2	107	110	91	0.43%	0.44%	0.35%
21	C25208W21PC3	83.59%	88	0.0094%	0.0112%	17	21	0	105	109	88	0.42%	0.44%	0.34%
22	C25208W22PE6	80.49%	103	0.0114%	0.0134%	25	29	2	128	132	105	0.51%	0.53%	0.41%
23	C25208W23PH1	84.87%	85	0.0089%	0.0107%	15	18	2	100	103	87	0.40%	0.41%	0.34%
24	C25208W24PC1	84.96%	79	0.0083%	0.0100%	14	17	0	93	96	79	0.37%	0.38%	0.31%
25	C25208W25PE4	88.90%	84	0.0084%	0.0101%	10	13	2	94	97	86	0.38%	0.39%	0.34%
Sum of entire Lot (a.u.)		**-**	**1896**	**-**	**-**	**371**	**448**	**25**	**2267**	**2344**	**1921**	**-**	**-**	**-**
Mean of entire Lot (a.u.)		**83.73%**	**75.84**	**0.01%**	**0.01%**	**14.83**	**17.92**	**1.00**	**90.67**	**93.76**	**76.84**	**0.36%**	**0.37%**	**0.30%**
Fraction of entire Lot (ppm)		**-**	**2955**	**-**	**-**	**578**	**698**	**39**	**3533**	**3654**	**2994**	**-**	**-**	**-**

E Product E: Summary of AT Results based on Production Data from 25 Wafer

Table 29: **Product E:** : Overview of AT Results comparing both developed Algorithm and AT with Continuity Tests as PAT Outlier Monitor Tests

Data of Conventional Test					AT with Pareto Algorithm			AT with Pareto and PAT Outlier Algorithm			AT with Pareto and PAT Outlier Algorithm with additionally Continuity Tests as PAT Outlier Monitor Tests		
Wafer ID	*Wafername*	*Dies tested #parts*	*Bad Dies #parts*	*Yield %*	Number of Test Escapes #parts	Fault Coverage %	Test Time Reduction %	Number of Test Escapes #parts	Fault Coverage %	Test Time Reduction %	*Number of Test Escapes #parts*	*Fault Coverage %*	*Test Time Reduction %*
1	C25357W01PH0	4694	272	94.21%	6	97.79%	28.26	4	98.53%	24.90	0	100.00%	18.14
2	C25357W02PC0	4694	258	94.50%	2	99.22%	24.25	1	99.61%	21.72	1	99.61%	16.95
3	C25357W03PE3	4694	317	93.25%	5	98.42%	21.68	4	98.74%	19.14	2	99.37%	14.08
4	C25357W04PG6	4694	338	92.80%	15	95.56%	30.72	13	96.15%	27.32	8	97.63%	20.03
5	C25357W05PB6	4694	319	93.20%	19	94.04%	42.59	10	96.87%	29.79	8	97.49%	22.52
6	C25357W06PE1	4694	356	92.42%	20	94.38%	46.39	10	97.19%	27.97	8	97.75%	21.76
7	C25357W07PG4	4694	317	93.25%	7	97.79%	27.96	7	97.79%	25.37	3	99.05%	18.63
8	C25357W08PB4	4694	334	92.88%	8	97.60%	17.44	8	97.60%	15.80	7	97.90%	12.10
9	C25357W09PD7	4694	336	92.84%	4	98.81%	25.75	3	99.11%	23.22	3	99.11%	17.85
10	C25357W10PB4	4694	334	92.88%	6	98.20%	28.62	6	98.20%	25.69	2	99.40%	18.37
11	C25357W11PD7	4694	314	93.31%	5	98.41%	26.61	5	98.41%	23.80	2	99.36%	17.30
12	C25357W12PG2	4694	331	92.95%	4	98.79%	23.56	4	98.79%	21.32	3	99.09%	16.85
13	C25357W13PB2	4694	306	93.48%	6	100.00%	26.85	2	100.00%	22.38	2	100.00%	17.62
14	C25357W14PD5	4694	292	93.78%	9	100.00%	30.89	9	100.00%	27.97	3	100.00%	21.33
15	C25357W15PG0	4694	343	92.69%	10	97.08%	28.28	5	98.54%	21.23	2	99.42%	15.19
16	C25357W16PB0	4694	330	92.97%	8	97.58%	26.74	8	97.58%	24.21	7	97.88%	19.31
17	C25357W17PD3	4694	352	92.50%	12	96.59%	28.29	12	96.59%	25.87	1	99.72%	15.68
18	C25357W18PF6	4694	350	92.54%	6	100.00%	25.77	6	100.00%	23.45	4	100.00%	16.81
19	C25357W19PA6	4694	328	93.01%	3	100.00%	23.60	3	100.00%	21.65	2	100.00%	16.59
20	C25357W20PF6	4694	288	93.86%	13	95.49%	25.31	6	97.92%	20.80	6	97.92%	16.67
21	C25357W21PA6	4694	334	92.88%	3	99.10%	19.95	2	99.40%	16.00	2	99.40%	12.60
22	C25357W22PD1	4694	310	93.40%	8	97.42%	28.26	5	98.39%	23.93	4	98.71%	18.09
23	C25357W23PF4	4694	403	91.41%	2	100.00%	25.24	1	100.00%	22.93	0	100.00%	18.00
24	C25357W24PA4	4694	362	92.29%	3	99.17%	25.19	3	99.17%	22.78	3	99.17%	17.82
25	C25357W25PC7	4694	423	90.99%	11	97.40%	26.20	5	98.82%	20.92	5	98.82%	16.31
Sum of entire Lot (a.u.)		**117350**	**8247**	**-**	**195**	**-**	**-**	**142**	**-**	**-**	**88**	**-**	**-**
Mean of entire Lot (a.u.)		**-**	**329.88**	**92.97%**	**7.8**	**97.95%**	**27.37%**	**5.68**	**98.54%**	**23.21%**	**3.52**	**99.07%**	**17.46**
Fraction of entire Lot (ppm)		**-**	**70276**	**-**	**1661**	**-**	**-**	**1210**	**-**	**-**	**749.89**	**-**	**-**

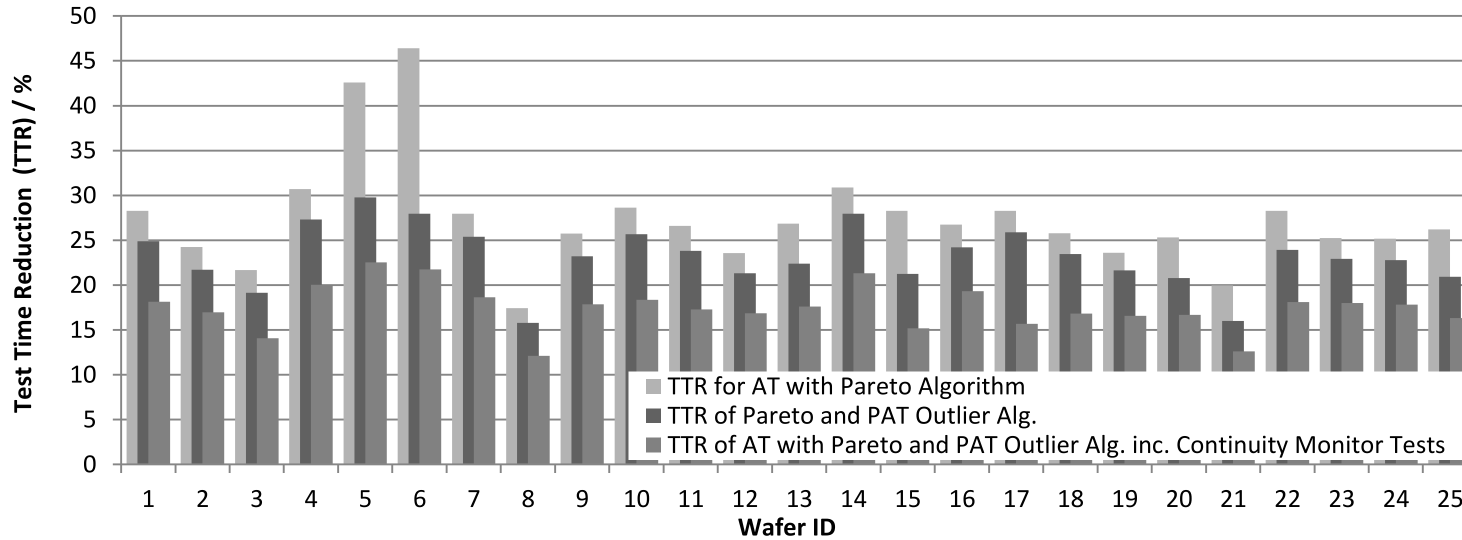

Figure 32: Comparison of Test Time Reductions for each Wafer of Product E for different AT Algorithm as well as AT with additionally Continuity Tests as Outlier Monitor Tests

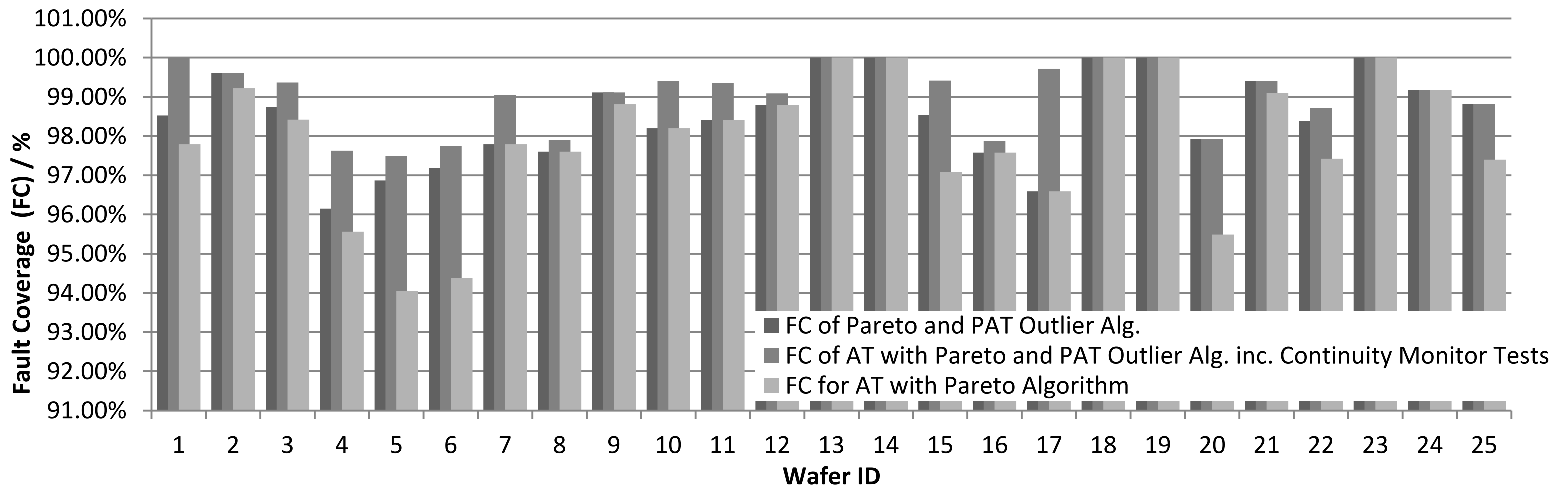

Figure 33: Comparison of Fault Coverage for each Wafer of Product E for different AT Algorithm as well as AT with additionally Continuity Tests as Outlier Monitor Tests

Table 30: **Product E: :** **Test Escapes and Fraction Defective Estimation and Validation of the Results by comparing with Test Data form Conventional Test for AT with Pareto and PAT Outlier Algorithm**

WaferID	Wafername	Percentage of Test Executions %	x_{sub}	$\hat{p}$	p_{wc}	$\hat{x}_{usub}$	$x_{wc,usub}$	x_{real}	$\hat{x}_{lot}$	$x_{wc,lot}$	x_{lot}	$\hat{p}_{AQL}$	$p_{AQL,wc}$	p_{AQL}
1	C25357W01PH0	84.81%	268	0.0638%	0.0706%	48	53	4	316	321	272	6.82%	6.93%	5.79%
2	C25357W02PC0	86.77%	257	0.0597%	0.0661%	39	43	1	296	300	258	6.38%	6.46%	5.50%
3	C25357W03PE3	89.12%	313	0.0711%	0.0781%	38	42	4	351	355	317	7.61%	7.69%	6.75%
4	C25357W04PG6	79.60%	325	0.0827%	0.0907%	83	91	13	408	416	338	8.85%	9.02%	7.20%
5	C25357W05PB6	83.38%	309	0.0751%	0.0825%	62	68	10	371	377	319	8.03%	8.17%	6.80%
6	C25357W06PE1	83.88%	346	0.0838%	0.0916%	66	73	10	412	419	356	8.97%	9.11%	7.58%
7	C25357W07PG4	84.65%	310	0.0741%	0.0814%	56	62	7	366	372	317	7.93%	8.05%	6.75%
8	C25357W08PB4	85.75%	326	0.0770%	0.0844%	54	59	8	380	385	334	8.24%	8.34%	7.12%
9	C25357W09PD7	84.38%	333	0.0799%	0.0875%	62	67	3	395	400	336	8.55%	8.67%	7.16%
10	C25357W10PB4	83.24%	328	0.0799%	0.0875%	66	72	6	394	400	334	8.55%	8.68%	7.12%
11	C25357W11PD7	85.73%	309	0.0729%	0.0801%	51	56	5	360	365	314	7.80%	7.90%	6.69%
12	C25357W12PG2	86.42%	327	0.0768%	0.0842%	51	56	4	378	383	331	8.22%	8.32%	7.05%
13	C25357W13PB2	85.75%	304	0.0716%	0.0787%	51	56	2	355	360	306	7.66%	7.78%	6.52%
14	C25357W14PD5	74.66%	283	0.0764%	0.0843%	96	106	9	379	389	292	8.18%	8.39%	6.22%
15	C25357W15PG0	88.93%	338	0.0770%	0.0842%	42	46	5	380	384	343	8.24%	8.32%	7.31%
16	C25357W16PB0	84.01%	322	0.0775%	0.0850%	61	67	8	383	389	330	8.29%	8.41%	7.03%
17	C25357W17PD3	83.55%	340	0.0824%	0.0901%	67	73	12	407	413	352	8.81%	8.94%	7.50%
18	C25357W18PF6	83.23%	344	0.0836%	0.0914%	69	76	6	413	420	350	8.94%	9.09%	7.46%
19	C25357W19PA6	85.96%	325	0.0764%	0.0838%	53	58	3	378	383	328	8.18%	8.28%	6.99%
20	C25357W20PF6	87.74%	282	0.0649%	0.0716%	39	43	6	321	325	288	6.94%	7.02%	6.14%
21	C25357W21PA6	90.62%	332	0.0742%	0.0813%	34	38	2	366	370	334	7.94%	8.02%	7.12%
22	C25357W22PD1	84.08%	305	0.0732%	0.0805%	58	64	5	363	369	310	7.83%	7.97%	6.60%
23	C25357W23PF4	84.76%	402	0.0959%	0.1042%	72	78	1	474	480	403	10.26%	10.39%	8.59%
24	C25357W24PA4	84.37%	359	0.0862%	0.0940%	67	73	3	426	432	362	9.22%	9.36%	7.71%
25	C25357W25PC7	88.17%	418	0.0968%	0.1049%	56	61	5	474	479	423	10.35%	10.46%	9.01%
Sum of entire Lot (a.u.)		**-**	**8105**	**-**	**-**	**1443**	**1581**	**142**	**9548**	**9686**	**8247**	**-**	**-**	**-**
Mean of entire Lot (a.u.)		**84.94%**	**324.2**	**0.08%**	**0.08%**	**57.73**	**63.24**	**5.68**	**381.93**	**387.44**	**329.88**	**8.27%**	**8.39%**	**7.03%**
Fraction of entire Lot (ppm)		**-**	**69067**	**-**	**-**	**12299**	**13473**	**1210**	**81366**	**82539**	**70277**	**-**	**-**	**-**

Table 31: Product E: : Test Escapes and Fraction Defective Estimation and Validation of the Results by comparing with Test Data form Conventional Test for AT with Pareto and PAT Outlier Algorithm and additionally Continuity Tests as PAT Outlier Monitor Tests

WaferID	Wafername	Percentage of Test Executions %	x_{sub}	$\hat{p}$	p_{wc}	$\hat{x}_{usub}$	$x_{wc,usub}$	x_{real}	$\hat{x}_{lot}$	$x_{wc,lot}$	x_{lot}	$\hat{p}_{AQL}$	$p_{AQL,wc}$	p_{AQL}
1	C25357W01PH0	88.44%	272	0.0621%	0.0686%	36	39	0	308	311	272	6.64%	6.72%	5.79%
2	C25357W02PC0	89.67%	257	0.0577%	0.0640%	30	33	1	287	290	258	6.18%	6.25%	5.50%
3	C25357W03PE3	91.79%	315	0.0695%	0.0763%	28	31	2	343	346	317	7.44%	7.50%	6.75%
4	C25357W04PG6	84.25%	330	0.0794%	0.0869%	62	68	8	392	398	338	8.49%	8.63%	7.20%
5	C25357W05PB6	87.66%	311	0.0719%	0.0790%	44	48	8	355	359	319	7.69%	7.78%	6.80%
6	C25357W06PE1	87.78%	348	0.0806%	0.0880%	48	53	8	396	401	356	8.62%	8.72%	7.58%
7	C25357W07PG4	88.22%	314	0.0720%	0.0791%	42	46	3	356	360	317	7.71%	7.79%	6.75%
8	C25357W08PB4	89.01%	327	0.0744%	0.0815%	40	44	7	367	371	334	7.96%	8.04%	7.12%
9	C25357W09PD7	88.01%	333	0.0767%	0.0839%	45	50	3	378	383	336	8.20%	8.30%	7.16%
10	C25357W10PB4	87.50%	332	0.0769%	0.0842%	47	52	2	379	384	334	8.23%	8.33%	7.12%
11	C25357W11PD7	89.15%	312	0.0708%	0.0777%	38	42	2	350	354	314	7.57%	7.66%	6.69%
12	C25357W12PG2	89.26%	328	0.0746%	0.0817%	39	43	3	367	371	331	7.98%	8.06%	7.05%
13	C25357W13PB2	88.79%	304	0.0692%	0.0760%	38	42	2	342	346	306	7.40%	7.48%	6.52%
14	C25357W14PD5	81.77%	289	0.0713%	0.0785%	64	71	3	353	360	292	7.62%	7.77%	6.22%
15	C25357W15PG0	91.88%	341	0.0752%	0.0822%	30	33	2	371	374	343	8.04%	8.11%	7.31%
16	C25357W16PB0	87.20%	323	0.0749%	0.0821%	47	52	7	370	375	330	8.01%	8.11%	7.03%
17	C25357W17PD3	91.08%	351	0.0780%	0.0852%	34	38	1	385	389	352	8.35%	8.42%	7.50%
18	C25357W18PF6	88.73%	346	0.0789%	0.0862%	44	48	4	390	394	350	8.44%	8.52%	7.46%
19	C25357W19PA6	89.41%	326	0.0737%	0.0808%	39	42	2	365	368	328	7.89%	7.96%	6.99%
20	C25357W20PF6	90.15%	282	0.0631%	0.0697%	31	34	6	313	316	288	6.75%	6.82%	6.14%
21	C25357W21PA6	92.63%	332	0.0726%	0.0795%	26	29	2	358	361	334	7.77%	7.83%	7.12%
22	C25357W22PD1	88.00%	306	0.0702%	0.0771%	42	46	4	348	352	310	7.51%	7.60%	6.60%
23	C25357W23PF4	88.42%	403	0.0922%	0.1001%	53	57	0	456	460	403	9.86%	9.95%	8.59%
24	C25357W24PA4	87.77%	359	0.0828%	0.0904%	50	55	3	409	414	362	8.86%	8.97%	7.71%
25	C25357W25PC7	90.75%	418	0.0940%	0.1019%	43	46	5	461	464	423	10.06%	10.13%	9.01%
Sum of entire Lot (a.u.)		-	***8159***	-	-	***1042***	***1142***	***88***	***9201***	***9301***	***8247***	-	-	-
Mean of entire Lot (a.u.)		***88.69%***	***326.36***	***0.07%***	***0.08%***	***41.66***	***45.68***	***3.52***	***368.02***	***372.04***	***329.88***	***7.97%***	***8.06%***	***7.03%***
Fraction of entire Lot (ppm)		-	***69527***	-	-	***8876***	***9732***	***750***	***78403***	***79259***	***70277***	-	-	-