DI Philipp Hütter, BSc

Printed Organic Electrochemical Transistors: Performance Parameters and Applications

DISSERTATION

zur Erlangung des akademischen Grades

Doktor der technischen Wissenschaften

eingereicht an der

Technischen Universität Graz

Betreuer

Ao.Univ.-Prof. DI Dr.techn. Karl Gatterer

Institut für Physikalische und Theoretische Chemie

Graz, August 2016

EIDESSTATTLICHE ERKLÄRUNG

Ich erkläre an Eides statt, dass ich die vorliegende Arbeit selbstständig verfasst, andere als die angegebenen Quellen/Hilfsmittel nicht benutzt, und die den benutzten Quellen wörtlich und inhaltlich entnommenen Stellen als solche kenntlich gemacht habe. Das in TUGRAZonline hochgeladene Textdokument ist mit der vorliegenden Dissertation identisch.

Datum

Unterschrift

Abstract

This thesis is focusing on an organic electronic device that has gained a lot of attention in the last decade, the organic electrochemical transistor or OECT. Investigated are the efficiency of the switching process of the transistor, the possibility to fabricate logic gates, different fabrication processes and the dependence of the transistor performance on its geometry.

To examine the OECT geometry/performance relationship entirely inkjet-printed devices are used, fabricated from only three different materials. Those simple devices are examined focusing on two key parameters of a transistor, the on-current and the on/off-current ratio, and how they depend on the transistor geometry. Geometry alterations concerning the dimension of the transistor channel but also the distance between gate electrode and channel are performed. The resulting transistors with optimized geometry are used to fabricate a basic building block of circuitry, an inverter, also entirely by inkjet-printing. To decrease the footprint of the transistor and monitor the influence of miniaturization on the device performance a hybrid inkjet-printing/nanoimprint-lithography fabrication process is developed. The resulting transistors, with feature sizes around 10µm, are used to fabricate inverters and also NAND gates. Based on these results more complex logic circuits are designed. Inverters, NAND gates, flipflops and also 2-bit shift registers are demonstrated, fabricated entirely by screen-printing and consisting of only five different materials. With the degree of complexity of these logic circuits, the excellent reproducibility of screen printed transistors and their usability for printed logic circuits is clearly demonstrated. Screen printed devices are also used for clarification concerning the electrochemical switching process in OECTs. By monitoring the current necessary to switch the transistor and examining it on a microscopic level, conclusions on the efficiency of this switching process are drawn. The obtained results contribute to a better understanding of the OECT and contribute to an optimization of design parameters for high performance OECTs.

Zusammenfassung

In dieser Arbeit liegt das Hauptaugenmerk auf dem organischen elektrochemischen Transistor (OECT), einem Bauteil der organischen Elektronik welchem im vergangenen Jahrzehnt viel Beachtung zuteilwurde. Im Zuge der Arbeit werden die Effizienz des Transistorschaltvorgangs, die Eignung für logische Schaltungen, verschiedene Herstellungsmöglichkeiten und der Zusammenhang zwischen Geometrie und Leistungsfähigkeit des Transistors untersucht.

Mittels Tintenstrahldruck werden OECTs hergestellt die aus nur drei verschiedenen Materialien bestehen. Sie werden für die Untersuchung des Zusammenhangs zwischen dem on-Strom sowie dem on/off Stromverhältnis und der Geometrie des Transistors verwendet. Veränderungen an der Geometrie des Transistors werden hinsichtlich der Abmessungen des Transistorkanals sowie dem Abstand zwischen Gate-Elektrode und dem Kanal vorgenommen. Aus diesen Untersuchungen gehen Transistoren mit optimierten Abmessungen hervor die für die Herstellung von Invertern verwendet werden. Diese Inverter sind ebenfalls vollständig durch Tintenstrahldruck hergestellt und stellen einen der Basisbausteine für logische Schaltungen dar. Basierend auf dem Herstellungsverfahren durch Tintenstrahldruck wird ein kombinierter Prozess aus Tintenstrahldruck und Nanoimprint-Lithographie entwickelt der eine Miniaturisierung der Transistoren erlaubt. Damit soll einerseits die benötigte Fläche für einen Transistor möglichst verkleinert werden und andererseits auch die Auswirkungen dieser Miniaturisierung auf die Leistungsfähigkeit der Transistoren untersucht werden. Des Weiteren werden diese Transistoren, deren Kanalbreiten im Bereich von 10 µm liegen, für die Herstellung von Invertern und auch von NAND Gattern verwendet. Hierbei gewonnene Erkenntnisse werden für die Planung von komplexeren Schaltungen wie Flipflops (bistabile Kippstufen) und 2-bit Schieberegistern eingesetzt. Diese Schaltungen werden mithilfe eines Siebdruckprozesses verwirklicht bei dem fünf verschiedene Materialien zum Einsatz kommen. Diese vollkommen siebgedruckten Schaltungen, die eine Komplexität aufweisen wie sie für OECTs zuvor noch nicht demonstriert wurde, belegen die herausragende Reproduzierbarkeit

von siebgedruckten OECTs und auch ihre Eignung für gedruckte organisch-elektronische Schaltkreise. Derselbe Siebdruckprozess wird auch herangezogen um OECTs herzustellen anhand derer der Schaltprozess der Transistoren genauer untersucht wird. Der Schaltstrom wird aufgezeichnet und mit den elektrochemischen Vorgängen im Kanal des Transistors in Zusammenhang gebracht. Damit lassen sich Rückschlüsse auf die Effizienz des Schaltprozesses ziehen. Dies trägt zu einem verbesserten Verständnis der organischen elektrochemischen Transistoren sowie zu einer weiteren Optimierung des Transistordesigns bei.

Acknowledgement

First of all I want to thank the heads of JOANNEUM RESEARCH – MATERIALS, Paul Hartmann and Georg Jakopic, for giving me the opportunity to write my thesis at this excellent research institution. I want to thank Barbara Stadlober for her supervision, for always sharing her tremendous amount of knowledge and for her endless patience. I also want to thank Thomas Rothländer for all of his support, for guiding me through the years of writing my master thesis and starting my PhD and for his moral support when things didn't go exactly as planned.

I want to thank Karl Gatterer for supervising this thesis. Without his support, his words of advice and his academic know-how this work would not have been possible.

I want to thank my parents for supporting me in all those years and giving me the opportunity to study. Of course my friends for always trying to keep my motivation high (and sometimes succeeding).

And most of all I want to thank you, Viki, for being there for me. I cannot express how much you mean to me.

Dissemination

Articles in peer reviewed journals, included in this thesis

Paper 1: P. C. Hütter, T. Rothländer, A. Haase, G. Trimmel, and B. Stadlober, "Influence of geometry variations on the response of organic electrochemical transistors," *Appl. Phys. Lett.*, vol. 103, no. 4, p. 043308, 2013.

Contribution: Majority of experimental work in close cooperation with T. Rothländer. Wrote the first draft and was involved in the final editing of the manuscript.

Paper 2: T. Rothländer, P. C. Hütter, E. Renner, H. Gold, A. Haase, and B. Stadlober, "Nanoimprint Lithography-Structured Organic Electrochemical Transistors and Logic Circuits," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1515–1519, 2014.

Contribution: Half of the experimental work. Minor contributions to the first draft and involved in the final editing of the manuscript.

Paper 3: P. C. Hütter, T. Rothländer, G. Scheipl, B. Stadlober, "All Screen Printed Logic Gates Based on Organic Electrochemical Transistors," *IEEE Trans. Electron Devices,* vol. 62, no. 12, pp. 4231-4236

Contribution: Majority of experimental work. Wrote the first draft and was involved in the final editing of the manuscript.

Paper 4: P. C. Hütter, A. Fian, K. Gatterer, B. Stadlober," Efficiency of the Switching Process in Organic Electrochemical Transistors," *ACS Appl. Mater. Interfaces*, vol. 8, no. 22, pp 14071–14076

Contribution: Majority of experimental work. Wrote the first draft and was involved in the final editing of the manuscript.

Further dissemination

conference proceeding: T. Rothländer, H. Gold, A. Haase, G. Jakopic, P. Hartmann, B. Stadlober, P. C. Hütter, Nanoimprinted Organic Electrochemical Transistors. *Proceedings of the Eurodisplay 2013*, pp. 179–180.

oral presentation: P. Hütter, T. Rothländer, H. Gold, G. Jakopic, P. Hartmann and B. Stadlober, *Geometry-Performance Relationship of Organic Electrochemical Transistors*, Regional Symposium on Electrochemistry South Eastern Europe, Ljubljana, May 2013

oral presentation: P. Hütter, T. Rothländer, H. Gold, A. Haase, W. Grogger, J. Kraxner, G. Jakopic, P. Hartmann and B. Stadlober, *Nanoimprinted Organic Electrochemical Transistors and Inverters,* International Conference on Organic Electronics, Grenoble, June 2013

oral presentation: P. C. Hütter, T. Rothländer, H. Gold, A. Haase, W. Grogger, J. Kraxner, G. Jakopic, P. Hartmann and B. Stadlober, *Nanoimprint Lithography Structured Organic Electrochemical Transistors and Logic Circuits,* International Symposium on Flexible Organic Electronics, Thessaloniki, July 2014

oral presentation: P. C. Hütter, T. Rothländer, H. Gold and B. Stadlober, *Nanoimprint Lithography Structured Organic Electrochemical Transistors,* DocDays and Summer School, Graz, July 2014

oral presentation: P. C. Hütter, T. Rothländer, G. Scheipl and B. Stadlober, *Fully printed 2-bit shift register based on organic electrochemical transistors,* SPIE Optics and Photonics, San Diego, August 2015

poster presentation: P. C. Hütter, T. Rothländer, G. Scheipl and B. Stadlober, *Fully printed 2-bit shift register based on organic electrochemical transistors,* International Winterschool on Bioelectronics, Kirchberg in Tirol, March 2015

poster presentation: P. C. Hütter, A. Fian, K. Gatterer, B. Stadlober, *Screen printed organic electrochemical transistors: basics and applications,* International Winterschool on Bioelectronics, Kirchberg in Tirol, March 2016

List of Abbreviations

γ	Doping Level
μ	Charge Carrier Mobility
ρ	Density
σ	Conductivity
τ	Time Constant (at transient state transistor model)
A	Activity
A_G	Active Area on Gate Electrode
A_{SD}	Active Area on Source-Drain Electrode
c	Charge Carrier Concentration
$CaCl_2$	Calcium Chloride
CF_4	Tetrafluoromethane
E	Electrode Potential
e^-	Electron
E^0	Standard Electrode Potential
EPR	Electron Paramagnetic Resonance Spectroscopy
F	Faraday Constant
f	Constant of Proportionality (at transient state transistor model)
G	Gap between Gate and Source-Drain Electrode
I_D, I_{DS}	Drain-Current
I_G, I_{GS}	Gate-Current
$I_{G,max}$	Maximum Switching Current

I_{OFF}	OFF-Current
I_{ON}	ON-Current
I_{ON}*	ON-Current normalized on real line width
Ion, calc*	ON-Current (calculated from the linear part of the I(V) curve)
I_{ON}/I_{OFF}	ratio between ON- and OFF-Current
IPA	Isopropyl Alcohol
I_{SS}	Steady State Source-Drain Current
ΔI_{SS}	Difference between the Source-Drain Current at 0V Gate Voltage and the Source-Drain Current when V_g is applied
J(x)	Current Flux
L	Width of the Electrolyte Line on the Source-Drain Electrode
M	Molecular Weight
M^+	Mobile Cation
m_A	Electrochemically Active Mass of PEDOT Present in the Transistor Channel
m_C	Total Mass of PEDOT Present in the Transistor Channel
MEC	Maximum Equal Criteria
n	Number of Transferred Electrons
NAND	Not And – Logic Gate
NIL	Nanoimprint-Lithography
NOR	Not Or – Logic Gate
OECT	Organic Electrochemical Transistor
OTFT	Organic Thin Film Transistor
p_0	Hole Density
PEDOT	Poly(ethylenedioxithiophene)
PEDOT:PSS	Poly(ethylenedioxithiophene):poly(styrenesulphonate)
PET	Polyethyleneterephthalat

q	Elementary Charge
Q	Turn-off Charge of OECT
R	Ideal Gas Constant
R_{OFF}	OFF-Resistance of OECT
R_{ON}	ON-Resistance of OECT
Rs	Sheet Resistance
S-D	Source-Drain
SF_6	Sulfur Hexafluoride
T	Thickness of Electrodes
T^0	Absolute Temperature
t_{Off}	Time to Switch Inverter Off
t_{On}	Time to Switch Inverter On
UV-Vis-NIR	Ultraviolet-Visible-Near Infrared
V_D, V_{DS}	Drain-Voltage
$+V_{DD}$	Positive Supply Voltage at Inverter
$-V_{DD}$	Negative Supply Voltage at Inverter
V_G, V_{GS}	Gate-Voltage
V_{IN}, V_{Input}	Input Voltage
V_{ol}	PEDOT:PSS Channel Volume
V_{OUT}, V_{Output}	Output Voltage
$V_{OUT,HIGH}$	High Level Voltage of Inverter
$V_{OUT,LOW}$	Low Level Voltage of Inverter
V_p	Pinch-off Voltage
VRH	Variable Range Hopping
W	Width of the Source-Drain Electrode
wt. %	Weight Percent

$\overline{x}_{HIGH}$	Arithmetic Mean Value of the High Level
$\overline{x}_{LOW}$	Arithmetic Mean Value of the Low Level
z	Charge Number

List of Figures

Contents

I Introduction

This chapter is providing a short overview on the advantages of organic electronics as well as a brief summary on the motivation for using printed organic electronics. Additionally the aim of this thesis is described. The state of the art of this field is outlined, pointing out the research tasks that have been pursued in the course of this work.

1. Motivation

1.1 Why Printed Organic Electronics

Organic electronics experienced a remarkable development over the past decades, starting from the first transistors in 1986 [1], light emitting diodes [2] and photovoltaic cells [3]. Stimulus for the research activities were both academic and economic interests. Astonishing results have been obtained, leading to high performing organic thin film transistors [4], flexible or even stretchable electronics [5], flexible displays [6], biocompatible and biodegradable electronics [7] and smart textiles [8], to name just a few. Some technologies even made their way into commercially available products, like bendable TV-screens or bended smartphone displays containing organic light emitting diodes [9,10]. In those applications one of the key advantages of organic electronics compared to conventional silicon based electronics, which is the possible use of large area flexible substrates, plays an important role. And this is only one of the many positive features this technology is offering. The utilized materials are to a large extent biocompatible, enabling in-vivo sensing applications difficult to achieve with classical electronics. They also demand only moderate process conditions (low temperature, non-hazardous chemicals), allowing for environmentally sustainable fabrication routines. Finally, they are obtainable from solution, making them perfectly suitable for processing by printing techniques. And those printing techniques, with their large area, high throughput, and flexible substrate fabrication routines are responsible for many of the advantages organic electronics has compared to classical electronics. Hence printed organic electronics are a rewarding target of research.

1.2 Aim of this Work/State of the Art

There are two main types of organic electronic transistors; the field effect transistor and the electrochemical transistor. While the field effect transistor has been studied in depth, advanced understanding of the organic electrochemical transistor (OECT) is still nascent. To make a contribution to this ongoing research the focus of this thesis is on the OECT, more precisely on the understanding of influences on the transistor behavior, on the possibility of creating logic circuits based on those transistors and on suitable simple fabrication methods.

The last objective was targeted using different printing methods, namely inkjet-printing and screen-printing. To keep the fabrication routine as simple as possible the entire transistors, or even the entire circuits based on those transistors, should be fabricated using solely one printing method. Simplified this task can be described as the structuring of the transistors

electrodes and its electrolyte. The possibility to fabricate organic electrochemical transistors with the aid of printing processes has already been demonstrated in literature. To the best of our knowledge only one group demonstrated OECTs that are entirely inkjet-printed [11] at the time this thesis was stared in 2012. A modified desktop printer was used in this work, focusing on the evaluation of their fabrication method concerning functional devices on foil and on photo-paper substrates. In the meantime (2014) another group demonstrated entirely inkjet-printed devices, indicating that this is still a valuable research target [12]. Others used inkjet-printing to structure the PEDOT:PSS electrodes of lateral OECTs, serving as the bottom layer for a drop of electrolyte applied on top by hand [13-15]. Inherently the geometry of those transistors is less defined compared to entirely printed transistors. A small number of research groups also used screen printing for the fabrication of organic electrochemical transistors. Transistors utilizing screen printed electrodes, consisting of PEDOT:PSS and a highly conducting inert material, and an electrolyte deposited by stencil printing, a process demanding a layer of UV-curable material in addition to the materials needed for the functionality of the transistor, were demonstrated [16]. A different approach based on screen-printing was pursued by Nilsson et al.: A deactivation material was printed onto an unstructured layer of PEDOT:PSS, over-oxidizing the exposed PEDOT:PSS and thereby structuring the electrodes. This process, somehow contradicting the additive approach of printing, was finalized by a printed electrolyte layer [17]. Also a combinatory six-step process for the fabrication of an active-matrix physical sensor circuit utilizing OECTs, comprising inkjet-printing as well as screen-printing steps, has been reported [18]. A rather extravagant printing process using flexography to structure the PEDOT:PSS electrodes on top of a structured ion conducting membrane was also demonstrated. The resulting devices use the electrolyte as the substrate and exhibit an “inverted” transistor structure, with the electrodes applied on top of the electrolyte, both being uncommon features for OECTs [19].Another extravagant type of OECTs is formed by fibers covered in PEDOT:PSS that are connected by a drop of electrolyte[20]. A more common fabrication method is based on xurography or razor writing using a cutting plotter. This method can be used to structure the electrodes by cutting an unstructured layer of PEDOT:PSS, or by cutting defined structures into plastic foils to create masks (for defining the electrolyte area or the electrode area) or a combination of both. Using this method at least one subsequent step of spin-coating or printing is inevitable [21-25]. Another field of fabrication techniques is based on photolithography and can roughly be divided in two groups: (i) Photolithography is used to structure the PEDOT:PSS electrodes and subsequent steps are necessary to structure the electrolyte. These steps involve another photolithography step to

create a well defining the electrolyte area, micro molding or printing [17, 20, 26, 27]. (ii) A multi-step photolithography process is used to structure metal electrodes and define areas for the semiconductor and also for the electrolyte. This process involves metal deposition, spin coating, dry etching and developing steps, making it very complex but yielding transistors with very small dimensions [28-33]. All in all a large variety of fabrication techniques is possible, with most of them including subtractive steps, vacuum processes, wet or dry etching, sophisticated equipment or a combination of different structuring methods. For that reason the demonstration of a simple fabrication process for OECTs is considered an important research task.

This fabrication process should then be used to demonstrate logic circuits based on OECTs, also entirely fabricated by a single manufacturing technique. Logic gates have been reported in the literature, including inverters, ring oscillators and also NOR and NAND gates [11, 20, 23]. To the best of our knowledge no one has ever demonstrated any logic circuit more complex than this. These complex circuits would increase the amount of possible applications for OECTs tremendously as not only simple switching but also more sophisticated tasks could be mastered. But these circuits demand a large number of transistors performing uniformly. Pronounced variations of the transistor performance would lead to malfunction of the circuit. Consequently working circuits would demonstrate the high uniformity achievable by printing methods. The large number of transistors can also be used to evaluate the deviation of transistor to transistor performance statistically. Until now there is only one other study examining the deviation of the transistors on-resistance for photo lithographically structured OECTs [32].But not only the printed transistors are of interest. Passive circuit elements, like resistors, capacitive and inductive structures, printed in a uniform manner are attractive as well [34]. So statistically evaluating the large number of resistors also needed in the printed circuits is another valuable research task.

When planning a circuit, knowing the characteristics of a single device is of advantage. This is one of the major goals; to understand the influence of the transistor geometry on the device performance. Additionally the basic understanding of the switching process should be enhanced. At the time the work for this thesis started not much information concerning this topic was to be found in literature. Two research groups examined the influence of the gate area to channel area ratio, with one group focusing on the transistor behavior [15] and the other on the sensitivity when the transistor serves as a sensor [29]. How the electrode dimensions alter the switching speed of the transistor was examined by another group using

photolithography structured devices [32]. During the time this thesis was realized other studies were published, one evaluating the influence of the channel thickness on the transistor performance to optimize the transistors for sensing applications [35] and the other examining the channel thickness effect on the on/off ratio of the transistor [36]. How to tune the channel geometry in order to obtain transistors with optimized performance was the target of another research paper published [37], confirming that this is a topic of major interest.

With this thesis contributions to a deeper understanding of the OECT features, both the switching process and the parameters influencing the transistor performance are provided. This work will also enhance the predictability when designing a very promising organic electronic device for circuitry as well as many other applications, the Organic Electrochemical Transistor.

References

[1] A. Tsumura, H. Koezuka, T. Ando, Macromolecular electronic device: Field-effect transistor with a polythiophene thin film. *Appl. Phys. Lett.* 1986, *49*, 1210.

[2] C. W. Tang, S. A. Vanslyke, Organic electroluminescent diodes. *Appl. Phys. Lett.* 1987, *51*, 913.

[3] C. W. Tang, Two-layer organic photovoltaic cell. *Appl. Phys. Lett.* 1986, *48*, 183.

[4] H. Sirringhaus, 25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon. *Adv. Mater.* 2014, *26*, 1319–1335.

[5] T. Sekitani, T. Someya, Stretchable, Large-area Organic Electronics. *Adv. Mater.* 2010, *22*, 2228–2246.

[6] L. Zhou, S. Park, B. Bai, J. Sun, S. C. Wu, T. N. Jackson, S. Nelson, D. Freeman, Y. Hong, Pentacene TFT driven AM OLED displays. *IEEE Electron Device Lett*. 2005, *26*, 640.

[7] M. Irimia-Vladu, P. A. Troshin, M. Reisinger, L. Shmygleva, Y. Kanbur, G. Schwabegger, M. Bodea, R. Schwödiauer, A. Mumyatov, J. W. Fergus, V. F. Razumov, H. Sitter, N. S. Sariciftci, S. Bauer, Biocompatible and Biodegradable Materials for Organic Field-Effect Transistors. *Adv. Funct. Mater.* 2010, *20*, 4069.

[8] K. Cherenack, L. van Pieterson, Smart textiles: Challenges and opportunities. *J. Appl. Phys*. 2012, *112*, 091301.

[9] http://gizmodo.com/samsung-galaxy-s6-edge-a-quirk-that-doesnt-really-work-1694821006, visited 02.06.2016.

[10] http://gizmodo.com/samsung-made-a-105-inch-bendy-uhd-tv-because-why-not-1677581763#_ga=1.41903842.1366711378.1442769390, visited 02.06.2016.

[11] R. Mannerbro, M. Ranlof, N. Robinson, R. Forchheimer, Inkjet printed electrochemical organic electronics. *Synth. Met.* 2008, *158,* 556–560

[12] R. Faddoul, R. Coppard and T. Berthelot, Inkjet printing of organic electrochemical immunosensors. *IEEE SENSORS 2014 Proceedings* 2014, pp. 1088-1091.

[13] L. Basiricò, P. Cosseddu, B. Fraboni, A. Bonfiglio, Inkjet printing of transparent, flexible, organic transistors. *Thin Solid Films* 2011, *520*, 1291–1294.

[14] M. Demelas, E. Scavetta, L. Basiricò, R. Rogani, and A. Bonfiglio, A deeper insight into the operation regime of all-polymeric electrochemical transistors. *Appl. Phys. Lett.* 2013, *102*, 193301.

[15] L. Basiricò, P. Cosseddu, A. Scidà, B. Fraboni, G.G. Malliaras, A. Bonfiglio, Electrical characteristics of ink-jet printed, all-polymer electrochemical transistors. *Org. Electron.* 2012, *13,* 244–248.

[16] P. Andersson Ersman, D. Nilsson, J. Kawahara, G. Gustafsson, M. Berggren, Fast-switching all-printed organic electrochemical transistors. *Org. Electron.* 2013, *14*, 1276–1280.

[17] D. Nilsson, M. Chen, T. Kugler, T. Remonen, M. Armgarth, M. Berggren, Bi-stable and Dynamic Current Modulation in Electrochemical Organic Transistors. *Adv. Mater*. 2002, *14*, 51-54.

[18] M. Zirkl, A. Sawatdee, U. Helbig, M. Krause, G. Scheipl, E. Kraker, P. Andersson Ersman, D. Nilsson, D. Platt, P. Bodö, S. Bauer, G. Domann, B. Stadlober, An All-Printed Ferroelectric Active Matrix Sensor Network Based on Only Five Functional Materials Forming a Touchless Control Interface. *Adv. Mater*. 2011, *23,* 2069–2074.

[19] N. Kaihovirta, T. Mäkelä, X. He, C. Wikman, C.-E. Wilén, R. Österbacka, Printed all-polymer electrochemical transistors on patterned ion conducting membranes. *Org. Electron.* 2010, *11*, 1207-1211.

[20] M. Hamedi, R. Forchheimer, O. Inganäs, Towards woven logic from organic electronic fibres. *Nat. Mater*. 2007, *6*, 357-362.

[21] P. Tehrani, I. Engquist, N. D. Robinson, D. Nilsson, M. Robertsson, M. Berggren, Printable organic electrochemical circuit to record time–temperature history. *Electrochim. Acta* 2010, *55*, 7061-7066

[22] S. Kanakamedala, H. T. Alshakhouri, .l Agarwal, M. A. DeCoster, A simple polymer based electrochemical transistor for micromolar glucose sensing. *Sens. Actuators B: Chemical* 2011, *157*, 92-97

[23] D. Nilsson, N. Robinson, M. Berggren, R. Forchheimer, Electrochemical Logic Circuits. *Adv. Mater.* 2005, *17,* 353–358.

[24] D. Tu, D. Nilsson, R. Forchheimer, Electrochromic Electrochemical Transistors Gated With Polyelectrolyte-Decorated Amyloid Fibrils. *Journal of Display Technology* 2013, *9*, 755-759.

[25] P. Andersson, R. Forchheimer, P. Tehrani, M. Berggren, Printable All-Organic Electrochromic Active-Matrix Displays. *Adv. Funct. Mater*. 2007, *17*, 3074–3082.

[26] P. O. Svensson, D. Nilsson, R. Forchheimer, M. Berggren, A sensor circuit using reference-based conductance switching in organic electrochemical transistors. *Appl. Phys. Lett.* 2008, *93*, 203301.

[27] J. T. Mabeck, J. A. DeFranco, D. A. Bernards, G. G. Malliaras, S. Hocdé, C. J. Chase, Microfluidic gating of an organic electrochemical transistor. *Appl. Phys. Lett*. 2005, *87*, 013503.

[28] G. Tarabella, C. Santato, S. Y. Yang, S. Iannotta, G. G. Malliaras, F. Cicoira, Effect of the gate electrode on the response of organic electrochemical transistors. *Appl. Phys. Lett*. 2010, *97*, 123304.

[29] F. Cicoira, M. Sessolo, O. Yaghmazadeh, J. A. DeFranco, S. Y. Yang, G. G. Malliaras, Influence of Device Geometry on Sensor Characteristics of Planar Organic Electrochemical Transistors. *Adv. Mater*. 2010, *22*, 1012–1016.

[30] G. Tarabella, G. Nanda, M. Villani, N. Coppedè, R. Mosca, G. G. Malliaras, C. Santato, S. Iannotta, F. Cicoira, Organic electrochemical transistors monitoring micelle formation, *Chem. Sci.* 2012, *3*, 3432-3435.

[31] J. A. DeFranco, B. S. Schmidt, M. Lipson, G. G. Malliaras, Photolithographic patterning of organic electronic materials. *Org. Electron*. 2006, *7*, 22–28.

[32] D. Khodagholy, M. Gurfinkel, E. Stavrinidou, P. Leleux, T. Herve, S. Sanaur, G. G. Malliaras, High speed and high density organic electrochemical transistor arrays. *Appl. Phys. Lett.* 2011, *99*, 163304.

[33] D. Khodagholy, J. Rivnay, M. Sessolo, M. Gurfinkel, P. Leleux, L. H. Jimison, E. Stavrinidou, T. Herve, S. Sanaur, R. M. Owens, G. G. Malliaras, High transconductance organic electrochemical transistors. *Nat. Commun*. 2013, *4*, 2133.

[34] A. E. Ostfeld, I. Deckman, A. M. Gaikwad, C. M. Lochner, A. C. Arias, Screen printed passive components for flexible power electronics. *Sci. Rep.* 2015, *5*, 15959.

[35] J. Rivnay, P. Leleux, M. Ferro, M. Sessolo,' A. Williamson, D. A. Koutsouras, D. Khodagholy, M. Ramuz, X. Strakosas, R. M. Owens, C. Benar, J.-M. Badier, C. Bernard, G. G. Malliaras, High-performance transistors for bioelectronics through tuning of channel thickness. *Sci. Adv*. 2015, *1,* e1400251.

[36] P. Kumar, Z. Yi, S. Zhang, A. Sekar, F. Soavi, F. Cicoira, Effect of channel thickness, electrolyte ions, and dissolved oxygen on the performance of organic electrochemical transistors. *Appl. Phys. Lett*. 2015, *107*, 053303.

[37] J. Rivnay, P. Leleux, M. Sessolo,D. Khodagholy, T. Hervé, M. Fiocchi, G. G. Malliaras, Organic Electrochemical Transistors with Maximum Transconductance at Zero Gate Bias. *Adv. Mater*. 2013, *25*, 7010–7014.

II Fundamentals

In the following section some fundamentals concerning the organic electrochemical transistor are presented. What is the base of the transistors functionality, what materials are used and what are their properties, how does an OECT work, what are possible designs and which design rules need attention, how to build a logic circuit using OECTs? Those questions will be answered in the following chapter.

2. OECT, Basic Principles

Although both, the organic field effect transistor (OFET) and the organic electrochemical transistor (OECT), are organic electronic devices, utilizing organic semiconductors as active materials and amplify or switch electronic signals, their working principles are differing significantly. The organic field effect transistor OTFT is driven by an electric field and the transition between the on- and the off- state is a matter of charge carriers accumulated just below the surface of an organic semiconductor in contact with an insulator. The OECT, on the other hand, is driven by an electrostatic potential and instead of an insulator the organic semiconductor is in direct contact with an ion conducting material. And most prominently, not only the surface but the whole volume of the organic semiconductor is involved in the switching process between the on- and the off-state. Switching is a result of modifying the conductivity of the bulk of the material. With the conductivity being proportional to the concentration of charge carriers c and their respective mobility μ (eq.2.1), there are two alterable factors present enabling modification.

$$\sigma \propto \mu * c \qquad \text{(Eq.2.1)}$$

It is suggested that the hole mobility μ decreases as there are ions injected into the bulk of the semiconductor. In this way the hole tunneling is disrupted, which can contribute to the change of conductivity [1]. For semiconductors used in OECTs the second mechanism, the change of the charge carrier concentration c, is of greater interest. Due to a reversible redox reaction, the semiconductor is switched between a doped state, where a large number of charge carriers is available (conducting state), and a de-doped state, where a very small number of charge carriers is available (non-conducting state) [1]. Like this a precise alteration of the conductivity is possible, of course under the prerequisite of a semiconductor material capable of reversible doping and de-doping via a redox reaction.

In the history of OECTs, starting in 1984 with H. S. White et al. [2], a variety of materials have been used that meet this requirement. The mentioned transistors of White et al. where fabricated using Polypyrrole as their organic semiconductor. Most commonly used semiconductors for the devices implemented in the following decades are Poly(3-Methylthiophene) [3], Polyaniline [4], Polycarbazole [5] and also Polypyrrole [6]. To the best of our knowledge it was in 2002 by D. Nilsson et al. [7] that the first organic electrochemical transistors utilizing PEDOT:PSS were demonstrated to work, the material of choice for most of the recently implemented OECTs.

PEDOT:PSS was first synthesized at Bayer AG in the 1980s. The derivative of polythiophene, poly(ethylenedioxithiophene), is doped with poly(styrenesulphonate) to form PEDOT:PSS. This chemical doping takes place during the polymerization process, resulting in a water soluble organic semiconductor capable of forming highly conductive films (10 S/cm) with excellent stability [8]. Initially designed for antistatic coatings in photographic films its potential for new applications was soon recognized [8]. To adopt the material properties for a wide range of applications, efforts were taken to increase the conductivity, resulting in PEDOT:PSS films exhibiting a conductivity of more than 3000 S/cm. To the best of our knowledge these films, treated with sulfuric acid and used as transparent electrodes for optoelectronic devices [9], mark the highest conductivity achieved for PEDOT:PSS. Its primary structure is shown in figure 2.1a, with the PEDOT drawn in blue and the PSS drawn in black. As depicted both polymers are present in their charged state. The secondary structure is shown in figure 2.1b. Small segments of PEDOT with a molecular weight of 1500 to 2500 g/mol are interacting with the long PSS chain, having a molecular weight of around 400000 g/mol [10]. Sections of the chain with linear conformation (as depicted in figure 2.1b) alternate with sections with coiled conformation [11]. Colloidal gel particles of several PEDOT:PSS chains, with the PEDOT located preferably in the particle center and enclosed by hydrophilic PSS chains, are suggested for the tertiary structure [12].These grains interact with each other to form the quaternary structure and the conductive bulk material [12].

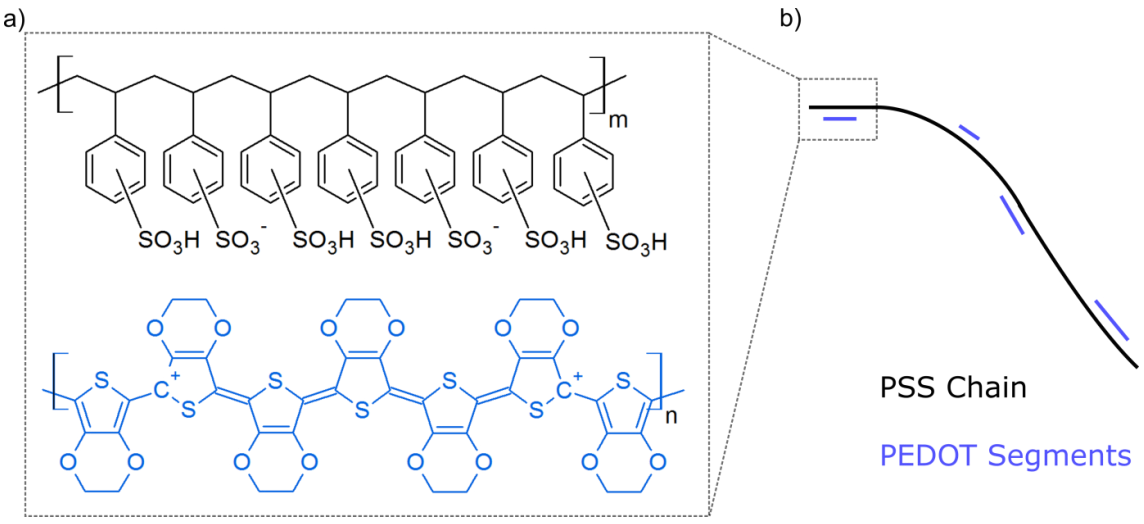


Figure 2.1: a) primary structure of PEDOT:PSS b) secondary structure of PEDOT:PSS (adapted from [10])

The conductivity of PEDOT:PSS, with PEDOT being p-doped, is based on the transport of holes in the material. The actual charge carriers are denoted as polarons and bipolarons [13]. In the neutral, de-doped form none of these charge carriers is present on a PEDOT segment. The

thiophene rings exhibit the aromatic configuration and the band gap between the valence band and the conductive band is too high to allow for a thermal excitation of a significant amount of charge carriers, resulting in a very poor conductivity. The allowed transition is indicated as black arrow in the band diagram in figure 2.2a. Upon withdrawal of one electron, a polaron is formed. This polaron consists of a positive charge as well as an unpaired electron present on the PEDOT segment. Both are marked in figure 2.2b, as well as the unpaired electron also highlighted in the band diagram in figure 2.2b. Additionally the double bond configuration is partially changed from the aromatic to the quinoid form, stabilized by the polaron. Due to the change in structure and charge of the polymer chain also the band structure is modified. With the formation of electronic levels inside the band gap energy barriers for excitation are lowered, resulting in an increased conductivity [14]. The allowed transitions are marked as black arrows in the band diagram in figure 2.2b. Bipolaron formation can be achieved in two ways; either two polarons in close proximity combine or a polaron gets further oxidized. Both cases result in a PEDOT segment carrying two positive charges, as marked in figure 2.2c. Similar to a polaron the double bonds configuration is partially changed to the quinoid form and the band structure is altered by formation of electronic levels inside the band gap. The result is enhanced conductivity [14]. Both of the described charge carrying structures are likely to be present in PEDOT:PSS. To examine which one is predominant, two useful characterization methods are at hand as they exploit intrinsic differences between polarons and bipolarons. First is electron paramagnetic resonance spectroscopy (EPR), exploiting the fact that polarons have a spin (due to the unpaired electron present after oxidation) while bipolarons are spinless. As EPR detects only species having a spin a statement can be made which type of charge carrier is predominant [15]. Second are UV-Vis-NIR measurements. Here the different chemical structures and band structures result in a differing absorption behavior. As indicated by the allowed transitions highlighted in the band diagrams of PEDOT in its three different oxidation states, excitations demand different energy. That energy is proportional to the allowed transitions and reflected by different absorption peaks in the spectra for undoped PEDOT, PEDOT carrying a polaron and PEDOT carrying a bipolaron. Using those measurements the relation between the two charge carrying structures is possible [16]. The mechanism proposed for the transport of the charge carriers is variable range hopping (VRH), as indicated by the temperature dependence of the PEDOT:PSS resistance that can be fitted with this model very well [17]. The VRH model describes the possibility for charges to hop short distances with high activation energies or long distances with low

activation energies. In this way a charge transport along the different polymer chains is possible. For more details we refer the reader to the original literature [18].

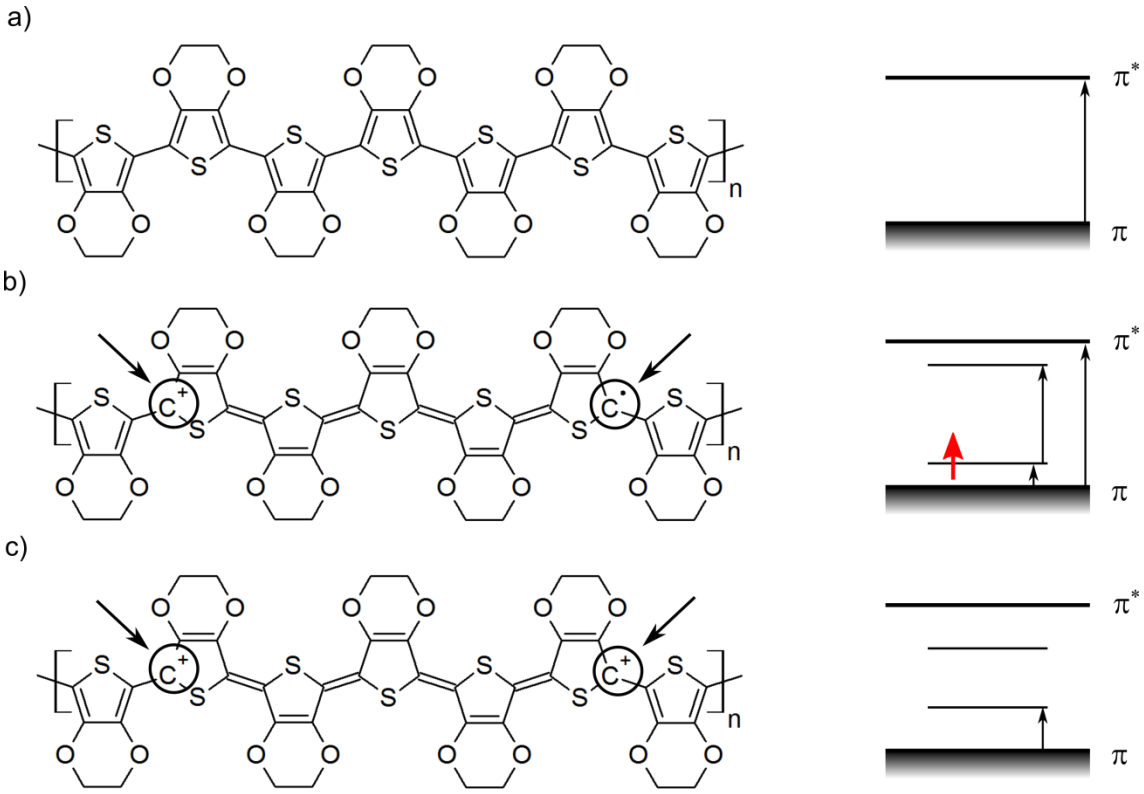


Figure 2.2: chemical structure and band diagram of a) undoped PEDOT b) PEDOT carrying a polaron c) PEDOT carrying a bipolaron. In the band diagrams the allowed transitions are marked with black arrows and the unpaired electron is marked with a red arrow.

3. OECT, Working Principle

As described in the previous section PEDOT:PSS is capable of being switched between a conducting state, with PEDOT in its oxidized form, and a non-conducting state, with PEDOT in its neutral form. The process of switching is achieved by electrochemical doping and de-doping and represented by the following equation [7].

$$PEDOT^+:PSS^- + M^+ + e^- \leftrightarrow PEDOT^0 + M^+:PSS^- \qquad \text{(Eq 3.1)}$$

In this equation the two states of PEDOT are present; the oxidized state $PEDOT^+$ coordinated to the PSS^- and the neutral state $PEDOT^0$. Switching between these two states is achieved by applying a voltage to the PEDOT:PSS while it is in contact with an electrolyte containing mobile

cations. The e^- in the equation represents the transferred electrons and the M^+ represents the mobile cations. To describe the functionality of OECTs Nilsson suggested two basic configurations of arranging PEDOT:PSS and the electrolyte, the bi-stable and the dynamic configuration. Chapter 3.1 is based on his work [7, 19].

3.1 Basic Configurations

3.1.1 Dynamic Configuration

In this configuration there is one electrode of PEDOT:PSS in contact with an electrolyte (compare fig 3.1a). When a constant voltage is applied the PEDOT:PSS gets de-doped at the negative biased side of the electrode. $PEDOT^+$ is taking up one electron and is reduced to $PEDOT^0$. The negative charge at the PSS^- is balanced by a mobile cation M^+ from the electrolyte that is transported into the bulk PEDOT:PSS via the electrolyte/electrode interface. At the positive biased side of the electrode the reactions is running in the opposite direction and PEDOT:PSS gets doped. An electron is removed from $PEDOT^0$, oxidizing it to $PEDOT^+$. That positive charge is balanced by the PSS^- present in the bulk material. As transport of M^+ at the negative biased side from the electrolyte into the electrode leads to a local depletion of M^+, a flow of cations is induced due to diffusion, inducing a migration of M^+ at the positive biased side from the electrode back into the electrolyte. In this configuration equilibrium is obtained with a doping degree gradient in the electrode reaching from de-doped at the negative biased side to doped at the positive biased side. Removing the voltage leads to resolving of this gradient as the reduced and oxidized areas are in direct contact with each other, giving this configuration its name. When the applied voltage is increased no equilibrium state is generated. At low negative voltages an electronic current corresponding to ohms law is flowing in the electrode that is increasing linearly with the applied voltage. At a certain voltage a critical concentration of de-doped non-conducting $PEDOT^0$ at the negative biased side of the electrode is reached. The resistance at the very end of the electrode (a few hundred nanometer) is very high in comparison to the rest of the electrode, so almost all of the potential drops over this area [20]. When increasing the voltage the only result is a higher potential drop at this area. As a consequence the current is saturating and becoming independent of the applied voltage, the so called pinch-off is reached (depicted in the characteristics in fig 3.1d at $V_2 = 0V$).

3.1.2 Bi-stable Configuration

The bi-stable configuration, depicted in figure 3.1b is formed by two separated electrodes of PEDOT:PSS that are connected solely by an electrolyte. When a voltage is applied electrochemical doping is the result. The electrode reactions are the same as described before in the dynamic configuration. The reduction at the negative biased electrode forces cations from the electrolyte into the electrode material. At the same time the oxidation at the positive biased electrode releases cations able to move from the electrode into the electrolyte. With the voltage applied an ionic current of cations is flowing between the two electrodes. The higher the applied voltage, the bigger is the driving force for the reduction as well as for the oxidation. The ionic current is intensified and the redox reaction rates are enhanced. When the voltage is removed, both electrodes stay in their reduced/oxidized state for a considerable time as the recombination depends on the diffusion of cations, giving this configuration its name.

3.1.3 Combined Configuration

When combining the two configurations described above a combination of their characteristics is achieved (compare figures 3.1c and 3.1d). The PEDOT:PSS electrode covered with an electrolyte and with a voltage V_1 applied at its ends, denoted before as dynamic configuration, is now connected with a second PEDOT:PSS electrode. This connection is accomplished solely by an electrolyte, which is the key attribute of the bi-stable configuration. If only the voltage V_1 is applied, same behavior as observed before is accomplished. Increasing V_1 leads to a linear increase of the current I_1 until the pinch-off voltage is reached and the current saturates. If a second voltage V_2 is applied and this voltage is positive then the driving force for the reduction at the negative biased end of the first electrode is increased. This intensified reduction results in a pinch-off of the first electrode occurring at a lower voltage V_1. The higher the voltage V_2 the earlier pinch-off is achieved. Like this it is possible to control the voltage/current characteristics of one electrode using a voltage applied to a second electrode.

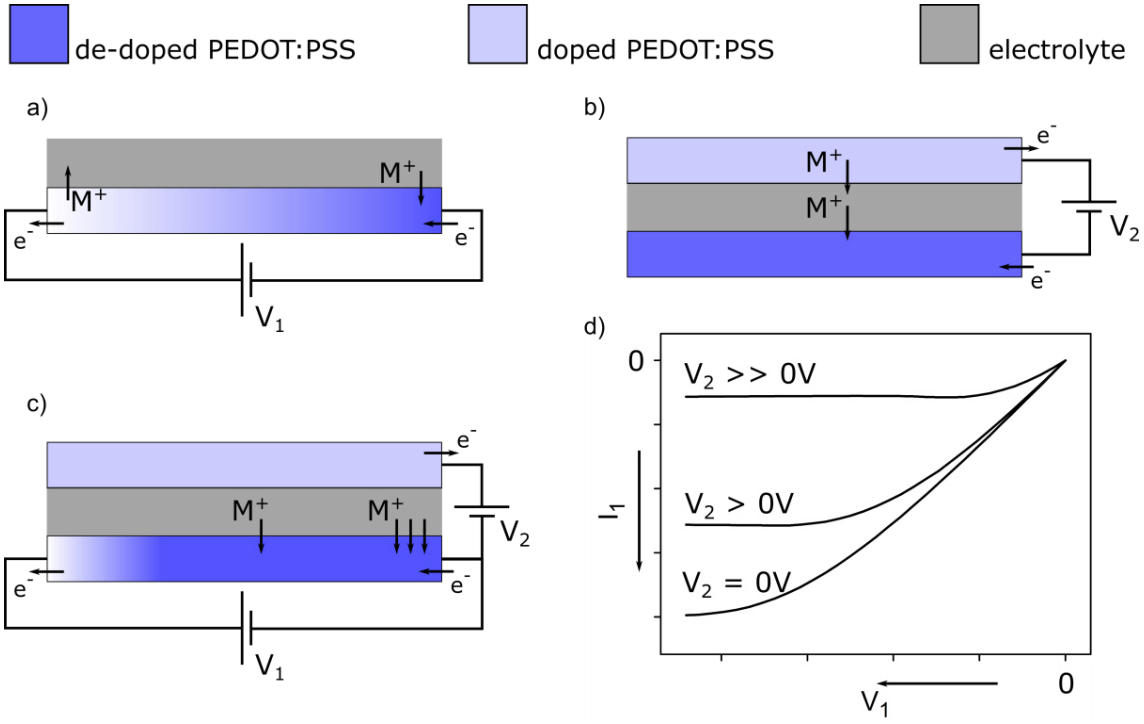


Figure 3.1: Arrangement of a PEDOT:PSS electrode and an electrolyte in a) the dynamic configuration b) the bi-stable configuration and c) the combined configuration. d) voltage-current characteristics of the combined configuration.

3.2 Transistor Configuration

The transistor configuration is basically identical with the combined configuration (section 3.1.3). A picture of the configuration depicting the electrodes, voltages and currents is shown in figure 3.2a.The source-drain line (S-D line) is a solid line of PDOT:PSS covered with an electrolyte containing mobile cations (M^+) and with a negative voltage applied (V_D). It resembles the dynamic configuration including its voltage/current characteristics with the pinch-off voltage where saturation of the drain-current (I_D) occurs. The gate electrode is connected to the source-drain line via the electrolyte. A positive voltage is applied between the gate electrode and the source-drain line, denoted as the gate voltage V_G. Using this voltage, control over voltage/current characteristics of the source-drain line is possible. With increasing gate voltage V_G the pinch-off at the source-drain line occurs at lower source-drain voltages (V_D). When no gate voltage is applied a significant drain current is flowing, representing the on-state of the transistor. When the gate voltage is high enough pinch-off happens immediately when a drain voltage is applied and the transistor is in the off state. As this characteristic, depicted in figure 3.2b, describes depletion mode behavior the transistor is a normally-on device. Another feature of the OECT is that the source-drain voltage and current

are negative but the gate voltage is positive. The transistor is working in the third quadrant of the set of characteristics depicted in figure 3.2c. This behavior implicates challenges when building circuits with this type of devices (compare chapter 5).

The area on the source-drain line that is covered with electrolyte can be considered as the transistor channel. In this area, highlighted in figure 3.2d, the resistance of the organic semiconductor is altered, representing the on- and off-switching of the organic electrochemical transistor. This area is defined by the width of the source-drain line, the thickness of the source-drain line and the width of the electrolyte line covering the PEDOT:PSS.

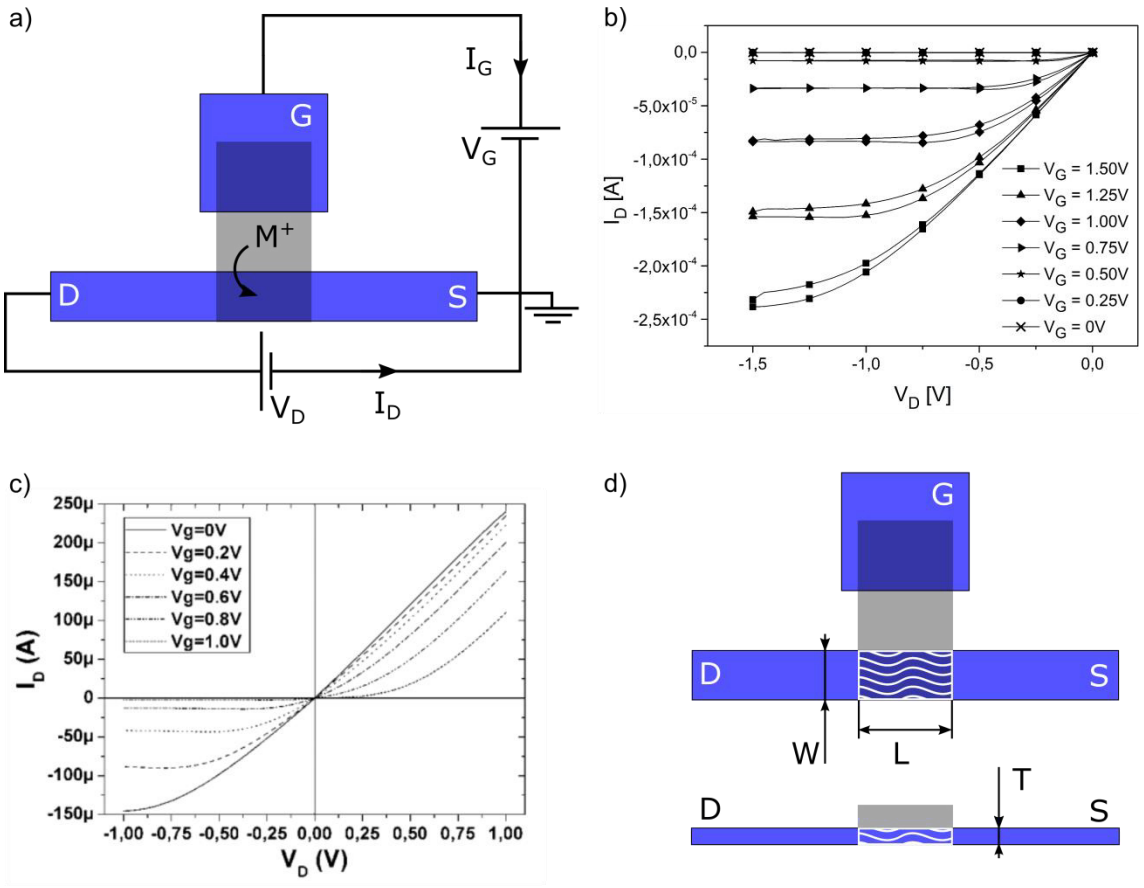


Figure 3.2: a) Transistor configuration with the source-drain line (S-D) and the gate electrode (G) fabricated from PEDOT:PSS in blue and the electrolyte in grey. Additionally the gate voltage and current (V_G, I_G), the drain voltage and current (V_D, I_D) as well as the mobile cations (M^+) are displayed. b) Output characteristics of an OECT. c) Set of characteristics displaying the four quadrants a transistor can work in [19]. d) Channel area of an OECT (highlighted with white waves) defined by the width of the source-drain line W, the thickness of the source drain line T and the width of the covering electrolyte line L.

3.3. Transistor Theory

Quantitative models to describe the transistor behavior and reproduce transistor characteristics are a useful tool. For OFETs these models have been refined over the last decades, enhancing the possibilities to predict voltage-current characteristics when physical properties of the transistor are known [21]. For OECTs on the other hand, to the best of our knowledge no such comprising model exists. A few attempts to describe the OECT behavior can be found in literature, which are summarized briefly in the following. In this thesis only an overview of the respective models is provided. For details the reader is referred to the original literature.

Prigodin and co-workers are describing the switch-off of the OECT [22]. Following a solid-state physics approach they describe the change of the organic semiconductors conductivity when in contact with an electrolyte and a voltage is applied. The charge transport mechanism is described as an intergrain hopping of charge carriers between crystalline sites inside the polymer network. Hopping states in the polymer are associated with the strongly localized negatively charged sites at the polymer backbone. When a voltage is applied cations migrate into the polymer network, which is loose enough for ions to penetrate easily. Those cations interact with the negatively charged sites at the polymer backbone. By this partial charge compensation, the intergrain hopping taking place between different crystalline areas of the polymer network is suppressed, thus reducing the conductivity to a very large amount. Hence this model depicts the relation between the applied voltage (driving the cations) and the increase of resistance in the semiconducting material.

Robinson and co-workers followed an approach combining electrochemistry and solid-state physics [20]. Their work is based on the Nernst equation, which is describing the relationship between activities and potential in equilibrium.

$$E - E^0 = -\frac{R*T^0}{n*F} * ln\left(\frac{A_{prod}}{A_{react}}\right) \quad \text{(Eq. 3.2)}$$

In this equation E is the potential, E^0 is the standard potential, R is the ideal gas constant, T^0 is the absolute temperature, n is the number of transferred electrons, F is the Faraday constant and A is the Activity, either of the products or of the reactants. Additionally a relation between

the activities and the doping fraction is established. Some assumptions have to be made, like a constant total amount of doped material, which is a standard assumption in electrochemistry when no side reactions occur. Also a maximum doping level is introduced, estimated for a specific material. With a constant amount of counter ions in the electrolyte assumed, a relationship for the activities A and the doping levels γ between two points in the transistor channel (a and b) can be made.

$$\frac{A_{prod}}{A_{react}} = \frac{\gamma_a}{(\gamma^{max} - \gamma_a)} * \frac{(\gamma^{max} - \gamma_b)}{\gamma_b} \qquad \text{(Eq. 3.3)}$$

Using those equations and setting a number of boundary conditions they were able to describe several parameters of the OECT in steady-state qualitatively. The gradients of the potential and of the doping fraction along the source-drain line are calculated using the set of equations described in their publication. This is particularly interesting as the pinch-off of the transistor can be described and understood like this. The calculations are backed by experiments monitoring the potential at several spots of the source-drain line by the use of potential sampling fingers and also the doping level by optical measurements. For simplified cases also I-V curves were correctly reproduced. Although a working qualitative model is described, no quantitative statements are possible. Many assumptions and simplifications have to be made and many parameters remain unknown. Nevertheless important aspects of OECT physics are highlighted.

Bernards and Malliaras show a model describing both the steady state and the transient behavior of OECTs [23]. They divide the transistor into two circuits; an electronic circuit and an ionic circuit, reflecting the fact that both types of charge carriers are transported in an OECT. In the electronic circuit holes are transported within the semiconductor. It is determined by the mobility and the density of those holes and described using Ohms law. The ionic circuit reflects the transport of ionic charge in the electrolyte and via the electrolyte/semiconductor interface. It is determined by the initial hole density and the charge of injected cations in the semiconductor film. The equivalent circuit used for those circuits, as well as the theoretical slice of organic semiconductor considered for the model are displayed in figure 3.3. A combination of the two circuits is used to model the steady-state and the transient behavior of the OECT.

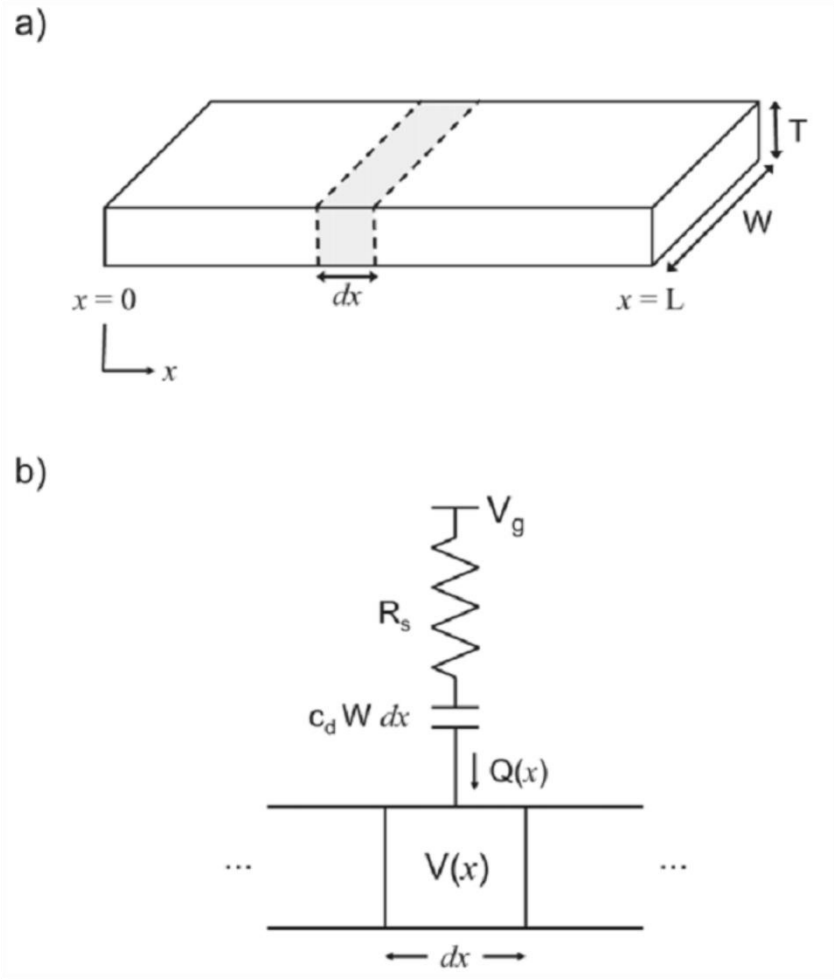


Figure 3.3: a) Channel of the OECT with the theoretic slice used for the model highlighted and the variable parameters marked. b) Equivalent circuit used for the demonstrated model [23].

Using equation 3.4, reflecting the combination of the ionic and electronic circuit in steady state, I-V characteristics can be modeled. The obtained results match experimentally determined characteristics to a very large extend, confirming the usability of this model.

$$J(x) = q * \mu * p_0 * \left(1 - \frac{V_g - V(x)}{V_p}\right) * \frac{dV(x)}{dx} \qquad \text{(Eq. 3.4)}$$

In this equation J(x) is the current flux, q is the elementary charge, μ is the hole mobility, p_0 is the hole density, V_g is the gate voltage, V_p is the pinch-off voltage and dV(x)/dx is the electric field.

The transient behavior is dominated by the injection of cations into the semiconductor film and the removal of holes at the source-drain electrode. It is described starting from the steady state and adding two time constants: One for the ionic transport in the electrolyte (τ_i), determined by the electrolyte resistance and the capacitance of the double layer, and another for the electronic transit time (τ_e), determined by the hole mobility, channel dimensions and the applied gate voltage. Assuming a homogeneous de-doping in the entire transistor channel without any saturation effects, the current, depending on gate voltage and time, can be expressed as follows:

$$I(t, V_g) = I_{SS}(V_g) + \Delta I_{SS} * \left(1 - f\frac{\tau_e}{\tau_i}\right) exp\left(\frac{-t}{\tau_i}\right) \quad \text{(Eq. 3.5)}$$

In this equation I_{SS} is the steady state source-drain current at the gate voltage V_g, ΔI_{SS} is the difference between the source drain current at 0 V gate voltage and the source-drain current when V_g is applied, f is a constant of proportionality to take the spatial non-uniformity of the de-doping into account and τ_i and τ_e are the time constants described above. The constant f is expected to depend on the drain voltage and the gate voltage. This undetermined factor f is influencing the time dependent response to a large extent, making quantitative modelling of the transient behavior unrewarding. Qualitative modelling on the other hand has taken a leap forward thanks to this model. In summary this model is providing a very precise description of the steady state behavior and also a deep insight into the transient behavior, considering the peculiarity of the OECT with both the ionic and electronic charge transport involved in the switching process.

4. Transistor design

There is one general design rule established concerning the geometry of the source-drain and the gate electrode. The area of the gate electrode covered with electrolyte should be at least ten times bigger than the area of the transistor channel. Like this an over-oxidation of the gate electrode is prevented when reducing the transistor channel (switching the transistor off). Such an over-oxidation leads to irreversible oxidation on the polymer chain of the PEDOT:PSS, causing an entire loss of conductivity and thereby the destruction of the transistor[19, 24, 25]. Apart from this design consideration there are two basic transistors designs possible, describing the arrangement of the electrodes and the electrolyte: the lateral and the vertical transistor design.

4.1 Lateral Design

The lateral design, as displayed in figure 4.1a, is used for all the transistors described in the paper reprint section of this thesis. Featuring this design the transistor is built utilizing only two active layers deposited on top of the substrate; the organic semiconductor (in this work PEDOT:PSS) and the electrolyte (in this work diverse electrolytes are used). All the semiconductor electrodes are located at one level, making this design tailor-made for fabrication by printing processes. Additionally no alignment of the electrodes is necessary as they are all structured in the same fabrication step. The electrolyte is placed on top of the semiconductor electrodes. An implicated advantage of this design is the high degree of freedom concerning the electrolyte material properties. Either liquid gelled or solid materials are possible in this transistor design as no other material has to be deposited on top of the electrolyte. Another advantage is that the electrolyte application is usually the fabrication step finalizing the laterally designed OECT, so the electrolyte is not exposed to follow up process steps that might deteriorate its stability or performance. A performance parameter, more precisely the switching time, is the major drawback of this transistor design. An inherent problem is the so called reduction front, an area of reduced PEODT outside the area covered with electrolyte on the drain side of the source-drain line. Due to the missing physical contact between reduced semiconductor and electrolyte, switching this area is depending on diffusion, making it very slow. This problem can be circumvented by using an adapted lateral design: a highly conductive inert material is printed over the organic semiconductor reaching the transistor channel but not connecting the source and drain electrode. Like this formation of the reduction front is hindered and faster switching devices are obtained [26].

4.2 Vertical Design

In this design, displayed in figure 4.1b, three layers are present: First the organic semiconductor, next the electrolyte and on top again the organic semiconductor. Transistors featuring this design are not that simple to fabricate compared to lateral OECTs. The electrolyte needs to be solid and stable enough to withstand the processing necessary to apply the second electrode. An alternative is the use of a second foil, carrying the top electrode, which is laminated onto the first foil containing layers one and two. A challenge arising from this process is the need for alignment of the first and the second electrode. An adapted form of the vertical design is the use of a liquid electrolyte placed in a reservoir above the source-drain electrode with a Pt-wire acting as the gate electrode. This transistor design is very common in sensing applications (an example is given in [27]). Vertically designed OECTs are

generally considered to be faster switching because (i) the formation of a reduction front is less pronounced than in lateral OECTs and (ii) the location of the gate electrode directly above the transistor channel, only separated by the electrolyte and thereby in close proximity, is favorable in terms of the driving force for insertion of cations into the semiconductor layer. Depending on the application it is necessary to evaluate if the performance demands justify the much more complicated fabrication process.

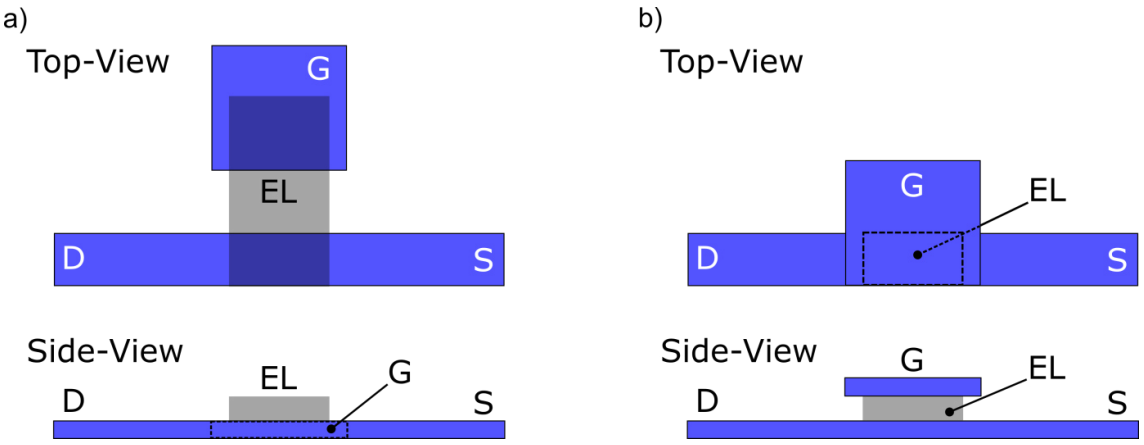


Figure 4.1: Top and side view of an OECT in a) lateral and b) vertical transistor design with S, D and G being the source, drain and gate electrodes, respectively, and EL being the electrolyte.

5. Logic Gates

When building transistors there is always the goal to fabricate circuits as well. In this way the complexity of tasks the device is able to complete can be enhanced. A modern Intel i7 processor contains around 1.8 billion transistors [28], numbers that are way beyond the reach of present day organic electronics. But Myny et al. demonstrated a processor comparable to an early days Intel 4004 -processor from 1971, based on OFETs and containing 3381 single transistors [29]. For OECTs on the other hand no circuits more complex than NAND gates have been demonstrated. A reason for this may be the architecture OECTs demand for the fabrication of inverters, a basic building block for every circuit. To the best of our knowledge Nilsson and co-workers were the first to publish research on logic circuits based on OECTs. Chapters 5.1 and 5.2 are based on this work [19, 30].

5.1 Inverter

In a NOT gate, also called inverter, the input signal is inverted. In Boolean terms an input of 1 results in an output of 0 and vice versa. An output of 0 lies in the region of zero volts whereas an output of 1 lies in the region of the maximum input voltage of the inverter. In OECTs the input signal is positive and the output signal negative (OECTs operate in the third quadrant of the set of characteristic, compare figure 3.2c). To obtain the described inverter behavior, where the output of 1, intrinsically negative for an OECT, is in the range of the maximum input voltage, intrinsically positive in an OECT, a specific inverter architecture is needed. A voltage divider consisting of three resistors is connected to the source-drain electrode of the transistor. Additionally two supply voltages, one positive and one negative ($+V_{DD}$, $-V_{DD}$), are applied to the ends of the voltage divider. The input of the inverter is at the gate electrode of the OECT whereas the output is at the voltage divider (figure 5.1a). When the input is 1, the OECT is switched-off. In this state the transistor acts as a very high-impedance resistor. The pathway of minimal resistance in this state is across the three resistors of the voltage divider (compare the blue highlighted path in figure 5.1a). The voltage divider and the supply voltages thereby define the output voltage level of the inverter in this state. They need to be adjusted to give a logical 0 as the output signal, meaning that R1 + R2 ≈ R3. When the input is 0, the OECT is switched-on. In this state the transistor exhibits a low resistance; lower than the resistor R1 of the voltage divider. R1 is bridged by the on-state transistor, resulting in the minimum resistive pathway via the transistor and R2 and R3 of the voltage divider (compare the red highlighted path in figure 5.1a). In this state the output of the inverter is defined by the resistances of R2, R3 and of the on-state transistor (on-resistance) as well as the supply voltage, adjusted to result in an output signal of 1. For the inverter design two parameters are crucial: The transistor`s on-resistance and the gate voltage necessary to switch-off the transistor. Calculations to define voltages and resistors considering the transistor characteristics are possible using voltage divider theory and the superposition principle. For more details the reader is referred to paper 3 included in this thesis (Chapter 9). With the described architecture inverter behavior is obtained using an OECT. The drawback of this architecture is that the characteristics of the single transistor are reflected in the transfer characteristics of the inverter. In contrast when using OFETs it is possible to use two transistors to fabricate an inverter. In an organic complementary inverter for example a combination of an n–type and a p-type transistor is used. In the ON-state of the inverter the p-type transistor is on, setting the output on the level of the supply voltage. In the OFF-state of the inverter the n-type transistor is on, setting the output on zero volts [31]. As long as leakage is prohibited,

one particular transistor is responsible for one particular inverter state. The transient between the two inverter states reflects the voltage area where one transistor is not entirely switched on and the other transistor is not entirely switched off. Accordingly the inverter transfer behavior is not depending on the characteristics of a single transistor and its ON- and OFF-state (as it is the case for OECT based inverters). A matching performance of the two transistors presumed highly symmetric switching behavior is possible, enabling higher gains and noise margins compared to OECT based inverters. Those two factors are important figures of merit for inverters. The gain represents the maximum slope of the inverter transfer characteristics (figure 5.1b). The higher the gain the lower is the input voltage area where the transistor is neither in the 1- nor in the 0-state. For the sake of precise switching the highest possible gain is therefore desirable. The noise margin represents the stability of the inverter against transistor parameter variations and electrical noise [31]. A common procedure for determining the noise margin is the “maximum equal criterion” or MEC. The noise margin is defined by the largest square one can possibly fit between inverter transfer curve and the mirrored inverter transfer curve (figure 5.1c) [32]. Using those two values a convenient quantification of the inverter performance and also a comparison of the performance of different inverters are possible.

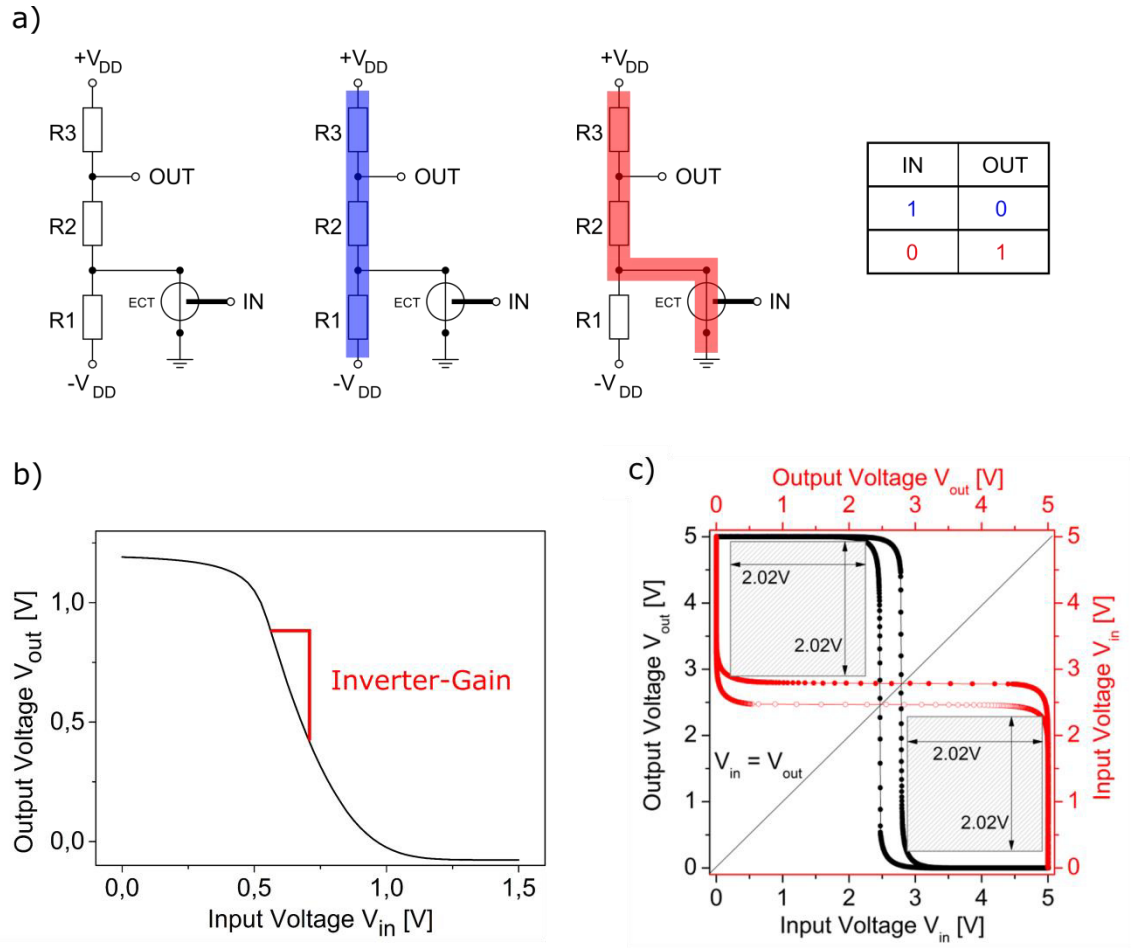
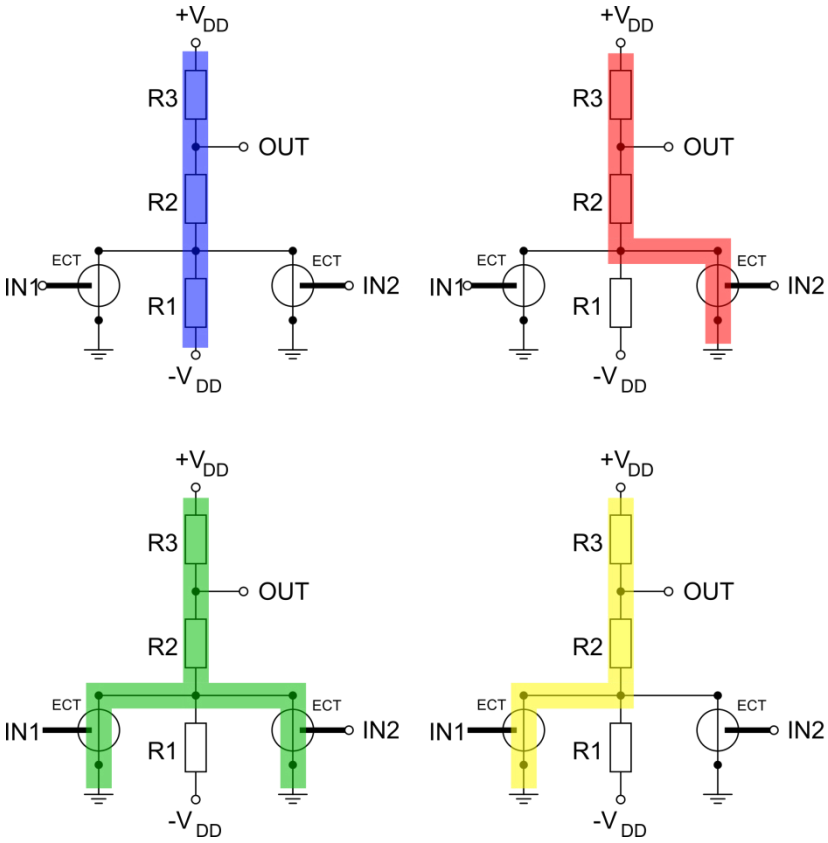


Figure 5.1: a) Inverter based on OECT; highlighted are the switching states. b) c) Inverter transfer characteristics with b) gain and c) noise margin [31] depicted.

5.2 NAND Gate

A NAND gate is a very important building block because any combinatorial logic function can be fabricated using a combination of NAND gates [33]. The added functionality compared to the inverter is achieved by a second transistor that is connected in parallel to the first one. Like this the function of a NAND gate is achieved. When a 0 is applied to the input of one of the transistors, this transistor is in the on-state. It exhibits a low resistance (R_{ON}), making the pathway via this transistor the one with the lowest resistance. From the combination of supply voltage, voltage divider and R_{ON} a logical 1 is obtained as the output signal (compare section 5.1). The same is true when both inputs signals are 0. Again the last resistor of the voltage divider is bridged by the on-switched transistors and logic 1 is obtained at the output. Logic 0 at the output is only obtained when both input signals are 1. Like this both transistors are in their non-conducting off-state, leaving the voltage divider as the pathway with the lowest

resistance. This combination of voltage divider and supply voltages results in logic 0 at the output. The different states of the NAND gate are depicted in figure 5.2.



IN 1	IN 2	OUT
1	1	0
1	0	1
0	0	1
0	1	1

Figure 5.2: NAND gate based on OECT; highlighted are the switching states.

References

[1] M. Nikolou, G. G. Malliaras, Applications of poly(3,4-ethylenedioxythiophene) doped with poly(styrene sulfonic acid) transistors in chemical and biological sensors. *Chem Rec.* 2008, *8*, 13-22.

[2] H. S. White, G. P. Kittlesen, M. S. Wrighton, Chemical Derivatization of an Array of Three Gold Microelectrodes with Polypyrrole: Fabrication of a Molecule-Based Transistor. *J . Am. Chem.* SOC. 1984, *106,* 5375-5377.

[3] J. W. Thackeray, H. S. White, M. S. Wrighton, Poly(3-methylthiophene)-Coated Electrodes: Optical and Electrlcal Properties as a Function of Redox Potential and Amplification

of Electrical and Chemical Signals Using Poly(3-methylthlophene)-Based Microelectrochemical Transistors. *J . Phys. Chem.* 1985*,89,* 5133-5140.

[4] S. Chao, M. S. Wrighton, Characterization of a solid-state polyaniline-based transistor: water vapor dependent characteristics of a device employing a poly(vinyl alcohol)/phosphoric acid solid-state electrolyte. *J Am Chem Soc* 1987, *109*, 6627.

[5] V. Rani, K.S.V. Santhanam, Polycarbazole-based electrochemical transistor, *J Solid State Electrochem* 1998, *2*, 99-101.

[6] T. Matsue, M. Nishizawa, T. Sawaguchi, l. Uchida, An Enzyme Switch Sensitive to NADH, *J. Chem. Soc., Chem. Commun.* 1991, 1029-1031.

[7] D. Nilsson, M. Chen, T. Kugler, T. Remonen, M. Armgarth, M. Berggren, Bi-stable and Dynamic Current Modulation in Electrochemical Organic Transistors. *Adv. Mater*. 2002, *14*, 51-54.

[8] L. Groenendaal, F. Jonas, D. Freitag, H. Pielartzik, J. R. Reynolds, Poly(3,4-ethylenedioxythiophene) and Its Derivatives: Past, Present, and Future. *Adv. Mater.* 2000, *12*,.

[9] J. Ouyang, ‘‘Secondary doping’’ methods to significantly enhance the conductivity of PEDOT:PSS for its application as transparent electrode of optoelectronic devices. *Displays* 2013, *34*, 423–436.

[10] U. Lang, E. Müller, N. Naujoks, J. Dual, Microscopical Investigations of PEDOT:PSS Thin Films. *Adv. Funct. Mater.* 2009, *19*, 1215–1220.

[11] J. Ouyang, Q. Xu, C.-W. Chu, Y. Yang, G. Li, J. Shinar, On the mechanism of conductivity enhancement in poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) film through solvent treatment. *Polymer* 2004, *45,* 8443–8450.

[12] T. Horii, Y. Li, Y. Mori, H. Okuzaki, Correlation between the hierarchical structure and electrical conductivity of PEDOT/PSS. *Polymer Journal* 2015, *47*, 695-699.

[13] A. J. Heeger, Charge Storage in Conducting Polymers: Solitons, Polarons, and Bipolarons. *Polymer Journal* 1985, *17*, 201-208.

[14] J. Bredas, G. Street, Polarons, Bipolarons, and Solitons in Conducting Polymers. *Acc. Chem. Res*. 1985, *18*, 309–315.

[15] O. Bubnova, Z. U. Khan, H. Wang, S. Braun, D. R. Evans, M. Fabretto, P. Hojati-Talemi, D. Dagnelund, J.-B. Arlin, Y. H. Geerts, S. Desbief, D. W. Breiby, J. W. Andreasen, R. Lazzaroni, W. M. Chen, I. Zozoulenko, M. Fahlman, P. J. Murphy, M. Berggren, X. Crispin, Semi-Metallic Polymers. *Nat. Mater*. 2013, *13*, 190–194.

[16] B. Park, Lei Yang, E. M. J. Johansson, N. Vlachopoulos, A. Chams, C. Perruchot, M. Jouini, G. Boschloo, A. Hagfeldt, Neutral, Polaron, and Bipolaron States in PEDOT Prepared by Photoelectrochemical Polymerization and the Effect on Charge Generation Mechanism in the Solid-State Dye-Sensitized Solar Cell. *J. Phys. Chem. C* 2013, *117*, 22484−22491.

[17] Y. Xia, J. Ouyang, Significant Different Conductivities of the Two Grades of Poly(3,4-ethylenedioxthiophene):Poly(styrenesulfonate), Clevios P and Clevios PH1000, Arising from Different Molecular Weights. *ACS Appl. Mater. Interfaces* 2012, *4*, 4131–4140.

[18] M. C. J. M. Vissenberg, M. Matters, Theory of the field-effect mobility in amorphous organic transistors. *Phys. Rev. B: Condens. Matter Mater. Phys.* 1998, *57*, 12964.

[19] D. Nilsson (2005). An Organic Electrochemical Transistor for Printed Sensors and Logic. Linköping Studies in Science and Technology, Dissertations, No. 921

[20] N. D. Robinson, P.-O. Svensson, D. Nilsson, M. Berggren, On the Current Saturation in Electrochemical Polymer Transistors. *J. Electrochem. Soc*. 2006, *153*, H39.

[21] G. Horowitz. “Organic Transistors.” In: *Organic Electronics*. Ed. by H. Klauk. Weinheim: Wiley-VCH, 2006. Chap. 1.

[22] V. N. Prigodin, F. C. Hsu, Y. M. Kim, J. H. Park, O. Waldmann, and A. J. Epstein, Electric Field Control of Charge Transport in Doped Polymers. *Synth. Met.* 2005, *153*, 157–160.

[23] D. A. Bernards, G. G. Malliaras, Steady State and Transient Behavior of Organic Electrochemical Transistors. *Adv. Func. Mat*. 2007, *17*, 3538.

[24] M. Berggren, R. Forchheimer, J. Bobacka, P.-O. Svensson, D. Nilsson, O. Larsson, A. Ivaska, “PEDOT:PSS based electrochemical transistors for ion-to-electron transduction and sensor signal amplification,” in Organic Semiconductors in Sensor Applications, vol. 107 of Springer Series in Materials Science, pp. 263–280, Springer, Berlin, Germany, (2008).

[25] [1] A. Zykwinska, W. Domagala, B. Pilawa, and M. Lapkowski, Electrochemical overoxidation of poly(3,4-ethylenedioxythiophene)—PEDOT studied by means of in situ ESR spectroelectrochemistry. *Electrochim. Acta* 2005, *50*, 1625–1633.

[26] P. Andersson Ersman, D. Nilsson, J. Kawahara, G. Gustafsson, M. Berggren, Fast-switching all-printed organic electrochemical transistors. *Org. Electron.* 2013, *14*, 1276–1280.

[27] P. Lin, F. Yan, Organic Thin Film Transistors for Chemical and Biological Sensing. *Adv. Mater.* 2012, *24*, 34.

[28] https://en.wikipedia.org/wiki/Transistor_count, visited 06.06.2016

[29] K. Myny, E. van Veenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, P. Heremans, An 8-Bit, 40-Instructions-Per-Second Organic Microprocessor on Plastic Foil. *IEEE J. Solid-State Circuits* 2012, *47*, 284–291.

[30] D. Nilsson, N. Robinson, M. Berggren, R. Forchheimer, Electrochemical Logic Circuits. *Adv. Mater.* 2005, *17,* 353–358.

[31] A. Petritz (2015), Photo reactive and natural source based materials as functional layers in organic thin film transistors and organic complementary inverters. Dissertation, Karl-Franzens-Universität, Graz.

[32] J. R. Hauser, Noise margin criteria for digital logic circuits. *IEEE Trans. Educ.* 1993, *36*, 363–368.

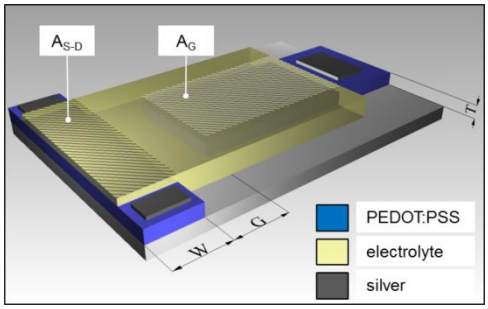
[33] V.P. Nelson, H.T. Nagle, J.D. Irwin, B.D. Carroll, “Introduction to Sequential Devices,” in *Digital Logic Circuit Analysis and Design*, Prentice Hall Inc.: Upper Saddle River, New Jersey, 1995, pp 406-407.

III Paper Reprints

The versions of the papers reprinted in this thesis are the final manuscripts as submitted by the authors. The final composition by the editorial office is missing and graphical alterations are conducted to improve the consistency with the thesis. This includes added captions in paper 1, removing of author affiliations and removing of keywords for improved readability as well as unifying the reference format.

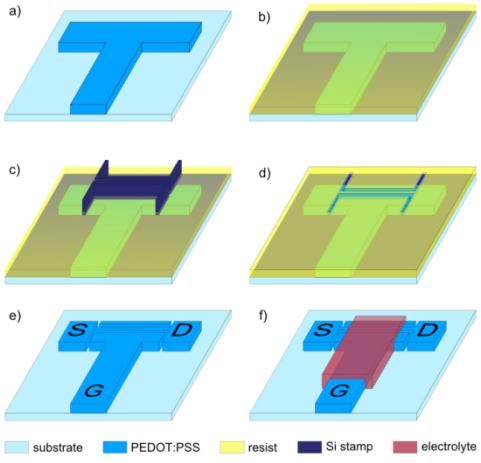
6. Paper Overview

6.1 Paper 1: Influence of geometry variations on the response of organic electrochemical transistors



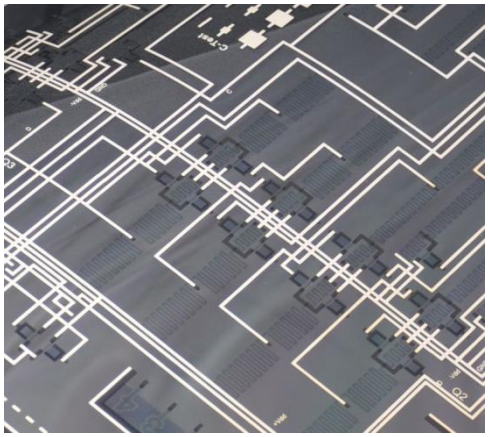
Entirely inkjet-printed OECTs are used to examine the relationship between the geometry of such a transistor and its performance. The width of the source-drain electrode, the electrode thickness and the gap between source-drain and gate electrode are varied, monitoring the influence of this variation on the on-current and the on/off-current ratio. In Addition entirely inkjet-printed inverters are fabricated.

6.2 Paper 2: Nanoimprint Lithography-Structured Organic Electrochemical Transistors and Logic Circuits



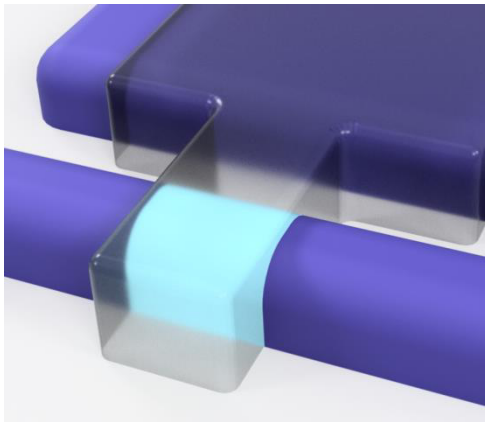
A hybrid fabrication process combining inkjet-printing and nanoimprint-lithography (NIL) is developed to fabricate OECTs with critical dimensions in the range of 10µm. The PEDOT:PSS is pre-structured by inkjet-printing before the electrodes are defined by a NIL structuring step. To finalize the OECTs the electrolyte is applied by inkjet-printing. Using these devices the effect of miniaturization on the device performance is examined. Additionally Inverters and also NAND gates utilizing these OECTs are fabricated and their performance is compared to entire inkjet-printed ones.

6.3 Paper 3: All Screen Printed Logic Gates Based on Organic Electrochemical Transistors



Entirely screen-printed OECTs and PEDOT:PSS resistors are used to fabricate inverters, NAND gates, flipflops and a 2-bit shift register. All of the basic building blocks and the circuits are examined concerning the uniformity of their performance. The performance of more than 380 OECTs and resistors is examined by comparing the output of eight flipflops. With this study both the usability of OECTS for complex circuits and the capability of fabricating organic electronic devices entirely by screen printing is demonstrated.

6.4 Paper 4: Efficiency of the Switching Process in Organic Electrochemical Transistors



In this paper the influence of the volume of PEDOT:PSS in the transistor channel V_C on the charge necessary to switch the transistor off is examined. Transistors are fabricated entirely by screen-printing, varying the volume of the transistor channel, and the gate current switching them off is monitored. The gate current is subsequently used to determine the amount of PEDOT actively participating in the electrochemical switching process and conclusions on the switching efficiency are drawn.

7. Influence of geometry variations on the response of organic electrochemical transistors

7.1 Abstract

We report on the fabrication and characterisation of entirely inkjet-printed organic electrochemical transistors (OECTs) based on poly(3,4-ethylenedioxithiophene) poly(styrenesulfonate) (PEDOT:PSS). These transistors were used to evaluate the assumed geometry-performance relationship of OECTs by changing the transistor dimensions and monitoring the output characteristics. We could show that the on-current depends on the PEDOT:PSS thickness and that the on-to-off current ratio is related to the distance between the printed electrodes. Taking these results into account, we fabricated entirely inkjet-printed electrochemical inverters with a switching time of about 4 s. These inverters outline a first step from organic electrochemical transistors towards logic circuits.

7.2 Introduction

Since the discovery of conducting polymers in the late 1970s, a lot of research activities in polymer science aimed at developing printed electronic circuits, which combine multifunctional materials with low-cost production and a versatile form factor [1]. The key elements of any electronic circuit are transistors and resistors. There are two main concepts to build transistors based on organic materials: organic thin film transistors (OTFT) and organic electrochemical transistors (OECT). The simplest way to realize both organic resistors and organic transistors is based on printable conjugated polymers that can be used as printed resistors or if combined with electrolytes form an OECT. One well known example of such a polymer is PEDOT:PSS (poly(3,4-ethylenedioxithiophen) poly(styrenesulfonate)) which shows electrochemical switching over five orders of magnitude [2] via a voltage-induced reversible redox process.

OECTs have several advantages compared to organic thin film transistors. First, due to the absence of a gate dielectric, the charge carrier transport is not determined by the often imperfect quality of the interface between semiconductor and gate dielectric, which leads to trapping and performance instabilities. Second, due to the high capacitance of the electrolyte their operating voltage is very low, allowing for a switching of the OECTs in the range of 1 V and below. Third, only few materials and a very simple design are needed for OECTs thus decisively simplifying the printing process. Finally, they act as an ideal platform for the integration of electronic and biological systems, because of their unique ability to conduct

both electronic and ionic carriers. Due to all these advantages, electrochemical transistors increasingly find their application in cell transport measurement [3], circuitry for disposable electronics [4], active-matrix physical sensor circuits [5], and in chemical [6] and biological sensors [7,8]. A comprehensive overview of OECTs and OTFTs for chemical and biological sensing is provided in literature [9].

An inherent characteristic of OECTs is that a positive input voltage is needed to switch the transistor, resulting in a negative output voltage. This makes it impossible to drive a transistor with a preceding one [4]. To shift the negative output voltage to positive values, a voltage divider connected to the output of the transistor is needed. This combination of an OECT and a voltage divider is working as an electrochemical inverter, generating an output signal of logic 1 when the input is 0 and logic 0 when the input is 1. One major drawback of OECTs is their low switching speed which is a result of the intrinsically low mobility of the ions in the electrolyte and the limited speed of the redox reaction. We assume that the geometry of the device also has a substantial influence on the transistor speed. Although the general working principle of OECTs was investigated intensively [10-13], there exists no comprehensive work on the geometry-performance relationship of OECTs; only the influence of the ratio between the gate area A_G and the source-drain area A_{SD} on the I(V) curves was investigated [14,15]. Additionally a faster response time of OECTs when the length of the source-drain line is decreased was observed [16]. The latter was also shown for transistors used in biosensing [17]. Accordingly, we examined the effect of varying the transistor geometry on the IV-curves of printed OECTs in a systematic way. The OECTs were fabricated by inkjet printing and had a lateral configuration (see Fig. 7.1(a)). The optimized geometry of the OECTs was implemented in the fabrication of printed inverters which serve well to showcase the effect of fundamental OECT parameters in practical applications. These inverters are composed of high performing OECTs and PEDOT:PSS resistors, based on only three inks (PEDOT:PSS, Silver, Electrolyte), and exhibit a gain of 2.7.

7.3 Experimental

The gate electrode and the source-drain line of the transistor are formed by inkjet printing of PEDOT:PSS on PET (polyethyleneterephthalat) substrates. A silver pad ensures good contact between the electrodes and the measurement circuits. A cationic electrolyte is applied by inkjet printing between gate and channel, thus covering parts of the source-drain line and the gate electrode. The voltage divider which is used to form an inverter is printed with PEDOT:PSS and silver ink. As the substrate for all devices we use untreated Melinex ST725 PET foil from DuPont. Inkjet printing processes are done with the Fujifilm Dimatix Material Printer DMP

2800 with Dimatix DMC 11610 printing cartridges. The substrate temperature during printing is 40 C for PEDOT:PSS and silver ink. The PEDOT:PSS Clevios P Jet HC from H.C.Starck is filtered with a 0.2 µm PET filter. The silver is processed either by hand (Electrolube silver conductive paint) or by inkjet printing. The inkjet-printed silver Cabot CCI-300 is sonicated for 15 min and filtered with a 0.2 µm PET filter before use. After printing, the ink is sintered on a hot plate for 30 min at 100°C. The electrolyte is also applied either by hand or by inkjet printing. When inkjet is printed, 20 layers of electrolyte are applied on the substrate at ambient temperature. The used polyelectrolyte formulation consists of: 51 wt. % deionized water, 33 wt. % Poly(sodium-4-styrene sulfonate), 8 wt. % D-sorbitol, and 8 wt. % glycerol (85 wt. %), as found in literature [18]. For electrical characterization, a Suess Microtec probe station and a MB Technologies parameter analyzer are used and for the dynamic measurements a Thurlby Thandar Instruments TG230 frequency generator and a Tektronix TDS 2014 B oscilloscope. The different thicknesses of the layers are measured with a Dektak Profilometer by Bruker. All process steps are carried out under ambient conditions.

7.4 Results and Discussion

Three different geometry parameters of OECTs were investigated (Fig. 7.1(a)). First the thickness T of the PEDOT:PSS electrode was varied by increasing the number of printed layers of PEDOT:PSS. Then the gap G between the gate and the source-drain line was tuned. Finally, different line widths W were investigated. While modifying the geometry parameters of the devices, the ratio of the active area (area covered with electrolyte) between the gate electrode A_G and the source-drain line A_{SD} (see Fig. 7.1(a)) was held constant at a ratio of 10:1. Thus the reported influence of the area ratio on the on-to off ratio could be excluded [15]. From the I_{DS} (V_{DS})-characteristics basically two parameters were extracted and compared with respect to the device geometry—the on-current I_{on} (I_{DS} @ V_{GS} = 0 V, V_{DS} = -1 V) and the on-to off-ratio I_{on}/I_{off} (with I_{off} = I_{DS} @ V_{GS} = -V_{DS} = 1 V). In Fig. 7.1(b) a typical I_{DS}-V_{DS} curve of an organic electrochemical transistor with inkjet-printed PEDOT:PSS and non-optimized geometry is displayed. From the on-current Ion = -6.48 * 10^{-6} A and the off-current I_{off} = -6.54 * 10^{-8} A an on-to-off-ratio of 1 * 10^{2} is extracted. Between forward and reverse drain voltage sweep a clockwise hysteresis in the drain current is observed which results from the slow motion of the ions during the switching process; the respective gate switching current is also plotted in Fig. 7.1 (b) and is in the order of 1 * 10^{-7}A.

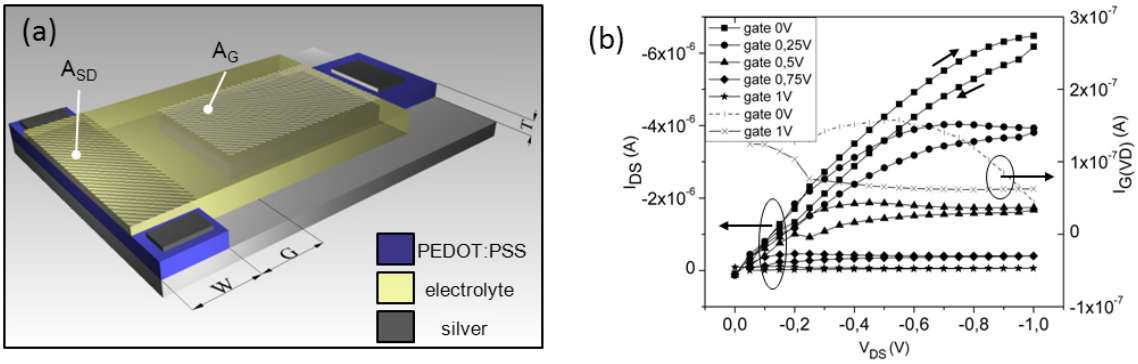


Figure 7.1: a) Architecture of a lateral OECT, the varied geometry parameters are (i) the thickness T of the PEDOT:PSS electrodes, (ii) the gap G between the gate electrode and the source-drain line and (iii) the width W of the source-drain line b) Output characteristics of an OECT with a non-optimized geometry (W = 100 µm, G = 1500 µm, T = 180 nm) and an area ratio A_G/A_{SD}= 10:1, the gate current is plotted for V_{GS}=-1 V and V_{GS}=0 V.

The electrodes' thickness T of transistors with nominal line widths W = 10 µm, 50 µm, 100 µm, 250 µm, and a gap G = 1500 lm was modified by multiple printing of PEDOT:PSS layers. Thickness values between 40 and 75 nm were obtained for one layer of printed PEDOT:PSS. For two, three, five, and seven layers of successively printed PEDOT:PSS, thickness values up to 450 nm were achieved. It can be assumed that a variation of T results in a change of the electrical properties of the PEDOT:PSS electrodes such as the conductivity (Fig. 7.2(a)). A decrease of the sheet resistance R_S with increasing thickness values T is observed, following the expected 1/T dependence [19]. From $R_S = \rho/T$, a resistivity of ρ = 0.01578 Ω∗cm is deduced, which corresponds to a conductivity of σ = 63 S/cm of the printed PEDOT:PSS layer. The effect of varying T on the OECT parameters is plotted in Figs. 7.2(b) and 7.2(c). The on-current I_{on} increases approximately linearly with the line thickness T (Fig. 7.2(b)) being consistent with the 1/T decrease of the sheet resistance. Since the linear I_{on}(T) correlation is valid for lines with different width W, the normalized I_{on}*(T) curves collapse together (Fig. 7.2(c)). Here I_{on}* corresponds to I_{on} divided by the actual line width W*; the latter can differ from the nominal line width W due to the limited alignment accuracy and the spreading of the PEDOT:PSS ink. The linear fit to the normalized on-current results in I_{on}* = -15.6 *T. In a simple model I_{on}* can be calculated from the linear part of the I(V) curve according to $I_{on, calc}$* = V/(R_S *L) = (V/L) * σ * T. In our example, L = 2.5 cm is the length of the printed S-D line, V = -0.7 V is the voltage range of the linear I(V)-part. Taking the conductivity σ = 63 S/cm from the fitted sheet resistance in Fig. 7.2(a), $I_{on, calc}$* = -17.6 * T which is very close to the fitted I_{on}* line.

The on-to-off ratio seems to be independent of T, meaning that I_{off} increases with T equivalently to I_{on} (Fig. 7.2(b)). The same observation holds for the dependence of the on-to off-ratio on the width W. A possible explanation for this might be the slower reduction of the PEDOT:PSS in the deeper regions of the source-drain line and in regions farther away from the gap edge. This leads to a graduation of reduced material during the measurement with mostly unreduced, high conducting material on the bottom of the line and fully reduced material on the top of the line, resulting in a higher overall off-current. This so-called reduction front is moved from the top towards the bottom of the line by the gate field and from the gap-sided electrode edge to the other. We can conclude that it is possible to increase the on-current by increasing the PEDOT:PSS line thickness T (and the width W), but the onto-off ratio remains virtually unchanged.

Next, the influence of the gap G on the device performance is examined. All OECTs in this experimental setup had a nominal line width W = 50 µm and a thickness T = 120 nm (optimized values). G was varied between 500 µm and 5 mm. The magnitude of the on-current does not depend on G (Fig. 7.2(d)) which can be expected since the on-current is measured with no gate voltage applied. So there should be no influence of the current on the distance between the gate and the source drain line.

However, the on-to-off ratio clearly increases for small G values (Fig. 7.2(d)). This observation can be explained as follows: When the gap is small enough, the redox reaction time is sufficient to reduce the entire width of the source-drain line within one measurement cycle and the transistor can be switched off much better. An additional requirement for achieving a complete switch-off is a gate potential that is big enough to move the cations all across the source-drain line and cause a reduction of the whole line width. These two preconditions lead to a low off-current. Assuming a constant on-current, transistors with smaller gaps reach higher on-to-off ratios than transistors with larger gaps.

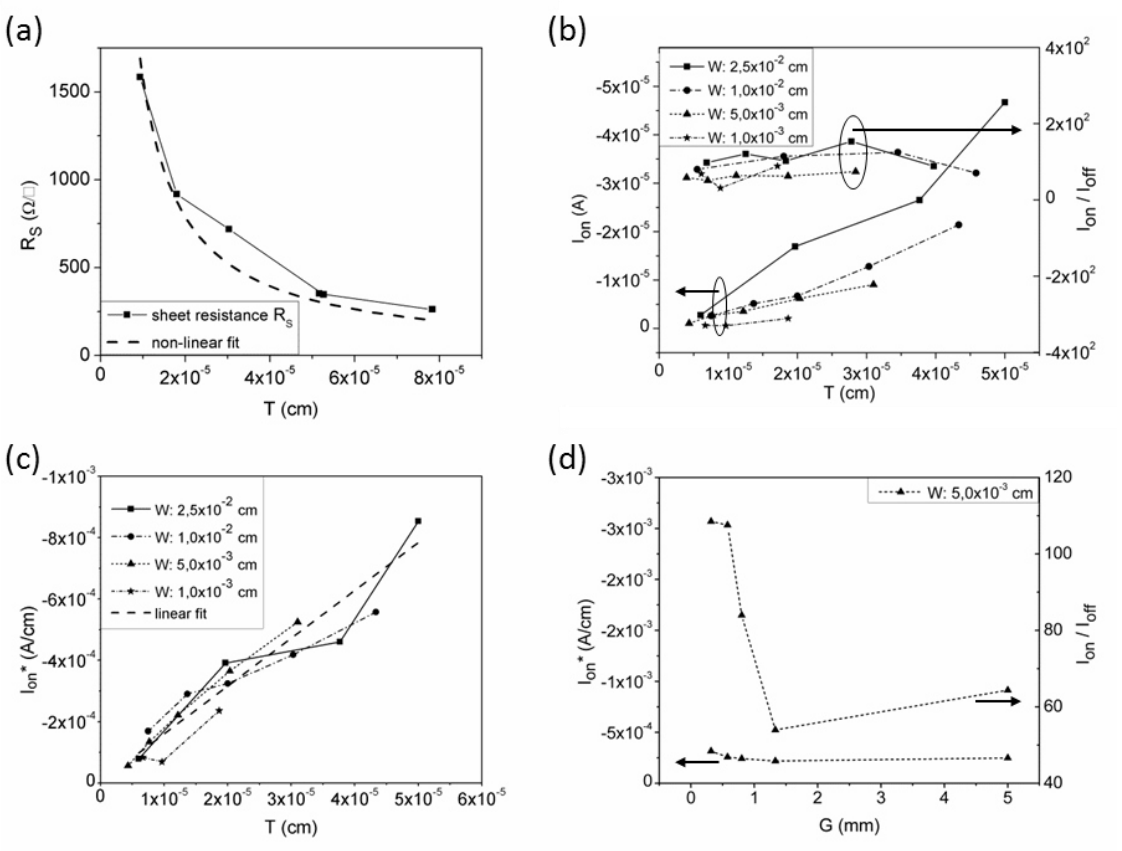


Figure 7.2: a) Dependence of sheet resistance R_S on PEDOT:PSS thickness T; fit-equation R_s = 0,01578 * T^{-1}. b) Dependence of the on-current I_{on} and of the on-to-off ratio on the line thickness T. c) Dependence of the normalized on-current I_{on}* on the line thickness T; I_{on} is normalized to the widths of the source-drain lines W*; fit- equation I_{on}* = -15,60158 * T. d) Dependence of the on-current and the on-to-off ratio on the gap G for transistors with W = 0,05 mm and T = 120 nm.

For the printing of the electrolyte, its viscosity had to be adapted and the minimum electrolyte volume for achieving satisfactory OECT characteristics had to be determined. It turned out that a minimum of 20 layers of electrolyte (50 µm thickness) is needed and that a 1 + 3 solution of electrolyte in deionized water is optimal with respect to high precision splash-free printing. For printed inverters, transistors with high on-to-off ratios rather than high on-currents are needed. Therefore, we chose a geometry of the all inkjet-printed OECTs with a small gap value (G = 500 µm) and a source-drain line width W = 250 µm with only one layer of PEDOT:PSS. Their output characteristics (Fig. 7.3(a)) reveal I_{on} = -4.5 * 10^{-5} A and I_{off} = -2.7 * 10^{-8} A, leading to an on-to-off ratio of 1.6 * 10^{3} which is more than one order of magnitude higher than what has been achieved for devices with non-optimized geometry. The lower hysteresis may indicate a higher switching speed compared to transistors without optimized geometry (compare Fig. 7.1(b)) Based on this design rule electrochemical inverters were fabricated with

the aim to determine the switching speed of the OECTs. As pointed out in the beginning, a voltage divider has to be printed and connected to the output of the transistor (Fig. 7.3(b)). This voltage divider is made of PEDOT:PSS and printed silver pads, the latter used to define the magnitude of resistance of the three needed resistors by their length. Considering the switch-on resistance of the transistor R_{ON} = 32 kΩ and the switch-off resistance R_{OFF} = 18 MΩ, resistors with R1: R2: R3 = 427 kΩ: 280 kΩ: 154 kΩ = 7.93: 5.20: 2.86 in length ratios were printed. For such a geometry and a symmetric voltage supply of $+V_{DD}$ = +3 V and $-V_{DD}$ = -3 V (see Ref. [8]), an output voltage of 1 V when the transistor is switched on and 0 V when it is switched off can be achieved. The transfer characteristics of such all inkjet-printed inverters show clear plateaus at the high and the low level (Fig. 7.3(c)). The voltage of the high level (transistor = on) is V_{out} = 0.97 V and the voltage of the low level (transistor = off) is V_{out} = -0.01 V, almost reaching the theoretical voltage levels. Moreover, the gain of 2.7 (Fig. 7.3(c) inset) is comparable to values reported in literature [4]. In general, these transfer characteristics confirm that the ratio of the resistors as well as the supply voltages are appropriate and that the chosen design can be considered as functional. Concerning their dynamical behavior a typical response to a square wave input signal with a frequency of 0.05 Hz is shown in Fig. 7.3(d). The high and low levels of +1 V and 0 V are constant for a measuring period of 110 s and also a fast response of the output voltage V_{out} on V_{in}, depicted by a very small shift of the two signals, is visible. Additionally, a speed difference in switching the transistor on and back off is observable. The switching speed of the inverter is determined by graphic extraction, resulting in a switch-on time of 3.3 s to achieve 0.9 V and a switch-off time of only 0.4 s to achieve 0.1 V. An explanation for this mismatch may be the edge of the reduction front. During the reduction process it is possible that this front is moving beyond the electrolyte edge towards the drain electrode. In this case, the reverse process of oxidizing the PEDOT and returning to the conducting state of PEDOT:PSS takes more time because the electrolyte, triggering the reaction, is not in direct contact with the PEDOT. The total switching speed is 3.7 s, when the on- and off-switching times are added, being in the same order of magnitude as reported for non-printed inverters with lateral design [4].

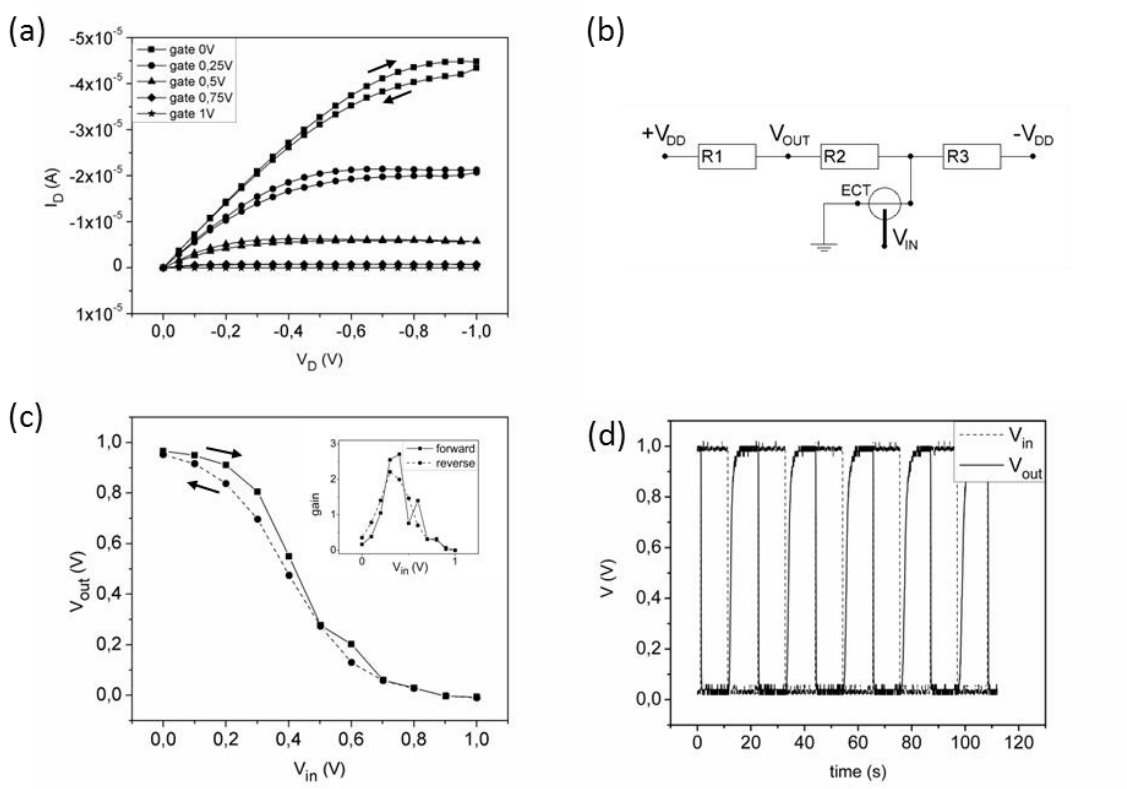


Figure 7.3: a) Output characteristic of an entirely inkjet-printed OECT with W = 250 µm, G = 500 µm, T = 70 nm and an area ratio between the gate electrode and the active area on the source-drain line of 12:1 b) circuit diagram of an electrochemical inverter c) Transfer characteristic of an entirely inkjet-printed inverter; Inset: Gain of the inverter d) Response characteristics for an electrochemical inverter

7.5 Conclusion

In summary, our investigations on lateral all-printed OECTs concerning their geometry-performance relationship have shown that the on-current increases with the PEDOT:PSS layer thickness and, less pronounced, the width and that the on-to-off ratio increases substantially with a smaller gap between gate and source-drain area. We assume that reducing the gap to even smaller dimensions will further increase the on-to-off ratio. This will be investigated in future studies with structuring methods like Nano Imprint Lithography. The ink-jet printed inverters that account for these design rules show convincing on-off switching behavior. As logic gates, they will soon form the base for more complex circuits such as flip-flops and shift registers. Since only three materials are needed to realize these circuits in a very straightforward process, they have a strong potential for mass-fabricated low-cost and disposable electronics.

7.6 Acknowledgement

Financial support from the FFG (NILaustria project cluster) is gratefully acknowledged.

References

[1] M. Berggren, D. Nilsson, N. D. Robinson, Organic Materials for Printed Electronics. *Nat. Mat*. 2007, *6*, 3.

[2] T. Johansson, L. A. A. Pettersson, O. Inganäs, Conductivity of De-Doped Poly(3,4-ethylenedioxithiophene). *Synth. Met.* 2002, *129*, 269.

[3] L. H Jimison, S. A. Tria, D. Khodagholy, M. Gurfinkel, E. Lanzarini, A. Hama, G. G. Malliaras, R. M. Owens, Measurement of Barrier Tissue Integrity with an Organic Electrochemical Transistor. *Adv. Mat*. 2012, *24*, 5915.

[4] D. Nilsson, N. Robisson, M. Berggren, R. Forchheimer, Electrochemical Logic Circuits. *Adv. Mat.* 2005, *17*, 353.

[5] M. Zirkl, A. Sawatdee, U. Helbig, M. Krause, G. Scheipl, E. Kraker, P. A. Ersman, D. Nilsson, D. Platt, P. Bodö, S. Bauer, G. Domann, and B. Stadlober, An All-Printed Ferroelectric Active Matrix Sensor Network Based on Only Five Functional Materials Forming a Touchless Control Interface. *Adv. Mat*. 2011, *23*, 2069.

[6] G. Tarabella, M. Villani, D. Calestani, R. Mosca, S. Iannotta, A. Zappettini, and N. Coppede, A single cotton fiber organic electrochemical transistor for liquid electrolyte saline sensing. *J. Mater. Chem.* 2012, *22*, 23830.

[7] F. Yan , S. M. Mok , J. J. Yu , H. L. W. Chan, and M. Yang, Label-free DNA sensor based on organic thin film transistors. *Biosens. Bioelectron*. 2009, *24,* 1241.

[8] Z. T. Zhu, J. T. Mabeck, C. C. Zhu, N. C. Cady, C. A. Batt, G. G. Malliaras, A Simple Poly(3,4-Ethylene Dioxythiophene)/Poly(Styrene Sulfonic Acid) Transistor for Glucose Sensing at Neutral pH. *Chem. Commun*. 2004, 1556.

[9] P. Lin, F. Yan, Organic Thin Film Transistors for Chemical and Biological Sensing. *Adv. Mater.* 2012, *24*, 34.

[10] D. Nilsson, M. Chen, T. Kugler, T. Remonen, M. Armgarth, and M. Berggren, Bi-stable and Dynamic Current Modulation in Electrochemical Organic Transistors. *Adv. Mat*. 2002, *14*, 51.

[11] D. A. Bernards, G. G. Malliaras, Steady State and Transient Behavior of Organic Electrochemical Transistors. *Adv. Func. Mat*. 2007, *17*, 3538.

[12] N. D. Robinson, P.-O. Svensson, D. Nilsson, M. Berggren, On the Current Saturation in Electrochemical Polymer Transistors. *J. Electrochem. Soc*. 2006, *153*, H39.

[13] D. Tu, R. Forchheimer, Self-oscillation in Electrochemical Transistors: An RLC Modeling Approach. *Solid-State Electronics* 2012, *69*, 7.

[14] L. Basirico, P. Cosseddu, A. Scidà, B. Fraboni, G.G. Malliaras, A. Bonfiglio, Electrical Characteristics of Ink-jet Printed, All-Polymer Electrochemical Transistors. *Org. Electron*. 2012, *13*, 244.

[15] M. Berggren, R. Forchheimer, J. Bobacka, P.-O. Svensson, D. Nilsson, O. Larsson, A. Ivaska, "PEDOT:PSS based electrochemical transistors for ion-to-electron transduction and sensor signal amplification," in Organic Semiconductors in Sensor Applications, vol. 107 of Springer Series in Materials Science, pp. 263–280, Springer, Berlin, Germany, (2008).

[16] D. Khodagholy, M. Gurfinkel, E. Stavrinidou, P. Leleux, T. Herve, S. Sanaur, G. G. Malliaras, High Speed and High Density Organic Electrochemical Transistor Arrays. *Appl. Phys. Lett.* 2011, *99*, 163304.

[17] M. Zhang, P. Lin, M. Yang, F. Yan, Fabrication of Organic Electrochemical Transistor Arrays for Biosensing. *Biochim. Biophys. acta* 2012, *1830*, 4402.

[18] J. Isaksson, C. Tengstedt, M. Fahlman, N. Robinson, M. Berggren, A Solid-State Organic Electronic Wettability Switch. *Adv. Mat*. 2004, 16, 316.

[19] Y.H. Kim, C. Sachse, M. L. Machala, C. May, L. Müller-Meskamp, K. Leo, Highly Conductive PEDOT:PSS Electrode with Optimized Solvent and Thermal Post-Treatment for ITO-Free Organic Solar Cells. *Adv. Func. Mat*. 2011, *21*, 1076.

8. Nanoimprint Lithography-Structured Organic Electrochemical Transistors and Logic Circuits

8.1. Abstract

We report on the fabrication of organic electrochemical transistors structured by nanoimprint lithography. The devices were scaled down as a consequent result of our previous findings for inkjet-printed transistors, where a reduced source-drain width and a shorter distance to the gate resulted in higher onto-off current ratio. We could show that these findings also prove true for transistors with feature sizes below 10 µm. Furthermore, we fabricated inverters and NAND gates with switching times below one second. These logic gates mark an important step for organic electrochemical transistors towards their usability in more complex logic circuits.

8.2. Introduction

There are two main concepts to build organic transistors: the organic thin-film transistor (OTFT) and the organic electrochemical transistor (OECT), the latter being studied in this work. Using an electrolyte and the well-known conducting and printable polymer PEDOT:PSS (poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate)), electrochemical switching over five orders of magnitude via a voltage-induced reversible redox process has been shown and exploited in OECTs and circuits thereof [1]. Naturally, their performance depends heavily on the used materials, but different geometry parameters also play a significant role [2–4]. We could show for all-inkjet-printed OECTs that the on-to-off current ratio can be improved by reducing the width of the source-drain electrode (width W) and its distance to the gate (gap G) [5] (compare Fig. 8.1a). In this work, we aim to further exploit this relation by fabricating devices with a higher resolution than provided by inkjet printing. Thus it is necessary to pattern the PEDOT:PSS electrodes with minimum feature sizes of 10 µm and below. Different approaches to achieve this goal have been shown in literature. One technique is to rely on a previous surface treatment of the substrate, using structured hydrophobic layers [6], CF4 etching [7] or self-assembled monolayers and V-shaped, embossed groves [8]. The methods are promising for producing feature sizes well below one micrometer, but the first two require a very good control over the drop volume to achieve thin layers while the third one requires a quite complicated, high resolution surface treatment. PEDOT:PSS can also be mechanically structured, either by laser ablation [9], oxygen plasma etching using a stainless steel mask [10] or photolithography and lift-off [11]. However, in the context of low cost production a roll-to-roll compatible, parallel structuring technique would be advantageous. Accordingly we

introduce UV-based nanoimprint lithography (UV-NIL) as a high resolution, high throughput patterning technique to structure PEDOT:PSS. Devices with a gap of G = 6 µm and a width of W = 13 µm were fabricated and measured. Full usability of the NIL-structured electrochemical transistors (NIL-OECTs) in higher integrated logic circuitry is demonstrated on the basis of inverters and NAND gates. Furthermore, the transistors are compared to our previously published all-inkjet-printed OECTs in terms of static and dynamic behavior.

8.3. Experimental

The OECTs presented here consist of PEDOT:PSS (Clevios P Jet HC by Heraeus) an inkjet printable polymer electrolyte and silver ink (Cabot CCI-300) for the contact pads. The electrolyte formulation consists of: 51 wt.% deionized water, 33 wt.% Poly(sodium-4-styrene sulfonate), 8 wt.% D-sorbitol, and 8 wt.% glycerol (85 wt.%) [12]. As shown in Figure 8.1b-g on an SF6 plasma treated PET foil (Melinex ST725 PET foil from DuPont) the PEDOT:PSS electrodes are pre-structured by inkjet printing using a Dimatix DMP 2800 inkjet printer. The substrate is held at room temperature during the printing process. The PEDOT:PSS film is dried on a hotplate held at 100°C for 10 minutes. Next, a UV curable imprint resist [13] is spin-coated on top of the electrodes at 2000 rpm for 30 seconds. The resist is structured by UV-NIL using a silicon stamp and curing the resist through the substrate with an EVG 620 mask aligner. After separating the stamp from the sample, the resist acts as an etch mask. With an oxygen plasma dry etch in a reactive ion etcher from Oxford Instruments the pattern is transferred from the resist into the PEDOT:PSS lines. The sample is submersed in AZ 726 MIF photo developer (microchemicals GmbH) for 15 minutes and rinsed with IPA to remove the resist. To improve the electrical connection to the measurement tips, Ag contact pads are inkjet-printed onto the electrodes at room temperature and cured at 110°C for 10 minutes on a hotplate. As a last step the electrolyte is applied, again using inkjet printing [14].

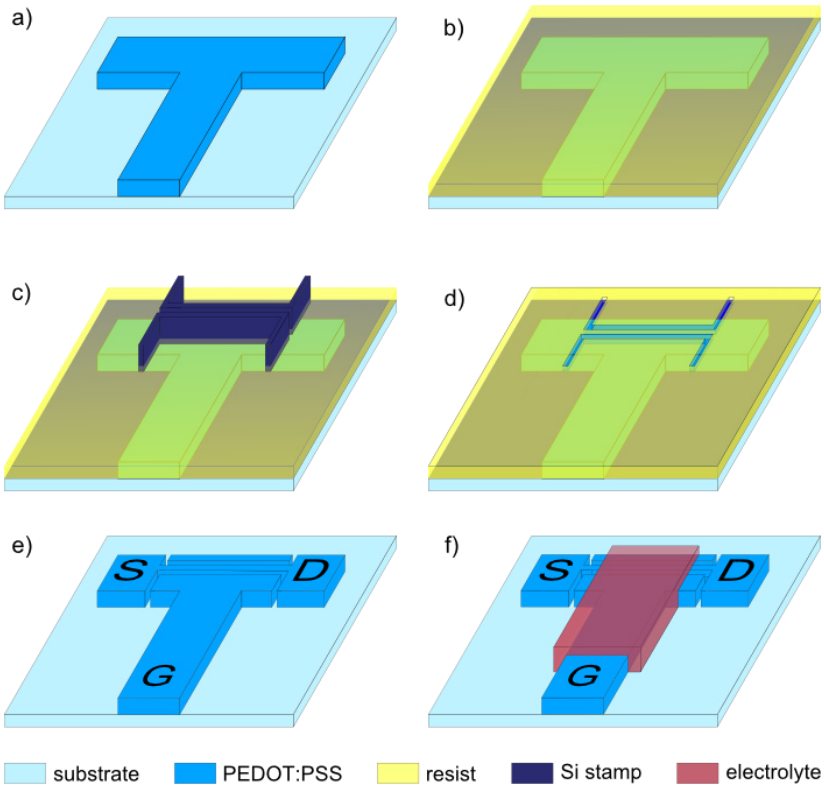


Figure 8.1.: Schematic top view (a) and NIL-process scheme (b-g) of a lateral electrochemical transistor; Definition of the gap between the gate and the source-drain line G and the width of the source-drain line W (a). On a sample with pre-structured PEDOT:PSS (b) an imprint resist is applied by spin coating (c). Then a Si stamp with the wanted features is pressed into the resist (d), the resist is UV-cured through the substrate and the stamp is removed, leaving an etch-mask for the underlying PEDOT:PSS (e).The etch pattern is transferred using an oxygen plasma etch and the resist is wet chemically removed (f). As a last step the electrolyte is inkjet printed on the sample (g).

8.4. Results and Discussion

8.4.1. Nanoimprint lithography structured electrochemical transistor and logic gates

From Figure 8.2, showing the output characteristics of a typical NIL-OECT with a gap of 6 µm and a width of 13 µm, the on current I_{ON} (I_D at V_{GS} = 0 V, V_{DS} = −1 V), the off current I_{OFF} (I_D at V_{GS} = 1 V, V_{DS} = −1 V), and the on-to-off current ratio I_{ON}/I_{OFF} can be extracted. The shown device reveals $I_{ON} = 6.4 \times 10^{-7}$ A, $I_{OFF} = 1.0 \times 10^{-10}$ A and $I_{ON}/I_{OFF} = 6.4 \times 10^{3}$. Peak devices showed an even higher ratio of up to 1×10^{4}. The maximum switching current ($I_{G,max}$) is $I_{G,max} = 1 \times 10^{-10}$ A and the largest hysteresis at V_{GS} = 0 V reaches 13 % of I_{ON}. The hysteresis is a result of the ions present in the electrolyte. As a next step, all printed NIL-structured OECT-based inverters using the circuit design shown in Figure 8.3a were investigated. For the resistors inkjet-printed

PEDOT:PSS is used. In order to reduce the footprint of the circuit, the resistors are also structured by NIL. Ideally, the circuit acts as a voltage divider between R3 and R1 + R2 for a switched off OECT or R3 and R2 + R_{ON} for a switched-on OECT. In reality, the parallel resistances of R_{ON} and R_{OFF} (R_{OFF} = R_{ON} at V_{GS} = 1 V) have to be taken into account. For the proper function it is important that R_{OFF} > R1 > R_{ON}. Considering the on- and off-resistances of the transistor (compare Fig.8.2) (R_{ON} = 875 kΩ, R_{OFF} = 3 GΩ) and symmetrical supply voltages (V_{DD} = 3 V, $-V_{DD}$ = −3 V) resistances of R1 : R2 : R3 = 15 MΩ : 25 MΩ : 40 MΩ should result in good inverter performance. Alternatively the supply voltages can be adjusted to compensate for a mismatch in the resistance ratios. One solid NIL-structured resistor line was fabricated and divided into the needed length parts by inkjet-printed Ag contact pads. For the inverter shown in Figure 8.3c the resistances revealed R1 : R2 : R3 = 6 MΩ : 16.6 MΩ : 37.7 MΩ and the supply voltages were adapted to V_{DD} = 4.0 V and $-V_{DD}$ = −2.1 V respectively. The device has clear plateaus at the high and the low level. The voltage of the high level (V_{Output} at V_{Input} = 0 V) is $V_{Output,high}$ = 0.94 V and the voltage of the low level (V_{Input} = 1 V) is $V_{Output,low}$ = −0.03 V. This result is in good agreement with the target voltage levels of $V_{Output,high}$ = 1 V and $V_{Output,low}$ = 0 V. The extracted gain of 3.8 (Fig. 8.3c inset) is comparable to values reported in literature [1, 5].

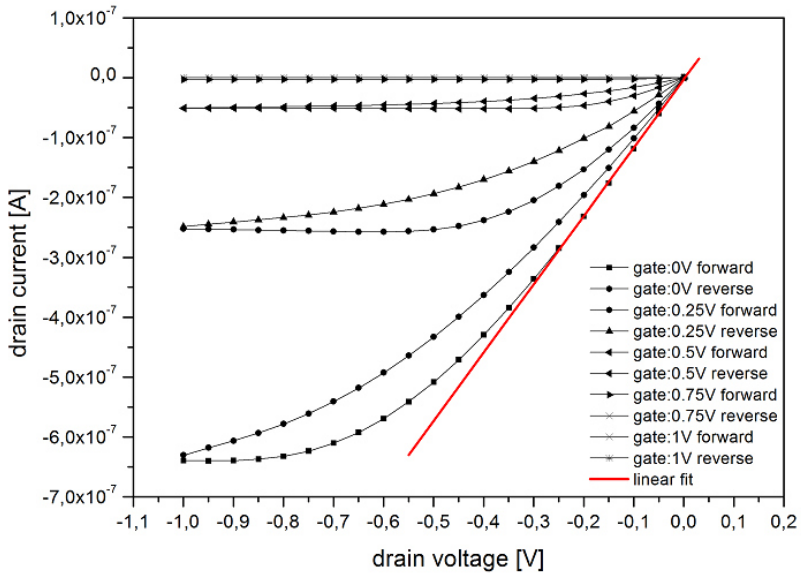


Figure 8.2.: Output characteristics of a NIL-structured electrochemical transistor. The width of the source-drain line W = 13 µm and its distance to the gate G = 6 µm. From the slope of the linear fit R_{ON} = 875 kΩ can be extracted.

To show that NIL-structured OECTs can be used for all Boolean logic operations, NAND gates are fabricated [15] (Fig. 8.3b). The dynamic response of the NAND gate (Fig. 8.3d) shows good

logic switching behavior, the $_{VOutput,high}$ value (representing Logic 1) shows a slight instability with plateau values in the range of $V_{Output,high}$ =1.01 V to 0.86 V, however there is still a clear distinction to the low level state (Logic 0) being $V_{Output,low}$ = 0.02 V. The switching time was also measured, revealing a mismatch between switching the device from the on- to the off-state (t_{Off} = 0.03 s) and back on again (t_{On} = 0.9 s) (Fig. 8.4c). There are three different artifacts visible in the NAND characteristics that can also be found in literature [1]. The sharp peak labeled "1" in Figure 8.3d, when OECT1 is switched on and OECT2 is switched off, is a result of the mismatch of the switching times. As stated above, OECT2 switches off over 0.03 s, so for a short time both transistors are off. This results in the visible short drop of V_{Output} towards the logic 0 state. The ΔV_{Output} = 0.2 V drop in the logic 1 level when OECT1 is on and OECT2 is off (labeled "2" in Fig. 8.3d) is a result of the higher R_{ON} of OECT1 (and thus the higher parallel resistance to $R1$). The output characteristics of both OECTs used in the NAND gate can be found in the Appendix of this chapter (Fig. 8.5). The third artefact appears whenever OECT1 is switching off, especially pronounced when OECT2 is also off (labeled "3" in Fig. 8.3d). It is not a stable artefact but varies both in height and transistor number from device to device. It is only visible when the NIL-OECT switches off and in all devices most prominent when both transistors are switched off. The artefact is thought to be a result of parasitic capacitances between the gate and the source-drain line. When both transistors are off the parasitic capacitance is discharged through the voltage divider and thus results in a peak in V_{Output}. This is in good agreement with the smaller change in V_{Output} when only OECT1 switches off, since then part of the parasitic charge can flow over OECT2 to ground and the voltage divider is less affected.

8.4.2. Comparison with all inkjet-printed organic electrochemical transistors

When compared to the all-inkjet-printed transistors published elsewhere the on-current is two orders of magnitude lower for the NIL-structured devices (compare Fig. 8.4a,b) [5]. This is a result of the decreased device geometries, but also the process steps performed on top of the PEDOT:PSS. I_{ON} is lowered because the width of the S-D line is one order of magnitude smaller. Also the sheet resistance of the PEDOT:PSS lines rises significantly due to the exposure to the NIL process steps. A control experiment, where the sheet resistance of all-inkjet-printed PEDOT:PSS lines has been measured before and after being exposed to application, curing and stripping of the resist, revealed an increase from about 1 kΩ/square to 300 kΩ/square. On the other hand I_{ON} is increased because the length of the source-drain line is reduced from 20 mm to 1 mm. The PEDOT:PSS thickness is in the same order of magnitude for both the all-inkjet-

printed and the NIL-structured devices, being around 100 nm. Despite the lower on-current the on-to-off ratio has improved up to one order of magnitude. This represents a further continuation of the trend that reducing both width and gap has a positive influence on the transistor performance.

Concerning the dynamic behavior of the OECTs, the NIL-structured transistors show an overall switching frequency of approximately 1.1 Hz. Compared to the 0.27 Hz of the inkjet-printed OECTs the switching speed only improved by a factor of four (compare Fig. 8.4c). This indicates that an effect different from the dimensions W and G seems to dominate the switching speed for small geometry devices. The reduction front moving beyond the electrolyte area and towards the drain electrode when switching the OECT off may be this dominant effect [16]. When switching the device back on, this area takes a relatively long time to be oxidized again. This is supported by the dynamic behavior, which is heavily dominated by the time needed to switch the device from the off to the on-state. While in all inkjet-printed OECTs the switching time ratio is t_{On}/t_{Off} = 8.3, the NIL-OECTs show a ratio of t_{On}/t_{Off} = 30. This explanation can be further backed by literature as switching speeds over 1 Hz have to the best of our knowledge only been reported for device geometries where this reduction front is suppressed (e.g. by replacing the PEDOT:PSS not covered by electrolyte with a conductor [3, 17]) or not affecting the switching at all (e.g. in a vertical electrochemical transistor design [18]).

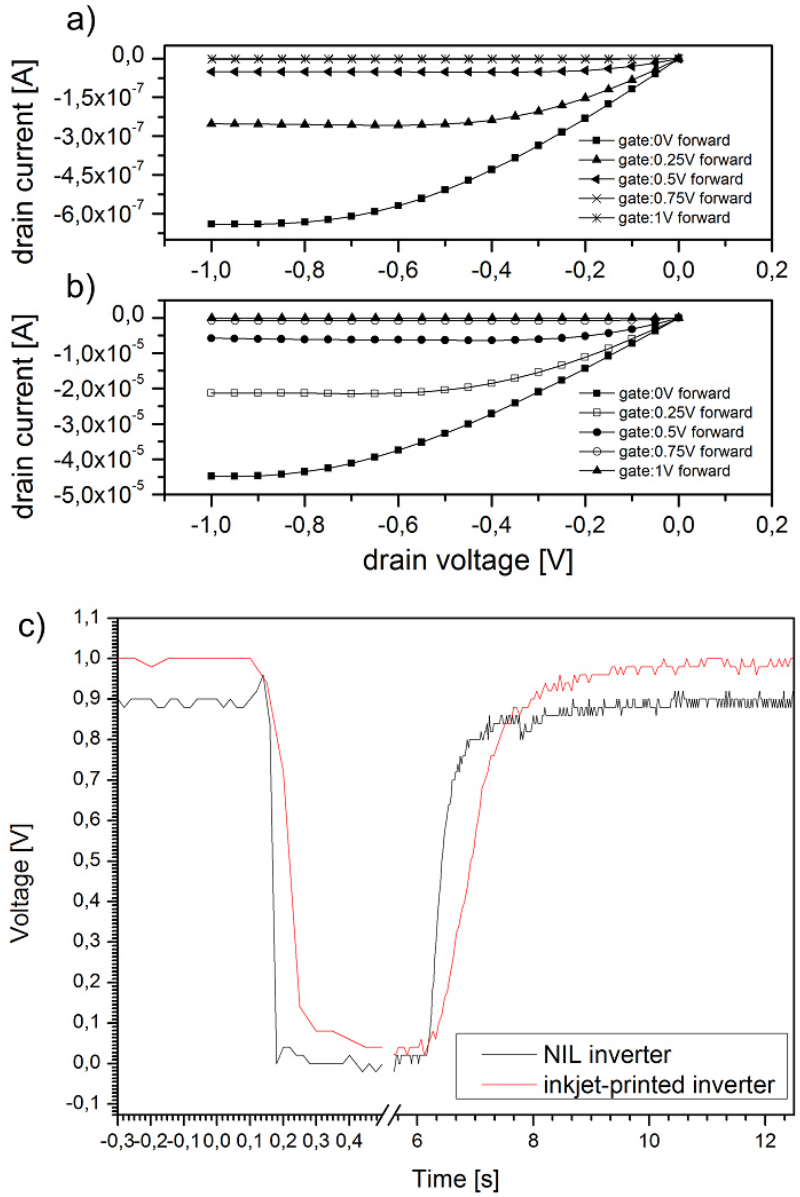


Figure 8.4.: Output characteristics of a NIL-structured (a) and an inkjet-structured (b) OECT; (c) Dynamic response of electrochemical inverters to a square wave signal. The switching times can be graphically extracted and read t_{Off} = 0.9 s, t_{On} = 3.3 s (inkjet) and t_{Off} = 0.03 s, t_{On} = 0.9 s (NIL).

8.5. Conclusion

To conclude we could show that it is possible to use nanoimprint lithography for the structuring of PEDOT:PSS and fabricate fully-printed organic electrochemical transistors as well as logic circuits. By reducing the device geometry both the on-to-off current ratio and the switching speed were improved. The results indicate that further size reduction might not lead to better device performance, as other influences beyond the geometry start to dominate the dynamic transistor behavior. Future work will deal with the determination and evaluation of

these influences (e.g. by suppressing the reduction front, modulating the gate area or comparing different electrolytes) for different device geometries. Nevertheless, we could show that lateral electrochemical transistors can exhibit good switching speeds and high on-to-off current ratio. With the successful fabrication of logic gates future application as flip-flops or shift registers and more complex devices with electrochromic displays can be addressed.

8.6. Appendix

Figure 8.5 shows the output characteristics of the two NIL-OECTs used for the NAND gate. The on resistances can be calculated from the slope of the linear regime. For the devices R_{ON} equals $R_{ON,OECT1}$ = 3.9 MΩ and $R_{ON,OECT2}$ = 1.8 MΩ respectively.

8.7. Acknowledgment

T. Rothlander would like to thank E. Zojer for fruitfull discussions and advice.

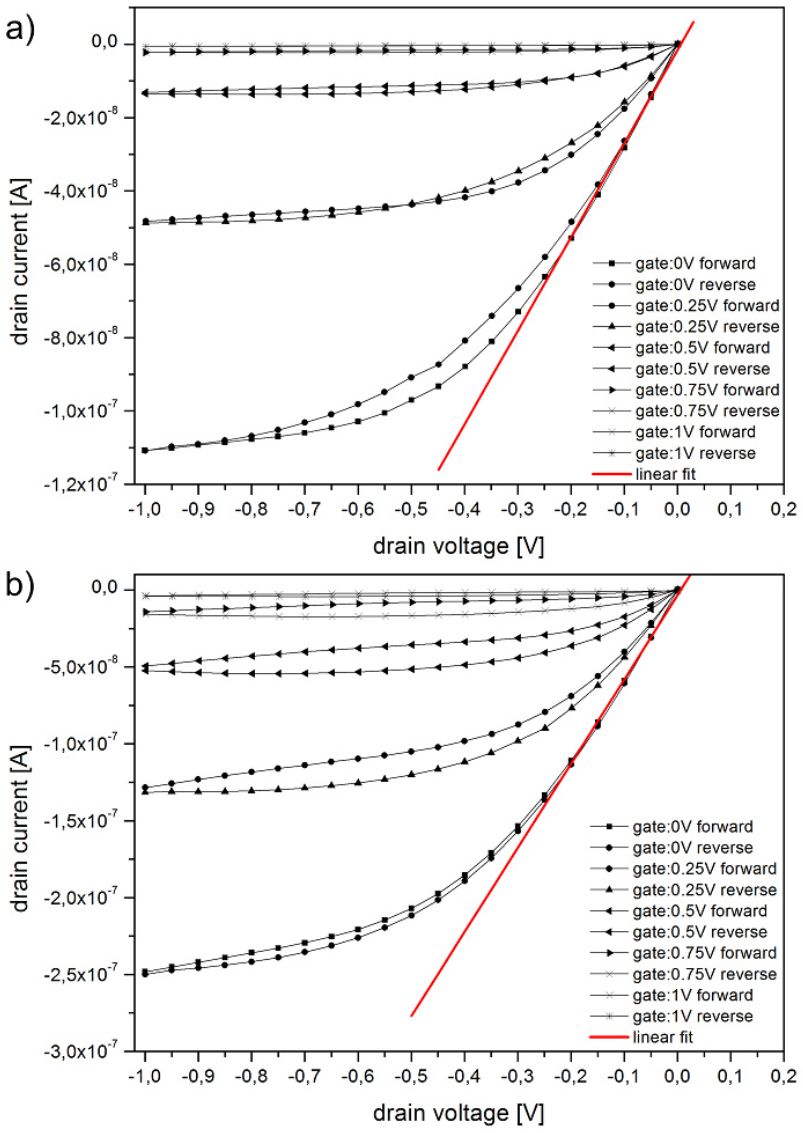


Figure 8.5.: Output characteristics of (a) OECT1 and (b) OECT2 used for the NAND-gate.

References

[1] D. Nilsson, N. Robinson, M. Berggren, R. Forchheimer, Electrochemical Logic Circuits. *Adv. Mater.* 2005, *17,* 353–358.

[2] L. Basiricò, P. Cosseddu, A. Scidà, B. Fraboni, G.G. Malliaras, A. Bonfiglio, Electrical characteristics of ink-jet printed, all-polymer electrochemical transistors. *Org. Electron.* 2012, *13,* 244–248.

[3] D. Khodagholy, M. Gurfinkel, E. Stavrinidou, P. Leleux, T. Herve, S. Sanaur, G. G. Malliaras, High speed and high density organic electrochemical transistor arrays. *Appl. Phys. Lett.* 2011, *99*, 163304.

[4] M. Berggren et al. PEDOT:PSS-Based Electrochemical Transistors for Ion-to-Electron Transduction and Sensor Signal Amplification. *Organic Semiconductors in Sensor Applications*. Ed. by D. A. Bernards, G. G. Malliaras, and R. M. Owens. Springer Berlin Heidelberg, 2008, pp. 263– 280.

[5] P. C. Hütter, T. Rothländer, A. Haase, G. Trimmel, B. Stadlober, Influence of geometry variations on the response of organic electrochemical transistors. *Appl. Phys. Lett.* 2013, *103*, 043308.

[6] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, E. P. Woo, High-Resolution Inkjet Printing of All-Polymer Transistor Circuits. *Science* 2000, *290*, 2123–2126.

[7] C. W. Sele, T. von Werne, R. H. Friend, H. Sirringhaus, Lithography-Free, Self-Aligned Inkjet Printing with Sub-Hundred-Nanometer Resolution. *Adv. Mater*. 2005, *17,* 997–1001.

[8] N. Stutzmann, R. R. H. Friend, H. Sirringhaus, Self-aligned, vertical channel, polymer field effect transistors. *Science* 2003, *299*, 1881.

[9] M. Schrödner, R.-I. Stohn, K. Schultheis, S. Sensfuss, H.-K. Roth, Polymer field effect transistors made by laser patterning. *Org. Electron.* 2005, *6*, 161–167.

[10] A. Colsmann, F. Stenzel, G. Balthasar, H. Do, U. Lemmer, Plasma patterning of Poly(3,4-ethylenedioxythiophene): Poly(styrenesulfonate) anodes for efficient polymer solar cells. *Thin Solid Films* 2009, *517*, 1750–1752.

[11] J. Huang, R. Xia, Y. Kim, X. Wang, J. Dane, O. Hofmann, A. Mosley, A. J. de Mello, J. C. de Mello, D. D. C. Bradley, Patterning of organic devices by interlayer lithography. *J. Mater. Chem.* 2007, *17*, 1043.

[12] J. Isaksson, C. Tengstedt, M. Fahlman, N. Robinson, M. Berggren, A Solid-State Organic Electronic Wettability Switch. *Adv. Mat*. 2004, 16, 316.

[13] C. Auner, U. Palfinger, H. Gold, J. Kraxner, A. Haase, T. Haber, M. Sezen, W. Grogger, G. Jakopic, J.R. Krenn, G. Leising, B. Stadlober, Residue-free room temperature UV-nanoimprinting of submicron organic thin film transistors. *Org. Electron.* 2009, *10*, 1466–1472.

[14] T. Rothländer, H. Gold, A. Haase, G. Jakopic, P. Hartmann, B. Stadlober, P. C. Hütter, Nanoimprinted Organic Electrochemical Transistors. *Proceedings of the Eurodisplay 2013*, pp. 179–180.

[15] H. Sheffer. A set of five independent postulates for Boolean algebras, with application to logical constants. *Transactions of the American Mathematical Society* 1913, 14, 481–488.

[16] R. Mannerbro, M. Ranlof, N. Robinson, R. Forchheimer, Inkjet printed electrochemical organic electronics. *Synth. Met.* 2008, *158,* 556–560

[17] P. Andersson Ersman, D. Nilsson, J. Kawahara, G. Gustafsson, M. Berggren, Fast-switching all-printed organic electrochemical transistors. *Org. Electron.* 2013, *14*, 1276–1280.

[18] M. Taniguchi, T. Kawai, Vertical electrochemical transistor based on poly(3-hexylthiophene) and cyanoethylpullulan. *Appl. Phys. Lett.* 2004, *85*, 3298.

9. All Screen Printed Logic Gates Based on Organic Electrochemical Transistors

9.1 Abstract

We report on the fabrication and characterization of entirely screen printed integrated logic circuits based on organic electrochemical transistors on flexible PET substrates. The transistors are based on poly(3,4-ethylenedioxithiophene) poly(styrenesulfonate) and operate at a voltage of 1.5 V. Together with screen printed resistors the printed transistors were used as the building blocks for inverters, NAND-gates, flipflops and a 2-bit shift register. Dynamic characterizations of these logic gates needing only five different inks reveal a high reproducibility of the measured devices' output signals. These results clearly indicate the high uniformity and reproducibility of the screen printed transistors and resistors, emphasizing their applicability for integrated circuitry.

9.2 Introduction

Organic electrochemical transistors (OECTs) have received considerable attention in recent years. The function principle has been studied in several publications mathematically describing the current saturation [1] and examining the gate electrode's (faradaic or capacitive) working regime [2]. A model of the working principle has been presented by Bernards and Malliaras, describing it as a combination of an ionic and electronic circuit [3]. The feature that both ionic and electronic charge carriers are used in OECTs makes them particularly interesting for sensing and for applications at the interface with biology [4]. A comprehensive overview of OECTs and OTFTs for chemical and biological sensing is provided in literature [5]. Even applications as advanced as in-vivo recordings of brain activity have been demonstrated [6]. Nevertheless, the use of OECTs is not limited to sensing. Their additional advantages like the low operating voltage, the simple design allowing for a fabrication by additive printing techniques and the possibility to use large area and flexible substrates make them attractive for a large variety of applications. In this context the successful integration of OECTs in basic electronic circuits [7,8], smart textiles [9], electrochromic displays [10] and active-matrix physical sensor circuits was reported [11]. The latter uses OECTs for the readout of a physical sensor, combining it with a simple two-color electrochromic display. To date more complex organic electronic circuits [12] were presented only for organic thin film transistors (OTFT)– examples here are integrated temperature sensors [13], a piezoelectricity based pedometer [14] and the control-circuit of an e-ink display [15]. Further impressive examples

demonstrating complex circuits using OTFTs are an 8-bit microprocessor, to some extent being comparable to a silicon Intel 4004 early-days processor [16] that has recently been advanced [17], a 240-stage shift register employing 13440 OTFTs [18], the design of a high-frequency AM demodulator in a printed complementary organic technology [19] and an organic smart sensor system on foil [20]. However, to the best of our knowledge complex integrated circuits based on OECTs were not reported so far. A disadvantage of OTFT based circuits is the often complicated fabrication process, including sophisticated equipment and corrosive chemicals for the subtractive steps. Accordingly, circuitry based on OECTs with their simple design and fabrication could be advantageous, especially when combined with applications that require large-areas and flexible substrates.

The robust and fairly simple to process logic circuits presented in the work on hand mean an important step in this direction. They are fabricated entirely by screen printing and are based on electrochemical transistors with an operating voltage of 1.5 V. The printed transistors and resistors consist of only three materials. For combining these basic components to integrated logic circuits only two additional printable materials are needed for the wiring and the isolation of interconnections. As a final step, printed flipflops and 2-bit shift registers were demonstrated as basic building blocks for a printed sequential logic component. These devices add the possibility to store an input signal, allowing for the use of OECTs in memory circuits.

9.3 Experiment

All OECTs are fabricated on PET foil (Melinex ST505) using PEDOT:PSS (Clevios S V3), a water-based UV-curable polymer electrolyte and carbon paste (DuPont 7102). The voltage dividers for the inverters also consist of PEDOT:PSS (Clevios S V3) and carbon paste (DuPont 7102). All the wiring is based on screen printing of a silver paste (DuPont 5000). To facilitate the unavoidable crossing of the silver lines a metal interlayer isolation is necessary. A screen printable and UV-curable dielectric based on polyurethane acrylate is used. All materials are processed by a Technical Industrial Co., Ltd. SFM 550 screen printer. The parameters of the used screens are 100-40 mesh for the PEDOT:PSS and silver layer, 120-34 mesh for the dielectric and carbon paste layer and 30-120 mesh for the electrolyte layer.

As a first step the carbon pads, connecting the transistor electrodes to the silver wiring and defining the resistors for the voltage dividers, are printed. Next the PEDOT:PSS electrodes and resistor lines are printed, followed by the first set of silver wiring. After each printed layer, the paste is cured in an oven at 100°C for 10 minutes. To allow for crossings in the wiring, a

dielectric is necessary. Two layers are printed wet on wet and cured under UV-light for 4 minutes. The process is repeated to increase the dielectric thickness, further reducing the parasitic capacitance of the crossing wires as well as the probability of short circuits. The second set of silver lines, completing the wiring, is printed and dried at 100°C for 10 minutes in an oven. Finally two layers of electrolyte are printed wet on wet and cured under UV-light for 8 minutes. For the electrical characterizations a Suess Microtec probe station, a MB Technologies parameter analyzer and, for the dynamic measurements, a Tektronix TDS 2014 B oscilloscope are used. All measurements are carried out under ambient conditions.

9.4 Results and Discussion

Fig. 9.1(a) shows a photograph of a typical screen-printed OECT with a 0.5 mm wide and 3 mm long source/drain poly(3,4-ethylenedioxithiophene) poly(styrenesulfonate) (PEDOT:PSS) line. Since uniformity is desired, all transistors in the circuit have equal dimensions. In Fig. 9.1(b) the output $I_D(V_D)$ characteristics (drain current vs. drain voltage) of such a transistor are depicted, revealing an on-current of $I_{ON} = -2.38 * 10^{-4}$ A at a gate voltage $V_G = 0$ V and an off-current of $I_{OFF} = -3.17*10^{-8}$ A at $V_G = 1.5$ V, resulting in an on-to-off ratio of $I_{ON}/I_{OFF} = 7.5*10^4$. Additionally, the transistor's on-resistance (R_{ON}) is extracted from the slope of the linear part of the $I_D(V_D)$ -curve at $V_G = 0$ V [red line in Fig. 9.1(b)]. In the inset of Fig. 9.1(b), the variation of the as-determined R_{ON} for 36 OECTs is presented as a boxplot indicating a narrow and symmetric distribution of the R_{ON} values with 1st quartile and 3rd quartile values of 3.84 kΩ and 4.33 kΩ respectively, and a median of 4.03 kΩ.

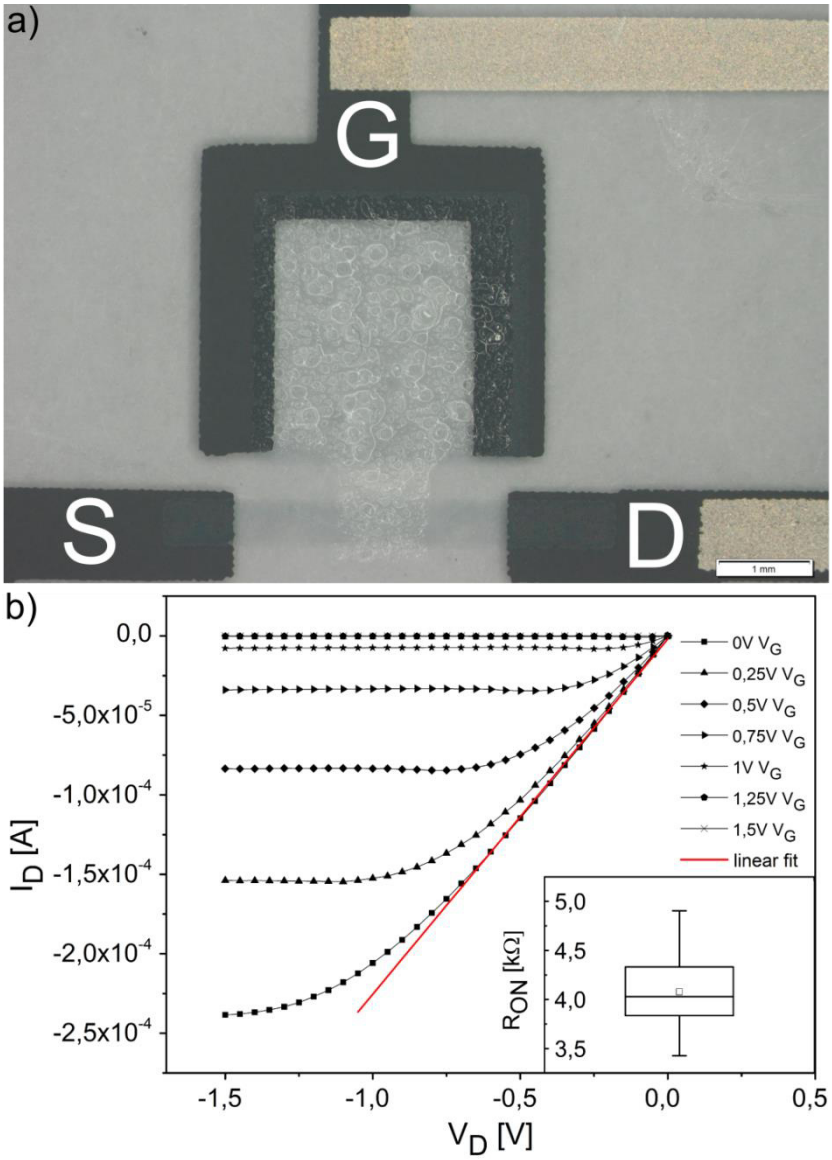


Figure 9.1. (a) Photograph of a screen printed OECT, gap between the gate electrode (G) and the source/drain line (S/D) is 0.4 mm, active areas on G and on S/D of 2.8 mm * 2.8 mm and 1 mm * 0.5 mm respectively (b) $I_D(V_D)$ of a screen printed OECT; from the fit of the linear part of the V_G = 0V curve the on-resistance R_{ON} is extracted; inset: Box-Plot depicting the distribution of R_{ON} measurements of 36 OECTs.

R_{ON} is very important for the design of inverters based on electrochemical transistors. Such inverters are built from an OECT and a voltage divider [Fig. 9.2(a)], covering an area of 3.2 cm^2 including all the wiring. The voltage divider consists of two supply voltages ($+V_{DD}$, $-V_{DD}$) and three resistors (R_1, R_2, R_3). In an idealized device, two states of the inverter are observed: The first state is the so-called high level state, when logic 0 is applied and the transistor is switched on. Here R_{ON} is assumed to be so much smaller than (the parallel) R_1 that R_1 is negligible, resulting in the equivalent circuit depicted in Fig. 9.2(b). Here V_{OUT} depends on the ratio between resistors $R_2 + R_{ON}$ and R_3, the relevant voltages being the positive supply voltage $+V_{DD}$

and ground. The second state is the low level state, when logic 1 is applied to V_{IN} and the transistor is switched off. Here it is assumed that R_{OFF} exceeds R_1 so much that R_{OFF} can be neglected. This state is represented by the equivalent circuit shown in Fig. 9.2(c). In this case V_{OUT} depends only on the three resistors (R_1, R_2, R_3) and the supply voltages ($+V_{DD}$, $-V_{DD}$).

In reality these idealized cases are not sufficient to describe the inverter. The parallel resistances of R_{OFF} and, to a greater extend, R_{ON} with respect to R_1 have to be taken into account. To include these parallel resistances into the dimensioning of the inverter the superposition principle is used (compare [21]). All the calculated voltage levels presented in this work are based on this principle. A typical voltage transition curve for a screen printed electrochemical inverter is plotted in Fig. 9.2(d) revealing a high level voltage of $V_{OUT,HIGH}$ = 1.25 V at V_{IN} = 0 V and a low level of $V_{OUT,LOW}$ = 0.02 V at V_{IN} = 1.5 V. In the following, an input voltage of V_{IN} = 0 V will be referred to as logic 0 and an input voltage of V_{IN} = 1.5 V as logic 1. The inverter has a gain of 3.3 which is a common value for inverters based on OECTs [7, 8, 22]. The average noise-margin of eight inverters, determined by the maximum equal criteria (MEC) [23], is 0.31 V with a standard deviation of 0.013 V, corresponding to 41.3 % of $V_{IN}/2$. The voltage levels are in good agreement with calculated levels using mean values for R_{ON} (4.1 kΩ), R_1 (25.4 kΩ), R_2 (76.6 kΩ) and R_3 (101.1 kΩ) as well as supply voltages of $+V_{DD}$ = 3.5 V and $-V_{DD}$ = -3.5 V (as used for all circuits presented in this work). Calculations deliver values of $V_{OUT,HIGH,CALC}$ = 1.28 V for the high level and $V_{OUT,LOW,CALC}$ = 0.016 V for the low level. The difference between the optimum high level voltage of 1.5 V and the level obtained is a result of a non-optimized voltage divider geometry for the obtained on-resistance of the transistors. Nevertheless, as will be proven later, the achieved output levels are sufficient for the use of these inverters in integrated logic circuits. For the proper function it is important that $R_{OFF} > R_1 > R_{ON}$ and that $(R_1+R_2):R_3 = 1$. The off-resistance is R_{OFF} = 67.6 MΩ [extracted from the slope of the V_G = 1.5 V curve of the output characteristics in Fig. 9.1(b)] and is thus several orders of magnitude larger than R_1. Considering this, three important parameters for a proper function of an inverter can be identified: i) the on-resistance R_{ON} of the transistor, ii) the resistor R_1 of the voltage divider and iii) the ratio between the sum of the resistors R_1+R_2 and the resistor R_3.

The stability of these parameter values is of great importance for the integration of such inverters in more complex circuits. The high stability of R_{ON} (~ 5% variation) is illustrated by the box-plot shown as an inset of Fig. 9.1(b). To determine the distribution of the resistor values R_1, R_2 and R_3, 30 resistor chains are measured [Fig. 9.2(e)]. Similar to R_{ON} the values of R_1 show

a very small variation with 1st quartile and 3rd quartile values of 24.3 kΩ and 26.6 kΩ and a median of 25.8 kΩ. Comparing R_1 and R_{ON}, the ratio of the 1st quartile values and the 3rd quartile values is 6.3 and 6.1, depicting that R_1 is significantly larger than R_{ON} and that the value of the ratio stays approximately the same across the distribution. Also very promising is the narrow distribution of the resistor ratio $(R_1+R_2):R_3$ with 1st quartile and 3rd quartile values of 0.99 and 1.03 and a median of 1.01 (< 2% variation), implying consistent R_2 and R_3 values. In summary, all key resistor parameters are in the desired range and show very narrow distributions for a sample size of 30.

Fig. 9.2(f) shows the dynamic response (voltage V over time t) of 18 inverters to a square wave input voltage signal. The almost identical output signals depict the high uniformity of the different samples. The arithmetic mean value of the high level (V_{IN} = logic 0) is $\bar{x}_{HIGH}$ = 1.21 V with a standard deviation of σ_{HIGH} = 0.055 V. For the low level (V_{IN} = logic 1) the results are $\bar{x}_{LOW}$ = 0.002 V and σ_{LOW} = 0.038 V. These values are in good agreement with the calculated values of $V_{OUT,HIGH,CALC}$ = 1.28 V and $V_{OUT,LOW,CALC}$ = 0.016 V. The dynamic characterizations reveal a switching speed of 1.12 s for switching the inverter on and of 0.26 s for switching it off, resulting in a total switching time of 1.38 s or 0.72 Hz. These values are in the range of electrochemical inverters published earlier [7]. Note that the inverter noise margin distribution can also be used to predict the yield of more complex circuits than presented in this work [18, 24].

The next step was the realization of a fully printed NAND gate. The equivalent circuit of a NAND gate using electrochemical inverters is found in the appendix [Fig. 9.5(a)]. Compared to the inverter circuit a second OECT, also connected to the voltage divider, is required, expanding the covered area to 4.2 cm^2. Dynamic measurements of 16 NAND gates are shown in Fig. 9.2(g). Despite the increased complexity of the circuit compared to the inverters, the obtained NAND gates show very high uniformity. The high levels ($V_{IN1} \neq V_{IN2}$, $V_{IN1} = V_{IN2}$ = logic 0) and low levels ($V_{IN1} = V_{IN2}$ = logic 1) are comparable to the inverter levels ($\bar{x}_{HIGH}$ = 1.21 V with σ_{HIGH} = 0.033 V, $\bar{x}_{LOW}$ = 0.005 V with σ_{LOW} = 0.042 V). The high levels of the NAND gates show instability. An additional rise of V_{OUT} is visible [marked “A” in Fig. 9.2(g)] when both transistors are switched on ($V_{IN1} = V_{IN2}$ = logic 0) and can be explained by basic resistor theory using Ohms law. When two resistors are connected in parallel, the resulting resistance is lower than the value of the smaller resistance. In this way the resistance R_1 of the voltage divider is bridged

more efficiently when both OECTs are on, resulting in a shift of the high level towards an increased voltage. Including this lowered on-resistance in the output level calculations, we obtain a value of $V_{OUT,HIGH,CALC} = 1.38$ V which is in good agreement with the observed arithmetic mean value for the elevated high level of $\bar{x}_{HIGH} = 1.33$ V for the 16 NAND gates. This high level shift is visible for all the integrated logic circuits presented in this work and can be attributed to the same effect.

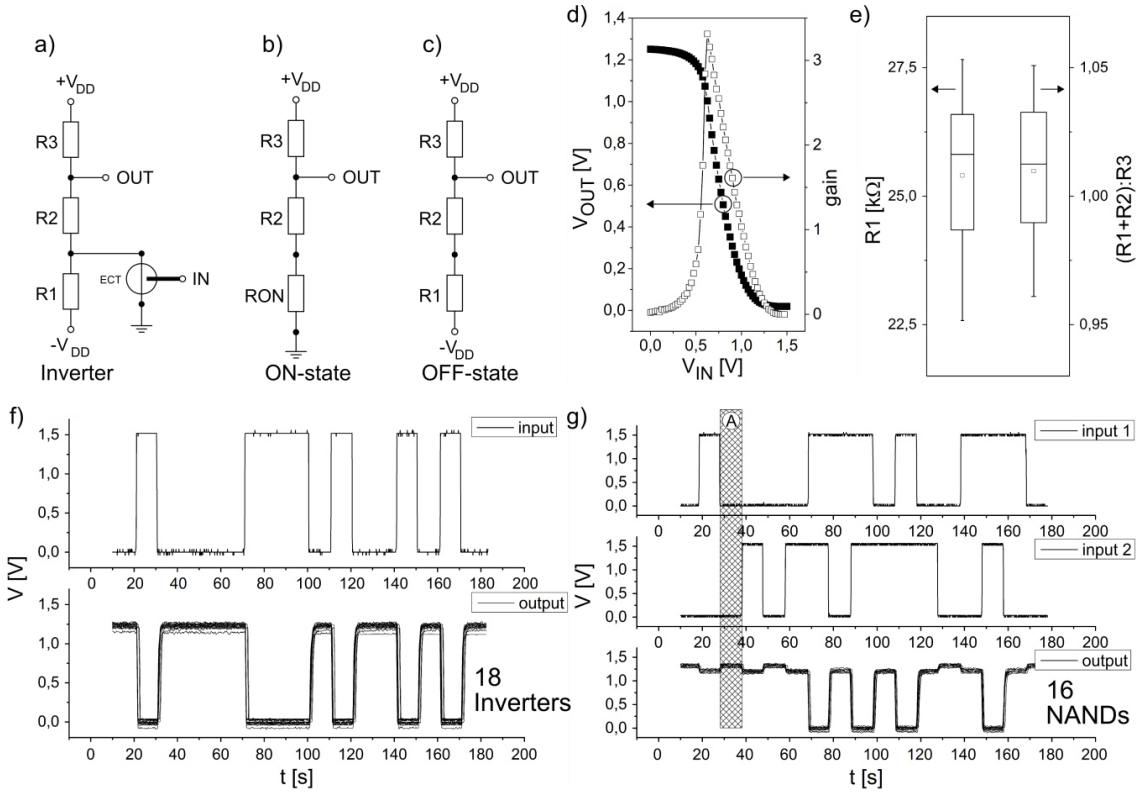


Figure 9.2. (a) Circuit design of an organic electrochemical inverter (b)(c) equivalent circuit of an ideal inverter with the OECT switched (b) on and (c) off (d) inverter transfer characteristics and gain (e) Box-Plot summarizing measurements of 30 resistor chains depicting the distribution of resistor 1 (R_1) and the resistor ratio ((R_1+R_2):R_3) (f) Dynamic response (voltage V over time t) of 18 inverters to square-wave input signals (g) Dynamic response of 16 NAND gates to square-wave input signals; mark "A" highlighting the high level shift (compare text).

The successful fabrication as well as the high reproducibility of the NAND gates and inverters opens up the possibility to fabricate a large variety of complex integrated logic circuits. This capability is demonstrated by fabricating positive-edge triggered master-slave D flipflops and a 2-bit shift register. A flipflop based on OECTs consists of two inverters and eight NAND gates, covering an area of approximately 12.6 cm^2, including all the wiring. A photograph of a typical printed electrochemical flipflop on PET substrate is shown in Fig. 9.3(a) (for a circuit diagram

compare appendix Fig. 9.5(b) or [25]). The basic function of this flipflop is to sample the data input voltage state at the rising edge of the clock signal. This state is stored until the next rising edge of the clock signal when again the data input signal is sampled. In Fig. 9.3(b) the response of eight such flipflops to a square wave data and clock input signal is plotted. The logic 1 state is sampled at the first rising edge of the clock. This state is stored until the logic 0 state of the data input is sampled with the third rising edge of the clock signal and the output is changed to the low level. In addition to the functionality, the output signals also evince the uniformity of the printed devices with high levels comparable to the levels of the basic components and only slightly increased low levels ($\overline{x}_{HIGH} = 1.23$ V with $\sigma_{HIGH} = 0.018$ V, $\overline{x}_{LOW} = 0.068$ V with $\sigma_{LOW} = 0.052$ V). Taking into account that 144 transistors and 240 resistors are necessary for realizing eight flipflops, this remarkable uniformity clearly indicates the high applicability of screen printed OECTs and PEDOT:PSS resistors for complex circuitry.

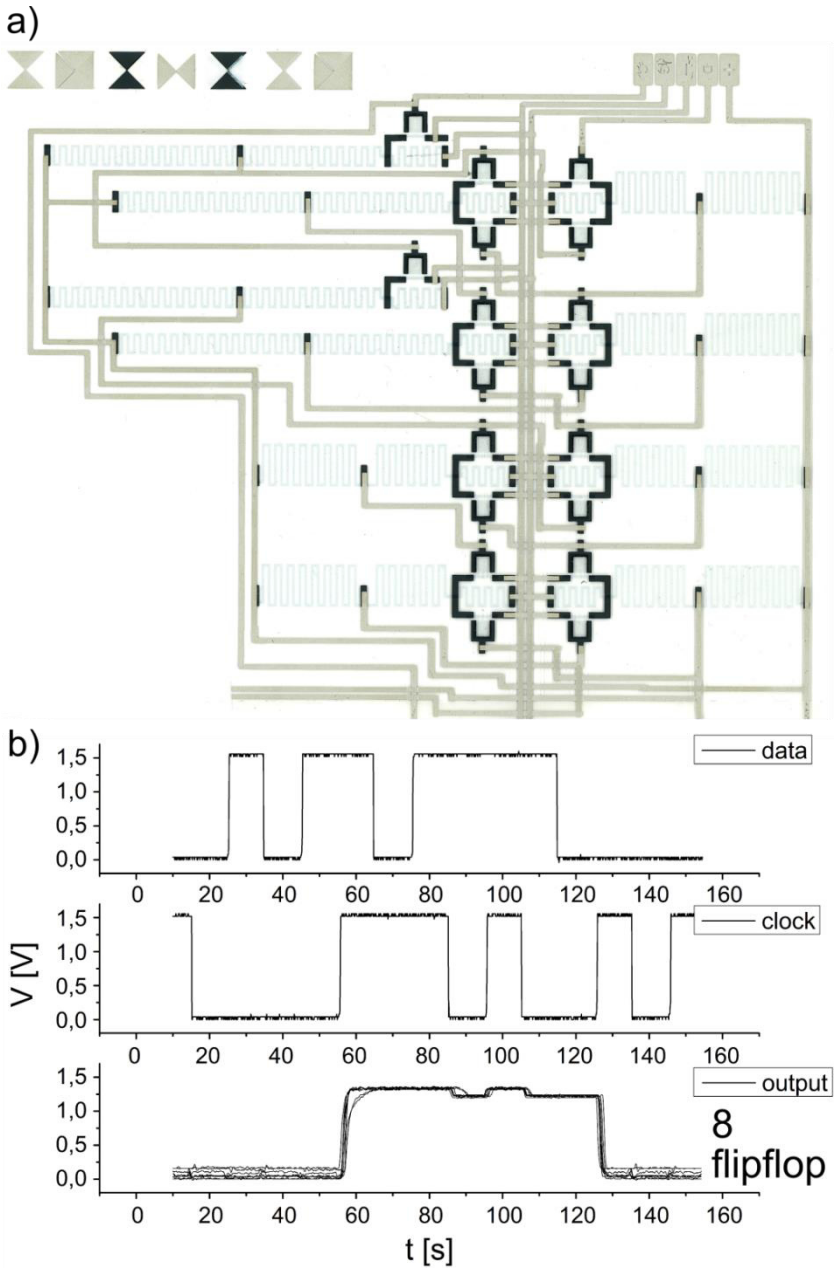


Figure 9.3. (a) Scanned screen printed electrochemical flipflop depicting the needed two inverters and eight NAND-gates (b) Dynamic response of eight flipflops to square-wave data and clock input signals.

By combining two master-slave flipflops, it is possible to fabricate a 2-bit shift register. Fig. 9.4 shows the response of such a device (fabricated on a single PET substrate) to a square wave data and clock input signal. In this shift register the data signal should be stored in the first bit (first flipflop) at the rising edge of the clock signal, while the previous stored state is pushed to the second bit. The full functionality of the printed 2-bit shift register is visible when the logic 1 stored in the first bit at the second rising clock edge [marked 1 in Fig. 9.4] is shifted into the second bit at the third rising clock edge [marked 2 in Fig. 9.4].

Comparing the voltage levels of the two connected bits a slight increase of the lower voltage level $V_{OUT,LOW}$ is visible, resulting in a smaller difference between the high and the low voltage level from ΔV=1,02 V at the output of the first bit (after 4 NAND-gates in series) to ΔV=0,96V at the output of the second bit (after 8 NAND-gates in series). This decrease, representing a decrease in signal quality, indicates that there is an upper limiting number of consecutive stages that can operate without using an external input signal. Considering that the decrease in ΔV is about 20% of the inverter noise margin of 0.31 V this limit will most likely be reached when building a 6 bit shift register.

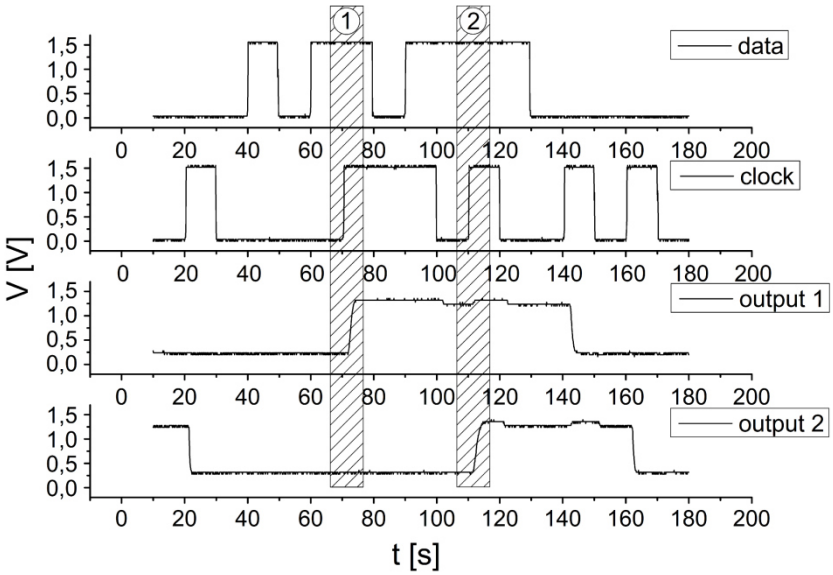


Figure 9.4. Dynamic response of a 2-bit shift register to square-wave data and clock input signals, with parts of the switching process highlighted (marks 1 and 2, compare text).

9.5 Conclusion

In conclusion, we have demonstrated the functionality of integrated logic circuits based on electrochemical transistors and resistors that can operate at very low voltage levels. The devices are fabricated entirely by screen printing on a flexible PET substrate and consist of only five different materials. Inverters, NAND-gates, flipflops and 2-bit shift registers show nearly identical output signals, which is traced back to the high uniformity and stability of the basic building blocks for these circuits, namely more than 380 OECTs and PEDOT:PSS resistors. In this way the suitability of PEDOT:PSS based devices for integrated logic circuitry on flexible substrates by means of a low-cost printing technique is clearly shown.

9.6 Appendix

In the appendix the circuit diagrams for a NAND-gate [Fig. 9.5(a)] and a flipflop [Fig. 9.5(b)] based on organic electrochemical transistors and PEDOT:PSS resistors are presented.

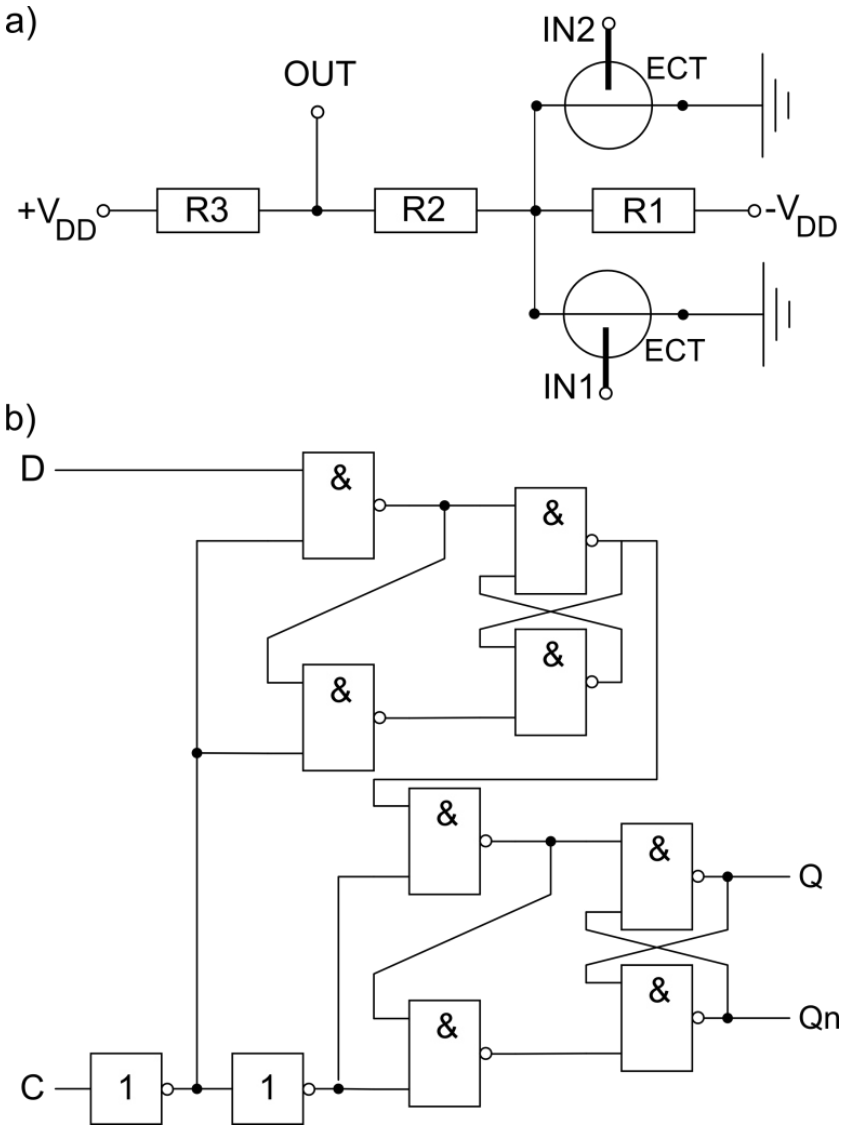


Fig. 9.5. (a) circuit diagram of a NAND-gate consisting of two transistors (ECT) and a voltage divider (R1, R2, R3, +VDD, -VDD) (b) circuit diagram of a flipflop consisting of two inverters and eight NAND-gates

9.7 Acknowledgement

P.C. Hütter would like to thank Prof. K. Gatterer for fruitful discussions and advice.

References

[1] N. D. Robinson, P.-O. Svensson, D. Nilsson, M. Berggren, On the Current Saturation Observed in Electrochemical Polymer Transistors. *J. Electrochem. Soc.* 2006, *153*, H39.

[2] M. Demelas, E. Scavetta, L. Basiricò, R. Rogani, A. Bonfiglio, A deeper insight into the operation regime of all-polymeric electrochemical transistors. *Appl. Phys. Let.* 2013, *102*, 193301.

[3] D. A. Bernards, G. G. Malliaras, Steady-State and Transient Behavior of Organic Electrochemical Transistors. *Adv. Funct. Mater.* 2007, *17*, 3538–3544.

[4] R. M. Owens, G. G. Malliaras, Organic Electronics at the Interface with Biology. *MRS Bull.* 2010, *35*, 449–456.

[5] P. Lin, F. Yan, Organic thin-film transistors for chemical and biological sensing. *Adv. Mater.* 2012, *24*, 34–51.

[6] D. Khodagholy, V. F Curto, K. J Fraser, M. Gurfinkel, R. Byrne, D. Diamond, G. G Malliaras, F. Benito-Lopez, R. M Owens, Organic electrochemical transistor incorporating an ionogel as a solid state electrolyte for lactate sensing. *J. Mater. Chem*. 2012, *22*, 4440.

[7] D. Nilsson, N. Robinson, M. Berggren, R. Forchheimer, Electrochemical Logic Circuits. *Adv. Mater.* 2005, *17*, 353–358.

[8] T. Rothländer, P. C. Hütter, E. Renner, H. Gold, A. Haase, and B. Stadlober, Nanoimprint Lithography-Structured Organic Electrochemical Transistors and Logic Circuits. *IEEE Trans. Electron Devices* 2014, 61, 1515–1519.

[9] M. Hamedi, R. Forchheimer, O. Inganäs, Towards woven logic from organic electronic fibres. *Nat. Mater.* 2007, *6*, 357–362.

[10] P. Andersson, R. Forchheimer, P. Tehrani, M. Berggren, Printable All-Organic Electrochromic Active-Matrix Displays. *Adv. Funct. Mater.* 2007, 17, 3074–3082.

[11] M. Zirkl, A. Sawatdee, U. Helbig, M. Krause, G. Scheipl, E. Kraker, P. A. Ersman, D. Nilsson, D. Platt, P. Bodö, S. Bauer, G. Domann, and B. Stadlober, An all-printed ferroelectric active matrix sensor network based on only five functional materials forming a touchless control interface. *Adv. Mater.* 2011, 23, 2069–2074.

[12] B. Crone, A. Dodabalapur, Y.-Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, W. Li, Large-scale complementary integrated circuits based on organic transistors. *Nature* 2000, *403*, 521–523.

[13] D. D. He, I. A. Nausieda, K. K. Ryu, A. I. Akinwande, V. Bulovic, C. G. Sodini, An integrated organic circuit array for flexible large-area temperature sensing. *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, Feb 7-11, 2010, pp 142-143.

[14] K. Ishida, T.-C. Huang, K. Honda, Y. Shinozuka, H. Fuketa, T. Yokota, U. Zschieschang, H. Klauk, G. Tortissier, T. Sekitani, H. Toshiyoshi, M. Takamiya, T. Someya, T. Sakurai, Insole Pedometer With Piezoelectric Energy Harvester and 2 V Organic Circuits. *IEEE J. Solid-State Circuits* 2013, *48*, 255–264.

[15] A. Sou, S. Jung, E. Gili, V. Pecunia, J. Joimel, G. Fichet, H. Sirringhaus, Programmable logic circuits for functional integrated smart plastic systems. *Org. Electron.* 2014, *15*, 3111–3119.

[16] K. Myny, E. van Veenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, P. Heremans, An 8-Bit, 40-Instructions-Per-Second Organic Microprocessor on Plastic Foil. *IEEE J. Solid-State Circuits* 2012, *47*, 284–291.

[17] K. Myny, S. Smout, M. Rockelé, A. Bhoolokam, T. Huei Ke, S. Steudel, B. Cobb, A. Gulati, F. Gonzalez Rodriguez, K. Obata, M. Marinkovic, D.-V. Pham, A. Hoppe, G. H. Gelinck, J. Genoe, W. Dehaene, P Heremans, A thin-film microprocessor with inkjet print-programmable memory. *Sci. Rep.* 2014, *4*, 7398.

[18] D. Raiteri, P. Van Lieshout, A. Van Roermund, E. Cantatore, Positive-feedback level shifter logic for large-area electronics. *IEEE J. Solid-State Circuits* 2014, *49*, 524–535.

[19] S. Abdinia, F. Torricelli, G. Maiellaro, R. Coppard, A. Daami, S. Jacob, L. Mariucci, G. Palmisano, E. Ragonese, F. Tramontana, A.H.M. van Roermund, E. Cantatore, Variation-based design of an AM demodulator in a printed complementary organic technology. *Org. Electron.* 2014, *15*, 904–912.

[20] H. Marien, M. S. J. Steyaert, E. Van Veenendaal, P. Heremans, Analog building blocks for organic smart sensor systems in organic thin-film transistor technology on flexible plastic foil. *IEEE J. Solid-State Circuits* 2012, *47*, 1712–1720.

[21] G. Hagmann, „Netzwerkberechnung durch Anwendung des Überlagerungsgesetzes,“ in *Grundlagen der Elektrotechnik,* AULA Verlag: Wiebelsheim, 2001; 8. korrigierte Auflage, pp 60-63.

[22] P. C. Hütter, T. Rothländer, A. Haase, G. Trimmel, and B. Stadlober. Influence of geometry variations on the response of organic electrochemical transistors. *Appl. Phys. Lett.* 2013, *103*, 043308.

[23] J. R. Hauser, Noise margin criteria for digital logic circuits. *IEEE Trans. Educ.* 1993, *36*, 363–368.

[24] S. De Vusser, J. Genoe, P. Heremans, Influence of transistor parameters on the noise margin of organic digital circuits. *IEEE Trans. Electron Devices* 2006, *53*, 601–610.

[25] V.P. Nelson, H.T. Nagle, J.D. Irwin, B.D. Carroll, “Introduction to Sequential Devices,” in *Digital Logic Circuit Analysis and Design*, Prentice Hall Inc.: Upper Saddle River, New Jersey, 1995, pp 406-407

10. Efficiency of the Switching Process in Organic Electrochemical Transistors

10.1 Abstract

Entirely screen printed organic electrochemical transistors (OECTs) based on poly(3,4-ethylenedioxithiophene) poly(styrenesulfonate) (PEDOT:PSS) and a polymer electrolyte are investigated in view of a correlation between the electrical charge consumed during switching and the volume of PEDOT:PSS in the transistor channel. An understanding of the relation between charge consumption and the amount of electrochemically active PEDOT is essential for the design of high performance transistors and for providing a deeper insight into the fundamentals of the electrochemical switching process in OECTs. It turned out that a precise control of the width of the PEDOT:PSS source-drain line is imperative for maximizing both the on-current and the on/off current ratio of lateral OECTs.

10.2 Introduction

Organic electrochemical transistors (OECTs) are implemented in a broad variety of applications, such as basic logic circuits [1, 2], smart textiles [3], electrochromic display backplanes [4], and in active-matrix physical sensor circuits [5]. In these applications their intrinsic advantages, like simple design allowing for a fabrication by additive manufacturing techniques, low operating voltage, the compatibility with large and flexible substrates, and the ability to conduct both ionic and electronic charge carriers are exploited. Especially the latter led to recent investigations of OECTs in a different context: the field of organic bioelectronics, which combines the realms of biology and electronics and is therefore highly promising for OECTs [6-12]. Despite the specific demands for the different applications, the fundamental requirement of estimating the characteristics of an OECT prior to fabrication is almost always present. In circuit design, for example, the power consumption of an integrated circuit depends on the characteristics of each individual device, which determines a great number of critical design considerations [13]. Another example is the application of OECTs in sensing, where a reproducible influence on the transistor characteristics is needed to qualify or/and quantify a given analyte (an example of measuring the concentration of different cations is provided by literature [14]). Accordingly, in order to predict the transistor's characteristics, a variety of theoretical investigations of the basic functionalities of OECTs were performed [15-17]. Moreover, the relationship between geometry and performance on OECTs has been investigated experimentally [18]. Recent reports show that the uptake of ions from an

electrolyte into a film of poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonate (PEDOT:PSS) ,when arranged in a capacitor configuration, takes place in the entire volume of the PEDOT:PSS, indicating a direct relation between the volume of the film and the measured capacitance (denoted as purely volumetric capacitance) [27]. In line with this approach we are investigating the dependence of the current (and charge), needed to switch the transistor off, on the volume of PEDOT:PSS in the transistor channel. We show that the turn-off charge Q correlates with the amount of PEDOT:PSS that participates in the electrochemical switching process at the interface of electrolyte and PEDOT:PSS. In addition, we demonstrate that the PEDOT:PSS volume is an important design parameter for optimizing the performance of organic electrochemical transistors.

10.3 Results and Discussion

In Figure 10.1a the top-view of a screen printed OECT in a lateral configuration is shown. The lateral design, with the source-drain and gate electrode in the same plane, is perfectly suited for fabrication through additive manufacturing techniques like screen printing. This is a great benefit as it is possible to fabricate highly reproducible OECTs using screen printing, even uniformly enough to serve as building blocks in screen printed logic circuits as we demonstrated in another publication of our research group [39]. A scheme of the three-step printing process used for fabricating the transistors included in this work is depicted in figure 10.1b whereas details on the fabrication process can be found in the experimental section. In these lateral designed transistors PEDOT:PSS forms the active channel, the source-drain electrodes and the gate electrodes. The carbon layer is used to prevent the PEDOT:PSS electrodes from damage during the electrical characterization and ensuring minimally resistive interconnections. Water based, $CaCl_2$ containing gel serves as the polymer electrolyte. Figure 10.1c displays the design of such a lateral OECT, indicating the applied potentials and currents during transistor operation. In Figure 10.1d, the output characteristics $I_D(V_D)$ (drain current vs. drain voltage) of a typical entirely screen printed transistor is shown. The on-current amounts to about I_{ON} = -0.32 mA at a gate voltage V_G = 0 V and the off-current to I_{OFF} = -39 nA at V_G = 1.5 V, which corresponds to an on/off current ratio I_{ON}/I_{OFF} of over 8000.

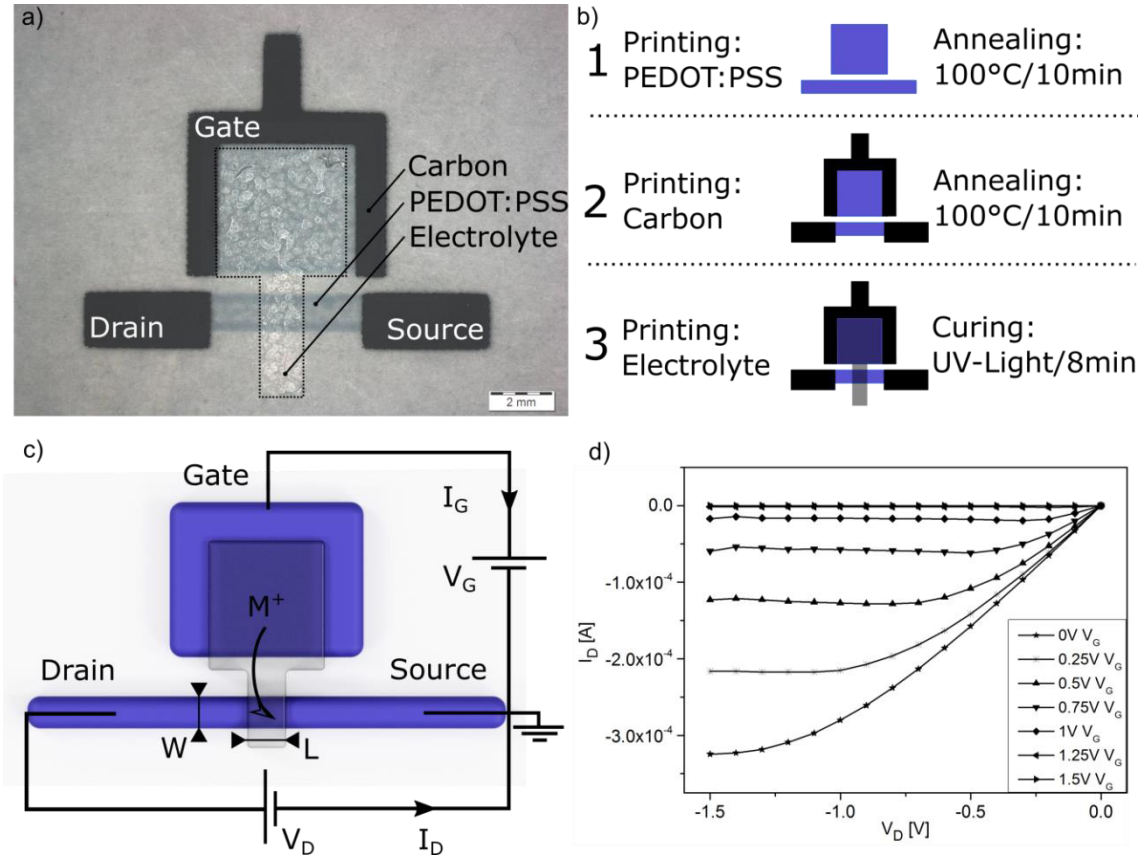


Figure 10.1: a) photograph of an entirely screen-printed OECT. b) scheme depicting the three-step fabrication process by screen printing. c) design of a lateral OECT with the applied voltages and currents indicated. V_G and I_G are the gate voltage and gate current, V_D and I_D are the source-drain voltage and source-drain current, and M^+ denotes the mobile cations. Additionally the width of the source-drain line W and the width of the electrolyte line L are denoted. d) output characteristics of a transistor with a thickness T and a width of the source-drain line W of T = 0.7µm and W = 530µm, respectively, and an electrolyte line width L of L = 1200µm.

PEDOT can be reduced (undoped) and oxidized (doped) in a reversible manner by switching between a non-conducting and a conducting state induced by an external electric field. These states determine the off- and on-states of the organic electrochemical transistor. The reversible redox reaction of PEDOT is as follows [28]:

$$PEDOT^+:PSS^- + M^+ + e^- \leftrightarrow PEDOT^0 + M^+:PSS^- \qquad \text{(Eq 10.1)}$$

The reaction is driven by the voltages V_D and V_G (compare Figure 10.1c). According to the applied electric fields between the gate and the channel an electron current (I_G) is induced via the external interconnects that is balanced by a flow of positively charged ions (M^+) via the electrolyte. As PEDOT:PSS is the redox active species it is obvious that the total current depends on the amount of PEDOT:PSS. In the lateral transistor design shown in Figure 10.1c

the electrochemically active amount of PEDOT:PSS is formed by the width of the source-drain line W, its thickness T and the width of the electrolyte covering the source-drain line L. This active volume, hereinafter also referred to as the channel volume V_{ol}, is highlighted in Figure 10.2a.

For an examination of the relation between the PEDOT:PSS channel volume V_{ol} and the current consumed during OECT switch-off, first a voltage of V_D = -1.5V is applied to the drain electrode and the source electrode is connected to ground. Subsequently, a square-wave transitional voltage V_G changing from 0 to +1.5V is applied to the gate electrode, inducing a non-stationary flow of charge carriers between gate and channel denoted as the switch-off gate current I_G. Figure 10.2b depicts a typical time profile of I_G showing a sharp peak when V_G switches to 1.5V, followed by a flattening out for three samples with different channel volumes. V_G was kept high for 70s, giving the transistor sufficient time to completely switch off.

Time-integration of the measured I_G yields the charge Q that is consumed in the course of this switching process. In order to underpin the assumption of a direct correlation between the 'switching charge' Q (the amount of gate charge needed to suppress the current flow between source and drain), and V_{ol} (the PEDOT:PSS channel volume), we prepared 38 samples with V_{ol} varying between $5\times10^{-15}m^3$ and $5\times10^{-13}m^3$ and determined Q for all of these. The result is shown in Figure 10.2c. It indeed reveals an almost perfect linear increase of Q with increasing V_{ol}. The strong correlation between Q and V_{ol} allows for a quantitative prediction of the charge consumed during transistor switching by using linear interpolation of the fitted curve. For example, when V_{ol} is increased by 100 μm^3, the charge Q needed to switch off the OECT increases by 1 pC.

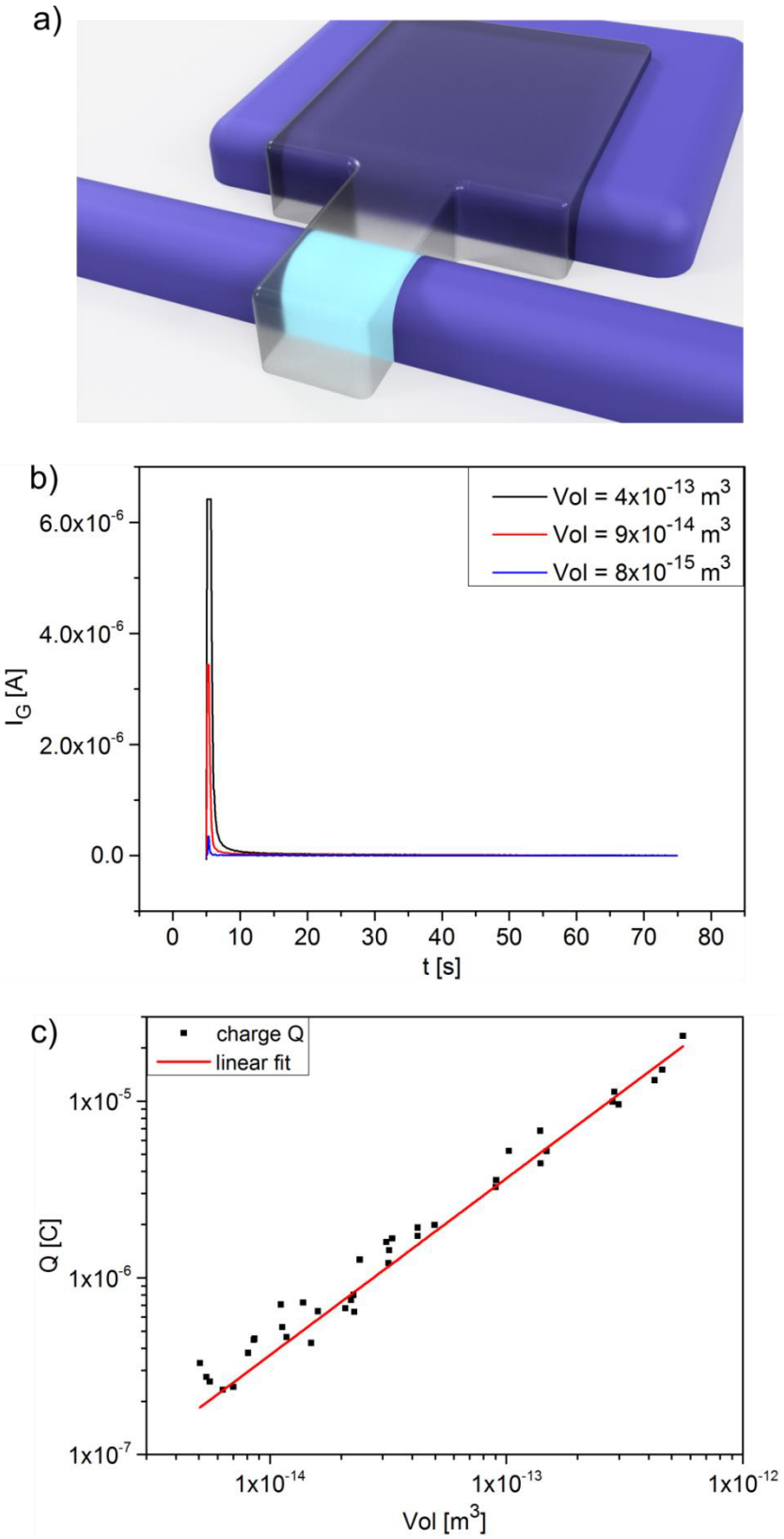


Figure 10.2: a) detailed view of the transistor channel with the electrochemically-active volume of PEDOT:PSS highlighted; b) evolution of the gate current I_G over a measurement period of 70 s at V_D = -1.5V and V_G = +1.5V for transistors with volumes of $V_{ol} = 4 \times 10^{-13} m^3$, $V_{ol} = 9 \times 10^{-14} m^3$ and $V_{ol} = 8 \times 10^{-15} m^3$ c) relationship between the electric charge Q consumed during off-switching and V_{ol} ,the volume of PEDOT:PSS in the channel. The red line is a

linear fit to the data with Q = 3.66 × $10^7 \cdot V_{ol}$ with a correlation coefficient of R = 0.98, carried out with a fixed intercept at 0/0 to meet the requirement of zero consumed charge when there is zero organic semiconductor present.

The gate current I_G is predominantly a result of the cation transport from the electrolyte into the PEDOT:PSS volume [29]. Recent reports on the purely volumetric capacitance of PEDOT:PSS structures covered with electrolyte state that the cations face only a negligible injection barrier and penetrate the channel without any ion accumulation at the PEDOT:PSS surface [27]. Consequently, the majority of transported cations (denoted as M^+) are available for the redox reaction described in equation 10.1. As each injected cation compensates one acceptor in the PEDOT:PSS film [17], the charge Q required to switch the transistor off can be used to determine the amount of PEDOT participating in the electrochemical doping/de-doping process by using a modification of Faradays law:

$$m_A = \frac{M*Q}{z*F} \qquad \text{(Eq. 10.2)}$$

In Equation 10.2 Q denotes the charge, F the Faraday constant, M the molecular weight and z the charge number. The Faraday constant F is defined as 96485 A*s/mol. The molecular weight M is not exactly determined for PEDOT; values range from 1000 to 2500 g/mol in literature [30, 31]. We therefore chose three values for M in the following calculations: 1000g/mol, 1750g/mol and 2500g/mol. The co-factor z is the product of two variables, the charge per charge carrier X, and the number of charge carriers per polymer chain Y, so that z = X*Y.

For the determination of X, the relation between the two types of charge carriers in PEDOT:PSS, polarons and bipolarons [32] has to be clarified. It is important to distinguish between those two contributions to the charge transport as polarons carry one positive charge and bipolarons carry two positive charges. For highly doped PEDOT:PSS, the literature provides values as high as 97% for the relative amount of bipolarons [33], so it can be justified to assume a predominantly bipolaron-based charge transport. As polarons and bipolarons differ in their optical absorption behavior we performed UV-Vis-NIR spectroscopy to corroborate this assumption. Polarons show a distinct absorption band between 600nm and 1200nm, peaking around 900nm, whereas bipolarons display a very broad band in the NIR region above 1500nm [34, 35]. Figure 10.3a shows the recorded absorption spectrum of PEDOT:PSS, revealing the broad absorption band of bipolarons above 1500nm and a peak around 800nm, indicating the presence of polarons as well. Comparing the areas under the fitted polaron peaks (Fit Peak

Polaron 1 and 2 in figure 10.3a) and the bipolaron peak (Fit Peak Bipolaron), we determined a ratio of 97% bipolarons and 3% polarons. With our measurements being consistent with the values provided in literature X is approximated to be 1.97.

As a next step, Y, the number of charge carriers per polymer chain, has to be determined. This variable is based on the conjugation length of a bipolaron and the length of the polymer chains. Six monomeric units are involved in carrying the two positive charges on the polymer chain [36]. As mentioned before, the molecular weight in literature ranges from 1000g/mol to 2500g/mol, yielding a chain length between 7 and 17 monomeric units. Taking the chain length and the conjugation length into account we evaluated the factor Y, the probable number of charge carrying structures per polymer chain. Accordingly, Y is approximated to be 1, 1.5 and 2 for chain lengths of 7, 12 and 17 monomeric units, respectively. With these values for X and Y the co-factor z is obtained: z = 1.97 for M 1000g/mol, 2,955 for M 1750g/mol and 3,94 for M 2500g/mol.

On the basis of equation 10.2 we are now able to calculate the active mass m_A of PEDOT in the transistor as a function of the volume V_{ol} for the different molecular weights M. The result is displayed in Figure 10.4a, again supporting the assumption of a linear relationship between electrochemically active mass and channel volume.

For a deeper and more quantitative understanding of the active mass values it is beneficial to calculate the upper limit total mass m_c of PEDOT in the channel to participate in the electrochemical process during the transistor switching process. We therefore need the density ρ of PEDOT:PSS and the ratio r between PEDOT and PSS in the thin film. A hydrostatic balance (see Experimental section) delivered a density of ρ = 1240 kg/m^3 for PEDOT:PSS. The ratio of PEDOT to PSS is quantified by XPS measurements. In the S(2p) spectra shown in Figure 10.3b three peaks are visible in the cumulative curve at binding energies of 168 eV, 164.6 eV and 163.5 eV. The peak at 168 eV corresponds to the sulfur signal of PSS while the peaks at 164.6 eV and 163.1 eV correspond to the sulfur signal of PEDOT [37, 38]. Based on the ratio of the peak intensities the ratio between PEDOT and PSS was determined to be r = 1:3 (PEDOT:PSS). To rule out any potential effects of PSS cumulating on the film surface [38] we performed measurements at different angles. Since no significant angular dependence of the relative peak intensities and positions was observed we may assume a homogeneous distribution of PEDOT and PSS with r = 1:3 throughout the entire film.

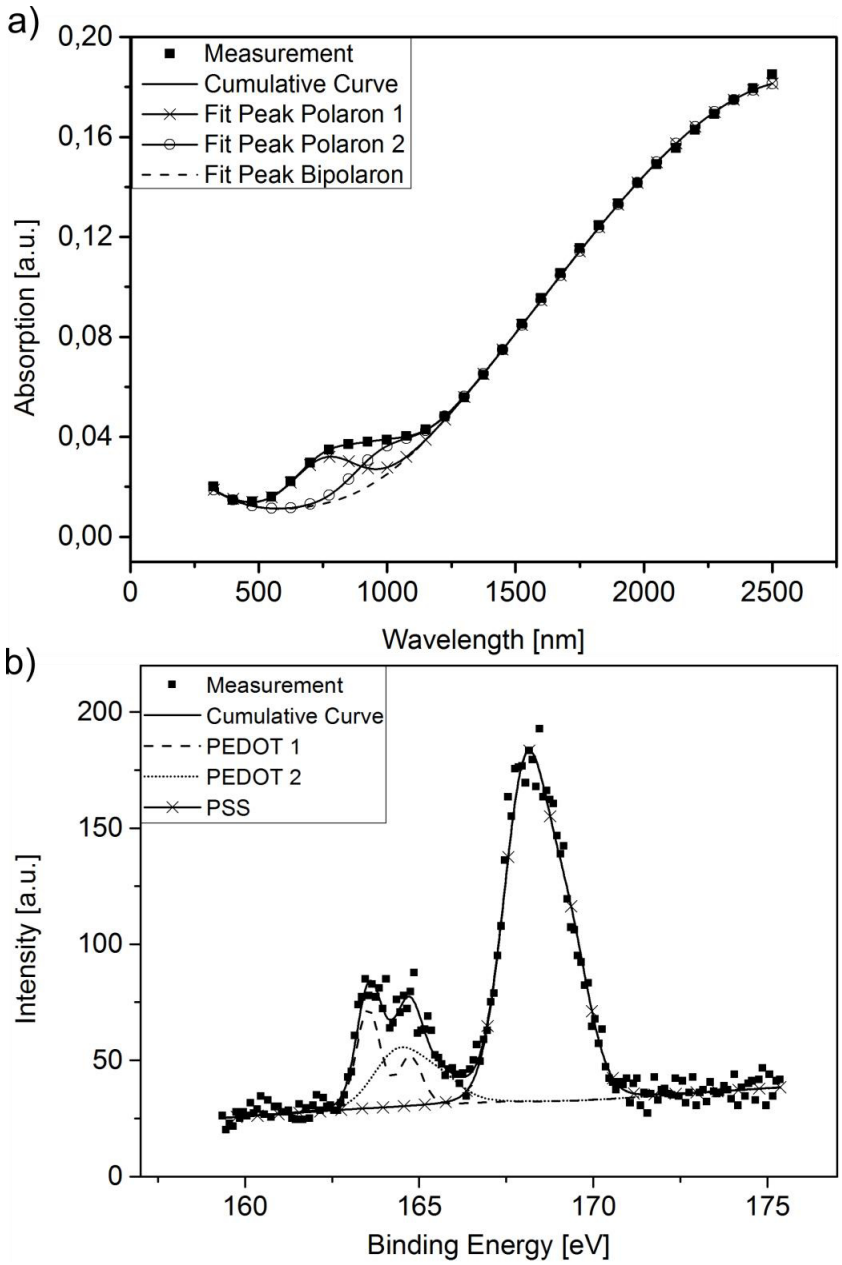
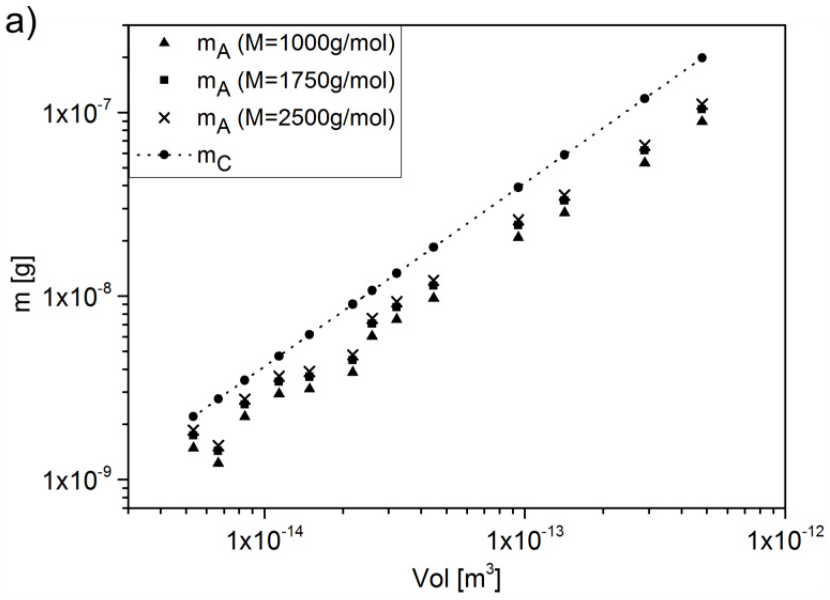


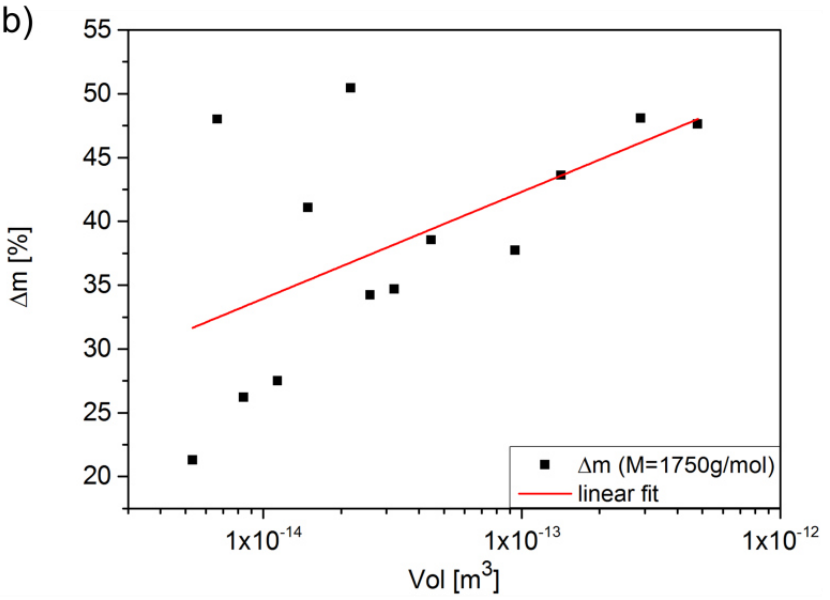
Figure 10.3: a) UV-Vis-NIR spectra of PEDOT:PSS film, showing the measured spectra and fitting of the peaks. b) S(2p) XPS spectra of a 500 nm thin PEDOT:PSS films, showing the peaks for sulfur in PEDOT (PEDOT 1 and PEDOT 2) and in PSS (PSS).

Based on the measured parameters V_{ol}, ρ and r we calculated the total mass m_C of PEDOT present in the transistor channel and compared it to m_A - the mass of electrochemically active PEDOT. From a plot of m_c and m_A as a function of V_{ol} over 15 samples (Figure 10.4a) we can estimate which portion of the theoretical upper limit mass m_C is electrochemically active during switching. Several conclusions can be drawn from Figure 10.4a:

First, there is only little variation among the masses m_A determined for the three different molecular weights M. The variation lies within ± 10% of the mean value of m_A revealing the modest influence of M, a parameter that is not determined precisely. Second, it is evident that m_C exceeds m_A in the whole range of examined PEDOT:PSS volumes. This was anticipated as there is a non-vanishing current in the off-state of the OECT (I_{OFF} = -3.89 × 10^{-8} A according to the output characteristics shown in Figure 10.1d), indicating some amount of PEDOT still present in its oxidized state. This can be traced back to the tertiary structure of PEDOT:PSS [30, 31] and steric hindrance. Due to the partly coiled conformation of the polymer chains it is unlikely that all the conducting sites are reduced [29], resulting in a residual conductivity of PEDOT:PSS. Figure 10.4b shows to what extend m_C and m_A (M = 1750g/mol) are differing, revealing that 21% of the PEDOT at a volume of 5 × $10^{-15}$$m^3$ and 48% of the PEDOT at a volume of 5 × $10^{-13}$$m^3$ are not electrochemically active. Overall, a linear trend is visible, indicated by the fitted line in Figure 10.4b. The higher the volume of PEDOT:PSS in the transistor channel, the higher the amount of PEDOT that does participate in the switching process. In other words: The higher the volume, the less efficient the PEDOT:PSS is used. This observation is supported by comparing the performance of transistors with different channel volumes in terms of their on/off current ratio. As seen in Figure 10.4c, the on/off current ratio decreases from 5 × 10^4 to 5 × 10^3 with the volume of PEDOT:PSS increasing from 5 × 10^{-15} m^3 to 5 × 10^{-13} m^3. To increase the volume of PEDOT:PSS the widths of the source-drain line W and of the electrolyte L are increased. Unintentionally, in the fabrication process, the thickness of the source-drain line T increases with its width W. These changes in the source-drain line geometry might explain the observed decreasing on/off current ratio when the PEDOT:PSS volume is increased: (i) with increasing thickness T of the source-drain line, the (vertical) distance between the interface PEDOT:PSS – electrolyte and the bottom face of the PEDOT:PSS source-drain line increases, resulting in a larger distance for the positive charged ions to travel [26]. (ii) with increasing width of the source-drain line W, the lateral distance of the PEDOT surface facing away from the gate electrode increases, resulting in a smaller electric field and therefore a weaker driving force for positive charged ions [26]. Both geometric effects result in a less effective off-switching of the transistor. These findings allow for the presumption that a larger PEDOT:PSS volume not only leads to a higher charge consumption for switching the transistor off (due to the increase of m_C) but also to a less efficient use of the present PEDOT:PSS in terms of on/off current ratio, at least for the lateral organic electrochemical transistors used in this work. As shown in Figure 10.4c, the on-current I_{on} increases with increasing PEDOT:PSS volume, because a larger total number of charge carriers in a larger PEDOT:PSS volume results in a lower

resistance of the source-drain line. Thus the two transistor parameters on/off current ratio I_{on}/I_{off} and on-current I_{on} are affected in an opposite manner by an increasing PEDOT:PSS volume, which manifests a trade-off in the optimization of the transistor design. In our case a PEDOT:PSS volume of $V_{ol} = 4.5 \times 10^{-14}$ m^3, realized by a transistor with a source-drain line width of W = 320 µm and a thickness T = 0.53 µm, shows a high on/off current ratio of $I_{on}/I_{off} = 3 \times 10^4$ and also a high on current of $I_{on} = 3 \times 10^{-4}$ A. Both values are larger than 65% of the maximally achieved values.


a)
m_A (M=1000g/mol)
m_A (M=1750g/mol)
m_A (M=2500g/mol)
m_C
m [g]
1x10^-7
1x10^-8
1x10^-9
1x10^-14
1x10^-13
1x10^-12
Vol [m^3]


b)
Δm [%]
55
50
45
40
35
30
25
20
Δm (M=1750g/mol)
linear fit
1x10^-14
1x10^-13
1x10^-12
Vol [m^3]

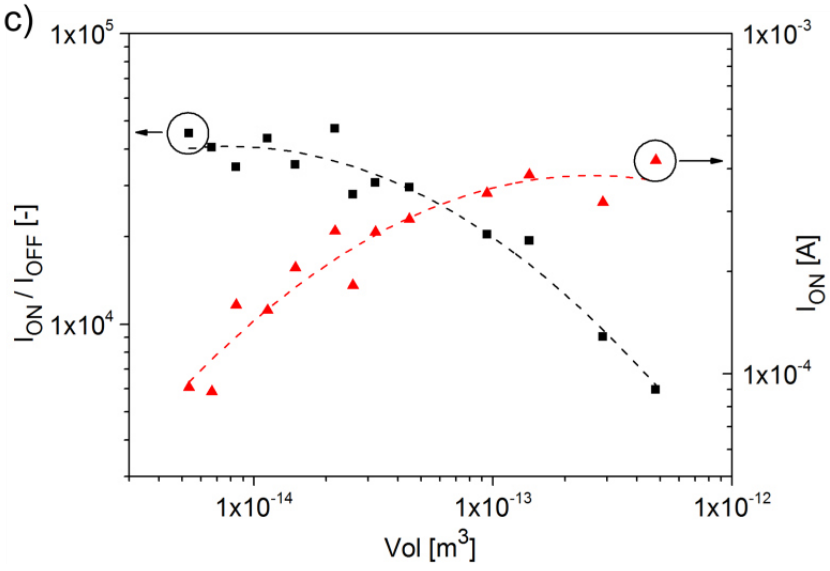

c)
1x10^5
1x10^4
1x10^-3
1x10^-4
I_ON / I_OFF [-]
I_ON [A]
1x10^-14
1x10^-13
1x10^-12
Vol [m^3]

Figure 10.4: a) Mass of PEDOT vs. V_{ol} with m_C being the total mass of PEDOT present in the channel and m_A the calculated electrochemically active mass (for molecular weights M of 1000, 1750 and 2500 g/mol). b) Difference between m_C and m_A (for M = 1750g/mol). The linear fit highlights the trend of increasing difference with increasing volume. c) on/off current ratio I_{ON}/I_{OFF} as well as on-current I_{ON} vs. V_{ol} plotted in dashes as guidelines for the eyes.

10.4 Conclusion

In conclusion, we were able to quantitatively explain the volume dependence of the charge necessary to switch an OECT off by identifying a positive linear correlation between the required charge and the volume of PEDOT:PSS in the transistor channel. Moreover, above a specific volume threshold, the amount of PEDOT actually participating in the electrochemical switching process decreases relative to the total PEDOT volume when the PEDOT design line width increases, leading to a decrease of the on/off current ratio as well. Accordingly, we could demonstrate that the PEDOT:PSS volume and especially the source-drain line width W is an important design parameter for optimizing the performance of organic electrochemical transistors in terms of maximizing both the on-current and the on/off current ratio.

10.5 Experimental

All OECTs used in this work were fabricated from PEDOT:PSS (Clevios S V3), a screen-printable electrolyte and carbon paste (DuPont 7102). The electrolyte consists of 22.8 wt.% calcium chloride, 45.6 wt.% deionized water, 7.6wt.% Mowiol 56-98, 22.8 wt.% UCECOAT 6558 and 1.1wt.% Additol BCPK. A Technical Industrial Co., Ltd. SFM 550 semi-automatic screen printer was used for the fabrication of the devices. The parameters of the used screens are 100-40 mesh for the PEDOT:PSS layer, 120-34 mesh for the carbon paste layer and 30-120 mesh for the electrolyte layer. As a first step the PEDOT:PSS electrodes are printed followed by an annealing step in an oven at 100°C for 10 minutes. Next the carbon pads are printed, again followed by an annealing step in an oven at 100°C for 10 minutes. Finally two layers of electrolyte are printed wet on wet and cured under UV-light (354 nm) for 8 minutes. To obtain different volumes of PEDOT:PSS the widths of the source-drain line W and the covering electrolyte L were varied. Line widths between W = 120µm and W = 1050µm for the PEDOT:PSS and between L = 180µm and L = 1300µm for the electrolyte were used. In the fabrication process, the thicknesses T of the PEDOT:PSS lines unintentionally changed with their widths. Accordingly, thicknesses between T = 300nm and T = 750 nm were obtained, also contributing to a variation of the PEDOT:PSS volume in the transistor channel. The linewidths were measured using an Olympus BX51 microscope with a Colorview 1 digital imaging system. Thicknesses were measured with a Dektak 150 Profilometer by Bruker. For the density

measurements according to the Archimedes' principle a self-constructed hydrostatic balance using a Sartorius MC1 RC 210 P balance and 100 mg PEDOT:PSS samples were used. The UV-Vis-NIR measurements were conducted using a PerkinElmer Lambda 950 spectrometer. XPS was performed in an Omicron Nanotechnology "Multiprobe" UHV-surface-analysis system using monochromatic Al Kα1-line X-Rays at 1486eV with a line width (FWHM) of 0.2 eV. The signals, emitted from the analyzed area of $1mm^2$, were detected using a pulse-counting channeltron (5 channels for count-rate enhancement).

10.6 Author Information

Corresponding Author

*E-mail: barbara.stadlober@joanneum.at

Notes

The authors declare no competing financial interest.

10.7 Acknowledgment

P.C. Hütter would like to thank Thomas Rothländer for fruitful discussions and advice.

References

[1] D. Nilsson, N. Robinson, M. Berggren, R. Forchheimer, Electrochemical Logic Circuits. *Adv. Mater.* 2005, *17*, 353–358.

[2] T. Rothländer, P. C. Hütter, E. Renner, H. Gold, A. Haase, B. Stadlober, Nanoimprint Lithography-Structured Organic Electrochemical Transistors and Logic Circuits. *IEEE Trans. Electron Devices* 2014, *61*, 1515–1519.

[3] M. Hamedi, R. Forchheimer, O. Inganäs, Towards Woven Logic from Organic Electronic Fibers. *Nat. Mater.* 2007, *6*, 357–362.

[4] P. Andersson-Ersman, R. Forchheimer, P. Tehrani, M. Berggren, Printable All-Organic Electrochromic Active Matrix Displays. *Adv. Funct. Mater.* 2007, *17*, 3074–3082.

[5] M. Zirkl, A. Sawatdee, U. Helbig, M. Krause, G. Scheipl, E. Kraker, P. A. Ersman, D. Nilsson, D. Platt, P. Bodö, S. Bauer, G. Domann, and B. Stadlober, An all-printed ferroelectric active matrix sensor network based on only five functional materials forming a touchless control interface. *Adv. Mater.* 2011, 23, 2069–2074.

[6] M. Berggren, A. Richter-Dahlfors, Organic Bioelectronics. *Adv. Mater*. 2007, *19*, 3201–3213.

[7] R. M. Owens, G. G. Malliaras, Organic Electronics at the Interface with Biology. *MRS Bull*. 2010, *35*, 449–456.

[8] G. Tarabella, F. Mahvash Mohammadi, N. Coppedè, F Barbero, S. Iannotta, C. Santato, F. Cicoira, New Opportunities for Organic Electronics and Bioelectronics: Ions in Action. *Chem. Sci*. 2013, *4*, 1395–1409.

[9] J. Rivnay, R. M. Owens, G. G Malliaras, The Rise of Organic Bioelectronics. *Chem. Mater*. 2014, *26*, 679–685.

[10] J. Rivnay, M.Ramuz, P. Leleux, A. Hama, M. Huerta, R. M. Owens, Organic Electrochemical Transistors for Cell-Based Impedance Sensing. *Appl. Phys. Lett*. 2015, *106*, 043301.

[11] X. Strakosas, M. Bongo, R. M. Owens, The Organic Electrochemical Transistor for Biological Applications. *J. Appl. Polym. Sci*. 2015, *132*, 41735.

[12] G. Scheiblin, A. Aliane, X. Strakosas, V. F. Curto, R. Coppard, G. Marchand, R. M. Owens, P. Mailley, G. G. Malliaras, Screen-Printed Organic Electrochemical Transistors for Metabolite Sensing. *MRS Commun*. 2015, *5*, 507–511.

[13] J.M. Rabaey, A. Chandrakasan, B. Nikolic, In *Digital Integrated Circuits: A Design Perspective*, Prentice-Hall, Inc. Upper Saddle River, NJ, USA 1996; Chapter 1, pp 15-34

[14] P. Lin, F. Yan, H. L. W. Chan, Ion Sensitive Properties of Organic Electrochemical Transistors. *ACS Appl. Mater. Interfaces* 2010, *2*, 1637–1641.

[15] N. D. Robinson, P.-O. Svensson, D. Nilsson, M. Berggren, On the Current Saturation Observed in Electrochemical Polymer Transistors. *J. Electrochem. Soc*. 2006, *153*, H39–H44.

[16] M. Demelas, E. Scavetta, L. Basiricò, R. Rogani, A. Bonfiglio, A Deeper Insight into the Operation Regime of All-Polymeric Electrochemical Transistors. *Appl. Phys. Lett*. 2013, *102*, 193301.

[17] D. A. Bernards, G. G. Malliaras, Steady State and Transient Behavior of Organic Electrochemical Transistors. *Adv. Funct. Mater*. 2007, *17*, 3538–3544.

[18] L. Basiricò, P. Cosseddu, A. Scidà, B. Fraboni, G. G. Malliaras, A. Bonfiglio, Electrical Characteristics of Ink-jet Printed, All-Polymer Electrochemical Transistors. *Org. Electron.* 2012, *13*, 244–248.

[19] M. Berggren, R. Forchheimer, J. Bobacka, P.-O. Svensson, D. Nilsson, O. Larsson, A. Ivaska, In *Organic Semiconductors in Sensor Applications*; Bernards, D. A.; Malliaras, G. G.; Owens, R. M.; Springer Series in Materials Science, Vol. 107 (Springer, Berlin, Germany, 2008), pp.263–280.

[20] D. Khodagholy, M. Gurfinkel, E. Stavrinidou, P. Leleux, T. Herve, S. Sanaur, G. G. Malliaras, High Speed and High Density Organic Electrochemical Transistor Arrays, *Appl. Phys. Lett*. 2011, *99*, 163304.

[21] G. Tarabella, C. Santato, S. Y. Yang, S. Iannotta, G. G. Malliaras, F. Cicoira, Effects of the Gate Electrode on the Response of Organic Electrochemical Transistors. *Appl. Phys. Lett*. 2010, *97*, 123304.

[22] F. Lin, M. C Lonergan, Gate Electrode Processes in an Electrolyte-Gated Transistor: Non-Faradaically versus Faradaically Coupled Conductivity Modulation of a Polyacetylene Ionomer. *Appl. Phys. Lett.* **2006**, *88***,** 133507.

[23] J. Rivnay, P. Leleux, M. Sessolo, D. Khodagholy, T. Hervé, M. Fiocchi, G. G. Malliaras, Organic Electrochemical Transistors with Maximum Transconductance at Zero Gate Bias. *Adv. Mater*. 2013, *25*, 7010–7014.

[24] P. Kumar, Z. Yi, S. Zhang, A. Sekar, F. Soavi, F. Cicoira, Effect of Channel Thickness, Electrolyte Ions, and Dissolved Oxygen on the Performance of Organic Electrochemical Transistors. *Appl. Phys. Lett*. 2015, *107*, 053303.

[25] F. Cicoira, M. Sessolo, O. Yaghmazadeh, J. A. Defranco, S. Y. Yang, G. G. Malliaras, Influence of the Device Geometry on the Sensor Characteristics of Planar Organic Electrochemical Transistors. *Adv. Mater*. 2010, *22*, 1012–1016.

[26] P. C. Hütter, T. Rothländer, A. Haase, G. Trimmel, B. Stadlober, Influence of Geometry Variations on the Response of Organic Electrochemical Transistors. *Appl. Phys. Lett*. 2013, *103*, 043308.

[27] J. Rivnay, P. Leleux, M. Ferro, M. Sessolo, A. Williamson, D. A. Koutsouras, D. Khodagholy, M. Ramuz, X. Strakosas, R. M. Owens, C. Benar, J.-M. Badier, C. Bernard, G. G. Malliaras, High-Performance Transistors for Bioelectronics through Tuning of Channel Thickness. *Sci. Adv*. 2015, *1*, e1400251–e1400251.

[28] M. Lapkowski, A. Pron, Electrochemical Oxidation of Poly(3,4-ethylenedioxithiophene) – "in situ" Conductivity and Spectroscopic Investigations. *Synth. Met*. 2000, *110*, 79–83.

[29] Y. Xia, J. Ouyang, Significant Different Conductivities of the Two Grades of Poly(3,4-ethylenedioxthiophene):Poly(styrenesulfonate), Clevios P and Clevios PH1000, Arising from Different Molecular Weights. *ACS Appl. Mater. Interfaces* 2012, *4*, 4131–4140.

[30] U. Lang, E. Müller, N. Naujoks, J. Dual, Microscopical Investigations of PEDOT:PSS Thin Films. *Adv. Funct. Mater*. 2009, *19*, 1215–1220.

[31] S. Kirchmeyer, K. Reuter, J. C. Simpson, In *Conjugated polymers: Theory, synthesis, properties, and characterization*; Skotheim, T. A., Reynolds, J. R., Eds.; CRC Press, Taylor & Francis Group: Boca Raton, FL, 2007; Chapter 10.

[32] J. Bredas, G. Street, Polarons, Bipolarons, and Solitons in Conducting Polymers. *Acc. Chem. Res*. 1985, *18*, 309–315.

[33] O. Bubnova, Z. U. Khan, H. Wang, S. Braun, D. R. Evans, M. Fabretto, P. Hojati-Talemi, D. Dagnelund, J.-B. Arlin, Y. H. Geerts, S. Desbief, D. W. Breiby, J. W. Andreasen, R. Lazzaroni, W. M. Chen, I. Zozoulenko, M. Fahlman, P. J. Murphy, M. Berggren, X. Crispin, Semi-Metallic Polymers. *Nat. Mater*. 2013, *13*, 190–194.

[34] I. Cruz-Cruz, M. Reyes-Reyes, R. López-Sandoval, Formation of Polystyrene Sulfonic Acid Surface Structures on Poly(3,4-ethylenedioxithiophene):Poly(styrenesulfonate) Thin Films and the Enhancement of its Conductivity by using Sulfuric Acid. *Thin Solid Films* 2013, *531*, 385–390.

[35] J. Luo, D. Billep, T. Waechtler, T. Otto, M. Toader, O. Gordan, E. Sheremet, J. Martin, M. Hietschold, D. R. T. Zahn, T. Gessner, Enhancement of the Thermoelectric Properties of PEDOT:PSS Thin Films by Post-Treatment. *J. Mater. Chem. A* 2013, *1*, 7576–7538.

[36] W. Domagala, B. Pilawa, M. Lapkowski, Quantitative in-situ EPR Spectroelectrochemical Studies of Doping Processes in Poly(3,4-alkylenedioxithiophene)s Part 1: PEDOT. *Electrochim. Acta* 2008, *53*, 4580–4590.

[37] G. Greczynski, T. Kugler, W. R. Salaneck, Characterization of the PEDOT:PSS System by means of X-Ray and Ultraviolet Photoelectron Spectroscopy. *Thin Solid Films* 1999, *354*, 129–135.

[38] J. Hwang, F. Amy, A. Kahn, Spectroscopic Study on Sputtered PEDOT:PSS: Role of Surface PSS Layer. *Org. Electron*. 2006, *7*, 387–396.

[39] P. C. Hütter, T. Rothländer, G. Scheipl, B. Stadlober, All Screen-Printed Logic Gates Based on Organic Electrochemical Transistors. *IEEE Trans. Electron Devices* 2015, *62*, 4231–4236.

IV Summary and Outlook

In this chapter the targets defined in the introduction of this thesis are recapitulated. Results of the presented research and how they contribute to achievement of the aims are summarized. Finally an outlook on valuable research goals building on these results is presented.

A goal of this work was to use simple techniques to fabricate the presented organic electronic transistors and logic circuits, preferably processes focusing on printing techniques. Any complicated fabrication routes including vacuum and etching processes, demanding sophisticated and expensive equipment and potentially dangerous and health hazard chemicals, should have been avoided. With the presented entirely inkjet-printed and entirely screen-printed OECTs and also logic circuits we were successful in demonstrating fabrication routes involving only printing steps. The number of steps necessary to prepare a transistor is only three for both the inkjet-printing and screen printing fabrication routine, with only three different materials involved. The three step screen-printing process is displayed in Figure A.1. Three different materials and three process steps are also enough to prepare the entirely inkjet-printed inverters. Inverters, NAND gates, flipflops and the 2-bit shift register fabricated by screen-printing demanded a process containing six printing steps and five different materials, which is still very simple considering the complexity of the demonstrated logic circuits. The presented results clearly show the suitability of printing processes for the entire fabrication of OECTs and OECT-based circuits.

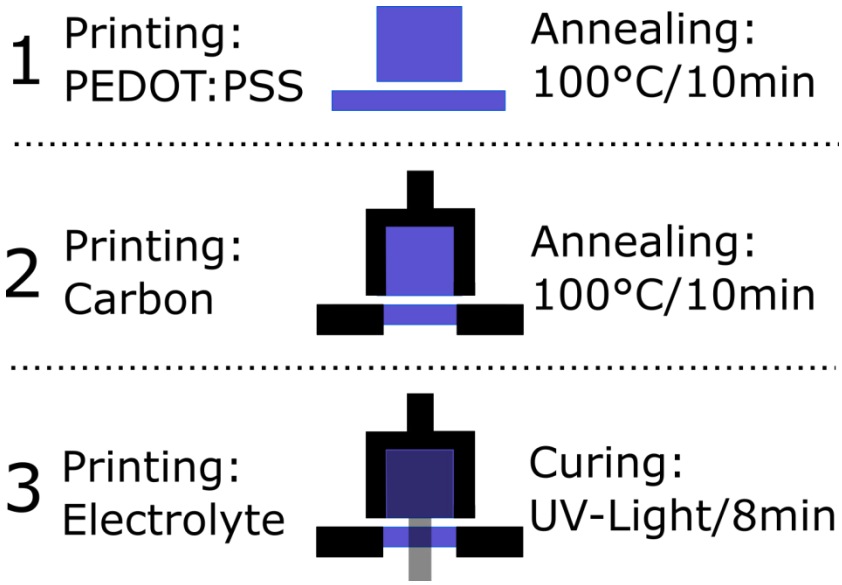


Figure A.1: Screen-printing fabrication process

The hybrid inkjet-printing/Nanoimprint-lithography process is against the intent of keeping the fabrication routing as simple as possible. In this process a dry etching step and the wet chemically removing of an imprint resist is needed. This compared to printing complex fabrication pathway was necessary to fabricate transistors with dimension being way beyond the resolution limit of printing. These miniaturized transistors were used to validate the results

on the geometry/performance relationship obtained for entirely inkjet-printed OECTs. Printing transistors and varying the thickness of the electrodes, the width of the source-drain line and the gap between the source-drain line and the gate electrode the influence of the transistor geometry on the on-current and the on/off-current ratio was examined. The varied geometry parameters are displayed in Figure A.2a Thicker electrodes lead to an enhanced on-current due to a reduced resistance of the source-drain line but also to a higher off current, so no benefit concerning the on/off current ratio is derived from the enhanced on-current. A possible explanation for this effect might be the larger distance between the electrolyte/electrode interface and the bottom of the electrode, making a complete reduction of the PEDOT:PSS in the entire electrode less likely. The same holds true for a variation of the width of the source-drain line, but much less pronounced. Broader lines lead to slightly higher on currents due to a reduced resistance, but no significant enhancement of the on/off current is visible. Here a lack of reduction in the area facing away from the gate electrode might be the reason for the insufficient switching-off of the transistor, leading to a higher off-current that is compensating the positive effect of a higher on-current on the on/off-current ratio. But, as stated before, this effect is much less pronounced then the effect of the higher electrode thickness. Reducing the gap between the source-drain line and the gate electrode is leading to a higher on/off-current ratio. The on-current remains unchanged, so the enhancement must be a result of a better switching-off of the transistor, most likely based on a bigger driving force for the reduction when the gate electrode is in close proximity to the source-drain electrode. These investigations resulted in a comprehensive overview on the geometry/performance relationship of OECTs. The majority of the results are validated by measurements conducted with transistors fabricated either by the hybrid inkjet-printing/Nanoimprint-Lithography process or by screen printing. The miniaturized transistors showed an on/off-current ratio enhancement of one order of magnitude compared to inkjet-printed transistors, exhibiting a drastically reduced gap between the transistors electrodes and also narrower source-drain electrodes. But the effect of miniaturization was smaller than expected, indicating that the performance might not be enhanced by further size reduction. Using screen-printed transistors not only the results concerning the geometry/performance relationship obtained for the inkjet-printed ones were validated, also a new design parameter was examined: the volume of PEDOT:PSS in the transistor channel, displayed in Figure A.2b. By changing this volume and monitoring the gate current during the switching process of the transistor, a linear relationship between the amount of PEDOT:PSS and the charge necessary to switch-off the OECT was found. Higher volumes lead to a larger amount of PEDOT:PSS

needing to be reduced during switching, resulting in an increased charge consumption. This data was also used to examine the electrochemical switching process on a microscopic level. By determination of the potentially redox active share of bulk material in the channel and examination of the charge carrying species the amount of PEDOT actively participating in the electrochemical switching process was identified. The results indicate that a smaller volume of PEDOT:PSS in the channel is favorable as the amount of inactive PEDOT, not participating in the switching process, is increasing disproportionately with increasing channel volume. All of those results concerning the relationship between the geometry and the performance of organic electrochemical transistors tremendously enhance the understanding of their working principle and their predictability.

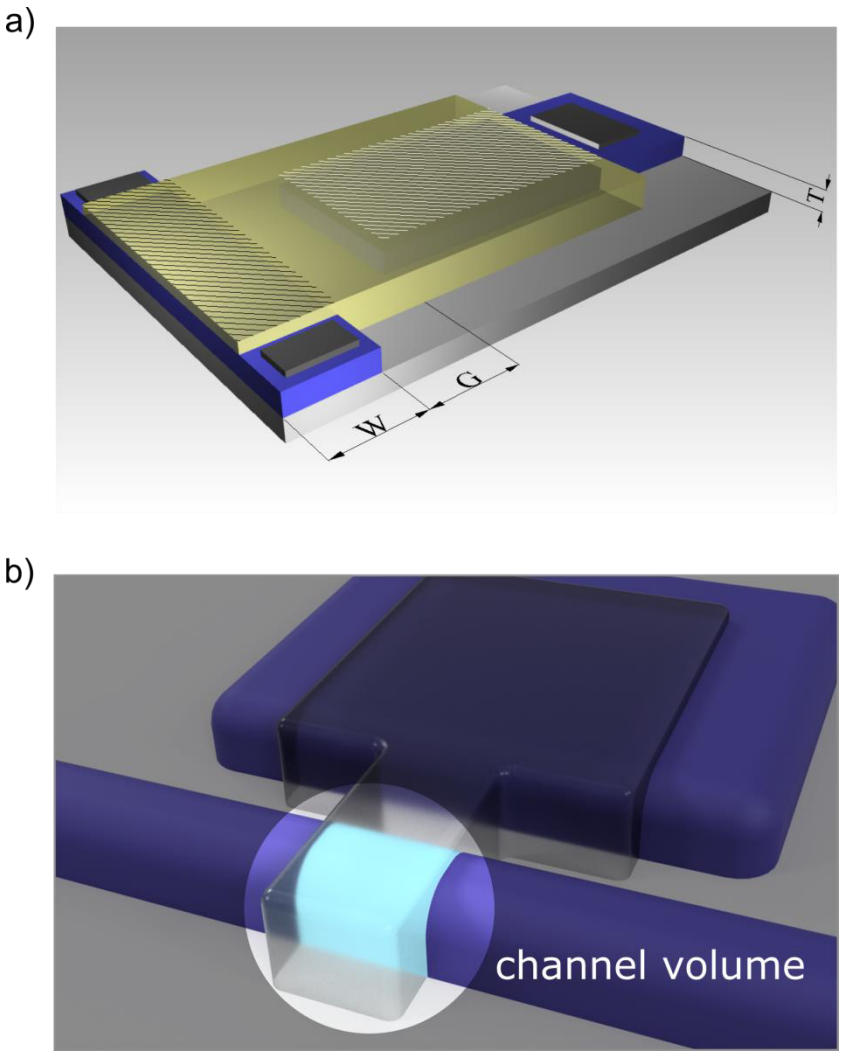


Figure A.2: Geometry parameters that are modified to examine the influence on the transistor performance at a) entirely inkjet-printed and b) entirely screen-printed devices.

Screen-printed transistors were not only used for performance examinations, they were also used to reveal the degree of reproducibility and uniformity achievable by screen-printing fabrication processes. For that reason logic circuits were fabricated based on a large number of single devices. The basic building blocks were OECTs and resistors, also made from PEDOT:PSS. Their resistance was controlled by the length of the resistive line and had to be adapted to fit the transistor characteristics. A precise fabrication was thereby inevitable. Three resistors with a certain ratio are necessary for an inverter. Measuring 90 resistors a deviation fewer than 5% was obtained for this resistor ratio, demonstrating the high uniformity obtainable by the printing process. Printed devices were used to fabricate inverters, NAND gates, flipflops and also a 2-bit shift register. For one flipflop 18 transistors and 30 resistors are needed, giving a total number of more than 380 basic building blocks for the eight flipflops whose output signals are depicted in figure A.3a, showing only a small deviation. A photograph depicting a segment of the printed circuits on PET-foil is displayed in Figure A.3b. The first time demonstration of such complex circuits based on OECTs that are entirely screen-printed marks a big leap forward in for the field of large area printed organic electronics.

But logic circuits were not only demonstrated using screen-printed transistors and resistors. Also every other fabrication technique resulted in working logic gates. Using inkjet-printing entirely printed inverters were demonstrated, the hybrid inkjet-printing/Nanoimprint-Lithography process brought out inverters and also NAND gates. Successful fabrication of the latter marks a leap forward as any Boolean function can be implemented by using a combination of NAND gates. Obtaining this significant building block opened the opportunity for the fabrication of the complex logic circuits by screen-printing.

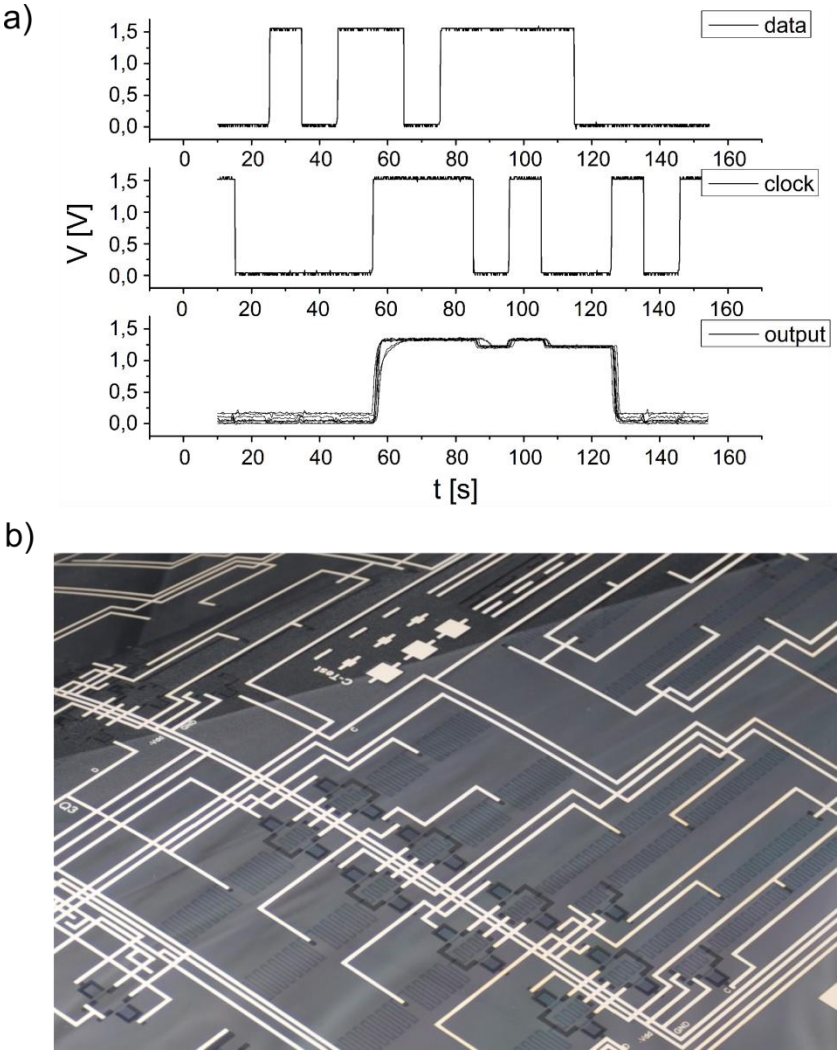


Figure. A.3: a) Output signals of 8 flipflops, containing more than 380 screen printed transistors and resistors in total. b) Segment of the A3 size PET-foil containing four entirely screen-printed flipflops

With the capabilities of printing processes demonstrated, the next goal could be to transfer the fabrication of OECTs and circuits to high throughput fabrication methods, like roll-to-roll processing. Materials processible out of solution are a basic requirement for this processing, a requirement met by a majority of the materials used in this work. Further research will be necessary to adapt those materials to the specific processing needs concerning the viscosity, the polarity or wetting/de-wetting behavior, to name only a few. Once this transfer was successful, a production by roll-to-roll Nanoimprint-Lithography would be a goal worth pursuing. This method is combining both high throughput and high lateral resolution, widening the field of possible applications.

Using the logic circuits based on OECTs demonstrated in this work in the field of sensing might be beneficial as well. OECTs are commonly used as sensors and the demonstrated logic circuits

could provide supportive electronics. Using the principle of electrochemical doping/de-doping also electrochromic displays can be obtained. Sensors, read-out logic and a simple electrochromic display combined, all using the same set of materials and entirely printed, might be of great use as a sensing unit. So is the implication of the OECTs on simple disposable “Lab on a Chip”-type devices, a very interesting and “hot” topic of research.

In my opinion the organic electrochemical transistors is contributing massively to the bright future of organic electronics.