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Pentacene and Epindolidione Based Organic Thin-Film Transistors:

In Situ Preparation, Modification and Characterization

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ABSTRACT

This thesis covers electrical and surface analytical investigations of organic thin-film transistors. The most distinct aspect of the experimental work was that the organic film preparation, as well as the chemical and electrical characterization of the organic devices, were performed *in situ* under ultra-high vacuum conditions. This allowed unprecedented measurements of the performance of organic transistors, in particular with regard to reproducibility and the correlation between film morphology and electrical properties. To this end, *in situ* Auger Electron Spectroscopy and Thermal Desorption Spectroscopy, as well as *ex situ* Atomic Force Microscopy were applied to determine the chemistry, thermal stability and morphology of the dielectric substrates and the semiconducting organic layers. A special sample holder allowed the cooling and heating of the organic devices, thus enabling the study of the transistor performance *in situ* as a function of film thickness, sample temperature and substrate modifications.

In particular, organic transistors with pentacene and epindolidione as the active semiconducting material, and silicon dioxide, as well as spin-coated capping layers PVCi and PNDPE as dielectric substrate, were prepared and characterized. The main findings can be summarized as follows: The transistor properties, mainly characterized by the charge mobility and threshold voltage, were governed by a subtle interplay between the grain size and density, the molecular ordering in the grains, and the overlap between the organic film and the gold contacts. Deposition of the film at elevated temperature increased the grain size and the molecule ordering, thus increasing the charge mobility; however, at the same time dewetting effects diminished the overlap between the organic film and the gold source and drain contacts, thus decreasing the attainable drain current and consequently the mobility. With an elaborate deposition technique, by utilizing the specific layer growth modes at different substrate temperatures, this restriction could be overcome and excellent mobilities for the pentacene/silicon dioxide system at comparably low film thickness were obtained.

Another important parameter for the film formation was the diffusivity of the organic molecules at the substrate. The diffusivity could be intentionally altered by ion sputtering of the silicon oxide substrate and a modification of the silicon oxide by less polar organics, such as PVCi and PNDPE, which both influenced the resulting mobility considerably. One of the main results of this work was the finding that only 3 - 4 layers of the organic film contributed to the major part of the drain current.

KURZFASSUNG

Die vorliegende Dissertation befasst sich mit der elektrischen und oberflächenanalytischen Charakterisierung von organischen Dünnschichttransistoren. Ein Großteil der experimentellen Arbeiten wurde dabei *in situ* unter Ultrahochvakuumbedingungen durchgeführt. Dadurch war es möglich die Leistungsfähigkeit der organischen Transistoren zu untersuchen, im Besonderen in Bezug auf Reproduzierbarkeit und die Zusammenhänge zwischen Schichtmorphologie und elektrischen Eigenschaften. Zusätzlich zu der elektrischen Charakterisierung wurden sowohl *in situ* Auger Elektronenspektroskopie und thermische Desorptionsspektroskopie, als auch *ex situ* Rasterkraftmikroskopie eingesetzt um die chemische Zusammensetzung, thermische Stabilität und Morphologie der dielektrischen Substrate und organischen Schichten zu bestimmen. Der Einsatz eines spezifisch dafür konstruierten Probenhalters ermöglichte das Heizen und Kühlen der Proben, sowie Untersuchungen der Transistoreigenschaften als Funktion der Schichtdicke, der Temperatur und von Oberflächenmodifikationen.

Pentacen und Epindolidione Transistoren mit den Dielektrika SiO_2, PVCi und PNDPE wurden hergestellt und charakterisiert. Die dabei gewonnenen Haupterkenntnisse waren, dass die Transistoreigenschaften, repräsentiert durch die Ladungsträgermobilität und Einsatzspannung, vorwiegend durch ein Zusammenspiel der Korngröße und –dichte im Halbleiter, der Struktur in den Körnern und der Überlappung der Halbleiterschicht mit den Goldkontakten bestimmt werden. Filmabscheidung bei erhöhter Substrattemperatur steigerte die mittlere Korngröße und Ordnung im Film, wodurch sich einerseits die Mobilität erhöhte aber andererseits auch Entnetzungseffekte begünstigt wurden, welche die erreichbaren Leistungsparameter negativ beeinflussten. Ein spezialisiertes Abscheidungsprotokoll bei verschiedenen Abscheidungstemperaturen konnte die Vorteile beider Bereiche kombinieren und führte zu exzellenten Mobilitäten bei verhältnismäßig geringen Pentacen Schichtdicken.

Ein weiterer wichtiger Parameter des Filmwachstums war das Diffusionsvermögen der organischen Moleküle auf dem Dielektrikum. Dieses konnte mittels Argon-Ionen-Sputtern oder Benetzen des Siliziumoxids mit weniger polaren Schichten wie PVCi und PNDPE bewusst modifiziert werden und wirkte sich direkt auf die erreichbare Ladungsträgermobilität aus, welche zum überwiegenden Teil von den untersten 3 – 4 Schichten des Halbleiters bestimmt wurde.

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List of Abbreviations and Acronyms

OTFT	Organic Thin-Film Transistor
UHV	Ultra-High Vacuum
ML	Monolayer
AES	Auger Electron Spectroscopy
TDS	Thermal Desorption Spectroscopy
AFM	Atomic-Force Microscopy
FET	Field-Effect Transistor
MTR	Multiple Trapping and Release Model
QMS	Quadrupole Mass Spectrometer
QMB	Quartz Microbalance
PVD	Physical Vapor Deposition
PVCi	poly(vinyl-cinnamate)
PNDPE	poly((±)endo,exo-bicyclo[2.2.1]hept-5-ene-2,3-dicarboxylic acid, diphenylester)

U_{DS}	Drain-Source Voltage
I_{DS}	Drain-Source Current
U_{GS}	Gate-Source Voltage
μ	Charge Carrier Mobility
μ_{Lin}	Charge Carrier Mobility in the Linear Regime
μ_{Sat}	Charge Carrier Mobility in the Saturation Regime
U_{Th}	Threshold Voltage
U_{On}	Onset Voltage
I_{On}/I_{Off}	On- to Off-Current Ratio
U_{Eff}	Effective Gate Voltage
Q	Number of Charge Carriers

C_G	Gate Dielectric Capacitance
W	Transistor Channel Width
L	Transistor Channel Length
n	Charge Carrier Density
d	Thickness of the Dielectric
μ_{Eff}	Effective Charge Carrier Mobility
μ_0	Intrinsic Free Charge Carrier Mobility
E_A	Activation Barrier Height
k_B	Boltzmann Constant (1.38×10^{-27} J/K)
T	Temperature
N_C	Density of States at the bottom of the band
N_T	Trap Density
R_C	Contact Resistance
$D(E)$	Density of States
E_F	Fermi Energy
$f(E,E_F)$	Fermi Function
N	Number of States
$\vec{E}$	Electric Field
$\overrightarrow{v_d}$	Charge Carrier Drift Velocity
V_{LJ}	Lennard-Jones Potential
E_a	Depth of the Potential Well in the Lennard-Jones Model
δ	Distance for Zero Inter-Particle Potential
r	Distance between Particles
s	Sticking Coefficient
D	Diffusion Coefficient
ν_D	Attempt Frequency for Diffusion
a	Lattice Constant

z	Number of Nearest Neighbor Sites
E_{Diff}	Activation Energy for Diffusion
S_D	Diffusion Entropy
i	Critical Island Size
Θ	Coverage
ΔE_{ES}	Ehrlich Schwoebel Barrier
R	Desorption Rate
ν_0	Attempt Frequency for Zero Order Desorption
N_{ML}	Molecular Surface Density
E_{Des}	Desorption Energy
T_M	Maximum Desorption Temperature
β	Heating Rate
amu	Atomic Mass Units (1 amu = 1.66×10^{-27} kg)
Δf	Change in Quartz Resonance Frequency
Δd	Thickness of Deposited Material
S	Quartz Sensitivity (2.26×10^{-6} cm^2s/g)
f_0	Eigenfrequency of the Quartz Oscillation (6 MHz)
ρ	Density of the Deposited Material
T_{Corr}	Corrected Temperature
T_0	Adsorption Temperature
T_M^{SS}	Maximum Desorption Temperature from the Stainless Steel Plate
T_M^{Si}	Maximum Desorption Temperature from the Silicon Sample
ε_0	Dielectric Permittivity (8.8×10^{-12} As/Vm)
ε_r	Relative Dielectric Permittivity

1 INTRODUCTION

Electronic devices based on organic semiconductors are on the verge of taking over large shares of several markets currently dominated by inorganic systems. Organic electronics is therefore already far beyond being a primarily research specific term and is frequently used in today's marketing strategies, symbolizing high quality, cutting-edge technology [1,2]. The field remains highly relevant for the future of our electronic world, as it offers the possibility to utilize highly advantageous organic material properties for present-day and prospective applications. The widespread scientific interest in organic electronic devices can be largely attributed to the unique possibility to deposit and pattern the involved semiconducting materials at room temperature, while maintaining excellent biodegradability and biocompatibility [3,4]. This enables the creation of low-cost, large-area electronic functions on flexible substrates via comparably inexpensive processes and therefore to realize applications not feasible with silicon or other inorganic transistor technologies [1,5–12]. Some examples for devices based on these unique advantages are displayed in **Figure 1.1**.

As one of the most basic building blocks of organic electronic devices, switches in the form of organic thin-film transistors (OTFTs) [13,14] are one of the pillars for technological success. While the possibility to create and optimize organic devices is evident, to the present date, many of the underlying principles affecting critical device parameters such as performance and lifetime are not yet fully understood and controllable in satisfactory detail, as outlined in a number of review articles [13,15–17]. In general, the film morphology of the active layer, the molecular ordering, and chemical impurities are recognized as prominent factors for the attainable OTFT

performance [18–25]. Additionally, high performance organics are often sensitive to oxygen [26,27], humidity [28], and light exposure [29], leading to, sometimes severe, device degradation under ambient conditions and limited operational lifetime.

To gain conclusive insight into thin-film growth and the connected electrical properties, recently several groups turned their attention to *in situ* measurements under vacuum conditions, in an effort to improve reproducibility and reduce atmosphere induced contamination and degradation [30–38]. Some experimental work showed that ultra-high vacuum (UHV) chamber deposition, in combination with *in situ* surface analytical and electrical characterization, is able to accurately connect active layer growth and morphology with the resulting electrical transistor properties, based on specific, well-controlled surface alterations [18,19]. One distinguished and common point of interest is the number of closed monolayers (ML) at which the rise in mobility with increasing coverage saturates and therefore indicates the maximum effective Debye length in the film [39,40]. This was subject-matter of a number of articles [30,31,34,36,39–43] and formed the basis for our publications on this topic [44–46].

Being part of organic thin-film transistor research and development for almost 25 years [47–49], the polycyclic aromatic hydrocarbon pentacene ($C_{22}H_{14}$, **Figure 1.2 (a)**) has earned a reputation as a working horse material in OTFT fabrication [50]. This is for the most part attributable to the attainable high charge carrier mobilities of greater than 1 cm^2/Vs [50–52] and can be related to the materials tendency to form well-ordered layers of standing molecules with excellent long axis alignment of the five linearly connected benzene rings [53,54], which form the molecules structure [20]. Typically, pentacene is deposited in vacuum on a gate dielectric of choice, with gold electrodes in a bottom or top-contact configuration. Subsequently, the devices are contacted and electrically characterized in air. Recently, some investigations on *in situ* pentacene device fabrication and electrical characterization have been reported as well. Kiguchi *et al.* [30] were one of the first to study the conductivity of pentacene films *in situ* continuously during film growth, and found that the accumulation layer is just a few nm thick. Similar experiments were performed by Liu *et al.* [31], who additionally focused on the role of pentacene purification [32] and on the influence of vacuum breaking on the device performance [33]. Furthermore, *in situ* and real time electrical measurements were also carried out in the group of Biscarini [34,35], who studied the influence of the deposition rate on the device performance and on the number of active layers

contributing to the drain current. Finally, the evolution of mobility, threshold voltage, and hysteresis during pentacene deposition was investigated *in situ* by Fiebig *et al.* [36].

In order to go beyond this type of *in situ* research on organic semiconductors, the focus of this work was the analysis of the semiconducting layer in organic thin-film transistors through a unique combination of *in situ* layer deposition, real-time electrical *and* surface analytical characterization, with all investigations being performed under ultra-high vacuum conditions. A specialized experimental setup enabled full control over the semiconductor deposition process through precise deposition temperature and rate adjustment, as well as exact sample surface temperature control and variation between 120 K and 800 K, during and subsequent to the deposition itself. Through this, it was possible to realize unprecedented investigations during deposition and during layer thinning by thermal desorption. Auger electron spectroscopy (AES) was applied to control the chemical composition of the surfaces involved prior and after film deposition. The deposited film could also be desorbed and analyzed by Thermal Desorption Spectroscopy (TDS) in a controlled way, establishing the thermal stability of the film. Due to the fact that repeated film deposition and removal could be achieved without breaking the vacuum, it was possible to test the influence of various parameters on the reproducibility of the transistor characteristics, such as argon-ion sputtering of the gate dielectric ahead of semiconductor deposition. *Ex situ* atomic-force microscopy (AFM) was used to characterize the morphology of the films.

Following the successful implementation of pentacene OTFTs and the pioneering success by Głowacki *et al.* [4,55–57], the organic pigment epindolidione ($C_{16}H_{10}N_2O_2$, **Figure 1.2 (b)**) was investigated as well. As a hydrogen-bonded analogue of the well-studied tetracene, it had emerged as one of the most interesting candidates for the active layer material in OTFTs [25,58]. As a structural isomer, the yellow to orange colored epindolidione is closely related to the industrially mass produced indigo, a blue organic dye with which it shares many advantageous properties. Epindolidione based OTFTs had shown excellent application potential, featuring very promising charge carrier mobility values of up to 1.5 cm^2/Vs for p-type conduction [55], electrode material and derivatization induced n-type behavior, high air, water and temperature stability, excellent biocompatibility, and stable operation in ionic solutions in a pH range of 3 to 10 [57].

The same specialized experimental setup was applied which enabled the manufacturing and characterization of electrical and surface physical properties of

epindolidione OTFTs *in situ* under ultra-high vacuum conditions. While inferior in terms of charge carrier injection and therefore maximum attainable mobility [14,59], the employed bottom-gate geometry allowed more insight into the correlation between semiconducting and growth properties to be gained. An investigation of the layer growth and transistor behavior of epindolidione as a function of the employed gate dielectric material, its surface treatment, i.e. sputtering, and of the sample temperature over a wide temperature range was performed. The *in situ* experiments were again complimented by *ex situ* AFM measurements.

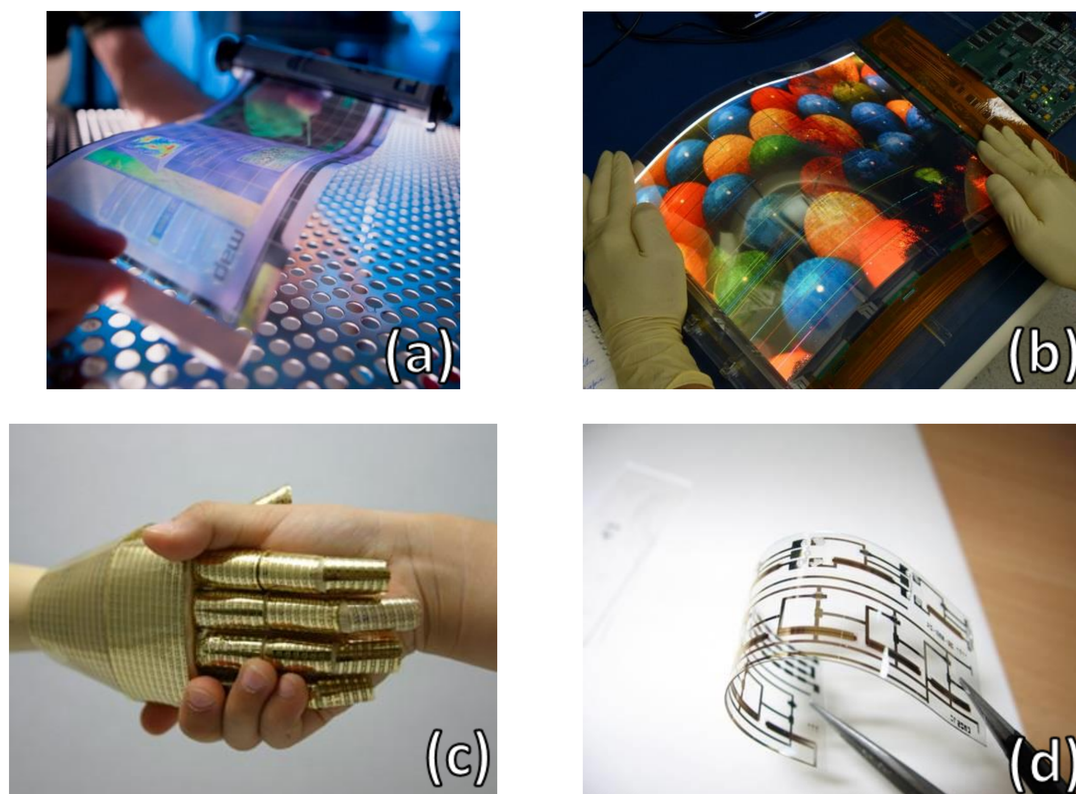


Figure 1.1: Various examples for the application of organic electronics based on flexible substrates, such as (a) and (b) displays [60,61], (c) artificial skin [62], and (d) circuitry [63].

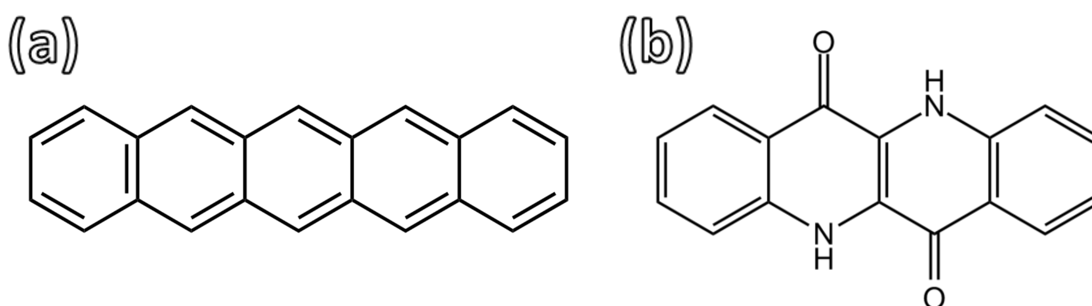


Figure 1.2: Chemical structure of (a) pentacene and (b) epindolidione.

1.1 General Organization of this Thesis

In this thesis, electrical and surface analytical studies on pentacene and epindolidione organic field-effect transistors will be discussed in detail. The applied experimental methods include electrical characterization as a function of dielectric material, sample and device temperature during deposition and surface analytical characterization by thermal desorption spectroscopy, Auger electron spectroscopy and *ex situ* atomic-force microscopy.

Chapter 2 outlines the fundamental theoretical aspects of organic transistor technology, charge transport, parameter extraction and characterization. Additionally, the basic physical principles of semiconducting layer formation, including the adsorption process and nucleation are covered.

In chapter 3 the main analytical methods employed throughout this work and their applicability to the present experimental challenges are covered, namely thermal desorption spectroscopy, Auger electron spectroscopy and atomic-force microscopy.

Chapter 4 then focusses on the experimental setup and instrumentation used throughout this work, as well as the sample and device preparation and the corresponding method and material choices. Details on the sample temperature control and surface modification through argon-ion sputtering are also found here.

The following three chapters then represent the main body of this thesis, detailing all experimental results. The basic field effect transistor investigations for pentacene are covered in chapter 5, optimization of the semiconducting layer growth and pentacene device performance are detailed in chapter 6 and finally, chapter 7 covers the application of the then well-established experimental system to an up-to-date organic semiconductor in the form of epindolidione.

The concluding chapters contain a short summary of the results and findings obtained in the scope of this thesis and a list of conference contributions in chapter 8 and the list of literature references in chapter 9.

1.2 List of Enclosed Publications

PAPER I (REF. [44])

***In situ* preparation, electrical and surface analytical characterization of pentacene thin film transistors**

R. Lassnig, B. Striedinger, M. Hollerer, A. Fian, B. Stadlober and A. Winkler

Journal of Applied Physics **116** (2014) 114508

Author Contribution: Following the successful implementation of *in situ* OTFT fabrication and characterization for our vacuum setup, pentacene based model devices were studied in detail. This work focused on the electrical device properties as a function of film morphology, preparation, and characterization temperature. B. Striedinger applied the gold bottom-contacts to the SiO_2 samples and in conjunction with A. Fian and B. Stadlober assisted in the interpretation of data. M. Hollerer performed the auxiliary AFM measurements. All pentacene deposition, TDS, and electrical characterization experiments were performed by R. Lassnig.

The publication was written by R. Lassnig in accordance with input and corrections from Prof. A. Winkler, who supervised this project.

Large parts of this publication were used in chapter 5.

PAPER II (REF. [45])

Optimizing pentacene thin-film transistor performance: Temperature and surface condition induced layer growth modification

R. Lassnig, M. Hollerer, B. Striedinger, A. Fian, B. Stadlober and A. Winkler

Organic Electronics **26** (2015) 420-428

Author Contribution: In extension of the previous publication, this work included investigations and possible routes of performance optimization for pentacene deposition at different temperatures and on sputtered SiO_2. M. Hollerer performed detailed AFM analysis on different pentacene layer thicknesses on the gold contacts, SiO_2, and the transition between those regions. B. Striedinger applied the gold bottom-contacts to the SiO_2 samples and in conjunction with A. Fian and B. Stadlober assisted in the

interpretation of data. All pentacene deposition, surface modification and electrical characterization experiments were performed by R. Lassnig.

The publication was written by R. Lassnig in accordance with input and corrections from Prof. A. Winkler, who supervised this project.

Large parts of this publication were used in chapter 6.

PAPER III (REF. [46])

Temperature and layer thickness dependent in situ investigations on epindolidione organic thin-film transistors

R. Lassnig, B. Striedinger, A. O. F Jones, B. Scherwitzl, A. Fian, E. D. Głowacki, B. Stadlober and A. Winkler

Synthetic Metals **218** (2016) 64-74

Author Contribution: Following the successful studies on pentacene, the highly promising, hydrogen-bonded organic semiconductor epindolidione was investigated. Once more the influence of preparation and characterization temperature, as well as dielectric configuration on the resulting transistor performance was studied in detail. B. Striedinger applied the investigated organic dielectrics and gold bottom-contacts to the SiO_2 samples and in conjunction with A. Fian and B. Stadlober assisted in the interpretation of data. A. O. F. Jones performed X-ray investigations on epindolidione layers and supplied information on the epindolidione growth mode at different temperatures. B. Scherwitzl performed preliminary TDS evaluations on the material and came up with the suggestion to use epindolidione, which E. D. Głowacki supplied, in addition to consultancy in experimental matters. All epindolidione deposition, TDS, and electrical characterization experiments were performed by R. Lassnig.

The publication was written by R. Lassnig in accordance with input and corrections from Prof. A. Winkler, who supervised this project.

Large parts of this publication were used in chapter 7.

Co-Authorship Publications (Ref. [64,65])

Electrical in-situ characterisation of interface stabilised organic thin-film transistors

B. Striedinger, A. Fian, A. Petritz, R. Lassnig, A. Winkler and B. Stadlober

Physica Status Solidi Rapid Research Letters 9 Issue 7 (2015) 420-424

Author Contribution: R. Lassnig assisted in the interpretation of experimental data.

Adsorption, desorption and film formation of quinacridone and its thermal cracking product indigo on clean and carbon-covered silicon dioxide surfaces

B. Scherwitzl, R. Lassnig, M. Truger, R. Resel, G. Leising and A.Winkler

Submitted to Journal of Physical Chemistry C (May 2016)

Author Contribution: R. Lassnig supplied a number of AFM images and performed the analysis of the AFM data.

Structure solution of epindolidione from thin films and tuning of crystallite orientations

A. O. F. Jones, C. Röthel, O. N. Bedoya-Martinez, R. Lassnig, P. Christian, I. Salzmann, A. Winkler and R. Resel

Submitted to Journal of Physical Chemistry C (June 2016)

Author Contribution: R. Lassnig manufactured all investigated epindolidione films and supplied a number of AFM images, including analysis of the data.

Electrical in-situ characterisation of dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) OTFTs

B. Striedinger, A. Fian, A. Petritz, R. Lassnig, A. Winkler and B. Stadlober

Submission to Physica Status Solidi Rapid Research Letters in preparation

Author Contribution: R. Lassnig assisted in the interpretation of experimental data.

2 FUNDAMENTALS

Before going into the details of the experimental setup and sample preparation, the basic theoretical principles applied in this work are covered. This includes fundamental definitions and concepts for thin-film transistor technology, charge transport, and electrical performance parameter extraction. The second major part of this chapter contains the foundations of semiconducting material deposition, adsorption and film growth, as well as the thermal desorption of molecules.

2.1 Organic Thin-Film Transistors

As the fundamental building block for modern electronic devices, the transistor, in its most simple functionality as an on/off switch, represents the tool to translate binary code into electronic functions and vice versa. The following basic properties of field-effect transistors are largely based on the works by Sze and Ng [66]. In **Figure 2.1** the elementary components of a transistor, as employed throughout this thesis, are shown. The switch functionality relies on the regulation of the voltage (U_{DS}) driven current flowing in between the drain and source electrodes (I_{DS}). This is achieved by a potential applied to a gate electrode (U_{GS}), which is separated from the semiconducting channel by a dielectric. The current path running through the semiconductor between the source and drain electrodes is called the channel. Usually, the source electrode is grounded and used as a reference potential for the voltages applied to the gate and drain electrodes. Therefore, the terms drain and gate bias are used synonymous with drain-source and gate-source bias throughout this work. Since no significant current can flow between the gate and the other electrodes, the attainable drain-source current is modulated by the

gate potential induced electric field, leading to the terminology field-effect transistor (FET). As a subcategory of field-effect transistors, thin-film transistors (TFT) feature the eponymous relatively thin semiconducting layer and a number of operational differences compared to FET. Most notably, TFTs operate exclusively in the accumulation regime and therefore a simple attraction of mobile charge carriers by the gate potential towards the dielectric-semiconductor interface is responsible for the formation of the charge transporting channel. These mobile charge carriers can be injected from both electrodes and are not bound to generation in the semiconductor bulk. The depletion and inversion regimes essential to FET operation are not found in TFTs, as are the associated chemical doping regions. The majority of transistor systems employing organic materials as a semiconductor, including the devices investigated in this thesis, are TFTs [67].

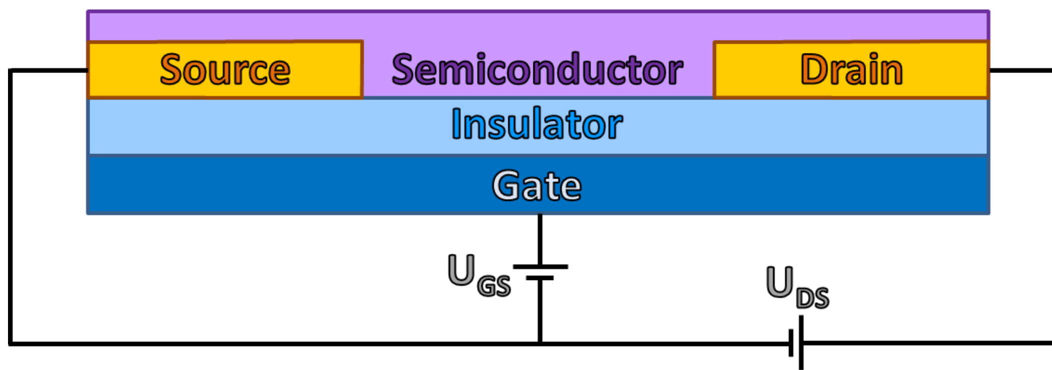


Figure 2.1: Schematic organic thin-film transistor structure and applied voltages between the gate and source (U_{GS}), as well as drain and source (U_{DS}) contacts.

OTFTs can be constructed in four basic configurations, termed after the order in the layering and/or deposition of the substrate, gate electrode, insulator or dielectric, semiconductor, and source and drain electrodes. In **Figure 2.2** the schematics of these four architectures are shown. Each arrangement features specific, geometry related, advantages and disadvantages when it comes to crucial device parameters such as charge carrier injection and transport, contact resistance, device degradation, and prominently the ease and feasibility of the manufacturing process itself. The bottom-gate, bottom-contact architecture had been chosen for this work, since it offered, among other advantages, the unique possibility to study the OTFT devices *in situ* under UHV conditions and during the semiconductor deposition and layer growth itself. In addition, it is very often the configuration of choice for industrial scale production based on large area deposition techniques, such as spin-coating or inkjet-printing [67].

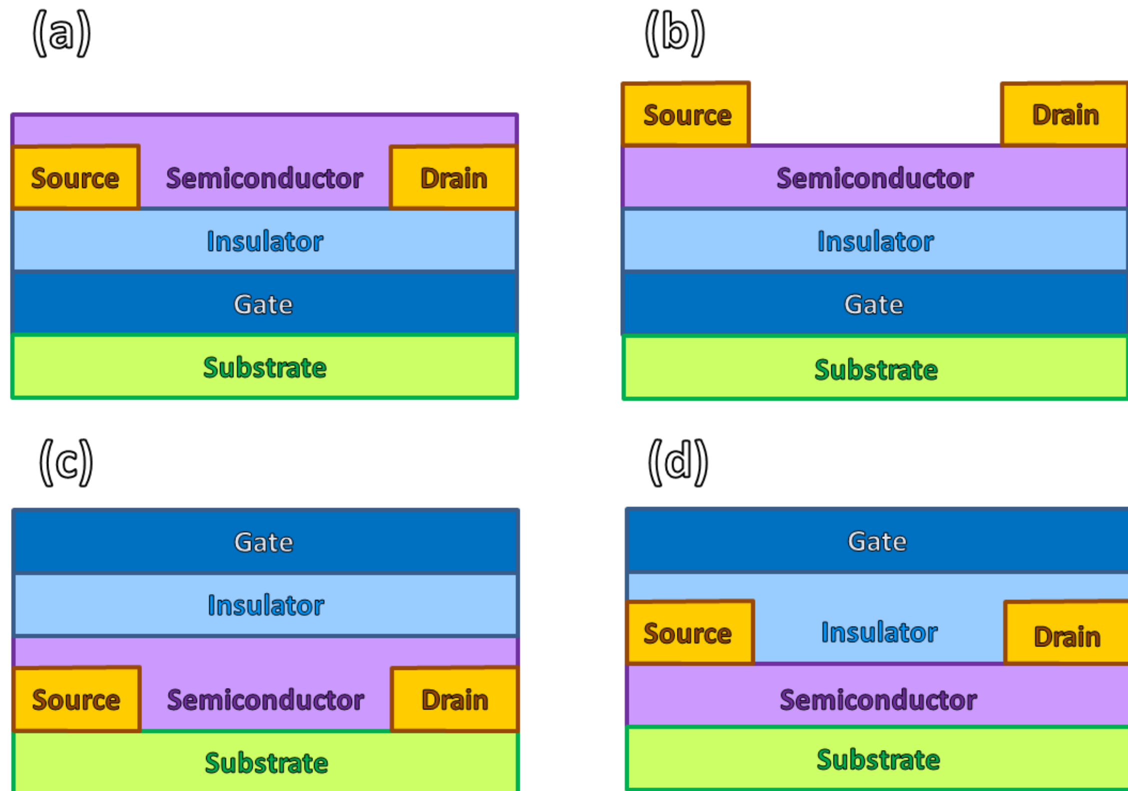


Figure 2.2: Basic organic thin-film transistor architectures: (a) Bottom-gate, bottom-contact, (b) bottom-gate, top-contact, (c) top-gate, bottom-contact, and (d) top-gate, top contact.

2.1.1 Basic Device Operation and Characteristics

In order to characterize and analyze OTFT properties, parameters of interest have to be defined and established. While not always applicable to its full extent [39,68], the formalism developed for silicon based FETs [66] has proven to be the most efficient and intuitive way to compare the performance characteristics between different samples and with results from other research groups. By setting either the drain-source voltage (U_{DS}) and sweeping the gate-source voltage (U_{GS}), or vice versa, and measuring the resulting drain-source current (I_{DS}) as a function of the swept voltage, so-called transfer and output characteristics can be generated for a device. In turn, these contain the necessary information to extract the parameters of relevance for organic transistor characterization. In our case, these parameters are the charge carrier mobility in the linear (μ_{Lin}) and in the saturation (μ_{Sat}) regime, the threshold (U_{Th}) and onset voltages (U_{On}), the on/off-ratio (I_{On}/I_{Off}), and the subthreshold swing, which will all be covered in more detail in the following sections [69–73]. In **Figure 2.3** exemplary transfer and output characteristics for commercial n-type, metal-oxide FETs are shown as extracted

from the corresponding data sheet, which have also been used to test the viability of the electrical measurement system. These characteristic curve progressions can also be found to a high degree in all transfer and output curves for OTFTs presented in this thesis and enable the formalism developed for inorganic FETs to be applied to OTFTs. Noticeable deviations in presented OTFT characteristics from the classical form displayed in **Figure 2.3** hint towards the limitations of the classical FET picture for organic semiconductors and the additional parameters not accounted for in the model and will be covered where applicable.

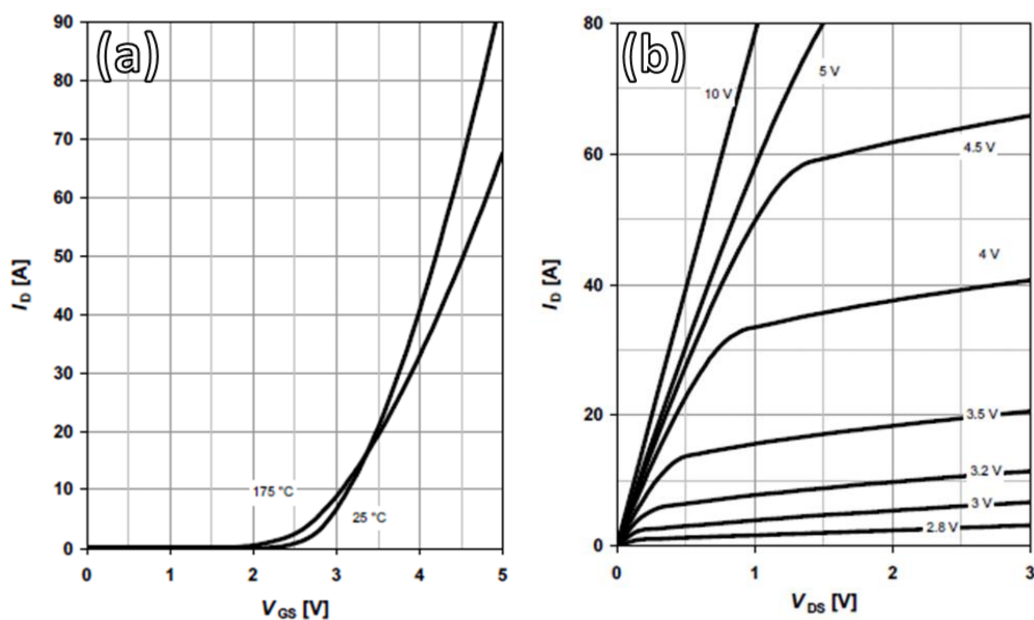


Figure 2.3: Characteristic n-type (a) transfer and (b) output curves for commercial metal-oxide power-FETs [74].

2.2 Charge Transport in Organic Materials

Contrary to inorganic FETs, no intrinsic free charge carriers exist in the semiconductor and as a consequence of the absence of any doping regions, ambipolar electron and hole transport is theoretically feasible. In practice most OTFTs operate in hole conduction. The main reason for this is the higher Schottky barrier for electron injection into organic semiconductors from the commonly used high work function metal electrodes. As mentioned in the previous chapter, TFTs operate in the accumulation regime. The application of a sufficient gate bias U_{GS} enables the uniform collection of mobile charge carriers, injected into the semiconductor from the source and/or drain electrodes, at the dielectric-semiconductor interface above the gate electrode. At the application of a drain-source bias U_{DS}, the mobile charge carriers can

then transport charge between these two electrodes. The gate voltage at which the channel first becomes conducting is the so-called onset voltage (U_{On}), which equals the flat-band voltage in the traditional FET picture and similarly the gate-source voltage at which the drain current is at its minimum [75]. In order to apply the formalism for parameter extraction developed for inorganic FET systems, the concept of a threshold voltage (U_{Th}) for the OTFT system was introduced [70]. While denoting the transition point from weak to strong inversion in traditional FETs [66], it signifies the necessary gate voltage to obtain *appreciable* drain current for OTFTs and therefore implies a current criteria for evaluation [19]. Both parameters, U_{Th} and U_{On}, have the same origin and have similar meaning, but follow different evaluation procedures. Often the *effective* applied gate voltage (U_{Eff}) is an important parameter for the analysis of an OTFT system, defined as the part of the applied voltage that actively contributes to the majority of the charge carrier generation above the gate dielectric:

$$U_{Eff} = U_{GS} - U_{Th} \tag{2-1}$$

Consequently the accumulated mobile charge Q at the semiconductor-dielectric interface is defined by

$$Q = C_G U_{Eff} \tag{2-2}$$

with the gate dielectric capacitance, C_G.

In **Figure 2.4** exemplary transfer and output characteristics for the p-type transistors investigated in this thesis are shown. The application of the drain-source bias U_{DS} leads to a shift in the previously uniform charge carrier distribution above the gate and, with the previously defined voltages, two conduction regimes can be established.

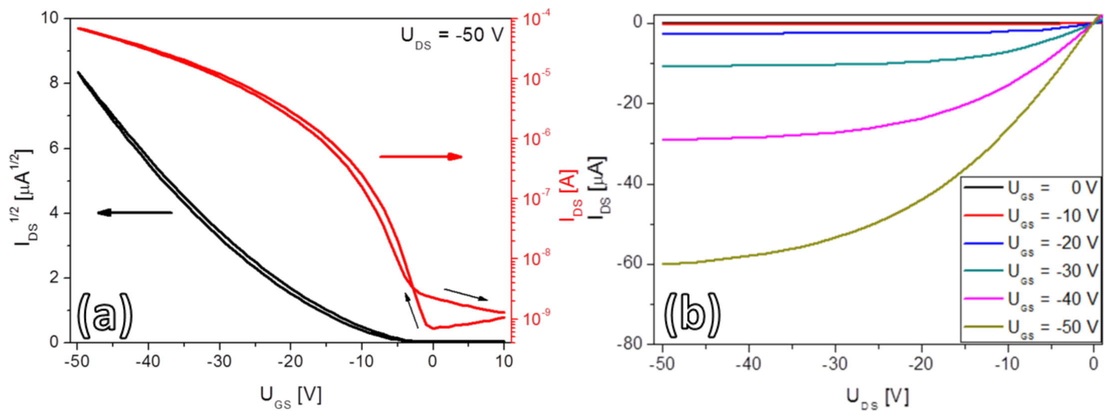


Figure 2.4: Exemplary transfer (a) and output characteristics (b), measured at 300 K, of an 8 nm thick pentacene film after deposition on a carbon covered device at 200 K.

For a certain gate voltage U_{GS} exceeding U_{Th}, one can assume that a fixed number of charge carriers Q is injected and supplied in relation to U_{Eff}. Then the drain current scales with the drain-source bias U_{DS} (**Figure 2.3 (b)** and **Figure 2.4 (b)**) in two distinct ways. For low drain-source bias U_{DS}, the drain current is not limited by the number of accessible charge carriers and increases linearly with the applied drain-source potential. This represents the so-called *linear regime* of OTFT operation. With increasing U_{DS}, a point is reached, where the fixed number of charge carriers supplied by the effective gate voltage U_{Eff} limits the attainable drain-source current. The so-called *saturation regime* is reached, where for a certain U_{GS} the eponymous saturation of I_{DS} as a function of U_{DS} is attained and the conducting channel is pinched-off in accordance to the classic FET picture and the current flow is then space-charge limited. Consequently, I_{DS} becomes independent of the drain-source voltage. The transition from the linear to the saturation regime can be observed in the evolution of the drain current in **Figure 2.4 (b)** from low to higher drain-source voltage (right to left). In terms of the established voltages the regimes can be characterized by:

Linear regime: $$|U_{GS} - U_{Th}| = |U_{Eff}| > |U_{DS}| > 0 \quad (2\text{-}3)$$

Saturation regime: $$|U_{DS}| > |U_{GS} - U_{Th}| = |U_{Eff}| > 0 \quad (2\text{-}4)$$

The transfer characteristics shown in **Figure 2.3 (a)** and **Figure 2.4 (a)** represent a different evaluation of the circumstances depicted in the output curves and the same two regimes can be specified. The drain-source potential U_{DS} is now the constant parameter and the low U_{GS} parts of the graphs represent the saturation regime, where the current is limited by the amount of mobile charge carriers supplied at a certain U_{GS}. With increasing gate bias, more and more charge carriers are injected into the semiconductor until the applied drain source voltage doesn’t suffice to utilize the present number of charge carriers to its full extent. The drain current as a function of the drain source voltage U_{DS} is therefore once more in the linear regime. This linearity is observable in the spacing of transfer characteristics for a number of drain-source voltages and a specific gate-source voltage (not shown here). In **Figure 2.4 (a)** a logarithmic ($\log(I_{DS})$ vs. U_{GS}) and a square root representation ($\sqrt{I_{DS}}$ vs. U_{GS}) of the drain current are depicted, highlighting the quadratic dependence of the attainable drain current as a function of the applied gate bias in the saturation regime. For output curves, as depicted in **Figure 2.4 (b)**, the same quadratic relationship can be observed. At a fixed

drain-source voltage U_{DS}, the attained I_{DS} values then show the quadratic spacing as a function of the applied gate voltage U_{GS}.

In both regimes, the channel itself acts as a resistor. The equivalent resistance is determined by the channel length L, defined as the shortest drain-source contact distance, and the channel width W in the perpendicular in-plane direction. Additionally, the charge transport properties in the semiconductor itself, related to the charge carrier density n and mobility μ and gate dielectric parameters, such as thickness d and capacitance C_G, are of crucial importance for the resulting electrical performance. The square-root representation is generally the data representation of choice in order to extract the threshold voltage (U_{Th}) and consequently charge carrier mobility in the linear (μ_{Lin}) and, more commonly, the saturation (μ_{Sat}) regime [76,77]. Additionally, the logarithmic form of representation immediately yields the onset voltage U_{On}, as specified before, and the on/off-ratio (I_{On}/I_{Off}), defined as the ratio between the highest and lowest attainable drain currents in the corresponding on and off states. From the first major rise of the logarithmic transfer curve as a function of gate bias the subthreshold swing can be extracted, which is the inverse of the slope in this regime and noted in V/decade. An optimal OTFT features a low onset voltage and threshold voltage, as well as a high on/off-ratio and subthreshold swing.

2.2.1 Charge Transport Mechanism and Temperature Dependence

Due to the fact that all our devices show a rather low mobility, in large part attributable to the, maximum performance wise, inferior bottom-contact architecture [14,59], we assume that the contact resistance should play only a minor role for the mobility determination from the transfer curves. The contacts are able to supply the channel with a sufficiently high amount of charge carrier and the temperature dependence of the effective mobility should then by largely determined by the properties of the organic film itself.

Several models have been discussed in the literature for the charge transport mechanism in organic electronics [67,73]. Unlike in inorganic semiconducting systems, band-like charge transport by delocalized states is generally assumed not to play the most significant role in polycrystalline or amorphous organic materials [78,79]. Horowitz *et al.* [13] have shown that the mean free path of charge carriers can actually be shorter than the mean atomic distance, invalidating a pure band-like charge transport model. Charge hopping and tunneling between localized states and their activation into

temporary delocalized states are the major contributions to charge transport. This often encompasses the intermolecular overlap of orbitals of states that are delocalized over a single molecule (intramolecular delocalization). This entails, that the layer formation and the relative orientation of molecules and grains to each other becomes highly significant for the charge transport. For the sheet-like, benzene ring based molecules pentacene and epindolidione studied in the present work (**Figure 1.2**), the charge transport largely relies on the stacking and overlap of the π-orbitals perpendicular to the ring planes between neighboring molecules [80,81]. This so called π-π stacking of the molecules will be covered in more detail in section 2.3 on the semiconductor deposition and layer formation.

In the following, a number of charge transport mechanisms are described, which are all temperature-dependent to some degree. A comprehensive, schematic overview of the involved transport regimes of interest is depicted in **Figure 2.5**. The most frequently discussed model is the so called MTR (multiple trapping and release) model, which assumes that most of the carriers are trapped in localized states, which have to be promoted temporarily into a delocalized band, in which charge transport occurs (**Figure 2.5 (c)**). In this case, the drain current depends on the activation barrier between the localized trap level and the delocalized band edge [13,82]. Contrary to inorganic FET, thermally induced phonon scattering is not the main limiting factor for charge transport and the mobility has been shown to increase with temperature [83]. According to the MTR model [67,79,84], the effective mobility μ_{Eff} is determined by a recurrent charge carrier trapping, where the mobility is naturally zero, and subsequent release from shallow trap states below the conduction band edge. By assuming, for simplicity, a single trap state with energy E_A above the conduction band the effective mobility can be described by

$$\mu_{Eff} = \mu_0 \alpha \cdot \exp\left(-\frac{E_A}{k_B T}\right) \tag{2-5}$$

where μ_0 is the intrinsic free carrier mobility near the bottom of the extended states and $\alpha = N_C/N_T$, where N_C denotes the density of states at the bottom of the band and N_T the trap density [13,85]. However, even in the case of non-single level trap states, e.g., in the case of a linear or uniform distribution of states, it has been shown that equation (2-5) still holds. The activation energy E_A then corresponds to the difference between the lowest lying trap states and the extended band edge. The value

of α depends of course on the distribution of the trap states, but can be approximated by $\alpha = E_A/k_BT$ [85].

In addition, in a polycrystalline film the charge transfer between the individual grains also plays an important role (**Figure 2.5 (b)**). Measured activation barriers should be then explained as the barrier necessary for thermionic emission or tunneling of charge carriers between the individual organic semiconductor grains [83]. Under those circumstances the mobility will strongly depend on the grain density of the film. Furthermore, the metal electrode may form a Schottky contact with the organic semiconductor, such that the thermally activated charge injection may dominate the temperature dependence of the drain current and the related contact resistance R_C (**Figure 2.5 (a)**) [39,86–88]. As pointed out in chapter 2.1 and displayed in **Figure 2.2**, due to the potentially different semiconductor growth modes on the dielectric compared to the contact regions, a low conductivity region may form in this transition region [89,90].

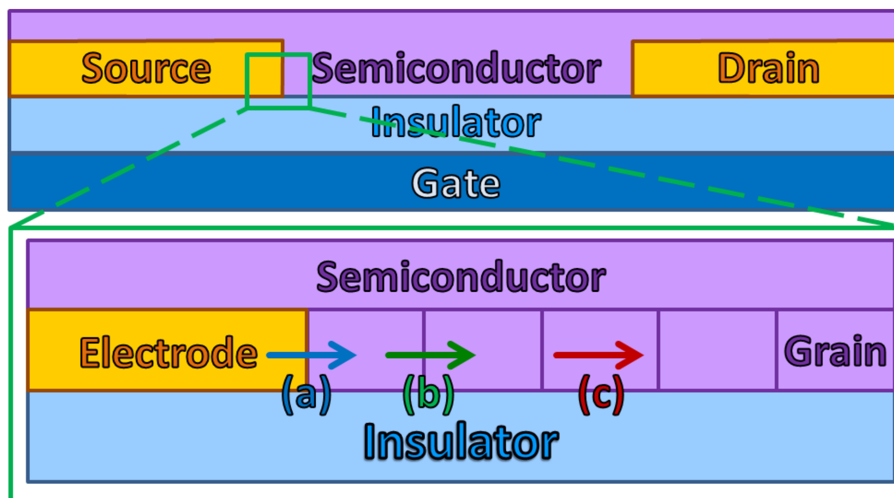


Figure 2.5: Charge transport contributions in an organic thin film transistor: (a) The charge carrier injection into the semiconductor, (b) the transition between grain boundaries and (c) the charge transport within a grain.

In order to gain information on the prevailing charge carrier mechanism and its temperature dependence, the natural logarithm of the mobility ($\ln\mu$) can be plotted against the inverse temperature $1/T$. According to equation (2-5), from the slope of this Arrhenius type representation, the involved activation barriers for the thermally activated carrier transport can be deduced.

Additional information can be extracted from the temperature dependence of the threshold voltage. The general increase of the threshold voltage (higher negative values for p-type channels) with decreasing temperature can be explained by the mobility edge model [91]. In this model, two types of carriers are classified: mobile carriers in the band-like state and immobile carriers in the trap states. The trap states extend more or less (deep and shallow traps) into the gap in an exponential like form. For hole conductivity, the density of occupied states $D(E)$ is given by

$$N = \int D(E) f(E, E_F)\, dE \qquad (2\text{-}6)$$

where $f(E,E_F)$ is the Fermi-Dirac distribution for holes. By increasing the (negative) gate voltage, the Fermi level moves towards the hole conduction band and the deep traps become more and more filled until at a certain gate voltage (the onset voltage) states in the delocalized band and shallow trap states become filled as well and charge starts to flow in the channel. At lower temperature, the tail of the Fermi-Dirac distribution is less pronounced, thus a higher (negative) gate voltage is needed to fill the traps. This effect was observed in all temperature-dependent threshold voltage investigations and subsequently influences the applied effective gate potential U_{Eff}.

2.2.2 Threshold Voltage Evaluation

In **Figure 2.6** the aforementioned threshold voltage (U_{Th}) extraction from the $\sqrt{I_{DS}}$ vs U_{GS} plot is shown. In this representation, U_{Th} is then given by the intercept of this slope of the linear part with the abscissa. The threshold voltage itself, as observed for disordered organic field-effect transistors, is seen as a mere fit parameter by some authors, lacking a clear physical basis [75]. As a characterization parameter these authors suggest the onset voltage (U_{On}) to be used. According to their calculations, the onset voltage should be close to zero and in particular independent of the temperature. This is apparently not the case in our work, where the extracted onset voltages often deviate from zero and show a shift with temperature comparable to the threshold voltage.

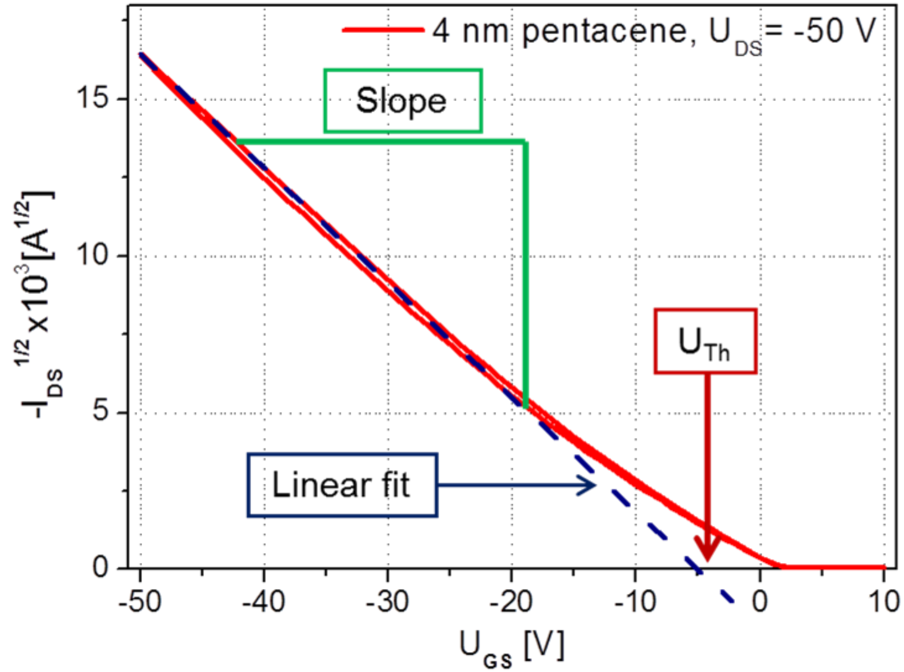


Figure 2.6: Threshold voltage extraction from a drain current square root ($\sqrt{I_{DS}}$) vs. gate bias (U_{GS}) plot.

2.2.3 Charge Carrier Mobility Evaluation

One of the most commonly investigated parameters and therefore often the choice for comparing results between different materials and research groups is the charge carrier mobility μ. In a classical picture it is simply defined as the relation between the applied electric field ($\vec{E}$) and the resulting average charge carrier drift velocity ($\overrightarrow{v_d}$):

$$\mu = \frac{|\overrightarrow{v_d}|}{|\vec{E}|} \tag{2-7}$$

For the analysis of the obtained OTFT transfer and output curves, we used the formalism for standard MOSFET devices [68,69]. Under the assumption that the mobility is constant along the channel and that the contact resistance at the metal-semiconductor interface is low in comparison to the channel resistance, the saturation mobility (μ_{Sat}) as a function of coverage can be extracted from the well-known formula:

$$I_{DS} = C_G \mu_{Sat} \frac{W}{2L} [U_{GS} - U_{Th}]^2 \tag{2-8}$$

and consequently:

$$\mu_{Sat} = \frac{2L}{C_G W} \frac{I_{DS}}{[U_{GS} - U_{Th}]^2} \tag{2-9}$$

$$\text{for } |U_{DS}| > |U_{GS} - U_{Th}| > 0$$

Therefore, μ_{Sat} could be derived from the linearly fitted slope in a $\sqrt{I_{DS}}$ vs U_{GS} plot (**Figure 2.6**). While the threshold voltage in some experiments shifted to quite negative values (down to -45 V and more), the effective gate voltage U_{Eff} used in the regime characterization remained at relatively low values compared to the applied U_{DS}. This ensured the validity of the condition for the saturation regime, as stated above.

In similar fashion, the linear mobility μ_{Lin} was derived from the $\sqrt{I_{DS}}$ vs U_{GS} plot representation for U_{DS} = -3 V in all cases, ensuring the compliance with the condition for the linear regime:

$$I_{DS} = C_G \mu_{Lin} \frac{W}{L} \left[(U_{GS} - U_{Th}) U_{DS} - \frac{U_{DS}^2}{2} \right] \tag{2-10}$$

and consequently:

$$\mu_{Lin} = \frac{L}{C_G W} \frac{I_{DS}}{\left[(U_{GS} - U_{Th}) U_{DS} - \frac{U_{DS}^2}{2} \right]} \tag{2-11}$$

$$\text{for } |U_{GS} - U_{Th}| > |U_{DS}|$$

2.3 Formation of the Semiconducting Layer

A crucial aspect in the manufacturing of OTFT devices is the deposition and formation of the semiconducting layer itself. As pointed out in chapter 2.2.1, the charge transport in organic materials relies heavily on an activated transition of charge carriers from the electrodes into the semiconductor, from molecule to molecule, and in between the grains of the polycrystalline material. It is evident, that in this case the layer quality in terms if crystallinity, preferential grain orientation and defect density are of major influence on the resulting charge transport properties. For the particular case covered in this work, the aforementioned π-π stacking between molecules is of critical relevance for the charge transport in the layer. Therefore, the maximization of this overlap through the selection of optimal deposition and growth conditions will be a focus throughout all the experimental sections. The study of the growth of rod-like organic molecules has been a major topic in a number of comprehensive publications [92–96].

In the following chapters, largely based on the works by Oura *et al.* [97], the fundamental principles of molecular deposition from the gas phase, adsorption and subsequent nucleation in the form of islands will be covered. Additionally, the formation of thicker layers and the thermal desorption of molecules will be discussed.

2.3.1 Adsorption and Surface Diffusion

When a solid substrate surface is exposed to a particle flux from the gas phase, the impinging molecules can adsorb on the surface when an attractive force between the adsorbate and the surface is present and the adsorption process is energetically favorable. This circumstance is intuitively described by the Lennard-Jones potential (V_{LJ}) model for the approach of a particle to another, as displayed in **Figure 2.7** and described by

$$V_{LJ} = 4\mathrm{E}_a \left[\left(\frac{\delta}{r}\right)^{12} - \left(\frac{\delta}{r}\right)^{6} \right] \tag{2-12}$$

with the depth of the potential well E_a, the distance for zero inter-particle potential δ and the distance between the particles r. The attractive force can be of physical and/or chemical nature and ranges in binding energy from meV to several eV, depending on the involved material systems and types of binding. This substrate-surface interaction is most prominent for the first monolayer of coverage, which is often labeled wetting layer, and subsequently weaker in the following layers, since the surface potential is then partially blocked by the already deposited material.

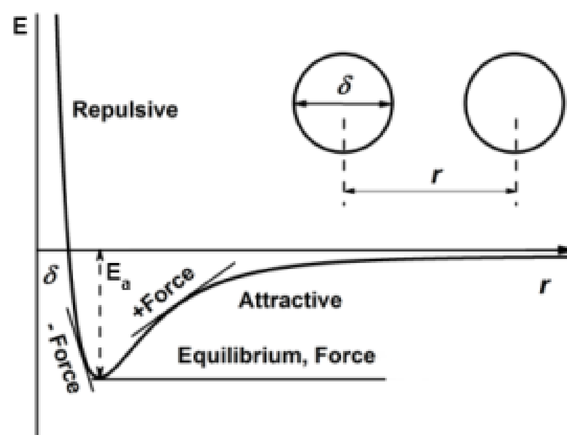


Figure 2.7: Lennard-Jones potential between two particles, displaying the attractive and repulsive forces as a function of distance *r* (adapted from [98]).

In a general case, an impinging particle has to be in range of an attractive surface potential. The concept of a sticking coefficient s is introduced and defined by,

$$s = \frac{\text{number of adsorbing molecules}}{\text{number of impinging molecules}} \tag{2-13}$$

for a given, available surface site. A number of parameters, such as the surface roughness, temperature, and existing coverage heavily influence the sticking, as does the impingement angle, kinetic energy and orientation relative to the surface of an incoming particle.

Once a particle adsorbs, a number of surface diffusion related processes is possible, as displayed in **Figure 2.8**. In terms of the diffusion coefficient D the consideration of a random walk motion [97] yields

$$D = \frac{\nu_D a^2}{z} \cdot \exp\left(-\frac{E_{Diff}}{k_B T}\right) \cdot \exp\left(-\frac{S_D}{k_B}\right) \tag{2-14}$$

with the attempt frequency for diffusion ν_D, the lattice constant a, the number of next-nearest neighbor sites z, the activation energy for diffusion E_{Diff} and the diffusion entropy S_D. As developed for the activated charge transport in the previous sections, the surface diffusion is once more highly dependent on the surface temperature. The diffusion energy E_{Diff} is related to present potential barrier heights for specific diffusion steps and varies greatly with the surroundings of the diffusing particle, such as the number of nearest neighbors on, for example, step-edges versus a single particle on a large terrace. The actual rate of diffusion for a particle is then determined by the relation of this barrier height E_{Diff} to the thermal energy $k_B T$.

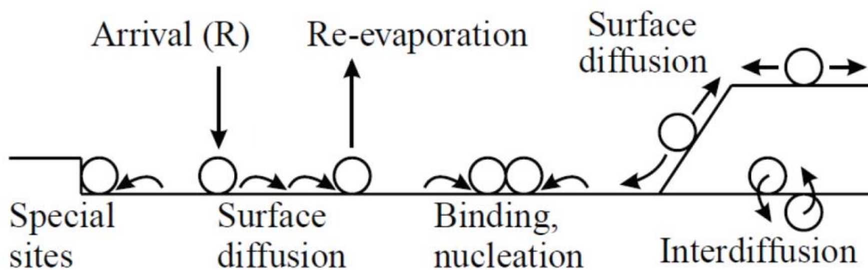


Figure 2.8: Overview of possible processes and corresponding activation energies for an adsorbing particle [99].

2.3.2 Island Nucleation and Film Growth Modes

As outlined in **Figure 2.8**, adsorbates diffusing on a surface can either re-evaporate into the gas phase, or if the adequate conditions are met, bind to a special site or other diffusing particles. The interaction with the nearest neighbors at sites such as kinks and steps, or the nucleation into islands with other adsorbates, significantly reduces the mobility of the diffusing species, inhibiting further diffusion processes. On an initially clean surface, island nucleation is the first step of adsorbate layer formation. In order to form these islands, for each material system a specific number of particles have to meet to ensure sufficient binding strength between them. This leads to the definition of the critical island size i, which denotes the number of particles found in the largest, non-stable cluster. Therefore, the addition of a single adsorbate particle during the lifetime of a cluster of size i leads to the formation of a stable island. The parameter i is once more strongly dependent on the material system and especially the surface temperature during the material deposition [99–102].

With increasing surface coverage (Θ) more and more islands nucleate, leading to an increased island density. The involved mechanisms can either be described by the classical nucleation theory, of diffusion-limited aggregation [103,104] or attachment-limited aggregation [95,105]. The initial nucleation often significantly influences the growth and properties of the film up to a thickness of several layers [93,96,106]. This is attributable to the fact that the number and form of islands, be it large, flat two-dimensional or structured, high three-dimensional, determine the coarseness and growth pattern for the subsequent layer formation. Once a nominal coverage of about 0.2 monolayers (ML) is reached the system is referred to be in the aggregation regime, where number of islands stays nearly constant, and the islands subsequently grow with increasing adsorbate coverage.

In general, changes in the island density are referred to as coarsening, which can be attained in different ways [97]. The coalescence of islands through merging of mobile ones is called dynamic or Smoluchowski ripening and is most prominent at low coverages around 0.1 ML, while the joining of islands as a result of increasing island size is termed as static coalescence and appears at 0.4 - 0.5 ML of coverage. The most significant related property for the formation of a charge conducting layer is the so-called percolation threshold, which denotes the coverage necessary to form larger, interconnected structures, as necessary for charge transport between the drain and source electrodes. A third form of coarsening is Ostwald ripening, which describes the

thermodynamically driven growth of larger islands on the expense of smaller ones as a result of different vapor pressures related to the free energy at island edges.

At a coverage of a full monolayer the classification of the system transitions from the wetting layer to the thin-film phase. All systems strife towards total free energy minimization, which manifests in an interaction between the different surface tensions for the substrate, the interface, and the adsorbate [107]. Under the condition that the system is in thermodynamic equilibrium the predominant, ensuing growth behavior with increasing coverage usually falls into one of the three categories displayed in **Figure 2.9**. These range from pure island growth (Volmer-Weber) to pure layer-by-layer (Frank van der Merwe) growth and a mixture of both systems (Stransky-Krastanov), where the wetting layer fully closes before the system transitions into an island type growth mode. The final, prevailing morphology for a certain material system is subsequently determined by the relative bond strength between the substrate and the adsorbate in relation to the bond strength between adsorbate particles and therefore by an interplay of the thermodynamic and possible kinetic processes [97,108].

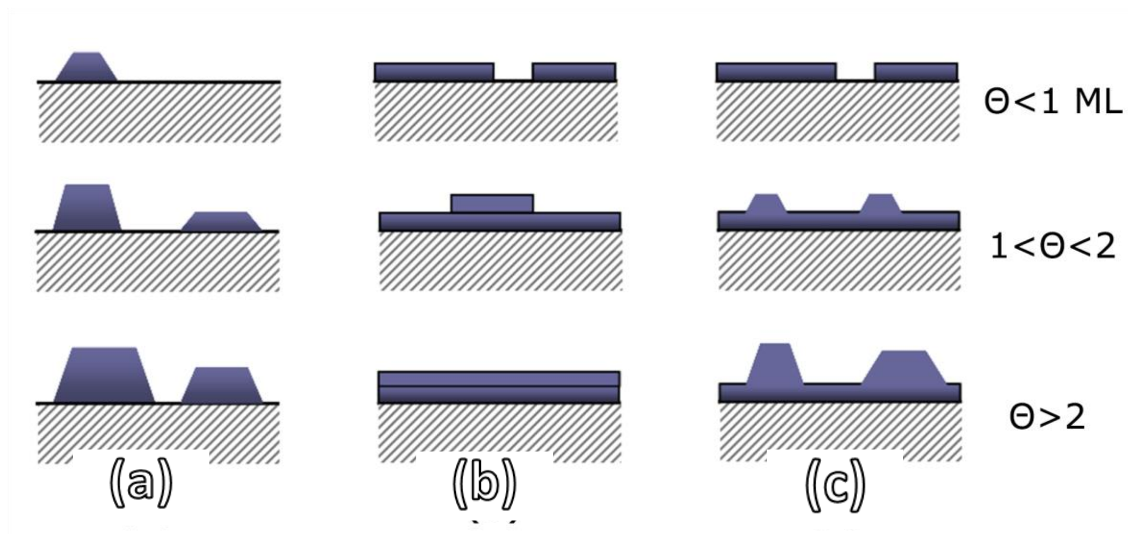


Figure 2.9: The basic thin-film growth modes (a) Volmer-Weber, (b) Frank van der Merwe and (c) Stransky-Krastanov [99].

For the layer growth of organic molecules in the low coverage regime on the dielectrics covered in this thesis, the growth of comparably large and relatively flat islands was observed for all material systems. Since the closing of layers is directly related to the evolution of charge transport with increasing semiconductor coverage, the so-called Ehrlich-Schwoebel-barrier (ΔE_{ES}) for interlayer diffusion is of particular interest [109,110]. This barrier, as displayed in **Figure 2.10**, denotes the difference in

energy necessary for an adsorbate particle to overcome a step edge of an island structure in comparison to a normal diffusion step. The change in energy stems from the variation in the number of next nearest neighbors for a diffusing particle at the encounter of a step edge. The barrier therefore signifies the amount of energy it takes for a particle adsorbing on top of an island to hop down, as well as for a lower sitting particle to hop up onto an existing island [111]. The predominant thin-film morphology is heavily influenced by this barrier since the additional kinetic hindering in the layer formation prohibits the layer from reaching the absolute thermodynamic equilibrium configurations shown in **Figure 2.9**. A large Ehrlich-Schwoebel-barrier leads to the formation of high number of strongly cascaded islands, as particles adsorbing on top of existing islands have difficulties reaching lower layers, while a very low barrier entails the formation of large, flat islands as displayed [92,106].

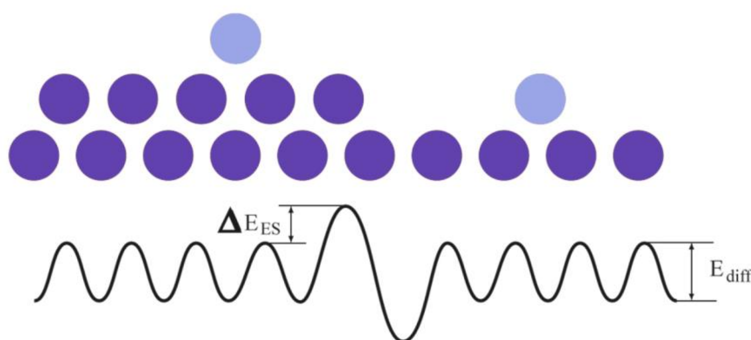


Figure 2.10: Ehrlich-Schwoebel barrier for a down-hopping layer transition [97].

Another important aspect when it comes to island and subsequent layer growth is the orientation of the molecules within the islands and grains relative to the substrate and transistor electrodes. As pointed out before, the organic molecules analyzed in this thesis feature a rectangular, sheet-like structure based on a number of joined, flat benzene rings (**Figure 1.2**). These rings have to be geometrically aligned between neighboring molecules in order to achieve the overlap of π-orbitals and subsequently reasonable charge transport. Additionally, for the investigated OTFT systems this π-π stacking alignment has to be oriented perpendicular to the dielectric surface, so that the formation of a current path between the source and drain electrodes becomes possible (**Figure 2.1**). It is reasonable to assume that all diffusing single particles and smaller clusters at the critical island size and below consist of flat-lying molecules, which also diffuse in this configuration along the surface. The desired upright standing configuration on the dielectric is therefore linked to a reorientation during the nucleation phase at a sufficiently high coverage [112]. This is intuitively dependent on the present

substrate – adsorbate interaction during the nucleation process and entails specific criteria for the selection of a suitable gate dielectric: the interaction between the substrate and the diffusing molecules has to be strong enough to ensure adsorption and subsequently sufficient sticking of islands and layers to the substrate, while it also has to be weak in comparison to the adsorbate – adsorbate interaction to allow the formation of islands and layers composed of upright standing molecules. This situation is achieved for all investigated dielectric – organic semiconductor systems employed in this work and will be further discussed in the sections on the deliberate modification of this balance through surface modification.

3 ANALYTICAL METHODS

This chapter covers the basic analytical principles employed throughout this thesis. A closer look into the foundations of thermal desorption spectroscopy, Auger electron spectroscopy and atomic-force microscopy will be supplied.

3.1 Thermal Desorption Spectroscopy

Next to the electrical characterization of OTFTs, temperature-programmed or thermal desorption spectroscopy (TDS) was the main analytical method used in the scope of this thesis. While the basic principle of TDS is rather simple [113–115], namely the controlled desorption of the adsorbate as a function of temperature, it presents a powerful tool for the analysis of the adsorbate layer and ad/desorption process itself. Important parameters such as the thermal stability of the film, as well as involved desorption energies and kinetics can be extracted from a well calibrated system. Desorption spectra for a variation of coverages, heating rates and substrate temperatures during deposition allow, under specific conditions, the distinction between the present molecular orientations in the film and the analysis of dewetting, and surface decomposition processes. Additionally, data evaluation enables the calculation of sticking coefficients as a function of coverage.

The principle of TDS relies on the increase in intensity of thermal vibrations of adsorbed molecules with increasing surface temperature. At a certain level these vibrations are strong enough to overcome the attractive potential well the particle is trapped in and a thermal desorption process is initiated. The required energy in order to desorb a particle is directly related to the attractive potentials involved in the preceding

binding process, which can therefore be described by rate equations. For the desorption of multilayers of non- or very weakly interacting particles, as it is the case for the desorption experiments in this thesis, these rate equations are referred to as the Polanyi-Wigner equations for zero order or multilayer desorption, which assume a constant, full surface coverage of the adsorbate throughout the whole desorption process [97,113]:

$$R(T) = \nu_0 N_{ML} \cdot \exp\left(-\frac{E_{Des}}{k_B T}\right) \tag{3-1}$$

with the desorption rate R, the attempt frequency for zero order desorption ν_0, the molecular surface density of one full monolayer N_{ML} and the desorption energy E_{Des}. E_{Des} is equal to the heat of evaporation for the adsorbate and, in the case of a non-activated adsorption, also equal to the adsorption energy. The pre-exponential factor ν_0 is usually in the order of 10^{13} s^{-1} for small non-interacting atoms [115]. It stems from transition-state-theory [116–118], which denotes the ratio of the number of translational, rotational and vibrational degrees of freedom a particle experiences in the adsorbed and desorbed state. As a result of the geometric hindering by the surface and internal degrees of freedom present in multi-atom systems, it is apparent that the comparably large organic molecules investigated in this thesis experience a significant shift in the number of thermally excitable degrees of freedom upon entering the gas phase. This is especially true in comparison to small, mono-atomic particles [118] and leads to much higher values for ν_0 for large organic molecules [119], as will be highlighted in the result sections.

Experimentally, TDS is most often realized by the in-line desorption of an adsorbate into a mass spectrometer under UHV conditions as a function of linearly increasing sample temperature. The high pumping speed in the UHV chamber ensures that a clear relationship between the registered partial pressure and the molecular flux of the desorbing molecule can be established. Large organic molecules tend to stick on contact with most surfaces in the vacuum chamber, making in-line detection necessary for meaningful data extraction. The higher prevalence of mass spectrometers as the detector of choice in comparison to simple pressure gauges, stems from the fact that, in contrast to the simple non-mass specific detection in pressure gauges, through in-line detection the monitoring of specific masses in the desorption flux becomes possible. In addition, large molecules and tend to fragment upon ionization in both detector types. Therefore a mass spectrometer can specifically detect the signals of fragmentation masses and yield information on the desorption process and possible decomposition

during the desorption from the sample surface for molecules, which is again not possible to deduce from a rise in overall pressure. A well-known cracking pattern of the involved materials is then necessary in order to attain reliable and exact results. Additionally, the angular distribution of the desorption flux, which is a cosine distribution in the ideal case, and the kinetic energy distribution of the desorbing species have to be kept in mind, especially its influence on the detection accuracy.

As expected from equation (2-14), the desorption rate R is exponentially dependent on the sample temperature and increases up to a maximum at T_M, where the rate then rapidly drops to zero as result of the diminishing surface coverage. In **Figure 3.1** representative spectra for the zero order desorption of epindolidione layers from a sputtered SiO_2 sample are shown. In this graph the received data is represented without the temperature and background corrections necessary for meaningful parameter extraction, which will be discussed at a later point. The peak shapes and maximum desorption temperatures T_M yield information on the involved desorption energies for the investigated systems.

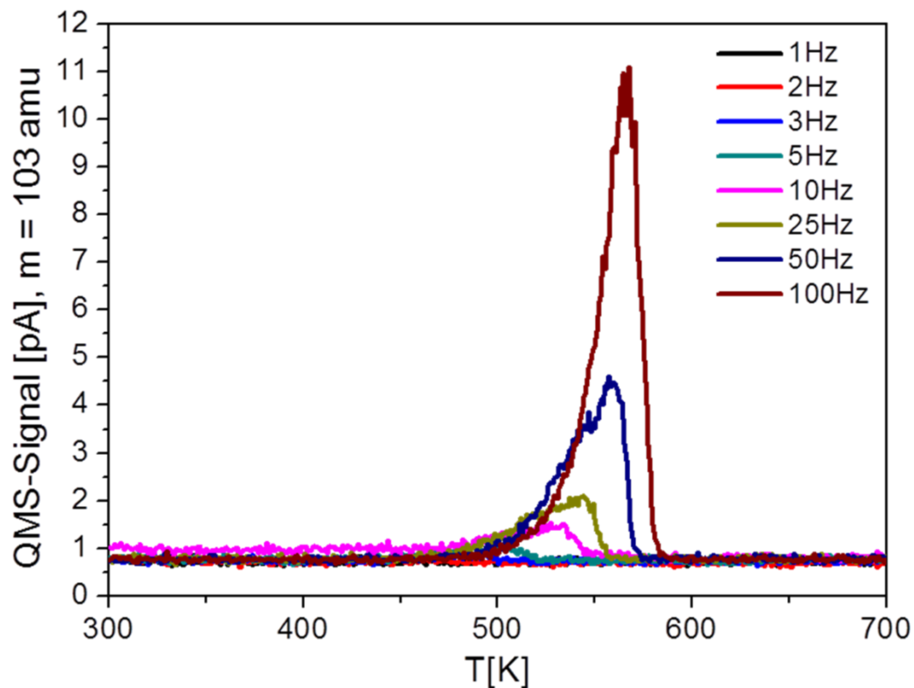


Figure 3.1: Exemplary thermal desorption spectra from a sputtered SiO_2 surface for different epindolidione film thicknesses deposited at 300 K substrate temperature. Heating rate $\beta = 1$ K/s. No temperature or background corrections have been applied.

Generally, the shape, number and relative position of peaks in a TDS spectrum allows the distinction between wetting and multilayer desorption, and even the

differentiation between molecular orientations in the layer, if the desorption energies are significantly different for, e.g., islands of upright-standing and flat-lying molecules. For the present zero order desorption the rate only depends on the temperature, according to equation (2-14). This allows the extraction of the desorption energy E_{Des} and attempt frequency for desorption ν_0 from Arrhenius type $\ln(R(T))$ vs. $1/T$ plots, where E_{Des} is proportional to the slope and ν_0 can be determined by the intercept of the graph with the y-axis following a careful calibration of the desorption rate to the corresponding quadrupole mass spectrometer signal.

3.2 Auger Electron Spectroscopy

Representing a highly surface sensitive spectroscopic method, Auger electron spectroscopy (AES) was used throughout this thesis to characterize chemical substrate surface compositions. AES relies on a three electron process, initiated by an electron or X-ray photon in an energy range of approximately 2 - 10 keV, which ejects a primary core electron and therefore ionizes an atom. Subsequently, the atom relaxes through the filling of the core hole with a secondary electron from a higher orbital. The energy difference between these two electron states is then released in the form of an X-ray photon, or in the form of the eponymous, tertiary Auger electron (**Figure 3.2**). The expelled Auger electrons kinetic energy is then directly given by the inner atomic energy level spacing minus the binding energy and the work function for the material and acts as a fingerprint for the elemental species. Chemical shifts can influence this energy spacing, which is compiled in an Auger atlas for elemental characterization.

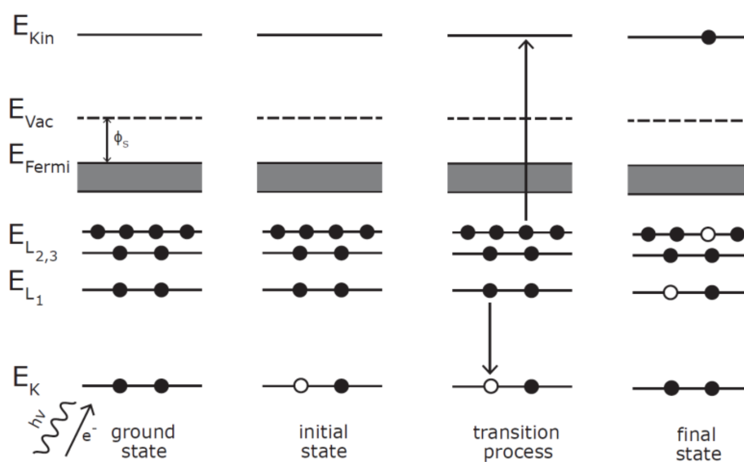


Figure 3.2: Representation of the three-electron Auger process and the involved energy levels (adapted from [97]).

The extreme surface sensitivity of AES stems from the fact that the emitted electrons in the range of 50 eV to 3 keV have a very short mean free path in the solid material resulting in a high energy loss with travel distance in the solid sample. Therefore, only electrons generated in the first few nm from the surface contribute to the registered Auger electron signal. The low Auger electron energy also makes the operation under UHV conditions necessary in order to minimize residual gas collisions and detrimental surface contamination during spectroscopy [97,120].

Quantitative Auger analysis is usually limited to the relative comparison of registered peaks in a single spectrum, since a large number of variables are involved in the actual Auger process and have to be known in detail in order to ensure meaningful data interpretation. The emission probability for the Auger electron or the competing X-Ray photon is determined by the atomic species. Auger emission is favored for lighter elements, except for hydrogen and helium, which do not possess the three electrons necessary for Auger emission. The relatively small Auger signals are superimposed on a large background of secondary and backscattered electrons and are therefore usually registered in derivative mode, by modulating the energy analyzer voltage and detected by a lock-in amplifier. For non-conducting samples the additional possibility of electrical charging effects has to be taken into account.

In this work the main point of interest for AES was the chemical composition of the gold electrode and dielectric surface, as the surface composition in these areas directly affected the subsequent organic layer formation on these substrates. Next to the distance of the energy analyzer from the sample surface, the actual spot size of the incident electron beam directly affects the quality and precision of the resulting signal. In our case a spot size of about 0.5 mm was attained with the experimental system, making, for example, detailed AES in the micrometer channel between the transistor electrodes not feasible. For these measurements the mask limiting the semiconductor deposition to the channel area had to be removed, in order to analyze the dielectric sample surface outside of the gold contacts, under the assumption that this area is equivalent to the channel area. In **Figure 3.3** an exemplary Auger spectrum for the SiO_2 sample surface employed throughout this work is depicted. AES enables the distinction of the present silicon and oxygen peaks in the dielectric, as well as the analysis of any present carbon surface contamination. The freshly installed sample features atmospheric carbon contamination (black graph in **Figure 3.3**) as well as the expected SiO_2 peaks. The deposition of the organic layer, in this case 5 nm of the hydrocarbon pentacene,

completely blocks the Auger electrons generated in the dielectric from reaching the energy analyzer, leading to a pure carbon signal from the organic material (red graph in **Figure 3.3**). Thermal desorption of this layer and subsequent sputter cleaning yields a carbon free surface with very distinct silicon and oxygen peaks (blue graph in **Figure 3.3**).

The AES system used in this work was manufactured by Staib Instruments. With an electron source voltage of 2 kV and a filament current of 1.4 A the emission current was then tuned to 1 μA and the detection voltage set to 2000 V. An energy resolution of 10 eV and a dwell time of 50 ms were used throughout this work [121].

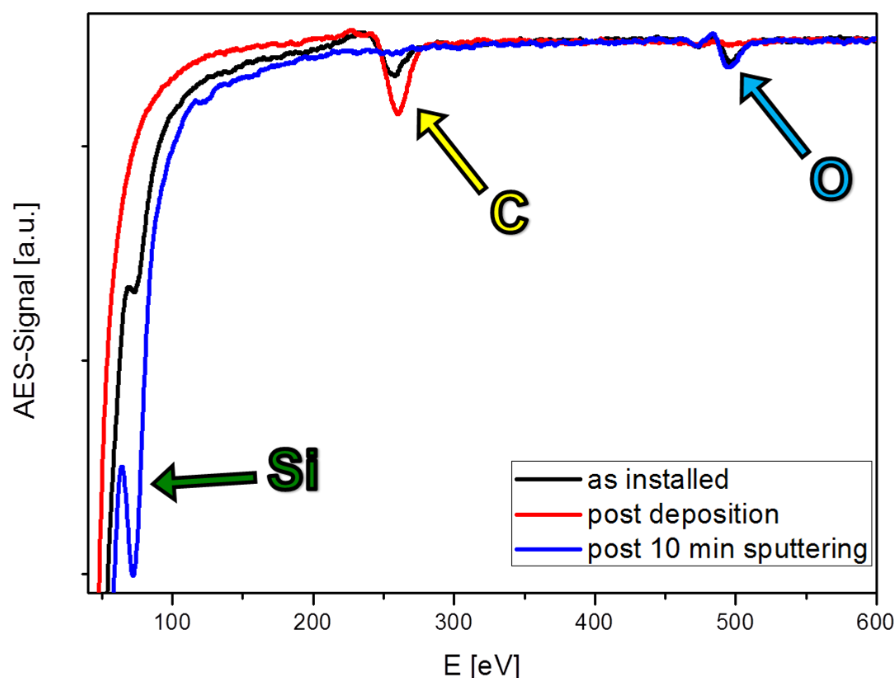


Figure 3.3: Exemplary Auger electron spectroscopy graph, featuring a freshly installed sample (black), sample covered with 5 nm of pentacene (red) and sputtered sample after thermal pentacene removal (blue).

3.3 Atomic-Force Microscopy

As one of the most common surface analytical methods today, atomic-force microscopy (AFM) allows the direct topographic scanning of surface corrugations down to the sub-nm regime, far exceeding optical diffraction limited systems and on any type of surface, independent of its conductivity. To achieve this, a sharp tip with a curvature in the nanometer range attached to a, typically silicon, cantilever is scanned over the sample surface and, at the same time, the cantilevers deflection is monitored. The deflection can stem from a number of possible surface interactions, such as mechanical

contact force, chemical bonding, van der Waals forces and even electrical or magnetic forces, depending on the probe in use. In the simplest case, an interaction in the form of the Lennard-Jones potential presented in **Figure 2.7** is obtained, with an attractive interaction down to cantilever-surface distances in the chemical range, where the electrostatic repulsion starts to take over. This leads to three main operation regimes; contact mode, where the tip is in direct connection to the surface and is pushed into the repulsive surface potential leading to high sample and cantilever wear; tapping mode, where the cantilever is oscillated close to its resonance frequency and dips from the attractive into the repulsive interaction regime and therefore directly *taps* the surface and lastly the cantilever can be operated in the non-contact mode, where the tip-surface distance is larger and once more excited at or close to the cantilevers resonance frequency. Hereby, the tip-surface distance is short enough, so that the tip enters the attractive short-range surface potential, such as van der Waals potentials, but also sufficiently high, so that the tip never enters the repulsive surface potential.

The main advantage of the most commonly employed tapping-mode is that precise surface information can be obtained under ambient conditions, while minimizing the lateral forces on the cantilever and sample degradation present for soft samples in contact mode. The cantilever position is most commonly excited via a piezo element and its displacement detected optically with a laser diode and a four-segment photo detection sensor. While the driving signals frequency and amplitude are kept constant, surface interaction leads to a change in the cantilever amplitude, which is in turn used in a feedback loop that controls the tip-surface distance. The change in height to attain the preset cantilever oscillation amplitude is then proportional to the surface corrugation [122].

In the scope of this work a Nanosurf easyScan 2 AFM system has been used, as displayed in **Figure 3.4**. While all cross sections have been obtained from line scans on the topography data, the displayed AFM scans are shown in the derived data mode, which creates a shaded representation of the surface data in order to highlight the surface structure [123]. In **Figure 3.5** a schematic representation of the AFM working principle and cantilever system are shown.

Figure 3.4: Nanosurf easyScan 2 atomic force microscope.

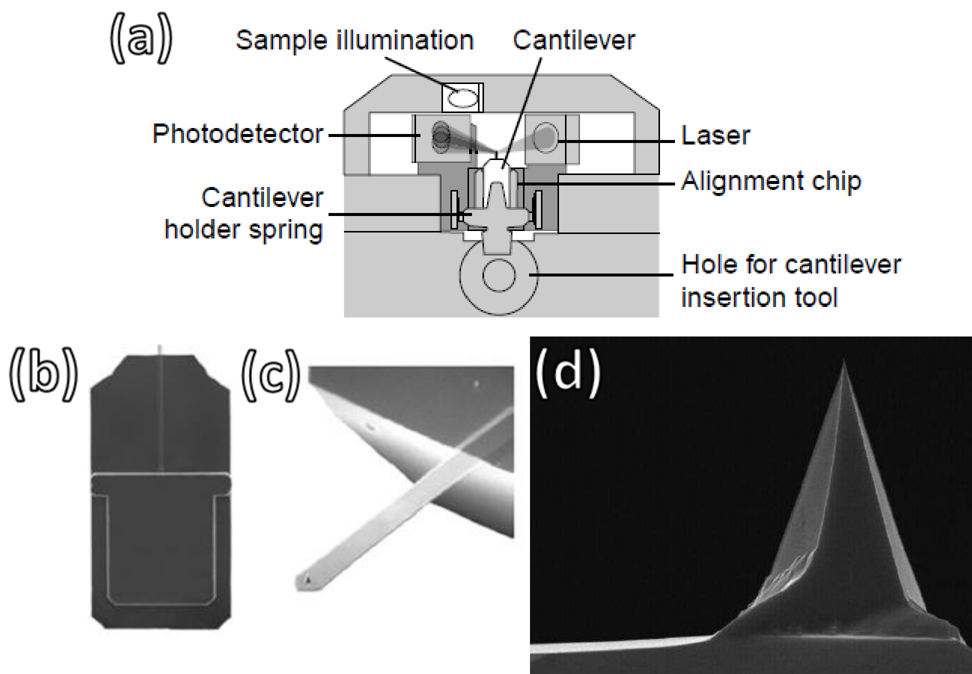


Figure 3.5: Detailed depiction of the (a) Nanosurf easyScan 2 setup and electron microscope pictures of (b) the cantilever holder, (c) the cantilever and (d) the tip [123,124].

4 INSTRUMENTATION

In this chapter, the experimental setup used throughout this thesis, as displayed in **Figure 4.1** and **Figure 4.2**, and the methods of sample preparation will be covered. This includes details on the ultra-high vacuum system, quadrupole mass spectrometer, semiconductor deposition system, and argon-ion sputtering. Finally, the sample processing from a silicon wafer piece to a fully prepared and installed sample will be detailed.

4.1 Ultra-High Vacuum System and Experimental Array

The measurements performed in the scope of this thesis necessitated a vacuum of high to ultra-high quality. This stems from the fact that for reasonable surface analysis and precise semiconducting layer formation, the surface had to remain virtually unchanged during the experimental timeframes. Consequently, the formation of a residual gas layer, for the most in the form of the main residual component water, had to be prohibited during the experimental steps. In addition, a better vacuum leads to a background reduction and therefore increased sensitivity to the desorbing species for thermal desorption spectroscopy. The ultra-high vacuum chamber in use was pumped by a rotary vane roughing pump down to about 10^{-3} mbar and subsequently further evacuated by two turbo molecular pumps and is displayed in **Figure 4.1**. The resulting pressure was monitored by a cold cathode manometer and, without bake-out of the vacuum system, a base pressure of 2×10^{-8} mbar could be reached by overnight evacuation. This level of vacuum ensured a characteristic timeframe for the formation of a residual gas layer on the sample surface in the range of hours and also allowed a

sufficiently large mean free path for the semiconductor deposition, so that the semiconducting molecules reached the sample surface without residual gas collisions.

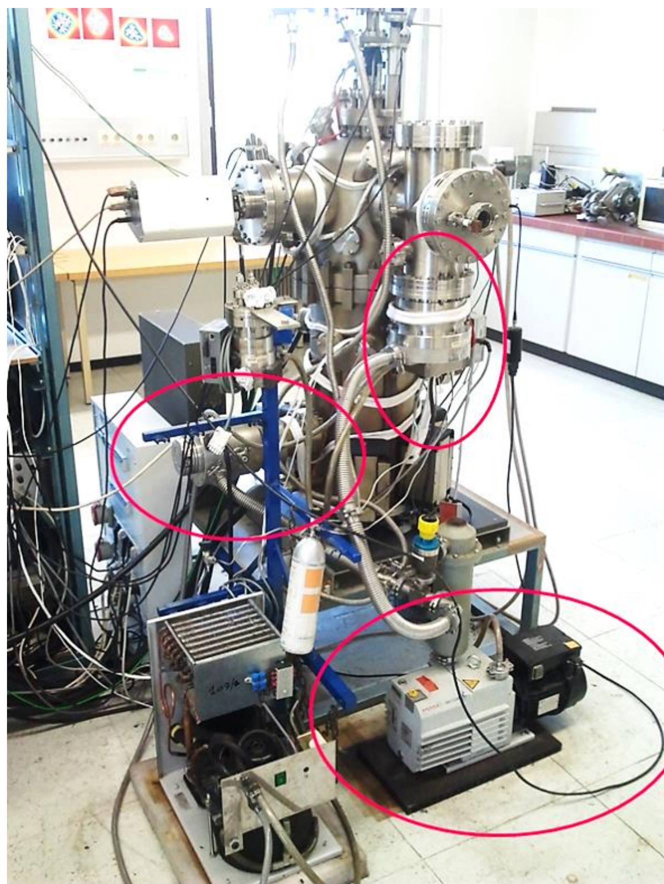


Figure 4.1: Photograph of the employed ultra-high vacuum chamber. From bottom to top the rotary vane roughing pump and the two turbo molecular pumps have been circled in red.

The analytical and preparative components employed in this thesis are displayed in **Figure 4.2** and consisted of a quadrupole mass spectrometer, Auger electron spectrometer, Knudsen cell and quartz microbalance semiconductor deposition system, and a sputter gun with an argon gas inlet.

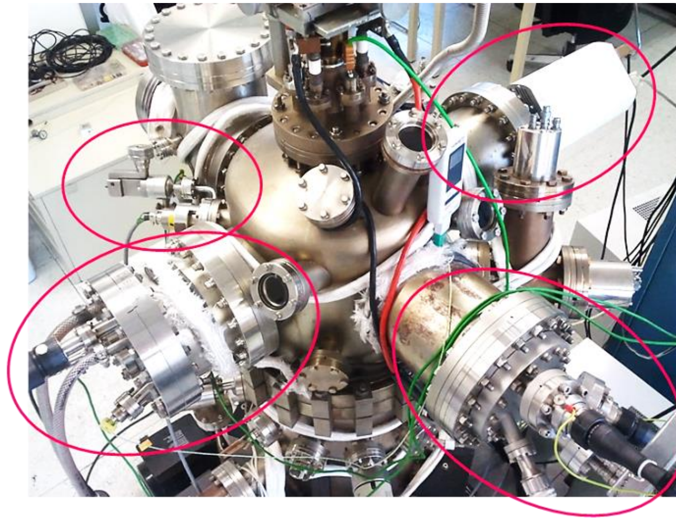


Figure 4.2: Photograph of the analytical and preparative components with the installed rotatable sample holder in the center. Clockwise from the top right the quadrupole mass spectrometer, Auger electron spectrometer, deposition system and sputter gun have been circled in red.

4.1.1 Quadrupole Mass Spectrometer

As one of the integral parts of thermal desorption spectroscopy and residual gas analysis, the experimental setup included an inline quadrupole mass spectrometer (QMS 200) by Pfeiffer with a measurement range of 0 – 200 amu and secondary electron multiplier detector type. The basic working principle of a QMS is outlined in **Figure 4.3**. It relies in the ionization of gas particles which enter the spectrometer and the subsequent acceleration towards an ion detector. Through a focusing system and a quadrupole field, generated by the interplay of direct and alternating voltages applied to four conducting rods, a precise charge to mass ratio selection for a particle traveling through the field becomes possible. Only a certain value for this ratio enables a particle to traverse the system and reach the ion detector, including a secondary ion multiplier, without deionization by coming in contact with one of the metal rods. The electric field applied to the mass filter rods, more precisely the ratio of the AC/DC voltages, can be used to scan the spectrometer through a range of masses and enables operation down to a detection limit of approximately 10^{-14} mbar partial pressure [125]. It has to be kept in mind that in accordance with the working principle a double-ionized particle then appears at half mass in a mass spectrum.

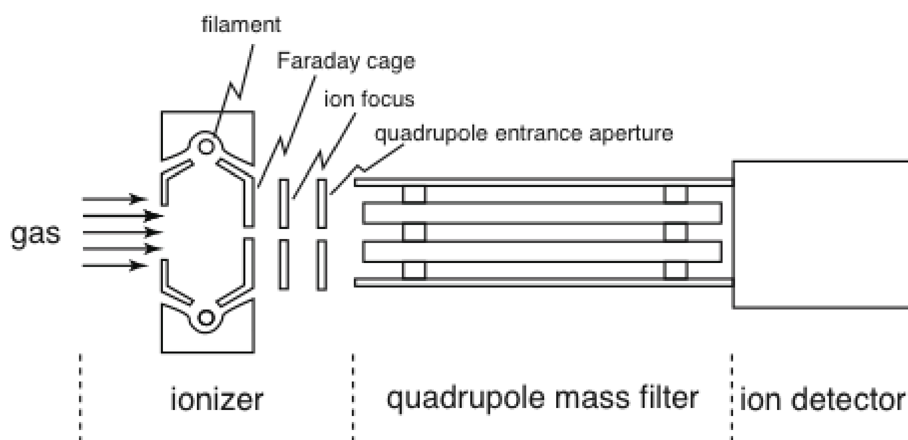


Figure 4.3: Basic structure of a quadrupole mass spectrometer (adapted from [126]).

For TDS measurements, as described in principle in chapter 3.1, the sample was positioned in front of the QMS and the mass spectrometer set to a specific mass, which was then monitored as a function of the sample temperature; in our case, we used a heating rate of 1 K/s. The emission current was set to 2 mA, with potentials of 90 V to the cathode and 65 V to the extractor. The ion detector operated under a secondary electron multiplier voltage of 1600 V. By multiplexing the QMS, other masses, if so required, could be simultaneously measured in order to, for example, monitor increased hydrogen levels from a high amount of cracking processes during film desorption.

Since the full masses of both investigated organic semiconducting materials, 278 amu for pentacene and 262 amu for epindolidione, were beyond our maximum QMS measurement range, prominent cracking masses had to be used for the desorption analysis. This cracking of the molecules as consequence of the ionization, as mentioned in chapter 3.1, is displayed in **Figure 4.4**, where an example for the selection of the most prominent cracking mass for pentacene is given. By continuously scanning the QMS in a specific mass range during a thermal desorption process and adding the scan cycle number as a third axis, a three dimensional TDS representation can be achieved. After the subtraction of the background signal, the emerging peaks can then be selected in respect to their signal to noise ratio. For the example of pentacene this led to the selection of 125 amu as the optimal cracking mass with the best signal-to-noise ratio for all TDS investigations.

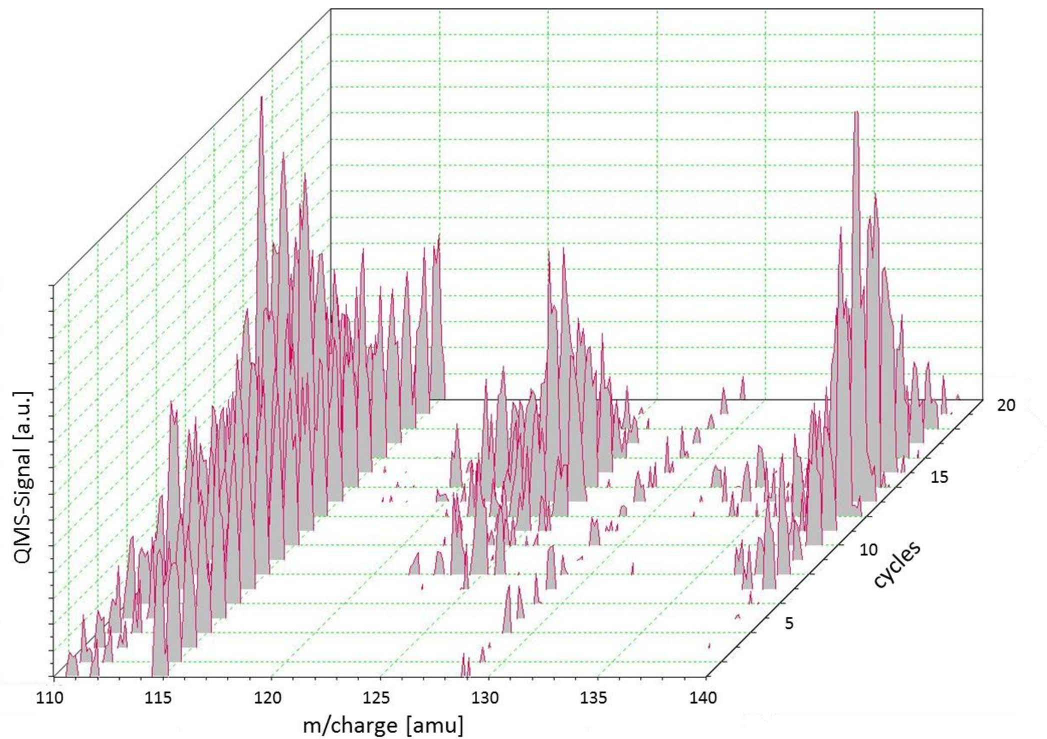


Figure 4.4: Prominent cracking masses for pentacene in the range of 110 to 140 amu during a thermal desorption measurement cycle with a heating rate β of 1 K/s and a scan rate of approximately 5 s per cycle. The background signals have been subtracted for clarity reasons.

4.1.2 Physical Vapor Deposition and Quartz Microbalance

In order to be able to manufacture and characterize organic semiconducting layers from the sub-monolayer to thin-film regime, the application of a reliable and accurate deposition monitoring system is indispensable. The semiconductor deposition system employed throughout this thesis consisted of a resistively heated stainless steel Knudsen cell, a double shutter system and a quartz microbalance (QMB).

The general working principle of a Knudsen cell is shown in **Figure 4.5** and relies on the materials evaporation through a small opening from an isothermal enclosure [127]. This Knudsen cell was then, as shown in **Figure 4.6**, placed in a larger metal tube (shielding shroud) with the aforementioned double shutter system, which featured corresponding openings for simultaneous or selective deposition onto the sample and the oscillating quartz crystal. In order to ensure Knudsen type evaporation under the characteristic cosine distribution, a number of requirements have to be fulfilled [128]: the cell orifice has to be one-tenth or less of the evaporating molecules mean free path at the equilibrium vapor pressure, and the inner cell surface has to be

much larger than the orifice area. Additionally, the walls around the orifice have to be sufficiently thin, so that adsorption and scattering contributions to the total flux from this area are negligible.

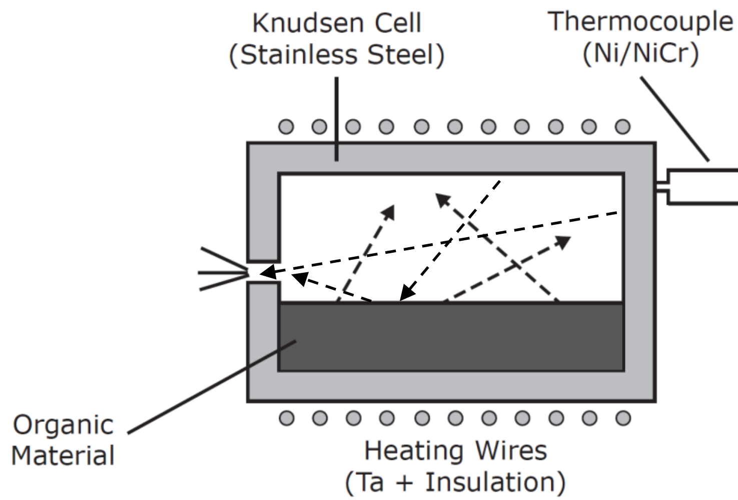


Figure 4.5: Schematic representation of the Knudsen cell working principle [129].

The stainless steel Knudsen cell was manufactured with the aforementioned geometric considerations in mind and heated resistively by insulated tantalum wires. The Knudsen cell dimensions used throughout this thesis were: 2 cm length, 1 cm diameter, 1 mm effusion opening. Under awareness of the considerable temperature lag of the system and constant observation via a spot-welded, type K thermocouple, the heating was adjusted manually until the desired deposition flux was maintained, as monitored by the quartz microbalance.

Figure 4.6: (a) Side and (b) frontal view of the semiconductor deposition system. In (a) the rotary double shutter system and in (b) the central Knudsen cell and shielding shroud for simultaneous evaporation onto the quartz microbalance (bottom) and the sample are shown.

The operating principle of the Inficon quartz microbalance is based on the detection of a frequency change of the eigenfrequency f_0 of an AT-cut quartz crystal upon material deposition [130]. The AT-cut is the most widely used industrial cut and denotes the cutting of a quartz y-bar at a theta angle of $35\frac{1}{4}°$from the z-axis. The microbalance features a very high detection accuracy and resolution, even for low density materials and deposition rates. From the Sauerbrey equation [131], the change in resonance frequency Δf of the quartz crystal can be related to the thickness change of a deposited material Δd according to:

$$\Delta d = -\frac{\Delta f}{S f_0^2 \rho} \tag{4-1}$$

with the sensitivity of the quartz S, the aforementioned eigenfrequency of the quartz oscillation f_0 and the density of the deposited material ρ. The sensitivity S encompasses a number of quartz parameters and is 2.26×10^{-6} cm^2s/g. The quartz microbalance eigenfrequency f_0 usually amounts to approximately 6 MHz and water cooling is used throughout the deposition in order to minimize temperature induced effects. The densities ρ for the organic materials used in this thesis are 1.3 g/cm^3 for pentacene and 1.5 g/cm^3 for epindolidione. In **Figure 4.7** a schematic structure **(a)** and photograph **(b)** of the deposition system are shown. **Figure 4.7** **(c)** depicts a quartz oscillator sample, which is routinely replaced after a number of extensive deposition experiments or when the deposition material species is changed.

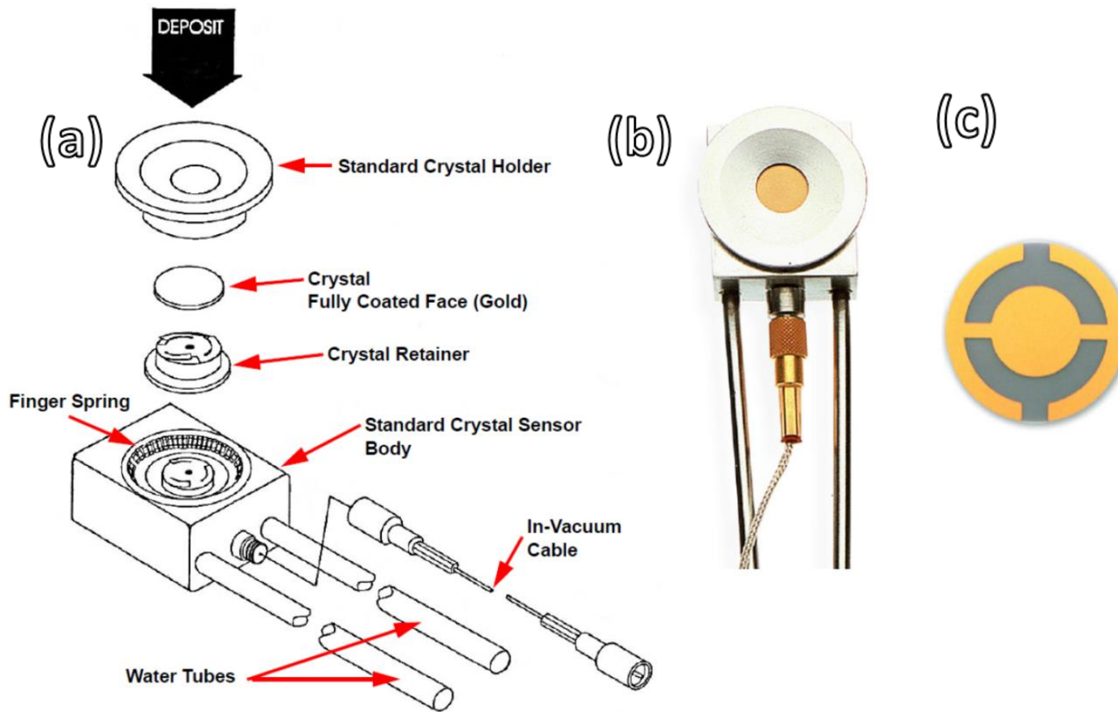


Figure 4.7: (a) Schematic structure and (b) photograph of the quartz microbalance and (c) exchangeable oscillator crystal [129,130].

The deposition system operates under the assumption that the sticking coefficient *s*, as introduced in chapter 2.3.1, is unity on the quartz surface. This is a reasonably assumption for the room temperature quartz surface and for condensable molecules such as the large organic molecules covered in this thesis [105,119]. The opening and angular deviation from the in-line deposition for the parallel deposition onto the quartz, as shown in the bottom of **Figure 4.6 (b)**, and the distances from the Knudsen cell orifice for the quartz and the sample were then chosen in such a way that under the cosine distribution of molecular flux from the Knudsen cell, both surfaces are exposed to the same amount of material flux. The adsorbed amount of material as measured by the quartz microbalance then corresponds to an impingement rate which is the same for the sample surface according to the above-mentioned geometrical considerations. In connection with TDS measurements this known impingement rate for the sample surface can then be used to extract the sticking coefficient for the sample surface, which also turned out to be unity for the applied conditions of the investigated material systems.

In combination with the double shutter system, which enables the accurate setting of a desired deposition rate before starting the parallel exposure of the sample, very precise control of the deposited layer thickness, as well as an accurate deposition rate

and exposure time control could be achieved for all coverage ranges. Typically, quite low deposition rates of about 0.1 ML/min were used for both semiconductor systems.

4.1.3 Argon-Ion Sputtering

The final tool for surface modification consisted of a Specs IQE 11/35 ion sputtering gun with direct, inline gas supply, which allowed sample surface cleaning by argon-ion sputtering prior to semiconductor deposition. An influence of the sputtering on the prevalent growth mode has been shown for example for the pentacene related molecule para-hexaphenyl [92,132]. The working principle for ion-sputtering is based in the ionization of the argon atoms entering the UHV chamber by electron impacts in the ionizer part of the system, creating a source of Ar^+ ions. These are then subsequently accelerated towards the sample in a high voltage field and impinge on the surface. The nature of the ion-surface interaction can be of electronic or nuclear nature. The latter encompasses elastic interactions and tends to dominate in the most often employed keV ion-energy regime. The collision of the primary ions with present surface particles then yields a collision cascade in which the primary ion causes a number of primary and higher-order collisions as described in detail by P. Sigmund [133]. By attaining sufficient energy through the collision cascade, some of the surface particles can then overcome the characteristic surface binding energy and leave the surface. This process enables the abrasion of the surface by the impinging ion flux and is widely used in science and industry. The sputtering of the surface is also related to the involved materials and mass ratios between the target and projectile, which can lead to additional phenomena such as preferential sputtering of one surface species or surface amorphization.

The main purpose of sputtering in this work was the removal of the most significant residual impurity in the form of carbon. Carbon is always present on the sample surface, both on the dielectric channel surface and the gold electrode surfaces, after it had been kept in air for a significant time, or after thermal desorption induced hydrocarbon dissociation. Typically, mild sputtering for 10 minutes with ion energies of 800 eV and an argon partial pressure of 8×10^{-6} mbar was used, since a sequence of AES and sputter cycles, as shown in **Figure 4.8**, was able to show that these parameters sufficed for the complete removal of carbon within the AES detection limit. This minimal sputter dose also ensured that the SiO_2 surface morphology remained virtually unchanged by the process [134], which had been highlighted as a possible problem for

subsequent layer deposition [135,136]. The influence of the carbon removal on the subsequent organic layer growth will be a major issue of discussion throughout this thesis.

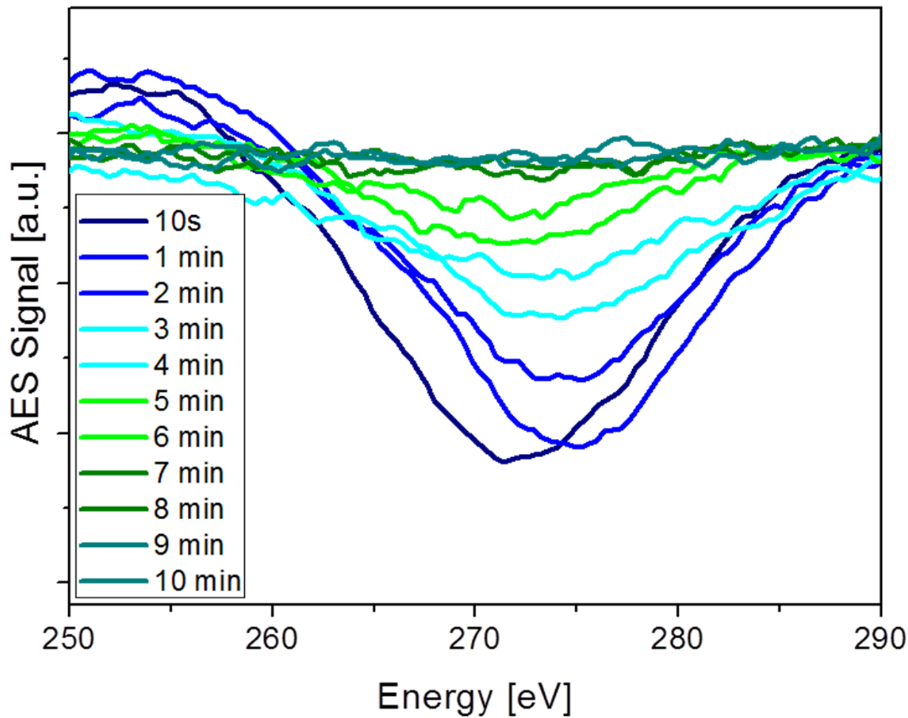


Figure 4.8: Auger electron spectroscopy carbon signal decrease as a function of exposure to the argon-ion sputter beam for the carbon residue from a 4 nm pentacene thermal desorption cycle.

4.2 Sample Preparation and Mounting

The standard samples consisted of highly p-doped silicon wafer pieces (0.6 mm×1.0 cm×1.0 cm) with a bulk resistivity of <0.01 Ω cm and a 150±10 nm thick dry-oxide layer on top, as manufactured by Siegert Wafer [137]. Following an oxygen plasma etch cleaning step, 60 nm thick gold contacts were thermally deposited through a shadow mask, forming a 25 µm wide (*W*) and 4 mm long (*L*) channel area. The contact preparation was performed at Joanneum Research Weiz by B. Striedinger. The shadow mask and resulting samples are shown in **Figure 4.9 (a)** and **(b)**, respectively. Additionally, a light microscope picture **(c)** and AFM line-scan **(d)** of the channel dimensions are shown. Contacting of the source and drain gold electrodes was established by connecting thin nickel wires (0.1 mm diameter) with conductive silver solder to the gold electrodes and by employing the sample rim of the highly conducting silicon as gate contact in the same way (**Figure 4.9 (b)**).

The back ends of the nickel wires were connected to Kapton insulated, electrically shielded cables leading to the outside of the ultra-high vacuum chamber via BNC-feedthroughs. The sample mounting itself, as shown in a schematic exploded assembly in **Figure 4.10**, was based on then attaching the 1 cm^2 silicon wafer to a stainless steel back plate, with a thin mica sheet in between for electrical insulation. In front of the sample, a thin aluminum shadow mask with a rectangular aperture (3 mm×4 mm) was positioned, which limited the area of organic material deposition, and hence reduced the leakage and off-currents. Pictures of the sample holder and different stages of the sample mounting are shown in **Figure 4.11**. This sample holder was then subsequently installed into the vacuum chamber, where it could be rotated between the experimental stations shown in **Figure 4.2** and adjusted in the mounting plane of those stations for fine tuning of, for example, the AES spot position.

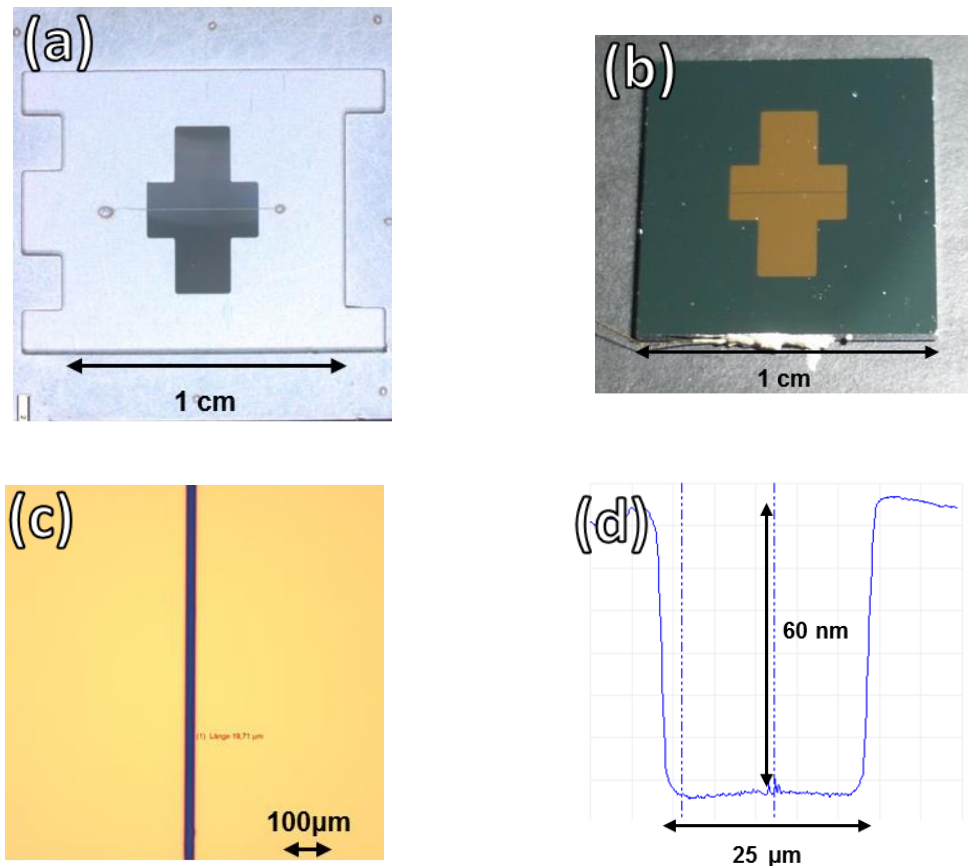


Figure 4.9: (a) Shadow mask for gold contact deposition, (b) sample with gold contacts and applied gate contact and (c) light microscopy picture, as well as (d) atomic force microscopy scan of the channel dimensions.

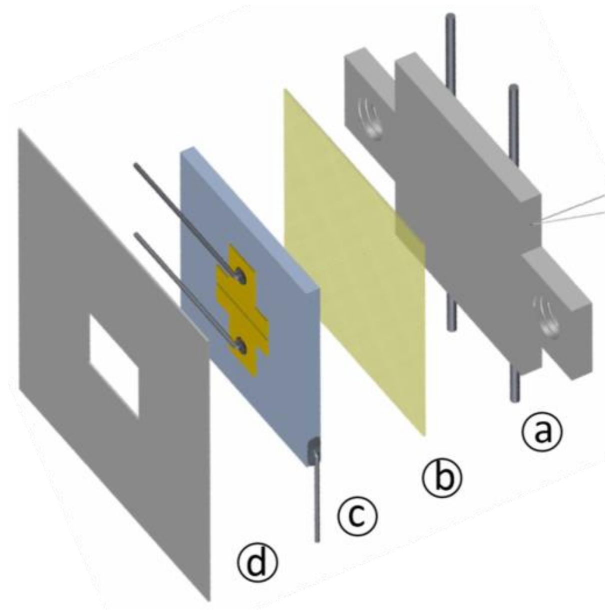


Figure 4.10: Exploded assembly of sample and sample holder: (a) stainless steel plate with Ta heating wires and Ni-NiCr thermocouple, (b) insulating mica foil, (c) Si/SiO_2 sample device with gold contact pads and Ni contacting wires, and (d) Al-shadow mask.

4.2.1 Experimental Sample Temperature Determination

One of the most important features of the experimental setup was the aforementioned capability to accurately control the sample temperature during semiconductor deposition and electrical evaluation. To achieve this, the steel plate of 1 mm thickness, which served as the sample carrier, could be heated resistively and/or cooled with liquid nitrogen through two 0.25 mm diameter, spot-welded tantalum wires. A type K thermocouple, also spot-welded to the steel plate's backside, monitored the temperature in the accessible range from about 120 K to 800 K, far exceeding the desorption temperature of both investigated semiconductors. This is necessary in order to be able to conduct TDS measurements. Ceramic washers between the sample and its mounting screws, in addition to the mica sheet, kept the sample insulated from the steel plate, which allowed precise electrical measurements in parallel to the resistive heating of the sample. The cooling was performed by filling the L-shaped stainless steel and copper sample holder setup, as shown in **Figure 4.11 (b)**, with liquid nitrogen. Through an electronic feedback loop and a LabView® program, the resistive heating could be adjusted to the liquid nitrogen counter-cooling in such a way, that the temperature could be kept at a constant level for any level of the full, abovementioned temperature range. The second functionality of the program was a linear heating ramp up to a defined

temperature, which usually featured a heating rate β of 1 K/s for all desorption or heating experiments.

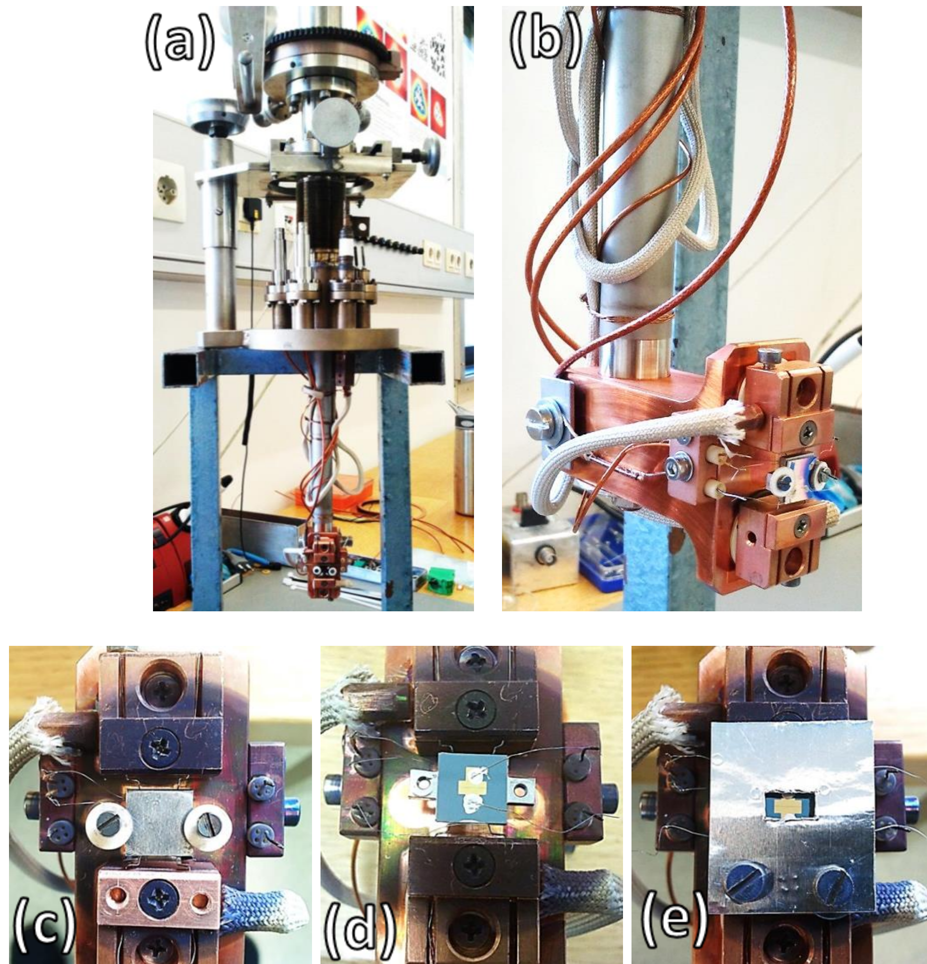


Figure 4.11: Pictures of (a) the sample holder and (b) the L-shaped mounting. (c) to (e) display the steel back plate with the thermocouple (top left), a fully wired sample and a sample ready for installation into the vacuum chamber.

Due to the special mounting setup and the thermal resistance between the heated steel plate sample holder and the silicon wafer sample, the actual temperature on the sample surface lagged behind the temperature measured by the thermocouple. Therefore a temperature correction had to be taken into account before commencing parameter extraction for E_{Des} or ν_0 out of measured TDS spectra (see chapter 3.1). This had to be done separately for pentacene and epindolidione and will here be discussed for pentacene. The procedure for epindolidione was performed accordingly.

Figure 4.12 shows, that the 8 nm thick pentacene multilayer, formed by an exposure equivalent to a 100 Hz resonance frequency change for the quartz microbalance, desorbs at 420 K from the steel mounting plate. A pentacene layer of the

same nominal layer thickness on a carbon covered SiO_2 sample surface showed a peak desorption temperature of 530 K, which in turn again corresponds to the true desorption temperature of 420 K from the steel. Thus the temperature scale can be corrected by assuming that during adsorption both the steel plate and the SiO_2 substrate share the same temperature, and that the temperature lag during the heating process follows a linear dependence. The correction formula for the temperature T_{Corr} can then be expressed as

$$T_{Corr} = T_0 + \left(\frac{T_M^{SS} - T_0}{T_M^{Si} - T_0}\right)(T - T_0) \tag{4-2}$$

with the adsorption temperature T_0 (300 K), the desorption temperature for a multilayer from the steel plate T_M^{SS} and the desorption temperature for a multilayer from the Au/SiO_2 silicon wafer surface T_M^{Si} .

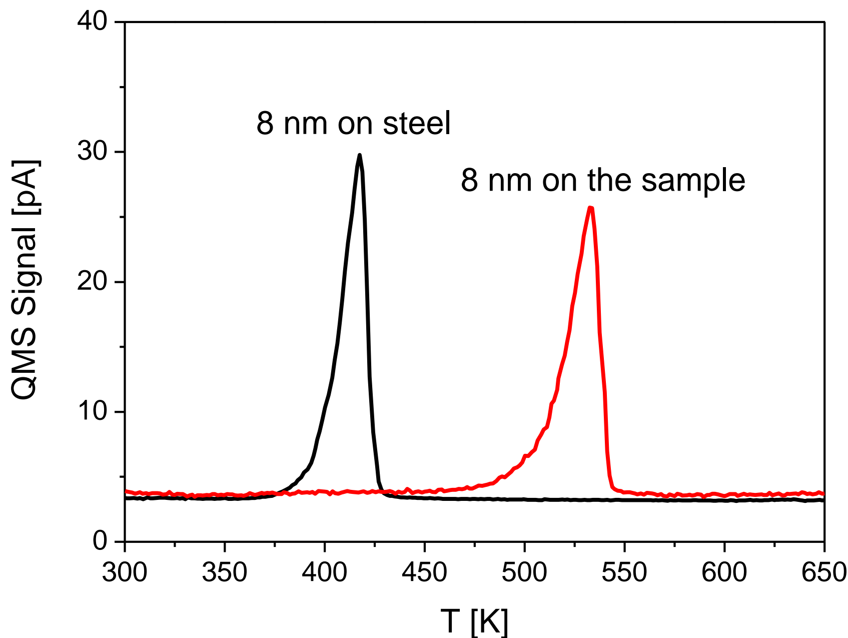


Figure 4.12: Comparison between thermal desorption spectra of 8 nm pentacene from a stainless steel sample holder and a standard SiO_2 sample surface used for temperature correction. Adsorption temperature $T_0 = 300$ K, heating rate $\beta = 1$ K/s. The peak maximum for the steel plate desorption is reached at 420 K.

As described, for pentacene T_M^{SS} amounted to 420 K and T_M^{Si} to 530 K and the adsorption temperature T_0 was always set to 300 K if not stated otherwise. For 8 nm of epindolidione the steel plate peak desorption temperature T_M^{SS} amounted to 430 K, while

the corresponding temperature for a SiO_2 sample T_M^{Si} increased to 560 K. This allowed meaningful parameter extraction out of TDS measurements after all TDS spectra had been temperature corrected according to equation (4-2).

4.2.2 Investigated Gate Dielectric Configurations

As discussed in chapter 2, the choice of the gate dielectric is crucial for the attainable OTFT performance in organic electronic systems [56]. In particular, at the highly critical dielectric-semiconductor interface, the dielectric material fundamentally influences the electrical properties as well as the layer growth and molecular orientation, and thereby the intermolecular π-π stacking necessary for charge transport between molecules [73,138–140].

As an electron trapping material [141], SiO_2 was a simple and easily available choice for the, mainly hole-conducting, organic semiconducting materials pentacene and epindolidione. Therefore, SiO_2, in its untreated, that is freshly installed, TDS residue carbon covered, and sputtered form has been investigated as a basic gate dielectric. For large parts of this work, we intentionally abstained from intensive sputtering of the dielectric, but rather tried to prepare stable and reproducible gold and silicon dioxide surfaces covered by a monolayer of carbon. Such stable surfaces were produced by repeated deposition and thermal desorption of pentacene, as checked by AES.

For the epindolidione experiments, a number of alternate dielectrics have been studied with the aim to optimize the resulting transistor performance. Głowacki *et al.* employed tetratetracontane-capped AlO_x layers as the gate dielectric and reported the non-polarity and/or aliphatic nature of the dielectric to be vital in achieving optimal device performance [55–57]. To gain more information on epindolidione performance on polar dielectrics we used SiO_2 in its untreated, carbon covered and sputtered form, which had previously only been investigated for the related quinacridone molecules but not epindolidione itself [142,143].

Additionally, we modified the SiO_2 surface with spin coated, comparably more hydrophobic capping layers in the form of the, relative to SiO_2, less polar, organic dielectrics poly(vinyl-cinnamate) (PVCi) and poly((±)endo,exo-bicyclo[2.2.1]hept-5-ene-2,3-dicarboxylic acid, diphenylester) (PNDPE, from the class of poly norbornenes) [64,144,145]. Subsequently, the gold source and drain contacts were deposited on top as usual.

The gate dielectric capacitance C_G, as mentioned as an important parameter in the equations (2-9) and (2-11) in chapter 2.2.3 on the mobility extraction from transfer curves, could be calculated from the relation

$$C_G = \frac{\varepsilon_0 \varepsilon_r}{d} \tag{4-3}$$

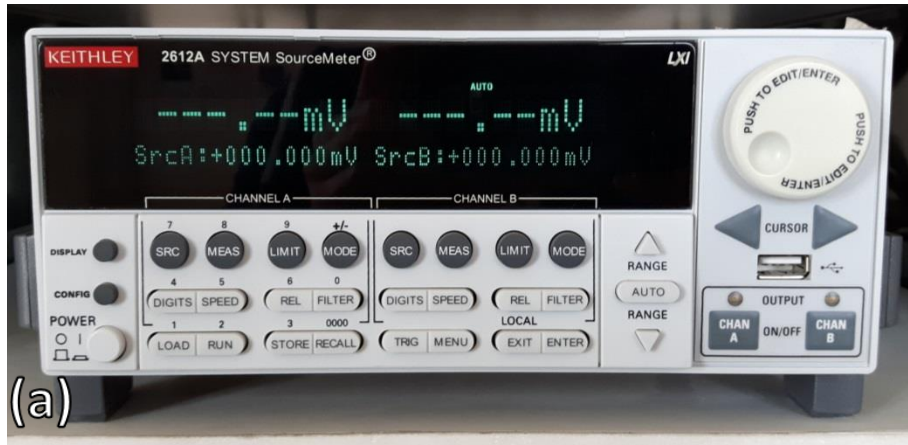
with the vacuum dielectric permittivity $\varepsilon_0 = 8.8 \times 10^{-12}$ As/Vm and gate dielectric permittivity ε_r, as well as the layer thickness of the dielectric d. As previously mentioned, the SiO_2 layer was 150 nm thick, while the spin coated layer thicknesses were approximately 35 nm for PVCi and 15 nm for PNDPE. The corresponding relative permittivities ε_r where obtained from literature for SiO_2 to be 3.9 [146] and extracted from capacitor structure measurements and calculated to be roughly 4.2 and 2.5 for PVCi and PNDPE, respectively. The gate dielectric capacitance for the full dielectric stack, C_G, then amounted to 23 nF/cm^2 for SiO_2, and 18.7 nF/cm^2 and 19.8 nF/cm^2 for the PVCi and PNDPE-capped systems, respectively. With this setup we were able to realize, characterize and reproduce coverage-dependent mobilities and threshold voltages for bottom-gate, gold bottom-contact, p-type conduction OTFTs.

4.2.3 Electrical Parameter Extraction and Characterization

The equations (2-9) and (2-11) in chapter 2.2.3 describe the dependence of the drain current I_{DS} on the drain-source voltage U_{DS} and the gate voltage U_{GS} in the various regimes, with the parameters gate dielectric capacitance C_G, carrier mobility in the semiconductor μ, channel width W, and channel length L. In our particular case, the geometric parameters amounted to $W = 4$ mm, $L = 25$ µm and the gate dielectric capacitances are discussed in the previous chapter.

For electrical characterization itself, a Keithley 2612A double source measure unit (SMU) was used (**Figure 4.13 (a)**), which was addressed via a specifically designed LabView® program (**Figure 4.13 (b)**) developed by T. Obermüller in the scope of his Master Thesis [147]. Using the formalism developed for silicon based FETs, the crucial device parameters saturation mobility (μ_{Sat}), linear mobility (μL_{in}) and threshold voltage (U_{Th}) were extracted out of measured transfer characteristics (drain-source current (I_{DS}) vs. gate-source voltage (U_{GS})) [69]. All devices were characterized in the common-low set-up, connecting the low ports of the gate and drain SMUs with the source electrode (see circuit in **Figure 2.1**). For the applied characterization and electrical shielding

system the measurement limits was reached at about 0.1 nA, yielding results for I_{DS} below this threshold meaningless.



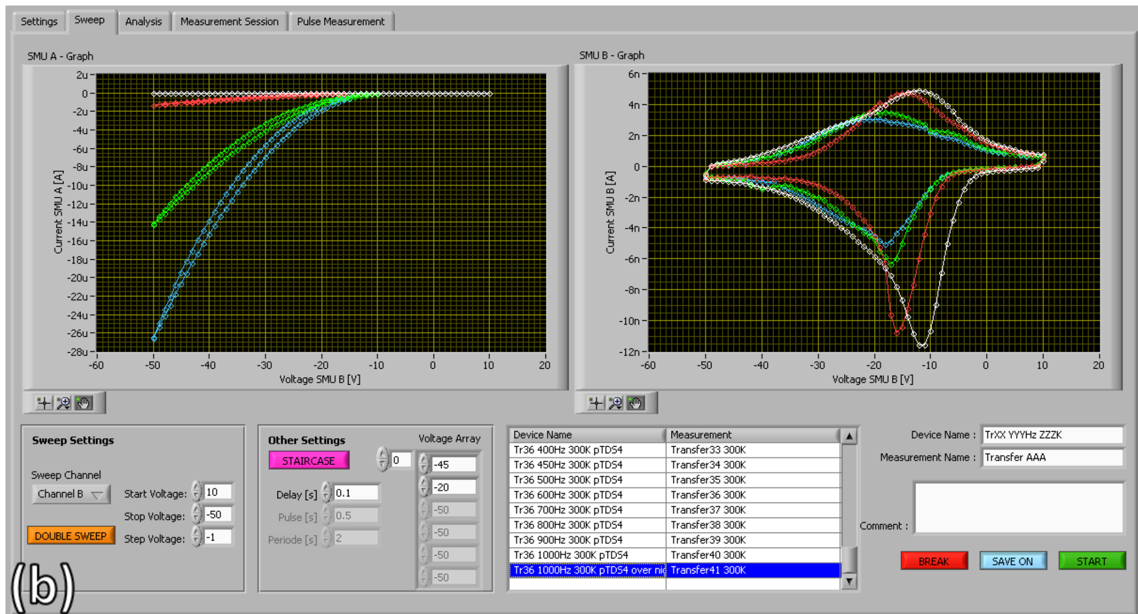


Figure 4.13: (a) Keithley 2612A double source meter [148] and (b) screenshot of the LabView® interface [147] for electric thin-film transistor characterization.

5 BASIC PENTACENE OTFTS

5.1 Introduction

The inherent advantage of room temperature processing and patterning for organic electronic systems enables a completely new class of temperature critical substrates and materials for device application, with associated qualities such as low-cost, flexibility, and bio-degradability [3,149]. With the first systems achieving commercial status, scientific focus expands from the hands-on creation of organic thin-film transistor devices towards more and more fundamental research. Indeed, device features of critical interest, such as transistor performance and organic semiconductor growth, are to the present date not fully understood and controllable in satisfactory detail. Closely tied to the transistor performance, the growth, structure, and charge transport properties of the organic semiconducting layers have to be identified and controlled to suit the respective applications. Additionally, the known disadvantages when it comes to attainable performance, air and water stability, and utilization on an industrial scale still have to be addressed and solved [13,14,16,17].

Pentacene ($C_{22}H_{14}$), as shown in the inset in **Figure 5.1**, is one of the most promising and most frequently studied organic semiconductors for the active component in OTFTs, which is mainly due to the observed high field-effect mobilities and ease of application. In order to demonstrate the potential and versatility of the experimental setup, as a first step, the classic OTFT model system pentacene on silicon dioxide with bottom-contact gold electrodes was investigated.

In the first part of the experimental section, the focus lay on the realization of highly reproducible devices, which was achieved by creating a saturation carbon layer,

both on the gold contacts and the gate oxide surfaces. The required samples had been created according to chapter 4.2 and were subsequently characterized by electrical characterization, Auger electron spectroscopy (AES), as well as thermal desorption spectroscopy (TDS) and atomic-force microscopy (AFM). The pentacene used for all experiments was purchased from Tokyo Chemical Industries and purified twice in a train sublimation system.

This chapter is in large parts based on a publication in the Journal of Applied Physics (Paper I, Ref. [44]), to which I have contributed as the leading author.

5.2 Calibration of the Deposition System for Pentacene

As described in chapter 4.1.2, the deposition system had to be calibrated in order to enable precise control over the deposited pentacene layer thickness. With the well-known density of pentacene of $\rho = 1.3$ g/cm^3 and equation (4-1) in chapter 4.1.2, a correlation between the frequency change Δf of the quartz microbalance (QMB) and the mean thickness Δd of the corresponding pentacene layer of $1\ \text{Hz} \equiv 0.094\ \text{nm}$ was obtained. However, coverage calibration of sub-monolayer films via AFM revealed that actually 1 Hz in frequency change corresponded rather to 0.08 nm, due to the actual geometry of the deposition setup. In combination with the nominal thickness of about 1.6 nm for a monolayer (ML) of standing pentacene molecules [150], a change of 20 Hz in the QMB resonance frequency corresponded to about 1 ML.

5.3 Initial Surface Preparation and Characterization

The basic transistor samples created according to chapter 4.2 were exposed to air and installed, without further cleaning, onto the appropriate sample holder for electrical contact and subsequently transferred into the UHV chamber for surface analytical and electrical characterization. On such a freshly installed sample, the gold contacts and the silicon dioxide surfaces were contaminated with an ill-defined carbon layer. Moderate sputtering with Argon ions, as described in chapter 4.1.3 (800 eV, 10 min. at 8×10^{-6} mbar Ar), was sufficient to remove the carbon from the surface. Heating of the sputtered surface to 800 K did not lead to further contamination. However, deposition of several monolayers of pentacene on the cleaned surface and subsequent desorption led to some pentacene decomposition, resulting again in a carbon contamination.

After proper tuning of the mass spectrometer to the optimal pentacene cracking mass of 125 amu, as described in detail in chapter 4.1.1, TDS investigations could be

commenced. Desorption spectra for pentacene from a SiO_2 surface after depositing 8 nm and 80 nm, respectively, which are characteristic for zero-order desorption, i.e., multilayer desorption [119], are shown in **Figure 5.1**. As discussed in chapter 4.2.1, the temperature scale as shown in this figure does not accurately reflect the true desorption temperature, due to the existence of a considerable temperature difference between the stainless steel sample holder, where the temperature is measured, and the sample surface, attributable to poor thermal conductivity of the insulating mica foil and the silicon sample itself. However, a simple first-order temperature correction was possible just by comparing the peak maximums of pentacene desorption from the sample with that from the stainless steel sample holder, which the thermocouple is connected to. It turns out that a measured peak temperature of 530 K for an 8 nm thick pentacene layer corresponds to a true desorption temperature of 420 K. This agrees nicely with the literature data [151]. It should be noted that for layers of this thickness (multilayers) no difference in the desorption behavior from the gold and silicon dioxide surface could be observed. Repeated pentacene adsorption and desorption eventually led to a saturation coverage of carbon, which was largely inert against further decomposition of pentacene. Such a surface is very stable and allowed repeated fabrication of transistors with high reproducibility. Unfortunately, based on the experimental techniques used (Auger spectroscopy) it was not possible to specify the chemical nature of the carbon layer. However, from literature it is known that carbon covered silicon dioxide shows a higher hydrophobicity [152]. On the contrary, transistors fabricated on freshly installed samples without further surface treatment showed quite strong variations in their electrical performance. In the inset of **Figure 5.1**, the correlation between the integrated TDS areas and the deposited amount, as measured by the quartz microbalance, is plotted. The linear relationship demonstrates the constant sticking coefficient in the whole coverage range. This suggests that the sticking coefficient of pentacene on the carbon covered gold and silicon oxide surface is one, independent of the coverage, allowing a precise determination of the deposited pentacene amount.

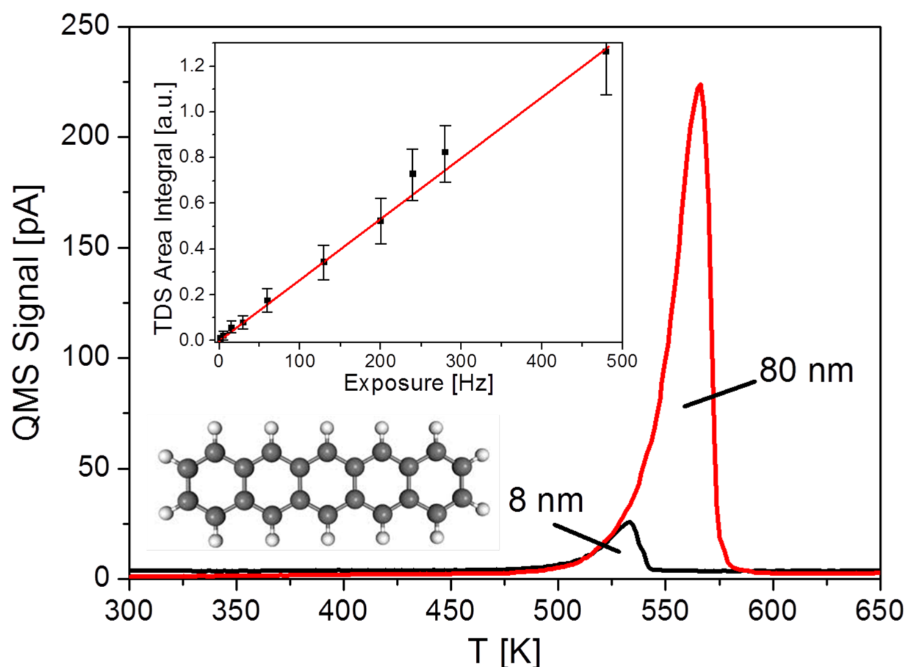


Figure 5.1: Desorption spectra of pentacene from the SiO_2 surface after deposition of 8 nm and 80 nm thick films at 300 K, respectively. Heating rate $\beta = 1$ K/s. Regarding the meaning of the measured temperature see chapter 4.2.1. In the insets, the molecular structure of pentacene and the correlation between TDS area and pentacene exposure are shown.

5.4 Electrical Characterization of a Stable Pentacene Device

The deposition of pentacene on the carbon saturated gold and SiO_2 surfaces yielded highly reproducible device properties. In **Figure 5.2**, representative output (a) and transfer characteristics (b) for an 8 nm thick pentacene device are presented, with the film being deposited and measured *in situ* at 300 K. The transfer curve is shown in forward and reverse measurement and indicates an almost hysteresis free behavior.

The scan rate for the transfer and output curves was 5 V/sec. From **Figure 5.2 (a)** and **(b)** and the evaluation according to chapter 2.2, we obtain field-effect mobilities of $\mu_{Sat} = 2.3\times10^{-3}$ cm^2/Vs and $\mu_{Lin} = 1.4\times10^{-3}$ cm^2/Vs, a threshold voltage of $U_{Th} = -13$ V, an onset voltage $U_{On} = -1$ V, and the ratio $I_{On}/I_{Off} \approx 1\times10^4$. μ_{Sat} was derived from the slope of the linear part of the $\sqrt{I_{DS}}$ vs U_{GS} plot, with $U_{DS} = -50$ V and $U_{GSmax} = -50$ V. The sub-threshold swing amounted to 3.6 V/decade. The linear mobility μ_{Lin} was derived from the linear part of the transfer curve for $U_{DS} = -3$ V (not shown).

Although the obtained mobilities are smaller than those reported in the literature for similar pentacene transistors in bottom-contact configuration (0.1 – 0.3 cm^2/Vs)

[153], the asset of our setup was that we can repeatedly desorb the pentacene film and deposit another layer of the same thickness, resulting in the same outcome within a relatively small margin of error. This is shown in **Figure 5.3**, where output and transfer characteristics were analyzed in terms of saturation mobility and threshold voltage for ten pentacene films of 8 nm thickness, prepared by repeated adsorption and desorption processes. The obtained values for the mobility did not take possible influences of the contact resistance into account. Thus, these values should be seen as effective mobilities, allowing a comparison in device-quality for specific preparation conditions. Actually, the particular non-linear shape of the output characteristic at low drain voltage (**Figure 5.2 (b)**) hints at a possible influence of the contact resistance [69].

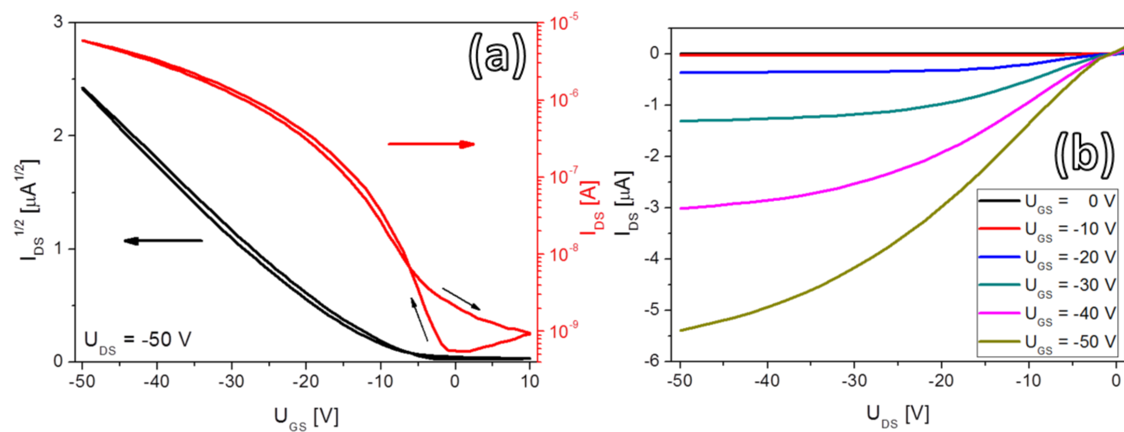


Figure 5.2: (a) Transfer and (b) output characteristics, measured at 300 K, of an 8 nm thick pentacene film after deposition on a carbon covered device at 300 K.

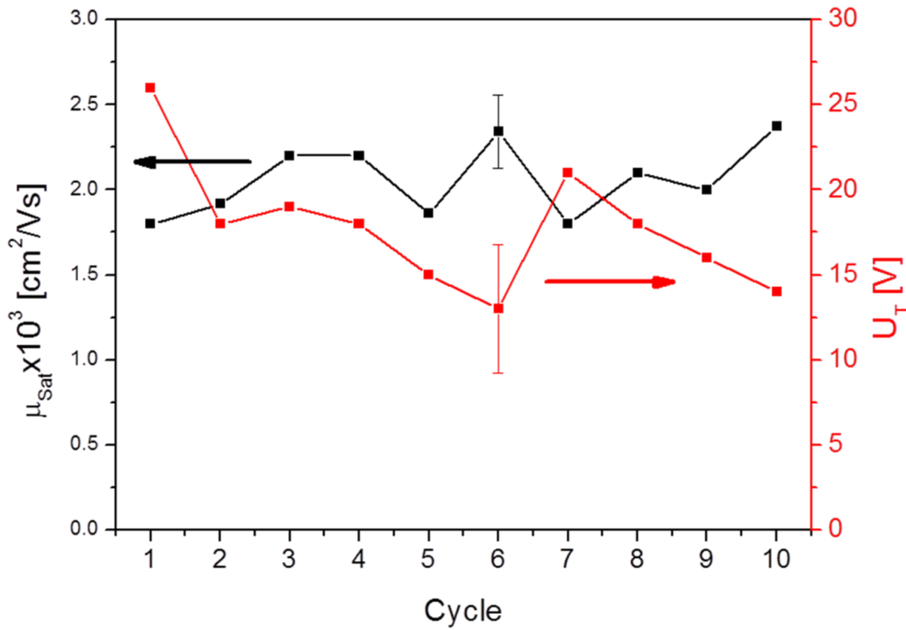


Figure 5.3: Saturation mobilities and threshold voltages for ten subsequently prepared devices by adsorption and desorption of 8 nm thick pentacene films. Adsorption and measurement temperature was 300 K. For cycle 6 the calculated standard deviations are added as exemplary error bars.

5.5 Influence of Sample Preparation Temperature

It is commonly known that device properties crucially depend on the morphology of the active layer in the channel and in the transition region between channel and contact area [69]. In addition, the morphology depends on the substrate chemical composition, as well as on the deposition rate and substrate temperature, as described in some detail in the literature [31,34,151]. In this section the focus is on the influence of the substrate temperature during deposition. Transfer and output characteristics for an 8 nm thick pentacene film deposited at 200 K and consequently warmed up to 300 K for electrical characterization have already been shown in the introduction as **Figure 2.4 (a)** and **(b)** and display behavior comparable to **Figure 5.2**. A significant improvement of the device performance could be observed. The mobilities increased by a factor of 15 (μ_{Sat} = 3.6×10^{-2} cm^2/Vs, μ_{Lin} = 2.3×10^{-2} cm^2/Vs), the on/off-ratio was now ~10^5, and U_{Th} and U_{On} changed to -17 V and -1 V, respectively. It is most reasonable to assume that the change in the characteristics was due to morphological changes at the oxide/semiconductor interface and/or at the contact/semiconductor interface. This was supported by AFM measurements of 12 nm thick pentacene films, deposited on SiO_2 at 300 K and 200 K, respectively, as shown in **Figure 5.4**. While the film deposited at

300 K showed the well-known terraced mounds of micrometer size [31,85] and an average island height of approximately 7 nm, the film prepared at 200 K was composed of very small grains with an average size of less than 200 nm and an average island height of approximately 4 nm.

To get more information on this subject and to see if the morphological change happens at a particular temperature, an 8 nm thick film was prepared and repeatedly heated to increasing terminating temperatures and subsequently cooled to 200 K for electrical characterization. This is summarized in **Figure 5.5** where the saturation mobility is plotted vs the maximum heating temperature. For these experiments, the samples were heated with a rate of 1 K/s to the desired final temperature and immediately cooled down afterwards. This experiment showed that the performance of the device increases continuously with temperature, most probably due to a continuous irreversible morphological change of the active layer in the channel region and at the interface. For the value at 350 K the film was held at this temperature for 5 min.

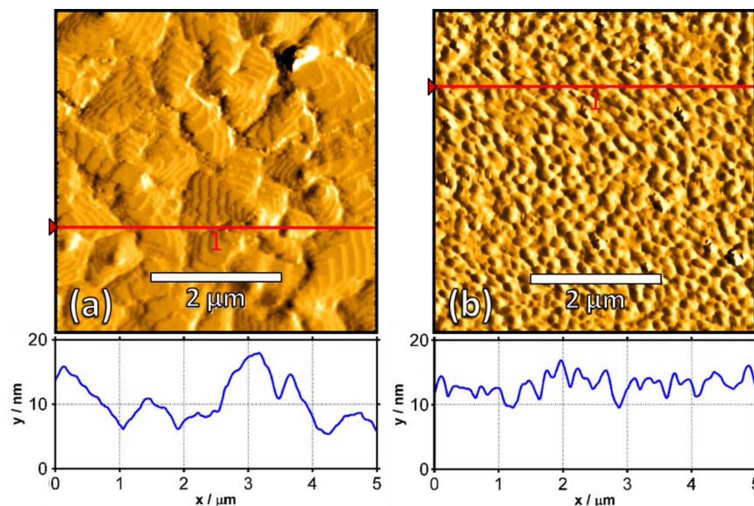


Figure 5.4: AFM images (5 µm×5 µm) of 12 nm thick pentacene films on silicon dioxide, deposited at 300 K (a) and at 200 K (b). The corresponding cross sections are indicated by a red line in the AFM images and shown underneath. The measurements were performed at 300 K.

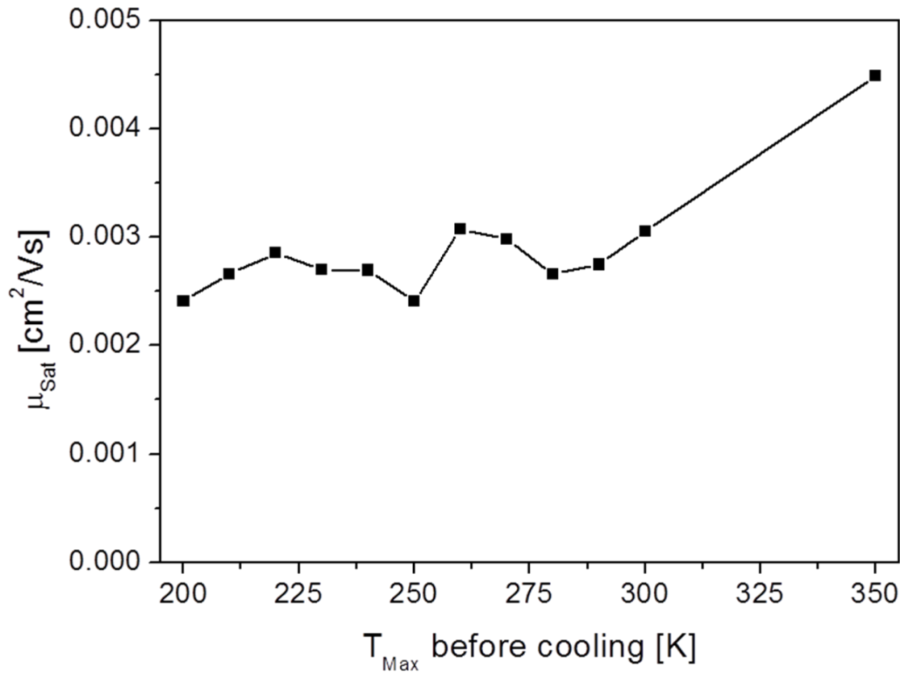


Figure 5.5: Improvement of the saturation mobility due to heating to the indicated temperatures of an 8 nm film deposited at 200 K. Device characterization was done at 200 K in all cases.

In order to check the thermal stability of the devices, similar experiments were performed by annealing films to increasing terminating temperatures up to the desorption temperature, as shown in **Figure 5.6**. In this case, the pentacene film was deposited at 200 K and subsequently annealed at 350 K for several hours, before the actual experiment was started. The device characterization after the heating steps was always done at 300 K. This is the reason why in this case the mobilities are larger than those derived from **Figure 2.4 (b)**. It can be seen that already some diminution of the mobility sets in at an annealing temperature of about 350 K, although desorption of pentacene has not yet started. This hinted to morphological changes in the channel area, most probably due to dewetting processes. The mobility decreased drastically when desorption set in, as determined by TDS, and already reached zero with about 3 nm of pentacene still present on the surface. This was a further indication of strong dewetting prior and/or during desorption.

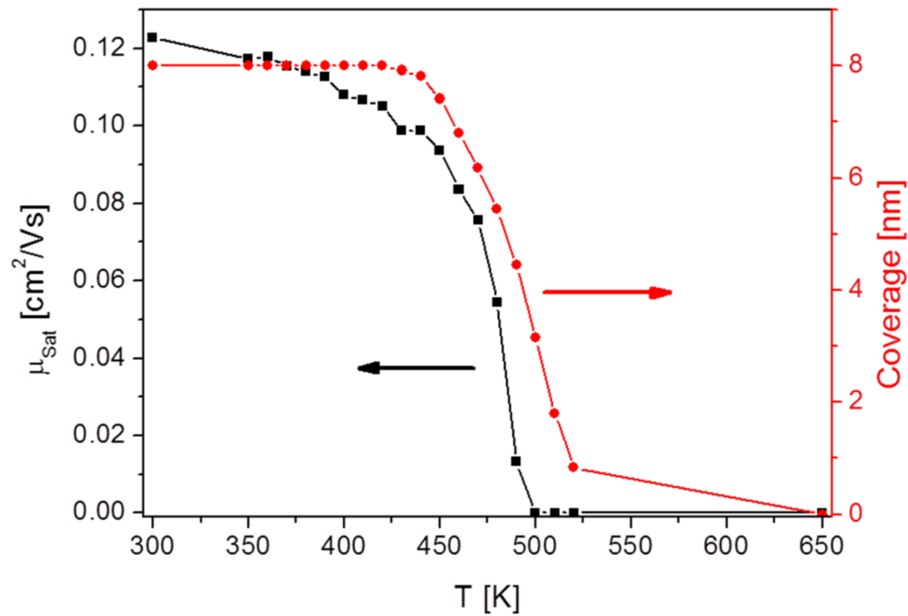


Figure 5.6: Mobility change with increasing annealing temperature up to the indicated temperature values after deposition of 8 nm pentacene at 200 K and initial annealing at 350 K for several hours. Device characterization was done at 300 K. In addition, the remaining coverage after each annealing step, as determined by TDS, is shown.

5.6 Temperature Dependence of the Field-Effect Mobility

After a pentacene film has been prepared at 200 K and annealed to 350 K, no further morphology changes can be expected when remaining in this temperature interval. This allowed the measurement of the mobility as a function of device temperature and hence to get information on activation barriers involved in the generation of the drain current according to chapter 2.2. In **Figure 5.7 (a)**, the logarithm of the saturation mobility μ_{Sat} and the linear mobility μ_{Lin} are plotted vs $1/T$ for an 80 nm thick pentacene layer prepared at 200 K, then cooled to 125 K (squares), afterwards heated to 350 K (diamonds), and then again cycled between 350 K and 125 K (circles and triangles). One sees that the mobility was reversible between 200 K and 125 K, demonstrating that in this temperature range no morphological changes took place. However, increasing the temperature to 350 K led to a stronger than expected increase of the mobility at around room temperature. A subsequent cooling/heating cycle between 350 K and 125 K did not show a hysteresis, indicating that the pentacene film was now morphologically stable in this temperature range.

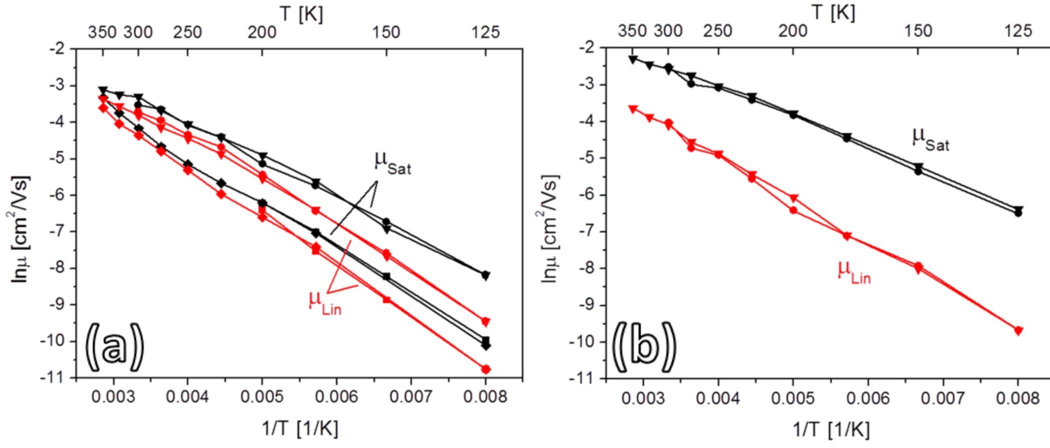


Figure 5.7: (a) Temperature dependence of saturation and linear mobility for an 80 nm thick pentacene device, prepared at 200 K, cooled to 125 K (squares), then heated to 350 K (diamonds), and subsequently cycled once more between 350 K and 125 K (circles and triangles). (b) Similar experiment after deposition of an 80 nm thick pentacene film at 300 K, cooled to 125 K (circles), and heated subsequently to 350 K (triangles).

Using the MTR model (chapter 2.2.1), the data in **Figure 5.7 (a)** and **(b)** could be evaluated. It is observable that the curve in the ln μ vs $1/T$ do not follow a straight line, but are slightly bent, indicating a distribution of activation barriers. Nevertheless, a linear least squares fit through the data set of **Figure 5.7 (a)** (film prepared at 200 K) yielded (mean) activation barriers of $E_A = 100\pm10$ meV, obtained from the linear mobility ($U_{GSmax} = -50$ V, $U_{DS} = -3$ V) and $E_A = 91\pm10$ meV, obtained from the saturation mobility ($U_{GSmax} = -50$ V, $U_{DS} = -50$ V). The absolute values for the saturation mobility were always larger by a factor of about 2 at room temperature than for the linear mobility and the difference increased to a factor of about 4 at 125 K. Equivalent evaluation of the data set in **Figure 5.7 (b)** (film prepared at 300 K) yielded activation energies of $E_A = 103\pm10$ meV, obtained from the linear mobility, and $E_A = 66\pm10$ meV as obtained from the saturation mobility. The derived values for the saturation mobilities were larger by a factor of 4 at 300 K and of about 30 at 125 K compared to the linear mobilities.

For the pre-exponential factor $\mu_0\alpha$ of equation (2-5), for measurements at room temperature, the following values were obtained: For the 200 K prepared device, using μ_{Lin} yielded $\mu_0\alpha = 1.15$ cm^2/Vs and using μ_{Sat} yields $\mu_0\alpha = 1.08$ cm^2/Vs. For the 300 K prepared device, using μ_{Lin} yielded $\mu_0\alpha = 0.93$ cm^2/Vs and using μ_{Sat} yielded $\mu_0\alpha = 1.03$ cm^2/Vs. It is interesting to note that similar values were obtained for

$\mu_0 \alpha$ (1.0±0.1 cm^2/Vs) for all cases, although the film prepared at 200 K showed a much higher grain density than the one prepared at 300 K (**Figure 5.4**). This suggests that the observed temperature dependence of the mobility was indeed mainly determined by the activation of shallow trap states in the pentacene islands, rather than by the thermionic emission between islands. Making use of the above mentioned relationship $\alpha = E_A/kT$ and taking an average activation barrier of 80 meV into account, a value of $\alpha \approx 3$ was obtained, and consequently a free carrier mobility for pentacene of about 0.3 cm^2/Vs.

Further information on the physics involved could be obtained from the changes of the threshold voltage U_{Th} and onset voltage U_{On} as a function of temperature. These values are summarized in **Figure 5.8** for pentacene films prepared at 200 K and 300 K, respectively. The threshold voltage increased nearly linearly from about -35 V at 150 K to about -14 V at 350 K for the film prepared at 200 K, and from -31 V at 150 K to -9 V at 350 K, for the film prepared at 300 K. Similarly, the onset voltage changed from -18 V at 125 K to +2 V at 350 K for the 300 K sample. For the 200 K sample, U_{On} changed from -20 V to +4 V in the same temperature regime (not shown for clarity reasons).

The increase of the threshold voltage (higher negative values) with decreasing temperature can be explained by the mobility edge model, as mentioned in chapter 2.2.1. The fact that for the devices prepared at 200 K a higher negative threshold voltage was needed, compared to the devices prepared at 300 K, hints to a correlation between the density of deep traps and the grain density in the semiconducting film (**Figure 5.4**). Thus, one can draw the conclusion that the deep traps are mainly located at the grain boundaries.

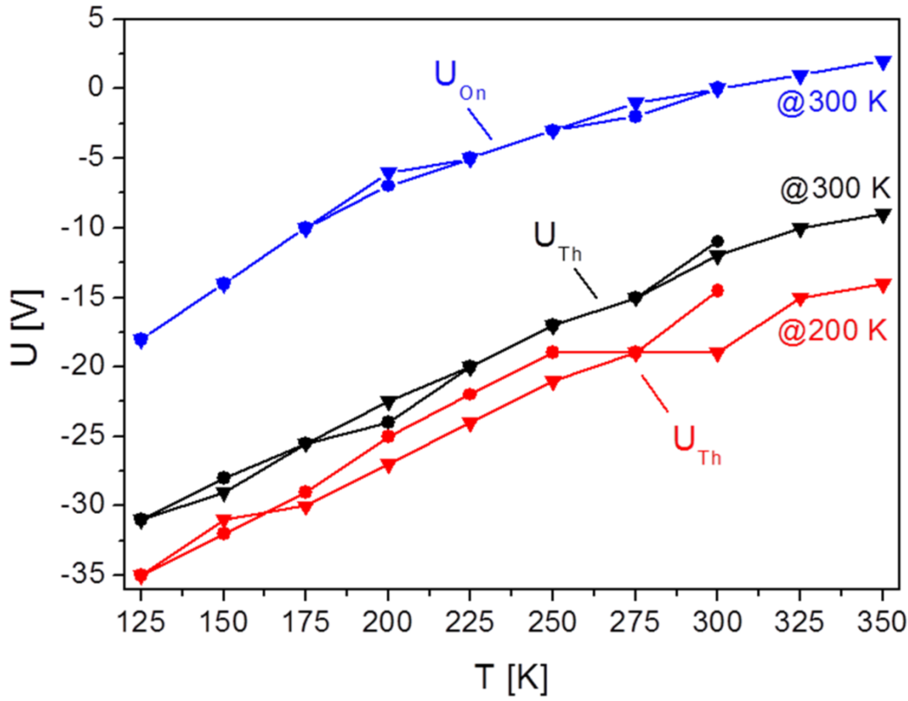


Figure 5.8: Temperature dependence of the threshold voltage U_{Th} and onset voltage U_{On} for 80 nm thick pentacene devices, prepared at 200 K and 300 K, respectively. U_{On} for the 200 K sample is, for clarity reasons, not shown, but has a similar offset compared to U_{Th}, as shown for the 300 K sample. The circles indicate the cooling to 125 K and the triangles indicate the subsequent heating up to 350 K.

5.7 Thickness Dependence of the Mobility

A further advantage of *in situ* film preparation and simultaneous electrical characterization is the possibility to determine the electrical behavior as a function of film thickness. There exists some literature dealing with this subject for pentacene devices; however, the reported results showed quite a few discrepancies. While there is agreement that drain-source current starts to flow when the first monolayer is completed (or slightly before), there are differing statements as to the saturation of the drain current (or mobility) and the change of the threshold voltage with film thickness. Park *et al.* [41] reported a drain current saturation for pentacene at two monolayers (3 nm) already, Liu *et al.* [31] observed saturation around 7 nm, Kiguchi *et al.* [30], Shehu *et al.* [34], and Ruiz *et al.* [42] found saturation at around 10 nm, Fiebig *et al.* [36] noted saturation of the mobility above 30 nm and Wang and Cheng [43] reported threshold voltage (and mobility) changes up to 180 nm.

Therefore, output and transfer characteristics have been measured as a function of thickness for devices prepared at 300 K and 200 K and the linear and saturation

mobilities, as well as the threshold and onset voltages have been evaluated. In **Figure 5.9** μ_{Lin} and μ_{Sat} are compiled for films in the range of 0 – 10 nm mean thickness.

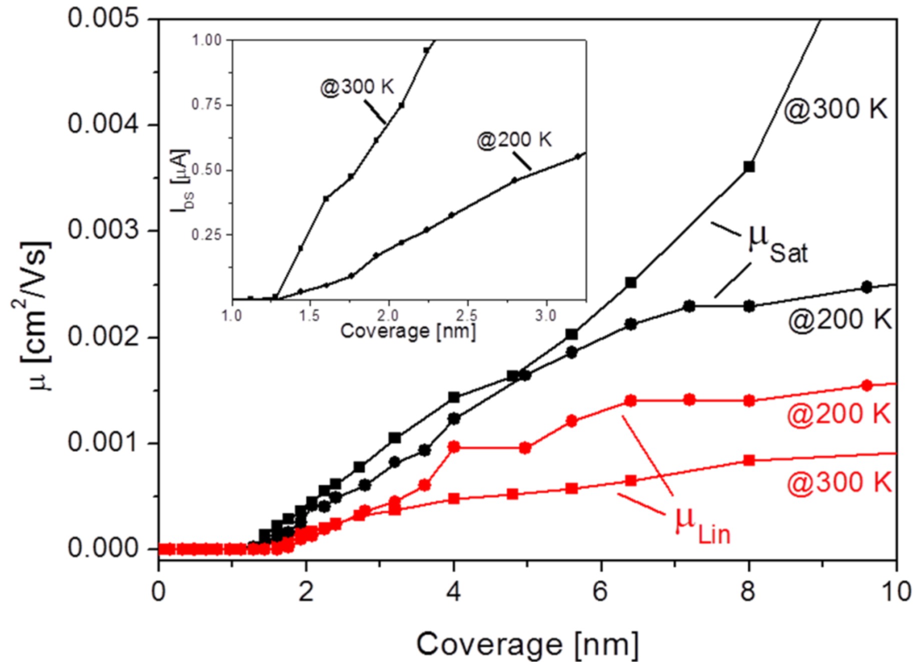


Figure 5.9: Linear (red symbols) and saturation (black symbols) mobilities in the low coverage regime for pentacene films prepared and measured at 200 K (circles) and 300 K (squares), respectively. In the inset, the onset of I_{DS} in the very low coverage regime is shown.

In the inset of **Figure 5.9**, the onset of the drain current at the very beginning of channel conductivity is shown. A sharp onset at about 1.3 nm, equivalent to a coverage of 0.86 monolayers of standing molecules, is observable. This agreed quite well with the percolation threshold of about 0.7 monolayers, depending on the models used [154–156]. The fact that the mobility was smaller for the film when prepared and measured at 200 K was mainly due to its temperature dependence, as shown in the previous chapter. With increasing coverage, the linear mobility increased and reached a weakly pronounced saturation at about 6 nm (4 ML) for both the 200 K and 300 K prepared films. Interestingly, the saturation mobility for a film prepared at room temperature did not show a saturation in this coverage range. In **Figure 5.10**, the evolution of the mobilities for even thicker films is depicted. For the film deposited at 200 K, a final saturation of the mobilities was reached at about 10 nm. However, for the film prepared at room temperature a further mobility increase was observed, which did not show saturation before a coverage of about 40 nm. Considering the fact that the mobilities measured at 300 K were by about a factor of 5 larger than those measured at 200 K (for

the same morphology), as shown in the previous chapter, it is interesting to note that the saturation mobility for the thick film prepared at 300 K was still larger than for the film prepared at 200 K, but measured at 300 K. However, the opposite behavior was observed in the low coverage regime (<10 nm). Here, the temperature corrected μ_{Lin} and μ_{Sat} were significantly larger for the films prepared at 200 K compared to those prepared at 300 K. For completeness, the threshold and onset voltage as a function of pentacene coverage have also been evaluated, for preparation at 200 K and 300 K, respectively, as shown in **Figure 5.11**.

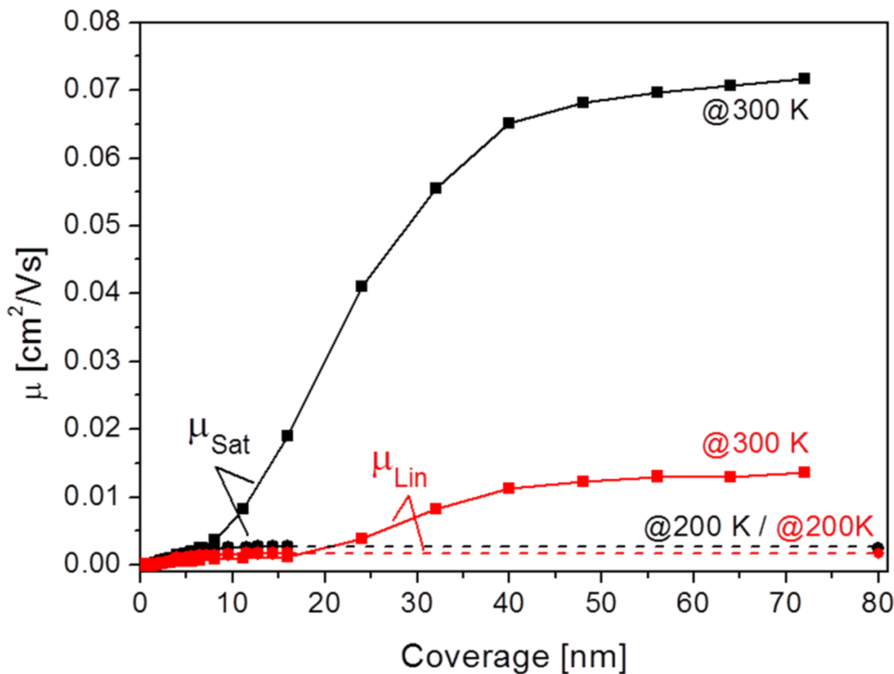


Figure 5.10: Linear (red symbols) and saturation (black symbols) mobilities in the high coverage regime for pentacene films prepared and measured at 200 K (circles) and 300 K (squares).

From this set of data, the following conclusions could be drawn: The onset of the channel current agreed quite well with the percolation of the first monolayer of standing pentacene molecules, more or less independent of the substrate temperature. With increasing coverage, the measured mobilities increased and reached a first saturation at about 6 nm (4 ML). Taking the temperature dependence of the mobility into account, in this coverage regime the mobility for 200 K prepared films was by a factor of about 5 higher than that for 300 K devices. This was most likely a result of the different film morphologies. At room temperature, pentacene showed clear Stranski-Krastanov growth [108], where the first layer nearly fully closes before further layers start to form. The additional layers then showed strong islanding, due to a high Ehrlich-Schwoebel

barrier [109,110] for step-down diffusion (**Figure 5.4**). At 200 K sample temperature, the first layer still developed quite well, although the island density increased by more than a factor of 20 to approximately 30 islands per µm^2 from approximately 1.5 islands per µm^2 at 300 K. However, the following layers were also composed of many small islands, where step-down diffusion was facilitated and a more layer-like film growth took place. According to the investigations of the Biscarini group [34], it is known that not only the first layer contributes to the channel current but that the effective Debye length can reach up to 5 ML into the semiconductor. Thus, in a fine-grained, layer-like film, several layers, which are already percolated, will allow more charge to flow than in a Stranski-Krastanov film, where only little percolation exists above the first layer. On the other hand, at higher grain density more charge traps will be generated, which decreases the mobility [157]. Thus, at higher coverage when finally many layers of the 300 K prepared film were percolated, the smaller grain density and probably also the better molecular structure in the grains finally yielded a higher mobility for the 300 K film than for the pentacene film prepared at 200 K.

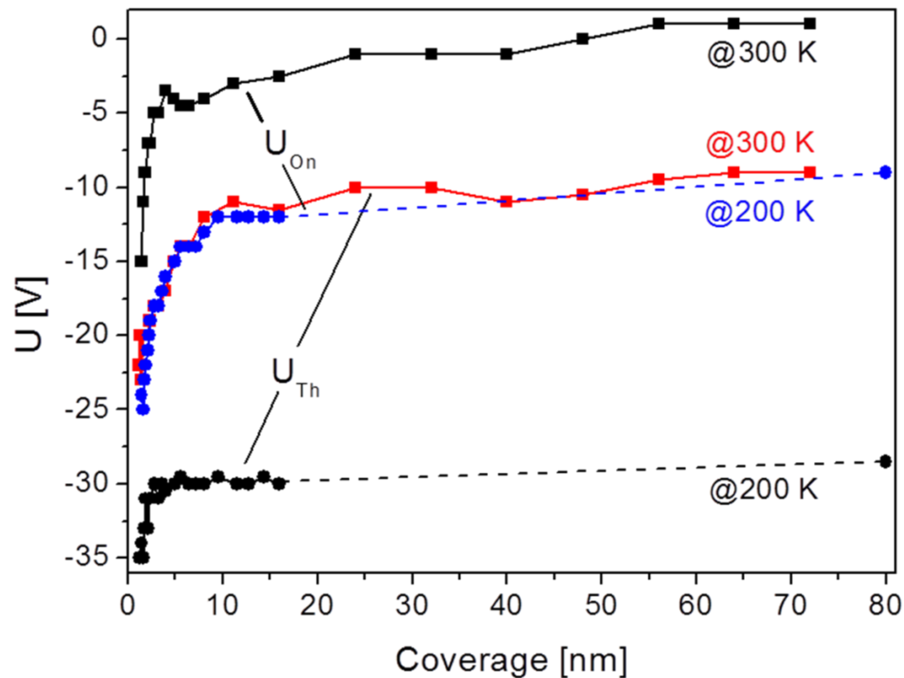


Figure 5.11: Coverage dependence of the threshold and onset voltage for pentacene devices prepared at 200 K and 300 K.

In addition to the grain density and percolation within the film, the contact between the semiconductor and the gold electrodes (access resistance) will finally determine the channel current and thus the effective mobility. This was the reason for

the further increase in mobility above 15 nm for the 300 K film, which finally led to saturation above 50 nm mean thickness. This assumption was supported by the coverage dependence of the threshold and onset voltage, which are characteristic quantities reflecting the physics involved in the charge carrier transport. A significant change of these values only up to a coverage of about 10 nm, for the 300 K film, and up to about 5 nm for the 200 K film was observed. This is the coverage regime where the mobility is governed by increasing film thickness within the Debye length. For the 200 K film, the initial U_{Th} had a value of -35 V, whereas U_{Th} = -23 V for the 300 K film. This was in accord with the above stated correlation between the threshold voltage and the density of deep traps due to the grain density. Interestingly, with increasing coverage the threshold voltage changed to less negative values by about 13 V for the 300 K film and by about 5 V for the 200 K film, which suggested a decrease of the deep hole traps with increasing film thickness. Fiebig *et al.* [36], who found a very similar threshold change as a function of coverage, postulated the formation of electron traps in the semiconductor and/or the surface of the film. With increasing film thickness more electron traps exist, which are filled by electrons. This leads to negative charging of the film and consequently a more positive gate voltage is needed for compensation. For the 200 K film, the surface was less corrugated and a constant threshold voltage was reached earlier than for the 300 K film, which was composed of large mounds. The fact that no significant change of the threshold and onset voltage with further coverage increase took place demonstrated that the mobility change in this coverage range was not due to a conductivity change in the semiconductor but most likely due to a changed access resistance at the Au-pentacene interface.

5.8 Chapter Summary and Conclusions

In this chapter, *in situ* preparation, electrical and surface analytical characterization of bottom-gate, bottom-contact pentacene transistors have been described, which allowed the fabrication of highly reproducible devices. With the special sample holder setup, it was possible to cool each device to 125 K and heat it to 800 K, if so desired. By repeated deposition and desorption of pentacene on the model device, both the gold contact pads and the SiO_2 channel were intentionally contaminated with carbon, as verified by Auger electron spectroscopy. Although this surface modification reduced the absolute values of the charge carrier mobility, devices with unprecedented reproducibility could repeatedly be established. The focus lay on the

impact of the film morphology on the temperature and coverage dependency of the mobility and threshold voltage. While the deposition of pentacene at room temperature led to the well-known Stranski-Krastanov film morphology, deposition at 200 K resulted in a fine grained, nearly layer like film. It was shown that the threshold voltage is mainly governed by deep traps induced by the grain boundaries, while the temperature dependence of the mobility can be described well by the multiple trapping and release model, when assuming that the shallow traps are mainly located within the grains. With respect to the coverage dependency, the onset of channel conductance at a percolation threshold of about 0.8 ML was observed, followed by an intermediate saturation of the mobility at around 4 ML. This demonstrated that charge transport is not restricted to the oxide/semiconductor interface and the very first layer, as sometimes assumed, but that rather several layers contribute to the channel current. In this coverage range, the mobility for the 200 K prepared device was larger than that for the 300 K device, due to the more layer-like film morphology within the Debye length. With further coverage increase, the mobility of the 300 K device once more increased until a saturation was eventually reached at about 50 nm thickness. Since this continued mobility increase did not take place for the 200 K device this behavior was traced back to insufficient connections of the pentacene film to the gold contacts at higher substrate temperature due to poor wetting (increased access resistance). For a sufficiently thick film, when charge transport was not limited by the contact resistance, films grown at 300 K showed higher mobilities than those deposited at 200 K sample temperature, due to the smaller grain density and probably also due to a better molecular structure within the grains.

6 IMPROVED PENTACENE OTFTS

6.1 Introduction

The complementary measurements described in this part of the thesis address and expand the results for pentacene growth discussed in the previous chapter. Pentacene layers were deposited on carbon contaminated as well as sputter cleaned SiO_2 for sample temperatures up to 350 K. This allowed gaining further insight into the optimal processing temperatures for pentacene deposition for a range of semiconductor thicknesses. Based on the gained information it was possible to prepare mixed layer systems, featuring different sample temperatures during deposition, which showed improved transistor behavior.

In the previous chapter, a saturation of the mobility at a layer thickness of about 4 monolayers (approximately 6.4 nm) for low temperature (200 K) layers had been reported. For room temperature deposition a significant additional mobility increase up to 50 nm layer thickness was observed. This was attributed to a decrease of the access resistance due to better, continuous film formation in the silicon dioxide-gold electrode transition region [44]. In **Figure 6.1** a schematic, graphical representation of the processes investigated in this chapter is shown.

This chapter is in large parts based on a publication in the journal Organic Electronics (Paper II, Ref. [45]), to which I have contributed as the leading author.

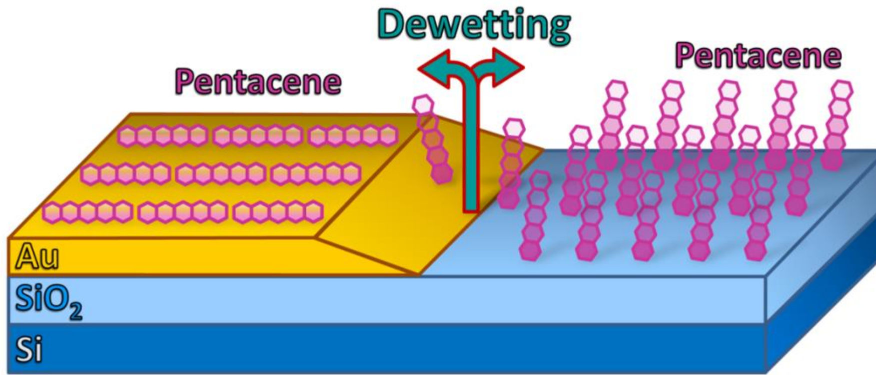


Figure 6.1: Graphical abstract of the processes investigated in this chapter.

6.2 Preparation Condition Matrix

The main intention of this experimental chapter was to reach a comprehensive understanding of the influence of film preparation parameters on the transistor properties. For this purpose, pentacene films on a SiO_2 bottom-gate, gold bottom-contact configuration were deposited at three different temperatures (200 K, 300 K, 350 K). Following the preceding investigations in chapter 5 on substrates, which had been sputter cleaned before creating a carbon saturation layer (labeled as Sputtered + C), the investigations were expanded to the contrasting surface conditions of unsputtered and additionally carbon covered samples through repeated pentacene adsorption/desorption cycles (labeled Unsputtered + C) as well as sputter cleaned samples (labeled Sputtered). The carbon saturation layer was established by repeated adsorption/desorption cycles of pentacene layers, as described in more detail in the previous chapter. For all of the samples (3 temperatures, 3 surface conditions) full *in situ* electrical characterization was performed via output and transfer curves and subsequently the film morphology was investigated by *ex situ* AFM in the SiO_2 channel region, the gold contact region and in the very important SiO_2-Au transition region. This resulted in a (3×3×3) information matrix. Additionally, the experimental systems unique possibility of repeated pentacene deposition and removal allowed the depicted coverage dependency measurements to be performed on a single silicon wafer sample for each parameter set and therefore ensured optimal reproducibility for the displayed results. The obtained values for the mobilities and threshold voltages showed excellent agreement with the previous measurements for similar parameter sets. This comparability of measurements performed over a timespan of more than a year and over 50 samples is proof of the reliability and reproducibility provided by the experimental setup.

6.3 Coverage-Dependent Mobility on Unsputtered + C Samples

A series of pentacene transistors were prepared on the Unsputtered + C sample surface at 200 K, 300 K and 350 K. The corresponding output and transfer curves were recorded for parameter extraction, in particular the mobility and threshold voltage as a function of coverage. The mobility evolution with increasing pentacene layer thickness for these temperatures in a coverage range of 0 – 150 nm, as well as an inset depicting the formation of the first percolation layer for electrical conductivity at low coverage are shown in **Figure 6.2**. Characteristic output and transfer curves for the three temperature regimes are shown in the **Figure 6.3**, **Figure 6.4** and **Figure 6.5**. The non-linearity for low drain-source voltages (U_{DS}) in **Figure 6.4** and **Figure 6.5** could be related to contact resistance effects [69].

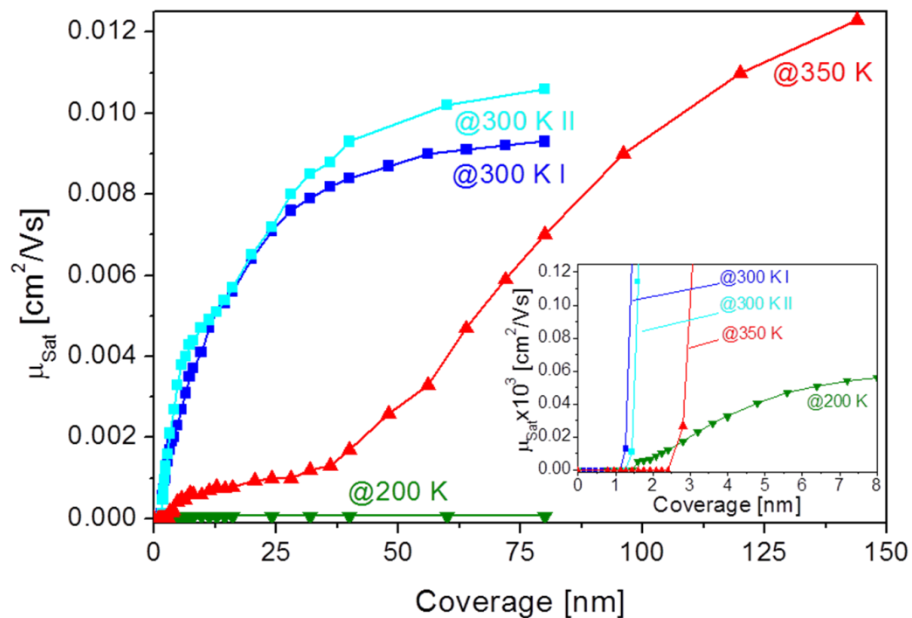


Figure 6.2: Saturation mobility μ_{Sat} as a function of coverage for pentacene films on the Unsputtered + C SiO_2 surface, prepared and measured at 200 K, 300 K and 350 K, respectively. The inset shows the onset of transistor behavior in the very low coverage regime.

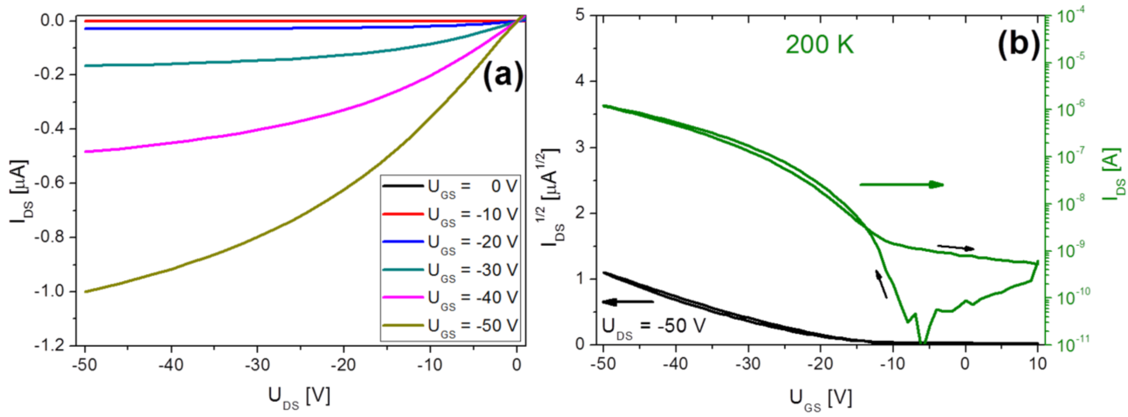


Figure 6.3: (a) Output and (b) transfer characteristics of an 80 nm thick pentacene film on an Unsputtered + C surface, deposited at 200 K and measured at 300 K sample temperature.

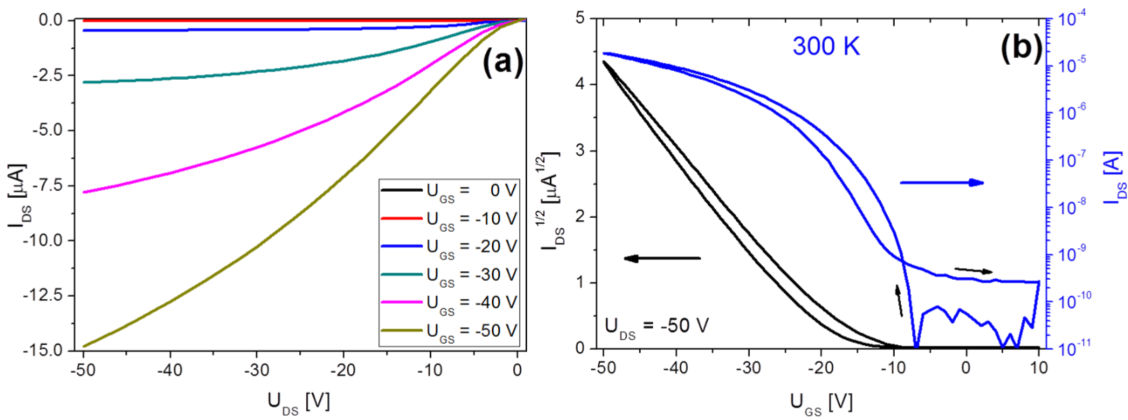


Figure 6.4: (a) Output and (b) transfer characteristics of an 80 nm thick pentacene film on an Unsputtered + C surface, deposited and measured at 300 K sample temperature.

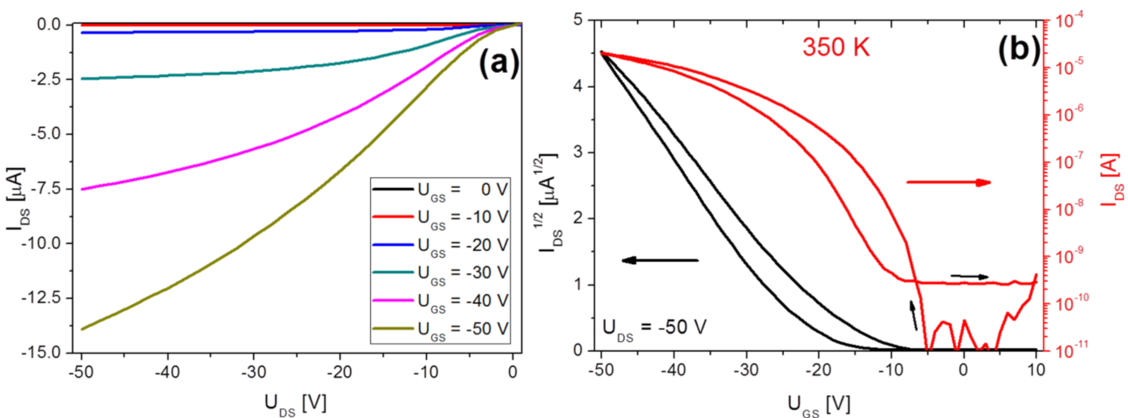


Figure 6.5: (a) Output and (b) transfer characteristics of a 144 nm thick pentacene film on an Unsputtered + C surface, deposited at 350 K and measured at 300 K.

6.3.1 Pentacene Deposition at 200 K and 300 K

An immediately observable feature in the electrical evaluations was the excellent reproducibility within error margins when it comes to the extracted mobility values for the two 300 K measurements on the Unsputtered + C surface. The first drain-source currents and therefore mobilities larger than zero could be observed at around 1.2 nm to 1.5 nm nominal pentacene coverage for the 200 K and 300 K layers (see inset in **Figure 6.2**), equivalent to a layer thickness of approximately 0.75 monolayers, which in turn showed good agreement with the postulated percolation threshold of about 0.7 monolayers reported by other groups [154–156]. The maximum recorded saturation mobilities for both temperatures on the Unsputtered + C surface were roughly a factor of 10 lower than the results on the Sputtered + C samples discussed in the previous chapter [44], indicating a strong influence of the surface preparation. The 200 K growth showed mobility saturation at the completion of 3 - 4 monolayers, corresponding to approximately 5 - 7 nm of nominal pentacene coverage. This saturation indicated the complete filling of all the charge contributing semiconducting layers in the channel region within the Debye length [34,39,40]. AFM investigations on 1.5 ML (equivalent to 2.4 nm) of pentacene in the channel and in the gold contact region, as well as 7.5 ML (12 nm) in the transition between those two, revealed the underlying layer growth responsible for the electrical results (**Figure 6.6**). At the comparably low process temperature of 200 K the pentacene molecules impinge on the surface and stick within a comparably short timeframe, without having the possibility to diffuse over a large area in order to occupy an energetically more favorable site, such as the accommodation at an existing island edge [103]. This led to the formation and growth of a high number of small, sub 250 nm diameter grains on the silicon dioxide (**Figure 6.6 (a)**) (The very large mean layer thickness suggested by the cross section was caused by the numerous high and pointy islands and a resulting overestimation and feature broadening by the AFM tip.) On gold (**Figure 6.6 (b)**), the low temperature also significantly influenced the layer growth of the pentacene islands, leading to a distribution of short but high 3D-islands with a maximum length of about half a µm. According to Käfer *et al.* [151] these islands are composed of lying molecules. In **Figure 6.6 (c)** an AFM analysis on 7.5 ML of pentacene in the transition from the gold contact area (top left) to the channel region is shown. The small grains forming at 200 K substrate temperature covered the whole transition region uniformly, as can be observed in the cross section.

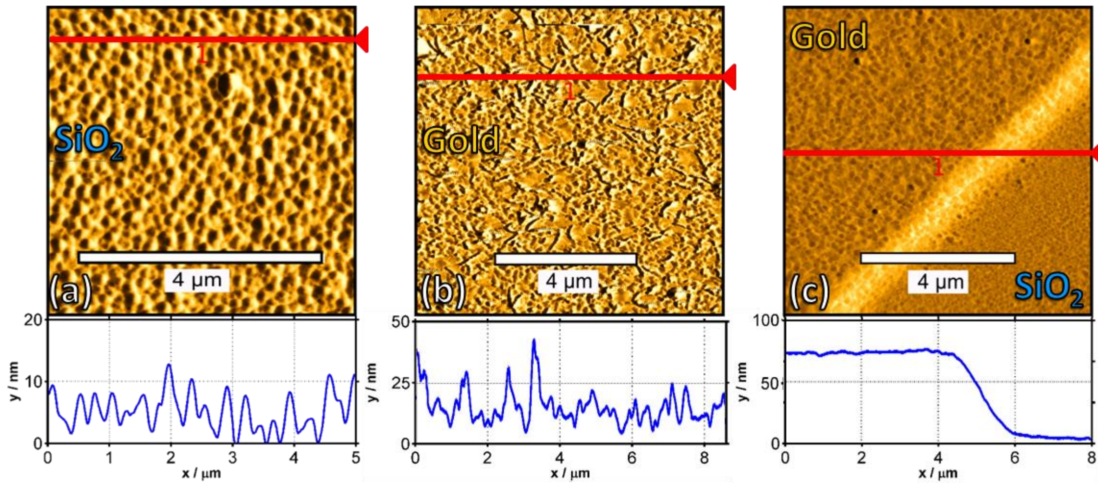


Figure 6.6: Pentacene deposited at 200 K: 1.5 monolayers on (a) SiO_2 and (b) gold, as well as (c) 7.5 monolayers on the gold contact-channel transition region. The corresponding cross sections are indicated in the AFM scans by a line and shown underneath.

In **Figure 6.7** AFM images of 1.5 ML (equivalent to 2.4 nm) of pentacene in the channel and in the gold contact region, as well as 7.5 ML (12 nm) in the transition region, all deposited at 300 K, are depicted. For the room temperature deposition on SiO_2 a Stranski-Krastanov like growth mode was observable [108] (**Figure 6.7 (a)**), characterized by the full development of the first monolayer of standing molecules before transitioning into a more island-like layer form, again featuring the characteristic step heights of approximately 1.6 nm, equivalent to the long pentacene axis. The excellent calibration of the deposition system for low coverages and the accompanying small margin of error for actual layer thickness evaluations became evident by the congruence of the second layer area in **Figure 6.7 (a)** with the nominally deposited layer thickness of 1.5 full monolayers. This allowed clear conclusions to be drawn from the differences in the onset of transistor behavior for different growth regimes. At this elevated temperature, impinging molecules can diffuse over a larger distance than at 200 K and overcome diffusion and Ehrlich-Schwoebel barriers more easily [109,110]. This led to a decrease in the total number of the now dendritic islands and the preferable accommodation of molecules at the energetically favorable edges of existing islands, which were then accessible by diffusion and up- and down-hopping between island layers [111].

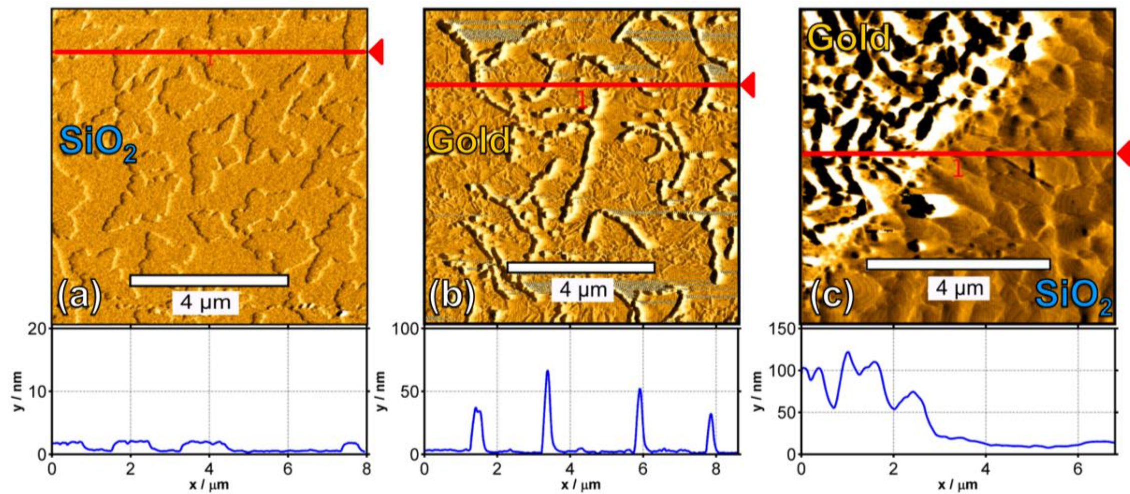


Figure 6.7: Pentacene deposited at 300 K: 1.5 monolayers on (a) SiO_2 and (b) gold, as well as (c) 7.5 monolayers on the gold contact-channel transition region. The corresponding cross sections are indicated in the AFM scans by a line and shown underneath.

For growth on gold at 300 K distinguished, several µm long and comparably high island structures composed of flat-lying molecules (**Figure 6.7 (b)**) were observable and followed once more the growth patterns reported by Käfer *et al.* [151]. The very different island structures on SiO_2, consisting of strongly cascaded islands with monomolecular steps of standing pentacene molecules played a significant role for island growth in the channel-contact transition region (**Figure 6.7 (c)**). With the increased diffusion at 300 K, compared to 200 K deposition, more pentacene molecules were able to escape the energetically unfavorable transition region. The molecules then tended to incorporate into the existing structures on either the gold or the silicon dioxide, inhibiting the smooth layer formation in the transition region observed at 200 K. Following the formation of one full wetting layer between the two gold contacts, characterized by the onset of transistor behavior at about one monolayer (**Figure 6.2**), a further closing of layers in the transition region with increasing coverage was delayed. This led to an ongoing rise in the virtual charge carrier mobility up to coverages of over 50 nm.

6.3.2 Pentacene Deposition at 350 K

For coverage dependent mobility measurements on the Unsputtered + C surface at 350 K sample temperature the recorded mobility values were still more than a factor 10 below those of the layers of comparable thickness on the Sputtered + C system

described in the previous chapter [44]. The shape of the coverage dependent mobility curve showed a very pronounced double saturation behavior (**Figure 6.2**). The 350 K layer reached a very early and strongly pronounced first mobility saturation around a pentacene coverage of 6 – 8 nm, indicating 4 – 5 fully closed layers within the Debye length in the channel region [39]. This was attributed to the increase in molecular mobility with increasing temperature [20], usually facilitating a more layer by layer like growth of the pentacene in the channel region and the formation of larger, well-ordered crystals, entailing a lower number of grain boundaries. In **Figure 6.8 (a)** an AFM image for a film of 7.5 ML pentacene, deposited onto the SiO_2 channel region at 350 K, is displayed. While the 200 K layers showed a very high number of small grains (**Figure 6.6 (a)**) and the 300 K film featured the characteristic and often reported terraced mounds **(Figure 6.7 (a))**, the 350 K film displayed very large, well-ordered islands with little cascading and associated islanding and a large number of fully closed layers underneath the visible islands, as can be seen in the corresponding cross section (**Figure 6.8 (a)**). The higher coverage of 7.5 ML, compared to the 1.5 ML depicted for 200 K and 300 K, had been selected to display the uniformity in layer formation for a wide coverage range. On the gold contacts (**Figure 6.8 (b)**), large island structures formed on top of closed layers, which were once more most probably composed of flat lying pentacene molecules since the morphology closely followed the reported structures by Käfer *et al.* [151].

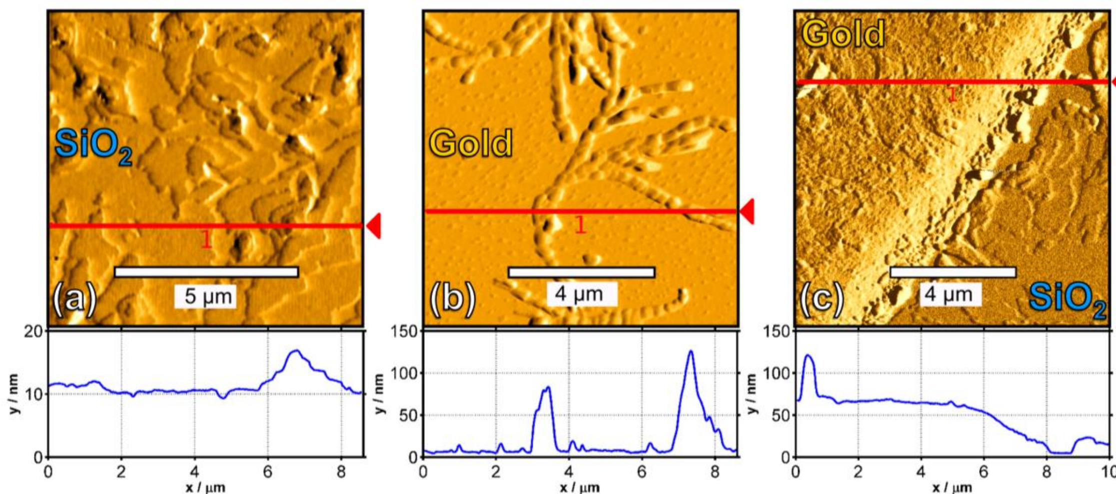


Figure 6.8:. Pentacene deposited at 350 K: 7.5 monolayers on (a) SiO_2, (b) gold and on (c) the gold contact-channel transition region. The corresponding cross sections are indicated in the AFM scans by a line and shown underneath.

The transition region from the channel area onto the gold contacts showed the well-ordered layer formation on the SiO_2, as well as rather smooth layers with a few very high islands on the gold contacts (**Figure 6.8 (c)**). One would generally expect an increase in charge carrier mobility in a 350 K film compared to the same layer thickness deposited at 200 K and 300 K through the superior layer structure and the general temperature dependence of the mobility [44]. However, the SiO_2-Au transition region seemed to be an energetically very unfavorable region for pentacene growth in this sample configuration and the deciding factor for the maximum attainable mobility for elevated temperature deposition. The formation of distinct trenches took place at the edge of the channel-contact transition, as can be seen in the corresponding cross section under **Figure 6.8 (c)**. Apparently, the increased temperature allowed the molecules not only to diffuse over larger distances, but also to overcome Ehrlich-Schwoebel barriers for up-hopping onto existing islands and the partial formation of double layers [111]. This resulted in a delay in the onset of transistor behavior to around 2.5 nm of pentacene coverage, almost twice the coverage necessary for percolation at 200 K and 300 K (inset in **Figure 6.2**). At higher coverages, this dewetting in the transition region counteracted the superior conductivity of the inner channel structure within the Debye length. Thus, the advantage of well-ordered pentacene films in the channel region due to high temperature deposition could only be utilized to its full extent once the gold contact was sufficiently connected to the active semiconducting layer. Therefore, a pentacene coverage of approximately 120 nm was necessary for the 350 K layer to fully overtake the 300 K layer in performance.

6.4 Coverage-Dependent Mobility on Sputtered Samples

Following the measurements on the Unsputtered + C surface, the same sample was then used for investigations on pentacene growth and electrical performance on sputtered SiO_2 and gold. **Figure 6.9** shows the output and transfer curves for the highest recorded mobility measured for a 96 nm thick pentacene layer deposited at 350 K onto the sputtered surface. The outliers in the low U_{GS}-regime stem from the measurement limits of our characterization system of approximately 0.1 nA. The mobility evolution as a function of pentacene coverage on the sputtered sample surface for all three temperature regimes and an inset depicting the onset of the transistor behavior are displayed in **Figure 6.10**. Sputtering is generally assumed to increase surface roughness and therefore decrease the diffusion of particles on the surface [158]. On the other hand,

depending on the material system, the removal of contaminations can lead to an increase in diffusion. As no significant surface roughening of the very smooth SiO_2 surface through the relatively low-intensity sputtering could be registered with our AFM setup, an increase of diffusion probability could be assumed [129].

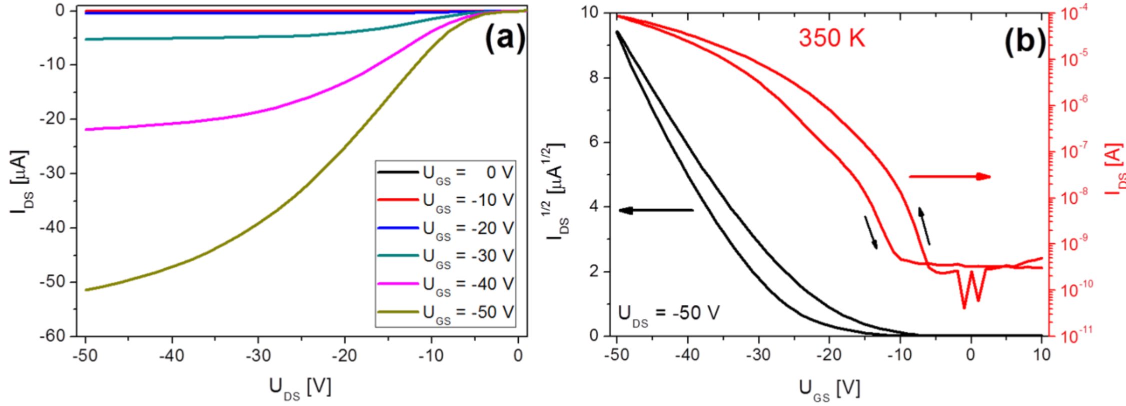


Figure 6.9: (a) Output and (b) transfer characteristics of a 96 nm thick pentacene film on a sputtered surface, deposited at 350 K and measured at 300 K sample temperature. Channel width and length are 4 mm and 25 µm, respectively.

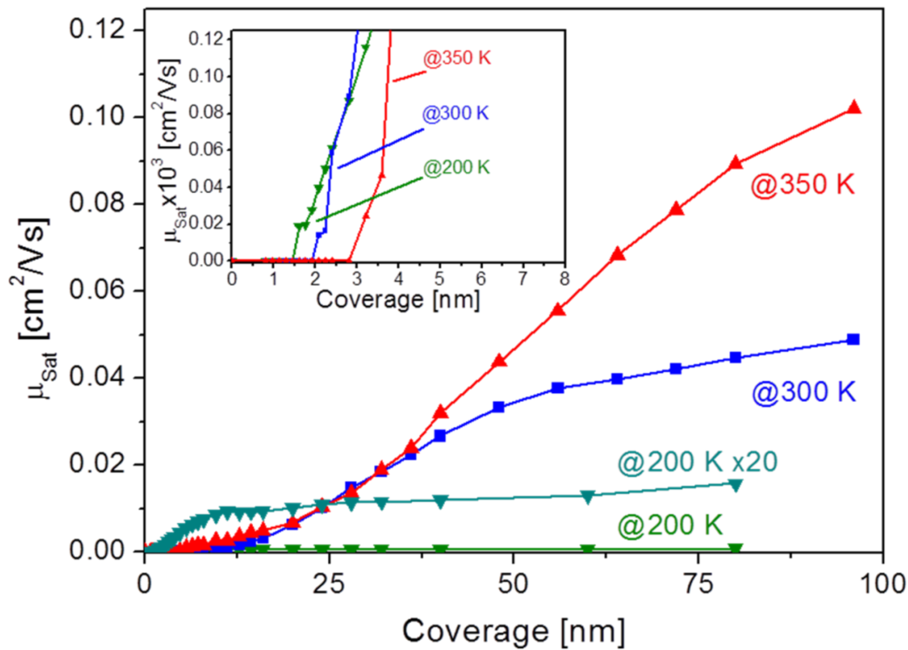


Figure 6.10: Saturation mobility μ_{Sat} as function of coverage for pentacene films on a sputtered SiO_2 surface prepared and measured at 200 K (including x20 magnification), 300 K and 350 K, respectively. The inset shows the onset of transistor behavior in the very low coverage regime.

As expected from the previous discussions, the increase in diffusion led to a trend of an even more delayed onset of transistor functionality for the sputtered samples. Only

the 200 K experiment demonstrated no change in onset behavior from the sputtering process, once more showing first percolation at approximately 1.5 nm of pentacene coverage.

The coverage necessary for the first percolation increased from approximately 1.2 nm to 2 nm of pentacene coverage for the 300 K deposition and from about 2.5 to 3 nm for the 350 K measurement in comparison to the unsputtered samples. The reason for this behavior was the above described tendency to form double layers instead of monomolecular wetting layers by up-hopping when the diffusion probability is sufficiently high [111]. In **Figure 6.11 (a)**. a detailed AFM analysis of this region for the critical transition coverage of 2.5 ML just below the percolation threshold for the sputtered 350 K configuration is depicted. From the absence of transistor functionality at this coverage and the corresponding cross section it was concluded that the darkest area in **Figure 6.11 (a)** close to the gold electrode indeed had to be the silicon dioxide surface, since the deposited amount of material wouldn’t suffice to form a third underlying layer. Thus, virtually no contact between the pentacene layer and the gold contact area existed. In **Figure 6.11 (b)** an analysis of a similarly prepared film with a coverage of 7.5 ML (sputtered sample, 350 K temperature) in the mid-channel region also showed the described up-hopping behavior, leading to the preferred formation of double layers for the lowest observable plane even for thicker layers, as depicted by the measured step height of two standing pentacene molecules (3.2 nm) for the lowest layer in the corresponding cross section.

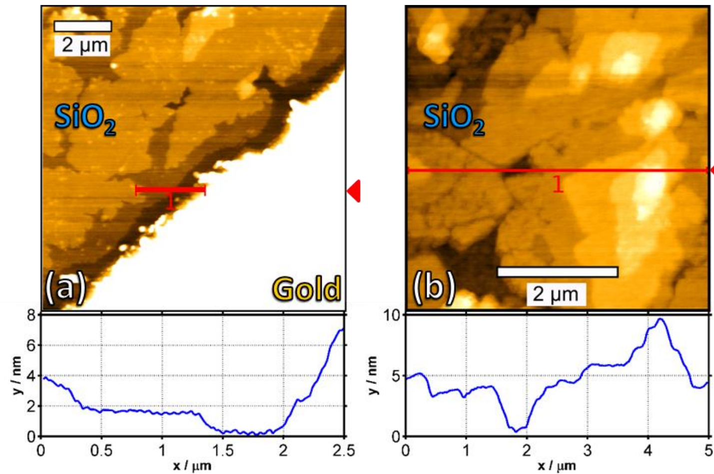


Figure 6.11: Topography scans of2.5 monolayers of pentacene on (a) the gold contact-silicon dioxide channel transition region and (b) 7.5 monolayers of pentacene on SiO_2, both deposited onto sputtered surfaces at a sample temperature of 350 K. The corresponding cross sections are indicated in the AFM scans by a line and shown underneath.

As described in section 6.3.2, an increase in maximum attainable charge carrier mobility from the reduction of the total number of grain boundaries was expected for all preparation temperatures on the sputtered samples. The analysis of the electrical data proved this claim and indicated a rise of the saturation mobility by factors of 5 to 10 for all temperature settings (mind the difference of one order of magnitude in the mobility axis scaling between **Figure 6.2** and **Figure 6.10**). Nonetheless, the dewetting processes in the channel-contact transition region were so strongly developed for those samples, that no complete saturation in mobility with increasing coverage took place up to pentacene layer thicknesses of 96 nm for all three processing temperatures.

6.5 Coverage-Dependent Threshold Voltages

Next to the mobility, the threshold voltage (U_{Th}) is a transistor parameter of very high interest. Defined as the voltage for *appreciable* drain-source current flow [19], U_{Th} had to be extracted in order to employ our selected method of saturation mobility calculation (see chapter 2.2.2 and 2.2.3). As displayed in **Figure 6.12**, the threshold voltage generally displayed rather early saturation behavior with increasing coverage, especially compared to some of the connected results for delayed mobility saturation. This could be explained with the aforementioned 3 - 4 full monolayers of pentacene channel coverage being responsible for the vast majority of the charge transport between the electrodes. Once a sufficient level of gate voltage is reached, the channel

fully opens and all accessible charge carrier transport sites within the Debye length can contribute to the transport. For layer configurations featuring a very uniform growth and therefore low access resistance towards the gold electrodes, the threshold voltage and the mobility saturated at a coverage representing approximately 4 fully closed monolayers, as can be observed for the measurements at 200 K sample temperature (**Figure 6.2** and **Figure 6.10**).

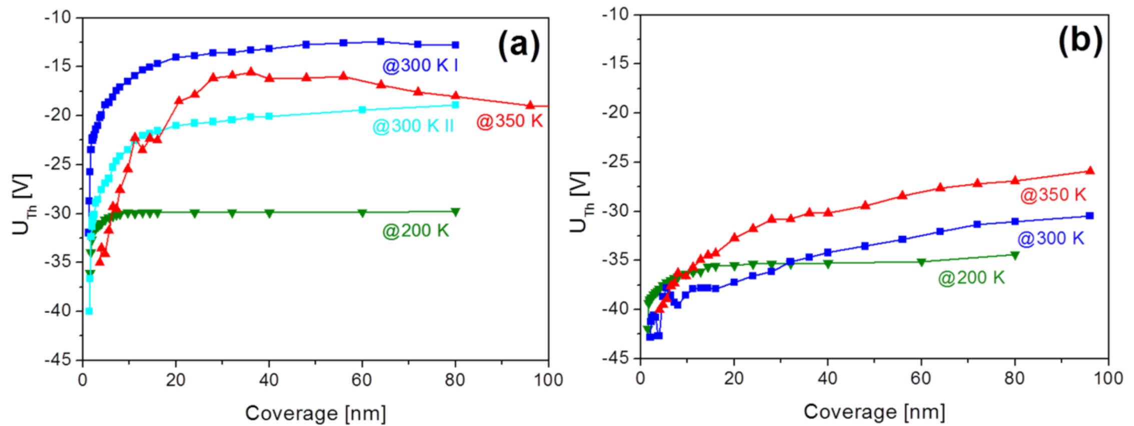


Figure 6.12: Threshold voltage U_{Th} as function of coverage for pentacene films on (a) an Unsputtered + C and (b) a Sputtered SiO_2 surface, prepared and measured at 200 K, 300 K and 350 K, respectively.

For samples with a delayed formation of closed layers in the gold electrode-SiO_2 channel transition region a larger influence of the contact resistance was observable (S-shape of the output curves in **Figure 6.9 (a)**) [69]. Layers on the SiO_2 inside the channel still fully closed, leading to a saturation of the threshold voltage at the aforementioned coverage of 3 – 4 monolayers, representing the Debye length. A further, *virtual* increase of mobility with pentacene coverage, as observed for all measurements at 300 K and 350 K (**Figure 6.2** and **Figure 6.10**), was then attributable to the closing of layers in the SiO_2-Au transition region.

The general threshold voltage curve shape as a function of pentacene coverage is governed by the density of trap states in the layer. Deep hole trap states related to the semiconductor-dielectric interface influence the starting point for conduction and were responsible for the lowest values of U_{Th} to be found at low coverage, since a more negative gate voltage was necessary in order to attract enough charge carriers to the dielectric surface to fill the traps and allow conduction between source and drain. According to Fiebig *et al.* [36] and as seen in our previous evaluations [44], the rise in threshold voltage with increasing coverage could be attributed to the formation of

electron traps in the pentacene film and especially on its surface. These traps led to a negative charging of the film and counteracted the deep-hole traps. This effect leveled off at higher coverage, where the surface shape related traps had no direct influence on the electrically conducting layers at the bottom of the film, which were closest to the gate electrode. Therefore, above sufficient pentacene coverage, the threshold voltage should remain nearly constant with increasing coverage. This saturation behavior was most obvious for the 300 K and 350 K layers on the Unsputtered + C sample and for both 200 K films. For the sputtered sample at 300 K and 350 K an ongoing slight increase in threshold voltage with pentacene coverage was observable, attributed to the introduction of new traps states through the Ar^+-ion bombardment.

Nonetheless, the major sputter influence was a uniform threshold voltage decrease compared to the Unsputtered + C sample. This was probably caused by a shift in the electrostatic potential due to the incorporation of Ar^+-ions in the channel area. In turn, this led to a screening of the gate potential, requiring stronger negative gate voltages in order to achieve the same charge attracting field and therefore shifts of the threshold into the negative direction. By heating the sample to temperatures above 650 K, Ar^+-ions that had been implanted in the surface near region could be degassed prior to pentacene deposition, as shown by thermal desorption spectroscopy. Indeed, this led to an upward shift in the threshold voltage. This opened up the possibility of influencing the threshold voltage in a controlled way via argon implantation and therefore the adjustment of the threshold voltage to specific application needs. Specifically designed experiments performed in our system have shown stable and reversible shifts of the threshold voltage through argon sputtering and annealing processes. Since the focus of this work was on the layer formation and morphology as a function of coverage and growth conditions this special feature was not covered in further detail.

6.6 Optimized Pentacene Growth and Experimental Conclusion

In the previous sections, the pentacene layer growth within the channel and in the SiO_2-Au transition region, as a function of deposition temperature and sputter controlled carbon surface contamination, had turned out to be the major area of interest for optimizing the semiconductor growth in the experimental system. The demonstration of the sample temperature dependent layer growth mode on the Unsputtered + C samples in **Figure 6.6**, **Figure 6.7** and **Figure 6.8** depicts the entire transition from the uniform growth of small islands at 200 K (**Figure 6.6 (c)**), through the strongly cascaded growth

at 300 K (**Figure 6.7 (c)**), up to the formation of the largest and most well-ordered islands with the detrimental SiO_2-Au transition region dewetting at 350 K (**Figure 6.8 (c)**). A corresponding representation of the sputter influence on the layer growth mode and island density is depicted in **Figure 6.13**.

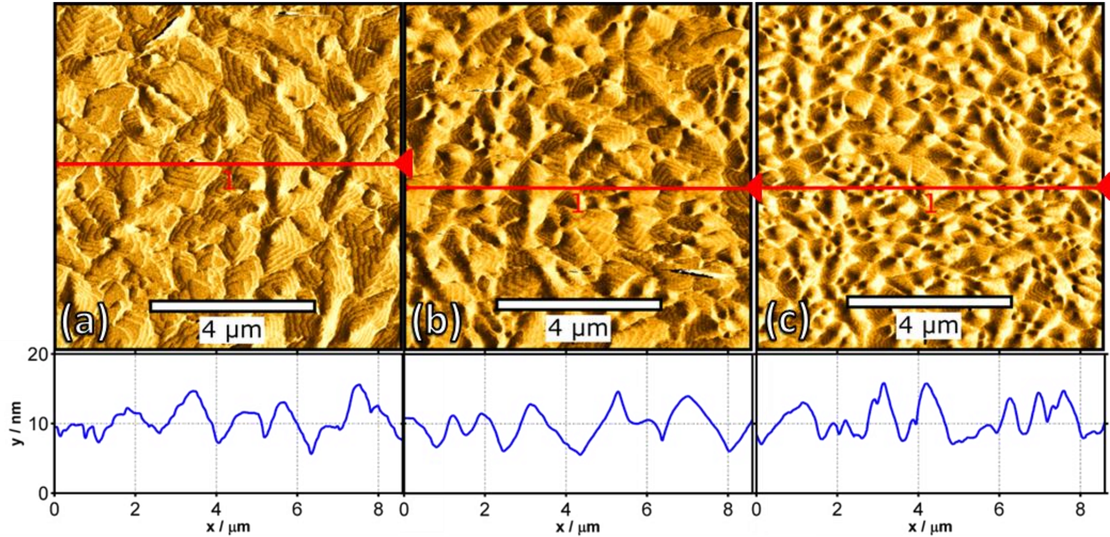


Figure 6.13: 7.5 monolayers of pentacene on (a) a sputtered, (b) Sputtered + C and (c) Unsputtered + C SiO_2 sample, all deposited at 300 K surface temperature.

The sample temperature of 300 K had been chosen to be the most representative one, based on the pronounced sputter influence on layer growth mode in **Figure 6.10** and the corresponding largest shift in mobility onset. The AFM evaluations showed excellent agreement with our investigations on diffusion dominated layer growth. From the largest, most well-ordered and cascaded islands on the Sputtered sample in **Figure 6.13 (a)**, a clear transition to higher island density on the Unsputtered + C sample was observable (**Figure 6.13 (c)**). The Sputtered + C sample, as analyzed in the previous chapter [44], depicted a film morphology in between those two configurations (**Figure 6.13 (b)**). According to the abovementioned considerations, the approximate island number density increased from about 1.5 islands per μm^2 on the Sputtered, to 3 islands per μm^2 on the Sputtered + C sample and 7 islands per μm^2 on the Unsputtered + C sample. At the same time, the average island base size decreased from about 1 µm (**Figure 6.13 (a)** to less than 0.6 µm (**Figure 6.13 (c)**).

With this gathered information one could then return to the question of optimized layer growth for our pentacene transistors. Most research groups employ various forms of surface cleaning and elevated surface temperatures to improve the pentacene layer growth [20]. One factor of importance is the often comparably high total pentacene

layer thickness deposited. This puts the system into the high temperature-high coverage regime, where the best performance results have been achieved in the scope thesis as well (**Figure 6.10**). On the other hand, this neglects the influence of the highly critical SiO_2-Au transition region for the bottom-contact configuration, which might be the dominant factor for the large variation in saturation mobility values as a function of coverage reported in literature, ranging from 3.2 nm to over 150 nm [30,34,36,41–43]. Therefore the layer thickness is of fundamental interest when it comes to the selection of the optimal processing temperatures. As it often is the case in semiconductor physics, the tendency to make layers as thin as possible is a major factor in device design and fabrication. The charge transport takes place in only the first few monolayers within the Debye length [39,40]. For thinner layers this implies that, through an improved contact to the electrodes, the low surface temperature growth regime, in spite of the inferior layer quality in the channel, can result in an increase in performance compared to higher temperature layers, featuring the originally better inner layer structure. Following our investigations on sputtered and unsputtered systems a mixed layer system on a sputtered substrate was proposed, consisting of a thin 350 K film to form a well-ordered conducting layer in the channel region, covered by a thin 200 K film. This ensures a low number of grain boundaries for high mobility in the channel and a uniform coverage and electrode connection in the SiO_2-Au transition region. The result of this experiment, compared to non-mixed layers of equivalent coverage, is shown in **Figure 6.14**.

The combination of 4 ML (6.4 nm) of pentacene deposited at 350 K (i) and covered with another 4 ML at 200 K (ii) displayed the expected qualities. While a 8 ML (12.8 nm) film deposited at 350 K gave a mobility of about 0.004 cm^2/Vs, the deposition of 4 ML at 350 K and additional 4 ML at 200 K resulted in a mobility increase by a factor of four to approximately 0.016 cm^2/Vs. The mixed layer configuration was fully stable at room temperature and the 200 K layer showed no dewetting over time in this temperature range. Additional 4.5 ML deposited at 300 K sample temperature then only increased the mobility in the range expected from previous 300 K investigations.

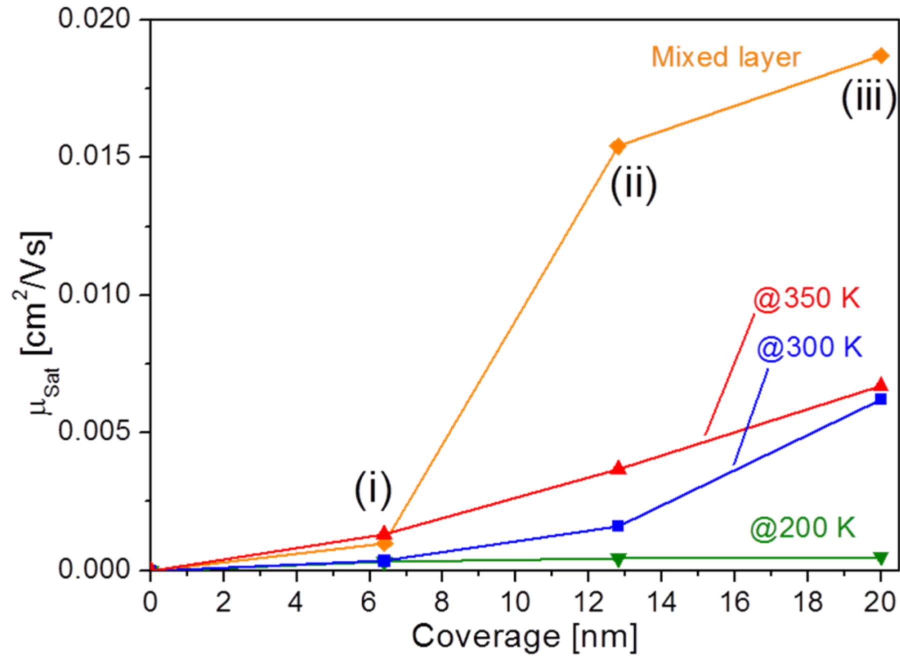


Figure 6.14: Coverage dependent saturation mobility μ_{Sat} for 200 K, 300 K, 350 K and mixed temperature layers on a sputtered sample. The mixed layer represents (i) 4 monolayers (6.4 nm) at 350 K, (ii) additional 4 monolayers at 200 K and finally (iii) 4.5 additional monolayers at 300 K.

6.7 Chapter Summary and Conclusions

In extension of our previous work on *in situ* fabrication and characterization of silicon/silicon dioxide bottom-gate, gold bottom-contact pentacene transistors devices on carbon covered and sputter-cleaned samples, at three different surface temperatures during deposition of 200 K, 300 K and 350 K, were prepared and analyzed. The unique sample setup allowed precise temperature control, as well as the repeated desorption of pentacene off the sample surface, enabling all of the coverage dependent mobility evaluations to be performed on only a single sample, ensuring maximum comparability of the obtained results. It was possible to achieve conclusive insight into the primary parameters affecting the pentacene layer growth, namely the growth temperature during layer formation and the surface contamination through carbon residues. The newly acquired data supports the model of a gradual transition in growth mode and related transistor performance from 200 K to 350 K as well as from growth on carbon covered to sputter-cleaned samples. Electrical evaluations showed a rise in the maximum attainable mobility and an increase of the required layer thickness for the first percolation through sputtering for all temperatures, attributed to an increase in surface diffusion.

In combination with AFM and threshold voltage analysis, it was shown that the formation of the active layer and electrode contact is mainly governed by a surface temperature and treatment induced variation in the prevalent diffusion probability during the semiconductor deposition process. While a high diffusion probability increased the conductivity in the channel, due to a reduced number of grain boundaries and a better molecular ordering in the grains, increased dewetting in the contact – channel transition region counteracted this benefit.

With the acquired knowledge a particular deposition sequence on a sputtered sample was designed, featuring 4 ML of pentacene deposited at 350 K as the conducting layer within the channel with the most optimal charge transport properties, followed by a 4 ML capping layer deposited at 200 K sample temperature, ensuring optimal connection of the active layer to the gold electrodes. The mixed layer configuration was stable at room temperature and the 200 K layer showed no dewetting in this temperature range. With this preparation method a considerable increase in charge carrier mobility was achieved compared to all other single deposition temperature processes on sputtered samples.

7 EPINDOLIDIONE OTFTS

7.1 Introduction

The successful integration of organic materials into established inorganic semiconductor systems and technologies has proven to be one of the largest driving forces in research and development for the last decade [1]. Characteristics, such as, low material cost and weight, room temperature deposition, and patterning for flexible substrates, as well as economical large area fabrication techniques, can all be found in these materials [2,8].

One of the most promising approaches for commercial success is the integration of already mass produced organic semiconductors into electronic systems. This led to the investigations of Głowacki *et al.* on the organic pigment epindolidione ($C_{16}H_{10}N_2O_2$, inset in **Figure 7.1**), which is present in everyday applications such as the yellow pigment in printer inks and closely related to the already industrially mass produced indigo [4,55–57]. A large variety of the properties wanted in an optimal organic semiconductor can be found in epindolidione, such as a sufficiently large attainable charge carrier mobility [55], possible ambipolar behavior, high air, water and temperature stability, and excellent biocompatibility and degradability [57]. With all these required qualities present, the goal of mass-produced eco-friendly, light and last but not least inexpensive organic electronics could to be attainable with hydrogen-bonded organic pigments such as the here investigated epindolidione.

This chapter is in large parts based on a publication in the journal Synthetic Metals (Paper III, Ref. [46]), to which I have contributed as the leading author.

7.2 Film Preparation and Surface Characterization

Same as in the previous two chapters on pentacene OTFTs, the conducted experimental work was based on the characterization of 1 cm×1 cm model OTFT devices *in situ* under a base pressure of approximately 2×10^{-8} mbar. In order to create these samples, highly p-doped silicon wafer pieces with a 150 nm thick dry-oxide layer were plasma etched for cleaning, before 60 nm thick gold contacts were deposited through a shadow mask. This yielded SiO_2 bottom-gate, gold bottom-contact transistor samples with a 4 mm wide (W) and 25 µm long (L) channel structure, which were then contacted *ex situ* and installed into the sample holder. The physical vapor deposition (PVD) of epindolidione from a Knudsen cell was performed through a 4.5 mm×2.5 mm aluminum foil shadow mask in order to limit the deposition to the active channel area.

The sublimation purified epindolidione material was synthesized at the JKU Linz and supplied by the group of Sariciftci *et al*, following the procedure by Jaffe and Matrick [159] and considerations by Kemp *et al.* [160]. The high thermal stability and poor solubility of H-bonded organic semiconductors, attributed to the strong intermolecular interactions based on H-bonds and π-π stacking, limit the application of solution processed deposition and makes vacuum deposition the most applicable method [161–163].

The wide temperature range attainable by the experimental setup, as described in chapter 4.2.1, permits thermal desorption spectroscopy (TDS) and a subsequent re-deposition of new epindolidione layers for reproducibility evaluations. Argon-ion sputtering has been used for sample surface cleaning and Auger electron spectroscopy (AES) allowed analysis of the sample surface in-between cleaning and semiconductor deposition steps.

7.3 Calibration of the Deposition System for Epindolidione

The parameters for the quartz microbalance controlled Knudsen cell deposition could not be found in literature and had to be approximated. In order to use the deposition system as described in chapter 4.1.2, the density of epindolidione ρ was estimated to be approximately 1.5 g/cm^3 while a long molecular axis length of 1.26 nm was assumed for all epindolidione experiments. These estimations could subsequently be verified by X-ray diffraction (XRD) and *ex situ* atomic-force microscopy (AFM) investigations. On the quartz microbalance, which was covered by thick layers of

epindolidione, a sticking probability of one could be assumed for impinging epindolidione molecules, resulting in a correlation of quartz resonance frequency change and nominal epindolidione layer thickness d of 1 Hz ≈ 0.083 nm. To attain sufficient precision for the deposition of thin layers a comparably low deposition rate of approximately 0.1 ML/min was employed throughout all experiments.

7.4 Dielectrics and Electrical Characterization

The investigated dielectrics have been introduced in chapter 4.2.2 and included untreated SiO_2 at substrate temperatures of 200, 300 and 350 K during deposition, as well as sputtered SiO_2 and the organic capping layers PVCi and PNDPE at substrate temperatures of 300 K. The organic capping layers were employed in order to increase the performance potential for the epindolidione OTFTs by reducing the polarity of the SiO_2 surface [55–57]. SiO_2 still represented an experimental system of high interest, since it still is one of the most easily available material systems for semiconductor experiments and features a very well-established and studied surface configuration [142,143]. The electrical characterization of epindolidione OTFTs was once more performed according to the methods described in chapter 2.2.

7.5 Thermal Desorption Spectroscopy

In the planar transistor geometry implemented in most OTFTs, the layer formation and growth kinetics of the active organic layer, in this case epindolidione, are highly critical for the ensuing transistor performance. Only a comparably low number of closed monolayers above the gate dielectric are known to actively contribute to the majority of the charge transport, signifying the Debye length for the material system [164]. This aspect has been thoroughly investigated for the model organic semiconductor pentacene in the literature and in the previous chapters [34,36,39,40,42,45], but so far not been investigated in detail for the class of H-bonded organic semiconductors. Thermal desorption spectroscopy (TDS) enables the analysis of adsorption and desorption kinetics and the calculation of binding energies from the crucial low coverage regime up to the bulk phase. Therefore, insight into the thermal stability of the charge transporting layer could be gained by employing this method.

In order to perform TDS, the cracking pattern of epindolidione from our specific quadrupole mass spectrometer (QMS) had to be known. This had previously not been investigated and therefore no literature data on epindolidione cracking could be

obtained. **Figure 7.1** shows the main cracking masses observed for epindolidione stemming directly from the Knudsen cell effusion flux. The process in order to establish the optimal cracking mass is detailed in chapter 4.1.1 and followed the same procedure as for pentacene. In contrast to **Figure 4.4**, for clarity reasons here only one out of the approximately 20 cycles recorded during the corresponding TDS measurement is shown. For evaluation and display purposes, the prominent cracking mass *m* of 103 amu was selected, as it featured the best signal to noise ratio for the setup.

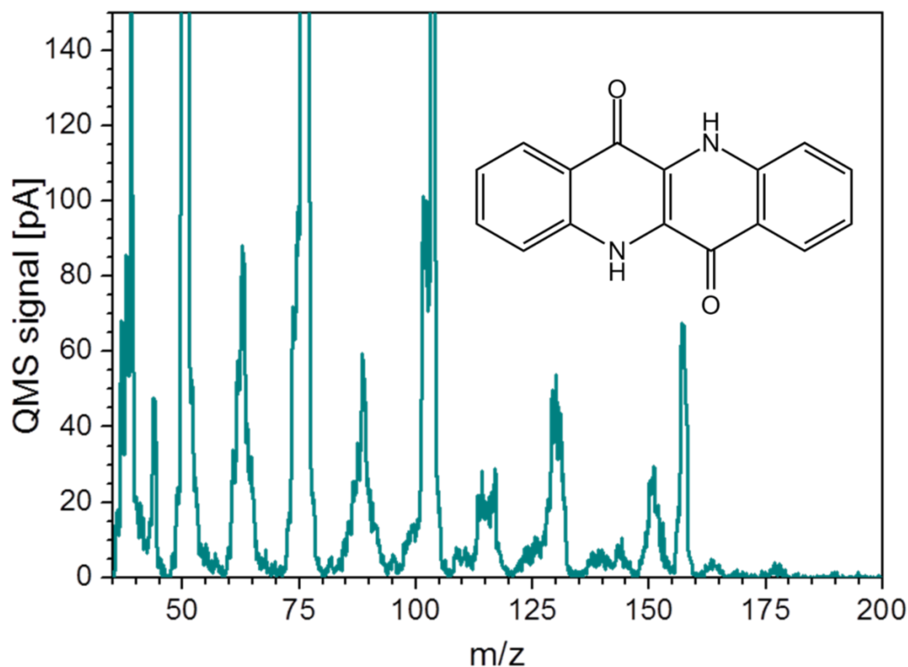


Figure 7.1: Cracking pattern of epindolidione in the quadrupole mass spectrometer. In the inset, the molecular structure of epindolidione is shown.

Figure 7.2 shows a series of TDS measurements for epindolidione on an untreated SiO_2 surface. Similar results were obtained for desorption from sputtered and carbon-covered SiO_2, as well as from gold and PNDPE surfaces. The displayed temperature has been corrected to account for the lag between the temperature measurement on the sample holder backside and the sample surface, as described in detail in chapter 4.2.1. This yielded information on the temperature limits for stable epindolidione adsorption and transistor operation, and was applied in the subsequent growth and electrical characterization experiments.

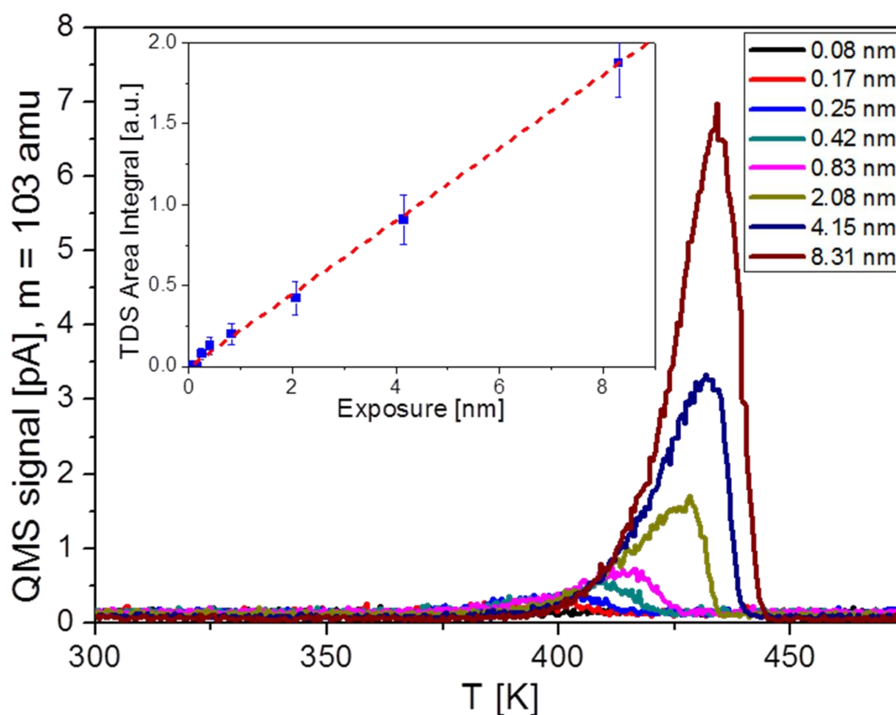


Figure 7.2: Thermal desorption spectra from the SiO_2 surface for different epindolidione film thicknesses deposited at 300 K substrate temperature. Heating rate $\beta = 1$ K/s. In the inset, the correlation between TDS area and epindolidione exposure is shown. The abscissa shows the corrected temperature.

The desorption spectra demonstrate clear zero-order desorption behavior, characteristic for multilayer desorption [119]. No second desorption peak in the low coverage regime could be found, which would be indicative for the formation of an subjacent, more strongly bound wetting layer of flat-lying molecules. Pure multilayer desorption from islands could therefore be assumed for all epindolidione coverages. The inset in **Figure 7.2** depicts the correlation between the exposure, as monitored by the quartz microbalance (impinging amount), and the area under the desorption spectra registered by the QMS (adsorbed amount). The linear relationship indicates that the sticking coefficient is constant for the full range of coverage investigated, it is therefore reasonable to assume that the sticking coefficient is unity for these coverages.

With the desorption rate, R, and the molecular surface density of one full layer of standing epindolidione, $N_{ML} = 4.34\times10^{14}$ molecules/cm^2, the desorption energy, E_{Des}, and the frequency factor, ν_0, for epindolidione desorption could be extracted from the TDS data according to the considerations in chapter 3.1 [113]. The calculated desorption energy amounted to $E_{Des} = 1.83 \pm 0.05$ eV and the frequency factor to $\nu_0 = 1\times10^{21\pm1}$ s^{-1}. The desorption energy and the peak desorption temperature of 435 K,

for an 8 nm thick layer, correlated well with results obtained for comparable molecules with the same layer thickness. For example, pentacene [151] and quinacridone [65] showed desorption energies of 1.65 eV and 2.1 eV, respectively. The obtained high frequency factor aligns with similar results for other large organic molecules [119,165,166]. This feature is related to the vast difference in the number of vibrational and rotational degrees of freedom between the free and adsorbed state for large organic molecules, especially compared to the desorption of single atoms or small molecules, where the frequency factor amounts to values of about 10^{13} s^{-1} [115,167].

In contrast to the results obtained for pentacene, which is known for its tendency to form a full 'wetting layer' of standing molecules on SiO_2 with a subsequent formation of terraced mounds (quasi Stranski–Krastanov growth) [108,154,156], epindolidione displayed pure island-growth (Volmer-Weber growth) with no explicit tendency to close the first ML before second layer formation begins. In **Figure 7.3**, a low-coverage AFM analysis of the transition from 0 to 2.5 ML of epindolidione coverage is shown for **(a)** an untreated and **(b)** a carbon-covered SiO_2 surface, which depicts the aforementioned Volmer-Weber growth mode. The carbon-covered surface was obtained by repeated epindolidione adsorption and desorption cycles. The gradient in coverage stemmed from the surface shadow masking by the sample mounting washers during the epindolidione deposition, as can be seen in **Figure 4.11 (c)**. Even at very low coverage, islands higher than one standing epindolidione molecule formed on both surface types.

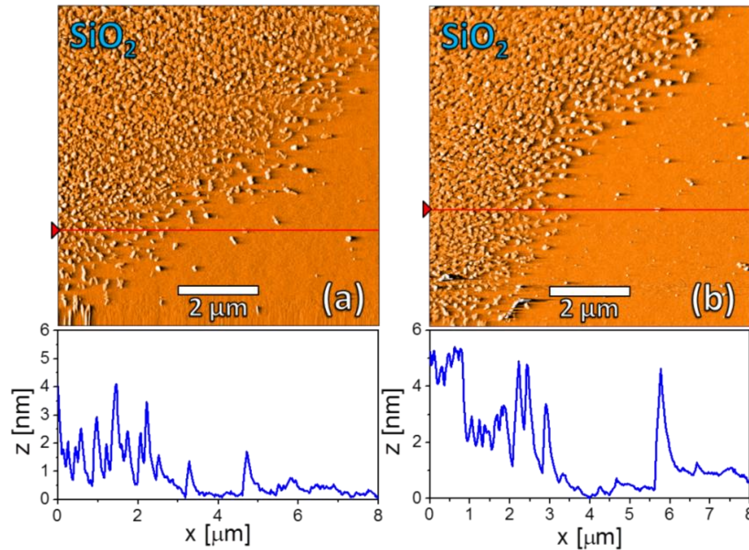


Figure 7.3: AFM images of the shadowing induced transition from 0 to 2.5 monolayers of epindolidione coverage, deposited onto (a) untreated and (b) carbon-covered SiO_2. The corresponding cross sections are indicated in the AFM images by a red line and shown underneath.

7.6 Electrical Evaluation

In situ electrical measurements were done on bottom-gate, gold bottom-contact epindolidione transistors for a range of substrate temperatures and gate dielectrics. A set of representative transfer curves for thick epindolidione layers on the four investigated dielectrics (untreated and sputtered SiO_2, PVCi, and PNDPE) is shown in **Figure 7.4**. These representative curves highlight many of the fundamental differences the choice of gate dielectric entailed. All transfer curves showed significantly higher negative threshold and onset voltages than observed for pentacene in our previous work [44,45], which was attributed to the increased sensitivity of the H-bonded semiconductor to the polar dielectrics. All of the investigated surface preparations and dielectrics exhibited significantly different charge transport properties. While the untreated SiO_2 samples displayed the lowest hysteresis (**Figure 7.4 (a)**) and a threshold voltage dependence of the charge carrier mobility, visible in the $I_{DS}^{1/2}$ plot, the less polar surface attributed to the organic capping layers yielded the desired quadratic current to voltage ratio, apparent in the linearity of the $I_{DS}^{1/2}$ plots in **Figure 7.4 (c)** and **Figure 7.4 (d)**. A sputter induced shift of the threshold voltage to more negative values and an increase in hysteresis, as well as the highest charge carrier mobility, were observed on sputtered SiO_2 (**Figure 7.4 (b)**) and could be related to sputter beam implanted Ar^+-ions in the

dielectric, as described in chapter 6.5 for pentacene [45,168]. Nonetheless, sputtering offered the most reproducible surface conditions.

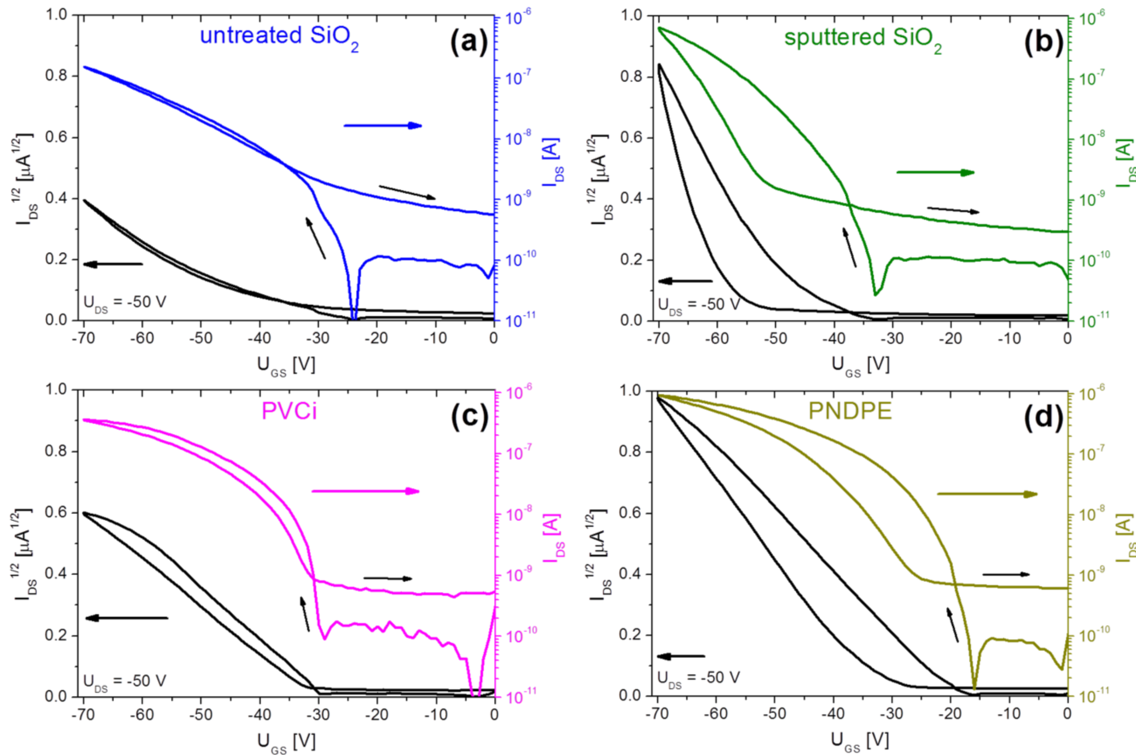


Figure 7.4: Transfer characteristics of (a, b, d) 62 nm and (c) 100 nm thick epindolidione films on (a) untreated SiO_2, (b) sputtered SiO_2, (c) PVCi, and (d) PNDPE dielectrics in bottom-gate bottom-contact configurations, deposited and measured at 300 K sample temperature. Channel width and length are 4 mm and 25 µm, respectively.

7.6.1 Coverage-Dependent Charge Carrier Mobility

The key experiment of this chapter was once more the analysis of the evolution of extracted transistor parameters, namely the saturation mobility, μ_{Sat}, and threshold voltage, U_{Th}, as a function of increasing epindolidione layer thickness. **Figure 7.5** shows the extracted charge carrier mobilities as a function of epindolidione coverage for different dielectrics and surface configurations in the low (0 - 10 nm, **Figure 7.5 (a)**) and high (0 - 62 nm, **Figure 7.5(b)**) coverage regime. The primary point was to determine the onset of transistor behavior through the formation of the first paths of percolation of current between the source and drain electrodes (**Figure 7.5(a)**), as well as the maximum attainable mobility and the curve shape of the mobility evolution (**Figure 7.5 (b)**).

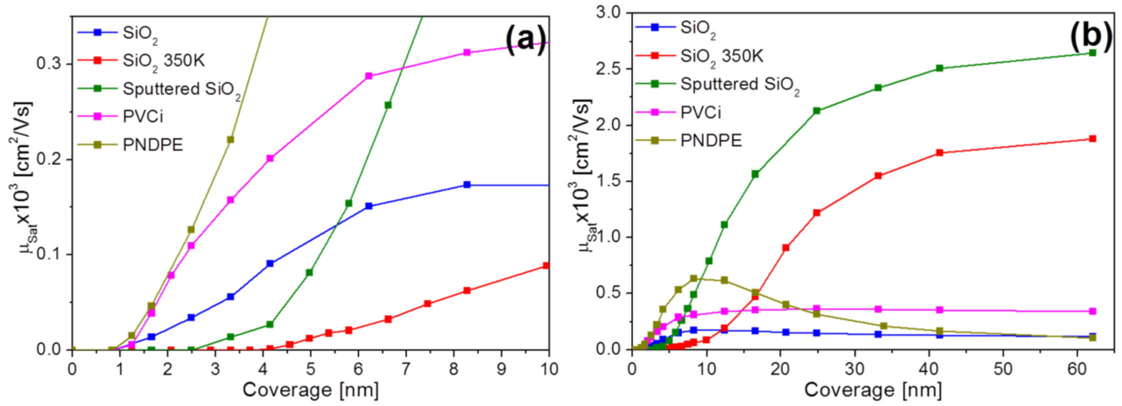


Figure 7.5: Saturation mobility, μ_{Sat}, as a function of coverage in the (a) low and (b) high coverage regime for epindolidione films in bottom-gate bottom-contact configurations on different dielectrics. All films were measured and prepared at 300 K, if not stated otherwise.

The Volmer-Weber growth mode of epindolidione resulted in a first percolation of current at coverages of approximately 90% to 95% of one full standing ML (1.26 nm) on untreated SiO_2, PVCi, and PNDPE. This represents a significant delay compared to the 75% of a full ML required for charge transport in the quasi Stranski-Krastanov growth of pentacene reported in chapter 6 [45]. The percolation behavior could be modified by tuning the diffusion-governed island growth, for example by increasing the substrate temperature or by sputter removal of atmospheric carbon contamination stemming from the *ex situ* sample handling. In **Figure 7.6**, AFM images of 0.8 nm thick epindolidione layers (65% of one full ML) deposited onto SiO_2 at different sample surface temperatures are shown.

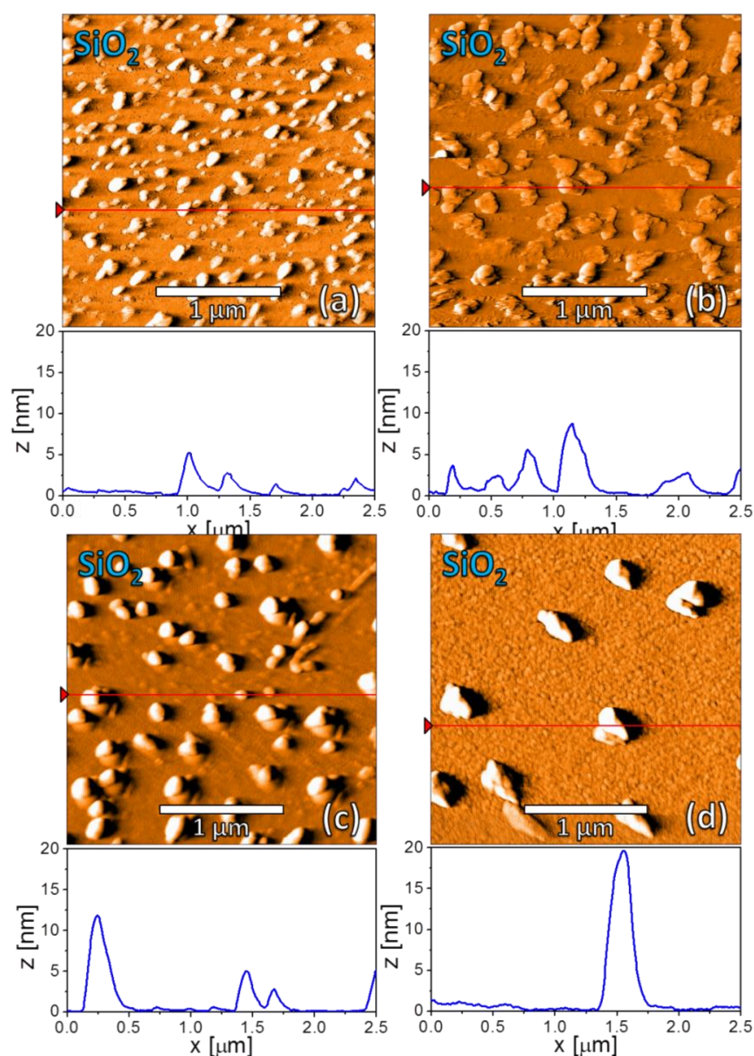


Figure 7.6: AFM images of 0.8 nm thick epindolidione layers (65% of a full monolayer) deposited onto SiO_2 at sample surface temperatures of (a) 200 K, (b) 300 K, (c) 350 K and (d) 375 K. The corresponding cross sections are indicated in the AFM images by a red line and shown underneath.

A clear correlation between the SiO_2 surface temperature during deposition and number and height of islands was observed. The direct increase in maximum island size by about 5 nm per evaluated temperature step from 5 nm to 20 nm is displayed in the cross sections in **Figure 7.6**. At the same time the island number density decreased from about 40 islands per μm^2 at 200 K, to 20 islands per μm^2 at 300 K, 10 islands per μm^2 at 350 K and finally only about 1.5 islands per μm^2 at 375 K. Compared to low and room temperature deposition, higher temperatures increased the surface diffusion probability for the impinging molecules and enabled them to overcome Ehrlich-Schwoebel barriers for up-hopping with greater ease [109–111]. In agreement with results for pentacene in chapter 6, sputter treatment caused a similar effect of increasing diffusion probability

for the adsorbing molecules through the removal of diffusion-inhibiting surface contaminants. The ensuing formation of a lower number of higher islands delayed the percolation threshold for drain-source current, which is directly related to the ongoing connection of islands between the contacts, to over 2.5 ML (3 nm) for the sputtered sample and 3 ML (4 nm) for the 350 K sample (**Figure 7.5(a)**). For the epindolidione system, the increased diffusion inherently led to the formation of larger crystallites with improved molecular ordering in the channel area (**Figure 7.6**), which reduced the total number of grain boundaries and, therefore, the number of necessary grain boundary transitions in the current flow between source and drain. Accordingly, the highest attainable mobilities in the high coverage regime were observed for the sputtered SiO_2, as well as for the 350 K sample temperature deposition (**Figure 7.5(b)**). Sputtering also yielded a highly reproducible surface configuration, which was not attainable to the same extent on the other surfaces. Sputtered SiO_2 samples averaged the highest maximum saturation mobility of around 2.5×10^{-3} cm^2/Vs, closely followed by the average of 1.7×10^{-3} cm^2/Vs on 350 K samples. PVCi and PNDPE surfaces led to mobilities at high coverage comparable to untreated SiO_2 and maximum mobility values of 1.5 - 3.5×10^{-4} cm^2/Vs, with the added benefits of a more quadratic current to voltage behavior and lower threshold voltages (**Figure 7.4**). The mobility remained below the values of up to 1.5 cm^2/Vs reported by Głowacki et al. [55–57] and the 0.04 cm^2/Vs by Yang et al. [58]. This discrepancy in maximum mobility of an order of magnitude and more is explainable by the inferior charge carrier injection and therefore attainable performance for bottom-gate OTFT geometries and the advantageous non-polar and/or aliphatic dielectrics employed in these contributions [14,59]. A similar ratio of previously reported top-contact (≈ 1 cm^2/Vs) to then measured bottom-contact mobilities (≈ 0.1 cm^2/Vs) had been found in our studies on pentacene in the chapters 5 and 6. Nonetheless, the gold bottom-contact setup enabled investigations on the otherwise inaccessible *in situ* evolution of charge carrier mobility as a function of coverage. This yielded information on the effective Debye length in the films and the number of fully closed and charge contributing layers [34,39,40].

In contrast to the earlier investigations on pentacene in the previous chapters, no significant transistor operation could be achieved for low temperature deposition with a 200 K sample temperature and for deposition onto SiO_2 covered with carbon from an epindolidione desorption step. The low temperature layer displayed an irreversible phase transition, which was therefore not observed by *ex situ* room temperature AFM

and XRD measurements, to a semiconducting phase at a device temperature of approximately 280 K, as will be discussed in the section on temperature-dependent mobility and threshold voltage. For the carbon-covered surface, no apparent differences in layer growth could be discerned by AFM (**Figure 7.3)** and XRD investigations. It is believed that, due to the decomposition of epindolidione on the gold contacts during the deposition process, the work function of the gold surface is changed to such an extent, that the injection barrier becomes too high for a reasonable charge injection into the semiconductor.

On the other hand, no indication of the diffusion-promoted dewetting effects present for pentacene devices at the gold contact-channel transition region was found [45]. **Figure 7.7** depicts AFM images of this region for epindolidione coverages of 2.5 ML on SiO_2 and 1.3 ML on PNDPE. The uniform coverage in the transition region is representative for all of the investigated gate dielectrics and sample surface temperatures during epindolidione deposition.

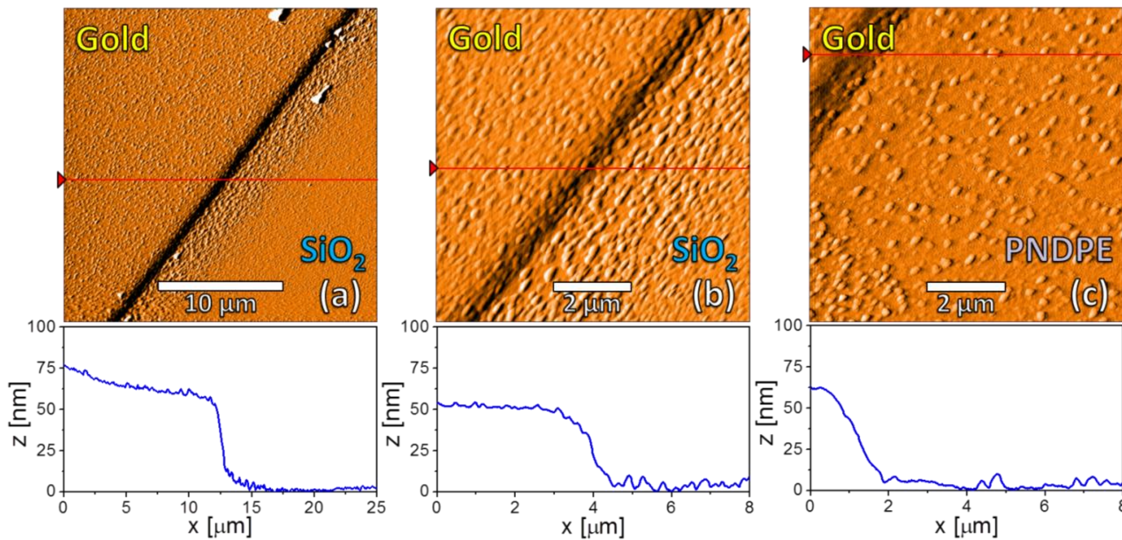


Figure 7.7: AFM images of (a, b) 2.5 monolayers and (c) 1.3 monolayers of epindolidione deposited onto the gold contact-channel transition region at 300 K for the gate dielectrics (a, b) SiO_2 and (c) PNDPE. The corresponding cross sections are indicated in the AFM images by a red line and shown underneath.

None of the epindolidione measurements displayed the pronounced double saturation behavior of mobility as a function of coverage, which is characteristic for strong dewetting effects, as observed for pentacene deposition at higher sample temperatures and on sputtered samples in chapter 6. Traceable to the Volmer-Weber growth of a comparably low density of multilayer islands, the delay in the saturation of

mobility with coverage for the sputter treated and heated samples could in this case be attributed to the continuous closing of layers within the Debye length in the whole channel region. As a result, the sputtered and the 350 K samples showed an apparent increase in mobility up to coverages of over 30 ML (40 nm), (**Figure 7.5 (b)**). The difficulties that arise with the filling of deep trenches between islands are well documented in the literature [92].

For the untreated SiO_2 and the PVCi, as well as PNDPE-capped samples, a more even layer growth and an earlier saturation of the coverage-dependent mobility, starting at approximately 5 - 6 full closed monolayers, was observed. This could in turn be assumed to be the upper limit for the Debye length in the investigated epindolidione transistor system.

When compared to the significant temperature-related changes observed for pentacene growth [45], epindolidione features a rather stable growth mode of a large number of relatively small crystallites on all substrates. **Figure 7.8** shows AFM images of 5 ML of epindolidione grown at SiO_2 sample temperatures during deposition of 300 K **(a)** and 350 K **(b)**. The topography images yielded a root mean square average of height deviation of about 1 nm to 2.3 nm between the 300 K and 350 K sample and the cross sections display the higher corrugation of the films prepared at 350 K. Nonetheless, these values are small compared to the complete changes in morphology observed for pentacene as a function of substrate temperature during layer growth. The variation of the substrate material or surface sputter treatment also showed only subtle changes in the topography of the films. On the other hand, the electrical measurements revealed significant differences in the absolute values of the mobilities and their coverage dependence. Apparently, even the subtle changes of the film morphology and molecular arrangement in the islands, which cannot be observed *via* AFM, can crucially affect charge transport properties.

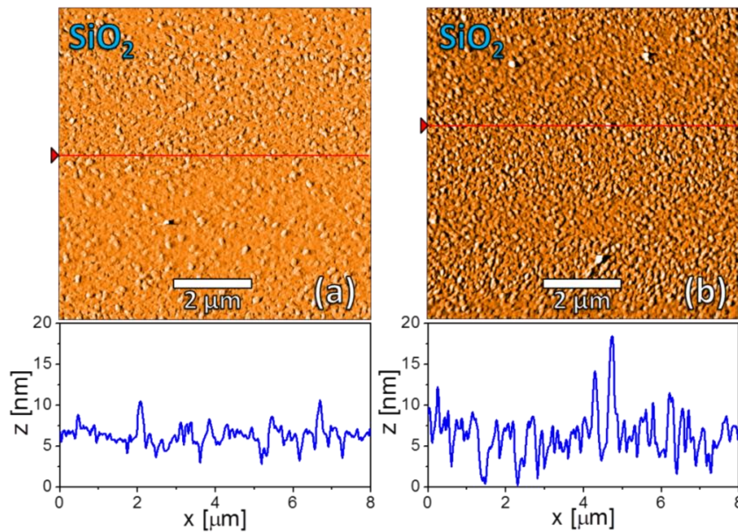


Figure 7.8: AFM images of 5 monolayers of epindolidione grown on SiO_2 at a sample surface temperature during deposition of (a) 300 K and (b) 350 K. The corresponding cross sections are indicated in the AFM images by a red line and shown underneath.

Finally, we want to comment on the noticeable decrease in charge carrier mobility with increasing coverage exceeding the first saturation for the PNDPE-capped dielectric and, to a lesser extent, the untreated SiO_2 and PVCi-capped dielectric. This was in fact not a coverage-dependent effect, but rather a time-related property. Coverage-dependent mobility measurements on PNDPE samples, where the deposition had been halted as soon as mobility saturation was reached (5 - 6 ML), have shown an asymptotic decrease and subsequent stabilization in mobility within three hours of waiting time at about 10% of the originally observed maximum value. This behavior was attributed to a time-dependent transition from a thin-film phase, where the molecules are standing upright and consequently exhibit optimum intermolecular coupling, into a bulk phase, where the molecules are slightly tilted. Even such a slight tilting of the molecules away from the upright standing position in relation to the dielectric surface can significantly alter the π-π stacking between neighboring molecules and therefore affect the charge transporting properties, as observed for pentacene [80,81]. A possible explanation for the differing prevalence of this effect for the various dielectrics and surface treatments investigated could be a layer stabilization through surface interactions with the dielectric. This would explain the present case, where the least polar and lowest surface energy dielectric (PNDPE) showed the strongest change over time, while the highly reactive sputtered SiO_2 surface fully stabilized the epindolidione layer, with the untreated SiO_2 and PVCi-capped surfaces falling in between those two extremes. For the experiments featuring a sample temperature during epindolidione deposition of

350 K a better ordered and more stable layer formation could be assumed to take place, yielding results that are comparable to those on the sputtered SiO_2 surface.

7.6.2 Coverage-Dependent Threshold Voltage

The threshold voltage, U_{Th}, has been extracted from linear extrapolations in $I_{DS}^{1/2}$ vs. U_{GS} plots (**Figure 7.4**), according to the formalism described in chapter 2.2.2 and by Street *et al.* [69]. In order to average out hysteresis effects, a linear fit was performed between the highest current point and the gate-source voltage where the current drops to two thirds of the maximum value. For each gate-source voltage in this range, the mean value of the current between the forward and backward measurement was considered for the linear extrapolation. **Figure 7.9** shows the threshold voltage as a function of epindolidione layer thickness for a set of surface dielectric configurations. Generally, the coverage dependence of the threshold voltage is governed by trap states in the layer and at the dielectric interface. The filling of deep hole trap states at the dielectric-semiconductor interface is responsible for the most negative U_{Th} values to be found in the very low coverage regime, where a higher negative gate voltage is necessary in order to produce a sufficient number of mobile charge carriers. The initial fast rise of the threshold voltage with coverage is in turn attributed to deep electron traps in the bulk and/or at grain boundaries. These coverage-related electron trap states counteract the deep hole traps at the gate dielectric interface. At higher coverage, when the mean thickness of the film exceeded the Debye length, the influence of these trap states leveled off [36]. This leveling process is a material property of the organic semiconductor and its grain boundaries and is largely independent of the gate dielectric material or surface temperature during deposition (**Figure 7.9**).

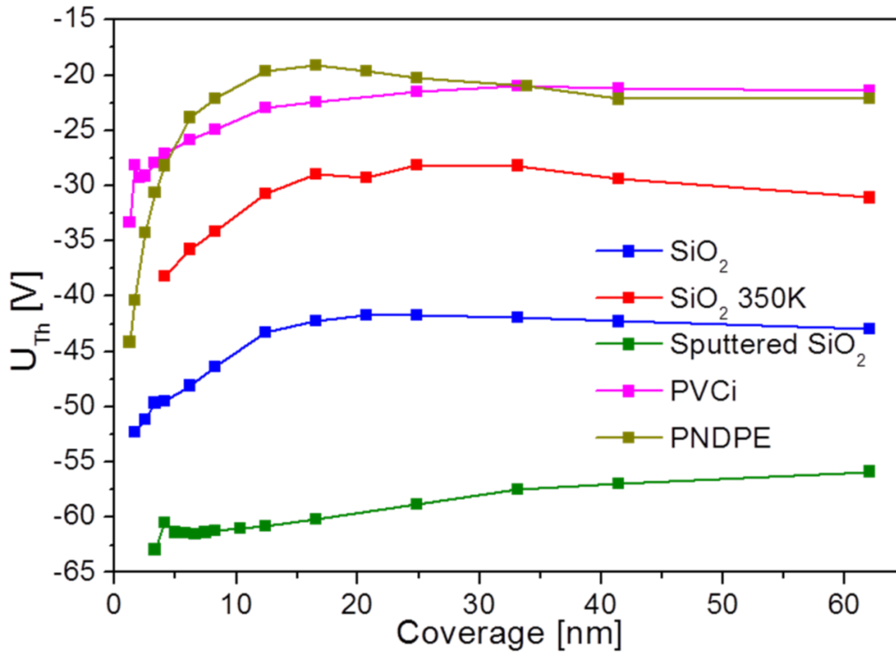


Figure 7.9: Threshold voltage, U_{Th}, as a function of coverage for epindolidione films in bottom-gate bottom-contact configurations on different dielectrics. All samples were prepared and measured at 300 K if not stated otherwise.

The differences in the absolute values of U_{Th} for the investigated dielectrics and surface configurations are explainable by dielectric surface induced effects. The high polarity of the SiO_2 surface, especially compared to the PVCi and PNDPE-capped dielectrics, led to a negative shift in the threshold voltage. While the comparably high number of trap states on the untreated SiO_2 surface was further enhanced by the sputtering process, entailing the large hysteresis observed in **Figure 7.4**, the implanted Ar^+-ions also acted as a screening potential for the gate and caused an additional uniform shift to more negative U_{Th} values. Unfortunately, no further information on the density and implantation depth of the Ar^+-ions could be obtained. For the 350 K samples, an improved molecular ordering and the formation of larger crystallites entailed a lower number of grain boundaries and therefore grain boundary-related trap states, leading to a scenario in-between those of the untreated SiO_2 surface and the organic capping layers. The decrease of U_{Th} above a certain coverage for the PNDPE-capped sample could again be traced back to a restructuring effect, as described above.

7.7 Temperature-Dependent Electrical Properties

In order to gain deeper insight into the charge transport properties and mechanisms of epindolidione the precise temperature control capabilities offered by the experimental setup were utilized. This allowed the saturation mobility and threshold voltage to be monitored as a function of device temperature in the range of 120 - 400 K. **Figure 7.10** plots the logarithm of the charge carrier mobility, μ, against the inverse temperature, $1/T$, for epindolidione layers with a thickness of 62 nm. The layers were deposited at a sample temperature of 200 K and 300 K for untreated SiO_2 and at 300 K for the sputtered SiO_2 surface. The order of heating and cooling steps is indicated by numbers and arrows next to the graphs.

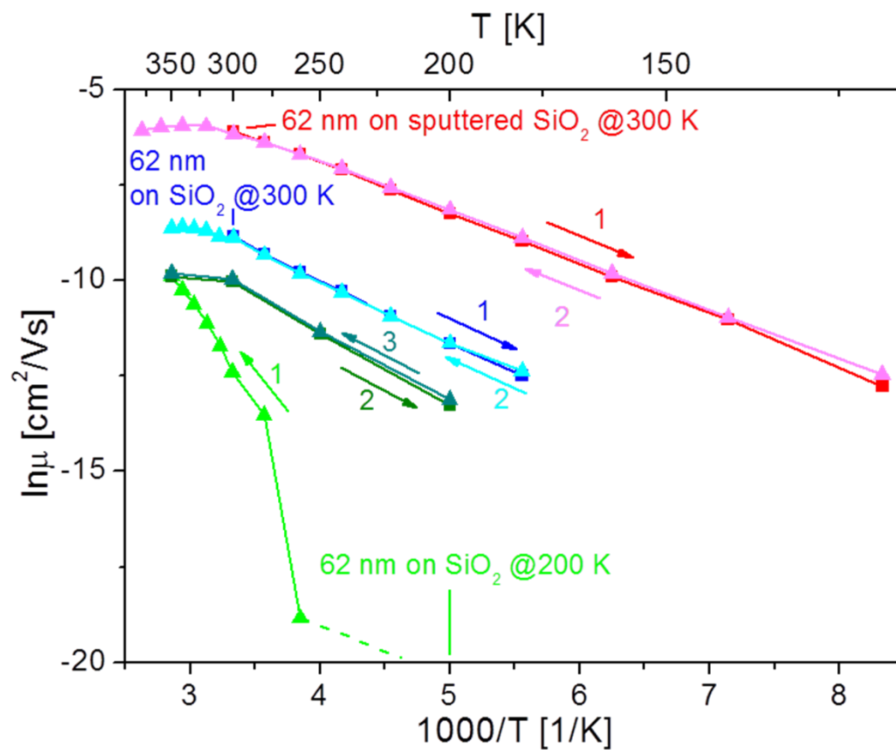


Figure 7.10: Temperature dependence of the saturation mobility for 62 nm thick epindolidione layers deposited onto untreated SiO_2 at 200 K (light and dark green) and 300 K (blue and cyan), and on sputtered SiO_2 at 300 K (red and pink). The order of heating and cooling steps is indicated by the numbers and arrows.

Both room temperature layers were fully stable in their morphology and yielded reversible mobility values for cooling and subsequent heating between 120 K and 350 K. At temperatures lower than 180 K, the formalism for mobility analysis was only applicable for the sputtered sample, since the temperature-dependent source-drain current for the untreated SiO_2 sample dropped to values too low to guarantee

meaningful parameter extraction. The 200 K layer showed no measurable charge transport until it was heated to 280 K. The data in **Figure 7.10** suggests an ongoing, irreversible change in layer morphology and/or structure taking place between 280 K and 350 K. Subsequent cooling and heating cycles yielded linear and reversible mobility behavior as a function of temperature, comparable to results of the room temperature samples. Interestingly, and contrary to the results obtained for pentacene, the mobility slightly decreased with temperature above 320 K. This is attributed to an ongoing rise in phonon scattering events with sample temperature for the moving charge carriers in the epindolidione crystallites. This behavior has been reported previously for highly ordered organic crystals with band like charge transport [169], most notably for the epindolidione-related quinacridone [143].

The thermal activation energy, E_A, for the charge transport can be derived from the ln μ vs. $1/T$ plot by a linear least-squares fit of the shown Arrhenius type behavior. A detailed explanation of the theory and the evaluation methods involved can be found in the literature [13,85] and in chapter 2.2.1. E_A combines a number of temperature-related effects, namely the promotion of charge carriers trapped in localized states into the delocalized band for conduction according to the multiple trapping and thermal release model (MTR) [13], the thermionic hopping of charge carriers between the individual epindolidione grains [83], as well as charge injection and contact-resistance-related effects at the semiconductor-contact metal interface. Due to the comparably low mobilities, contact resistance effects should play only a minor role as the transport is dominated by the properties of the organic film in the channel.

According to $\mu \propto exp(-E_A/k_BT)$, the activation energy, E_A, could be calculated as 110 ± 10 meV for the film on the sputtered SiO_2 sample, 140 ± 10 meV for the film grown on untreated SiO_2 at 300 K, and 160 ± 10 meV for the film grown at 200 K. In agreement with the lower recorded mobilities, these values were larger than the thermal activation energies obtained for pentacene ($E_A \approx 100 \pm 10$ meV) and compared to the values of $E_A \approx 130$ meV reported for quinacridone [143], which featured similar mobility values of around $1.5{\times}10^{-3}$ cm^2/Vs, albeit in a top-contact configuration.

Additional information on the charge transport in epindolidione can be obtained from the temperature-dependent threshold voltage. In **Figure 7.11**, the threshold voltages corresponding to the mobility values in **Figure 7.10** are plotted against the device temperature. For the untreated SiO_2 sample surface, similar tendencies as for the mobility were observed. Starting at a temperature of 280 K, a meaningful threshold

voltage could be extracted for the layers deposited at 200 K, which then also showed the irreversible morphological and/or structural change up to 350 K. Further heating and cooling for both the untreated SiO_2 samples, prepared at 200 K and 300 K, then showed full reversibility when it comes to the temperature-dependent mobility, which also followed the same slope. The higher negative U_{Th} values with decreasing temperature are explainable by the mobility edge model [44,91], where the temperature influences the density of occupied hole states that extend into the bandgap through the shape of the involved Fermi-Dirac distribution. With increasing negative gate voltage, the Fermi level is moved closer towards the hole conduction band and more and more deep trap states are filled, until, at the threshold voltage, mobile shallow trap states and states in the delocalized band are accessed and a current can flow. A higher temperature entails a broader Fermi-Dirac distribution and therefore requires a less negative gate voltage in order to fill the deep trap states and enable conduction.

The results for the sputtered sample surface were very different in nature, since the threshold voltage was nearly constant between 120 K and 300 K and even decreased slightly at higher temperatures. The addition of the Ar^+-ions seems to effectively pin the threshold voltage to very negative values. Currently this behavior is not explainable.

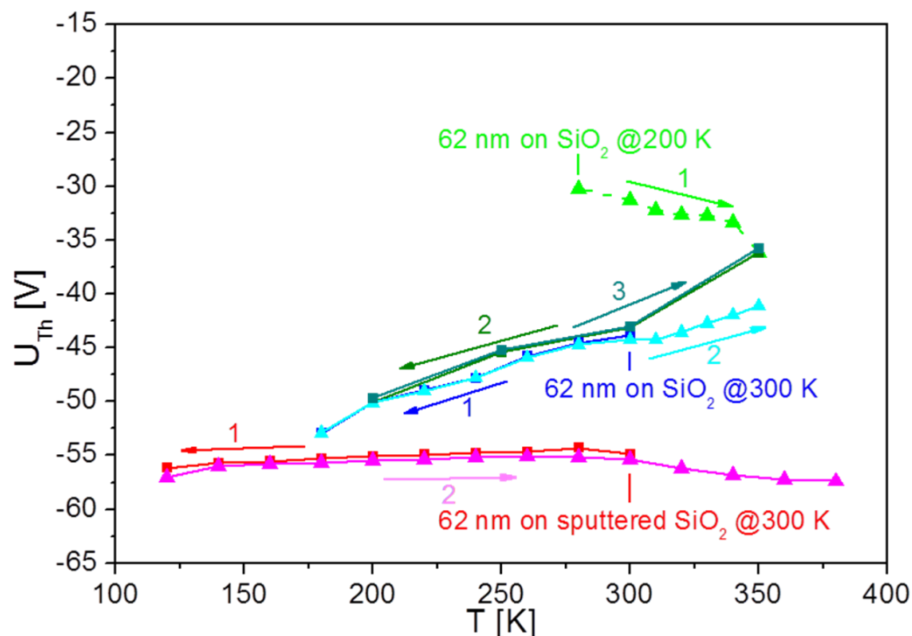


Figure 7.11: Temperature dependence of the threshold voltage for 62 nm thick epindolidione layers deposited onto untreated SiO_2 at 200 K (light and dark green) and 300 K (blue and cyan) and sputtered SiO_2 at 300 K (red and pink). The order of heating and cooling steps is indicated by the numbers and arrows.

7.8 Chapter Summary and Conclusions

The device characteristics of bottom-gate, bottom-contact epindolidione OTFTs were studied *in situ* under controlled UHV conditions as a function of layer thickness and sample temperature, for various gate dielectrics. *Ex situ* AFM was used in order to complement the *in situ* methods with information on layer formation and surface morphology. The investigated gate dielectric configurations included SiO_2, in its untreated and sputtered forms, as well as the spin-coated organic capping layers PVCi and the polynorbornene PNDPE, each displaying significantly different charge transport properties. A predominant Volmer-Weber island growth mode was found to be responsible for the comparably late onset of transistor behavior as a function of epindolidione coverage, with a required nominal coverage of 90 - 95% of a monolayer composed of standing molecules. The percolation behavior could be tuned by surface sputtering and increased sample temperatures during deposition, augmenting the surface diffusion of adsorbing epindolidione molecules and therefore facilitating the formation of a lower number of higher, better-ordered islands. In turn, this led to the highest, bottom-contact configuration, mobilities of approximately 2.5×10^{-3} cm^2/Vs for high coverages on sputtered and 350 K samples. The PVCi and PNDPE-capped SiO_2 layers showed excellent quadratic current to gate voltage behavior, but lower maximum mobilities of about 1.5 - 3.5×10^{-4} cm^2/Vs. No transistor operation could be achieved for deposition at 200 K sample temperature and for layers deposited on carbon residue covered SiO_2, produced after an epindolidione adsorption/desorption cycle.

The saturation behavior of the mobility and threshold voltage with increasing coverage could be traced to the ongoing closing of layers in the channel area. An upper limit for the Debye length of 5 - 6 ML was extracted. Additionally, time-related mobility degradation effects were observed for devices with organic dielectric capping layers, tentatively attributed to a transition from upright standing molecules at low coverage (thin-film phase) to slightly tilted molecules at higher coverage (bulk phase), which negatively influences the π-π overlap of neighboring molecules. Finally, temperature-dependent charge carrier mobility and threshold voltage evaluations were performed for devices with 62 nm thick epindolidione layers. Following an irreversible phase change at approximately 280 K for the device prepared at 200 K, all devices showed a linear and reversible relationship between the logarithm of the mobility and the inverse temperature between 120 K and 300 K. From this relationship, activation barriers for the promotion of trapped charges into the conduction band could be

deduced, ranging from E_A = 110 meV for the device prepared at 300 K with a sputtered SiO_2 dielectric to E_A = 160 meV for the device prepared at 200 K with an untreated SiO_2 dielectric.

In addition to the electrical characterization of epindolidione films, the thermal stability and adsorption/desorption kinetics of epindolidione were studied by thermal desorption spectroscopy. TDS revealed island growth behavior even at the lowest coverages, without any indication of a subjacent wetting layer. The desorption energy was calculated to be 1.83 ± 0.05 eV and the frequency factor for desorption was determined to be $1\times10^{21\pm1}$ s^{-1}. The sticking coefficient for epindolidione on SiO_2 was found to be unity, independent of the coverage.

8 SUMMARY

In the scope of this thesis, electrical and surface analytical investigations on bottom-gate, bottom-contact organic thin film transistors have been performed. The experimental methods applied included the *in situ* characterization of surfaces and transistor devices via Auger electron spectroscopy, thermal desorption spectroscopy, as well as transfer and output curves for electrical parameter extraction. Careful electric insulation ensued that the electrical characterization of devices could be performed parallel to all other *in situ* investigations, enabling a number of rarely accessible measurements. Additionally, *ex situ* atomic-force microscopy was used in order to associate layer growth dependent phenomena with the electrical results.

A distinguishing characteristic of the experimental setup was the sample holder construction, which allowed the sample temperature to be modified or kept at a constant level anywhere in the accessible range of 125 K to over 800 K. In addition to the aforementioned possibility to perform thermal desorption spectroscopy experiments and electrical characterization, this also enabled studies on the layer growth of the investigated organic semiconductors at a range of temperatures and the correlation with electrical results.

In the first experimental chapter, the fabrication of highly reproducible pentacene devices was the main focus. This set the baseline for all following more complex measurements and experiments and proved the scientific validity of the system. Through repeated deposition and desorption of pentacene onto the device surfaces, both the gold contact pads and the SiO_2 channel were intentionally contaminated with a thin carbon layer, as verified by Auger electron spectroscopy. While this surface

modification was accompanied with a reduction of the maximum attainable charge carrier mobility, devices with unprecedented reproducibility could repeatedly be established.

Further studies focused on the temperature and coverage dependency of the main electrical parameters of interest, namely the charge carrier mobility and the threshold voltage. Complementary growth mode investigations via atomic-force microscopy revealed a predominant layer like film growth at 200 K device temperature during deposition, while room temperature deposition yielded the well-known Stranski-Krastanov growth of cascaded islands. Several literature results could be confirmed for the system, such as the good applicability of the multiple trapping and release model for charge transport, as well as the mobility edge model for the temperature dependence of the threshold voltage. Additionally, the onset of transistor behavior at about 0.8 monolayer nominal pentacene thickness and the apparent Debye length of approximately 4 - 5 monolayers agreed with reported literature results.

More in detail investigations on the mobility as a function of the 200 K and 300 K layer growth modes revealed that coverage dependent mobility is strongly dependent on the present growth mode, as it fundamentally influences the closing of charge transporting layers and the grain density and ordering in the layers. Additionally, first signs of dewetting effects at the gold contact – transistor channel transition were observed, which were then covered in detail in the second experimental section.

In extension of the preliminary results on pentacene organic field effect transistors on carbon covered SiO_2, the second large experimental part focused on the optimization of transistor properties as a function of the parameters temperature and surface configuration. Growth analysis was performed on the gold contacts, the channel region and the critical transition region between those two areas. The surface temperatures during deposition of 200 K, 300 K and 350 K were analyzed and sputtered, untreated and carbon covered surfaces configurations were investigated. The unique sample setup allowed repeated desorption of pentacene off the sample surface and optional sputtering in between deposition cycles, enabling all of the coverage dependent mobility evaluations to be performed on only a single sample, ensuring optimal reproducibility and comparability between experimental results.

Through extensive atomic-force microscopy measurements, a gradual transition in growth mode as a function of temperature as well as surface carbon contamination was

found. Additionally, a direct correlation between the ease of surface diffusion and the formation of better-ordered, lower grain density films, albeit with higher and more dewetting prone islands could be established. For this reason, the highest recorded mobilities were found for thick layers of pentacene on sputtered sample surfaces accompanied by a delay in percolation through dewetting effects.

The experimental findings culminated in a specific deposition sequence, which featured 4 monolayers of pentacene deposited at 350 K sample temperature for optimal charge transport in the low grain density film and a subsequent 4 monolayer 200 K deposition for optimal electrode connection without dewetting. This mixed film considerably increased the attainable mobility compared to all single temperature deposition films of the same pentacene layer thickness and established the desired total layer thickness as an important and generally overlooked process parameter in organic field-effect transistor fabrication.

Finally, the experimental findings and accumulated experience on the measurement system were applied to the promising, up-to-date, H-bonded organic semiconductor epindolidione. Due to the more surface sensitive nature of the material in comparison to pentacene, two new organic dielectric materials, namely the spin-coated organic capping layers, PVCi and PNDPE, had been included into the established temperature, surface configuration and layer thickness dependent experiments.

In a first step, due to a lack of available literature data, preliminary cracking pattern and thermal desorption spectroscopy investigations were performed for the relatively new material system epindolidione on SiO_2, which revealed constant sticking and island formation without a subjacent wetting layer, independent of the coverage.

Atomic-force microscopy studies revealed a predominant Volmer-Weber island growth mode for epindolidione at all temperatures and dielectrics, which in turn increased the necessary coverage for percolation to 90 - 95% of a monolayer. Once more, a direct correlation between the surface diffusion and the surface treament, when it comes to contaminations in the form of carbon, as well as the surface temperature could be established: increased surface diffusion entailed a better-ordered, lower grain density films and therefore higher attainable mobilities. Due to the sensitivity of the material system to the investigated growth parameters, no operational transistors could be established on heavily carbon covered samples and for deposition at 200 K sample temperature, up to an irreversible transition to a conducting phase at approximately

280 K. The mobility evolution as a function of layer thickness could once more be traced to the ongoing closing of layers in the channel up to an upper limit for the Debye length of 5 – 6 monolayers

Additionally, time-related mobility degradation effects were observed for devices with organic dielectric capping layers, attributed to a transition from upright standing molecules at low coverage (thin-film phase) to slightly tilted molecules at higher coverage (bulk phase), which negatively influences the π-π overlap of neighboring molecules.

In conclusion, the functionality and versatility of the designed measurement setup could be shown for two highly relevant organic semiconductor systems. In the current state, the system allows reliable *in situ* characterization of any semiconductor that can be deposited via the Knudsen cell system. While the quality and extent of the AFM evaluations could surely be improved, the electrical characterization, especially in conjunction with X-ray analysis, allows conclusive investigations on new, up-and-coming materials.

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8.1 List of Conference Contributions

1) *School of Organic Electronics 2015 - poster, Como, Italy:*

   Temperature Dependent Pentacene Growth: In-Situ Transistor Fabrication and Characterization

2) *ÖPG 2015 - oral, Vienna, Austria:*

   Optimizing pentacene thin-film transistor performance: Temperature and surface configuration induced growth modifications

3) *DGP 2015 - oral, Berlin, Germany:*

   Ultra-high vacuum fabrication and characterization of organic thin film transistors: In-situ electrical and surface sensitive analysis on temperature effects and layer growth

4) *nanoFIS 2015 - oral, Graz, Austria:*

   In-situ pentacene thin film transistor fabrication and characterization: Electrical and surface sensitive analysis under ultra-high vacuum conditions

5) *ÖPG 2014 - oral, Pöllau, Austria:*

   Organic thin film transistors under ultra-high vacuum conditions: Deposition and device temperature dependent in-situ electrical and surface analytical characterization

6) *ICPS 2014 - oral, Heidelberg, Germany:*

   In-situ surface analytical and electrical characterization: A case study on pentacene thin film transistors

Authors for all above:
R. Lassnig, M. Hollerer, B. Striedinger, A. Fian, B. Stadlober and A. Winkler

7) *JVC15 2014 - oral, Vienna, Austria:*

   Surface analytical methods in conjunction with in-situ electrical characterization and performance evaluation: A case study on pentacene thin film transistors

8) *BioEL 2014 - poster, Kirchberg, Austria:*

   Pentacene thin film transistor characterization under ultra-high vacuum conditions: The combination of electrical and surface analytical methods

9) *Advanced Materials Day 2013 - poster, Graz, Austria:*
   In-situ thin film transistor fabrication: Electrical and surface analytical characterization

10) *ICSS 15 2013 - oral, Paris, France:*
    In-situ production, electrical and surface analytical characterization of pentacene thin film transistors

11) *ICPS 2013 - oral, Edinburgh, Scotland:*
    In-situ production, electrical and surface analytical characterization of pentacene thin film transistors

12) *ÖPG 2013 - oral, Linz, Austria:*
    In-situ thin film transistor fabrication: Electrical and surface analytical characterization

Authors for all above:

R. Lassnig, B. Striedinger, A. Fian, B. Stadlober and A. Winkler

13) *DPG 2013 - poster, Regensburg, Germany:*
    Initial growth of ultra-thin films of pentacene on mica: Influence of water and substrate morphology

L. Tümbek, R. Lassnig and A. Winkler

8.2 List of Seminar Contributions

1) *Doctoral School Physics - Oberseminar WS 2015 - oral, Graz, Austria:*
   Organic thin-film transistor performance optimization: Temperature and surface configuration induced layer growth

2) *Institute of Solid State Physics - Seminar SS 2015 - oral, Graz, Austria:*
   Temperature and surface modification dependent pentacene film growth: In-situ ultra-high vacuum transistor fabrication and characterization

3) *Institute of Solid State Physics - Seminar SS 2013 - oral, Graz, Austria:*
   In-situ OTFT fabrication and characterization

Authors for all above:

R. Lassnig and A. Winkler

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Additionally, the whole environment at the Institute of Solid State Physics was always extremely friendly, supportive and positive. There, especially Elisabeth as my encouraging doctoral-mother, Georg, Pachi, Andrew and Paul, with their (partially weird) humor and occasional AFM visits always brightened my days. Furthermore, Birgit, Harald and Martin definitely have to be mentioned here, who always supported me on the technical side of things.

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This being a two-page acknowledgement shows how much more support I had around me on the social side of things which made it possible for me to endure the hardships that come with a PhD.

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