Design of a Generic Low Voltage, Ultra-Low Power Sensor Interface for Wirelessly Powered ICs

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Graz, September 2013

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Abstract

Radio Frequency Identification (RFID) tags nowadays still offer very limited functionality with regard to sensing capabilities. This thesis presents various modular Wireless Sensor Nodes (WSNs) with an in itself modular Sensor Interface (SI) built in. The smallest proposed sensor node consists only of a single die of silicon with a volume of below $1\,mm^3$. Various other slightly larger implementations with extended features are also presented.

As the main topic of this thesis a generic sensor interface is discussed, which is specialized to achieve a good measurement result with a very small amount of energy that most appropriately is stored in a capacitor. Thus ultra-low power and low voltage designs of vital system components are proposed and results presented in this thesis.

Commonly, SI circuits are supplied by one or multiple fixed supply voltages, whereas this SI has to be able to operate from just one non fixed supply voltage in the range of 2 to 4 V. Flexible power management is an essential part of the SI to be able to adapt to different application scenarios. To be able to achieve the needed energy efficiency new circuit design concepts have been proposed and implemented in the sub circuits and are discussed and compared to state of the art.

A highly efficient conversion of analog values to the digital domain is realized by a highly scalable hybrid Successive Approximation Register (SAR) Analog to Digital Converter (ADC) which underwent three evolutionary steps. With a nominal resolution of 11 bit the converter achieves good energy efficiency values of down to 24 fJ/CS and effective resolutions of up to close to 10 bit. It can operate at supply voltages below 800 mV and consumes less than 10 nA when operated at a low clock rate.

Reference voltages are needed throughout the circuit and are provided by a novel, ultra-low power, low voltage compatible and low area consuming switched capacitor bandgap circuit. Three different implementations of the architecture are presented to show the broad applicability of the concept. The ultra-low power version consumes just 25 nA and works down to 750 mV supply voltage at room temperature. Also the area with just $0.0336\,mm^2$ is very small when compared to other low power references. A proposed figure of merit for reference circuits shows the excellent power, area and temperature stability combination of the presented circuit. Another version was implemented in a 65 nm Complementary Metal-Oxide-Semiconductor (CMOS) process to show the compatibility with a wide variety of process nodes and offers a shorter than 10 μs start-up time.

To offer some actual functionality of the sensor node, two analog front-ends which can connect to various sensors, mostly for biomedical applications, were implemented and are presented in this work. One of them, the impedance measurement interface, can excite sensors with a sine signal and measure the amplitude and phase relation between voltage and current at the sensor. A wide frequency range from DC up to several MHz is achieved by digital signal generation. Small signal amplitudes of nominal 30 mV are supported to enable non-destructive measurements of living cells. The second front-end is capable of performing cyclic voltammetry measurements which are used in analytical chemistry.

Kurzfassung

Radio Frequency Identification (RFID) Transponder enthalten heutzutage immer noch wenig bis keine Fähigkeiten Umgebungsvariablen zu messen. Diese Arbeit präsentiert mehrere modulare Wireless Sensor Nodes (WSNs), welche mit einem ebenfalls modular aufgebauten Sensorinterface ausgestattet sind. Der kleinste vorgestellte Sensorknoten besteht nur aus einem einzigen winzigen Stück Silizium und weist ein Volumen von unter $1\,\mathrm{mm}^3$ auf. Mehrere andere Implementationen, welche etwas größer sind, dafür aber mehr Fähigkeiten bieten, werden auch gezeigt.

Das Hauptthema dieser Arbeit stellt das allgemein einsetzbare Sensorinterface dar. Sein Ziel ist es mit einer sehr kleinen Energiemenge, welche in einem kleinen Kondensator gespeichert sein kann, ein möglichst gutes Messergebnis zu erzielen. Die Lösung dieser Aufgabe erfordert den Entwurf von neuen und Einsatz von vorhandenen Techniken zum Minimieren der benötigten Versorgungsspannung und des Stromverbrauchs. Die verwendeten Schaltungen und erzielten Ergebnisse werden in dieser Arbeit vorgestellt.

Im Allgemeinen werden bereits existierende Sensorinterfaces mit einer oder mehreren fixen Versorgungsspannungen betrieben. Die hier beschriebene Schaltung kann mit einer einzigen, sich während des Betriebs ändernden Versorgungsspannung im Bereich von 2 bis 4 V, betrieben werden. Ein flexibles Management der zur Verfügung gestellten Energie ermöglicht es, dem Sensorinterface sich an viele Anwendungsfälle optimal anzupassen.

Eine Umsetzung der analogen Messgrößen in digitale Werte wird durch einen hoch effizienten hybriden Sukzessive Approximations Register Analog-Digital-Umsetzer (SAR ADC) erledigt, welcher im Laufe dieser Arbeit drei Evolutionsstufen durchlief. Der Umsetzer bietet eine nominelle Auflösung von 11 Bit und erreicht eine Umsetzungseffizienz von 24 fJ/CS bei einer effektiven Auflösung von bis zu 10 Bit. Die Schaltung ist in der Lage mit Betriebsspannungen von unter 800 mV zu arbeiten und verbraucht, wenn mit niedriger Umsetzungsfrequenz betrieben, unter 10 nA Strom.

Referenzspannungen werden an vielen Stellen der Gesamtschaltung benötigt und werden von einer neuartigen Schaltung bereitgestellt, welche trotz niedriger Versorgungsspannung und sehr niedrigem Stromverbrauch bei geringem Flächenbedarf am Chip immer noch arbeitet. Die sonst unerreichte Kombination dieser erwünschten Eigenschaften wurde durch den Einsatz von geschalteten Kapazitäten erreicht. Drei verschiedene Varianten der vorgeschlagenen Architektur werden vorgestellt und zeigen die breite Anwendbarkeit des Schaltungskonzepts. Die Version mit dem geringsten Stromverbrauch kommt mit 25 nA Strom aus und kann bei Versorgungspannungen von nur 750 mV bei Raumtemperatur bereits eine stabile Referenzspannung bereitstellen. Auch der Flächenbedarf ist mit $0.0336\,\mathrm{mm}^2$ deutlich geringer als bei den meisten anderen Referenzschaltungen. Um die Kombination der Parameter: Stromverbrauch, Versorgungsspannung, Flächenbedarf und Temperaturstabilität zum Ausdruck zu bringen, wird eine Kennzahl für Referenzschaltungen vorgeschlagen und die entworfenen Schaltungen mit bestehenden Publikationen verglichen. Eine zweite Variante der Schaltung wurde in einem 65 nm CMOS Prozess entworfen und zeigt, dass die Schaltung auch in modernen Technologien funktioniert und Einschaltzeiten von unter $10\,\mu$s erreicht werden können.

Um den Sensorknoten eine eigentliche Funktionalität zu geben, wurden zwei spezielle analoge Schnittstellen für das Sensorinterface entworfen. Beide sind hauptsächlich für den biomedizinischen Bereich konzipiert und werden in dieser Arbeit auch beschrieben. Eine der beiden Schnittstellen,

eine Schaltung zur Messung der komplexen Impedanz eines Sensors, ist in der Lage einen Sensor mit einem sinusförmigen Signal anzuregen und die Verhältnisse zwischen Spannung und Strom in Amplitude und Phase zu ermitteln. Dies kann für Frequenzen vom DC-Bereich bis zu einigen MHz erfolgen und wird durch eine digitale Erzeugung des Sinussignals erreicht. Um die im Applikationsbereich vorkommenden lebenden Zellen nicht zu verletzen, kann die Schaltung mit kleinen Spannungsamplituden von nominell 30 mV arbeiten. Die zweite Schaltung dient der Auswertung von Reaktionsmechanismen mittels der Durchführung einer Voltammetriemessung.

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Martin Wiessflecker (Graz, September 2013)

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Acronyms

AC	Alternating Current
ADC	Analog to Digital Converter
ALU	Arithmetic Logic Unit
ASIC	Application Specific Integrated Circuit
CDF	Cumulative Distribution Function
CMOS	Complementary Metal-Oxide-Semiconductor
CPU	Central Processing Unit
CS	Conversion Step
CTAT	Complementary to Absolute Temperature
DAC	Digital to Analog Converter
DC	Direct Current
DC/DC	Direct Current to Direct Current
DMOS	Double-Diffused MOSFET
DNL	Differential Non Linearity
ENOB	Effective Number of Bits
EPC	Electronic Product Code™
eWLB	Embedded Wafer Level Ball Grid Array
FFT	Fast Fourier Transformation
FOM	Figure of Merit
GPB	General Purpose Bus
HF	High Frequency
IDAC	Current-Steering Digital to Analog Converter
IDES	Interdigitated Electrode Structure
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral Non Linearity
ISSCC	IEEE International Solid-State Circuits Conference
LSB	Least Significant Bit
MOM	Metal-Oxide-Metal
MOS	Metal Oxide Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor

MSB	Most Significant Bit
NFC	Near Field Communication
NMOS	n-channel MOSFET
OPA	Operational Amplifier
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PMOS	p-channel MOSFET
PSRR	Power Supply Ripple Rejection
PTAT	Proportional to Absolute Temperature
RFID	Radio Frequency Identification
RSSI	Received Signal Strength Indication
SAR	Successive Approximation Register
SFDR	Spurious-Free Dynamic Range
SiP	System-in-Package
SNDR	Signal to Noise and Distortion Ratio
SoC	System-on-Chip
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
TG	Transmission Gate
UHF	Ultra High Frequency
UWB	Ultra-Wideband
VLSI	IEEE Int. Symposium on Very Large Scale Integration
WSN	Wireless Sensor Node

Chapter 1

Introduction

1.1 The Need for Wireless Sensor Nodes

In the past several years, publications about wireless sensor nodes have become more and more popular. Figure 1.1 shows the publications that can be found on IEEE Xplore® Digital Library on the topic of wireless sensor nodes each year. A peak of more than 3400 publications after just about ten years of growth can be seen in the year 2010, with a subsequent slight decrease.

So was this the all-time high of research effort in this topic? Are all problems solved and the wireless sensor nodes already in production and everywhere around us? Or are there unavoidable issues with the idea of wireless sensor nodes? While many of these questions cannot be answered right now it is obvious that in everyday life these sensor nodes have not been able to establish themselves yet. The biggest issue is probably that they are still too expensive to be attractive for high-volume markets. Nevertheless, interesting applications are possible with wireless sensor nodes, but the power demand of certain sensors requires the use of batteries which are rather big, mostly toxic and expensive. On the other hand, commonly sold RFID tags work passively but nowadays offer little to no sensor capabilities and are still mostly the size of a credit card. In this thesis a highly integrated sensor node in multiple configurations is presented, and system sizes far smaller than most of today's available systems were achieved. This also allows for a vigorous reduction of cost when produced in mass quantities. To broaden the possible use case scenarios and hence to allow these large production quantities, the sensor node can easily be adapted for multiple applications with various system sizes, sensors and communication devices.

1.2 Challenges of Wireless Sensor Nodes

The dream of wireless sensor nodes often also referred to as wireless sensor tags or wireless sensor grains especially for biomedical applications is that they should be ubiquitous while being invisible. They should give valuable information to their user without making him or her feel uncomfortable. This requires the system to shrink in size by a large margin from today's bulky analysis tools. This miniaturization comes with its benefits and drawbacks. The drawbacks are mostly a limited communication range due to the very small integrated antenna and a limited amount of power and energy available for a single measurement. Also, classic discrete components have to be avoided as their physical sizes are too big.

To tackle the given constraints of a small system, existing traditional designs have to be changed to a great extent while reuse and multi-purpose usability should be kept available. The following chapters will introduce a integrated modular wireless sensor node with a generic sensor interface.

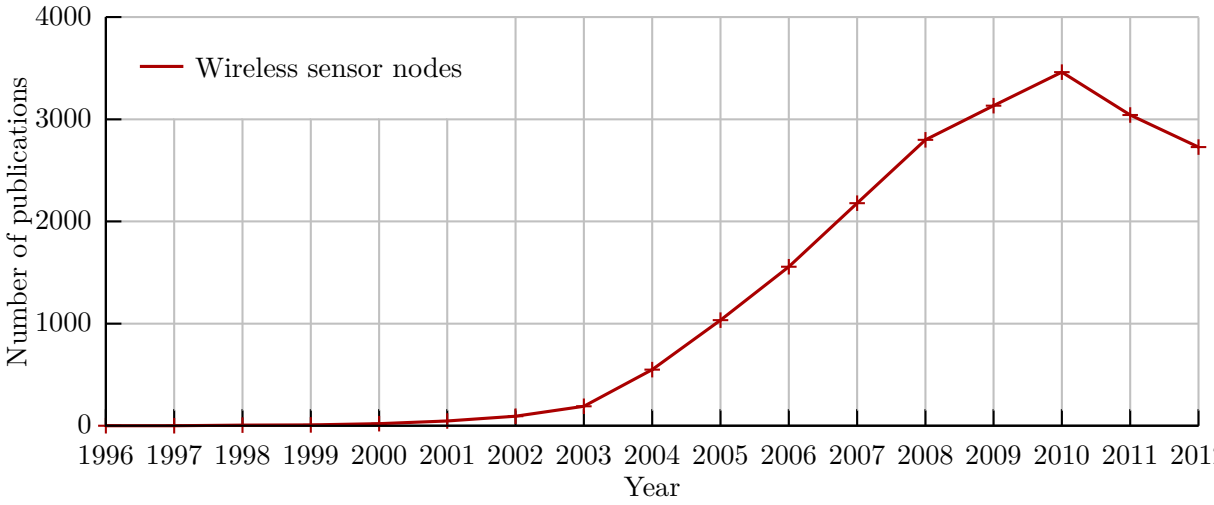


Figure 1.1: Number of publications found on IEEE Xplore® Digital Library on the topic of wireless sensor nodes over time

1.3 Wireless Sensor Node Concept

A platform concept has been developed to form the basis for specialized implementations to cover a vast field of applications. The design is kept modular with simple connections so multiple different combinations are possible, of which several will be shown in more detail.

The basic block diagram of the wireless sensor node is shown in Figure 1.2. It consists of an antenna, an energy storage device, one or multiple sensors and the Application Specific Integrated Circuit (ASIC). The border of the ASIC is marked by the dashed gray line.

As can be seen three components of the system are not within the ASIC as they are hard to implement in CMOS technology. Since the physical size of the system should be as small as possible a System-in-Package (SiP) solution based on the Embedded Wafer Level Ball Grid Array (eWLB) technology was developed which needs no further components outside of the package. A three-dimensional rendering of this 6x6x1 mm small SiP can be seen in Figure 1.3a. Two only 100 μm thick silicon dies can be seen next to each other that are surrounded by molding material. Two layers of metal form connections between the two dies, a loop antenna with 15 windings, test pads and a sensor which is explained in detail in Section 5.1. Of the two dies the smaller one is the ASIC containing all blocks that are also shown in Figure 1.2. The bigger die is the storage capacitor which is manufactured on silicon by IPDiA® using trench capacitor technology. An alternative grain shown in Figure 1.3b is available which also incorporates two separate dies. The smaller one contains only the sensor interface while the second one is a fully fledged Near Field Communication (NFC) compatible microcontroller based communication and power supply chip which also enables encrypted communication.

Though it is hard to implement all the previously mentioned components within a single ASIC, it

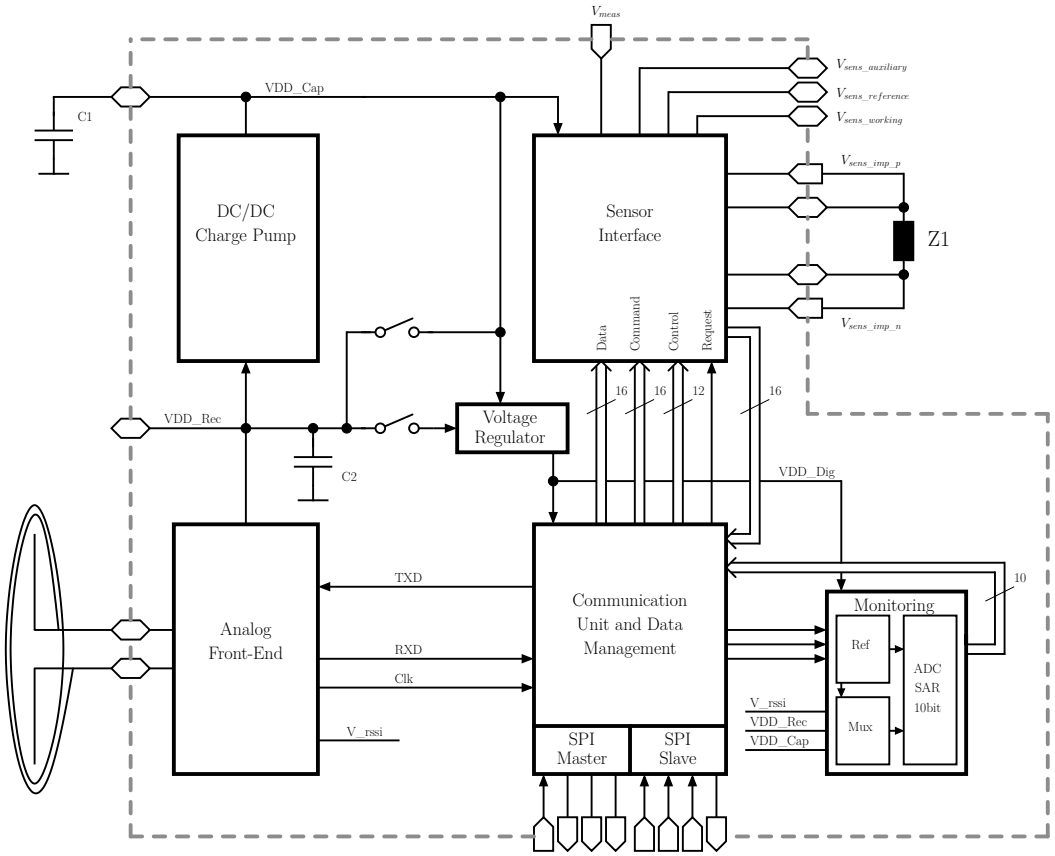
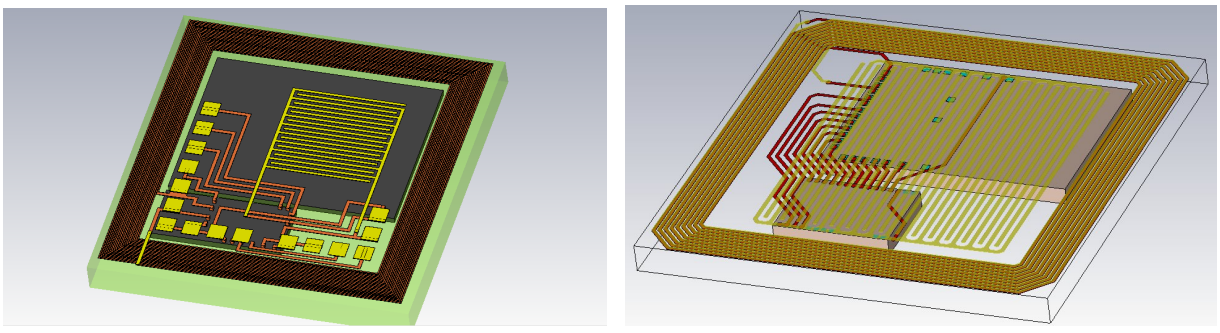


Figure 1.2: Wireless Sensor Grain - System overview



(a) Variant 1 (b) Variant 2

Figure 1.3: 3D render of Wireless Sensor Grain as SiP implemented in eWLB

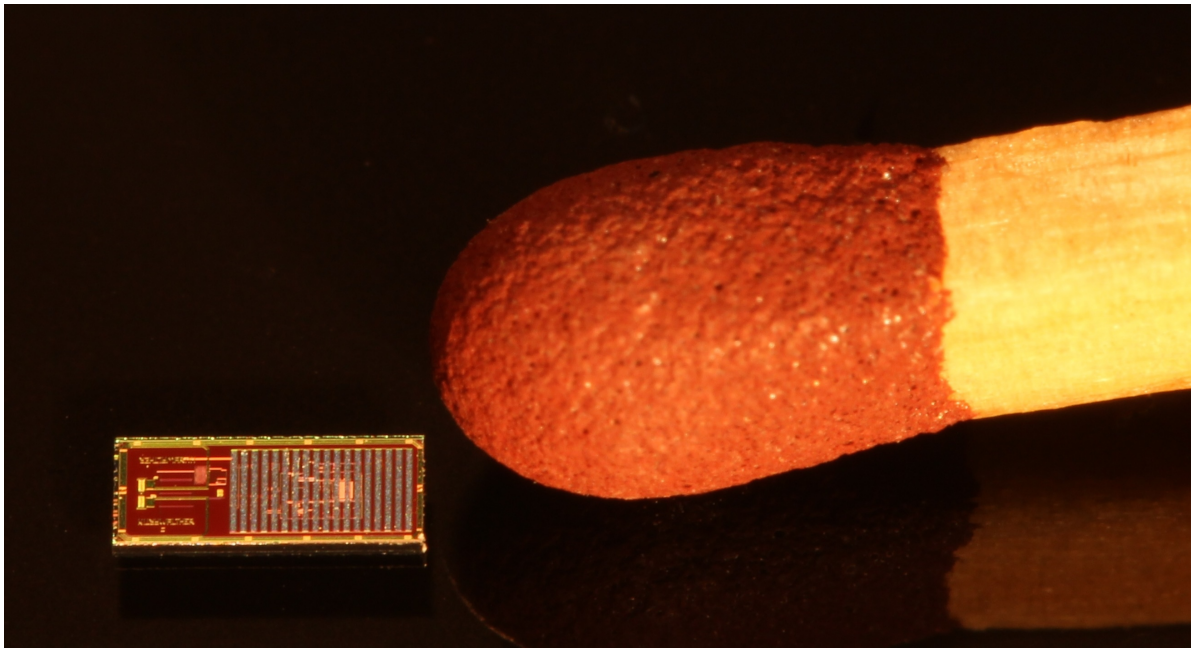


Figure 1.4: Fully integrated CMOS only sensor grain

still is possible and was done. This 1.2x3.0x0.22 mm small System-on-Chip (SoC) solution is shown in Figure 1.4. A layout plot and a micrograph of this chip are shown in Figure A.3 and Figure A.4. The comparison with a match stick shows that such a system can be built very small. The drawback of such a highly integrated system is that the integrated components show worse performance than their external discrete cousins. The energy storage device can store considerably less energy, the communication range of the antenna and the area of the implementable sensors are limited.

To cover even more applications which require higher performance and especially higher communication range the same ASIC was also manufactured without the on-chip antenna, sensor and capacitor. This allows the chip to connect to a conventional credit card sized antenna which allows for communication distances up to 8 m. The layout plot and a micrograph of this chip are shown in Figure A.1 and Figure A.2. This chip is also great for debugging and performance characterization purposes.

1.3.1 Communication, Energy Transfer and Harvesting

The developed ASIC features a dual frequency Radio Frequency Identification (RFID) front-end which can supply power to the circuit as well as provide bidirectional communication. As RFID is a passive protocol with a master reader device and a slave tag, every data transfer has to be initiated by the reader device. As depicted in Figure 1.2 the analog front-end is responsible for rectification of the AC signal from the antenna. Signals from the reader are supported according to the Electronic Product Code™ (EPC) HF standard at 13.56 MHz and EPC Class 1 Gen2 UHF standard at 868 MHz. In addition to energy, the front-end also extracts clock and data from the modulated field sent by the reader. A digital input enables the front-end to take a serial communication stream from the communication unit to modulate data back to the reader device.

Additionally a Received Signal Strength Indication (RSSI) signal is generated by the front-end which is used to monitor the signal strength at the tag.

The communication unit and data management block [1] handles the wireless communication as well as the optional wire-based communication via Serial Peripheral Interface (SPI). Both interfaces are compliant to the standards. The wire-based interface offers master and slave operation. SPI master mode enables the chip to act as bridge between the RFID and SPI interface while the slave mode can be used to control the chip with another master device. The main functionality, though, is transferring configuration data to the sensor interface block and relaying measurement results from the sensor interface back to the reader device.

A DC/DC converter [2] used as a charge pump can be activated by the communication unit via a command of the reader device. It takes energy from the analog front-end and converts it to a higher voltage and lower current level and is used to store energy on capacitor $C1$. The voltage residing at $C1$ is fed to the sensor interface and a voltage regulator. During times when the system receives no energy from the outside this capacitor can supply the chip.

The voltage regulator [3] can be either fed by the voltage VDD_Rec from the analog front-end or from the storage capacitor $C1$. It supplies a regulated voltage to the communication unit and the monitoring block.

1.3.2 Monitoring

The monitoring block is used to measure basic system parameters like the received signal strength, the voltage at the rectifier, the voltage at the storage capacitor and the chip temperature. A bandgap voltage reference according to the principle shown in Section 3 and a 10 bit Analog to Digital Converter (ADC) [4], combined with some logic for control are implemented in this block. The information the monitoring offers enables the software running on the reader to adapt to the system status. As an example the software can wait for the storage capacitor to be charged to a certain value, warn the user of a too weak communication link or prevent the usage of the system at temperatures it was not specified for.

1.3.3 Measurement Software

To get actual measurement results out of the proposed sensor nodes requires a considerable amount of software with many layers of abstraction. Software is running on the host device, a PC or a NFC enabled smart phone, to form a measurement firmware for the sensor interface, to evaluate and display the measurement results and to communicate with the reader. The firmware for the sensor interface is transferred via one of the available interfaces into the memory of the microcontroller and is subsequently executed.

The end user should always interact only with an attractive and easy to use graphical user interface while complex analysis software interprets the measurement results. These parts were not implemented as they vary from application to application, are mostly not known up front and need a multidisciplinary approach with all partners involved. Nevertheless as the instruction set

of the microcontroller inside the sensor interface is proprietary, a basic assembler was developed to enable easier development of measurement software. Also stand-alone versions of the sensor interface are available to ease implementation and characterization of measurement procedures.

1.3.4 Example Measurement Flow

Figure 1.5 depicts how a single measurement looks in time domain. It should be noted that the time on the x-axis is not to scale as the actual times can vary by a great extent in reality.

The first row of the plot indicates the amplitude of the RFID field which is sent out by the reader and modulated during communication either by the reader itself or the sensor grain. The whole measurement cycle begins with the reader activating the field. Very shortly after, the communication starts and the reader identifies the sensor node. If an appropriate identification string was received the process is continued and the reader sends a command to the tag which activates the charge pump of the chip. As a result of this, as seen in the third row of the plot, the voltage on the storage capacitor starts to rise. This charging process is monitored until a certain configurable voltage level is reached. As now the software on the host can be sure that enough energy is available for a measurement, the sensor interface gets activated by another command. After some time the regulated supply voltage for the bus system within the sensor interface settles and enables communication to its inner parts. All these parts are further discussed in Section 2. Another command activates the supply in the sensor interface which feeds the volatile program memory and the microcontroller. Next the measurement firmware is transferred from the host through the wireless interface, the communication unit and the bus system in the sensor interface to the program memory. Another command enables the microcontroller which begins to execute the just transferred program. At this moment in time the tag becomes independent from the reader and thus the RFID field can be deactivated to not interfere with the measurement. Within the control of the microcontroller and the bus system are all the analog sensor interface blocks and companion blocks. Additionally, the microcontroller can adjust its own supply voltage which allows for low power operation at the desired clock rate. Thus the measurement can run until its code tells it to stop and ideally turn off its own power supply to preserve energy. Measurement results can be stored on a separated volatile memory which is supplied with the same voltage as the bus system. After some predefined time the reader can be sure the measurement process ended and thus the reader reactivates the RFID field and requests the measurement results. After this the program can start another measurement cycle or end communication until further user interaction.

Due to the fact that the measurement can draw a high current from the storage capacitor while the charging process can occur at a low current, the achievable operating range is maximized and the noise induced by the RFID field during measurements is eliminated. This, though, comes with a reduced overall speed of the measurement process if multiple measurements are necessary. Also the voltage level of the storage capacitor during the measurement and information holding time has to be considered. A high current consumption for a long time would drain the capacitor to an extent where the sensor interface would cease working and data integrity could not be ensured anymore. This is why the sensor interface is able to measure the voltage at the capacitor even during the normal measurement process. Thus the firmware can take action if a voltage threshold was breached. The main power consumer can be turned off, an error code can be stored in the

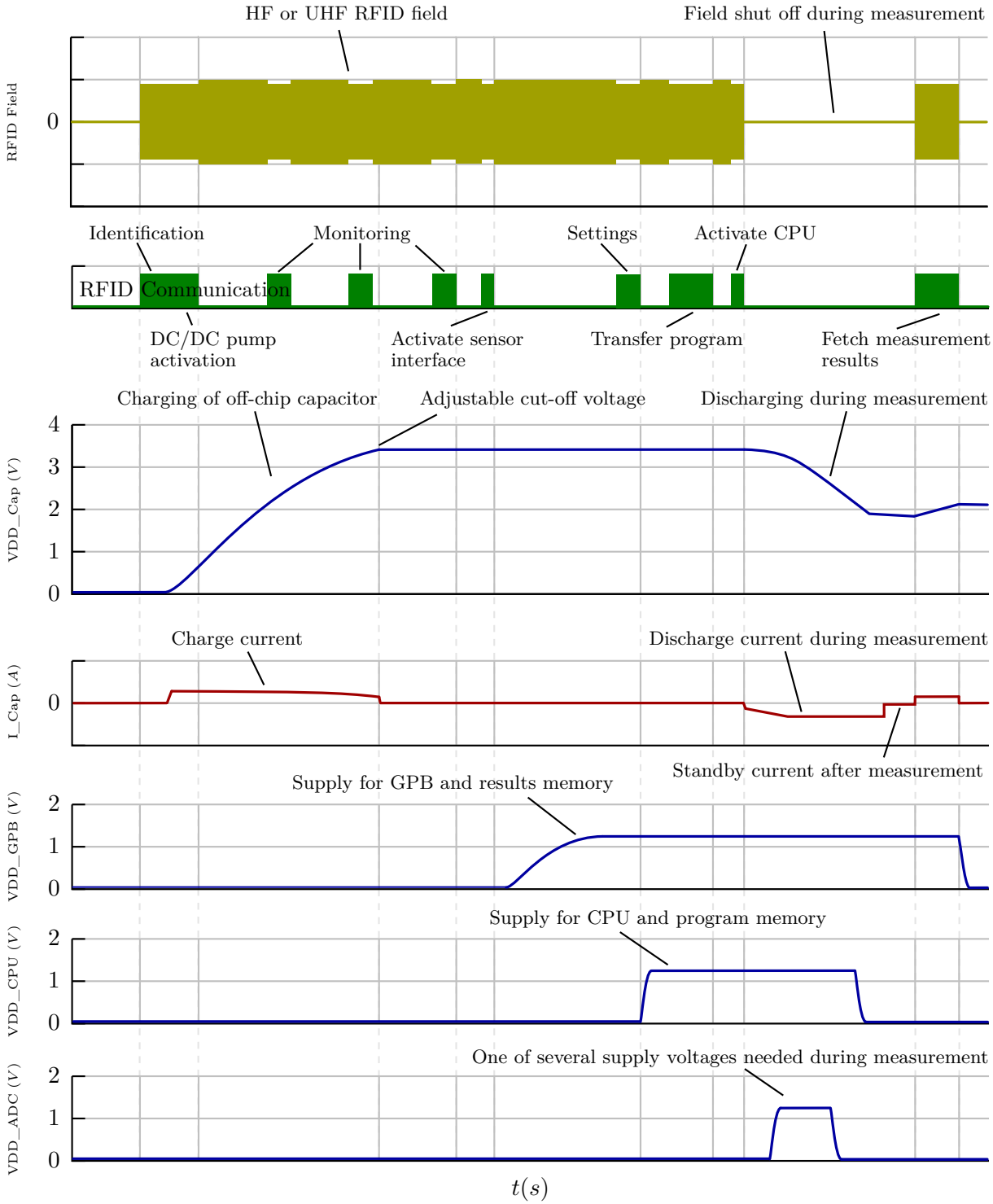


Figure 1.5: Transient operation of sensor grain

memory retained with the remaining energy in the capacitor and the reader can read it back later. In this case the software on the host device should be smart enough to change the measurement configuration in a way so that the available energy is sufficient.

Chapter 2

Generic Sensor Interface Concept

2.1 Introduction and Sensor Interface Concept

The sensor interface shown in the block diagram in the previous chapter represents the main focus of this thesis. The features of the sensor interface should include the ability to connect to various sensors while maintaining a low voltage and low current consumption operation and to be implemented purely in CMOS technology. Configuration and measurement data should be exchanged via a digital interface.

As it is not possible to include specialized analog interfaces for each type of sensor all at once a modular design was created which allows adding or dropping abilities. This makes it possible to create area efficient implementations for multiple specific applications while maintaining low system design effort.

Figure 2.1 shows the final top-level structure of the sensor interface. A simpler intermediate version of the sensor interface was included in a Wireless Sensor Node (WSN) and was published in [5]. Certain blocks are discussed in more detail in the following sections. The bandgap reference blocks and the ADC were designed with special care and Chapter 3 and 4 discuss them in great detail. Two types of specialized sensor front-ends were implemented. One is briefly introduced in this chapter while the other is explained in more detail in Chapter 5.

2.2 Power Management of Sensor Interface

Only a single voltage supply VDD_Cap is necessary for the sensor interface to operate. As this voltage can be connected to the external storage capacitor or a charge pump, non-constant voltages have to be expected. When the current is drawn from a capacitor a steadily decreasing voltage can be expected, while a continuous operation at the output of a charge pump implies a dynamic voltage ripple. The power management should provide multiple stabilized and configurable supply voltages for the sensor interface and its numerous analog blocks. Also, a low drop operation is inevitable to be able to best utilize the stored energy in the capacitor or to allow operation at weak field strength.

To be able to generate regulated supply voltages a reference voltage is needed. Since VDD_Cap can be non-constant and the Power Supply Ripple Rejection (PSRR) of every reference is limited a two stage architecture was implemented. VDD_Cap supplies a standard bandgap [6] which offers a buffered output voltage of 1.2 V. This voltage is used to supply another bandgap which is implemented according to the principle shown in Section 3 and has an integrated oscillator and

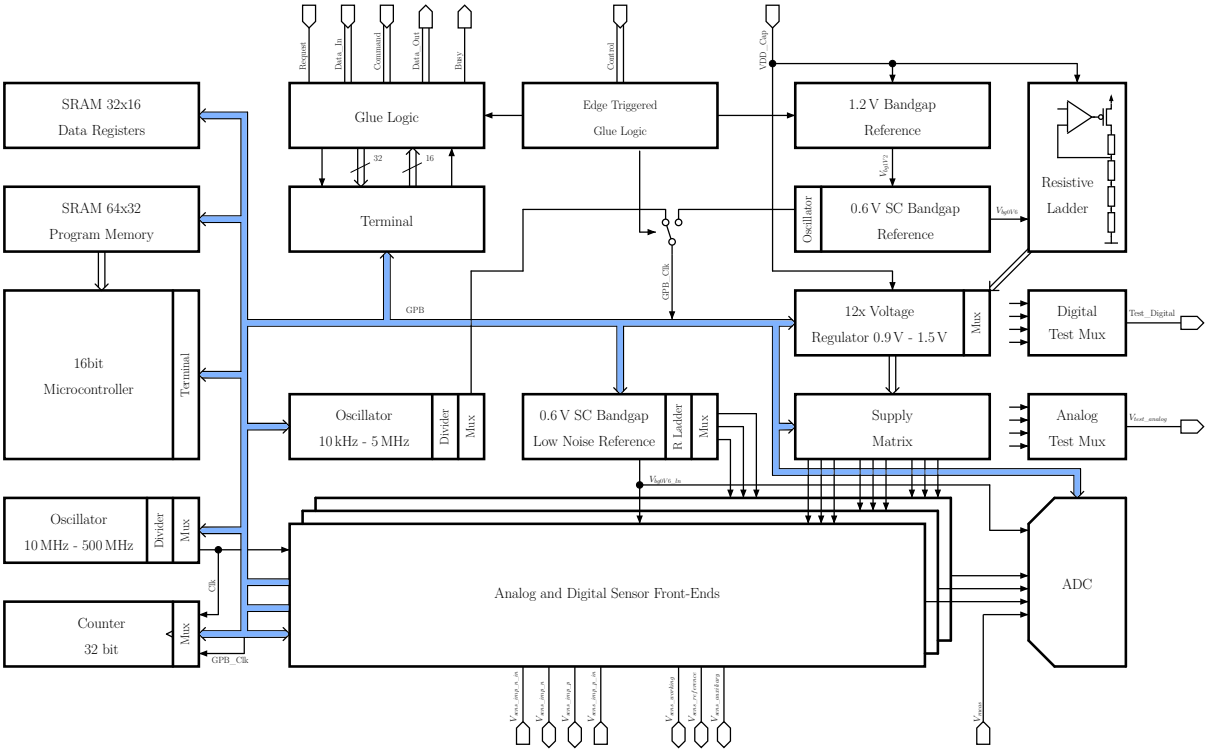


Figure 2.1: System overview

an output voltage of approximately 0.6 V. Its output voltage is fed to a resistive ladder which has multiple taps. These taps are placed in a way so that seven voltages from 0.9 to 1.5 V in 0.1 V steps are generated. The scaled reference voltages are fed to twelve linear NMOS voltage regulators which each have an analog mux to select their reference voltage. Four of the generated supply voltages are assigned to fixed blocks within the sensor interface while the other eight are connected to a supply matrix which can selectively distribute the supplies to multiple blocks. The four preassigned supplies are reserved for the bus system, the microcontroller, the low speed oscillator and basic analog blocks like the analog test mux.

2.3 Start-Up and Stand-Alone Operation

When the sensor node is within reach of the reader and the field gets activated the sensor interface has to stay in a state where it does not consume any power, as it otherwise would eventually drain the supply of the whole sensor node and would thus render communication impossible. Also, it should be possible for the sensor interface to operate when all other blocks outside of it are shut off. This implies a switch is needed that can be activated and deactivated and displays a controlled start-up behavior. Figure 2.2 shows how these requirements were met. Several of the depicted switches are integrated into the system to steer vital functions during start-up. The edge triggered switch consists of two pulse generators at its two inputs. Two separate inputs for activation and deactivation of the switch are present to guarantee controlled behavior. The pulse generators display a short high pulse at their output whenever a low-high transition occurs at

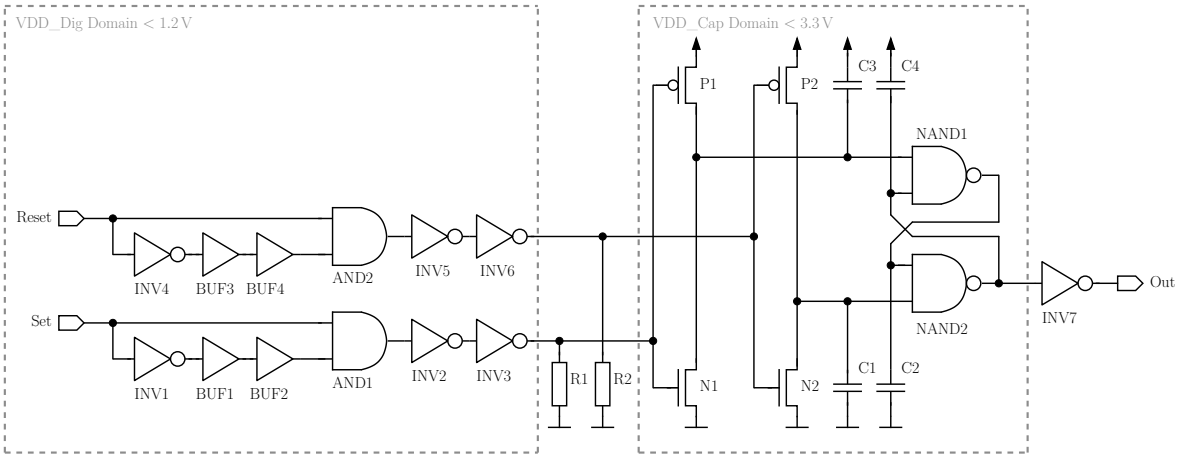


Figure 2.2: Edge triggered logic

their input. Inverters of increasing strength are connected to the pulse generator to be able to overwrite the impregnated low level by the two resistors $R1$ and $R2$. Till here the circuit has to be supplied by the same voltage as the controlling part uses. In case of the sensor node this is the communication and data management unit. This supply voltage can vary but only for voltages greater of 0.7 V are the inverters able to force a voltage across the resistors that is high enough to make the transistors N1 or N2 conductive enough. These two transistors combined with P1 and P2 form two inverters that act as level shifters. The n-channel transistors are designed to be far stronger than the p-channel transistors, which is necessary as the supply of the level shifters output can be higher than from the pulse generators. This circuit has no static current consumption as the expected signal of the pulse generators is low, which means no current has to flow through either of the resistors or transistors. The shifted pulses are fed to a reset-set flip-flop consisting of NAND1 and NAND2. An additional inverter buffers the output of the flip-flop to avoid feedback from downstream circuits. Four capacitors connected to the flip-flop are present to dynamically predefine the output value to zero when a supply gets connected to the circuit.

This circuit can hold the information of the output value for as long as the voltage on VDD_Cap does not become too low. The stored value can be changed by low-high transitions at two inputs with voltage levels high enough so that a correctly working control entity can be assumed. Besides leakage and short pulses during switching, no current is consumed. The circuit enables the sensor interface to be switched on only when the control entity is working and outputs clear low-high transitions to the sensor interface. No leakage at the inputs can occur as the gates at the input are supplied by the same supply voltage as the control entity itself, which is beneficial when the supply voltage can fade out. Once the sensor interface is switched on and configured it can operate on its own even if the control entity gets shut off, for as long as VDD_Cap can supply the circuit. When the control entity wakes up later it can again start to control the sensor interface.

2.4 General Purpose Bus

The sensor interface consists of many digital and analog blocks that serve different functions. The design passed through multiple evolutionary steps, and the first design had only the capability for

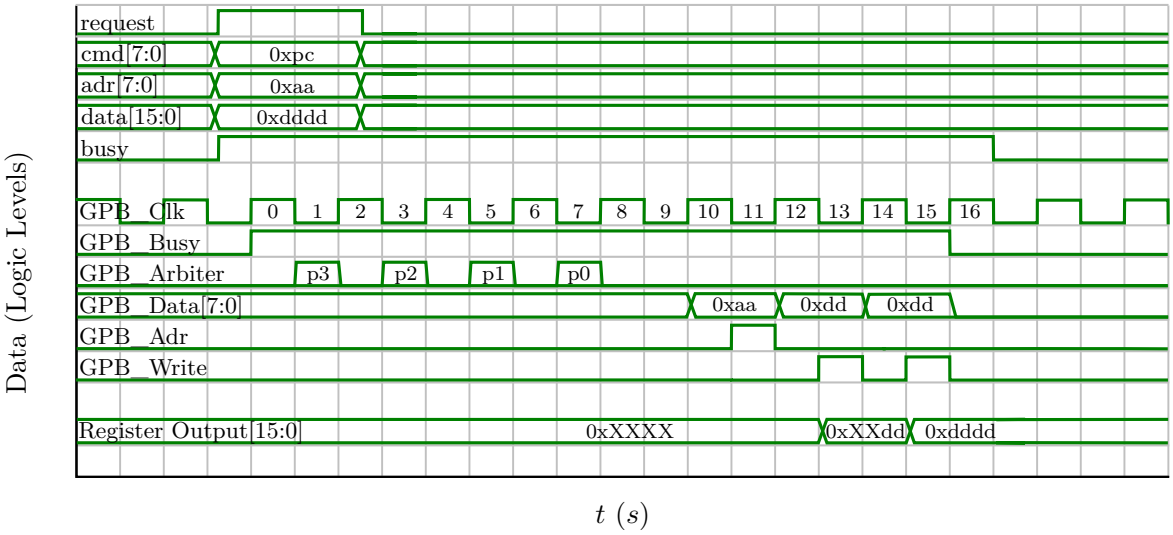


Figure 2.3: Write operation on GPB

one type of measurement. For this purpose a finite state machine was a good although not ideal solution. Configuration data that was passed to the sensor interface in a parallel manner was used to determine when which block was activated and for how long. Also, additional configuration of analog blocks was available. In sum a total of over 450 bits were necessary to fully configure the sensor interface, despite its limited functionality at that point in time. The configuration was supplied by the communication and data management unit with 256 parallel wires while the rest was set to predefined values. A larger amount of wires was not justifiable, and the data management unit had to stay connected to the power supply at all times since otherwise the unlatched configuration would have been lost.

The final version of the sensor interface therefore includes a so called General Purpose Bus (GPB). It makes it possible to send 16 bit wide words of configuration or measurement data over a 8 bit wide bus with addressing capabilities. Figure 2.1 shows the bus colored in light blue, which is consistent throughout this document. The bus is connected to two terminals which are the only bus participants which are able to actively write and read to or from the bus. A third terminal was planned for the ADC but due to complexity this was postponed for the next version. Besides the two terminals, the bus is connected to 53 configuration and data registers and Static Random-Access Memory (SRAM).

Figure 2.3 shows the timing of a write command executed on the GPB by a terminal. The terminal has a 33 bit wide input in total. The cmd[7:0] signal contains 4 bit of priority and 4 bit for selecting the operation to be executed. Write and reads inverted or non-inverted can be done. A read data word can be stored in the terminal itself and used as data for a subsequent write operation. This is helpful when content should be copied from one to another memory location. The adr[7:0] signal tells the terminal where to write to or read from. Two 16 bit data signals are available, one for input and one for output, but in the plot only the input is shown for this write operation. When all signals are steady the low-high transition at the request signal latches all information in

the terminal and the busy output signal of the terminal is set to high until the transmission finished.

The GPB consists of 15 signals in total of which 8 are for the transmitted address and data. A clock signal GPB_Clk is used to synchronize all operations. GPB_Busy is high when the bus is active to show another terminal that no action can be started right now. GPB_Arbiter is used to solve the problem of who is authorized to act on the bus if two or more terminals want to initiate action at the same time. Up to 15 terminals are supported and each terminal can be given a priority. During operation the 8 signals of GPB_Data[7:0] first carry the 8 bit address, then the low byte, and finally the high byte of the data. GPB_Adr is set to high when the address is present on the GPB_Data signal so the receiver of the write operation knows that it is addressed. Two high signals on GPB_Write initiate the takeover of the data from the data signal to the receiver. Two additional signals are not shown in the plot. They are used to reset all configuration registers and to initiate a read transaction.

2.5 Microcontroller

Since the aforementioned state machine's configurability was limited, another control instance was needed. This instance should be able to perform all actions needed for a highly complex measurement. For example it might be necessary to first configure various analog blocks, then to measure the offset of the circuit including the ADC, then to start the measurement itself and do multiple reconfigurations during the measurement. During the process multiple data words have to be collected and stored containing offset voltages, temperature and measurement results. All this in a flexible programmable manner is more or less only possible with a microcontroller.

So it was decided that a microcontroller was necessary. A few additional technical limitations however made the usage of an already existing design of a microcontroller not feasible. First, it is necessary to keep the area and complexity as low as possible. Many gates used in a design have the disadvantage of increased leakage. The performance of the microcontroller is of minor importance as no complex signal processing should be performed on-chip. From a technological point of view there is the problem that no non-volatile memory is available in the given technology. This means the program as well as the data must be stored in volatile memory with very limited size.

Due to all these constraints a new microcontroller was designed from the ground up. Its block diagram can be seen in Figure 2.4.

The measurement program can be stored in a 64x32 bit SRAM. Each instruction is 16 bit wide but there are several instructions which need two words. This means up to 128 instructions can be stored in the memory. It can be written by two registers which are connected to the GPB and also read by an additional register. The address is fed by the program counter which is 7 bit wide and can be preset by a register, the instruction decoder by a GOTO command or simply incremented.

The 16 bit wide instructions are fed to an instruction decoder which takes control of all parts of the controller. It steers a terminal which connects the controller to the GPB to actively do transfers. Values read from the terminal can be stored in two registers called WREG1 and WREG2. They can, together with a literal or the result of the last Arithmetic Logic Unit (ALU) operation, be

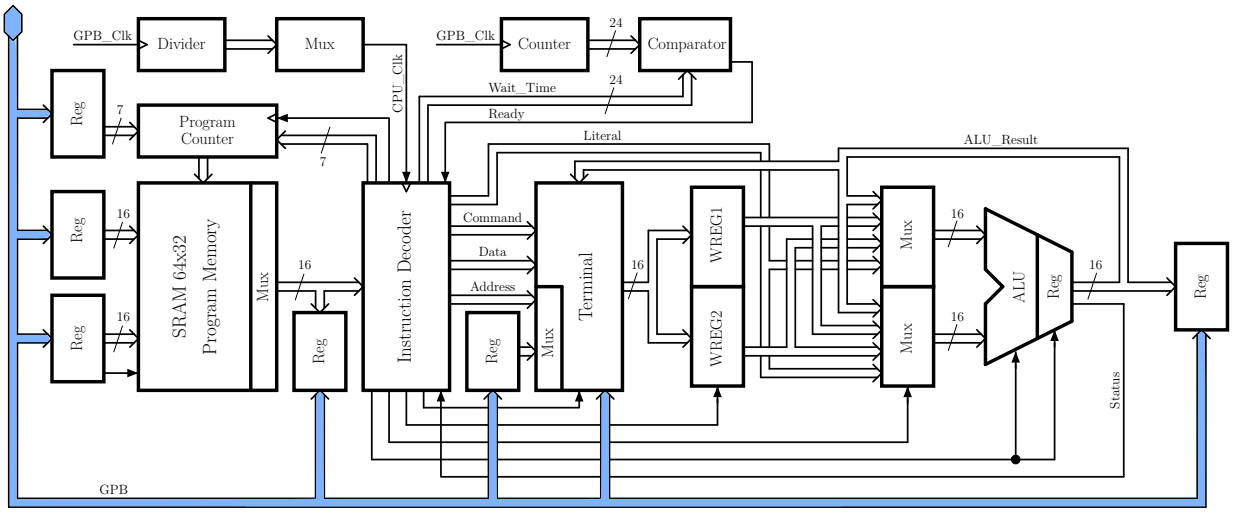


Figure 2.4: Microcontroller

fed to the ALU itself. The instruction decoder takes its clock from the clock included in the bus system with an additional pre-divider. The controller is able to access the configuration of this pre-divider itself so it can adaptively alter its speed to the changing requirements during program execution. A 24 bit wide counter and comparator is included which is triggered by a wait command instead of a simple single cycle no operation command. This enables the measurement program designer to implement wait times easily while power consumption is kept low during this wait operation. This was done to avoid the necessity of adding further complexity to the controller by adding a timer unit and interrupt capability.

Table 2.1 shows all commands which are supported by the instruction decoder and thus microcontroller. As already explained the WAIT command waits for a certain time. This time is determined by the clock on the bus, the pre-divider setting and a 24 bit number. This gives enough dynamic range to cover short as well as quite long events. This command, due to its large operand, needs two words in program memory.

The GOTO command is available in five different versions, independent or dependent on the last ALU operation result, and changes the next value of the program counter. This address is a 7 bit value but an eighth bit is available for modifications in future versions with increased memory.

The MOV command is available in three different versions. MOVLF writes a 16 bit value to the desired memory location. This operation, due to the additional literal, also needs two words in program memory. MOVBF writes the last read value of the terminal to the desired address. This is beneficial if the data of a memory location should be copied into another location. First a read command would be executed which stores the value to the buffer and subsequently this buffer would be written to the new location. MOVRF writes the result of the last ALU operation directly to another location.

Two read commands are implemented. READF reads, as already described, a memory location and stores the data in the internal buffer. READFW not only stores the read value to the internal

buffer but also to WREG1 and/or WREG2 which are two registers in front of the ALU. Both the read and the move commands are able to write/read to/from predefined addresses as well as indirect addresses. This can be used to store multiple measurement results in consecutive memory locations in an array-like structure.

Multiple logical and arithmetic functions are possible with the ALU. Their names are AND, OR, XOR, COMP, ADD, INC, RL and RR. All of them process one or two 16 bit values. The ones that use two optionally need two words of space in program memory as they can include a literal. Both inputs and the output of the ALU can be inverted if desired which extends the possible operations. A hardwired multiplier or divider was not implemented and has to be emulated in software if needed.

2.6 Analog to Digital Converter Environment

The sensor interface naturally includes an ADC, which is presented in Section 4. Figure 2.5 shows the environment the ADC is embedded into. Two optional buffers are available that can buffer the reference voltage and the input voltage of the ADC. The buffer for the input voltage is only active when the ADC is in reset mode, which saves energy. The clock of the ADC is generated by a clock divider which allows the speed to be varied in powers of two. A total of 53 configuration bits are fed to the ADC by registers connected to the GPB. Two bias currents for the buffers and five bias currents for the ADC are generated in a configurable way by a bias scaler block. This makes it possible to exactly fit the current consumption of all blocks in the ADC to the required speed and accuracy. The conversion result of the ADC can be read from a register connected to the GPB but is also fed to a summation block. This block adds up a configurable number of 1 to 32 samples of the ADC, which allows for a fast and easy averaging of the measurements. The result is again readable via a register. Conversion complete signals in both cases indicate if the conversion has already finished.

2.7 Specialized Sensor Front-Ends

The whole sensor interface was laid out in such a way that multiple specialized sensor front-ends can be included into the overall system. The previously presented blocks all work to feed these specialized interfaces with reference voltages, currents, frequencies, supply voltages and process control. Two specialized sensor front-ends have been implemented up to now, of which one is described in full detail in Section 5 while the other is only briefly presented in the following Section 2.7.1. Further front-ends can easily be added to the system in future versions.

2.7.1 Voltammetry Sensor Interface

The voltammetry sensor interface can be used to conduct the electroanalytical method of voltammetry, which is the study of current as a function of applied potential. [7, 8] Linear as well as cyclic voltammograms with three electrodes can be measured. Also amperometric responses can be measured, which are a subset of voltammetry.

Table 2.1: Instruction set of microcontroller

Command	Description	Word 1	Word 2
WAIT	Waits for n cycles	`00000001 nnnnnnnn`	`nnnnnnnn nnnnnnnn`
GOTO	Sets the program counter to c	`00000010 xccccccc`	
GOTOIFNZ	Sets the program counter to c if the zero bit is not set	`00000100 xccccccc`	
GOTOIFZ	Sets the program counter to c if the zero bit is set	`00000101 xccccccc`	
GOTOIFNOV	Sets the program counter to c if the overflow bit is not set	`00000110 xccccccc`	
GOTOIFOV	Sets the program counter to c if the overflow bit is set	`00000111 xccccccc`	
MOVLF	Move literal to register	`001000mi aaaaaaaa`	`kkkkkkkk kkkkkkkk`
MOVBF	Move buffer to register	`001001mi aaaaaaaa`	
MOVRF	Move ALU result to register	`001010mi aaaaaaaa`	
READF	Read value from register to buffer	`001100m0 aaaaaaaa`	
READFW	Read value from register to buffer and WREG1 or/and 2	`0011wwm0 aaaaaaaa`	
AND	Bitwise and operation	`1000l000 xiiissss`	`(kkkkkkkk kkkkkkkk)`
OR	Bitwise or operation	`1000l001 xiiissss`	`(kkkkkkkk kkkkkkkk)`
XOR	Bitwise exclusive-or operation	`1000l000 xiiissss`	`(kkkkkkkk kkkkkkkk)`
COMP	Test if value is zero	`10000011 sxixixss`	
ADD	Arithmetic addition of two values	`1000l100 xiiissss`	`(kkkkkkkk kkkkkkkk)`
INC	Increase or decrease a value by 1	`10000101 xidixxss`	
RL	Circular rotate left no carry	`10000110 xixixxss`	
RR	Circular rotate right no carry	`10000111 xixixxss`	

`n` Number of wait cycles
`c` Address in program memory
`a` Address in data memory
`m` Direct or indirect addressing
`i` Inverted or non-inverted transfer
`w` Working register
`s` ALU operand selector
`k` Literal
`l` Literal selection
`x` Do not care

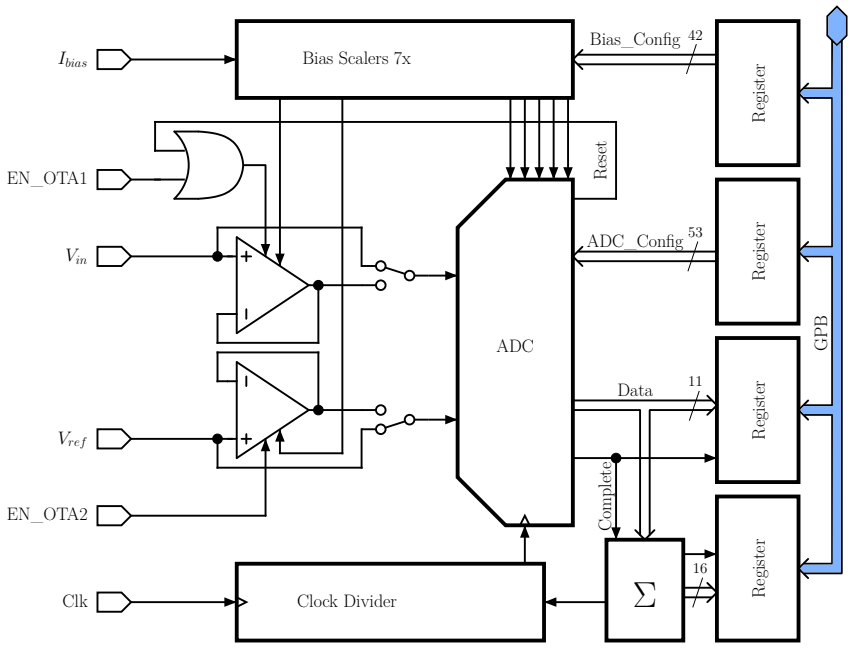


Figure 2.5: ADC block

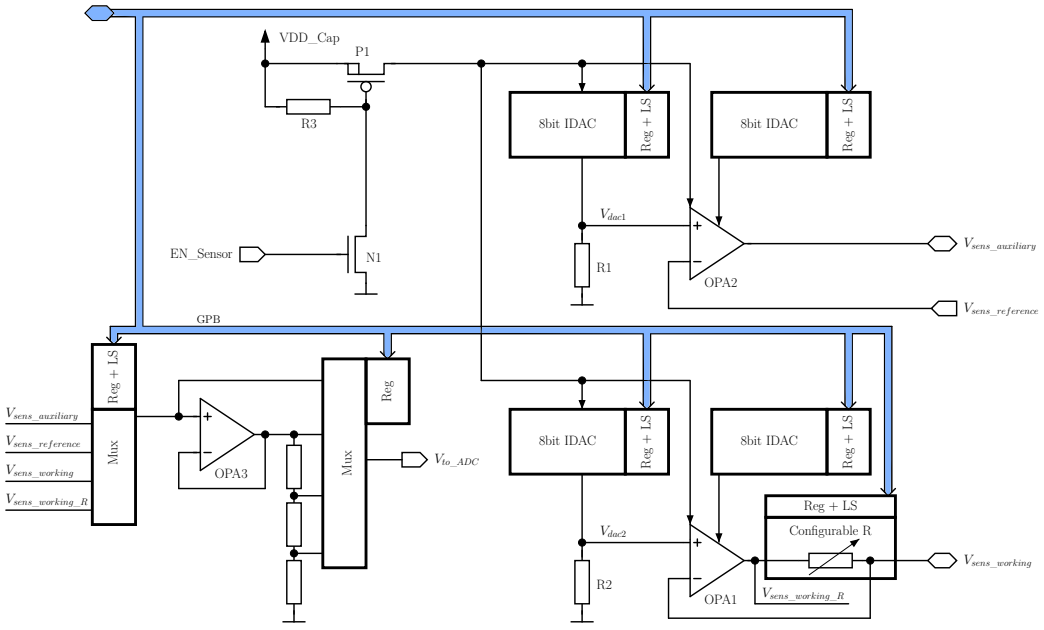


Figure 2.6: Voltammetry sensor interface block diagram

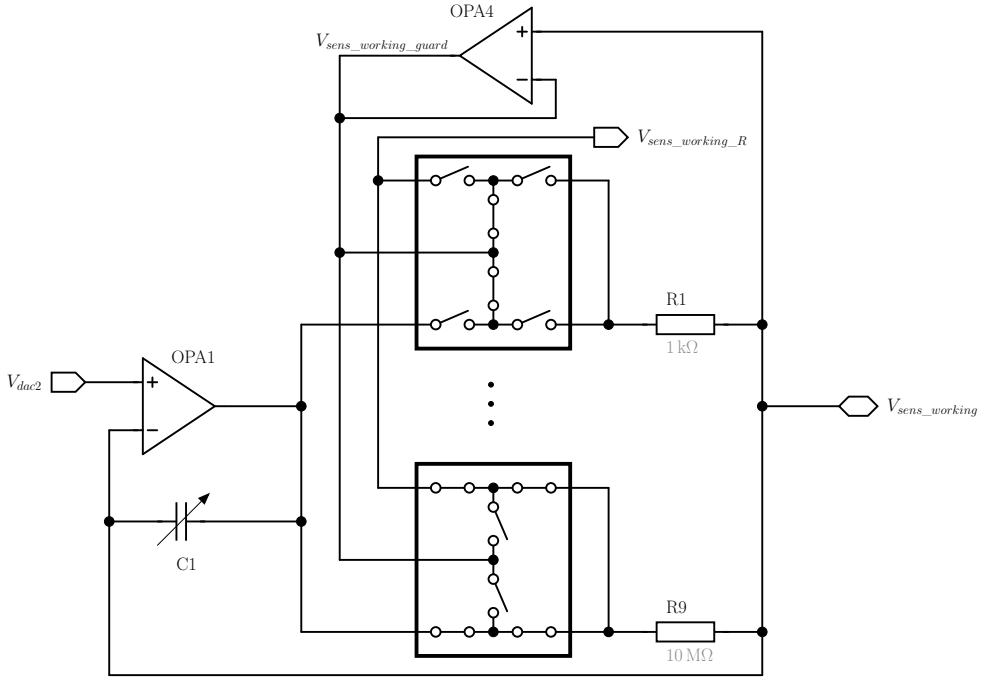


Figure 2.7: Low leakage adjustable resistor

Figure 2.6 depicts the circuit topology. Three connections to a potential sensor are present. Electrode $V_{sens\_reference}$ is only connected to the negative input of the Operational Amplifier (OPA), named OPA2, and thus carries no current. It is used to measure the potential of the fluid itself without a voltage drop. Electrode $V_{sens\_auxiliary}$ is connected to the output of OPA2 and is used to set the potential of the fluid to a certain value. With these two electrodes the potential of the liquid can be set to an exact value in respect to the third electrode $V_{sens\_working}$.

Four current steering Digital to Analog Converters (DACs) reside within this block. Two are used to generate the reference voltages V_{dac1} and V_{dac2} which should give reference for $V_{sens\_reference}$ and $V_{sens\_working}$. The resolution of the DACs is 8 bit. Since rather large voltage swings are necessary on the measurement electrodes, the DACs are supplied by VDD_Cap which can be 3.3 V and higher itself. The resistors R1 and R2 are sized so that the voltages V_{dac1} and V_{dac2} can reach voltages of up to 2.5 V, which gives a step size of 9.8 mV. The other two DACs are used to provide a configurable bias current to the output buffers OPA1 and OPA2. Output currents of up to 1 mA are achievable with the given implementation.

As the measurement method requires measuring the current which is flowing through electrode $V_{sens\_working}$, a shunt resistor was added between the electrode and OPA1. After scaling, the differential voltage at the resistor represents the current flowing through it. As the sensor impedance can vary over multiple decades, the shunt resistor also has to be able to scale in a wide range to achieve good measurement accuracy. Figure 2.7 shows how this scalable resistor is implemented. Nine resistors ranging from 1 kΩ to 10 MΩ are connected to the working electrode on one side. Switches on the other side connect the resistors to the output of OPA1. The problem with this is that the switches for the low-ohmic resistors have to be rather wide to be able to carry the full 1 mA current when needed. When small currents in the nanoampere range should be

measured these switches generate considerably large leakage currents which would deteriorate the measurement results. To omit this leakage nonstandard Transmission Gates (TGs) were used. OPA4 generates a replica of $V_{sens\_working}$ called $V_{sens\_working\_guard}$ which is subsequently used for guarding. Three switches are used so that when a switch should be non-conductive the voltage across one of its sub-switches is set to zero or just the offset voltage of OPA4. This way leakage current still flows through the other sub-switch, but this current is driven by OPA1 and cannot influence the voltage drop across the resistor which is actually used for the measurement. As at the same time the voltage directly at the resistors has to be measured, three additional sub-switches have to be added to avoid leakage. A measurement directly at the output of OPA1 would yield a big error as this voltage is dependent on the voltage drop across the switches.

Due to the higher voltages of the analog blocks in respect to the bus system, level shifters and a dedicated power switch P1 were implemented for this sensor front-end. Two analog multiplexers make it possible to select the voltages of the three electrodes and the voltage at the shunt resistor. As these voltages can exceed the input voltage range of the downstream analog multiplexers and ADC, another amplifier, OPA3, with a resistive divider and a selectable scaling factor is necessary.

Chapter 3

Switched Capacitor Bandgap

3.1 Introduction

In order to measure electrical quantities accurately, a reference to which to compare the measurements is indispensable. Operating conditions such as temperature or supply voltage should not have an impact on the value of the reference quantity. Achieving a suitable solution in a CMOS process with its very few building blocks can be hard, thus the topic of reference circuits is one of the most researched in circuit design. Mostly bandgap circuits are used to generate the reference voltages but all the known architectures have their limitations. Nevertheless, bandgap circuits are an essential building block for most analog and digital integrated systems. As system voltages go down with the scaling of devices, a reference circuit with a voltage of one bandgap voltage is not suitable anymore. A solution should be found to build a reference circuit for low voltage operation and ultra-low power consumption while maintaining good accuracy and small die area.

This chapter gives a short explanation of the two most commonly used voltage reference circuits and introduces an architecture up to now rather rarely used. An improvement on this state of the art circuit is shown and a detailed analysis of the properties of the topology is given.

The improved architecture was implemented in several different configurations, of which three distinct ones and their specialties are explained in more detail in Section 3.2, 3.6 and 3.7.

3.1.1 Standard Bandgap

A common and simple way to implement a bandgap reference in a CMOS technology is shown in Figure 3.1. It is a version of the one found in [6], adapted to CMOS technology.

The reference voltage generated can be expressed as in (3.1.1). For good temperature behavior the reference voltage has to be very close to the bandgap voltage of silicon.

$$V_{\text{ref}} = V_{\text{pnp3}} + \frac{R_2}{R_1} V_T \cdot ln(m) \tag{3.1.1}$$

3.1.2 Low Voltage Bandgap

A solution to the pressing low voltage compatibility requirement was provided by [9, 10], with a circuit topology as can be seen in Figure 3.2.

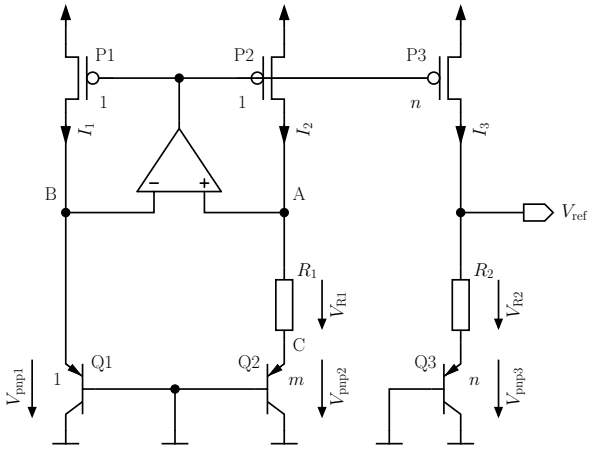


Figure 3.1: Schematic of standard bandgap

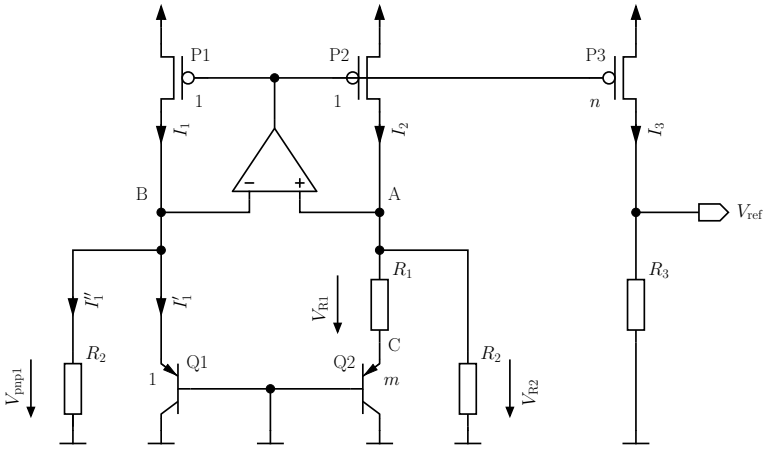


Figure 3.2: Schematic of low voltage bandgap

In contrast to the standard bandgap circuit, three additional resistors were added and the diode at the output removed. This architecture works by the principle of current summation, as Proportional to Absolute Temperature (PTAT) and Complementary to Absolute Temperature (CTAT) currents are generated and summed in the bias cell. By scaling these two parts in respect to each other a first order temperature compensation of the overall current can be achieved. This current is mirrored to another resistor, forming the output node, resulting in a reference voltage.

This topology makes it possible to scale the output reference voltage to arbitrary values as long as they are smaller than the supply voltage plus a saturation voltage. Thus when smaller voltages than the bandgap voltage of silicon are used, the supply voltage can also be lowered below this bandgap voltage. Equation (3.1.1) expresses the reference voltage.

$$V_{\text{ref}} = \frac{R_3}{R_2} \cdot \left[V_{\text{pnp1}} + \frac{R_2}{R_1} V_T \cdot ln(m) \right] \tag{3.1.2}$$

To be able to compare this structure to the subsequently presented switched capacitor bandgap, an already implemented version of this topology was used for simulations and also manufactured

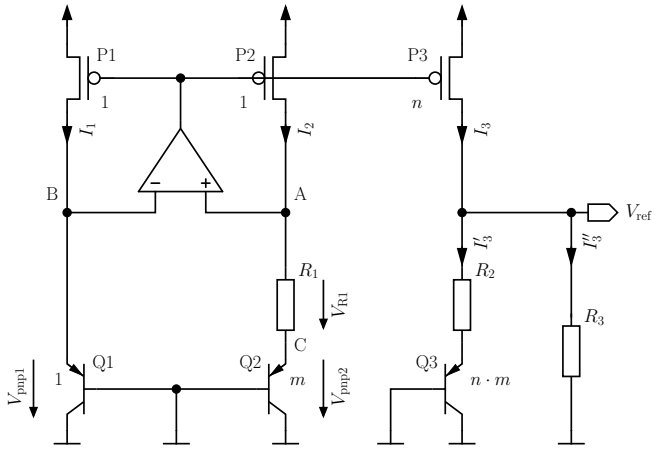


Figure 3.3: Schematic of variation of low voltage bandgap

and measured.

A variant of the circuit proposed in [9, 10] was proposed in [11] and is shown in Figure 3.3. The circuit is the same as in the standard bandgap but with an additional resistor R_3 connected at the output. This resistor draws a constant current I_3'' over temperature, since the output voltage can be considered constant. This subtracts from the PTAT current I_3 and leaves I_3' as a current that is linear to temperature but not proportional to absolute temperature anymore. This shifts the zero crossing point of the current I_3' from zero Kelvin up to a higher value. Negative currents are not possible, so the current for lower temperatures stays at close to zero. This has to be considered during the design as this can limit the minimum possible operating temperature. When R_3 is vastly bigger than R_2 the circuit behaves as the standard bandgap, which can achieve good precision and temperature stability. When the value of R_3 is lowered to also lower the reference voltage and the supply voltage limit, transistor Q3 begins to operate with a different current density as Q2 does. This worsens the temperature stability as also mentioned in [12]. Simulations show a more than five times worse temperature coefficient of this circuit when compared to the normal low voltage bandgap architecture when an output voltage of half the bandgap voltage is chosen. An actual implementation of the architecture can be found in [13] which confirms the bad temperature stability. A modification of the topology shown in Figure 3.3 [11] is proposed in [14] and [15]. The problem with the proposed modification of separating the PTAT and CTAT terms into two output branches and combining them with a resistive network is that large ratios between the resistors are needed to avoid influencing the PTAT and CTAT voltages themselves. To keep the total resistor size limited this requires an increase in current consumption. Due to the disadvantages of these variations of the low voltage bandgap, they were not further considered in this work but are included in the state of the art comparisons at the end of this chapter.

3.1.3 Switched Capacitor Bandgap

This architecture relies on the same principle as used in Section 3.1.1, of adding PTAT and CTAT voltages, but the addition and scaling is done with a switched capacitor circuit as can be seen in Figure 3.4 [16].

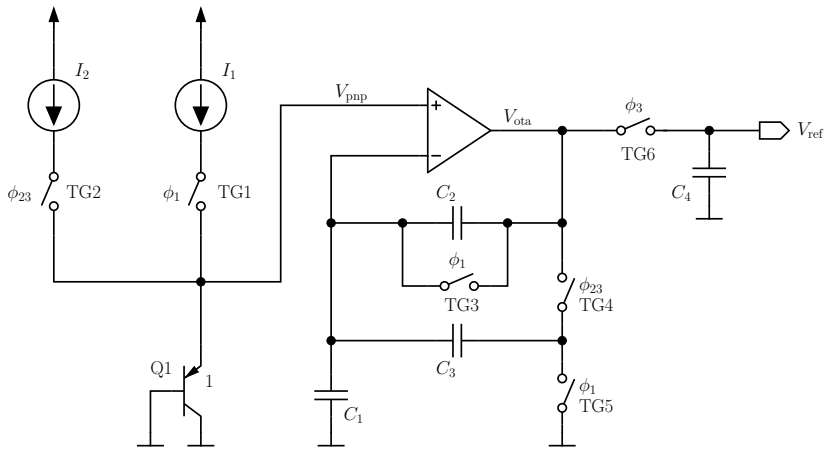
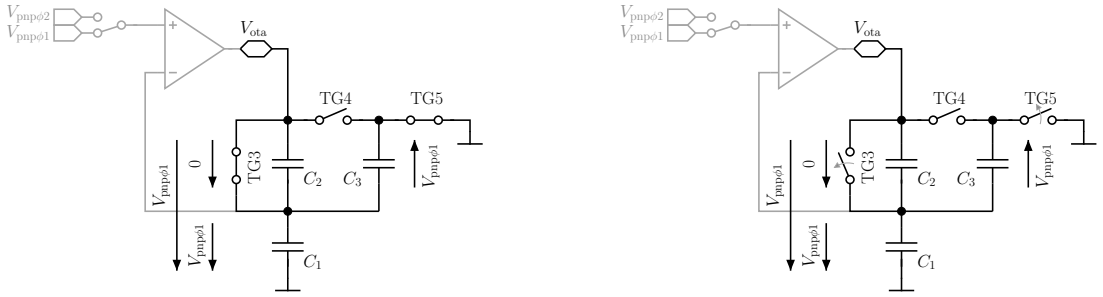


Figure 3.4: Principle of switched capacitor bandgap



(a) Precharge phase (ϕ_1)

(b) Floating interphase

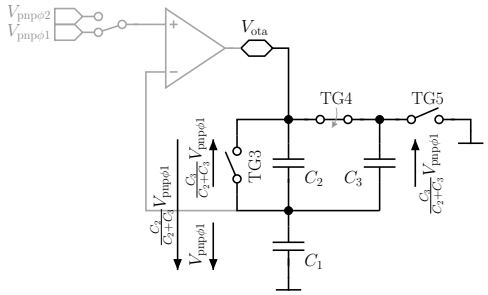
Figure 3.5: Switched capacitor operation 1

Early switched capacitor bandgap reference designs were published and patented by [17, 18]. Rather recently the topic was picked up again and a few new improvements were published [16, 19, 20, 21, 22, 23, 24]. All these publications use a bipolar transistor or a MOSFET in a time multiplexed manner with two different drive currents. It is also possible to keep the excitation current constant but vary the amount of transistors that share the current to get two voltages with slightly different temperature behavior. In Section 3.2 an improvement over these state-of-the-art circuits is shown by eliminating the need for a switched reference device.

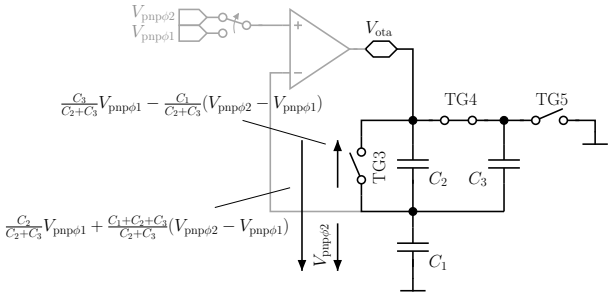
All switched capacitor circuits use a clock signal and operate in multiple phases. For this reference a total of 3 different phases is necessary to complete a single cycle.

The circuit starts in phase 1 ($\phi1$) with the switches configured as can be seen in Figure 3.5a. In this precharge phase transmission gate TG3 is conductive, resulting in the Operational Transconductance Amplifier (OTA) operating as a buffer trying to force the same voltage at its output as at its positive input which is the voltage $V_{pnp\phi1}$. Also, due to TG3 being conductive, C_2 gets discharged while C_1 and C_3 get charged to the voltage residing on the output node of the OTA.

During the switchover to phase 2 ($\phi2$) two interphases are run through. The first, the floating interphase, is a very brief moment in time only a few logic gate delays long where TG3 and TG5



(a) Charge redistribution interphase



(b) Multiplication phase (ϕ_2)

Figure 3.6: Switched capacitor operation 2

become non-conducting, placing the circuit in a floating state where all the vital node voltages are preserved. Second, the charge redistribution interphase takes place. TG4 gets conductive switching C_2 and C_3 in parallel. As they were charged to different voltage levels during phase 1, a charge redistribution process takes place. Since C_3 was flipped around, a negative voltage with respect to the output of the OTA resides, effectively subtracting voltage from its output but keeping the voltage on the negative input constant. Since the negative input voltage stays constant, the OTA has no differential input voltage and thus does not actively force a different output voltage. At this point in time the voltage at the output of the OTA can be expressed by Equation (3.1.3).

$$V_{\text{ota}} = V_{\text{pnp}\phi1} - \frac{C_3}{C_2 + C_3} \cdot V_{\text{pnp}\phi1} = \frac{C_2}{C_2 + C_3} \cdot V_{\text{pnp}\phi1} \tag{3.1.3}$$

It can be seen that the voltage V_{ota} can be scaled in value between a lower boundary of zero when C_2 is significantly smaller than C_3 and an upper boundary of $V_{\text{pnp}\phi1}$ when C_2 is significantly larger than C_3. This scaled voltage of $V_{\text{pnp}\phi1}$ keeps the same temperature behavior, thus it is a CTAT voltage. In phase 2, as can be seen in Figure 3.6a, the positive input voltage of the OTA is changed to $V_{\text{pnp}\phi2}$, which is higher than $V_{\text{pnp}\phi1}$, and the voltage difference between them shows a PTAT behavior. The OTA reduces its input differential voltage by increasing the voltage at its output, which is fed back to the negative input via a capacitor network. The attenuation of the feedback network results in a multiplication of the voltage jump at the input of the OTA:

$$\Delta V_{\text{ota}} = \frac{C_1 + C_2 + C_3}{C_2 + C_3} \cdot (V_{\text{pnp}\phi2} - V_{\text{pnp}\phi1}) \tag{3.1.4}$$

As this jump is added to the value that was stored on the output of the OTA the new and final voltage becomes:

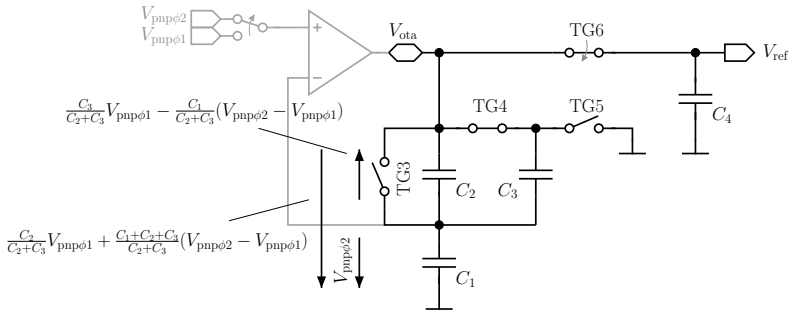


Figure 3.7: Switched capacitor operation 3 - storage phase (ϕ_3)

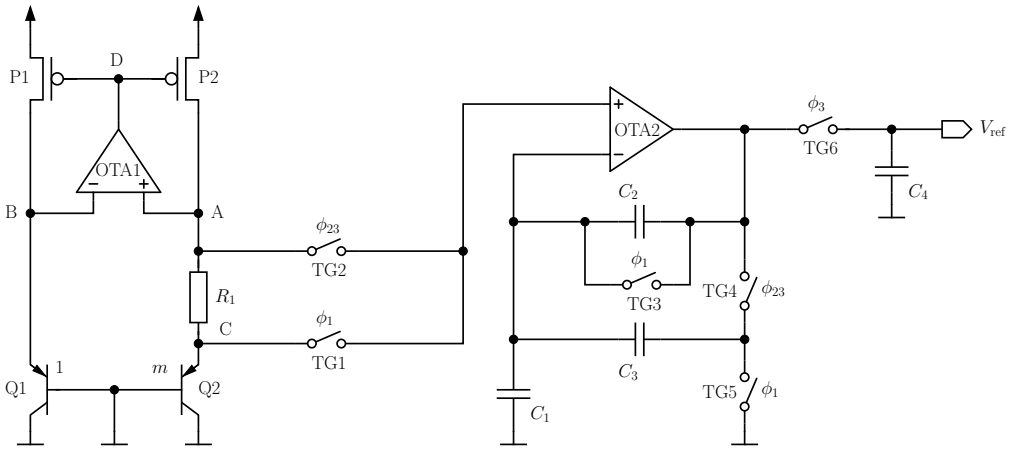


Figure 3.8: Simplified schematic of the proposed reference circuit

$$V_{\mathrm{ota}} = \frac{C_2}{C_2 + C_3} \cdot V_{\mathrm{pnp}\phi 1} + \frac{C_1 + C_2 + C_3}{C_2 + C_3} \cdot (V_{\mathrm{pnp}\phi 2} - V_{\mathrm{pnp}\phi 1}) \tag{3.1.5}$$

Since the voltage V_{ota} is not constant over time but a continuous reference voltage at the output of the reference block is desired, a third phase ($\phi 3$), the storage phase, is introduced. TG6 becomes conductive, connecting C_4 to the output of the OTA, charging it to the reference voltage.

3.2 General Purpose Low Power, Low Voltage Switched Capacitor Bandgap

The following subchapter is mainly taken from [25] (own publications).

This section describes an implementation of the afore-mentioned switched capacitor bandgap with all its necessary sub-blocks. The implementation represents a solid general purpose reference circuit that can be used in many applications. An oscillator is integrated into the circuit to allow an operation independent of other blocks. The total current consumption is in the range of 180 nA at room temperature. More specialized implementations are shown in Section 3.6 with an ultra-low power version with just 25 nA current consumption and a version designed in a 65 nm process and optimized for short start-up time in Section 3.7.

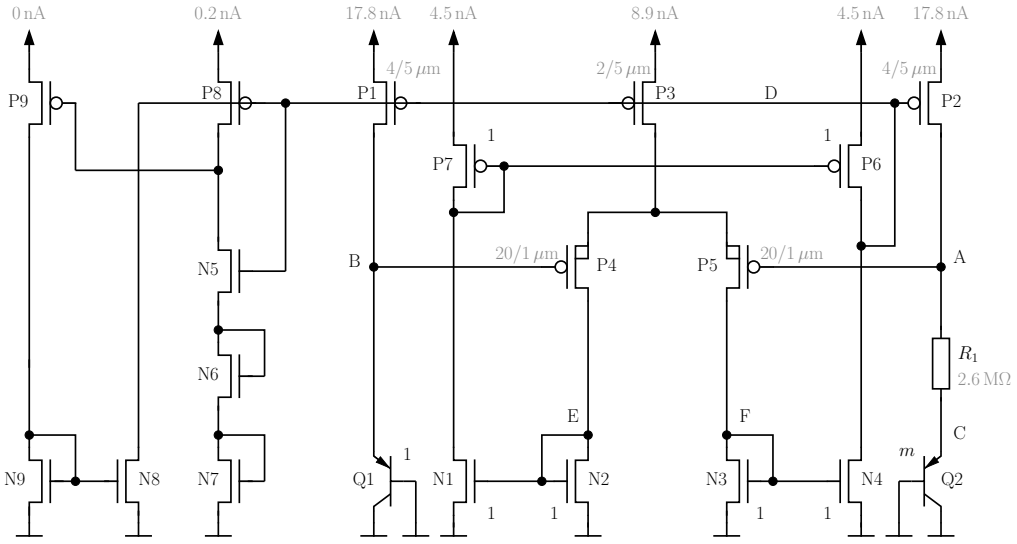


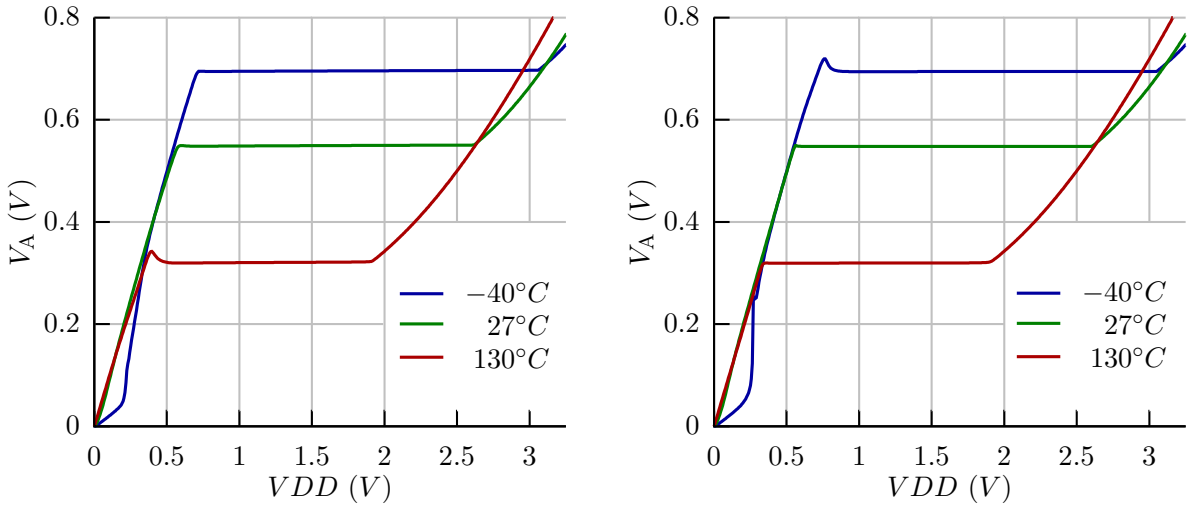
Figure 3.9: PTAT bias cell

The topology of the proposed bandgap circuit is shown in Figure 3.8 and a layout plot in Figure A.7. A standard bandgap core circuit, the so called PTAT cell, in combination with a start-up circuit provides bias currents and voltages as described in Section 3.2.1. Several transmission gates and capacitors work together with the operational transconductance amplifier OTA2 as a voltage multiplier and feed the generated reference voltage to the output capacitor C4. OTA2 is a class-AB amplifier and is described in more detail in Section 3.2.3. The oscillator which is built into the system is described in Section 3.2.4 and feeds a small digital part which generates multiple signals suitable for the transmission gates.

3.2.1 Bandgap Core

This cell is a standard PTAT cell. It contains OTA1, which is composed of the transistors N1 through N4 and P3 through P7 as shown in Figure 3.9. Its purpose is to minimize the voltage difference between node A and node B. This is possible for two operating points, of which only one is allowed for correct operation. To rule out the unwanted point, which is when both nodes A and B are at zero Volts, a start-up circuit is added. The transistors P8 and N5 are operating as an inverter monitoring the main gate voltage of the p-channel transistors at node D. N6 and N7 limit the maximum current that can flow through the inverter. If the voltage at the main gate is too high, almost no current is flowing through the whole circuit and P8 is less conductive than N5. This results in a low gate voltage of transistor P9, which sinks a start-up current through the current mirror N9 and N8 from the main gate line D, and the circuit is forced out of the unwanted operating point. During normal operation at 1.2 V supply voltage, room temperature and a nominal process, only 0.2 nA flow through the main start-up branch.

OTA1 is implemented with PMOS transistors P4 and P5 as a differential pair. Simulations were also performed with OTA1 converted to NMOS transistors as a differential pair. The resulting voltages of V_A over a supply voltage sweep at three temperatures can be seen in Figure 3.10. Only if the supply voltage is high enough for V_A to become constant a good reference voltage can be



(a) NMOS differential pair

(b) PMOS differential pair

Figure 3.10: PTAT bias cell VDD behavior

generated. At room temperature for both realizations the minimum supply voltage needed is at about 600 mV. For lower temperatures the CTAT voltage across diode Q2 increases, resulting in a higher minimum supply voltage requirement. Both versions show a slight overshoot of voltage V_A at either high or low temperatures, which can cause a slightly too high reference voltage at the output when the supply voltage is slightly below the required minimum. As the circuit is designed to operate at supply voltages up to 1.5 V, the start-up circuit has to work up to this voltage. The simulation results show an abrupt change of slope of V_A when the supply voltage gets too high. The point of this transition has to be above the intended maximum supply voltage, which was shown to be the case over the full temperature range.

As an NMOS differential pair does not result in a clear improvement of supply voltage range, but needs an additional current path as biasing from the NMOS side is needed, the PMOS variant was implemented. The transistors P4 and P5 are rather wide and operate in weak inversion. This allows them to have a small V_{GS} which maximizes the compatible voltage supply range.

When the circuit is operating in the desired operating point, Equation (3.2.1) describes the current flowing through each of the two diodes and Equation (3.2.2) describes the voltage drop across the resistor R_1.

$$I_Q = \frac{V_\mathrm{T} \cdot ln\,(m)}{R_1} \tag{3.2.1}$$

$$V_{R_1} = V_A - V_C = V_\mathrm{T} \cdot ln\,(m) \tag{3.2.2}$$

The overall current consumption should be very low, and to also keep the area small a small value of R_1 is anticipated. Therefore the only possible solution is to lower the value of m which is the area factor between the two pnp-diodes. For this implementation a factor m of six was chosen. For standard bandgaps low values of m would have the disadvantage that the resistor at the

output node would get bigger in order to keep the multiplication factor of PTAT to CTAT voltage constant. In this topology no resistor is needed at the output, thus this problem is irrelevant. Nevertheless a small factor m has other disadvantages, like an increased influence of OTA1's offset voltage and increased noise in the switched capacitor multiplication process. Thus a factor m of six poses a reasonable value.

As there is only one resistor R_1 in the design there is no need to match it to any other resistor, which simplifies the layout and makes the design more robust.

The cell provides complementary to absolute temperature voltages at the nodes A, B and C and a proportional to absolute temperature voltage difference between node A and C shown in (3.2.2). The voltages at the nodes E and F are also used to bias NMOS Transistors of the same size to get bias currents as can be seen in Section 3.2.3 and Section 3.2.4.

3.2.2 Transient Operation

The circuit operates according to the principle explained in Section 3.1.3, however the durations of the three clock phases differ. $\phi 3$ is two times as long as $\phi 1$ and $\phi 2$, giving OTA2 more time to charge the capacitor C_4 at the output. This results in a faster start-up time and a lower impedance of the reference voltage.

Equation 3.2.3 gives the output voltage. C_1 to C_3 are realized using unit elements to improve matching with a common centroid layout. Each unit element is 12 μm times 12 μm in size and uses one poly silicon layer as well as four metal layers to form a stacked capacitor. The wiring is done in metal 6 with metal 5 in between to minimize parasitics. The capacitance of each unit element was extracted from the layout and sums up to 70 fF. C_2 and C_3 consist of one unit element each while C_1 consists of twelve.

$$V_{\text{ref}} = \frac{C_2}{C_2 + C_3} \cdot V_{\text{C}} + \frac{C_1 + C_2 + C_3}{C_2 + C_3} \cdot V_{\text{T}} \cdot ln\,(m) \tag{3.2.3}$$

Equation 3.2.3 can be rewritten with a global scaling factor and by inserting Equation 3.2.2 giving Equation 3.2.4.

$$V_{\text{ref}} = \frac{C_2}{C_2 + C_3} \cdot \left[V_{\text{C}} + \frac{C_1 + C_2 + C_3}{C_2} \cdot V_{\text{T}} \cdot ln\,(m) \right] \tag{3.2.4}$$

As C_2 and C_3 were implemented to be the same size, the scaling factor becomes 1/2, which gives a reference voltage of half the bandgap voltage. The temperature voltage is scaled with a factor of 25.08 with respect to the voltage V_C to give an as flat as possible voltage behavior over temperature.

3.2.3 Class-AB OTA with nonlinear current mirror

OTA2, which is shown in Figure 3.11, has to ensure fast settling times at its output node during switching. The connected loads are of purely capacitive nature. The input voltage range has to have a lower limit of at most the voltage at node C, which is one PNP-diode voltage. This can be accomplished in the given process with the transistors N14 and N15 implemented as n-channel transistors as a differential pair, since their threshold voltage is well below the diode voltage.

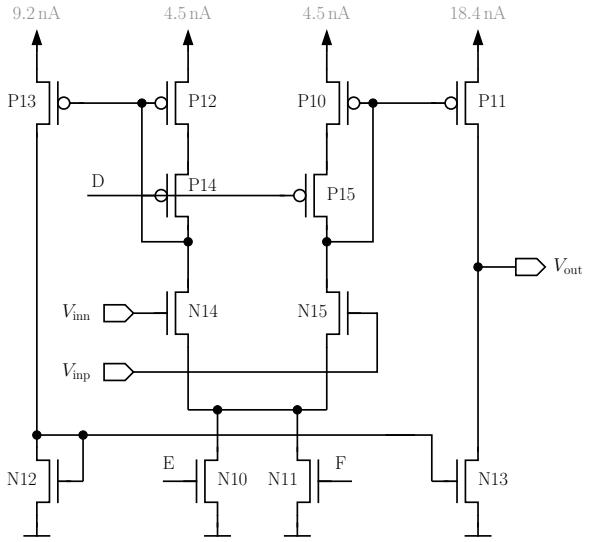


Figure 3.11: Class-AB OTA with non-linear current mirror

To speed up settling, two additional transistors, P14 and P15, were added to the high side current mirrors [26], which turn the amplifier into a class-AB amplifier. These two transistors need to be biased, which is easily possible by using the node voltage D from the bias cell. With this addition the mirrored currents can increase well over the set bias current supplied by N10 and N11 when a differential voltage is applied to the OTA's inputs. This results in more current sunk or sourced to the output node when needed. The idle current consumption, though, stays almost the same. The slight increase which arises has to be considered during design. The biasing of this non-linear current mirror can be tuned during design. A high voltage at the gates of P14 and P15 leads to improved settling but also to instability and huge offset voltages.

To further save current the current source of the OTA is implemented by N10 and N11, which supply the same amount of current as that flowing through N2 and N3 from the PTAT bias cell. Additionally, the output side, consisting of N13 and P11, is implemented two times as wide as the internal side N12 and P13, giving more current drivability.

3.2.4 Relaxation Oscillator

For switching the capacitors an external clock has to be provided, or an oscillator has to be present in the system or implemented directly into the reference circuit. As the bias cell in this implementation already supplies some vital resources for an oscillator, it was decided to implement it directly and deeply into the bandgap circuit itself.

A relaxation oscillator suits this circuit's needs best, and therefore it was implemented as depicted in Figure 3.12. A comparator compares the voltage across C_5 to the voltage of either node A or C. Depending on the current state of the voltage at C_5, it has to be charged to the value of node A or discharged to the lower value C. The charging and discharging happens with the same current as generated in the bias cell. As this current is proportional to temperature, a big variation of the frequency would be the result. To avoid this, the switching thresholds also vary over temperature, showing a proportional increase of the voltage difference between node A and C

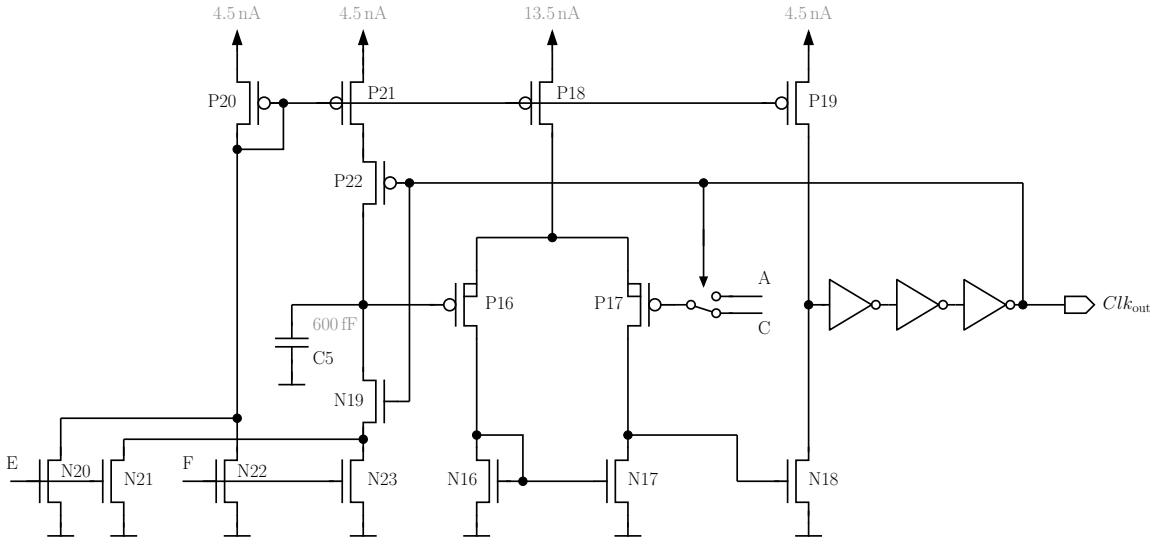


Figure 3.12: Relaxation oscillator

over temperature. This would give a perfectly flat frequency over temperature if the comparator itself had no influence, but its delay time adds to the cycle time as well. An increasing bias current should decrease the delay time, which should result in an increasing frequency over temperature as also shown in the measurement results. As with OTA2 the comparator and charging of C_5 is biased by the node voltages E and F. It has to be ensured that a ripple generated by the oscillation does not get fed back to the bias cell. Large capacitors on these bias nodes are also not ideal since they would increase the area as well as start-up time. Due to this the transistors P18, P19 and P21 cannot be biased by node voltage D but have to be biased by a separated bias path with N22 and P20.

The addition of the oscillator adds only a marginal die area of $0.000096\,\mathrm{mm}^2$, as for the capacitor C_5 the dummy capacitors surrounding the matched capacitor array composed of C_1 through C_3 are used. The comparator itself can be very small because offset voltages affect the upper threshold voltage as well as the lower. The oscillator can be found in Figure A.7 in area number 6.

3.2.5 Timing Unit

The timing unit steers the transmission gates TG1 to TG6 and has only the oscillators clock output as input. The circuit is shown in Figure 3.13. The flip-flops FF1 to FF4 form a shift register with the output of NOR1 at its very beginning. It supplies a one to the shift register whenever FF1 to FF3 have a zero at their outputs. This results in a single one being shifted through the registers. The pattern repeats after four falling edges at the clock input. The current consumption of the digital timing unit is a simulated average of 13 nA at room temperature, 1.2 V supply voltage and the standard clock rate of 57 kHz.

The output of FF1 could be used as signal $\phi 1$ but an additional AND-gate AND1 is added to ensure that $\phi 3$ goes to low state before $\phi 1$ goes to high. If this timing issue was not considered, an unnecessary voltage ripple at the reference output could be possible at the switchover from state $\phi 3$ to $\phi 1$, as a direct connection of the reference output to ground through TG4, TG5 and TG6 is

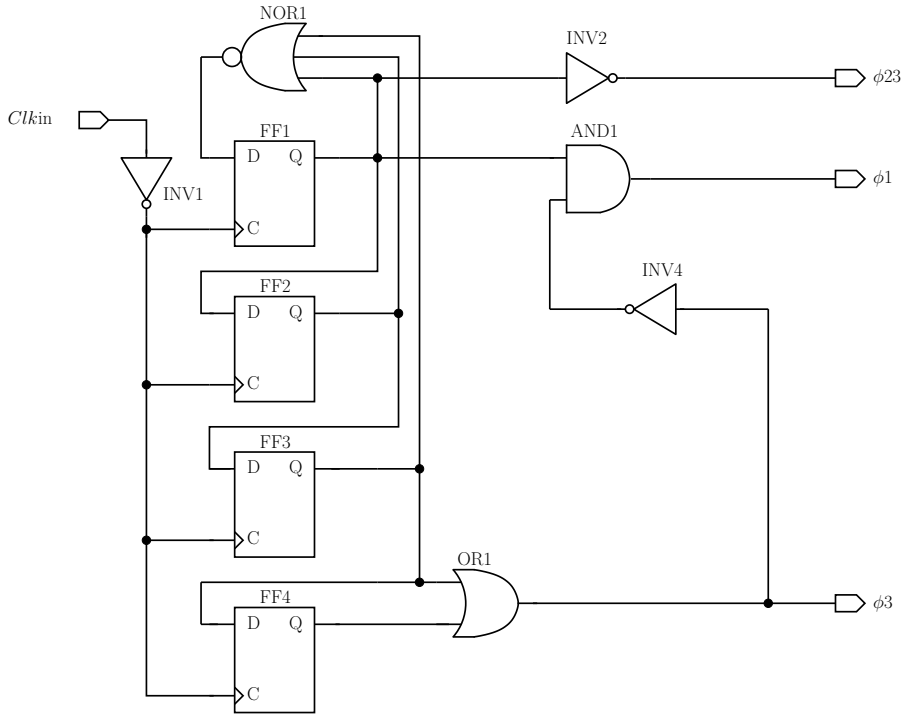


Figure 3.13: Timing unit

possible. $\phi 3$ itself is an OR-combination of the outputs of FF3 and FF4. As a result this phase is two times as long as $\phi 1$ or $\phi 2$. When $\phi 1$ is negated by INV2, the signal $\phi 23$ is generated, which is high during $\phi 2$ and $\phi 3$.

Two additional more specialized solutions of the timing unit were also implemented. An ultra-low power version with just one flip-flop is shown in Section 3.6 and a second configurable version was used for the test-bandgap, which can be seen in Figure A.5 in area 1.

3.2.6 Measurement Results

The circuit was implemented in an Infineon 130 nm standard CMOS process as can be seen in Figure A.7. It was put on a test chip together with a modified version of the switched capacitor bandgap for testing of noise properties and a continuous time low voltage bandgap according to 3.1.2. To be able to measure the high impedance reference voltages, an additional chopped output amplifier was attached. A serial configuration interface makes it possible to change the configuration. The layout of the test chip can be seen in Figure A.5.

Figure 3.14 shows the reference voltage plotted over the supply voltage. One measurement result of the switched capacitor bandgap circuit at room temperature with a typical sample is shown. For comparison the simulation results at room temperature, $-40\,^{\circ}\mathrm{C}$ and $130\,^{\circ}\mathrm{C}$ are added. Furthermore a simulation result of the continuous time low voltage bandgap, which has a standard output voltage of 500 mV, is added. The simulations do not cover the whole supply voltage range since at low voltages either the oscillator does not start or the start-up circuit does not work, resulting in a floating output or voltages very close to zero.

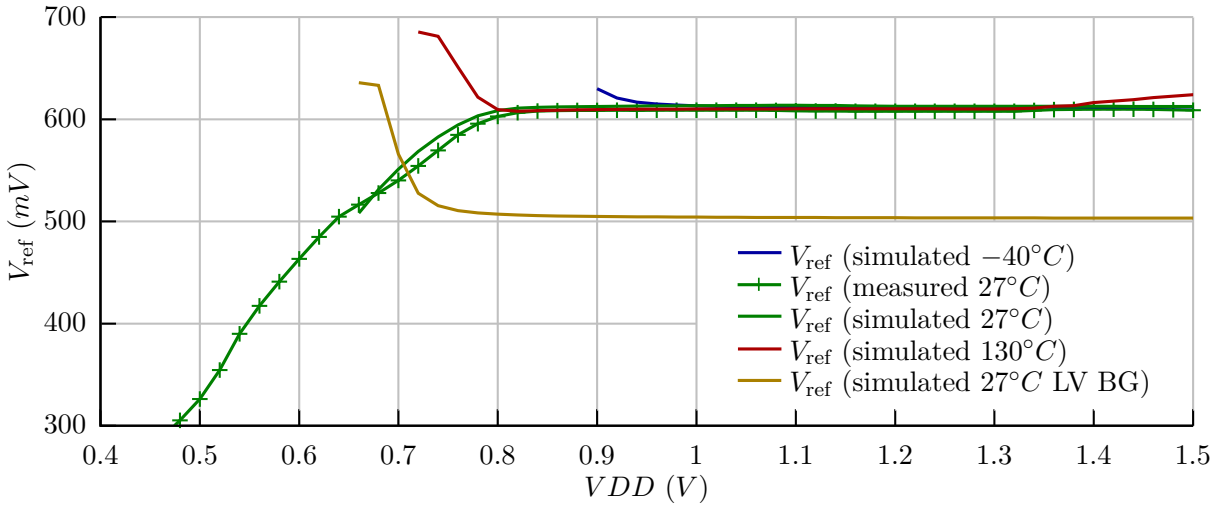


Figure 3.14: Measured reference voltage as a function of the power supply voltage

It can be seen that the switched capacitor bandgap circuit needs supply voltages of above 850 mV to work properly at room temperature. Under these conditions its output voltage stays within a ±1 mV band for supply voltages of up to 1.5 V. Simulation and measurement results fit quite well. As shown in the simulations, high temperatures do not help significantly to reduce the necessary supply voltage, though low temperatures have an effect, as about 950 mV are needed at −40 °C. At high temperature and high supply voltages leakage becomes severe and results in a slight increase of the output voltage. At supply voltages very close to the minimal possible value the oscillator might oscillate very slowly, thus the output voltages might float for long periods of time. Due to this they exhibit either an increase or decrease of value until the oscillation finally stops and no meaningful voltage can be measured any more.

The continuous time low voltage bandgap seems to show a slightly better minimum supply voltage requirement, though when a ±1 mV band is applied again the usable voltage range is just from 880 mV to 1.5 V.

To explore the output voltage to clock frequency dependency, a multiplexer is present in the switched capacitor bandgap implementation, which allows switching the clock of the system from the internal oscillator to an external one. This way, it is possible to supply a controlled clock signal via a pad to the circuit and to observe the output voltage. The results are shown in Figure 3.15. It can be seen that there is a very wide range of frequencies where the reference voltage is hardly influenced. If the frequency becomes too high, OTA2 cannot guarantee settling anymore, which results in a big error of the output voltage. At very low frequencies, below 1 kHz, leakage currents gain influence as the capacitors C1 to C3 are charged or discharged during operation. Multiple test chips were measured and show different behavior at these low frequencies. Some show an increase in reference voltage while others show a decrease. The internal oscillator frequency was designed to have a frequency at the upper limit of the usable frequency band. The intended frequency is about 55 kHz. A lower frequency would mean that the currents flowing in OTA2 could be decreased without compromising the reference voltage. Maximizing the switching frequency also

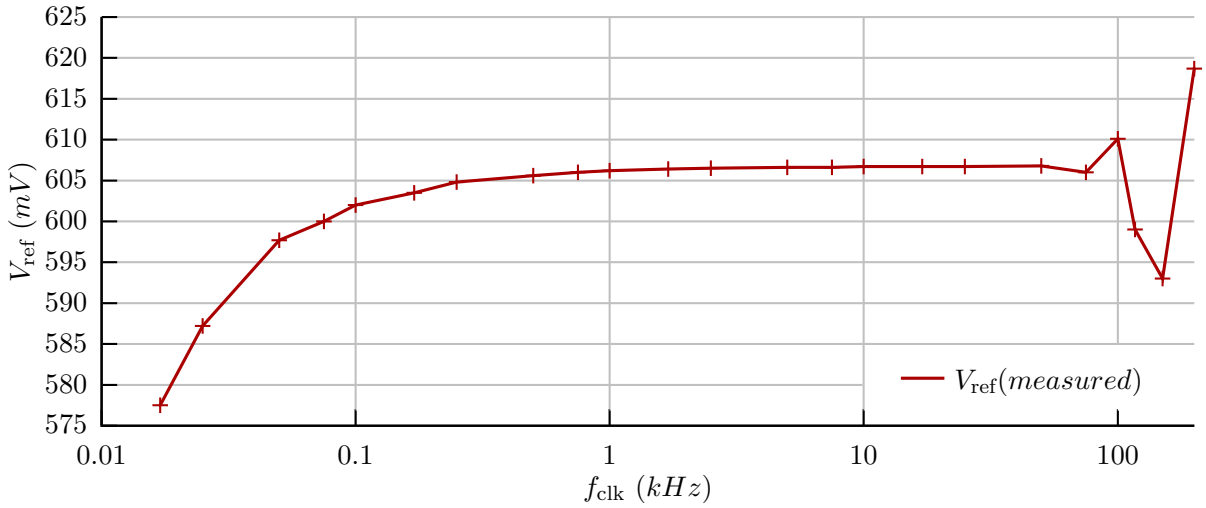


Figure 3.15: Measured reference voltage as a function of the clock frequency

minimizes start-up time which in this design is a nice to have feature. Other designs, as the for example the one presented in Section 3.7, had a specified maximum start-up time which had to be met.

The test chips were also fitted to a temperature forcing device and their behavior investigated at temperatures from −50 °C to 150 °C. The reference voltage in Figure 3.16 shows a second order curve as is to be expected for a bandgap circuit without second order compensation. Measurement and simulation differ a bit as the measurement results show a stronger curvature than the simulations. The absolute voltage level of the measurements varies from chip to chip as there is no trimming included in this version. A table of their mean absolute values at room temperature can be found in Table 3.1.

In total the measured values give a temperature coefficient of 42 ppm over the commercial temperature range (0 °C to 70 °C), 58 ppm over the industrial range (−40 °C to 85 °C) and 41 ppm over the full measured range (−50 °C to 150 °C) which at the low end very closely covers the military standard (−55 °C to 125 °C) but extends even further at the high end.

The clock frequency shows a mostly linear behavior over temperature with a coefficient of 1.1 ‰/°C as depicted in Figure 3.17. The coefficient could be reduced by supplying more current to the comparator in the relaxation oscillator at the price of increased overall power consumption. In ultra-low power systems the clock signal may be re-used to feed a polling counter instead of implementing a second oscillator. However as long as the frequency stays in a certain very wide range the output reference voltage is hardly influenced.

Table 3.1 shows a list of eleven measured samples from one wafer with calculated average values and standard deviations from measurements as well as from simulations. Good accordance of measurement to simulation results can be observed for absolute values as well as mismatch.

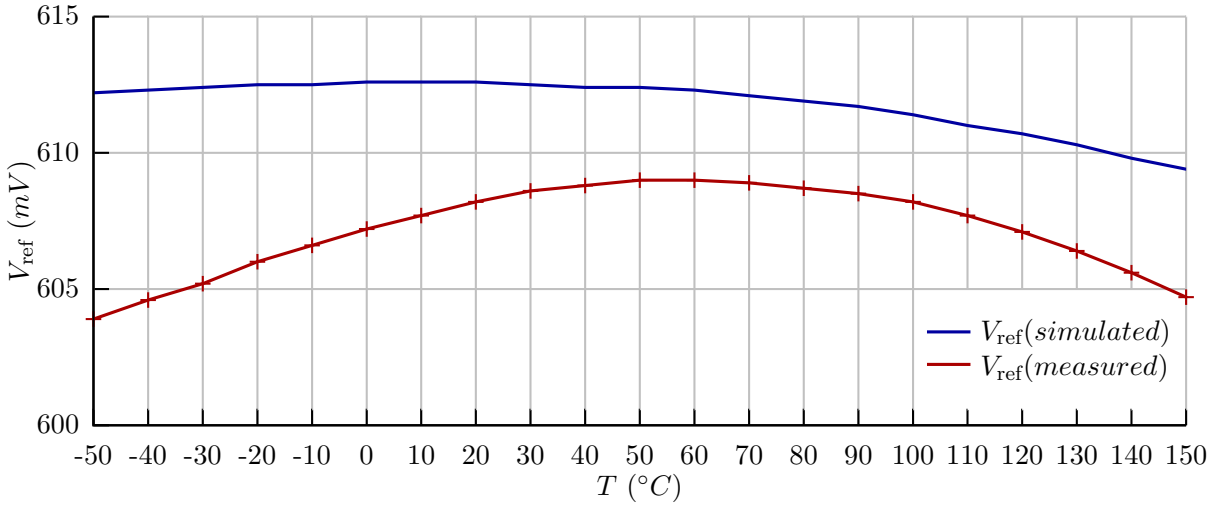


Figure 3.16: Measured reference voltage as a function of the temperature

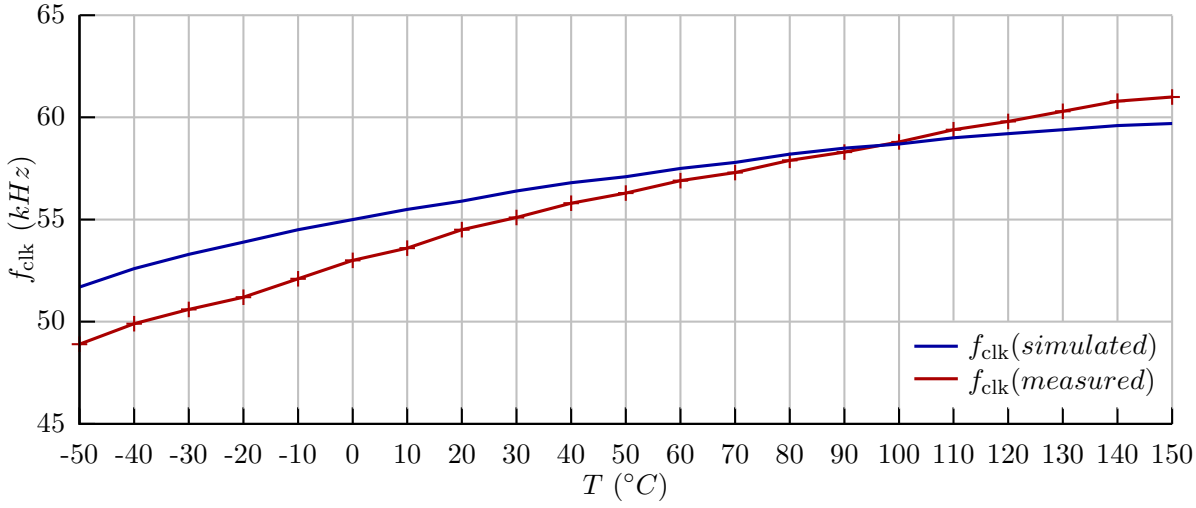


Figure 3.17: Measured frequency of the relaxation oscillator as a function of the temperature

Table 3.1: Statistical deviations of switched capacitor bandgap test chips

Test chip	V_{ref} (mV)	f_{clk} (kHz)	IDD_{bg} (nA)	IDD_{osc} (nA)	IDD_{total} (nA)
1	617.2	62.76	131	54	185
2	609.5	54.62	116	53	169
3	607.8	56.59	111	66	177
4	616.1	53.15	113	58	171
5	626.9	58.35	133	62	195
6	610.6	61.20	127	61	188
7	610.3	59.87	133	53	186
8	613.5	51.61	126	55	181
9	620.8	65.28	128	65	193
10	614.4	57.53	124	50	174
11	613.7	59.92	125	71	196
μ	615.2	58.26	124	58.9	183
σ (abs.)	5.42	4.13	7.71	6.61	9.55
σ (rel.)	0.88%	7.09%	6.20%	11.22%	5.21%
μ (simulated)	612.4	56.51	116	54.2	170
σ (abs.; simulated)	4.86	4.10	7.52	6.56	11.35
σ (rel.; simulated)	0.79%	7.26%	6.47%	12.10%	6.66%

3.3 Area Estimation

In this section a mathematical model is developed to help designers and concept engineers to choose the best fitting architecture under certain performance constraints.

There are a many trade-offs to be considered when a bandgap circuit is designed: area on die, required metal stack height, current consumption, start-up time, supply voltage range, power supply rejection ratio, supply voltage dependency, reference voltage flexibility, output impedance, temperature coefficient, temperature range, untrimmed accuracy, trimming capabilities, bias current generation, noise, long term stability and robustness. Complex relations arise between them and only a few of them can be discussed here.

For now we assume the circuit should work stand alone, so no bias currents or voltages are available, though we do not want to consider the start-up circuit so we assume the circuit is always in the intended operating point. The two presented continuous time bandgap structures from Section 3.1.1 and 3.1.2 should be compared to the switched capacitor principle from Section 3.1.3 with the improvements and bias cell shown in Section 3.2.

Also only three trade-offs of design are considered: active area, current consumption and supply voltage range. From the descriptions of the three bandgap architectures it is clear that the standard bandgap can only be used when the required supply voltage can stay above one bandgap voltage plus one saturation voltage. Nevertheless it is interesting to compare the circuits for certain current consumption budgets and investigate which architecture allows building the least area intensive circuit.

To derive the current consumption of each architecture more assumptions are needed to simplify the models. First, it is assumed that the OTAs used in the design do not contribute to the current consumption. As no restrictions concerning dynamic properties of the circuits are applied, this is legitimate as the OTAs in all circuits have no resistive loads and no leakage currents to drive. Also, with the bias cell of the bandgap working, it would be possible to generate arbitrarily small bias currents for the OTAs by using an extremely one-sidedly scaled current mirror. Second, the oscillator of the switched capacitor bandgap circuit also consumes no current, as without leakage the oscillation frequency could be set as low as desired, resulting in an ever-decreasing current consumption.

To be able to calculate the element values for the three circuits the ratio between CTAT and PTAT voltages to achieve temperature compensation first has to be derived. The voltage across a bipolar diode can be described as follows [27]:

$$V_Q = n_e V_T \cdot ln(I_Q/I_S) \tag{3.3.1}$$

With n_e being the ideality factor or emission coefficient, I_Q the current through the diode and I_S the saturation current of the diode. V_T, the temperature voltage is defined by:

$$V_T = kT/q \tag{3.3.2}$$

Where k is the Boltzmann constant, T is the absolute temperature of the pn-junction, and q is the magnitude of charge on an electron. As shown in [28] it is possible to calculate the temperature behavior of Equation 3.3.1 which gives Equation 3.3.3.

$$\frac{\partial V_Q}{\partial T} = \frac{V_Q - V_T \cdot (4 + m_p) - E_g/q}{T} \tag{3.3.3}$$

Where m_p is a process parameter and $E_g \approx 1.12\,\text{eV}$ is the bandgap energy of silicon. The same can be applied to Equation 3.3.2:

$$\frac{\partial V_T}{\partial T} = k/q \tag{3.3.4}$$

The temperature behavior of the temperature voltage computes to $0.08614\,\text{mV/K}$ while the voltage V_Q varies by approximately $-2\,\text{mV/K}$. Now the gain that is needed to be applied to the temperature voltage can be calculated:

$$Gain = -\frac{\partial V_Q/\partial T}{\partial V_T/\partial T} = -\frac{[kT/q \cdot (n_e \cdot log(I_Q/I_S) - (4 + m_p)) - E_g/q)]\,q}{kT} \tag{3.3.5}$$

It should be noted that all elements of Equation 3.3.5 are constant but I_Q. The temperature T is set to $300\,\text{K}$ to compare the architectures at room temperature.

To subsequently be able to calculate the area consumption, a few process dependent constants have to be known: the sheet resistance and minimum width of the layer the resistors are built with. For this comparison the resistors are made of poly-silicon as this material allows for the smallest area consumption for a certain resistance. Their path width was defined to be $600\,\text{nm}$ which is more than three times wider than the minimum width allowed by the design rules. This is done to keep yield high as huge resistors built with minimum width pose a serious thread for opens. The issue is due to the granular physical structure of poly-silicon.

The diodes are made of unit elements. To get a certain rational number of m, very many unit elements might be needed. To avoid this, and to get a smooth behavior of the model, it was defined that Q1 consists of one unit element and the other transistors can consist of any arbitrary real number of transistors. The area is determined by multiplying the amount of diodes with the area of one unit element diode. For an actual implementation m would have to be rounded to the closest integer number.

For the switched capacitor bandgap the capacitors are also considered. C_2 is determined to be the unit capacitor with a value of $70\,\text{fF}$ and a certain area which is needed to build a metal-oxide-metal capacitor. C_1 and C_3 again can scale to arbitrary values. In specific processes it might be possible to put special metal-insulator-metal capacitors at a top metal layer with high capacity densities reducing the total area consumption. It might also be possible to place these capacitors above other parts of the circuit, like the resistors, which would save quite a large amount of area. Nevertheless for this comparison it is assumed that everything lies next to each other and no special process features are available although it would be rather easy to adapt the model to these things.

The area of the OTAs should also be accounted. From multiple designs an approximate $750\,\mu\text{m}^2$ were determined for a symmetrical OTA with a reasonable offset voltage for a bandgap circuit. The standard and low voltage bandgap incorporate a single OTA while the switched capacitor bandgap uses two.

3.3.1 Standard Bandgap

As depicted in Figure 3.1 for the model the standard bandgap has only three paths of current consumption. The currents I_1 and I_2 can be described by Equation 3.3.6.

$$I_1 = I_2 = \frac{V_T \cdot ln(m)}{R_1} \tag{3.3.6}$$

Current I_3 is a version of I_1 and I_2 scaled by factor n. Thus the overall current consumption can be expressed as:

$$I_{\text{total}} = (2+n) \cdot \frac{V_T \cdot ln(m)}{R_1} \tag{3.3.7}$$

The voltage drop across R_1 can be expressed as:

$$V_{R_1} = V_T \cdot ln(m) \tag{3.3.8}$$

This PTAT voltage drop has to be amplified to get temperature compensation, since the value of R_2 can be expressed as follows:

$$R_2 = R_1 \cdot \frac{Gain}{n \cdot ln(m)} \tag{3.3.9}$$

This equation can be reformulated to give R_1.

$$R_1 = R_2 \cdot \frac{n \cdot ln(m)}{Gain} \tag{3.3.10}$$

Now Equation 3.3.10 can be inserted into Equation 3.3.7 which gives in combination with Equation 3.3.5 the final values for R_1 and R_2:

$$R_1 = (2+n) \cdot \frac{kT}{q} \cdot \frac{ln(m)}{I_{\text{total}}} \tag{3.3.11}$$

$$R_2 = \frac{-(2+n)}{n \cdot I_{\text{total}}} \cdot \left[\frac{kT}{q} \cdot (n_e \cdot ln(I_1/I_S) - (4+m_p)) - E_g/q\right] \tag{3.3.12}$$

The area is calculated as follows:

$$A_{\text{total}} = (R_1 + R_2) \cdot A_{\text{per }\Omega} + (1+m+n) \cdot A_{\text{per diode}} + 1 \cdot A_{\text{per OTA}} \tag{3.3.13}$$

3.3.2 Low Voltage Bandgap

The current consumption of the low voltage bandgap as in Figure 3.2 can be described as follows:

$$I_{\text{total}} = 2 \cdot \frac{V_T \cdot ln(m)}{R_1} + \frac{V_{\text{ref}}}{R_3} + 2 \cdot \left(\frac{V_{\text{ref}}}{n \cdot R_3} - \frac{V_T \cdot ln(m)}{R_1}\right) \tag{3.3.14}$$

The first term in Equation 3.3.14 describes the current flowing through the diodes Q1 and Q2, the second term represents the current through resistor R_3 and the last term defines the current through the two resistors R_2, which is the difference between the current through R_3 and the current through the diodes while taking into account the scaling factor n. This equation can be greatly simplified:

$$I_{\text{total}} = \frac{V_{\text{ref}}}{R_3} \cdot \left(1 + \frac{2}{n}\right) \tag{3.3.15}$$

From this and the introduction of a scaling constant $Scale$ to scale the bandgap voltage V_{bg} of approximately 1.25 V to the desired reference voltage V_{ref}, which was chosen to be 625 mV, R_3 can easily be calculated:

$$R_3 = \frac{Scale \cdot V_{\text{bg}}}{I_{\text{total}}} \cdot \left(1 + \frac{2}{n}\right) \tag{3.3.16}$$

R_2 can be calculated through the relation:

$$R_2 = R_3 \cdot \frac{n}{Scale} = \frac{n \cdot V_{\text{bg}}}{I_{\text{total}}} \cdot \left(1 + \frac{2}{n}\right) \tag{3.3.17}$$

R_1 can be expressed as:

$$R_1 = R_2 \cdot \frac{ln(m)}{Gain} = \frac{\frac{n \cdot V_{\text{bg}}}{I_{\text{total}}} \cdot \left(1 + \frac{2}{n}\right) \cdot ln(m) \cdot kT}{\left[\frac{kT}{q} \cdot (n_e \cdot ln\left(I_1'/I_S\right) - (4 + m_p)) - E_g/q\right] \cdot q} \tag{3.3.18}$$

where I_1' is represented by:

$$I_1' = \frac{\frac{kT}{q} \cdot ln(m)}{R_1} \tag{3.3.19}$$

It can be seen that if Equation 3.3.19 is inserted into Equation 3.3.18, R_1 still is dependent to itself. As this equation cannot be any further easily simplified analytically, although solutions exist [29], this means that only an iterative calculation is possible.

The area is calculated as follows:

$$A_{\text{total}} = (R_1 + 2R_2 + R_3) \cdot A_{\text{per }\Omega} + (1 + m) \cdot A_{\text{per diode}} + 1 \cdot A_{\text{per OTA}} \tag{3.3.20}$$

3.3.3 Switched Capacitor Bandgap

The current consumption of the switched capacitor bandgap as in Figure 3.8 with the shown bias cell is rather easy.

$$I_{\text{total}} = 2 \cdot \frac{\frac{kT}{q} \cdot ln(m)}{R_1} \tag{3.3.21}$$

This can be reformed to give the value of R_1, which is the only resistor in this design.

$$R_1 = 2 \cdot \frac{\frac{kT}{q} \cdot ln(m)}{I_{\text{total}}} \tag{3.3.22}$$

The reference output voltage is scaled with the same scaling factor as used for the low voltage bandgap.

$$V_{\text{ref}} = Scale \cdot V_{\text{bg}} = \frac{C_2}{C_2 + C_3} \cdot \left[V_C + \frac{C_1 + C_2 + C_3}{C_2} \cdot \frac{kT}{q} \cdot ln(m)\right] \tag{3.3.23}$$

Capacitor C_2 is set to one since it represents a single unit capacitor.

$$Scale = \frac{C_2}{C_2 + C_3} = \frac{1}{1 + C_3} \tag{3.3.24}$$

$$C_3 = \frac{1}{Scale} - 1 \tag{3.3.25}$$

$$Gain = \frac{C_1 + C_2 + C_3}{C_2} \cdot ln(m) \tag{3.3.26}$$

$$C_1 = -\frac{\left[\frac{kT}{q} \cdot \left(n_e \cdot ln\left(\frac{I_{\text{total}}/2}{I_S}\right) - (4 + m_p)\right) - E_g/q\right] \cdot q}{kT \cdot ln(m)} - \frac{1}{Scale} \tag{3.3.27}$$

The area is calculated as follows:

$$A_{\text{total}} = R_1 \cdot A_{\text{per }\Omega} + (1 + m) \cdot A_{\text{per diode}} + (C_1 + C_2 + C_3) \cdot A_{\text{per unitcap}} + 2 \cdot A_{\text{per OTA}} \tag{3.3.28}$$

As an overview all symbols used in the calculations are again listed in Table 3.2.

3.3.4 Comparison

The equations and constants were implemented into an easy to use MATLAB® program which calculates the area for many combinations of m and n over a sweep of the current consumption goal. A screen shot of the graphical user interface is shown in Figure 3.18. The environment settings can easily be changed to data taken from other process lines but significantly different results especially at low current consumptions are only to be expected with varying sheet resistance values of the resistors and their dimensions. The sweep range and granularity of m, n and current consumption are also configurable though care has to be taken with the granularity as calculation time easily surpasses several minutes for multiple thousands of points. The calculation can be done according to the equations derived in Section 3.3.1, 3.3.2 and 3.3.3 but a simplified model that uses a fixed *Gain* between PTAT and CTAT voltage is also available. This simple model speeds up calculation considerably since the calculation intensive diode behavior is neglected while giving results with only a minor error. To consider current consumption and area overheads in real implementations correction factors can be defined for each architecture separately. This way, for example, a 20 % area overhead accounting for start-up circuitry or a 50 % current consumption overhead accounting for the OTAs is possible. The subsequently discussed calculation results were performed with the complex calculation model, all correction factors set to one and a sufficiently high number of sweep points.

The resulting smallest areas for each total current consumption can be seen in Figure 3.19. As the areas mostly shrink with m getting closer to one, m was limited in the calculations to values greater than four as small values have a severe effect on the accuracy of the bandgap as mentioned earlier. The crosses represent actual implementations of bandgap circuits in the same Infineon C11 process. Due to the script calculating the minimum areas possible for every architecture it is not possible for an actual implementation to lie beneath its corresponding line without breaking any of the above specified requirements like limited m or resistor width.

Table 3.2: Summary of used symbols for area estimation

Symbol	Description
V_Q	Diode voltage
V_T	Temperature voltage
n_e	Emission coefficient
I_Q	Diode current
I_S	Diode saturation current
k	Boltzmann constant
T	Temperature
m_p	Process parameter
E_q	Bandgap energy of silicon
q	Magnitude of charge on an electron
$Gain$	Amplification factor of PTAT voltage
n	Ratio of current mirror at output branch
m	Bipolar transistor ratio
I_{total}	Total current consumption of circuit
A_{total}	Total area of circuit
$A_{per\Omega}$	Area of $1\,\Omega$ resistor on die
$A_{perdiode}$	Area of one bipolar diode on die
A_{perOTA}	Area of one ordinary OTA on die
V_{bg}	Unscaled output voltage of silicon based bandgap circuit
$Scale$	Factor for scaling the output reference voltage
V_{ref}	Reference output voltage

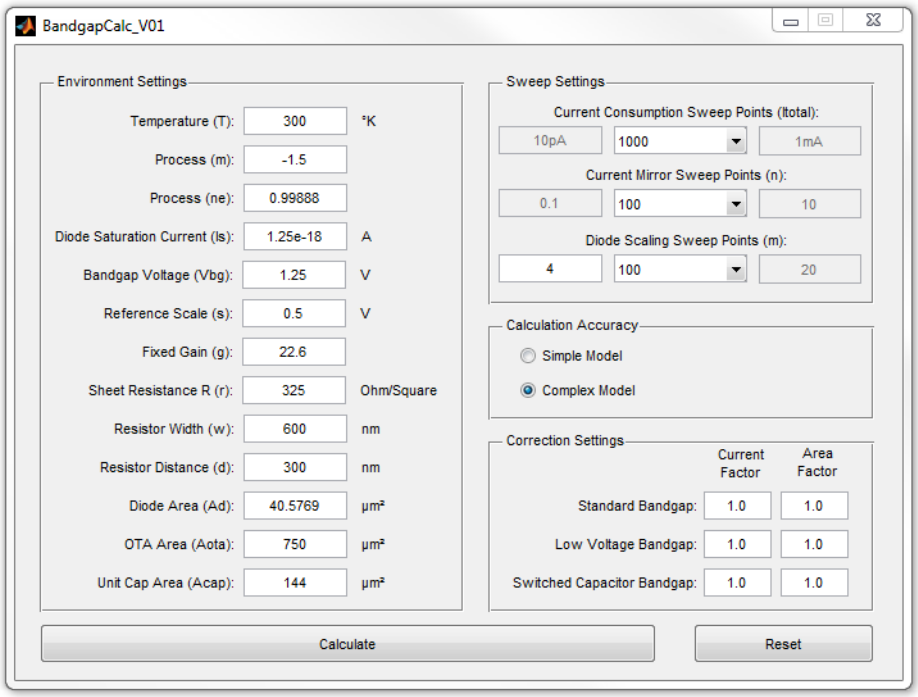


Figure 3.18: MATLAB® program for area estimation

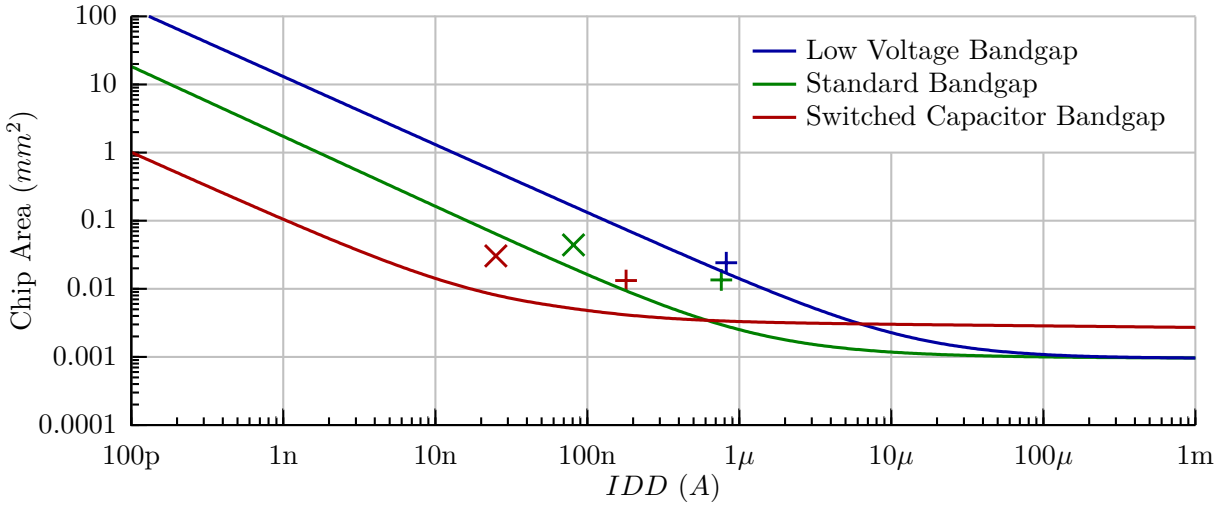
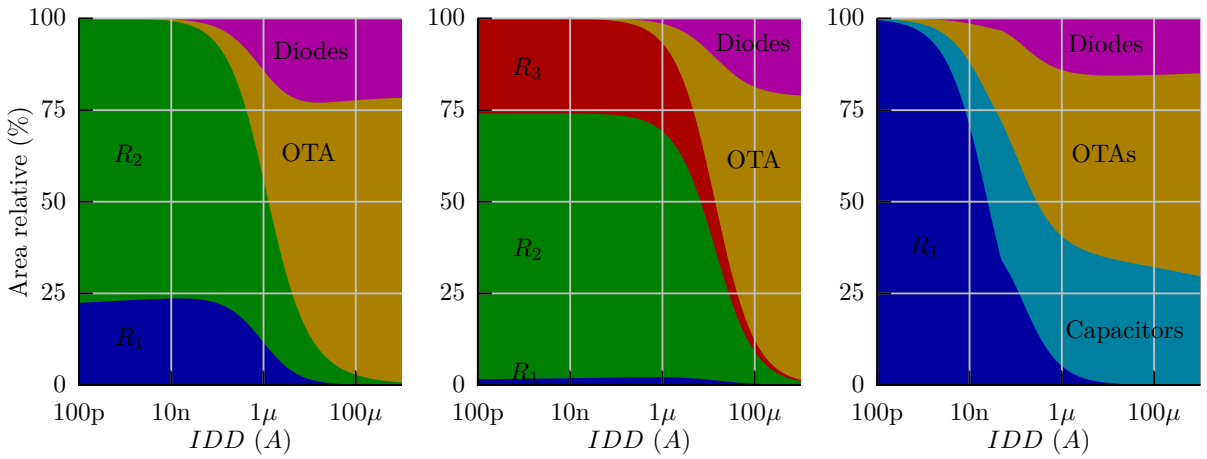


Figure 3.19: Area consumption of three different architectures for various current consumptions



(a) Standard bandgap (b) Low voltage bandgap (c) Switched capacitor bandgap

Figure 3.20: Relative area consumption

It can clearly be seen that for small current consumptions the switched capacitor architecture can achieve a die area at least ten times smaller than the standard bandgap, and compared to the low voltage bandgap even a factor of above 100 is possible. It has to be noted that total current consumptions of below 10 nA are rather unrealistic since most circuits would fail due to leakage. The leakage currents in the transmission gates of the switched capacitor bandgaps especially limit the minimum clock frequency and thus current consumption. Too low clock frequencies allow the voltages stored on the capacitors to change over time, which introduces an error voltage. The minimum clock frequency implies a certain drive current of the steering OTA is needed. Also, every actual implementation has additional area and current overhead for start-up circuitry, reference-ok signal generation, buffer capacitors, wiring and layout design rule reasons. It should also be mentioned that especially the current overhead expected for the switched capacitor bandgap is slightly higher compared to the other topologies.

From the plot as a rule of thumb it can be stated that for current consumptions below 5 μA a switched capacitor bandgap should be considered as long as low voltage operation is necessary. Without the supply limitation the switched capacitor bandgap gets competitive at about 500 nA when compared to the standard bandgap. For low currents an indirect relation between current and area can also be seen. This means for all structures that if the current consumption is cut in half the area increases by a factor of two.

The areas of parts of the circuits can also be investigated when plotted as shares of the total area as depicted in Figure 3.20. For the time continuous circuits at low current consumptions the resistors R_2 consume about 75 % of the total area. The share of resistor R_1 peaks at medium current consumptions and slightly falls for very low consumptions. This is due to the change of the gain that is needed for temperature compensation. As expected the area share of the OTAs diminishes for low current consumptions. In the plot for the switched capacitor circuit a minor non-continuity in the slope of the shares at around 50 nA can be seen. This is due to the limitation of m to values greater than 4 kicking in. In fact the switched capacitor bandgap is the only architecture that benefits from higher values of m than the limit, although only for current consumptions above 50 nA.

For the low voltage bandgap a noteworthy property was found in the simulations. The ideal current mirror scaling factor n is always very close to the square root of the reference voltage scaling factor $Scale$. This behavior should also be derived. The total resistor value of this architecture calculates as follows:

$$R_{\text{total}} = R_1 + 2R_2 + R_3 = \left(1 + \frac{2}{n}\right) \cdot \left[\frac{n \cdot ln(m) \cdot V_{\text{bg}}}{Gain \cdot I_{\text{total}}} + \frac{2n \cdot V_{\text{bg}}}{I_{\text{total}}} + \frac{Scale \cdot V_{\text{bg}}}{I_{\text{total}}}\right] \tag{3.3.29}$$

To get the best n for the smallest total resistor value, Equation 3.3.29 has to be differentiated by n and set to zero. Rearranging for n and applying the square root yields:

$$n = \sqrt{Scale} \cdot \sqrt{\frac{1}{1 + \frac{ln(m)}{2 \cdot Gain}}} \approx \sqrt{Scale} \tag{3.3.30}$$

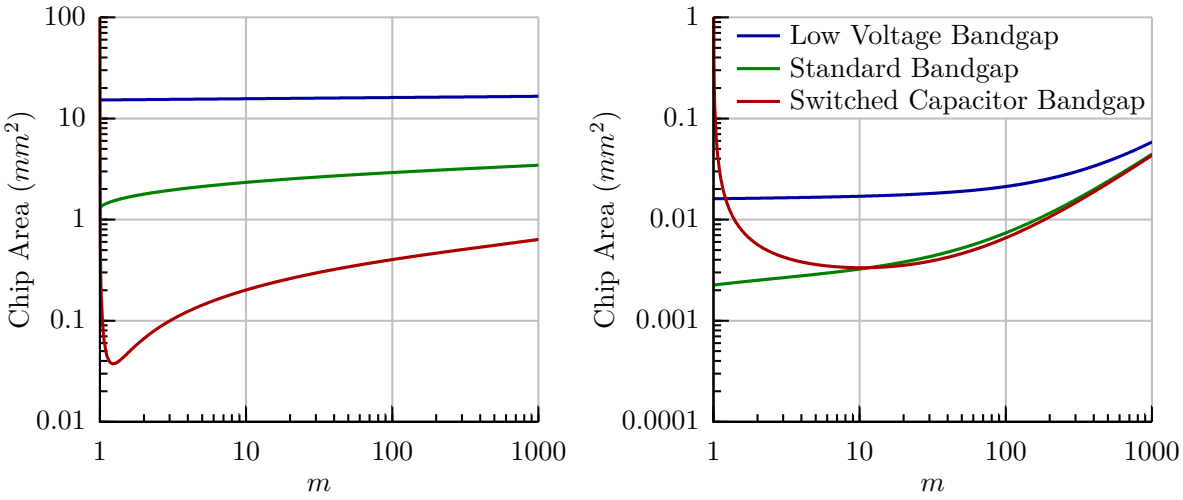
As can be seen in Equation 3.3.30 an ideal n from the area perspective is indeed proportional to the square root of $Scale$ multiplied with a factor. This factor can be approximated to one since $Gain$ is in the range of 20 and $ln(m)$ is significantly smaller than $Gain$, even for high numbers of m.

As stated before, the diode scaling factor m has an influence on chip area but factors approaching one also show inconvenient side effects. Thus the area calculations were repeated for two fixed current consumptions and a sweep over m as depicted in Figure 3.21. For low current consumptions where the resistors are the dominant area consumers the low voltage bandgap shows little to no influence on the factor m. Thus in a design it can be chosen from a wide range due to other constraints. The standard bandgap shows only a weak influence of factor m with the tendency for smaller area at lower factors m. The switched capacitor bandgap benefits most of small factors m, although at extremely low factors the trend reverses as the capacitor array starts to grow, since a very large multiplication factor of the capacitive multiplier is needed. At higher current consumptions the overall area consumptions are lower, thus a large factor m results in a significant increase in area for all three topologies. Again the switched capacitor bandgap shows the biggest variation over m with a minimum in area at a specific value of m.

3.4 Start-Up

Speed usually is not a well-known property for reference circuits. It is possible to interpret the term speed in two ways for a bandgap and they both relate to the output impedance. The first interpretation is how long it takes the circuit to reach its stable output voltage after the supply voltage is switched on. The second is the time the circuit needs to compensate a charge injection at the output like it happens when certain blocks are switched from or to the reference voltage. In this section only the first interpretation, also called start-up time, is investigated.

The start-up time can be an important factor for system performance if a non-continuous operating mode is desired. For example, a system containing a reference circuit combined with an ADC and a sensor should do single measurements. Between the measurements the system is put in a sleep mode to save energy and thus the power supply is switched off. Now for each measurement the bandgap has to be started and the ADC has to wait with conversion until the reference voltage has settled. If this start-up time is long, energy consumption for each measurement will be high since current flows through the circuit and the energy calculates as the product of supply voltage



(a) At a total current consumption of 1 nA

(b) At a total current consumption of 1 μA

Figure 3.21: Sweep over diode scaling factor m

and current integrated over time.

Figure 3.22 shows the start-up behavior of the switched capacitor bandgap presented in Section 3.2 for 100 Monte Carlo simulation runs. It can be seen that it takes quite some time after the supply voltage is activated at 0 μs for the output voltage to rise from the zero level. This is due to the time it takes the bandgap to pass through multiple clock phases. Some of the simulation runs show significant overshoots which disappear at the second cycle round. At around 400 μs all voltages are settled to their final individual voltage level. As Monte Carlo is applied all runs converge to their own specific output voltage level.

So the start-up time is the time it takes the reference to reach a stable output voltage. To be more precise it is postulated that the output voltage must be within a certain band around the average final settled voltage. As there is noise the voltage will actually slightly vary around the average all the time anyhow. One could do a single transient simulation and determine the time the settlement process takes but this is not very meaningful. In reality every chip behaves differently and there is noise. So to get useful information many simulations with Monte Carlo deviations and transient noise have to be done. The deviation of every voltage over the time compared to its final average value has to be determined. To compress this data the average voltage deviation over all runs at each time step has to be calculated which gives a single curve over time. It should be noted that the deviations have to be converted to positive values first as for noise and overshoots the deviations occur in both directions and would otherwise cancel each other out. The peak deviation is not as meaningful, as it is always prone to statistical luck.

Exactly this simulation has been done for the low voltage bandgap and the switched capacitor bandgap presented in Section 3.2 with a few modifications. As the low voltage bandgap has a current consumption of 900 nA some headroom to the switched capacitor topology with a total consumption of 180 nA was present, so that a few improvements are justified.

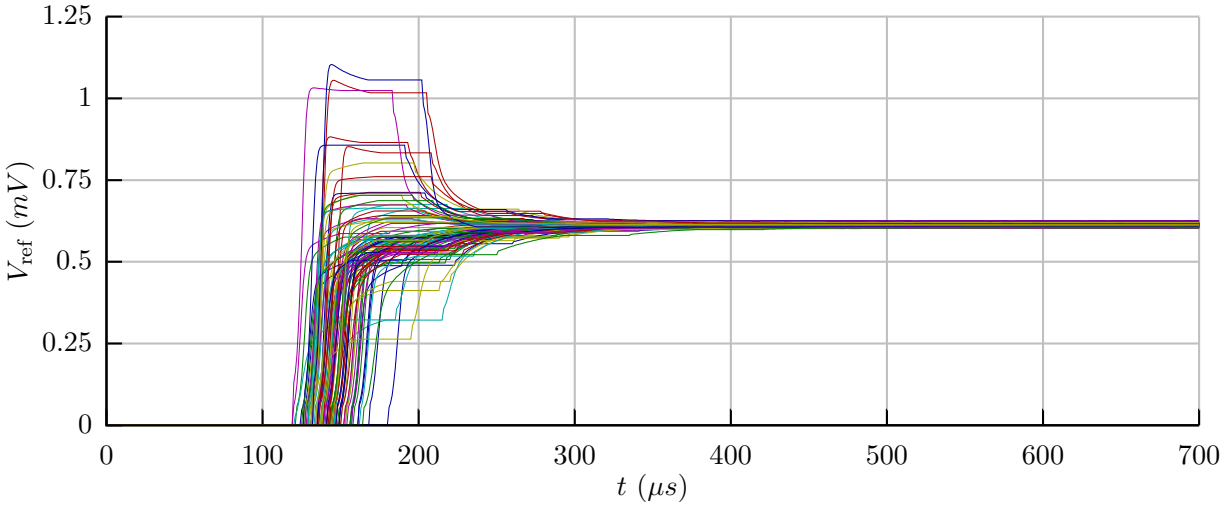


Figure 3.22: Simulation of start-up behavior at 27 °C for 100 Monte Carlo runs.

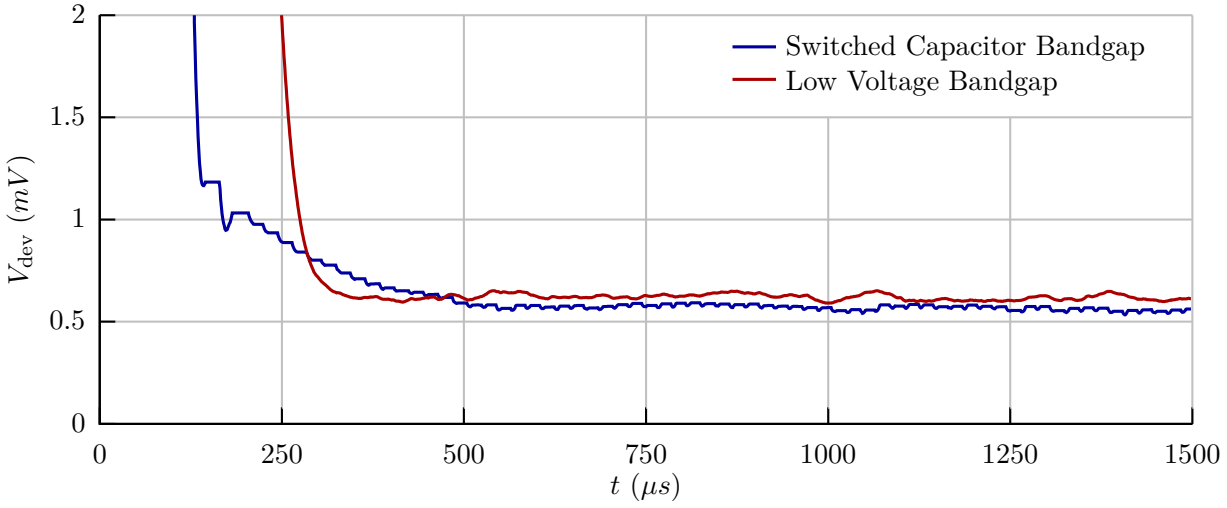


Figure 3.23: Simulation of start-up behavior at 27 °C for 1000 transient noise runs.

To speed up simulation the clock signal was generated by an ideal source and its frequency was increased to 150 kHz. Since a clock is always available for a switched capacitor bandgap some kick-start techniques were also applied. For the first two cycles clock phase $\phi 3$ is extended to three clock cycles and additionally the current in OTA2 is increased to four times its normal value. This helps to charge the capacitor at the output to values close to its final value relatively quickly. Nevertheless the current consumption stays rather low at 560 nA during start-up and 210 nA afterwards (values without oscillator). The decrease of current in OTA2 and shorter $\phi 3$ phases of one clock cycle during normal operation reduce the noise level as the voltage at the output capacitor cannot follow the voltage variations coming from OTA2 fast enough, resulting in a low pass behavior.

To be able to still get a fair comparison the two circuits were enhanced with capacitors at their outputs. The size of the capacitors was set to a value so that the average output deviation due to noise is close to 600 μV. In a system this reference voltage deviation adds or even defines the average measurement error. It has to be noted that this value is an average value and not a root mean square value. The results of 1000 simulation runs for each topology can be seen in Figure 3.23. With the help of the kick-start circuits the switched cap bandgap is able to settle to a deviation level smaller than 1 mV significantly faster than the low voltage bandgap. Unfortunately after kick-start it takes longer to settle to the noise level. An increased kick-start time does not help, as the noise level during this time is above 1 mV. Further improvements can be achieved by implementing a graduated kick-start but were not investigated in more detail.

Combined with the knowledge that was gathered in Section 3.3.4, it is likely that start-up times of the switched cap bandgap will be increasingly better when compared to the low voltage variant for decreasing current consumptions. This is due to the fact that for the low voltage bandgap the resistors R_2 become huge and present a considerably large capacitor for nodes A and B. Thus start-up is delayed, since these distributed capacitors have to be charged during start-up.

3.5 Power Supply Rejection Ratio and Noise

The switched capacitor bandgap shows a significantly different power supply rejection behavior than a time continuous bandgap. Due to the inherent clock frequency of a switched capacitor bandgap, disturbers can cause a beating behavior when the disturber frequency is close to the clock frequency or multiples of it.

To be able to show this behavior in a clear way measurements were conducted as follows. Three circuits were measured, the low voltage bandgap circuit with 4 pF output capacitor, the switched capacitor bandgap as presented in Section 3.2 with 2 pF output capacitor and the modified switched capacitor bandgap with adjustable output capacitor between 0 pF output capacitor and 31 pF output capacitor. All reference voltages are buffered by the same output buffer, which is fed by a separated power supply and has a -3 dB bandwidth of approximately 2 MHz. The supply voltage of the reference circuits is set to 1.2 V DC with a 100 $\mathrm{mV_{peak-peak}}$ AC sine shaped signal added to it. The frequency of the AC signal is swept logarithmically from 10 Hz to 10 MHz in a period of 1 s. The signal at the output buffer is measured by a digital oscilloscope which triggers synchronously to the frequency sweep. The oscilloscope is configured to record the probability of the measured

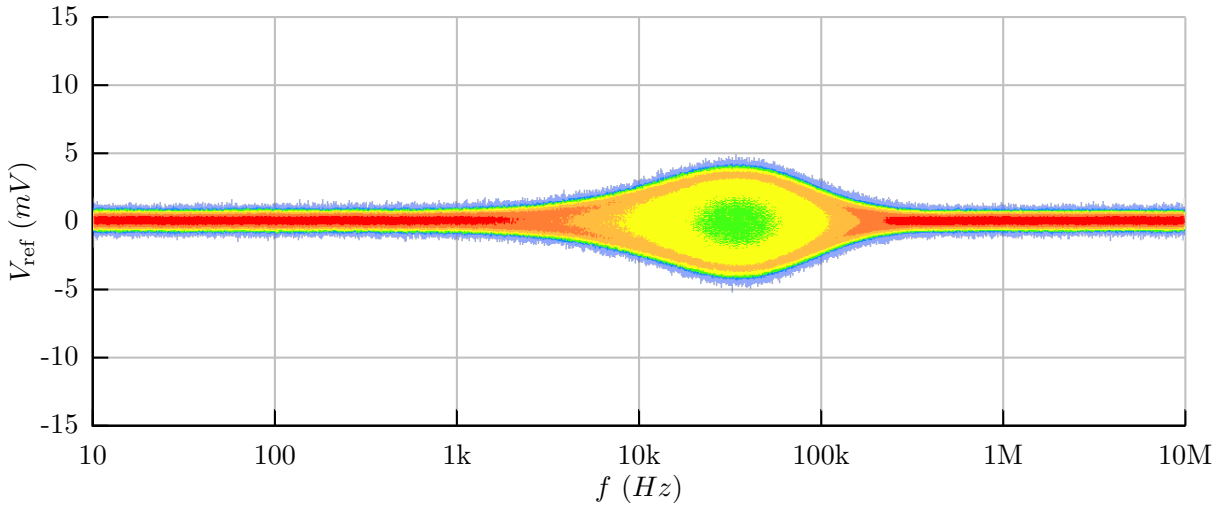


Figure 3.24: Power supply rejection of low voltage bandgap.

signal being at a certain voltage level. The measurement is repeated many times so that a good statistical distribution is present. As the oscilloscope is triggered by the signal generator each point in time can be assigned to a certain excitation frequency.

Figure 3.24 shows the measurement of the low voltage bandgap topology. Due to the measurement procedure the envelope of the density plot represents the peak deviation of the reference voltage. For supply ripple frequencies of up to approximately 2 kHz the output voltage stays within the normal deviation band caused by the limited DC line regulation capability and additional noise. Since the deviations due to noise are higher than from the supply ripple, the ripple at the output from the supply is hidden in this representation. To determine the value at a single frequency as shown in Table 3.4 the measurement principle had to be changed as described later. However for disturber frequencies between 2 kHz and 200 kHz a reduced power supply rejection rate can be observed. Peak voltage deviations of up to ±5 mV are present.

Figure 3.25 represents the same measurement but with the bandgap presented in Section 3.2 with internal oscillator and a small 2 pF output capacitor. This circuit with this configuration has an increased noise level at its output when compared to the low voltage bandgap which makes the line regulation undistinguishable. At a frequency of 55 kHz/4 = 13.75 kHz the first peak deviation of the output voltage can be observed. The internal oscillator frequency of 55 kHz is divided by a factor of four in the timing unit, which represents the slowest clock frequency in the system. Every integer multiple of this frequency another especially sensitive weak point is present. A special case is observed when the disturber frequency is very close to the oscillator frequency as a DC offset voltage of up to 10 mV can be present at the output voltage. In general it can be stated that this circuit in this configuration is much more susceptible to supply ripple as output deviations as high as ±30 mV are present.

The configurable version of the switched capacitor bandgap was also tested with its output capacitor set to the full 31 pF and an external clock source attached. Figure 3.25 shows the significantly better performance when compared to both other circuits. The noise level and line regulation are

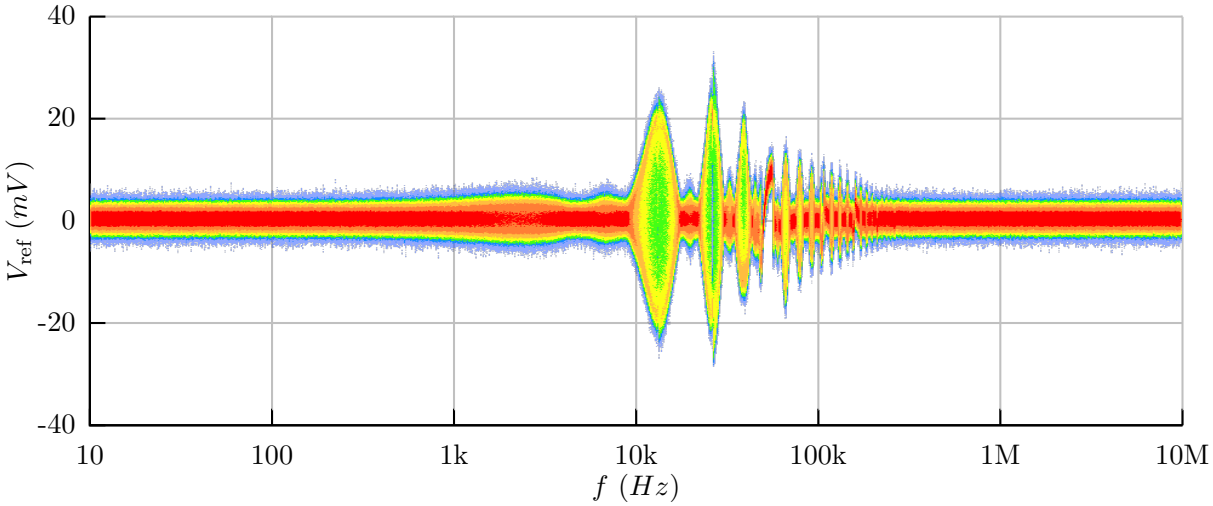


Figure 3.25: Power supply rejection of switched capacitor bandgap.

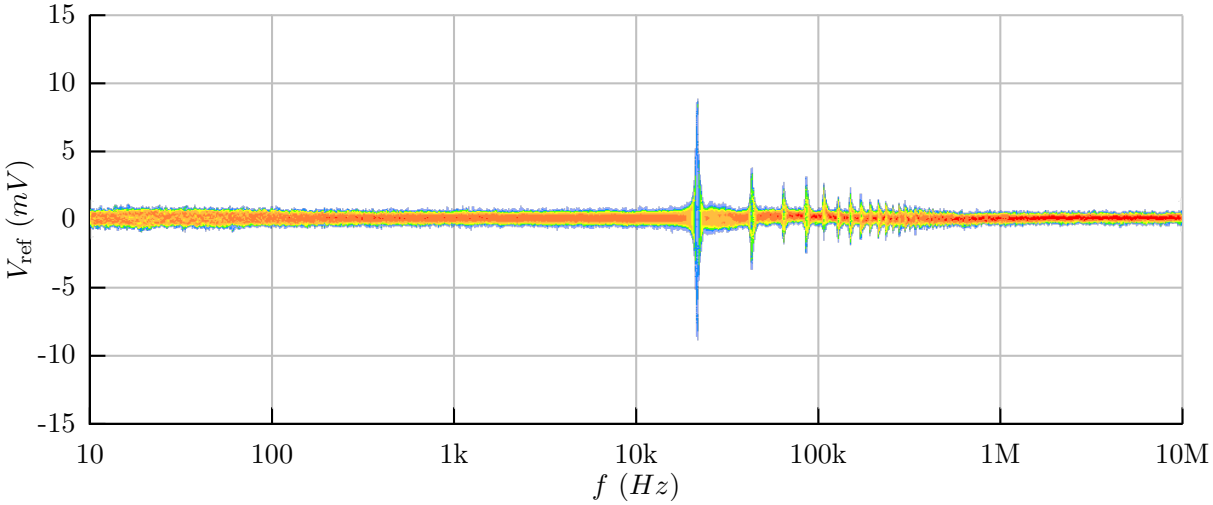
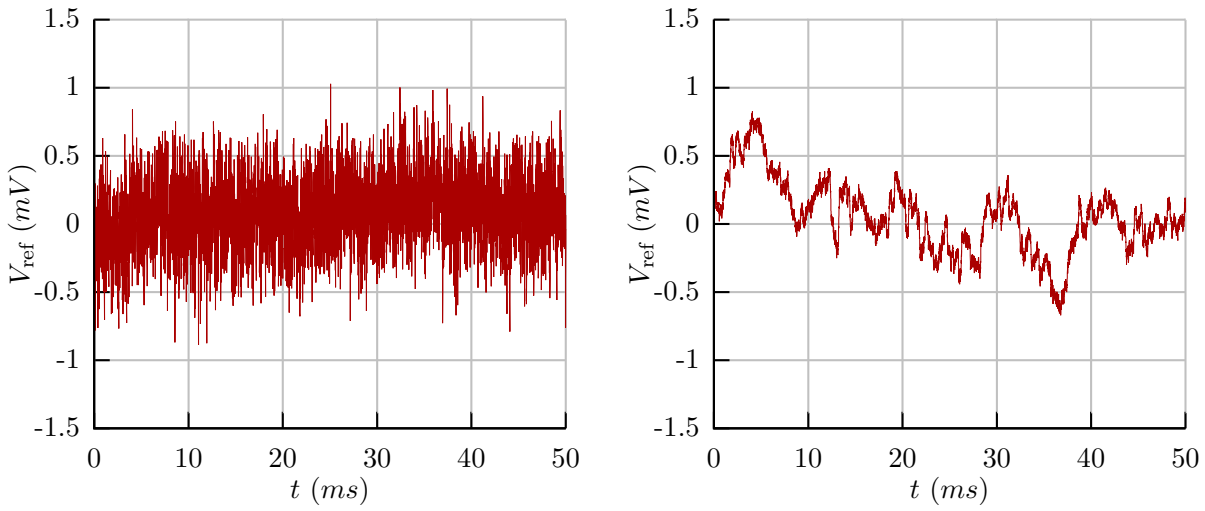


Figure 3.26: Power supply rejection of modified switched capacitor bandgap.



(a) Low voltage bandgap

(b) Switched capacitor bandgap

Figure 3.27: Transient noise measurement at approximately the same total integrated noise levels

considerably better and the regions where the power supply rejection ratio is poor are also much narrower. The weak spots are narrower due to the fact that the clock frequency with the external source is fixed whereas with the internal oscillator the supply disturber also influences the clock frequency.

In conclusion, it can be stated that as far as power supply rejection ratio is concerned the switched capacitor bandgap can definitely compete with the time continuous topologies when this issue is addressed during design phase. Big capacitors at the outputs help significantly but at the cost of increased start-up time. A supply filter with a cut-off frequency far enough from the lowest clock frequency in the system could further improve the power supply rejection ratio. Also, the lowest system frequency can be scaled up very easily at the drawback of increased power consumption.

As already mentioned in Section 3.4, noise is an important property of a reference circuit. Figure 3.27 shows the noise of the low voltage bandgap and the switched capacitor bandgap at approximately the same total noise level of 600 μV_{rms} in the time domain. Many high frequency components can be seen in the signal of the low voltage reference. The switched capacitor's noise is mostly generated by OTA2 and the amplification process of the rather small PTAT voltage with a capacitor network of limited size. For every sample OTA2 tries to recharge the output capacitor to a new voltage during $\phi 3$. The output impedance combined with the storage capacitor form a low-pass filter which is why a bigger capacitor or a reduced bias current reduces the noise.

3.6 25nA Implementation

The switched capacitor bandgap shown in Section 3.2 with a total power consumption of approximately 180 nA was modified in the subsequently shown ways to reach a total current consumption of below 25 nA at room temperature.

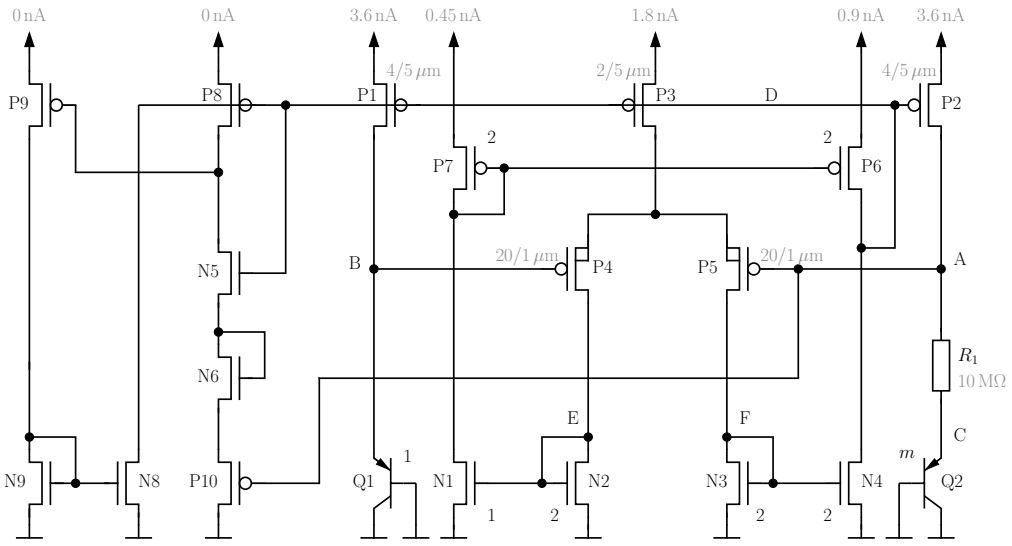


Figure 3.28: Modified PTAT bias cell

The PTAT bias cell was slightly modified, as can be seen in Figure 3.28. The p-channel transistor P10 was placed instead of the n-channel transistor N7. This was done to decrease the current consumption of the start-up circuit during normal operation. When the circuit first gets connected to the supply voltage the node voltages at the nodes A and B can be expected to be close to zero as no current is fed to the bipolar transistors Q1 and Q2 through P1 and P2 and all parasitic capacitors are discharged. This means P10 acts like a diode connected load as N7 would. As a result start-up works just as in the previous case. The source voltage of P10 follows its gate voltage with a threshold voltage in-between. So when the voltage at node A rises as the circuit gets into its normal operating point the source voltage of P10 also rises. Thus less current can flow through the start-up branch during normal operation. The gate of P10 was connected to node A rather than node B because node A is loaded with significantly more capacitive loads, in particular R1. Due to this capacitive load node A stays at low voltage levels for a longer period of time than node B does. Connecting the gate to node B would prematurely end the start-up current injection, thus the start-up process would take significantly longer.

The timing unit, shown in Figure 3.29, despite its minor influence on area and current consumption, was reduced to its bare minimum. Only one flip-flop is sufficient to represent all three clock phases that are needed for operating the circuit. To achieve this, not only the edge of the clock signal is used but also its logical level. When the clock input and the output of FF1 are at the low level NOR1 generates a one at its output which represents $\phi 1$. The inverted signal of $\phi 1$ simply represents $\phi 23$. With the positive edge at the clock signal the output of FF1 changes to high. As both signals are now high EXOR1, which only outputs a high signal when the signals at its input are different from each other, stays at low. This phase represents $\phi 2$ but there is no node in the circuit that represents this phase. With the negative edge at the clock signal $\phi 3$ is initiated which lasts through the next positive edge at the clock input until the second falling edge. This way $\phi 3$ is two times as long as $\phi 1$ or $\phi 2$ which helps to keep output impedance low and to speed up start-up. Compared to the timing unit that uses four flip-flops, this version can introduce some unwanted timing errors and overlaps, but due to the extremely low power and thus slow design

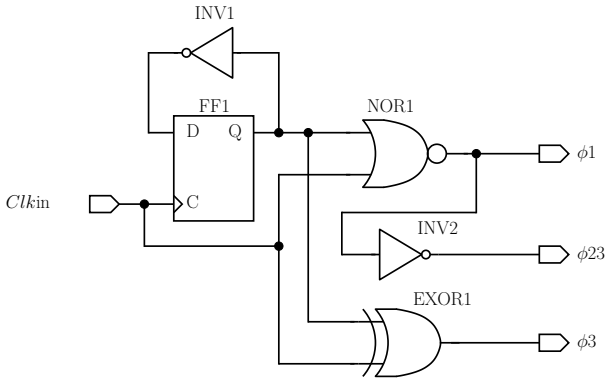
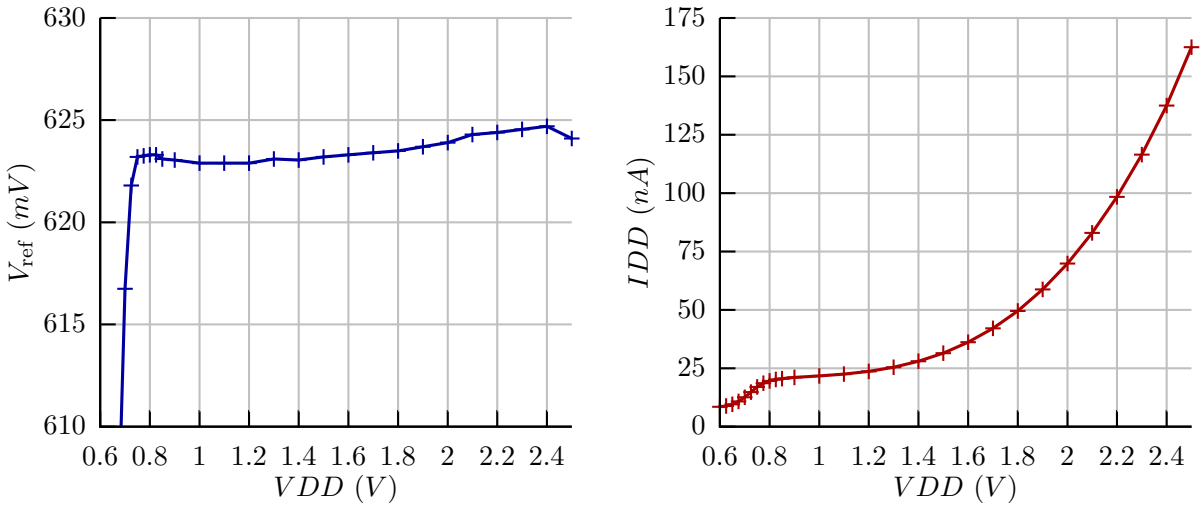


Figure 3.29: Timing unit



(a) Reference voltage

(b) Current consumption

Figure 3.30: Measured characteristics of 25 nA bandgap at room temperature

the effect of these short glitches is negligible. Also with this timing unit the duration of phases $\phi 1$ and $\phi 2$ are dependent on the duty cycle of the clock signal. For that reason it has to be ensured that settling of all nodes is possible during these two phases for the given oscillator. Additionally, as the transmission gates in the overall circuit need inverted as well as non-inverted signals to steer their p- and n-channel MOSFETs, the inverters usually used to do this can be partly left out. This is done by using the inverse behavior of $\phi 1$ and $\phi 23$ for the transmission gates TG1, TG2, TG3, TG4 and TG5, which stay the same as already seen in Figure 3.8. Only TG6 needs an additional inverter to generate the signal $\phi 12$.

The resistor R1 was increased from an original size of 2.6 MΩ for the 180 nA variant to 10 MΩ. This, combined with a reduced diode scaling factor of $m = 4$, results in a decreased current through Q1 and Q2 of 3.6 nA compared to the previous 17.9 nA at room temperature.

Ten test chips were measured at the nominal supply voltage of 1.2 V at room temperature and

Table 3.3: Statistical deviations of switched capacitor bandgap test chips with 25nA current consumption

Test chip	V_{ref} (mV)	f_{clk} (kHz)	$IDD_{\text{bg+osc}}$ (nA)
1	622.9	2.630	23.7
2	633.5	2.796	37.8
3	619.7	2.628	29.9
4	627.7	2.642	30.5
5	630.2	2.356	25.7
6	634.7	2.724	29.4
7	622.7	2.739	26
8	636.6	2.545	25.1
9	624.8	2.725	25.2
10	608.1	2.486	23.6
μ	626.1	2.627	27.7
σ (abs.)	8.48	0.134	4.35
σ (rel.)	1.36%	5.08%	15.7%
μ (simulated)	620.0	3.140	23.0
σ (abs.; simulated)	6.52	0.280	1.80
σ (rel.; simulated)	1.05%	8.86%	7.99%

the results are presented in Table 3.3. Measurements over supply voltage were performed and the results of test chip number 1 are shown in Figure 3.30. It can be seen that the reference voltage reaches its final value at about 750 mV supply voltage and stays within a ± 0.9 mV band up until 2500 mV . Thus the line regulation from 750 to 2500 mV calculates to 0.16 %/V. The current consumption over supply voltage shows a consumption of below 25 nA for voltages below 1.3 V. For higher voltages the current consumption shows a rather large increase. At more than 2.5 V the circuit stops working properly and this region is thus not shown in the plots. Due to the fact that at the time of measurement no temperature forcing device was available, only one test chip was measured over temperature with the help of a cooling spray and heat gun. The cooling spray achieves approximately a temperature of $-50\,^{\circ}$C, whereas the heat gun was set to 80, 100 and 130 °C. Over this temperature range no abnormal behavior could be observed and the reference voltage stayed within a ± 1.0 mV band from its value at room temperature.

3.7 65nm Implementation

The switched capacitor bandgap structure was also implemented in an Infineon C65 process with 65 nm gate length and the capability to build poly-poly capacitors. As the circuit should replace a

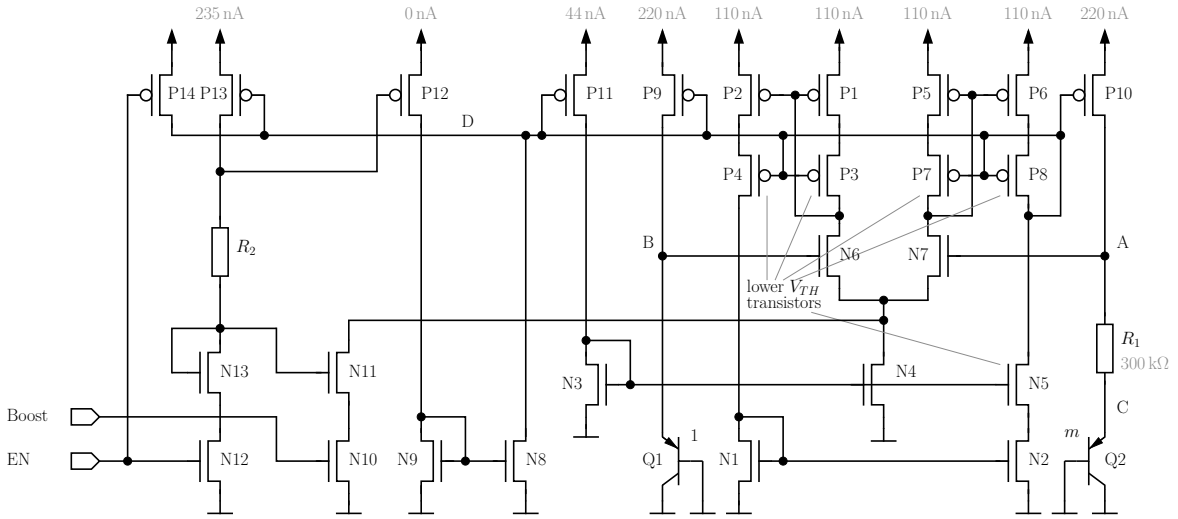


Figure 3.31: Bias cell of 65nm implementation

continuous time low voltage bandgap in an actual product some requirements were given. The output voltage had to be 800 mV with a better than 0.8 % one sigma untrimmed accuracy while operating with supply voltages as low as 1 V. Also the start-up time had to be shorter than 10 μs and area and current consumption reductions compared to the low voltage bandgap were anticipated.

To meet the specifications several changes had to be made to the design shown in Section 3.2. The PTAT bias cell including the start-up circuit is depicted in Figure 3.31. In the given process only thin oxide transistors that are mainly designed for digital circuits are available resulting in a bad analog performance of the transistors. At least the transistors can be built with two different threshold voltages.

Due to the low early voltage of the transistors the gain of the OTA minimizing the voltage difference between nodes A and B was too low. Thus cascodes were added. Since the transistors P3, P4, P7 and P8 are implemented with lower threshold voltages than the other devices, node voltage D presents a good bias voltage for them. The differential pair comprised of the transistors N6 and N7 was implemented with the higher V_{TH} devices to give the cascodes more voltage headroom.

Due to the fact that in this process a high resistive poly is available, the start-up circuit can be realized with R_2 in series with transistor N13 instead of two diode connected transistors. This combination gives a more linear behavior of the current in this path over temperature at increased area consumption. Transistor P13 mirrors the PTAT bias current to the two devices and the resulting gate voltage on P12 decides if a start-up current is needed. To achieve the start-up time requirement a boost signal is supplied by the digital phase generation unit. This signal is used in the bias cell to use N13 and N11 during boosting as an additional current source for the OTA.

The boost signal is also used in the OTA used for the switched capacitor operation to increase the current in the OTA by four times during this period of time. The OTA itself is a class-A amplifier and not class-AB as in the previous implementations, as this adds some additional unwanted

reference voltage inaccuracy. Again, to improve gain, cascodes were added. The switching of the capacitive network and output capacitor to the output of the OTA results in a non-constant capacitive load and subsequently to stability issues. To keep the OTA stable at all times even during start-up an additional load capacitor 700 fF in size had to be added to its output during clock phase 1 ($\phi 1$). As this capacitor as well as the capacitor array for the voltage multiplication was implemented using the high capacitance density poly-poly capacitors, only very minor area consumption was necessary. During start-up a rather high current is driven into the capacitive load of up to 2 pF through the transmission gate at the output. This transmission gate is designed using minimum width transistors to minimize charge injections during switching. This results in a low start-up speed as a large voltage drop occurs on this device. Thus a second wider transmission gate is connected in parallel to the first transmission gate to lower the resistance. This transmission gate is only activated during boosted operation and $\phi 3$ thus minimizing the output ripple during normal operation.

Again the bandgap includes its own relaxation oscillator to steer the switching operation. As the current consumption requirement is more relaxed in this implementation and resistors can be built small due to the high sheet resistance of the poly silicon layer, the threshold voltages for the comparator are generated separately by applying a PTAT current to an additional resistor. The resulting PTAT voltage is compared to the voltage on a capacitor charged and discharged by the same PTAT current. The oscillation frequency was designed to be around 500 kHz. During boosting the clock frequency is directly fed to the clock phase generation unit whereas during normal operation it is divided by two in advance.

The circuit was laid out and simulations performed with the extracted netlist. During start-up a current consumption of 5.4 μA at room temperature was recorded. During normal operation, which is reached after approximately 20 μs after supply voltage is turned on, a current consumption of 3.1 μA is reached. Monte Carlo simulations show that the first full clock phase cycle is completed before the 10 μs mark, resulting in a first good value of the reference voltage at this point in time. The full accuracy, though, is only reached after boosting is complete and the output voltage settled. Then a simulated untrimmed accuracy of 0.586 % for one sigma is reached. The area consumption compared to the existing low voltage bandgap could be decreased by approximately 30 %.

3.8 Comparison to State of the Art

Voltage references are a popular topic for publications, thus there exists a vast amount of them. In Table 3.4 a condensed comparison of the presented bandgap structures to recent and not-so-recent publications is given.

The first line in the first section in the table represents the switched capacitor bandgap presented in Section 3.2, the second line is the reduced power variant shown in Section 3.6. The third line shows the fast start-up variant which is described in Section 3.7. The following three lines represent one low voltage bandgap and two standard bandgaps that were designed in the same process for comparison purposes. Only the low voltage bandgap of these three was included on a test-chip, thus measurement results are only available for this architecture whereas the other two where only simulated with an extracted netlist.

Section two in the table shows seven other publications of switched capacitor bandgap references, of which one is not based on bipolar transistors but MOSFETs. The third section shows seven bandgap structures that operate by adding two voltages at the output, whereas in the fourth section eleven circuits are shown that rely on adding currents. In the sixth section eleven additional publications are listed that cannot be assigned to the aforementioned working principles.

From the values in the table it can be seen that the presented switched capacitor bandgaps can combine low voltage operation with ultra-low power at small die area and good untrimmed accuracy optimally. There are publications that can rival the presented designs in every single parameter, but the combination of multiple parameters is the most important part. Subsequently a few of the competitors in the list will be discussed, commented upon and compared to the switched capacitor circuits presented in this work.

Of the other switched capacitor references the circuit presented by [19, 20] combines ultra-low power (250 nA) with medium low voltage operation (1.00 V to 4.00 V) but the die area (0.049 mm^2) is significantly bigger than the presented solution. Also, as the threshold voltages of MOSFETs are used rather than bipolar transistors, the untrimmed accuracy is worse, which is why trimming is necessary. Additionally the temperature range is limited and the output voltage is not flexible and fixed to an uncomfortably low value of 190 mV. The circuit in [30] can additionally achieve low die area (0.0055 mm^2) but due to a passive switching principle that employs stacking of capacitors to realize a gain unavoidable parasitic capacitors deteriorate the untrimmed accuracy (2.2 %). Also, the circuit is sensitive to leakage resulting in a rather limited useable temperature range (−35 °C to 80 °C) and a bad temperature coefficient (160 ppm/°C). The other four switched capacitor-based solutions with published current consumptions consume substantially more current in excess of 1 μA. Of those four only [31] achieves a very small die area (0.0025 mm^2), but true low voltage operation (>1.10 V) is not given anymore.

Of the seven circuits that employ voltage adding at their output, all but two are not low voltage compatible. These two [32] and [33, 34], however, have current consumptions of 1 μA and 18 μA respectively. Also, the circuit presented in [32, 35] uses Double-Diffused MOSFETs (DMOSs) rather than bipolar transistors, which is why trimming is again needed.

The eleven current adding circuits are more suited to low voltage operation with none of them requiring more than 1.1 V supply voltage to operate. Again only two of those have current consumptions below 1 μA and neither is based on bipolar transistors. [36] can achieve a very low 20 nA operation at reasonable die area (0.0189 mm^2), but the necessary minimum supply voltage of 1.1 V and the extremely low reference voltage of 96.6 mV can represent a big drawback. The circuit presented in [37, 38] has a lot of positive features but temperature range is limited (0 °C to 80 °C) and the untrimmed accuracy (3.1 % 1σ) is bad.

From the eleven references using other working principles, five have current consumptions below 1 μA and seven of them work below or at 1.00 V supply voltage. [39] achieves good values at most specifications but has a very unstable current consumption over the full operating range.

To be able to better compare the reference circuits to each other a new Figure of Merit (FOM) is proposed in Equation 3.8.1.

Table 3.4: Bandgap performance comparison

Reference	Year and place of first publication	Technology	Principle	Circuit elements	Temperature range ($^\circ C$)	Temperature coefficient ($ppm/^\circ C$)	Supply voltage range (V)	Power supply rejection ratio (dB)	Line regulation (%/V)	Reference voltage (mV)	Untrimmed accuracy (1σ) (%)	Current consumption (nA)	Active Area (mm^2)	FOM $\left(\frac{pWm^2}{K^2}\right)$
This work [25] 180nA	2012 ISCAS	0.13 μm CMOS 1p6m	switched cap	MOSFET, BJT, R, C	-50 to 150^M	41^M	0.85 to 1.50^{MR}	50^{MA} 47^{MC}	0.33^{MR}	615	0.88^M	183^{MR}	0.0132	2.105
This work 25nA		0.13 μm CMOS 1p6m	switched cap	MOSFET, BJT, R, C	-50 to 130^M	18^M	0.75 to 2.50^MR		0.16^{MR}	626	1.36^M	27.7^{MR}	0.0336	0.388
This work 65nm		0.065 μm CMOS 2p4m	switched cap	MOSFET, BJT, R, C	-40 to 130^S		0.90 to 1.30^S			800	0.59^S	3100^{SR}	0.0063	
This work LVBG		0.13 μm CMOS 1p6m	current adding	MOSFET, BJT, R	-40 to 130^S	7.1^S	0.80 to 1.50^{MR}	62^{MA} 23^{MC}	0.83^{MR}	505	2.27^M	821^{MR}	0.0241	3.889
This work STBG		0.13 μm CMOS 1p6m	voltage adding	MOSFET, BJT, R	-40 to 130^S	9.7^S	1.30 to 3.30^S	49^{SA} 36^{SC}	0.14^{SR}	1212	1.55^S	760^{SR}	0.0132	4.344
This work STBG		0.13 μm CMOS 1p6m	voltage adding	MOSFET, BJT, R	-40 to 130^S	16.1^S	1.45 to 3.30^S	37^{SA} 65^{SC}	0.99^{SR}	1265	2.02^S	81^{SR}	0.0440	2.879
[16] S.Chen et al.	2006 IEICE	0.13 μm CMOS	switched cap	MOSFET , BJT, C	-55 to 125^S	2^S	1.20^S			552	1.97^S			
[30] W.Biederman et al.	2012 CICC	0.065 μm CMOS	switched cap	MOSFET, BJT, C	-35 to 80^M	160^M	$>0.75^M$			423	2.20^M	138^M	0.0055	6.887
[24] H.Chun et al.	2012 MWSCAS	0.065 μm CMOS	switched cap	MOSFET, BJT, R, C	-40 to 100^S	$28-43^S$	0.85 to 1.50^S	45^{SA}	2.92^S	multiple		$>40000^S$	0.0380	2834
[19, 22] H.Huang et al.	2008 ISSCC	0.35 μm CMOS 2p4m	switched cap	MOSFET, C	-40 to 80^M	16.9^M	1.00 to 4.00^M	41^{MA} 17^{ME}	0.76^M	190	trimmed	250^{MR}	0.0490	14.38
[21] Z.Peng et al.	2009 JoS	0.35 μm CMOS 1p4m	switched cap	MOSFET BJT, R, C	20 to 100^M	112^M	3.00 to 5.00^M	40^{MA} 33^{ME}	0.98^M	1260		34000^M	0.0480	85680
[40, 41] P.Chen	2012 VLSI-DAT	0.18 μm CMOS, discrete	switched cap	MOSFET, BJT, R, C	-40 to 100^M	44.6^M	$>0.90^M$		0.35^M	425		48100^M	0.0650	6403
[31] A.Annema	2012 ISSCC	0.16 μm CMOS	switched cap	MOSFET, BJT, R, C	-45 to 135^M	30.0^M	$>1.10^M$			944	0.76^M	1400^M	0.0025	3.565
[32, 35] A.Annema	1998 ESSCIRC	0.35 μm CMOS	voltage adding	MOSFET, DMOST, R	-20 to 100^M	58^M	$>0.85^M$			650	trimmed	1000^M	0.0630	215.7
[34] K.Leung	2002 JSCC	0.60 μm CMOS	voltage adding	MOSFET, BJT, R	0 to 100^M	15^M	$>0.98^S$	44^{MB} 17^{ME}	1.40^M	603	2.00^M	18000^M	0.2400	6350
[33, 42] K.Leung	2001 ESSCIRC	0.60 μm CMOS	voltage adding	MOSFET, R	0 to 100^M	36.9^M	1.40 to 3.00^M	47^{MA} 20^{ME}	0.083^M	309		9700^{MF}	0.0550	2756
[43] M.Miguez	2012 ESSCIRC	0.60 μm CMOS	voltage adding	MOSFET, BJT, R, C	20 to 50^M	647^M	1.70 to 5.50^M		0.09^M	1030	1.26^M	$<200^M$	0.1100	26886
[44] Y.Chen	2012 VLSIC	0.18 μm CMOS	voltage adding	MOSFET, BJT, R, C	-20 to 100^M	24.7^M	$>1.30^S$	67^{MA} 45^{MD}	0.06^M	1198	trimmed	2.98^{MX}	0.0980	0.651
[6] K.Kuijk	1973 JSSC	discrete	voltage adding	BJT, R	0 to 65^M	3.1^M	13 to 30^M		0^S	9880		2300000		
[45, 46] G.Ge	2010 ISSCC	0.16 μm CMOS 1p5m	voltage adding	MOSFET BJT, R, C	-40 to 125^M	12^M	1.80^M	70^M		1088	0.25^M	5500^M	0.1200	5236
[9, 10] H.Banba et al.	1998 VLSIC	0.40 μm CMOS 1p1s2m	current adding	MOSFET BJT, R	27 to 125^M		0.84 to 4.00^M		0.22^R 0.65^F	515	0.97^M	2200	0.1000	
[47] S.Wadhwa	2008 ISCAS	0.09 μm CMOS	current adding	MOSFET, BJT, R, C	-40 to 125^S	14.8^S	1.10 to 1.30^S	45^{MA} 12^{MD}		611		68000		
[48] X.Xing	2007 Norchip	0.18 μm CMOS	current adding	MOSFET, BJT, R, C	0 to 150^M	$10-40^M$	1.00 to 2.60^M		0.8^M	657		43000	0.1860	14219
[49] A.Aldokhaiel	2004 NEWCAS	0.60 μm CMOS	current adding	MOSFET, BJT, R, C	0 to 100^S	33^S	0.80 to 1.60^S	$>50^{SA}$	0.84^S	592		<1100	0.0510	148.1
[50, 51] P.Malcovati	2001 ESSCIRC	0.80 μm BiCMOS	current adding	MOSFET, BJT, R	0 to 85^M	7.5^M	$>0.85^{MR}$		0.021^M	536		92000	0.2500	20294
[52] J.Navarro	2011 ISCAS	0.35 μm CMOS	current adding	MOSFET, BJT, R	-10 to 90^S	21^S	$>1.00^S$		0.33^S	510		6170^{SR}	0.0420	544.2
[36] W.Yan	2009 EL	0.35 μm CMOS	current adding	MOSFET, R, C	-20 to 80^M	11.4^M	1.10 to 4.00^M	60^{MA} 40^{ME}	0.09^M	96.6		20^M	0.0189	0.474
[53] A.Annema	2009 ISSCC	0.032 μm CMOS	current adding	FinFET, BJT, R	0 to 125^M	1018^M	0.80 to 1.50^M			550		14000^{MR}	0.0160	11675
[37, 38] G.De Vita	2006 ESSCIRC	0.35 μm CMOS	current adding	MOSFET, R	0 to 80^M	10^M	0.90 to 4.00^M	47^{MA} 40^{ME}	0.27^M	670	3.10^M	40^{MR} 70^{MF}	0.0450	2.531
[12] A.Boni	2002 JSSC	0.35/0.18 μm CMOS	current adding	MOSFET BJT, R	-40 to 140^M	28^M	0.90 to 3.30^M			492	< 1	40000^R		
[54] A.Cabrini	2005 ESSCIRC	0.13 μm CMOS	current adding	MOSFET BJT, R, C	-50 to 160^M	6.64^M	1.00 to 2.00^M	58^M	0.031^M	798	1.63^M	26000^{MR}	0.0200	78.30
[11] H. Neuteboom	1997 JSSC	0.80 μm CMOS low V_{TH}	other	MOSFET, BJT, R			$>0.90^M$			670				
[13] J. Nebhen	2012 NEWCAS	0.35 μm CMOS	other	MOSFET, BJT, R, C	-25 to 80^M	305^M	$>1.25^M$			1021				
[55, 56] G.De Vita	2005 ISSCC	1.50 μm CMOS 2p2m	other	MOSFET, FGT, R, C	-40 to 85^M	$<1^M$	$>5.00^M$	30^{MA} 10^{MD}	0.002^M	multiple	trimmed	$<500^M$	1.6000	256.0
[57, 58] V.Ivanov	2011 ESSCIRC	0.13 μm CMOS	other	MOSFET, BJT, R, C	-20 to 85^M	40^M	0.75 to 1.50^M	86		256	0.50^M	200^M	0.0550	29.93
[39] P.Yuan	2011 ISCAS	0.18 μm CMOS	other	MOSFET	-30 to 150^M	30^M	1.00 to 2.50^M	54^{MA} 27^{MB}	0.122^M	548		46^{MR} $>1000^{MF}$	0.0036	0.153
[59, 60] K.Sanborn	2006 CICC	0.50 μm BiCMOS	other	MOSFET, BJT, R, C	-40 to 125^M	11^M	1.00 to 2.00^M		0.0063^M	190.9	0.19	20000	0.4000	3232
[61] K.Ueno	2009 ASP-DAC	0.35 μm CMOS 2p4m	other	MOSFET C	-20 to 80^M	7^M	1.40 to 3.00^M	$45^M A$	0.0027^M	745	0.87^M	195^{MR}	0.0520	9.937
[62] T.Hirose	2010 A-SSCC	0.35 μm CMOS	other	MOSFET BJT	-20 to 80^M	394^M	1.10 to 3.30^M		0.11^M	553	1.63^M	100^M	0.2200	953.5
[15] J.Doyle	2004 JSSC	0.50 μm CMOS	other	MOSFET BJT, R, C	-40 to 125^M	17^M	0.95 to 6.00^M			627	trimmed	$<10000^{MF}$	1.0904	6468
[14] A.Mitra	2007 ISIC	0.18 μm CMOS	other	MOSFET BJT, R	0 to 150^S	7.91^S	0.95 to 1.80^S		0.0045^S	620		60000^{SR}		
[63] I.Akita	2009 JSSC	0.18 μm CMOS	other	MOSFET R	-40 to 80^M	25.5^S	0.60 to 1.00^S			400		15000^S	0.1680	2678

^{S} simulated
^{M} measured
^{R} at room temperature
^{F} over full temperature range
^{X} time multiplexed operation, oscillator not included

^{A} at 100 Hz
^{B} at 10 kHz
^{C} at 100 kHz
^{D} at 1 MHz
^{E} at 10 MHz

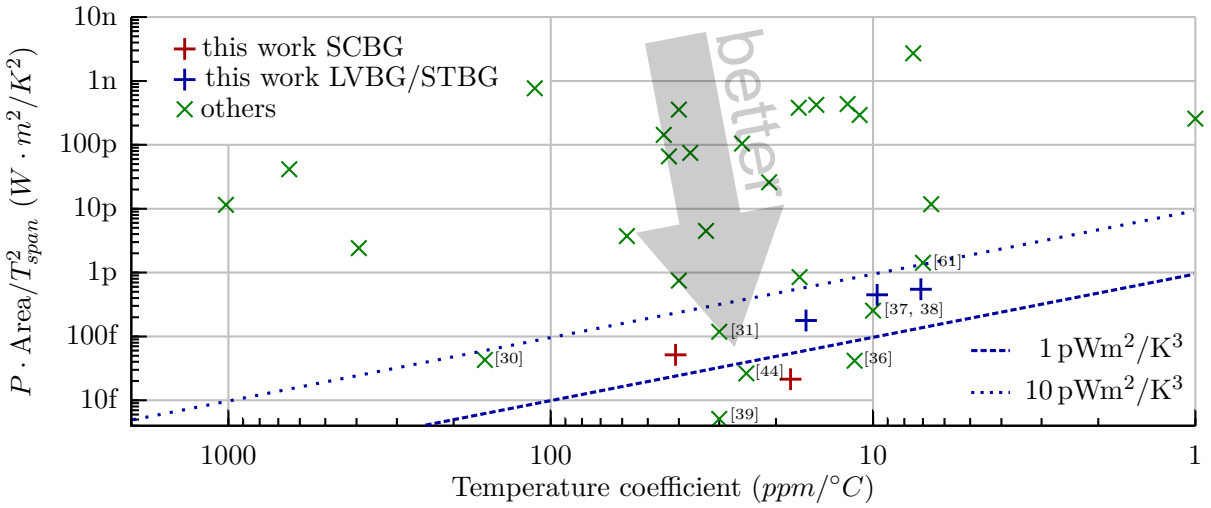


Figure 3.32: Proposed figure of merit with outsourced temperature coefficient

$$FOM = \frac{P \cdot Area \cdot TC}{T^2_{range}} \tag{3.8.1}$$

The current consumption is multiplied with the lowest possible operating voltage to get the power consumption of the circuit. It is multiplied with the area of the circuit. This is done to account for the relation between needed area and current consumption as shown in Section 3.3. Most of the time when the current consumption should be halved a doubling of the resistor size is needed, which doubles the area in a resistor dominant design. The value of the figure of merit so far can indicate how well these major limitations can be handled by the architecture. To further increase the information content, the temperature behavior, as one of the most significant features of a reference, is included. This is done by multiplication with the temperature coefficient and division by the measured temperature range squared.

When the residing voltage deviation over temperature is linear to temperature the range would not necessarily have to be included as the temperature coefficient in this case is constant everywhere along the voltage over temperature line. For first order compensated references a second order shaped residing voltage deviation is to be expected which has a single point with temperature coefficient zero. One could use this to specify a very limited temperature range but an excellent temperature coefficient, which would yield an unfairly good figure of merit. The square of the range is needed since for a second order shape of the voltage over temperature a doubling of the range would yield a temperature coefficient four times bigger.

The calculated values of the FOM are included in Table 3.4 for all references that supply all the necessary values. Smaller values of the FOM indicate a better performance. A plot of the FOM is shown in Figure 3.32. The y-axis is not directly the FOM but the FOM without the temperature component which is plotted on the x-axis. This means that a low area consumption and low power reference is at the lower part of the chart and the ones with a good temperature coefficient are at the right. An ideal reference circuit is supposed to be as far down and right as possible.

In the chart the bandgaps designed in this work are marked in red and blue. The red crosses represent the switched capacitor implementations, and it can be seen they are very competitive when compared to the other solutions. A few other very competitive references are also cited directly within the plot. Additionally it should be noted that not all references in this plot are low voltage compatible which might be an important criterion for selecting the ideal architecture for an application. Also not all values that were used are measured values which could lead to unpleasant surprises during verification.

3.9 Conclusion

A new highly integrated bandgap circuit topology was shown in this chapter. The use of the switched capacitor technique allows a reduction in resistor and thus overall die size while keeping a low voltage operation possible. A mathematical model for each of the three discussed bandgap reference architectures was developed and analyzed in detail. For convenience a small program was implemented that can calculate estimated area consumptions on die of these structures. The switched capacitor bandgap when compared to state-of-the-art designs offers a significant advantage in terms of current consumption and active area while maintaining a good untrimmed accuracy as shown in table 3.4.

The proposed architecture was implemented in three different ways, which of two were measured and the results presented. The base circuit shows a good untrimmed accuracy of 0.79 % in simulation and 0.88 % in measurements for one sigma, works down to 850 mV supply voltage at room temperature, consumes just 183 nA with the oscillator combined and supplies an additional clock signal which can be used for other purposes in a system like determining a polling time. The output reference voltage can be adjusted by a ratio of capacitors thus can be easily fit for many applications. In combination with an ADC temperature measurements are also possible, as a temperature stable and a temperature proportional voltage are available. Even lower supply voltages are possible with this topology when MOS transistors in diode configuration would be placed instead of the pnp-diodes Q1 and Q2 although this would severely worsen the untrimmed accuracy.

Also, an extreme implementation shown in Section 3.6 proves the robustness of the proposed architecture as the total current consumption of this implementation is measured at approximately just 25 nA. Due to the advantages of the proposed topology it was already picked up by multiple other departments within Infineon and will be deployed in multiple low power applications in the near future.

Chapter 4

Successive Approximation Analog to Digital Converter

4.1 Introduction

For the sensor interface to be able to deliver digital values of sensor measurements, temperature readings and on-chip monitoring tasks, an ADC is indispensable. As to be expected for a highly integrated system quite a few prerequisites arise for the circuit. For one thing the ADC should be able to work with the system voltage of 1.2 V. To avoid supply ripple injection a separate supply voltage free of ripple can be provided, however. As with all circuits in the system power consumption is of a major concern. For general purpose use sample rates from extremely low up to moderately high frequencies should be possible. This means that the power consumption should be able to scale in a linear way over the conversion rate range. Also, the resolution requirements can be defined as medium high.

For the given use case and performance requirements the well-known Successive Approximation Register (SAR) principle is best suited as it can achieve high efficiency at medium resolutions. This statement is backed by many publications [64]. A comparison of the efficiencies possible with different state of the art working principles and the proposed architecture is given in Section 4.2.8.

This chapter presents a SAR ADC architecture which evolved over three generations of design steps with all three designs manufactured and measured. The evolution process and the improvements achieved will also be discussed.

The implemented converters have a configurable resolution of 8 or 11 bit. The resolutions are achieved by combining an 8 bit split-capacitor array with a 3 bit resistive ladder allowing for a simpler layout and good power efficiency. Configurable buffers are included and enable a wide range of operation frequencies. Sample rates between 300 S/s and 80 kS/s were tested where at the lower frequency a total current consumption of just 8.4 nA was measured. A configurable time domain comparator is employed to adapt the noise requirement to the desired resolution. The circuit is developed in a 130 nm CMOS technology and occupies an active area of 0.0726 mm^2. Due to the general purpose character and flexibility the ADC was not just integrated into the sensor interface presented in Section 2 but also in a range of other ASICs which partly have been published (see own publications). As a result of all the features an excellent conversion efficiency of down to 24 fJ/CS is achieved which is shown in detail in the measurements.

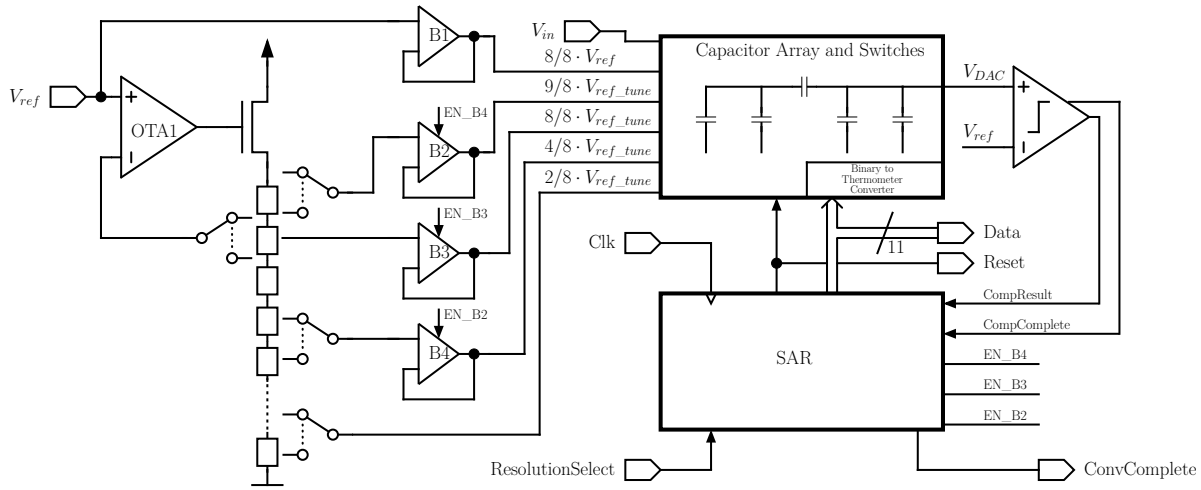


Figure 4.1: ADC system overview

4.2 11bit SAR ADC

A typical SAR ADC consists of a DAC, a comparator and a logic block. The DAC generates voltage levels according to a reference voltage input and the digital signal it receives from the logic block which performs the successive approximation operation. The comparator is used to compare the DAC output to the input voltage which should be discretized. This implies that the input voltage should not change during the conversion. As this would only be possible with a dedicated sample and hold circuit, which would consume additional power, another concept can be applied. An array of capacitors is formed which combines the DAC operation with the sample and hold function.

4.2.1 System

The topology of the proposed ADC is shown in Figure 4.1. The circuit consists of a heavily modified split-capacitor array described in Section 4.2.2, a comparator shown in Section 4.2.4, a logic block discussed in Section 4.2.5 and additional reference scaling circuitry OTA1, four buffers and a tunable resistive ladder described in Section 4.2.3.

4.2.2 Capacitor Array

Figure 4.2 shows the simplest implementation of a capacitive DAC with a resolution of 8 bit during the reset or sample phase as first proposed by [65]. The capacitors are grouped in numbers that double for every additional bit of resolution. One extra capacitor drawn in gray is present in the circuit which can be left out optionally. Its sole influence in this architecture is a slight change in the gain of the converter. The total number of unit elements in this circuit calculates to 2^n or $2^n - 1$, where n denotes the resolution or number of bits. During the sample phase a TG connects the top plates of all capacitors in the array to the reference voltage input. At the same time the bottom plates of the capacitor groups are connected to the input voltage. This way the difference between the reference and the input voltage is stored on all capacitors. The successive approximation operation starts by disconnecting the reference voltage from the top plates and connecting all but one capacitor group bottom plate to ground. This one group has to be the most

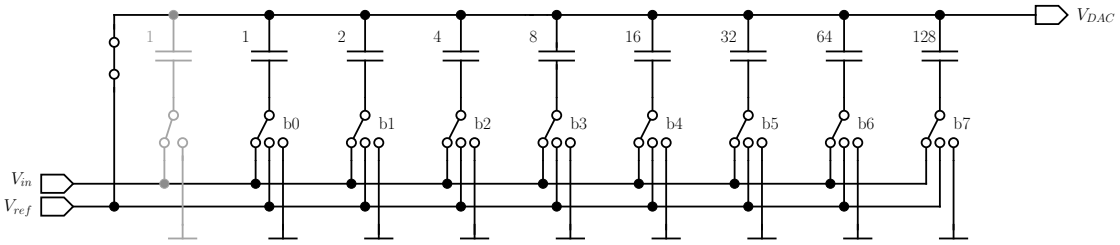


Figure 4.2: Binary scaled capacitor array DAC

significant capacitor group and is represented as a digital value in the logic block as the Most Significant Bit (MSB). Its bottom plate gets connected to the reference voltage instead of ground. When the voltages are settled the comparator can make a comparison between the voltage V_{DAC} and the reference voltage V_{ref}. If the result of this comparison is that V_{DAC} is larger than V_{ref} the MSB is set to zero. Independent of the result the next bit towards the Least Significant Bit (LSB) is set as a next step. This process is repeated until the LSB itself is reached. When the process is finished the binary value stored in the logic block represents the discretized value of the input voltage.

The problem with this simple structure is that the amount of unit capacitors grows exponentially with the resolution. Also, matching between the capacitors becomes an issue for high resolutions, especially for the more significant bits. One good thing is that parasitic capacitances on the node V_{DAC} have hardly any influence on the conversion result. As the voltage on V_{DAC} during the reset phase is set to V_{ref} and during the conversion the voltage, due to the successive approximation process, also converges towards V_{ref}, there is no influence on the absolute conversion result. The only influence that can be seen is a reduced amplitude of V_{DAC} around V_{ref} which due to noise requires a better comparator. In order to not deteriorate the dynamic performance of the converter this capacitance should be kept small when possible.

To overcome the increasing number of unit elements a so called split-capacitor array is introduced as in [66] and depicted in Figure 4.3. The array is now composed of two smaller sub-arrays which are connected via a coupling capacitor C_c. It would be even better if not a single split but multiple splits could be introduced, resulting in a C-2C design, though the problem is that parasitic capacitances at the nodes of the DAC degenerate the linearity. [67, 68] Circuits that try to compensate for these parasitic capacitances exist but cannot yet achieve excellent power efficiency and are limited in resolution. [69, 70, 71] For this design a single split architecture with a non-symmetrical distribution of the capacitors was chosen, as will be explained later on.

The sub-array with the node V_{DAC} is directly connected to the comparator and thus has a strong influence on the comparison result and represents the more significant bits of the result. It can be called the major array. Connected via the coupling capacitor C_c to the major array is the so called minor array which represents the low significance bits. The number of binary scaled capacitors in each of the two sub-arrays can be varied but the total number of the steps still determines the achievable resolution. The total number of unit elements calculates to $2^m + 2^n - 1$ or $2^m + 2^n - 2$ where m denotes the number of bits in the minor array and n the number of bits in the major array. C_c can only be sized the same as a unit element if the optional capacitor at the end of the minor array is not present and the number of bits in both arrays are the same. Also the

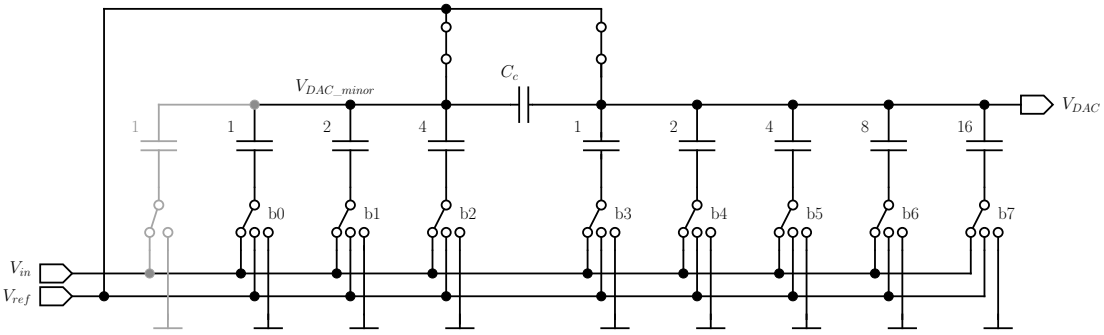


Figure 4.3: Basic split-capacitor array DAC

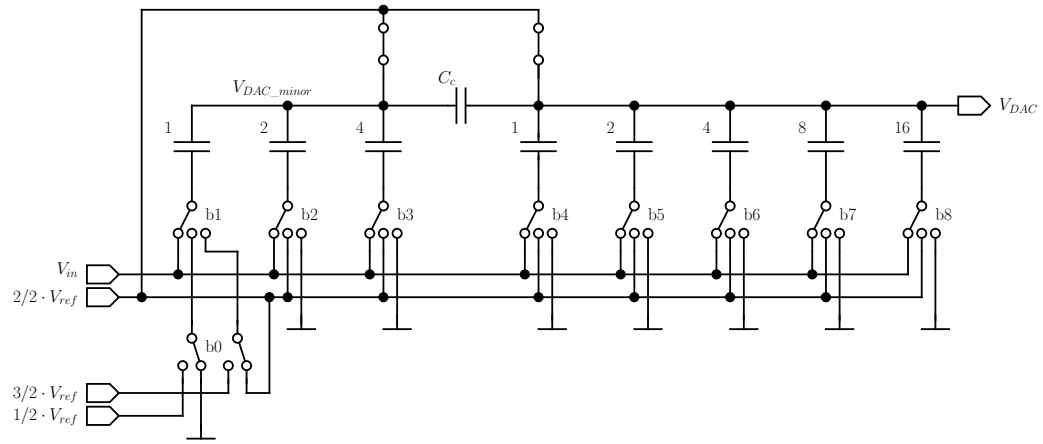


Figure 4.4: Basic split-capacitor array DAC with resolution extension

parasitic capacitance on the node V_{DAC_minor} has to be negligible. For now the decision to make the resolution distribution uneven seems to be a bad choice, since non-unit element sized devices are hard to match, but later on when trimming is introduced the error can be compensated.

This split structure also comes with a couple of new problems. First, the parasitic capacitance on V_{DAC} is not an issue but the capacitance on V_{DAC_minor} is. Such a capacitance detunes the influence of the minor array compared to the major array which would result in a bad Differential Non Linearity (DNL). Also a non-ideally sized coupling capacitor has the same influence due to matching. Nevertheless, up to certain resolutions these obstacles can be tackled and many published SAR ADCs rely on this basic structure. Subsequently an improved implementation is gradually introduced.

As a first step to enhance the structure it is possible to increase the resolution of the converter without additional capacitors in the array. How such an additional single bit can be achieved is depicted in Figure 4.4. As ever smaller voltage steps on V_{DAC} are necessary but no smaller capacitors in the capacitive array should be introduced, additional voltage steps on the bottom plates of the capacitor groups can be introduced. By applying voltage steps half of the reference voltage to the smallest capacitor group in the minor array, one additional bit of resolution can be added.

To add another bit of resolution, steps one fourth of the reference voltage are necessary. This in

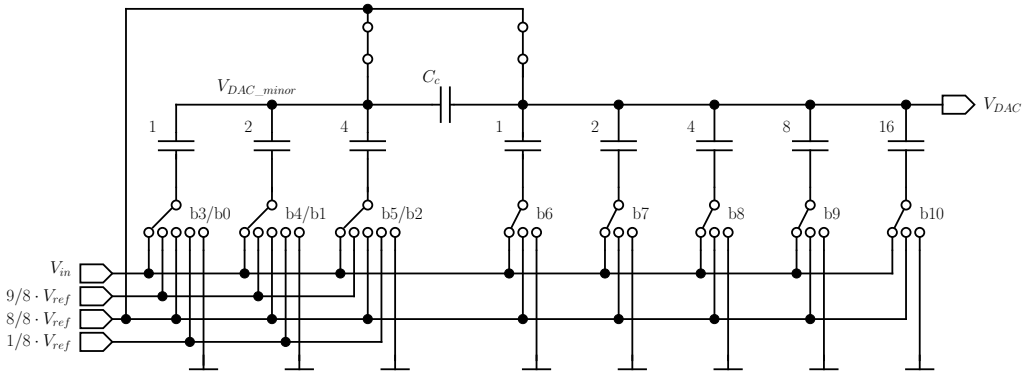


Figure 4.5: Basic modified split-capacitor array DAC with resolution extension

theory can be carried on to infinite resolution, but in reality mismatch of the capacitor array, the reference voltages and noise limit the maximum achievable resolution. Also, it is obvious that since the voltage at the bottom plate of the last capacitor group has to be varied around its last value, reference voltages higher than the reference voltage itself are necessary. For high numbers of additional bits the highest needed reference voltage would approach two times V_{ref}. As the reference voltage itself should not be too low to increase the input voltage range of the converter and to maximize the voltage swing and thus signal to noise ratio, the supply voltage itself would have to be at least two times as high as the reference voltage as well.

As an alternative approach the voltage steps can be applied to the bottom plate of the optional capacitor in the minor array if this capacitor is implemented. This has the inherent advantage that no voltages higher than V_{ref} are necessary. It even seems to cut the needed number of scaled reference voltages in half, as only the lower half is needed. Still, this concept was not implemented, as the number of necessary scaled reference voltages for the previously shown architecture can be reduced even more dramatically, as will be shown subsequently.

To overcome the need for high supply voltages without the optional capacitor a modification can be done to the circuit as shown in Figure 4.5. As depicted three additional bits are added to the basic eight bits of resolution. In this concept, after the eighth bit, instead of changing the voltage of the smallest capacitor group by half, the reference voltage of four capacitors are changed by one eighth the reference voltage. This has the same influence on the output voltage of the overall DAC. Another two bits are added by changing the two capacitor and one capacitor group by one eighth of the reference voltage. As can be seen three additional bits can be achieved with the highest necessary reference voltage of $9/8 \cdot V_{ref}$, which is a significant improvement.

The difficulty lies in designing a buffer that is able to work with the lowest needed voltage of $1/8 \cdot V_{ref}$. The switching scheme thus can be changed again as depicted in Figure 4.6. First all single capacitors are split in two to be able to design a common centroid layout, which is essential for good matching. This enables the partial individual steering of the bottom plates of the capacitors in the capacitor groups. Now the ninth bit of resolution is done as follows. If the last voltage on the capacitor group with eight capacitors was ground after the eighth bit, only one of the eight gets set to $8/8 \cdot V_{ref}$. This has the same effect on V_{DAC} as before when setting the smallest capacitor group to half of V_{ref}, but no additional reference voltage is needed. When

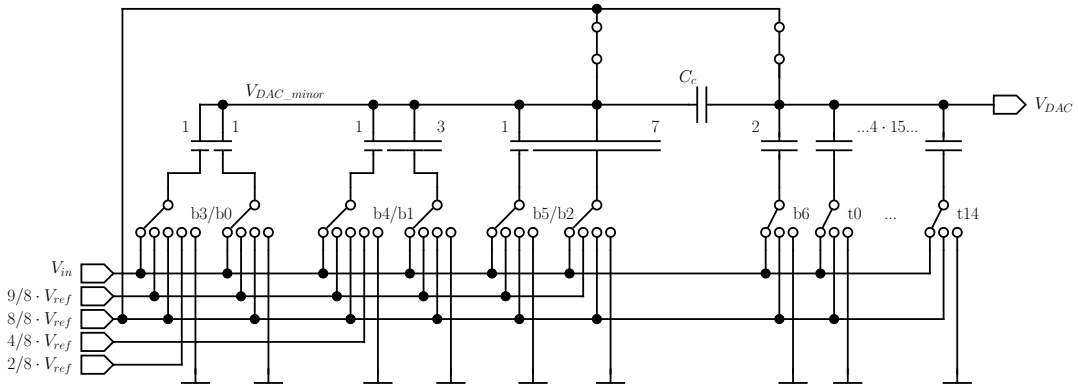


Figure 4.6: Modified split-capacitor array DAC with resolution extension

the voltage at the capacitor group was already $8/8 \cdot V_{ref}$ all eight capacitors get set to $9/8 \cdot V_{ref}$. Again the voltage step on V_{DAC} stays the same. For the tenth bit the same is done, only for the transition from ground another reference voltage, $4/8 \cdot V_{ref}$, has to be introduced to achieve a correctly sized voltage step. This voltage, though, is already high enough to be handled by a standard buffer as shown later. The eleventh and last bit again needs an additional voltage of $2/8 \cdot V_{ref}$. This would require another buffer, but due to the fact that only one very small capacitor gets connected to this voltage, a dedicated buffer can be left out without a severe deterioration of the reference voltages.

Also introduced in this design step is a thermometer scaling of the top four bits, which drastically reduces DNL and improves Integral Non Linearity (INL). The conversion from binary code to thermometer code is done by a couple of logic gates, which during operation consume some additional power. Also, the number of wires going to and from the capacitive array increases but still can be handled.

With the so far presented structure good results can be achieved, as was shown in [72], but the problem of limited matching of the coupling capacitor remains. Certain publications propose a trimming or calibration of this capacitor but this always means an interference into the otherwise mostly homogeneous capacitive array. The circuit as shown in Figure 4.7 introduces a separate reference voltage scaling between the two sub arrays. The major array keeps working with the original reference voltage, which also is the reference voltage which can have the lowest noise. The minor array works with scaled versions of the slightly tunable reference voltage V_{ref_tune}. This scaling enables the circuit to compensate for matching and scaling errors of the coupling capacitor C_c. Due to this C_c can be built of unit elements.

The final architecture contains a few more changes as depicted in Figure 4.8. First the switches are broken into smaller sub switches to simplify the layout. Also, the bottom plates of the minor array do not get reset to V_{in} but ground instead. This gives a very much appreciated reduced input capacitance but no further influence on the conversion efficiency. Only a tiny constant offset of the output value can be observed as the node V_{DAC_minor} operates at lower voltage levels during the conversion process.

Additionally, another technique is applied to this ADC which introduces the possibility of shifting

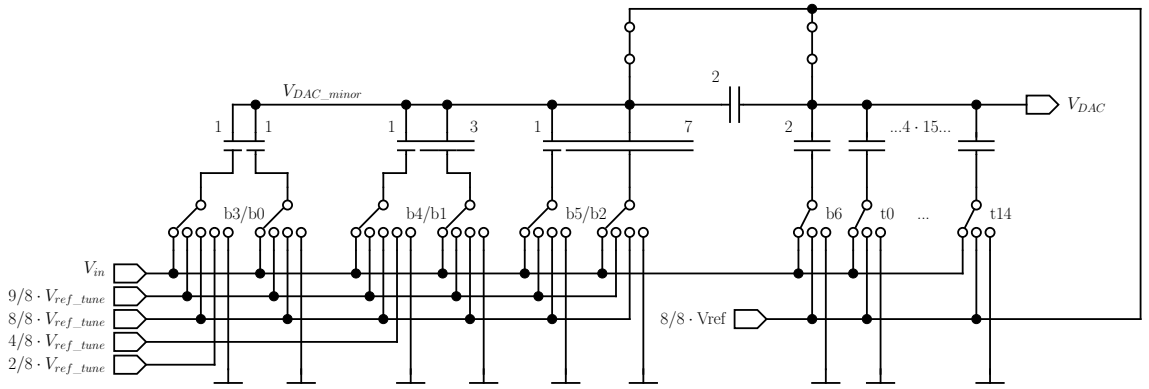


Figure 4.7: Modified split-capacitor array DAC with resolution extension and trimming capability

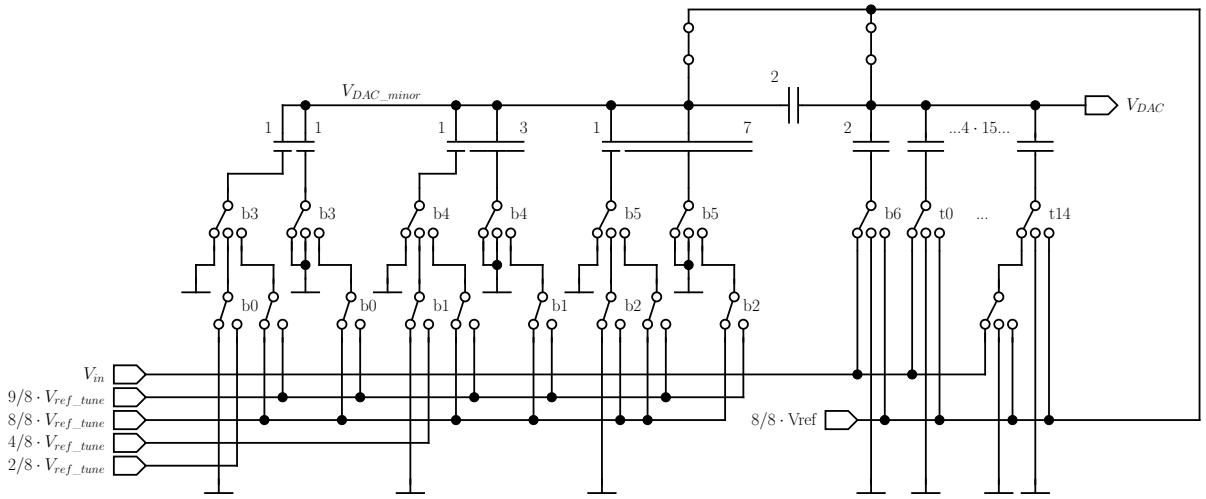
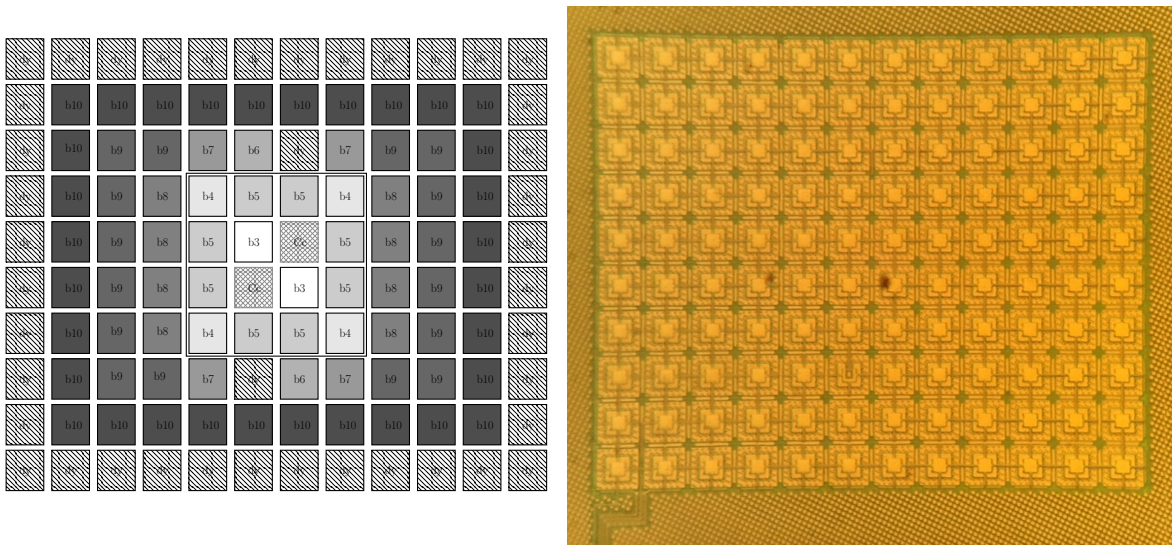


Figure 4.8: Modified split-capacitor array DAC with resolution extension, trimming and input voltage scaling capability

or scaling the input voltage range according to the principle protected by the patent found in [73]. This is done by not connecting all bottom nodes of the major array to V_{in} during reset. The more capacitors are connected to ground during reset the higher the maximum input voltage can get. A shift can be applied by connecting the capacitors partly to V_{ref} rather than ground. Various input ranges are possible and results shown in the measurement section.

The final capacitor array was chosen to have 8 bits in total, with 3 bits at the minor side and 5 bits at the major side. The 4 most significant bits b7 to b10 are converted from binary code to thermometer code t0 to t14 to improve linearity. This configuration consists of a total of $1 + 2 + 4 + 1 + 1 + 2 + 4 + 8 + 16 = 39$ capacitors. To be able to make a common centroid layout and to enhance matching each capacitor consists of two capacitor unit elements with a size of 50 fF each which doubles the aforementioned amount. This gives a total capacity of 3.2 pF of the major array and a kT/C noise of 36 μV which is still significantly lower than the expected LSB step size. The capacitor size was chosen larger than the kT/C limit imposes due to matching. The capacitors are realized with stacked Metal-Oxide-Metal (MOM) capacitors and their capacitance was determined by layout extraction.



(a) Schematical view (b) Micrograph view

Figure 4.9: Common centroid layout of capacitor array

The array as implemented is depicted in Figure 4.9a and a detailed micrograph of it is also included in Figure 4.9b. The array is enclosed by a ring of dummy devices which were used for supply voltage buffering. Two additional dummy devices within the array are necessary to be able to generate an optimal placement of all capacitors. The minor side of the array and the coupling capacitors are in the middle, surrounded by the major side. The two DAC nodes sensitive to parasitics are realized in top metal and the connections to the bottom plates of the capacitors are routed at a low metal in-between the capacitors. Filling and cheesing of the metal layers is turned off in the area to avoid unwanted coupling capacitances. The connection to the DAC node of the minor side is especially sensitive to parasitic capacitances, thus its only connection to devices other than the capacitors themselves, the reset switch, is placed directly into the array in one of the two dummy capacitor cells that are directly placed inside the array. The connection from V_{DAC} to the comparator can be seen in the lower left edge of the micrograph. This connection is realized as short as possible and a shielding metal layer resides beneath it since coupling capacitances from digital signals to this node would decay the performance severely.

4.2.3 Reference Scaling

The ADC can be operated in the high accuracy/high power mode with 11 bit resolution or the low accuracy/low power mode with 8 bit resolution. Figure 4.1 shows the basic structure of the ADC and the reference scaling. For simplification several switches that allow bypassing the buffers are not shown in the figure.

In the 8 bit mode only one reference voltage is needed thus no reference scaling is needed and no static power consumption is necessary. It is, though, possible to use the scaling to trim the reference voltage in the minor array to fit the major array, but the conversion performance degradation at

8 bit resolution, due to the coupling capacitor mismatch, is very small. Depending on use case buffers B1, B2 and OTA1 need to be enabled in this mode.

When higher accuracy measurements are desired the reference scaling has to be active, meaning at least OTA1 has to be enabled. It regulates the voltage on the eight tap of a resistive ladder with nine resistors in total close to the reference voltage input. This way nine taps with voltages between $1/8 \cdot V_{ref}$ and $9/8 \cdot V_{ref}$ in $1/8 \cdot V_{ref}$ steps are available. For the steering of the capacitive array only the $2/8 \cdot V_{ref}$, $4/8 \cdot V_{ref}$, $8/8 \cdot V_{ref}$ and $9/8 \cdot V_{ref}$ taps are required. To allow trimming of the overall scaling of the two capacitive arrays the resistors are split into 32 sub-resistors each. An analog multiplexer makes it possible to pick the feedback voltage for OTA1 from 16 sub-taps that are created by the sub-resistors around the $8/8 \cdot V_{ref}$ tap. Individual trimming of $2/8 \cdot V_{ref}$, $4/8 \cdot V_{ref}$ and $9/8 \cdot V_{ref}$ is also possible with three additional multiplexers with 4 pick options each. The overall area share of the reference scaling without the buffers is about 13 % of the total area of the ADC.

In either mode it is possible to drive the capacitor array with unbuffered voltages from the reference input and the reference ladder or the buffers B1 to B4 can be used. The unbuffered mode can be used to save power at low conversion rates when settling times are sufficiently long. B2 to B4 are standard current mirror OTAs whereas B1 is a class-AB OTA [26]. As these amplifiers are tricky to stabilize for varying capacitive loads, an additional capacitor can be connected to the output of B1 when the capacitive load the capacitor array poses is small. Thus an approximately constant load can be ensured.

4.2.4 Time Domain Comparator

In order to be able to provide an ADC which scales its power consumption to the rate of conversion a comparator architecture with no static current draw was chosen. The principle is based on the conversion of analog input voltages to digital pulses in the time domain as proposed in [74, 64].

The comparator as can be seen in Figure 4.11 incorporates two three stage voltage to time converters as depicted in Figure 4.10. Before each comparison in each of the two converters capacitors C_1, C_2 and the parasitic capacitance on the node connected to the drains of N6 and P3 are discharged by transistors P1 and N5 by the appropriate signals Reset and ResetN. The comparison itself starts with the low-high transition on the Clk signal which has to be supplied to the circuit. ClkD is a buffered version of Clk and is used in the voltage to time converter on transistor N4 to start the current flow in the first branch. To reduce charge injection into this first stage current path the inverted signal ClkN is fed to the dummy transistor N2. As the signal EN_Charge is high at this point in time, current can start to flow in this branch through N1 and R or N8 out of C_1. Thus the voltage level on C_1 begins to decrease, which at some point starts to make P2 conductive. This results in a current being injected in stage two which accumulates into C_2. Thus the voltage on C_2 increases, which is also the voltage at the gate of N6. N6 combined with P3 form the third stage in this design but in this stage only the parasitic drain capacitances of N6, P3 and gate capacitances of P4 and N7 are used. The output signal of the third stage is fed to a normal inverter, which forms the output of the converter block. In each of the three stages the slew rate of the voltage is increased. The inverter then finally makes the low-high transition as fast as possible in the given technology. The slew rates and thus the time it takes for the low-high transition to occur at the output of each converter cell depends on a number of

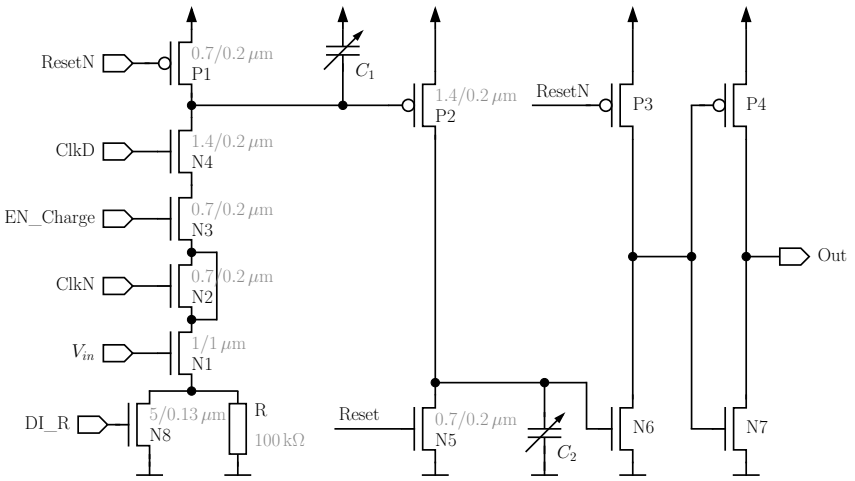


Figure 4.10: Voltage to time converter

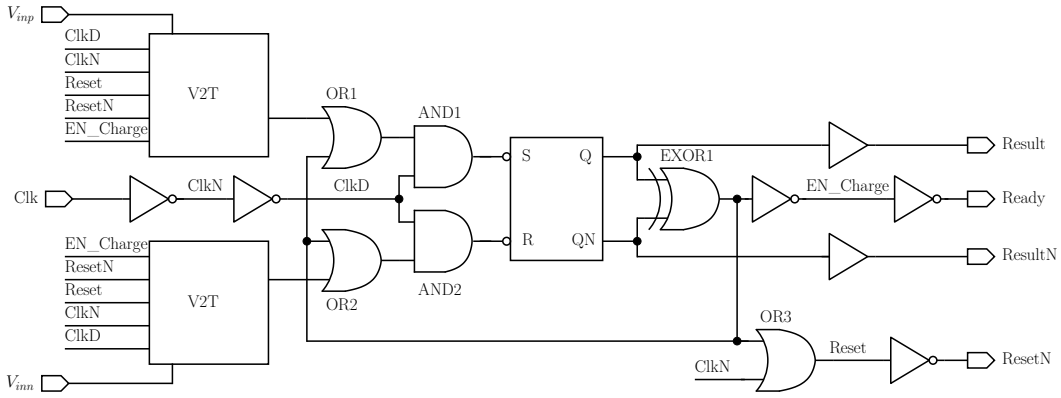


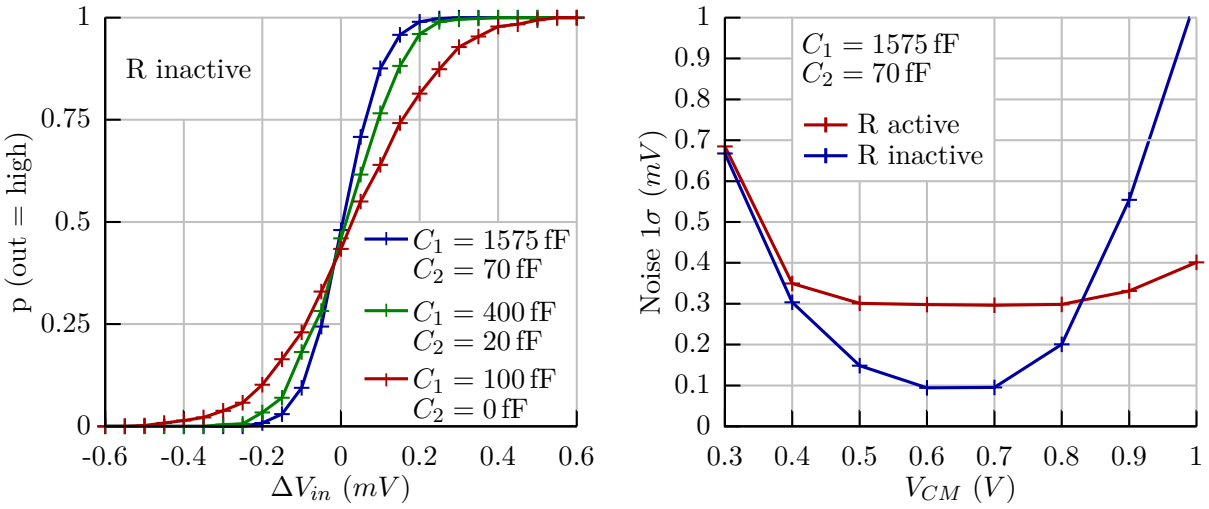
Figure 4.11: Time domain comparator

factors. All factors should have the same relative influence on this time. Only one factor, which is a different input voltage at the two transistors N1 distinguishes the two voltage to time converters.

As depicted in Figure 4.10 instead of only one integration capacitor, two are used which are implemented as configurable in size. This allows changing the noise and power consumption of the comparator. The sizes are independently digitally controllable for both branches which additionally allows offset calibration. C1 consists of binary scaled MOS capacitors with a resolution of 6 bit and an estimated capacity of 25 fF per unit cell. Thus capacities between 0 fF and 1575 fF can be selected. C2 is configurable by only 3 bit and the capacitor unit cell is just 10 fF in size.

Additionally, a rather wide transistor ($R_{ON} \approx 1\,\mathrm{k\Omega}$) is connected in parallel to resistor R, which has a resistance of 100 kΩ so that it can be bypassed on request.

Figure 4.11 shows the top level of the comparator, which includes two voltage to time converter cells and a few logic gates. The faster of the two signals from the V2T cells decides which state the flip-flop is put into. If a clear decision was made, EXOR1 recognizes the difference between the normal output Q and the negated output QN. As soon as this state is reached the current flow into



(a) Output value probability for different capacitor settings at 600mV common mode voltage

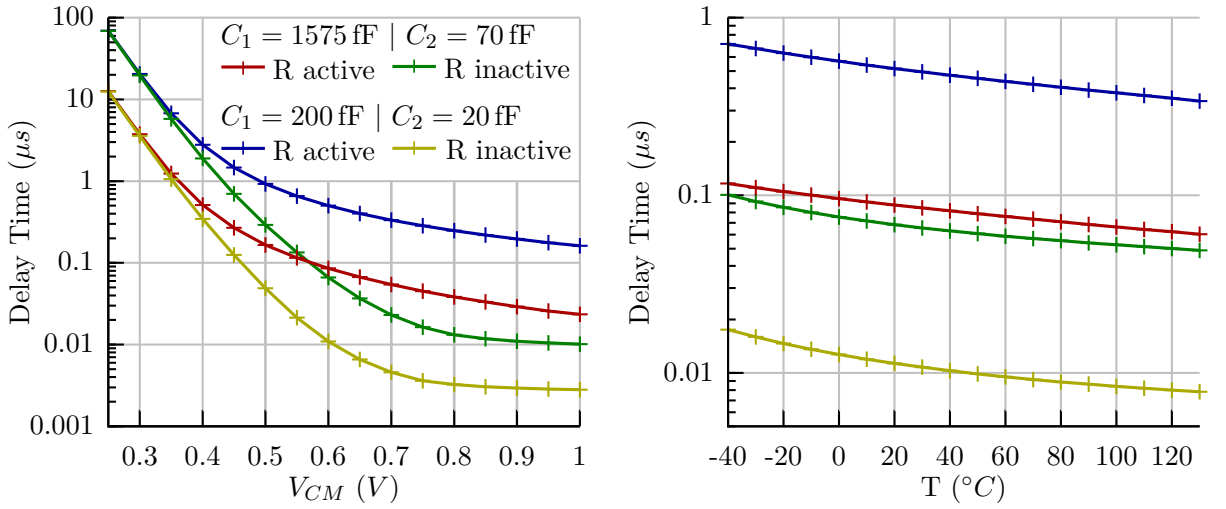
(b) Noise over common mode voltage

Figure 4.12: Noise characteristics of comparator

the capacitors of the V2T cells is immediately stopped, and they get reset for the next comparison. In addition to that, both inputs of the flip-flop are forced to high via OR1 and OR2 so that the result is stored even during the reset of the V2T cells. This procedure saves energy, as there is no use in further charging the capacitors when the decision has already been made. Still, the delay from the gates is sufficient to avoid meta-stability at the output of the comparator. It is important to load the two outputs of the flip-flop with rather small and equal loads, otherwise an offset voltage will arise. Thus two digital buffers were added to be able to connect it to the SAR unproblematically.

To investigate the behavior of the comparator multiple simulations have been performed using the extracted netlist. Figure 4.12a shows the probability of the comparison result being low or high over a differential input voltage while the DC input level is held at a constant 600 mV. Due to the fact that the probability for a false comparison follows a normal distribution the plot forms a Cumulative Distribution Function (CDF). As can be seen with three different capacitor configurations bigger capacitors lead to a steeper slope and thus better comparison. For this and several of the following simulation results rather computational expensive calculations have to be performed. Transient simulations have to be done for every step on the x-axis with transient noise enabled with a sufficiently high maximum noise frequency and a sufficiently high number of comparisons for each point. An automated script performs the parameter sweeps and evaluates the resulting probability for the comparison result.

One can also describe the probability with a $1\,\sigma$ standard deviation number as shown in Figure 4.12b. The x-axis in this plot represents the common mode voltage level of the two comparator inputs and the y-axis represents the differential voltage difference at the input needed to get a $1\,\sigma$ deviation at the output, which means 36.8 % of the comparisons have to be high or low. This value is determined by simulation of the whole CDF, which then was fed to the built-in curve fitting toolbox of MATLAB®. This tool searches the best fitting CDF and outputs its parameters. The



(a) Over common mode voltage at room temperature (b) Over temperature at 600mV common mode voltage

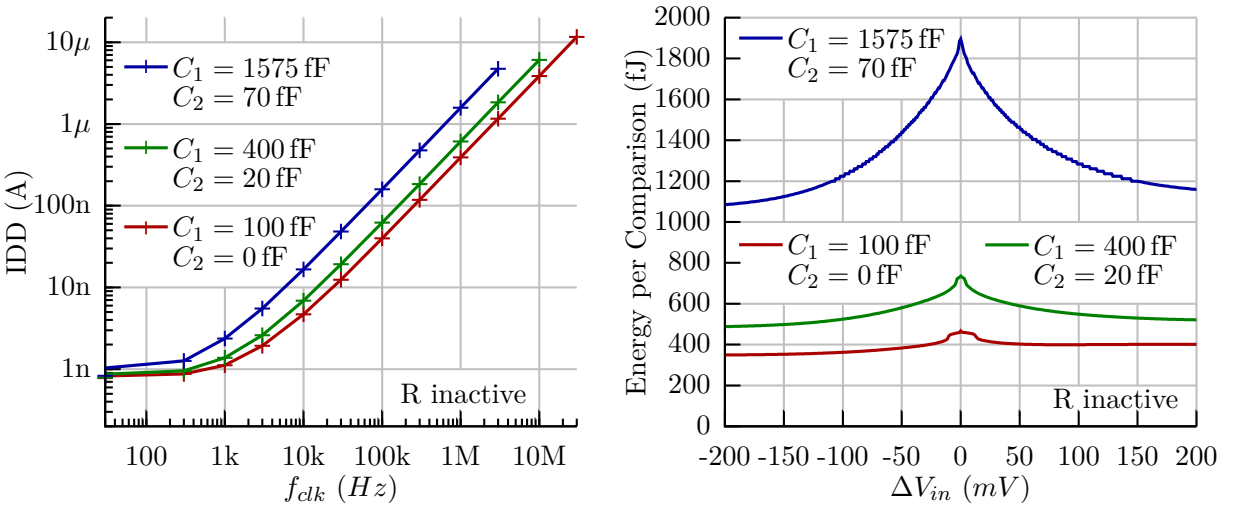
Figure 4.13: Delay time of comparator

sigma value is used in this plot, and it can also be called the input referred noise. As mentioned earlier the comparator can be operated with or without resistor R, which is why two curves are plotted here and in the following plots. The plot shows that the noise level of the comparator is lowest for common mode voltages of about 650 mV which fits very well with the intended use case, which is a bandgap as reference voltage with 620 mV output voltage. It can also be seen that the noise level with activated resistor increases up to three fold at this voltage level. For very low voltages the noise levels are almost the same and for high voltage levels above 850 mV the resistor even starts to become an advantage. This is due to the fact that at high voltages the voltage to time converter cells become very fast and the noise level becomes determined by the flip-flop. The resistor in this case can limit the speed of the voltage to time converters and thus limits the noise level.

To investigate the speed of the comparator a simulation of the delay time over the common mode voltage level and for different capacitor and resistor settings was performed as shown in Figure 4.13a. This simulation also has to be performed with transient noise, as an ideal simulation without noise would suggest a flip-flop stuck in the middle for zero differential input voltage. The plot shows that the delay time of the comparator changes by several decades over the input voltage range. For very low voltages the resistor is insignificant as no substantial voltage drop can occur across it due to the low currents. For high voltages it increases the delay time by a factor of 5 to 10. Also, the capacitor setting has a significant influence of more than one order of magnitude.

As the threshold voltage of N1 in the time to voltage converters changes over temperature this influence on the delay time also has to be considered. Therefore, Figure 4.13b shows the delay time over temperature. A variation of up to a factor of 3 can be seen from -40 to 130 °C.

A comparator should achieve a low noise comparison with as little current consumption as possible. Figure 4.14a shows the average current consumption of the comparator at 1.2 V supply voltage over clock frequency. The input differential voltage is set to zero so that transient noise is again needed.



(a) Over frequency at 1.2V supply voltage

(b) Over input voltage difference at 1.2V supply voltage and with one input fixed to 600mV

Figure 4.14: Current consumption of comparator

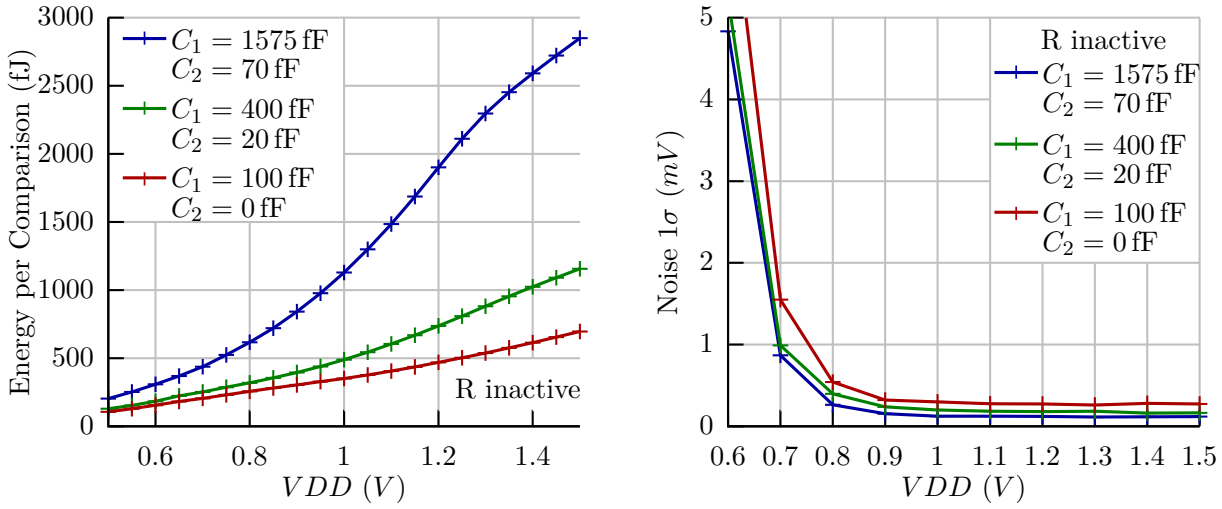
The plot shows that the current consumption of the comparator scales very well over frequency. Only for frequencies below 1 kHz does leakage become dominant. Increasing the capacitor values in the voltage to time converters leads to an increased current consumption as expected.

Figure 4.14b depicts the energy consumption per comparison at 1.2 V supply voltage. For this plot one input of the comparator was held at a constant 600 mV while the other was swept up and down by 200 mV from this point. This way the common mode voltage does not stay the same, but the process within the ADC is better modeled, as there one input is also always fixed to the reference voltage while the other one is determined by the DAC. Nevertheless, as a result the curves are not symmetrical around the center. The center where both input voltages are the same consumes the most energy per comparison as the flip-flop needs the longest time to make its decision. In the SAR ADC this point is searched by the algorithm, so most likely the comparisons for the first bits of resolution will consume less energy than for the last bits.

As Figure 4.15a and Figure 4.15b show, one can reduce the energy per comparison by lowering the supply voltage. The energy consumption can be reduced by a factor of 10 going from a 1.5 V to a 0.6 V supply. The problem, though, is that the noise significantly increases for low supply voltages. This noise is again generated by the flip-flop as it needs more time to make a decision.

4.2.5 Successive Approximation Register

The digital SAR was implemented in two different variants and is responsible for steering the conversion process while remembering the comparison results from the comparator. Both variants are connected to the same power supply as the analog part of the ADC. The inputs to this block are a clock signal, the result and ready signal from the comparator and a signal to determine the desired resolution of the conversion. The outputs are a reset signal to sample the input signal



(a) Energy consumption per comparison over supply voltage

(b) Noise over supply voltage

Figure 4.15: Noise level and energy consumption over supply voltage

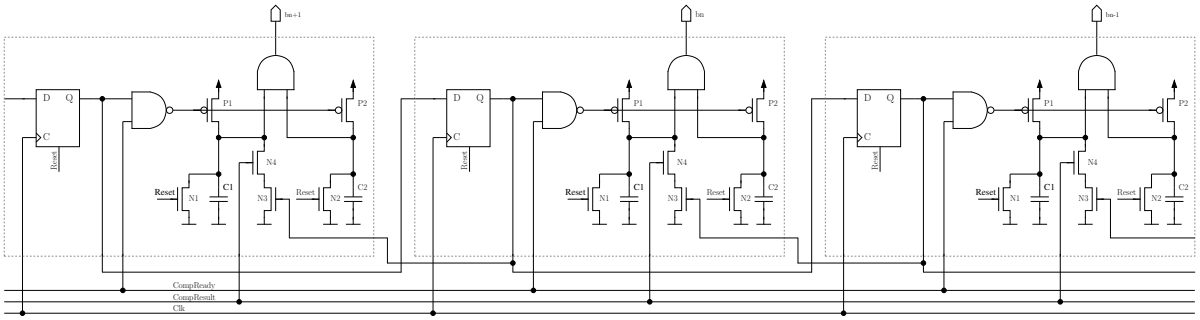


Figure 4.16: Successive approximation register build with static and dynamic logic

on the capacitor array, the eleven data bits which also steer the voltages at the capacitors, three signals to enable certain buffers only when they are needed and a conversion complete signal to signal blocks in the system that a completed conversion result is available.

The first implementation of the SAR uses a combination of static and dynamic logic. It is configurable to be used for the 8 and the 11 bit mode. Each bit in the conversion is implemented by a logic cell. Three of these cells and their interconnections are shown in Figure 4.16. Each cell consists of a static logic flip-flop which in combination with the other cells forms a shift register. A single logic one is shifted through this shift register during the conversion and the cell with the one at the flip-flop is the currently active cell. During the reset phase the capacitors $C1$ and $C2$ are discharged via N1 and N2. If a cell is active and the comparator ready signal goes to high at the same time, both capacitors are charged to VDD via P1 and P2. This is necessary to set the data bit at the output of the cell, as the voltages of both capacitors are connected to an AND-gate. $C1$ gets discharged again if the result of the comparator was a one, meaning the voltage of the DAC was higher than the reference voltage, which means the last bit has to be reset. This discharge

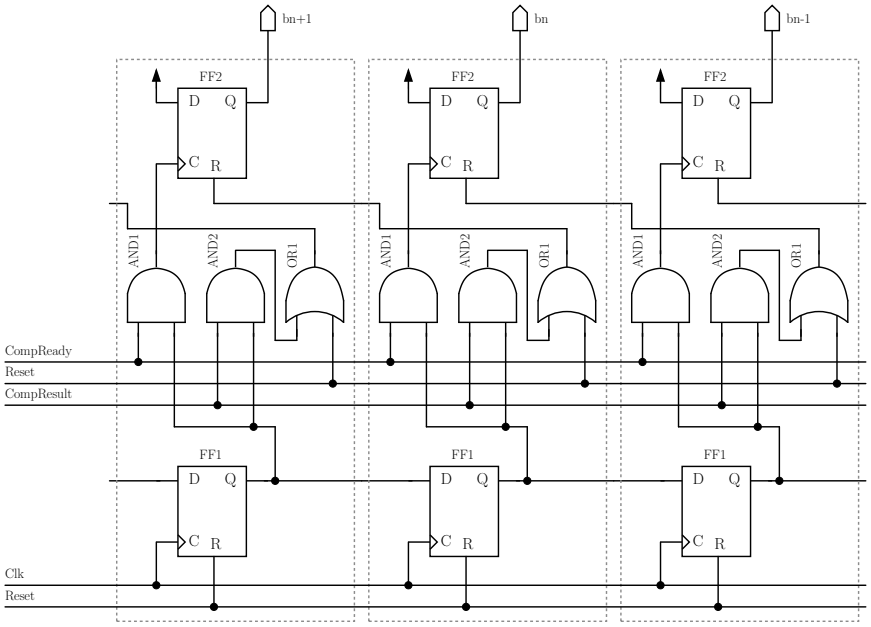


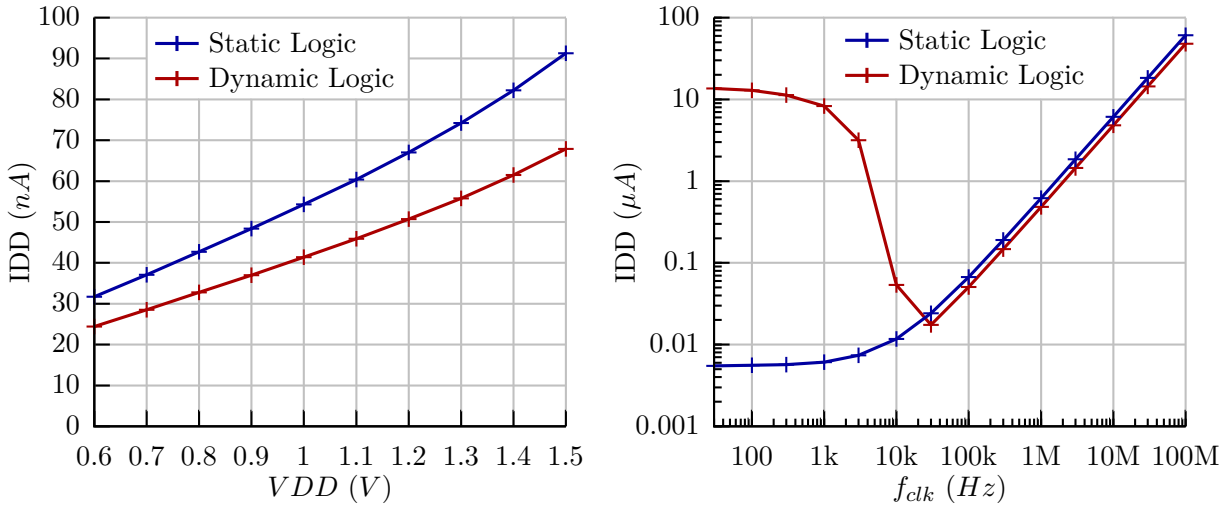
Figure 4.17: Successive approximation register build in static logic

path is only active if N4 is active, which receives a fed back signal from the next cell.

The second alternative implementation, as shown in Figure 4.17, consists only of static logic. Again cells are formed which each represent a single bit of resolution and consist of two flip-flops and three combinatory gates. The combination of all FF1s again forms a shift register where a single one is shifted through. When a cell becomes active and the comparators comparison from the previous bit is finished FF2 gets set to high which puts a high to the corresponding switch in the DAC. If the reset signal is set to high or the result of the comparator for this bit is high, FF2 gets reset to zero.

The feedback is needed in both implementations as each cell waits for the comparator to finish. The timing is designed in a way so that during the time a cell is active the DAC can settle. Only at the end of the activity of the cell is the comparator triggered and the next cell waits with its operation until the comparator has finished. As shown in the simulations of the comparator the time it takes to do the comparison is significantly shorter than the time the settling takes. Thus an almost constant settling time for each step can be provided. Only for very high conversion rates and slow settings of the comparator does the delay of the comparator have to be considered more closely.

Figure 4.18 shows the simulated current consumption of the static and dynamic version over supply voltage at 100 kHz clock rate and over the clock rate at 1.2 V supply voltage. To include the influence of parasitic capacitors due to wiring, the extracted netlist was used. It can be seen that for frequencies over 30 kHz the dynamic logic achieves a rather consistent 25 % current consumption advantage over static logic, independent of supply voltage. For frequencies below 30 kHz, though, problems arise for the dynamic logic variant. Due to leakage the small capacitors $C1$ and $C2$ charge or discharge to an extent so that the AND-gate becomes conductive and drains considerable amounts of current from the supply. Also, the information stored on the capacitors is lost as a result and no correct conversion can be performed anymore. Measurements of the ADCs



(a) Over supply voltage

(b) Over clock frequency

Figure 4.18: Current consumption of successive approximation register logic at room temperature

showed that there is less leakage at room temperature than simulated, so that frequencies down to 10 kHz are possible. The capacitors could be increased in size to further decrease the minimum operating frequency but this would, at the same time, increase the current consumption. The explained behavior was the decisive factor in choosing to use the static logic over the dynamic logic for the third evolution step of the ADC. Nevertheless, the static logic also suffers from leakage, which results in a current drain of single digit nA values at room temperature.

4.2.6 Area Shares

Table 4.1 shows the relative area shares of the proposed ADC.

4.2.7 Measurement Results

Figure 4.19 shows the measured transient operation of the ADC in 11 bit mode with a result value of 10101010101 in binary representation. Twelve clock cycles are needed to complete one conversion. The first clock cycle in each conversion is used to sample the measurement voltage on the capacitor array. During this phase it can be seen that the voltage V_{DAC} is set to the reference voltage of 600 mV. During conversion it again converges to this voltage level but a small constant offset remains which is caused by losses during the charge redistribution process and the parasitic capacitances prior to the first step.

$8/8 \cdot V_{ref}$ is fed by buffer B1 which is active during the whole conversion cycle. A large drop of this voltage can be seen for the four first bits of resolution, and one additional drop after the fourth bit. Subsequently only small deviations from the intended voltage can be measured, since they are only induced indirectly from the minor array. For the next four bits of resolution $8/8 \cdot V_{ref\_tune}$ is needed, which is why buffer B3 gets activated after the fourth bit of resolution. The lowest three bits require the voltages $9/8 \cdot V_{ref\_tune}$ and $4/8 \cdot V_{ref\_tune}$, which are buffered by B2 and B4, and $2/8 \cdot V_{ref\_tune}$ which is taken directly from the reference ladder. After the last conversion by the

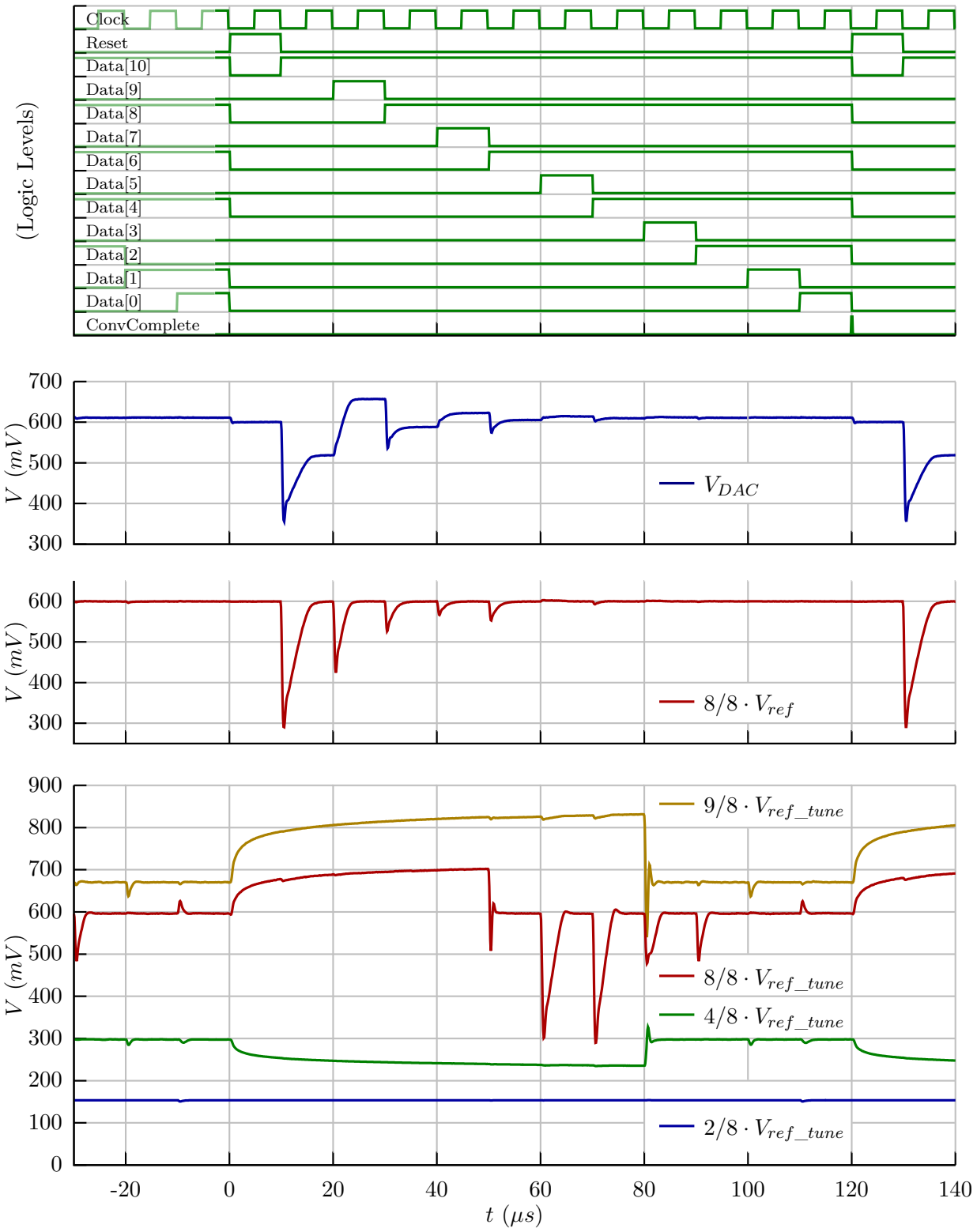


Figure 4.19: Measured transient operation of the ADC in 11 bit mode

Table 4.1: Area shares of components of the ADC

Component	absolute area	relative area
Capacitor array	0.031520 mm^2	43.4 %
Reference scaling	0.009120 mm^2	12.6 %
Buffers	0.006600 mm^2	9.1 %
Comparator	0.003956 mm^2	5.4 %
Logic	0.002680 mm^2	3.7 %
Wiring	0.016995 mm^2	23.4 %
Stabilizer capacitors	0.001764 mm^2	2.4 %
Total	0.072635 mm^2	100 %

comparator a short pulse is generated on the conversion complete signal, which can be used to latch the conversion result into a register. To save power with the conversion complete signal all buffers but B1 are disabled, which is why their output voltage floats until they get activated again. Subsequently the process starts over again for the next conversion.

Figure 4.19 shows the digital output value of the ADC for a sweep in input voltage and a fixed reference voltage of 600 mV. As mentioned before, different capacitor settings can be chosen during reset phase, which results in the transfer curves shown. The default mode is represented by the red line, which shows that the input range roughly covers voltages from 0 mV up to the reference voltage. By changing the capacitor setting represented by the green and blue line the upper input range can be extended to 850 mV and 1250 mV. Besides this change of slope of the transfer curve, it can also be shifted to lower voltages as shown by the yellow and cyan lines. This way voltages down to −200 mV can be converted. The lower voltage is limited by bulk diodes which are inherently present in the circuit and get conductive for voltages below −200 mV.

As described in Section 4.2.4, the comparator includes two capacitors for each of the two voltage to time converter paths. The first capacitor in each converter cannot only be used to adjust the noise level but also can be used to calibrate an offset voltage or to introduce an offset on purpose. Figure 4.21 shows the measured comparator offset voltage when the capacitor in one path is set to a fixed value of 32 times the unit capacitor and the capacitor in the second path is swept from 0 to 63 times the unit capacitor. As the comparator in most cases will be used with the resistors disabled, an offset voltage of −140 mV to 60 mV can be achieved. Around the center the step width amounts to approximately 2.5 mV.

Figure 4.22 shows the measured DNL of the ADC in 8 and 11 bit mode after calibration. The measurement was performed according to the code density test proposed in [75] with a total of 10 million samples. The achieved peak DNL amounts to −0.08/0.06 LSB in 8 bit and −0.51/0.21 LSB in 11 bit mode. Figure 4.23 shows the INL calculated from the same measurement. The peak INL calculates to −0.12/0.10 LSB in 8 bit and −0.36/0.76 LSB in 11 bit mode.

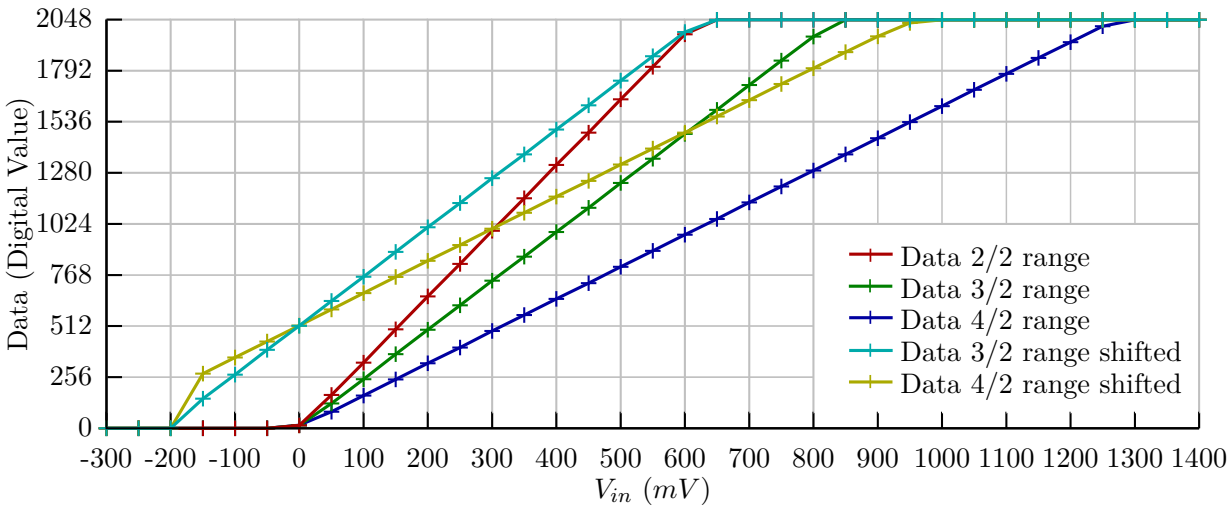


Figure 4.20: Input voltage range measurement of the ADC

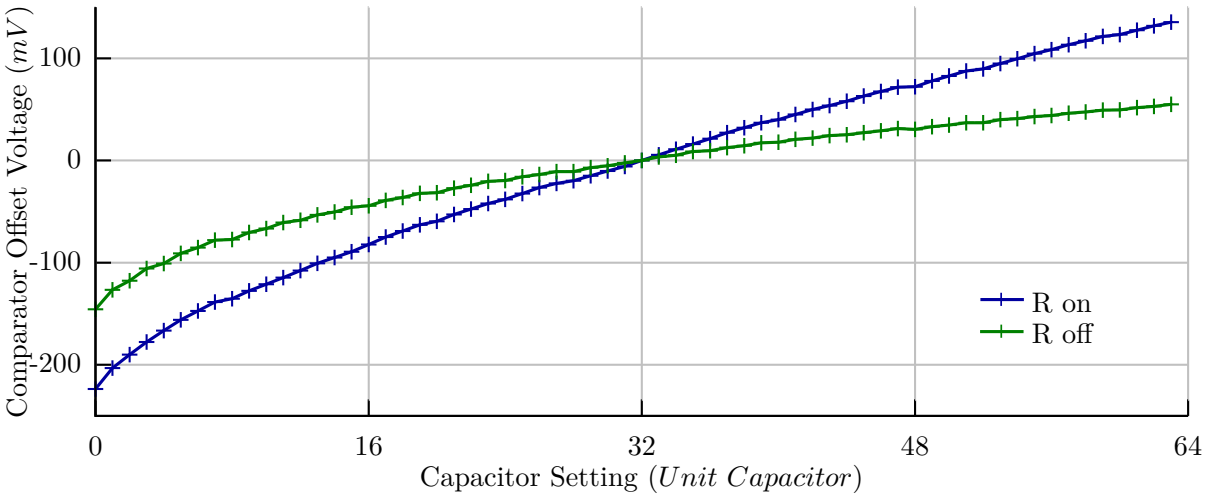
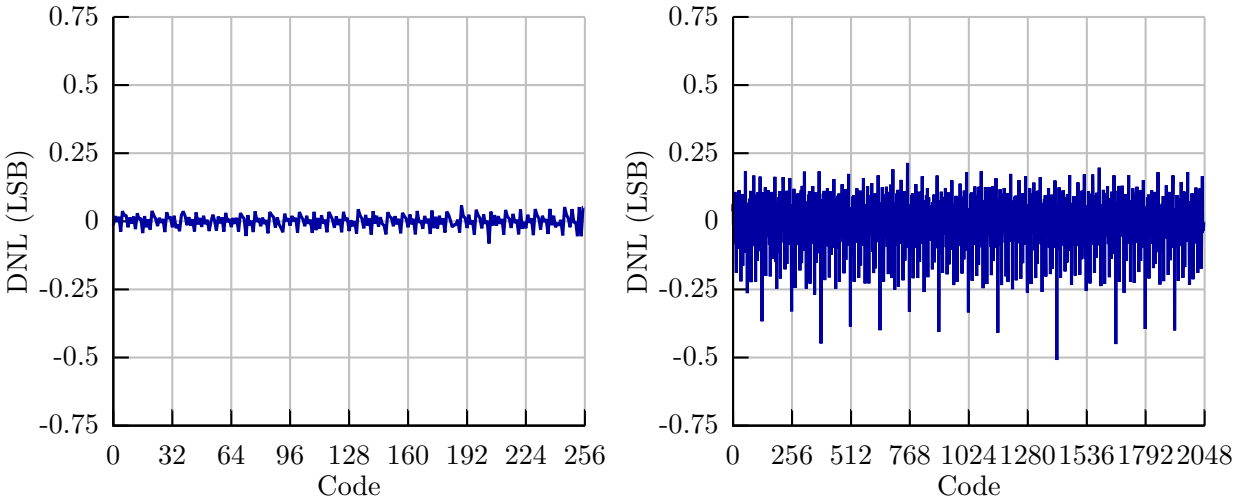
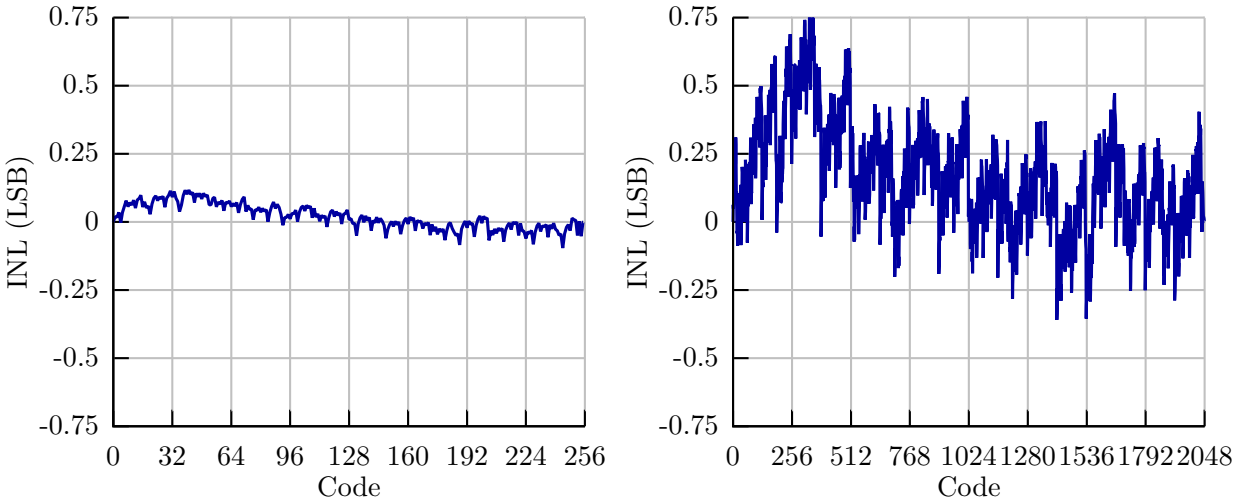


Figure 4.21: Measured offset voltage of time domain comparator for different capacitor settings



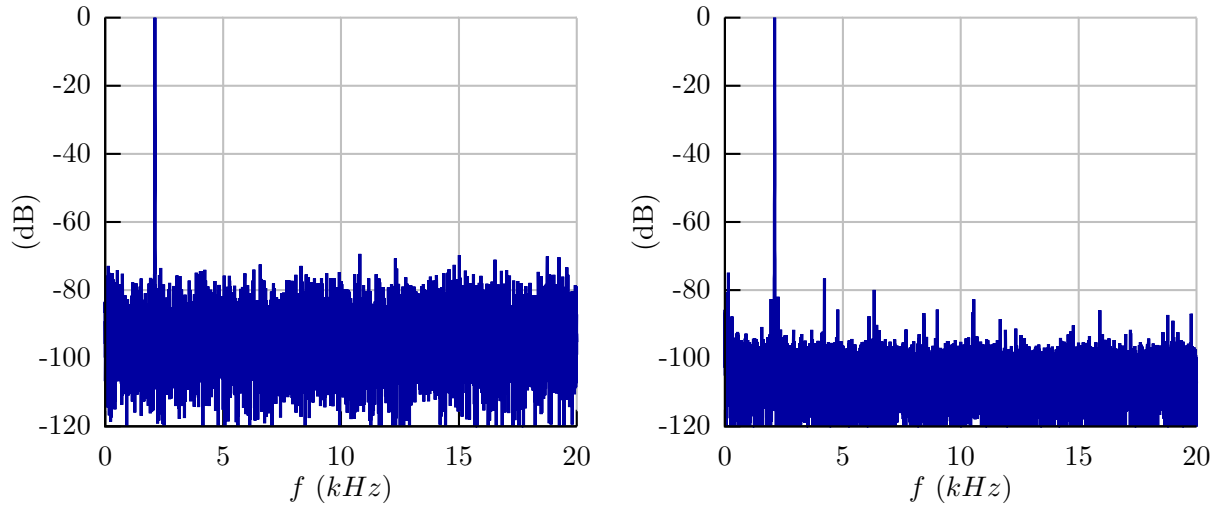
(a) 8 bit mode (b) 11 bit mode

Figure 4.22: Measured DNL of ADC after calibration



(a) 8 bit mode (b) 11 bit mode

Figure 4.23: Measured INL of ADC after calibration



(a) 8 bit mode, 7.946 bit ENOB

(b) 11 bit mode, 9.924 bit ENOB

Figure 4.24: Measured FFT of ADC with 16384 samples at 40 kS/s and 2.1 kHz input signal

Figure 4.24 shows the measured spectral density of 16384 samples sampled by the ADC at 40 kS/s with a close to full scale 2.1 kHz sine at the input and generous biasing of the buffers. From this data the Signal to Noise and Distortion Ratio (SNDR) of the ADC can be calculated. 49.6 dB and 61.5 dB were achieved in 8 bit and 11 bit mode respectively which gives 7.946 ENOB and 9.924 ENOB.

Table 4.2 lists 5 configurations of the ADC and corresponding measurement results. In comparison with the plots in Figure 4.24 for these measurements, the biasing and supply voltage were chosen more aggressively to achieve the best possible FOMs.

Configuration 1 shows the ADC in 8 bit mode with all buffers disabled. This means the major as well as the minor array are fed by the external reference voltage directly, thus a low-ohmic reference is necessary. This way, no calibration of the minor array with respect to the major array is possible resulting in a slightly worse DNL and SNDR. Nevertheless, in this configuration no static current consumption besides the leakage current is needed in the circuit. When clocked slowly, current consumptions of well below 10 nA are possible. For this measurement the clock was set to 90 kHz, which results in a conversion rate of 10 kS/s at just 95 nA current consumption. The supply voltage can be lowered to about 750 mV without deteriorating the performance severely. The aforementioned characteristics in this configuration lead to a FOM of 30.9 fJ/CS according to (4.2.1).

$$FOM = Power/2^{ENOB} f_S \tag{4.2.1}$$

Configuration 2 represents another measurement in 8 bit mode but with Buffer B1 enabled. In this specific configuration B1 is configured to drive the major array as well as the minor array. Thus the use of a high impedance reference source is possible in this configuration, but still, no calibration is possible. To drive the buffer a slightly higher supply voltage of 850 mV is ideal for

Table 4.2: Measurement results and key specifications

Parameter	Config 1	Config 2	Config 3	Config 4	Config 5
Selected resolution	8 bit	8 bit	11 bit	11 bit	11 bit
Reference buffer B1	Off	On	Off	On	On
Scaled reference buffers B2 to B4	Off	Off	Off	Off	On
Reference ladder and OTA1	Off	Off	On	On	On
Supply voltage (V)	0.75	0.85	0.90	0.80	1.40
Current consumption (nA)	95	433	558	603	1865
Sample rate (kS/s)	10.0	20.0	30.0	20.0	20.0
SNDR (dB)	49.01	48.72	58.65	54.74	60.46
ENOB (bit)	7.85	7.80	9.45	8.80	9.75
FOM (fJ/CS)	30.9	82.6	24.0	54.0	152.0

this measurement. The achieved Effective Number of Bits (ENOB) combined with the chosen sampling rate of 20 kS/s and a current consumption of 433 nA result in a FOM of 82.6 fJ/CS. Therefore the calculated efficiency worsens by approximately 63 % just for the buffer.

Configuration 3 represents a measurement in 11 bit mode with the buffers disabled but OTA1 and thus the resistive reference ladder activated. The major array is fed directly by the reference voltage whereas the minor array is fed directly by the reference ladder. In this configuration calibration is already possible and was adjusted manually. At a supply voltage of 900 mV and a current consumption of 558 nA a conversion rate of 30 kS/s and 9.45 bit effective resolution were achieved. This calculates to a FOM of 24.0 fJ/CS.

Configuration 4 changes configuration 3 so that buffer B1 is activated and thus again high impedance reference sources can be used. The minor array is still fed directly by the reference ladder as buffers B2 to B4 are bridged. In this configuration a FOM of 54.0 fJ/CS is achieved, which represents a 56 % decrease in efficiency just for the buffer.

Configuration 5 represents the high performance mode with 11 bit resolution and all buffers activated. In this configuration the circuit is not dependent on the settling times of the reference ladder and its capacitive load but rather the biasing of the buffers. The conversion rate can be set to rather high values and is mostly limited by the conversion time of the comparator and the settling times of the buffers. Measurements were only possible for rates up to 100 kS/s as the microcontroller based measurement equipment can only handle data streams up to this rate. With an oscilloscope it was possible to observe even higher conversion rates but no performance measurements were possible. The shown measurement values in the table are at 20 kS/s with a high supply voltage of 1.4 V and a current consumption of 1.865 μA. An effective resolution of 9.75 bit is achieved which calculates to a FOM of 152 fJ/CS.

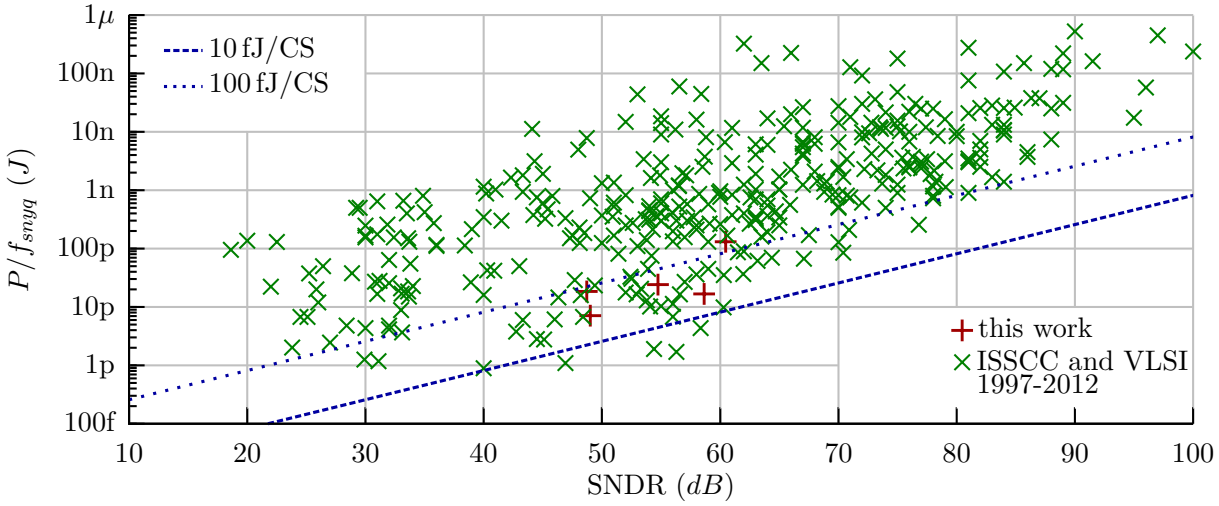


Figure 4.25: Comparison to state of the art

4.2.8 Comparison to State of the Art

A vast amount of publications regarding ADCs is available as quite a few different architectures are known and new CMOS processes constantly require adaptation of the circuits. Thankfully there is a frequently updated publication that collects reported ADC performance characteristics [76], which will be used here to compare the proposed architecture to state of the art work.

Figure 4.25 shows all 359 ADCs that were published at IEEE International Solid-State Circuits Conferences (ISSCCs) and IEEE Int. Symposium on Very Large Scale Integrations (VLSIs) between 1997 and 2012. The chart includes all types of ADCs. On the x-axis the SNDR, representing the quality of the conversion is plotted while the y-axis represents the power consumption divided by the sample rate which is an energy per conversion plotted in joule. This way the power to frequency relation of each ADC is not shown in this plot, which is a good thing, as for many architectures this relation is of a proportional behavior. In the chart efficient points are those that are the farthest down and right, as for those the energy per sample is low while the effective resolution is high. The blue dashed lines represent points where the FOM is 10 fJ/CS or 100 fJ/CS. The five measurements from Table 4.2 are included in the plot and made to stand out by denoting them in red. As can be seen, the proposed ADC is about in the middle of achievable resolution while consuming less than average energy.

Figure 4.26 is a more condensed version of Figure 4.25 with some zoom and only SAR ADCs shown. Also, the designs are differentiated by minimum process dimensions. It can be seen that the proposed ADC can achieve the best efficiency when compared to circuits in the same process node. There are, though, two publications of designs in 180 nm that can beat this design which is realized in a 130 nm process. In general, designs in smaller process nodes can achieve better efficiency as the digital parts in particular can be built to consume less power. The ADCs in the plot which surround this design are also listed in Table 4.3. The table also lists the measured results of the proposed design in 8 and 11 bit mode for all three evolution steps.

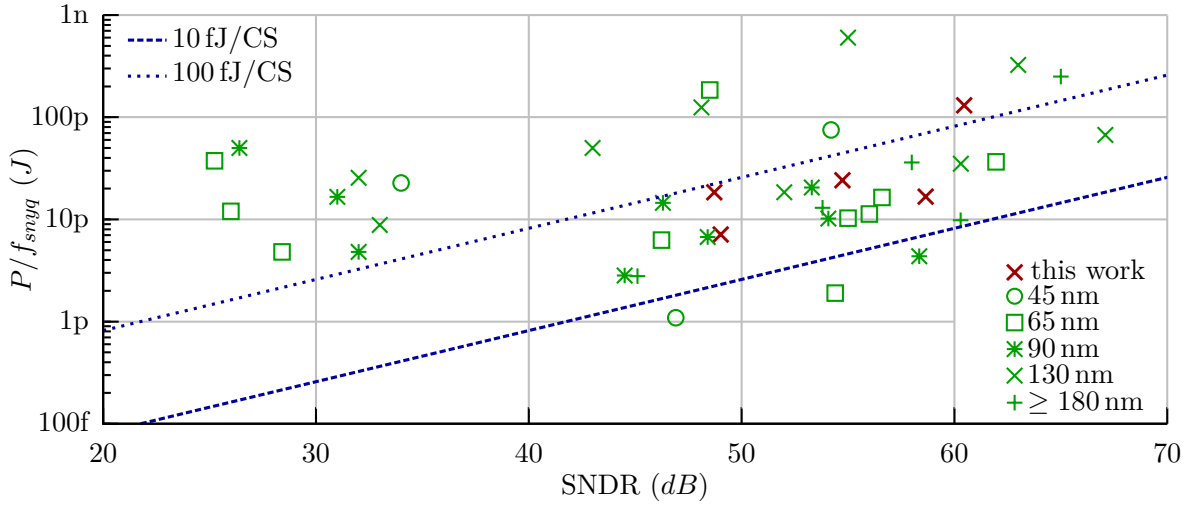


Figure 4.26: Comparison to state of the art with other SAR ADCs

It should be noted that efficiency alone is not sufficient to completely describe the performance of an ADC. One particular problem is the fact that hardly any publication mentions if the reference buffers are included in the power budget. One could also add the power for the input voltage buffer, but often this buffer has a smaller voltage range than the ADC itself which would prohibit full scale performance measurements. Another thing to consider is by which factor the sample rate is lower than the actual needed clock rate, as high clock rates need more power to be generated. It can be stated that often power savings in the ADC core are outweighed by additional power consumption in surrounding blocks, like clock, reference and supply voltage generation. As an example some of the published ADCs use the supply voltage itself as the reference voltage, which obliterates the supply rejection ratio and can only be used in specific applications.

4.2.9 Evolutions

Three different evolutionary steps of the presented architecture were passed through during the time of this work. All three generations were implemented in the same process so that changes in performance could be traced back to architectural changes only. Also, the measurement platform, a Printed Circuit Board (PCB) with a microcontroller, stayed the same during this time.

The first generation already had the concept of the hybrid DAC, but no thermometer coding for the MSBs was included and the trimming option was missing. As Table 4.3 shows the achieved DNL was poor which resulted in a rather low ENOB and thus high FOM.

Generation two added the thermometer coding which significantly improved the DNL from 17.20 LSB down to 0.65 LSB. While the area only increased by a mere 1 %, the FOM could be decreased from 113 fJ/CS to 36.8 fJ/CS in 11 bit mode. The ADC in this version was published at Institute of Electrical and Electronics Engineers (IEEE) International Midwest Symposium on Circuits and Systems 2012. [72]

Table 4.3: ADC performance comparison

Reference	Year and place of first publication	Technology	Principle	Nominal resolution (bit)	SNDR (dB)	ENOB (bit)	Supply voltage (V)	Current consumption (μA)	Clock cycles per sample (1)	Sample rate (kS/s)	Figure of merit (fJ/CS)	peak DNL/INL (LSB/LSB)	Active Area (mm^2)
This work V3 11 bit mode		0.13 μm CMOS 1p6m	SAR SC + R	11	58.7^M	9.45^M	0.90	0.558^M	12	30.0	24.0^M	0.51^M/0.76^M	0.0726
This work V3 8 bit mode		0.13 μm CMOS 1p6m	SAR SC + R	8	49.0^M	7.85^M	0.75	0.095^M	9	10.0	30.9^M	0.08^M/0.12^M	0.0726
This work V2 [72] 11 bit mode	2012 MWSCAS	0.013 μm CMOS 1p6m	SAR SC + R	11	59.0^M	9.51^M	1.02	0.841^M	14	32.0	36.8^M	0.65^M/1.48^M	0.0664
This work V2 [72] 8 bit mode	2012 MWSCAS	0.13 μm CMOS 1p6m	SAR SC + R	8	48.7^M	7.80^M	0.66	0.0115^M	11	1.0	34.1^M	0.29^M/0.42^M	0.0664
This work V1 11 bit mode		0.13 μm CMOS 1p6m	SAR SC + R	11	52.3^M	8.40^M	1.00	0.575^M	14	15.0	113^M	8.90^M/17.20^M	0.0658
This work V1 8 bit mode		0.13 μm CMOS 1p6m	SAR SC + R	8	45.7^M	7.30^M	0.89	0.289^M	11	14.1	116^M		0.0658
[77] C. Liu	2009 VLSI	0.13 μm CMOS 1p8m	SAR SC	10	52.8^M	8.48^M	1.20	76.6^M		50000	52.0^M	1.00^M/2.20^M	0.0750
[78] R. M. Walker	2011 VLSI	0.13 μm CMOS	SAR SC	10	60.3^M	9.72^M	1.20	5416^M		31.25	41.5^M	1.00^M/2.20^M	0.1100
[79] W. Liu	2010 ISSCC	0.13 μm CMOS	SAR SC	12	68.4^M	11.06^M	1.20	2350^M	34	45000	36.3^M		0.0590
[80] J. J. Kang	2009 VLSI	0.13 μm CMOS	SAR SC	12	63.0^M	10.17^M	1.00	3570^M	13	11000	281^M	0.80^M/3.00^M	0.7000
[81, 82] S. Chen	2006 ISSCC	0.13 μm CMOS 1p6m	SAR SC	6	33.0^M	5.19^M	1.20	4417^M		600000	242^M	0.50^M/0.52^M	0.0600
[83] W. Liu	2009 ISSCC	0.13 μm CMOS 1p8m	SAR SC	9	43.0^M	6.85^M	1.20	25000^M		600000	433^M	0.23^M/0.30^M	1.1000
[84, 85] S. Louwsma	2007 VLSI	0.13 μm CMOS	TI SAR SC	12	48.1^M	7.70^M		420000^M		1800000	600^M		1.6000
[86] F. Kuttner	2002 ISSCC	0.13 μm CMOS 1p4m	SAR SC non-binary	10	55.0^M	8.84^M	1.20	10000^M		20000	1306^M		0.0800
[87] S. Chang	2011 VLSI	0.25 μm CMOS 1p5m	SAR SC	8	45.1^M	7.20^M	1.00	0.087^M		31.25	20.1^M	0.50^M/0.75^M	0.0396
[88] S. Lee	2009 VLSI	0.18 μm CMOS	SAR SC	10	53.8^M	8.70^M	0.60	2.167^M		100	31.0^M	0.50^M/0.50^M	0.1250
[74] A. Agnes	2008 ISSCC	0.18 μm CMOS 2p5m	SAR SC	12	58.0^M	9.34^M	1.00	3.600^M	14	100	55.5^M	0.70^M/0.80^M	0.2400
[89] C. Liu	2010 VLSI	0.18 μm CMOS	SAR SC	10	60.3^M	9.83^M	1.00	98.0^M		10000	11.0^M	0.34^M/0.38^M	0.0860
[90] N. Verma	2006 ISSCC	0.18 μm CMOS 5m2p	SAR SC	12	65.0^M	10.50^M	1.00	25.0^M		100	172^M	0.66^M/0.68^M	0.6300
[91] J. Tsai	2011 VLSI	0.09 μm CMOS	SAR SC	8	44.5^M	7.75^M	1.00	113^M		40000	20.6^M	0.88^M/0.88^M	0.0560
[92] J. Craninckx	2007 ISSCC	0.09 μm CMOS	SAR SC	9	46.3^M	7.40^M	1.00	290^M		20000	85.9^M	0.60^M/0.60^M	0.0800
[93] P. Harpe	2010 ISSCC	0.09 μm CMOS	SAR SC	8	48.4^M	7.75^M	1.00	69^M		10240	31.4^M	0.36^M/0.56^M	0.0700
[94] V. Giannini	2008 ISSCC	0.09 μm CMOS 1p9m	SAR SC	9	53.3^M	8.56^M	1.00	820^M		40000	54.3^M	0.7^M/0.65^M	0.0902
[95] Y. Lin	2010 VLSI	0.09 μm CMOS	Flash+SAR SC	9	54.1^M	8.66^M	1.20	1275^M		150000	24.7^M	0.48^M/0.48^M	0.0280
[96] P. Harpe	2012 ISSCC	0.09 μm CMOS	SAR SC	10	58.3^M	9.40^M	1.10	15.9^M		4000	6.5^M	0.28^M/0.42^M	0.0470
[97] H. Wei	2011 ISSCC	0.065 μm CMOS low v_{th}	SAR Resistive	8	46.7^M	7.46^M	1.00	1800^M		250000	42^M	1.00^M/1.00^M	0.0240
[98] M. van Elzakker	2008 ISSCC	0.065 μm CMOS	SAR SC	10	54.4^M	8.74^M	1.00	1.90^M		1000	4.4^M	0.50^M/2.20^M	0.0275
[99] M. Yip	2011 ISSCC	0.065 μm CMOS low leakage	SAR SC	10	55.0^M	8.84^M	1.00	0.26^M		20	22.4^M	0.58^M/0.57^M	0.2120
[100] C. Liu	2010 ISSCC	0.065 μm CMOS 1p6m	SAR SC	10	56.0^M	9.01^M	1.20	942^M		100000	21.9^M	0.58^M/0.69^M	0.0260
[101] M. Yoshioka	2010 ISSCC	0.065 μm CMOS 1p7m	SAR SC	10	56.6^M	9.11^M	1.00	820^M		50000	29.7^M	0.82^M/0.72^M	0.0390
[102] J. Fredenburg	2012 ISSCC	0.065 μm CMOS	SAR SC oversampling	8	62.0^M	10.00^M	1.00	806^M		22000	35.8^M		0.0462
[103] A. Shikata	2011 VLSI	0.040 μm CMOS	SAR SC	9	46.9^M	7.50^M	0.50	2.4^M		1100	6.3^M	0.60^M/0.60^M	0.0112
[104] B. Malki	2012 ISSCC	0.040 μm CMOS low power	SAR SC	10	54.2^M	8.71^M	1.10	5455^M		80000	179^M	0.72^M/0.70^M	0.07963

^{S} simulated
^{M} measured

The third generation changed from dynamic logic to static logic for the successive approximation register, which enabled even lower minimum operating frequencies than before but slightly increased the power consumption. Also, with this design step trimming was introduced, which further improved the DNL down to 0.51 LSB while the area increased by 9 %. Overall the efficiency could again be increased which led to a FOM of 24.0 fJ/CS.

4.3 Conclusion

This chapter presented a general purpose SAR ADC architecture based on the split-capacitor array architecture combined with a resistive ladder. This combination allows the ADC to be operated with two different resolutions and a small and simple layout can be achieved. Due to the hybrid architecture trimming can also be used to improve the problem of scaling mismatch between the two capacitor arrays. A time domain comparator was used for the successive approximation process which additionally allows for offset compensation and configurable noise performance.

The proposed architecture was implemented in three evolutionary steps and measurement results of all three design stages were presented. The achieved performance can compete very well with state-of-the-art designs, especially when designs in much newer and smaller process nodes are neglected. Measured FOM values as low as 24.0 fJ/CS in 11 bit and 30.9 fJ/CS in 8 bit mode were achieved. In ultra-low power configuration current consumptions of below 10 nA at 0.9 V supply voltage and room temperature while doing 300 conversions per second are possible.

A layout plot in Figure A.8 and a micrograph in Figure A.9 show the third test chip used for the measurements. A more detailed layout plot of the ADC core is also shown in Figure A.8.

Chapter 5

Impedance Measurement Circuit

5.1 Introduction

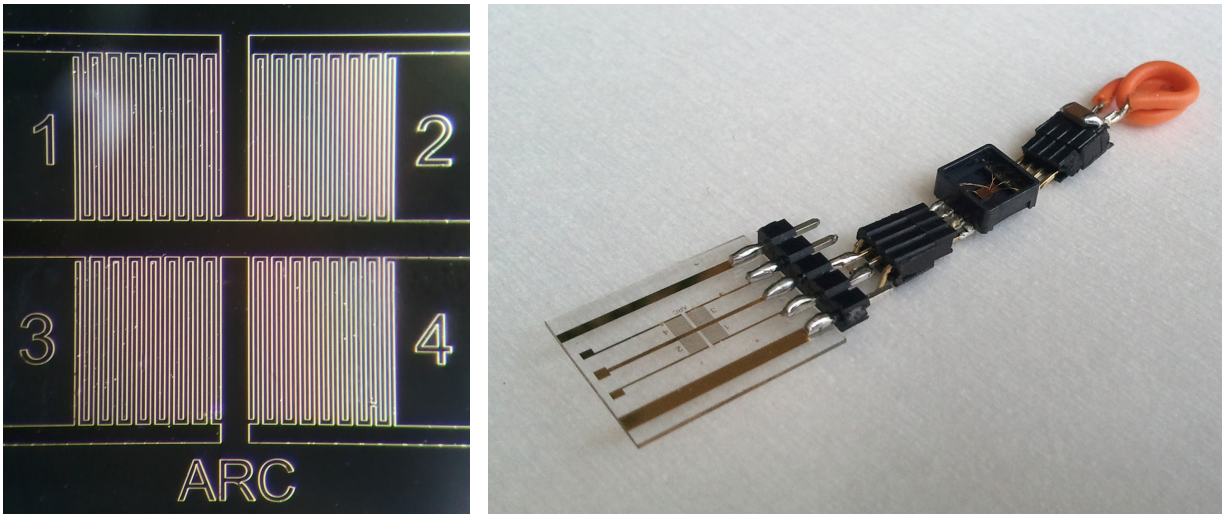
A large number of sensors need their impedance measured. Especially for biomedical topics, the electrochemical impedance makes it possible to measure a wide variety of interesting quantities. The phase relation between current and voltage over frequency often contains valuable measurement information. This kind of measurement is often also referred to as impedance spectroscopy and is mostly used to monitor concentration, proliferation and the physiologic condition of adherent cell cultures. A sensor from the Austrian Institute of Technology GmbH was available during this work and a sub-circuit of the sensor interface which can measure the phase and amplitude relation between voltage and current over a wide frequency span was implemented. This chapter presents the implementation of this circuit, which excites the sensor with a sinusoidal current of digitally adjustable frequency and amplitude. The resulting voltage amplitude and phase shift are measured and represent the impedance of the sensor.

5.1.1 Measurement Principles

Measuring the impedance a of sensor device is one of the most generic and easiest application one can think of as long as sophisticated measurement equipment is available. However, measuring the complex impedance with a CMOS only chip without additional external components is a challenging task, especially when further restrictions regarding voltage supply and current consumption have to be fulfilled.

The main application of the sensor interface is an Interdigitated Electrode Structure (IDES) sensor presented in [105, 106]. A photograph of the sensor on a glass substrate is shown in Figure 5.1a and one of the sensors connected in a discrete manner with the developed sensor grain in Figure 5.1b. The sensor shows a mostly capacitive behavior as the capacitance between the two electrodes is mainly given by the double layer capacity of the cell membranes.

The sensor needs to be excited by a sinusoidal signal to be able to measure the impedance. This can be done by forcing a voltage or current on the sensor, but either way a maximum of 30 mV peak voltage is allowed to be applied to the sensor as otherwise the biological matter would be damaged and the quasi linear region would be left. The frequency of the excitation should be varied over a range of several kHz up to a few MHz. The electrical equivalent circuit of the sensor contains a Warburg diffusion element which makes the behavior over frequency very interesting. Additionally, to measure the impedance of a sensor over a band of frequencies one must measure



(a) IDES close-up

(b) IDES with discrete sensor grain

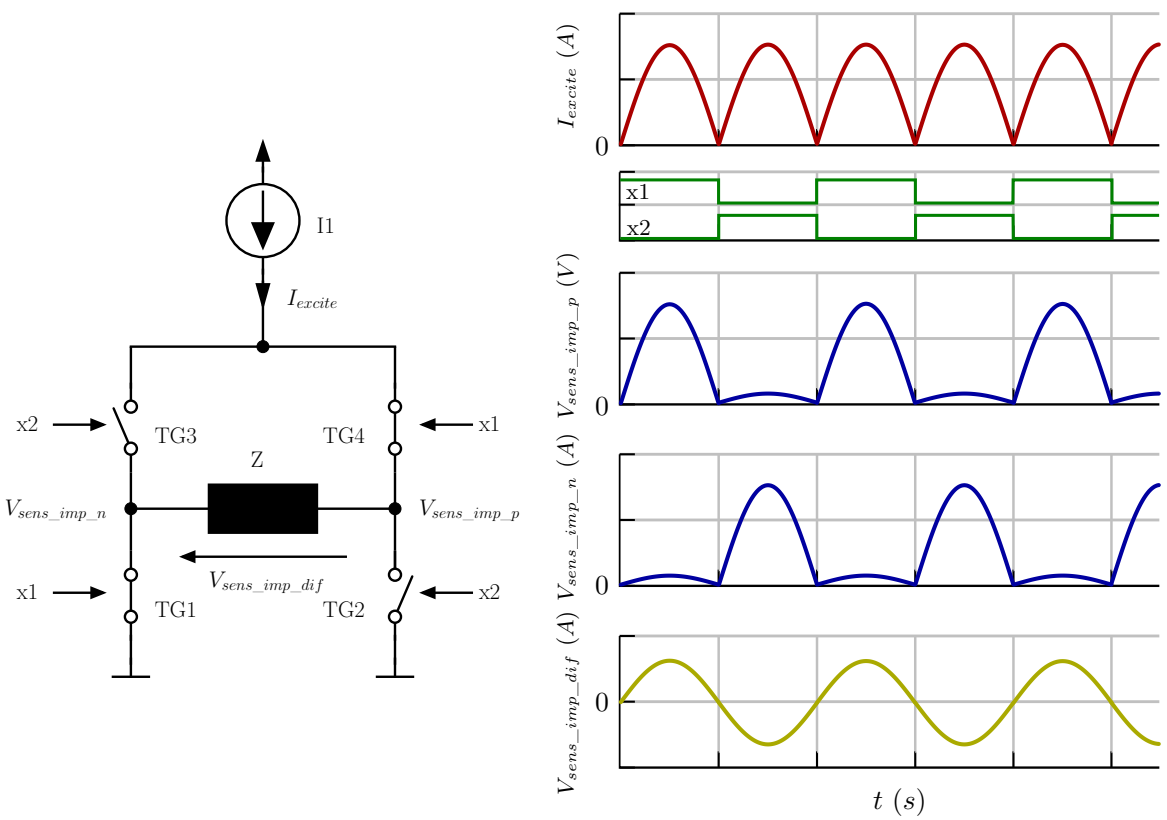
Figure 5.1: Interdigitated Electrode Structure

it at one frequency at a time. So multiple distinct measurements are necessary to collect the complete measurement data set.

Applying voltage steering, an operational amplifier may be used to force a sinusoidal voltage on one node of the sensor while the other node is connected to ground. Since a DC voltage across the sensor is not allowed the operational amplifier would have to be able to force voltages below ground which is not possible for single supply voltages typically found in wireless sensor nodes. To overcome this problem the second node of the sensor has to be put to a virtual ground, which is generated by another operational amplifier. This requires a total of two amplifiers where both have to be capable of driving the full current flowing through the sensor while still maintaining stability for a wide variety of sensor loads.

When voltage steering is applied the current flowing through the sensor has to be measured. When the sinusoidal voltage is generated in a digital way, jumps between the voltage levels are to be expected due to the limited resolution of the digital representation of the amplitude. When a capacitive load is driven, small jumps in the voltage difference result in short but high jumps in the current flow since the amplifiers try to force the new given voltage on the capacitive load by charging it as fast as they can. Since the intended use case for the sensor interface focuses on biological sensors that mostly show resistive to capacitive behavior, this is not a good way to excite such a sensor.

The following sections explain a current excitation scheme and present an actual implementation of a circuit capable of doing exactly this.



(a) Proposed excitation principle

(b) Plot of the voltages on a purely resistive load

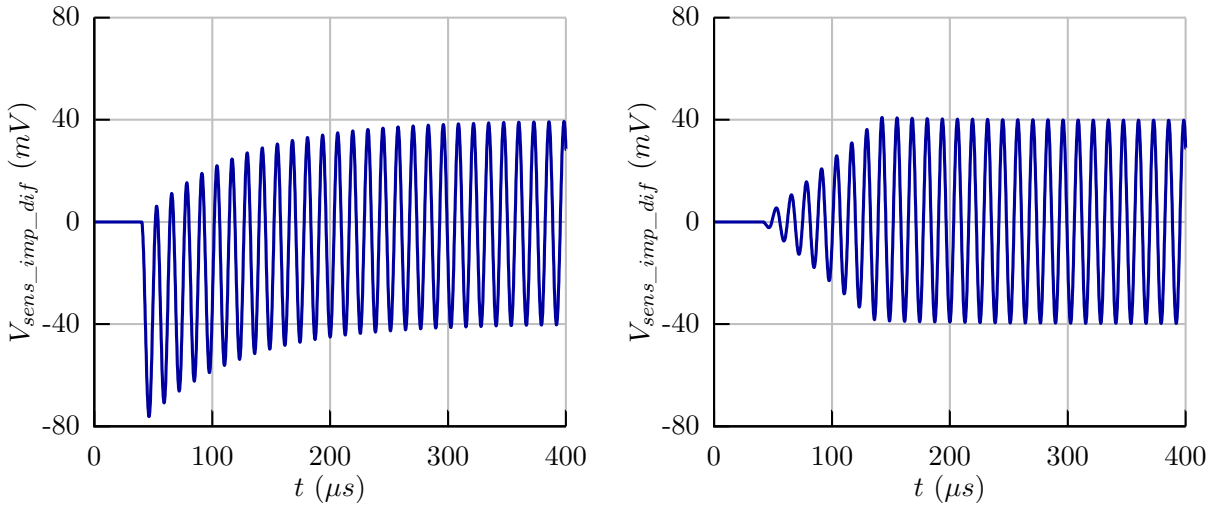
Figure 5.2: Current excitation principle

5.2 Current Excitation Impedance Measurement Circuit

5.2.1 Concept

With current steering one supplies or drains a sinusoidal current to or from one node of the sensor and fixes the other to ground. Since again it is not possible to drain a current at voltages below ground a circuit as shown in Figure 5.2a can be used, which represents an H-bridge circuit. This circuit uses a rectified sinusoidal current via a current source from VDD and applies it in an alternating way to the nodes of the sensor. The opposite node is connected to ground. The result is a sinusoidal current flowing through the sensor and a jumping common mode voltage on the sensor. Nevertheless at wireless sensor nodes there is no fixed ground voltage so the IC's ground potential is also moving with respect to the potential of the sensor. But still the differential voltage across the sensor remains free of jumps and can be measured with amplifiers providing a high common mode rejection ratio.

With current steering, small jumps in the current coming from the digital generation of the current are integrated by a capacitive sensor and a smooth voltage and measurement quantity across the sensor can be achieved. Inductive loads should be avoided with this principle, as small jumps in the current generate high voltage jumps, but anyhow there are hardly any applications for wireless



(a) Abrupt start-up

(b) Linear ramp-up

Figure 5.3: Voltage across a mixed capacitive and resistive load during two startup scenarios

measurements of sensors with inductive behavior.

Figure 5.2b shows the resulting transient behavior of the current steering principle when connected to a purely resistive load. The non-zero resistivity of the turned on switches can also be seen as a small voltage drop across them on node voltages $V_{sens\_imp\_n}$ and $V_{sens\_imp\_p}$. Since the voltage across the sensor is measured the voltage drops have no influence on the result. When a capacitive load is connected to the interface negative voltages also occur at the node voltages $V_{sens\_imp\_n}$ and $V_{sens\_imp\_p}$ due to the phase shift of current to voltage. Since the intended voltage swing on the sensor is below 100 mV this does not pose a problem, as bulk diodes get conductive at around -200 mV.

Since the current excitation principle is clearly the better choice for the given range of applications it was implemented and will be subsequently described in this section.

5.2.2 Start-Up Behavior

When the excitation is started one additional thing has to be considered. For a load with an unknown phase shift between current and voltage it is not good to start the sinusoidal current in the zero crossing point. This is only feasible for purely resistive loads since the phase shift is zero. For capacitive loads in steady state the current is zero when the voltage is at its maximum or minimum. However at the start the expected voltage across the sensor is zero. Figure 5.3 shows the voltage across a mixed capacitive and resistive sensor during two startup scenarios. In the right case the current is linearly increased and no DC offset voltage is generated. The left case, however, shows what happens when the current is not ramped up but switched on abruptly. Only due to the resistor in parallel to the capacitive load, does the mean voltage across the sensor settle back to zero after some time. When this resistor has a large value this process can take a long time, thus delaying a possible exact measurement.

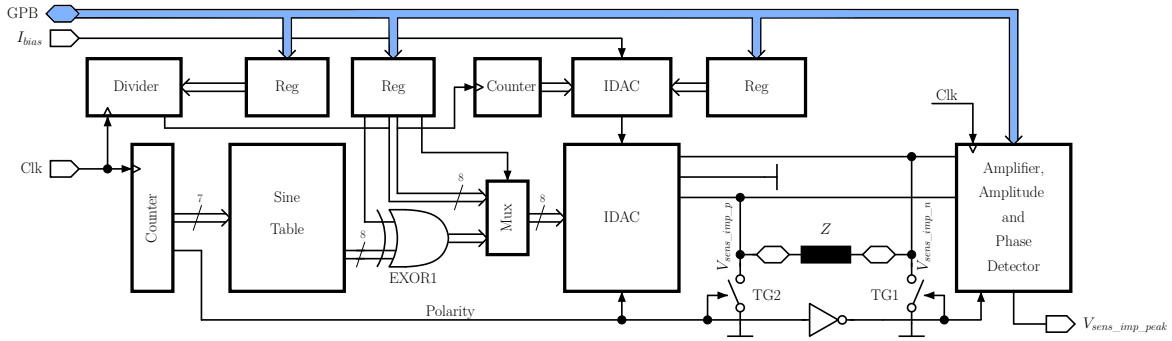


Figure 5.4: Impedance measurement circuit architecture

5.2.3 Implementation

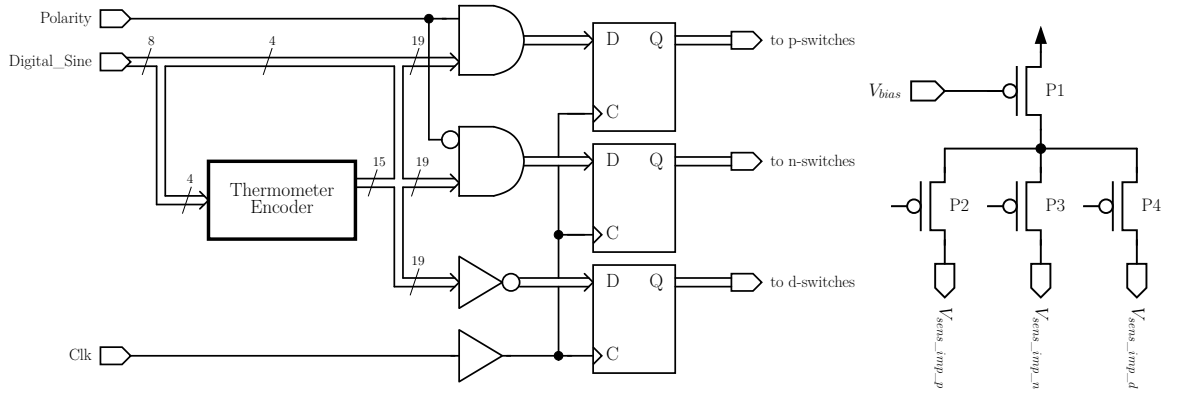
The topology of the proposed circuit is shown in Figure 5.4. As can be seen the Clk input is used to feed an 8 bit counter. The seven lower bits are used to feed a sine lookup table, which converts the digital ramp to a digital representation of a sine wave with 128 steps in time and 256 steps in amplitude. The output of the lookup table is connected to eight exclusive OR-gates which can invert the signal if desired. The purpose of this is shown in Section 5.2.4. The output of the OR-gate is fed to a multiplexer which can be used to select configurable values if wanted. This signal is then fed to the current steering DAC with 8 bit resolution. The eighth bit of the counter is used to steer the switches of the H-bridge as well as to present a reference signal for the phase detector explained in Section 5.2.8. Additionally, the Clk signal is fed to a configurable divider, which steers a second counter and a companion 5 bit resolution current steering DAC. This DAC is biased by the bandgap reference in the sensor interface and steers the main DAC. Together the aforementioned ramp-up of the excitation current is implemented in a configurable way. Additionally the companion DAC can scale the overall current level so that the output current can be configured.

The main DAC in interaction with the sensor is described in Section 5.2.4. The resulting voltages on the two sensor nodes are fed to the detector block which is discussed in Sections 5.2.5, 5.2.6, 5.2.7 and 5.2.8.

5.2.4 Current Steering Digital to Analog Converter

The value read from the lookup table is fed to this 8 bit resolution current steering DAC with three outputs. Figure 5.5 shows the used p-channel current sources with the three output switches and the digital steering of the switches. Two of the current outputs steer the sensor while the third output carries the difference to the maximum output current and is usually dumped to ground. Thus no charge is accumulated on the current sources in the DAC which otherwise would lead to unwanted charging processes during the switching of the DAC. Additionally the third output results in a constant overall current consumption of the DAC, relaxing the requirements for an upstream supply voltage regulator. The drawback is an increased average current consumption over time of $1 \cdot I_{max}$ instead of $2/\pi \cdot I_{max} \approx 0.6366 \cdot I_{max}$.

An additional switch is implemented that makes it possible to break this dummy current according to a configuration bit which can be useful for low frequency excitations where the supply regulator



(a) Digital steering of current sources

(b) Current sources with switches

Figure 5.5: Current steering digital to analog converter

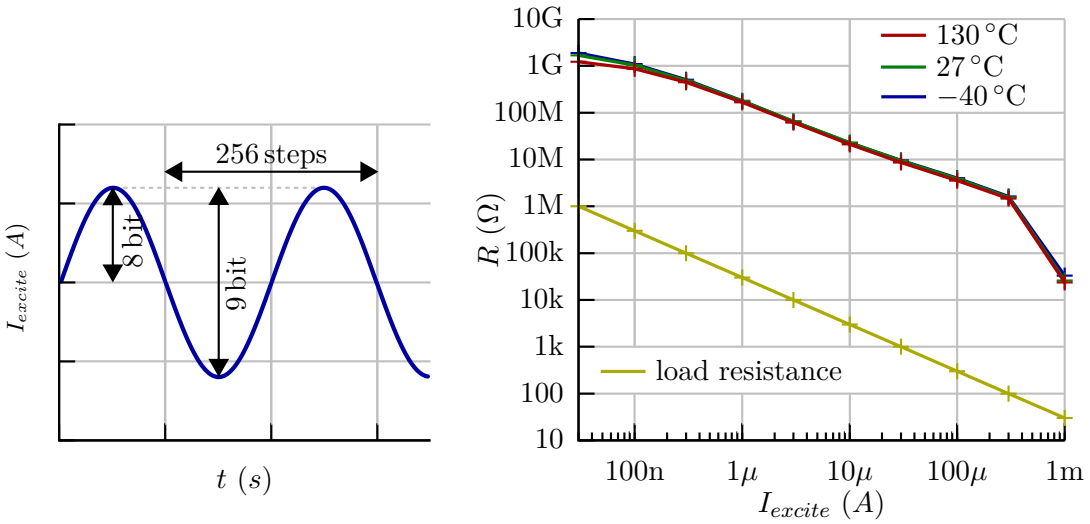
can handle the load current up- and downturns and the induced charges only have a diminutive influence.

The 8 bit digital signal steering the DAC is partially converted to thermometer code which helps to improve the linearity of the output current. Two AND-gates separate the signal according to the signal level of the polarity signal. Since different delay times of the signals are to be expected an additional flip-flop clocked by the global clock signal for every switch or group of switches was added to avoid glitches. To avoid coupling of supply noise to the sensor the current sources and digital logic are supplied by separated supply voltages.

Figure 5.6a depicts the resulting excitation current on the sensor. Due to the fact that 8 bit of resolution is available for the upper half wave as well as for the lower half wave a total amplitude resolution of 9 bit is achieved. Every full period consists of 256 steps, which means that the clock frequency of the lookup table has to be 256 times higher than the resulting excitation frequency, which easily leads to frequencies in the several 100 MHz range. To extend the possible excitation frequency range it is, however possible to change the step width of the counter feeding the lookup table, resulting in fewer steps per full wave. According to the configuration 256, 128, 64 or 32 steps are possible.

Figure 5.6b shows the simulated output resistance of one DAC output at three different temperatures over peak current. Also the estimated expected load resistance which is necessary to get a 30 mV signal at the load was added to the plot. It can be seen that the output resistance of the DAC is at least 1000 times higher than the resistance of the load, except for the highest and lowest current limits. The high values are achieved due to the fact that the switches made of p-channel transistors, when switched on, act as cascodes to the current sources. At very low currents leakage and at very high currents the operating region of the current sources deteriorate the output resistance. Nevertheless the ratio between the resistances should be high enough to achieve quite good measurements in any case.

Figure 5.7 depicts the current excitation and the dummy current path in more detail. It can be seen that the dummy current I_d can be dumped to ground via various resistors. The voltage across these resistors can be used to feed the measurement blocks if desired. This can be used



(a) Current signal on sensor

(b) Output and load resistance of the IDAC

Figure 5.6: Properties of the sine signal and the output resistance of the IDAC

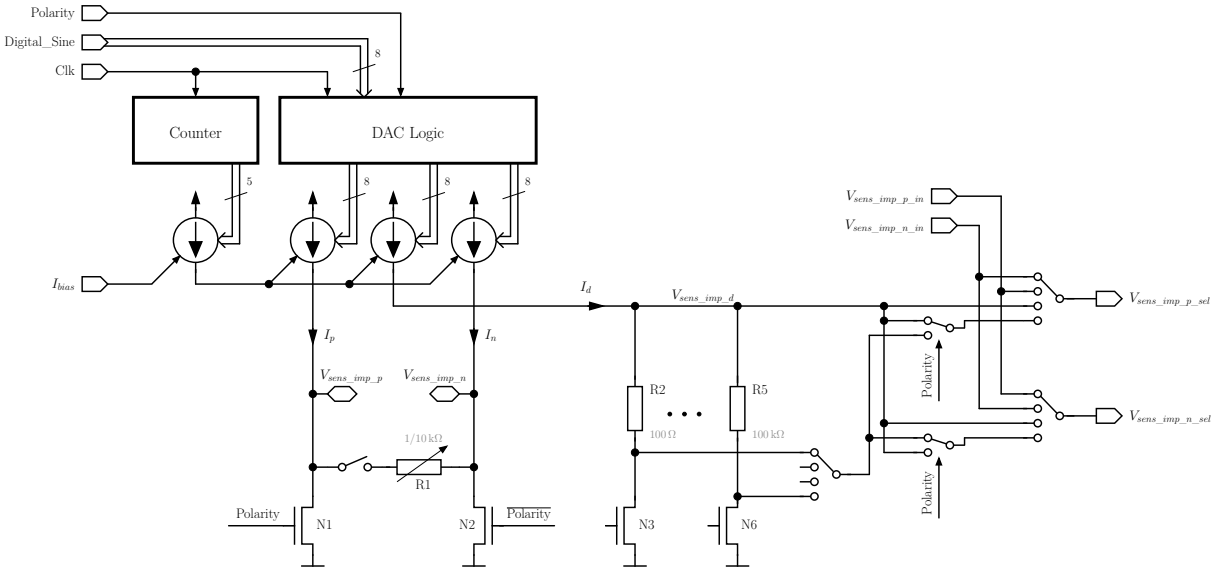
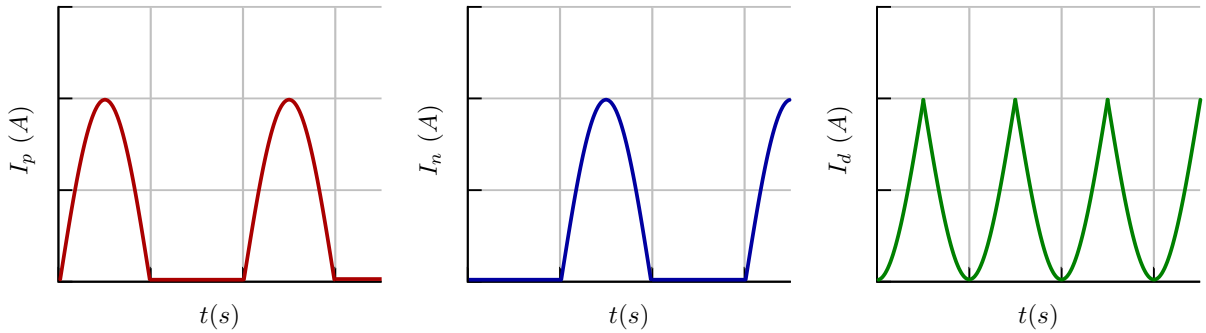


Figure 5.7: Detailed circuit of excitation scheme



(a) Positive output (b) Negative output (c) Dummy output

Figure 5.8: Current outputs of IDAC

to calibrate the measurement block to the internal resistors. Figure 5.8a shows the currents at the three current outputs of the DAC during normal operation. I_d does show an inverted and rectified sine behavior in this case. To achieve a non-inverted excitation of the dummy resistors, the aforementioned exclusive OR-gate can be used. This way, a rectified sine wave shaped voltage is to be expected on $V_{sens\_imp\_d}$. Two additional switches driven by the polarity signal convert the rectified signal into a non-rectified sine signal.

During normal sensor measurement the differential input of the measurement block is connected to the two sensor pins in a 4-wire sensing configuration. This avoids measuring voltage drops on the current carrying wires from the DAC to the sensor. In parallel to the sensor an on-chip resistor can be connected to make reference measurements or to accelerate the reduction of DC offsets on the sensor if desired.

5.2.5 Level Shifter

As can be seen in Figure 5.9 the detector block consists of a level shifting stage, an amplification stage and two detector circuits.

Since the voltages at the sensor are close to ground level they have to be shifted to a higher voltage to be further processed. As it is shown in Figure 5.9 this is done by a capacitive level shifter composed of C_1 and C_2. At start-up OTA1 sets the output voltages $V_{imp\_det\_p\_shift}$ and $V_{imp\_det\_n\_shift}$ equal to a 600 mV reference. C_3 keeps the whole loop stable during this operation. Additionally, C_1 and C_2 can be partly connected to ground so that an input attenuation can be achieved for large input signals to avoid clipping of the downstream blocks. Attenuation factors of 1, 2, 3 and 4 are selectable.

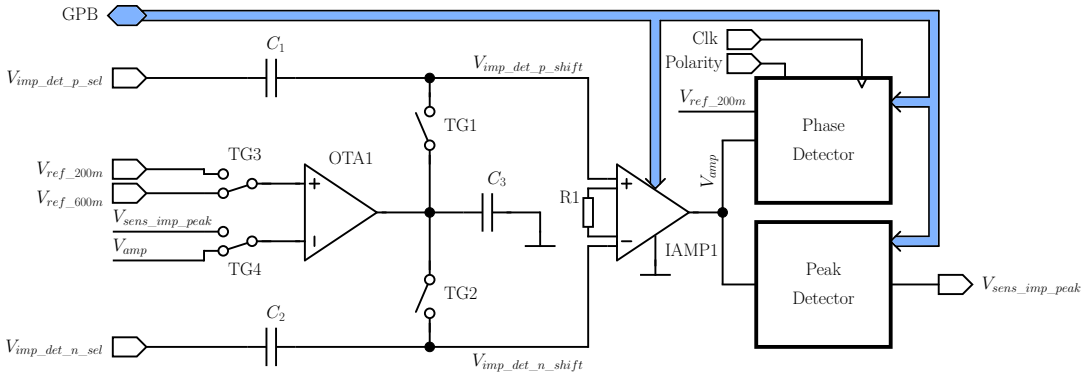


Figure 5.9: Detector architecture

5.2.6 Instrumentation Amplifier

After the sensor voltages are shifted their difference is amplified by an instrumentation amplifier with a fixed amplification factor of 27. In a calibration step before each measurement the output voltage V_{amp} of either the amplifier or $V_{sens\_imp\_peak}$ of the peak detector is set to 200 mV by slightly changing the voltage of just one of the shifted sensor voltages. This way, the offset voltages of the instrumentation amplifier and the peak detector can be calibrated out and only the offset voltage of OTA1 in the voltage level shifter remains. This means that after calibration at zero voltage across the sensor, the output voltage of the peak detector is 200 mV. It is also possible to take another sample with the ADC of the output voltage at the calibration step. When subtracted later from the measurement result itself even the remaining offset gets canceled out. At large enough signals on the sensor the amplifier would have to output voltages below ground level but is not able to, thus goes into saturation. It was designed in a way that the time to get out of saturation is short enough so that above the 200 mV level no influence can be seen anymore at all interesting signal frequencies.

A fixed gain amplifier with adjustable input attenuation instead of a variable gain amplifier was chosen because only in this way could a fixed overall amplification factor over temperature be guaranteed. The instrumentation amplifier is composed of three operational 2-stage miller amplifiers [107]. Their bias current, compensation capacitor and cascodes can be configured to achieve a flexible and power efficient operation for all frequencies.

5.2.7 Amplitude Detector

The amplitude detector is implemented as a peak detector, as can be seen in Figure 5.10. The amplified single ended voltage V_{amp} is compared to the voltage $V_{sens\_imp\_peak\_store}$ which is stored on capacitor C_1. When V_{amp} is higher than $V_{sens\_imp\_peak\_store}$, C_1 is charged via transistor N1 up to the peak level of V_{amp}. A current mirror consisting of P1 and P2 limits the maximum rate at which C_1 is charged, increasing the accuracy and stability of the circuit. The comparing OTA has a configurable bias current, thus can be adapted to the signal frequency.

The voltage $V_{sens\_imp\_peak\_store}$ is very sensitive to leakage currents, thus it is buffered by another OTA with thick oxide transistors at its inputs to avoid leakage into the buffer. To reset the peak detector C_1 can be discharged via TG1. TG1 itself consists of three transmission gates

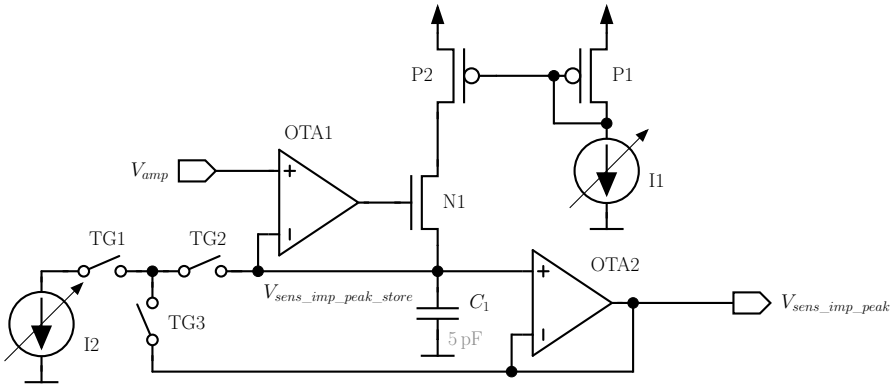
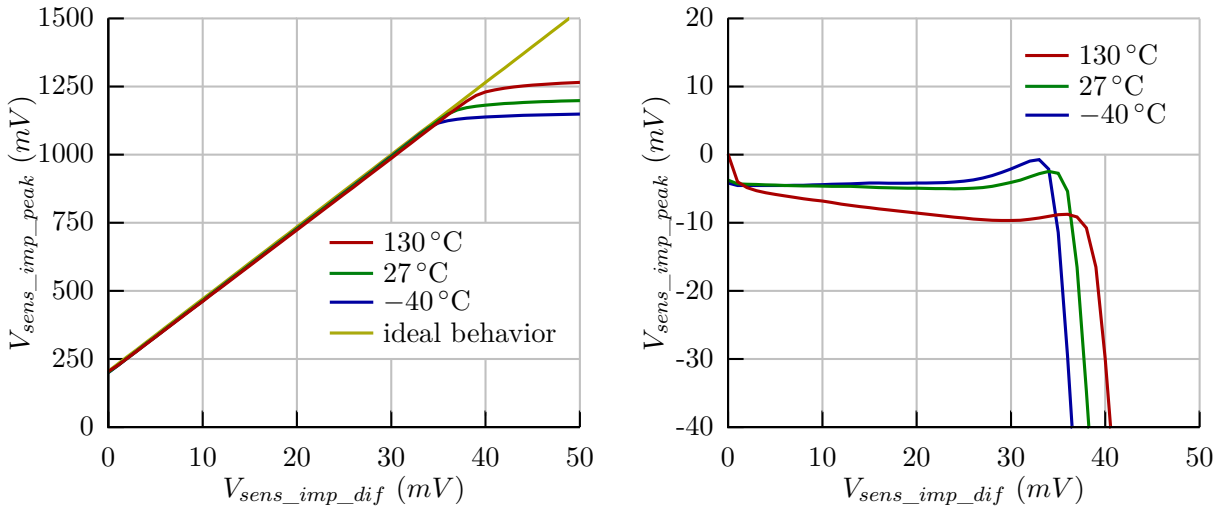


Figure 5.10: Peak detector circuit



(a) Absolute voltages

(b) Relative voltages to ideal behavior

Figure 5.11: Simulated output voltage of peak detector at three temperatures

that enable very low leakage currents to be drawn from C_1 when TG1 should be non-conductive. This is achieved by connecting the buffered peak voltage $V_{sens\_imp\_peak}$ to one side of one of the transmission gates and the other to $V_{sens\_imp\_peak\_store}$. This results in this transmission gate only seeing the offset voltage of the buffer as voltage difference at both of its connections, giving a very low current through it. The discharge speed by I2 can be varied over a large range and cannot only be used to completely reset the capacitor after a measurement but also during measurement, to avoid storing rare pulses on V_{amp} introduced by noise for extended periods of time on the output voltage. The capacitor size of C_1 was chosen to be 5 pF which gives a kT/C noise of 29 μV which is more than sufficient for the accuracy of the ADC which samples this voltage. Nevertheless, this capacitor size is still very small in the layout. Even larger capacitors would further improve the leakage influence at low frequencies.

The simulated output voltage $V_{sens\_imp\_peak}$ of the whole detector circuit including the amplitude detector over the sensor voltage for three different temperatures while supplied with a 1.5 V supply

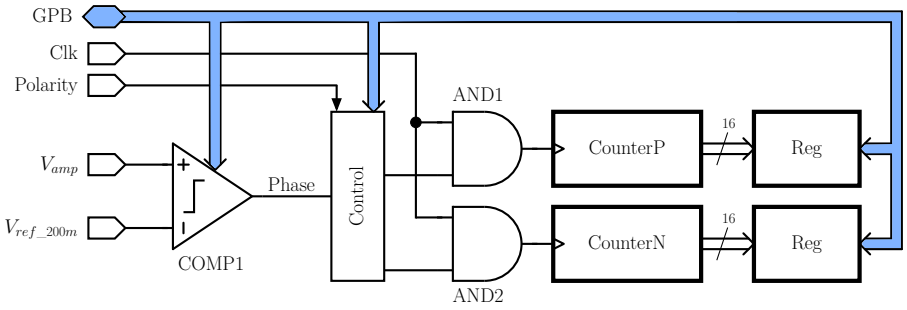


Figure 5.12: Phase detector architecture

using no attenuation is shown in Figure 5.11. It can be seen that as already mentioned the output voltage starts at 200 mV for a sensor voltage amplitude of zero volt and increases with a slope of 27 mV per mV at the sensor. The maximum output voltage varies with temperature due to the threshold dependency of transistor N1. Nevertheless, a sufficiently constant gain over temperature and a good linearity are achieved.

The output voltage $V_{sens\_imp\_peak}$ has to be fed to an ADC in the system to get a digital representation of the amplitude on the sensor. All circuits in the impedance measurement block except the amplitude detector are designed to work with a nominal supply voltage of 1.2 V and operate with separated supply lines to limit digital noise coupling into sensitive analog blocks. To fit the usable signal swing of the amplitude detector to the input voltage range of the intended ADC, it was decided to operate the amplitude detector at a higher operating voltage of 1.5 V, as the input voltage of the ADC ranges from ground to 1.2 V. This higher supply can be configured in the power management unit of the sensor interface. To avoid problems with the digital signals from the GPB and its registers additional level shifters were added.

5.2.8 Phase Detector

As depicted in Figure 5.12 the phase detector uses the zero crossings of the voltage on the sensor, which after the amplifier means V_{amp} crossing the 200 mV level. Two counters count the pulses of the sine generator between the zero current point and the zero voltage point. As this is done for the positive half-wave and the negative half-wave a DC offset cancels out as long as the amplitude of V_{amp} is big enough to exceed the offset voltage. The offset voltage most likely is not present on the sensor itself but is introduced by the mismatch of the transistors in the comparator. The resulting number of pulses counted can be read separately for the positive and negative half-wave. Thus the two values include information of the phase shift as well as the offset voltage. By adding the two values, the phase shift is gained.

Since the clock of the sine generator is used for counting, a maximum resolution of $360°/256 \approx 1.41°$ can be achieved. The control block also allows for multiple sine waves to be counted so that an average value can be determined.

The delay time of the comparator adds to the phase shift and must be accounted for in the post-processing. To get a feel for how big the delay time is, a calibration measurement with a

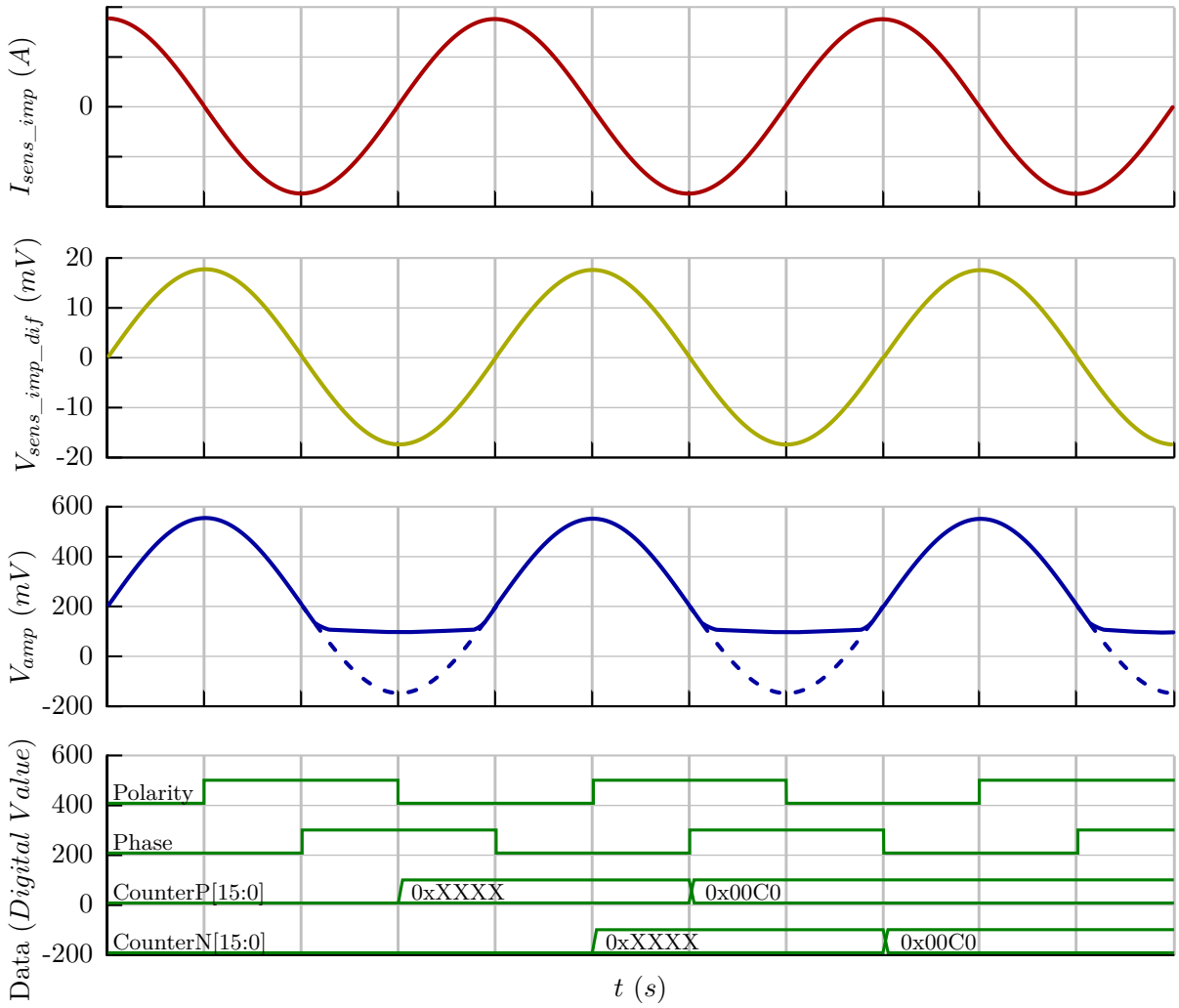


Figure 5.13: Working principle of phase detector

purely resistive load is advised. Since the variation of this time between multiple chips should be rather small compared to the overall time, a fixed trim value should be sufficient for most applications. Nevertheless, the bias current of the comparator is digitally controllable and thus the delay time is adjustable to the frequency and accuracy requirements. The aforementioned internal dummy resistor can also be used to measure this phase offset.

Figure 5.13 depicts the transient behavior of the phase detector. The current through the sensor as well as the voltage across the sensor are plotted. A phase shift of 90 ° between voltage and current can be seen as is to be expected for a purely capacitive load. V_{amp} which is the voltage after level shifting and amplification follows the voltage on the sensor but saturates at voltages above a certain value due to the limited output range of the amplifier. This does not compromise the crossings at 200 mV which the detector looks for. The polarity signal changes its state exactly at the zero crossing of the current. Its high-low transition starts CounterP for the positive current half-wave and its low-high transition starts CounterN for the negative current half-wave. The

counters are stopped whenever the phase signal from the comparator makes the opposite level change transition. This way phase shifts of almost $-180\,^\circ$ to $180\,^\circ$ can be measured, although including inductive and capacitive loads, only $-90\,^\circ$ to $90\,^\circ$ are to be expected.

5.2.9 Measurement Results

Figure 5.14 shows the transient measurement of a simple but complete impedance measurement cycle of the full sensor interface. To make it possible to observe the behavior of the sensor interface the dedicated test chip for the sensor interface was used. Its layout and die shot can be seen in Figure A.11 and Figure A.12. To emulate the limited energy available in a WSN the sensor interface is supplied by a 2.2 pF capacitor precharged to 3.3 V. As can be seen in the plot, at approximately 2 ms the sensor interface is activated by the measurement equipment and the blocks are configured and turned on one after another. For this scenario the microcontroller within the sensor interface was not used as the measurement equipment is able to time the configurations by itself. About 1.5 ms pass by until the start-up of the sine excitation can begin. During this time the current consumption of the circuit is rather low, which can be seen at the only slightly decreasing voltage on the supply voltage VDD_Cap. The ramp-up of the excitation starts at approximately 6 ms, and thus the sinusoidal voltage at the sensor steadily increases until at 8 ms the sensor is fully excited. During this time also the level shifter is activated and as a first step its output voltage is set to 600 mV. Subsequently the positive output voltage of the level shifter is increased a bit more to get an output voltage of 200 mV at the peak detector. Next, the voltage on the sensor is connected to the input of the level shifter, which causes its output voltages to follow the input voltages with the voltage shift in-between. The voltage difference of the two voltages is amplified by the instrumentation amplifier and subsequently its peak value is detected. After some settling time the ADC can take one or multiple samples of the peak voltage $V_{sens\_imp\_peak}$. During the peak measurement the phase measurement is also executed. After the measurement is complete the supply is disconnected which causes some spikes at the analog voltages during fading out. In this example the remaining voltage on the storage capacitor amounts to 2.3 V which would be enough to sustain data storage in the SRAM for several milliseconds more.

Figure 5.15 shows transient measurements of the single ended and differential voltages on different loads. All measurements were configured to take place at 25 kHz and a rather large amplitude of 200 mV peak. The large amplitude can be chosen in this case as no biological cells are present that would be harmed by such high voltages, and additionally, the high voltage levels lower the noise contribution of the measurement equipment.

Figure 5.15a shows the behavior for a purely resistive load. It can be seen that voltage and current are in phase. During the transitions of the polarity signal the induced current is zero and also both nodes of the sensor are at close to zero volt. Also a small voltage drop across the switches in the H-bridge can be seen during the time when current is induced.

Figure 5.15b changes to a purely capacitive load. It now can be seen that the differential voltage is at its maximum during the transition of the polarity signal. The single ended voltages at the sensor jump during this transition but do not affect the differential voltage as long as no parasitic capacitances to other nodes are present. The measurement equipment, two single ended oscilloscope probes in this case, poses only a rather small parasitic load, thus no distortions can be

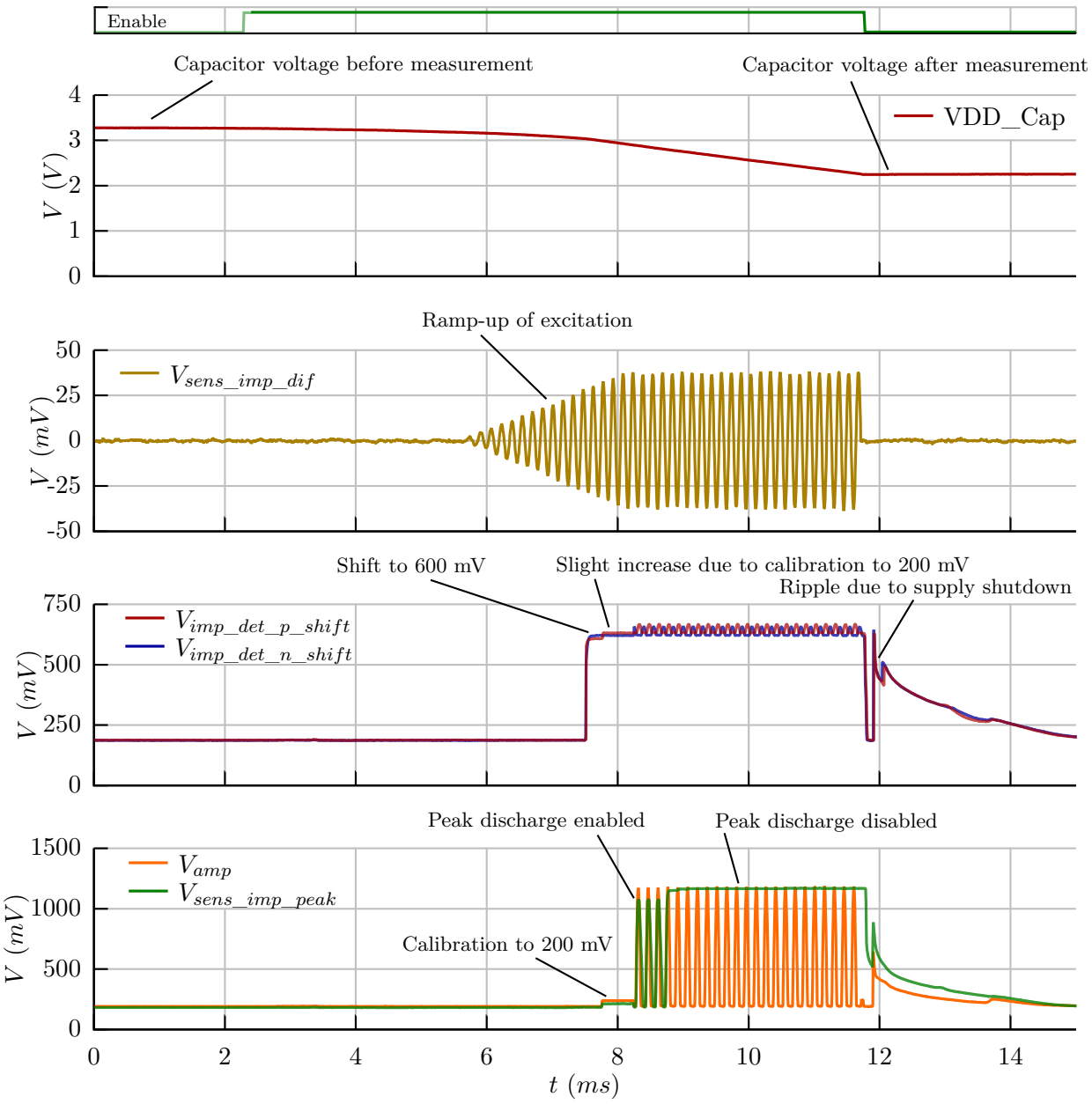
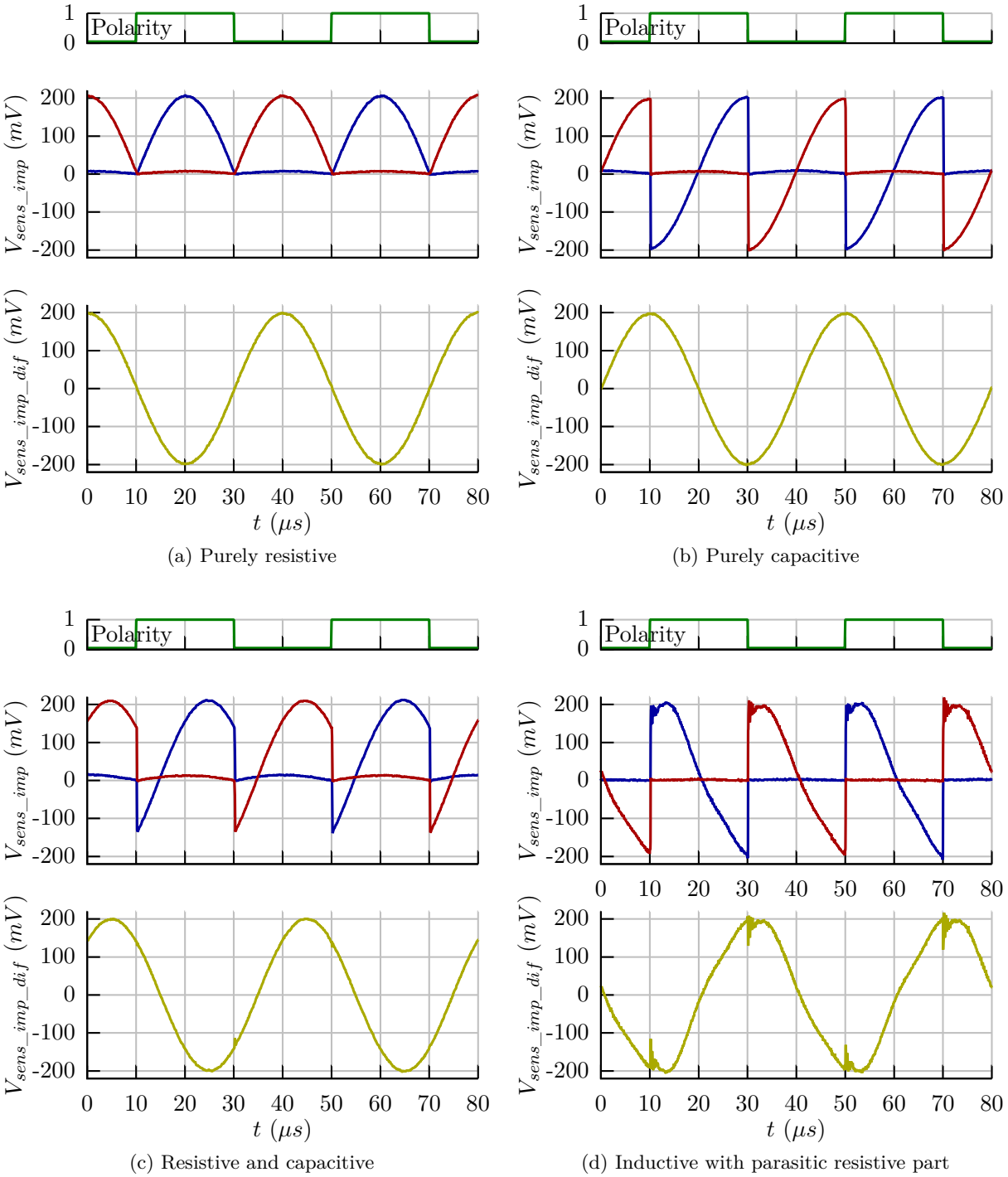


Figure 5.14: Measured transient operation of the impedance sensor interface



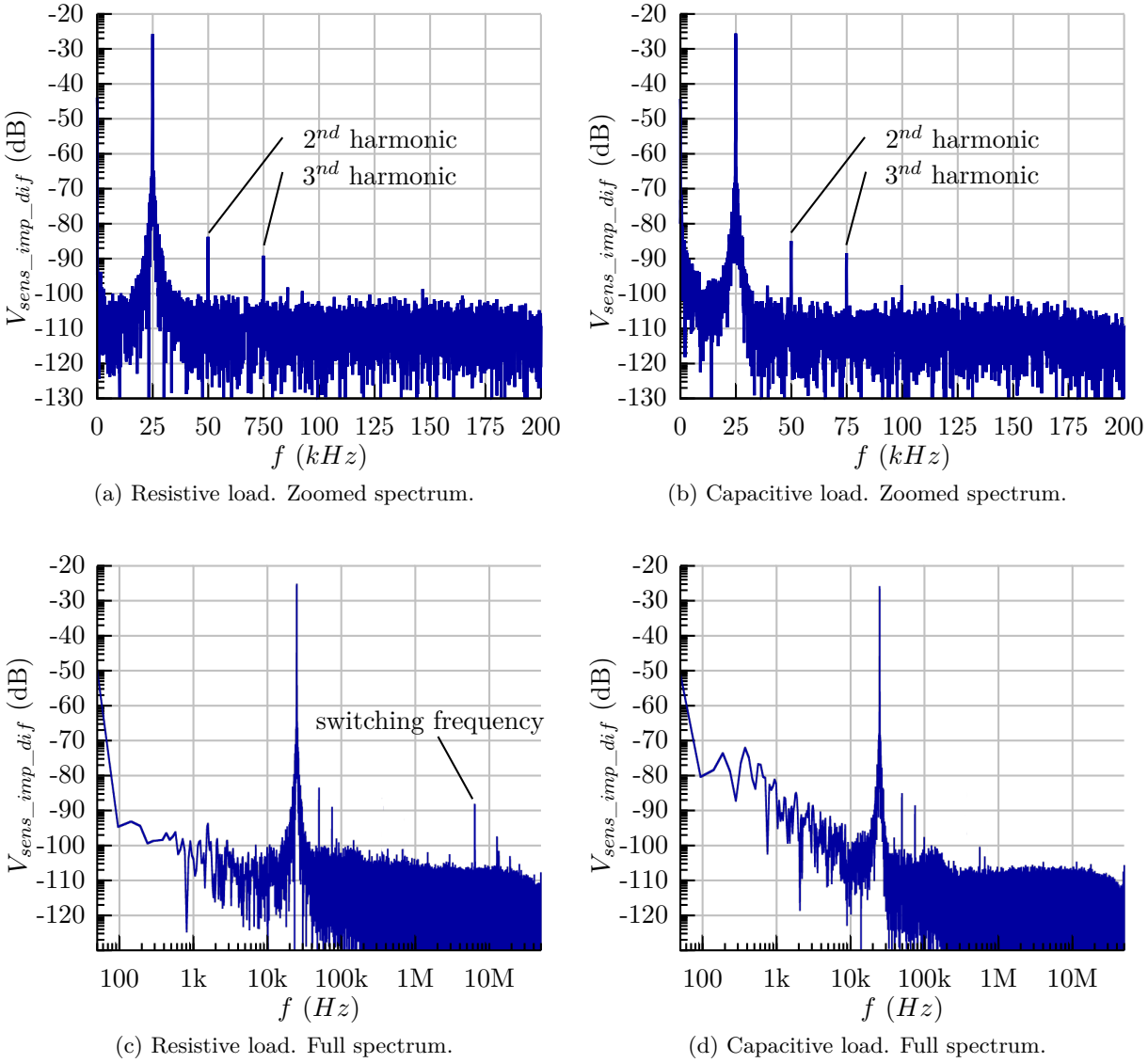
(a) Purely resistive

(b) Purely capacitive

(c) Resistive and capacitive

(d) Inductive with parasitic resistive part

Figure 5.15: Measured voltages on various loads



(a) Resistive load. Zoomed spectrum.

(b) Capacitive load. Zoomed spectrum.

(c) Resistive load. Full spectrum.

(d) Capacitive load. Full spectrum.

Figure 5.16: Measured spectrum of voltage on different loads at 100 mV peak voltage and 25 kHz sine frequency

seen in this plot.

Figure 5.15c is a measurement of a resistor in series with a capacitor. As a result this has the effect that the phase shift between voltage and current is somewhere in between 0 to 90°. Still, a nice sine-shaped voltage is achieved across the load.

Figure 5.15d concludes the measurement with an inductive load. Due to the fact that the parasitic series resistance of the inductor used was not zero a not quite −90° phase shift was measured. As can be seen during the transition of the polarity signal, some ringing occurs. This is caused by the resonant circuit that is formed by the inductor, its own parasitic capacitance and the parasitic capacitances of the sensor interface circuit and the measurement equipment. As already envisioned during the concept phase of the impedance measurement circuit, inductive loads suit this kind of excitation scheme the least.

For purely resistive and capacitive loads the voltage across the sensor was investigated in more detail. Figure 5.16 depicts the measured spectral density for these two loads. A signal amplitude of 100 mV peak and a frequency of 25 kHz were chosen for this measurement. The signal across the sensor was sampled with a digital oscilloscope at 200 MS/s and 5 million samples were taken and fed to a Fast Fourier Transformation (FFT) algorithm with a hanning window. It can be seen that with the implemented excitation scheme a Spurious-Free Dynamic Range (SFDR) of close to 60 dBc is achieved. It has to be noted that the results should be better in reality, but the measurement equipment and discrete measurement setup introduce parasitic capacitances which deteriorate the performance. Nevertheless, it can be seen that the main frequency component, the excitation frequency, is not placed in a single frequency bin. This means the frequency of the excitation is not stable enough. Other oscillators with better noise performance would improve this, but probably at the cost of frequency range or power consumption.

The switching frequency, which is 256 times higher than the excitation frequency, can only be seen with the resistive load as the capacitive load smoothes these high frequency components. The noise level at low frequencies is higher in the case of a capacitive load, which is because noise can accumulate at the capacitor during multiple wave periods.

5.3 Conclusion

A fully integrated impedance measurement circuit for wirelessly powered ICs was shown. The circuit was designed and simulated in an Infineon 130 nm CMOS process and no off-chip components are required.

The complex impedance of a sensor can be measured in a wide frequency band from near DC up to the low MHz range. The induced current on the sensor can be set from just microamperes up to one milliampere and the measurable voltage swing on the sensor can be up to 200 mV peak. The circuit operates at low supply voltages of 1.2 V with the exception of one block, the peak detector, at 1.5 V. It was shown that the proposed measurement principle with induced currents works well for capacitive and resistive loads which are expected for biomedical applications. The scheme used manages to avoid stability problems found with conventional voltage excitation schemes.

Chapter 6

Conclusion and Research Summary

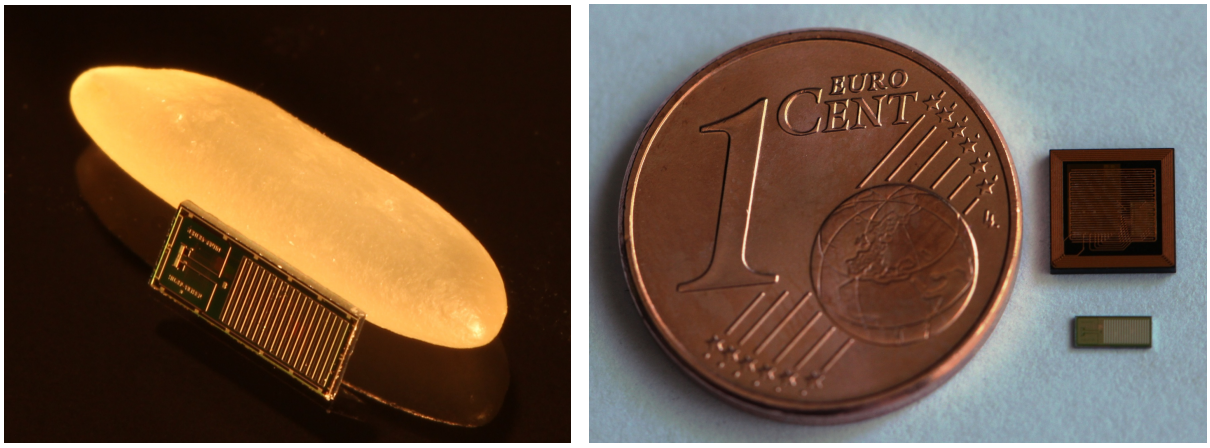
In this thesis the topic of *Design of a Generic Low Voltage, Ultra-Low Power Sensor Interface for Wirelessly Powered ICs* was discussed. Five chapters discussed a wireless sensor node, two vital generic analog building blocks and a specialized measurement front-end.

6.1 Chapter 1 - Introduction

To get started with wireless sensor nodes this chapter gave a short overview of the topic and showed multiple proposals for wireless sensor nodes. Various implementations using the eWLB packaging technology were discussed. Figure 6.1b shows such an implementation, which is functional and only 6x6x1 mm small. The smallest implemented sensor node consists only of a single die of silicon, as compared in Figure 6.1a to a corn of rice. For this also functional realization no external components are required and a total volume of just $1\,\mathrm{mm}^3$ was achieved.

6.2 Chapter 2 - Generic Sensor Interface Concept

As the title of this thesis suggests this chapter introduced the generic sensor interface which is included in all WSNs proposed in Chapter 1. The heart of the sensor interface is a bus system which enables its components to communicate with each other. The controlling entity taking actions on the bus can either be the built in microcontroller or an external control entity which steers the digital interface connections of the sensor interface. These two options ensure that programmed measurement sequences can be executed with or without activated external system components. This enables the WSN to completely shut down all of its components but the sensor interface and still be able to do measurements. This is useful during times when no communication to external reader devices is available, like it is done for measurements where communication disturbs the sensitive measurement. The sensor interface itself includes a power management unit, which can work off supply voltages from 2 to 4 V and thus can work off a single capacitor used as an energy storage device. It supplies a total of 12 configurable supply voltages to various blocks within the sensor interface. To keep the whole interface flexible and extendable generic functions like supply generation, analog to digital conversion, bias signals in voltage and current, clock frequencies and digital configuration signals are provided. They can be used by front-ends that are specialized on one specific type of sensor device. Two of those front-ends were implemented during this thesis, one for voltammetry analysis and another for impedance spectroscopy. Further front-ends should be added or existing ones replaced by master students in the future to adapt to upcoming sensor devices and new applications.



(a) Silicon only wireless sensor node in comparison to a grain of rice

(b) eWLB packaged wireless sensor node and silicon only wireless sensor node in comparison to a coin

Figure 6.1: Two proposed implementations of wireless sensor nodes

6.3 Chapter 3 - Switched Capacitor Bandgap

Almost all analog and digital circuits rely in a way on some sort of reference voltage, either as a stabilized supply voltage, a reference voltage for analog to digital conversion or as bias voltage for various analog circuits. With the appearance of new process nodes with ever smaller physical dimensions, and consequently decreasing supply voltages, the use of classic bandgap references becomes impossible. Fractional bandgap references are available but at the cost of current consumption, area and accuracy. An improved architecture for an alternative fractional bandgap reference using switched capacitors was introduced in this chapter and three implementations specialized for different use cases were presented. The lowest power version allows operation at supply voltages down to 750 mV with a current consumption of about 25 nA including an oscillator at room temperature. This ultra-low power consumption comes with significantly better accuracy compared to non-bandgap-based architectures and maintains a reasonable die area. A measured temperature coefficient of 18 ppm/°C over a temperature range from −50 to 130 °C is achieved. The circuit consumes only 0.0336 mm^2 of die area in the 130 nm CMOS process used, with no high resistive poly resistor option, and an one sigma untrimmed accuracy of 1.36 %, which is significantly better than for other non bandgap based circuits, was reached. An extensive comparison to state of the art work is able to show the currently unmatched combination of low voltage compatibility with ultra-low current consumption at low area and good accuracy. A proposed figure of merit for reference circuits, which aggregates the mentioned specifications, is also able to show the outstanding performance combination when compared to other circuits and publications. The improved switched capacitor bandgap architecture appeals to many existing products within Infineon and is planned for multiple future products at the moment.

6.4 Chapter 4 - Successive Approximation Analog to Digital Converter

Analog to digital converters are omnipresent in systems connecting the analog to the digital world, which is the case for a vast amount of circuits nowadays. Also, the wireless sensor node presented in this thesis relies on more than one converter to be able to deliver digital measurement results. To fulfill the ultra-low energy consumption restriction given by the sensor node a new hybrid nyquist rate converter architecture, which combines a split capacitor array with a resistive ladder, is presented. A time domain comparator with adjustable noise level, trimming, a class-AB amplifier and various digital concepts allow for maximizing the energy efficiency of the design. 8 and 11 bit operation is possible over a wide range of conversion rates. Energy consumptions per conversion step down to 24 fJ/CS without and 54 fJ/CS with reference buffer were measured and low peak DNL and INL values despite the use of a split capacitor array were achieved. The converter is able to operate at supply voltages down to 750 mV and current consumptions of below 10 nA. In high performance configuration an effective resolution of 9.924 bit in 11 bit mode and 7.946 bit in 8 bit was measured, which shows that the split capacitor array architecture can be used not just for low resolution converters. Comparison to state of the art work at prominent conferences shows the competitiveness of the design. For the given minimum gate length of 130 nm of the process, the current best energy efficiency is achieved.

6.5 Chapter 5 - Impedance Measurement Circuit

To show the applicability of the wireless sensor node an impedance measurement circuit was implemented, which takes advantage of the provided capabilities of the sensor interface. It performs an impedance spectroscopy, which is useful for a wide area of sensors, especially in the biomedical domain. To avoid stability problems and to enable a wide range of sensor impedances a current excitation scheme was used. The sensor connected to the circuit is excited by a digitally generated sine current and the resulting phase and amplitude of the voltage across the sensor are measured. Excitation frequencies from close to DC up to a few MHz and currents up to 1 mA can be forced with this implementation. As an example an interdigitated electrode structure sensor was used which was also built into various sensor nodes that were presented.

6.6 Outlook

With the increasing number of NFC enabled smart phones, the presented WSNs and subsequently developed products will be able to be used by millions of people around the globe. Complementary technologies that are known to be already under development, like integrated high capacity capacitors and on-chip batteries, will enhance the functionality and measurement quality even further. The use of these energy storage devices and new communication principles like Ultra-Wideband (UWB) communication will increase the possible operating distance and enable polling operation with only sporadic communication to a host device. Also, in the sensor field, new highly selective devices including carbon nanotubes are investigated and were already reviewed in conjunction with the presented sensor interface during this thesis.

The proposed low voltage and ultra-low power circuits and their architectures can be used to lower the current consumption of many state of the art systems. The switched capacitor bandgap

architecture can be optimized for various application requirements. Further current consumption savings are envisioned by using an OTA sharing principle which should enable current consumptions below 10 nA. Since a switching principle is already used, high accuracy references using offset compensation or chopped operation and dynamic element matching, are also possible with relatively low additional effort.

The architecture of the successive approximation ADC can also be used in smaller process nodes and even better energy efficiency values should be thus achievable.

Appendix A

Layout Plots

Note: All circuits except the UHF/HF rectifier, the sine look-up table and the EPC compliant communication unit were designed and laid out by myself. The two mentioned blocks were designed by Dipl.-Ing. Hannes Reinisch and Dipl.-Ing. Michael Klamminger. The on-chip antennas were designed by Dipl.-Ing. Walther Pachler and the top level designs of the sensor grains were done in collaboration with Dipl.-Ing. Günter Hofer.

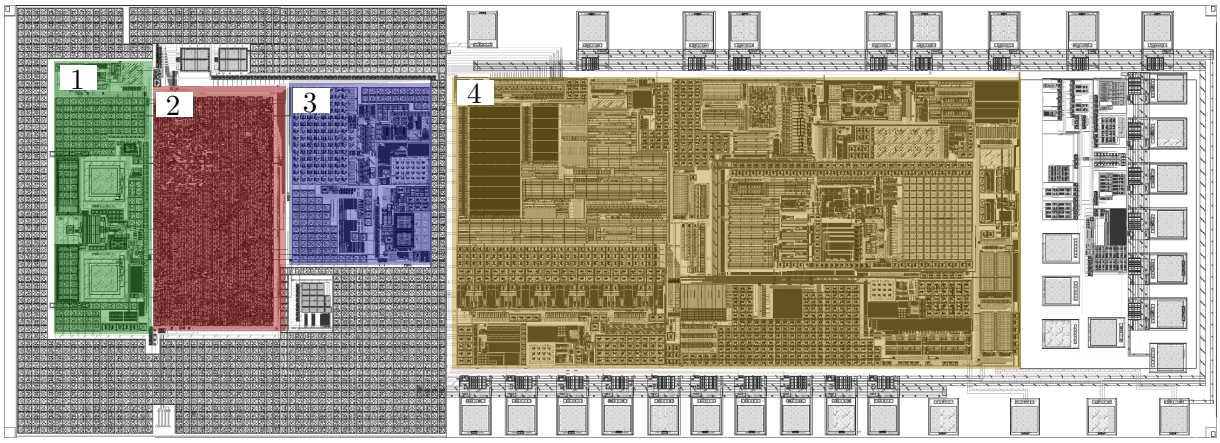


Figure A.1: Layout of sensor grain ASIC.

1	. . . . .	UHF and HF rectifier
2	. . . . .	EPC HF and EPC Class 1 Gen2 UHF compliant communication unit
3	. . . . .	On-chip monitoring block
4	. . . . .	Sensor interface

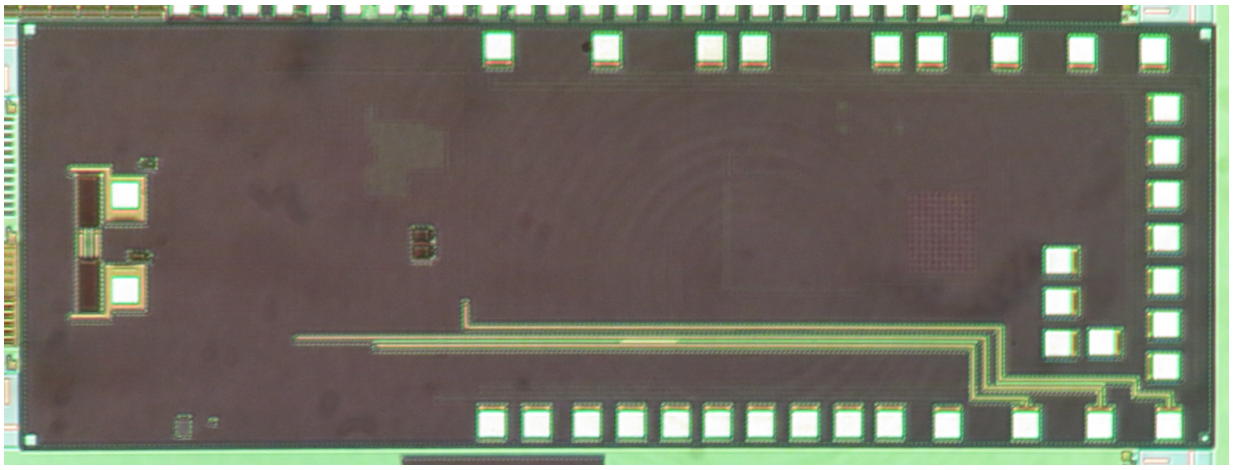


Figure A.2: Chip micrograph of sensor grain ASIC. 2.8mm x 1.0mm

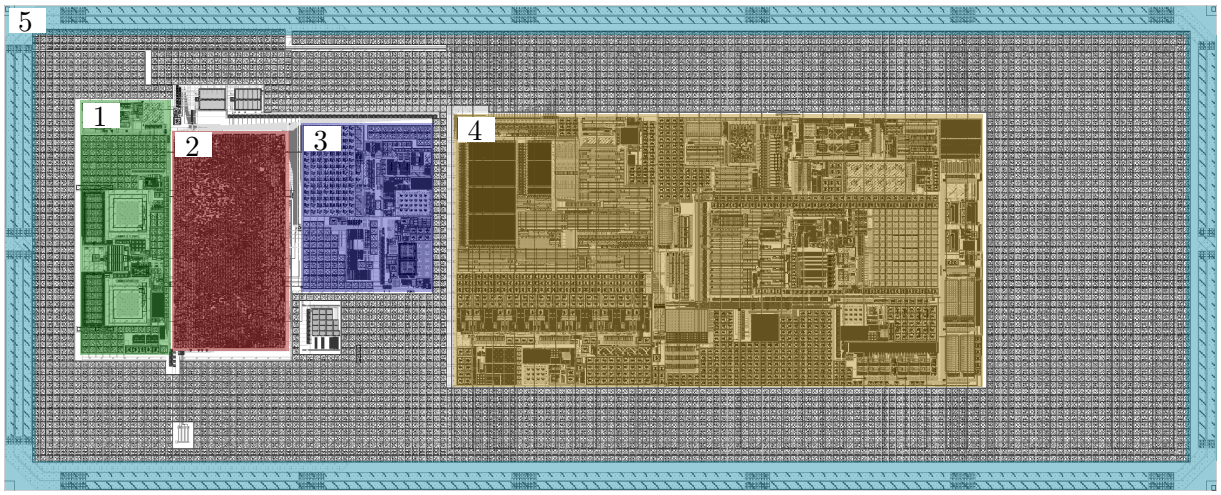


Figure A.3: Layout of fully integrated sensor grain ASIC.

1	. . . . .	UHF and HF rectifier
2	. . . . .	EPC HF and EPC Class 1 Gen2 UHF compliant communication unit
3	. . . . .	On-chip monitoring block
4	. . . . .	Sensor interface
5	. . . . .	On-chip UHF antenna

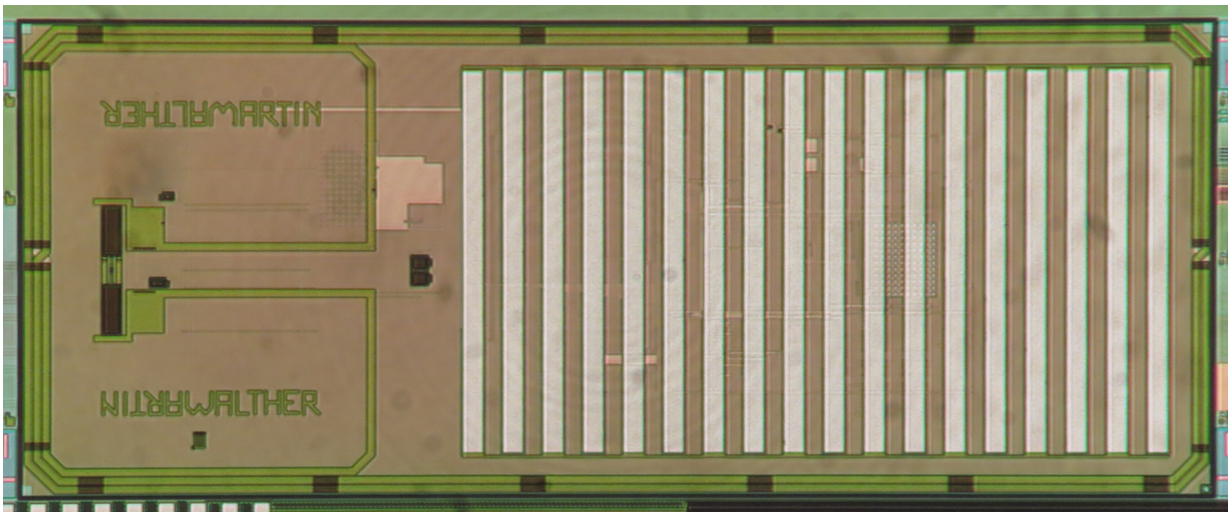


Figure A.4: Chip micrograph of fully integrated sensor grain ASIC. 3.0mm x 1.2mm

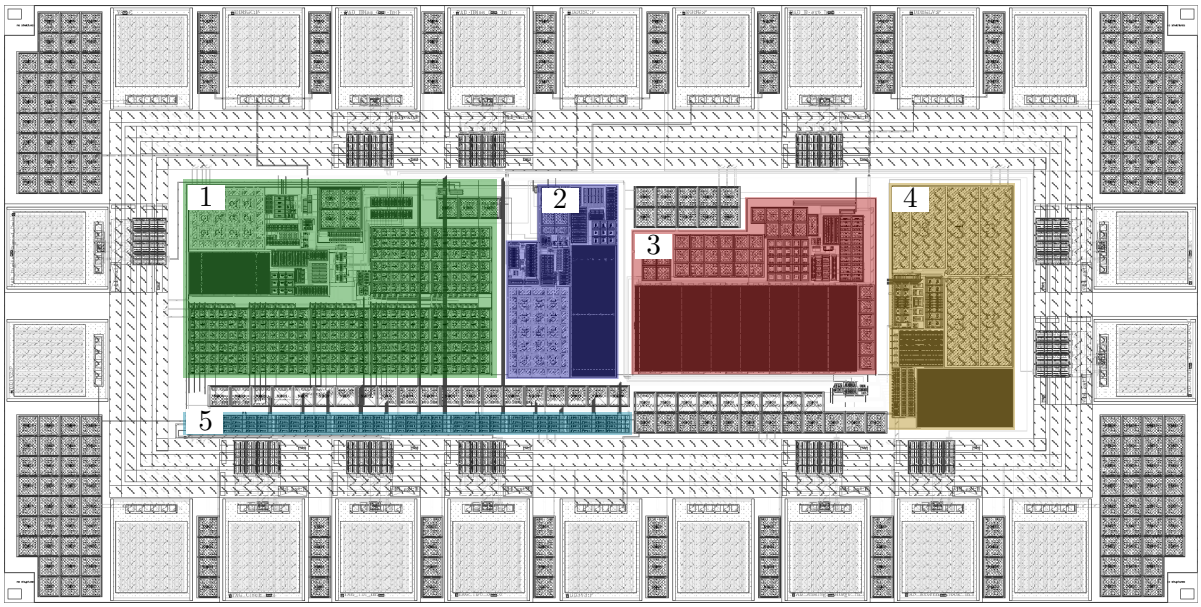


Figure A.5: Layout of bandgap test-chip.

1	. . . . .	Switched capacitor bandgap with adjustable capacitors
2	. . . . .	Switched capacitor bandgap
3	. . . . .	Low voltage bandgap
4	. . . . .	Analog output buffer
5	. . . . .	Serial configuration interface

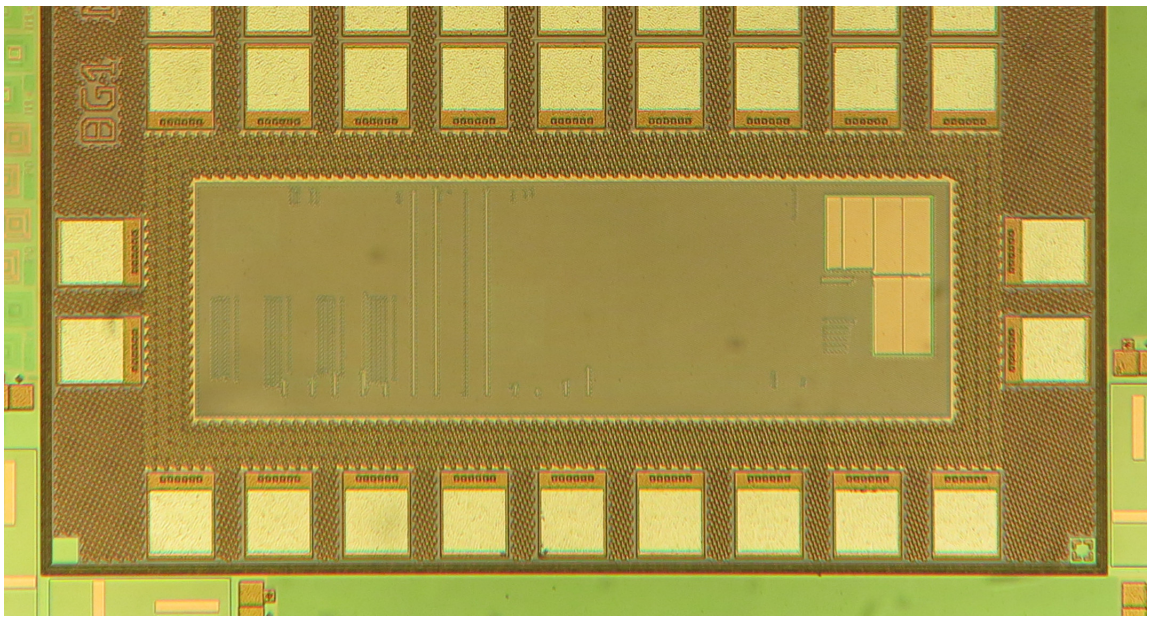


Figure A.6: Chip micrograph of bandgap test-chip. 1.0mm x 0.5mm

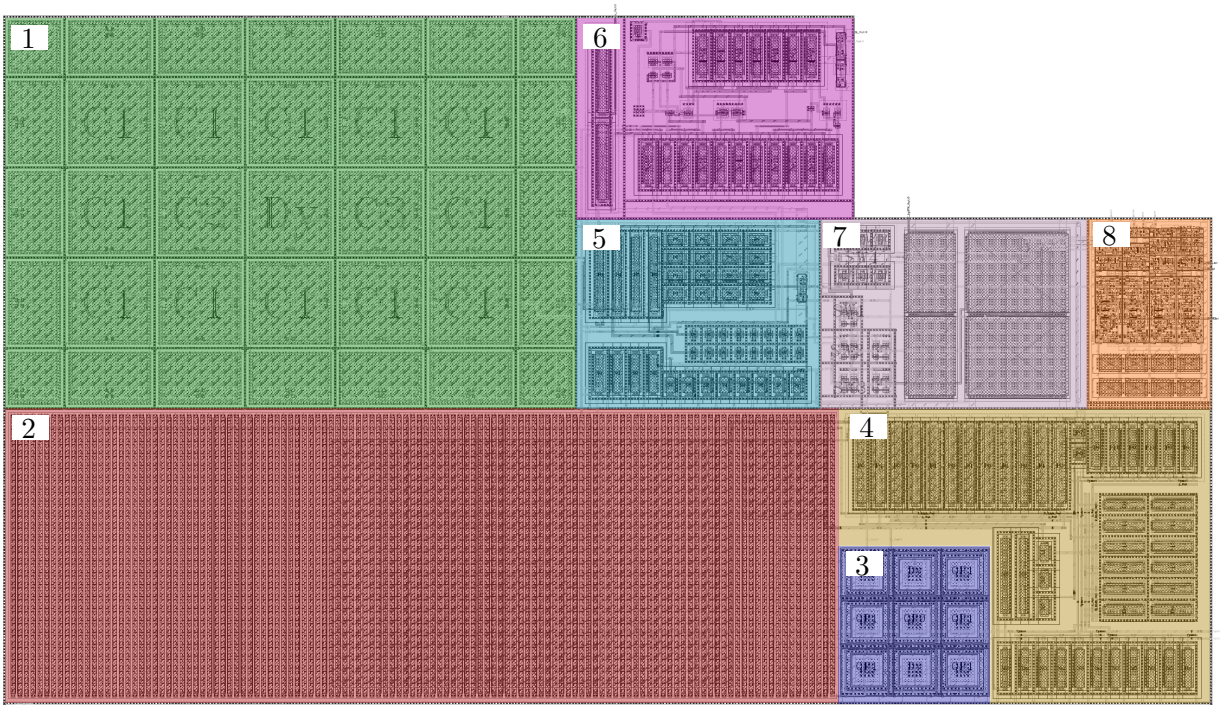


Figure A.7: Detailed layout of switched capacitor bandgap.

1	. . . . .	Capacitor array with dummy ring
2	. . . . .	Resistor R_1
3	. . . . .	PNP diode array
4	. . . . .	OTA1 in PTAT bias cell
5	. . . . .	OTA2 for switched capacitor steering
6	. . . . .	Comparator for relaxation oscillator
7	. . . . .	Transmission gates and capacitors
8	. . . . .	Digital timing unit

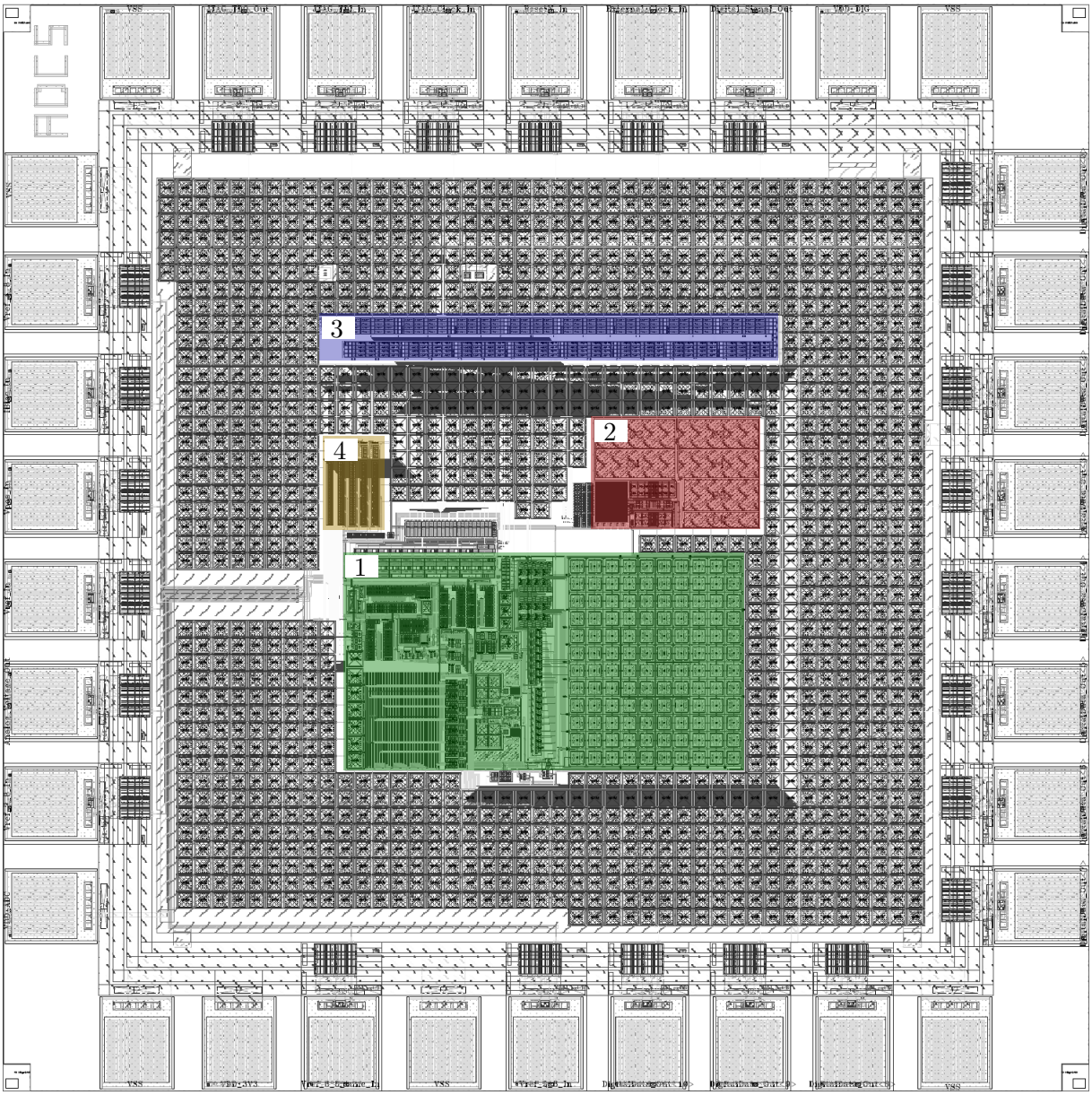


Figure A.8: Layout of dedicated ADC test-chip.

1	. . . . .	11 bit SAR ADC with capacitive array and resistive ladder
2	. . . . .	Analog output buffer
3	. . . . .	Serial configuration interface
4	. . . . .	Configurable biasing circuitry

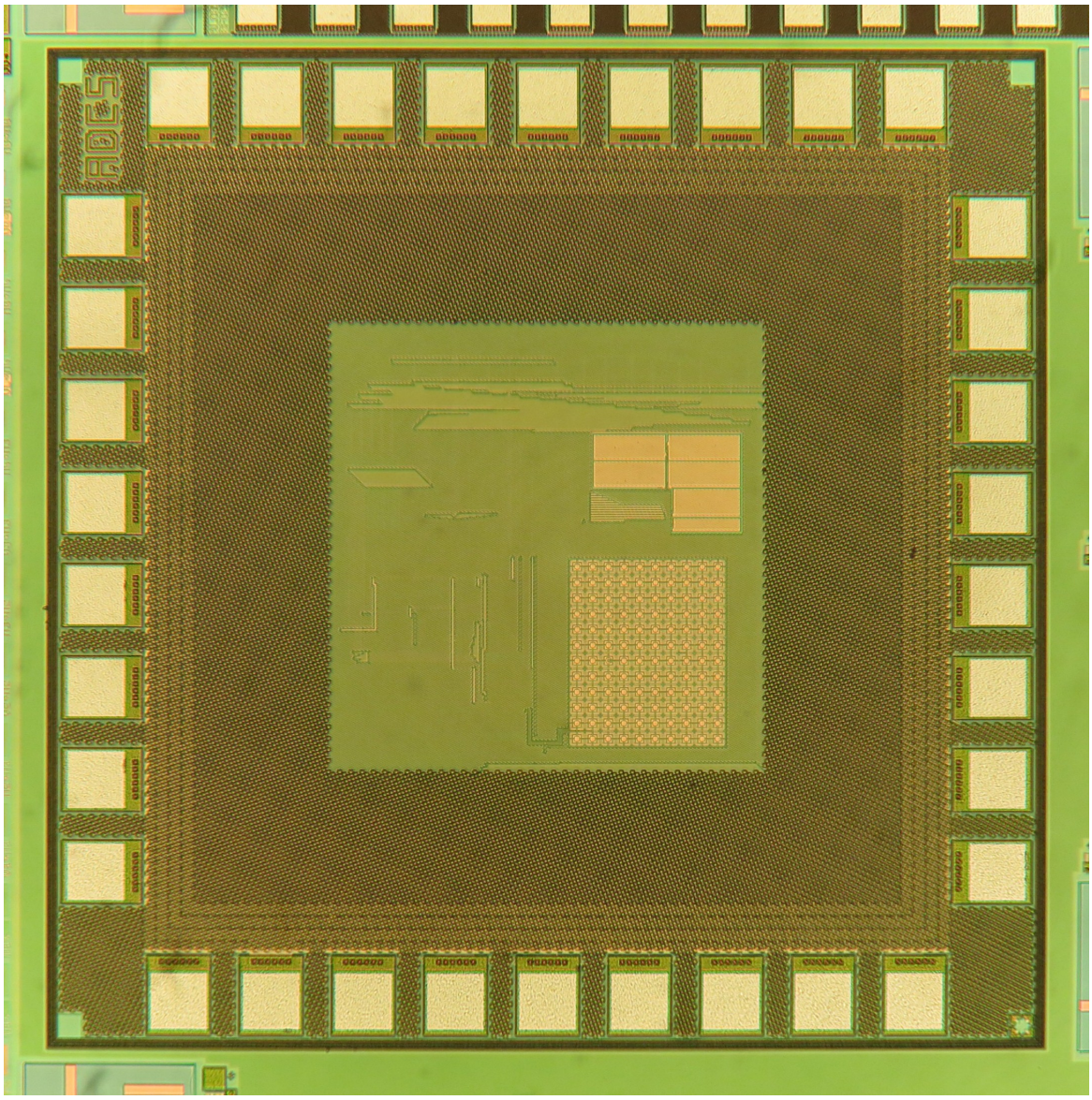


Figure A.9: Chip micrograph of dedicated ADC test-chip. 1.0mm x 1.0mm

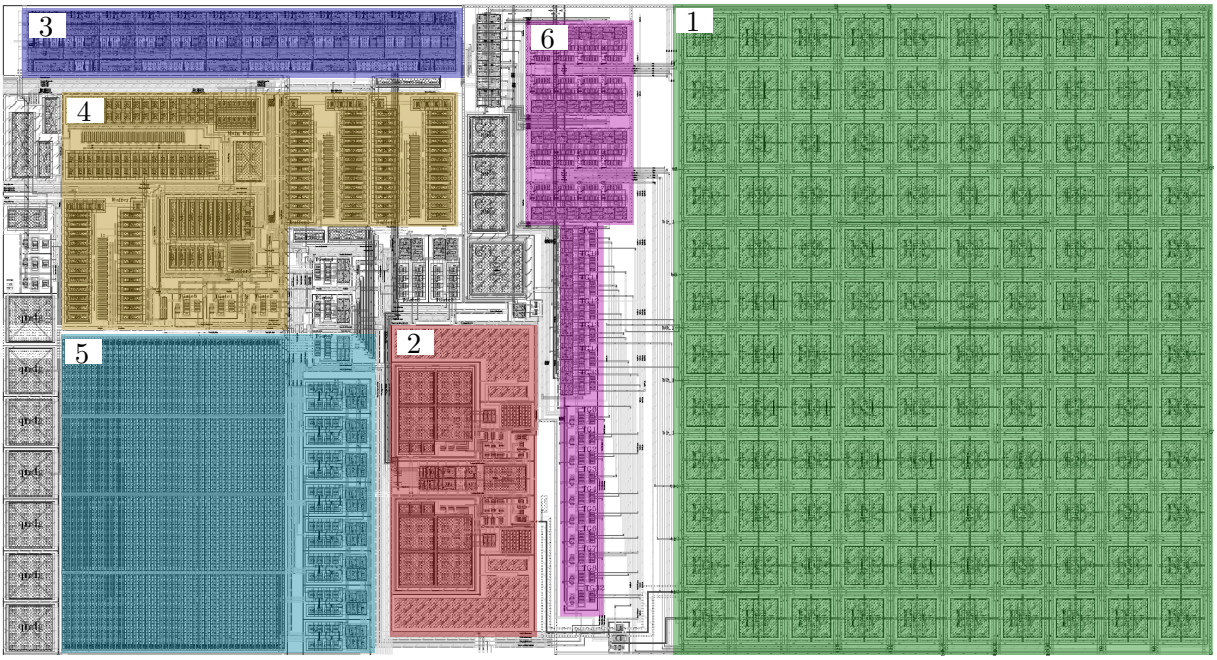


Figure A.10: Detailed layout of the 11 bit SAR ADC.

1	. . . . .	Single split capacitive array DAC with 8 bit resolution
2	. . . . .	Configurable noise time domain comparator
3	. . . . .	Successive approximation register
4	. . . . .	Analog buffers
5	. . . . .	Resistive ladder with transmission gates for calibration
6	. . . . .	Transmission gates for steering of the DAC capacitors

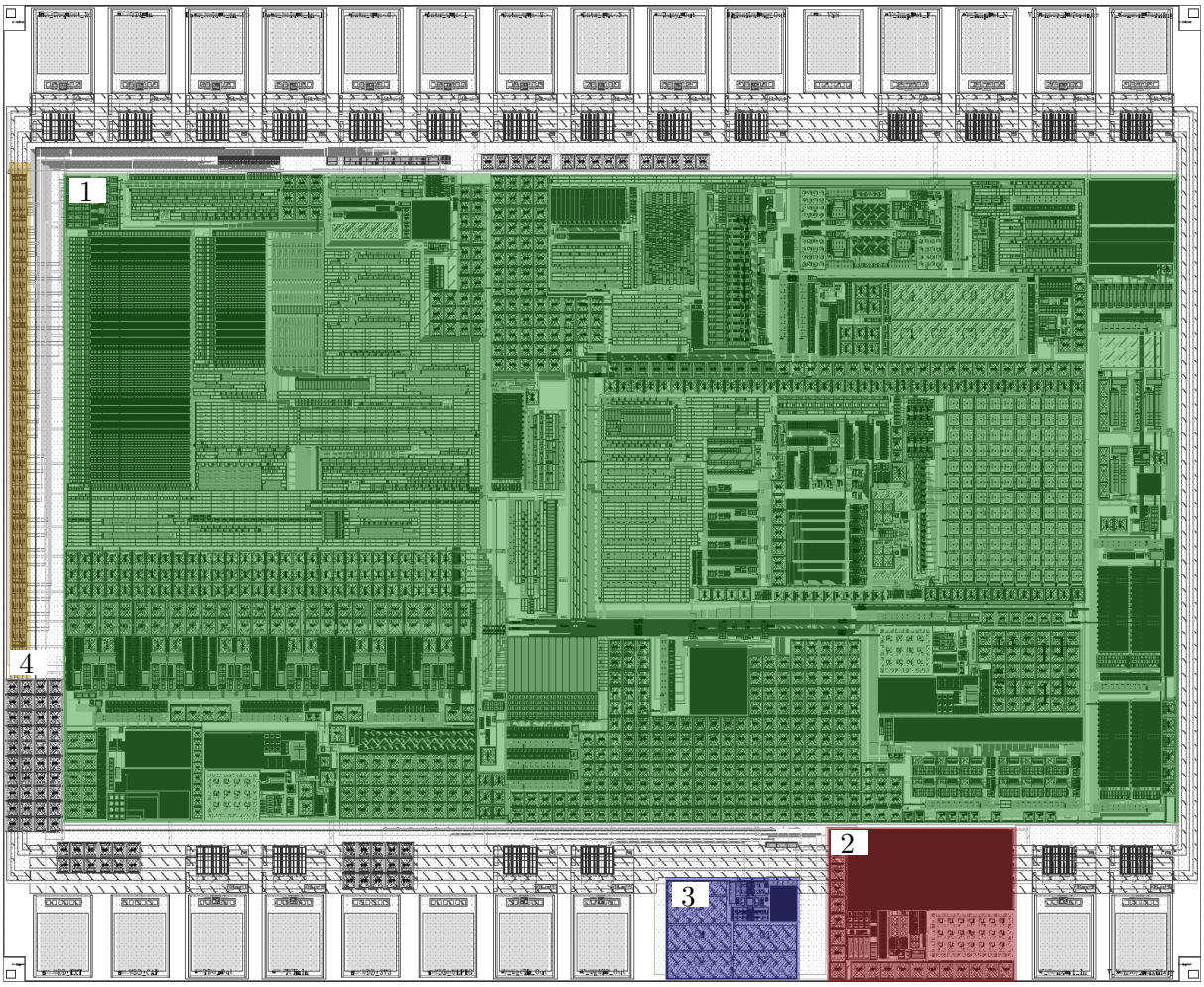


Figure A.11: Layout of dedicated sensor interface test-chip.

1	. . . . .	Sensor interface
2	. . . . .	Switched capacitor bandgap with 25nA current consumption
3	. . . . .	Analog output buffer
4	. . . . .	Serial configuration interface

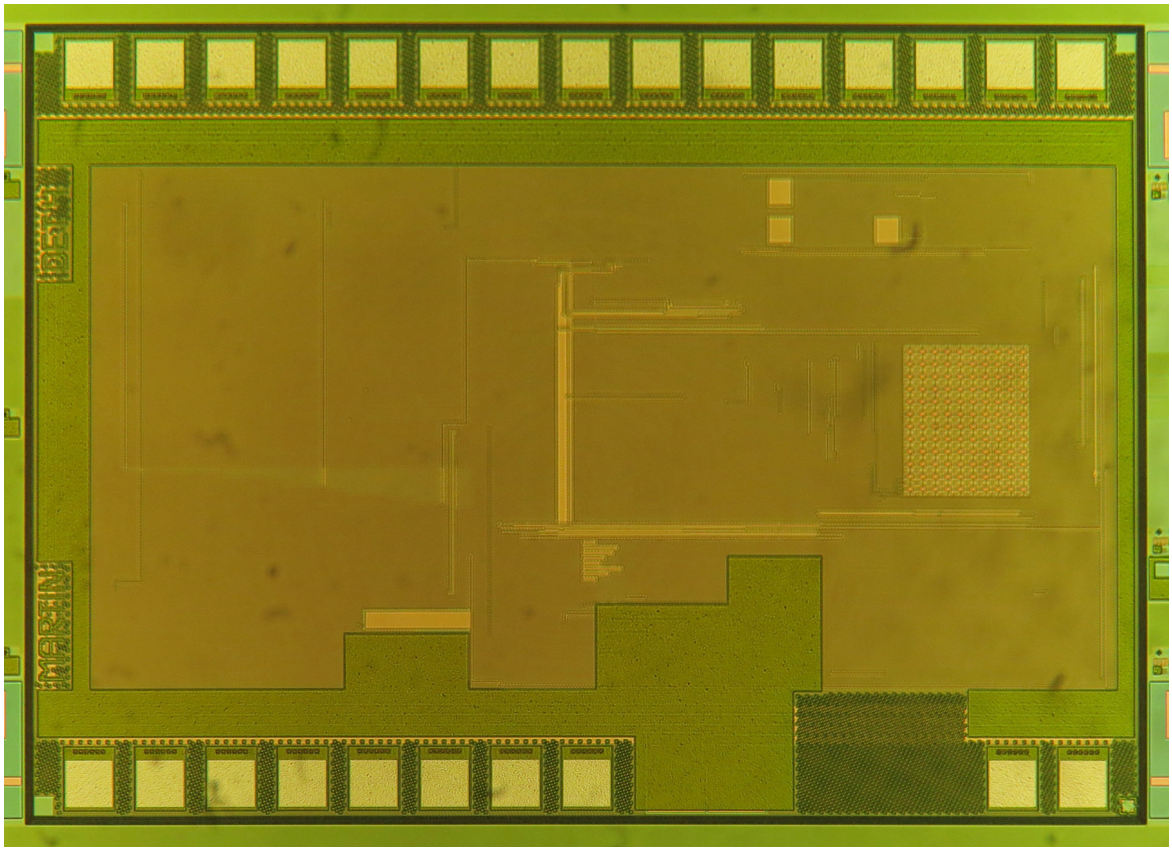


Figure A.12: Chip micrograph of the dedicated sensor interface test-chip. 1.4mm x 1.0mm

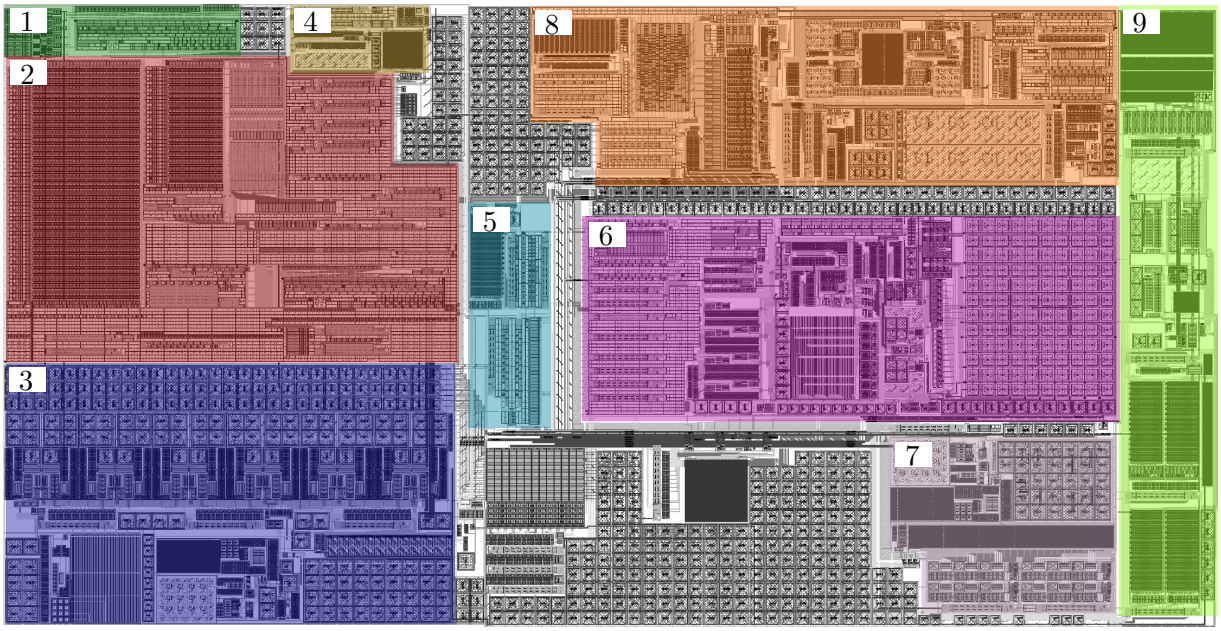


Figure A.13: Detailed layout of sensor interface.

1	. . . . .	Glue logic and digital communication interface
2	. . . . .	Microcontroller with SRAM
3	. . . . .	Voltage regulators
4	. . . . .	Oscillator for microcontroller
5	. . . . .	High frequency oscillator and 32 bit frequency counter
6	. . . . .	11 bit SAR ADC with biasing
7	. . . . .	Low noise reference generation, scaling and selection
8	. . . . .	Complex impedance measurement block
9	. . . . .	Voltammetry measurement block

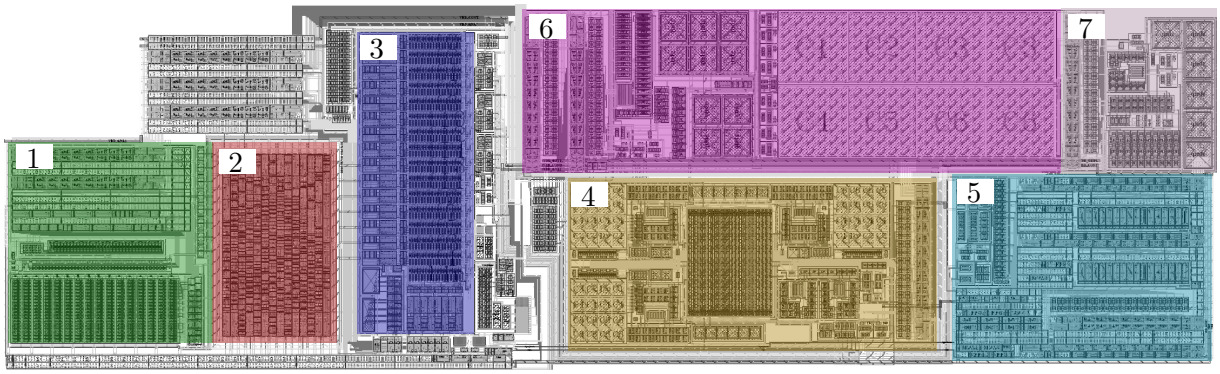


Figure A.14: Detailed layout of impedance detector.

1	. . . . .	Companion DAC
2	. . . . .	Sine look-up table
3	. . . . .	Current steering DAC
4	. . . . .	Instrumentation amplifier
5	. . . . .	Phase detector
6	. . . . .	Level shifter
7	. . . . .	Peak detector

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