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Design and verification of low quiescent current, general purpose, start-up regulators for SoC

Master Thesis

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Abstract

This work focuses on fast starting, low-dropout regulators intended to provide a crude voltage regulation for the start-up phase of SoC. An existing voltage regulator is analyzed and modifications to the design are discussed, in order to reduce current consumption and die area. The regulator contains a current reference and bias circuit, designed to work in weak inversion, which is employed to achieve a fast start-up of the regulator. The stability of this bias circuit is closely examined. The project specially addresses minimum current consumption (below 1 µA) and stability over wide load ranges (supporting load currents from 1 µA to 100 µA and load capacitors from 100 pF to 1 nF). The transient output behavior of the voltage regulator is analyzed and measures to decrease overshoot are discussed. Additionally, a different regulator topology is presented, which greatly improves the voltage regulation. Miller compensation with Q-reduction technique is employed to achieve stability in all load conditions. The circuit implements a novel back-gate circuitry to compensate the degradation of PSRR due to minimizing the current consumption. The presented designs are verified by simulation. A test-chip with prototypes of the designs is fabricated in a 160 nm CMOS technology and verified in laboratory.

Keywords: Power management, start-up regulator, LDO, beta-multiplier reference, low quiescent current, weak inversion design, Q-reduction, PSRR, back-gate circuitry.

Contents

Abstract iv

List of acronyms ix

1 Introduction 1
- 1.1 Structure of the work . . . 2

2 Specifications and design criteria 4
- 2.1 Circuit specifications . . . 4
- 2.2 Circuit topology . . . 5

3 Theory of subthreshold conduction and LDO regulators 7
- 3.1 MOSFET operation in weak inversion . . . 7
  - 3.1.1 Large and small signal model . . . 7
  - 3.1.2 Mismatch . . . 9
- 3.2 Linear regulators . . . 10
  - 3.2.1 Voltage divider . . . 10
  - 3.2.2 Regulation, stability . . . 12
  - 3.2.3 PMOS pass element . . . 17
  - 3.2.4 PSRR . . . 18
  - 3.2.5 Verification . . . 21

4 Current reference 23
- 4.1 Circuit description . . . 23
  - 4.1.1 Principle of operation . . . 23
  - 4.1.2 Stability of regulation . . . 25
  - 4.1.3 Resistor area reduction . . . 27
  - 4.1.4 Start-up circuit . . . 27
- 4.2 Circuit dimensioning . . . 28
- 4.3 Simulation . . . 29
  - 4.3.1 Temperature behavior . . . 29
  - 4.3.2 Start-up behavior . . . 31
  - 4.3.3 Stability . . . 32
  - 4.3.4 Power supply dependance . . . 32

4.3.5 Process variation and mismatch simulation 34

5 Analysis of the existing circuit and improvement 35
5.1 Circuit description 35
5.1.1 Bias circuit 35
5.1.2 Voltage divider 35
5.1.3 Reference voltage generation 37
5.1.4 Error amplifier and pass element 38
5.1.5 Frequency compensation 40
5.1.6 Power-down circuitry 42
5.1.7 Fine tuning 42
5.2 Simulation 43
5.2.1 Temperature behavior 43
5.2.2 Stability, regulation 43
5.2.3 Overshoot, caused by supply voltage variations 46
5.2.4 Overshoot and undershoot, caused by transient load current changes 48
5.2.5 Power supply ripple rejection 48
5.2.6 Current consumption 48
5.2.7 Process variation and mismatch simulation 51
5.2.8 Static line and load regulation 52
5.3 Circuit comparison 52

6 An LDO with a multi-stage error-amplifier 54
6.1 Bias ciruit 56
6.2 Voltage divider 56
6.3 Reference voltage generation 56
6.4 Frequency compensation 56
6.5 Supply voltage dependance 58
6.6 Dimensioning 59
6.7 Simulation 62
6.7.1 Temperature behavior 62
6.7.2 Stability, regulation 63
6.7.3 Overshoot, caused by supply voltage 63
6.7.4 Overshoot and undershoot, caused by transient load current changes 63
6.7.5 Power supply ripple rejection 66
6.7.6 Current consumption 66
6.7.7 Process variation and mismatch simulation 67
6.7.8 Static line and load regulation 67
6.8 Circuit comparison 68

7 Measurements and verification **69**
7.1 Static measurements 69
7.1.1 Temperature behavior 69
7.1.2 Static line and load regulation 72
7.2 Transient measurements 73
7.2.1 Overshoot, caused by supply voltage variations 73
7.2.2 Overshoot, caused by load variations 76
7.2.3 Stability 78
7.3 PSRR 80
7.4 Observed issues 81
7.4.1 No load condition 81
7.4.2 Oscillation of the new regulator 81

8 Conclusion **84**

Bibliography **86**

List of Figures

2.1 Topology of the regulator 6

3.1 Simplified diagram of a MOSFET voltage divider. 11
3.2 Simple model of the control system's topology. 12
3.3 Typical Bode plot of a loop gain with dominant pole. 13
3.4 Configuration for measuring the Bode plot of the loop gain. 14
3.5 Relationship between loop gain and PSRR. 19
3.6 OTA model presented by Gupta, Rincon-Mora, and Raha [10]. 19
3.7 Extended OTA model, derived from Gupta, Rincon-Mora, and Raha [10]. 20

4.1 Schematic diagram of the bias circuit. 24
4.2 Drain current plotted versus gate voltage of M1 and M2. 24
4.3 Small signal equivalent circuit of the beta multiplier. 26
4.4 Schematic diagram of the beta multiplier circuit with bypass transistor. 27
4.5 Schematic diagram of bias start-up circuit. 28
4.6 Schematic of the bias circuit. 30
4.7 Temperature plot of the bias current. 31
4.8 Start-up of the bias circuit. 32
4.9 Loop gain of the bias regulation. 33
4.10 Power supply ripple dependance of the bias circuit. 34

5.1 Schematic diagram of the existing circuit. 36
5.2 Schematic diagram of the modified circuit. 44
5.3 Output voltage of the regulator plotted over temperature. 45
5.4 Transient response of the regulator to supply voltage variations. . . . 47
5.5 Transient response of the regulator to load changes. 49
5.6 Plot of the improved circuit's PSRR over frequency. 50

6.1 Schematic of regulator circuit proposed by Lau, Mok, and Leung [16] . 55
6.2 Schematic of the back gate circuit to improve the PSRR. 60
6.3 Schematic of the start-up regulator with Q-reduction and PSRR back-gate circuit. 61
6.4 Output voltage of the regulator plotted versus temperature. 62
6.5 Bode plot of the loop gain. 64
6.6 Transient response of the regulator to supply voltage variations. . . . 65

6.7 Transient response of the regulator to load changes. 65
6.8 Plot of the PSRR versus frequency. 66

7.1 Measured output voltage of the regulators versus temperature 70
7.2 Measured current consumption of the regulators versus temperature . 70
7.3 Measured output voltages of all samples at 25 °C 71
7.4 Measured current consumption of all samples at 25 °C 72
7.5 Existing regulator: Overshoot of the output voltage due to a fast rising supply voltage. 74
7.6 Modified regulator: Overshoot of the output voltage due to a fast rising supply voltage. 74
7.7 New regulator: Overshoot of the output voltage due to a fast rising supply voltage. 75
7.8 Existing regulator: Response of the output voltage to a large load step. 76
7.9 Modified regulator: Response of the output voltage to a large load step. 77
7.10 New regulator: Response of the output voltage to a large load step. . 77
7.11 Existing regulator: Small signal load step response. 78
7.12 Modified regulator: Small signal load step response. 79
7.13 New regulator: Small signal load step response. 79
7.14 PSRR of the regulators, at minimal dropout voltage. 80
7.15 PSRR of the regulators, at typical conditions. 81
7.16 Existing regulator: Small signal load step response, no load condition. 82
7.17 Modified regulator: Small signal load step response, no load condition. 82
7.18 New regulator: Small signal load step response, no load condition. . . 83

List of acronyms

SoC	System on a Chip
STUP	Start-up Voltage Regulator
IP	Intellectual Property
ESD	Electrostatic Discharge
ESR	Electrical Series Resistance
PSRR	Power Supply Ripple Rejection
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PTAT	Positive to Absolute Temperature
NTAT	Negative to Absolute Temperature
UGF	Unity Gain Frequency
PM	Phase Margin
LHP	Left Half Plane
RHP	Right Half Plane
OTA	Operational Transconductance Amplifier
GBW	Gain-Bandwith Product
VLSI	Very Large Scale Integration
LDO	Low Drop-out Regulator
BIBO	Bound-input-bound-output
V_{DD}	Supply Voltage
V_{out}	Output Voltage
C_L	Load Capacitor
I_L	Load Current

List of acronyms

R_L	Load Resistor
C_C	(Miller) Compensation Capacitor
V_T	Thermal Voltage ($k \cdot T/q$)
g_m	Transconductance
DIP	Dual Inline Package

1 Introduction

Power management is an increasingly important topic in today's system-on-a-chip (SoC) development. As mobile equipment becomes a key market for many semiconductor manufacturers, new requirements for SoCs gain importance. One of the main requirements of the market is, that SoCs can operate absolutely autarkic. External voltage regulators or buffer capacitors are no longer accepted by the customers. This calls for complete and accurate on-chip power management solutions. Buffer capacitors and compensation capacitors need to be implemented as on-chip devices, making the design of power regulators a challenging task.

Another key requirement is power efficiency. Battery sizes start to dominate dimensions of mobile equipment. To increase the battery lifetime without enlarging the dimensions of a mobile device, all sub-systems of the device need to be optimized for current efficiency. This does not only apply to the power consumption in normal operation, but also to standby currents.

Today's SoCs are manufactured in large volumes. Thus, area consumption on the die and production yield are the most important performance figures in semiconductor manufacturing. Both figures need to be optimized to become competitive on the market.

All these requirements lead to completely integrated power regulators with minimum area and current consumption, as part of the SoC. Robust design and high accuracy are key features. These regulators need to provide a safe and controlled environment for the on-chip system and protect it from a potentially noisy and unstable environment.

Typically, the core of a power management systems consists of an accurate voltage regulator. This regulator is intended to provide a specified and stable power supply for the SoC's sub-systems, regardless of changing line and load conditions. The accuracy of such a voltage regulator depends on an exact voltage reference. In most cases a band-gap circuit is used, which provides an accurate and temperature compensated reference voltage.

In order to improve the performance of such a band-gap circuit, it may be supplied from the stable output of the voltage regulator. However, in that case a chicken-egg problem arises. At start-up, the voltage regulator has no reference voltage for

operation, as the reference circuit is powered by the regulator. One solution to overcome this issue is to use an additional start-up regulator (STUP). This is a crude voltage regulator, which contains a simple voltage reference. The STUP does not provide an accurate output voltage, but starts up and settles quickly. It is used in the first instance of time after power-on, to provide a safe power supply for the band-gap circuit to start up. Once the band-gap circuit has settled, the main voltage regulator of the power management system is switched on and takes over the voltage regulation from the STUP. In turn, the STUP is shut off.

A STUP should not be seen as a classic voltage regulator of great accuracy with excellent line and load regulation. Its only task is to provide a safe supply voltage at start-up. It must start up very fast and contains a fast settling voltage reference circuit. A STUP is not used in normal operation, thus it must exhibit an ultra low standby-current. It must be seen as overhead for the SoC and is usually designed for minimum area and power requirements, at the cost of accuracy and regulation performance.

In the fast evolving semiconductor market, the project cycle times are progressively reduced. The time from project specification to chip tape-out can only be decreased efficiently by reusing already existing functional blocks. It is therefore a general practice to keep analog building blocks in IP-libraries for reuse. For best re-usability, such libraries should possibly contain blocks, which are designed to work in a wide range of operation conditions.

The scope of this work is focused on the design of a STUP regulator with a wide operation range and a wide load range. The STUP is intended to be used in different SoC products. After complete characterization of the circuit, it shall be entered into an IP-library. The work especially aims for power reduction and die area reduction of the designed STUP, while maintaining a wide operation range.

The starting point of this work was an already existing STUP. It was the aim of this work to entirely analyze the existing circuit and do a complete verification. In a second step, different modifications to the circuit were proposed, implemented and verified. At last, a literature research for a state-of-the-art circuit topology was performed. After selection of an appropriate circuit topology, a new STUP was designed and verified.

1.1 Structure of the work

This work is divided into 8 chapters which describe the different phases of the project.

Chapter 1: Introduction

Chapter 2: Specifications and design criteria
This chapter contains the project specifications and requirements of the STUP.

Chapter 3: Theory of subthreshold conduction and LDO regulators
This chapter describes the needed theoretical concepts to design the STUP. The used device models, the different building blocks of voltage regulators, stability and power-supply-ripple-rejection are explained.

Chapter 4: Current reference
This chapter explains the theoretical concept and the implementation of the needed bias and reference circuitry.

Chapter 5: Analysis of the existing circuit and improvement
This chapter describes the analysis of the existing STUP, the modifications implemented and a circuit comparison.

Chapter 6: An LDO with a multi-stage error-amplifier
This chapter provides the design and implementation of a state-of-the-art voltage regulator.

Chapter 7: Measurements and verification
This chapter describes the executed measurements and the test setup, as well as the measurement results.

Chapter 8: Conclusion
This chapter provides a summary of the work and a conclusion.

2 Specifications and design criteria

The start-up regulator shall be designed in the standard NXP *CMOS*14 technology. This is a 160 nm CMOS technology with 5 metal layers. It provides 1.8 V and 3.3 V devices. The regulator is to be used in SoC products operated at supply voltages of 1.8 V to 3.6 V.

2.1 Circuit specifications

The STUP is intended to be connected directly to a supply pad with only first order ESD (Electrostatic Discharge) protection. Therefore it needs to operate at input voltages V_{DD} ranging from 1.8 V up to 3.6 V. Due to this, it is essential to use thick oxide (3.3 V) devices in the design, which have a minimum channel length of 322 nm.

It needs to provide a stable voltage at the output V_{out}, to ensure a safe start-up phase for the following circuits. The low voltage transistors in the following circuits are specified to work at maximum 1.8 V and will withstand voltages up to 2.5 V [22]. Thus it was specified, that the output voltage V_{out} shall stay in the range of 1.2 V to 1.8 V. Voltage spikes which may happen at start-up and transient line or load changes, up to 2 V are allowed.

For a wide operation range, the STUP should work with capacitive loads (C_L) ranging from 100 pF to 1 nF and output currents (I_L) from 1 µA to 100 µA. The operation temperature (T) was specified $-50\,°C$ to $150\,°C$. The current consumption (I_{DDq}) of the regulator in steady-state conditions should be well below 1.5 µA.

The voltage regulation should be stable for the above specified input voltages and load conditions. The regulation loop should have a unity gain frequency (UGF) higher than 5 kHz with a phase margin (PM) higher than 15° at worst case conditions.

The power supply ripple rejection ($PSRR = \frac{\delta V_{out}}{\delta V_{DD}}$) should stay below 0 dB for all frequencies.

It must be possible to switch off the STUP. Via a power-down signal, the output should go into a high impedance mode, the circuit should then draw no more current from the supply line.

Table 2.1: Summary of the circuit specifications.

	Min.	Max.	
T	-50	150	°C
V_{DD}	1.8	3.6	V
V_{out}	1.2	1.8	V
$V_{out_{spike}}$		2	V
UGF	5		kHz
PM	15		°
$PSRR$		0	dB
I_{DDq}		1.5	µA
C_L	0.1	1	nF
I_L	1	100	µA

2.2 Circuit topology

The circuit topology had already been defined. A basic linear voltage regulator design with a PMOS pass element was to be used. A schematic can be seen in figure 2.1. The output voltage is sensed via a voltage divider network. An error amplifier is used to compare the sensed voltage with a reference voltage. The voltage error is then used to control the gate voltage of the PMOS pass element. The reference voltage is generated via a MOS-Diode and a reference current source. This reference current source is also used to bias the error amplifier.

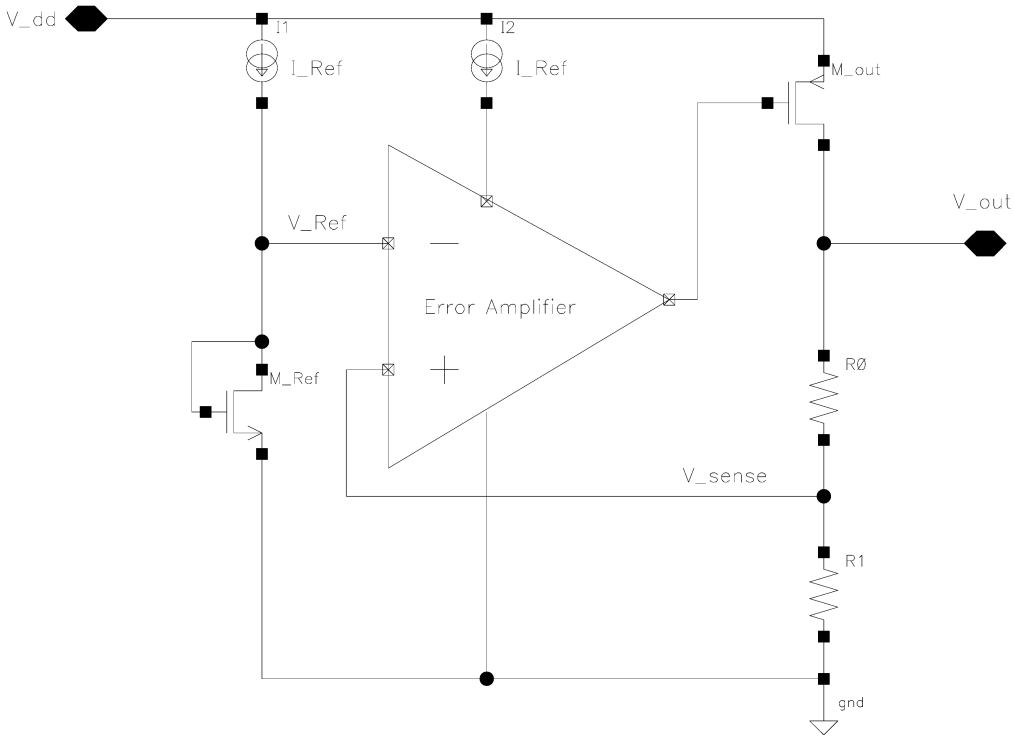

Figure 2.1: Topology of the regulator circuit

3 Theory of subthreshold conduction and LDO regulators

An extensive literature research was done on selected topics needed for this project, which are the operation of MOSFET transistors in the weak inversion region and low drop-out linear regulators.

3.1 MOSFET operation in weak inversion

The overall current of the voltage regulator will be smaller than 1.5 µA. Thus, the transistors will operate with bias currents in the range of nA. For the used technology, avoiding extremely small aspect ratios, most MOSFET devices will operate in weak inversion (at a gate source voltage below the threshold voltage). Some literature research was done on large and small signal models and mismatch of MOSFET transistors in weak inversion.

3.1.1 Large and small signal model

The drain current of a MOSFET in weak inversion is due to diffusion processes and not caused by drift as in normal operation [29]. In this work a simple exponential [31] model was used to calculate the large signal behavior of a MOSFET transistor in weak inversion. The drain current I_D of a MOSFET in weak inversion is approximately given by formula 3.1. Where I_{D0} represents the normalized current when the gate source voltage V_{GS} equals the threshold voltage V_{th}, $\frac{W}{L}$ represents the aspect ratio of the transistor channel, V_T is the thermal voltage ($\frac{k \cdot T}{q}$) and n is the process dependent slope factor of the sub-threshold diffusion current. The slope factor n is usually between 1 and 1.5 [29]. It is assumed that the drain source voltage V_{DS} is much higher than V_T.

$$I_D \approx \frac{W}{L} I_{D0} \cdot e^{\frac{V_{GS}-V_{th}}{n \cdot V_T}} \tag{3.1}$$

The similarity of the above quoted formula with the *Ebers–Moll model* [5] is evident. The behavior of the transistor in weak inversion is therefore similar to that of a bipolar transistor. Formula 3.2 gives the transconductance g_m of such a transistor. It can be seen that $\frac{g_m}{I_D}$ is constant for any transistor, independent of device sizes [29], as for bipolar transistors. Still, the transconductance-to-current ratio is smaller, due to the slope factor n.

$$g_m = \frac{I_D}{n \cdot V_T} \tag{3.2}$$

However, this model is not absolutely accurate. The model assumes a gate source voltage well below the threshold voltage. The region around the threshold voltage, where drift currents and diffusion currents are both present, is sometimes called moderate inversion and does neither show an exponential, nor a quadratic behavior. Additionally, the model does not take leakage currents into account. For very low gate-source voltages, the leakage currents reach the same magnitude as the gate induced currents. Thus the exponential curve flattens out with further decreasing gate-source voltages and eventually, the gate induced currents are masked by the leakage currents [29, p. 174].

In the used technology, the transconductance-to-current ratio $\frac{g_m}{I_D}$ is only constant for gate source voltages approximately 100 mV below the threshold voltage. For gate source voltages below this limit, $\frac{g_m}{I_D}$ for NMOS transistors is approximately 25, and approximately 23 for PMOS. At the threshold voltage, $\frac{g_m}{I_D}$ for NMOS transistors is approximately 17.5, and approximately 15 for PMOS, as simulations show.

Formula 3.1 suggests, that the drain source voltage has no influence on the drain current. This implies an infinite output resistance. However, in reality the behavior is similar to that in saturation [29]. The output resistance r_{ds} can be approximated with[29]:

$$r_{ds} = \frac{U_{AW}}{I_D} \quad , \tag{3.3}$$

where U_{AW} resembles the *Early Voltage* of bipolar transistors. Again, it is assumed that V_{DS} is much higher than V_t. As for saturation, U_{AW} is roughly proportional to the channel length L [29].

It can be shown that the intrinsic voltage gain of a transistor is independent of the drain current and only proportional to L (channel length):

$$A_0 = g_m \cdot r_{ds} = \frac{I_D}{n \cdot V_T} \frac{U_{AW}}{I_D} = \frac{U_{AW}}{n \cdot V_T} \propto L \tag{3.4}$$

Thus the channel length becomes a major design factor when designing a circuit in weak inversion.

For a MOSFET in weak inversion, the negative temperature behavior of the threshold voltage is the dominant temperature effect. Thus, for a given gate voltage, the drain current increases with temperature [29]. The transconductance depends on the drain current and the thermal voltage V_T. To keep a constant g_m over temperature, a transistor needs to be biased with a PTAT (positive to absolute temperature) current, proportional to $n \cdot V_T$. Keeping g_m of some transistors nearly constant is necessary for a constant small signal behavior, to retain stability of the voltage regulator over temperature, as described later on.

3.1.2 Mismatch

"Mismatch is the process that causes time-independent random variations in physical quantities of identically designed devices" (Pelgrom, Duinmaijer, and Welbers [23])

Mismatch is a dominant topic in VLSI design. As circuit dimensions decrease, mismatch reduction methods become a major design criterion. Circuit designs where mismatch reduction measures were considered will typically exhibit a higher production yield. Methods and design rules for mismatch reduction of MOS transistor circuits operated in strong inversion are well known for several years [1, 23, 25]. However, there has not been as much research on mismatch of MOS transistors operated in weak inversion.

Some research on mismatch of MOS-transistors in weak inversion was considered [9, 14, 30]. The research works were all done by measuring the current mismatch of current mirror pairs. The common outcomes of these researches are:

- Current mismatch increases, when moving from strong to weak inversion. However, when entering weak inversion, the mismatch curve flattens out and becomes nearly independent of the inversion level. An alternative approach to understand this behavior is to use the $\frac{g_m}{I_d}$ design methodology [6, 13]: In order to reduce mismatch, a current mirror should be designed with low $\frac{g_m}{I_d}$ [1, 13, 25]. By decreasing the overdrive voltage, $\frac{g_m}{I_d}$ increases at first, but then becomes nearly constant in weak inversion (neglecting leakage currents).
- The current mismatch in weak inversion is nearly independent of the current density in the transistor. This implies, together with the first result, that the aspect ratio of the transistor has no influence on the current mismatch as long as it stays in weak inversion. Again, from the $\frac{g_m}{I_d}$ point of view: $\frac{g_m}{I_d}$ is independent of the aspect ratio in weak inversion.
- The transistor area is a dominant design criterion to reduce mismatch (as for strong inversion [23]). Mismatch is roughly inversely proportional to the square root of the channel area.

3.2 Linear regulators

This section is focused on selected topics of a simple PMOS regulator as introduced in chapter 2.2.

3.2.1 Voltage divider

A voltage divider is connected to the output of the regulator to sense the output voltage. The sensed voltage is then fed back to the input of the error amplifier. Assuming an ideal error amplifier, the output will be regulated, such that both inputs of the error amplifier are at the same potential. Thus, considering the topology in figure 2.1, it is clear that the voltage drop over $R1$ will be equal to V_{Ref}. The output voltage can then be calculated via

$$V_{out} = V_{Ref} \cdot \left(\frac{R1 + R0}{R1} \right) = V_{Ref} \cdot \frac{1}{\beta} \ , \tag{3.5}$$

where β is called the feedback factor.

The current flowing through the voltage divider is limited by the circuit specifications. The complete regulator is targeted to need less than $1\mu A$ at $27°C$ (to stay below the specification of $1.5\mu A$ at $150°C$). The voltage divider should therefore consume less than $100nA$. At a nominal output voltage of $1.5V$, the resistors would need to be in the range of $M\Omega$. They would need a very large die area. It is more practical to use transistors instead of resistors, as shown in figure 3.1.a. The output voltage is then:

$$V_{out} = V_{Ref} \cdot \left(1 + \frac{V_{GS1}}{V_{GS2}} \right) = V_{Ref} \cdot \frac{1}{\beta} \tag{3.6}$$

Such a MOSFET divider can be made process and temperature independent in a very simple way: First of all, only PMOS transistor should be used (in a N-Well process), with source and bulk connection shorted. In this manner threshold voltage changes due to body effect will be avoided. Next, the transistors should be operated at the same gate source voltage, meaning the transistors should have an equal aspect ratio and channel area. In that case, their gate source voltage will exhibit the same temperature behavior, and they will have the same process variation. As only the ratio $\frac{V_{GS1}}{V_{GS2}}$ defines the voltage division factor, these changes will be suppressed. If the transistors are designed with a large area, the mismatch between the transistor will be minimized [23], which will improve the accuracy of the designed feedback factor.

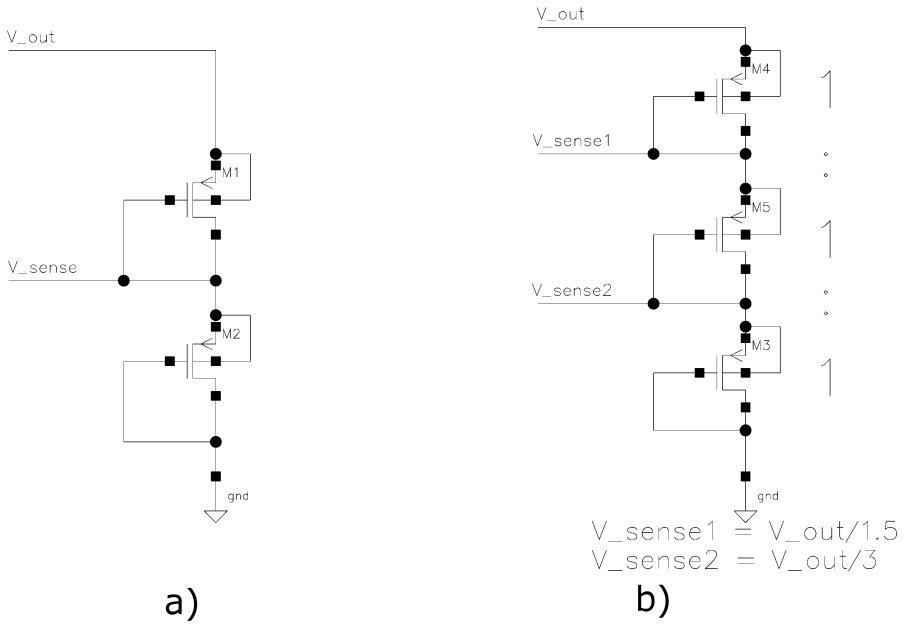

Figure 3.1: Simplified diagram of a MOSFET voltage divider.

At higher frequencies, the parasitic capacitance of the MOSFETs are to be considered. As the frequency of the output voltage increases, the voltage divider will turn into a capacitive voltage divider. In this case, the MOSFET's parasitic capacitance should have the inverse ratio as the gate source voltages, to keep the feedback factor constant. Again, this can be achieved with transistors of the same aspect ratio and channel area.

However, using unity transistors will greatly limit the possible feedback factors. As every transistor will typically consume 0.5 V or more, it will not be possible to use more than 3 transistors to sense an output voltage of 1.5 V as seen in figure 3.1.b. Thus the possible feedback factors are $\frac{2}{3}$, $\frac{1}{3}$ (using 3 transistors), and $\frac{1}{2}$, which leads to 3 possible reference voltages: 0.5 V, 1 V and 0.75 V. Additionally, the output voltage could be fed back without a voltage divider. In that case a reference voltage of approximately 1.5 V would be needed.

The design of the voltage divider must therefore begin with choosing a reference voltage suitable for the input common mode range of the error amplifier. The voltage divider is then chosen from the above values. The aspect ratio of the transistors is then sized for the desired current through the voltage divider.

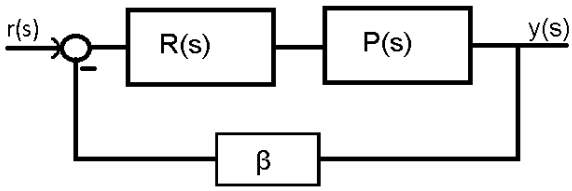

Figure 3.2: Simple model of the control system's topology.

3.2.2 Regulation, stability

The circuit topology described in 2.2 can be modeled as a linear, time invariant control system. Figure 3.2 shows such a simple model. The signals $r(s)$ and $y(s)$ represent the reference voltage and the output voltage, respectively. The subtracter and $R(s)$ model the error amplifier, $P(s)$ models the the PMOS pass element and the load impedance connected to the regulator and β represents the feedback network, which is realized as voltage divider. β is typically 1 or smaller and constant up to very high frequencies. The transfer function of such a system can be given by formula 3.7. The expression $\beta \cdot L(s)$ is called the loop gain of the system [25].

$$\frac{y(s)}{r(s)} = \frac{R(s) \cdot P(S)}{1 + \beta \cdot R(s) \cdot P(s)} = \frac{L(s)}{1 + \beta \cdot L(s)} \tag{3.7}$$

Such a system is considered BIBO (bound input bound output) stable if the denominator of the transfer function is a *Hurwitz-polynomial*. Analytical methods like the *Hurwitz-criterion* or the *Routh-scheme* may be used [4] to verify stability. However, this is not very convenient because $P(s)$ might be difficult to determine as it is is a function of the load impedance.

A practical way to check the stability of such a system, is using the *simplified Nyquist-criterion*. With this criterion, the stability of a system (as described above) can be determined by evaluating the loop gain $\beta \cdot L(j\omega)$. The loop gain may be determined by simulation or measurement. In order to use this criterion the loop gain needs to satisfy the following conditions [4, p. 110]:

- $\beta \cdot L(j\omega)$ has a low pass character.
- The amplification factor (DC gain $\beta \cdot L(j0)$) is positive.
- All poles of $\beta \cdot L(j\omega)$ are on the left half-plane, except from one possible pole at zero.
- There exists only one transition frequency ω_c [rad], where the absolute magnitude of $\beta \cdot L(j\omega)$ is one: $|\beta \cdot L(j\omega_c)| = 1$

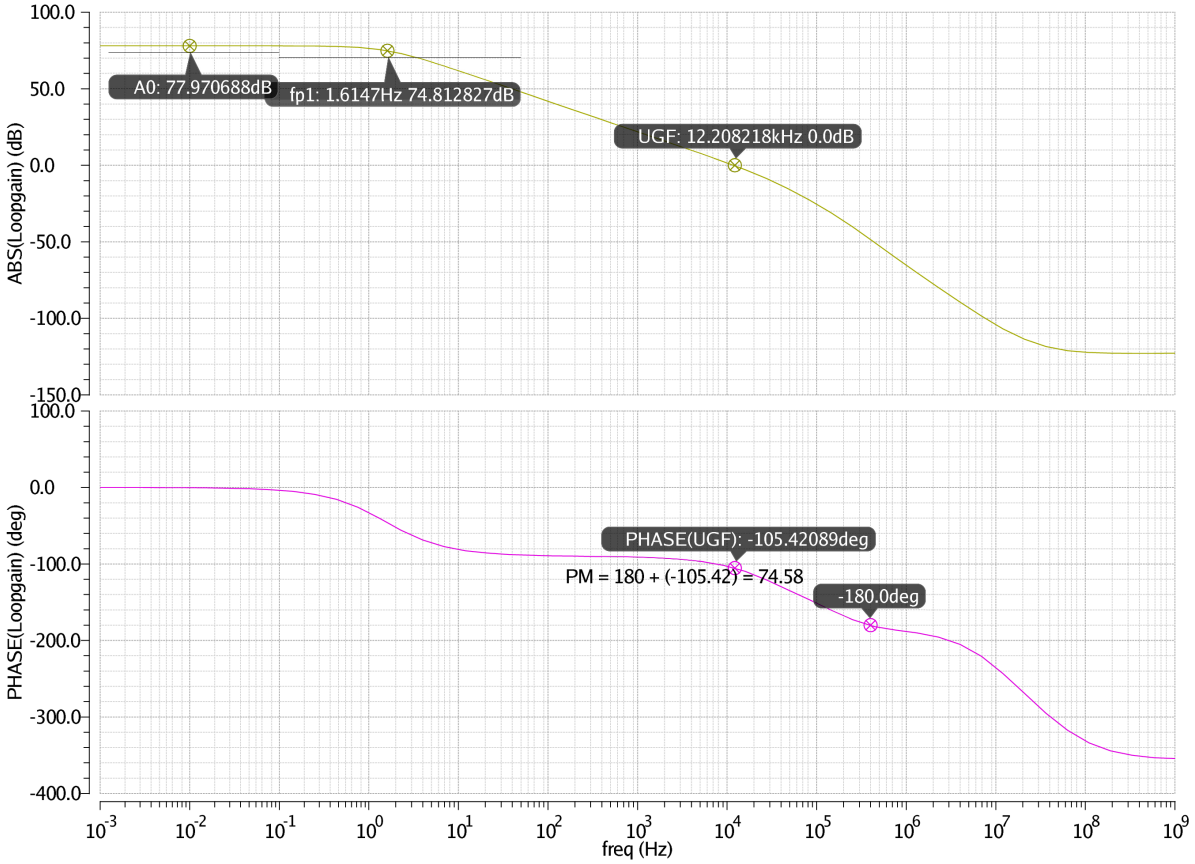

Figure 3.3: Typical Bode plot of a loop gain with dominant pole.

Whether these conditions are fulfilled, can be seen from the Bode plot of $\beta \cdot L(j\omega)$. Conditions 1, 2 and 4 are evident. Condition 3 is more difficult to see. However, the condition is satisfied, if the loop gain complies to condition 2 and the phase of the loop gain at DC is $0°$ or $-90°$ [4].

Figure 3.3 shows a typical bode plot of a regulator's loop gain. It can be seen, that all the prerequisites for the simplified Nyquist criterion are fulfilled. The stability is determined by observing the point, where the magnitude of $\beta \cdot L(j\omega_c)$ becomes unity. This frequency is called the transition frequency ω_c [rad] or unity gain frequency (UGF) [Hz]. The phase ϕ_c at this frequency is used to calculate the phase margin (PM) with formula 3.8. It is a measure for the stability of the system. The system is stable, if the PM is positive.

$$PM = 180° + \phi_c \tag{3.8}$$

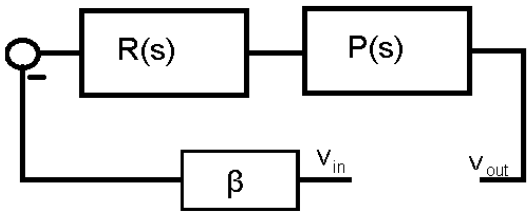

Figure 3.4: Configuration for measuring the Bode plot of the loop gain.

With this method, the stability of the regulator can be checked very easily doing an AC simulation. Keeping $r(s)$ constant and using the model in figure 3.4, a Bode plot of $\frac{v_{out}}{v_{in}}$ can be generated. The PM can be determined directly from this plot, as $\frac{v_{out}}{v_{in}} = -\beta \cdot L(j\omega)$. It should be noted, that a smaller feedback factor β will improve the PM, as the magnitude of $\beta \cdot L(j\omega)$ is shifted down and thus, ω_c moves closer to the origin [25].

The PM has a dominant influence on the settling behavior of the output signal $y(s)$, when applying a step on the input $r(s)$. The step response of systems with small PM (below 45°) will typically show excessive ringing on the output. Systems with high PM (above 80°) will typically exhibit a slow and creeping settling behavior. For systems with dominant pole pair[1] the maximum amplitude of the ringing (R_p expressed in percent of the overall step) can be estimated by a simple rule of thumb[4]: $R_p \approx 70 - PM$.

The transition frequency ω_c is a measure for the speed of the system. For instance, ω_c has an impact on the rise time t_r of a step response. The rise time (t_r in seconds) for a unity step on the input can be approximated by another rule of thumb[4]: $t_r = \frac{1.5}{\omega_c}$.

The absolute value of the loop gain for DC (or low frequencies) A_0 has a major impact on the accuracy of the regulation. Using the transfer function, the DC gain from input $r(0)$ to the output $y(0)$ is $\frac{L(0)}{1+\beta \cdot L(0)}$ (assuming the loop gain has no pole at 0: it has no integral action). If the DC gain is very high compared to β, this expression can be simplified to $\frac{1}{\beta}$. β models the voltage divider, which can be designed to stay nearly constant under all circumstances. Thus, the DC gain and therefore the output voltage can be defined only by the feedback network. The accuracy of this defined gain is determined by the size of A_0.

Using the above stated relations, the loop gain can be designed to fit a specific application. The regulation speed, the settling behavior and the regulation accuracy

[1] This means that one pole (pair) dominates the frequency behavior of the transfer function for frequencies below the transition frequency.

of a specific regulation system can be estimated by simply observing the Bode plot of the loop gain.

However, these estimations are only valid for small signals. For large steps sizes, slewing effects and non-linearity caused by shifts in the bias conditions might dominate the regulation characteristics. Especially in the described voltage regulator topology, a step at the input can only occur in conjunction with a change of the supply voltage, causing significant changes in the bias currents. Thus, a careful transient analysis/simulation of the system is necessary as well.

Frequency compensation

It can be seen from formula 3.8, that a system with only one pole is always stable. This is because a pole introduces a phase shift of $-90°$ and a gain reduction of $-20\,\mathrm{dB/decade}$. For systems with multiple poles, compensation measures need to be applied to ensure stability. These measures are usually targeted on making one pole the dominant pole of the system. Thus, moving one pole closer to the origin, to ensure that all other poles are located above ω_c.

Every independent energy storage in the system will typically contribute one pole. For the voltage regulator, the frequency compensation may be done in a way, such that either the pole originating from the output load, or from an internal energy storage becomes the dominant pole. However, the loads (capacitive and resistive) specified for this regulator can vary over several magnitudes, making the pole at the output hard to predict. Thus a pole originating from inside the regulator should be chosen.

Additionally, the zeros of the loop gain should be examined carefully. A zero which is located in the left half-plane (LHP), introduces a phase shift of $90°$ and a gain rise of $20\,\mathrm{dB/decade}$. Such a zero may be used to compensate a pole. A zero located in the right half-plane (RHP), introduces a phase shift of $-90°$ and a gain rise of $20\,\mathrm{dB/decade}$. A RHP zero may significantly deteriorate the stability, as it may move the UGF away from the origin (which decreases the PM in a multipole system) and additionally introduces negative phase shift. It has to be considered, that this negative phase shift starts to have an effect at $\frac{1}{10}$ of the zero frequency. Even a RHP zero located far away from the UGF may reduce the PM [25].

The compensation can be done using the well known *Miller Compensation scheme* [1, 25]. The pole originating from the output should be chosen as first non-dominant pole. The Miller capacitor C_C is then placed between the output of the error amplifier and the regulator's output. This compensation scheme moves the dominant pole

closer to the origin and the non-dominant pole further away. This behavior is called *pole splitting*. The UGF of the regulation loop can than be given by:

$$UGF = \frac{\beta \cdot g_{m_{EA}}}{2\pi \cdot C_C} \quad , \tag{3.9}$$

where $g_{m_{EA}}$ is the transconductance of the error amplifier (which is an OTA in the simplest case). For a large load capacitor (C_L is much larger than any internal capacitor and the Miller compensation capacitor) the output pole frequency f_{pout} after Miller compensation can be approximated with formula 3.10 [25], where g_{mout} is the transconductance of the PMOS pass element.

$$f_{pout} \approx \frac{g_{m_{out}}}{2\pi \cdot C_L} \tag{3.10}$$

However, Miller compensation also forms a right half-plane (RHP) zero in the loop gain. This zero locates at:

$$\omega_z \approx \frac{g_{m_{out}}}{C_C} \tag{3.11}$$

There are different ways to deal with this zero. C_C could be chosen much smaller than C_L, moving the zero to high frequencies. Another approach commonly used is to place a resistor R_z in series with C_C [25]. The zero is then modified to:

$$\omega_z \approx \frac{1}{C_C \cdot (g_{m_{out}}^{-1} - R_z)} \tag{3.12}$$

If R_z is chosen higher than $g_{m_{out}}^{-1}$, the zero moves to the left half-plane. R_z may even be chosen such that the zero compensates the output pole (which is the first non-dominant pole). Using formula 3.10 and 3.12 this happens when:

$$R_z \approx \frac{C_L}{g_{m_{out}} \cdot C_C} \tag{3.13}$$

However, such a pole zero compensation may be difficult, as $g_{m_{out}}$ depends on the output current and C_L may vary according to the specifications.

The first non-dominant pole will be closest to origin (making the PM small) for the largest load capacitor ($C_L = 1\,\text{nF}$) and minimal load current ($I_L = 1\,\mu\text{A}$). Assuming the PMOS pass element has a $\frac{g_m}{I_D}$ of 20 as it operates close to weak inversion for such small currents, leads to a non-dominant pole frequency of approximately 3.2 kHz. If this pole is not compensated with a left half-plane zero, then it will define the unity gain frequency.

In LDO design, a LHP zero for compensation is usually inserted into the loop gain, using the electrical series resistance (ESR) of the load capacitor [7, 17]. The resistive

components of the load capacitor can be modeled as a resistor R_{ESR} in series with the (ideal) load capacitor C_L. This resistor creates a LHP zero which is located at [17]:

$$\omega_{z_{ESR}} = -\frac{1}{R_{ESR} \cdot C_L} \tag{3.14}$$

It is also possible to place a distinct resistor in series to the load capacitor, if its ESR is not sufficient. However, considering the specified load capacitors (smaller than 1 nF), a high ESR of several kilo Ohms would be needed, to create an ESR-zero close to the first non dominant pole. This is unacceptable, because such a resistor would completely deteriorate the output transient response.

Assuming a pole-zero compensation is not possible, then the specification of the unity gain frequency $UGF > 5\,\text{kHz}$ (Table 2.1) will lead to a PM of approximately 30°. This is within the PM specification $PM > 15°$.

In order to retain stability over the complete temperature range, the above stated small signal parameters must be observed. The location of the first non dominant pole depends mainly on the load current. As the temperature behavior of the load current cannot be determined, it is assumed, that the first non dominant pole is nearly constant over temperature. This assumption is fairly accurate, if the load current slightly increases with temperature. The UGF should then stay constant over temperature to preserve the adjusted PM. It can be seen from formula 3.9, that the transconductance $g_{m_{EA}}$ of the error amplifier must be temperature compensated, as the Miller capacitor C_C will not exhibit a high temperature coefficient. Generally, the error amplifier is realized as an OTA topology. In that case, the transconductance is defined by the OTA's input differential pair. As stated above, the transistors in this design will operate in weak inversion. To obtain a constant transconductance, these transistors must be biased with a PTAT current proportional to $n \cdot V_T$.

3.2.3 PMOS pass element

The voltage at the output is controlled via a PMOS pass element. Together with the load impedance it forms a common source stage. This transistor must be designed such that it can provide the maximum load current at all supply voltages. It might be difficult to size the transistor, such that it stays in saturation at worst conditions (high current, low input voltage, high output voltage, slow transistors, high temperature). A very large transistor will be needed, which will occupy a lot of area, have high leakage currents and introduce large capacitance to the circuit. Thus, the pass element should be permitted to go into triode region, allowing a small transistor size. However, the transistor should be sized, such that the loop gain stays sufficiently high for regulation accuracy. Additionally, when using a pass transistor with small aspect ratio, it should

be checked that the output swing of the error amplifier is high enough to provide the needed gate voltage of the pass transistor.

3.2.4 PSRR

Power supply ripple rejection (PSRR)[28] is a measure of the capability of a regulator to shield the output voltage from ripples on the input voltage. It is a function of frequency and must be evaluated over all possible input frequencies. The PSRR of a linear regulator can be calculated using formula 3.15. Good PSRR behavior is signaled by high negative numbers [28].

$$PSRR = 20 \cdot log\left(\frac{V_{RippleInput}}{V_{RippleOutput}}\right) \tag{3.15}$$

Different publications [10, 11, 21] suggest, that the PSRR of a linear regulator (as described in chapter 2.2) has a close relationship to its loop gain. A qualitative first order approximation of the PSRR can be done by calculating the inverse of the open-loop gain. Figure 3.5 shows a typical PSRR plot of a linear regulator and its loop gain.

At very low frequencies (region I), PSRR will be good, as the regulation suppresses ripples on the output. In this frequency range, the PSRR is dominated from supply noise which couples to the reference voltage input of the regulation loop. The voltage reference should be shielded as well as possible from noise of these frequencies. Above the dominant pole of the loop gain, the gain decreases causing the PSRR to increases (region II). It will then reach a maximum around the unity gain frequency (UGF), as the regulation is not fast enough to suppress these ripples. For even higher frequencies (region III) PSRR will decrease again, because capacitive loads at the output of the regulator will start to short these signals to ground [10, 21].Thus a regulator with good PSRR over a large frequency range needs high loop gain at DC and a high UGF [28].

It should be noted here, that in the condition where the output PMOS pass element is operated in linear region, its transconductance decreases. This causes the loop gain to decrease and thus, the PSRR is degraded.

Additionally the conductance from the supply V_{DD} to the output V_{out} through the error amplifier (see figure 2.1) needs to be considered [10]. When using a linear regulator with a PMOS pass element, ripples on the supply line will appear on the source terminal of the PMOS transistor. To achieve high PSRR, the gate of this

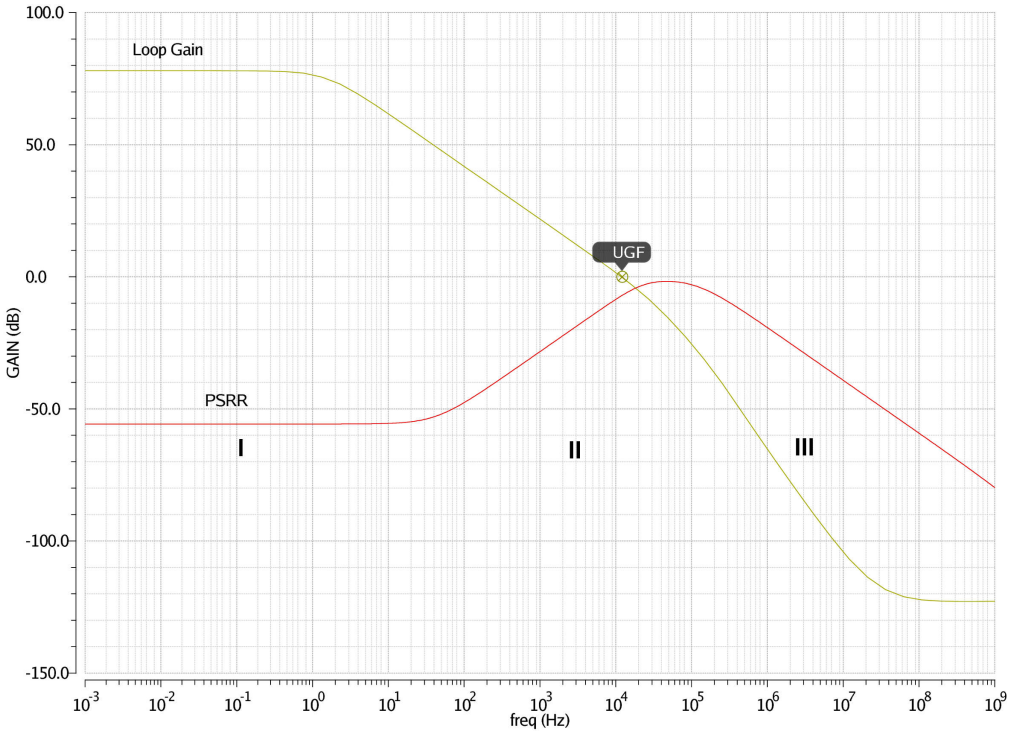

Figure 3.5: Relationship between loop gain and PSRR.

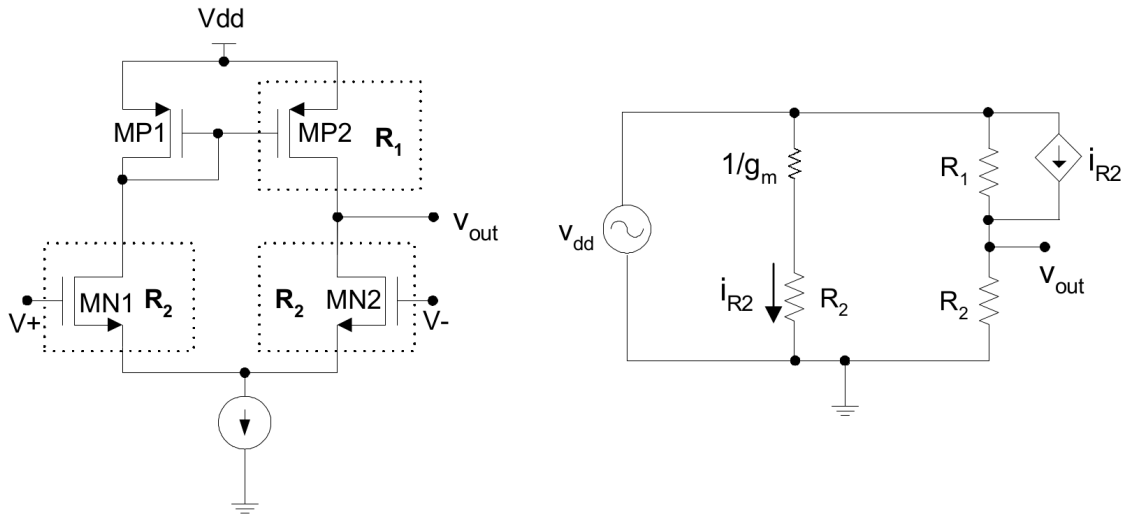

Figure 3.6: OTA model presented by Gupta, Rincon-Mora, and Raha [10].

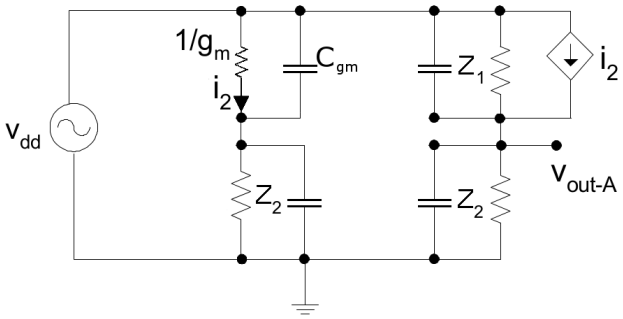

Figure 3.7: Extended OTA model, derived from Gupta, Rincon-Mora, and Raha [10].

transistor needs to be fed with a correlated ripple of the same magnitude to cancel the effect [10].

Gupta, Rincon-Mora, and Raha [10] have presented a PSRR model for an OTA with PMOS current mirror load, as shown in figure 3.6. R_1 and R_2 present the output resistances of the transistors, the current source i_{R2} models the current flowing through $MP1$ copied to $MP2$. It is assumed that $\frac{1}{g_m}$ is much smaller than R_2, thus $i_{R2} \approx \frac{V_{DD}}{R_2}$. Then, it can be shown that the supply ripple of V_{DD} entirely appears at the output of the OTA (formula 3.16)[10].

$$V_{out} = V_{DD}\frac{R_2}{R_1 + R_2} + \frac{V_{DD}}{R_2} \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} = V_{DD} \tag{3.16}$$

According to formula 3.16 a transconductance amplifier with PMOS current mirror load is suitable to to be used as error amplifier together with a PMOS pass element: The supply ripples on the source of the PMOS transistor are canceled with ripples at the gate coming from the output of the OTA. Thus, a common mode voltage is applied at gate and source. The PMOS which operates as common source stage, will not alter its drain current. However, when the OTA is biased with very low currents (below $100nA$), output resistances and the $\frac{1}{g_m}$ resistance become very high. At moderate frequencies the parasitic device capacitance will form low impedance paths, which are in a comparable magnitude and parallel to these resistances. Therefore, the above cited model was extended with capacitors, which model the according parasitic device capacitance. Figure 3.7 shows the extended model. The current i_2 which is mirrored to the current source can be calculated with formula 3.17.

$$i_2 = \frac{V_{DD}}{Z_2 + (\frac{1}{g_m} || \frac{1}{s \cdot C_{gm}})} \cdot \frac{\frac{1}{s \cdot C_{gm}}}{\frac{1}{g_m} + \frac{1}{s \cdot C_{gm}}} = \frac{V_{DD}}{Z_2 + \frac{1}{g_m + s \cdot C_{gm}}} \cdot \frac{g_m}{g_m + s \cdot C_{gm}} \tag{3.17}$$

Using formula 3.17 the output voltage can be calculated with formula 3.18.

$$V_{out} = V_{DD}\frac{Z_2}{Z_1+Z_2} + \frac{V_{DD}}{Z_2+\frac{1}{g_m+s\cdot C_{gm}}}\cdot\frac{g_m}{g_m+s\cdot C_{gm}}\cdot\frac{Z_1\cdot Z_2}{Z_1+Z_2}$$
$$Z_2 \gg \frac{1}{g_m+s\cdot C_{gm}}: \qquad V_{out} = V_{DD}\cdot\frac{Z_2+\frac{g_m}{g_m+s\cdot C_{gm}}\cdot Z_1}{Z_1+Z_2} \tag{3.18}$$

Formula 3.18 shows that for high frequencies, the output of the OTA no longer reflects the supply ripple. The output signal decreases. Thus a differential gate source voltage appears at the PMOS pass element. This voltage is then amplified to the output of the regulator via the transconductance of the pass element and the output resistance. As the output resistance of the regulator is high for high frequencies (above UGF), this behavior will significantly degrade the PSRR performance (gains higher than 1 have been detected in simulations) above UGF. The circuit designer can only increase the transconductance of the current mirror and minimize the area of the mirror transistors to decrease the parasitic capacitance. These measures are both contradictory to matching considerations [1, 23].

However, the above described degradation can be avoided using the simple "Miller Compensation" scheme [25], where a large capacitor is added between the gate and the drain of the PMOS pass element. In that case the PMOS pass transistor will form a MOS diode for high frequencies. Thus, a simple voltage divider circuit is formed for high frequency ripples. The voltage divider consists of a $\frac{1}{g_m}$ resistance (PMOS pass element) between V_{DD} and V_{out} and the load resistance parallel to the feedback network between V_{out} and ground. It this case the PSRR can not exceed 0 dB.

3.2.5 Verification

The specifications in chapter 2.1 can be verified with a small number of tests. All tests should be done with different combinations of supply voltages, load currents, load capacitors and temperatures. However, to keep the number of tests small, it is a general practice to test only corners of specified ranges. Still, if only the maximum and minimum values of the specified operation ranges are tested, there are 16 operating points to test.

The output current can be adjusted/sunk using different methods: Using an ideal current source, a current source with a finite output resistance and with a linear resistor. The differential resistance of the circuits which will load the regulator is

unknown. Thus it was decided to do all simulations and transient measurements with ohmic loads.

The voltage spike specifications need transient measurements. The voltage spikes may occur due to fast changes of the supply voltage and due to fast load changes. In order to test for input caused voltage spikes, a voltage test pattern should be applied to the supply pin of the regulator. It is assumed, that faster rising edges of the input voltage cause higher overshoot at the output. The fastest rising edges of the supply voltage may occur during ESD events. Additionally, overshoot on the output may depend on the charging condition of internal capacitors. The overshoot may be different for a circuit that has not been powered for a long time than for a circuit, where all internal capacitors are charged to a specific value. The test pattern should therefore contain phases, where the internal nodes can discharge to a specific level.

The specifications of the regulation loop can only be verified on the simulator. It should be done as described in section 3.2.2, creating a Bode plot of the loop gain. The operating points, where minimum PM is detected in simulations, may than be tested in laboratory with transient measurements.

A basic method [24] to measure the PSRR is to add an AC voltage to the DC supply voltage and apply it to the supply pin of the regulator. The frequency of the AC signal is varied and the AC voltage at the output is measured. The ratio of the AC output voltage to the AC input voltage is then plotted over frequency.

Additionally, voltage regulators are generally characterized by the following parameters [3], not listed in the specifications from chapter 2.1:

Load regulation specifies the maximum change in output voltage at different load currents. The test is done for minimum supply voltage. The output voltage at minimum and maximum load current is measured. The output voltage difference ΔV is then normed by the output current difference ΔI:

$$load\ regulation = \frac{\Delta V}{\Delta I}|_{V_{DD_{min}},\ \Delta I_{max}} \tag{3.19}$$

Line regulation specifies the maximum change in output voltage at different supply voltages. The test is done at the maximum load current. The output voltage at minimum and maximum supply voltage is measured. The output voltage difference ΔV is then normed by the input voltage difference ΔV_{DD}:

$$line\ regulation = \frac{\Delta V}{\Delta V_{DD}}|_{I_{max},\ \Delta V_{DD_{max}}} \tag{3.20}$$

These two parameters shall be measured as well, to classify the performance of the STUP in comparison to standard voltage regulators.

4 Current reference

4.1 Circuit description

As mentioned before a simple current reference circuit as described by Razavi [25, p. 379] was used. This circuit offers a basic, low accuracy, bias generation without the need for bipolar transistors. A basic schematic diagram can be seen in Figure 4.1.

4.1.1 Principle of operation

The circuit is sometimes called *beta multiplier* [1, 2]. This is because the aspect ratio of $M1$ needs to be m times higher than $M2$, thus its transconductance parameter $\beta_1 = m \cdot \beta_2 = m \cdot \beta$. A typical drain current I_D vs. gate Voltage V_G plot of $M1$ and $M2$ can be seen in Figure 4.2. It can be observed that at low V_G the drain current of $M1$ is approximately m times higher than $M2$. The source resistor R of $M1$ provides negative current feedback, causing I_D of $M1$ to flatten out at higher V_G. Thus at a certain V_G the drain currents of both transistors are equal. The circuit is forced to remain at this special operating point ($I_{D1} = I_{D2} = I_{Ref}$) via the current mirror $MP1$, $MP2$. However, there is a second stable operating point, where $I_{D1} = I_{D2} = 0$. A proper start-up circuit is needed to ensure, that this degenerated operating point is avoided.

The circuit can be used with $M1$ and $M2$ operating in strong or weak inversion. Using the simple square-law model [12, 25], the reference current I_{Ref}, when operating in strong inversion can be calculated by formula 4.1 [25]. Channel-length modulation and body-effect are neglected for simplicity.

$$I_{Ref} = \frac{2}{R^2 \cdot \beta_2} \left(1 - \frac{1}{\sqrt{m}}\right)^2 \tag{4.1}$$

It can be shown that the transconductance g_m of the transistors $M1$ and $M2$ is only dependent on the resistor R and multiplication factor m:

$$\left[\frac{2}{R}\left(1 - \frac{1}{\sqrt{m}}\right)\right] = \sqrt{2\beta_2 I_{Ref}} = g_{m2} = \frac{g_{m1}}{\sqrt{m}} \tag{4.2}$$

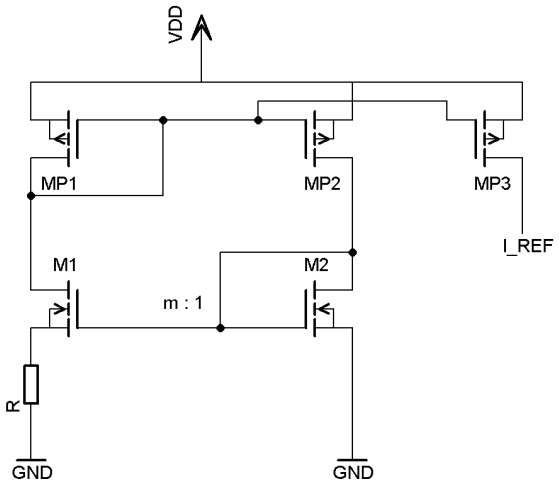

Figure 4.1: Schematic diagram of the bias circuit.

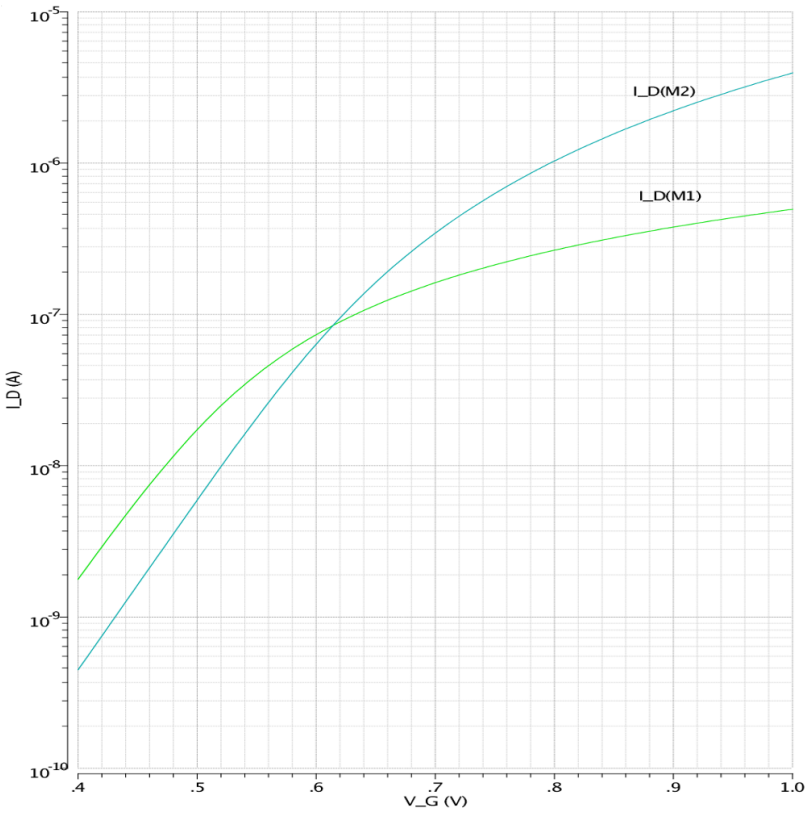

Figure 4.2: Drain current plotted versus gate voltage of M1 and M2.

The reference current for weak inversion operation is calculated using the simple exponential model from chapter 3.1. From formula 3.1 the reference current can be derived. It is given by formula 4.3.

$$I_{Ref} = \frac{n \cdot V_T}{R} ln\,(m) \tag{4.3}$$

Again, using formula 3.2 it can be shown that the g_m of $M1$ and $M2$ is determined by R and m (formula 4.4).

$$\frac{ln\,(m)}{R} = \frac{I_{Ref}}{n \cdot V_T} = g_{m2} = g_{m1} \tag{4.4}$$

Comparing the two operation modes (formula 4.1 and formula 4.3) and assuming the temperature dependence of R can be neglected[1], leads to following observations:

- In strong inversion operation, I_{Ref} has a larger dependence on R.
- I_{Ref} shows a PTAT behavior. However, in weak inversion operation, it has a larger temperature dependence. This is because V_T usually exhibits a larger temperature dependence than $\frac{1}{\beta}$.

It was decided to design the reference circuit to work in weak inversion. The value of the resistor R has high process variations [22]. Weak inversion operation will improve the precision of I_{Ref}. In weak inversion the desired temperature behavior is observed: $I_{Ref} \propto V_T$.

It can be shown, that biasing a transistor in weak inversion with the reference current of the beta multiplier operated at weak inversion will lead to a constant g_m: $g_m = \frac{I_D}{nV_T} = \frac{I_{Ref}}{n \cdot V_T} = \frac{ln(m)}{R}$.

4.1.2 Stability of regulation

The circuit works as a positive feedback system [1], with additional negative feedback provided by the resistor. The regulation remains stable, as long as the loop gain is smaller than 1 (at all frequencies). It can be shown that the maximum loop gain occurs at DC. Thus calculating the DC loop gain will be sufficient to evaluate the stability of the regulation loop.

In order to calculate the loop gain, the regulation loop was opened at the gate connection of $M1$ and $M2$. Figure 4.3 shows a simple small signal equivalent circuit.

[1] The temperature coefficient of the used n+POLY resistor [22] is approximately $-640 ppm/K$.

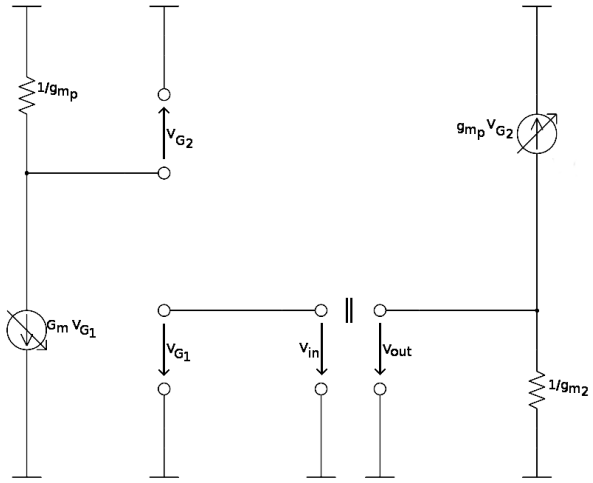

Figure 4.3: Small signal equivalent circuit of the beta multiplier.

Output resistances of the transistors are assumed very high and are therefore neglected. The transconductance G_m of a source degenerated transistor is approximately $G_m \approx \frac{g_m}{1+R(g_m+g_{mb})}$ [25], where g_m and g_{mb} are the transconductance and back-gate transconductance, respectively. The DC loop gain A_{Vloop} can then be calculated with formula 4.5.

$$A_{Vloop} = \frac{V_{out}}{V_{in}} = \frac{-G_m}{g_{mp}} \cdot \frac{-g_{mp}}{g_{m2}} = \frac{G_m}{g_{m2}} = \frac{g_{m1}}{g_{m2}} \cdot \frac{1}{1 + R(g_{m1} + g_{mb1})} \tag{4.5}$$

When implying weak inversion operation (as determined in 4.1.1: $g_{m1} = g_{m2}$), formula 4.4 can be used to simplify the expression. Neglecting body effect, A_{Vloop} is approximately given by formula 4.6.

$$A_{Vloop} \approx \frac{g_{m1}}{g_{m2}} \cdot \frac{1}{1 + R \cdot g_{m1}} = \frac{1}{1 + R \cdot \frac{ln(m)}{R}} = \frac{1}{1 + ln(m)} \tag{4.6}$$

This simple approximation shows clearly, that increasing the multiplication factor m decreases the loop gain and therefore improves the stability of the regulation. However, the loop gain will approach a minimum value, above a certain value of m. This result can also be evaluated from another point of view: A higher multiplication factor, will lead to a sharper intersection point of the drain currents of $M1$ and $M2$ (see figure 4.2) and thus to a more distinct operating point. At higher values of m, the intersection will approach 90°.

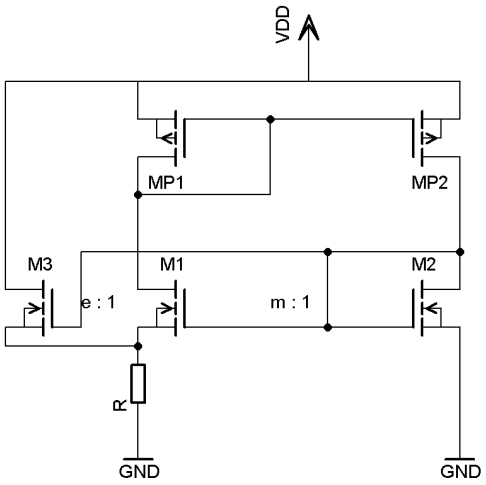

Figure 4.4: Schematic diagram of the beta multiplier circuit with bypass transistor.

4.1.3 Resistor area reduction

The circuit requires a large resistor R (several hundred kilo ohms). This resistor will typically occupy a large die area. In order to reduce the resistor area a bypass transistor $M3$ was added. Figure 4.4 shows the schematic. The bypass transistor has an aspect ratio e times higher than $M1$. Thus by sacrificing some current ($e \cdot I_{Ref}$), the resistor is decreased by a factor $1 + e$.

It is assumed, that the output resistance of $M3$ is very high. In this case, adding the transistor $M3$ and reducing the resistor R does not affect the circuit performance, because the voltage drop over the resistor does not change.

4.1.4 Start-up circuit

It was already stated in 4.1.1, that the beta multiplier circuit needs a start-up circuitry. Different circuits are published [1, 2, 25]. A solution similar to the one described by Baker, Li, and Boyce [1] was chosen.

Figure 4.5 shows a basic schematic diagram of the start-up circuit. The major difference to the original circuit [1] is the gate connection of MPS. Instead of connecting it to the gate of MNS (making MNS and MPS form a standard CMOS inverter function) it was connected to ground via a pull-down resistor. The potential of V_{Start} needs to be high when $I_{Ref} = 0$ in order to pull down the gates of $MP1$ and $MP2$. This causes a high current to flow through $M1$ and $M2$ and thus making $I_{Ref} = 0$ an unstable operating point. On the other hand, V_{Start} needs to be low, when I_{Ref} has settled

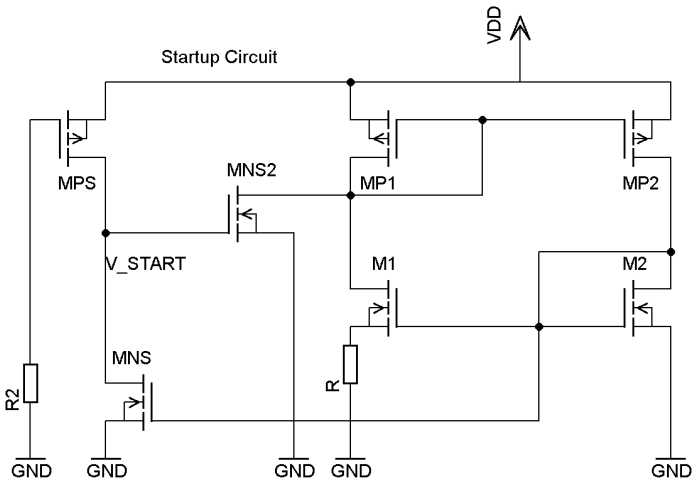

Figure 4.5: Schematic diagram of bias start-up circuit.

in order not to disturb the circuit at normal operation. The control voltage for the inverter-like structure is derived from the gate of $M2$. As determined in 4.1.1, $M2$ will operate in weak inversion. Thus the inverter structure needs to switch V_{Start} from high to low at about 300 mV. This can only be achieved with MPS being very long and narrow (having a very small aspect ratio). As the minimum channel length of the used transistors is limited to 322 nm, this leads to a large transistor (with a large gate source capacitance). If the gate of MPS is connected to the gate of MNS (as suggested by [1]) this parasitic capacitance would form a low impedance path (even for moderate frequencies) from the supply V_{DD} to the gate of $M2$, leading to inferior power supply ripple rejection (PSRR) performance. This is avoided by pulling the gate of MPS down via a resistor. However, this leads to increased current consumption, as the gate of MPS is permanently tied to the lowest possible potential.

4.2 Circuit dimensioning

The starting point of the design was an already existing beta-multiplier circuit. The existing circuit was designed to work in weak inversion and provided a reference current of approximately 84 nA at 27 °C. From this starting point, the circuit design was modified to reduce current consumption and die area. A bias current I_{Ref} of 80 nA was determined.

The current mirror transistors $MP1$-$MP2$ were designed long and narrow for mismatch and output resistance reasons [1]. The aspect ratio of $M2$ was designed such that the the transistor will operate in weak inversion for the given current, while

keeping the aspect ratio as small as possible to minimize mismatch. The length was chosen, such that the output resistance becomes high which is important for PSRR [25, p. 379].

The multiplication factor m was chosen 4. This was considered sufficient from the point of stability, while the size of $M1$ is kept sufficiently small. Using formula 4.6 a DC loop gain of approximately 0.42 can be calculated. Simulations revealed a DC loop gain of 0.48.

The resistor area reduction method was implemented as described above. The multiplication factor e for the bypass transistor was chosen 1. This was considered the best compromise between area reduction and current consumption. Then the value of the resistor R was determined by simulation sweep, because the slope factor n (formula 4.3) was unknown for the used process.

The start-up transistor MPS (which is always on) of the start-up circuit was sized longer and narrower as in the existing circuit, to reduce the current consumption. Some capacitors were added to improve the start-up behavior.

Additional measures were implemented to shut down the circuit via a power-down signal (marked with pd in the schematic).

Figure 4.6 shows the full schematic of the bias circuit with transistor sizes.

4.3 Simulation

Simulations were done with a $MOS11010$ 160 nm CMOS model from NXP Semiconductors. All following simulations were done for 3 supply voltages (1.8 V, 2.7 V and 3.6 V), 3 temperatures (−40 °C, 27 °C and 150 °C) and 5 corner transistor models provided by the foundry (nominal, snsp (considering slow transistors), fnfp (considering fast transistors), fast (considering fast transistors and small resistors) and slow (considering slow transistors and large resistors)).

4.3.1 Temperature behavior

The temperature behavior was simulated using a DC simulation sweeping over the temperature. Figure 4.7 shows a typical temperature plot of the bias current I_{Ref}. The PTAT behavior predicted by formula 4.3 can be observed.

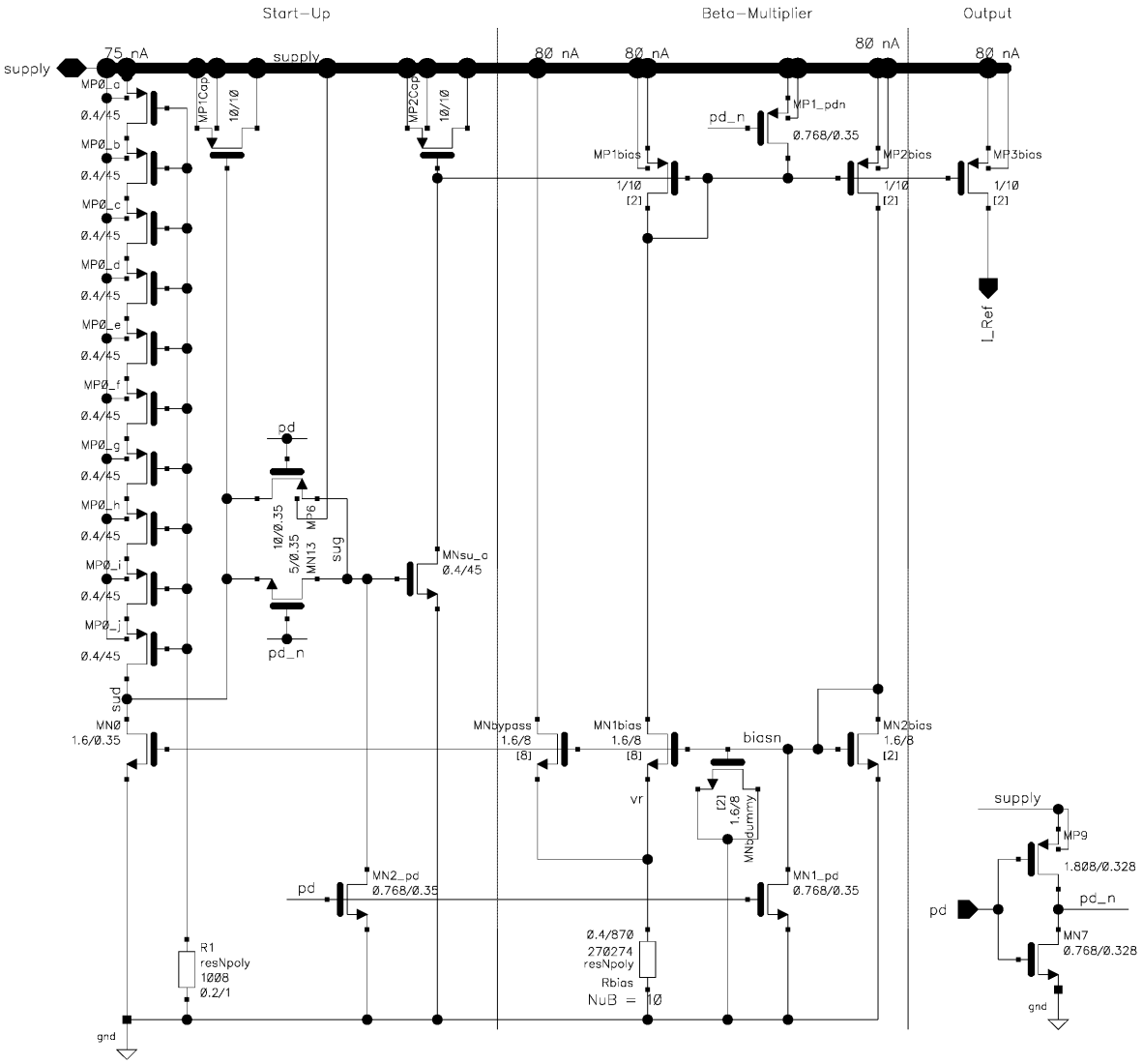

Figure 4.6: Schematic of the bias circuit.

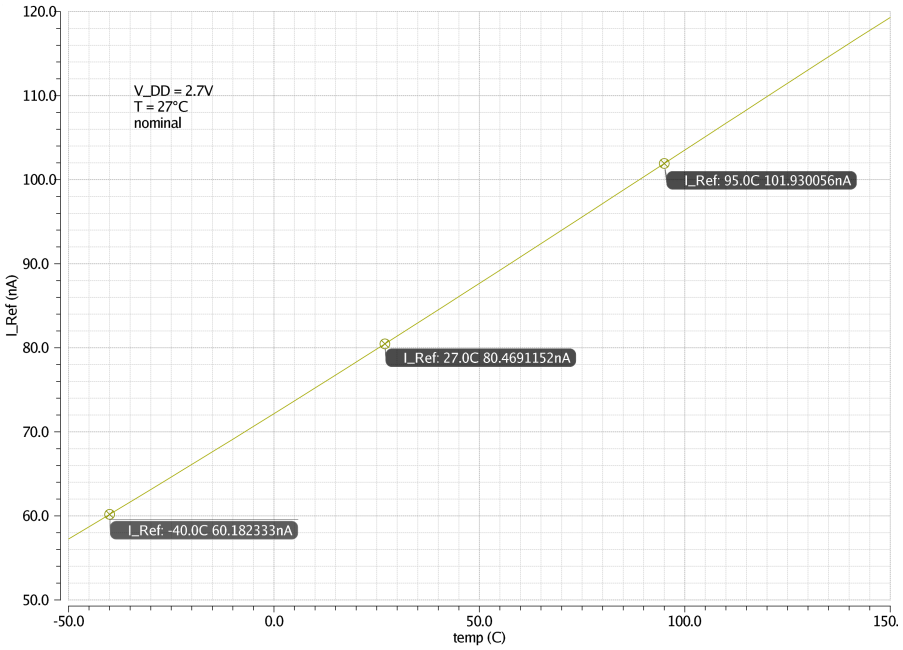

Figure 4.7: Temperature plot of the bias current.

4.3.2 Start-up behavior

The start-up behavior was simulated using transient simulations. The rise time t_{sup} of the supply voltage V_{DD} was systematically varied from 1 ns to 100 ms. This was done to ensure that the circuit properly starts operation at different slopes of the supply voltage. Figure 4.8 shows a typical start-up plot of the bias current I_{Ref} versus time for a supply rise time of 1 µs. The reference current at nominal conditions and at minimum and maximum corner conditions are shown. It can be seen that the start-up circuit forces a high current through the transistors at the beginning. The regulation loop then sets the current at the desired value.

Simulations show, that the circuit starts up at all different corner conditions. For fast supply rise times up to 1 µs the bias current settles at the desired value within 10 µs. For slower rise times above 100 µs the circuit works as expected as soon as the supply voltage reaches about 1.2 V. This is well below the minimum specified V_{DD} value of 1.8 V.

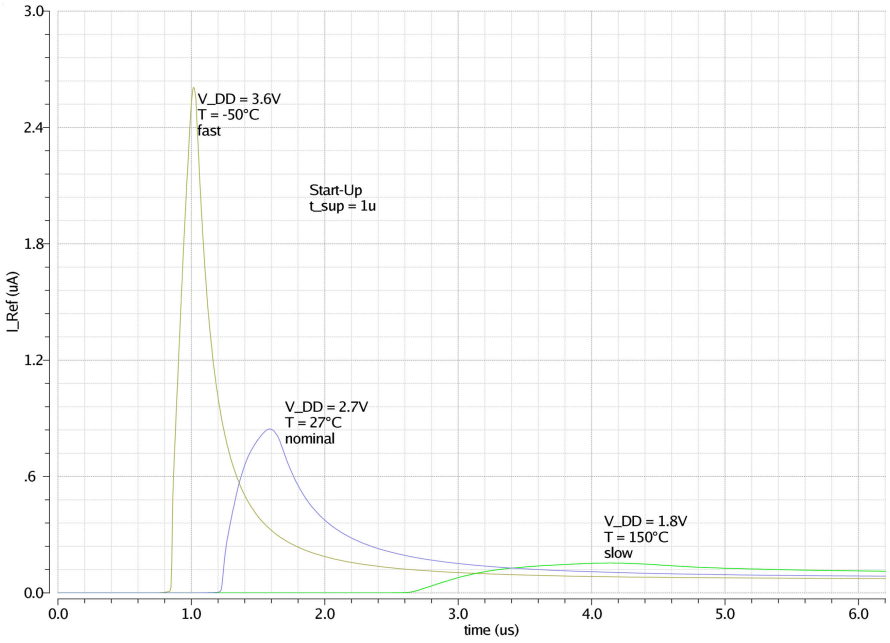

Figure 4.8: Start-up of the bias circuit.

4.3.3 Stability

The stability of the circuit was evaluated by simulating the loop gain of the regulation loop (see section 4.1.2). Figure 4.9 shows a plot of the loop gain under typical conditions. As assumed before, the maximum loop gain is at low frequencies. The DC-value is close to the value approximated by formula 4.6. Simulation results are nearly identical for all corners.

4.3.4 Power supply dependance

The reference circuit's dependence on the supply voltage level was tested using a DC simulation. The bias current at minimum supply voltage $V_{DD} = 1.8\,\mathrm{V}$ and at maximum supply $V_{DD} = 3.6\,\mathrm{V}$ voltage was simulated over temperature. The difference of these values $\Delta I = I_{Ref_{3.6}} - I_{Ref_{1.8}}$ was then normalized by the reference current at the typical supply voltage $V_{DD} = 2.7\,\mathrm{V}$. This normalized error $\frac{\Delta I}{I_{Ref}}$ over the complete supply range is 1.65 % for nominal transistors at 27 °C and smaller than 2 % for all corners over the complete temperature range.

The bias current's dependance on supply voltage ripples was simulated using an AC simulation. The transconductance g_{vdd} from V_{DD} to I_{Ref} was evaluated. Figure 4.10

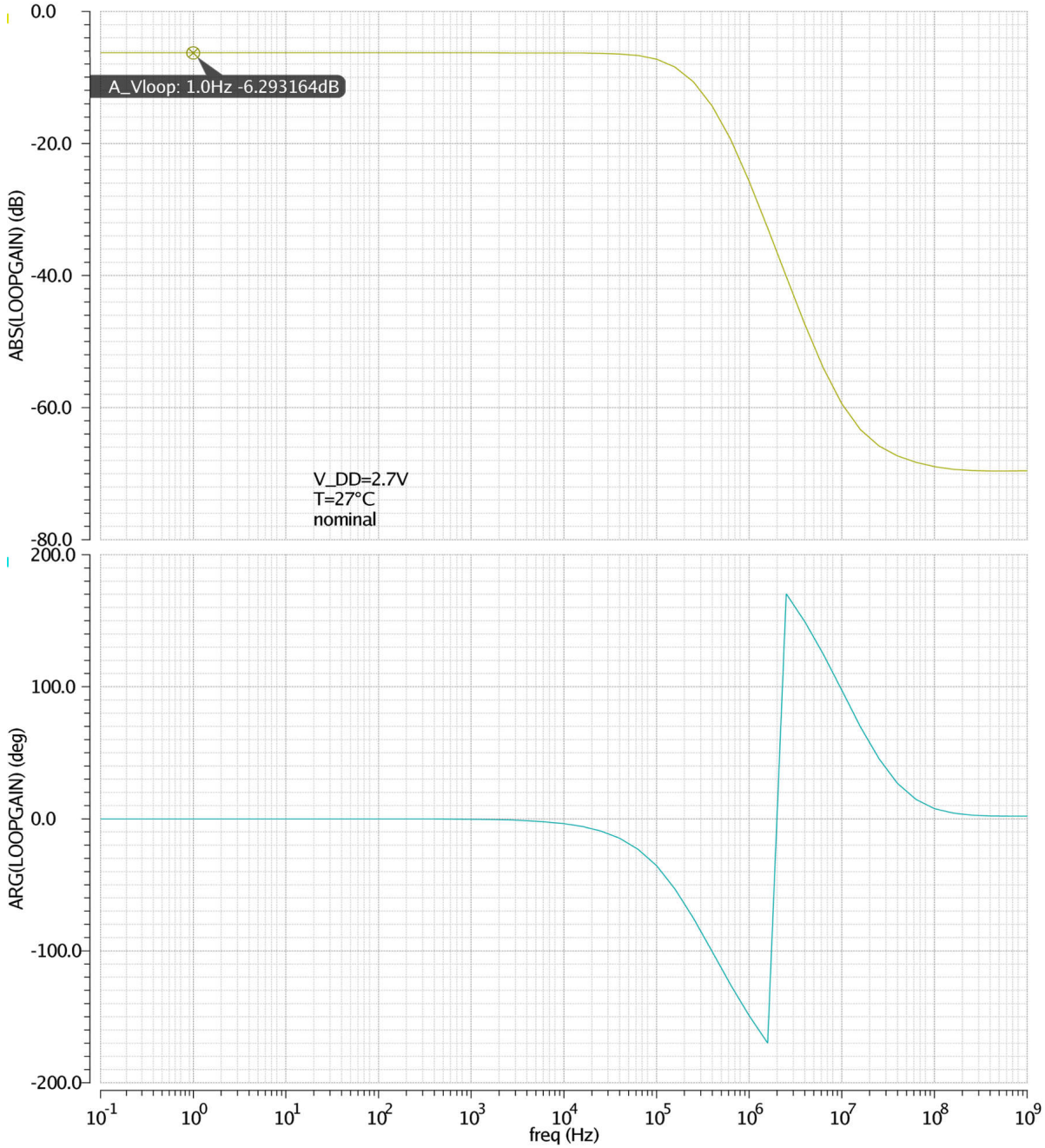

Figure 4.9: Loop gain of the bias regulation.

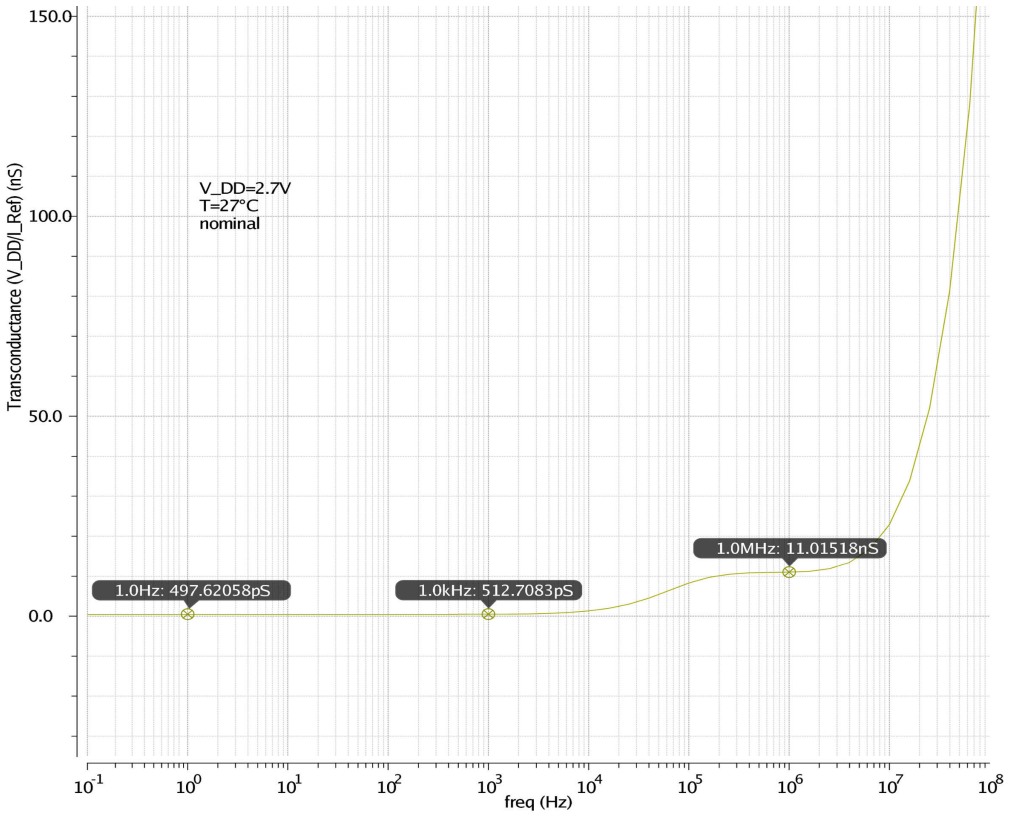

Figure 4.10: Power supply ripple dependance of the bias circuit: Transconductance from V_{DD} to I_{Ref}.

shows a plot of g_{vdd}. At low frequencies power supply changes have very small impact on the bias current I_{Ref}. However, at frequencies above 1 MHz the transconductance increases rapidly, leading to a high variation of the bias current. This is due to parasitic capacitance of the transistors [25].

4.3.5 Process variation and mismatch simulation

A Monte-Carlo simulation was used to simulate the impact of process variations and mismatch on the bias current I_{Ref}. The simulation was done for typical conditions ($V_{DD} = 2.7\,\mathrm{V}$, 27 °C, nominal transistors), 500 iterations were performed. The simulation revealed an estimated mean value $\overline{I_{Ref}} = 80.5\,\mathrm{nA}$ and an estimated standard deviation $\sigma = 5.5\,\mathrm{nA}$.

5 Analysis of the existing circuit and improvement

At the beginning of the project, a start-up regulator design was already existing. Figure 5.1 shows the existing schematic of the regulator. The project started with verification of the design on the simulator. However, simulations (as described below) revealed some weaknesses of the design. Thus, the design was analyzed and potential modifications were worked out. This chapter describes the proposed modifications after analysis and shows a comparison of the existing and modified circuit after simulation.

5.1 Circuit description

The circuit is an implementation of the topology described in chapter 2.2. A beta-multiplier bias circuit as described in chapter 4.1 is used. The reference voltage is derived with a NMOS transistor in diode configuration, biased with the beta-multiplier current. A simple OTA [25] with NMOS input is used as error amplifier. The output voltage is fed back using a MOS voltage divider [1]. A simple *Miller compensation* [25] is applied to assure stability.

5.1.1 Bias circuit

The original bias circuit was replaced by the design described and verified in chapter 4.1. The main differences to the original circuit are the use of the resistor area reduction method (as described in 4.1.3), and a modified start-up circuitry. These modifications reduce area consumption and current consumption.

5.1.2 Voltage divider

As described in section 3.2.1, the reference voltage needs to be adapted first according to the used error amplifier. The OTA has an NMOS input stage, thus a high reference

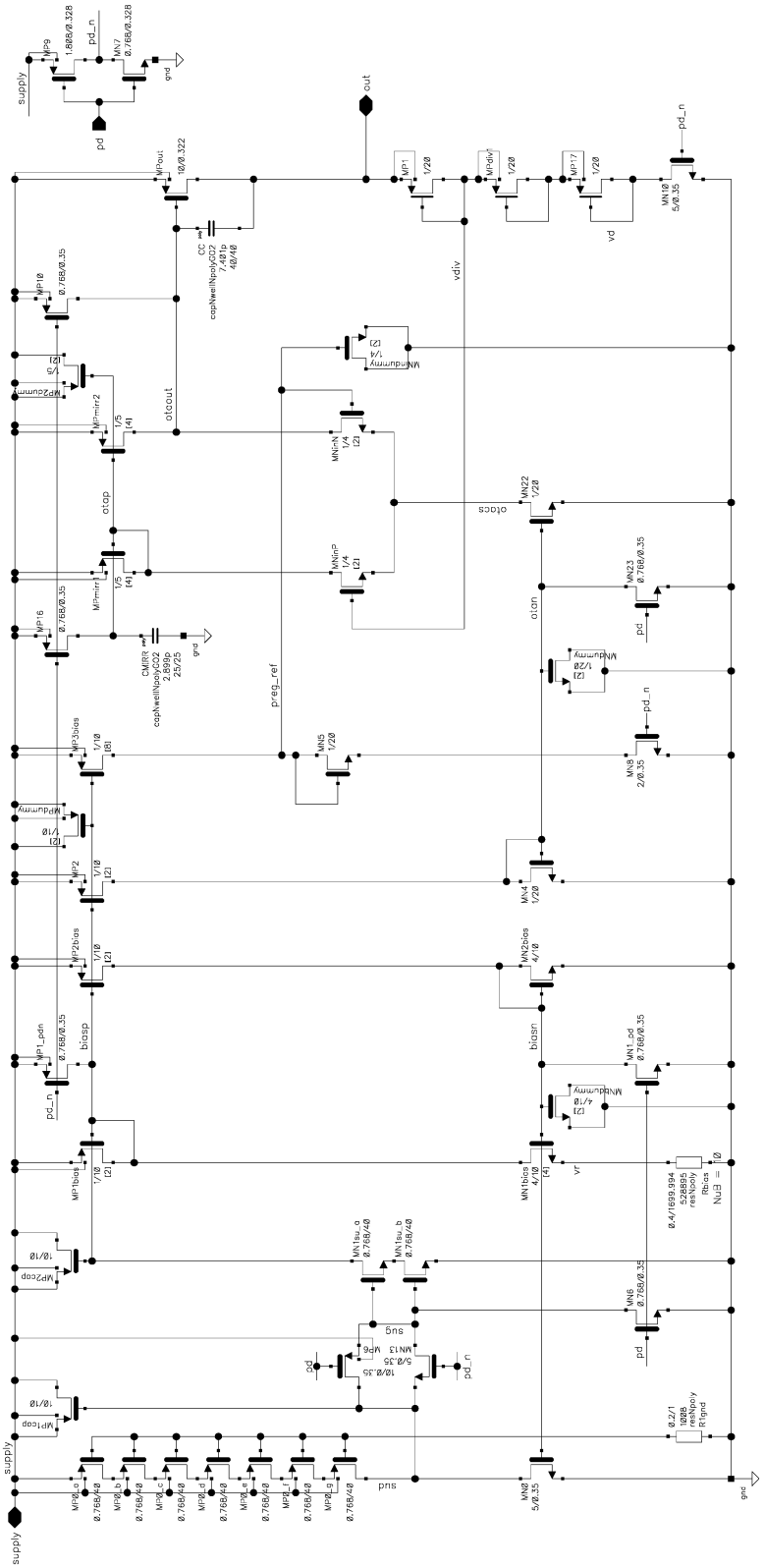

Figure 5.1: Schematic diagram of existing start-up regulator circuit

voltage V_{Ref} should be chosen to guarantee enough voltage headroom for the input stage and the current source. However, the output of the OTA can only swing down to approximately $V_{Ref} - V_{th}$, limiting the maximum gate source voltage of the PMOS pass element to $V_{DD} - V_{Ref} + V_{th}$. Choosing V_{Ref} too high, would require a large PMOS output transistor. A reference voltage of approximately 1 V was chosen in the existing design.

According to this, the voltage division factor is 1.5 ($\beta = \frac{2}{3}$) to obtain the desired output voltage of approximately 1.5 V. The transistors are designed narrow, with a large area to reduce current consumption and mismatch. The voltage divider was not modified.

5.1.3 Reference voltage generation

The reference voltage V_{Ref} is derived from a MOS-diode biased with a multiple d of the reference current I_{Ref}. This reference current was set to approx. 80 nA and a PTAT behavior, as described in chapter 4.2. The needed reference voltage of 1 V is much higher than the threshold voltage of the used transistor. The gate voltage of a MOS-transistor operated at a high overdrive voltage will typically show a PTAT behavior for a given current [1]. This is because at high overdrive voltages the charge carrier's mobility reduction is dominant over the threshold voltage reduction for increasing temperature. At a given current, the gate source voltage of the MOS-diode will increase with temperature. If a diode connected transistor operated at a high overdrive voltage is biased with a PTAT current, then the reference voltage will have a high positive temperature coefficient. Thus using a smaller overdrive voltage should be preferred, to reinforce the influence of the threshold voltage's NTAT behavior. This would stabilize the reference voltage of the regulator.

The reference current may deviate from the expected value of 80 nA due to process variations, mismatch, supply voltage changes and other reasons. Thus, the gate-source voltage of the MOS-diode, biased with a multiple d of the reference current I_{Ref}, will also show deviations from the designed value. Formula 5.1 gives the relation between small changes in the reference current ΔI_{Ref} and resulting changes in the reference voltage ΔV_{Ref}. The value g_m represents the transconductance of the transistor.

$$\Delta V_{REF} = \frac{\Delta I_{Ref} \cdot d}{g_m} \tag{5.1}$$

Using a simple square-law model [12, 25], the expression can be further simplified (formula 5.2). In this expression, $\frac{W}{L}$ and K' represent the aspect ratio of the transistor and a process dependent factor, respectively.

$$\Delta V_{REF} = \frac{\Delta I_{Ref} \cdot d}{g_m} = \frac{\Delta I_{Ref} \cdot d}{\sqrt{2\frac{W}{L} \cdot K' \cdot d \cdot I_{Ref}}} \propto \sqrt{\frac{d}{\frac{W}{L} \cdot K'}} \tag{5.2}$$

Formula 5.2 shows clearly, that in order to decrease variations of the reference voltage due to current variations, a transistor with a high aspect ratio biased with a low current (small d) is favorable. However, as the needed reference voltage is much higher than the threshold voltage, a NMOS-transistor $MN5$ with a low aspect ratio and a high bias current (d =4) was used in the existing circuit (Figure 5.1).

In the used process [22], the PMOS transistors have a smaller K' and a higher threshold voltage in comparison to NMOS transistors. Using a PMOS transistor, less current will be needed to obtain the desired reference voltage of 1 V. Thus a PMOS can be designed to have a similar variation factor $\sqrt{\frac{d}{\frac{W}{L} \cdot K'}}$ as the existing NMOS at a lower overdrive voltage (which is good for temperature stability). This is because d can be reduced and $\frac{W}{L}$ increased (because of the higher threshold voltage) to compensate for the smaller K'. It will reduce the current consumption of the circuit and improve the temperature behavior of the reference voltage without degrading the current variation performance.

By using a PMOS transistor, it was then possible to realize a first order temperature compensation of the reference voltage. The overdrive voltage for the needed reference voltage is so small, that the PTAT reference current is compensated by the NTAT behavior of the transistor's threshold voltage.

5.1.4 Error amplifier and pass element

The error amplifier (see figure 5.1) is realized using a simple OTA with NMOS input and current mirror load. All transistors operate in weak or moderate inversion. The OTA is biased with a current source, which sinks a bias current I_{SS} of 80 nA. The OTA's output is connected to the PMOS pass element, which forms a common source stage with the load impedance. The Miller compensation scheme is applied to convert the pole originating from the output of the OTA into the dominant pole of the loop gain. The GBW (gain bandwidth product) can be approximately given by, where C_C and $g_{m_{in}}$ are the Miller capacitance and the transconductance of an input transistor, respectively:

$$GBW \approx \frac{g_{m_{in}}}{2\pi \cdot C_C} \tag{5.3}$$

It has to be noted that the UGF of the loop gain $\beta \cdot L(j\omega)$ is approximately $\beta \cdot GBW$. Keeping in mind the specifications, the OTA must be designed for a GBW higher than 7.5 kHz.

Simulations showed unacceptably high overshoot of the output voltage, when switching on the supply voltage. This overshoot could not be explained with a linear circuit model. It is caused by the large Miller capacitance required for compensation: When supply is off, the output of the OTA and the output of the regulator are at ground potential. When switching on the supply, the reference voltage of the regulator rises faster than the output voltage (because of the large load capacitance at the output). Because of this, the output of the OTA stays at the lowest possible value to fully open the pass element. As output voltage rises, the OTA output remains at the lowest possible value. Thus, the Miller capacitor is charged, exhibiting a positive voltage from the regulator output to the OTA output. When the output voltage reaches the desired voltage level, the OTA output needs to move to a high voltage to switch off the pass element. In order to do so, the Miller capacitance needs to be charged. However, at this time the capacitance is inversely charged to the desired value. The small bias current needs a long time to provide this charge. In this time, the output voltage rises higher than desired, causing the overshoot.

The capacitance C_{mirr} (see schematic: figure 5.1) was introduced in the existing circuit to improve the overshoot behavior. The capacitance 'senses' a rising of the supply voltage, by forcing a high current through MP_{mirr1}. This high current is mirrored to MP_{mirr2}. Thus the slew rate of the circuit at rising edges of the supply voltage is greatly improved. The size of C_{mirr} is related to the size of the Miller capacitance. Larger Miller capacitance requires larger C_{mirr}. However, the used C_{mirr} is sufficiently large to move the *mirror pole* [1, 25] close to the origin and thus decreases the PM.

The frequency of the mirror pole can be approximated with formula 5.4 [25]. C_m represents the total capacitance at the mirror node and $g_{m_{mirr}}$ the transconductance of the current mirror.

$$f_{p_{mirr}} \approx \frac{g_{m_{mirr}}}{2\pi \cdot C_m} \approx \frac{g_{m_{mirr}}}{2\pi \cdot C_{mirr}} \tag{5.4}$$

Simulations of the existing circuit showed, that neither the overshoot requirements nor the stability requirements were met. Overshoot up to 2.4 V was observed, which is beyond the specifications of 2 V and very close to a possible IC destruction at 2.5 V. At some corners the PM was below 15°. Additionally, a large part of the regulator's die area was occupied only by capacitors. It was the aim of this work to modify the circuit in order to reduce overshoot, improve the stability behavior and minimize on-chip capacitors.

5.1.5 Frequency compensation

Different measures were considered to improve the phase margin. First a pole zero compensation was considered. This was realized adding a series resistor R_z to the Miller capacitor, as described in chapter 3.2.2. Attempts to compensate the second non-dominant pole induced by C_{mirr} were undertaken. Using formula 3.12 and 5.4 the needed resistor can be calculated with

$$R_z = g_{m_{out}}^{-1} + \frac{C_{mirr}}{g_{m_{mirr}} \cdot C_C} \quad , \tag{5.5}$$

where $g_{m_{out}}$ is the transconductance of the output PMOS transistor. The PM will be smallest at minimum possible $g_{m_{out}}$ (from chapter 3.2.2). The resistor was dimensioned for that point. Calculations showed, that a resistor of about 500 kΩ was needed. It can be seen from formula 3.12 that the zero will be nearly independent of the load current, as $R_z \gg g_{m_{out}}^{-1}$. However, such a compensation was not possible to realize, due to several reasons:

- Using the standard n+POLY resistor [22] which was already used in the current reference circuit, would occupy an unacceptably large die area because of its low sheet resistance. The used process offers also a high resistive, nPoly resistor. However, the sheet resistance of this resistor exhibits large production variations and a high temperature coefficient. This characteristic will cause large variations in the zero's frequency.
- Transient simulations showed a negative effect on the overshoot behavior. At rising edges of the supply voltage, C_{mirr} induces a high current flowing into C_C (several µA). This current causes a high voltage drop over R_z, degrading the slew rate.

Next, it was tried to implement the output pole as the dominant pole, without using Miller compensation. This was tried, because the specified load capacitance is quite high compared to the internal capacitance of the OTA. It would completely solve the overshoot problem. The mirror capacitor C_{mirr} could be removed. No compensation capacitance would be needed. The dominant pole would be located at

$$\omega_p = -\frac{1}{C_L \cdot r_{out}} \quad , \tag{5.6}$$

where r_{out} is the differential resistance at the output.

For this compensation scheme, stability will be worst, if ω_p is located at high frequencies (r_{out} and C_L is small). It is not possible to predict r_{out}, as it depends on the small signal resistance of the connected load. Thus, a diode like device connected to the output will deteriorate the stability. However, the calculations and simulations were done using ohmic loads to evaluate the feasibility of this concept.

The calculations showed, that the output pole is located at about 106 kHz in the worst case and 106 Hz in the best case. However, the OTA exhibits a low frequency pole originating from its high impedance output node at about 20 kHz. Therefore, this compensation scheme will not be successful.

The simple Miller compensation scheme is probably the only feasible compensation measure to assure stability in all conditions.

Overshoot reduction

The current mirror load of the OTA is designed to work in weak inversion. However, at rising edges of the supply voltage, C_{mirr} induces a high current through these transistors. In that case, the mirror transistors suddenly operate in strong inversion. In this state, a high aspect ratio of the mirror transistors is favorable, to increase their drain current, which will shorten the time needed to load the Miller capacitance.

Therefore the dimensions of these two transistors were adapted for a high aspect ratio, to improve the overshoot behavior. This was done by shortening the channel length and increasing the width, keeping the area constant. In normal operation, this modification only has minor impact on the circuit: The transistors move deeper into weak inversion. However, their g_m stays nearly constant and thus mismatch will not become significantly worse, as the area of the transistors remains the same (see chapter 3.1). The channel length was chosen three times the minimum length, which ensures sufficient output resistance. So, the gain of the OTA is not degraded.

Area reduction

The area consumption of the regulator is dominated by the Miller capacitor C_C and the mirror capacitor C_{mirr}. As the size of C_{mirr} is linked to the size of C_C, C_C should be as small as possible.

It can bee seen from formula 5.3, that to decrease the Miller capacitance, while keeping the GBW constant, the transconductance of the input differential pair needs to be decreased. This can only be done by reducing the bias current I_{SS} of the OTA.

This measure will not decrease the gain of the OTA (see chapter 3.1): The DC gain A_0 of the OTA is given by:

$$A_0 = g_{m_{in}} \cdot R_{out} \tag{5.7}$$

The transconductance $g_{m_{in}}$ of the input transistors, which operate in weak inversion is proportional to I_{SS}. R_{out} is formed by the parallel connection of the output resistances,

it is roughly proportional to $\frac{1}{I_{SS}}$ (see section 3.1). Thus the gain is independent of I_{SS}.

The slew rate of the regulator is also not affected: Ignoring the overshoot reduction circuit, the slew rate is dominated by the time the OTA current needs to charge C_C and can be given by:

$$\frac{\delta V_{OTAout}}{\delta t} \approx \frac{I_{SS}}{C_C} \tag{5.8}$$

Keeping in mind that the transistors are operated in weak inversion, the expression can be rewritten using formula 5.3:

$$\frac{\delta V_{OTAout}}{\delta t} = \frac{I_{SS} \cdot 2\pi \cdot GBW}{g_{m_{in}}} = 4\pi \cdot GBW \cdot n \cdot V_T \tag{5.9}$$

When applying the simple Miller compensation, the slew rate is to the first order determined by the GBW and not by the OTA current.

The considerations above are only valid as long as the bias current is significantly higher than the leakage currents. Thus, the OTA current was reduced only by factor two, such that C_C and C_{mirr} can be decreased by factor two.

5.1.6 Power-down circuitry

The regulator can be switched off with a power-down signal (marked with *pd* in the schematics). The expected voltage levels for this signal are ground and the supply voltage. The regulator shall operate normally, as long as this signal has a low level (ground). When this signal is pulled up to V_{DD} the regulator shall be switched off.

This behavior was achieved, by adding transistors, which act as a switch and pull all transistors' gates to their source potential upon receiving the *pd* signal. Series switches were added to all transistors with diode connection, which are controlled by the inverted *pd* signal. Thus, there is no active current path from supply to ground in power-down mode.

5.1.7 Fine tuning

The PMOS pass element was analyzed. It was observed, that in some conditions, when the pass element enters the triode region, the output swing of the OTA is no longer sufficient to provide the needed gate voltage. In this case the DC loop gain falls below 0 dB. Thus the PMOS' width was increased, such that that the loop gain stays sufficiently high under all conditions.

Then, the Miller capacitor was slightly increased to provide the specified PM under all conditions. Finally, the mirror capacitor was adapted to reduce the overshoot to a value close to the specified one, while considering the decrease of PM due the mirror pole. However, as the simulation results below show, the specifications for overshoot could not be met, while providing enough PM.

Figure 5.2 shows the modified circuit. The bias circuit as designed in chapter 4.1 was used.

5.2 Simulation

Simulations were done with a *MOS*11010 160 nm CMOS model from NXP Semiconductors. All following simulations were done for 3 supply voltages (1.8 V, 2.7 V and 3.6 V), 3 temperatures (−40 °C, 27 °C and 150 °C) and 5 corner transistor models provided by the foundry (nominal, snsp (considering slow transistors), fnfp (considering fast transistors), fast (considering fast transistors and small resistors) and slow (considering slow transistors and large resistors)). All plots in this section were done for 27 °C and nominal transistors, unless otherwise stated.

The regulator was simulated with a capacitive load parallel to a resistive load. The specified capacitive load ranges from 100 pF to 1 nF. All simulations were done for the minimum and maximum value. The output current was adjusted with a resistor. The specified load current ranges from 1 µA to 100 µA. As the typical output voltage is 1.5 V, a 1.5 MΩ and a 15 kΩ resistor were used to adjust the load current. The simulations, which are described as typical, were performed with a 500 pF capacitor parallel to a 30 kΩ resistor.

5.2.1 Temperature behavior

The temperature behavior was simulated using a DC simulation sweeping over the temperature. Figure 5.3 shows a typical temperature plot of the output voltage. The existing circuit exhibits a strong temperature dependence. The modified voltage reference exhibits a first order temperature compensation of the modified regulator.

5.2.2 Stability, regulation

The stability of the circuit was verified by evaluating the loop gain as described in chapter 3.2.2. A AC Simulation was done to obtain the Bode plot of the loop gain. Then, the DC loop gain A_0, phase margin PM and the transfer frequency UGF were

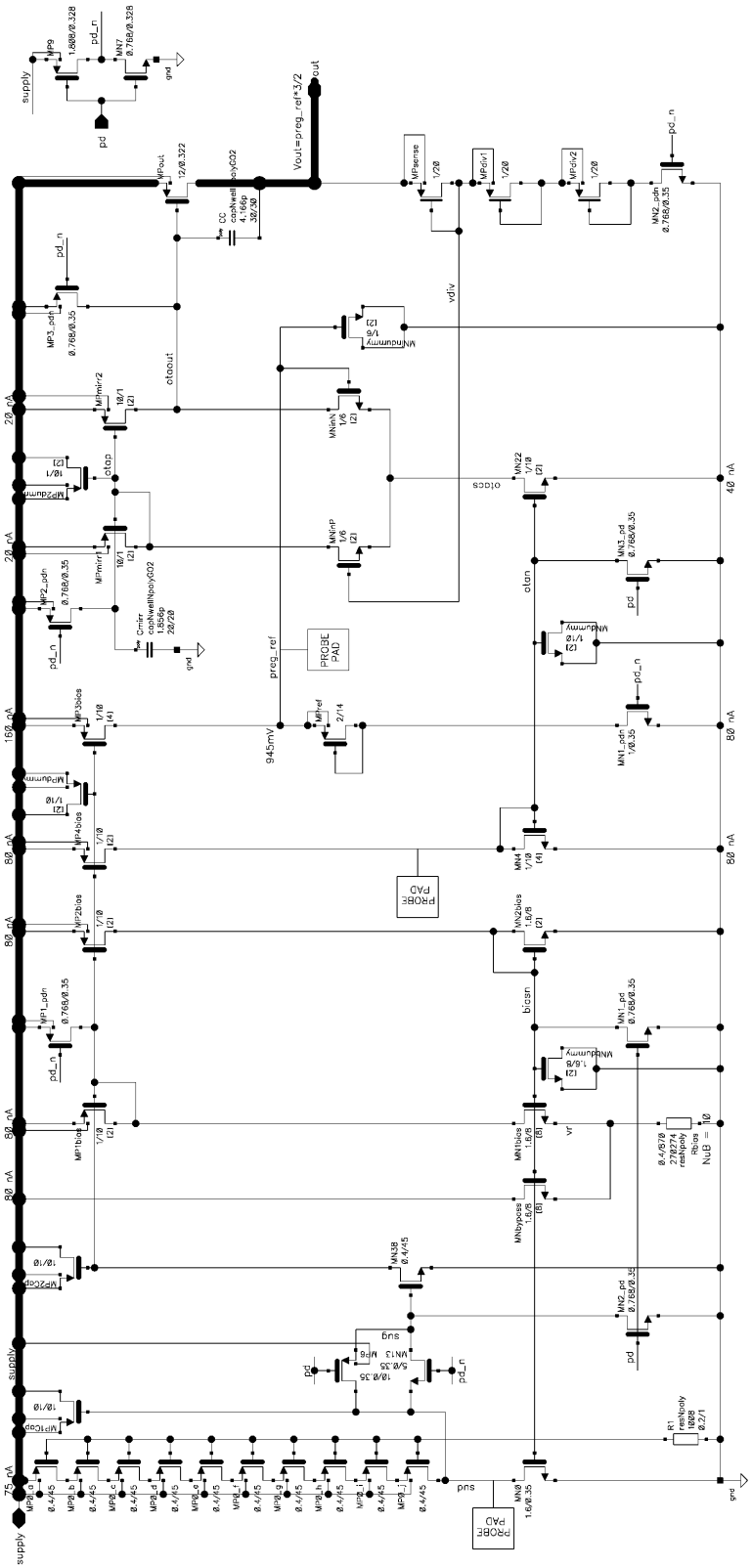

Figure 5.2: Schematic diagram of the modified start-up regulator circuit

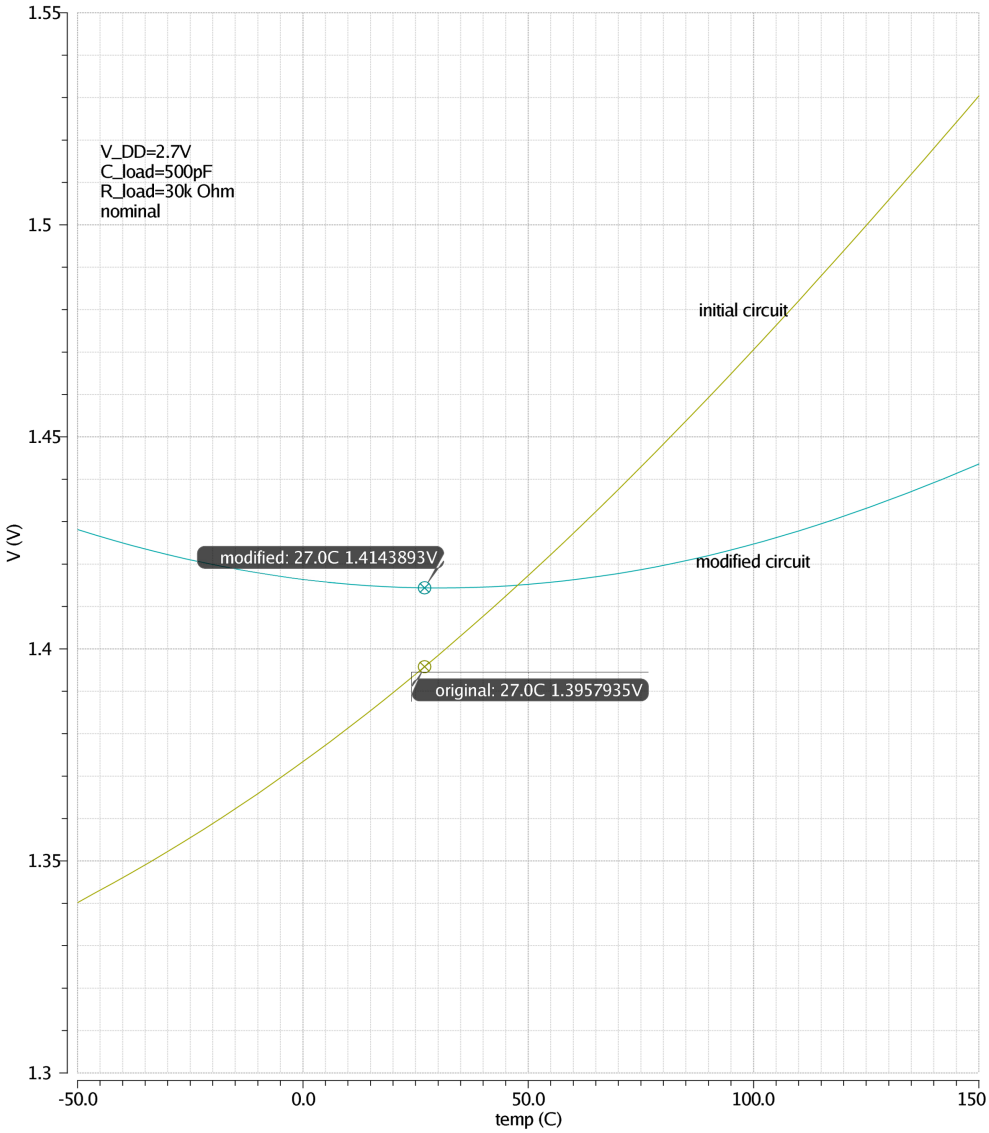

Figure 5.3: Output voltage of the regulator plotted over temperature.

obtained from the plot. Table 5.1 shows the simulated values of the existing and modified circuit. Typical values specify a supply voltage of 2.7 V, load capacitance of 500 pF and a load resistor of 30 kΩ at the output of the regulator. Minimum PM is observed for a supply voltage of 1.8 V, load capacitance of 1 nF and a load resistor of 1.5 MΩ. Minimum UGF is observed for a supply voltage of 3.6 V, load capacitance of 1 nF and a load resistor of 1.5 MΩ.

The negative loop gain of the existing circuit happens at low input voltages ($V_{DD} =$ 1.8 V), high temperature (150 °C) and slow transistors. In this case, the PMOS pass element is in triode and the output swing of the OTA is not sufficient to provide the needed gate source voltage.

Table 5.1: Simulated stability and regulation values

Existing regulator			
	Min.	Typ.	
A_0	<0	83	dB
PM	13.4	73.8	°
UGF	5	13	kHz

Modified regulator			
	Min.	Typ.	
A_0	47	78	dB
PM	16.4	75.0	°
UGF	4.7	11.8	kHz

5.2.3 Overshoot, caused by supply voltage variations

As described above the regulator is sensitive to fast rising edges of the supply voltage V_{dd}. In order to check the possible overshoot at the regulator's output, a supply rise time t_{supply} of 1 ns was applied. This value was considered the minimum rise time that could possible occur in any real application. The regulator was connected to the ideal supply source via a 50 Ω resistor. Transient simulation was performed. A test pattern for the supply voltage was applied. The pattern can bee seen in figure 5.4. The rise and fall time of the supply voltage is always 1 ns, the off times are indicated. The output signal of the two circuits at 27 °C are plotted. The worst overshoot was observed with minimal output capacitor ($C_L = 100$ pF) and maximum output resistance ($R_{load} =$ 1.5 MΩ). It can be observed, that the modified circuit exhibits significantly smaller overshoot. Table 5.2 shows the worst case values of overshoot generated by the test pattern when simulating the corners.

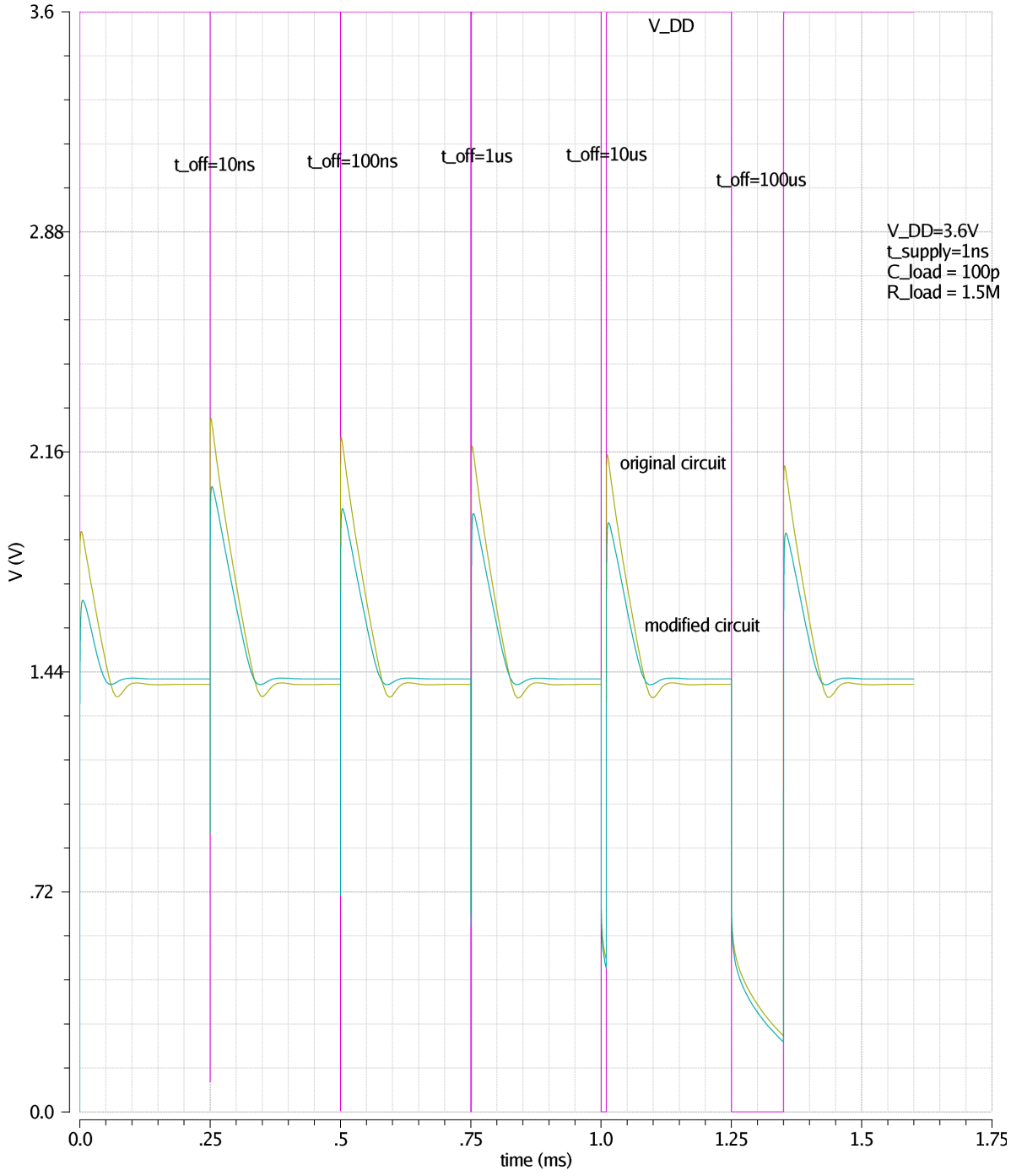

Figure 5.4: Transient response of the regulator to supply voltage variations.

Table 5.2: Maximum overshoot generated by the test pattern

	Existing circuit	Modified circuit	
Maximum overshoot	2.40	2.15	V

5.2.4 Overshoot and undershoot, caused by transient load current changes

Transient load current changes will also alter the output voltage. As there were no transient load regulation specifications given, it was only investigated, whether a transient load change would cause an overshoot of the output voltage. This was simulated with a transient analysis. The ideal supply source was connected to the regulator via a 50 Ω resistor. The output of the regulator was loaded with a minimal output capacitor ($C_L = 100\,\text{pF}$) and maximum output resistance ($R_{load} = 1.5\,\text{M}\Omega$). At a given time, a current source was switched on, sinking the maximum specified current from the output. After some time the current source was switched off again. Figure 5.5 shows the output voltage of the two circuits at 27 °C and the load current. The observed overshoot is nearly identical for both circuits and significantly smaller than the overshoot caused by fast supply steps.

5.2.5 Power supply ripple rejection

The PSRR was measured using an AC simulation. The gain from V_{DD} to V_{out} was evaluated. Figure 5.6 shows a plot of the gain over frequency for typical conditions. Table 5.3 shows the simulated values for all corner simulations. The PSRR at different frequencies f and the peak values are listed. The table presents the values for typical conditions and the worst case values over all corner simulations. The cases, where the loop gain of the existing circuit is below 0 dB (see above) were ignored. In these cases, the PSRR at low frequencies is close to 0 dB.

5.2.6 Current consumption

The current consumption (I_{DDq}) of the circuit was measured as the difference of current flowing into V_{DD} and current flowing out of V_{out}. The simulation was done for normal operation and for power down mode. Simulations revealed that load on the output has no influence on I_{DDq}, as expected. Table 5.4 shows the simulated

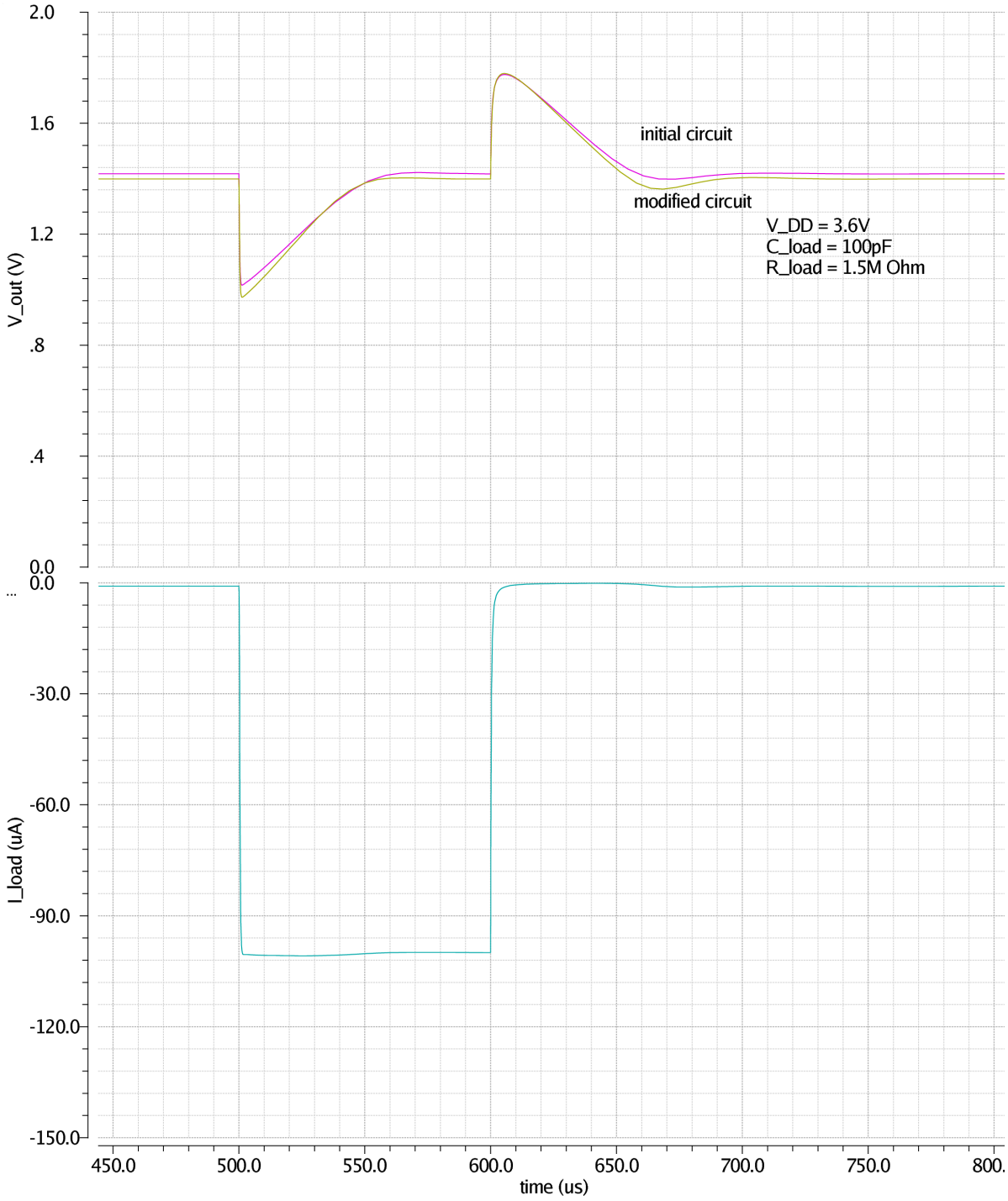

Figure 5.5: Transient response of the regulator to load changes.

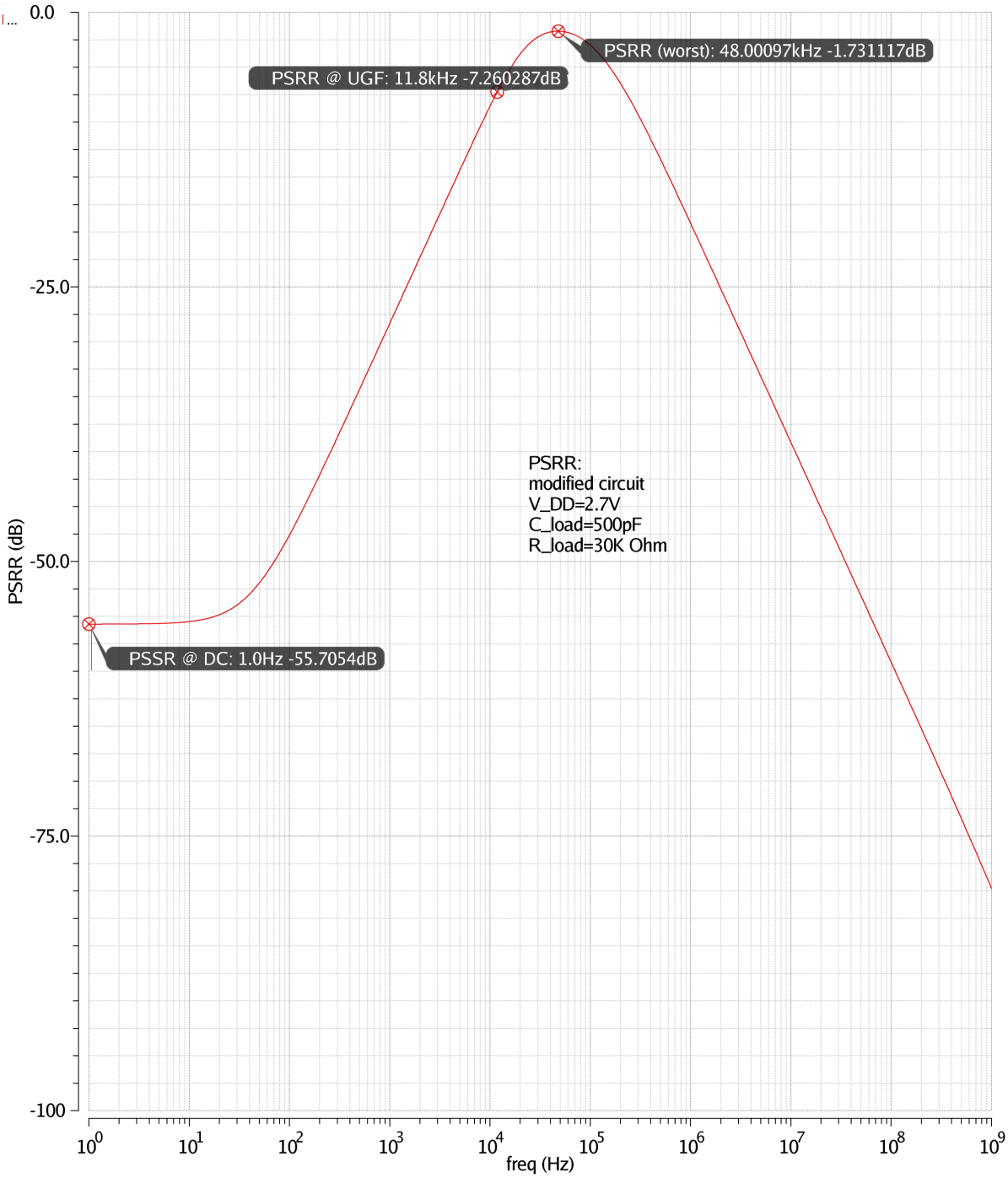

Figure 5.6: Plot of the improved circuit's PSRR over frequency.

Table 5.3: Simulated values of PSRR

Original circuit	PSRR		Modified circuit	PSRR	
f	Typ.	Max.	f	Typ.	Max.
1 Hz	−54.9 dB	−35.9 dB	1 Hz	−55.7 dB	−37.5 dB
50 Hz	−51.6 dB	−35.9 dB	50 Hz	−52.0 dB	−37.4 dB
1 kHz	−28.2 dB	−25.4 dB	1 kHz	−28.3 dB	−25.4 dB
10 kHz	−8.5 dB	−2.6 dB	10 kHz	−8.6 dB	−4.7 dB
100 kHz	−3.3 dB	−1.1 dB	100 kHz	−3.0 dB	−1.0 dB
1 MHz	−19.9 dB	−4.0 dB	1 MHz	−19.2 dB	−3.4 dB
10 MHz	−39.9 dB	−21.1 dB	10 MHz	−39.2 dB	−20.1 dB
peak	−1.7 dB	−0.8 dB	peak	−1.7 dB	−0.9 dB
at f	44 kHz	27.4 kHz	at f	48 kHz	145 kHz

values. Typical values are for $V_{DD} = 2.7\,\text{V}$ and 27 °C. Minimum values are for $V_{DD} = 1.8\,\text{V}$ and −50 °C, maximum values are for $V_{DD} = 3.6\,\text{V}$ and 150 °C.

Table 5.4: Current consumption

Existing circuit					Modified circuit				
	Min.	Typ.	Max.			Min.	Typ.	Max.	
I_{DDq} normal	437	813	1560	nA	I_{DDq} normal	327	582	1130	nA
I_{DDq} pd		0.12	11.9	nA	I_{DDq} pd		0.14	10.3	nA

5.2.7 Process variation and mismatch simulation

A Monte-Carlo simulation was used to simulate the impact of process variations and mismatch on the output voltage V_{out}. The regulator was simulated under typical conditions ($V_{DD} = 2.7\,\text{V}$, $C_L = 500\,\text{pF}$, $R_{load} = 30\,\text{k}\Omega$, 27 °C), 1500 iterations were performed. The estimated mean $\overline{V_{out}}$ value and the estimated standard deviation σ of the output voltage can be seen in table 5.5.

Table 5.5: Monte Carlo Simulation of the output Voltage

	Existing circuit	Modified circuit	
$\overline{V_{out}}$	1.395	1.415	V
σ	35.5	39.5	mV

5.2.8 Static line and load regulation

From the simulations above, the line and load regulation was calculated as described in section 3.2.5. These values are presented in table 5.6.

Table 5.6: Line and load regulation

Existing circuit			
	Typ.	Max.	
Line reg.	2.52	38.2	mV/V
Load reg.	3.25	640.40	mV/mA

Modified circuit			
	Typ.	Max.	
Line reg.	2.26	3.67	mV/V
Load reg.	5.75	15.35	mV/mA

The degraded line and load regulation of the original circuit appears at high temperatures, when the PMOS pass element is in triode. In that case the output swing of the error amplifier is not sufficient to provide the needed gate voltage.

5.3 Circuit comparison

The modifications done to the existing circuit were primarily aimed to improve specification fulfillment. Additionally the modifications were focused on area reduction and current reduction.

The maximum voltage overshoot at the output was reduced by approximately 10 percent. Still, the specification for maximum voltage is not met. However, the violation of the limit was significantly reduced.

The PM was slightly increased to fulfill the specifications, however accordingly the minimal UGF had to be decreased. Mismatch and PSRR are similar in both circuits.

The redesign of the voltage reference induced great improvement to the regulator. The output voltage of the modified circuit is temperature compensated to first order. The output voltage changes less than 30 mV over the whole temperature range in comparison to 190 mV in the existing circuit (Figure 5.3).

Current consumption was significantly reduced. The start-up circuitry of the bias current reference, the current through the voltage reference and the OTA's bias current were modified. From table 5.4 a typical reduction of approximately 28 % was achieved.

The layout of the existing circuit occupies $122\,\mu m \cdot 64\,\mu m = 7808\,\mu m^2$ excluding pads. Modifications were done to reduce the needed capacitors and the reference resistor for the bias circuitry. The modified circuit needs $105\,\mu m \cdot 58\,\mu m = 6090\,\mu m^2$. Thus a reduction of $1718\,\mu m^2$ was accomplished, which is about 22 % of the initial size.

6 An LDO with a multi-stage error-amplifier

The modifications suggested in chapter 5 greatly improved the start-up regulator. However, the overshoot requirement is still not reached. A large mirror capacitor is needed, which degrades the PM. Additionally there is no pole-zero compensation possible, which limits the bandwidth of the circuit. Thus, an extensive literature research was done to find a circuit topology, which will overcome these drawbacks. The basic concepts of reference and bias generation together with a PMOS pass element were to be retained.

Rincon-Mora and Allen [26] have presented an LDO with a two stage error amplifier containing a gain stage and a buffer stage. The buffer stage is adaptively biased according to the output current of the LDO. They achieve a frequency response and slew rate behavior, which adapts to the load condition. Lam, Ki, and Tsui [15] have presented a LDO with an adaptively biased OTA. They have suggested an improved current sensing circuit. However, as the specified maximum output current is small (100 µA), sensing the output current could not be realized with the possible transistor measures while fulfilling the current consumption specifications.

Milliken, Silva-Martinez, and Sanchez-Sinencio [20] have presented an LDO which does not need external compensation. This is achieved by using an error amplifier and additionally a differentiator, which forms a second control loop to improve the transient behavior of the regulator. However, the differentiator needs a large capacitor ($>$10 pF) for sensing current changes, which would occupy too much die area.

Fernandes [8] has proposed a two stage error amplifier with a push-pull stage on the output to overcome slew rate issues. Lau, Mok, and Leung [16] have presented a similar circuit with an advanced frequency compensation scheme to reduce on chip capacitors.

It was decided to design an LDO based on the work of Lau, Mok, and Leung [16], as their suggestion involves an error amplifier with a push-pull output stage, to overcome slew rate limitations and an advanced compensation scheme, which allows higher bandwidth than the existing circuit from chapter 5, while using minimum area for compensation capacitors. In contrast to the published circuit, all transistors

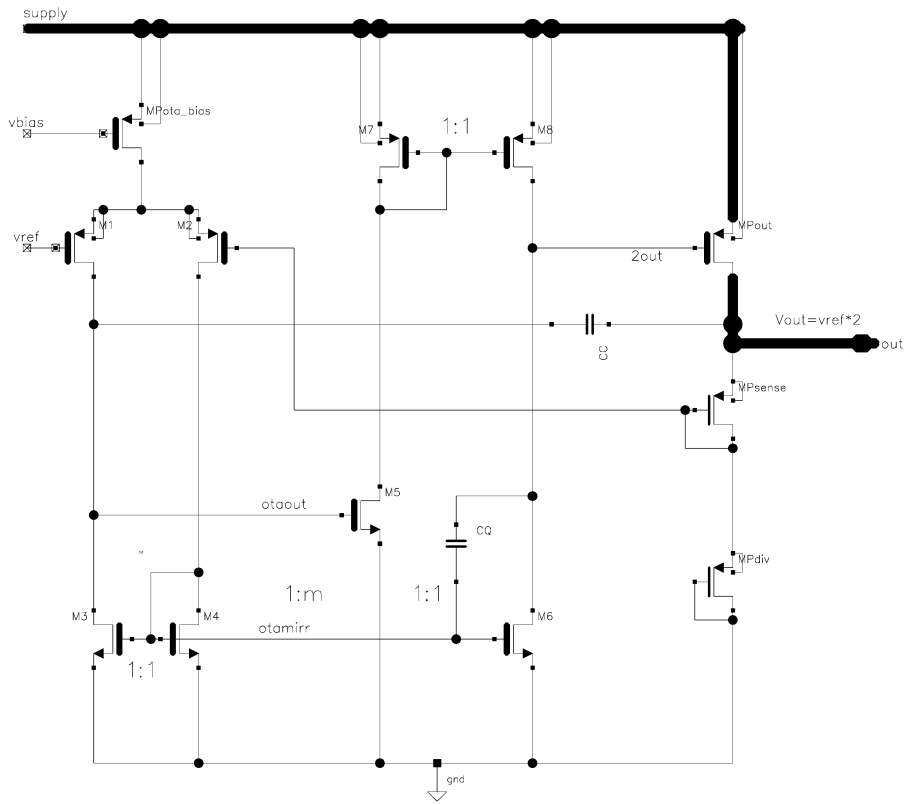

Figure 6.1: Schematic of regulator circuit proposed by Lau, Mok, and Leung [16] .

(apart from the output PMOS) were designed to operate in weak inversion, to meet the current specifications.

Figure 6.1 shows the principle circuit. A OTA with PMOS input compares the output voltage to a reference voltage. The output of the OTA is further amplified with a push-pull stage. The push-pull stage can source a high current, which is not bound to the OTA's bias current. Miller compensation is applied from the OTA's output to the LDO output. The push-pull stage offers additional gain. This gain significantly improves the compensation, allowing a smaller compensation capacitor. Additionally, the output of the OTA remains nearly constant because of the gain of the push-pull stage. Thus, the slewing behavior due to the Miller capacitor at the output of the OTA will be greatly improved.

6.1 Bias ciruit

The bias circuit described in chapter 4.1 was used. As mentioned above, the bias circuit is designed to provide an output current of 80 nA.

6.2 Voltage divider

The error amplifier has a PMOS input differential pair. To obtain enough voltage headroom at the minimum supply voltage $V_{DD_{min}} = 1.8\,\text{V}$, a reference voltage of 0.75 V was chosen. The voltage divider is then designed to have a feedback factor $\beta = 0.5$.

6.3 Reference voltage generation

As in the circuits from the last chapter, the reference voltage is derived from a MOS-diode biased with a reference current. As a lower reference voltage is needed for this circuit, a NMOS transistor was used, which has a lower threshold voltage in the used technology. It was designed to provide a gate source voltage of 0.75 V. In order to minimize current consumption and reference voltage variation (see section 5.1.3), a small bias current was used. In this case a slightly negative temperature behavior was chosen. This will provide some voltage headroom for the PMOS pass element at high temperatures, as the output voltage will slightly decrease for rising temperature.

6.4 Frequency compensation

The circuit includes several gain stages, requiring a sophisticated compensation scheme to maintain stability. Lau, Mok, and Leung [16] present a linear circuit model of the regulator. They model the circuit with three gain stages which represent the input OTA, the push-pull stage and the output transistor. Additionally, they identify a feed forward path formed by $M2$, $M4$ and $M6$. This path creates a left half-plane (LHP) zero, which significantly improves the frequency response.

In their analysis, they distinguish three different load conditions: high load current, moderate load current and low load current. However in this work, only the case of moderate load current was considered, where the transconductance of the output transistor $g_{m_{out}}$ is higher than the transconductance of the push-pull stage g_{m_5}, but

of similar magnitude. This is valid, because the minimum current through MP_{out} is higher, but in about the same magnitude as the bias currents through M_5. The maximum output current is 100 times higher, which will increase $g_{m_{out}}$ by a factor of $15-25$, as MP_{out} changes from moderate inversion to strong inversion operation.

The analysis of Lau, Mok, and Leung [16] shows that the frequency response is then formed by a dominant pole, a LHP zero and a pair of complex poles [16]. The dominant pole, which is formed by the output resistance of the OTA and the Miller capacitor can be calculated with formula 6.1. R_L, r_{2out} and r_{otaout} represent the load resistance, the differential resistance at the output of the push-pull stage and the differential resistance at the output of the OTA, respectively. Formula 6.2 can be used to calculate the UGF. The zero can be approximately calculated with formula 6.3, where m is the multiplication factor between $M3/4$ and $M5/6$. The frequency of the complex poles can be approximated with formula 6.4, its quality factor ($Q-factor$) with formula 6.5. Where C_{gd}, C_{2out} and C_L are the gate drain capacitance of MP_{out}, the lumped capacitance at the output of the push-pull stage and the load capacitance, respectively. However, simulations showed, that the complex poles' frequency is a little smaller than approximated, while the approximation of the zero is quite accurate.

$$f_{p1} = \frac{1}{2\pi \cdot C_c \cdot g_{m_5} \cdot r_{2out} \cdot g_{m_{out}} \cdot R_L \cdot r_{otaout}} \tag{6.1}$$

$$UGF \approx GBW \cdot \beta = \frac{g_{m_1} \cdot \beta}{2\pi \cdot C_c} \tag{6.2}$$

$$f_z \approx \frac{g_{m_6}}{2\pi \cdot C_c \cdot m} = \frac{g_{m_4}}{2\pi \cdot C_c} \tag{6.3}$$

$$f_{p2,3} \approx \frac{1}{2\pi} \cdot \sqrt{\frac{g_{m_5} \cdot g_{m_{out}}}{(C_{gd} + C_{2out} + C_Q) \cdot C_L}} \tag{6.4}$$

$$Q \propto \frac{g_{m_4}}{C_Q} \tag{6.5}$$

Some conclusions can be drawn from these formulas. The circuit operates in weak inversion, thus $g_{m_1} \approx g_{m_4}$, as the slope factor n is similar for PMOS and NMOS. The zero is then located at approximately $\frac{UGF}{\beta}$. It is interesting to see, that the first non dominant pole at $f_{p2,3}$ is independent of the Miller capacitor. This complex pole pair may cause a magnitude peak in the frequency response at $f_{p2,3}$, due to small damping factor [18], which might cause stability issues. Thus, the Q-factor of the poles must

be made as small as possible, which causes the magnitude peak to decrease. This can be done by adapting g_{m_4} and C_Q separately. It should be noted, that adapting the Q-factor via C_Q will decrease the frequency of the pole pair. Thus g_{m_4} should be minimized first, which will also improve mismatch of the OTA's current mirror. The transconductance g_{m_5} can be adapted with the multiplication factor m. The frequency of the complex pole pair will increase, as g_{m_5} increases. However, as the lumped capacitance at the output of the push-pull stage C_{2out} also increases with m, the pole frequency will decrease again above a particular multiplication factor.

6.5 Supply voltage dependance

In contrast to the circuits in the last chapter, the Miller capacitor does not short gate and drain of the PMOS pass element for high frequencies. Signals between gate and source of MP_{out} will be amplified to the output up to high frequencies. The gate of MP_{out} must be fed with a signal correlated to the ripples on the supply line up to frequencies where the load capacitor starts to short the output. As described in chapter 3.15, providing this correlated signal is inherent to PMOS current mirrors. However, the model presented in figure 3.7 predicts, that this is not valid for low-power mirrors at high frequencies. The correlated ripple signal will decrease at higher frequencies.

PSRR is especially problematic for small load capacitors C_L and high load currents. As described in chapter 3, the PSRR is worst above UGF but will decrease for even higher frequencies because the load capacitors C_L will short power supply ripples to ground. Thus, the PSRR's peak value shifts to higher frequencies, when using smaller load capacitors. The higher the load current is, the higher the output transistor's transconductance grows. Therefore the gain of the output PMOS at high frequencies

$$A_{HF} \approx \frac{g_{m_{out}}}{2\pi \cdot f \cdot C_L} \tag{6.6}$$

is higher.

Simulations revealed, that the device capacitance and the transconductance of the current mirror transistors $M7$ and $M8$ have a major impact on the PSRR at about 1 MHz as predicted by the model. The performance could only be improved by increasing the transconductance and decreasing the parasitic capacitance. The transconductance could be increased by higher current through the push-pull stage. Noting that $g_{m_5} = g_{m_6} = m \cdot g_{m_4}$, the multiplication factor m had to be increased to increase the current. Above a certain value of m, the slew rate of the regulator will be limited only by the OTA current and C_C and no longer by the gate capacitance of the PMOS pass element. As noted above, further increasing m will not improve the circuit

performance (apart from PSRR), but will increase the current consumption. Thus above a certain value of m, improving the PSRR can only be achieved by excessive current consumption.

Additionally another mechanism which degrades the PSRR was identified. The gate of $M6$ senses the correlated ripple signal via capacitor C_Q. Then the signal is additionally decreased via $M6$ and $M3 - M5 - M7 - M8$. Therefore C_Q should be designed as small as possible.

Heng and Pham [11] present a circuit structure, which improves the PSRR of a LDO without increasing the power consumption. This is achieved by a circuit connected to the back gate of one input transistor. However, their circuit is intended to improve the PSRR at low and middle frequencies. In order to enhance the PSRR performance at higher frequencies, the proposed circuitry was slightly adapted and connected to the back gate of $M8$. Figure 6.2 shows this circuit. $M9$ can be modeled as linear resistor, which pulls the bulk of $M8$ to V_{DD} in normal operation. Only changes of the supply voltage are sensed via C_{PSRR} and cause a voltage drop over $M9$. This signal is applied to the back gate of $M8$. The signal at the back gate compensates, up to some degree, the decrease in the output ripple signal. The signal shows a high pass behavior with a cutoff frequency of

$$f_c = \frac{1}{2\pi \cdot R_{on} \cdot C_{PSRR}} \quad , \tag{6.7}$$

where R_{on} is the linear resistance of $M9$. The cutoff frequency should be designed well above the UGF of the regulator, but below the critical peak of the PSRR (which is to be suppressed), such that the circuit does not disturb the normal operation.

6.6 Dimensioning

As a first starting point, a UGF of 35 kHz was targeted, this is about 3 times the UGF of the existing circuit. In order to keep the needed capacitors small (formula 3.9 and 6.5), the OTA's bias current I_{SS} was chosen 40 nA. The input differential pair was designed with a high $\frac{g_m}{I_D} = 23$ to minimize mismatch [1] and a length 10 times higher than the minimum length to increase the output resistance. As $\beta = 0.5$ the needed compensation capacitor can be calculated with formula 6.2 and is approximately 1 pF. The length of the NMOS diode-connected load was chosen such that the output resistance is similar to the input differential pair. The width was chosen small, while maintaining sufficient channel area for mismatch reasons.

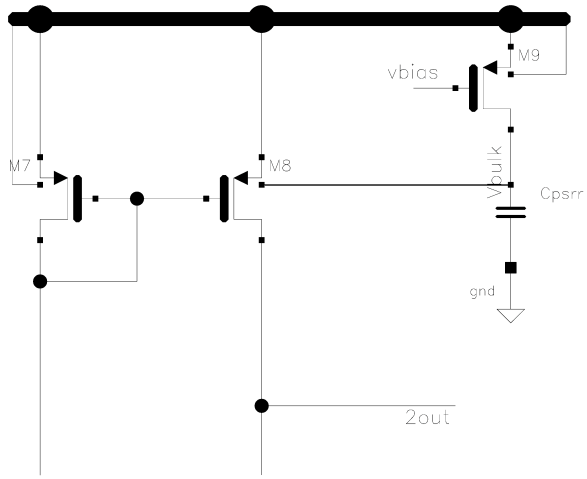

Figure 6.2: Schematic of the back gate circuit to improve the PSRR.

The multiplication factor m should be chosen high. This will increase the DC loop gain and improve the slewing behavior at the gate of the PMOS pass element. The frequency of the complex pole pair will also increase, as g_{m_5} increases. However, as the lumped capacitance at the output of the push-pull stage C_{2out} also increases with m, the pole frequency will decrease again above a particular multiplication factor. Additionally, the current consumption will increase with high m. As a compromise, the multiplication factor was chosen 4.

The PMOS current mirror of the push-pull stage was designed to maximize its transconductance at minimum area. This is needed to improve the PSRR (see section 3.15). This design will increase the mismatch of the PMOS current mirror. However, as the offset voltage (which appears as the permanent error at the output) is mainly dominated by the first stage of the regulator, this mismatch will not significantly decrease the circuit performance.

The output transistor MP_{out} was designed with minimum length, to keep the parasitic capacitance small. The width was chosen such that the output swing of the push-pull stage is sufficient to provide the needed gate potential at all conditions.

The bias circuit from chapter 4.1 was adopted. The complete circuit can be seen in figure 6.3. The layout of the circuit occupies 5081.25 µm^2.

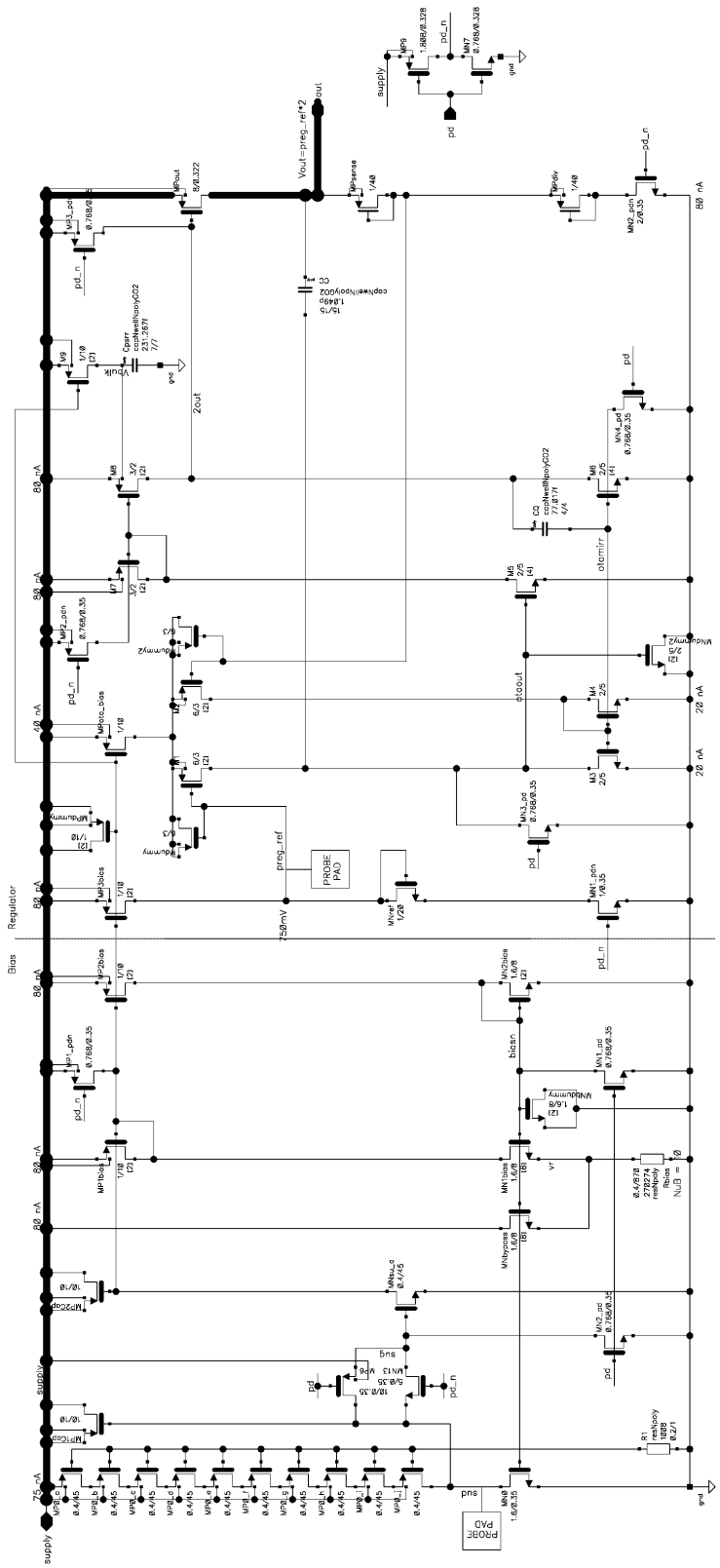

Figure 6.3: Schematic of the start-up regulator with Q-reduction and PSRR back-gate circuit.

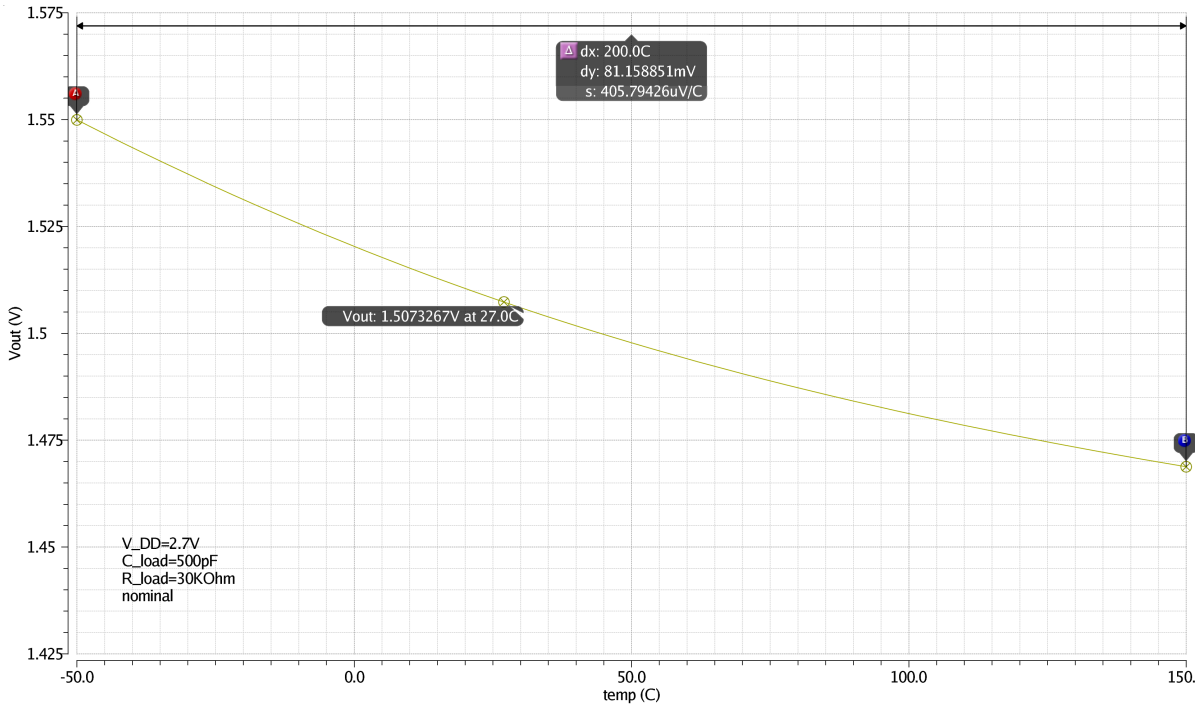

Figure 6.4: Output voltage of the regulator plotted versus temperature.

6.7 Simulation

Simulations were done with a *MOS*11010 160 nm CMOS model from NXP Semiconductors. All following simulations were done for 3 supply voltages (1.8 V, 2.7 V and 3.6 V), 3 temperatures (−40 °C, 27 °C and 150 °C) and 5 corner transistor models provided by the foundry (nominal, snsp (considering slow transistors), fnfp (considering fast transistors), fast (considering fast transistors and small resistors) and slow (considering slow transistors and large resistors)). All plots in this section were done for 27 °C and nominal transistors, unless otherwise stated.

6.7.1 Temperature behavior

The temperature behavior was simulated using a DC simulation sweeping over the temperature. Figure 6.4 shows a typical temperature plot of the output voltage. The slightly negative temperature behavior, as described above can be seen.

6.7.2 Stability, regulation

The stability of the circuit was verified by evaluating the loop gain as described in chapter 3.2.2. An AC Simulation was done to obtain the Bode plot of the loop gain. Then, the DC loop gain A_0, phase margin PM and the transfer frequency UGF were obtained from the plot. Table 6.1 shows the simulated values. Typical values and the extreme values over all corners and load conditions are shown. Typical values specify a supply voltage of 2.7 V, load capacitance of 500 pF and a load resistor of 30 kΩ at the output of the regulator. The Bode plot of the loop gain at typical conditions can be seen in figure 6.5. The load current is varied.

Table 6.1: Simulated stability and regulation values

	Min.	Typ.	Max.	
A_0	65	112	141	dB
PM	26.0	98.7	100.9	°
UGF	21.6	39.6	58.5	kHz

6.7.3 Overshoot, caused by supply voltage

The same test pattern as in chapter 5 was applied to test the overshoot at the output. Figure 6.6 shows the output when applying the test pattern. The plot shows the circuit with the same load conditions as the circuits in figure 5.4. The maximum overshoot generated by the test pattern when simulating the corners was 1.955 V.

6.7.4 Overshoot and undershoot, caused by transient load current changes

The simulation was done as in chapter 5. The output current was increased from the minimum value to the maximum specified value. Figure 6.7 shows the output voltage at transient load changes. The plot shows the circuit with the same load conditions as the circuits in figure 5.5. The observed overshoot is significantly smaller than the overshoot caused by fast supply steps.

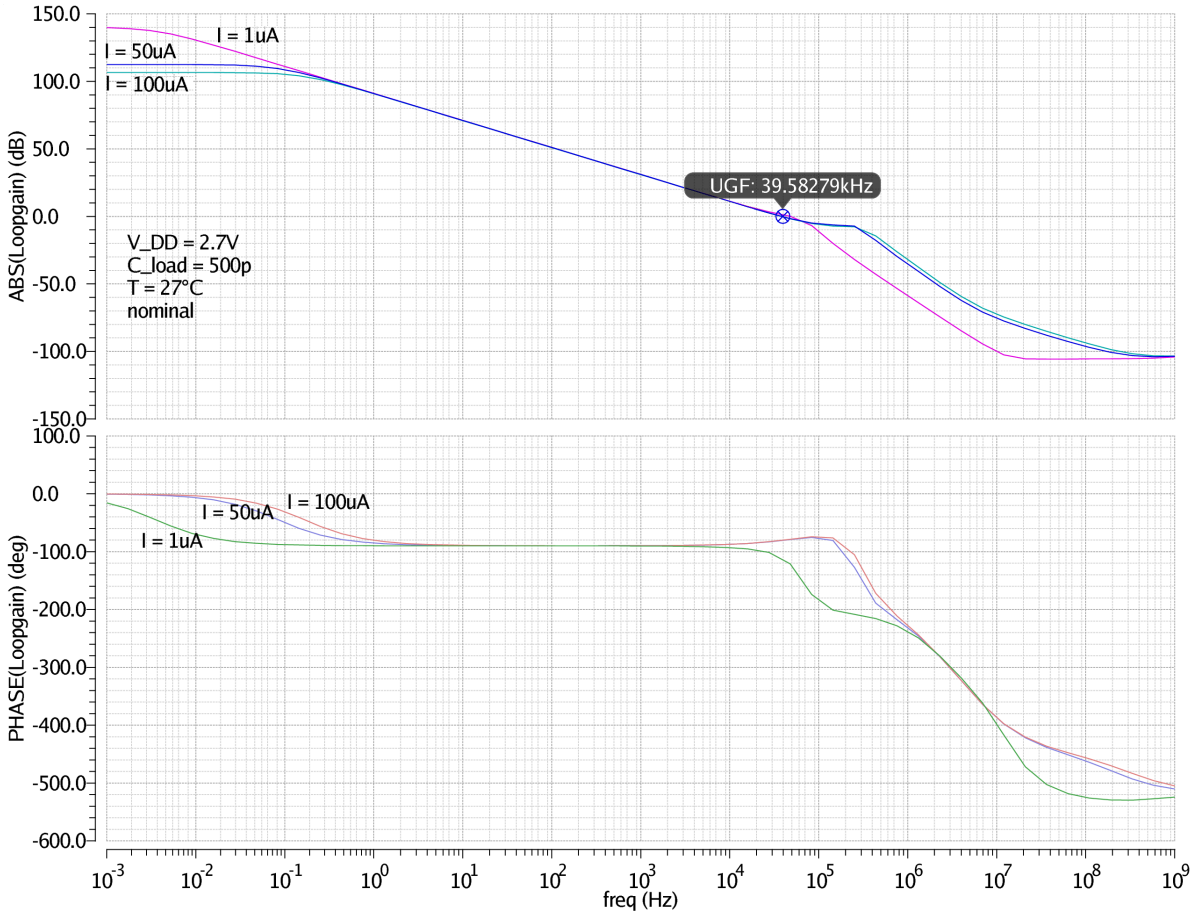

Figure 6.5: Bode plot of the loop gain.

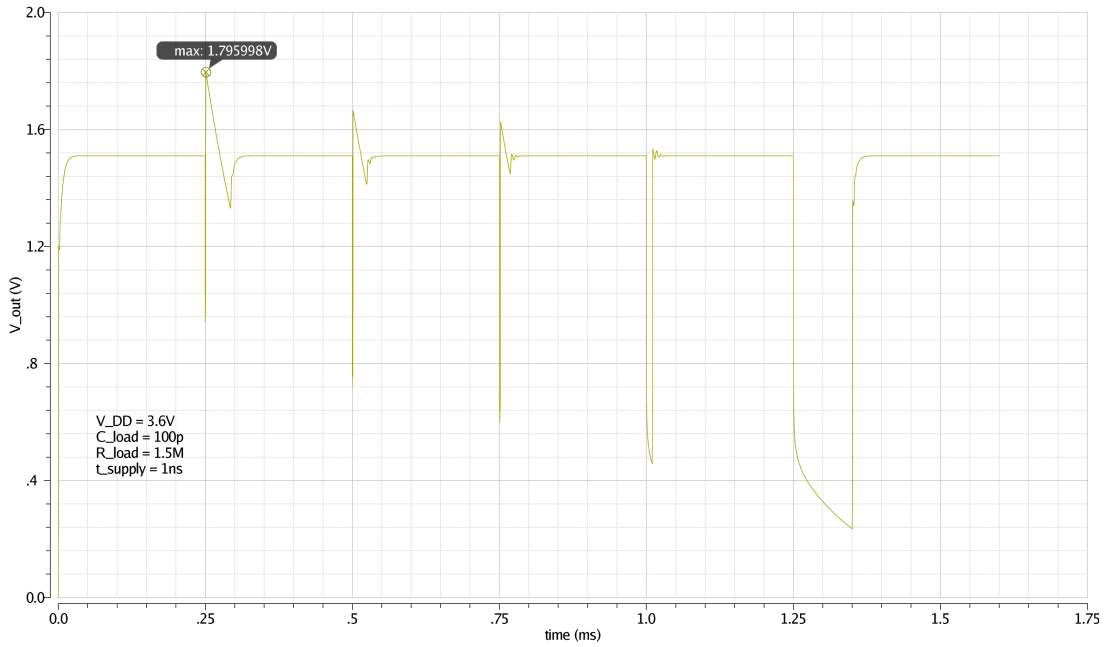

Figure 6.6: Transient response of the regulator to supply voltage variations.

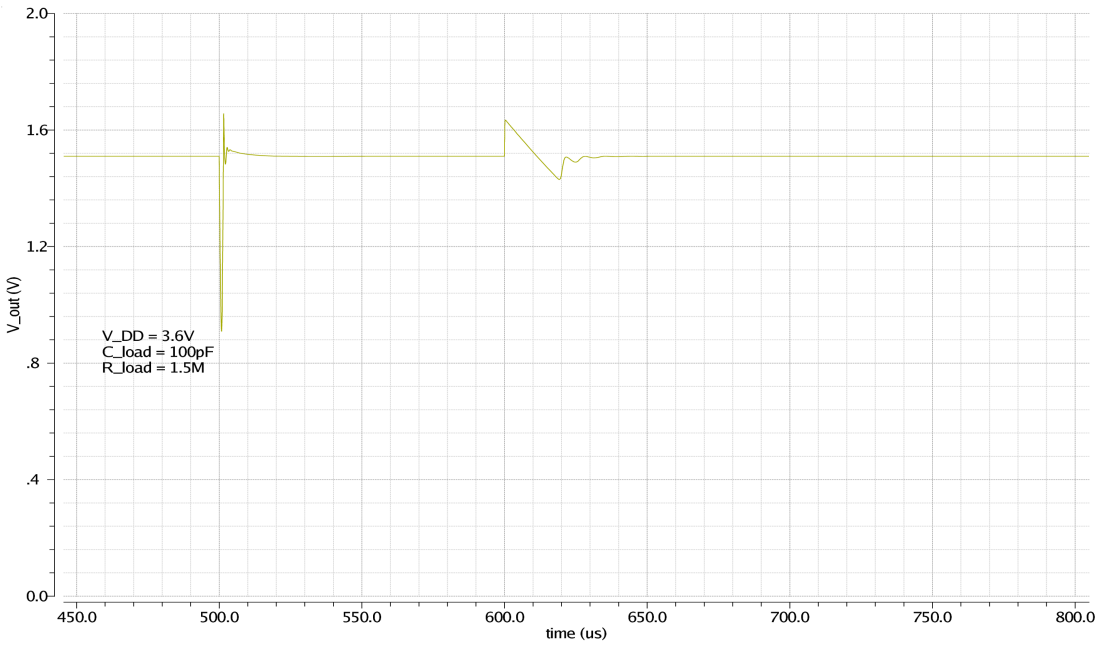

Figure 6.7: Transient response of the regulator to load changes.

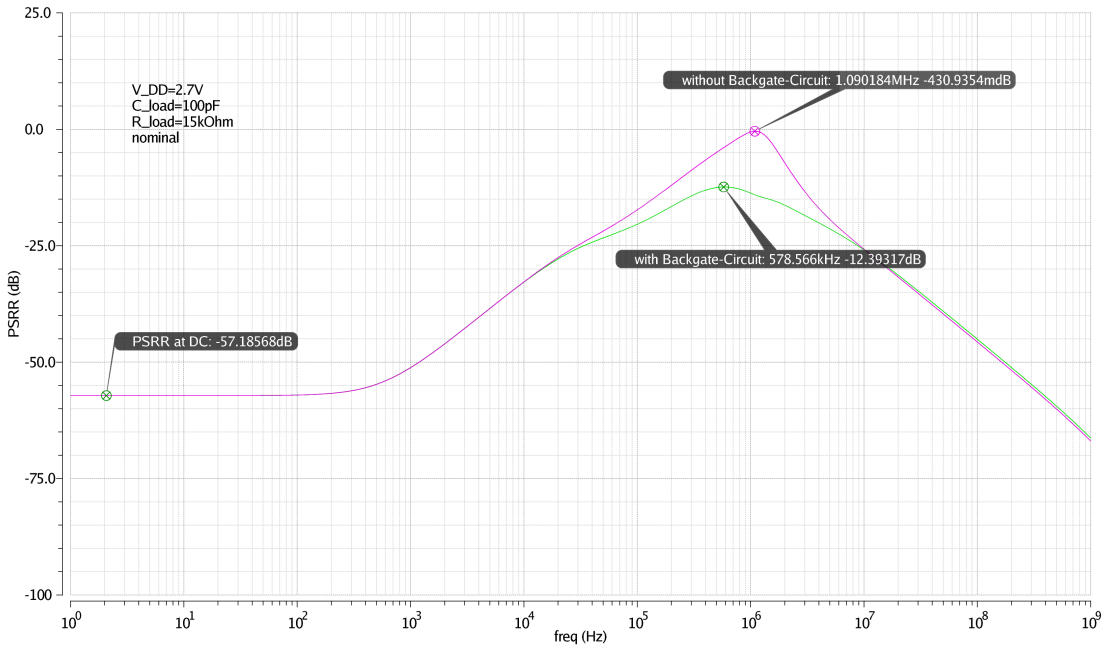

Figure 6.8: Plot of the PSRR versus frequency for the regulator with and without back gate circuit.

6.7.5 Power supply ripple rejection

The PSRR was measured using an AC simulation. The gain from V_{DD} to V_{out} was evaluated. Figure 6.8 shows a plot of the gain versus frequency for a high supply voltage, a high load current and small load capacitance. In this state the PSRR is worst because the output PMOS is in saturation and has a high transconductance. The plot shows the circuit with and without the back gate circuit. Table 6.2 shows the results of all corner and load simulations. Worst case results and typical values are presented.

6.7.6 Current consumption

The current consumption (I_{DDq}) of the circuit was measured as the difference of current flowing into V_{DD} and current flowing out of V_{out}. The simulation was done for normal operation and for power down mode. Simulations revealed that load on the output has no influence on I_{DDq}, as expected. Table 6.3 shows the simulated values. Typical values are for $V_{DD} = 2.7\,\mathrm{V}$ and $27\,^{\circ}\mathrm{C}$. Minimum values are for $V_{DD} = 1.8\,\mathrm{V}$ and $-50\,^{\circ}\mathrm{C}$, maximum values are for $V_{DD} = 3.6\,\mathrm{V}$ and $150\,^{\circ}\mathrm{C}$.

Table 6.2: Simulated values of PSRR

	PSRR	
f	Typ.	Max.
1 Hz	−57.2 dB	−38.3 dB
50 Hz	−57.1 dB	−38.3 dB
1 kHz	−51.1 dB	−33.6 dB
10 kHz	−32.8 dB	−14.5 dB
100 kHz	−19.3 dB	−4.4 dB
1 MHz	−32.8 dB	−2.2 dB
10 MHz	−42.7 dB	−16.5 dB
peak	−8.5 dB / 274 kHz	−2 dB / 566 kHz

Table 6.3: Current consumption of the new regulator

	Min.	Typ.	Max.	
I_{DDq} normal	394	653	1180	nA
I_{DDq} pd		0.15	10	nA

6.7.7 Process variation and mismatch simulation

A Monte-Carlo simulation was used to simulate the impact of process variations and mismatch on the output voltage V_{out}. The regulator was simulated under typical conditions ($V_{DD} = 2.7\,\text{V}$, $C_L = 500\,\text{pF}$, $R_{load} = 30\,\text{k}\Omega$, $27\,^\circ\text{C}$), 1500 iterations were performed. The simulation revealed an estimated mean value $\overline{V_{out}} = 1.50\,\text{V}$ and an estimated standard deviation $\sigma = 40.5\,\text{mV}$.

6.7.8 Static line and load regulation

From the simulations above, the line and load regulation was calculated as described in 3.2.5. Table 6.4 shows the values.

Table 6.4: Line and load regulation

	Typ.	Max.	
Load regulation	0.075	0.120	mV/mA
Line regulation	1.99	3.22	mV/V

6.8 Circuit comparison

From the simulation results, it can be seen that the new circuit topology is far superior compared to the initial, already existing circuit. The proposed circuit has a 20 % smaller current consumption and a 35 % smaller area consumption compared to the existing circuit.

The voltage variation of the temperature behavior is significantly smaller, while the temperature behavior was designed to support the PMOS pass element at high temperatures.

The proposed compensation scheme by Lau, Mok, and Leung [16] allows a 3 to 4 times higher UGF with minimum compensation capacitance. The DC loop gain was increased by nearly 20 dB. Additionally the worst case PM for large load capacitors was increased by 10° to improve the settling behavior. These measures greatly improve the regulation behavior. From the simulations, faster settling and improved line and load regulation are evident. Additionally, the PSRR at low frequencies has greatly improved due the higher UGF and higher DC gain. The typical PSRR at 1 kHz has improved by approximately 20 dB.

The overshoot problem is completely solved by the new circuit topology. Even high and fast voltage spikes on the supply line (3.6 V in 1 ns) will not cause a critical overshoot at the output of the regulator. Figure 6.6 and 6.7 clearly show the improved slew rate of the new circuit.

Great effort was put into improving the PSRR behavior of the circuit in order to meet the specifications. Especially, the PSRR behavior of the circuit at frequencies around 1 MHz was challenging. However, the simulation results show that the applied measures are sufficient. All specifications are met, compared to the existing circuit, the new circuit is superior over the whole frequency range.

The Monte-Carlo simulations predict a slightly larger output voltage variation due to process variations and mismatch. However, taking the specifications ($Vout = 1.2$ V to 1.8 V) into account, the calculated standard deviation is still small enough to achieve more than a six sigma range to the specified limits.

7 Measurements and verification

A test-chip with the existing, the modified and the new regulator was fabricated in 160 nm CMOS technology. The test-chip contains separate supply pads and output pads for each regulator and a common power-down pad.

20 samples of the test-chip, in a ceramic DIP8 package were measured in the laboratory.

7.1 Static measurements

These measurements were done using a pico-amperemeter with integrated voltage source and a source-meter. The pico-amperemeter was used to supply the regulators. The sourcemeter was used to sink a defined output current. The current consumption was measured as difference of supply current to output current. The regulators were loaded with an output capacitor of 470 pF.

7.1.1 Temperature behavior

The temperature behavior of the output voltage was measured at typical conditions. The supply voltage was 2.7 V, the load current was 50 µA. The temperature was varied from −40 °C to 125 °C with a thermostream. The design was simulated from −50 °C to 150 °C, however, the measurements were done for a smaller range, due to the limited capabilities of the measurement equipment. To save laboratory time, only 3 samples were measured over this temperature range. The reported measurement values are the mean value of these 3 samples. There was no significant difference of measured readings between the three samples.

Figure 7.1 shows the output voltage of the regulators versus temperature. The modified regulator showed, as expected, a good temperature compensation. On all three samples the voltage deviation of the modified regulator was less than 6 mV over the measured temperature range.

Figure 7.2 shows the current consumption of the regulators versus temperature.

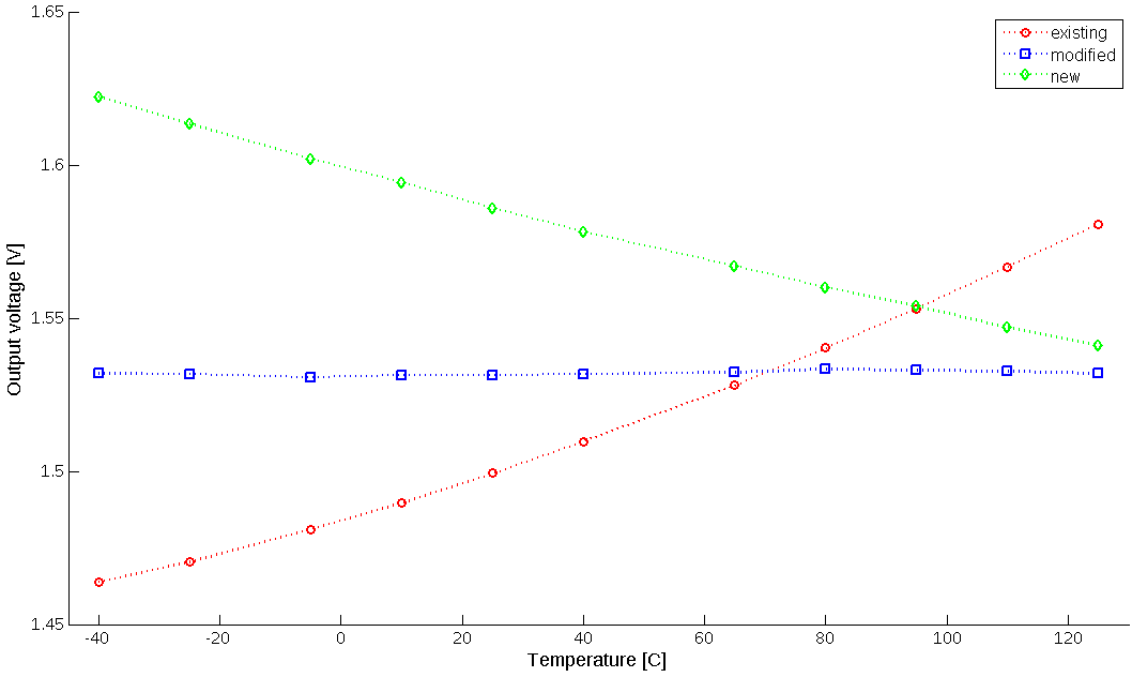

Figure 7.1: Measured output voltage of the regulators versus temperature

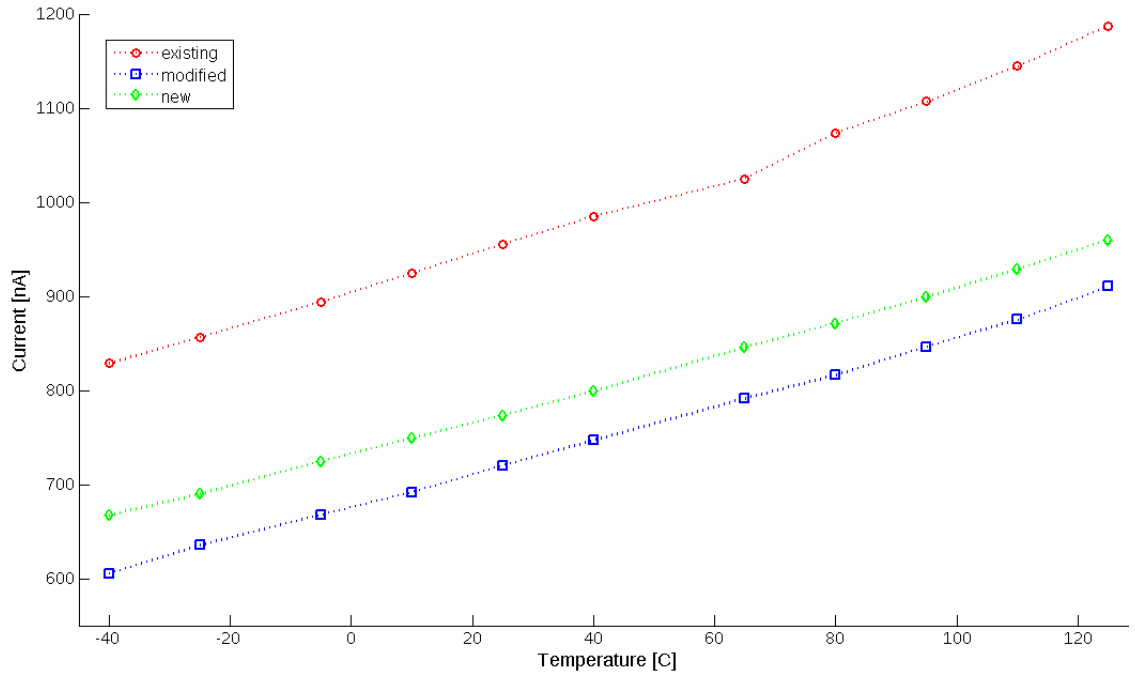

Figure 7.2: Measured current consumption of the regulators versus temperature

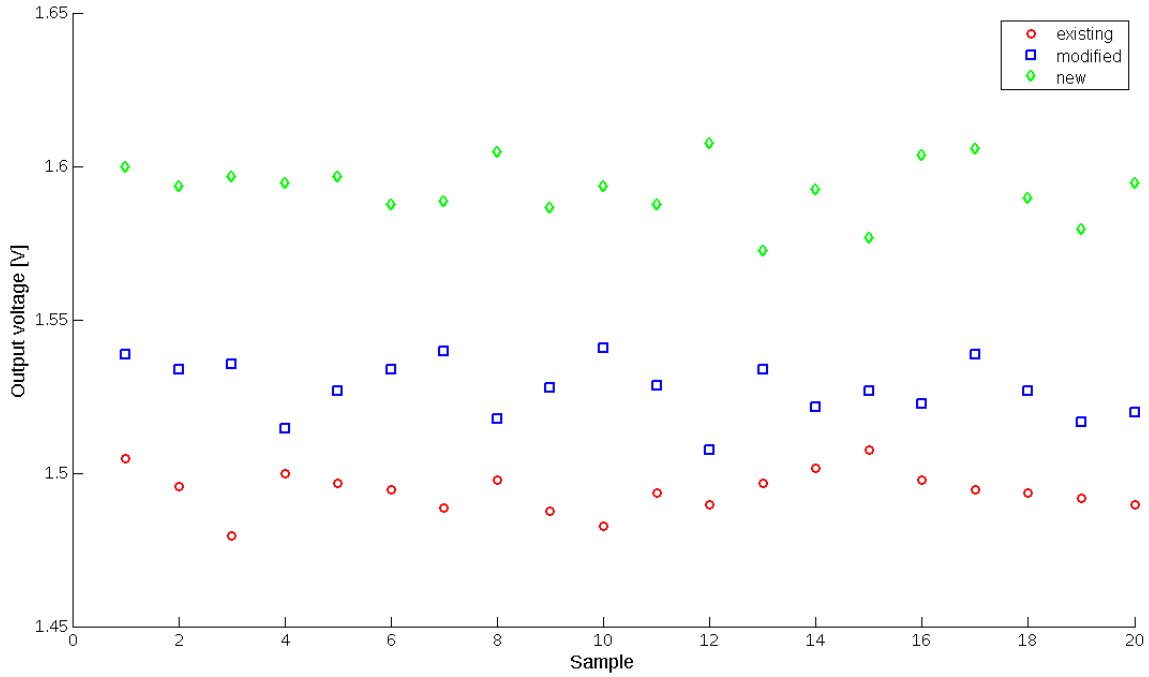

Figure 7.3: Measured output voltages of all samples at 25 °C

Figure 7.3 shows the output voltages of all samples at 25 °C. However, due the limited number of samples, a statistical analysis was omited.

Figure 7.4 shows the current consumption of all samples at 25 °C.

The current consumption in power-down mode was measured with a grounded output pad. For all three regulators, it is below 1 nA for temperatures up to 80 °C. Table 7.1 shows the measured values for higher temperatures.

Table 7.1: Current consumption in power-down mode

Temperature	Existing circuit	Modified circuit	New circuit
95 °C	1.70 nA	1.74 nA	1.59 nA
110 °C	4.12 nA	4.27 nA	4.01 nA
125 °C	9.77 nA	9.83 nA	9.90 nA

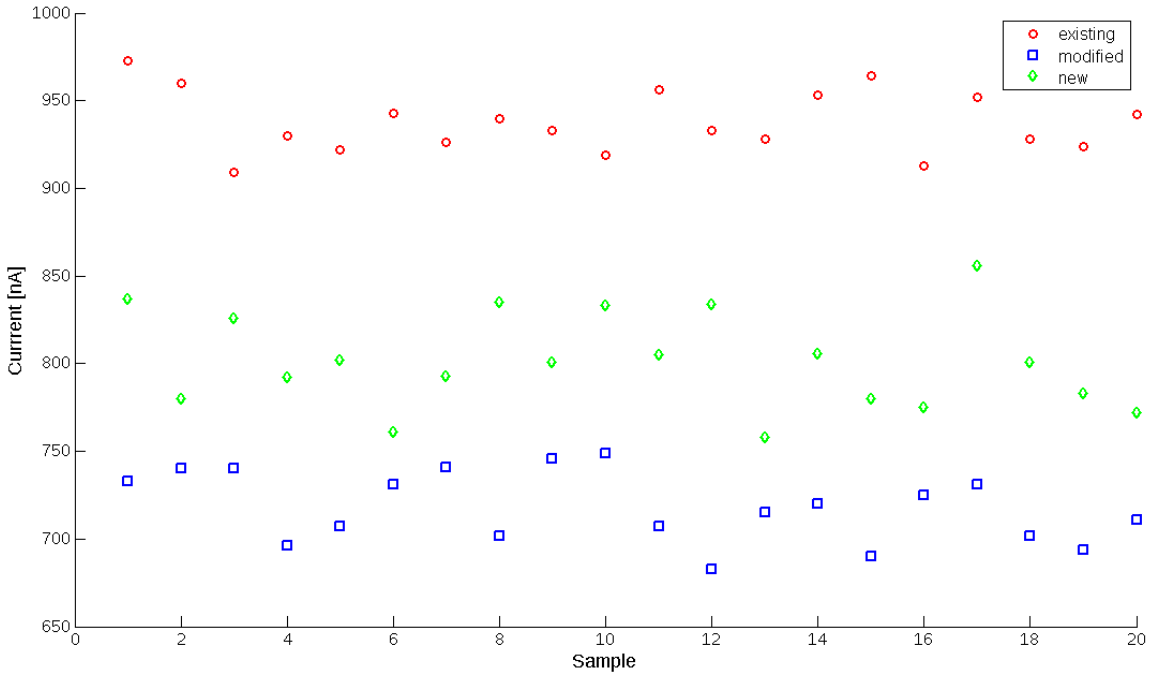

Figure 7.4: Measured current consumption of all samples at 25 °C

7.1.2 Static line and load regulation

The line and load regulation was measured as described in section 3.2.5. Table 7.2 shows the mean value of 4 samples for all three regulators at 25 °C. It was checked whether the values would degenerate at low (40 °C) or high (125 °C) temperatures, however no significant changes could be measured.

Table 7.2: Measured line and load regulation

	Existing	Modified	New	
Line regulation	4.0	4.48	2.9	mV/V
Load regulation	12.9	66.4	44.2	mV/mA

The line regulation is as predicted by the simulations. In contrast, the load regulation is far worse than expected. Surprisingly, the existing regulator shows better load regulation than the new one. The root cause of this degradation is currently unknown. The voltage drop across the bond wires and the external lines on the test-board is assumed to be negligible, due to the small load currents (<100 µA). However, the

absolute output voltage change over the complete load range is sufficiently small for all regulators (<10 mV).

7.2 Transient measurements

All transient measurements were executed only at room temperature (approximately 23 °C). This was done to save time, as the simulation results show only minor differences in overshoot, phase margin and PSRR over the complete temperature range.

A small circuit board with a load resistor and a load capacitor was used. The test-chip was connected to this test-board via a DIP-socket. All parts were placed to each other as close as possible, to keep parasitics small. The output voltage was measured using a voltage buffer, *LF*356 in unity gain configuration, to avoid additional loading of the output. A detailed description of *LF*356 can be found in the datasheet [19].

7.2.1 Overshoot, caused by supply voltage variations

Potential overshoot by fast ramping supply was evaluated by applying a square wave signal to the supply pin. A waveform generator with 50 Ω output impedance was used to generate a signal that ramps up from 0 V to the maximum supply voltage 3.6 V in about 25 ns.

Figure 7.5, 7.6 and 7.7 show the supply voltage applied to the regulators at the top and the according output voltage at the bottom. The plots were done for the operating point, which shows maximum overshoot in the simulations: A resistor of 1.5 MΩ was used to adjust the output current to about 1 µA and a capacitor of 100 pF was used as capacitive load. The plot of the new regulator was recorded with a smaller timescale, due to the regulators' faster start-up and settling time.

Similar to the simulations, it was checked, whether a short interruption of the supply voltage would generate an overshoot of the output voltage. This was evaluated by applying a square wave signal to the supply pin, which ramps up from 0 V to the maximum supply voltage 3.6 V in about 25 ns. The pulse width of the signal was varied to simulate short interruptions of the supply voltage. As predicted by the simulations (see section 5.2.3), the overshoot increases, as the time of the interruption decreases. Table 7.3 shows the observed, worst overshoots of the three regulators, for an off-time of 1 µs. However, it depends on the actual application circuit, whether such short interruptions may appear.

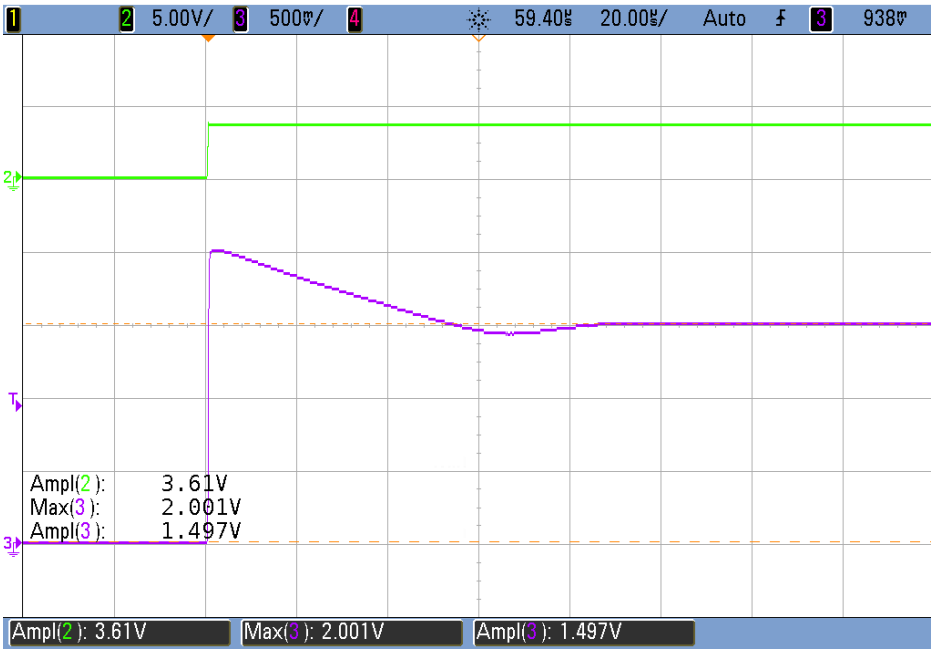

Figure 7.5: Existing regulator: Overshoot of the output voltage due to a fast rising supply voltage.

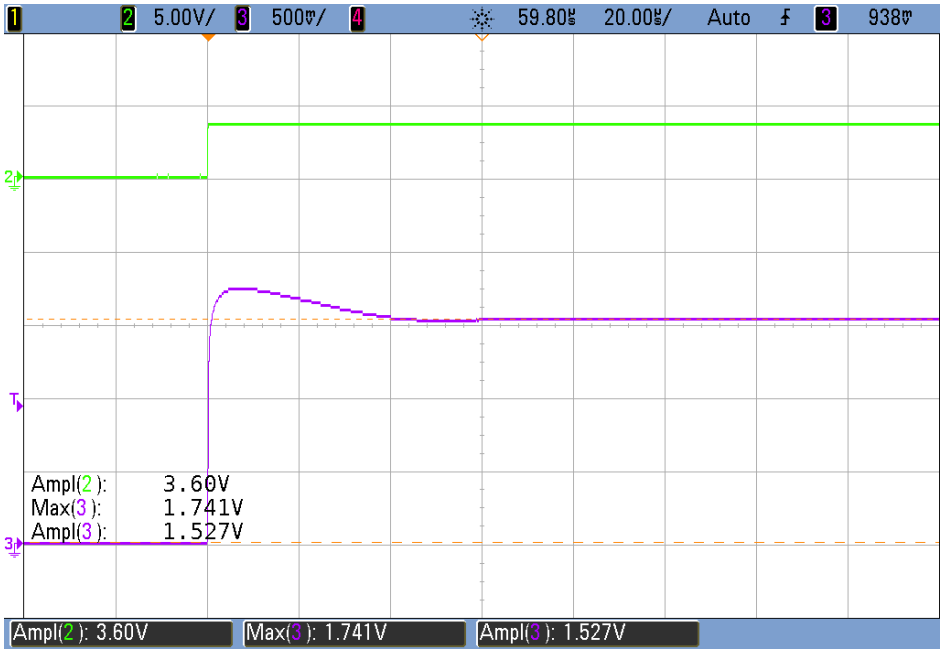

Figure 7.6: Modified regulator: Overshoot of the output voltage due to a fast rising supply voltage.

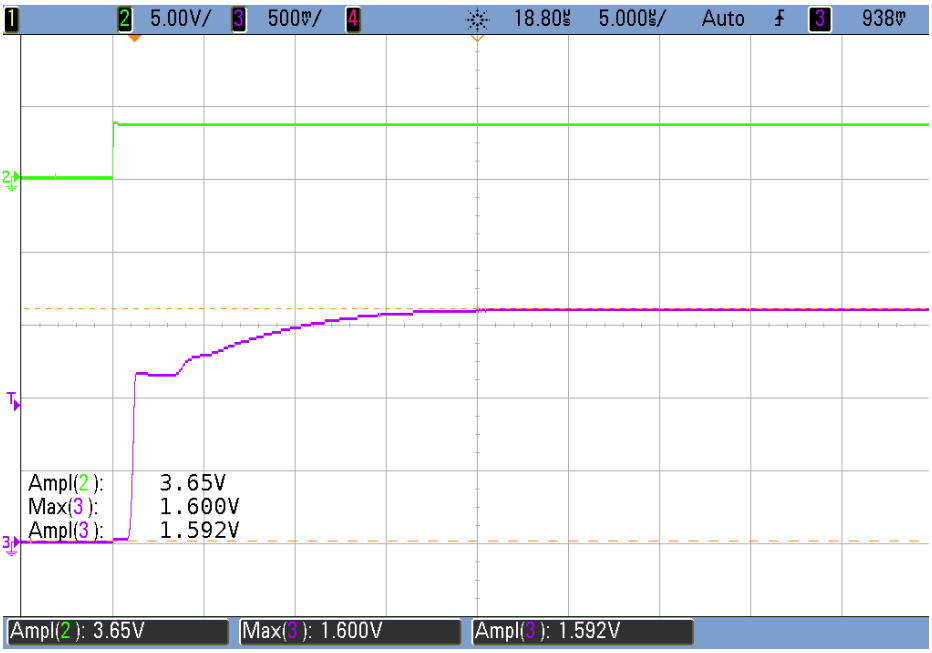

Figure 7.7: New regulator: Overshoot of the output voltage due to a fast rising supply voltage.

Table 7.3: Maximum observed overshoot, caused by interruptions of the supply voltage

Off-time	Existing circuit	Modified circuit	New circuit
1 µs	2.46 V	2.11 V	1.74 V

Finally, it was tested, whether an overshoot would appear if the supply changes from a low voltage to a higher voltage. The existing and the modified regulator show worst overshoot, when the supply is 0.6 V for some time and then ramps up to 3.6 V within 25 ns. In this case, the existing regulator produces an overshoot of **2.60 V**. As the regulator is supposed to power circuits which may potentially be damaged at 2.50 V, this is a knock-out criterion for the existing regulator. The overshoot of the modified regulator was measured as 2.35 V. The new regulator shows worst overshoot, when the supply ramps up to 3.6 V from initially 1.35 V. The overshoot measured was 2.40 V.

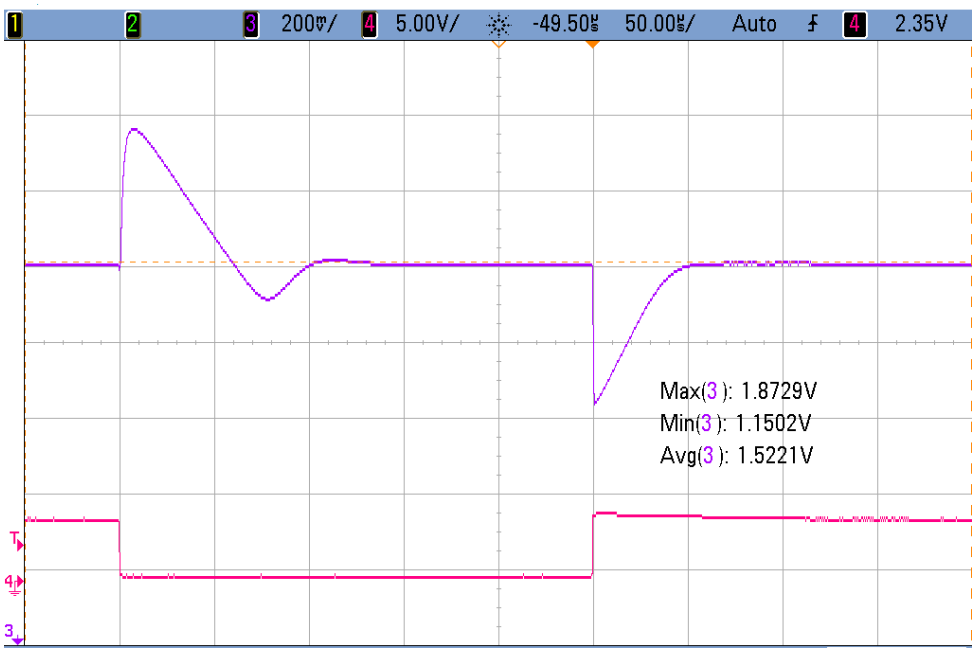

Figure 7.8: Existing regulator: Response of the output voltage to a large load step.

7.2.2 Overshoot, caused by load variations

These measurements were done to observe the ability of the regulators to adapt to large load changes. Highest overshoots of the output voltage occur for small output capacitors. Thus the regulators were loaded with a capacitor of 100 pF. A large resistor of 1.5 MΩ was used to adjust the output current to about 1 µA. A smaller resistor (15 kΩ), was connected between output and ground via a series switch (NMOS BS170). A square wave signal was applied to the gate of this transistor, such that the load current of the regulators switched between 1 µA and 100 µA, which corresponds to a 100 % load jump.

Figure 7.8, 7.9 and 7.10 show the signal at the gate of the transistor at the bottom, a high voltage (5 V) corresponds to a high load current. The output voltage of the according regulator is shown at the top. The new regulator shows a much faster response to the load change. The settling time is approximately four times faster compared to the existing regulator.

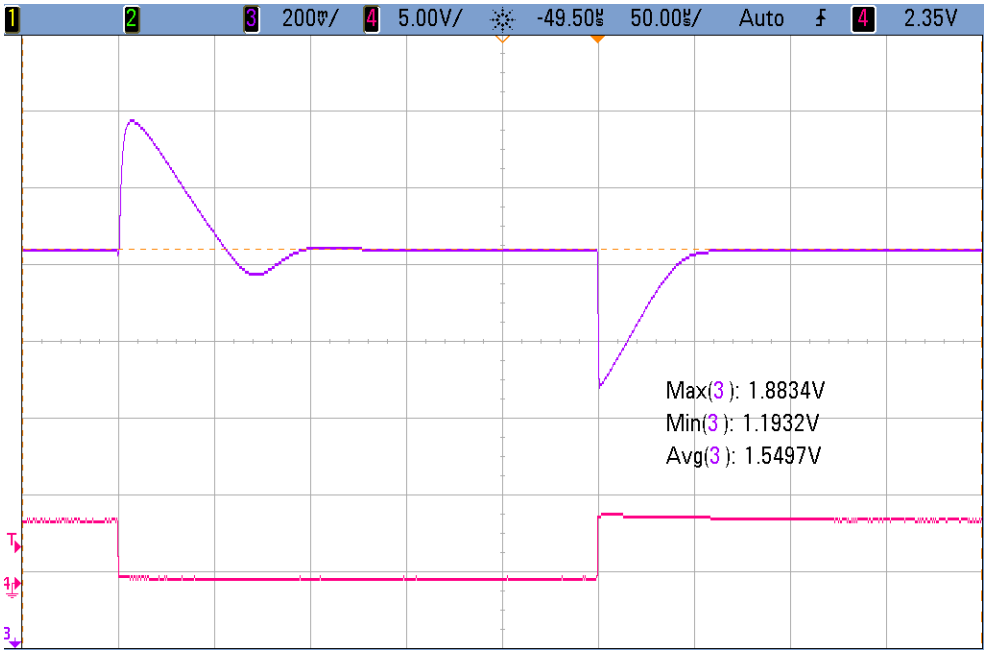

Figure 7.9: Modified regulator: Response of the output voltage to a large load step.

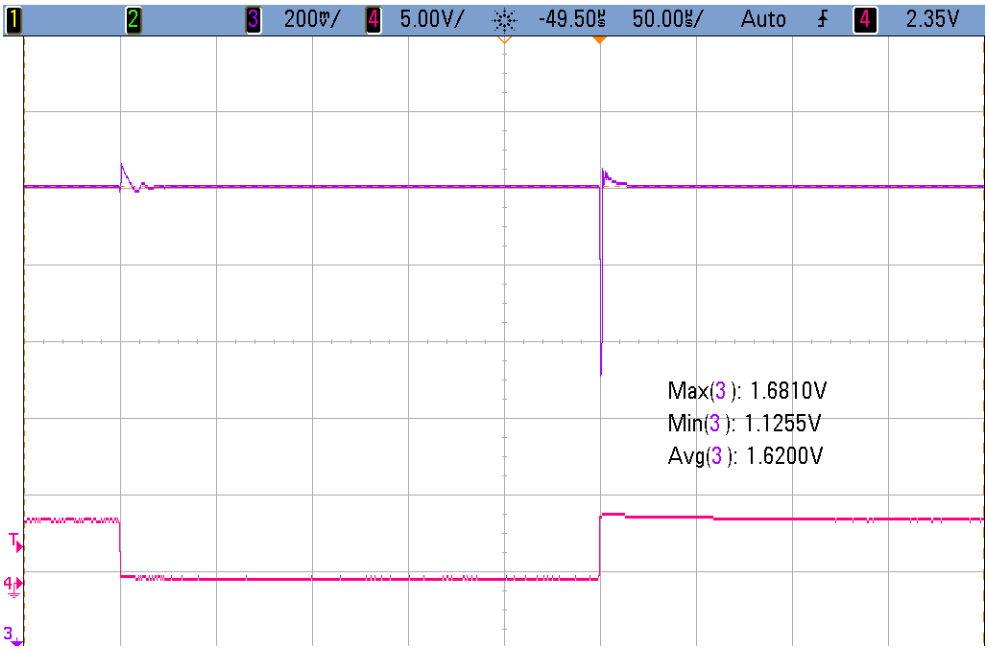

Figure 7.10: New regulator: Response of the output voltage to a large load step.

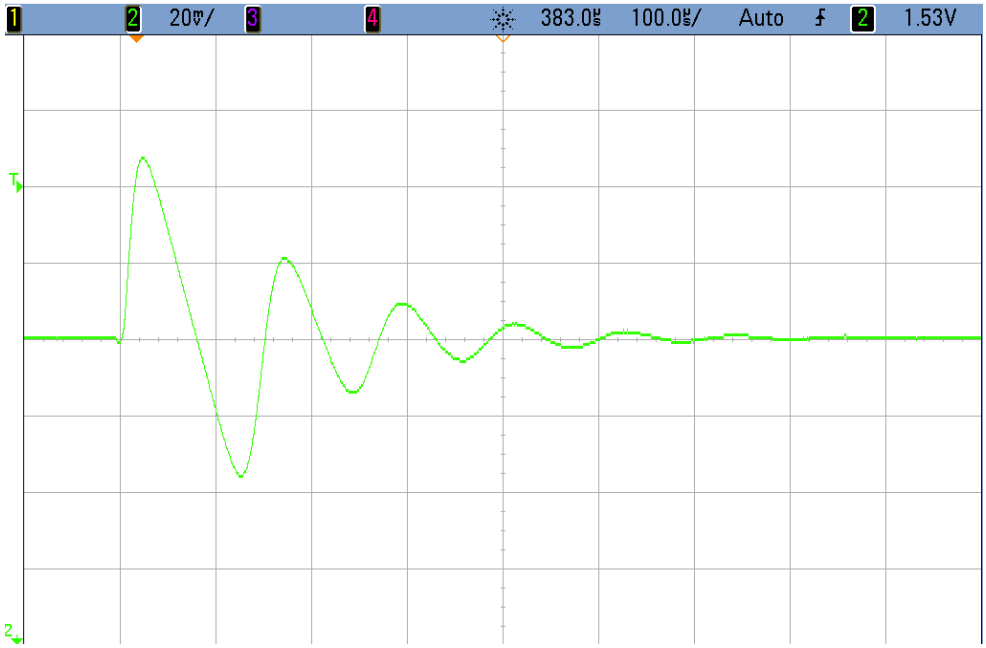

Figure 7.11: Existing regulator: Small signal load step response.

7.2.3 Stability

In order to estimate the minimum phase margin, a small signal load step response measurement was performed. As described by Stevens [27], the ringing of the step response can be related to the phase margin of a voltage regulator. Simulations predicted the minimum phase margin for a supply voltage of 1.8 V, a load capacitor of 1 nF and small current. The measurements were done for this operating point. The current was switched from initially 10 µA to 1 µA to observe a small signal load step response.

Figure 7.11 shows the small signal load step response of the existing regulator for the described operating point. According to Stevens [27] this corresponds to about 9° to 19° phase margin.

Figure 7.12 shows the small signal load step response of the modified regulator for the described operating point. According to Stevens [27] this corresponds to about 19.5° phase margin.

Figure 7.13 shows the small signal load step response of the modified regulator for the described operating point. According to Stevens [27] this corresponds to about 27.5° phase margin.

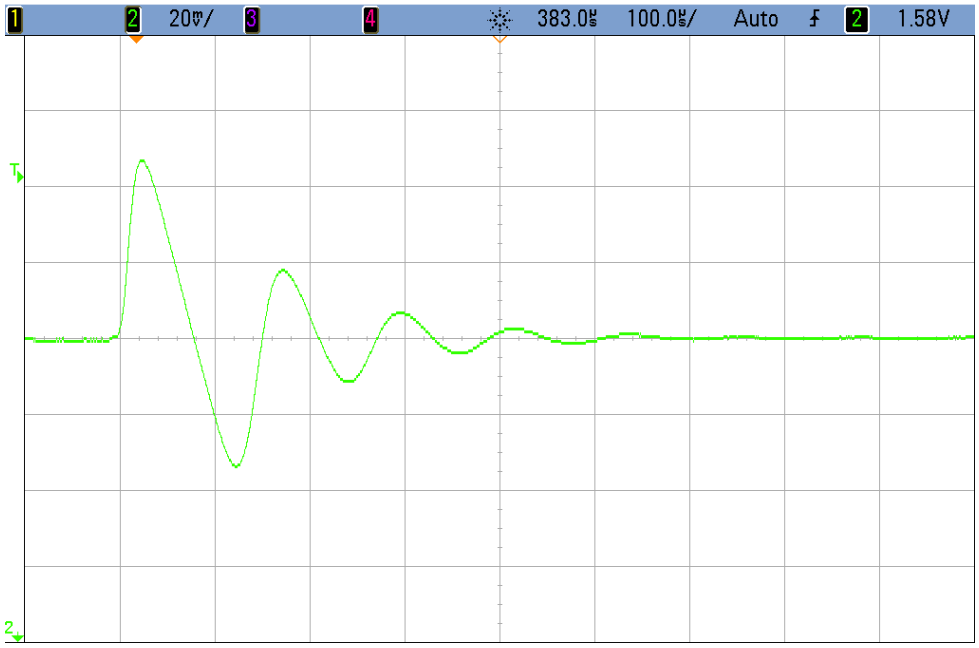

Figure 7.12: Modified regulator: Small signal load step response.

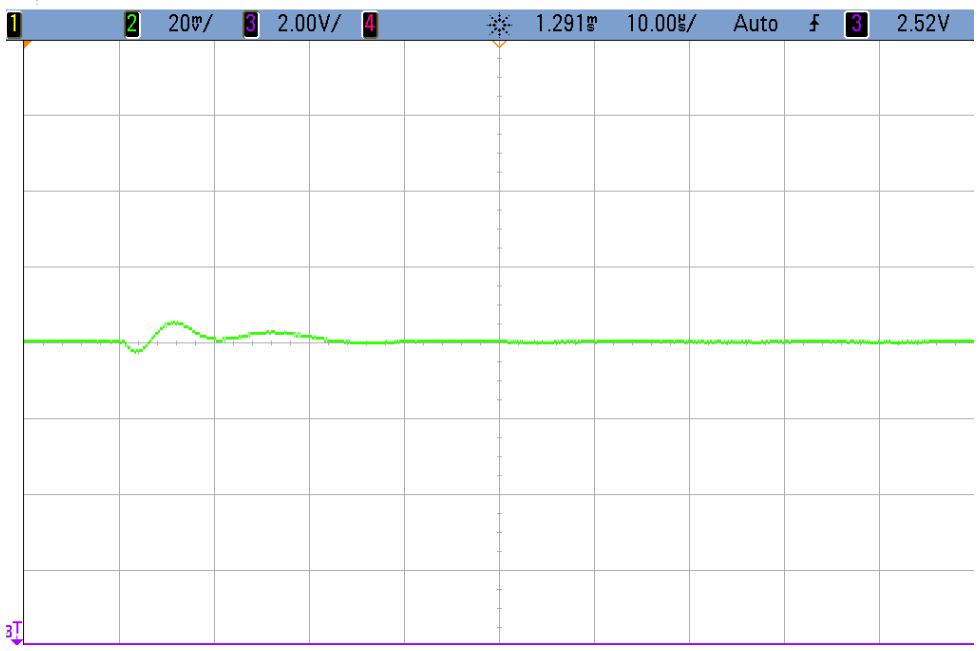

Figure 7.13: New regulator: Small signal load step response.

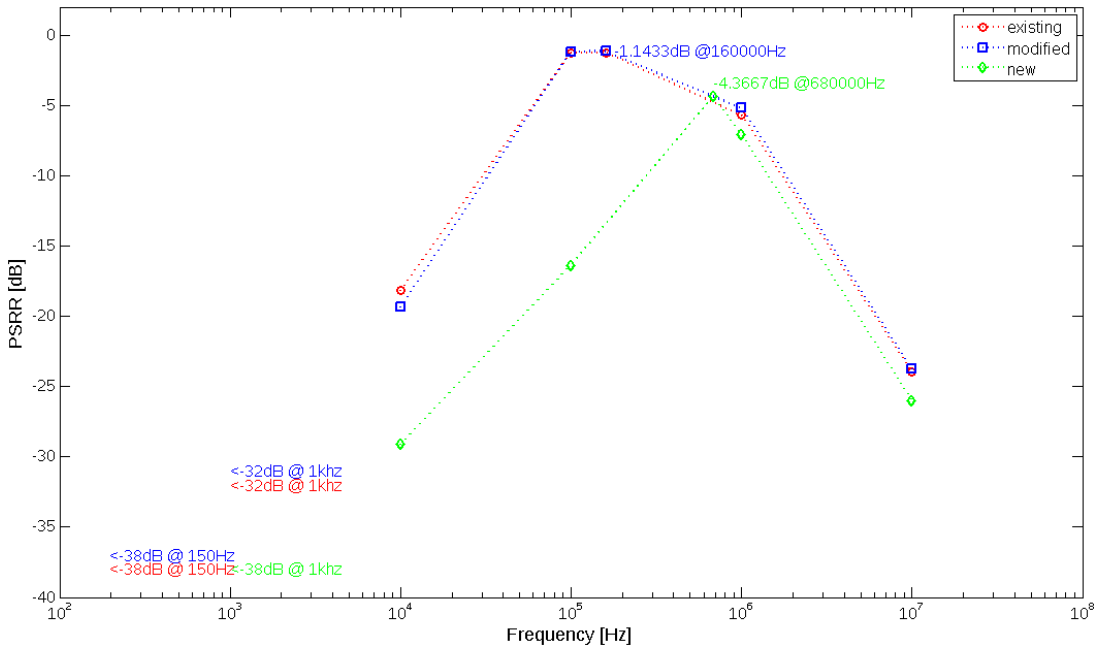

Figure 7.14: PSRR of the regulators, at minimal dropout voltage.

7.3 PSRR

PSRR was measured as described by Pithadia and Lester [24], using a signal generator and an oscilloscope. An AC signal together with a DC offset is applied to the supply pin of the regulator. The voltage ripple on the output is measured with an oscilloscope. PSRR is then calculated via formula 3.15. This measurement is done for different frequencies.

Simulations predicted, that high frequency PSRR will be worst for low input voltages, small load capacitors and small load resistors, where dropout voltage is minimal. Figure 7.14 shows the measured PSRR for this operating point. An AC signal of 200 mV peak to peak, with a DC offset of 1.9 V was used as supply voltage. The load capacitor was 100 pF, the load resistor was 15 kΩ. Due to the resolution of the oscilloscope, accurate measurements were only possible down to −30 dB.

Figure 7.15 shows the PSRR versus frequency for the 3 regulators at typical conditions. The supply voltage was 2.7 V, a load capacitor of 470 pF was used and a load resistor of 30 kΩ adjusted the load current to approximately 50 µA. The PSRR was measured by applying a ripple of 400 mV to the input.

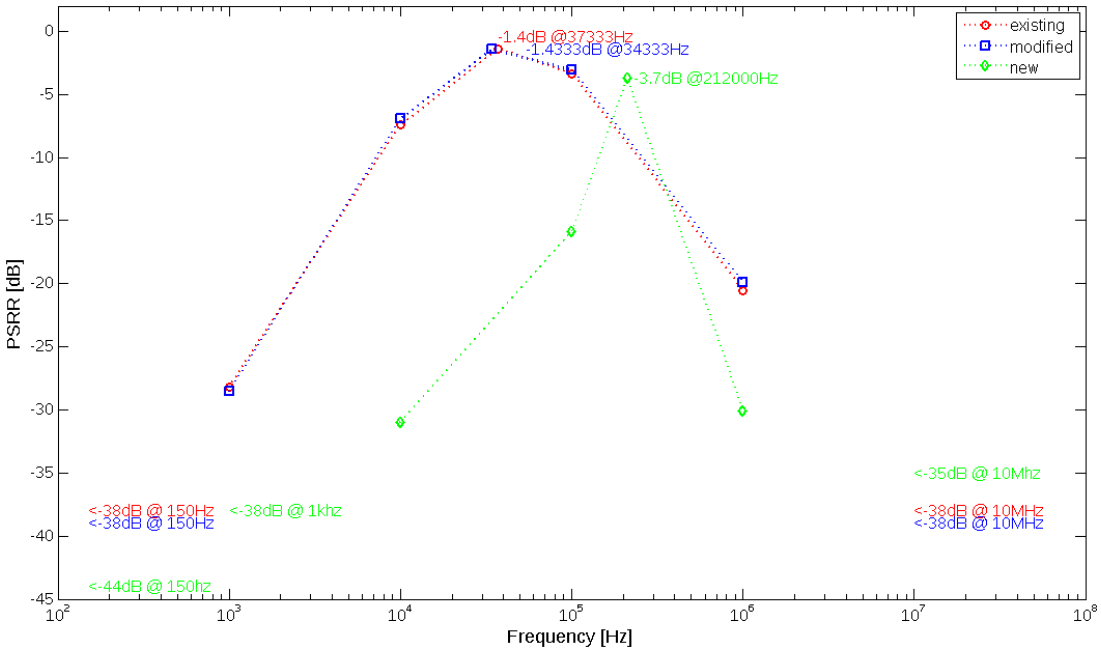

Figure 7.15: PSRR of the regulators, at typical conditions

7.4 Observed issues

7.4.1 No load condition

Although the minimum output current was specified as 1 µA, it was checked whether the regulators are stable in no load conditions. This was done using the setup from section 7.2.3. In this case, an initial current of 10 µA was switched off.

Figures 7.16, 7.17 and 7.18 show the small signal step responses. It can be observed, that the existing regulator shows nearly undamped oscillation. Thus, it can be considered not stable without load. In contrast, the modified regulator may be considered stable, as the ringing of the step response is clearly damped. The step response of the new regulator was difficult to measure, due to the small signal. However, it can be seen, that the step response is damped.

7.4.2 Oscillation of the new regulator

When measuring the PSRR, an unexpected behavior of the new regulator was encountered, when applying a high output current and small load capacitor. At ripple

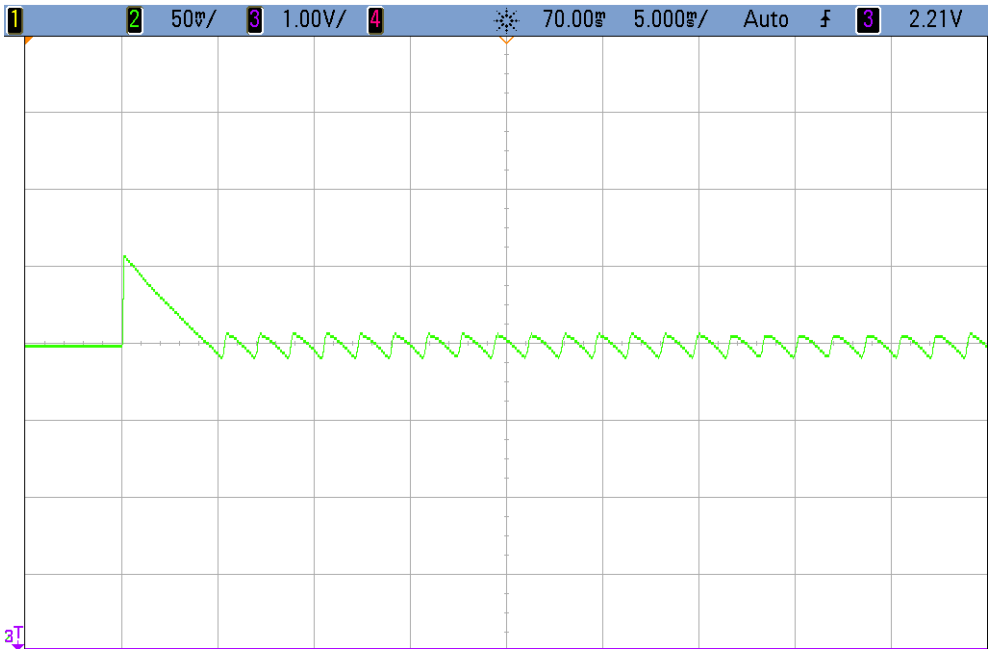

Figure 7.16: Existing regulator: Small signal load step response, no load condition.

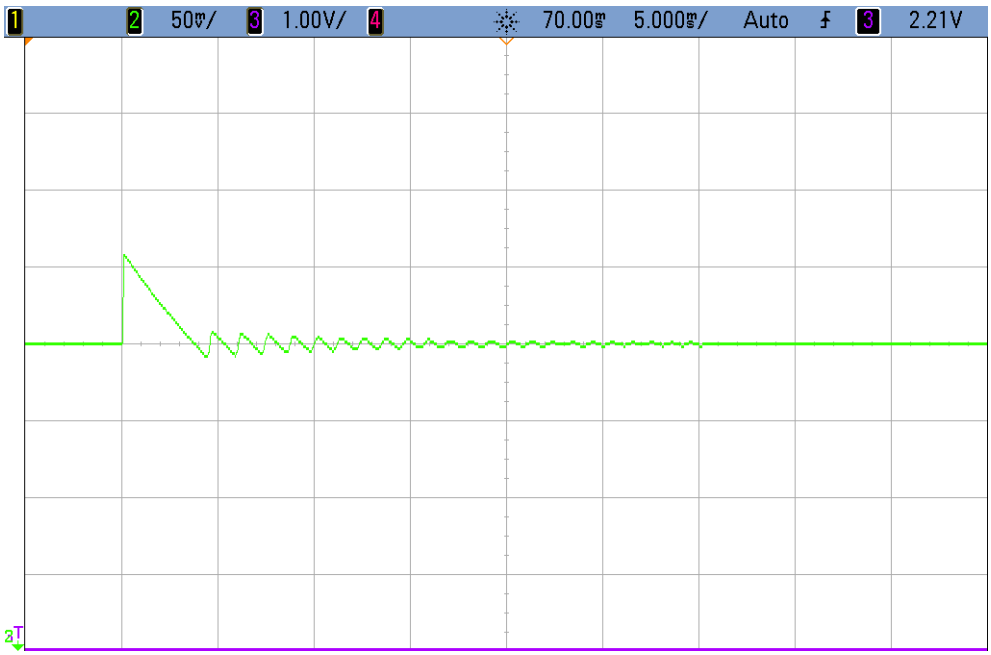

Figure 7.17: Modified regulator: Small signal load step response, no load condition.

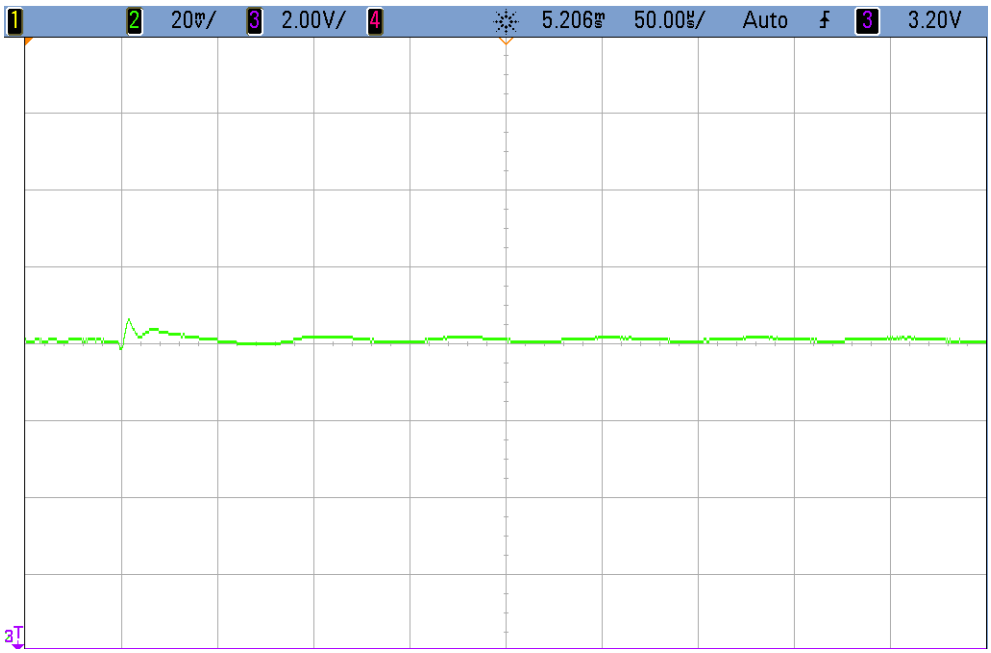

Figure 7.18: New regulator: Small signal load step response, no load condition.

frequencies around 500 kHz (300 kHz to 700 kHz), the PSRR shows a dependency on the ripple amplitude. For input ripples below 0.2 V_{pp} the PSRR behaves as simulated in the AC-Simulations. Higher ripples cause the PSRR to increase significantly. Values up to 6 dB were observed. In that case, the output oscillates with the frequency of the supply ripple.

It was tried to reproduce this behavior in the simulator. Transient simulations revealed the same behavior, while it can not be detected with AC simulations, additionally small-signal stability analysis predict a phase margin higher than 90° for the concerned operating point. Thus, it is assumed, that this behavior is due to the large shifts in the bias conditions. However, further investigation is needed to find the root cause of this issue.

8 Conclusion

Different aspects of LDOs for the use in SOC were analyzed in this work. Some issues, which arise from low current consumption were especially addressed: namely inferior transient behavior, limited bandwidth and degraded PSRR. Additionally a reference current circuit was presented and analyzed in detail.

In the first step, different measures were implemented to improve an existing LDO, without changing the overall topology of the design. As stated in chapter 5.1.5, the slew rate and gain of an OTA which works in weak inversion is in first order independent of its bias current, if the GBW is kept constant. Thus, the current consumption was reduced, while in the same time, the on-chip compensation capacitor was minimized, without degrading the gain or slew rate. Measurements in the laboratory prove, that the regulation behavior and PSRR of the existing LDO and the improved version are nearly identical, while the improved LDO needs significantly less current ($>-20\,\%$). Additionally, the improved version shows a slightly better phase margin, less overshoot at start-up and excellent temperature compensation. The area consumption could be reduced by more than 20 %. The static load regulation of the existing regulator appears to be better in the measurements. However, load regulation was not specified and is not an important criterion when used as a STUP.

In the next step, a literature study was done, to find a LDO topology, which would overcome slew rate and bandwidth limitations. It was decided to employ an error amplifier with a class AB output stage to improve the slew rate and apply Miller-Compensation with Q-Reduction technique to extend the bandwidth of the regulation circuit. This design was than implemented to work with a very small quiescent current (the regulation loop of the LDO consumes about 280 nA at 25°). Simulations showed a 3 to 4 times higher bandwidth together with an improved phase margin compared to the existing LDO. A novel back-gate circuit was employed to compensate the degradation of PSRR at high frequencies due to the small current consumption. The complete LDO needs about 35 % less area on the die, mainly due to reduction of on-chip compensation capacitors. Measurements revealed the improved transient behavior: The LDO does not show overshoot at start-up, the settling time after load jumps is strongly decreased and low frequency PSRR is improved. Additionally, the measured current consumption is approximately 15 % less than for the existing LDO. Thus, it is proven, that the new topology offers significant better voltage regulation, without increasing the current consumption.

However, an open issues of this new design was identified in the laboratory. High supply ripples above 300 kHz cause the LDO to become unstable. Thus, further investigation and design work is needed, in order to use this promising topology in an application.

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