System Design of an Automated Semiconductor Test Equipment for Acceleration Sensor Calibration

Master's Thesis

MA 718

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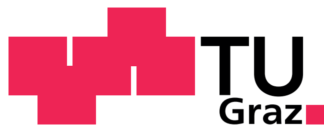

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Abstract

The goal of this thesis is to develop and implement a semiconductor test system for functional testing and calibration of a micromachined accelerometer. This sensor is embedded in a next generation Tire Pressure Monitoring System. Hence automotive standards apply, which also require physical stressing of the device.

Microsensors are mostly fabricated using well known semiconductor processes. Hence they are also subject to the same production deviations. Starting with the description of a standard process for micromachined inertial sensors, the actual need for calibration is derived.

Since the test system is installed in a centrifuge special care is taken of board robustness. Additionally the system is exclusively passive cooled, which requires a low power design. With all requirements and limitations being defined, the system concepts are set up.

The core component of the tester is an embedded system which is running a standard operating system. It is controlling the test execution and calibration process. Different types of such systems are compared and briefly outlined. Furthermore the high parallel device communication and power supply concepts are described.

At the end the most innovative concepts, compared to previous implementations, are selected and described in detail. Especially the device communication and power distribution is discussed in detail. Considering all key facts the current status of the system is outlined and a short outlook on future developments is made.

Keywords: MEMS, MEMS calibration, semiconductor test, micromachining, test system development, embedded system, high parallel communication

Kurzfassung

Ziel dieser Arbeit ist es, ein funktionales Testsystem für einen mikroelektromechanischen Beschleunigungssensor zu entwickeln. Dieser Sensor ist Bestandteil eines Reifendrucksensors der nächsten Generation. Für diesen Einsatzzweck in Kraftfahrzeugen sind daher spezielle Anforderungen zu berücksichtigen, unter anderem, physikalische Belastungstests.

Mikrosensoren werden in den meisten Fällen mittels bekannter Halbleiterprozesse hergestellt und unterliegen daher auch denselben Prozessschwankungen. Ausgehend von einem grundlegenden Standardprozess für Trägheitssensoren, wird die Notwendigkeit einer Kalibrierung abgeleitet.

Der Umstand, dass das Testsystem in einer Zentrifuge montiert wird, ergibt für die Entwicklung zusätzliche Anforderungen. Dazu zählen die Robustheit der Platinen, die Notwendigkeit eines passiv gekühlten Systems und ein geringer Gesamtstromverbrauch.

Die Kernkomponente des Systems stellt ein Embedded System dar, das den Testablauf und die Kalibrierung steuert. Verschiedene derartige Systeme werden verglichen und kurz beschrieben. Besonders die hochparallele Kommunikation und die Spannungsversorgung werden eingehend erklärt.

Schlussendlich wird die Implementierung jener Konzepte erläutert, die einen besonders innovativen Charakter im Vergleich zu vorherigen Systemen darstellen. Speziell die Kommunikation und die Energieverteilung werden detailliert beschrieben. Abschließend wird, unter Berücksichtigung aller Systemkomponenten, der jetzige Status dargestellt und ein Ausblick auf mögliche zukünftige Verbesserungen gegeben.

Schlagwörter: MEMS, MEMS Kalibrierung, Halbleiter Test, Mikrobearbeitung, Testsystem Entwicklung, eingebettetes System, Hochparallele Kommunikation

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List of Abbreviations

ABS Anti-Lock Braking System

ADC Analog-to-Digital-Converter

AEC Automotive Electronics Council

API Application Programming Interface

ASIC Application Specific Integrated Circuit

ATE Automatic Test Equipment

BE Backend

BGA Ball Grid Array

COM Computer-On-Module

CPLD Complex Programmable Logic Device

CPU Central Processing Unit

CVD Chemical Vapor Deposition

DAC Digital-to-Analog Converter

DfM Design for Maintainability

DUT Device Under Test

EDA Electronic Design Automation

ESD Electrostatic Discharge

ESP Electronic Stability Program

ETX Embedded Technology eXtended

List of Abbreviations

ETX-IG Embedded Technology eXtended Industrial Group

FIFO First In First Out

FPGA Field Programmable Gate Array

I2C Inter-Integrated Circuit

IC Integrated Circuit

ISA Industry Standard Architecture

JEITA Japan Electronics and Information Technology Industries Association

JTAG Joint Test Action Group

LDO Low-Dropout

MEMS Microelectromechanical Systems

PAT Part Average Testing

PCB Printed Circuit Board

PCIe Peripheral Component Interconnect Express

PICMG PCI Industrial Computer Manufacturers Group

PSG Phosphosilicateglass

RAM Random Access Memory

RF Radio Frequency

SGET Standardization Group for Embedded Technologies

SMBus System Monitoring Bus

SPI Serial Peripheral Interface

TPMS Tire Pressure Monitoring System

UART Universal Asynchronous Receiver Transmitter

1 Introduction

When the first Integrated Circuits (ICs) were built back in the 1950s nobody would have thought that this is the start of a new and promising era of technology. With continuous improvements and innovations those devices became more powerful yet decreasing their size even more. A little more than sixty years later many things have evolved - from the development to the applications.

Testing semiconductor devices in the early days was more tokenistic - if there was some testing at all. There was no real test equipment available and verification was merely done on a ”looks good” basis. Over the years this has evolved via measuring basic device functionality to test systems with nearly the same degree of complexity as the tested device itself. Therefore Automatic Test Equipments (ATEs) have taken up an integral position within the whole development and production process of an IC.

In today’s semiconductor market many things have to be considered to fulfill the costumer’s expectations. While maintaining the highest possible level of quality and integration the price needs to be low enough to stay competitive. This is where the work of a semiconductor test engineer starts. He has to develop the necessary hardware and software in order to assure the tested device at least satisfies the datasheet. This leads to the always reoccurring keywords in a test engineer’ s every day life: **yield**, **test time** and **quality**.

In general **yield** is defined as the ratio between the number of acceptable and the fabricated parts. As soon as only one test out of hundreds is failing the device is assumed to be non-acceptable, a so called fail part. Therefore it is desirable that the tests by no means detract the yield. Also the devices themselves are developed in a way that they withstand more than what is

promised in the specification. Therefore many integrated circuits are largely over-engineered in order to also reduce yield loss.

The **test time** is always calculated per device. Since tests are performed in parallel on multiple DUTs the time of the whole test run is divided by the number of devices tested at the same time. Taking this into account the test time will only reduce if the number of devices tested in parallel is increased or the execution time of one single test is decreased. In modern ATEs the parallelism is inherently supported by the measurement instruments (which exist multiple times) and the software framework. Thus it makes nearly no time difference if two or ten devices are tested.

For test engineering **quality** is something harder to measure than the yield or test time. The outgoing quality is always expected to be the highest possible. Starting from the project leader all the way to the end customer. Today everything is expected to work - forever - without any issues. But we are in a real world where things just go wrong for whatever reason.

So when it comes to quality everything being feasible has to be done to ensure any device leaving the company will do it's job as it is stated in the datasheet. The testing circuit should be close to the field application, all use cases should be covered by the test program and all devices suffering from "infant mortality" should be rejected. But these are just some examples. In the end it always has to be clear that the test hardware and the test program will be the last ones being able to detect faulty behavior before the DUTs become "electronic devices".

2 Motivation

As already outlined in the introduction the three key factors of success for test engineering are yield, test time and quality. In addition they all need to be implemented in a cost effective way since this is one of the main requirements to stay competitive on today's semiconductor market.

The DUT being tested with the developed system is a next-generation Tire Pressure Monitoring System (TPMS) device. It comprises of micromachined pressure and acceleration sensors which are interfaced with an Application Specific Integrated Circuit (ASIC) for signal conditioning. Additionally a microcontroller core is included that also provides various wired and wireless communication channels. The device is tailored towards the need of automotive supply industry in order to fulfill the latest legislation for example in the EU, USA or Japan.

When talking about quality in the automotive industry there are also many standards and regulations that must be complied with. Many integrated circuits in modern cars are used in areas that are directly influencing passenger safety like Anti-Lock Braking System (ABS) sensors, airbag trigger devices and similar. Additionally they are often directly exposed to a harsh environment and still need to perform their functions properly.

High parallelism, so called multisite testing, is an appropriate measure to reduce test time and therefore overall test cost. Considering that in nowadays' automotive products the test cost per device is equally high as the fabrication itself special care has to be taken about economical feasibility. Therefore when developing the test hardware for a new product the maximum possible parallelism of the test system being used or developed is a main consideration. Sometimes even a new ATE platform needs to be acquired in order to cope with the new test challenges

Unfortunately standard ATEs do not provide out-of-the-box features to simulate those environmental conditions like pressure, temperature or acceleration. Hence special equipment needs to be developed in order to fulfill customer requirements and automotive safety standards by the likes of Automotive Electronics Council (AEC) or Japan Electronics and Information Technology Industries Association (JEITA). Given that such a system also needs to be economically feasible, a trade-off has to be found between precision and cost.

The system developed during this thesis is used to ensure proper device functionality at high g-forces. The DUT will be accelerated up to 100g and being calibrated for that value. It is a functional tester that is designed to fulfill the requirements given by the standards and the customers. As an additional challenge the whole test system is mounted within a centrifuge hence special requirements regards board robustness are given.

This thesis first outlines the technology behind an accelerometer and why it is necessary to calibrate at all. Afterwards the concept behind the test system is discussed. Requirements for the implementation are set up and specified in detail. In the end the most challenging parts of the actual implementation are described.

3 MEMS Technology

Microelectromechanical Systems (MEMS) are devices containing electrical and mechanical components miniaturized down to the size of an IC. Such systems are already known for a long time and individual developments can be traced back to the early 20th century.

This chapter will briefly trace back those systems to their roots and give a short overview on applications and current developments. As in the course of this thesis a test system for accelerometer testing was built, a deeper look will be made on inertial sensors. This includes fabrication and its challenges as well as the testing and calibration of such devices.

3.1 Overview

As MEMS are a very diverse field of technology the following section will shortly give an overview on the historical roots. Additionally the types and applications of such systems will be described.

3.1.1 Types and applications

Research on the roots and history of MEMS showed up that there is no definite date when those systems really were invented. Common interest has kicked of in the mid 1980s where a lot of essential development was done. Since MEMS incorporate key technologies of humankind, their actual historical roots split up here.

There are three key components of such a system: Mechanics, miniaturization and microelectronics [Fuj97]. The first two can be traced back to the

middle ages where fine mechanics came to life. So they are known for quite a long time, but thinking about further use started not before sometime in the middle of the second industrial revolution. Rapid evolution of the third technology, microelectronics, has finally brought life into the development of MEMS as we know them today.

Many historical reviews also mention the lecture *There's Plenty of Room at the Bottom* by Richard Feynman that he held in the year of 1959. It notably influenced later developments in the field of microsystems and nanotechnology. He was one of the first to declare that in the future it will be absolutely necessary to miniaturize systems, in particular computers [Fey92].

Looking at computers and systems today we seem to have reached what Feynman was outlining more than 50 years ago. In terms of MEMS, existing technologies from the semiconductor industry are used that are already proven and well established. Being able to implement mechanical components onto a small piece of silicon alongside with microelectronic circuitry really unleashed the power of MEMS. In fact they paved the way for a new kind of environmental interaction for ICs.

Considering that a lot of development and research kick-started only a little more than 25 years ago the progress in this field is really outstanding and still does not seem to flatten. Today there are also many types of different integrated sensors available. Such so called *intelligent sensors* are packaged together with their electronic processing circuitry in a tiny IC package. This kind of development is essential for the feature-set of many ICs today.

3.1.2 Categorization and applications

As diverse as is the history of MEMS also the applications of such systems nowadays seem to be endless. Especially the triumphal procession of smart phones a few years ago made everybody carry around a bunch of different miniaturized sensors in his or her pocket.

In general MEMS can be categorized into **microsensors** and **microactuators**. These two are obviously the microscopic counterparts of sensors and

actuators. While a sensor will transform a non-electrical quantity into an electrical signal the actuator does the converse.

Development in the direction of MEMS has gone further than accepting that a sensor would transform a sensed value into an electrical signal. Because miniaturization also requires to understand new physical effects those two types should be grouped together and be seen as transducers. In fact there is no *the* way to categorize these systems.

Often MEMS are grouped by application or the market they are primarily used in. After research the probably best way seems to describe their features by grouping them together by their primary energy domain. According to [KP05, p. 3] these are:

- Mechanical
- Electrical
- Thermal
- Magnetic
- Radiant
- Chemical

Given that all MEMS are transducers in one or the other way overall classification now gets easier.

Actuators

Actuators are translating energy into mechanical form. In many cases this output can then again be used to influence another non-mechanical signal or energy. They are currently being used to build up a wide range of applications. There are optical switches using movable mirrors, Radio Frequency (RF) switches or microvalves for controlling flow of gas and liquids [Fuj07]. Recent developments also include a complete brushless DC micromotor using special multilayer coils to achieve high performance [MKP09].

One of the commercially probably most successful implementations of a microactuator is the printhead of an inkjet printer [Bou11]. It consists of small MEMS nozzles to control ink ejection onto the paper.

In fact there are also other, more pervasive and invasive actuators that one could think of in the area of medical engineering. Research and development is already ongoing for MEMS that would help with critical micro surgeries inside the human heart [Gos+12].

Within this area of medical engineering there clearly is a strong trend towards special microsensors. Unfortunately they currently seem to suffer from the same issues when it comes to enter the market: finding partners willing to invest into such new technologies [Lam12]. For example performing an in-situ measurement of blood pressure would allow for constant monitoring while not hindering the patient's every day life [Cho+10].

Sensors

Sensors and especially microsensors have changed the world in the last few years. Starting from legislation that would require every new car to have a TPMS all the way to the omnipresent smartphones.

Sensors are generally translating any sensed energy into the electrical domain. Considering the classification given before there are many microsensors that can be thought of. Following the four currently most successful ones which will be further described afterwards [Bou11]:

- Pressure sensors
- Microbolometers
- Accelerometers
- Gyroscopes

One main contributor to the rising request for **pressure sensors** is the latest EU legislation that requires every new car platform to include a TPMS. Those systems are used in order to reduce accidents caused by defective or under-inflated tires. In this special case a microelectronic circuit is used for interfacing the sensor. It consists of a membrane that is deflected depending on the applied pressure. Naturally those systems are considered to be more complex since at least one part of the membrane needs to have contact with the probably harsh environment [KP05, p. 550]. First developments can be

traced back to the 1950s and thus were the first ever micromachined sensors with a very mature technology today [GV01, p. 257].

Microbolometers are the miniaturized version of the already long known bolometers. These sensors are resistors that are sensitive for thermal radiation and thus make it possible, if used in an array, to generate a thermal picture of the environment. The macroscopic version of bolometers have always been suffering from their large thermal capacity compared to photon detectors. This considerably increased the response time on temperature changes which made them not an option for infrared cameras. Through miniaturization, bolometers do no longer suffer from these high response times and are now used in panel arrays for uncooled infrared detectors [KP05, p. 236].

Considering the evolution on the mobile market **accelerometers** and **gyroscopes** have considerably increased their share in the market. These two types are both sensing inertial forces and are in most cases used side-by-side within an application circuit. Accelerometers are sensitive for a change in speed, the acceleration, whereas gyroscopes are sensing the change in rotation. Inertial forces are the driving key behind both types hence they are grouped together as inertial sensors.

Basic principle for both sensors is, as the name already suggests, the mass inertia. Accelerometers are built using a cantilever based mass that deflects on the levitating end due to inertial forces. This deflection is sensed by either a capacitive or piezoresistive measurement [GV01, p. 263]. For gyroscopes a similar concept is used although it consists of oscillating masses that are deflected because of the coriolis force. This derivation from the oscillation direction can then be detected using capactive sensing [KP05, p. 549].

While before these sensors have mainly been used in the automotive area they are now omnipresent due to high usage in smartphones and similar devices. Usage in cars makes up around 80% of the overall MEMS accelerometer market [Kem11, p. 7]. Applications there include, but are not limited to, ABS, Electronic Stability Program (ESP), airbag triggering and also inertial navigation.

3.2 Micromachining

As it was outlined in the previous section 3.1 there is a very diverse field of applications for MEMS. Although fabrication of such micromachines is very similar in many cases the main focus in this section will be on the production of inertial sensors.

MEMS' success was substantially enhanced through the evolution in microelectronic fabrication processes. Those IC processes did evolve over a long time in volume production and thus made it possible to establish a large area of expertise around them. Such fabrication technologies are relatively cheap to be sustained or adapted compared to the cost of a complete new process or fabrication line for MEMS alone [Kem11, p. 152].

In general the production of MEMS based on microelectronic technologies can be divided into two different base categories: **surface** and **bulk** [Bee04, p. 3]. The former is describing the techniques where thin film layers are processed onto the wafer and then partially removed in order to build the structures. This technology was first used back in the 1960 where also first experiments with metallic layers were made. The latter technology is working in the other direction and removes significant parts of the substrate (also called bulk) for building the microstructures [KP05, p. 805].

Especially for fabrication of accelerometers the so called poly-silicon based surface micromachining is used nowadays. In the beginning of inertial microsensor production also bulk technology was used but surface micromaching provided more robust sensors [Gad05, p. 2.16].

3.2.1 Basic process

As mentioned before a significant amount of inertial sensors built is using surface technologies nowadays. Therefore this technology will be further analyzed and its basic process sequence is outlined. Every step will be shortly described and possible problems are discussed.

For the following descriptions general semiconductor processing steps as lithography or implant are either implied or skipped. Also the layers to measure the beam's deflection, like a resistor pickup array, is not considered in this section.

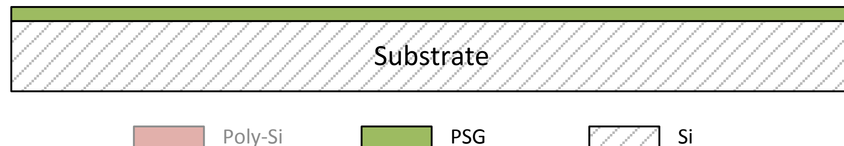

Figure 3.1: Deposited spacer layer ([cf. Gad05])

Processing sequence as depicted in figure 3.1 starts with the deposition of a Phosphosilicateglass (PSG) layer in a Chemical Vapor Deposition (CVD) process. It will serve as the sacrificial or spacing layer for building the free standing micromechanical element. PSG is a SiO_2 layer doped with phosphorous and having a significantly higher etch rate compared to plain SiO_2 [MSH92] [Poe+94]. Because of the characteristics of PSG etching will still not be perfectly uniform and thus it must be densified using a dedicated furnace process with high oxygen concentration at temperatures around 900 °C [Gad10, p. 3.130].

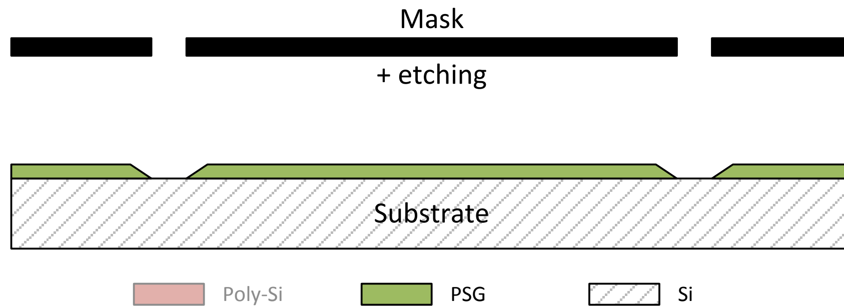

Figure 3.2: Masked removal of parts of the sacrifical layer ([cf. Gad05])

As a second step the previously deposited and densified PSG will be masked in a lithography step and parts being removed as depicted in figure 3.2. This builds the basis for the future mechanical element.

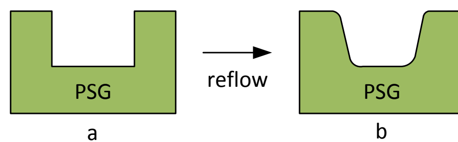

Figure 3.3: Changes made to trench with reflow process

The edges made during etching of the masked layer are usually around 90 °C as depicted in figure 3.3a. This could result in cracks in layers being deposited later on [Ang09, p. 10]. To avoid this a special reflow process is needed afterwards that is smoothing the edges as it can be seen in figure 3.3b [Gad10, p. 3.132].

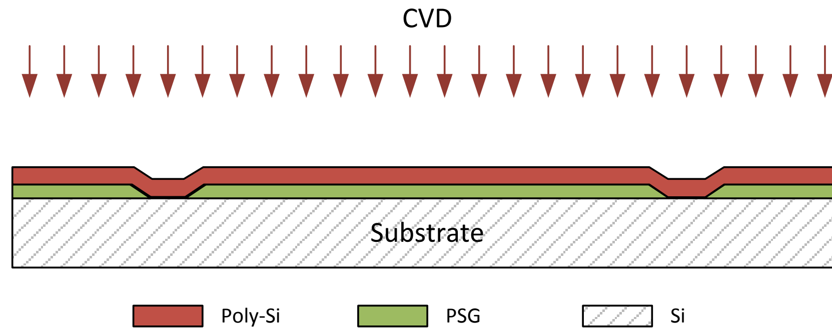

Figure 3.4: Process building poly-Si layer for the structural element ([cf. Gad05])

In the third step the actual poly silicon layer as depicted in figure 3.4 is deposited on the sacrificial layer. This layer represents the structural element for the mechanical part of the MEMS. In recent years this layer was mostly created using an epitaxial instead of a CVD process. It allows to build structural elements having higher aspect rations [Gad05, p. 2.16].

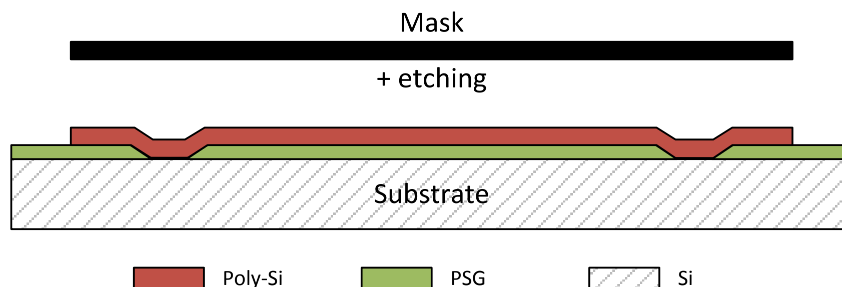

Figure 3.5: Trimming of structural element ([cf. Gad05])

After deposition of the structural layer the next step is to trim it to its final geometry as shown in figure 3.5. This again is achieved through a lithographic and an etching process.

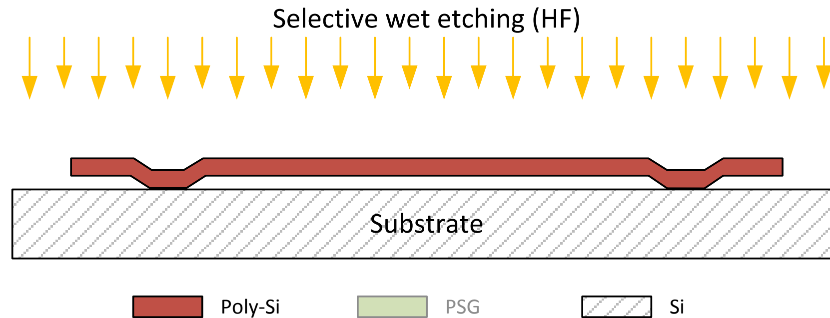

Figure 3.6: Final removal of sacrificial layer ([cf. Gad05])

In the last step depicted in figure 3.6, the sacrificial layer that is still supporting the mechanical element will be removed. This is now done using a wet etching process incorporating hydrofluoric acid (*HF*) [Gad10, p. 3.134]. Undercutting the structural element involves risk of also removing too much of the poly silicon layer. Given that HF is attacking all materials it is mainly controllable through exposure time and selectivity of certain materials. For PSG, thicker layers and higher concentration of phosphorous significantly decrease etching time compared to the structural poly-Si [MSH92].

3.2.2 Challenges

As for every process at micron or submicron level physics brings in unwanted effects. These very challenging problems need to be coped with in a sometimes very creative way. The most common problems arising with the standard process [Gad05, p. 2.17] described in section 3.2.1 are outlined below.

Stiction

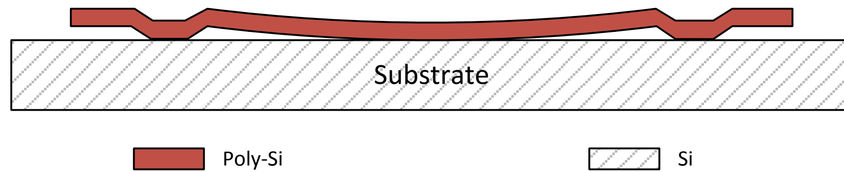

Figure 3.7: Result of release stiction

After removal of the sacrifical layer using wet etching a cleaning process is needed to remove any residual etchant. Because of the drying water capillary forces push the levitating layer towards its adjacent surfaces as depicted in 3.7. Due to the van der Waals' force between those two layers they are firmly kept together [Gad05, p. 2.18]. This is also known as *release stiction*.

This type of stiction is quite well under control these days. Currently implemented measures in order to reduce this effect include using liquids with low surface tension for the cleaning. Another countermeasure is to provide a temporary support under the beam that gets removed after the drying [Tas+96].

Stiction may also occur during normal device operation. There are two possible causes for this - electrostatic pull-down and acceleration push-down [Tas+96]. The former is caused if the capacitance and thus its resulting electrostatic force between substrate and beam is larger than the restoring elastic force. Push-down caused by too high acceleration would also result in a collapse of the beam and make the sensor unusable.

For both of the above mentioned causes there are some considerations to avoid beam contact during operation. This includes thickness and length of the poly silicon layer and also distance between beam and substrate that needs to be taken care of at design-time. Additional damping of the cantilever structure can be achieved by sealing the sensor and filling it with special gas.

Sealing and packaging

Given that the cantilever beam itself is very sensitive to its environment it is obvious that it needs to be hermetically sealed. This facilitates calibration and handling after wafer level processing [Gad05, p. 2.19] [Gad10, p. 3.141].

A lot of research is ongoing in this specific area of MEMS. In general there are three potential sealing methods [Can+03]:

- Using generic packages and careful handling
- Attaching separate finish on top of a single device
- Deposition of a sealing layer at wafer level

Considering costs and resulting device quality, wafer level deposition of an encapsulation layer seems to be used in most of the cases. Nowadays many new MEMS sensors also require a high vacuum and therefore a high quality hermetic sealing [TLC07].

Geometric variation

As for every semiconductor there is a certain probability of perspective distortion that also comes in as a negative side effect for micromachined devices. Especially for poly silicon based resonators the frequency is directly proportional to the width and length of the beam [Gad10, p. 3.141].

Due to the variations in the lithographic processes Gad-el-Hak proposes an approximately 5% uncertainty in the resulting resonant frequency of the beam for a very common deviation of 10 % in size. Furthermore he states that this variation will require a calibration after packaging.

3.3 Pickup principles

In this section the possibilities to actually measure the value of the accelerometer's beam deflection are shortly described. Considering a process as given in section 3.2.1 there are mainly two used methods [Gad05, p. 2.11] - **piezoresistive** and **capactive** sensing.

There are also four other methods available that are under intense research and are worth mentioning: resonant frequency shifting, floating gate FET sensing, FET strain sensing and tunneling-based sensing. Unfortunately they have proven to be complicated to implement in a semiconductor volume processes and are too sensitive on the environmental conditions for most applications [Gad05, p. 2.11].

3.3.1 Piezoresistive sensing

As the name already suggests sensing in this case is based on the piezoresistive effect. As discovered in section 3.1.2 this principle has already been used for years in pressure sensors. Therefore it has also been adopted for the first accelerometers and was successfully applied for years [Gad05, p. 2.11].

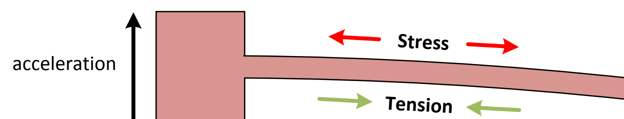

Figure 3.8: Piezoresistive cantilever beam

The effect relies on the fact that materials under either tension or stress are changing their resistance. As it can be seen in figure 3.8 the inertia bends the beam down thus resulting in the top surface being stressed and the bottom side being compressed. Silicon shows relatively large changes in resistance compared to its geometric deformation. Especially films deposited using

plasma enhanced CVD processes show a strong piezoresistive response as stated by [Alp+11].

First experiments on this effect have been made in the 1920s by Percy Bridgman [Bri22]. So it can be considered as well known and understood to be broadly used for sensing applications.

3.3.2 Capacitive sensing

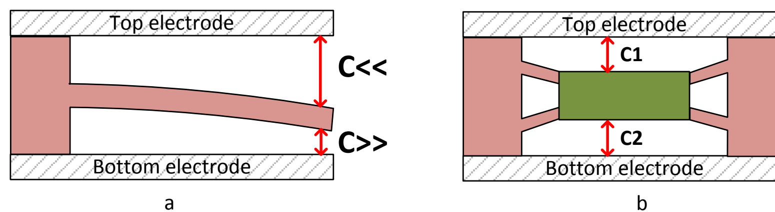

Figure 3.9: Capacitive sensing

In contrary to the piezoresistive sensing which performs an in-situ measurement on the deforming beam itself, capacitive sensing requires two electrodes. One above the beam and one below as shown in figure 3.9a.

On a first micromachined capacitive accelerometer described by [Bee04, p. 182] these electrodes were made up of two wafers with a thin aluminum film on each of them. Those wafers were then bonded on each side of the wafer containing the seismic mass.

This sensing principle has some big advantages compared to the piezoresistivity. First of all it is very insensitive to temperature changes [Gad05, p. 2.12]. Additionally it provides a larger output signal for the same deflection and also better noise-performance [Bee04, p. 182]. This results in capacitive sensing being used for high performance sensors.

Drawbacks on this type of sensing is the sensitivity for electromagnetic fields and the parasitic capacitive components in the circuit around the electrodes. Therefore in most cases only the capacitive change is measured.

An additional problem is that cantilever beams are only partially suitable for capacitive measurement. To achieve a linear change in capacity the seismic mass should move in parallel to the electrodes. This can be achieved by holding a mass in place with micromachined suspension as depicted in figure 3.9b [YN00]. Nevertheless this also requires high precision on the fabrication process to avoid any cross axis sensitivity [Bee04, p. 184].

3.4 Test & calibration

Considering process challenges from section 3.2.2 there is an obvious need for calibrating the micromachined sensor. From test side of view accelerometers can be categorized into two main categories: low-g for consumer and high-g for automotive applications [Sol+11]. Since the test system developed during this thesis is used to test an automotive grade TPMS device focus will be on the latter category.

Having a look on the evolution over the last two decades it soon becomes clear that test measures from the earlier days are not able to deal with today's products [OTC08]. Especially the rapid development of MEMS has brought up many new challenges including physical stressing.

3.4.1 Accelerometer test challenges

Examining the main tasks for testing accelerometers for the automotive area one may come up with the following as stated by [Sol+11]:

1. Sensor level check
2. Noise source isolation and elimination
3. Temperature conditioning
4. Mechanical stimulus
5. Outlier screening

As there is no harsh environment expected for consumer products items 3 to 5 are not applicable for such devices. Automotive standards do require more in-detail testing as semiconductor devices are mostly deployed in safety critical areas.

The first item is probably the most crucial as it has to be ensured that the fabricated device is perfectly leveled on the test system. This means that every device must be setup in a reproducible position. Any deviations could result in an offset error that would lead to systematic errors in the later test insertions.

Noise always was and probably forever will be an issue when it comes to highly accurate measurements. Since an ATE comprises of a large variety of very sensitive measurement instruments special care has to be taken when designing the loadboard for a tester. One should adhere to standard Printed Circuit Board (PCB) routing guidelines in order to avoid unnecessary susceptibility for noise even if a semiconductor test floor can be considered to be a low noise environment.

Physical stressing of the device is probably the highest demanding in terms of cost and development. For the targeted product there are three environmental conditions that have to be simulated: pressure, temperature and acceleration. At least for the latter there is a standard available [09] describing setup and requirements on centrifugal testing.

The last item on the list, also known as Part Average Testing (PAT) has its roots in the 1990s. Test limits are usually very wide while the actual results of a lot will aggregate in a small part of those limits. Using statistics it is presumed that devices within the same lot or wafer are showing the same characteristics. Due to that, new limits are calculated which are set tightly around those aggregated results. Any devices of one lot or wafer being outside those new limits are supposedly predamaged or are more likely to produce premature fails in the field [03].

3.4.2 Calibration

The necessity of calibration is basically given by the fact that even small process deviations are leading to a relatively large uncertainty (see section 3.2.2) on the actual output value. Accurate calibration requires an absolute reference of known values and would result in factors correcting the sensor's raw value to the referenced value [Cig+10].

Considering a single-axis accelerometer a simple calibrated centrifuge is sufficient to calibrate the DUTs. When it comes to 2-axis or 3-axis accelerometers calibration gets more complicated as the devices need to be accelerated in all directions. Special test systems are developed to cope with such multi-axis sensors including usage of machines that are moving on Lissajous traces [GBF11].

The system presented in the following chapters allows for a single-axis acceleration of up to 100g with simultaneous testing and calibration.

4 System design concept

When designing a complete test hardware solution from scratch many things have to be considered, that one would normally not care about if only a new loadboard for an existing ATE has to be developed. Amongst others this includes measurement circuity, software framework, mechanical robustness or simply the power supply concept. For the time being no generic off-the-shelf solution for testing of intelligent MEMS is available. The available microsystems are too different and complex to have one tester that would fit all.

In the following sections those main considerations and concepts are explained. First the **overall system** design is outlined describing the coarse features and components. This also includes components outside of this thesis' boundaries that are necessary to understand the feature set of this test system.

From this overview the most critical **requirements and limitations** are derived. Also their impact on the development and design is briefly discussed.

In the next section the main **system concepts** are explained in detail. Amongst others these are: *Device communication*, *analog measurement circuitry* and *power supply*.

The actual **test system components** are described in the last section. Some concepts outlined before are brought to life and transferred into a nearly final idea of a board.

Bringing together all main concepts inevitably wraps up a lot of questions. Many decisions during the concept phase were made on an iterative basis. This means that not all parts have been defined at once. First they have been outlined weakly and refined once another detail, that has an impact on the former, is specified.

4.1 System overview

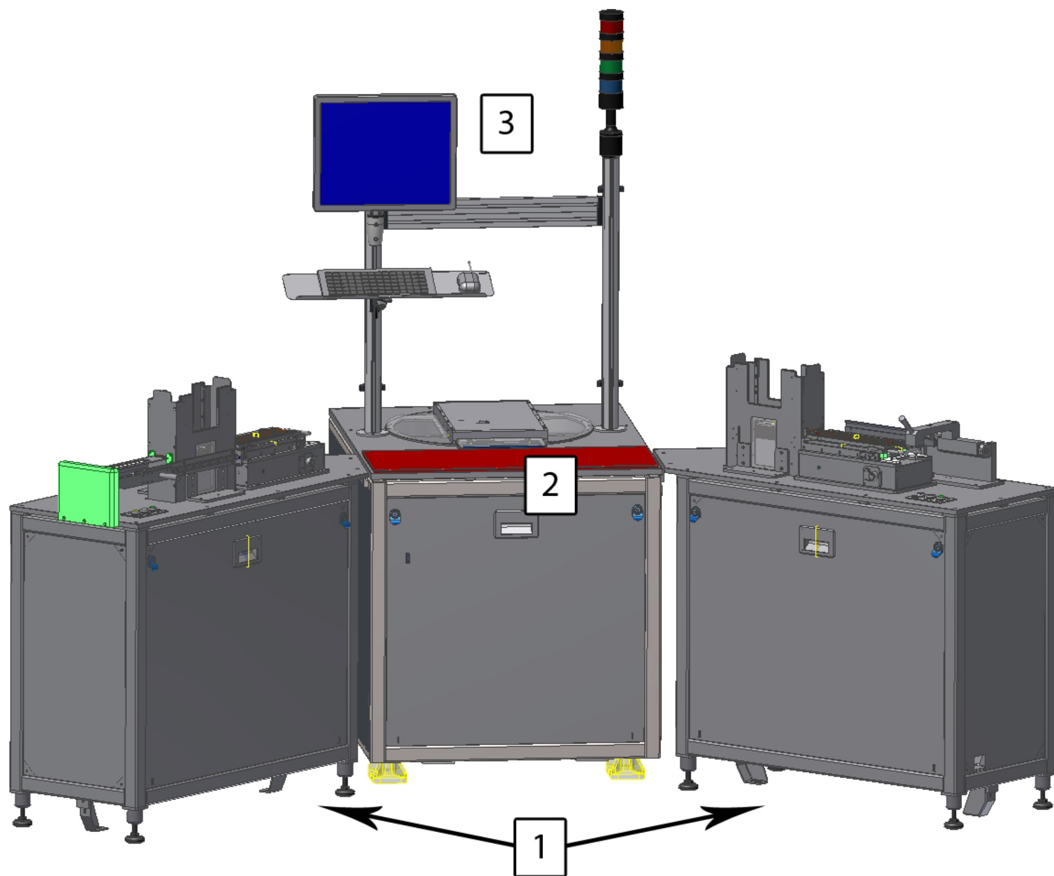

Figure 4.1: Tester and device handler overview

The whole system (as it can be seen in figure 4.1) consists of the following parts:

1. Strip loading/unloading station
2. Centrifuge with test system mounted
3. Operator interface

During this thesis only the actual test system is planned, verified and installed. The mechanical components like the centrifuge are built by a different company internal team. Nevertheless it is necessary to shortly introduce the mechanical parts and the device handler in order to understand the limiting factors for the test system development.

4.1.1 Device strips

The system is used on the Backend (BE) test floor of a semiconductor production fab. In this area the devices are already molded into their final package. However the DUTs are still kept together on so called *strips* which is a special type of leadframe that is optimized for automatic handling. This way multiple devices must be brought to a test system at once similar to a wafer that could contain more than thousand devices. Each strip contains 160 devices which are organized in five rows and 32 columns.

One option would be to use an existing ATE and only test the number of devices supported in parallel. This parallelism is limited by the amount of available measurement cards and channels in the tester. It usually varies between 4- to 10-fold parallelism in a configuration that can test TPMS devices. This makes sense where high quality analog and high speed digital measurements need to be done.

For the acceleration test and calibration there is no need to execute these kinds of measurements. All significant results have already been gathered in previous insertions. Thus it is possible to fully exploit the high parallel testing concept and develop a functional test system around these strips. The next step after acceleration testing is the final taping process which then also separates the devices from the strip.

4.1.2 Acceleration platform

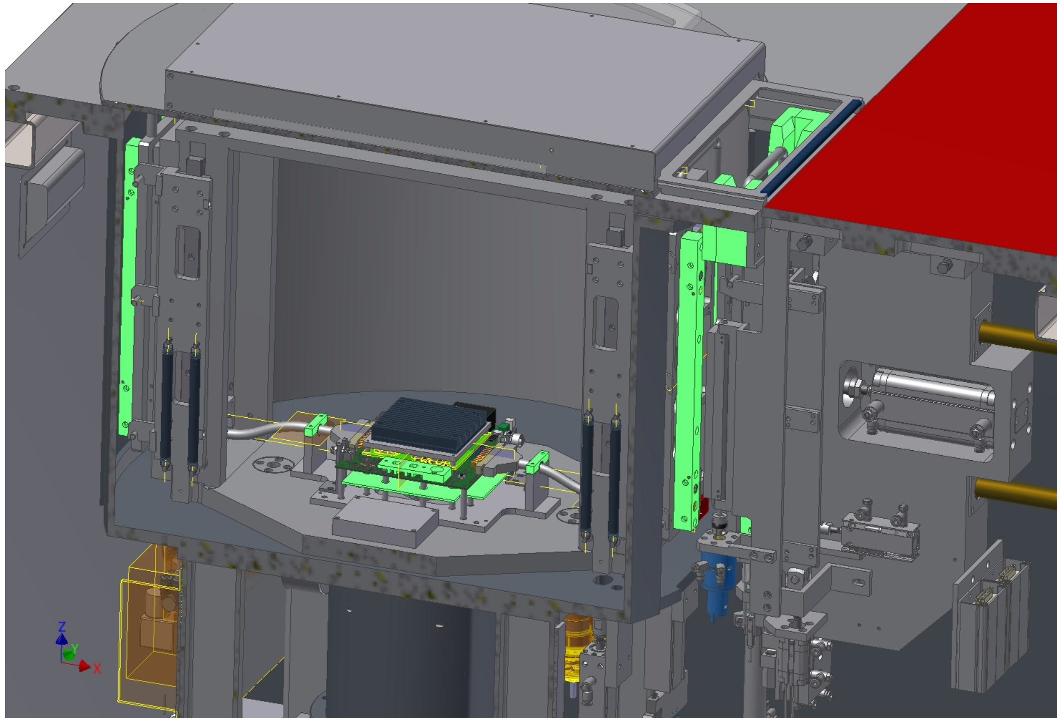

Figure 4.2: Cut-away view of the centrifuge with the contained boards

The platform for acceleration is the rotating part of the centrifuge. It consists of the table where the main PCB is mounted on the rotational axis as well as the contacting units on each side.

In case of the developed system it is necessary to keep the turntable, as it is depicted in figure 4.2, balanced. Thus it takes two opposing strips at once resulting in an overall capacity of 320 devices. The strips are mounted onto a special carrier at the loading station which can be seen in figure 4.1. Those carriers are then loaded into the centrifuge where they are locked and pressed against the socketboards.

In order to cope with the high-parallel testing and device communication a mainboard as it can be seen in the center of the turntable in figure 4.2 is needed. Connection between this board and the two opposing socketboards will be made through cable connectors on each side of the mainboard. A more detailed look on the subparts of this board is given in the next section 4.2.

4.1.3 Systematic error

To have all DUTs experience the exact same acceleration on all axes the strip would have to be bended. While it would probably be possible to have a curved strip carrier the mechanical stress for the strip would be too high.

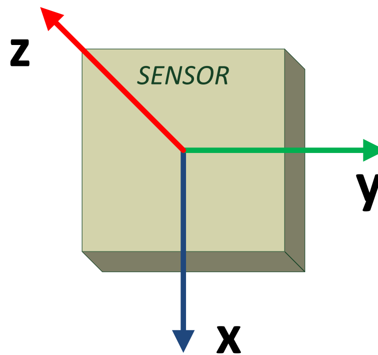

Figure 4.3: Simplified three-dimensional view on the sensor die

The sensor itself is supposed to be only sensitive on the main axis (z-axis) as it can be seen in figure 4.3. However a small cross-sensitivity exists on the other two axes which is difficult to model. As mentioned in chapter 3 the sensor underlies some process variations which make a precise statement on cross-sensitivity nearly impossible and not calculable.

Nevertheless in the following steps at least the relative amount of acceleration on the x and y axis will be calculated. Considering that after a certain amount of produced devices empirical values will be available on the cross-sensitivity these calculations can then be taken into account.

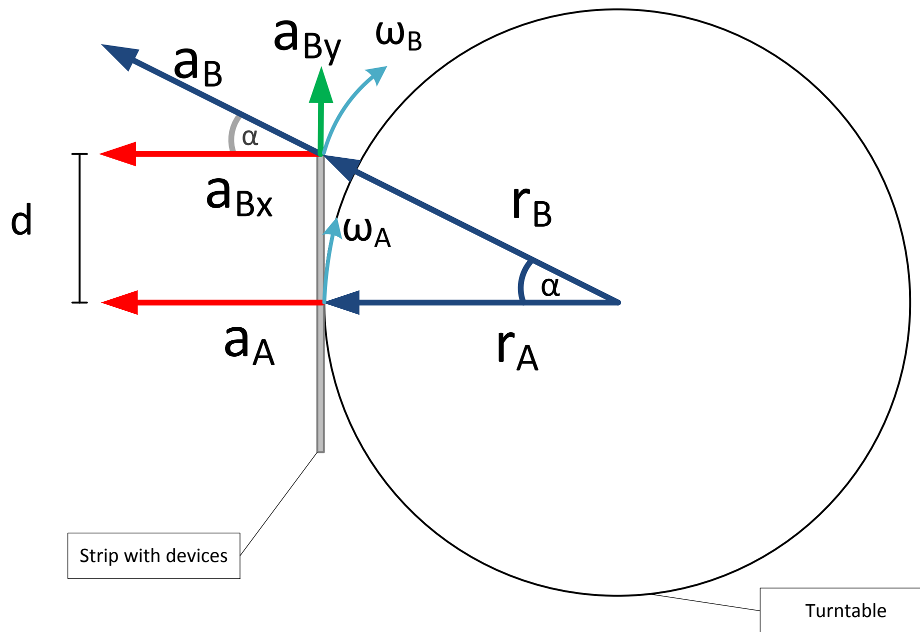

Figure 4.4: Top-view on rotating strip with acceleration vectors - Not to scale

Drawing 4.4 shows the simplified top-view of the turntable with one mounted strip. First it is demonstrated that the acceleration on the sensor's x-axis is always the same - independent of their position on the strip. For the sake of convenience only the central (vector index A) and the outermost device (vector index B) are considered.

It is known that the centrifugal acceleration is given as

$$a = r \cdot \omega^2 \tag{4.1}$$

which results in

$$\begin{aligned} a_A &= r_A \cdot \omega^2 \\ a_B &= r_B \cdot \omega^2 \end{aligned}$$

for both devices. The angular frequency is well known to be $\omega = \frac{2\pi}{T}$. Since it takes the same time for both devices to travel by 360° their values for ω are the same. Therefore this ends up in

$$\frac{a_B}{a_A} = \frac{r_B \cdot \omega^2}{r_A \cdot \omega^2} = \frac{r_B}{r_A}$$

Taking this into account it can be resolved for the value of a_{Bx} using the *cos*:

$$\begin{aligned} \cos\alpha &= \frac{a_{Bx}}{a_B} \\ &= \frac{r_A}{r_B} \\ a_{Bx} &= \frac{r_B}{r_A} \cdot a_A \cdot \cos\alpha \\ &= \frac{r_B}{r_A} \cdot a_A \cdot \frac{r_A}{r_B} \\ a_{Bx} &= a_A \end{aligned}$$

This proves that for the x-axis the sensor will always return the same result - independent of the position on the strip. Nevertheless figure 4.4 already shows that there is another acceleration vector in y direction.

The magnitude of this lateral component can be calculated as follows using the tan:

$$\begin{aligned}
\tan\alpha &= \frac{a_{By}}{a_{Bx}} \\
&= \frac{d}{r_A} \\
\frac{a_{By}}{a_{Bx}} &= \frac{d}{r_A} \\
a_{By} &= \frac{d}{r_A} \cdot a_{Bx} \\
&= \frac{d}{r_A} \cdot a_A
\end{aligned}$$

It is now obvious that the unwanted cross acceleration is dependent on the ratio between d (distance between the central and outermost device) and the radius r_A. Considering real values for the formula given above

$$\begin{aligned}
d &\ldots\ 24\,\text{mm} \\
r_A &\ldots\ 250\,\text{mm}
\end{aligned}$$

$$a_{By} = 0.096 \cdot a_{Bx}$$

the y-axis sees around 10% of the main acceleration. Even if there are no results on the sensor's cross-sensitivity available it is very likely that it is going to be below 10%. This then leads to a sensed cross-acceleration of below 1% in the worst case.

Additionally the equipment will be characterized against a reference centrifuge. Correlated results will then give correction factors for each row on the strip. These values can then be considered when calculating calibration factors for each device.

4.2 Requirements and limitations

Because of the system's nature a lot of mechanical and physical constraints limit the component selection. Also requirements have been derived from what is needed, physically possible and economically feasible.

The mechanical assembly serving as the mounting platform for the boards also inherently limits the board design:

- Turntable diameter (50 cm)
- Main power supply (12 V, max. 4 A)
- Loading unit applies high force (approx. 10 kg) on socketboard in order to fix strip carrier
- Size of the device strip
- Handler-Tester signal transmission via slip-ring only

From those given points the development restrictions for the mainboard and the socketboards can be deduced:

- Socketboards need additional strengthening to bear the high contact pressure
- Socketboards should not be much bigger than device strips
- Maximum available size for each DUT circuit (1.05 cm^2)
- Keep size of mainboard as small as possible to reduce centrifugal force at outermost components
- Avoid moving parts
- Distance of 15 cm between mainboard and socketboards

One major aspect is to avoid any moving parts on the boards themselves. This includes fans and electro-mechanical devices. Those devices are more likely to fail if they encounter high acceleration (up to 100g) as their solid-state counterpart would.

Another critical requirement is to have an exclusively passive cooled system. As mentioned above fans are not an option for cooling the system. Hence the amount of heat to be dissipated should be as low as possible in order to be able to use simple heat sinks.

Dissipated heat directly correlates with the amount of power that is needed to operate a certain device. The main power supply being available on the turntable is rated at 12 V and a maximum current of 4 A. Doing early power estimations during the design process is crucial to avoid any late surprises that would result in costly redesigns.

The distance between the mainboard and the two socketboards will have to be overcome with a multiwire cable. Special connectors are needed in order to ensure that the acceleration and vibration does not negatively affect the connection quality. Those wires will also carry noise-sensitive signals thus special measures are taken in order to avoid cross talk or glitches.

4.3 System concepts

4.3.1 Test system - Handler connection

A very sophisticated component of the assembled centrifuge is the slipring. It is providing the electrical interface between the centrifuge and the handler. All signals and the power supply will be brought into the drum solely via inductive and capacitve coupling. This makes it possible to also transmit high-frequency signals like Ethernet. Inductive coupling is used for static signals like the power supply while capacitive coupling is used for dynamic ones. Compared to traditional slip rings that use brushes the advantages are obvious. There is no abrasion and also no interference induced on the signal as it is caused by metal rubbing at high speeds.

4.3.2 Matrix structure

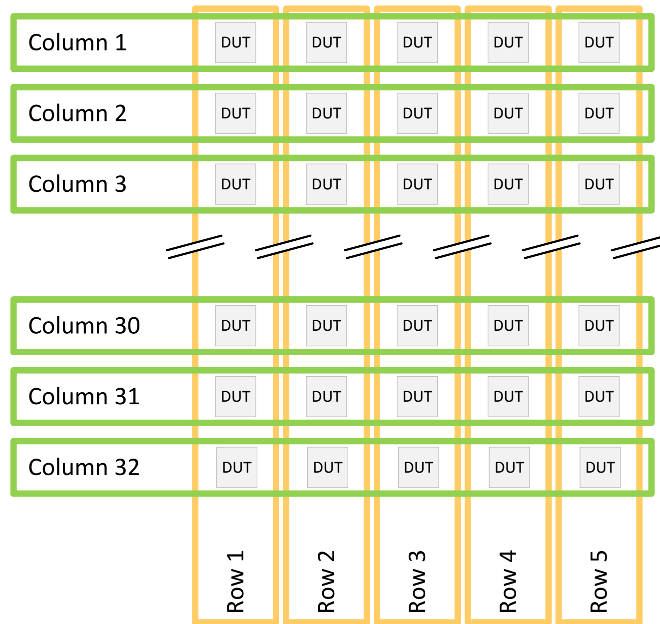

Figure 4.5: Matrix structure used

As depicted in figure 4.5 one can interpret the row and column layout of the device strips in a hierarchical manner: Each DUT is one row object out of five in one column. This column object is one out of a total of 32. When using modern Electronic Design Automation (EDA) tools such types of hierarchical designs are actively supported.

In terms of the test systems this means that many monitoring and controlling circuits are for example only available once per column. This largely reduces the space needed per device and also simplifies the PCB layout process since similar circuits can be reused multiple times.

4.3.3 Parallelism types

In terms of the developed test system two types of parallelism need to be defined. They will be referred to in the context of device count tested in parallel.

The first is the so called **hard parallelism** which in fact reflects the standard definition of things happening at the exact same time.

The second type is called **soft parallelism** and describes that many small parallel tasks are happening sequentially very fast. This is especially necessary because coping with 320-times parallelism with the given restrictions needs some type of multiplexing.

4.3.4 Device communication

Besides the fact that the DUTs incorporate an Inter-Integrated Circuit (I2C) interface some other options are possible in order to build the system monitoring and power management bus. This includes but is not limited to Serial Peripheral Interface (SPI) or System Monitoring Bus (SMBus).

These busses consist of devices monitoring board health, for example temperature and acceleration sensors, power monitors and Analog-to-Digital-Converters (ADCs) that measure the current on a certain power domain.

The decision to use I2C was made after the selection of the embedded system. The system already has an I2C interface included and a software Application Programming Interface (API) to access the bus. Also the fact that thousands of different devices using this bus are available, made the decision obvious.

The communication busses were partitioned into the following parts:

- System bus
- Power management bus
- ADC bus
- DUT busses

The **system bus** contains all devices that monitor the system's state. Their values are not mandatory for the test execution but for determining that the system is fully functional. This includes temperature sensors, power monitors and trimming resistors.

Controlling of the power supply for each DUT will be done by a device that is using an explicit **power management** bus. Separation is mainly done to keep device response time low.

The ADC bus is a separate I2C channel for all converters supporting the high speed mode. This enables data rates up to 3.4 MBit/s. It will solely be used by the reference acceleration sensors and the DUTs current measurement sensors. Having low speed devices on the same channel would be possible but they cannot be accessed while the high speed mode is enabled.

Finally the bus that is experiencing the highest load during measurement runs is the DUT bus. It will use some sort of soft parallelism because a total of 320 separate I2C channels would be not affordable in terms of control, connector size as well as PCB area.

For the implementation of such a highly parallel communication with the DUTs a Field Programmable Gate Array (FPGA) is used. It acts as an I2C master for five devices in parallel per site. This results in a hard parallelism of ten devices.

Using an FPGA makes the design very scalable and extensible. Especially when it comes to a pure digital subsystem like this parallel I2C master the abilities of reconfigurable devices clearly stick out. Later changes in the digital logic can be easily programmed to the device without having to do a board redesign.

4.3.5 Analog measurement circuitry

Acceleration testing and calibration is the last test insertion thus there's no need to do in-depth testing of the devices. Those mixed signal measurements are done in earlier steps. Executing those tests again in the acceleration insertions would only drive up costs and test time.

Therefore the new test system will only have two basic analog measurement circuitries:

- DUT current (accuracy around 100 µA)
- Contact resistance (accurate down to 0.1 Ω range)

Because of the limitation on board size it is in no way feasible to have two explicit ADCs (one for contact resistance and one for current measurement) for each DUT. Within this limited area per device (around 1 cm^2) it is more important to ensure a correct device circuit (e.g. decoupling caps, precise supply voltage). Taking advantage of a hierarchical design as outlined in section 4.3.2 can significantly reduce costs and redundancy.

Contact resistance

Contact resistance measurements are normally executed at the very beginning of each test insertion. Such measurements can either be performed to measure contact quality between measurement board and device pin or between the pin and the actual silicon pad. Such tests are crucial for pins delivering high-power signals. Additionally the measurement of the contact resistance between the board and the pin (in the form of pogo pins or needle cards) is used to determine if the board may negatively influence the measurements.

Apart from that, contact resistance measurements are mainly necessary here because no such system was built before. Consequently there is no experience on how much the boards would deform and influence pin contact during acceleration. Even slight deformations could result in a bad device contact which further leads to irreproducible yield loss.

In case of the developed system a combined method is used that measures resistance via the two ground pins of the device. Into one of those pins a very small specified current will be forced while the other one will be connected to the "real" ground. By measuring the voltage drop across this circuit one may easily calculate the resulting contact resistance.

DUT current measurement

Measuring the device's current consumption is used to detect faulty DUTs. While a too high value means that the device is shorting the supply, a too small current indicates that the device did not power up properly.

Since the DUT's run current is below 1 mA exact measurements are not an easy thing to do. ADCs being precise enough in this measurement range are soon getting very expensive while the overall additional benefit for the test system more or less stays the same.

For the acceleration test system it is absolutely sufficient to be able to approximate the current and make a simple "working" or "not working" statement. Nevertheless it is still necessary to have switchable current limiters for each DUT available. Being completely pessimistic and saying that all of the 160 devices could fail at the same time a board with no current limiting regulator would soon get overheated.

4.3.6 Power supply

There is one main supply coming from the slip ring and providing 12 V with a maximum rated current of 4 A. Especially the mainboard needs many different voltages to deliver power to all of the used ICs.

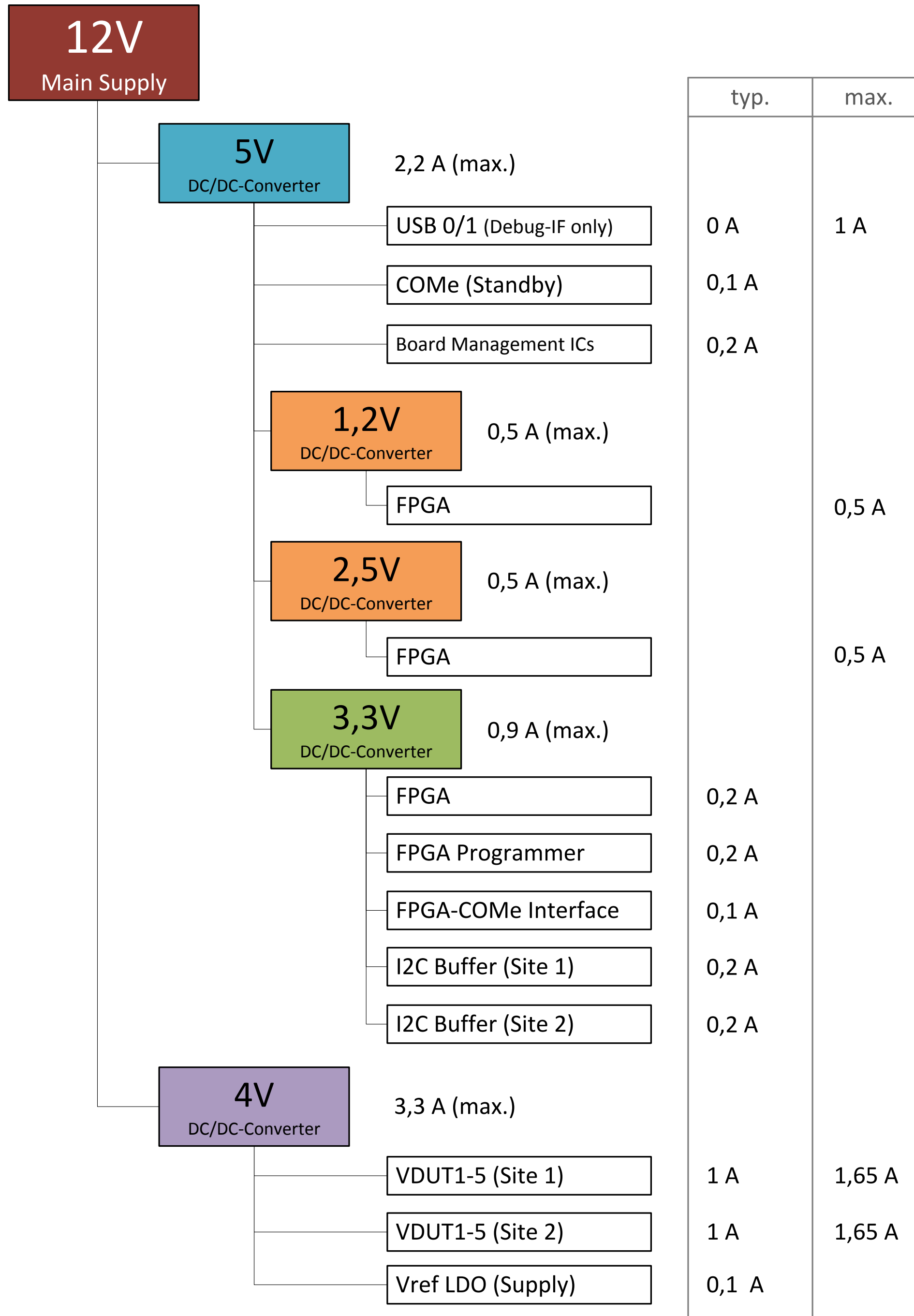

Figure 4.6: Supply planning and power estimation

Basic concept

In figure 4.6 the five different voltages that need to be generated can be seen. 3.3 V and 5 V are de facto standard voltages used by many ICs. Additionally it is also necessary to provide 1.2 V and 2.5 V as core voltages for the FPGA.

Since the main supply is rated at a maximum of 4 A it is necessary to implement highly efficient voltage translators. Conversion losses and dissipated heat are the main selection criteria in this case. Additionally the converter size needs to be as small as possible to easily fit onto the mainboard.

Switched-mode conversion therefore seems to be the best option especially in regard of availability. Nowadays such converters are already available in tightly integrated packages while achieving high output power ratings. At the moment converters with an overall efficiency of more than 90% and a package size of around 3 mm x 3 mm are available. Nevertheless they are still able to deliver a maximum of 1 A at voltages from 1.0 V to 3.3 V.

DUTs

Voltage generation for the DUTs will be done by a separate 4 V converter. This voltage is then distributed to each DUT circuit where a regulator stabilizes it to the applicable test voltage by its adjust pin. The actual value of this adjust voltage is set by the reference Low-Dropout (LDO) regulator.

While it would also be possible to use the 5 V converter for the DUTs there are some risky disadvantages of this solution. Considering a faulty behavior in the adjust voltage circuitry it is very likely that the DUT could get supplied with 5 V which is way out of the specified range. Whereas 4 V is marginally within the specification it would surely not have a lasting effect on the device. Also having a completely separated supply exclusively for the DUTs reduces negative effects of ICs that show a dynamic current consumption profile like FPGAs or ADCs.

Power estimation

As mentioned beforehand power estimation is definitely necessary. In figure 4.6 the approximate power consumption per block can be seen. Since power estimation is done in a very late concept phase there are already some approximate values available. The ratings for the single blocks are consciously overrated in order to avoid the converters operating at their absolute electrical limits later on.

4.4 Test system components

This section covers the system's logical parts, their design and function within the test system. First a general discussion is made on the possible embedded system types in respect to the previously assessed requirements. Subsequently the mainboard and the socketboard are outlined and an estimation on their functional blocks is made.

4.4.1 Embedded system - *Computer-on-module*

One major decision within the project was to go for a separate PC-like system that would run the actual test program and represent the core unit of the system. Selection was mainly driven by the requirement of a small form factor, low power consumption and the ability to run a full-grown operating system like Windows or Unix/Linux. Additionally it should rather have a few large connectors carrying all signals instead of many explicit media connectors, like VGA or USB. While this enables full freedom on board and application development it most likely requires a complete carrier board to be built around this system.

This system will be an industry grade application and needs to be tailored towards the specific needs of a test system. This inherently requires some type of embedded systems. Such computers are categorized into multiple different sub classes. For our specific needs the so called Computer-On-Modules (COMs) are fulfilling most of the requirements. The term of COM

itself is not standardized but many standards evolved out of it. All of them usually describe a single circuit board including a Central Processing Unit (CPU), Random Access Memory (RAM) and controllers resulting in a full-fledged computer. Additionally all IO signals are brought to at least one board-to-board connector. This is the interface to the base board that is required to run the system.

Researches on available COM systems soon brought up three industry standards that would fulfill the requirements:

- Embedded Technology eXtended (ETX)
- COM Express
- Qseven

While *ETX* exists as a long-term supported sophisticated embedded solution it's roots can clearly be seen in the earlier days of computing. For example it includes Industry Standard Architecture (ISA) bus but no Peripheral Component Interconnect Express (PCIe) interfaces. Nevertheless the *ETX* standard is still actively driven by the Embedded Technology eXtended Industrial Group (ETX-IG) and boards are still being developed using latest technologies. [cf. Gro07]

COM Express is a very new system type being standardized by the PCI Industrial Computer Manufacturers Group (PICMG). Its first specification was released in 2005 and was continuously improved since then. The standard defines four different form factors ranging from around 11 cm x 15 cm down to the size of a credit card. All signals are brought to one or two (depending on the pin out type) 220 pin connectors. [cf. Gro12]

The *Qseven* standard is following a similar direction as *COM Express* but with the difference that there is no support of legacy interfaces (e.g. VGA). Its specification was initially released in 2008. There are two different form factors available sharing one common pin out. The standard is actively driven by the Standardization Group for Embedded Technologies (SGET). [cf. Sta12]

Out of the standards listed above *COM Express* was selected as to be the most suitable. Compared to *ETX* it was more future-oriented. Especially the availability of a 95 mm x 95 mm form factor did fit better into the overall design concept. On the other hand *Qseven* also is a modern standard but

availability of boards is limited at the time of research. Considering modularity and the option to choose from a wide range of suppliers influenced the decision towards the *COM Express* standard.

4.4.2 Mainboard

The mainboard serves two purposes. On the one hand it is the carrier board for the COM and on the other hand it contains the core logic for controlling the device communication and measurement runs.

In figure 4.7 a general overview of the mainboard components can be seen. Below a list of the most important blocks with a short description:

In the **power input stage** the 12 V main supply is prepared to be distributed over the board. Furthermore a power monitor is measuring voltage and current. In addition a reverse polarity protection and decoupling capacitors are included.

The block of **power converters** contains all power regulators and DC/DC converters used to generate the voltages for the ICs.

I/O Buffers and connectors concentrate all power supplies and communication signals (I2C channels) for transmission to the socketboard. Additional measures against noise will be taken in the I/O buffers stage including Electrostatic Discharge (ESD) protection.

The **FPGA** will contain multiple I2C masters that are managing communication to and from the DUTs on the socketboard.

Board utilities are all other system monitoring devices like temperature sensors or power monitors.

COM & mSATA are the embedded system being used to run the test environment software.

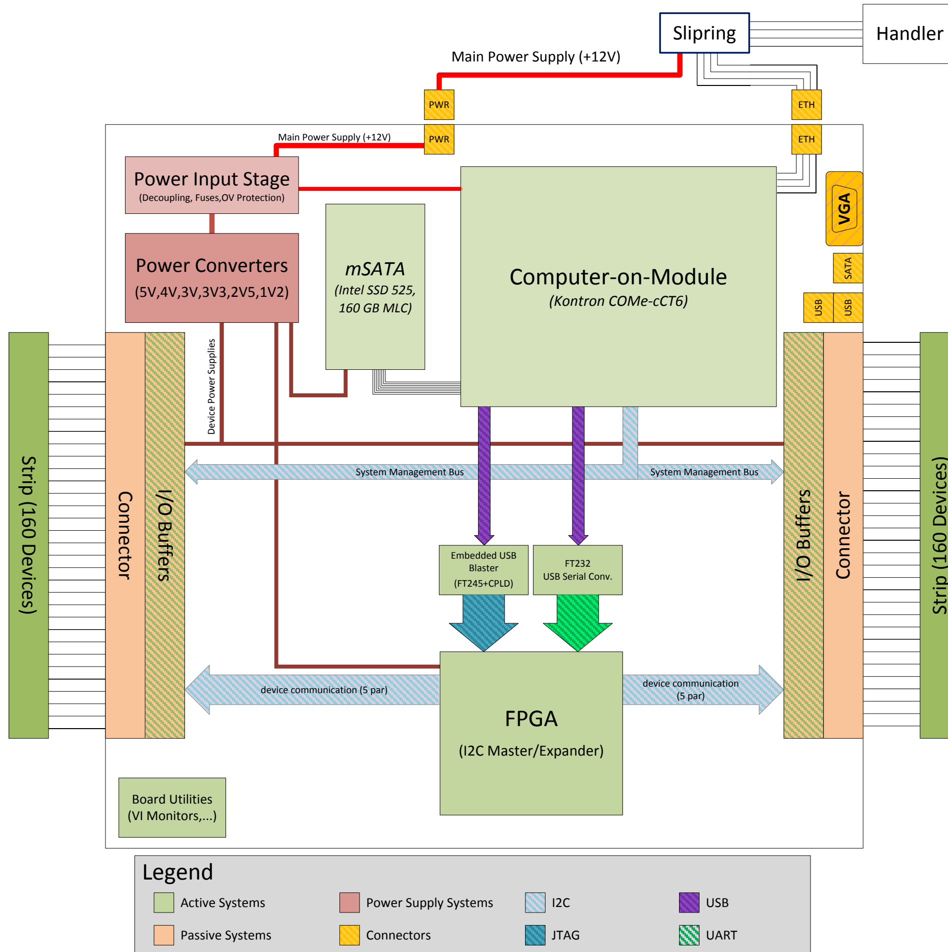

Figure 4.7: Conceptual view of the test system's mainboard

4.4.3 Socketboard

The socketboard is mounted on a special stiffener to provide mechanical stability and its front side is facing to the outside of the centrifuge. Pogo pins will be the connecting element between each pad of a DUT circuit and

the device mounted on the strip carrier. These carriers will be mechanically locked to the board with a force of around 10 kg.

DUT circuit

As already mentioned in previous sections the space for each DUT circuit is very limited. The available area for each device is limited to a maximum of 1.05 cm^2. Because of the stiffener there will also be some extra mounting holes that are obstructing this area in some cases.

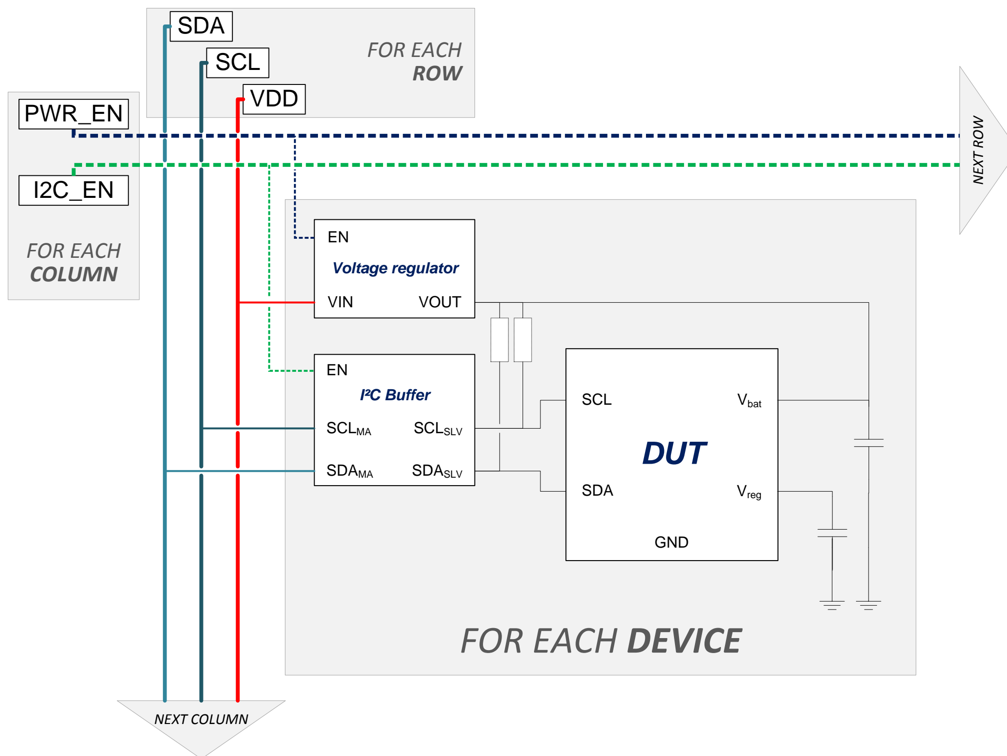

Figure 4.8: General idea of DUT circuit implementing matrix structure

In figure 4.8 a basic device circuit is shown that is using the matrix concept described in 4.3.2. It is planned to have one I2C channel and a common power supply per row. There should be a controlling device for each column that can switch the two enable signals.

Each DUT does at least require a separate voltage regulator and an I2C buffer. Additionally some place will be needed for decoupling capacitors and pull-up resistors for the I2C lines.

The voltage regulator needs to be inherently able to limit the current on the output and have an *enable* input. In case of a faulty device it must be possible to explicitly switch off supply for it.

Device communication is decoupled using a dedicated buffer for the I2C channel. It will serve two purposes: switching the common clock and data lines to a device and also limit the capacitive load on the main bus.

Board stability

As mentioned previously a strip carrier will be pressed on the front side socket board. Together with the stiffener being mounted on the backside the board could easily deform. To avoid any late surprise the board will receive a special coating similar to Kevlar on its front side.

Considering that there are also ICs mounted on the backside with a rather large package, deformation could also stress their soldering joints. This type of wear out is even worse since finding such errors on productive boards easily takes multiple hours. In this case equipment downtime is inevitable and will largely affect production capacity.

5 Implementation

In this chapter some of the concepts described in the previous chapter 4 are picked up and a detailed look will be made on their actual implementation. First and foremost those parts have been selected which show a more innovative character compared to the previously used techniques for testing of such TPMS accelerometers within the company.

5.1 Power supply

Power supply clearly is an essential part of every electronic system. Since the main supply of the test system in the centrifuge offers only a maximum of 4 A highly efficient converters need to be used. In the following section the power supply network and its special features are described.

5.1.1 Power distribution network

The actual implementation of the power supplies is very similar to the concept mentioned in section 4.3.6. Compared to the typical power estimation the actual current consumption is way below the target. Hence enough headroom is available.

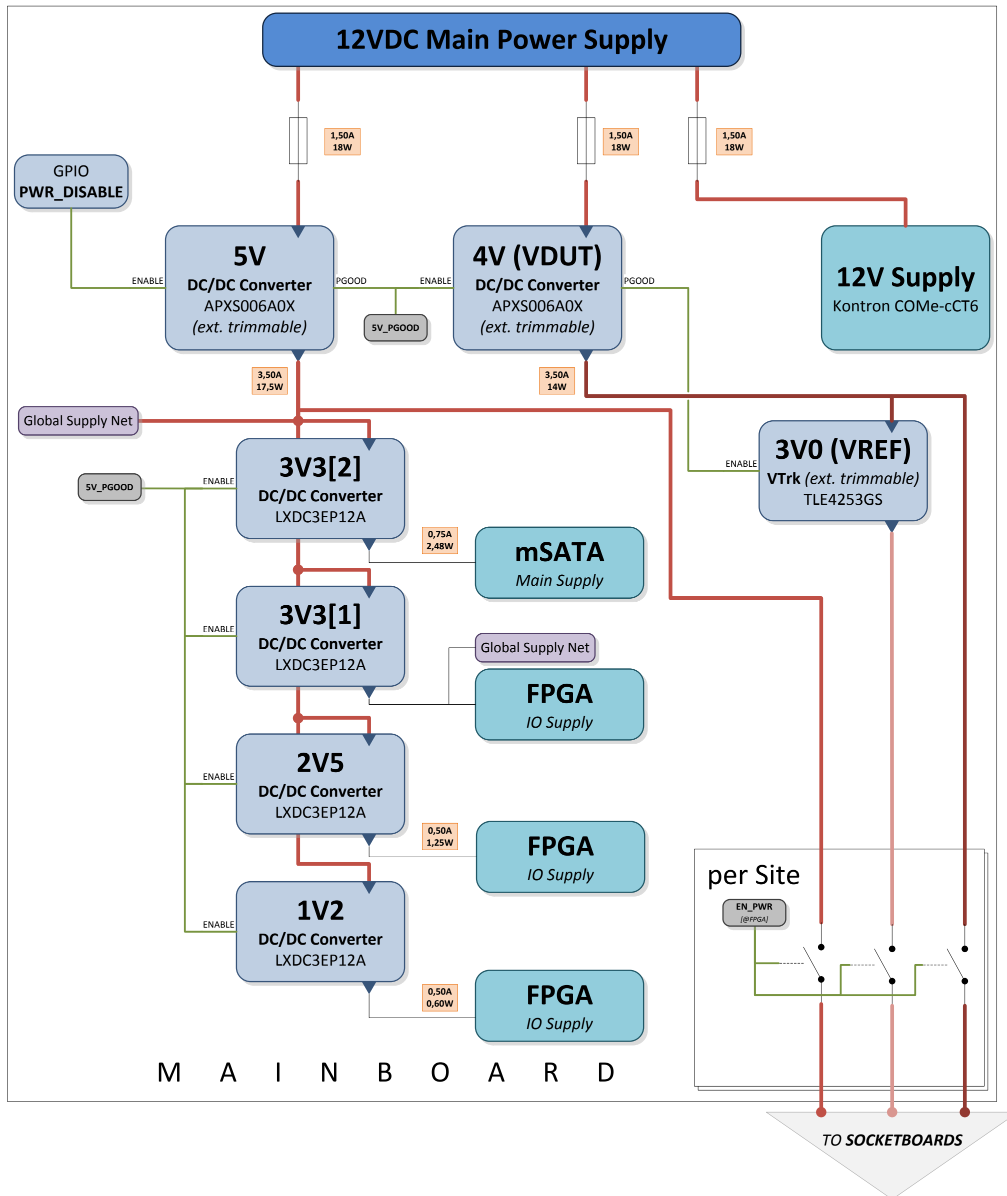

Figure 5.1: Power distribution network on the mainboard

In the block diagram in figure 5.1 all converters including their main consumers can be seen. Apart from the direct connection of the embedded system the network is divided into three main sections: **High power converters**, **low power converters** and **reference regulation**.

The **high power converters** are responsible for generating the 5V and the 4V domain respectively. While the former powers a global supply net and acts as source for the low power converters, the latter is the power source for each DUT. They can be trimmed externally with a digital potentiometer connected via I2C.

Both domains are using the *Pico TLynx* DC-DC modules manufactured by Lineage Power. These converters are surface mountable with a maximum rated output current of 6 A. Their overall efficiency lies around 90% resulting in nearly no dissipated heat.

Additionally they are providing a *power good* pin that outputs a high level after the module has successfully powered up and is delivering a stable output voltage. This signal is used to implement a cascaded power up in order to avoid any glitches that could make other converters unstable.

Hierarchically seen the **low power converters** are connected to the output of the 5V converter. They provide the additional standard voltages needed to operate certain ICs and the FPGA. There is an additional 3.3 V converter that is providing an isolated power domain for the hard disk of the embedded system. The converters used are from the *LXDC3EP* series produced by Murata also achieving an efficiency of around 90%.

The last section **reference regulation** is responsible for generating the voltage V_{ref}. This power domain solely provides a reference level that is tracked by each voltage tracker in a DUT circuit.

Only the 5V, 4V and V_{ref} domains are transmitted to the socketboards. They can be switched by the FPGA in order to avoid voltages being applied to an open connector.

5.1.2 Power monitoring

In order to easily monitor sanity of the power distribution network mentioned above the mainboard contains special monitoring ICs for each power domain. These are shortly described below and the additional power control features are outlined.

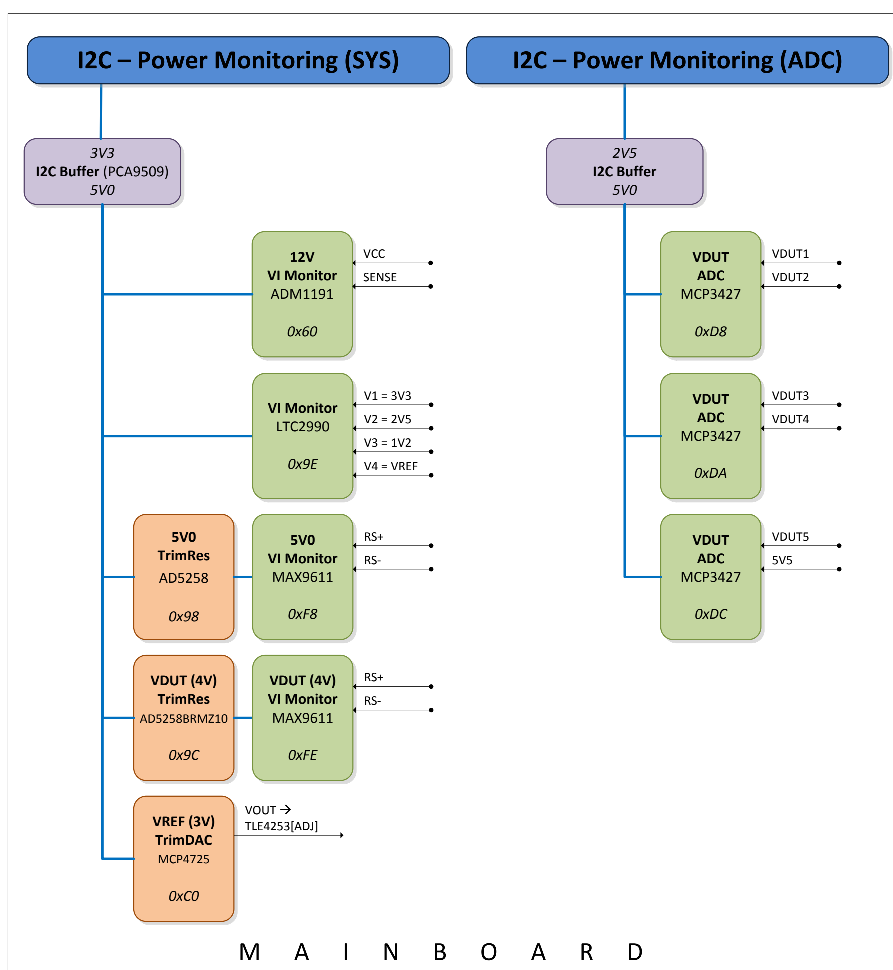

Figure 5.2: Block diagram of power monitoring ICs

Figure 5.2 shows the ICs available for measuring and influencing the power domains. They are divided into those monitored directly with the inbuilt I2C channel of the embedded system and those monitored by the FPGA via a dedicated ADC channel. Their function within the power distribution network is described below.

Main power monitoring

The main power domains are measured using different monitors. This variation is mainly caused by the fact that not for every power domain the same precision is needed. All devices used are connected to the system I2C bus which is controlled by the embedded system.

The main supply is monitored using the 12 Bit power monitor ADM1191 by Analog Devices in combination with a kelvin-contact current sense resistor. It is possible to either measure the single-ended voltage at the pin *VCC* or the voltage drop between *VCC* and *SENSE* input. Constantly monitoring these two values allows to react on overcurrent or overvoltage conditions that could permanently damage the boards.

All low power converters and the reference voltage are constantly monitored using a LTC2990 produced by Linear Technologies. This monitor allows different setups ranging from differential measurement to all single-ended. Additionally it can be setup to permanently perform measurements or only on demand. The measured voltages are constantly watched by the software on the embedded system and eventually triggers an alarm.

Finally the two high power domains are monitored using a MAX9611 by Microchip with a resolution of 12 bit each. The two measurement pins of the monitor are again connected to a kelvin-contact current sense resistor. Hence a voltage and a current measurement is possible.

VDUT current monitoring

The ICs responsible for measuring the DUT current are the 16 Bit ADCs MCP3427 manufactured by Microchip. They provide two channels that

can either be measured differentially or single ended against ground. This allows to measure either the absolute voltage or the drop across the current sense resistor. They are connected to an explicit ADC I2C channel that is controlled by the FPGA.

A total of three ADCs is used in order to measure all of the five rows. The remaining sixth channel is used to measure the current consumption on the 5V power domain of the socketboard.

Since all DUTs in one row are powered by the same VDUT rail, measurement is done on a differential basis between two consecutive measurements. Before the first device is powered up the idle current consumed by the voltage trackers is measured. Afterwards a whole column is powered up and a new measurement of the current is performed. The difference between the new measurement and the previously measured value is the consumed power of the DUTs in the first row. This step is repeated for each column until all devices are powered up.

This implementation however has some disadvantages. First and foremost it is not possible to measure the current of one device after all columns have been powered up. Secondary if measurement is done too fast it can happen that some dynamic power up current consumption is measured instead of the static run current. Nevertheless this implementation allows for roughly estimating if the DUT is working properly or not. In this case a trade-off between precision and available area was made that is sufficient for this test system.

Trimming

For the power domains where higher precision is necessary because of attached ADCs or DUTs a trimming function as depicted in figure 5.2 is implemented. In case of the high power domains a digital potentiometer is attached to the *TRIM* input of the DC-DC converters. In combination with constant monitoring of the voltage the supply can be setup very precisely.

For the reference voltage V_{ref} the 12 Bit Digital-to-Analog Converter (DAC) MCP4725 by Microchip is used instead. Its output is connected to the adjust

pin of the voltage tracker TLE4253 manufactured by Infineon. The output of this tracker is then distributed to each DUT circuit.

5.2 DUT circuit

5.2.1 Schematics

As discovered in section 4.4.3 a maximum area of 1.05 cm^2 is available for each device circuit. The DUT itself is contacted from the outside of the board and thus does not obstruct this space. Nevertheless the circuitry for each device must still be limited to the parts really necessary.

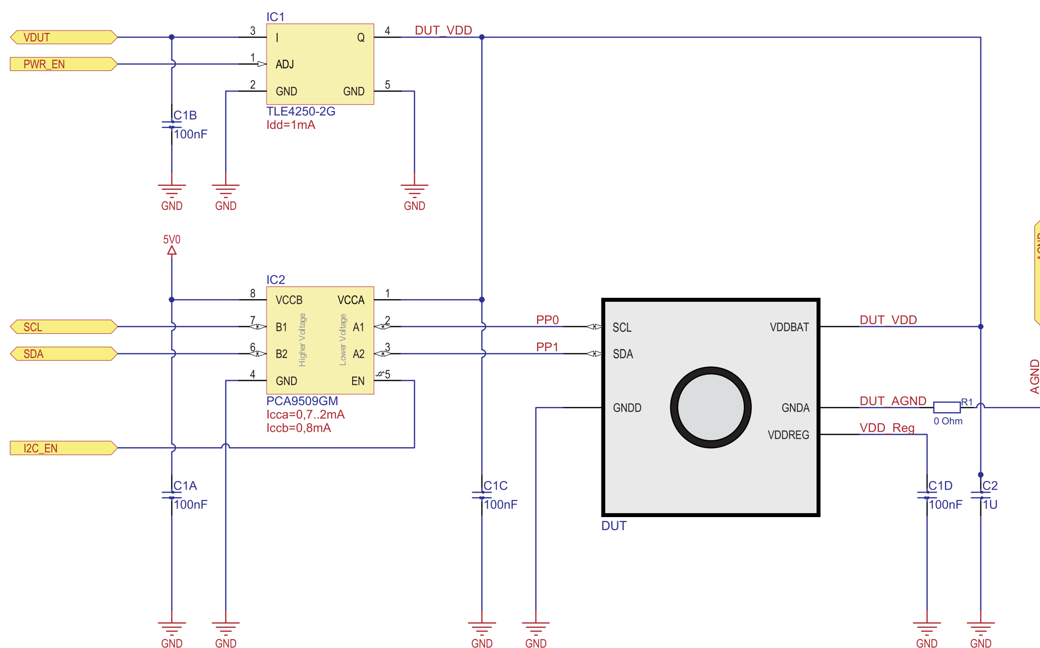

Figure 5.3: Schematics of the DUT circuit

As depicted in figure 5.3 each circuit will consist of the following parts:

Voltage tracker (Infineon TLE4250-2G)
: Provides a stable supply for each DUT. Can be switched on separately for each of the 160 device circuits.

I2C buffer (NXP PCA9509GM)
: Mainly used for controlling which column of the matrix structure is currently connected to the I2C bus.

Passive components
: Several decoupling capacitors in order to ensure stable device operation.

DUT
: Reduced circuit that only connects the minimum required pins. Its footprint provides the pads on the PCB where the pogo pins are mounted.

5.2.2 DUT power management

The voltage tracker TLE4250 manufactured by Infineon provides the basis for the power supply control of each DUT circuit. In comparison to a voltage regulator a tracker has no internal reference and simply tracks an external voltage. The *ADJ* pin is a combined adjust and enable input. If voltage drops below 1.2 V it switches the output *Q* off. If it is above this threshold it tracks the voltage level on the *ADJ* pin.

DUT current measurement and supply switching is implemented using the matrix structure described in section 4.3.2. For each column there is an IO expander available that is connected to the power management I2C bus. It has five power enable (*PWR_EN*) outputs that are switching the generated reference voltage V_{ref} to the respective adjust pin (*ADJ*) of each TLE4250 in the DUT circuits.

In addition to the delta current measurements described in 5.1.2 of the VDUT lines the TLE4250 also inherently limits output current to typically 85 mA. Since the columns are switched on sequentially this would lead to an additional current consumption of 425 mA in the worst case.

5.3 FPGA - DUT communication

The core element of DUT communication is built by an FPGA that serves as a multi I2C master. Implementing the matrix structure as outlined in section 4.3.2 it has a hard parallelism of ten devices and a soft parallelism of 320 devices.

Following the parts are outlined that are directly involved in transmitting data between the embedded system and the DUTs on the socketboards.

5.3.1 Embedded system interface

Initially a PCIe interface between the COM and the FPGA was planned. The idea behind was to have a high-speed serial interface available as the speed of this communication channel directly influences test time. After thorough investigation this unfortunately proved to be not adequate in terms of overall implementation effort. Apart from the very short initial start up time frames required by the PCIe specification the drivers on operating system side is fairly complex if being setup from scratch.

Therefore the communication between the embedded system and the FPGA is realised by using a FT232H USB-FIFO/Serial converter by FTDI. Main benefit of using this IC is the support for either parallel First In First Out (FIFO) or serial communication at very high data rates up to 40 MB/s. For the first implementation an asynchronous Universal Asynchronous Receiver Transmitter (UART) interface was selected running at a bitrate of 460 kbit/s. During board design it was already taken care of being able to switch from the serial to a parallel FIFO interface.

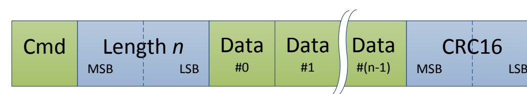

Figure 5.4: UART frame structure

On top of the UART interface a custom protocol is implemented in order to reduce the communication overhead and to be able to detect transmission fails. In fact it partially encapsulates I2C frames and functions. As depicted in figure 5.4 a frame consists of the following parts:

Command *(Length: 1 byte)*
: Microcode to indicate content of the following payload section (e.g. Result (from FPGA), Command (to FPGA), etc.)

Length *(Length: 2 bytes)*
: Number of bytes in the following data section.

Data *(Length $<$ (4096-5) byte)*
: Actual data consisting of microcodes to write to or read from the DUTs. Number of maximum bytes is limited by the 4 kByte UART buffer in the FPGA.

CRC16 *(Length: 2 bytes)*
: CRC of all previous bytes in order to detect errors during transmission. It is evaluated by the receiver and in case of a mismatch a retransmission is requested from the sender.

This encapsulation allows for easier handling and sanity checking of the transmitted data on software level. Without header data defined parsing of the byte stream in the application would be way more error-prone if not impossible at all.

5.3.2 In-system reconfiguration

FPGAs are usually configured using special programmer devices that are connected to the Joint Test Action Group (JTAG) chain of the FPGA. In many cases also a configuration device is used alongside the FPGA in order to permanently store this configuration.

As already outlined in chapter 4 the test system will be mounted in the centrifuge. Hence attaching auxiliary devices is normally not possible or at least not practical. Unfortunately there are also no ICs or integrated modules available for the programming task that could be designed onto the mainboard. Additionally such programmers are above all very expensive

and large compared to the mainboard. Therefore they are also not really suitable for directly mounting them on the mainboard.

After careful research a JTAG programmer was built using demo implementations and considering the FPGA manual. It uses an FT245 by FTDI to connect the circuit to the embedded system. Additionally a Complex Programmable Logic Device (CPLD) is necessary to transform the byte-based protocol, used by the programming software, to the JTAG protocol. This way it is possible to use the default programming software of the manufacturer to reconfigure the FPGA.

5.3.3 Site fanout

The hard parallelism of ten devices also requires ten independent I2C masters to be implemented in the FPGA which are split up into five per socketboard. Each of them is fed with the data coming from the buffered UART interface.

Column multiplexing

The matrix structure outlined in section 4.3.2 allows for a reduced wiring between the mainboard and the socketboard. In order to control this hierarchical structure the IO expander PCA9670 by NXP is connected to the power management bus. It has a total of eight outputs.

As already mentioned in section 5.2.2 five outputs are connected to the *ADJ* input of every voltage tracker in the column. Hence it is possible to individually switch a DUT on or off.

There are only five I2C busses available for DUT communication - one per row. They can be accessed by the devices if the respective I2C buffer of a DUT circuit (see section 5.2.1) is switched on. This is controlled via the sixth output of the PCA9670.

The remaining two output ports of the IO expander are used to activate the contact resistance measurement for a single column and to drive an activitiy LED.

Signal path

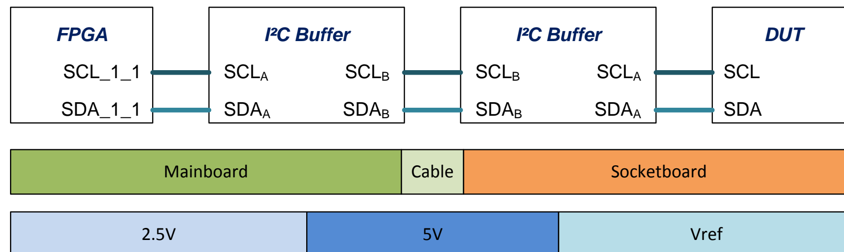

Figure 5.5: Signal path of an I2C channel

In figure 5.5 the basic way an I2C signal takes from the FPGA to the DUT on the socketboard is shown. Signals that are coming from the FPGA are within the 2.5 V domain which is the native IO voltage of the FPGA. Since the signals will be transmitted via an exposed cable they need to be transformed to a higher level.

In this case 5 V is selected as it is less susceptible for electromagnetic interference. In addition the voltage needs to be higher than the maximum value of V_{ref} because of the requirements by the used I2C buffers.

On either side of the cable the implemented I2C buffer is a PCA9509 produced by NXP. It has built in pull-up resistors for the lower voltage side (port A). This is a big advantage especially for the DUT circuit since those two resistors can be omitted. The buffer is also not degrading system performance which is essential in terms of test time and quality.

Pull-up resistors

Dimensioning of pull-up resistors on the I2C channels is necessary to ensure proper bus operation. Together with the capacitive load on the bus this determines the maximum possible frequency of the bus signals. Bus capacitance is influenced by attached devices and the cable or PCB trace.

As proposed in the I2C specification [12] a certain maximum rise time for the SDA and SCL lines is required depending on the operating mode of the bus. While many devices are very tolerant on out-of-specification signals a rough estimation on bus capacitance is necessary during board design.

Since the bus is designed as an open-drain bus the pull-up resistors are necessary to restore the high level. Too high resistors values would inevitably lead to scattered signals whereas too small resistor values could lead to glitches or higher crosstalk between SDA and SCL.

5.4 System monitoring

Monitoring a test system's health is necessary in order to determine the quality of its measurements. Especially high temperatures could easily lead to unexpected fails of ICs or at least unpredictable results.

In addition to the power monitoring as described in section 5.1.2 there are a few more components shown in figure 5.6. They comprise of the following sensors and identification devices:

Board-ID/EEPROM (Microchip 24AA025E48)
: This IC serves two purposes. First of all it has a unique ID which is used to identify the board in the software. Additionally there is 128 Byte memory available for storing extra identification data.

Reference temperature sensor (Analog Devices ADT7410)
: This sensor allows to precisely measure the board temperature. It can be used to determine if there are any deviations between the two socketboards which should not be the case under normal circumstances.

Reference acceleration sensor
: In order to be able to check for any centrifuge problems a reference sensor is built in. It is possible to read the acceleration over multiple turns thus a graph can be drawn showing any deviations from the required acceleration.

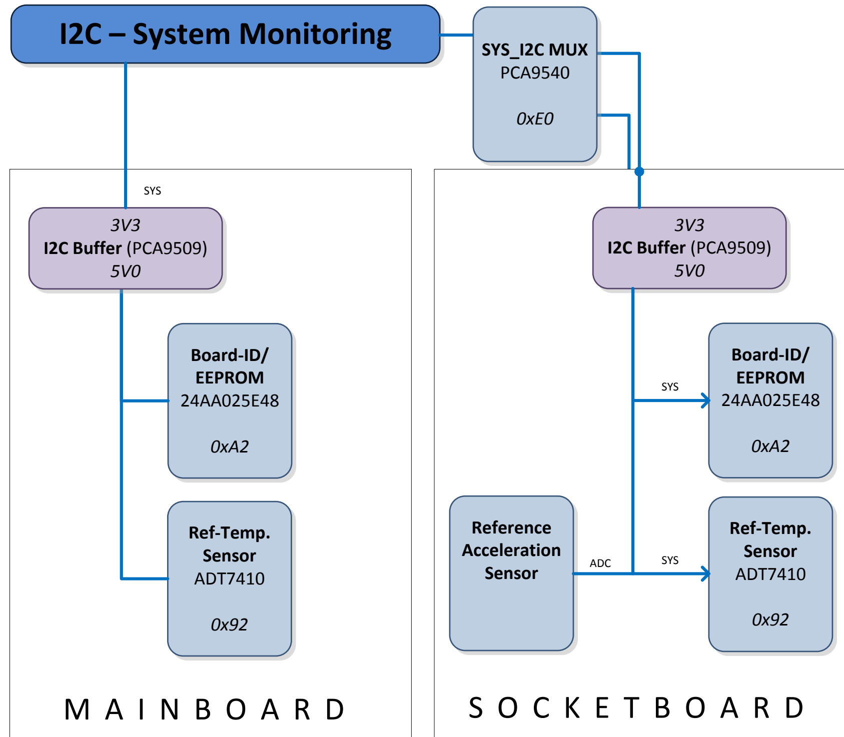

Figure 5.6: Overview of system monitoring sensors

5.5 DfM - Design for Maintainability

Design for Maintainability (DfM) is critical when developing a system that is supposed to be maintained in an environment where downtime is undesired. As soon as the system's development is finished and the production of the TPMS device starts the test system is handed over to the production. There is specially trained maintenance personnel available that is taking care of the system. Thus it should be possible to find errors fast and have the ability to easily correct them.

In the case of the developed system some initial requirements were set up in order to comply with the maintainability demanded by production:

Minimum IC package size
: The package size for discrete circuits should not be smaller than 0603 (imperial code; 1.6 mm x 0.8 mm) in size and for ICs any Ball Grid Array (BGA) footprints should be avoided. Nevertheless there are still components which are violating this rule, like the FPGA where a bigger package would not fit onto the board.

Testpoints
: For non-high-speed signals (below 1 MHz) testpoints are being placed on the PCB traces. It makes debugging substantially easier if one can simply hook an oscilloscope onto the actual signal. Unfortunately this is not possible for high speed or impedance-controlled signals as breaking up the trace could negatively affect signal integrity.

Equality of DUT circuits
: As already outlined in section 4.3.2, implementing a matrix structure using modern EDA tools, like *Altium Designer*, makes the design highly reusable. Not having such an ability in the software would result in an error prone search-and-replace activity in case of only one changed component or value. Hence all of the 160 DUT circuits on the actual socketboard are using the same schematics and layout.

Board robustness
: Although the boards are usually installed in the centrifuge maintenance will need to dismount them in case of an error. As this might happen quite soon if the board is assumed to be failing it should withstand those mounting cycles.

6 Conclusion

In the course of this thesis a new test system was developed that enables high-parallel testing and calibration of an accelerometer. Research on MEMS technology reveals the challenges from the fabrication of those devices. Consequentially the necessity to perform a calibration after the production is also given.

An embedded system in combination with an FPGA is used in order to cope with the required high parallelism. The test system is a functional tester with main focus on high parallel digital communication. Additionally analog measurement circuitry is included for roughly estimating device sanity.

Main challenge is to provide a mechanical robust system since it is installed in a centrifuge. The boards are experiencing high acceleration and thus must only contain solid-state devices. Hence the system requires passive cooling, requiring all of the used circuitry to be highly efficient in order to keep dissipated heat low.

In retrospect it can be said that the time for system development was slightly underestimated. There are many little things to consider when it comes to concept, component selection or design itself. Nevertheless this thesis reveals that it is possible to build a low-cost and low-power functional test equipment for semiconductor testing while still maintaining a high degree of precision.

After nearly one and a half years of conceptual and implementation work on the project behind this thesis there still is room for improvement. Regarding device communication an even higher degree of hard parallelism would be possible. This allows even further reduction of the test time.

Concerning the analog measurement circuitry to measure the DUT current a more integrated solution is conceivable. Especially a more granular control over the measurement could result in a higher system precision. Additionally the possibility on contact resistance measurement can be enhanced.

Since the semiconductor business and thus also the testing requirements are rapidly evolving it is not easy to estimate future demands. The signs bode well that the modularity and scalability for ICs and semiconductor modules will increase. In turn this will also facilitate system design for test engineering purposes.

As of now the first prototypes of the boards have been manufactured. They have proven to be fully functional during board verification. First tests in the centrifuge showed very promising results. Additionally the whole software environment is prepared for final productive use.

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