AFFIDAVIT

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ABSTRACT

The insatiable need for higher data rates in the communication market enforces communication systems in the long term to move up in frequency. In order to significantly boost channel capacities and therewith the net data throughput, frequencies in the higher microwave spectra need to be allocated in the future to provide sufficient bandwidth. This in turn makes even a greater demand on the measurement equipment to be able to build and test such communication systems in the first place. Especially power amplifiers (PAs) prove to be one of the key components in the transmitter chain of measurement instruments, since they mainly constitute the last performance bottleneck before the test signal is fed to the device under test (DUT).

Ever since solid-state PAs based on GaAs semiconductor technology came up in the early 80's, nearly all of the high-end applications, such as mobile communications, radar systems, military equipment or measurement instruments, comprise GaAs PAs as performance enabler for achieving high power at high frequencies. With the advent of commercial available GaN on SiC technology in 2005, a new chapter in III-V semiconductor technology has been openend. Peak power densities in continuous-wave mode up to 40 W/mm have been reported for AlGaN/GaN HEMTs on SiC in [1]. Out of the roughly four times higher power densities of GaN compared to GaAs (p)HEMTs, most of the GaAs PAs are/will be nowadays replaced by their GaN competitor to boost the output power for the next application generations. In particular, the high output power per capacitance ratio of GaN technology allows for better matching of the HEMT's input and output to the typical 50 Ω environment at higher frequencies. This in turn enables the implementation of wideband PAs over multiple decades, which makes this technology so attractive for the application in measurement instruments.

This work focuses on the realization of multi-decade broadband PAs in a 0.25µm GaN technology, which are optimized for the use in measurement instruments, such as e.g. signal generators. The most promising PA topologies for wideband operation from DC up to several GHz are the resistive feedback PA (FBPA) and the traveling-wave PA (TWA) or distributed PA (DPA), respectively. Since not only the maximum output power but moreover also linearity and noise play a decisive role for the applicability of GaN PAs in measurement instruments, this work investigates adequate wideband on-chip linearization and noise reduction concepts for FBPAs and TWAs in detail, which further improve the linearity and noise compared to conventional FBPA and TWA designs.

During the course of this work a DC-6 GHz FBPA was designed on the one hand in the conventional single-ended way and on the other hand in a truly-differential approach (TD-FBPA) in order to improve the harmonic distortion (HD) by even-order nonlinearity cancellation. The final TD-FBPA design showed to improve the $HD2$ by more than 25 dB and the overall $SFDR$ by 10 dB compared to the single-ended FBPA design, resulting in a $SFDR$ of -55 dBc at P_{OUT} = 25 dBm. Moreover an $OIP3$ at 1 GHz of 51 dBm and at 6 GHz of 46 dBm was measured for the TD-FBPA, which results in an improvement of more than 5 dB of the 3rd order intermodulation product, showing an outstanding linearity performance for a 4 Watt broadband FBPA in GaN technology. On top, the general small-signal stability of pseudo-differential (PD) and truly-differential (TD) amplifiers was analyzed, where the latter topology proved to be especially prone to CM-instabilities in GaN technology. Therefore, an analytical boundary condition for low frequency CM-stability dependent on the intrinsic HEMT parameters and the impedance environment was derived. The striking cause for the CM-instability in GaN technology was identified to be related to the small amount of feedback capacitance (C_{GD}) compared to the input (C_{GS}) and output (C_{DS}) capacitances. Especially for a usually given impedance environment of Z_0 = 50 Ω, the necessary

ratio of C_{GD} to C_{GS} and C_{DS} for low frequency stability is more severe. With increasing Z_0 and a higher transit-frequency (f_T), which results from a smaller C_{GS} and/or a larger g_m, the requirements for the necessary capacitance ratios become more relaxed. Based on these theoretical findings, remedies for CM-stabilization in TD-amplifiers, such as applying parallel feedback, omission of the gate-source field-plates or inductive compensation of the tail-current-source (TCS) capacitance, were deduced and verified by the DC-6 GHz TD-FBPA design.

For a similar frequency range from DC-6.5 GHz, a linearized low-noise TWA (L²NTWA) design, which makes use of a diode predistortion concept for the first time in a distributed structure, was designed with the goal of achieving high linearity and low-noise performance at the same time in a 2 W PA class. By means of an external diode-tuning voltage, the even- and odd-order linearity can be traded off against each other up to a certain degree without degrading the gain or I/O-RL of the L²NTWA to a greater extent. The measurement of the assembled MMIC in package showed a flat gain of larger than 14 dB from 10 MHz up to almost 7 GHz, whereby the lower operational frequency was only limited by the values of the off-chip SMD components. Linearity measurements additionally revealed a high linearity with a maximum $SFDR$ of -38 dBc at P_{OUT} = 25 dBm and an $OIP3$ of larger than 42 dBm at its optimum diode-tuning voltage. A minimum NF of 1.8 dB at 2 GHz was measured for the nominal bias point of V_{DS} = 28 V and I_{DS} = 200 mA/mm. Together with a P_{1dB} of greater than 1 W over the whole band, the design classifies into the high power LNA class and is perfectly suited as a highly linear low-noise driver stage for their DC-6 GHz GaN FBPA or TD-FBPA counterparts.

In terms of noise performance, conventional TWAs exhibit a significant increase in noise toward low frequencies, which makes this topology inappropriate for low frequency applications in measurement instruments. By means of a DC-15 GHz reference design, the steep increase in NF below 2 GHz was verified by measurements, after identifying all different noise contributors. The corresponding transfer functions to the output of all present noise sources were calculated mathematically and the contribution to the overall NF analytically evaluated. The largest low frequency noise contribution was identified to originate from the gate bias resistors, when capacitive gate-coupling is applied. If no capacitive gate-coupling is present, the gate-line termination resistor introduces the second largest amount of noise to the output due to the TWA's inherent reverse transfer function from the gate-termination to the output. In order to minimize this noise contribution, three distinct active cold load (ACL) concepts are reviewed and theoretically analyzed in order to find the best suited topology for TWAs. Out of the three different ACL concepts, the common-source topology with parallel resistive feedback (CS-PRF) proved to be the most suited one. Furthermore, among the two presented possibilities of terminating the gate-line with the CS-PRF ACL at either the last stage of the TWA or as substitution of the resistive load, the latter showed from the analysis to be the more promising solution with respect to the targeted gain and ORL of the TWA. Nevertheless, the analysis revealed that both methods are effective to minimize the low frequency noise. Based on the preceding analysis the more suited CS-PRF ACL concept was combined with an upstream RLC-filter to obtain a wider input match, which is also called "blue noise active termination" (BNAT) due to its shaped high frequency noise spectrum. The BNAT was first of all designed on a separate die to verify its general functionality by on-wafer measurements. After successful proof of concept the BNAT was attached to the L²NTWA design to investigate the degree of NF improvement compared to a resistive load. The NF measurements showed an improvement of 1.9 dB from 5.5 dB with resistive load down to 3.6 dB with BNAT.

KURZFASSUNG

Die unstillbare Nachfrage nach höheren Datenraten im Kommunikationssektor zwingt langfristig Kommunikationssyteme bei höheren Frequenzen zu arbeiten. Um die Kanalkapazität und damit den Netto-Datendurchsatz zu steigern, müssen die Trägerfrequenzen in Zukunft immer weiter ins höhere Mikrowellenspektrum verschoben werden, um ausreichend Bandbreite zur Verfügung zu stellen. Dies wiederum stellt noch höhere technische Anforderungen an die Messinstrumente, damit derartig hochfrequente Kommunikationssysteme überhaupt gebaut und getestet werden können. Im Speziellen stellen breitbandige Leistungsverstärker eine der Schlüsselkomponenten in Sendesignalpfaden von Messinstrumenten dar, da diese als letzte aktive Komponente vor der Herausführung des Testsignals zum Messobjekt (DUT) maßgeblich die Signalintegrität beeinflussen.

Seit dem Aufkommen von GaAs Halbleitertechnologie in den 80er Jahren, beinhalten fast alle High-End Andwendungen, wie z. B. die Mobilkommunikation, Radarsysteme, Militärgeräte oder Messinstrumente, GaAs MMIC PAs um hohe Leistungen bei hohen Frequenzen zu realisieren. Mit der Etablierung kommerziell verfügbarer GaN auf SiC Technologie seit 2005 wurde ein neues Kapitel in der Geschichte der III-V Halbleitertechnologie geöffnet. Spitzenleistungsdichten im CW-Betrieb von bis zu 40 W/mm für AlGaN/GaN auf SiC wurden in [1] demonstriert. Aufgrund der ungefähr viermal höheren Leistungsdichte von GaN HEMTs im Vergleich zu GaAs HEMTs wird ein Großteil der GaAs PAs heutzutage durch die konkurrierende GaN Technologie ersetzt, um die Ausgangsleistung in Anwendungen für neuere Generationen zu steigern. Besonders das Verhältnis von Ausgangsleistung zu Kapazität ermöglicht bei höheren Frequenzen eine bessere Eingangs-/Ausgangsanpassung der GaN HEMTs in einem 50 Ω - System. Dies wiederum ermöglicht es breitbandige PAs über mehrere Dekaden zu realisieren, was diese Technologie so attraktiv für Anwendungen in Messinstrumenten macht. Diese Arbeit konzentriert sich daher auf die Realisierung von breitbandigen PAs über mehrere Frequenzdekaden in 0.25µm GaN Technologie, die für den Einsatz in Messinstrumenten, wie z. B. Signalgeneratoren (SG), optimiert sind. Für breitbandigen Betrieb von DC bis zu mehreren GHz sind die zwei vielversprechendsten PA Topologien zum Einen der resistive Rückkopplungsverstärker (FBPA) und zum Anderen der Wanderwellen (TWA) oder verteilte (DPA) PA. Da nicht nur die maximale Ausgangsleistung sondern auch die Linearität und das Rauschen eine entscheidende Rolle für die Eignung von GaN PAs in Messinstrumenten spielt, widmet sich diese Arbeit der detaillierten Untersuchung von geeigneten breitbandigen Linearisierungs- und Rauschminimierungskonzepten, welche die Linearitäts- und Rauscheigenschaften speziell von FBPAs und TWAs auf Chipebene verbessern.

Im Laufe dieser Arbeit wurde ein DC-6 GHz FBPA zum einen auf konventionelle unsymmetrische Weise (FBPA) und zum anderen in voll-differentieller Form (TD-FBPA) entworfen, um die harmonischen Verzerrung (HD) durch Auslöschung der geradzahligen Harmonischen zu verringern. Das finale Design des TD-FBPA zeigt im Vergleich zum unsymmetrischen FBPA dabei eine Verbesserung des $HD2$ von 25 dB und der $SFDR$ von 10 dB auf, was in einer $SFDR$ von -55 dBc bei P_{OUT} = 25 dBm resultiert. Darüber hinaus wurde ein $OIP3$ bei 1 GHz von 51 dBm und bei 6 GHz von 46 dBm gemessen, was zu einer Verbesserung des Intermodulationsprodukts dritter Ordnung von mehr als 5 dB führt. Dies zeigt das herausragende Gesamtlinearitätsverhalten eines 4 Watt DC-6 GHz FBPAs. Zusätzlich wurde die Kleinsignalstabilität von pseudo-differentiellen (PD) und voll-differentiellen (TD) Verstärkern untersucht, wobei sich heraustellte, dass letztere Topologie speziell in GaN Technologie anfällig für Gleichtaktinstabilitäten ist. Aus diesem Grund wurde eine analytische Grenzbedingung für die niederfrequente Gleichtaktstabilität in Abhängigkeit der intrinsischen HEMT Parameter und Umge-

bungsimpedanz hergeleitet. Als ausschlaggebendes Kriterium für die Gleichtaktinstabilität in GaN Technologie kann auf die kleine Rückkopplungskapazität (C_{GD}) im Vergleich zur Eingangs- (C_{GS}) und Ausgangskapazität (C_{DS}) zurückgeführt werden. Speziell für die übliche Umgebungsimpedanz von Z_0 = 50 Ω ist die niederfrequente Stabilitätsanforderung and das Verhältnis von C_{GD} zu C_{GS} und C_{DS} äußerst hoch. Mit steigendem Z_0 und höheren Transitfrequenzen (f_T), sprich kleinerem C_{GS} und größerem g_m, verringert sich die Anforderung an das notwendige Kapazitätsverhältnis. Basierend auf diesen theoretischen Erkenntnissen wurden Gegenmaßnahmen zur Gleichtaktstabilisierung abgeleitet, wie z. B. das Hinzufügen einer parallelen Rückkopplung, das Entfernen der Gate-Source Feldplatten oder durch eine induktive Kompensation der parasitären Kapazität der Versorgungsstromquelle und diese mit Hilfe des DC-6 GHz TD-FBPA Designs verifiziert.

Für einen ähnlichen Frequenzbereich von DC-6.5 GHz wurde ein linearisierter rauscharmer TWA (L²NTWA) mit integriertem Dioden-Vorverzerrungskonzept zum ersten Mal in einer verteilten Struktur entworfen, mit dem Ziel gleichzeitig hohe Linearität und geringes Rauschen in einem 2 W PA zu erzielen. Mit Hilfe einer externen Dioden-Abstimmspannung können die geraden als auch ungeraden Harmonischen bis zu einem bestimmten Grad gegeneinander abgewägt werden ohne die Verstärkung oder die Eingangs-/Ausgangsanpassung des L²NTWAs signifikant zu verschlechtern. Die Messungen des assemblierten gehäusten MMICs zeigen einen flachen Verstärkungsverlauf von größer 14 dB über einen Frequenzbereich von 10 MHz bis fast hoch zu 7 GHz, wobei die untere Grenzfrequenz lediglich von den Werten der externen SMD Komponenten bestimmt wird. Die Linearitätsmessungen haben zusätzlich gezeigt, dass eine hohe Linearität mit einem maximalen störungsfreien dynamischen Bereich ($SFDR$) von -38 dBc bei einer Ausgangsleistung von P_{OUT} = 25 dBm und ein $OIP3$ von größer als 42 dBm bei optimaler Dioden-Abstimmspannung erreicht wird. Messungen der Rauschzahl (NF) haben ein minimum von 1.8 dB bei 2 GHz für den nominalen Arbeitspunkt von V_{DS} = 28 V and I_{DS} = 200 mA/mm ergeben. In Kombination mit einem P_{1dB} von über 1 W über das komplette Frequenzband ordnet sich dieses Design in die Hochleistungs-LNA-Klasse ein und ist somit geeignet als hoch lineare und rauscharme Treiberstufe für den vorher erwähnten DC-6 GHz FBPA oder TD-FBPA.

Konventionelle TWAs weisen in der Regel einen erheblichen Anstieg des Rauschens zu niedrigen Frequenzen auf, was diese Verstärkertopologie in Bezug auf ihr Rauschverhalten für die niederfrequente Anwendung in Messgeräten ungeeignet macht. Mit Hilfe eines DC - 15 GHz Referenzdesigns wurde der steile Anstieg der NF unterhalb von 2 GHz messtechnisch verifiziert, nachdem alle Rauschquellen identifiziert wurden. Die zugehörigen Rauschübertragungsfunktionen zum Ausgang wurden jeweils mathematisch berechnet und der Beitrag zur gesamten NF analytisch bewertet. Der größte Anteil des niederfrequenten Rauschens stammt von den Gate-Vorspannwiderständen für den Fall, dass die Gates kapazitiv gekoppelt sind. Ist dies nicht der Fall, dann steuert der Gate-Leitungsabschlusswiderstand aufgrund des typischen Verlaufs der Rückwärtsübertragungsfunktion von der Abschlusslast zum Ausgang den zweitgrößten Rauschanteil bei niedrigen Frequenzen bei. Um diesen Rauschbeitrag zu minimieren wurden drei unterschiedliche rauscharme Lastkonzepte (ACL) untersucht und theoretisch analysiert, um die am besten geeignete Topologie für TWAs zu identifizieren. Von diesen drei ACL-Konzepten erwies sich die Common-Source Topologie mit paralleler Rückkopplung (CS-PRF) als äußerst geeignet. Dabei gibt es prinzipiell zwei verschiedene Ansätze, um die Gate-Leitung mittels der CS-PRF abzuschließen. Beim ersten Ansatz wird die letzte aktive Stufe im TWA ersetzt wohingegen beim zweiten Ansatz der resistive Gate-Leitungsabschlusswiderstand direkt ersetzt wird. Letztere Methode zeigt ausgehend von einer vereinfachten mathematischen Analyse, dass diese die vielversprechendere Lösung in Bezug auf die Verstärkung und die Ausgangsanpassung des TWAs ist. Dennoch sind beide Ansätze effektive Maßnahmen, um das niederfrequente Rauschen in TWAs zu minimieren. Basierend auf der vorhergehenden Analyse wurde das CS-PRF Konzept mit einem vorgeschalteten RLC-Filter kombiniert, um eine breitbandigere Eingangsanpassung des

TWAs zu ermöglichen. Diese Schaltung wird auch als „aktive blaue Rauschlast“ (BNAT) bezeichnet, da ihr resultierender Rauschfrequenzgang in Analogie zum Lichtspektrum blauem Licht entspräche. Zur Verifizierung wurde die BNAT zunächst auf einem separaten Chip entworfen, um die generelle Funktionalität messtechnisch zu verifizieren. Nach erfolgreicher Überprüfung des Konzeptes wurde die BNAT als Gate-Leitungsabschlusslast zum bestehenden L^2NTWA Design hinzugefügt, um den Grad der niederfrequenten NF Verbesserung im Vergleich zu einer resistiven Abschlusslast zu evaluieren. Die Rauschmessungen ergaben eine Verbesserung der NF um 1.9 dB von 5.5 dB mit resistiver Last auf 3.6 dB mit aktiver Rauschlast (BNAT).

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Symbol	Description	Unity
α	Conduction angle	rad or °
Δa	Amplitude imbalance	V
$\beta_{G/D}$	Phase coefficient of gate-/drain-line	1/m
Γ_S	Source reflection coefficient	-
$\Gamma_{S,opt}$	Optimum source reflection coefficient for noise match	-
ε_r	Relative dielectric constant	F/m
$\varepsilon_{r,eff}$	Effective relative dielectric constant	-
η_{max}	Maximum efficiency	%
λ	Wavelength	m
μ, μ'	Small-signal stability measure at output / input	-
$\Delta\phi$	Phase imbalance	rad or °
ω	Angular frequency	rad
$ABCD$	Chain parameters / ABCD-parameters	
$ACPR$	Adjacent channel power ratio	(dBc)
$\underline{c}$	Complex noise correlation coefficient	-
$c_{re/im}$	Real-/imaginary-part of noise correlation coefficient	-
C_{DS}	Drain-source capacitance	F
C_{GD}	Gate-drain capacitance	F
C_{GS}	Gate-source capacitance	F
C_P	Power handling capability	-
$\overleftrightarrow{C}_{I,Rx}$	Noise correlation matrix in immittance parameter form of resistor R_x	
$\overleftrightarrow{C}_{I,Tfx}$	Noise correlation matrix in immittance parameter form of HEMT plus $R_{fp/fs}$	
$CMRR$	Common-mode rejection ratio	(dB)
E_{BD}	Electric breakdown field	V/m
f	Frequency	Hz
f_c	Cut-off frequenc	Hz
f_H	Upper frequency corner	Hz
f_L	Lower frequency corner	Hz
f_0	Center frequency	Hz
f_{max}	Maximum frequency of oscillation	Hz
f_T	Transit frequency	Hz
F, F_{min}	Noise factor, minimum noise factor	-
g_m	Complex transconductance	S
$g_{m,0}$	Magnitude of transconductance	S
G_V	Voltage gain	(dB)
h	Substrate height	m
$HD2/3$	Harmonic distortion of 2nd/3rd order	dBc
H_n	Harmonic signal component of n^{th}-order	V or A
$\underline{i}_{n,\mathrm{G/D}}$	Complex induced-gate/channel noise current	A
I_{DC}	DC current	A
$I_{\mathrm{D},i}$	Drain-current of i^{th}-stage	A

I_{DS}	Drain-source current	A
$I_{\mathrm{DS},max}$	Maximum drain-source current	A
I_{GS}	Gate-source current	A
$IM3$	3rd order intermodulation product	(dBm)
I_P	Peak current	A
k_B	Boltzmann constant	J/K
$l_{G/D}$	Length of gate-/drain-line section	m
MAG	Maximum available gain	dB
MSG	Maximum stable gain	dB
m_T	Process mismatch factor between two transistors	-
N	Number of stages	-
$NCSD$	Noise current spectral density	A /$\sqrt{\mathrm{Hz}}$
NF	Noise figure	
$NVSD$	Noise voltage spectral density	V /$\sqrt{\mathrm{Hz}}$
$OIP3$	3rd order output intercept point	-
$P_{OUT}, P_{OUT,max}$	Output power, maximum output power	W (dBm)
Q	Quality factor	-
R_{DS}	Drain-source resistor	Ω
R_{fp}	Parallel feedback resistor	Ω
R_{fs}	Series feedback resistor	Ω
$R_{GT/DT}$	Gate/drain-line termination resistor	Ω
R_{GS}	Gate-source resistor	Ω
R_n	Equivalent noise resistance	Ω
S_{ij}	Scattering parameters	-
SNR	Signal-to-noise ratio	dB
τ	Channel transit time	s
T	Temperature	K
TGW	Total gate width	m
UGW	Unity gate width	m
$V_{\mathrm{D},i}$	Drain-voltage of i^{th}-stage	V
V_{DS}	Drain-source voltage	V
V_{GD}	Gate-drain voltage	V
V_{GS}	Gate-source voltage	V
V_{IN}	Input voltage	V
V_{kn}	Knee-voltage	V
V_{OUT}	Output voltage	V
V_{th}	Gate threshold voltage	V
W_{G}	Gate-width of HEMT	m
Y_{ij}	Admittance parameters	S
Y_{opt}	Optimum noise admittance	S
Z_{ij}	Impedance parameters	Ω
Z_0	Characteristic impedance	Ω
$Z_{0,G/D}$	Characteristic gate/drain-line impedance	Ω
Z_L	Load impedance	Ω
Z_S	Source impedance	Ω

ABBREVIATIONS

2DEG	two dimensional electron gas
3GPP	3rd generation partnership project
III-V	chemical element of 3rd and 5th group in periodic table
ACL	active cold load
CM	common-mode
CG	common-gate
CS	common-source
CW	continuous wave
DA	distributed amplifier
DPA	distributed power amplifier
DUT	device under test
DSM	derivative superposition method
EDGE	enhanced data rates for GSM evolution
FFNC	feed-forward noise cancellation
GaAs	gallium arsenide
GaN	gallium nitride
GSM	global system for mobile communications
HEMT	high electron mobility transistor
HSPA	high speed package access
IMN	input matching network
ISV	individual source via
LDMOS	laterally diffused metal oxide semiconductor
LNA	low noise amplifier
L²NTWA	linear low-noise traveling-wave amplifier
LTE	long term evolution
MIM	metal-insulator-metal
MMIC	monolithic microwave integrated circuit
OFDM	orthogonal frequency division multiplex
OMN	output matching network
PA	power amplifier
PAE	power added efficiency
PAPR	peak to average power ratio
PCB	printed circuit board
PDK	process design-kit
PD	pseudo-differential
PEP	peak envelope power
pHEMT	pseudomorphic HEMT
PLL	phase locked loop
PRF	parallel resistive feedback
SG	signal generator
SiC	silicon carbide (chemical element)
SIF	series inductive feedback

SiGe	silicon germanium (chemical element)
TCXO	temperature compensated crystal oscillator
TD	truly-differential
TD-SCDMA	time division synchronous code division multiple access
TFR	thin-film resistor
TWA	traveling-wave amplifier
TWTA	traveling-wave tube amplifier
UMTS	universal mobile telecommunications system
VCCS	voltage-controlled current source
VNA	vector network analyzer
VSG	vector signal generator
WiMAX	worldwide interoperability for microwave access
WCDMA	wideband code division multiple access
WLAN	wireless local area network

CHAPTER 1

INTRODUCTION

The advent of III-V solid-state semiconductors in the early 1980´s, as i.e. gallium-arsenide (GaAs), enabled the manufacturing and integration of high power and high frequency devices on small integrated circuits for the first time in history. Due to their small feature sizes, high frequency operation up to several tens of GHz could be realized on one single chip, leading to the birth of the so called microwave monolithic integrated circuits (MMIC). This starting miniaturization, combined with the continuous progress in manufacturing larger wafers, led some years later to a significant reduction in costs, which is nowadays the primary driving force for the economical acceptance of new semiconductor technologies. As the mobile communication market started to emerge in the mid 1990´s in the U.S. and Europe, mobile phones and later partly base station transmitters were equipped with commercial available GaAs power amplifiers (PA), replacing the hitherto existing maintenance-intensive electron tubes. Despite being more and more replaced by silicon (Si) laterally diffused metal oxide semiconductor (LDMOS) transistors in base station transmitters, GaAs technology is due to its compactness and high efficiencies still present in power amplifier modules in the 2G up to 4G mobile phone market, as e.g. in the iPhone or Samsung Galaxy S smartphone generations. A real breakthrough in III-V semiconductor technology has been achieved with the advent of gallium nitride (GaN) on silicon carbide (SiC) substrates in the early 2000´s. Based on GaN´s high intrinsic bandgap of $E_G = 3.4$ eV, higher breakdown voltages and therewith larger output powers can be achieved opposed to GaAs or Si semiconductor, exhibiting bandgaps of only 1.4 eV and 1.1 eV, respectively. When the power-bandwidth product per chip area is considered, III-V semiconductors prove to be superior in performance to their Si and SiGe counterparts. The use of III-V semiconductor based PAs proves to present the optimum solution for realizing high output powers from the C- up to D-band, as it is nowadays the case e.g. in several military applications. In particular in the small market niche of measurement instruments is the development of GaN technology eyed with growing interest, since GaAs PAs transpire to become more and more a decisive bottleneck for the next generations of high performance measurement instruments. Based on the recent advances in manufacturing and the increasing commercial availability of GaN, GaN is deemed to be the next promising III-V semiconductor candidate for the implementation of a new generation of high performance measurement instruments.

1.1 Motivation

The development of leading edge MMICs or RFICs for all different kind of technical applications requires high performance measurement systems in order to characterize the performance of the chips accurately. It is therefore a substantial precondition that the measurement system itself provides a higher dynamic range (DR) than the device under test (DUT) in order to obtain accurate measurement results. On this account, great demands are made on the internal components of the measurement instrument with respect to bandwidth, power, linearity and noise. By focusing on the application of high power MMICs in microwave signal generators (SG), this work examines and develops MMIC PAs in AlGaN/GaN on silicon carbide (SiC) technology, which are capable of realizing high DRs and are hence suitable for the implementation of PA modules in SGs. To understand the performance requirements for the MMIC PA imposed by the SG system, it is first of all necessary to grasp the implications for the PA MMIC within the system.

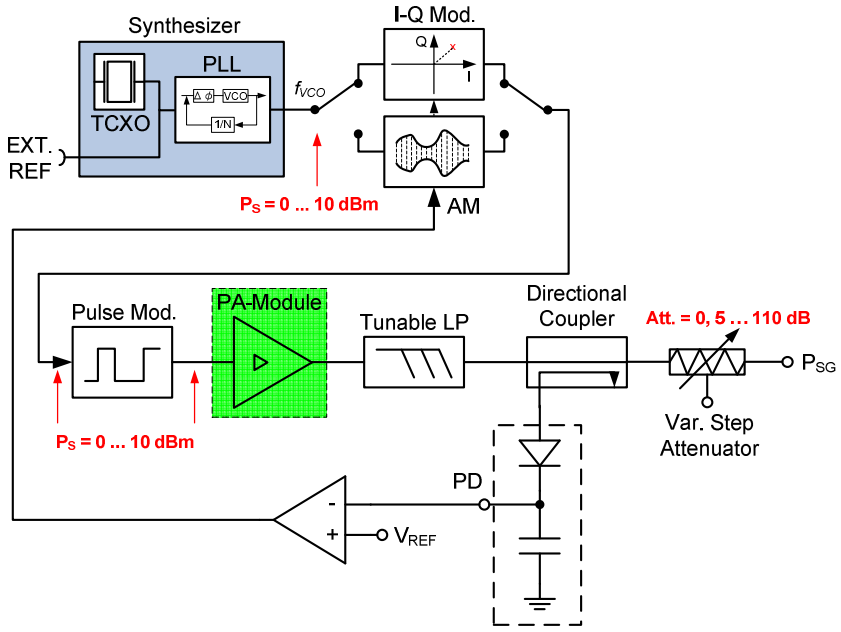


Fig. 1-1: Typical component blocks of an analog/vector microwave signal generator

A typical analog/vector SG with its basic building blocks is depicted in Fig. 1-1. First of all a stable reference frequency f_{ref} has to be synthesized, either by an internal temperature compensated crystal oscillator (TCXO) or by an external reference oscillator over the EXT. REF port. Usually f_{ref} is around 10 MHz. By means of this stable reference, different stable carrier frequencies can be synthesized by a phase locked loop (PLL), where the desired carrier frequency at the output of the PLL can be controlled by the division ratio N of the frequency divider in the feedback path of the PLL. The output frequency of the synthesizer`s PLL is then set to

$$f_{VCO} = N \cdot f_{ref}, \tag{1.1}$$

where N has to span large intervals in order to synthesize frequencies from a few kHz up to several GHz. Dependent on the type of SG, the stable carrier frequency f_{VCO} is now processed by either an amplitude modulator (AM), in the case of an analog SG, or by an in-phase quadrature-phase (IQ)-modulator, in the case of a vector SG (VSG). The final step in the signal synthesis chain is the pulse modulation of the analog AM/complex IQ-signal, where the signal can be additionally modulated by on-off keying (OOK) or even more complex pulse modulation schemes. After modulating the information in the AM/IQ-modulator and pulse modulator onto the carrier, the information signal has to be amplified linearly to attain a distortion free signal with the desired output power at the output socket of the microwave SG. This is realized in the so-called front-end part of the SG. Within this part plays the PA module the key role in maintaining signal integrity, since the signal quality cannot be improved by the subsequent attenuator.

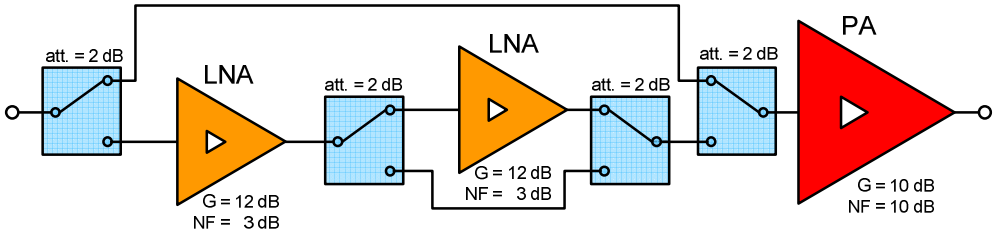


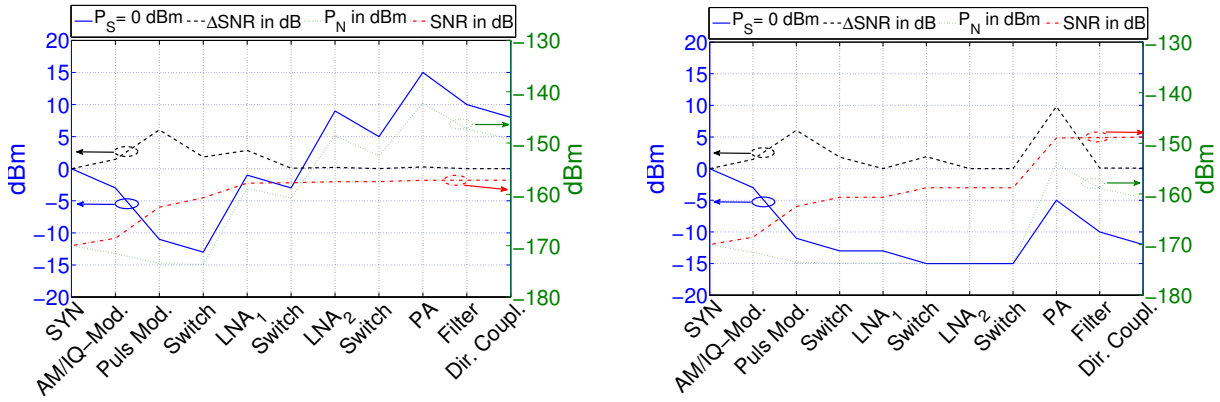
Fig. 1-2: PA module of microwave signal generator with typical commercial MMICs

The PA module itself is in general composed of several switchable LNAs in cascade, followed by the PA MMIC. Fig. 1-2 shows a typical SG PA module with only two LNAs for simplicity. The number of cascaded LNAs depends on the maximum interruption-free DR of the corresponding SG in order to cover the specified full output power range at the SG´s output socket. Thereby it is important to distinguish between the characteristic DR and the interruption-free DR of the SG. The former refers to the maximum DR which can be realized by stepping the attenuation in the variable step attenuator and additionally sweeping the power level electronically, whereas the latter can only be obtained by electronically increasing or decreasing the power level at a fixed attenuation level of the variable step attenuator. Based on the interruption-free DR specifications in the order of magnitude of 20 to 30 dB, two implications with respect to noise and linearity at the lower and upper end of the DR can be drawn.

- First, too much signal attenuation within the signal chain degrades the SNR either when the signal power P_S drops below a minimum specified power level or when the system´s noise floor drops below the systems minimum noise power density.
- Second, signals with too large voltage swing degrade the linearity by signal clipping. Choosing higher power levels to allow more attenuation comes with the drawback of more costly active circuit components.

Thus, it is important to keep the power level within the signal path within a certain power level range in order to avoid SNR and linearity degradation. To fully understand these two system constraints it is meaningful to take a closer look at the power-leveling within the SG`s signal path. Fig. 1-3 illustrates the power levels of the signal, noise and their corresponding signal-to-noise ratios (SNR) at the output of the individual building blocks in the SG chain from Fig. 1-1. Assuming that the signal power at the output of the frequency synthesis block is at the lower end of the power level range and equal to $P_S = 0$ dBm and the power P_{SG} at the output socket of the

SG is electronically leveled down from e.g. 8 dBm to -12 dBm, it is necessary to bypass the upstream LNAs depicted in Fig. 1-2 in the signal path to reduce the overall gain. As can be seen from the ΔSNR- and SNR-curves in Fig. 1-3 (a) and (b), bypassing the LNAs leads to a reduction in SNR, which is mainly contributed by the noise of the PA. At first sight, realizing the required gain only by the PA seems to make no sense according to Friis-formula for noise in cascaded stages [2]. In terms of noise it would be preferable to bypass the PA instead of the LNA to avoid attenuation before amplification.



(a) (b)

Fig. 1-3: Power-levels in SG chain for P_S = 0 dBm with (a) 2 LNAs + PA and (b) PA only

Unfortunately, this would lead to constraint number two, because in this case the spurious free output signal has to be generated by the first LNA in the PA module. Since the maximum available output power of LNAs is usually by far smaller than the one of PAs and the first LNA is located even further away from the output socket with additional lossy components in between, the output power and accordingly the available DR at the output socket of the SG will be reduced. Commonly, a spurious free dynamic range ($SFDR$) of larger than 70 dBc at the SG´s output socket is specified, which requires an additional multi-decade tunable low-pass (LP) filter behind the PA module to suppress higher in-band harmonics. If smaller $SFDR$s of about 40 dBc are tolerated the tunable LP-filter is often arranged in front of the PA module to obviate additional attenuation introduced by the LP-filter behind the PA module. This relaxes the maximum power specifications for the PA MMIC but sets more stringent specifications in terms of harmonic distortion ($HD2$, $HD3$). With respect to intermodulation ($IP3$, $ACPR$) the arrangement of the tunable LP-filter position is irrelevant, because undesired intermodulation products are too close to the carrier to be filtered out. Since $HD3$ and $IP3$ are mutually dependent, as will be shown in chapter 4.1, good intermodulation performance premises low HD and vice versa.

Inferring from the two above mentioned constraints inflicted by the SG system, a PA MMIC design compromise between high power, high linearity and low noise results. Additionally, the PA MMICs have to cover very broad frequency ranges from only a few kHz up to tens of GHz. Table 1-1 gives a general overview over typical system requirements regarding small-signal performance, output power, linearity and noise, which are imposed on the PA MMIC by three different SG classes with operational frequencies from 10 MHz up to 6, 13 and 20 GHz.

Table 1-1: Typical MMIC PA specifications for next generation SGs

Parameter	Specification
f_{min}	10 MHz
f_{max}	6/13/20 GHz
G_P	9 - 12 dB
Gain Flatness	± 0.5 dB
I/O-RL	> 10 dB
Isolation	< -30 dB
max. P_{in}	> 25 dBm
P_{sat}	> 35 dBm
$OIP3$	> 40 dBm
$SFDR$ @ P_{OUT} = 25 dBm	< -40 dBc
NF	< 5 dB
Operating Temp.	0…85°C

1.2 Challenges and Questions

This work focuses on the development of multi-decade broadband PAs with high linearity and low-noise performance for the application in measurement instruments. GaN technology proves to be a promising candidate for the implementation of high power and high frequency PAs, featuring high linearity and low noise at the same time. In order to further boost linearity and minimize noise, suitable concepts for the linearization and noise reduction of two well-known broadband amplifier topologies will be examined. These two are the feedback PA (FBPA) on the one hand and the distributed or traveling-wave PA (DPA/TWA) on the other.

Throughout the course of this work the following questions will be answered:

- What are typical specifications for power amplifiers in broadband measurement instruments?
- What kind of noise models are suited for the description of thermal noise in GaN HEMTs?
- Is there a difference between small-signal, noise and power matching?
- How does the power matching of each stage in a TWA look like?
- What are the noise sources in TWAs and to which extent do they contribute to the overall output noise?
- By means of which measures and concepts can low frequency noise be effectively reduced in TWAs?
- Which intrinsic elements of the HEMT are the dominant contributors to nonlinearity?
- How can linearity be “tweaked” by adjusting the bias point of the PA?
- What kind of on-chip linearization concepts are suited for broadband PAs and what are the trade-offs?
- Is a truly-differential topology with respect to linearity, noise and output power superior toward a pseudo-differential topology?
- Are phase, amplitude and process imbalances more critical for the pseudo- or truly-differential pair?
- How critical is common-mode stability for the design of truly-differential pairs based on GaN technology?

1.3 “State-of-the-Art” Broadband GaN PAs

Among the increasing number of publications on GaN PAs in the last decade there are only a few which deserve to be entitled “broadband PA designs”. Since most of the publications are mainly driven by the communication standards UMTS or LTE nowadays and therefore focus on concepts and techniques for increasing efficiency in S/C-band by using digital predistortion (DPD) as e.g. in [3, 4, 5], envelope tracking (ET) as e.g. in [6, 7, 8] or more recently outphasing (OP) as e.g. in [9, 10, 11], none of these approaches can be efficiently implemented over more than a single octave. For real “broadband” designs up to multiple octaves only two well-known and almost “ancient” PA topologies exist. This is on the one hand the feedback power amplifier (FBPA) and on the other hand the traveling-wave amplifier (TWA or DPA). These two concepts will be explained in more detail in Chapter 3.

Table 1-2: "State-of-the-Art" GaN FBPAs

Ref.	L_G /µm	Topology	f /GHz	P_{sat} /dBm	P_{1dB} /dBm	G_P /dB	ΔG_P /dB	$OIP3$ /dBm	NF /dB	Area /mm²
[12]	0.25	CC-FBPA	1.0-2.0	> 39	> 38.5	> 19.0	±0.5	> 50	2.5-3.0	2.1
[13]	0.35	CS-FBPA	0.1-4.0	> 32.5	-	> 13.5	±0.5	-	-	-
[14]	0.2	CS-FBPA	0.2-8.0	> 34	> 33	8-19	±5.5	> 43	< 1.2	2.9
[15]	0.2	DS-FBPA	1-25	-	17.5	> 10	±1.5	>28.5	3.5-4.5	1.45
This Work	0.25	CS-FBPA	0.01-6.0	> 36	> 33	> 9	±0.5	> 42	3.5-5.0	4.35
This Work	0.25	TD-CS-FBPA	0.01-6.0	> 35	> 33	> 10	±0.5	> 45	4.5-6.0	8.15

Table 1-3: "State-of-the-Art" GaN TWAs

Ref.	L_G /µm	Topology	f /GHz	P_{sat} /dBm	P_{1dB} /dBm	G_P /dB	ΔG_P /dB	$OIP3$ /dBm	NF /dB	Area /mm²
[16]	-	DG-UDPA	2-32	30	-	> 12	±1.0	-	-	-
[17]	0.25	Bal.-NDPA	6-18	> 41	-	> 9.0	±1.0	-	-	18.7
[18]	0.2	DS-DG- UDPA	2-18	> 26	-	> 18.5	±2.0	-	-	8
[19]	0.2	Casc.- UDPA	0.2-24	> 30	> 25	> 10.5	±3.0	> 36	< 8	4.8
		CC-Casc.- UDPA	0.2-20	> 29	> 26	> 10.5	±1.5	> 36	< 16	4.8
[20]	0.2	Bal.-NDPA	1 – 6	> 43	-	> 8.5	±1.5	-	-	47.4
[21]	0.2	Bal.-NDPA	2-18	> 41	-	> 10	±2.0	-	-	38.25
This Work	0.25	CS-UDPA	0.01-15	> 37	> 33	> 10.5	±0.5	> 40	< 7	12.5
This Work	0.25	CS-NDPA	0.2-20	> 36	> 32	> 8.0	±1.0	> 40	-	8.3
This Work	0.25	CS-UDPA with AT	0.01-6.5	> 34	> 29	> 15.0	±1	> 42	< 5.5	12.5

Table 1-2 and Table 1-3 shall give an overview of existing state-of-the-art FBPA- and TWA-designs in GaN technology. Both tables show a benchmark of competitive exisiting GaN PA designs in comparison with the designs developed within this work. At first glance it can be recognized that the number of references is very limited, because only a few publications exist which exhibit comparable wide-band performance. With respect to the large number of parameters of interest, such as power, linearity and noise, it is very difficult to classify the achievements of this work in a straightforward manner. Due to the fact that not all parameters are presented in the given reference designs, it is furthermore not possible to come up with a meaningful FoM, which combines all performance parameters of interest, such as matching, output power, linearity and noise. The latter aspect impedes thus to end up with a definite classification of the designed PAs within this work.

1.4 Thesis Synopsis

This thesis is structured into five different main parts, which discuss the following topics:

Chapter 2 gives basic background about gallium nitride (GaN) from a purely technological perspective. After a short review of the physical properties of GaN, the process stack and the epitaxial structure of AlGaN/GaN HEMTs on s.i. SiC substrate will be presented. Additionally, typical process parameters of the utilized GaN25 (0.25µm AlGaN/GaN on s.i. SiC) technology from Fraunhofer IAF will be shortly presented.

Chapter 3 deals with broadband amplifiers in general, wherein the focus is set on two widely applied concepts, namely feedback amplification and distributed amplification. After starting with a general review of amplifier classes, small-signal as well as large-signal matching schemes of the feedback power amplifier (FBPA) and traveling-wave amplifier/distributed power amplifer (TWA/DPA) are discussed from a theoretical point of view. The subsequent sections 3.3.2 and 3.4.3 present furthermore a detailed analysis of the noise characteristics of the FBPA and TWA, underpinned by the design of a DC-6 GHz FBPA and DC-15/20 GHz TWA in 0.25µm GaN technology.

Chapter 4 covers the topic of linearity in more detail. At the beginning, a short summary of important FoMs describing linearity is presented in order to introduce the most important indicators for linearity, before talking about on-chip linearization concepts in detail in the following subsections. In the main part of chapter 4, broadband on-chip linearization concepts are presented and analyzed for their applicability to FBPAs and TWAs. Based on the presented examinations of the broadband linearization concepts, the two most promising concepts were implemented in 0.25µm GaN technology for the first time. This is on the one hand the design of a truly-differential DC-6 GHz FBPA (TD-FBPA) and on the other hand the design of a linear low-noise TWA (L²NTWA) applying a distributed diode predistortion concept.

Chapter 5 succeeds the analytically derived noise dependencies in chapter 3 and transfers the gained knowledge to appropriate noise reduction schemes, applicable to FBPAs and TWAs. Since the latter topology reveals to exhibit a higher degree of low frequency noise optimization than the former one, several active cold load (ACL) concepts are reviewed and analytically analyzed. Afterwards, two distinct approaches for the reduction of low frequency gate-termination noise in TWAs are presented. One of these concepts, namely the blue-noise active termination (BNAT) concept, proved to be the most promising approach in terms of the targeted electrical performance and was thus implemented for verification purposes in the L²NTWA design from chapter 4 in GaN technology for the first time.

Chapter 6 addresses the stability of truly-differential PAs in GaN technology and analyses the trade-offs and pitfalls by means of the in chapter 4 presented DC-6GHz TD-FBPA design. Not only the differential-mode stability but rather the common-mode stability proves to be the critical design parameter for the design of GaN TD-PAs under a 50 Ω environment. Moreover, possible stabilization measures are analyzed and verified by the designed TD-FBPAs.

CHAPTER 2

GAN TECHNOLOGY AND MODELING

The following section serves to give some basic background about technological parameters and properties of GaN technology. In the first part the reason for using aluminium gallium nitride/gallium nitride (AlGaN/GaN) on semi-insulating silicon carbide (s.i. SiC) substrate is disclosed and the advantages over other substrates are pointed out. In the second part of this chapter a discussion of how to accurately model the electrical characteristics of HEMTs in this technology follows. Emphasis is put on semi-empirical models, which are half physical and half analytical and therefore are well suited for the efficient implementation in nowadays design software tools such as ADS or AWR. Before starting to concentrate on broadband amplifier concepts in chapter 3 it is thus meaningful to understand the prospects and problems of GaN technology and its models in order to better grasp and assess arising difficulties within a typical MMIC design process.

2.1 GaN Technology

2.1.1 AlGaN/GaN on SiC

Over the last 15 years, gallium nitride (GaN) on semi-insulating silicon carbide (s.i. SiC) evolved to a mature and reliable III-V semiconductor technology for high power microwave applications. Due to the non-availability of single crystalline GaN substrate in this time, first GaN films were deposited on sapphire substrates. After the first demonstration of single crystalline growth of gallium nitride on sapphire substrates by hybride vapor-phase epitaxy (HVPE) by H. P. Maruska and J.J. Tietjen in 1969 [22] at RCA Labratories, it should take another 24 years until the first high performance blue light-emitting diode (LED) was processed in 1993 [23]. At that very same year, the first single crystalline GaN metal semiconductor field-effect transistor (MESFET) was also grown on sapphire by metal-organic chemical vapor deposition (MOCVD). Another seven years later in 2000, after first successful reports of growing s.i. SiC with larger diameters [24], Cree Inc. turned out to be the first larger company seeing the high potential of GaN technology for high power applications in

microwave electronics. In 2005, they were also the first company, which introduced discrete AlGaN/GaN HEMTs on s.i. SiC for commercial applications. Cree Inc. together with a high number of other companies, such as Qorvo, ADI, UMS, Ommic etc., facilitated over the last 10 years that GaN on s.i. SiC became the number one III-V technology for high frequency and high power commercial applications, gradually replacing gallium arsenide (GaAs) technology.

One big drawback of GaN is the instability of the chemical bond between gallium and nitride, which impedes the growth of ingots with larger diameters than up to 3-inch today [25]. A different compound as substitute substrate with similar physical properties as GaN is hence required in order to grow a thin epitaxial GaN layer onto the substrate. The larger the lattice mismatch between the two materials, the higher the number of defects in the transistion region. The result are lattice defects and thus deep traps for the electrical charges within this region, which deteriorate the electrical performance of the HEMTs and thus need to be eliminated. Typical substrate materials for GaN are Si, Sapphire (Al_2O_3) and SiC [26]. Pure Si possesses a lattice constant (a_0) of 0.542 nm, as Fig. 2-1 reveals, but when growing GaN on the the 111-plane of Si, the lattice constant is around $a_0 = 0.384$ nm, giving only a 16.9 % mismatch. Despite of its large lattice mismatch, the use of Si wafers is desirable in terms of cost efficiency due to the commercial availability of large wafer diameters. Furthermore, the high quality and thus low number of defects opposed to other seminconductors makes Si a very promising candidate. One disadvantage is the difference in the coefficient of thermal expansion (CTE) compared to GaN, which can lead to enormous lattice strain and wafer bowing during the epitaxial growth. A slightly better matched material is sapphire (Al_2O_3) with only 14.8 % of mismatch, but which comes with the downside of a very low thermal conductivity of only $\kappa_{Sap} = 42$ W/(mK) opposed to Si with $\kappa_{Si} = 150$ W/(mK), which is even slightly better than the thermal conductivity of GaN bulk material with $\kappa_{GaN} = 130$ W/(mK). In order to cope with large power densities it is therefore necessary to thin the sapphire wafers down to a minimum thickness, which in turn brings up issues such as mismatched induced stress and wafer bowing during the processing. SiC in contrast combines both advantages, exhibiting superior characteristics in terms of lattice mismatch and thermal conductivity with $\Delta a_0 = 3.3$ % and $\kappa_{SiC} = 330$ W/(mK). The high thermal conductivity of SiC is owed to the hardness of the material, which comes close to diamond and thus makes the dicing of the chips very time-consuming and expensive for the manufacturer. This handling issue is one of the main cost factors and makes SiC one of the most expensive substrate material nowadays.

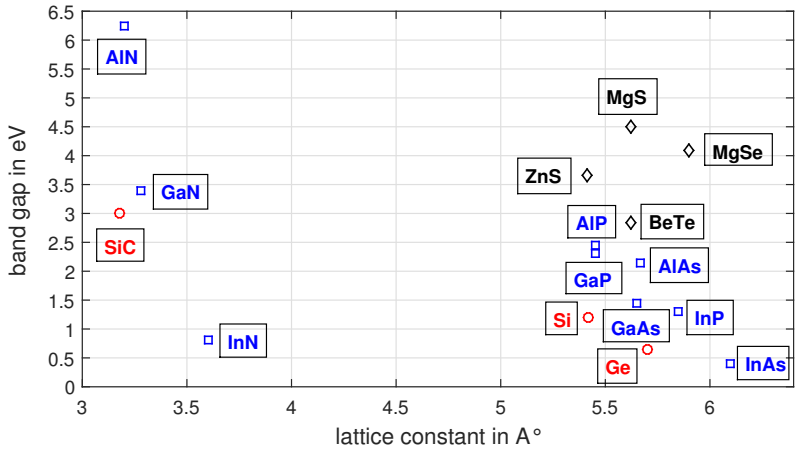


Fig. 2-1: Bandgap vs. lattice constant for different semiconductor materials ((□) III-V,(○) IV-IV,(◊) II-VI)

2.1.2 HEMT Technology

Fig. 2-2 sketches the layer stack of a typical AlGaN/GaN on s.i. SiC process. The channel of the HEMT is formed by the two-dimensional electron gas (2DEG), which results from the triangular shaped quantum-well formed by the $Al_xGa_{1-x}N$ and GaN heterostructure. Opposed to other III-V semiconductor technologies, no doping is necessary to generate the quantum-well, since the inherent piezoelectric and spontaneous polarization together with the bangap between the AlGaN donor layer and the GaN buffer layer causes already the generation of free electrons in the 2DEG [27]. Typical sheet densities of around 10^{13} cm^{-2} in the 2DEG allow for maximum channel currents of larger than 800 mA/mm [28]. The Hall mobility of the electrons in the channel is larger than 2000 cm^2/Vs, which is indeed much lower than e.g. in GaAs with 8500 cm^2/Vs, but combined with the high electrical critical fields of larger than 10 MV/cm, peak saturation velocities of $2 \cdot 10^7$ cm/s can be achieved. This enables to manufacture HEMTs with high transit frequencies according to the relationship [29]

$$f_T = \frac{v_{sat}}{2\pi \cdot l_G}, \tag{2.1}$$

where l_G is the effective gate length of the channel and v_{sat} the saturated electron velocity.

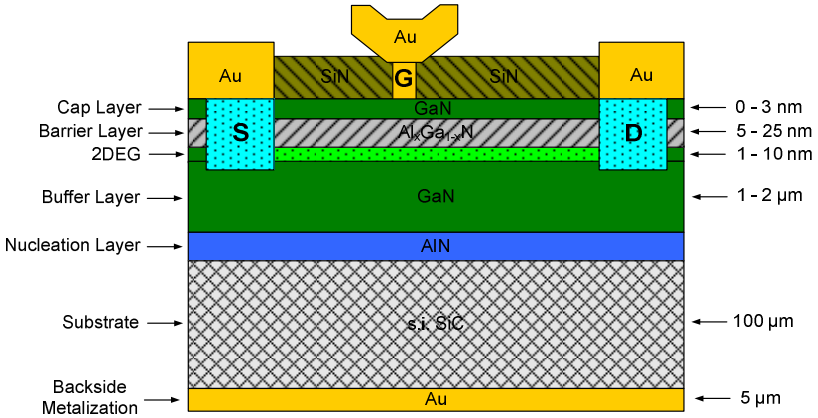


Fig. 2-2: Cross-section of a AlGaN/GaN HEMT on SiC

To reduce the number of defects and therewith traps close to the channel, it is crucial to grow high-quality, low defect-density layers on top of each other. Due to the inherent lattice mismatch between 4H-SiC and GaN, a strain relief layer or nucleation layer (AlN) needs to be deposited before growing the GaN buffer onto the SiC substrate. To further minimize the number of defects present in the channel, the GaN buffer layer needs to have a thickness of roughly 1-2 µm. The channel of the HEMT is formed by the heterostructure $Al_xGa_{1-x}N$/GaN. Thereby, the electrons for the 2DEG are mainly provided by the barrier layer, which hop into the conduction band due to the piezo-electric and spontaneous polarization at the interface [27]. The doped GaN cap layer of only a few nanometer thickness is introduced to improve the contact formation at the semiconductor passivation interface. Dependent on the amount of doping, dispersive effects evoked by traps, gate-leakage currents or the source access resistance can be controlled. A thin passivation layer (SiN) on top additionally helps to reduce parasitic gate-leakage effects and greatly reduces aging effects and thus enhances the reliability of the chips. Another delicate matter in terms of reliability is the exact material composition of the gate-metal at its semicon-

ductor interface. Effects such as gate-sinking into the semiconductor or micro-cracking can be minimized by selecting proper alloys, mainly composed of Pd, Ti, Ni and Au. At its gate terminal, the metal contact to the GaN cap-layer forms the Schottky diode, which exhibits a turn-on voltage of usually around 1 V for depletion mode (D-mode) devices. Exceeding this voltage leads to electron flooding of the channel via the gate, which can be thermally destructive under static condition for the HEMT.

2.1.3 IAF GaN25 Technology

For the realization of broadband power amplifier MMICs with high output power, high linearity and low-noise performance in the frequency range from DC – 20 GHz, the GaN25 technology from the Fraunhofer Institute of Applied Physics (IAF) is utilized within this work. As already suggested by the name, the active devices of the process are GaN HEMTs with gate lengths of L_G= 0.25µm. The AlGaN/GaN semiconductor is stacked on 4-inch semi-insulating 4H-SiC substrates with 100µm of thickness. Metal-organic chemical vapor deposition (MOCVD) is applied to grow the active AlGaN/GaN heterostructure epitaxy. High electron mobility transistors (HEMT) with gate lengths (L_G) of 250 nm and asymmetric gate-source/gate-drain spacings form the active device basis. These devices include field-plates to realize breakdown voltages in excess of 80 V with a peak transconductance (g_m) of 330 mS/mm at a class AB bias of I_{DS} = 100 mA/mm and V_{DS} = 28 V [30]. As the MSG/MAG-curves of a 8×125µm ISV-HEMT in Fig. 2-3 demonstrate, the peak transit frequency is located at around f_T = 30 GHz and the maximum frequency of oscillation at around f_{max} = 50 GHz.

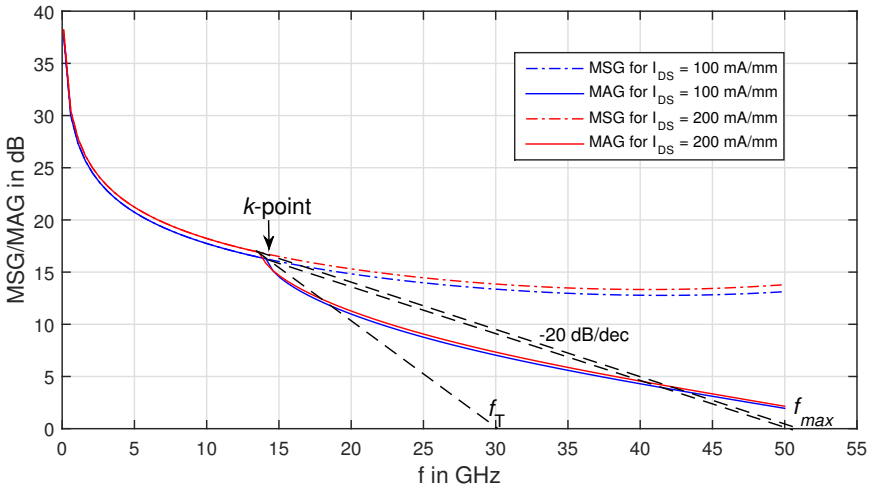


Fig. 2-3: MSG/MAG vs. f

The passive part of the GaN MMIC process comprises two kinds of interconnects, one thin gold microstrip line (MSL) defined by a lift-off process and one thick gold MSL formed by galvanic plating. The latter is also used to implement cross-overs in the form of low capacitance air-bridges. NiCr thin-film resistors (TFR) with 50 Ω/sqr sheet resistance, GaN epi-resistors with 490 Ω/sqr and metal-insulator-metal (MIM) capacitors with a capacitance density of 300 pF/mm² complete the passive MMIC process. In terms of losses, the s.i. SiC substrate with a $tan(\delta_{SiC})$ of roughly $2{\cdot}10^{-4}$ has slightly lower attenuation than GaAs substrates with a $tan(\delta_{GaAs})$ of around $4{\cdot}10^{-4}$…$6{\cdot}10^{-4}$. Moreover, based on the lower ε_r of 9.7 of GaN on s.i. SiC compared to the 12.9 of

GaAs substrates, the dominant metal losses of the former gold lines are also slightly lower than the latter ones for the same characteristic line impedance and max. current density of the MSLs. Therefore, the losses are even slightly lower for GaN on s.i. SiC with ~ 0.44 dB/cm than for GaAs MMICs with ~ 0.54 dB/cm, considering a typical 50 Ω MSL at 20 GHz on a substrate with a thickness of h = 100µm.

It can be summarized that based on the HEMT´s excellent high frequency device characteristic, which results from the high mobility and saturation velocity of the electrons in the two-dimensional electron gas (2DEG), this process is a promising candidate for the implementation of multi-decade PAs for the application in T&M instruments. The Typical DC- and RF-characteristics of the Fraunhofer IAF GaN25 process are once again summarized in Table 2-1 below.

Table 2-1: Typical characteristics of the IAF GaN25 process with an $Al_{0.25}GaN_{0.75}$/GaN heterostructure

L_G/nm	V_{th}/V	$I_{D,max}$/mA/mm	V_{BD}/V	$g_{m,max}$mS/mm	f_T/GHz	f_{max}/GHz
250	-3	800	> 80	330	30	50

2.2 Modeling of GaN HEMTs

The following sections shall give some basic background information on the topic of HEMT modeling. In general it can be differentiated between two different model types, one is the small-signal model, where the characteristics of the HEMT are described for small input drive signals and the other is the large-signal model, where the nonlinear properties of the HEMT under large-signal operation are incorporated. A further distinction can be made between models describing the signal or noise properties of the HEMT. Both in turn exist for the small-signal as well as large-signal case.

2.2.1 Small-Signal Modeling

A typical small-signal model of a HEMT containing extrinsic contact and intrinsic device elements is shown in Fig. 2-4. The outside lying extrinsics model the parasitic shell of the HEMT, which is only dependent on the device geometry, as e.g. on the number of fingers (NGF) and unity gate-width (UGW), but not on the bias-point. The intrinsic parameters in contrast are bias dependent and thus have to be determined for each operational bias-point separately.

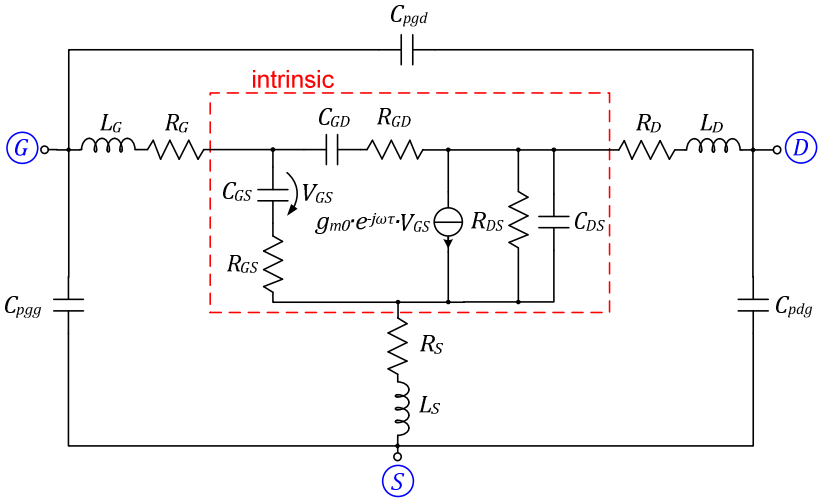


Fig. 2-4: HEMT equivalent small-signal model with extrinsic parasitic shell

The intrinsic resistive and reactive HEMT elements can be calculated by means of the Y-parameters of the intrinsic two-port. Equations (2.2) to (2.9) give the relations between Y-parameters and corresponding intrinsic small-signal parameters (red dashed box).

$$R_{GS} = Re\left\{\frac{1}{Y_{11}+Y_{12}}\right\} \tag{2.2}$$

$$C_{GS} = \left(\omega \cdot Im\left\{\frac{-1}{Y_{11}+Y_{12}}\right\}\right)^{-1} \tag{2.3}$$

$$R_{GD} = Re\left\{\frac{-1}{Y_{12}}\right\} \tag{2.4}$$

$$C_{GD} = \left(\omega \cdot Im\left\{\frac{1}{Y_{12}}\right\}\right)^{-1} \tag{2.5}$$

$$R_{DS} = (Re\{Y_{22} + Y_{12}\})^{-1} \tag{2.6}$$

$$C_{DS} = \frac{Im\{Y_{22} + Y_{12}\}}{\omega} \tag{2.7}$$

$$g_{m0} = |Y_{21} - Y_{12}| \cdot (1 + (\omega R_{GS} C_{GS})^2) \tag{2.8}$$

$$\tau = \frac{1}{\omega} \cdot arcsin\left(\frac{Im\{Y_{12} - Y_{21}\} - \omega R_{GS} C_{GS} \cdot Re\{Y_{21} - Y_{12}\}}{g_{m0}}\right) \tag{2.9}$$

In order to create a bias-dependent small-signal model, several S-parameters measurements at different bias points for the targeted device size are necessary to build a look-up table or fitting function of the intrinsic parameters. If the model should be also scalable, the whole procedure has to be conducted over the entire range of device sizes. Each set of measured S-parameters has to be de-embedded first to adjust the reference planes before starting with the small-signal extraction procedure. After removing the influences of the MSL and RF-pads at the input and output of the HEMT, it is crucial to exactly determine the extrinsic parasitics of the device in order to find the right values of the intrinsic elements. The frequency response of the intrinsic parameters, which should be ideally constant and show now frequency dependency, reveals if the extrinsic elements are properly modelled. There are in general two different approaches to identify the extrinsic element values. The first is a bottom-up approach, which is known as cold-FET method [31] and the second one is a generic top-down approach, further referred to as intrinsic parameter flattening.

Cold-Fet Method: The HEMT is operated at V_{DS} = 0 V with its gate control voltage under either pinch-off ($V_{\mathrm{GS}} < V_{th}$) or forward bias condition ($V_{\mathrm{GS}} \gtrsim 1$ V). One condition is usually enough to extract the parasitic elements, but the measurement of both conditions gives a more accurate estimate for the starting values in the optimization routine by establishing an upper and lower bound. First of all, the parasitic capacitances C_{px} are determined from low frequency S-parameter measurements and stripped-off after conversion into Y-parameters. After deembedding of the capacitance shell, the Z-parameters of the remaining device are computed from broadband frequency S-parameter measurements. The Z-parameters comprise now only the resistive and inductive parasitics. By multiplication of the Z-parameters with ω, the parasitic inductances $L_{\mathrm{G}}, L_{\mathrm{D}}$ and L_{S} can be read out of the slopes from the plots of $\omega \cdot Im\{Z_{11} - Z_{12}\}$, $\omega \cdot Im\{Z_{22} - Z_{12}\}$ and $\omega \cdot Im\{Z_{12}\}$ versus ω^2. Likewise by multiplication of the Z-parameters with ω^2 and plotting of $\omega^2 \cdot Re\{Z_{11}\}$, $\omega^2 \cdot Re\{Z_{22}\}$ and $\omega^2 \cdot Re\{Z_{12}\}$ versus ω^2 gives the parasitic resistances $(R_{\mathrm{G}} + R_{\mathrm{S}}), (R_{\mathrm{D}} + R_{\mathrm{S}})$ and R_{S}, which can be consecutively computed by linear regression. An erroneous extraction of the reactive elements in the foregoing steps will result in a nonlinear dependency of the parasitic resistances in the plots and can be used as a control mechanism for proper deembedding.

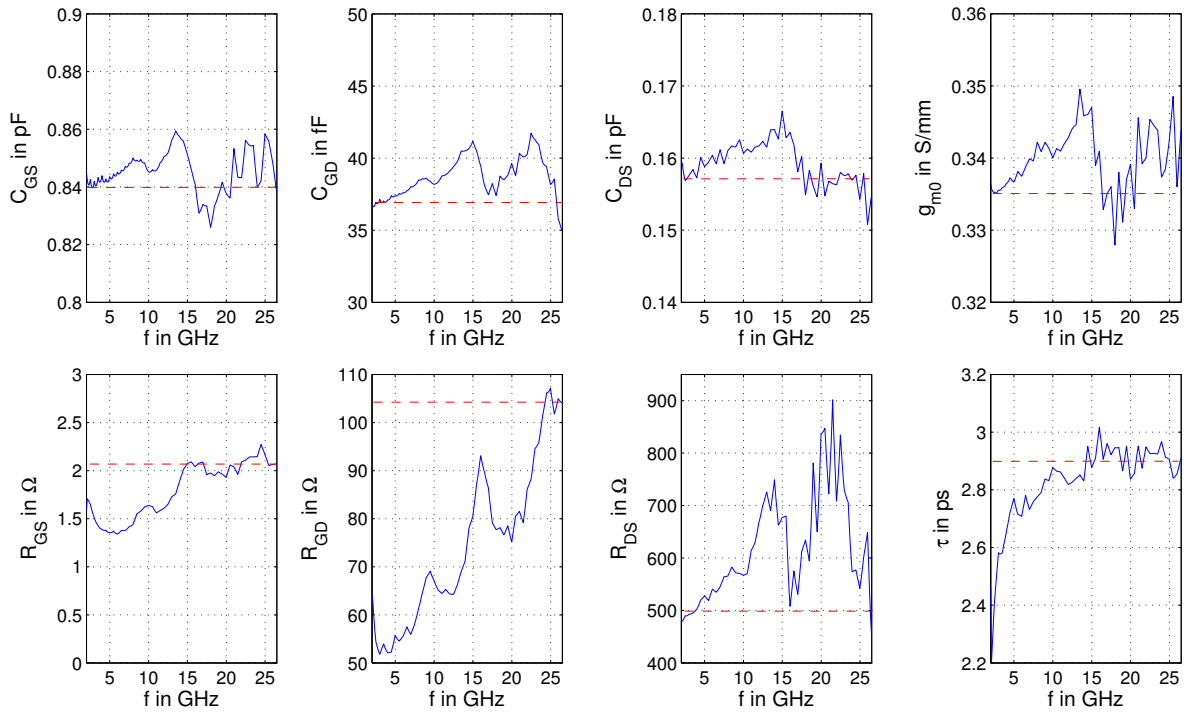


Fig. 2-5: Extracted intrinsic HEMT model parameters of an 8×50µm HEMT in the frequency range from 2 GHz to 26.5 GHz at V_{DS} = 28 V and I_{DS} = 200 mA/mm

Intrinsic Parameter Flattening: In the intrinsic parameter flattening approach in contrast, all extrinsic elements are iteratively optimized or tuned in the intrinsic parameter extraction procedure until a flat frequency response of the instrinisc elements is obtained. The advantage of this method lies in the reduced measurement complexity, because no cold-FET measurements are required anymore. Though, the disadvantage of this method is founded in the higher degree of freedom for the extrinsic parameters, especially for the resistive elements, since they feature no frequency dependence. Thus it should be noted that this method does not necessarily give the most realistic/physical model, since some parameters, e.g. R_G and R_{GS}, can be traded off for each other. This basic method can be above all also applied to the cold-FET method after computation of the starting values.

Fig. 2-5 shows the extracted small-signal parameters over frequency for a 8×50µm GaN HEMT (W_G = 0.4 mm) at V_{DS} = 28 V and I_{DS} = 200 mA/mm, after de-embedding of the MSL-feeding structures and RF-pads. Clearly visible is the remaining frequency dependence of the intrinsic device parameters, which is caused by the non-perfect deembedding of the measured S-parameters. Based on measurement inaccuracies and on the applied topology of the model, it is in general not possible to obtain a real constant value over frequency. Especially the resistive elements R_{GS}, R_{GD} and R_{DS} show a strong frequency dependence, making it often difficult to uniquely identify them. Since the extraction procedure applied is based on Y-parameters (see (2.2)-(2.9)), it is meaningful to determine the resistive parallel elements (R_{DS}) at low frequencies and the resistive series elements (R_{GS}, R_{GD}) at high frequencies, because they are masked at low frequencies by their series capacitances C_{GS} and C_{GD}. The capacitances C_{GS}, C_{GD} and C_{DS} as well as the transconductance g_{m0} are extracted at low frequencies in order to minimize the impact of the extrinsic reactive elements on the correct capacitance values. The influence of the transit time τ of the charge carriers in the channel increases with frequency, which leads to an increasing phase shift between gate- and drain in the HEMT. Therefore, it is meaningful to extract τ at higher

frequencies. The red dashed lines in Fig. 2-5 mark the extracted parameter values (Table 2-2) under the just mentioned considerations, which are taken to create the small-signal model.

Table 2-2: Final intrinsic HEMT parameters of a 8×50µm GaN HEMT at I_{DS} = 200 mA/mm and V_{DS} = 28 V

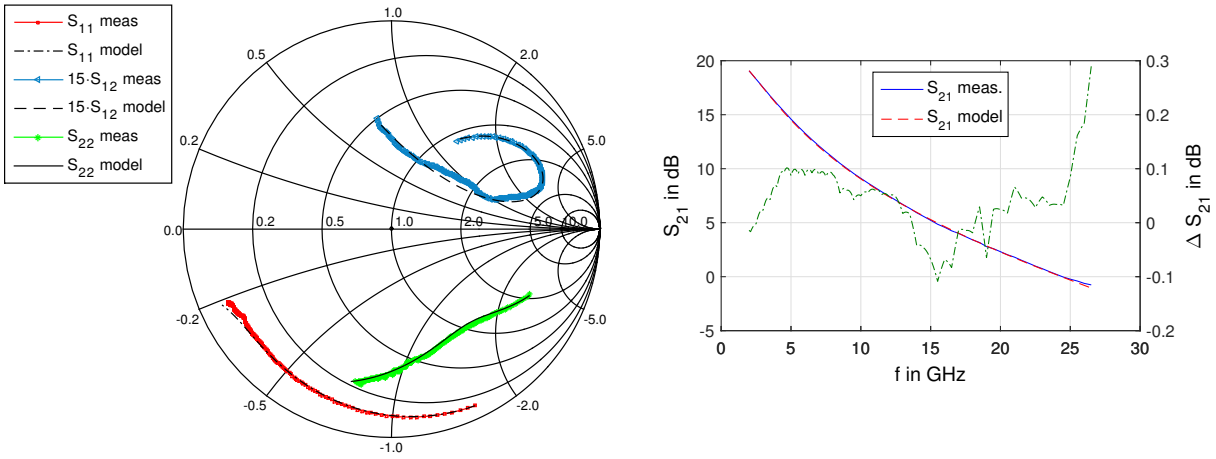
R_{GS} / Ω	C_{GS} / pF	R_{GD} / Ω	C_{GD} / fF	R_{DS} / Ω	C_{DS} / fF	g_{m0} / mS	τ / ps
2.1	0.84	105	37	500	157	134	3

The corresponding extrinsic elements of the 8×50µm HEMT have been determined simply by intrinsic parameter flattening (method 2), because for the creation of a small-signal noise model in chapter 2.2.3 it is sufficient to generate a simple model rather than a realistic/physical one. For the curves depicted in Fig. 2-5 the following extrinsic values in Table 2-3 have been found. R_G has been deliberately set to zero for better noise modeling later on and the existing physical value of the gate-contact resistace has been shifted into R_{GS}, which is a valid modeling assumption based on the much smaller C_{GD} compared to C_{GS} in GaN.

Table 2-3: Extrinsic HEMT parameters of a 8×50µm GaN HEMT at I_{DS} = 200 mA/mm and V_{DS} = 28 V

R_G / Ω	R_D / Ω	R_S / Ω	L_G / pH	L_D /pH	L_S / pH
0	1.2	0.8	10	15	15

The results of the model are compared to the de-embedded measurements in Fig. 2-6 in the frequency range from 2 GHz to 26.5 GHz. A good match between all four S-parameters over the full measurement bandwidth is achieved, proving that the model reflects the HEMT characteristics in reasonable approximation.



(a) (b)

Fig. 2-6: Measured and modeled (a) S_{11}, 15· S_{12} and S_{21} and (b) S_{21} vs. frequency of a de-embedded 8×50µm HEMT

2.2.2 Large-Signal Modeling

Accurate electro-thermal large-signal HEMT models form the base for efficient and cost optimized PA designs by means of CAD tools. In order to minimize the time-to-market of PA products, which plays a critical role especially in the communications sector nowadays, the large-signal model needs to predict power and linearity precisely to avoid lengthy and therewith costly try-and-error hardware iteration cycles. To shorten the design time, large-signal models need to feature short simulation times and good convergence properties on simulation level, besides the general prerequisite of high accuracy and scalability. Since the focus of this work is primarily set on linearization and noise reduction concepts, only a short side note on the huge realm of large-signal modeling will be given in this section. Among the large variety of existing large-signal models, three general model groups can be identified, as depicted in Fig. 2-7.

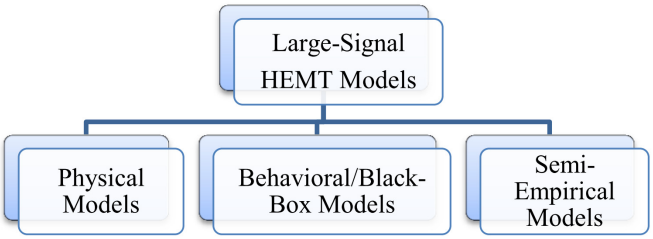
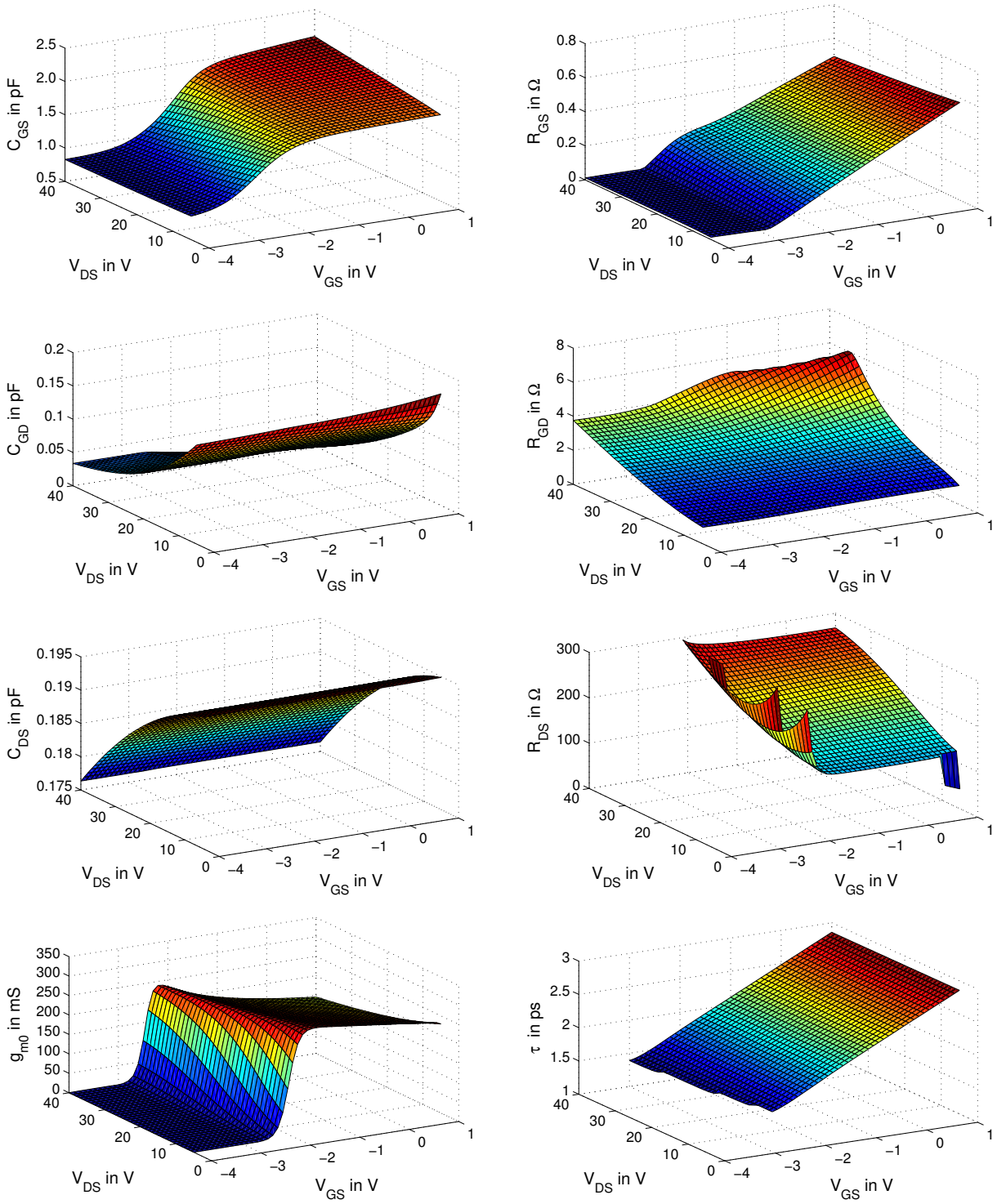


Fig. 2-7: Large-signal modeling classes

The first large-signal model group contains all different kind of physical based models, in which the large-signal transfer characteristic is mainly described by drift-diffusion equations or hydrodynamic modeling approaches of the electrons in the 2DEG, as e.g. published in [32, 33, 34]. The second group contains all kind of behavioral models, where the HEMT is considered as a simple two- or three-port black-box. Only the input-output characteristic is described by either purely analytical mathematical functions (e.g. Hammerstein model [35], Volterra-series [36, 37, 38, 39, 40, 41] or artificial neural network (ANN) approaches [42, 43, 44, 45]) or by measurement based look-up tables. In the third group, all kind of semi-empirical models are embodied.

This is the most widespread and common approach applied in the III-V semiconductor community. Typical semi-empirical models for GaN are the Angelov-Chalmers model [46, 47, 48, 49] and the EEHEMT model [50], followed by several further additional modifications. The state-space voltage-lag model in contrast is not as popular as the two mentioned ones, but it is capable of describing low-frequency dispersion and thermal memory effects and their resulting effect on the nonlinearity of the HEMT precisely by means of internal state variables, such as the intrinsic channel current and the gate-source and gate-drain space charges. The corresponding state quantities are the external control voltages V_{GS} and V_{DS}. All of the internal parameters of this model are extracted from DC and pulsed small-signal S-parameter measurements. Fig. 2-8 depicts the large-signal dependence of the intrinsic HEMT parameters for an 8×125µm GaN device, derived from the two-dimensional state-space voltage-lag model. All PAs designed within this work are based on this model, which is impelemented in the PDK of the GaN25 process from the Fraunhofer IAF. A more detailed description about the model can be found in [51]. One big advantage of all semi-empirical models is the connection between partly physical description of the HEMT and purely mathematical fitting functions. Based on this mixture, the benefit of these models is founded in their scalability and accuracy over relatively wide parameter spaces. Nevertheless, the accuracy of all presented models depends strongly on the correctness and accuracy of the underlying measurements, which might often be a major obstacle on the way to generate accurate large-signal models.



(a) (b)

Fig. 2-8: Intrinsic HEMT parameters dependent on V_{GS} and V_{DS} according to the IAF nonlinear state-space voltage-lag model for a 8×125µm GaN HEMT

2.2.3 Noise Modeling

Various noise models have been developed in the past decades to describe the noise in FETs, mainly in MESFETs and HEMTs. The following section shall provide a short historical overview over the endeavors undertaken in noise modeling. All started in the early 1960s with A. van der Ziel, who developed a noise model for JFETs in 1963 [52] and 1964 [53]. With the advent of new upcoming transistor technologies with shorter gate-lengths van der Ziel´s noise model has been adapted by W. Baechthold *et al.*, who were the first taking short channel effects, such as e.g. hot carrier effects, into account and modified van der Ziel´s model correspondingly in [54] for GaAs MESFETs in 1971. Four years later R. Pucel *et al.* additionally included the noise contribution from the extrinisic transistor parameters R_G and R_S of a MESFET in their model [55] in order to obtain higher accuracy and better noise prediction. In 1979, H. Fukui further simplified Pucel´s semi-empirical noise model by introducing a numerical fitting constant K_f, which takes the bias independent noise of R_G and R_S into account [56]. This is equivalent to the limiting case of full correlation between input and output noise ($C = 1$) and/or the negligence of induced-gate noise ($R = 0$) of Pucel´s noise model. Pospiezalski was the first who followed the approach of modeling noise by the equivalent temperatures T_G and T_D at the gate and drain side of the transistor rather than by equivalent input and output noise currents or voltages, as all other models before. This led to a simpler mathematical description, where only two noise temperatures are necessary. Furthermore, a correlation coefficient between the gate- and drain-side noise is not present within this noise model anymore, which reduces the complexity of the noise measurement [57]. Today, among all these mentioned noise models the Pucel and Pospieszalski model are the most prominent for small-signal noise modeling, because of their effective way of describing small-signal noise within a MESFET or HEMT analytically. Nevertheless, there is limited accuracy of the models, which will be pointed out by a direct comparison of these two models. The next few pages are thus dedicated to give some more insight into the basics and differences of these two models. In a final step, noise measurements of an 8×50µm GaN HEMT are used to extract the noise temperatures T_G and T_D of Pospieszalski´s model as well as the fitting constants PRC of Pucel´s model. The result serves to establish a small-signal noise model based on Pucel, which is applicable to the IAF large-signal model and thus enables to make a noise prediction for the DC-15 GHz TWA design presented later in chapter 3.4.5.

Van der Ziel´s / Pucel`s Noise Model

As the equivalent noisy small-signal circuit in Fig. 2-9 below sketches, Pucel modelled the noise of a FET by two correlated noise current sources at the input and output rather than by equivalent noise temperatures as Pospieszalski. Under the simplified assumption that the feedback is negligible ($C_\mathrm{GD} = 0$ F), the equivalent input- and output noise currents and their correlation can be described by the following equations.

$$\langle {i_{n,\mathrm{g}}}^2 \rangle = 4k_B T_0 \frac{(\omega C_\mathrm{GS})^2}{g_m} R \tag{2.10}$$

$$\langle {i_{n,d}}^2 \rangle = 4k_B T_0 g_m P \tag{2.11}$$

$$\langle i_{n,g}^* \cdot i_{n,d} \rangle = \underline{c} \cdot \sqrt{\langle {i_{n,g}}^2 \rangle \langle {i_{n,d}}^2 \rangle} \tag{2.12}$$

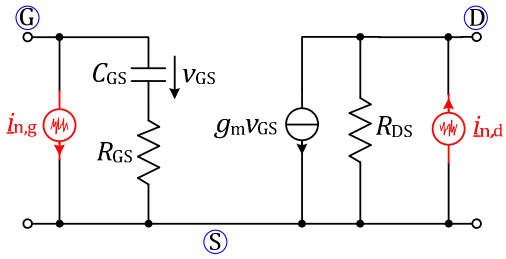


Fig. 2-9: Schematic of Pucel´s small-signal noise model

R and P in (2.10)-(2.12) are bias dependent fitting factors and $\underline{c}$ describes the complex correlation between the induced gate- and drain-noise. Usually the correlation coefficient $\underline{c}$ is almost purely imaginary for HEMTs, when τ in the model is negligibly small, with a magnitude in the range of $j \cdot 0.7 \ldots 0.9$ [58, 59]. Care has to be taken about the sign of $\underline{c}$, since this depends on the direction and complex conjugate of the noise current sources in Fig. 2-9 to each other. The following Table 2-4 gives an overview over the eight possible combinations and their corresponding correlation coefficients $\underline{c}$, which has been presented by E. Säckinger in [60]. Table 2-4 is a very useful look-up table for the calculation of Pucel´s noise models, because it reduces confusion between the sign of the correlation coefficient $\underline{c}$.

Table 2-4: Coherency between direction of noise current generators and noise correlation coefficient

Direction of $\underline{i}_{n,G}$	Direction of $\underline{i}_{n,D}$	Correlation Coefficient $\underline{c}$	$sgn(Im\{\underline{c}\})$
↓	↓*	$-\underline{c}^*$	+
↑	↑*		
↓*	↑	$\underline{c}$	
↑*	↓		
↓*	↓	$-\underline{c}$	-
↑*	↑		
↓	↑*	$\underline{c}^*$	
↑	↓*		

Recently in [61] Rudolph *et al.* extended Pucel´s small-signal noise model to the large-signal domain. The advantage of Pucel´s large-signal noise model lies in the compatibility with all different kinds of semi-empirical large-signal models, where in general C_{GS} and I_{DS} are modelled by bias dependent fitting functions (see e.g. Chalmers-Angelov model [62, 47, 49]). So, making (2.10)-(2.11) bias dependent is problematic in terms of the transconductance g_m, which itself is already the 1st derivative of I_{DS} vs. V_{GS} and thus more prone to variations. This problem can be skirted by reformulating (2.10)-(2.11) to

$$\langle {i_{n,G}}^2 \rangle = 4q \frac{(\omega C_{GS})^2}{I_{DS}} R' \tag{2.13}$$

$$\langle {i_{n,D}}^2 \rangle = 2q I_{DS} P' \tag{2.14}$$

As can be seen from equations (2.13) and (2.14), the equivalent gate- and drain noise current spectral densities ($NCSD$) are now dependent on C_{GS} and I_{DS} only, which are already given from the large-signal model. The parameters R and P in contrast change to the fitting functions

$$R' = NP_1 - NP_2 \cdot tanh\left(\frac{I_{\mathrm{DS}}}{\alpha}\right) \cdot \left(1 + \frac{I_{\mathrm{DS}}}{\beta}\right) \tag{2.15}$$

$$P' = \frac{1}{\gamma} \cdot I_{\mathrm{DS}} + \frac{V_{\mathrm{DS}}}{\delta} {I_{\mathrm{DS}}}^3 \tag{2.16}$$

with α, β, γ, δ and NP_1, NP_2 being fitting constants. The correlation coefficient $\underline{c}$ for the large-signal noise model can be still assumed to be purely imaginary, constant at around 0.8 and frequency independent. It has to be noticed that expressing the large-signal noise by an equivalent shot-noise model, similar to the large-signal Pospieszalski noise model in (2.21), does not change the physical cause for the noise but is only a more convenient mathematical way of describing the bias dependence of white thermal noise.

Pospieszalski`s Noise Model

One of the most simple and straightforward small-signal noise models was invented by Pospiezalski [63] in 1989. Therein, Pospieszalski described the noise of a HEMT not directly by its input and output referred noise current sources as Pucel, but rather by its noise power spectral densities (NSD) of the intrinsic resistances R_{GS} and R_{DS}. Fig. 2-10 depicts the Pospieszalski model with its two uncorrelated noise temperatures.

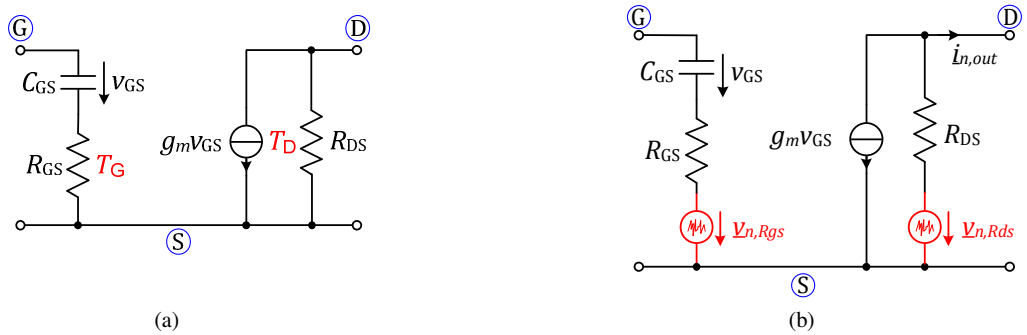


Fig. 2-10: Schematic of Pospieszalski´s small-signal noise model (a) with equivalent noise temperatures and (b) equivalent noise voltage sources

Expressing the noise-voltage spectral densities ($NVSD$) in terms of their equivalent noise temperatures T_{G} and T_{D} gives

$$\langle {v_{n,Rgs}}^2 \rangle = 4 k_B T_{\mathrm{G}} R_{\mathrm{GS}} \tag{2.17}$$

$$\langle {v_{n,Rds}}^2 \rangle = 4 k_B T_{\mathrm{D}} R_{\mathrm{DS}}. \tag{2.18}$$

Pospiezalski´s noise model was later extended to the large-signal domain by L. Klapproth *et al.* in 1997 [64]. Therein, L. Klapproth *et al.* replaced the constant temperatures T_G and T_D by the bias dependent expressions

$$T_\mathrm{G}(V_\mathrm{GS}, V_\mathrm{DS}) = \kappa \cdot (V_\mathrm{DS} - \lambda)^2 + \varphi \tag{2.19}$$

$$T_\mathrm{D}(V_\mathrm{GS}, V_\mathrm{DS}) = (\gamma + \delta V_\mathrm{DS}) \cdot tanh(\alpha \cdot (V_\mathrm{DS} - \beta)^2) + \varepsilon, \tag{2.20}$$

with α ... φ being fitting parameters dependent on V_GS.

Recently in 2014 another approach was taken by M. Rudolph *et al.* in [65]. In their approach the necessity of an accurate and exact large-signal g_DS-model, which is difficult to establish based on the large uncertainty of R_DS or g_DS in the model extraction procedure, was mitigated. Instead of finding a large-signal description for the equivalent noise temperature $T_\mathrm{D}(V_\mathrm{GS}, V_\mathrm{DS})$ for R_DS, as done by L. Klapproth *et al.*, M. Rudolph *et al.* expressed the channel noise via the existing I_DS bias dependence, using the following shot-noise expression in (2.21) instead of the thermal noise representation for white noise.

$$\langle {i_{n,\mathrm{D}}}^2 \rangle = 2qI_\mathrm{DS}{X_\mathrm{D}}', \tag{2.21}$$

The variable q in (2.21) stands for the electron charge and ${X_\mathrm{D}}'$ for the bias dependent fitting function

$${X_\mathrm{D}}' = NP_1 - NP_2 \cdot \left(tanh(NP_3 \cdot I_\mathrm{DS}) + tanh(NP_4 \cdot I_\mathrm{DS})\right) \tag{2.22}$$

with the fitting constants NP_1 ... NP_4.

Integration of L. Klapproth´s or M. Rudolph´s large-signal noise model into the existing empirical large-signal model from the IAF is due to the non-existence of any lumped R_GS or R_DS in the state-space model not possible. Since this model is purely based on mathematical descriptions of the intrinsic HEMT, no direct access to R_GS and R_DS is given within the equations. Hence, only Pucel´s noise model using equivalent input and output noise current sources can be taken for the IAF large-signal model.

Comparison of Pospiezalski´s and Pucel´s Noise Model

In order to obtain comparable expressions for Pospieszalski and Pucel the former model can be converted to the latter one by calculating the equivalent input and output short-circuited noise currents from Fig. 2-11. It is worth noting that any parallel feedback in Fig. 2-11 can be taken into account for the computation of the equivalent input and output noise currents $\underline{i}_{n,\mathrm{G}}$ and $\underline{i}_{n,\mathrm{D}}$ in (2.23)-(2.25) without introducing errors. In doing so, the following expressions (2.23) - (2.25) can be determined under the prerequisite of the Pospieszalski model assumption that $v_{n,Rgs}$ and $v_{n,Rds}$ are uncorrelated.

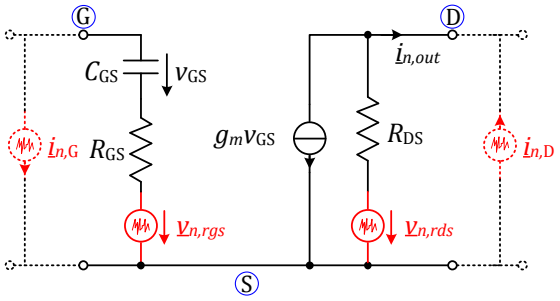


Fig. 2-11: Schematic of Pospieszalski´s small-signal noise model with corresponding noise voltage sources for the calculation of the equivalent input and output short circuit noise currents of Pucel´s equivalent noise model

$$\langle \underline{i}_{n,\mathrm{G}}{}^2 \rangle = 4k_B T_\mathrm{G} R_\mathrm{GS} \left| \frac{j\omega C_\mathrm{GS}}{1 + j\omega C_\mathrm{GS} R_\mathrm{GS}} \right|^2 \tag{2.23}$$

$$\langle \underline{i}_{n,\mathrm{D}}{}^2 \rangle = 4k_B \left(\frac{T_\mathrm{D}}{R_\mathrm{DS}} + T_\mathrm{G} R_\mathrm{GS} \left| \frac{g_m}{1 + j\omega C_\mathrm{GS} R_\mathrm{GS}} \right|^2 \right) \tag{2.24}$$

$$\langle \underline{i}^*_{n,\mathrm{G}} \underline{i}_{n,\mathrm{D}} \rangle = 4k_B T_\mathrm{G} \frac{g_m \cdot j\omega C_\mathrm{GS} R_\mathrm{GS}}{1 + (\omega C_\mathrm{GS} R_\mathrm{GS})^2} \tag{2.25}$$

It becomes obvious from (2.25) that a purely imaginary correlation between the input and output noise current for the Pospiezalski model exists, since the noise voltage $v_{n,Rgs}$ has to be transferred via C_GS to the input and output. In a further step R, P and C can also be calculated for the Pospieszalski model by setting (2.10)-(2.12) equal to (2.23)-(2.25). This leads to the equations (2.26) to (2.28).

$$R_{Pszk} = \frac{T_\mathrm{G}}{T_0} \frac{g_m R_\mathrm{GS}}{1 + (\omega C_\mathrm{GS} R_\mathrm{GS})^2} \tag{2.26}$$

$$P_{Pszk} = R_{Pszk} + \frac{T_\mathrm{D}}{T_0} \frac{1}{g_m R_\mathrm{DS}} \tag{2.27}$$

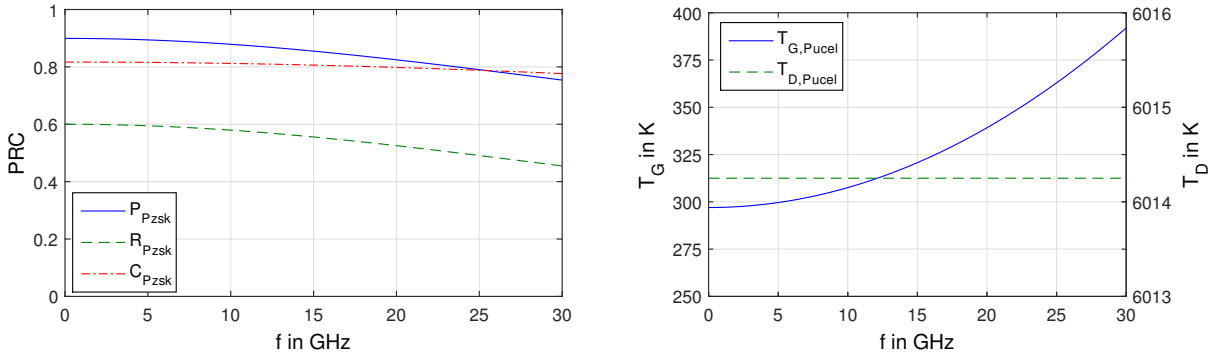
$$\underline{c}_{Pszk} = \frac{\langle \underline{i}^*_{n,\mathrm{G}} \underline{i}_{n,\mathrm{D}} \rangle}{\sqrt{\langle \underline{i}_{n,\mathrm{G}}{}^2 \rangle \langle \underline{i}_{n,\mathrm{D}}{}^2 \rangle}} = j \cdot \frac{1}{\sqrt{1 + \frac{T_\mathrm{D}}{T_\mathrm{G}} \cdot \frac{1 + (\omega R_\mathrm{GS} C_\mathrm{GS})^2}{g_m{}^2 R_\mathrm{GS} R_\mathrm{DS}}}} = j \cdot \sqrt{\frac{R_{Pszk}}{P_{Pszk}}} \tag{2.28}$$

Likewise for the equivalent noise temperatures of the Pucel model, $T_{\mathrm{G},Pucel}$ and $T_{\mathrm{D},Pucel}$ result from (2.26) and (2.27) in

$$T_{\mathrm{G},Pucel} = T_0 R \cdot \frac{1 + (\omega C_\mathrm{GS} R_\mathrm{GS})^2}{g_m R_\mathrm{GS}} \tag{2.29}$$

$$T_{\mathrm{D},Pucel} = T_0 (P - R) g_m R_\mathrm{DS} \tag{2.30}$$

The parameter T_0 in (2.26), (2.27) and (2.29), (2.30) is equal to the ambient temperature in Kelvin at 297 K. From the equations (2.26) to (2.28) it can be derived that the PRC-parameters of the Pospieszalski model have to be frequency dependent in order to match the constant temperatures T_G and T_D. Vice versa, the gate-side temperature $T_{G,Pucel}$ of Pucel´s model is also frequency dependent in order to match the PRC-parameters. The drain-side temperature $T_{D,Pucel}$ in contrast is constant. This can be verified by the plots in Fig. 2-12, where in (a) the equivalent PRC-parameters of the Pospieszalski model for T_G = 297 K and $T_D \cong$ 6014 K are depicted and in (b) the equivalent noise temperatures of the Pucel model for P = 0.9, R = 0.6 and $Im\{\underline{c}_{Pszk}\}$ = 0.816 are plotted. The same results have been also obtained by Rudolph *et al.* in [58]. All of the derived equivalent parameters in the paper are frequency independent, which is a good approximation for $(\omega C_{GS} R_{GS})^2 \ll 1$. For frequencies approaching f_T the voltage-divider term $(1 + (\omega C_{GS} R_{GS})^2)$ in (2.26) and (2.29) has to be considered in order to obtain exact results, as can be seen in Fig. 2-12.



(a) (b)

Fig. 2-12: Equivalent noise parameters of (a) Pospieszalski´s (T_G = 297 K, $T_D \cong$ 6014 K) and (b) Pucel´s (P = 0.9, R = 0.6, $Im\{\underline{c}\}$ = 0.816) small-signal noise model from (2.26)-(2.30) for a 8×125µm low-noise device

Up to now it has been silently presumed in the recalculation that g_m is only real and exhibits accordingly no delay (τ = 0 s). Expression (2.28) is only valid under this condition and the correlation coefficient $\underline{c}_{Pszk}$ is purely imaginary. As soon as any delay is taken into account ($\tau \neq$ 0 s), the recalculated correlation coefficient $\underline{c}_{Pszk}$ from the Pospieszalski model possesses an additional real-part, as it is shown in (2.31) below.

$$\underline{c}_{Pszk} = \frac{\langle \underline{i}_{n,G}^{*} \underline{i}_{n,D} \rangle}{\sqrt{\langle \underline{i}_{n,G}{}^2 \rangle \langle \underline{i}_{n,D}{}^2 \rangle}} = j \cdot e^{-j\omega\tau} \cdot \sqrt{\frac{R_{Pszk}}{P_{Pszk}}}$$
$$= \sqrt{\frac{R_{Pszk}}{P_{Pszk}}} \cdot (sin(\omega\tau) + j \cdot cos(\omega\tau)) \tag{2.31}$$

By simply regarding the corrersponding model parameters no additional insight into the different modeling capabilities of the two noise models is gained. It is more meaningful to take a closer look onto the general four noise parameters F_{min}, $\measuredangle(\Gamma_{s,opt})$, $|\Gamma_{s,opt}|$ and R_n. The noise factor F of a transistor is only dependent on the minimum obtainable noise factor F_{min} and the input matching to the source impedance and can be in general expressed by [66]

$$F = F_{min} + \frac{4R_n}{Z_0}\frac{\left|\Gamma_{s,opt} - \Gamma_s\right|^2}{\left|1 + \Gamma_{s,opt}\right|^2(1 - |\Gamma_s|^2)}. \tag{2.32}$$

$\Gamma_{s,opt}$ in (2.32) stands for the optimum source reflection coefficient to be synthesized in order to retain NF_{min}. Γ_s is the source reflection coefficent, Z_0 the characteristic impedance and R_n gives the noise sensistivity of the transistor to input impedance mismatches. A small R_n is of advantage, because the transistor is then less susceptible to any input mismatch, which facilitates the design of low NFs over broad bandwidths. The minimum noise factor F_{min} is itself only dependent on R_n and the sum of the optimum source conductance ($G_{S,opt}$) and the equivalent input noise correlation transconductance (G_c), as (2.33) shows.

$$F_{min} = 1 + 2R_n\left(G_{s,opt} + G_c\right). \tag{2.33}$$

The computation of F_{min} for Pospieszalki´s and Pucel´s noise model according to [55] on p. 252 delivers equations (2.34) to (2.35) below.

Pucel:
$$F_{min} = 1 + \cdots$$
$$\ldots + 2\frac{\omega C_{\mathrm{GS}}}{g_m}\sqrt{PR(1 - C^2)(1 + (\omega C_{\mathrm{GS}})^2) + \left(\omega C_{\mathrm{GS}} R_{\mathrm{GS}} P\left(1 - C\sqrt{\frac{R}{P}}\right)\right)^2} \tag{2.34}$$
$$\ldots + 2g_m R_{\mathrm{GS}} P\left(1 - C\sqrt{\frac{R}{P}}\right)\left(\frac{\omega C_{\mathrm{GS}}}{g_m}\right)^2$$

Pospieszalski:
$$F_{min} = 1 + 2\frac{T_{\mathrm{D}}}{T_0}\cdot\frac{\omega C_{\mathrm{GS}}}{g_m}\frac{R_{\mathrm{GS}}}{R_{\mathrm{DS}}}\left[\sqrt{\frac{R_{\mathrm{DS}}}{R_{\mathrm{GS}}}\frac{T_{\mathrm{G}}}{T_{\mathrm{D}}} + \left(\frac{\omega C_{\mathrm{GS}}}{g_m}\right)^2} + \frac{\omega C_{\mathrm{GS}}}{g_m}\right] \tag{2.35}$$

The comparison of (2.34) with (2.35) shows that F_{min} and accordingly all other three noise parameters (not shown here), have one degree of freedom more in Pucel´s model than in Pospieszalski´s. On the one hand this makes Pucel´s model more versatile and allows for a higher modeling accuracy. On the other hand, a higher measurement effort has to be taken in order to determine three instead of only two noise parameters. M. Rudolph *et al.* have proven in [57] that for the extraction of Pospieszalski´s model parameter a single 50 Ω measurement is sufficient under the assumption that T_{G} is at room temperature, whereas for Pucel´s model parameters at least four source-pull measurements are required. As long as the measured noise characteristic of any technology matches well to the Pospieszalski model, there is no need for taking a more complex model. One important reason to use Pucel´s model might be the underlying transistor model and its accessability of R_{GS} and R_{DS} in the model, as already mentioned for the large-signal noise models in the previous sections. This makes the integration of Pospieszalski´s noise model into some large-signal models impossible.

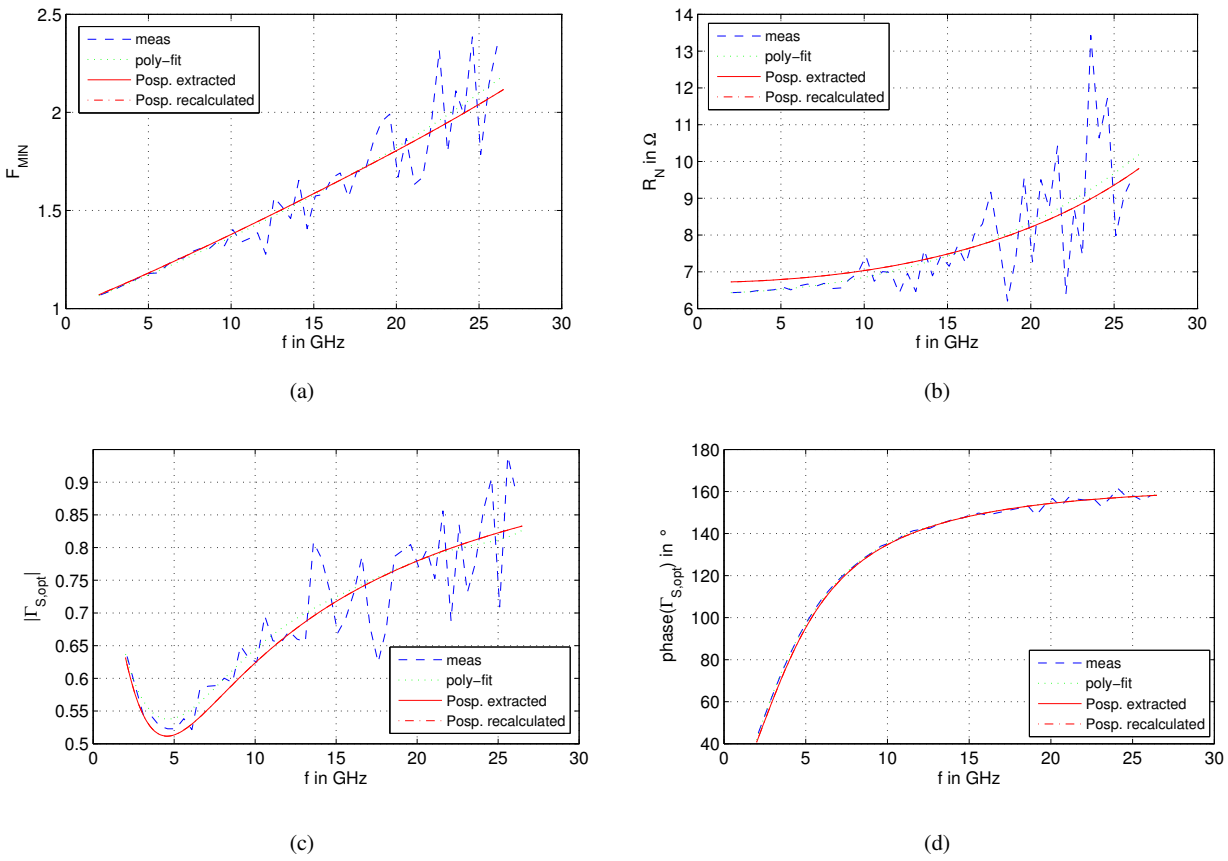


Fig. 2-13: Measured and modelled noise parameters of a 8×50µm HEMT at V_{DS} = 28 V and I_{DS} = 200 mA/mm.

Unfortunately, there is no such small-signal or even large-signal noise model based on Pospieszalski´s or Pucel´s approach available for the utilized power HEMTs with larger gate-drain spacing in the GaN25 technology. In order to obtain a good estimate for the DC-15GHz TWA´s noise performance, which will be presented later in chapter 3.4.5, the T_G, T_D noise temperatures and PRC-parameters have been extracted for a 8×50µm power HEMT at several operational bias points of V_{DS} = 28 V and I_{DS} = 100…200 mA/mm by using the extraction method presented in [57]. The extraction procedure is based on correlation matrices, first published by H. Hillbrand and P. Russer in [67]. The advantage of making use of this method is the freedom in choosing the desired equivalent small-signal HEMT model, including extrinsic parasitic elements. Furthermore, it is possible to take noise arising from the extrinsic elements in the noise analysis into account. For the intrinsic noise calculation the noise correlation matrix in Y-parameter representation is the most suited one, since the feedback capacitance C_{GD} has no influence on the equivalent input and output short-circuit noise currents and can be hence either omitted or taken into account without the need to recalculate the intrinsic noise of the HEMT again. Fig. 2-13 graphs the four noise parameters F_{min}, $\measuredangle(\Gamma_{s,opt})$, $|\Gamma_{s,opt}|$ and R_n of the noise extraction method from M. Rudolph *et al.* in [57] for a 8×50µm GaN HEMT at V_{DS} = 28 V and I_{DS} = 200 mA/mm.

The equivalent noise temperatures T_G and T_D of the Pospieszalski model result in T_G = 327 K at the gate-side and in T_D = 10972 K for the drain-side. Equivalently, for the PRC-model the parameter result in P = 0.83, R = 0.24 and $Im\{\underline{c}\}$ = 0.54. If the network to be analyzed is too complex for a theoretical derivation, it is also possible to chose a bottom up approach by determination of the correlation matrix C_A from noise measurements

of the four noise parameters by the coherency between C_A and F_{min}, $\measuredangle(\Gamma_{s,opt})$, $|\Gamma_{s,opt}|$ and R_n, as given in equations (B.1.2)-(B.1.5) in the Appendix B.1.

CHAPTER 3

BROADBAND POWER AMPLIFIERS

Throughout the past two to three decades several solid-state amplifier topologies have evolved mainly in the field of telecommunication, wireless-communication and broadcasting. The trend in these applications is to make mobile devices and back-bone networks more efficient. Correspondingly the power amplifier modules, which mainly determine the overall power consumption of the whole system, are designed to feature improved power added efficiencies (PAE), as e.g. the Doherty-, Chireix- or Envelope-Tracking amplifier topologies. These amplifiers are besides often claimed to be broadband, arising from historical considerations. Fifty years ago a bandwidth of several hundred MHz presented a technological challenge for a broadband amplifier design. With the technological progress in the semiconductor industry, today a different light is shed on the term "broadband", making it unfortunately ubiquitous in electrical engineering publications. Hence, the exact definition of "broadband/wideband" is not clear and often depends on the application. Out of this reason the term "broadband" within this work is related to the bandwidth demands set by measurement instruments, where several octaves or even decades are required.

3.1 Amplifier Classes

Among the huge diversity of amplifier classes ranging from A to S are only those amplifier classes suited for the implementation of a wideband linear power amplifier, in which the input signal is linearly related to the output signal. If this linear relationship is violated the broadband linearity behavior of such amplifier classes is degraded, but bringing up the secondary positive effect of improved efficiency, which is important for narrowband consumer electronics. Since the most important amplifier parameters in this work are bandwidth, power and linearity, efficiency is not of major concern, but will be reviewed nevertheless shortly in terms of completeness. S. Cripps introduced the so called conduction angle method, in which the conduction angle expresses the ratio of the on-time t_{ON} of a transistor to the signal period time T in radians [68].

$$\alpha = 2\pi\frac{t_{ON}}{T} \tag{3.1}$$

In doing so, the different amplifier classes can be assigned to certain conduction angles α between 0 and 2π.

$$\text{Operational Class} = \begin{cases} A, & \alpha = 2\pi \\ B, & \alpha = \pi \\ C, & \alpha < \pi \end{cases} \tag{3.2}$$

Assuming a sinusoidal drain current with phase $\theta = \omega t$, DC current I_{DC} and peak amplitude I_P, the corresponding waveform signal is of the form

$$I_{\text{DS}} = \begin{cases} I_{DC} + I_P \cdot cos(\theta) & if\ I_{\text{DC}} > I_P \\ 0 & else \end{cases}. \tag{3.3}$$

Based on the fact that the $cos(\theta)$ in (3.3) always varies between -1 and 1, θ can be replaced by values between $-\pi$ and π, which is equal in terms of the conduction angle to the range from $-\alpha/2$ to $\alpha/2$. When the negative RF-signal part in (3.3) becomes equal to the DC current, the drain current $\boldsymbol{I_{DS}}$ becomes zero, thus satisfying the relationship

$$I_{DC} = -I_P \cdot cos\left(\frac{\alpha}{2}\right). \tag{3.4}$$

The drain current in (3.5) can finally be expressed dependent on α by replacing I_{DC} in (3.3) by (3.4), together with the relationship of the maximum peak current $I_{max} = I_{DC} + I_P$.

$$I_{\text{DS}} = \begin{cases} \dfrac{I_{max}}{1 - cos\left(\frac{\alpha}{2}\right)}\left(cos(\theta) - cos\left(\frac{\alpha}{2}\right)\right) & for\ -\alpha/2 < \theta < \alpha/2 \\ 0 & else \end{cases}, \tag{3.5}$$

In a next step applying the Fourier transform gives the desired information about the spectral content of I_{DS} dependent on the conduction angle α. The Fourier transform of the DC component of the drain current I_{DS} can be calculated with

$$I_{DC} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{\text{DS},max}}{1 - cos\left(\frac{\alpha}{2}\right)}\left(cos(\theta) - cos\left(\frac{\alpha}{2}\right)\right)\,\mathrm{d}\theta \tag{3.6}$$

and the corresponding higher n^{th}-order components by

$$I_{D,n} = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{\mathrm{DS},max}}{1 - cos\left(\frac{\alpha}{2}\right)} \left(cos(\theta) - cos\left(\frac{\alpha}{2}\right) \right) \cdot cos(n\theta) \ \mathrm{d}\theta. \tag{3.7}$$

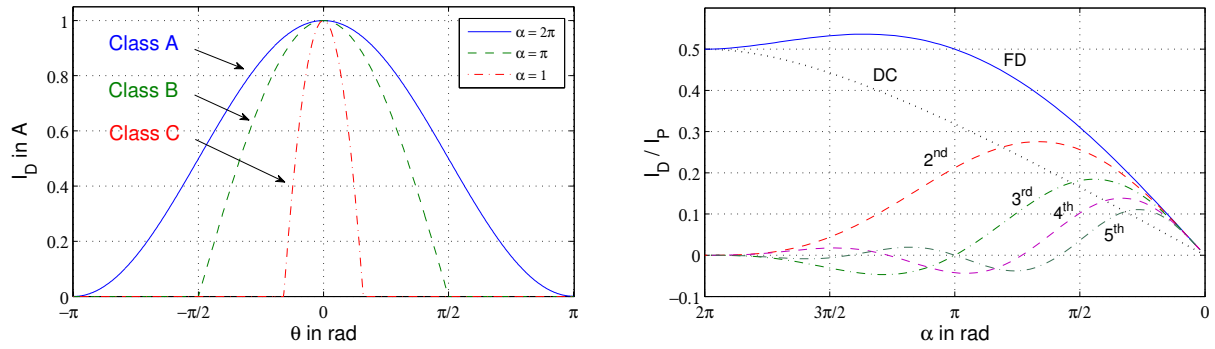
In (3.6) and (3.7) only the real-part of the Fourier transform is considered, since only the magnitude and not the phase of the drain current components is of further interest. The equations in (3.6) and (3.7) can be furthermore simplified to

$$I_{DC} = \frac{I_{\mathrm{DS},max}}{2\pi \left(1 - cos\left(\frac{\alpha}{2}\right)\right)} \left(2 \cdot sin\left(\frac{\alpha}{2}\right) - \alpha \cdot cos\left(\frac{\alpha}{2}\right) \right) \tag{3.8}$$

$$I_{D,1} = \frac{I_{\mathrm{DS},max}}{2\pi \left(1 - cos\left(\frac{\alpha}{2}\right)\right)} \left(\alpha - sin(\alpha) \right) \tag{3.9}$$

and for $n > 1$ to

$$I_{D,n} = \frac{I_{DS,max}}{\pi \left(1 - cos\left(\frac{\alpha}{2}\right)\right)} \left(\frac{sin\left((n-1)\frac{\alpha}{2}\right)}{n-1} + \frac{sin\left((n+1)\frac{\alpha}{2}\right)}{n+1} - \frac{sin\left(\frac{n\alpha}{2}\right) cos\left(\frac{\alpha}{2}\right)}{n/2} \right). \tag{3.10}$$



(a) (b)

Fig. 3-1: (a) I_D vs. θ in rad for the operational classes A,B and C and (b) normalized Fourier components of I_n vs. the conduction angle α

Fig. 3-1 (a) shows three sample waveforms for typical class A, B and C bias. Fig. 3-1 (b) illustrates the just derived Fourier components of the normalized drain current $I_{D,n}$ waveforms over the conduction angle α up to 5th order. For a conduction angle of $\alpha < \pi$, which corresponds to class C operation, the contribution of higher order harmonics increases significantly, whereas the fundamental starts to decrease. The only advantage in this mode of operation is the reduced DC power, which yields higher efficiency the smaller the conduction angle gets. This is owed to the smaller overlapping area under the current and the voltage waveform. At $\alpha = \pi$, which equals class B operation, the fundamental exhibits exactly the same magnitude as in class A ($\alpha = 2\pi$). Based on

the operation for exactly half of the period in class B, as Fig. 3-1 (a) shows, the odd-order (here 3rd & 5th) harmonics get completely cancelled due to the even-order symmetry of the signal. Unfortunately is the 2nd harmonic in class B dominant, which makes this mode of operation unsuitable based on the high demands set by the $SFDR$ requirements in the amplifier specifications.

Furthermore, the normalized output power capability C_P and the maximum efficiency η_{max} are often of interest and can be calculated accordingly dependent on the conduction angle α. When the amplifier is biased with a DC voltage V_{DC}, the maximum obtainable output voltage swing is thus equal to V_{DC} and the effective maximum output power yields

$$P_{OUT,max} = \frac{1}{2} V_{DC} I_P. \tag{3.11}$$

Setting $P_{OUT,max}$ in relation to the theoretical peak power, which is composed of the maximum peak voltage $2V_{DC}$ and maximum peak current $I_{\mathrm{DS},max}$, gives in (3.12) the so called normalized output power capability C_P. If $P_{OUT,max}$ is considered with respect to the dissipated DC power the maximum theoretical realizable efficiency is obtained in (3.13).

$$C_P = \frac{P_{OUT,max}}{2V_{DC} I_{\mathrm{DS},max}} = \frac{\alpha - sin(\alpha)}{8\pi\left(1 - cos\left(\frac{\alpha}{2}\right)\right)} \tag{3.12}$$

$$\eta_{max} = \frac{P_{OUT,max}}{P_{DC}} = \frac{\alpha - sin(\alpha)}{2 \cdot \left(2 \cdot sin\left(\frac{\alpha}{2}\right) - \alpha \cdot cos\left(\frac{\alpha}{2}\right)\right)} \tag{3.13}$$

As Fig. 3-2 shows, the efficiency goes for conduction angles approaching zero up to its theoretical maximum of 100%, whereas the output power capability goes down to 0%. In class B ($\alpha = \pi$) is the output power capability equal to class A ($\alpha = 2\pi$) at 12.5%, but the efficiency is with 78.5% higher than in class A with 50%.

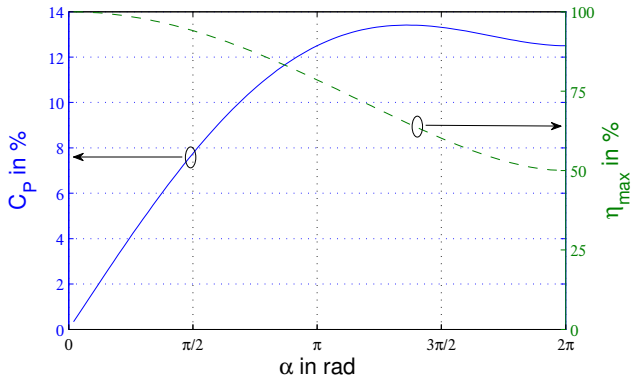


Fig. 3-2: Normalized power capability C_P and maximum effiency η_{max} vs. conduction angle α

The optimum solution of a power amplifier design to end up in high gain, high output power and high linearity is thus only class A. Operation in light class AB ($3\pi/2 < \alpha < 2\pi$) might still be a sufficient solution for the

amplifier design, depending on the actual transfer characteristic of the utilized transistor technology. Therefore, the exact determination of the optimum bias point can only be done by taking a closer look at the real transfer characteristic of the GaN process considered in this work, which is done in chapter 4.2.1. Nevertheless, the conduction angle method is a useful and very effective tool to investigate the different operational classes with respect to gain, power, linearity and efficiency from a very general point of view, which helps the designer to find the proper bias setting.

3.2 Matching

After taking a closer look onto the different linear operational amplifier classes in the foregoing chapter 3.1, it is important to differentiate between the active device (HEMT) matching possibilities in order to attain the targeted performance given by the specifications of the amplifier application. Often there are several different requirements as e.g. good small-signal matching, high output power or low-noise performance of which some of them have to be fulfilled at the same time over wide bandwidths. The following considerations shall help to understand the existing trade-offs for broadband amplifiers.

3.2.1 Small-Signal Matching

(a) Reactive Matching

The simplest amplifier consists of a single-stage common-source HEMT, which is biased at its gate and drain via the RF-chokes L_B, as sketched in Fig. 3-3 below.

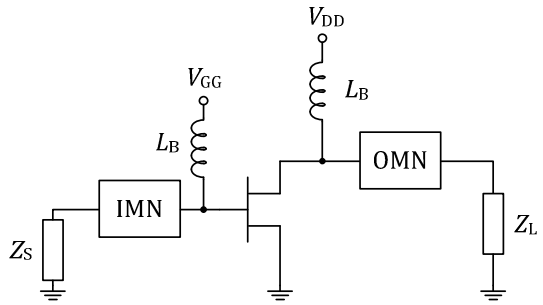


Fig. 3-3: Schematic of common-source HEMT with input- and output matching networks

For proper input- and output match over a certain bandwidth it is necessary to provide an input- and output matching network (IMN/OMN). The task of the IMN/OMN is the compensation of the frequency dependence of the HEMT´s input/output impedance, which will be transformed to the source/load impedance Z_S/Z_L. Narrowband power amplifiers are in general matched by means of a reactive matching network rather than by resistive elements, which introduce additional loss and thus reduce gain, output power and degrade noise performance. Sometimes when the amplifier stability is critical and cannot be guaranteed purely by reactive matching networks, resistive matching elements have to be inserted for stability reasons. The most common stabilization

method found in power amplifiers is a parallel RC-filter in series to the gate of the HEMT, since the amplifier becomes most likely unstable toward low frequencies due to its higher gain of the active device. Thus, at low frequencies the series resistance helps to obtain a better match between source impedance and high input impedance of the HEMT, with the drawback of an increased NF.

In Fig. 3-4 are two options for a purely reactive matching network depicted. Either a series inductance with a parallel capacitance is used or vice versa. Applying the matching concept depicted in Fig. 3-4 (b) for a simple HEMT in common-source configuration, which has to be biased by a voltage at its gate and drain terminals, is not a meaningful approach due to the series capacitors C_1 to C_n. Moreover, based on the fact that the input/output impedance of a HEMT is capacitive and not inductive, the compensation of the input/output capacitance can only be realized by using a series inductance, which affirms that the matching concept from Fig. 3-4 (a) is best suited for broadband matching. The higher the number of LC-stages the more broadband is the matching and the lower is the Q-value of the LC-ladder. Instead of cumbersome mathematical calculations, drawing of the constant Q-region into a smith-chart often helps to find the optimum number of LC-stages for a given bandwidth, since Q is inversely proportional to the bandwidth, as the equation

$$Q = \frac{f_0}{BW} = \frac{\sqrt{f_L f_H}}{f_H - f_L} \tag{3.14}$$

reveals. The necessary Q-factor value can be simply calculated by the given bandwidth and the number of LC-stages can be derived by the number of hops in the smith-chart, which are necessary for the impedance transformation from the source/load impedance to the input/output impedance of the HEMT. Fig. 3-6 (a) displays the constant Q-factor lines and the corresponding number of necessary LC-matching stages in order to stay below a given Q-factor value.

(a) (b)

Fig. 3-4: (a) LC-low pass and (b) CL-high pass matching network

As an example, Fig. 3-6 (b) depicts the transformation from a 50 Ω source impedance to an input impedance of 1.5-j17.5 Ω of an 8×125µm HEMT at 6 GHz by means of a 2-stage LC-ladder, which is shown in Fig. 3-5. Because the minimum realizable Q-factor value is dominated by the input $R_{\mathrm{GS}}C_{\mathrm{GS}}$ low-pass filter of the HEMT, the resulting Q-factor value is equal to 11.8 and cannot be reduced any further by the reactive LC-ladder matching network.

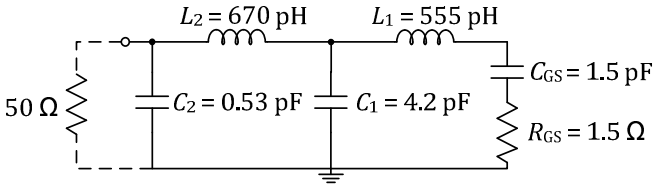
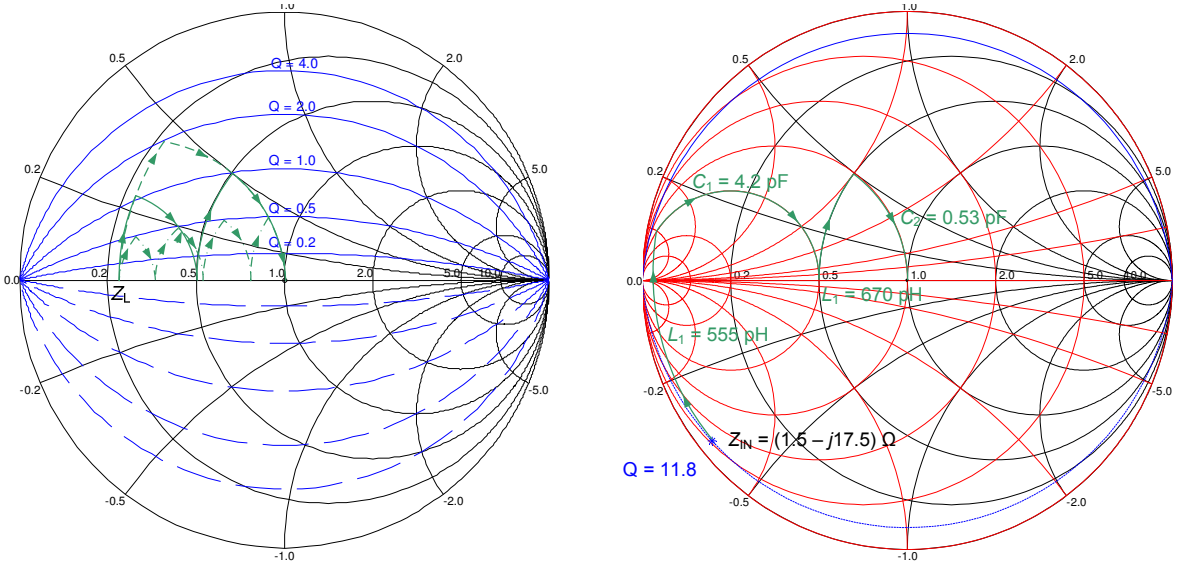


Fig. 3-5: 2-stage LC-low pass matching for a 8×125µm HEMT input impedance to 50 Ω source impedance match

Nevertheless, the number of LC-stages cannot be chosen arbitrarily high to minimize Q in reality, since the series inductors are lossy and have to be interconnected with the grounded capacitors via lossy MSLs. At one point the losses and parasitics of the MSLs become dominant, which hamper further downscaling of the LC-filter sections.



(a) (b)

Fig. 3-6: (a) constant Q-factor curves for RLC-networks with $Q < 0.5$, 1 and 2 and (b) 2-stage LC input matching for an input match of a 8×125µm HEMT to 50 Ω at 6 GHz.

The blue and green trajectory in Fig. 3-7 show the necessary input reflection coefficients over frequency for optimum unilateral gain $G_{s,opt}$ and for attaining minimum noise (NF_{min}) of a 8×125µm HEMT. It can be clearly seen that the optimum source impedances for high gain and low noise diverge over frequency and only start to converge the closer the frequency gets to f_T. When approaching f_T, the source impedances become capacitive again, since the extrinsic parasitic inductances start to dominate over the capacitive intrinsics. But more important is the counterclockwise rotation of the source reflection/impedance curves, which cannot be realized by any real matching circuit as the red two-stage LC-IMN trajectory shows. This is deeply rooted in the causality of the matching network according to the "Kramers-Kronig"-relation [69] or "Foster's" reactance theorem [70], forcing the phase to rotate always in clockwise direction. Optimum match can thus be only realized over narrow bandwidths, as the loop of the red trajectory of a single stage matching network illustrates at around 5 GHz. Increasing the number of matching stages increases the number of loops, which helps to increase the matching bandwidth or performance, according to the Bode-Fano limit [71]. Moreover perfect matching at one single fre-

quency can only be achieved for one single parameter, either for optimum noise or optimum gain performance of the amplifier, but never together at the same time.

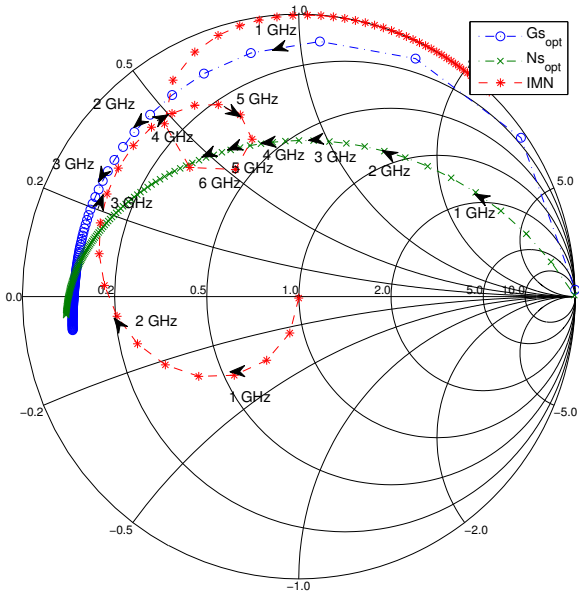


Fig. 3-7: Source reflection circles for max. unilateral gain and optimum noise match for a low-noise 8×125µm GaN HEMT at V_{DS} = 15 V and I_{DS} = 200 mA/mm

(b) Resistive Matching

In the case of broadband amplifiers, the input/output has to be matched over much broader frequency ranges than it is the case for narrow-band amplifiers, where the bandwidth usually stays within one single octave. This cannot be realized over multiple octaves or even decades by means of purely reactive matching networks. Moreover, as soon as the minimum frequency gets close to DC, reactive matching elements have no effect. Therefore, frequency independent resistive elements have to be used for matching purposes. This section concetrates thus on the DC matching trade-offs for the most simple but effective broadband matching approach of parallel and series feedback, as sketched in Fig. 3-8 below.

(a) (b)

Fig. 3-8: (a) CS-HEMT with parallel and series feedback and (b) simplified equivalent circuit for DC matching

The Y-matrix for the DC approximation of Fig. 3-8 (b) can be set up to

$$\overleftrightarrow{Y_{fb}} = \begin{bmatrix} \frac{1}{R_{fp}} & \frac{-1}{R_{fp}} \\ \frac{-1}{R_{fp}} + \frac{g_{m0}R_{\mathrm{DS}}}{R_{fs} + R_{\mathrm{DS}}(1 + g_{m0}R_{fs})} & \frac{1}{R_{fp}} + \frac{1}{R_{fs} + R_{\mathrm{DS}}(1 + g_{m0}R_{fs})} \end{bmatrix}. \tag{3.15}$$

By expressing the input and output impedance of the amplifier by its Y-parameters according to

$$Z_{IN} = \frac{Y_{22} + Y_L}{Y_{11}(Y_{22} + Y_L) - Y_{12}Y_{21}} \tag{3.16}$$

and

$$Z_{OUT} = \frac{Y_{11} + Y_S}{Y_{22}(Y_{11} + Y_S) - Y_{12}Y_{21}}, \tag{3.17}$$

the DC input and output impedance can be calculated for Fig. 3-8 (b) by the following two equations (3.18) and (3.19) below.

$$Z_{IN} = \frac{Z_L + R_{fp}\left(1 + \frac{Z_L}{R_{fs} + R_{DS}(1 + g_{m0}R_{fs})}\right)}{1 + (1 + g_{m0}R_{DS})\frac{Z_L}{R_{fs} + R_{DS}(1 + g_{m0}R_{fs})}} \tag{3.18}$$

$$Z_{OUT} = \frac{Z_S + R_{fp}}{1 + \frac{R_{fp} + Z_S(1 + g_{m0}R_{\mathrm{DS}})}{R_{fs} + R_{\mathrm{DS}}(1 + g_{m0}R_{fs})}} \tag{3.19}$$

Since it is more convenient to think in terms of S-parameters rather than impedances when speaking about matching, the input and output impedance can be translated into the scattering-wave parameters by the relationship

$$S_{11/22} = \frac{Z_{IN/OUT} - Z_S}{Z_{IN/OUT} + Z_S}. \tag{3.20}$$

In the following, Z_S and Z_L are assumed to be only real valued and equal to 50 Ω. Fig. 3-9 (a) illustrates the input (S_{11}) and output (S_{22}) matching dependence given in (3.20) on R_{fp} for a 8×125µm GaN HEMT, considering a full intrinsic small-signal model, which was already presented in section 2.2.1. Applying parallel feedback via R_{fp} enables a wider match to Z_S and Z_L at the same time by reducing the effective input/output impedance Z_{IN} of the HEMT, especially toward low frequencies. It can be clearly seen that the matching at low frequencies can be in particular very well controlled by proper selection of R_{fp}. When applying parallel feedback only, the input and output matching features to be very sensitive to changes in g_{m0} and is thus very bias dependent, as the g_{m0}-term in (3.18)-(3.19) suggests. Only by adding series feedback this bias dependence of Z_{IN} and Z_{OUT} can be reduced, as shown in Fig. 3-10. Therefore, if only parallel feedback in an amplifier design is applied, the matching performance will be strictly limited to its intended operational class.

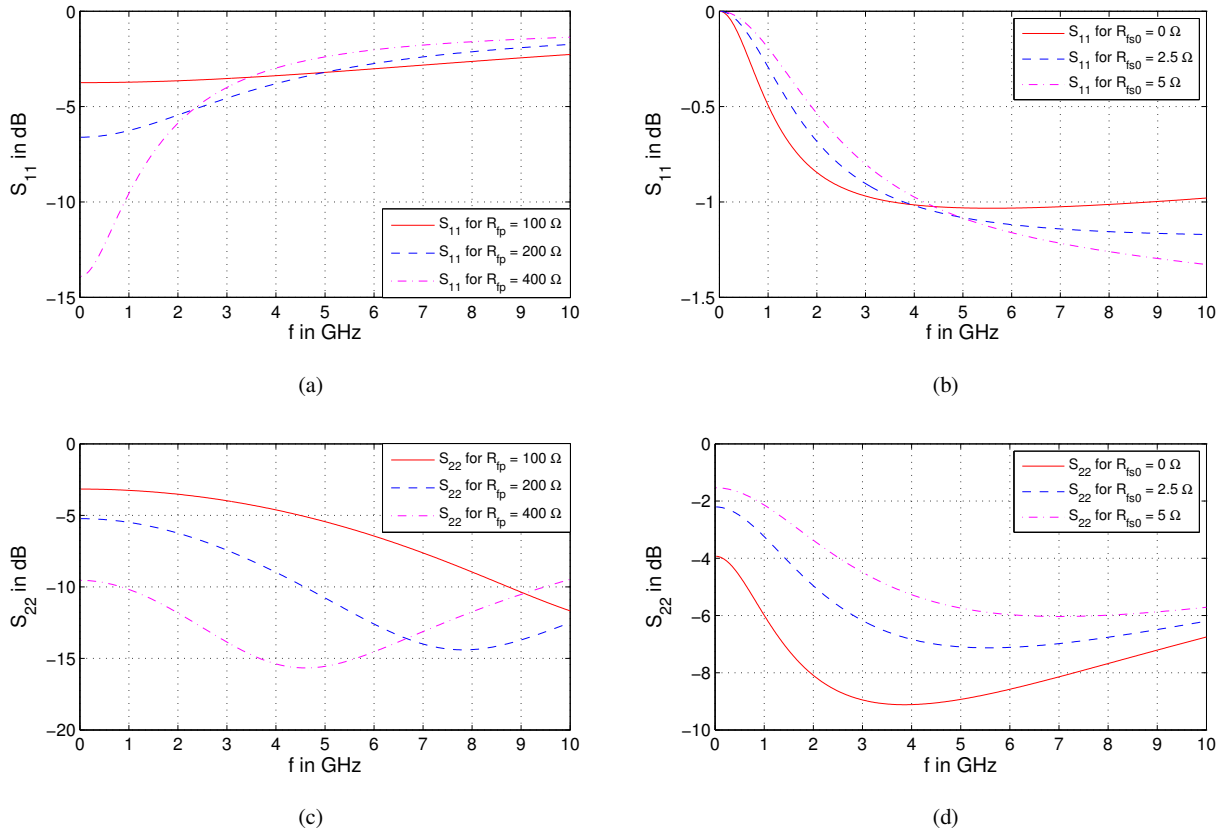


Fig. 3-9: Simulated (a,b) S_{11} and (c,d) S_{22} of parallel (R_{fp}) (left) and series (R_{fs}) (right) resistive feedback matching of a 8×125µm HEMT

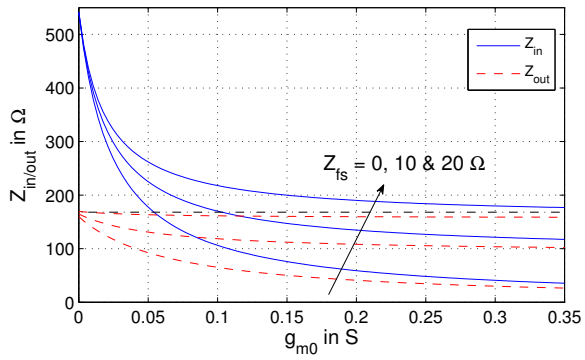


Fig. 3-10: Calculated Z_{IN} and Z_{OUT} vs. g_{m0} of a 8×125µm GaN HEMT with parallel and series feedback for Z_{fp} = 500 Ω and Z_{fs} = 0,10…20 Ω

In the case of series resistive feedback the effective DC input/output impedance Z_{IN} strives toward infinity based on the capacitive input of the HEMT and is thus independent of R_{fs}, as Fig. 3-9 (b) graphs. With increasing frequency the magnitude of Z_{IN} starts to decay due to the capacitive input of the HEMT and R_{fs} takes more effect toward higher frequencies. Z_{OUT} in contrast is affected at DC by R_{fs} due to the finite output resistance R_{DS}. Since a 8×125µm GaN HEMT exhibits at DC a higher output resistance ($R_{\mathrm{DS}} \approx 225\ \Omega$) than the load impedance ($Z_L = 50\ \Omega$), an increase in R_{fs} only impairs the DC output match.

So far neither of the two feedback approaches alone is sufficient to match the 8×125µm GaN HEMT at its input and output simultaneously at DC, as Fig. 3-9 showed. It is thus vital to apply series as well as parallel resistive feedback in GaN to obtain a better input and output match than -10 dB toward DC. Fig. 3-11 depicts all four S-parameters of a 8×125µm GaN HEMT with R_{fp} = 225 Ω and R_{fs} = 0…5 Ω. It already can be seen that for the selected resistor values the input and output match of the amplifier is already better than -10 dB at DC.

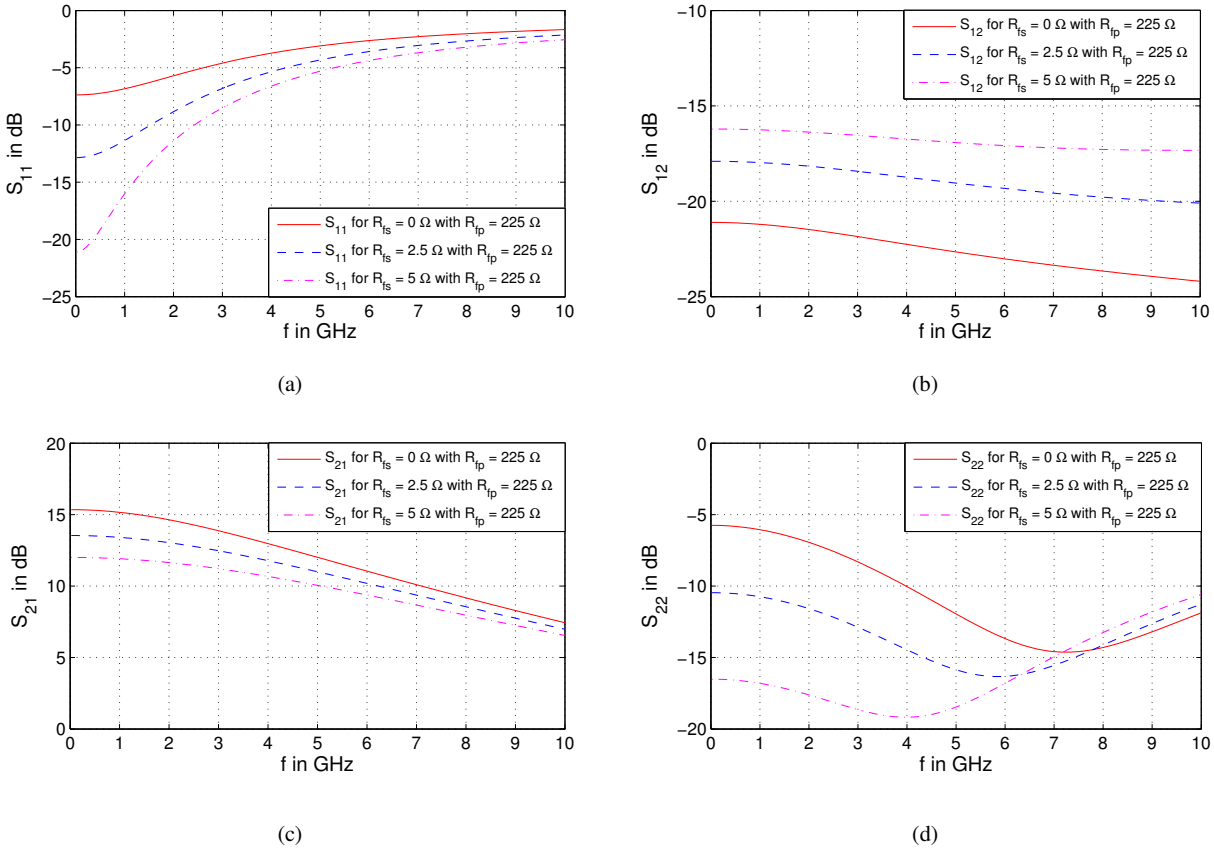


Fig. 3-11: Simulated (a) S_{11}, (b) S_{12}, (c) S_{21} and (d) S_{22} for low frequency matching of a 8×125µm HEMT by means of parallel (R_{fp} = 225 Ω) and series (R_{fs}= 0, 2.5, 5 Ω) resistive feedback

This also can be verified by taking a look at the trajectories of ${S_{11}}^*$ and ${S_{22}}^*$ for a complex conjugate input/output match in the smith-charts in Fig. 3-12. The magenta coloured dashed circle depicts the -10 dB matching area in the smith-charts. It is obvious that S_{11} at DC is strongly dependent on the parallel feedback resistor R_{fp} in (a), whereas the impact of R_{fs} becomes only noticeable towards higher frequencies in (c). S_{22} in contrast is not only dependent on R_{fp} at DC, but additionally on R_{fs} (see (d)), compensating for the decay in output resistance caused by a decrease in R_{fp}. Applying both feedback concepts shows in (e) and (f) that a simultaneous input/output match of better than -10 dB can be achieved by staying within the value range of R_{fp} = 155…327 Ω and R_{fs} = 4.1…12.7 Ω for the 8×125µm device.

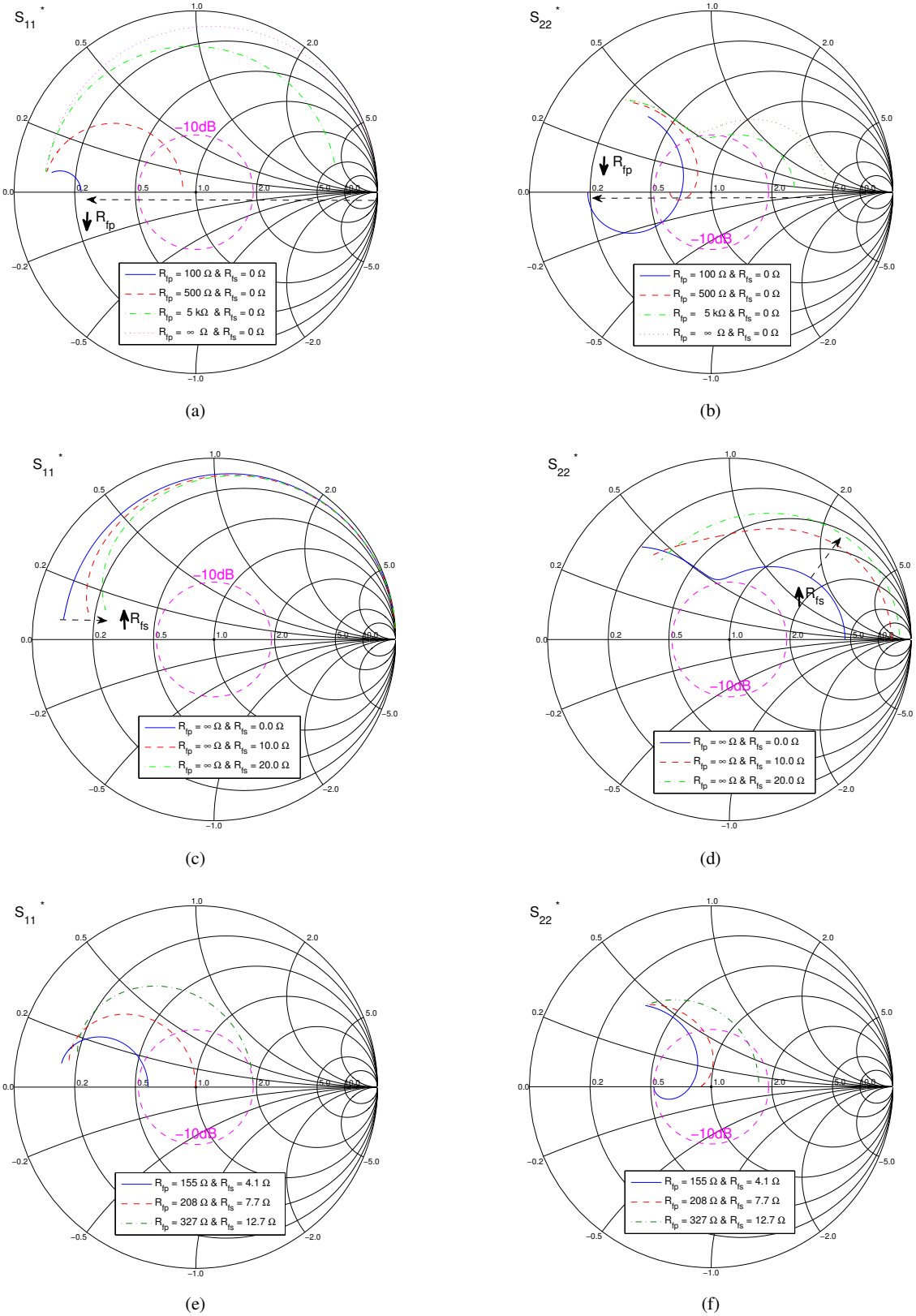


Fig. 3-12: Simulated $S_{11}{}^{*}$ and $S_{22}{}^{*}$ trajectories of (a,b) only parallel (R_{fp}), (c,d) only series (R_{fs}) and (e,f) parallel & series resistive feedback matching of a 8×125µm HEMT in the frequency range from DC – 20 GHz

The value sets for R_{fp} and R_{fs} are unfortunately not very meaningful without considering the gain of the amplifier. Based on the required specifications of the SGs, the amplifier´s S_{21} has to be in the range from 9…12 dB with an I/O-RL of better than 10 dB, as given in Table 1-1. Hence, R_{fp} and R_{fs} cannot be chosen independent from each other. Therefore, it is first off all necessary to determine the relationship between the series- (R_{fs}) and parallel- (R_{fp}) feedback resistance in order to stay within a specified S_{21} range. By expressing the S-parameters in terms of the Y-parameters [72], S_{21} can be in general expressed by

$$S_{21} = \frac{-2Z_0Y_{21}}{(1+Z_0Y_{11})(1+Z_0Y_{22}) - {Z_0}^2Y_{12}Y_{21}}. \tag{3.21}$$

The following expression (3.22) for either R_{fp} or its counterpart R_{fs} in Appendix A result from (3.21) and (3.15). Under the prerequisite of S_{21} being real and constant, R_{fp} and R_{fs} are now related to each other for the low frequency case by

$$R_{fp,S21} = -\frac{2Z_0(S_{21}-1)\left(R_{fs}+R_{\mathrm{DS}}\left(1+g_{m0}R_{fs}\right)\right) + S_{21}{Z_0}^2(1+g_{m0}R_{\mathrm{DS}})}{S_{21}\left(Z_0+R_{fs}+R_{\mathrm{DS}}\left(1+g_{m0}R_{fs}\right)\right) + 2g_{m0}R_{\mathrm{DS}}Z_0} \tag{3.22}$$

After identification of the R_{fp} and R_{fs} dependency on S_{21}, a second boundary is set by S_{11} and S_{22}. Similar to (3.21) for S_{21}, S_{11} and S_{22} can be calculated by

$$S_{11/22} = \frac{(1 \mp Z_0Y_{11/22})(1 \pm Z_0Y_{22/11}) + {Z_0}^2Y_{12}Y_{21}}{(1+Z_0Y_{11})(1+Z_0Y_{22}) - {Z_0}^2Y_{12}Y_{21}}. \tag{3.23}$$

Solving of S_{11} in (3.27) now for R_{fp} gives

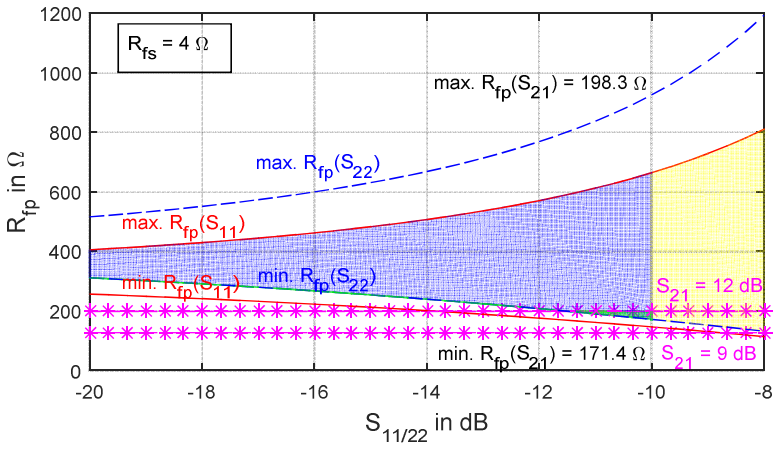
$$R_{fp,S11} = \frac{(1+S_{11})(1+g_{m0}R_{\mathrm{DS}}){Z_0}^2 + 2Z_0S_{11}\left(R_{fs}+R_{\mathrm{DS}}\left(1+g_{m0}R_{fs}\right)\right)}{(1-S_{11})\left(R_{fs}+Z_0+R_{\mathrm{DS}}\left(1+g_{m0}R_{fs}\right)\right)} \tag{3.24}$$

and correspondingly solving of S_{22} for R_{fp}

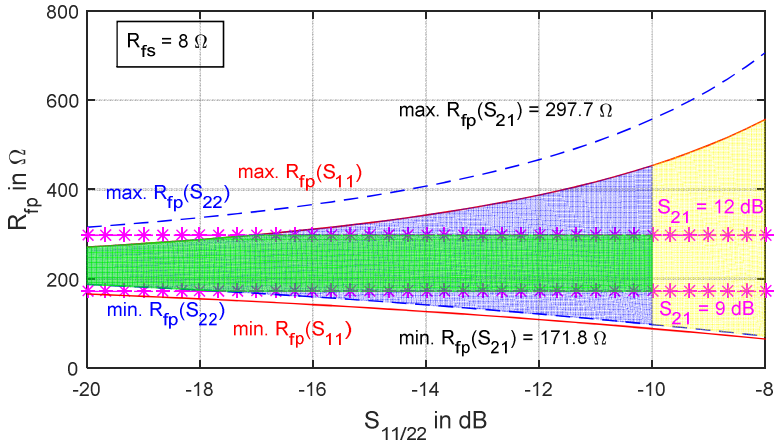
$$R_{fp,S22} = \frac{(1+S_{22})(1+g_{m0}R_{\mathrm{DS}}){Z_0}^2 + 2Z_0S_{22}\left(R_{fs}+R_{\mathrm{DS}}\left(1+g_{m0}R_{fs}\right)\right)}{(1-S_{22})\left(R_{fs}+R_{\mathrm{DS}}\left(1+g_{m0}R_{fs}\right)\right) - Z_0(1+S_{22})}. \tag{3.25}$$

Simplification of the expressions (3.24) and (3.25) for $R_{\mathrm{DS}} \to \infty\,\Omega$ result for $S_{11} = S_{22} = 0$ in the ideal matched condition for R_{fp} to

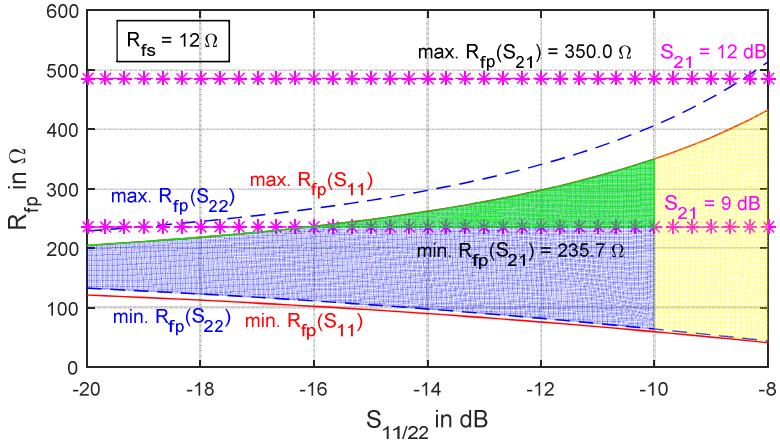
$$R_{fp,match} = \frac{g_{m0}{Z_0}^2}{1+g_{m0}R_{fs}}. \tag{3.26}$$



(a)



(b)

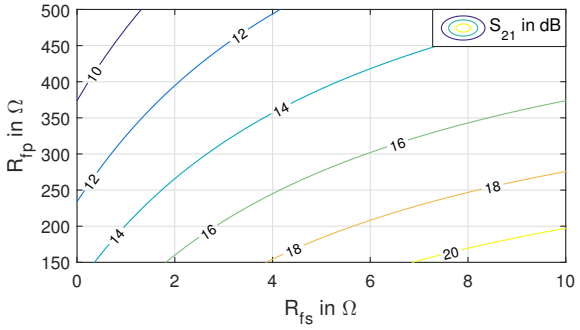


(c)

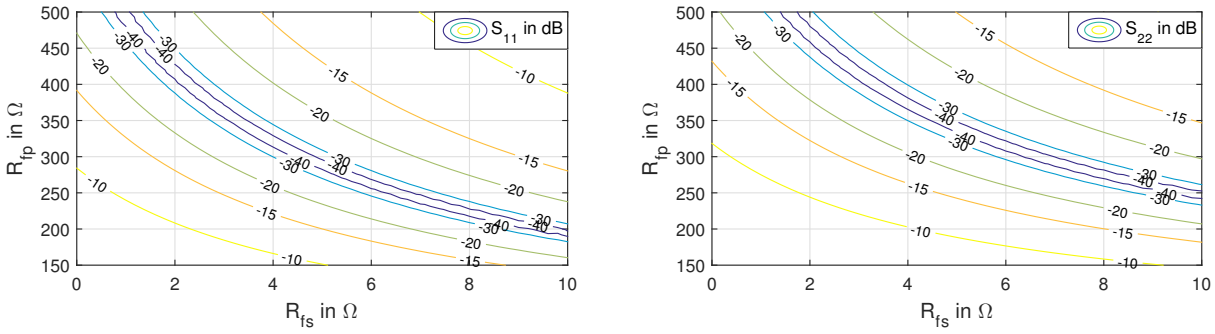
Fig. 3-13: Calculated Z_{fp} vs. $S_{11/22}$ of a 8×125µm GaN HEMT with parallel and series feedback for (a) Z_{fs} = 4 Ω and (b) Z_{fs} = 8 Ω and (c) Z_{fs} = 12 Ω

The now obtained relationships in (3.22), (3.24) and (3.25) between S_{21}, S_{11}, S_{22} and R_{fs}, R_{fp} can be used to determine the valid value set of the feedback elements for a 8×125µm HEMT by plotting R_{fp} vs. $S_{11/22}$ for different R_{fs}. It is also possible to switch the dependence from R_{fp} to R_{fs}, giving the same possible value set for the series feedback resistor R_{fs}. By means of this (graphical) method it is possible to find the exact values for R_{fp} and R_{fs}, which fulfill a given set of low frequency small-signal specifications. It can be seen from Fig. 3-13 that the minimum and maximum value for R_{fp} is limited on the one hand by the minimum required S_{22} at the lower end and on the other hand by S_{11} at the higher end. The enclosed area in yellow marks the valid value set for R_{fp} that results from the corresponding matching constraint on the abscissa, giving a RL below 10 dB. Additionally the blue area encloses the possible value set for R_{fp} for an I/O-RL of better than 10 dB. Since not only the matching is affected by the feedback elements but also the gain (S_{21}), it is necessary to plot additionally the specified gain range from 9 to 12 dB into the same graph. The finally spaned green area illustrates the resulting reduced value set for R_{fp}, limited by the values max. $R_{fp}(S_{21})$ and min. $R_{fp}(S_{21})$, which fulfill the condition of $S_{11/22}$ < -10 dB plus S_{21} = 9…12 dB. It can be derived from Fig. 3-13 (a) to (c) that the valid value set for R_{fs} is constraint by the realizable gain range. If e.g. R_{fs} is chosen equal to 4 Ω, as in Fig. 3-13 (a), a S_{21} of 12 dB with 10 dB I/O-RL can just be realized. A further reduction of R_{fs} would allow for a gain increase but at the same time violates the matching requirement. Similarily, chosing R_{fs} larger than 12 Ω as in Fig. 3-13 (c), sets an upper limit on the maximum obtainable gain. Accordingly, the optimum value in terms of DC matching is found from Fig. 3-13 (b) for R_{fs} to be around 8 Ω. Any change in R_{fp} will directly impact S_{21} but will only affect S_{11} and S_{22} to a minor extent. Translated to a concrete feedback amplifier design with e.g. a 8×125µm GaN device, selection of R_{fp} between 172 Ω and 297.5 Ω with R_{fs} = 8 Ω will end up in a low frequency S_{21} between 9 dB to 12 dB with an input/output match of better than at least -17 dB.

Another way of visualizing the dependency between the feedback resistors is in form of contour plots in Fig. 3-14. Therein, the direct coherency between (a) S_{21}, (b) S_{11} and (c) S_{22} and R_{fp} and R_{fs} is depicted. Mentionable is the perpendicular trajectory of the constant gain (S_{21}) and matching (S_{11}, S_{22}) contours, which underlines the unique existence of a specific gain-matching point for one specific R_{fp} and R_{fs} value set.



(a)



(b) (c)

Fig. 3-14: Calculated (a) S_{21}, (b) S_{11} and (c) S_{22} of a 8×125µm GaN HEMT for different R_{fs} and R_{fp}

3.2.2 Theory of Optimum Power Matching

It is tempting to simply think of conjugate complex matching in terms of small-signal S-parameters as the optimal solution in terms of power matching. In order to maximize the power transfer from the input to the output load, it is necessary to add input/output matching networks (IMN/OMN) to transform S_{11} into Z_S^* and S_{22} into Z_L^*, as already discussed in the foregoing section 3.2.1 and once again shown in Fig. 3-15 below.

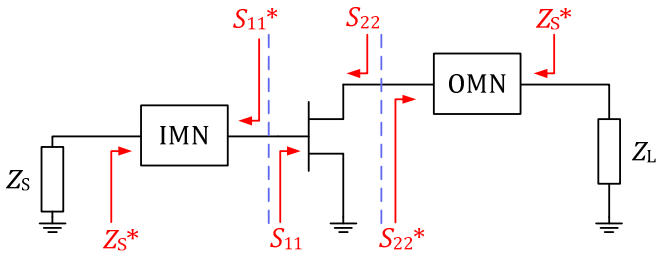
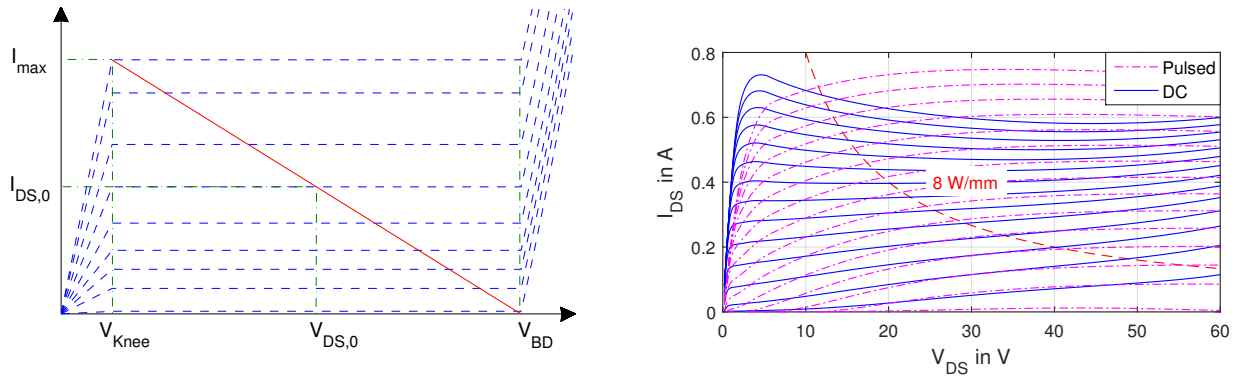


Fig. 3-15: Schematic of a complex conjugate matched transistor to the source and load impedance Z_S and Z_L

From this simple small-signal point of view power matching would be independent of the RF drive signal and thus only dependent on frequency. Unfortunately, this is only true for one single bias-point under large-signal operation, because the intrinsic transistor parameters are dependent on the bias voltages V_{GS} and V_{DS}, as presented in section 2.2.2. Hence, the optimum complex conjugate input/output impedance changes with bias condition. Moreover, the source and load impedance seen by the transistor determine the amount of current and voltage swing, which is seen by the transistor and which in turn affect the values of the nonlinear intrinsic elements. It is therefore crucial to sweep the source and load impedance for a predefined input power and bias-point across a certain parameter space in order to identify the optimum load, which maximizes output power. This approach is also known as load-pull measurement. Nevertheless, a simple but ingenious analytical approach for the determination of the load-pull contours was presented by S. Cripps in [68], which will be shortly reviewed here.



(a) (b)

Fig. 3-16: (a) ideal I-V-curves of HEMT with optimum load-line and (b) simulated DC and pulsed isothermal I-V-curves of a 8×125µm GaN HEMT, including the recommended max. power dissipation hyperbola for P_{diss} = 8 W/mm

The optimum load impedance under large-signal operation can be traced back to the bias settings and basic I-V-characteristics of the transistor. The basic idea is depicted in Fig. 3-16 (a), showing the optimum load-line for an idealized I-V-transfer characteristic. Based on this coherency the optimum load resistance $R_{L,opt}$, which exploits the full power handling capability of a transistor in class A, has to be chosen equal to

$$R_{L,opt} = \frac{V_{BD} - V_{kn}}{I_{DS,max}} \approx \frac{V_{DS,0}}{I_{DS,0}}. \tag{3.27}$$

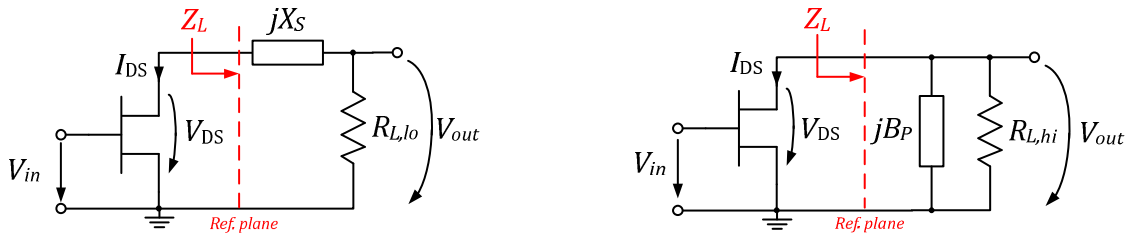
The approximation in (3.27) is only valid if the knee-voltage V_{kn} is negligibly small compared to the break-down-voltage V_{BD}. In reality, thermal as well as frequency dependent trapping effects lead to a significant difference in the DC/static and RF-/isothermal I-V-curves, as indicated in Fig. 3-16 (b) for a 8×125µm GaN HEMT. As can be observed, V_{kn} as well as the magnitude of I_{DS} are strongly dependent on the applied bias-pont as well as on the operational frequency. This huge thermal impact on the I-V-characteristics leads to the well-known effects, such as "knee-walk out", "current slump" or low-frequency dispersion, making the GaN HEMT's I-V-characteristic heavily dependent on the applied bias-point and frequency of operation, as discussed in detail e.g. in the publications [73, 74, 75, 76, 77].

Returning to the ideal I-V-curves in (a), the trajectory of the ideal load-pull contours can be deduced, marking all load impedances in a smith-chart which deliver constant output power. The deviation from the maximum output power is furthermore described by the linear degradation factor p, giving for the delivered output power

$$P_L = \frac{P_{L,max}}{p}. \tag{3.28}$$

In general two different load impedance values exist, which give the same output power P_L. One exhibits a higher value than $R_{L,opt}$, so that the voltage starts to clip and the other is found at a lower value, where the current starts to clip. These two resistance values can be expressed in terms of p by $R_{L,hi} = p \cdot R_{L,opt}$ and $R_{L,lo} = R_{L,opt}/p$. Furthermore, any change in reactance will not necessarily affect the delivered output power, as long

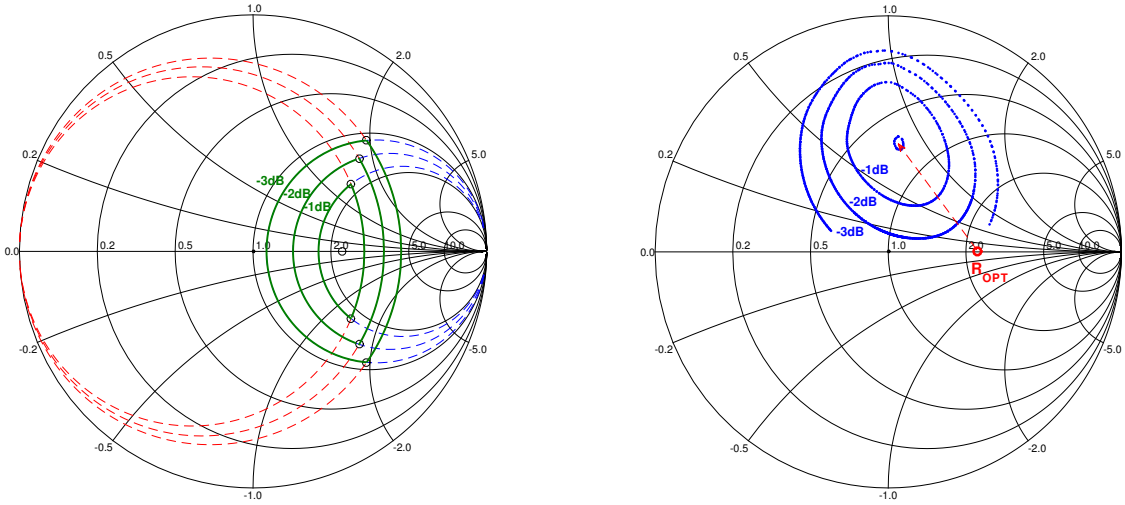
as the overall real-part is not changed. This holds true for either a series reactance (X_S) or a parallel susceptance (B_P), as Fig. 3-17 sketches.



(a) (b)

Fig. 3-17: Large-signal output matching for (a) series reactance and (b) parallel susceptance delivering constant output power to $R_{L,lo}$ and $R_{L,hi}$

The former increases the voltage swing of V_{DS} with an additional shift in phase but does not alter the current I_{DS} through $R_{L,lo}$, as (a) shows. Thus, for different reactance values X_S exactly the same output power equal to ${I_{\mathrm{DS}}}^2 R_{L,lo}/2$ is delivered to the load. For the parallel combination in (b) the current I_{DS} is partly dumped in the parallel susceptance B_P, whereas the magnitude of V_{DS} stays constant and only gets shifted in phase. Therefore, the output power is constant and equal to ${V_{\mathrm{DS}}}^2/\left(2 \cdot R_{L,hi}\right)$. So by moving on a constant resitsance ($R_{L,lo}$) and constant conductance ($1/R_{L,hi}$) circle (dashed lines), the ideal load-pull contours can be drawn into the smith-chart, as depicted in Fig. 3-18 (a). The intersection of both trajectories, which is indicated by circles, is the point where $R_{L,lo} + jX_S$ becomes equal to $1/\left(R_{L,hi} + jB_P\right)$. This explains the non-circular nature of the load-pull contours opposed to the circular constant gain contours, which are based upon small-signal complex conjugate matching.



(a) (b)

Fig. 3-18: (a) Calculated ideal load-pull contours according to Fig. 3-17 and (b) simulated load-pull constours of a 8×125µm HEMT at f = 6 GHz and P_{IN} = 26 dBm

It has to be noticed that as soon as any reactive component is placed to the left hand side of the reference plane in Fig. 3-17, as e.g. the parallel output capacitance C_{DS}, the load-pull contours start to rotate counter-clockwise, as shown in Fig. 3-18 (b) for the load-pull contours of a 8×125µm GaN HEMT. The "egg-shaped" nature of the trajectories results mainly from the changing nonlinear intrinsic parameter values for different loading conditions of the HEMT.

Also worth mentioning is the impact of frequency induced phase shifts between current and voltage by a complex load on the load-line, which leads to an opening of the load-line into an ellipse opposed to the perfect matched load-line sketched in Fig. 3-16 (a). If the load impedance seen by the current source of the HEMT is capacitive, the load-line rotates counterclockwise. Vice versa if it is inductive, the load-line starts to rotate clockwise. The output conductance of a HEMT is furthermore not perfectly zero, as up to now silently presumed by the ideal current source. In order to maintain the perfect load-line for an optimum power match, the parallel connection of R_{DS} and R_L needs to be equal to $R_{L,opt}$. In some cases R_L cannot be chosen completely freely but is predefined by the application. In this case an optimum $R_{\mathrm{DS},opt}$ can be determined by (3.29) for a given load resistance R_L.

$$R_{DS,opt} = \frac{R_L}{\frac{R_L I_{DS,0}}{V_{DS,0} - V_{kn}} - 1}. \tag{3.29}$$

As long as the condition $R_{\mathrm{DS}} > R_{\mathrm{DS},opt}$ is satisfied, the output voltage-swing of the HEMT clips and the delivered output power to R_L stays constant at $(V_{BD} - V_{kn})^2/(8R_L)$. For $R_{\mathrm{DS}} < R_{\mathrm{DS},opt}$ in contrast, the maximum output voltage-swing is lowered due to the lower effective load resistance seen by the current source. Accordingly, the current-swing through R_L decreases, because part of I_{DS} is now dumped in R_{DS} and not delivered to the output load anymore. In this case the delivered output power becomes equal to

$$P_L = \frac{{I_{\mathrm{DS},0}}^2 R_L}{2}\left(\frac{1}{1 + \frac{R_L}{R_{\mathrm{DS}}}}\right)^2, \tag{3.30}$$

showing that for $R_{\mathrm{DS}} \to \infty$ the delivered output power P_L saturates at ${I_{\mathrm{DS},0}}^2 R_L/2$, which is equal to

$$P_{L,max} = \frac{(V_{BD} - V_{kn})^2}{8R_L}. \tag{3.31}$$

3.2.3 Load-Line Matching in TWAs

Within this section power matching of each single transistor stage in a uniform distributed amplifier (UDPA) will be discussed from a very general and theoretical point of view. Despite the known improvement in power matching in TWAs by using nonuniform designs with tapered drain-lines and tapered transistors (NDPA), as was presented by C. Duperrier *et al.* in [78], this section focuese only on the power match in uniform TWAs. Moreover, on top of the often only regarded static load condition, the frequency dependent loads will be calculated for each stage in a UDPA. It is important to distinguish between static and frequency dependent load conditions, since in a UDPA the static load condition is equal for each transistor stage, but the frequency dependent load varies strongly. To the author´s best knowledge only few papers in the common literature exist, dealing with the phenomenon of load-line mismatch in UDPAs [78, 79, 80]. As already mentioned in [79], the load-line of the 1st transistor in a UDPA is strongly mismatched at certain frequencies and the transistor is almost short-circuited. Up to now, the fact that the load-line of the 1st transistor in UDPAs tilts more than 45° clockwise and starts to dissipate power has only been briefly addressed in [80]. The reason for this phenomenon is based on the phase difference of propagating voltage waves on the drain line and transistor output current with changing frequency, which has not been addressed in the literature so far. In this condition the transistor might be operated in a state with undesired high power dissipation with output current and voltage "in-phase"[1], exceeding the typical maximum power dissipation hyperbola. This might lead to degraded reliability or severe short term damage of the transistor. All considerations in the ongoing sections refer to a simplified and idealized UDPA structure, as depicted in Fig. 3-19. Each transistor stage is substituted by an ideal voltage-controlled current-source (VCCS), which is pertinent for a general study of the dynamic RF load-line behavior in UDPAs.

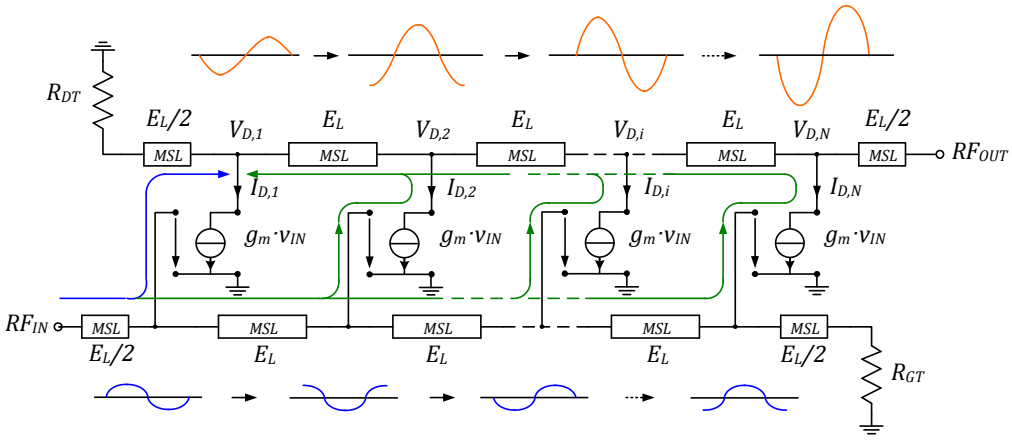


Fig. 3-19: Simplified schematic of a N-stage UDPA

As already deduced from theory [78], the load impedance each transistor has under RF-drive in a UDPA differs from stage to stage, but is close to DC proportional to the amount of current sunk in the effective load Z_L and can be expressed by

[1] "In-phase" refers herein to the phase-difference $\Delta\varphi_{V1,i}(N)$ between voltage and current being smaller than 90° or larger than 270°.

$$V_{OUT} = N \cdot \frac{I_{D,i}}{2} \cdot Z_L \;\Leftrightarrow\; \frac{V_{OUT}}{I_{D,i}} = Z_{L,i} = \frac{N \cdot Z_L}{2}. \tag{3.32}$$

Thus, to obtain power match in a UDPA the number of stages N can be chosen such that at very low frequencies all stages or at higher frequencies the Nth transistor matches the "Cripps-load" condition for a given device size. Fig. 3-20 depicts the load-lines for $E_l = 0°$ for simplicity, neglecting RF-influences on the trajectory.

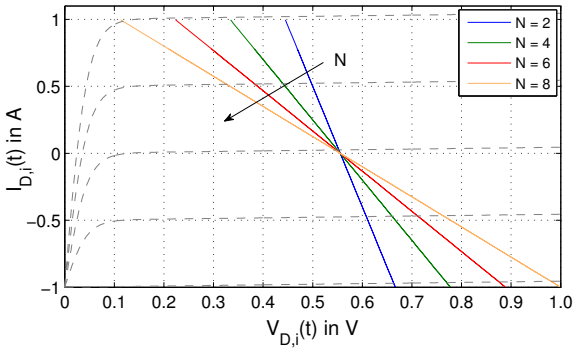


Fig. 3-20: Normalized transistor load-lines in a UDPA for N = 2,4,6 & 8 at E_l = 0°

In a simplified approach the corresponding magnitudes of voltage and current at the drain terminal of the i^{th}-stage can be derived for N equal stages. From Fig. 3-19 $V_{\mathrm{D},i}(N)$ can be expressed by the following relationship

$$V_{D,i}(N) = \frac{1}{2} V_{IN} \cdot g_m \cdot Z_L \cdot exp\left(-j\frac{1}{2}\beta_G l_G\right) \cdot \sum_{k=1}^{N} exp\left[-j\left((k-1)\beta_G l_G + |k-i|\beta_D l_D\right)\right] \tag{3.33}$$

for $i = 1 \ldots N$, assuming that attenuation coefficients on gate- and drain-line are $\alpha_G = \alpha_D = 0$ and g_m is identical for each transistor stage. Additionally, the factor 1/2 in (3.33) assumes that $Z_L = R_{DT}$. Correspondingly, the drain current $I_{\mathrm{D},i}(N)$ of the ith transistor can also be calculated to

$$I_{\mathrm{D},i}(N) = V_{IN} \cdot g_m \cdot exp\left[-j\left(i - \frac{1}{2}\right)\beta_G l_G\right]. \tag{3.34}$$

Now, the load impedance seen by the i^{th}-stage can be calculated by means of (3.33) and (3.34) to

$$Z_{\mathrm{D},i}(N) = \frac{V_{\mathrm{D},i}(N)}{I_{\mathrm{D},i}(N)} = \frac{Z_L}{2} \cdot \left[\sum_{k=1}^{N} exp\left[-j\left((k-i)\beta_G l_G + |k-i|\beta_D l_D\right)\right]\right]. \tag{3.35}$$

The real-part of the load impedance from (3.35) seen by the i^{th}-stage can be used as a measure of the degree of load-line tilt. Furthermore to keep the analysis simple, $\beta_{\mathrm{G}} l_{\mathrm{G}} = \beta_{\mathrm{D}} l_{\mathrm{D}} = \beta l$, which results in

$$Re\{Z_{\mathrm{D},i}(N)\} = Re\left\{\frac{V_{\mathrm{D},i}(N)}{I_{\mathrm{D},i}(N)}\right\} = \frac{R_L}{2}\cdot\sum_{k=1}^{N} cos\big((k-i+|k-i|)\beta l\big). \tag{3.36}$$

From (3.36) it can be inferred that the impedance seen by the i^{th}-stage is symmetric with respect to $\beta l = E_{\mathrm{l}} = 90°$. Contrary to the often misleading assumption that each transistor sees the same load impedance, the impedance starts to decline with increasing E_l from the N^{th}- to the 1st stage due to the constructive drain line voltage superposition toward the output. It is also worth mentioning that not only the 1st stage suffers from optimum load mismatch, but rather the first N-1 stages. The closer the stage is placed to the drain-termination R_{DT} the more pronounced is the mismatch. Noticeable are the electrical length regions, where the $Re\{Z_{\mathrm{D},i}(N)\}$ becomes negative. Exactly this criterion can be used as an indicator for the more than 45° tilt of the 1st transistor´s load-line. The dependence of the $Re\{Z_{\mathrm{D},1}(N)\}$ on E_l and N is plotted in Fig. 3-22. It can be seen that the magnitude of $Z_{\mathrm{D},1}(N)$ increases proportional to N for $E_{\mathrm{l}} = 0°$ and $E_{\mathrm{l}} = 180°$. Therefore, the larger N the higher is the load-impedance for the 1st transistor stage, as already shown in Fig. 3-20. With increasing E_{l}, $Z_{\mathrm{D},1}(N)$ starts to decrease and to vary, diverging from optimum power match. In accordance to the number of transmission line sections N-1 roots in $V_{\mathrm{D},1}(N)$ occur at electrical lengths of

$$E_{l,180°}(n,N) = 180^{\circ}\cdot\frac{n}{N}\,;n = 1\ldots N-1 \tag{3.37}$$

and the phase $\Delta\varphi_{VI}(N)$ between current $I_{\mathrm{D},1}(N)$ and voltage $V_{\mathrm{D},1}(N)$ exceeds multiples of 180°. The critical region of $E_{\mathrm{l}}(N)$, denoted by $\Delta E_{\mathrm{l}}(n,N)$, where $\Delta\varphi_{VI}(N)$ exceeds 180° ± 90° until it shifts by 180° in phase at $E_{\mathrm{l},180°}(n,N)$, is presented in Fig. 3-21 and calculated in (3.38).

$$\Delta E_l(n,N) = \begin{cases} 180°\left(\frac{n}{N} - \frac{2n-1}{2(N-1)}\right), n = 1\ldots\left\lceil\frac{N-1}{2}\right\rceil \\ 180°\left(\frac{2n-1}{2(N-1)} - \frac{n}{N}\right), n = \left\lceil\frac{N+1}{2}\right\rceil\ldots N-1 \end{cases} \tag{3.38}$$

The distinction between $E_{\mathrm{l}}(N) < 90°$ and $E_{\mathrm{l}}(N) > 90°$ in (3.38) has to be made based on the symmetry around $E_{\mathrm{l}}(N) = 90°$.

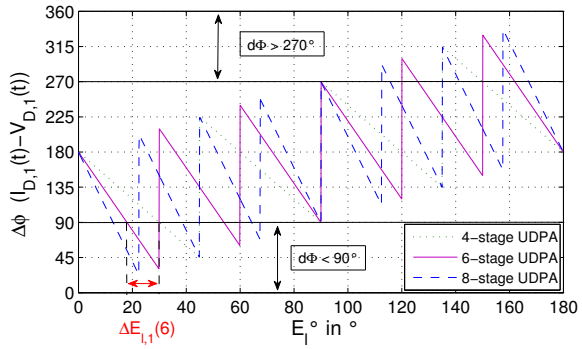
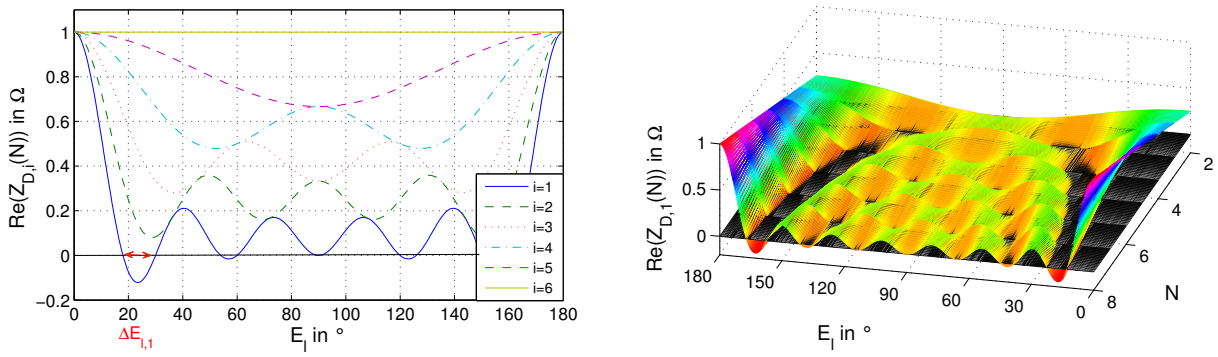


Fig. 3-21: Phase difference at the drain terminal of the 1st gain-stage between current $I_{\mathrm{D},1}(t)$ and voltage $V_{\mathrm{D},1}(t)$ for N = 4, 6, 8.



(a) (b)

Fig. 3-22: Normalized (a) $Re\{Z_{\mathrm{D},i}(N)\}$ vs. E_l for $N = 6$ and $i = 1,2\ldots6$ and (b) $Re\{Z_{\mathrm{D},1}(N)\}$ vs. E_l and N for $Z_\mathrm{L} = 50\ \Omega$

Furthermore, the higher the number of stages N, the higher the negative real-part and the more distinct the tilt of the load line into the passive region. Finally by means of (3.39) the critical electrical length realm for the tilting load-lines dependent on N can be identified and transferred to every UDPA design independently of the chosen technology.

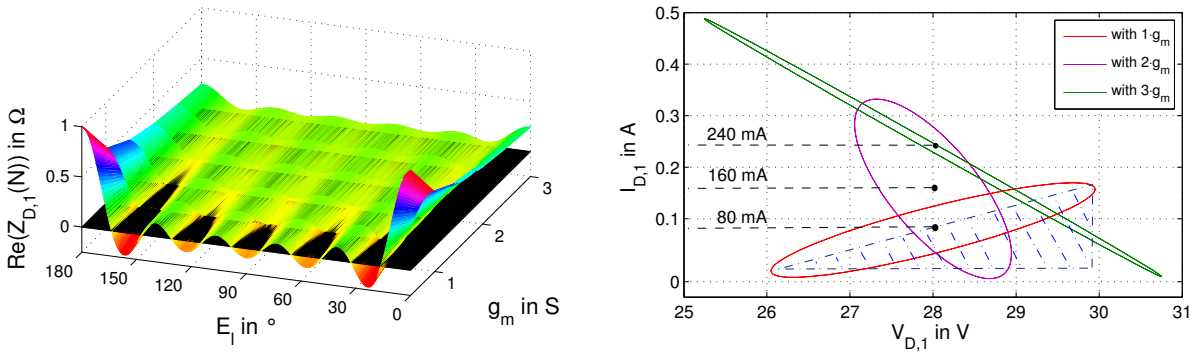
$$E_{l,t}(n,N) = \begin{cases} E_{l,180^\circ}(n,N) - \Delta E_l(n,N), n = 1 \ldots \left\lceil \frac{N-1}{2} \right\rceil \\ E_{l,180^\circ}(n,N) + \Delta E_l(n,N), n = \left\lceil \frac{N+1}{2} \right\rceil \ldots N-1 \end{cases} \tag{3.39}$$

Remedies to Suppress Tilting Load-Lines

In general, there are three options to suppress tilting load-lines in the 1st transistor stage in a UDPA. The first option is to taper the drain lines toward R_{DT} in order to increase the line impedances. This reduces the magnitude of backward traveling waves on the drain line and therewith diminishes destructive voltage superposition at the 1st transistor drain terminal. Unfortunately, tapering is accompanied by the drawback of worse output matching and is limited by the maximum current density of the drain-line. In order to comply with design specifications and technology limitations, tapering was applied in the UDPA design without success.

The second is using a non-uniform DPA (NDPA), where the 1st transistor stage exhibits higher gain (g_m) than the subsequent stages. Thereby the current contribution of the 1st transistor stage to the overall current on the drain-line is increased, which yields less phase drift between $I_{\mathrm{D},1}(N)$ and $V_{\mathrm{D},1}(N)$. This can be verified from Fig. 3-23 (a), where the $Re\{Z_{\mathrm{D},1}(N)\}$ for ratios $r = g_{m,1}/g_{m,n\neq1} \gtrsim 2$ does not exhibit negative values. The opposite is obtained, when r is smaller than one, leading to an increased $\Delta E_l(n,N)$, which is highlighted by black areas in Fig. 3-23. The simulated load-lines in Fig. 3-23 (b) of the implemented UDPA from Fig. 3-19 underline the just mentioned relations, where the bias current increases proportional to g_m but all other intrinsic transistor parameters have been kept constant. Choosing values for r larger than 2 in real designs is not meaningful, since C_{GS} and C_{DS} increase by almost the same amount and thus deteriorate gain and matching performance of the UDPA. Alternatively a gate-coupling capacitor C_C can be used to compensate for the increase in C_{GS} at the 1st stage, but also with the downside of reduced current contribution on the drain-line, which equals

an effective smaller g_m. Other measures, as e.g. mistuning of the transmission line lengths or of other circuit components just produce a shift in frequency but do not suppress tilting of the load-line. Sometimes also misleadingly interpreted is the opening of the load-line that is not the result of RF transistor parasitics but rather the artefact of the phase difference between $I_{\mathrm{D},i}(N)$ and $V_{\mathrm{D},i}(N)$, representing inductive or capacitive loads to the transistor. The third option would be the operation of the UDPA only in the frequency range where the load-line of the 1st transistor does not tilt, which sets a high low frequency boundary for the design and thus limits the maximum obtainable bandwidth.



(a) (b)

Fig. 3-23: (a) normalized $Re\{Z_{\mathrm{D},1}(N)\}$ vs. E_{l} & g_m for N = 6 and (b) load-lines of 1st transistor of the DC-15 GHz UDPA with r = 1, 2 & 3 at f = 3.1 GHz & P_{IN} = 18 dBm

3.3 Feedback Power Amplifiers

3.3.1 Transfer Characteristics

Feedback based amplification is a well-known concept to realize flat gain with good linearity and low noise performance at the same time over wide bandwidths. As presented in chapter 3.2.1, to obtain good input and output matching down to DC it is crucial to apply parallel as well as series resistive feedback, as depicted in Fig. 3-24 below. But before heading into the exact transfer characteristic of the series- and parallel FBPA, a short review of the existing power gain definitions will be conducted.

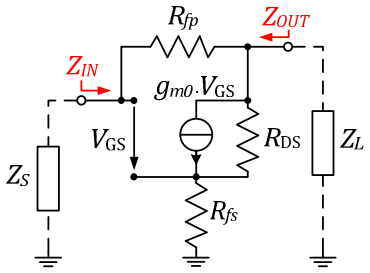


Fig. 3-24: Equivalent circuit of FBPA with series and parallel resistive feedback at DC.

A large number of different definitions for power gain exist in the literature, e.g. the unilateral power gain (U) defined by S. J. Mason in [81], the maximum efficient power gain (MEG) by K. L. Kotzebue in [82], the maximum stable gain (MSG) and the maximum available gain (MAG) by J. M. Rollett in [83]. All of these FoMs take different matching conditions into account, except for the first one which is also valid for unstable or oscillating devices due to the lossless reciprocal unilateralisation. The latter three can be expressed in terms of immitance parameters and Rollett´s stability factor k, whereby the MSG represents the maximum power gain at the stability limit (k = 1) of the MAG. The MAG and MSG can be in general expressed according to [83] by

$$MSG = \left|\frac{S_{21}}{S_{12}}\right| = \left|\frac{Y_{21}}{Y_{12}}\right| \tag{3.40}$$

and

$$MAG = \left|\frac{S_{21}}{S_{12}}\right|\left(k - \sqrt{k^2 - 1}\right) = \left|\frac{Y_{21}}{Y_{12}}\right|\left(k - \sqrt{k^2 - 1}\right), \tag{3.41}$$

where k can be expressed by the immitance parameter I_{xy} and is equal to

$$k = \frac{2\,Re\{I_{11}\}Re\{I_{22}\} - Re\{I_{12}I_{21}\}}{|I_{12}I_{21}|}. \tag{3.42}$$

I_{xy} in (3.42) can be exchanged by any of the conventional Z-,Y-,G- or H-parameters. Plotting of the MSG might be of interest for the designer in order to take a look at the theorertically maximum obtainable power gain of the PA. The MAG in contrast shows the actual power gain limit under a given impedance environment, including a possible intended stability margin. Plotting of both FoMs into one digramm often helps the designer to

assess how close a PA is designed to the stability limit of $k = 1$. For the DC case, the MSG results according to the Y-parameters already derived in (3.15) in

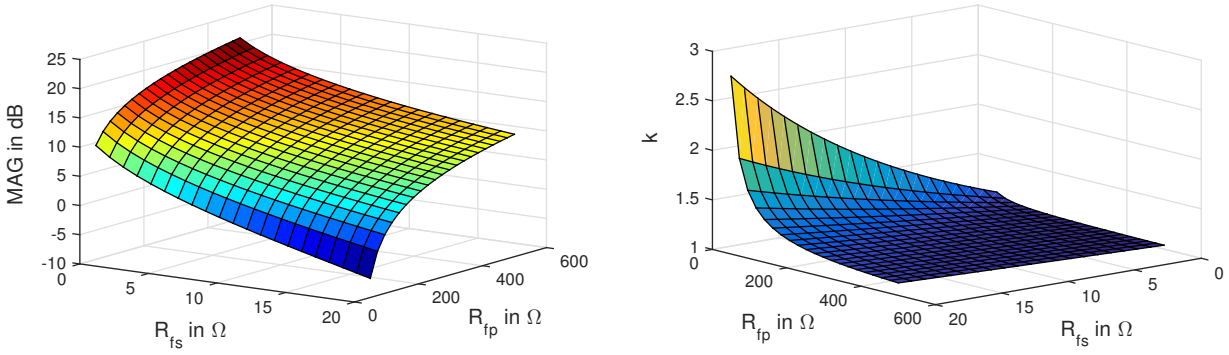
$$MSG = \left| 1 - \frac{g_{m0} R_{DS} R_{fp}}{R_{fs} + R_{DS}\left(1 + g_{m0} R_{fs}\right)} \right| \tag{3.43}$$

and the MAG in

$$MAG = MSG \cdot \left(k - \sqrt{k^2 - 1} \right), \tag{3.44}$$

with

$$k = \frac{2R_{fp} + R_{fs} + g_{m0} R_{DS}\left(R_{fs} + R_{fp}\right)}{\left| R_{DS} + R_{fs} + g_{m0} R_{DS}\left(R_{fs} - R_{fp}\right) \right|}. \tag{3.45}$$



(a) (b)

Fig. 3-25: (a) MAG and (b) Rollett´s stability factor k vs. R_{fp} and R_{fs} of a FBPA at DC with a 8×125um HEMT

Fig. 3-25 illustrates in (a) the dependency of the MAG on R_{fp} and R_{fs} and (b) the corrresponding stability factor k for a 8×125um HEMT. It is worth mentioning that in this special case of no reactive elements, the resistive parallel- and series-feedback always leads to an unconditionally stable behavior of the PA. By taking a look at (b) it can be observed that with decreasing amount of feedback, the k-factor converges to the limit of $k = 1$. As a result, the MSG is only existent for the single point of $R_{fp} = \infty$ and $R_{fs} = 0$ at DC. Looking at the MAG in (a) reveals that the highest sensitivity is located in the region for small values of R_{fp}, where for increasing R_{fs} the drop in gain is more significant than for large R_{fp}. This is based on the fact that the smaller the effective g_{m0} including the parallel feedback is the larger is the impact of R_{fs} on the gain.

3.3.2 Noise Analysis of FBPAs

As has been reported in several publications over the last decades, using feedback provides superior performance in terms of noise among all kind of amplifier topologies. Especially in narrow-band applications enables the use of inductive series feedback the implementation of high performance LNAs, where noise matching and gain/power matching can be achieved simultanesouly for one single frequency [84, 85]. For the design of broadband amplifiers down to DC this well-known reactive matching concept can not be applied. Therefore, frequency independent elements such as resistors have to be used in order to realize a good noise match over a wide frequency range. Towards DC it is furthermore crucial to make use of series as well as parallel feedback in order to realize a sufficiently good input/output match, as already presented in section 3.2. Unfortunately by using resistive components in the feedback paths additional noise will be introduced. In the following only thermal noise will be considered, since knowledge about the $1/f$-noise characteristics of the utilized GaN25 technology is not available. This section investigates the dependency of the thermal noise on the resistive feedback elements to find the optimum values for a broadband low-noise FBPA design.

The core of the noise analysis in this section relies on the noise correlation matrix (NCM) method presented by H. Hillbrand and P. Russer in [67], which is also described briefly in the Appendix B.1. Similar to the procedure for the intrinsic HEMT noise characteristics, this section investigates the impact of the parallel and series feedback resistors on the noise performance. For simple noise computations the NCM method might not be the easiest and fastest approach due to the necessary parameter conversions, but its general validity enables the designer to compute even the most complex systems in a systematic way by making use of fast computer calculations, as e.g. in MATLAB.

The overall noise correlation matrix (NCM) of a HEMT with parallel feedback can be expressed in Y-parameter form and can be written to

$$\vec{\vec{C}}_{Y,Tfp} = \vec{\vec{C}}_{Y,T} + \vec{\vec{C}}_{Y,Rfp}, \tag{3.46}$$

where $\vec{\vec{C}}_{Y,T}$ and $\vec{\vec{C}}_{Y,Rfp}$ stand for the NCM of the HEMT and the parallel feedback network, respectively. Similarly, for series feedback the Z-parameter form of the NCM can be utilized and the total NCM of the HEMT including resistive feedback becomes equal to

$$\vec{\vec{C}}_{Z,Tfs} = \vec{\vec{C}}_{Z,T} + \vec{\vec{C}}_{Z,Rfs}. \tag{3.47}$$

Final transformation of the NCM into chain-parameter representation yields the equivalent input referred noise current and voltage representation from which the four noise parameters can be computed according to Appendix B.1. This gives according to the general transformation rule of $\vec{\vec{C}}' = \vec{\vec{T}} \cdot \vec{\vec{C}} \cdot \vec{\vec{T}}^{+}$ for the parallel feedback network

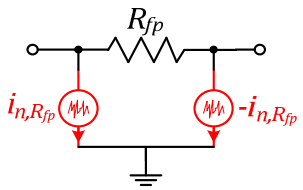
$$\vec{\vec{C}}_{A,Tfp} = \begin{bmatrix} 0 & B \\ 1 & D \end{bmatrix} \cdot \vec{\vec{C}}_{Y,Tfp} \cdot \begin{bmatrix} 0 & 1 \\ B^* & D^* \end{bmatrix} \tag{3.48}$$

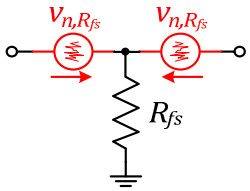
and for the series feedback

$$\overleftrightarrow{C}_{A,Tfs} = \begin{bmatrix} 1 & -A \\ 0 & -C \end{bmatrix} \cdot \overleftrightarrow{C}_{Z,Tfs} \cdot \begin{bmatrix} 1 & 0 \\ (-A)^* & (-C)^* \end{bmatrix}. \tag{3.49}$$

If both feedback networks are present, the NCMs need to be converted between Y- and Z-parameter form before final computation of the NCM in $ABCD$-parameter form, which can be achieved by either setting $\overleftrightarrow{T} = \overleftrightarrow{Y}$ for NCM conversion from Z- to Y-parameters or $\overleftrightarrow{T} = \overleftrightarrow{Z}$ from Y- to Z-parameter conversion. The needed ABCD-parameters in (3.48) and (3.49) of the whole network can then be computed in a final step from either Y- or Z-parameters by (3.50), as derived in [72].

$$\overrightarrow{ABCD} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} -\frac{Y_{22}}{Y_{21}} & -\frac{1}{Y_{21}} \\ \frac{Y_{12}Y_{21} - Y_{11}Y_{22}}{Y_{21}} & -\frac{Y_{11}}{Y_{21}} \end{bmatrix} = \begin{bmatrix} \frac{Z_{11}}{Z_{21}} & \frac{Z_{11}Z_{22} - Z_{12}Z_{21}}{Z_{21}} \\ \frac{1}{Z_{21}} & \frac{Z_{22}}{Z_{21}} \end{bmatrix} \tag{3.50}$$





$$\overleftrightarrow{C}_{Y,Rfp} = 4kT \begin{bmatrix} \frac{1}{R_{fp}} & \frac{-1}{R_{fp}} \\ \frac{-1}{R_{fp}} & \frac{1}{R_{fp}} \end{bmatrix}$$

(a)

$$\overleftrightarrow{C}_{Z,Rfs} = 4kT \begin{bmatrix} R_{fs} & R_{fs} \\ R_{fs} & R_{fs} \end{bmatrix}$$

(b)

Fig. 3-26: (a) parallel and (b) series resistive-feedback and its corresponding noise representation

Under the simplifying but valid assumption of a unilateral device up to moderate frequencies, Pucel´s noise model from Fig. 2-9 can be taken for a first noise estimation. Since R_{GS} does not introduce any additional thermal noise and is in general comparably small, it is out of simplicity reasons furthermore neglected. Following the NCM procedure gives for the parallel resistive feedback and series resistive feedback the following two equivalent noise representations, as depicted in Fig. 3-26 (a) and (b). It is important to note that the direction of the noise current and voltage sources has to be chosen equally in the HEMT noise model as well. According to (3.46) and (3.47) the corresponding NCMs of the HEMT with parallel and series resistive feedback thus result in (3.51) and (3.52) with (3.53), respectively.

$$\overleftrightarrow{C}_{Y,Tfp} = \begin{bmatrix} \left|i_{n,\mathrm{G}}\right|^2 + \dfrac{4kT}{R_{fp}} & -\underline{c}^* \cdot \sqrt{\left|i_{n,\mathrm{G}}\right|^2 \left|i_{n,\mathrm{D}}\right|^2} - \dfrac{4k_B T}{R_{fp}} \\ -\underline{c} \cdot \sqrt{\left|i_{n,\mathrm{G}}\right|^2 \left|i_{n,\mathrm{D}}\right|^2} - \dfrac{4k_B T}{R_{fp}} & \left|i_{n,\mathrm{D}}\right|^2 + \dfrac{4k_B T}{R_{fp}} \end{bmatrix} \tag{3.51}$$

$$\overleftrightarrow{C}_{Z,Tfs} = \begin{bmatrix} C_{Z11,Tfs} & C_{Z12,Tfs} \\ C_{Z21,Tfs} & C_{Z22,Tfs} \end{bmatrix} \tag{3.52}$$

$$\begin{aligned} C_{Z11,Tfs} &= \frac{\left|i_{n,\mathrm{G}}\right|^2}{(\omega C_{GS})^2} + 4k_B T R_{fs} \\ \overleftrightarrow{C}_{Z12,Tfs} &= -R_{DS}\left(\frac{\left|i_{n,\mathrm{G}}\right|^2 g_m}{(\omega C_{GS})^2} + \frac{\underline{c}^*}{j\omega C_{GS}} \cdot \sqrt{\left|i_{n,\mathrm{G}}\right|^2 \left|i_{n,\mathrm{D}}\right|^2}\right) + 4k_B T R_{fs} \\ C_{Z21,Tfs} &= {C_{Z12,Tfs}}^* \\ C_{Z22,Tfs} &= {R_{DS}}^2\left(\frac{\left|i_{n,\mathrm{G}}\right|^2 {g_m}^2}{(\omega C_{GS})^2} + \left|i_{n,\mathrm{D}}\right|^2 - 2\frac{g_m}{\omega C_{GS}} Im\{\underline{c}\}\sqrt{\left|i_{n,\mathrm{G}}\right|^2 \left|i_{n,\mathrm{D}}\right|^2}\right) + 4k_B T R_{fs} \end{aligned} \tag{3.53}$$

From (3.48) - (3.50) it becomes evident that only Z_{11} and Z_{21}, respectively Y_{11} and Y_{21}, are necessary to compute the needed $ABCD$-parameters for the final NCM in chain-parameter representation. The needed chain parameters result for the simplified HEMT with parallel (3.54) and series (3.55) resistive feedback in

$$B_{Tfp} = \frac{R_{fp}}{1 - g_m R_{fp}}, \qquad D_{Tfp} = \frac{1 + j\omega C_{GS} R_{fp}}{1 - g_m R_{fp}} \tag{3.54}$$

$$A_{Tfs} = \frac{1 + j\omega C_{GS} R_{fs}}{j\omega C_{GS} R_{fs} - g_m R_{DS}}, \qquad C_{Tfs} = \frac{j\omega C_{GS}}{j\omega C_{GS} R_{fs} - g_m R_{DS}}. \tag{3.55}$$

Final insertion of (3.54)-(3.55) into (3.48) and (3.49) gives for the final NCM in chain-parameter representation

$$\begin{aligned} \frac{C_{A11,Tfp}}{4k_B T} &= \left(\frac{R_{fp}}{1 - g_m R_{fp}}\right)^2 \left(g_m P + \frac{1}{R_{fp}}\right) \\ \frac{C_{A12,Tfp}}{4k_B T} &= \frac{R_{fp}}{1 - g_m R_{fp}}\left(\frac{1 - j\omega C_{GS} R_{fp}}{1 - g_m R_{fp}}\left(\frac{1}{R_{fp}} + g_m P\right) - \left(\underline{c} \cdot \omega C_{GS}\sqrt{RP} + \frac{1}{R_{fp}}\right)\right) \\ C_{A21,Tfp} &= {C_{A12,Tfp}}^* \end{aligned} \tag{3.56}$$

$$\frac{C_{A22,Tfp}}{4k_BT} = \frac{1}{R_{fp}} + \frac{(\omega C_{GS})^2}{g_m} R + \frac{1+\left(\omega C_{GS} R_{fp}\right)^2}{\left(1-g_m R_{fp}\right)^2}\left(\frac{1}{R_{fp}} + g_m P\right)$$
$$- 2 \cdot Re\left\{\frac{1+j\omega C_{GS} R_{fp}}{1-g_m R_{fp}}\left(\underline{c} \cdot \omega C_{GS}\sqrt{RP} + \frac{1}{R_{fp}}\right)\right\}$$

for the parallel resistive feedback and

$$\frac{C_{A11,Tfs}}{4k_BT} = \frac{R}{g_m} + R_{fs}$$
$$+ \frac{1+\left(\omega C_{GS} R_{fs}\right)^2}{\left(\omega C_{GS} R_{fs}\right)^2 + (g_m R_{DS})^2}\left(R_{fs} + g_m {R_{DS}}^2\left(R + P - 2 \cdot Im\{\underline{c}\}\sqrt{RP}\right)\right)$$
$$+ 2 \cdot Re\left\{\frac{1+j\omega C_{GS} R_{fs}}{j\omega C_{GS} R_{fs} - g_m R_{\mathrm{DS}}}\left(R_{fs} + R_{DS}\left(R + \underline{c} \cdot j\sqrt{RP}\right)\right)\right\}$$

$$\frac{C_{A12,Tfs}}{4k_BT} = \frac{\omega C_{GS}\left(\omega C_{GS} R_{fs} + j g_m R_{DS}\right)}{(g_m R_{DS})^2 + \left(\omega C_{GS} R_{fs}\right)^2}\left(\frac{1+j\omega C_{GS} R_{fs}}{j\omega C_{GS} R_{fs} - g_m R_{\mathrm{DS}}} \cdot \ldots\right. \tag{3.57}$$
$$\left. \ldots\left(R_{fs} + g_m {R_{DS}}^2\left(R + P - 2 \cdot Im\{\underline{c}\}\sqrt{RP}\right)\right) + R_{fs} + R_{DS}\left(R - \underline{c}^* \cdot j\sqrt{RP}\right)\right)$$

$$C_{A21,Tfs} = {C_{A12,Tfs}}^*$$

$$\frac{C_{A22,Tfs}}{4k_BT} = \frac{(\omega C_{GS})^2}{(g_m R_{DS})^2 + \left(\omega C_{GS} R_{fs}\right)^2}\left(g_m {R_{DS}}^2\left(R + P - 2 \cdot Im\{\underline{c}\}\sqrt{RP}\right) + R_{fs}\right)$$

for the series resistive feedback. The correlation coefficient $\underline{c}$ in (3.56) and (3.57) refers to the correlation between the noise current sources according to Pucel´s model. By means of the just derived NCM parameters $C_{A11,Tfp}$, $C_{A22,Tfp}$ and $C_{A11,Tfs}$, $C_{A22,Tfs}$ the dependency of the overall noise characteristic of the parallel and series feedback amplifier on the magnitude of R_{fp} and R_{fs} can be deduced without moving to further complicated expressions for the four noise parameters. Assuming that the FBPA is driven by a low source resistance, the input referred noise voltage source is dominant and thus C_{A11} describes solely the noise characteristics of the amplifier, whereas for high source resistances C_{A22} contains most of the important noise information. The specific dependency of $C_{A11,Tfp}$ and $C_{A22,Tfp}$ on R_{fp} as well as $C_{A11,Tfs}$ and $C_{A22,Tfs}$ on R_{fs} for a 8×125µm HEMT is plotted in Fig. 3-27 below. Pucel´s noise parameters P and R are assumed to be equal to 1.5 and 0.7 for the typical bias point of V_{DS} = 28 V and I_{DS} = 200 mA/mm here, but any other values only affect the overall magnitude but not the dependence on the feedback values R_{fp} or R_{fs}. Clearly observable from (a) and also (3.56) is that the effective input referred $NVSD$ caused by R_{fp} is independent of frequency and exhibits only a minor contribution for values larger than 100 Ω. Since for proper I/O-matching R_{fp} needs to be at least in the order of magnitude of 150 Ω (see chapter 3.2.1), the parallel feedback shows only negligible contribution for low source

impedances. For high source impedances in contrast a slight frequency dependence of the $NCSD$ becomes visible in (b) for $C_{A22,Tfp}$, but with a similar characteristic as $C_{A11,Tfp}$ for values larger than 100 Ω.

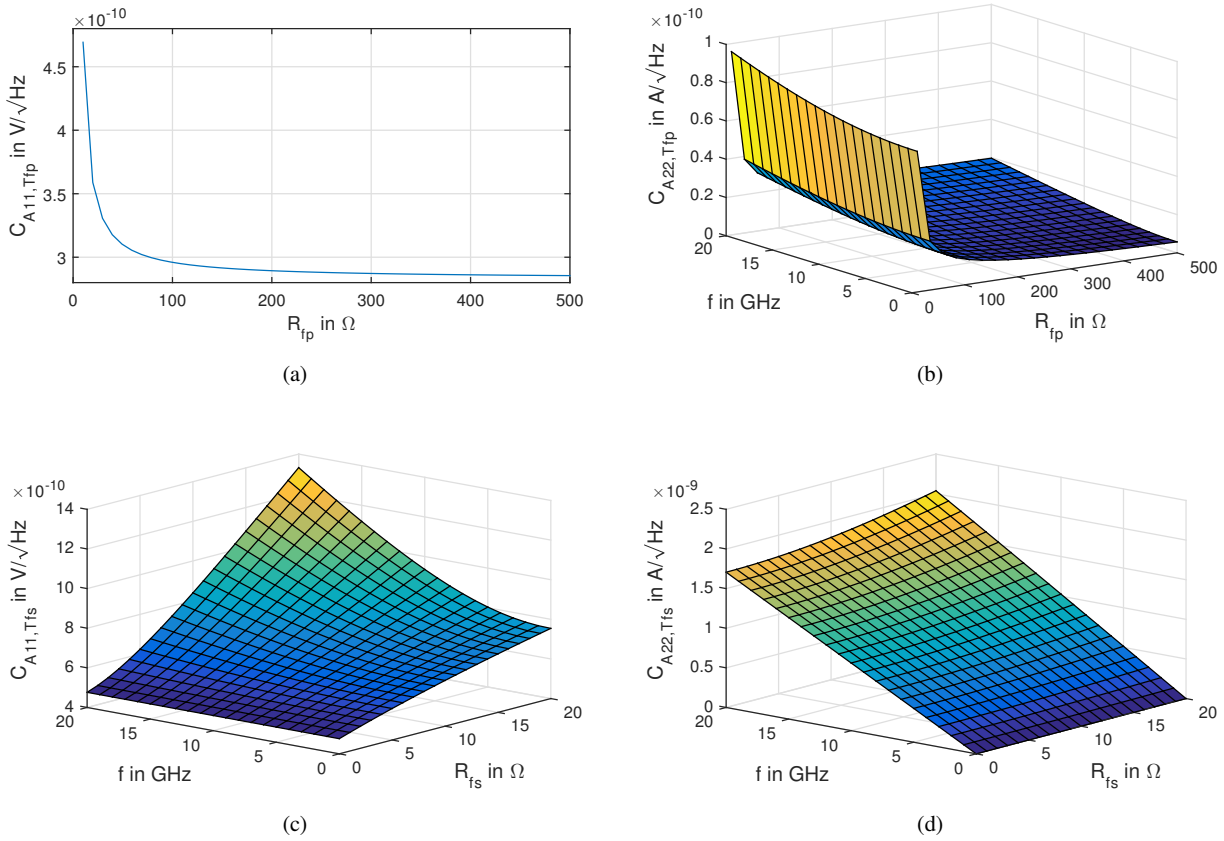


Fig. 3-27: Dependency of (a) $C_{A11,Tfp}$ on R_{fp}, (b) $C_{A22,Tfp}$ on R_{fp} and f, (c) $C_{A11,Tfs}$ on R_{fs} and f and (d) $C_{A22,Tfs}$ on R_{fs} and f for a 8×125µm HEMT

The input referred $NVSD$ and $NCSD$ in case of resistive feedback possesses a much stronger dependency on R_{fs} as well as on frequency, as (c) and (d) illustrate. Additionally, the overall amount of noise contribution coming from R_{fs} is already much larger than from R_{fp}. Consequently, series feedback leads to a much faster degradation of the FBPA´s NF than parallel feedback. At this poinnt of the analysis it can be already stated that it is thus beneficial for a low noise design to keep R_{fs} as small as possible and to control the amount of desired feedback via the parallel feedback resistor, still under consideration of adequate I/O-matching, as discussed in section 3.2.1. By even further simplifying the NCM matrices from (3.56) and (3.57) for the DC case (ω = 0), the oversimplified NCMs in (3.58)-(3.59) can now even serve to compute the four noise parameters.

$$\frac{\overleftrightarrow{C}_{A,Tfp}}{4k_BT} = \frac{1}{\left(1-g_mR_{fp}\right)^2}\begin{bmatrix} R_{fp}\left(1+g_mPR_{fp}\right) & g_mR_{fp}(P+1) \\ g_mR_{fp}(P+1) & g_m\left(P+g_mR_{fp}\right) \end{bmatrix} \tag{3.58}$$

$$\frac{\overleftrightarrow{C}_{A,Tfs}}{4k_BT} = \begin{bmatrix} \frac{P}{g_m} + R_{fs}\left(1 + \frac{1 - 2g_mR_{\mathrm{DS}}}{(g_mR_{\mathrm{DS}})^2}\right) & 0 \\ 0 & 0 \end{bmatrix} \tag{3.59}$$

From (3.58) the four noise parameters of the parallel feedback hence result at DC in

$$F_{Tfp} = 1 + \frac{\frac{R_{fp}}{R_S}\left(1 + g_mPR_{fp}\right) + 2g_mR_{fp}(P+1) + g_mR_S\left(P + g_mR_{fp}\right)}{\left(1 - g_mR_{fp}\right)^2} \tag{3.60}$$

$$F_{min,Tfp} = 1 + 2 \cdot \frac{\sqrt{g_mR_{fp}\left(1 + g_mPR_{fp}\right)\left(P + g_mR_{fp}\right)} + g_mR_{fp}(P+1)}{\left(1 - g_mR_{fp}\right)^2} \tag{3.61}$$

$$Y_{opt,Tfp} = \frac{1}{R_{fp}}\sqrt{1 + \frac{\left(g_mR_{fp}\right)^2}{1 + g_mPR_{fp}}} \tag{3.62}$$

$$R_{n,Tfp} = R_{fp}\frac{1 + g_mPR_{fp}}{\left(1 - g_mR_{fp}\right)^2} \tag{3.63}$$

and accordingly for the series feedback from (**3.59**) in

$$F_{Tfs} = 1 + \frac{1}{R_S}\left[\frac{P}{g_m} + R_{fs}\left(1 + \frac{1 - 2g_mR_{\mathrm{DS}}}{(g_mR_{\mathrm{DS}})^2}\right)\right] \tag{3.64}$$

$$F_{min,Tfs} = 1 \tag{3.65}$$

$$Y_{opt,Tfs} = 0 \tag{3.66}$$

$$R_{n,Tfs} = \frac{P}{g_m} + R_{fs}\left(1 + \frac{1 - 2g_mR_{\mathrm{DS}}}{(g_mR_{\mathrm{DS}})^2}\right). \tag{3.67}$$

As equation (3.60) for the DC case shows, the noise factor of the parallel feedback HEMT tends for $R_{fp} \to \infty\ \Omega$ to

$$F_{Tfp} = 1 + P/(g_mR_S), \tag{3.68}$$

which is equal to $R_{fs} \to 0\ \Omega$ for the series feedback in (3.64), representing the noise factor of the HEMT's channel-noise alone. For $R_{fp} \to 0\ \Omega$ in contrast, F_{Tfp} strives toward the constant value of

$$F_{Tfp} = 1 + g_m P R_S, \tag{3.69}$$

after exhibiting a pole ($F_{Tfp} = \infty$) for $R_{fp} = 1/g_m$. For $R_{fs} \to \infty\ \Omega$ in contrast, the noise factor F_{Tfs} tends continuously to infinity.

After the investigation of the general low frequency noise dependencies for the series and parallel feedback amplifiers separately, both feedback concepts are now applied together to identify the optimum values of R_{fp} and R_{fs} for retaining low noise performance. Since any difference in gain would cause variations in the NF and thus do not allow for a meaningful comparison in the noise analysis, the parallel and series feedback resistor values of R_{fp} and R_{fs} are somehow dependent on each other, as already presented in section 3.2.1 and defined by (3.22). It is now possible to derive the optimum values for R_{fs} and R_{fp}, which give optimum noise performance at a fixed gain of 10 dB and at the same time an I/O-RL of better than 10 dB. The computations are conducted again for a 8×125um HEMT with P = 1.5, R = 0.7 and c = -j0.8 and are based on the frequency dependent NCMs from (3.56) and (3.57). Furthermore, the four noise parameters are only plotted against R_{fp} in Fig. 3-28, since R_{fs} is coupled to R_{fp} by the 10 dB value sets defined by the small-signal matching in 3.2.1. All the computations were done in Matlab, since the equations for the NCM with both feedbacks are very complex and thus very prone to errors for hand calculations.

(Remark: The matching performance at higher frequencies will differ from the computed values due to the reactive elements of the HEMT. Since only DC-matching is considered here for the computation of the R_{fp} and R_{fs} value set, decreasing R_{fs} will not only improve F_{min} at high frequencies but alter the matching performance as well!).

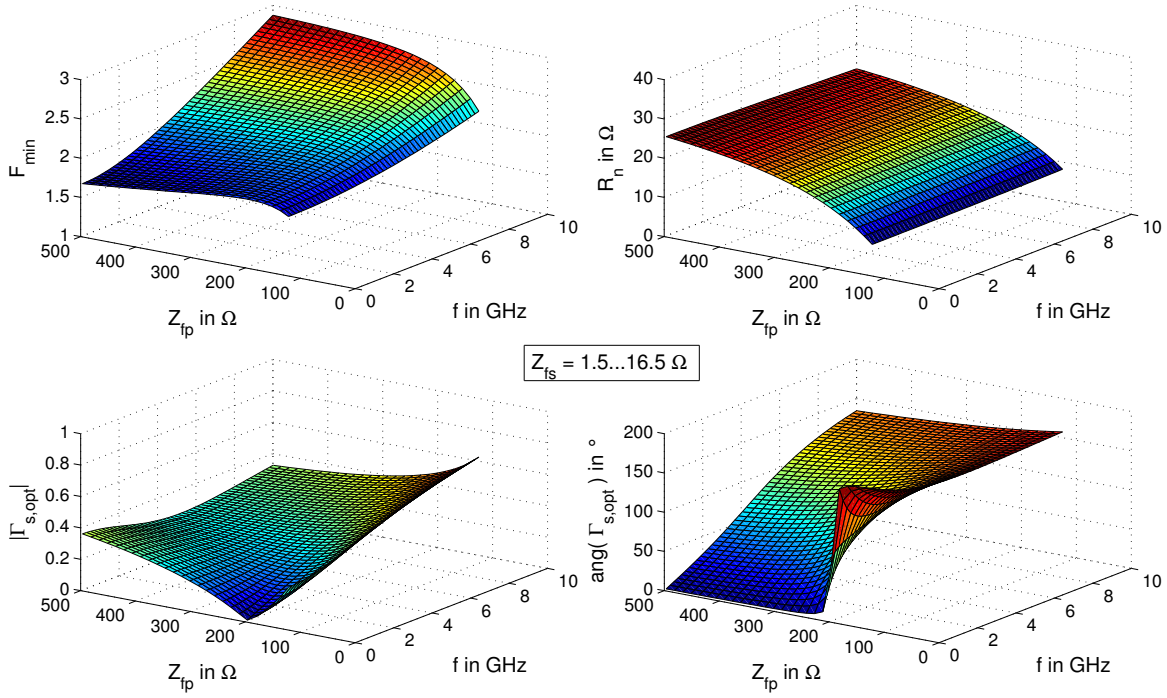


Fig. 3-28: F_{min}, R_n, $|\Gamma_{s,opt}|$ and $\measuredangle(\Gamma_{s,opt})$ vs. f and vs. R_{fp} for S_{21}= 10 dB (R_{fs} = 1.5…16.5 Ω) of an 8×125µm HEMT applying parallel and series feedback

As can be seen from Fig. 3-28 above, F_{min} shows a stronger frequency dependence for larger R_{fp} and therewith also for larger R_{fs} values than for smaller ones. This leads to the conclusion that with increasing amount of series feedback the frequency dependence of F_{min} rises, as already indicated by $C_{A11,Tfs}$ and $C_{A22,Tfs}$ in Fig. 3-27 (c) and (d). Dependent on the targeted BW of the design, it might be beneficial in terms of a flat noise performance to either choose large values for R_{fp} and R_{fs} for applications with an upper frequency of only a few GHz or small values for R_{fp} and R_{fs} for applications reaching up to several GHz. It needs to be furthermore kept in mind that large values for R_{fp} and R_{fs} lead to a higher effective noise resistance R_n, which increases the sensitivity of the FBPA´s NF to input matching deviations, as can be seen in Fig. 3-28. From the two $\Gamma_{s,opt}$ plots it can be further deduced that for feedback values of $R_{fp} \approx 200\ \Omega$ the optimum noise match for obtaing F_{min} comes close to 50 Ω at low frequencies.

3.3.3 FBPA Design Criteria

As presented in chapter 3.2, realizing good small-signal matching, high output power, high linearity and low noise at the same time can only be met by making trade-offs and performance sacrifices. In the case of FBPAs, the design procedure is unfortunately not as straightforward as it is for narrow-band PA designs. Dependent on the operational frequency, the often used valid approximation of $S_{12} \approx 0$ in narrow-band designs simplifies the design process, because the input and output matching network (IMN/OMN) can be designed separately and almost independent of each other. Starting from a mathematically synthesized MN leads very quickly to a proper result without time consuming tuning of the MNs. In the case of FBPAs, where S_{12} is of noticeable magnitude due to the feedback, the IMN and OMN design cannot be separated due to the resulting bilateral amplifier. This complicates the determination of the starting MN component values and makes an iterative approach unavoidable.

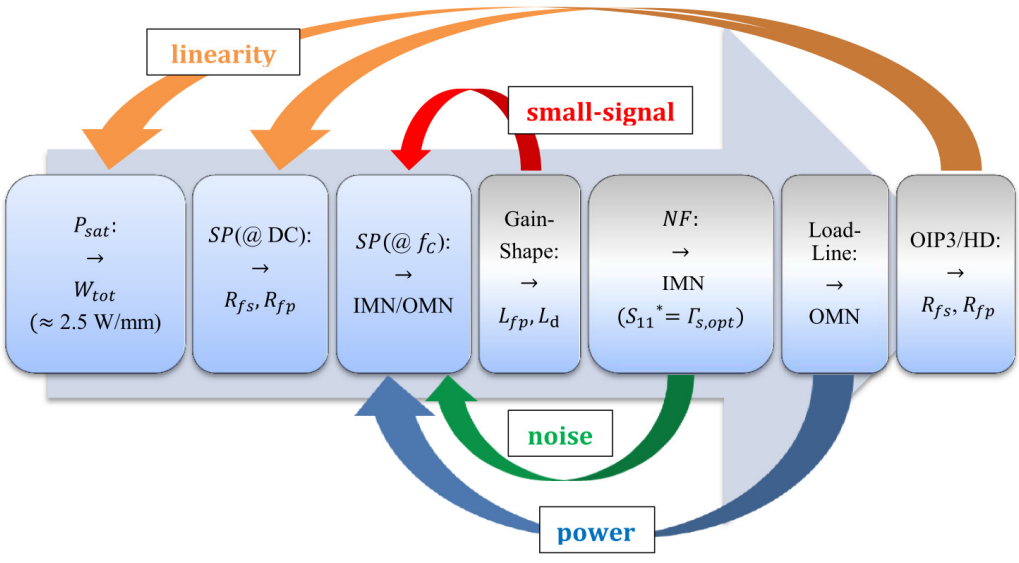


Fig. 3-29: Flow-chart for FBPA design guidelines

The flow-chart in Fig. 3-29 presents an iterative guideline for the design of a FBPA, comprising parallel- as well as series-feedback. Depending on whether small-signal matching, power, linearity or noise is the most critical parameter given in the specifications, the other parameters have to be always traded-off for the key parameter. The optimization process for the targeted key parameter is indicated by the corresponding colored arrow in Fig. 3-29, forming iteration loops. The last four action items can be skipped independently, if their corresponding parameters are not of major concern. In case all four parameters are of equal importance a meaningful trade-off by successive approximation has to be found.

Recommended Design Procedure

1. Selection of the proper device size (W_{tot}) to obtain the specified maximum output power (P_{sat}). (Recommendation: A rule-of-thumb for 0.25µm GaN FBPAs is around 2.5 W/mm for broadband PAs as a reasonable starting value).
2. Determination of the parallel- and series-feedback resistors based on the DC/low-frequency specifications for small-signal gain (S_{21}) and input/output matching (S_{11}/S_{22}), as described in section 3.2.1 in equations (3.22), (3.24) and (3.25).
3. Initial calculation of the complex conjugate input ($Z_{IN}{}^{*}$) and output ($Z_{OUT}{}^{*}$) impedances at the targeted upper band edge in order to retain starting values for a proper small-signal match at f_c. (Remark: Dependent on the bandwidth and required matching, the number of MN-stages has to be selected wisely).
4. Gain shape trimming by means of either a series feedback inductor (L_{fp}) or/and by an inductor (L_d) connected to the drain of the power HEMT. Both approaches help to reduce the feedback toward the band edge and thus boost gain if desired. (Remark: This step has to be done at an early stage, since IMN and OMN are very dependent on the parallel feedback elements).
5. If step 4 is applied, again tuning of the IMN and OMN from step 3 is crucial to maintain the desired small-signal matching.
6. Tuning of the IMN until $S_{11}{}^{*}$ features a trajectory close to $\Gamma_{s,opt}$ in the smith-chart. If minimum noise is the key parameter, this step has to be done at an early stage and prior to the OM design, since only the IM ascertains low noise performance.
7. If step 6 is applied, again tuning of the OMN from step 3 is crucial to maintain the specified output matching.
8. Tuning of the HEMT´s load-line by adapting the OMN values or number of MN stages. Dependent on the bandwidth requirements an additional MN stage might reduce the opening of the load-line over frequency and even improve the small-signal matching. (The introduction of an additional zero leads to a twist in the load-line, which minimizes the generation of idle power in the HEMT).
9. If step 8 is applied, again tuning of the IMN from step 3 is crucial to maintain the specified input matching.
10. Examination of the resulting linearity performance (e.g. $HD, OIP3$). If the linearity specifications are met the design is completed. If not, either chosing a larger device or changing the amount of feedback might help to improve linearity.

3.3.4 DC - 6 GHz Feedback PA Design

The following section presents the design of a high linear and low noise DC - 6 GHz HPA with a targeted P_{sat} of 35 dBm. Due to the given linearity specifications from Table 1-1 and also out of gain flatness and bandwidth reasons, the feedback topology is very well suited, enabling also low frequency operation down to DC in general. Frequencies below a few hundred MHz can only be achieved when external SMD capacitors (C_{ext}) areused, as sketched in the general schematic of the FBPA in Fig. 3-30 below.

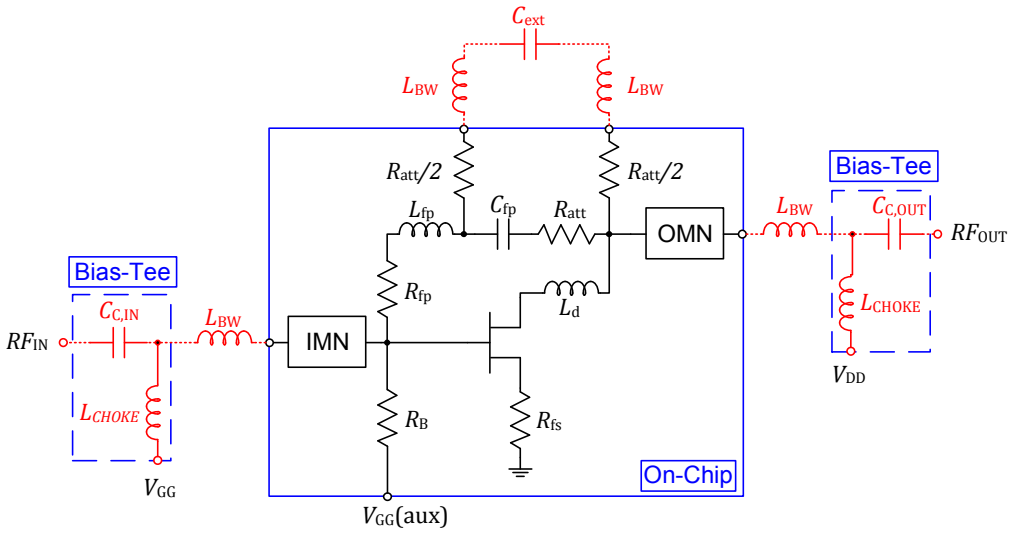
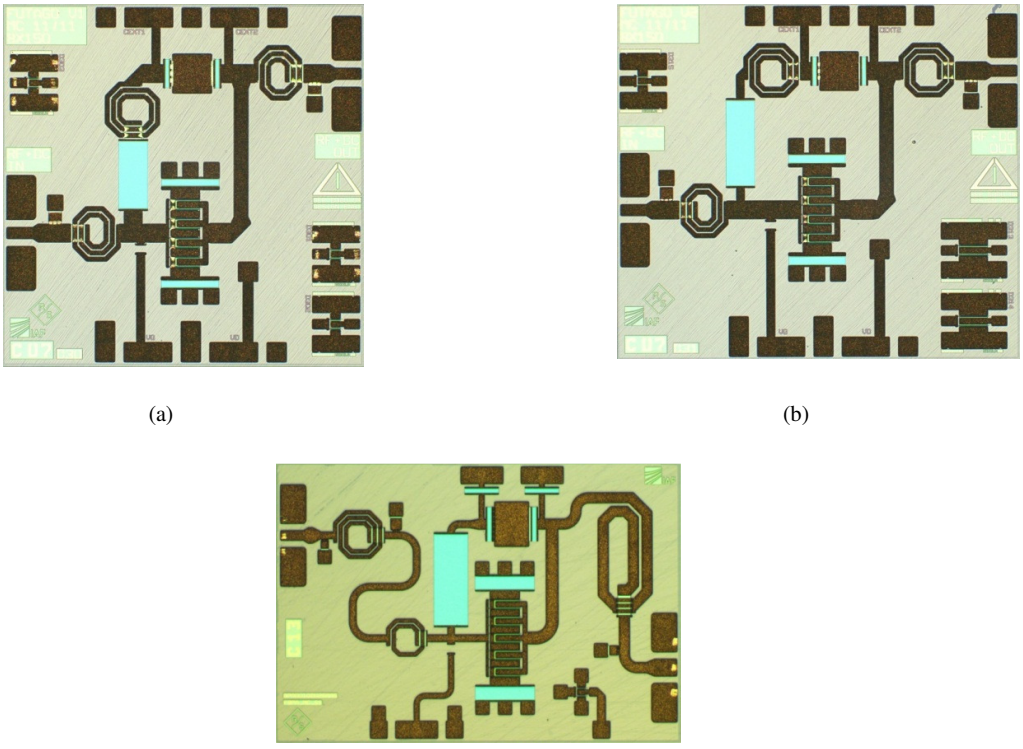


Fig. 3-30: Schematic of FBPA applying series and parallel resistive feedback with off-chip low frequency extension and external bias-tees

Series feedback cannot be omitted to boost output power, since it is cruicial to obtain a reasonable S_{11}input match, as presented in section 3.2.1. Also the slight increase in NF due to R_{fs}, which was analyzed in the previous chapter 3.3.2, cannot be avoided in terms of proper input matching. Since R_{fs} is deliberately chosen small to only 4-5 Ω, the corresponding degradation in output power and NF is kept relatively small. The input matching network (IMN) and output-matching-network (OMN) were in the first designs simple one-stage L-section filters in order to realize an I/O-RL of better than 10 dB over the whole bandwidth. The two initial versions (a) and (b) depicted in Fig. 3-31 are matched for different BWs, because the accuracy of the models and the process variations were completely unknown for the utilized GaN technology for the first design. After first in package measurements with an external 1µF SMD capacitor in the parallel feedback path, the designs proved to be prone to arsinig oscillations at the upper frequency band. The reason for this was the LC-resonance circuit generated by C_{fp} and the bond-wires L_{BW}, connecting C_{ext} off-chip. One approach is to chose the constant $L_{BW}C_{fp}$ in such a way, that f_{res} falls out of band (f_{res} > 6.5 GHz). C_{fp} has to be thus designed sufficiently small, since L_{BW} is limited by manufacturing tolerances and cannot be made arbitrarily small. This leads to the problem of nonoverlapping frequency ranges for the on-chip and off-chip capacitor, since the 1µF SMD capacitor exhibits a self-resonance frequency (SFR), where the on-chip capacitor is still too high-impedance. Consequently, the effective impedance in the parallel feedback path is altered, which in turn manifests in a kink in the S-parameter around the SRF of the SMD capacitor. The other more efficient solution is to simply add a few Ohms of attenuation resistance (R_{att}) on chip to decrease the Q of the resonance circuit and therewith damp possible arising

oscillations within the band. It has to be considered that the additional resistance has to be of equal size on-chip and on the external PCB. Otherwise a small kink in the gain will become visible based on the difference in overall feedback resistance $R_{fp} + R_{att}$. Moreover, the position of R_{att} on chip is of vital importance. Placement of R_{att} in front of the right C_{ext} bonding pad leads to additional loading of the FBPA´s output by a series RC-low pass filter. This filter is formed by R_{att} and the parasitic footprint pad capacitance of the external SMD capacitor C_{ext}. Therefore, placement of R_{att} in front of the left C_{ext} bonding pad only, as depicted in Fig. 3-31 (c), does have the same damping effect on the external resonance loop but not any effect on the ouput loading. Solely the feedback is affected slightly, which decreases anyway with increasing frequency and is thus not noticeable at the upper band edge.



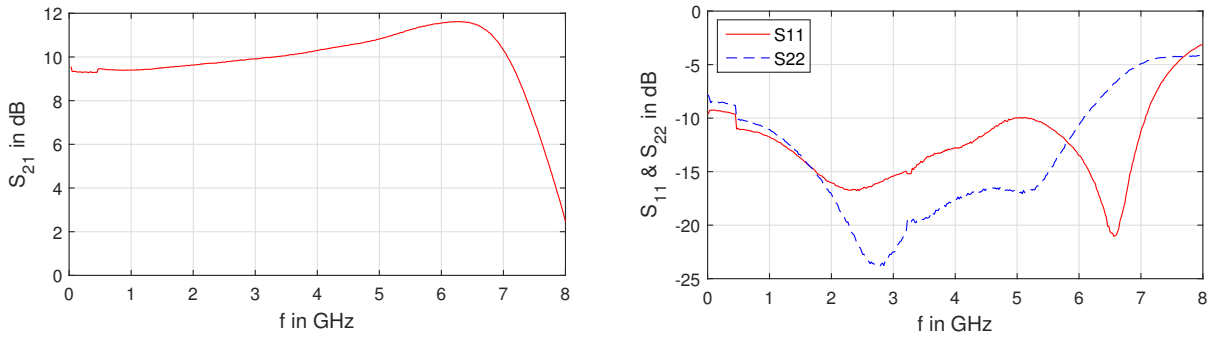
(a) (b)

(c)

Fig. 3-31: Photograph of DC-6 GHz Feedback MMICs (a) “Futago V1”, (b) “Futago V2” and (c) “Futago V3”

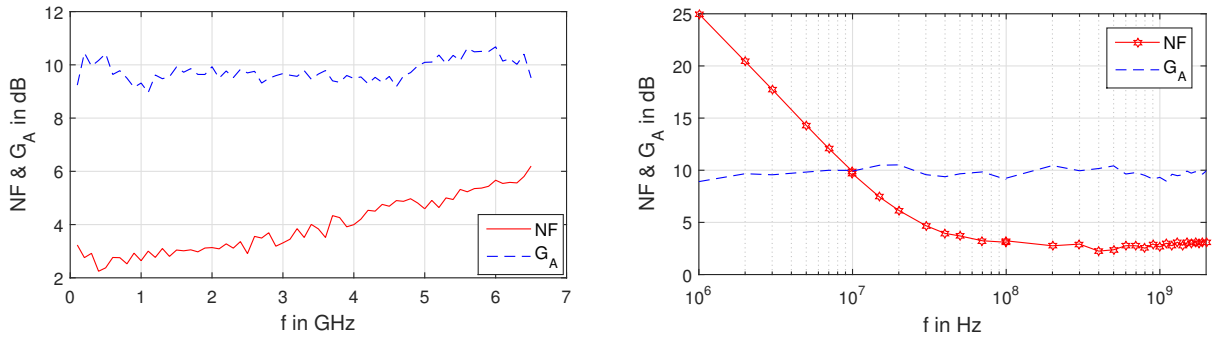
The third and final version of the DC–6 GHz FBPA “Futago V3” is depicted in Fig. 3-31. After the experience of the first two chip designs, the 8×150µm HEMT (W_G = 1.2 mm) was replaced by a 10×175µm HEMT (W_G = 1.75 mm) to further boost the output power in package above 35 dBm, which could not be achieved with the 8×150um HEMT in the first two versions in Fig. 3-31 (a) and (b). Unfortunately, this comes at the cost of slightly worse I/O-matching. Part of the degraded matching was compensated by making use of a 2-stage IMN, giving a second notch in the S_{11} and improving the *I*-RL back below 10 dB, as shown in Fig. 3-32 (b). The small kink at 500 MHz is owed to the two different measurement setups, which are necessary to characterize the small-signal performance down to 10 MHz. Worth mentioning in terms of output machting is the necessity for an external drain biasing in such broadband FBPAs down to DC. Opposed to narrow-band designs, where the resonance frequency of the on-chip biasing structure (usually RF-chokes) can be designed to lie below the band

of interest, multi-decade FBPAs operating down to DC cannot make use of such purely reactive on-chip bias topologies. Because of this reason the drain bias needs to be fed via the output of the FBPA, which causes another design problem. The need for an off-chip drain biasing, increases the current through the OMN. In order not to restrict the life-time or reliability of the FBPA caused by electromigration failures, the MSLs and coils in the OMN need to be wide enough to handle the total amount of DC plus RF current. Moreover, the maximum current handling capability of the coils and MSLs in the output matching network (OMN) is especially for frequencies below a few MHz significantly reduced due to the increased thermal triggering of electromigration. The MSLs and coils have to be therewith dimensioned sufficiently wide to handle also the DC current, which affects in turn the SRF of the matching coils and makes a decent matching of the output of the HEMT to 50 Ω at high frequencies much more challenging.



(a) (b)

Fig. 3-32: Measured (a) S_{21} and (b) S_{11} and S_{22} of the DC-6 GHz FBPA "Futago_V3" in package at V_{DS} = 28 V and I_{DS} = 200 mA/mm



(a) (b)

Fig. 3-33: Measured NF and G_A for (a) 1-6 GHz and (b) 10 MHz - 2 GHz of the DC-6 GHz FBPA "Futago_V3" in package at V_{DS} = 28 V and I_{DS} = 200 mA/mm

Since for the application in a SG the NF of the FBPA is also an important FoM, NF measurements over the whole frequency range were conducted and are depicted in Fig. 3-33 for (a) above 1 GHz and (b) below 1 GHz. The minimum in NF was determined to 2.7-3.0 dB at around 1 GHz and clearly visible is the typcial flat noise behavior towards 100 MHz, which is beneficial in feedback based topologies. Over the frequency range from 30 MHz to almost 5.5 GHz stays the NF below 5 dB. Below 100 MHz the NF starts to rise again, which is deemed to be caused by the $1/f$ noise of the HEMTs on the one hand and by the resistive gate-bias on the other

hand. The exact $1/f$ noise corner frequency of the utilized process is not known, but the present actual measurements indicate that it lies below 50 MHz. This is in accordance with reported GaN HEMT $1/f$ noise corner frequencies from the literature, which are in the order of 1 – 10 MHz [86].

As already mentioned, the increase in device size from W_G = 1.2 mm to W_G = 1.75 mm in order to increase the maximum output power above the targeted 35 dBm is sufficient, as Fig. 3-34 illustrates. A remarkable flat P_{sat} characteristic with a ΔP_{sat} of only 0.5 dB could be realized over the full band, after fixing some minor SMD self-resonance issues arising from the package assembly.

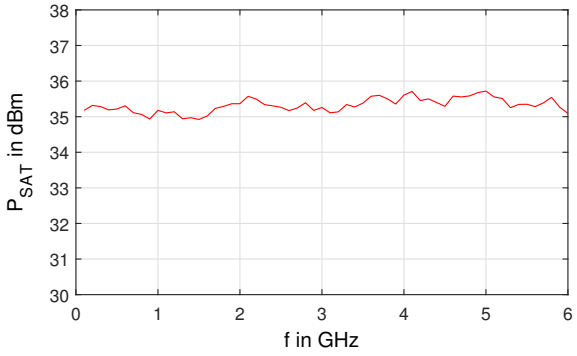
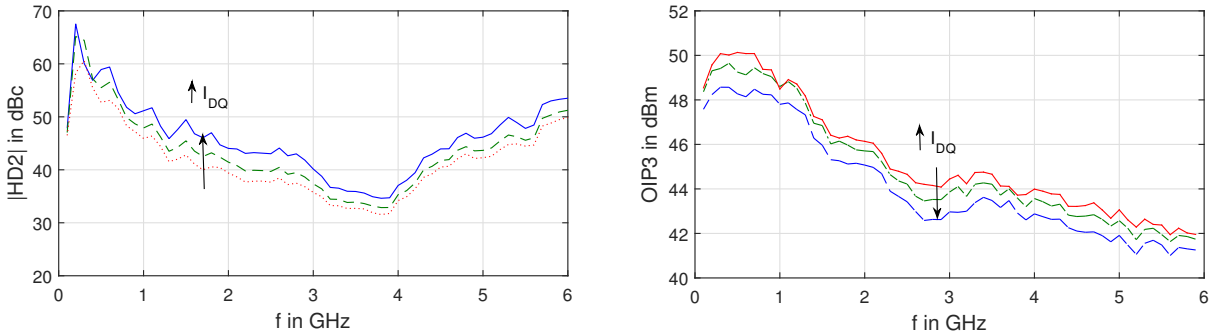


Fig. 3-34: Measured P_{sat} of the DC-6 GHz Feedback MMIC Futago_V3 in package at V_{DS} = 28 V and I_{DS} = 200 mA/mm

The downside of the improved ΔP_{sat} performance by increasing the device size by roughly 46% is the increase in $HD2$ from prior -40 dBc to only -35 dBc at P_{out} = 25 dBm at midband, as the measurements in Fig. 3-35 (a) reveal. By further increasing the drain quiescent current from I_{DS} = 200 mA/mm to 250 mA/mm the second order harmonic can be reduced by 5 dB. Surprisingly for the two-tone intermodulation measurements the $OIP3$ behaves in an opposite way, showing that a further increase of I_{DS} toward class A does not necessarily reduce third order intermodulation products.



(a) (b)

Fig. 3-35: Measured (a) $HD2$ at P_{out} = 25 dBm and (b) $OIP3$ with Δf = 5 MHz of the DC-6 GHz Feedback MMIC "Futago V3" in package for V_{DS} = 28 V and I_{DS} = 200, 225 & 250 mA/mm

3.3.5 Performance Improvement Measures

The following sub-sections will shortly address circuit concepts, which are suited to improve the gain-bandwidth product compared to a simple CS-FBPA. Due to the lack of CG-models in the PDK and the limited time-frame of this work, none of the suggested concepts has been implemented in hardware, but is intended in the future work.

Cascode FBPA

The implementation of cascodes is a useful measure to increase the bandwidth of an amplifier by the suppression of the Miller effect [87]. Due to the increased output voltage swing, the maximum output power as well as gain is raised. In general it is possible to apply two different concepts of parallel feedback over a cascode, which are shown in Fig. 3-36. Either the feedback loop is closed over the whole cascode, as depicted in (a), or only over the CS-HEMT as in (b). The former approach is the more common one due to its larger feedback effect, which was successfully applied without series resistive feedback in GaN by e.g. K. Kobayashi in [88, 89], achieving a BW from 0.25-3.0 GHz with roughly 20 dB gain together with an output power of 8 W and an $OIP3$ of larger than 50 dBm.

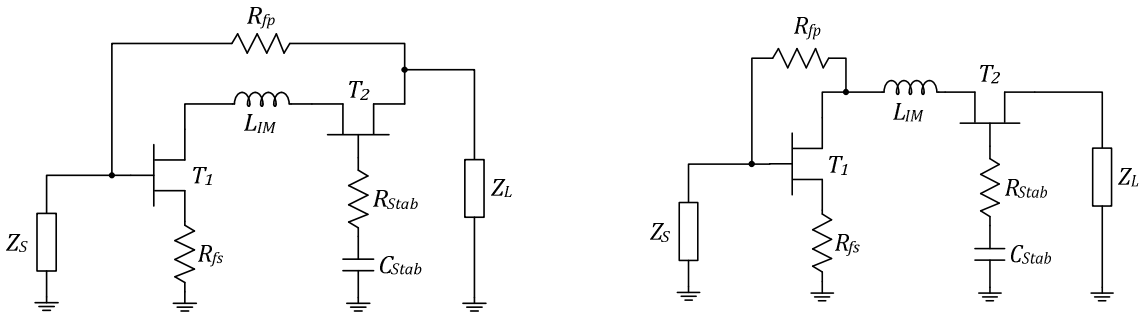


Fig. 3-36: Schematic of Cascode FBPA with series and (a) parallel resistive feedback over CS-HEMT and (b) parallel resistive feedback over CS- and CG-HEMT

Unfortunately as already mentioned at the beginning, based on the lack of proper CG-HEMT models in the utilized GaN25 technology and on the susceptibility to instabilities of the cascode, the FBPA design with cascodes was not realized within this work. A second disadvantage of the cascode is its inherent frequency dependent mismatch between the CS-output and CG-input, which complicates power matching over wide frequency ranges without sacrificing too much gain at the same time. Nevertheless, making use of cascodes might give superior performance dependent on the targeted frequency range.

Darlington f_T-Doubler & Darlington f_T-Doubler-Cascode FBPA

In order to overcome the inflicted BW-restriction by C_{GS} in CS- and CC-FBPAs, the implementation of a Darlington stage, as depicted in Fig. 3-37, helps to boost the BW significantly. Since originally R_{fs} is equal to infinity in a Darlington-stage, the input impedance would be first of all equal to

$$Z_{IN} = R_{\mathrm{GS1}} + R_{\mathrm{GS2}} - \frac{g_{m1}}{\omega^2 C_{\mathrm{GS1}} C_{\mathrm{GS2}}} - \frac{j}{\omega}\left(\frac{1}{C_{\mathrm{GS1}}} + \frac{1 + R_{gs2} g_{m1}}{C_{\mathrm{GS2}}}\right), \tag{3.70}$$

which gives an effective input capacitance of

$$C_{IN,eff} = \frac{C_{\mathrm{GS1}} C_{\mathrm{GS2}}}{C_{\mathrm{GS2}} + C_{\mathrm{GS1}}(1 + R_{\mathrm{GS2}} g_{m1})}, \tag{3.71}$$

under negligence of any feedback ($C_{\mathrm{GD}} = 0$ F). Equation (3.71) reveals that the effective input capacitance $C_{IN,eff}$ is only for very small R_{GS2} equal to the shunt connection of C_{GS1} and C_{GS2}. For equal C_{GS1} and C_{GS2} the final input capacitance would be halved, which also can be viewed as doubling the f_T, according to $f \approx g_m/(\omega C_{IN,eff})$. A Darlington stage forms thus a kind of f_T-doubler circuit. Due to the loading of T_1's source by C_{GS2} in a Darlington stage ($R_{fs} = \infty\ \Omega$), no RF-current and thus output power can be contributed by T_1 at DC. Only toward f_T, enough RF-current can sink through C_{GS2} towards ground and the output power contribution becomes more equally distributed between T_1 and T_2. In order to keep the output power contribution of both HEMTs constant over frequency, a series resistive and inductive feedback needs to be applied at the source of T_1, as already proven by K. Krishnamurthy *et al.* in [90]. Moreover, T_1 and T_2 need to be of equal size to reach saturation of both devices simultaneously. Under consideration of the series feedback elements, the input impedance results in

$$Z_{IN,2f_T} = R_{\mathrm{GS}} + \frac{1}{j\omega C_{\mathrm{GS}}} + \left(1 + \frac{g_m}{j\omega C_{\mathrm{GS}}}\right)\left(\frac{Z_{fs}(1 + j\omega C_{\mathrm{GS}} R_{\mathrm{GS}})}{j\omega C_{\mathrm{GS}} Z_{fs} + (1 + j\omega C_{\mathrm{GS}} R_{\mathrm{GS}})}\right) \tag{3.72}$$

where $Z_{fs} = R_{fs} + j\omega L_{fs}$. Chosing now the values for the series feedback elements equal to $L_{fs} = C_{\mathrm{GS}} R_{\mathrm{GS}}/g_m$ and $R_{fs} = 1/g_m$, ends up in the compensated input impedance

$$Z_{IN} = 2 \cdot \left(R_{\mathrm{GS}} + \frac{1}{j\omega C_{\mathrm{GS}}}\right), \tag{3.73}$$

such that the drive voltages for T_1 and T_2 are constant over frequency and hence the RF-currents through T_1 and T_2. Moreover, by adding a series inductance at the source the input sees a frequency independent real-part (see [91]), which compensates the negative real-part in (3.70) and hence stabilizes the standard Darlington-stage. With respect to output power, the Darlington f_T-doubler stage with the same overall device size performs slightly worse than a simple CS-HEMT. This is based on the fact that the maximum voltage swing of T_1 is reduced by the series feedback Z_{fs} by around one pinch-off voltage.

Furthermore, the Darlington f_T-doubler stage can be in general also combined with a CG-HEMT, forming a cascode, as depicted in Fig. 3-37 (b). This might even further improve BW, power and linearity, as already pro-

posed for the CS-FBPA in the preceding part. Based on the limited time for this work a comparison of a Darlington FBPA with the designed CS-FBPA has not been conducted, but is intended in the future.

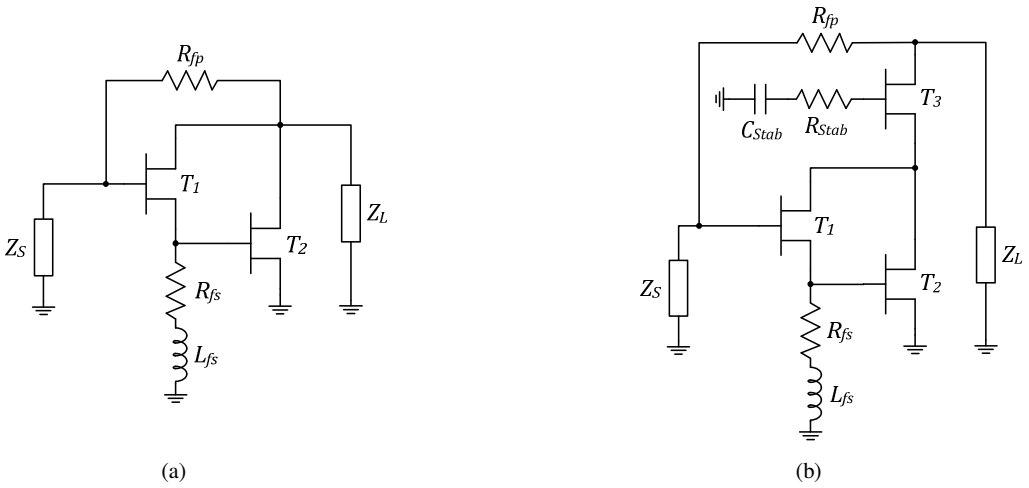


Fig. 3-37: Schematic of FBPA with (a) Darlington-stage and (b) Cascode Darlington-stage applying series and parallel resistive feedback

3.3.6 Key Findings

The concept of feedback based amplification is well suited for the implementation of multi-decade PAs, where not only P_{sat} is of interest but morevoer high linearity and low noise operation are required at the same time down to very low frequencies. From the preceding analyses in chapter 3.2.1, 3.3.1 and 3.3.2, the trade-off between optimum small-signal matching, high power gain and low-noise performance was examined down to low frequencies. It becomes evident that not all design optima can be fullfiled at the same time. On the on hand with increasing feedback the power gain drops and the NF increases, but on the other hand small-signal I/O-matching and linearity improve up to a certain point. The exact trade-offs for linearity will be discussed later in chapter 4.3.

In order to verify the suitability of GaN technology for building multi-decade FBPAs, a multi-decade 10 MHz - 6 GHz FBPA implemented in a 0.25µm GaN technology with an f_T of 30 GHz was designed and the measurement results are presented. The FBPA design exhibits a power gain-bandwidth product of larger than 60 GHz and is capable to operate even down to DC, dependent on the lowest frequency provided by the external SMD feedback blocking capacitor. Moreover, a NF in the frequency range from 30 MHz up to 5.5 GHz of smaller than 5 dB with a minimum of 2.8 dB at around 1 GHz was achieved. The maximum output power of the FBPA is larger than 35 dBm with a corresponding output power flatness of ΔP_{sat} = 0.5 dB over the full band. The measured linearity performance proved to be reasonably good with a HD of better than -35 dBc at P_{out} = 25 dBm and an $OIP3$ of larger than 40 dBm over the full bandwidth. All of the measurements were taken at a nominal bias point of V_{DS} = 28 V and I_{DS} = 200 mA/mm, which gives with respect to thermal simulations a reliability of larger than 10^6 hrs, according to the Arrhenius plots provided by the foundry.

3.4 Distributed Power Amplifiers

The traveling-wave amplifier concept was invented in 1936 by W.S. Percival, based on electron tubes [92]. The main idea behind this concept is the integration of the parasitic elements of the amplifying devices into the input and output transmission lines, forming so called artificial transmission lines. It was only after the advent of solid-state circuits in the early 1980`s that the TWA concept was picked up again by Y. Ayasli [93, 94, 95, 96], J. B. Beyer in [97, 98] and later K. B. Niclas [80, 99] and the first GaAs TWAs discovered their commercial break-through. Frequencies exceeding several GHz opened up new application spectra, as e.g. in the realm of radar systems, optical communications and also measurement instruments. For the latter application, solid-state TWAs enabled to push the BW in e.g. network analyzers (NVA) or (vector) signal-generators ((V)SG) above any known limit by that time.

3.4.1 Transfer Characteristics

The principal of operation of a traveling-wave amplifier (TWA) or distributed amplifier (DA) is very straight-forward, once it is understood. As can be seen in Fig. 3-38, the input signal applied to the port RF_{IN} travels down the gate-line and is at the end of the gate-line absorbed by the impedance matched gate-termination RF_{GT} in order to minimize reflections seen from the input. On its way along the gate-line, the signal experiences ideally only a shift in phase, so each amplifying stage connected to the gate-line is driven by the same signal amplitude. After amplification of the gate-line signal by each amplifying stage the signal is fed forward onto the output line, which is also called drain-line, in correspondence to the drain output port of the amplifying stages. The crucial condition for amplification is the coherency of the phase delay on the gate- and drain-line, which has to be exactly equal in order to obtain constructive interference at the output port RF_{OUT}. It can hence be deduced from the fundamental prerequisite of constructive interference that the gain of the TWA depends on the sum of the amplifying stages rather than on the product, as it is the case in chain- or cascaded amplifier structures. In Fig. 3-38, voltage controlled current sources with equal transconductance g_m are assumed in each amplifying stage at the beginning. Based on the foregoing simple consideration the voltage gain for equal phase velocities on the gate- and drain-line of the TWA can be derived to

$$G_V = \frac{1}{2} N g_m Z_{0,D}, \tag{3.74}$$

where $Z_{0,D}$ represents the characteristic impedance of the drain-line. The factor 1/2 illustrates that due to the symmetry half of the output current is dumped in the drain-termination R_{DT}, which is disadvantageous in terms of output power, but helps likewise to R_{GT} to obtain lower reflections and therewith better output matching. As equation (3.74) already suggests, the gain of the TWA is only of moderate magnitude, but the great advantage is the high bandwidth, based on the distributed nature of the TWA. Despite its parallel appearing structure, the amplifying stages are not truly electrically arranged in parallel but rather are integral parts of the gate- and drain-TLs. Thus, all parasitic input and output capacitances of the amplifying stages are not added, as e.g. in a real parallel amplifier where the bandwidth decreases with the number of parallel stages, but are part of the gate- and drain-TL, forming so called artificial transmission lines.

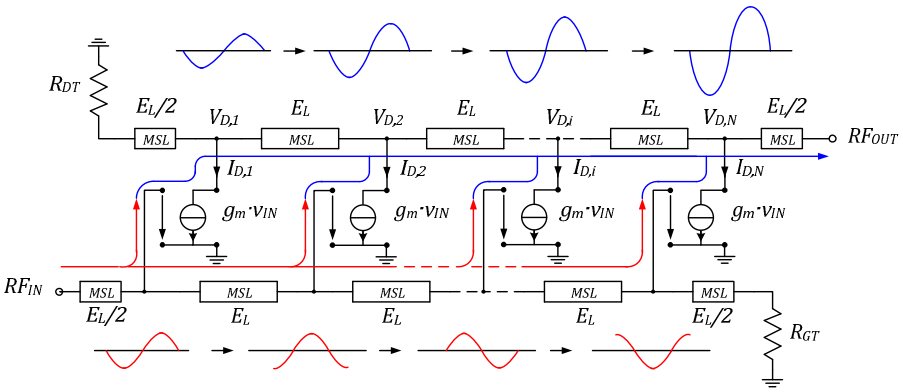


Fig. 3-38: Conventional uniform TWA (UDPA) topology with voltage controlled current sources as active elements

If the voltage controlled current sources of Fig. 3-38 are replaced by common-source HEMTs with a simplified small-signal equivalent circuit model (green dashed box in Fig. 3-39), the artificial gate- and drain-line become capacitively and resistively loaded, as Fig. 3-39 indicates. The so formed T-sections can be approximated by lossy constant k-sections, which suppose to be ideally terminated at both sides in their image impedance. In this way, a distributed nature of the line can be assumed for the derivation of the following transfer characteristics, which are summarized in Table 3-1 and are derived in Appendix D and E according to [100].

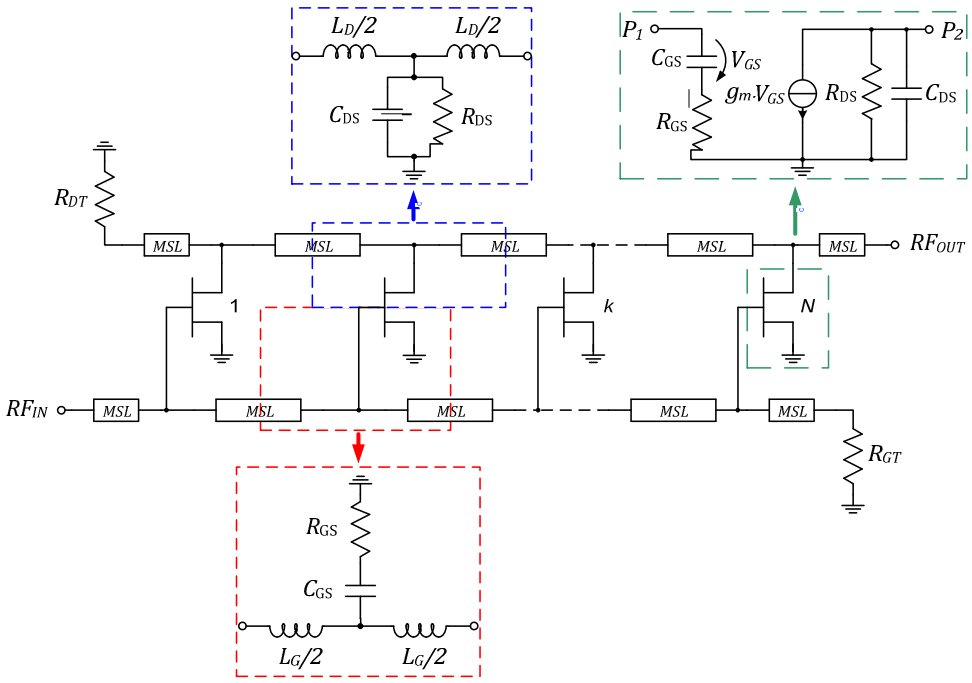


Fig. 3-39: Conventional uniform TWA topology (UDPA)

Table 3-1: General uniform TWA formulas

Power Gain	$G_P = \frac{{g_m}^2 Z_G Z_D}{4(1+j\omega C_{GS}R_{GS})^2} \cdot \left\| \frac{e^{-N\cdot\gamma_D l_D} - e^{-N\cdot\gamma_G l_G}}{e^{\frac{1}{2}(\gamma_G l_G - \gamma_D l_D)} - e^{-\frac{1}{2}(\gamma_G l_G - \gamma_D l_D)}} \right\|^2$ $= \frac{{g_m}^2 Z_G Z_D}{4(1+j\omega C_{GS}R_{GS})^2} \cdot \left\| e^{-\frac{N}{2}(\gamma_G l_G + \gamma_D l_D)} \cdot \frac{sinh\left(\frac{N}{2}(\gamma_G l_G - \gamma_D l_D)\right)}{sinh\left(\frac{1}{2}(\gamma_G l_G - \gamma_D l_D)\right)} \right\|^2$	(3.75)
Gate/Drain-Line Impedance	$Z_G = \sqrt{\frac{{R_G}' + j\omega {L_G}'}{\left({G_G}' + \frac{(\omega C_{GS})^2 R_{GS}}{2\cdot l_G(1+(\omega C_{GS}R_{GS})^2)}\right) + j\omega({C_G}' + \frac{C_{GS}}{l_G(+(\omega C_{GS}R_{GS})^2)})}}$	(3.76)
	$Z_D = \sqrt{\frac{{R_D}' + j\omega {L_D}'}{\left({G_D}' + \frac{1}{R_{DS}l_D}\right) + j\omega({C_D}' + \frac{C_{DS}}{l_D})}}$	(3.77)
Gate/Drain-Line Attenuation ($\beta_G = \beta_D$)	$\alpha_G \cong \frac{\omega^2 C_{GS}R_{GS}}{2} \cdot \sqrt{\frac{{L_G}' C_{GS}}{l_G(1+(\omega C_{GS}R_{GS})^2)}}$	(3.78)
	$\alpha_D \cong \frac{1}{2\cdot R_{DS}l_D} \cdot \sqrt{\frac{{L_D}'}{C_{DS}}} l_D$	(3.79)
Gate/Drain-Line Phase Coeff.	$\beta_G \cong \omega \cdot \sqrt{\frac{{L_G}' C_{GS}}{l_G(1+(\omega C_{GS}R_{GS})^2)}}$	(3.80)
	$\beta_D \cong \omega \cdot \sqrt{\frac{{L_D}' C_{DS}}{l_D}}$	(3.81)

Equation (3.76) and (3.77) describe the characteristic loaded gate- and drain-line impedance with the unloaded series gate-/drain-line resistance ${R_{G/D}}'$, series inductance ${L_{G/D}}'$, shunt line conductance ${G_{G/D}}'$ and shunt capacitance ${C_{G/D}}'$ per unit length. It is always assumed that the input and output impedance of the transistor is "smeared" over the gate- and drain-line length l_G and l_D per section. This distributed assumption is only valid up to frequencies at which the gate- and drain-line become periodically loaded by the transistors. The corresponding gate- and drain-line attenuation and phase coefficients can be approximated by (3.78) to (3.81) under the valid assumption of $C_{GS/DS}/l_{G/D} \gg {C_{G/D}}'$ and for small ω. Note that in all presented equations (3.75) to (3.81) above the impact of the feedback capacitance ($C_{GD} = 0$ F) is neglected for simplicity.

3.4.2 Capacitively Coupled TWA Biasing

Capacitively coupled TWAs (CCTWA) make use of a series coupling capacitor (C_C) in front of each amplifying stage in a TWA. In this way, the effective input capacitance seen by the gate-line is lowered by means of the additional introduced series capacitance and therefore bandwidth can be traded-off for gain, as presented by A. Ayasli in [95]. In order to provide proper gate-biasing to all transistor stages in a CCTWA usually one of the two most common topologies is applied, which are depicted in Fig. 3-40 below.

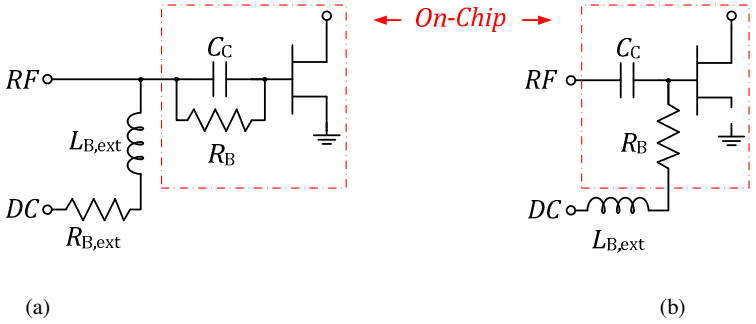


Fig. 3-40: (a) parallel RC-biasing scheme and (b) separate biasing scheme for capacitively coupled TWA stages

In Fig. 3-40 (a), the gate-bias is fed over the RF gate-line and for this reason an on-chip DC by-pass resistor R_B is needed. If operation down to DC is desired the external RF-choke $L_{B,ext}$ has to be replaced or expanded by a series resistor $R_{B,ext}$ providing several hundreds of Ohms, since otherwise the lowest frequency of operation is confined by $L_{B,ext}$. In Fig. 3-40 (b) in contrast is the gate-bias immediately connected over R_B to the gate of the transistor. Though the additional RF-choke $L_{B,ext}$ is not necessarily needed as long as the value of R_B is sufficiently high in order not to load the gate. Consequentially, the value for R_B has to be in the order of several hundreds of Ohms in order to not degrade RF-performance.

If no gate-coupling capacitor is needed in terms of bandwidth, the TWA´s output noise is not significantly affected by the biasing circuitry since either no resistive components are present or to a major extent mismatched to Z_0, as will be more closely discussed in section 3.4.3.

3.4.3 Noise Analysis of TWAs

Within this section a detailed analysis and comparison of noise in conventional and capacitively coupled TWAs (CCTWA) is presented. C. Aitchison *et al.* [101] were the first in 1985 who found an analytical expression for the NF of a conventional TWA. Later in 2005, W. Ko *et al.* [102] extended the analysis by taking losses introduced by the extrinsic shell of the HEMT and the gate- and drain-feeding structures of the TWA into account. By using lossy m-derived sections instead of lossless constant k-sections they found out that the NF can be mainly underestimated towards higher frequencies, when additional propagation losses as well as parasitic inductances are neglected. In terms of broadband amplifiers down to DC, which are intended for the application in signal generators (SG), especially the NF at low frequencies is a critical parameter, because the step attenuator at the output of the SG exhibits less attenuation at low frequencies than at high frequencies. Accordingly, the minimum SNR specification of the SG is more likely violated at low frequencies than at high frequencies, as

was also shortly discussed in the introduction in chapter 1.1. Out of this reason, the following noise analysis is based on the analysis from C. Aitchison *et al.* [101], since the absolute NF value at the upper band edge is not of major concern. More important is the low frequency noise arising from the bias network in a TWA, which is in the following examinations considered in order to identify the optimum bias scheme for achieving low noise performance. Additionally, the influence of capacitively coupled gates [95] on the overall NF in a TWA is investigated for the first time.

In the course of the analysis each uncorrelated noise contributor in the TWA, denoted by x in (3.82), is identified and its noise impact calculated separately by computation of the corresponding NF_x according to

$$NF_x = 10 \cdot log\left(\frac{SNR_i}{SNR_o}\right) = 10 \cdot log\left(1 + \frac{N_x \cdot Z_0}{G_P \cdot kT}\right). \tag{3.82}$$

Equation (3.82) assumes that the input and output of the TWA are sufficiently well matched and the power gain (G_P) is constant over the desired bandwidth. Latter is in terms of capacitively coupled gates a realistic approximation, because the gain flatness of the TWA can be very well adjusted by using series gate capacitors [95].

At the end of the noise analysis the summation of the noise-current spectral densities ($NCSD$) over all m noise contributors yields an analytical expression for the computation of the total NF (NF_{tot}), which predicts the noise characteristics of a capacitively coupled TWA design.

$$NF_{tot} = 10 \cdot log\left(1 + \frac{\sum_{x=1}^{m} N_x \cdot Z_0}{G_P \cdot k_B T}\right) \tag{3.83}$$

Additional Note: It has to be mentioned that in the ongoing analysis the electrical length βl is used interchangeably with the frequency ω by making use of the following relationship (3.84)

$$E_l = \beta l = \omega \cdot \frac{l}{v_p}, \tag{3.84}$$

where l is the length of the transmission-line section in Fig. 3-41 and v_p is the phase velocity of the signal. The electrical length of each gate- and drain-line section is furthermore assumed equal ($\beta_G l_G = \beta_D l_D = \beta l$).

Induced-gate noise in TWAs

For the conventional TWA with no capacitive gate-coupling the induced-gate noise current $\underline{i}_{n,G}$ feeds on each gate the real impedance $Z_0/2$, producing a rms-noise voltage, which applies to all N stages and is further amplified by g_m of each stage to the output.

The forward transfer function from the k^{th}-stage to the output in a TWA can be derived from Fig. 3-41 and can be expressed by

$$\underline{T}_F(k, \beta l) = (N - k + 1) \cdot e^{-j\left(N-k+\frac{1}{2}\right)\beta l}. \tag{3.85}$$

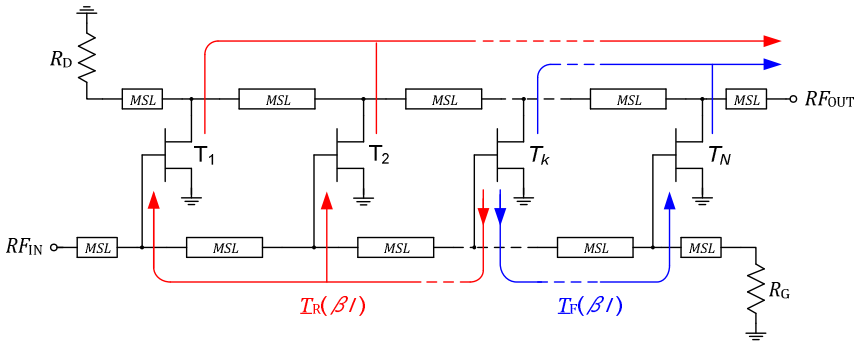


Fig. 3-41: Forward and reverse transfer functions $T_F(\beta)$ and $T_R(\beta)$ in a conventional TWA

Accordingly, the reverse transfer function yields

$$\underline{T}_R(k,\beta l) = \left(\frac{\sin\big((k-1)\beta l\big)}{\sin(\beta l)}\right)\cdot e^{-j\left(N+\frac{1}{2}\right)\beta l}. \tag{3.86}$$

The factor $Ng_mZ_0/4$ embodied in the forward and reverse transfer functions is simply omitted in (3.85) and (3.86) for a better clarity and visibility. To obtain the resulting noise spectral density (NSD) transfer function $f_N(k,\beta l)$, the squared magnitude of the vector sum of equations (3.85) and (3.86) has to be formed. By making use of the complex relationship

$$\left|\underline{x}+\underline{y}\right|^2 = \left|\underline{x}\right|^2 + \left|\underline{y}\right|^2 + 2\cdot Re\left\{\underline{x}\cdot\underline{y}^*\right\}, \tag{3.87}$$

$f_N(k,\beta l)$ results in

$$f_N(k,\beta l) = (N-k+1)^2 + \left(\frac{\sin\big((k-1)\beta l\big)}{\sin(\beta l)}\right)^2 + \frac{2(N-k+1)\cdot\sin((k-1)\beta l)\cdot\cos(k\beta l)}{\sin(\beta l)}. \tag{3.88}$$

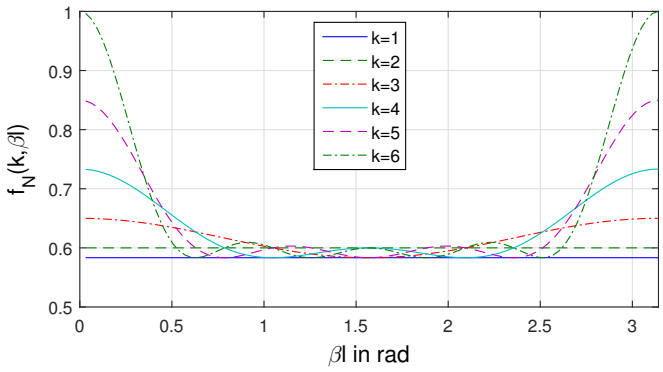


Fig. 3-42: Normalized $f_N(k,\beta l)$ vs. βl for different k and (N = 6) of TWA

The first and second term of the sum in equation (3.88) constitute the forward and reverse transfer function squared, whereas the last term results from correlation, generating additional noise power at the output. Fig. 3-42 shows the normalized sum of $f_N(k,\beta l)$ for the k^{th}-stage of a 6-stage TWA. At the lower and higher band edges the transfer function becomes more pronounced toward $k = N$.

The resulting $CNSD\ N_{i,G}(N)$ of the induced-gate noise flowing through the drain load $Z_L = Z_0$ can be finally described by

$$N_{i,G}(N) = \left[\sqrt{\overline{|\underline{i}_{n,G}|^2}}\frac{Z_0}{2}g_m\right]^2 \cdot \sum_{k=1}^{N} f_N(k,\beta l). \tag{3.89}$$

The factor 1/2 takes into account that half of the induced-gate noise current is absorbed by the drain-line termination in a uniform TWA (UDPA). The sum term over k in equation (3.89) incorporates the sum of the noise power of all N stages, where the induced-gate noise $\underline{i}_{n,G}$ of each single stage is uncorrelated. This is only true as long as no capacitive gate-coupling is applied. In the case of capacitively coupled gates, the induced-gate noise current does not feed $Z_0/2$ at its gate, as mentioned in the foregoing section, but rather sees different complex (trans)-impedances in the forward and reverse transfer functions. These two transfer functions will be distinguished in the ongoing considerations. First of all, influences of the BNs are simply neglected, which corresponds to $R_B \to \infty\,\Omega$ in Fig. 3-40 (a) and (b). Later on in this section the implemented BNs will be taken into account.

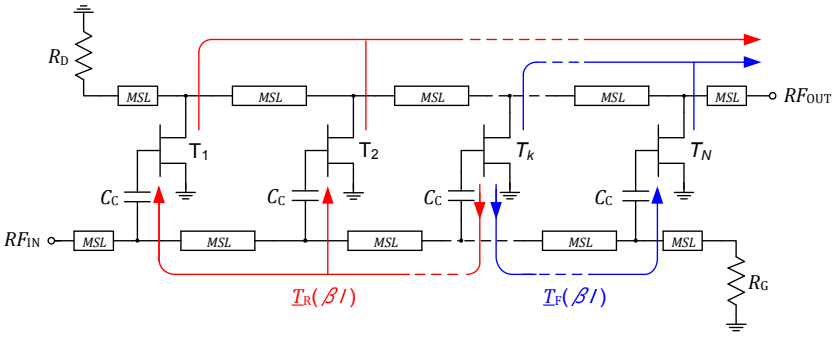


Fig. 3-43: Forward and reverse transfer functions $T_F(\beta l)$ & $T_R(\beta l)$ in a CCTWA

Fig. 3-43 sketches the same TWA schematic as already presented in Fig. 3-41, but now including the series gate capacitors C_C. Due to the reverse amplification exhibits $\underline{i}_{n,G}$ the same transfer function as already equated in (3.88) but sees a different transimpedance $\underline{Z}_T(\omega)$ from the k^{th}-stage to the foregoing stages k-i (i = 1…k-1), incorporating the capacitive voltage divider formed by C_C and C_{GS}. In this case the corresponding expression for $\underline{Z}_T(\omega)$ equals

$$\underline{Z}_T(\omega) = \frac{C_C}{C_{\text{GS}} + C_C} \cdot \frac{j\omega C_C \frac{Z_0}{2}}{j\omega C_{\text{GS}}\left(1 + j\omega C_C \frac{Z_0}{2}\right) + j\omega C_{\text{GS}}}. \tag{3.90}$$

Now, the output induced-gate noise current of the k^{th}-stage due to reverse amplification can be expressed via

$$\underline{i}_{G,R}(k,\beta l) = \frac{1}{2} g_m \sqrt{\overline{\left|\underline{i}_{n,\mathrm{G}}\right|^2}} \cdot \underline{Z}_T(\omega) \frac{\sin\big((k-1)\beta l\big)}{\sin(\beta l)} e^{-j\left(N+\frac{1}{2}\right)\beta l}. \tag{3.91}$$

Similarly for the forward amplification $\underline{i}_{n,G}$ sees at the k^{th}-stage the complex gate impedance $\underline{Z}_{\mathrm{G}}(\omega)$, giving

$$\underline{Z}_G(\omega) = \frac{1 + j\omega C_C \frac{Z_0}{2}}{\left(1 + j\omega \frac{Z_0}{2}\right) \cdot j\omega C_{\mathrm{GS}} + j\omega C_C}. \tag{3.92}$$

For stages k+1 up to N, the same transimpedance $\underline{\mathrm{Z}}_T(\omega)$ as for the reverse amplification applies. Replacing $\mathrm{Z}_0/2$ in (3.89) by $\underline{Z}_G(\omega)$ and $\underline{Z}_T(\omega)$, $\underline{i}_{n,G}$ due to forward gain for the k^{th}-stage results in

$$\underline{i}_{\mathrm{G},F}(k,\beta l) = \frac{1}{2} g_m \sqrt{\overline{\left|\underline{i}_{n,\mathrm{G}}\right|^2}} \cdot \left[\underline{Z}_{\mathrm{G}}(\omega) + (N-k)\underline{Z}_T(\omega)\right] \cdot e^{-j\left(N-k+\frac{1}{2}\right)\beta l} \tag{3.93}$$

In the final step, applying vectorial summation of the reverse and forward amplified $\underline{i}_{n,G}$ from (3.91) and (3.93) gives the $NCSD$ of $\underline{i}_{n,G}$ of the k^{th}-stage at the CCTWA´s output

$$N_{i,G,tot}(N) = \left|\underline{i}_{G,R}(\beta l) + \underline{i}_{G,F}(\beta l)\right|^2 = \left[\sqrt{\overline{\left|\underline{i}_{n,G}\right|^2}} \frac{g_m}{2}\right]^2 \cdot \sum_{k=1}^{N} f_{Nx}(k,\beta l), \tag{3.94}$$

where

$$\begin{aligned} f_{Nx}(k,\beta l) = {} & \left\{\left|\underline{Z}_G(\omega) + (N-k)\underline{Z}_T(\omega)\right|^2 + \left|\underline{Z}_T(\omega) \frac{sin\big((k-1)\beta l\big)}{sin(\beta l)}\right|^2 \right. \\ & \left. + 2 \cdot \frac{(sin((k-1)\beta l)}{sin(\beta l)} \cdot Re\left\{\left(\underline{Z}_G(\omega) \cdot \underline{Z}_T(\omega)^* + \left|\underline{Z}_T(\omega)\right|^2 (N-k)\right) e^{jk\beta l}\right\}\right\} \end{aligned} \tag{3.95}$$

in (3.94) describes the transfer function of one single stage to the output, taking forward and reverse transmission and the summation over all N stages into account. Comparison of (3.94) with (3.89) for the CCTWA and the TWA leads to the conclusion that $NF_{i,G}$ for the CCTWA increases toward low frequencies due to $\underline{Z}_G(\omega)$ and hence the contribution of the induced-gate noise at the output compared to the conventional TWA is augmented to a greater extent toward DC, as can be seen from Fig. 3-44.

Channel Noise in TWAs

For the drain-channel noise in (3.96) the $CNSD$ $N_{i,D}(N)$ at the output is simply the sum of the channel noise of each single stage, which therefore yields

$$N_{i,D}(N) = \frac{1}{4} \cdot N \cdot \overline{\left|\underline{i}_{n,D}\right|^2}, \tag{3.96}$$

where again half of the noise-current is dissipated in the drain-termination for the case of a uniform TWA. Opposed to the frequency dependent induced-gate noise shows the channel noise no frequency dependence at all, as Fig. 3-44 below reveals.

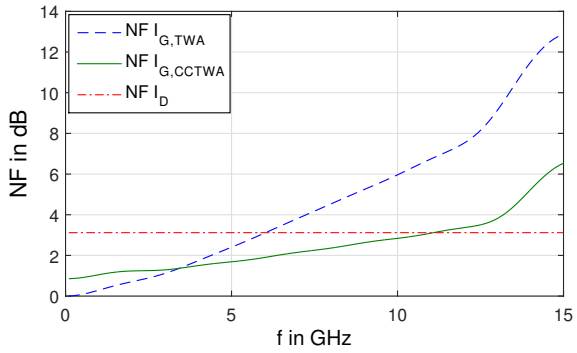


Fig. 3-44: NF of induced-gate- and channel-noise for TWA & CCTWA with $N = 6$

Correlation between Induced-gate Noise and Channel Noise in TWA & CCTWA

As stated in [101], in terms of no capacitive gate-coupling the correlation term between $\underline{i}_{n,G}$ and $\underline{i}_{n,D}$ of the k^{th}-stage can be omitted due to the fact that both currents feed real impedances $Z_0/2$ on the gate- and drain-line and the correlation coefficient $\underline{c}$ of HEMTs can be very well approximated to be purely imaginary [59, 103]. In this case is the output NSD simply the sum of the induced-gate and channel noise transferred to the output. This observation is only valid in terms of forward noise transfer, but does not take into account that the reverse transfer function creates correlation between $\underline{i}_{n,G}$ and $\underline{i}_{n,D}$ at the output, affecting NF. In [101], this has not been considered and is therefore incorporated in the following for the case of a TWA and CCTWA. The $NCSD$ for the TWA can hence be expressed by

$$\begin{aligned} C_i(k) &= 2 \cdot Re\left\{\left(\underline{i}_{G,F}(k,\beta l) + \underline{i}_{G,R}(k,\beta l)\right)^* \cdot \underline{i}_{D,O}(k,\beta l)\right\} \\ &= \frac{g_m Z_0}{4}\sqrt{\overline{|\underline{i}_{n,G}|^2 |\underline{i}_{n,D}|^2}} \cdot Re\left\{\underline{c} \cdot \left[(N-k+1) + \frac{sin\big((k-1)\beta l\big)}{sin(\beta l)} e^{jk\beta l}\right]\right\}. \end{aligned} \tag{3.97}$$

Equation (3.97) simplifies further for $\underline{c}$ being purely imaginary to

$$C_i(k) = -\frac{g_m Z_0}{4} c \cdot \sqrt{\overline{|\underline{i}_{n,G}|^2 |\underline{i}_{n,D}|^2}}\, \frac{sin\big((k-1)\beta l\big)}{sin(\beta l)} sin(k\beta l) \tag{3.98}$$

If capacitive gate-coupling is applied, $\underline{Z}_G(\omega)$ seen by the HEMT-gates is almost purely capacitive, highly effecting the correlation term $C_i(k)$ toward low frequencies (see Appendix C). The resulting correlation between $\underline{i}_{n,G}$ and $\underline{i}_{n,D}$ at the output yields the following $NCSD$ in (3.99).

$$C_i(k) = 2 \cdot Re\left\{\left(\underline{i}_{G,F}(k,\beta l) + \underline{i}_{G,R}(k,\beta l)\right)^* \cdot \underline{i}_{D,O}(k,\beta l)\right\} \tag{3.99}$$

$$= \frac{1}{2} g_m \sqrt{\overline{|\underline{i}_{n,G}|^2 |\underline{i}_{n,D}|^2}} \cdot Re\left\{\underline{c} \cdot \left[\left(\underline{Z}_G(\beta l) + (N-k) \cdot \underline{Z}_T(\beta l)\right)^* + \underline{Z}_T(\beta l)^* \cdot e^{jk\beta l} \cdot \frac{sin\big((k-1)\beta l\big)}{sin(\beta l)}\right]\right\}.$$

Fig. 3-45 depicts the difference in utilizing capacitive gate-coupling and no capacitive gate-coupling for the noise correlation term C_i, defined by

$$C_i(N) = \sum_{k=1}^{N} C_i(k). \tag{3.100}$$

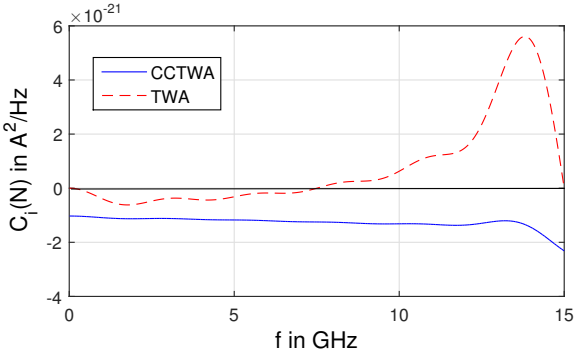


Fig. 3-45: Simulated C_i vs. f for a conventional TWA and a CCTWA with $N = 6$

As can be derived from Appendix C, cancellation in terms of capacitive gate-coupling is more pronounced, in particular toward higher frequencies compared to the case of no capacitive gate-coupling. From the factor $sin(k\beta l)$ in (3.99) it is obvious that if no capacitive gate-coupling is applied, $C_i(N)$ becomes positive above $f_c/2$ or $\beta l = 90°$, respectively, giving rise to the output noise. By designing the TWA only up to frequencies of $f_c/2$ or $\beta l = 90°$, which might be necessary to reduce ripple in order to obtain flat gain, noise cancellation by correlation can be exploited in low noise applications.

Thermal Noise from Gate- and Drain-Line Termination

In order to identify the noise influence of the noise arising from the gate-line termination impedance R_G, first of all the transfer function from the gate-line impedance to the output has to be determined, which can be obtained from straightforward calculation or by replacing k in (3.86) with N and adding the additional time delay from R_G to the N^{th}-stage. The final result gives

$$\underline{T}_R(\beta l) = \left(\frac{sin(N \cdot \beta l)}{sin(\beta l)}\right) \cdot e^{-jN\beta l}. \tag{3.101}$$

$\underline{T}_R(\beta l)$ is valid for all TWA structures and up to this point independent of the type of implemented gain stages (Cascodes, Darlington, etc.), capacitive gate-coupling or utilized topology (UDPA or NDPA). To attain

the corresponding NSD from the gate- and drain-line termination impedances for the CCTWA with simple common-source HEMTs, the capacitive voltage divider formed by C_C and C_{GS} has to be taken into account.

$$N_{GT}(N) = k_B T \cdot (1 - |\Gamma_{GT}|^2) \cdot \left(\frac{g_m Z_0}{2} \frac{C_C}{C_{GS} + C_C} \left| \frac{sin(N \cdot \beta l)}{sin(\beta l)} \right| \right)^2 \tag{3.102}$$

$$N_{DT}(N) = k_B T \cdot (1 - |\Gamma_{DT}|^2) \tag{3.103}$$

The transfer function in parenthesis in equation (3.102) represents the overall reverse power gain from the gate-termination to the output. Conversely, noise arising from R_{DT} is completely transferred to the output without undergoing any noise-shaping. In (3.102) and (3.103) it is furthermore assumed that R_{GT} and R_{DT} are not equal to Z_0, as it is often found in real designs in order to enhance gain or matching characteristics. This is considered by introducing the factor $\left(1 - \left|\Gamma_{GT/DT}\right|\right)^2$, which takes the noise power mismatch between the characteristic line impedance and line termination impedance into account. $\Gamma_{GT,DT}$ in (3.102) and (3.103) is simply equal to

$$\Gamma_{GT,DT} = \frac{R_{GT/DT} - Z_0}{R_{GT/DT} + Z_0}. \tag{3.104}$$

Thermal Noise from Bias-Networks

As already mentioned only noise contribution of biasing-networks for capacitively coupled TWAs is treated in this section. In terms of simplicity the input-impedance of the HEMT is simply assumed to be purely capacitive and is denoted by C_{GS} in the following. Furthermore, the RF-input is terminated by the characteristic impedance Z_0 = 50 Ω. For noise calculations the following equivalent noisy circuits are utilized and the noise voltage $\underline{v}_{n,R}$ transformed into $\underline{i}_{n,BNx}$ to make use of a similar transimpedance function, which was calculated for the induced-gate noise already in (3.95).

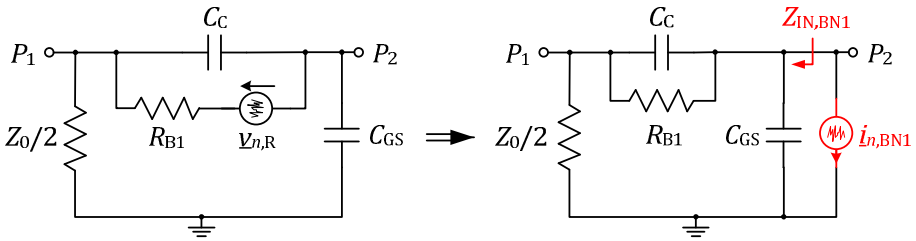


Fig. 3-46: Equivalent noise representation for TWA´s BN1 of Fig. 3-40 (a)

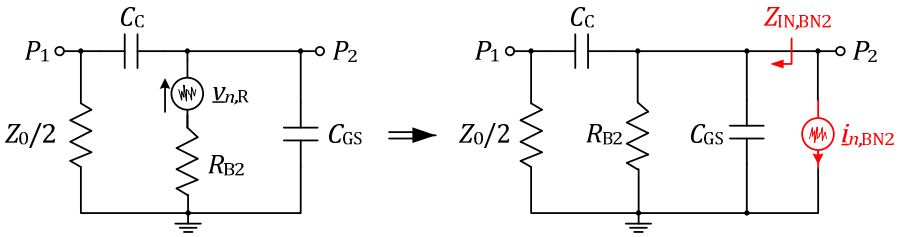


Fig. 3-47: Equivalent noise representation for TWA´s BN2 from Fig. 3-40 (b)

From Fig. 3-46 the following $CNSD$ can be determined for BN1 dependent on R_{B1} to

$$\overline{\left|\underline{i}_{n,BN1}\right|^2} = 4k_B T R_{B1} \cdot \frac{(\omega C_{GS})^2}{1 + (\omega C_C R_{B1})^2} \tag{3.105}$$

and equivalently from Fig. 3-47 for BN2 to

$$\overline{\left|\underline{i}_{n,BN2}\right|^2} = \frac{4k_B T}{R_{B2}}. \tag{3.106}$$

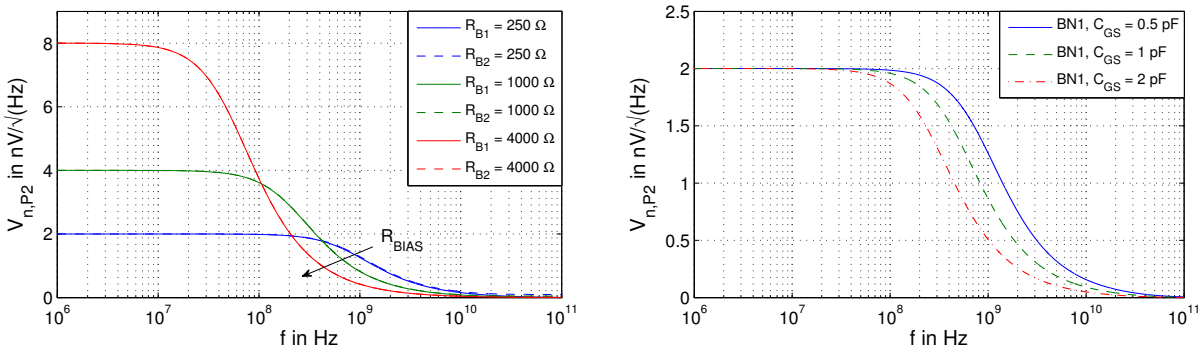
Comparison of the two NSDs should be conducted in terms of voltages rather than currents, since the transistor operates as a voltage controlled current source and thus the noise voltage is the dominant quantity. Therefore, the noise current needs to be multiplied by $Z_{IN,BNx}(\omega)$ from Fig. 3-46 and Fig. 3-47 and its magnitude squared to obtain the $NVSD$ at P2, giving for BN1

$$\overline{\left|\underline{v}_{n,BN1}\right|^2} = \frac{4k_B T R_{B1}}{\left(1 - \left(\omega^2 C_C C_{GS} R_{B1} \frac{Z_0}{2}\right)^2\right)^2 + \left(\omega\left(C_C R_{B1} + C_{GS}\left(R_{B1} + \frac{Z_0}{2}\right)\right)\right)^2} \tag{3.107}$$

and correspondingly for BN2

$$\overline{\left|\underline{v}_{n,BN2}\right|^2} = \frac{4k_B T R_{B2} \cdot \left(1 + \left(\omega C_C \frac{Z_0}{2}\right)^2\right)}{\left(1 - \left(\omega^2 C_C C_{GS} R_{B2} \frac{Z_0}{2}\right)^2\right)^2 + \left(\omega\left(C_{GS} R_{B2} + C_C\left(R_{B2} + \frac{Z_0}{2}\right)\right)\right)^2}. \tag{3.108}$$

For exact the same values of R_{B1} and R_{B2}, both $NVSD$ at P2 behave similar and become equal for $\omega \to 0$, as can be seen in Fig. 3-48 below. The comparable low characteristic line impedance of $Z_0/2 = 25\ \Omega$ has almost no influence on the overall noise voltage at the input, which can be also derived by shorting port P1 in Fig. 3-46 and Fig. 3-47, respectively.



(a) (b)

Fig. 3-48: (a) noise voltage vs. f at P2 for (a) BN1 and BN2 with R_B= 0.25, 1.0, 4.0 kΩ, C_{GS} = 0.5 pF, C_C = 0.25 pF, Z_0 = 50 Ω and (b) BN1 for C_{GS}/C_C sweep, R_B= 250 Ω, Z_0 = 50 Ω)

With decreasing frequency the HEMT´s input impedance at node P2 becomes due to C_{GS} very high, giving rise to the noise-voltage at P2. For the extreme case at DC (ω = 0 Hz), equations (3.107) and (3.108) strive for their maximum value of $4k_BTR_{Bx}$. The fact that the difference in noise contribution at high frequencies between bias network BN1 and BN2 is only very small is based on the typically small characteristic line impedance Z_0 = 50 Ω compared to $\underline{Z}_{IN} = 1/j\omega C_{\mathrm{GS}}$ of the HEMT toward low frequencies. With increasing R_B the noise maximum according to the numerator in (3.107) and (3.108) increases, but on the same time noise matching dependent on R_B and $\underline{Z}_{IN}$ shifts toward lower frequencies. This enables trimming of the biasing noise by means of proper sizing of R_B, as depicted in Fig. 3-48 (a). From Fig. 3-48 (b) it becomes also evident that a larger gate width (W_G) of the HEMT helps to minimize noise contribution from the bias networks BN1 and BN2 due to the larger C_{GS} values and therefore lower transistor input impedance.

Noise Calculations for complete CCTWA Bias Noise

Up to now, noise of the biasing networks BN1 and BN2 was only considered for one single stage. In a TWA structure the bias networks cannot be considered individually, but rather are connected in parallel to each other. Either they are physically connected over the RF gate-line (R_{B1}) or over a common bias line (R_{B2}) on-chip, as depicted in Fig. 3-49. At low frequencies the RF-choke provides a lower input impedance than the parallel stages. Therefore, only noise contribution from R_{B2} of the k^{th}-stage has to be taken into account. For the input impedance of $Z_{IN,k}$ seen by each stage into the gate-line in Fig. 3-49 the approximation of $Z_{G,k} \gg Z_{GL,k}$ is valid. Accordingly, taking $Z_{GL,k} = Z_0/2$ as input impedance seen into the gate-line, as in Fig. 3-46 and Fig. 3-47 already presumed, is a valid approximation for the TWA topology down to DC. Finally, the noise spectral densities of the k^{th}-gate noise current can be transferred to the output with the same function $f_{Nx}(k, \beta l)$ from (3.95) as the induced-gate noise.

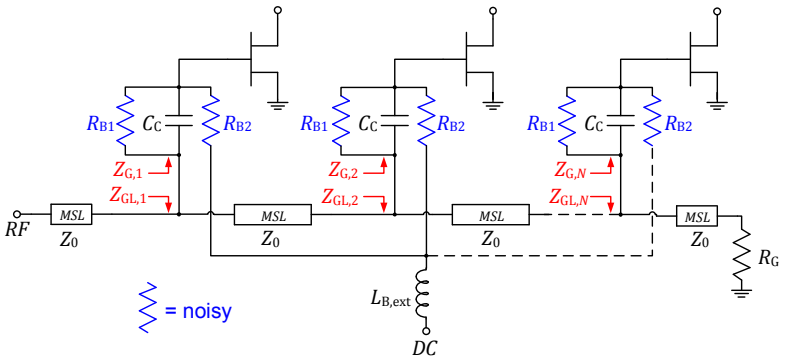


Fig. 3-49: CCTWA with direct gate bias over R_{B1} and separate gate bias over R_{B2} with an external choke $L_{\mathrm{B,ext}}$

$$N_{BN}(N) = \begin{cases} \left[\frac{1}{4} \cdot \sqrt{\overline{|\underline{i}_{n,BN}|^2}} \cdot g_m\right]^2 \cdot \sum_{k=1}^{N} f_{Nx}(k, \beta l) & ; \text{for UDPA} \\ \left[\frac{1}{2} \cdot \sqrt{\overline{|\underline{i}_{n,BN}|^2}} \cdot g_m\right]^2 \cdot \sum_{k=1}^{N} f_{Nx}(k, \beta l) & ; \text{for NDPA} \end{cases} \tag{3.109}$$

Merely the impedance $\underline{Z}_G(\omega)$ and the transimpedance $\underline{Z}_T(\omega)$ in $f_{Nx}(k, \beta l)$ in (3.95) have to be exchanged in order to take the different loading by R_B into account. $\underline{Z}_G(\omega)$ for BN1 and BN2 are equal to

$$\underline{Z}_{G,BN1}(\omega) = \frac{1}{j\omega C_{\mathrm{GS}} + \left(\frac{2(1 + j\omega C_C R_{B1})}{Z_0(1 + j\omega C_C R_{B1}) + R_{B1}}\right)} \tag{3.110}$$

and

$$\underline{Z}_{G,BN2}(\omega) = \frac{1}{\frac{j\omega C_C}{1 + j\omega C_C \, Z_0/2} + \frac{1 + j\omega C_C R_{B2}}{R_{B2}}}. \tag{3.111}$$

The transimpedance $\underline{Z}_T(\omega)$ can be expressed by $\underline{Z}_G(\omega)$ and the transfer functions $\underline{A}_{BNx}(\omega)$ and $\underline{B}_{BNx}(\omega)$, which transfer the noise-voltage at the gate of the k^{th}-stage over the gate-line to the gates of the other N-1 stages. Therein, $\underline{A}_{BNx}(\omega)$ specifies the transfer function from the k^{th}-gate voltage onto the gate-line and $\underline{B}_{BNx}(\omega)$ from the gate-line onto the i^{th}-gate, respectively, with $i = 1 \ldots N$ and $i \neq k$. The transimpedance $\underline{Z}_T(\omega)$ can be thus expressed by

$$\underline{Z}_{T,BNx}(\omega) = \underline{Z}_{G,BNx}(\omega) \cdot \underline{A}_{BNx}(\omega) \cdot \underline{B}_{BNx}(\omega). \tag{3.112}$$

$\underline{A}_{BNx}(\omega)$ and $\underline{B}_{BNx}(\omega)$ for BN1 and BN2 (3.112) are equal to

$$\underline{A}_{BN1}(\omega) = \frac{1}{1 + \frac{2R_{B1}}{Z_0(1 + j\omega C_C R_{B1})}} \tag{3.113}$$

$$\underline{B}_{BN1}(\omega) = \frac{1 + j\omega C_C R_{B1}}{1 + j\omega R_{B1}(C_C + C_{GS})} \tag{3.114}$$

$$\underline{A}_{BN2}(\omega) = \frac{1}{1 + \frac{2}{j\omega C_C Z_0}} \tag{3.115}$$

$$\underline{B}_{BN2}(\omega) = \frac{j\omega C_C R_{B2}}{1 + j\omega R_{B2}(C_C + C_{GS})}. \tag{3.116}$$

Accordingly, the magnitude of $\underline{Z}_{T,BNx}(\omega)$ from (3.112) is plotted below in Fig. 3-50, showing that the noise transfer to the other stages for BN1 increases with decreasing frequency, whereas for BN2 the noise transfer tends to drop to zero.

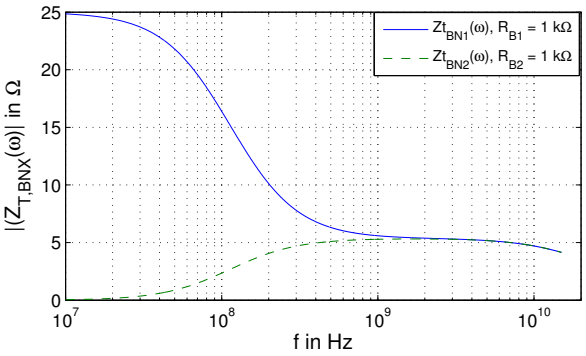


Fig. 3-50: $|\underline{Z}_{T,BNx}(\omega)|$ of BN1 and BN2

Noise Calculations of Conventional TWA Bias

By means of Fig. 3-40 the influence of the BN for conventional TWAs can also shortly be discussed. In this case the TWA is usually biased by an external RF-choke $L_{B,\mathrm{ext}}$ together with a series resistor $R_{B,ext}$, whose values depend on the lowest targeted frequency. By omitting R_{B1} and shorting C_{C} in Fig. 3-40, $R_{B,ext}$ just sees for low frequencies the parallel impedance of $Z_0/2$ and hence the root-spectral-density of the noise voltage referenced to ground at the input can be determined to

$$\sqrt{\overline{\left|\underline{v}_{n,\mathrm{P2}}\right|^2}} = \frac{\sqrt{4kTR_{B,ext}}}{1 + 2\frac{R_{B,ext}}{Z_0}}. \tag{3.117}$$

In equation (3.117) it becomes apparent that only the ratio of $R_{B,ext}$ to $Z_0/2$ affects the noise-voltage, showing its maximum at $R_{B,ext} = Z_0/2$. Choosing $R_{B,ext}$ smaller than roughly ten times Z_0 loads the input additional-

ly and consequently deteriorates RF operation. Therefore the maximum noise voltage on the gate-line is expected to be around 0.2 nV/$\sqrt{\text{Hz}}$ for $R_{B,ext} \approx 10 \cdot Z_0$.

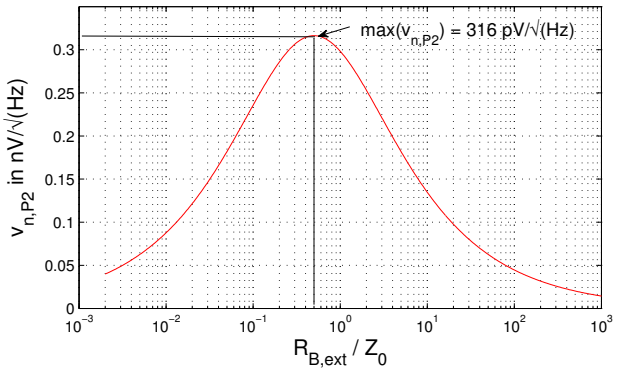


Fig. 3-51: $v_{n,\text{P2}}$ vs. $R_{B,ext}/Z_0$ of conventional biased TWA

NF Comparison of Conventional TWA and CCTWA Bias

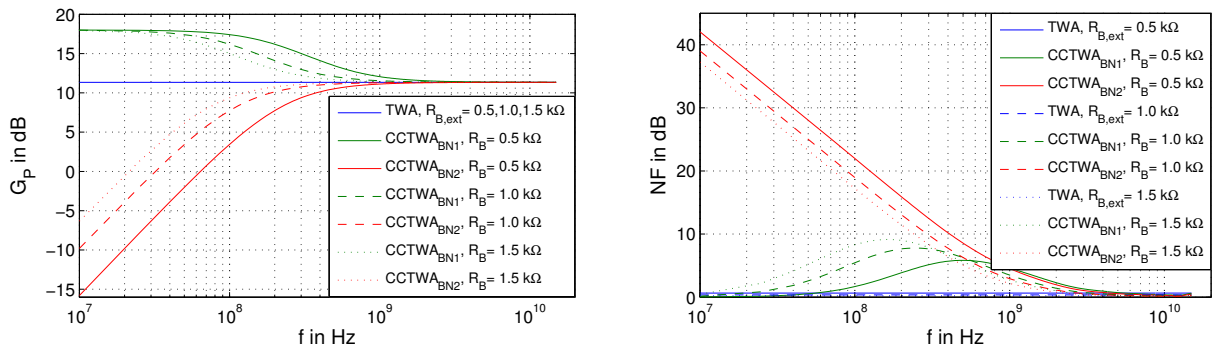
In order to obtain reasonable and comparable NF results the differences in biasing schemes have to be also accounted for in the power-gain calculations for BN1 and BN2, leading to the following gain expressions

$$G_{P,BN1} = \frac{(N \cdot g_m \cdot Z_0)^2}{4} \left|\underline{B}_{BN1}(\omega)\right|^2 \tag{3.118}$$

$$G_{P,BN2} = \frac{(N \cdot g_m \cdot Z_0)^2}{4} \left|\underline{B}_{BN2}(\omega)\right|^2. \tag{3.119}$$

With the aid of equations (3.118), (3.119) together with (3.114),(3.116) and by means of equations (3.109) and (3.82), the power gain (G_P) and noise-figure (NF) dependence on typical bias resistor values such as R_B = 0.5, 1.0 and 1.5 kΩ can be plotted for a 6-stage TWA and CCTWA. From Fig. 3-52 the main differences in G_P for BN1 and BN2 emanate. Since C_C in BN1 is bypassed at low frequencies the voltage divider formed by C_C and C_GS strives for the transfer magnitude of one. In return in BN2, C_GS is bypassed by R_B bringing the transfer magnitude down to zero. The lower corner frequency is at the same time dependent on R_{Bx} and shifts with increasing values to lower frequencies. In Fig. 3-52 (b) it can be clearly seen that the NF for BN1 exhibits a bump, which is the result from the increasing noise-voltage $\underline{v}_{\text{n,P2}}$ toward low frequencies (see Fig. 3-48) and the increasing G_P from Fig. 3-52 (a). Choosing smaller values for R_{B1} reduces the maximum NF, but on the same time shifts the slope toward higher frequencies and more importantly limits the maximum obtainable bandwidth of the TWA, which is not shown here. The NF for BN2 simply rises steadily due to the gain drop, in which R_{B2} determines the lowest frequency of operation.

For the case of no capacitive gate-coupling, the NF stays flat toward low frequencies and does not significantly change with R_B. Hence, it can be inferred that capacitive gate-coupling has to be avoided to obtain optimum low frequency noise performance.



(a) (b)

Fig. 3-52: Computed (a) G_P and (b) NF of conventional TWA and CCTWA with BN1 & BN2 (N = 6)

Overall Noise Factor & Noise Figure of CCTWA

In the final step, the noise-factor F of the CCTWA can be calculated by means of summation of all uncorrelated noise sources at the output. With (3.94), (3.96), (3.99), (3.102), (3.103) and (3.109), equation (3.82) finally yields

$$
\begin{aligned}
F = 1 \; &+ M_{R_G}\left(\frac{\sin(N\cdot\beta l)}{N\cdot\sin(\beta l)}\right)^2 && (N_{R_G})\\
&+ M_{R_D}\frac{4}{(g_m N Z_0)^2\left|\underline{B}_{BNX}(\omega)\right|^2} && (N_{R_D})\\
&+ \frac{4(\omega C_{GS})^2 R|Z_G(\omega)|^2}{g_m N^2 Z_0\left|\underline{B}_{BNX}(\omega)\right|^2}\sum_{k=1}^{N} f_{BNx}(k,\beta l) && (N_{iG})\\
&+ \frac{4P}{N g_m Z_0\left|\underline{B}_{BNX}(\omega)\right|^2} && (N_{iD})\\
&+ M_{BNX}\frac{4R_B\left|\underline{H}_{BNX}(\omega)\right|^2}{N^2 Z_0\left|\underline{B}_{BNX}(\omega)\right|^2}\sum_{k=1}^{N} f_{BNx}(k,\beta l) && (N_{BN})
\end{aligned}
\qquad (3.120)
$$

In (3.120), $Z_S = Z_L$ and M_X describes the excess temperature ratio between on-chip temperature T_{OC_X} ($T_{\mathrm{OC}} > T_{\mathrm{A}}$) and ambient temperature T_A (usually T_A= 290 K), which can either be approximated by experienced estimation or thermal simulations.

$$
M_X = \frac{T_{\mathrm{OC}_X}}{T_A} \qquad (3.121)
$$

By simply leaving out the term $N_{\mathrm{R_D}}$ from the drain-termination in (3.120), the NF of nonuniform TWAs (NDPA) can be calculated in the same manner. This is based on the fact that not only the noise contribution increases by 3 dB but also the power gain G_P, giving the same NF results.

Remarks and Trade-Offs

One assumption silently agreed to and not mentioned yet is the influence of the difference in quality factor Q of the intrinsic capacitance C_{GS} of the HEMT and the coupling capacitance C_{C}, which might take effect especially at low frequencies. Since C_{GS} results from the Shottky-junction at the gate and C_{C} is typically a well defined MIM-capacitance , their parasitic shunt-resistances are different, affecting capacitive voltage division toward lower frequencies. Usually, the quality factor of C_{GS} is much lower than the one of C_{C}, leading to a smaller control voltage of the HEMT at low frequencies and thus ending up in a gain drop. One countermeasure to keep the gain constant is to use a combination of the bias networks BN1 and BN2 from Fig. 3-49 in order to shunt the resistive voltage divider provided by the parasitic shunt resistances with the downside of frequency independent loss, which gives rise to slightly reduced gain performance. If both BNs are applied $\underline{Z}_{\mathrm{G}}(\beta)$ and $\underline{Z}_T(\beta)$ change to

$$\underline{Z}_{\mathrm{G}}(\omega) = \frac{1}{\frac{1+j\omega C_{\mathrm{GS}}R_{B2}}{R_{B2}} + \frac{1+j\omega C_{\mathrm{C}}R_{B1}}{R_{B1}+\frac{Z_0}{2}(1+j\omega C_{\mathrm{C}}R_{B1})}} \tag{3.122}$$

and

$$\underline{Z}_T(\omega) = \underline{Z}_{\mathrm{G}}(\omega) \cdot \underline{A}_{\mathrm{BN1}}(\omega) \cdot \underline{B}_{\mathrm{BN1,2}}(\omega) \tag{3.123}$$

with $\underline{A}_{\mathrm{BN1}}(\omega)$ being the same transfer function from BN1 in equation (3.123) and $\underline{B}_{\mathrm{BN1,2}}(\omega)$ being equal to

$$\underline{B}_{\mathrm{BN1,2}}(\omega) = \frac{1}{1+\frac{R_{B1}}{R_{B2}}\frac{1+j\omega C_{\mathrm{GS}}R_{B2}}{1+j\omega C_{\mathrm{C}}R_{B1}}}. \tag{3.124}$$

Since $\underline{B}_{\mathrm{BN1,2}}(\omega)$ expresses the voltage division produced by the now loaded capacitive voltage divider formed by C_C and C_{GS}, the power-gain G_P is also controlled by $\left|\underline{B}_{\mathrm{BN1,2}}(\omega)\right|^2$. Now, the ratio of R_{B1} to R_{B2} determines the DC-gain, which has to be set equal to

$$\frac{R_{B2}}{R_{B1}} = \frac{C_C}{C_{\mathrm{GS}}}. \tag{3.125}$$

to maintain low frequency gain-flatness down to DC. For the chosen gain of G_P = 10 dB, the assumed ratio of (3.125) equals roughly 0.588. For this ratio, the NF is plotted once again for comparison of all BNs, including now the BN compromise of BN1 plus BN2.

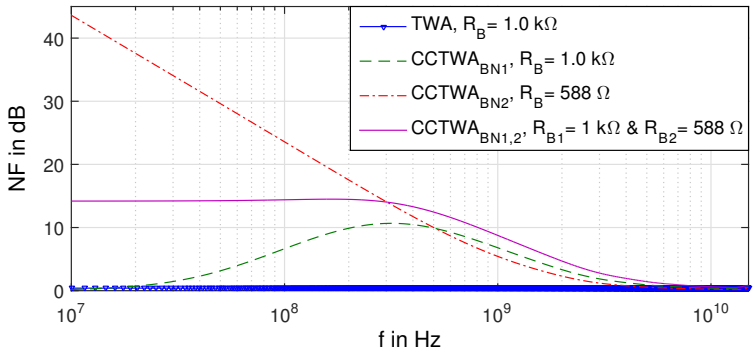


Fig. 3-53: NF of TWA & CCTWA with BN1, BN2 and BN1+BN2

It can be seen from Fig. 3-53 that the NF for the case of BN1 plus BN2 rises up to higher values than it is the case for BN1 or BN2 due to the fact that the effective noisy bias resistance is higher, but stays flat below the maximum NF of BN1 is reached.

3.4.4 TWA Design Criteria

This section shall provide some insight into the typical design procedure of TWAs and the corresponding trade-off between small-signal matching and output power maximization. The two most stringent design parameters from Table 1-1 in chapter 1.1 are the multi-decade bandwidth with an I/O-RL of larger than 10 dB and a maximum output power of $>$ 36 dBm over the whole frequency range from DC-6 GHz, DC-15 GHz or DC-20 GHz, respectively. Starting with the minimum I/O-RL constraint imposes an important restriction to the minimum and maximum characteristic loaded gate- and drain-line impedances ($Z_{0GL/0DL}$) in the TWA design, where $Z_{0GL/0DL}$ has to be in the range of

$$26\ \Omega < Z_{0GL,0DL} < 96\ \Omega. \tag{3.126}$$

in order to fulfill

$$S_{11/22} = \pm 0.316 \equiv -10\ \text{dB}, \tag{3.127}$$

assuming a 50 Ω impedance environment. Under the simplified assumption of no losses, equations (3.76) and (3.77) for the artificial gate- and drain-line impedances in a TWA become equal to

$$Z_{0GL/0DL} = \sqrt{\frac{L_{G/D}}{C_{G/D} + C_{IN/OUT}}}, \tag{3.128}$$

where $C_{IN/OUT}$ represents the capacitive loading of the gate- and drain-lines by the effective input and output capacitance of the HEMTs and $L_{G/D}$ and $C_{G/D}$ are the inductance and capacitance of the MSL with length $l_{\mathrm{G/D}}$, which can be approximated for $l_{G/D} < \lambda_{G/D}/10$ by

$$L_{G/D} = \frac{l_{G/D}}{v_{ph}} Z_{0G/0D} \tag{3.129}$$

$$C_{G/D} = \frac{l_{G/D}}{v_{ph}} \frac{1}{Z_{0G/0D}}. \tag{3.130}$$

$Z_{0G/0D}$ in (3.129) and (3.130) is the characteristic unloaded gate-/drain-line impedance defined by the inductance and capacitance per unit length of the MSL alone, according to

$$Z_{0G/0D} = \sqrt{\frac{L_{G/D}{}'}{C_{G/D}{}'}}. \tag{3.131}$$

The phase velocity can be also expressed by the distributed reactances of the MSL or the effective dielectric constant of the substrate

$$v_{ph} = \left(\sqrt{L_{G/D}{}' C_{G/D}{}'}\right)^{-1} = \frac{c_0}{\sqrt{\varepsilon_{eff}}} \tag{3.132}$$

Insertion of (3.129), (3.130) and (3.132) into (3.128) and solving for $l_{G/D}$ results in the necessary gate- and drain-line lengths for a targeted impedance environment of

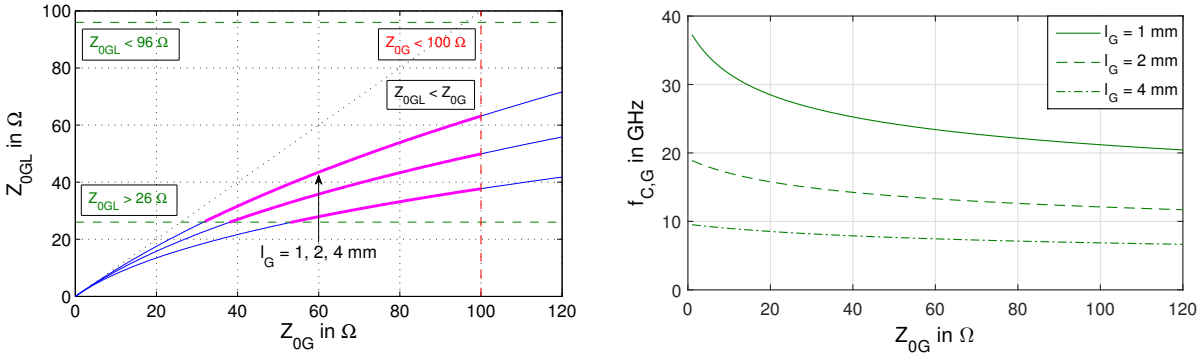
$$l_{G/D} = \frac{Z_{0G/0D}}{\left(\frac{Z_{0G/0D}}{Z_{0GL/0DL}}\right)^2 - 1} \cdot C_{IN/OUT} \cdot \frac{c_0}{\sqrt{\varepsilon_{eff}}}. \tag{3.133}$$

With the aid of (3.128) and the effective dielectric constant ε_{eff} of the MSLs in the utilized GaN technology ([104] – chapter 3.8), it is now possible to find the appropriate gate- and drain-line lengths in terms of the desired I/O-matching performance for a given capacitive loading ($C_{IN/OUT}$) of the MSL. It is important to keep in mind that to end up in conctructive interference of the traveling-waves at the output, the wave propagation constants within each section have to be identical ($\beta_G = \beta_D$). Therefore, assuming no loss and negligible capacitance per unit length of the MSLs ($C_{G,D}{}' \ll C_{\mathrm{GS/DS}}/l_{G/D}$), (3.80) and (3.81) can be further simplified, giving the following necessary condition (3.134) between the input capacitance and output capacitance in a TWA.

$$\frac{L_D{}' l_G}{L_G{}' l_D} = \frac{C_{IN}}{C_{OUT}}. \tag{3.134}$$

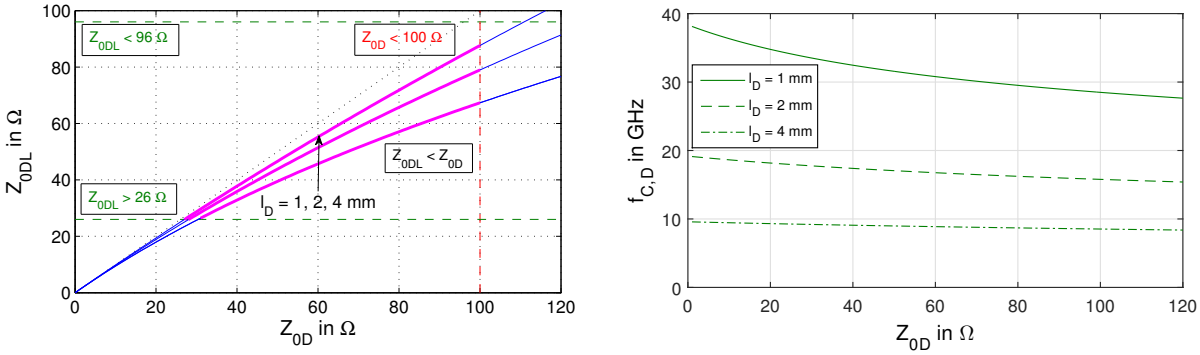
As a result, in order to find the corresponding length of the MSLs, the characteristic gate- and drain-line impedance (or capacitance and inductance per unit length) of the unloaded MSL needs to be known a priori, which can be obtained either by commercially available TLine calculators or by looking up the corresponding equations in [104]. For a more detailed visualization of the dependency between loaded ($Z_{0GL/0DL}$) and unloaded

($Z_{0G/0D}$) characteristic line impedances, a W_G = 0.3 mm HEMT with C_{IN} = 0.5 pF and C_{OUT} = 0.1 pF is considered. By solving (3.128) for Z_{0GL} and plotting it versus Z_{0G} for different l_G in Fig. 3-54 (a) allows to determine the optimum value for Z_{0G} and l_G, at which the loaded line impedance Z_{0GL} is close to 50 Ω in order to end up in the best matching condition.



(a) (b)

Fig. 3-54: (a) loaded gate-line impedance (Z_{0GL}) vs. characteristic microstrip gate-line impedance (Z_{0G}) for different gate-line lengths (l_G) of 1,2 and 4 mm and (b) corresponding dependence of the gate-line cut-off frequency ($f_{c,G}$) on Z_{0G} (C_{IN} = 0.5 pF)



(a) (b)

Fig. 3-55: (a) loaded drain-line impedance (Z_{0DL}) vs. characteristic microstrip drain-line impedance (Z_{0D}) for different drain-line lengths (l_D) of 1,2 and 4 mm and (b) corresponding dependence of the drain-line cut-off frequency ($f_{c,D}$) on Z_{0D} (C_{OUT} = 0.1 pF)

From Fig. 3-54 (a) it becomes apparent that this results in a trade-off between Z_{0G} and l_G. In order to stay within the input matching limitation for Z_{0GL} presented in (3.126), l_G cannot be made arbitrarily small without violating the matching condition of 10 dB. But as Fig. 3-54 (b) shows, minimizing l_G is crucial to push the cut-off frequency $f_{c,G}$ of the gate-line above the targeted maximum operational frequency of 15 GHz or 20 GHz, respectively. Increasing Z_{0G} close to 100 Ω instead helps to maintain a sufficiently high $f_{c,G}$ in combination with optimum input matching at the same time. Values in excess of 100 Ω for Z_{0G} are physically not realizable based on the manufacturing constraints for MSL-width below w_{MSL} = 10 µm. Taking a closer look at Fig. 3-55 (a) shows that the deviation between Z_{0D} and Z_{0DL} is much smaller due to the lower capacitive loading caused by the much smaller output capacitance C_{OUT} of the HEMT. Based on the weaker influence of C_{OUT} on Z_{0DL},

smaller line impedances (Z_{0D}) than for the gate-line (Z_{0G}) can be selected, which plays to the handling of higher current-densities on the drain-line of the TWA. As Fig. 3-55 (b) depicts, the smaller output capacitance C_{OUT} leads also to higher cut-off frequencies $f_{c,D}$ of the drain-line compared to the gate-line in Fig. 3-54 (b). This shows that the bandwidth limitation in TWAs is in general dominated by $f_{c,G}$ rather than by $f_{c,D}$. This coherency puts an additional upper limit on the HEMT´s maximum allowable input capacitance C_{IN} for each stage in the TWA design.

Based on the second constraint from the maximum output power specification it is crucial to choose a total gate-width of $TGW \geq 2$ mm to achieve $P_{sat} > 36$ dBm, if an average output power density of around 2 W/mm is assumed. This ends up in an estimated total input capacitance of at least $C_{IN,tot} \geq 3.4$ pF ($C_{\mathrm{GS}} \cong 1.8$ pF/mm) and a total output capacitance of $C_{OUT,tot} \geq 0.6$ pF ($C_{\mathrm{DS}} \cong 0.3$ pF/mm) for the GaN25 technology. Still, the exact capacitance per stage is dependent on the number of stages N chosen in the design. By the formulation given in (3.135) below, the optimum number of stages N_{opt} maximizing G_P given by (3.75) can be calculated according to the gate- and drain-line losses per section to (see also [97, 98])

$$N_{opt} = \frac{ln(a_D l_D / a_G\, l_G)}{a_D l_D - a_G l_G}. \tag{3.135}$$

(see also Appendix E.2 for derivation of (3.135)). Thus, knowledge of the exact values for a_G, a_D and l_G, l_D enables the designer to determine the optimum number of stages. The gate- and drain-line attenuations can be expressed in terms of the 3 dB corner frequency and a cut-off frequency of the artificial transmission lines, as in [97] and also as derived in equation (D.2.11) and (D.2.13) in Appendix D.1, by

$$\alpha_G = \frac{\omega^2/(\omega_G \omega_{c,G})}{\sqrt{1 + \left(\frac{\omega}{\omega_{c,G}}\right)^2 - \left(\frac{\omega}{\omega_G}\right)^2}} \tag{3.136}$$

$$\alpha_D = \frac{\omega_D/\omega_{c,D}}{\sqrt{1 - \left(\frac{\omega}{\omega_{c,D}}\right)^2}}, \tag{3.137}$$

with

$$\omega_{G/D} = \frac{1}{R_{IN/OUT} C_{IN/OUT}} \tag{3.138}$$

$$\omega_{c,G/c,D} = \frac{2}{\sqrt{L_{G/D}(C_{G/D} + C_{IN/OUT})}}. \tag{3.139}$$

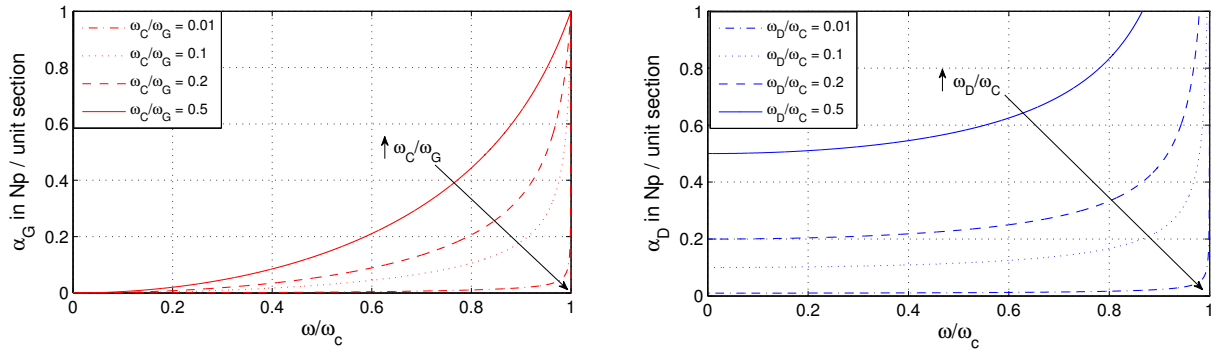


Fig. 3-56: (a) gate-line attenuation α_G and (b) drain-line attenuation α_D vs. normalized frequency ω/ω_c

The plots in Fig. 3-56 illustrate the dependency of α_G and α_D on the normalized frequency ω/ω_c for varying ω_G/ω_c and ω_c/ω_D-ratios. From Fig. 3-56 (b) it becomes evident that for reduced ω_D/ω_c-ratios the loss on the drain-line increases and does not vanish for $\omega \to 0$, as it is the case for the gate-line loss in Fig. 3-56 (a). The reason for this is the decreasing parallel output resistance R_{OUT}, which lowers the ω_D/ω_c-ratio and accordingly introduces higher losses. It is in general advantageous in the design of broadband TWAs to make use of GaN technology, which offers low input resistance and high output resistance to minimize losses. This means also translated to the device geometry point of view, the smaller the device the higher is the bandwidth. Unfortunately, in order to maintain the necessary total gate-width of e.g. a $TGW \geq 2$ mm, the number of stages N has to be increased proportionally. Hence N cannot be chosen arbitrarily high, since with decreasing device size the MSL losses become predominant from a certain point and are not negligible compared to the losses from the HEMTs anymore. At this point, going beyond a certain number of stages introduces more losses than the additional stages bring gain, since the gain-contribution of the stage to the TWA becomes lower than the attenuation.

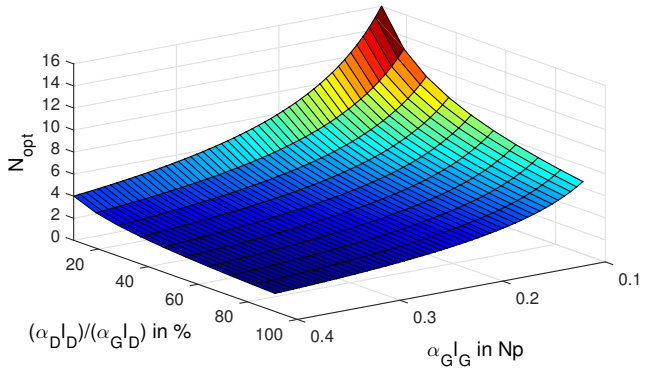


Fig. 3-57: Calculated optimum number of stages N_{opt} dependent on gate- and drain-line attenuation

In the last step by means of plotting N_{opt} vs. $a_G l_G$ and vs. $a_D l_D / a_G l_G$, as shown in Fig. 3-57 below, the optimum number of stages can be read from the graph, after determining the attenuation on the gate- and drain-line. It is important to note that the mentioned TWA design criteria always refer to the distributed nature of the artificial gate- and drain line, where the loading of the MSLs by the HEMTs is assumed to be "smeared" over the length of the MSL in one single section. This is only true as long as the cut-off frequency of the artificial

loaded transmission lines is far away from the highest frequency of operation of the TWA. Since this is not always the case in real designs, the unloaded MSLs become periodically loaded toward the highest frequency and the simplified before made distributed assumptions are not valid anymore.

Recommended TWA Design Approach

1. Calculate gate- and drain-line impedance range for targeted I/O-matching, as in (3.137) and take the lower impedance value.
2. Choose C_{IN} and L_G in such a way, that the minimum matching requirement from 1. for the loaded gate-line is fulfilled by $Z_{0,GL} = \sqrt{L_G/C_{IN}}$. Make sure that at the same time $\omega_{c,G}$ in (3.139) is larger than at least $5 \cdot \omega_{3dB}$. Afterwards, do the same for the drain-line.
3. Determine l_G and l_D based on the calculated L_G and L_D values from 2. by means of a TL-calculator or (3.129) and (3.133).
4. By means of the value for C_{IN} from 2., the initial device size W_G for a single cell can be derived via the C_{GS}/mm-ratio of 1.8 pF/mm in the applied GaN25 technology.
5. Select the best device geometry (NGF, GW) for W_G by comparison of the different MAG-plots, giving the most promising gain performance at the upper frequency corner of the TWA design.
6. Calculate the initial number of stages N by means of the targeted P_{sat} under the assumption of roughly 2-2.5 W/mm for the applied GaN25 technology. If the simulated small-signal performance does not meet the specifications, gain flatness and BW can be tuned by adding series gate-capacitors in order to reduce C_{IN} by the so formed capacitive voltage divider.
7. Double-check total gate-width (TGW) based on the simulated small-signal (gain/matching) and large-signal (P_{sat}/P_{1dB}) performance and increase TGW if necessary under the constraint of maintaining a sufficiently good low frequency ORL, which is proportional to R_{DS} of the total device size.

Remark: From the analytical expression derived in (3.120) in the foregoing chapter 3.4.3 and as will be shown later in chapter 4.4 it emerges that with increasing number of stages N the broadband noise decreases and the linearity improves in a TWA. It is therefore in terms of low-noise and high linearity performance desirable to select the highest possible number of stages for the design.

3.4.5 DC – 15/20 GHz Traveling-Wave Amplifier Designs

This section presents the designs of a DC-15 GHz and DC-20 GHz TWA in the 0.25µm GaN on SiC technology from Fraunhofer IAF. For the former design two different topologies, namely uniform and nonuniform, have been implemented to end up in a realistic assessment of the resulting differences in performance between these two topologies. Fig. 3-58 shows the photographs and schematics of the two DC-15 GHz TWAs. As an initial guess a power density of 2.0 W/mm was assumed for the broadband design, which was based on the non-optimum load-line matching of each stage in a TWA over frequency, giving a total device periphery of TGW = 2.0 mm to obtain a maximum saturated output power of 36 dBm. The choice for the device size of each cell is based on the targeted gain of 10 dB at 15 GHz, which is derived from the comparison of the MAG-curves versus frequency of different device sizes. After first simulations and still sufficient I/O-RL performance, TGW was further increased up to the final 2.4 mm.

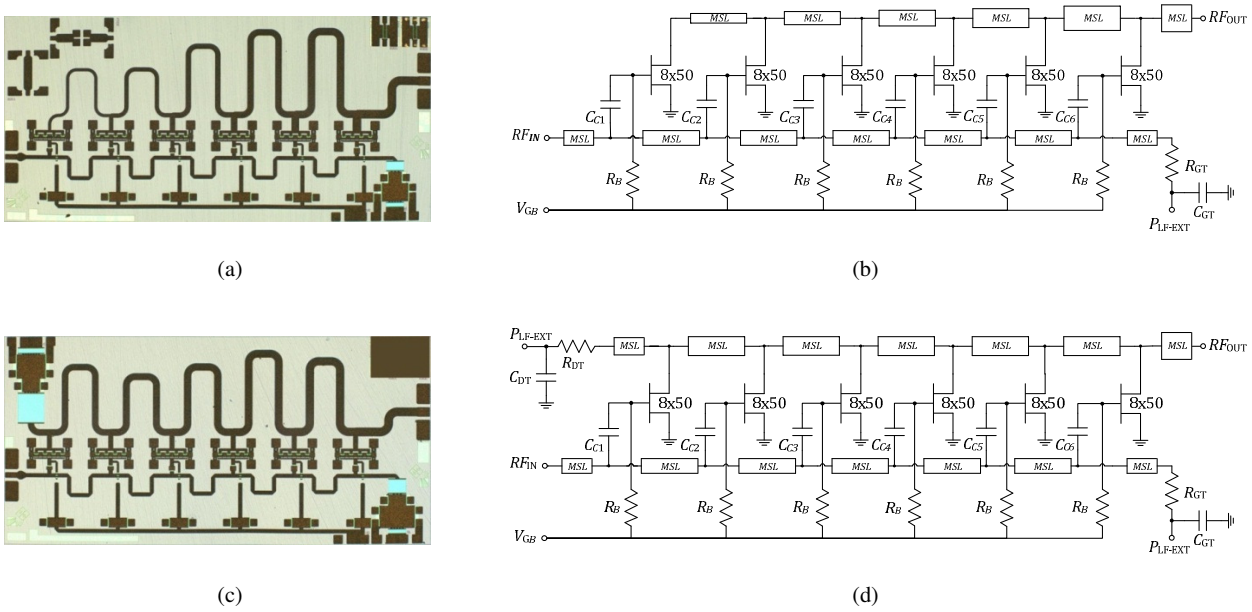


Fig. 3-58: Photograph of the DC-15 GHz (a) nonuniform (Nasu) GaN TWA with schematic in (b) and (c) uniform GaN TWA (Unzen) with schematic in (d)

As can be seen from Fig. 3-58, both designs consist finally of six equal stages with a total gate width of $W_{G,tot}$ = 2.4 mm. The overall device size resulted from the maximum obtainable output power under the constraint of achieving still a sufficiently good ORL of 8-10 dB toward DC. With respect to a proper choice for the optimum number of gate-fingers (NGF) and gate-width of the HEMT, for a constant device size a higher NGF might be preferable, since the extrinsic gate-contact resistance R_G reduces linearly with increasing NGF, leading to lower losses on the artificial gate-line of the TWA. This enables in turn the use of a higher number of stages, which might be preferable in terms of linearity again (see chapter 4.4). Moreover, it was in general shown by H. Fukui in [56] that the smaller the parasitics of the HEMT the lower is F_{min}. Accordingly choosing a higher number of gate fingers (NGF) might be advantageous in terms of noise due to the reduced R_G. The downside of a high NGF is, dependent on the structure of the gate-feed (as straight bus, taper or y-feed), the increased delay between the center finger and the outmost finger, which introduces distributed effects on the gate-bus. As long as the difference in electrical length of the sum of gate-bus and drain-bus between each gate-finger is smaller

than at least $\lambda/20$ of the highest targeted frequency of operation, distributed effects can be neglected as a rule of thumb. This is still valid for the 8×50µm device, which was also observed from the MAG-curve, making it the desired choice over its six finger counterpart.

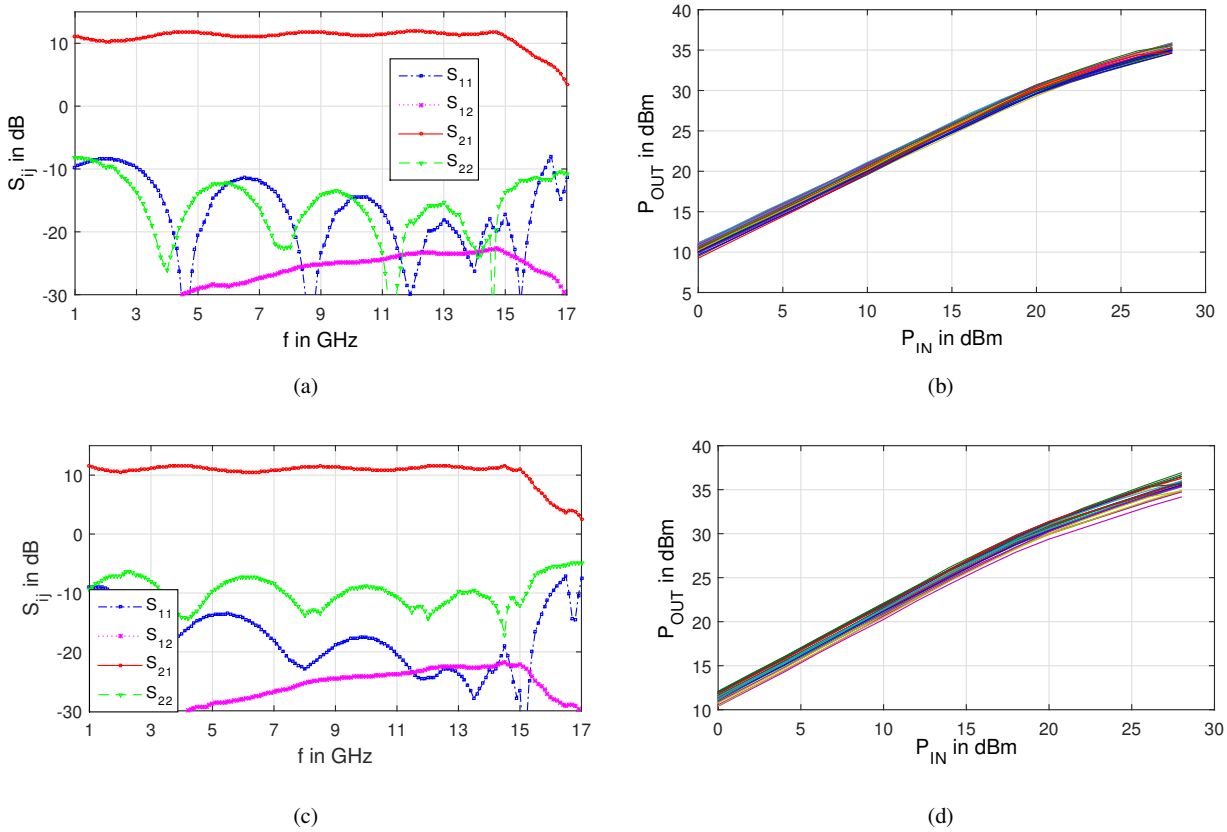


Fig. 3-59: On-wafer measured (a) S-Parameter vs. f and (b) P_{OUT} vs. P_{IN} of the DC-15 GHz uniform TWA (Unzen) and (c) S-Parameter vs. f and (d) P_{OUT} vs. P_{IN} of the DC-15 GHz nonuniform TWA (Nasu) for V_{DS} = 28 V and I_{DS} = 200 mA/mm

The graphs in Fig. 3-59 present the measured on-wafer S-parameters and P_{OUT} vs. P_{IN} curves of the uniform (Unzen) and nonuniform (Nasu) DC-15 GHz TWAs. Based on the limited BW towards DC, caused by the missing off-chip low frequency gate- and drain-line extensions, the on-wafer measurements were started from 1 GHz. The backside temperature was kept constant at 25°C during all measurements by a thermal chuck. From (a) and (b) it is clearly visible that both chips operate up to 15 GHz with a flat gain of larger than 10 dB and an almost equal S_{11} of better than 8 dB at low frequencies and 15 dB at high frequencies. From the valid assumption that the ORL at DC is determined by the total amount of output conductance, a maximum output conductance of $g_{DS,tot}$ = 20 mS would be sufficient to realize 10 dB ORL in case of the UDPA, whereas the NDPA would allow for $g_{DS,tot}$ = 40 mS due to the missing parallel 50 Ω drain dumping load. Translated to a total gate-periphery this would mean that TGW could be increased up to 4 mm in a UDPA design and even up to 8 mm in the NDPA design, taking the typical g_{DS} value of 5 mS/mm for the 0.25µm GaN process. According to this simplified consideration, the effective output power in a nonuniform TWA could be doubled under the same matching requirement of S_{22} = -10 dB. This is not fully true in reality, because C_{DS} grows also linearly with the device size, leading to decreased RF matching performance in the low GHz-range, as Fig. 3-59 (a) and (c) around 1-2 GHz indicate. The slightly higher gain ripple in the nonuniform design (Nasu) stems from the worse

S_{22} match opposed to the uniform design (Unzen), which is evoked by the absence of a drain-dumping load. By means of drain-line tapering (Fig. 3-58 (a)) the large load-mismatch present at the first stage is slightly mitigated, as already described in chapter 3.2.3, but cannot be fully compensated under compliance of the maximum current handling of the drain microstrip lines, giving $w > 20$ µm. Still, at 15 GHz an $I/O\text{-}RL$ of better than 10 dB was achieved in both designs. From the P_{OUT} vs. P_{IN} curves in (b) and (d) it becomes obvious that the uniform design (Unzen) exhibits less variance in terms of large-signal gain than the nonuniform design (Nasu), but provides slightly less output power due to the additional power losses in the drain-dumping load. Because of the limited input power of the driver PA, full saturation of the chips has not been reached during the measurement but is expected to be in the order of 36 dBm for P_{sat} with a corresponding P_{1dB} of 33 dBm. One possible way to further improve the output power of the nonuniform design (Nasu) would be the implementation of transistor tapering. By means of choosing a larger device size for the 1st HEMT the power match to the lower provided load impedance can be improved and thus the power contribution of the 1st HEMT raised, as also described in [78]. Since for the targeted application the ORL down to low frequencies is a critical design parameter, a further increase of the total active device size above $W_{G,tot}$ = 2.4 mm was not a viable option in terms of output matching.

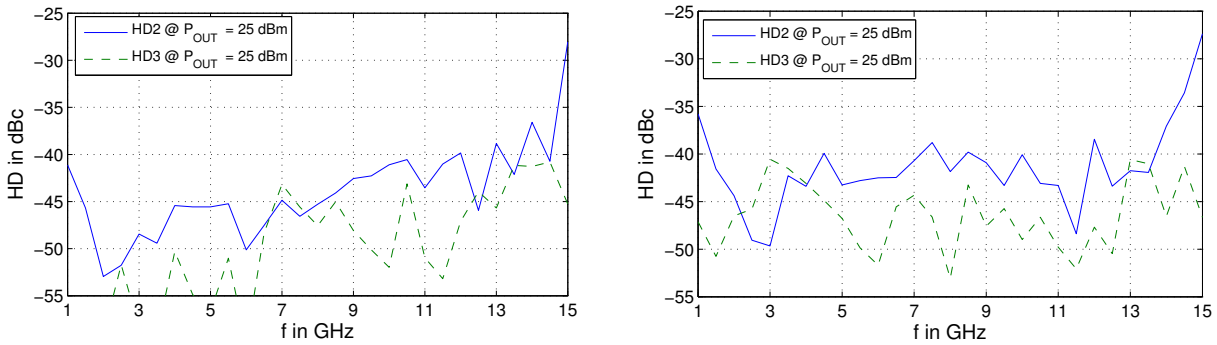
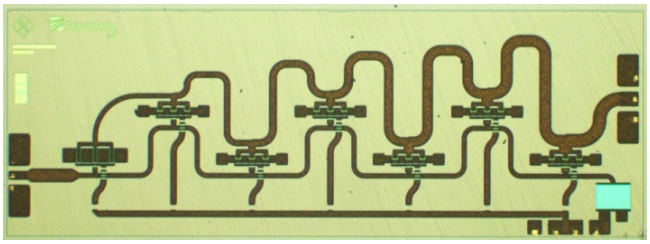
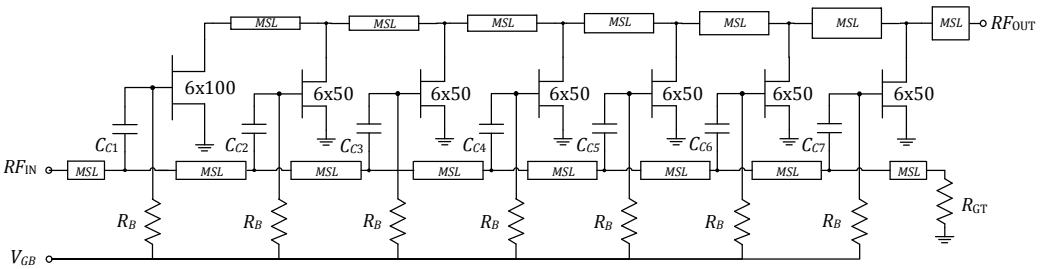


Fig. 3-60: On-wafer measured HD @ P_{OUT} = 25 dBm for (a) nonuniform (Nasu)and (b) uniform (Unzen) DC-15 GHz TWA at V_{DS} = 30 V and I_{DS} = 200 mA/mm

With respect to linearity, the HD was measured on-wafer at P_{OUT} = 25 dBm and is plotted in Fig. 3-60. Both MMICs exhibit an $HD2$ and $HD3$ of better than -40 dBc up to one-half and one-third of the band. It can be furthermore derived, that the nonuniform design (Nasu) in (a) behaves slightly superior in $HD2$ and $HD3$ up to midband. This is mainly based on the better loadline match of the transistor stages closer to the input in a nonuniform design opposed to the uniform design, where the load impedances vary more heavily over frequency. Especially around 3 GHz, a clear degradation in $HD3$ for the uniform design (Unzen) in (b) can be observed, which matches well with the strong mismatch / tilt of the 1st HEMT´s load-line, as already shown in Fig. 3-23 (b) in chapter 3.2.3. From these load-line considerations it is expected that the closer both PAs are biased to class A, the smaller will be the difference in HD-performance, since the mismatched load-lines start to clip at higher output powers. The increase in $HD2$ towards 1 GHz in both MMICs is deemed to be owed to the impedance variation of the directional coupler in the measurement setup, which had a frequency range from 1-18 GHz. Unfortunately in terms of limited time, there was no time left to measure the $OIP3$ performance of the TWAs.



(a)

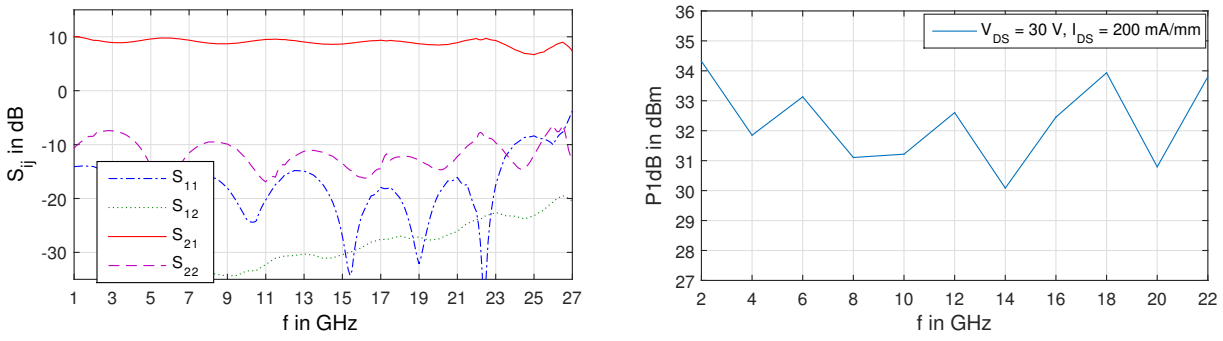


(b)

Fig. 3-61: (a) photograph of DC-20 GHz TWA MMIC (Numazawa) and (b) corresponding schematic

Fig. 3-61 depicts the chip photograph and schematic of a DC-20 GHz nonuniform TWA with $N = 7$ stages. In the design of the DC-20 GHz, the approach of transistor tapering according to [78] is applied for the 1st stage to obtain a better output power match and thus boost the total output power. By insertion of a 6×100µm individual source via (ISV) HEMT in the 1st stage, $W_{G,tot}$ could also be chosen to 2.4 mm, where the other six stages were designed uniformly with 6×50µm HEMTs. The positions of the HEMTs were chosen deliberately in a zig-zag shape in order to decrease thermal coupling. In this way, the distance between each device could be raised by a factor of $\sqrt{2}$, leading to lower maximum channel temperatures and in turn to an increased overall output power. The drawback of this approach might be founded in the higher EM-coupling between gate- and drain-line, which needs to be carefully taken into account by EM-simulations. As Fig. 3-62 (a) shows, the MMIC operates up to 20 GHz with a S_{21} of larger than 8 dB at the nominal bias condition of V_{DS} = 28 V and I_{DS} = 200 mA/mm. The extended frequency range up to even 26 GHz is found to be owed to differences in the small-signal model above 16 GHz on the one hand and to underestimated EM-coupling on the other hand. Again, the 2.4 mm total device periphery allows for a better ORL than 10 dB at DC, but the minimum ORL is found to be around 7 dB at 3 GHz.

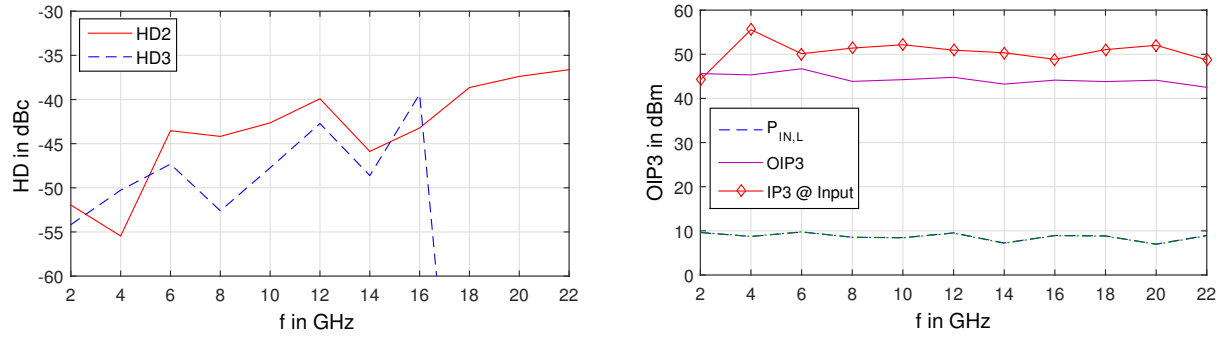
The large-signal measurements predict a $P1dB$ of larger than 31 dBm across the full band, with a notch of 30 dBm at 14 GHz for the very same class AB bias point as for the small-signal case. Unfortunately due to the extended frequency range of the design and its consequentially reduced stability, the MMIC could not fully be driven into saturation without starting to oscillate. Nevertheless, the small-signal and large-signal performance up to the $P1dB$ have been precisely reproducible over the whole wafer for different cells, showing that the design is stable under the given conditions.



(a) (b)

Fig. 3-62: (a) Measured on-wafer S-parameters and (b) $P1dB$ of DC-20 GHz TWA (Namazuwa) at V_{DS} = 30 V and I_{DS} = 200 mA/mm

Linearity measurements have proven that the design exhibits a high linearity with a HD < -40 dBc at P_{OUT} = 20 dBm and an $OIP3$ of greater than 44 dBm up to 20 GHz, which is deemed to be a remarkable linearity performance for a broadband TWA in a 0.25µm GaN technology, designed up to $2f_T/3$.

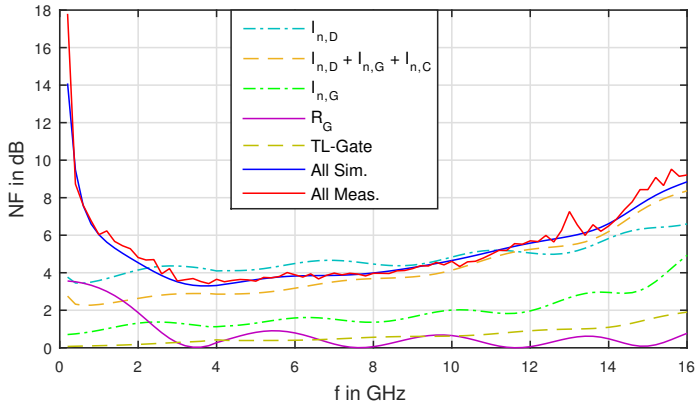


(a) (b)

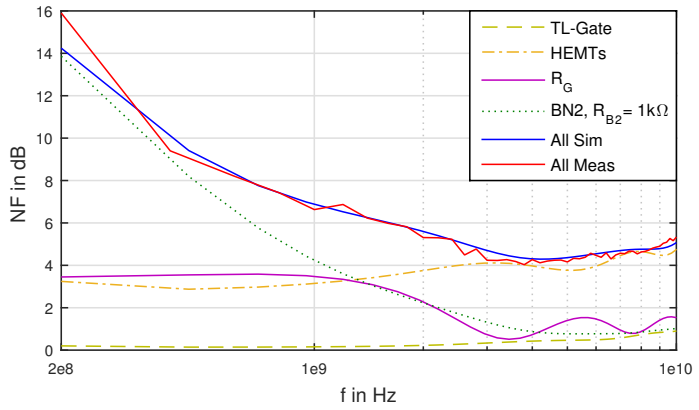
Fig. 3-63: On-wafer measured (a) HD vs. f @ P_{OUT} = 20 dBm and (b) $OIP3$ vs. f with Δf = 5 MHz for V_{DS} = 28 V and I_{DS} = 200 mA/mm of DC-20 GHz TWA (Namazuwa)

Last but not least, the NF of the TWAs is an important design parameter, according to the system requirements of the SGs described in Table 1-1. The NF of both TWAs, Unzen and Nasu, has been measured on-wafer for several bias points. Since section 3.4.3 revealed that both topologies behave equal in terms of their signal-to-noise ratio at the output, only the uniform TWA (Unzen) will serve in the following considerations as example to embrace the correlation between theory, simulation and measurement. Fig. 3-64 shows the comparison between the measured NF and the ADS back-fitted simulated NF, broken down into all the relevant noise contributors, which are identified and described in detail in section 3.4.3. For the bias point of V_{DS} = 28 V and I_{DS} = 100 mA/mm, the back-fitted simulated results in ADS and the on-wafer measurement match very well over the whole BW. The values for the PRC-model were finally determined for the best fit to P = 1.4, R = 0.63 and $\underline{c}$ = -j0.78, which are larger than the values extracted for the 8×50µm HEMT in chapter 2.2.1 due to impedance match variations in the real measured TWA design, which are not considered in the ideal mathematical noise analysis. Due to thermal heating of the passive components by the HEMTs during the NF measurement, the over-temperature factor M_x, which was defined in (3.121) in chapter 3.4.3, was back-fitted to physically meaningful values in the range between 2 to 4 (50-100°C). The logarithmic low frequency excerpt in (b) additionally

underlines the large influence of the 1 kΩ gate-bias resistor R_{B2} on the overall low frequency NF, which shorts the capacitive divider formed by C_C and C_{GS} at the gate and hence dumps the RF-signal toward low frequencies. Compared to R_{B2} a much smaller but still decisive noise contribution toward low frequencies comes from R_{GT}. If no capacitive gate-coupling is applied, R_{GT} is the dominant noise source due to the increasing reverse transfer function from the gate-termination toward the output toward DC, as already discussed in 3.4.3.



(a)



(b)

Fig. 3-64: Comparison between measured & ADS back-fitted simulated NF of the DC-15 GHz TWA (Unzen) at V_{DS} = 28 V and I_{DS} = 100 mA/mm

By analytical computation of the single noise contributors with the in chapter 3.4.3 derived equation (3.120), the ideal NF of each single noise source as well as the total sum of the DC-15 GHz UDPA (Unzen) without back-fitting of the noise model parameters is plotted in Fig. 3-65. By comparsion of Fig. 3-64 with Fig. 3-65 it can be seen that the analytically derived equations in (3.120) can serve as a useful tool within the design procedure of low noise TWAs. Before starting with exact simulations in ADS/AWR, the principle NF characteristic can be very well assessed, which helps in the preselection process of choosing the proper number of stages or the targeted HEMT cell size. Furthermore, noise models are often not applicable in the process design kits (PDK), provided by commercial foundries. Therefore, it is very beneficial to gain at least a very general

statement about the final NF characteristic, where it is often sufficient for a first guess to set the noise model parameters to typical textbook values.

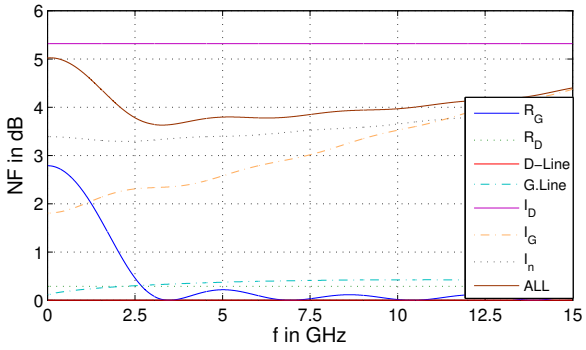


Fig. 3-65: Calculated NF separated by its contributors in the ideal DC-15 GHz TWA (Unzen), assuming a constant gain of G_P = 10 dB and an I/O-RL of 10 dB

3.4.6 Performance Improvement Measures

The influences of the gain shape over frequency have been considered up to now in terms of the attenuation constants α_G and α_D. Since the loss of the gate-line increases with frequency, as shown in section 3.4.4 in Fig. 3-56, the signal swing on the gate-line toward the gate termination decays over frequency. Mainly the losses introduced by the resistive parts of the transistors` input impedances add up from stage to stage and thereupon a drop in gain over frequency is observed. There are three general concepts to compensate for the gain degradation over frequency in a TWA, which will be discussed in the following.

Capacitive Coupled Gate Tapering

One very common remedy to compensate for the loss in signal amplitude toward the gate termination is tapering of the series gate-capacitors [95]. This is a very simple and effective approach, since it does not alter the layout structure to a greater extent. Using series capacitors in the gates of the transistor stages leads to a smaller effective capacitive loading of the gate-line [95]. Choosing

$$C_{\mathrm{S}} = m \cdot C_{\mathrm{GS}} \tag{3.140}$$

gives for the effective capacitance seen by the gate-line

$$C_{\mathrm{G},eff} = \frac{C_{\mathrm{S}} \cdot C_{\mathrm{GS}}}{C_{\mathrm{S}} + C_{\mathrm{GS}}} = \frac{m}{m+1} C_{\mathrm{GS}}. \tag{3.141}$$

By properly adjusting m, the resonance frequency of the gate-line, which is now equal to

$$f_{res} = \frac{1}{\pi \frac{m}{m+1} C_{GS} R_0}, \tag{3.142}$$

can be shifted to higher frequencies, allowing higher bandwidths in the TWA design. Whereas the bandwidth increases with $m/(m+1)$, the power gain drops by the square of this ratio. Consequently, gain can be traded off for bandwidth by adding a series gate capacitor.

Gate Line Tapering

A second approach is the tapering of the gate-lines toward the gate termination in order to reduce losses at high frequencies and accordingly to minimize the gain drop. Unfortunately, besides affecting the impedance level, the margin for loss reduction is constrained to the transmission line physical dimensions, which is compared to the transistor in III-V technology not the major initiator of loss.

Loss Compensation of Gate-Line

This leads to the third counteraction, where the loss introduced by the transistors gate and drain resistances is reduced by an optimized circuit. The intrinsic resistance R_{GS} of a HEMT represents the main source for gate-line losses. In a similar fashion as the effective input capacitance $C_{G,eff}$ was reduced by adding a series capacitor in front of each stage, adding a series impedance Z_{fs} at the source of the transistor reduces the value of R_{IN} seen by the gate-line and so increases ω_G, as also done in [105].

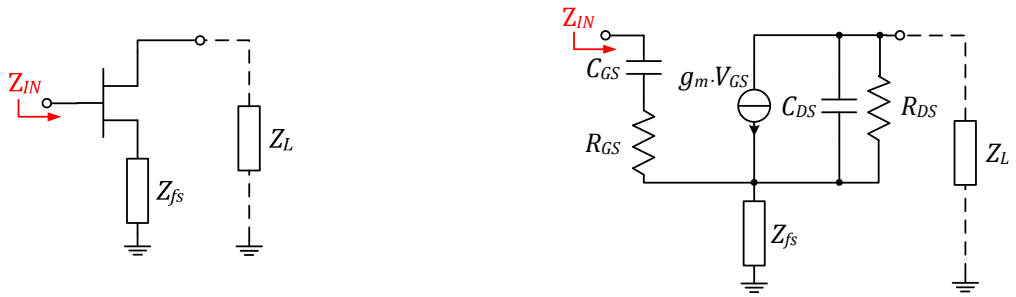


Fig. 3-66: Schematic of HEMT (a) with series feedback impedance Z_S (b) simplified equivalent small-signal circuit

The input impedance of the transistor can be then expressed by means of Fig. 3-66 (b) as

$$Z_{IN} = \left[Z_{GS} + Z_{fs} \left(1 + \frac{g_m}{j\omega C_{GS}} \left(1 - \frac{Z_L}{Z_L + Z_{DS}} \right) + \frac{Z_{GS}}{Z_L + Z_{DS}} \right) \right] \cdot \frac{Z_L + Z_{DS}}{Z_L + Z_{DS} + Z_{fs}}, \tag{3.143}$$

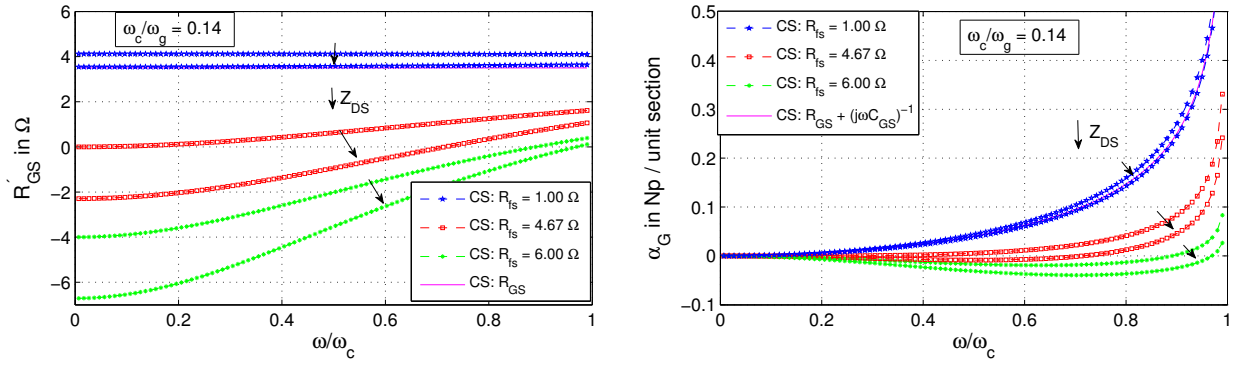
which simplifies for the assumption of $Z_{DS} >> Z_L, Z_{fs}, Z_{GS}$ to

$$Z_{IN} = Z_{GS} + Z_{fs} \left(1 + \frac{g_m}{j\omega C_{GS}} \right). \tag{3.144}$$

Now, if Z_{fs} consists of a parallel RC-network (R_{fs},C_{fs}), equation (3.144) gives for the compensated equivalent resistive part, further denoted as $R_{\mathrm{GS}}{}'$,

$$Re\{Z_{IN}\} = R_{\mathrm{GS}}{}' = R_{\mathrm{GS}} - \frac{R_{fs}}{1 + \left(\omega R_{fs} C_{fs}\right)^2}\left(R_{fs} C_{fs} \frac{g_m}{C_{\mathrm{GS}}} - 1\right). \tag{3.145}$$

As long as the condition $R_{fs}C_{fs} > C_{\mathrm{GS}}/g_m$ for the RC-time constant is guaranteed, $R_{\mathrm{GS}}{}' < R_{\mathrm{GS}}$ is always satisfied and thus the loss of the gate-line is reduced by the negative real-part incorporating R_{fs} and C_{fs}. Fig. 3-67 (a) shows the compensated real-part $R_{\mathrm{GS}}{}'$ over normalized frequency of a 6×50µm GaN CS-HEMT for $Z_{\mathrm{DS}} = \infty\ \Omega$ (see (3.145)) and for C_{DS} = 85 fF, R_{DS} = 580 Ω and Z_L = 50 Ω (see (3.143)). Fig. 3-67 (b) depicts the corresponding gate-line attenuation α_{G}, according to the equation already defined in (3.136). The cut-off frequency $\omega_{c,\mathrm{G}}$ of the gate-line loaded by a 6×50µm GaN HEMT is equal to 88.9 GHz, derived by the approximation of $\omega_{c,\mathrm{G}} = 2/\sqrt{L_{\mathrm{G}}C_{\mathrm{GS}}}$, with $L_{\mathrm{G}} = Z_{0,\mathrm{G}}{}^2 C_{\mathrm{GS}}$ and $Z_{0,\mathrm{G}}$ = 50 Ω. The corner frequency is equal to $\omega_g = 1/R_{\mathrm{GS}}C_{\mathrm{GS}} \approx 635$ GHz.



(a) (b)

Fig. 3-67: (a) Loss compensated R_{GS}' and (b) corresponding gate-line attenuation α_{G} for different R_{fs} of a CS-HEMT (W_{G} = 0.3 mm) with $C_{fs} = 5 \cdot C_{\mathrm{GS}}$ = 2.25 pF for $Z_{\mathrm{DS}} = \infty$ and for C_{DS} = 85 fF, R_{DS} = 580 Ω, Z_L = 50 Ω

Fig. 3-67 reveals that for Z_{DS} being finite and larger than Z_L, R_{GS}' becomes even more compensated the smaller the imaginary-part of Z_{DS} or the larger C_{DS} becomes. The reason can be found by taking a closer look onto the innermost parenthesis in (3.143). Supposed that Z_L is purely real, C_{DS} generates a negative imaginary-part which turns into a negative real-part by the multiplication with $g_m/j\omega C_{\mathrm{GS}}$. This compensating negative real-part is further increased by the multiplication with the real-part of Z_{fs}. Contrarily, the real-part of the innermost parenthesis, which is for DC equal to $R_{\mathrm{DS}}/(R_{\mathrm{DS}} + Z_L)$, becomes smaller with decreasing R_{DS} and thus counteracts after multiplication with $g_m/j\omega C_{\mathrm{GS}}$ and the imaginary-part of Z_{fs} the positive real-part compensation. A smaller R_{DS} and C_{DS} therefore increases R_{GS}', whereas a larger R_{DS} and C_{DS} leads to a stronger compensation.

Based on the just seen complexity of the full terms in (3.143), it is meaningful to stay with the approximation from (3.144). The denominator in (3.145) reveals that the product of $R_{fs}C_{fs}$ sets a corner frequency $\omega_{c,fs}$, where $R_{\mathrm{GS}}{}'$ starts to converge to the value of R_{GS} and becomes for $\omega = \omega_{c,fs}$ equal to

$$R_{\mathrm{GS}}{}'(\omega_{c,fs}) = R_{\mathrm{GS}} - \frac{R_{fs}}{2}\left(\frac{g_m}{\omega_{c,fs}C_{\mathrm{GS}}} - 1\right). \tag{3.146}$$

It can be inferred from equation (3.145) that for smaller R_{GS} values the feedback resistor R_{fs} can be chosen likewise smaller in order to achieve the same loss compensation towards lower frequencies. Towards higher frequencies the corner frequency $\omega_{c,fs} = 1/R_{fs}C_{fs}$ cannot be shifted up arbitrarily to improve loss compensation, since small values for C_{S} enforce R_{S} to be unreasonably large in order not to violate the condition $R_{fs}C_{fs} > C_{\mathrm{GS}}/g_{\mathrm{m}}$. Hence, the gain is reduced significantly by the negative feedback. Conversely, choosing R_S very small to maintain optimal gain performance enforces C_{fs} to be very large, which translates into a large-scale geometry for an on-chip MIM-capacitor. Out of this reason a certain upper and lower bound is defined, restricting the free choice for R_{fs} and C_{fs} to meaningful values. For the presented HEMT with W_{G} = 0.3 mm the ratio $C_{\mathrm{GS}}/g_{\mathrm{m}}$ is equal to 6 ps, which results for e.g. for a reasonable value of C_{fs} = 3 pF in R_{fs} > 2 Ω. Furthermore from equation (3.145) or Fig. 3-67 it can be derived that by selecting

$$R_{fs} > \frac{1}{2 \cdot \zeta \cdot g_m} + \sqrt{\frac{1}{4(g_m\zeta)^2} + \frac{R_{\mathrm{GS}}}{g_m\zeta}}, \tag{3.147}$$

where $\zeta = C_{fs}/C_{\mathrm{GS}}$, negative values for $R_{\mathrm{GS}}{}'$ result. A slightly negative value for $R_{\mathrm{GS}}{}'$ might still be acceptable or even desired if additional loss from the on-chip gate-lines, as e.g. lossy MSL or GCPW, of the TWA is beard in mind. In order to avoid the possibility of instabilities, $R_{\mathrm{GS}}{}'$ should be designed to be close to zero, but still positive.

Loss Compensation of Drain-Line

For the drain-line on the contrary, based on the parallel RC-output impedance, it is important to increase R_{DS} and so decrease ω_D in order to avoid loading of the artificial drain line. A good solution to this problem is the implementation of cascodes [106], where the real-part of the output impedance $Z_{OUT,CC}$ of the cascode is decreased due to the series connected negative output impedance of the common-gate (CG) HEMT. After a series to parallel transformation of $Re\{Z_{OUT,CC}\}$, the effective $R_{\mathrm{DS}}{}'$ of an equivalent common-source transistor is thus larger in a cascode than R_{DS} of a single CS-HEMT.

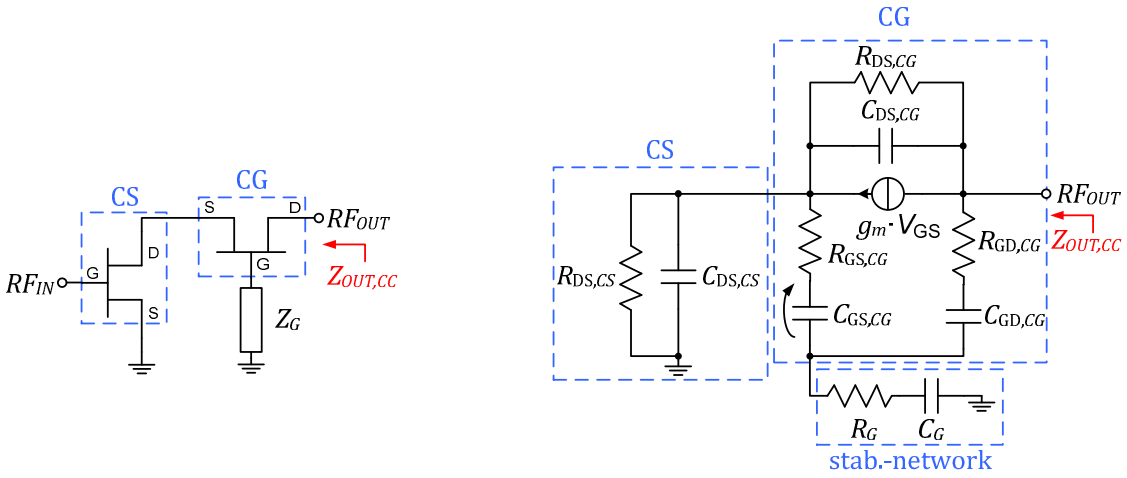


Fig. 3-68: Schematic of (a) Cascode configuration and (b) small-signal approximation of cascode for output impedance calculation

By straightforward analysis of the simplified small-signal equivalent circuit from Fig. 3-68 (b), the output impedance of the cascode can be calculated to

$$Z_{OUT,CC} = \frac{Y_{11,CG} + Y_{\mathrm{DS},CS}}{\Delta Y_{CG} + Y_{22,CG} Y_{\mathrm{DS},CS}}, \tag{3.148}$$

with

$$Y_{11,CG} = Y_{\mathrm{DS},CG} + \frac{Y_{\mathrm{GS},CG} \cdot \left(Y_G + Y_{\mathrm{GD},CG}\right)}{Y_{\mathrm{GS},CG} + Y_G + Y_{\mathrm{GD},CG}} \left(1 + \frac{g_m}{j\omega C_{\mathrm{GS},CG}}\right) \tag{3.149}$$

$$Y_{12,CG} = -\left(Y_{\mathrm{DS},CG} + \frac{Y_{\mathrm{GS},CG} Y_{\mathrm{GD},CG}}{Y_{\mathrm{GS},CG} + Y_G + Y_{\mathrm{GD},CG}} \left(1 + \frac{g_m}{j\omega C_{\mathrm{GS},CG}}\right)\right) \tag{3.150}$$

$$Y_{21,CG} = -\left(Y_{\mathrm{DS},CG} + \frac{Y_{\mathrm{GS},CG} Y_{\mathrm{GD},CG}}{Y_{\mathrm{GS},CG} + Y_G + Y_{\mathrm{GD},CG}} \left(1 + \frac{g_m}{j\omega C_{\mathrm{GS},CG}} \left(1 + \frac{Y_G}{Y_{\mathrm{GD},CG}}\right)\right)\right) \tag{3.151}$$

$$Y_{22,CG} = Y_{\mathrm{DS},CG} + \frac{Y_{\mathrm{GS},CG} Y_{\mathrm{GD},CG}}{Y_{\mathrm{GS},CG} + Y_G + Y_{\mathrm{GD},CG}} \left(1 + \frac{g_m}{j\omega C_{\mathrm{GS},CG}} + \frac{Y_G}{Y_{\mathrm{GS},CG}}\right) \tag{3.152}$$

and $\Delta Y_{CG} = Y_{11,CG} Y_{22,CG} - Y_{21,CG} Y_{12,CG}$. $Y_{\mathrm{DS},CS}$ in (3.148) is the output admittance of the CS-HEMT and the stabilizing admittance Y_G comprises the series connection of R_G and C_G. Further simplifying the expression of (3.148) under the condition of $Y_G = \infty$ S, $Y_{GD} = 0$ S and $Y_{\mathrm{DS},CS} = 0$ S yields the output impedance of the idealized CG-HEMT only, which is equal to

$$Z_{OUT,CC} = R_{\mathrm{GS}} + \frac{1}{j\omega C_{\mathrm{GS}}} + \frac{R_{\mathrm{DS}}}{1 + j\omega C_{\mathrm{DS}} R_{\mathrm{DS}}}\left(1 + \frac{g_m}{j\omega C_{\mathrm{GS}}}\right). \tag{3.153}$$

The real-part of (3.153) gives accordingly

$$Re\{Z_{OUT,CC}\} = R_{\mathrm{GS}} - \frac{R_{\mathrm{DS}}}{1 + (\omega C_{\mathrm{DS}} R_{\mathrm{DS}})^2}\left(g_m R_{\mathrm{DS}} \frac{C_{\mathrm{DS}}}{C_{\mathrm{GS}}} - 1\right). \tag{3.154}$$

The last term in (3.154) is the only term containing the active transconductance g_m and hence is able to provide a negative real-part, which cancels partly the real-part of the passive elements. Possible instabilities might arise for the case when the real-part of $Z_{OUT,CC}$ becomes negative. In order to stay within the stable region g_m has to satisfy the condition

$$g_m < \frac{C_{\mathrm{GS}}}{R_{\mathrm{DS}} C_{\mathrm{DS}}}\left(\frac{R_{\mathrm{GS}}}{R_{\mathrm{DS}}}\xi(\omega) + 1\right), \tag{3.155}$$

with $\xi(\omega) = 1 + (\omega C_{\mathrm{DS}} R_{\mathrm{DS}})^2$. As soon as g_m becomes significantly larger than the right-hand side of the inequality in (3.155) and overcompensates the loss from the drain-line of the TWA, instabilities might arise. The condition (3.155) is very conservative and is relaxed for $Z_{\mathrm{DS},CS}$ being finite.

In a final step the equivalent resistance $R_{\mathrm{DS}}{}'$ can be computed by means of a series to parallel transformation of $Z_{OUT,CC}$. Splitting of (3.153) into $Re\{Z_{OUT,CC}\}$ and $Im\{Z_{OUT,CC}\}$ leads to the equivalent resistance in parallel configuration of

$$R_{\mathrm{DS}}{}' = \frac{Re\{Z_{OUT,CC}\}^2 + Im\{Z_{OUT,CC}\}^2}{Re\{Z_{OUT,CC}\}}, \tag{3.156}$$

which ends up for $Y_{\mathrm{DS},CS}$ = 0 S in the full expression of

$$R_{\mathrm{DS}}{}' = \underbrace{R_{\mathrm{GS}} + \frac{R_{\mathrm{DS}}\left(1 - g_m R_{\mathrm{DS}} \frac{C_{\mathrm{DS}}}{C_{\mathrm{GS}}}\right)}{\xi(\omega)}}_{Re\{Z_{OUT,CC}\}} - \frac{\left(\frac{1}{\omega C_{\mathrm{GS}}}\left(1 + \frac{g_m R_{\mathrm{DS}}}{\xi(\omega)}\right) + \frac{\omega C_{\mathrm{DS}} {R_{\mathrm{DS}}}^2}{\xi(\omega)}\right)^2}{\frac{R_{\mathrm{DS}}\left(g_m R_{\mathrm{DS}} \frac{C_{\mathrm{DS}}}{C_{\mathrm{GS}}} - 1\right)}{\xi(\omega)} - R_{\mathrm{GS}}}. \tag{3.157}$$

The first two terms in (3.157) itself represent the real-part of $Z_{OUT,CC}$, whereas the last term incorporates the series to parallel transformation. For low frequencies latter term is dominant and strives for DC toward -∞, showing that the reverse voltage drop over C_{GS} causes a current flowing toward the output port in Fig. 3-68 (b). Fig. 3-69 depicts $R_{\mathrm{DS}}{}'$ for different values of g_m over normalized frequency for (a) (3.157) with $Y_{\mathrm{DS},CS} = Y_{\mathrm{GD},CG}$ = 0 S, Y_G = ∞ S and (b) $Y_{\mathrm{DS},CS} = Y_{\mathrm{DS},CG}$, C_G = 0.26 pF and R_G = 20 Ω. The cut-off frequency $\omega_{c,\mathrm{D}}$ of the drain-line loaded by a 6×50µm GaN CS-HEMT is equal to 470.6 GHz, which is an approximation from $\omega_{c,\mathrm{D}} = 2/\sqrt{L_{\mathrm{D}} C_{\mathrm{DS}}}$, with $L_{\mathrm{D}} = {Z_{0,\mathrm{D}}}^2 C_{\mathrm{DS}}$ and $Z_{0,\mathrm{D}}$ = 50 Ω. The corner frequency is equal to $\omega_d = 1/R_{\mathrm{DS}} C_{\mathrm{DS}} \approx$ 20.3 GHz. From (a) it can be derived that the CG-HEMT with open source port exhibits an extremely high negative real-part, which leads to a positive S_{22} and thus an unstable behavior. As soon as a finite impedance is connected to its source port, as e.g. the output impedance Z_{DS} of a CS-HEMT in a cascode, the

impact of the CG-current source is diminished. Since the input impedance of a CG-HEMT is low-ohmic, the connection of a few ohms at the source node leads to a stable and positive output impedance based on the reduced impact of the CG-current source with smaller Z_{DS}. Unfortunately, the output impedance provided by a CS-HEMT is usually several orders larger than the optimum input matching impedance of a CG-HEMT (~ 5..20 Ω in GaN), bringing up the necessity for a RC-stabilization network (Y_{G}) at the gate-node of the CG-HEMT. Fig. 3-69 (b) sketches the equivalent output resistance $R_{\mathrm{DS}}{}'$ of a stabilized cascode with C_G = 0.26 pF, R_G = 20 Ω for different g_m. If g_m is increased from 50 mS up to 100 mS, the resulting $R_{\mathrm{DS}}{}'$ becomes larger and so the loss decreases. Exceeding a value of 100 mS would result in a pole for $R_{\mathrm{DS}}{}'$, based on the zero-crossing of the real-part of $Z_{OUT,CC}$ (→ positive S_{22}). This is in accordance with the idealized constraint of an upper g_m bound, as derived in (3.155).

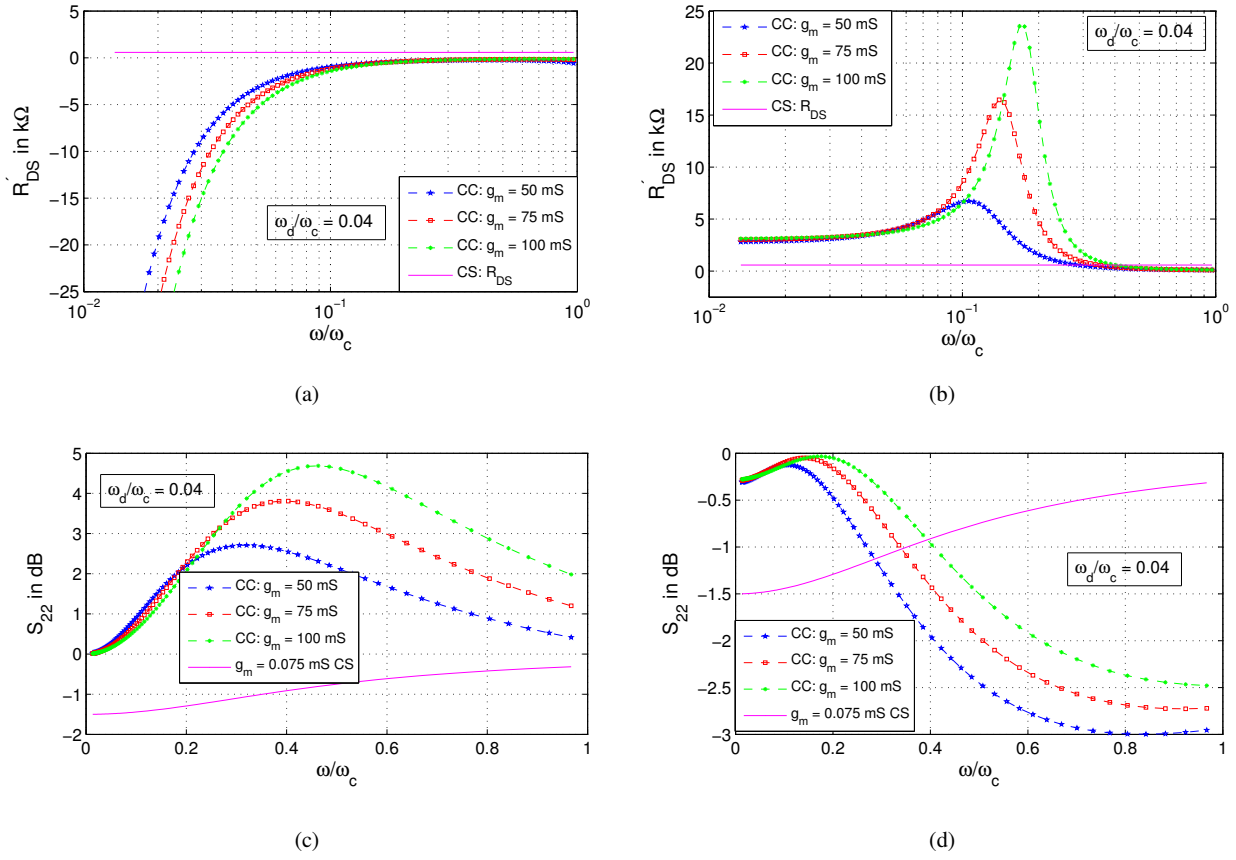


Fig. 3-69: $R_{\mathrm{DS}}{}'$ vs. $\frac{\omega}{\omega_c}$ of CG-HEMT (W_{G} = 0.3 mm) for different g_m values with (a) $Y_{\mathrm{DS},CS} = Y_{\mathrm{GD},CG} = 0$ S and $Y_{\mathrm{G}} = \infty$ and (b) $Y_{\mathrm{DS},CS} = Y_{\mathrm{DS},CG}$ and C_G = 0.26 pF, R_G = 20 Ω. (c) and (d) show the corresponding S_{22} of (a) and (b).

In order to obtain minimum loss, the values R_G and C_G of the stabilization network have to be chosen carefully to end up in a S_{22} close to 0 dB, but still staying within the passive/stable operating region. The resulting drain-line attenuation α_D according to (3.137) in Fig. 3-70 shows that the use of a stabilized cascode with W_G = 0.3 mm provides lower loss on the artificial drain-line than a CS-HEMT at frequencies smaller than roughly $0.3 \cdot \omega_c$. Above this frequency, the drain-line loss becomes larger, which is based on the stronger decay of $R_{\mathrm{DS}}{}'$, as Fig. 3-69 (b) illustrates.

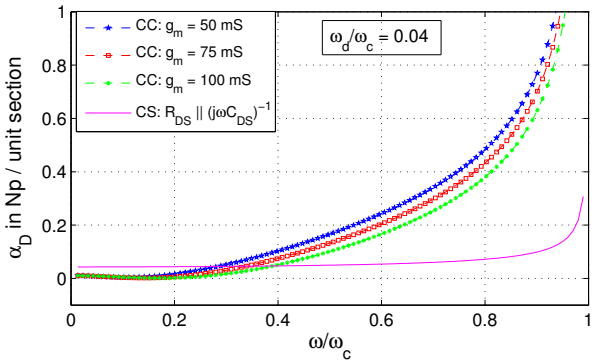


Fig. 3-70: α_D vs. $\frac{\omega}{\omega_c}$ of CC-HEMT (W_G = 0.3 mm) for different g_m with $Y_{DS,CS} = Y_{DS,CG}$ and C_G = 0.26 pF, R_G = 20 Ω.

Of all three presented approaches to tune the characteristics of the TWA´s gain shape, the first one is the most practical and simplest way in terms of layout compactness and stability. Nevertheless, the gain-bandwidth product is always kept constant, whereas by making use of the gate-/drain-line compensation schemes a real enhancement of the gain-bandwidth product can be obtained under the constraint of reduced stability margin.

3.4.7 Key Findings

The presented DC-15 GHz and DC-20 GHz TWA designs have shown that a power gain-bandwidth product of larger than 45 GHz and 50 GHz, respectively, can be obtained with the field-plated 0.25µm GaN technology from IAF. Additionally, an outstanding linearity performance especially of the 7-stage DC-20 GHz NDPA with an HD < -42 dBc at P_{OUT} = 20 dBm up to midband and an $OIP3$ > 43 dBm over the full band, was demonstrated. This underlines the high performance and suitability of TWA designs in GaN technology for the application in T&M instruments.

The maximum obtainable output power in multi-decade TWAs down to DC is strongly linked to the targeted output return loss, the characteristic load resistance R_L and the total active device size. In the case of a non-uniform design, the output resistance of the overall active gate-width should not be lower than $R_L/2$ in order to maintain an ORL > 10 dB. In the case of a uniform design, this requirement becomes even more stringent, since $R_L/2$ has to be provided by the parallel combination of the drain dumping load R_{DT} and the total active device output resistance R_{DS}/N. Accordingly, either f_{min} or P_{sat} in a TWA is limited by the specified S_{22} requirements.

The maximum frequency of operation of a TWA is dominated by the cutoff frequency $\omega_{c,G}$ of the artificial gate-line. Due to the roughly five times larger input capacitance compared to the output capacitance of the 0.25µm GaN HEMTs, the cutoff frequency $\omega_{c,G}$ for the same characteristic line impedances with $Z_0 = \sqrt{L_{G/D}/C_{G/D}}$ is also approximately smaller than the cutoff frequency of the drain-line $\omega_{c,D}$ by a factor of

$$\frac{\omega_{c,D}}{\omega_{c,G}} = \frac{\sqrt{L_G C_G}}{\sqrt{L_D C_D}} = \frac{C_G}{C_D} \approx 5.$$

The maximum number of stages in a TWA is limited by the losses of the artificial gate-line. Decisive for the magnitude of losses is the finite input conductance provided by the active HEMTs. Since the gain in a TWA is only linearly increasing with the number of stages N, the losses on the gate-line start to outweigh the benefit in gain as soon as a certain number of stages is reached. The optimum number of stages can be computed by means of the well-known equation, given in (3.135) and derived by J.B. Beyer *et al.* in [97, 98]. Mohammad-Taheri *et al.* presented in [105] a remedy for the compensation of the gate-line losses by adding capacitive series feedback and Deibele at al. presented in [106] a viable solution for lowering the drain-line losses by making use of cascodes.

The NF at low frequencies in TWAs applying capacitive gate coupling is primarily determined by the gate-bias resistors. Due to their required minimum magnitude in the order of $R_B > 500\ \Omega$ in order not to load the input of the HEMTs at RF, a noise match at each gate node results as soon as the gate input impedance converges exactly to the value of R_B at low frequencies. If no capacitive gate-coupling is applied, the large mismatch between R_B and the much lower characteristic input impedance Z_0 leads to no significant noise contribution. In this case the dominating source of noise becomes the gate-line termination resistor R_{GT} based on the increasing transfer function from the gate-termination resistor toward the ouput at low frequencies, as was already shown by C. Aitchison in [101]. It is furthermore advantageous to increase the number of stages N in the TWA design to its maximum to minimize the contribution of the induced-gate and channel noise to the overall NF according to (3.120) in chapter 3.4.3.

CHAPTER 4

LINEARIZATION CONCEPTS

Describing and predicting linearity of amplifiers precisely is still one of the most challenging tasks in III-V semiconductor amplifier designs today. Numerous modeling publications exist, dealing with physical and behavioral modeling approaches in the realm of linearity. The main difficulty resides on linearity prediction over large dynamic ranges, where no universal solution is found up to today. There are several existing approaches ranging from detailed physical over empirical analytical to measurement based descriptions. Among all these approaches, none is capable of describing the nonlinear transistor behavior over the full dynamic range accurately within a scalable model form. Either an accurate model in form of measurement based S-Functions / X-Parameter (e.g. in [107, 108, 109, 110, 111]) or artificial neural networks (ANN) (e.g. in [42, 43, 44, 45]) can be obtained for one transistor geometry or a scalable model in form of a weakly nonlinear polynomial description, such as the Volterra-Series (e.g. in [36, 37, 38, 39, 40, 41]), is derived. Most of the time it is sufficient to reproduce only the weak nonlinearities of the transistor as in the latter case, which can be more easily described mathematically. As soon as the transistor becomes saturated, nonlinearities are usually not of interest within the system requirements. This applies also for signal generators and a weakly nonlinear examination of the PAs is thus satisfactory.

Once a nonlinear model for the targeted application is created, the first important step and prerequisite for starting a linear PA design has been taken. A good nonlinear model is a prerequisite to give an accurate linearity prediction within the design process, but does not guarantee that the chosen amplifier topology behaves linearly. The second fundamental step is the choice of the linearization concept on circuit level. The three most common and well-known linearization concepts are (digital) predistortion, feedback- and feedforward linearization. Currently, the former is one of the most effective linearization schemes to be found in mobile communications standards, as e.g. GSM, UMTS or LTE. By applying digital adaptive baseband predistortion a diversity of application specific algorithms can be permitted to optimize the linearity of the PA over a limited bandwidth, as e.g. in [3, 5, 4, 112, 113]. The advantage of using adaptive predistortion for linearization is founded in the drift compensation of the amplifier characteristics over time and in the adaption to varying channel characteristics. Feedback linearization on system-level usually suffers from its limited loop bandwidth and is mainly used for

narrow-band applications, as e.g. in [114, 115, 116, 117]. In feedforward linearization schemes this bandwidth limitation is not as restrictive as in feedback schemes, but the higher bandwidth has to be traded-off for the amount of linearity improvement on the one hand and for the double power consumption on the other (e.g. in [118, 119, 120, 121, 122, 123]). The latter is based on the necessary time delayed replica of the exact same main PA in the feedforward path.

All above described concepts suffer either from limited bandwidth of usually one up to two octaves or from intricate and costly system designs. The main critical distortion comes from intermodulation in these band limited concepts and is mainly rooted in 3rd order nonlinearities. 2nd order nonlinearities can often be neglected, since their spectral content lies usually out of band. This does not hold for multi-decade broadband amplifiers anymore, where the spurious signal content lies completely inside the useable bandwidth. Out of this reason 2nd order nonlinearities, which are often dominant, pose a severe challenge for the overall SG´s linearity performance, because they cannot be filtered out by a subsequent low-pass filter. From the SG´s system point of view it is thus a meaningful approach to avoid generation of spurious harmonics at first place rather than implementing complex tunable filters, which introduce additional attenuation.Therefore within this work only linearization concepts on MMIC level are covered, which provide sufficient bandwidth and are hence suitable for the realization of multi-decade broadband PAs. The basic idea of all presented linearization concepts is the on-chip cancellation of the transistor's intrinsic nonlinearities, which are described in more detail in chapter 4.2.

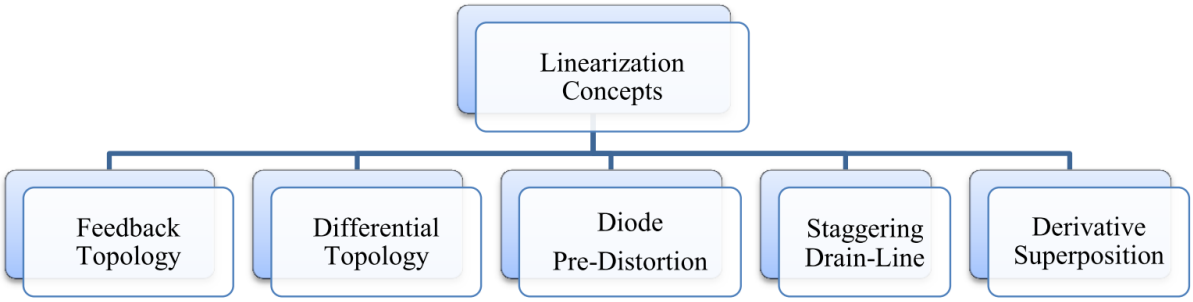


Fig. 4-1: Proposed on-chip linearization concepts for FBPAs and TWAs

During the course of this chapter five different linearization concepts have been investigated and assessed with respect to their linearization improvement and suitability for the application in SGs. It has cristallized that the well-known concept of feedback is a very good candidate for the implementation of broadband highly-linear PAs. Moreover, a diode predistortion concept has been implemented for the first time in a TWA structure (L²NTWA) and also a fully differential feedback PA (TD-FBPA) has been implemented for the first time in GaN technology. Both of the latter two concepts showed that a promising improvement in linearity with these approaches can be obtained. To better understand the made discoveries and investigations it is helpful to first of all recall general linearity terms and important FoMs to end up in a clear and comprehensible assessment of the linearity performance later on.

4.1 Linearity FoMs

4.1.1 Harmonic Distortion

Harmonic distortion (HD) is an important linearity measure to assess CW-single tone amplifier performance for the application in SGs. As already stated in chapter 1.1, some SG avoid the additional loss introduced by the LP-filter behind the PA-module and shift it before the PA-module (Fig. 1-1). This benefit in output power comes at the cost of higher linearity requirements, since in this case the PA mainly determines the output linearity of the whole SG. Due to the bandwidth of multiple octaves all generated higher harmonics fall within the band and cannot be filtered out, as e.g. in telecommunication "narrow-band" systems such as GSM, UMTS or LTE. Therefore, not only the intermodulation performance of the PA is of interest but moreover the harmonic distortion plays a key role in SGs, which describe the maximum achievable $SFDR$.

The output signal $y(t)$ of a weakly nonlinear amplifier to a single-tone CW input signal of the form

$$x(t) = A \cdot cos(\omega t) \tag{4.1}$$

can be expressed by a Taylor-series expansion up to third order by

$$y(t) = k_0 x_{DC} + k_1 x(t) + k_2 x(t)^2 + k_3 x(t)^3, \tag{4.2}$$

where k_1, k_2 and k_3 are the factors including the Taylor-Series coefficients dependent on the order n, determined by

$$k_n = \frac{1}{n!} \frac{d^n y(t)}{dx(t)^n}\bigg|_{x=0}. \tag{4.3}$$

Inserting equation (4.1) into equation (4.2) finally gives

$$\begin{aligned} y(t) = \underbrace{k_0 x_{DC} + \frac{k_2}{2} A^2}_{A_{DC}} + \underbrace{\left(k_1 A + \frac{3}{4} k_3 A^3\right)}_{A(f_0)} cos(\omega t) \\ + \underbrace{\frac{k_2}{2} A^2}_{A(2f_0)} cos(2\omega t) + \underbrace{\frac{k_3}{4} A^3}_{A(3f_0)} cos(3\omega t). \end{aligned} \tag{4.4}$$

From equation (4.4) it is now possible to calculate the second ($HD2$) and third ($HD3$) order harmonic distortion. $HD2$ is defined as the amplitude of the second harmonic to the amplitude of the fundamental, giving

$$HD2 = \frac{A(2f_0)}{A(f_0)} = \frac{k_2 A}{2k_1 + \frac{3}{2} k_3 A^2} \cong \frac{k_2}{2k_1} A \tag{4.5}$$

and correspondingly for $HD3$

$$HD3 = \frac{A(3f_0)}{A(f_0)} = \frac{k_3 A^2}{4k_1 + 3k_3 A^2} \cong \frac{k_3}{4k_1} A^2. \tag{4.6}$$

The approximations made in equations (4.5) and (4.6) are valid for weakly nonlinear systems only, where A is sufficiently small and hence $k_3 A^2 \ll k_1$.

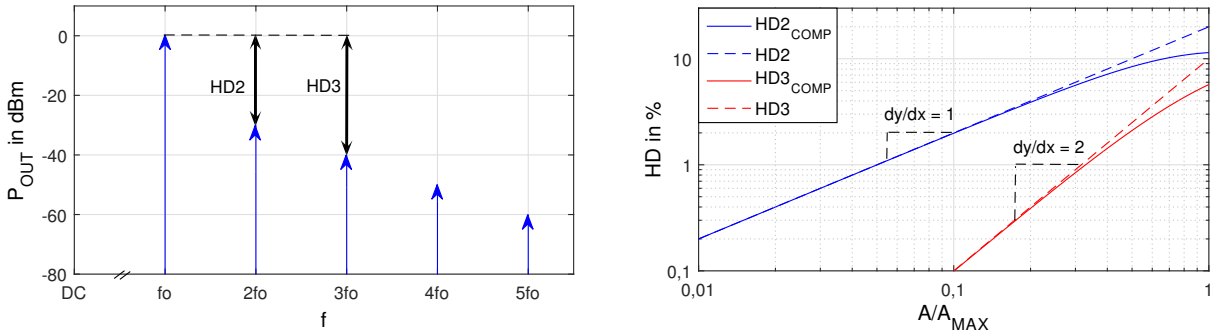


Fig. 4-2: (a) CW-spectrum of a nonlinear PA and (b) $HD2$ & $HD3$ in percent vs. normalized input amplitude A

Fig. 4-2 shows in (a) the spectrum of a nonlinear PA with spurious harmonics up to fifth order and in (b) the HD in percent versus the normalized input voltage. The dotted lines show the made approximation in (4.5) and (4.6) and the solid lines the compression caused by odd-order nonlinearities. The magnitude of $HD2$ and $HD3$ sheds also light on the magnitude of intermodulation distortion, which is the most common linearity figure and will be hence discussed more closely in the upcoming section 4.1.2.

4.1.2 Intermodulation Distortion

Undoubtedly, intermodulation distortion (IMD) is the most popular FoM when speaking about amplifier linearity. This bears on the fact that IMD is an in-band distortion which cannot be filtered out and hence might falsify information in complex modulated data transmission systems. SGs have to synthesize arbitrarily shaped signals where the spectral purity of the signal is of paramount importance. The spectrum of such signals is often too difficult to be described analytically. Out of this reason, two-tone excitation is in general sufficient to assess the amplifier´s intermodulation characteristics.

Thus, assuming a sinusoidal two-tone signal of the form

$$x(t) = A \cdot cos(\omega_1 t) + B \cdot cos(\omega_2 t + \varphi) \tag{4.7}$$

at the input of the nonlinear amplifier with the same transfer characteristic as described in (4.2), generates several intermodulation products. If only the first terms up to the order of $n = 3$ are considered, as presented in equation (4.2), the magnitude of the spectral components due to mixing can be calculated to the values given in Fig. 4-3. As already stated, only the third order nonlinearities produce the frequencies $2f_2 - f_1$ and $2f_1 - f_2$ which are close to the fundamental frequencies f_1 and f_2 and therefore cannot be filtered out. Additionally, the

fundamental frequencies are also impacted by the third order nonlinearity. Furthermore, not only the third order nonlinearity affects the amplifier´s linearity but also the second order nonlinearity, which generates new spectral components in the baseband at $f_{1,2} - f_{2,1}$ and at the second harmonic $2f_{1,2}$, plus more important at DC. The DC component is the main contributor to the often observed phenomenon of amplifier self-biasing for all nonlinear amplifier classes (e.g. AB, B, C etc.), which shifts the bias point and therewith also alters linearity again. For weak nonlinearities there is a close relation between the HD and intermodulation (IM), making single-tone measurements sometimes sufficient to assess or predict the power amplifier´s intermodulation characteristics.

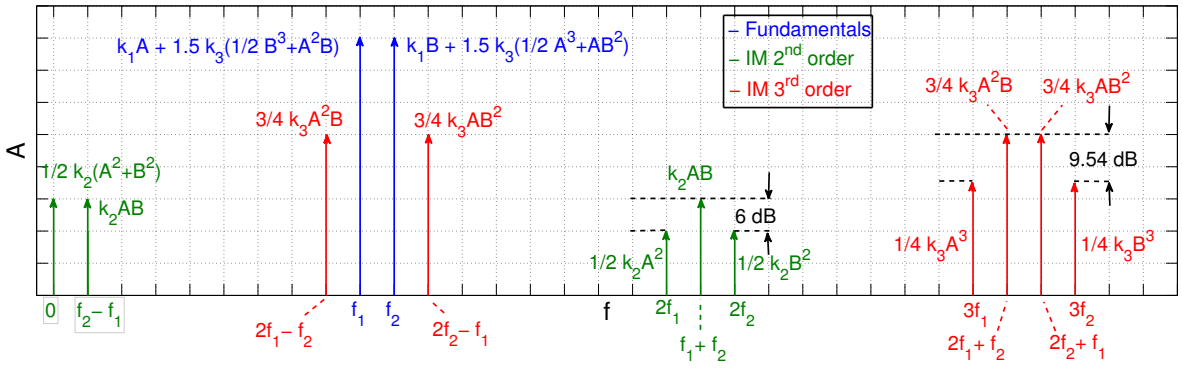


Fig. 4-3: Two-tone IM spectrum with corresponding amplitude coefficients

By setting the input amplitude A equal to B, the carrier to $IM2$- and $IM3$-ratio, denoted as $C/IM2$ and $C/IM3$, can be calculated by the ratio of the fundamental coefficient at $f_{1,2}$ to the second and third order inter-modulation coefficient at $f_2 \pm f_1$ and $2f_{2,1} \pm f_{1,2}$ from Fig. 4-3.

$$C/IM2 = \frac{A(f_{1,2})}{A(f_{2,1} \pm f_{1,2})} = \frac{k_1 A + \frac{9}{4} k_3 A^3}{k_2 A^2} = \frac{4k_1 + 9k_3 A^2}{4k_2 A} \cong \frac{k_1}{k_2 A} \tag{4.8}$$

$$C/IM3 = \frac{A(f_{1,2})}{A(2f_{2,1} \pm f_{1,2})} = \frac{k_1 A + \frac{9}{4} k_3 A^3}{\frac{3}{4} k_3 A^3} = \frac{4k_1 + 9k_3 A^2}{3k_3 A^2} \cong \frac{4}{3} \frac{k_1}{k_3 A^2} \tag{4.9}$$

Comparing the result of equation (4.9) with the obtained HD results from (4.5) and (4.6) gives

$$C/IM2 \cong \frac{1}{2 \cdot HD2} \tag{4.10}$$

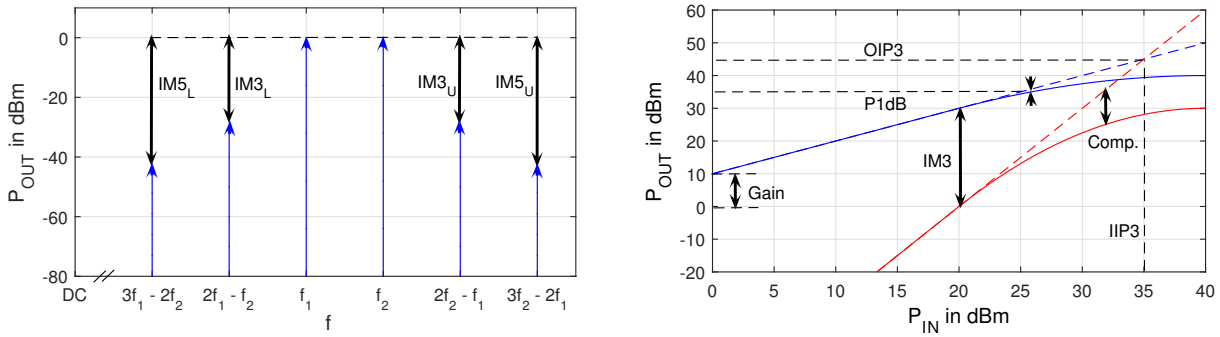
$$C/IM3 \cong \frac{1}{3 \cdot HD3} \tag{4.11}$$

for small amplitudes A, which is in dB equal to

$$C/IM2_{dBc} \cong -(HD2_{dBc} + 6.02\ dB). \tag{4.12}$$

$$C/IM3_{dBc} \cong -(HD3_{dBc} + 9.54\ dB). \tag{4.13}$$

The magnitude of $C/IM2_{dBc}$ and $C/IM3_{dBc}$ is thus around 6 dB and 9.5 dB below the magnitude of $HD2_{dB}$ and $HD3_{dB}$, respectively, which serves as a good rule of thumb. A silently presumed pre-condition for the validity of (4.11) is that this is only valid for constant source and load impedances over frequency, since in reality the impedances at $3f_{1,2}$ might differ from those at $f_{1,2}$. From the measurement complexity point of view it seems more straightforward to measure $HD3$ by means of a simpler single-tone measurement setup and calculate the $IM3$ rather than vice versa. Unfortunately, this comes with the drawback of larger measurement inaccuracies, because the amplitude of the 3rd harmonic spectral component is three times smaller than the one of the $IM3$. Therefore it is better to measure the $IM3$ in order to obtain an accurate linearity statement. The two most important intermodulation products of 3rd and 5th order are depicted in Fig. 4-4. Therein are the lower and upper IM-products of $IM3$ and $IM5$ assumed to be symmetric, which is only the case for an ideal amplifier without memory and ideal baseband bias impedances.



(a) (b)

Fig. 4-4: Two-tone intermodulation distortion of 3rd and 5th order ($IM3$ & $IM5$) and (b) relationship between $OIP3$ and $IIP3$

Another useful FoM is the 3rd order intercept point (TOI or $IP3$) to express intermodulation performance in the presence of two-tone signals. It is a non-measurable FoM describing the artificial intersection point, where the fundamental signal power P_1 and the signal power due to third order nonlinearities P_3 would become equal. The mathematical expression in dB can be derived from Fig. 4-4 (b). It should be kept in mind that all $OIP3$ calculations refer to a weakly nonlinear system and so a P_{1dB} back-off operation of larger than 6-10 dB has to be taken for granted, as a rule of thumb.

$IIPn$ stands for the input referred IPn, whereas the $OIPn$ is associated to the output. The connection between both FoMs can be made via the gain and can be expressed in dBm by

$$OIPn_{dBm} = IIPn_{dBm} + G_{P,dB}. \tag{4.14}$$

One way to express the $OIPn_{dBm}$ by means of the n^{th}-order intermodulation product IMn_{dBm} or C/IMn_{dBc} is based on the convergence of the fundamental output power $P_{OUT1,dBm}$ and the IMn_{dBm} with a difference in slope of n - 1, giving

$$\begin{aligned} OIPn_{dBm} &= P_{OUT1,dBm} + \frac{1}{n-1}\left(P_{OUT1,dBm} - IMn_{dBm}\right) \\ &= P_{OUT1,dBm} - \frac{1}{n-1} \cdot C/IMn_{dBc}. \end{aligned} \tag{4.15}$$

This gives for the output 3rd order intermodulation product

$$OIP3_{dBm} = P_{OUT1,dBm} - \frac{1}{2} \cdot C/IM3_{dBc}. \tag{4.16}$$

The other way to calculate the IPn is based on the convergence of C/IMn_{dBc} to zero dB at $P_{IN} = IIPn_{dBm}$ in Fig. 4-4 (b). Hence to express the $IIP3$ in terms of the Taylor series coefficients, the value for the $C/IM3$ has to be set equal to one in equation (4.9) and solved for A. This results in an $IIP3$ and $OIP3$, respectively, of

$$IIP3_{dBm} = 20 \cdot log\left(\sqrt{\frac{4}{3}\frac{k_1}{k_3}}\right) \tag{4.17}$$

$$OIP3_{dBm} = 20 \cdot log\left(\frac{2k_1}{\sqrt{3k_3}}\right). \tag{4.18}$$

Additionally, a close conjunction between $OIP3$ and P_{1dB} can be seen from Fig. 4-4 (b). The difference between $OIP3$ and P_{1dB} is often used to evaluate the linearity of a given amplifier design, where typical values are found to be in the range of 10-13 dB for GaAs and GaN broadband PAs, as can be underlined by several product datasheets (e.g. TriQuint, Hittite, RFMD, etc.) or by [124].

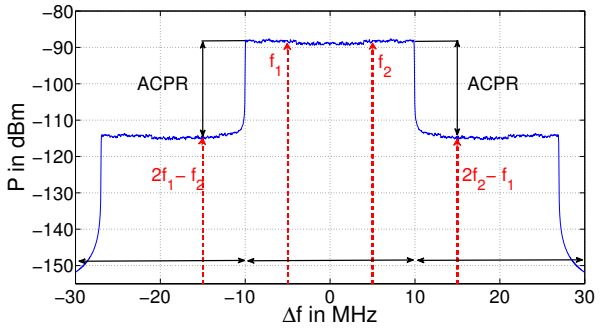


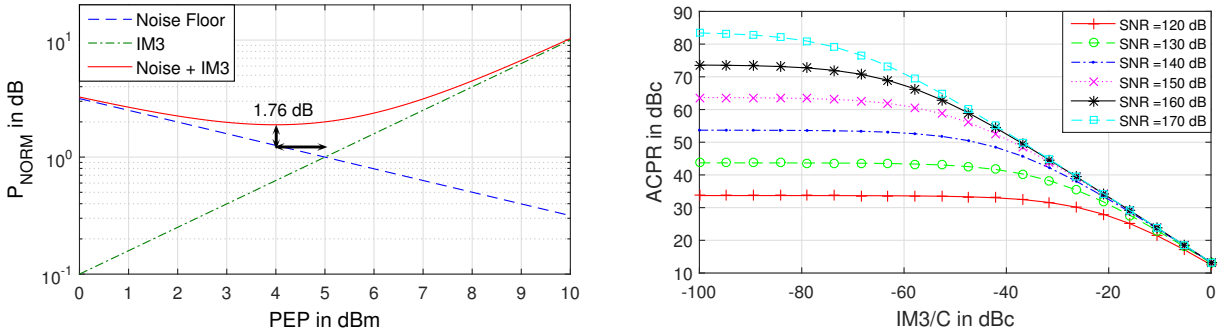
Fig. 4-5: Typical LTE-spectrum with a BW of 20 MHz, distorted by the neighbor channel

An additional two-tone FoM besides the $IM3$ is the $ACPR$. $ACPR$ stands for adjacent-channel-power-ratio and is a common linearity measure for wireless communication systems. In systems where e.g. orthogonal-frequency-division-multiplex (OFDM) is applied, such as the mobile standard long-term-evolution (LTE), independent information is sent over closely spaced carrier frequencies with up to 20 MHz of bandwidth or up to 2048 closely spaced channels. To better assess the system´s performance of the dense frequency spectra, the

power within a specified bandwidth of the desired signal S_S and the neighboring interferers S_{NC} are put into relation. Thus, the ACPR value in dB can be calculated by

$$ACPR = 10 \cdot log\left(\frac{\int_{f_L-BW}^{f_H-BW} S_{NC}}{\int_{f_L}^{f_H} S_S}\right). \tag{4.19}$$

To identify the optimum input power for CW-signals or optimum PEP for modulated signals which maximizes the $ACPR$, an idealized consideration of the system is sufficient. Assuming a constant noise floor, the SNR increases by the amount of increasing input power, which in turn leads to a decrease in noise level for a normalized output power, as depicted by the blue dashed line in Fig. 4-6 (a). The $IM3$-product in contrast increases with a slope of two in logarithmic scale, as can be seen from equation (4.9), resulting in an intersection of the decreasing noise floor and increasing $IM3$-product. Interestingly, the minimum $ACPR$ value does not coincide with the intersection point but rather is 1 dB below this point due to the vectorial summation of noise power and $IM3$ power. Determination of the absolute $ACPR$ minimum yields that the theoretical minimum of the $ACPR$ lies exactly 1.76 dB above the noise floor, as depicted in Fig. 4-6 (a). Fig. 4-6 (b) illustrates the dependency of the $ACPR$ on the invers $C/IM3$-ratio for different SNR values. With increasing $IM3$ power all $ACPR$ curves converge to the same value, independent of the SNR. At an $C/IM3$ equal to 0 dBc the $ACPR$ value becomes equal to the Crest-factor of 13.3 dB of the modulated LTE signal.



(a) (b)

Fig. 4-6: (a) $ACPR_{norm}$ vs. PEP and (b) $ACPR$ vs. $IM3/C$

4.2 GaN HEMT Nonlinearities

Before focusing on different linearization concepts, it is meaningful to gain a general understanding of the intrinsic nonlinearity sources and their voltage dependencies. The sources of nonlinearities in a GaN HEMT are highlighted by the red color in the equivalent intrinsic large-signal model in Fig. 4-7 below.

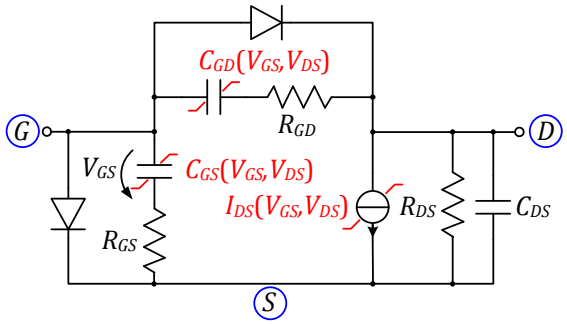
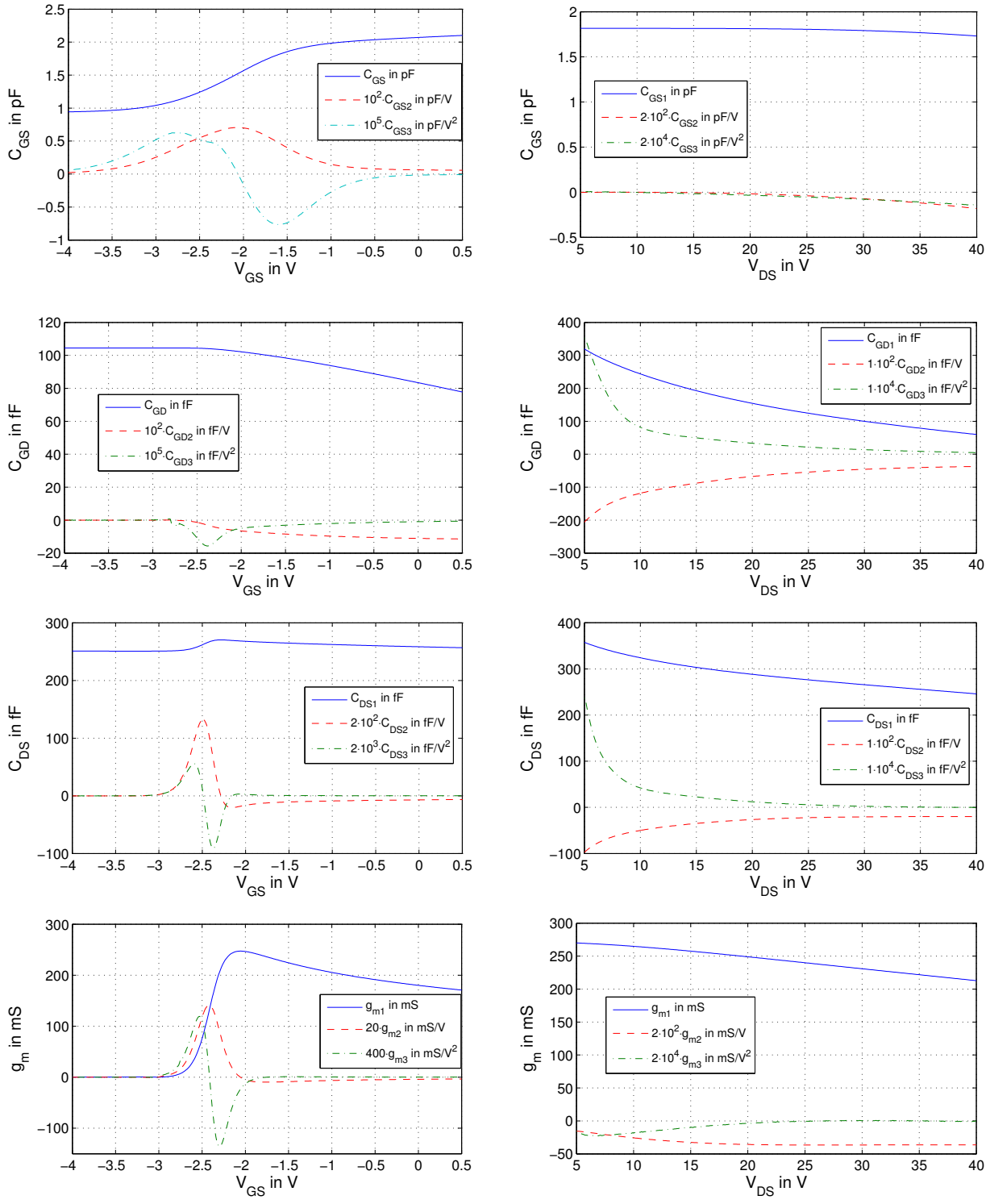


Fig. 4-7: Intrinsic large-signal model of GaN HEMT with nonlinear drain-source channel current and capacitances

First of all it is useful to estimate the impact factor of each nonlinearity on the overall nonlinearity. Fig. 4-8 illustrates therefore the dependency of the intrinsic capacitances and transconductance on V_{GS} and V_{DS}. The largest part of the HEMT´s nonlinearity arises from the drain-source channel current I_{DS} followed by the gate-source capacitance C_{GS}, whereas only a small part is generated by the gate-drain capacitance C_{GD}. This smaller part can be often neglected due to its roughly 15 times smaller size compared to C_{GS} at an operational bias of V_{DS} = 30 V in GaN. It can be moreover assumed that the dependence of C_{GS} and C_{GD} are mainly determined by the voltages V_{GS} and V_{DS}, where the former capacitance is almost only dependent on V_{GS} and the latter one on V_{DS} (see Fig. 4-8). In the following linearity investigation the nonlinearity dependence is thus simplified to the approximation of $C_{\mathrm{GS}}(V_{\mathrm{GS}})$ and $C_{\mathrm{GD}}(V_{\mathrm{DS}})$. The transconductance g_m is highly dependent on V_{GS} and also on V_{DS}, whereby the dependency on V_{DS} is approximately linear.

Nonlinearities arising from dynamic effects and memory effects, such as frequency dispersion [125] and self-heating [126, 127, 128], are not covered in the following linearity analysis. Moreover, asymmetries in IMD caused by the variation in baseband load-impedance in the presence of multi-tone signals are also not within the scope of this chapter [129, 130, 131, 132]. Despite of all these effects being present, taking them into account unnecessarily complicates the examinations and does not help to gain a better understanding of the later proposed linearization concepts in chapters 4.3 to 4.7.



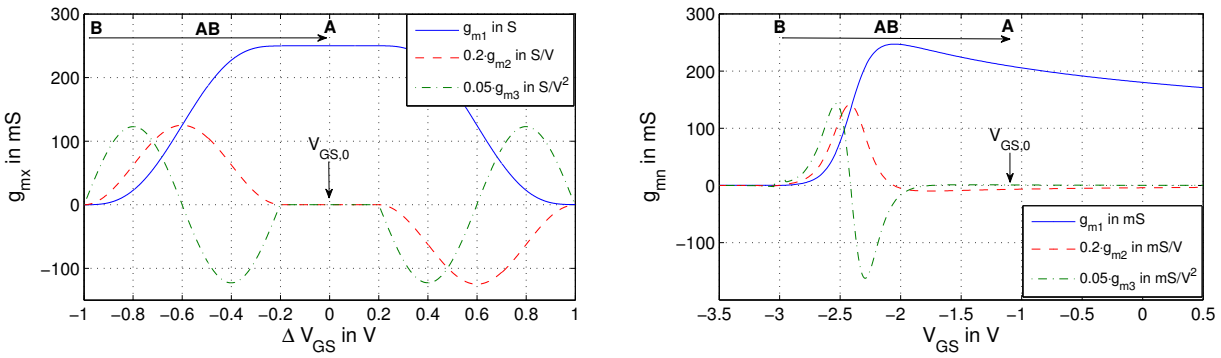
(a) (b)

Fig. 4-8: C_{GS}, C_{GD}, C_{DS} and g_m dependence (a) on V_{GS} for V_{DS} = 30 V and (b) on V_{DS} for I_{DS} = 200 mA/mm of a 8×125µm GaN HEMT

4.2.1 Investigation of Channel-Current Nonlinearities

At the very beginning it seems reasonable to find a procedure, which is capable of predicting the optimum operational bias conditions for a single HEMT before setting up and designing a complete amplifier MMIC. Out of this reason it is useful to take a closer look at the typical GaN nonlinearity characteristics of the channel current. To better understand the different linearization concepts in the following sections it is meaningful to first of all understand the 2nd and 3rd order nonlinearity dependence of the channel current on the bias point selection and input power for a single CS-HEMT. The channel current nonlinearity of a HEMT can be modelled in terms of the intrinsic g_m nonlinearity. Presuming weakly nonlinear signals, the following Taylor series expansion up to the third order in (4.20) expresses the nonlinear channel current.

$$I_{\mathrm{DS}} = I_{\mathrm{DS},0} + g_{m1}\left(V_{\mathrm{GS}} - V_{\mathrm{GS},X}\right) + \frac{g_{m2}}{2}\left(V_{\mathrm{GS}} - V_{\mathrm{GS},X}\right)^2 + \frac{g_{m3}}{6}\left(V_{\mathrm{GS}} - V_{\mathrm{GS},X}\right)^3 \tag{4.20}$$

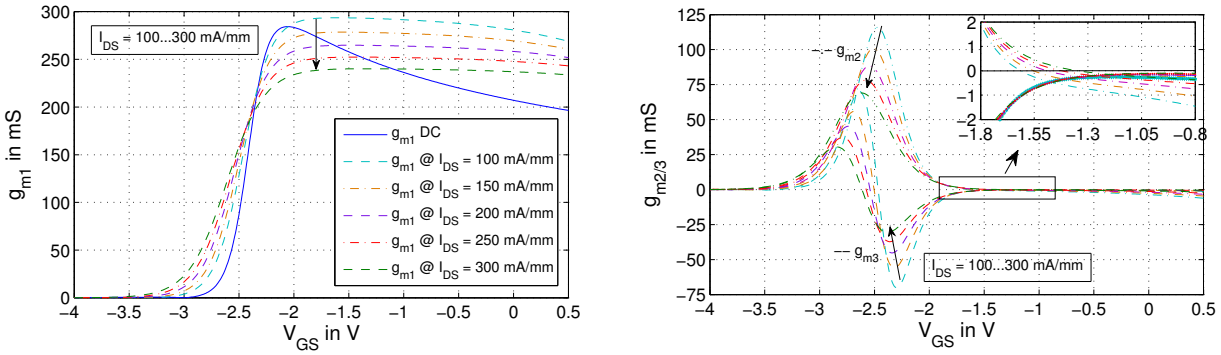


(a) (b)

Fig. 4-9: g_m-curves of (a) idealized HEMT and (b) 8×125µm GaN HEMT LS-model; g_{m2} and g_{m3} are both multiplied by a factor of 0.2 and 0.05, respectively.

For achieving better comparison, an idealized "HEMT" transfer characteristic will be introduced to better grasp the implications of the typical GaN nonlinearity properties on different linearization concepts. Fig. 4-9 (a) depicts the so introduced "idealized" g_m-curve with its corresponding first and second order derivatives g_{m2} and g_{m3}. It can be clearly seen that g_{m2} and g_{m3} exhibit only one single common root at V_{GS} = 0 V, reflecting that ideally class A operation results in the highest linearity. Choosing any other bias point ends up in the often observed trade-off between 2nd and 3rd order nonlinearity, since only g_{m2} or g_{m3} can be minimized at the same time. Under small-signal operation the small-signal sweet-spots occur only at the roots of the $g_{m2/3}$-curves. Unfortunately is the idealized flat shape of the g_m-curve usually nonexistent in III-V semiconductor processes. Fig. 4-9 (b) shows the g_m-curves for an 8×125µm GaN HEMT, where the g_m-curve is extracted from the large-signal model, still including the extrinsic lead resistances $R_{\mathrm{G}}, R_{\mathrm{D}}$ and R_{S}. The process is optimized for class AB operation and shows a constantly decaying g_m-gradient from class AB towards class A bias due to the strong thermal dependence of GaN semiconductor. It has to be noticed that the g_m-curve in Fig. 4-9 (b) does not reflect the high frequency large-signal g_m of the HEMT. For input signal frequencies higher than one over the minimum thermal time constant, which is usually in the ms-range, no thermal impact of the signal swing on the

operational device temperature will be observed. Hence, the large-signal isothermal g_m shows less degradation for higher V_{GS} than the thermal dependent DC-g_m, as Fig. 4-10 reveals. Furthermore, from Fig. 4-10 (b) it can also be derived that with increasing bias current the magnitudes of g_{m2} and g_{m3} decay, which leads to an additional higher linearity by moving from class AB to class A operation. The gain in linearity performance of a class A amplifier is thus visible, but additionally reveals that the device gain becomes lower with increasing linearity.



(a) (b)

Fig. 4-10: Transient RF- (a) g_{m1} and (b) $g_{m2/3}$ vs. V_{GS} for I_{DS} = 100…300 mA/mm of an 8×125µm GaN HEMT

To make a statement about the nonlinearity under large signal operation not only the roots or minima of $g_{m2/3}$ are important but moreover the shape of the whole g_m-curve, because the input signal traverses a much larger part of the g_m-curve. Dependent on the selected bias point position this might end up in a continuously changing magnitude and phase for the 2nd and 3rd order nonlinearities. Cancellation around a root can only be maintained as long as the magnitudes of $g_{m2/3}$ are equal for the positive and the negative half of the input signal swing.

C.P. Lee et. al made use of the coherency between phase/time and amplitude of a sinusoidal input signal to derive an expression which helps to predict the input power dependency of large-signal sweet-spots analytically [133]. They proved that the resulting large-signal nonlinearity caused by the channel current is dependent on the integrated area under the $g_{m2/3}$-curve, multiplied by a symmetric weighting function $w_n(x)$. The weighting function incorporates the nonlinear relation between phase/time and amplitude of a sinusoidal signal, reflecting that the energy conservation during the transformation of the Fourier-integral over time to the input voltage domain is fulfilled. The amplitude of the n^{th}-order harmonic Fourier component H_n for the channel current under sinusoidal single-tone excitation can be expressed by

$$H_n = \frac{1}{\pi} \int_{-\pi}^{+\pi} \underbrace{f\left(V_{GS0} + \frac{\Delta V_{IN}}{2} cos(\omega t)\right)}_{f(\Delta V_{IN}, \omega t)} \cdot cos(n\omega t)\, d\omega t. \tag{4.21}$$

Equation (4.21) presents the general solution, where the integration takes place over the phase in the time-domain. Therein, $f(\Delta V_{IN}, \omega t)$ describes the nonlinear function, which causes the nonlinearity and which is dependent on the input signal swing. In terms of the channel current nonlinearity, $f(\Delta V_{IN}, \omega t)$ is in this case equal

to the output channel current I_{DS}. Since it is desirable to integrate over the input voltage swing rather than over the phase in order to express the nonlinearity by the input voltage dependent derivatives of I_{DS}, C.P. Lee et. al derived in [133] by smart integration by parts the following expression for the n^{th}-order harmonic Fourier component H_n, where the integrand is now dependent on the input voltage swing only.

$$H_n = \frac{2(\Delta V_{IN}/2)^{n-1}}{\pi(2n-1)!!} \int_{V_{GS0}-\frac{\Delta V_{IN}}{2}}^{V_{GS0}+\frac{\Delta V_{IN}}{2}} g_{mn}(\Delta V_{IN})|_{V_{GS0}} \cdot \underbrace{\left(1-\left(\frac{2x}{\Delta V_{IN}}\right)^2\right)^{\frac{(2n-1)}{2}}}_{w_n(x)} dx \tag{4.22}$$

The variable x in (4.22) is equal to $x = \Delta V_{IN}/2 \cdot cos(\omega t)$. In other words, the integral over ΔV_{IN} of $g_{m,2/3}$ has to be minimized or simply speaking, the smaller the enclosed area the smaller is the corresponding harmonic content. As long as the shape of the regarded $g_{m2/3}$-curve is symmetric around the bias point, omission of the symmetric weighting function $w_n(x)$ does only result in an error in absolute magnitude of the integral but not in the overall trend of the curve. This means that the nulls of the integral of $g_{m2/3}$ over ΔV_{IN} are at the exact same positions with or without weighting function $w_n(x)$. Given that the shape of $g_{m2/3}$ is asymmetric around the bias point, $w_n(x)$ has to be included in the calculation.

The weighting function $w_n(x)$ will be always incorporated for a better comparability in the following analysis. By contemplating a sinusoidal time-domain signal it might not be fully intuitive at first sight why the nonlinearity cancels out. The existing time-delay between positive and negative half of the input signal period leads to a traverse of the nonlinearity such that the opposing signs of $g_{m2/3}$ occur also delayed in time. The trick is the transformation into the frequency-domain by the Fourier-transform, where the 180° phase shift of $g_{m2/3}$ at half of the signal period transfers the odd-order signal energy into the even-order signal components and vice versa.

$$FD = \frac{2}{\pi} \int_{-\Delta V_{IN}/2}^{+\Delta V_{IN}/2} g_{m1}(V_{IN}) \cdot \underbrace{\left(1-\left(\frac{x}{\Delta V_{IN}/2}\right)^2\right)^{1/2}}_{w_1(x)} dx \tag{4.23}$$

$$H_2 = \frac{2}{3\pi}\Delta V_{IN} \int_{-\Delta V_{IN}/2}^{+\Delta V_{IN}/2} g_{m2}(V_{IN}) \cdot \underbrace{\left(1-\left(\frac{x}{\Delta V_{IN}/2}\right)^2\right)^{3/2}}_{w_2(x)} dx \tag{4.24}$$

$$H_3 = \frac{1}{30\pi}{\Delta V_{IN}}^2 \int_{-\Delta V_{IN}/2}^{+\Delta V_{IN}/2} g_{m3}(V_{IN}) \cdot \underbrace{\left(1-\left(\frac{x}{\Delta V_{IN}/2}\right)^2\right)^{5/2}}_{w_3(x)} dx \tag{4.25}$$

Returning to Fig. 4-9 (a) and applying the just mentioned relations to the g_m-curve enables now to predict the input power dependency of the 2nd and 3rd order nonlinearity for the ideal HEMT. The resulting fundamental, 2nd and 3rd order harmonics H_2 and H_3 are then equal to (4.24) and (4.25). Since only the trend of the large-signal $g_{m2/3}$-nonlinearity is of interest and not the exact magnitude, the integral factor in (4.22) is simply omitted in the subsequent investigations. Fig. 4-11 depicts the integrals from (4.23) and (4.25) of the $g_{m2/3}$-curves versus the gate-source bias voltage V_{GS0} and the peak-to-peak amplitude of the drive signal ΔV_{IN}. Considering

class A (ΔV_{GS0} = 0V) operation in the plots of Fig. 4-11 (a) shows in the upper picture that the 2nd order nonlinearity will be canceled independent of the applied input power due to the odd-symmetry of g_{m2} around V_{GS} = 0 V in Fig. 4-9 (a), whereas the 3rd order nonlinearity in the lower picture of Fig. 4-11 (a) shows an input power dependent characteristic due to the even-symmetry of g_{m3} around V_{GS} = 0 V in Fig. 4-9 (a). The integral of the 3rd order components will first of all decrease with increasing input power and will only for large input signals converge to zero again due to the positive g_{m3}-area contribution towards pinch-off and breakdown (see Fig. 4-9 (a)). This results in the often observed sweet-spot in $HD3$ or $IM3$ of amplifiers close to P_{SAT} [134, 134, 135], which is owed to the flat shape of the g_m-curve [136]. For the plotted ΔV_{IN}-range from 0 V to 2 V the best $HD3$ or $IM3$ performance is to be expected for ΔV_{GS} = -0.6 V, indicated by the red line in the lower Fig. 4-11 (a). Fig. 4-11 (b) illustrates the corresponding input power and bias point dependence of the 8x125µm GaN HEMT´s 2nd and 3rd order nonlinearity. Therein, it becomes obvious that the minimum for g_{m2} and g_{m3} over a large input dynamic range can only be realized in class A. If only the 3rd order nonlinearity is of concern it might be meaningful to bias the HEMT in deep class AB-B at V_{GS0}= -2.47 V in order to increase the power added efficiency, if power is of concern in the intended application. As can be seen from the upper Fig. 4-11 (b), the 2nd order nonlinearity exhibits a very input power dependent sweet-spot characteristic between class AB and class A at V_{GS0}= -2…-1.1 V. Out of these considerations it can be concluded that it is the best option to bias the HEMT in class A in order to achieve the highest linearity over a large dynamic range.

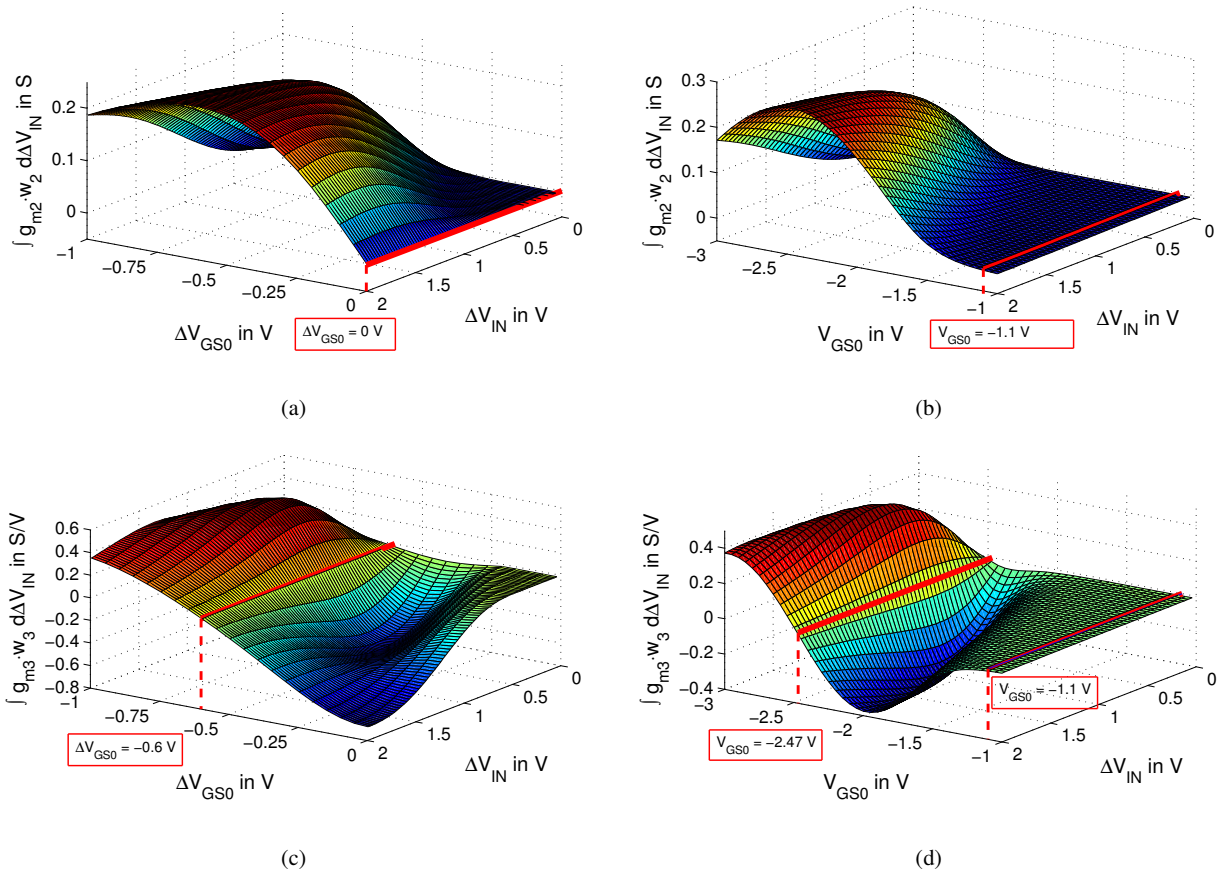


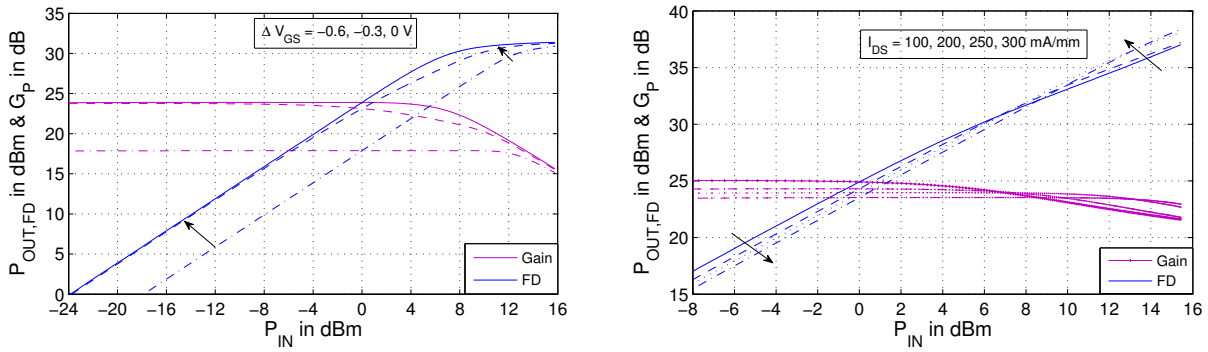
Fig. 4-11: Integral of g_{m2} and g_{m3} over ΔV_{IN} plotted vs. ΔV_{IN} and V_{GS0} for (a,c) an idealized HEMT and (b,d) 8×125µm GaN HEMT

In the foregoing investigation only the integral of the g_{m2} and g_{m3} nonlinearity for different bias points and different input powers has been examined. Now, a statement about the ratio between fundamental and harmonic distortion, will be made to identify the input power dependent sweet-spots. Fig. 4-14 depicts the ratio of g_{m2} and g_{m3} to g_{m1}, each weighted by $w_n(x)$ and integrated over the input signal swing, as described in (4.20), for the given g_m-curves from Fig. 4-9 (a) and Fig. 4-10. In doing so, this ratio can be taken as a measure for the degree of $HD2$ and $HD3$ contribution from the nonlinear channel current, as expressed in (4.26) and (4.27) below.

$$HD2_{dBc} = 20 \cdot log\left(\frac{H_2}{FD}\right) \tag{4.26}$$

$$HD3_{dBc} = 20 \cdot log\left(\frac{H_3}{FD}\right) \tag{4.27}$$

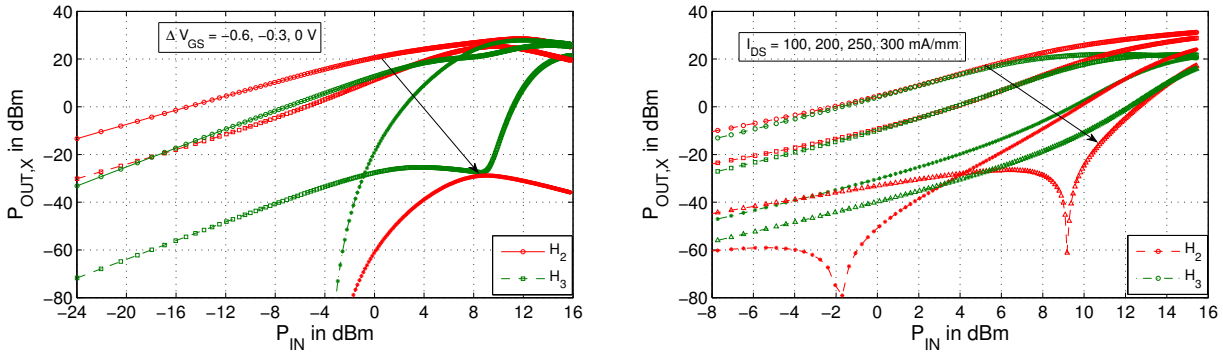
It is important to note that the constant integral factors from (4.20) have been included now in (4.26) to visualize the input power dependency and sweet-spots of the 2nd and 3rd order harmonic distortions $HD2$ and $HD3$. The first sweet-spot for the ideal HEMT occurs based on the zero of the 3rd order derivative for input signals smaller than $\Delta V_{IN} \approx 0.4$ V ($P_{IN} \approx$ -4 dBm) in class A bias, as Fig. 4-13 (a) and Fig. 4-14 (a) show. As expected, the second sweet-spot comes close to saturation, where the input signal swing covers the whole input signal range and based on the odd-order symmetry cancels completely at P_{SAT}.



(a) (b)

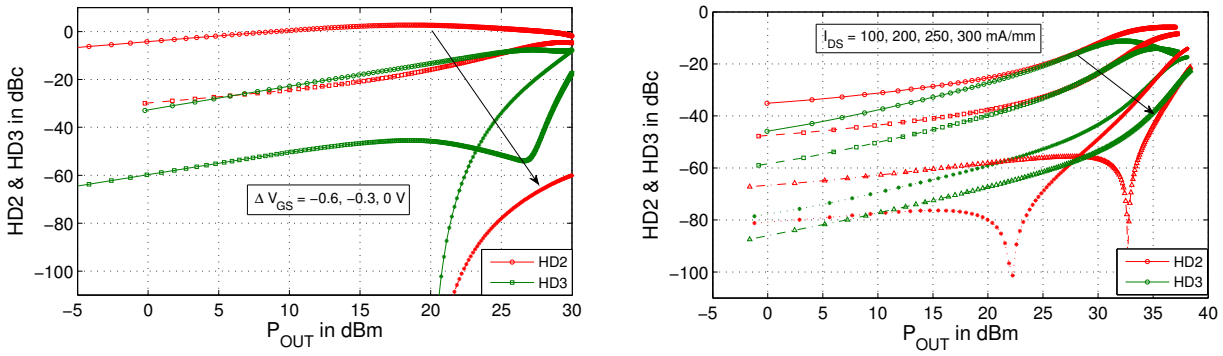
Fig. 4-12: Calculated $P_{OUT,FD}$ & G_P vs. P_{IN} of (a) an idealized HEMT for ΔV_{GS} = -0.6…0 V and (b) 8×125µm GaN HEMT with I_{DS} = 100…300 mA/mm

For the 8×125µm GaN HEMT in Fig. 4-14 (b) no input power dependent 3rd order sweet-spot occurs but instead a 2nd order sweet-spot for a peak-to-peak input signal swing of $\Delta V_{IN} \approx 0.5$ V ($P_{IN} \approx$ -2 dBm) at I_{DS} = 250 mA/mm and for $\Delta V_{IN} \approx 1.8$ V ($P_{IN} \approx$ 9 dBm) at I_{DS} = 300 mA/mm, approaching class A bias. This is based on the alternating sign of g_{m2} around V_{GS0}= -1.65…-1.35 V, as indicated by the inset in Fig. 4-11 (b). As has been stated, in general it is also possible to cancel the second order nonlinearity, but in most applications, where e.g. vector modulated signals have to be amplified, it is more usesful to improve the IMD performance rather than to suppress the 2nd spurious harmonic. Suppressing the 2nd harmonic might only be desirable if either only single tone performance is sought or very strong second order distortions in a two-octave bandwidth system are present.



(a) (b)

Fig. 4-13: Calculated H_2 & H_3 in dBm vs. P_{IN} of (a) an idealized HEMT for ΔV_{GS} = -0.6…0 V and (b) 8×125µm GaN HEMT with I_{DS} = 100…300 mA/mm



(a) (b)

Fig. 4-14: Calculated $HD2$ and $HD3$ vs. P_{OUT} of (a) an idealized HEMT for ΔV_{GS} = -0.6…0 V and (b) 8×125µm GaN HEMT with I_{DS} = 100…300 mA/mm

4.2.2 Investigation of Gate-Source Capacitor Nonlinearities

Similar to the procedure from chapter 4.2.1 regarding the channel current nonlinearity of a HEMT, this chapter focuses on the large-signal nonlinearity caused by the nonlinear input capacitor C_{GS}. The main goal of this chapter is to understand the input power and frequency dependence of the C_{GS} nonlinearity of the HEMT. The nonlinearity of C_{GS} manifests itself in a distortion of the gate-source voltage V_{GS}, which is amplified to the output of the HEMT via the transconductance g_m. The gate-source current can be in general expressed by the following derivative of the gate-source charge with respect to time.

$$I_{\mathrm{GS}}(V_{\mathrm{GS}}) = \frac{dQ_{\mathrm{GS}}(V_{\mathrm{GS}})}{dt} = C_{\mathrm{GS}}(V_{\mathrm{GS}}) \cdot \frac{dV_{\mathrm{GS}}}{dt} \tag{4.28}$$

Multiplication with dt and reorganization of (4.28) yields

$$C_{\mathrm{GS}}(V_{\mathrm{GS}}) = \frac{dQ_{\mathrm{GS}}(V_{\mathrm{GS}})}{dV_{\mathrm{GS}}}. \tag{4.29}$$

Assuming a weakly nonlinear input signal, the nonlinear gate-source charge stored in C_{GS} can be described by the following Taylor-series up to third order.

$$Q_{\mathrm{GS}}(V_{\mathrm{GS}}) = q_0|_{V_{\mathrm{GS0}}} + q_1(V_{\mathrm{GS}} - V_{\mathrm{GS0}}) + \frac{q_2}{2}(V_{\mathrm{GS}} - V_{\mathrm{GS0}})^2 + \frac{q_3}{6}(V_{\mathrm{GS}} - V_{\mathrm{GS0}})^3 \tag{4.30}$$

The coefficients q_1, q_2 and q_3 in (4.30) are nothing else than the 1st, 2nd and 3rd order derivatives of Q_{GS} with respect to V_{GS} at the bias point V_{GS0}. Thus, the coefficient q_n has the unity Farad and therefore it is meaningful to replace q_1, q_2 and q_3 by the capacitance coefficients c_0, c_1 and c_2. By insertion of (4.30) in (4.29), $C_{\mathrm{GS}}(V_{\mathrm{GS}})$ can be finally rewritten to

$$C_{\mathrm{GS}}(V_{\mathrm{GS}}) = c_0 + c_1\big(V_{\mathrm{GS}} - V_{\mathrm{GS},X}\big) + \frac{c_2}{2}\big(V_{\mathrm{GS}} - V_{\mathrm{GS},X}\big)^2. \tag{4.31}$$

Equation (4.31) illustrates that the resulting nonlinearity of the gate-source capacitor C_{GS} can be again expressed by a Taylor-series. Comparison of equation (4.31) with (4.30) shows now that c_1 causes a 2nd order harmonic distortion and c_2 correspondingly a 3rd order harmonic distortion in the gate-source current, which translates one to one into an input voltage distortion. Based on this relationship the characteristic of the 1st, 2nd and 3rd order derivatives c_0, c_1 and c_2 versus V_{GS} are of major interest for the assessment of the C_{GS} nonlinearity.

The c_k-coefficients versus V_{GS} of an 8×125µm GaN HEMT are depicted in Fig. 4-15. The curves possess a similar characteristic as the g_m-curves in their turn-on behavior, which might anticipate that the resulting output nonlinearity from C_{GS} shows a similar V_{GS} or input power dependence, respectively. In contrast to the g_m-nonlinearity, the C_{GS}-nonlinearity is additionally dependent on frequency and not only on the applied input power. It is therefore meaningful to differentiate between the input power dependency and frequency dependency of the C_{GS}-nonlinearity in the further analysis.

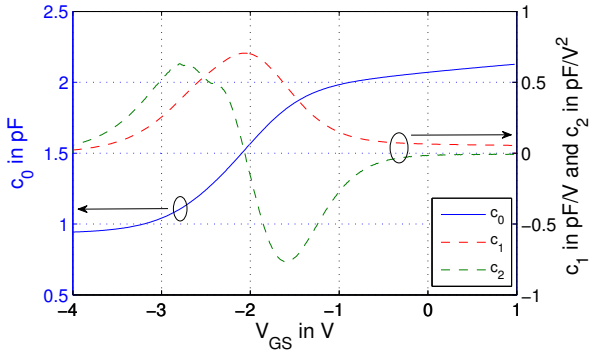


Fig. 4-15: C_{GS0} (c_0) and its higher derivatives c_1 and c_2 versus V_{GS}

Input Power Dependency

The impact of the input power dependence of the C_{GS}-nonlinearity on the output linearity can be explained shortly by means of Fig. 4-15 above and is similar to the considerations done for the channel nonlinearities in chapter 4.2.1. Similar to the g_m-nonlinearity exhibits the C_{GS}-nonlinearity a positive first order derivative (c_1), which increases steadily with increasing P_{IN} independent of the chosen bias-point. The outcome from the even-order symmetry around V_{GS} = -2.05 V is an increasing 2nd harmonic at the output of the HEMT. The second order derivative (c_2) in contrast possesses a zero at V_{GS} = -2.05 V, which manifests itself in a sweet-spot of the 3rd harmonic, at least for very small input signal swings. As soon as P_{IN} increases, the 3rd harmonic starts to increase as well due to the slight odd-order asymmetry of c_2 around V_{GS} = -2.05 V. Given the assumption that c_2 would be completely point symmetric, no 3rd order nonlinearities would be generated by C_{GS} and thus amplified to the output. The size of the C_{GS}-trajectory is thereby not only dependent on P_{IN} but furthermore on the frequency, as will be explained in the following subsection in more detail.

Frequency Dependency

It has been stated in several papers that the impact of the nonlinearity arising from the reactive circuit components increases with increasing frequency, as e.g. in [137]. At a first glance at Fig. 4-16 this might be counter-intuitive if simply the input low-pass filter of a HEMT, comprised by C_{GS} and R_{GS}, is regarded. With increasing frequency the control voltage swing V_{GS} will be reduced due to the increasing voltage drop over R_{GS}. According to the before made analysis about the input power dependent C_{GS}-nonlinearity this would translate into a lower output nonlinearity due to the reduced nonlinearity traverse of C_{GS}. What is completely left out is the matching consideration with the source impedance. Considering the two extreme cases, where the HEMT is either driven with a sinusoidal signal at f = 1 Hz (low frequencies) or $f = f_T$ (very high frequencies) helps to understand the frequency dependence of the C_{GS}-nonlinearity. Presuming that the input power is applied to the HEMT via an equivalent "Thévenin"-source with the series source impedance Z_S, neither v_{IN} nor i_{GS} stays constant over frequency.

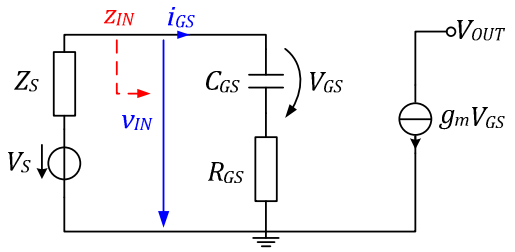


Fig. 4-16: Simplified HEMT schematic driven by a Thévenin source

For low frequencies v_{IN} in Fig. 4-16 is almost equal to V_S and i_{GS} is equal to zero based on the high input impedance provided by C_{GS}. Thus, the "Thévenin"-source can be replaced by a pure voltage source, as shown in Fig. 4-17 (a). Vice versa, for very high frequencies the input impedance of the HEMT becomes very small, so i_{GS} dominates and the "Thévenin"-source behaves more and more like an ideal current source, as Fig. 4-17 (b) depicts. In the latter case it is supposed that $Z_S \gg z_{IN}$, which is a valid approximation e.g. for a GaN HEMT in a 50 Ω environment at several GHz.

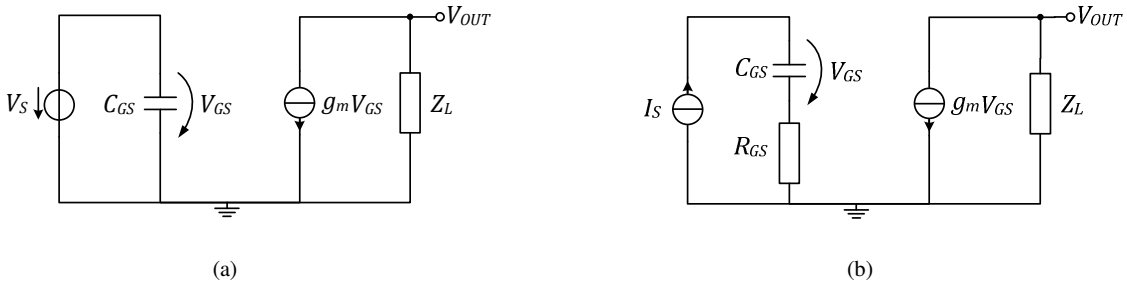


Fig. 4-17: (a) low frequency and (b) high frequency approximation of HEMT driven by a constant power source

From Fig. 4-17 (a) it can be now seen that V_{GS} cannot feature any distortion for low frequencies, because it is equal to the linear drive voltage V_S. The corresponding output nonlinearity contributed by C_{GS} is therefore equal to zero at low frequencies. For high frequencies in the contrary, V_{GS} in Fig. 4-17 (b) is solely evoked by the current I_S, which flows through the nonlinear capacitor C_{GS}, giving rise to nonlinearities in V_{GS} and hence at the output. The feedback provided by R_{GS} plays only a minor role in terms of linearity, because it only slightly reduces the V_{GS}-swing and therewith only shifts the input power dependent C_{GS}-nonlinearity. Unfortunately, at the same time R_{GS} reduces also the effective gain, which ends up referenced to the fundamental output signal in a similar HD. To put it into a nutshell, the nonlinearity contributed by C_{GS} rises with increasing frequency whereby its exact trend is dependent on the frequency characteristic of the input match of the HEMT. This leads to the question of perfect input matching for a HEMT over frequency in terms of optimum broadband linearity. The voltage transfer function $H_V(\omega)$ from V_S to V_{GS} in Fig. 4-16 can be determined to

$$H_V(\omega) = \frac{1}{1 + j\omega C_{\mathrm{GS}}(Z_S + R_{\mathrm{GS}})}. \tag{4.32}$$

Fig. 4-18 illustrates the magnitude of $H_V(\omega)$ for different Z_S for a 8×125µm GaN HEMT. For the inexistent ideal case of a frequency independent match with $Z_S = R_{\mathrm{GS}} - 1/j\omega C_{\mathrm{GS}}$, $H_V(\omega)$ would strive to infinity at DC

based on the perfect LC-compensation. If Z_S exhibits only a real-part, $H_V(\omega)$ saturates towards DC at unity when z_{IN} becomes much larger than Z_S. The smaller the $Re\{Z_S\}$ the higher is the corner frequency at which $H_V(\omega)$ falls below unity and C_{GS}-nonlinearities arise. The optimum source impedance Z_S in terms of linearity would be thus equal to zero, because V_{GS} is then equal to V_S for very small R_{GS} values, giving almost no room for any nonlinearity caused by i_{GS}, as also already depicted by Fig. 4-17(a).

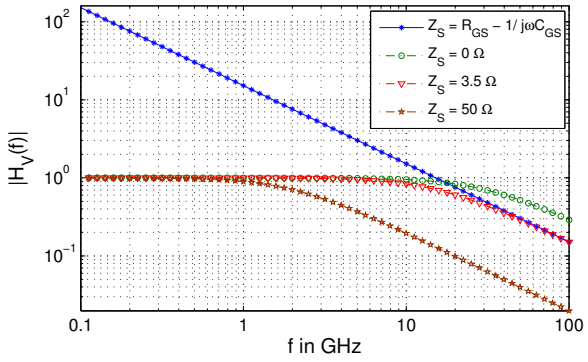


Fig. 4-18: Voltage transfer function $H_V(\omega)$ vs. f for different source impedances Z_S

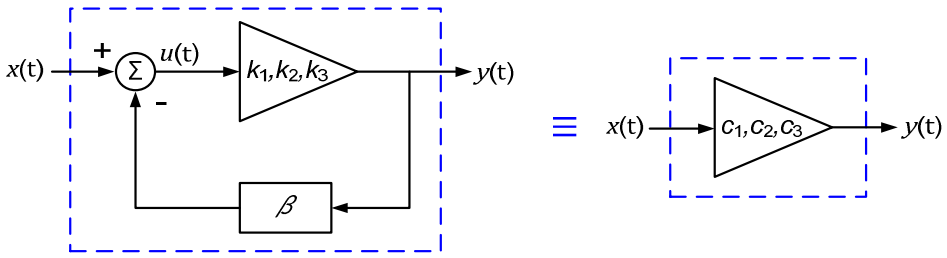
4.2.3 Key Findings

Nonlinearities arising in GaN HEMTs are mainly determined by the channel current I_{DS} and the nonlinear space-charge capacitance C_{GS}. The nonlinearity of the gate-drain space charge-charge capacitance C_{GD} can be in general neglected without introducing significant errors due to its roughly 10-15 times smaller magnitude. The dominating nonlinearity of I_{DS}, which can be expressed via a nonlinear g_m, is almost purely dependent on the drive signal amplitude V_{GS} whereas the nonlinear space-charge capacitance C_{GS} (and also C_{GD}) exhibits additionally frequency dependence, based on the fact that with increasing frequency the displacement current through C_{GS} (and also C_{GD}) increases. Correspondingly, the nonlinearity of C_{GS} leads to an increased nonlinear V_{GS} with increasing frequency. Since the resulting nonlinearity at the output caused by C_{GS} is only dependent on the nonlinearity of V_{GS}, the gate driving impedance level is also of major importance. If the gate is driven by a voltage source with low source impedance, V_{GS} is mainly determined by the voltage source and thus no nonlinearities in V_{GS} can occur. Contrarily, if the source impedance is highly resistive, V_{GS} is caused solely by the displacement current through the nonlinear C_{GS}. Additionally, the magnitude of the nonlinearity coming from C_{GS} is also dependent on the actual device size W_G. With increasing device size not only $C_{\mathrm{GS},0}$ increases almost linearly but also the dependence on V_{GS}.

4.3 Parallel and Series Feedback Linearization

One of the most familiar linearization concepts is feedback linearization, which was invented by H.S. Black at the Bell Laboratories and dates back to the year 1934 [138]. In his work he showed that by applying feedback to an amplifier the amplifier can be stabilized, the gain flattened and the BW further shifted up in frequency. Additionally, the impact of gain variations of the amplifier are greatly minimized by introducing feedback, so that thermal drift and aging effects could be diminished. It should take seven more years before the reviewers at the patent office were finally convinced that H.S. Black´s submitted patent on feedback linearization is actually plausible and was finally accepted in 1937. Nowadays, feedback linearization has been applied through all kind of different technologies and has become over the last 80 years a well-known method for linearization. [88, 90, 139, 140, 141, 142]. The linearity investigation on feedback in this chapter is closely related to W. Sansen´s excellent publication on distortion in elementary transistor circuits in [143].

4.3.1 Linearity in Feedback Systems



(a) (b)

Fig. 4-19: (a) Nonlinear feedback system with distortion coefficients k_n and unilateral feedback β and (b) its equivalent representation with converted distortion coefficients c_n

The output linearity of a weakly nonlinear system excited by a sinusoidal input signal has been described already in section 4.1.1 equation (4.2). If the feedback system from Fig. 4-19 is considered, the new Talyor-series coefficients c_n up to 3rd order can be expressed by the already known open loop coefficients k_n and the unilateral feedback transfer function β in an equivalent manner, as shown in [143]. By means of the feedback relationship $u(t) = x(t) - \beta \cdot y(t)$, replacement of $x(t)$ in (4.2) by $u(t)$ gives the following power series expressions for the system in Fig. 4-19.

$$\begin{aligned} y(t) &= k_1(x(t) - \beta \cdot y(t)) + k_2(x(t) - \beta \cdot y(t))^2 + k_3(x(t) - \beta \cdot y(t))^3 \\ &= c_1 x(t) + c_2 x(t)^2 + c_3 x(t)^3 \end{aligned} \tag{4.33}$$

Insertion of the second equation in (4.33) into the first leads to an equality where only the open loop (k_n) and closed loop (c_n) coefficients together with the unilateral feedback transfer function β are contained. After solving (4.33) for c_n, the coefficients of the power series for the nonlinear feedback system can be determined to (see also [143])

$$c_1 = \frac{k_1}{(1+A_l)} \tag{4.34}$$

$$c_2 = \frac{k_2}{(1+A_l)^3} \tag{4.35}$$

$$c_3 = \frac{k_3}{(1+A_l)^4} - \frac{2 \cdot A_l {k_2}^2}{k_1(1+A_l)^5}, \tag{4.36}$$

where $A_l = \beta \cdot k_1$ stands for the loop-gain. Equations (4.34) to (4.36) show that the higher the loop-gain A_{cl} the more degenerated are the higher order harmonics. Furthermore, the 3rd order coefficient c_3 in (4.36) exhibits a zero, so the contribution from the 2nd order nonlinearity k_2 of the amplifier cancels out the 3rd order nonlinearity k_3 at a certain amount of feedback. This dependency can be verified from the $HD3$ and $C/IM3$ dependency on the loop-gain A_l in Fig. 4-20, whereby the HD and C/IM incorporating feedback in (4.37)-(4.40) are computed from (4.5)-(4.6) and (4.8)-(4.9) for $A = V$.

$$\begin{aligned} HD2 &= \frac{1}{2}\frac{c_2 V^2}{c_1 V + \frac{3}{4}c_3 V^3} = \frac{1}{2}\frac{k_2(1+A_l)^2 V}{k_1(1+A_l)^4 + \frac{3}{4}\left(\frac{k_3}{(1+A_l)} - 2A_l\frac{{k_2}^2}{k_1}\right)V^3} \\ &\cong \frac{1}{2}\frac{k_2 V}{k_1(1+A_l)^2}, \qquad \text{for } V \ll 1 \end{aligned} \tag{4.37}$$

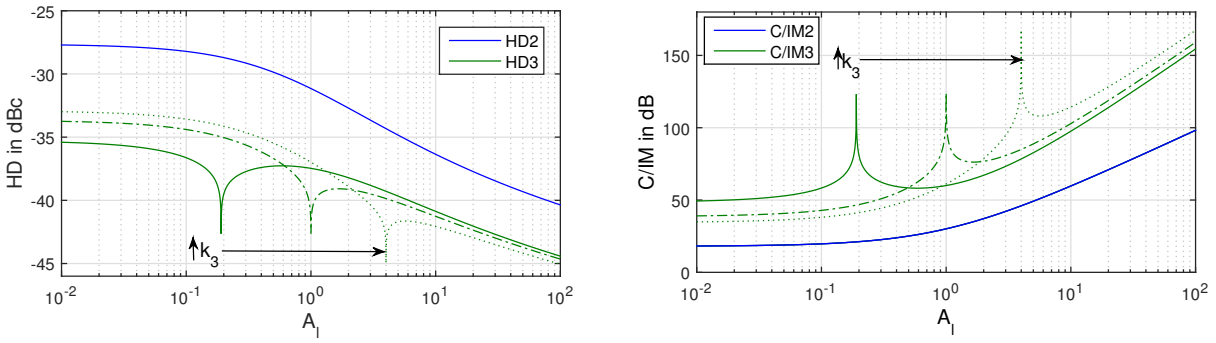
$$\begin{aligned} HD3 &= \frac{1}{4}\frac{c_3 V^3}{c_1 V + \frac{3}{4}c_3 V^3} = \frac{\left(k_3(1+A_l) - \frac{2A_l {k_2}^2}{k_1}\right)V^2}{4k_1(1+A_l)^4 + \left(3k_3(1+A_l) - 6A_l\frac{{k_2}^2}{k_1}\right)V^2} \\ &\cong \frac{1}{4}\left(\frac{k_3}{k_1}\frac{1}{(1+A_l)^3} - \left(\frac{k_2}{k_1}\right)^2\frac{2 \cdot A_l}{(1+A_l)^4}\right)V^2, \qquad \text{for } V \ll 1 \end{aligned} \tag{4.38}$$

$$\begin{aligned} \frac{C}{IM2} &= \frac{c_1 V + \frac{9}{4}c_3 V^3}{c_2 V^2} = \frac{k_1}{k_2 V}(1+A_l)^2 + \frac{9}{4}\left(\frac{k_3}{k_2}\frac{1}{(1+A_l)} - 2A_l\frac{k_2}{k_1(1+A_l)^2}\right)V \\ &\cong \frac{k_1}{k_2 V}(1+A_l)^2, \qquad \text{for } V \ll 1 \end{aligned} \tag{4.39}$$

$$\begin{aligned} \frac{C}{IM3} &= \frac{c_1 V + \frac{9}{4}c_3 V^3}{\frac{3}{4}c_3 V^3} = 3 + \frac{4}{3}\frac{k_1(1+A_l)^4}{\left(k_3(1+A_l) - 2A_l\frac{{k_2}^2}{k_1}\right)V^2} \\ &\cong \frac{4}{3}\frac{k_1(1+A_l)^4}{\left(k_3(1+A_l) - 2A_l\frac{{k_2}^2}{k_1}\right)V^2}, \qquad \text{for } V \ll 1 \end{aligned} \tag{4.40}$$

From (4.37) to (4.40) it can be again seen, that for small amplitudes ($V \ll 1$) the relationship $C/IMn = 1/(n \cdot HDn)$ is valid and the impact of the 3rd order nonlinearity on the fundamental can be neglected. More importantly, sweet-spots at a certain loop-gain A_l in the $HD3$ and $IM3$-products occur, which suppress the 3rd harmonic ($H3$) and give optimum in-band intermodulation performance ($C/IM3, OIP3$). When the amplifier's nonlinear coefficients k_1 to k_3 together with the loop-gain A_l satisfy the condition (4.41), full $H3/IM3$-cancellation at the output occurs. For $A_l = 1$ and $k_1 = 1$ the simple relationship of $k_2 > \sqrt{k_3}$ results (see dashed-dotted line in Fig. 4-20). The larger A_l gets the smaller has to be the difference between k_2 and k_3 in order to maintain the $H3/IM3$ sweet-spot and vice versa. It is important to bear in mind that $H3/IM3$-cancellation can only occur, when k_3 and k_1 exhibit the same sign, as the denominators in (4.38) and (4.40) reveal.

$$A_l = \frac{k_1 k_3}{2{k_2}^2 - k_1 k_3} \tag{4.41}$$



(a) (b)

Fig. 4-20: (a) HD and (b) C/IM-ratio vs. A_l of nonlinear feedback system with distortion coefficients $k_1 = 1$, $k_2 = 1/8$ and $k_3 = 5 \cdot 10^{-3}/\mathrm{V}^3$ (solid), $15.625 \cdot 10^{-3}/\mathrm{V}^3$ (dashed-dotted), $25 \cdot 10^{-3}/\mathrm{V}^3$ (dotted)

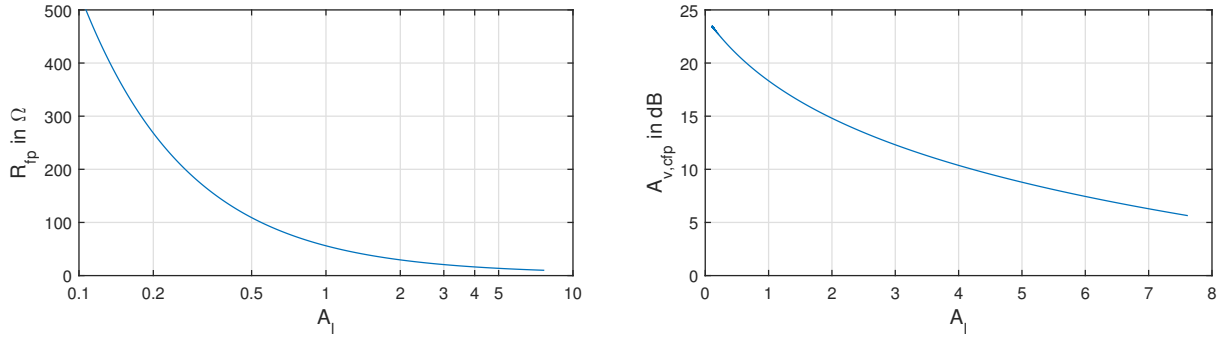
4.3.2 Linearization in GaN FBPAs

The before derived theoretical dependence will be translated to the topology of a CS-HEMT with parallel resistive feedback (series-shunt feedback) in the following. Since the presented approach is similar for series resistive feedback (shunt-series feedback) it will not be covered within this work. The analysis shall reveal, if the 3rd harmonic and the $IM3$-product can be fully eliminated in resistive FBPAs implemented in 0.25µm GaN technology by cancellation of the 3rd order nonlinearity through the 2nd order nonlinearity. First of all, the closed-loop gain and loop gain of the FBPA applying parallel resistive feedback needs to be determined. The voltage gain or closed-loop gain of a simple CS-HEMT with parallel feedback R_{fp} and load resistance R_L can be determined to

$$A_{v,cfp} = \left(1 - g_m R_{fp}\right) \frac{R_L}{R_L + R_{fp}}. \tag{4.42}$$

The corresponding open-loop gain is equal to $A_o = -g_m R_L$, wherefrom the loop gain $A_l = \beta \cdot A_o$ results in

$$A_l = \frac{g_m(R_L + R_{fp})}{g_m R_{fp} - 1} - 1. \tag{4.43}$$



(a) (b)

Fig. 4-21: (a) Loop gain A_l vs. R_{fp} and (b) closed-loop gain $A_{v,cfp}$ vs. A_l of parallel resistive FBPA for a 8×125µm HEMT

The loop-gain dependency of a 8×125µm HEMT with g_m = 0.33 S terminated with a load of R_L = 50 Ω on R_{fp} is plotted in Fig. 4-21 (a) above. It can be seen that the loop gain A_l lies for typical R_{fp} values, which are needed for a proper DC matching to 50 Ω (see 3.2.1), in the range from 50 Ω to 500 Ω between 0.1 to 1.0. The corresponding power gain, as shown in (b), is within this range between 18 and 23 dB, which is still sufficiently large. Turning back to the condition (4.41), the coefficients k_1 to k_3 in (4.40) can be now simply replaced by the Taylor series coefficients g_{m1}, $g_{m2}/2$ and $g_{m3}/6$, which describe the nonlinear channel current of the HEMT, as already presented in section 4.2.1. By insertion of the g_{mx}-coefficients for k_x into (4.41) and subsequently setting (4.41) equal to (4.43), the exact value for R_{fp}, which leads to an $IM3$ sweet-spot can be determined to

$$R_{fp,c} = \frac{3{g_{m2}}^2}{{g_{m1}}^2 g_{m3}} + R_L\left(\frac{3{g_{m2}}^2}{g_{m1}g_{m3}} - 1\right). \tag{4.44}$$

Equation (4.44) reveals, that not only the g_{mx}-ratios but also the absolute value of R_L plays an important role for the $H3/IM3$-cancellation. As soon as the condition $3{g_{m2}}^2 > g_{m1}g_{m3}$ is satisfied, $R_{fp,c}$ stays always positive. If $3{g_{m2}}^2$ is smaller than the product of g_{m1} and g_{m3}, condition (4.45) needs to be fulfilled to still retain positive values for $R_{fp,c}$.

$$\frac{1}{g_{m1}} > \left(1 - \frac{3{g_{m2}}^2}{g_{m1}g_{m3}}\right) R_L \tag{4.45}$$

Furthermore, a negative g_{m3} leads always to negative values for $R_{fp,c}$, showing that under such condition no $H3/IM3$-cancellation is possible, as already mentioned in the section before. So far, the exact dependencies and conditions for the presence of an $HD3/C/IM3$ sweet-spot have been analytically derived.

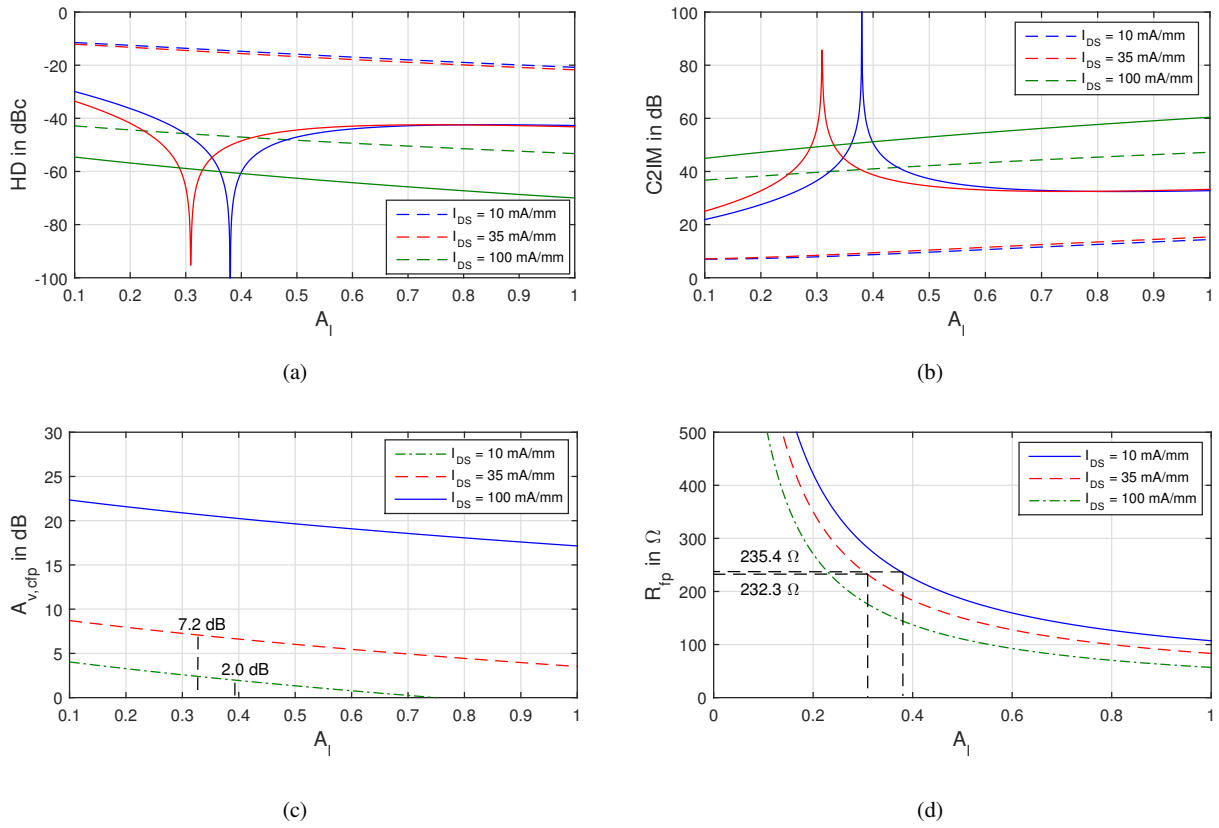


Fig. 4-22: (a) $HD2$ (dashed) & $HD3$ (solid) vs. A_l, (b) $C/IM2$ (dashed) & $C/IM3$ (solid) vs. A_l, (c) $A_{v,cfp}$ vs. A_l and (d) R_{fp} vs. A_l of an 8×125µm FBPA with parallel resistive feedback for the distortion coefficients at I_{DS} = 10, 35 and 100 mA/mm from Table 4-1

To obtain a final statement about the usability of the $H3/IM3$-cancellation in GaN25 technology, the derivatives of the transconductance (g_{m1}, g_{m2} and g_{m3}) for a 8×125µm HEMT were taken from the large-signal model (see Fig. 4-10). The values given in Table 4-1are for the different bias points of V_{DS} = 28 V and I_{DS} = 10, 35, 100, 200 & 300 mA/mm with R_L = 50 Ω. As can be clearly seen, the g_{m3} exhibits mainly a negative sign within the class AB-A range, giving negative values for $R_{fp,c}$. Only for very deep class AB-B operation below I_{DS} = 35 mA/mm becomes g_{m3} positive and $H3/IM3$-cancellation can be successfully exploited, as also demonstrated in Fig. 4-22. For the two bias-points at I_{DS} = 10 & 35 mA/mm, a much higher 2nd as well as 3rd order nonlinearity can be observed from the HD and C/IM curves, when approaching open-loop gain condition ($A_l = 0$) opposed to the bias-point I_{DS} = 100 mA/mm. This is in accordance with the higher $g_{m2/3}$-values in Table 5-1 for the two deep class AB-B bias-points. As soon as the loop-gain increases, a clear sweet-spot can be noticed in the two plots, where the 3rd order nonlinearity can be completely cancelled and the corresponding $HD3$ values and $C/IM3$-ratios outperfrom the "more linear" bias point of I_{DS} = 100 mA/mm. As the negative value for $R_{fp,c}$ or g_{m3} already reveals in Table 4-1, no linearity sweet-spots for I_{DS} = 100 mA/mm exist in Fig. 4-22 (a) and (b).

Table 4-1: Derivatives of the nonlinear channel current for I_{DS} = 10, 35, 100, 200 & 300 mA/mm and V_{DS} = 28 V

I_{DS} / mA/mm	10	35	100	200	300
g_{m1} / mS	35	60	290	265	240
g_{m2} / mS/V	50	77	10	0.6	-0.14
g_{m3} / mS/V²	59	70	-17	-1.3	-0.15
$R_{fp,c}$ / Ω	235.4	232.3	-53.25	-50.17	-50.09
A_l	0.380	0.309	-	-	-

The downside of this approach is that the de-/increase in $HD3$ and $C/IM3$ comes at the cost of small-signal gain, because g_{m1} drops also below 20% of its maximum gain at roughly 100 mA/mm to values below 60 mS. This dependency can be also seen in (c), where the gain of the FBPA drops at the sweet-spot for I_{DS} = 35 mA/mm at A_l = 0.309 to roughly 7.2 dB and for I_{DS} = 10 mA/mm at A_l = 0.380 even down to 2 dB. Moreover, because the second harmonic is much larger for the deep class AB-B bias-point and thus dominates, the overall HD-performance is strongly degraded. Based on these findings, $H3/IM3$-cancellation cannot be utilized with respect to the given specifications from Table 1-1 in the FBPA design in chapter 3.3.4, where low harmonics are vital. Since HD-performance needs to be sacrificed to lower the in-band $IM3$-products, this approach is only useful in narrow-band designs, where any HD falls out of the BW of interest.

4.3.3 Key Findings

Feedback Linearization is a well-known and suitable concept to realize broadband linearization for PAs. Within this section the trade-off between the amount of applied feedback and the implications on the even- and odd-order harmonics as well as in-band intermodulation products were examined from a very general point of view. Analytical calculations based on a Taylor series expansion, which describe the weak nonlinearity of the HEMT's channel current, showed that with increasing loop-gain (feedback) the even- as well as odd-order linearity can be improved effectively. Interestingly under specific conditions, the 3rd harmonic ($H3$) as well as the $IM3$-product can be completely cancelled, as long as the relationship (4.41) is satisfied by the Taylor-series coefficients k_n and the loop gain A_l of the feedback PA. Based on this analytical finding, the linearity investigation was further extended to the GaN25 process, where k_n was simply replaced by the derivatives of the I_{DS} vs. V_{GS} characteristic of a 8×125µm HEMT. By means of a simplified low frequency HEMT model, A_l was first of all computed for a parallel resistive feedback PA dependent on the transconductance g_m, the feedback resistance R_{fp} and the load resistance R_L of the FBPA. In a next step, a boundary condition for R_{fp} was derived, where the value of $R_{fp,c}$ serves as an indicator for the general presence of $H3$ and $IM3$-cancellation for a given set of $g_{m,n}$-values. As long as $R_{fp,c}$ is negative, no 3rd order nonlinearity sweet-spot is present. If the set of $g_{m,n}$-values gives positive values for $R_{fp,c}$, 3rd order nonlinearity cancellation can be realized within a parallel FBPA design. Furthermore the analysis shows that negative $g_{m,3}$-values always impede the generation of a sweet-spot. Based on this latter finding it can be thus asserted that class AB to A biasing never leads to a $H3/IM3$-sweet-spot in feedback based designs, making it impossible to exploit this beneficial linearization feature in the design of class A parallel FBPAs. Although, for very deep class AB to B bias the positive $g_{m,3}$ characteristic proved to enable the cancellation of the $g_{m,2}$ contribution to the $H3$ and $IM3$-product for the GaN25 process, but with the downside of reducing gain and increasing 2nd order nonlinearities.

4.4 Staggering Drain-Line Principle in TWAs

In this section linearity of the TWA topology from a purely theoretical point of view will be regarded. First of all, the HD for a single tone CW signal is examined and later, the intermodulation for a two tone CW-signal with narrow frequency spacing. The dependency of the the $HD2$, $HD3$ and $C/IM3$ on additional phase delays on the gate- or drain-line, further referred to as "staggering", will be investigated and the possible improvements assessed. For the calculation of the $HD2$, $HD3$ and $C/IM3$, the following simplifying assumptions are made:

- the input and output impedance each transistor stage sees in the TWA is constant over frequency.
- the calculation of the $HD2$ and $HD3$ is only valid up to half and respectively one-third of the TWA´s operational bandwidth. Above these frequencies the out of band impedance for the 2nd and 3rd harmonic changes significantly, violating the prior mentioned condition.
- the T-line attenuation α is constant and the phase coefficient β shows a linear dependency over frequency/electrical length, which is a simplifying but reasonable approximation for a real design.

4.4.1 Harmonic Distortion

According to these approximations the theoretical dependency of the HD content of the output signal on the gate- and drain line lengths (l_G, l_D) and the number of stages (N) can be established. Fig. 4-23 sketches a typical UDPA with 3rd order harmonic signal content at frequency 3ω on the drain-line, generated by the nonlinearity of the transistors when a sinusoidal input signal of the form $V_{IN} = a \cdot \cos(\omega t)$ is applied at the input. These harmonics travel with m-times the frequency on the drain-line toward the output, which results in an m-times larger phase coefficient β_D via the relationship $\beta_D = m \cdot \omega\sqrt{LC}$. For simplicity reasons, the attenuation on gate- and drain-line is equal to zero ($\alpha_G = \alpha_D = 0$), because no impact on linearity is to be expected over frequency by consideration of a constant attenuation.

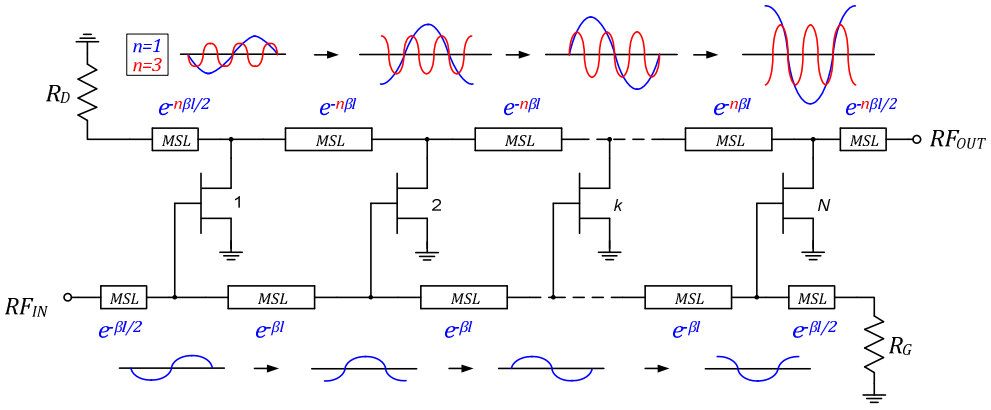


Fig. 4-23: Sketch of the drain-line propagation difference between fundamental and 3rd harmonic due to nonlinear transistors in a UDPA

In general the m^{th}-harmonic output current $I_{N,m}$ of an N-stage UDPA into the output load at port RF_{OUT} can be expressed via the relationship

$$I_{N,m} = \frac{1}{2}\frac{g_{m,m}a^m}{m!}\, e^{-j\frac{n}{2}(\beta_G l_G + m\cdot\beta_D l_D)} \frac{sin\left(\frac{n}{2}(\beta_G l_G - m\cdot\beta_D l_D)\right)}{sin\left(\frac{1}{2}(\beta_G l_G - m\cdot\beta_D l_D)\right)}, \tag{4.46}$$

where the amplitude of the m^{th}-harmonic output signal is solely described by a Taylor series expansion of the nonlinear transconductance, as already described in (4.20) in chapter 4.2.1. By means of (4.46) the m^{th}-order HD can thus be derived to

$$HDm = \frac{a^{m-1}}{m!}\frac{g_{m,m}}{g_{m,1}} \cdot e^{-j\frac{n}{2}(m-1)\beta_D l_D} \cdot \frac{sin\left(\frac{n}{2}(\beta_G l_G - m\cdot\beta_D l_D)\right)\cdot sin\left(\frac{1}{2}(\beta_G l_G - \beta_D l_D)\right)}{sin\left(\frac{1}{2}(\beta_G l_G - m\cdot\beta_D l_D)\right)\cdot sin\left(\frac{n}{2}(\beta_G l_G - \beta_D l_D)\right)} \tag{4.47}$$

In a final step the total output current of the fundamental signal $I_{N,1}$ can be made independent of the number of stages for a better assessment of the resulting HD. By solving (4.46) for a (m = 1) and setting $I_{N,1}$ to a constant value, as e.g. unity, (4.47) can be rewritten to

$$HDm = \frac{2^{m-1}}{m!}\frac{g_{m,m}}{{g_{m,1}}^m} \cdot e^{j\frac{n}{2}(m-1)\beta_G l_G} \cdot \frac{sin\left(\frac{n}{2}(\beta_G l_G - m\cdot\beta_D l_D)\right)}{sin\left(\frac{1}{2}(\beta_G l_G - m\cdot\beta_D l_D)\right)}\left(\frac{sin\left(\frac{1}{2}(\beta_G l_G - \beta_D l_D)\right)}{sin\left(\frac{n}{2}(\beta_G l_G - \beta_D l_D)\right)}\right)^m . \tag{4.48}$$

The plots in Fig. 4-25 show the $HD2$ and $HD3$ according to (4.48) for m = 2 and m = 3 versus a difference in electrical length between the gate- and drain-line sections ($\Delta E_l = \beta_G l_G - \beta_D l_D$) and for different number of stages. In order to simply show the theoretical dependence of the HD and the resulting power gain G_P on a mismatch of the propagation constants and the number of stages N, the Taylor series coefficients which express the nonlinear drain currents were chosen equal to $g_{m,1}$= 1, $g_{m,2}$= 0.1 and $g_{m,3}$ = 0.01. As expected, from (a) and (b) it can be seen that for a single distributed transistor stage the $HD2$ and $HD3$ performance in dBc is independent on the propagation mismatch and equal to $20\cdot\log(g_{m,2}/g_{m1})$ and $20\cdot\log(2g_{m,3}/(3g_{m,1}))$, respectively. As the number of stages increases, the HD further improves, as was also already mentioned by V. Paschalidou and C. Aitchison in [144]. For equal propagation constants the dependence of HDm on N is only determined by the sin-terms in (4.48), which can be further reduced to

$$\frac{sin\left(\frac{n}{2}(\beta_G l_G - m\cdot\beta_D l_D)\right)}{sin\left(\frac{1}{2}(\beta_G l_G - m\cdot\beta_D l_D)\right)}\left(\frac{sin\left(\frac{1}{2}(\beta_G l_G - \beta_D l_D)\right)}{sin\left(\frac{n}{2}(\beta_G l_G - \beta_D l_D)\right)}\right)^m = \left(\frac{1}{N}\right)^{m-1} . \tag{4.49}$$

As the plot of (4.49) in Fig. 4-24 reveals, the higher the order of the harmonics, the larger the improvement in HD. In order to reduce e.g. the $HD2$ by 10 dB, N needs to be increased from 4 to 10 stages, whereas for the $HD3$ a number of N = 7 stages would be sufficient. It can be concluded that the highest $SFDR$ will be obtained in a UDPA, when the maximum number of stages is taken.

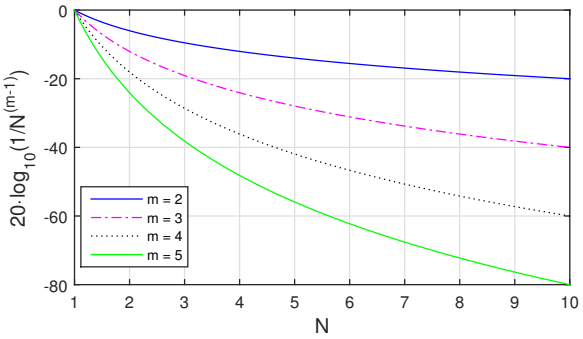


Fig. 4-24: Dependency of HDm vs. N in dB for equal gate- and drain-line phase coefficients

It can be furthermore deduced that sweet-spots occur at propagation mismatches of $\Delta E_l = 180°/N$ for the $HD2$ and $\Delta E_l = 120°/N$ for the $HD3$, as Fig. 4-25 reveals. These sweet-spots repeat for the $HD2$ at odd-numbered multiples, whereas for the $HD3$ the even-numbered multiples of these electrical lengths yield again 2nd or 3rd order spurious free output signals. The so called "staggering drain-line principle" makes use of exactly this dependency of the nonlinear terms on the propagation mismatch. Taking a closer look onto (c) reveals that the sacrifice for lower HD comes at the cost of decreasing gain. To operate a UDPA with e.g. $N = 6$ stages in the $HD2$ sweet-spot, the mismatch between $\beta_G l_G$ and $\beta_D l_D$ has to be equal to 30° per section, which leads according to (c) to a reduced gain by roughly 3.8 dB from 28 dB to 24.2 dB. Based on the larger phase velocity of the 3rd harmonic, this situation is more relaxed for the $HD3$, where operation in the sweet-spot requires only 2/3 of the $HD2$ propagation mismatch, giving only 20° and accordingly only 2 dB less gain. It can be thus inferred that higher order nonlinearities can be more easily suppressed by the staggering drain-line principle than lower order nonlinearities. Unfortunately, the 2nd and 3rd order nonlinearities are in most technologies the dominant distortions, which need to be suppressed or eliminated to obtain high linearity in the application. Another drawback not tackled up to now is the reduced bandwidth of the UDPA, which accompanies the staggering of the dran-line. By means of (3.75) for $\alpha_G = \alpha_D = 0$ and $R_{GS} = 0\ \Omega$, the power gain of the TWA with no losses results in

$$G_P = \frac{{g_m}^2 Z_G Z_D}{4} \cdot \left| e^{-j\frac{N}{2}(\beta_G l_G + \beta_D l_D)} \cdot \frac{sin\left(\frac{N}{2}(\beta_G l_G - \beta_D l_D)\right)}{sin\left(\frac{1}{2}(\beta_G l_G - \beta_D l_D)\right)} \right|^2 . \tag{4.50}$$

Fig. 4-26 plots the normalized power gain of (4.50) versus the normalized frequency in a UDPA with $N = 6$ stages for different additive phase delays $\Delta\Phi_d$ on the drain-line. It can be inferred that the larger $\Delta\Phi_d$ becomes and the closer the UDPA operates at its maximum corner frequency, the higher are the losses in power gain. Picking up the example for $N = 6$ stages, Fig. 4-25 (a) reveals that in order to achieve optimum $HD2$ performance $\Delta\Phi_d$ needs to be equal to 30° for the sweet-spot. This translates according to Fig. 4-26 now into a gain-drop of around 3.8 dB at f_{max} compared to the ideal case of $\Delta\Phi_d = 0$. Exactly this value was already read from the G_P vs. ΔE_l plot in Fig. 4-25 (c) for the $HD2$ sweet-spot. As Fig. 4-26 for $\Delta\Phi_d = 10°$ illustrates in contrast, the gain loss over the whole BW amounts to only 0.4 dB, which would correspond for $\Delta\Phi_d = 30°$ to only one-quarter of the BW. It can be thus summarized that in order to realize constant gain in the staggering drain-line concept but significant improvement in HD performance, the BW of the UDPA is significantly reduced. Out of

this reason, the staggering drain-line linearization approach was not furthermore pursued for an implementation in hardware under the targeted specifications of gain and BW from Table 1-1.

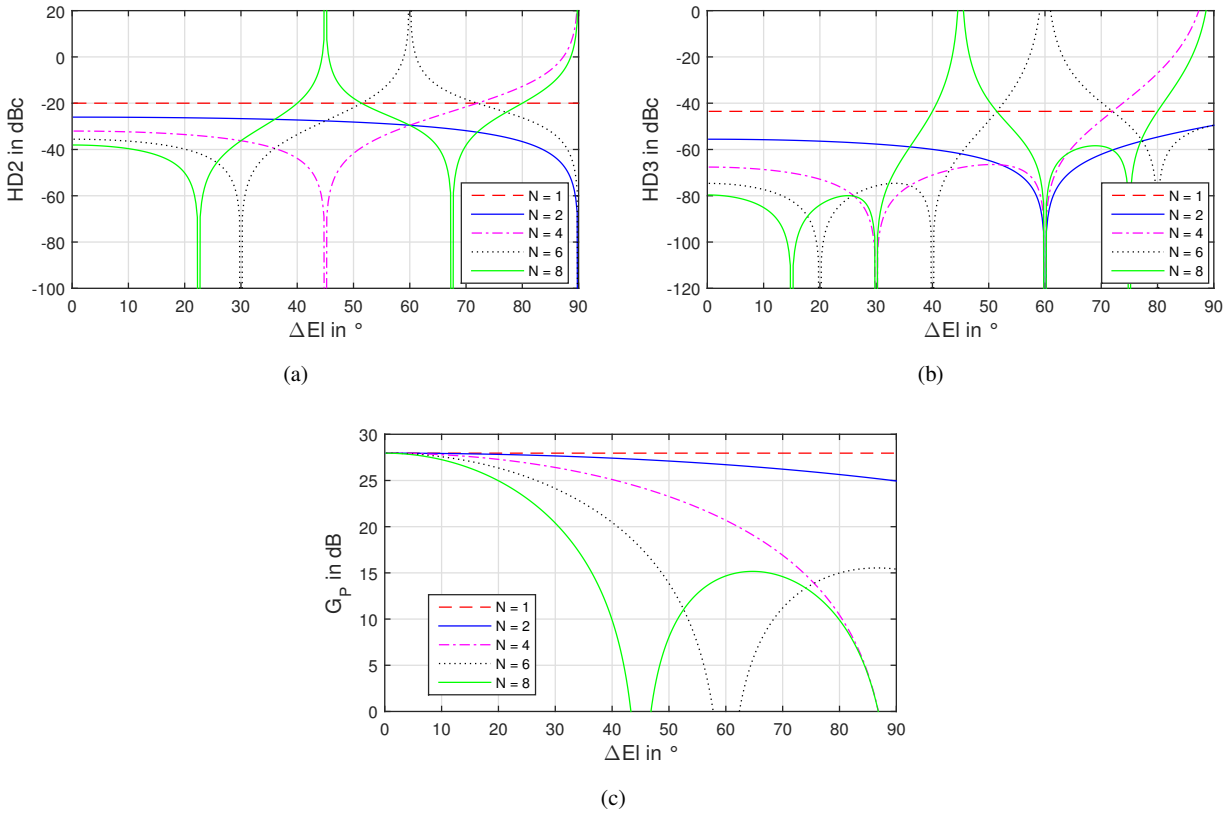


Fig. 4-25: (a) $HD2$, (b) $HD3$ and (c) G_P of fundamental vs. ΔE_l for different number of stages N in a UDPA

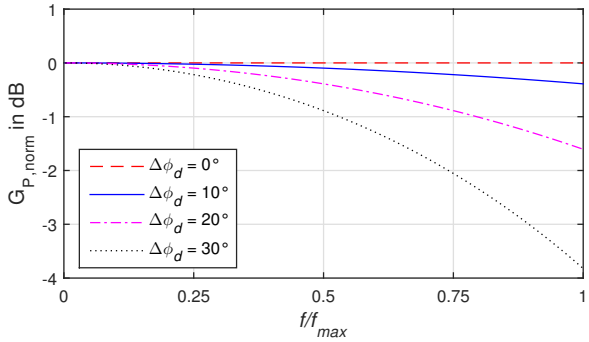


Fig. 4-26: Dependency of G_P vs. f/f_{max} in dB and $N = 6$ for a staggered drain-line with an additional phase offset $\Delta\Phi_d$ at f_{max}

4.4.2 Intermodulation

As already shown by C. Aitchison and M. Mbabele in [145] based on the findings by V. Paschalidou and C. Aitchsion much earlier in 1985 [144], the $C/IM3$-ratio can be in principle improved in DAs by simply increasing the number of stages. Assuming the loss-free limiting case and equal phase velocities on gate- and drain-lines, C. Aitchison and M. Mbabele showed that the $C/IM3$-ratio for negligible losses on the drain-line is theoretically propoprtional to N^4. This is in close relationship to the investigations conducted in the previous section, where the HD showed to improve for a constant output power with increasing number of stages by a factor of $(1/N)^{m-1}$. Similar to the HD considerations in the previous chapter deals this section with the dependency of intermodulation products on gate- and drain-line propagation mismatch under the consideration of lossless gate- and drain-lines.

Considering the following two sinusoidal input drive signals of the form $V_{IN1} = a_1 \cdot \cos(\omega_1 t)$ and $V_{IN2} = a_2 \cdot \cos(\omega_2 t)$, which pass through the 3rd order nonlinearity of the transistors, yield spectral output current components according to $I_{N,3} = g_{m,3}(V_{IN1} + V_{IN2})^3 / 3!$ at the drain of each transistor. Only the mixing terms at frequencies of $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ with a corresponding amplitude of 1/8 ${a_1}^2 a_2 g_{m,3}$ and 1/8 $a_1 {a_2}^2 g_{m,3}$ produce the well known in-band spectral 3rd order intermodulation products ($IM3$), which are close to ω_1 and ω_2 and therefore cannot be filtered out. Since the two fundamental input signals at ω_1 and ω_2 are close to the $IM3$ products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, no significant difference in phase velocity is to be expected, opposed to the case for the HD where the m^{th}-harmonic travels with m-times the phase velocity. Nevertheless, due to the strong dependency of the $IM3$ products on ${V_{IN}}^3$, the phase velocity on the gate-line appears to be three times as high as on the drain-line. This leads to the following total $IM3$ current at the output of

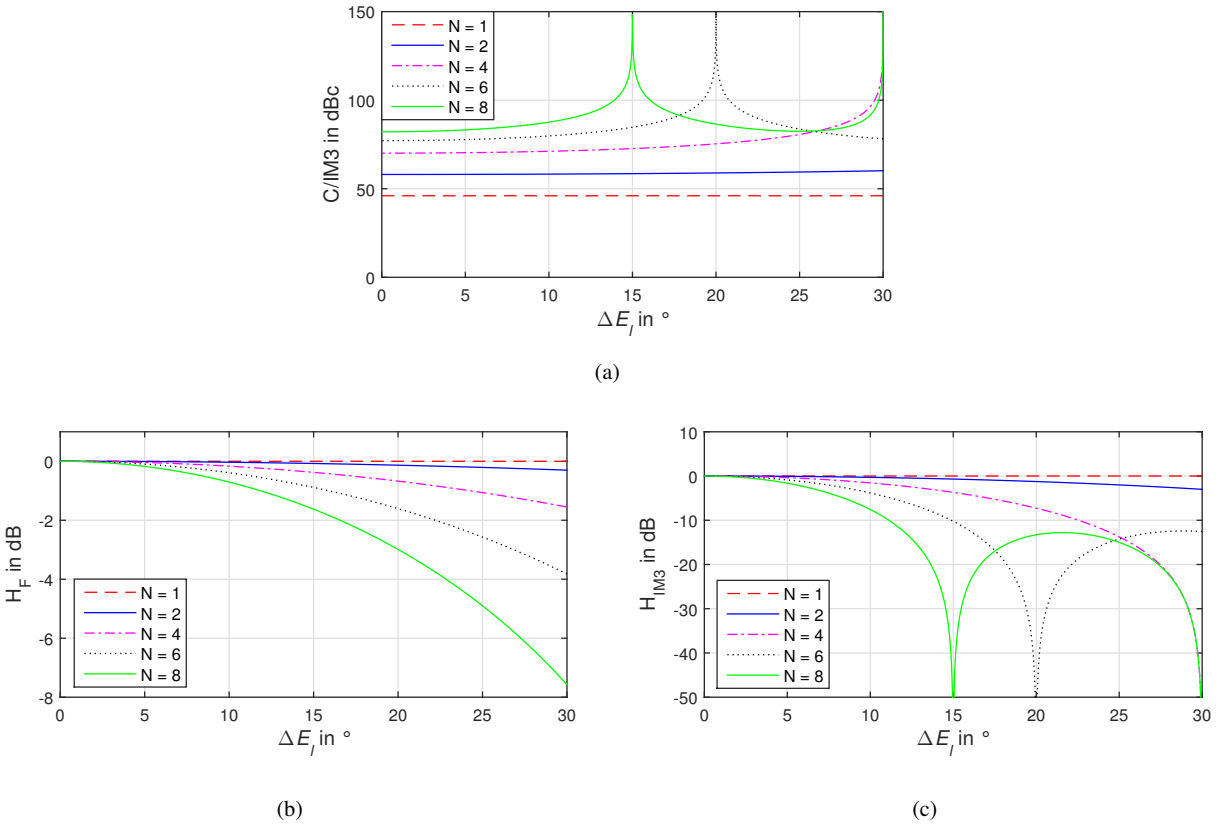
$$I_{N,IM3} = \frac{1}{16} {a_1}^3 g_{m,3}\, e^{-j\frac{n}{2}(3\beta_G l_G + \beta_D l_D)} \frac{sin\left(\frac{n}{2}(3\beta_G l_G - \beta_D l_D)\right)}{sin\left(\frac{1}{2}(3\beta_G l_G - \beta_D l_D)\right)}, \tag{4.51}$$

where $a_1 = a_2$ is assumed for simplicity reasons. The impact of the 3rd order nonlinearity on the fundamental is for simplicity neglected herein, since it is negligibly small under small-signal operation. To obtain the $C/IM3$-ratio, the fundamental (m = 1 in (4.46)) needs to be set into relation to (4.51), giving

$$\frac{C}{IM3} = \frac{8 \cdot g_{m,1}}{g_{m,3} \cdot {a_1}^2} \cdot e^{jn\beta_g l_g} \cdot \frac{sin\left(\frac{n}{2}(\beta_g l_g - \beta_d l_d)\right)}{sin\left(\frac{1}{2}(\beta_g l_g - \beta_d l_d)\right)} \cdot \frac{sin\left(\frac{1}{2}(3\beta_g l_g - \beta_d l_d)\right)}{sin\left(\frac{n}{2}(3\beta_g l_g - \beta_d l_d)\right)}. \tag{4.52}$$

After normalization of the fundamental signal current to the number of stages N, as was also done within the HD calculations, the $C/IM3$-ratio finally results in

$$\frac{C}{IM3} = \frac{2{g_{m,1}}^3}{g_{m,3}} \cdot e^{-jn\beta_D l_D} \cdot \left(\frac{sin\left(\frac{n}{2}(\beta_G l_G - \beta_D l_D)\right)}{sin\left(\frac{1}{2}(\beta_G l_G - \beta_D l_D)\right)} \right)^3 \cdot \frac{sin\left(\frac{1}{2}(3\beta_G l_G - \beta_D l_D)\right)}{sin\left(\frac{n}{2}(3\beta_G l_G - \beta_D l_D)\right)}. \tag{4.53}$$



(a)

(b)

(c)

Fig. 4-27: (a) $C/IM3$, (b) H_F of the fundamental and (c) H_{IM3} of the intermodulation products vs. ΔE_l for different number of stages N in a UDPA

Fig. 4-27 (a) depicts equation (4.53) vs. phase delay ΔE_l of a staggered drain-line, dependent on the number of stges N. Similar to the $HD3$ graph in Fig. 4-25 (b), a full suppression of the $IM3$ components occurs every $120°/N$, as also shown by the $IM3$-transfer function in Fig. 4-27 (c). In combination with the much weaker phase delay dependence of the fundamental signal in (b), the $C/IM3$-ratio can be improved significantly by introducing an additional phase delay on the drain-line, as was also presented in [146]. This improvement of the $C/IM3$-ratio, which can be one-to-one transferred to the $OIP3$ by means of the relationship derived and presented in section 4.1.2, comes again at the cost of gain and BW, as depicted in (b).

4.4.3 Key Findings

By means of some simplified considerations, the single-tone linearity in form of the HD as well as the two-tone intermodulation performance in form of the $C/IM3$-ratio were analytically derived for a UDPA. The overall linearity is very dependent on the number of sections N and on the different phase delays of the gate- and drain-line in a UDPA. From the theoretical analysis it emerged that with increasing number of stages N, the HD as well as the $C/IM3$-ratio improves, assuming a constant total device size (TGW). As far as the author is aware, the general HD dependency on N has been identified for the first time to be proportional to $HDm{\sim}(1/N)^{m-1}$ in a UDPA. The improvement of the $C/IM3$-ratio with increasing N on the contrary has already been reported in [144, 145]. Furthermore, by introducing some additional delay on the drain-line in form of line-length staggering, the linearity additionally can be improved at the expense of gain and BW. In general it can be stated that higher order nonlinearities can be reduced with less loss in gain and BW performance than the lower order nonlinearities. Based on these findings and the given gain and BW specifications from Table 1-1, the staggering drain-line linearization concept was not further pursued within this work. Because full suppression of the dominating 2nd harmonic would require a phase delay of 180°/N per section, which leads to a significant reduction in gain by almost 5 dB or a severe limitation in BW. Nevertheless, for applications with relaxed BW requirements and where harmonic distortion is not of major importance but rather intermodulation performance, this concept proves to be an efficient approach for improving the two-tone linearity of TWAs.

4.5 Derivative Superposition Method

The derivative superposition method (DSM) is a linearization concept which dates back to the year 1996, where D. Webster presented for the first time a linearization technique taking advantage of the alternating sign of the 3rd order derivative of the transconductance g_m [147]. The first section 4.5.1 discusses first of all the general principle of the DSM by making use of a HEMT with ideal transfer characteristic. With the obtained knowledge from chapter 4.2.1 for the bias point and input power dependencies of the channel current nonlinearity of a single CS-HEMT, the applicability of the DSM principle in 0.25µm GaN-technology will be investigated in section 4.5.2.

4.5.1 General DSM Principle

Fig. 4-28 sketches the basic principle of the DSM for n equally sized parallelized HEMTs, where the different bias voltages are set by a resistive divider ladder. The inductances shall additionally prevent intercoupling between the stages at high frequencies, but can be also omitted.

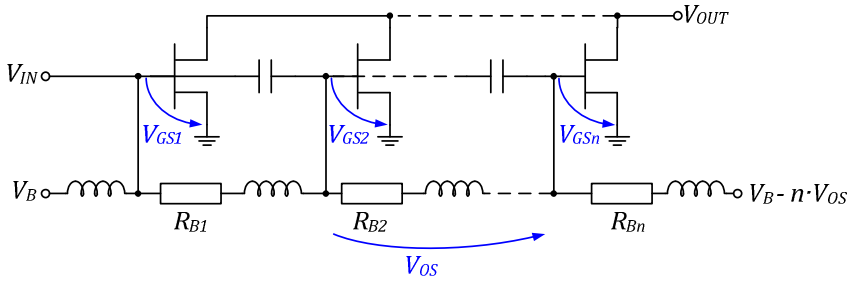
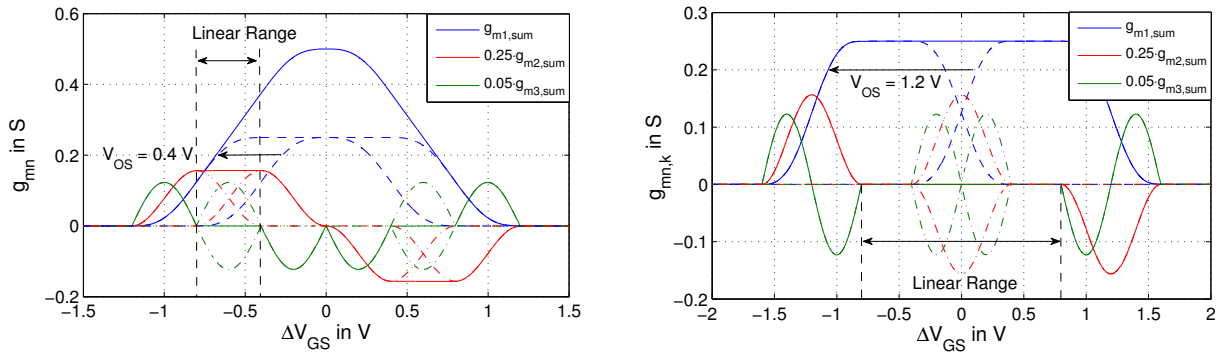


Fig. 4-28: Schematic of the derivative superposition method applied to HEMTs via resistive voltage division

By introducing some offset voltage between each transistor, each transistor operates at a different V_{GS}, as Fig. 4-28 shows. If the offset between the kth and the (k+1)th HEMT in Fig. 4-28, is chosen in such a manner that the summation of the 3rd order derivative yields zero over the maximum possible input power range, the 3rd order nonlinearity and hence $HD3$ and the $IMD3$ products are significantly minimized. The higher the number of stages, the broader is the 3rd order input power cancellation range. But before focusing on the implementation with GaN HEMTs, the idealized HEMT introduced in chapter 4.2.1 is taken to gain a principle understanding of the DSM. In general there are two different approaches to end up in an optimum g_{m3} cancellation, which are displayed by the idealized HEMT transfer characteristics in Fig. 4-29 (a) and (b).

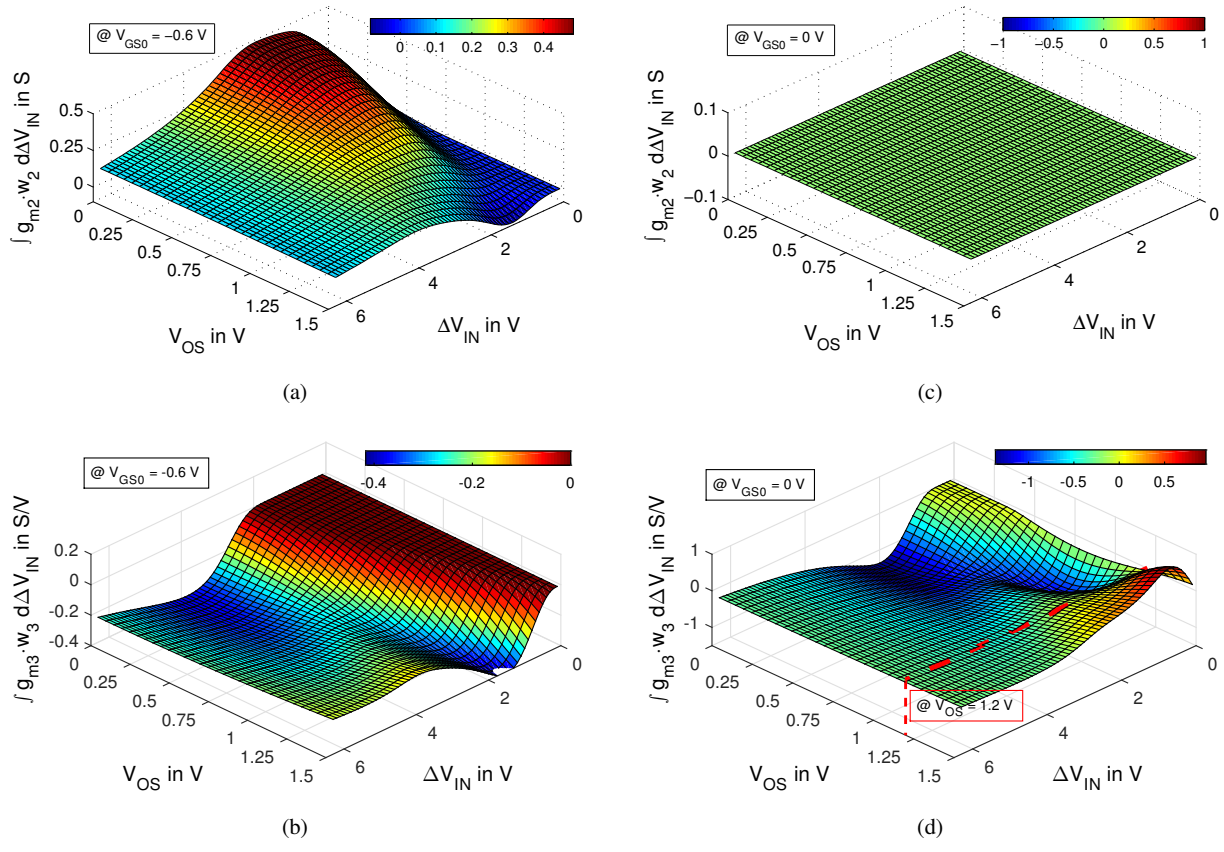
In the first case, V_{OS} is chosen equal to 0.4 V between two HEMTs in order to cancel the negative g_{m3}-part by the positive g_{m3}-part of the offset HEMT, as depicted in Fig. 4-29 (a). The corresponding optimum bias point is then located at a bias voltage of ΔV_{GS} = -0.6 V in class AB to realize a 3rd order nonlinearity compensation up to an input voltage swing of ΔV_{IN} = 0.4 V. Unfortunately, the g_{m2}-contribution is not cancelled at this bias point but only shows no input power dependency up to a signal swing of ΔV_{IN} = 0.4 V. For the second case in Fig. 4-29 (b), the shift in offset voltage is chosen equal to V_{OS} = 1.2 V. Thereby, the 3rd order nonlinearity resulting from the positive slope of the g_{m1}-curve exactly is cancelled by the one caused by the negative slope, as long as the g_{m1}-curve is fully symmetric. The corresponding optimum bias point is then located at a bias

voltage of ΔV_{GS} = 0 V in class A to realize a 3rd order nonlinearity compensation up to an input voltage swing of ΔV_{IN} = 1.6 V. It can be immediately inferred that the linear range is thus much larger for V_{OS} = 1.2 V than for V_{OS} = 0.4 V. If the 2nd order nonlinearity is also of concern, the sum of g_{m2} shows in Fig. 4-29 (a) that the 2nd order distortion is not nulled around ΔV_{GS} = -0.6 V, whereas in Fig. 4-29 (b) also g_{m2} will stay zero over almost the same input power range as g_{m3} does.



(a) (b)

Fig. 4-29: g_m-transfer characteristics of DSM applied to two HEMTs for (a) V_{OS} = 0.4 V and (b) V_{OS} = 1.2 V

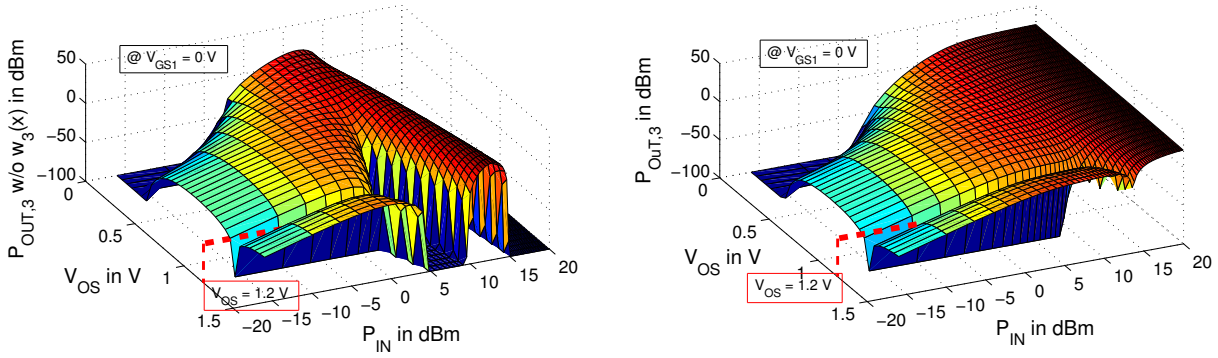


(a) (c)

(b) (d)

Fig. 4-30: Weighted integrals of (a) g_{m2} and (b) g_{m3} at V_{GS0} = -0.6 V and (c) g_{m2} and (d) g_{m3} at V_{GS0} = 0 V over different input voltage swings ΔV_{IN} and different offsets V_{OS} of the DSM applied to two ideal HEMTs

Fig. 4-30 illustrates the dependency of the g_{m2}- and g_{m3}-integral weighted by $w_n(x)$ from equation (4.20) over different input signal swings ΔV_{IN} and now also for various offset voltages V_{OS}. The plots (a) and (b) show that for V_{GS0} = -0.6 V the best 3rd order harmonic cancellation over large input signal swings is achieved for small V_{OS} values, whereas the best 2nd order harmonic cancellation is obtained at large V_{OS} values. In contrast to this contradicting trade-off between 2nd and 3rd order linearity, Fig. 4-30 (b) and (d) with V_{OS} = 1.2 V shows that optimum 2nd and 3rd order linearity over a peak-to-peak input voltage swing from 0 V to 1.6 V can be maintained. Whereas for g_{m2} in Fig. 4-30 (c) the ideal cancellation is independent of ΔV_{IN} and V_{OS} based on the even symmetry of g_{m2} around V_{GS0} = 0 V, the 3rd order nonlinearity starts to deteriorate for larger swings than 1.6 V due to the additional negative g_{m3}-area, as Fig. 4-29 (b) depicts. At an input signal swing of ΔV_{IN} > 2.5 V, where the signal starts to saturate and the signal traverses also through the positive part of the g_{m3}-curve, the negative area under g_{m3} gets completely cancelled by the positive part. Since this coherency is not clearly observable in Fig. 4-30 (d), Fig. 4-31 graphs the signal power of the 3rd harmonic in dBm contributed by the integrated area under the g_{m3}-curve for (a) with and (b) without weighting function $w_n(x)$. It is clearly visible in Fig. 4-31 (a) that for P_{IN} > 10…15 dBm the area under the g_{m3}-curve goes down to zero again. Resulting from the transformation of equation (4.21) from the time-domain to the voltage-domain in equation (4.22), the output signal components have to comprise the weighting function $w_n(x)$ for a correct mapping. Out of this reason has the outlying positive area always less impact on the cancellation than the nearby negative area under g_{m3}. As a rule of thumb it can be stated that with respect to ΔV_{GS0} the farther the positive/negative part is apart from the opposing negative/positive part of g_{m3}, the lower is the cancellation effect. Fig. 4-31 (b) illustrates exactly this fact that the output power of the 3rd harmonic exhibits no zero for large P_{IN} due to the presence of the weighting function $w_n(x)$. Thus, the 3rd harmonic exhibits the expected saturation behavior after starting with a slope of three for small input powers. Nevertheless, it has to be mentioned that the real saturation behavior is not fully modelled due to the Taylor series approximation.



(b) (d)

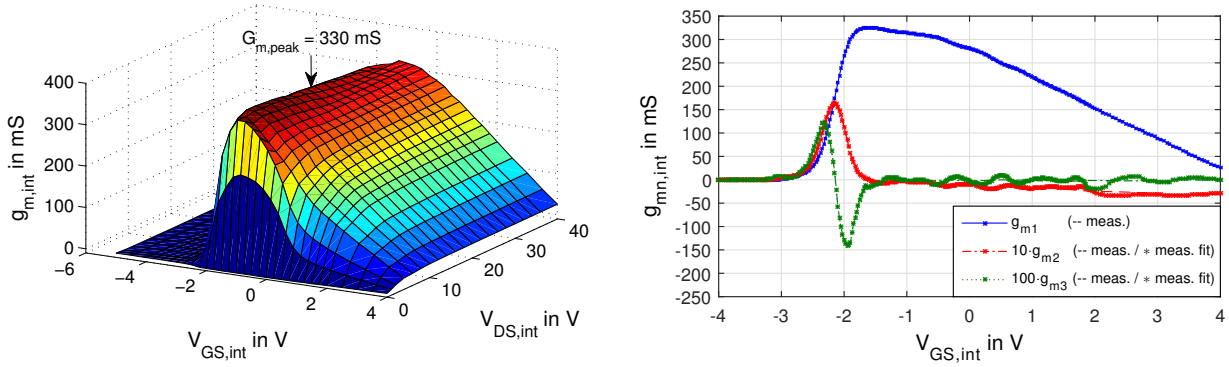
Fig. 4-31: $P_{OUT,3}$ in dBm over P_{IN} and V_{OS} for V_{GS0} = 0 V in (a) w/o and (b) with weighting function $w_3(x)$ of DSM for two ideal HEMTs

The observant reader might ask why the DSM concept for the idealized g_m-curve might give any linearity benefit, since the optimum linearity in terms of 3rd order cancellation for a simple CS-HEMT has been already found in class AB at V_{GS0} = -0.6 V from Fig. 4-11 (a). Moreover, class A operation gives additionally very low 2nd order distortion, leading to an optimum where the 2nd and 3rd order derivatives possess a common minimum (see Fig. 4-11 (b)). The major difference between the single CS-HEMT and the DSM is founded in the cancella-

tion of the 3rd order nonlinearity over larger input power ranges. Especially for non-symmetric g_{m3}-curves offers the DSM higher linearity, because choosing the bias point at the class AB small-signal sweet-spot of the g_{m3}-curve of a simple CS-HEMT does not yield full cancellation with increasing input signal swing anymore due to the asymmetry of g_{m3} around the bias point. By replacing the CS-HEMT by n parallelized HEMTs in DSM configuration, the linear range can be extended dependent on the asymmetry of the g_{m3}-curve and the number of stages. The higher the number of stages the larger becomes the linear input/output power range. In the following we will investigate the potential implementation of the DSM for small and large V_{OS} for GaN technology.

4.5.2 Evaluation of DSM for GaN

At the very beginning it is important to know the exact I-V-transfer characteristic of the GaN technology also for very large input signals before making a statement about the potential achievable linearity improvement of the DSM. The plotted g_m-curve in Fig. 4-32 (a) is extracted from isothermal large-signal measurements for different V_{GS} and V_{DS} up to the maximum DC power dissipation curve of 8 W/mm and is from there linearly extrapolated, whereas Fig. 4-32 (b) depicts one single linearly extrapolated $g_{m,iso}$-curve for V_{DS} = 30 V and its corresponding derivatives $g_{m2,iso}$ and $g_{m3,iso}$. Clearly visible is the maximum isothermal intrinsic large-signal g_m of around 330 mS/mm at V_{GS} = -1.8 V, which is due to the de-embedding of the extrinsic lead resistances R_G, R_D and R_S higher than the one from the LS-model, as e.g. shown in Fig. 4-9 (b). Fig. 4-32 (a) illustrates that as soon as the gate-source diode opens at around $V_{\mathrm{GS}} \approx 1$ V a more distinct saturation characteristic for values of $V_{\mathrm{DS}} \leq 5$ V than for larger V_{DS} values exists. The reason for the difference in saturation with increasing V_{DS} in HEMTs can be explained by the formation of a parasitic intrsinic MESFET, where the conduction channel is formed in the AlGaN layer between the gate and drain node. At the maximum measurable power dissipation point of the HEMT at a bias-point of roughly V_{GS} = 4 V and V_{DS} = 10 V, the $g_{m,iso}$-curve approaches an almost linear dependence for V_{GS} values larger than 1 V in Fig. 4-32 (a). Since $g_{m,iso}$ has to be close to zero when the maximum channel current density at a gate bias of $V_{\mathrm{GS}} \approx 4$ V is reached, linear extrapolation for V_{GS} values larger than 1 V for higher V_{DS} values is thus a good approximation, reflecting the real physical transfer characteristic of the GaN HEMT.



(a) (b)

Fig. 4-32: Extrapolated measured isothermal intrinsic g_m-transfer characteristic of an 8×125µm GaN HEMT (a) vs. V_{GS} and V_{DS} (courtesy: IAF) and (b) vs. V_{GS} for V_{DS} = 30 V including g_{m2} and g_{m3}

Based on the more symmetric $g_{m,iso}$ characteristic around class A bias for $V_{\mathrm{DS}} \leq 5$ V than for $V_{\mathrm{DS}} = 28$ V, as depicted in Fig. 4-32 (b), low V_{DS} operation would be advantageous in terms of an implementation of the DSM with large V_{OS}, as was sketched in Fig. 4-29 (b) for the ideal HEMT. Unfortunately, the most important limitation in applying large V_{OS} in the DSM in GaN technology is based on the maximum DC power dissipation of the first device. In order to exploit the 3rd order cancellation over the maximum input power range, the HEMT has to be biased far above class A. Besides, V_{DS} operation below 10 V yields reduced gain and limited output power. Accordingly, choosing large V_{OS} values in the DSM to improve the linearity is not a viable solution for GaN technology. The only remaining solution is thus to bias the different DSM-stages with small V_{OS}. Fig. 4-33 (b) shows the superposition of the g_{mn}-curves from two HEMTs for $V_{OS} = 0.4$ V, where $V_{\mathrm{GS},1}$ and $V_{\mathrm{GS},2}$ are selected in such a way that the 3rd order nonlinearity contributed by g_{m3} exhibits equal magnitude but opposite signs, as depicted in (a). Fig. 4-33 (c) and (d) show the corresponding dependency of the 2nd and 3rd order nonlinearity on different offset voltages V_{OS} and on different peak-to-peak input voltage swings ΔV_{IN}. From Fig. 4-33 (d) the optimum offset voltage V_{OS} for the 8×125µm GaN CS-HEMT in order to attain an almost input power independent 3rd order linearity is located at roughly $V_{OS} = 0.4\ldots0.5$ V. The 2nd order nonlinearity in contrast increases steadily with increasing ΔV_{IN}, but its input power dependency can be only minimized by choosing V_{OS} as large as possible, as already indicated for the ideal HEMT in Fig. 4-30 (a).

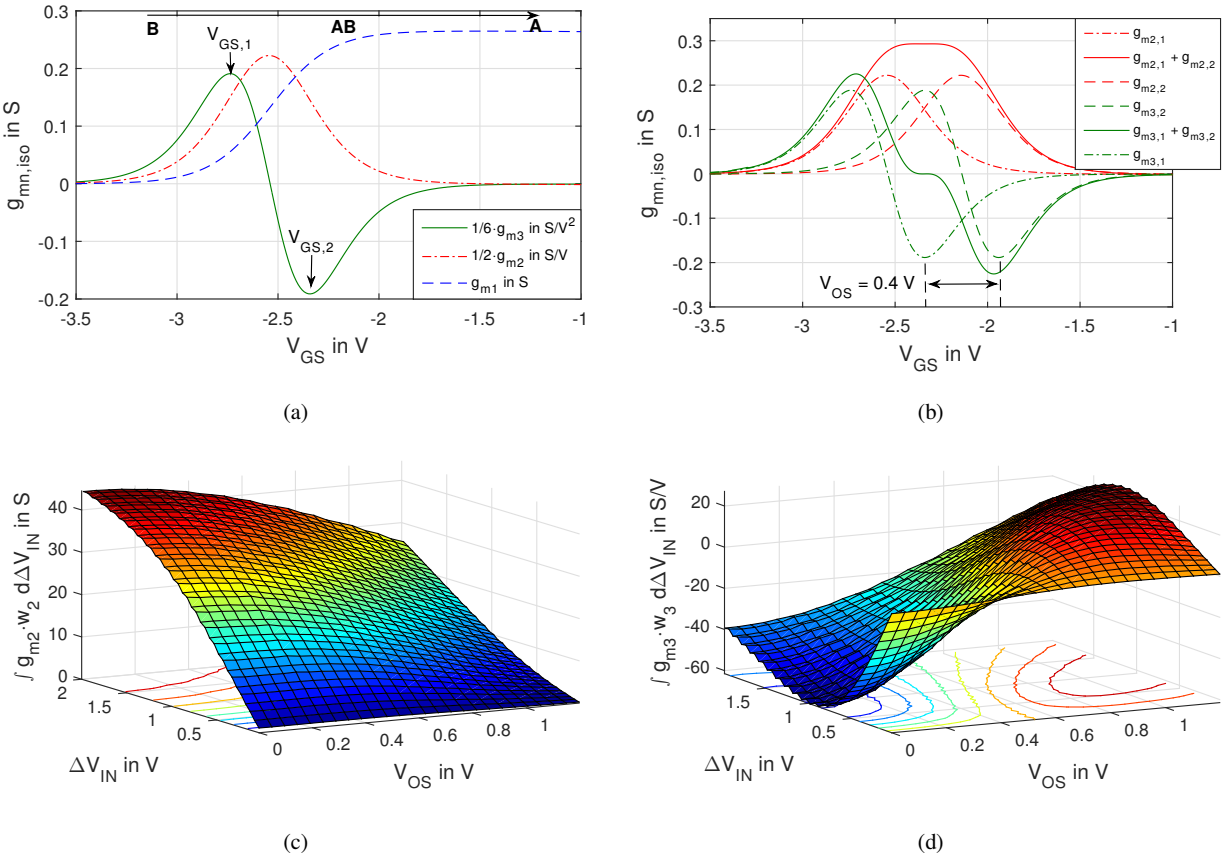


Fig. 4-33: (a) isothermal g_{mn}-curves, (b) sum of two isothermal g_{mn}-curves with $V_{OS} = 0.4$ V and integral of (c) g_{m2} and (d) g_{m3} over different input voltage swings ΔV_{IN} and different offset voltages V_{OS} for the DSM with two 8×125µm HEMTs at $V_{\mathrm{DS}} = 30$ V and $I_{\mathrm{DS}} = 200$ mA/mm

Overall, it can be concluded that the linearity improvement brought by the DSM is strongly confined by the GaN25 process. This is on the one hand the result of the sharp turn-on characteristic of these GaN HEMTs, as the resulting flat part from the summation of the two g_{m3}-curves in Fig. 4-33 (b) shows. To significantly increase the input dynamic range for 3rd nonlinearity cancellation, several HEMTs need to be connected in parallel, which raises circuit complexity drastically and thus brings up additional layout constraints. On the other hand, the 2nd order nonlinearity always dominates for small V_{OS}-values and cannot be cancelled out due to its positive sign, which makes this linearization concept inappropriate for maximizing the $SFDR$ in wideband PAs. Besides the limited improvement in $HD3$ and IMD performance over wide input DRs for GaN, one general advantage of applying the DSM-concept lies in the robustness against temperature variations and process deviations. All HEMTs are physically located close together on one chip and thus the drift over temperature is equal for each HEMT. Compared to a single CS-HEMT, where it is crucial to keep the bias point exactly at the g_{m3}-root in order to maintain cancellation, both DSM HEMTs are biased at g_{m3}-values with opposing signs, giving a more stable cancellation with temperature varying bias points.

Table 4-2: Advantages and disadvantages of the DSM

	Advantages	Disadvantages
Low V_{OS}	• Improved $HD3$ and $IMD3$ over a limited input power range	• $HD2$ and $IMD2$ are large and dominate nonlinearity • Self-biasing leads to linearity degradation for increasing P_{IN} • High number of parallel HEMTs necessary for large DRs • $\Longrightarrow$ limited BW due to high number of necessary interconnects in the layout
High V_{OS}	• Improved $HD2$, $HD3$ and $IMD2$, $IMD3$ over a large input power range • Only small number of parallel HEMTs necessary	• Bias above class A only possible in GaN for low V_{DS} operation due to thermal constraints • Non-symmetric g_m characteristic of GaN25 process around class A bias-point prohibits implementation of DSM with high V_{OS}
General	• Improved $HD3$ and $IMD3$ over a larger input power range • More temperature robust than CS-HEMT biased in deep class AB at g_{m3} sweet-spot	• reduced GBW-product due to o increased input capacitance based on parallelized devices o higher number of parallel RF-interconnects

One major drawback of the DSM silently neglected for 3rd order nonlinearity cancellation is founded in the reduced gain due to the operation in deep class AB at around I_{DS} = 20 to 50 mA/mm, far below the maximum g_m at I_{DS} = 100 mA/mm. Based on the high GBW-product requirements it is not justifiable to sacrifice so much gain for such a little improvement in 3rd order linearity. Moreover, a second difficulty emerges with respect to bandwidth from the parallelization of two HEMTs, which effectively doubles the input capacitance. Thus, the bandwidth additionally degrades proportional to the number of DSM-stages. Another major issue is self-biasing, which has been neglected so far. As can be seen from Fig. 4-33 (b) the bias voltages $V_{\mathrm{GS},1}$ and $V_{\mathrm{GS},2}$ and accordingly drain-source currents have to be accurately maintained in order to retain the optimum nonlinearity cancel-

lation. The increasing input power leads in reality to self-biasing, deteriorating linearity by the change in bias current. Optimum linearity can only be adhered by means of applying a constant bias current, which in turn limits the maximum available output power of the HEMT. The Table 4-2 summarizes the advantages and disadvantages, with the tendency that the disadvantages outweigh the advantages of the DSM in GaN25 technology. An on-chip hardware implementation was therefore skipped.

Remarks

One important aspect to mention is that the nonlinear capacitances, which have been up to now omitted in the DSM considerations in terms of simplicity, exhibit a different input power and bias point dependence than the nonlinear channel current, affecting optimum IMD performance (see Fig. 4-8). This leads to a smoother input power dependency of the 3rd order nonlinearity, giving less distinctive IMD sweet-spots, as also mentioned in [136]. Another important aspect to consider is the impact of the inductive source degeneration on the exact 3rd order nonlinear cancellation [148, 149]. Every source inductance introduces some feedback from I_{DS} to the input voltage V_{GS}, which becomes with increasing frequency stronger. A high inductive impedance hence feeds back the 2nd order nonlinearity of I_{DS} at $2\omega_{a,b}$ towards the input, where it adds up with the fundamental frequency $\omega_{a,b}$ of V_{GS}. Finally, this signal is mixed by g_{m2} towards the output, creating additional spectral components at $2\omega_a \pm \omega_b$ and $2\omega_b \pm \omega_a$. Thus, if the source inductance is sufficiently large there might be significant contribution to the $IMD3$ caused by the 2nd order nonlinearity from g_{m2}. The optimum bias setting for the 3rd order DSM cancellation might deviate from the optimum bias point settings found by the g_{m3}-curve and the $OIP3$ peaking is significantly reduced. There are different concepts to get rid of the additional $IMD3$ contribution from the 2nd order nonlinearity, as e.g. the introduction of an auxiliary path which provides a negative replica of the $IMD3$ component [150] or by additive multiple gated transistors in order to relax the 2nd order nonlinearity of C_{GS} [148, 151]. Unfortunately, all of these concepts are only effective for narrow-band designs and are thus not suitable for the application in multi-decade designs regarded in this thesis.

Another kind of DSM exists in bipolar technology and is accordingly named after the current transfer characteristic of bipolar differential pairs as “multi-tanh” principle. The multi-tanh principle has been first presented by B. Gilbert in 1998 [152] and later implemented by several analogue RFIC designers [153, 154, 155]. The nomenclature for “multi-tanh” is, as already stated, well-founded in the I-V-transfer-characteristic of bipolar differential pairs, which can be described by a hyperbolic tangent function. The basic idea of the multi-tanh principle is the superposition of the I-V-characterisitics of several differential pairs shifted solely in their pinch-off voltage in order to increase the operational dynamic range and thus linearity. Up to now, application in III-V semiconductor technology has so far not been reported to the author´s best knowledge. This might be based on the typically non-symmetric g_m characteristic around any bias point, as just presented for the DSM in section 4.5.2. Nevertheless, it might be worth looking at a modified “multi-tanh” principle for differential GaN PAs for processes exhibiting a more symmetric g_m-shape. If such “symmetric” processes were available even- as well as odd-order nonlinearities could be theoretically completely canceled.

4.5.3 Key Findings

The analysis of the DSM has revealed that the degree of linearity improvement is very dependent on the g_m-shape of the utilized process. The more symmetric the shape around the bias point, the higher the improvement in linearity and thus of the DR. Unfortunately for the applied 0.25µm GaN process, which is trimmed for class AB operation in terms of efficiency, the DSM proved due to its asymmetric g_m-shape not to be a viable candidate for improving linearity in wideband PAs. A large number of parallel GaN HEMTs would be required to widen the linear drive signal range, which in turn poses severe limitations in bandwidth by the necessary interconnects from a layout perspective. Another disadvantage of the DSM is the limitation in output power. In order to keep the bias-points fixed for optimum 3rd order nonlinearity cancellation, any form of self-biasing needs to be avoided by e.g. a proper gate-bias control or a fixed drain current, which again limits P_{sat}. Moreover, for low offset-voltages between the parallelized HEMTs, the HEMT needs to be operated in deep class AB which reduces the maximum available gain of the PA. Out of all these mentioned reasons, the DSM has not been considered as a suitable linearization method for broadband PAs in GaN and hence was not implemented within this work.

4.6 Nonlinear Diode Predistortion

4.6.1 Principle of Diode Predistortion

The basic principle of the diode predistortion concept is founded on the cancellation of the large-signal $C_{\mathrm{GS}}(V_{\mathrm{GS}})$ nonlinearity by adding a replica of $C_{\mathrm{GS}}(V_{\mathrm{GS}})$, which exhibits the exact opposite large-signal dependency. A HEMT in diode configuration features exactly this opposite characteristic of $C_{\mathrm{GS}}(V_{\mathrm{GS}})$, as long as it possesses the same size as the amplifying HEMT. Fig.4-34 sketches the basic idea of the predistortion concept by means of an antiparallel diode. By applying $2 \cdot V_{\mathrm{GS}}$ to the gate of the antiparallel diode, the voltage drop across the diode will be equal to - V_{GS}. As soon as the RF input signal becomes larger (smaller) the voltage over $C_{\mathrm{GS}}(V_{\mathrm{GS}})$ of the amplifying HEMT gets smaller (larger) and the voltage over $C_{\mathrm{SG}}(V_{\mathrm{GS}})$ of the antiparallel diode becomes larger (smaller). The result is an input power independent effective input capacitance C_{eff} with approximately two times the size of the average capacitance value of $C_{\mathrm{GS}}(V_{\mathrm{GS}})$. Fig. 4-35 (a) depicts the described C_{GS}-nonlinearity cancellation for a 8×125µm HEMT with an equally sized antiparallel diode. It can be seen that the summation of both C_{GS} gives an input voltage independent characteristic. What has been so far neglected is the $C_{\mathrm{GS}}(V_{\mathrm{DS}})$ dependence, which is negligible compared to the $C_{\mathrm{GS}}(V_{\mathrm{GS}})$ dependence in GaN HEMTs. Unfortunately, this is not valid for the feedback capacitance C_{GD}, since C_{GD} is strongly dependent on V_{DS}. The C_{GD}-value for the antiparallel diode with V_{DS} = 0 V is thus around three times larger than the C_{GD}-value for the HEMT at V_{DS} = 28 V, as Fig. 4-35 (b) shows. Furthermore, C_{GD} transforms due to the Miller effect [87] to an equivalent input capacitance, which increases by the amount of voltage gain A_V, as (4.54) below shows.

$$C_{\mathrm{GD},in} = C_{\mathrm{GD}}(1 - A_V) \tag{4.54}$$

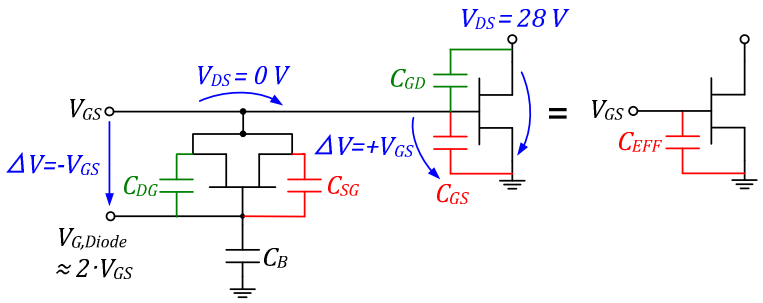


Fig.4-34: simplified diode predistortion concept for C_{GS}-nonlinearity cancellation

Assuming a typical g_m of 330 mS/mm for the GaN25 process and a load resistance of R_L = 50 Ω gives a 17.5 times larger C_{GD} seen at the input, according to the low frequency Miller approximation of $A_V = -g_m R_L$. This translates into an effective $C_{\mathrm{GD},in}$ being almost equal to 2 pF/mm and being now larger than C_{GS} with around 1.6 pF/mm. Additionally, not only the absolute DC C_{GD}-value rises but moreover also the nonlinear dependence of C_{GD} on V_{GS} will increase at the input. Fortunately under large-signal condition, A_V starts to decrease with increasing drive signal amplitude, reducing the Miller effect significantly. However, due to the input power dependence of $C_{\mathrm{GD},in}$, the nonlinearity arising from C_{GD} cannot be completely cancelled by the antiparallel diode as it is the case for the C_{GS}-nonlinearity. For simplicity reasons, the dependence of the Miller effect on the signal-swing and the Miller effect itself will be neglected for a better understanding.

Fig. 4-35 (c) and (d) show the resulting effective input capacitance C_{eff} and its corresponding 1st and 2nd order derivatives for a 8×125µm HEMT with shorted output and for the same HEMT with an upstream 8×125µm antiparallel diode. The overall C_{eff} of the predistorted HEMT in (d) is as expected doubled compared to C_{eff} of the single HEMT, but the higher order derivatives are smaller by a factor of 25. The focus is only put on the 1st and 2nd order derivative, because they are responsible for generating the most dominant 2nd and 3rd order nonlinearities, which are amplified to the output.

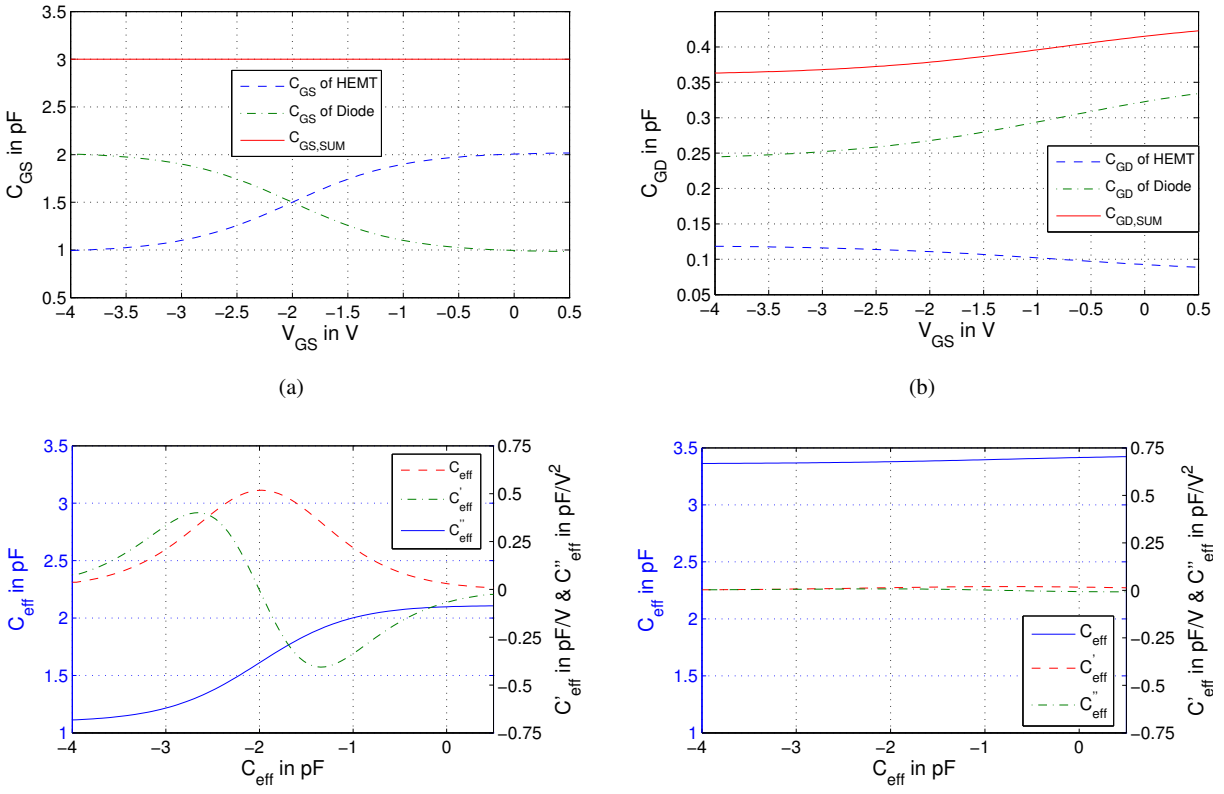


Fig. 4-35: Approximated (a) C_{GS} and (b) C_{GD} vs. V_{GS} dependence of a predistorted 8×125µm HEMT. C_{eff} and its 1st and 2nd order derivatives vs. V_{GS} of (c) the single 8×125µm HEMT and (d) the predistorted 8×125µm HEMT

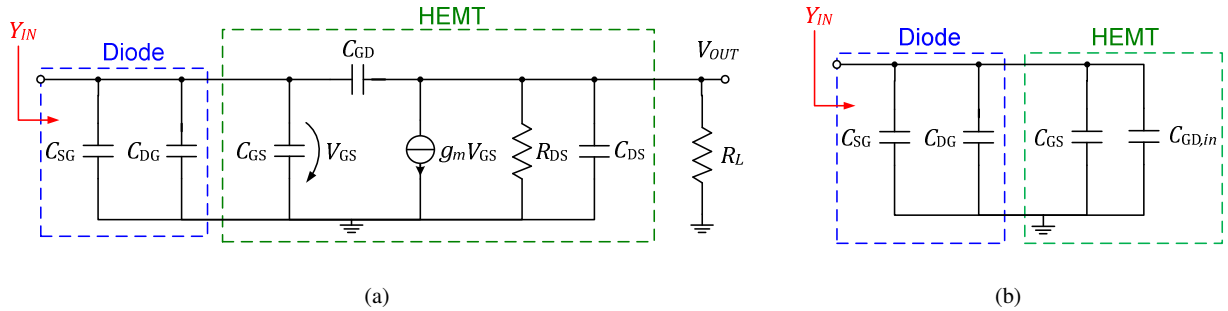


Fig. 4-36: (a) Equivalent small-signal circuit for diode predisortion plus HEMT and (b) equivalent Miller effect representation

In Fig. 4-35 (c) and (d) it has been so far implicitly presumed that C_{GS} and C_{GD} of the diode and the HEMT are simply in parallel, which is only true when the output in Fig. 4-36 below is shorted and thus no Miller effect is present. It is therewith meaningful to take a closer look at the actual frequency dependence of the effective input capacitance C_{eff}, as described by the equivalent small-signal model depicted in Fig. 4-36. The effective input capacitance of the antiparallel diode and the HEMT can be calculated by

$$C_{eff}(\omega) = \frac{Im\{Y_{IN}(\omega)\}}{\omega}, \tag{4.55}$$

which gives according to Fig. 4-36 (a) and (b) in combination with equation (4.54)

$$C_{eff}(\omega) = 2C_{\mathrm{GS}} + C_{\mathrm{GD}}\left(2 + \frac{g_m R_A}{\sqrt{1 + (\omega C_{\mathrm{DS}} R_A)^2}}\right), \tag{4.56}$$

R_A in (4.56) stands for the total output resistance, which is equal to $R_L || R_{\mathrm{DS}}$. The graph in Fig. 4-37 shows the frequency dependence of $C_{eff}(\omega)$ for different C_{DS} and R_{DS}. For the limits of $C_{\mathrm{DS}} = 0$ F, $R_{\mathrm{DS}} = \infty\ \Omega$ and $C_{\mathrm{DS}} = \infty$ F, $R_{\mathrm{DS}} = 0\ \Omega$ the maximum deviation of C_{eff} over frequency cannot be larger than $|A_V| \cdot C_{\mathrm{GD}}$. This can be also simply seen by either shorting the output in Fig. 4-36 (a), so that C_{eff} is equal to $2(C_{\mathrm{GS}} + C_{\mathrm{GD}}) =$ 3.42 pF (green dotted curve in Fig. 4-37) or by removing C_{DS} and R_{DS}, so that C_{eff} becomes equal to $2C_{\mathrm{GS}} + C_{\mathrm{GD}}(2 + g_m R_L) = 5.235$ pF (purple solid curve in Fig. 4-37).

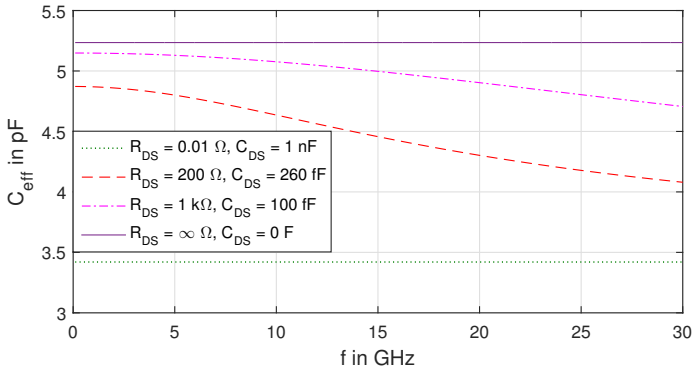
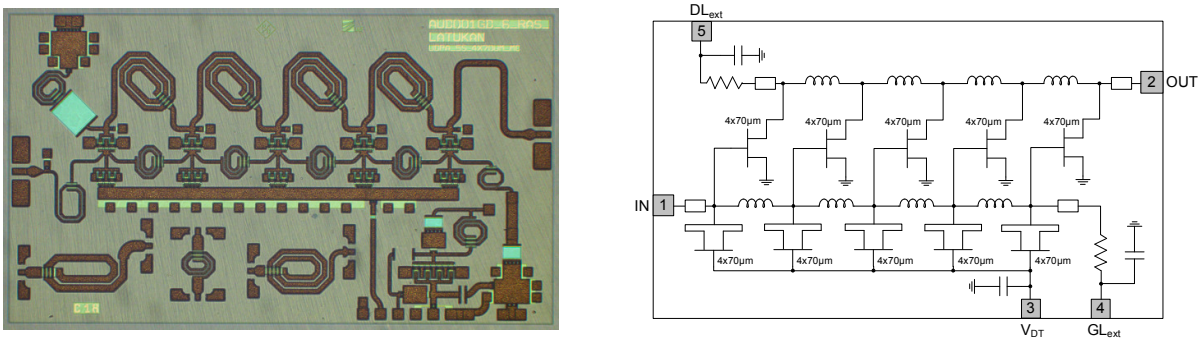


Fig. 4-37: Calculated C_{eff} of the 8×125µm predistorted HEMT for different R_{DS} and C_{DS} values

For the typical values of a 8×125µm HEMT ($R_{\mathrm{DS}} = 200\ \Omega$ and $C_{\mathrm{DS}} = 260$ fF), a strong dependence of C_{eff} for an output load of $R_L = 50\ \Omega$ becomes visible in Fig. 4-37. Responsible for this is the decreasing Miller effect with increasing frequency, which leads to a decaying contribution of the C_{GD}-nonlinearity compared to the C_{GS}-nonlinearity. Nevertheless, both nonlinearities increase with increasing frequency in general due to the increasing displament current through the capacitors, as already described in section 4.2.2.

4.6.2 DC – 6.5 GHz Highly Linear Low Noise TWA Design

For verification purposes of the antiparallel diode predistortion concept, which was theoretically presented in the preceding chapter 4.6.1, a DC - 6.5 GHz TWA was designed in the IAF GaN25 process. Goal of the design was to examine the effectiveness of the C_{GS}-nonlinearity compensation and to assess to which degree the overall linearity of a multi-decade distributed amplifier can be improved. Furthermore in chapter 5.2, the noise performance especially toward low frequencies without making use of capacitively coupled gates is investigated by means of the here presented linear low-noise TWA (L²NTWA) design. Therein, possible noise improvement measures will be discussed, which are not within the scope of this section.



(a) (b)

Fig. 4-38: (a) Photograph and (b) corresponding schematic of the DC-6.5 GHz highly linear low-noise TWA MMIC (“Latukan”)

Fig. 4-38 (a) shows the chip photograph of the final MMIC and (b) its corresponding schematic. The L²NTWA topology was chosen to be uniform with drain-dumping load to provide good output matching down to DC. The optimum number of stages resulted in $N = 5$ with each HEMT equally sized to 4×70µm, amounting to a total gate width of TGW = 1.4 mm. Parallel to each gate node of the five amplifying stages are HEMTs placed in diode configuration, which are of equal size but exhibit the opposite C_{GS} vs. V_{GS} characteristic. As already presented in chapter 4.6.1, due to V_{DS} = 0 V for the parallel diodes C_{GD} cannot be fully compensated. As Fig. 4-35 illustrates, C_{GD} of the diode is around two-times larger than the biased HEMT C_{GD} at V_{DS} = 28 V. Thus to find the optimum V_{SG} voltage for the parallel diodes in terms of linearity, some tuning is necessary dependent on the targeted bias point. Out of this reason, an external diode tuning voltge (V_{DT}) can be applied via the pin 3 in Fig. 4-38 (b) to control and tune the linearity of the L²NTWA. This generates on the one hand an important degree of freedom for the V_{DS} biasing, which can now be adjusted without deteriorating linearity and on the other hand allows for the compensation of process variations, which affect the large-signal dependency of the intrinsic capacitances (such as e.g. threshold drift). By adding the parallel diodes at the input only, the effective input capacitance of each stage is doubled and the cut-off frequency of the gate-line halved. This reduces the maximum achievable BW by a factor of two opposed to applying no predistortion. If no parallel diodes are used, the active gate periphery could be doubled, maintaining the same BW and simply operating the TWA farther in back-off condition. This might end up in a similar linearity performance as with the diode predistortion concept. Such a reference design was due to the limited time of this work not implemented, but could be designed for a more precise reference in a future work. The downside of an increased active device periphery comes at the cost of increased power consumption and even worse a higher NF due to the higher quiescent current. The latter parameter is besides linearity the most crucial design parameter for such a LNA-TWA design.

The output capacitance in contrast and thus the cut-off frequency of the drain-line is not affected by the parallel diode linearization concept, which generates twice the mismatch between input and output capacitance of the amplifying HEMTs. In order to equalize the phase delays on the gate- and drain-line, either a very large inductance in the drain-line is necessary or some additional capacitance at the output of each stage. The former approach has the drawback of a reduced SRF of the drain-line coils, which would increase the sensitivity of the drain-line design. The latter approach in contrast simplifies the design procedure significantly, because the coils in the drain-line can be designed equal for each stage, which reduces the effort of time consuming EM-simulations and enables the fine-tuning of the phase delays via adjustment of the MIM-capacitors instead of the coils. An important aspect to mention in terms of stability of the design is the RF-decoupling of the diode gates. Therefore, a large on-chip capacitor is placed directly at the gates of the diodes to provide a decent RF-ground. This might seem at first sight counter-intuitive, because the MIM-capacitor connects all of the diode gates together. But, as long as the RF-ground is "good" enough over the whole frequency range, the decoupling is suppressed to a great extent and the benefit in layout is the use of the capacitor top-metal for feeding the V_{DT} control voltage to all of the diode gates.

To realize operation down to DC, the L²NTWA has been assembled in a custom-made package and mounted onto a PCB for testing, including on-board gate and drain bias-tees. To obtain optimum thermal and electrical performance the chip was soldered with 25µm thin AuSn-preforms onto a Cu heat-spreader and integrated via flip-chip assembly into the test PCB, as Fig. 4-39 below shows. The former allows maximum heat transfer through the Cu-heatsink in the vertical direction and the latter minimum electrical loss due to the minimized signal path length in horizontal direction. In Fig. 4-39 additional SMD capacitors for the gate- and drain-line terminations are visible, which serve to extend the operational frequency down to 10 MHz.

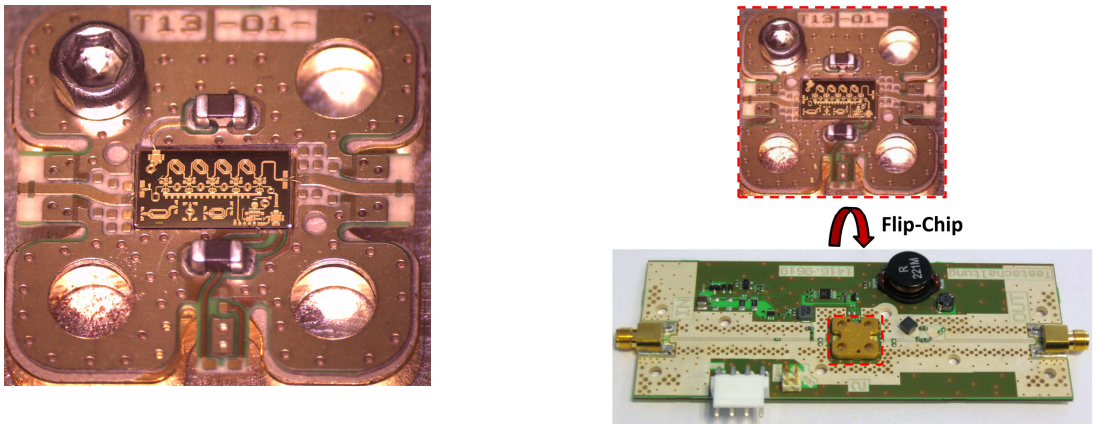


Fig. 4-39: (a) photograph of the packaged DC-6.5 GHz L²NTWA ("Latukan") including SMD capacitors for low frequency extensions on gate- and drain-line and (b) flip-chip assembly in RO4350 test board including on-board bias-tees

Fig. 4-40 shows the comparison between the simulated and measured S-parameters of the packaged L²NTWA. Clearly visible is the good correlation between simulation and measurement, whereas the measured results even outperform the simulation results. Over the BW of more than 2.5 decades from 10 MHz up to 6.5 GHz, the L²NTWA exhibits a small-signal gain of larger than 15 dB with an I/O-RL of better than 10 dB at the nominal bias point of V_{DS} = 28 V and I_{DS} = 200 mA/mm. The influence of the drain-termination off-chip SMD capacitor can be seen especially in the S_{22} below 1 GHz.

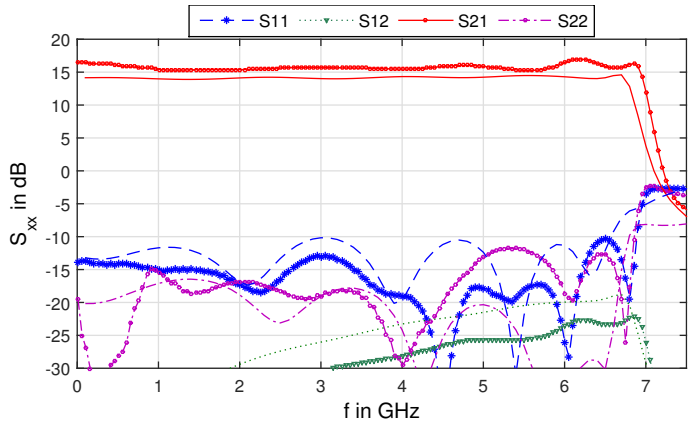
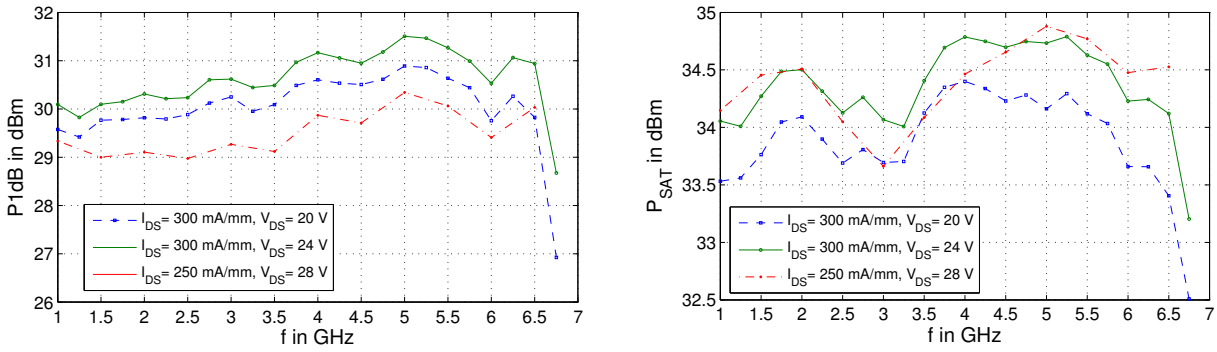


Fig. 4-40: Simulated & measured *S*-parameters of L²NTWA ("Latukan") from 10 MHz - 7.5 GHz in package at V_{DS} = 28 V and I_{DS} = 200 mA/mm



(a) (b)

Fig. 4-41: Measured (a) $P1dB$ and (b) P_{sat} of DC-6.5 GHz L²NTWA ("Latukan") in package for different V_{DS} and I_{DS} at $V_{DT} = 2.5 \cdot V_{GS}$

The large-signal 1-tone measurements shown in Fig. 4-41 reveal an outstanding P_{1dB} of larger 29 dBm and a corresponding P_{sat} of larger 33.5 dBm of the L²NTWA over the full band, giving an average output power density of larger than 1.8 W/mm. By trading V_{DS} for I_{DS}, under safe operation in the maximum DC power region of roughly 7 W/mm in terms of reliability, the optimum bias point can be determined to V_{DS} = 24 V and I_{DS} = 300 mA/mm, giving even a P_{1dB} > 30 dBm and a P_{sat} > 34 dBm. A further reduction in V_{DS} leads again to a decay in P_{1dB} and P_{sat} at a quiescent current of I_{DS} = 300 mA/mm.

Before moving on to the linearity measurements of the L²NTWA, the effective C_{GS}-nonlinearity of one-single stage will be reviewed in more detail. Fig. 4-42 shows the 1st, 2nd and 3rd order coefficients of $C_{GS}(V_{GS})$ for the combination of a 4×70µm common-source HEMT with a parallel 4×70µm HEMT in antiparallel diode configuration at a drain supply voltage of V_{DS} = 28 V. The curves from the large-signal model show that in (a) $C_{GS,2}$ can be approximated by an odd function around the operational bias pont of V_{GS} = -1.4 V for V_{DT} = -3.5 V. This results in an input power independent cancellation of the 2nd order nonlinearity, since the integral of $C_{GS,2}$ over V_{GS} becomes very small. On the contrary, the 3rd order nonlinearity shows an input dependent characteristic, where only above a certain input level the integral of $C_{GS,3}$ over V_{GS} becomes smaller again. Fig. 4-42 (b) depicts the flattest $C_{GS,1}$ vs. V_{GS} dependence around the operational bias point V_{GS} for V_{DT} = -4.9 V, constituting the smallest obtainable magnitudes for $C_{GS,2}$ and $C_{GS,3}$. The input power independent 2nd order cancellation is

not maintained anymore, based on the odd symmetry of $C_{GS,2}$ around the bias point. Now, the advantage lies in the simultaneous minimization of $C_{GS,2}$ and $C_{GS,3}$, leading to optimal $SFDR$ performance. From these linearity considerations at least two minima can thus be expected for the 2nd and 3rd order nonlinearities. Unfortunately, the location for the highest linearity cannot be predicted exactly from these simplified assumptions, since on the one hand nonlinearities arising from the channel are not considered here and on the other hand each stage sees varying 2nd and 3rd order harmonic load impedances over frequency instead of constant ones, as the load-line analysis from section 3.2.3 revealed.

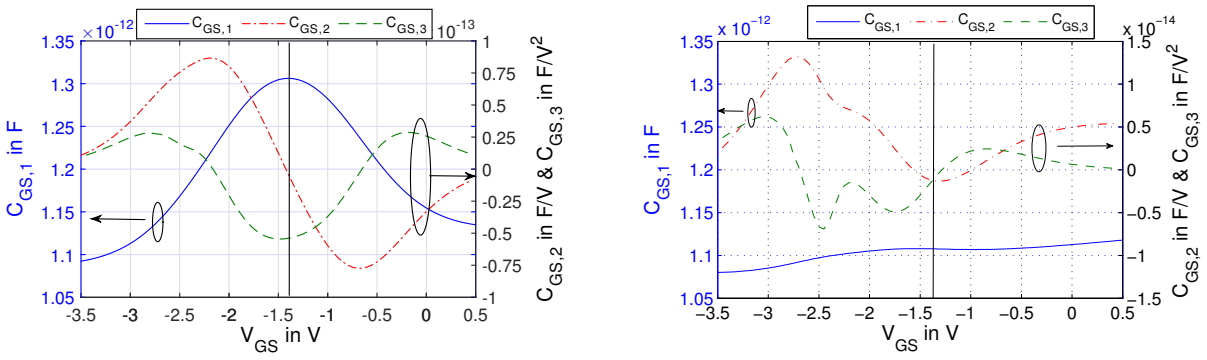


Fig. 4-42: C_{GS11}, C_{GS2} and C_{GS3} of a 4×70µm as diode plus a 4×70µm common-source HEMT vs. V_{GS} for (a) V_{DT} = -3.5 V and (b) V_{DT} = -4.9 V (@ V_{DS} = 28 V)

The linearity measurements, depicted in Fig. 4-43, underline the flat P_{1dB} characteristic over frequency. By sweeping the diode control voltage V_{DT}, the dependency of the HD and $OIP3$ on the amount of C_{GS}-nonlinearity cancellation is identified. From Fig. 4-43 (a) and (b) it becomes obvious that even-order distortions are traded-off for odd-order distortions and vice versa. The sweet-spots for the $HD2$ are located around $V_{DT} = 2.2 \cdot V_{GS}$ with a maximum $HD2$ of -37 dBc and around $V_{DT} = 2.6 \cdot V_{GS}$ with a maximum $HD2$ of -38 dBc at P_{OUT} = 25 dBm. In contrast, the $HD3$ exhibits its best characteristic exactly in between these two values at $V_{DT} = 2.4 \cdot V_{GS}$ with a maximum of -39 dBc at P_{OUT} = 25 dBm. For values of $V_{DT} < 2.0 \cdot V_{GS}$ and $V_{DT} > 2.8 \cdot V_{GS}$ the $HD3$ starts to improve again. As a consequence, the highest $SFDR$ for an output power of 25 dBm results for V_{DT}-values at which $HD2$ and $HD3$ are together minimized, which leads to values around $V_{DT} = 2.8 \cdot V_{GS}$. As expected from general theory, which was derived in section 4.1.2, a similar dependence for the $OIP3$ as for the $HD3$ can be seen in Fig. 4-44 (c) due to the same dependency of $HD3$ and $OIP3$ on 3rd order nonlinearities. Exactly at $V_{DT} = 2.4 \cdot V_{GS}$, where the sweet-spot of $HD3$ is located, a sharp local maximum in $OIP3$ can be observed. Since this local maximum is very sensistive to variations in V_{DT}, it is beneficial to set V_{DT} either to values below 2.0 or above 2.8. The corresponding $OIP3$ for these two values is plotted again in Fig. 4-44 for visibility reasons. For $V_{DT} = 2.0 \cdot V_{GS}$ a slightly more linear performance can be identified, but for both values an $OIP3$ of larger than 41 dBm up to 6.5 GHz is achieved. This is in accordance with Fig. 4-43 (c).

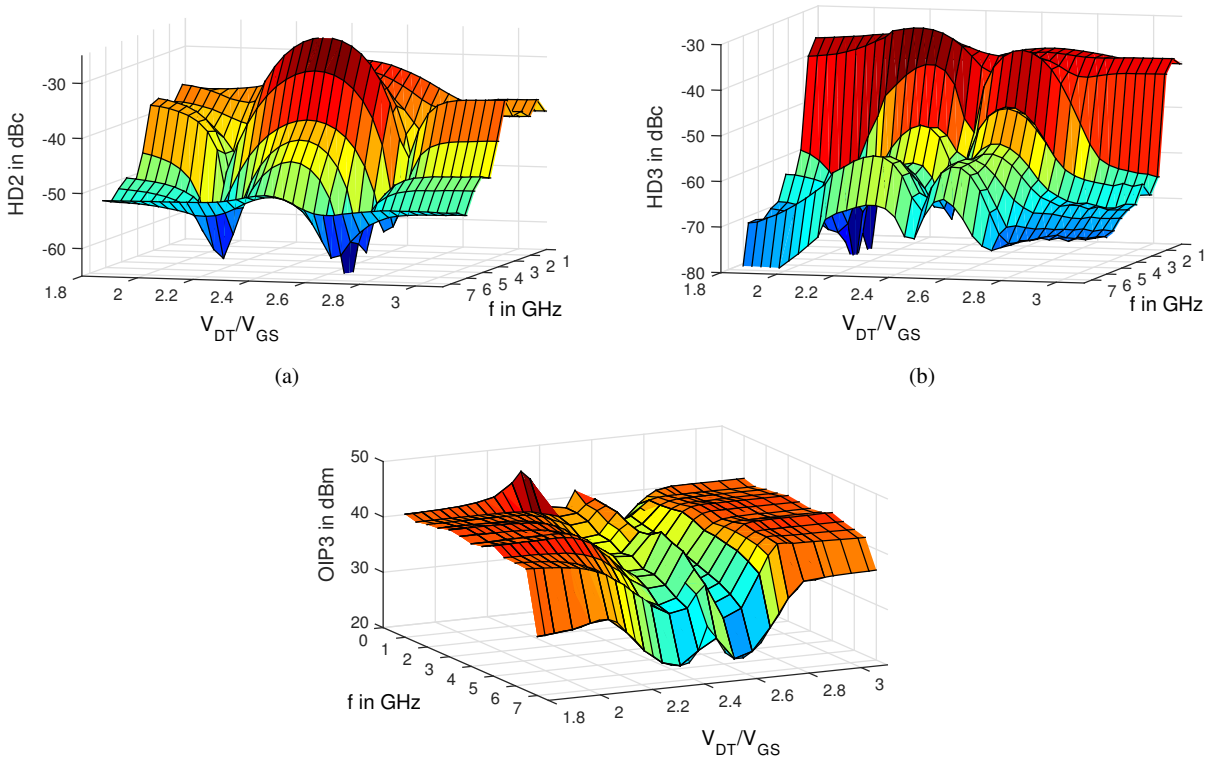


Fig. 4-43: Measured (a) $HD2$, (b) $HD3$ at P_{OUT} = 25 dBm and (c) $OIP3$ at Δf = 10 MHz vs. f and vs. V_{DT}/V_{GS} of L²NTWA ("Latukan") from 1-6.5 GHz in package (V_{DS} = 28 V and I_{DS} = 250 mA/mm)

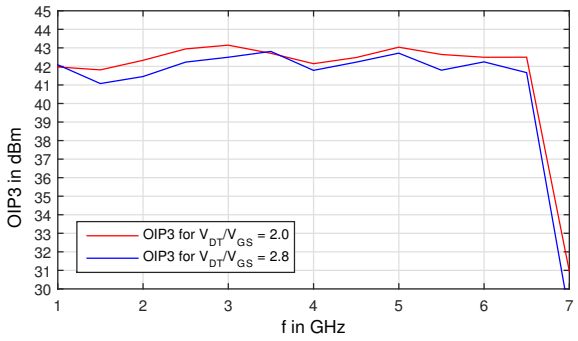


Fig. 4-44: Measured $OIP3$ with Δf = 10 MHz vs. f for V_{DT}/V_{GS} = 2.0 & 2.8 of the L²NTWA ("Latukan") from 1-6.5 GHz in package (V_{DS} = 28 V and I_{DS} = 250 mA/mm)

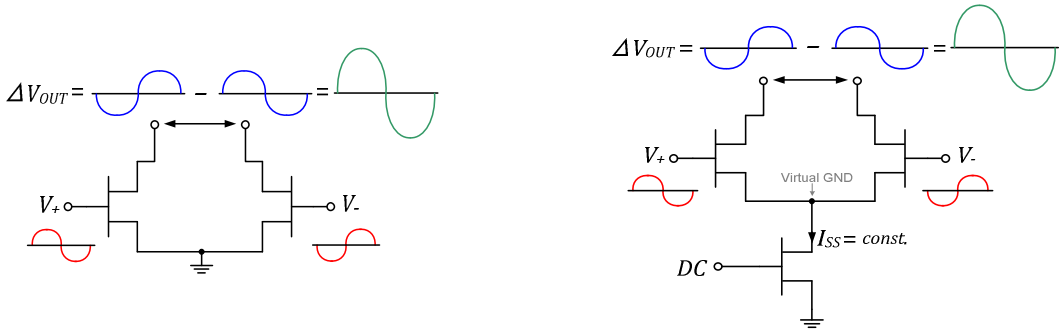
As a result it can be shortly summarized, that the compensation of the C_{GS}-nonlinearity has only little effect at low frequencies due to the small displacement current through C_{GS}, as was examined in chapter 4.2.2, but effectively improves linearity of the L²NTWA towards higher frequencies. Therefore the improvement in $HD2$ and $HD3$, which is in general only important up to 1/2 and 1/3 of the maximum frequency of operation, is recognizable but much lower than the improvement in $OIP3$ at high frequencies.

4.6.3 Key Findings

For the first time a diode predistortion concept has been applied in a multi-decade distributed amplifier design, operating from DC up to 6.5 GHz (L²NTWA). By means of the complementary dependency of the space-charge capacitance C_{GS} on V_{GS} in the antiparallel diode, the nonlinearity of C_{GS} can be compensated to a great extent over a large dynamic range. Measurements of the L²NTWA revealed that the harmonic distortion can be tuned very well b,y the externally accessible diode control voltage V_{DT}. At its optimum control voltage, a $SFDR$ at P_{OUT} = 25 dBm of greater than -38 dBc was measured. In terms of two-tone intermodulation performance, which is an important FoM especially for VSGs, an $OIP3$ of larger than 42 dBm could be achieved over the whole band up to 6.5 GHz. Despite its very promising high linearity, the diode predistortion concept suffers from one single limitation, namely the halved BW based on the doubled input capacitance. This is the main parameter, which has to be sacrificed but which most of the time can be traded-off in TWA designs due to their inherent high BW nature. Doubling of the active device periphery from TGW = 1.4 mm to 2.8 mm would end-up in the same BW limitation and would maybe give a similar linearity based on the higher back-off operation (at least at lower frequencies), but also doubles the power consumption and increases the channel noise in the HEMTs. With respect to all the mentioned aspects, the implementation of the diode predistortion concept in TWAs is a viable option for achieving high linearity, low-noise, low power consumption and still reasonable wide BWs at the same time.

4.7 Truly and Pseudo-Differential Linearization

Differential topologies are not widely applied in the "MMIC-world", because front-end parts of transceivers usually process single-ended signals. In SGs it could be advantageous to feed the differential signaling coming from the analog/digital synthesizer through to the output port in order to maintain signal integrity and also to be less prone to external noise and electromagnetic interference (EMI). Certainly, implementing differential circuits would boost the overall power consumption of the SG, but this is usually not a real matter of concern in stationary measurement equipment, which is plugged into a power socket. As a matter of fact, the integration of multi-decade broadband amplifiers with its spurious signal content lying inside the useable bandwidth poses a severe challenge for the overall SG´s linearity performance, because higher order harmonics fall into the useable bandwidth and hence cannot be filtered out easily. From the SG´s system point of view it is thus a meaningful approach to avoid generation of spurious harmonics at first place rather than implementing intricate adaptive filters on system level, which introduce additional attenuation at the output. In order to eliminate the most dominant 2nd order distortion and additionally all even order harmonics, differential topologies are well suited, which are well-known and extensively used in almost all analog CMOS-designs. The question which needs to be answered is, if all the typical characteristics of differential circuits in GaN technology can be fully exploited and if such GaN technology is really suited for the implementation of fully differential power amplifiers, which feature the expected improvement in linearity performance. This question will be answered in the following analysis after a short review of the theoretical principle of even-order harmonic cancellation in differential amplifiers.



(a) (b)

Fig. 4-45: Schematic of (a) pseudo-differential (PD) and (b) truly-differential (TD) amplifier

4.7.1 Even-Order Harmonic Cancellation

In principal there are two distinct differential concepts. The first concept is called pseudo-differential (PD) (see Fig. 4-45 (a)) and the second one truly-differential (TD) (see Fig. 4-45 (b)). For the PD-pair no shared ground node exists but instead each transistor is grounded independently. Accordingly, the current through the two transistors is also independent of each other. This is not the case for the TD-pair, where both transistors share the same current and thus a virtual ground node due to the opposing input signals is created. If the input signal is perfectly 180° out of phase at the input, no difference in performance for both concepts is to be expected and the even-order cancellation is ideally perfect. The following mathematical derivation will show the inherent even-order harmonic cancellation in differential pairs.

If the nonlinearities of the HEMTs are are weak enough to be approximated by a Taylor-series expansion up to n^{th}-order, the output signals can be expressed by the sum of their harmonic spectrum to

$$V_{OUT,+/-} = \sum_{k=1}^{n} a_k {V_{+/-}}^k, \tag{4.57}$$

where a_k represents the coefficients from the Taylor-series expansion, $V_{+/-}$ the two single-ended input voltages, $V_{OUT,+/-}$ the single-ended output voltages and n the maximum considered order of nonlinearity. Computation of the differential output signal accordingly gives

$$\Delta V_{OUT} = V_{OUT,+} - V_{OUT,-}. \tag{4.58}$$

When V_+ is equal to $-V_-$, the differential output signals for the odd- and even-order harmonics result in

$$\begin{aligned} \Delta V_{OUT} &= \sum_{k=1}^{n/2-1} a_{2k-1} {V_+}^{2k-1} - \sum_{k=1}^{n/2-1} a_{2k-1}(-V_+)^{2k-1} = 2 \cdot {V_+}^n && \text{for odd } n \\ \Delta V_{OUT} &= \sum_{k=1}^{n/2} a_{2k} {V_+}^{2k} - \sum_{k=1}^{n/2} a_{2k}(-V_+)^{2k} = 0 && \text{for even } n \end{aligned} \tag{4.59}$$

As has been stated, equation (4.59) shows that all even-order harmonics are cancelled out and only the odd-order signal components remain at the output. So far, there is no difference in even-order harmonic cancellation between the PD- and TD-pair as long as the input signals exhibit a phase difference of exactly 180° and are of equal amplitude.

4.7.2 Susceptibility to Phase & Amplitude Imbalances and Process Variations

In reality, a differential input signal with exactly 180° phase difference and of equal voltage amplitudes cannot be provided perfectly over large bandwidths. Usually some kind of either passive or active circuitry, which performs a single-ended to differential signal conversion is operated upstream to the differential circuitry. For such circuits it is not uncommon that a phase imbalance ($\Delta\phi$) of up to 10° together with a a few tens of dB of amplitude imbalance (Δa) is present in their output signal. On top, process variations within one cell lead to mismatches between the two transistors (m_T) in the differential pair and thus to an asymmetrical operation. An impact of these three types of imbalances on linearity is hence always present in reality, which makes it important to scrutinize the impact of each of these effects on linearity separately within the next sub-sections for the PD-pair and the TD-pair.

Phase Imbalance

From Fig. 4-45 it can be immediately seen that the PD-pair in (a) has a seperate physical connection to ground for each transistor and does not share a common virtual ground node, as it is the case in the TD-pair in (b). Based on this fact that the $CMRR$, which is defined here as S_{c2c1}/S_{d2d1}, is equal to one for the PD-pair (see Fig. 4-45 (a)), all CM-components will be present at each of the two output ports of the PD-pair. Since all even-order harmonics exhibit a positive phase at each of the two outputs, all even-order harmonics can be also considered as a CM excitation, as already shown in (4.59) in the preceding section. Therefore, by simply taking the difference of the two output signals, all even-order harmonics will hence exactly cancel out for $\Delta\phi$ = 0°. As soon as $\Delta\phi$ deviates from zero, the differential output signal of the PD-pair will contain some sort of even-order spectral componnoents a t its output. Assuming that the differential pair comprises two nonlinear transistors possessing nonlinearities up to the 3rd order and that it is driven by the two input signals of the form $V_+ = A \cdot sin(\omega t + \Delta\phi)$ and $V_- = -A \cdot sin(\omega t)$, the differential output voltage becomes equal to

$$\begin{aligned} \Delta V_{OUT}(\Delta\phi, \omega t) &= k_1 A \cdot [sin(\omega t + \Delta\phi) + sin(\omega t)] + k_2 A^2 \cdot [sin^2(\omega t + \Delta\phi) - sin^2(\omega t)] \\ &\quad + k_3 A^3 \cdot [sin^3(\omega t + \Delta\phi) + sin^3(\omega t)], \end{aligned} \tag{4.60}$$

where k_n expresses the voltage gain ($g_{m,n}R_L$) of the n^{th}-order nonlinear component. Separation of (4.58) into its nonlinear terms and making use of equivalent trigonometric functions leads to the following voltage sectrum in (4.61) of the differential output voltage.

$$\begin{aligned} H_1(\Delta\phi, \omega t) &= \left(2k_1 A + \frac{3}{2}k_3 A^3\right) \cdot cos\left(\frac{\Delta\phi}{2}\right) \cdot sin\left(\omega t + \frac{\Delta\phi}{2}\right) \\ H_2(\Delta\phi, \omega t) &= k_2 A^2 \cdot sin\left(\frac{\Delta\phi}{2}\right) \cdot sin(2\omega t + \Delta\phi) \\ H_3(\Delta\phi, \omega t) &= -\frac{k_3}{2} A^3 \cdot cos\left(\frac{3\Delta\phi}{2}\right) \cdot sin\left(3\omega t + \frac{3\Delta\phi}{2}\right) \end{aligned} \tag{4.61}$$

Once again, equation (4.61) shows that for $\Delta\phi$ = 0° the second harmonic H_2 cancels completely out. The third harmonic H_3 in contrast vanishes only for an input phase imbalance of $\Delta\phi = \pi/3$ and the fundamental tone H_1 becomes fully suppressed for $\Delta\phi = \pi$ (see also Fig. 4-48 (a)). Additionally, the 3rd order nonlinearity contributes to the fundamental tone, which is comparably small as long as the PD-pair is operated at high back-off ($A \ll 1$).

For the TD-pair the situation is unfortunately a bit more complex and cannot be expressed by simple trigonometric functions in such a clearly laid out manner. Due to the common TCS, each transistor cannot be regarded independently from each other but rather its output signal is dependent on the operation of its counterpart. In a first step perfect circuit symmetry and $\Delta\phi$ = 0° is assumed. For this case all even-order nonlinearities of the transistor lead due to their always positive phase to in-phase even-order harmonics at the two drain terminals. Since these even-order in-phase currents would appear at the virtual ground node of the TCS in form of a CM-distortion, the ideal TCS starts to adjust to the exact negative voltage replica in order to keep the imprinted tail-current constant.

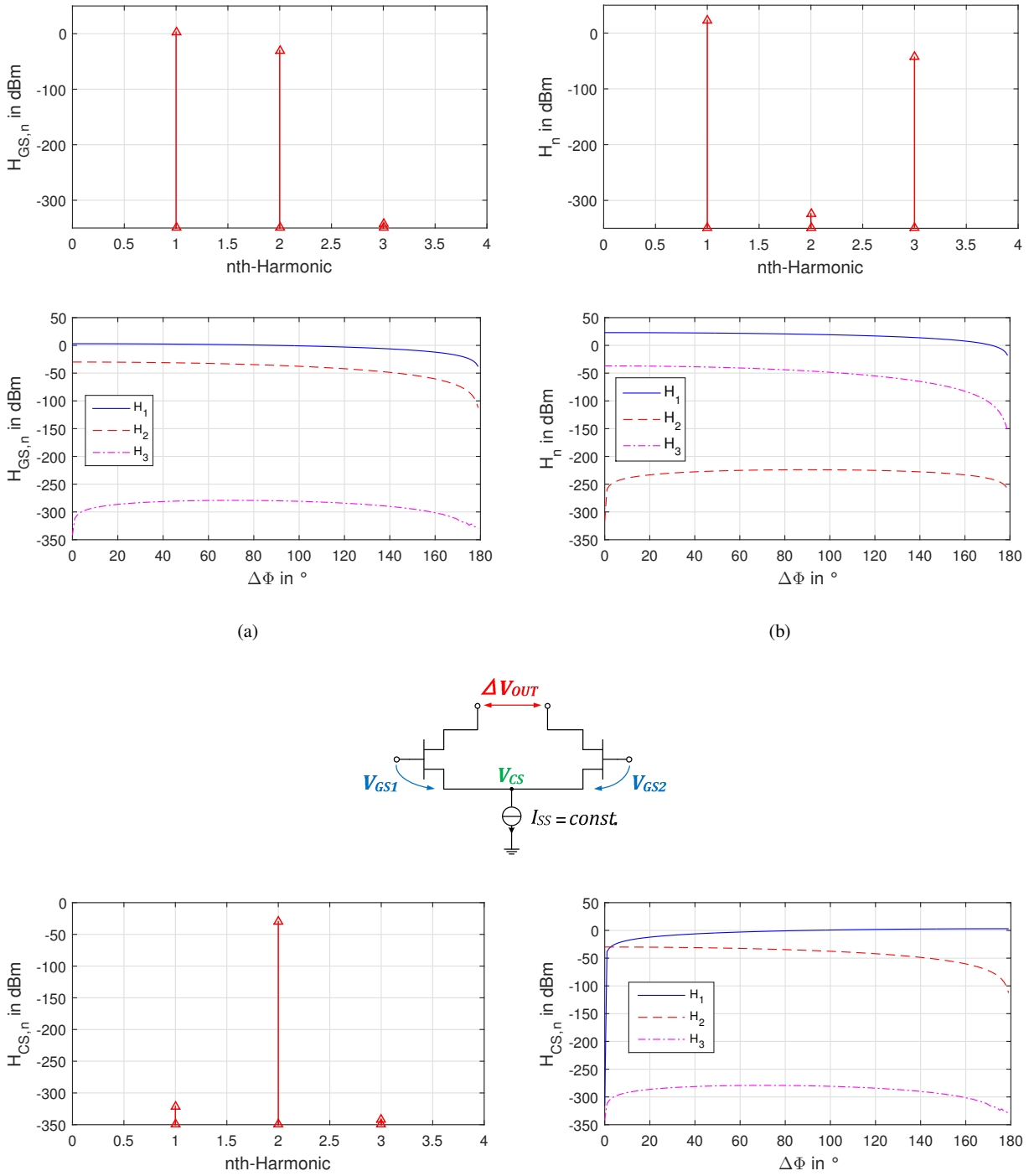


Fig. 4-46: Simulated output spectral components at $\Delta\phi = 0°$ and corresponding dependence on $\Delta\phi$ of (a) V_{GS}, (b) ΔV_{OUT} and (c) V_{CS} of an ideal TD-pair comprising 2rd order nonlinear transistors with coefficients $g_{m1} = 0.1$ S, $g_{m2} = 0.01$ S/V ($g_{m3} = 0$ S/V²) and an ideal TCS.

This voltage is fed back via the source node of the transistors to the input, which therewith completely cancels out the corresponding even-order nonlinearity of the transistor at its output. Due to this forced "even-order feed-

back" arising from the TCS, no even-order harmonics are present at the single-ended drain terminals and hence in the differential output signal, as Fig. 4-46 (b) illustrates.

At first sight, it seems to be surprising that a 3rd harmonic (H_3) component is present in the differential output signal even when the transistor exhbitis no 3rd order nonlinearity ($g_{m3} = 0$ S/V²). The reason for this is found to be rooted in the mixing of the second harmonic voltage component in (c), which is present at the TCS node and the fundamental input voltage by the 2nd order nonlinearity of the transistor. This leads to a 3rd harmonic component in the differential output signal, as depicted in Fig. 4-46 (b). If the transistor additionally possesses a 3rd order nonlinearity ($g_{m3} \neq 0$ S/V^2) the resulting magnitude of H_3 depends on the sign and absolute magnitude of the 3rd order coefficient, as Fig. 4-47 illustrates. For a positive 3rd order coefficient, the portion of H_3 contributed by the 3rd order nonlinearity might get cancelled partly by the portion coming from the "even-order feedback" mixing term, whereas a negative 3rd order coefficient always increases H_3. The former is only true as long as the resulting magnitude of the sum of the 3rd order coefficient and the "even-order feedback" mixing term is not larger than the "even-order feedback" mixing term itself. In principle the TD-pair can be thus operated in a H_3 sweet-spot by means of adjusting the bias-point to the proper g_{m3}-value, increasing the $SFDR$ of the TD-pair significantly. (Note: all other nonlinear sources, such as the capacitors in the transistor which might counteract the H_3 cancellation are neglected herein).

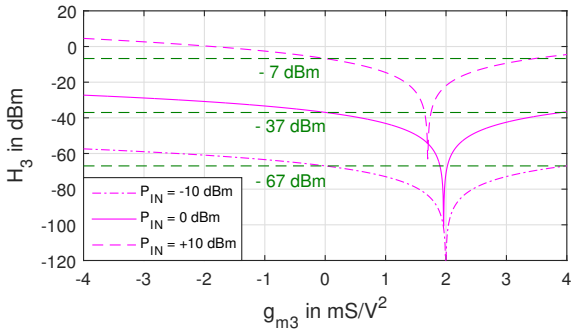


Fig. 4-47: Simulated 3rd harmonic (H_3) vs. g_{m3} at P_{IN} = -10, 0…10 dBm and $\Delta\phi = 0$ of an ideal TD-pair with ideal TCS (g_{m1} = 0.1 S, g_{m2} = 0.01 S/V)

As soon as $\Delta\phi$ becomes larger than zero, the odd-order harmonics start to appear at the TCS node, such that the voltage-swing of H_1 and H_3 at the TCS increases with increasing $\Delta\phi$, as V_{CS} in Fig. 4-46 (c) reveals. The maximum of H_3 is reached at $\Delta\phi = \pi/3$ due to the three times faster phase rotation whereas H_1 exhibits its maximum at $\Delta\phi = \pi$, which corresponds at the input to a full CM-excitation. The latter has the effect that the fundamental of V_{GS} in (a) decreases due to the increasing feedback of V_{CS} in (c) and so does H_1 of ΔV_{OUT} in (b). H_2 of ΔV_{OUT} increases only marginally with increasing $\Delta\phi$ due to the fact that the increasing H_3 of V_{CS} mixes down with the fundamental tone H_1 at V_{GS} to H_2 in ΔV_{OUT}, possessing its maximum at $\Delta\phi = \pi/2$. As the result of being a mixing product, H_3 of ΔV_{OUT} decays steadly with increasing $\Delta\phi$ due to the decreasing H_2 and H_1 components in V_{GS}.

A comparison between the linearity of the PD-pair and TD-pair is shown in Fig. 4-48, incorporating now also the presence of the 3rd order nonlinearity g_{m3} (k_3). For the PD-pair in (a), a small phase imbalance at the input results already in a fast increase of H_2 due to the independent phase rotation of H_2 at the two output terminals. Same accounts for H_3 except now with a three-times higher phase rotation, giving a sweet-spot at $\Delta\phi = \pi/3$. For the TD-pair in contrast, as can be deduced from Fig. 4-48 (b), the second harmonic H_2 of the TD-pair

is not as sensitive to phase imbalances as for the PD-pair. In a similar fashion as the fundamental tone H_1 becomes supressed toward $\Delta\phi = \pi$ in the TD-pair, also H_3 is more and more attenuated for increasing phase imbalances, exhibiting no H_3 sweet-spot as the PD-pair due to the common feedback via the constant TCS.

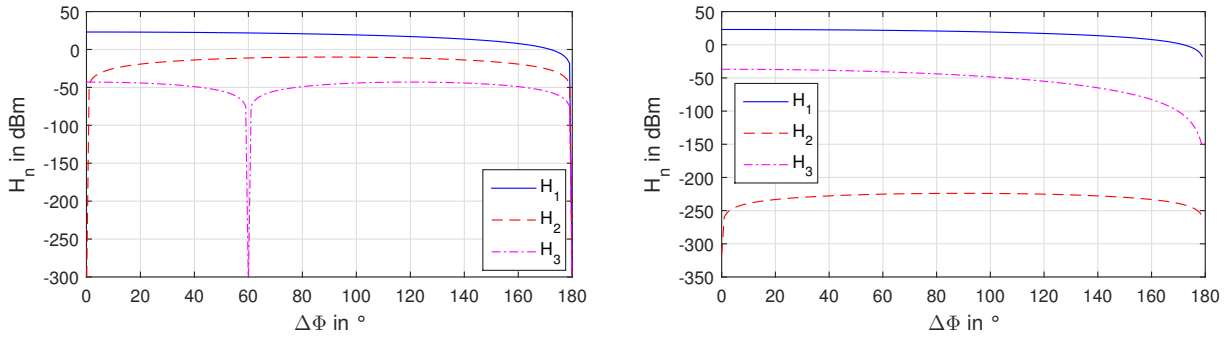


Fig. 4-48: Simulated/Computed spectral output components (H_1, H_2, H_3) in dBm vs. $\Delta\phi$ of an ideal (a) PD-pair and (b) TD-pair with ideal TCS for P_{IN} = 0 dBm (g_{m1} = 0.1 S, g_{m2} = 0.01 S/V, g_{m3} = 0.001 S/V²)

To end up with a realistic statement about which of the two topologies is the more robust in terms of linearity and thus more suited for an implementation in GaN technology, the linearity dependent on the phase imbalance is assessed by means of the GaN25 IAF models. The simulated linearity data in Fig. 4-49 shows for an unmatched PD-pair with two 6×50µm HEMTs (blue dot-dashed curve) that the $HD2$ is e.g. at $\Delta\phi$ = 10° more than 20 dB degraded compared to the TD-pair with ideal TCS (red solid curve), which is in good agreement with the preceding theoretical analysis. If for the TD-pair also a real TCS-HEMT of size 6×50µm with a finite output impedance is assumed, the $HD2$ still improves by 10 dB, which lies between the performance of a PD-pair and TD-pair with ideal TCS. The odd-order nonlinearity, represented in form of the $HD3$ in Fig. 4-49 (b), is only slightly dependent on the phase imbalance $\Delta\phi$, as already expected from the analysis. Nevertheless, a slightly higher suppression of the third harmonic in the TD-pair opposed to the PD-pair can be seen, which is deemed to be the result of the H_3 cancellation by the "even-order feedback" mixing term and the 3rd order nonlinearity of the HEMT.

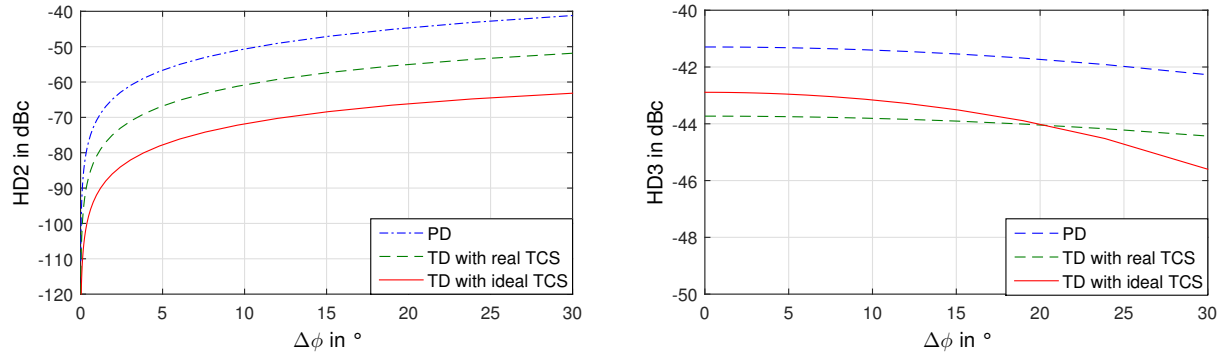


Fig. 4-49: Simulated (a) $HD2$ vs. $\Delta\phi$ and (b) $HD3$ vs. $\Delta\phi$ at P_{out}= 20 dBm for f = 6 GHz of an unmatched 6×50µm PD-pair, 6×50µm TD-pair with 6×50µm TCS and a 6×50µm TD-pair with ideal current source

Amplitude Imbalance

Similar to the case of phase imbalances, amplitude imbalances of magnitude Δa between the two input signals lead also to a difference in output linearity. The two sinusoidal input signals incorporating the amplitude mismatch can expressed by $V_+ = (A + a/2) \cdot sin(\omega t)$ and $V_- = -(A - \Delta a/2) \cdot sin(\omega t)$, giving a differential output voltage for the PD-pair equal to

$$\Delta V_{OUT}(\Delta a, \omega t) = 2k_1 A \cdot sin(\omega t) + 2k_2 \Delta a A \cdot sin^2(\omega t) + k_3 \left(2A^3 + \frac{3}{2}\Delta a^2 A\right) \cdot sin^3(\omega t). \tag{4.62}$$

Again, by making use of trigonometric relationships, the fundamental (H_1), 2nd harmonic (H_2) and 3rd harmonic (H_3) components of the differential output voltage result in

$$\begin{aligned} H_1(\Delta a, \omega t) &= \left[2k_1 A + k_3 \left(\frac{3}{2}A^3 + \frac{9}{8}\Delta a^2 A\right)\right] \cdot sin(\omega t) \\ H_2(\Delta a, \omega t) &= -k_2 \Delta a A \cdot cos(2\omega t) \\ H_3(\Delta a, \omega t) &= -k_3 \left(\frac{1}{2}A^3 + \frac{3}{8}\Delta a^2 A\right) \cdot sin(3\omega t). \end{aligned} \tag{4.63}$$

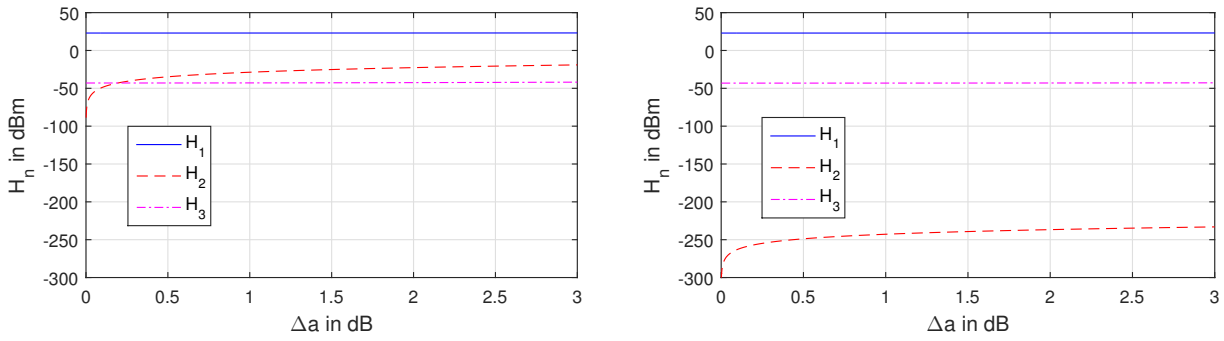
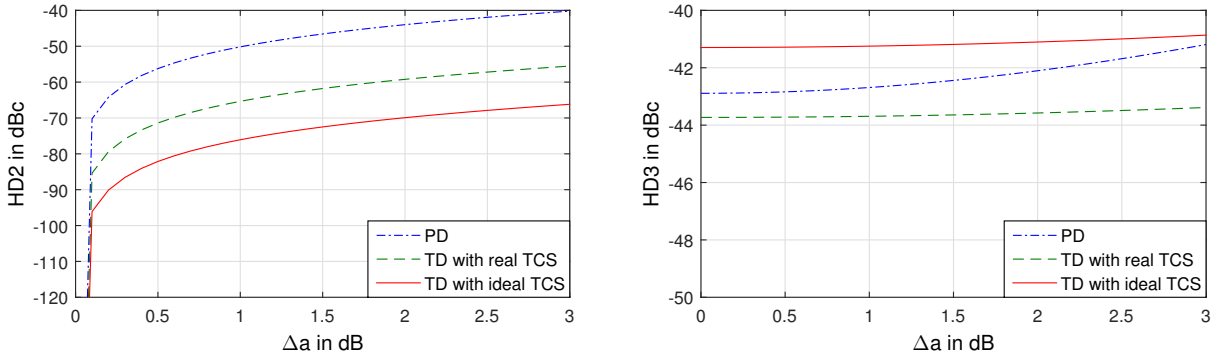


Fig. 4-50: Simulated/Computed spectral output components (H_1, H_2, H_3) in dBm vs. Δa in dB of an ideal (a) PD-pair and (b) TD-pair with ideal TCS for P_{IN} = 0 dBm (g_{m1} = 0.1 S, g_{m2} = 0.01 S/V, g_{m3} = 0.001 S/V²)

Equation (4.63) shows, that the differential output swing of the fundamental tone H_1 is only to a minor extent dependent on amplitude mismatches at the input, whereby the dependence is only caused by the 3rd order nonlinearity and which can be neglected for $\Delta a \ll 1$. The second harmonic H_2 in contrast increases linearly with Δa starting at zero, whereas the third harmonic H_3 increases with $3/8 \cdot \Delta a^2$ under constant input drive. As long as the condition $\Delta a \ll 1$ is satisfied, H_3 is only dependent on the input voltage amplitude A and the increase of H_3 with Δa is only marginally. Since the linearity dependence of the TD-pair on amplitude imbalances exhibits a very similar characteristic in terms of negative feedback and nonlinear mixing processes, as already described for the case of phase imbalances in the preceding subsection (Fig. 4-46), the just gained knowledge of

the harmonic dependencies can be transferred to the case of amplitude imbalances. As depicted in Fig. 4-50, the 2nd harmonic (H_2) of the TD-pair in (b) is only slightly dependent on Δa and as such not as sensitive to amplitude imbalances as it is the case for the PD-pair in (a). The odd-order harmonics H_1 and H_3 in contrast do not show any relevant dependence on Δa within the 3dB range. Nevertheless, H_3 at the output of the TD-pair is again dependent on the sign and magnitude of the nonlinear 3rd order coefficient (g_{m3}), as it is the case for phase imbalances (see Fig. 4-47).

In order to make a realistic assessment about the resulting linearity for GaN, the linearity simulations with the GaN25 IAF models in Fig. 4-51 reveal that for an unmatched PD-pair with two 6×50µm HEMTs (blue dot-dashed curve) the $HD2$ is e.g. at Δa = 1 dB more than 25 dB degraded compared to the TD-pair with ideal TCS (red solid curve). Replacement of the ideal TCS by a real TCS-HEMT of size 6×50µm yields still an impvoement in $HD2$ of larger than 15 dB, which again lies in the middle of the $HD2$ of the PD-pair and TD-pair with ideal TCS. The odd-order nonlinearity, represented in form of the $HD3$ in Fig. 4-51 (b), is almost independent on the amplitude imbalance Δa, as already derived in the foregoing theoretical analysis.



(a) (b)

Fig. 4-51: Simulated (a) $HD2$ vs. Δa and (b) $HD3$ vs. Δa at P_{out}= 20 dBm for f = 6 GHz of an unmatched 6×50µm PD-pair, 6×50µm TD-pair with 6×50µm TCS and a 6×50µm TD-pair with ideal current source

Process Variations

Besides the superior performance in terms of input signal imbalances of the TD-pair compared to the PD-pair, actual processing tolerances need to be also taken into account. Both HEMTs in the differential stage are in reality slightly mismatched due to process variations. This translates for the PD-pair into a similar linearity dependence as already computed for the amplitude imbalances. Linear scaling of the nonlinear voltage gain coefficients k_n of the two independent output voltages by a gain-mismatch factor $(1 \pm m_T/2)$ yields a differential output voltage up to 3rd order nonlinearity of

$$\Delta V_{OUT}(m_T, \omega t) = 2k_1 A \cdot sin(\omega t) - m_T k_2 A^2 \cdot sin^2(\omega t) + 2k_3 A^3 \cdot sin^3(\omega t). \quad (4.64)$$

By making once again use of trigonometric relationships, the fundamental (H_1), 2nd harmonic (H_2) and 3rd harmonic (H_3) components of the differential output voltage result in

$$H_1(m_T,\omega t) = \left[2k_1A + \frac{3}{2}k_3A^3\right]\cdot sin(\omega t)$$
$$H_2(m_T,\omega t) = \frac{m_T}{2}k_2A^2\cdot cos(2\omega t) \tag{4.65}$$
$$H_3(m_T,\omega t) = -\frac{1}{2}k_3A^3\cdot sin(3\omega t).$$

As equation (4.64) reveals, the odd-order harmonics H_1 and H_3 are not affected by any mismatch between the two transistors, whereas the even-order harmonic H_2 increases proportional to $m_T/2$. For the TD-pair in contrast, the feedback to the input by the TCS gives again rise to a 3rd harmonic (H_3) at the output due to the mixing process, even if no 3rd order nonlinearity in the transistors is present. Also regarding the dependence of H_1 and H_3 on m_T, the TD-pair exhibits a "shifted" virtual ground node due to the device mismatch, which leads to unequal currents in the two branches and similar to the case of phase imbalances to the presence of odd-order harmonic voltages at the TCS node. Since again the latter are fed back to the input, H_1 and H_3 at the output decrease only minimally with increasing mismatch. H_2 of the TD-pair in Fig. 4-52 (b) degrades in contrast much faster than in the PD-pair in (a), as the difference of 6 dB at a mismatch of $m_T = 5$ % indicates. The reason for the faster degradation of H_2 has its origin in the internally introduced mismatch between the two transistors, which does not longer appear at both inputs as a CM-distortion of equal amplitude. It can be thus concluded that the most critical factor for the TD-pair is the even-order linearity degradation introduced by device mismatch.

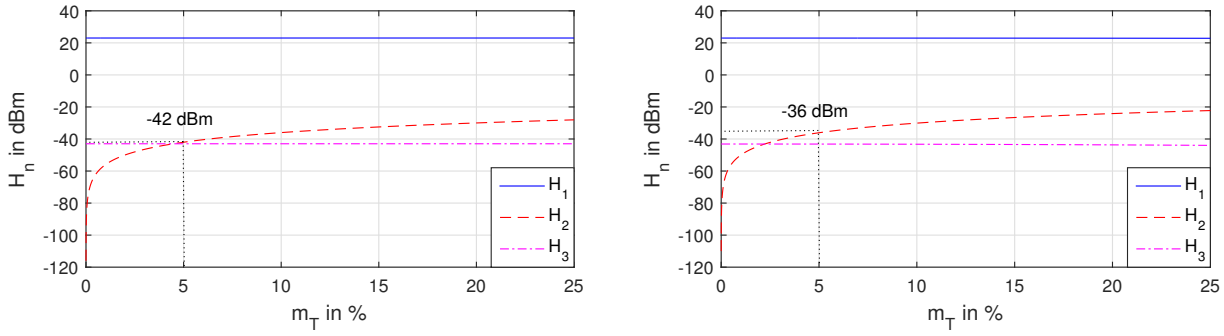


Fig. 4-52: Simulated/Computed spectral output components (H_1, H_2, H_3) in dBm vs. m_T in % of an ideal (a) PD-pair and (b) TD-pair with ideal TCS (g_{m1} = 0.1 S, g_{m2} = 0.01 S/V, g_{m3} = 0.001 S/V²)

One last important aspect with respect to process variations is the differential output signal response of the PD- and TD-pair to input CM-distortions ($V_{in,CM}$), which is also known as CM- to DM-conversion. Assuming that $g_{m,T1}$ is not exactly equal to $g_{m,T2}$ translates for the differential output current of the TD-pair into

$$\Delta I_{OUT} = V_{in,CM}\frac{g_{m,T2} - g_{m,T1}}{1 + (g_{m,T1} + g_{m,T2})Z_{CS}}, \tag{4.66}$$

with Z_{CS} being the complex impedance of the TCS-HEMT and $V_{in,CM}$ the common-mode input voltage amplitude. Equation (4.66) reveals that in case of device asymmetry a CM-distortion at the input leads to a DM-

distortion at the output. Since for the PD-pair Z_{CS} is always equal to zero, any component mismatch in the two differential paths leads one-to-one to an input CM to output DM conversion, such that e.g. CM-noise or CM-voltage vairations at the input lead to a distorted differential output signal. For the TD-pair in contrast Z_{CS} is always larger than zero, which manifests even for the non-ideal case with Z_{CS} being finite in a significant suppression of the CM-to-DM distorters. This is an important and advantageous feature of the TD-pair compared to the PD-pair, making the differential output signal less dependent on CM-distortions present at the input from preceding circuitry.

4.7.3 The Series Feedback Dilemma in TD-amplifiers

In order to design a differential FBPA down to DC, series as well as parallel feedback needs to be implemented, as it is the case for the single-ended FBPA. Parallel feedback poses no problem with respect to the external applied bias conditions. Series feedback in contrast shifts the gate bias voltage up due to the voltage drop across the series feedback resistor, which leads to an increased DC headroom for the TD-FBPA. Splitting of the tail current source into two current sources, as depicted in Fig. 4-53, would help to circumvent the DC voltage drop over R_S and hence help to minimize power dissipation.

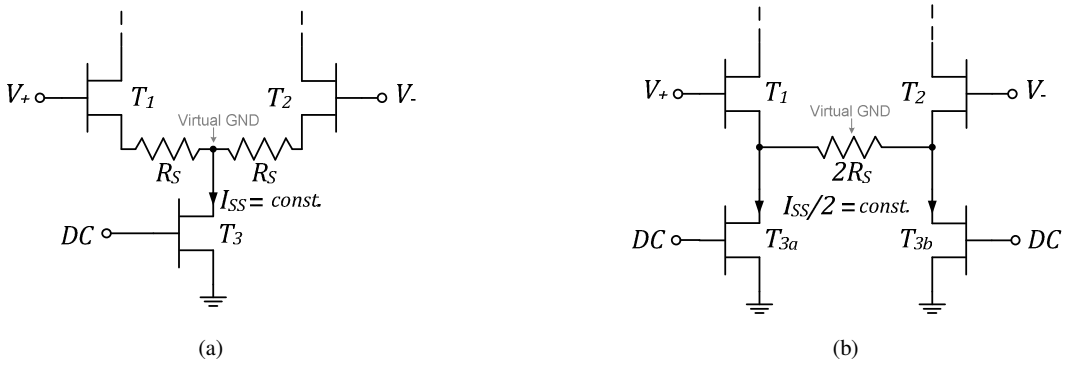


Fig. 4-53: TD-pair with series feedback and (a) common current source and (b) split current source

Based on the parasitic capacitances of the current source HEMTs T_{3a} and T_{3b} towards ground a parallel RC-low-pass at the source nodes of the differential pair HEMTs T_1 and T_2 is introduced in differential mode, which bypasses the series feedback resistor R_S and thus slightly degrades linearity, as shown in Fig. 4-54 (b). In terms of $CMRR$, this topology might be better suited than the single current source solution for lower frequencies, because the resistor $2R_S$ has no influence in common-mode and therefore does not increase the RC-time constant of the source impedance in common-mode, as it is the case for the single current source solution in Fig. 4-54 (a). However, for low frequencies the pure capacitive series feedback might lead to an instable behavior in CM, because its imaginary-part is turned into a negative real-part at the input (see also "Loss Compensation of Gate-Line" in section 3.4.6). When the parasitic capacitance $C_{P,CS}$ becomes shorted towards higher frequencies the advantage of a low series resistance turns into a disadvantage in terms of the $CMRR$, since the series R_S provides negative feedback and thus lowers the common-mode gain.

As a conclusion it can be stated that there are two compelling reasons why the presented double-current source solution has not been implemented in a first concept evaluation. First, a difference in threshold-voltages

of the current source HEMTs T_{3a} and T_{3b} due to device impairment leads to the undesired condition of unequal current distribution in T_1 and T_2. This makes the TD-pair asymmetric with respect to the virtual ground node and accordingly gives rise to even-order nonlinearities, as presented in the preceding section 4.7.2. Second, the parasitic capacitive loading leads to a reduced CM-suppression at high frequencies and to a reduced stability at low frequencies, as will be shown later in section 6.1.1.

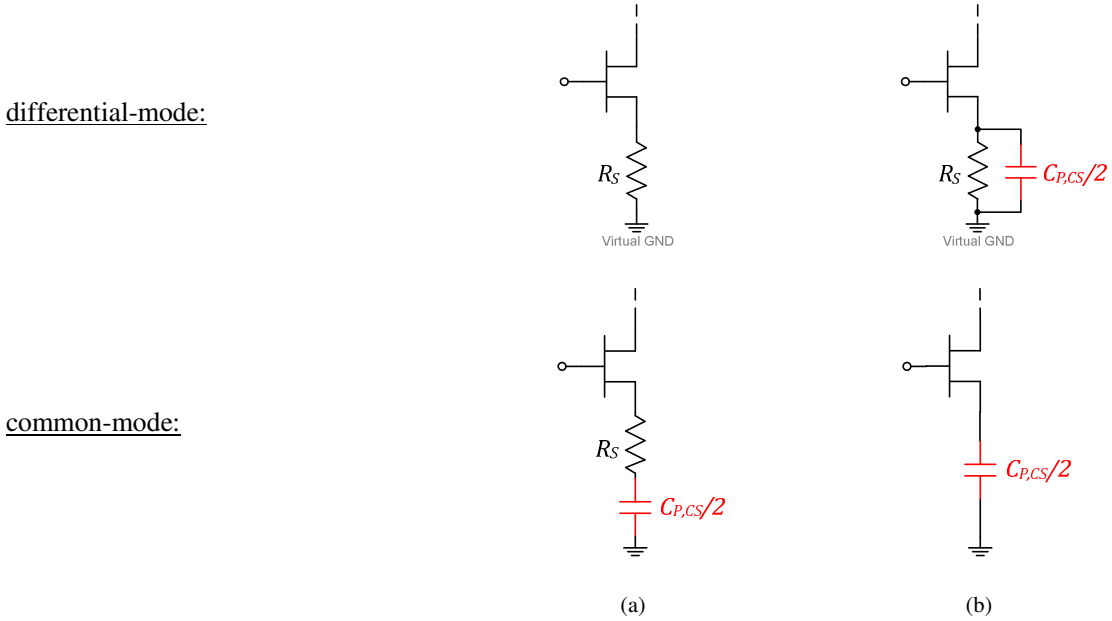
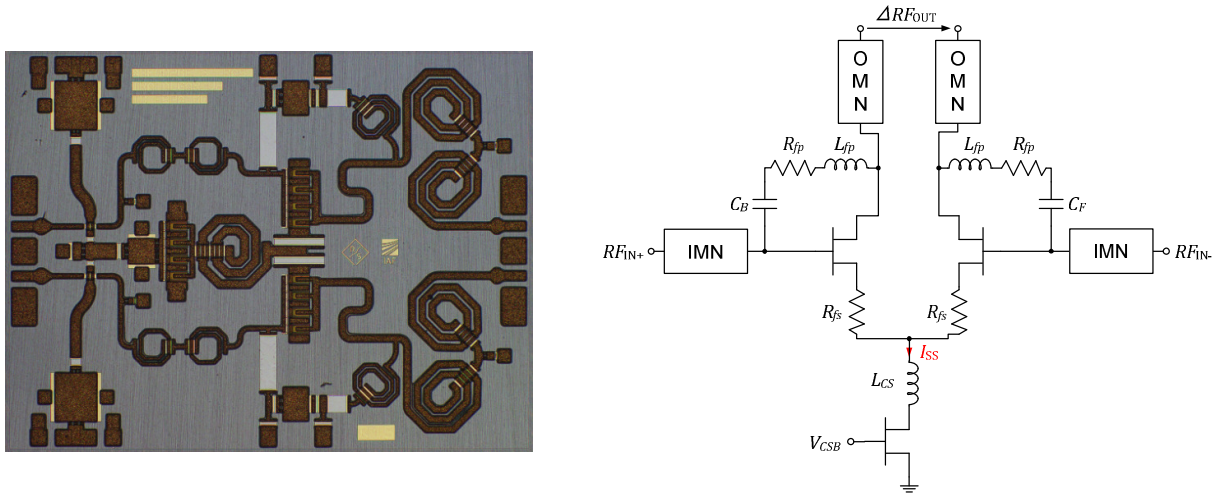


Fig. 4-54: Equivalent half-section of single- and double-current source solution of TD-pair for differential- and common-mode from (a) Fig. 4-53 (a) and (b) Fig. 4-53 (b)

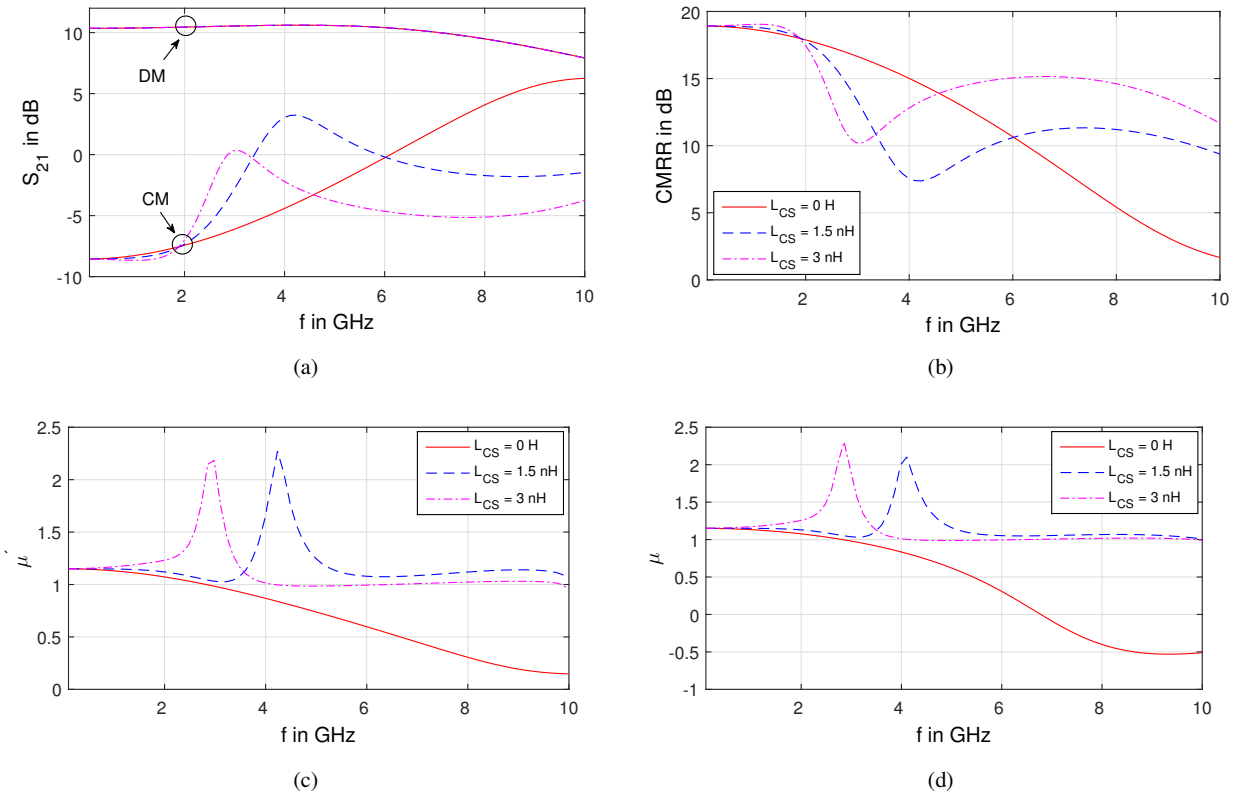
4.7.4 DC-6 GHz Truly-Differential PA Design

In order to assess and evaluate the expected theoretical linearity improvement of TD-FBPAs in GaN technology, a DC-6 GHz Truly-differential PA has been designed in the 0.25µm AlGaN/GaN technology from Fraunhofer IAF. The simplified schematic and its corresponding layout are depicted in Fig. 4-55 below. As can be seen, the circuit comprises parallel as well as series feedback and is additionally matched at its input and output via reactive matching networks (IMN/OMN). Two 8×125µm HEMTs without field-plates are taken for the differential pair to achieve 6 GHz of bandwidth and a tail current source HEMT with W_G= 8×125µm to maintain sufficient current control at low $V_{\mathrm{DS},CS}$ or V_{GG}, respectively. In order to suppress the rising CM-gain toward high frequencies, a series inductor (L_{CS}) is placed in series with the TCS-HEMT to compensate its output capacitance. The stabilizing effect for different inductor values on the DM-stability performance is sketched in Fig. 4-56 below. From (a) it becomes clearly visible that L_{CS} has no effect on the differential mode (DM) S_{21}, but helps to improve the high frequency $CMRR$ and thus stability, as depicted in (c) and (d). Additional bond pads in the parallel feedback path enable the connection of an external SMD capacitor to extent the operational bandwidth down to a few kHz if desired.



(a) (b)

Fig. 4-55: Photograph of DC-6 GHz truly-differential FBPA (a) "Trafalgar V2" and (b) corresponding simplified general schematic



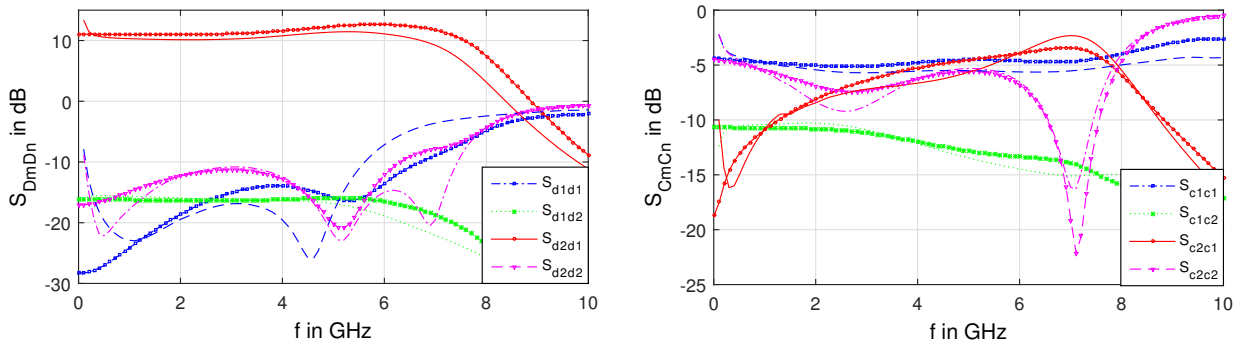
(a) (b)

(c) (d)

Fig. 4-56: (a) S_{21}, (b) $CMRR$, (c) μ' and (d) μ for different inductive compensation values of the parasitic capacitance towards ground of the TCS-HEMT

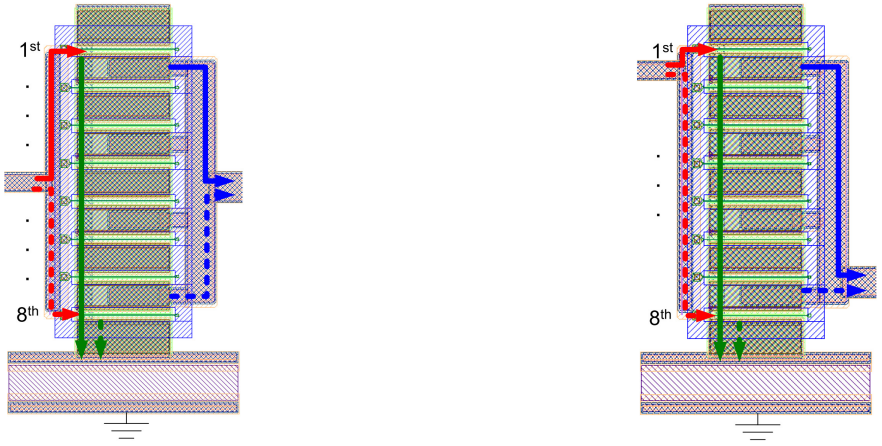
Small-Signal Performance

Fig. 4-57 depicts the simulated and measured differential (S_{DD}) and common-mode (S_{CC}) S-parameters. The simulated S-parameters match good with the measured data and show a S_{d2d1} of larger than 10 dB and a S_{d2d2} of smaller than -12 dB up to 6 GHz. Only S_{D1D1} in Fig. 4-57 (a) deviates from the simulated values, which leads to a bandwidth reduction of S_{D2D1} by roughly 1 GHz. The reason for the reduced bandwidth is mainly deemed to be rooted in the increased parasitic gate- and source-inductance (L_G , L_S) of the resulting asymmetry in the physical layout compared to the symmetric model. Since the model assumes a fully symmetric source termination, the modified asymmetric layout connection of the series feedback resistor R_{fs} in Fig. 4-55 (a) exhibits a larger series source inductance based on the higher number of air bridges connecting the source fingers farther away from R_{fs}.



(a) (b)

Fig. 4-57: Simulated (markers) & on-wafer measured (lines) (a) S_{DD} vs. f and (b) S_{CC} vs. f of DC-6 GHz TD-FBPA ("Trafalgar V2") for V_{DD} = 38 V, V_{GG} = 6 V and I_{DS} = 100 mA/mm



(a) (b)

Fig. 4-58: Layout of (a) symmetric gate/drain-bus connection (SBS) and (b) asymmetric gate/drain-bus connection (ABS) of an asymmetric source-terminated 8×125µm, as applied in the DC-6 GHz TD-FBPA ("Trafalgar V2")

Due to the single current source HEMT only one series feedback resistor can be connected at one side of the HEMTs, which results in an increased source inductance from the 1st to the 8th finger, as shown by the green

lines in Fig. 4-58. Splitting of the current-source HEMT into two individual current-sources would circumvent the limitation of one single asymmetric source feedback resistor and accordingly decrease L_S, but comes with several other drawbacks as was already addressed in the previous chapter 4.7.3. In order to compensate for the variation in inductance and propagation delay over the gate-fingers it is meaningful to connect the gate/drain-bus in an asymmetric manner, as sketched in Fig. 4-58 (b). When the gate-bus inductance L_G, based on the relationship $L_G \sim l_G$, is small (short solid red arrow), the source inductance L_S is large (long solid green arrow) and vice versa. In this way the gain of each finger can be held almost constant.

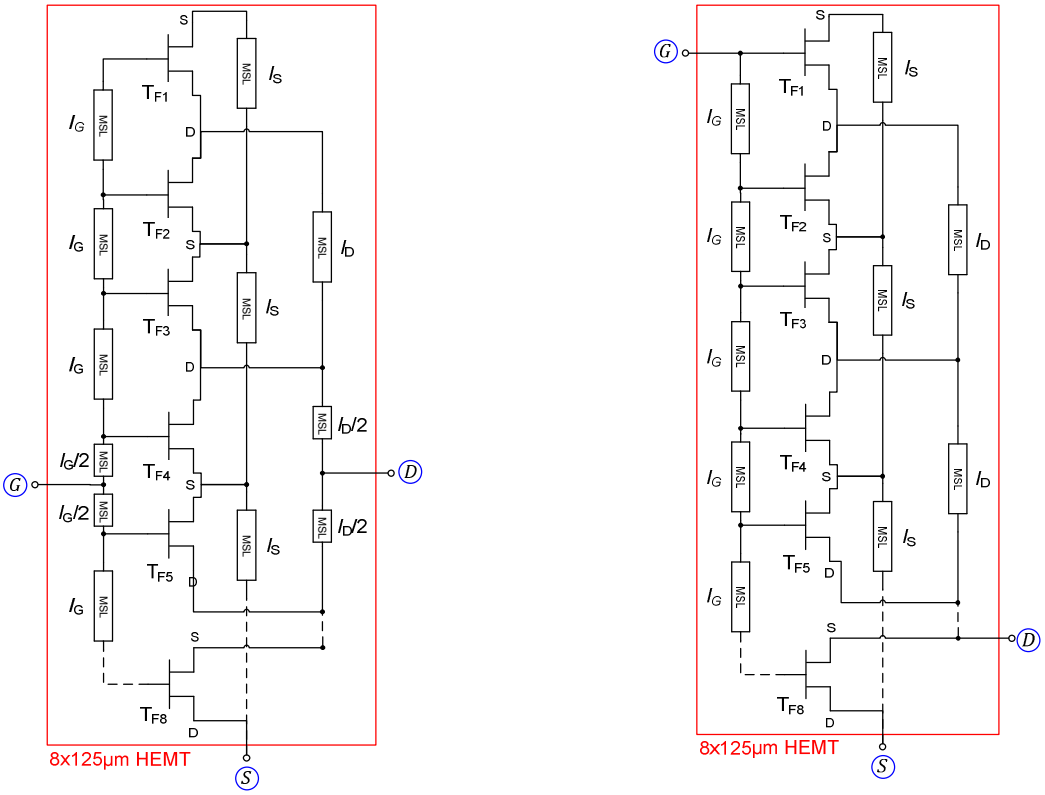


Fig. 4-59: Schematic of (a) symmetric gate/drain-bus connection and (b) asymmetric gate/drain-bus connection of the asymmetric source-terminated 8×125µm from Fig. 4-58

In order to proof the just made assertion, a distributed HEMT model presented in Fig. 4-59 of the symmetric and asymmetric gate-/drain-bus structure (SBS & ABS) from Fig. 4-58 was adopted. Thererin the 8×125µm HEMT is composed of 8 single intrinsic HEMTs ($T_{F,1-8}$), where each transistor finger itself is modelled by the same intrinsic small-signal model, as already presented in section 2.2.1. The microstrip interconnections connecting physically all of the fingers at the gate- and drain-side in the layout, as depicted in Fig. 4-58, are modelled by short MSL-sections. Moreover the source air-bridges are also approximated by simple short MSL-sections, whereby for all MSLs no intercoupling is so far considered. Table 4-3 and Table 4-4 summarize the model parameters applied for the distributed small-signal model fitted to the IAF-model and the distributed MSL elements taken from the layout.

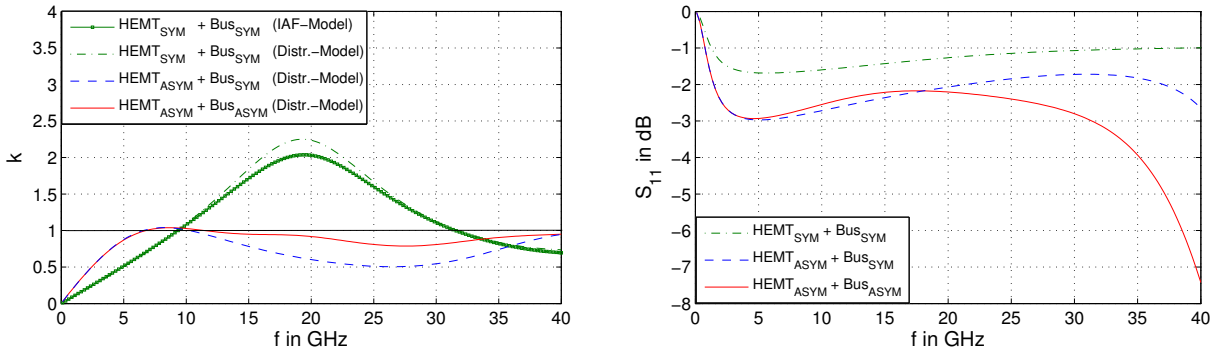
Table 4-3: Intrinsic HEMT parameters for $T_{F,1-8}$ of 8×125µm distributed GaN HEMT model from Fig. 4-59 (I_{DS} = 100 mA/mm, V_{DS} = 30 V)

$R_{GS,1-8}$ / Ω	$C_{GS,1-8}$ / fF	$R_{GD,1-8}$ / Ω	$C_{GD,1-8}$ / fF	$R_{DS,1-8}$ / Ω	$C_{DS,1-8}$ / fF	$g_{m0,1-8}$ / mS	τ / ps
9.6	194	96	13.2	1800	28.2	31	3.5

Table 4-4: MSL-parameters of distributed 8×125µm GaN HEMT model from Fig. 4-59 (I_{DS} = 100 mA/mm and V_{DS} = 30 V)

l_G / µm	w_G / µm	l_D / µm	w_D / µm	l_S / µm	w_S / µm
50	30	100	40	75	20

As Fig. 4-60 (a) and (b) illustrate, the error between the IAF-model and the approximated distributed model is negligibly small, allowing for a good evaluation of the optimal gate-/drain-bus structure by means of the small-signal distributed HEMT model. Fig. 4-60 (a) shows that the k-point of the asymmetrically source-terminated HEMT shifts down in frequency by roughly 2 GHz compared to the symmetric source-terminated HEMT. This is based on the increased source inductance, as already mentioned. More interesting is the question, which of the two possible gate-/drain-bus connections is better suited for a DC-6 GHz TD-FBPA design, the symmetric bus structure (SBS) or the asymmetric bus structure (ABS). Considering only the targeted frequency range, there is no vital difference between the SBS and ABS, based on the almost equal MSG/MAG characteristic up to 6 GHz. Above 6 GHz the ABS shows some minor improvement with predominant MSG/MAG performance in the X- to Ku-band. The stability factor k in Fig. 4-60 (a) additionally reveals that the ABS is more stable in that frequency range than the SBS without any additional stability measures. The reason for the better stability of the ABS can be explained by the higher input feeding inductance, providing in average a slightly better compensation of the effective input capacitance and thus better matching. This can be verified by taking a closer look at the input machting S_{11} in Fig. 4-60 (b).



(a) (b)

Fig. 4-60: Simulated (a) stability factor k vs. f and (b) S_{11} vs. f of SBS and ABS for an asymmetric source-terminated 8×125um HEMT in comparison to a 8×125um HEMT with SBS and symmetric source-termination

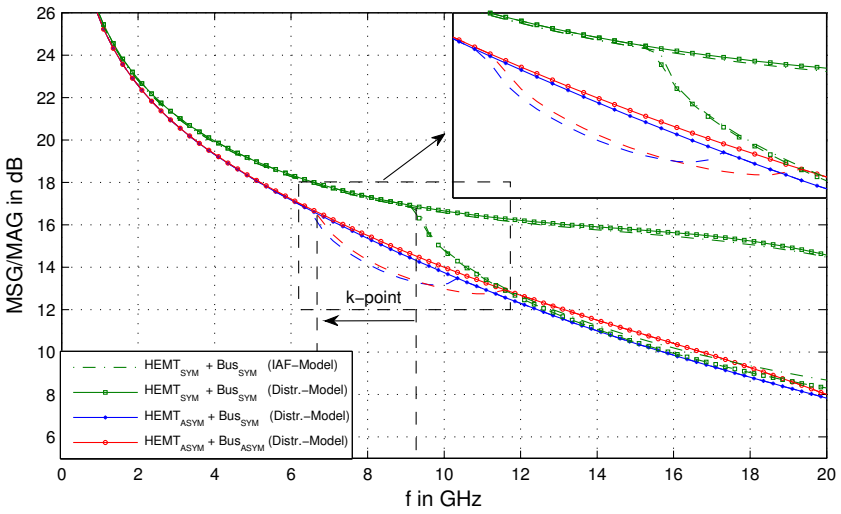


Fig. 4-61: Simulated MSG/MAG vs. f of SBS and ABS for an asymmetric source-terminated 8×125um HEMT in comparison to a 8×125µm HEMT with SBS and symmetric source-termination

So without sacrificing gain performance the ABS exhibits better high frequency stability, which was the decisive criterion for the implementation in the DC-6 GHz TD-FBPA design, presented in this chapter (see Fig. 4-55). Assuming that at very high frequencies the HEMT operates more like a distributed (traveling-wave HEMT) rather than a lumped structure, it is additionally beneficial to equalize the propagation delay on the gate- and drain-bus in order to maximize the gain. Unfortunately is the input capacitance C_{IN} of the HEMT roughly five times larger than the output capacitance C_{out}, leading to a much slower phase velocity on the gate-bus than on the drain-bus, according to

$$v_{ph} = 1/\sqrt{\left(L_{G/D}{}' \cdot C_{in/out}{}'\right)} \tag{4.67}$$

Out of this reason can the difference in propagation delay only be scaled to a minor extent, since the gate-bus inductance cannot be made arbitrarily small in order equalize the phase velocity on gate- and drain-line. In order to show the impact of unequal phase delays on the gate- and drain-bus between the center and outermost gate-fingers, the power loss of a SBS-HEMT with gate center feed (as depicted in Fig. 4-58 (a)) but symmetric source-termination is set into relation to the same SBS-HEMT, which exhibits equal phasing at each gate-finger and thus no delays. The resulting power loss (PL) can then be computed under assumption of a sinusoidal CW drive-signal dependent on the number of gate-fingers (NGF) to

$$PL = 20 \cdot log_{10}\left(\frac{NGF/2}{max\left\{\sum_{m=1}^{\frac{NGF}{2}} sin(\omega t + m \cdot \Delta\varphi)\right\}}\right). \tag{4.68}$$

$\Delta\varphi$ in (4.20) incorporates the phase delay between each gate-finger arising on the gate- and drain-bus. It is important to notify that the phase delay is linearly dependent on the gate-to-gate pitch (GG-pitch). Thus the smaller the GG-pitch, the lower the effect of a higher NGF. The graphs in Fig. 4-62 indicate that if the GG-pitch (or phase delay) is minimized, the power loss can be very easily minimized as well. This is only true if thermal

effects would be non-existant. In reality in contrast, an undershoot of a certain GG-pitch would lead to an enormous increase in channel temperature due to thermal coupling of the gate-fingers, which would in turn degrade output power to a greater extent than the reduced losses based on the distributed gate-/drain-bus effects. Therefore, an optimum for NGF and the GG-pitch exists, which maximizes the power gain-bandwidth product. Fig. 4-62 reveals that for delay lengths larger than $\lambda/20$ between each gate-finger, significant power losses of greater 0.5 dB for $NGF > 8$ occur. This translates for a W_G = 1 mm device into a GG-pitch of larger than 50 µm at 20 GHz ($\lambda/20$) above which distributed effects start to dominate the power loss. Based on these considerations and the presented gate- and drain-bus feeding structure, the 8×125µm HEMT with a 50µm GG-pitch is deemed to come very close to the electrical and thermal optimum within this 0.25µm GaN process and has therefore been used for the design of the TD-FBPA.

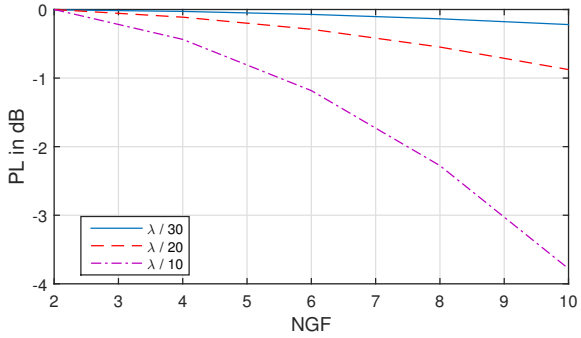
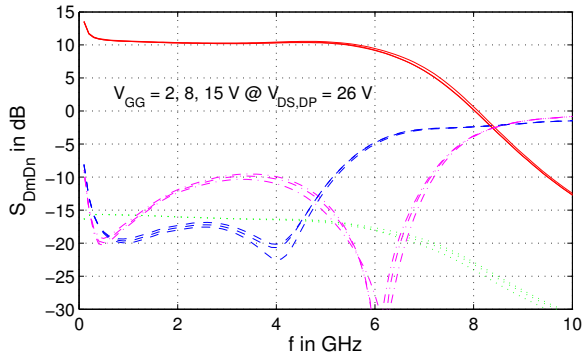
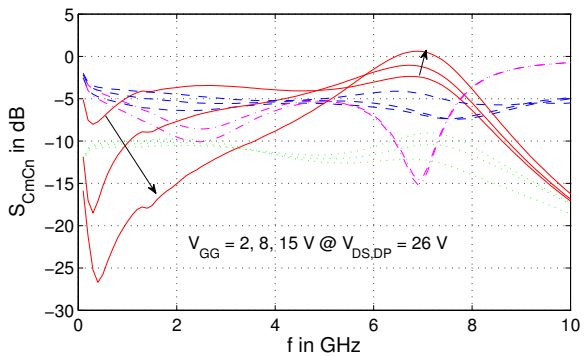


Fig. 4-62: Power loss (PL) vs. number of gate-fingers (NGF) for different phase delays ($\Delta\varphi = \lambda/x \cdot 360°$) between each gate-finger in a SBS-HEMT with symmetric source-termination

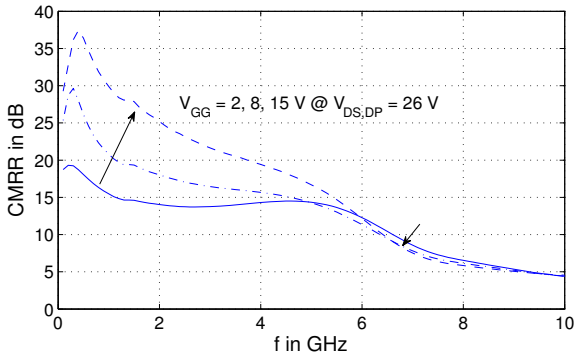
Visible in Fig. 4-63 (b) is the increase of S_{C2C1} over frequency due to the output capacitance of the tail current source HEMT, leading also to a decay in $CMRR$ towards the upper band. The interesting point is the dependency of the $CMRR$ on the applied bias. Due to the fact that the output capacitance and resistance of the GaN HEMTs are strongly dependent on V_{DS}, especially close to their knee-voltage, a strong dependence of the $CMRR$ on the applied gate-bias voltage V_{GG} is to be expected, which is underlined by the on-wafer measured S-parameter in Fig. 4-63 (b). When V_{GG} is increased the $CMRR$ in (c) increases as well at low frequencies but decreases at the band edge for constant applied $V_{\mathrm{DS},DP}$ = 26 V. Since $V_{\mathrm{DS},DP}$ is kept constant, no major change in the differential S-parameters S_{DmDn} can be noticed in (a).



(a)



(b)



(c)

Fig. 4-63: On-wafer measurement of (a) S_{DD} vs. f, (b) S_{CC} vs. f and (c) $CMRR$ vs. f of DC-6 GHz TD-FBPA ("Trafalgar V2") for different V_{GG} with $V_{\mathrm{DS},DP}$ = 26 V

Linearity Performance

In order to assess the linearity performance of the TD-FBPA large-signal one-tone as well as two-tone measurements were conducted. By means of additional baluns at the input and output of the die, a large-signal single-ended measurement setup was used, comprising a PNA-X NWA for sensing the input and output signals and an additional driver PA to obtain 1 W of drive power. The frequency dependent attenuation introduced by the baluns was de-embedded by preceding back-to-back measurements. The existing phase imbalance of the balunes was determined to $\pm 5°$ over the bandwidth from 1-26.5 GHz by reference measurements, which was also accounted for in the simulation for a more realistic comparsion between simulation and measurement. The most critical part for proper linearity assessment of the TD-FBPA is the driving amplifier itself, which produces significant spurs. It is therefore of utmost importance to guarantee a sufficiently large dynamic range of at least 80 dBc at the input to obtain accurate HD measurement results of the linear TD-FBPA. If the dynamic range is smaller than the one of the DUT, the measured HD at the output is misleadingly dominated by the one of the driver amplifier. Out of this reason six narrow bandpass filters matched with their center frequency to each corresponding input frequency were used in the measurement setup to synthesize a purely sinusoidal drive signal and thus to guarantee a sufficiently large DR of the measurement setup.

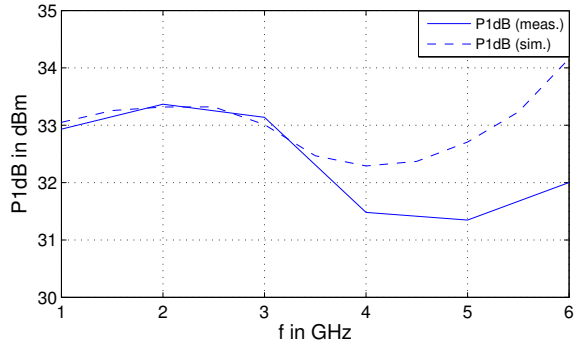
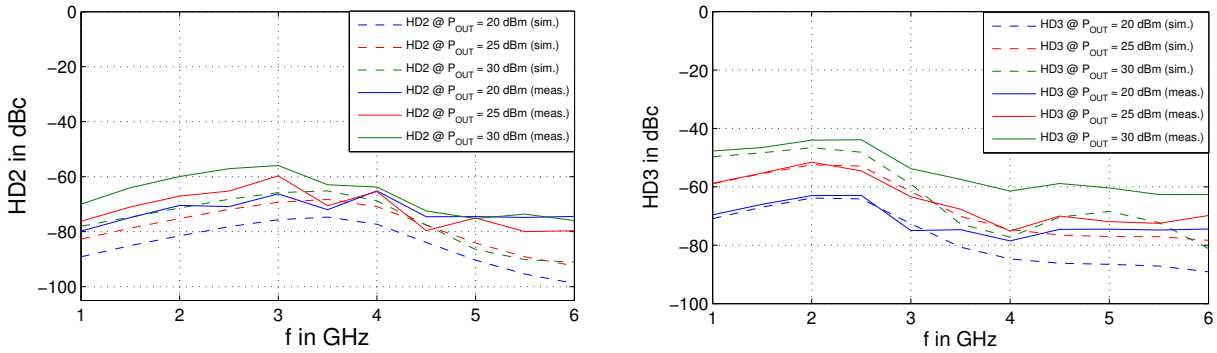


Fig. 4-64: On-wafer measurement of $P1dB$ vs. f of DC-6 GHz TD-FBPA ("Trafalgar V2") at V_{DD} = 38 V, V_{GG} = 6 V and I_{DS} = 200 mA/mm

Fig. 4-64 shows that the on-wafer measured $P1dB$ of the TD-FBPA at V_{DD} = 38 V, V_{GG} = 6 V and I_{DS} = 200 mA/mm is in good correlation with the simulation. Solely above mid-band, the $P1dB$ seems to be overestimated by the model due to the slightly worse matching toward 6 GHz, which deteriorates and hence decreases the bandwidth, as already presented by the S-parameters in Fig. 4-57 (a). The very good even-order harmonic suppression of the TD-FBPA can be observed from Fig. 4-65 (a), where the usually dominant second-order harmonic is around 15-20 dB lower than the third-order harmonic. A $HD2$ of still lower than -55 dBc at 30 dBm of output power at mid-band was measured. The difference in $HD2$ of roughly 10 dB between simulated and measured data is deemed to result from the non-ideal symmetry of the two differential branches, caused by intra-cell process spread. Besides the even-order linearity deterioration due to phase imbalances, as shown in section 4.7.2, symmetry plays the second crucial part in even-order harmonic suppression. The higher the symmetry of the differential circuit, the better the even-order linearity performance. Odd-order nonlinearity in the TD-FBPA in contrast is not affected by circuit symmetry and is solely dependent on the linearity of the amplifying HEMTs and the amount of feedback linearization. Surprisingly, the $HD3$ results even show that the TD-FBPA outperforms the single-ended FBPA also slightly in its odd-order harmonics, which can be traced back to the overall larger TGW of 2 mm compared to the 1.75 mm of the CS-FBPA from chapter 3.3.4.



(a) (b)

Fig. 4-65: On-wafer measurement of (a) $HD2$ and (b) $HD3$ vs. f at P_{OUT} = 20, 25 & 30 dBm of the DC-6 GHz TD-FBPA ("Trafalgar V2") with V_{DD} = 38 V, V_{GG} = 6 V and I_{DS} = 200 mA/mm

Fig. 4-66 presents the on-wafer measured third order intermodulation performance in presence of a two-tone signal with a spacing of Δf = 5 MHz at the input of the TD-FBPA. The TD-FBPA achieves an $OIP3$ of larger than 51 dBm at 1 GHz and 46 dBm at 6 GHz and shows the typical decaying trend over frequency, which stems from the inductive parallel feedback (see also chapter 3.3.4). Again, the measurement fits well to the simulation, whereby the deviation of around 3 dB at 1 GHz results from the limited dynamic range (DR) of the measurement setup. To further reduce the amount of intermodulation present at the input of the measurement system and hence to obtain more accurate $OIP3$ results, either each driver amplifer needs additional harmonic filtering before summation of the two signals in the power combiner or the isolation between the two signal sources needs to be increased by insertion of additional attenuators or isolators. Since for the conducted measurement no low loss isolators were available, a maximum of 6 dB of attenuation in each path could be inserted in front of the power combiner in order to minimize mixing of the two input signals. The limiting parameters in the measurement were the maximum drive signal of the PNA-X, its introduced nonlinearity and the noise floor. It is important to recall that even if the drive signal would be an ideal sinusoid, the signal-to-noise ratio still determines

the maximum achievable DR, so that the drive signal cannot be arbitrarily decreased to reduce the driver PA nonlinearities to a minimum amount.

The measured $OIP3$ result clearly shows that the designed TD-FBPA exhibits, besides its outstanding even-order harmonic suppression, also very good intermodulation performance and is therefore a good candidate for the application in vector signal generators for emulating 3GPP communication standards such as e.g. LTE, UMTS/HSPA, GSM/EDGE, WCDMA/TD-SCDMA, WLAN or WiMAX.

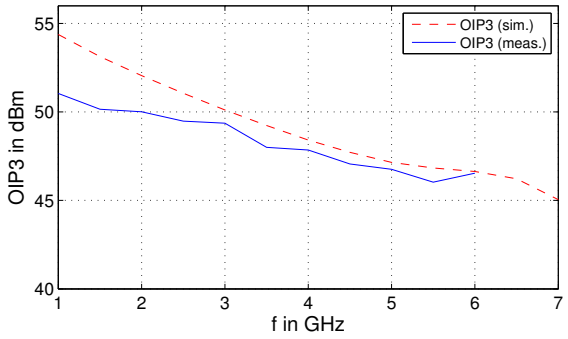


Fig. 4-66: On-wafer measurement of average $OIP3$ vs. f with Δf = 5 MHz of the DC-6 GHz TD-FBPA ("Trafalgar V2") at V_{DD} = 38 V, V_{GG} = 6 V and I_{DS} = 200 mA/mm. (Remark: simulation result accounts for 5° phase input imbalance)

Differential Noise Performance

Several methods for differential noise measurements have been published in the last decades of which most of them are based on single-ended two-port noise measurements by using baluns and a proper deembedding procedure [156, 157, 158]. Belostotski´s method in contrast provides the nice feature of measuring the differential NF without the necessity of extra baluns and thus can be done with standard noise measurement equipment [159]. Due to its simplicity, the on-wafer differential NF measurements of the TD-FBPA were therefore conducted according to "Belostotski's"-method. This method is an effective and fast measurement approach, which relies on multiple single-ended noise measurements. Since the whole method is based on single-ended measurements, correlated noise arising from the TCS-HEMT is treated as uncorrelated. As long as the $CMRR$ is large, only a negligible error will be introduced, because any noise generated by the TCS-HEMT will appear in common-mode and hence will not be transferred to the output. If the common-mode signals are not sufficiently suppressed due to a low $CMRR$, the correlated noise of the TCS-HEMT becomes a significant error component in this method, because Belostotski's method treats correlated noise always as uncorrelated. The basic concept of this method is to measure the noise figure at the two output ports and its corresponding single-ended direct- and cross-transducer gains from the input to the output ports ($S_{31}, S_{41}, S_{32}, S_{42}$). Based on the symmetry of the topology it results that $NF_{42} = NF_{31}$ and $NF_{32} = NF_{41}$ as well as $G_{42} = G_{31}$ and $G_{32} = G_{41}$. Based on these assumptions the differential NF computed in [159] further simplifies to

$$NF_{diff} = 10 \cdot log_{10}\left(1 + \frac{N_{as}}{kT\Delta f}\right), \tag{4.69}$$

where N_{as} in (4.69) stands for the input referred equivalent noise powers at port 1 and port 2. Due to the symmetry, N_{as} is equal to $N_{as} = 0.5 \cdot (N_{as1} + N_{as2})$ and can be hence computed by

$$N_{as} = \frac{kT\Delta f \cdot (G_{31} - G_{32}) \cdot \left[\frac{G_{31}F_{31} + G_{32}F_{32}}{2} - G_{31} - (G_{32} + G_{34})\right]}{{G_{31}}^2 - {G_{32}}^2} \tag{4.70}$$

Equation (4.70) gives the most simplified way to determine the input referred noise power of a fully symmetrical differential amplifier. Based on the fact that the system of equations is overdetermined for a fully symmetrical design, additional measurement data from ports 1 and 2 to the output port 4 can be used to reduce possible existing measurement errors by averaging. Assuming a perfectly calibrated measurement setup, equation (4.70) solely describes the input referred noise power from which the differential NF of the TD-FBPA can be calculated by this single equation. Furthermore, the measurement of the transducer gain between the two output ports (G_{43}, G_{34}), which would be necessary for an exact determination of the differential NF from (4.69) and (4.70), can be omitted without introducing significant error. Because G_{34} (or G_{43}) is in general very small compared to the direct transducer gains G_{31} (or G_{42}) its noise contribution toward the output is negligible. This also simplifies the measurement procedure, because the noise figure analyzer (NFA) or network analyzer (NVA) does not need to inject a measurement signal at the output ports to measure G_{34} and G_{43}, This reduces the expenditure of time for reassembling the measurement setup.

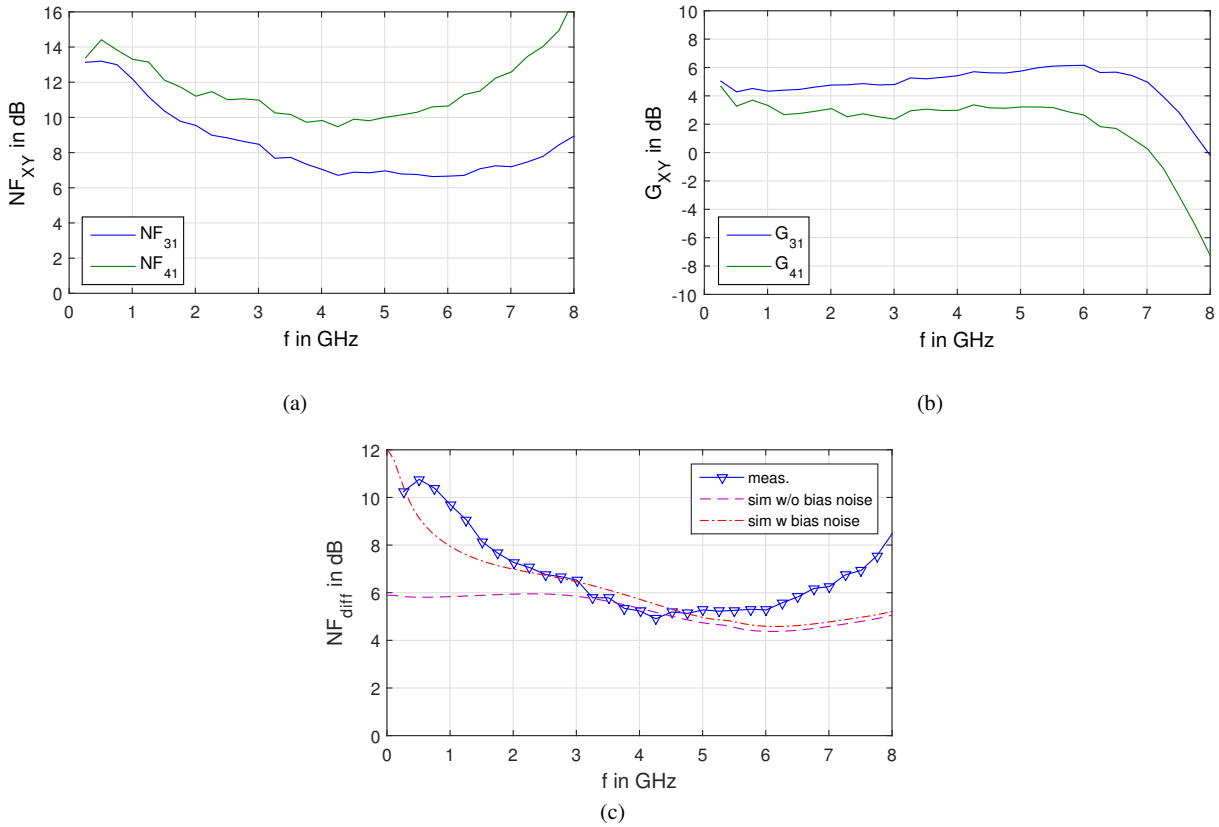


Fig. 4-67: On-wafer measured (a) NF_{31} & NF_{32}, (b) G_{31} & G_{32} and (c) NF_{diff} compared to simulated NF_{diff} w & w/o TCS bias noise of the DC-6 GHz TD-FBPA ("Trafalgar V2") at V_{DD} = 38 V, V_{GG} = 6 V and I_{DS} = 200 mA/mm.

Fig. 4-67 depicts the on-wafer single-ended NFs and transducer gain measurements from port 3 to port 1 and from port 3 to port 2 of the TD-FBPA, which can be computed by means of [159]. From Fig. 4-67 (c) it can be seen that NF_{diff} of the TD-FBPA increases unexpectedly toward low frequencies. This is not an artefact of the "Belostotski"-method but rather the result of the TCS-HEMT gate-biasing scheme. As can be seen from Fig. 4-55 (a), the gate-bias to the TCS-HEMT is fed via some additional series gate resistors, which help to reduce the sensitivity of the TCS-HEMT with respect to distortions arising from external circuitry. Unfortunately, these resistors exhibit thermal noise, which is amplified by the g_m of the TCS-HEMT and thus generates a large amount of correlated noise in the amplifier. Though the $CMRR$ is largest at low frequencies, it is not large enough to fully suppress all noise injected by the gate-bias resistors, especially at low frequencies. The comparison of the measured and simulated data in Fig. 4-67 (c) reveals that by introducing a large blocking capacitor at the gate-node of the TCS-HEMT the low frequency noise can be filtered out. For operation down to a few MHz it is thus a viable solution to make use of an external SMD capacitor close to the gate of the TCS-HEMT, when a large on-chip capacitor cannot be placed due to the spatial layout limitations.

4.7.5 Key Findings

To the author´s best knowledge the well-known differential concept for even-order harmonic cancellation has been applied in GaN technology for the first time. Prior to the design of a DC-6 GHz truly-differential demonstrator PA, an analytical and simulation based study of the susceptibility to phase, amplitude and process imbalances of a pseudo-differential (PD) and a truly-differential (TD) pair was conducted. From this analysis it can be concluded that the susceptibility of the even-order harmonics to input phase and amplitude imbalances is much lower for the TD-pair than for the PD-pair. The superior performance in $HD2$ of the TD-pair compared to the PD-pair is mainly owed to the fact that the HEMTs in the differential pair share a common tail current I_{SS}, which is forced and fixed by the tail current source (TCS). Although, the magnitude of H_3 in ΔV_{OUT} for the PD-pair can be significantly lower opposed to the TD-pair, when $\Delta\phi$ is close to $\pi/3$. For the TD-pair, the magnitude and sign of g_{m3} (k_3) plays a major role for the final value of H_3 at the output, because the contribution from the 2nd order mixing-term to H_3, based on the feedback of the 2nd harmonic from the TCS drain node to the input, affects the overall output H_3. For a positive 3rd order nonlinear coefficient g_{m3} (k_3), H_3 can be partly cancelled out as long as the 2nd order feedback mixing term exhibits a similar magnitude as g_{m3}. For the case of input amplitude imbalances the dependence of H_1, H_2 and H_3 on Δa is quite similar to the case of phase imbalances. For amplitude imbalances even up to 3 dB no impact on the odd-order harmonics in the PD- as well as TD-pair are noticeable. For the even-order harmonics (H_2) in contrast, a direct linear degradation of the PD-pair with Δa and input amplitude A can be observed, whereas the TD-pair shows only a very weak dependence on Δa with almost perfect suppression of the even-order harmonics. More critical is the susceptibility of the TD-pair to transistor mismatches m_T, which result from slight process variations even within one cell on a wafer. A small difference in transconductance between the two transistors leads to unequal nonlinearities in each of the two transistor paths. The same accounts for the PD-pair, but with the difference that the odd-order nonlinearities in the TD-pair are coupled to the input via the feedback over the TCS, which does not apply for the separately grounded PD-pair. The reason for the fast degradation of H_2 with increasing m_T is based on the feedback of H_3 at the TCS to the input, which contributes via 2nd order mixing with the fundamental input tone directly to H_2 at the output. The latter effect leads thus to a much faster degradation of H_2 at the output with increasing m_T for the TD-pair.

In order to verify if the theoretically derived advantages of a TD-topology in GaN hold true in reality, a DC-6 GHz TD-FBPA was designed in the GaN25 technology from IAF. In terms of linearity, the $HD2$ of the TD-FBPA improves by more than 25 dB compared to the single-ended FBPA design from 3.3.4. At only 6 dB back-off (P_{out}= 30 dBm) the $HD2$ is still larger than -55 dBc. The third harmonic represents the dominant distorter in the TD-FBPA design opposed to the usual dominant second harmonic in GaN single-ended designs. This leads to an increased $SFDR$ of over 10 dB of the TD-FBPA design compared to the single-ended FBPA design. Two-tone measurements reveal also a very good intermodulation performance with an $OIP3 > 51$ dBm at 1 GHz and an $OIP3 > 46$ dBm at 6 GHz, making the TD-FBPA a very suitable candidate for the application in T&M instruments, such as e.g. VSGs. The comparison of the small-signal simulation and measurement results shows that the asymmetric source-connection of the HEMTs in the TD-pair is reasonably well predicted by the modified distributed small-signal models. Only S_{11} differs based on the different gate-bus/source inductance (L_G, L_S). The NF of the presented TD-FBPA exceeds the one of the single-ended FBPA by ~1.5 dB at the center frequency due to additional noise coming from the TCS-HEMT and its gate-bias resistors. Towards DC, the NF in the TD-FBPA rises significantly due to the noise coming from the bias resistors in the gate path of the TCS-HEMT. Due to the limited $CMRR$ in GaN, common-mode noise generated in the TCS-HEMT can be a major contributor at the output. Placing a large capacitor at the gate-node toward ground of the TCS-HEMT helps to filter any noise coming from the bias circuitry. Differential noise measurements by means of baluns are deemed to be advantageous compared to the Belostotski method due to the relative low $CMRR$ in GaN TD-pairs. Any correlated noise arising from the TCS-HEMT is considered as uncorrelated in the Belostotski method and thus the NF is very likely to be overestimated. The higher the $CMRR$ the lower the introduced NF measurement error by the Belostotski method.

The following Table 4-5 summarizes once again advantages and disadvantages of a PD- and TD-pair with respect to the critical design parameters output power, linearity and noise.

Table 4-5: Comparison of important PD- and TD-pair parameters

	PD-pair	TD-pair
Self-biasing	• Yes	• No
Linearity	• P_{IN} dependent • Less prone to process mismatches	• P_{IN} independent due to fixed TCS-current • Linearity is less prone to amplitude & phase imbalances
Noise	• Roughly 3 dB higher NF opposed to single-ended CS-HEMT	• Slightly larger than in a PD-pair (dependent on $CMRR$ for TCS noise suppression) • Suppression of input CM-noise to output DM-noise
Output Power	• Not limited by bias current	• Maximum is limited by constant I_{SS} of TCS

4.8 Conclusion

Among the five analyzed linearization concepts in the preceding chapters 4.3 to 4.7 are three, which show from the simulation and measurement results a real linearity improvement for the design of highly linear multi-decade wideband PAs. These three are the well-known parallel- and series feedback linearization, the nonlinear diode predistortion and the differential pair concept.

The first and oldest concept of parallel- and series feedback linearization turns out to be still one of the most promising concepts, which enable decent small-signal matching, low-noise performance and wideband operation with still high output power, as the measurement results of the DC-6 GHz FBPA in 3.3.4 already revealed. Furthermore, its compactness and simple topology makes the FBPA very efficient in terms of die size and thus attractive from a cost perspective. A detailed analytic investigation within chapter 4.3 has once again shown that with incrasing feedback the linearity improves effectively. Interestingly, it transpired that a $HD3$ and $IM3$ sweet-spot in FBPAs occurs, which is dependent on the amount of loop-gain and the sign of the 3rd order nonlinear coefficient. As long as g_{m3} is negative, no sweet-spot is present, but for a positive sign full cancellation of the 3rd order nonlinearity can be achieved. Translated to the utilized GaN25 technology this means that class AB to A operation never yields such a sweet-spot. Deep class AB operation in contrast yields a positive g_{m3}, which leads to a very low 3rd harmonic and also intermodulation products. However, this comes unfortunately at the cost of an increased 2nd harmonic due to the very large g_{m2} around the g_{m3}-zero, which thus increases the $SFDR$ again.

The second promising concept is based on diode predistortion and has been applied for the first time in a distributed topology in order to integrate the additional complementary nonlinear capacitance of the predistortion diodes into the artificial gate-line. This limits the operational BW opposed to parallelized PA topologies only to a minor extent and is thus well suited for PA designs over multiple decades. The nonlinearity introduced by the transistors input capacitance takes more and more effect with increasing frequency due to the increasing displacement current. When addind an anti-parallel diode, a capacitance with opposite dependence on the input drive signal leads to a compensation of the HEMT´s nonlinear input capacitance, such that the output nonlinearity of the DPA/TWA toward high frequencies can be partly cancelled out. Although, due to the different operating points for the diode and the HEMT, the nonlinearity arising from C_{GD} of the HEMT is due to the Miller effect A_V-times larger than the complementary nonlinearity of the anti-parallel diode. A full nonlinearity cancellation by means of a simple anti-parallel diode is thus not feasible. Nevertheless, the measurement results of a DC-6.5 GHz TWA applying the diode predistortion concept reveal a very good linearity performance, especially toward higher frequencies. With a TGW of only 1.3 mm the L²NTWA achieves an $OIP3$ of larger than 42 dBm over the whole band. Single-tone HD measurements also underline the high linearity of the design with an HD of smaller than -38 dBc at an output power of 20 dBm.

The third linearization concept makes use of a differential pair as amplifying stage in order to suppress all even-order harmonics at the output and hence increases the $SFDR$. An in-depth analytical and simulation based investigation of the general susceptibility to phase and amplitude imbalances as well as process variations of a pseudo-differential pair (PD) compared to a truly-differential pair (TD) was conducted in 4.7.2. The analysis showed that the TD-pair is less prone to input phase and amplitude imbalances but exhibits worse linearity performance in terms of process related mismatch. Since the latter takes only noticeable effect for mismatches larger than 1%, it is not deemed to be a critical factor for two closely spaced transistors on one single die. Based on the preceding analysis, a DC-6 GHz FBPA based on a TD-concept was designed for the first time in GaN technology. The measurements showed an improvement of more than 25 dB down to -60 dBc in $HD2$ at an output

power of P_{out} = 25 dBm and more than 10 dB improvement down to -55 dBc in $SFDR$. Above all, two-tone intermodulation measurements revealed additionally a very high $OIP3$ of larger than 46 dBm at 6 GHz and even 51 dBm at 1 GHz, underlying the outstanding linearity performance of the TD-FBPA in GaN technology.

Besides the just mentioned three implemented linearization concepts, the concept of derivative superposition (DSM) as well as the staggering drain-line principle for TWAs were also investigated from a theoretical point of view for a possible implementation in GaN. Based on the theoretical analysis with respect to the targeted specifications, the decision was made to skip the verification of these two concepts by hardware implementations. From the analysis of the derivative superposition method (DSM) it turned out that the g_m-shape of the utilized GaN25 process is not well suited for an efficient linearization. Due to the very sharp turn-on behavior together with the gain maximum located at deep class AB, the GaN25 technology is originally optimized for achieving high efficiencies rather than high linearities. This process characteristic counteracts the DSM for maintainting g_{m3}-cancellation over a large input dynamic range. To boost the dynamic range up to a useful level, a high number of parallel stages with only slightly shifted gate-offset voltages would be necessary in order to significantly raise the dynamic range of the 3rd order nonlinearity cancellation. Moreover, in favor of an increased $SFDR$ a compromise between 2nd and 3rd order nonlinearity cancellation has to be made, since the 2nd order nonlinearity exhibits its maximum when the 3rd order nonlinearity is minimized. Based on these theoretical findings, the conclusion is that for achieving good intermodulation performance and large $SFDR$s at the same time, the DSM as standalone linearization concept is not suitable for the linearization of wideband PAs over multiple decades. Although, due to the improved 3rd order linearity performance, one might think for a future implementation of a differential-DSM, which additionally alleviates the dominating even-order nonlinearities present in the single-ended DSM.

For a general understanding of the TWA linearity characteristics, the single-tone and two-tone linearity response a uniform DPA has been analytically computed, dependent on the number of stages and on the electrical gate- and drain-line lengths. To the author´s best knowledge, for the first time the general HD dependence on N in a UDPA has been analytically identified to be proportional to $HDm \sim (1/N)^{m-1}$. So, by increasing the number of stages N, the amount of harmonic distortion can be reduced. In principle, the larger the order of the nonlinearity the higher is the suppression. If on top a certain amount of phase delay between the gate- and drain-line is introduced, higher order harmonics can be suppressed at the output. To fully eliminate the m^{th}-order harmonic component at the output, a phase delay of $m \cdot 90°/N$ per section is required. The introduction of the phase delay is also called “staggering” of the drain-line, which has been already reported in [144, 145] as a successful measure to improve intermodulation performance. Out of this reason, the improvement of the $C/IM3$-ratio with increasing N and phase delay (“staggering”) on the drain-line was also once again theoretically reviewed and verified. However, since a phase delay of around $180°/N$ would be necessary to effectively suppress the dominating 2nd harmonic for an increase of the $SFDR$ of the UDPA, the gain and/or BW would strongly be degraded. The staggering drain-line principle is therefore to the author´s opinion not the best approach under the given linearity specifications and as such was not implemented on chip-level.

CHAPTER 5

NOISE REDUCTION SCHEMES

Within this section noise improvement schemes for FBPAs and TWAs will be discussed, based on the acquired theoretical understanding from chapter 3.4. As already presented in chapter 3.3.2, the noise performance in a FBPA is mainly determined by the selection of the optimum bias-point for the HEMT and by the amount of applied resistive feedback in order to stay as close as possible to the optimum noise matching trajectory in the Smith-Chart. Apart from these general noise trade-offs in FBPAs, a feedforward noise cancellation (FFNC) concept will be reviewed in chapter 5.1 and its applicability for a further noise reduction in GaN FBPAs investigated.

As has been discussed in detail in chapter 3.4.3, especially the increase in NF toward DC is an undesired characteristic in conventional TWAs. The cause for this rise in noise was shown to be generated by the reverse transfer function from the gate-termination resistor R_{GT} to the output port RF_{OUT} (see (3.102)), which amplifies the thermal noise power $k_B T$ present in the resistive load R_{GT} to the output. In theory, NF values below 3 dB in TWAs with perfectly matched gate- and drain-lines cannot be realized by matched resistors. The simplest improvement thus would be to introduce mismatch between the characteristic gate-line impedance Z_0 and the gate termination R_{GT} to minimize noise matching. Unfortunately, this deteriorates at the same time S_{11} of the TWA and is hence only up to a certain point a viable method for the low frequency NF improvement. Out of this reason, chapter 5.2 will present two approaches, which are capable of reducing the low frequency NF in TWAs by active cold load (ACL) terminations in the gate-line.

5.1 Feedforward Noise Cancellation in FBPAs

Taking a look back at the noise analysis of the FBPA presented in section 3.3.2 and the resistive input matching chapter in 3.2.1 shows that the feedback structure is a suitable candidate for retaining low noise performance at low frequencies together with a wide input impedance match. Nevertheless, F_{min} increases with increasing amount of feedback on the one hand, because of the decreasing gain and on the other hand due to the introduction of lossy components in the series- and parallel-feedback paths. It might be thus desirable to build a

circuit, where the input matching is independent of the noise performance. This can be achieved by making use of a feedforward noise cancellation (FFNC) concept, which is described in F. Bruccoleri´s *et al.* excellent paper on thermal noise cancellation in LNAs [160]. After shortly reviewing the general idea of the FFNC-concept, one promising topology will be more closely examined for a possible implementation in FBPAs in GaN-technology.

5.1.1 General FFNC Principle

In the following, the theory behind the FFNC-principle will be theoretically reviewed by means of simplified considerations in order to fully grasp its limitations, before discussing its application in FBPAs in section 5.1.2. By taking a closer look onto Fig. 5-1 the general principle of the FFNC can be explained very briefly. Toward low frequencies the propagation delay between input and output is negligible and hence noise ($i_{n,d}$) present at the output of the FB-stage (T_1) is on the one hand transferred via the parallel feedback resistance R_{fp} with 0° phase shift to the input and on the other hand amplified via the HEMT T_3 with a phase shift of 180°. Both signals are summed up at the output terminal by means of the source follower T_2 such that the noise from T_1 is partially cancelled at the output. It adumbrates that the amount of cancellation is on the one hand dependent on the amount of feedback over T_1 and on the other hand on the g_m's of T_2 and T_3. The general trade-offs will be examined more closely analytically at low frequencies.

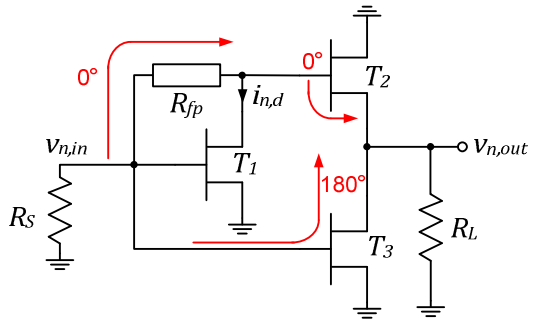


Fig. 5-1: Small-signal circuit of single-ended feedforward noise cancellation concept with common-source parallel feedback stage at the input (noise phase indicated by red arrows)

The input and output noise voltage $\underline{v}_{n,in}$ and $\underline{v}_{n,out}$ for Fig. 5-1, under the assumption of channel noise only, can be expressed as

$$v_{n,in} = -\underline{i}_{n,d} \cdot R_S \tag{5.1}$$

$$\underline{v}_{n,out} = -\underline{i}_{n,d} \cdot R_L\left(g_{m2}\left(R_{fp} + R_S\right) + g_{m3}R_L\right), \tag{5.2}$$

where $\underline{i}_{n,d}$ describes the thermal channel noise current of HEMT T_1. By means of $\underline{v}_{n,out}$ and $\underline{v}_{n,in}$, the noise voltage transfer function can be hence calculated to

$$A_{v,n} = \frac{R_L\left(g_{m2}\left(R_S + R_{fp}\right) - g_{m3}R_S\right)}{R_S(1 + g_{m2}R_L)}. \tag{5.3}$$

In order to cancel out the noise contribution from T_1 and thus obtain $A_{v,n}$= 0, the numerator in (5.3) has to become equal to zero, which is fulfilled for the condition of

$$\frac{g_{m3}}{g_{m2}} = 1 + \frac{R_{fp}}{R_S}. \tag{5.4}$$

As can be seen from (5.4), the noise cancellation of T_1's channel noise is only dependent on the g_m-ratio of the HEMTs T_2 and T_3 in the output adder-stage, the source resistance R_S and the feedback resistor R_{fp}. So by adjusting the device size of T_2 and T_3, the input impedance of the feeback stage can be chosen freely as desired and perfectly matched to the input, whereas the noise of the matching device can be cancelled. The exact same principle for the noise cancellation also counts for the linearity, because any nonlinear signal component undergoes the same signal transfer as the channel noise and is hence cancelled at the output (see also [160]). For the input matched condition of $R_{in} = R_S$, g_{m1} needs to be chosen equal to $1/R_S$, giving e.g. a g_{m1} of 20 mS for 50 Ω.

Left out so far are the signal considerations. The general signal voltage gain A_v from the input to the output of the FFNC-stage can be determined in a similar way from Fig. 5-1 as the noise transfer function and results in

$$A_v = -\frac{\left(\left(g_{m1}R_{fp} - 1\right)g_{m2} + g_{m3}\right)R_L}{1 + g_{m2}R_L}. \tag{5.5}$$

Equation (5.5) demonstrates that the signals traveling along the T_1, T_2- and T_3-path add in-phase at the output. T_3 reveals to be the major contributor boosting the voltage gain, whereas T_2 as source follower has only negligible impact on the overall gain, especially for very large R_L.

5.1.2 FFNC in FBPAs

For a possible improvement of the noise performance in FBPAs, the trade-offs of the FFNC-concept will be reviewed with respect to output power in the following. All of the investigations undertaken in 5.1.1 are only true for low frequencies, since all reactive elements of the HEMTs have been neglected up to now, which is sufficient to gain a very general understanding of the FFNC-principle at the beginning. As soon as the input frequency increases, T_3 starts to capacitively load the input. In order to minimize the loading and keep the input matching over a large frequency range constant, T_3 needs to be sized small compared to T_1. With respect to the noise cancellation condition from (5.4) in contrast, T_3 needs to be sized $\left(1 + R_{fp}/R_S\right)$-times larger than T_2, which in turn leads to either a high amount of feedback over T_1 or a very small device size for T_2. The former leads to a reduction in gain whereas the latter limits the maximum power handling capability of the PA and thus limits the maximum output power delivered to the load. Contrarily, if T_2 and T_3 become very large, their noise contribution starts to dominate over the noise from the feedback stage at the output and the FFNC-concept be-

comes useless. Moreover, the output impedance, which is mainly determined by the source follower, increases with increasing device size due to the low output impedance of T_2, which is proportional to $1/g_m$. Transferred to GaN-technology this means that a g_{m2} for a 50 Ω output load has to be equal to 20 mS, which leads under the assumption of 330 mS/mm for the 0.25µm GaN technology to a device size of $W_{G,T2}$ = 60 µm (e.g. 2×30µm). Furthermore, such a small device restricts the maximum device size of the $\left(1 + R_{fp}/R_S\right)$-times larger power device T_3 to values for $W_{G,T3}$ of around 0.2 mm to 0.5 mm. Unfortunately delivers a 0.5 mm GaN device only a maximum output power of roughly 1 W, assuming an approximate power density of 2 W/mm in broadband PA designs. Therefore, implementation of the proposed FFNC-concept in 0.25µm GaN technology suffers from limited output power under a 50 Ω environment and would thus not comply with the given specifications in Table 1-1. It needs to be mentioned that all of these matching and output power considerations become more stringent, when the frequency of operation increases and the input and output capacitances start to play a major role. Out of the limited time and the basic limitations in output power of the FFNC-concept, analytical frequency-dependent expressions were not derived and are not within the scope of this work.

Completely neglegted in the power considerations so far is the voltage-swing limitation of the output-stage, formed by T_2 and T_3. The maximum rail-to-rail voltage is limited to V_{DD} instead of the maximum swing of $2 \cdot V_{DD}$, as in ideal class A PAs biased with an RF-choke. This in turn reduces the output power by 6 dB in order to maintain operation of T_2 in saturation. One remedy against the reduced signal swing would be to bias the drain of the source follower at $2 \cdot V_{DD}$, which would come at the cost of increased power dissipation. All of these aspects, which need to be followed to make the FFNC-concept work, contradict with the goal of maximizing output power in a FBPA design and are hence only suited for LNA designs.

5.1.3 Key Findings

After a short review of the general feedforward noise-cancellation concept (FFNC), which was first proposed by Bruccoleri *et al.* in [160] for CMOS LNAs, the applicability of the FFNC-concept to FBPAs in GaN technology has been assessed. Based on the much smaller required device sizes of the output combining stage (T_2, T_3) to perfectly cancel the channel noise of the feedback matching device at the output, the maximum output power is strictly limited. By chosing larger device sizes for T_2, T_3 noise cancellation cannot be maintained and the noise contribution of the output stage starts to outweigh the noise contribution from the feedback matching device at the input. Moreover, a large output stage leads to significant bandwidth and thus matching problems at the input, since the input capacitance of T_3 becomes a major contributor to the overall input capacitance of the whole PA. Based on these simple considerations, the concept of FFNC is not deemed to be a proper candidate and is thus not further taken into account for the implementation of GaN wideband PAs.

5.2 Active Gate-Line Termination in TWAs

As was presented in chapter 3.4.3, the minimum low frequency NF in a TWA without capacitively coupled gates is limited by the gate-termination resistor R_{GT}. It is thus worth to investigate if a substitution of R_{GT} by any active circuitry, which exhibits a matched input impedance to the gate-line but introduces less noise, leads to an improvement in the low frequency NF. These kinds of circuits are often referenced as active cold loads (ACL) in the common literature, since they provide a load impedance which is "colder" than a corresponding resistor at a certain temperature. The first active cold load (ACL) was presented by Frater and Williams in 1981 [91]. Therein, a common-source GaAs-FET with series inductive feedback (L_S) was used to synthesize a resistive load which exhibits lower input noise than an equivalent ohmic resistor. By making use of the impedance transformation of L_S to the input, a frequency independent feedback resistor can be seen. In this way the difference in impedance necessary for a complex conjugate match and noise match can be minimized. Thus the input becomes matched to the source resistance but provides minimum noise at the same time. Since this ACL approach is due to L_S only suited for narrow-band designs, three different solutions for the implementation of a broadband ACL are reviewed in the following and their theoretical trade-offs compared.

For the noise analysis, the PRC-model of Van der Ziel/Pucel is considered for modeling the channel noise ($\underline{i}_{n,d}$) and induced-gate noise ($\underline{i}_{n,g}$) of the HEMT. All other resistors incorporate thermal noise of the form $4kT_0\Delta f R_x$ only. It is important to recall that only noise available at the input of the ACL is of interest and not the equivalent input referred noise of the ACL. Latter misleadingly takes the output noise transferred to the input into account, which is the general approach taken to separate a noisy circuit into its equivalent input noise sources and the noiseless circuit itself (as e.g. for the computation of the NF of a circuit). In terms of the ACL only the termination impedance and its corresponding available input noise power influence the upstream circuitry. Latter can be computed by the total resulting noise voltage at the input ($\underline{v}_{n,tot}$) and the related input impedance ($\underline{Z}_{IN,x}$) of the circuit, as described below in (5.6).

$$P_{n,tot} = \frac{\overline{\left|\underline{v}_{n,tot}\right|^2}}{4 \cdot Re\{\underline{Z}_{IN,x}\}}, \tag{5.6}$$

For a detailed derivation of the available noise power at the input and its noise transfer functions see also [161].

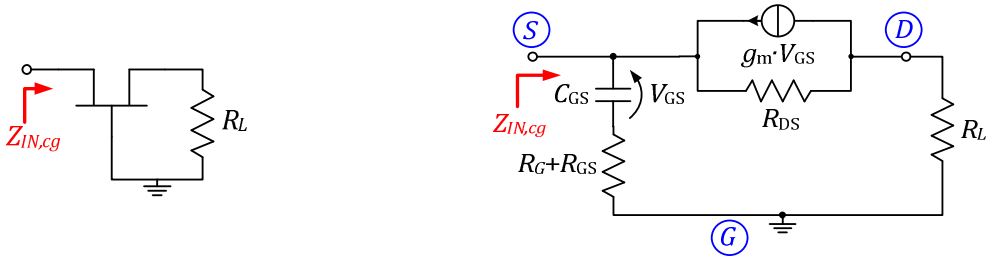
5.2.1 Common-Gate ACL

One of the best and simplest concepts to realize a constant resistance over large frequencies is based on a single common-gate (CG) stage. Fig. 5-2 depicts a simple CG-HEMT terminated at its drain with the resistive load R_L. According to Fig. 5-2 (b) the input impedance of the CG-HEMT can be computed to

$$\underline{Z}_{IN,cg} = \frac{R_L + R_{\mathrm{DS}} + j\omega C_{\mathrm{GS}}(R_{\mathrm{GS}} + R_{\mathrm{G}})(R_L + R_{\mathrm{DS}})}{1 + g_m R_{\mathrm{DS}} + j\omega C_{\mathrm{GS}}(R_{\mathrm{GS}} + R_{\mathrm{G}} + R_L + R_{\mathrm{DS}})}. \tag{5.7}$$

Under the in general valid assumption that $R_{\mathrm{DS}} \gg R_{\mathrm{GS}} + R_{\mathrm{G}} + R_L$ for an ACL with a $Re\{\underline{Z}_{IN,cg}\} = 50\ \Omega$ and furthermore with $f_T = g_m/2\pi C_{\mathrm{GS}} \gg f$, equation (5.7) can be approximated by

$$\underline{Z}_{IN,cg} \approx \frac{1}{g_m}. \tag{5.8}$$



(a) (b)

Fig. 5-2: (a) ACL in common-gate configuration and (b) its corresponding simplified equivalent small-signal circuit

Equation (5.8) shows that the input impedance of a CG-HEMT is only proportional to the reciprocal of g_m and is thus mainly resistive for moderate frequencies ($f \ll f_T$). By proper selection of the device size and hence g_m the load resistance can be synthesized as desired.

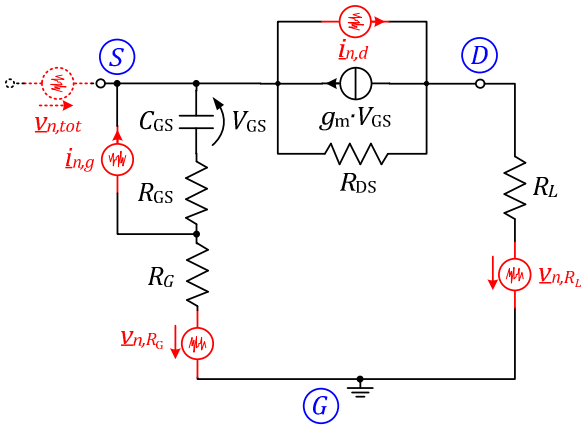


Fig. 5-3: Noisy small-signal equivalent circuit of ACL in CG-configuration (CG)

The total input noise voltage according to Fig. 5-3 at the input of the CG-HEMT can be computed to

$$\begin{aligned}\langle \underline{v}_{n,tot}{}^2 \rangle = \left|\frac{\underline{Z}_{IN,cg}}{R_L + R_{DS}}\right|^2 \Bigg[&\langle \underline{v}_{n,R_L}{}^2 \rangle + \left|\frac{R_L + R_{DS}}{\underline{Z}_{IN,cg}} - 1\right|^2 \langle \underline{v}_{n,R_G}{}^2 \rangle \\ &+ R_{DS}{}^2 \langle \underline{i}_{n,d}{}^2 \rangle + \left|\frac{g_m R_{DS} R_G - (R_L + R_{DS})(1 + j\omega C_{GS} R_{GS})}{1 + j\omega C_{GS}(R_{GS} + R_G)}\right|^2 \cdot \langle \underline{i}_{n,g}{}^2 \rangle \\ &+ 2 \cdot Re\left\{ \underline{c} \cdot R_{DS} \left(\frac{g_m R_{DS} R_G - (R_L + R_{DS})(1 + j\omega C_{GS} R_{GS})}{1 + j\omega C_{GS}(R_{GS} + R_G)} \right)^* \right\} \sqrt{\langle \underline{i}_{n,g}{}^2 \rangle \langle \underline{i}_{n,d}{}^2 \rangle} \Bigg],\end{aligned} \tag{5.9}$$

where $\underline{Z}_{IN,cg}$ is the input impedance from (5.7) and $\langle \underline{i}_{n,g}{}^2 \rangle$, $\langle \underline{i}_{n,d}{}^2 \rangle$ and $\underline{c}$ Pucel's noise parameters from (2.10)-(2.12). Finale insertion of (5.7) and (2.10)-(2.12) into (5.9) and further into (5.6) gives

$$P_{n,cg} = k_B T_0 \Delta f \cdot \frac{1}{Re\{\underline{Z}_{IN,cg}\}} \left| \frac{\underline{Z}_{IN,cg}}{R_L + R_{\mathrm{DS}}} \right|^2 \cdot \left[R_L + \left| \frac{R_L + R_{\mathrm{DS}}}{\underline{Z}_{IN,cg}} - 1 \right|^2 \cdot R_{\mathrm{G}} \right.$$

$$+ g_m {R_{\mathrm{DS}}}^2 P + \left| \frac{g_m R_{\mathrm{DS}} R_{\mathrm{G}} - (R_L + R_{\mathrm{DS}})(1 + j\omega C_{\mathrm{GS}} R_{\mathrm{GS}})}{1 + j\omega C_{\mathrm{GS}}(R_{\mathrm{GS}} + R_{\mathrm{G}})} \right|^2 \cdot \frac{(\omega C_{\mathrm{GS}})^2}{g_m} R \qquad (5.10)$$

$$\left. + 2\omega C_{\mathrm{GS}} \cdot Re\left\{ \underline{c} \cdot R_{\mathrm{DS}} \left(\frac{g_m R_{\mathrm{DS}} R_{\mathrm{G}} - (R_L + R_{\mathrm{DS}})(1 + j\omega C_{\mathrm{GS}} R_{\mathrm{GS}})}{1 + j\omega C_{\mathrm{GS}}(R_{\mathrm{GS}} + R_{\mathrm{G}})} \right)^* \right\} \sqrt{RP} \right].$$

5.2.2 Common-Source ACL with Series Inductive Feedback

Another ACL concept is based on series inductive feedback and was first applied by Frater and Williams in 1981 [91]. The basic idea behind the additional series inductances L_{SF} in the source path and L_{GF} in the gate path is founded in the improved matching performance to a source resistance R_{S}. On the one hand, L_{SF} transforms into a frequency independent and noiseless real-part at the input whereas L_{GF} enables the compensation of the capacitive imaginary-part from C_{GS}. In this way optimum noise matching and gain matching can be achieved at the same time, as was shown in 1974 by A. Anastassiou *et al.* [84, 85] and is still today one of the most applied concepts in narrow-band LNAs.

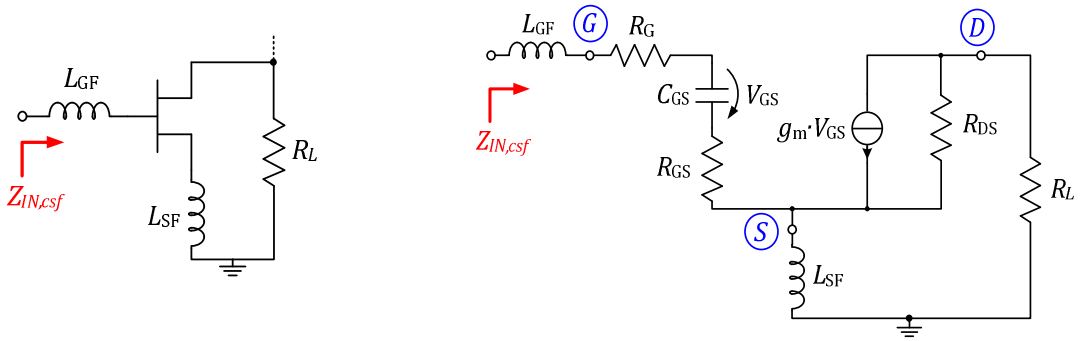


Fig. 5-4: (a) ACL in common-source configuration with series inductive feedback and (b) its corresponding simplified equivalent small-signal circuit

The corresponding input impedance of the CS-HEMT with series inductive feedback can be obtained from Fig. 5-4 (b) and equals

$$Z_{IN,csf} = R_{\mathrm{G}} + R_{\mathrm{GS}} + g_m \frac{L_{SF}}{C_{\mathrm{GS}}} + j\left(\omega(L_{SF} + L_{GF}) - \frac{1}{\omega C_{\mathrm{GS}}}\right) \tag{5.11}$$

$$+ \frac{(\omega L_{SF})^2 - g_m \frac{L_{SF}}{C_{GS}}(R_L + j\omega L_{SF})}{R_L + R_{\mathrm{DS}} + j\omega L_{SF}}.$$

At moderate frequencies and for the case of $R_{\mathrm{DS}} \gg R_L + j\omega L_{SF}$, (5.15) can be simplified to

$$Z_{IN,csf} \approx R_{\mathrm{G}} + R_{\mathrm{GS}} + g_m \frac{L_{SF}}{C_{\mathrm{GS}}} + j\left(\omega(L_{SF} + L_{GF}) - \frac{1}{\omega C_{\mathrm{GS}}}\right). \tag{5.12}$$

By taking a closer look onto (5.12) it can be inferred that the real-part of $Z_{IN,csf}$ is frequency independent and can be tuned on the one hand by the device size ($R_{\mathrm{G}}, R_{\mathrm{GS}}, g_m, C_{\mathrm{GS}}$) and on the other hand by the series inductance L_{SF}. The imaginary-part in contrast is strongly frequency dependent and exhibits a capacitive behavior in the low frequency range ($\omega(L_{SF} + L_{GF}) < 1/\omega C_{\mathrm{GS}}$) and an inductive behavior in the high frequency range ($\omega(L_{SF} + L_{GF}) > 1/\omega C_{\mathrm{GS}}$).

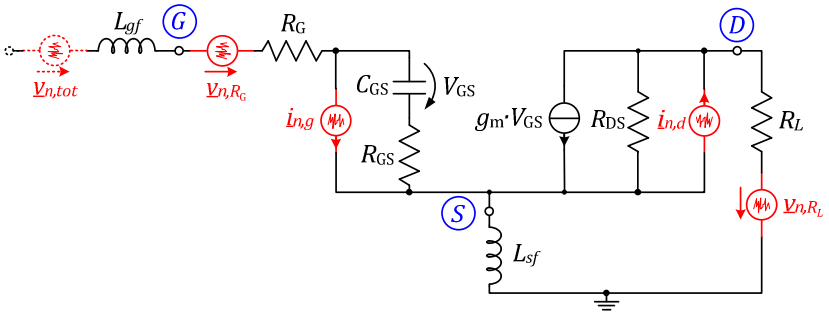


Fig. 5-5: Noisy small-signal equivalent circuit of ACL in CS-configuration with series inductive feedback (CS-SIF)

The total input noise voltage spectral density at the input of the CS-HEMT with series inductive feedback can be computed from Fig. 5-5 to

$$\langle \underline{v}_{n,tot}{}^2 \rangle = \langle \underline{v}_{n,R_G}{}^2 \rangle + \frac{(\omega L_{SF})^2}{(R_L + R_{\mathrm{DS}})^2 + (\omega L_{SF})^2}\left[\langle \underline{v}_{n,R_L}{}^2 \rangle + \langle i_{n,d}{}^2 \rangle \cdot R_{\mathrm{DS}}{}^2\right]$$

$$+ \left| R_{\mathrm{GS}} + g_m \frac{L_{SF}}{C_{\mathrm{GS}}} \frac{R_{\mathrm{DS}}}{R_{\mathrm{DS}} + R_L + j\omega L_{SF}} + \frac{1}{j\omega C_{\mathrm{GS}}} \right|^2 \cdot \langle \underline{i}_{n,g}{}^2 \rangle \tag{5.13}$$

$$+ 2Re\left\{ \underline{c} \cdot \frac{j\omega L_{SF} R_{\mathrm{DS}}}{R_{\mathrm{DS}} + R_L + j\omega L_{SF}} \left(R_{\mathrm{GS}} + g_m \frac{L_{SF}}{C_{\mathrm{GS}}} \frac{R_{\mathrm{DS}}}{R_{\mathrm{DS}} + R_L + j\omega L_{SF}} + \frac{1}{j\omega C_{\mathrm{GS}}} \right)^* \right\} \sqrt{\langle \underline{i}_{n,g}{}^2 \rangle \langle \underline{i}_{n,d}{}^2 \rangle} \Bigg]$$

where $\langle \underline{i}_{n,g}{}^2 \rangle$, $\langle \underline{i}_{n,d}{}^2 \rangle$ and $\underline{c}$ are again Pucel's noise parameters from (2.10)-(2.12). Finale insertion of (5.13) and (2.10)-(2.12) into (5.6) gives

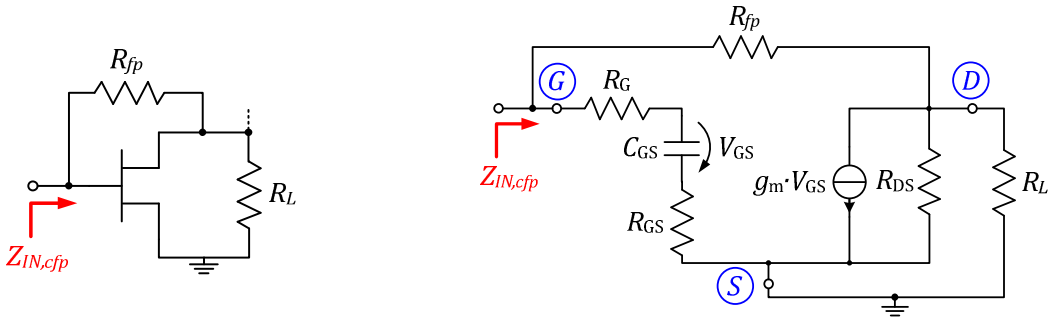
$$P_{n,csf} = kT_0\Delta f \cdot \frac{1}{Re\{\underline{Z}_{IN,csf}\}}\left[R_G + \frac{(\omega L_{SF})^2}{(R_L + R_{DS})^2 + (\omega L_{SF})^2}\left[R_L + g_m {R_{DS}}^2 P\right]\right.$$

$$+\left|R_{GS} + g_m \frac{L_{SF}}{C_{GS}} \frac{R_{DS}}{R_{DS} + R_L + j\omega L_{SF}} + \frac{1}{j\omega C_{GS}}\right|^2 \cdot \frac{(\omega C_{GS})^2}{g_m} R \tag{5.14}$$

$$\left.+2Re\left\{\underline{c} \cdot \frac{j\omega L_{SF} R_{DS}}{R_{DS} + R_L + j\omega L_{SF}}\left(R_{GS} + g_m \frac{L_{SF}}{C_{GS}} \frac{R_{DS}}{R_{DS} + R_L + j\omega L_{SF}} + \frac{1}{j\omega C_{GS}}\right)^*\right\}\sqrt{PR}\right].$$

5.2.3 Common-Source ACL with Parallel Resistive Feedback

Instead of applying inductive series feedback, parallel resistive feedback shows the advantage of decent matching over much larger bandwidths especially down to DC (as shown in 3.2.1), where the series inductive compensation doesnot have any effect. Due to the parallel resistive feeback, the input capacitance C_{GS} is masked at low frequencies and thus the input impedance mainly resistive. The input noise characteristic of this topology is unfortunately slightly higher than for the series inductive feedback, since the feedback resistor R_{fp} contributes additional thermal noise. Nevertheless, it will be shown in this section that the available input noise is still significantly lower than in a resistor, which provides the same load resistance as the ACL.



(a) (b)

Fig. 5-6: (a) ACL in common-source configuration with parallel resistive feedback and (b) its corresponding simplified equivalent small-signal circuit

From Fig. 5-6 (b) the corresponding input impedance of the CS-HEMT with parallel resistive feedback can be computed to

$$\underline{Z}_{IN,cfp} = \frac{R_a + R_{fp} + j\omega C_{GS}(R_{GS} + R_G)(R_A + R_{fp})}{1 + g_m R_a + j\omega C_{GS}(R_{GS} + R_G + R_A + R_{fp})}, \tag{5.15}$$

where $R_A = R_{DS}||R_L$. Further separation of (5.15) into its real- and imaginary-part yields

$$Re\{Z_{IN,cfp}\} = \frac{(R_A + R_{fp})[1 + g_m R_A + (\omega C_{GS})^2 (R_{GS} + R_G)(R_{GS} + R_G + R_A + R_{fp})]}{(1 + g_m R_A)^2 + \left(\omega C_{GS}(R_{GS} + R_G + R_A + R_{fp})\right)^2} \tag{5.16}$$

$$Im\{Z_{IN,cfp}\} = \frac{\omega C_{GS}(R_a + R_{fp})[g_m R_A (R_{GS} + R_G) - (R_A + R_{fp})]}{(1 + g_m R_A)^2 + \left(\omega C_{GS}(R_{GS} + R_G + R_A + R_{fp})\right)^2}. \tag{5.17}$$

From (5.17) it becomes apparent that the imaginary-part is equal to zero at DC and increases with frequency. Since in general the numerator term $g_m R_A (R_{GS} + R_G)$ is smaller than $(R_A + R_{fp})$, the input impedance shows a capacitive behavior, which exhibits its maximum at

$$f_{res} = \frac{1 + g_m R_A}{2\pi(R_{GS} + R_G + R_A + R_{fp})}. \tag{5.18}$$

Above this frequency the imaginary-part tends back to zero again with increasing frequency. Equation (5.16) reveals that the real-part is also frequency dependent and strives at DC to

$$Re\{\underline{Z}_{IN,cfp}\}\big|_{f=0} = \frac{R_A + R_{fp}}{1 + g_m R_A} \tag{5.19}$$

and for very high frequencies to

$$Re\{\underline{Z}_{IN,cfp}\}\big|_{f=\infty} = \frac{(R_A + R_{fp})(R_{GS} + R_G)}{R_{GS} + R_G + R_A + R_{fp}}, \tag{5.20}$$

which can be very well approximated by $R_{GS} + R_G$ based on the fact that usually $R_A + R_{fp} \gg R_{GS} + R_G$. The optimum input match at low frequencies is therefore strongly dependent on the ratio between R_{fp} and R_L and can be thus very well adapted to any desired resistance value over a much larger range than e.g. in the CG-ACL.

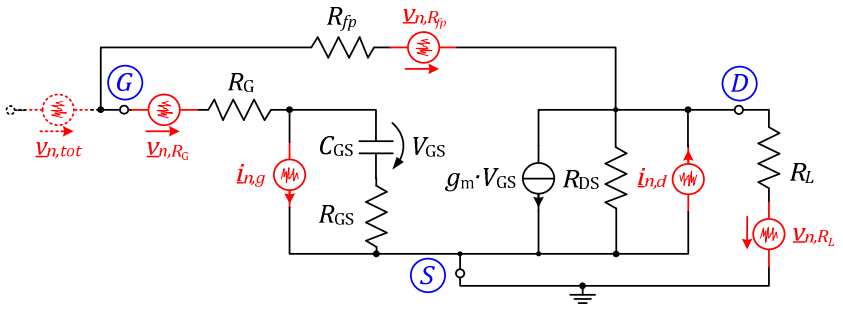


Fig. 5-7: Noisy small-signal equivalent circuit of ACL in CS-configuration with parallel resistive feedback (CS-PRF)

According to Fig. 5-7, the total input noise voltage sprectral density of the CS-HEMT with parallel resistive feedback can be calculated to

$$\langle \underline{v}_{n,tot}{}^2 \rangle = \left| \frac{\underline{Z}_{IN,cfp}}{R_A + R_{fp}} \right|^2 \left[\left(\frac{R_A}{R_L} \right)^2 \langle \underline{v}_{n,R_L}{}^2 \rangle + \langle \underline{v}_{n,R_{fp}}{}^2 \rangle + \left| \frac{R_A + R_{fp}}{\underline{Z}_{IN,cfp}} - 1 \right|^2 \langle \underline{v}_{n,R_G}{}^2 \rangle \right.$$

$$+ R_A{}^2 \langle \underline{i}_{n,d}{}^2 \rangle \cdot \left| \frac{g_m R_A R_{\mathrm{G}} - (R_A + R_{fp})(1 + j\omega C_{\mathrm{GS}} R_{\mathrm{GS}})}{1 + j\omega C_{\mathrm{GS}}(R_{\mathrm{GS}} + R_{\mathrm{G}})} \right|^2 \langle \underline{i}_{n,g}{}^2 \rangle \tag{5.21}$$

$$\left. + 2 \cdot Re \left\{ \underline{c} \cdot R_A \left(\frac{g_m R_A R_{\mathrm{G}} - (R_A + R_{fp})(1 + j\omega C_{\mathrm{GS}} R_{\mathrm{GS}})}{1 + j\omega C_{\mathrm{GS}}(R_{\mathrm{GS}} + R_{\mathrm{G}})} \right)^* \right\} \sqrt{\langle \underline{i}_{n,g}{}^2 \rangle \langle \underline{i}_{n,d}{}^2 \rangle} \right]$$

where $\langle \underline{i}_{n,g}{}^2 \rangle$, $\langle \underline{i}_{n,d}{}^2 \rangle$ and $\underline{c}$ are again Pucel's noise parameters from (2.10)-(2.12). Finale insertion of (5.13) and (2.10)-(2.12) into (5.6) gives

$$P_{n,cfp} = k_B T_0 \Delta f \cdot \frac{1}{Re\{\underline{Z}_{IN,cfp}\}} \left| \frac{\underline{Z}_{IN,cfp}}{R_A + R_{fp}} \right|^2 \left[\frac{R_A{}^2}{R_L} + R_{fp} + \left| \frac{R_A + R_{fp}}{\underline{Z}_{IN,cfp}} - 1 \right|^2 \cdot R_{\mathrm{G}} \right.$$

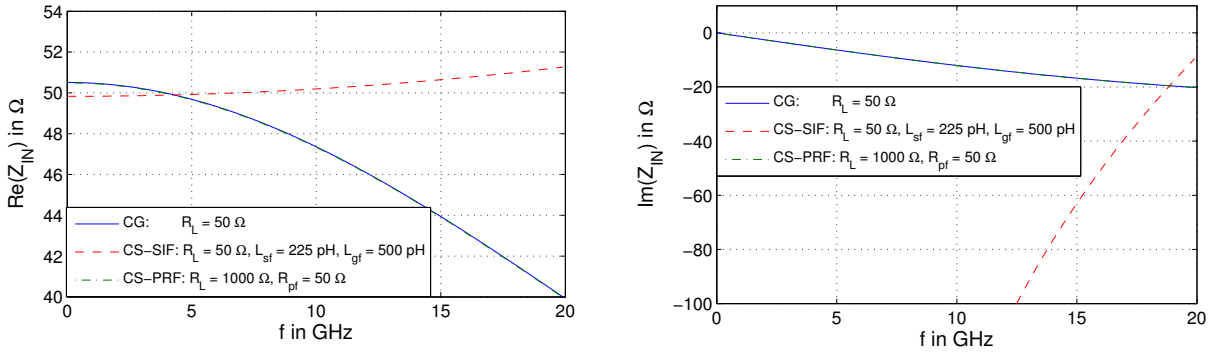
$$+ g_m R_A{}^2 P + \left| \frac{g_m R_A R_{\mathrm{G}} - (R_A + R_{fp})(1 + j\omega C_{\mathrm{GS}} R_{\mathrm{GS}})}{1 + j\omega C_{\mathrm{GS}}(R_{\mathrm{GS}} + R_{\mathrm{G}})} \right|^2 \cdot \frac{(\omega C_{\mathrm{GS}})^2}{g_m} R \tag{5.22}$$

$$\left. + 2\omega C_{\mathrm{GS}} \cdot Re \left\{ \underline{c} \cdot R_A \left(\frac{g_m R_A R_{\mathrm{G}} - (R_A + R_{fp})(1 + j\omega C_{\mathrm{GS}} R_{\mathrm{GS}})}{1 + j\omega C_{\mathrm{GS}}(R_{\mathrm{GS}} + R_{\mathrm{G}})} \right)^* \right\} \sqrt{PR} \right]$$

for the available noise power at the input of the CS-PRF ACL.

5.2.4 Comparison of ACL Concepts

Fig. 5-8 depicts the real- and imaginary-parts of the input impedance for the three ACL concepts presented in the preceding sections 5.2.1 to 5.2.3. In order to retain a meaningful comparison between the three concepts, the device size, bias point and thus the dissipated power are maintained for each topology. Merely the feedback values (R_{fp}, L_{GF}, L_{SF}) and load impedances (R_L) were adjusted to end up in a good 50 Ω match from DC to 20 GHz. Out of this reason, the CG-HEMT proved to be the limiting factor in device size, because the $Re\{Z_{IN,cg}\}$ is proportional to $1/g_m$, which gives for a 2×35µm GaN HEMT biased at V_{DS} = 10 V and I_{DS} = 50 mA/mm with a g_m of 19.8 mS a real-part close to 50 Ω. As can be seen from Fig. 5-8 (a), the CS-HEMT with series inductive feedback (CS-SIF) provides an almost frequency independent real-part as derived in (5.11) and (5.12), whereas the CG-HEMT (CG) and the CS-HEMT with parallel resistive feedback (CS-PRF) exhibit a noticeable decay over frequency. The imaginary-part in Fig. 5-8 (b) in constrast shows a contrary behavior, where the CG and CS-PRF demonstrate the lowest input reactance, followed by the CS-HEMT with PRF. The CS-SIF shows to be purely capacitive at DC and becomes only fully compensated at 20 GHz based on the series inductances in the gate and source path. The exact superposition of the CG and CS-PRF real- and imaginary-parts is founded in the simplification of C_{GD} = C_{DS} = 0 F, which makes both of them only dependent on frequency via C_{GS}.



(a) (b)

Fig. 5-8: (a) $Re\{Z_{IN}\}$ and (b) $Im\{Z_{IN}\}$ of a 2×35µm GaN HEMT in CG-, CS-SIF and CS-PRF configuration. (Note: CS-SIF and CS-PRF curves are congruent in (a) and (b))

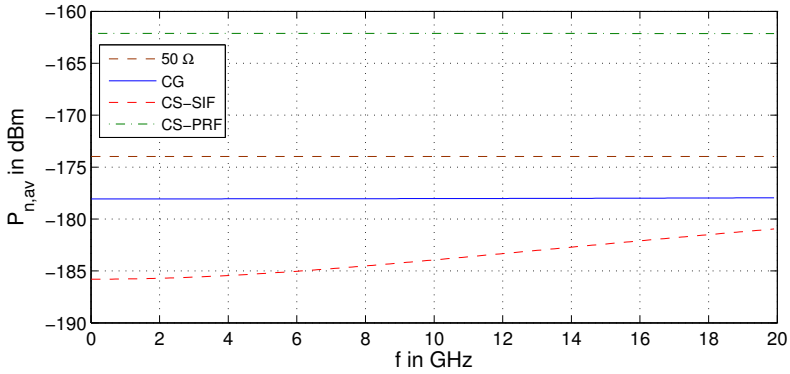


Fig. 5-9: $P_{n,av}$ of a 2×35µm GaN HEMT in CG-, CS-SIF and CS-PRF configuration with V_{DS} = 10 V and I_{DS} = 50 mA/mm

The available noise power at the input of the three ACLs according to the equations derived in (5.10), (5.14) and (5.22) is plotted in Fig. 5-9 above. The PRC-parameters for the noise model were computed at DC according to the conversion formulas derived in (2.26)-(2.28) from Pospieszalski´s equivalent gate and drain noise temperatures (T_G, T_D), which were taken from the IAF small-signal model. The frequency dependence of the PRC-parameters arising from the mathematical conversion between Pospieszalski´s and Pucel´s model are neglected here for simplicity (see section 2.2.3). Accordingly, P, R and $\underline{c}$ of a 2×35µm GaN HEMT at V_{DS} = 10 V and I_{DS} = 50 mA/mm can be determined to the values given in Table 6-1 below. The low values for R and $\underline{c}$ result from the low frequency dependence of the small 2×35µm device in the regarded low frequency range.

Table 5-1: Recalculated PRC-parameters of a 2×50µm GaN HEMT

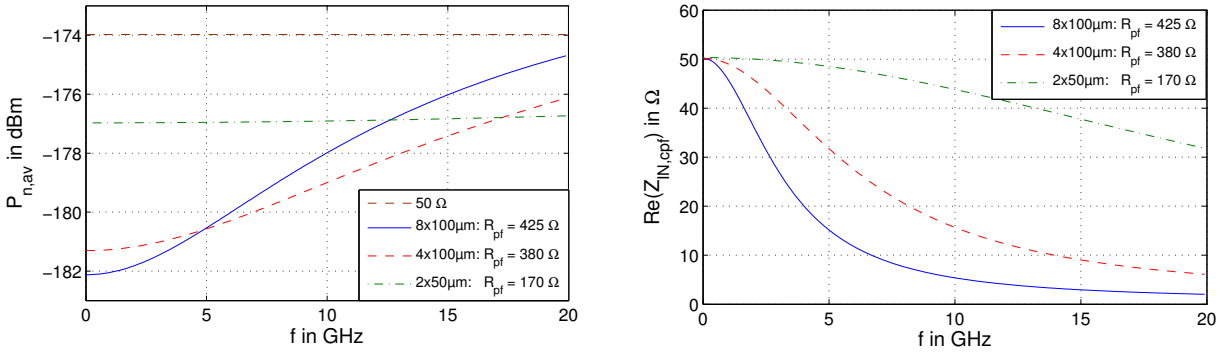
P	R	$\underline{c}$
0.44	0.022	$-j0.23$

The resulting available input noise power $P_{n,av}$ of the ACLs with a 2×35µm GaN HEMT in CG-, CS-SIF- and CS-PRF-configuration is plotted in Fig. 5-9. The brown dotted line gives the reference of a 50 Ω resistor at

T_0 = 290 K of approximately -174 dBm/Hz. Best noise performance for a 2×35µm device provides the CS-SIF topology, followed by the CG topology. Only the CS-PRF topology exhibits a noise behavior inferior to the one of a 50 Ω resistor. The reason for this is rooted in the low gain of the small 2×35µm device. By taking a closer look at $P_{n,cfp}$ at DC, (5.22) reduces to

$$P_{n,cfp}\big|_{f=0} = \frac{k_B T_0 \Delta f}{(1+g_m R_A)(R_{fp}+R_A)}\left[\frac{{R_A}^2}{R_L} + R_{fp} + g_m {R_A}^2 (g_m R_G + P)\right]. \tag{5.23}$$

Equation (5.23) illustrates that under the presumption of a constant input impedance $Z_{IN,cfp}$ and load resistance R_L that the device size (g_m, R_{DS}) and the feedback resistance R_{fp} mainly determine the absolute noise power present at the input. Since the device size W_G is proportional to g_m and to $1/R_{DS}$, the term $g_m R_A$ stays almost constant, whereas ${R_A}^2$ drops faster than R_{fp} needs to be increased in order to keep $Z_{IN,cfp}$ constant. According to the latter relationship the noise contribution originating from R_{fp} increases not as fast as ${R_A}^2$ decays with device size, so the overall available input noise decreases. It is furthermore helpful to choose $R_L \gg R_{DS}$ in order to obtain $R_A \approx R_{DS}$ and thus make R_A reciprocal proportional to W_G. In summary, for the same input impedance a larger device size helps to reduce the available input noise power at DC, as Fig. 5-10 (a) illustrates. For the 8×100µm device, $P_{n,cfp}$ is smaller than -182 dBm/Hz ($T_{n,cfp} \approx 45$ K) in the frequency range below 2 GHz and further reduces the available input noise power by around 5 dB opposed to the 2×50µm device.



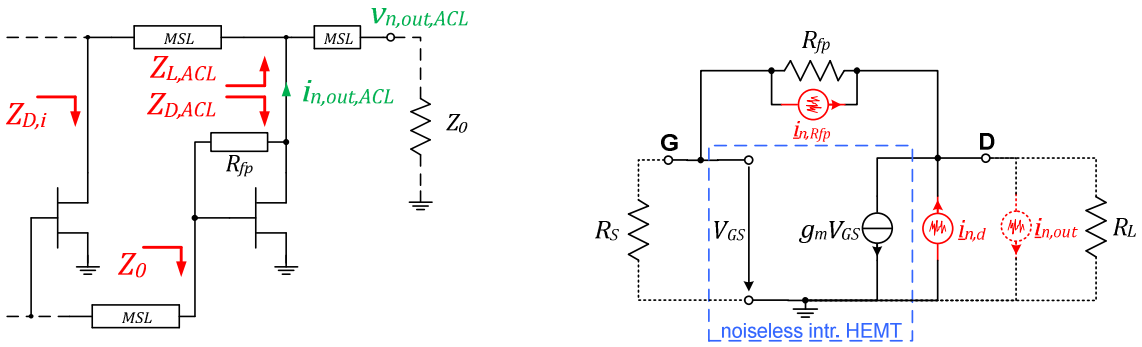
(a) (b)

Fig. 5-10: $P_{n,av}$ of a 2×50µm, 4×100µm and 8×100µm GaN HEMT CS-PRF configuration for V_{DS} = 10 V and I_{DS} = 50 mA/mm

Unfortunately, choosing a larger device comes at the cost of a much stronger frequency dependence, as Fig. 5-10 shows. Dependent on the type of application, this might not necessarily be a "show-stopper", as will be shown for the application of ACLs in TWAs in the next two sections 5.2.5 and 5.2.6.

5.2.5 ACL Termination as Last Stage in TWAs

To end up in a definite statement about the usefulness of the ACL concept in TWAs, the just gained information about input matching and noise suppression dependent on the amount of feedback can now be transferred to the TWA structure. As Fig. 5-11 sketches, replacement of the last stage in a TWA by the ACL with a parallel resistive feedback over a common-source HEMT (CS-PRF) allows to terminate the gate-line properly in its characteristic impedance. This concept has been also patented in the course of this work by K. W. Kobayashi in 2012 [162].



(a) (b)

Fig. 5-11: Schematic of (a) low-frequency noise cancellation concept with an ACL in CS-PRF configuration as last stage in a TWA and (b) simplified equivalent output noise representation of CS-PRF stage

Silently neglected is the slight difference in the design of the last MSL-section in the gate-line in (a). By properly adjusting the characteristic impedance and length of the last gate-MSL section the amount of reflections from the CS-PRF-stage can be further minimized, which will not be addressed any further within this section. For the following theoretical analysis of the noise contribution of the ACL to the overall TWA noise, the low frequency approximation $\beta_G l_G = \beta_D l_D \ll 1$ is made, which is a valid assumption for assessing the low frequency noise improvement by using an ACL as last stage.

The equivalent output noise representation of the CS-PRF-stage for low frequencies is depicted in Fig. 5-11 (b). It is important to bear in mind that the noise current of R_{fp} is located between the input and ouput and therefore is fully correlated. Accordingly, the overall short-circuited output noise current can be therefrom determined to

$$i_{n,out} = \sqrt{\frac{4k_B T\Delta f}{R_{fp}}\left(1+\left(g_m-\frac{1}{R_{fp}}\right)\frac{R_S R_{fp}}{R_S+R_{fp}}\right)^2 + 4k_B T\Delta f\, g_m P.} \tag{5.24}$$

Insertion of the CS-PRF-stage as the last stage in a TWA, as depicted in Fig. 5-11 (a), changes the general impedance environment of the ACL. The load impedance $Z_{L,ACL}$ seen by the ACL is now equal to

$$Z_{L,ACL} = \frac{Z_0}{2} \,||\, \frac{Z_{\mathrm{D},i}}{N-1}, \tag{5.25}$$

where $Z_{\mathrm{D},i}$ describes the impedance seen into each drain terminal of the preceding N-1 stages. $Z_{\mathrm{D},i}$ can be calculated by

$$Z_{\mathrm{D},i} = \frac{1}{g_m}\left(1 + \frac{R_{fp}}{Z_0}\right). \tag{5.26}$$

Insertion of (5.26) into (5.25) yields

$$Z_{L,ACL} = \frac{1}{\frac{2}{Z_0} + \frac{g_m(N-1)}{1 + \frac{R_{fp}}{Z_0}}}. \tag{5.27}$$

Equation (5.27) shows, that the load impedance seen by the ACL is surprisingly also dependent on its own value of the parallel feedback resistor. For $R_{fp} \to \infty\,\Omega$, the output load resistance $Z_{L,ACL}$ strives toward $Z_0/2$, as it is the general case in a conventional UDPA. Since for low frequencies the parallel feedback applies over all N stages of the UPDA, the output noise current $i_{n,out,ACL}$ in Fig. 5-11 (b) needs to incorporate, opposed to the noise current of the single ACL stage from (5.24), now the N-times higher g_m of the whole UPDA, as (5.28) below shows.

$$i_{n,out,ACL} = \sqrt{\frac{4k_BT\Delta f}{R_{fp}}\left|1 + \left(Ng_m - \frac{1}{R_{fp}}\right)\frac{Z_0R_{fp}}{Z_0 + R_{fp}}\right|^2 + 4k_BT\Delta f g_m P}. \tag{5.28}$$

The corresponding output noise power, which is added by the CS-PRF-stage and delivered to the output load Z_0 of the TWA can be furthermore calculated to

$$P_{n,ACL} = \left|i_{n,out,ACL} \cdot \frac{Z_{L,ACL}Z_{\mathrm{D},ACL}}{Z_{L,ACL} + Z_{\mathrm{D},ACL}}\right|^2 \Big/ Re\{Z_0\}. \tag{5.29}$$

$Z_{D,ACL}$ in (5.29) is according to Fig. 5-11 (a) equal to

$$Z_{\mathrm{D},ACL} = \frac{Z_0 + R_{fp}}{1 + g_mZ_0}, \tag{5.30}$$

which gives for $P_{n,ACL}$ in (5.29) the following dependency on the characteristic gate- and drain-line impedance Z_0 and on the parallel feedback resistor R_{fp}.

$$P_{n,ACL} = 4k_BT\Delta f \cdot \frac{\frac{1}{R_{fp}}\left|1 + \left(Ng_m - \frac{1}{R_{fp}}\right)\frac{Z_0R_{fp}}{Z_0 + R_{fp}}\right|^2 + g_mP}{Re\{Z_0\} \cdot \left|\frac{2}{Z_0} + \frac{1 + Ng_mZ_0}{R_{fp} + Z_0}\right|^2} \tag{5.31}$$

The forward power gain transfer function from the input to the output under the same low frequency assumption can be computed to

$$G_{P,f} = \left| \frac{1 - N g_m R_{fp}}{1 + \frac{1}{2}(1 + N g_m Z_0) + \frac{R_{fp}}{Z_0}} \right|^2, \tag{5.32}$$

leading with the aid of the just derived equations (5.31) and (5.32) to the following noise factor of the ACL (F_{ACL}) under the consideration of input and output mismatch.

$$F_{ACL} = 1 + \frac{P_{n,ACL}}{G_{P,f} \cdot k_B T \Delta f}. \tag{5.33}$$

If in a last step also the channel noise ($\underline{i}_{n,d}$) of the preceding N-1 stages is taken into account, the following additional noise power is added to the output

$$\begin{aligned} P_{n,N-1} &= 4 k_B T \Delta f g_m P \cdot \frac{(N-1)}{Re\{Z_0\}} \left| \frac{Z_{D,i} Z_{L,i}}{Z_{D,i} + Z_{L,i}} \right|^2 \\ &= \frac{4 k_B T \Delta f g_m P \cdot (N-1)}{Re\{Z_0\} \cdot \left| 1 + 2\left(1 + \frac{R_{fp}}{Z_0}\right) + g_m Z_0 N \right|^2}, \end{aligned} \tag{5.34}$$

where $Z_{\mathrm{D},i}$ is the same impedance as in (5.26) and $Z_{L,i}$ is the load impedance seen by each of the preceding N-1 stages, which is equal to

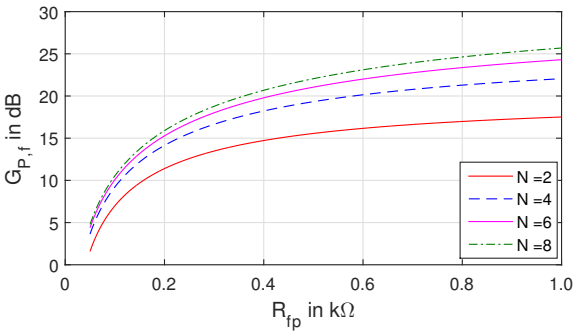
$$\begin{aligned} Z_{L,i} &= \frac{Z_0}{2} || \frac{Z_{\mathrm{D},i}}{N-2} || Z_{\mathrm{D},ACL} \\ &= \frac{Z_0 + R_{fp}}{1 + 2\left(1 + \frac{R_{fp}}{Z_0}\right) + g_m Z_0 (N-1)}. \end{aligned} \tag{5.35}$$

Finally, the overall low frequency noise factor of the TWA with ACL as last stage (F_{TWA}) can be hence calculated to

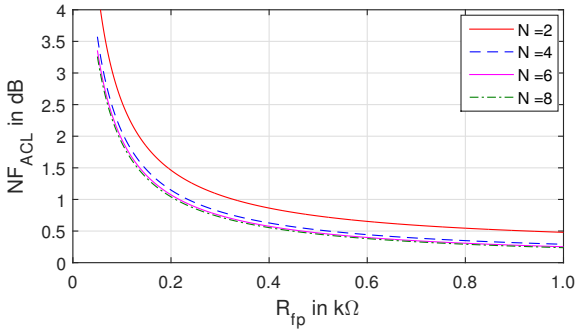
$$F_{TWA} = 1 + \frac{P_{n,ACL} + P_{n,N-1}}{G_{P,f} \cdot k_B T \Delta f}. \tag{5.36}$$

Fig. 5-12 (a) illustrates the corresponding dependence of the power gain G_T on R_{fp} and N with the CS-PRF ACL as last stage in a UDPA, as defined in (5.32). For increasing R_{fp} values and with a rising number of stages, G_T converges to its maximum gain value for $R_{fp} = \infty\ \Omega$. The graphs in Fig. 5-12 (b) and (c) show the resulting NF dependence on R_{fp} and N according to (5.33) and (5.36). The noise contribution of the ACL only is plotted

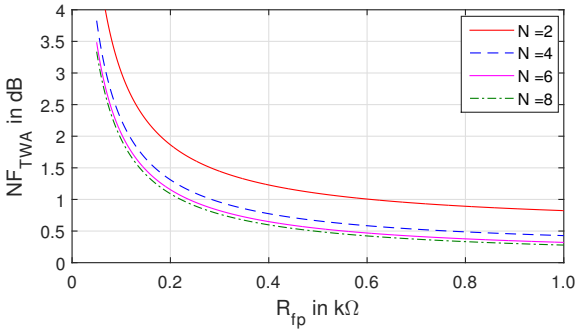
in (b), assuming that only the channel ($P = 1$) and R_{fp} contribute to the output noise and the rest of the HEMTs in the UDPA are noiseless, whereas in (c) the channel noise contribution of the preceding N-1 stages is additionally taken into account (see also chapter 3.4.3). From both figures (b) and (c), it can be derived that with increasing number of stages N and for larger values of R_{fp} the noise contribution of the ACL at the output is more and more suppressed due to the increasing $G_{P,f}$. More important, the absolute value of the NF of the ACL alone is roughly 1-2 dB below the ideal NF value of 3 dB, which arises from a resistive matched gate-line termination R_{GT}, assuming all other noise sources are neglected as presented in section 3.4.3.



(a)



(b)



(c)

Fig. 5-12: (a) forward power gain $G_{P,f}$ vs. R_{fp} of TWA with CS-PRF ACL as last stage, (b) NF contribution solely from ACL (NF_{ACL}) vs. R_{fp} and (c) NF of whole TWA (NF_{TWA}) vs. R_{fp} incorporating also channel noise from the N-1 preceding stages. (g_m = 0.1 S, P = 1)

Since the ACL needs to provide an input impedance close to Z_0 in order to terminate the gate-line properly, R_{fp} cannot be selected arbitrarily. The plot of the $Re\{Z_{in,TWA}\}$ in Fig. 5-13 (a) shows the corresponding input resistance of the TWA from (5.30) below versus R_{fp} and for different N.

$$Z_{in,TWA} = \frac{\frac{Z_0}{2} + R_{fp}}{1 + g_m N \frac{Z_0}{2}}, \tag{5.37}$$

The value of R_{fp} for maintaining a perfect input match ($Z_0 = Z_{in,TWA} = 50\ \Omega$) needs to be in the range from 275 Ω to 775 Ω for $N = 2\ldots6$ stages, when the transconductance per stage equals g_m = 0.1 S. Moreover, the higher the number of stages, the larger needs to be R_{fp}, as becomes also apparent from the plot of S_{11} in Fig. 5-13 (c). For the output matching, the situation is even more critical, because the total output impedance decays with increasing parallel feedback over the last stage, as equation (5.38) and the graphs in Fig. 5-13 (b) below indicate.

$$Z_{out,TWA} = \frac{Z_0 + R_{fp}}{2 + g_m N Z_0 + \frac{R_{fp}}{Z_0}} \tag{5.38}$$

Accordingly, a significant aggravation of the ORL is the result, as the S_{22} curves in Fig. 5-13 (c) demonstrate. To realize an ORL of larger than 10 dB, the input matching has to be sacrificed to a great extent. Note that even a finite output resistance R_{DS} of the HEMTs parallel to the output is not yet considered, which further deteriorates S_{22}.

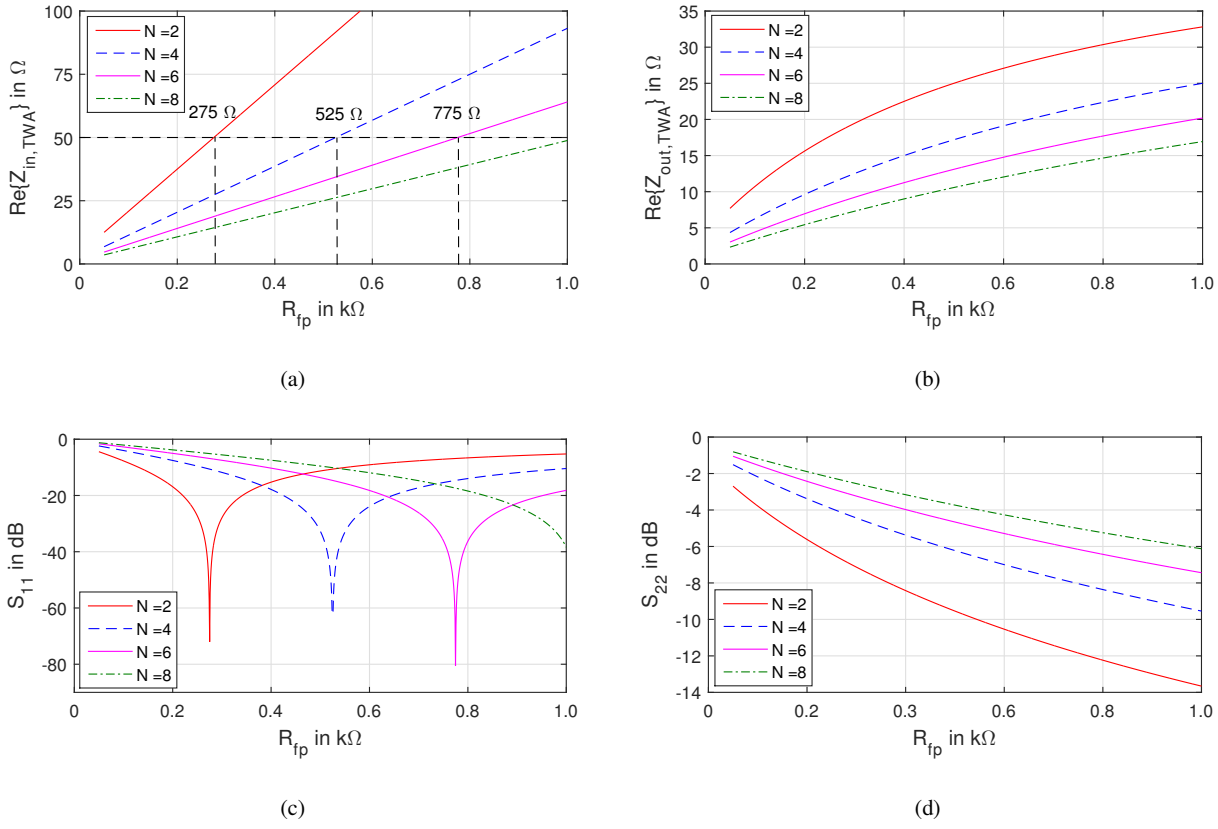
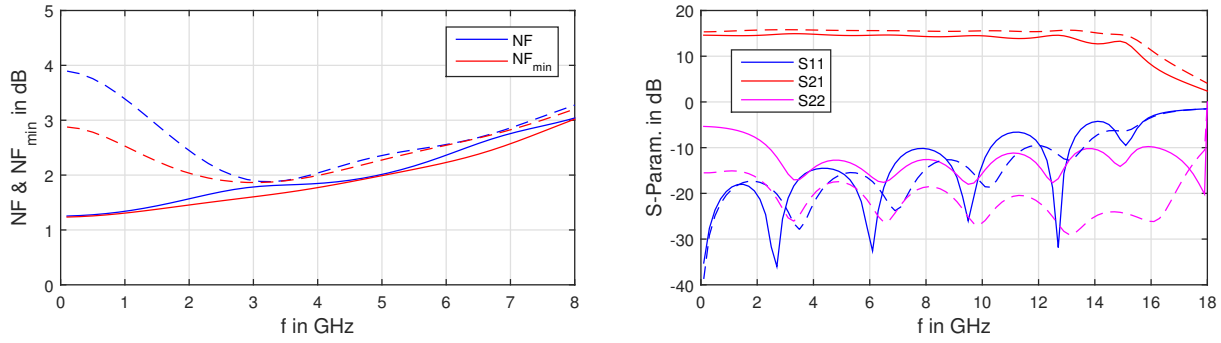


Fig. 5-13: (a) $Re\{Z_{in,TWA}\}$ vs. R_{fp} and (c) corresponding S_{11}, (b) $Re\{Z_{out,TWA}\}$ vs. R_{fp} and (d) corresponding S_{22} for different N.

After the analytical examination of the general low frequency noise and matching characteristics of a TWA with CS-PRF ACL, an ADS reference design was taken to retain also a frequency dependent comparison between the conventional resistive gate-terminatioin concept and the ACL concept with a CS-PRF-stage as last TWA section. Fig. 5-14 shows the ADS small-signal simulation results of an ideal 6-stage UDPA design with

4×50µm HEMTs, where no capacitive gate-coupling was applied in order to provide a decent gate-termination impedance at DC by the CS-PRF-stage. Insertion of series gate coupling capacitors for all other stages in order to enhance the BW is due to the increasing gate bias-noise toward low frequencies not practical (see 3.4.3) and needs to be therefore always omitted to retain low noise performance.



(a) (b)

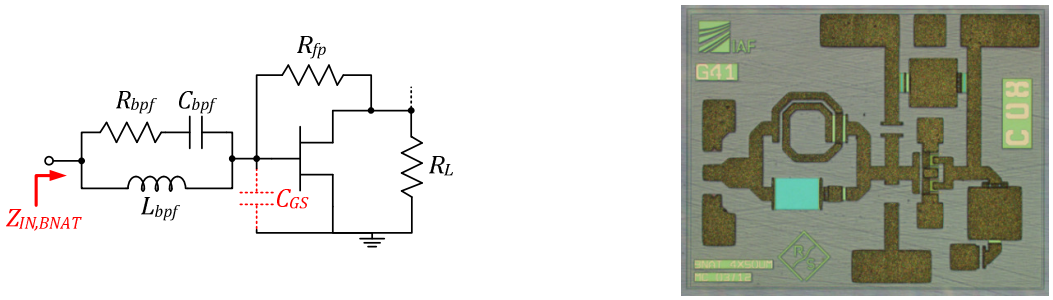
Fig. 5-14: Comparison of (a) NF & NF_{min} and (b) corresponding S-parameter of an ideal 6-stage UDPA reference design from DC-15 GHz without capacitively coupled gates (TGW = 6×4×50µm = 1.2 mm) with resistive gate-termination R_{GT} on the one hand and with CS-PRF ACL-stage (R_{fp} = 330 Ω) on the other hand.

The NF simulation results in (a) reveal that insertion of the CS-PRF-stage enables to reduce the low frequency NF by roughly 2.5 dB compared to a resistive gate-termination R_{GT}. At the same time, the same perfect input match of S_{11}, visible in (b), at low frequencies can be maintained. With increasing frequency though S_{11} becomes slightly worse due to the non-perfect gate-termination based on C_{IN} of the CS-PRF ACL-stage. This explains also the fractionally lower NF of the CS-PRF-TWA toward higher frequencies in (a). By replacing the last gate-line MSL-section in front of the ACL by an impedance transformer, C_{IN} can be compensated and the input matching maintained (not shown here).

An inherent disadvantage of the ACL-principle with CS-PRF in TWAs is the low output impedance of the feedback stage, as already mentioned and computed in (5.38), which results from the low feedback resistor value necessary to terminate the gate-line of the TWA in its characteristic line impedance of usually 50 Ω. Therewith, S_{21} degrades on the one hand due to the increased feedback and on the other hand S_{22} deteriorates especially toward low frequencies, as can be seen from Fig. 5-14 (b) by the drop from -15 dB to -5dB in ORL. The latter makes this concept inappropriate for the targeted application in T&M instruments, where a good ORL down to DC is crucial. Moreover, a lower gain-ripple can be provided when the feedback resistor is spread over all N-stages in the TWA and decreasingly tapered from the input to the output, which allows for a smoother distributed transition of the gate-termination toward the input. Unfortunately, to enable operation down to the MHz-regime, off-chip SMD capacitors become necessary in each of the N feedback paths in order to separate the DC gate- and drain supply voltages. Limited by the maximum allowable physical spacing between each section on chip, this approach is thus especially for very wide BWs, ranging from almost DC up to several GHz, not a practical solution.

5.2.6 BNAT in DC-6.5 GHz Highly Linear Low Noise TWA

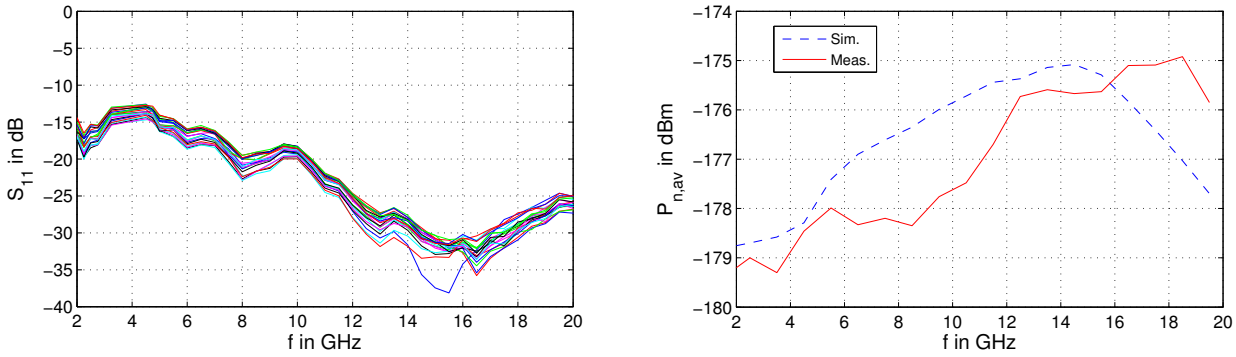
P. Ikalainen implemented the first ACL based on the CS-HEMT with parallel resistive feedback concept from section 5.2.3 in a GaAs TWA in order to reduce the amount of noise coming from the gate-line termination at low frequencies [163]. Later in 2008, A. Kopa and A. Apsel [164] replenished the feedback-based topology from P. Ikalainen in their CMOS TWA by an additional RLC-filter to increase the bandwidth performance by an extended impedance matching for higher frequencies. The additional upstream RLC filter enables the use of the CS-PRF ACL over larger bandwidths, based on the improved compensation of the decaying input impedance, which was shown in Fig. 5-10 (b). The exact impedance compensated topology is presented in Fig. 5-15 (a) below. For low frequencies, where the ACL based on the CS-PRF-concept exhibits its "coldest" performance, bypasses L_{bpf} the RC-filter and the input noise is determined by the ACL. As soon as the frequency increases, impedes L_{bpf} the signal transfer to the ACL and redirects it into the RC-filter. Thus, $Z_{IN,BNAT}$ strives to R_{bpf} for very high frequencies and therefore the available input noise power $P_{n,BNAT}$ toward $k_B T \Delta f$, assuming a perfect match.



(a) (b)

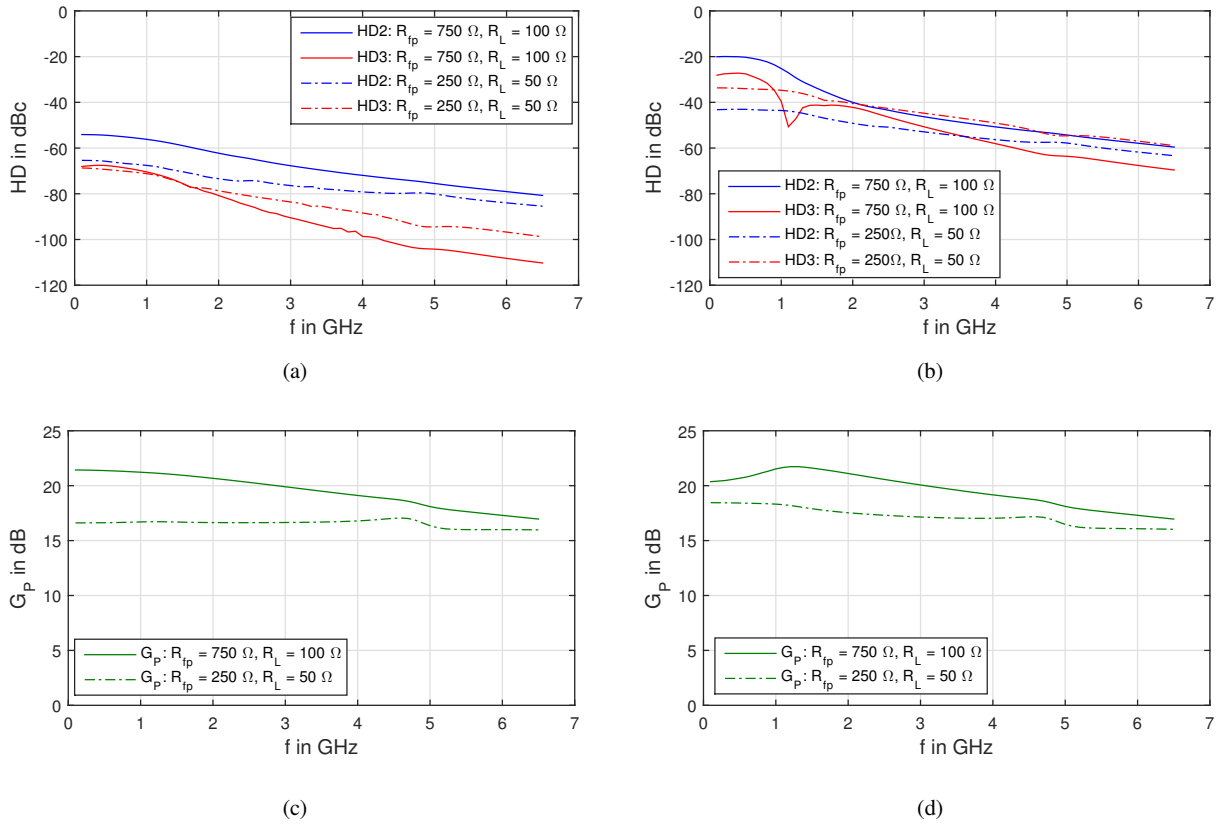
Fig. 5-15: (a) schematic of BNAT with resistive parallel feedback and upstream RLC-filter and (b) BNAT test chip with a 4×50µm GaN HEMT (chip size: 1.15 × 0.9 mm^2)

For verification purposes of the general BNAT concept a separate test-chip for the frequency range from 2-20 GHz was fabricated comprising a 4×50µm GaN HEMT with parallel resistive feedbacks, which is depicted in Fig. 5-15 (b). The measured S-parameter of a wafer map and the measured available input power $P_{n,BNAT}$ of one representative die are depicted in Fig. 5-16 below. It can be seen that the input matches well over a broad frequency range and the available input noise power is close to the simulated values, clearly showing and improvement by around 5 dB at 2 GHz opposed to a matched resistor (-174 dBm/Hz). The slight deviation in $P_{n,BNAT}$ between simulation and measurement is owed to the worse 50 Ω matching and the slightly higher g_m of the HEMT compared to the model. Therefore, the lower noise in the measurement stems from mismatch on the one hand and on the higher gain on the other hand. One cause for the shift in frequency and deviation in matching is based on the utilization of GaN epi-resistors for R_{fp} and R_L in order to obtain a small and compact die. Compared to their linear counterparts, the NiCr-resistors, epi-resistors exhibit with 500 Ω/□ unfortunately a much higher variance in their sheet-resistance due to process variations and a much higher temperature dependence than the linear 50 Ω/□ TFR resistors. This becomes especially noticeable in the lower frequency range of the BNAT, where the input impedance is principially determined by R_{fp} and R_L (see (5.15) for $\omega \ll 1$). Despite all experienced difficulties in the design and measurement, the functionality of the ACL concept has been verified in GaN technology for the first time.



(a) (b)

Fig. 5-16: Measured (a) mapped S-parameter and (b) averaged $P_{n,av}$ of one single BNAT test chip with 4×50µm GaN HEMT



(a) (b)

(c) (d)

Fig. 5-17: Simulated HD and G_P at (a,c) P_{IN} = -10 dBm and (b,d) P_{IN} = +10 dBm of L²NTWA BNAT alone with a 8×100µm HEMT for R_{fp} = 750 Ω, R_L = 100 Ω and R_{fp} = 250 Ω, R_L = 50 Ω

After the proof of concept, the BNAT was applied as active gate-termination in the DC-6.5 GHz L²NTWA design presented in chapter 4.6.2 in order to examine the degree of NF improvement opposed to a resistive gate-termination. As shown by the analysis in section 5.2.3, a larger HEMT device reduces the BW but at the same time improves the noise suppression at low frequencies. Since only the low frequency NF is affected by the reverse transfer function in a TWA, the BNAT only needs to provide less noise than a matched resistive load at low frequencies. Out of this reason a 8×100µm device was taken for the realization of the feedback stage. One

big drawback, which has not been mentioned yet, is the nonlinearity introduced by the BNAT under large-signal operation. As soon as the input signal power drives the BNAT into the nonlinear regime all output nonlinearities generated in the ACL are fed back via the feedback resistor to the input, where they are amplified by the reverse TWA gain to the output. Furthermore, it would be beneficial in terms of noise to even further increase the values of R_{fp} and R_L, since only the ratio of R_{fp} to R_L is of importance for the low frequency matching. Chosing a large value for R_L leads unfortunately to a premature saturation of the BNAT due to clipping, introducing even more nonlinearities to the TWA, as Fig. 5-17 shows. Under small signal operation in (a), the BNAT does not introduce significant nonlinearity and hence the HD at the input of the BNAT is far below -50 dBc. The difference in HD between R_{fp} = 750 Ω, R_L = 100 Ω and R_{fp} = 250 Ω, R_L = 50 Ω is clearly visible, but the overall nonlinearity is still sufficiently small not to impact the linearity of the L²NTWA significantly. Under large-signal drive in contrast, as shown in (b), the HD takes maximum values of -20 dBc for R_{fp} = 750 Ω and R_L = 100 Ω due to the large-gain of the 8×100µm FB-stage in the BNAT, as depicted in (d). Although the feedback is much lower than for the case of R_{fp} = 250 Ω and R_L = 50 Ω and it might be therefore misleadingly assumed that also less nonlinear signal components are transferred from the output of the BNAT, the linearity at the input of the BNAT improves with increasing feedback due to the lower gain, which in turn leads at the same time in a higher back-off operation of the FB-stage. So by minimization of R_{fp} and R_L, the overall impact of the BNAT on the L²NTWA's linearity can be reduced. This is only true up to a certain point, where the FB-stage does not provide sufficient gain so that the BNAT does not perform as an ACL anymore.

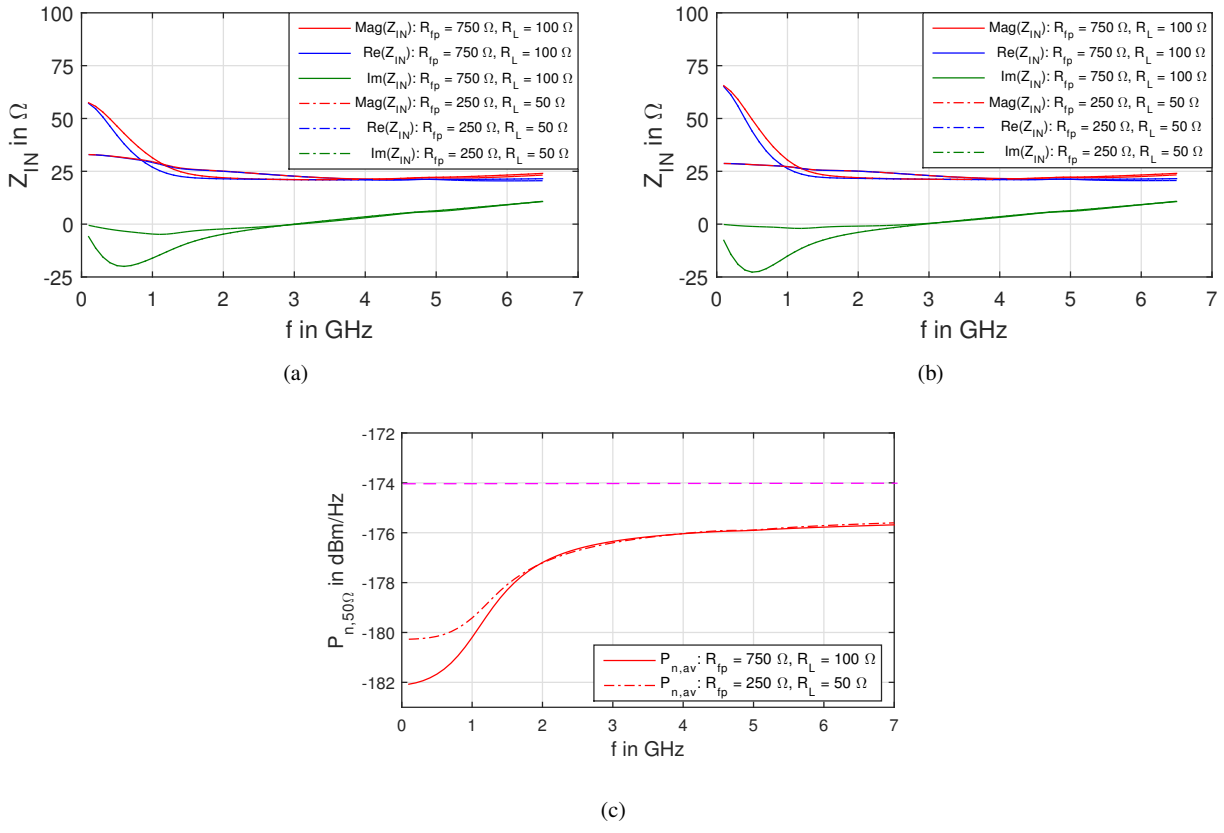
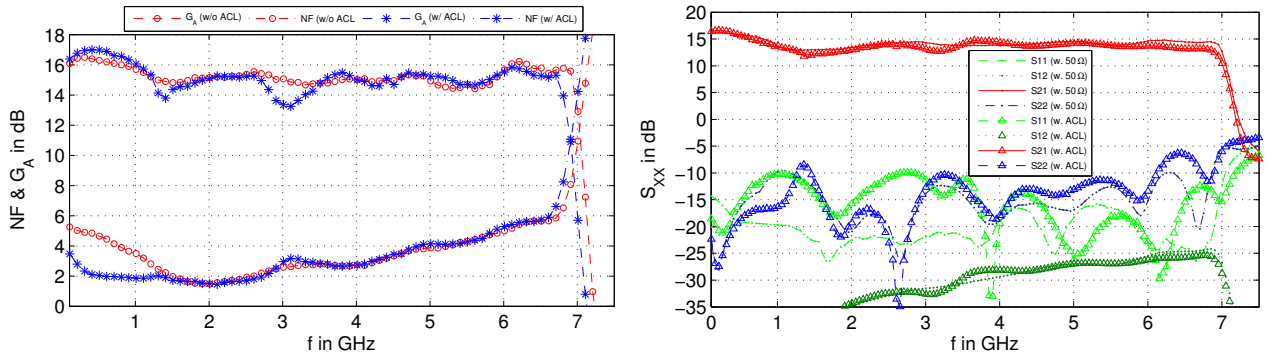


Fig. 5-18: Simulated Z_{IN} at (a) P_{IN} = -10 dBm and (b) P_{IN} = +10 dBm and (c) $P_{n,av}$ at the input of L²NTWA BNAT alone with a 8×100µm HEMT for R_{fp} = 750 Ω, R_L = 100 Ω and R_{fp} = 250 Ω, R_L = 50 Ω

As can be seen from Fig. 5-18 (a) and (b), the resulting input impedance Z_{IN} of the BNAT is also strongly affected by the applied input power. For the case R_{fp} = 750 Ω, R_L = 100 Ω the effective low frequency input impedance rises from roughly 57 Ω to 65 Ω for a 20 dB higher P_{IN}. For the case R_{fp} = 250 Ω, R_L = 50 Ω in contrast exhibits Z_{IN} the opposite dependency and decreases with increasing P_{IN} by roughly 4 Ω to 29 Ω. This can be explained by means of the gain characteristics depicted in Fig. 5-17 (c) and (d). For R_{fp} = 750 Ω and R_L = 100 Ω, G_P shows at low frequencies a compressive behavior with increasing P_{IN}, whereas for R_{fp} = 250 Ω and R_L = 50 Ω an expansive behavior can be observed. This results one to one in an increasing or decreasing input impedance characteristic, as (5.15) reveals for an effective smaller or larger g_m in the denominator. In small-signal mode the difference in Z_{IN} leads to a difference in the noise power delivered to the characteristic gate-line impedance of Z_0 = 50 Ω, as Fig. 5-18 (c) illustrates. When the matching between BNAT and Z_0 is degraded, as it is for the case with R_{fp} = 250 Ω, R_L = 50 Ω, less noise is delivered to the gate-line compared to a perfect match. Although the setting with R_{fp} = 750 Ω and R_L = 100 Ω shows from (a) to exhibit a better match to Z_0, less noise power is available to the gate-line due to the higher noise suppression, which is dependent on the amount of gain in the FB-stage and on the absolute magnitude of R_{fp} and R_L, as equation (5.39) reveals.

$$P_{n,BNAT} = \frac{k_B T_0 \Delta f}{1 + g_m R_L}\left(1 + \frac{g_m {R_L}^2 P}{(R_L + R_{fp})}\right) \tag{5.39}$$

Equation (5.39) is derived from (5.23) under the further simplifying assumptions of R_G = 0 Ω and $R_L \ll R_{DS}$. It should be noticed that for $\omega \ll 1$ the upstream RLC-filter does not shape the input noise power and thus $P_{n,BNAT}$ becomes equal to $P_{n,cfp}$, wherefrom (5.39) is computed.



(a) (b)

Fig. 5-19: Measured (a) NF and associated gain G_A and (b) S-parameter measurement for the DC-6.5 GHz L²NTWA "Latukan" with and w/o BNAT

So far it has be shown that a certain trade-off between linearity and optimum noise performance in terms of R_{fp} and R_L in the BNAT exists. Since the primary focus was set on the verification of the BNAT principle in GaN technology, the resistor values in the design of the L²NTWA were chosen equal to R_{fp} = 750 Ω and R_L = 100 Ω, giving a higher noise suppression at low frequencies, as presented in Fig. 5-18 (c). The final measured small-signal performance of the L²NTWA with BNAT compared to the case with resistive gate-termination

is plotted in Fig. 5-19. The small-signal and noise measurements were conducted in the same custom made package as the linearity measurements, which were already presented in chapter 4.6.2. It can be seen in Fig. 5-19 that the overall small-signal performance is only slightly affected by the gate-line termination with a BNAT. Clearly observable from the comparison of the resistive load R_{GT} with the BNAT is the difference in S_{11} in Fig. 5-19 (b), which results from the slightly degraded input matching introduced by the non-ideal BNAT. This higher input mismatch comes along with a higher gain-ripple for the L²NTWA with BNAT opposed to the resistive termination. Nevertheless, S_{21} is pretty much similar at low frequencies, which enables to make a meaningful statement about the amount of NF improvement gained by the BNAT. Fig. 5-19 (a) shows that the noise below 1.5 GHz is significantly reduced by the BNAT, resulting in a NF improvement of around 1.9 dB at 10 MHz opposed to the resistive gate-termination with R_{GT}. Hence, the shown measurements prove that the concept of low-frequency noise reduction by means of terminating the gate-line with an ACL/BNAT is a viable option for realizing low-noise TWA designs operating down to DC.

5.2.7 Key Findings

Three possibilities for the implementation of an ACL were studied and theoretically examined in 5.2.1 - 5.2.4 to find the optimum topology for the targeted application in a DA. Among the three concepts, which are a common-source HEMT with parallel resistive feedback (CS-PRF), a common-source HEMT with series inductive feedback (CS-SIF) and a simple common-gate HEMT, the CS-PRF topology proved to be the best under the given requirements of low frequency noise improvement in a DA under a 50 Ω environment. The best solution in terms of bandwidth is the CS-SIF topology, since it exhibits an almost constant real-part of Z_{IN} over a very large frequency range, but unfortunately its reactive part shows a purely capacitive behavior at low frequencies. The CG-HEMT shows a similar suited Z_{IN} dependence as the CS-PRF topology, but since its real-part is proportional to $1/g_m$, W_G of the CG-HEMT has to be very small to be matched to 50 Ω. This leads unfortunately to insufficient noise suppression at low frequencies, which is always proportional to g_m. Out of these mentioned reasons, the CS-PRF topology was identified as the proper candidate for the implementation of the DA's gate-termination, whereby the decaying real-part of Z_{IN} toward high frequencies was compensated by an upstream RLC-filter, as already presented in [164].

Instead of replacing the resistive gate-line termination in a TWA design by an ACL, the concept of low frequency noise reduction by using the CS-PRF ACL as last active stage has also been analytically verified. Thereby, NF equations for the low frequency case were derived, which can be used either directly for the design flow of a low-noise TWA or just for gaining a better understanding of the trade-off between noise and matching, which is dependent on the number of stages N, the transconductance g_m of the HEMTs and the value of the feedback resistor R_{fp}. Due to the degraded low frequency ORL, which is the result of the additional parallel feedback resistor, a chip implementation of this concept was not carried out with regard to the targeted matching requirements. However, the active cold load (ACL) concept in form of a "blue-noise" active load termination (BNAT) has been implemented for the first time in GaN technology as a substitute for the resistive gate-line termination. The noise performance compared to a simple resistive gate-termination was verified by small-signal and noise measurements over a broad frequency range from 10 MHz up to 6.5 GHz. Dependent on the external SMD circuitry after assembly and packaging of the presented DA, the lowest frequency of operation could be extended even down to DC if desired, giving a net total frequency range of more than 9 decades. By connectiong the BNAT to the end of the gate-line, the NF of the DA was improved at 10 MHz by 1.9 dB from

5.5 dB (without BNAT) down to 3.6 dB (with BNAT). This represents a significant low-frequency noise improvement and shows the capability of GaN DAs to be even used as low-noise small-signal amplifiers. The overall chip area was increased by the BNAT by roughly 25% (DA 12.5 mm², BNAT 2.5 mm²).

Due to the nonlinear behavior of the BNAT under large-signal operation, the overall linearity of the DA is impacted by the the low-noise gate termination, especially at low frequencies. Since the generated harmonics of the BNAT become due to the relatively low isolation provided by the feedback with increasing P_{IN} more and more noticeable on the gate-line of the DA. From there, these nonlinearities are further amplified by the DA toward the output, which is tantamount to an upstream distorter to the DA. Thus, to maintain a certain linearity of the TWA, noise performance needs to be sacrificed by lowering the values of the feedback resistor R_{fp} and the load resistor R_L in the BNAT. More detailed linearity investiagtions of the whole TWA including BNAT could not be conducted due to the limited time frame of this work. However it can be concluded, if a low NF and a low HD need to be guaranteed at the same time, it is necessary to distinguish between a small-signal and large-signal operation mode in the DA. One possible solution under CW-operation might be either to introduce a pre-defined P_{IN} threshold, which is already known from the instrument settings or to implement an on-chip power detector circuit which bypasses the BNAT by a simple resistive termination under large-signal operation. Both solutions need additional on-chip switches for differentiation between small-signal and large-signal modes, which would further increase the total chip area.

5.3 Conclusion

In the preceding chapters 5.1 and 5.2 possible noise reduction concepts were presented and analyzed for their applicability to broadband PAs. Section 5.1 concentrated on the wideband thermal noise improvement for FBPAs by means of porting the feed-forward noise cancellation (FFNC) technique to GaN technology, which is originally intended for building LNAs in CMOS technology, as described by F. Bruccoleri in [160]. The basic idea of this concept is the cancellation of the feedback PA output noise, which is fed back in-phase via the parallel feedback path to the input, by a separate parallel inverting amplifier stage. In this way, by addition of the noisy output signal of the FBPA on the one and and the noisy input signal by the inverting amplifier stage on the other hand, the two out-of-phase signals cancel out in the output adder stage, when the gain of the inverting amplifier is set correctly. Unfortunately, this imposes a maximum device size constraint on the output adder-stage HEMTs, since the gain of the inverting amplifier has to be reduced to meet exactly the gain of the parallel-feedback stage. This leads to a much smaller device size for the output stage than for the FBPA, which drastically affect the maximum obltainable output power of the whole PA. Out this reason, this concept is only applicable to amplifier designs with low output power levels and is hence not suited for GaN PAs.

The one and only remaining "regulation screw" to achieve low-noise performance in a broadband FBPA design is hence to sacrifice small-signal matching, gain performance and output power, by matching the input to $S_{opt}{}^{*}$ for obtaining optimum low noise performance. As already presented in 3.3.2, it furthermore helps to keep the value of the series feedback resistor as small as possible.

For the TWA topology the trade-off between noise, small-signal matching, gain and output power is quite similar for each single stage to the case of the FBPA. The only major difference is the increasing low frequency noise contribution coming from the gate-bias resistors and the gate-line termination resistor. In order to achieve a flat noise performance down to DC, it is thus crucial to omit any series gate-coupling capacitors for bandwidth enhancement in the gate-line. Due to the increasing impedance with decreasing frequency of these capacitors, the total available noise power of the gate-bias resistors will be amplified to the output. Omission of the gate-coupling capacitors results in a large impedance mismatch between the gate-bias resistors of usually a few hundred Ohms and the characteristic gate-line impedance of usually 50 Ω, leading to a negligible noise contribution of the bias resistors toward low frequencies. Without applying capacitive gate-coupling, the second largest noise contributor is now the gate-line termination resistor R_{GT}. Since the reverse gain-transfer function from R_{GT} to the output increases with decreasing frequency, the introduction of mismatch between R_{GT} and $Z_{0,G}$ would help to reduce the amount of injected noise into the gate-line. However, the input matching of the TWA would be at the same time heavily affected by this introduced mismatch. Instead of making use of mismatch, it is more reasonable to lower the amount of noise coming from R_{GT} but maintaining perfect matching to the gate-line. This can be achieved by replacing R_{GT} by a so called active cold load (ACL) circuit, which exhibits a much lower available input noise power density (noise temperature) than the -174 dBm/Hz (297 K) of R_{GT} at room temperature, but still exhibits R_{GT} as input impedance for a perfect match to the gate-line.

Three different ACL topologies, namely a CG-HEMT, a CS-HEMT with series inductive feedback (CS-SIF) and a CS-HEMT applying parallel resistive feedback (CS-PRF), were therefore first of all analytically assessed for their suitability as a TWA gate-termination. The analysis of the CG-HEMT revealed that the noise improvement is not sufficient, because the device size has to be chosen according to its input impedance very small in order to satisfy the low frequency matching condition of $1/g_{m,CG} = R_{GT}$. The CS-SIF ACL showed the best broadband matching performance due to the impedance transformation of the source inductance into a fre-

quency independent real-part at the input. Together with a larger device size and thus gain, the available input noise power can be significantly reduced. In terms of wideband matching possesses the CS-PRF ACL the strongest frequency dependence compared to the other two mentioned topologies and thus seems to be not a viable option at first sight. Since the input noise power of the ACL in a TWA only needs to be minimized where the reverse gain increases, the ACL does not necessarily need to cover the full BW of the TWA but rather only a small low frequncy fraction of it. Therefore, a much larger HEMT can be taken for the CS-PRF ACL, which then exhibits a reduced BW but now a much lower available input noise power due to the increased gain. This gives a certain degree of freedom for the low frequency noise shaping by selecting a proper device size and parallel feedback resistor value for the targeted bandwidth. Furthermore, in order to avoid degraded input matching of the TWA with increasing frequency, an upstream parallel RLC-filter in front ot the CS-PRF ACL can be used to maintain impedance matching to $Z_{0,G}$ over the entire TWA frequency range. The combination of the RLC-filter and the CS-PRF ACL is also called blue-noise active termination (BNAT), where the low-frequency noise shaping is in analogy to the spectrum of blue light.

It is important to mention that in general two different positions for the ACL within a TWA exist. The first is the already discussed position as R_{GT} substitute, which gives the advantage of an almost independent design of the ACL, detached from the TWA topology. For some low cost designs it is even imaginable to place only the RLC-filter on-chip to save die area but to attach the ACL off-chip, maybe even in a different technology. Moreover, the amplifiying device periphery of the TWA is unchanged. Opposingly, the second position would be as substitute of the last amplifying stage in the TWA, as in the meantime patented by K. Kobayashi in 2012 [162], which has now impact on the overall transfer function of the TWA. Due to the parallel feedback resistor in the last stage, the gate-line is properly terminated but the ORL is strongly degraded, especially toward low frequencies. Also the overall gain and BW are slightly worse dependent on the amount of applied feedback in the last stage. Out of the last two mentioned reasons, the CS-PRF ACL together with a RLC-filter was implemented as replacement of R_{GT} in the DC-6.5 GHz L²NTWA from section 4.6.2. Beforehand, a standalone BNAT test-chip was designed and measured for a general prove of concept. The measurements of the L²NTWA, which incorporates a 8×100µm device in the BNAT, showed a NF improvement of 1.9 dB from 5.5 dB down to 3.6 dB at 100 MHz, which proves to be an outstanding low frequency noise performance for a 2W PA. At midband a minimum NF of even 1.9 dB was measured.

CHAPTER 6

STABILITY INVESTIGATION OF DIFFERENTIAL AMPLIFIERS

Differential amplifiers are well suited for applications, where the dominant 2nd order nonlinearity needs to be eliminated in order to increase the $SFDR$ of the output signal, as the analysis and design of a TD-FBPA in chapter 4.7 revealed. Besides the necessary requirement for differential stability, all differential circuits need to behave also stable under common-mode excitation. Out of this reason, the following chapters will investigate the differential as well as common-mode stability of pseudo-differential- (PD) and truly-differential (TD)-pairs.

6.1 Theoretical Stability Investigation of an Unmatched TD-pair

Fig. 6-1 depicts the small-signal equivalent circuit of a PD- and TD-amplifier in common-mode operation, in which the real loading of the source node by the current source can be represented by the current source output conductance Y_{CS}. There are two possible small-signal equivalent circuit representations of the TD-pair in common-mode. One representation considers the two HEMTs of the TD-pair as one big parallel device in the common-mode environment with $Z_{0,cm} = 25\ \Omega$. The other takes due to symmetry only one half of the TD-pair in the single-ended impedance environment with $Z_0 = 50\ \Omega$ into account, where the Y-parameters correspond to only half of the actual physical device size in common-mode. Whereas in common-mode the PD-pair behaves exactly identical as in differential-mode and thus the common-mode rejection ratio ($CMRR$) is zero, which can be seen by Fig. 6-1 (a), the TD-pair sees the impedance $1/Y_{\mathrm{CS}}$ of the current source towards ground and thus exhibits a high $CMRR$. (Note: The $CMRR$ is in the following defined by S_{d2d1}/S_{c2c1})

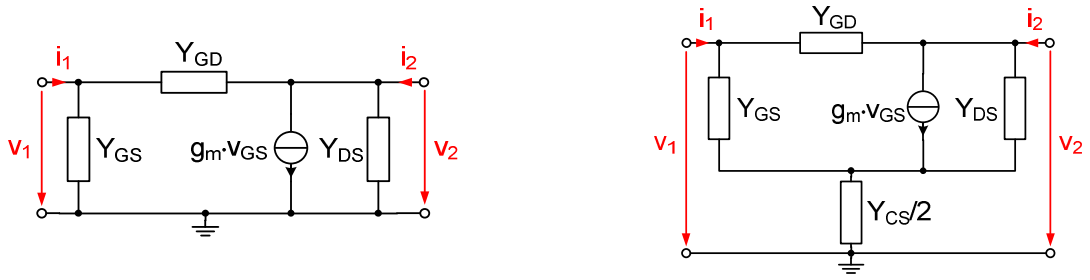


Fig. 6-1: (a) Pseudo-differential (PD) and (b) Truly-differential (TD) small signal equivalent circuit under common-mode excitation

For the common-mode Y-parameters (Y_{cc}) of the TD-pair in Fig. 6-1 (b), the following equations (6.1) to (6.5) hold.

$$Y_{c1c1} = Y_{\mathrm{GD}} + \frac{Y_{\mathrm{GS}}(Y_{\mathrm{DS}} + Y_{CS}/2)}{D_{n,cm}} \tag{6.1}$$

$$Y_{c1c2} = -\left(Y_{\mathrm{GD}} + \frac{Y_{\mathrm{GS}}Y_{\mathrm{DS}}}{D_{n,cm}}\right) \tag{6.2}$$

$$Y_{c2c1} = -\left(Y_{\mathrm{GD}} + \frac{Y_{\mathrm{GS}}(Y_{\mathrm{DS}} + j \cdot g_m Y_{CS}/2 \cdot Im\{1/Y_{\mathrm{GS}}\})}{D_{n,cm}}\right) \tag{6.3}$$

$$Y_{c2c2} = Y_{\mathrm{GD}} + \frac{Y_{\mathrm{DS}}(Y_{\mathrm{GS}} + Y_{CS}/2)}{D_{n,cm}} \tag{6.4}$$

with

$$D_{n,cm} = (Y_{\mathrm{GS}} + Y_{\mathrm{DS}} + Y_{CS}/2) - j \cdot g_m Y_{\mathrm{GS}} \cdot Im\{1/Y_{\mathrm{GS}}\}. \tag{6.5}$$

For an ideal current source ($Y_{CS} = 0$ S) the Y_{cc}-parameters become equal to

$$\begin{aligned} Y_{c1c1} &= \left(Y_{\mathrm{GD}} + \frac{Y_{\mathrm{GS}}Y_{\mathrm{DS}}}{(Y_{\mathrm{GS}} + Y_{\mathrm{DS}}) - j \cdot g_m Y_{\mathrm{GS}} \cdot Im\{1/Y_{\mathrm{GS}}\}}\right) \\ &= -Y_{c1c2} = -Y_{c2c1} = Y_{c2c2}. \end{aligned} \tag{6.6}$$

From equation (6.6) above two general characteristics of a TD-pair in common-mode operation can be derived. First, the differential amplifier is reciprocal ($Y_{c1c2} = Y_{c2c1}$) and second input and output admittances are equal ($Y_{c1c1} = Y_{c2c2}$), leading to full symmetry. Hence, it can be stated in terms of S-parameters that $S_{c1c1} = S_{c2c2}$ and $S_{c1c2} = S_{c2c1}$. Therefore, for $Y_{CS} = 0$ S it is sufficient to regard only two of the four S_{cc}-parameters, which can be expressed in terms of the already calculated Y_{cc}-parameters according to [72] to

$$S_{c1c1/c2c2} = \frac{(1 - Z_0{}^* Y_{c1c1/c2c2})(1 + Z_0 Y_{c2c2/c1c1}) + |Z_0|^2 Y_{c1c2/c2c1} Y_{c2c1/c1c2}}{(1 + Z_0 Y_{c1c1/c2c2})(1 + Z_0 Y_{c2c2/c1c1}) - Z_0{}^2 Y_{c1c2/c2c1} Y_{c2c1/c1c2}} \tag{6.7}$$

$$S_{c1c2/c2c1} = \frac{-2 \cdot Y_{c1c2/c2c1} Re\{Z_0\}}{(1 + Z_0 Y_{c1c1/c2c2})(1 + Z_0 Y_{c2c2/c1c1}) - Z_0{}^2 Y_{c1c2/c2c1} Y_{c2c1/c1c2}}. \tag{6.8}$$

In the following stability analysis a TD-Pair comprising two 8×125µm HEMTs is assumed, which is loaded by R_{CS} and C_{CS} at the source terminals, representing the parasitic loading by a real current source, as shown in Fig. 6-2. The corresponding HEMT parameters are listed in Table 6-1.

Table 6-1: Transistor parameters of 8×125µm HEMT at V_{DS} = 30 V and I_{DS} = 100 mA/mm

Parameter	Value
C_{GS}	1.6 pF
R_{GS}	2.8 Ω
C_{GD}	100 fF
R_{GD}	12 Ω
C_{DS}	260 fF
R_{DS}	235 Ω
g_{m0}	240 mS
τ	3.5 ps

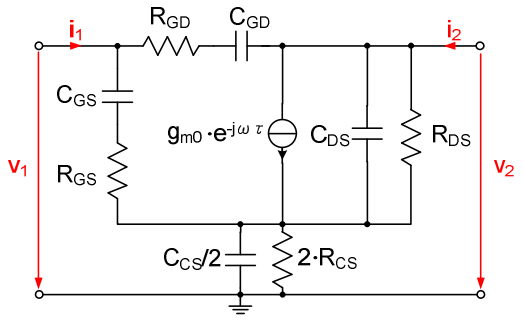


Fig. 6-2: Small-signal equivalent circuit of Fig. 6-1 (b)

Furthermore, all small-signal stability investigations for the TD-pair depicted in Fig. 6-2 are undertaken by means of the stability measures μ and μ' [165], which are defined by

$$\mu = \frac{1 - |S_{c1c1}|^2}{|S_{c2c2} - S_{c1c1}{}^* \cdot det(S_{cc})| + |S_{c1c2} \cdot S_{c2c1}|} \tag{6.9}$$

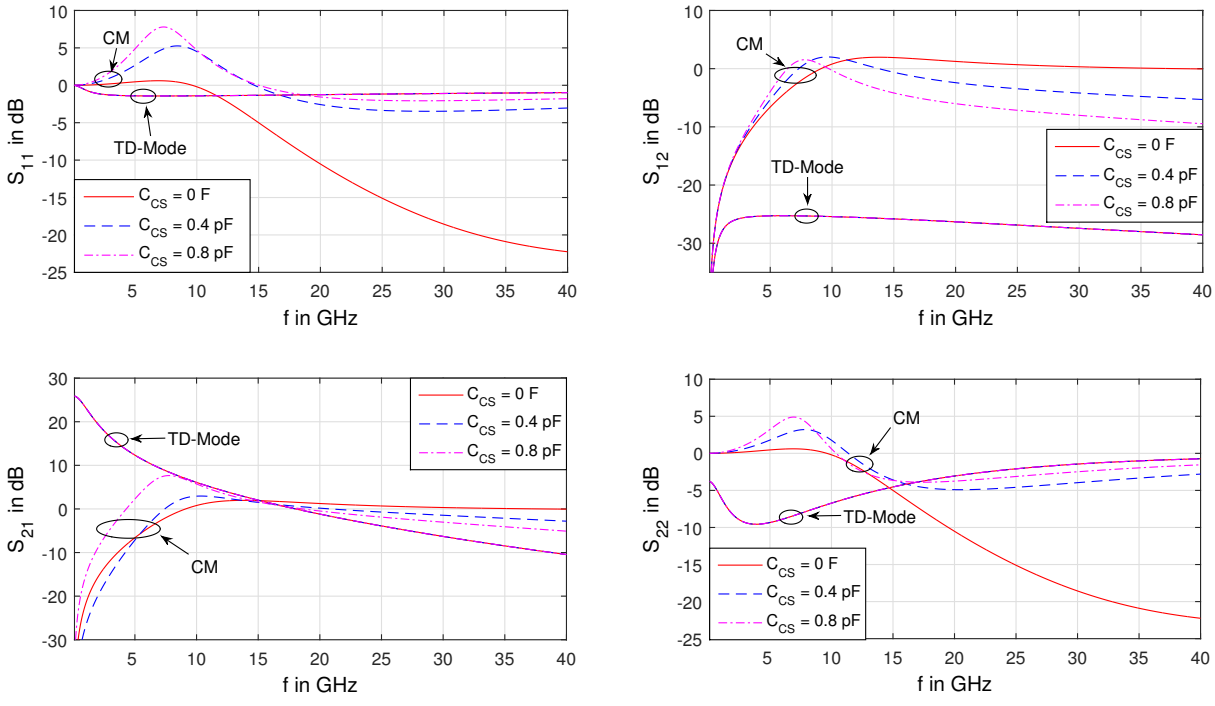
for the load and correspondingly for the source by

$$\mu' = \frac{1 - |S_{c2c2}|^2}{|S_{c1c1} - S_{c2c2}{}^* \cdot det(S_{cc})| + |S_{c1c2} \cdot S_{c2c1}|}. \tag{6.10}$$

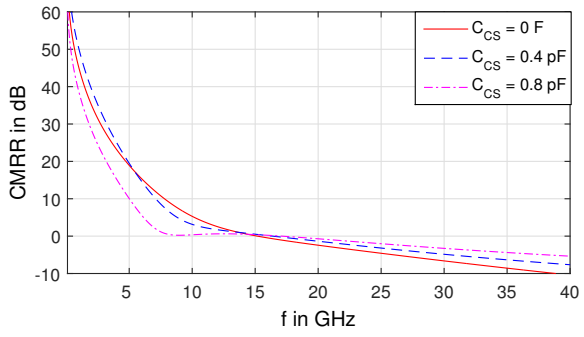
By means of (6.9) and (6.10), an exact statement about unconditional or conditional stability under common-mode operation can be now made. To fulfill the necessary and sufficient condition in terms of unconditional stability, μ and μ' have to be both larger than one. As long as μ or μ' are between zero and one, the TD-pair is only conditionally stable. If μ and μ' are smaller than zero, S_{c1c1} and S_{c2c2} have to be larger than one, which gives rise to instabilities at the input or output port.

6.1.1 Stability Dependence on the Current-Source Capacitance

If the small-signal parameters of the 8×125µm HEMT from Table 6-1 are considered and the common-mode S-parameters are calculated by means of equations (6.7) and (6.8) the following dependencies become evident by taking a closer look onto Fig. 6-3. For the sake of completeness the differential S-parameters are added in the plots in order to derive from S_{d2d1} and S_{c2c1} the dependency of the $CMRR$ on C_{CS} for $R_{CS} = \infty\,\Omega$. The corresponding differential Y-parameter equations are explicitly not shown in this section, because they are equal to a double-sized single-ended CS-HEMT, which exhibits only half of the transconductance ($g_m/2$).



(a)



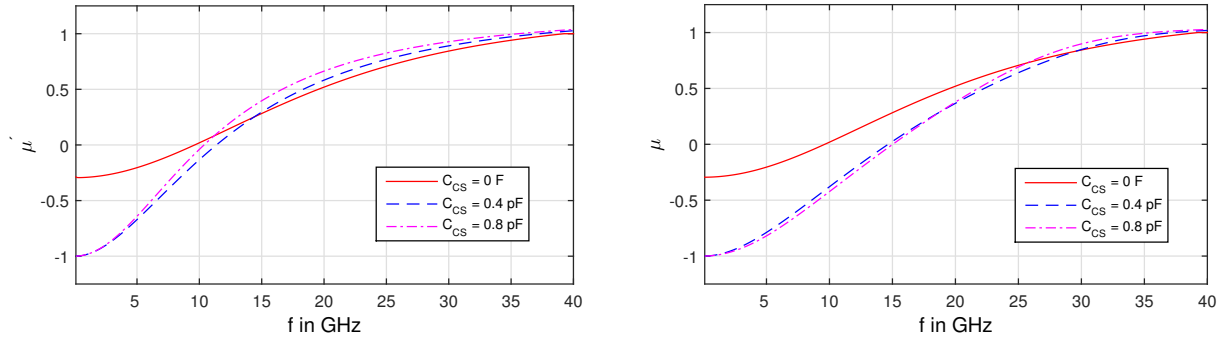
(b)

Fig. 6-3: (a) common-mode (CM) and truly-differential-mode (TD-mode) S-parameters and (b) the corresponding $CMRR$ for different capacitive loading at the virtual ground node of the TD-pair comprising two 8×125µm HEMTs

From the plots in Fig. 6-3 the following three conclusions can be drawn:

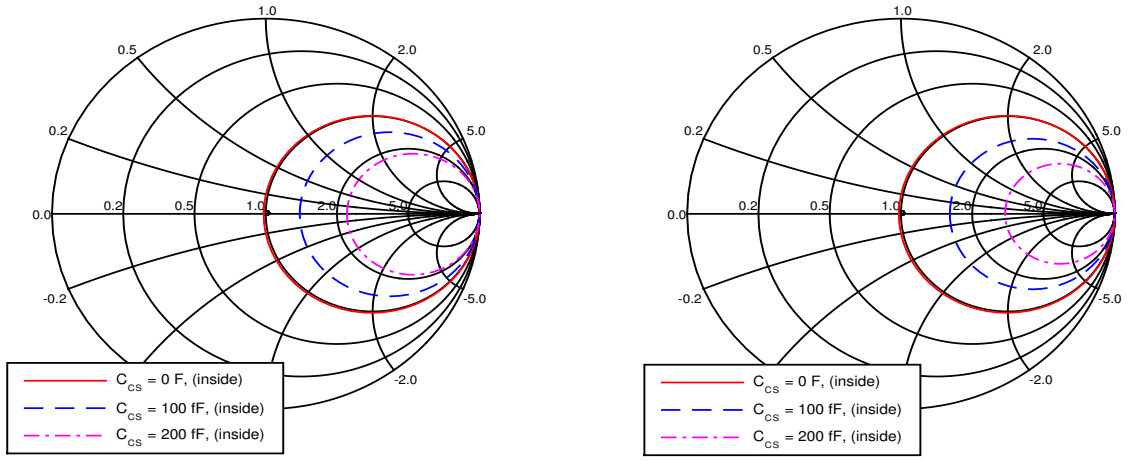
1. The common-mode gain S_{c2c1} shifts down to lower frequencies and increases with increasing C_{CS} and hence lowers the $CMRR$.
2. $S_{c2c1} = S_{c1c2}$ and above all $S_{c1c1} = S_{c2c2}$ become already positive for an ideal current source ($C_{CS} = 0$ F, $R_{CS} = \infty\ \Omega$).
3. The maximum magnitude of S_{c1c1}, S_{c2c2} and S_{c2c1} goes up with increasing C_{CS}

Point number one is more or less obvious by comparing Fig. 6-1 (a) and (b), because with increasing C_{CS} the TD-pair topology converges more and more to the one of a PD-pair. Number two on the contrary is the more surprising statement, since it reveals that the TD-pair is not inherently stable under common-mode operation. Point number three moreover indicates that the higher the parasitic capacitance to ground of the tail current-source gets, the more instable becomes the TD-pair at low frequencies.



(a) (b)

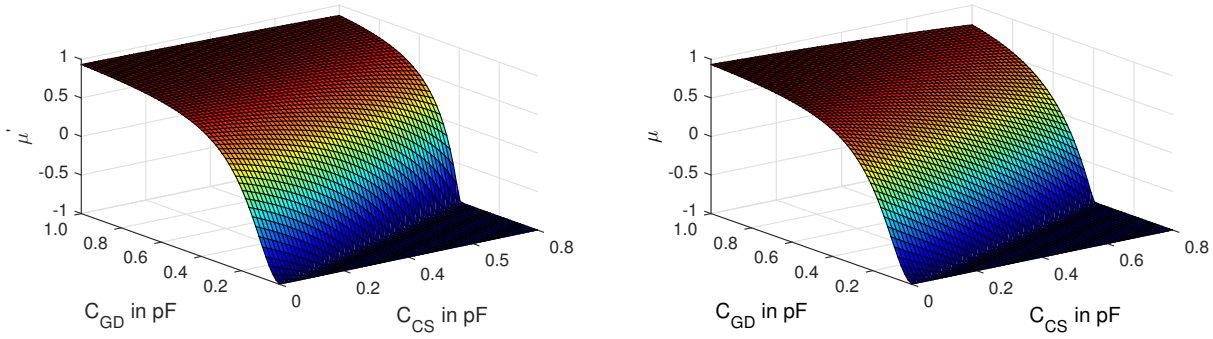
Fig. 6-4: Simulated stability measures μ and μ' for different capacitive loading C_{CS} at the virtual ground node of the TD-pair for two 8×125µm HEMTs



(a) (b)

Fig. 6-5: Simulated (a) source stability and (b) load stability circles for different C_{CS} at the virtual ground node of the 8×125µm TD-pair

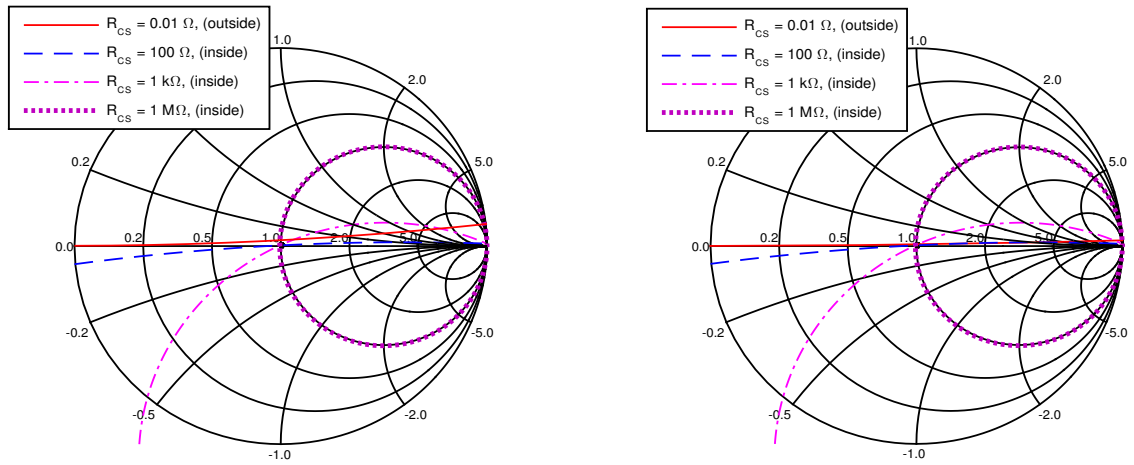
In order to find a way to properly evaluate the source and load stability under 50 Ω for different capacitive loading at the virtual ground node and to minimize computational effort, it is straightforward to plot the stability measures μ or μ' versus C_{GD} and C_{CS} for constant $C_{\mathrm{DS}} = 260$ fF only at low frequencies and graphically deduce the necessary values of C_{GD} and C_{CS} for obtaining conditional stability under 50 Ω. All values giving μ or μ' greater than zero in Fig. 6-6 yield stable behavior in 50 Ω environment. The tendency shows that with increasing C_{CS} a larger C_{GD} is required to guarantee stability. At the ideal limit condition $C_{CS} = 0$ F of the 8×125µm HEMT with $C_{\mathrm{DS}} = 260$ fF, the center of the smith-chart is only touched/enclosed for values of $C_{\mathrm{GD}} \geq 188$ fF, as can be read out from Fig. 6-5 and Fig. 6-6.



(a) (b)

Fig. 6-6: (a) μ' and (b) μ vs. C_{GD} and C_{CS} for the 8×125µm TD-pair with C_{DS} = 260 fF

6.1.2 Stability Dependence on the Current-Source Resistance



(a) (b)

Fig. 6-7: (a) source and (b) load stability circles for different resistive loading R_{CS} at the virtual ground node of the 8×125µm TD-pair

In a similar fashion to the foregoing section, where the dependence of C_{GD} on C_{CS} with $R_{CS} = \infty\ \Omega$ was derived, now the dependence of C_{GD} on R_{CS} for the condition of $C_{CS} = 0$ F is examined. The stability circles are depicted in Fig. 6-7 for various R_{CS} values for $C_{\mathrm{GD}} = 188$ fF, which was derived from Fig. 6-6 for $C_{CS} = 0$ F. For all R_{CS} values stability under 50 Ω is preserved. The stability circles for $R_{CS} = 0.01\ \Omega$ are equal to the stability circles of the PD-pair in common-mode and differential mode. With decreasing R_{CS} the TD-pair becomes more and more stable for lower input and output impedances.

6.1.3 Stability Dependence on Intrinsic HEMT Parameters

In order to obtain a more detailed insight into the common-mode stability behavior and its dependency on important HEMT parameters, it is useful to include all possible source and load impedances, which might cause instabilities. Therefore, the source and load stability circles are computed for the ideal case of $C_{CS} = 0$ F and $R_{CS} = \infty\ \Omega$ and plotted in Fig. 6-8 for a variation of the feedback capacitance C_{GD}, drain-source capacitance C_{DS}, gate-source capacitance C_{GS} and transconductance g_{m0} for a 8×125µm HEMT. Since the source node capacitance C_{CS} towards ground is set to zero it is sufficient to consider only the stability circles for either source or load, because of the two-port reciprocity for $C_{CS} = 0$ F, as equation (6.6) revealed. Moreover, to properly assess the stability of the TD-pair in common-mode and to reduce computational overhead based on the large parameter space, it is meaningful to regard the stability circles only at the frequency, where μ or μ' exhibit their minimum, which can be found from Fig. 6-4 being at low frequencies. The four plots above in Fig. 6-8 show the dependency of the stability circles on C_{GD}, C_{DS}, C_{GS} and g_{m0} at 0.1 GHz. An increase of C_{GD} above 150 fF (≙ 50 % increase of nominal value 100 fF) makes the TD-pair already stable under 50 Ω environment, as Fig. 6-8 (a) depicts. A similar behavior can be found from Fig. 6-8 (d) for increasing g_{m0}, where above 600 mS (≙ 200 % increase of nominal value 300 mS) stability is obtained. The stability region for $g_{m0} = 0$ S moves outside the stability circle in the smith-chart in Fig. 6-8 (c) due to the fact that no gain impedes any occurrence of instabilities. Opposing to C_{GD} and g_{m0}, an increase in C_{DS} beyond 150 fF (≙ 42 % decrease of nominal value 260 fF) leads to an instabilities under 50 Ω as well as an increase of C_{GS} beyond 550 fF (≙ 66 % decrease of nominal value 1.6 pF). On the one hand, the dependency of the CM-stability close to DC shows that it is dependent on g_{m0} and C_{GS} and thus on the transit frequency f_T, which can be approximated by

$$f_T \cong \frac{g_{m0}}{2\pi \cdot (C_{\mathrm{GS}} + C_{\mathrm{GD}})}. \tag{6.11}$$

On the other hand, the relation between the parameters C_{GD} and C_{DS} mainly determines the stability of the TD-pair in common-mode as well. This is only true for the TD-pair in differential mode, but in common-mode the high impedance of $1/Y_{CS}$ towards ground at the virtual ground node effects the common-mode stability of the TD-pair and makes it very sensitive to the relation between C_{GD} and C_{DS}. A mathematical dependency for C_{GD} on C_{DS} or vice versa can be defined, which guarantees that the TD-pair is stable under Z_0 as long as the ratio g_m/C_{GS} is kept constant. From the stability measures μ and μ' in equations (6.9) and (6.10) it can be derived that as long as $|S_{c1c1}|$ and $|S_{c2c2}|$ stay below one in combination with S_{c2c1} and S_{c1c2} being negligibly small close to DC, μ and μ' stay above zero. This merely means that the TD-pair is only conditionally stable, but it is already stable for Z_0, since the stability circles always encompass the center of the smith-chart. From this condition the following approximation in (6.12) for the stability limit can be set.

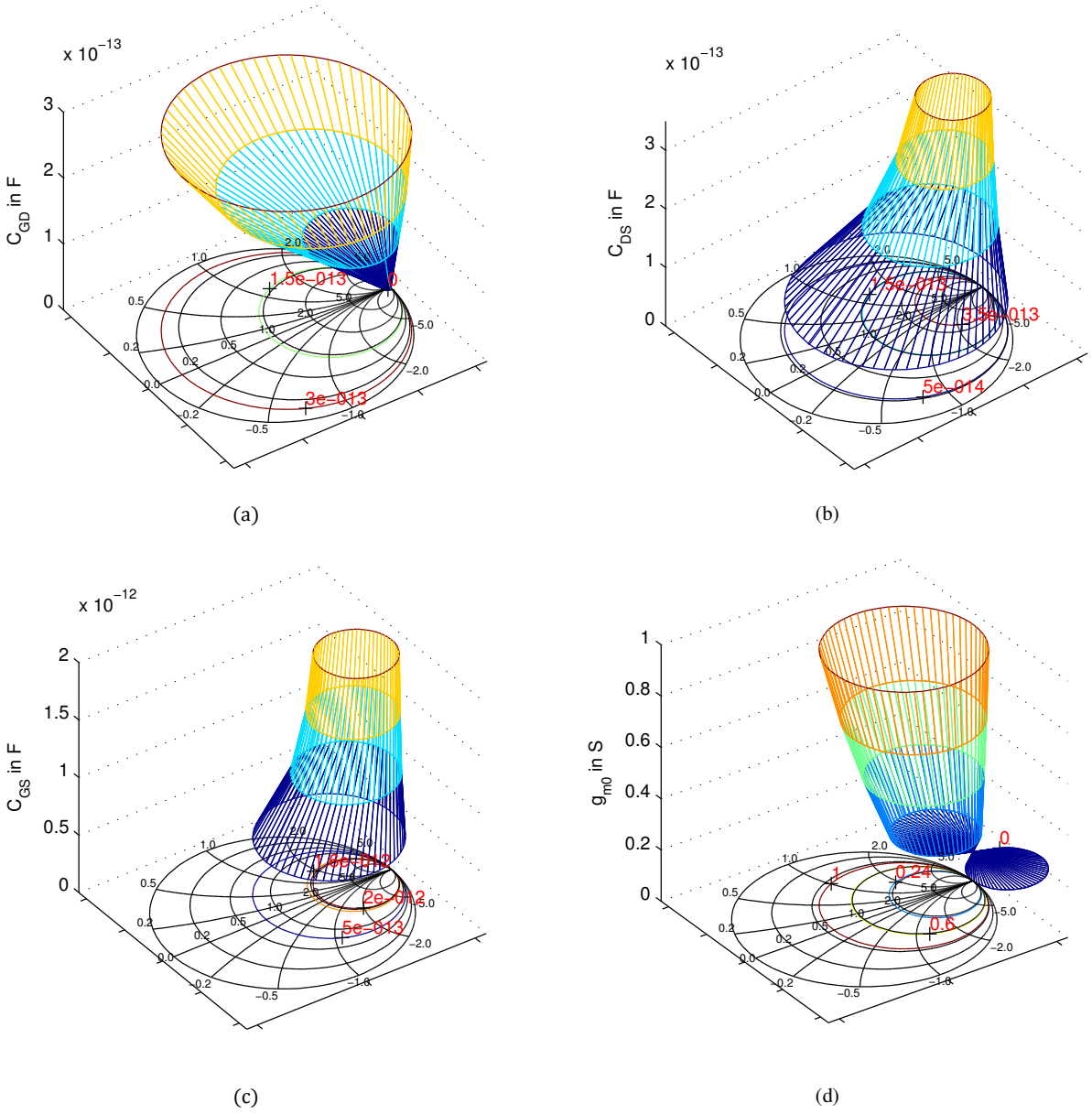


Fig. 6-8: Source/load stability circles for (a) different C_{GD}, (b) different C_{DS}, (c) different C_{GS} and (d) different g_{m0} of the 8×125µm TD-pair with the HEMT parameters of Table 6-1 and C_{CS} = 0 F at 0.1 GHz

$$|S_{c1c1}| = |S_{c2c2}| = 1 \tag{6.12}$$

As soon as $|S_{c1c1}|$ or $|S_{c2c2}|$ exceed one, the circuit becomes instable, which means for Y_{c1c1} or Y_{c2c2} that

$$Y_{c1c1} = Y_{c2c2} \leq 0. \tag{6.13}$$

Replacement of Y_{GS}, Y_{GD} and Y_{DS} by $Y_{GS} = j\omega C_{GS}$, $Y_{GD} = j\omega C_{GD}$ and $Y_{DS} = j\omega C_{DS}$ in equations (6.1) or (6.4) and rearranging the terms for the condition derived in equation (6.13), the following dependency of C_{GD} on C_{DS} or vice versa can be deduced (see Appendix F.1 for derivation).

$$C_{GD} \geq \sqrt{C_{DS} \cdot \frac{C_{GS}}{Re\{Z_0\} g_m}} \quad or \quad C_{DS} \leq \frac{{C_{GD}}^2 g_m Re\{Z_0\}}{C_{GS}}. \tag{6.14}$$

Inclusion of the resistive elements R_{GS}, R_{GD} and R_{DS} of the HEMT in the analysis only mitigates the worst case condition for the stability relationship between C_{GD} and C_{DS} and unnecessarily complicates computation. Thus, it is meaningful to omit the resistive elements in the analysis. From (6.14) it additionally emerges that the strict relationship between C_{GD} and C_{DS} becomes more relaxed the larger Z_0 or g_m gets.

The plot in Fig. 6-9 shows the boundary condition of equation (6.14) for the dependency of C_{GD} on C_{DS} for different g_m with the 8×125µm HEMT parameters given in Table 6-1. The area enclosed by the abscissa and the curve highlights the region, where any combination of C_{GD} and C_{DS} leads to instable circuit performance for Z_0 = 50 Ω. Vice versa, values located above the curves deliver stable common-mode performance.

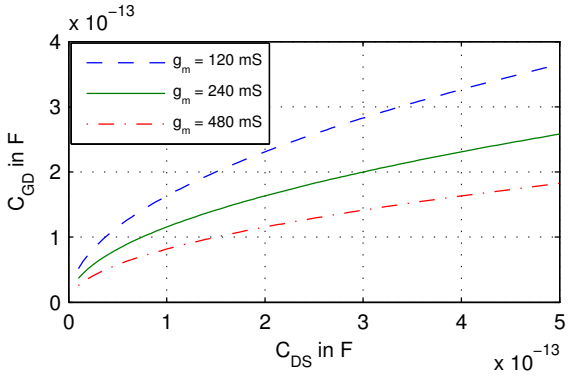
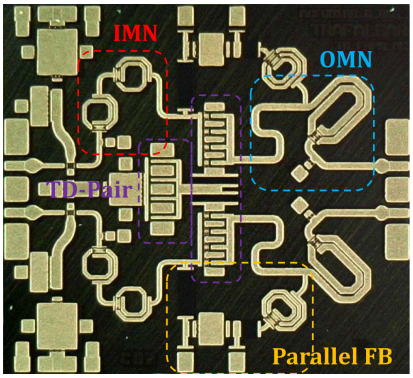


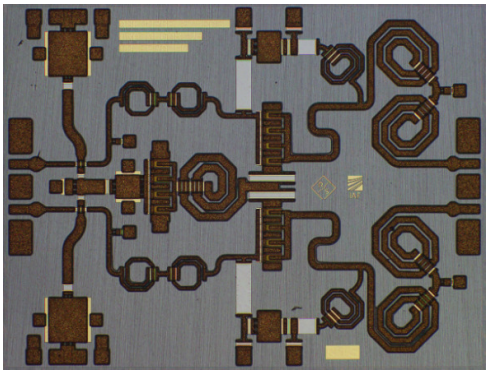
Fig. 6-9: C_{GD} vs. C_{DS} stability dependence for different g_m of a 8×125µm TD-pair in common-mode operation for C_{CS} = 0 F and Z_0 = 50 Ω

6.2 Stability Investigation of a DC – 6 GHz Truly-Differential FBPA

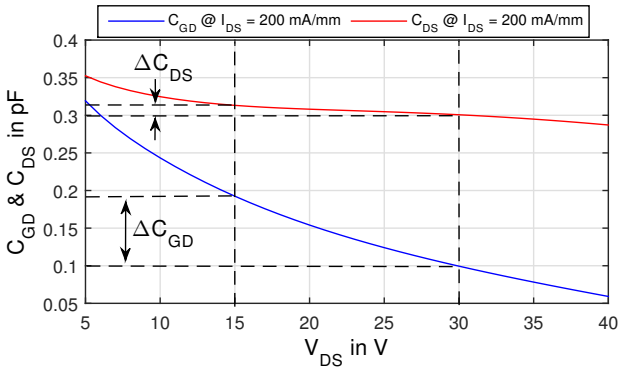
Transferring the above obtained knowledge to a differential feedback based design leads to the important design consideration, that small-signal CM-matching is a crucial design criterion to obtain stability of the whole amplifier and should hence be scrutinized in detail. Therefore, the first TD-FBPA design from chapter 4.7.4 is used to further investigate the stability of a matched TD-pair with parallel resistive feedback. Since the analysis from 6.1.3 revealed that the common-mode stability is dependent on the C_{DS}/C_{GD}-ratio, combined with the knowledge that C_{GD} is strongly dependent on V_{DS} in GaN, leads to the conclusion that the stability of the amplifier can be controlled by adjusting V_{DS}. Fig. 6-10 (c) sketches the dependency of C_{GD} and C_{DS} on V_{DS} for a 8×125µm common-source HEMT. A variation in V_{DS} from 30 V to 15 V approximately doubles C_{GD} but has only a minor effect on C_{DS}. Thus, by reducing V_{DS} the necessary common-mode stability requirement derived in (6.14) can be fulfilled. Fig. 6-10 (a) shows the chip photograph of the first design version "Trafalgar V1" of the DC - 6 GHz TD-FBPA from chapter 4.7.4.



(a)



(b)

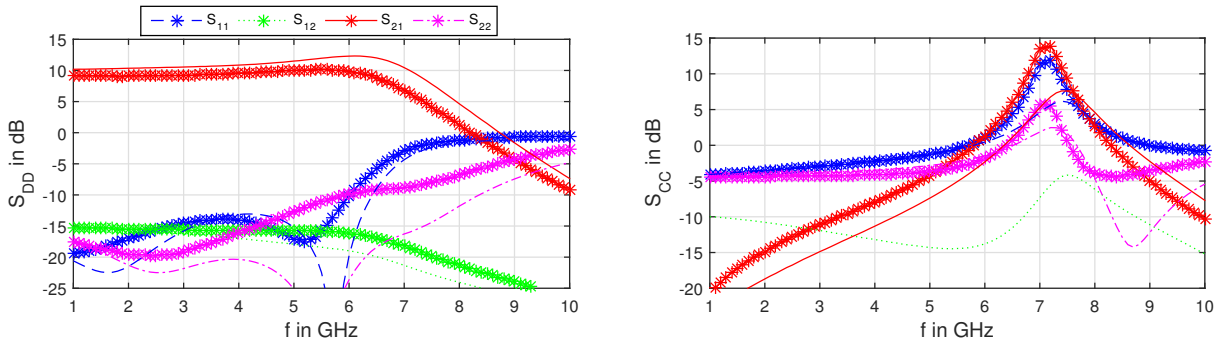


(c)

Fig. 6-10: Die photograph of the TD-FBPA GaN MMIC (a) "Trafalgar V1" (2.40 × 2.65 mm^2) and (b) "Trafalgar V2" (3.15 × 2.4 mm^2). (c) Dependence of C_{GD} and C_{DS} vs. V_{DS} for a 8×125µm common-source HEMT.

Besides the differential topology, which enables to eliminate even-order nonlinearities, series- as well as parallel-feedback was applied to obtain flat gain and good input and output matching performance towards low frequencies. Additional peaking inductors were included in the parallel feedback paths in order to reduce the

amount of feedback at the upper band edge. There are two striking differences besides the difference in the I/O-MNs between the two chip versions in (a) and (b). First, an additional inductor/coil at the virtual ground node in series to the TCS-HEMT is placed in the "Trafalgar V2" design, which serves to compensate for the output capacitance of the TCS-HEMT at 6 GHz. Second, the gate-source field-plates in the amplifying HEMTs of the "Trafalgar V2" design were omitted, which helps to significantly decrease C_{DS} and C_{GS} by almost 50 % whereas C_{GD} stays almost constant. In this way the f_T is almost doubled and the necessary boundary condition for conditional CM-stability from (6.14) becomes more relaxed.



(a) (b)

Fig. 6-11: (a) Differential (S_{DD}) and (b) common-mode (S_{CC}) S-parameter of the simulated (-.) and measured on-wafer (*) DC - 6 GHz TD-FBPA "Trafalgar V1" for V_{DD} = 22 V and I_{DS} = 200 mA/mm (V_{DS1} = 7 V, V_{DS2} = 15 V)

Omission of the inductive compensation led to significant CM-gain above the upper band edge at 7 GHz in the first chip version "Trafalgar V1", as the simulation and measurement results in Fig. 6-11 (a) reveal for the reduced bias-point of V_{DD} = 22 V. Any further increase in V_{DD} above 22 V and thus V_{DS2} above 15 V for the amplifying HEMTs, results in an oscillation of the whole TD-FBPA. This behavior is in close relation to the findings on the necessary $C_{\mathrm{DS}}/C_{\mathrm{GD}}$-ratio to obtain CM-stability from section 6.1.3. It needs to be considered that the introduction of parallel feedback relaxes the requirement given in (6.14) but does not necessarily make the TD-FBPA unconditionally stable, which more or less depends on the amount of applied feedback. Since the design proved to be unconditionally stable up to V_{DD} = 40 V under differential excitation, the increase in CM-gain with frequency due to the output capacitance of the TCS-HEMT is deemed to be the major cause for oscillation of the whole TD-FBPA at the upper band edge. The most effective countermeasure to suppress the increase in CM-gain toward 7 GHz proved to be the incorporation of a TCS-inductor ($L_{\mathrm{DS},comp}$), which helps to resonate out the capacitance of the TCS-HEMT towards ground at the band edge. In a similar fashion plays the device size of the TCS-HEMT therefore also an important role in terms of CM-stability, because $C_{\mathrm{DS},TCS}$ of the TCS-HEMT should be kept as small as possible to keep the resonance frequency $\omega_{TCS} = 1/\sqrt{C_{\mathrm{DS},TCS} L_{\mathrm{DS},comp}}$ out of band. As presented in chapter 6.1.1, an increase in $C_{\mathrm{DS},TCS}$ leads to a higher instability at low frequencies and lowers the useable BW, where the $CMRR$ is still sufficiently high to suppress the CM-gain within the band. Out of this reason, the device size of the TCS-HEMT should be minimized, such that on the one hand the targeted drain current for the TD-pair HEMTs can be provided and properly controlled by the TCS-HEMT and on the other hand its maximum DC power density of around 7 W/mm is not exceeded. Based on the fact that the TCS-HEMT operates close to its knee-voltage and is thus able to provide a higher drain current, which can reach up to 600 mA/mm without thermally destroying the device, the device size for the TCS-HEMT does not have to be

twice the size of the TD-pair HEMT but rather can be of equal device size, as the redesign in Fig. 6-10 (b) depicts. This helps to minimize the parasitic capacitance $C_{\mathrm{DS},TCS}$ toward ground of the TCS-HEMT and thus improves CM-stability and the $CMRR$ of the design. Another approach to reduce $C_{\mathrm{DS},TCS}$ is the use of cascodes, where the effective output capacitance is slightly lower than in a CS-HEMT. Unfortunately, the reduction in capacitance is not very large, which does not justify the necessary increased supply voltage and the increased dissipated power of a cascode-TCS, so that cascodes were not used for the final implementation of the TCS in the TD-FBPA design.

6.3 Conclusion

The theoretical stability analysis of a PD- and TD-pair within this chapter revealed that especially TD-pairs are prone to common-mode (CM) oscillations. With increasing output conductance ($g_{\mathrm{DS},TCS}$) and output capacitance ($C_{\mathrm{DS},TCS}$) of the tail-current-source (TCS) HEMT, the CM-stability condition of the TD-pair becomes more relaxed and approximates more and more the characteristic of the PD-pair, which is in general equal under differential and common-mode excitation. For very small values of $g_{\mathrm{DS},TCS}$ and $C_{\mathrm{DS},TCS}$, the intrinsic HEMT parameter ratios between C_{GS}, C_{GD}, C_{DS} and g_m in the differential stage start to play a decisive role for the CM-stability. Therefore, the following theoretical low frequency dependency between the intrinsic HEMT parameters and the environment impedance Z_0 was derived, which marks the boundary condition for achieving conditional CM-stability (μ and $\mu' > 0$).

$$C_{\mathrm{GD}} \geq \sqrt{C_{\mathrm{DS}} \cdot \frac{C_{\mathrm{GS}}}{Re\{Z_0\} g_m}} \tag{6.15}$$

From (6.15) it emerges that the condition becomes more relaxed with a higher f_T of the utilized process, assuming that the f_T is mainly dominated by g_m and C_{GS}. Under a 50 Ω environment, a TD-pair implemented in the GaN25 technology exhibits stability measures (μ and μ') which are smaller than zero. Thus, the TD-pair is always instable for $Z_0 = 50$ Ω. The main reason for the instability was found to be the small fraction of feedback capacitance (C_{GD}) compared to the input (C_{GS}) and output (C_{DS}) capacitance present in GaN technology. By increasing C_{GD} by roughly 50 % in a 8×125µm device, CM-stability in a TD-pair with $Z_0 = 50$ Ω can be already obtained. Another effective stabilization measure instead of increasing C_{GD} is to apply parallel feedback. This approach was already chosen in the design of the DC-6 GHz TD-FBPA in chapter 4.7.4, which automatically stabilizes the TD-pair in CM at low frequencies. Nevertheless, due to the finite $C_{\mathrm{DS},TCS}$ of the TCS-HEMT in a real design, the CM-gain increases and accordingly the $CMRR$ decreases over the frequency band. Dependent on the TCS-HEMT's device size this might even lead to CM-oscillations at the upper band edge based on the present high CM-gain. One effective remedy is to minimize the TCS-HEMT's device size and therewith $C_{\mathrm{DS},TCS}$. A further countermeasure is the compensation of $C_{\mathrm{DS},TCS}$ by a series inductance $L_{\mathrm{DS},comp}$ at the upper band edge, which suppresses the increasing CM-gain and thus keeps the $CMRR$ sufficiently high.

The most effective measures for guaranteeing CM-stability in GaN-technology are summarized once again:

- Use GaN process with highest available f_T
- Avoid HEMTs with gate-source field-plates to minimize C_{GS} and C_{DS}
- Choose smallest possible device size for TCS-HEMT
- Use cascodes in TCS (if power dissipation is not of concern)
- Apply parallel feedback to mask / bypass C_{GD}
- Add series inductance to compensate / resonate-out $C_{\mathrm{DS},TCS}$ of TCS-HEMT

Not all of the above mentioned CM-stabilization measures need to be applied necessarily simultaneously in one single design. Which concrete measure to use is strongly related to the given requirements of the TD-PA.

FINAL CONCLUSION AND OUTLOOK

The overall goal of this work was the implementation of multi-decade broadband PA topologies in GaN technology, which are suitable for the application within T&M instruments. In contrast to the class of narrow-band PAs used in mobile communications, which leveraged GaN technology in the last five years due to its higher efficiency and chip size compactness, broadband PAs applied in measurement instruments are on top of their output power mainly assessed by their linearity and noise performance. Because of this reason, the core of this work was dedicated to the investigation of suitable on-chip linearization and noise reduction schemes for the realization of multi-decade broadband PAs implemented in AlGaN/GaN on s.i. SiC technology. The two most promising PA topologies, namely the resistive feedback PA (FBPA) and the traveling-wave amplifier (TWA), which are able to operate over multiple decades from DC up to several GHz, were analyzed in detail with respect to matching, output power, linearity and noise performance within this work.

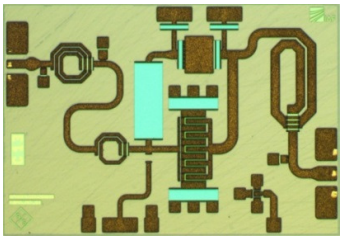
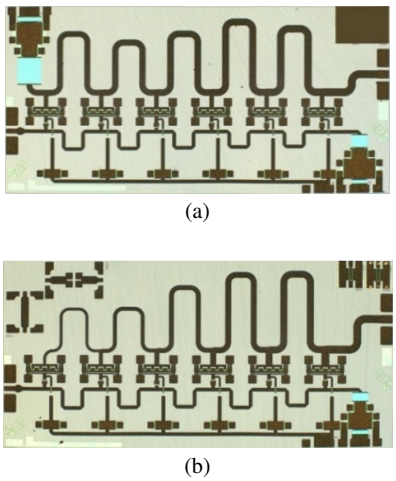


Fig. 6-12: Photograph of DC-6 GHz GaN FBPA "Futago V3"

By means of a DC-6 GHz single-ended FBPA in 0.25µm AlGaN/GaN technology from the Fraunhofer IAF, the performance trade-offs of FBPAs have been verified also by hardware measurements. The FBPA "Futago V3" showed a very flat but slightly increasing gain from 9 dB to 11 dB, which is in general a desired characteristic for PAs in T&M instruments in order to compensate for the increasing losses of the upstream or subsequent switches in the system architecture toward higher frequencies. With a P_{sat} of 36 dBm and a corresponding P_{1dB} of 33 dBm, high output power with good linearity could be obtained at the same time. Moreover, the linearity measurements revealed a HD of better than -36 dBc at P_{out} = 25 dBm and an $OIP3$ of better than 41 dBm. Together with the NF results of smaller than 6 dB at 6 GHz and 3.5 dB toward DC, the combined outstanding performance of the FBPA in frequency operation down to DC, gain flatness, linearity and low-noise at the same time, makes this topology the optimum choice for the application in signal generators, operating down from a few kHz up to several GHz.



(a)

(b)

Fig. 6-13: Photograph of DC-15 GHz GaN (a) UDPA "Unzen" and (b) NDPA "Nasu"

If higher BWs are targeted in the application, the distributed or traveling-wave topology (TWA/DPA) proves to exhibit best wideband performance. A DC–15 GHz uniform ("Unzen") as well as non-uniform ("Nasu") distributed power amplifier (UDPA/NDPA) were implemented in the same 0.25 GaN technology, achieving a flat gain with a maximum ripple of $\pm$ 0.5 dB at 10 dB of gain and better than 8 dB of $I/O\text{-}RL$ over the full band. The P_{3dB} and P_{1dB} have been measured over the full band to be larger than 35 dBm and 32 dBm, respectively. Comparison of the UDPA with the NDPA yielded a slightly superior output power and gain performance of the NDPA, since no portion of the output power gets dissipated in the drain-dumping load. Although, based on the absence of the drain-dumping load, a slightly worse ORL together with a higher gain ripple is the result. In terms of linearity both circuits exhibit high linearity with an HD of lower than -40 dBc at P_{out} = 25 dBm up to 13 GHz. The HD measurements of the NDPA showed again to be slightly better

than of the UPDA, which is owed to the much better load-line matching of the first stages due to the missing drain-dumping load. This coherency was also investigated in detail analytically, proving the present inherent mismatch of the load in the 1st stage in a UDPA, where the load-line even starts to tilt into the passive region the more ideal the design becomes. On top, the NF measurement of the two TWAs showed a strong rise toward DC, with a minimum of 3.5 dB at around 3.5 GHz. After conducting a detailed analytically investigation of the TWA noise, the cause for the low frequency rise in noise was identified to come from the gate-bias resistors on the one hand and from the gate-line termination resistor on the other. The former noise contribution is only present, when capacitive gate-coupling is applied in the design, whereas the latter is caused by the reverse transfer function from the gate-line termination to the output.

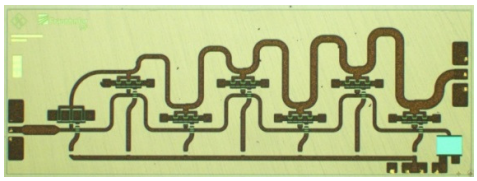


Fig. 6-14: Photograph of 0.5-20 GHz GaN NDPA "Namazuwa"

To fully bail out the maximum frequency of the GaN25 process, a 0.5 GHz to 20 GHz non-uniform TWA was also implemented with a targeted gain of 9 dB and a P_{sat} of larger than 33 dBm. In order to minimize thermal coupling between the active devices, the HEMTs were shifted in their positions in form of a zig-zag path. The measurements showed excellent linearity with a HD < -40 dBc up to 12 GHz at P_{out} = 20 dBm and an $OIP3$ of greater than 44 dBm up to 20 GHz, which is deemed to be an outstanding linearity performance for a broadband TWA in a 0.25µm GaN technology, which is designed up to $2f_T/3$.

Based on the high requirements in T&M instruments for a low NF at low frequencies and high one-tone and multi-tone linearity, different noise reduction and linearization concepts capable of operating over multiple decades were examined and the most promising ones implemented in chapter 3 and chapter 5.

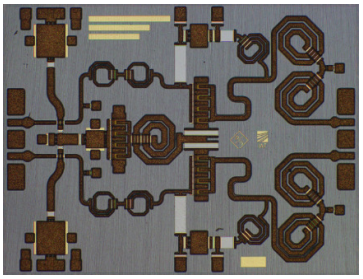


Fig. 6-15: Photograph of DC-6 GHz GaN TD-FBPA "Trafalgar V2"

For the linearization of the FBPA, a truly-differential (TD) design concept was applied for the first time in GaN in order to further improve the DR of the DC–6 GHz FBPA. Due to the inherent even-order harmonic cancellation in differential amplifiers, the 2nd harmonic could be suppressed below the 3rd harmonic, giving an increased $SFDR$. The measurements showed for the DC–6 GHz TD-FBPA design an improvement of more than 25 dB down to -60 dBc in $HD2$ at P_{out} = 25 dBm and more than 10 dB down to -55 dBc in $SFDR$. Above all, two-tone intermodulation measurements revealed additionally a very high $OIP3$ of larger than 46 dBm at 6 GHz and even 51 dBm at 1 GHz. Power measurements showed a P_{1dB} of larger than 31 dBm at a nominal bias of V_{DD} = 36 V, V_{GG2} = 6 V and I_{DD} = 200 mA/mm, whereas the maximum output power is confined by the tail current-source (TCS), which imprints a constant supply current in a TD-FBPA. In order to gain the full output power, the gate-voltage of the TCS-HEMT needs thus to be adjusted to class A. Despite this limitation, the TCS-HEMT enables on the other hand the exact control of I_{DD}, which is often adjusted by additional on-board control circuitry in T&M instruments to compensate for thermal variations or aging effects. Therefore, by making use of a TD-circuit concept, control complexity could be minimized at the expense of an increased DC power due to the stacking of two HEMTs. Not addressed so far is the sensitivity of TD-pairs to common-mode oscillations in GaN technology. A detailed analytical analysis revealed that the cause for this unstable common-mode behavior is the very large intrinsic capacitance ratio of C_{DS} to C_{GD}, which is characteristic for GaN. The higher the $CMRR$

of the TD-circuit is, the more unstable becomes the circuit. For the ideal case of an ideal tail current source (TCS), a TD-pair under 50 Ω behaves always unstable in common-mode at low frequencies. Fortunately, implementation of a TCS in GaN technology alleviates this condition based on its "relatively" high output conductance, which is typical for III-V semiconductors. Another remedy is the use of parallel resistive feedback, as applied in the TD-FBPA, which bypasses C_{GD} and hence stabilizes the TD-circuit at low frequencies. Furthermore, in order to avoid unstable behavior at the upper band edge, which might be caused by the increasing common-mode gain over the band, it is beneficial to incorporate a series tail-inductor to the TCS-HEMT, which compensates the output capacitance of the TCS-HEMT at the band edge and therewith counteracts the increasing common-mode gain. Also, omission of the gate field-plates helps in general to relax the overall stability requirements in terms of the intrinsic C_{GD} to C_{DS} and C_{GS} capacitance ratios.

In the next step, a further improvement in linearity could be obtained by the combination of two class B biased TD-FBPA designs. On top of the even-order harmonic cancellation, the class B bias eliminates all odd-order harmonics, giving high linearity. Unfortunately, a class B amplifier suffers from 6 dB less power gain, which would be equal to a 16 dB design for the current 10 dB TD-FBPA. This would end up in a significant frequency limitation for such a design. Nevertheless, it might be desirable for a quick evaluation of the degree of linearity improvement to combine two TD-FBPAs by means of a Wilkinson power combiner on a PCB in a first step.

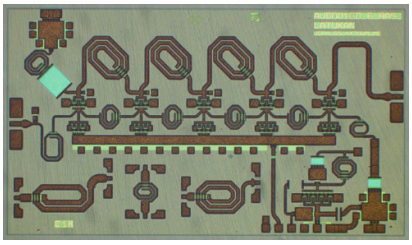


Fig. 6-16: Photograph of DC-6.5 GHz GaN L²NTWA "Latukan"

Another linearization approach for TWAs, the so called nonlinear diode predisortion concept, targets the compensation of the nonlinearity introduced by the space-charge capacitor C_{GS} and has been applied for the first time in a distributed structure. By placing anti-parallel diodes with an invers V_{GS}-dependence in each stage of the TWA, the resulting total input capacitance becomes almost independent of V_{GS}, but is at the same time effectively doubled. The latter represents the only drawback of this concept, which leads to an effectively halved BW. This is deemed to be an acceptable sacrifice due to the very high intrinsic BW of TWAs. The analysis additionally revealed that the nonlinearity introduced by C_{GS} increases with increasing frequency due to the rising displacement current. Out of this reason, the linearization takes especially effect toward the upper band edge. The proof of concept was done by means of a DC-6.5 GHz linear low-noise TWA (L²NTWA) design, achieving a gain of 15 dB and up to 33 dBm of saturated output power. The high linearity especially at the upper band was verified by two-tone intermodulation measurements, showing an $OIP3$ of larger than 42 dBm over the whole band. Single-tone HD measurements also underline the high linearity of the design with an HD of smaller than -38 dBc at an output power of 20 dBm. NF measurements indicate that a classification of the design as high power LNA is suitable. With a minimum of 1.8 dB at around 2 GHz, the L²NTWA exhibits an extremely low noise performance with a P_{1dB} of larger than 29 dBm and the before mentioned high linearity at the same time. Since no capacitive gate-coupling is applied in the design, solely the increase in NF up to 5.5 dB owed to the gate-line termination resistor needs to be tackled.

For this reason, three different active cold load (ACL) concepts were investigated more closely and among these (common-gate (CG), common-source with series inductive feedback (CS-SIF) and common-source with parallel resistive feedback (CS-PRF)), the CS-PRF ACL proved to be the best candidate for the reduction of the low frequency NF in TWAs due to its outstanding low frequency noise suppression of better than -180 dBm/Hz.

Moreover, two different possibilities exist for the placement of the ACL in a TWA. Either the ACL substitutes the gate-line termination resistor R_{GT} or it replaces the last amplifying stage in the TWA to terminate the gate-line, whererby R_{GT} is simply omitted. The former solution exhibits the best low frequency NF, but degrades also output matching and gain at the same time, whereas the latter solution does not affect output matching and gain, but the NF is slightly higher. This is the preferred solution, since the general TWA topology is maintained and thus the electrical output power performance not altered. As the ACL concept analysis revealed, the input impedance of the CS-PRF ACL can only be kept constant for a certain frequency range, which is dependent on the actual device size. In order to minimize the noise at low frequencies it is desirable to take the largest possible device size, which offers enough gain up to the corner frequency, wherefrom the NF starts to rise significantly. Since above this corner frequency the gain starts to drop noticeably, the input impedance changes also accordingly, which in turn was compensated by an upstream RLC-filter. The resulting combination of the CS-PRF ACL together with the RLC-filter is also called "blue-noise" active termination (BNAT) due to the analogy of the high frequency noise shaping to the optical spectrum of blue light. The measurements of the L²NTWA with a 8×100µm device in the BNAT showed a NF improvement at 100 MHz of 1.9 dB from 5.5 dB with R_{GT} to 3.6 dB with BNAT. The general small-signal performance of the L²NTWA has not been altered, except for deviations in the input match based on process variations of the active device in the BNAT. The results nevertheless prove for the first time that the BNAT enables the design of low-noise TWAs in GaN technology compensating the well known NF "bathtub"-shape of conventional TWAs.

The impact of the BNAT on the TWA's linearity could not be fully covered within this work, but needs to be investigated in the future. It can be generally stated that the larger the device-size ratio between the HEMT in the BNAT and the HEMTs in the active TWA stages is, the lower is the degradation of the overall TWA's linearity for larger drive signals. This relationship is simply owed to the larger back-off operation of the BNAT HEMT, which leads to a lower introduction of spurious harmonics onto the gate-line.

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APPENDIX A

The Y-parameter matrix of the simplified FBPA from Fig. 3-30 (a) at DC can be computed to

$$\underleftrightarrow{Y}_{FBPA} = \begin{bmatrix} \frac{1}{R_{fp}} & -\frac{1}{R_{fp}} \\ -\frac{1}{R_{fp}} + \frac{g_{m0}R_{DS}}{R_{fs} + R_{DS}(1 + g_{m0}R_{fs})} & \frac{1}{R_{fp}} + \frac{1}{R_{fs} + R_{DS}(1 + g_{m0}R_{fs})} \end{bmatrix}. \quad \text{(A.1.0)}$$

A.1. Computation of Series- and Parallel Feedback Resistance for Constant S21

Insertion of (A.1.10) into (3.21) yields R_{fp} for a given S_{21} equal to

$$R_{fp,S21} = \frac{2Z_0(1 - S_{21})\left(R_{fs} + R_{\mathrm{DS}}(1 + g_{m0}R_{fs})\right) - S_{21}{Z_0}^2(1 + g_{m0}R_{\mathrm{DS}})}{S_{21}\left(Z_0 + R_{fs} + R_{\mathrm{DS}}(1 + g_{m0}R_{fs})\right) + 2g_{m0}R_{\mathrm{DS}}Z_0} \quad \text{(A.1.1)}$$

and correspondingly for R_{fs}

$$R_{fs,S21} = \frac{R_{fp}(S_{21}(Z_0 + R_{\mathrm{DS}}) + 2g_{m0}R_{\mathrm{DS}}Z_0) + S_{21}{Z_0}^2(1 + g_{m0}R_{\mathrm{DS}}) + (S_{21} - 1)2Z_0R_{\mathrm{DS}}}{\left(2Z_0(1 - S_{21}) - R_{fp}S_{21}\right)(1 + g_{m0}R_{\mathrm{DS}})} \quad \text{(A.1.2)}$$

If R_{DS} is sufficiently high, $R_{fp,S21}$ and $R_{fs,S21}$ can be approximated very well for $R_{\mathrm{DS}} \to \infty$ by

$$R_{fp,S21} = \frac{2(1 - S_{21})\left(1 + g_{m0}R_{fs}\right) - g_{m0}Z_0S_{21}}{\frac{S_{21}}{Z_0}\left(1 + g_{m0}R_{fs}\right) + 2g_{m0}} \quad \text{(A.1.3)}$$

and

$$R_{fs,S21} = \frac{R_{fp}(S_{21} + 2g_{m0}Z_0) + 2Z_0\left(1 - S_{21}\left(\frac{g_{m0}Z_0}{2} + 1\right)\right)}{g_{m0}S_{21}\left(R_{fp} - 2Z_0\right) + 2g_{m0}Z_0}. \quad \text{(A.1.4)}$$

A.2. Computation of Series- and Parallel Feedback Resistance under Constant S11 and S22

Similarily, for a given S_{11} and S_{22}, R_{fp} results in

$$R_{fp,S11} = \frac{(1+S_{11})(1+g_{m0}R_{\mathrm{DS}}){Z_0}^2 + 2Z_0S_{11}\left(R_{fs}+R_{\mathrm{DS}}\left(1+g_{m0}R_{fs}\right)\right)}{(1-S_{11})\left(Z_0+R_{fs}+R_{\mathrm{DS}}\left(1+g_{m0}R_{fs}\right)\right)} \tag{A.2.1}$$

$$R_{fp,S22} = \frac{(1+S_{22})(1+g_{m0}R_{\mathrm{DS}}){Z_0}^2 + 2Z_0S_{22}\left(R_{fs}+R_{\mathrm{DS}}\left(1+g_{m0}R_{fs}\right)\right)}{(1-S_{22})\left(R_{fs}+R_{\mathrm{DS}}\left(1+g_{m0}R_{fs}\right)\right) - Z_0(1+S_{22})}. \tag{A.2.2}$$

and R_{fs} in

$$R_{fs,S11} = \frac{(1+S_{11})(1+g_{m0}R_{\mathrm{DS}}){Z_0}^2 - R_{fp}(1-S_{11})(Z_0+R_{\mathrm{DS}}) + 2Z_0R_{\mathrm{DS}}S_{11}}{\left((1-S_{11})R_{fp}-2Z_0S_{11}\right)(1+g_{m0}R_{\mathrm{DS}})} \tag{A.2.3}$$

$$R_{fs,S22} = \frac{(1+S_{22})(1+g_{m0}R_{\mathrm{DS}}){Z_0}^2 - R_{fp}((1-S_{22})R_{\mathrm{DS}} - (1+S_{22})Z_0) + 2Z_0R_{\mathrm{DS}}S_{22}}{\left((1-S_{22})R_{fp}-2Z_0S_{22}\right)(1+g_{m0}R_{\mathrm{DS}})}. \tag{A.2.4}$$

If again R_{DS} is sufficiently high, $R_{fp,S11/22}$ and $R_{fs,S11/22}$ can be approximated very well for $R_{\mathrm{DS}} \to \infty$ by

$$R_{fp,S11/22} = \frac{2Z_0S_{11/22}\left(1+g_{m0}R_{fs}\right) + g_{m0}{Z_0}^2(1+S_{11/22})}{\left(1-S_{11/22}\right)\left(1+g_{m0}R_{fs}\right)} \tag{A.2.5}$$

and

$$R_{fs,S11/22} = \frac{g_{m0}{Z_0}^2\left(1+S_{11/22}\right) + 2Z_0S_{11/22} + R_{fp}(S_{11/22}-1)}{g_{m0}\left(\left(1-S_{11/22}\right)R_{fp}-2Z_0S_{11/22}\right)}. \tag{A.2.6}$$

APPENDIX B

B.1. Noise Parameter Derivation from Correlation Matrices

As H. Hillbrand and P. Russer have derived in their excellent paper [67], the four noise parameters $(F_{min}, |Y_{opt}|, \measuredangle Y_{opt}, R_n)$ can be derived by determination of the equivalent correlation matrix of the noisy HEMT in chain-parameter format equal to

$$\overleftrightarrow{C_A} = \begin{bmatrix} C_{A,11} & C_{A,12} \\ C_{A,21} & C_{A,22} \end{bmatrix} = \begin{bmatrix} < v_n v_n{}^* > & < v_n i_n{}^* > \\ < v_n{}^* i_n > & < i_n i_n{}^* > \end{bmatrix}$$
$$= 4kT_0 \cdot \begin{bmatrix} R_n & \frac{F_{min}-1}{2} - R_n Y_{opt}{}^* \\ \frac{F_{min}-1}{2} - R_n Y_{opt} & R_n |Y_{opt}|^2 \end{bmatrix}. \quad \text{(B.1.1)}$$

It is sufficient to determine C_A of the HEMT and the four noise parameters can be computed from (B.1.1) to

$$F_{min} = 1 + \frac{(C_{A,12} + C_{A,22} Y_{opt}{}^*)}{2kT_0} \quad \text{(B.1.2)}$$

$$Y_{opt} = \sqrt{\frac{C_{A,11}}{C_{A,22}} - \left(Im\left\{\frac{C_{A,12}}{C_{A,22}}\right\} \right)^2} + j \cdot Im\left\{\frac{C_{A,12}}{C_{A,22}}\right\} \quad \text{(B.1.3)}$$

$$R_n = \frac{C_{A,11}}{4kT_0} \quad \text{(B.1.4)}$$

The corresponding noise factor F results hence in

$$F = 1 + \frac{[1 \quad Z_S] \cdot C_A \cdot \begin{bmatrix} 1 \\ Z_S{}^* \end{bmatrix}}{4kT_0 \cdot Re\{Z_S\}}, \quad \text{(B.1.5)}$$

with Z_S being the source impedance. By following the transformation rules given in [67], the HEMT including parasitics can be split up into several building blocks, where each block is described by its noise correlation matrix in the best suited parameter representation, as Fig. B.1-17 depicts. It is worth noting that the the parasitic pad capacitances are not shown, since they can be de-embedded from the model in a first step and do not contribute any thermal noise.

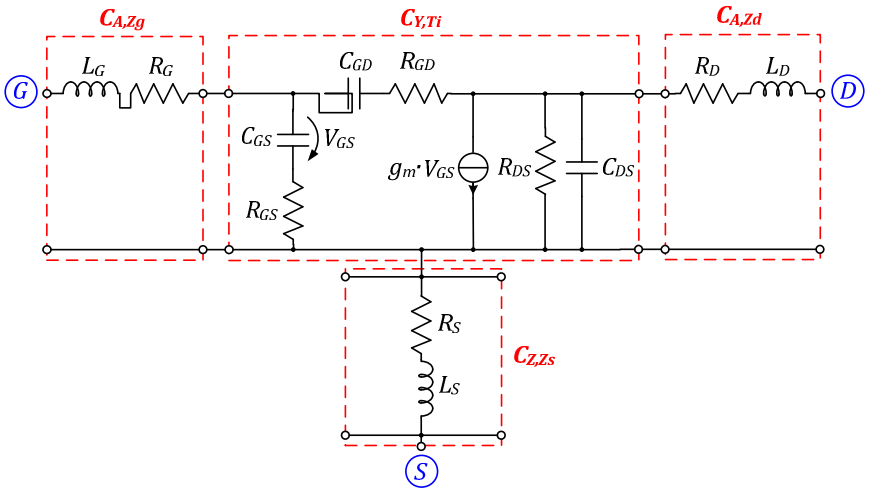


Fig. B.1-17: Schematic of equivalent small-signal noise model of a HEMT split up into its correlation matrices

The following recipe will describe the procedure to derive $\vec{\vec{C}}_A$ by simply following the noise correlation transformation rules from [67]:

Computation of intrinsic transistor noise correlation matrix in Y-parameter representation $\vec{\vec{C}}_{Y,Ti}$ (input/output short-circuit noise currents)

$$C_{Y,Ti} = \begin{bmatrix} < i_G i_G^* > & < i_G i_D^* > \\ < i_G^* i_D > & < i_D i_D^* > \end{bmatrix} \tag{B.1.6}$$

Transformation of $\vec{\vec{C}}_{Y,Ti}$ into Z-parameter reprensentation $\vec{\vec{C}}_{Z,Ti}$ (input/output open-circuit noise voltages) by the transformation

$$\vec{\vec{C}}_{Z,Ti} = \vec{\vec{T}}_{Y\to Z}\vec{\vec{C}}_{Y,Ti}\left(\vec{\vec{T}}_{Y\to Z}\right)^{+} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \vec{\vec{C}}_{Y,Ti} \begin{bmatrix} Z_{11}^* & Z_{21}^* \\ Z_{12}^* & Z_{22}^* \end{bmatrix} \tag{B.1.7}$$

Inclusion of the series feedback parasitic impedance Z_S by simple summation of $\vec{\vec{C}}_{Z,Ti}$ with $\vec{\vec{C}}_{Z,Zs}$ yields

$$\vec{\vec{C}}_{Z,Ti+Zs} = \vec{\vec{C}}_{Z,Ti} + \vec{\vec{C}}_{Z,Zs}. \tag{B.1.8}$$

Transformation into ABCD-parameter representation of $\vec{\vec{C}}_{Z,Ti+Zs}$ from step 3 gives

$$\begin{aligned} \vec{\vec{C}}_{A,Ti+Zs} &= \vec{\vec{T}}_{Z\to ABCD}\vec{\vec{C}}_{Z,Ti+Zs}\left(\vec{\vec{T}}_{Z\to ABCD}\right)^{+} \\ &= \begin{bmatrix} 1 & -A \\ 0 & -C \end{bmatrix} C_{Y,Ti} \begin{bmatrix} 1 & 0 \\ -A^* & -C^* \end{bmatrix}. \end{aligned} \tag{B.1.9}$$

The noise of the extrinsic elements Z_{G} and Z_{D} is included by the transformation rule for the correlation matrices in chain-format, which is defined by

$$\overleftrightarrow{C}_A = \overleftrightarrow{C}_{A1} + \overleftrightarrow{T}_{A1} \cdot \overleftrightarrow{C}_{A2} \cdot \left(\overleftrightarrow{T}_{A1}\right)^{+}. \tag{B.1.10}$$

Insertion of the correlation matrix obtained in step 4 and twofold execution of (B.1.10) in order to include $\overleftrightarrow{C}_{A,Zg}$ and $\overleftrightarrow{C}_{A,Zd}$ gives for the total noise correlation matrix of the HEMT in Fig. B.1-17

$$\overleftrightarrow{C}_A = \left(\overleftrightarrow{C}_{A,Zg} + \overleftrightarrow{T}_{Zg} \cdot \overleftrightarrow{C}_{A,Ti+Zs} \cdot \left(\overleftrightarrow{T}_{Zg}\right)^{+}\right) + \left(\overleftrightarrow{T}_{Zg} \cdot \overleftrightarrow{T}_{Ti+Zs}\right) \cdot \overleftrightarrow{C}_{A,Zd} \cdot \left(\overleftrightarrow{T}_{Zg} \cdot \overleftrightarrow{T}_{Ti+Zs}\right)^{+}. \tag{B.1.11}$$

The noise correlation matrices of the passive parasitics in Y-parameter ($\overleftrightarrow{C}_{Y,Zx}$) or Z-parameter ($\overleftrightarrow{C}_{Z,Zx}$) representation can be simply computed by the corresponding admittance or impedance representations of the two-ports.

$$\overleftrightarrow{C}_{Y,Zx} = 4kT_0 \cdot Re\{\overleftrightarrow{Y}_x\} \quad \wedge \quad \overleftrightarrow{C}_{Z,Zx} = 4kT_0 \cdot Re\{\overleftrightarrow{Z}_x\} \tag{B.1.12}$$

APPENDIX C

C.1. Correlation Between Induced-Gate & Drain Noise-Current for Capacitively-Coupled TWAs

The correlation coefficient of Van der Ziel´s / Pucel´s noise model between induced-gate- and channel-nose can be expressed via [55]

$$\underline{c} = \frac{\overline{\underline{i}_{n,\mathrm{G}}{}^{*} \cdot \underline{i}_{n,\mathrm{D}}}}{\sqrt{\overline{\left|\underline{i}_{n,\mathrm{G}}\right|^2} \cdot \overline{\left|\underline{i}_{n,\mathrm{D}}\right|^2}}}. \tag{C.1.1}$$

The $NCSD$ of the noise current at the output of the k^{th}-stage is according to Fig. 3-41 equal to

$$\begin{aligned} \left|\underline{i}_{n,k}\right|^2 &= \overline{\left|\underline{i}_{n,\mathrm{G}} \cdot \underline{g}_m \cdot \underline{Z}_{\mathrm{G}}(\omega) + \underline{i}_{n,\mathrm{D}}\right|^2} \\ &= \overline{\left|\underline{i}_{n,\mathrm{G}} \cdot g_m \cdot \underline{Z}_{\mathrm{G}}(\omega) + \underline{i}_{n,\mathrm{D}}\right|^2} + \overline{\left|\underline{i}_{n,\mathrm{D}}\right|^2} + \underbrace{2 \cdot Re\left\{\overline{(\underline{i}_{n,\mathrm{G}} \cdot \underline{g}_m \cdot \underline{Z}_{\mathrm{G}}(\omega))^* \cdot \underline{i}_{n,\mathrm{D}}}\right\}}_{C_{i_{n,k}}}, \end{aligned} \tag{C.1.2}$$

where $\underline{Z}_{\mathrm{G}}(\omega)$ is the complex impedance seen by the k^{th}-gate. Replacement of the term in curly braces in (C.1.2) by (C.1.1) yields

$$C_{i_{n,k}} = 2 \cdot \underline{g}_m \cdot Re\{c \cdot \underline{Z}_{\mathrm{G}}(\omega)^*\} \cdot \sqrt{\overline{\left|\underline{i}_{n,\mathrm{G}}\right|^2} \cdot \overline{\left|\underline{i}_{n,\mathrm{D}}\right|^2}} \tag{C.1.3}$$

In equation (C.1.3) $\underline{g_m}$ can be considered to exhibit only a real-part for GaN HEMTs, because τ is with a few ps very small and does not affect noticeably the intrinsic g_m up to several tens of GHz. Finally, since the correlation coefficient $\underline{c}$ of GaN HEMTs can be very well approximated to be only imaginary with $\underline{c} \approx j0.8$, the $Re\{c \cdot \underline{Z}_{\mathrm{G}}(\omega)^*\}$ in (C.1.3) is only existent if $\underline{Z}_{\mathrm{G}}(\omega)$ exhibits an imaginary-part [59, 103]. Since from (C.1.3) it can be inferred that the $Re\{\underline{Z}_G(\omega)^*\}$ does not have any effect on $C_{i_{n,k}}$ due to the purely imaginary correlation coefficient $\underline{c}$, only the $Im\{\underline{Z}_{\mathrm{G}}(\omega)^*\}$ has to be taken into account. The imaginary-part of $\underline{Z}_{\mathrm{G}}(\omega)$ is for low frequencies extremely negative due to the capacitances C_{GS} and C_{C} and strives with increasing frequency towards zero. Hence, the complex conjugate $Im\{\underline{Z}_{\mathrm{G}}(\omega)^*\}$ is positive, giving negative values for $Re\{c \cdot \underline{Z}_{\mathrm{G}}(\omega)^*\}$. Therewith, the noise contribution from $\underline{i}_{\mathrm{n,G}}$ and $\underline{i}_{\mathrm{n,D}}$ is partially cancelled at the output. This takes unfortunately only noticeable effect, where the frequency is large enough to produce significant noise contribution from $\underline{i}_{n,\mathrm{G}}$, since $\underline{i}_{n,\mathrm{G}}$ is increasing with frequency.

C.2. Noise Correlation of Conventional TWAs

If no capacitive gate-coupling is applied, $\underline{Z}_G(\omega)$ can be assumed to be purely real and ideally equal to $Z_0/2$. The correlation term from (C.1.3) therefore yields

$$C_{i_{n,k}} = \underline{g}_m \cdot Z_0 \cdot Re\{\underline{c}\} \cdot \sqrt{\overline{|\underline{i}_{n,\mathrm{G}}|^2} \cdot \overline{|\underline{i}_{n,\mathrm{D}}|^2}}. \tag{C.2.1}$$

Again, with a purely imaginary correlation coefficient $\underline{c}$ for GaN HEMTs $C_{i_{\mathrm{n,k}}}$ becomes equal to zero. It is thus noticeable that additional noise power contributed by correlation between induced-gate noise $\underline{i}_{n,\mathrm{G}}$ and channel-noise $\underline{i}_{n,\mathrm{D}}$ in the output load can be omitted if no series gate capacitors are present in the TWA.

APPENDIX D

D.1. Derivation of Gate- and Drain-Line Propagation Constant

The propagation constant $\gamma = \alpha + j\beta$ of a two-port network refers to the amplitude ratio between the output and the input of the two-port and can thus be expressed by the ABCD-parameters in the following form of [100]

$$e^{-\gamma} = \sqrt{AD} - \sqrt{BC}. \tag{D.1.1}$$

Since the artificial gate- and drain-line constant k-sections are always reciprocal ($S_{12} = S_{21}$ or in terms of ABCD-parameters $AD - BC = 1$), equation (D.1.1) can be rewritten to

$$-\gamma = \ln\left(\sqrt{AD} - \sqrt{AD - 1}\right). \tag{D.1.2}$$

With the mathematical relationship

$$\ln\left(x + \sqrt{x^2 - 1}\right) = cosh^{-1}(x) \;\; ; \; x \geq 1, \tag{D.1.3}$$

equation (D.1.2) can now be expressed by the inverse hyperbolic cosine, giving

$$\gamma = cosh^{-1}\left(\sqrt{AD}\right). \tag{D.1.4}$$

If the following, the general constant k-section in T-shape form is considered, as depicted in Fig. D.1-18.

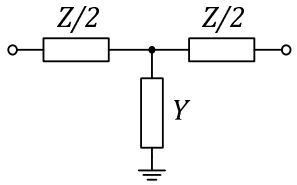


Fig. D.1-18: T-shaped constant k-section

The corresponding $ABCD$-matrix results in

$$ABCD_k = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_k = \begin{bmatrix} 1 + \frac{ZY}{2} & Z\left(1 + \frac{ZY}{4}\right) \\ Y & 1 + \frac{ZY}{2} \end{bmatrix}. \tag{D.1.5}$$

Accordingly, if a T-shaped m-derived section is considered, as depicted below in Fig. D.1-19, the ABCD-matrix can be calculated in a similar fashion. In general there are two different options for the description of a T-shaped m-derived section, depending on the magnitude of m.

(a) (b)

Fig. D.1-19: T-shaped lossy m-derived sections for (a) $m < 1$ and (b) $m > 1$

Calculation of the ABCD-matrix for Fig. D.1-19 (a) with $m < 1$ yields

$$ABCD_{m<1} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{m<1}$$

$$= \begin{bmatrix} 1 + \dfrac{m^2 ZY}{2(1 + (1 - m^2)ZY)} & mZ\left(1 + \dfrac{m^2 ZY}{4(1 + (1 - m^2)ZY)}\right) \\ mY\left(1 + \dfrac{1}{(1 - m^2)ZY}\right) & 1 + \dfrac{m^2 ZY}{2(1 + (1 - m^2)ZY)} \end{bmatrix} \tag{D.1.6}$$

and correspondingly for Fig. D.1-19 (b) with $m > 1$

$$ABCD_{m>1} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{m>1}$$

$$= \begin{bmatrix} 1 + \dfrac{ZY}{2(m^2 + (m^2 - 1)ZY)} & \dfrac{Z}{m}\left(1 + \dfrac{ZY}{4(m^2 + (m^2 - 1)ZY)}\right) \\ \dfrac{Y}{m}\left(1 + \dfrac{m^2}{(m^2 - 1)ZY}\right) & 1 + \dfrac{ZY}{2(m^2 + (m^2 - 1)ZY)} \end{bmatrix}. \tag{D.1.7}$$

It can be simply checked that the matrices (D.1.6) and (D.1.7) reduce to the k-section matrix in (D.1.5) for $m = 1$. In the following, only the case (a), where $m < 1$, will be considered for minimizing calculation overhead. From (D.1.4) the propagation constant for the k-section can now be determined to

$$\gamma_k = cosh^{-1}\left(1 + \frac{ZY}{2}\right) \Leftrightarrow cosh(\gamma_k) = 1 + \frac{ZY}{2} \tag{D.1.8}$$

and accordingly for the m-derived section ($m < 1$) to

$$\gamma_m = cosh^{-1}\left(1 + \frac{m^2 ZY}{2(1 + (1 - m^2)ZY)}\right)$$
$$\Leftrightarrow\ cosh(\gamma_m) = 1 + \frac{m^2 ZY}{2(1 + (1 - m^2)ZY)} \tag{D.1.9}$$

It is desirable to split up the term $cosh(\alpha + j\beta)$ into its real and imaginary-part, which can be obtained by the equivalent mathematical trigonometric expression

$$cosh(\alpha + j\beta) = cosh(\alpha)\, cos(\beta) + j \cdot sinh(\alpha)\, sin(\beta). \tag{D.1.10}$$

For relative small attenuations ($\alpha < 0.4$ Neper/m) the hyperbolic functions can furthermore be approximated by $cosh(\alpha) \approx 1$ and $sinh(\alpha) \approx \alpha$, giving

$$cosh(\alpha + j\beta) = cos(\beta) + j \cdot \alpha \cdot sin(\beta). \tag{D.1.11}$$

By separating the last term in equation (D.1.11) for its real and imaginary-parts gives on the one hand for the real-part

$$Re\{cosh(\alpha + j\beta)\} = cos(\beta), \tag{D.1.12}$$

wherefrom the phase constant β ($[\beta] = 1°$/m per unit section) can be calculated to

$$\beta = cos^{-1}(Re\{cosh(\gamma)\}) \tag{D.1.13}$$

and on the other hand in an analogous manner from the imaginary-part the attenuation constant α ($[\alpha] =$ Np/m per unit section

$$\alpha = \frac{Im\{cosh(\gamma)\}}{sin(\beta)} = \frac{Im\{cosh(\gamma)\}}{\sqrt{1 - \cos(\beta)^2}} = \frac{Im\{cosh(\gamma)\}}{\sqrt{1 - (Re\{cosh(\gamma)\})^2}}. \tag{D.1.14}$$

Expressing the $sin(\beta)$ by $\sqrt{1 - cos(\beta)^2}$ in (D.1.14) enables the reuse of the already calculated term from (D.1.12). Finally, inserting equations (D.1.8) and (D.1.14) into equations (D.1.13) and (D.1.14) leads to the general formulas for the propagation constants of a k- and m-derived section ($m < 1$).

$$\alpha_k = \frac{Im\left\{1 + \frac{ZY}{2}\right\}}{\sqrt{1 - \left(Re\left\{1 + \frac{ZY}{2}\right\}\right)^2}}, \qquad \alpha_m = \frac{Im\left\{1 + \frac{m^2 ZY}{2(1 + (1 - m^2)ZY)}\right\}}{\sqrt{1 - \left(Re\left\{1 + \frac{m^2 ZY}{2(1 + (1 - m^2)ZY)}\right\}\right)^2}}$$

$$\beta_k = cos^{-1}\left(Re\left\{1+\frac{ZY}{2}\right\}\right), \qquad \beta_m = cos^{-1}\left(Re\left\{1+\frac{m^2ZY}{2(1+(1-m^2)ZY)}\right\}\right)$$

(D.1.15) (D.1.16)

D.2. T-shaped lossy constant *k*-section

After derivation of the general dependencies between Z and Y and the phase constant β and attanution coefficient α of a constant k-section in (D.1.15), Z and Y can be replaced by the lossy gate- and drain-line components, as illustrated in Fig. D.2-20.

(a) (b)

Fig. D.2-20: T-shaped lossy k-section of artificial (a) gate- and (b) drain-line

By comparison of Fig. D.1-18 with Fig. D.2-20 (a) and (b), the complex gate and drain-line Z and Y can be derived to

$$Z_G = j\omega L_G \qquad Z_D = j\omega L_D$$

$$Y_G = \frac{j\omega C_{GS}}{1+j\omega R_{GS}C_{GS}} \qquad Y_D = \frac{1}{R_{DS}} + j\omega C_{DS}$$

(D.2.1) (D.2.2)

By insertion of equations (D.2.1) and (D.2.2) into the values for A and D from (D.1.5) and normalization for of the transistor parameter for unit line length, the following expressions for the gate- and the drain-line result

$$1+\frac{Z_G{}'Y_G{}'}{2} = \underbrace{1-\frac{\omega^2 L_G{}'C_{GS}}{2\cdot l_G(1+(\omega C_{GS}R_{GS})^2)}}_{Re\{cosh(\gamma_g)\}} + j\cdot\underbrace{\frac{\omega^3 C_{GS}{}^2 L_G{}'R_{GS}}{l_G(1+(\omega C_{GS}R_{GS})^2)}}_{Im\{cosh(\gamma_g)\}} \qquad \text{(D.2.3)}$$

$$1+\frac{Z_D{}'Y_D{}'}{2}=\underbrace{1-\frac{\omega^2 L_D{}'C_{\mathrm{DS}}}{2\cdot l_D{}^2 R_{\mathrm{DS}}}}_{Re\{cosh(\gamma_d)\}}+j\cdot\underbrace{\frac{\omega L_D{}'}{2\cdot l_D R_{\mathrm{DS}}}}_{Im\{cosh(\gamma_d)\}}. \tag{D.2.4}$$

By finally taking the real- and imaginary-parts of (D.2.3) and (D.2.4) the phase and attenuation constants for the gate- and drain-line, as derived in equation (D.1.15), can be rewritten to

$$\begin{aligned}\alpha_G &= \frac{1}{2}\frac{\omega^2 C_{\mathrm{GS}}R_{\mathrm{GS}}\sqrt{L_G{}'C_{\mathrm{GS}}}}{\sqrt{l_G(1+(\omega C_{\mathrm{GS}}R_{\mathrm{GS}})^2)\left(1-\frac{L_G{}'C_{\mathrm{GS}}}{4\cdot l_G(1+(\omega C_{\mathrm{GS}}R_{\mathrm{GS}})^2)}\right)}}\\ &\approx \frac{1}{2}\omega^2 C_{\mathrm{GS}}R_{\mathrm{GS}}\sqrt{\frac{L_G{}'C_{\mathrm{GS}}}{l_G(1+(\omega C_{\mathrm{GS}}R_{\mathrm{GS}})^2)}}\end{aligned} \tag{D.2.5}$$

$$\begin{aligned}\beta_G &= cos^{-1}\left(1-\frac{\omega^2 L_G{}'C_{\mathrm{GS}}}{2\cdot l_G(1+(\omega C_{\mathrm{GS}}R_{\mathrm{GS}})^2)}\right)\\ &\approx \omega\cdot\sqrt{\frac{L_G{}'C_{\mathrm{GS}}}{l_G(1+(\omega C_{\mathrm{GS}}R_{\mathrm{GS}})^2)}}\end{aligned} \tag{D.2.6}$$

$$\begin{aligned}\alpha_D &= \frac{1}{2}\sqrt{\frac{L_D{}'}{C_{\mathrm{DS}}}}l_D\frac{1}{R_{\mathrm{DS}}l_D\sqrt{1-\omega^2\frac{L_D{}'C_{\mathrm{DS}}}{4\cdot l_D}}}\\ &\approx \frac{1}{2}\sqrt{\frac{L_D{}'}{C_{\mathrm{DS}}}}l_D\frac{1}{R_{\mathrm{DS}}l_D}\end{aligned} \tag{D.2.7}$$

$$\begin{aligned}\beta_D &= cos^{-1}\left(1-\frac{\omega^2 L_D{}'C_{\mathrm{DS}}}{2\cdot l_D}\right)\\ &\approx \omega\cdot\sqrt{\frac{L_D{}'C_{\mathrm{DS}}}{l_D}}\end{aligned} \tag{D.2.8}$$

With

$$\omega_{C,g}=\frac{2}{\sqrt{L_G C_{\mathrm{GS}}}} \qquad \omega_{C,d}=\frac{2}{\sqrt{L_D C_{\mathrm{DS}}}} \tag{D.2.9}$$

$$\omega_{G,g}=\frac{1}{R_{\mathrm{GS}}C_{\mathrm{GS}}} \qquad \omega_{G,d}=\frac{1}{R_{\mathrm{DS}}C_{\mathrm{DS}}} \tag{D.2.10}$$

equations (D.2.5) - (D.2.8) can be expressed in terms of the corner (ω_G) and cut-off frequencies (ω_c) of the gate- and drain-lines, as it is often found in the literature [97, 100].

$$\alpha_G = \frac{\frac{\omega^2}{\omega_{c,G}\omega_G}}{\sqrt{1+\left(\frac{\omega}{\omega_G}\right)^2-\left(\frac{\omega}{\omega_{c,G}}\right)^2}} \tag{D.2.11}$$

$$\beta_G = cos^{-1}\left(1-\frac{2\left(\frac{\omega}{\omega_{c,G}}\right)^2}{1+\left(\frac{\omega}{\omega_G}\right)^2}\right) \tag{D.2.12}$$

$$\alpha_D = \frac{\frac{\omega_D}{\omega_{c,D}}}{\sqrt{1-\left(\frac{\omega}{\omega_{c,D}}\right)^2}} \tag{D.2.13}$$

$$\beta_D = cos^{-1}\left(1-2\left(\frac{\omega}{\omega_{c,D}}\right)^2\right) \tag{D.2.14}$$

APPENDIX E

E.1. Power Gain Approximations for TWAs

It is often meaningful to find a simplified expression for the power gain G_P other than presented in section 3.4.1 in equation (3.75). To come up with a solution it is necessary to determine validity ranges for the power gain approximated formulas. In general, it is a valid assumption that the phase delays on gate- and drain-line are equal ($\beta_G = \beta_D$) striving for maximum bandwidth. If so, a simplified expression for G_P in terms of the gate- and drain-line attenuations per section α_G and α_D can be established, as shown in (E.1.1) below.

$$G_P = \frac{{g_m}^2 Z_G Z_D}{4} \cdot \underbrace{\left| e^{-j\frac{N}{2}\cdot\alpha_D l_D} \right|^2}_{=1} \cdot \left| \frac{[e^{-N\cdot\alpha_D l_D} - e^{-N\cdot\alpha_G l_G}]}{e^{\frac{1}{2}(\alpha_G l_G - \alpha_D l_D)} - e^{-\frac{1}{2}(\alpha_G l_G - \alpha_D l_D)}} \right|^2 \tag{E.1.1}$$

Since the magnitude squared of a complex exponential function is equal to 1, (E.1.1) can be further simplified to

$$G_P = \frac{{g_m}^2 Z_G Z_D}{4} \cdot \underbrace{\left| \frac{[e^{-N\cdot\alpha_D l_D} - e^{-N\cdot\alpha_G l_G}]}{e^{\frac{1}{2}(\alpha_G l_G - \alpha_D l_D)} - e^{-\frac{1}{2}(\alpha_G l_G - \alpha_D l_D)}} \right|}_{TF(G_P)}^2 . \tag{E.1.2}$$

Since usually the attenuation on the gate- and drain-line has to be sufficiently small in the design, first expressing the denominator by a $sinh$-function, as in (3.75), and then approximating the $sinh$-function by the following Taylor-series expansion

$$sinh(x) = x + \frac{x^3}{3!} + \frac{x^5}{5!} + \cdots, \tag{E.1.3}$$

gives the following first order approximation in (E.1.3) for the denominator in (E.1.2)

$$2 \cdot sinh\left(\frac{1}{2}(\alpha_G l_G - \alpha_D l_D)\right) = \alpha_G l_G - \alpha_D l_D \tag{E.1.4}$$

This results in the same approximation as already found by Y. Ayasli *et al.* in [93], which is equal to

$$G_P = \frac{{g_m}^2 Z_G Z_D}{4} \cdot \left(\frac{e^{-N\cdot\alpha_D l_D} - e^{-N\cdot\alpha_G l_G}}{\alpha_G l_G - \alpha_D l_D} \right)^2 . \tag{E.1.5}$$

If furthermore the usually much smaller drain-line attenuation per section is approximated by $\alpha_D = 0$, (E.1.5) leads to

$$G_P = \frac{{g_m}^2 Z_G Z_D}{4} \cdot \left(\frac{1 - e^{-N\cdot\alpha_G l_G}}{\alpha_G l_G} \right)^2 . \tag{E.1.6}$$

In a final step, making again use of the Taylor-series expansion for the exponential function

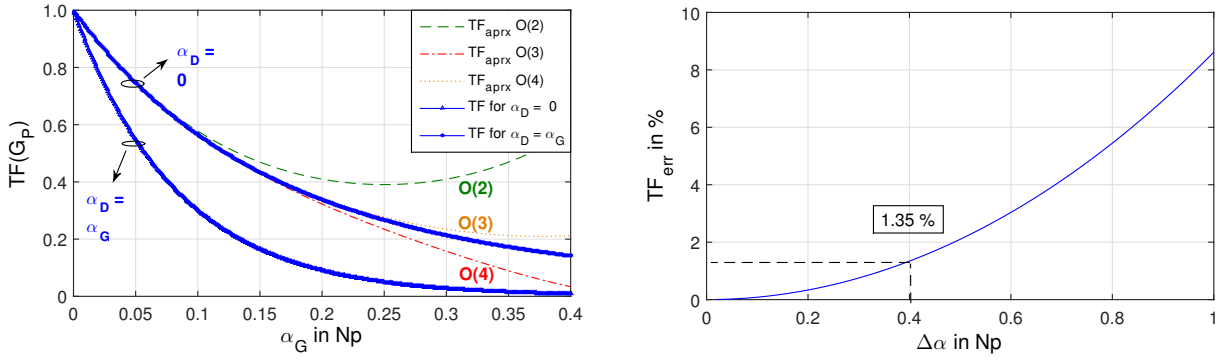
$$e^{-x} = 1 - x + \frac{x^2}{2!} - \frac{x^3}{3!} + \cdots \tag{E.1.7}$$

in (E.1.6) yields

$$G_P = \frac{{g_m}^2 Z_G Z_D}{4} \cdot \underbrace{N^2 \left(1 - \frac{N \cdot \alpha_G l_G}{2!} + \frac{(N \cdot \alpha_G l_G)^2}{3!} - \frac{(N \cdot \alpha_G l_G)^3}{4!} + \cdots\right)^2}_{TF(G_P)}. \tag{E.1.8}$$

Taking expression (E.1.8) up to the second order ($O(2)$), as used by Y. Ayasli *et al.* in [96], is only a valid approximation as long as $\alpha_G < 0.1$ Np, as the comparison of (E.1.8) with (E.1.6) in Fig. E.1-1 (a) depicts. For higher α_G it is necessary to extent the Taylor-series expansion up to third order ($O(3)$) to attain a larger validity range up to $\alpha_G < 0.2$ Np. The graph for $O(4)$ illustrates that taking even higher order terms into account does not necessarily give a better approximation. Important to note is the fact that (E.1.5) is only valid for $\alpha_D = 0$. As soon as the drain-line attenuation per section (α_D) gets in the order of magnitude of the gate-line attenuation per section (α_G), the approximation is not valid anymore.

Fig. E.1-1 (b) shows in addition the variation of (E.1.2) over $\Delta\alpha$ ($= \alpha_G - \alpha_D$) in percent compared to (E.1.5). As soon as the attenuation difference between gate- and drain-line approaches unity, the approximation from (E.1.5) results in a maximum error of 8.6 %. For a difference in attenuation $\Delta\alpha$ of smaller than 0.4 Np, the error introduced by (E.1.5) stays below 1.35 %. This proofs that (E.1.5) is a sufficiently good approximation for (E.1.2) for the design of TWAs.



(a) (b)

Fig. E.1-1: (a) normalized power gain transfer function $TF(G_P)$ vs. gate-line attenuation α_G for (E.1.8) with 2nd, 3rd and 4th order approximation and (b) power gain transfer function error in percent introduced by first order Taylor-series approximation for the $sinh$-function in (E.1.5) compared to (E.1.2)

E.2. Determination of Optimum Number of Stages

Based on the preceding considerations in D.1 regarding the power gain dependence on the gate- and drain-line attenuations per section the optimum number of stages can be derived from (E.1.2), which maximizes the transfer function $TF(G_P)$. Therefore, $TF(G_P)$ has to satisfy the following equation

$$\frac{\delta}{\delta N}\left(\frac{[e^{-N\cdot\alpha_D l_D} - e^{-N\cdot\alpha_G l_G}]}{e^{\frac{1}{2}(\alpha_G l_G - \alpha_D l_D)} - e^{-\frac{1}{2}(\alpha_G l_G - \alpha_D l_D)}}\right) \triangleq 0, \tag{E.2.1}$$

which can be calculated to

$$\alpha_G l_G \cdot e^{-N_{opt}\cdot\alpha_G l_G} = \alpha_D l_D \cdot e^{-N_{opt}\cdot\alpha_D l_D}. \tag{E.2.2}$$

Taking the natural logarithm of (E.2.2) and solving for N_{opt} gives the final solution for the optimum number of stages, which is equal to

$$N_{opt} = \frac{ln(\alpha_D l_D/\alpha_G l_G)}{\alpha_D l_D - \alpha_G l_G}. \tag{E.2.3}$$

APPENDIX F

F.1. Common-Mode Stability of Differential Amplifiers

For the common-mode stability limit of a TD-pair it was shown in chapter 6.1 that as long as $|S_{c1c1}|$ or $|S_{c2c2}|$ stays below one and an ideal constant tail current-source with $Y_{CS} = 0$ S is presumed, the amplifier is stable under Z_0. The stability condition can thus be expressed by

$$\left|S_{\mathrm{c1c1/c2c2}}\right| \leq 1. \tag{F.1.1}$$

with

$$S_{\mathrm{c1c1/c2c2}} = \frac{(1 - {Z_0}^{*} Y_{\mathrm{c1c1/c2c2}})(1 + Z_0 Y_{\mathrm{c2c2/c1c1}}) + |Z_0|^2 Y_{\mathrm{c1c2/c2c1}} Y_{\mathrm{c2c1/c1c2}}}{(1 + Z_0 Y_{\mathrm{c1c1/c2c2}})(1 + Z_0 Y_{\mathrm{c2c2/c1c1}}) - {Z_0}^2 Y_{\mathrm{c1c2/c2c1}} Y_{\mathrm{c2c1/c1c2}}} \tag{F.1.2}$$

and the additional information that the TD-pair is for $Y_{\mathrm{CS}} = 0$ S symmetric, equation (F.1.2) can be rewritten for a real Z_0 to

$$\left|S_{c1c1/c2c2}\right| \leq \left|\frac{1}{1 + 2Z_0 Y_{c1c1}}\right|. \tag{F.1.3}$$

Separation of Y_{c1c1} into real and imaginary-part and rearrangement of the terms in equation (F.1.3) gives the relation

$$Re\{Y_{\mathrm{c1c1}}\} \geq -Z_0 \cdot (Re\{Y_{\mathrm{c1c1}}\}^2 + Im\{Y_{\mathrm{c1c1}}\}^2). \tag{F.1.4}$$

Insertion of the HEMT parameters from equation (6.1) in section 6.1 into (F.1.4) and polynomial sequencing of the form

$$\sum_{q=0}^{p} c_p \omega^q \leq 0 \tag{F.1.5}$$

yields the following polynomial coefficients c_p in Table F.1-1 below.

The magnitude of the single weighting terms $w(p) = \left|c_p\right| \cdot \omega^p$ can be now meaningful assessed by means of the plot in Fig. F.1-2. Neglecting the terms for $p > 2$ leads to no significant error in computation for low frequencies, because the magnitude of all higher order terms is several orders of magnitude smaller and therewith does not impact the result.

Table F.1-1: Polynomial coefficients c_p for common-mode stability

$\boldsymbol{c_2}$	$g_m{}^3\left(C_{GS}C_{DS} - C_{GD}{}^2 g_m Z_0\right)$
c_4	$C_{GS}C_{DS}g_m(C_{GS}+C_{DS})^2 - Z_0[g_m{}^2((C_{GS}C_{DS})^2 + 2(C_{GD}(C_{GS}+C_{DS}) + C_{GS}C_{GD}C_{DS}(C_{GS}+C_{DS}))^2)]$
c_6	$Z_0\left(C_{GD}(C_{GS}+C_{DS})^2 + C_{GS}C_{DS}(C_{GS}+C_{DS})\right)^2$

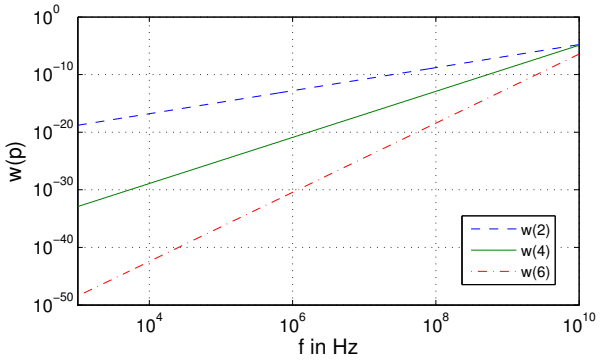


Fig. F.1-2: Weighting functions $w(p)$ of TD-pair separated by their polynomial order

Thus, taking only the second order expression into account leads for equation (F.1.5) to

$$g_m{}^3\left(C_{GS}C_{DS} - C_{GD}{}^2 g_m Z_0\right)\omega^2 \leq 0. \tag{F.1.6}$$

Solving of (F.1.6) in a final step for either C_{GD} or C_{DS} gives the relation between C_{GD} and C_{DS} for which stability under Z_0 is guaranteed.

$$C_{GD} \geq \sqrt{\frac{C_{GS}}{g_m Z_0} C_{DS}} \quad or \quad C_{DS} \leq \frac{C_{GD}{}^2 g_m Z_0}{C_{GS}}. \tag{F.1.7}$$