A Hierarchical Pre-Layout Power Integrity Simulation Flow for Mixed Signal & RF Integrated Circuits

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Kurzfassung

Der anhaltende Trend zu vollständig integrierten Systems-on-Chip (SoC) in denen auch empfindliche analoge und RF Schaltungsblöcke integriert werden, verlangt nach leistungsfähigen und komplexen Systemen zur Spannungsversorgung. Dabei kommen oft mehrere separate Spannungsdomänen, on-chip Spannungsregler und on-chip Entkopplungskapazitäten zum Einsatz. Derartige Versorgungskonzepte erhöhen den Aufwand für die Schaltungsentwicklung und Simulation deutlich, da parasitäre Eigenschaften der Metallleitungen, die normalerweise nicht in Simulationen berücksichtigt werden, einen dominierenden Einfluss auf Signalübersprechen und auf die Restwelligkeit der Versorgungsspannung haben. Eine genaue Berechnung und Modellierung der Versorgungsleitungen ist deshalb notwendig um erfolgreich Power-Integrity-Simulationen durchführen zu können.

Diese Dissertation stellt einen Pre-Layout-Power-Integrity-Simulationsflow vor, der es den Schaltungsentwicklern ermöglicht das elektrische Verhalten von on-chip Versorgungsleitungen zu modellieren und in Schaltungssimulationen zu verwenden. Ein zu Spice kompatibler Flow wurde ausgewählt, da nur die Rechenmethoden analoger Schaltungssimulatoren eine genaue Analyse von Power-Integrity-Phänomenen sowohl im Frequenz- als auch im Zeitbereich ermöglichen, wo auch die nichtlinearen Eigenschaften aktiver Bauelemente berücksichtigt werden. Weiters erlaubt es der Pre-Layout-Ansatz Probleme und Schwachstellen im Versorgungskonzept bereits frühzeitig in der Designphase zu erkennen. Dadurch verringert sich das Risiko, dass Power-Integrity-Probleme erst nach Post-Layout-Extraktionen sichtbar und teure arbeitsintensive Anpassungen an fertigen Chip Layouts notwendig werden. Da keine Layoutdaten in der Designphase zur Verfügung stehen, wird eine textbasierte Konfigurationsdatei verwendet um die Geometrie des Versorgungsnetzwerks zu beschreiben. Softwaretools wurden programmiert um diese Leitungsmodelle automatisiert zu erstellen und in die ursprüngliche Schaltung einzubauen. Der Power-Integrity-Flow unterstützt hierarchische Leitungsmodelle, die auf mehrere Schaltungsblöcke verteilt und auf verschiedenen Hierarchieebenen entsprechend der zu simulierenden Schaltung gespeichert werden. Analoge Simulationen eines kompletten Chips mit extrahierten Leitungsmodellen sind in den meisten Fällen nicht möglich, da die Komplexität der Schaltungen zu groß ist. Die neuen in dieser Dissertation vorgestellten Leitungsmodelle basieren aber auf deutlich weniger komplexen Geometrien als komplette Chip Layouts und ermöglichen daher effiziente analoge Schaltungssimulationen.

Diese Modelle bestehen aus Netzwerken konzentrierter RLCK Elemente, da alle Simulationsmethoden von Spice diese effizient verwenden können, wobei sowohl par-

tielle Eigen- als auch Gegeninduktivitäten inkludiert sind um genaue Simulationen bei hohen Frequenzen zu ermöglichen. Die textbasierten Geometriebeschreibungen erlauben auch benutzerdefinierte Variablen und arithmetische Ausdrücke für alle Geometrieparameter, wodurch praktische Optionen zur Skalierung und Modifikation der Leitergeometrie möglich werden. Um ein erneutes Erstellen der Simulationsnetzlisten nach jeder Modifikation von Geometrieparametern zu vermeiden, werden anstatt fixer numerischer Werte einfache Formeln zu Berechnung der RLCK Elemente in das Modell integriert, die direkt im Analogsimulator berechnet werden. Neue Formeln zur Berechnung der partiellen Selbstinduktivität von Leitern mit rechteckigem Querschnitt werden vorgestellt, deren Genauigkeit mit numerischen Methoden vergleichbar ist, und die auch in einer modifizierten Methode zur Berechnung der Gegeninduktivität verwendet werden. Außerdem werden RF Anwendungen ermöglicht indem eine optimierte Methode zur Diskretisierung des Leiterquerschnitts zum Einsatz kommt, die es erlaubt den Skin Effekt mit nur drei oder fünf Teilsegmenten zu approximieren. Weiters werden die relevanten Algorithmen und Datenstrukturen beschrieben, die notwendig sind um hierarchische Leitungsmodelle mit parametrisierten Geometriebeschreibungen per Software zu erstellen.

Abschließend wird die Stabilitätsanalyse eines fünfstufigen CMOS RF Leistungsverstärkers gezeigt, die eine typische Anwendung des Power-Integrity-Simulationsflows darstellt. Die Versorgungs- und Masseleitungen verursachen Signalrückkopplungen zwischen den Verstärkerstufen, die zu Oszillationen auf den Signalleitungen führen können. Deshalb musste die Verstärkung jeder einzelnen Rückkopplungsschleife berechnet werden um die Anordnung und Geometrie der Versorgungsleitungen optimieren zu können. Aufgrund dieser Analysen konnte eine Leitergeometrie definiert werden, die einen stabilen Betrieb der Schaltung unter allen Betriebsbedingungen ermöglicht.

Abstract

The ongoing trend to fully integrated SOCs including sensitive analog and RF blocks is demanding for increasingly stringent power supply requirements. Hence sophisticated supply concepts are required in contemporary systems including multiple separated voltage domains, on-chip voltage regulators and decoupling capacitors. Such power distribution concepts add significant complexity to the design and electrical analysis process, since wire parasitics, which are normally not considered in circuit simulations, represent the dominant cause of supply ripple and crosstalk issues. Therefore, accurate power grid extraction and modeling is crucial for successful power integrity simulations.

A pre-layout power integrity simulation flow is presented in this thesis that enables circuit designers to incorporate interconnect models handling power grids into Spice compatible analog circuit simulation environments. A Spice compatible flow was selected, since full featured analog circuit simulators are required to accurately analyze power integrity phenomena of analog circuits in frequency or time domain where computing the non-linear behavior of active devices is enabled. Moreover, a pre-layout approach allows to detect and simulate power integrity issues early in the design phase to reduce the risk of expensive and cumbersome redesigns when post layout extractions would reveal critical power grid structures at the final stage of a chip development. Since no layout data is available in this stage, a text based configuration file is utilized to describe the grid geometry and tools were developed that automatically generate the interconnect models and connect them to the original circuit. The power integrity flow supports hierarchical interconnect models, which are divided into several subcircuits and stored on different hierarchy levels according to the original circuit structure. While analog full chip simulations including extracted power grid models are intractable due to model and circuit complexity, the novel power grid models presented in this thesis are derived from significantly less complex grid geometry data and therefore enable efficient analog circuit simulations.

The interconnect models are based on lumped-element partial RLCK networks which are handled efficiently by all Spice simulation methods, while self and mutual inductance elements are included to allow viable RF power integrity simulations. The text based pre-layout geometry definition provides user defined variables and arithmetic expressions for all geometry parameters introducing convenient scaling and customization options to the interconnect models. To avoid regenerating the netlist after parameter alterations, compact resistance, inductance and capacitance equations are incorporated in the power grid model to calculate the lumped element values di-

rectly by the analog simulator, instead of using numerical computations during the model generation. Novel partial self inductance equations for rectangular wires are presented that provide accurate results comparable to numerical approaches, while a modified mutual inductance calculation method exploits these self inductance equations. Additionally, an optimized volume filament approach that needs only three or five filaments is used to approximate the skin effect, enabling the power grid model to handle RF applications. Furthermore, algorithms and data structures are presented, which are required to generate grid models that contain parametrized geometry descriptions and circuit elements distributed over several hierarchy levels.

Finally, the stability analysis of a 5 stage CMOS RF power amplifier is presented representing a typical application of the power integrity simulation flow. Local feedback loops between the amplifier stages which are closed by the power and ground networks may lead to common mode oscillations. Thus, the loop gain had to be analyzed at the supply nodes of each stage and power grid geometry optimizations had to be executed to identify a topology, where a stable operation may be ensured without modifying the signal path and therefore affecting the performance of the amplifier.

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[1] Robust design for efficient use of nanometer technologies

Acknowledgments

Contents

List of Abbreviations and Symbols

Abbreviations

AC	Alternating Current
AMD	Arithmetic Mean Distance
ASIC	Application Specific Integrated Circuit
AWE	Asymptotic Waveform Evaluation
BEM	Boundary Element Method
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
FEM	Finite Element Method
FFT	Fast Fourier Transform
GMD	Geometric Mean Distance
GSM	Global System for Mobile Communications
ITRS	Internation Technology Roadmap for Semiconductors
LDO	Low Dropout Regulator
M/S	Mixed Signal
MOM	Method of Moments
MOS	Metal Oxide Semiconductor
MSG	Maximum Stable Gain
NMOS	N-Channel MOS Transistor
OFDM	Orthogonal Frequency Division Multiplexing
OIP3	Third Order Intermodulation Product
PA	Power Amplifier
PEEC	Partial Elements Equivalent Circuit
PLL	Phase-Locked Loop
PMOS	P-Channel MOS Transistor
PRIMA	Passive Reduced-Order Interconnect Macromodeling Algorithm
PSRR	Power Supply Rejection Ratio
RF	Radio Frequency
RLCK,RC,RLC,RLK	Resistor (R), Inductor (L), Capacitor (C), Coupling Coeff. (K)
ROBIN	Robust Design for Efficient Use of Nanometer Technologies
SoC	System on Chip
SPICE	Simulation Program with Integrated Circuits Emphasis

TEM ..... Transmission Electron Microscopy
TEM ..... Transverse Electromagnetic Mode
TICER ..... Time Constant Equilibration Reduction
TWA ..... Travelling Wave-Guide Amplifier
USB ..... Universal Serial Bus
UWB ..... Ultra Wideband
VPEC ..... Vector Potential Equivalent Circuit
WiMedia ..... Wireless Media Alliance

Symbols

$\mathbf{A}$ ..... Vector Potential
$\mathbf{B}$ ..... Magnetic Field Intensity
$\mathbf{E}$ ..... Electric Field Intensity
$\mathbf{F}_{12}$ ..... Force Between Two Charges or Filaments
$\mathbf{J}$ ..... Current Density
$\mathbf{R}_{12}$ ..... Distance Vector
A_D ..... Arithmetic Mean Distance of One Rectangular Area
$AMD(S_1, S_2)$ ..... Arithmetic Mean Distance of Two Areas
C ..... Capacitance
f_t ..... Cut-Off Frequency of a Transistor
f_{MAX} ..... Maximum Oscillation Frequency of a Transistor
G_D ..... Geometric Mean Distance of One Rectangular Area
$GMD(S_1, S_2)$ ..... Geometric Mean Distance of Two Areas
k_{12} ..... Inductive Coupling Coefficient of Two Conductors
L ..... Self Inductance
L_{ext} ..... External Inductance
L_{int} ..... Internal Inductance
L_{loop} ..... Loop Inductance
M_{12} ..... Mutual Inductance of Two Conductors
Mf_{12} ..... Mutual Inductance of Two Parallel Filaments
R ..... Electrical Resistance
T ..... Loop Gain
T_i ..... Loop Gain Measured During Current Injection
T_v ..... Loop Gain Measured During Voltage Injection
δ ..... Attenuation Distance (Skin Depht)
ϕ_{12} ..... Magnetic Flux
ρ ..... Electrical Resistivity
σ ..... Electrical Conductivity

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1 Power Integrity and Crosstalk of Analog or M/S Integrated Circuits

This chapter presents the motivation of this thesis pointing out that power integrity and crosstalk simulations are crucial tasks during the design of deep sub micron integrated circuits. After a short overview of power integrity approaches for digital designs, the basic concept and key features of a novel hierarchical pre-layout power integrity simulation flow for analog or mixed signal circuits are introduced.

1.1 Introduction

The development of deep sub micron integrated circuits is not only challenged by the functional complexity or the required performance figures of design targets, but also by phenomena like crosstalk noise, voltage drops or electromigration effects on interconnects. Crosstalk noise is invoked mainly by high frequency signals that propagate via parasitic capacitance, resistance or inductance of metal interconnects to sensitive circuit blocks, leading to functional failures or performance degradation. Moreover, the impedance of on-chip interconnects causes static or dynamic voltage drops depending on the current consumption of the circuits that may result in invalid operating conditions. This current consumption may also lead to electromigration effects where high current densities due to small on chip wire cross-sections permanently break metal interconnects or vias. These effects are mainly critical for power distribution networks, because they typically have to conduct higher currents than signal wires and crosstalk may even propagate to distant circuit blocks, since supply networks have to reach the complete chip area. Additionally, the ongoing trend to reduce the size of active elements while increasing the their speed of operation [1], will further increase the importance of these phenomena. Higher switching frequencies lead to higher current consumption that has to be distributed by shrinked supply grids, and inductive voltage drops come into play at frequencies in the GHz range [2, 3]. To mitigate these challenges, complex hierarchical interconnect technologies as illustrated in figure 1.1 were introduced that use dual damascene copper wires offering 9 or more metal layers together with low-k dielectrics [4, 5]. Such interconnect technologies allow a multitude of different power grid geometries, while most contemporary chip designs also exhibit several different power domains, leading to complex power grid design tasks. Especially mixed signal system on chips are critical where sensitive analog blocks are combined with noisy high speed digital circuits. Rough estimations

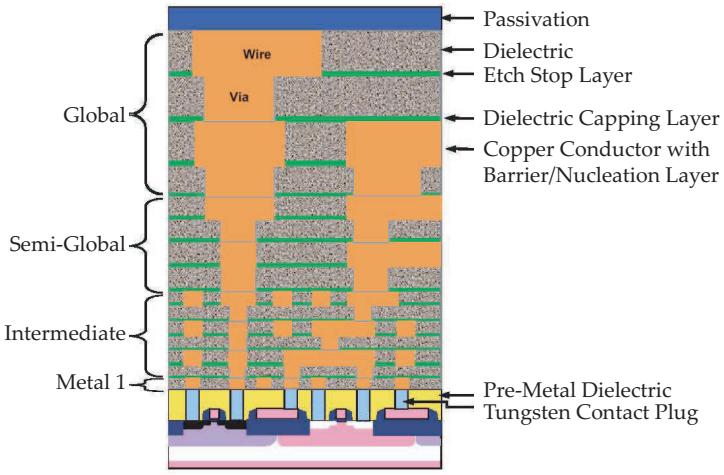

Figure 1.1 Cross-section of Hierarchical Interconnects - ASIC Device, published in ITRS Roadmap 2007: Interconnects [5].

based on hand calculations are insufficient for most designs, therefore simulation tools are required that compute the power grid impedance from layout data and the current consumption of affected circuit blocks to enable voltage drop or crosstalk noise calculations. Moreover, it has to be noted that all power integrity simulation and design methods have to cover also ground networks to provide meaningful analysis results. Since both supply and ground networks are implemented equally utilizing on chip metal interconnects, it is evident that they are handled by the same models and computational methods. Therefore, throughout this thesis, all considerations, methods or figures regarding supply grids inherently include the corresponding ground networks if those are not specifically mentioned.

1.1.1 Power Integrity Simulation Methods

State of the art power integrity simulation methods mainly cover digital designs, because the high current density of fast switching circuits and the relatively large dimensions of complex designs represent the most common sources of power integrity issues. Due to the high complexity of digital designs that may comprise of millions of transistors, full chip power integrity simulations require computational efficient methods. Since on-chip metal interconnects are accurately modeled by linear time invariant systems, a considerable number of efficient approaches were developed. Unfortunately, basic static IR drop simulations are not sufficient any more to estimate functional failures in high performance digital designs where dynamic voltage drops are dominant. Thus, more complex time domain methods as shown in [6] are required to ensure valid simulation results. Moreover, for critical high performance circuits, it may be necessary to incorporate inductance effects on interconnects and the impedance of active circuits in power integrity simulations [7], while dense power

and ground meshes limit the impact of wire inductance to long global nets.

A large group of methods reduces the computational complexity by exploiting domain decomposition, where large power grids are divided into separate sections increasing the sparsity of the problem [8]. Such methods allow parallel computations to simulate very large networks [9] and the original grid hierarchy may be used to additionally reduce the problem size [10]. Moreover, algebraic model order reduction methods [11, 12] or multi grid based methods [13] are also utilized to further improve the efficiency of of power integrity simulations. Since power grids are modeled as linear time invariant systems, frequency domain methods [14] similar to the small signal AC analysis of Spice represent an effective alternative, where a final inverse FFT is utilized to obtain the time domain supply noise. Moreover, pre-layout power integrity analysis methods were introduced that use estimated supply grid models to improve the floor planning process regarding power supply noise [15, 16]. Besides avoiding expensive redesigns after completed place and route tasks, these methods also improve the quality of power grids enabling higher clock frequencies while noise and electromigration issues are reduced.

In contrast to analog circuits where power consumption is easily evaluated in most applications due to constant biasing circuits, digital designs exhibit varying current consumptions and supply noise frequencies that strongly depend on the switching activity. Therefore, power estimation methods have to take the digital signal patterns into account to compute valid worst case switching currents. As described in [17], two alternative approaches to estimate the power consumption namely pattern dependent simulation base methods or probabilistic methods are utilized. Pattern dependent analog simulations are accurate but lead to very long simulation times, which are not feasible for full chip simulations. Hence, to enable valid results while investing reasonalbe computational effort, accuracy bounds for switching activity estimations may be beneficial that allow to calculate a minimum number of required switching patterns [18]. On the other hand, the faster but less accurate probabilistic methods rely on signal and transition probabilities, while computational efficient approaches are used to derive the current consumption. Monte Carlo based approaches like in [19] use a large amount of random signals to approximately find worst case pattern, and these results may be further improved by genetic algorithms [20]. Moreover, probabilistic methods are useful when it is not possible to determine worst case switching pattern easily, especially when pre-layout power integrity simulations have to rely on still uncertain working modes like in [21], where an algorithm based on random walks is employed, that allow efficient computations for highly regular grid structures that are common in digital designs.

1.2 Structure of the Thesis

- *Chapter 1, Power Integrity and Crosstalk of Analog or M/S Integrated Circuits:* After the introduction, this chapter continues with a presentation of the main thesis

topic, illustrating the basic concept and key features of the hierarchical pre-layout power integrity simulation flow for analog or mixed signal circuits.

- *Chapter 2, Calculation of the Power Grid Impedance:* A survey of methods to compute the electromagnetic behavior of on-chip metal interconnect structures is presented, with a focus on approaches that are useful for pre-layout power grid models. Partial element equivalent circuits are explained in detail, since this approach was selected for the pre-layout power grid model.

- *Chapter 3, Analytical Equations for Partial Element Equivalent Circuits:* Instead of numerically computing the partial element values, the power grid models contain arithmetic expressions, which are evaluated later by the circuit simulator. Therefore, novel compact analytical self and mutual inductance equations are introduced in this chapter that provide accurate results for most on-chip geometries.

- *Chapter 4, High Frequency Effects:* Skin and proximity effects cannot be discarded in RF applications. Based on the equations of chapter 3, a semi-empiric method is introduced where a volume filament discretization approach requires only three or five filaments per wire cross section.

- *Chapter 5, Implementation Details of the Power Grid Software:* Implementation details and the structure of hierarchical power grid models are described in this chapter together with a selection of data structures and algorithms, which are utilized to generate these models.

- *Chapter 6, Stability Analysis of a Multi Stage Power Amplifier:* This chapter presents a typical application of pre-layout power grid models, enabling the stability analysis of a 5 stage CMOS RF power amplifier, where local feedback loops on the power grid may lead to an unstable circuit. Power grid geometry optimization runs were executed to identify a grid topology that ensures a fully functional circuit.

- *Appendix:* Finally some basic electromagnetic relations, a power grid configuration example and a detailed manual of the implemented tools are appended to this thesis.

1.3 A Hierarchical Pre-Layout Power Integrity Simulation Flow

1.3.1 A Spice Compatible Simulation Flow

In contrast to traditional power integrity analysis methods for digital designs, analog and mixed signal circuits demand a slightly different methodology. Digital power integrity tools concentrate on the simulation of voltage drops and their influence on

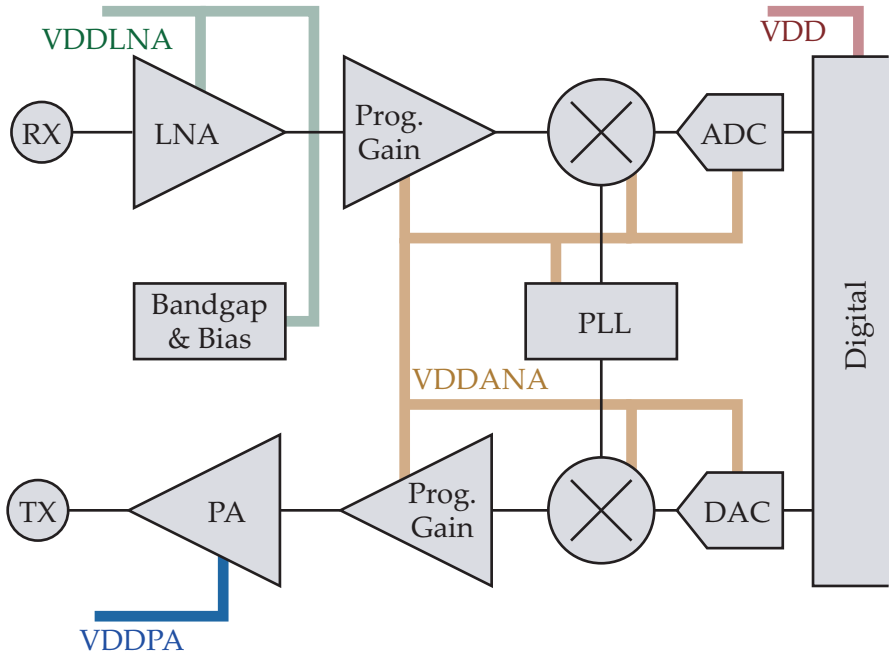

Figure 1.2 Illustration of basic circuit blocks for an RF transceiver including a typical supply concept, where several separate supply domains are utilized.(Ground networks are handled analogous)

signal integrity or propagation delays, and therefore allow highly optimized simulation methods, whereas a reasonable analog circuit analysis is only provided by full featured analog circuit simulators. Moreover, analog circuits may suffer from very specific supply ripple induced effects, for example clock jitter in PLLs, distortion in transceiver circuits or stability issues due to feedback loops as explained in more detail in a subsequent chapter. Therefore, it is obvious that an analog power integrity flow cannot provide a simple straightforward methodology for such diverse analysis tasks. Fortunately analog circuit blocks like the transceiver front end illustrated in figure 1.2 normally contain orders of magnitude less elements than the digital part of an SOC where it is still feasible to perform a detailed manual power integrity analysis. Hence, the main objective of the presented work was to introduce a power integrity tool set and Spice compatible interconnect models that alleviate such simulation tasks where Spice netlists may be still regarded as a standard format that is supported by the majority of analog circuit simulators. Furthermore, the tool set integrates well into the standard analog simulation flow allowing circuit designers to perform power integrity analyzes within their well known design environment.

1.3.2 Considerations About Model Complexity

While analog circuit simulators already provide accurate time and frequency domain simulations for both linear and nonlinear circuits, it is not possible to conveniently

simulate the electrical behavior of complex metal interconnects. Post layout parasitic extraction tools provide accurate models of the interconnects, including the power grid, but the resulting models are as complex as the corresponding layout geometries that were used in the extraction process. Especially grid models for RF applications that should include inductive effects are limited to only very basic circuit structures and analysis methods. Thus, it was one major goal of the presented work to limit the complexity of power grid models even when mutual inductance elements are utilized. Instead of using complex layout data to generate the grid models, a pre-layout approach was selected where the geometry is described in a text based configuration file. Since user interaction is required to obtain a grid geometry, the complexity of these pre-layout structures is limited by practical reasons. Moreover, subcircuits are the smallest units that are considered within the grid model and the related software tools, similar to the dominant full custom integrated circuit CAD flow[1] that provides a hierarchical symbolic approach for supply nodes named inherited connections. Instead of normal interconnects that have to be drawn as wires in the schematic, supply interconnects are defined by special node names within a subcircuit and methods are provided to inherit or to individually assign supply connections between different subcircuits. Therefore, this approach enables a considerable more convenient handling of supply networks. Obviously, the pre-layout power grid models have to reflect this behavior to integrate seamlessly into the original design flow without modifying the circuit structure, while this level of abstraction is also reasonable for the majority of power integrity topics. Moreover, this approach allows hierarchical grid models as described in more detail in chapter 6 that retain the original circuit structure. Instead of one single grid model that connects the supply nodes of a circuit where all hierarchy levels are removed, the pre-layout power integrity tools generate a set of small interconnect models which are distributed over all affected circuit hierarchies.

1.3.3 Advantages of a Pre-Layout Simulation Flow

A pre-layout simulation flow enables circuit designers to perform power integrity analyzes and evaluations without having to rely on chip layouts, that are normally only available at the final stages of a design project. This flow may be very useful in concept engineering tasks, where sensitive circuit blocks require a thoroughly designed supply concept. Instead of relying on rough hand calculations, estimations, or experiences from earlier designs, a pre-layout flow enables engineers to accurately evaluate different supply concepts. Moreover, the resulting grid models could be used throughout the complete circuit design phase, because the relatively compact grid models do not significantly extend the simulation times. Hence, power integrity or cross talk issues may be identified and solved early during the design of the affected circuit blocks. When post-layout parasitic extractions reveal design or layout issues, circuit redesigns become necessary which result in cumbersome and expensive circuit and layout modi-

[1] Cadence Virtuoso

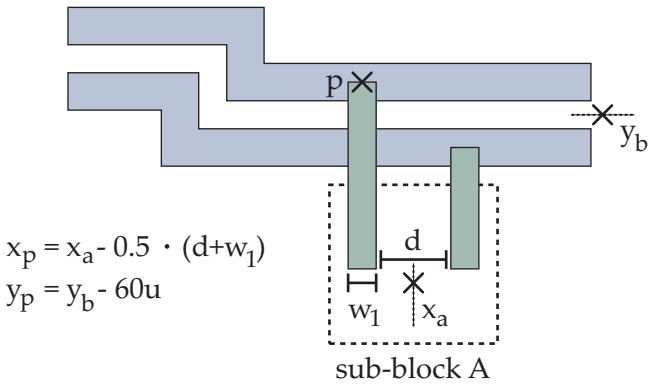

Figure 1.3 An example of a parametrized grid geometry: Arithmetic expressions are used to define the coordinates of a wire endpoint P that relies on the user defined variables x_a, y_b, w_1 and d.

fications. The presented pre-layout models help to avoid such tasks considering power integrity topics, where redesigns normally involve more than one circuit block and additionally induce side effects that have to be analyzed. Therefore, the initially invested effort for creating and analyzing pre-layout models might easily pay off under such circumstances. Nevertheless it has to be noted that pre-layout simulations do not substitute a final post layout analysis that incorporates parasitic effects of the complete circuit structure including signal and power interconnects, but one major objective of a pre-layout simulation flow is avoiding unexpected results from these final simulation runs.

1.3.4 Features of a Text Based Geometry Description

Initially pre-layout models cause some additional effort for circuit designers, who have to enter the grid geometries in a configuration file manually, since no layout is available to automatically extract the required data. On the other hand this text based configuration file provides certain advantages compared to extracted layout data besides the already mentioned lower complexity. Contrary to layout data the geometry of pre-layout models does not use simple numerical values but arithmetic expressions and variables to describe the coordinates or dimensions of wire segments. Figure 1.3 illustrates the use of arithmetic expressions and user defined variables for a simple geometry. The coordinate P representing the endpoint of a wire segment is defined by arithmetic expressions that depend on user defined variables like x_a or d, hence changing the values of variables will inherently update the coordinates of P. Therefore, it possible to conveniently modify the geometry of grid models during the design process. Moreover these arithmetic expressions are not only valid within the configuration file, but are also available in the resulting Spice model. Hence, the element values of the RLCK networks are also automatically updated when geometry parameters are changed within the simulation environment. This allows parameter

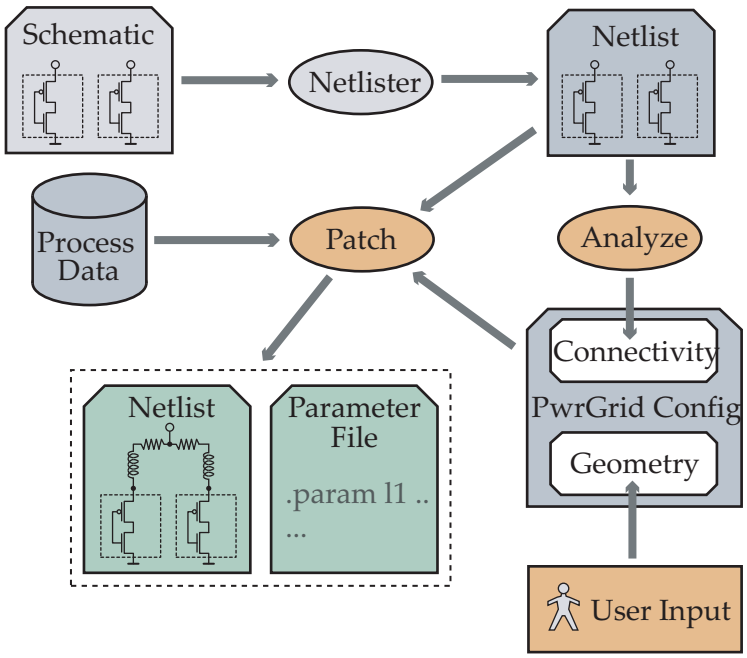

Figure 1.4 A netlist based flow to generate pre-layout power grid models. "Patch" and "Analyze" represent the tools that are provided by the power grid flow.

sweeps on the power grid geometry without having to re-netlist the input file of the simulator enabling sensitivity analyzes or optimization runs that are not possible with extracted grid layouts. Furthermore, this approach exhibits the advantage that it is possible to reuse power grid models for multiple different circuits that additionally reduces the required editing effort for the grid configuration file. Arbitrary orthogonal geometries are supported by the power integrity flow, while additionally provided basic bus topologies and simple star connections that only consider wire lengths and no wire positions allow very fast grid impedance estimations in applications where accuracy requirements are not critical. A detailed description of the grid configuration syntax and all software and model features is included in the appendix B of this thesis.

1.3.5 Software Tools to Automate the Model Generation

To minimize the additional workload that is required for handling pre-layout power grid models, it was necessary to introduce software tools that automatically create and connect grid models to the original circuits. It was necessary to find an approach that integrates well into the design environment but does not require modifications in the original schematics of the chip design environment. Nevertheless, power grid models have to replace an ideal supply node by several local supply nodes and RLCK elements are used to connect these nodes depending on the computed interconnect impedance. A netlist based approach as illustrated in figure 1.4 allows to define the ideal supply connections by the schematic entry of the design environment, whereas power grid

models are added only to separate netlists for circuit simulations. Therefore, the standard full custom design flow and its data structures are not affected by the power integrity flow, and tools like electrical rule and layout versus schematic checks do not need any modifications.

Two power grid tools named ”Analyze” and ”Patch” are provided by the flow, where ”Analyze” is used for the initial setup of the grid configuration and ”Patch” creates and inserts the model to the resulting netlist. ”Analyze” extracts the circuit hierarchy and the supply connectivity from the original netlist that correspond to the circuit schematic, and generates a power grid configuration file with valid connectivity data and templates for the user defined geometry definitions. These templates significantly reduce the necessary manual editing effort and ensure a valid connectivity of the grid models.

After manually editing the geometry configuration of the power grid, ”Patch” creates the lumped element RLCK networks, connects them to the corresponding subcircuits of the original netlist, and finally generates the required patched netlist. One netlist file consists of the original circuit and RLCK elements of the grid model, while all grid model related arithmetic expressions and user defined variables are stored in a separate file to optionally allow netlist updates without affecting previously edited parameter definitions. Moreover, the physical behavior of metal layers provided by process data files are also appended to this parameter file.

Even though the RLCK values are not computed during the model generation, but during a simulation run to enable parameter alterations without netlist updates, initial or default numerical values have to be defined in the configuration file. These values are used to check the validity of grid definitions and allow a graphical output to visualize the power grid geometries. While a a textual description of the grid configuration is preferable over graphical tools for editing parametrized geometry definitions, the graphical output proved as a valuable feature for debugging and documenting the pre-layout power grid models.

Concluding, the presented simulation flow enables circuit designers to conveniently analyze and optimize the supply grids of analog circuits where parametrized interconnect models are provided that include inductive effects without significantly sacrificing the computational complexity of circuit simulations. The hierarchical grid models do not require modifications of the original circuit structure, while a netlist based tool set is used to ensure a seamless integration in the full custom chip design flow.

2 Calculation of the Power Grid Impedance

This chapter presents an overview of the currently most popular interconnect technology and discusses methods to compute the electromagnetic behavior of such structures, focusing on those approaches that are useful for pre-layout power grid models. Partial element equivalent circuits and similar methods are therefore presented in detail since this approach was selected for the pre-layout power grid model. Moreover, model order reduction methods and the strongly linked stability issues of reduced partial element networks are presented as analogous effects turned out to be the main motivation to develop accurate analytic inductance equations.

2.1 Damascene Copper Interconnects

Damascene copper electroplating is currently the dominant technology to create on-chip metal interconnects, therefore a short description of this method based on [22] is presented. A dual damascene process is illustrated in figure 2.1, which has the advantage that via connections and wires are plated during one single process step. As shown in image 2.1 insulator layers, normally SiO_2, are added on the silicon substrate and patterned according to the interconnect geometry. Since copper plating is an electrolytic process, a seed layer is required that covers the complete chip area. This seed layer is used as conducting layer where copper deposits occur during the plating process. Tantalum or TiN are typically used for such layers and after the plating, the unavoidable excess material is removed during the planarization step, using for example a chemical-mechanical polishing method. Optionally, an additional barrier layer may be inserted between the insulator and the seed layer to avoid interaction between the metal and insulator. Moreover, void free and seamless deposits are possible by a "superconformal" plating process [22], where the bottom of a wire trench exhibits a faster deposition rate than the sidewalls due to a properly selected plating solution.

The resistance of copper interconnects is approximately 40% lower compared to previously used aluminium wires, leading to significantly shorter signal delays and to reduced voltage drops, which is considered more important for power grids. Moreover, copper interconnects exhibit also an improved electromigration robustness, hence modern deep submicron CMOS technologies use almost exclusively this technology. The DC resistance of rectangular wires of length l, width w and thickness t may be computed by the following well known equation

$$R = \rho_{eff} \frac{l}{wt}, \tag{2.1}$$

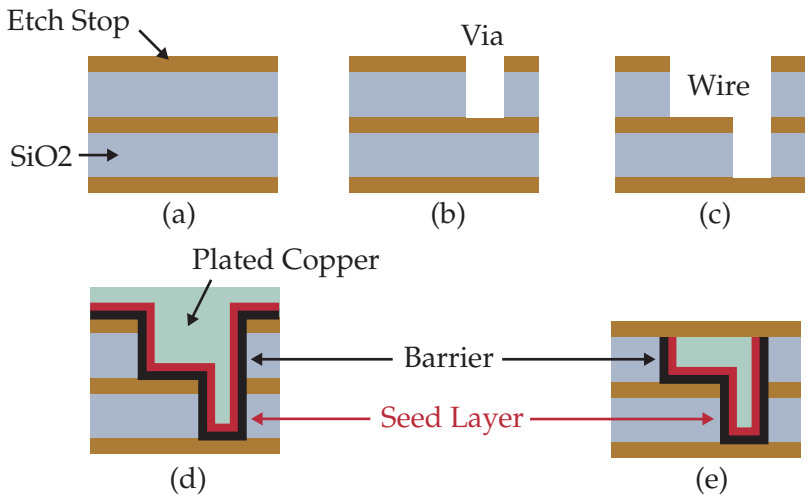

Figure 2.1 Process steps of dual damascene interconnect fabrication; (a) Insulator deposition; (b) Via definition/etching; (c) Wire definition/etching; (d) Barrier and seed layer deposition + copper electroplating; (e) Planarization via chemical-mechanical polishing; Figures were extracted from [22].

which is also used within the power grid model. To account for the material properties, equation 2.1 utilizes the effective resistivity ρ_{eff} that is significantly higher than the resistivity ρ for bulk metals like copper (ρ_{cu} = 17.6 nΩm) or aluminium (ρ_{al} = 28.2 nΩm) for on-chip interconnects. The trapezoidal cross section of wires as shown in figure 2.2a leads to reduced wire conductance values, especially for narrow wires where inclined sidewalls have a large influence on the wire cross section. Moreover, typical seed layer materials have significantly larger resistivity than the plated metal, therefore together with scattering effects thin metal layers close to the silicon surface with smaller layer thicknesses exhibit a higher effective resistance than thicker metal layers on top of the chip backend. Hence, when equation 2.1 is used for on-chip resistance computations it is advisable to use different values of ρ_{eff} for each metal layer.

Future technologies with additionally shrinked feature dimensions will most likely use also dual damascene interconnects similar to the structures shown in 2.2a, but wire widths below $\approx$ 300 nm show a significant rise of resistance compared to larger structures. As described in [23, 24] effects like diffuse scattering of electrons at the wire surface and at grain boundaries cause this effect and figure 2.2b shows measured and computed resistance values for such wires. Even though models are available that cover these effects [23], a constant wire resistance could be safely assumed for power grid models in this thesis since wire widths below 300 nm are currently not commonly used there. Nevertheless, future interconnect resistance models will have to account for these effects.

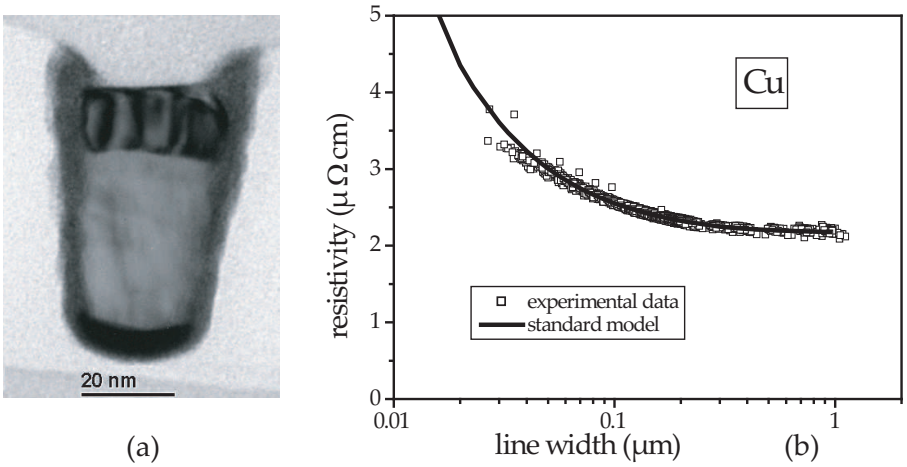

Figure 2.2 Nanometer interconnects for deep submicron processes; (a) Cross sectional TEM micrograph; (b) Electrical resistivity of ≈1700 Cu lines with a conductor height of 150 nm; Both pictures were published by G. Schindler et. al. in [24].

2.2 Computing the Electromagnetic Behavior of Interconnects

2.2.1 Numerical Methods

Several numerical methods are available to accurately compute the electromagnetic behavior of on-chip interconnects by solving Maxwell's equations [25]. These methods are based on a discretization of the volume occupied by the interconnect section under investigation. Finite difference methods approximate the derivatives of the electromagnetic equations by simple difference quotients for each volume or area element leading to a system of linear equations that can be solved numerically. On the other hand, finite element methods (FEM) approximate the solution of the electromagnetic equations by finite basis functions resulting again in a system of linear equations. Moreover, the method of moments (MOM) or boundary element method (BEM) solves the integral form of the electromagnetic equations exploiting Green's functions. This approach has computational advantages to the finite difference and finite element methods for planar structures with linear and homogenous media. All these methods are able to cover electromagnetic, thermal or even the mechanical behavior of on-chip interconnects without restricting the supported wire geometries. Unfortunately the computational effort only allows the simulation of small structures in reasonable time, therefore the simulation of complete chip layouts or even larger circuit blocks is not feasible. A survey of numerical simulation techniques for on-chip interconnect structures is published in [26, 27].

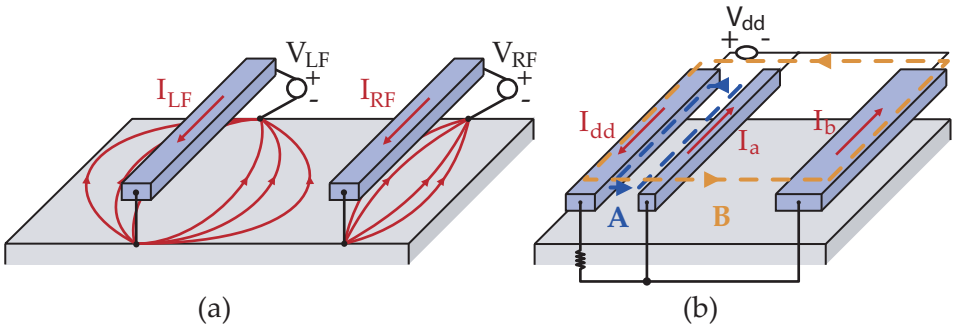

Figure 2.3 Frequency dependent return current paths; (a) comparison of high and low signal frequencies for wires above conductor plane; (b) two possible return current paths.

2.2.2 Return Limited Inductance Approach

Full chip resistance and capacitance extraction tools that are commonly used in the design process are mainly based on R and C templates, which are scaled according to the layout. Inductance extractions were mainly limited to particular RF structures due to the computational complexity of the extraction method and the size of resulting interconnect models, whereas a return limited inductance approach [28] enables full chip inductance extractions for arbitrary routed signal lines [1]. Instead of evaluating all possible inductive couplings, this method defines current loops between a signal wire and its nearest supply line and to compute the corresponding self inductance. This approach provides a decent inductance estimation at least for higher frequency signals, since most chip layouts and especially digital designs have a rather dense supply grid. Furthermore, the power supply lines act as a magnetic shielding because the mutual inductance is considered only for parallel wires if no supply line is placed inbetween. Hence, the resulting extracted netlist size remains reasonable small, but for obvious reasons this approach is not suitable for power grid analysis.

2.2.3 Microstrip Transmission Lines

At high signal frequencies in RF or very fast digital circuits it is advisable to model on-chip interconnects as transmission lines, if well defined return current paths are available. Among a multitude of publications treating transmission line calculations the following selection of papers present calculation approaches for on-chip applications. On-chip planar microstrip transmission lines were introduced in [29] including lumped element models and formulas to compute the element values. As published in a basic paper about microstrips on a silicon substrate [30], three different fundamental conduction modes were defined that are derived from parallel plate waveguide

[1] This method is implemented in Cadence Assura-PL, a layout extraction tools widely used in industrial chip design environments.

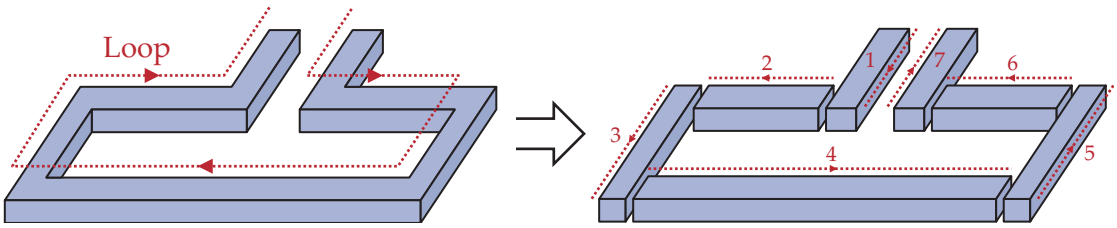

Figure 2.4 Basic concept of partial inductance: Division of conductor loops in straight wire segments.

equations. High frequencies and high resistance dielectrics lead to a "dielectric quasi-TEM" propagation mode, whereas a higher conducting silicon substrate affects the propagation leading to a mode named "skin effect mode", because its behavior is dominated by the skin effect occurring in the substrate. Besides these two conduction modes a slow wave propagation occurs when the signal frequency and the dielectric resistance are not high enough to consider the dielectric TEM propagation. Based on these fundamental propagation modes, analytical formulas for transmission line models in on-chip applications were published in [31] that also consider the narrow line widths common in on-chip microstrip structures. Furthermore, when the conducting silicon substrate is not considered in the transmission line model it is possible to define approximated closed form formulas for the frequency dependent resistance and inductance of microstrip lines [32] that are far more compact than the equations of [31]. Concluding this topic, transmission lines are very useful to design critical on-chip high frequency signal paths, while accurate broad band models for these structures are available.

2.3 Partial Element Equivalent Circuits

According to appendix A, both self and mutual inductance are only defined for closed current loops, thus it is mandatory to identify the correct conductor loops for inductance computations [33]. Inductance values of interconnects, which have well defined return current paths as for example transmission lines, coaxial cables or twisted pair wires may be computed by loop inductance methods, but this is not possible for arbitrary routed geometries like on-chip interconnects. Figure 2.3a illustrates the challenge using a very simple case of rectangular straight wires above a metal ground plain. At low frequencies the current flow in the ground plane spreads over a wider area to minimize the ohmic resistance of the ground path, whereas most of the current is concentrated just below the wire at higher frequencies to minimize the loop inductance. Hence it is not possible to identify these loops without knowing the frequencies and directions of wire currents. This issue is not only critical for metal planes but also for geometries like figure 2.3b with more than one possible current path. In such cases the return current may flow over multiple paths while the current distribution

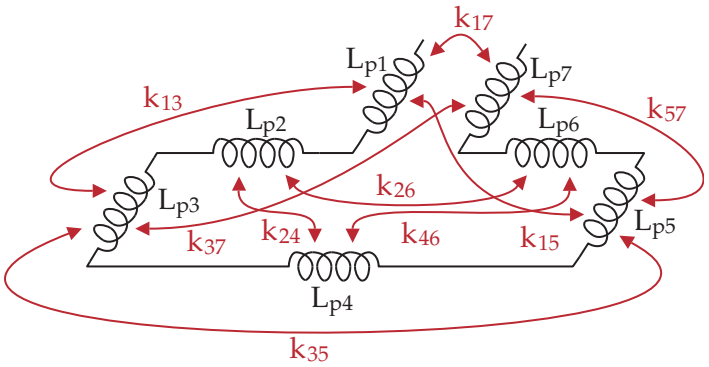

Figure 2.5 Lumped elements circuit based on partial inductance, where k elements are used to represent the partial mutual inductance elements.

changes over signal frequencies. Even though the two different return paths of figure 2.3b may be covered by approximations, this is not feasible for realistic and normally far more complex geometries. Additionally, parasitic extraction is more convenient if computations only require wire geometries and material properties without relying on electrical signals and stimuli. Hence the following alternative approach is popular for on-chip inductance computations.

Ruehli introduced the concept of partial inductance for on-chip parasitic extraction applications in [34], where current loops are opened as shown in figure 2.4 and straight wire segments are utilized instead for inductance computations. Hence, the inductance values of the segments are computed by splitting the integral of the current loop in several segments. Considering figure 2.4 and the equation A.31 it is possible to rewrite the loop inductance as

$$L_{loop} = \frac{\mu_0}{4\pi} \oint_C \oint_C \frac{d\mathbf{r}_1}{R} \cdot d\mathbf{r}_1 = \frac{\mu_0}{4\pi} \sum_{a=1}^{7} \sum_{b=1}^{7} \int_{C_a} \int_{C_b} \frac{d\mathbf{r}_a}{R} \cdot d\mathbf{r}_b = \sum_{a=1}^{7} \sum_{b=1}^{7} Mp_{ab}. \tag{2.2}$$

The inductance of the straight segments is called partial inductance to differentiate it from the loop inductance, and figure 2.5 illustrates the resulting lumped elements network, where Lp_a represent the partial self inductance values and k_{ab} are coupling factors [2] derived from partial mutual inductance values Mp_{ab}. Even though the inductance of a single open segment has no valid physical meaning, figure 2.6 illustrates the physical interpretation of a partial inductance system. A second independent conductor was added to this figure to show that the partial inductance approach is not limited to single loop geometries and the resulting current loops and magnetic fields of three parallel segments are drawn in more detail. Partial inductance elements are based on current loops that are closed at infinity, thus all elements are inductively linked to each other. Furthermore, figure 2.6 also shows how magnetic fields of partial inductance elements are combined leading to a physically correct system. In case

[2] $k_{ab} = \frac{Mp_{ab}}{\sqrt{Mp_{aa} \cdot Mp_{bb}}}$

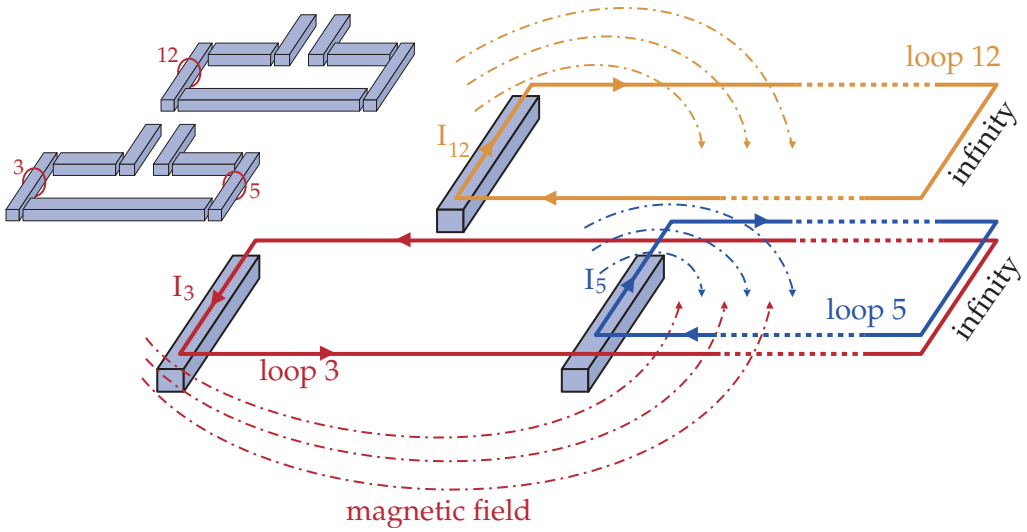

Figure 2.6 Illustration of return currents at infinity for three wire segments including their magnetic fields.

of the wire segments 3 and 5, the magnetic fields are canceled outside the current loop as expected since segment 5 acts as return current path. Moreover, the current loop of segment 12 is linked to all other loops indicating that inductively coupled independent wire geometries are correctly modeled by partial inductance elements. Similar discretizations may be applied to wire surfaces resulting in partial capacitance elements as described in [35], and partial elements equivalent circuits (PEEC) [36, 37] combine partial inductance, capacitance and DC resistance elements to completely model the electromagnetic behavior of on-chip interconnects. PEEC models are especially useful for circuit simulations since no additional computing steps are required to generate Spice compatible models. Moreover, computational advantages by two orders of magnitude compared to MOM methods of a 2.5D field solver were published in [38], but from a general point of view the computational complexity of PEEC approaches is strongly depending on the discretization level and the numerical methods used to solve linear systems.

2.3.1 Advanced PEEC Methods

Based on the initial approach of Ruehli [34] several improvements were developed considering the modeling accuracy or the computational complexity. Thus a short overview of these methods is presented in this chapter. PEEC models may be utilized to compute arbitrary 3D structures [39] by employing proper discretization strategies, and triangular discretizations [40] may improve the model accuracy of such arbitrary shaped wires. Non orthogonal wires are efficiently computed in [41], while PEEC models that incorporate retardation as described in [42] are required for wire geometries with dimensions in the range of signal wavelengths. Moreover, substrate eddy

currents may be included in partial elements [43], thus enabling PEEC models to cover critical RF applications.

From a computational point of view the biggest drawback of the PEEC approach is the large number of mutual inductance elements that rises quadratically with the resulting number of wire segments after the discretization step. One approach for reducing the number of mutual elements utilizes a partial inductance method which places the return current not at infinity [44]. Therefore, mutual inductance elements are discarded where finite current loops do not intersect.

In addition to reducing the number of circuit elements, modern numerical methods for solving linear equations may significantly improve the computational efficiency [45, 41]. Furthermore, PEEC models are useful for arbitrary routed rather dense interconnect structures, while transmission lines effectively model longer interconnect structures with well defined return current paths, hence hybrid PEEC / transmission line models [46] allow efficient computations of such geometries (e.g. chip interconnects plus some board wires).

2.3.2 Model Order Reduction and Passivity Considerations

Since PEEC models are linear time invariant systems, algebraic model order reduction methods offer effective approaches to significantly reduce the computational complexity. Unfortunately simply removing the smallest mutual inductance terms is not feasible, because the passivity of the resulting reduced model cannot be ensured. This effect can be explained mathematically by the eigen-energy of a partial inductance matrix. Assuming that the partial self and mutual inductance of an interconnect network are stored in in an orthogonal matrix

$$\mathcal{L} = \begin{pmatrix} L_{11} & M_{12} & \cdots & M_{1n} \\ M_{21} & L_{22} & \cdots & M_{2n} \\ \cdots & \cdots & \cdots & \cdots \\ M_{n1} & M_{n2} & \cdots & L_{nn} \end{pmatrix} \tag{2.3}$$

and the corresponding element currents in the vector $\mathbf{i}$ allow to compute the energy stored in the magnetic field of the network [44, 47]

$$E = \mathbf{i}^T \cdot \mathcal{L} \cdot \mathbf{i} \geq 0. \tag{2.4}$$

The current vector $\mathbf{i}$ can be represented as a linear combination of the normalized eigenvectors $\hat{\mathbf{v}}_j$ of $\mathcal{L}$

$$\mathbf{i} = \sum_{j=1}^{n} a_j \cdot \hat{\mathbf{v}}_j, \tag{2.5}$$

and the energy may be reformulated as sum of eigen-energy terms

$$E = \sum_{j=1}^{n} a_j^2 \cdot \lambda_j, \tag{2.6}$$

where each eigenvalue λ_j and the corresponding current vector and eigen energy represents a particular current assembly, and all eigenvalues are positive, because the energy stored in the system cannot be negative. As illustrated in figure 2.3 the smallest possible return current paths are used at high frequencies to set the magnetic energy and therefore the inductance at the lowest possible value. This state corresponds to the current vector of the smallest eigen energy, hence the high frequency response of the system is determined by the smallest eigenvalues of the partial inductance matrix. On the other hand at low frequencies larger energy values may be stored in the magnetic field, hence the large eigenvalues are linked to the low frequency behavior of the interconnect network. Thus the largest eigenvalues of the partial inductance matrix correspond to to lowest frequency poles.

The eigenvalues of full partial inductance matrices are always positive, but this is not true for reduced systems where, for example, the smallest mutual inductance values are removed. Negative eigenvalues lead to positive poles, therefore the models of stable passive circuits may exhibit physically impossible oscillations after the truncation of mutual inductance terms. Since reduced partial inductance matrices do not necessarily lead to unstable models, several arithmetic methods were published that maintain the passivity of reduced models. Asymptotic waveform evaluation (AWE) [48] algorithms approximate the transfer functions of a linear network in the s-domain by using only the dominant poles in the reduced network. Directly evaluating the the transfer function is computational too complex for large linear networks, therefore different numerical approximations were proposed for this task like Padé [48] or Padé via Lanczos [49] approaches. Numerically more robust approaches are Arnoldi based approximations [50], and variants of these methods were published that maintain the passivity of the reduced network like PRIMA [51] or more recent approaches published in [52, 53]. These model order reduction methods derive reduced impedance matrices that cannot be used directly in circuit simulators. Besides directly representing all matrix elements by the corresponding circuit elements, time varying macromodels are possible alternatives and [54] presents a comparison different synthetization methods considering the resulting model size and the computational complexity. Unfortunately these model order reduction algorithms require high calculation efforts so alternative approaches like TICER [55] or $Y-\Delta$ transformations [56] that modify nodes only locally are useful for very large networks. The run-time of such methods scales with O(n) and no additional steps are necessary to create lumped elements RLCK models.

2.3.3 Inverse Inductance Based Circuits

Recently a novel circuit element the inverse inductance was introduced [57], which significantly reduces the computational issues of large partial inductance networks. The matrix $\mathcal{K}$ is defined as the inverse of the inductance matrix $\mathcal{L}$

$$\mathcal{K} = \mathcal{L}^{-1}, \tag{2.7}$$

which is inspired from the relationship of the inductance and the capacitance of transmission lines

$$L_{loop} = \mu_0 \epsilon_0 C^{-1}. \tag{2.8}$$

It has to be noted that the inverse inductance matrix $\mathcal{K}$ and the capacitance matrix $\mathcal{C}$ have no physical relation, because the transmission line impedance is computed using the loop inductance, whereas $\mathcal{K}$ is related to a partial inductance matrix. Nevertheless $\mathcal{K}$, also named susceptance matrix, exhibits a similar locality like $\mathcal{C}$, enabling efficient model reduction and circuit simulation methods. Moreover $\mathcal{K}$ is diagonal dominant and positive definite [58], therefore it is possible to truncate very small elements without affecting the stability of the resulting network. These advantages are exploited by parasitic extraction methods as published in [58] or in [59], where a windowing method is used for extracting small partial inductance submatrices that are inverted to obtain the inverse inductance matrix. After truncation these submatrices are inverted again and merged to a stable sparse partial inductance matrix. Sophisticated circuit aware clustering and reduction strategies of [60] or [61] provide alternative methods for efficient inductance extractions.

2.3.4 Vector Potential Equivalent Circuits

Another attractive alternative to traditional PEEC approaches utilizes the vector potential to model the inductive behavior for interconnect networks that was introduced in [62] and extended to N-body problems in [63]. In contrast to PEEC models, vector potential equivalent circuits (VPEC) describe the propagation of the vector potential from one volume segment to its neighbors, similar to the electric potential. Therefore, only couplings between neighboring segments have to be modeled compared to PEEC where all possible segment pairs are computed, leading to a relatively sparse and passive linear system. The vector potential may realized with controlled current sources and resistors, therefore Spice compatible models can be easily created. The VPEC approach was recently improved to incorporate the skin effect [64] enabling efficient broad band interconnect models, and VPEC networks turned out as a good basis for additional model order reduction methods [65] to further reduce the complexity of resulting networks.

2.3.5 Transmission Matrix

The transmission matrix approach [66] is a partial elements variant that is useful for power plane simulations mainly on board level. Rectangular unity cells as illustrated in figure 2.7 are precalculated, which contain power ground capacitance, resistance and inductance values of the metal layers and dielectric losses. Furthermore, these unity cells are arranged on a regular rectangular array to approximate the arbitrary layout of a power plane. A matrix is populated by the lumped elements of these unity cells leading to a rather sparse linear system that may be solved efficiently by common

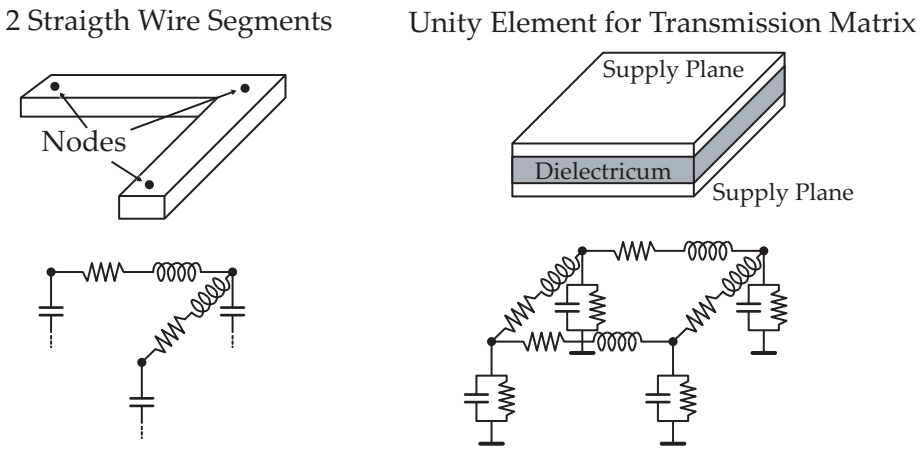

Figure 2.7 Illustration of a transmission matrix unity cell compared to a standard PEEC network for two wire segments.

linear solvers or even by a Spice compatible simulator. The transmission matrix was extended for multiple layer systems in [67] leading to viable method to obtain broadband models for arbitrary routed power planes. Since unity cells are only connected to their direct neighbors the transmission matrix is more sparse than standard PEEC matrices allowing fast and accurate models for this particular application.

2.4 The Modeling Method for Pre-Layout Power Grids

Numerical methods like MOM or FEM are not useful for pre-layout power grid models, since parametrized arithmetic grid models cannot be realized by numerical methods and the computational complexity limits the grid size that may be simulated investing reasonable amounts of time and processing power. Transmission lines are very useful for geometries with well defined return current paths, but this is not the case for mostly arbitrary routed power grids in analog circuit blocks. Thus, a partial element approach turned out as the most feasible method for on-chip power grid models, because planar orthogonal routed wire networks may be conveniently modeled by Spice compatible lumped elements. The model complexity may be an issue for very large power grids when inductive effects are required, and model order reduction methods cannot be employed without affecting the parametrization feature of the pre-layout model. Geometry alteration would require recomputing the reduction algorithm, which is not possible with the arithmetic methods provided by standard analog circuit simulators. Nevertheless, typical pre-layout geometries are significantly less complex than extracted detailed layouts, hence the resulting model complexity is no limiting factor in real applications. Full PEEC models on the other hand allow severe geometry modifications without having to re-netlist the model since all segments are magnetically linked and only the coupling factors change. Regarding the sparse

variants of partial element models, VPEC models allow geometry modifications only as long as wire segments do not change their neighbors, hence the model parametrization is more limited compared to traditional PEEC networks and transmission matrix approaches are useful only for supply planes, which are typically not utilized for on-chip power networks. On the other hand susceptance based approaches will provide interconnect models with similar features like parametrized PEEC networks, but to fully benefit from these methods inverse inductance elements have to be supported by analog circuit simulators, which is currently not the case for most Spice compatible tools. Therefore, susceptance based models may provide a viable option in the future to improve the computational efficiency of the pre-layout power grid models presented in this thesis. The stability considerations presented in the context of model order reduction methods are also important for the pre-layout model, where approximated formulas are used for partial inductance calculations. It is possible that calculation errors lead to negative eigenvalues in the partial inductance matrix, thus positive poles in the transfer functions may render the resulting interconnect model unstable. To avoid such problems accurate inductance formulas are required that cover all possible wire geometries, even though pre-layout models would not require this accuracy from an application point of view.

2.4.1 Conclusion

Concluding, fully coupled PEEC networks were selected for the pre-layout interconnect models, where each straight wire segment is represented by one single partial element. No additional segmentation along the current flow direction was required, since on-chip wire dimensions allow quasi static models for the whole frequency range of interest. Moreover, the required methods and arithmetic expressions to compute the particular partial element values are described in detail in the following two chapters.

3 Analytical Equations for Partial Element Equivalent Circuits

Compact analytical equations to calculate the wire parasitics are mandatory for parameterized pre-layout power grid models. Since the partial element approach described in the previous chapter is utilized, resistance and inductance equations for straight rectangular wire segments are required. While resistance calculations are performed using the well known equation 2.1 and capacitive effects are covered by appropriate blocking capacitor models, this chapter is mainly focusing on the development of novel analytical self and mutual inductance formulas. The main results of this chapter regarding inductance equations were published in [68].

3.1 Capacitance Equations

3.1.1 Parasitic Wire Capacitance Equations

The power grid model is tailored for analog RF circuits where decoupling capacitors are mandatory in most circuit blocks. Therefore, the parasitic wire capacitance could be discarded in the power grid model since blocking capacitor arrays dominate the capacitive behavior of such power grids. Nevertheless an overview of wire capacitance formulas and computational methods is presented in this chapter to provide a complete set of analytical equations for lumped elements RLCK models. The capacitance of the sidewalls plays a dominant role in modern CMOS technologies where the metal layer thickness is relatively large compared to wire widths. Hence the simple parallel plate capacitor equation A.11 is not accurate except for very wide supply wires. The paper [69] compares several equations calculating the capacitance of one wire to a reference plane (ground) and shows that parallel plate models seriously underestimate the capacitance of typical on-chip wire geometries. Figure 3.1 illustrates such a wire to ground capacitance including the parameter names utilized in the following equations. The most accurate analytical capacitance formula that might be useful for pre-layout grid models was published in [70] where two consecutive conformal

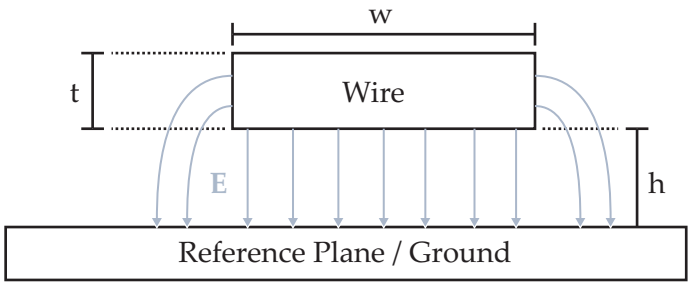

Figure 3.1 Wire to ground capacitance, the wire length is l.

mappings transfer the rectangular geometry into a parallel plate structure leading to

$$
\begin{aligned}
C &= l\frac{2\epsilon}{\pi}\ln\frac{2R_b}{R_a} \qquad (3.1)\\
\ln R_a &= -1-\frac{\pi w}{2h}-\frac{p+1}{p^{0.5}}\tanh^{-1}p^{-0.5}-\ln\frac{p-1}{4p}\\
R_b &= \eta+\frac{p+1}{2p^{0.5}}\ln\Delta\\
\Delta &= \begin{cases}\eta & \text{if} \quad p\le\eta\\ p & \text{if} \quad p>\eta\end{cases}\\
\eta &= p^{0.5}\left[\frac{\pi w}{2h}+\frac{p+1}{2p^{0.5}}\left(1+\ln\frac{4}{p-1}\right)-2\tanh^{-1}p^{-0.5}\right]\\
p &= 2\left(1+\frac{t}{h}\right)^2-1+\sqrt{\left[2\left(1+\frac{t}{h}\right)^2-1\right]^2-1}.
\end{aligned}
$$

Compared to numerical calculations this equation provides a relative error below 1.1% for $w:h$ ratios greater than $1:1$. Another approach published in [71] models the capacitance on the sidewalls by adding 2 half-cylinders on each side of the wire cross section. Hence, the sum of a parallel plate and a cylindrical capacitor

$$
C = l\,\epsilon\left[\frac{w-\frac{t}{2}}{h}+\frac{2\pi}{\ln\left(1+\frac{2h}{t}+\sqrt{\frac{2h}{t}\left[\frac{2h}{t}+2\right]}\right)}\right] \qquad (3.2)
$$

may be used to approximate the capacitance of wires with $w \ge \frac{t}{2}$. This method is significantly less complex than equation 3.1, but calculation errors are also larger especially for narrow wires. Furthermore the compact empirical equation

$$
C = l\,\epsilon\left[1.15\frac{w}{h}+2.80\left(\frac{t}{h}\right)^{0.222}\right] \qquad (3.3)
$$

published in [72], yields to calculation errors $\le$ 6% for wires with w:h and w:t ratios of 0.3:1 to 30:1 compared to numerical calculations. Unfortunately the accuracy of this equations is not very good for wide wires beyond a w:t ratio of 30:1, which may be of

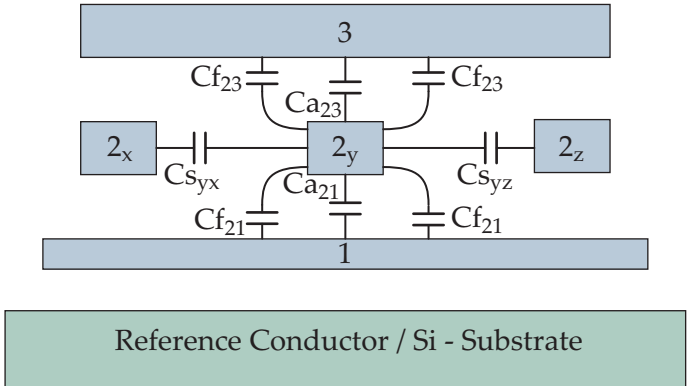

Figure 3.2 Capacitance between metal interconnects; Cs_{**} are overlap capacitors; Cf_{**} are fringing capacitors; Cs_{**} are lateral capacitors;

use for supply wires conducting high currents. Furthermore, the values obtained by the following extended empirical formula [73]

$$C = l\,\epsilon\left[\frac{w}{h} + 0.77 + 1.06\left(\frac{w}{h}\right)^{0.25} + 1.06\left(\frac{t}{h}\right)^{0.5}\right] \tag{3.4}$$

deviate not more than 6% from equation 3.1 for most on-chip wire geometries. CMOS metal interconnects consist of several stacked metal layers including partially overlapping or laterally aligned wires. The previously presented analytical equations cannot represent such structures, therefore different approaches are required to model the capacitive behavior of a complex interconnect network. Figure 3.2 illustrates the approach presented in [74] and utilized in common parasitic extraction tools, where the capacitance of a wire is treated via separate capacitors namely as overlap, lateral and fringing capacitors. The overlap capacitors (Ca) are caused by the overlapping area of conductors on two different metal layers and lateral capacitors (Cs) represent the capacitance between wires on the same layer. Furthermore, the fringing capacitors (Cf) model the capacitance between different metal layers and perpendicular wire surfaces. The corresponding capacitance values between two wires are numerically precalculated for all required metal layer combinations and stored for the extraction process. Furthermore, these capacitor parameters are scaled according to the particular layout data during the parasitic extraction process. Compared to numerical field simulations the scaling operations are very efficient and enable fast full chip capacitance extractions with decent accuracy. Additionally, accurate measurements of coupling capacitances as described in [75] may allow the inclusion of process variations to the capacitance parameters.

3.1.2 Decoupling Capacitor Arrays

Area efficient capacitor arrays enable reduced production costs, therefore capacitors using the relatively thin gate oxides are preferred in most circuits. In modern deep

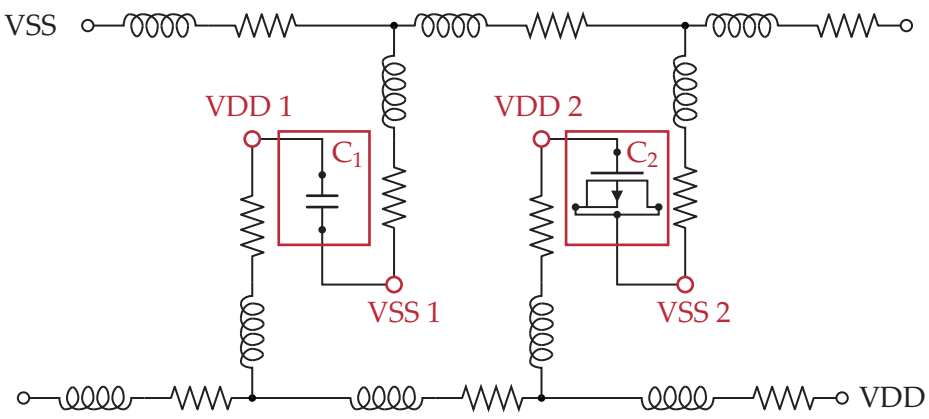

Figure 3.3 Power grid network with decoupling capacitors where C_1 and C_2 represent decoupling capacitors of two different subcircuits.

submicron technologies gate oxide thicknesses are significantly below 10 nm, even for IO or medium voltage devices. Therefore, considering the relatively large oxide thickness between metal layers, allows to roughly estimate that even capacitors using medium voltage transistors exhibit capacitance values approximately 50 times larger than the wire to ground plane capacitance of metal wires with equal dimensions [1]. Although representing only one exemplary case, this factor demonstrates clearly that the parasitic wire capacitance may be safely discarded in most power grid models, especially for the pre-layout applications discussed in this thesis.

The power grid tools provide the option to include macromodels of different decoupling capacitor types within the subcircuits directly at the local supply nodes. Figure 3.3 illustrates a RLCK network of such a power grid model where decoupling capacitors are modeled either by transistors or optionally ideal capacitors. Moreover, parameters to modify capacitor sizes analogous to the wire dimensions within the power grid model are also available. In contrast to wire parasitics, which are not represented in the circuit schematics, decoupling capacitors are treated like other circuit devices. Hence power grid tools have to scan for the original capacitors in the netlist before replacing them by parametrized capacitor models. Furthermore it is also possible to simply add decoupling capacitors which are not drawn in the schematics of the involved subcircuits.

3.2 Inductance Equations

3.2.1 Mutual Inductance of 2 Parallel Filaments

Two parallel filaments of equal length represent a basic geometry that allow exact analytical mutual inductance calculations since all required integrals may be solved

[1] e.g. assume equation 3.4 with $w = 30\ \mu m$, $t = 250\ nm$ and $h = 5\ nm$ or $h = 250\ nm$

in a closed form. Figure 3.4 illustrates this configuration and all required parameters. Considering the definition of the mutual inductance

$$M_{12} = \frac{\phi_{12}}{I_1}, \tag{3.5}$$

the flux ϕ_{12} at filament 2 invoked by I_1 has to be evaluated. The vector potential $\mathbf{A}$ defined by the line integral in A.26 and equation A.27 are exploited to obtain ϕ_{12}, therefore the following integrals have to be solved

$$\phi_{12} = \int_{x_2=0}^{l} \mathbf{A}\, dx_2 = \frac{\mu I}{4\pi} \int_{x_2=0}^{l} \int_{x_1=0}^{l} \frac{1}{R}\, dx_1\, dx_2. \tag{3.6}$$

The distance R is defined as the euclidean distance between two arbitrary points on the filaments

$$R = \sqrt{(x_2 - x_1)^2 + d^2}, \tag{3.7}$$

and applying R in equation 3.6 yields to the following equation

$$Mf_{12} = \frac{\mu}{4\pi} \int_{x_2=0}^{l} \int_{x_1=0}^{l} \frac{1}{\sqrt{(x_2 - x_1)^2 + d^2}}\, dx_1\, dx_2. \tag{3.8}$$

These integrals can be derived in a closed form utilizing the two integration formulas found in [76].

$$\int \frac{1}{\sqrt{a^2 + x^2}}\, dx = \operatorname{arsinh}\frac{x}{a} = \ln\left(x + \sqrt{a^2 + x^2}\right) \tag{3.9}$$

$$\int \operatorname{arsinh}\frac{x}{a}\, dx = x \operatorname{arsinh}\frac{x}{a} - \sqrt{a^2 + x^2} \tag{3.10}$$

The inner integral of equation 3.8 is solved using integral 3.9 and leads to

$$\begin{aligned} \int_{x_1=0}^{l} \frac{1}{\sqrt{(x_2 - x_1)^2 + d^2}}\, dx_1 &= -\operatorname{arsinh}\frac{x_2 - x_1}{d}\Bigg|_0^l \\ &= \operatorname{arsinh}\frac{x_2}{d} - \operatorname{arsinh}\frac{x_2 - l}{d}. \end{aligned} \tag{3.11}$$

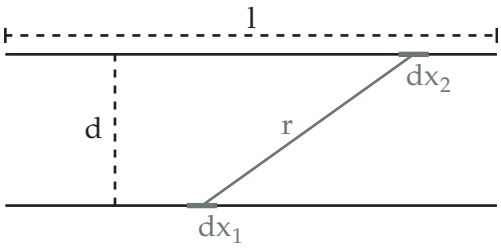

Figure 3.4 Illustration of two parallel filaments of equal length

Furthermore applying equation 3.10 to the second integral yields the following mutual inductance equation

$$\begin{aligned} Mf_{12} &= \frac{\mu}{4\pi} \int_{x_2=0}^{l} \left[\operatorname{arsinh}\frac{x_2}{d} - \operatorname{arsinh}\frac{x_2 - l}{d} \right] dx_2 \\ &= \frac{\mu}{4\pi} \left[x_2 \operatorname{arsinh}\frac{x_2}{d} - \sqrt{x_2^2 + d^2} \right. \\ &- \left. (x_2 - l) \operatorname{arsinh}\frac{x_2 - l}{d} + \sqrt{(x_2 - l)^2 + d^2} \right] \Bigg|_0^l \\ &= \frac{\mu}{2\pi} \left[l \operatorname{arsinh}\frac{l}{d} - \sqrt{l^2 + d^2} + d \right]. \end{aligned} \tag{3.12}$$

Finally the arsinh term of equation 3.12 is replaced by the equivalent logarithmic term and modifying the position of the filament length l leads to the well known mutual inductance equation for 2 parallel filaments of equal length

$$Mf_{12} = \frac{\mu}{2\pi} l \left[\ln\left(\sqrt{1 + \left(\frac{l}{d}\right)^2} + \frac{l}{d} \right) - \sqrt{1 + \left(\frac{d}{l}\right)^2} + \frac{d}{l} \right]. \tag{3.13}$$

No approximations are required to obtain equation 3.13 and the mutual inductance between distant wires with small cross sections is calculated accurately. Unfortunately, on-chip interconnect geometries that frequently exhibit large cross sections compared to wire lengths and distances are not represented well by filaments, hence equation 3.13 alone is not sufficient for accurate on-chip inductance calculations. On the other hand this case is used within more elaborate calculation methods that consider the involved wire cross sections and that are presented later in this chapter.

3.3 Inductance Calculation of Wires With Rectangular Cross Sections

Figure 3.5 shows two parallel rectangular wires where the volume of conductor 1 is V_1, the cross section is $\mathbf{S}_1$ and the direction of the current flow is $\mathbf{C}_1$. To incorporate

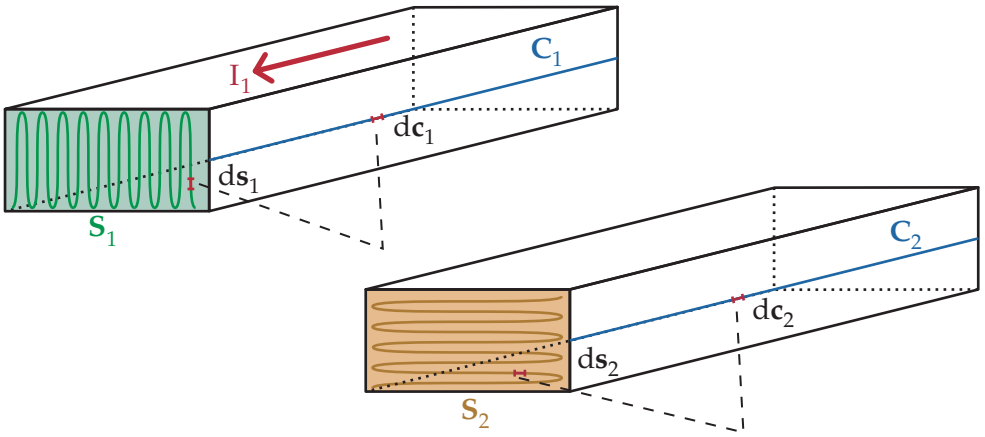

Figure 3.5 Illustration of integrals and variables required for the inductance calculation of wires with rectangular cross sections

the wire cross sections in the inductance calculations, the vector potential $\mathbf{A}_1$ is computed by equation A.25, while a constant current density $\mathbf{J_1}$ may be assumed at low frequencies. Therefore it is possible to replace $\mathbf{J_1}$ by the fraction $\frac{I_1}{s_1}$ and to rewrite the volume integral as nested integrals over the conductor cross section and the current flow direction. Hence $\mathbf{A}_1$, the vector potential of conductor 1, is calculated by

$$\mathbf{A}_1 = \frac{\mu}{4\pi} \iiint_{V_1} \frac{\mathbf{J_1}}{R} d\mathbf{v}_1 = \frac{\mu}{4\pi} \frac{I_1}{s_1} \int_{C_1} \iint_{S_1} \frac{d\mathbf{s}_1}{R}\, d\mathbf{r}_1. \tag{3.14}$$

To continue the calculation it is advantageous to take the magnetic energy stored by two filaments into account. For only one filament the energy may be found by integrating the power dissipated by the filament current $i_1(\tau)$ and the induced voltage $u_{ind1}(\tau)$. Starting with no current in the filament, the integration limit is set to the time t_1 that is needed to reach the expected current I_1. This leads to the well known magnetic energy equation

$$W_1 = -\int_{\tau=0}^{t_1} u_{ind1}(\tau)\, i_1(\tau) d\tau = L_1 \int_{\tau=0}^{t_1} i_1 \frac{di_1}{d\tau} d\tau = L_1 \int_0^{I_1} i_1 di_1 = \frac{1}{2} L_1 I_1^2. \tag{3.15}$$

Furthermore, analoguous calculations for two filaments as shown in [77] result in the following equation that describes the total magnetic energy stored by two filaments with currents I_1 and I_2

$$W_{tot} = \frac{1}{2} L_1 I_1^2 + \frac{1}{2} L_2 I_2^2 + M_{12} I_1 I_2. \tag{3.16}$$

Considering the magnetic energy stored by the mutual inductance W_{12} that may be computed by

$$W_{12} = M_{12} I_1 I_2 = \int_{C_2} I_2 \left[I_1 \frac{\mu_0}{4\pi} \int_{C_1} \frac{d\mathbf{r_1}}{R} \right] d\mathbf{r_2} = \int_{C_2} I_2\, \mathbf{A}_1(\mathbf{r}_2) d\mathbf{r_2}, \tag{3.17}$$

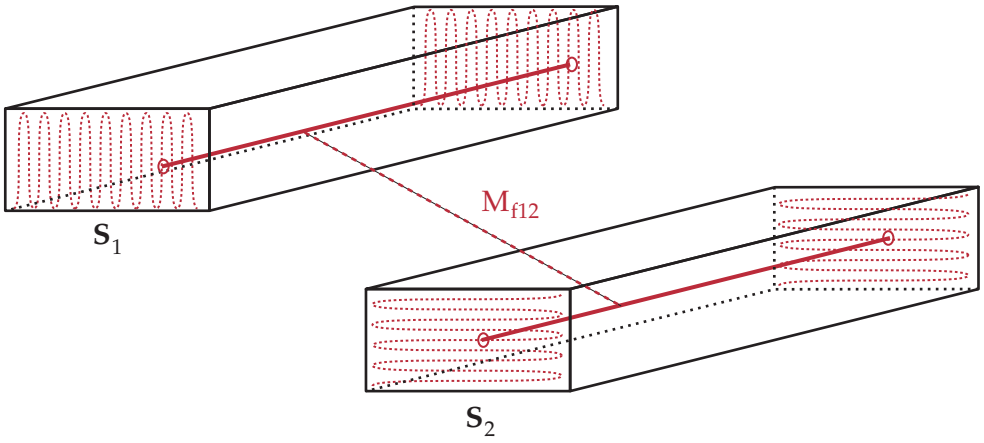

Figure 3.6 Integration of M_{f12} over the cross sections of two wires

since equation A.31 is used to calculate M_{12} and the term in square brackets represents the vector potential $\mathbf{A}_1$ of a filament (see eq. A.26). This filament based equation may be generalized for wires with real wire cross sections by using the wire volume V_2 and the current density $\mathbf{J}_2$ resulting in

$$W_{12} = \int_{V_2} \mathbf{J}_2 \cdot \mathbf{A}_1(\mathbf{r}_2) d\mathbf{r_2}. \tag{3.18}$$

Furthermore, assuming a constant current density in both wires by replacing $\mathbf{J}_2$ with $\frac{I_2}{s_2}$ and utilizing equation 3.14 allows to formulate W_{12} as

$$W_{12} = \frac{I_2}{s_2} \iint_{S_2} \int_{C_2} \mathbf{A}_1 \, d\mathbf{r}_2 \, d\mathbf{s}_2 = \frac{\mu}{4\pi} \frac{I_1 I_2}{s_1 s_2} \iint_{S_1} \iint_{S_2} \int_{C_1} \int_{C_2} \frac{1}{R} \, d\mathbf{r}_2 \, d\mathbf{r}_1 \, d\mathbf{s}_2 \, d\mathbf{s}_1. \tag{3.19}$$

Thus, dividing by the wire currents I_1 and I_2 leads to the mutual inductance of two parallel wires with cross sections S_1 and S_2

$$M_{12} = \frac{1}{s_1 s_2} \iint_{S_1} \iint_{S_2} \left[\frac{\mu}{4\pi} \int_{C_1} \int_{C_2} \frac{1}{R} \, d\mathbf{r}_2 \, d\mathbf{r}_1 \right] d\mathbf{s}_2 \, d\mathbf{s}_1. \tag{3.20}$$

As indicated by the square brackets of equation 3.20 the two line integrals are equivalent to equation 3.13 for straight parallel conductors with constant cross sections. Hence as illustrated by figure 3.6 it is possible to calculate the mutual inductance of two wires by integrating Mf_{12} over the cross sections of the involved wires.

$$M_{12} = \frac{1}{s_1 s_2} \iint_{S_1} \iint_{S_2} Mf_{12} \, d\mathbf{s}_2 \, d\mathbf{s}_1 \tag{3.21}$$

Moreover the self inductance of a wire can be calculated also by this formula using the cross section of this conductor for both surface integrals.

$$L = \frac{1}{s_1 s_1} \iint_{S_1} \iint_{S_1} Mf_{12} \, d\mathbf{s}_1 \, d\mathbf{s}_1 \tag{3.22}$$

Unfortunately the integrals of equations 3.21 or 3.22 cannot be solved analytically for rectangular wire cross sections, therefore approximations cannot be avoided to obtain compact self and mutual inductance equations. Utilizing equation 3.22, the self inductance case of a straight rectangular wire defined by width w, height t and the wire length l leads to the following integral

$$d(\mathbf{P}_1, \mathbf{P}_2) = D = |\mathbf{P}_2 - \mathbf{P}_1| = \sqrt{(x_2 - x_1)^2 + (y_2 - y_1)^2} \tag{3.23}$$

$$L = \frac{\mu}{2\pi} \frac{l}{s_1 s_1} \int_{x_1=0}^{w} \int_{y_1=0}^{t} \int_{x_2=0}^{w} \int_{y_2=0}^{t} \left[\ln\left(\sqrt{1 + \left(\frac{l}{D}\right)^2} + \frac{l}{D} \right) - \sqrt{1 + \left(\frac{D}{l}\right)^2} + \frac{D}{l} \right] dy_2\, dx_2\, dy_1\, dx_1. \tag{3.24}$$

Considering the surface integrals of 3.24 that are divided by the area of this surface reveals the obvious approximation approach of using average distances applied to Mf_{12} instead of solving the integrals directly.

3.3.1 Arithmetic Mean Distance

Figure 3.7 illustrates the concept of mean distances which is described in more detail on the following pages. Let $\mathbf{P}_1(x_1, y_1)$ and $\mathbf{P}_2(x_2, y_2)$ be two arbitrary points within rectangular areas S_1 and S_1, and two variables are introduced $z_1 = |x_1 - x_2|$ and $z_2 = |y_1 - y_2|$. The Euclidean distance between these two points is defined by

$$D = \sqrt{z_1^2 + z_2^2}. \tag{3.25}$$

Furthermore the arithmetic mean distance of two areas is the mean value of the Euclidean distances of arbitrarily chosen points inside these areas. Computing the mean value using integrals leads to

$$AMD(S_1, S_2) = \frac{1}{s_1 s_2} \iint_{S_1} \iint_{S_2} \sqrt{z_1^2 + z_2^2}\, dz_1\, dz_2. \tag{3.26}$$

For two separate conductors the solution of the arithmetic mean distance may be approximated very accurately by the Euclidean distance of the center points of both rectangles. But on the other hand the arithmetic mean distance within one single cross section which is useful for self inductance calculations requires more effort. Initially the solution for the one-dimensional case is derived [78]. The arbitrary points P_1 and P_2 lie between $0 < x < a$ and are used as two independent random variables. Their probability density function is $f(p_i) = 1/a$ between 0 and a. Moreover the density function $h(w)$ for $\mathbf{W} = \mathbf{P}_1 - \mathbf{P}_2$ is given by the following convolution integral

$$h(w) = \int_{-\infty}^{\infty} f(w - y) f(-y) dy. \tag{3.27}$$

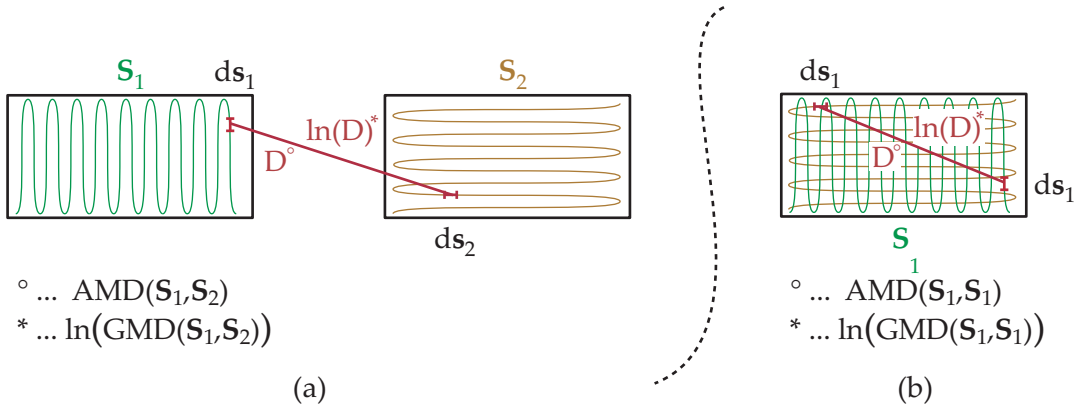

Figure 3.7 Illustration of arithmetic and geometric mean distances

Regarding $f(p_i)$ which is only non-zero between 0 and a and results in a simple relation for $h(w)$.

$$h(w) = \begin{cases} 1/a^2\,(a+w) & \text{if} \quad -a < \quad w \quad \leq 0 \\ 1/a^2\,(a-w) & \text{if} \quad 0 < \quad w \quad < a \end{cases} \tag{3.28}$$

The absolute value of w is required since absolute distance values are used in equation 3.26. Thus providing the option to add the part with $w < 0$ to the positive part of the density function leads to a density function of z with $0 < z < a$

$$k(z) = \frac{2}{a^2}\,(a-z). \tag{3.29}$$

Moreover, the AMD is then calculated as the mean value of z and results in the following simple equation

$$AMD_{1D} = \frac{2}{a^2}\int_0^a z(a-z)\,dz = \frac{a}{3}. \tag{3.30}$$

The derivation of the two dimensional case is very similar to the 1D case. Hence using the initially defined variables, the arithmetic mean distance of a rectangular cross section can be calculated with the following integral

$$AMD(w,t) = \frac{4}{w^2t^2}\int_0^w\int_0^t \sqrt{z_1^2+z_2^2}(w-z_1)(t-z_2)\,dz_2\,dz_1. \tag{3.31}$$

It is obvious that this equation allows the following rule

$$AMD(w,t) = AMD(t,w), \tag{3.32}$$

and the following useful relation may be derived also from equation 3.31

$$AMD(w,t) = wAMD(1,\frac{t}{w}). \tag{3.33}$$

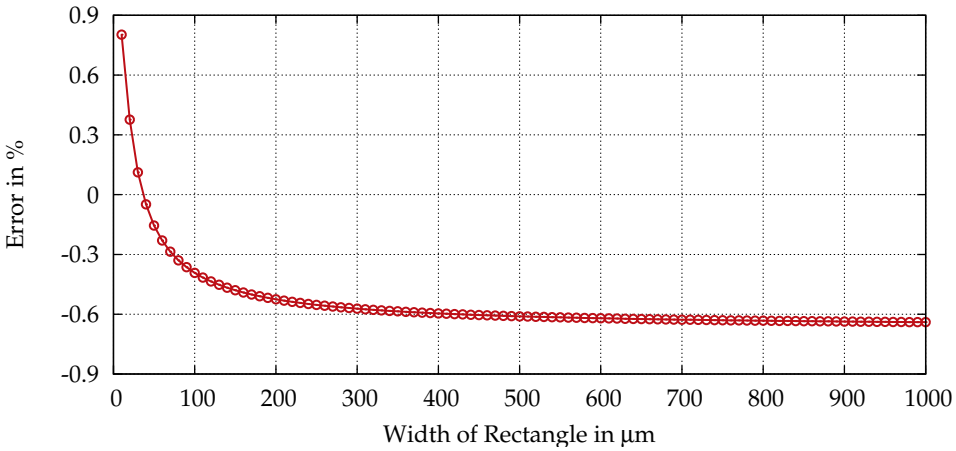

Figure 3.8 Relative error caused by a linear approximation of the arithmetic mean distance of a rectangular area using equation 3.34. The height t of the rectangle is 1 µm.

The integral of equation 3.31 has to be solved numerically but AMD(1,w/t) turns out as almost linear function that can be fitted with reasonable accuracy by the linear polynomial [78]

$$\mathrm{AMD}(1,\frac{t}{w}) \approx 0.3311\frac{t}{w} + 0.1015. \tag{3.34}$$

Figure 3.8 plots the relative error of equation 3.34 for t:w ratios of 1:1 to 1:1000 covering a sufficient range of rectangular geometries, where the linear approximation exhibits an error below 1%. Furthermore the equations 3.32 and 3.33 enable this simple linear approximation to cover rectangular wire cross sections with arbitrary width to height ratios.

3.3.2 Geometric Mean Distance

The geometric mean distance of arbitrary points in 2 rectangular areas is also important in inductance calculations. Using again the geometry shown in figure 3.7, and assuming arbitray points P_1 and P_2, the geometrical mean distance is defined by

$$\mathrm{GMD}(S_1,S_2) = \sqrt[n]{\prod_{i=1}^{n} |\mathbf{P}_{1i} - \mathbf{P}_{2i}|}. \tag{3.35}$$

While equation 3.35 itself is not directly used, the natural logarithm of the GMD is of interest, since it describes the average of the natural logarithm of the distance D between two arbitrary points in two cross sections $\mathbf{S}_1$ and $\mathbf{S}_2$ [79].

$$\begin{aligned} \ln \mathrm{GMD}(S_1,S_2) &= \frac{1}{s_1\, s_2} \iint_{S_1} \iint_{S_2} \ln D \; d\mathbf{s}_1 \; d\mathbf{s}_2 \\ &= \frac{1}{s_1\, s_2} \iint_{S_1} \iint_{S_2} \ln \sqrt{(x_2-x_1)^2+(y_2-y_1)^2} \; d\mathbf{s}_1 \; d\mathbf{s}_2 \end{aligned} \tag{3.36}$$

In contrast to the arithmetic mean distance, an analytical solution exists for integral 3.36 exploiting the following relationship published in [80, 81]

$$\frac{\delta^4 \mathbf{F}(x-x',y-y')}{\delta x \delta x' \delta y \delta y'} = -\ln\left[(x-x')^2+(y-y')^2\right] - \frac{25}{6} \tag{3.37}$$

where $\mathbf{F}(x,y)$ is defined as

$$\mathbf{F}(x,y) = \frac{x^4-6x^2y^2+y^4}{24}\ln(x^2+y^2) - \frac{xy}{3}\left(x^2\arctan\frac{y}{x}+y^2\arctan\frac{x}{y}\right). \tag{3.38}$$

Applying the wire dimensions of figure 3.18 to the integrals leads to $\ln \mathrm{GMD} =$

$$-\frac{\mathbf{F}(x-x',y-y')}{2t_1t_2w_1w_2}\Bigg|_{x=-w_1/2}^{w_1/2}\Bigg|_{x'=-w_2/2+d}^{w_2/2+d}\Bigg|_{y=-t_1/2}^{t_1/2}\Bigg|_{y'=-t_2/2+m}^{t_2/2+m} - \frac{25}{12}. \tag{3.39}$$

Unfortunately equation 3.39 is rather complex, therefore approximations are used in many inductance calculation methods. Furthermore Grover [82] published a GMD approximation for a single rectangle enabling convenient self inductance calculations. Analogous to the AMD, the GMD of a rectangle is accurately approximated by a linear function, since it is nearly proportional to the perimeter of the rectangle and may be calculated by

$$\mathrm{GMD}(S_1,S_1) = \mathrm{GMD}(w,t) \approx K(w+t) \approx 0.2235(w+t). \tag{3.40}$$

Figure 3.9 plots the relative error of equation 3.40 compared to the accurate analytical solution of equation 3.39, showing that the deviation from the accurate solution is never larger than 0.2% for all width to length ratios of interest. Furthermore the mainly used logarithm of the GMD is approximated by

$$\ln\mathrm{GMD}(w,t) = \ln(w+t) - \frac{3}{2} + \ln\epsilon. \tag{3.41}$$

Together with equations 3.40 and 3.41 a table with precalculated values of K and $\ln\epsilon$ for different w/t ratios was published in [82]. The values of K for different w:t ratios are within $0.22313 \leq K \leq 0.22369$, therefore using a fixed value of $K = 0.2235$ turns out as a reasonable approximation. Moreover, the maximum value of $\ln\epsilon$ is 0.00249 that can be discarded safely for many practical applications.

Concluding, the linear approximations of $\mathrm{AMD}(w,t)$ and $\mathrm{GMD}(w,t)$ (equations 3.34 and 3.40) will be used in the following sections for calculating the self inductance.

$$\begin{aligned} A_D &= 0.3311t + 0.1015w &&\approx \mathrm{AMD}(w,t) \\ G_D &= 0.2235(w+t) &&\approx \mathrm{GMD}(w,t) \end{aligned}$$

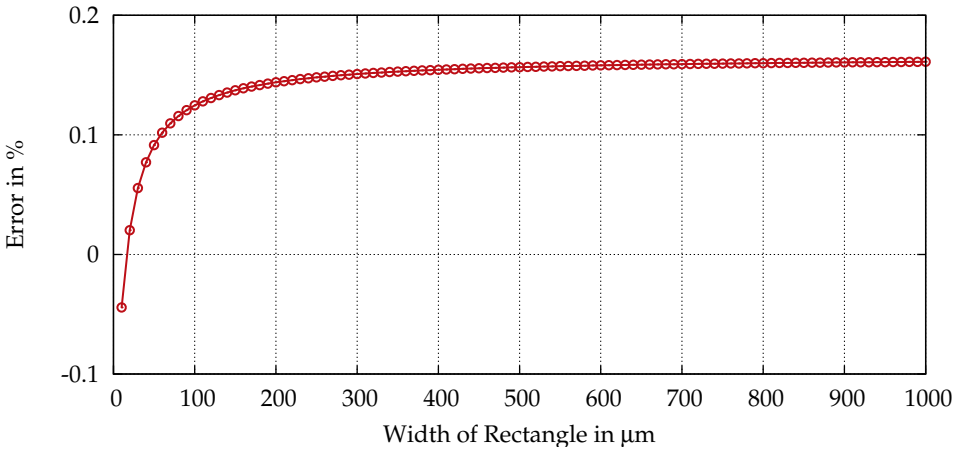

Figure 3.9 Relative error caused by a linear approximation of the geometric mean distance of a rectangular area using equation 3.40. The height t of the rectangle is 1 µm.

3.3.3 The Inductance Formula of Grover

For a wire geometry with $l >> w, t$ it is possible to simplify the square root terms within the integrals of the general self inductance equation 3.24 leading to

$$\sqrt{1+\left(\frac{l}{D}\right)^2} =\approx \frac{l}{D} \quad \text{and} \quad \sqrt{1+\left(\frac{D}{l}\right)^2} \approx 1. \tag{3.42}$$

Hence it is possible to rewrite the mutual inductance of filaments (equation 3.13) and the integral 3.24 to

$$Mf_{12} = \frac{\mu}{2\pi} l \left[\ln\left(\frac{2l}{D}\right) - 1 + \frac{D}{l}\right] \tag{3.43}$$

$$L = \frac{\mu}{2\pi}\frac{l}{w^2t^2} \int_{x_1=0}^{w}\int_{y_1=0}^{t}\int_{x_2=0}^{w}\int_{y_2=0}^{t} \left[\ln\left(\frac{2l}{D}\right) + \frac{D}{l} - 1\right] dy_{1,2}\, dx_{1,2} \tag{3.44}$$

Moreover the geometric and arithmetic mean distances are employed to avoid solving the integrals of equation 3.44 leading to the following compact inductance formula [82]

$$L = \frac{\mu}{2\pi} l \left[\ln\frac{2l}{G_D} - 1 + \frac{A_D}{l}\right]. \tag{3.45}$$

For most applications calculating geometries with $l >> w$ or t, it is feasible to discard the arithmetic mean distance term. Furthermore equation 3.45 is additionally simplified by exploiting the ln GMD relation 3.41 and results in

$$L = \frac{\mu}{2\pi} l \left[\ln\frac{2l}{w+t} + \frac{1}{2} - \ln\epsilon\right]. \tag{3.46}$$

Furthermore the following equation [83, 84] represents a popular variant of Grover's self inductance equations that provides a slightly improved accuracy compared to 3.45 for shorter wires.

$$L = \frac{\mu}{2\pi} l \left[\ln \frac{2l}{w+t} + \frac{1}{2} + 0.2235 \cdot \frac{w+t}{l} \right] \tag{3.47}$$

3.3.4 Improved Self Inductance Formula

Due to the filament approximation applied to Mf_{12}, Grover's equations are only accurate when large length to width ratios can be ensured, but for on-chip power grids this assumption does not hold. Typical grid geometries commonly include short and wide wires, since low impedance power supply lines are often preferred to minimize supply voltage ripple and electromigration defects. Unfortunately the passivity of the RLCK model demands very accurate inductance calculations which cannot be provided by equations 3.45 to 3.47. Because the simplified version of Mf_{12} (eq. 3.43) represents the major error source, strongly improved results may be obtained if the accurate version of Mf_{12} (eq. 3.13) is used instead. Analogous to the previous inductance formulas, arithmetic and geometric mean distances are employed to avoid solving the integrals of equation 3.24 what leads to the following self inductance formula

$$L = \frac{\mu}{2\pi} l \left[\ln \left(\sqrt{1 + \left(\frac{l}{G_D} \right)^2} + \frac{l}{G_D} \right) - \sqrt{1 + \left(\frac{A_D}{l} \right)^2} + \frac{A_D}{l} \right]. \tag{3.48}$$

In this case solving integrals by arithmetic and geometric mean distances is not equivalent to solving the integrals directly, but it represents a very good approximation. Figure 3.10 illustrates the accuracy of self inductance equations for different width to length ratios. Fasthenry [85, 86], an accurate numerical inductance calculation tool, was used to create the reference results, while equation 3.48 shows reasonable accurate values down to width to length ratios of 1.58:1. (see table 3.3.4)

Self inductance formulas have to be evaluated for each wire segment of the power grid, therefore compact self inductance equations are crucial to provide efficient and useful pre-layout power grid models. The self inductance formula 3.48 may be further simplified exploiting the method of Heron [87], without significantly sacrificing the accuracy. The method of Heron is an iterative approach, similar to a newton approximation, to compute the square root of a number. Let y be an arbitrary real number and $x_0 \approx \sqrt{y}$ be a first guessed or defined value of the square root, then using the following iteration approximates the accurate value of $\sqrt{y}$.

$$x_{i+1} = \frac{x_i + \frac{y}{x_i}}{2} \tag{3.49}$$

$$\lim_{i \to \infty} x_i = \sqrt{y} \tag{3.50}$$

First, the following part of equation 3.48 is simplified employing Herons method.

$$\sqrt{1 + \left(\frac{A_D}{l} \right)^2}$$

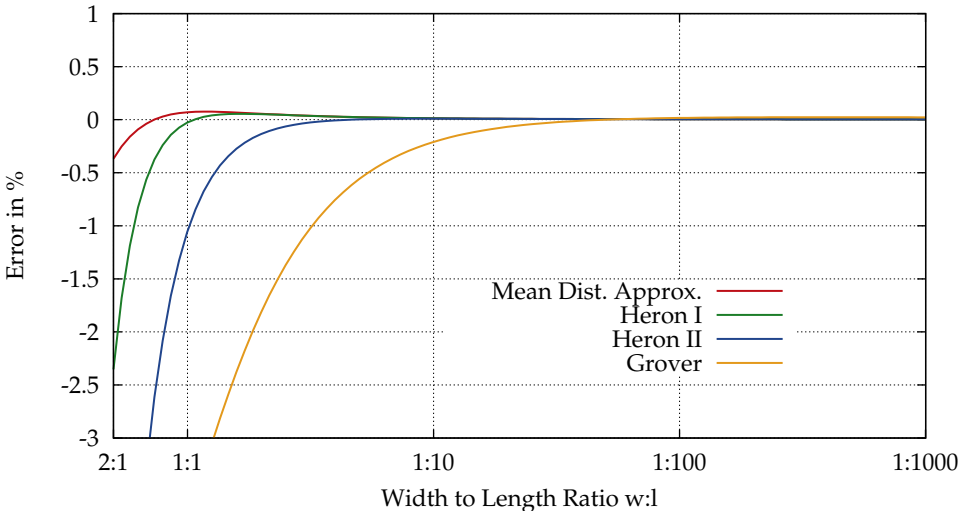

Figure 3.10 Relative error of self inductance equations compared to Fasthenry for different length to width ratios. The conductors height = 1, width = 10 and the length is swept. "Mean Dist. Approx." is eq. 3.48, "Heron I" is eq. 3.55, "Heron II" is eq. 3.56 and "Grover" is eq. 3.47.

The choice of x_0 determines the convergence rate of the iterations and therefore the accuracy of the method. For long narrow wires the filament approximation used in Grover's formulas is very accurate and this behavior has to be retained, since long wires have a dominant influence on the power grid impedance compared to short wire stubs. Hence a value for x_0 has to be selected that enables a fast convergence for long and thin wires.

$$\sqrt{1+\left(\frac{A_D}{l}\right)^2} \to 1 \quad \text{if} \quad l \gg A_D \tag{3.51}$$

Obviously the term 3.51 approaches 1 for $l \gg A_D$ and applying one iteration of equation 3.49 to the square root term using $x_0 = 1$ leads to

$$\sqrt{1+\left(\frac{A_D}{l}\right)^2} \approx 1+\frac{A_D^2}{2l^2}. \tag{3.52}$$

The other square root term of equation 3.48 is simplified in an analogous way.

$$\sqrt{1+\left(\frac{l}{G_D}\right)^2} \to \frac{l}{G_D} \quad \text{if} \quad l \gg G_D \tag{3.53}$$

To allow again fast convergence for long and thin wires with $l \gg G_D$ the term

$$x_0 = \frac{l}{G_D}$$

was selected, and therefore the following approximation is valid.

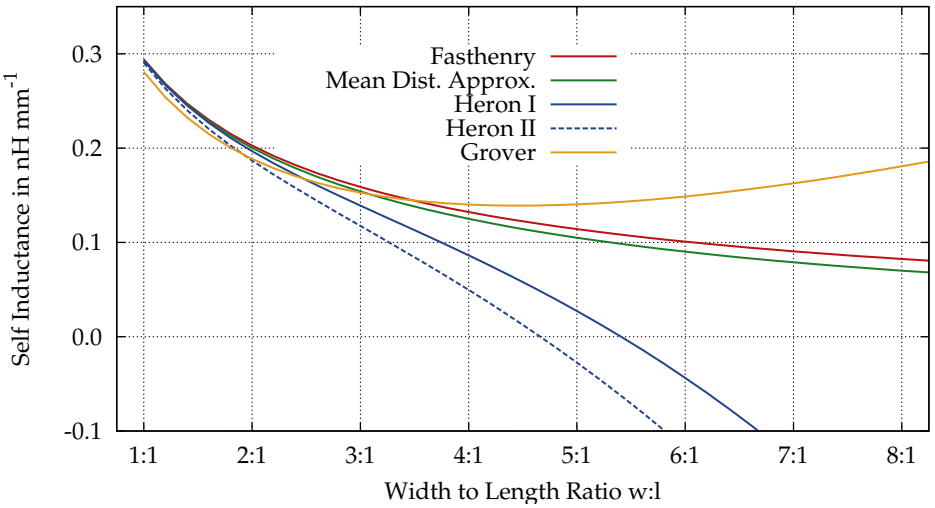

Figure 3.11 A comparison of formulas for the self inductance of short wires. The inductance value in nh per mm wire length is calculated for different width to length ratios.The conductors height = 1, width = 10 and the length is swept. "Mean Dist Approx." is eq.3.48, "Heron I" is eq. 3.55, "Heron II" is eq. 3.56 and "Grover" is eq. 3.47.

$$\sqrt{1+\left(\frac{l}{G_D}\right)^2} \approx \frac{l}{G_D}+\frac{G_D}{l} \tag{3.54}$$

Furthermore, applying these approximations to equation 3.48 results in the simplified inductance formula[2]

$$L = \frac{\mu}{2\pi}\, l \left[\ln\left(\frac{2l}{G_D}+\frac{G_D}{l}\right) - 1 - \frac{A_D^2}{2l^2}+\frac{A_D}{l}\right]. \tag{3.55}$$

The previous equation may be additionally simplified by removing the square root approximation of the logarithmic term, which does not sacrifice the accuracy too much.

$$L = \frac{\mu}{2\pi}\, l \left[\ln\left(\frac{2l}{G_D}\right) - 1 - \frac{A_D^2}{2l^2}+\frac{A_D}{l}\right] \tag{3.56}$$

The figure 3.10 compares the improved self inductance equations to Grover's self inductance formula using numerical Fasthenry [85, 86] calculations as reference results. While all equations deliver accurate results for long wires with small wire cross sections, both novel compact self inductance formulas (eqs. 3.55 and 3.56) exhibit a strongly improved accuracy for short wires compared to the inductance formula of Grover. Additionally, table 3.1 contains the length to width ratios where these equations yield to accuracies better than 0.1%. Moreover, figure 3.11 illustrates the behavior

[2] Alternatively, Taylor series expansions of the square root terms will lead to the equivalent result.

of self inductance equations for wires having width to length ratios below 1:1. The equations 3.55 and 3.56 show significant deviations from Fasthenry and even negative inductance values occur. Fortunately these geometries are not practically relevant and the resulting inductance values are in the single digit pH range and below, therefore this effect has no negative impact on the overall accuracy of power grid models. Furthermore, calculation results that lead to negative inductance values are bounded to zero in the grid model implementation to avoid effects of negative partial inductance values in Spice compatible netlists.

L Equation	No	l	:	w
Grover	3.47	15.8	:	1
Heron II	3.56	2.15	:	1
Heron I	3.55	1	:	1.1
Mean Dist. Approx.	3.48	1	:	1.58

Table 3.1: Minimum l:w ratio where the accuracy of the self inductance formulas is within 0.1% compared to Fasthenry.

3.4 Mutual Inductance Calculation

Analogous to the self inductance case, the mutual inductance of two parallel rectangular wires is calculated by solving equation 3.21. Assuming equally long wires with length l and naming conventions for the geometry parameters corresponding to figure 3.18 yields to

$$D = |\mathbf{P}_2 - \mathbf{P}_1| = \sqrt{(x_2 - x_1)^2 + (y_2 - y_1)^2} \tag{3.57}$$

$$M_{12} = \frac{\mu}{2\pi}\frac{l}{s_1 s_2} \int_{x_1=x_{p000}}^{x_{p100}} \int_{y_1=y_{p000}}^{y_{p010}} \int_{x_2=x_{q000}}^{x_{q100}} \int_{y_2=y_{q000}}^{y_{q010}} \left[\ln\left(\sqrt{1+\left(\frac{l}{D}\right)^2} + \frac{l}{D} \right) - \sqrt{1+\left(\frac{D}{l}\right)^2} + \frac{D}{l} \right] dy_2\, dx_2\, dy_1\, dx_1. \tag{3.58}$$

Due to the integrals of equation 3.58, approximations are again mandatory to obtain compact analytical mutual inductance equations. Several different approaches are evaluated in this chapter using a geometry setup illustrated in figure 3.12. Sweeping the distance d from $0\mu m$ to $1mm$ covers a multitude of different critical cases, including closely coupled, aligned, partially overlapping and also distant wires. Hence sufficient insight is gained by such simple parameter sweeps to derive appropriate mutual inductance equations for the pre-layout power grid model. Fasthenry is used again as reference, where a low frequency, thus a constant current distribution in the conductors is assumed.

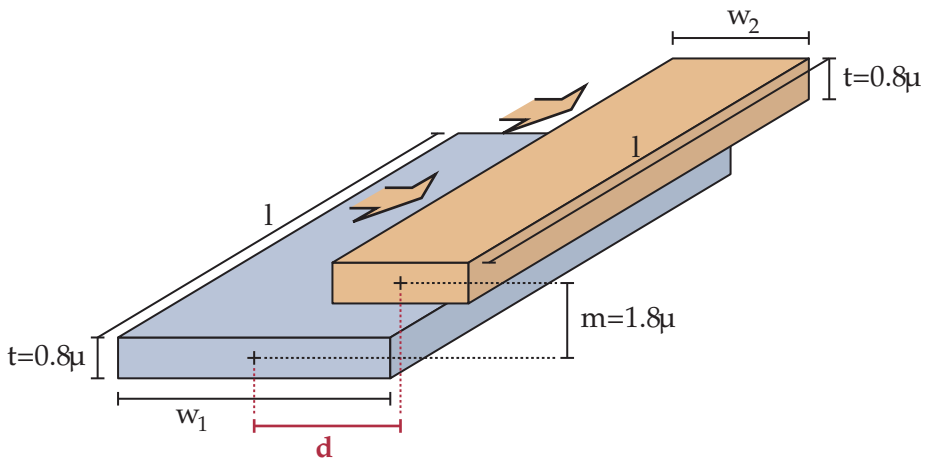

Figure 3.12 Geometry of two wires and the corresponding parameters used for the mutual inductance calculations

3.4.1 Mutual Inductance using Filament Equations

One promising approach for distant wires is the application of equation 3.13 or its simplified variant 3.43 to calculate the mutual inductance of two parallel filaments passing through the centers of both wires. It is safe to assume that the arithmetic mean distance A_D is approximated well by Euclidean distance D for most geometries that occur in on-chip interconnects. Moreover,for wires with distances significantly larger than the corresponding wire cross sections the Euclidean distance also approximates the geometric mean distance. Therefore, the figures 3.13 and 3.14 show that equation 3.13 leads to accurate results.

$$A_D \approx D = \sqrt{d^2 + m^2} \tag{3.59}$$

$$GMD(S_1, S_2) \approx D \quad when \;\; d \text{ or } m \gg w_{1,2} \text{ and } t_{1,2} \tag{3.60}$$

Furthermore it is obvious that the approximations applied to 3.43, although useful for several self inductance formulas, result in large errors rendering this formula unusable for mutual inductance calculations. Especially short wires as illustrated in figure 3.14 do require the accurate filament equation 3.13. Nevertheless, the mutual inductance of closely coupled wires is strongly overestimated by the two equations causing physically impossible coupling factors above 1.0. Since closely coupled wires are common in on-chip interconnects, more elaborate inductance equations that consider the wire cross sections are required.

3.4.2 Mutual Inductance using GMD Approximation

Similar to the self inductance calculation it is possible to avoid solving the integrals of equation 3.58 by exploiting the arithmetic and geometric mean distances. While the

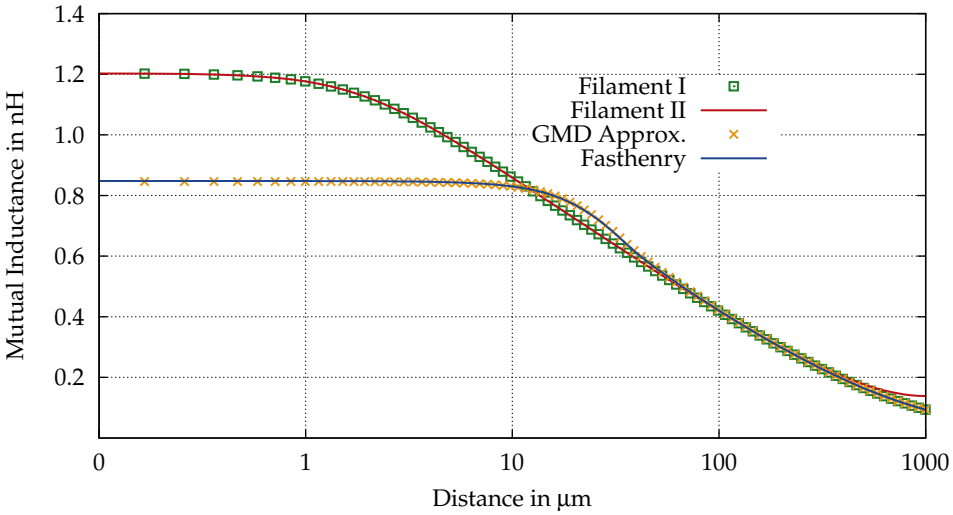

Figure 3.13 Mutual inductance of filaments compared to Fasthenry and GMD approximation for rectangular wires. Wire dimensions $w_1 = 20\,\mu m$, $t_1 = 0.8\,\mu m$, $w_2 = 10\,\mu m$, $t_2 = 0.8\,\mu m$, $m = 1\,\mu m$, $l = 1\,mm$. "GMD Approx." is eq. 3.61, "Filament I" is eq. 3.13 and "Filament II" is eq. 3.43.

arithmetic mean distance of two separated rectangular areas is again approximated by the Euclidean distance of the centers (eq. 3.59), the geometric mean distance has to be computed using equation 3.39. Hence the Mutual inductance of two rectangular wires can be approximated by

$$\begin{aligned} M_{12} &= \frac{\mu}{2\pi} l \left[\ln\left(\sqrt{1 + \left(\frac{l}{GMD(\mathbf{S}_1, \mathbf{S}_2)}\right)^2} + \frac{l}{GMD(\mathbf{S}_1, \mathbf{S}_2)} \right) \right. \\ &- \left. \sqrt{1 + \left(\frac{A_D}{l}\right)^2} + \frac{A_D}{l} \right]. \end{aligned} \tag{3.61}$$

In figures 3.13 and 3.14 equation 3.61 is compared to the previously discussed filament equations. As shown in figure 3.13, equation 3.61 allows accurate mutual inductance calculations also for closely coupled long wires where the results match well with Fasthenry. On the other hand equation 3.61 exhibits significant errors considering shorter wires as plotted in figure 3.14, even though the accuracy is still better compared to simple filament equations. The big disadvantage of this formula is the complex analytical solution of the geometric mean distance by equation 3.39. This issue prohibits the utilization of equation 3.61 in tools with only basic arithmetic capabilities like most analog circuit simulators. A more efficient GMD calculation method [88] is available that only requires basic arithmethics when combined with the GMD approximations for single rectangles (eq.3.40). But due to the fact that a more accurate approach especially for shorter wires was found, equation 3.61 is not utilized for the power grid model.

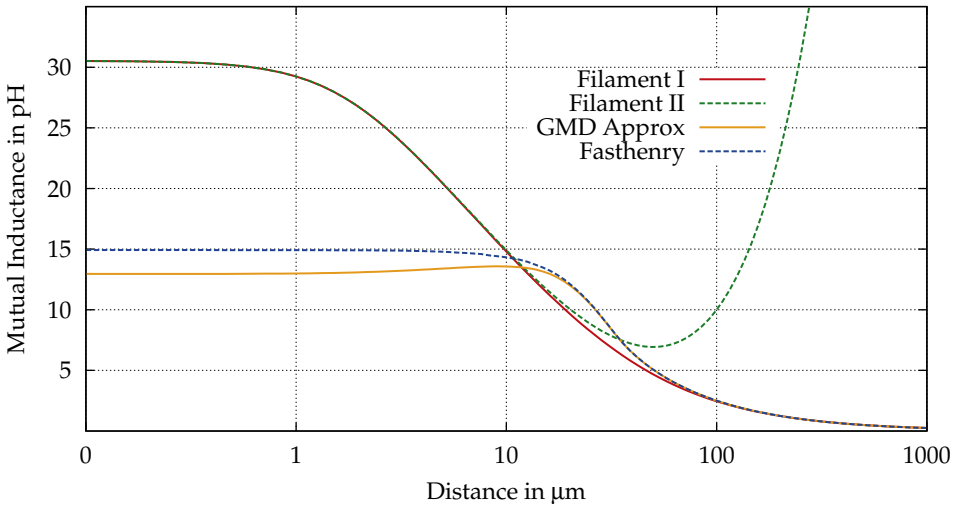

Figure 3.14 Mutual inductance of filaments compared to Fasthenry and a GMD approximation for rectangular wires. Wire dimensions $w_1 = 50\,\mu m$, $t_1 = 0.8\,\mu m$, $w_2 = 20\,\mu m$, $t_2 = 0.8\,\mu m$, $m = 1\,\mu m$, $l = 50\,\mu m$. "GMD Approx." is eq. 3.61, "Filament I" is eq. 3.13 and "Filament II" is eq. 3.43.

3.4.3 Mutual Inductance using Quadrature Formulas

The following section presents an alternative to the GMD approximation using quadrature formulas. Several points on the perimeters of the two wire cross-sections are selected as shown in figure 3.15. Furthermore the mutual inductance of filaments passing through these points are calculated and a weighted sum of these inductance values leads to a coarse approximation of the mutual inductance between these two wires. Two different approaches were evaluated, that are both illustrated in figure 3.15. One mutual inductance equation is derived from the average of all 16 mutual

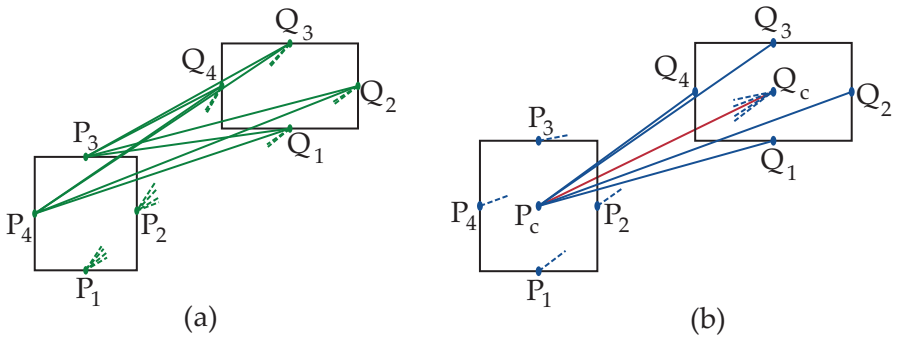

Figure 3.15 Average (a) and Rayleigh (b) quadrature approximation

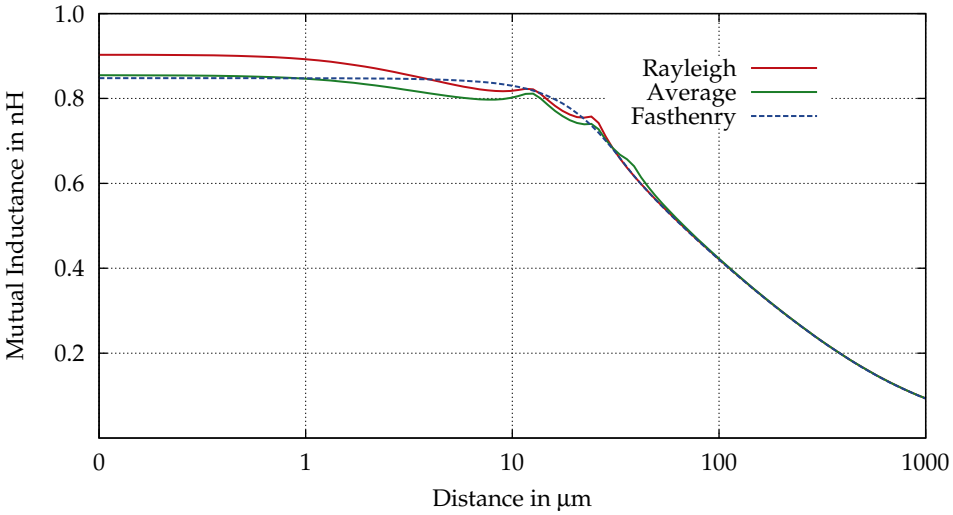

Figure 3.16 Quadrature based mutual inductance approximations compared to Fasthenry for rectangular wires. Wire dimensions $w_1 = 20\,\mu m$, $t_1 = 0.8\,\mu m$, $w_2 = 10\,\mu m$, $t_2 = 0.8\,\mu m$, $m = 1\,\mu m$, $l = 1\,mm$. "Rayleigh" is eq. 3.63, "Average" is eq. 3.62.

inductance values between the 8 points on the wire perimeters.

$$M_{12} = \frac{1}{16} \sum_{i=1}^{4} \sum_{j=1}^{4} Mf_{12}(l, |\mathbf{P}_i - \mathbf{Q}_j|) \tag{3.62}$$

The second equation is based on Rayleigh's quadrature formula as published in [82] and [89]. This quadrature formula takes the mutual inductance values from the center point of one rectangle to the 4 points on the perimeter of the second rectangle, thus requiring 9 filament equations including the mutual inductance between the two central points.

$$\begin{aligned} M_{12} &= \frac{1}{6} \Big(\sum_{i=1}^{4} Mf_{12}(l, |\mathbf{P}_i - \mathbf{P}_c|) \\ &+ \sum_{j=1}^{4} Mf_{12}(l, |\mathbf{Q}_j - \mathbf{Q}_c|) - 2 \cdot Mf_{12}(l, |\mathbf{P}_c - \mathbf{Q}_c|) \Big) \end{aligned} \tag{3.63}$$

Figure 3.16 compares these two formulas to Fasthenry results where both equations show a significantly better accuracy for small distances compared to the single filament approach. Moreover, the accuracy is also retained for short wires as shown in figure 3.17 since the utilized filament formula 3.13 does not contain any approximations. The Rayleigh quadrature exhibits a significant error for aligned wires ($d = 0$), hence using the simple average formula is preferable, even though it requires more mutual inductance terms. Quadrature formulas may be conveniently evaluated within Spice compatible grid models, but unfortunately the plots (figs. 3.16 3.17) show that

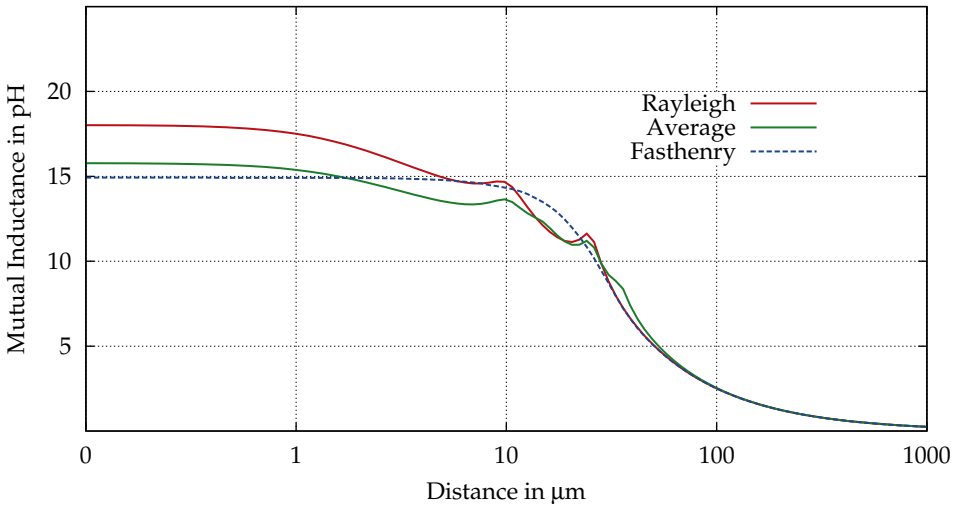

Figure 3.17 Quadrature based mutual inductance approximations compared to Fasthenry for rectangular wires. Wire dimensions $w_1 = 50\,\mu m$, $t_1 = 0.8\,\mu m$, $w_2 = 20\,\mu m$, $t_2 = 0.8\,\mu m$, $m = 1\,\mu m$, $l = 50\,\mu m$. "Rayleigh" is eq. 3.63, "Average" is eq. 3.62.

the two equations do not result in monotonic inductance to distance relations. Local maxima or minima may trap optimization tasks to wrong parameter values, or false interpretations of the parameter sweeps are possible. Since parameter sweeps and geometry optimizations represent main applications of the power grid model, both quadrature based inductance formulas are not overly useful in this context.

3.4.4 Mutual Inductance using Self Inductance Formulas

A different approach for accurate mutual inductance calculations based on self inductance terms was published in [90]. This approach is combined with the previously presented self inductance equations and modified to provide accurate results for typical on-chip wire geometries. The following relation of integrals is the key for this method, where the mutual inductance integrals of equation 3.58 are reformulated to a linear combination of integrals that correspond to self inductance terms. Let $f(x)$ be an arbitrary function, then a double integral may be rewritten by reordering the

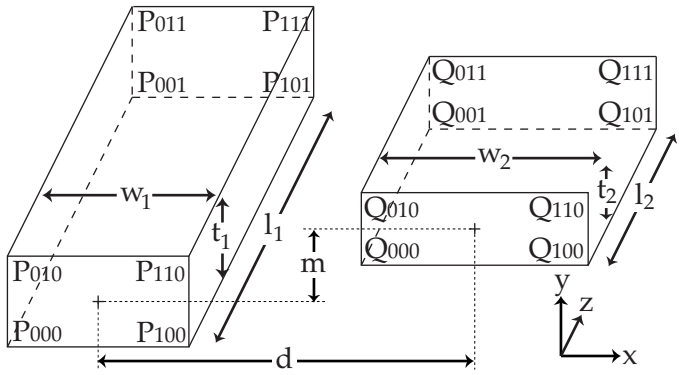

Figure 3.18 Illustration of two rectangular wires including the parameters for mutual inductance calculations.

integral limits

$$\begin{aligned}
&\int_{p_0}^{p_1}\int_{q_0}^{q_1} f(|x_0-x_1|)dx_0\,dx_1 = \\
\frac{1}{2}\Bigg(&\int_{p_0}^{q_1}\int_{p_0}^{q_1} f(|x_0-x_1|)dx_0\,dx_1 + \int_{p_1}^{q_0}\int_{p_1}^{q_0} f(|x_0-x_1|)dx_0\,dx_1 \\
-&\int_{p_0}^{q_0}\int_{p_0}^{q_0} f(|x_0-x_1|)dx_0\,dx_1 - \int_{p_1}^{q_1}\int_{p_1}^{q_1} f(|x_0-x_1|)dx_0\,dx_1\Bigg) \\
=&\ \frac{1}{2}\sum_{i,j=0}^{1}(-1)^{i+j+1}\int_{p_i}^{q_j}\int_{p_i}^{q_j} f(|x_0-x_1|)dx_0\,dx_1. \qquad (3.64)
\end{aligned}$$

Figure 3.18 illustrates two parallel rectangular wires including their corner points and parameters. Even though wires with unequal lenghts are drawn in this figure and the calculation method is capable of treating such geometry, equally long wires were assumed throughout this section. For a first less complex case a single layer structure is assumed, thus both wires have the same thickness t and they are aligned on the x/z- plane. Applying equation 3.64 on the y - axis integrals allows to rewrite equation 3.21 in conjunction with equations 3.13 and 3.57 to the following term.

$$\begin{aligned}
M_{12} &= \frac{1}{w_1 t_1 w_2 t_2}\int_{x_1=x_{p000}}^{x_{p100}}\int_{y_1=y_{p000}}^{y_{p010}}\int_{x_2=x_{q000}}^{x_{q100}}\int_{y_2=y_{q000}}^{y_{q010}} Mf_{12}(l,D)\,dx_1\,dy_1\,dx_2\,dy_2 \\
&= \frac{1}{w_1 t_1 w_2 t_2}\int_{y_1=y_{p000}}^{y_{p010}}\int_{y_2=y_{q000}}^{y_{q010}} \\
&\quad\left[\frac{1}{2}\sum_{i,j=0}^{1}(-1)^{i+j+1}\int_{x_1=x_{pi00}}^{x_{qj00}}\int_{x_2=x_{pi00}}^{x_{qj00}} Mf_{12}(l,D)\,dx_1\,dx_2\right]dy_1\,dy_2 \qquad (3.65)
\end{aligned}$$

In this particular case, the corner points on the y coordinates are equal ($y_{p010} = y_{q010} = t$ and $y_{p000} = y_{q000} = 0$), and due to the assumption that both wires have the same length and are aligned on the z - axis it is possible to modify the integral for such wires to

$$\begin{aligned} M_{12} &= \frac{1}{2}\frac{1}{w_1 t_1 w_2 t_2}\sum_{i,j=0}^{1}(-1)^{i+j+1} \\ &\int_{x_1=0}^{t}\int_{x_2=0}^{t}\int_{y_1=y_{p0i0}}^{y_{p0j0}}\int_{y_2=y_{p0i0}}^{y_{p0j0}} Mf_{12}(l,D)\,dx_1\,dx_2\,dy_1\,dy_2. \end{aligned} \tag{3.66}$$

Moreover it is obvious that the integral limits of 3.66 are equivalent to the limits used for self inductance calculations (3.22). Therefore it is possible to rewrite the mutual inductance of two wires as a weighted sum of self inductance values, and following formula is derived using the wire dimensions and the distances instead of corner points P_{xyz} or Q_{xyz}.

$$\begin{aligned} M_{12} &= \frac{1}{2}\frac{1}{w_1 w_2}\left[\left(d+\frac{w_1}{2}+\frac{w_2}{2}\right)^2 L\left(d+\frac{w_1}{2}+\frac{w_2}{2}\right)\right. \\ &- \left(d-\frac{w_1}{2}+\frac{w_2}{2}\right)^2 L\left(d-\frac{w_1}{2}+\frac{w_2}{2}\right) \\ &- \left(d+\frac{w_1}{2}-\frac{w_2}{2}\right)^2 L\left(d+\frac{w_1}{2}-\frac{w_2}{2}\right) \\ &+ \left.\left(d-\frac{w_1}{2}-\frac{w_2}{2}\right)^2 L\left(d-\frac{w_1}{2}-\frac{w_2}{2}\right)\right]. \end{aligned} \tag{3.67}$$

In equation 3.67 $L(x)$ corresponds to the self inductance of metal lines of width x and of constant length l and thickness t. These four different cross-sections are illustrated in figure 3.19 together with the required parameters. Equation 3.67 is useful for single layer structures but chip backends with metal lines that overlap on different metal layers require more degrees of freedom on the y - axis. To obtain an equation for such geometries, relation 3.64 is subsequently applied to equation 3.65 leading to

$$\begin{aligned} M_{12} &= \frac{1}{w_1 t_1 w_2 t_2}\left[\frac{1}{2}\sum_{k,l=0}^{1}(-1)^{k+l+1}\int_{y_1=y_{p0k0}}^{y_{q0l0}}\int_{y_2=y_{p0k0}}^{y_{q0l0}}\left(\frac{1}{2}\sum_{i,j=0}^{1}(-1)^{i+j+1}\right.\right. \\ &\left.\left.\int_{x_1=x_{pi00}}^{x_{qj00}}\int_{x_2=x_{pi00}}^{x_{qj00}} Mf_{12}(l,D)\,dx_1\,dx_2\right)dy_1\,dy_2\right] \\ &= \frac{1}{w_1 t_1 w_2 t_2}\left[\frac{1}{4}\sum_{i,j,k,l=0}^{1}(-1)^{i+j+k+l}\right. \\ &\left.\int_{x_1=x_{pi00}}^{x_{qj00}}\int_{x_2=x_{pi00}}^{x_{qj00}}\int_{y_1=y_{p0k0}}^{y_{q0l0}}\int_{y_2=y_{p0k0}}^{y_{q0l0}} Mf_{12}(l,D)\,dy_1\,dy_2\,dx_1\,dx_2\right]. \end{aligned} \tag{3.68}$$

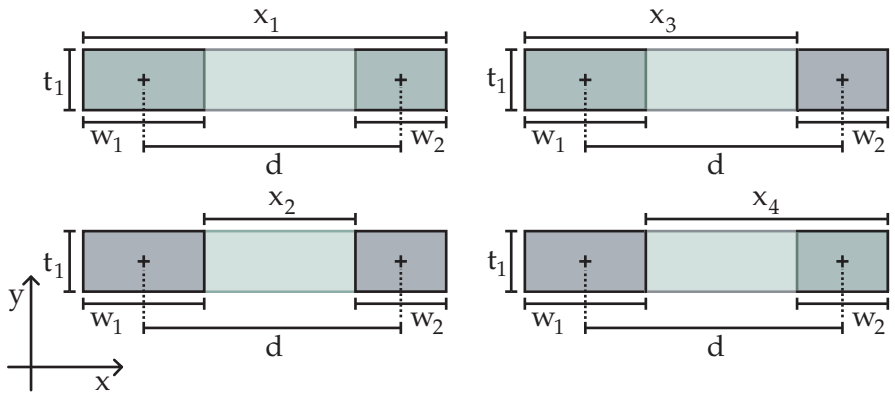

Figure 3.19 Cross sections of self inductance terms used for mutual inductance calculation (green). Cross sections of wires (grey).

Width and center point coordinates are defined in the power grid configuration file, but not the required corner point coordinates. Hence all corner points have to be expressed by the width and distance parameters illustrated in figure 3.18.

$$X_p = \begin{pmatrix} 0 & w_1 \\ 0 & w_1 \end{pmatrix} \qquad X_q = \begin{pmatrix} d + \frac{w_1}{2} - \frac{w_2}{2} & d + \frac{w_1}{2} + \frac{w_2}{2} \\ d + \frac{w_1}{2} - \frac{w_2}{2} & d + \frac{w_1}{2} + \frac{w_2}{2} \end{pmatrix}$$
$$Y_p = \begin{pmatrix} 0 & 0 \\ t_1 & t_1 \end{pmatrix} \qquad Y_q = \begin{pmatrix} m + \frac{t_1}{2} - \frac{t_2}{2} & m + \frac{t_1}{2} - \frac{t_2}{2} \\ m + \frac{t_1}{2} + \frac{t_2}{2} & m + \frac{t_1}{2} + \frac{t_2}{2} \end{pmatrix} \tag{3.69}$$

These matrices which represent the coordinates of the corner points P_{ij0} and Q_{ij0} allow a very compact writing of the mutual inductance formula.

$$\begin{aligned} A^2_{i,j,k,l} &= \Big(X_q(k,l) - X_p(i,j)\Big)^2 \Big(Y_q(k,l) - Y_p(i,j)\Big)^2 \\ L_{i,j,k,l} &= L\Big(l, |X_q(k,l) - X_p(i,j)|, |Y_q(k,l) - Y_p(i,j)|\Big) \\ M_{12} &= \frac{1}{w_1 t_1 w_2 t_2} \left[\frac{1}{4} \sum_{i,j,k,l=0}^{1} (-1)^{i+j+k+l} A^2_{i,j,k,l} L_{i,j,k,l}\right] \end{aligned} \tag{3.70}$$

$A^2_{i,j,k,l}$ computes the square of the rectangular area spanned between two corner points, while $L_{i,j,k,l}$ calculates the inductance of a corresponding wire [3] with length l. Since no approximations are necessary to obtain these formulas, the accuracy of equations 3.67 and 3.70 only depends on the self inductance formulas that are used for $L_{i,j,k,l}$. Equation 3.55 is utilized as self inductance formula in the power grid model representing a proper compromise between accuracy and compactness. Only the very complex formula used in Fasthenry [83], exhibits a significantly better accuracy, but this equation cannot be evaluated using Spice compatible arithmetic expressions. Figure 3.20 shows that equation 3.70 corresponds well with the accurate numerical results

[3] a self inductance formula with the notation "$L = L(length, width, height)$"

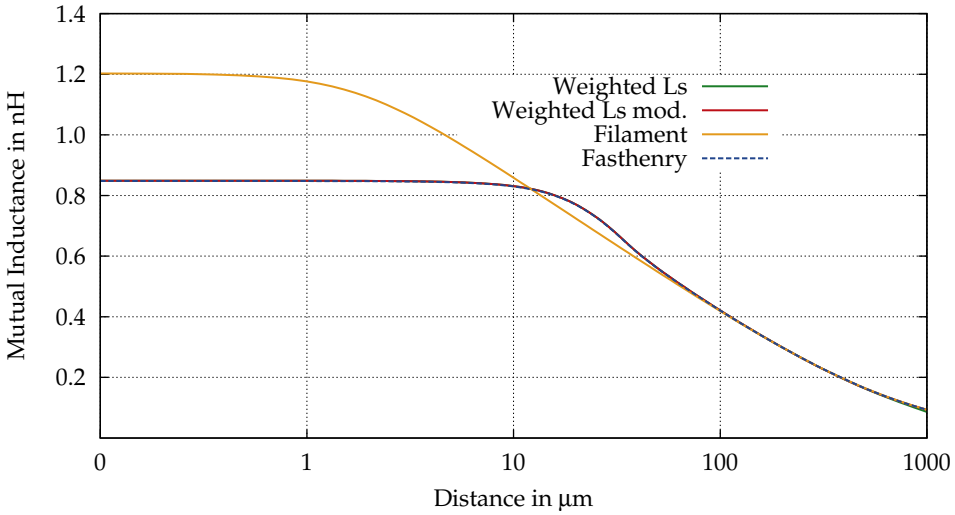

Figure 3.20 Mutual inductance approximations compared to Fasthenry for rectangular wires. Wire dimensions $w_1 = 50\,\mu m$, $t_1 = 0.8\,\mu m$, $w_2 = 20\,\mu m$, $t_2 = 0.8\,\mu m$, $m = 1\,\mu m$, $l = 1\,mm$. "Weighted Ls" is eq. 3.70, "Weighted Ls mod." is eq. 3.72 and "Filament" is eq. 3.13

obtained from Fasthenry and the approximations applied to the self inductance equation 3.55 have no negative impact on the accuracy as long as the wire length is not shorter than the distance between the wires. Unfortunately the mutual inductance calculations are also required for wire segments with a small distance to length ratio and figure 3.21 indicates the problem caused by approximated self inductance formulas for such wire geometries. Short wires and larger distances require self inductance terms in equation 3.70 with very small width to length ratios, and no simple self inductance formula presented in the previous section is capable of calculating these terms with sufficient accuracy. The simple filament equation 3.13 is utilized to circumvent this issue, since this equation calculates accurately the mutual inductance of rectangular wires with distances significantly larger than the cross sections of the wires, thus exactly of those geometries where 3.70 fails. The obvious solution is using equation 3.70 for short wire distances and switching to 3.13 for long wire distances. To avoid points of discontinuity caused by a hard switch between these equations a continuous weighting function is preferable.

$$W = \left[1 + \left(\frac{l + w_1 + w_2 + t_1 + t_2}{2(d + m)}\right)^{\alpha}\right]^{-1} \tag{3.71}$$

Equation 3.71 is an empirical weighting function useful for typical on-chip metal geometries. The metal wire cross sections are used to shift the transition between equations 3.70 and 3.13 to larger distance values if wire dimensions are relatively large. The transition rate between the weighting function limits of 1 and 0 is controlled with the factor α where larger values lead to a faster transition between these limits. A

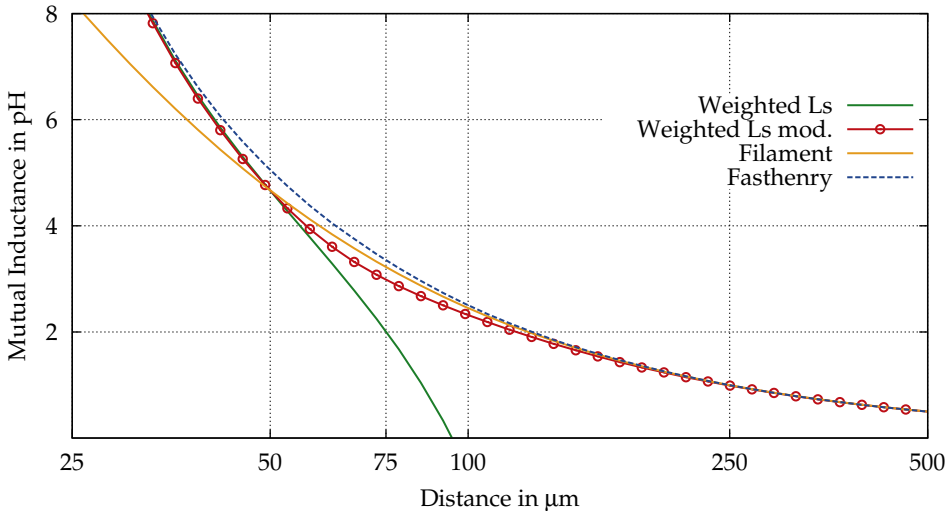

Figure 3.21 Mutual inductance approximations compared to Fasthenry for rectangular wires. Wire dimensions $w_1 = 50\,\mu m$, $t_1 = 0.8\,\mu m$, $w_2 = 20\,\mu m$, $t_2 = 0.8\,\mu m$, $m = 1\,\mu m$, $l = 50\,\mu m$. "Weighted Ls" is eq. 3.70, "Weighted Ls mod." is eq. 3.72 and "Filament" is eq. 3.13

value of $\alpha = 6$ is used in figure 3.21 and good results are obtained with this value for typical on-chip metal geometries. Finally the modified mutual inductance equation that combines filament and self inductance terms is

$$\begin{aligned} M_{12} &= \frac{1-W}{w_1 t_1 w_2 t_2}\left[\frac{1}{4}\sum_{i,j,k,l=0}^{1}(-1)^{i+j+k+l}\,A^2_{i,j,k,l}\,L_{i,j,k,l}\right] \\ &+ W\,\frac{\mu}{2\pi}\,l\left[\ln\left(\sqrt{1+\left(\frac{l}{d}\right)^2}+\frac{l}{d}\right)-\sqrt{1+\left(\frac{d}{l}\right)^2}+\frac{d}{l}\right]. \end{aligned} \tag{3.72}$$

It has to be noted that unrealistic wire dimensions were chosen for figure 3.21 that overemphasize the calculation error of (3.70) to allow a proper illustration. Beyond the small distance ranges where the transitions occur, equation (3.72) matches very well with Fasthenry results, and for realistic wire length to wire cross section ratios of 5 : 1 and more the accuracy even in the transition region is better than 1.5%.

3.4.5 Mutual Inductance Between Wires of Unequal Lengths

Since power grid models require mutual inductance calculations for arbitrarily arranged rectangular wires and not only for the simple wire geometry handled in the previous sections, analytical formulas treating such geometries are required. In contrast to figure 3.18 where the current flow is always assumed along the z axis, the power grid model is using a different coordinate system. The metal layer are stacked along the z axis and the coordinates denote the distance to the active silicon area.

Since all metal layers are planes, z is constant for each layer. Therefore the x and y coordinates are used to describe the two dimensional layout of the power grid. Since only orthogonal geometries along the x and y axes are supported by the power grid model, the wire endpoint coordinates $c[ab]_{[12]}$ illustrated in figure 3.22b are either x or y coordinates depending on the wire orientation. Since no mutual inductance occurs between perpendicular wires it needs to be calculated only for parallel wires. Fortunately the previously derived mutual inductance formulas may be applied for calculating unequal parallel wires using the following relation [83].

$$M_{12} = \frac{1}{2}\Big[M_{l_1+l_2+\delta} + M_{|\delta|} - M_{l_1+\delta} - M_{l_2+\delta}\Big] \tag{3.73}$$

Figure 3.22a illustrates 2 parallel wires and the parameter δ describing the distance or the overlapping part of both wires along the current conducting axis. The mutual inductance terms $M_{...}$ in equation 3.73 represent the mutual inductance of parallel equally long wires with the distance and the cross-sections of the actual wires and wire lengths indicated by the subscripts. A proof for equation 3.73 may be obtained by computing the mutual inductance of two parallel but otherwise different filaments Mf^*_{12}. The same integrals as in equation 3.8 but with different limits have to be solved and applying the integral rule of 3.64 on this equation leads to

$$\begin{aligned} Mf^*_{12} = \frac{\mu_0}{4\pi} \int_{ca_1}^{cb_1}\int_{ca_2}^{cb_2} \frac{dx_1\,dx_2}{\sqrt{(x_2-x_1)^2+d^2}} = \frac{\mu_0}{4\pi}\frac{1}{2}\Bigg[\\ \int_{ca_1}^{cb_2}\int_{ca_1}^{cb_2} \frac{dx_1\,dx_2}{\sqrt{(x_2-x_1)^2+d^2}} + \int_{cb_1}^{ca_2}\int_{cb_1}^{ca_2} \frac{dx_1\,dx_2}{\sqrt{(x_2-x_1)^2+d^2}} - \\ \int_{ca_1}^{ca_2}\int_{ca_1}^{ca_2} \frac{dx_1\,dx_2}{\sqrt{(x_2-x_1)^2+d^2}} - \int_{cb_1}^{cb_2}\int_{cb_1}^{cb_2} \frac{dx_1\,dx_2}{\sqrt{(x_2-x_1)^2+d^2}}\Bigg]. \end{aligned} \tag{3.74}$$

Furthermore, expressing the wire endpoint coordinates by the wire lengths l_1, l_2 and δ allows to rewrite the integrals from above as mutual inductance between equally long filaments at distance d[4].

$$\begin{aligned} Mf^*_{12} &= \frac{1}{2}\Big[Mf_{12}(d, l_1+l_2+\delta) + Mf_{12}(d, |\delta|) \\ &- Mf_{12}(d, l_1+\delta) - Mf1_2(d, l_2+\delta)\Big] \end{aligned} \tag{3.75}$$

It is obvious that the previous equation, although derived for filaments, remains valid for parallel wires with arbitrary cross sections as long as these cross sections are constant along the current flow axis.

[4] $Mf_{12}(distance, length)$; eq. 3.13

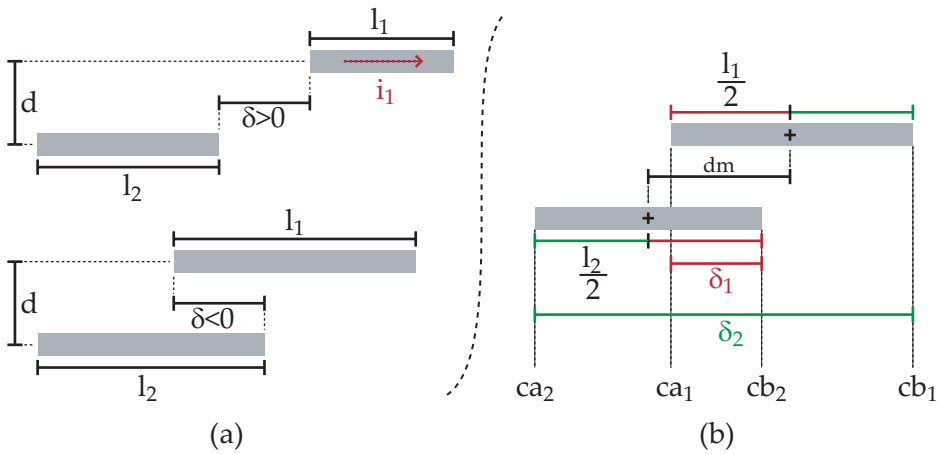

Figure 3.22 Illustration of two wires with unequal length; (a) two geometries with positive and negative δ; (b) illustration of δ computation (bird's eye view on layout)

Within the power grid model these mutual inductance terms are calculated by equation 3.72 and δ is determined by three simple relations.

$$\delta_1 = -\frac{1}{2}\Big[|cb_2 - ca_2| + |cb_1 - ca_1| - |ca_2 + cb_2 - ca_1 - cb_1|\Big] \tag{3.76}$$

$$\delta_2 = +\frac{1}{2}\Big[|cb_2 - ca_2| + |cb_1 - ca_1| + |ca_2 + cb_2 - ca_1 - cb_1|\Big] \tag{3.77}$$

$$\delta : \begin{cases} |\delta_1| \leq |\delta_2| \rightarrow \delta = \delta_1 \\ |\delta_1| > |\delta_2| \rightarrow \delta = \delta_2 \end{cases} \tag{3.78}$$

As shown by figure 3.22b, the distance between the midpoints of both wires dm together with the wire lengths l_1 and l_2 computed by

$$dm = \frac{1}{2}\Big|ca_1 + cb_1 - ca_2 - cb_2\Big| \quad \text{and} \tag{3.79}$$

$$l_x = |ca_x - cb_x| \tag{3.80}$$

are used to derive δ. The two possibilities δ_1 and δ_2 are obtained by adding or subtracting one half of both wire lengths to the midpoint distance dm, and finally the shorter distance represents the correct value of δ. Obviously this is not the most straightforward calculation method for δ since subtracting the two appropriate wire endpoints would be sufficient, but the presented approach covers all possible geometrical arrangements as shown in [91] without having to choose the right endpoints and therefore less conditional statements are required in the power grid model. Moreover the order of the endpoint coordinates is not critical, allowing parameter sweeps that change this order while the validity of the model is retained.

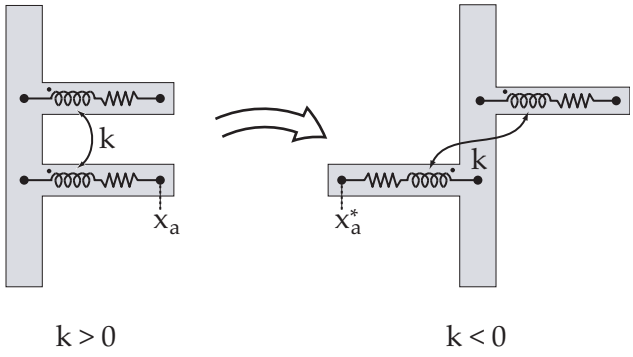

Figure 3.23 Change of coupling coefficient sign

3.4.6 Coupling Coefficients

Instead of the mutual inductance (M_{12}) the resulting Spice circuits contain coupling coefficients (k_{12}) between the self inductance elements of two wires (L_1, L_2), which are calculated by

$$|k_{12}| = \sqrt{\frac{M_{12}^2}{L_1 \cdot L_2}}. \tag{3.81}$$

The signs of these coefficients depend on the orientation of the involved self inductance elements as illustrated in figure 3.23, thus positive coupling coefficients are required if the self inductance elements exhibit equal directions, while negative coefficients are valid for opposite orientations. Since parameter alterations in the pre-layout model may change the orientation of self inductance elements (fig. 3.23 $x_a \rightarrow x_a^*$) the following equation is included in the power grid model to determine the sign for parallel wires

$$\mathrm{sign}(k_{12}) = \begin{cases} +, & (ca_1 - cb_1) \cdot (ca_2 - cb_2) > 0 \\ -, & (ca_1 - cb_1) \cdot (ca_2 - cb_2) < 0 \end{cases} \tag{3.82}$$

where ca and cb represent the coordinates of the positive (a) and negative (b) inductance terminals either along the x- or the y axis.

Finally, since the presented compact analytical inductance equations are not valid for very short wire stubs and computational issues come into play for extremely small inductance values, coupling coefficients for wire segments with inductance values $< 1 \times 10^{-16}$ H are discarded. Applying all these measures allowed the implementation of lumped element RLCK networks based on analytical equations that exhibit a reasonable accuracy and numerical robustness.

4 High Frequency Effects

Due to the integration of RF circuit blocks in CMOS chips and rising signal frequencies in the GHz range, the resistance and inductance values of on-chip wires are increasingly affected by a frequency dependent current redistribution within the wire. The previously presented inductance and resistance equations assume constant current densities in wires, but this premise is not valid for power grids of RF analog blocks or fast digital circuits. This chapter presents a method based on volume filaments to compute the skin effect in rectangular on-chip interconnects that requires only a small number of filaments.

4.1 Resistive and Inductive Skin Effect

In an uncharged conducting medium like metal interconnects the wave equations

$$\nabla^2\mathbf{E} - \epsilon\mu\frac{\partial^2\mathbf{E}}{\partial t^2} - \sigma\mu\frac{\partial\mathbf{E}}{\partial t} = 0 \quad , \quad \nabla^2\mathbf{B} - \epsilon\mu\frac{\partial^2\mathbf{B}}{\partial t^2} - \sigma\mu\frac{\partial\mathbf{B}}{\partial t} = 0 \tag{4.1}$$

derived from Maxwell's equations may be solved by the following solution describing a plane wave along the x axis

$$\psi = \psi_0 e^{-\alpha x} e^{-\jmath(\omega t - \beta x)}. \tag{4.2}$$

As described in more detail in [92] α and β are calculated by

$$\alpha = \sqrt{\frac{\epsilon\mu}{2}}\left[\sqrt{1+Q^{-2}}-1\right]^{0.5}\omega \tag{4.3}$$

$$\beta = \sqrt{\frac{\epsilon\mu}{2}}\left[\sqrt{1+Q^{-2}}+1\right]^{0.5}\omega, \tag{4.4}$$

where Q is defined as $Q = \frac{\epsilon\omega}{\sigma}$. Thus α represents the wave attenuation of both electric and magnectic waves in a conducting media, while $\frac{\omega}{\beta}$ denotes the corresponding wave velocity. Metal conductors exhibit conductivities in the order of $\sigma \approx 5 \times 10^7 \Omega^{-1}m^{-1}$ hence Q will be $\ll 1$ for all frequencies used in electronic circuits. This allows to simplify the formula for the attenuation distance δ in metals leading to

$$\delta = \frac{1}{\alpha} = \sqrt{\frac{2}{\omega\mu\sigma}}. \tag{4.5}$$

In the context of skin effect calculations δ is also called the skin depth, the distance from the wire surface where the current density J is reduced to $J_{surf} \cdot e^{-1}$. Thus, for

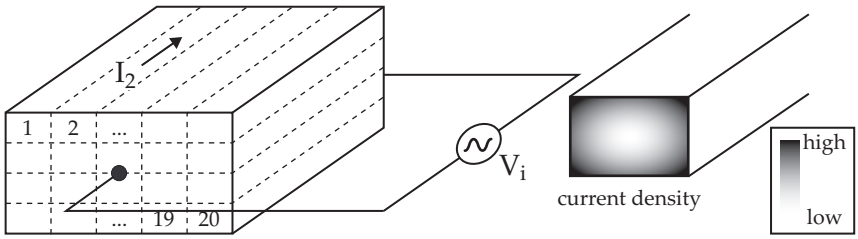

Figure 4.1 Volume filament discretization of a straight wire and an illustration of the current density affected by the skin effect.

low signal frequencies where δ is large compared to the wire dimensions, the current distribution may be assumed constant over the cross section of the wire. But with rising frequencies an exponential current distribution emerges. Since copper interconnects are dominant in modern CMOS technologies the following material parameters[1] $\rho = 16.78\ n\Omega m$ and $\mu = \mu_0$ are used throughout this chapter resulting in a skin depth smaller than 2.06 μm above 1 GHz. Therefore metal interconnects with wire widths of several μm exhibit significant changes of their impedance due to skin effect. Especially the effective wire resistance is quadratically increasing with rising frequencies and should not be discarded in interconnect models for RF applications. Unfortunately appropriate analytical methods to calculate this effect for rectangular wires are not available, hence numerical calculations or approximations derived from numerical methods have to be used.

4.2 Calculation and Modeling Methods

4.2.1 Volume Filament Discretization

Volume filament discretization [80] represents the most popular approach for calculating the current distribution within conductors. A wire geometry similar to the magnetostatic calculations of the previous chapter is assumed, where current conduction occurs along the z axis and the electrical potential is constant on the wire cross section that is parallel to the xy plane. To account for unequal current distributions the wire is subdivided in parallel segments with small cross sections as illustrated in figure 4.1. The number and the size of these segments determine the accuracy of the calculation, where wire cross sections with dimensions below the skin depth δ yield to reasonable accurate results. DC resistance and inductance values have to be calculated for all n segments and are stored in the following matrices

[1] The process dependent resistance of interconnects is slightly higher than bulk copper with values mostly around $\rho = 22\ n\Omega m$ for wire widths above 300 nm. Wires with smaller lateral dimensions will exhibit a size dependent rise of the resistance [23], nevertheless such narrow wires do not show skin effect in the required frequency range.

$$\mathcal{R} = \begin{pmatrix} R_1 & 0 & 0 & 0 \\ 0 & R_2 & 0 & \cdots \\ 0 & 0 & \cdots & 0 \\ 0 & \cdots & 0 & R_n \end{pmatrix} \qquad \mathcal{L} = \begin{pmatrix} L_{11} & M_{12} & \cdots & M_{1n} \\ M_{21} & L_{22} & \cdots & M_{2n} \\ \cdots & \cdots & \cdots & \cdots \\ M_{n1} & M_{n2} & \cdots & L_{nn} \end{pmatrix}. \tag{4.6}$$

A harmonic voltage signal $V_i = v_0 \cdot e^{\jmath\omega t}$ is applied to all segments to obtain a current vector $\mathbf{I}$ at one signal frequency ω

$$\begin{aligned} v_0 \mathbf{O}^T &= (\mathcal{R} + \jmath\omega\mathcal{L}) \cdot \mathbf{I} \quad \text{with} \quad \mathbf{O} = [1, 1, \ldots, 1] \\ \mathcal{Y} &= (\mathcal{R} + \jmath\omega\mathcal{L})^{-1} \\ \mathbf{I} &= v_0 \left[\mathcal{Y} \cdot \mathbf{O}^T\right]. \end{aligned} \tag{4.7}$$

Furthermore the effective resistance and inductance values of the whole wire are obtained by summing up the filament currents stored in $\mathbf{I}$ leading to

$$R = \frac{1}{v_0} \cdot \mathrm{Re}\left\{ \sum_{x=0}^{n} I_x \right\} \tag{4.8}$$

$$L = \frac{1}{\omega v_0} \cdot \mathrm{Im}\left\{ \sum_{x=0}^{n} I_x \right\}. \tag{4.9}$$

This method also computes the proximity effect between different wires, enabling accurate resistance and inductance calculations for complex geometries. The computational effort depends strongly on the number of filaments n, since $O(n^2)$ self and mutual inductance terms have to be computed and the required matrix inversion to obtain $\mathcal{Y}$ requires $O(n^3)$ multiplications. To reduce the computational complexity advanced methods like [93] where geometry templates that enable an optimized discretization are used. Very high signal frequencies require a large number of filaments hence other approaches like surface impedance calculations [94, 95] result in faster calculations. Furthermore empirical approximations as published in [91] may be used for fast but not overly accurate computations. Unfortunately Spice compatible circuit simulators do not support frequency dependent resistance or inductance elements, hence additional effort is required to represent skin and proximity effect in lumped element RLCK models.

4.2.2 Lumped Element Models for Wire Segments

Utilizing the elements from the $\mathcal{R}$ and $\mathcal{L}$ matrices defined in 4.6 represents the most straightforward approach to model the frequency dependency of wires. As illustrated in figure 4.2 for a 3 filament discretization, each filament is modeled as a series connection of its DC resistance (R_i) and self inductance (L_{ii}) while all filaments are coupled by the mutual inductance coefficients (k_{ij}). The big disadvantage of this approach is the very large number of required circuit elements that render analog simulations intractable except for very simple geometries. Therefore reduction techniques are required to obtain efficient power grid models.

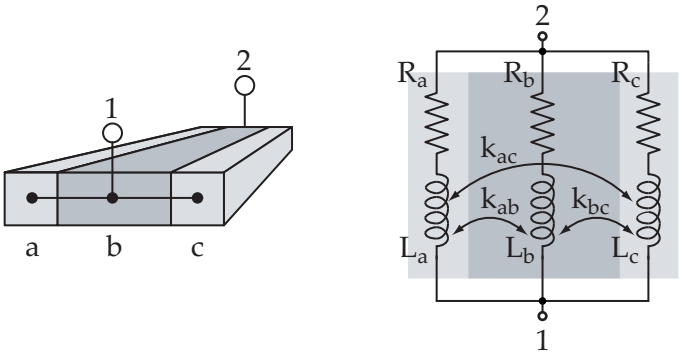

Figure 4.2 RLK network of a straight wire using three filaments

The inductance matrix $\mathcal{L}$ is real and symmetric, therefore an orthogonal matrix $\mathcal{Q}$ always exists that may be used to diagonalize the inductance matrix.

$$\mathcal{L}_{dia} = \mathcal{Q}^T \mathcal{L} \mathcal{Q} = \begin{pmatrix} L_{d1} & 0 & 0 & 0 \\ 0 & L_{d2} & 0 & \cdots \\ 0 & 0 & \cdots & 0 \\ 0 & \cdots & 0 & L_{dn} \end{pmatrix} \tag{4.10}$$

As published in [96, 97] $\mathcal{Q}$ and $\mathcal{L}_{dia}$ may be used to compute an equivalent network of n parallel RL current branches where no mutual inductance between the current branches is needed. Thus, the resistors and inductors of the equivalent network R'_i and L'_i are calculated by

$$R'_i = \frac{R_i}{q_i^2} \qquad L'_i = \frac{L_{di}}{q_i^2} \tag{4.11}$$

$$\mathbf{O}\mathcal{Q} = [q_1, q_2, \ldots, q_n]. \tag{4.12}$$

Even though finding $\mathcal{Q}$ is computationally expensive since eigenvalues have to be found, circuit simulations may benefit from the strongly reduced number of elements in interconnect model. Nevertheless, the reduction potential of this method is limited since mutual inductance between different wire segments are not removed.

Another popular approach to model frequency dependent impedance values with constant lumped elements are ladder networks as illustrated in figure 4.3. In this case the frequency dependent impedance $Z(\omega)$ is modeled by rational polynomials like

$$Z(\jmath\omega) \approx \frac{N(\jmath\omega)}{D(\jmath\omega)} = \sum_{k=0}^{n} \frac{R_k(\jmath\omega)}{(\jmath\omega) + p_k} \tag{4.13}$$

where $N(\jmath\omega)$ represents the nominator and $D(\jmath\omega)$ the denominator of the polynomial. One common fitting approach are Foster networks shown in figure 4.3a that use pole and residue pairs to approximate the wire impedance. These pairs are determined by solving linear equation systems [98] derived from equation 4.13 using measured or

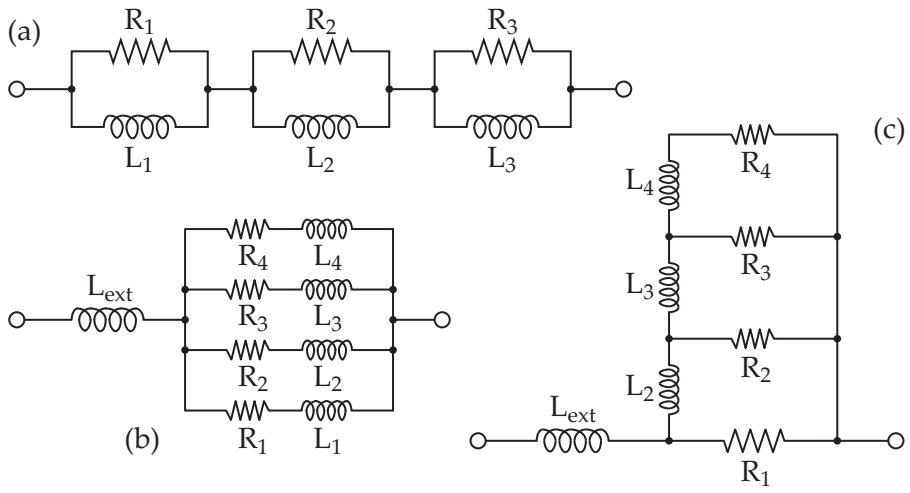

Figure 4.3 Ladder networks for modeling the skin effect. (a) is a Foster network;(b) and (c) are ladder networks with separate external inductance.

simulated $Z(\jmath\omega)$ values for at least as many different frequencies as poles are added to the Foster network. Figure 4.3b and 4.3c show alternative implementations of ladder networks where the frequency independent external inductance is treated separately and either ladder or parallel networks model the frequency dependent resistance and internal inductance values.

$$L_{ext} = L_{DC} - L_{int} \tag{4.14}$$

The ladder network in figure 4.3c has a direct physical interpretation for the resistance R_i which represent concentric shells of a circular conductor. Starting with R_1 in the high frequency case more and more inner shells start conducting at lower frequencies. Several mostly empirical strategies exist to obtain appropriate values for these R_i and L_i elements. In [99] R_1, L_2 together with the factors RR and LL are selected empirically leading to a geometric progression for the ladder elements where

$$R_{i+1} = \frac{R_i}{RR} \quad \text{and} \quad L_{i+1} = \frac{LL}{L_i}. \tag{4.15}$$

This approach does not consider the aspect ratio of rectangular wires, therefore an improved approach published in [100] is more useful for on-chip interconnects. Since resistance values are far more affected by the skin effect, the ladder network calibration of this method considers only the frequency dependent resistance, while wire inductance values are implicitly modeled with decent accuracy. Separating the wire inductance in internal (L_{int}) and external (L_{ext}) inductance simplifies the application of ladder topologies in partial element networks. Discarding the proximity effect it may be assumed that the internal inductance is not affected by the magnetic flux from other wire segments, hence mutual inductive couplings need to link only the external

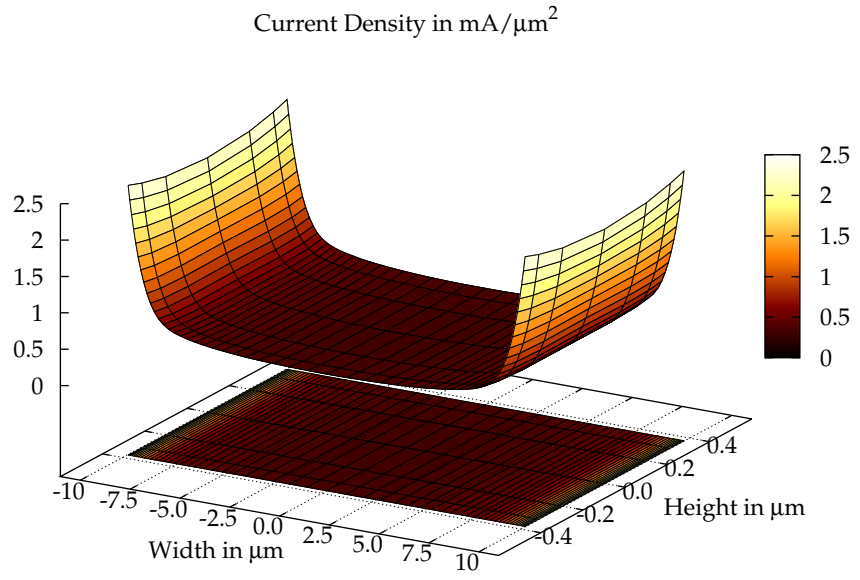

Figure 4.4 Current density of an on-chip metal wire with rectangular cross section. Both the 3D curve and the color data on the XY-plane illustrate the non-constant current density within a wire cross section having a width of 20 µm and a height of 0.8 µm. The signal frequency was set to 20 GHz.

inductance elements. Hence, the number of mutual inductance elements is significantly lower in such networks compared to a network directly derived from volume filament discretization where all filaments of all wire wire segments have to be linked. While a compact accurate internal inductance formula is available for round wires with

$$L_{int} = \frac{\mu l}{8\pi}, \tag{4.16}$$

rectangular cross sections have to be computed numerically [101] and curve fitted approximations like in [100] may be used for fast calculations. The presented ladder networks do not incorporate the proximity effect in their results, but a second similar ladder network in parallel to the topology of figure 4.3c may be used to model two parallel wire segments where proximity effect may be considered [102, 99].

One main feature of the pre layout power grid model is its scalability by user defined parameters and modeling the skin effect should not affect this feature. But unfortunately none of the presented methods to generate reduced lumped element models can be implemented as a simple set of equations, since they all require certain methods like eigenvalue decompositions, quadrature based optimization or other algorithms to compute the ladder networks. Therefore, a volume filament discretization and a direct realization of the corresponding RLK networks as illustrated in figure 4.2

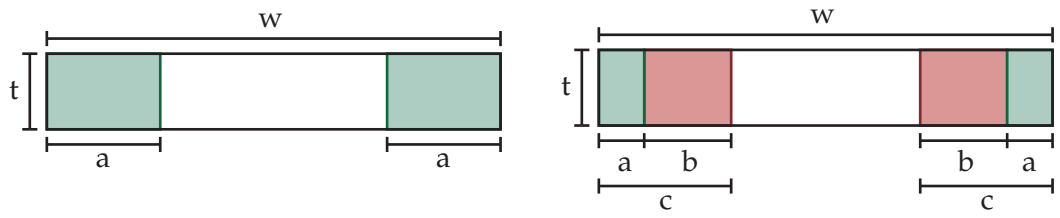

Figure 4.5 Volume filament subdivision using three or five filaments

turned out as the most practical approach for this application. Skin and proximity effects are correctly modeled by this method for all supported grid geometries and the analytical equations presented in the previous chapter may be used to compute the circuit elements. Thus, only an additional discretization step had to be included in the power grid tools.

4.3 Efficient Volume Filament Discretization

The biggest drawback of volume filaments, the complexity of the resulting RLCK networks, can be alleviated by minimizing the number of filaments. The discretization approach presented in this chapter and employed in the power grid models is tailored for typical on chip interconnect geometries, while a frequency range up to 20 GHz is assumed that covers the majority of current RF applications. For this frequency the resistance value of copper $\rho = 16.78\ n\Omega m$ leads to a skin depth of $\delta = 0.461\ \mu m$. Figure 4.4 show the cross section of a rectangular wire and the current density at 20 GHz that was calculated numerically by Fasthenry [85] using a very fine discretization. The skin effect is developed only laterally along the wire width, whereas the current density remains almost constant over the wire thickness. Since current CMOS processes rarely use metal layer thicknesses above 1 μm, it is safe to assume that skin effect occurs only laterally in the required frequency range.

This behavior allows a very simplified and coarse discretization strategy illustrated in figure 4.5 where only three or five filaments are used. Obviously, the filament sizes a and b have direct influence on the approximation accuracy. Larger filaments lead to more accurate calculations at lower frequencies where the skin effect starts to show its influence, whereas smaller filaments improve the results at higher signal frequencies. Therefore, analogous to the calibration of ladder networks, the filament sizes can be optimized to approach the desired frequency response using the expected maximum signal frequency (f_m) and the wire width (w) as independent variables. Resistance and inductance values for the wire used in the current density plot 4.4 are shown in the figures 4.6 or 4.7, illustrating that resistance values rise exponentially with increasing signal frequencies, while the partial self inductance is decreased by the internal inductance that vanishes at high frequencies. The internal inductance is only a small fraction of the total self inductance like approximately 2.2% for this particular wire,

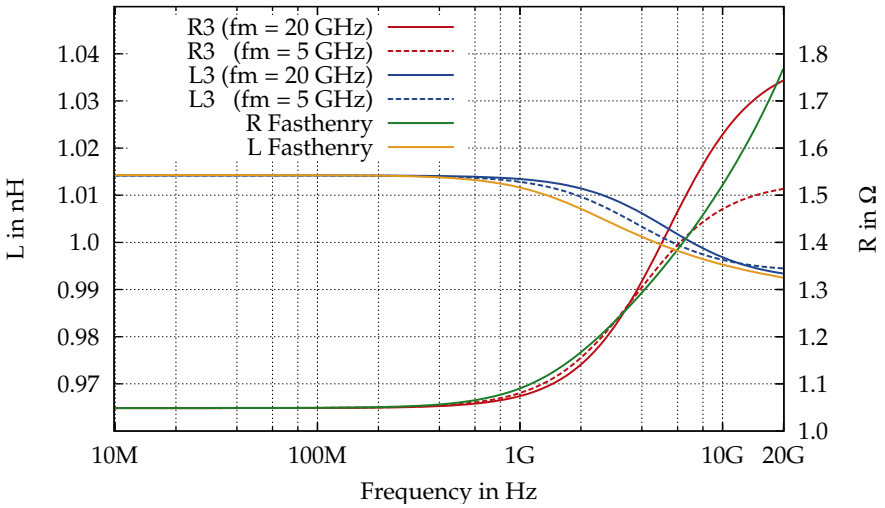

Figure 4.6 Skin effect approximation using 3 filaments for a wire with $w = 20\mu m$, $t = 0.8\mu m$. f_m represents the maximum signal frequency for this approximation.

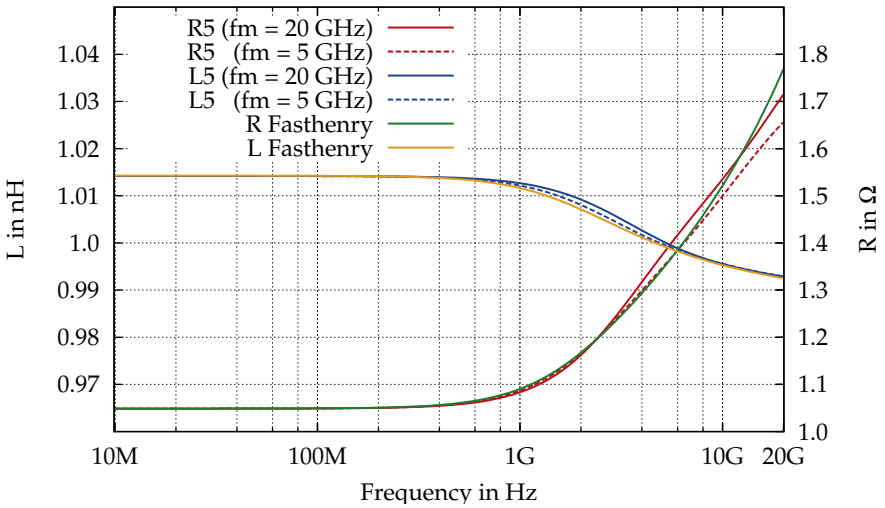

Figure 4.7 Skin effect approximation using 5 filaments for a wire with $w = 20\mu m$, $t = 0.8\mu m$. f_m represents the maximum signal frequency for this approximation.

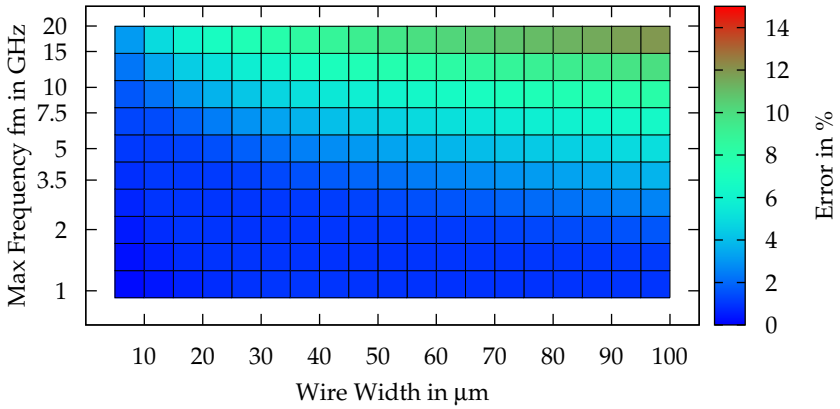

Figure 4.8 Error map for the 3 filament approximation. The frequency f_m is used to compute the filament size, and the maximum error is obtained for a frequency from DC to f_m.

therefore calculation errors of the skin effect approximation will have only a minor impact on the total wire inductance. Consequently the quality of the resistance approximation was targeted during the evaluation of ideal filament sizes, whereas self inductance calculations turned out sufficiently accurate when these "optimized for resistance" filaments were utilized. Numerical resistance values were computed by Fasthenry as accurate reference results for wire widths ranging from 5 µm to 100 µm and for several frequency points up to 20 GHz. Furthermore, sweeping the parameters a and b yielded ideal filament dimensions for each particular wire width and frequency point. Considering the very coarse discretization and the target for very simple discretization rules, a numerical curve fitting process was discarded. Instead this data was used to identify and adjust manually appropriate fitting functions for the filament dimensions. For the three filament case the following empirical rule

$$a = 60 \cdot w^{0.7} \cdot \delta^{0.7} \tag{4.17}$$

results in reasonable accurate ($< 5\%$ error) skin effect approximations for wire widths up to 10 µm in the desired frequency range. The skin depth δ is used in equation 4.17 to account for the maximum expected signal frequency (f_m) and for the DC resistance of the conducting material. Nevertheless 3 filaments may not offer sufficient accuracy for wire widths above 10 µm so additionally discretization rules using five filaments are proposed for such wires.

$$\begin{aligned} c &= 150 \cdot w \cdot \delta^{0.5} \\ a &= c \cdot \left(\frac{2 \times 10^{-6}}{w}\right)^{0.5} \\ b &= c - a \end{aligned} \tag{4.18}$$

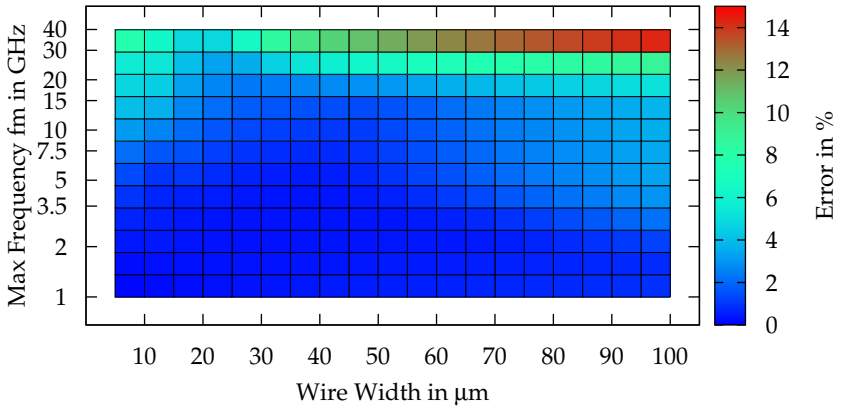

Figure 4.9 Error Map for 5 Filament Approximation. The frequency f_m is used to compute the filament size, and the maximum error is obtained for a frequency from DC to f_m.

An alternative approach for lateral subdivisions was utilized in [103], where adjacent filaments scale with a constant factor, thus more filaments are required compared to the presented method to obtain good approximations.

4.3.1 Calculation Results

To provide an overview of the achieved accuracy, error maps are plotted in the figures 4.8 and 4.9. These maps show the maximum deviation from numerical Fasthenry data for a certain wire width and maximum signal frequency f_m. This frequency is used to determine the filament sizes and the maximum error is calculated within a frequency range from DC to f_m. Figure 4.8 shows the results for the three filament discretization where errors around 5% can be maintained for all wires up to 5 GHz and narrow wires up to 10 µm maintain this accuracy for the complete required frequency range. Figure 4.9 plots the results for the five filament discretization showing errors around or below 5% for frequencies below 20 GHz within the complete range of wire widths, while frequencies up to 40 GHz were plotted to illustrate the limits of this approach. Furthermore, the figures 4.6 and 4.7 show the effect of different values for f_m on the accuracy of the approximation confirming the advantages of adapting the filament size to the required frequency range.

4.4 Test Structures

Even though considerable effort was spent in analyzing partial element calculations for simple parallel wires, test structures were required to validate the accuracy of

the power grid models for more complicated geometries. Planar spiral inductors, although normally not used as a supply structure, turned out as valuable test applications, since calculation errors of wire segments accumulate over the inductor turns, and computationally critical cases like very closely coupled adjacent wire segments or weakly coupled segments at the opposite sides of the spiral have to be computed. Moreover, skin and proximity effect also have significant influence on the behavior of planar inductors providing additional challenges for the grid model. Reference calculations were again performed by Fasthenry using very dense wire discretizations to provide accurate calculations for the required frequency range. The grid models were included in Spice netlists and simulated by Titan, the Infineon analog circuit simulator, where S-parameter analysis was used to obtain inductance and resistance values at the inductor terminals. A 3 filament skin effect approximation was used in the grid model and the maximum working frequency was set to 5 GHz, but plots up to 20GHz illustrate the increasing error due to skin effect approximations beyond the predefined frequency range.

4.4.1 Description of Figures

The plot 4.11 compares simple spiral inductors illustrated in figure 4.10, where ”Spiral 1” consists of one single metal layer and ”Spiral 2” is using two stacked and parallel connected layers. Both spiral inductors exhibit the same dimensions and the wire cross sections of the two metal layers are also equal. Furthermore, planar transformers were calculated to show that more complex geometries can be handled with good accuracy by the lumped RLCK model. A planar transformer is illustrated figure 4.12 where different colors are used to identify easily primary and secondary windings. A winding ratio of 1:2 was used hence the absolute impedance values of the secondary windings are scaled accordingly to allow plotting them to figure 4.13. Furthermore, the relative errors of the grid model are plotted in figure 4.14. The symmetric planar transformer of figure 4.16 was used for testing the ability of the software to correctly calculate a combination of three subcircuits, where a central part on the toplevel is connected to two instances of the same spiral model. One instance is mirrored to obtain a symmetric geometry, and again a winding ratio of 1:2 called for scaled impedance values in plot 4.17. Additionally the relative error of the symmetric transformer model is shown in figure 4.15.

4.4.2 Notes on Planar Spiral Inductors

Modeling of planar spiral inductors is a major research topic in RF circuit design, therefore the pre layout grid models are discussed here in relation to special purpose spiral inductor models. Accurate inductor calculations are typically performed by numerical field solver and the results are incorporated in s-parameter based multi-port networks. Because such numerical simulations are time consuming, a calculation of spiral inductors by partial elements may be preferable. Inductance and wire resis-

tance calculations may use similar methods like the power grid model as shown in [81, 103, 104], but especially wire to substrate capacitance and substrate losses should not be discarded in useful inductor models. Compact physical models as presented in [105] include such second order effects and even patterened ground shields to improve the quality factor are considered [106]. On the other hand, power integrity simulations mainly focus on metal interconnect impedance, hence substrate losses are not required in pre-layout power grid models. Therefore reusing the grid models for inductors is not advisable, except for estimating inductance values and quality factors. Nevertheless the parameterized nature of the grid models enables applications like geometry optimizations, optionally together with active devices, what is not viable using other inductor models. Even though inductor modeling was never in the focus of the thesis, the presented inductance and resistance calculations represent a decent base for parameterized planar inductor models.

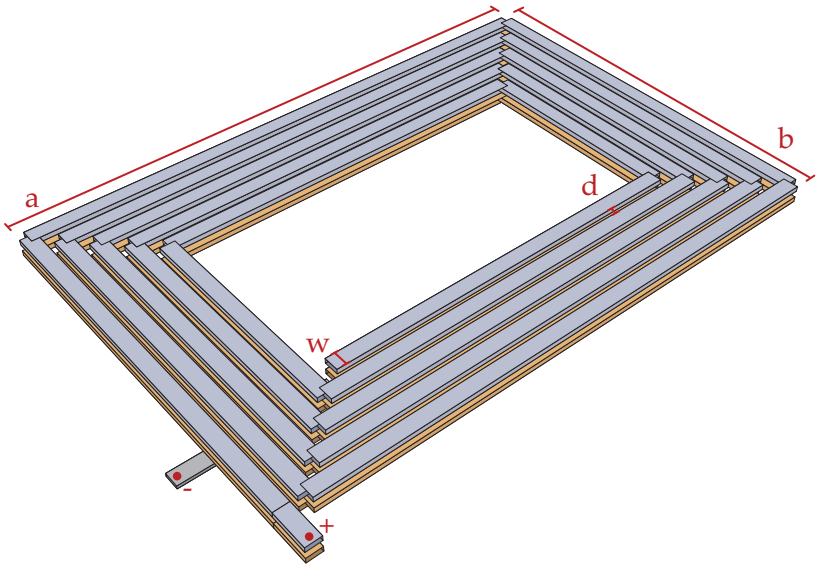

Figure 4.10 Illustration of planar spiral inductor with 2 stacked metal layers in parallel $a = 300\mu$, $b = 200\mu m$, $w = 8\mu m$, $d = 3.5\mu m$, $t = 0.8\mu m$.

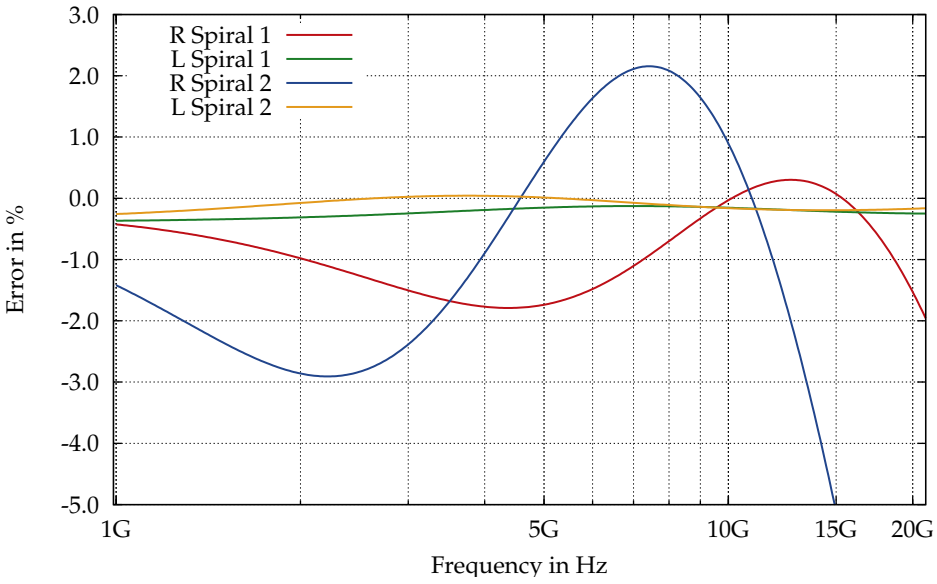

Figure 4.11 Error of RLCK model of spiral inductors (figure 4.10). Spiral 2 has two parallel metal layers. Spiral 1 uses only one layer.

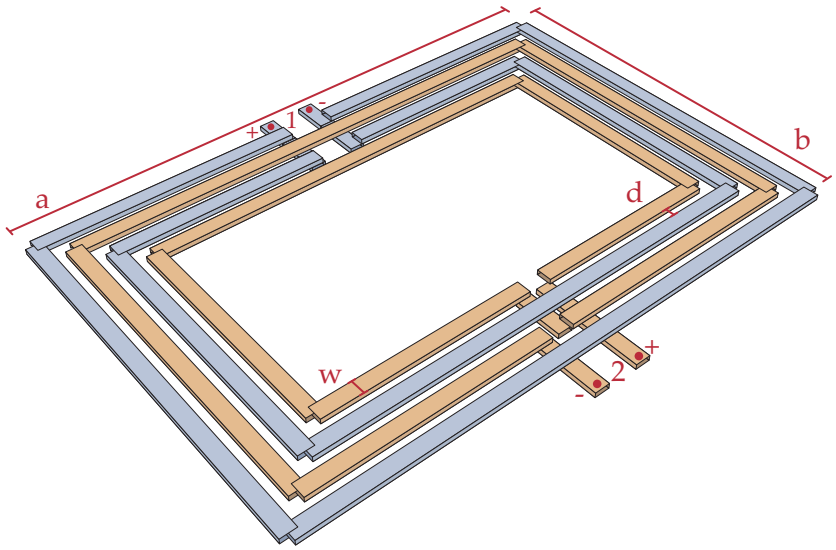

Figure 4.12 Illustration of planar transformer with a = 300µm, b = 200µm, w = 8µm, d = 1.5µm, t = 0.8µm.

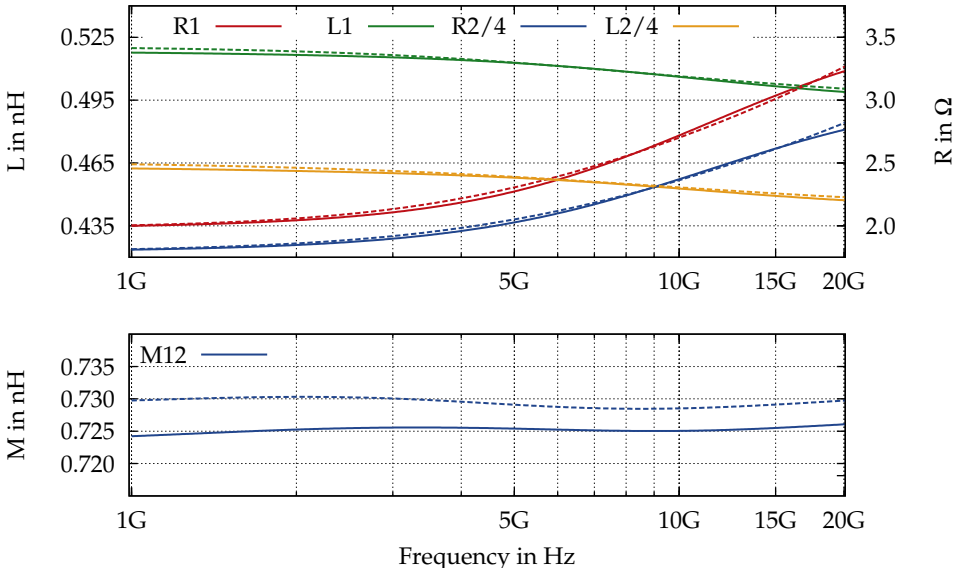

Figure 4.13 Simulation results of planar transformer (4.12) Fasthenry results are plotted in dashed style.

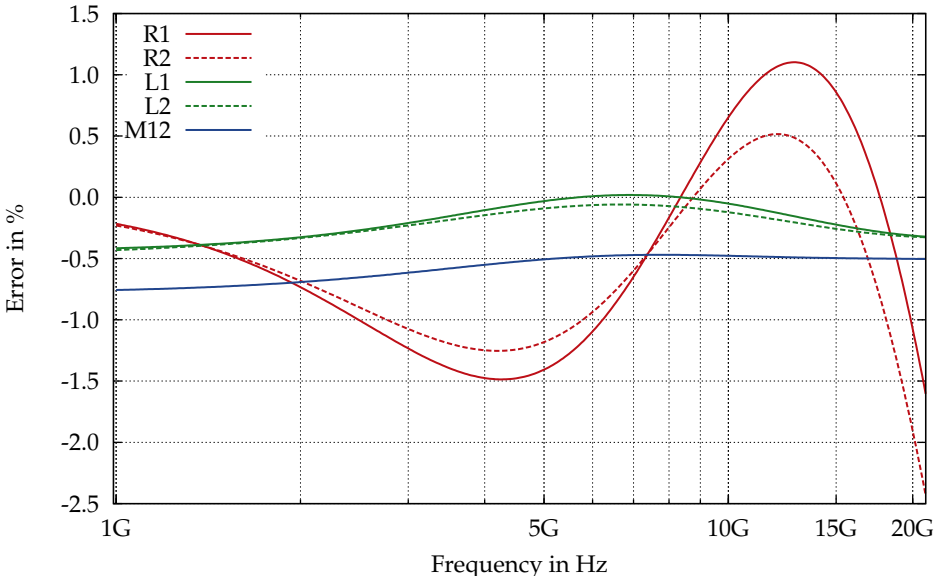

Figure 4.14 Error of RLCK model of planar transformer (4.12)

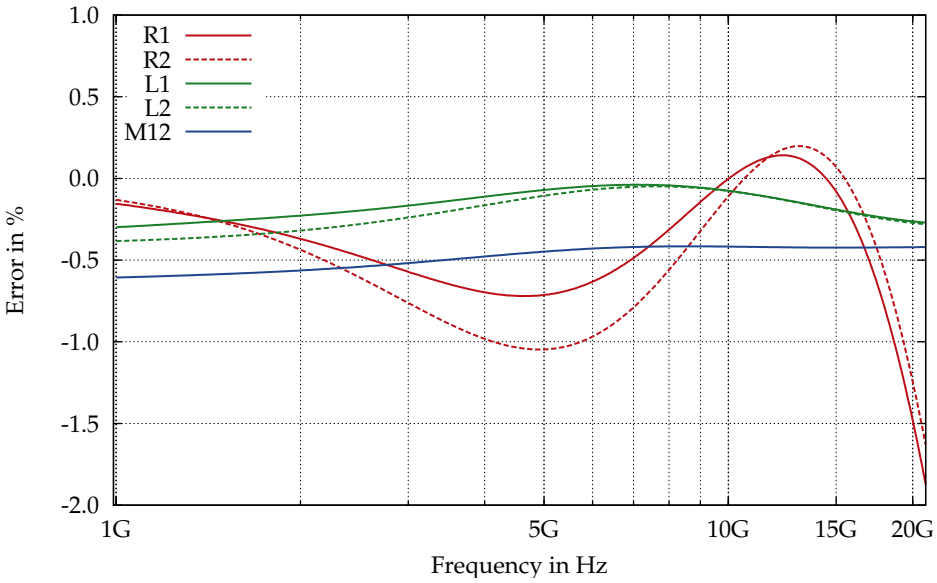

Figure 4.15 Error of RLCK model of planar transformer (4.16)

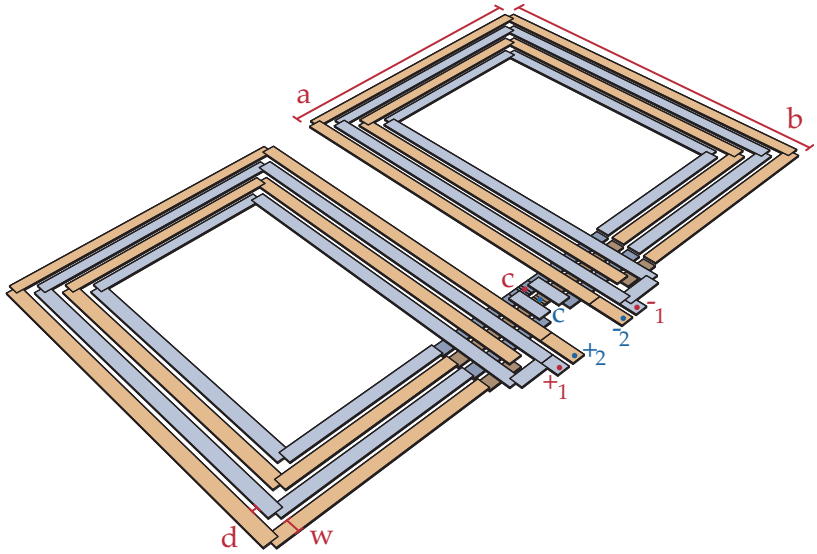

Figure 4.16 Illustration of symmetric planar transformer with a = 300µm, b = 200µm, w = 7µm, d = 2.5µm, t = 0.8µm.

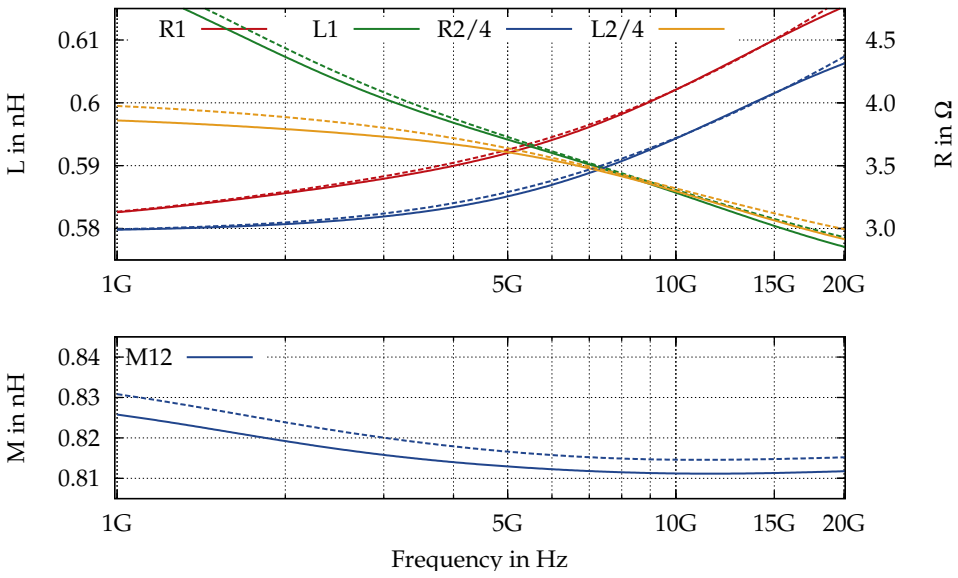

Figure 4.17 Simulation results of symmetric planar transformer (4.16) Fasthenry results are plotted in dashed style.

5 Implementation Details of the Power Grid Software

This chapter presents in detail the structure of the pre-layout power grid model and how it is included in the original circuit netlist. Since most parasitic extraction tools in industrial environments do no provide hierarchical models, a selection of data structures and algorithms that enable such hierarchical and parametrized models are presented in more detail.

5.1 The Structure of Pre-Layout Power Grid Models

Circuit hierarchies are flattened in most parasitic extraction applications where it is necessary to rename all affected circuit nodes and elements in the simulation netlists. Moreover the extracted and inserted RLCK elements result in cluttered and complex netlists that prohibit a convenient and efficient simulation flow. The pre-layout power grid model presented in this section retains the original circuit structure based on hierarchical schematics, therefore it has to be structured analogous to the original netlist. The model is focused on interconnects between subcircuits not on single Spice elements, and provides a level of abstraction that allows an efficient grid modeling process. Moreover it enables fast circuits simulations, because the number of RLCK elements is often orders of magnitude smaller than in post layout extracted netlists.

The interconnect model is separated into several grid sub-blocks to retain the hierarchical circuit structures, where each sub-block corresponds to one particular subcircuit and one supply node. These grid blocks are connected to the original supply node within the subcircuit and these blocks provide local supply nodes for circuit blocks at the next lower hierarchy level. The grid blocks are stored as separate subcircuits to maintain a clearly arranged structure especially when multiple independent power domains are modeled within a subcircuit. Figure 5.1 illustrates the tree-like structure of a supply grid with three hierarchy levels that connects several circuit blocks to VDD on toplevel. The shaded blocks represent the power grid circuit blocks that are generated by the pre-layout power grid tools, and the grid block terminals are directly connected to the local VDD nodes of each subcircuit. Multiple voltage domains are inherently supported where one grid block per supply domain is integrated in the original subcircuits and this approach is also used to model the required ground or VSS networks. The power grid configurations described in detail in appendix B represent this structure, where geometry definitions are entered separately for each grid

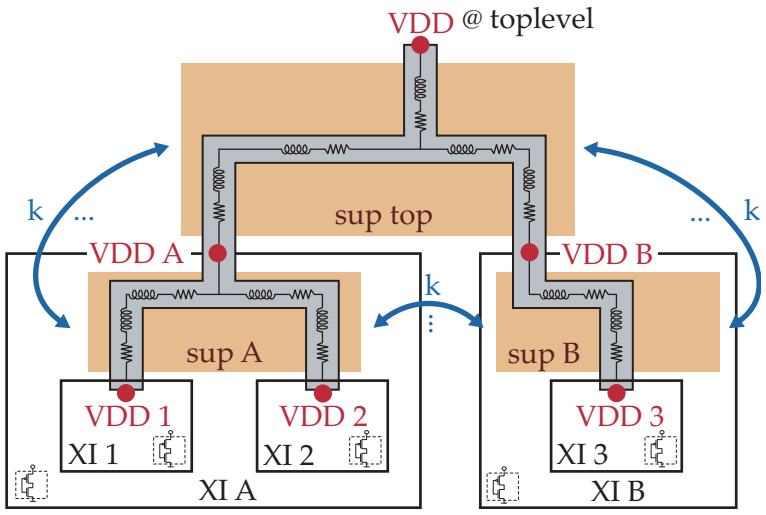

Figure 5.1 Illustration of a hierarchical power grid model for VDD on toplevel connecting several subcircuits. (Grid models for ground networks exhibit an equal structure.)

block and supply domain. These geometry definitions use local coordinate systems, where coordinates of the local supply node that connects to the parent circuit is used as reference point to derive the global position of the block. Therefore geometry modifications of grid blocks on higher hierarchy levels are automatically considered in all dependent child blocks ensuring meaningful grid geometries.

Furthermore, figure 5.2 shows parts of a typical circuit netlist where the lines belonging to the power grid models are indicated by several colors. All subcircuit definitions including the grid blocks are placed on the toplevel to provide compatible netlists also for Spice simulators that do not support nested subcircuit definitions. Grid subcircuits contain the RLK elements that model the wire interconnect impedance, and instances of these grid blocks are inserted into the original circuit blocks. The grid subcircuit terminal nodes are connected to local supply nodes that are generated by the power grid tools in each subcircuit. To inherently support multiple instances of decoupling capacitors it is necessary to inserted these power grid elements directly into the original subcircuits and not into the grid sub-blocks. In many applications decoupling capacitor arrays are already included in the original schematics and the power grid tools allow to replace these elements by parametrized capacitor models. Therefore storing these models at the place of the original elements is an obvious approach.

Mutual inductance elements are stored in two different places. Local coupling coefficients of wire segments in the same grid subcircuit are stored inside this block and therefore do not require any hierarchy prefixes. Elements that mutually couple wires in different grid sub-blocks eventually on different hierarchy levels are stored on the

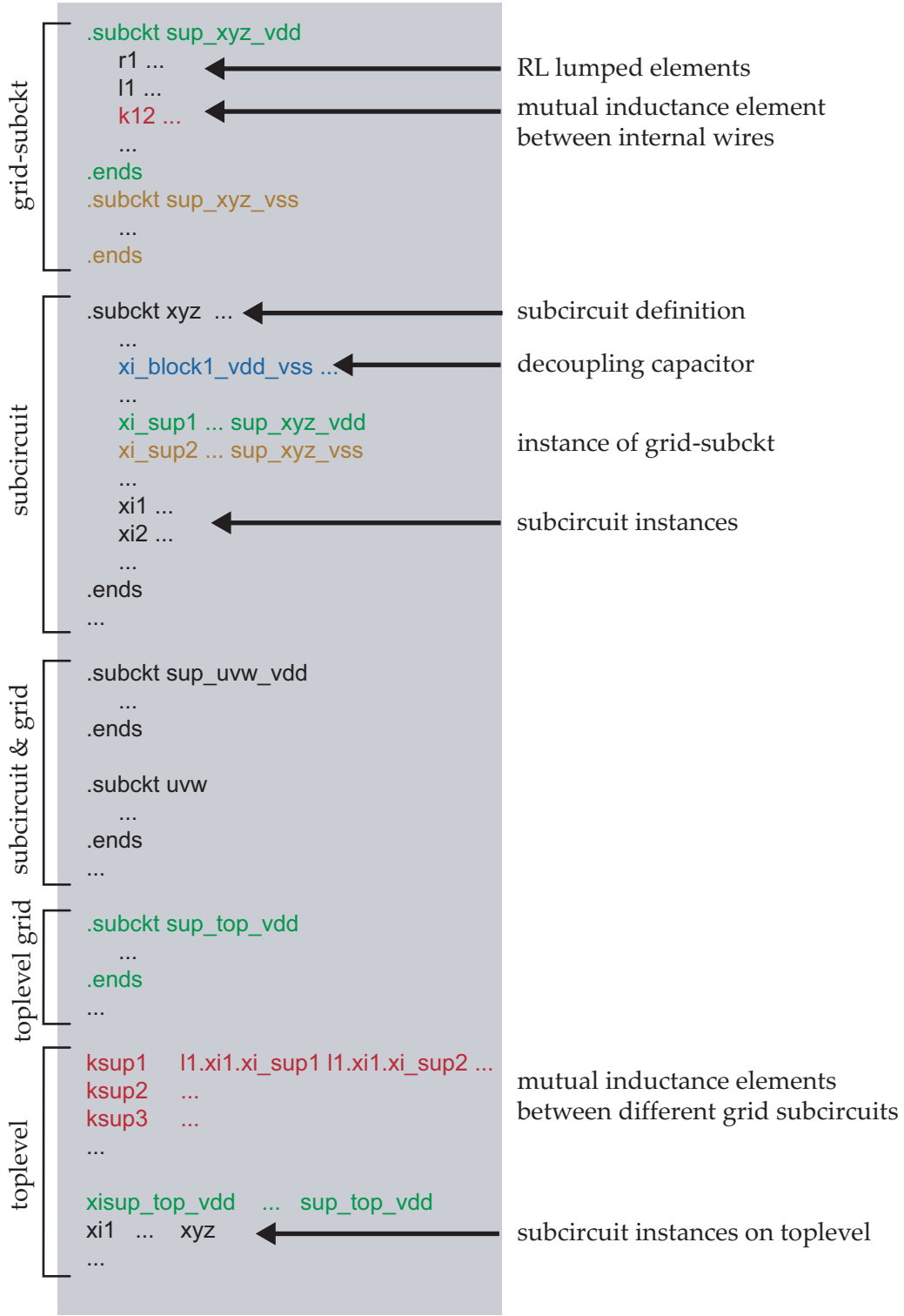

Figure 5.2 Typical structure of a Spice netlist that was patched by the pre-layout power grid tool and contains a RLCK grid model.

toplevel of the netlist, and hierarchy prefixes are added to reach the corresponding inductance elements. Fortunately mutual inductance elements do not require additional circuit nodes or other modifications to the original circuit, hence the original circuit hierarchy is not changed by K elements on the toplevel. Only the simulation speed is affected when complex grid geometries are modeled. Furthermore, besides storing the K elements, the toplevel of the circuit is treated similar to normal subcircuits.

5.2 Data Structures for Symbolic Data Processing

Since the pre-layout power grid models utilize a set of spice compatible arithmetic expressions to compute the grid geometry and RLCK element values, a special data structure is used in all affected algorithms. Spice compatible parameter definitions always exhibit the following syntax

$$\overbrace{.\mathrm{param}}^{\text{keyword}} \ \overbrace{\mathrm{something}}^{\text{name}} \ = \ \overbrace{'\mathrm{expression}'}^{\text{expression or value}} \ , \tag{5.1}$$

and numerical values of geometry parameters are also derived in the software enabling plausibility checks and the graphical output. Therefore, a three field record is utilized for each data point.

$$\mathrm{data} \rightarrow \begin{cases} \mathrm{parameter\ name}, & \text{e.g.} \quad x_{vvd} \\ \mathrm{expression}, & \text{e.g.} \quad '330u + 3 \cdot w_1' \\ \mathrm{numerical\ value}, & \text{e.g.} \quad 50 \times 10^{-6} \end{cases} \tag{5.2}$$

A relatively large number of dependent parameters have to be created for the grid model to support features like nested local coordinate systems, rotation commands or filaments for skin effect approximations. Hence, this record significantly simplifies the software implementation by providing consistent access to all three representations of data points. Fortunately Spice and Perl utilize an equivalent syntax for basic arithmetic expressions, thus the standard built in Perl evaluation function could be used to compute the numerical value of data points. Numerical values of grid parameters are not stored in the resulting model, but the software tool requires them for several operations, like evaluating the order of wire segments on a bus, which depends on the coordinates of the connection noded. Furthermore it should be noted, that this record is not fully populated for each data point, because not all data representations are required for every parameter [1].

To support user defined parameter definitions, a dictionary storing this data is populated during the input parsing procedure, where all related expressions are evaluated. This dictionary is only required for the user input in contrast to all other data points that are generated later when the model is synthesized. The number of configuration parameters is significantly and in many cases two orders of magnitude smaller

[1] e.g. numerical values of RLCK values are never computed during the model generation

than the number of derived data points, hence the execution speed and the memory consumption of the power grid tool is not affected by searching and filling a large parameter dictionary.

5.3 Data Structures and Algorithms for Hierarchical Models

As illustrated in figure 5.1, the power grid model is integrated within the hierarchy of the original netlist. Therefore, object oriented data structures are required that provide the required information of the circuit structure and also of the power grid elements.

5.3.1 Data Structures

- **netlist related data objects**
  These data object are created during the parsing procedure of the original netlist, and contain the netlist related data like line numbers of important Spice elements or node names of subcircuits, while the netlist itself is stored in a separate data structure.
  - **Subcircuit** Each subcircuit of the original netlist is described by one of these objects.
  - **Instance** The instance object is used in subcircuit and contains netlist related data of subcircuit instances defined within a certain circuit block.
  - **Hierarchy** Hierarchy is generated as a linked list that exhibits a tree like structure that is equivalent to the circuit hierarchy. It is utilized by several algorithms to iterate correctly through the circuit hierarchy.
- **power grid related data objects**
  These objects contain the parameters of the grid model like coordinates wire dimensions or rotation commands.
  - **GridData** contains the data from the grid configuration file.
  - **WireData** is used to store coordinates and dimensions of single wire segments.
  - **InstData** represents a single grid block in the power grid model. This object is required in addition to GridData because grid blocks may be instantiated several times. Even though these grid blocks are derived from the same GridData object, several parameters are unique for each instance like global coordinates and rotation commands.

Most of these data objects are strongly related to each other like each **WireData** object corresponds to an **InstData** object and every grid instance is linked to netlist related data objects. Within the power grid generation procedures a convenient access to all these data object is required, therefore an object named **GridDB** was created that contains linked lists and hashes of all previously described data objects. Moreover

GridDB provides methods to find, access insert or modify these data structures efficiently.

5.3.2 Procedures

Besides data structures, several procedures are required to generate the power grid models. The algorithm 5.3 illustrates the complete sequence that is utilized to generate the grid subcircuits, where a set of netlist related data-objects is already available after parsing the original netlist. Because the sequence of processing steps in algorithm 5.3 is straightforward, this description is focused on how these actions were separated into different objects and functions to provide the flexibility for switching between different network types or computational methods. Therefore, several objects named **GRID**, **PWIRES**, **TYPE**, **EQUATION** and **PROCESS** were implemented that contain the required processing steps.

The configuration file is parsed blockwise by the function **CONFIG.ParseGridBlock** that is called before the grid blocks can be generated. At first, the process and equation objects **PROCESS** and **EQUATION** are selected and initialized based on the configuration data. These objects provide the necessary functions to compute the RLCK element values and will be used for all grid blocks. Furthermore, the GridData objects **GDATA** are created for each grid model subcircuit and stored in a list, because the mutual inductance element generation requires this data in subsequent processing steps. As shown in algorithm 5.3, the grid type objects **TYPE** are created individually for each grid block since Perl allows to dynamically change object types during the program execution. Therefore, this feature enables the option to select the network types individually for all grid blocks. Each supported computational method and grid type is represented by individual **TYPE** or **EQUATION** objects with standardized interfaces to provide a straightforward approach for extending the functionality of the software.

Figure 5.4 illustrates a grid block including its lumped elements and identifies Perl objects which are responsible for certain parts of the model. While **PROCESS**, **TYPE** and **EQUATION** provide the methods to compute wire parasitics, the objects described in this paragraph implement all required connectivity and geometry related tasks. Before generating the RLK elements, the object **PWIRES** derives a list of wire segments as defined by the geometry description. It invokes the method **GetWire** that is implemented in **TYPE** to generate simple resistive or RL lumped element networks depending on the **TYPE** object that was previously selected. This function also generates the volume filaments if skin effect approximations are required, whereas all Spice elements and parameters are created by the **EQUATION** object. Moreover, the geometry data of all wire segments is stored in an array of **WIREDATA** objects, thus mutual inductance computations can utilize this data and do not need to consider grid geometries or volume filaments again. Finally the object **GRID** is used to encapsulate the finished lumped element network into Spice subcircuits and connect them to the original circuitry. This fine grained separation of tasks was mainly imple-

```
Input: all netlist related data objects stored in GridDB
utilized objects GRID, PWIRES, TYPE, EQUATION, PROCESS ;
call CONFIG.ParseGridBlock; (first block)
PROCESS ← ProcessObject(CONFIG) (←...create object instance);
EQUATION ← EquationObject(CONFIG, PROCESS);
GRIDLIST = [], WIRELIST = [];
foreach grid block BI of CONFIG do
    GDATA ← GridData(BI);
    append GDATA to GRIDLIST;
    TYPE ← TypeObject(BI);
    WIRES = PWIRES.GetWires(CONFIG); (all wiresegments of block)
    foreach WireData WR defined by WIRES do
        call TYPE.GetWire to create RL elements of WR;
            call EQUATION.GetResistor; (invoked within TYPE.Getwire)
            call EQUATION.GetInductor; (...)
        append WR to WIRELIST[BI];
    end
    if TYPE supports mutual inductance then
        foreach Pair of WireObjects W1,W2 in WIRELIST[BI] do
            if W1 parallel W2 then
                call EQUATION.GetMutualInductance; (internal K elements)
            end
        end
    end
    call GRID.CreateGridSubcircuit;
    call GRID.ReconnectSubcircuits;
    call CONFIG.ParseGridBlock (next block);
end
```

Algorithm 5.3 The required processing steps to generate grid model subcircuits.

mented to provide highly customized grid models by parameters that are described in detail in appendix B, but it also allowed a less error prone and convenient software development.

While internal K elements that link only wire segments within a certain subcircuit are easily added to the affected RL networks, mutual inductance elements between wires of different subcircuits require several additional processing steps. To compute mutual inductance elements relative positions and distances are needed, therefore it necessary to transfer the local coordinates of the grid blocks to global coordinates. It is also necessary to duplicate grid blocks that are utilized more than once and apply rotate and mirror commands, thus leading to a flat geometry description without hierarchies. This flat geometry description is only stored in a data structure and uti-

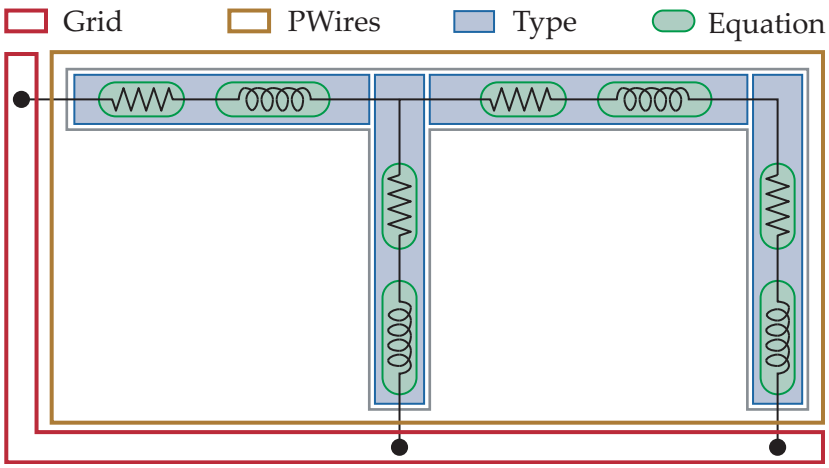

Figure 5.4 Illustration of a power grid network and the corresponding Perl objects that are involved in the model generation.**Grid** controls the connectivity of the circuit block; **PWires** creates the wire segments depending on the power grid geometry; **Type** generates the lumped element networks within each wire segment; **Equation** computes the element values of the Spice network.

lized within the software, whereas the final RLCK models retain the original circuit hierarchies. Therefore it was necessary to split the generation of internal K-elements in algorithm 5.3, and the mutual inductance elements between different blocks into separate procedures. The algorithm 5.5 illustrates the operations to generate an array of **InstData** objects that describe the flat grid hierarchy. It necessary to parse recursively through the complete hierarchy data structure and check if power grid blocks are defined for some subcircuits. **InstData** objects with unique identifiers are created for each grid block and appended to an array. Furthermore, the rotate and mirror commands are evaluated while data structures from previous processing steps like the **GridData** or **Hierarchy** arrays are already available and linked to the **InstData** object. Rotation commands are evaluated during the model generation in contrast to all other parameters, because implementing these operations as Spice functions would lead to very large netlists where swapping all x and y coordinates would have to be supported. Moreover rotation commands require reconnecting mutual inductance elements since different parallel wire segments may come into play. This compromise was selected since rotation commands are not commonly used in parameter alterations and compact netlists are considered as a more important advantage. Moreover, it is necessary to employ the rotation commands of the parent and the current subcircuit to correctly obtain the final block orientations on all hierarchy levels. The previously decried **InstData** array is not only utilized during the generation of mutual inductance elements between different circuit blocks, but also for the graphical output or the Fasthenry export functions, which need a flat geometry description to correctly generate their output files. Furthermore, all wire geometries are based on individual

```
Input: hierarchy object PARENT;
Result: array of ALLBLOCKS
foreach subcircuit XI in PARENT do
    foreach supply name SUP do
        if exists GridData(XI, SUP) then
            BLOCK ← InstData(XI, SUP);
            rot1 = RotationCommand from InstData(PARENT);
            rot2 = RotationCommand from BLOCK;
            call BLOCK.Rotate(rot1,rot2);
            append BLOCK to ALLBLOCKS;
        end
    end
    call CreateInstData(XI, ALLBLOCKS);
end
```

Algorithm 5.5 The algorithm **CreateInstData** generates an array of **InstData** objects that describes all employed power grid blocks.

coordinate systems for every grid sub-block, therefore global values for the coordinate origins are needed to obtain the correct relative positions of wires.

As illustrated in algorithm 5.6 these coordinate definitions exploit the circuit hierarchy where it is only necessary to add the required offset (CX,CY) for the actual grid sub-block to the origin coordinates of its parent subcircuit. Thus, geometry modifications that affect coordinate systems at lower circuit levels are inherently supported by such parameter definitions. All possible pairs of **InstData** objects have to be considered to ensure that all parallel wire segments are coupled by mutual inductance elements. To reach the inductance elements at different circuit hierarchies prefixes separated by single dots are required, while the procedure **GetHierarchyPrefix** is used to derive the prefixes for two InstData objects.

$$\text{"}\overbrace{\texttt{xi\_first}}^{\text{prefix}}.\overbrace{\texttt{xi\_next}}^{\text{prefix}}.\ldots.\overbrace{\texttt{xi\_parent}}^{\text{prefix}}.\overbrace{\texttt{xi\_instance}}^{\text{required instance}}\text{"} \tag{5.3}$$

Even though it would be sufficient to derive hierarchy prefixes that start with the first common parent instance and store the mutual inductance elements on the lowest possible hierarchy level, some Spice implementations only support hierarchy prefixes on the toplevel of the netlist. Therefore, it was necessary to place all K elements on the toplevel that couple inductance elements of different subcircuits. The resulting netlists are slightly larger compared to the optimal approach and may contain more K elements in case of subcircuits that are used more than once, but this has no negative impact on the simulation speed, because both netlists would result in equivalent circuit representations within the simulation software. Furthermore, the previously created **WireData** objects are utilized again to obtain the geometry of wire segments,

```
Input: all previously generated data objects;
Result: mutual inductance elements on toplevel & parameter definitions
foreach Ins Data INS do
    PAR = parent of INS;
    [CX,CY] = PAR.Rotate();
    INS_ORIG_X = 'PAR_ORIG_X + CX';
    INS_ORIG_Y = 'PAR_ORIG_Y + CY;
end
foreach pair of InstData (INS, NIBS) do
    [PREFIX, PREFIX] = GetHierarchyPrefix(INS, NIBS);
    foreach WireData WA in INS do
        foreach WireData B in NIBS do
            if (WA parallel to B) then
                call EQUATION.GetMutualInductance(WA,B,PREFIX;PREFIX);
            end
        end
    end
    call CreateInstData(XI, ALLBLOCKS);
end
```

Algorithm 5.6 this algorithm generates parameters for the local coordinate system origins and the mutual inductance elements between wires of different grid subcircuits.

and finally the equation object provides Spice functions that compute the element values analogous to the other lumped elements computations.

Decoupling capacitor models are connected directly to the local supply nodes that were introduced by the power grid models. Since capacitor models only exhibit a single scaling parameter that does not depend on other parameters of the power grid, no additional processing steps are required besides inserting appropriate capacitor models and scaling parameters to the final netlist. Different capacitor types like MOS gate capacitors or ideal C elements are supported analogous to the previously described **TYPE** objects for different wire models. Besides the function to insert the appropriate Spice elements, each capacitor object has to provide a method to find and replace existing capacitors in the original netlist.

6 Stability Analysis of a Multi Stage Power Amplifier

This chapter presents a typical application of pre-layout power grid models during the analysation of the stability of a fully integrated CMOS RF power amplifier used on an UWB transceiver. After a short presentation of the PA related key design parameters, the root cause of instability namely local feedback loops on the power grid are explained in detail. Furthermore the analysis method and the power grid setups are presented while statistical evaluations of the simulation results are used to propose a power grid topology that enables a stable operation. The power grid induced feedback issue and analysis results utilizing a preliminary version of the model were introduced in [107] and a paper investigating the trends of power amplifier for short-range broad band communication was published in [108] and [109].

6.1 UWB Compliant PA Requirements and CMOS Technology Figures

Due to the trend to very high data rates in wireless communications wide bandwidths are increasingly used in recent years. Following the Shannon theorem (6.1) a high data rate on a digital communication channel can be achieved by using a wide bandwidth B without requiring an increased radiated output power P_o.

$$C = B \cdot ld\left(1 + \frac{P_o}{kT}\right) \tag{6.1}$$

Therefore wide band communication standards are especially attractive for battery powered devices and cost effective single chip implementations including RF power are feasible. The PA analyzed in this chapter is tailored for WiMedia compliant ultra wideband (UWB), a short range high data rate communication standard using a very broad frequency band from 3 to 10 GHz and reaching data rates up to 480 MBits. Orthogonal frequency division multiplexing (OFDM), a multi carrier modulation scheme, is used in the UWB specification [110] that splits the frequency band in N narrow-band channels. Hence the symbol duration can be extended by the factor N making the transceiver more robust against fading while the implementation effort in the analog part of the receiver is relaxed. Although the focus of this chapter is on the PA block, complete CMOS UWB transceiver architectures and critical analog building blocks were published in [112] and [113] giving an overview of the design

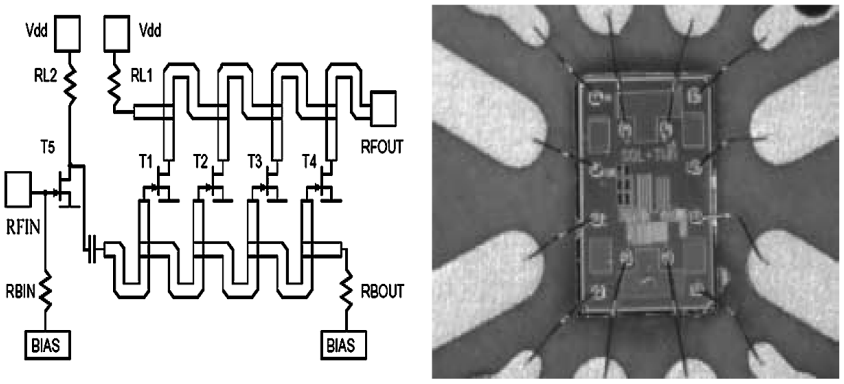

Figure 6.1 Schematic and chip photo of UWB compliant travelling wave guide amplifier published in [111].

challenges that have to be met. Unfortunately an ODFM modulation requires a high peak to average output power ratio since independent sub-carriers with uncorrelated amplitudes and phases are added at the modulator. Therefore highly linear PAs like class A or AB are required in UWB transceivers covering a frequency range from 3 up to 10 GHz. In contrast to constant envelope schemes like GSM or Bluetooth where typically fractional PLLs drive directly the PA, the UWB transmit path utilizes a Gilbert cell as modulator. Due to the negative conversion gain of the modulator a comparatively high amplifier gain of 20 dB up to 30 dB is required to reach an output power of 3 dBm. Furthermore since UWB is targeted as a wireless USB replacement a low cost CMOS or BiCMOS implementation is mandatory. The process dependent cut-off frequency f_T and the maximum oscillation frequency f_{MAX} of a transistor are defined by

$$f_T = \frac{gm}{2\pi \cdot C_{gs}} \qquad f_{MAX} = \frac{f_T}{2 \cdot \sqrt{(R_i + R_g) \cdot (g_{ds} + 2\pi f_T C_{gd})}} \tag{6.2}$$

where R_i and R_g represent the input resistance and gate resistance respectively. Equation 6.2 exhibits a strong dependence on the gate-source C_{gs} and gate-drain capacitances C_{gd} so shrinking transistor dimensions will improve f_{MAX} and f_T as published in [114]. Furthermore is possible to estimate the maximum stable power gain (MSG) at frequency f of CMOS transistors using equation 6.3 because the power gain of a transistor rolls of with -20dB per decade reaching 0 dB at f_{MAX}.

$$MSG \approx \frac{f_{MAX}^2}{f^2} \tag{6.3}$$

The maximum stable gain allows determining the required number of amplifier stages although accurate estimations have to take the quality factor Q of the planar coils into account because R_i of equation 6.2 is affected by the coil resistance. In contrast to narrow band systems at lower frequencies where the inductor quality is limiting the performance of the circuits, UWB implementations have to use inductors with low

quality factors around 3 to obtain the 1.5 GHz bandwidth of one band group. Hence the specs of broad band circuits are mainly defined by the previously mentioned transistor performance figures and these circuits will benefit from reduced transistor sizes in future CMOS deep submicron technologies [115]. Moreover the linearity of the amplifier represented by the third order intermodulation product OIP3 [116] can be estimated by the cut-off frequency f_T as described in [117] and [118]

$$OIP3_{f_t'=0} \approx \sqrt{\frac{8f_T}{f_T''}} \tag{6.4}$$

The maximum OIP3 is reached for an operating point that allows the maximum cut-off frequency, so optimizing linearity is equal to minimizing the number of required stages and therefore the area occupied by the amplifier. It has to be expected that f_T and f_{MAX} of future technology nodes will exhibit less beneficial scaling. Even though this will impair the linearity of RF circuits, but the available gain improvements will allow less amplifier stages or local feedback to linearize the signal. It has to be noted that the performance of the last stage is not only limited by f_T but also by the operating voltage V_{sup} described by the Johnson product [119]

$$V_{sup} \cdot f_T = \frac{E \cdot v_S}{2\pi} \quad (\approx \ 200 \text{ GHzV in Si}). \tag{6.5}$$

Unfortunately the right hand side of equation 6.5, the product of the saturated drift velocity v_S and the breakdown electrical field E, is constant for a particular semiconductor, so integrated CMOS PAs are only feasible for moderate output power but it is sufficient for the UWB standard. Summing up the presented findings it can be pointed out that modern deep submicron CMOS technologies allow the implementation of UWB compliant PAs and future technology scaling will enable reduced area and power consumption.

6.1.1 Amplifier Toplogies

Travelling wave-guide amplifier (TWA) and multi stage type A amplifiers are the most common used circuit topologies for wideband PAs. The power grid impedance plays a crucial role in both topologies whereas TWAs include the supply routing into the design process. TWAs are distributed amplifiers with multiple parallel connected amplifier stages where a pair of transmission lines is respectively connecting inputs and outputs of the active devices as illustrated in figure 6.1. The input signal travels on the input transmission line while the propagation constants are designed that the output signals of the transistors are summed without undesired phase lags and termination resistors avoid reflections. In contrast to cascaded multi stage amplifier the overall gain delivered by a TWA is the sum of the gains of all stages and not the product so high gains cannot be expected. Moreover the transistor sizes have to be small to obtain the required bandwidth resulting in limited transconductances and gains at the individual stages so tradeoffs between gain and bandwidth cannot be avoided. The paper

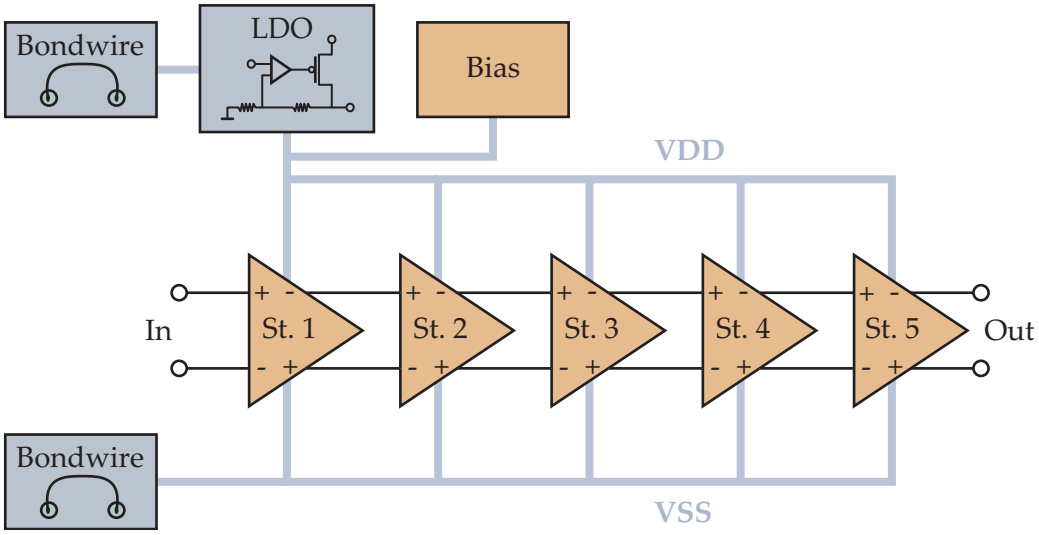

Figure 6.2 Block diagram of 5 stage fully differential PA and its supply concept.

[120] describes a detailed analysis of distributed amplifiers and [111] presents a TWA implementation tailored for UWB reaching a gain of 17 dB and a bandwidth of 8 GHz. Other circuits published in [121], [122] and [123] show that very high bandwidths are possible with CMOS TWAs but gain or 1 dB compression points do not meet the requirements of UWB transceivers. On the other hand PAs with higher output power as published in [124] do not reach the required bandwidth. One stringent disadvantage of TWAs is the area consumption of the transmission lines especially when micro strip structures are used. Moreover these circuits will not exhibits significantly less area consumption due to modern technologies since area dominant micro strip structures cannot be scaled down. Due to the area and gain disadvantages it is very likely that TWAs are replaced by cascaded type A amplifiers in UWB transceivers. Mode locking or injection locking techniques are frequently used in PAs for constant envelope signals. The efficiency of these amplifiers is improved by oscillations invoked by positive feedback in the signal path [125]. Unfortunately highly linear UWB PAs cannot benefit from these techniques. On the contrary the stability of linear amplifiers has to be ensured for all required operating conditions. Therefore a detailed stability analysis including power grid impedances being the dominant source for oscillations turned out to be essential.

6.2 Common Mode Feedback via Power Grid

A fully differential 5 stage integrated CMOS PA with an operating bandwidth of 6-9 GHz is analyzed in this chapter, whereas a low dropout regulator (LDO) is integrated on the chip delivering the supply voltage to the amplifier and isolating low frequency crosstalk noise from other circuit blocks. As illustrated in figure 6.2 all amplifier stages

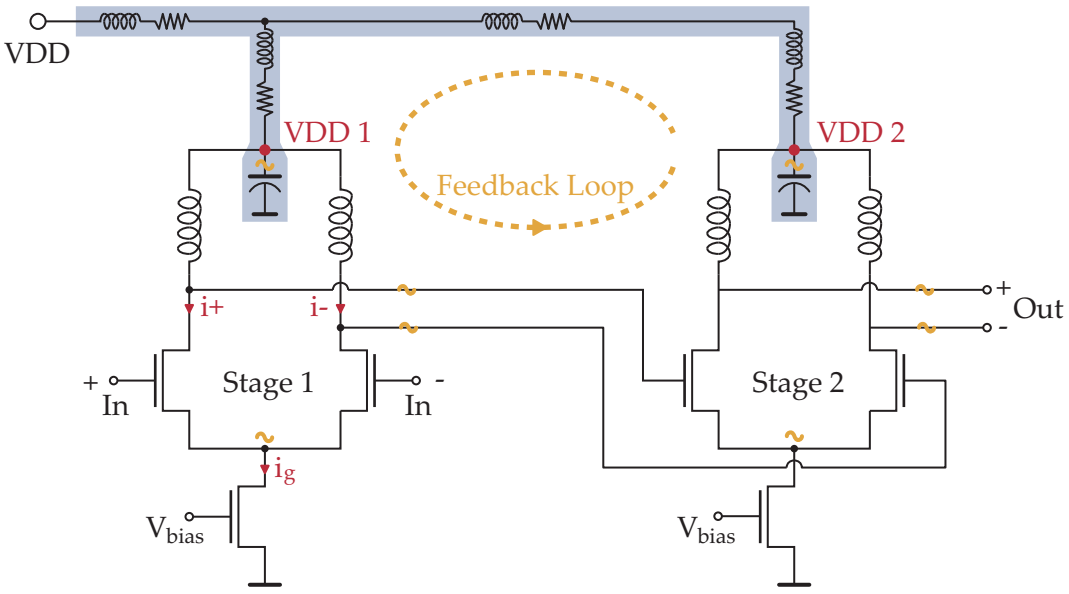

Figure 6.3 2 Stage fully differential PA with feedback loop via power grid including illustration of lumped element power grid model.

and the biasing circuit are connected to the same LDO and bond-wires from VSS and the LDO are also used to isolate the PA voltage domain from the other blocks of the chip. The LDO contains a PMOS pass device and therefore exhibits rather high impedance for signals in the operating frequency range. Furthermore the bond-wires have a self inductance in the nH range so galvanic crosstalk to other blocks is filtered effectively. But on the other hand VDD supply ripple and ground bounce of signals at RF cannot be avoided due to the impedance of bond wires and it has to be considered that the regulating loop of the LDO , typically in the kHz or lower MHz range, is far too slow to regulate RF supply ripple. Besides the doubled signal swing and lower distortion due to the canceled out even harmonics, fully differential circuits have an additional advantage to single ended designs concerning their power consumption. Amplifier stages similar to those drawn in figure 6.3 are analyzed throughout this chapter. Due to the large signal swing especially at the higher stages of the PA, the non-linear current signals i_+ and i_- have to be examined. The well known first order current equation of NMOS transistors in strong inversion is defined as

$$i(V_{GS}) = \frac{k_n}{2} \cdot (V_{GS} - V_t)^2 \tag{6.6}$$

where V_{GS}, V_t and k_n represent the gate source voltage, the threshold voltage, and the current gain factor of the NMOS. Using equation 6.6 together with the input bias voltage V_b and the differential input signal leads to the following signal currents i_+

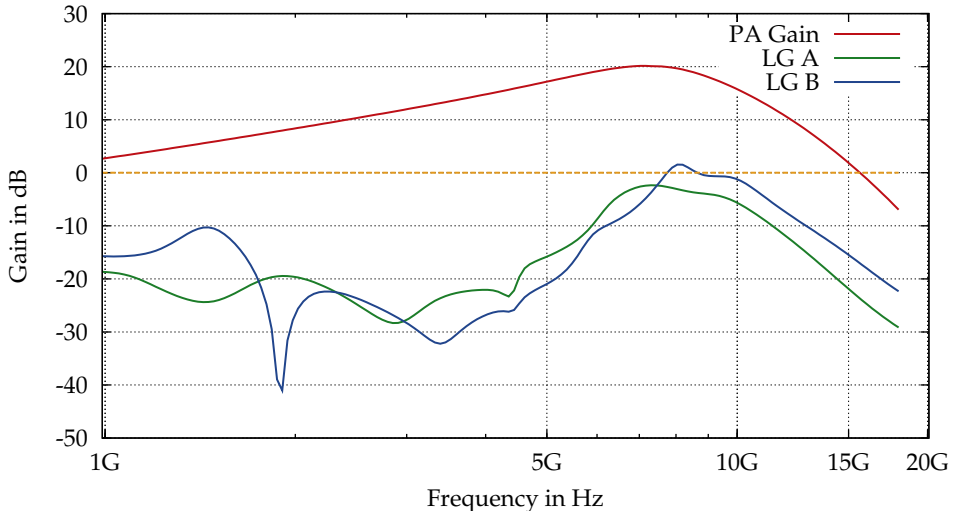

Figure 6.4 Loop gain amplitude of 2 different power grid topologies vs. signal gain of the PA. Topology A → stable PA; Topology B → unstable PA

and i_-

$$\begin{aligned} i_+ &= \frac{k_n}{2} \cdot \left(V_b + V_{sig} - V_t\right)^2 \\ i_- &= \frac{k_n}{2} \cdot \left(V_b - V_{sig} - V_t\right)^2 \end{aligned} \tag{6.7}$$

and to the complete current of the amplifier i_g

$$i_g = i_+ + i_- = \frac{k_n}{2} \cdot \left[\left(V_b + V_{sig} - V_t\right)^2 + \left(V_b - V_{sig} - V_t\right)^2\right]. \tag{6.8}$$

Furthermore a differential harmonic input signal with frequency f_s and maximum amplitude $2 \cdot V_p$

$$V_{sig} = V_p \cdot \cos(2\pi f_s) \tag{6.9}$$

is applied to the inputs and after some arithmetic reformulations i_g is defined as

$$i_g = k_n \cdot \left[\left(V_b - V_t\right)^2 + \frac{1}{2} \cdot V_p^2 \cdot \left(1 + \cos(4\pi f_s)\right)\right]. \tag{6.10}$$

In most cases for amplifier stages with reasonable gain V_p is significantly smaller than $V_b - V_t$ therefore a predominantly DC current consumption may be assumed simplifying the design of a proper power distribution network. If the left and right current paths (i_+,i_-) are connected together symmetrically after the inductive load, the second harmonic of the input signal is the main source of supply ripple. This VDD ripple is considerably smaller than supply ripples in single ended designs while local decoupling capacitor arrays are used to further reduce this voltage ripple. The open loop

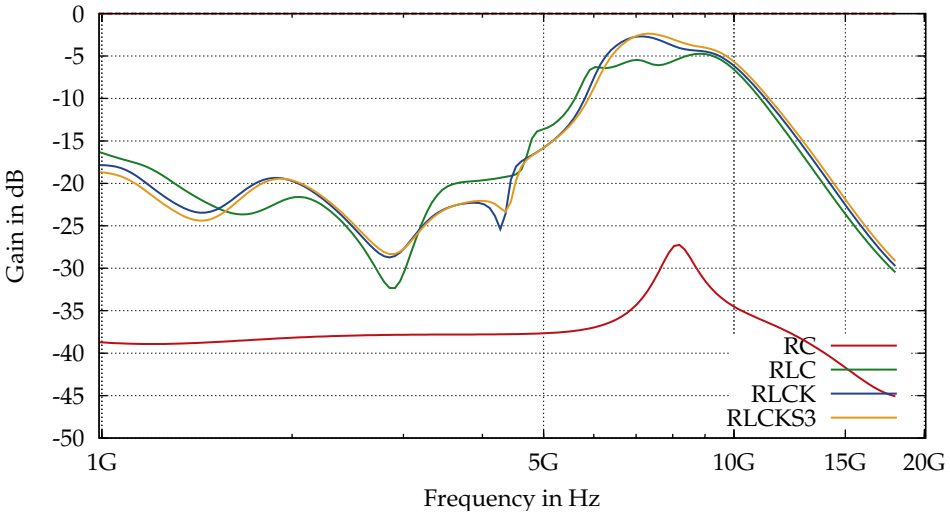

Figure 6.5 Loop gain amplitude for different power grid model types (RC; RLC; RLCK; RLCK using 3 filaments). Topology A.

design is mandatory to obtain the required bandwidth and multi stage PAs should be unconditionally stable if the signal path is designed correctly. Unfortunately for integrated PAs with very high bandwidths this is not always the case. Figure 6.3 uses a two stage amplifier to illustrate the basic case of an unwanted feedback loop on the power grid. Analogous to the 5 stage PA this two stage amplifier exhibits a shared power network and figure 6.3 shows the wire parasitics and the decoupling capacitors on the local supply nodes. Considering these power grid parasitics it is obvious that noise and signal harmonics on the local supply node of stage 2 (VDD2) may easily propagate via the power grid to the VDD node of stage 1. Unfortunately the simple circuit topology of the amplifier that is optimized for high operating frequencies exhibits a poor power supply rejection ratio (PSRR) considering common mode signals. Hence the VDD ripple appears as a common mode signal at the outputs of stage one and it finally appears at VDD 2 after being amplified by stage 2. Unlike differential pairs at low frequencies stage 2 exhibits a significant common mode gain for RF signals, because the NMOS used as current source for the differential pair cannot maintain a DC current mainly due to parasitic capacitances that couple the RF ripple to the transistors gate and drain. The resulting common mode current ripple appears at the amplifier outputs and finally closes a feedback loop at VDD 2. Reconsidering the 5 stage PA of figure 6.2 indicates the complexity of this problem since 10 different VDD and VSS nodes are involved whereas several loops over different stages using VDD and VSS networks are superimposed. Typically the supply nodes at the higher stages can be assumed more critical since more loops passing previous stages are available. Figure 6.4 shows the loop gain amplitude at the VDD node of the last stage for 2 slightly different power grid topologies where simple bus structures as illustrated in figure 6.2 were utilized for VDD and ground networks. The difference

between bus topology A and B is only a shorter wire length to stage 5 in case B while the amplifier blocks remain unchanged. Regarding the differential voltage gain of the amplifier versus the loop gain amplitudes it is obvious that the operating frequency range from 6 to 9 GHz is the most critical range to maintain the stability of the circuit. For low frequency signals the PSRR and the common mode rejection of the amplifier stages show a better performance while at very high frequencies above 16 GHz no gain whether for differential nor common mode signals is available any more. Therefore it is sufficient that the stability analysis performed throughout this chapter covers a frequency range from DC up to 20 GHz. Figure 6.6 shows transient simulations of the PA including the same power grid models used in figure 6.4. At 5 ns a short pulse is added to the inputs of the PA to excite oscillations and at 10 ns an 8 GHz harmonic input signal is switched on. As long as the loop gain amplitude is smaller than 0 dB over the frequency range of interest like in case A the circuit is unconditionally stable and no oscillations occur. But on the other hand in case B common mode oscillations emerge after the spike at 5 ns. Furthermore figure 6.6 illustrates that the differential output signal becomes unusable due to the large amplitude of the common mode oscillation that will reach rail to rail levels. Since supply grid parasitics have dominant impact on the stability of the power amplifier appropriate models have to be used for valid simulations. Figure 6.5 shows different types of power grid model created by the pre-layout power grid tool presented in the previous chapter. Obviously RC-only networks are not sufficient for the required frequency range and yield to far too optimistic results, so inductances have to be included in the model. RLC networks are sufficiently accurate for estimating the loop gain amplitude, but for certain geometries it is preferable to include mutual inductances that ensure a realistic model. Skin effect is not critical for this particular analysis since loop gain simulations using the simple RLCK model and the model with skin effect approximations (RLCKS3) exhibit very similar results.

6.3 Middlebrook Closed-Loop Loop-Gain Analysis

Since gain and phase margin of the involved feedback loops define the stability of the circuit it is required to simulate these loop gains of local power nodes at all amplifier stages. Due to the signal swings especially at the last amplifier stage, large signal nonlinear simulations like transient or harmonic balance transient simulations are mandatory to accurately analyze the operating performance of the amplifier. But nevertheless small signal (AC) analysis is perfectly valid for loop gain simulations at the local supply nodes since these nodes will not exhibit large signal swings if the power distribution network is properly designed. AC simulations have the advantage that a wide frequency range may be covered by a single simulation run, while simulation time is also significantly shorter than in transient simulations. Modern Spice simulators are able to simulate large linear networks like our power grid model so AC loop gain simulations turned out as the most favorable method for optimizing the

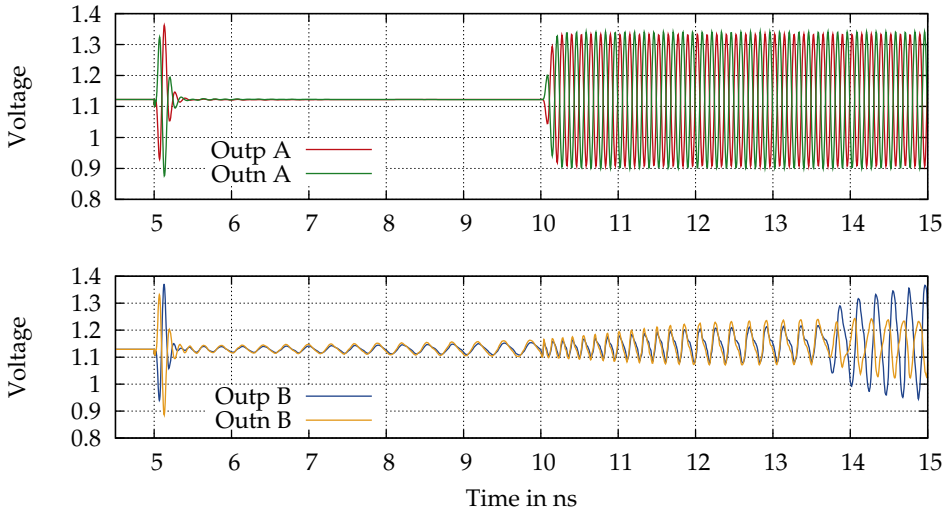

Figure 6.6 Output voltage of a stable PA (A) and one oscillating PA (B); @ 5 ns: spike on PA input; @ 10 ns: 8 GHz harmonic input signal;

supply grid topology for the power amplifier. The following methodologies to calculate the loop gain are presented in more detail in [126] and a similar variant ot the method is published in [127]. Figure 6.7 illustrates a feedback loop at node A using the Norton equivalent of the circuit. Z_1 and Z_2 represent the impedances at both sides of node A and gm models the gain of the feedback loop. So the loop gain T at node A is defined as

$$T = gm \cdot (Z_1 \| Z_2). \tag{6.11}$$

The impedances and the transimpedance of formula (6.11) are not available for the simulator so the loop gain T cannot be calculated directly. One possibility to evaluate T is shown in figure 6.8 where the loop is opened at node A. Furthermore a test signal V_{test} is added to the forward looking part of this node, while the resulting voltage at the backward looking part v_y is used to calculate the open loop gain T_{ov} that is equal to the true loop gain T. Moreover an alternative solution is available where a current test source is inserted, hence the open loop gains T_{ov} and T_{oi} are calculated by

$$T_{ov} = \frac{v_y}{v_x} \quad \text{or} \quad T_{oi} = \frac{i_y}{i_x}. \tag{6.12}$$

Unfortunately opening the loop has the disadvantage that additional care has to be taken to set the correct DC operating voltage at the test node. In the context of loop gain simulations on power grids the test nodes are the local power nodes introduced by the power grid model. Since the voltage level at these nodes depends on the power grid parasitics and on the current consumption of the corresponding circuit block, a simple precalculated DC operating voltage would lead to inaccuracies. The test signal is inserted in the closed loop to overcome this issue as illustrated in figure 6.9. In

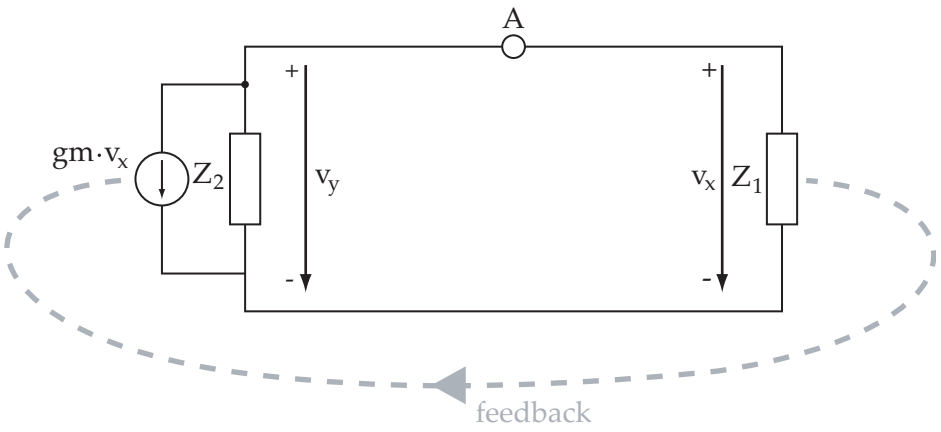

Figure 6.7 Norton equivalent of a feedback loop

these cases the original circuit topology and the resulting voltage levels are retained. Analyzing the circuit in figure 6.9 using the voltage injection leads to the following loop gain

$$T_v = \frac{v_y}{v_x} = Z_2 \cdot \left(gm + \frac{1}{Z_1}\right) \tag{6.13}$$

It is obvious that in contrast to the open loop case T_v is not equal to the true loop gain T. Eliminating the transconductance gm in equation 6.13 by using equation 6.11 allows to express T_v in terms of the true loop gain.

$$T_v = \left(1 + \frac{Z_2}{Z_1}\right) \cdot T + \frac{Z_2}{Z_1} \tag{6.14}$$

Thus voltage injection leads to accurate results only at circuit nodes where $Z_1 \gg Z_2$. The current injection is analyzed in an analogous way where

$$T_i = \frac{i_y}{i_x} = Z_1 \cdot \left(gm + \frac{1}{Z_2}\right) \tag{6.15}$$

T_i is again not equal to the true loop gain but it can be set in relation to T.

$$T_i = \left(1 + \frac{Z_1}{Z_2}\right) \cdot T + \frac{Z_1}{Z_2} \tag{6.16}$$

So current injection allows to measure accurate loop gains where $Z_2 \gg Z_1$. Depending on the impedance at the test node, the appropriate test signal has to be chosen. Referring to the previous findings voltage injection should be used only at nodes that behave similar to ideal voltage sources while current injection is valid at nodes that behave like ideal current sources. To enable the simulator to analyze nodes of arbitrary impedances both injection method are employed consecutively. Furthermore the following relation

$$\frac{1}{1+T} = \frac{1}{1+T_v} + \frac{1}{1+T_i} \tag{6.17}$$

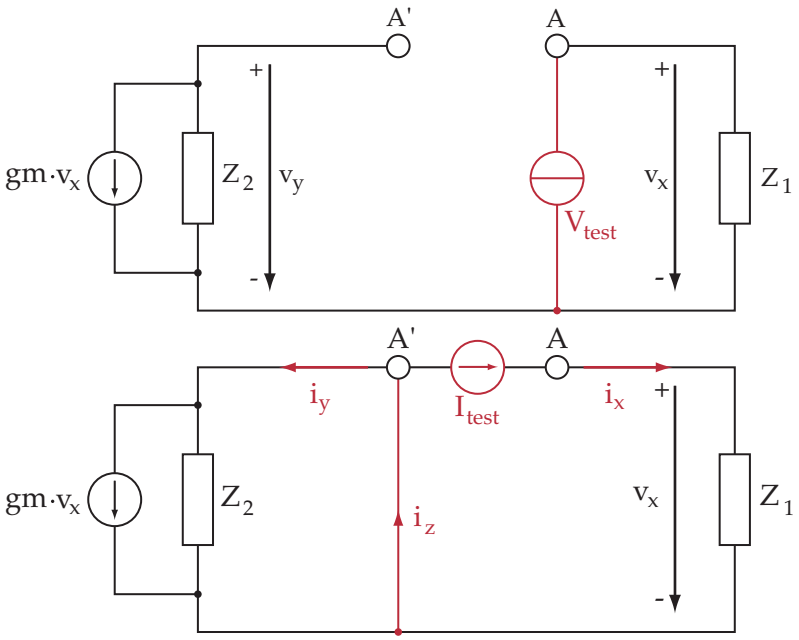

Figure 6.8 Test voltage and test current applied to opened loop at node A

allows an accurate calculation of the true loop gain

$$T = \frac{T_v \cdot T_i - 1}{2 + T_v + T_i}. \tag{6.18}$$

Concluding the presented method enables us to simulate conveniently the small signal gain and phase of feedback loops at arbitrary circuit nodes.

6.4 Heuristic Analysis of Power Grid Topologies

The main purpose of the analysis was finding a power grid topology where no possible feedback loop may invoke oscillations. Fully parameterized pre-layout power grid models that were previously introduced in this thesis were utilized to model the electrical behavior of the power grid. The dominant parameters of the unwanted feedback loops are parasitic effects of metal interconnects and transistors at RF whereas several of these effects are not strictly monitored in CMOS production. Therefore it is not advisable to optimize for narrow phase margins or loop gains just close to 0 dB. Moreover during the design phase when detailed layout data is not yet available significant safety margins for loop gain amplitudes have to be employed to account for the inherent uncertainties of a pre-layout analysis. Hence all statistical findings throughout this chapter are based on loop gain amplitudes while phase margins could be ignored. This statistical data was used to tailor a power grid topology for very low loop gains and reasonable area consumption.

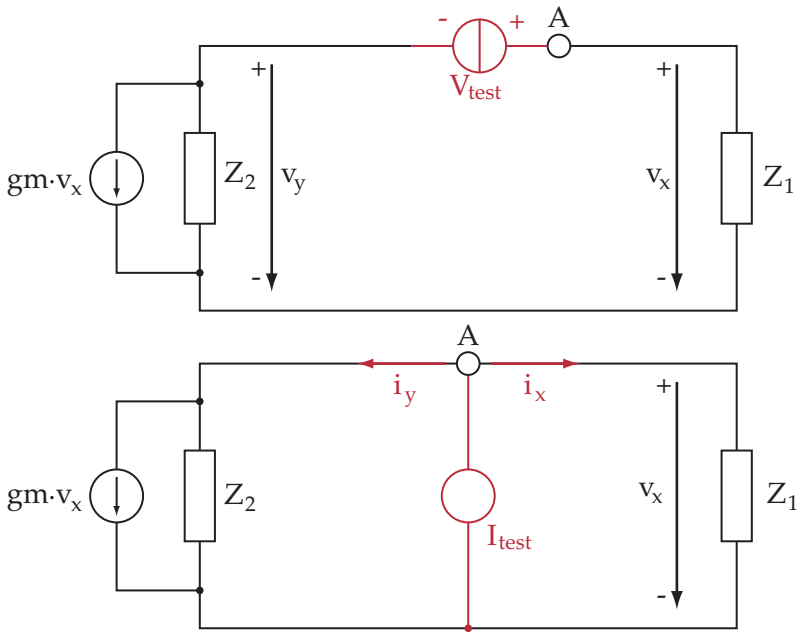

Figure 6.9 Test voltage and test current inserted in closed loop at node A

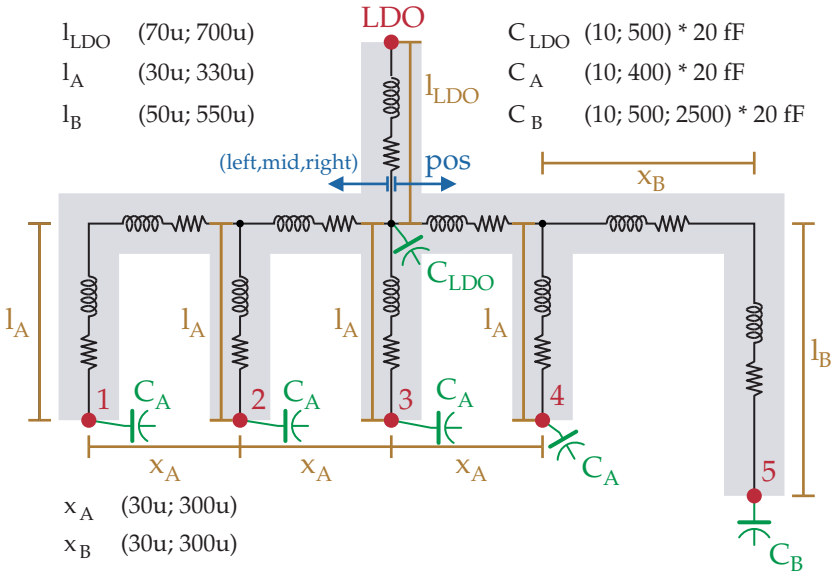

Figure 6.10 Illustration of basic power grid model geometry including the parameters used in the heuristic analysis.

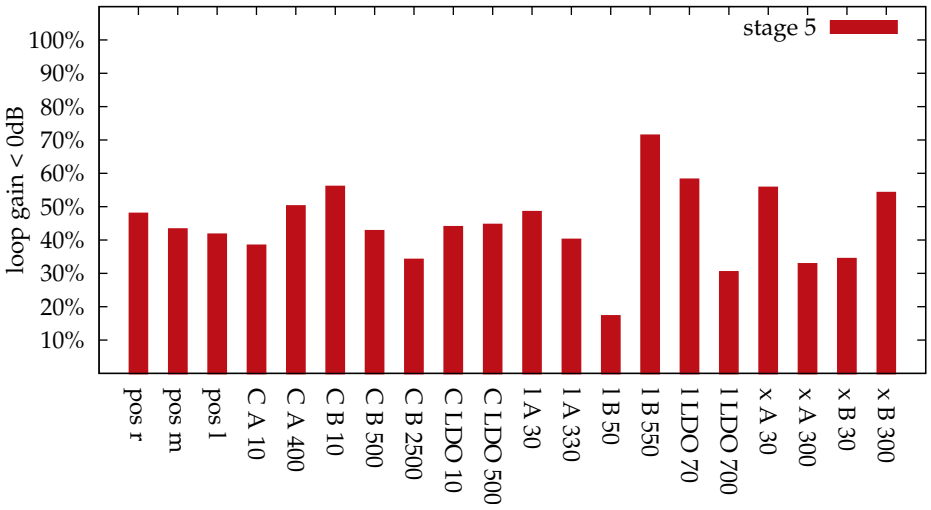

Figure 6.11 Histogram of loop gain analysis using the basic RLC power grid model. The VDD node of stage 5 was analyzed.

6.4.1 Basic Simulations using an RLC Model

Designers have very large degrees of freedom in choosing between different topologies, wire dimensions and blocking capacitor sizes for each amplifier stage and both VDD and VSS networks. So considering all these design parameters it was not possible to define a straightforward process or strategy for identifying a valid power grid geometry. To identify critical topologies or wire dimensions a large set of different power grid configurations was simulated and statistically analyzed. A fully parameterized power grid model illustrated in figure 6.10 allowed the convenient creation of all different power grid configurations by automatically sweeping the user defined parameters. Additionally all parameters that were altered during the simulation run are shown in figure 6.10 including all used values. For this first batch of loop gain simulations an RLC power grid model was selected where only wire distances but no exact x/y positions are required and a simple bus structure was preferred since it represents the most straightforward topology. To gain first insight to the problem only the loop gain of stage 5 was simulated, since the last stage was expected to be the most critical one. Therefore the wires to the stages 1 to 4 can use a shared length parameter l_A and also the distance on the shared power bus is represented by the common parameter x_A (Figure 6.10). These simplifications are necessary as every additional parameter value increases the number of simulations significantly since all permutations of parameter values are simulated. Even though only two or three values per parameter were used, a total number of 1152 simulations were computed. The other parameters are l_{LDO} representing the wire length of the voltage regulator connection, l_B and x_B denoting the wire lengths to the last stage and pos that defines the LDO connection at the left, right or in the center of the bus wire. Additionally C_A, C_B and C_{LDO} define the size

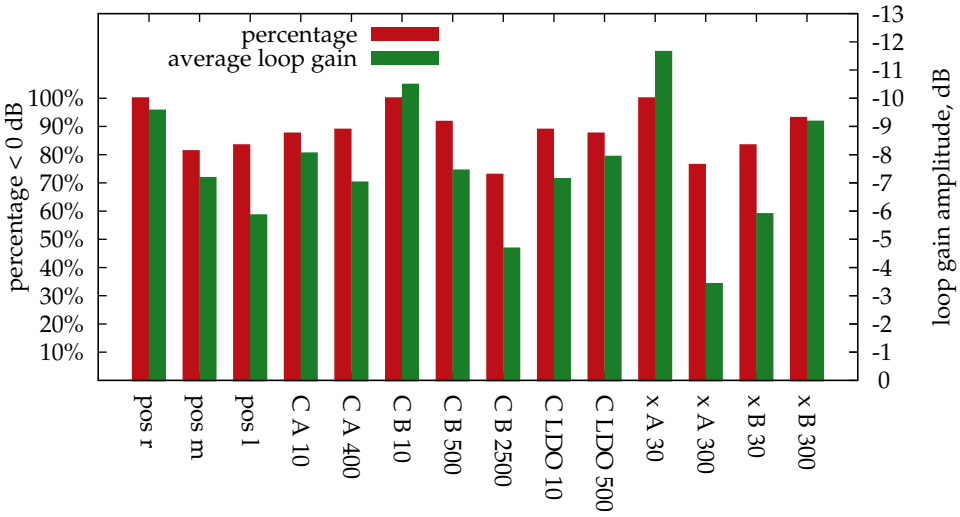

Figure 6.12 Reduced histogram of power grid loop gain analysis using the basic RLC model. Fixed parameters $l_{LDO} = 70\mu m$,$l_A = 330\mu m$, $l_B = 550\mu m$

of the blocking capacitor arrays located at the local supply nodes. Previous simulations revealed that the VSS networks show similar behavior, hence exactly the same power grid model sharing the parameters from the VDD model was utilized. The wires widths have to be defined considering electromigration since very high supply currents occur especially in the last amplifier stage. To avoid excessive wire widths up to thee metal layers were used in parallel. From each simulation run the maximum value of the AC loop gain in the frequency range (up to 20 GHz) was extracted and utilized in the following histograms. Referring to the previously presented observations, simulation results that exhibit maximum loop gains below 0 dB are counted as stable power grid configurations whereas positive loop gains may yield to oscillations. Figure 6.11 shows a histogram where each bin represents a subset of the results with one particular fixed parameter value. The probability plotted in figure 6.11 represents the number of stable power grid configurations of one subset versus the complete number of grid configurations covered by a certain histogram bin. The wire length to the last stage l_B is easily identified as the most critical parameter because the percentage of stable configurations is reduced significantly when l_B is changed from $550\mu m$ to $50\mu m$. Other dominant parameters are l_{LDO}, x_A and x_B showing analogous behavior. In contrast to a majority of power integrity related topics low impedances on power distribution networks are not necessarily beneficial for this application so a more thorough investigation is required. Basically this first simulation run indicates that wires conducting the supply current of several stages should be short while wires that connect only one stage should be long. The high impedance of the longer wires filtering the cross talk distributed to other stages is essential to obtain a stable PA. Because the mentioned dominant parameters might mask the impact of the remaining parameters a second histogram was created using only the results where $l_B = 550\mu m$,

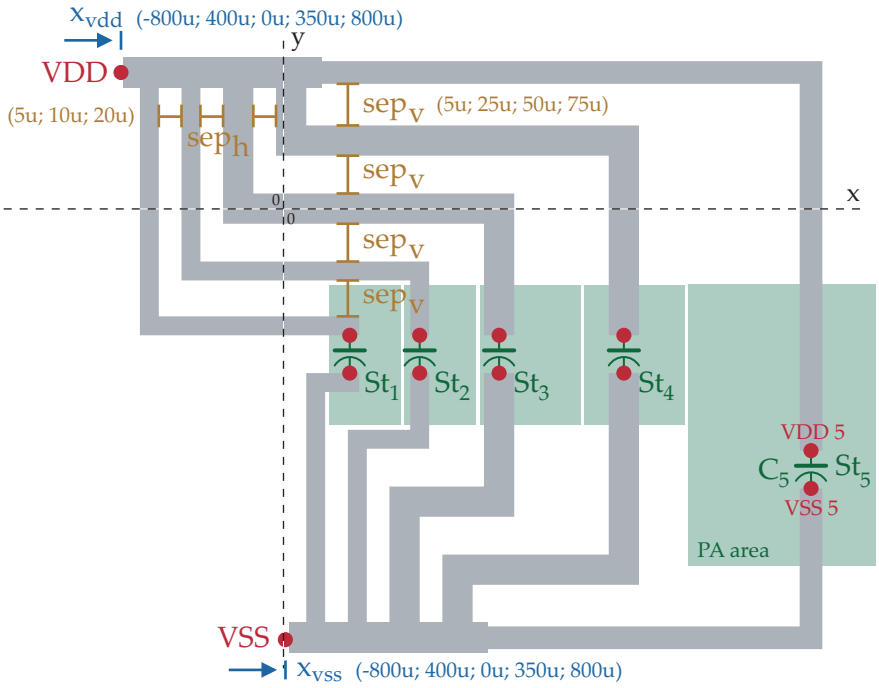

Figure 6.13 Illustration of the detailed RLCK power grid model geometry showing the VDD and the VSS grid. Parameters used for the sweeps are included, the fixed parameters are presented in Appendix C.

$l_{LDO} = 70\mu m$ and $l_A = 330\mu m$. Figure 6.12 shows this histogram and additionally plots the average loop gain of each bin. Several parameters do not exhibit significant changes in the probability plot because the loop gain drifts do not traverse the 0 dB value. In these cases the average loop gain allows to identify those parameter values that improve the safety margin of already stable power grid configurations. The results of the parameters x_A and x_B confirm the previously drawn assumption that amplifier stages should not share supply wires, therefore a star topology should be used for both VDD and VSS networks. It is also obvious that blocking capacitor arrays directly at the amplifier stages do not improve the stability in contrast to additional capacitors at the LDO. The unexpected reduced stability for large capacitor arrays at stage 5 was caused by a LC resonance peak. Therefore additional care has to be taken to ensure that the unavoidable LC resonance frequencies do not occur in the critical frequency range. The location where the LDO is connected to the bus has only minor influence on the loop gain and this parameter is not relevant for star topologies. Furthermore similar simulations were made for VSS nodes that yield to the same conclusions.

6.4.2 Detailed RLCK Model and Simulation Results

Figure 6.13 illustrates the power grid model that was utilized for a second set of loop gain simulations. This power grid model requires fully defined x/y coordinates be-

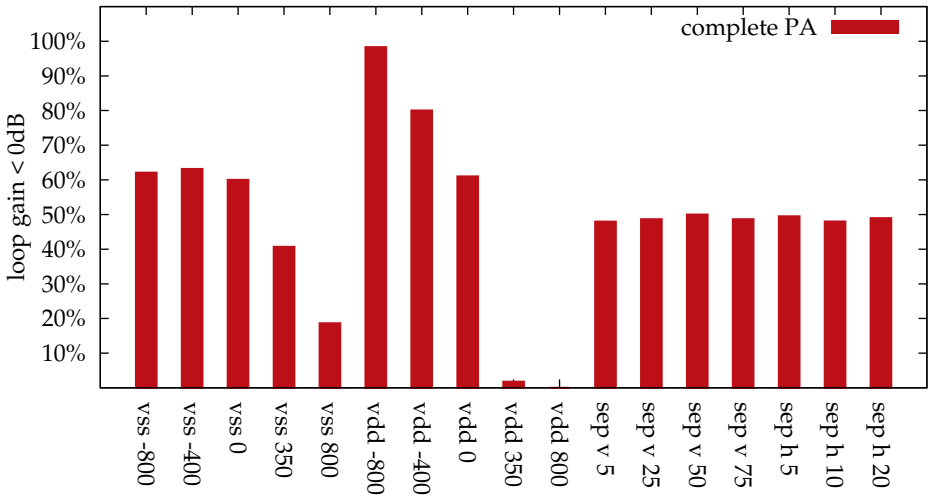

Figure 6.14 Histogram of the loop gain analysis using the delailed RLCK model. The results consider the loop gains of all amplifer stages.

cause RLCK interconnect parasitics are calculated that require the positions, distances and orientations of all wire segments. Due to the results of the previous simulation runs a star topology for VDD and VSS networks was chosen and the size of the blocking capacitor arrays was preassigned. Furthermore the arrangement of the amplifier stages was defined including the x/y coordinates for all local VDD and VSS nodes. The sweeping parameters X_{vdd} and X_{vss} define x coordinates of the star connection node while the y coordinates are assumed to be just outside the expected layout area of the PA. And finally sep_h and sep_v define the horizontal and vertical spacing between the parallel wires. Obviously this model is a decent case to illustrate the usefulness of arithmetic expressions and variables instead of numerical values. Because all wires of the power grid model automatically adjust their positions and lengths during the parameter sweeps, no tedious and error-prone manual rearrangements of wire segments are required This second simulation run contains loop gain simulations of all five amplifier stages and figure 6.14 shows the resulting histogram for all swept parameter values. In this histogram a power grid configuration is considered stable when the local VDD nodes of all five stages exhibit loop gains below 0 dB in contrast to previous plots where only stage 5 was analyzed. The critical parameters of this simulation run are unsurprisingly the x-coordinates of star connection nodes that have direct influence on the wire lengths to the stages while on the other hand wire spacing is not critical. To identify better the critical stages figure 6.15 shows the average loop gain amplitude of all stages. The histogram bins of the x-coordinates were rearranged, so ”par” represents a parallel x-coordinate sweep of both VDD and VSS nodes, while ”dia” represents a diagonal sweep with VDD starting at the leftmost (-800µm) and VSS at the rightmost position. All stages show the expected behavior that short wires on either VDD or VSS networks cause an increased loop gain although

the first two stages are not critical. The inherently longer wire to stage 5 accounts for a lower loop gain therefore mainly the stages 3 and 4 invoke oscillations. X_{vdd} and X_{vss} values of -400 µm and -800 µm yield to low loop gain values for all stages so $X_{vdd} = X_{vss} = -400\mu m$ was chosen for our layout proposal resulting in a significantly smaller area consumption compared to -800 µm without sacrificing the stability of the amplifier. Finally figure 6.16 plots the wire separation related histogram bins for the selected X_{v**} value indicating a very minor rise of loop gain when vertical spacing between parallel wires is only 5 µm. The analysis of local VSS nodes yield to the same conclusions therefore no additional simulation results need to be presented.

6.5 Conclusion

To ensure a stable circuit operation it turned out that an independent power routing for each stage is mandatory including single common nodes directly at the LDO and at the VSS bonding pad respectively. Due to the fully differential circuit topology the amplifier performance is not affected by the power grid as long as the required DC supply voltage levels are retained. Simulations showed that the additional supply voltage ripple due to larger wire impedances has neither negative influence on the output power, the bandwidth or the linearity of the PA. Because on-chip wire inductances are only geometry but not temperature dependent temperature and process sweeps were omitted during the stability analysis to avoid an excessive number of simulation runs. Final corner simulations using the proposed power grid topology showed no critical influence on stability caused by process and temperature variations.

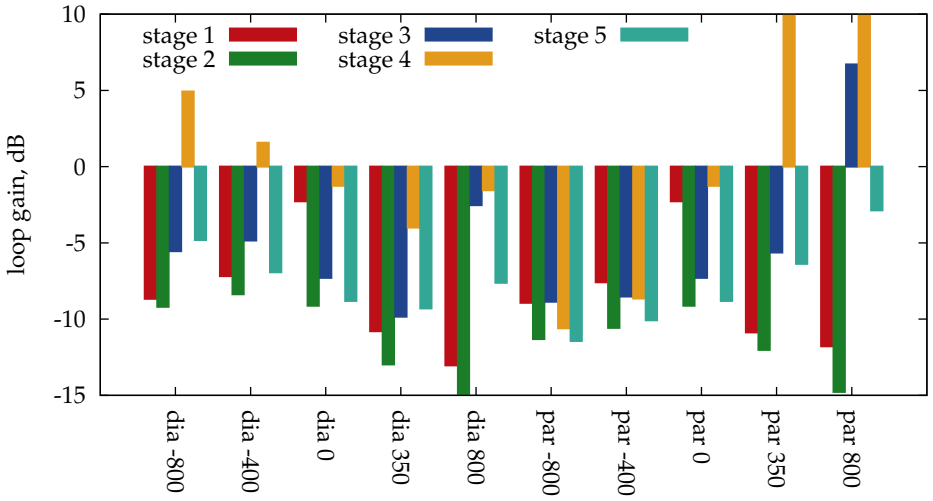

Figure 6.15 Histogram of loop gain analysis of individual PA stages. The histograms show sweeps of x_{vdd} and x_{vss} parameters. "par" bins represent parallel sweeps of the star connection nodes ($x_{vdd} = x_{vss}$) and "dia" bins represent diagonal positions ([x_{vdd}, x_{vss}], [-800;800], [-400;350], [0;0], [350;-400], [800;-800]) of star connection nodes where x_{vvd} positions define bin names.

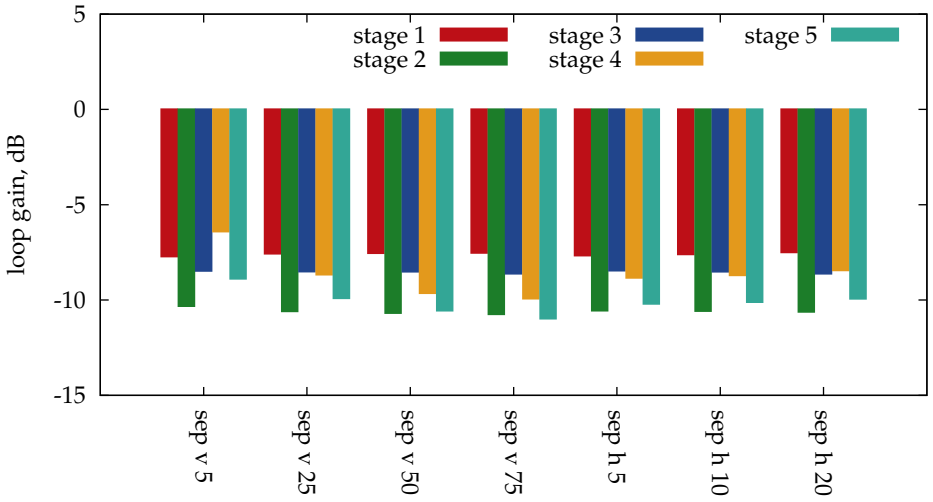

Figure 6.16 Histogram of loop gain analysis focusing on wire spacing parameters sep_v and sep_h. The positions of VDD and VSS star connection nodes are fixed to $x_{vdd} = x_{vss} = -400\mu m$.

7 Conclusion

7.1 Summary

The main goal of this work was the development of a power integrity simulation flow for analog and mixed signal integrated circuits. A pre-layout flow was selected enabling circuit designers to consider power integrity issues early in the design phase to minimize the risk of expensive redesigns of already finished layouts. Moreover, this approach proved to be useful during the concept phase, where different supply concepts may be evaluated conveniently, while the employed grid models are significantly more accurate than simple hand calculated estimations. In contrast to digital power integrity simulations, which mainly evaluate static or dynamic voltage drops by utilizing optimized special purpose simulation tools, the presented power integrity flow is based on Spice, since only full featured analog simulators provide the required analysis methods to identify power integrity phenomena in analog circuits. Therefore, this work could focus on the development of Spice compatible pre-layout power grid models and software tools that generate and incorporate these models into the standard analog simulation environment. RF applications are commonly affected by power integrity issues due to high signal frequencies, thus grid models have to consider inductive effects to provide reasonable results. Lumped elements RLCK networks were selected since both time and frequency domain analysis methods of Spice are handling such networks efficiently. The geometry parameters of the grid models may consist of arithmetic expressions and user defined variables to enable convenient customization and scaling options. If the connectivity is not changed by parameter alterations, re-netlisting the grid model is not required, since all RLCK element values are represented by a set of equations which are evaluated during the Spice simulation. From an application point of view, accuracy requirements of pre-layout models are not very critical, but it turned out that errors due to approximated mutual inductance values frequently lead to unstable interconnect models. Therefore, it was necessary to find accurate but compact self and mutual inductance formulas for rectangular orthogonal wire geometries. The presented self inductance equations, which are based on arithmetic and geometric mean distance approximations, are also utilized for mutual inductance computations. Even though these equations are compact enough to be implemented as Spice expressions, the achieved accuracy is comparable to numerical methods. Furthermore, an optimized volume filament approach that requires only three or five filaments may be used to approximate the skin effect, enabling the power grid model to cover broad band applications. Finally, the stability analysis of a 5 stage

CMOS RF power amplifier represents a typical application of the pre-layout power integrity simulation flow. Local feedback loops between the amplifier stages which are closed by the power and ground networks may lead to common mode oscillations. Hence, the loop gain at the supply nodes of each stage was analyzed and power grid geometry optimizations were executed to ascertain that a star topology where longer wires are used allows a stable operation. These grid optimizations required a large number of parameter sweeps and geometry modifications, which were only possible by exploiting a fully parametrized model.

7.2 Future Work

Power integrity simulation methods will remain an important research topic, since future shrinked CMOS technologies will be increasingly affected by power integrity phenomena. Besides a rising current consumption and higher signal frequencies in high performance circuits, lower supply voltages will lead to reduced supply rejection ratios of analog circuits, and interconnects in the nanometer range exhibit elevated resistance values.

Pre-layout metal interconnect models could be extended by wire capacitance models to improve the accuracy in applications where no dominant decoupling capacitor arrays are used, and size dependent specific resistance models [23] will be important for wire widths below 100 nm. Most contemporary chips utilize several separate power domains to allow different supply voltages on one chip and to reduce the crosstalk between circuit blocks, but substrate noise that propagates in the bulk silicon cannot be avoided. Substrate shielding is accomplished by ground contacts, therefore the shielding behavior strongly depends on the involved ground networks and pre-layout substrate resistance models combined with grid models would significantly extend the range of applications enabled by the power integrity flow. Additional research to find compact substrate resistance models is required, since current calculation methods are computational expensive and not feasible for pre-layout models. Furthermore, the influence of the chip package and board interconnects should be incorporated in power integrity simulations, where especially systems using multi chip packages would benefit from such approaches. The geometry and dimensions of package interconnects require different modeling methods using for example transmission line or transmission matrix approaches that should to be combined with the presented on-chip models.

A Electrostatic and Magnetostatic Equations

This summary is included in the thesis since some of the rules and equations are used in chapter 3 to develop the necessary formulas for calculating lumped element RLCK models that are employed in the power grid models.

On-chip power grid dimensions for analog blocks are in a mostly less than 1 mm range and signal frequencies up to 20 GHz cover most contemporary RF applications. Hence time independent electrical forces were assumed and electrostatic and magnetostatic relations are sufficient to calculate the electrical behavior of on-chip interconnects. All equations and concepts presented in this appendix are covered in detail in [92] or other publications treating basic electromagnetics.

A.1 Electrostatic Equations

The Helmholtz theorem states that a vector field $\mathbf{X}(\mathbf{r})$ in an unbounded region V may be described completely only by the two equations

$$\begin{aligned} \nabla \cdot \mathbf{X} &= a(\mathbf{r}) \\ \nabla \times \mathbf{X} &= b(\mathbf{r}). \end{aligned} \tag{A.1}$$

Considering this theorem two equations for the electrical field intensity $\mathbf{E}$ are presented in this chapter together with additional relations used for electrical field and capacitance calculations. Moreover, an analogous set of equations are presented in the following section that allow magnetic field and inductance calculations.

Coulombs law describes the force between two charges q_1 and q_2 at a distance R.

$$\mathbf{F}_{12} = \frac{1}{4\pi\epsilon_0}\frac{q_1 q_2}{R^2}\,\hat{\mathbf{R}}_{12} \tag{A.2}$$

Instead of working with the actual force between charges, the force on q_2 per unit charge is commonly used ($\mathbf{E} = \frac{\mathbf{F}_{12}}{q_2}$), which is named electric field density. Furthermore, the source charge q_1 can be replaced by a continuous charge distribution $\rho(\mathbf{r}_1)$ in a volume V, then the electric field density at a certain point $\mathbf{r}_2$ may be defined as

$$\mathbf{E}(\mathbf{r}_2) = \frac{1}{4\pi\epsilon_0}\frac{q_1}{R^2}\,\hat{\mathbf{R}}_{12} = \frac{1}{4\pi\epsilon_0}\iiint_{V_1}\frac{\rho(\mathbf{r}_1)}{R^2}\,\hat{\mathbf{R}}_{12}\,dv_1. \tag{A.3}$$

An alternative method to calculate the electrical field intensity without knowing the exact charge distribution in the volume of interest is provided by Gauss law

$$\iint_S \mathbf{E} \cdot \mathrm{d}\mathbf{s} = \frac{1}{\epsilon_0} Q, \tag{A.4}$$

where Q represents the complete charge that is enclosed by a surface **S**. Furthermore the divergence theorem of Gauss allows to reformulate equation A.4 to

$$\nabla \cdot \mathbf{E} = \frac{\rho}{\epsilon_0}. \tag{A.5}$$

Additionally to equation A.5 a relation for $\nabla \times \mathbf{E}$ is required which is derived in the following lines. The unit vector in A.3 may be replaced by

$$\nabla\left(\frac{1}{R}\right) = -\frac{1}{R^2}\,\hat{\mathbf{R}}_{12},$$

leading to

$$\mathbf{E}(\mathbf{r}_2) = -\frac{1}{4\pi\epsilon_0}\iiint_{V_1} \rho(\mathbf{r}_1)\nabla\left(\frac{1}{R}\right)\mathrm{d}v_1 = \nabla\left[-\frac{1}{4\pi\epsilon_0}\iiint_{V_1} \rho(\mathbf{r}_1)\left(\frac{1}{R}\right)\mathrm{d}v_1\right]. \tag{A.6}$$

It is possible to move the nabla operator in front of the integral since it depends on $\mathbf{r}_2$ while the independent variables of the integral are x_1, y_1 and z_1. Applying the curl to equation A.6 results in

$$\nabla \times \mathbf{E} = 0, \tag{A.7}$$

because the curl of the gradient of every function is zero. Considering equation A.6 the scalar potential ϕ may be defined as

$$\mathbf{E} = -\nabla\phi, \tag{A.8}$$

where ϕ is computed by

$$\phi(\mathbf{r}_2) = -\frac{1}{4\pi\epsilon_0}\iiint_{V_1} \rho(\mathbf{r}_1)\left(\frac{1}{R}\right)\mathrm{d}v_1. \tag{A.9}$$

A system of two conductors without current flow but charged to $+q$ and $-q$ is used to describe the capacitance. If additional charges $+\Delta q$ are added to the positive conductor and the same amount is subtracted from the negative conductor no additional electrical field **E** is created, but the flux of **E** between the two conductors is increased. Due to to the constant distribution of the electrical field it possible to define a constant factor C, the capacitance, that describes the relation between the charge on the conductors and the potential difference

$$q = C\Delta\phi. \tag{A.10}$$

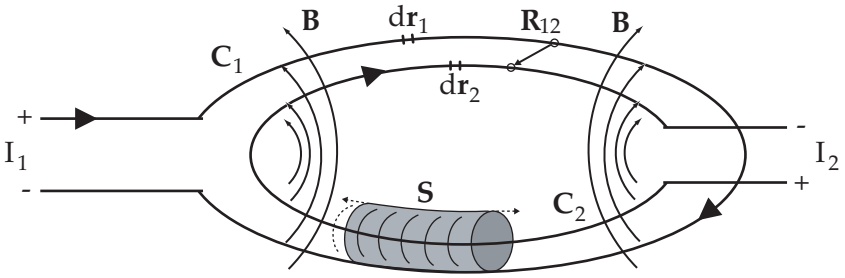

Figure A.1 Illustration of two linked current loops and the magnetic field

The basic case of a parallel plate capacitor leads to the following capacitance equation

$$C = \epsilon \frac{A}{d}, \tag{A.11}$$

where A represents the area of each capacitor plate and d is the distance of the plates. Equation A.11 results in accurate capacitance approximations, if the plate dimenstions are significantly larger than the distance between the plates.

A.2 Magnetostatic Equations

The concept of the magnetic field together with Ampere's law and the vector potential is derived from the force $\mathbf{F}_{12}$ between two filament currents I_1 and I_2

$$\mathbf{F}_{12} = -\frac{\mu_0 I_1 I_2}{4\pi} \oint_{C_1} \oint_{C_2} \frac{(d\mathbf{r}_1 \cdot d\mathbf{r}_2)}{R^2} \hat{\mathbf{R}}_{12}. \tag{A.12}$$

Some mathematical operations allow an alternative formulation of equation A.12 leading to the following force definition

$$\mathbf{F}_{12} = \oint_{C_2} I_2 d\mathbf{r}_2 \times \mathbf{B} \tag{A.13}$$

where the magnetic field or magnetic flux density is defined by the law of Biot-Savart

$$\mathbf{B}(\mathbf{r}_2) = \frac{\mu_0}{4\pi} \oint_{C_1} \frac{I_1 d\mathbf{r}_1 \times \hat{\mathbf{R}}_{12}}{R^2}. \tag{A.14}$$

In this case the path C_1 is considered as the current source creating the magnetic field $\mathbf{B}$ that acts on the current path C_2. Furthermore Amperes law is found by integrating equation A.14 over C_1 resulting in

$$\oint_{C_2} \mathbf{B} \cdot d\mathbf{r}_2 = \mu_0 I. \tag{A.15}$$

I is the current passing through the surface bounded by the curve C_2. If curves C_1 and C_2 do not intersect then $I = 0$ otherwise $I = w \cdot I_1$ where w indicates the number

of turns of curve C_2 intersecting C_1. Furthermore the current I can be expressed by an integral of the current density $\mathbf{J}$ over an open area $\mathbf{S}$ bounded by C_1.

$$I = \iint_S \mathbf{J} \cdot d\mathbf{S}. \tag{A.16}$$

Stokes law is used to reformulate the integral of $\mathbf{B}$ in equation A.15

$$\oint_{C_2} \mathbf{B} \cdot d\mathbf{r}_2 = \iint_S (\nabla \times \mathbf{B}) \cdot d\mathbf{S} = \mu_0 \iint_S \mathbf{J} \cdot d\mathbf{S}, \tag{A.17}$$

which leads to the following notation of Amperes law

$$\nabla \times \mathbf{B} = \mu_0 \mathbf{J}. \tag{A.18}$$

Considering the Helmholtz theorem and equation A.18, an expression for $\nabla \cdot \mathbf{B}$ is sufficient to completely describe the magnetic field strength $\mathbf{B}$. Calculating the divergence of $\mathbf{B}$ utilizing equation A.14 results in

$$\nabla \cdot \mathbf{B} = 0, \tag{A.19}$$

indicating that no point sources or sinks of magnetic flux have been discovered until now, in contrast to electrostatic fields that are invoked by electrical charges. Analogous to the electrical potential equation, a magnetic vector potential is defined, where A.19 yields to the following definition

$$\mathbf{B} = \nabla \times \mathbf{A}, \tag{A.20}$$

since $\nabla \cdot \nabla \times \mathbf{A} = 0$ for all $\mathbf{A}$. The vector potential offers a convenient approach to calculate the magnetic flux, which is required for inductance calculations. Therefore a direct expression for $\mathbf{A}$ depending only on the current and the geometry is derived and presented here in more detail than the other relations. The law of Biot-Savart using a volume integral

$$\mathbf{B}(\mathbf{r}_2) = \frac{\mu_0}{4\pi} \iiint_{V_1} \frac{\mathbf{J}(\mathbf{r}_1) \times \hat{\mathbf{R}}_{12}}{R^2} \, dv_1 \tag{A.21}$$

is reformulated exploiting equation A.6 to

$$\mathbf{B}(\mathbf{r}_2) = \frac{\mu_0}{4\pi} \iiint_{V_1} \mathbf{J}(\mathbf{r}_1) \times \left[-\nabla\left(\frac{1}{R}\right) \right] dv_1 = \frac{\mu_0}{4\pi} \iiint_{V_1} \left[\nabla\left(\frac{1}{R}\right) \right] \times \mathbf{J}(\mathbf{r}_1) \, dv_1. \tag{A.22}$$

Furthermore the rule $\nabla \times (a\mathbf{X}) = [\nabla a \times \mathbf{X}] + [a \nabla \times \mathbf{X}]$ with $a = \frac{1}{R}$ and $\mathbf{X} = \mathbf{J}(\mathbf{r}_1)$ allows the following relation

$$\nabla \times \left[\frac{\mathbf{J}(\mathbf{r}_1)}{R} \right] = \left[\nabla\left(\frac{1}{R}\right) \right] \times \mathbf{J}(\mathbf{r}_1) + \frac{1}{R} \nabla \times \mathbf{J}(\mathbf{r}_1). \tag{A.23}$$

The term $\nabla \times \mathbf{J}(\mathbf{r}_1) = 0$ and the del operator does not depend on the variables of the integral, hence the law of Biot-Savart can be written as

$$\mathbf{B}(\mathbf{r}_2) = \frac{\mu_0}{4\pi} \iiint_{V_1} \nabla \times \left[\frac{\mathbf{J}(\mathbf{r}_1)}{R}\right] \, dv_1 = \frac{\mu_0}{4\pi} \nabla \times \iiint_{V_1} \frac{\mathbf{J}(\mathbf{r}_1)}{R} \, dv_1. \tag{A.24}$$

Comparing the definition of the vector potential A.20 and the previous formulation leads to the following rule for $\mathbf{A}(\mathbf{r}_1)$.

$$\mathbf{A}(\mathbf{r}_1) = \frac{\mu_0}{4\pi} \iiint_{V_1} \frac{\mathbf{J}(\mathbf{r}_1)}{R} dv_1 \tag{A.25}$$

Furthermore the following alternative notation of the previous equation is useful to calculate the vector potential of filament current loops.

$$\mathbf{A}(\mathbf{r}_1) = \frac{\mu_0 I_1}{4\pi} \oint_{C_1} \frac{d\mathbf{r}_1}{R} \tag{A.26}$$

The magnetic flux caused by the current I_1 of the circuit $\mathbf{C}_1$ and passing through $\mathbf{C}_2$ is calculated by

$$\phi_{12} \quad = \quad \iint_{S_2} \mathbf{B} \cdot d\mathbf{s}_2 = \iint_{S_2} (\nabla \times \mathbf{A}) \tag{A.27}$$

The mutual inductance M_{12} between two individual circuits is defined as a geometry dependent factor describing the proportionality of the magnetic flux ϕ_{12} and the resulting currents.

$$\phi_{12} \quad = \quad M_{12} I_2 = \phi_{21} \tag{A.28}$$

$$M_{12} \quad = \quad M_{21} \tag{A.29}$$

To obtain M_{12}, Stokes theorem is used to transform equation A.27 to a line integral

$$\phi_{12} = \oint_{C_2} \mathbf{A} \cdot d\mathbf{r}_2 \tag{A.30}$$

that leads together with equation A.26 to the following useful formula for inductance calculations.

$$M_{12} = \frac{\phi_{12}}{I_2} = \frac{\mu_0}{4\pi} \oint_{C_2} \oint_{C_1} \frac{d\mathbf{r_1}}{R} \cdot d\mathbf{r_2} \tag{A.31}$$

Moreover the self inductance L describes the influence of the magnetic flux of one single loop to its own current

$$\phi_{11} \quad = \quad L \, I_1, \tag{A.32}$$

requiring calculation methods similar to equation A.31.

B Manual of the Power Grid Tools

The pre-layout power grid tool set ”PGrid” consists of two Perl programs accompanied by several different grid and blocking capacitor model types. To use these programs a Perl 5.x installation is required and the Spice compatible analog circuit simulator Titan is currently supported. The installation is rather straightforward, since it is sufficient to copy the tool directory to the installation directory of choice and to modify the search paths for the Perl libraries.

This chapter explains all tool parameters, the syntax of the configuration files for power grid geometries and interconnect technologies, and some customization options. Configuration files for two different interconnect technologies (90 nm and 130 nm CMOS) and a file that contains typical software options useful for Infineon’s analog design environment are available.

B.1 Creating a Power Grid Configuration

To use power grid models in a simulation it is necessary to create a configuration file where type, topology, physical dimensions and other parameters of such models are defined.

B.1.1 analyze.pl

The Perl script analyze.pl reduces the manual effort needed for creating such a configuration by extracting the useful data from the original netlist. The tool creates a configuration file that already contains the connectivity information and the hierarchy of the power grid model corresponding to the circuit structure under analysis. Moreover, the geometry data is filled with predefined or dummy values for all supported grid topologies. A configuration file that contains some options to customize the behavior of analyze.pl is supplied with the tool set and named ”IFXtyp.acf”.

To prepare a successful run of analyze.pl it is necessary to:

- copy IFXTyp.acf (from pgrid installation dir) to the simulation directory
- modify IFXTyp.acf to particular requirements
- create a titan netlist of the circuit

Then analyze.pl may be invoked with the following mandatory parameters:

`-n`	*filename*	the titan netlist
`-c`	*configfile*	the configuration file (IFXTyp.acf in this case)
`-o`	*outputfile*	the name of the output files (*outputfile*.grd.cfg and *outputfile*.blk.cfg)
`-s`	*supply*	list of supply names to analyze (e.g. vdd1 vss1 vdda)

Moreover, these optional parameters may be used:

`-f`	*namelist*	a filter: only the sub-circuits or instances of namelist are printed
`--list`		prints no configfile but a power supply connectivity graph
`-h`		a short help

The analyzed supply names are used on the toplevel of the circuit and the tool descends in the circuit hierarchy following the supply connections. Therefore changing supply names over hierarchy levels (e.g. from ”vss” to ”gnd” in sub-blocks) represents no issue for the software. The filter `-f` option is useful for large design where the power supply of selected critical blocks is analyzed. This option accepts both subcircuit and instance names to allow a convenient selection of either particular instances or of all instances belonging to a subcircuit type. Moreover, the `--list` option provides an overview of the supply connectivity in the Spice netlist, which is not always easily visibly in schematics due to the inherited connections feature of the Cadence design environment, especially in designs with multiple supply domains.

Example Call:

```
analyze.pl -c IFXtyp.acf -n test.nd.tit -o test -s vdd! vss! -f top xi1
```

This command creates a power grid configuration file that includes VDD! and VSS! grids for the toplevel and the subcircuit xi1. The grid configuration is stored in ”test.grd.cfg” while decoupling capacitor definitions are stored in ”test.blk.cfg”.

B.1.2 The Configuration File for analyze.pl

This file is used to configure the behavior of analyze.pl in detail, where initial values are defined for most of the power grid and blocking capacitor parameters.

```
* config for analyze.pl

* filter: analyze only follows these nodenames
*         normally vss/lsup can be discarded for blocking caps
*         these caps are already covered by the vdd analysis run
*
```

```
*  use regular expression in the filters:
*
*  examples:
*  /.*(vdd|hsup|vss|lsup).*/ if vdd or vss or lsup or hsup in the name
*  /.*/                      all characters
*

 .pfilter   = '/.*(vdd|hsup|vss|lsup).*/'   * analyze of power grid
 .no_caps   = '/.*(vss|lsup).*/'            * analyze of blocking caps

* initial values

 .struct    = 'bus'
 .wire_type = 'RLC'
 .equation  = 'Grover'

 .line_met  = 'M1'
 .bus_met   = 'LB'
 .line_w    = '1.0u'
 .bus_w     = '2.0u'
 .line_l    = '4.0u'

 .cap_m     = '5'
 .cap_node2 = '__smart'

 .replace   = 'Csimple'
 .remove    = 'Csimple'
```

The parameter `.pfilter` is a regular expression that modifies the behavior of the analyze process. Every node name connected to the analyzed power grid is checked against this regular expression. If the result is true the corresponding subblock is analyzed, otherwise the block and all its subblocks are discarded. The main purpose of `.pfilter` is to ensure that only power nodes are considered in the grid configuration files, since many designs may contain normal signal nodes which are constantly tied to ground or VDD.
Furthermore, `.no_caps` is a regular expression similar to `.pfilter` that defines the power node names where no decoupling capacitor definitions will be printed into the control file. In most common cases it is not necessary to include the decoupling capacitors when ground networks are analyzed, since these capacitors will be covered during analyzing the corresponding VDD network.
The other parameters in this configuration file are default values for geometry parameter of the power grid and of the decoupling capacitor arrays. These values are user configurable, because in many applications parameters like the metal layer of the

supply grid are fixed by design constraints, hence the required typing effort could be reduced by clever choices of these default values.

The parameter `.cap_node2` has a special value `__smart` that invokes the capacitor node rule described in more detail in the decoupling capacitor section. If `__smart` is replaced by any other string, the ground node of the decoupling capacitor will be set to this string value and the correct ground node name is not examined by the software.

B.1.3 The Grid Configuration File

After executing analyze.pl, the grid configuration file (*.grd.cfg) contains a set of configuration blocks with a syntax similar to Spice netlists. Comments are indicated for each line by a leading * enabling a good readability of the grid configurations. Commands that fill more than one line require a leading '+' for all but the first line. All supported grid types will be printed by analyze.pl marked as comments, hence selecting a particular grid type only requires removing the comment indicators and filling in valid geometry data. The following example contains grid definitions for all possible topologies to explain the file format, but usable configurations have to describe only one single topology.

Global Parameters

The following mandatory parameters are required for each configuration file:

process — This parameter contains the filename where the technology dependent information like layer names, thicknesses or resistance values are stored.

fmax — The maximum signal frequency of the circuit. This data is required when skin and proximity effects are included in the model, because the filament dimensions will be optimized for this frequency.

equation — This parameter selects the set of equations that will be incorporated into the power grid model. While resistance computations are equal in all equation sets, the following options regarding inductance formulas are provided:

- *Grover* The self inductance equation published by Grover is utilized. This equation set is useful only for RLC or the more trivial models.
- *Enhanced* The improved self inductance equation introduced in chapter 4 is utilized. This equation set is again limited to RLC or the more trivial models.

- *Mutual* Besides the improved self inductance equation, this set also includes the mutual inductance formula of chapter 4. This equation set supports all network types that are currently provided by the power grid tools.

This equation option was initially created to allow selecting the best computation method for certain grid geometries or applications, but the inductance equations of chapter 4 turned out accurate enough to cover all orthogonal wire geometries used in on-chip applications. Therefore, using Mutual represents the best choice for all applications in the current tool version.

User Defined Variables

User defined variables are defined by the following syntax equal to standard Spice parameters

```
.param name  = ' value ',
```

where `name` defines the variable name and `value` may contain the corresponding numeric value or an arithmetic expression. Numeric values may be written in standard integer or floating point notations with integer exponents (e.g. 1.234E5, 98.76E-12), and scaling factors are additionally supported that allow shorter and better readable numerical values.

T	G	X / M	K	m	u	n	p	f
1.0E12	1.0E9	1.0E6	1.0E3	1.0E-3	1.0E-6	1.0E-9	1.0E-12	1.0E-15

Moreover, arithmetic expressions may contain the basic operands +,-,*,/, the brackets (,) and the exponential operator ** that also supports non-integer exponents. It is also possible to utilize other user defined variables in these expressions, if these variables are defined earlier in configuration files. Even though these expressions are finally evaluated by the simulator to provide convenient parameter alterations, the power grid tools pre-evaluate the expressions to check the validity of the configuration file and to provide a graphical output of the grid geometry. Hence, all required variables have to be defined within the grid configuration file.

```
*---------------------------------------------------------------------
* Control file for power grid parameters
*---------------------------------------------------------------------

  process   ./l90.prc     * process dependent data
  equation  Mutual        * the equations for RLCK element computations
  fmax      20G           * max signal frequency
```

```
  * an example of a user defined parameter

  .param  something = '1.0u'

  * an arithmetic expression that defines a parameter

  .param  derived   = '(something * 25.0)+10.0u'

  * single index nr allows parameter alteration

  .param  metalidx  = '4'

*----------------------- power grid definition ------------------------
  subcircuit  top
  local_sup   vdd!
*---------------------- connectivity information-----------------------
  blockname   sup_top
  top_dir     R0
  con_blocks  xi1 = 'R0'  xi2 = 'R90'
*------------------------------ measures ------------------------------
 measure     xi1  xi2
*--------------------------- power grid data --------------------------
 type RLCK
*---------------------------------------------------------------------
  struct star
     l_xi1='40.0u'   w_xi1='something' m_xi1='M1'
+    l_xi2='derived' w_xi2='something' m_xi2='metalidx'
*---------------------------------------------------------------------
  struct bus xb='0.0u' wb='10.0u' mb='LB'
     x_xi1='5.0u'   l_xi1='80.0u' w_xi1='10.0u' m_xi1='M1'
+    x_xi2='100.0u' l_xi2='40.0u' w_xi2='10.0u' m_xi2='M1'
*---------------------------------------------------------------------
  struct xybus xb='0.0u' yb='20.0u' wb='10.0u' mb='LB'
     x_xi1='5.0u'   y_xi1='-60.0u' w_xi1='10.0u' m_xi1='M1'
+    x_xi2='100.0u' y_xi2='-30.0u' w_xi2='10.0u' m_xi2='M1'
*---------------------------------------------------------------------
  struct free

*  I/O Nodes (do not change names)

    node b_vdd! x='5.0u'   y='0.0u'
```

```
    node p_xi1  x='50u'    y='0.0u'
    node p_xi2  x='250u'   y='-100.0u'

*  Internal Nodes

    node nint1  x='250u'   y='0.0u'

*  Wire Definitions

    wire b_vdd! p_xi1  w='something' m='M1,M2'
    wire p_xi1  nint1  w='something' m='M1,M2'
    wire nint1  p_xi2  w='something' m='1,3,4' * layer def. by index nr

  .end
*--------------------------------------------------------------------
```

Grid Block Definitions

Grid block definitions are required for each subcircuit and supply name that have to be covered by the power grid model. The grid definition and the connectivity data[1] is automatically extracted from the original netlist by analyze.pl, therefore with the exception of the rotation commands, no manual editing is typically required for these definitions.

subcircuit	The name of the subcircuit that will contain this particular power grid block. The toplevel of the circuit is represented by 'top'.
local_sup	The name of the supply node in the original subcircuit. The grid model connect this node to the local supply nodes of the sub-blocks in the next lower hierarchy level
blockname	The subcircuit name of the power grid model.
top_dir	This parameter is only available for toplevel grid blocks and allows to rotate or mirror the supply grid.
con_blocks	A list of all sub-blocks (instance names) that are connected to the supply node local_sup. Rotation or mirror commands may be used for individually for each subblock.

Grid Block Parameters

The following data objects are used to describe grid types and geometries. Most of the required data has to be edited manually since it is not possible to extract the information from the original netlist. To limit the typing effort to a minimum, dummy

[1] colored in yellow in the example

definitions for all parameters are provided thus in many cases only the actual values have to be completed.

measure A list of subcircuit instance names where 0 Volt DC voltage sources are inserted at the supply terminal. These sources are typically used to determine the current passing over them, enabling a convenient approach to analyze the supply current on a subcircuit level. Alternatively these sources may be utilized to define the node of interest in closed-loop loop gain analyzes as described in chapter 7.

type This parameter describes the network type for the grid block. Instead of globally selecting the grid type, it is possible to choose the level accuracy and complexity of the grid model for each subblock individually. The following model types are currently supported:

- RC — RC only power grid models covering the DC wire resistance and the capacitance of decoupling capacitor arrays. All grid topologies are supported.
- RLC — Similar to RC networks but the DC self inductance of wires is included. All grid topologies are supported.
- RLCK — Complete DC partial inductance models combined with the DC wire resistance and the capacitance of decoupling capacitors. Mutual inductance computations require a complete 2.5D geometry description so only the topologies ″xybus″ and ″free″ are supported.
- RLCKS3 — Similar to RLCK models but each wire segment is divided into 3 volume filaments to model the skin and proximity effect of on-chip wires at high frequencies.This type allows only ″xybus″ and ″free″ topologies.
- RLCKS5 — An alternative volume filament based model using 5 filaments per wire to provide more accurate results especially for wires with more than 10µm wire width.This type allows only ″xybus″ and ″free″ topologies.
- Dummy — A network with 0.1nΩ resistors to simulate the circuit with the hierarchy and nodenames of a power grid model but without grid parasitics. All grid topologies are supported.

Grid Topologies

The element struct defines the topology of the power grid block and the additional parameters describe the wire dimensions and alignments. Since no geometry data is available in the original netlist analyze.pl can print templates for all supported struct topologies that contain only the correct supply node names. The geometry data has to be filled in by the user. Besides the possibility to freely define orthogonal networks generalized bus and star topologies are provided that require less user interaction and

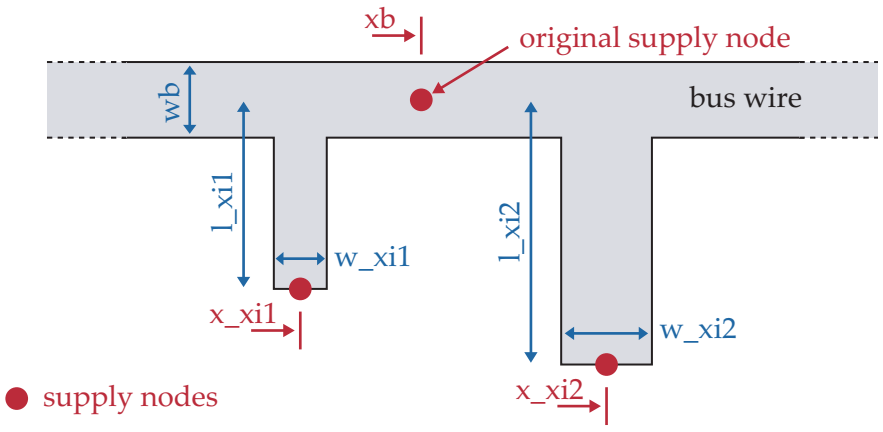

Figure B.1 Illustration of the simple bus structure and its parameters. Two subcircuits xi1 and xi2 are connected to the bus wire.

allow a fast model generation.

- star The star topology represents the most basic grid geometry that is supported by the toolset. It consists of the original supply node connected to all sub-blocks by separate wires and the wire width (w_xi*), length (l_xi*) and metal layer (m_xi*) may be defined individually for each connection. Since wire orientations and positions in the layout are not regarded, only Dummy, RC, and RLC network types may be used. Thus, the main purpose of such star topologies is a convenient and fast estimation of the power grid behavior.

- bus The bus topology as illustrated in figure B.1 consists of one bus wire that is described by the wire width (wb) and the metal layer (mb). The original supply node of the subcircuit is placed directly on bus wire and the coordinate (xb) is used to define the position on the bus. Moreover, each subcircuit is connected by a separate wire to the bus at the coordinate (x_i*). Again this basic bus structure, may be used only in Dummy, RC, and RLC network types, since the 2.5D geometry information are not complete.

- xbus or ybus These variants of the bus topology contain full 2.5D geometry information to enable mutual inductance computations, therefore slightly more editing effort is required than for the simple bus topology. As illustrated in figure B.2, xbus grids consist of a bus line along the x-axis and orthogonal connections to subcircuits, whereas bus wires of ybus grids are in parallel to the y-axis. All grid nodes are defined by x and y coordinates (x_xi* and y_xi*), and since the original supply node is placed on the bus wire, its coordinates (xb and yb) also define the position of the bus wire.

- free This option allows to freely define orthogonal geometries for the power grid block. The grid is composed from a set of nodes that contain 2D coordinates and

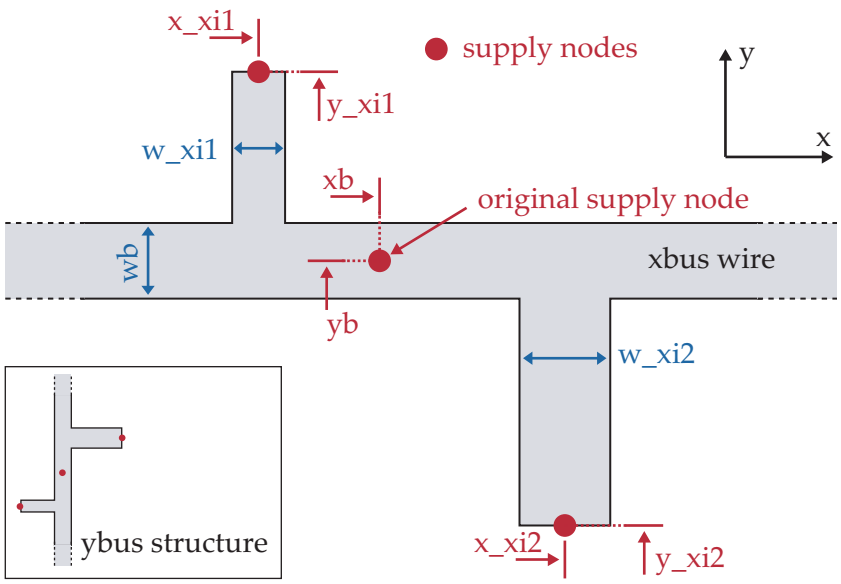

Figure B.2 Illustration of the xbus structure and its parameters, where two subcircuits xi1 and xi2 are connected to the bus wire. The ybus structure has similar parameters but the bus wire direction is along the y axis.

a set of wires connecting these nodes. In contrast to the other struct topologies, free definitions are spread over multiple lines and have to be placed between the lines with the keywords struct and .end.

Node definitions have to use the syntax
`node <nodename> x = '...' y = '...'`,
and wires between two nodes are defined by
`wire <nodename1> <nodename2> w = '...' m = '...'`.
Whereas only orthogonal wire geometries are supported by the power grid model, the number of nodes and wires is not limited by the tools, only by practical reasons. All wires that use one common node are connected even if the wires are placed on different metal layers, therefore besides defining corner or connection points, nodes may be used also like vias to switch metal layers. (No special via models are currently available.) Considering the connectivity to the rest of the grid, analyze.pl extracts the required supply node names from the netlist to ensure valid names, hence it is advisable to modify only the coordinates but not the names of these nodes. Finally it has to be noted that the user has to take care not to leave wires unconnected since such segments will cause problems during Spice simulations.

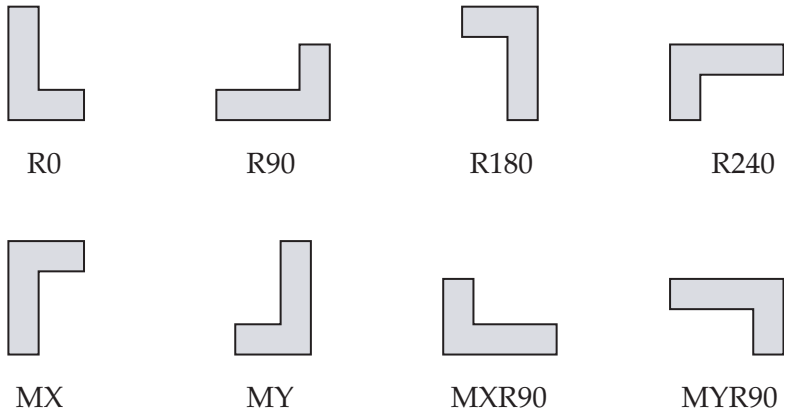

Figure B.3 Illustration of rotate and mirror commands for power supply grid geometries.

Rotation and Mirror Commands

Rotation and mirror commands were already mentioned in the grid block definition section since these command are applied to the subcircuit instances of a grid block, since rotation commands are required for each grid block instance to enable supply grids of multiply used subcircuits that have different directions. Rotation commands act hierarchically so all grid blocks at lower hierarchies are rotated according to their parent, nevertheless it is possible to apply additional rotation commands to these subcircuits. Furthermore, toplevel grids may be rotated by the parameter top_dir. The center of rotation or the position of the mirror axis is defined by the position of the original supply node as illustrated in figure B.2, and the following commands are supported by the tools and illustrated in figure B.3:

R0	No rotation or mirror operation. This is normally the default value.
R90	Rotation of the grid and its subgrids by 90 degrees counterclockwise
R180	Rotation the grid and its subgrids by 180 degrees counterclockwise
R240	Rotation the grid and its subgrids by 240 degrees counterclockwise
MX	The grid and its subgrids are mirrored using a mirror axis that is parallel to the x axis and intersects the original supply node.
MY	The grid and its subgrids are mirrored using a mirror axis that is parallel to the y axis and intersects the original supply node.
MXR90	A combination of two commands: At first the grid is mirrored using MX then it is rotated by R90.
MYR90	A combination of two commands: At first the grid is mirrored using MY then it is rotated by R90.

Rotate or mirror commands are only meaningful for the grid structures xbus, ybus and free where complete 2.5D coordinates are available, and the electrical behavior

is only affected for models that incorporate mutual inductance, because the relative position of wires is not required to compute resistance and self inductance elements. Changing the direction of certain grid block needs a model update since different wire segments will be parallel and require new mutual inductance elements to model this behavior.

Metal Layer Definitions

Metal layers have to be selected for each individual wire segments where two different notations are supported. The more intuitive layer names which are defined in the process description have the disadvantage that it is not possible to use user defined variables in the layer definition, therefore index numbers may be used alternatively. Additionally it is possible to define multiple layers for a wire segment resulting in two or more parallel wires that are connected at their nodes. Whereas changing metal layer indexes does not require a re-netlisting of the model, changing the number of metal layer requires an update since additional RLCK element have to be added to the netlist.

B.1.4 Decoupling Capacitor Arrays

```
.param csize = '50'
*------------------------ blockcap definition -------------------------
  subcircuit a_circuit
  supply     sup1 = 'hsup' sup2 = 'lsup'    * opt=forcenodes
*------------------------------ parameter -----------------------------
  parameters m = '10'
  type       remove = 'CPana' replace = 'Csimple'
*--------------------------------------------------------------------
  subcircuit a_circuit  * a second capacitor for hsup2
  supply     sup1 = 'hsup2' sup2 = 'lsup2'    * opt=forcenodes
*------------------------------ parameter -----------------------------
  parameters m = 'csize'
  type       remove = 'CPana' replace = 'Csimple'
*--------------------------------------------------------------------
```

Decoupling or blocking capacitor arrays may be defined for each subcircuit and supply name, and the resulting models are placed inside the subcircuit. Decoupling capacitor arrays are in most applications standard circuit elements and therefore already included in the schematics. Thus the power grid tools have to provide an option to find and replace such capacitor arrays by parametrized models generated by this software. Additionally it is also possible to simply add capacitor models to subcircuits without decoupling capacitors in the schematic.The capacitor models are defined and described in a separate configuration file (*.blk.cfg) that is also created and filled with

template definitions by analyze.pl. The syntax is again similar to Spice and allows the definition of user defined variables analogous to the the grid configuration.

subcircuit — This parameter contains the name of the subcircuit where the decoupling capacitor is placed.

supply — Two supply nodes are required that are connected to the capacitor terminals. The value of sup1 represents the supply node that is connected to the positive terminal of the capacitor and sup2 contains the nodename used for the negative terminal. The following rules determine the node names that are connected to the capacitor terminals and how this behavior may be modified.
In those cases where decoupling capacitors are found in the original netlist, the original nodenames of the capacitor terminals are used. The supply parameters of the configuration file are then ignored, but the option opt='forcenodes' (disabled by a comment in the example) may be used to force the tools to use the parameters sup1 and sup2 as intended.
Without decoupling capacitors in the original netlist analyze.pl assigns the supply node to sup1 and derives the ground node name sup2 from the supply node utilizing the following regular expressions in Perl syntax: $1vdd$2 → $1vss$2 or $1hsup$2 → $1lsup$2. In most cases the tool will provide the valid nodenames, and these two parameters addtionally enable designers to freely modify the connections. (e.g. for applications like 2 separate capacitor arrays for vdd domains that share one vss domain)

parameters — Currently only a parameter m is supported that represents the number of capacitor cells used in the decoupling array or a scaling factor for the capacitance. The value of m may be parametrized similar to the geometry parameters in the grid configuration file.

type — Two capacitor model types are required in the configuration file: The tools scan for capacitors of the type remove in the original netlist and replace them by capacitor models defined by replace . This value is also used when capacitor models are only added but nothing to replace was found. It is valid to use the same capacitor type for both parameters, because in this case the original circuit element is replaced by a parametrized version.

Capacitor types are represented by Perl objects stored in the blocking capacitor directory of the tool. Two different types Csimple and Cpana are supplied with the current tool version. Csimple creates ideal capacitors where the parameter m defines the capacitance and Cpana represents a capacitor based on the gate capacitance of a MOS transistor. This element uses m as a multiplication factor for the transistor and was used in the previously presented power amplifier analysis. Many different types decoupling capacitor arrays with differently scaled unity elements may be used

depending on the application and the technology, hence it is not possible to cover all options by predefined blocking capacitor models. To provide convenient customized capacitor models, new Perl objects with the same set of functions are automatically incorporated by the power grid tool if the corresponding file is stored in the blocking capacitor directory. The required object interface is described in detail in Cpana.pm that also provides a typical example for a decoupling capacitor model.

B.2 Generating and Using the Pre-Layout Power Grid Model

When power grid and decoupling capacitor configuration files are prepared the Perl program patchpwgrid.pl may be invoked to generate a simulation netlist that contains the original circuit, the power grid and the decoupling capacitor models (*.nd.tit). All model parameter definitions including the user defined variables are stored in an additional Spice netlist (*.param.nd.tit) and both files are used as input files for the circuit simulator.

To call patchpwgrid.pl these files have to be available in the working directory:

- the original netlist
- a grid configuration file (*.grd.cfg)
- a decoupling capacitor configuration file (*.blk.cfg)
- a process definition file (*.prc)

The program is called with the following command line parameters:

```
patchpwgrid.pl <original_netlist> <output_file> <config_file>
```

original_netlist	The filename of the original netlist.
output_file	The filename for the resulting netlist that includes the power grid. This parameter should contain only the required name of file, because file extensions are concatenated to the files output_file.nd.tit and output_file.param.nd.tit automatically.
config_file	The power grid and decoupling capacitor configuration files have to use the same filename with the different extensions .grd.cfg and .blk.cfg, hence again config_file must not contain file extensions.

Besides the two Spice netlists patchpwgrid.pl additionally generates a postscript file (output_file.ps) that contains a graphical illustration of the complete power grid. This illustration is based on the default values of user defined variables, since parametrized features of the power grid model have to be evaluated to numerical results for a proper illustration. Moreover the program also creates a Fasthenry compatible geometry file (output_file.geo) that was mainly used to evaluate the accuracy of the pre-layout

power grid model and offers an alternative approach to determine the electromagnetic behavior of a power grid. Unfortunately Fasthenry does not support circuit hierarchies when computing the interconnect impedance, therefore only flattened Spice netlists may be simulated with the resulting models.

B.2.1 The Process Configuration File

The process configuration file contains physical parameters of the metal layers that are available for a particular process. Each grid configuration loads such a configuration file[2], and all circuit element values of the grid model are computed using the layer descriptions stored in this configuration.

```
*********************************************
* example process configuration file
*********************************************

.process name='CMOS'

 .metal name='M1'    t=0.3u r=0.1  z=0.5u m=cu idx = 1
 .metal name='M2'    t=0.3u r=0.1  z=1.5u m=cu idx = 2
 .metal name='M3'    t=0.3u r=0.1  z=2.5u m=cu idx = 3
 .metal name='LB'    t=0.8u r=0.05 z=4.0u m=al idx = 4

*********************************************
```

The sample configuration contains all the required data fields for a 4 metal layer technology and shows both copper and aluminium layer definitions. The mandatory .process name=... parameter defines the name of the technology, and each metal layer is represented by a a structure indicated by .metal. Each valid metal layer definition requires the following parameters

- **name** The name of the metal layer. This name or alternatively the index value idx are used in grid configurations in metal layer definitions.
- **t** The thickness of the metal layer.
- **r** The resistivity of the metal layer per square. $R = r \cdot \frac{l}{w}$ where l and w are the length and width of a wire.
- **z** The height of the metal layer center above the surface of the substrate.
- **m** A material identifier where currently **cu** for copper and **al** for aluminium are supported.
- **idx** The metal layer index. Arbitrary numbers may be utilized for this parameter as long as these numbers are unique identifiers. Numerical layer identifiers are more convenient to use if automatic parameter alterations for metal layers are executed in Titan.

[2]The grid config parameter process defines the filename of the required process configuration file.

C Example of a Power Grid Configuration

The following power grid configuration was used for AC stability analyzes of a 5 stage fully integrated power amplifier. An illustration of this power grid is drawn in figure 6.13 and simulation results are presented in the corresponding chapter.

```
*-------------------------------------------------------------------------
* Control file for power grid parameters
*-------------------------------------------------------------------------

process    ./l90_420.prc
equation   Mutual
fmax       20G

*-------------------------------------------------------------------------

* parameters for blocking capacitors
.param m_ldo    = '1'
.param m_bias   = '1000'
.param m_st1    = '2000'
.param m_st2    = '2000'
.param m_st3    = '2000'
.param m_st4    = '2000'
.param m_st5    = '3000'

*-------------------------------------------------------------------------

* parameters for vdd toplevel grid

.param m1_a1 = '8'
.param m1_a2 = '6'
.param m1_a3 = '5'
.param w1_a  = '50u'

.param m2_a1 = '4'
.param w2_a  = '5u'

.param XVDD  = '-400u'
.param YVDD  = '200u'
.param l_ldo = '51u'

.param XBia = 'XVDD+20u+w2_a'
.param YBia = 'YVDD+20u+w1_a'

* parameters for vdd stage
```

```
.param XB      = 'XVDD'
.param YB      = 'YVDD'

.param seph     = '20u'
.param sepv     = '75u'

.param w1_b    = '20u'
.param w2_b    = '50u'
.param w3_b    = '30u'

.param m1_b1   = '8'
.param m1_b2   = '6'
.param m1_b3   = '5'
.param m2_b1   = '6'

.param  d_b1   = '(seph)'
.param  d_b2   = '(sepv)'

* coordinates for the amplifier stages

.param stage_y = '-330u'

.param ys1     = 'stage_y'
.param ys2     = 'stage_y'
.param ys3     = 'stage_y'
.param ys4     = 'stage_y'
.param ys5     = '-550u'

.param xs1     = '10u'
.param xs2     = '150u'
.param xs3     = '300u'
.param xs4     = '600u'
.param xs5     = '1070u'

*------------------------ power grid definition ------------------------
  subcircuit  top
  local_sup   vddpa!
*----------------------- connectivity information-----------------------
  blockname   sup_top
  top_dir     R0
  con_blocks  xi186='R0'  xi193='R0'
*------------------------------ measures -------------------------------
  measure     xi186  xi193
*---------------------------- power grid data ---------------------------
  type RC
*--------------------------------------------------------------------------
  struct free

*  I/O Nodes (do not change names)

    node b_vddpa! x='XVDD'       y='YVDD'
    node p_xi186  x='XVDD+l_ldo' y='YVDD'
```

```
    node p_xi193  x='XBia'       y='YBia'

*  Internal Nodes

    node nint1    x='XBia'   y='YVDD'

*  Wire Definitions

    wire b_vddpa! nint1    w='w1_a' m='m1_a1,m1_a2,m1_a3'
    wire nint1    p_xi186  w='w1_a' m='m1_a1,m1_a2,m1_a3'
    wire nint1    p_xi193  w='w2_a' m='m2_a1'

  .end
*--------------------------------------------------------------------------
*------------------------ power grid definition ------------------------
  subcircuit  rf_pa_79g_sim
  local_sup   hsup
*----------------------- connectivity information-----------------------
  blockname   sup_rf_pa_79g_sim
  con_blocks  xi151='R0'  xi25='R0'  xi16='R0'  xi21='R0'
+             xi150='R0'
*------------------------------ measures ------------------------------
  measure     xi151  xi25  xi16  xi21
+             xi150
*--------------------------- power grid data ---------------------------
  type RLCKS3
*--------------------------------------------------------------------------
   struct free

*  I/O Nodes (do not change names)

    node b_hsup   x='XB' y='YB'
    node p_xi151  x='xs3' y='ys3+1u'
    node p_xi25   x='xs4' y='ys4+1u'
    node p_xi16   x='xs5' y='ys5+1u'
    node p_xi21   x='xs2' y='ys2+1u'
    node p_xi150  x='xs1' y='ys1+1u'

*  Internal Nodes

    node na1 x='XB + 1.0*d_b1 + w1_b*0.5'             y='YB'
    node na2 x='XB + 2.0*d_b1 + w1_b*1.5'             y='YB'
    node na3 x='XB + 3.0*d_b1 + w1_b*2.0 + w2_b*0.5'  y='YB'
    node na4 x='XB + 4.0*d_b1 + w1_b*2.0 + w2_b*1.5'  y='YB'
    node na5 x='XB + 5.0*d_b1 + w1_b*2.0 + w2_b*2.0'  y='YB'

    node nb1 x='XB+1.0*d_b1+w1_b*0.5'  y='YB-0.5*w3_b-4.0*d_b2-w2_b*2.0-w1_b*1.5'
    node nb2 x='XB+2.0*d_b1+w1_b*1.5'  y='YB-0.5*w3_b-3.0*d_b2-w2_b*2.0-w1_b*0.5'
    node nb3 x='XB+3.0*d_b1+w1_b*2.0+w2_b*0.5'  y='YB-0.5*w3_b-2.0*d_b2-w2_b*1.5'
    node nb4 x='XB+4.0*d_b1+w1_b*2.0+w2_b*1.5'  y='YB-0.5*w3_b-1.0*d_b2-w2_b*0.5'

    node nc1  x='xs1' y='YB - 0.5*w3_b - 4.0*d_b2 - w2_b*2.0 - w1_b*1.5'
```

```
    node nc2  x='xs2' y='YB - 0.5*w3_b - 3.0*d_b2 - w2_b*2.0 - w1_b*0.5'
    node nc3  x='xs3' y='YB - 0.5*w3_b - 2.0*d_b2 - w2_b*1.5'
    node nc4  x='xs4' y='YB - 0.5*w3_b - 1.0*d_b2 - w2_b*0.5'
    node nc5  x='xs5' y='YB'

*  Wire Definitions

    wire b_hsup na1 w='w1_a' m='m1_b1,m1_b2,m1_b3'
    wire na1    na2 w='w1_a' m='m1_b1,m1_b2,m1_b3'
    wire na2    na3 w='w1_a' m='m1_b1,m1_b2,m1_b3'
    wire na3    na4 w='w1_a' m='m1_b1,m1_b2,m1_b3'
    wire na4    na5 w='w1_a' m='m1_b1,m1_b2,m1_b3'

    wire na1 nb1 w='w1_b' m='m2_b1'
    wire na2 nb2 w='w1_b' m='m2_b1'
    wire na3 nb3 w='w2_b' m='m2_b1'
    wire na4 nb4 w='w2_b' m='m2_b1'

    wire nb1 nc1 w='w1_b' m='m1_b3'
    wire nb2 nc2 w='w1_b' m='m1_b3'
    wire nb3 nc3 w='w2_b' m='m1_b3'
    wire nb4 nc4 w='w2_b' m='m1_b3'
    wire na5 nc5 w='w3_b' m='m1_b1,m1_b2,m1_b3'

    wire nc1 p_xi150 w='w1_b' m='m2_b1'
    wire nc2 p_xi21  w='w1_b' m='m2_b1'
    wire nc3 p_xi151 w='w2_b' m='m2_b1'
    wire nc4 p_xi25  w='w2_b' m='m2_b1'
    wire nc5 p_xi16  w='w3_b' m='m1_b1,m1_b2,m1_b3'

 .end
*--------------------------------------------------------------------------
```

Own Publications

[1] M. Unterweissacher, K. Mertens, T. Brandtner, and W. Pribyl, "Stability analysis of on-chip multi-stage RF power amplifiers," in *RFIC Radio Frequency Integrated Circuits Symposium*. IEEE, Jun 2007, pp. 471–474.

[2] M. Unterweissacher, T. Brandtner, K. Mertens, and W. Pribyl, "Inductance formulas adapted for direct use in Spice simulators," *IET Electronic Letters*, vol. 44, no. 2, pp. 92–94, January 2008.

[3] K. Mertens, M. Unterweissacher, M. Tiebout, and C. Sandner, "Integrated CMOS power amplifiers for highly linear broadband communication," in *16th Workshop on Advances in Analogue Circuit Design 2007 (AACD) Oostende*, Mar 2007.

[4] K. Mertens, M. Unterweissacher, M. Tiebout, and C. Sandner, *Analog Circuit Design: ch. 6 Integrated CMOS power amplifiers for highly linear broadband communication*, H. Casier, M. Steyaert, and A. H. v. Roermund, Eds. Springer, 2008.

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[1] "International technology roadmap for semiconductors: Process integration, devices, and structures," *ITRS*, 2007.

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