Mag. Stefan Padlesak

Eless deposition of platinum on silicon wafers

PHD THESIS

Thesis submitted for the degree of Doctor of natural science

submitted to

Graz University of Technology

in corporation with

Never stop thinking
Infineon Technologies Austria AG

Supervisors

Univ. Prof. Frank Uhlig
Institute of Inorganic Chemistry
Graz University of Technology

Dr. Petra Fischer
Infineon Technologies Austria AG

2009

Abstract

Modern electronic devices must fulfil a wide range of requirements. The containing microchips must be efficient, cheap and resistant against different environment influences (temperature, humidity, etc.). Moreover these microchips require low energy consumption, low heat heat emission, long lifetime, etc. The devices must be optimized for their certain application and often fulfil contrary requirements. One requirement for diodes is a high switching time, with an also high reverse voltage (VR). To achieve this goal platinum is diffused into the silicon. The platinum silicide reduces the lifetime of charge carriers and thus ensures a fast switching time. There are various possibilities to deposit a platinum layer on silicon. The standard process at Infineon is to vaporize platinum on silicon.

The goal of this thesis was to develop and test methods for electroless metal deposition of platinum on silicon and evaluate their probability to be used in ultra-large scale integration (ULSI).

Two methods to fulfill these requirements were developed.

The HF bath process is a plating bath containing hydrofluoric acid and dissolved platinum salt.

In the hydrazine spin coating process an aqueous solution of ammonium hexachloroplatinate and hydrazine are spinned on a wafer.

STATUTORY DECLARATION

I declare that I have authored this thesis independently, that I have not used other than the declared sources / resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

16.11.2009 Stefan Padlesak

Contents

Acknowledgements

My supervisor Petra Fischer has both given me relentless support throughout my work on this project. Besides initiating the project, she has both dedicated a great amount of time to discussing it with me and providing me with invaluable guidance while allowing me the freedom to make my own decisions at crucial points in the work. For this I would like to express my appreciation.
Further, I want to express my gratitude to the all Infineon employees, especially Gerhard Schmidt, Holger Schulze, Wolfgang Altenburg, Hildegard Hoefler, Heimo Moederndorfer, Emil Prax, Helmut Singer, Noreddine Zaami, Hannelore Wimmer.

I would also like to thank all members of the Uhlig-researchgroup TU Graz for their support.

Finally I appreciate the help and support of my family and friends.

1. Aims

The aim of this PhD thesis was the development of an electroless deposition process for platinum on silicon wafers. The requirements of the electroless metal deposition process are to deposit the platinum directly on the silicon on patterned or unpatterned wafers, to deposit platinum on p- or n-doped silicon from different base material or from different implantation doses of boron (B), phosphor (P) and arsenic (As). To be used in ultra-large scale integration (ULSI), it should be more cost effective than the platinum vaporize process, little to non influence on the other processes for the device. Catalytic precursor layers, e.g. palladium [18], tin [8], [27], should be avoided. The received device must have a similar electrical behavior as the reference diode.

2. Introduction

Layers of platinum silicide in semiconductors have been proven to enhance the life time of semiconductor devices. Platinum is mainly used in SIPFRED (single inline package fast recovery epitaxial diode) and IGBT (insulated gate bipolar transistor) to enable soft reverse recovery behavior and thus enhance the life time of the diode. The soft reverse recovery behavior is achieved through diffused platinum in the silicon. The platinum silicide in the semiconductor device reduces the diffusion lengths of the charge carriers and reduces their life time. So a desired forward voltage (VF) for certain applications is produced.

To produce a platinum silicide layer requires depositing a thin layer of platinum selectively on the silicon wafer, generating a platinum silicide layer on the surface of the wafer in the furnace at ca. 400 °C and diffusing the platinum atoms into the silicon at ca. 850 °C. To generate the desired forward voltage, the platinum atoms have to be diffused into the silicon.
Possible applications for metal deposition are sputter deposition, chemical vapor deposition (CVD), vacuum deposition, galvanic deposition, electroless deposition (EMD).

A standard application for the deposition of platinum on silicon wafer used in the semiconductor industry is to evaporate platinum on the silicon. This application is extremely cost intensive due to the poor yield in the evaporation apparatus as the platinum is not only vaporized on the wafers, it is deposited in the whole chamber of the apparatus and the high price of platinum. Therefore the semiconductor industry, especially Infineon, is interested in an alternative method to deposit a few nanometer thin layer of platinum on silicon. An alternative method is the electroless metal deposition process.

Electroless metal deposition processes are widely used in a variety of fields to provide metal coating of surfaces by a simple immersion in a suitable aqueous metal solution. Many advantages of electroless coating have been reported, namely selective deposition and a high purity, low operating temperatures, good filling characteristics, simplicity, and low cost of the process. These reasons make electroless metal deposition very appropriate for industrial applications. [4], [5]

Electroless metal deposition generally refers to one of two different processes. Direct electroless deposition, in which the metal is directly reduced by a reducing agent (e.g. by hydrazine) or a displacement reaction, in which a more active metal is responsible for the reduction process.

3. Review of Previous Studies

3.1. Deposition of platinum in Literature

There are several methods to deposit platinum. Each application is only usable for specific requirements and circumstances. After analyzing different methods described in literature, a decision of which methods to use and adapt for this project and its unique requirements, has been made.

Cachet, et. al., showed that it is possible to deposit platinum with perchloric acid ($HClO_4$) as reducing agent under UV light on silicon substrates. They use a ca. 2.10^{-3} mol/l solution of ammonium hexachloroplatinate ($(NH_4)_2PtCl_6$) and 1 mol/l perchloric acid ($HClO_4$). The UV light controls whether n-type or p-type silicon is prefered in the platinum deposition. [1]

Titan substrates could be plated with platinum using perchloric acid ($HClO_4$) as reducing agent. [10]

Rao, et. al., reported a method to deposit platinum with hydrazine (N_2H_4) as reducing agent on polyethylene terephtalate. They used palladium chloride ($PdCl_2$) to deposit a thin palladium layer on the polyethylene terephtalate. The palladium layer acts as catalytic site for the platinum electroless deposition. [18]

US Patent 3698939 describes a platinum plating bath with hydrazine as reducing agent under basic conditions, whereas US Patent 6391477 describes a hydrazine bath process under acidic conditions.
US Patent 3698939 uses a solution of ammonium hexachloroplatinate ($(NH_4)_2PtCl_6$), hydrazine (N_2H_4), ammonium hydroxide (NH_4OH), ammonium or alkali metal chlorides (NH_4Cl, NaCl, KCl) as stabilizer and wetting agents.

The net reaction is:

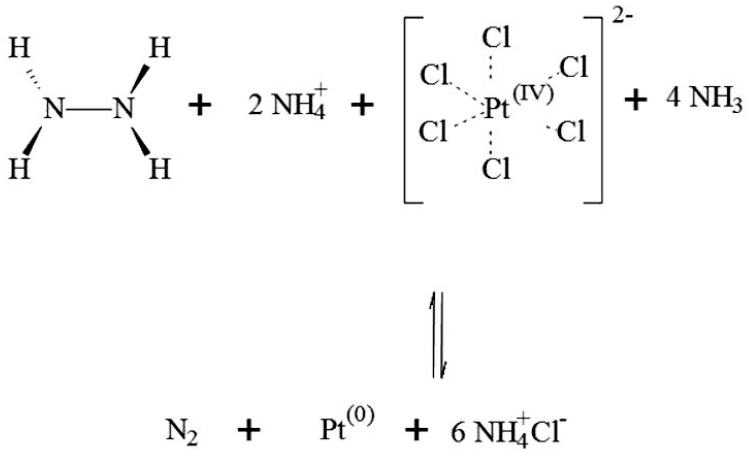

Figure 1 Reduction of ammonium hexachloroplatinate with hydrazine under alkaline conditions

US Patent 6391477 uses platinum nitrite or/and platinum ammine-nitrite salts (e.g. $Pt(NH_3)_2(NO)_2$) as platinum sources. Hydrazine (N_2H_4) is the reducing agent. A combination of acetic acid (CH_3COOH) and nitric acid (HNO_3) is used to get the pH value below 7. [24], [26]

The team about Steinmetz, et. al., deposits platinum on silicon with hydrazine (N_2H_4) as reducing agent under alkaline conditions. They used dissolved platinum ions, ethylenediamine (en) as complexing agent, hydrazine as reducing agent, imidazole ($C_3H_4N_2$) as secondary stabilizing agent and arsenic pentoxide (As_2O_5) as primary stabilizing agent at pH 13. [23]

Diaz, et. al., describes a method to deposit electroless gold and platinum on porous gallium nitride. The plating solution contained ammonium hexachloroplatinate ($(NH_4)_2PtCl_6$), hydrazine (N_2H_4) as reducing agent and DBSA (dodecylbenzenesulfonic acid salt) as surfactant at pH 10 – 11. [3]

Yeh, et. al., deposited a thin tin (Sn) layer on silicon. On this layer platinum was deposited with hydrazine as reducing agent. The contact hole has got the size of ca. 2 µm. The wafer was cleaned with RCA clean (Radio Corporation of America), dipped in HF, rinsed with water, tined, rinsed with water and deposited with platinum. The deposition bath contained chloroplatinic acid ($H_2PtCl_6.H_2O$), hydrofluoric acid (HF), ammonium chloride (NH_4Cl), ammonium hydroxide (NH_4OH) and hydrazine (N_2H_4). [27]

Platinum-rhodium alloys could be deposited with using platinum nitrite salt or platinum ammine-nitrite salt and hydrazine as reducing agent. [25]

Gorostiza, et. al., developed an autocatalytic plating bath for the platinum plating of semiconductors. The plating solution contains hydrofluoric acid (HF) under alkaline conditions, which oxidizes the silicon and reduces the platinum.

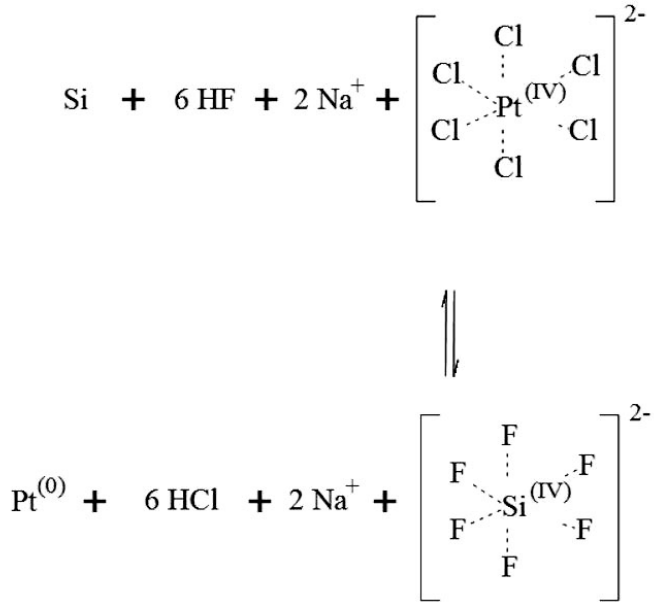

Figure 2 Reduction of sodium hexachloroplatinate with hydrofluoric acid under alkaline conditions

The reaction is autocatalytic and does not need an extra reducing agent. Their electrochemical bath contained aqueous hydrofluoric acid and solved disodium hexachloroplatinate hexahydrate ($Na_2PtCl_6.6H_2O$). [4], [5], [11]

Liang, et. al., plated pyrolyzed photoresits films (PPF) with platinum, using hydrofluoric acid (HF) as reducing agent. [12]

Zhang, et. al., decomposed platinum acetylacetonate ($C_{10}O_4H_{14}Pt$) dissolved in chloroform ($HCCl_3$) under UV light (172 nm) to deposit a thin platinum layer on silicon. The platinum film was used as reactive site for electroless copper plating. [28]

EVOH-g-SO_3H membrane was coated with platinum by Zhang, et. al.. They used hexaamine platinum chloride hydrate as platinum source and sodium boron hydride ($NaBH_4$) as reducing agent. [29], [30]

Phillips, et. al., used sodium boron hydride ($NaBH_4$) to reduce a platinum salt on a polymer. [15]

Jeannmenne, et. al., showed that medical polymer catheters can be coated with platinum with thin as precursor. [8]

Porter, et. al., demonstrated the deposition of platinum on germanium. They used solved tetrachloroplatinate (Na_2PtCl_4). The deposition proceeds via galvanic displacement in the absence of fluoride (HF, NH_4F), pH adjusters, complexing agents, or external reducing agents. Metallic films are formed spontaneously.

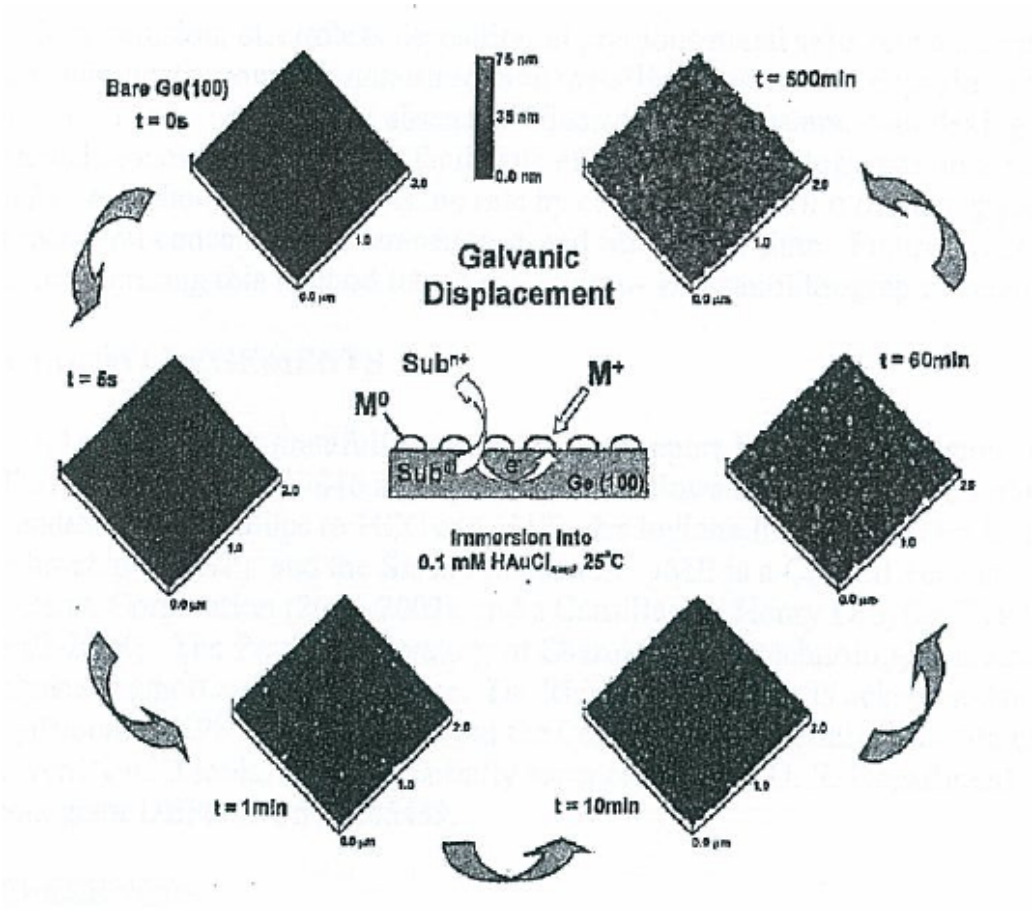

Figure 3 Schematic picture of galvanic displacement [16]

Germanium from the substrate is dissolved as germanium ions (Ge^{2+}), whereas platinum ions (Pt^{2+}) form the solution, tetrachloroplatinate (II), are deposited as platinum on the surface (see Figure 3). [16], [17]

An ion beam was used by Chattopadhyay, et. al., to decompose TMCP-Pt (trimethylmethylcyclopentadienyl-Pt) on silicon. Gallium ions (Ga^+) decompose TMCP-Pt. The remaining Pt forms a layer on the silicon. [2]

3.2. Analysing platinum a Literature survey

There are several methods to analyze deposited platinum. Each analyzing method has got its advantages and disadvantages. There is no ideal analyzing method.

Mostly scanning electron microscopy (SEM) is used to analyze the deposited platinum.
[1] to [5], [11], [12], [15] to [18], [23], [27] to [30]
SEM pictures show the form of the platinum layer. (The form of the layer contains information like: is it a homogenous layer or are there single platinum crystals or crystal clusters, where are the crystals localized, are the crystals distributed uniform over the layer or are they non-uniform distributed, etc.) They allow to estimate the quantity of the platinum roughly, but do not allow an exact measurement of the platinum as well as measuring the quality of the layer. (The quality of the layer contains information as whether it is it pure platinum or are there impurities, etc.)

Jeannmenne, et. al. use normal microscopie to observe the deposited platinum crystals on a latex urinary catheter. [8]

An other used microscopic method is transmissions electron microscopy (TEM). [1], [4], [5], [15], [27], [31]

To measure the thickness of the deposited platinum crystals a lot of groups use atomic force microscopy (AFM). [2], [4], [5], [16] to [18], [31]
The AFM is used in the intermittent mode or taping mode. The method delivers a 3D picture of the platinum crystals on the substrate.

To classify the deposited crystals (Is it pure platinum or are there impurities?) various methods are used. Some groups use energy dispersive X-ray (EDX). [3], [27] It is problematic to identify individual crystals on a substrate with EDX.
Often X-ray photoelectron spectroscopy (XPS) is used to determine the deposited particles. [4], [5], [16] to [18]

Other used spectroscopic methods are rutherford back scattering spectroscopy (RBS) [18], electron dispersive spectroscopy (EDS) [4], [5], UV spectroscopy (detects the thickness of a platinum acetylacetonate film) [29], [30], Fourier transformed infrared spectroscopy (FTIR) (detects the decomposing of an organic ligand) [28] to [30] and Auger electron spectroscopy (AES) [2], [11].

Other methods use electrical parameters to detect the platinum, such as I-V curves (current-voltage curves) [11]. Some groups use a potentiostatic method [23], [31] or cyclic voltammetry [12].
Platinum in the silicon of a semiconductor device reduces the diffusion length of the charge carriers and also reduces their life time. This effect changes the electrical parameters, mainly the forward voltage (VF), of the semiconductor device. The changed parameters can be used to measure the platinum in the device. [19], [21]

3.3. Options for the platinum deposition

After analyzing and evaluating the extensive literature for using in this project, five options are as promising starting points for further experiments.

1.) A bath with Ammonium hexachloroplatinate ($(NH_4)_2PtCl_6$) under irritation with UV light with perchloric acid ($HClO_4$) as reducing agent. [1]

2.) Various bath compositions with Ammonium hexachloroplatinate ($(NH_4)_2PtCl_6$) with hydrazine (N_2H_4) as reducing agent in basic conditions with various stabilizer and wetting agents. [23], [24]

3.) A bath with platinum nitrite or platinum ammine-nitrite salts with hydrazine (N_2H_4) as reducing agent in acid conditions. [26]

4.) A bath with sodium hexachloroplatinate (Na_2PtCl_6) and hydrofluoric acid (HF). The mechanism is a form of a displacement reaction in which silicon acts as the active metal. [4], [5], [11]

5.) A spin coating process with platinum acetylacetonate ($PtC_5O_2H_9$) solved in chloroform under UV light. [28]

1.) Experiments with perchloric acid did not show the desired results (see chapter "Experimental").

2. and 3.) The baths with hydrazine show the problem that the platinum is reduced in the solution, which leads to a black colloid platinum liquid. Although various compositions of complexing and stabilizing agents were tested none yield a productive plating solution. But an excellent alternative to a bath was found, a spin coating process. A solution with dissolved platinum salt is mixed with an aqueous hydrazine solution and instantly spinned on the silicon wafer at room temperature.

4.) The HF bath process showed good results also for different implantation doses.

5.) Experiments with platinum acetylacetonate required irritation with UV light at a high energy and a very short wave length (172 nm, vacuum UV light), which required special equipment. The funds for the equipment were not approved by Infineon. Vacuum processes if not really necessary, are avoided in semi conductor industry, because they are very expensive. It was not possible to decompose platinum acetylacetonate with a lower UV wave length and energy. The process with platinum acetylacetonate would not bring any cost benefit compared to the existing process.

4. Results and Discussion

4.1. HF bath process

Gorostiza, et. al. proved that it is possible to deposit platinum on silicon from an electrochemical bath containing aqueous hydro fluoric acid (HF) and solved disodium hexachloroplatinate hexahydrate ($Na_2PtCl_6.6H_2O$). [4], [5], [11]

Sodium (Na) is avoided in semiconductor industry, as sodium easily solves into silicon and easily diffuses in wafer. Sodium changes the electrical parameters of the chip. Thus for this project, ammonium (NH_4) is used as counterion instead of sodium.

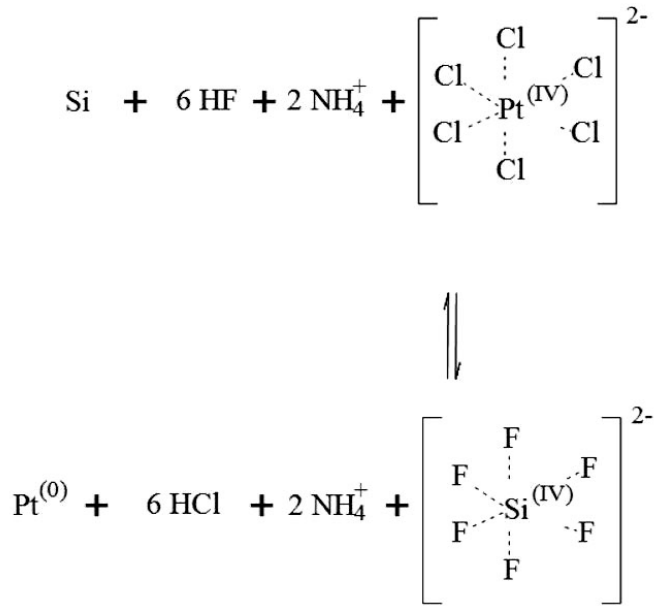

Figure 4 Reduction of platinum ions (ammonium hexachloroplatinate) with fluoride ions (hydrofluoric acid), net reaction in the HF bath process

The picture above shows the overall reaction in the HF bath process. The fluoride ions reduce the platinum and form a solvable silicon fluoride complex. The reaction concurs at the silicon

surface. The silicon is dissolved in the aqueous solution and the platinum is deposited on the silicon wafer. The exact reaction mechanism is not solved.

Acidic hydro fluoric solutions etch silicon oxide. On most Infineon products are a silicon oxide mask and a silicon contact hole. The platinum should be deposited in the silicon contact holes, whereas the silicon mask should not be etched, which is why the plating bath should have a higher pH than pure HF to ensure a lower silicon oxide etch rate.
Therefore the first tested plating bath consisted of 200 ml 50% HF, 200 ml 40% NH_4F, 300 ml 25% NH_3 and 3,091 g $(NH_4)_2PtCl_6.6H_2O$ with pH = 6,5. A wafer piece of wafer material 1 was immersed for 110 minutes at 70 °C. (For the exact experimental procedure see chapter "Experimental".)
The result was that the silicon surface of the wafer piece was strongly etched with a poor coverage of platinum crystals on it (see Figure 5).

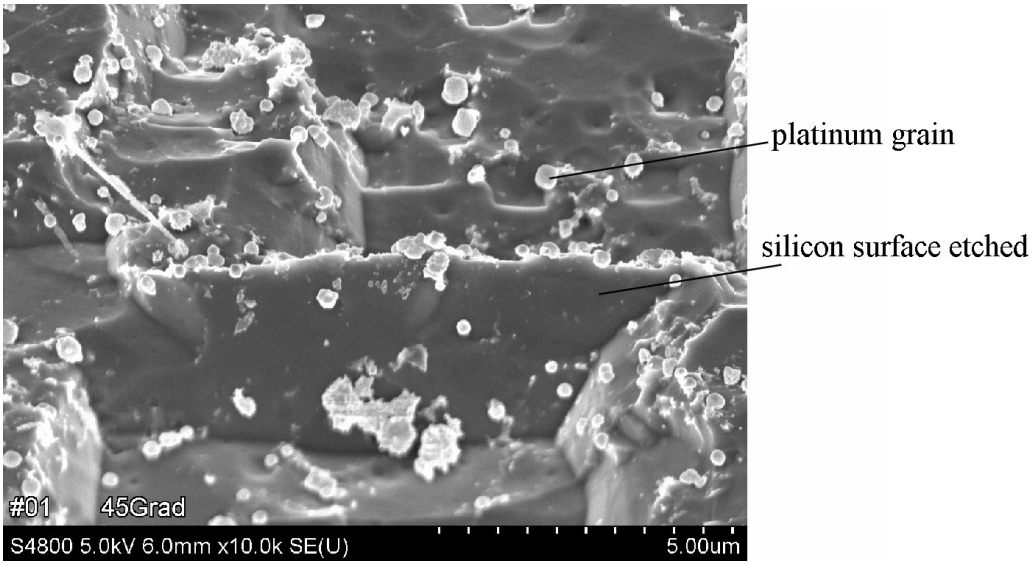

Figure 5 SEM picture of a silicon piece (wafer material 1) after the HF bath process, T = 70 °C, pH = 6,5, immersion duration = 110 min., Pt concentration in the bath ca. 0,0099 mol/l, the white spheres are platinum grains

The next experiment was with the same bath at a lower temperature (T = 40 °C) with a shorter immersion time (30 min). The SEM picture (see Figure 6) shows that the wafer piece was less etched and has got more platinum on it. The platinum spheres have got the form of a sea

urchin instead of a globular form observed in the previous experiment. The energy dispersive X-ray (EDX) measurement confirmed that the white spheres are platinum (see Figure 7).

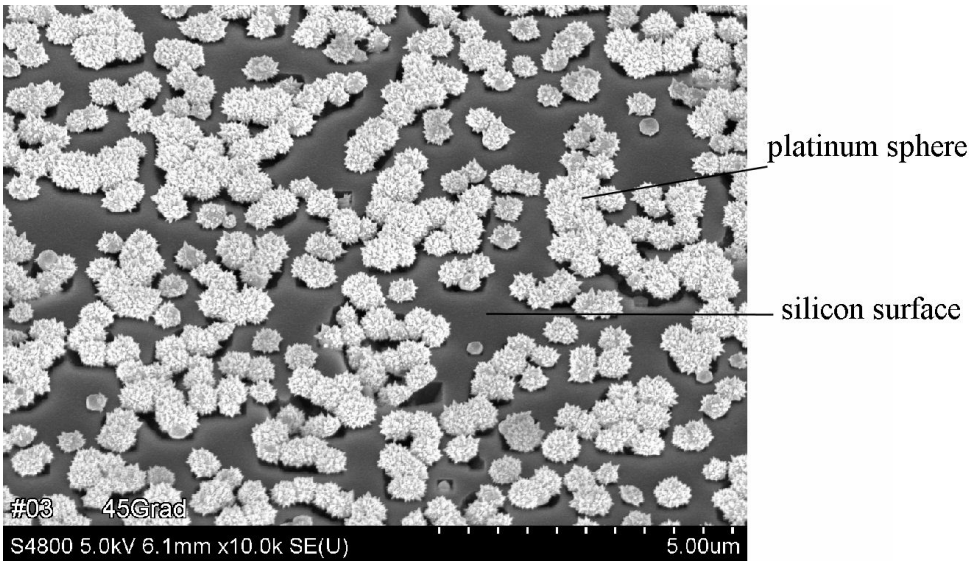

Figure 6 SEM picture of a silicon piece (wafer material 1) after the HF bath process, T = 40 °C, immersion duration = 30 min., Pt concentration in the bath ca. 0,0099 mol/l, the white spheres are platinum grains

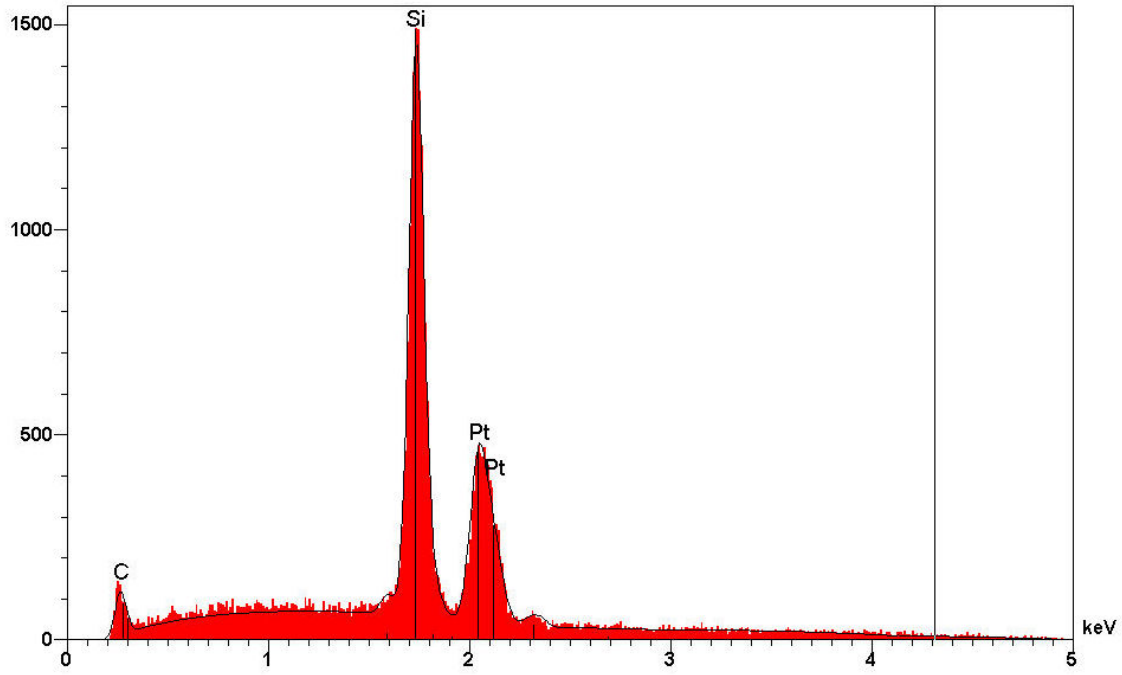

Figure 7 EDX with 5 keV of a silicon piece with platinum on it, the EDX is form the same sample as in Figure 6

These results were promising for further experiments. The bath parameters, bath composition, temperature, pH, must be optimized for a short process time, low etching rate of silicon and silicon dioxide, high platinum deposition rate and workable on different implanted silicon.

Ammonium hexachloroplatinate has a solubility in water (15 °C) of 7 g/l. [7]
The solubility in the presence of ammonia is drastically reduced. In the presence of 1 mol/l ammonium chloride, its solubility is only 0.0028g/100 ml (20 °C). [9]
Instead of ammonia, tetramethylammonium hydroxide (TMAH) was used as base, which improved the solubility of the platinum salt. Solubility of ammonia hexachloroplatinate in HF bath solution is approximately 0,147 g/100 ml (40 °C) (see chapter “Experimental”).

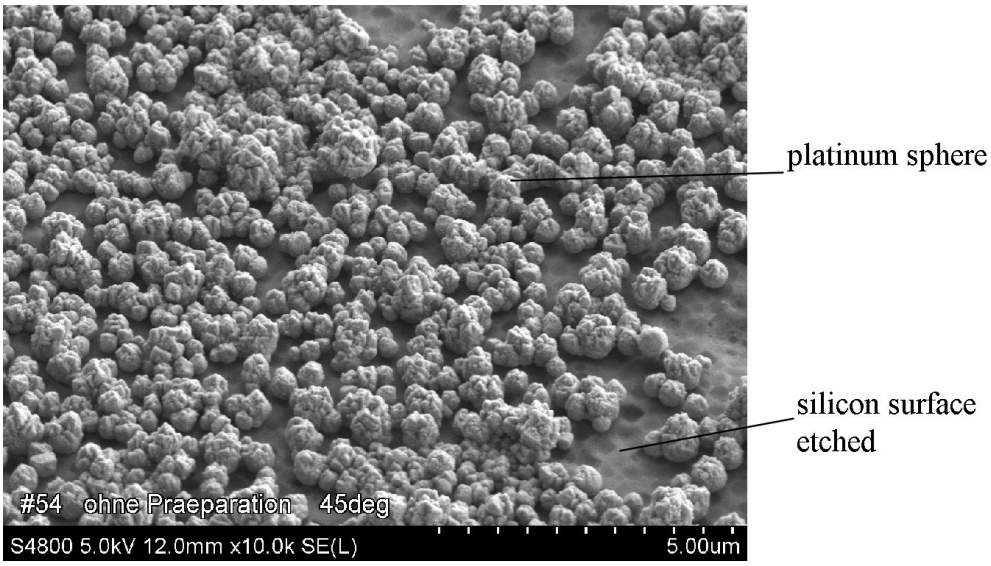

Figure 8 SEM picture of a silicon piece (wafer material 1) after the HF bath process, T = 70 °C, pH = 1,0, immersion duration = 30 min, Pt concentration in bath ca. 0,0013 mol/l

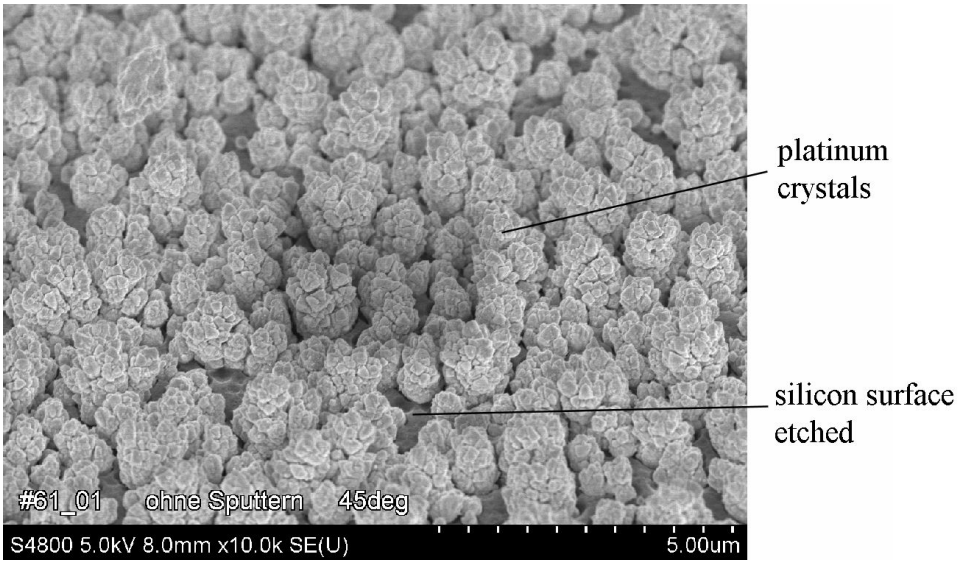

Figure 9 SEM picture of a silicon piece (wafer material 1) after the HF bath process, T = 70 °C, pH = 3,4, immersion duration = 30 min, Pt concentration in bath ca. 0,0013 mol/l

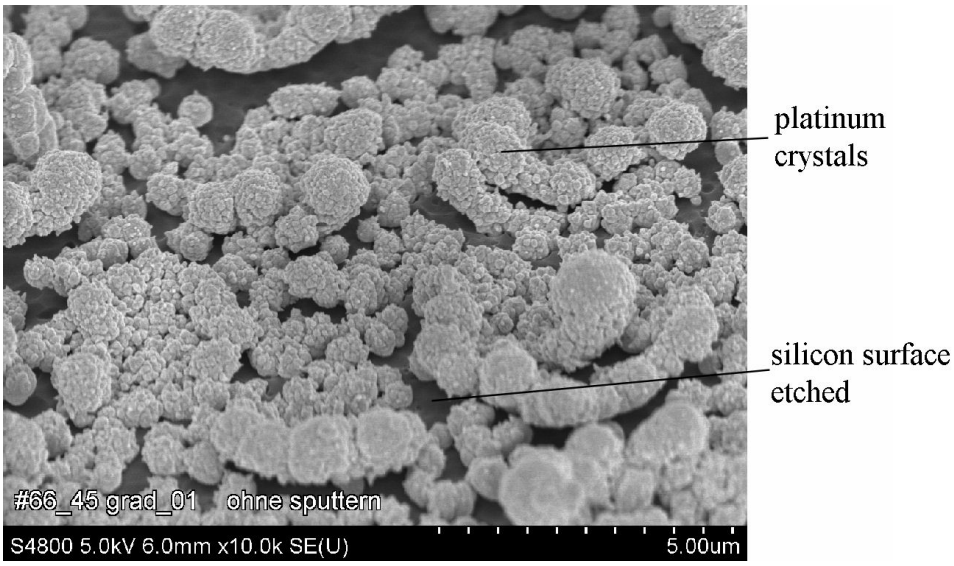

Figure 10 SEM picture of a silicon piece (wafer material 1) after the HF bath process, T = 70 °C, pH = 4,5, immersion duration = 30 min, Pt concentration in bath ca. 0,0026 mol/l

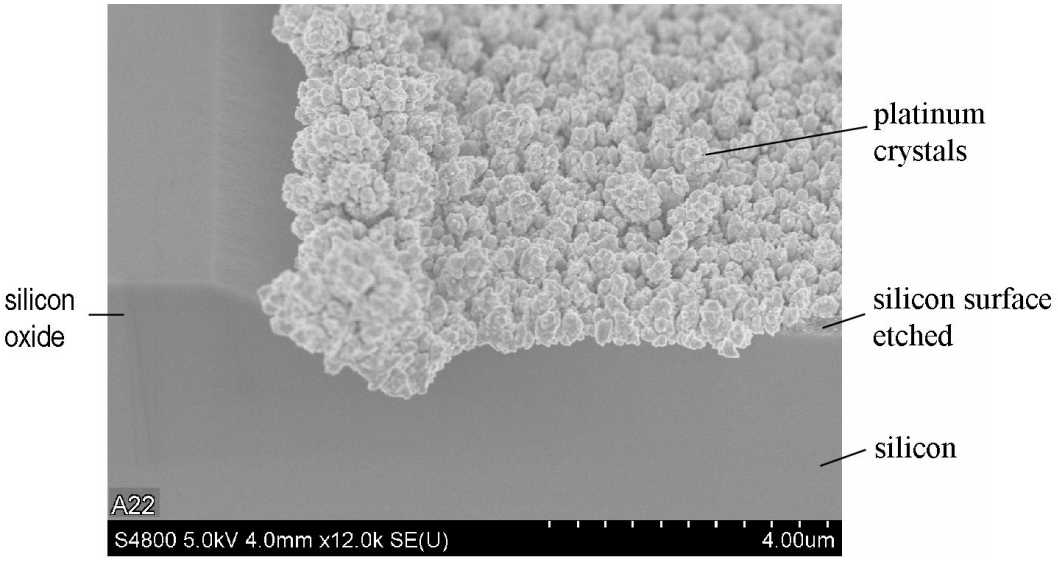

Figure 11 SEM picture of a silicon wafer (wafer material 2) with silicon oxide mask after the HF bath process, T = 68 °C, pH = 4,9, immersion duration = 10 min, Pt concentration in bath ca. 0,0021 mol/l

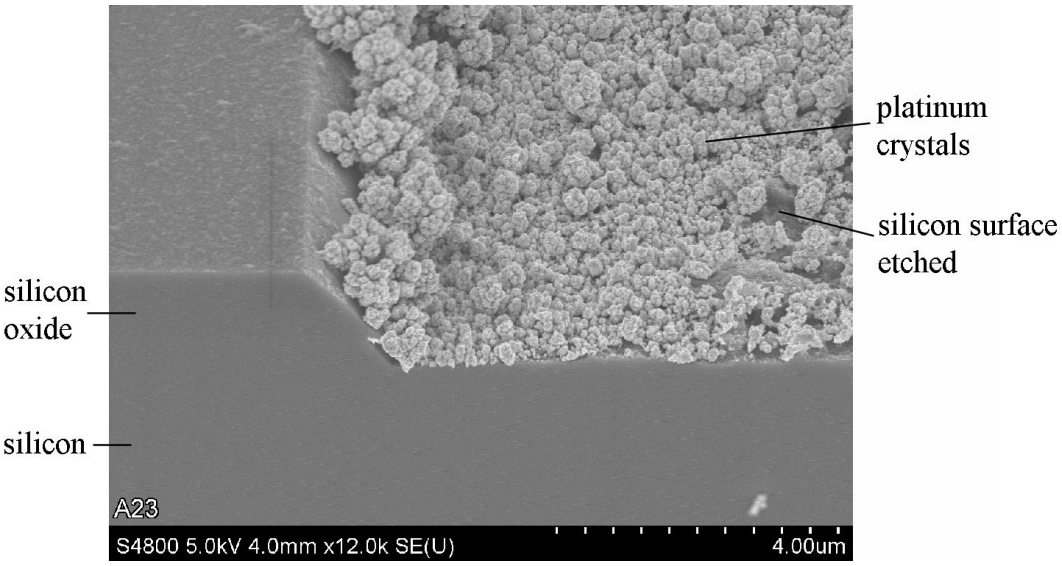

Figure 12 SEM picture of a silicon wafer (wafer material 2) with silicon oxide mask after the HF bath process, T = 71 °C, pH = 5,5, immersion duration = 10 min, Pt concentration in bath ca. 0,0021 mol/l

The SEM pictures (Figure 8 - Figure 12) show deposited platinum on silicon. The platinum is not deposited in a homogenous layer. It grows in spheres on the silicon. The form of the spheres, their size, the density on the silicon varies with the pH value of the bath. The optimal pH value for the desired process is pH 5,0. At pH 5,0 the deposited platinum spheres are big enough (over 200 nm) and dense enough (the whole silicon surface is covered), whereas the etch rate of silicon oxide and silicon is low enough (see Figure 11)

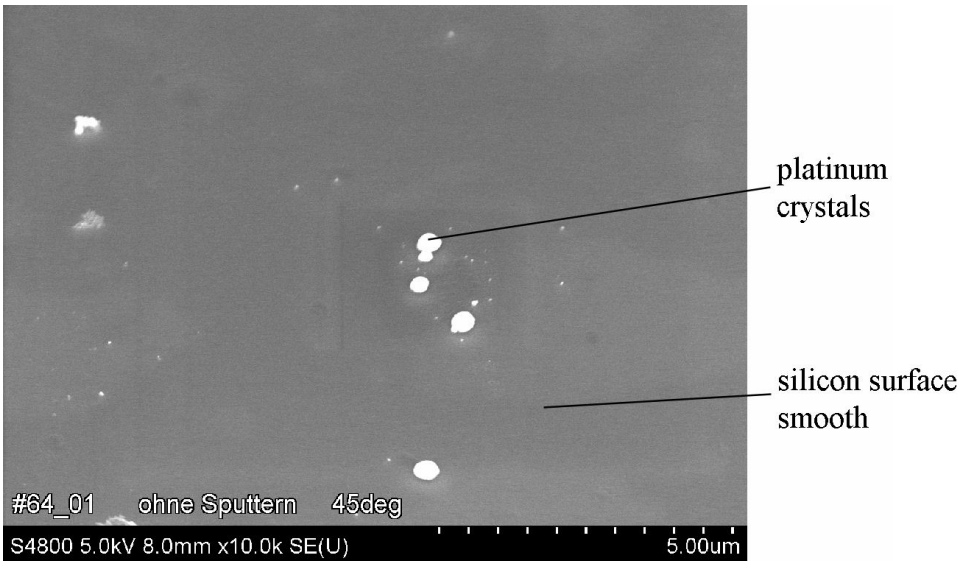

Figure 13 SEM picture of a silicon piece (wafer material 1) after the HF bath process, T = RT, pH = 4,5, immersion duration = 30 min, Pt concentration in bath ca. 0,0026 mol/l

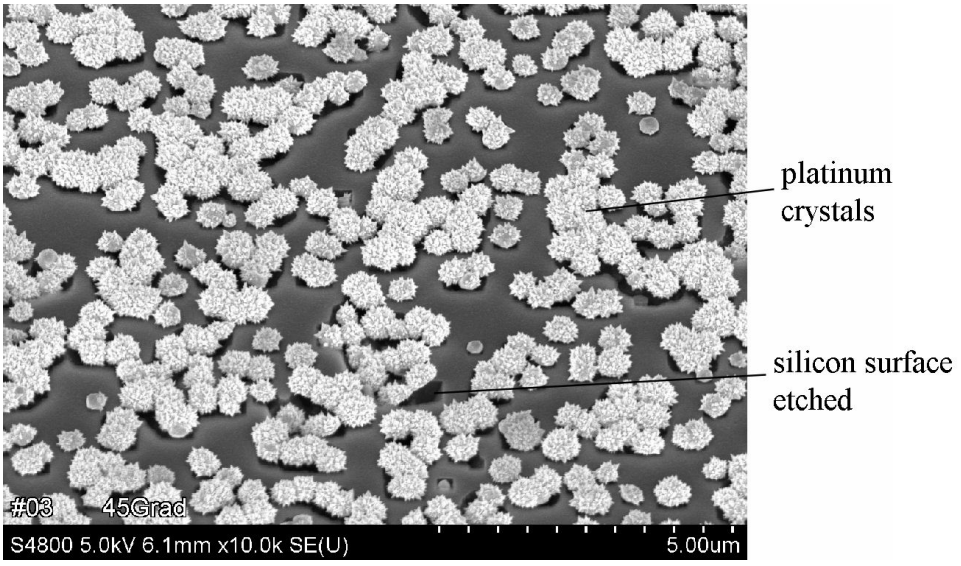

Figure 14 SEM picture of a silicon piece (wafer material 1) after the HF bath process, T = 40 °C, pH = 6,5, immersion duration = 30 min, Pt concentration in bath ca. 0,0099 mol/l

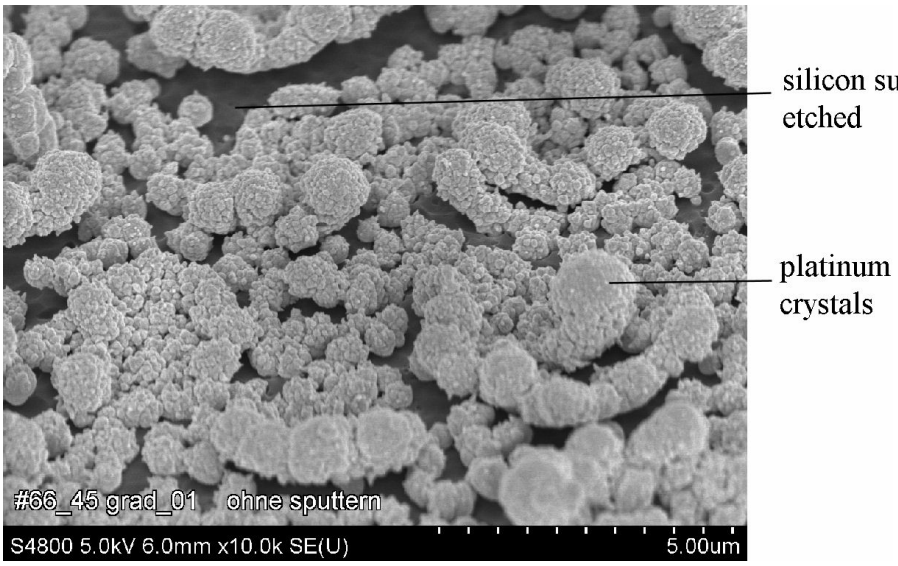

Figure 15 SEM picture of a silicon piece (wafer material 1) after the HF bath process, T = 70 °C, pH = 4,5, immersion duration = 30 min, Pt concentration in bath ca. 0,0026 mol/l

The electrochemical reaction was tested at room temperature, at 40 °C and at 70 °C.
(Figure 13 - Figure 15) The deposition rate increases according to the temperature. A higher temperature was not tested, because the vaporization of solvent at 70 °C is quite high and the deposition rate at 70 °C was sufficient. If the vaporization of the solvent is too high, the bath composition would change too much. To control the process the bath composition should be relatively stable and not change too much.

Various process times were tested (2, 5, 10, 15, 30, 60, 80, 110 minutes). Finally an immersion duration of 10 minutes has been used. 10 minutes are an acceptable time frame for a batch process in the semi conductor industry and a sufficient time for the reaction as the experiments have shown.

The deposition also depends on the implantation dose of the used silicon. The conducted experiments for this thesis suggest that wafers with a boron implantation have got a higher deposition rate compared to wafers with an arsenic implantation. Wafers with a phosphor implantation have got a similar deposition rate compared to wafers with an arsenic implantation. The fact that the deposition rate was not measured exactly but estimated with

SEM pictures (see chapter “Analyzing Platinum”) has to be considered. The electrochemical bath was optimized for the deposition of platinum on the Infineon Emmcon diode, which consists of an n-doped silicon layer with a boron implantation.

The HF bath process was optimized for its use for the Infineon Emmcon diode with a low silicon dioxide etch rate, a low silicon attack and a high platinum deposition rate. Although the process was optimized for the Infineon Emmcon diode, the silicon dioxide, which defines the silicon contact hole, was still etched. The etched silicon dioxide edge is responsible for a reverse voltage (VR) too low.
Therefore the front side of the wafer was protected with a resist and the platinum was only deposited on the back side of the wafer. That is why the stability of the resist in the HF bath has been tested to query whether enough platinum can be diffused in the wafer from the back side only. The resist TSMR showed a good adhesion in the HF bath and was easily removable with dimethylformamide (DMF) after the process. A measurement of the electrical parameters shows a similar VF and VR as the standard Emmcon diode.

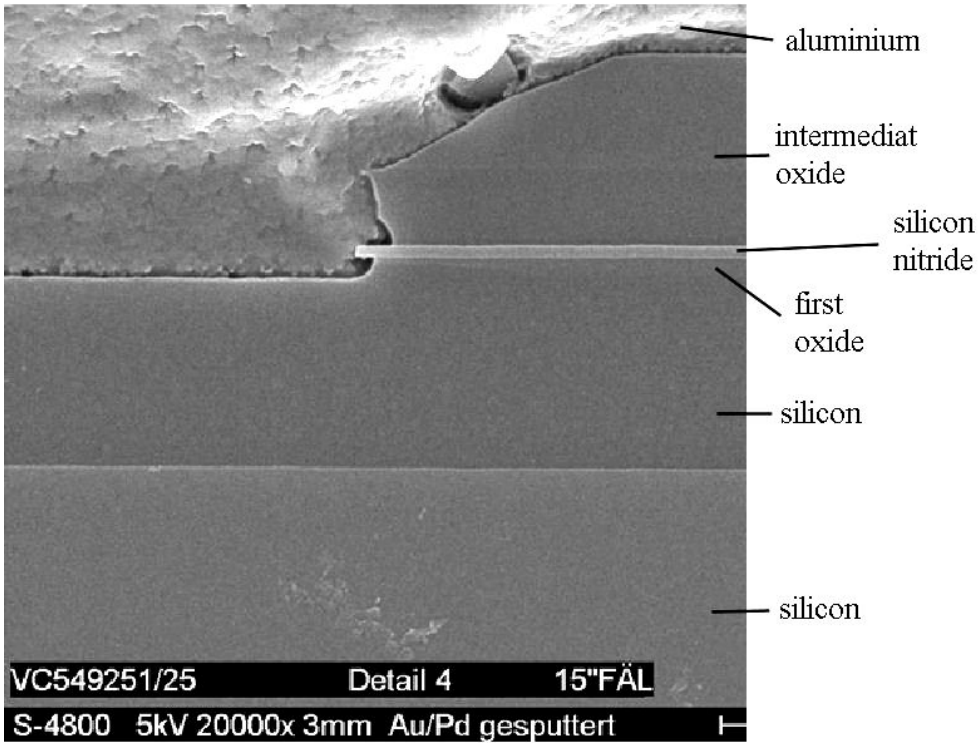

Figure 16 SEM picture of a finished Infineon Emmcon diode, the platinum was vaporized on the wafer and diffused in the silicon

The SEM picture shows an Infineon Emmcon diode manufactured with the standard process. The left side shows the silicon contact hole, the right side shows a thin silicon dioxide layer. On this silicon oxide layer is a silicon nitride layer (the light grey layer). On the silicon nitride is a thick intermediate silicon oxide layer. The whole is covered by an aluminum layer. The platinum is already diffused in the silicon. There is only a small under etch below the silicon nitride layer.

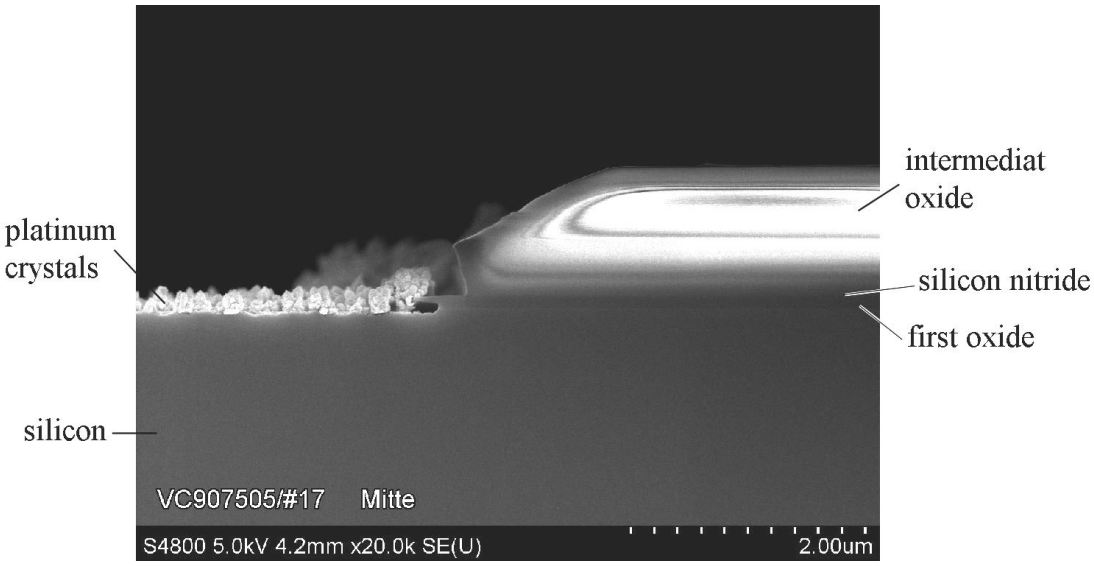

Figure 17 SEM picture of a Infineon Emmcon diode after HF bath process, T = 70 °C, pH = 4,9, immersion duration = 10 min., Pt concentration in the bath ca. 0,0021 mol/l

The SEM picture displays an Infineon Emmcon diode after the HF bath process. The left side shows the silicon contact hole. The white spheres on the silicon are deposited platinum grains. The right side shows a thin silicon dioxide layer. On this silicon oxide layer is a silicon nitride layer (the lighter grey layer). A thick intermediate silicon oxide layer covers the silicon nitride. There is a large under etch under the silicon nitride.

The SEM pictures display that the silicon oxide after the HF bath process, without protection of the front side, is thinned in comparison to the standard process. Also the under-etch below the silicon nitride layer is higher after the HF bath process.

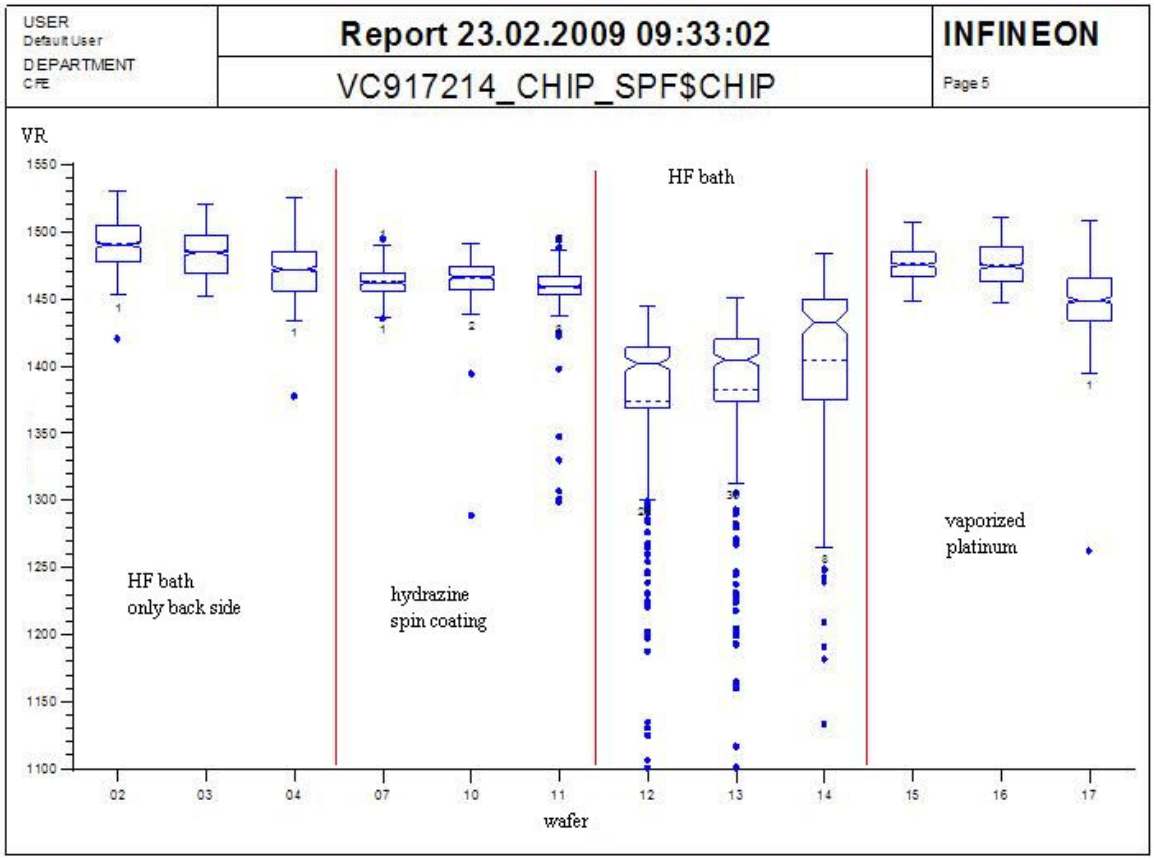

Figure 18 VR of a Infineon Emmcon diode, 02-04 HF bath only back side, 07-11 hydrazine spin coating process, 12-14 HF bath, 15-17 vaporized platinum

The picture illustrates the VR of Emmcon diodes with platinum deposited with the HF bath process from the front and back side and only from the back side compared to the standard process. The wafers with an unprotected front side in the HF bath present a lower VR. The wafers with a protected front side in the HF bath display a similar VR than the reference wafers.

4.1.1. Comparison between vapor coating and HF bath

The standard process by Infineon for the deposition of platinum on silicon is vapor coating. Therefore platinum is vaporized in a vacuum chamber. Inside the calotte on the side lie the silicon wafers. The Infineon vapor equipment has got only a capacity for 11 6-inch wafers or 8 8-inch wafers. The whole inside of the calotte (the wafers and the sidewall) is vaporized with platinum. The deposited platinum film thickness is 25 nm. The deposited film has got this thickness to guarantee a good uniformity on the wafer, although only a thin platinum layer (few nm) are needed for the forming of the platinum silicide.

The advantages of the HF bath process are the following:
As it is a batch process, it has a higher throughput.
In the HF-bath the platinum is only deposited in the silicon dioxide free contact holes and on the silicon oxide free back side. Therefore less platinum is needed for the process. In the vapor calotte the whole chamber is vaporized with platinum.

There are also disadvantages, namely:
The silicon dioxide mask is etched, which results in a lower VR.
The silicon is etched, which results in a rougher surface and a higher contact resistance. In the contact hole of the Infineon Emmcon diode the topmost layer is a thin silicon layer with a high boron implantation, which guarantees a low contact resistance. If the silicon layer is etched with the HF bath process the contact resistance increases.
Both problems can be solved however, by using a resist, which protects the front side during the deposition process. The platinum is deposited only on the back side of the wafer and only diffused from the back side. DLTS measurements show that the platinum concentration in silicon on the front side is the same as when the platinum is diffused from the front side (see chapter “Analyzing Platinum”).
This method can be only used for technologies, where etching of the backside does not matter. The back side of the Infineon Emmcon diode runs through grinding process after the platinum diffusion, so the rough silicon surface is removed.

4.2. Hydrazine spin coating process

There are various processes that use hydrazine to reduce platinum ions. A wide range of platinum salts, stabilizing, wetting, complexing agents are used.
In this thesis ammonium hexachloroplatinate is used as platinum source. According to literature alkali metals are used more often, but as already mentioned before they should be avoided in the semiconductor industry.

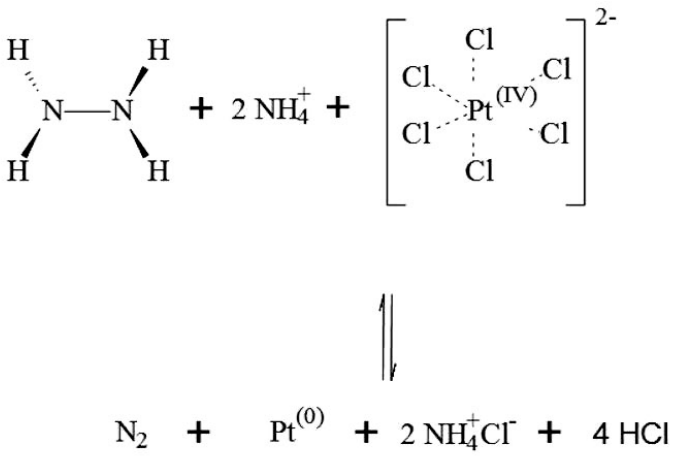

Figure 19 Reduction of platinum ions (ammonium hexachloroplatinate) with hydrazine

Figure 19 displays the overall reaction of the reduction of platinum ions with hydrazine as reducing agent. Hydrazine is decomposed to nitrogen and hydrogen ions and the platinum ions are reduced to platinum.

On the basis of US Patent 6391477, a bath containing ammonium hexachloroplatinate, hydrazine hydrate solution and acetic acid was tested. No platinum crystals were deposited on the silicon with this bath at 70 °C.
So the bath was modified. A solution containing ammonium hexachloroplatinate, hydrazine hydrate solution, acetic acid, hydrochloric acid and imidazole with pH 4,2 at 70 °C was tested.

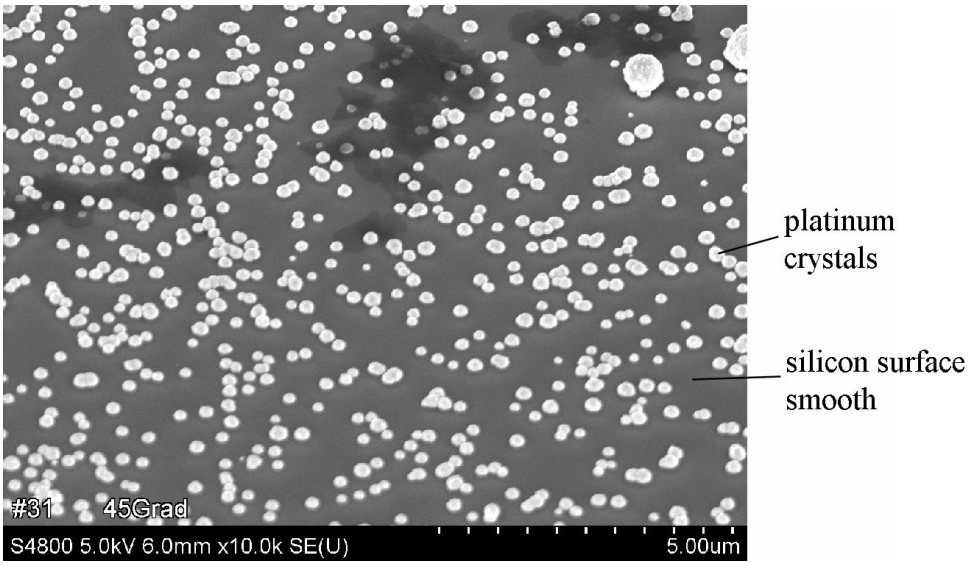

Figure 20 SEM picture of a wafer piece (silicon material 1) after a hydrazine bath, T = 70 °C, pH = 4,9, immersion duration = 10 min., Pt concentration in the bath ca. 0,0014 mol/l

The SEM picture shows that some platinum was deposited on the silicon, but the coverage of the platinum is not dense enough. Therefore future experiments with such baths should result in a higher platinum deposition rate. Moreover, the hydrazine bath has got a low stability. After a few minutes the solution turns black, as the platinum ions are reduced to colloid black platinum particles.

Various complexing and stabilizing agents were tested. Imidazole, ethylenediamine (en) and ammonium chloride did not produce a stable plating solution (see chapter “Experimental”).

To solve the stability problem, the process was modified. Instead of a bath process, a spin coating process was used. An aqueous ammonium hexachloroplatinate solution was mixed with an aqueous hydrazine solution and instantly put on the wafer. The wafer was spinning with 200 rpm to ensure a uniform distribution of the platinum.

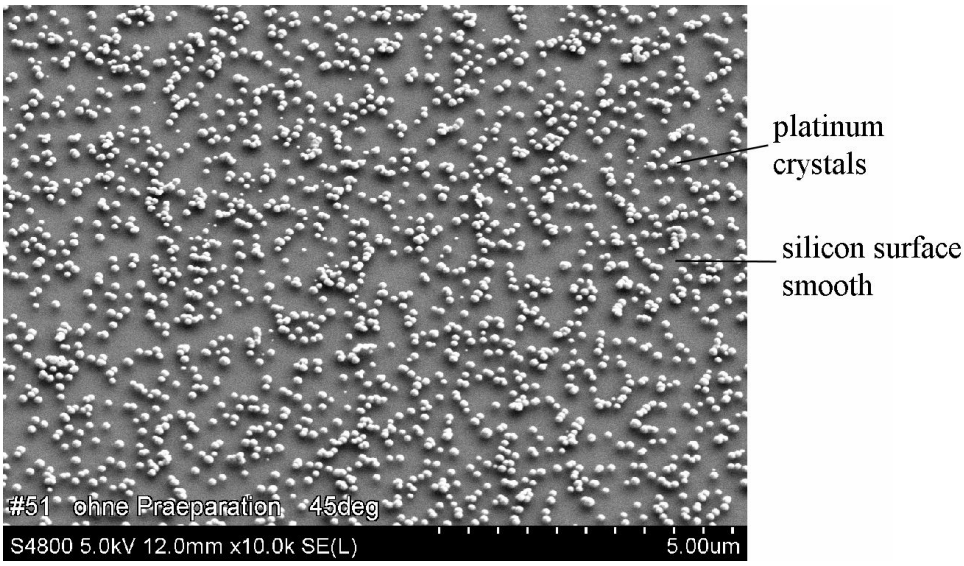

Figure 21 SEM picture of a wafer (silicon material 1) after the hydrazine spin coating process, T = RT, duration = 3 min., 10 ml platinum solution (No. 8), 10 ml hydrazine solution (No. 1)

The SEM picture shows a silicon wafer after the hydrazine spin coating process. The silicon wafer was dipped in 1% hydrofluoric acid for 1 min to remove the native silicon oxide layer. The wafer was rinsed with water and dried with nitrogen. The wafer was rotated at 200 rpm and an aqueous ammonium hexachloroplatinate solution and an aqueous hydrazine solution was put together on the wafer. The wafer was rinsed with water. After the water cleaning it was dried with a higher rotation. Finally the wafer was dried on air.

One problem with the spin coating process was that the wafer was hydrophobic, because the native oxide layer on the silicon was removed with the HF dip. So the aqueous solutions form droplets on the wafer instead of a homogenous liquid film. To solve this problem, mixtures with isopropanol and or a surfactant (Easywet) were tested. In mixtures with isopropanol white flakes flock out and proofed unpractical for further experiments. Solutions with Easywet turned out to be processable. It is important to avoid a too high concentration of Easywet, because it forms micelles in higher concentrations, which reduces its effect as surfactant.

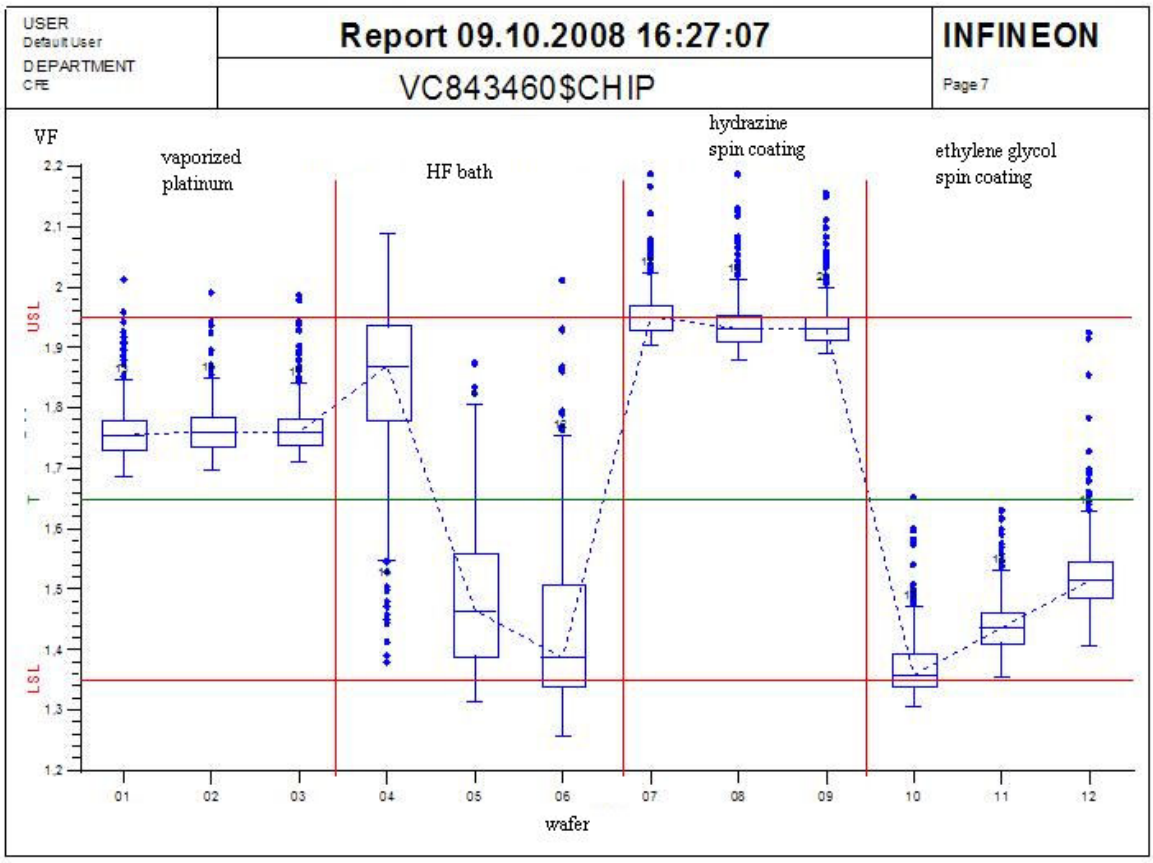

Figure 22 VF of a Infineon Emmcon diode, 01 to 03 vaporized platinum, 04 to 06 HF bath, 07 to 09 hydrazine spin coating process, 10 to 12 ethylene glycol spin coating process

The box plot diagram represents the VF of Infineon Emmcon diodes, in which the platinum was deposited with different methods. On wafer 01 to 03 the platinum was vaporized on the wafer. Wafer 04 to 06 were immersed in a HF bath with platinum. On wafer 07 to 09 the platinum was deposited with the hydrazine spin coating process, whereas wafer 10 to 12 were processed with the ethylene glycol spin coating process.

Wafer 01 to 03 have got a median VF from 1,75 V, which is inside the specification for the diode. The ideal VF for the Emmcon diode is 1,8 V.

Wafer 04 to 05 and 10 to 12 are not inside the specification. The median VF of wafer 07 to 09 are 1,94 V, which is too high, but it can be adjusted with a different temperature at the

platinum diffusion process. That is why the hydrazine spin coating process appears most promising for integration in ULSI.

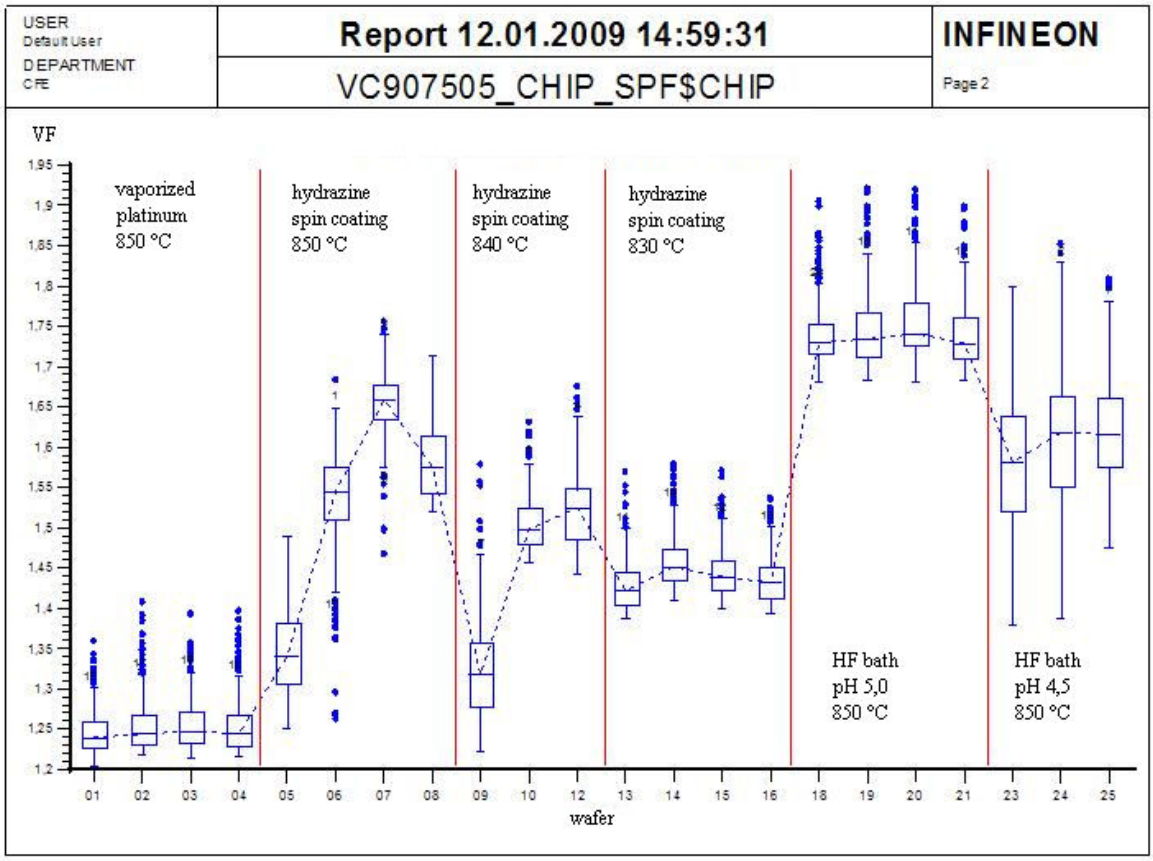

Figure 23 VF of a Infineon Emmcon diode, 01 to 04 vaporized platinum, 05 to 08 hydrazine spin coating process with 850 °C diffusion temperature, 09 to 12 hydrazine spin coating process with 840 °C diffusion temperature, 13 to 16 hydrazine spin coating process with 830 °C diffusion temperature, 18 to 21 HF bath with pH = 5,0 and 860 °C diffusion temperature, 23 to 25 HF bath with pH = 4,5 and 860 °C diffusion temperature

The box plot diagram shows the VF of Infineon Emmcon diodes, where the platinum was deposited with different methods and the diffusion temperature was varied. On wafer 01 to 04 the platinum was vaporized on the wafer. The low VF of approximately 1,25 V is an indicator

that no platinum was deposited on the wafer, although the operation was signed on the route paper.

On wafer 05 to 16 the platinum was deposited with the hydrazine spin coating process and the diffusion temperature was varied. The VF varies considerably and is too low. The low VF indicates that too little platinum is diffused in the silicon wafer. The used platinum solution (ammonium hexachloroplatinate dissolved in water with a surfactant) in this experiment has got a lower platinum concentration than the solution in the experiment with lot VC843460.

A lot is a quantity of components that have passed through the manufacturing process together. Changes in the manufacturing process affect all parts of a batch. Lot is also called batch. A lot normally consists of 25 wafers. VC843460 is an example for the Infineon nomenclature of lots. An explanation of the Infineon lot coding is given in the “List of Abbreviations”. The high variation of each hydrazine group was unexpected, as the results of VC84360 07-09 have a very low variation.

Wafer 18 to 21 were processed with a HF bath with a pH of 5,0. They have got a good VF with ca. 1,75 V and an acceptable variation. On Wafer 23 to 25 the platinum was also deposited with a HF bath, but at pH 4,5. Wafer 23 to 25 show a lower VF ca. 1,6 V with a higher variation. The SEM picture (Figure 25) shows that fewer platinum is deposited at pH 4,5.

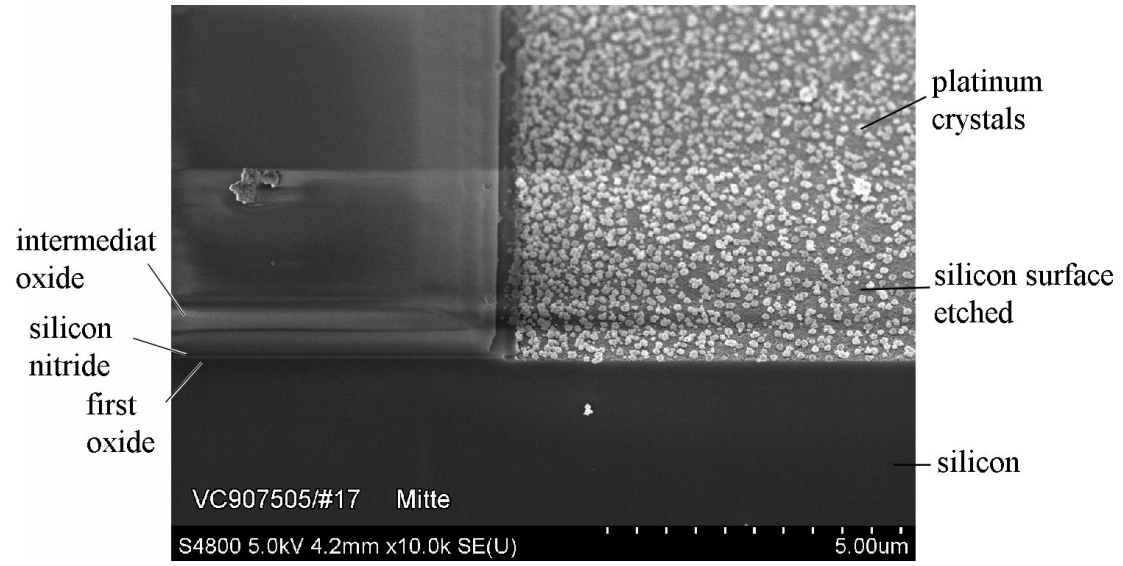

Figure 24 SEM picture of Infineon Emmcon diode, after the HF bath process, T = 70 °C, pH = 5,0, immersion duration = 10 min, Pt concentration in the bath ca. 0,0021 mol/l

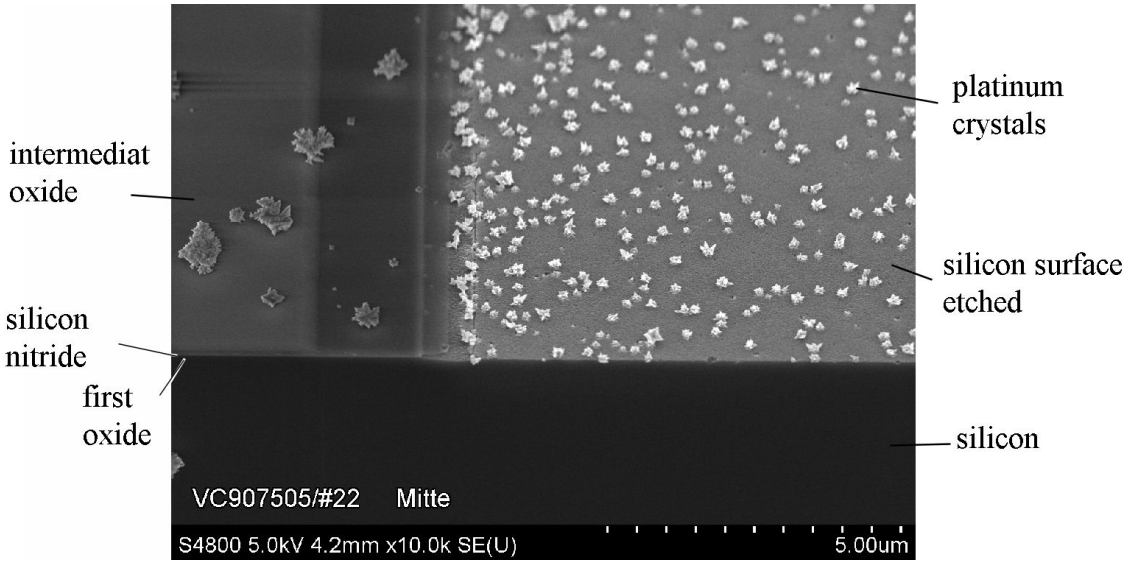

Figure 25 SEM picture of Infineon Emmcon diode, after the HF bath process, T = 70 °C, pH = 4,5, immersion duration = 10 min, Pt concentration in the bath ca. 0,0021 mol/l

To test the hydrazine process as ULSI application an Infineon developer machine was modified and a lot (VC917215) was tested with it. In the machine the wafers were rotated with 100 rpm for 3 minutes. At the same time the hydrazine and platinum solution was mixed and injected on the wafer with a syringe. Then the wafers were rotated with 200 rpm for 1 min. with a back side rinse of water. Then the rotation speed was increased to 2000 rpm for 1 min to dry the wafers. After that they were transferred over three hot plates at 60 °C for 1 min to dry them. Finally the wafers were ready for the next process step of the Infineon Emmcon diode. The concentration of the platinum and the hydrazine, which were applied on the wafer, were varied.

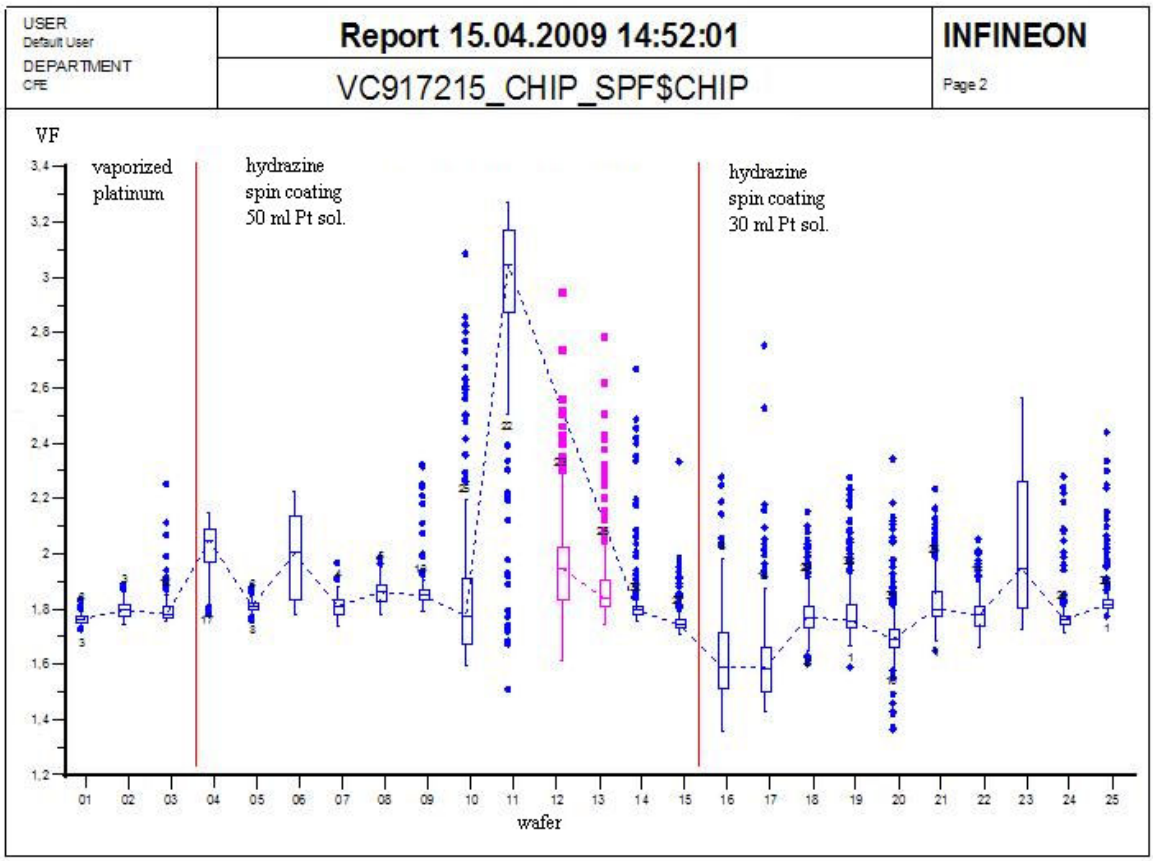

Figure 26 VF of a Infineon Emmcon diode, 01 to 03 vaporized platinum, 04 to 15 hydrazine spin coating process with 50 ml platinum solution (No. 4) and 50 ml hydrazine solution (No.1), 16 to 25 hydrazine spin coating process with 30 ml platinum solution (No. 4) and 20 ml hydrazine solution (No. 1)

Figure 26 shows the box plot diagram for VF of an Infineon Emmcon diode. On wafer 01 to 03 the platinum was vaporized on the wafer. On wafer 04 to 25 the platinum was deposited with the hydrazine spin coating process.

The vaporized wafers 01 to 03 have a VF of approximately 1,8 V, whereas a lot of wafers from 04 to 25 differ from this value. Only wafer 05, 07, 08, 09, 14, 15, 18, 19, 25 are inside the VF specification for the Infineon Emmcon diode.

During processing wafer 06 an equipment failure occurred, which is the reason for the high VF variation of the wafer. The second problem was that the platinum solution and the hydrazine solution were mixed in a beaker and sucked into a syringe and put on the wafer. The platinum particles and hydrazine leftovers in the beaker and syringe from the previous sequence caused a faster reduction of the platinum ions. The platinum precipitates in the beaker and the syringe instead on the wafer. This resulted in the very high VF variation of certain wafers. Thus a further lot, VC935747, was tested with the developer, where the platinum ions and the hydrazine were mixed direct on the wafer.

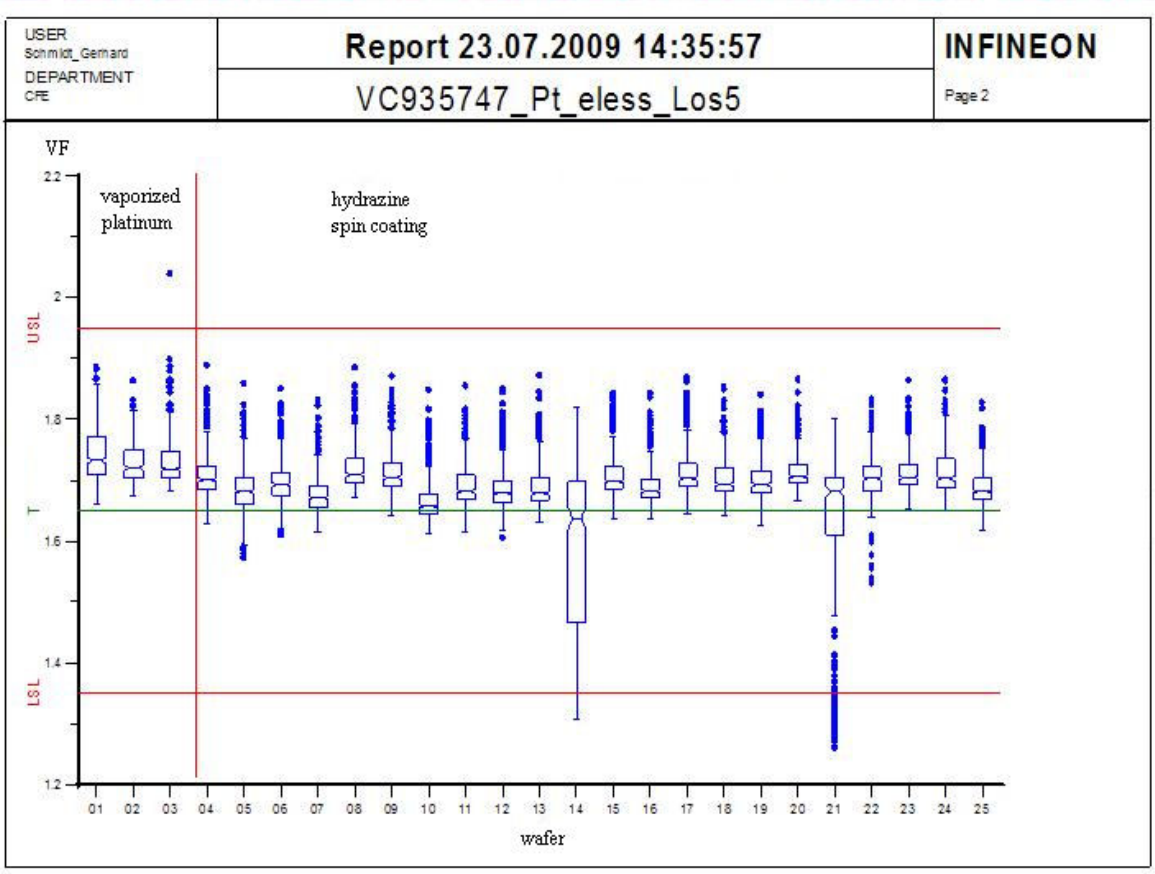

Figure 27 VF of a Infineon Emmcon diode, 01 to 03 vaporized platinum, 04 to 25 hydrazine spin coating process with 50 ml platinum solution (No. 1) and 50 ml diluted 1:10 hydrazine solution (No. 1)

Figure 27 displays the box plot diagram for VF of an Infineon Emmcon diode. On wafer 01 to 03 the platinum was vaporized on the wafer. On wafer 04 to 25 the platinum was deposited with the hydrazine spin coating process.

The vaporized wafers 01 to 03 have a VF of approximately 1,7 V with a low variation. Wafer 04 to 25 also have a VF of approximately 1,7 V with a low variation, except wafer 14 and 21. The outliners 14 and 21 were treated exactly in the same way as the rest of the lot and there is no obvious reason why they differ from the rest. This should be investigated in further experiments.

Lot VC935747 demonstrates that the hydrazine spin coating process is applicable in ultra-large scale integration.

The costs for usage of the hydrazine spin coating process in production were also estimated (see Chapter 4.5).

4.2.1. Comparison of vapor coating and hydrazine spin coating

The advantages of the hydrazine spin coating process are the following:
The process is easy to handle and no temperature or vacuum is needed.
Only the wafer is coated with platinum (the silicon contact hole and the silicon oxide mask), whereas in the vapor calotte the whole chamber is also vaporized with platinum.

There are also disadvantages of the hydrazine spin coating process namely:
As hydrazine may cause cancer, certain safety regulations have to be applied, when dealing with hydrazine.
The process is a single wafer process, whereas the vapor coating process is a batch process for 11 6-inch wafer or 8 8-inch wafer. But the process time of the hydrazine spin coating process is relatively short, which guarantees a high output.
The mixed solution is not stable. It has to be mixed immediately before injection on the wafer.

Points that are similar between the hydrazine spin coating process and the vapor coating process are:
The silicon dioxide is not etched.
The silicon is not etched or only marginal. [13]

4.3. Other Pt deposition processes

4.3.1. Ethylene glycol spin coating process

Hydrazine may cause cancer (R-phrase R45), therefore working with hydrazine means a health risk. In order to reduce these risks, alternative reducing agents were tested.

Skrabalak, et. al, showed the use of ethylene glycol as reducing agent. Ethylene glycol itself acts as reducing agent, but under temperature and oxygen (air) it reacts to glycolaldehyde, which acts as a primary reductant in polyol syntheses for noble metals. [22]

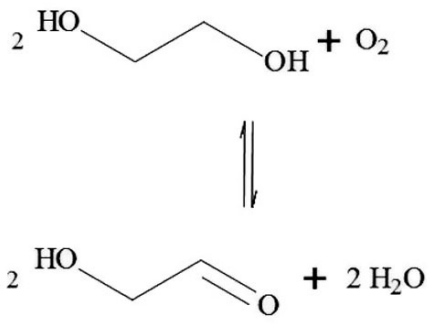

Figure 28 Oxidation of ethylene glycol to glycolaldehyde

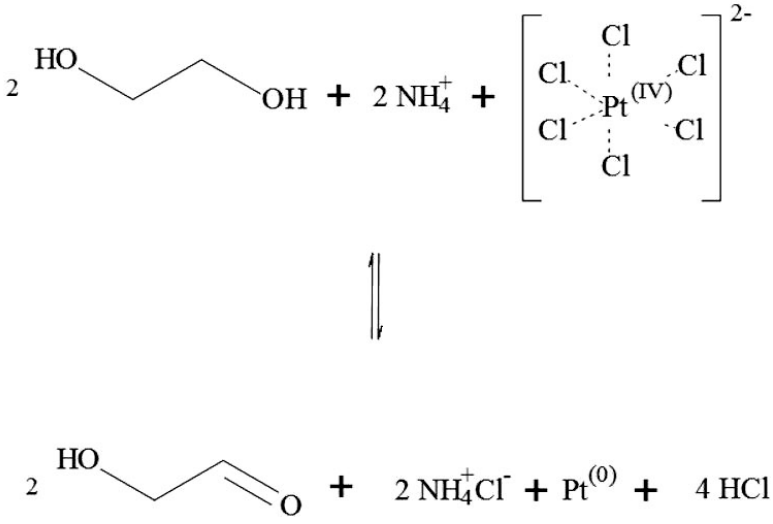

Figure 29 Reduction of platinum with ethylene glycol as reducing agent

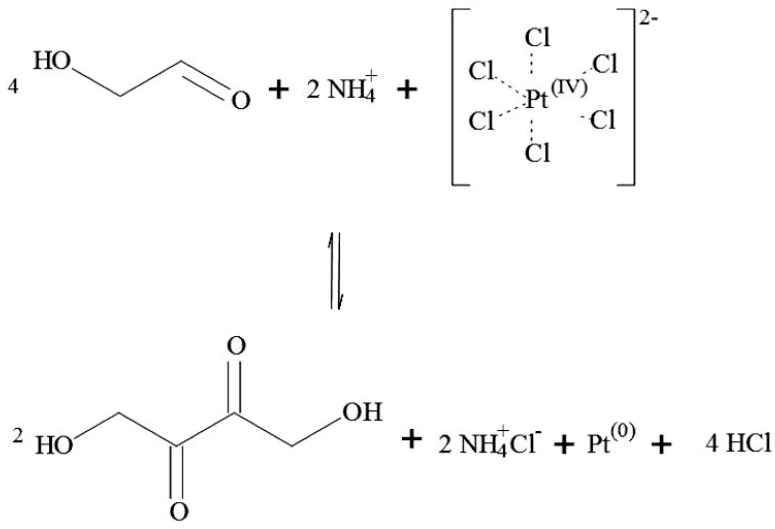

Figure 30 Reduction of platinum with glycolaldehyde as reducing agent

In contrast to hydrazine, ethylene glycol and glycolaldehyde are not carcinogenic. Thus a coating bath with ethylene glycol and an ethylene glycol spin coating process were tested.

The bath with ethylene glycol has the same problem as the hydrazine bath. The platinum ions were reduced in the solution and the bath turned black. Little platinum was deposited on the wafer.

The ethylene glycol spin coating process was processable, but only little platinum was deposited on the wafer.

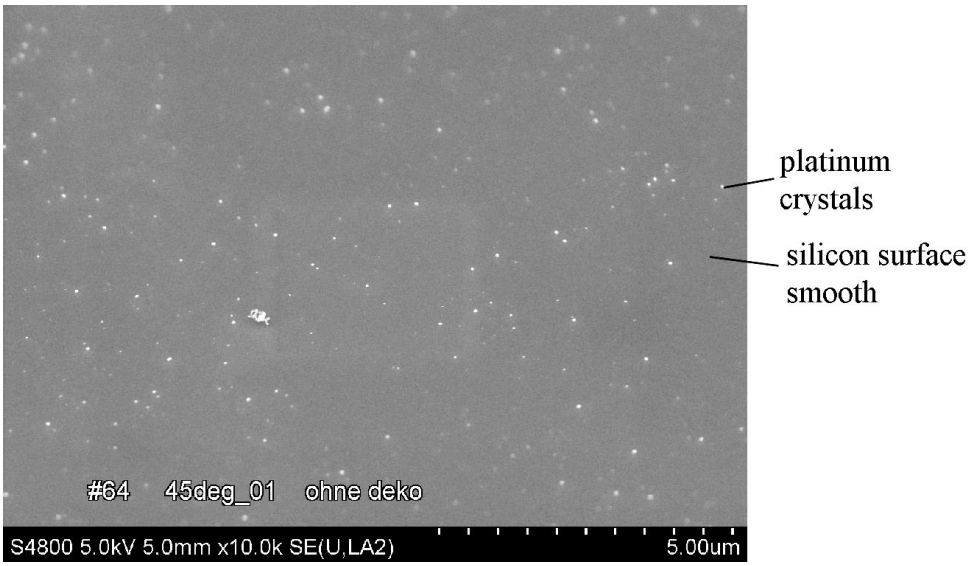

Figure 31 SEM picture of a silicon wafer (silicon material 1) after the ethylene glycol spin coating process

The SEM picture presents a wafer after the ethylene glycol spin coating process. Very little platinum were deposited. One reason for that may be that the wafer only had room temperature during the process. To produce glycolaldehyde, the ethylene glycol was heated up to 100 °C. The solution is mixed with the heated platinum solution, containing solved ammonium hexachloroplatinate in water. The mixed solution was dispensed on the rotating wafer. The spinning equipment has not the possibility to heat the wafer, so the wafer only had room temperature. In further experiments a heated wafer should be used to ensure the proper temperature for the reaction.

4.3.2. Palladium as catalytic precursor layer

A lot of electrochemical deposition methods use a catalytic precursor layer for the deposition of the metal. Infineon uses a palladium layer for the electrochemical deposition of nickel and nickel molybdenum alloys. Palladium has similar chemical properties as platinum, thus it was tested as catalytic layer (see Chapter "Experimental").

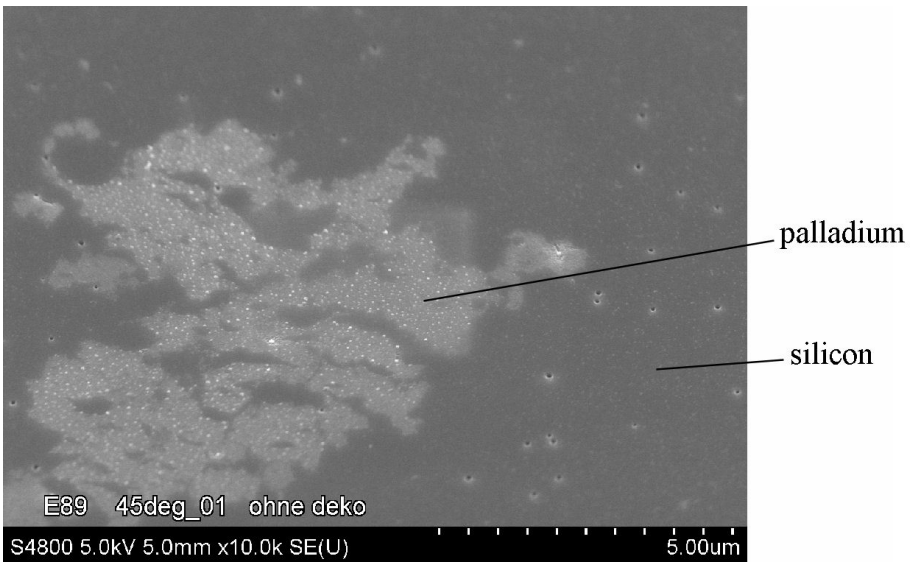

Figure 32 SEM picture of a silicon wafer (silicon material 1) with deposited palladium (as precursor)

The SEM picture (Figure 32) displays a wafer with a deposited palladium layer. The white light grey spots are palladium. The dark grey areas are silicon.

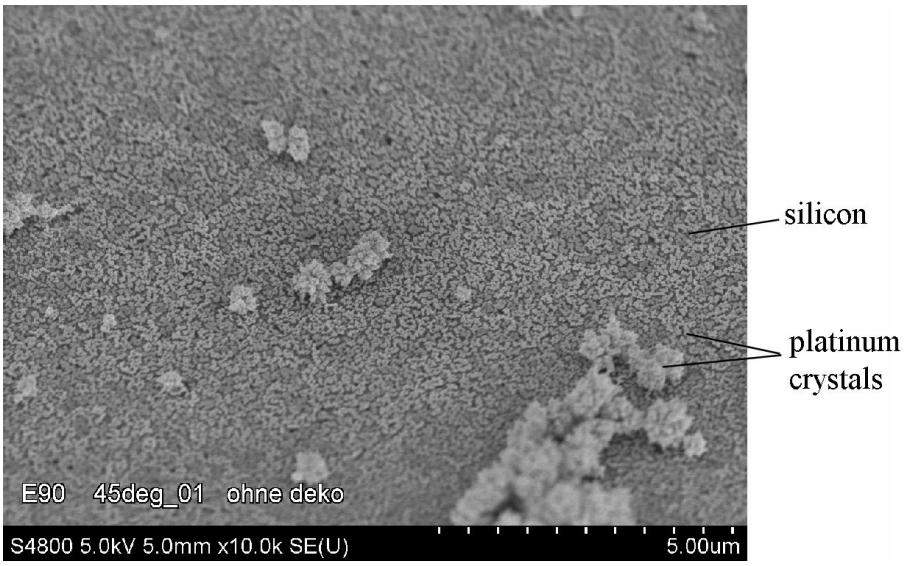

Figure 33 SEM picture of a silicon wafer (silicon material 1) with deposited palladium as precursor and deposited platinum on it with the HF bath process

The SEM picture displays the palladium precursor and deposited platinum on the palladium layer with the HF bath process.

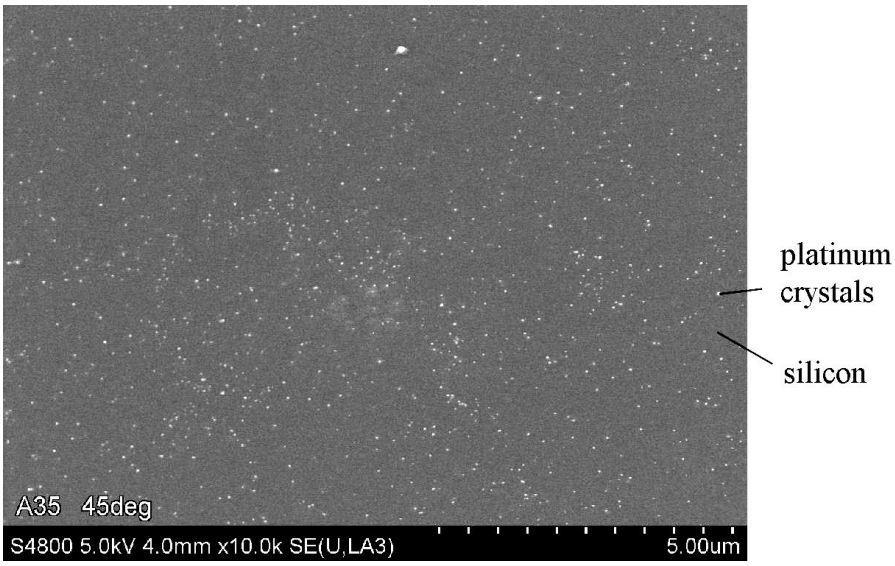

Figure 34 SEM picture of a wafer (silicon material 2) with deposited palladium as precursor and deposited platinum on it with the hydrazine spin coating process

The SEM picture displays the palladium precursor and deposited platinum on the palladium layer with the hydrazine spin coating process.

The palladium does not improve the deposition of platinum significantly, which is why a palladium precursor layer was not used in further experiments.

4.3.3. Spin coating process with platinum acetylacetonate

Zhang, et. al., deposited platinum on silicon by using a spin coating process with platinum acetylacetonate. They dissolved platinum acetylacetonate in chloroform and injected it on a silicon wafer. The wafer was radiated with UV light at 172 nm with a high intensity. The platinum layer was used as reactive site for electroless copper plating. [28]

Unfortunately, the only available UV light lamps have got a wavelength of 254 nm and 366 nm with a power of 6 W per lamp. This energy was too low to decompose the platinum acetylacetonate.

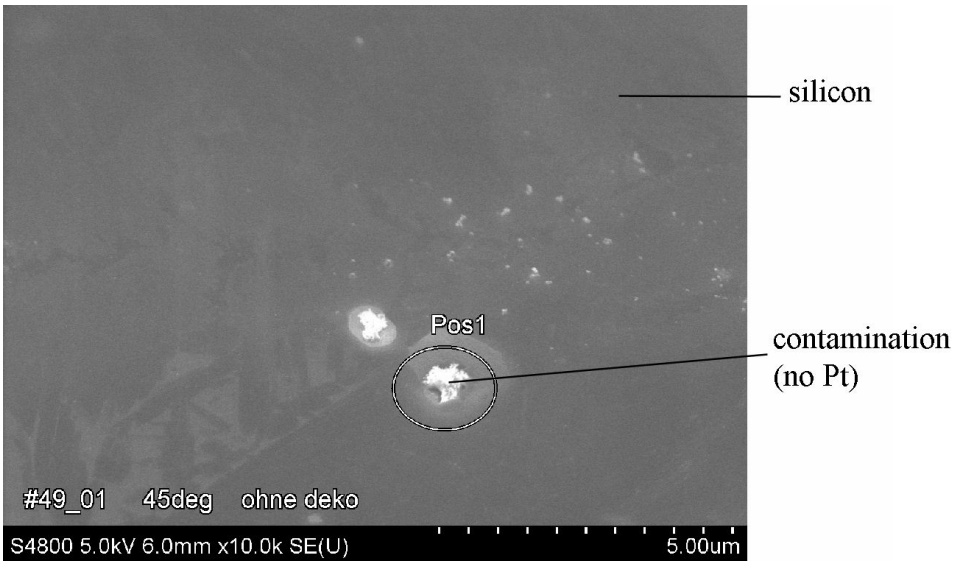

Figure 35 SEM picture of a wafer (silicon material 1) after the spin coating experiment with platinum acetylacetonate

The SEM picture shows a silicon wafer after the spin coating experiment with platinum acetylacetonate. No platinum was deposited on the silicon.

4.4. Analyzing Platinum

In the initial experiments the HF bath and the hydrazine spin coating process showed the most promising results, therefore these processes were chosen for further experiments.
The crucial step was to find an easy and cheap method to analyze the deposited platinum layer in order to identify the quantity, form and nature of the platinum on the silicon: is it pure platinum or a platinum complex, is it a homogenous layer or several crystal islands. Further, an analyzing method should explain or rather measure the electrical parameters of the device.

Microscopic pictures of blank silicon pieces after the deposition process only show a black layer, but do not deliver information of the nature of the layer: is it pure platinum or a platinum complex, is it a homogenous layer or several crystal islands. It does not allow estimating the quantity of the deposited platinum.

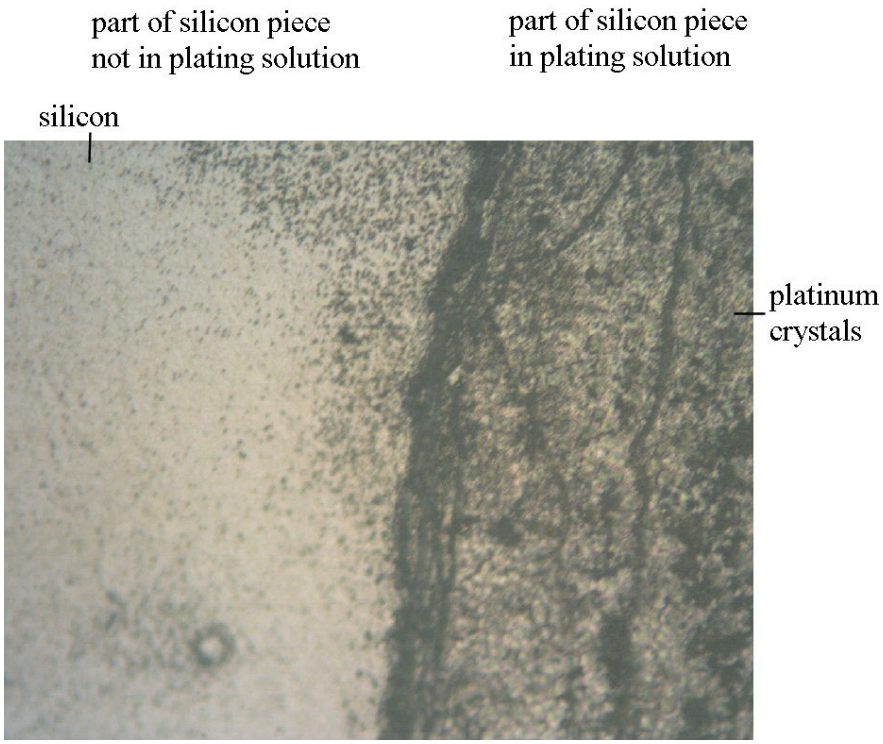

Figure 36 Microscopic picture of silicon (wafer material 1) with a deposited platinum layer, the platinum was deposited with the HF bath process, front side, 20x magnification. On the left side of the picture the silicon piece was not in plating solution, but it was on the right side.

In order to analyze the deposited black substance, a wafer piece with the black precipitate was immersed in aqua regia ($HCl:HNO_3$ = 3:1). The black precipitate was dissolved and the solution analyzed with the ICP-MS (inductive coupled plasma mass spectroscopy). The measurement displays 1,075 . 10^3 ppb (parts per billion) platinum, which results in 2,28 mg platinum on the wafer piece. This results in a theoretical layer thickness of approximately 17,3 nm. SEM pictures show that the platinum is deposited in crystal spheres instead of a homogenous layer.

The next logical step was to look at the pieces with a scanning electron microscope (SEM). The SEM pictures provide information about the form of the layer and allow an estimation of the platinum quantity. They do not allow however, an exact measurement of the amount of

platinum on the surface. It is also not possible to answer the question whether it is pure platinum or a platinum complex or if there are a lot of impurities in the layer.

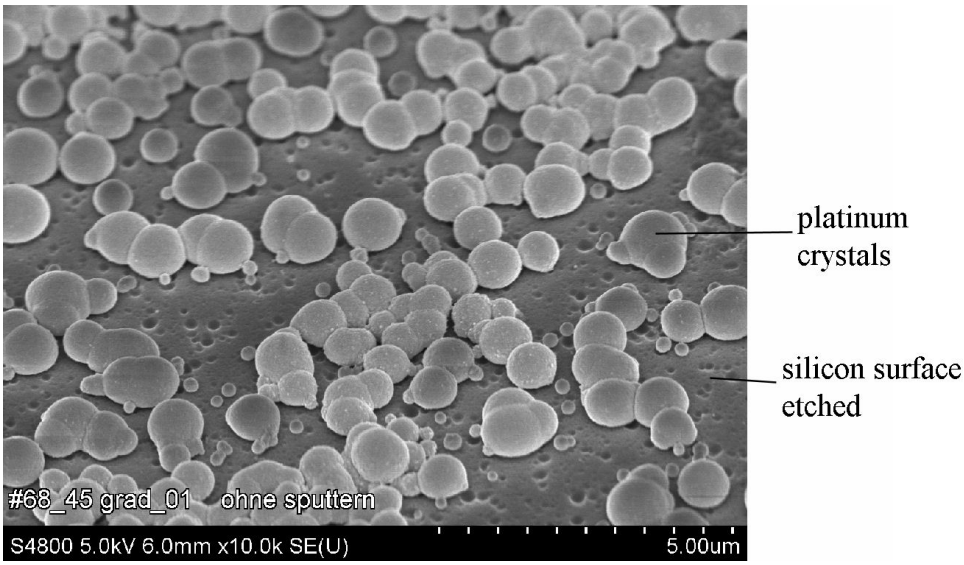

Figure 37 SEM of a silicon piece (wafer material 1) after the HF bath process, T = 70 °C, pH = 4,5, immersion duration = 30 min., Pt concentration in the bath ca. 0,0026 mol/l, the white spheres are platinum grains

The SEM picture presents that with the HF bath process, the platinum is deposited in crystal spheres instead of a homogenous layer. It further shows that the silicon surface is affected by the process. The principle of the process is a displacement reaction, silicon is oxidized and dissolved, whereas platinum is reduced and deposited on the surface.

To clarify whether the spheres are pure platinum or a platinum complex, a sample was sent to the FELMI laboratory of Graz University of Technology for further analysis. The FELMI laboratory cut through a sphere and took various transmission electron microscope (TEM) pictures and analyzed the sphere. The sphere was tested with EELS and EFTEM on various ligands (N, C, O, etc.). The sphere consists of over 98% pure platinum.

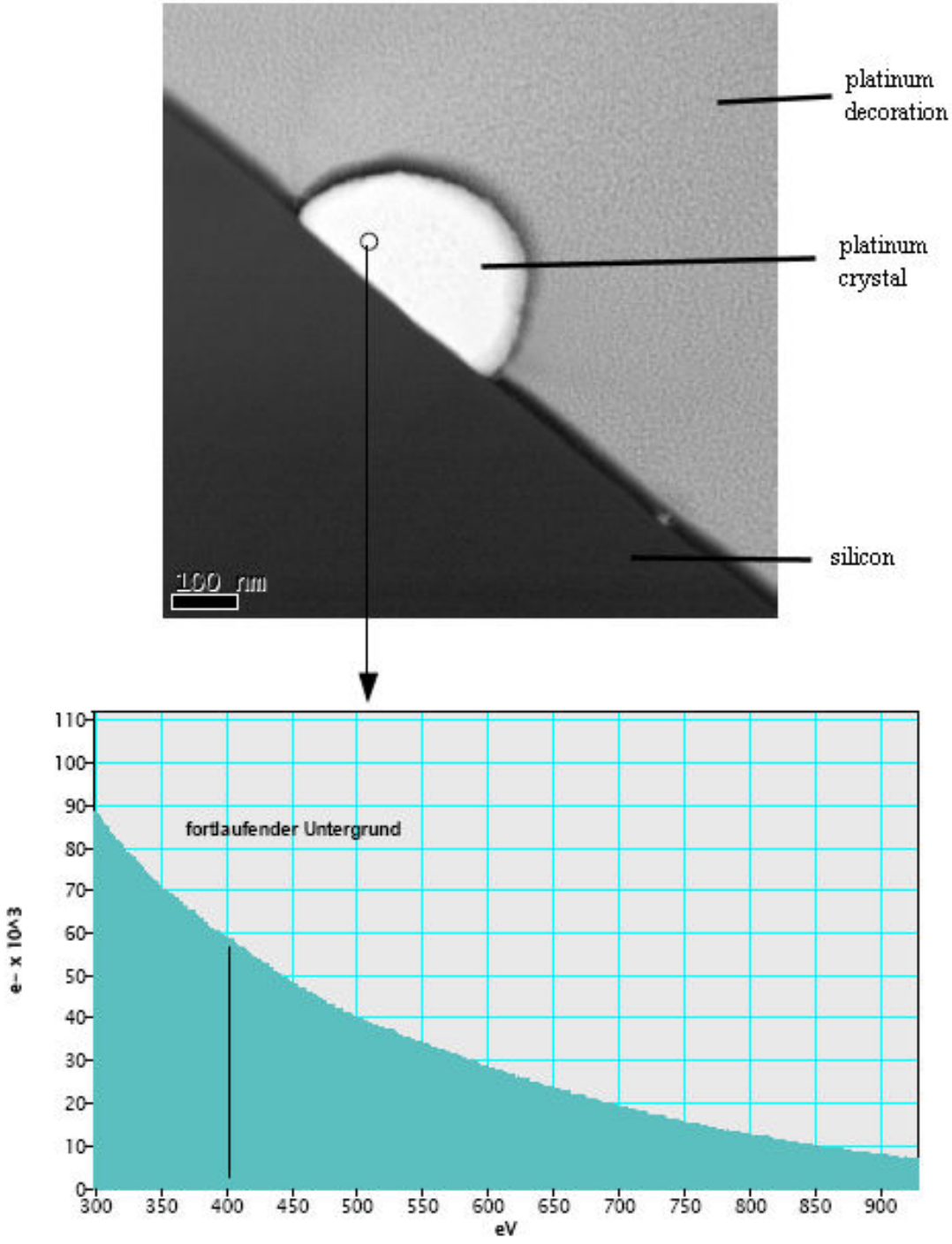

Figure 38 Top: TEM picture of a crystal sphere. Below: EELS of the crystal sphere

The EELS displays that there is no nitrogen in the crystals sphere. This proves that the sphere is not a platinum nitrogen complex. Ammonium is the counter ion of the platinum salt. Ammoniac or TMAH is in the plating solution to regulate the pH value.

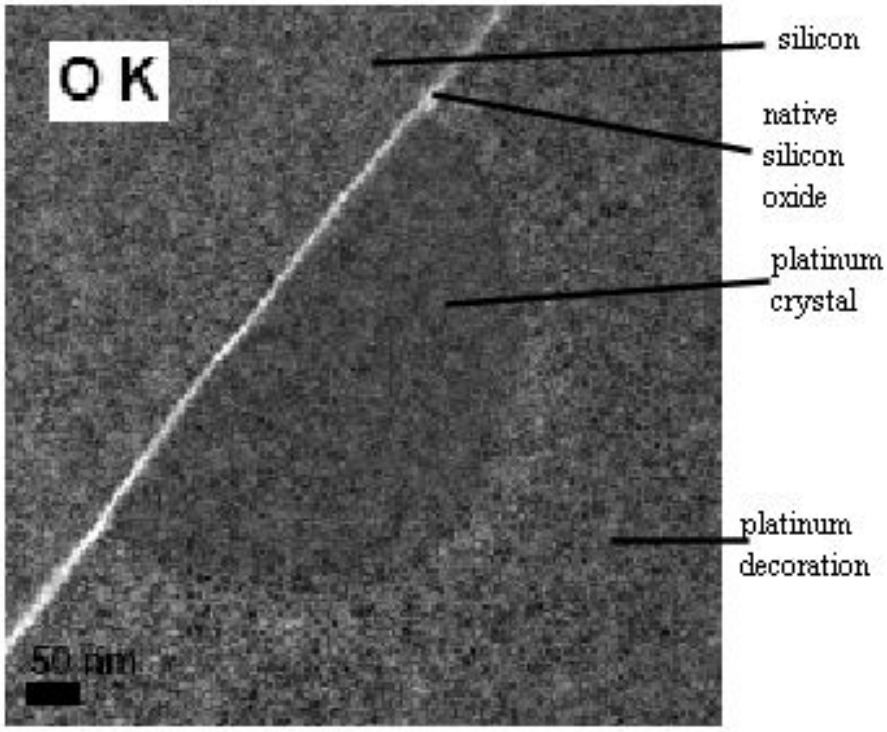

Figure 39 EFTEM picture shows the oxygen (white line)

The EFTEM picture demonstrates that there is no oxygen in the sphere. A thin layer of oxygen is on the silicon surface, shown by a white line, the native silicon oxide.

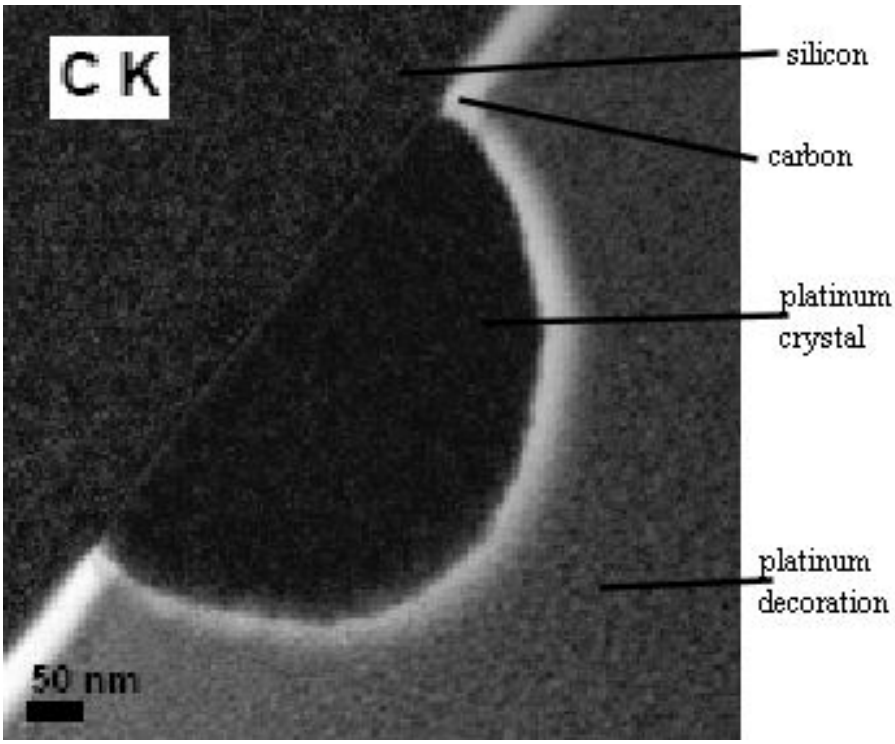

Figure 40 EFTEM picture shows the carbon (white line)

The EFTEM picture presents that there is no carbon in the sphere. A thin layer of carbon is on the silicon surface and the surface of the platinum sphere, shown by the white line. This carbon comes from the sample preparation.

The most important thing is that the finished diode fulfils certain electrical parameters. One important parameter is the forward voltage (VF), which depends on the charge carrier life time in the semi conductor device. The charge carrier life time is direct proportional to the charge carrier diffusion length. That is why a measurement of the charge carrier diffusion length of platinum silicide in silicon should answer the question of forward voltage. All impurities, e.g. iron, sodium, etc., which diffuse in the silicon wafer have an influence on the diffusion length. It was assumed that there are very few impurities and the main effect on the diffusion length is from the diffused platinum.

Silicon wafers with a platinum silicide in it were measured with Elymat and SDI. Both equipments measure the diffusion length of charge carriers. A platinum layer was created through different processes (HF bath, hydrazine spin coating, vaporize Pt, ethylene spin

coating, etc.), a platinum silicide formed at 400 °C, the excessive platinum removed with aqua regia and the platinum silicide diffused at ca. 850 °C. The diffused wafers were measured with Elymat and SDI and the results of the charge carrier diffusion length were compared with each other. Both measurement equipments do not deliver conclusive results.

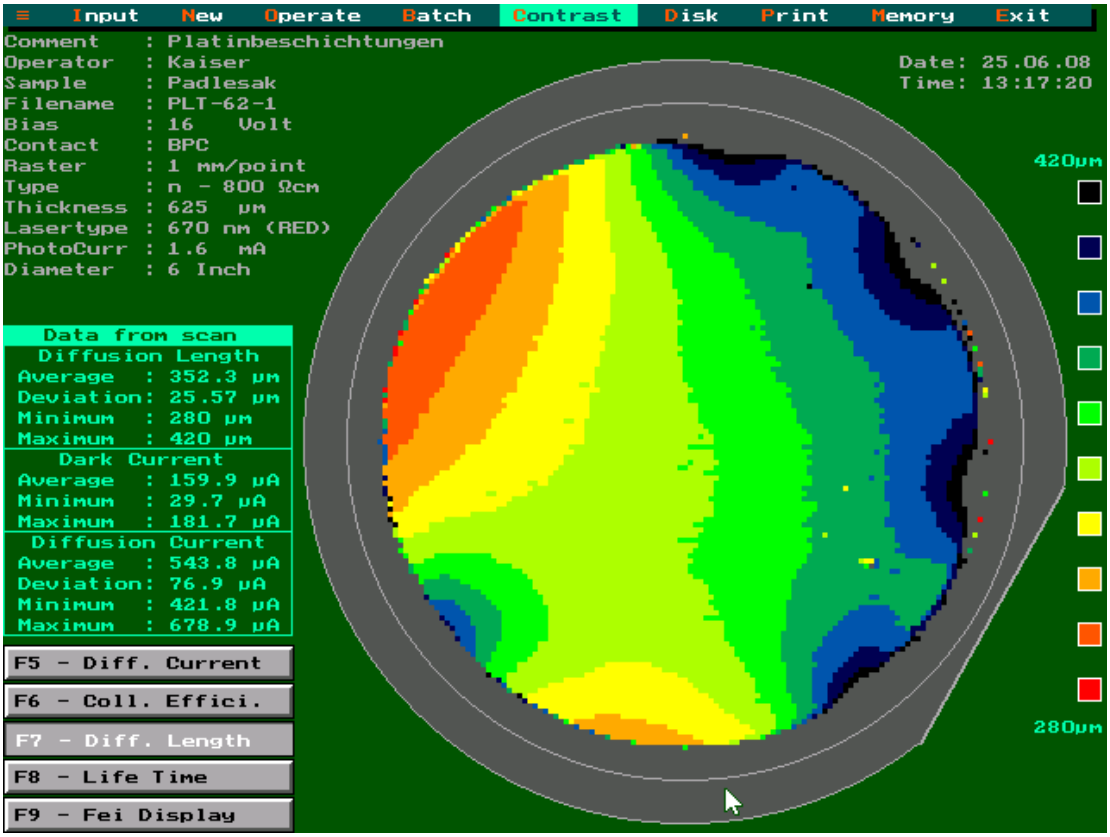

Figure 41 Elymat, diffusion length of a blank silicon wafer (wafer material 1)

The Elymat measurement of a blank silicon wafer shows the diffusion length range from 280 – 420 µm and is not homogenous over the wafer. Based on the design of the Elymat, the rim of the wafer is not measured. The colors for the different diffusion length ranges are chosen arbitrarily by the Elymat, so it is important to pay more attention to the values than to the colors in order to receive a correct interpretation of a measurement.

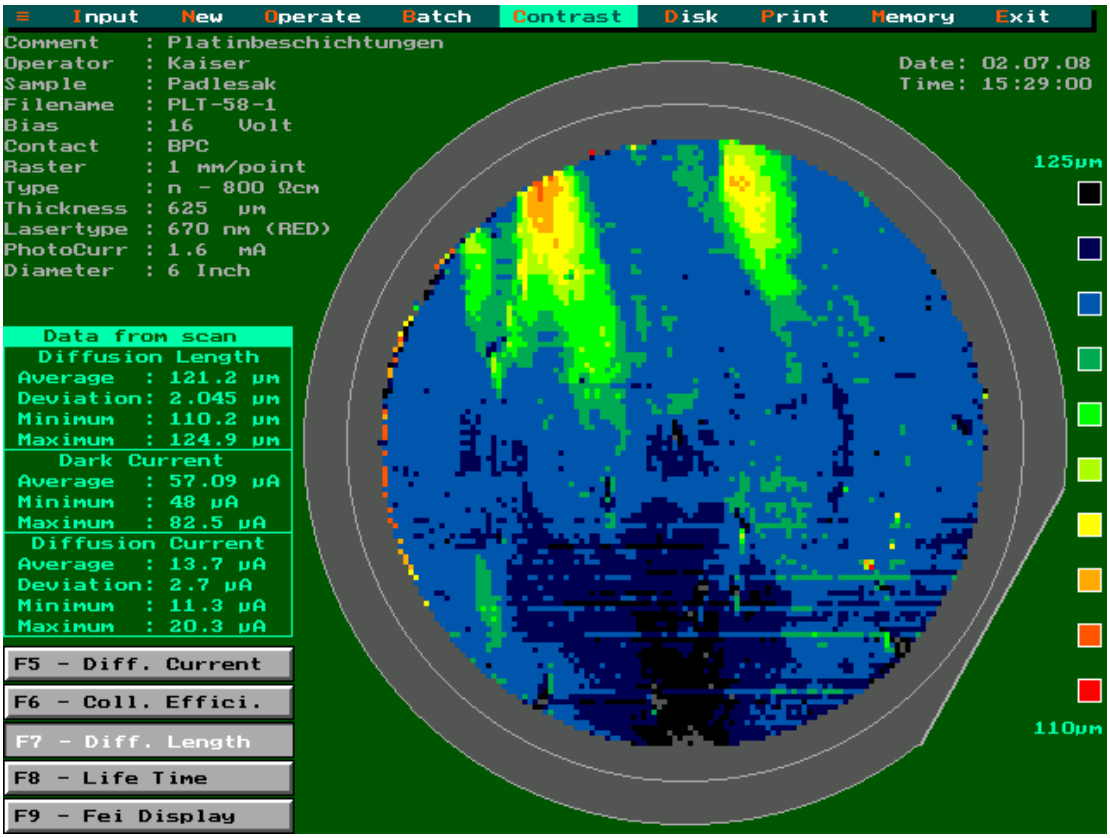

Figure 42 Elymat, diffusion length of a silicon wafer (wafer material 1) with diffused platinum in it. The Pt was vaporized on the wafer.

The Elymat measurement shows a silicon wafer in which platinum was diffused. The platinum was vaporized on the wafer, siliconized and diffused in a furnace. The diffusion length ranges from 110 to 125 µm and is nearly homogenous dispensed over the wafer. In comparison the diffusion length of the blank wafer material has got a diffusion length range from 280 to 420 µm and is not homogenous over the wafer. The result of the vaporized wafer is taken as a reference for the other platinum deposition processes.

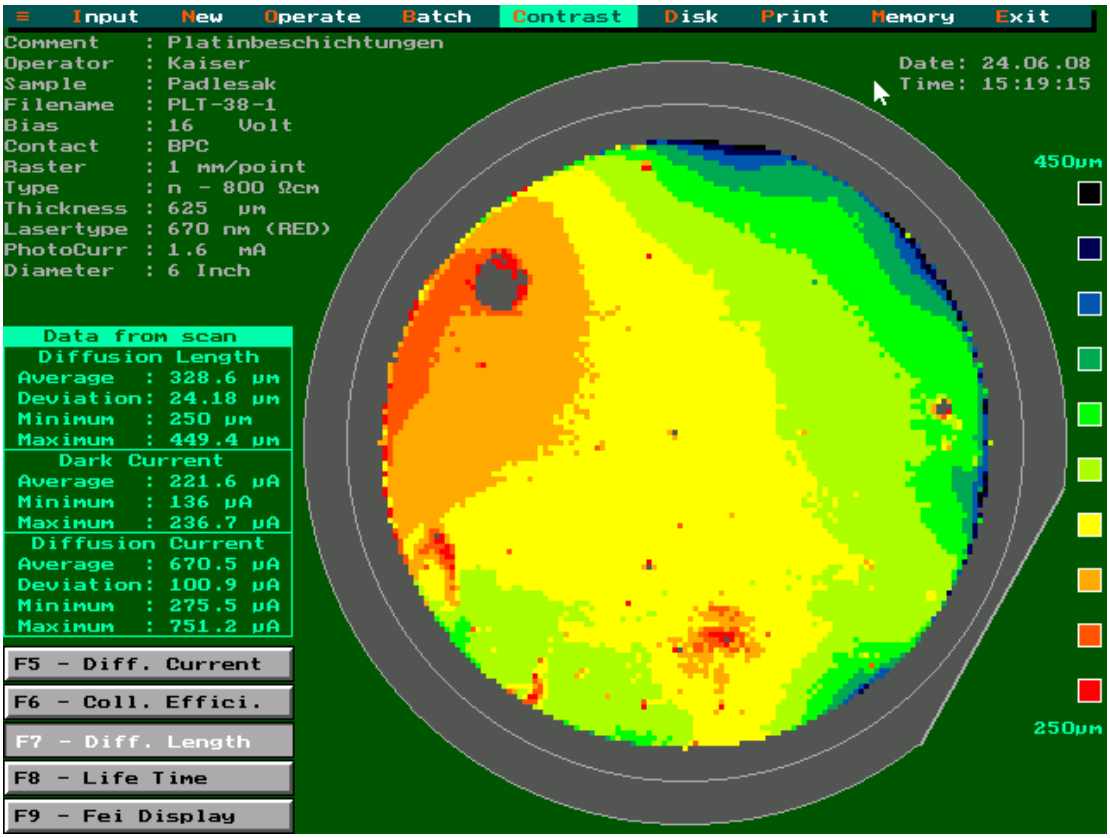

Figure 43 Elymat, diffusion length of a silicon wafer with diffused platinum in it. The Pt was deposited with a HF bath on the wafer

The Elymat measurement displays a silicon wafer in which platinum was diffused. The platinum was deposited on the wafer by electroless chemical deposition in a HF bath, siliconized and diffused in a furnace. The diffusion length range from 250 to 450 µm and is not homogenous dispensed over the wafer. It does not differ significantly from the measurement of the blank wafer. One reason for the high diffusion length is that too few platinum was deposited on the wafer. Another reason might be a problem with the following processes (siliconize, aqua regia, diffusion).

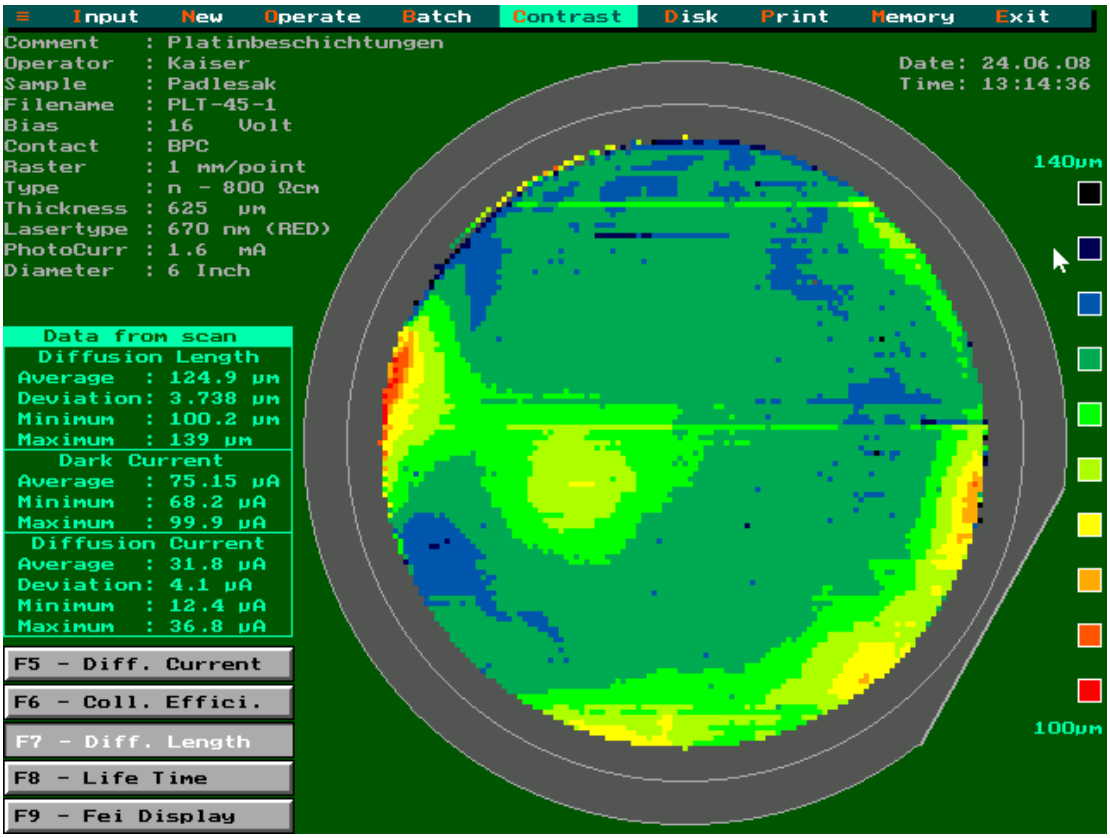

Figure 44 Elymat, diffusion length of a silicon wafer with diffused platinum in it. The Pt was deposited with the hydrazine spin coating process on the wafer

The Elymat measurement demonstrates a silicon wafer in which platinum was diffused. The platinum was deposited on the wafer by electroless chemical deposition with the hydrazine spin coating process and siliconized and diffused in a furnace. The diffusion length ranges from 100 to 140 µm and is nearly homogenous dispensed over the wafer. The result is comparable with the result of the vaporized wafer, which is why the hydrazine spin coating process is promising for future applications.

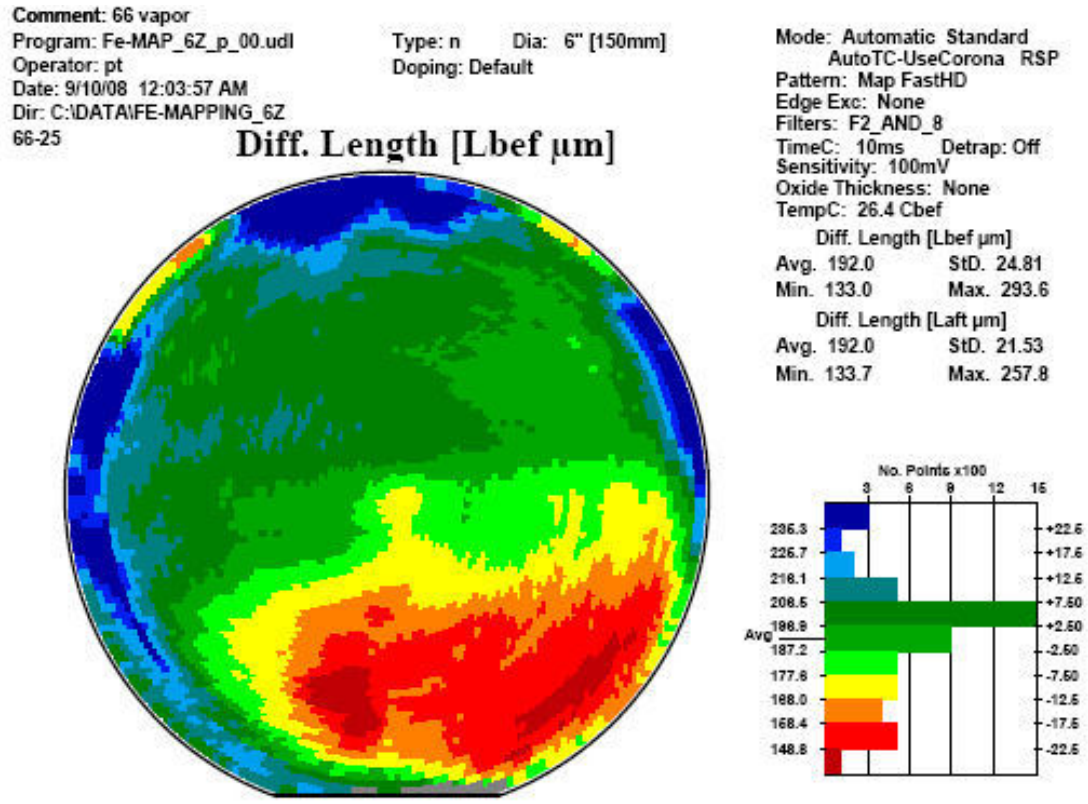

Figure 45 SDI, diffusion length of a silicon wafer (wafer material 1) with diffused platinum in it. The Pt was vaporized on the wafer.

The SDI measurement presents a silicon wafer in which platinum was diffused. The platinum was vaporized on the wafer, siliconized and diffused in a furnace. The diffusion length ranges from approximately 150 to 250 µm and is relatively homogenous dispensed over the wafer. This result is taken as a reference for the other platinum deposition processes.

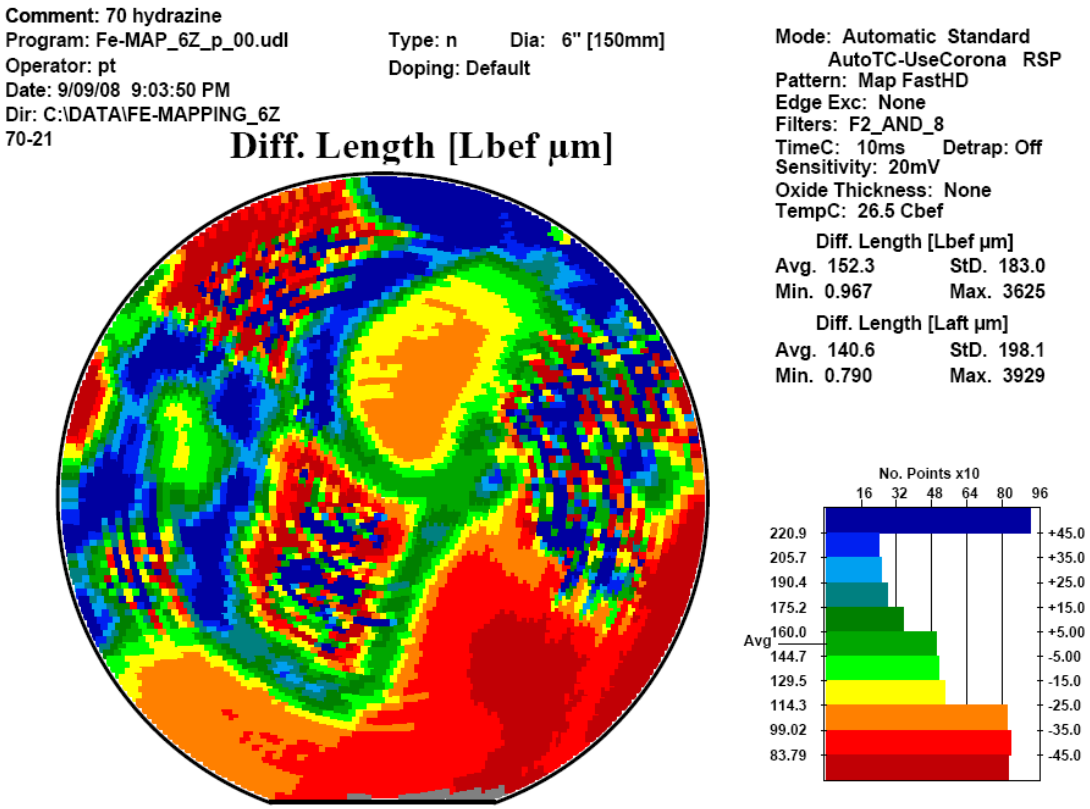

Figure 46 SDI, diffusion length of a silicon wafer (wafer material 1) with diffused platinum in it. The Pt was deposited with the hydrazine spin coating process on the wafer

The SDI measurement shows a silicon wafer in which platinum was diffused. The platinum was deposited on the wafer by electroless chemical deposition with the hydrazine spin coating process, siliconized and diffused in a furnace. The diffusion length ranges from approximately 80 to 220 µm and is blotchy dispensed over the wafer. The result differs from the result of the vaporized wafer. The width of the diffusion length range is higher and the not as homogenous dispensed on the wafer. The diffusion length is generally shorter, which indicates that more platinum got diffused into the silicon.

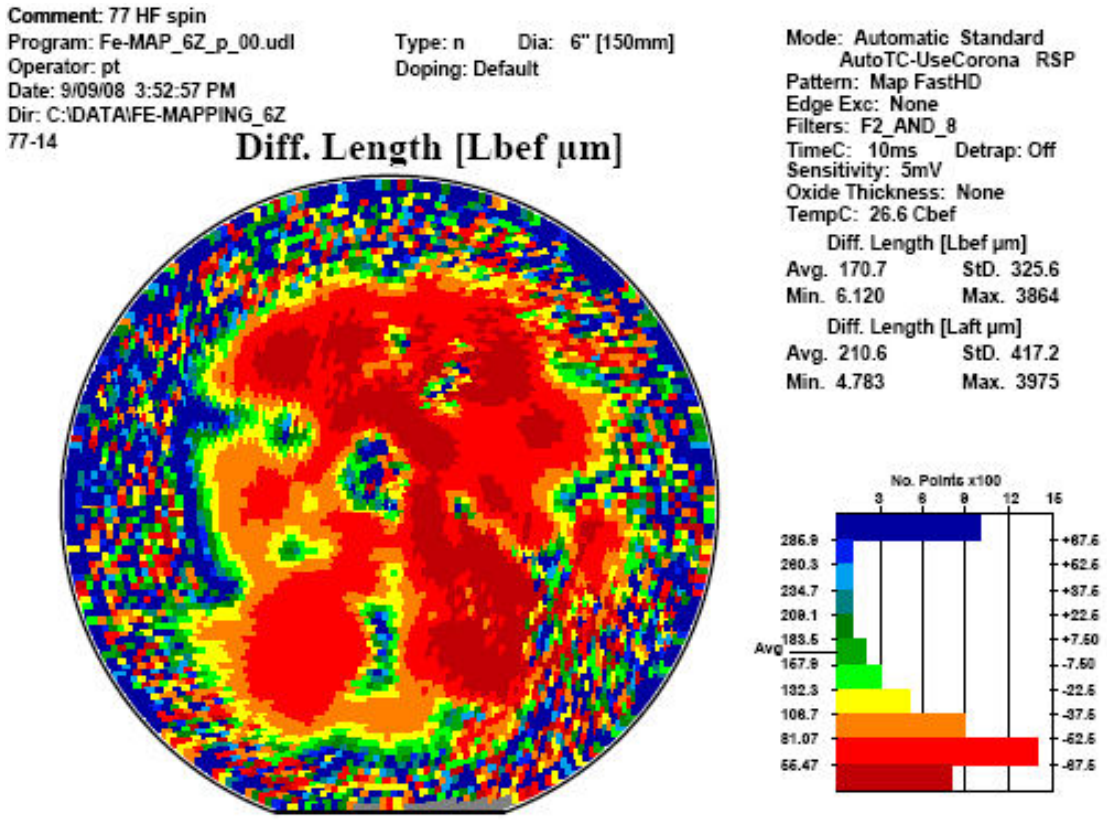

Figure 47 SDI, diffusion length of a silicon wafer (wafer material 1) with diffused platinum in it. The Pt was deposited with a HF spin coating process on the wafer

The SDI measurement displays a silicon wafer in which platinum was diffused. The platinum was deposited on the wafer by electroless chemical deposition with a HF spin coating process, siliconized and diffused in a furnace. The diffusion length range from approximately 50 to 290 µm and is blotchy dispensed over the wafer. The result differs from the result of the vaporized wafer, but the diffusion range is comparable to the hydrazine spin coating wafer, however with an other dispense pattern.

The SDI measurements are not comparable to the Elymat measurements. A reason for that could be that both measurements are optimized for p-doped wafers and not n-doped, thus the measurements are close to the detectorlimit. The wafers have a high resistivity (800-1600 Ohm.cm), therefore the measured current is relatively low and not significant over the signal noise ratio.

The best analyzing method to get dependable results is to process a development lot of the diodes and measure the electrical parameters. The disadvantages are high costs, high response time (a whole lot must be processed before it can be measured) and multiple possibilities for errors. There are other factors, which influence the forward current beside the platinum concentration in the wafer. These factors result from other operation steps in the fabrication of the device. That is why an electrical behavior from the required specification has got more reasons than just the platinum deposition.

A development lot of the Infineon Emcon diode was used to test the different platinum deposition processes and to compare the electrical parameters of the finished processed diodes with each other.
The lot was split as followed:
Three wafers with the vaporize process (the reference method)
Three wafers with the HF bath process
Three wafers with the hydrazine spin coating process
Three wafers with the ethylene glycol spin coating process.

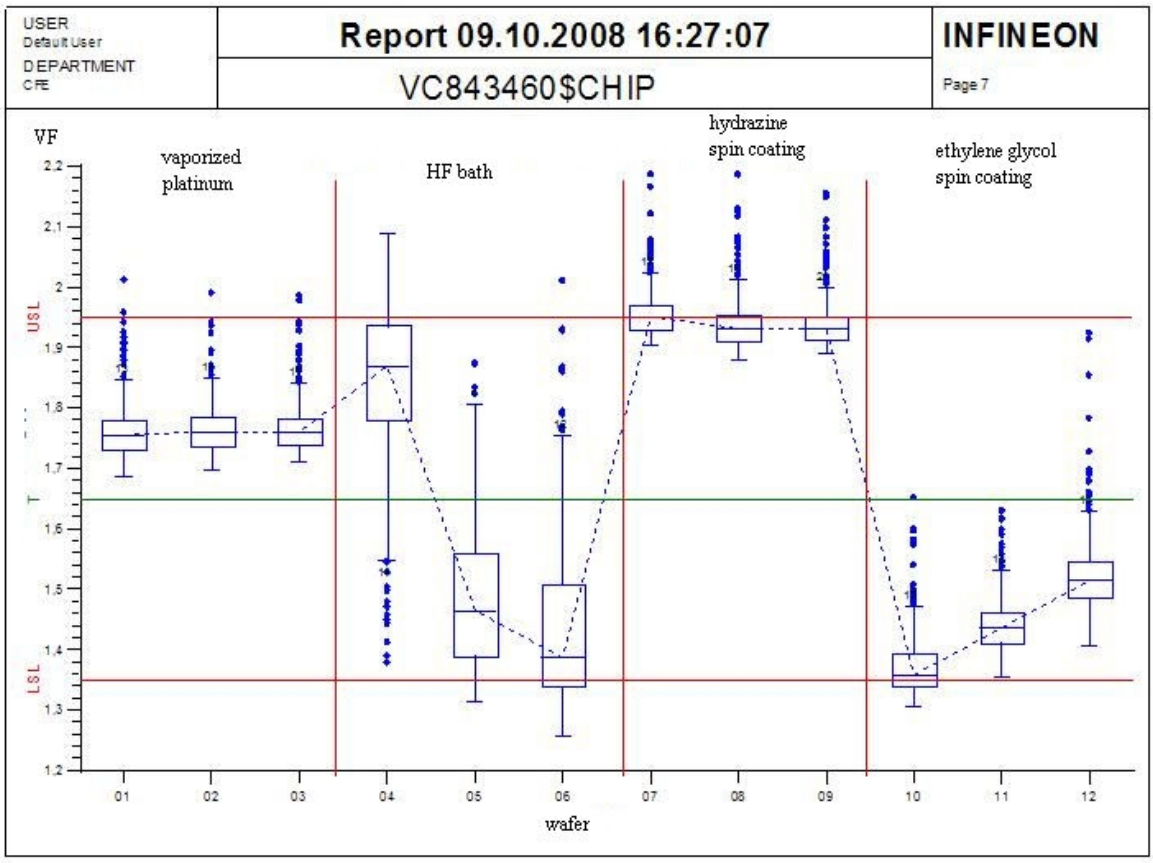

Figure 48 VF of a Infineon Emmcon diode, 01 to 03 vaporized platinum, 04 to 06 HF bath process, 07 to 09 hydrazine spin coating process, 10 to 12 ethylene glycol spin coating process

Wafers 01 to 03 all show the desired result of 1,7 V. Wafers 07 to 09 have a higher value of 1,9 V. It is possible to change this value with a different diffusion temperature. This was tested with a further development lot. The forward voltage of wafers 04 to 06 and 10 to 12 are too low and do not fulfill the requirements for the device.

This result proves that the hydrazine spin coating process appears promising to displace the vapor process.

Another method to measure electrically active defects, known as traps, in semiconductors is the Deep Level Transient Spectroscopy (DLTS) measurement. DLTS measurements were taken by Mathias Rommel of Fraunhofer institute in Erlangen. Infineon Emmcon diodes were prepared as follows: The top layers were removed from the silicon. Gold was vaporized through a mask to enable Schottky-contacts. For the backside contact an indium-gallium-silicon eutectic was established on the backside of the device.

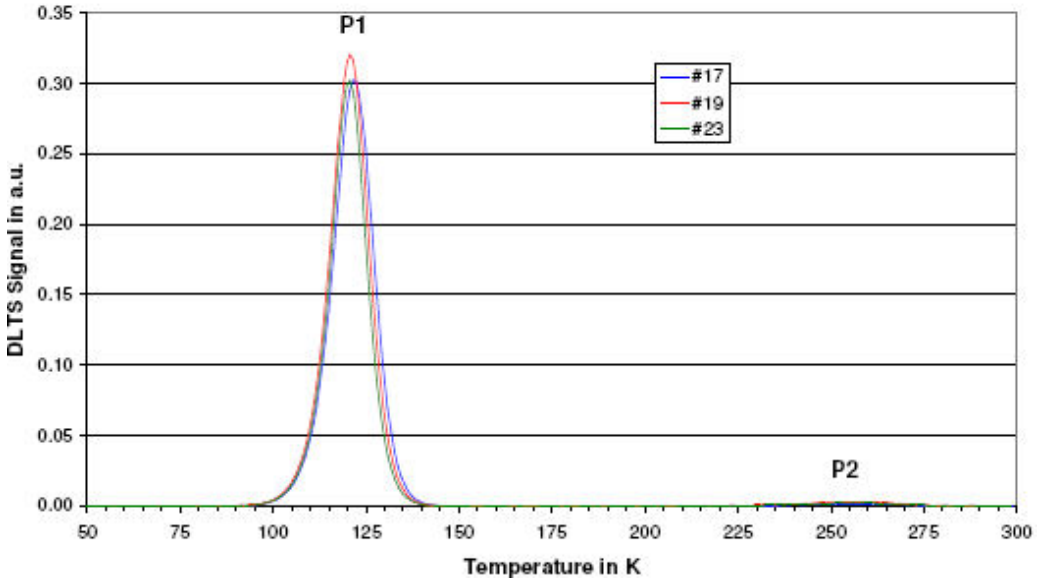

Figure 49 DLTS-tempraturescan for a period width of Tw = 20,48 ms and reverse voltage VR = -5 V, #17 Emmcon diode with vaporized platinum (reference process), #19 Emmcon diode with platinum deposited only on the backside with HF bath process, #23 Emmcon diode with platinum deposited with the hydrazine spin coating process.

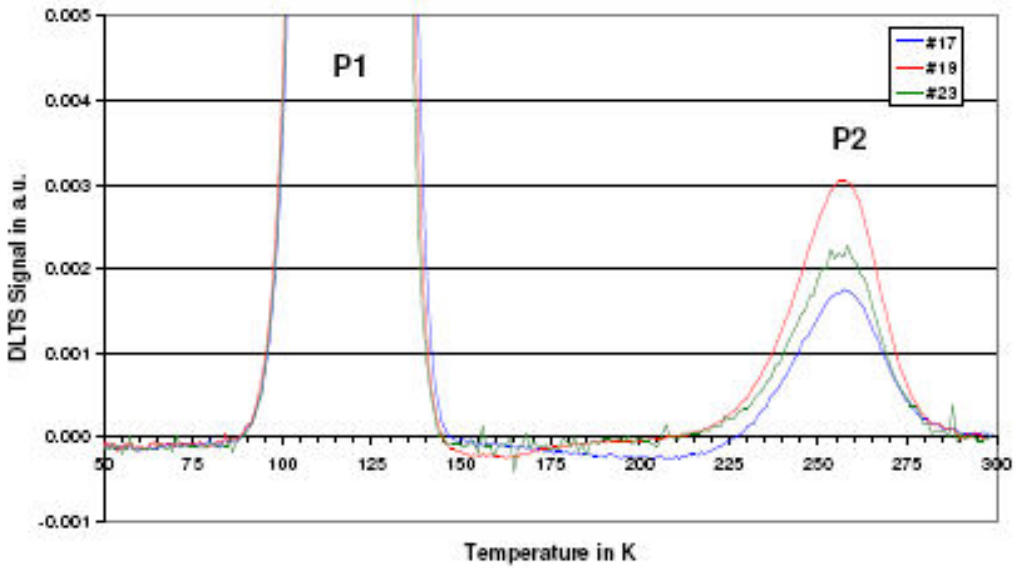

Figure 50 DLTS-tempraturescan for a period width of Tw = 20,48 ms and reverse voltage VR = -5 V, #17 Emmcon diode with vaporized platinum (reference process), #19 Emmcon diode with platinum deposited only on the backside with HF bath process, #23 Emmcon diode with platinum deposited with the hydrazine spin coating process.

The pictures display DLTS-tempraturescans of three Infineon Emmcon diodes. Sample 17 is a diode with vaporized platinum (reference process). Sample 19 is a diode with platinum deposited only on the backside with the HF bath process. Sample 23 is a diode with platinum deposited with the hydrazine spin coating process. The doping concentration in silicon of sample 17 is approximately 1,7 . 10^{13} cm^{-3}. For sample 19 and 23 it is approximately 2,0 . 10^{13} cm^{-3}. The peak P1 associates with an energy level of approximately E_C = -0,23 eV, which refers to the Fermi level of platinum. The smaller peak P2 associates with a energy level from approximately E_C = -0,53 eV to approximately E_C = -0,55 eV, which refers to the Fermi level of PtH. (Literature E_C = -0,50 eV)

The sample preparation for a DLTS measurement is quite extensive, thus the analyzing costs are very high. That is why no further DLTS measurements were taken for this thesis.

Analyzing the platinum concentration on the silicon wafer after electrochemical deposition and analyzing the platinum concentration in the silicon wafer after diffusion was a major challenge for this thesis. To take SEM pictures to estimate the platinum concentration after e-less deposition has emerged to be the most effective method. The only definite method to determine the platinum concentration after diffusion respectively the influence on the forward voltage, is to process a development lot and measure the electrical parameters.

4.5. Costs of the HF bath process and the hydrazine spin coating process

Infineon calculates by using the Infineon Toolbox for the platinum vapor coating process 3,50 Euro for each 6-inch wafer.

The Infineon Toolbox estimates:
The costs of a developer are approximately 0,70 Euros for each 6-inch wafer.
To put on a 1,5 µm thick layer of TSMR resist on a 6-inch wafer is 0,51 Euros.
To remove a resist is 0,40 Euros.
The costs of a etch bank are approximately 0,50 Euros for each 6-inch wafer.

The prices at IWG Garhöfer are:
1 g ammonium hexachloroplatinate costs approximately 17 Euros.
1 ml 26 % hydrazine hydrate costs approximately 0,070 Euros.

For the hydrazine spin coating process ca. 90 mg ammonium hexachloroplatinate per 6-inch wafer are needed. This estimates to roughly 1,53 Euros of platinum costs. There is a high excess of platinum, as the process is not optimized. A lot of platinum ends in the developer, whereas only a small part ends on the silicon wafer. Thus it is to say there is room for improvement.
For the hydrazine spin coating process approximately 50 ml 2,6 % hydrazine hydrate solution per 6-inch wafer are needed. This estimates to roughly 0,35 Euros hydrazine costs. This is a high excess of hydrazine, as the process is not optimized.
The costs for chemicals per 6-inch wafer in the hydrazine spin coating process are ca. 1,88 Euros. The costs for a developer are 0,70 Euros. This results in approximately 2,58 Euros per processed 6-inch wafer.

For the HF bath process with a protected front side approximately 10 mg ammonium hexachloroplatinate per 6-inch wafer are needed. This results in about 0,17 Euros platinum costs. With the costs for a resist layer on the front side, the removing of the resist and equipment costs (etch bank) the production costs for a 6-inch wafer amounts approximately 1,58 Euros.

5. Experimental

5.1. Chemicals

All used chemicals for this thesis are of high purity and especially qualified for the usage in the semi conductor industry. It is important that the chemicals have got none or only few impurities of sodium (Na) and other metals, since metals, especially sodium, diffuse easily in silicon and change the diffusion length.

Ammonium hexachloroplatinate, dihydrogen hexachloroplatinate and hydrazine hydrate solution 24 to 26 % were purchased by IWG Garhöfer.
EDTA and imidazole were purchased by VWR.
HF, HCl, TMAH and easywet were purchased by Kinetics.

5.2. Used Equipment

The Clean room was provided by Infineon Technologies Austria AG.
The SEM pictures were taken by Infineon department for failure analyses.
The used SDI was a FAaST 230 by Semiconductor Diagnostics, Inc
The Elymat was provided by Infineon Technologies Austria AG.

5.3. HF bath process

The following process scheme was used.
The plating bath (newly mixed or old) is stirred and heated on operating temperature, which is mostly 70 °C, but also room temperature of approximately 20 °C, 40 °C, 60 °C, 80 °C was tested.)
The wafer is dipped for 1 minutes or 30 seconds into 1% hydrofluoric acid to remove the native silicon oxide.

The wafer is put into the plating bath, mostly for 10 minutes, but also 2, 5, 15, 30, 60, 80 and 110 minutes.
The wafer is then put into pure water.
After the water rinsing, it is dried below a nitrogen stream and on air.
For wafers with a protected front side a TSMR resist is deposited before the HF dip. The resist is removed with DMF and IPA after the plating.

The following plating baths were tested.

Table 1: Tested baths for the HF process Part 1

HF baths: Part 1

bath name	**V [ml]**	**HF 50% [ml]**	**NH_4F 40% [ml]**	**NH_3 25% [ml]**	**H_2O [ml]**	**TMA 248 WA (2 to 3% TMAH with surfactant) [ml]**
bath 1	700	200	200	300	0	0
bath 2	-	0	some	30	0	0
bath 3	540	0	500	40	0	0
bath 8	ca. 400	few drops	400	0	0	0
bath 14	600	0	300	0	300	0
bath 15	800	0	20	0	780	0
bath 16	750	20	30	0	700	0
bath 17	800	100	0	0	500	200
bath 18	800	16	0	0	514	270
bath 19	800	5	0	0	295	500
bath 21	800	16	0	0	514	270
bath 22	800	10	0	0	290	500
bath 23	800	10	0	0	290	500
bath 24	800	10	0	0	290	500
bath 25	800	10	0	0	290	500
bath 26	2000	25	0	0	725	1250
bath 27	2000	25	0	0	725	1250
bath 29	ca. 11000	150	0	0	ca. 9000	1400
bath 30	10350	150	0	0	9000	1200

Table 2: Tested baths for the HF process Part 2

HF baths: Part 2

bath name	**$(NH_4)_2PtCl_6$ $*6H_2O$ [g]**	**$H_2PtCl_6*6H_2O$ [g]**	**pH**	**T [°C]**
bath 1	3,0910	0,0000	6,5	40, 70
bath 2	3,0871	0,0000	8,5	40
bath 3	3,1777	0,0000	7,0 - 7,5	70 - 80
bath 8	2,0544	0,0000	4,8 - 6,0	50 - 75
bath 14	1,0680	0,0000	-	70
bath 15	0,3662	0,0000	5,0	70
bath 16	0,7841	0,0000	-	65
bath 17	0,9365	0,0000	acid	40, 60
bath 18	0,4558	0,0000	1,0	70
bath 19	0,4622	0,0000	5,0	70
bath 21	0,4794	0,0000	3,4	70
bath 22	1,0000	0,0000	4,5	RT, 70
bath 23	1,0000	0,0000	4,5	RT, 70
bath 24	1,0000	0,0000	4,5	RT, 70
bath 25	2,0710	0,0000	4,5	70
bath 26	2,5000	0,0000	4,6, 4,9	60 - 80
bath 27	0,0000	2,7000	-	70, 75
bath 29	10,3367	0,0000	4,9 - 5,5	70
bath 30	10,3820	0,0000	5,1	70

The table demonstrates various bath compositions, which were tested in different experiments. Two values in the pH column mean that the bath was tested in one experiment at a certain value. Then the pH was changed and the bath was tested during another experiment at another pH value. Various values in the temperature column mean that the bath was tested with a different temperature in different experiments.

5.3.1. Solubility of Ammonium Hexachloroplatinate in HF bath solution

HF bath solution:
900 ml H_2O
120 ml TMAH 25% (0,35 mol/l)
15 ml HF 50% (0,83 mol/l)

ca. 0,147 g/100 ml (T = 40°, pH = 5,3)

5.4. Hydrazine Bath Process

The following process scheme was used:
The plating bath was stirred and heated on operating temperature, mostly 70 °C, also room temperature of approximately 20 °C was tested.
Then, the wafer was dipped for 30 seconds or 1 minute into 1% hydrofluoric acid to remove the native silicon oxide.
The wafer was further put into the plating bath, mostly for 10 minutes, but also for 20, 30 and 40 minutes.
The wafer was put into pure water.
Finally after the water rinsing it was dried below a nitrogen stream and on air.

Various plating baths with hydrazine as a reducing agent were tested, but none of them delivered a good result. The reason for that was that the hydrazine baths were too instable. Thus the hydrazine spin coating process was developed.

The following baths were tested.

Table 3: Tested baths for the hydrazine bath process Part 1

hydrazine baths: Part 1

bath name	V [ml]	$N_2H_4.H_2O$ 24-26% [ml]	CH_3COOH 100% [ml]	H_2O [ml]	HCl 32% [ml]	EN [ml]
bath 4	500	50	50	400	0	0
bath 5	570	200	120	200	50	0
bath 6	500	200	100	150	50	0
bath 7	100	40	20	30	10	0
bath 9	100	40	0	40	0	1
bath 10	100	1	0	59	0	0
bath 11	100	0,1	0	80	0	1
bath 12	500	100	100	247	50	3
bath 13	1000	100	100	747	50	3

Table 4: Tested baths for the hydrazine bath process Part 2

hydrazine baths: Part 2

bath name	NH_3 25% [ml]	imidazole [g]	NH_4Cl [g]	$(NH_4)_2PtCl_6$ $*6H_2O$ [g]	H_2PtCl_6 $*6H_2O$ [g]	pH	T [°C]
bath 4	0	0	0	3,1720	0,0000	4,1	70
bath 5	0	17,5604	0	0,5380	0,0000	4,2	70
bath 6	0	0,761	0	1,1021	0,0000	-	70, 73
bath 7	0	0,1687	0	0,1952	0,0000	-	-
bath 9	19	0,1853	0	0,2148	0,0000	10,3	70
bath 10	40	0	0,2893	0,2584	0,0000	14,8	70
bath 11	19	0,16	0	0,2000	0,0000	-	RT
bath 12	0	1,7	0	2,0000	0,0000	-	-
bath 13	0	1,7	0	2,0000	0,0000	-	70

The table presents various bath compositions, which were tested during different experiments. Two values in the temperature column mean that the bath was tested in one experiment at a certain value and in another experiment at another temperature value.

5.5. The hydrazine spin coating process

Firstly, the wafer was dipped for 30 seconds or 1 minute into 1% hydrofluoric acid to remove the native silicon oxide.

Then, the wafer was put on the spinning equipment and rotated at a certain speed, that is 100, 200, 300 and 400 rpm.

An aqueous solution with solved platinum ions and hydrazine was further mixed and put on the wafer.

The solution interacted for a certain time, mostly for 3 minutes, but also for 1 and 5 minutes.

Then, the wafer was put into pure water.

Finally, after the water cleaning it was dried with a higher rotation of 1000 or 2000 rpm. The rest humidity was dried on air.

The following solutions were used:

Table 5: Used solutions for the hydrazine spin coating process

platinum solution:

No.	**H_2O [ml]**	**$(NH_4)_2PtCl_6*6H_2O$ [g]**	**$H_2PtCl_6*6H_2O$ [g]**	**easywet [µl]**
1	2000	4,1560	0,0000	100
2	1000	2,1563	0,0000	50
3	800	1,5000	0,0000	50
4	800	1,7156	0,0000	50
5	800	1,3223	0,0000	50
6	100	0,0000	1,7218	80
7	100	1,2000	0,0000	50
8	200	0,8021	0,0000	0

hydrazine solution:

No.	**$N_2H_4*H_2O$ 24 to 26% [ml]**	**easywet [µl]**
1	2000	100

The table shows various compositions of solutions, which were tested in different spin coating experiments.

5.6. Other Pt deposition processes

5.6.1. HCl bath

A bath with hydrochloric acid instead of hydrofluoric acid was tested. The bath could not deposit platinum on the wafer. The same process scheme as for the HF bath was used.

bath 20:
V = 800 ml
45 ml HCl 32% (0,57 mol/l)
270 ml TMA 248 WA (0,11 mol/l)
485 ml H_2O
$(NH_4)_2PtCl_6.6H_2O$: 0,4125 g ($1,3\ 10^{-3}$ mol/l)
pH = 0,5

5.6.2. Ethylene glycol process

The following process scheme was used for the ethylene glycol bath.
Firstly, the plating bath was stirred and heated on operating temperature, of mostly 70 °C, but also room temperature of approximately 20 °C was tested.
Then, the wafer was dipped for 30 seconds or 1 minute into 1% hydrofluoric acid to remove the native silicon oxide.
The wafer was further put into the plating bath, mostly for 10 minutes, but also for 20, 30 and 40 minutes.
Then, the wafer was put into pure water.
Finally, after the water rinsing, it was dried below a nitrogen stream and on air.

A plating bath with ethylene glycol as reducing agent was tested. It did not deliver a good result however, since the bath with ethylene glycol was too instable. Thus the ethylene glycol spin coating process was developed.

The following bath was tested.

bath:
V = 900 ml
200 ml H_2O
700 ml ethylene glycol
$(NH_4)_2PtCl_6.6H_2O$: 1,3574 g
T = 100 °C

The ethylene glycol spin coating process:
Firstly, the wafer is dipped for 30 seconds or 1 minute into 1% hydrofluoric acid to remove the native silicon oxide.
Then, the wafer is put on the spinning equipment and rotated at a certain speed, of mostly 200 rpm, but also 100 rpm.
A heated aqueous solution with solved platinum ions and ethylene glycol (T = ca. 100 °C) was further mixed and put on the wafer.
The solution interacted for a certain time, of mostly 3 minutes, but for also 2, 5 and 10 minutes.
The wafer was then put into pure water.
Finally, after the water cleaning, it was dried using higher rotation of 1000 or 2000 rpm. The rest humidity was dried on air.

5.6.3. Palladium as catalytic precursor layer

The following process scheme was used for the deposition of palladium as catalytic precursor layer:
Firstly, the palladium dip bath was stirred and heated on operating temperature. (T = 40 °C)
Then, the wafer was dipped for 10 minutes into 1% hydrofluoric acid to remove the native silicon oxide.
The wafer was put into the palladium pre dip bath for 3 minutes.
Then, the wafer was put into the palladium dip bath for 1 minute.
The wafer was further put into pure water.
Finally, the wafer was used for the HF bath process or the hydrazine spin coating process.

Palladium pre dip bath:
1900 ml H_2O
100 ml H_2SO_4 96 %

Palladium dip bath:
The bath has been bought from BASF. Infineon is not informed about the exact composition of the bath.

5.6.4. Platinum acetylacetonate spin coating process

The platinum acetylacetonate spin coating process:
Firstly, the wafer is dipped into 1% hydrofluoric acid for 1 minute to remove the native silicon oxide.
Then, the wafer was put on the spinning equipment and rotated at a certain speed of 200 rpm.
A solution of solved platinum acetylacetonate in dichloromethane (CCl_2H_2) was further put on the wafer.
The solution interacted for a certain time (10 minutes) under UV light (254 nm and 366 nm).
The wafer was then rinsed with 10 ml IPA and 10 ml dichloromethane.
Finally, the water was rotated with a higher speed of 2000 rpm.

6. Conclusion of Thesis

Layer of platinum silicide in semiconductors, especially in reverse recovery diodes, ensure a soft reverse recovery behaviour, a low forward voltage (VF) and a high reverse voltage (VR). Usally in large scale fabrication the platinum is vaporized on the silicon. Then platinum silicide is formed in a furnace, after that the excess metal is removed with aqua regia. Following this step platinum is diffused in the silicon. The vapor coating process is very expensive, because vacuum is needed and a lot of platinum is wasted in the vapor equipment. It is therefore that the semiconductor industry is interested in an alternative process to deposit the platinum. An alternative to that is electroless deposition. This process must fulfil the following requirements: to deposit the platinum directly on the silicon on patterned or unpatterned wafers, to work on p- or n-doped silicon from different base material or from different implantation doses of boron (B), phosphor (P) and arsenic (As), to be used in ultra-large scale integration (ULSI), to be much cheaper than the platinum vapor coating process and little to non influence on the other processes for the device. The finished device, eg. Emmcon diode, has to have the same electrical behavior (VF, VR, etc.) as the reference device, fabricated with the vapor coating process.

Thus various methods to deposit platinum electroless on silicon were tested in this thesis. Two methods the HF bath process and the hydrazine spin coating process can be used in ultra-large scale integration (ULSI).

The HF bath process is a plating bath containing hydrofluoric acid and dissolved platinum salt. In the hydrazine spin coating process an aqueous solution of ammonium hexachloroplatinate and hydrazine are spinned on a wafer. Both processes deliver the required electrical parameters (VF, VR) for an Infineon Emmcon diode.

The HF bath process has got the disadvantage of that platinum can only be diffused from the back side of the wafer, but it is considerably more cost effective than the standard vapor coating process.

The hydrazine spin coating process is easy to handle. It is more cost effective than the standard vapor coating process. There is still a great saving potential in it, which has not been fully explored yet.

7. Appendix

7.1.1. Platinum

Electrochemical potential of platinum:

$E^0_{Pt^{4+}/Pt^0} = 0{,}74V$ [4], [5]

$E^0_{Pt^{2+}/Pt^0} = 1{,}2V$ [6]

$E^0_{PtCl_4{}^{2-}/Pt^0} = 0{,}73V$ [6]

$E^0_{PtCl_6{}^{2-}/PtCl_4{}^{2-}} = 0{,}74V$ [6]

$E^0_{Pt(0H)_2{}^0/Pt^0} = 0{,}16V$ [6]

Fermi level:

Pt: $E_c = -0{,}23eV$ [6]

PtH: $E_c = -0{,}50eV$ [6]

Solubility of ammonium hexachloroplatinate:

Solubility in water at 15 °C: 7 g/l [7]

Solubility in water at 20 °C: 0,5 g/100 ml, 5 g/l [9]

Solubility in water at 100 °C: 3,365 g/100 ml, 33,65 g/l [9]

Solubility in 1M NH_4Cl at 20 °C: 0.0028 g/100 ml, 0,028 g/l [9]

Solubility in HF bath at 40 °C: 0,147 g/100 ml, 1,47 g/l (see Experimental)

7.1.2. Silicon

Electrochemical potential of silicon/silicon fluoride: $-E^0_{SiF_6{}^{2-}/Si^0} = 1{,}2V$ [4], [5]

7.2. Wafer material

wafer material 1:

Infineon
Diameter (mm): 150
Product: Polished
Orientation: 1-0-0
Crystalgr.: FZ
Type: N
Dopant: PH
Thickness (µm): 625 ± 15
Resistivity (Ohm.cm): 800 to 1600
SILTRONIC AG

wafer material 2:

Infineon
Diameter (mm): 150
Product: Polished
Orientation: 1-0-0
Crystalgr.: FZ
Type: N
Dopant: PH
Thickness (µm): 625 ± 15
Resistivity (Ohm.cm): 56,0 to 72,5
Poly-Si
SILTRONIC AG

7.3. Infineon Emmcon diode

The Infineon Emmcon diode is a socalled reverse recovery diode. It is used in IGBT modules as an overvoltage protective device. It is important to ensure that the diode has a soft reverse recovery behaviour, a low forward voltage (VF) and a high reverse voltage (VR).
The IGBT modules are mainly used in inverted rectifier for three-phase motor. There are various voltage classes for the different applications.

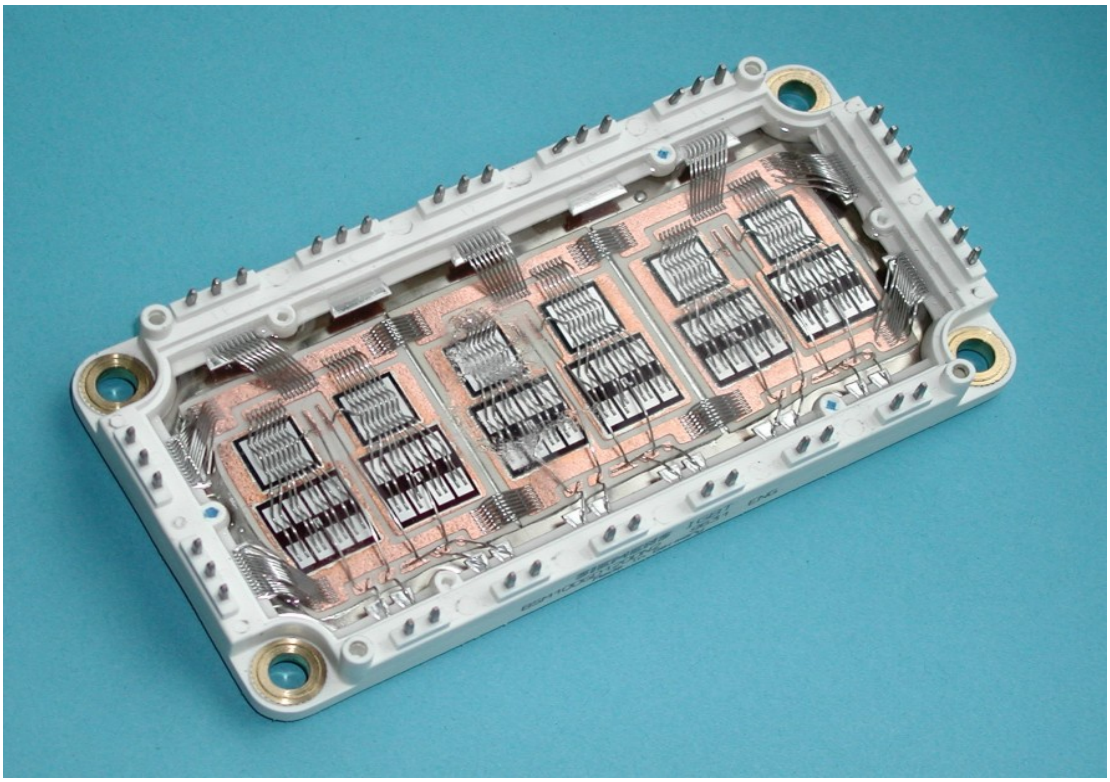

Figure 51 EconoPack: 6 IGBTs and 6 Diodes, up to 1700 V and 600 A

The picture displays a IGBT module, which can be used in washing machines and air conditions.

There are various applications where an Emmcon diode is used:
washing machines, air condition, induction cookers, rice cookers, microwave oven, steamers, refrigerators, uninterruptible power supplies (UPS), power converters for solar energy, power converters for wind energy, hybrid electric vehicle (HEV), escalators, elevators, subways, local and intercity rail traffic, plasma display panel (PDP), ships, just to name a few.

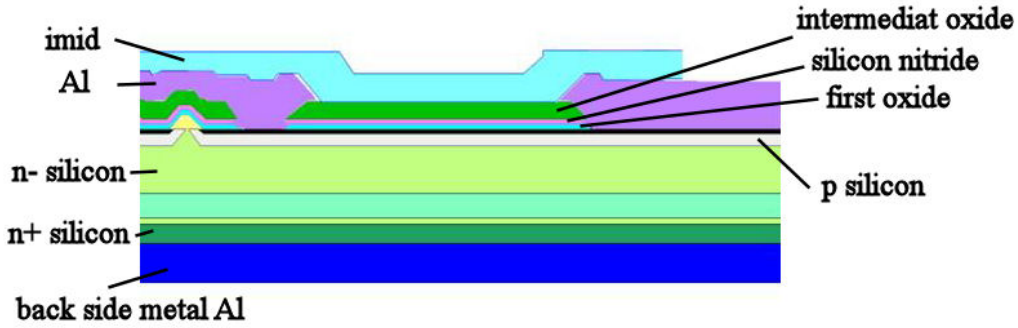

Figure 52 Schematic design of a reverse recovery diode

The picture shows the schematic design of a reverse recovery diode. One contact can be found on the front side of the chip, where the pn-junction lies. The other contact is found on the back side of the chip.

The important steps of the Infineon route of the Emmcon diode in relevance of the platinum deposition are the following:
Firstly, the wafers are dipped into 1% hydrofluoric acid for 30 seconds. Then, they are dried in a spin-dryer. A 25 nm thick platinum layer is further deposited on the front side of the wafers in a vacuum chamber. Platinum silicide is formed in a furnace at 470 °C. The excessive platinum is solved into aqua regia at 50 °C for 15 minutes. The wafers are cleaned with water and then dried. Finally, the platinum silicide is diffused in the silicon in a furnace at 850 °C.

7.4. Methods

7.4.1. SDI (Semiconductor Diagnostics Inc.)

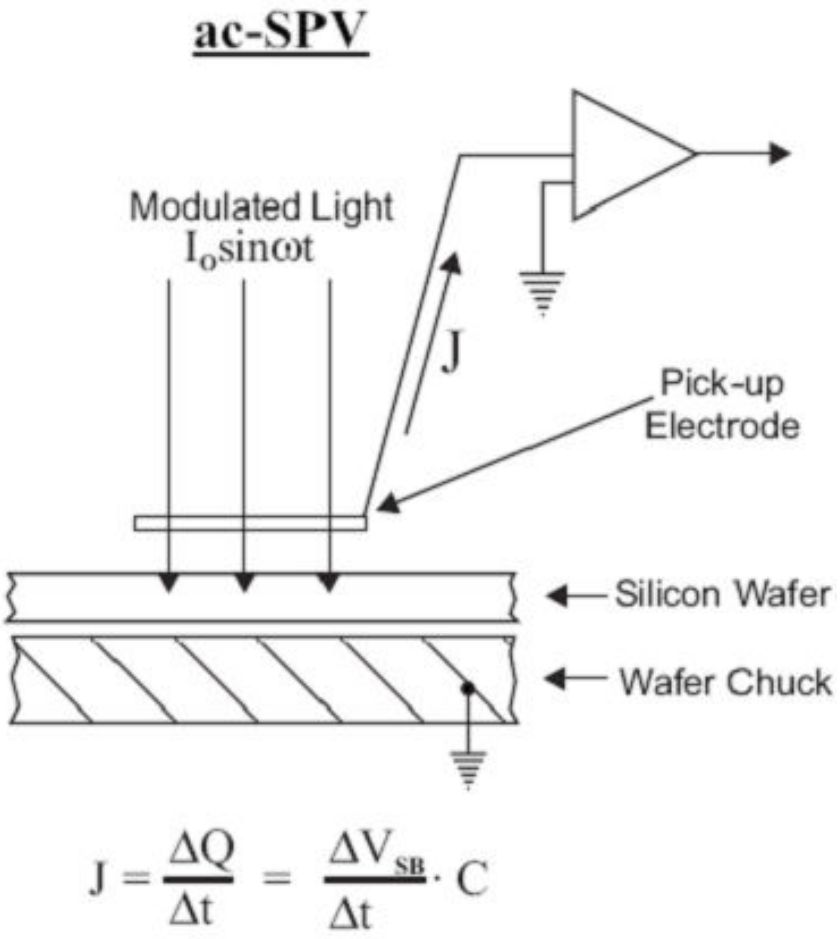

Figure 53 Measure principle of the SDI [21]

In the SDI apparatus the wafer is contacted on the back side. Above the wafer an electrode is placed, which results in a certain capacity. A Laser with a certain wavelength shots on the wafer and induce charge carriers in the silicon. This results in a current J which is measured. J is proportional ΔV_{SB} (light induced change of the silicon surface barrier) which is proportional to the diffusion length.

7.4.2. Elymat

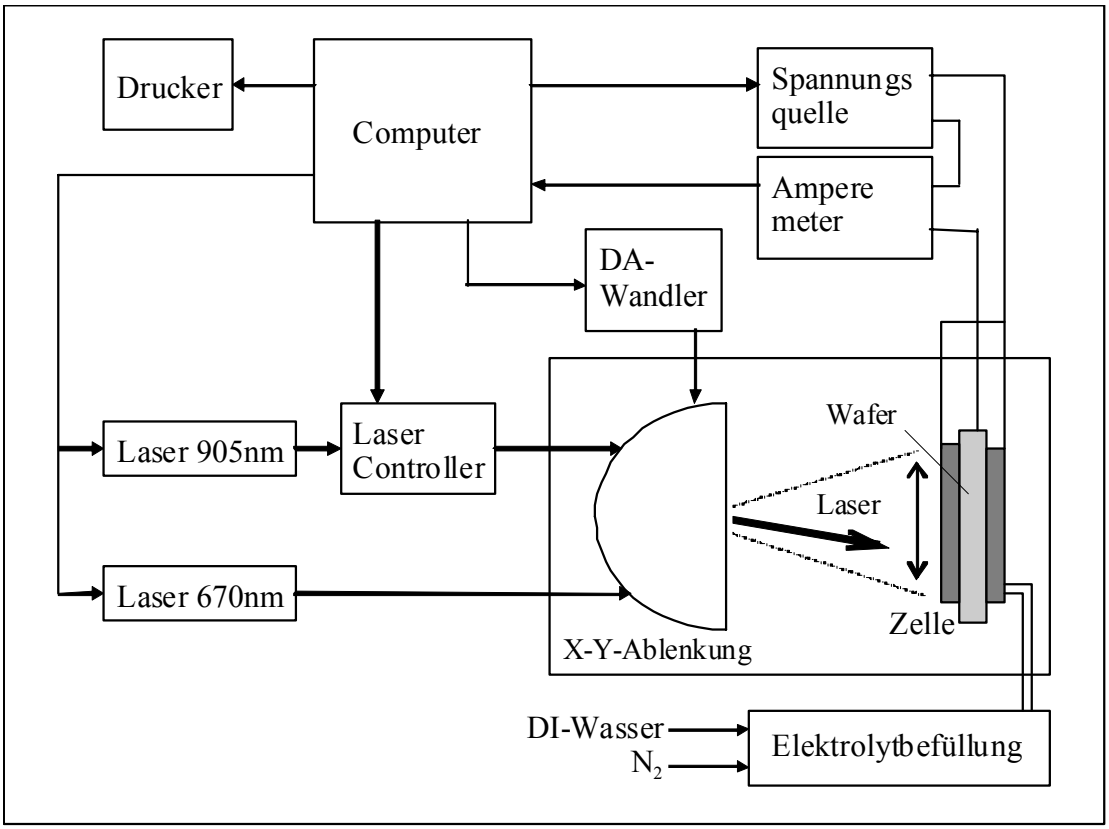

Figure 54 Schematic design of the Elymat [19]

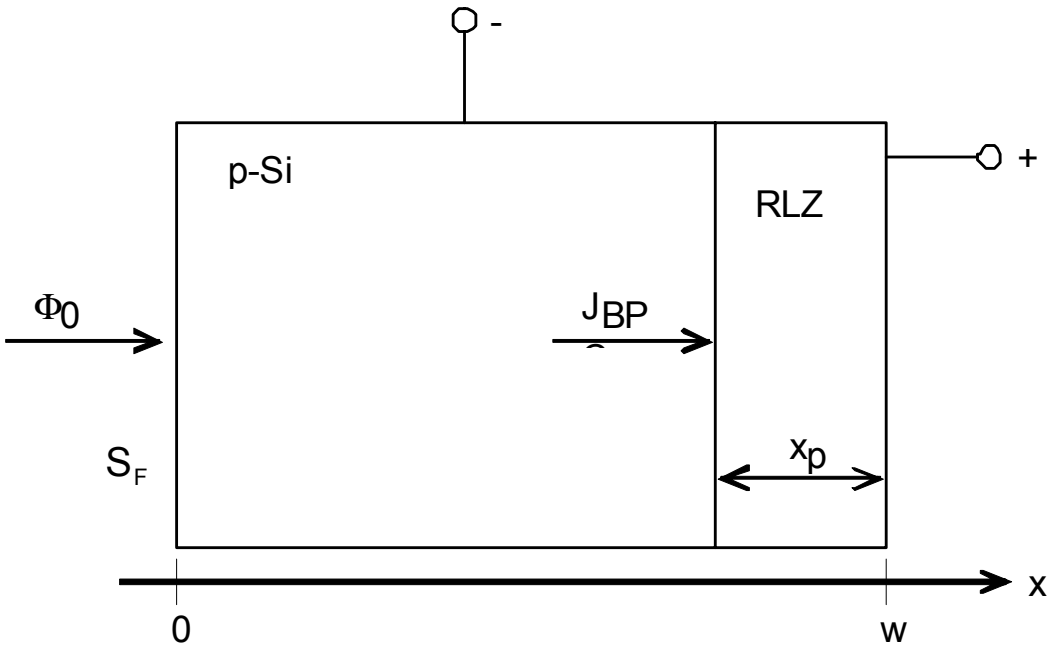

Figure 55 Measure principle of the Elymat [19]

In the Elymat apparatus the wafer is contacted on the back and front side with ring electrodes. A Laser with a certain wavelength shots on the wafer and induces charge carriers in the silicon. This results in a current, which is measured. The measured current is proportional to the diffusion length.

7.5. Curriculum Vitae

Personal:

Name:	Stefan Padlesak
Academic Decree:	Mag. rer. nat.
Date of Birth:	14.09.1979
Nationality:	Austria
Adress:	1100 Vienna, Neusetzgasse 2/1/1
Email	stefan.padlesak@gmx.at

Education:

1990 - 1998	Realgymnasium, Ettenreichgasse 1100 Wien
1998 - 2006	Chemistry Study at the University of Vienna, specialized in food chemistry and analytical chemistry
May 2006	Graduation of the University of Vienna with excellent success
2007 - 2009	Phd study at Technical University of Graz, specialized in chemistry

Professional Training:

March 2005	Excursion and seminars: UNO New York, World Bank Washington D.C., Austrian Embassy Washington D.C.
September 2006	Organisation and participation of the Seminar: Austrian Food Chemestry 2006
2007 - 2009	Various seminars: semiconductor technologies, analytical methods for semiconductors, energy efficiency, photovoltaic, etc.
April 2008	Seminar: project management
May 2008	Seminar: base of semiconductor technology
May 2009	Seminar: communication, discussion techniques and rhetoric

Business Experience:

1998 - 2003 periodical practice	CINCINNATI EXTRUSION GmbH, in the mechanical construction office, construction of extruder parts and assemblies with the ProEngineer program
2005 - 2006 continuous	UNIVERSITY OF VIENNA, Tutor for "Food Chemistry Lab Course" and "Analytical Chemistry Practice for Molecular Biologists", supervision of the students during the courses, holding exams, doing evaluation and administrative work for the courses.
2007 - 2009	INFINEON TECHNOLOGIES AUSTRIA AG, in cooperation of Phd study at TU Graz, in R&D division, practical working in laboratory and clean room, coordination and working in teams.

Published Articles:

Braunrath R., Podlipna D., Padlesak S., Chichna-Markl M., Determination of bisphenol A in canned foods by immunoaffinity chromatography, HPLC, and fluorescence detection, Journal of Argricultural and Food Chemistry, Vol. 53, p. 8911, 2005

Language:

German (mother language), English (fluent, general and chemistry specific), Italian (basic)

Computer Skills:

MS Windows, MS Office (Word, Excel, Power Point, Access), Adobe Photo Deluxe Business Edition, Corel Paint Shop Pro, ProEngineer (construction of extruder parts)

Other Skills:

Working in clean rooms

Interests:

Reading, swimming, role play gaming (DSA, WOD), member of a non-profit association (Liechtenstein Wien)

8. Literature

[1] H. Cachet, M. Froment, and E. Souteyrand, Selective Metal Deposition on Silicon Substrates, J. Electrochem. Soc., Vol. 139, No. 10, 1992

[2] S. Chattopadhyay, P. W. Bohn, Direct-write Patterning of microstructured porous silicon arrays by focused-ion-beam Pt deposition and metal-assisted electroless etching, Journal of Applied Physics, Vol. 96, No. 11, 2004

[3] D. J. Diaz, T. L. Williamson, X. Guo, A. Sood, P. W. Bohn, Electroless deposition of gold and platinum for metallization of the intrapore space in porous gallium nitride, Thin Solid Films, 514, p. 120 – 126, 2006

[4] P. Gorostiza, J. Servat, J. R. Morante, F. Sanz, First Stages of Platinum Electroless Deposition on Silicon (100) from Hydrogen Fluoride Solutions studied by AFM, Thin Solid Films, 275, 1996

[5] P. Gorostiza, R. Diaz, F. Sanz, J. R. Morante, Different Behavior in the Deposition of Platinum from HF Solutions on n- and p-Type (100) Si Substrates, J. Electrochem. Soc., Vol. 144, No. 12, 1997

[6] A. F. Holleman, E. Wiberg, Lehrbuch der Anorganischen Chemie, Gruyter, Auflage 101, p. D156, 1995

[7] IWG Garhöfer, MSDS Ammonium hexachloroplatinate, 2007

[8] R. A. Jeanmenne Jr., M. DeLaurentis, K. Pourrezaeik, R. B. Beard, Electroless Plating on Medical Catheters, PF Online

[9] G. B. Kauffman, J. J. Thurner, D. A. Zatko, Ammonium Hexachloroplatinate (IV), Inorganic Synthesis, Vol. 9, p. 182 – 185, 1967

[10] G. Kokkinidis, A. Papoutsis, D. Stoychev, A. Milchev, Electroless deposition of Pt on Ti : catalytic activity for the hydrogen evolution reaction, Journal of electroanalytical chemistry ISSN 1572-6657, Vol. 486, No. 1, p. 48-55, 2000

[11] G. V. Kuznetsov, V. A. Skryshevsky, T. A. Vdovenkova, A. I. Tsyganova, P. Gorostiza, F. Sanz, Platinum Electroless Deposition on Silicon from Hydrogen Fluoride Solutions, J. Electrochem. Soc., Vol. 148, 2001

[12] V. L. Liang, R. Chan, O. Chyan, Preparation and Characterization of Electrolessly Deposited Platinum and Palladium Nanoparticles on Pyrolyzed Photoresist Films on Silicon Substrates, American Journal Of Undergraduate Research, Vol. 1, No. 1, 2002

[13] M. J. Madon, Fundamentals of Microfabrication, CRC Press, 2nd Ed., 2002

[14] G. O. Mallory, J. B. Hajdu, Electroless Plating Fundamentals And Applications, AESF, Reprint Edition, 1990

[15] A. K. Phillips, R. B. Moore, Ionic acuators based on novel sulfonated ethylene vinyl alcohol copolymer membranes, Polymer; No. 46, p. 7788-7802, 2005

[16] L. A. Porter, H. C. Choi, A. E. Ribbe, J. M. Buriak, Electroless Deposition and Patterning of Morphologically Complex Precious Metal Films on Semiconductor Surfaces, Materials Research Society Symp. Proc., Vol. 737, 2003

[17] L. A. Porter, H. C. Choi, J. M. Schmelzer, A. E. Ribbe, L. C. C. Elliott, J. M. Buriak, Electroless Nanoparticle Film Deposition Compatible with Photolithography, Microcontact Printing, and Dip-Pen Nanolithography Patterning Technologies, Nano Letters, Vol. 2, No. 12, p. 1369 – 1372, 2002

[18] Z. Rao, E. K. Chong, N. L. Anderson, M. G. Stevens, R. Driver, K. V. Paulose, A tin-free catalyst for electroless platinum deposition on polyethylene terephtalate, Journal of Materials Science Letters, No. 17, p. 303 – 305, 1998

[19] G. Schagerl, Nachweis von Kontaminationen in Silizium-Wafer mit dem Elymat (Electrolytic Metal Tracer), Diplomarbeit, 1998

[20] H. Seidel, L. Csepregi, A. Heuberger, H. Baumgärtel, Anisotropic Etching of Crystalline Silicon in Alkaline Solutions, J. Electrochem. Soc., Vol. 137, No. 11, 1990

[21] Semiconductor Diagnostics Inc., FAaST 230 Operations, 1998

[22] S. E. Skrabalak, B. J. Wiley, M. Kim, E. V. Formo, Y. Xia, On the Polyol Synthesis of Silver Nanostructures: Glycolaldeyde as a Reducing Agent, Nano Letters, Vol. 8, No. 7, p. 2077 – 2081, 2008

[23] P. Steinmetz, S. Alperine, A. Friant-Costantini, P. Josso, Electroless Deposition of Pure Nickel, Palladium and Platinum, Surface and Coatings Technology, 43/44, 1990

[24] US Patent 3698939, Method and Composition of Platinum Plating, 1972

[25] US Patent 611182 , Electroless platinum-rhodium alloy plating

[26] US Patent 6391477, Electroless autocatalytic platinum plating

[27] J. B. Yeh, C. Y. Chang, J. W. Chou, K. F. Huang, M. S. Feng, Novel Selective Platinum Deposition on VLSI Contact Hole, Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials, Sendai, p. 227 – 230, 1990

[28] J. Y. Zhang, I. W. Boyd, Excimer lamp-induced decomposition of platinum acetylacetonate films for electroless copper plating, Solid-State Electronices, No. 43, 1999

[29] Y. J. Zhang, F. F. Li, L. J. Dai, Microactuator Based on EVOH-g-SO3H IPMC, IEEE 1-4244-0139-9/06, 2006

[30] Y. J. Zhang, F. F. Li, L. J. Dai, Investigations on Actuation Critical Response Voltage for IPMC Based on Modified EVOH Ionomer, IEEE 1-4244-0609-9/07, 2007

[31] J. V. Zoval, J. Lee, S. Gorer, R. M. Penner, Electrochemical Preparation of Platinum Nanocrystallites with Size Selectivity on Basal Plane Oriented Graphite Surfaces, J. Phys. Chem. B, Vol. 102, p. 1166 – 1175, 1998

9. List of Abbreviations

abbr.	expanded abbreviation	remark
(aq)	aqueous	substance solved in water, with hydrate shell
(g)	gaseous	
(l)	liquid	
$(NH_4)_2PtCl_6$	Ammonium hexachloroplatinate	
(s)	solid	
AES	Auger electron spectroscopy	
AFM	atomic force microscopy	
ca.	circa	Latin for approximately
CMP	chemical mechanical polishing	
CVD	chemical vapor deposition	
DLTS	deep level transient spectroscopy	
DMF	dimethylformamide	C3H7NO
e.g.	exempli gratia	Latin for example
EDS	electron dispersive spectroscopy	
EDX	The energy dispersive X-ray	
EELS	electron energy loss spectrum	
EFTEM	energy filter transmission electron microscopy	
EMD	Electroless metal deposition	
en	ethylenediamine	$C_2H_4(NH_2)_2$
et al.	et alli/alia	Latin for and others
FTIR	Fourier transformed infrared spectroscopy	
HAADF	high angle annular dark field	
HCl	hydrochloric acid	
$HClO_4$	perchloric acid	

HEV	hybrid electric vehicle	
HF	hydrofluoric acid	
HNO_3	nitric acid	
ICP-MS	inductive coupled plasma mass spectroscopy	
IGBT	insulated gate bipolar transistor	
lot	lot	A lot is a quantity of components that have passed through the manufacturing process together. Changes in the manufacturing process affect all parts of a batch. Lot is also called batch. A lot normally consists of 25 wafers. Infineon codes lots with a two letters and 6 numbers code, for example VC843460.
lot code	lot code	Infineon codes lots with a two letters and 6 numbers code, for example VC907505. The first letter stands for the production site. (V = Villach) The second letter indicates the wafer size. (C = 6-inch) The first number stands for the year. (9 = 2009) The next two numbers stands for the week. (07 = the 7^{th} week of the year) The last numbers are a sequence number.
N_2H_4	hydrazine	
$NaBH_4$	sodium boron hydride	
PDP	plasma display panel	
ppb	parts per billion	
ppm	parts per million	

Pt	platinum	
$C_{10}O_4H_{14}Pt$	platinum acetylacetonate	
RBS	Rutherford back scattering spectroscopy	
RCA	Radio Corporation of America	standard cleaning process in semiconductor industry consisting of removal of the organic contaminants, removal of thin oxide layer and removal of ionic contamination
rpm	rotation per minute	
SDI	Semiconductor Diagnostics Inc.	
SEM	scanning electron microscopy	
Si	silicon	
SIPFRED	single inline package fast recovery epitaxial diode	
STEM	scanning transmission electron microscopy	
TEM	electron microscope	
TMAH	tetramethylammonium hydroxide	$N(CH_3)_4OH$
T_W	period width	
ULSI	ultra-large scale integration	
UPS	uninterruptable power supplies	
UV	ultra violett	electromagnetic radiation with a wavelength from 400 nm to 10 nm
VF	forward voltage	
VR	reverse voltage	
XPS	X-ray photoelectron spectroscopy	
X-ray	X-ray	electromagnetic radiation with a wavelength from 10 nm to 0,01 nm