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Nanoimprint lithography as a structuring method of printable materials for organic electronics

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Abstract

Since the discovery of conducting polymers in the late 1970s, a lot of research activities in polymer science aimed at developing printable electronic circuits, which combine multifunctional materials with roll-to-roll (R2R) processing. The advantages offered by R2R production (high throughput, low costs) are often limited by the resolution of the available R2R printing techniques.

In this thesis, nanoimprint lithography (*NIL*) as a R2R compatible, high resolution structuring technique was evaluated as a structuring method for printed materials used in two different organic transistor concepts, namely organic electrochemical transistors (*OECT*s) and organic thin-film transistors (*OTFT*s). As little research existed on *OECT*s, the first task was to identify and validate geometry parameters that improve the device performance. In the case of all-inkjet printed *OECT*s it could be shown that the on-to-off current ratio increases substantially with a smaller gap between the gate and the source-drain area. By optimizing this parameter it was furthermore possible to reduce the switching time of the transistors to 4 s. The data indicated that a further size reduction of the devices will result in even better device performance. Consequently, a *NIL* structuring process allowing for critical feature sizes below 10 µm in fully printed *OECT*s was developed and proof of principle devices were fabricated. Without any material modification, the switching time could be further decreased to about 1 s. Simultaneously, the on-to-off current ratio increased by one order of magnitude compared to the inkjet printed devices.

Similar to *OECT*, *NIL* has also shown its capabilities in increasing the device

performance by miniaturization of critical geometry parameters in *OTFT*s. For a future roll-to-roll (R2R) fabrication of such *NIL* structured *OTFT*s, the use of printed materials (which are also R2R processable) would be advantageous. Thus, the second part of this thesis focuses on the implementation of such materials into the fabrication of *NIL* structured *OTFT*s. An already established *NIL* structured, self-aligned transistor process was modified to better suit the needs of printed materials. This modified process was thoroughly evaluated by analyzing the short channel behavior of reference devices without printed materials. Special focus was put on the parameters correlated to the threshold and sub-threshold transistor regime. Furthermore, the high number of investigated devices with similar characteristics underlined the reliability of the used fabrication method. In the applied self-aligned process, the thicknesses of substrate and dielectric determine the magnitude of the gate-source and gate-drain overlap; the thinner the layers, the smaller the overlap. This raised the question of the smallest possible overlap length maintaining proper DC transistor behavior and sufficient on-current level. Consequently, the process was modified such that the gate-to-source and gate-to-drain overlap lengths of coplanar *OTFT*s can be varied systematically. The results reveal that even devices with a gap instead of an overlap function as transistors and that the on-current decreased only for devices with negative source overlap. The on-current is robust to variations of the overlap length at the drain electrode. As a last step, *OTFT*s with printed, *NIL* structured gate electrodes were fabricated to validate the modified process. Evaluations of the resulting transistors revealed no loss in performance compared to reference devices with evaporated gates.

Zusammenfassung

Seit der Entdeckung leitfähiger Polymere Ende der 1970er Jahre wurde viel Energie in die Entwicklung und Erforschung von gedruckter Elektronik investiert. In diesem Kontext ist vor allem die Möglichkeit, gedruckte Bauteile in einer Rolle-zu-Rolle-Fertigung (R2R) herzustellen, hervorzuheben, da diese einen hohen Durchsatz bei vergleichsweise niedrigen Produktionskosten ermöglichen würde. Allerdings werden die Vorteile dieser Art der Herstellung bei vielen Anwendungsszenarien durch die relativ geringe Auflösung der R2R-Drucktechniken aufgewogen.

Aus diesem Grund beschäftigt sich diese Dissertation mit der Kombination von Nanoimprint Lithographie (NIL), einer hochauflösenden, R2R kompatiblen Strukturierungsmethode, und druckbaren Materialien zur Herstellung von organischen Transistoren. Dabei wurden zwei verschiedene Transistorkonzepte untersucht: zum einen der organische elektrochemische Transistor (OECT) und zum anderen der organische Dünnschichttransistor (OTFT). Da es zu Beginn dieser Arbeit wenig Erkenntnisse über die Einflüsse der Bauteilgeometrie auf die Performance von OECTs gab, wurden verschiedene Parameter in vollständig tintenstrahlgedruckten Transistoren variiert. Die Untersuchung zeigte, dass sich das Verhältnis von Einschalt- zu Ausschaltstrom signifikant mit verringertem Abstand zwischen Gate- und Source-Drain-Elektrode erhöht. Durch Die Optimierung der untersuchten Geometrieparameter war es außerdem möglich, die Schaltzeit der OECTs auf vier Sekunden zu reduzieren. Die Ergebnisse deuteten darauf hin, dass sich die Performance durch weitere Bauteilverkleinerung

zusätzlich steigern lassen würde. Deshalb wurde ein NIL Prozess zur Herstellung von OECTs mit Elektrodenstrukturen von unter 10 µm Größe entwickelt. Allein durch diese Maßnahme war eine Verringerung der Schaltzeit auf eine Sekunde bei gleichzeitiger Erhöhung des Verhältnisses Einschalt- zu Ausschaltstrom um eine Größenordnung möglich.

Die Nanoimprint Lithographie ist nicht nur in der Lage, durch Bauteilminiaturisierung die Leistungsfähigkeit von OECTs zu erhöhen, sondern zeigte in der Vergangenheit auch ähnliche Erfolge bei organischen Dünnschichttransistoren (OTFTs). Für eine zukünftige Rollenfertigung dieser OTFTs wäre die Verwendung von gedruckten Materialien vorteilhaft, da sich moderne Drucktechniken ebenfalls hevorragend für die R2R Prozessierung eignen. Deshalb beschäftigt sich der zweite Teil dieser Dissertation mit der Prozessentwicklung und Evaluation von OTFTs mit NIL strukturierten, gedruckten Materialien. Im Rahmen dieser Arbeit wurde ein bereits etablierter Prozess zur Herstellung von selbstjustierten, NIL strukturierten, organischen Dünnschichttransistoren (NIL OTFTs) modifiziert, um den, durch den Einsatz von druckbaren Materialien entstandenen, geänderten Anforderungen gerecht zu werden. Dieser Prozess wurde zuerst mit Hilfe von Referenzbauteilen ohne gedruckte Materialien evaluiert. Weiters wurde das Auftreten von Kurzkanaleffekten bei diesen Bauteilen im Detail untersucht. Die hohe Anzahl an gefertigten und analysierten Transistoren mit vergleichbarem elektrischem Verhalten zeugt für die hohe Zuverlässigkeit des Prozesses. Bei der verwendeten Selbstjustierung der OTFTs kann die Source/Drain zu Gate Überlapplänge durch die Dicke des Substrates und des Dielektrikums gesteuert werden – je dünner die Schichten, desto kleiner der Überlapp. Dies warf die Frage auf, wie klein der Überlapp sein kann, ohne Abstriche bei der Gleichstromcharakteristik und dem Einschaltstrom machen zu müssen. Durch eine weitere Modifikation des Herstellungsprozesses war es möglich, systematisch den Überlapp zu variieren und auch Bauteile mit asymmetrischen Überlapp herzustellen. Die Untersuchung dieser Bauteilen ergab, dass auch OTFTs mit einem Abstand zwischen Source/Drain und Gate

Elektrode anstatt eines Überlapps als Transistoren funktionieren und dass sich lediglich der Einschaltstrom bei negativem Sourceüberlapp verringerte. Bei negativem Drainüberlapp konnte keine Beeinträchtigung der Kennlinien festgestellt werden. Zuletzt wurden OTFTs mit gedruckten, NIL strukturierten Gateelektroden hergestellt. Die Bauteile zeigten keinerlei Performanceverlust im Vergleich zu Transistoren mit herkömmlichen, aufgedampften Gateelektroden.

Initiatory Statement

The author would like to take this opportunity to clearly state that despite the fact, that my supervisor Prof. Egbert Zojer of the Graz University of Technology did not co-author any of the manuscripts presented in this work, he supported and supervised my research throughout the entire doctoral studies. All research performed for this thesis was done entirely at the JOANNEUM RESEARCH Forschungsgesellschaft mbH as part of the NILecho II project supervised by the author. Nevertheless, Prof. Zojer and the author held monthly to bimonthly meetings to analyze the research results, consult supporting literature and discuss next steps. It was Prof. Zojers explicit wish with respect to the ethics of scientific publication to not appear as a co-author on the papers included in this work, as he felt that his contributions were not significant enough to warrant co-authorship. His support is nevertheless acknowledged in all publications included in this work.

Dissemination

Articles in peer reviewed journals

- P. C. Hütter, T. Rothländer, A. Haase, G. Trimmel, B. Stadlober, *Influence of geometry variations on the response of organic electrochemical transistors*, Applied Physics Letters 103 (2013) 043308.
- T. Rothländer, P.C. Hütter, E. Renner, H. Gold, A. Haase, B. Stadlober, *Nanoimprint Lithography-Structured Organic Electrochemical Transistors and Logic Circuits*, IEEE Trans. Electron Devices. 61 (2014) 1515–1519.
- T. Rothländer, A. Fian, J. Kraxner, W. Grogger, H. Gold, A. Haase, B. Stadlober, *Channel length variation in self-aligned, nanoimprint lithography structured OTFTs*, Organic Electronics, submitted
- T. Rothländer, J. Kraxner, R. Schmied, A. Haase, H. Gold, C. Palfinger, H. Plank, W. Grogger and B. Stadlober, *Influence of the source-gate and drain-gate overlap length on the on-current of self-aligned, NIL structured OTFTs*, Applied Physics Letters, submitted

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- T. Rothländer, P. C. Hütter, H. Gold, A. Haase, G. Jakopic, P. Hartmann, B. Stadlober, *Nanoimprinted Organic Electrochemical Transistors*, Proceedings of the Eurodisplay 2013 (2013) 179-180.

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- T. Rothländer, P. C. Hütter, H. Gold, A. Haase, G. Jakopic, P. Hartmann, and B. Stadlober, *Nanoimprinted Organic Electrochemical Transistors*, Eurodisplay 2013.
- T. Rothländer, P. Hütter, H. Gold, J. Kraxner, W. Grogger, A. Haase and B. Stadlober, *Introduction of printable materials into the fabrication of self-aligned nanoimprint lithography structured OTFTs*, International Symposium on Flexible Organic Electronics 2013.

Further dissemination

- **Conference Proceeding:** T. Rothländer, P. C. Hütter, H. Gold, A. Haase, G. Jakopic, P. Hartmann, B. Stadlober, *Nanoimprinted Organic Electrochemical Transistors*, Proceedings of the Eurodisplay 2013 (2013) 179-180.
- **Invited talk:** T. Rothländer, P. Hütter, A. Haase, A. Fian, H. Gold, G. Jakopic, P. Hartmann and B. Stadlober, *Nanoimprint Lithography in Organic Electronics*, Nanoforum Linz 2013.
- **Poster presentation:** T. Rothländer, P. Hütter, H. Gold, G. Jakopic, P. Hartmann and B. Stadlober, *Nanoimprinted Organic Transistors with Printed Electrodes*, Winterschool on Organic Electronics 2012.

- **Poster presentation:** T. Rothländer, J. Kraxner, W. Grogger, A. Fian, H. Gold, A. Haase, K. Zojer, E. Zojer, B. Stadlober, *Influence of the source and drain overlap on the transistor performance of self-aligned, nanoimprint lithography structured OTFTs*, International Conference on Organic Electronics 2014.

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Thank you, Dani, for always being there, when I needed you the most. The longer we are together, the more I appreciate the great and special relationship we have.

Abbreviations

$MOSFET$	Silicon-silicon dioxide metal-oxide-semiconductor field-effect transistor
A_G	Electrolyte covered gate area
A_{SD}	Electrolyte covered source-drain area
Au	Gold
C'	Capacitance of the gate insulator per unit area
$DIBL$	Drain induced barrier lowering
t_{Diel}	Dielectric layer thickness
ΔV_{ON}	Difference in onset voltage
$OECT$	Organic electrochemical transistor
E_{Drain}	Drain induced electric field
E_{Gate}	Gate induced electric field
f_T	Cutoff frequency
$HOMO$	Highest occupied molecular orbital
I_D	Drain current
I_{FLOOR}	Floor current
I_G	Gate current
I_{OFF}	Off current
I_{ON}	On current
$I_{ON,max}$	Maximum on current
I^*_{ON}	Effective on current
$I^*_{ON,max}$	Maximum effective on current
$I_{G,max}$	Maximum switching current

L	Channel length
L_{depl}	Length of the depletion region
L_{eff}	Effective channel length
L_{OV}	Overlap length
$LUMO$	Lowest unoccupied molecular orbital
μ	Charge carrier mobility
μ^*	Intrinsic mobility
μ_{sat}	Saturation mobility
$N_{SS,max}$	Maximum interface trap density
$OLED$	Organic light emitting diode
I_{ON}/I_{OFF}	On-to-off current ratio
$OTFT$	Organic thin-film transistor
$PEDOT:PSS$	Poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate)
R_{CH}	Channel resistance
R_C	Contact resistance
R_{OFF}	Off resistance
R_{ON}	On resistance
R_S	Sheet resistance
S	Subthreshold swing
t_{Off}	On-to-off switching time
t_{On}	Off-to-on switching time
$TTF-TCNQ$	Tetrathiofulvalene-tetracyanoquinodimethane
V_{DS}	Drain-source voltage
$-V_{DD}$	Negative supply voltage
V_{DD}	Positive supply voltage
V_{GS}	Gate-source voltage
V_{Input}	Input voltage
V_{ON}	Onset voltage
V_{Output}	Output voltage
$V_{Output,high}$	High level output voltage
$V_{Output,low}$	Low level output voltage

V_T	Threshold voltage
W	Channel width

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1. Introduction

1.1. Motivation

Why printed organic electronics?

The combination of printing techniques and organic electronics enables the fabrication of devices that are as inexpensive as printed paper, as large as billboards and as flexible as plastic foil or paper. All that is currently not feasible with conventional microelectronics. A tremendous cut-down in costs compared to silicon-based manufacturing arises mainly due to the omission of assembling and packaging. The ability to integrate printed organic circuits on light-weight and flexible substrates enables new applications like rollable displays [1], stretchable electronics in smart textiles [2] or large area organic photovoltaics [3]. Furthermore, compared with silicon-based electronics the low processing temperatures and less aggressive chemicals needed make printed organic electronics more environmentally sustainable. Because of these advantages, the global market for printed, flexible and organic electronics is forecast to grow from $16.04 billion in 2013 to $76.79 billion in 2023 [4].

Why high-resolution printed organic electronics?

While standard printing techniques like e.g. screen printing, gravure printing or inkjet printing allow for both large and inexpensive roll-to-roll production,

they lack in lateral resolution. However, high resolution is highly beneficial to increase the performance of *OTFT*s (higher switching speed, higher current through the device, higher on-to-off current ratios) and increase device integration density. Highly integrated devices are a necessity when addressing high-performance applications like e.g. radio frequency identification tags. To date nanoimprint lithography (*NIL*) is the only available technique uniting roll-to-roll compatibility and high printing resolution.

1.2. Aim of this work

The main goal of this thesis was the development of a fabrication process for organic transistors combining printed materials and nanoimprint lithography. Furthermore, the impact of this process and the used solution-based materials on the devices should be evaluated. Two different organic transistors, namely the organic electrochemical transistor (*OECT*) and the organic thin-film transistor (*OTFT*), are investigated and devide this thesis into two main parts, subdivided into five chapters:

Part I: Organic electrochemical transistors The first part of this thesis comprises studies regarding the impact of *NIL* on printed organic electrochemical transistors.

As little was known concerning the influence of the geometry on the device performance of *OECT*s, the first task was to validate, whether high resolution structuring of *OECT*s using *NIL* can improve these devices. Thus, in chapter 3: "Influence of geometry variations on the response of OECTs" geometry variations in fully inkjet printed *OECT*s are studied. It was shown that a decrease of the studied geometry parameters significantly increases switching speed and on-to-off current ratio. The results also indicated a potential further improvement using high resolution structuring [5].

Consequently, chapter 4: "Nanoimprint Lithography Structured OECTs" deals with the process development and evaluation of high resolution structured *OECT*s using nanoimprint lithography. As expected, the resulting transistors show a further increase in performance, proving the potential of *NIL* for the structuring of *OECT*s [6].

Part II: Organic thin-film transistors It has been shown in the past, that similar to the results achieved in *OECT*s in this work, *NIL* is also capable of reducing the critical dimensions of *OTFT*s and thus improve their performance. For a future roll-to-roll (R2R) fabrication of such *NIL* structured *OTFT*s, the use of printed materials (which are also R2R processable) would be advantageous. Due to this the second part of this thesis focuses on the analysis of self-aligned, nanoimprint lithography structured organic thin-film transistors and the introduction of printed gates into the fabrication process.

As a first step an already established fabrication process for *NIL OTFT*s was modified to better suit the needs of printed materials. In chapter 5: "Channel length variation in self-aligned, NIL structured OTFTs", the short channel behavior of refernce devices without printed materials *OTFT*s is thoroughly analyzed to identify an optimum channel length for the transistors and to validate the reliability of the modified process.

The self-alignment used in the fabrication of the *NIL OTFT*s allows for gate-source and gate-drain overlaps well below 200 nm. This raised the question whether an optimum overlap length exists and what would happen if the overlap is smaller than this optimum or even worse, no overlap is present at all. Chapter 6: "Influence of the source/drain to gate overlap in self-aligned, NIL structured OTFTs" gives a detailed analysis of this topic. By deliberately changing the incident angle during the self-alignment the overlap is controlled and varied. It could be shown that for devices with no gate-source overlap the on-current drops significantly, nevertheless, transistor characteristics are still visible.

To achieve the set goal of the second part of this thesis the developed fabrication process was combined with printed materials. Chapter 7: "OTFTs with NIL structured, printed gate electrodes" evaluates and compares *OTFT*s with a *NIL* structured, printed gate electrode with devices with a *NIL* structured, evaporated electrode to determine the usability of printed, *NIL* structured materials in organic electronics. No decrease in performance compared to the reference devices was found when using printed gate electrodes, showing the high compatibility of *NIL* and printed materials.

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2. Fundamentals

This chapter gives a short introduction to organic transistors based on the book chapters by Klauk and Gnade [1], Fix et al. [2], Leenen et al. [3], Horowitz [4], and James et al. [5]. The interested reader is referred to these works for a more detailed view on the topic.

2.1. Historical development

2.1.1. Electronics

This section is based on the works of Klauk and Gnade [1] and Horowitz [4].

The electronics age started around the beginning of the 20th century. Based on the vacuum rectifier invented by Ambrose Fleming in 1904 and the cathode ray tube by Karl Braun in 1897, Lee de Forest invented the triode in 1906. The invention marked the first electrical amplification device, a ground breaking discovery leading to the development of radio communication and long distance telephony. However, it soon turned out that the triode had its limitations (high power consumption, difficult to miniaturize, slow). In 1926 the first patent for a solid-state device to replace the triode and overcome its limitation was filed by Julius Edgar Lilienfeld. He described an "apparatus for controlling the flow of an electric current between two terminals of an electrically conducting solid by establishing a third potential between said terminals" [6]. The first

working field effect transistors were the famous "point contact" transistors by Bardeen and Brattain (1947), shortly followed by the first bipolar transistor in 1948 by Shockley. Still it took over ten more years of development before the first silicon-silicon dioxide metal-oxide-semiconductor field-effect transistor (*MOSFET*) was presented [7]. Today, *MOSFET*s are omnipresent in our daily life, building the core components of every personal computer, mobile phone and many other microelectronic devices.

2.1.2. Organic electronics

This section is based on the works of Klauk and Gnade [1], Horowitz [4], and Witte and Wöll [8].

Despite the astonishing variety of known organic materials and their excellent and often tunable physical properties, they are often said to be linked by the fact, that they are inable to conduct electric current. Even more, a huge number of applications rely on organic materials being excellent insulators. Nevertheless, this assumption is not true as there are a number of materials that show are semiconductors or even conductors. The discovery of conducting organic solids can be traced back to the same year as the triode was developed, when scientists reported on the dark conductivity and photoconductivity of anthracene crystals [9, 10]. Scientific interest in the conductivity of organic materials trailed away over the next years and it was not revived before Nobel laureate Albert Szent-Györgyi stated that the transfer of electrical charge along molecular chains plays a role in certain processes in biological systems [11]. Further investigation lead to the synthesis of the first true organic metal in 1973, tetrathiofulvalene-tetracyanoquinodimethane ($TTF-TCNQ$), which exhibits a conductivity of the same order of magnitude as inorganic metals [12]. Organic semiconductors have first been discovered in the late 1940 [13], but the key work was the accidental discovery, that the conductivity of polyacetylene can be varied over eleven orders of magnitude by adding small amounts of impurities [14]. This discovery

resulted in the Nobel Prize in Chemistry for three of the authors, namely Alan Heeger, Hideki Shirakawa and Alan MacDiarmid. A further milestone was the demonstration of the first organic light emitting diode (*OLED*) in 1987 [15]. With the invention of poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (*PEDOT* : *PSS*) in 1988 it was shown that high conducting polymers can also be highly air stable. Probably the first organic thin-film transistor (*OTFT*) was published by Ebisawa, Kurokawa, and Nara [16] in 1983, showing a small but measurable difference in drain current with gate voltage. The first *OTFT*s with usefully large current modulation emerged in the late 1980s, with polymers [17, 18] and small molecules [19, 20] as semiconductors. Due to the poor performance of the devices, only limited scientific interest remained for the next ten years. The main research effort was put on the improvement of the charge-carrier mobility, which is to the present day a very important research topic of organic electronics [21–25]. *OTFT* investigation on a broader scale, including industrial groups, started not before 1997, when the first pentacene based *OTFT* with a mobility comparable to amorphous silicon was found [26, 27]. Today, organic electronics is a thriving field of research with over 25000 publications alone in the year 2013 [28].

2.2. The organic thin-film transistor

For a better understanding of the organic thin-film transistor this section will give a brief summary of the concept of semiconductivity in general and organic semiconductivity in special. Furthermore, the working principle of an *OTFT* is explained. The section is based on the work by Horowitz [4].

2.2.1. Semiconductor definition

Generally speaking, a semiconductor is defined as a nonmetallic solid, that conducts worse than a conductor, but better than an insulator [4]. This definition

lacks distinctive boundary conditions that allow for a categorization of different materials. The distinction of conductors from semiconductors is clearly defined in the band theory of solids. It states that a conductor is defined as a material, where the Fermi level lies within the conduction band (Figure 2.1). As this paragraph will show, it is much more difficult to clearly separate the definition of a semiconductor and an insulator, as these materials show no fundamental difference in their conduction bands. In semiconductors and insulators alike the Fermi level lies in the band gap between the conduction and the valence band. In a number of books on basic solid state physics the width of the band gap is used to separate the two categories, stating that by convention all materials with a band gap smaller than 4 eV are considered semiconductors, higher band gap materials are considered insulators [29, 30]. Note that only at sufficiently high temperatures charge carriers can populate the conduction band of semiconductors (and insulators), which allows for a measurable conductivity in such materials. The band theory based semiconductor definition is only true for intrinsic semiconductors [4]. More often extrinsic semiconductors are used. Extrinsic means that the electronic properties of a base material have been modified by doping it with small amounts of impurities (usually part per million). This doping results in localized energy levels that are closer to the conduction (n-type doping) or valence band (p-type doping) and thus lower the energy needed to promote charge carriers to the conduction or valence band, respectively (Figure 2.2.2). The resulting materials are then called p-type or n-type semiconductors, as one type of charge carriers (electrons or holes) contributes more to the conductivity. Different from inorganic semiconductors like e.g., silicon, most organic materials known to date cannot be synthesized with comparable purity [4]. As a result, both p-type and n-type impurities are usually present in the materials and compensate each other. These so-called compensated semiconductors behave much like intrinsic semiconductors. The famous results achieved with polyacetylene is one of the few examples of successful doping in organic materials [14]. To reach a significant change in electronic properties of most *OTFT*s, the doping concentration has to be a

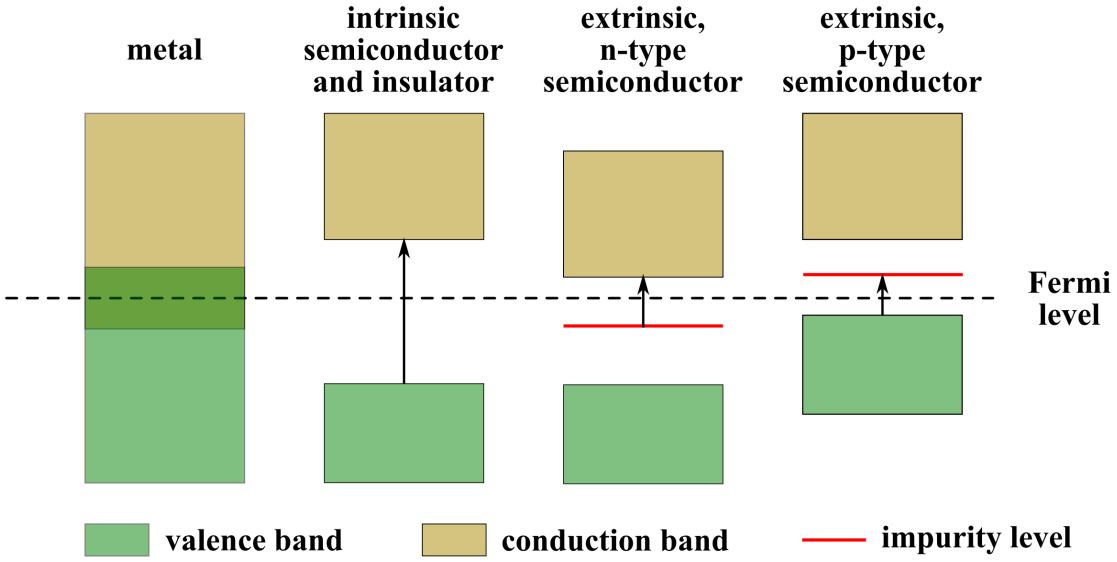

Figure 2.1.: Energy diagram of a metal, an insulator, intrinsic and extrinsic semiconductors including the difference between n-type and p-type semiconductors [4]

few percent instead of the part per million concentrations in silicon. Organic materials with such a high amount of dopants usually behave like conductors and thus can no longer be used in the fabrication of transistors [4]. Nevertheless, n-type and p-type semiconductors exist in organic electronics, but the terms refer to a different concept of electron or hole conductivity as will be explained in section 2.2.3.

2.2.2. Thin-film transistor architecture

Numerous different types of transistors are in use in todays electronics. By far the most relevant for organic electronics is the thin-film transistor [1], first proposed for inorganic electronics by Weimer [31] in 1962 (Figure 2.2). It consists of three electrodes, a semiconducting layer and a dielectric layer. Two of the electrodes, called source and drain, are on the same layer and connected to the semiconductor, while the third, called gate, is isolated by the dielectric layer from the semiconductor. All materials are present as thin layers and have been processed on one another. A thin-film transistor is called organic thin-

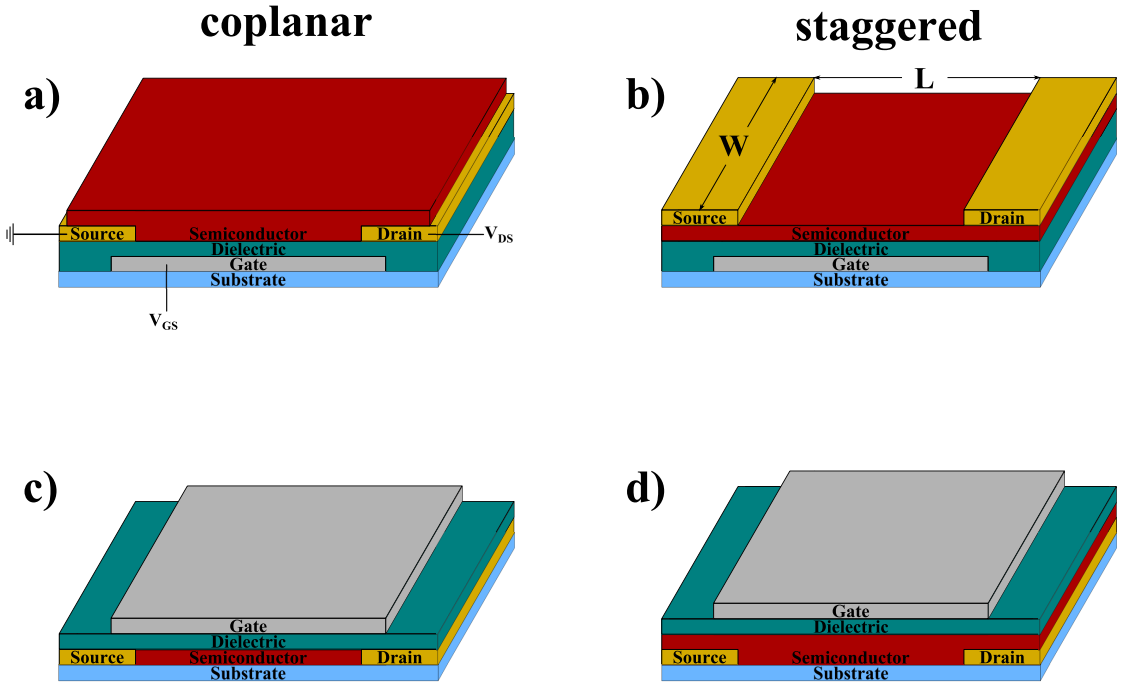

Figure 2.2.: Schematics of bottom gate (a,b) and top gate (c,d) *OTFT*s, visualizing the difference between coplanar (a,c) and staggered (b,d) geometries; the electrical connections of V_{GS} and V_{DS} are visible in (a), the definitions of the L and the W in (b); all devices in this work are fabricated as bottom gate, coplanar transistors

film transistor when at least the semiconducting layer consists of an organic material. There are four different geometry variations in *OTFT*s. They are divided according to the position of the electrodes. Top gate (Figure 2.2 a,b) and bottom gate (Figure 2.2 c,d) refer to whether the gate is the first layer with respect to the substrate or the last one. Staggered (Figure 2.2 b,d) and coplanar (Figure 2.2 a,c) differentiate between source and drain being in direct contact with only the semiconductor or also with the dielectric layer. Figure 2.2 a also shows how the transistor is electrically connected. Note that by definition the electrode connected to ground is called source. In accordance with the name of the electrodes, the two applied voltages are called gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}), in short gate voltage and drain voltage.

The four geometries differ not only concerning electrical properties, but also pose different challenges in terms of fabrication, especially when considering

*OTFT*s with critical dimensions of 1 µm and below. Top gate configurations have the advantage of the semiconductor being encapsulated by the dielectric. This allows for a higher lifetime of the often fragile organic semiconductors under ambient conditions. For most applications the staggered version is favored, as the coplanar design is very difficult to process. It is the only *OTFT* layout where three layers (source/drain, semiconductor, gate) instead of two have to be aligned with respect to each other. Also note that small errors in the semiconductor alignment with respect to source/drain result in the device not being coplanar any more. The biggest advantage of top gate transistors (dielectric layer on top of the semiconductor) is also its greatest weakness. Only very few materials have proven to be processable on top of an organic semiconductor without negatively influencing its electrical characteristics. This is the reason why bottom gate configurations are more common. The bottom gate, coplanar layout offers the advantage that the organic semiconducting layer is applied last, allowing for the use of otherwise semiconductor harming structuring methods like e.g., standard photolithography for the source/drain layer. The staggered layout on the other hand has been reported to have advantages concerning the electronic characteristics, as the influence of the energy barrier is lowered, resulting in lower contact resistance (compare Section 2.2.3) [32].

2.2.3. Organic semiconductors

As stated in section 2.2.1, doping is not the main promoter of charge carriers into the conduction/valence band of organic semiconductors, instead an alternative method of charge injection through the contacts is used. Figure 2.3 shows the energy scheme for the well studied material combination of gold (*Au*) source electrode (grounded) and pentacene as a semiconductor. Apart from the Fermi level of *Au* it shows the highest occupied molecular orbital (*HOMO*) and lowest unoccupied molecular orbital (*LUMO*) levels of pentacene [33]. A positive voltage applied to the gate would result in negative charges being induced into the *LUMO* of the semiconductor. As there is a significant energy difference

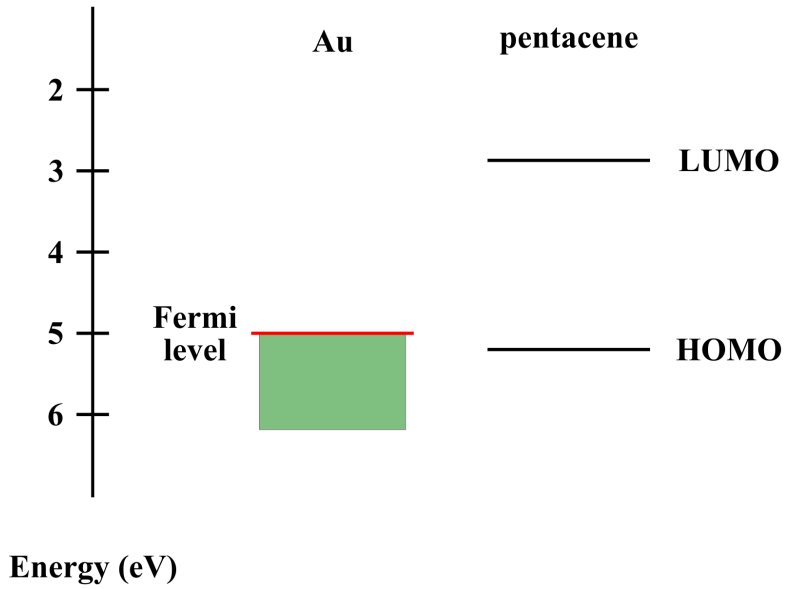

Figure 2.3.: Energy diagram comparing the position of the Fermi level of gold with the *HOMO* and *LUMO* levels of pentacene [33].

between the source Fermi level and the *LUMO* level of about 2 eV it is highly unlikely that charge carriers can overcome this barrier. Thus, little to no current will pass through the semiconductor [4]. For negative gate voltages holes are injected into the *HOMO* level. The energy barrier in this case is only about 0.2 eV, which can easily be overcome by the charge carriers [4]. Because of this behavior, pentacene in combination with gold electrodes is said to be p-type [4]. If the injection barrier between the contact and the semiconductor is lower for an injection into the *LUMO* level, the material/electrode combination is called n-type. Note that these definitions are very different from what has been stated about doped semiconductors in section 2.2.1.

2.2.4. Working principle

This section is based on the works by Klauk and Gnade [1], Fix et al. [2], Leenen et al. [3], Horowitz [4], James et al. [5], and Newman et al. [34].

To demonstrate the electrical behavior of an *OTFT* output and semilogarithmic

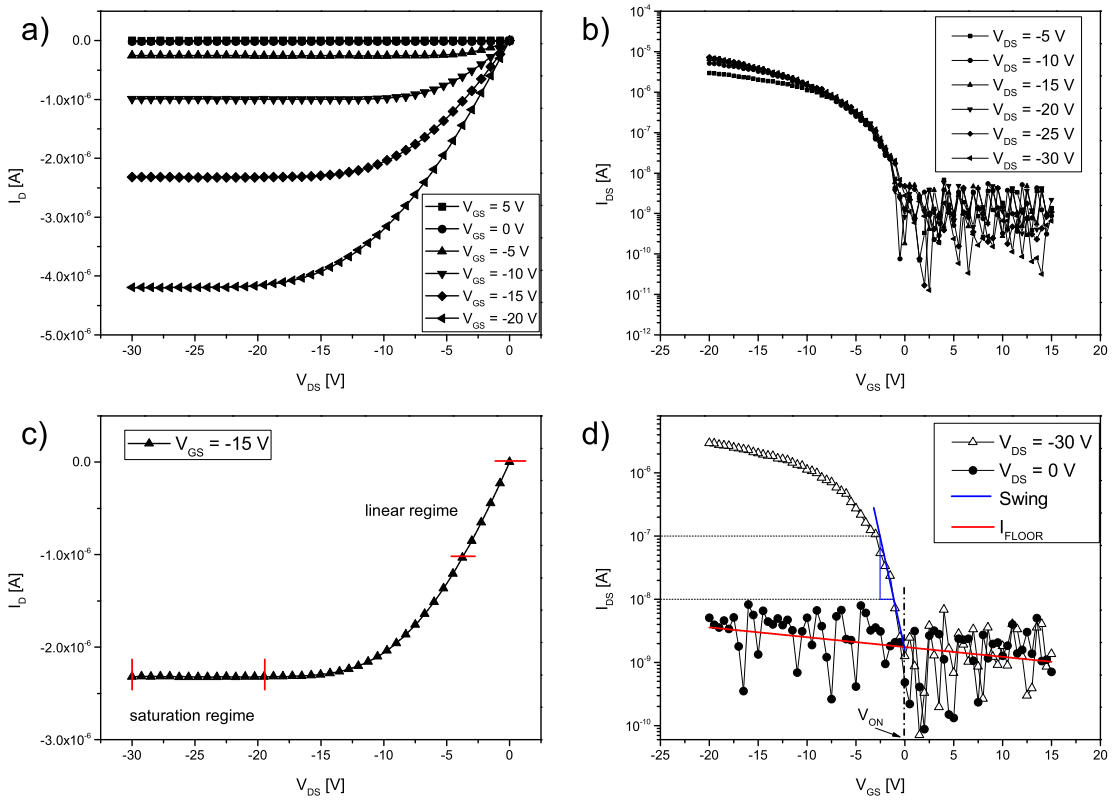

Figure 2.4.: Typical output (a) and transfer (b) characteristics of a pentacene *OTFT*; visualization of the linear and saturation regimes (c); extraction method of onset voltage (V_{ON}) and subthreshold swing (S) as performed in this work

transfer characteristics (called subthreshold characteristics throughout this work) are shown in Figure 2.4 a,b[1]. When looking at a transistors output characteristic for a certain V_{GS} (Figure 2.4 c) one can distinguish two main regimes. The linear regime, where the drain current (I_D) follows Ohm's law and rises linearly with the V_{DS} (visible at low drain-source voltage values) and the saturation regime where I_D is independent of V_{DS} (visible at drain-source voltage values above V_{GS}) [34]. These behaviors can best be explained by looking at the charge carrier concentration in the channel of the *OTFT* (Figure 2.5) and by treating the transistor as a capacitor between the gate electrode on one side, and the semiconductor plus the source and drain electrodes on the other. When a voltage

[1]The semilogarithmic plot improves visibility of the threshold region crucial for subthreshold swing and onset voltage extraction.

is applied to the gate, a charge is induced at the insulator-gate interface. This induces a countercharge with opposing sign at the insulator-semiconductor interface. As discussed before, this results in charge carrier injection, given that the energy barrier (source electrode - semiconductor) is low enough. Due to this behavior the *OTFT* is said to work in accumulation (as the charge carriers are accumulated at the insulator-semiconductor interface to form the channel).

Note that the channel formation in *OTFT*s is very different from that in a *MOSFET*, where the gate voltage is used to deplete the insulator-semiconductor interface of majority charge carriers (present in the semiconductor without applied potentials) to allow for a minority carrier channel to be formed and conduct the current. This effect is called inversion and the channel is called the inversion channel. By that an ideal ohmic connection to the source and drain contacts is guaranteed which are typically highly n-doped for p-doped semiconductors or highly p-doped for n-doped semiconductors [35].

When $V_{DS} = 0$, the charge is evenly distributed along the channel [34]. The charge density at a given position x along the channel is proportional to the voltage difference $V_{GS} - V(x)$ [34]. It is given by

$$q_{ind}(x) = n(x) \cdot e \cdot t = C' \left(V_{GS} - V(x) \right) \tag{2.1}$$

with $n(x)$ being the number of charges in the channel, e the fundamental unit of charge, t the thickness of the charged layer and the capacitance of the gate insulator per unit area (C'), usually given in $\mathrm{nF\,cm^{-2}}$. In actual devices, charge injection seldomly starts at exactly $V_{GS} = 0\mathrm{V}$. The energy barrier between the Fermi level and the *HOMO* (for p-type semiconductors) or *LUMO* (n-type) shifts the voltage needed for initial charge injection. Traps in the semiconductor film and at the insulator-semiconductor interface further contribute to this shift, as they immobilize injected charge carriers and thus hinder a current flow [34]. All these effects are combined in the threshold voltage (V_T), changing equation 2.1 to

$$q_{ind}(x) = n(x) \cdot e \cdot t = C' \left(V_{GS} - V_T - V(x) \right) \tag{2.2}$$

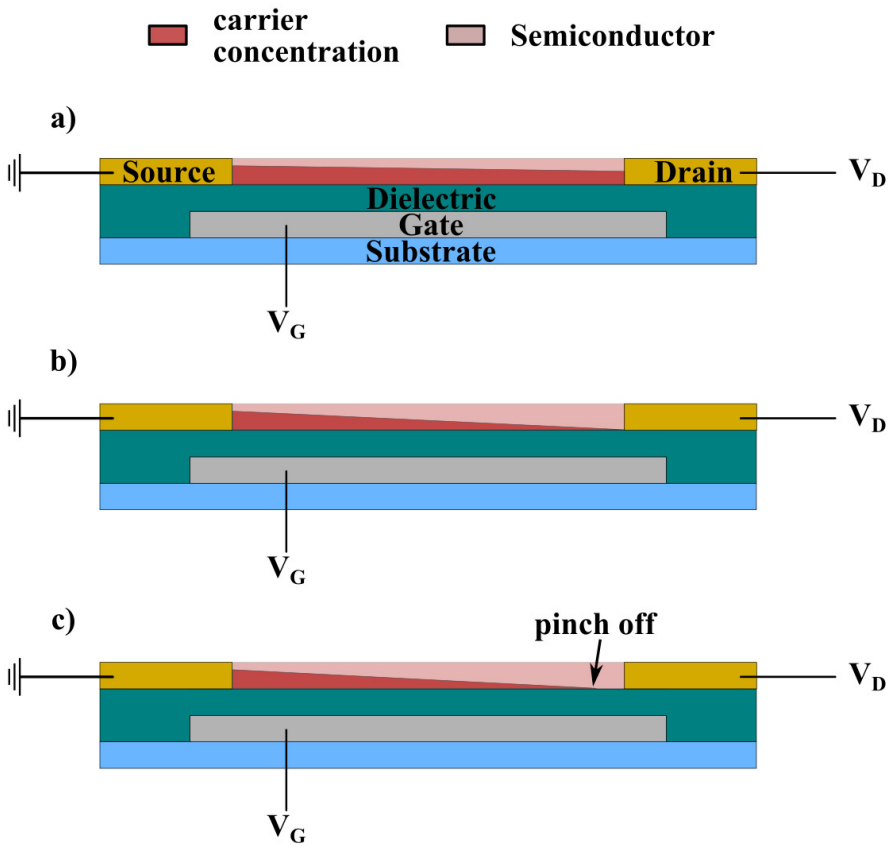

Figure 2.5.: Charge carrier concentration of an *OTFT* (a) in the linear regime, (b) when pinch-off occurs at $V_{DS} = V_{GS} - V_T$ and (c) in the saturation regime. [34]

The extraction of V_T is a largely discussed, but yet not fully resolved topic in *OTFT*s [36–38]. While a complete description of the difficulties of the extraction would be beyond the scope of this work, a brief description will be given. In *MOSFET*s the threshold voltage corresponds to the point of inversion. Using that fact and performing the corresponding device calculations the V_T value can be extracted from a $\sqrt{I_D} = f(V_{GS})$ plot in the saturation regime [34]. Since *OTFT*s work solely in accumulation, the calculations for *MOSFET*s are not fully applicable and thus a similar extraction will not lead to correct values [36, 37]. Also V_T is not independent of the drain voltage, as it is for poly-silicon based *MOSFET*s [38]. Nevertheless, it is a good approximation used in numerous publications on organic thin-film transistors.

When applying a small voltage to the drain electrode the charge distribution

decreases linearly along the channel from the source to the drain electrode (Figure 2.5 a) [34]. Note that the charge density minimum (at the semiconductor/drain electrode interface) is still a positive value. In this linear regime the average charge density is

$$\overline{q_{ind,channel}} = C' \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \tag{2.3}$$

Combining equation 2.3 with Ohm's law and the definition of the conductivity leads to an equation that describes the current-voltage behavior in the linear regime:

$$I_D = \frac{W}{L} \left(\overline{q_{ind,channel}} \cdot e \cdot t \right) \mu V_{DS} \Rightarrow \tag{2.4}$$

$$I_D = \frac{W}{L} C' \mu \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \tag{2.5}$$

with μ being the charge carrier mobility (= the charge carrier velocity per unit electric field), W the channel width and L the channel length (compare Figure 2.2 b). Considering that in the linear regime $V_{GS} - V_T \gg V_{DS}/2$, the $V_{DS}/2$ term can in good approximation be omitted. Equation 2.5 can thus be reduced to

$$I_{D,lin} = \frac{W}{L} C' \mu_{lin} \left(V_{GS} - V_T \right) V_{DS} \tag{2.6}$$

When $V_{DS} = V_{GS} - V_T$ the potential difference between the gate electrode and the channel area closest to the drain electrode vanishes, and this part of the channel is depleted of free charge carriers (Figure 2.5 b) [34]. Further increase in V_{DS} only pushes this so called pinch-off point towards the source electrode, but the integrated resistance of the channel, and thus I_D, remains unchanged (Figure 2.5 c). The charge carriers are pulled through the small depleted area close to the drain electrode by the comparably large electric drain field [34]. Note that the independence of I_D of V_{DS} in the saturation regime is only true when L is much larger than the depletion region (compare section 2.3). Implementing $V_{DS} = V_{GS} - V_T$ into equation 2.5 results in the following I-V relation for the saturation regime:

$$I_{D,sat} = \frac{W}{2L} C' \mu_{sat} \left(V_{GS} - V_T \right)^2 \tag{2.7}$$

The charge carrier mobility can be extracted by measuring I_D over V_{GS} curves for fixed values of V_{DS} [34]. Three more parameters are generally extracted from the transistor characteristics, namely the on-to-off current ratio (I_{ON}/I_{OFF}), the subthreshold swing (S) and the onset voltage (V_{ON}). I_{ON} is usually extracted as the maximum I_D value measured for a given device. The off current (I_{OFF}) is the average I_D value for $V_{GS} < V_T$. The ratio is usually given in orders of magnitude only. To prevent the difficulties of V_T extraction in $OTFT$s, the onset voltage (V_{ON}) can be extracted instead. It represents the intercept of $log(I_D/[A])$ with a defined floor current (I_{FLOOR}) (Figure 2.4 d). While this value cannot be used in the very basic equations presented in this chapter, it can help comparing different devices, especially in terms of I_{ON}. For obvious reasons, one would obtain different I_{ON} values for identical devices with varying V_{ON}, since it is quite common to measure all devices up to the same gate-source voltages. $OTFT$ models considering V_{ON} instead of V_T can also be found in literature [37]. Finally, the subthreshold swing is defined as

$$S = \frac{dV_{GS}}{d\left(log\left(I_D/[A]\right)\right)} \tag{2.8}$$

usually given in $V/decade$. It is defined as the steepest inverse slope of the subthreshold curve (compare Figure 2.4 d). In order to correctly compare the subthreshold swing for $OTFT$s with different dielectric layers and/or thicknesses, a C' normalized $S^* = C' \cdot S$ should be used [34].

A self-written extraction software was used to extract V_{ON} and S in the devices of chapters 5 and 6. In this software I_{FLOOR} is defined by a linear fit through the subthreshold curve at $V_{DS} = 0$V curve (Figure 2.4 d). To define the intersect point V_{ON}, the algorithm searches for the first $log(I_D/A)$ value smaller than I_{FLOOR} at a target V_{DS} value, starting at the highest V_{GS} value. A second linear fit is performed through the n earlier $log(I_D/[A])$ values. The intersection of the two linear fits defines V_{ON}. The slope of the second fit defines S. While this method leads to lower V_{ON} and higher S values compared to the original definition, it ensures that outliers in the measurement have less influence on the extraction method as they are somewhat smoothed by the linear fit. This

is important as the currents close to V_{ON} are small and thus often affected by noise.

2.3. Short channel effects in OTFTs

This section is based on the works by Haddock et al. [39], Reese and Bao [40], and Klauk [41].

Equations 2.6 and 2.7 were derived using the so-called gradual-channel approximation. This approximation states that the electric field induced by V_{GS} at the semiconductor - dielectric interface is only a function of the position along the channel. This is only true for devices where this gate induced electric field E_{Gate} is much larger than the longitudinal drain induced field E_{Drain} [39]. Considering that the two fields are defined as

$$E_{Gate} = \frac{V_{GS}}{t_{Diel}}, \quad E_{Drain} = \frac{V_{DS}}{L} \tag{2.9}$$

with t_{Diel} being the thickness of the dielectric layer, it is clearly visible that short channel lengths paired with high dielectric thicknesses and high drain voltages with respect to the gate voltage result in inapplicability of the gradual-channel approximation [39]. As small L values result in often required higher switching speeds, this parameter is often the cause for transistor characteristics that do not obey equations 2.6 and 2.7. The resulting devices show (usually unwanted) deviations from the ideal transistor characteristics and are referred to as devices experiencing short channel effects. A number of such effects can be determined and the three most common ones will be explained in the following section.

2.3.1. Channel-length modulation

The channel-length modulation is characterized by a linear increase of I_D in the saturation regime [39]. As described in section 2.2.4, a depletion region forms

at the drain electrode when $V_{DS} > V_{GS} - V_T$ and its length increases towards the source with increasing V_{DS}. As this region is by definition free of charge carriers, it is not part of the channel and hence instead of L, an effective channel length L_{eff} has to be used in equation 2.7 [42]:

$$I_{D,sat} = \frac{W}{2L_{eff}} C' \mu_{sat} (V_{GS} - V_T)^2 \tag{2.10}$$

with

$$L_{eff} = L - L_{depl} \tag{2.11}$$

with L_{depl} being the length of the depletion region. When decreasing L, the influence of L_{depl} increases, resulting in a linear increase of I_D with V_{DS} in the saturation regime [43].

2.3.2. Drain induced barrier lowering

In short channel devices the strong lateral field induced by the drain electrode reduces the potential barrier in the channel, especially close to the source electrode [44]. This results in an increased charge carrier concentration in the channel and thus an increased current through the channel. To still be able to deplete the channel of charge carriers and thus switch the transistor off, a higher gate voltage compared to long channel devices is necessary [44]. Haddock et al. [39] could show that similar to *MOSFET*s the change in threshold voltage compared to long channel devices is inversely proportional to the channel length:

$$\Delta V_T = V_T(L) - V_{T,long\,channel} \propto \frac{1}{L} \tag{2.12}$$

This "threshold voltage roll-off" [39, 43, 45] shifts the threshold voltage towards more positive values for p-type and more negative values for n-type transistors.

2.3.3. Contact resistance and short channels

If not explicitly stated otherwise this section is based on the works of Reese and Bao [40] and Klauk [41]. A complete insight on the very complex topic of the contact resistance in general and its influence on short channel devices in particular is beyond the scope of this work. The interested reader is referred to numerous experimental and theoretical works in literature [40, 41, 46–54]. This chapter will focus solely on the "[...] most wide-spread method to determine [the contact resistance] R_C experimentally" [51], namely the transmission line model (TLM) by Luan and Neudeck [55]. As will be discussed later the simplified and idealized assumptions of the TLM are seldomly given in real $OTFT$s and thus the method will most likely not result in an accurate extraction of R_C [51–56], but merely in a rough estimation.

In the linear regime it is assumed that an $OTFT$ acts according to Ohm's law with respect to V_{DS}, when V_{GS} is held constant. Thus, a total resistance R_T can be calculated. It can furthermore be divided into two contributions, namely the channel resistance (R_{CH}) and the contact resistance (R_C) [55]:

$$R_T(L) = R_{CH}(L) + R_C \tag{2.13}$$

As indicated, the former is assumed to depend on the channel length while the latter is not. In long channel devices R_{CH} will be much larger than R_C, but for small channel length devices the contact resistance will influence R_T and thus the measured mobility. This results in a contact resistance dependent, effective mobility μ^*. Combining Ohm's law, equation 2.6 and μ^*, R_C can be extracted as

$$\left(\frac{W}{L}C'\mu^*\left(V_{GS}-V_T\right)\right)^{-1} = \left(\frac{W}{L}C'\mu_{lin}\left(V_{GS}-V_T\right)\right)^{-1} + R_C \tag{2.14}$$

By measuring the total resistance of similar devices with different channel lengths a value for R_C and thus for the intrinsic mobility μ^* can be calculated [55] (compare Chapter 5).

The TLM method is only valid if "[...] ohmic contacts are present and [...] R_C is independent of L" [51]. In $OTFT$s ohmic contacts are rarely present, especially in bottom contact devices [48, 57]. As soon as non-ohmic contacts are present, R_C also depends on L [51]. Furthermore, the methods relies on the measurement of multiple devices with different channel lengths, which despite best efforts in fabrication may not have the exact same contact and channel resistances [53]. As the extraction of R_T is performed in the linear regime, gate leakage currents can negatively influence the measurement. It should also be noted that TLM cannot destinct between contact resistance at the source and drain electrode [53].

A number of improvements to the method as well as alternative methods to extract R_C and μ^* have been proposed. Nevertheless, if one knows about the limitations of the method, the very simple extraction of the contact resistance provided by TLM can improve the understanding of $OTFT$s (compare Chapter 5).

2.4. The electrochemical transistor

This section introduces the concept of organic electrochemical transistors using the most prominent organic representative, the *OECT* based on *PEDOT* : *PSS* as the electrode material. It is based on the work of Nilsson [58].

Different from the *OTFT*s discussed in section 2.2, the modulation of the current in *OECT*s is not controlled by the accumulation of charge in the channel, but by the oxidation state of a polymer present in the channel. The switching is driven by an electrostatic potential and not by an electric field, resulting in low voltage operation at the expense of switching speed. In the case of *PEDOT* : *PSS* the reversible redox reaction controling the current through the device is given by

$$PEDOT^{+}PSS^{-} + M^{+} + e^{-} \rightleftharpoons PEDOT^{0} + M^{+}PSS^{-} \tag{2.15}$$

with M^{+} being cations from an electrolyte and e^{-} being electrons. As $PEDOT^{0}$ has an orders of magnitude higher impedance compared to $PEDOT^{+}PSS^{-}$, the current through a *PEDOT* : *PSS* electrode can be modulated with this redox reaction.

2.4.1. Electrochemical transistor architecture

Due to the concept of not using a dedicated semiconducting layer as a channel, but modulating the current through the electrode instead, an *OECT* has a very different device architecture. In the lateral configuration used throughout this work the device consists of only two different layers (compare Figure 2.6) [58]. The first layer consists of *PEDOT* : *PSS*, structured into two separate areas, the second one consists of an electrolyte providing the cations for the redox reaction. It covers up parts of the *PEDOT* : *PSS* areas. One solid line of *PEDOT* : *PSS*, called source-drain line, is oxidized or reduced depending on the potential applied to the other *PEDOT* : *PSS* area, called the gate electrode. For a better understanding of the working principle of the *OECT*, two more primitive

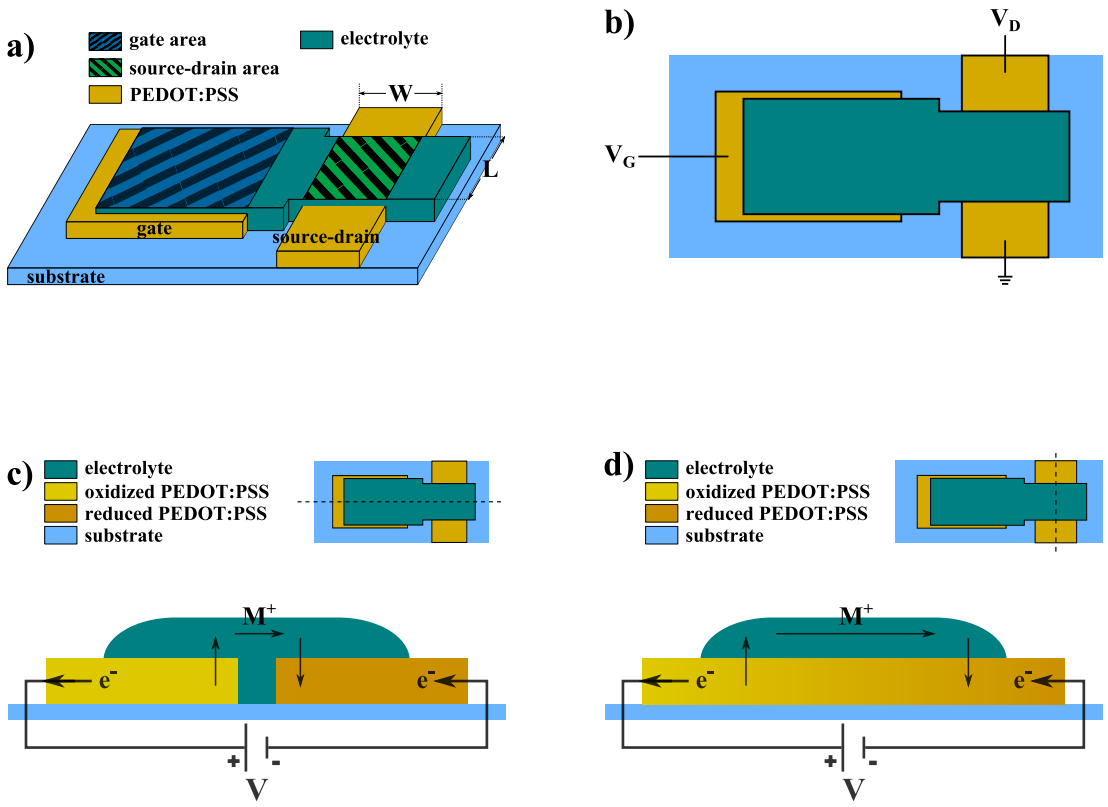

Figure 2.6.: Schematics of an organic electrochemical transistor (a); top view with electrical connections (b); bi-stable (c) and dynamic electrochemical cell (d); dashed lines in the insets of (c) and (d) indicate where each cell is used in the *OECT*

configurations are discussed first. These configurations represent two different cuts through the *OECT*, as indicated in Figure 2.6 c,d.

2.4.2. The bi-stable configuration

Figure 2.6 c shows a schematic of a bi-stable electrochemical cell. Two separate areas of *PEDOT : PSS* share a common electrolyte. When applying a voltage between the two areas, an ionic current in the electrolyte is induced. As the cations are driven away from the positively biased electrode it will be further oxidized. On the other hand the negatively biased electrode attracts the cations and thus is reduced. To maintain electroneutrality and obey equation 2.15, either cations have to move out of the positively biased and into the negatively biased

area or anions have to move the opposite way. In the case of $PEDOT:PSS$ the anions are PSS^-, which are too large to move out of the film [58]. Thus, the cations provided by the electrolyte move and ensure electroneutrality. Concerning the conductance in a bi-stable cell, the negatively biased area is reduced and thus less conducting, while the positively biased area is further oxidized and thus higher conducting. The cell is called bi-stable, as both areas remain in their redox state for a relatively long time even when the applied voltage is removed [58].

2.4.3. The dynamic configuration

In this configuration the two ends of one solid line of $PEDOT:PSS$ with an electrolyte on top are biased with respect to each other (Figure 2.6 d). This results in a gradient of electrochemical potential along the line. Comparable to the bi-stable configuration reduction occurs close to the negatively biased end, oxidation close to the positive end. After the equilibrium is reached, there is no ionic current in the $PEDOT:PSS$ film [58]. For low voltages the current rises linearly with the voltage, obeying Ohm's law. After a critical potential is reached, the current saturates and becomes independent of the voltage. In accordance with the pinch-off in $OTFT$s this potential is called pinch-off potential (compare Chapter 2.2.4). Saturation occurs due to the redistribution of the redox states in the $PEDOT:PSS$ line, where the concentration of $PEDOT^0$ gets very high in the first few hundred micrometres close to the negatively biased end [59]. As this region has a very high impedance compared to the rest of the line, almost all of the potential drops over this area. Further increases in the voltage only result in a higher potential drop over this area and thus not in an increase of current through the line. The cell is called dynamic because the redox states vanish as soon as the external potential is removed, as the reduced and oxidized areas are in direct contact with each other [58].

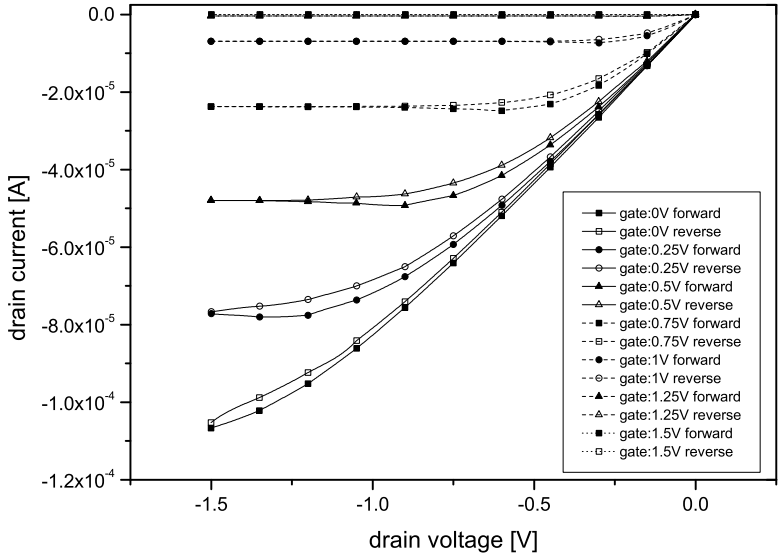

Figure 2.7.: Typical output characteristics of an *OECT*

2.4.4. Working principle

The *OECT* combines the behaviors of the bi-stable and the dynamic configuration. In accordance with *OTFT*s a channel with a channel length (L) and a channel width (W) is defined as the part of the source-drain line covered by electrolyte (compare Figure 2.6 a). Figure 2.6 b shows the electrical connections of the device. By applying a positive voltage to the gate the channel is reduced and thus the overall impedance is increased. A negative drain voltage drives the charge carriers through the channel, but also further reduces a part of the channel and thus allows for the distinctive transistor characteristics of linear and saturation regime [58]. Note that the needed voltages are not "symmetrical" (meaning they are not both positive or both negative), which has to be accounted for in circuitry. Figure 2.7 shows typical output characteristics of an *OECT*. Despite the very different working principle the electrical behavior is very similar to that of an *OTFT* (compare Chapter 2.2.4).

An important parameter is the area ratio between the electrolyte covered source-drain area (A_{SD}) and the electrolyte covered gate area (A_G). In order to fully reduce the channel the same amount of $PEDOT^0$ has to be present in A_G as

there is $PEDOT:PSS$ in A_{SD} (as the redox reaction is an equilibrium reaction) [58]. In its pristine state a $PEDOT:PSS$ film consists of approximately 80 % oxidized sites. Hence, an area ratio of $A_{SD}/A_G = 1/4$ is needed to fully reduce the channel, idealizing that every site is available for the reaction. In reality, area ratios of at least $1/10$ are needed to achieve reasonably high on-to-off current ratios [58]. Note that the resistance in the linear regime is unaffected by the area ratio, but the off-current as well as the saturation current are influenced [58]. To the best of the authors knowledge no quantitive model comparable to section 2.2.4 for $OTFT$s exists for $OECT$s. A qualitative model illustrating how saturation occurs in $OECT$s has been proposed by Robinson et al. [59] (compare section 2.4.3). Unfortunately, the model cannot be used to quantitatively model real transistor characteristics as "The [model] curves [...] have not been fit to the experimental data [...] because there are too many unknowns."[59]. Thus the authors conclude that in the proposed model "[...] the details to quantitatively predict the behavior of a real device are lacking [...]"[59]. Because of this limited practical relevance a detailed description of the model is omitted in this work.

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Part I.

Organic electrochemical transistors

3. Influence of geometry variations on the response of organic electrochemical transistors

Preamble

This whole chapter has been published by P. C. Hütter, T. Rothländer, A. Haase, G. Trimmel and B. Stadlober in the journal Applied Physics Letters, Vol. 103. (2013) 043308. The version shown here is the final manuscript as submitted by the authors prior to final composition by the editorial office. For improved consistency with this thesis the original manuscript has been graphically recomposed. This included the addition of captions for improved readability. The full paper can be found in Appendix A.

The paper evolved from the diploma thesis of P. C. Hütter, titled "Inkjet Printed Electrochemical Transistors and Inverters". T. Rothländer supervised the research project and acted as the single corresponding author of the paper. Process development, sample preparation and all results for the electrochemical transistors have been achieved in close cooperation by P. C. Hütter and T. Rothländer. The experiments were designed by T. Rothländer, B. Stadlober and P.C. Hütter. A. Haase, G. Trimmel and B. Stadlober supported the work with inputs to overcome arising challenges. All samples for the sheet resistance analysis have been prepared and measured by P. C. Hütter. The idea of investigating the

influence of geometry parameters on the performance of *OECT*s was proposed by B. Stadlober. The first manuscript and the figures were prepared by P. C. Hütter. It was then improved in close cooperation with T. Rothländer. All other co-authors revised the manuscript. Reuse of the published results in accordance with the APL Copyright and Consent Form (Appendix B).

3.1. Abstract

We report on the fabrication and characterisation of entirely inkjet-printed organic electrochemical transistors (*OECT*s) based on poly(3,4-ethylene dioxithiophene) poly(styrenesulfonate) (*PEDOT* : *PSS*). These transistors were used to evaluate the assumed geometry-performance relationship of *OECT*s by changing the transistor dimensions and monitoring the output characteristics. We could show that the on-current depends on the *PEDOT* : *PSS* thickness and that the on-to-off current ratio is related to the distance between the printed electrodes. Taking these results into account, we fabricated entirely inkjet printed electrochemical inverters with a switching time of about 4 seconds. These inverters outline a first step from organic electrochemical transistors towards logic circuits.

3.2. Introduction

Since the discovery of conducting polymers in the late 70's a lot of research activities in polymer science aimed at developing printed electronic circuits, which combine multifunctional materials with low-cost production and a versatile form factor [1]. The key elements of any electronic circuit are transistors and resistors. There are two main concepts to build transistors based on organic materials: organic thin film transistors (*OTFT*) and organic electrochemical transistors (*OECT*). The simplest way to realize both organic resistors and organic transistors is based on printable conjugated polymers that can be used as printed resistors or if combined with electrolytes form an *OECT*. One well known example of such a polymer is *PEDOT* : *PSS* (poly(3,4-ethylenedioxithiophen) poly(styrenesulfonate)) which shows electrochemical switching over five orders of magnitude [2] via a voltage-induced reversible redox process. *OECT*s have several advantages compared to organic thin film transistors. First, due to the absence of a gate dielectric, the charge carrier transport is not determined by

the often imperfect quality of the interface between semiconductor and gate dielectric, which leads to trapping and performance instabilities. Second, due to the high capacitance of the electrolyte their operating voltage is very low, allowing for a switching of the *OECT*s in the range of 1 V and below. Third, only few materials and a very simple design are needed for *OECT*s thus decisively simplifying the printing process. Finally, they act as an ideal platform for the integration of electronic and biological systems, because of their unique ability to conduct both electronic and ionic carriers. Due to all these advantages, electrochemical transistors increasingly find their application in cell transport measurement [3], circuitry for disposable electronics [4], active-matrix physical sensor circuits [5] and in chemical [6] and biological sensors [7, 8]. A comprehensive overview of *OECT*s and *OTFT*s for chemical and biological sensing is provided in literature [9].

An inherent characteristic of *OECT*s is that a positive input voltage is needed to switch the transistor, resulting in a negative output voltage. This makes it impossible to drive a transistor with a preceding one [4]. To shift the negative output voltage to positive values, a voltage divider connected to the output of the transistor is needed. This combination of an *OECT* and a voltage divider is working as an electrochemical inverter, generating an output signal of logic 1 when the input is 0 and logic 0 when the input is 1. One major drawback of *OECT*s is their low switching speed which is a result of the intrinsically low mobility of the ions in the electrolyte and the limited speed of the redox reaction. We assume that the geometry of the device also has a substantial influence on the transistor speed. Although the general working principle of *OECT*s was investigated intensively [10–13], there exists no comprehensive work on the geometry-performance relationship of *OECT*s; only the influence of the ratio between the gate area A_G and the source-drain area A_{SD} on the I(V) curves was investigated [14, 15]. Additionally a faster response time of *OECT*s when the length of the source-drain line is decreased was observed [16]. The latter was also shown for transistors used in biosensing [17].

Accordingly, we examined the effect of varying the transistor geometry on the IV-curves of printed *OECT*s in a systematic way. The *OECT*s were fabricated by inkjet printing and had a lateral configuration (see Fig.3.1a). The optimized geometry of the *OECT*s was implemented in the fabrication of printed inverters which serve well to showcase the effect of fundamental *OECT* parameters in practical applications. These inverters are composed of high performing *OECT*s and *PEDOT* : *PSS* resistors, based on only three inks (*PEDOT* : *PSS*, Silver, Electrolyte), and exhibit a gain of 2.7.

3.3. Experimental

The gate electrode and the source-drain line of the transistor are formed by inkjet printing of *PEDOT* : *PSS* on PET substrates. A silver pad ensures good contact between the electrodes and the measurement circuits. A cationic electrolyte is applied by inkjet printing between gate and channel, thus covering parts of the source-drain line and the gate electrode. The voltage divider which is used to form an inverter is printed with *PEDOT* : *PSS* and silver ink. As the substrate for all devices we use untreated Melinex ST725 PET (polyethylene terephthalat) foil from DuPont®. Inkjet printing processes are done with the Fujifilm® Dimatix Material Printer DMP 2800 with Dimatix DMC 11610 printing cartridges. The substrate temperature during printing is 40 °C for *PEDOT* : *PSS* and silver ink. The *PEDOT* : *PSS* Clevios P Jet HC from H.C.Starck® is filtered with a 0.2 µm PET filter. The silver is processed either by hand (Electrolube® silver conductive paint) or by inkjet printing. The inkjet printed silver Cabot® CCI-300 is sonicated for 15 minutes and filtered with a 0.2 µm PET filter before use. After printing, the ink is sintered on a hot plate for 30 minutes at 100 °C. The electrolyte is also applied either by hand or by inkjet printing. When inkjet printed, 20 layers of electrolyte are applied on the substrate at ambient temperature. The used polyelectrolyte formulation consists of: 51 wt% deionized water, 33 wt% Poly(sodium-4-styrene sulfonate), 8 wt% D-sorbitol and 8 wt%

glycerol (85 wt%), as found in literature [18]. For electrical characterization a Suess Microtec® probe station and a MB Technologies® parameter analyzer are used and for the dynamic measurements a Thurlby Thandar Instruments® TG230 frequency generator and a Tektronix® TDS 2014 B oscilloscope. The different thicknesses of the layers are measured with a Dektak Profilometer by Bruker. All process steps are carried out under ambient conditions.

3.4. Results and Discussion

Three different geometry parameters of $OECT$s were investigated (Fig. 3.1a). First the thickness T of the $PEDOT:PSS$ electrode was varied by increasing the number of printed layers of $PEDOT:PSS$. Then the gap G between the gate and the source-drain line was tuned. Finally, different line widths W were investigated. While modifying the geometry parameters of the devices, the ratio of the active area (area covered with electrolyte) between the gate electrode A_G and the source-drain line A_{SD} (see Fig.3.1a.) was held constant at a ratio of 10:1. Thus the reported influence of the area ratio on the on-to-off ratio could be excluded [15]. From the I_D (V_{DS})-characteristics basically two parameters were extracted and compared w.r.t the device geometry - the on-current I_{ON} (I_D at $V_{GS} = 0V$, $V_{DS} = -1V$) and the on-to-off ratio I_{ON}/I_{OFF} (with $I_{OFF} = I_D$ @ $V_{GS} = -V_{DS} = 1V$). In Fig. 3.1b a typical I_D-V_{DS} curve of an organic electrochemical transistor with inkjet printed $PEDOT:PSS$ and non-optimized geometry is displayed. From the on-current $I_{ON} = -6.48 \times 10^{-6}$ A and the off-current $I_{OFF} = -6.54 \times 10^{-8}$ A an on-to-off ratio of 1×10^2 is extracted. Between forward and reverse drain voltage sweep a clockwise hysteresis in the drain current is observed which results from the slow motion of the ions during the switching process; the respective gate switching current is also plotted in Fig.3.1b and is in the order of 1×10^{-7} A. The electrodes' thickness T of transistors with nominal line widths W = 10 µm, 50 µm, 100 µm, 250 µm and a gap G = 1500 µm was modified by multiple printing of $PEDOT:PSS$ layers. Thickness values

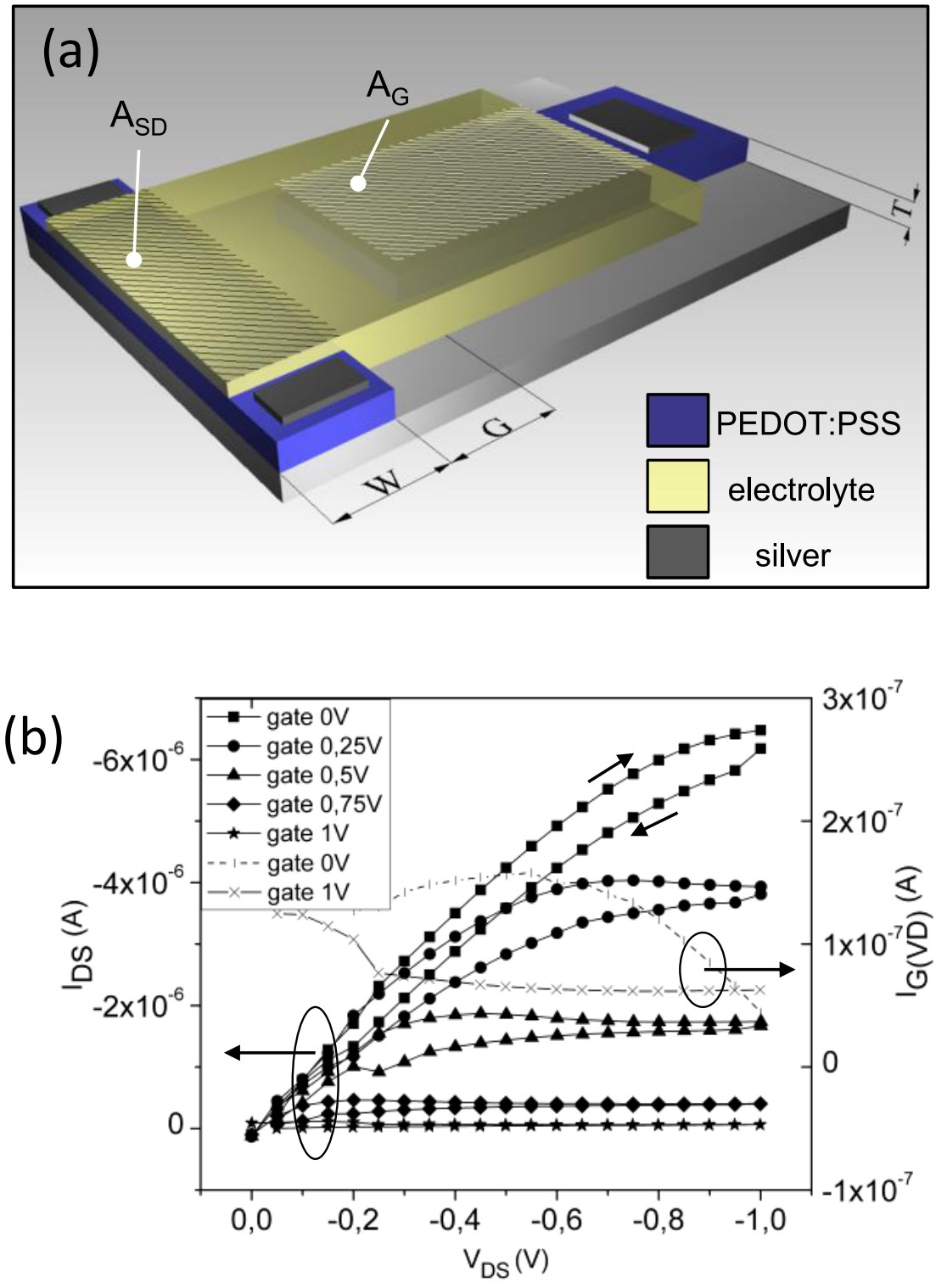

Figure 3.1.: a) Architecture of a lateral OECT, the varied geometry parameters are (i) the thickness T of the PEDOT:PSS electrodes, (ii) the gap G between the gate electrode and the source-drain line and (iii) the width W of the source-drain line b) Output characteristics of an OECT with a non-optimized geometry ($W = 100\,\mu m$, $G = 1500\,\mu m$, $T = 180\,nm$) and an area ratio $A_G/A_{SD} = 10:1$, the gate current is plotted for $V_{GS} = -1\,V$ and $V_{GS} = 0\,V$.

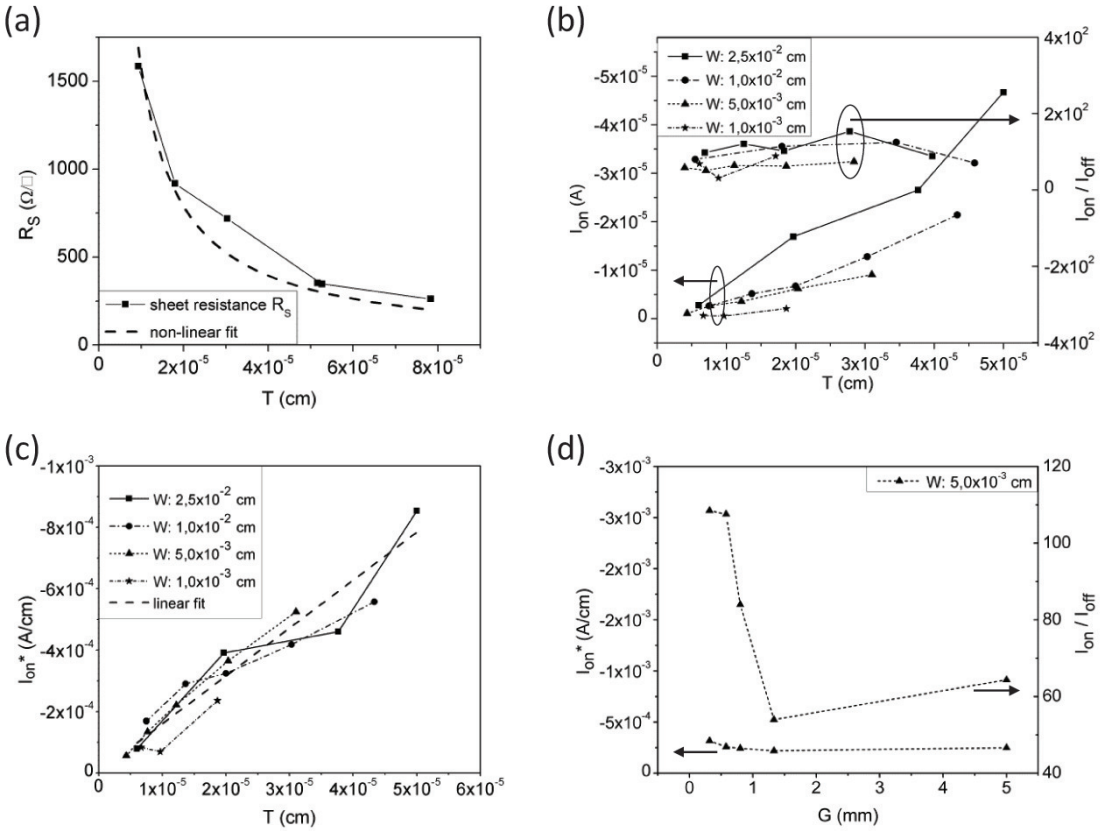

Figure 3.2.: a) Dependence of sheet resistance R_S on $PEDOT:PSS$ thickness T; fit-equation $R_S = 0.015\,78 \times T^{-1}$ b) Dependence of the on-current I_{ON} and of the on-to-off ratio on the line thickness T c) Dependence of the normalized on-current I_{ON}* on the line thickness T; I_{ON} is normalized to the widths of the source-drain lines W*; fit-equation $I_{ON}{}^{*} = -15.601\,58 \times T$ d) Dependence of the on-current and the on-to-off ratio on the gap G for transistors with $W = 0.05\,\text{mm}$ and $T = 120\,\text{nm}$.

between 40 and 75 nm were obtained for one layer of printed $PEDOT:PSS$. For two, three, five and seven layers of successively printed $PEDOT:PSS$, thickness values up to 450 nm were achieved. It can be assumed that a variation of T results in a change of the electrical properties of the $PEDOT:PSS$ electrodes such as the conductivity (Fig. 3.2a). A decrease of the sheet resistance R_S with increasing thickness values T is observed, following the expected 1/T dependence [19]. From $R_S = \rho/T$ a resistivity of $\rho = 0.015\,78\,\Omega\,\text{cm}$ is deduced, which corresponds to a conductivity of $\sigma = 63\,\text{S}\,\text{cm}^{-1}$ of the printed $PEDOT:PSS$ layer. The effect of varying T on the $OECT$ parameters is plotted in Fig. 3.2b-c.

The on-current I_{ON} increases approximately linearly with the line thickness T (Fig. 3.2b) being consistent with the 1/T decrease of the sheet resistance. Since the linear I_{ON}(T) correlation is valid for lines with different width W, the normalized I_{ON}*(T) curves collapse together (Fig. 3.2c). Here I_{ON}* corresponds to I_{ON} divided by the actual line width W*; the latter can differ from the nominal line width W due to the limited alignment accuracy and the spreading of the $PEDOT:PSS$ ink. The linear fit to the normalized on-current results in $I_{ON}{}^{*} = -15.6 \times T$. In a simple model I_{ON}* can be calculated from the linear part of the I(V) curve according to $I_{ON,calc}^{*} = V/(R_S \times L) = (V/L) \times \sigma \times T$. In our example, $L = 2.5\,\text{cm}$ is the length of the printed S-D line, $V = -0.7\,\text{V}$ is the voltage range of the linear I(V)-part. Taking the conductivity $\sigma = 63\,\text{S}\,\text{cm}^{-1}$ from the fitted sheet resistance in Fig. 3.2a $I_{ON,calc}^{*} = -17.6 \times T$ which is very close to the fitted I_{ON}* line.

The on-to-off ratio seems to be independent of T, meaning that I_{OFF} increases with T equivalently to I_{ON} (Fig. 3.2b). The same observation holds for the dependence of the on-to-off ratio on the width W. A possible explanation for this might be the slower reduction of the $PEDOT:PSS$ in the deeper regions of the source-drain line and in regions farther away from the gap edge. This leads to a graduation of reduced material during the measurement with mostly unreduced, high conducting material on the bottom of the line and fully reduced material on the top of the line, resulting in a higher overall off-current. This so-called reduction front is moved from the top towards the bottom of the line by the gate field and from the gap-sided electrode edge to the other. We can conclude that it is possible to increase the on-current by increasing the $PEDOT:PSS$ line thickness T (and the width W), but the on-to-off ratio remains virtually unchanged.

Next, the influence of the gap G on the device performance is examined. All $OECT$s in this experimental setup had a nominal line width $W = 50\,\mu\text{m}$ and a thickness $T = 50\,\text{nm}$ (optimized values). G was varied between 500 µm and 5 mm. The magnitude of the on-current does not depend on G (Fig.3.2d) which

can be expected since the on-current is measured with no gate voltage applied. So there should be no influence of the current on the distance between the gate and the source-drain line. However, the on-to-off ratio clearly increases for small G values (Fig.3.2d). This observation can be explained as follows: When the gap is small enough, the redox reaction time is sufficient to reduce the entire width of the source-drain line within one measurement cycle and the transistor can be switched off much better. An additional requirement for achieving a complete switch-off is a gate potential that is big enough to move the cations all across the source-drain line and cause a reduction of the whole line width. These two preconditions lead to a low off-current. Assuming a constant on-current, transistors with smaller gaps reach higher on-to-off ratios than transistors with larger gaps.

For the printing of the electrolyte, its viscosity had to be adapted and the minimum electrolyte volume for achieving satisfactory *OECT* characteristics had to be determined. It turned out that a minimum of 20 layers of electrolyte (50 µm thickness) is needed and that a 1+3 solution of electrolyte in deionized water is optimal w.r.t high precision splash-free printing. For printed inverters transistors with high on-to-off ratios rather than high on-currents are needed. Therefore, we chose a geometry of the all-inkjet printed *OECT*s with a small gap value (G = 500 µm) and a source-drain line width W = 250 µm with only one layer of *PEDOT : PSS*. Their output characteristics (Fig.3.3a) reveal $I_{ON} = -4.5 \times 10^{-5}$ A and $I_{OFF} = -2.7 \times 10^{-8}$ A, leading to an on-to-off ratio of 1.6×10^{3} which is more than one order of magnitude higher than what has been achieved for devices with non-optimized geometry. The lower hysteresis may indicate a higher switching speed compared to transistors without optimized geometry (compare Fig.3.1b)

Based on this design rule electrochemical inverters were fabricated with the aim to determine the switching speed of the *OECT*s. As pointed out in the beginning, a voltage divider has to be printed and connected to the output of the transistor (Fig.3.3b). This voltage divider is made of *PEDOT : PSS* and

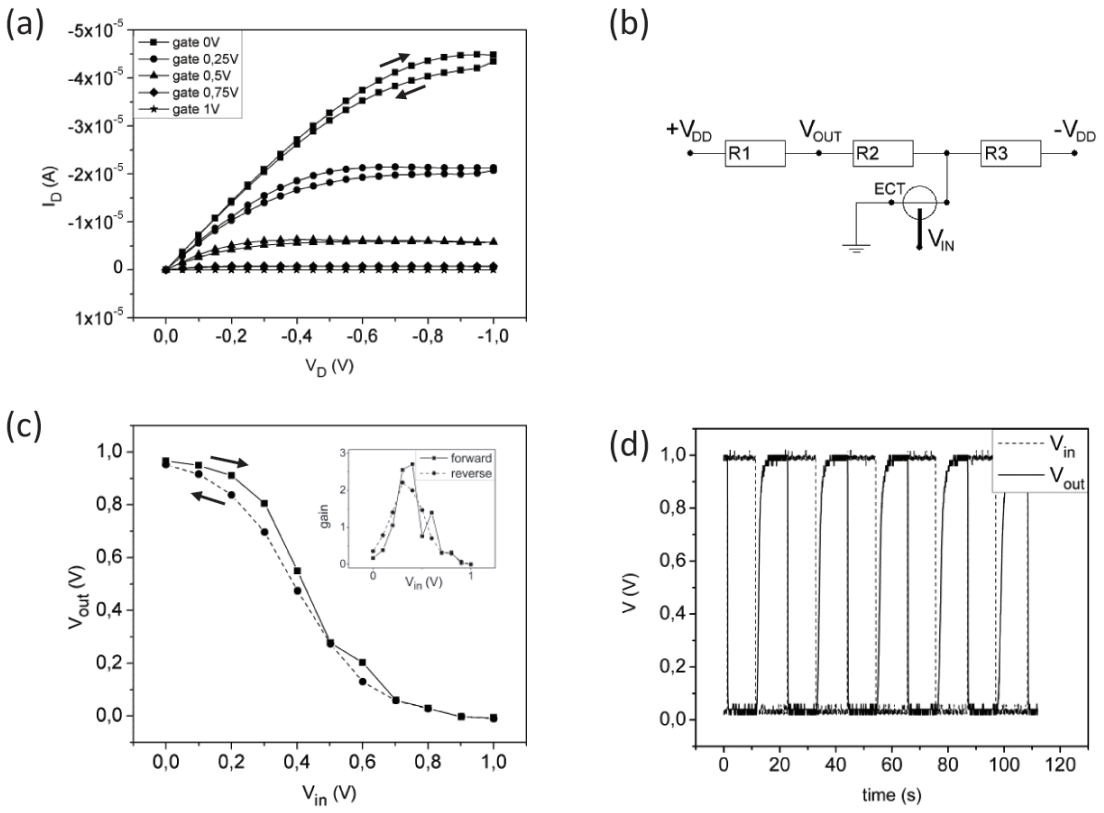

Figure 3.3.: a) Output characteristic of an entirely inkjet printed OECT with $W = 250\,\mu m$, $G = 500\,\mu m$, $T = 70\,nm$ and an area ratio between the gate electrode and the active area on the source-drain line of 12:1 b) circuit diagram of an electrochemical inverter c) Transfer characteristic of an entirely inkjet printed inverter; Inset: Gain of the inverter d) Response characteristics for an electrochemical inverter

printed silver pads, the latter used to define the magnitude of resistance of the three needed resistors by their length. Considering the switch-on resistance of the transistor $R_{ON} = 32\,k\Omega$ and the switch-off resistance $R_{OFF} = 18\,M\Omega$, resistors with $R1 : R2 : R3 = 427\,k\Omega : 280\,k\Omega : 154\,k\Omega = 7.93 : 5.20 : 2.86$ in length ratios were printed. For such a geometry and a symmetric voltage supply of $+V_{DD} = +3\,V$ and $-V_{DD} = -3\,V$ (see [8]), an output voltage of $1\,V$ when the transistor is switched on and $0\,V$ when it is switched off can be achieved. The transfer characteristics of such all-ink-jet printed inverters show clear plateaus at the high and the low level (Fig. 3.3c). The voltage of the high level (transistor = on) is $V_{out} = 0.97\,V$ and the voltage of the low level (transistor = off) is

$V_{out} = -0.01\,\mathrm{V}$, almost reaching the theoretical voltage levels. Moreover, the gain of 2.7 (Fig. 3.3c inset) is comparable to values reported in literature [4]. In general, these transfer characteristics confirm that the ratio of the resistors as well as the supply voltages are appropriate and that the chosen design can be considered as functional. Concerning their dynamical behavior a typical response to a square wave input signal with a frequency of 0.05 Hz is shown in Fig. 3.3d. The high and low levels of 1 V and 0 V are constant for a measuring period of 110 seconds and also a fast response of the output voltage V_{out} on V_{in}, depicted by a very small shift of the two signals, is visible. Additionally, a speed difference in switching the transistor on and back off is observable. The switching speed of the inverter is determined by graphic extraction, resulting in a switch-on time of 3.3 seconds to achieve 0.9 V and a switch-off time of only 0.4 seconds to achieve0.1 V. An explanation for this mismatch may be the edge of the reduction front. During the reduction process it is possible that this front is moving beyond the electrolyte edge towards the drain electrode. In this case the reverse process of oxidizing the PEDOT and returning to the conducting state of $PEDOT:PSS$ takes more time because the electrolyte, triggering the reaction, is not in direct contact with the PEDOT. The total switching speed is 3.7 seconds, when the on- and off-switching times are added, being in the same order of magnitude as reported for non-printed inverters with lateral design [4].

3.5. Conclusion

In summary, our investigations on lateral all-printed $OECT$s concerning their geometry-performance relationship have shown that the on-current increases with the $PEDOT:PSS$ layer thickness and - less pronounced - the width and that the on-to-off ratio increases substantially with a smaller gap between gate and source-drain area. We assume that reducing the gap to even smaller dimensions will further increase the on-to-off ratio. This will be investigated

in future studies with structuring methods like nanoimprint lithography. The ink-jet printed inverters that account for these design rules show convincing on-off switching behavior. As logic gates they will soon form the base for more complex circuits such as flip-flops and shift registers. Since only three materials are needed to realize these circuits in a very straightforward process, they have a strong potential for mass-fabricated low-cost and disposable electronics.

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4. Nanoimprint Lithography Structured Organic Electrochemical Transistors

Preamble

This chapter has been published by Thomas Rothländer, Philipp C. Hütter, Elisabeth Renner, Herbert Gold, Anja Haase, and Barbara Stadlober in the journal IEEE Transactions on Electron devices, Vol. 61 (2014) 1515. The version shown here is the final manuscript as submitted by the authors prior to final composition by the editorial office. For improved consistency with this thesis the original manuscript has been graphically recomposed. The full paper can be found in Appendix A.

The NIL structuring process was developed by T. Rothländer and improved by P.C. Hütter. The transistor measurements have been done by T. Rothländer. P. C. Hütter fabricated and measured the inverters. The NAND gates were produced and characterized by Elisabeth Renner and P. C. Hütter, assisted by T. Rothländer. H. Gold designed the stamps used for the nanoimprint lithography. A. Haase and B. Stadlober supported the work with crucial inputs to overcome arising challenges. The idea of combining *NIL* and *OECT*s was proposed by B. Stadlober. The first manuscript was written by T. Rothländer, who also prepared all figures. All co-authors helped to improve the manuscript. The proposed

changes by the co-authors have been implemented by T. Rothländer, who is also corresponding author of the work. The research project was supervised by T. Rothländer. Reuse of the published work in accordance with the IEEE Copyright and Consent Form (Appendix B).

4.1. Abstract

We report on the fabrication of organic electrochemical transistors structured by nanoimprint lithography. The devices were scaled down as a consequent result of our previous findings for inkjet printed transistors, where a reduced source-drain width and a shorter distance to the gate resulted in higher on-to-off current ratio. We could show that these findings also prove true for transistors with feature sizes below 10 µm. Furthermore, we fabricated inverters and NAND gates with switching times below one second. These logic gates mark an important step for organic electrochemical transistors towards their usability in more complex logic circuits.

4.2. Introduction

There are two main concepts to build organic transistors: the organic thin-film transistor (*OTFT*) and the organic electrochemical transistor (*OECT*), the latter being studied in this work. Using an electrolyte and the well-known conducting and printable polymer *PEDOT* : *PSS* (poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate)), electrochemical switching over five orders of magnitude via a voltage-induced reversible redox process has been shown and exploited in *OECT*s and circuits thereof [1]. Naturally, their performance depends heavily on the used materials, but different geometry parameters also play a significant role [2–4]. We could show for all-inkjet-printed *OECT*s that the on-to-off current ratio can be improved by reducing the width of the source-drain electrode (width W) and its distance to the gate (gap G) [5] (compare Fig. 4.1a). In this work, we aim to further exploit this relation by fabricating devices with a higher resolution than provided by inkjet printing. Thus it is necessary to pattern the *PEDOT* : *PSS* electrodes with minimum feature sizes of 10 µm and below. Different approaches to achieve this goal have been shown in literature. One technique is to rely on a previous surface treatment of the substrate, using

structured hydrophobic layers [6], CF4 etching [7] or self-assembled monolayers and V-shaped, embossed groves [8]. The methods are promising for producing feature sizes well below one micrometer, but the first two require a very good control over the drop volume to achieve thin layers while the third one requires a quite complicated, high resolution surface treatment. *PEDOT : PSS* can also be mechanically structured, either by laser ablation [9], oxygen plasma etching using a stainless steel mask [10] or photolithography and lift-off [11]. However, in the context of low cost production a roll-to-roll compatible, parallel structuring technique would be advantageous. Accordingly we introduce UV-based nanoimprint lithography (UV-NIL) as a high resolution, high throughput patterning technique to structure *PEDOT : PSS*. Devices with a gap of $G = 6\,\mu m$ and a width of $W = 13\,\mu m$ were fabricated and measured. Full usability of the NIL-structured electrochemical transistors (NIL-OECTs) in higher integrated logic circuitry is demonstrated on the basis of inverters and NAND gates. Furthermore, the transistors are compared to our previously published all-inkjet printed *OECT*s in terms of static and dynamic behavior.

4.3. Experimental

The *OECT*s presented here consist of *PEDOT : PSS* (Clevios P Jet HC by Heraeus) an inkjet printable polymer electrolyte and silver ink (Cabot® CCI-300) for the contact pads. The electrolyte formulation consists of: 51 wt.% deionized water, 33 wt.% Poly(sodium-4-styrene sulfonate), 8 wt.% D-sorbitol, and 8 wt.% glycerol (85 wt.%) [12]. As shown in Figure 4.1b-g on an SF6 plasma treated PET foil (Melinex ST725 PET foil from DuPont®) the *PEDOT : PSS* electrodes are pre-structured by inkjet printing using a Dimatix DMP 2800 inkjet printer. The substrate is held at room temperature during the printing process. The *PEDOT : PSS* film is dried on a hotplate held at 100 °C for 10 minutes. Next, a UV curable imprint resist [13] is spin-coated on top of the electrodes at 2000 rpm for 30 seconds. The resist is structured by UV-NIL using a silicon stamp and

curing the resist through the substrate with an EVG 620 mask aligner. After separating the stamp from the sample, the resist acts as an etch mask. With an oxygen plasma dry etch in a reactive ion etcher from Oxford Instruments the pattern is transferred from the resist into the $PEDOT:PSS$ lines. The sample is submersed in AZ 726 MIF photo developer (microchemicals GmbH) for 15 minutes and rinsed with IPA to remove the resist. To improve the electrical connection to the measurement tips, Ag contact pads are inkjet printed onto the electrodes at room temperature and cured at 110 °C for 10 minutes on a hotplate. As a last step the electrolyte is applied, again using inkjet printing [14].

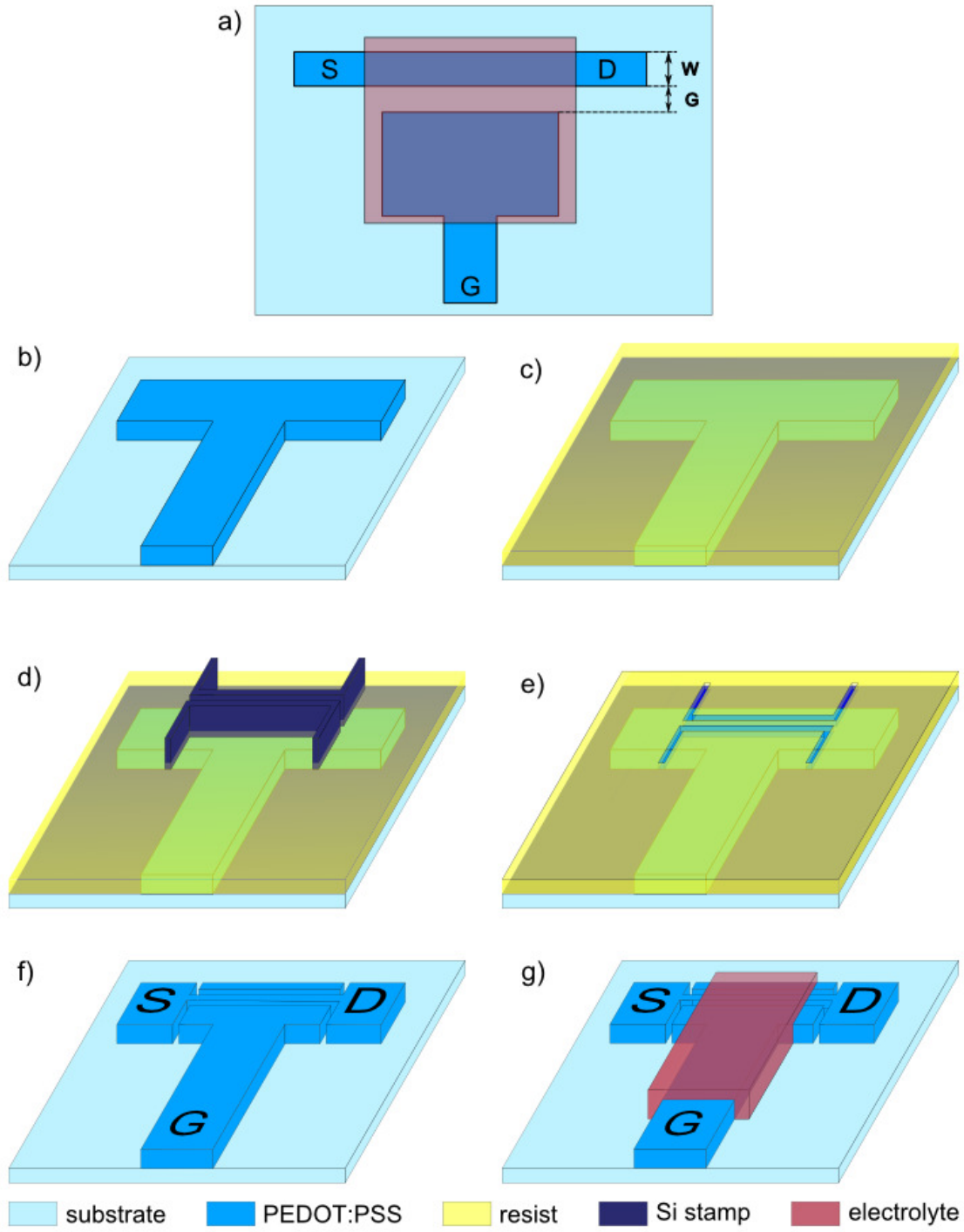

Figure 4.1.: Schematic top view (a) and NIL-process scheme (b-g) of a lateral electrochemical transistor; Definition of the gap between the gate and the source-drain line G and the width of the source-drain line W (a). On a sample with pre-structured PEDOT:PSS (b) an imprint resist is applied by spin coating (c). Then a Si stamp with the wanted features is pressed into the resist (d), the resist is UV-cured through the substrate and the stamp is removed, leaving an etch-mask for the underlying PEDOT:PSS (e).The etch pattern is transferred using an oxygen plasma etch and the resist is wet chemically removed (f). As a last step the electrolyte is inkjet printed on the sample (g).

4.4. Results and Discussion

4.4.1. Nanoimprint lithography structured electrochemical transistor and logic gates

From Figure 4.2, showing the output characteristics of a typical NIL-OECT with a gap of 6 µm and a width of 13 µm, the on current I_{ON} (I_D at $V_{GS} = 0\,\mathrm{V}$, $V_{DS} = -1\,\mathrm{V}$), the off current I_{OFF} (I_D at $V_{GS} = 1\,\mathrm{V}$, $V_{DS} = -1\,\mathrm{V}$), and the on-to-off current ratio I_{ON}/I_{OFF} can be extracted. The shown device reveals $I_{ON} = 6.4 \times 10^{-7}\,\mathrm{A}$, $I_{OFF} = 1.0 \times 10^{-10}\,\mathrm{A}$ and $I_{ON}/I_{OFF} = 6.4 \times 10^{3}$. Peak devices showed an even higher ratio of up to 1×10^{4}. The maximum switching current ($I_{G,max}$) is $I_{G,max} = 1 \times 10^{-10}\,\mathrm{A}$ and the largest hysteresis at $V_{GS} = 0\,\mathrm{V}$ reaches 13 % of I_{ON}. The hysteresis is a result of the ions present in the electrolyte. As a next step, all-printed NIL-structured OECT-based inverters using the circuit design shown in Figure 4.3a were investigated. For the resistors inkjet printed $PEDOT:PSS$ is used. In order to reduce the footprint of the circuit, the resistors are also structured by NIL. Ideally, the circuit acts as a voltage divider between either $R3$ and $R1 + R2$ for a switched off OECT or $R3$ and $R2 + R_{ON}$ for a switched-on OECT. In reality, the parallel resistances of R_{ON} and R_{OFF} ($R_{OFF} = R_{ON}$ at $V_{GS} = 1\,\mathrm{V}$) have to be taken into account. For the proper function it is important that $R_{OFF} > R1 > R_{ON}$. Considering the on- and off-resistances of the transistor (compare Fig.4.2) ($R_{ON} = 875\,\mathrm{k\Omega}$, $R_{OFF} = 3\,\mathrm{G\Omega}$) and symmetrical supply voltages ($V_{DD} = 3\,\mathrm{V}$, $-V_{DD} = -3\,\mathrm{V}$) resistances of $R1 : R2 : R3 = 15\,\mathrm{M\Omega} : 25\,\mathrm{M\Omega} : 40\,\mathrm{M\Omega}$ should result in good inverter performance. Alternatively the supply voltages can be adjusted to compensate for a mismatch in the resistance ratios. One solid NIL-structured resistor line was fabricated and divided into the needed length parts by inkjet printed Ag contact pads. For the inverter shown in Figure 4.3c the resistances revealed $R1 : R2 : R3 = 6\,\mathrm{M\Omega} : 16.6\,\mathrm{M\Omega} : 37.7\,\mathrm{M\Omega}$ and the supply voltages were adapted to $V_{DD} = 4.0\,\mathrm{V}$ and $-V_{DD} = -2.1\,\mathrm{V}$ respectively. The

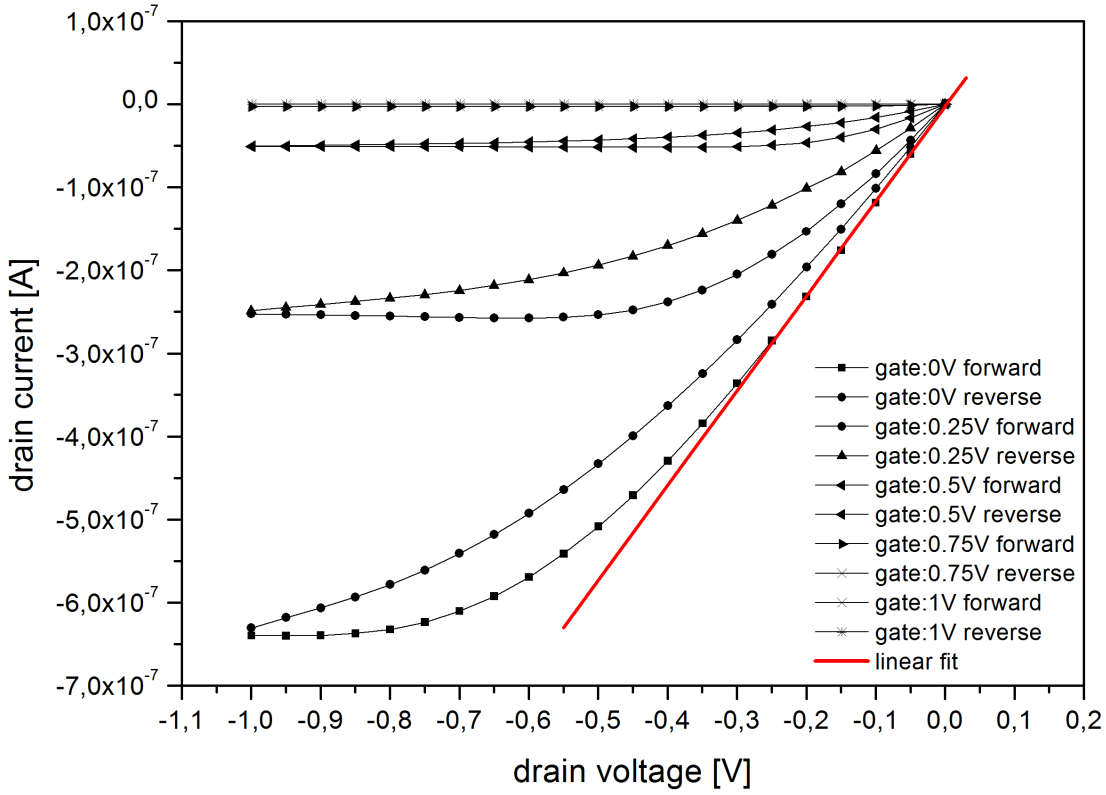

Figure 4.2.: Output characteristics of a NIL-structured electrochemical transistor. The width of the source-drain line $W = 13\,\mu m$ and its distance to the gate $G = 6\,\mu m$. From the slope of the linear fit $Ron = 875\,k\Omega$ can be extracted.

device has clear plateaus at the high and the low level. The voltage of the high level (V_{Output} at $V_{Input} = 0\,V$) is $V_{Output,high} = 0.94\,V$ and the voltage of the low level ($V_{Input} = 1\,V$) is $V_{Output,low} = -0.03\,V$. This result is in good agreement with the target voltage levels of $V_{Output,high} = 1\,V$ and $V_{Output,low} = 0\,V$. The extracted gain of 3.8 (Fig. 4.3c inset) is comparable to values reported in literature [1, 5].

To show that NIL-structured OECTs can be used for all Boolean logic operations, NAND gates are fabricated [15] (Fig. 4.3b). The dynamic response of the NAND-gate (Fig. 4.3d) shows good logic switching behavior, the $V_{Output,high}$ value (representing Logic 1) shows a slight instability with plateau values in the range of $V_{Output,high}$ =1.01 V to 0.86 V, however there is still a clear distinction to the low level state (Logic 0) being $V_{Output,low} = 0.02\,V$. The switching time was also

measured, revealing a mismatch between switching the device from the on- to the off-state ($t_{Off} = 0.03\,\mathrm{s}$) and back on again ($t_{On} = 0.9\,\mathrm{s}$) (Fig. 4.4c).

There are three different artifacts visible in the NAND characteristics that can also be found in literature [1]. The sharp peak labeled "1" in Figure 4.3d, when OECT1 is switched on and OECT2 is switched off, is a result of the mismatch of the switching times. As stated above, OECT2 switches off over 0.03 s, so for a short time both transistors are off. This results in the visible short drop of V_{Output} towards the logic 0 state. The $\Delta V_{Output} = 0.2\,\mathrm{V}$ drop in the logic 1 level when OECT1 is on and OECT2 is off (labeled "2" in Fig. 4.3d) is a result of the higher R_{ON} of OECT1 (and thus the higher parallel resistance to $R1$). The output characteristics of both OECTs used in the NAND gate can be found in the Appendix of this chapter (Fig. 4.5). The third artefact appears whenever OECT1 is switching off, especially pronounced when OECT2 is also off (labeled "3" in Fig. 4.3d). It is not a stable artefact but varies both in height and transistor number from device to device. It is only visible when the NIL-OECT switches off and in all devices most prominent when both transistors are switched off. The artefact is thought to be a result of parasitic capacitances between the gate and the source-drain line. When both transistors are off the parasitic capacitance is discharged through the voltage divider and thus results in a peak in V_{Output}. This is in good agreement with the smaller change in V_{Output} when only OECT1 switches off, since then part of the parasitic charge can flow over OECT2 to ground and the voltage divider is less affected.

4.4.2. Comparison with all inkjet printed organic electrochemical transistors

When compared to the all-inkjet printed transistors published elsewhere the on-current is two orders of magnitude lower for the NIL-structured devices (compare Fig. 4.4a,b) [5]. This is a result of the decreased device geometries, but also the process steps performed on top of the $PEDOT:PSS$. I_{ON} is lowered

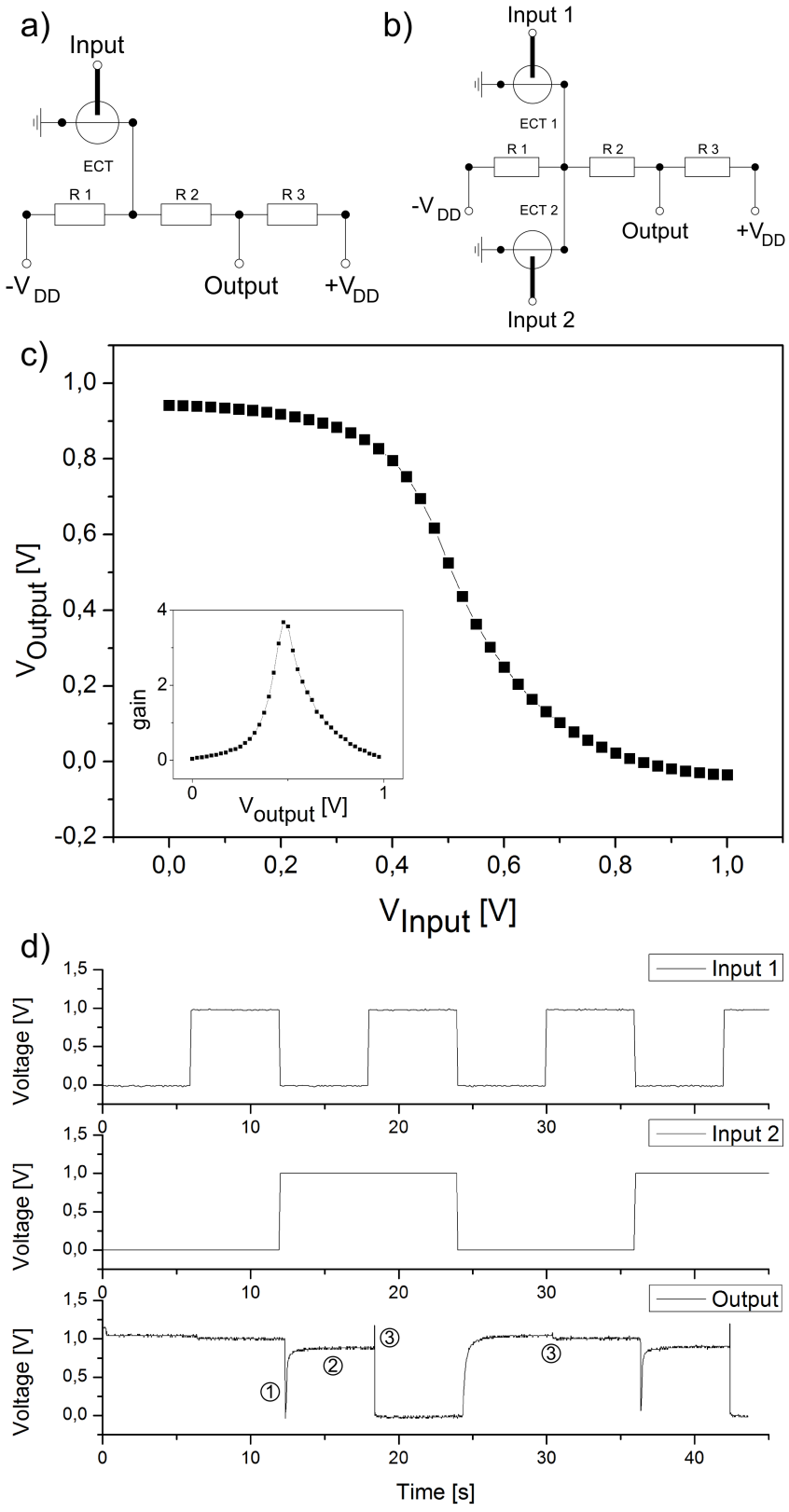

Figure 4.3.: Circuit design for an electrochemical inverter (a) and NAND gate (b)[1]; (c) inverter transfer characteristics with the gain as an inset; (d) Dynamic response of an electrochemical NAND gate to two square wave input signals. The highlighted artefacts (1-3) are described in detail in section 4.4.1.

because the width of the S-D line is one order of magnitude smaller. Also the sheet resistance of the $PEDOT:PSS$ lines rises significantly due to the exposure to the NIL process steps. A control experiment, where the sheet resistance of all-inkjet printed $PEDOT:PSS$ lines has been measured before and after being exposed to application, curing and stripping of the resist, revealed an increase from about 1 kΩ/square to 300 kΩ/square. On the other hand I_{ON} is increased because the length of the source-drain line is reduced from 20 mm to 1 mm. The $PEDOT:PSS$ thickness is in the same order of magnitude for both the all-inkjet printed and the NIL-structured devices, being around 100 nm. Despite the lower on-current the on-to-off ratio has improved up to one order of magnitude. This represents a further continuation of the trend, that reducing both width and gap has a positive influence on the transistor performance.

Concerning the dynamic behavior of the $OECT$s, the NIL-structured transistors show an overall switching frequency of approximately 1.1 Hz. Compared to the 0.27 Hz of the inkjet printed $OECT$s the switching speed only improved by a factor of four (compare Fig. 4.4c). This indicates that an effect different from the dimensions W and G seems to dominate the switching speed for small geometry devices. The reduction front moving beyond the electrolyte area and towards the drain electrode when switching the $OECT$ off may be this dominant effect [16]. When switching the device back on, this area takes a relatively long time to be oxidized again. This is supported by the dynamic behavior, which is heavily dominated by the time needed to switch the device from the off- to the on-state. While in all-inkjet printed OECTs the switching time ratio is $t_{On}/t_{Off} = 8.3$, the NIL-OECTs show a ratio of $t_{On}/t_{Off} = 30$. This explanation can be further backed by literature as switching speeds over 1 Hz have to the best of our knowledge only been reported for device geometries where this reduction front is suppressed (e.g. by replacing the $PEDOT:PSS$ not covered by electrolyte with a conductor [3, 17]) or not affecting the switching at all (e.g. in a vertical electrochemical transistor design [18]).

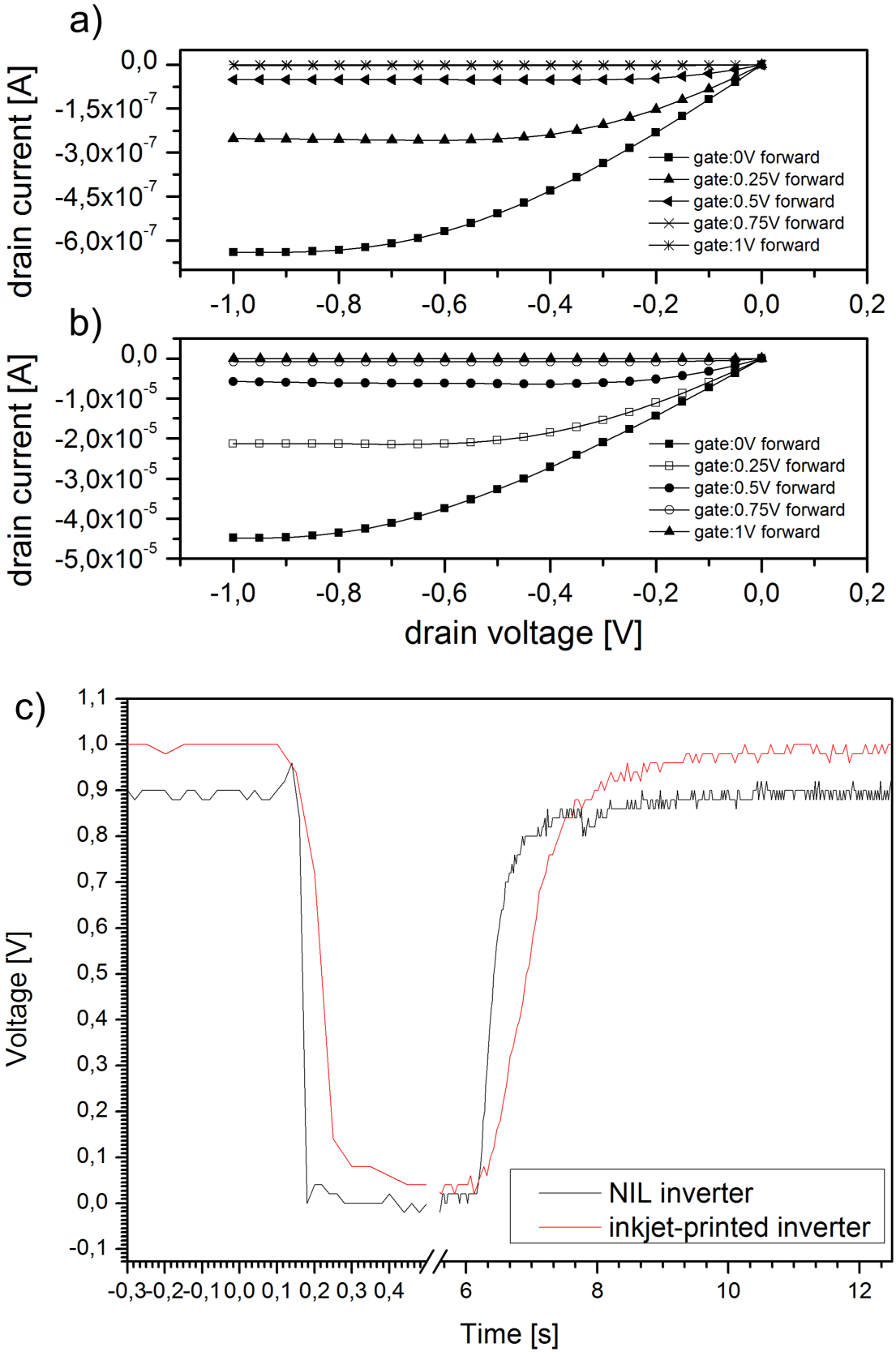

Figure 4.4.: Output characteristics of a NIL-structured (a) and an inkjet-structured (b) OECT; (c) Dynamic response of electrochemical inverters to a square wave signal. The switching times can be graphically extracted and read $t_{Off} = 0.9\,\mathrm{s}$, $t_{On} = 3.3\,\mathrm{s}$ (inkjet) and $t_{Off} = 0.03\,\mathrm{s}$, $t_{On} = 0.9\,\mathrm{s}$ (NIL).

4.5. Conclusion

To conclude we could show that it is possible to use nanoimprint lithography for the structuring of $PEDOT:PSS$ and fabricate fully-printed organic electrochemical transistors as well as logic circuits. By reducing the device geometry both the on-to-off current ratio and the switching speed were improved. The results indicate that further size reduction might not lead to better device performance, as other influences beyond the geometry start to dominate the dynamic transistor behavior. Future work will deal with the determination and evaluation of these influences (e.g. by suppressing the reduction front, modulating the gate area or comparing different electrolytes) for different device geometries. Nevertheless, we could show that lateral electrochemical transistors can exhibit good switching speeds and high on-to-off current ratio. With the successful fabrication of logic gates future application as flip-flops or shift registers and more complex devices with electrochromic displays can be addressed.

4.6. Appendix

Figure 4.5 shows the output characteristics of the two NIL-$OECT$s used for the NAND gate. The on-resistances can be calculated from the slope of the linear regime. For the devices R_{ON} equals $R_{ON,OECT1} = 3.9\,\mathrm{M\Omega}$ and $R_{ON,OECT2} = 1.8\,\mathrm{M\Omega}$ respectively.

4.7. Acknowledgment

T. Rothländer would like to thank E. Zojer for fruitfull discussions and advice.

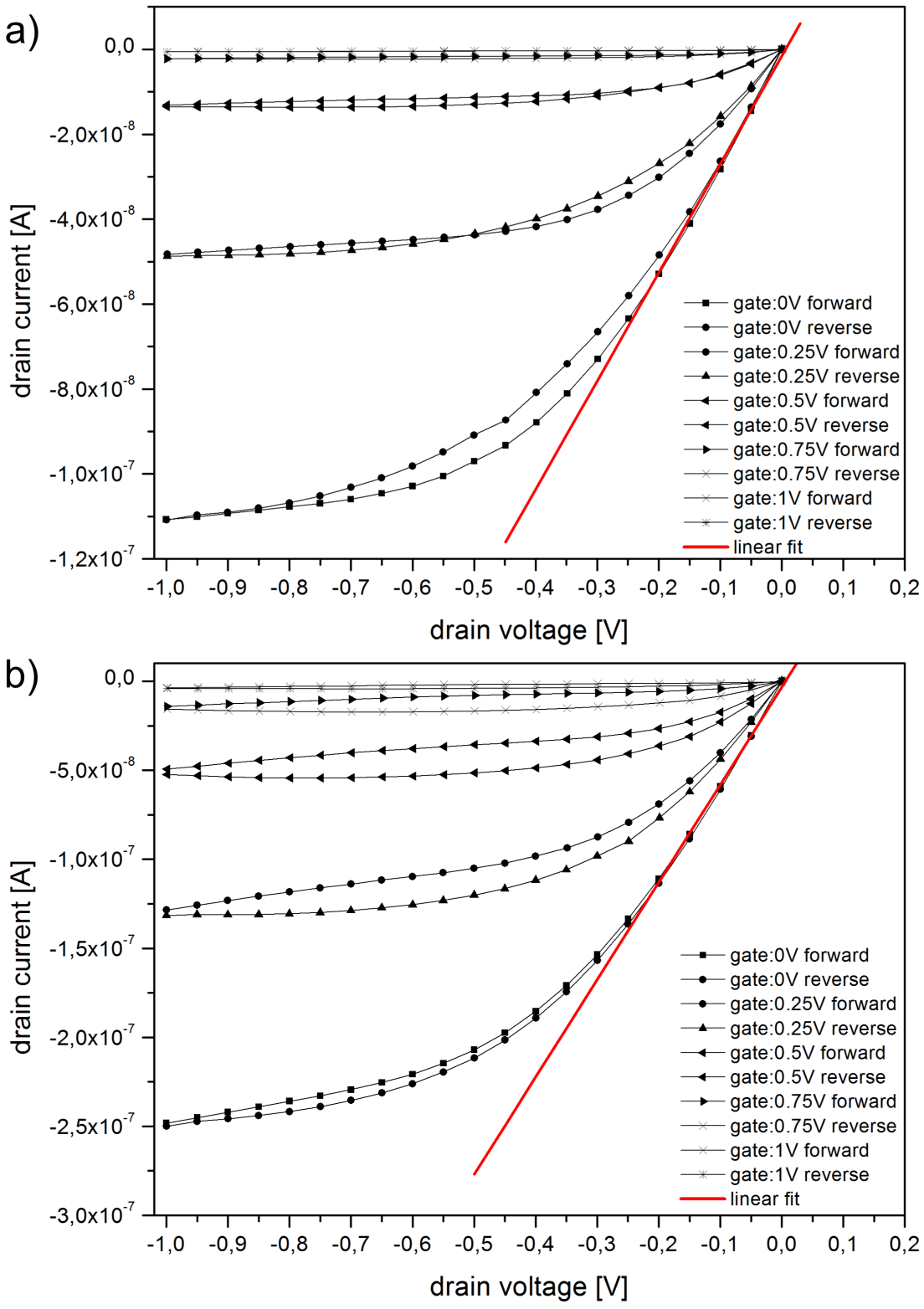

Figure 4.5.: Output characteristics of (a) OECT1 and (b) OECT2 used for the NAND-gate.

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Part II.

Organic thin-film transistors

5. Channel length variation in self-aligned, nanoimprint lithography structured OTFTs

Preamble

This chapter has been submitted by T. Rothländer, A. Fian, J. Kraxner, W. Grogger, H. Gold, A. Haase and B. Stadlober for publication in Organic Electronics. The version shown here is the manuscript revised in response to the reviewers as submitted by the authors. For improved consistency with this thesis the original manuscript has been graphically recomposed.

The *OTFT* structuring process using *NIL* has been developed by T. Rothländer and A. Fian. Transistor fabrication, measurement and data analysis has been performed by T. Rothländer. The cross section analysis was done by J. Kraxner, supervised by W. Grogger. H. Gold designed and fabricated the stamps for *NIL* structuring, A. Haase and B. Stadlober gave valuable input on the transistor data analysis. The idea of studying the short channel behavior in self-aligned, *NIL* structured *OTFT*s was proposed by T. Rothländer, who also designed the experiments. T. Rothländer prepared all figures and wrote the original manuscript except for the parts about the cross section preparation and results, which were written by J. Kraxner. The manuscript was then improved by all co-authors. All changes to the manuscript as a response to the reviewers have

been performed by T. Rothländer, except for the paragraphs on the DIBL effect and its influence on the onset voltage and the subthreshold swing, which has been written by B. Stadlober in close cooperation with T. Rothländer. T. Rothländer acted as the single corresponding author of the work and supervised the research project. Reuse of the manuscript in accordance with the Organic Electronics Copyright and Consent Form[1].

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5.1. Abstract

We report on the fabrication and characterization of self-aligned organic thin-film transistors with copper gate electrodes structured by nanoimprint lithography. The process has been improved to increase the compatibility with solution processed materials for future fabrication of fully printed, *NIL* structured transistors. We provide detailed analysis of the influence of the channel length on the fabricated devices. The on-current, the swing and the onset voltage are studied for channel lengths between 25 µm and 800 nm. The results indicate that for the given system a channel length of 5 µm results in the best device performance. This work marks a first step towards our goal of fabricating self-aligned *NIL OTFT*s consisting solely of printable materials.

5.2. Introduction

With the improvement of structuring processes for the fabrication of organic thin-film transistors, devices with channel lengths (L) far smaller than 100 nm have been shown [1–3]. In theory, the decreasing channel lengths should lead to improved device performance, especially concerning the increase of source-drain current and switching speed. Nevertheless, short channel effects due to contact resistance and the difficulty of adequate downscaling of other geometry parameters, notably the dielectric layer thickness and the overlap areas, compromise the theoretical improvements. Often devices with extremely small channel lengths even show deteriorated instead of improved performance. In order to benefit from the theoretical advantages of downscaling it is crucial to understand the influence of small L values on all significant organic thin-film transistor (*OTFT*s) parameters. Although many groups have studied the channel length dependence of the mobility [4–9], the threshold voltage [2, 5, 7, 9–12] and the on-resistance [4–6, 13–16] what exactly dictates the occurrence and the extent of short channel effects in *OTFT*s is still not fully understood. Haddock

and coworkers [10] compiled a selection of previously published transistors with comparable device geometries. Without an obvious reason some of the transistors showed strong short channel effects while others did not. Thus they concluded that for any given material system, layer sequence and fabrication process the influence of a channel length reduction on the device performance has to be studied separately in order to account for the interplay between the lateral and vertical electric field, the contact resistance and the parasitic contributions to the gate capacitance in a proper way.

In this work we study the change in the performance of *OTFT*s with minimized interlayer electrode overlap when reducing the channel length from 25 µm to 0.8 µm and try to identify an optimum channel length for the given device system. Special focus is put on parameters related to the threshold and sub-threshold transistor regime, namely the swing and the onset voltage. Additionally, the influence of L on the on-current is investigated. In the context of a future low cost production, a roll-to-roll compatible, parallel structuring technique is advantageous for the fabrication of organic thin-film transistors. Accordingly, all devices in this work are fabricated using nanoimprint lithography (*NIL*) as a high resolution, high throughput patterning technique.

In order to achieve a sufficient alignment of the *OTFT* electrode layers with dimensions down to the sub-µm range and to avoid high parasitic overlap capacitances, a self-aligned nanoimprint lithography process published by Palfinger et al. [17] was employed (see Figure 5.1). The process has been adapted in order to improve the compatibility with solution processed materials for future fabrication of fully printed, NIL structured transistors. Contrary to [17], copper is used as gate material instead of aluminum and the resist pattern is transferred to the gate metal layer by etch instead of lift-off.

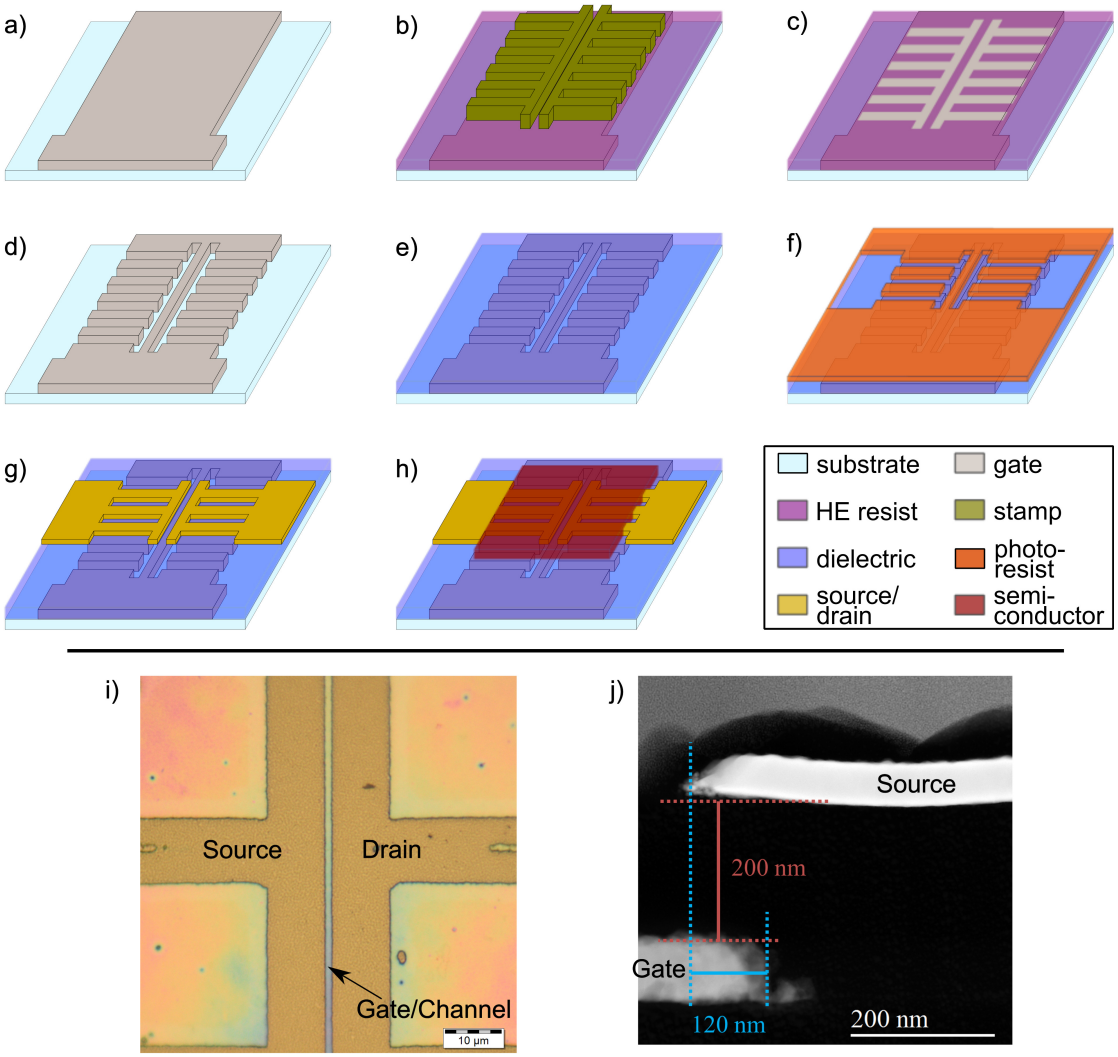

Figure 5.1.: Process scheme for a self-aligned, nanoimprint lithography structured OTFT: the gate metal is evaporated through a shadow mask (a); the gate pattern is transferred by pressing a silicon stamp into a hot embossing resist, heated over its glass transition temperature (b); the stamp is removed after cooling below the glass transition temperature of the resist, any residual resist layer in the structures is removed by an O_2 dry etch (c); after wet-etching of the metal the resist is stripped, with the NIL structured gate remaining (d); a dielectric layer is applied by spin coating (e), followed by a photolithography step to define source and drain: the resist is exposed through the substrate with the gate electrode acting as a photo mask for the channel (self-alignment); the overall shape of the source and drain electrodes is confined by an additional photo-mask on the backside of the substrate; the developed photoresist is shown in (f); the source-drain electrodes are structured by metal evaporation and liftoff (g); as a final step the semiconductor is evaporated through a shadow mask (h). (i): micrograph of a 1.2 µm channel; (j) STEM HAADF image of the cross section showing the source to gate overlap and the dielectric thickness.

5.3. Experimental

On a polyethylene terephthalate (PET) substrate (Melinex ST725 by DuPont®) 100 nm copper (Cu) is thermally evaporated through a shadow mask (Figure 5.1a). A hot embossing (HE) imprint resist (mr I 7030E by microresist technology) is spincoated onto the substrate (2000 rpm/30 s). The solvent is baked on a hotplate at 140 °C/3 min. A silicon stamp with the high resolution gate structures as a height profile is aligned with respect to the copper in an EVG® 620 mask aligner. The whole stack is heated to 142 °C and the stamp pressed into the resist with 1.5 kN using an EVG® 520 hot embosser (Figure 5.1b). Both pressure and temperature are held constant for 25 minutes. The stack is cooled to 50 °C before the stamp is separated from the now structured resist. The remaining resist in the structured areas is removed by an O_2 plasma etch (Plasmalab®80 RIE by Oxford Instruments), revealing the underlying copper (Figure 5.1c). This imprinted template is used as a wet etch mask for the copper. The copper is wet etched using 1 g ammonium persulfate (Sigma Aldrich) and 0.15 g potassium hydroxide in 50 ml deionized water. After stripping the etch mask using propylene glycol monomethyl ether acetate (PGMEA, $\geq$ 99.5%), the gate is structured by *NIL* (Figure 5.1d). The dielectric layer consists of 2.5 wt% poly(vinyl cinnamate) (PVCi, Sigma Aldrich, Mn = 45,000-55,000) in chloroform ($CHCl_3$) and is spin coated (2000 rpm/30 s). It is cured for 1 hour under inert conditions using a 254 nm UV lamp (Figure 5.1e). To structure the source/drain electrodes a positive photo resist (AZ® 1505 by MicroChemicals) is spin coated onto the dielectric layer (3000 rpm/30 s). To prevent photoresist side wall metalization a resist soaking technique is used [18]. The sample is dipped into a photo developer (AZ® 726 MIF by MicroChemicals) for five seconds, rinsed in deionized water and dried using N_2. Then the photo resist is prebaked (100 °C/90 s). The resist is UV exposed (70 mJ/cm^2) through the substrate, allowing the gate electrode to act as a photo mask. After the development (10 s in AZ® 726 MIF, rinsing in deionized water and drying in N_2) the shape of the photo resist can be schematically seen in Figure 5.1f. A 60 nm gold layer

is thermally evaporated onto the sample. The lift-off is performed using again PGMEA (Figure 5.1g). The semiconductor pentacene is thermally evaporated through a shadow mask (Figure 5.1h). The deposition rate is increased from 1 Å/s for the first 5 nm to 5 Å/s to reach a layer thickness of 40 nm while the substrate is held at room temperature and rotated at 8 rpm. The semiconductor is applied to all samples in one single run. A micrograph showing the channel area of a fully processed *OTFT* can be found in Figure 5.1i.

In order to determine the overlap of the source and drain electrodes with respect to the gate and the dielectric layer thickness of the devices, one transistor was cut using a focused ion beam (FEI NOVA 200) and the cross section was analyzed by means of transmission electron microscopy (FEI Tecnai F20) (Figure 5.1j). The transistor has a source to gate overlap of only 120 nm and a dielectric thickness $t = 200\,\text{nm}$.

All electrical measurements were performed in darkness under ambient conditions using an mb parameter analyzer by mb technologies. All parameters extracted from the electrical characteristics are an average of forward and reverse sweep. It has to be mentioned though that the hysteresis is negligible.

5.4. Results and Discussion

To study the influence of the channel length on the performance of self-aligned, *NIL* structured organic thin-film transistors, 74 devices with five different channel lengths between $L = 25\,\mu\text{m}$ and $L = 0.8\,\mu\text{m}$ and a constant channel width $W = 150\,\mu\text{m}$ have been fabricated and characterized. Table 5.1 gives extracted transistor parameters for each channel length, typical output and transfer characteristics are compiled in Figure 5.2. According to the positive onset voltage all devices are normally on with mobility values comparable to literature [19, 20]. The maximum on-current $I_{ON,max}$ increases from the largest to the smallest channel length by a factor of 4.2. Nonlinearity in the

Table 5.1.: Mean values of extracted transistor parameters for different channel lengths. Sample size 74 devices.

L	channel length
$I_{ON,max}$	maximum on-current (I_D@ $V_{GS} = V_{DS} = -10\,\mathrm{V}$)
S	subthreshold swing (slope of a linear fit through the I_D values between $V_{GS} = V_{ON}$ and $V_{GS} = V_{ON} - 2.5\,\mathrm{V}$
μ	saturation mobility @ $V_{GS} = V_{DS} = -10\,\mathrm{V}$
V_{ON}	onset voltage @ $V_{DS} = -10\,\mathrm{V}$
I^*_{ON}	effective on-current @ $V_{DS} = -10\,\mathrm{V}$, ($I^*_{ON} = I_D$ @ $V_{GS} = -10\,\mathrm{V} + V_{ON}$)
$N_{SS,max}$	maximum interface trap density @ $V_{DS} = -10\,\mathrm{V}$

L	$I_{ON,max}$	S	μ	V_{ON}	ΔV_{ON}	I^*_{ON}	$N_{SS,max}$
µm	10^{-7} A	V/dec	$10^{-2}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$	V	V	10^{-8} A	$10^{11}\,\mathrm{cm^{-2}\,eV^{-1}}$
25	-0.8	2.2	1.8	5.5	0	-2.5	2.9
10	-1.4	1.93	1.4	5.9	0.4	-3.6	2.5
5	-2.0	1.86	1.0	6.1	0.6	-4.8	2.4
2	-2.2	2.17	0.4	7.5	2.1	-3.2	2.8
0.8	-3.2	2.31	0.2	9.19	3.7	-2.9	3.0

linear operation regime is visible for all devices, indicating the presence of contact resistance and traps [21]. The nonlinearity increases with decreasing L. Both, the off-current I_{OFF} (I_D @ $V_{GS} = +10\,\mathrm{V}$, $V_{DS} = -10\,\mathrm{V}$) and the gate leakage current (I_G @ $V_{GS} = +10\,\mathrm{V}$, $V_{DS} = -10\,\mathrm{V}$) are equal or smaller than the current measuring limit of our setup, being 10^{-11} A. The on-to-off ratio can thus only be indicated as $I_{ON}/I_{OFF} \geq 10^4$. From separately fabricated capacitors a specific capacitance of the PVCI dielectric of $13\,\mathrm{nF\,cm^{-2}}$ is extracted. Taking the dielectric layer thickness $t = 200\,\mathrm{nm}$ into account the relative permittivity is approximately 2.7.

For a better understanding of the short channel effects, the contact resistance R_C is estimated using the transmission line model (TLM) [22]. The model relies on an Ohmic behavior of the transistor current in the linear regime,

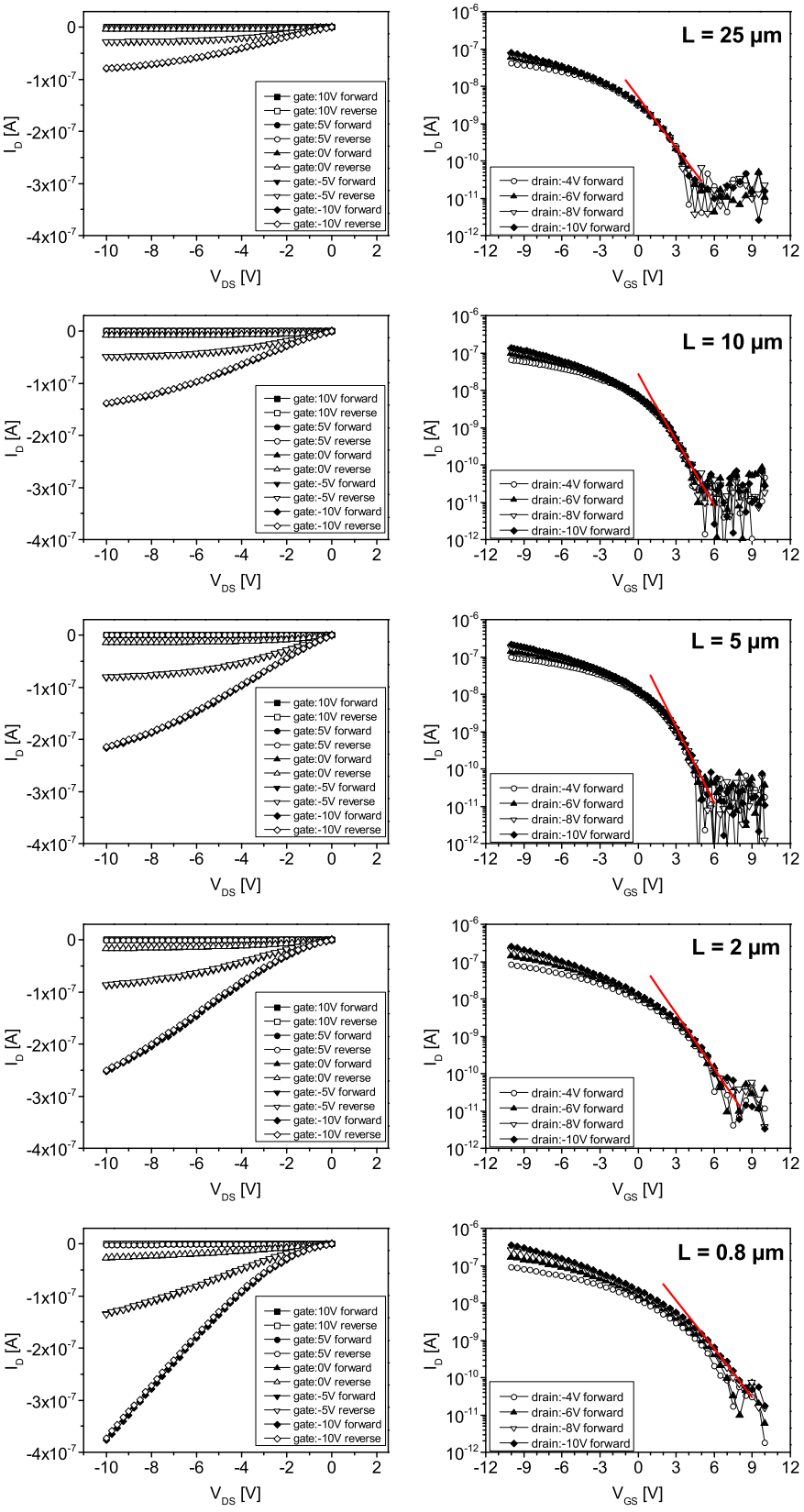

Figure 5.2.: Output and sub-threshold characteristics for all five analyzed channel lengths; The red line in the sub-threshold graphs represents the linear fit for the calculation of the swing for $V_{DS} = -10\,\mathrm{V}$.

which is not the case especially for the devices with $L \leq 2\,\mu m$. Therefore, these devices are excluded in the estimation of the contact resistance. A minimum R_C value of $R_C \sim 0.6\,M\Omega\,cm$ is extracted (Figure 5.3a), which is high, but comparable to what has been reported in literature for gold/pentacene $OTFT$s [23, 24]. The reduction of the gold work function due to resist residuals and contamination [25] from the photolithography process, decreased mobility of pentacene at the interface arising from bad morphology and the relatively low gate and drain voltages [26] could be reasons for the rather high R_C. TLM also allows for the extraction of an intrinsic, channel length independent mobility $\mu^* = 1.4 \times 10^{-2}\,cm^2\,V^{-1}\,s^{-1}$ (Figure 5.3b). This value is comparable to the saturation mobility of the devices with $L = 10\,\mu m$, indicating that devices with $L \geq 10\,\mu m$ can be considered as long channel devices [22].

The influence of the channel length on the onset voltage V_{ON} , the on-current I_{ON} and the swing is investigated for four different drain-source voltage values between $V_{DS} = -4\,V$ and $V_{DS} = -10\,V$ (Figure 5.4). All values displayed in Figure 5.4 are averaged over all devices of the same channel length.

The *onset voltage* shifts towards more positive values with smaller channel lengths (Figure 5.4a). For small absolute V_{DS} values the onset voltage is slightly higher (= lower positive value) than for higher drain voltages. This drain voltage induced difference in onset voltage increases with decreasing channel lengths to a value of 0.5 Vfor the devices with $L = 0.8\,\mu m$. When plotting the *shift of the onset voltage* ΔV_{ON} ($\Delta V_{ON} = V_{ON} - V_{ON}{}_{L=25\,\mu m}$) over the channel length a $1/L$ influence is visible (Figure 5.4b). All these observations upon decrease of the channel length - the shift of V_{ON} towards more positive values (= decrease), the 1/L dependence of ΔV_{ON}, and the drain voltage dependence of the threshold voltage - are typical behaviors of devices with short channels. They originate from the invalidity of the gradual channel approximation due to a growing influence of the lateral electric field. Specifically, the decrease of V_{ON} with increasing drain field in short channel devices (also known as threshold voltage roll-off) is generally referred to as drain induced barrier lowering ($DIBL$)

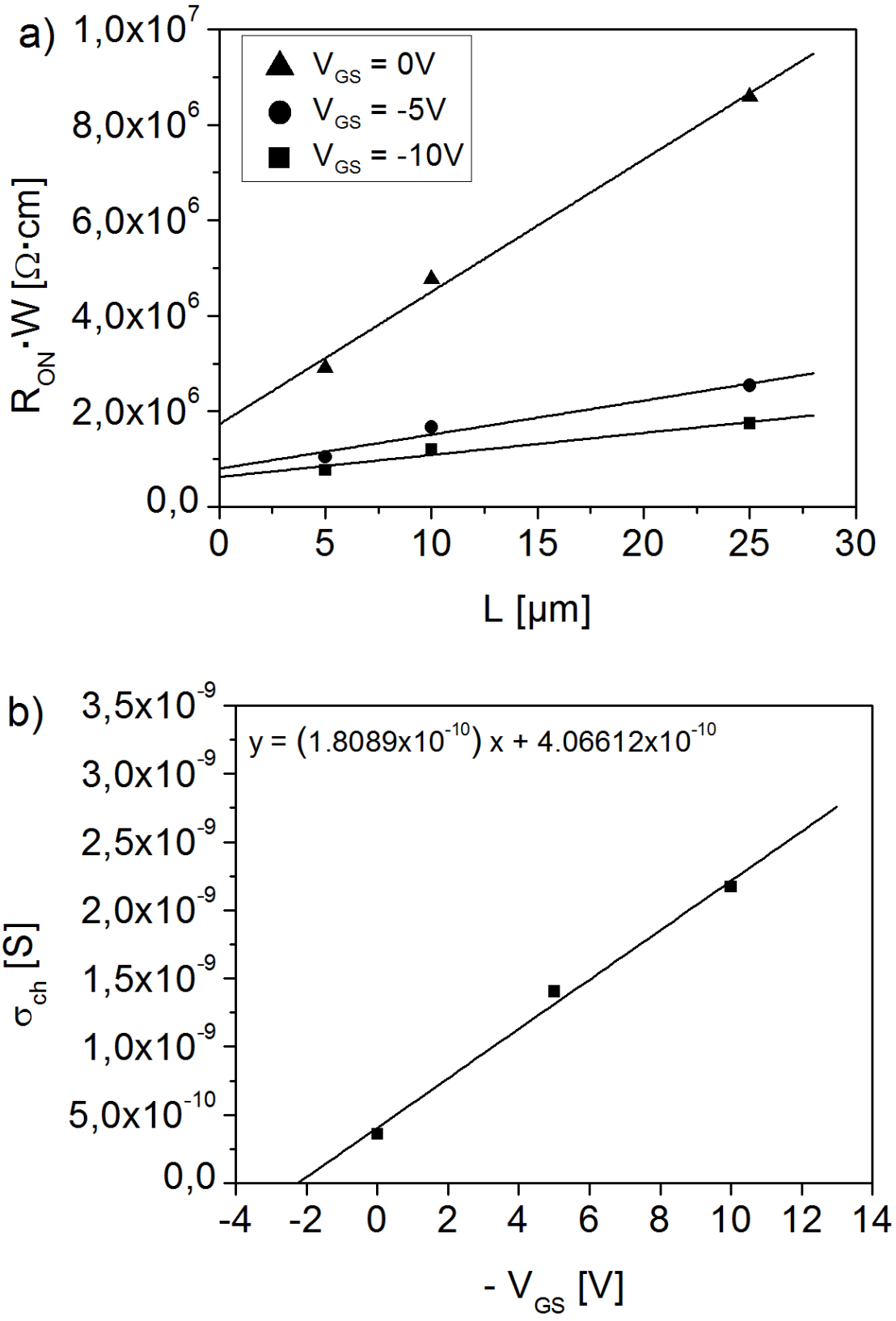

Figure 5.3.: (a) Width normalized R_{ON} as a function of the channel length L; the intercept of the linear fits with the x-axis represent the contact resistance for each gate voltage; (b) channel sheet conductance σ_{ch} as a function of the negative gate voltage V_{GS}; the slope of the linear fit is used to calculate the intrinsic mobility μ^*.

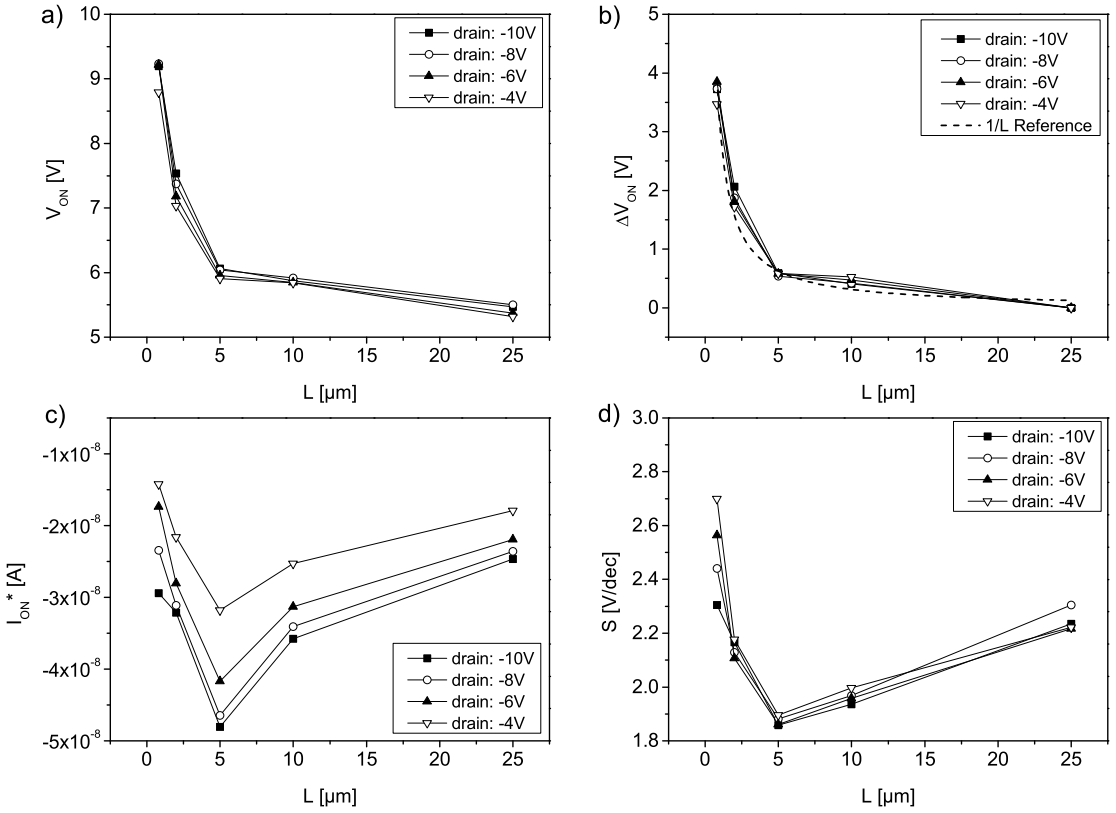

Figure 5.4.: Influence of the channel length on the (a) onset voltage, (b) onset voltage shift, (c) onset voltage normalized on-current and (d) onset swing; the 1/L curve in (b) is a guide for the eye.

and a well-known short channel effect in shrinked *MOSFET*s [27, 28]. As a consequence of the strong increase of the lateral with respect to the vertical electric field upon aggressive L scaling, the depletion regions associated with the source and drain junctions can now occupy a large fraction of the channel and act to deplete it of charge carriers. This reduces the required gate voltage to reach accumulation and hence lowers the device onset voltage [29]. For such devices the deviation of the onset voltage from the long channel value (ΔV_{ON}) is inversely proportional to the channel length [28, 30]. Furthermore, as the size of the depletion regions near source and drain is drain voltage dependent, threshold-voltage roll-off will also be a function of the drain voltage.

For *OTFT*s the *DIBL* effect has first been described in 2004 by Scheinert and Paasch [31] in a modified drift-diffusion model combined with non-degenerate

carrier statistics. A calculation of the surface potential in normally-on *OTFT*s at bias conditions near the threshold (off-state of the device) revealed, that the potential barrier in the channel is strongly decreased with increasing lateral field. Especially the potential maximum near the source contact is reduced, thus causing an increased accumulation of holes there. Consequently, a higher gate voltage is necessary to switch off the transistor. The crossover to the *DIBL* regime appearing as threshold voltage roll-off has been observed in literature at different L/t-values for devices with comparably long channels ($L/t < 80$ [11]), medium channels ($L/t < 50$ [10]) and short channels ($L/t < 10$ [9]), underlining that the definition of short versus long channel regime in *OTFT*s has to be determined individually for each device geometry and material system. In addition, it is expected that the influence of the drain voltage on $V_{ON}(L)$ and on ΔV_{ON} is significant only for lateral electric fields $\geq 10\,\mathrm{V\,\mu m^{-1}}$, in our case ($V_{DS} = -10\,\mathrm{V}$) corresponding to devices with $L \leq 1\,\mu\mathrm{m}$.

To determine the influence of L on the *on-current* independently of the onset voltage, an effective on-current I^*_{ON} is extracted from the transfer characteristics (Figure 5.4c). As expected, in the long channel regime I^*_{ON} increases with decreasing channel length, having its peak absolute value at $L = 5\,\mu\mathrm{m}$, but for smaller channel lengths the current drops again. This behavior is observed independent of the drain voltage (and the lateral field) and clearly shows that short channel effects, especially the parasitic contact resistance and the channel length modulation [10], dominate the current for $L \leq 5\,\mu\mathrm{m}$.

As a third parameter the *subthreshold swing* S is plotted against the channel length (Figure 5.4d). Generally, the swing is defined as the maximum slope of a tangent through the points closest to V_{ON}. The method used in this work leads to higher swing values, but increases comparability of different devices as it drastically reduces the influence of measurement spikes. This is important, as the currents close to the threshold region are in the order of $10^{-10}\,\mathrm{A}$ and thus very close to the measurement limits of the used parameter analyzer of $10^{-11}\,\mathrm{A}$. In the long channel regime of our devices ($L \geq 5\,\mu\mathrm{m}$), S decreases with

decreasing L, whereas in the short channel regime a strong rise of S is observed, corresponding well to the changes visible in I^*_{ON}. This behavior again is related to the $DIBL$ effect. As a consequence of the larger influence of the lateral electric field at the expense of the vertical electric field the potential barrier near the source contact will decrease due to the increase of the maximum negative surface potential, thus fostering the accumulation of holes [31]. Since below the threshold the channel conductance is exponentially dependent upon the magnitude of the surface potential, at short channel lengths the sub-threshold hole current has to increase strongly with increasing negative surface potential. Furthermore, the decreasing influence of the gate field appears as an increase of the swing. Based on the swing values the interface trap density $N_{SS,max}$ was calculated [32, 33], reaching a peak value of $N_{SS,max} = 3.0 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ for the devices with $L = 0.8\,\mu\mathrm{m}$ (compare Table 5.1). Again, the increase of $N_{SS,max}$ in the short channel regime is related to the increased accumulation region of holes (especially in the source region) thus giving rise to an increase of the hole trap density there.

The data reveal that for the given material system $L = 5\,\mu\mathrm{m}$ is the best compromise between short channel effects and minimum channel length. There are a number of possibilities for shifting this optimum towards smaller L values. As discussed above the dielectric thickness should be significantly lower than 1/10th of the channel length. For the present devices a 1/10 ratio is reached for the 2 µm devices, for the $L = 800\,\mathrm{nm}$ devices only a ratio of 1/4 is present. However, a further reduction of the dielectric thickness of PVCi resulted in short circuiting of the gate electrode. Thus a significant improvement of the performance for small channel lengths might only be possible when using a material with a lower intrinsic breakdown. Future work will deal with the implementation of such materials as e.g. PNDPE [33]. Furthermore, it is well known that the gap between the Fermi level of gold and the $HOMO$ level of pentacene is rather large, resulting in considerable contact resistance (compare the non-linearity in the linear regime of the transistors in Figure 5.2). The in-

fluence of the contact resistance increases with decreasing channel lengths [5], resulting in a reduced I^*_{ON} for small L values. By introducing a contact treatment e.g. by UV/ozone [34] or by application of a self-assembled monolayer [35] the contact resistance can be reduced significantly.

While this work focuses on the ideal channel length with respect to I^*_{ON}, is should be noted that also the cutoff frequency cutoff frequency (f_T) of a field-effect transistor is influenced by the channel length [4]. A frequently-used estimation for f_T is given by

$$f_T \leq \frac{V_{DS} \cdot \mu}{2\pi L \left(L + 2L_{OV}\right)} \tag{5.1}$$

with L_{OV} being the source/drain overlap length with respect to the gate. According to this equation the switching speed increases with decreasing L. The minimized overlap lengths of the self-alignment process used in this work further improves f_T. Previously, we could show cutoff frequencies of 400 kHz for a self-aligned $OTFT$ with $L = 4.8\,\mu m$ [17]. While one would aim for as low L values as possible by following Equation 5.1, quite recently it was found that the contact resistance reduces or even nullifies the benefits of small channel length $OTFT$s [15], thus again emphasizing the importance of a reduction of the contact resistance in downscaled devices.

5.5. Conclusion

To conclude, self-aligned nanoimprint lithography structured organic field effect transistors with channel lengths between 25 µm and 800 nm have been fabricated and analyzed with respect to their short channel behavior. The data reveal that the short channel effects have a significant influence on the on-current and the swing for transistors with channel lengths smaller than 5 µm. It was shown that copper can be used as gate material in a self-aligned process. Furthermore, etching instead of a previously used liftoff process is used to define the gate electrode by NIL. Since copper can be formulated in an ink the

results mark a first step towards our goal of fabricating self-aligned *NIL OTFT*s consisting only of printable materials. Such devices could exhibit improved performance and enhanced compatibility when being used in printed electronics applications.

5.6. Acknowledgements

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6. Influence of the source-gate and drain-gate overlap length on the on-current of self-aligned, NIL structured OTFTs

Preamble

This chapter has been submitted by T. Rothländer, J. Kraxner, R. Schmied, H. Plank, W. Grogger, C. Palfinger, A. Haase, H. Gold, and B. Stadlober for publication in Applied Physics Letters. The version shown here is the manuscript as submitted by the authors. For improved consistency with this thesis the original manuscript has been graphically recomposed.

The overlap variation process has been developed by T. Rothländer. Experimental design, transistor fabrication, measurement and data analysis has been performed by T. Rothländer. The cross section analysis was done by J. Kraxner and R. Schmied, supervised by H. Plank and W. Grogger. H. Gold designed and fabricated the stamps for *NIL* structuring, A. Haase and B. Stadlober gave valuable input on the transistor data analysis. The idea of studying the influence of the overlap on the performance of *OTFT*s by varying the exposure angle was proposed by A. Haase. T. Rothländer prepared all figures and wrote the manuscript except for the parts about the cross section preparation and results,

which were written by J. Kraxner. The manuscript was then improved by all co-authors. T. Rothländer acted as the single corresponding author of the work and supervised the research project. Reuse of the manuscript in accordance with the APL Copyright and Consent Form (Appendix B).

6.1. Abstract

We report on the influence of the gate-source and the gate-drain overlap on the on-current of organic thin-film transistors structured by nanoimprint lithography. By modifying an existing self-alignment process we are able to control both source to gate and drain to gate overlaps and even fabricate devices with a gap between the source/drain and gate electrode. Devices with overlap lengths between +1.5 µm and −0.2 µm are analyzed. When a gap is present between the source and gate electrode, the on-current drops significantly and an overlap > 180 nm is necessary for an overlap-independent on-current. No influence of the drain to gate overlap on the on-current has been found.

6.2. Introduction

Organic thin-film transistors (*OTFT*s) have experienced a steep rise in performance over the last decade. Besides the development of better performing materials the investigation of critical device geometry parameters like channel length [1–7], dielectric [8–12] and semiconductor layer thickness [13], and size of the electrodes [14–16] have helped to improve transistor characteristics with respect to e.g. switching speed or on-current level. Among other factors these improvements allow for the fabrication of integrated circuits [17, 18], RFID tags [19, 20], and display backplanes driven by *OTFT*s [21, 22]. What has not been studied in-depth so far, especially not in coplanar *OTFT* architecture, is the influence of the interlayer electrode overlap L_{OV} (the geometric overlap between source/drain and gate electrode) on the device characteristics. Most interesting are the effects of the length of the overlap region, of a vanishing overlap or of an asymmetrical overlap on the transistor curves [16]. For staggered *OTFT*s it has been shown that a too small L_{OV} increases the contact resistance and that the optimum overlap length depends on the semiconductor layer thickness [14, 15]. Our previous work on coplanar *OTFT*s demonstrated a reduction of L_{OV} to

values as low as 30 nm by a self-alignment back-substrate exposure patterning technique [23, 24]. Thereby, the parasitic capacitance of n-type *OTFT*s was significantly reduced resulting in remarkably high transition frequencies of around 400 kHz being close to the calculated maximum value of 700 kHz (considering the semiconductor mobility, bias voltage and measured channel geometry). In the mentioned self-alignment technique the thicknesses of the substrate and of the dielectric determine the magnitude of L_{OV} [23]; the thinner the layers, the smaller the overlap. Accordingly, by optimizing the layer setup we have a tool for further reduction of the overlap, thus supporting the continuous hunt for high speed transistors.

These considerations raise the question of the smallest possible overlap length maintaining proper DC transistor behavior and sufficient on-current level. In the late 1980s scaling of the interlayer electrode overlap length as a possibility to improve switching speed without overall device downscaling was investigated for submicron silicon based IGFETs. It has been shown that too small an overlap length leads to stability problems due to hot carrier effects stemming from an increased drain depletion field [25–27]. Despite the unwanted effects, negative overlap devices are used to study hot carrier effects and drain depletion motion [28]. More recently performance improvements due to negative overlaps have been shown for unified random access memories [29] (increased soft program immunity) and tunnel field effect transistors [30, 31] (reduced ambipolarity and thus higher on-to off-current ratio). For amorphous silicon thin-film transistors it has been shown that the gate leakage current decreases with decreasing overlap lengths [32]. Though these results cannot be directly transferred to *OTFT*s, it is still an indication of what effects can be expected.

In this work we have modified the reported self-alignment nanoimprint lithography (SANIL) process [23] such that the gate-to-source and gate-to-drain overlap lengths of coplanar *OTFT*s can be varied systematically. Thereby we could analyze the influence of a varying and asymmetric L_{OV} on the transistor characteristics and investigate the influence of L_{OV} on the carrier injecting and

extracting electrodes.

6.3. Experimental

On a polyethylene terephthalate (PET) substrate a 100 nm copper layer is thermally evaporated through a shadow mask (Figure 6.1a). A hot embossing (HE) imprint resist (mr-I 7030E by microresist technology) is spin-coated onto the substrate (2000 rpm/30 s) and baked on a hotplate (140 °C/3 min). A silicon stamp containing the high resolution gate structures as a topographic height profile is aligned with respect to the pre-structured gate (EVG® 620 mask aligner) and imprinted using an EVG® 520 hot embosser (142 °C, 1.5 kN, 25 min) (Figure 6.1b). The remaining residual in the structured areas is removed by an oxygen plasma etch (Oxford Instruments Plasmalab®80), uncovering the copper in the structured areas (Figure 6.1c). This imprinted polymer template is used as an etch mask for the underlying copper. The copper is removed during two minutes using an aqueous solution of 1 g ammonium persulfate (Sigma Aldrich) and 0.15 g potassium hydroxide in 50 ml deionized water. After stripping the etch mask (1 min in propylene glycol monomethyl ether acetate (PGMEA)), the Cu gate electrode defined by NIL remains on the substrate (Figure 6.1d). The dielectric layer (3.5 wt% poly(vinyl cinnamate) in CHCl3) is spin coated (2000 rpm/30 s) and UV cured (2 h/254 nm) under inert conditions (Figure 6.1e) (relative permittivity ~ 2.7). In order to structure the source and drain electrodes an elsewhere published self alignment process is employed [23]. A positive photo resist (AZ® 1505 by MicroChemicals) is spin coated onto the dielectric layer (3000 rpm/30 s). To avoid the well-known formation of photoresist side wall metallization in metal liftoff processes a resist soaking technique is used [33]. The sample is dipped into a photo developer (5 s in AZ® 726 MIF by MicroChemicals), cleaned and dried (DI-H_2O and N_2) before the photo resist is prebaked (100 °C/90 s). The resist is UV exposed through the substrate, and thus the gate electrode acts as a photo mask. For different exposure angles the

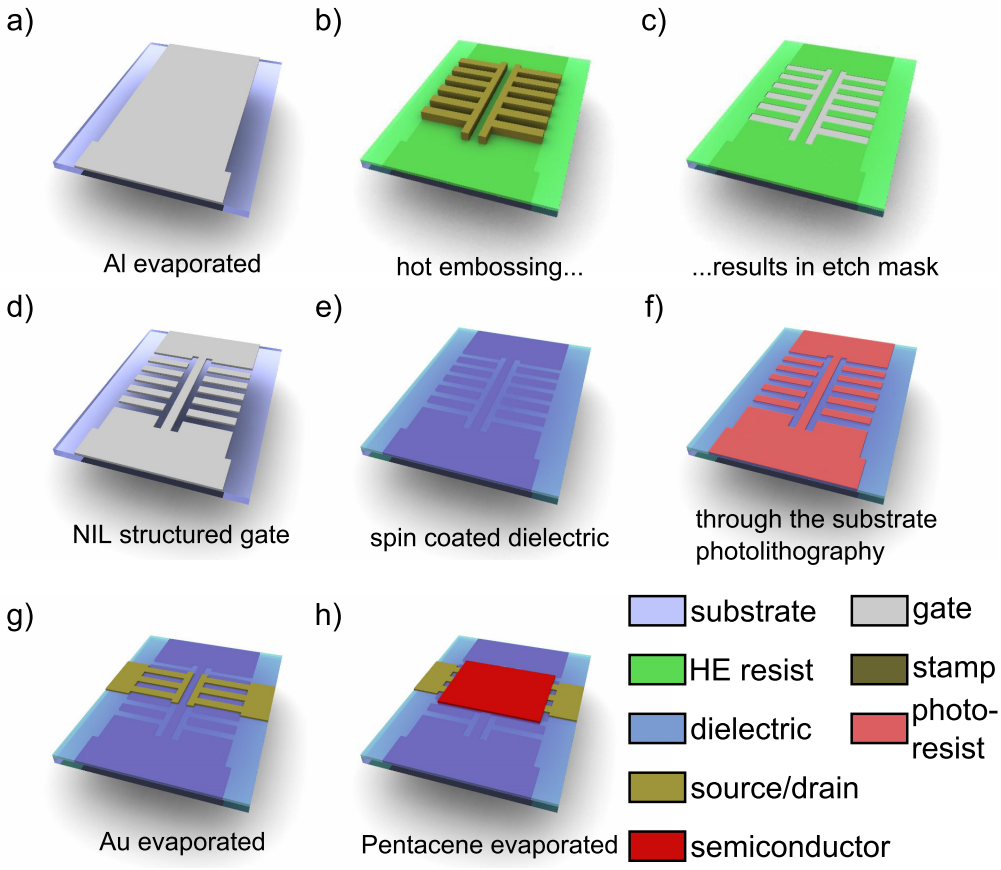

Figure 6.1.: Process scheme of a self-aligned, nanoimprint lithography structured OTFT: gate evaporated through shadow mask (a); hot embossing resist structured by pressing a stamp into the heated soft material (b); cooling, stamp removal, and residual etch resulting in an etch mask (c); gate structuring finalized after wet etch and strip of the hot embossing resist, (d); spin-coating of the dielectric layer (e); spin-coated photoresist, exposed through the substrate with the gate being the photo mask, after development (f); evaporation of source/drain metal through a shadow mask and lift-off of the photoresist (g); thermal evaporation of the semiconductor through a shadow mask (h).

samples are placed on 3D printed wedges (Makerbot 2 Replicator) with different inclinations α ranging from 55° to 85° in steps of 10°. The tilted samples have a smaller exposure area compared to flat lying ones, which is compensated by increasing the exposure dose from 70 mJ cm^{-2} to 650 mJ cm^{-2}. The shape of the photo resist after development (30 s in AZ® 726 MIF, cleaned and dried (DI-H_2O and N_2)) is schematically depicted in Figure 6.1f. A 60 nm gold layer is thermally evaporated through a shadow mask, which defines the overall shape of the source/drain electrodes. A lift-off is performed (PGMEA) (Figure 6.1g) and 40 nm pentacene is thermally evaporated through a shadow mask, while the substrate is held at room temperature and rotated at 8 rpm (Figure 6.1h). For improved comparability the semiconductor is applied to all devices in one single evaporation step.

Channel and overlap length are determined for one transistor per exposure angle on a FEI NOVA 200 dual beam system in the eucentric height of 19.3 mm. To prevent charging and avoid beam damage a protective Pt/Pd layer ($\sim$ 80 nm, Leica EM ACE600) and a Pt/C ($\sim$ 1 µm) ion beam induced layer are deposited. Acceleration voltage is kept constant at 30 kV and beam currents of 500 pA for trench milling while 100 pA and 50 pA for final polishing are used with constant pixel dwell times of 500 µs. FIB processing is performed using a recently introduced interlacing patterning strategy reducing chemical damage and increasing morphological stabilities [34–36] which is ideal for FIB based soft matter processing. Cross section analysis is performed in-situ via the electron beam using a through-the-lens-detector in secondary electron mode. Polishing and measurements have been repeated and the extracted values have been averaged.

All electrical measurements are performed in darkness under ambient conditions using an mb parameter analyzer by mb technologies.

6.4. Results and Discussion

To modify the gate-to-source and gate-to-drain overlap lengths the exposure angle α during the photolithographic patterning of the source and drain electrodes is varied. Ideally, at perpendicular incident angle of the UV-exposure beam no overlap should result (Figure 6.2a). In reality light gets scattered in the substrate and hits the photoresist under skewed angles (Figure 6.2b). Furthermore, the shape of the gate electrodes is not rectangular but rather trapezoid because of the isotropic wet etch of the Cu gate. Thus UV light can also pass through the thinner parts at the gate edges. Both these effects result in an overlap of source/drain electrodes with respect to the gate (Figure 6.2b). By deliberately tilting the sample (Figure 6.2c) and thus changing the incident angle, asymmetrical overlaps and even gaps between one electrode and the gate (called negative overlap throughout this work) are achieved (Figure 6.2d,e). A total of 22 samples with five different inclination angles of $\alpha = 0°$ (no wedge used), 55°, 65°, 75°, and 85° have been fabricated. By tilting the overlap length increases on side A ($L_{OV,A}$) and decreases on side B ($L_{OV,B}$) (Figure 6.2e).

For one representative device of each inclination cross sections are prepared by FIB milling. Figure 6.2f-i shows representative SEM images for the two extreme inclination angles ($\alpha = 0°, 85°$) whereas in Table 6.1 the extracted geometrical parameters of the *OTFT*s are summarized.

The variation in gate length between 4 and 5 µm is attributed to variations in etch rate of the Cu gate. The even larger variation in channel length between 2.8 and 4.7 µm is attributed to non-ideal compensation of the exposure dose for inclined incidence angles α. With the modulation of α, *OTFT*s with a constantly positive overlap on side A, ($L_{OV,A}$) ranging from 120 nm to 1530 nm and an overlap that changes from positive to negative values on side B, ($L_{OV,B}$) ranging from +270 nm to −220 nm are fabricated. Unequal overlaps at $\alpha = 0°$ are attributed to deviations from normal incidence angle as no wedge compensation of the mask aligner was possible within this experiment.

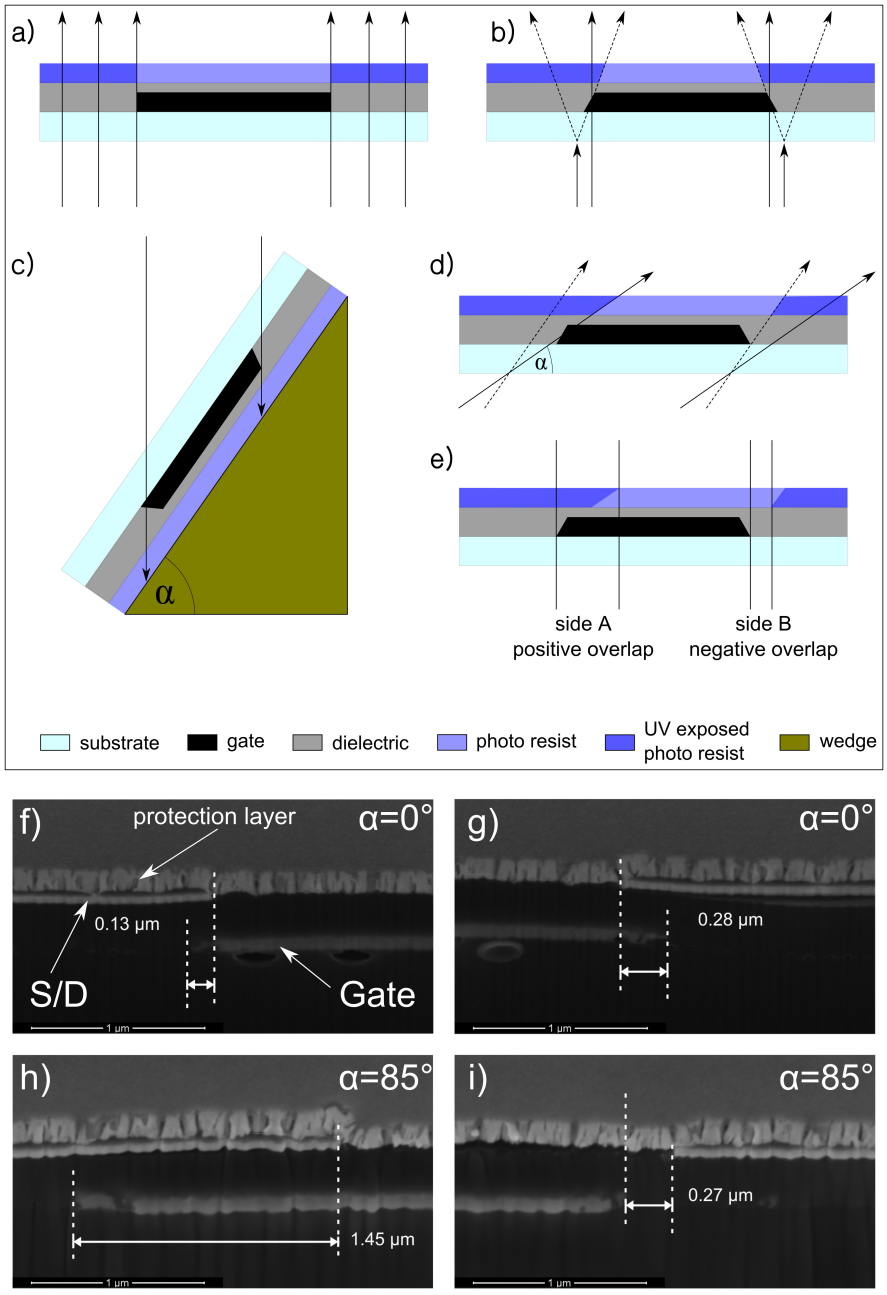

Figure 6.2.: Schematics of the self-alignment process (arrows indicate UV light): (a) idealized condition without scattering; (b) formation of an overlap due to light scattering (dashed arrows) and transparency at the gate edges; (c) variation of incident angle α using a wedge; (d) photoresist exposure with inclined incident light angle; (e) definition of side A and side B and of negative and positive overlap; SEM images of a cross section of a transistor where the inclination during the self-alignment was (f,g) 0° and (h,i) 85°; (f,h) show the measurement of side A overlap, (g,i) of side B overlap.

Table 6.1.: Results of the cross section analysis.

α	exposure angle during self-alignment
L_G	length of the gate electrode
L	channel length
$L_{OV,A}$	side A overlap length
$L_{OV,B}$	side B overlap length

α [°]	L_G [µm]	L [µm]	$L_{OV,A}$ [µm]	$L_{OV,B}$ [µm]
0	5.11 ± 0.06	4.74 ± 0.02	0.12 ± 0.07	0.27 ± 0.04
55	4.05 ± 0.05	2.87 ± 0.03	1.03 ± 0.01	0.18 ± 0.04
65	4.64 ± 0.06	3.76 ± 0.01	0.97 ± 0.09	-0.10 ± 0.13
75	5.10 ± 0.04	3.67 ± 0.07	1.70 ± 0.20	-0.17 ± 0.03
85	4.34 ± 0.25	3.05 ± 0.09	1.53 ± 0.07	-0.22 ± 0.11

The devices are electrically characterized twice. In the first measurement the side A electrode is used as source and the side B electrode as drain electrode (called source A in this work) and in the second measurement the assignment of source and drain was exchanged (called source B). Sub-threshold characteristics comparing the two measurement configurations for each inclination are compiled in Figure 6.3. All devices are normally-on with mobilities of about $1 \times 10^{-3}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. The specific capacitance C' of the dielectric layer was measured using separately fabricated capacitors, revealing $C' = 7\,\mathrm{nF\,cm^{-2}}$. Considering the average dielectric thickness of 335 nm, the relative permittivity is about 2.7.

While all measurements with source A show on-currents in saturation of about $I_{ON,A} = 1 \times 10^{-8}\,\mathrm{A}$ (I_{ON} = maximum drain-source current @ $V_{DS} = -14\,\mathrm{V}$) for positive as well as for negative $L_{OV,B}$, the situation is different for source B measurements. Transistor behavior is still visible for all overlaps, but $I_{ON,B}$ is higher than $I_{ON,A}$ for $\alpha = 0°$, equal for $\alpha = 55°$ and drops by about one order of magnitude for all other inclinations.

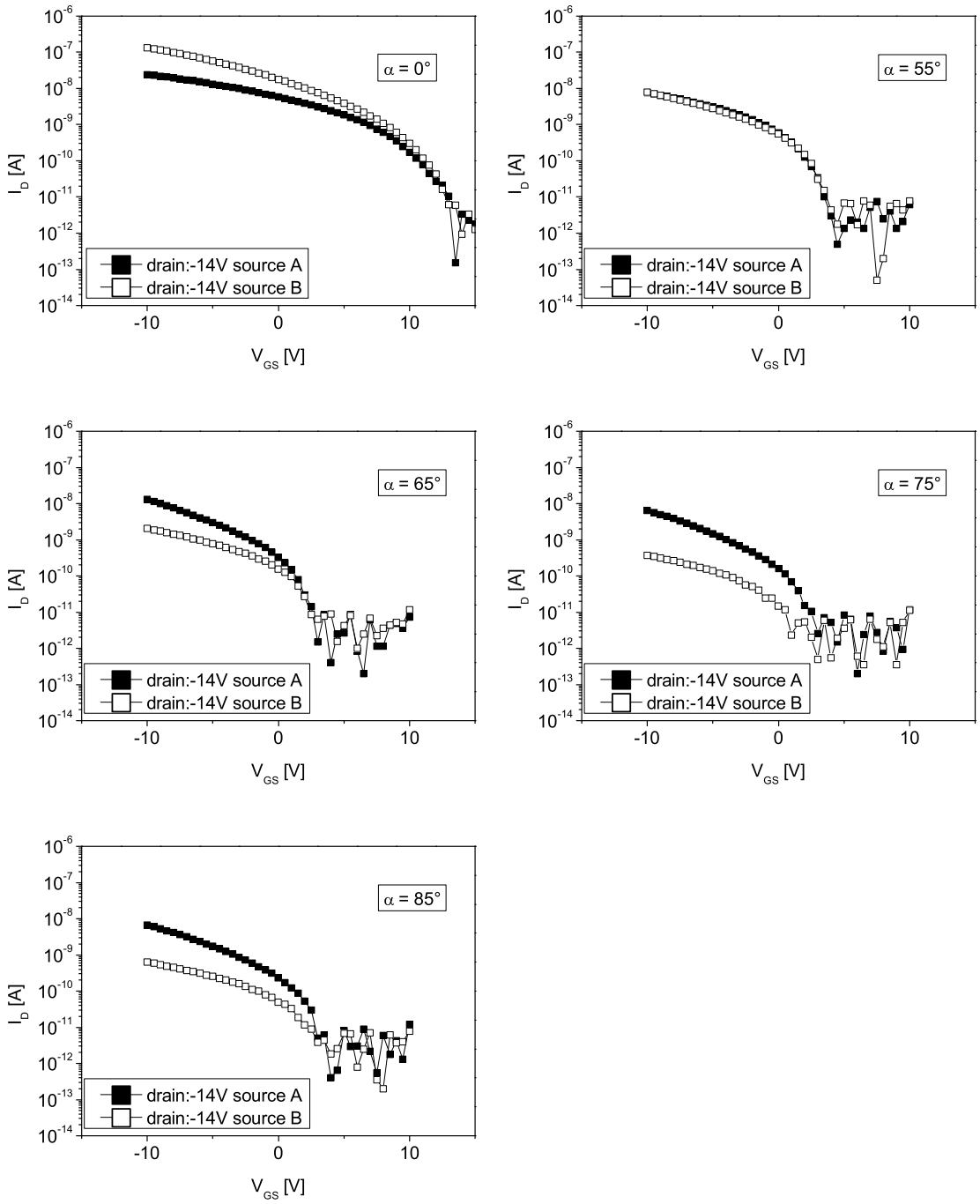

Figure 6.3.: Subthreshold characteristics for all five inclinations α, comparing source being the side A and side B electrode.

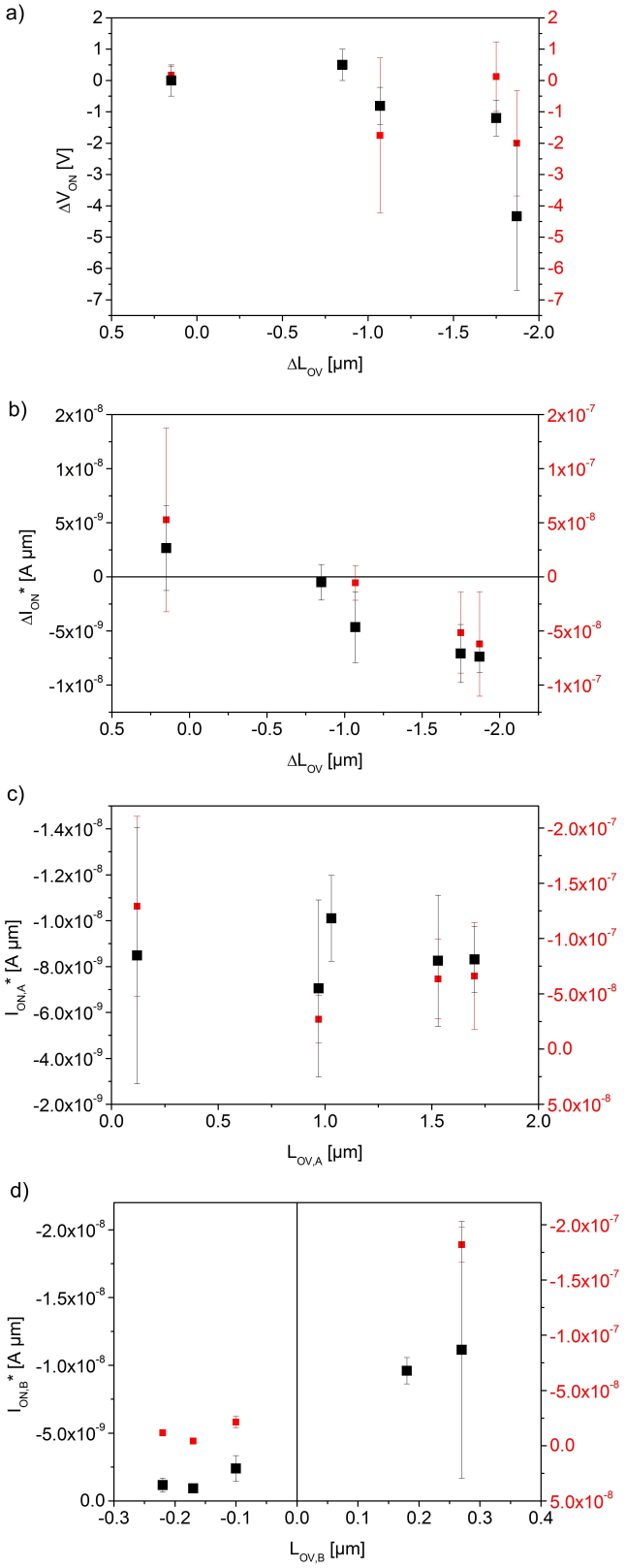

Figure 6.4.: Difference in onset voltage over difference in overlap length (a); Difference in normalized on-current between source A and source B over the difference in overlap length (b); Normalized on-current over source overlap for source A (c) and B (d) configuration.

Concerning the difference in onset voltage $\Delta V_{ON} = V_{ON,B} - V_{ON,A}$ between source A and source B, the data indicates a tentative shift towards more negative V_{ON} values for negative source overlaps, especially for devices with $\Delta L_{OV} = L_{OV,B} - L_{OV,A} = 1.75\,\mu m$ (Figure 6.4a). Since the data spread there is rather high, the whole experiment has been carefully repeated, electrically characterizing a total of 13 OTFTs with four of the five inclination angles. A freshly purified batch of pentacene was used in the second experiment, resulting in a one order of magnitude higher mobility (red data in Figure 6.4). The data of the second experiment strongly indicates that ΔV_{ON} is independent of ΔL_{OV}, whereas all trends concerning the influence of the overlap length on the on-current were clearly reproduced in the second experiment (Figure 6.4b-d).

To allow for an averaging of I_{ON} over all identical devices and a comparison between all inclinations, I_{ON} is normalized with respect to V_{ON} and the channel length L: $I^*_{ON} = I_D \cdot L$ with I_D @ $V_{GS} = -10\,V + V_{ON}$. In Figure 6.4b the normalized current difference $\Delta I^*_{ON} = I^*_{ON,B} - I^*_{ON,A}$ against the difference of the overlap lengths ΔL_{OV} is plotted. Even though the overlaps for $\alpha = 0°$ and $\alpha = 55°$ are positive on both sides (see Table 6.1), the ΔI^*_{ON} values are very different. Increasing the minimum positive overlap by only 60 nm decreases ΔI^*_{ON} by almost one order of magnitude, even though ΔL_{OV} has increased by 0.7 µm. This indicates that the increase of I^*_{ON} saturates at a overlap $L_{OV,SAT}$. The available data cannot exactly determine $L_{OV,SAT}$, nevertheless, it is possible to state that for the present device configuration an overlap of $L_{OV} = 180\,nm$ is sufficient to reduce ΔI^*_{ON} to about 7% of I^*_{ON}.

When plotting $I^*_{ON,A}$ over $L_{OV,A}$ (= the source electrode has a positive overlap for all inclinations α) no significant change in $I^*_{ON,A}$ is measured (Figure 6.4c). This is completely different when exchanging the source and drain electrode and plotting $I^*_{ON,B}$ over $L_{OV,B}$ (Figure 6.4d). At positive L_{OV} values $I^*_{ON,B}$ still has comparable values to$I^*_{ON,A}$. As soon as the source overlap becomes negative, the current drops by almost one order of magnitude. When the negative overlap increases from $L_{OV,B} = -100\,nm$ to $L_{OV,B} = -170\,nm$, $I^*_{ON,B}$ further drops by a

factor of about 2.5.

The results clearly indicate that the hole injecting electrode (the source) is decisive for the charge carrier transport and defines the current level. A positive overlap length between source and gate means a hole accumulation channel with homogenous charge density from source to drain in the linear regime (according to the gradual channel approximation). In the saturation regime the charge density around source will increase approximately with the square of the gate bias whereas a small depletion zone (the pinch-off) forms around drain (the hole extracting electrode). However, as soon as the overlap length is negative a smaller electric field at the source side of the channel can be expected, therefore the charge density around source will be decreased as compared to the positive overlap situation. This will strongly influence the charge carrier injection due to a decrease in the effective surface potential in the vicinity of the source leading to a decline of the injected charge carrier density. Accordingly, smaller current levels are observed for devices with negative overlap length at the source. In case of a negative overlap near drain almost no influence on I_{ON} is expected since the region around drain is already depleted in the saturation regime. Furthermore, no potential barrier has to be surmounted by the holes due to the lateral electric field. The fact that the current level increases somewhat with the magnitude of the source-sided positive overlap indicates a non-negligible contribution of field variations to the injection process that are induced by the sharpness of the electrode edges or by defects at the edges.

6.5. Conclusion

In the present work the influence of positive and negative gate-source and gate drain-overlap lengths on the on-current has been investigated. The results reveal that negative overlaps on the source electrode result in significant drop in on-current and that a minimum overlap length of about 180 nm is necessary

to eliminate an influence of the overlap on the on-current. The on-current is surprisingly robust to variations of the overlap length at the drain electrode, as no significant difference in the on-current is measured when varying the overlap from +1.5 µm to −0.2 µm. Future work will deal with detailed device simulations and the development of a model for the measured effects.

6.6. Acknowledgements

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7. OTFTs with NIL structured, printed gate electrodes

Preamble

The *OTFT* structuring process for silver (Ag) and printed silver has been developed by T. Rothländer and C. Palfinger. Design of experiment, transistor fabrication, measurement and data analysis has been performed by T. Rothländer. H. Gold designed and fabricated the stamps for the *NIL* structuring. The idea of combining printed materials and *NIL* in *OTFT*s was proposed by B. Stadlober. T. Rothländer supervised the research project.

7.1. Abstract

This chapter addresses the fabrication of self-aligned *OTFT*s with printed silver gate electrode as a step towards fully printed *OTFT*s. Time and funding did not allow for a full device analysis (requiring high sample counts), but proof of principle transistors have been successfully measured and compared with reference devices with both evaporated Cu and Cr/Ag gate.

7.2. Introduction

Fully printed *OTFT*s have been shown for common printing techniques like e.g. screen printing [1], pad printing [2], gravure printing [3] or inkjet printing [4–7]. The channel lengths are usually within the resolution limit of the used techniques, being 10 µm to 200 µm [3]. To achieve higher resolution structuring, methods improving the resolution limit as well as the alignment accuracy have been proposed. Tseng and Subramanian [8] developed a self-alignment in bottom gate, coplanar *OTFT*s by ink roll-off from the gate on a hydrophobic dielectric layer, achieving overlap lengths smaller than 500 nm. A method to decrease the gap between two adjacent printed electrodes and thus the channel length was proposed by Sele et al. [9], realizing resolutions below 100 nm by inkjet printing and subsequent hydrophobization of one of the source-drain electrodes. The second electrode is inkjet printed onto the first one and a roll-off technique ensures the high resolution alignment of the second electrode. Both these methods rely on high control of the surface tension and drying conditions of the inks, limiting the number of usable materials for the processes. A different approach was reported by Li and Guo [10], using micro-contact printing to structure *PEDOT : PSS* electrodes. Resolutions down to 2 µm have been shown, but the authors claim that even smaller feature sizes are possible.

The manufacturing process proposed in this work, while not yet fully printed,

combines high alignment accuracies (by using a self-alignment technique) with high resolution structuring (using nanoimprint lithography). It is furthermore reel to reel compatible and can in theory be combined with parallel structuring techniques like e.g. gravure printing allowing for a high throughput, low cost device fabrication.

7.3. Experimental

Again the self-aligned nanoimprint lithography process developed in chapter 5 is employed (see Figure 5.1). The process has been slightly adapted by using a different wet etch solution for the silver (Ag) gate electrode structuring.

For the reference devices with evaporated gate electrodes a polyethylene terephthalate (PET) substrate (Melinex ST725 by DuPont®) is coated with either 100 nm copper (Cu) or 2.5 nm of chrome (Cr) followed by 100 nm of silver (Ag), thermally evaporated through a shadow mask (Figure 5.1a). When fabricating devices with printed Ag gate, the same substrate is pre-treated with oxygen plasma (15 s). Cabot® CCI-300 silver ink (sonicated for 15 minutes and filtered with a 0.2 µm PET filter before use) is inkjet printed onto the substrate immediately after the plasma step, using a Fujifilm® Dimatix Material Printer DMP 2800 with Dimatix DMC 11610 printing cartridges. After printing, the ink is sintered on a hot plate for 30 minutes at 100 °C under ambient conditions, resulting in a about 100 nm thin conducting film. Details on the hot embossing process for the fabrication of the gate etch mask can be found in chapter 7.3. The copper is removed during two minutes in an aqueous solution of 1 g ammonium persulfate (Sigma Aldrich) and 0.15 g potassium hydroxide in 50 ml deionized water. Alternatively the Cr/Ag and printed Ag are removed using 5 ml of nitric acid (70% HNO_3) in 30 ml deionized water. After stripping the etch mask by submersing the sample in propylene glycol monomethyl ether acetate (PGMEA, $\geq$ 99.5%) in an ultrasonic bath for one minute, the gate electrode is successfully

structured by *NIL*. The dielectric layer consists of 3.5 wt% poly(vinyl cinnamate) (PVCi, Sigma Aldrich, Mn = 45,000-55,000) in chloroform ($CHCl_3$) and is spin coated at 2000 rpm for 30 seconds. It is cured for 1 hour under inert conditions using a 254 nm UV lamp. The self-alignment of the Au source and drain electrodes as well as the thermal evaporation of the semiconductor have been performed as described in chapter 7.3. To ensure comparability of the transistors on different substrates, the semiconductor is applied to all samples in one single run, while the substrate holder is rotating at 8 rpm. First sintering tests with solution processable copper were performed using Intrinsiq CI-002 copper ink (Intrinsiq Materials Inc).

All electrical measurements are performed in darkness under ambient conditions using an mb parameter analyzer by mb technologies. All parameters extracted from the electrical characteristics are an average of forward and reverse sweep.

7.4. Results and Discussion

After the in depth analysis and testing of *OTFT*s with evaporated copper gate in chapter 5, tests to replace the gate electrode with printed copper were performed. The used ink has to be to be sintered by a high intensity light pulse. Unfortunately no light source matching the manufacturers specifications was available to the author. Despite best effort no conduction in the cured films could be measured when available light sources are used. In order to show working *OTFT*s with printed gate, silver was used as an alternative to copper. A first experiment was performed to evaluate whether evaporated Ag and printed Ag can be structured by NIL. The experiment reveals that the adhesion of evaporated silver on PET is not sufficient to cope with the high temperatures and forces present during the hot embossing process. The gate metal partially delaminates from the substrate, thus making the fabrication of transistors im-

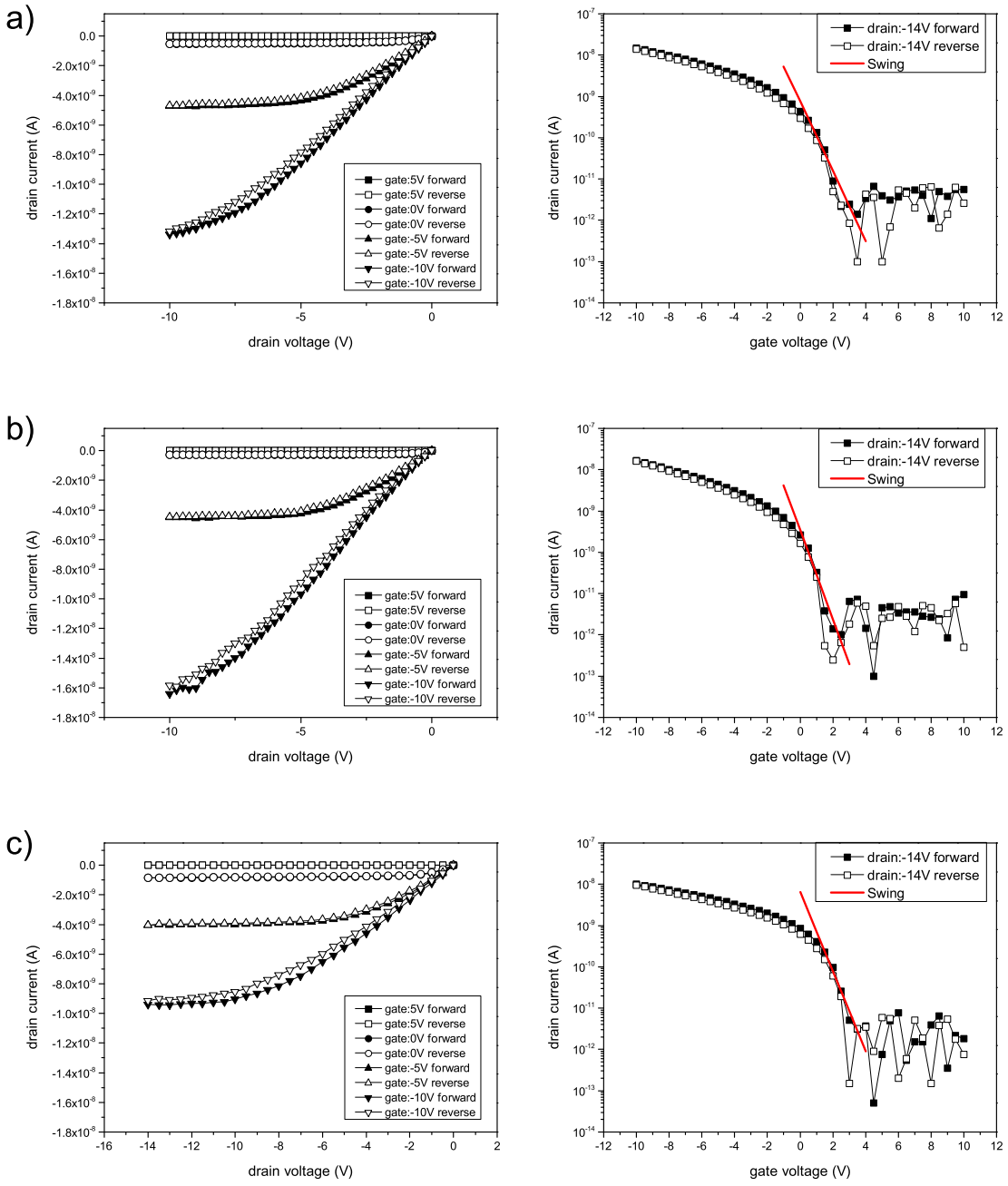

Figure 7.1.: Output and sub-threshold characteristics for a self-aligned, NIL structured OTFT with evaporated Cu (a), Cr/Ag (b) and printed Ag (c) as gate material.

possible. By introducing a thin chrome adhesion layer between the silver and the PET, working gate structures could be fabricated. Surprisingly, the adhesion of the printed Ag was high enough to withstand the NIL structuring without any adhesion promoters. It is thought that remaining compounds of the ink in the sintered film increase the adhesion to the PET foil. As a next step proof of principle self-aligned NIL transistors with evaporated Cr/Ag, printed Ag and copper gate are fabricated and compared. Figure 7.1 shows output and sub-threshold characteristics for devices with a channel length of $L = 5\,\mu m$ and a channel width of $W = 150\,\mu m$. All devices show comparable characteristics with negligible hysteresis and a saturation mobility of about $\mu_{sat} = 1 \times 10^{-3}\,cm^2/(V\,s)$. The maximum on-currents $I_{ON,max}$ (I_D @ $V_{GS} = -10\,V$, $V_{DS} = -14\,V$) for the Cr/Ag and Cu devices are $I_{ON,max} = -1.5 \times 10^{-8}\,A$ and $I_{ON,max} = -1.3 \times 10^{-8}\,A$ respectively. The subthreshold swing (slope of a linear fit through the I_D values between $V_{GS} = V_{ON}$ and $V_{GS} = V_{ON} - 1.5\,V$) and an effective on-current I^*_{ON}, corrected by V_{ON} ($I^*_{ON} = I_D$ @ $V_{GS} = -10\,V + V_{ON}$) are extracted. The values read $V_{ON} = 1.6\,V$, $S = 1.0\,V/dec$ and $I^*_{ON} = -1.1 \times 10^{-8}\,A$ for Cr/Ag and $V_{ON} = 2.5\,V$, $S = 1.2\,V/dec$ and $I^*_{ON} = -8.8 \times 10^{-9}\,A$ for Cu. The device with printed gate reveals $V_{ON} = 3.1\,V$, a swing of $S = 1.0\,V/dec$. I^*_{ON} is about a factor of two lower compared to the evaporated gate devices, being $I^*_{ON} = -5.5 \times 10^{-9}\,A$.

7.5. Conclusion

To conclude, self-aligned nanoimprint lithography structured organic field effect transistors with printed gate electrodes have been fabricated and compared to devices with evaporated gate electrodes. The data reveal no significant difference in performance, showing that the used process is fully usable for nanostructuring printed Ag. The results mark a first step towards the future goal of fabricating self-aligned $NIL\ OTFT$s consisting only of printable materials.

7.6. Acknowledgements

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8. Conclusion and outlook

In this thesis, nanoimprint lithography (*NIL*) was evaluated as a structuring method for printed materials used in two different organic transistor concepts, namely organic electrochemical transistors (*OECT*s) and organic thin-film transistors (*OTFT*s).

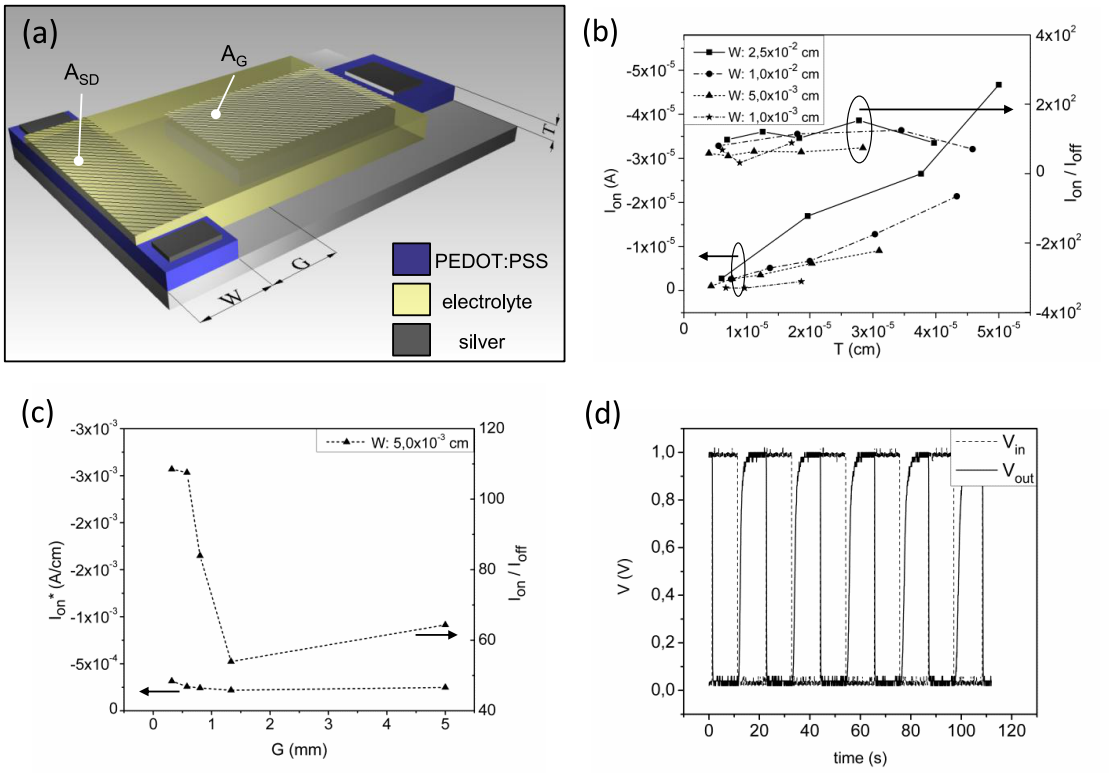

Figure 8.1.: a) Architecture of a lateral OECT, the varied geometry parameters are (i) the thickness T of the PEDOT:PSS, (ii) the gap G between the gate and the source-drain line and (iii) the width W of the source-drain line; Dependence of I_{ON} and I_{ON}/I_{OFF} b) on T and c) on G; d) Dynamic response of an *OECT* based inverter [1].

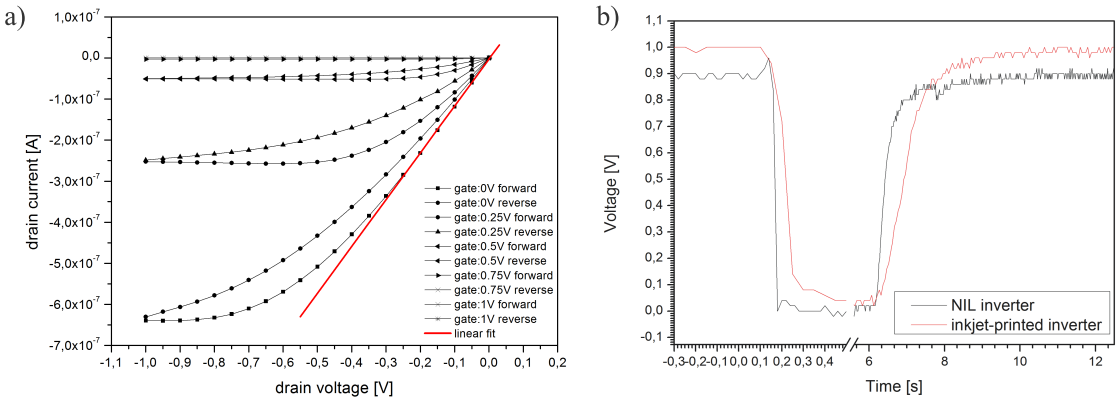

Figure 8.2.: a) Output characteristics of a *NIL* structured *OECT*; b) Dynamic response of electrochemical inverters to a square wave signal [2].

As at the beginning of the work for this thesis little research existed on *OECT*s, the first task was to identify and validate geometry parameters that improve the device performance. It could be shown using all-inkjet printed *OECT*s, that the on-current increases with the *PEDOT : PSS* layer thickness and width and that the on-to-off current ratio increases substantially with a smaller gap between the gate and the source-drain area [1] (Figure 8.1a-c). By optimizing these parameters it was furthermore possible to reduce the switching time from over 10 s to 4 s (Figure 8.1d).

The data indicated that a further size reduction of the devices should result in even higher device performance. Consequently, a *NIL* structuring process allowing for critical feature sizes below 10 µm in fully printed *OECT*s was developed and proof of principle devices were fabricated [2] (Figure 8.2a). Without any material modification the switching time could be further decreased to about 1 s (Figure 8.2b). Simultaneously, the on-to-off current ratio increased by one order of magnitude.

Note that the very same materials and working principles used for the *OECT*s in this work can also be applied to build electrochromic displays and thus allow for a one step fabrication of display pixels and driving transistors [3]. Thus, the increased switching speed of the *NIL OECT*s developed in this work can help

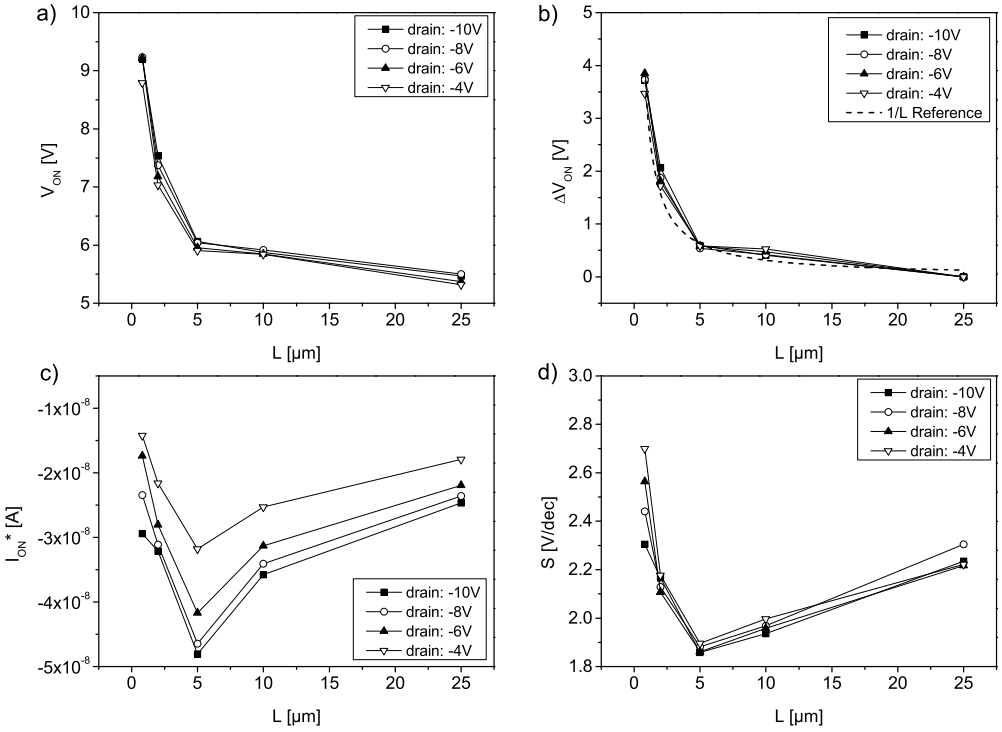

Figure 8.3.: Influence of the channel length on the (a) onset voltage, (b) onset voltage shift, (c) onset voltage normalized on-current and (d) onset swing; the 1/L fit in (b) for $V_{DS} = 10\,\mathrm{V}$ reads: $y = (3.1 \pm 0.2)\,/\,x$ [8].

in broadening the range of applications for such "smart" pixels. As comparable organic electrochemical concepts are also often used in sensors [4–7], the gained insights of this work can also help decrease the response time of such devices.

It has been shown in the past, that similar to the results achieved in *OECT*s in this work, *NIL* is also capable of reducing the critical dimensions of *OTFT*s and thus improve their performance [9–12]. For a future roll-to-roll (R2R) fabrication of such *NIL* structured *OTFT*s, the use of printed materials (which are also R2R processable) would be advantageous. Due to this the second part of this thesis focuses on the analysis of self-aligned, nanoimprint lithography structured organic thin-film transistors and the introduction of printed gates into the fabrication process.

As a first step, an already established *NIL* structured, self-aligned transistor process [11] was modified to better suit the needs of printed materials. The short

channel behavior of reference devices without printed materials was thoroughly evaluated[1] (Figure 8.3). Special focus was put on the parameters correlated to the threshold and sub-threshold transistor regime, namely the onset voltage and the swing (Figure 8.3b,d). The data revealed that for the given device system the short channel effects have a significant influence on the on-current and the swing for *OTFT*s with channel lengths below 5 µm. Furthermore, the high number of devices with similar electrical characteristics ($n > 70$) proved the reliability of the modified fabrication method.

In order to further investigate the capabilities and limitations of the modified fabrication process, in depth analysis of the influence of the gate-to-source and gate-to-drain overlaps on the *NIL OTFT*s were performed. In the applied self-alignment process the thicknesses of substrate and dielectric determine the magnitude of the gate-source and gate-drain overlap; the thinner the layers, the smaller the overlap. Accordingly, by optimizing the layer setup we had a tool for a further reduction of the overlap, thus supporting the continuous hunt for high speed transistors. In previous work, overlap lengths (L_{OV}s) as low as 30 nm have been demonstrated [11, 13]. This raised the question what the smallest possible overlap length maintaining proper DC transistor behavior and sufficient on-current level would be. Consequently, the reported self-alignment nanoimprint lithography (SANIL) process was modified such that the gate-to-source and gate-to-drain overlap lengths of coplanar *OTFT*s can be varied systematically[2]. Thereby, the influence of a varying and asymmetric overlap on the transistor characteristics can be analyzed and the influence of L_{OV} on the carrier injecting and extracting processes investigated. The results reveal that even devices with a gap of 200 nm instead of an overlap function as transistors. Nevertheless, the on-current decreases for devices with negative source overlap (Figure 8.4a). It was also found that for the investigated transistors a minimum overlap of about 200 nm is necessary to eliminate the influence of the overlap on the on-current. The on-current is surprisingly robust to variations of the overlap

[1] Rothländer et. al., Organic Electronics submitted

[2] Rothländer et. al., Applied Physics Letters submitted

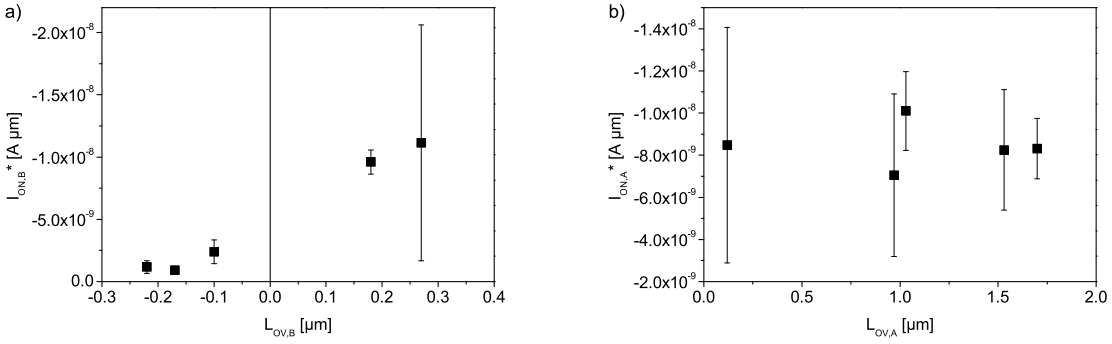

Figure 8.4.: Normalized on-current over source overlap when the varied source overlap switches from positive to negative and the drain overlap remains positive (A) and vice versa (B) [14].

length at the drain electrode, as no significant difference in the on-current is measured when varying the overlap from +1.5 µm to −0.2 µm (Figure 8.4b).

To achieve the set goal of the second part of this thesis the developed fabrication process was combined with printed materials. Self-aligned *OTFT*s with printed, *NIL* structured gate electrodes were fabricated. The characterization of the resulting transistors revealed no loss in performance compared to reference devices with evaporated gates (Figure 8.5). This result shows the high compatibility of *NIL* and printed electronics and is a major milestone for a future fabrication of fully solution processed *OTFT*s.

A comparison of the *OECT* and *OTFT* results achieved in this work is difficult due to their very different working and fabrication principles. While the *OTFT* has a much higher switching speed, allowing for the realization of circuits like e.g. radio frequency identification tags [15], it is more complex to fabricate (as it consists of more layers and materials) and imposes high requirements on the used materials. Especially the dielectric layer, which needs to combine electric strength with minimum layer thicknesses, and the mobility of the semiconductor as the bottleneck for high current switching should be mentioned. The *OECT*, on the other hand, has an intriguingly simple design. Charge carrier mobility is less of an issue, as it uses a conductor instead of a semiconductor. Downsides

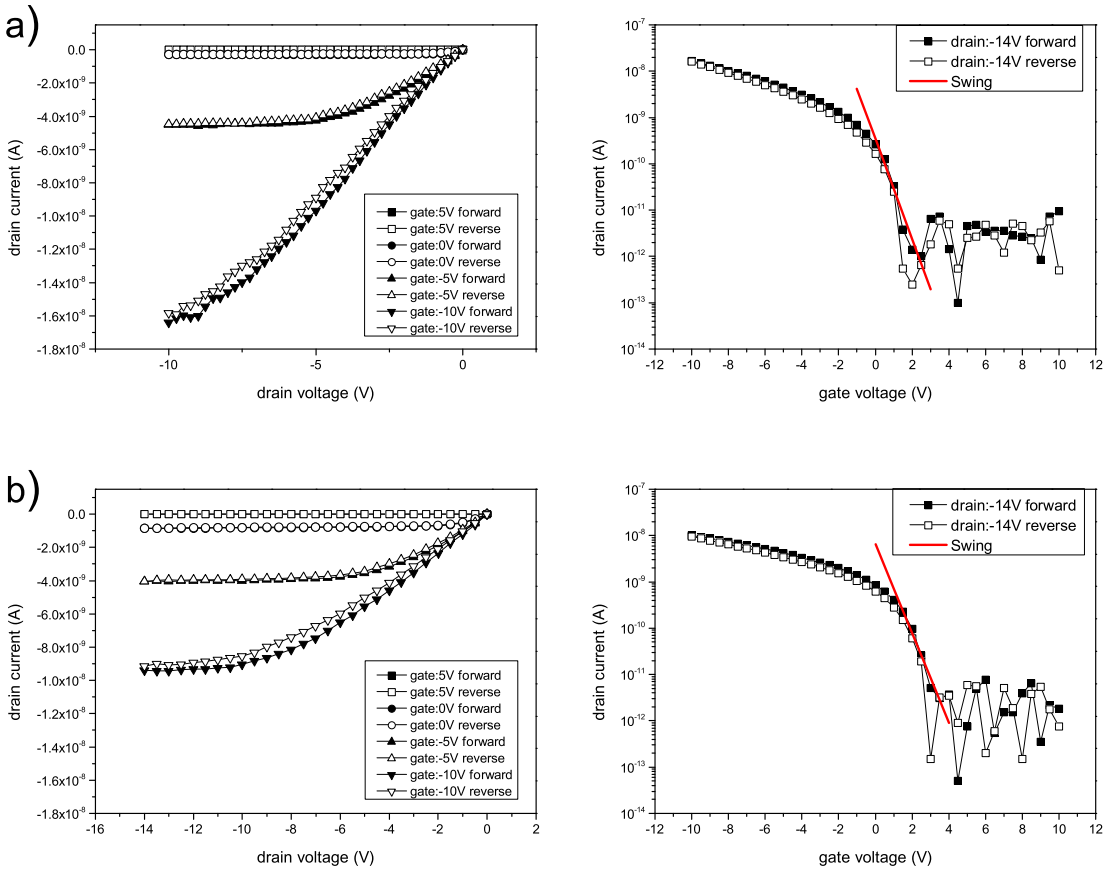

Figure 8.5.: Output and sub-threshold characteristics for a self-aligned, NIL structured OTFT with (a) evaporated Cr/Ag and (b) printed Ag as gate material.

of the *OECT* are its low switching speed and on-to-off current ratio, severely limiting the field of application for such devices.

Concerning the results achieved in *OECT*s, it has to be stated that although the *NIL* structuring showed a significant performance improvement, it did not fully meet the expectations. Despite a reduction of the identified geometry parameters by three orders of magnitude, the on-to-off current ratio and the switching speed increased by a much smaller factor. This indicates that a further size reduction will not lead to better performing transistors, because other paramters beyond the investigated geometry variations start to dominate the transistor behavior. Future work will deal with the determination and evaluation of these parameters. Concerning the dynamic behavior, the area of reduced

PEDOT : *PSS* spreading beyond the electrolyte area in the source/drain line was identified as the most probable dominating effect. As this area has no direct contact to the electrolyte, it takes a comparably long time to be oxidized again. This problem can be solved by covering the *PEDOT* : *PSS* next to the electrolyte with a higher conducting material [16, 17]. A main challenge will be to find a way to integrate this solution into the developed *NIL* process. Concerning a future low cost fabrication of the printed *OECT*s, a fully solution based process would be advantageous. The last remaining vacuum step in the process used in this work is the oxygen plasma etch to transfer the *NIL* pattern into the *PEDOT* : *PSS* electrodes. This could be replaced by a wet etch in the future, however with the disadvantage of possible pattern broadening due to the isotropic nature of a wet etch.

Regarding the introduction of printed materials into the fabrication of *NIL* *OTFT*s, a decisive milestone has been achieved by the *NIL* structuring of a printed gate electrode. As also the dielectric is already solution processed, two layers (source/drain electrodes, semiconductor) still rely on vacuum processes. The semiconductor can easily be replaced by a solution processed one [18, 19]. Replacement of the source/drain electrodes might be a more difficult task. The self-alignment process relies on a photo-lithographical structuring, which is not easily combined with printed materials. For *PEDOT* : *PSS*, a modified photo-lithography process has been reported by Huang et al. [20], which could be compatible with the fabrication method used in this work. Concerning a vacuum-process-free transistor, a replacement for the oxygen plasma etch to remove the residual resist after the imprint needs to be found. Very recently, Dhima et al. [21] presented a solution based residual removal technique combining thermal *NIL* and photo lithography that is in principle compatible with the process used in this work.

This work focuses mainly on single transistors. Consequently, the development of stable fabrication processes that allow for the use of the devices in circuitry should be the next major development milestone. For *OECT*s working logic

gates could be fabricated, both with and without the use of nanoimprint lithography. A detailed discussion of the achieved results will be an integral part of the PhD thesis of P.C. Hütter. Similar results for printed *OTFT*s have to be shown in the future.

In summary, this thesis could show that nanoimprint lithography is a great structuring method for printed materials in an organic electronics environment. The performance of organic electrochemical transistors could be improved by the high resolution structuring. The introduction of printed gate materials into the fabrication of *NIL* structured, self-aligned *OTFT*s did not decrease the already cutting edge performance of these devices.

Therefore, I believe in a bright future for printed high resolution organic electronics.

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Appendix

Appendix A.

Full papers

AIP | Applied Physics Letters

Influence of geometry variations on the response of organic electrochemical transistors

Philipp C. Hütter, Thomas Rothländer, Anja Haase, Gregor Trimmel, and Barbara Stadlober

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Influence of geometry variations on the response of organic electrochemical transistors

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We report on the fabrication and characterisation of entirely inkjet-printed organic electrochemical transistors (OECTs) based on poly(3,4-ethylenedioxithiophene) poly(styrenesulfonate) (PEDOT:PSS). These transistors were used to evaluate the assumed geometry-performance relationship of OECTs by changing the transistor dimensions and monitoring the output characteristics. We could show that the on-current depends on the PEDOT:PSS thickness and that the on-to-off current ratio is related to the distance between the printed electrodes. Taking these results into account, we fabricated entirely inkjet printed electrochemical inverters with a switching time of about 4 s. These inverters outline a first step from organic electrochemical transistors towards logic circuits. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4816781]

Since the discovery of conducting polymers in the late 1970s, a lot of research activities in polymer science aimed at developing printed electronic circuits, which combine multifunctional materials with low-cost production and a versatile form factor.[1] The key elements of any electronic circuit are transistors and resistors. There are two main concepts to build transistors based on organic materials: organic thin film transistors (OTFT) and organic electrochemical transistors (OECT). The simplest way to realize both organic resistors and organic transistors is based on printable conjugated polymers that can be used as printed resistors or if combined with electrolytes form an OECT. One well known example of such a polymer is PEDOT:PSS (poly(3,4-ethylenedioxithiophen) poly(styrenesulfonate)) which shows electrochemical switching over five orders of magnitude[2] via a voltage-induced reversible redox process.

OECTs have several advantages compared to organic thin film transistors. First, due to the absence of a gate dielectric, the charge carrier transport is not determined by the often imperfect quality of the interface between semiconductor and gate dielectric, which leads to trapping and performance instabilities. Second, due to the high capacitance of the electrolyte their operating voltage is very low, allowing for a switching of the OECTs in the range of 1 V and below. Third, only few materials and a very simple design are needed for OECTs thus decisively simplifying the printing process. Finally, they act as an ideal platform for the integration of electronic and biological systems, because of their unique ability to conduct both electronic and ionic carriers. Due to all these advantages, electrochemical transistors increasingly find their application in cell transport measurement,[3] circuitry for disposable electronics,[4] active-matrix physical sensor circuits,[5] and in chemical[6] and biological sensors.[7,8] A comprehensive overview of OECTs and OTFTs for chemical and biological sensing is provided in literature.[9]

An inherent characteristic of OECTs is that a positive input voltage is needed to switch the transistor, resulting in a negative output voltage. This makes it impossible to drive a transistor with a preceding one.[4] To shift the negative output voltage to positive values, a voltage divider connected to the output of the transistor is needed. This combination of an OECT and a voltage divider is working as an electrochemical inverter, generating an output signal of logic 1 when the input is 0 and logic 0 when the input is 1. One major drawback of OECTs is their low switching speed which is a result of the intrinsically low mobility of the ions in the electrolyte and the limited speed of the redox reaction. We assume that the geometry of the device also has a substantial influence on the transistor speed. Although the general working principle of OECTs was investigated intensively,[10–13] there exists no comprehensive work on the geometry-performance relationship of OECTs; only the influence of the ratio between the gate area A_G and the source-drain area A_{SD} on the I(V) curves was investigated.[14,15] Additionally a faster response time of OECTs when the length of the source-drain line is decreased was observed.[16] The latter was also shown for transistors used in biosensing.[17]

Accordingly, we examined the effect of varying the transistor geometry on the IV-curves of printed OECTs in a systematic way. The OECTs were fabricated by inkjet printing and had a lateral configuration (see Fig. 1(a)). The optimized geometry of the OECTs was implemented in the fabrication of printed inverters which serve well to showcase the effect of fundamental OECT parameters in practical applications. These inverters are composed of high performing OECTs and PEDOT:PSS resistors, based on only three inks (PEDOT:PSS, Silver, Electrolyte), and exhibit a gain of 2.7.

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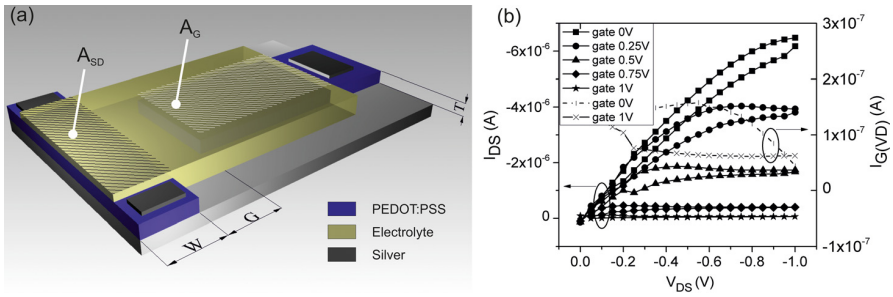

FIG. 1. (a) Architecture of a lateral OECT, the varied geometry parameters are (i) the thickness T of the PEDOT:PSS electrodes, (ii) the gap G between the gate electrode and the source-drain line, and (iii) the width W of the source-drain line (b) Output characteristics of an OECT with a non-optimized geometry ($W = 100\,\mu m$, $G = 1500\,\mu m$, $T = 180\,nm$) and an area ratio $A_G/A_{SD} = 10{:}1$, the gate current is plotted for $V_{GS} = -1\,V$ and $V_{GS} = 0\,V$.

The gate electrode and the source-drain line of the transistor are formed by inkjet printing of PEDOT:PSS on PET (polyethyleneterephthalat) substrates. A silver pad ensures good contact between the electrodes and the measurement circuits. A cationic electrolyte is applied by inkjet printing between gate and channel, thus covering parts of the source-drain line and the gate electrode. The voltage divider which is used to form an inverter is printed with PEDOT:PSS and silver ink. As the substrate for all devices we use untreated Melinex ST725 PET foil from DuPont®. Inkjet printing processes are done with the Fujifilm® Dimatix Material Printer DMP 2800 with Dimatix DMC 11610 printing cartridges. The substrate temperature during printing is 40 °C for PEDOT:PSS and silver ink. The PEDOT:PSS Clevios P Jet HC from H.C.Starck® is filtered with a 0.2 μm PET filter. The silver is processed either by hand (Electrolube® silver conductive paint) or by inkjet printing. The inkjet printed silver Cabot® CCI-300 is sonicated for 15 min and filtered with a 0.2 μm PET filter before use. After printing, the ink is sintered on a hot plate for 30 min at 100 °C. The electrolyte is also applied either by hand or by inkjet printing. When inkjet is printed, 20 layers of electrolyte are applied on the substrate at ambient temperature. The used polyelectrolyte formulation consists of: 51 wt. % deionized water, 33 wt. % Poly(sodium-4-styrene sulfonate), 8 wt. % D-sorbitol, and 8 wt. % glycerol (85 wt. %), as found in literature.[18] For electrical characterization, a Suess Microtec® probe station and a MB Technologies® parameter analyzer are used and for the dynamic measurements a Thurlby Thandar Instruments® TG230 frequency generator and a Tektronix® TDS 2014 B oscilloscope. The different thicknesses of the layers are measured with a Dektak Profilometer by Bruker. All process steps are carried out under ambient conditions.

Three different geometry parameters of OECTs were investigated (Fig. 1(a)). First the thickness T of the PEDOT:PSS electrode was varied by increasing the number of printed layers of PEDOT:PSS. Then the gap G between the gate and the source-drain line was tuned. Finally, different line widths W were investigated. While modifying the geometry parameters of the devices, the ratio of the active area (area covered with electrolyte) between the gate electrode A_G and the source-drain line A_{SD} (see Fig. 1(a)) was held constant at a ratio of 10:1. Thus the reported influence of the area ratio on the on-to-off ratio could be excluded.[15] From the I_{DS} (V_{DS})-characteristics basically two parameters were extracted and compared with respect to the device geometry—the on-current I_{on} (I_{DS} at $V_{GS} = 0\,V$, $V_{DS} = -1\,V$) and the on-to-off ratio I_{on}/I_{off} (with $I_{off} = I_{DS}$ @ $V_{GS} = -V_{DS} = 1\,V$).

In Fig. 1(b) a typical I_{DS}-V_{DS} curve of an organic electrochemical transistor with inkjet printed PEDOT:PSS and non-optimized geometry is displayed.

From the on-current $Ion = -6.48 * 10^{-6}$ A and the off-current $I_{off} = -6.54 * 10^{-8}$ A an on-to-off ratio of $1 * 10^2$ is extracted. Between forward and reverse drain voltage sweep a clockwise hysteresis in the drain current is observed which results from the slow motion of the ions during the switching process; the respective gate switching current is also plotted in Fig. 1(b) and is in the order of $1 * 10^{-7}$ A.

The electrodes' thickness T of transistors with nominal line widths $W = 10\,\mu m$, $50\,\mu m$, $100\,\mu m$, $250\,\mu m$, and a gap $G = 1500\,\mu m$ was modified by multiple printing of PEDOT:PSS layers. Thickness values between 40 and 75 nm were obtained for one layer of printed PEDOT:PSS. For two, three, five, and seven layers of successively printed PEDOT:PSS, thickness values up to 450 nm were achieved. It can be assumed that a variation of T results in a change of the electrical properties of the PEDOT:PSS electrodes such as the conductivity (Fig. 2(a)). A decrease of the sheet resistance R_S with increasing thickness values T is observed, following the expected 1/T dependence.[19] From $R_S = \rho/T$, a resistivity of $\rho = 0.01578\,\Omega{\cdot}cm$ is deduced, which corresponds to a conductivity of $\sigma = 63\,S/cm$ of the printed PEDOT:PSS layer.

The effect of varying T on the OECT parameters is plotted in Figs. 2(b) and 2(c). The on-current I_{on} increases approximately linearly with the line thickness T (Fig. 2(b)) being consistent with the 1/T decrease of the sheet resistance. Since the linear $I_{on}(T)$ correlation is valid for lines with different width W, the normalized $I_{on}^*(T)$ curves collapse together (Fig. 2(c)). Here I_{on}^* corresponds to I_{on} divided by the actual line width W*; the latter can differ from the nominal line width W due to the limited alignment accuracy and the spreading of the PEDOT:PSS ink. The linear fit to the normalized on-current results in $I_{on}^* = -15.6 \times T$. In a simple model I_{on}^* can be calculated from the linear part of the I(V) curve according to $I_{on,\,calc}^* = V/(R_S \times L) = (V/L) \times \sigma \times T$. In our example, $L = 2.5\,cm$ is the length of the printed S-D line, $V = -0.7\,V$ is the voltage range of the linear I(V)-part. Taking the conductivity $\sigma = 63\,S/cm$ from the fitted sheet resistance in Fig. 2(a), $I_{on,\,calc}^* = -17.6 \times T$ which is very close to the fitted I_{on}^* line.

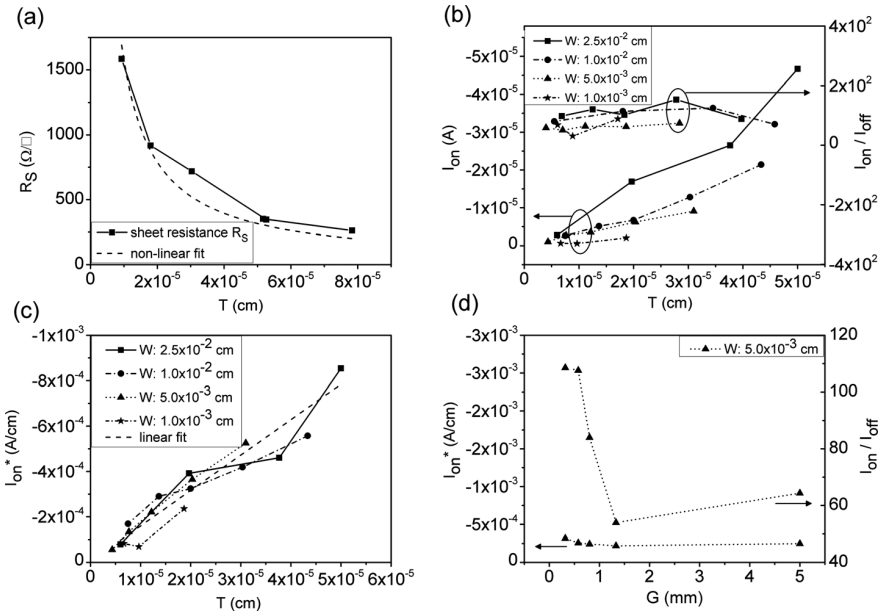

FIG. 2. (a) Dependence of sheet resistance R_S on PEDOT:PSS thickness T; fit-equation $R_s = 0.01578 \times T^{-1}$. (b) Dependence of the on-current I_{on} and of the on-to-off ratio on the line thickness T. (c) Dependence of the normalized on-current I_{on}* on the line thickness T; I_{on} is normalized to the widths of the source-drain lines W*; fit- equation $I_{on}* = -15.60158 \times T$ (d) Dependence of the on-current and the on-to-off ratio on the gap G for transistors with $W = 0.05$ mm and $T = 120$ nm.

The on-to-off ratio seems to be independent of T, meaning that I_{off} increases with T equivalently to I_{on} (Fig. 2(b)). The same observation holds for the dependence of the on-to-off ratio on the width W. A possible explanation for this might be the slower reduction of the PEDOT:PSS in the deeper regions of the source-drain line and in regions farther away from the gap edge. This leads to a graduation of reduced material during the measurement with mostly unreduced, high conducting material on the bottom of the line and fully reduced material on the top of the line, resulting in a higher overall off-current. This so-called reduction front is moved from the top towards the bottom of the line by the gate field and from the gap-sided electrode edge to the other. We can conclude that it is possible to increase the on-current by increasing the PEDOT:PSS line thickness T (and the width W), but the on-to-off ratio remains virtually unchanged.

Next, the influence of the gap G on the device performance is examined. All OECTs in this experimental setup had a nominal line width $W = 50\ \mu$m and a thickness $T = 120$ nm (optimized values). G was varied between 500 μm and 5 mm. The magnitude of the on-current does not depend on G (Fig. 2(d)) which can be expected since the on-current is measured with no gate voltage applied. So there should be no influence of the current on the distance between the gate and the source-drain line. However, the on-to-off ratio clearly increases for small G values (Fig. 2(d)). This observation can be explained as follows: When the gap is small enough, the redox reaction time is sufficient to reduce the entire width of the source-drain line within one measurement cycle and the transistor can be switched off much better. An additional requirement for achieving a complete switch-off is a gate potential that is big enough to move the cations all across the source-drain line and cause a reduction of the whole line width. These two preconditions lead to a low off-current. Assuming a constant on-current, transistors with smaller gaps reach higher on-to-off ratios than transistors with larger gaps.

For the printing of the electrolyte, its viscosity had to be adapted and the minimum electrolyte volume for achieving satisfactory OECT characteristics had to be determined. It turned out that a minimum of 20 layers of electrolyte (50 μm thickness) is needed and that a 1 + 3 solution of electrolyte in deionized water is optimal with respect to high precision splash-free printing.

For printed inverters, transistors with high on-to-off ratios rather than high on-currents are needed. Therefore, we chose a geometry of the all-inkjet printed OECTs with a small gap value ($G = 500\ \mu$m) and a source-drain line width $W = 250\ \mu$m with only one layer of PEDOT:PSS. Their output characteristics (Fig. 3(a)) reveal $I_{on} = -4.5 * 10^{-5}$ A and $I_{off} = -2.7 * 10^{-8}$ A, leading to an on-to-off ratio of $1.6 * 10^3$ which is more than one order of magnitude higher than what has been achieved for devices with non-optimized geometry. The lower hysteresis may indicate a higher switching speed compared to transistors without optimized geometry (compare Fig. 1(b))

Based on this design rule electrochemical inverters were fabricated with the aim to determine the switching speed of the OECTs. As pointed out in the beginning, a voltage divider has to be printed and connected to the output of the transistor (Fig. 3(b)). This voltage divider is made of PEDOT:PSS and printed silver pads, the latter used to define the magnitude of resistance of the three needed resistors by their length. Considering the switch-on resistance of the transistor $R_{ON} = 32$ kΩ and the switch-off resistance $R_{OFF} = 18$ MΩ, resistors with R1: R2: R3 = 427 kΩ: 280 kΩ: 154 kΩ = 7.93: 5.20: 2.86 in length ratios were printed. For such a geometry and a symmetric voltage supply of $+V_{DD} = +3$ V and $-V_{DD} = -3$ V (see Ref. 8), an output voltage of 1 V when the transistor is switched on and 0 V when it is switched off can be achieved.

The transfer characteristics of such all-inkjet printed inverters show clear plateaus at the high and the low level (Fig. 3(c)). The voltage of the high level (transistor = on) is $V_{out} = 0.97$ V and the voltage of the low level (transistor = off) is $V_{out} = -0.01$ V, almost reaching the theoretical voltage levels. Moreover, the gain of 2.7 (Fig. 3(c) inset) is comparable to values reported in literature.[4] In general, these transfer characteristics confirm that the ratio of the resistors

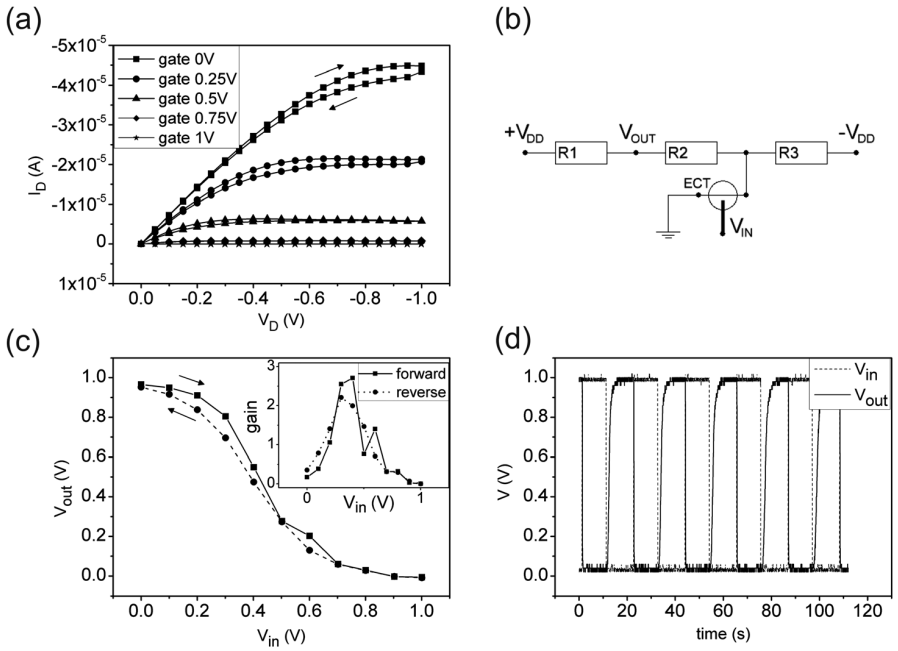

FIG. 3. (a) Output characteristic of an entirely inkjet printed OECT with W = 250 μm, G = 500 μm, T = 70 nm and an area ratio between the gate electrode and the active area on the source-drain line of 12:1; (b) circuit diagram of an electrochemical inverter; (c) transfer characteristic of an entirely inkjet printed inverter; Inset: Gain of the inverter (d) response characteristics for an electrochemical inverter.

as well as the supply voltages are appropriate and that the chosen design can be considered as functional.

Concerning their dynamical behavior a typical response to a square wave input signal with a frequency of 0.05 Hz is shown in Fig. 3(d). The high and low levels of +1 V and 0 V are constant for a measuring period of 110 s and also a fast response of the output voltage V_{out} on V_{in}, depicted by a very small shift of the two signals, is visible. Additionally, a speed difference in switching the transistor on and back off is observable. The switching speed of the inverter is determined by graphic extraction, resulting in a switch-on time of 3.3 s to achieve 0.9 V and a switch-off time of only 0.4 s to achieve 0.1 V. An explanation for this mismatch may be the edge of the reduction front. During the reduction process it is possible that this front is moving beyond the electrolyte edge towards the drain electrode. In this case, the reverse process of oxidizing the PEDOT and returning to the conducting state of PEDOT:PSS takes more time because the electrolyte, triggering the reaction, is not in direct contact with the PEDOT. The total switching speed is 3.7 s, when the on- and off-switching times are added, being in the same order of magnitude as reported for non-printed inverters with lateral design.[4]

In summary, our investigations on lateral all-printed OECTs concerning their geometry-performance relationship have shown that the on-current increases with the PEDOT:PSS layer thickness and, less pronounced, the width and that the on-to-off ratio increases substantially with a smaller gap between gate and source-drain area. We assume that reducing the gap to even smaller dimensions will further increase the on-to-off ratio. This will be investigated in future studies with structuring methods like Nano Imprint Lithography. The ink-jet printed inverters that account for these design rules show convincing on-off switching behavior. As logic gates, they will soon form the base for more complex circuits such as flip-flops and shift registers. Since only three materials are needed to realize these circuits in a very straightforward process, they have a strong potential for mass-fabricated low-cost and disposable electronics.

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Nanoimprint Lithography-Structured Organic Electrochemical Transistors and Logic Circuits

Thomas Rothländer, Philipp C. Hütter, Elisabeth Renner, Herbert Gold, Anja Haase, and Barbara Stadlober

***Abstract*— We report on the fabrication of organic electrochemical transistors structured by nanoimprint lithography. The devices were scaled down as a result of our previous findings for inkjet printed transistors, where a reduced source-drain width and a shorter distance to the gate resulted in higher ON-to-OFF current ratios. We could show that these findings also prove true for transistors with feature sizes below 10 μm. Furthermore, we fabricated inverters and NAND gates with switching times below 1 s. These logic gates mark an important step for organic electrochemical transistors toward their usability in more complex logic circuits.**

***Index Terms*— Electrochemical transistor, flip-flop, logic gates, nanoimprint lithography.**

I. Introduction

THERE are two main concepts to build organic transistors: the organic thin film transistor (OTFT) and the organic electrochemical transistor (OECT), the latter being studied in this paper. Using an electrolyte and the well-known conducting and printable polymer (poly(3, 4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS), electrochemical switching over five orders of magnitude via a voltage-induced reversible redox process has been shown and exploited in OECTs and circuits thereof [1]. Naturally, their performance depends heavily on the used materials, but different geometry parameters also play a significant role [2]–[4]. We could show for all-inkjet printed OECTs that the ON-to-OFF current ratio can be improved by reducing the width of the source-drain electrode (width W) and its distance to the gate (gap G) [5] [compare Fig. 1(a)].

In this paper, we aim to further exploit this relation by fabricating devices with a higher resolution than provided by inkjet printing. Thus it is necessary to pattern the PEDOT:PSS electrodes with minimum feature sizes of 10 μm and below. Different approaches to achieve this goal have been shown in literature. One technique is to rely on a previous surface treatment of the substrate, using structured hydrophobic layers [6], CF_4 etching [7], or self-assembled monolayers and V-shaped, embossed groves [8]. The methods are promising for producing feature sizes well below 1 μm, but the first two require a very good control over the drop volume to achieve thin layers while the third one requires a quite complicated, high-resolution surface treatment. PEDOT:PSS can also be mechanically structured, either by laser ablation [9], oxygen plasma etching using a stainless steel mask [10] or photolithography and liftoff [11]. However, in the context of low-cost production a roll-to-roll compatible, parallel structuring technique would be advantageous.

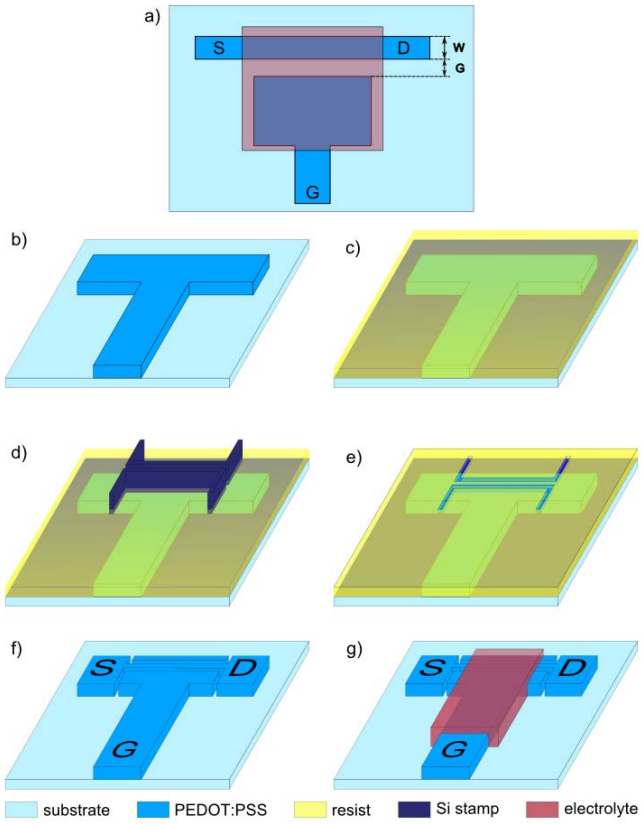

Fig. 1. (a) Schematic top view and (b)–(g) NIL-process scheme of a lateral electrochemical transistor; definition of the gap between the gate and the source-drain line G and the width of the source-drain line W (a). On a sample with (b) prestructured PEDOT:PSS an imprint resist (c) is applied by spin coating. Then a Si stamp with the wanted features is (d) pressed into the resist, the resist is UV-cured through the substrate and the stamp is removed, (e) leaving an etch-mask for the underlying PEDOT:PSS. The etch pattern is transferred using an oxygen plasma etch and the resist is (f) wet chemically removed. (g) As a last step the electrolyte is inkjet printed on the sample.

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Accordingly we introduce UV-based nanoimprint lithography (UV-NIL) as a high-resolution, high throughput patterning technique to structure PEDOT:PSS. Devices with a gap of $G = 6\ \mu$m and a width of $W = 13\ \mu$m were fabricated and measured. Full usability of the NIL-structured electrochemical transistors (NIL-OECTs) in higher integrated logic circuitry is demonstrated using inverters and NAND gates. Furthermore, the transistors are compared with our previously published all-inkjet printed OECTs in terms of static and dynamic behavior.

II. Experiment

The OECTs presented here consist of PEDOT:PSS (Clevios P Jet HC by Heraeus), an inkjet printable polymer electrolyte and silver ink (Cabot® CCI-300) for the contact pads. The electrolyte formulation consists of: 51 wt.% deionized water, 33 wt.% poly(sodium-4-styrene sulfonate), 8 wt.% D-sorbitol, and 8 wt.% glycerol (85 wt.%) [12]. As shown in Fig. 1(b)–(g) on an SF_6 plasma-treated PET foil (Melinex ST725 PET foil from DuPont®) the PEDOT:PSS electrodes are prestructured by inkjet printing using a Dimatix DMP 2800 inkjet printer. The substrate is held at room temperature during the printing process. The PEDOT:PSS film is dried on a hotplate held at 100 °C for 10 min. Next, a UV-curable imprint resist [13] is spin coated on top of the electrodes at 2000 r/min for 30 s. The resist is structured by UV-NIL using a silicon stamp and curing the resist through the substrate with an EVG 620 mask aligner. After separating the stamp from the sample, the resist acts as an etch mask. With an oxygen plasma dry etch in a reactive ion etcher from Oxford Instruments the pattern is transferred from the resist into the PEDOT:PSS lines. The sample is submersed in AZ 726 MIF photo developer (microchemicals GmbH) for 15 min and rinsed with IPA to remove the resist. To improve the electrical connection to the measurement tips, Ag contact pads are inkjet printed onto the electrodes at room temperature and cured at 110 °C for 10 min on a hotplate. As a last step the electrolyte is applied, again using inkjet printing [14].

III. Results and Discussion

A. Nanoimprint Lithography-Structured Electrochemical Transistors and Logic Gates

From Fig. 2, showing the output characteristics of a typical NIL-OECT with a gap of 6 μm and a width of 13 μm, the ON-current I_{ON} (I_{DS} at $V_{GS} = 0$ V, $V_{DS} = -1$ V), the OFF-current I_{OFF} (I_{DS} at $V_{GS} = 1$ V, $V_{DS} = -1$ V), and the ON-to-OFF-current ratio I_{ON}/I_{OFF} can be extracted. The shown device reveals $I_{ON} = 6.4 \times 10^{-7}$ A, $I_{OFF} = 1.0 \times 10^{-10}$ A, and $I_{ON}/I_{OFF} = 6.4 \times 10^3$. Peak devices showed an even higher ratio of up to 1×10^4. The maximum switching current is $I_{GS,max} = 1 \times 10^{-10}$ A and the largest hysteresis at $V_{GS} = 0$ V reaches 13% of I_{ON}. The hysteresis is due to the ions present in the electrolyte.

As a next step, all-printed NIL-structured OECT-based inverters using the circuit design [shown in Fig. 3(a)] were investigated. For the resistors inkjet printed PEDOT:PSS is used. To reduce the footprint of the circuit, the resistors are also structured by NIL. Ideally, the circuit acts as a voltage

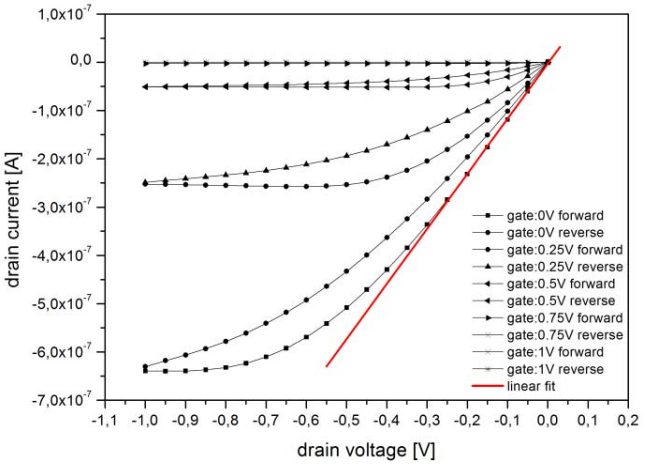

Fig. 2. Output characteristics of a NIL-structured electrochemical transistor. The width of the source-drain line $W = 13\ \mu$m and its distance to the gate $G = 6\ \mu$m. From the slope of the linear fit $R_{ON} = 875$ kΩ can be extracted.

divider between either $R3$ and $R1 + R2$ for a switched-off OECT or $R3$ and $R2 + R_{ON}$ for a switched-on OECT. In reality, the parallel resistances of R_{ON} and R_{OFF} ($R_{OFF} = R_{ON}$ at $V_{GS} = 1$ V) have to be considered. For the proper function, it is important that $R_{OFF} > R1 > R_{ON}$. Considering the ON- and OFF-resistances of the transistor [compare Fig. 2] ($R_{ON} = 875$ kΩ, $R_{OFF} = 3$ GΩ) and symmetrical supply voltages ($V_{DD} = 3$ V, $-V_{DD} = -3$ V) resistances of $R1 : R2 : R3 = 15$ MΩ : 25 MΩ : 40 MΩ should result in good inverter performance. Alternatively the supply voltages can be adjusted to compensate for a mismatch in the resistance ratios. One solid NIL-structured resistor line was fabricated and divided into the needed length parts by inkjet printed Ag contact pads. For the inverter [shown in Fig. 3(c)], the resistances revealed $R1 : R2 : R3 = 6$ MΩ : 16.6 MΩ : 37.7 MΩ and the supply voltages were adapted to $V_{DD} = 4.3$ V and $-V_{DD} = -2.1$ V, respectively. The device has clear plateaus at the high and the low level. The voltage of the high level (V_{Output} at $V_{in} = 0$ V) is $V_{Output,high} = 0.94$ V and the voltage of the low level ($V_{in} = 1$ V) is $V_{Output,low} = -0.03$ V. This result is in good agreement with the target voltage levels of $V_{Output,high} = 1$ V and $V_{Output,low} = 0$ V. The extracted gain of 3.8 [Fig. 3(c) inset] is comparable with values reported in [1] and [5].

To show that NIL-structured OECTs can be used for all Boolean logic operations, NAND gates are fabricated [15] [Fig. 3(b)]. The dynamic response of the NAND-gate [Fig. 3(d)] shows good logic switching behavior, the high-level V_{Output} value (representing Logic 1) shows a slight instability with plateau values in the range $V_{Output,high} = 1.01$–0.86 V; however, there is still a clear distinction to the low-level state (Logic 0) being $V_{Output,low} = 0.02$ V. The switching time was also measured, revealing a mismatch between switching the device from the ON-state to the OFF-state ($t_{OFF} = 0.03$ s) and back on again ($t_{ON} = 0.9$ s) [Fig. 4(c)].

There are three different artifacts visible in the NAND characteristics that can also be found in [1]. The sharp peak labeled "1" in Fig. 3(d), when OECT1 is switched on and

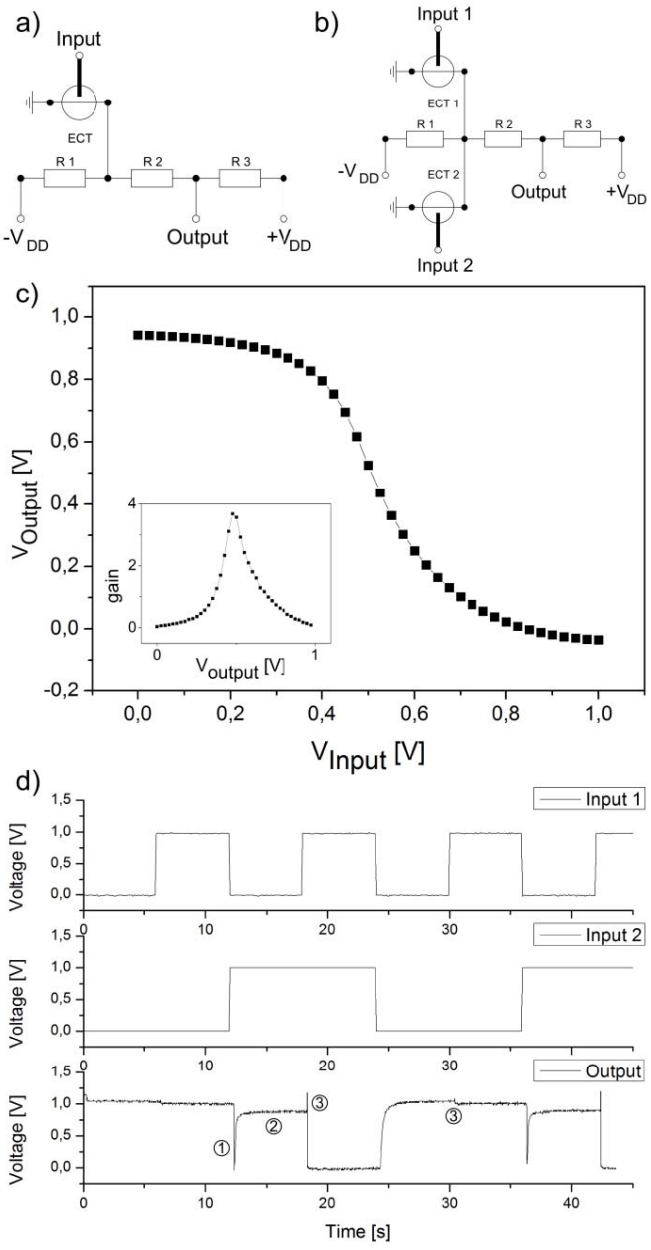

Fig. 3. Circuit design for (a) electrochemical inverter and (b) NAND gate [1], (c) inverter transfer characteristics with the gain as an inset, and (d) dynamic response of an electrochemical NAND gate to two square wave input signals. The highlighted artifacts (1–3) are described in detail in Section III.

OECT2 is switched off, is a result of the mismatch of the switching times. As stated above, OECT2 switches off over 0.03 s, so for a short time both transistors are off. This results in the visible short drop of V_{Output} toward the logic 0 state. The $\Delta V_{\mathrm{Output}} = 0.2$ V drop in the logic 1 level when OECT 1 is on and OECT 2 is off [labeled "2" in Fig. 3(d)] is a result of the higher R_{ON} of OECT 1 (and thus the higher parallel resistance to R1). The output characteristics of both OECTs used in the NAND gate can be found in Appendix A (Fig. 5). The third artifact appears whenever OECT 1 is switching off, especially pronounced when OECT 2 is also off [labeled "3" in Fig. 3(d)]. It is not a stable artifact but varies both in height and transistor number from device to device. It is only visible when the

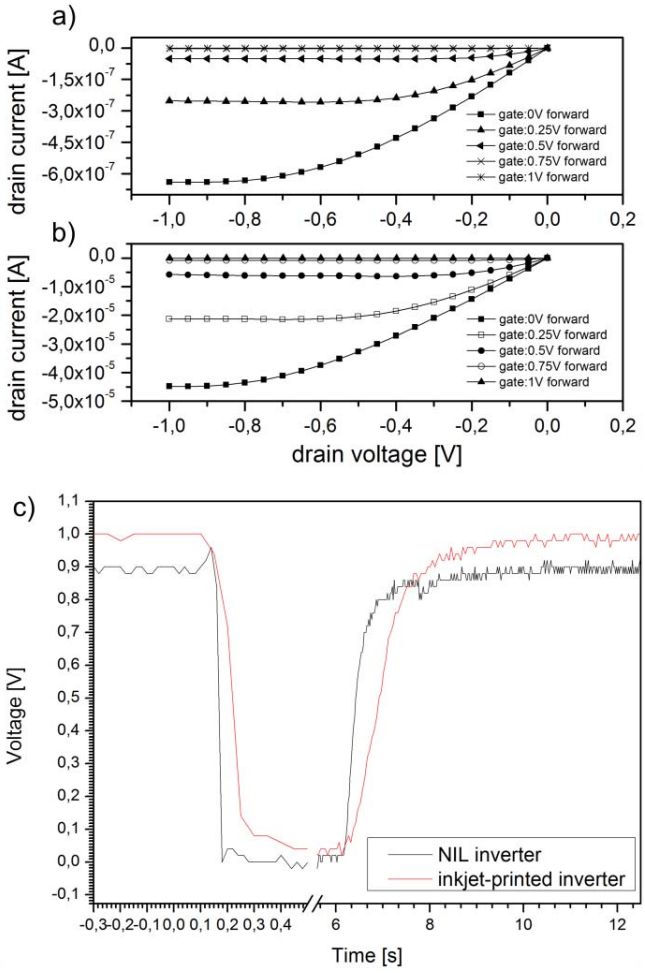

Fig. 4. Output characteristics of (a) a NIL-structured and (b) an inkjet-structured OECT, and (c) dynamic response of electrochemical inverters to a square wave signal. The switching times can be graphically extracted and read $t_{\mathrm{OFF}} = 0.9$ s, $t_{\mathrm{ON}} = 3.3$ s (inkjet) and $t_{\mathrm{OFF}} = 0.03$ s, $t_{\mathrm{ON}} = 0.9$ s (NIL).

NIL-OECT switches off and in all devices most prominent when both transistors are switched off. The artifact is thought to be a result of parasitic capacitances between the gate and the source-drain line. When both transistors are off, the parasitic capacitance is discharged through the voltage divider and thus results in a peak in V_{Output}. This is in good agreement with the smaller change in V_{Output} when only OECT1 switches off, since then part of the parasitic charge can flow over OECT2 to ground and the voltage divider is less affected.

B. Comparison With All-Inkjet Printed Organic Electrochemical Transistors

Compared with the all-inkjet printed transistors published elsewhere, the ON-current is two orders of magnitude lower for the NIL-structured devices [compare Fig. 4(a) and (b)] [5]. This is not only a result of the decreased device geometries, but also the process steps performed on top of the PEDOT:PSS. I_{ON} is lowered because the width of the S-D line is one order of magnitude smaller. Also the sheet resistance of the PEDOT:PSS lines rises significantly because of the exposure to the NIL process steps. A control experiment, where the

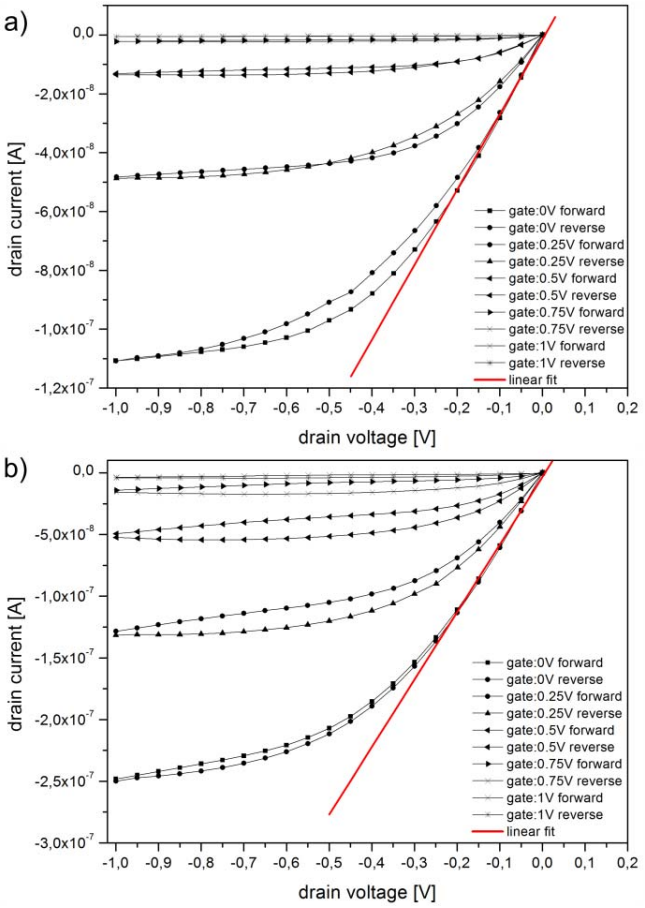

Fig. 5. Output characteristics of (a) OECT1 and (b) OECT2 used for the NAND-gate.

sheet resistance of all-inkjet printed PEDOT:PSS lines has been measured before and after being exposed to application, curing, and stripping of the resist, revealed an increase from about 1 kΩ/square to 300 kΩ/square. On the other hand I_{ON} is increased because the length of the source-drain line is reduced from 20 to 1 mm. The PEDOT:PSS thickness is in the same order of magnitude for both the all-inkjet printed and the NIL-structured devices, being around 100 nm. Despite the lower ON-current the ON-to-OFF ratio has improved up to one order of magnitude. This represents a further continuation of the trend that reducing both width and gap has a positive influence on the transistor performance.

Concerning the dynamic behavior of the OECTs, the NIL-structured transistors show an overall switching frequency of approximately 1.1 Hz. Compared with the 0.27 Hz of the inkjet printed OECTs the switching speed only improved by a factor of four [compare Fig. 4(c)]. This indicates that an effect different from the dimensions W and G seems to dominate the switching speed for small geometry devices. The reduction front moving beyond the electrolyte area and toward the drain electrode when switching the OECT off may be this dominant effect [16]. When switching the device back on, this area takes a relatively long time to be oxidized again. This is supported by the dynamic behavior, which is heavily dominated by the time needed to switch the device from the OFF-state to the ON-state. While in all-inkjet printed OECTs the switching time ratio is $t_{ON}/t_{OFF} = 8.3$, the NIL-OECTs show a ratio of $t_{ON}/t_{OFF} = 30$. This explanation can be further backed by literature as switching speeds over 1 Hz have to the best of our knowledge only been reported for device geometries where this reduction front is suppressed (e.g., by replacing the PEDOT:PSS not covered by electrolyte with a conductor [3], [17]) or not affecting the switching at all (e.g., in a vertical electrochemical transistor design) [18].

IV. Conclusion

To conclude we could show that it is possible to use nanoimprint lithography for the structuring of PEDOT:PSS and fabricate fully printed organic electrochemical transistors as well as logic circuits. Reducing the device geometry both the ON-to-OFF current ratio and the switching speed were improved. The results indicate that further size reduction might not lead to better device performance, as other influences beyond the geometry start to dominate the dynamic transistor behavior. Future work will deal with the determination and evaluation of these influences (e.g., by suppressing the reduction front, modulating the gate area, or comparing different electrolytes) for different device geometries. Nevertheless, we could show that lateral electrochemical transistors can exhibit good switching speeds and high ON-to-OFF current ratios. With the successful fabrication of logic gates future application as flip-flops or shift registers and more complex devices with electrochromic displays can be addressed.

Appendix

Fig. 5 shows the output characteristics of the two NIL-OECTs used for the NAND gate. The on-resistances can be calculated from the slope of the linear regime. For the devices R_{ON} equals $R_{ON,OECT1} = 3.9$ MΩ and $R_{ON,OECT2} = 1.8$ MΩ, respectively.

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Appendix B.

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