Thomas Rothländer

Organic Electronics: Complementary Inverters and Ring Oscillators

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Ao. Univ.-Prof. Mag. Dr.rer. nat. Joachim Krenn

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Abstract

Organic electronics has become a promising technology for applications requiring large-area coverage, mechanical flexibility and low-temperature processing. The implementation of organic electronics in various market segments is in fast progress and the organic contribution to all-day electronic devices is forecasted to massively enhance within the next 20 years.

The target of this work is the experimental realization of organic complementary inverters and ring oscillators. As a starting point all devices are fabricated with shadow masking techniques, resulting in transistors with a channel length of 100 μm. The active materials for the inverters are pentacene and PTCDI-$C_{13}H_{27}$. Once the fabrication know-how as well as the electrical behavior are sufficiently studied, ring oscillators are processed. Detailed studies concerning behavior and influence of different parameters on the oscillation will be performed.

As a next step the transistor channel lengths are reduced to the submicron regime, using the nanoimprint lithography technique. This results in higher device switching frequencies and better packing densities. The basis of this research is reported in [Haas 06].

With working ring oscillators a proof of the dynamic switching capabilities of our organic transistors is given.

Zusammenfassung

Organische Elektronik hat sich zu einer zukunftsträchtigen Technologie für Anwendungen entwickelt, die großflächige, mechanisch flexible Substrate und niedrige Prozesstemperaturen benötigen. Erste Produkte mit organischer Elektronik sind bereits auf dem Markt und ihre Zahl wird sich in den nächsten 20 Jahren massiv erhöhen.

Das Ziel dieser Diplomarbeit ist die Herstellung von organischen komplementären Invertern und Ringoszillatoren. Im ersten Teil werden alle Bauteile mit Hilfe der Schattenmaskentechnik hergestellt. Dies ermöglicht die Herstellung von Trasistoren mit einer Kanallänge von 100 μm. Als Halbleitermaterialien kommen Pentacen and PTCDI-$C_{13}H_{27}$ zum Einsatz. Diese werden bezüglich ihres elektrischen Verhaltens eingehend evaluiert. Im Anschluss werden Ringoszillatoren hergestellt und verschiedenste Einflüsse auf die Oszillation untersucht.

Um die Effizienz der Bauteile im Bezug auf Schaltgeschwindigkeit und Integrierbarkeit zu verbessern, kommt eine weitere Herstellungstechnik, die Nanoimprint Lithographie, zum Einsatz. Diese ermöglicht die Herstellung von Transistoren mit einer Kanallänge von unter 1 μm. Die Grundlagen zu dieser Technik sind in Referenz [Haas 06] nachzulesen.

Mit Hilfe von funktionsfähigen Ringoszillatoren wird die Möglichkeit der Inverter, dynamische Schaltvorgänge auszuführen, nachgewiesen.

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Introduction

Motivation - Why organic electronics?

The traditional semiconductor technology based on amorphous silicon has reached a point, where further improvements in primarily device packing density can only be reached with structure sizes down to less than 100 nm. The necessary technological effort as well as the investment costs to achieve this task are huge. Furthermore new product ideas require underlying electronics capable of being large-area coverable, structurally flexible and using substrate materials like plastic or paper. Furthermore disposable products are demanded, making low cost fabrication crucial.

A lot of these requirements can only be partially or not at all realized with silicon-based transistor technology. Especially the high processing temperatures make the fabrication of thin film transistors (TFTs) on plastic substrates only conditionally possible [Dimitrakopoulos 01]. First results using amorphous silicon have been reported by [Graz 06].

A lot of techniques have been developed allowing for fast and cheap coverage of large area substrates. Ink-jet printing for example makes it possible to pattern large samples in a single step without any material waste. Another technique, nanoimprint lithography, realizes very high resolutions by transferring structures from stamps to a variety of materials. This fabrication method also allows for reel-to-reel processing and thus for high throughput and low fabrication costs.

All these processes rely on liquid source materials, making the usage of silicon difficult. On the other hand liquid precursors with insulating, conducting or semiconducting properties can be found in great number in the class of organic materials. This makes the usage of these organic materials in electronics an important research field. The necessary temperatures for processing organic materials (e.g. baking steps, polymerization, ...) are often lower than 200 °C, allowing for the usage of flexible, organic or even biological substrates.

It needs to be stressed, that all the advantages of organic electronics come at a price. In the current point of view the performance and capability of organic thin-film transistors (OTFTs) will never reach crystalline silicon. The best mobility

reported to date is 2.4 cm^2/Vs. This reaches the values of amorphous silicon, but is still about three orders of magnitude lower than that of crystalline silicon [Taur 98, Dimitrakopoulos 02]. However, it can be assumed, that organic electronics plays a key role wherever low fabrication cost or large area coverage is important. The first generation of flat screens containing organic LEDs are on the market, for example smart cards or electronic paper are future applications.

Project scope of this work

The main target of this work is the experimental realization of organic inverters and ring oscillators. As a starting point all devices are fabricated with shadow masking techniques, as the process parameters are easier controlled. Starting with well working transistors first inverters are built. Once the fabrication know-how as well as the electrical behavior is sufficiently studied, ring oscillators are processed. Detailed studies concerning the behavior and influence of different parameters on the oscillation will be performed.

The next logic step in terms of device performance is the process transfer of inverters and ring oscillators to nanoimprint lithography. This results in higher device switching frequencies and better device packing densities. The basis of this research is reported in [Haas 06].

With this ring oscillators a proof of the dynamic switching capabilities of our organic transistors is given.

1. Theory

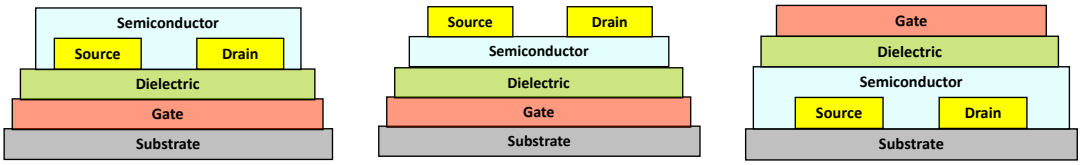
1.1 Organic transistor

1.1.1 Operation principle

A field-effect transistor is one of the most basic electronic devices. It consists of a semiconducting thin film with two electrodes on top, called source and drain. At the bottom a third electrode, the gate, is separated from the semiconductor by a dielectric layer (bottom gate, top source drain 1.1(b)).

Basically the transistor acts as a capacitance-controlled resistor. When a voltage is applied between source and gate, an electric field is induced, forcing the charge carriers to the insulator-semiconductor interface. This way a conduction channel is formed. The higher the gate voltage, the more charges form the channel, leading to higher conductance. Applying low voltages between source and drain leads to a current that follows Ohm's law, the transistor is in the linear regime. When the drain voltage reaches the gate voltage, the charge density saturates and the channel gets pinched off. The transistor is now in the saturation regime, where the current is independent of the drain voltage. This principle makes it possible to use the transistor to switch or amplify electronic signals. Furthermore it can be used to study charge transport in solid materials.

All organic transistors are thin film transistors, meaning that the different elements (dielectric, semiconductor, source, drain and gate) are fabricated as a multi-layer stack. There are different design possibilities, the most common shown in figure 1.1. In this work all nanoimprinted devices are bottom gate, bottom source drain devices (figure 1.1(a)), all the other devices are bottom gate, top source drain (figure 1.1(b)).



(a) Botton gate, bottom source-drain configuration

(b) Bottom gate, top source-drain configuration

(c) Top gate configuration

Figure 1.1: Common layer design possibilities for organic thin-film transistors

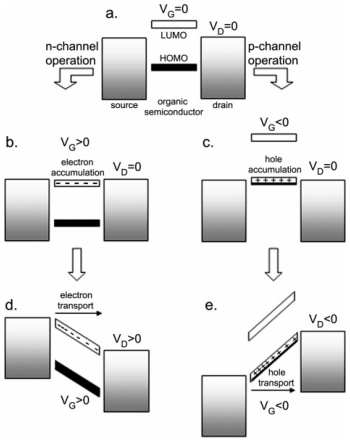


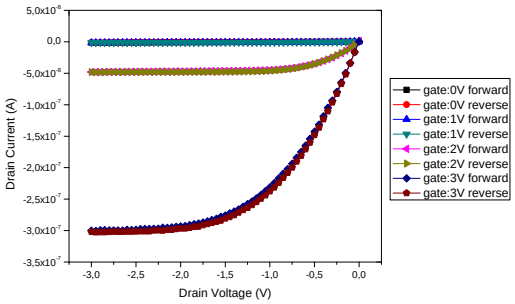
Figure 1.2: Idealized energy level diagram of an organic thin-film transistor [Newman 04]

1.1.2 Physics

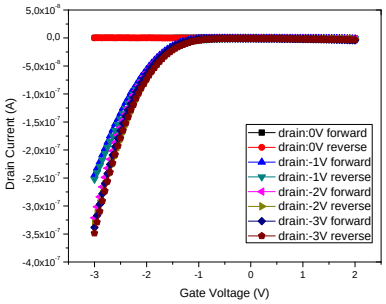
Band model

Physically the organic thin-film transistor can be explained using the energy-band model [Newman 04]. Figure 1.2 shows an idealized energy level diagram of a transistor. It shows the positions of the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) relative to the Fermi levels of the source and drain contacts. Applying a voltage between the two electrodes results in no conductivity, since there are no mobile charges in the semiconductor. By changing the gate voltage V_G, an electric field is induced, that causes the HOMO and LUMO levels to shift. In a p-channel operation a negative voltage is applied, resulting in the rise of the semiconductor levels. At a certain voltage the HOMO level becomes resonant with the Fermi levels and electrons can flow from the semiconductor into the contacts, leaving positively charged holes. The holes are now capable of charge transport, once a voltage is applied to the drain.

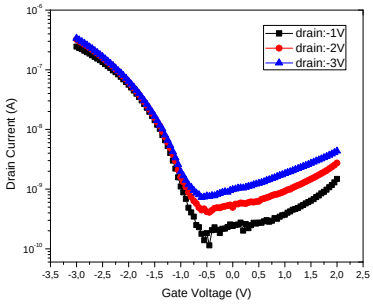
Of course this model is highly simplified, leading to some untrue assumptions. One is mislead to believe that by applying positive or negative gate voltage, one material can be used for both, electron and hole conduction. Experiments reveal that this is not the case for most organic semiconductors. The reason is that charge traps for



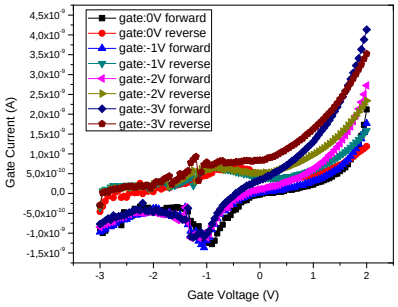
(a) Output characteristics



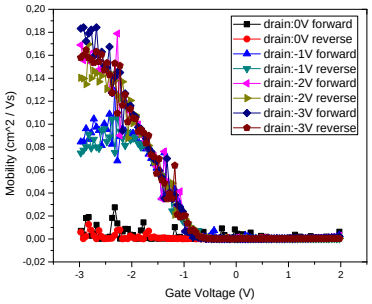
(b) Transfer characteristics



(c) Subthreshold characteristics



(d) Gate current vs gate voltage



(e) Charge carrier mobility vs gate voltage

Figure 1.3: Typical electrical measurements of a pentacene transistor

either holes or electrons are likely to occur at the semiconductor-dielectric interface preventing conductivity for that charge. Only if a lot of effort is put into a trap free fabrication of this interface, ambipolar behavior for a lot of organic semiconductors can be observed [Chua 05]. Because of this most of todays used organic semiconductors can only be made more conductive by applying a positive or a negative voltage, but not both. Hence they are classified according to their intrinsic properties into hole (p-type) or electron (n-type) conducting semiconductors. There are also a lot of further parameters influencing the charge transport and switching behavior of an organic transistor, as can be found in detail in references [Verlaak 04, De Vusser 06a].

Parameters

To give a better overview of the transistor parameters, figure 1.3 shows some typical results from an electrical measurement.

In the output characteristics (figure 1.3(a)) the drain current is plotted over the drain voltage, while the gate voltage is fixed. This nicely illustrates the two regimes of the transistor (compare chapter 1.1.1). The drain current for the linear regime can be written as:

$$I_{DLinear} = \mu_{FET} \frac{W}{L} C' \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right] \tag{1.1}$$

I_D	...	drain current
μ_{FET}	...	device mobility
W/L	...	transistor channel width to length ratio
C'	...	specific capacitance of the dielectric
V_G	...	gate voltage
V_T	...	threshold voltage
V_D	...	drain voltage

Once the transistor reaches saturation, the drain current becomes independent from the drain voltage:

$$I_{DSaturation} = \mu_{FET} \frac{W}{L} C' (V_G - V_T)^2 \tag{1.2}$$

The output characteristics is also used to extract the on- and off-currents, which are the current values at the highest gate voltage value for $\mathrm{V_D} = 0$ (off) and $\mathrm{V_D} = \mathrm{V_{DMax}}$ (on).
The transfer characteristics (figure 1.3(b)) is a $\mathrm{I_D(V_G)}$ plot, at a constant drain voltage. It gives a first clue of the switch-on voltage $\mathrm{V_{On}}$. This is the gate voltage where a current between source and drain greater than the off current can be measured. In our graph this voltage would be around $-1\,\mathrm{V}$. Again it is possible to extract the on- and off-currents. An easier way of extracting the information from the transfer characteristics is taking the absolute values of the current and display them in a semi-logarithmic scale (figure 1.3(c)). In this subthreshold characteristics it is much easier to extract $\mathrm{V_{On}}$, being around $-0.5\,\mathrm{V}$ at $\mathrm{V_D} = 3\,\mathrm{V}$. We are also able to see an leaking current of approximately $3 \cdot 10^{-9}\,\mathrm{A}$, which did not distinctly show up in the transfer curve. Looking at figure 1.3(d) it can be determined as being mostly a gate leaking current.

Finally figure 1.3(e) shows the transistor's charge carrier mobility over the gate voltage. This graph cannot be directly measured from the transistor, but it can be calculated from the transfer characteristics. For a saturated transistor the device mobility is given by:

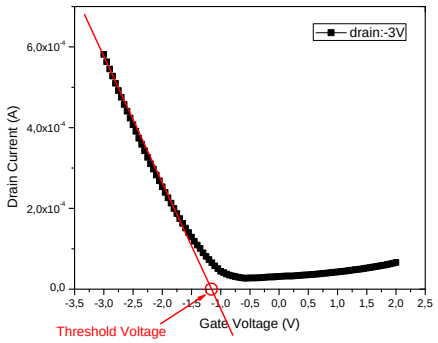


Figure 1.4: Graphical determination of the threshold voltage

$$\mu_{FET} = \frac{2L}{WC'} \left(\frac{\sqrt{\partial I_D}}{\partial V_G} \right)^2 \tag{1.3}$$

Another theoretically important parameter is the threshold voltage V_T. It is defined as the voltage needed to create inversion. Of course this only applies to inorganic electronics. Nevertheless since most of the formulae used to describe organic devices are taken from inorganic theory, it is needed for most of the calculations (for example equation 1.1). It can be extracted by plotting the square root of the drain current over the gate voltage. The intersection of a linear fit of the curve with the current axis is the value for V_T (figure 1.4). In organic electronics V_T is defined as the voltage, where an accumulation channel is formed between the source and the drain. Theoretically this process starts at $V_T = 0\,V$, but for real devices it is shifted, because a certain amount of charges are needed to fill up the traps at the dielectric-semiconductor interface [Stallinga 09].

Concerning the dynamic behavior of a transistor, usually the cut-off frequency is stated. This is the frequency, where the gate voltage is changed so fast, that the transistor is not able to form a conductive channel at the semiconductor-dielectric interface anymore. The transistor behaves as if it was off, although a gate voltage higher than the threshold voltage is applied [Sze 81]. The cut-off frequency is given by:

$$f_0 \leq \frac{\mu V_G}{2\pi L^2} \tag{1.4}$$

It needs to be stressed, that the switching time is decreased with the square of the channel length. This plays a key role in the motivation of device minimization to increase their performance (compare chapter 2.4).

If not defined explicitly the formulae used in this section to describe an organic transistor are taken from the model for inorganic transistors by William Shockley

[Shur 90]. Further details about his model and it's applicability on organic transistors are discussed in detail in references [Haas 06, Newman 04].

1.2 Organic inverter

1.2.1 Operation principle

Table 1.1: Logic table of an inverter

Input	Output
1	0
0	1

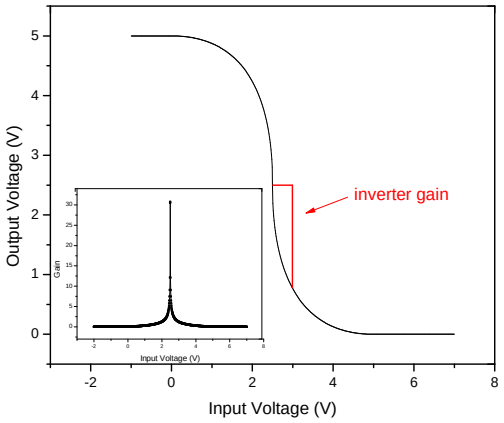


Figure 1.5: Transfer characteristics and gain

The inverter is, despite it's rather simple circuit design, the most important building block in digital logic circuits. It consists of two or more transistors and acts as a logic NOT gate, as shown in table 1.1. Figure 1.5 depicts a typical inverter transfer characteristics, where a low input signal transfers into a high output signal and vice versa.

Possible circuits can be built using unipolar (hole-only or electron-only) transistors or a combination of p-type and n-type transistors in a complementary design.

Gain

An important parameter of the inverter is the gain, which is the highest slope of the transfer curve (compare inset of figure 1.5). The higher the gain, the smaller the input voltage region, where the inverter is in an undefined logic state. This region is marked by V_{IL} and V_{IH} (figure 1.10). V_{IL} (V_{IH}) represents the maximum (minimum) input voltage that will still be recognized as logic low (high) by the inverter. They are defined as the points, where the slope of the transfer characteristics is:

$$\frac{dV_O}{dV_I} = -1 \tag{1.5}$$

1.2.2 Unipolar inverter

These type of inverters always consist of at least two transistors of the same type, but they can be connected in different manners. Generally they are divided into two categories, according to the threshold voltage V_T of the transistors.

Enhancement inverters

This group of inverters consists of either n-type transistors where $V_T > 0\,V$ or p-type transistors where $V_T < 0\,V$. When no bias is applied to the gate, no current is flowing between source and drain. To switch the n-type transistor on, a sufficient amount of positive voltage (negative voltage for a p-type) needs to be applied to the gate. Transistors acting in this way are called normally-off.

Depletion inverters

In this case the transistors are normally-on, meaning that their threshold voltage is negative for n-type and positive for p-type transistors. Hence a voltage has to be applied to the gate in order to switch the transistors off. (negative for n-type and positive for p-type).

Circuit design

The transistors fabricated in this work are all normally-off, so any further discussion concerning the design will refer to enhancement inverters. They consist of a load, a transistor, which has supply voltage connected to the source and the source of the second transistor connected to the drain. This second transistor is called switch, and has its drain connected to common. The gate of the switch acts as the signal input V_I and the connection between the load drain and the switch source as the signal output V_O. The gate of the load can be connected in different ways, all having their advantages and disadvantages. For further details concerning possible inverter circuits the interested reader is referred to [Hoffmann 93].

The design chosen for our unipolar inverters is the saturated load enhancement inverter, which is shown in figure 1.6. Generally a linear load enhancement inverter would have lead to a higher high and low level difference, but is not possible as the high gate voltages needed for this design are to high for our dielectrics.

In the chosen design the gate of the load is also connected to the supply voltage. This means the load can only work in saturation or in cutoff. When V_I is lower than the threshold voltage of the switch V_{TS}, the switch is off and no current is flowing between its source and drain. This leaves the load in cutoff mode, where only the threshold voltage of the load V_{TL} is lost.

$$V_{OHigh} = V_{Sup} - V_{TL} \tag{1.6}$$

V_O ... output voltage
V_{Sup} ... supply voltage

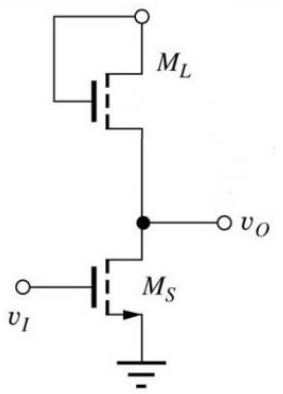


Figure 1.6: Circuit design of a saturated load enhancement inverter

When $V_I \geq V_{TS}$ the switch is turned on, going into linear mode. Since there is a current flowing, the load goes from cutoff to saturation, which leads to an additional voltage drop of V_{DL}.

$$V_O = V_{Sup} - V_{TL} - V_{DL} \tag{1.7}$$

When $V_I = V_{Sup} - V_{TL}$, the minimum of the output voltage V_{OLow} is reached. This minimum can be calculated by assuming that the current through the load and the switch should be equal.

$$I_L \stackrel{!}{=} I_S \tag{1.8}$$

$$\frac{\beta_L}{2} \cdot (V_{Sup} - V_{OLow} - V_{TL})^2 = \beta_S \cdot \left(V_I - T_{TS} - \frac{V_{OLow}}{2}\right) \cdot V_{OLow} \tag{1.9}$$

$$\frac{\beta_L}{2} \cdot (V_{Sup} - V_{OLow} - V_{TL})^2 = \beta_S \cdot \left(V_{Sup} - V_{TL} - V_{TS} - \frac{V_{OLow}}{2}\right) \cdot V_{OLow} \tag{1.10}$$

where

$$\beta = \frac{W}{L} \cdot \mu_{FET} \cdot C' \tag{1.11}$$

Solved for V_{OLow} we get a quadratic equation

$$V_{OLow} = V_{Sup} - V_{TL} - \frac{\beta_S}{\beta_L + \beta_S} \cdot V_{TS} \pm \sqrt{\left(V_{Sup} - V_{TL} - \frac{\beta_S}{\beta_L + \beta_S} \cdot V_{TS}\right)^2 - \frac{\beta_L}{\beta_L + \beta_S} \cdot (V_{Sup} - V_{TL})^2} \tag{1.12}$$

The positive sign has to be omitted for physical reasons (otherwise V_{OLow} could be higher than V_{Sup}). High threshold voltages lead to a good low level, but are hard to influence in organic transistors. Decreasing the supply voltage is also an option,

but this also worsens the signal-to-noise ratio. The third possibility is changing the β-ratio. A low V_{OLow} is achieved by choosing β_S to be much higher than β_L.

$$V_{OLow} \to 0 \Longrightarrow \frac{\beta_S}{\beta_L} \gg 1 \tag{1.13}$$

Since we are working with an unipolar inverter, the mobility as well as the specific capacitance are equal for the load and the switch, so the only changeable parameters are the W/L ratios.

The β-ratio also determines the gain of the unipolar inverter. It is given by:

$$G = \sqrt{\frac{\beta_S}{\beta_L}} \tag{1.14}$$

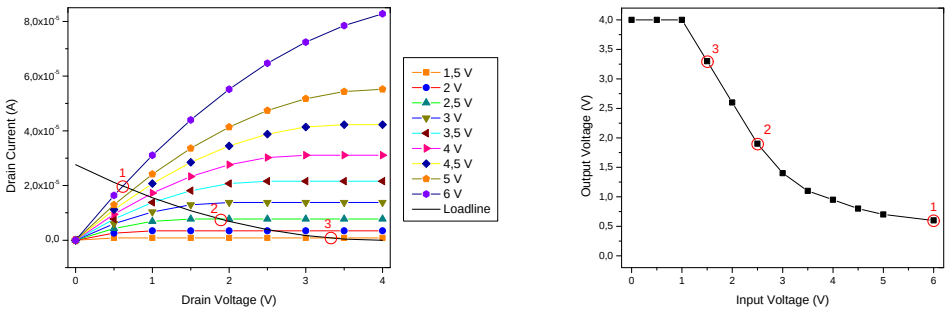
Further influences of the transistor can be demonstrated using the so-called load line construction. It allows to graphically determine the inverter transfer characteristics from the output characteristics of the switch and threshold voltage and the β-value of the load. Since the load is always in the saturated regime, the current through it at a given output voltage is defined by:

$$I_L = \frac{\beta_L}{2} \cdot (V_{Sup} - V_O - V_{TL})^2 \tag{1.15}$$

Plotting this load line into the output characteristics of the switch leads to the points along the inverter transfer characteristics (figure 1.7(a)). Again the currents through the load and the switch have to be equal (equation 1.8). Each intersection point of the load line with the output characteristics represents one point with current equality. The gate voltage of the switch curve represents the inverter's input voltage, the drain voltage at the intersection represents the inverter's output voltage (figure 1.7(b)).

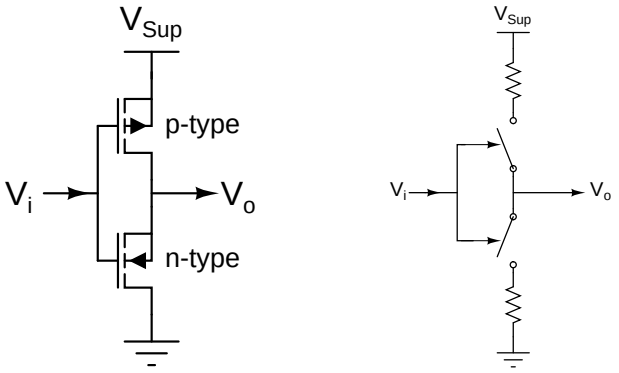
1.2.3 Complementary inverter

Complementary devices are much more popular than unipolar ones in inorganic electronics due to a wide range of advantages. These are for example a lower power dissipation, a higher noise margin, better robustness and easier circuit design. In organic electronics this advantages also apply, but come at a price. Organic n-type materials have a lower mobility, worse availability and an intrinsic instability upon exposure to air and moisture [De Vusser 06b]. Nevertheless, it is possible to cope with the disadvantages, as will be shown in chapter 3.2.2.



(a) Switch output characteristics with load line (b) Inverter tranfer characteristics

Figure 1.7: Graphical determination of the inverter transfer characteristics



(a) Circuit diagram (b) Equivalent circuit diagram

Figure 1.8: Different circuit schemes of a complementary inverter

Circuit design

The complementary inverter circuit consists of one p-type and one n-type transistor (figure 1.8(a)). The p-type transistor's source is connected to the supply voltage V_{Sup}. The gate and the drain are connected to the gate and the drain of the n-type transistor. The combined gate acts as the signal input V_I while the combined drain acts as the signal output V_O.

Table 1.2 shows the ideal switching behavior of the transistors during a whole inversion. When the inverter is in one of the logic states (V_{OHigh} or V_{OLow}) one of the transistors is off and the other is on, so there is no static power consumption. An equivalent circuit diagram of the complementary inverter is shown in figure 1.8(b).

Again the β-ratios greatly influence the device behavior, but in a different way than with the unipolar inverter. This can be shown by calculating the inverter threshold voltage V_{Ti} where

Table 1.2: Transistor operation regions in a complementary inverter

Region	signal input	signal output	n-type transistor	p-type transistor
1	$V_I < V_{Tn}$	$V_{OHigh} = V_{Sup}$	Cutoff	Linear
2	$V_{Tn} < V_I \leq V_O + V_{Tp}$	High	Saturation	Linear
3	$V_I \approx {}^{V_{Sup}}/_{2}$	${}^{V_{Sup}}/_{2}$	Saturation	Saturation
4	$V_O + V_{Tn} < V_I \leq V_{Sup} + V_{Tp}$	Low	Linear	Saturation
5	$V_I \geq V_{Sup} + V_{Tp}$	$V_{OLow} = 0$	Linear	Cutoff

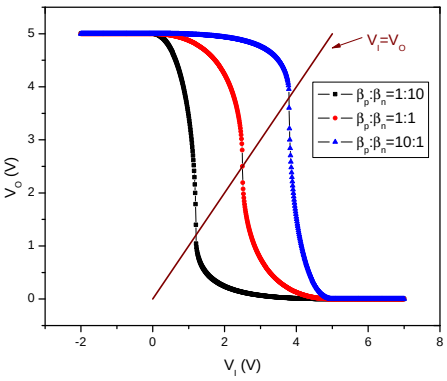


Figure 1.9: Switching point at different beta ratios

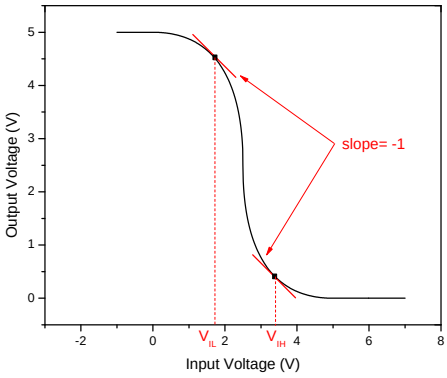


Figure 1.10: Logic voltage levels

$$V_{Ti} = V_I = V_O \tag{1.16}$$

At this point both transistors are in saturation and the current through both transistors is equal (compare table 1.2).

$$I_n \stackrel{!}{=} I_p \tag{1.17}$$

$$\frac{\beta_n}{2}\left(V_{Ti} - V_{Tn}\right)^2 = \frac{\beta_p}{2}\left(V_{Sup} - V_{Ti} - |V_{Tp}|\right)^2 \tag{1.18}$$

Solved for V_{Ti}:

$$V_{Ti} = \frac{V_{Tn} + \sqrt{\frac{\beta_p}{\beta_n}}\left(V_{Sup} - |V_{Tp}|\right)}{1 + \frac{\beta_p}{\beta_n}} \tag{1.19}$$

So the ${}^{\beta_p}/_{\beta_n}$ ratio shifts the switching point of the inverter. If ${}^{\beta_p}/_{\beta_n} = 1$ the inverter is called symmetrical, since it will switch from high to low level at ${}^{V_{sup}}/_{2}$. A higher ratio will shift V_{Ti} towards higher input voltages, a lower towards zero (figure 1.9).

It can also be seen that it is important for a symmetrical inverter that V_{Tn} and V_{Tp} are matching. With the same approach as equation 1.17 it is possible to show

further influences of the threshold voltages and the β ratios. We will calculate the input voltages V_{IL} and V_{IH} (see chapter 1.2.1).

For V_{IL} the p-type TFT is in the linear and the n-type TFT in the saturated regime (table 1.2). Assuming equal currents through both leads to:

$$\frac{\beta_n}{2}\left(V_{IL}-V_{Tn}\right)^2=\frac{\beta_p}{2}\left[2\left(V_{Sup}-V_{IL}-|V_{Tp}|\right)\left(V_{Sup}-V_O\right)-\left(V_{Sup}-V_O\right)^2\right] \quad (1.20)$$

The derivation condition for the slope is:

$$\frac{dV_O}{dV_I}=\frac{{}^{dI_{Dn}}\!/_{dV_I}-{}^{\partial I_{Dp}}\!/_{\partial V_I}}{{}^{\partial I_{Dp}}\!/_{\partial V_O}}=-1 \quad (1.21)$$

leading to:

$$V_{IL}=\frac{2V_O+\frac{\beta_n}{\beta_p}V_{Tn}-V_{Sup}-|V_{Tp}|}{1+\frac{\beta_n}{\beta_p}} \quad (1.22)$$

For V_{IH} the regimes are interchanged:

$$\frac{\beta_n}{2}\left[2\left(V_{IH}-V_{Tn}\right)V_O-V_O^2\right]=\frac{\beta_p}{2}\left(V_{Sup}-V_{IH}-|V_{Tp}|\right)^2 \quad (1.23)$$

$$\frac{dV_{out}}{dV_I}=\frac{{}^{dI_{Dp}}\!/_{dV_I}-{}^{\partial I_{Dn}}\!/_{\partial V_I}}{{}^{\partial I_{Dn}}\!/_{\partial V_O}}=-1 \quad (1.24)$$

leading to:

$$V_{IH}=\frac{2V_O+V_{Tn}+\frac{\beta_p}{\beta_n}\left(V_{Sup}-|V_{Tp}|\right)}{1+\frac{\beta_p}{\beta_n}} \quad (1.25)$$

For the high and low levels of the complementary inverter the off-currents and gate leaking currents are critical. Using the equivalent circuit diagram from figure 1.8(b) and treating the inverter as a voltage divider, the output voltage is defined as:

$$V_O=\frac{V_{Sup}}{R_p+R_n}\cdot R_n \quad (1.26)$$

and the high and low levels are:

$$High:\ R_n\gg R_p\Rightarrow V_O\approx\frac{V_{Sup}}{\cancel{R_n}}\cdot\cancel{R_n}=V_{Sup} \quad (1.27)$$

$$Low:\ R_p\gg R_n\Rightarrow V_O\approx\frac{V_{Sup}}{R_p}\cdot R_n\overset{R_p\to\infty}{\longrightarrow}0 \quad (1.28)$$

The lower the currents, the higher the resistances and the larger the difference between both levels. A high on-current for the n-type transistor further improves the low level.

With a complementary inverter a load line construction is far more complex than with an unipolar one. This is due to the fact, that both transistors change their regime during the inversion cycle. One would have to draw a saturation or linear load line for each region differently. At each regime transition it is hard to determine which equation would apply. On the whole the efforts outweigh the benefits, hence the load line construction of complementary inverters will not be discussed in this work.

1.2.4 Inverter dynamics

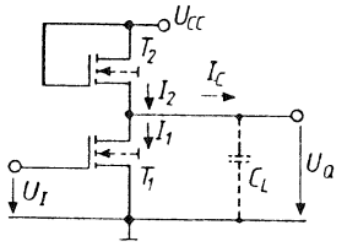
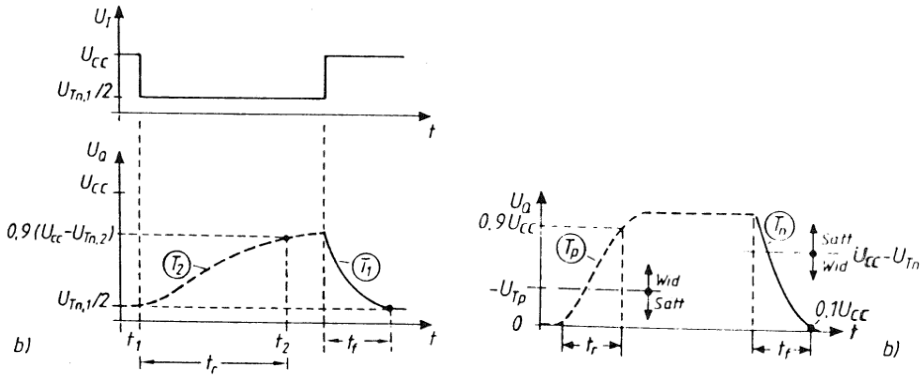


Figure 1.11: Equivalent circuit diagram of a dynamic unipolar inverter

Any capacitance in a circuit decreases its switching speed, because it needs to be charged and uncharged in every switching cycle. If these capacitances are not purposely put in the circuit, they are called parasitic capacitances. For an inverter they can be found in the single transistors as well as in the wiring. In the transistors the overlap of the source and drain contacts with the gate naturally result in a capacitance, but there is also a voltage dependent, nonlinear influence from the semiconductor and the gate [Hoffmann 93]. This combined with the nonlinear transistor characteristics makes accurate switching time calculations difficult. Yet by making some assumptions we are able to simplify the expressions and give a qualitative value for the switching times and its dependencies.

The assumptions made are:

- All capacitances are combined into a single inverter capacitance C_I, that is driven by the output voltage (figure 1.11)
- C_I is voltage independent
- The applied input voltage is a step function
- Wiring effects are not taken into account
- The off currents of the transistors can be neglected



(a) Unipolar inverter (b) Complementary inverter

Figure 1.12: Dynamic switching behavior of inverters[Hoffmann 93]

The current through the inverter capacitance is defined as:

$$I = C_I \frac{dV_O}{dt} \tag{1.29}$$

Through integration we can calculate the switching time:

$$t = \int_{t1}^{t2} dt = \frac{C_I}{I} \int_{V1}^{V2} V_O \, dV \tag{1.30}$$

Unipolar inverter

Again we use equation 1.17 to equal the currents. With the assumption that the off current of the switch can be neglected, the only current charging the capacitance C_I is the load current. On the other hand the only current discharging the capacitance is the current through the switch. For the rise time the load is always in saturation, leading to:

$$C_I \frac{dV_O}{dt} = \frac{\beta_L}{2} \left(V_{Sup} - V_O - |V_{TL}|\right)^2 \tag{1.31}$$

The integration limits were set to (figure 1.12(a)):

$$V_1 = \frac{|V_{TS}|}{2}$$
$$V_2 = 0.9 \cdot (V_{Sup} - |V_{TL}|)$$

This results in a rise time t_r of:

$$t_r = \frac{2C_I}{\beta_L} \cdot \left(\frac{1}{0.1 \left(V_{Sup} - |V_{TL}|\right)} - \frac{1}{V_{Sup} - |V_{TL}| - \frac{|V_{TS}|}{2}} \right) \tag{1.32}$$

During the fall the current of the switch changes, which also has to be taken into account. From $V_2 = V_{Sup}$ to $V_1 = V_{Sup} - |V_{TS}|$ the switch is in saturation:

$$C_I \frac{dV_O}{dt} = -\frac{\beta_S}{2} \left(V_{Sup} - |V_{TS}|\right)^2 \tag{1.33}$$

Then the switch is in the linear regime until the chosen lower limit of $V_1 = \frac{V_{TS}}{2}$ is reached:

$$C_I \frac{dV_O}{dt} = -\beta_S \left[\left(V_{Sup} - |V_{TS}|\right) V_O - \frac{V_O^2}{2} \right] \tag{1.34}$$

The final expression for the fall time is:

$$t_f = \frac{C_I}{\beta_S \left(V_{Sup} - |V_{TS}|\right)} \left[\frac{2|V_{TS}|}{\left(V_{Sup} - |V_{TS}|\right)} + ln\left(\frac{4V_{Sup}}{|V_{TS}|} - 5\right) \right] \tag{1.35}$$

Comparing the rise and the fall time shows that the rise time only consists of linear terms while the fall time has a logarithmic term as well. This means that the fall time is shorter than the rise time for an unipolar inverter.

Further details concerning the switching time calculation can be found in reference [Hoffmann 93].

Complementary Inverter

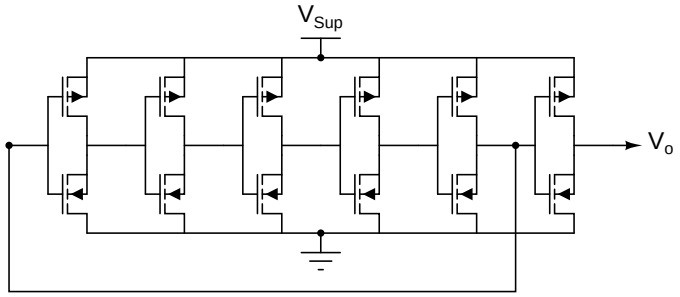
The calculations of the rise and fall times of the complementary inverter are similar to the unipolar one. The main difference is that for both the rise and the fall the calculations have to be separated between the linear and saturated regimes (figure 1.12(b)). The results are:

$$t_r = \frac{C_I}{\beta_p} \frac{1}{V_{Sup} - |V_{Tp}|} \left(\frac{-2V_{Tp}}{V_{Sup} - |V_{Tp}|} + ln \frac{1.9V_{Sup} - 2|V_{Tp}|}{0.1V_{Sup}} \right) \tag{1.36}$$

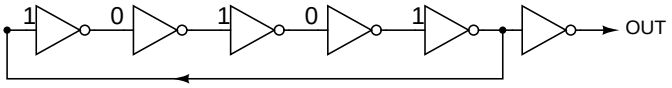
$$t_f = \frac{C_I}{\beta_n} \frac{1}{V_{Sup} - V_{Tn}} \left(\frac{2V_{Tn}}{V_{Sup} - V_{Tn}} + ln \frac{1.9V_{Sup} - 2V_{Tn}}{0.1V_{Sup}} \right) \tag{1.37}$$

Here both the rise and the fall time have a logarithmic term, hence they are equal if the threshold voltages und beta values are matched.

1.3 Organic ring oscillator



(a) Schematics using complementary inverters



(b) Schematics using logic gates

Figure 1.13: Schematics of a five stage ring oscillator with uncoupling stage

A ring oscillator is a device consisting of $2n + 1$ inverters, where $n \geq 1$. These so-called stages are connected in a chain, with the output of the last connected to the input of the first to close the ring (figure 1.13). It is often used as a proof of concept for new technologies since it is a rather simple design that requires a working dynamic switching behavior. It is also possible to measure the switching times of the inverters used in the oscillator (compare chapter 1.2.4).

Because of the odd number of NOT-gates any high or low input signal will start a switching chain reaction, with the last inverter switching the first. For ring oscillators even this initial input signal is not required. With supply voltage applied, thermal fluctuations provide the necessary signal voltages to start the oscillation. In an ideal device, where each inverter switches in an infinite short amount of time, an output signal measured at any point of the ring would result in a constant signal of $V_O = {}^{V_{Sup}}/_{2}$. Since all devices have a finite switching time, the signal measured will be an oscillation. The higher the gain of the inverters, the more rectangular the signal. The frequency measured for $2n + 1$ inverters will be:

$$f = \frac{1}{2t_i\,(2n+1)} \tag{1.38}$$

f $\cdots$ frequency of the ring oscillator
t_i $\cdots$ delay of a single gate

The frequency is easily influenced by parasitic capacitances, making further precautions necessary. To minimise the influence of the measurement, which is usually done using a tip prober, ring oscillators have at least one extra inverter not belonging to the ring. It uncouples the capacitance of the tip from the ring. Without this extra

inverter the measured frequency would be much lower and equation 1.38 would not apply.

2. Experimental

2.1 Source, drain and gate: Electron beam physical vapor deposition

Electron beam physical vapor deposition, or e-beam evaporation, is a kind of thermal evaporation where the required process temperature is reached by bombarding the source material with a focused electron beam. This allows for high temperatures in a defined area. The evaporated atoms reach the substrate with high kinetic energies, giving the possibility to not only adsorb at the target surface, but penetrate deeper into the underlying layer. Because of the high temperatures evaporation has to be done in vacuum. This also reduces interaction of the evaporated atoms along their path of flight. Evaporation is done in high or ultrahigh vacuum, starting at 10^{-5} mbar.

In this work all e-beam evaporation procedures are performed in a high-vacuum clustertool from Oerlikon Leybold Vacuum GmbH (figure 2.1).

Gate

For the gate electrode 80 nm of aluminum are applied to the substrate at a rate of $0.2 - 0.4$ nanometers per second. During the evaporation the substrate is rotated at 8 rotations per minute to ensure a homogeneous thickness of the Al layer. E-beam evaporation is our method of choice to provide a solid bond with the substrate.

Source and drain

The top electrodes are made from an 80 nm thick gold layer, again applied at a rate of $0.2 - 0.4$ nm/s. No rotation was applied to assure highly defined patterning

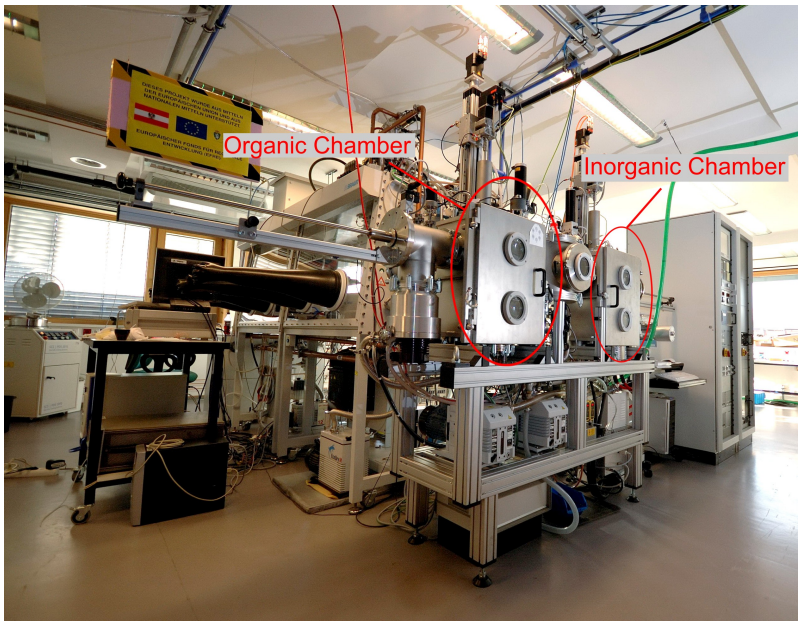


Figure 2.1: High-vacuum clustertool from Oerlikon Leybold Vacuum GmbH

through the shadow mask. Evaporated material scattered at shadow mask edges or insufficient mechanical contact (between mask and substrate) can cause inaccurate pattern transfer. Due to the penetration, the conduction at the gold-semiconductor interface is improved.

2.2 Nano composite dielectric layer

2.2.1 Metal oxide: Reactive sputtering

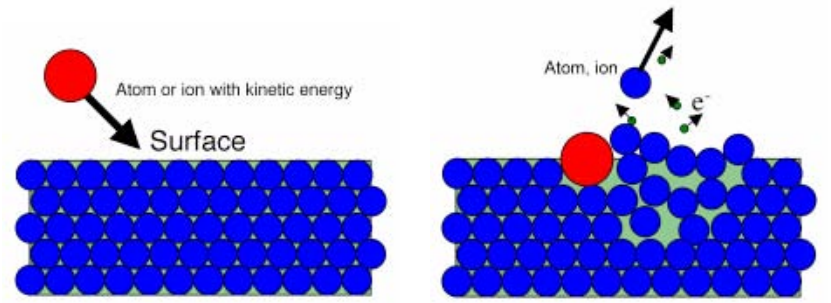


Figure 2.2: Schematics of the sputtering process [Gencoa 10]

Sputtering is a coating technique, where a target is bombarded by atoms, ions or molecules to eject surface atoms. Usually ions of an inert gas are used to minimize chemical interaction of the target material before adsorption at the substrate. By applying an electric field the sputtering gas is excited, forming a quasi-neutral plasma near the target (figure 2.3(c)). Through collisions with electrons the neutral gas atoms are ionized. The electric field accelerates these ions towards the target, where its material is physically ejected by collision cascades (figure 2.2). The sputtering rate is defined as:

$$\frac{dN}{Adt} = \gamma \frac{I}{e} \tag{2.1}$$

γ $\cdots$ sputter yield
I_{Ion} $\cdots$ ion current density
e $\cdots$ elemental charge

where

$$\gamma = \frac{sputtered\ atoms}{impact\ atoms} \tag{2.2}$$

According to equation 2.1 an easy way to increase the sputter rate is by increasing the ion current density, or more precisely by creating more ions within the plasma. This can be achieved by adding a magnetic field, forcing the electrons to remain longer in the plasma area, hence increasing the number of collisions. This technique is called magnetron sputtering (figure 2.3(a)). A side effect of the magnetic field is an inhomogeneous erosion of the target (figure 2.3(b)). Furthermore, instead of a constant one, an alternating electrical field is used. Its frequency is set high enough to make it impossible for ions with their high inertia to follow the changing field. The electrons are still able to oscillate, causing even more atom-electron collisions. By purposely adding a reaction gas, one can use the sputtering process to form for example oxidized layers. This method is called reactive sputtering.

(a) Magnetic field schematics during sputtering process

(b) Used aluminum target with typical inhomogeneous erosion

(c) Plasma during aluminum sputter process

Figure 2.3: Magnetron sputtering process [Haas 06]

The dielectric material used in this work is zirconium oxide (ZrO_2), which is built by sputtering zirconium in an oxygen reactive environment. Starting with a vacuum of 10^{-7} mbar, Argon (sputtering gas) and Oxygen (reaction gas) at a ratio of 10:4 are streamed into the chamber, up to a pressure of $5.8 \cdot 10^{-3}$ mbar. Under this condition a ZrO_2 layer of around 40 nm thickness is formed at a rate of 6 Å per minute.

2.2.2 Ultra-thin polymer: Spin-coating

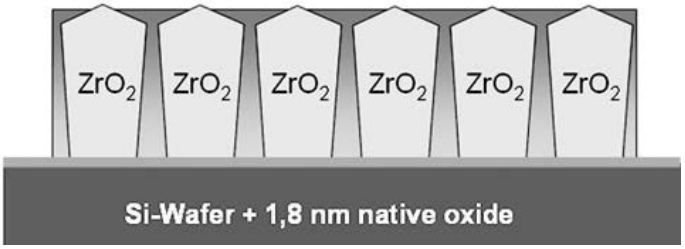


Figure 2.4: Island growth of ZrO_2 [Fian 08]

Figure 2.5: Laurell WS-650S-6NPP/Lite Spin-coater [Laurell 10]

An additional polymer layer is spin-coated on top of the ZrO_2 to improve the transistor performance. It acts as a smoothing layer, filling up the roughnesses occurring

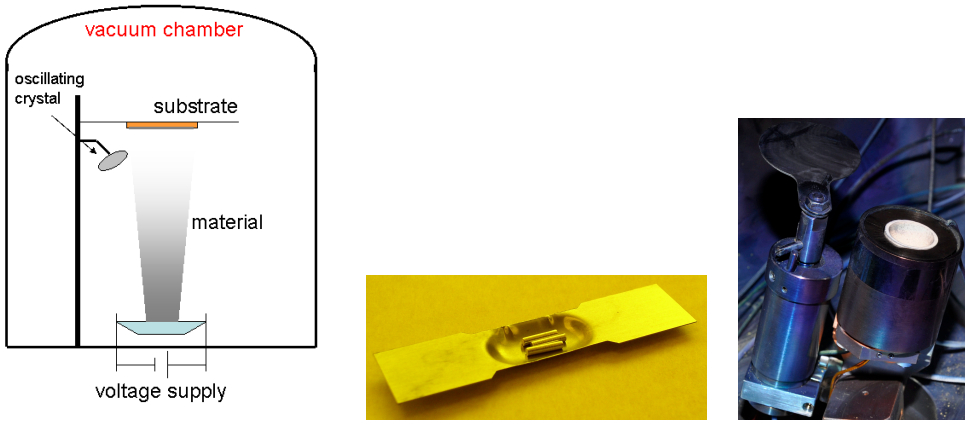
especially between the ZrO_2 islands (figure 2.4). This reduces the leakage currents and allows for low operation voltages [Fian 08, Jang 08].

Spin-coating is a common way of fabricating thin films from a liquid precursor. A small amount of resin is applied to the center of the substrate, which is afterwards rotated at 1000 to 6000 rpm. Due to the centrifugal forces, the liquid spreads to the edge of the substrate, leaving a thin film on the surface. Excess resin flows off the edges into the spin-coater. Homogeneity and film thickness depend on resin parameters like viscosity, surface tension or polarity as well as on spin-coating parameters like acceleration, rotational speed or spinning time.

Two different polymers are processed, poly(vinyl cinnamate) or PVCn [Jang 08] and poly(α-methylstyrene) or PαMS [Fian 08]. For the unipolar devices the smoothing layer is fabricated by spin-coating a solution of 0.2wt% of PVCn in chloroform at 2000 rpm for 30 seconds. Then it is UV-cross-linked for 60 minutes at a wavelength of $\lambda = 254\,nm$ in an Argon atmosphere. For the complementary devices better results were achieved using a solution of 0.5 wt% of PαMS with a chain length of 300000 in Toluene. It is spin-coated at 4000 rpm for 30 seconds and baked at 150 °C for 15 minutes on a hot plate.

All spin-coating processes in this work are performed using a Laurell WS-650S-6NPP/Lite Spin-coater (figure 2.5) in clean-room conditions.

2.3 Organic semiconductor thin films: Thermal evaporation



(a) Schematics of thermal evaporation (b) Evaporation boat (c) Evaporation cell

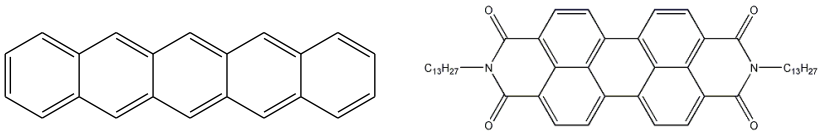
Figure 2.6: Details on thermal evaporation

Thermal evaporation is a physical vapor deposition performed in high vacuum. The mode of operation is almost identical to electron beam evaporation (section 2.1). The only difference is that the necessary temperatures are usually reached by resistive heating (figure 2.6(a)). The materials can be evaporated from boats or effusion cells (figure 2.6). Compared to sputtering or e-beaming the kinetic energy of the adsorbing atoms is much lower. This guarantees less deformation of the substrate and its underlying layers.

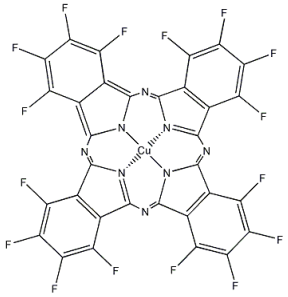
For this work all evaporation steps are done in a high-vacuum clustertool from Oerlikon Leybold Vacuum GmbH (figure 2.1). For all evaporated materials resistively heated effusion cells are used. The substrates can be heated using heat radiation. Heating the substrate allows for better diffusion of the adsorbed atoms resulting in a higher crystalline order and better charge carrier mobility [Jensen 99, Stadlober 06]. For a better layer homogeneity the substrates can also be rotated at up to 20 rpm.

Pentacene

Pentacene is one of the most used and studied organic p-type materials due to its superior field effect mobility compared to other organic p-type semiconductor [Dimitrakopoulos 02]. It consists of five benzene rings as shown in figure 2.7(a). Thermally evaporated in high vacuum it tends to crystallize in a herringbone structure (figure 2.8). This parallel arrangement of the molecules creates an overlap of the π-orbitals, making a charge carrier transport parallel to the substrate surface possible [Münch 01]. All p-type devices fabricated in this work use pentacene as active layer.



(a) Pentacene (b) PTCDI-$C_{13}H_{27}$



(c) $F_{16}CuPc$

Figure 2.7: Chemical structures of the semiconductors used in this work

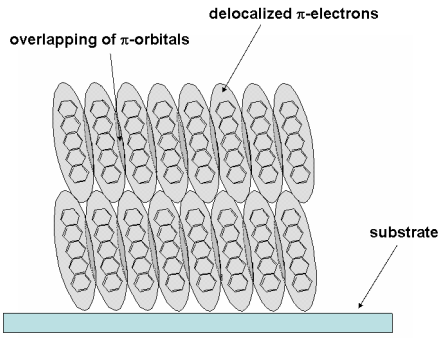


Figure 2.8: Pentacene herringbone structure and π-orbitals overlap [Münch 01]

The pentacene layer is fabricated in high vacuum (10^{-6} mbar) with the substrate held at 65 °C and rotated at 8 rpm. The deposition rate is increased during the process from 1 Å per minute for 5 nm over 3 Å per minute for the following 15 nm to 6 Å per minute until the final layer thickness of 30 - 50 nm is reached. This stepwise increasing of the rate results in good device performance at a reasonable processing time.

PTCDI-$C_{13}H_{27}$

PTCDI-$C_{13}H_{27}$ also has an extended π-electron system combined with a strong electron affinity [Horowitz 96, Tatemichi 06]. Due to this it is an n-type semiconductor allowing for high mobilities. Figure 2.7(b) shows its structural formula. A sufficient conductivity at the semiconductor-gold interface is only possible using the bottom gate, top source-drain configuration (figure 1.1(a)). To our best knowledge no detailed studies exist describing the charge carrier transport.

For layer fabrication the substrate was heated to 40 °C and rotated at 8 rpm, again under high vacuum conditions. During the evaporation process the rate was increased from 2 to 4 Å per minute.

$\mathbf{F_{16}CuPc}$

$F_{16}CuPc$ (figure 2.7(c)) is an n-type semiconductor well-known for being relatively stable when exposed to air and moisture [Bao 98]. It has about one to two orders lower mobility than PTCDI-$C_{13}H_{27}$, but can be used in both bottom and top source-drain configuration using gold as source-drain material (figure 1.1). It is used for all nanoimprinted n-type devices in this work (compare section 2.4).

It was processed at a substrate temperature of 80 °C while rotated at 8 rpm in high vacuum. Again the deposition rate was increased from 2 to 4 Å per minute to keep the processing times reasonable.

2.4 Device downscaling: Nanoimprint lithography

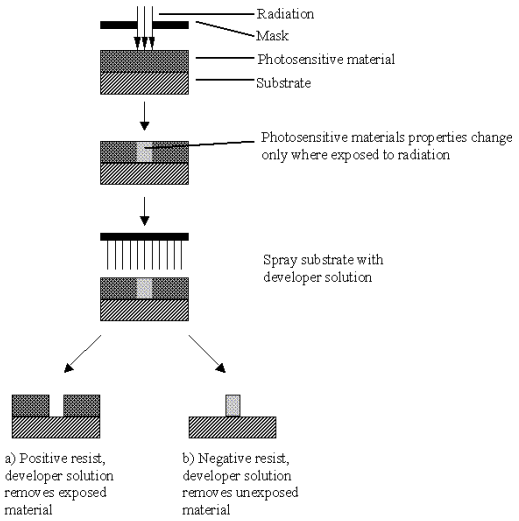


Figure 2.9: Schematics of the photolithography process [MEMSnet 10]

As the field of organic electronics matures, more complex circuits will have to be fabricated. Device packing density and especially switching frequency will play a key role in these processes. As already shown in equation 1.4 the frequency scales with the square of the channel length. This also approximately applies for the device packing density [Sze 81]. After proof of concept with relatively large devices of around 100 μm channel length, we challenge the task of fabricating transistors, inverters and ring oscillators with a channel length in the sub-micron regime.

There are a lot of structuring techniques with resolutions in the nanometer range. Common examples are e-beam lithography (EBL), focused ion beam lithography (FIB) or extreme ultraviolet lithography (EUV). All these methods share the disadvantages of being serial, very expensive and far from compatible with inline or reel-to-reel processes. Since cheap and large area fabrication are the main reason for organic electronics, a more convenient structuring method has to be used.

To fabricate submicron source-drain structures for organic electronics, the nanoimprint lithography (NIL) technique is used. This technique uses high resolution structure transfer from a hard or soft stamp onto the sample. There are different ways how this structure transfer is realized, in our case the hot embossing method is used. Figure 2.12 shows the schematics of this method. In detail the following fabrication steps are necessary to fabricate a NIL-OTFT:

Gate

The gate consists again of 80 nm of aluminum. Since shadow masking cannot provide the required resolution, the chosen technique is photolithography (figure 2.9).

In this widely used technique a resist sensitive to ultraviolet light is spin-coated on a pre-cleaned substrate. Then the sample is exposed to UV light through a mask containing the targeted structures. Depending if the resist is a positive or a negative one, the exposed areas become soluble or insoluble during development. The developer removes all unwanted resist. Aluminum is deposited on the whole sample. Finally the cured resist is chemically dissolved in a liftoff step, removing all excess metal as well.

Dielectric layer

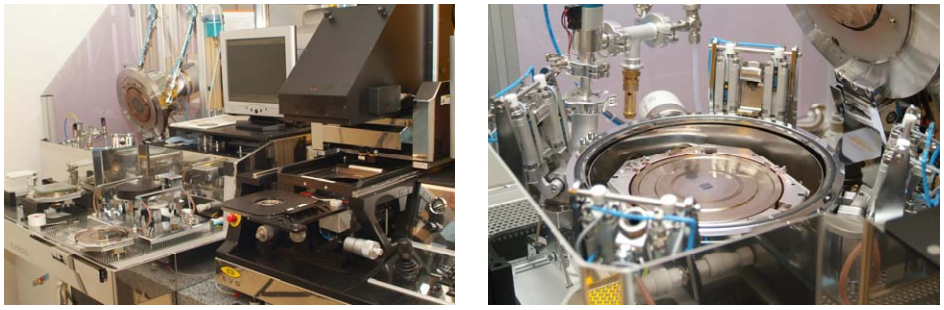
Different from the shadowmasked samples described in chapter 2.2 the dielectric material used for the imprinted devices is a benzocyclobutene (BCB) derivative [Chua 04]. ZrO_2 with a PVCn smoothing layer would also be possible, but due to the lower yield of the imprinted devices a dielectric with an easier and faster fabrication is advantageous. An approximately 100 nm thick layer of BCB is fabricated by spin-coating a solution of 1:3 BCB in 1,3,5-trimethylbenzene (mesitylene) at 2000 rpm for 30 seconds. On a hotplate it is baked at a temperature of 290 °C for 1 minute.

Source and drain

As the name "nanoimprint lithography" (NIL) implies, a stamp is pressed into a resist to ultimately structure the sample. Typically this resist is spin-coated onto the sample (figure 2.12(c)). During the NIL process the whole sample is heated well above the glass transition temperature of the resist. The stamp is pressed into the hot resist with a defined force (figure 2.12(d)). After being cooled down, the stamp is released from the sample, with the pattern transferred to the resist (figure 2.12(e)). A thin resist layer is left in the patterned area, which is removed by an etching step (figure 2.12(f)). Finally the source/drain material is applied and the excess resist is removed, leaving the structures on the sample (figures 2.12(g) and 2.12(h)).

All imprinting steps in this work are done using an EVG 520 imprinting tool and an EVG 620 mask aligner (figures 2.10(a) and 2.10(b)). After the alignment the sample is held in place by mechanical clamps and the whole stamp-sample system is transferred to the imprinting tool.

The imprint resist we use is mr-I 7030E from microresist dissolved in 1-methoxy-2-propyl-acetate (PGMEA). It is spin-coated at 4000 rpm for 30 seconds and baked at 140 °C for 3 minutes on a hot plate. The layer thickness is around 400 nm. Prior to the imprint the stamp is coated with an anti-sticking layer consisting of 1 mmol perfluoroctyl-trichlorosilane (F6) dissolved in isooctane. This coating has to be done under inert atmosphere to avoid bulk polymerization of the trichlorosilane.



(a) EVG 620 mask aligner (front) and EVG 520 imprinting tool (back)

(b) Detailed view of the EVG 520 imprinting tool

Figure 2.10: Imprinting tools used in this work

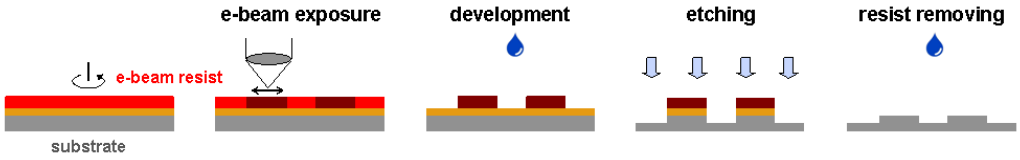


Figure 2.11: Stamp fabrication by e-beam lithography [Haas 06]

The stamp is dipped in the solution for 10 minutes and then rinsed in pure isooctane. Finally the stamp is treated with isopropanol and dried with N_2. This prevents the imprint resist from sticking to the stamp during its removal.

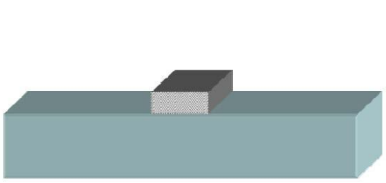
For the imprint the substrate and the stamp are heated to 125 °C. The the stamp is pushed into the sample with a force of 1000 N. After cooling the system down to 60 °C the stamp is removed. A 35 nm thick gold layer is thermally evaporated onto the sample. Then the resist and the excess gold are lifted off using PGMEA.

Stamp fabrication can be done by any of the structuring techniques mentioned in this chapter's introduction. In our case it is performed using e-beam lithography. Since the stamp is used for imprinting a resist material followed by a lift-off procedure, the structures have to be countersunk into the unstructured background. Therefore a negative e-beam resist is recommended since the writing of the contact structures is less time consuming than defining the whole background [Haas 06]. Figure 2.11 gives an overview of the stamp fabrication process.

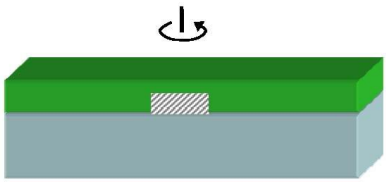
Semiconductor

The semiconductors are processed as described in chapter 2.3. They are applied on top of the source and drain electrodes (figure 2.12(i)), making the nanoimprinted transistor a bottom gate, bottom source-drain configuration (compare figure 1.1). In a top source-drain approach the crystal structure of organic semiconductors would be destroyed by the chemicals used in the NIL process. It is stressed again, that

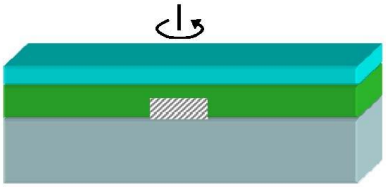
PTCDI-$C_{13}H_{27}$ is not forming a conductive interface atop the gold contacts, hence being replaced by F_{16}CuPc (see also chapter 2.3).



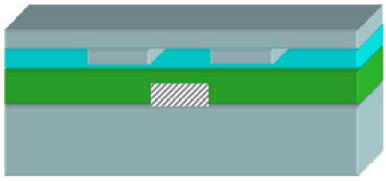
(a) Gate structured by photolithography



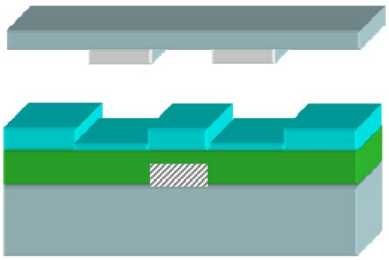
(b) Dielectric layer is applied



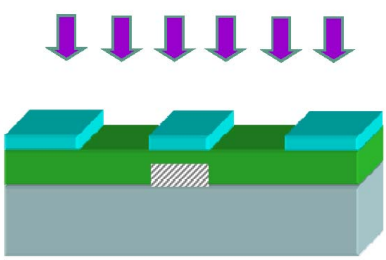
(c) Imprint resist is applied



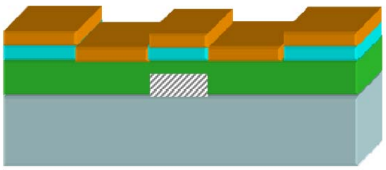
(d) The stamp is pressed into the heated resist



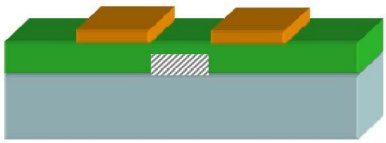
(e) The stamp is removed after cooling the resist



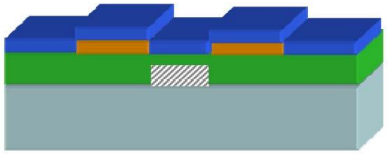
(f) Residual resist is removed by oxygen plasma etching



(g) Source-drain material is applied



(h) The remaining resist is removed in a lift-off process

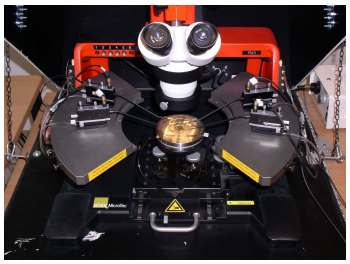


(i) Semiconductor is applied

Figure 2.12: Schematics of the transistor fabrication by means of nanoimprint lithography

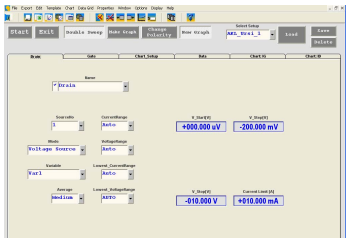
2.5 Electrical measurements

(a) Hioki 3532-50 LCR-meter



(b) Probe station with Suess Microtec probers

(c) MB parameter analyzer



(d) MB parameter analyzer operating software

Figure 2.13: Electrical measurement instruments [Haas 06]

To calculate the mobility of the devices, it is necessary to measure the impedance of the dielectric (equation 1.3). For this purpose thin film capacitors of ZrO_2/PVCn and ZrO_2/PαMS are fabricated (see chapter 2.2). The measurements are done using a Hioki 3532-50 LCR-meter, contacted on a probe station using probers from Suess Microtec (figures 2.13(a) and 2.13(b)).

For the characterization of the transistors, inverters and ring oscillators the samples are again contacted using the probers from Suess Microtec. The measurements are performed with a parameter analyzer from MB Technologies, housing four source measurement units (SMU), and a corresponding operating software (figures 2.13(c) and 2.13(d)). All measurements in this work are done under ambient conditions.

3. Results and Discussion

3.1 Organic transistors

This section will present the results of p-type and n-type transistors on a glass substrate fabricated by shadow masking. As a polymeric smoothing layer for both transistors PαMS is used. This is due to the fact, that no working n-type transistors were fabricated with a PVCn - PTCDI-$C_{13}H_{27}$ combination.

3.1.1 p-type transistors

Figure 3.1 shows the electrical measurements of a typical pentacene transistor. The output characteristics shows a linear as well as a saturated regime, as can also be found in theory. Very small hysteresis effects can be observed. Hysteresis happens due to charges (in case of a p-type ions, for an n-type electrons) from the ambiance being trapped at the transistor surface. When a voltage between source and drain is applied, these charges have to be moved to the respective electrode. This leads to different results when sweeping in different directions. For a transistor this behaviour is unwanted, as it results for example in an unstable current level for a certain gate voltage. Since the devices were measured in atmosphere, the trapped charges come most likely from the humidity.

The transfer and the subthreshold characteristics also reveal good switching behavior, although a small source drain leaking current at higher gate voltages can be observed. This leaking current has multiple origins. With higher voltages between gate and drain, the electric field "pulling" the charge carriers to the drain is increased. This results in a source drain current, even though the device is supposed to be off. This effect is observed best in the subthreshold characteristics (figure 3.1(c)). At $V_G = +2\,V$ the electric field of the drain is at maximum, and so is the current. This

field gets dampened with increased gate voltage (compare the pinch-off effect in chapter 1.1.1) reducing the current to a minimum value shortly before the transistor is switched on. This effect is also increased by higher mobilities, allowing for easier charge carrier movement. Also atmospheric trapped charges can contribute to the leaking.

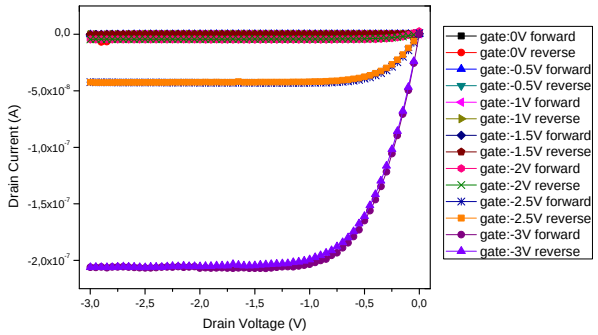
The transistor has on- and off-currents of $I_{on} = -2 \cdot 10^{-7}\,A$ and $I_{off} = -5 \cdot 10^{-10}\,A$ at -3 V drain and gate voltage. The threshold voltage is $V_T = -2.1\,V$ and the maximum mobility reveals $\mu = 0.5\,cm^2/Vs$. The mobility is reasonable, though mobilities of up to $\mu = 2\,cm^2/Vs$ have been reported [Dimitrakopoulos 02].

The gate leaking current is 1.5% of I_D, which is small, but not negligible. Gate leakage is generally indirectly proportional to the dielectric thickness. The thinner the dielectric layer, the smaller its resistance. If its resistance is in the same regime as the semiconductor, the transistor acts as a current divider, letting part of the current flow from source to gate instead of from source to drain. This effect is increased by surface roughnesses, holes or cracks in the dielectric layer. During the fabrication these are filled with semiconductor and/or electrode material further reducing the dielectric thickness. Still it is necessary to fabricate thin dielectric layers in order to keep the driving voltages of the transistor low. With higher moblities the gate leaking currents are reduced, as the semiconductor's resistance is decreased.

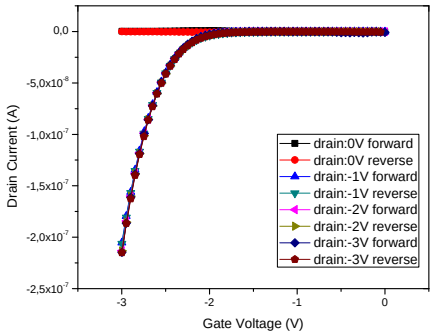
3.1.2 n-type transistors

To be able to fabricate complementary circuits, n-type transistors also have to be produced. With better complementary inverter performance and drain current matching in mind, the transistors are fabricated with a ten times larger channel length than the pentacene devices (for further explanations see chapter 3.2.2). Representative characteristics we depicted in figure 3.2. The transistor shows a good saturation regime, but looking at the output characteristics the linear regime is not linear at all. This is due to the contact resistance between the semiconductor and the gold contacts [Palfinger 09]. Unlike stated in the simple band model of chapter 1.1.2, it is difficult to completely equal the Fermi level of the electrodes with the HOMO or LUMO (p-type or n-type) level of the semiconductor. This results in a barrier, that the charge carriers have to overcome in order to move from the electrode to the semiconductor or vice versa. This effect is negligible for high drain voltages, the saturated regime is hardly effected. But for low voltages the ohmic behavior is influenced, resulting in the observed curvature of the linear regime.

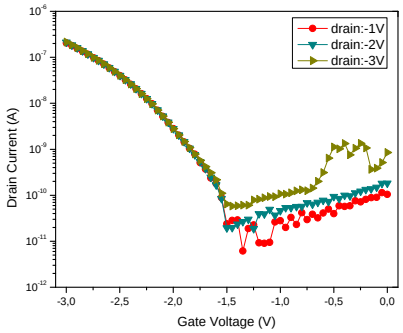
The transistor has a maximum hysteresis of $1 \cdot 10^{-9}\,A$, which is acceptable. A possible reason why it is higher than for the p-type transistor could be that the PTCDI-$C_{13}H_{27}$ is trapping more electrons than the pentacene traps holes.



(a) Output characteristics

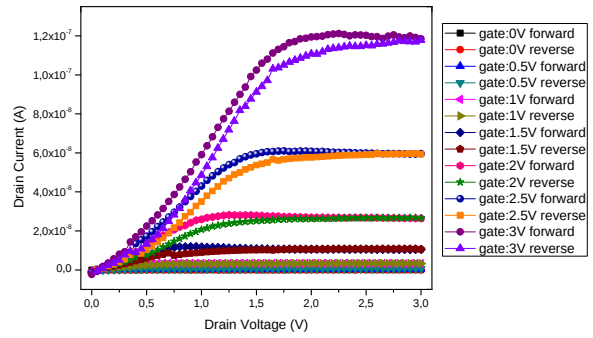


(b) Transfer characteristics

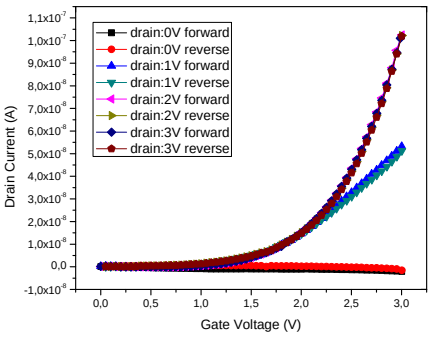


(c) Subthreshold characteristics

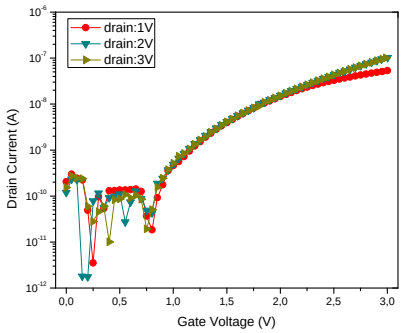
Figure 3.1: Electrical measurement results of a p-type transistor



(a) Output characteristics



(b) Transfer characteristics



(c) Subthreshold characteristics

Figure 3.2: Electrical measurement results of an n-type transistor

The transistor currents are $I_{on} = 1.2 \cdot 10^{-7}\,A$ and $I_{off} = 1 \cdot 10^{-11}\,A$. The maximum mobility is $\mu = 0.04\,cm^2/Vs$ and the threshold voltage is $V_T = 1.6\,V$. The gate leaking current is 4,2% of I_D, which is reasonable, taking the lower n-type mobility into account.

Since the linear regime of a transistor is not a crucial parameter for a well-performing inverter, no further attempts to decrease the contact resistance were done in this work (compare chapter 1.2.3).

3.2 Organic inverters

3.2.1 p-type inverters

For the first efforts in fabricating an inverter a unipolar design was used. Here only one type of semiconductor is necessary. Since the best transistor results were achieved using pentacene, our inverter consists of two pentacene transistors, the switch and the load. As equation 1.14 states, the gain of the inverter increases with the beta-ratio of the transistors. The load and the switch are processed simultaneously, so the mobility as well as the specific capacitance are equal. In order to achieve a high gain inverter, it is necessary to adjust the geometry of the inverters.

Since the resolution of the shadow masking technique is limited, we decided not to change the channel lengths, but the widths. For the load, that should be as small as possible, the width is a compromise between gain and source drain current (compar equations 1.1 and 1.2). To still get reasonable currents the width of the load is 1 mm. The switch should have a channel width as high as possible. Here the limitations are not given by the device performance, but by fabrication. With our high-vacuum clustertool we are able to process samples the size of a glass slide (26 x 76 mm), and ultimately we want a ring oscillator to fit it. This will need at least 6 inverters in a row. So taking wiring space into account, we are able to make the load 10 mm long.

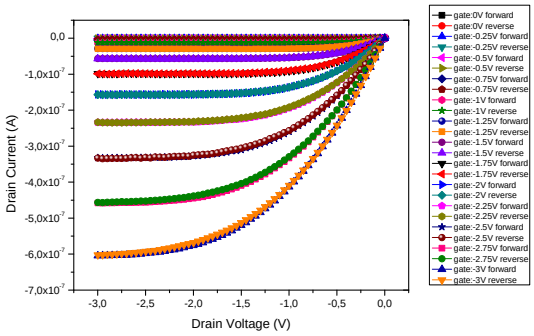
The dielectric used is ZrO_2 with a PVCn smoothing layer, as all transistors have pentacene as their semiconductor. Also for later fabrication of nanoimprinted devices it is necessary to find alternatives to PαMS. The reason for this is that PαMS is dissolved in 1-methoxy-2-propyl-acetate (PGMEA), which is necessary for the NIL process (see chapter 2.4).

The electrical measurements of the load and the switch can be found in figures 3.3 and 3.4 respectively.

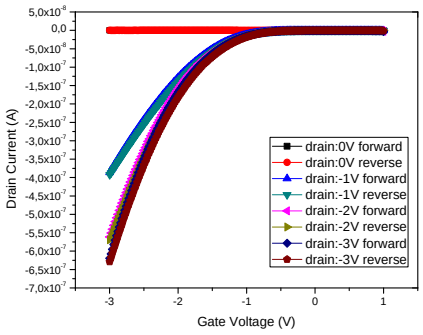
Load

The output characteristics show good linear as well as saturated behavior of the transistor. Observed hysteresis is negligible. The on- and off-currents are $I_{on} = -6.6 \cdot 10^{-7}\,A$ and $I_{off} = -7.6 \cdot 10^{-10}\,A$, resulting in a good on/off ratio. The threshold voltage is $V_T = -0.85\,V$ and the maximum mobility reveals $\mu = 0.3\,cm^2/Vs$. Again these are quite good values compared to literature.

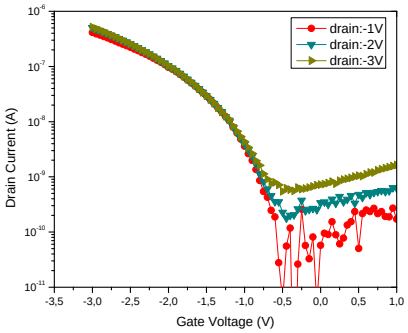
The gate leaking current is 0.3 % of I_D, but has a rather big hysteresis, reaching well into the positive regime (figure 3.3(d)). This may indicate, that the PVCn might also act as a charge trap when exposed to air and humidity. Since the leaking current is rather small compared to the drain current, this seems not to affect the transistor's behavior greatly.



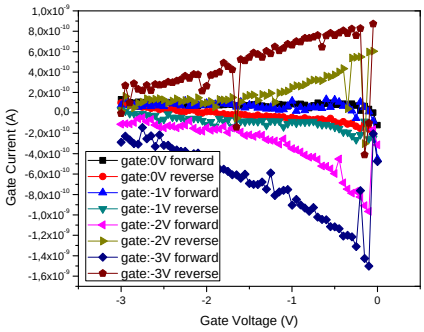
(a) Output characteristics



(b) Transfer characteristics

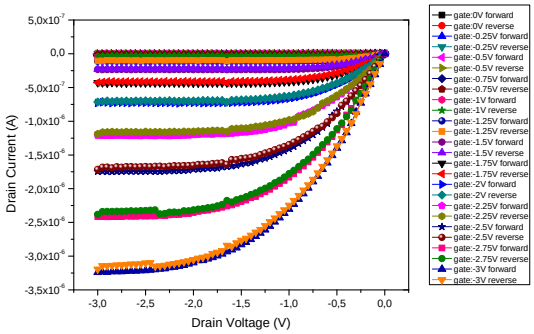


(c) Subthreshold characteristics

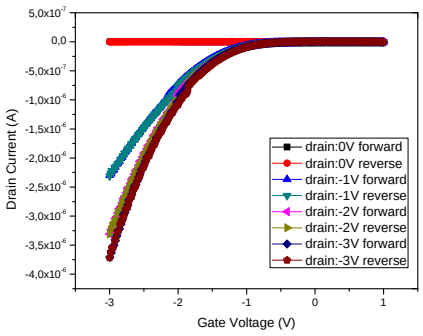


(d) Gate current vs gate voltage

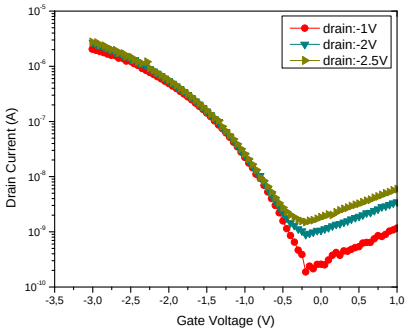
Figure 3.3: Unipolar inverter: electrical measurement results of the load



(a) Output characteristics



(b) Transfer characteristics



(c) Subthreshold characteristics

Figure 3.4: Unipolar inverter: electrical measurement results of the switch

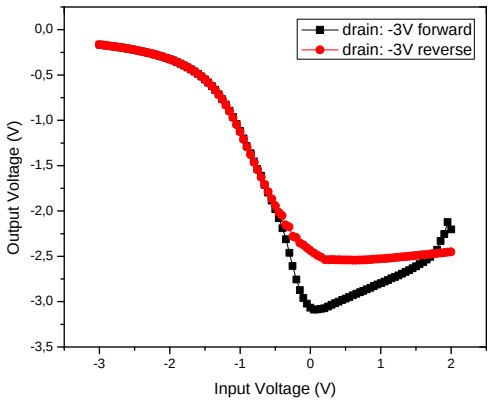


Figure 3.5: Electrical measurement results of the unipolar inverter

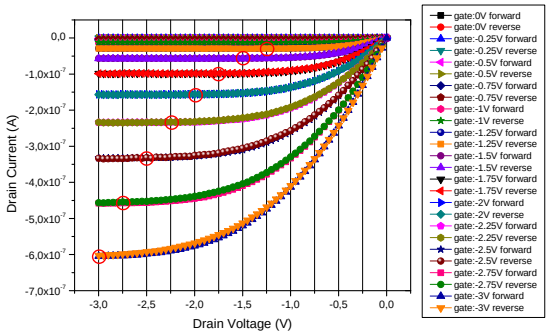
Switch

The transistor shows good regimes, hysteresis is higher than with the load, but still negligible. The currents measured are $I_{on} = -3.2 \cdot 10^{-6}\,A$ and $I_{off} = 3.1 \cdot 10^{-9}\,A$. The reason for the higher on- and off-currents compared to the load is the one order of magnitude greater channel width. The mobility calculation compensate this difference, showing a similar value of $\mu = 0.27\,cm^2/Vs$. The gate leaking current is also quite similar to the load, revealing 0.2 % of I_D and a hysteresis well into the positive regime. This shows, that the dielectric layer has indeed homogeneous electric properties over the sample. Finally the threshold voltage is comparable with the load, revealing $V_T = -0.9\,V$.

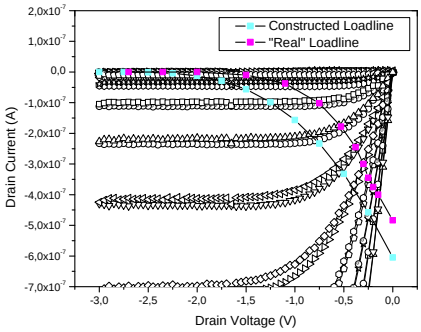
Inverter

As a final step the inverter transfer characteristics was measured (figure 3.5). A low level of -0.16 V and a high level of -2.8 V is reached, but what can be clearly seen is the large hysteresis of 0.6 V around the high level. Since the high level lies in the positive regime, this hysteresis indicates trapped charges from the environment are present in the transistor, even resulting in slightly higher output than supply voltages shortly before the threshold voltage of the switch is reached. This seems rather strange, since both single transistors did not show such significant hysteresis. However, a closer look at the loadline construction shows that at the high level the loadline's slope is very low, so even a small hysteresis can result in large high level shifts. Inserting the transistor's values into equation 1.14 reveals a theoretical gain of:

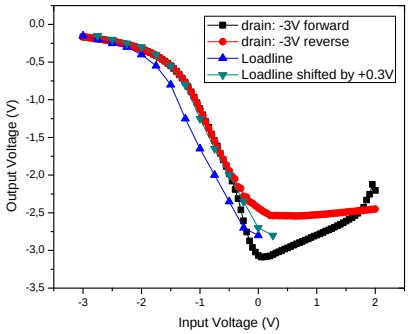
$$\sqrt{\frac{\beta_S}{\beta_L}} = \sqrt{\frac{10 \cdot 0.27\,cm^2/Vs}{0.3\,cm^2/Vs}} = 3.0 \tag{3.1}$$



(a) Output characteristics of the load with the loadline construction points



(b) Output characteristics of the switch with the loadline



(c) Constructed and real inverter transfer characteristics

Figure 3.6: Construction of the inverter transfer characteristics

It was expected to reach lower values in the experiment, as no parasitic effects whatsoever are included in the calculation. The theory is still quite far away from the experiment, which reveals a gain of 1.7. This corresponds to an error of 76.5 %. It needs to be stressed that the amount of fabricated devices is far to low for any statistic, meaning the big error is definitely not falsifying the theory. Also, as the goals of this work are proof-of-concept devices and not confirming theories, no further investigations in that direction are performed.

In a next step we want to verify the usability of the load line construction on our inverter sample. Because of the rather big difference between theory and experiment for the gain, the load line was not calculated from equation 1.15, but taken directly from the load's experimental data. This way, the result should be exactly the same as the experimental inverter transfer characteristics. This experimental load line can be constructed by simply reading the current values at points of equal drain and gate voltages from the ouput characteristics (figure 3.6(a)). The load line was drawn into the output characteristics of the switch to acquire the constructed transfer curve (figures 3.6(b) and 3.6(c)).

The constructed inverter characteristics shows a gain of 1.8. This can be treated as equal to the experiment, taking the fewer measurement points and the error of graphical extraction into account. Still there is a big difference in the shifting point as the whole curve is shifted by 0.3 V to the negative regime (figure 3.6(c)). Reverse engineering the load line from the experimental transistor curve shows that the load's source-drain current should be up to $2 \cdot 10^{-7}\,V$ lower than measured (figure 3.6(b)). Also the curvature is not equal to the measured load line, indicating that also the currents of the switch must have changed. An explanation might be that between the single device measurements and the inverter measurements the performance of both transistors changes, since they are exposed to air, moisture and UV light. This behavior was observed with a number of devices, making it a plausible reason for the shift in the inverter characteristics.

Overall the unipolar inverters presented in this work are not very promising. Their gain is to low to be used as a logic device, needing even positive input voltages to reach the high level. To fabricate better performing devices, we challenged the task of complementary organic electronics.

3.2.2 Complementary inverters

With the good performing transistors shown in chapter 3.1 a complementary inverter is realized. For the inverter to be symmetrical, the beta-ratio of both transistors should be ${}^{\beta_p}/_{\beta_n} = 1$ (equation 1.19). Since the mobility of PTCDI-$C_{13}H_{27}$ is roughly an order of magnitude lower than that of pentacene, the n-type transistor was designed with a 10 times larger channel width than the p-type. For the same reason as for the unipolar inverters (maximum sample size for a ring oscillator) the width of the p-type transistor is 1 mm while the n-type is 10 mm wide.

The smoothing layer of the dielectric system had to be changed in order for the n-type transistors to work. PVCn does not support the crystallinity of PTCDI-$C_{13}H_{27}$ in a satisfactory manner (compare chapter 3.1).

The complementary inverter's transfer characteristics can be found in figure 3.11. At a supply voltage of 3 V the realized high level is $V_{OH} = 3\,V$, as predicted by theory. The low level of $V_{OL} = 30\,mV$ at $V_I = 3\,V$ is higher than the theoretical 0 V. The reason is the one order of magnitude higher off-current of the p-type transistor, showing that low off currents are crucial in complementary electronics. The fact of having the low level minimum of only $V_{OL} = 3\,mV$ at $V_I = 1.6\,V$ corresponds to the observed increase of the p-type transistors off-current with higher gate voltages (figures 3.8).

The inverter reveals a gain of 55, which is a very good value taking the low supply voltage of only 3 V into account. This also shows the huge advantage of comple-

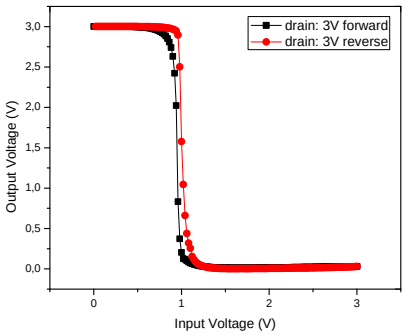


Figure 3.7: Electrical measurements of the complementary inverter

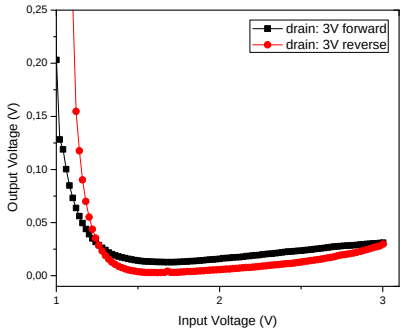


Figure 3.8: Zoom on the low level of the complementary inverter

mentary electronics in terms of device packing density. To only theoretically achieve such a high gain with our unipolar design, the switch needs to be almost 200 mm long, spreading over three glass slides.

As expected we were not able to achieve a symmetrical inverter with the 1:10 ratio of the transistor channel widths. Firstly the mobilities are slightly different for each device and secondly the devices have a threshold voltage difference of $\Delta V_T = 0.5\,V$. The inverter's threshold voltage is $V_{Ti} = 0.97\,V$. Inserting the experimental mobilities and threshold voltages into equation 1.19) should lead to a similar value. The theoretical inverter threshold calculates to:

$$V_{Ti} = \frac{1,6\,V + \sqrt{\frac{0.5\,cm^2/Vs}{0.4\,cm^2/Vs}}\,(3\,V - 2.1\,V)}{1 + \frac{0.5\,cm^2/Vs}{0.4\,cm^2/Vs}} = 1.16\,V \tag{3.2}$$

The theoretical error is 19.6 %, which seems to be reasonable, since the theory does not take off-currents or parasitic effects into account.

We will investigate, how suitable theory predictions are concerning the noise margins. The experimental V_{IL} and V_{IH} values were extracted by averaging the forward and reverse measurement of the points with a slope of -1. The experiment reveals:

- $V_{ILexperiment} = 0.87\,V$ at $V_O = 2.91\,V$
- $V_{IHexperiment} = 1.10\,V$ at $V_O = 0.11\,V$

We use the same output voltages in equations 1.22 and 1.25. Again the specific capacitance is treated equal over the sample. The calculations show:

$$V_{IL} = \frac{2 \cdot 2.91\,V + \frac{10 \cdot 0.04\,cm^2/Vs}{0.5\,cm^2/Vs} \cdot 1.6\,V - 3\,V - 2.1\,V}{1 + \frac{10 \cdot 0.04\,cm^2/Vs}{0.5\,cm^2/Vs}} = 1.105\,V \tag{3.3}$$

$$V_{IH} = \frac{2 \cdot 0.11\,V + 1.6\,V + \frac{0.5\,cm^2/Vs}{10 \cdot 0.04\,cm^2/Vs}(3\,V - 2.1\,V)}{1 + \frac{0.5\,cm^2/Vs}{10 \cdot 0.04\,cm^2/Vs}} = 1.305\,V \tag{3.4}$$

The theory is 27.0 % and 18.6 % off for V_{IL} and V_{IH} respectively. This seems reasonable for the same reasons as with the gain. Furthermore we want to know, if theory can predict the shape of the inverter curve correctly. The theoretical inverter threshold voltage was off by $\Delta V_{Ti} = 0.19\,V$; if the shape of the theoretical inverter curve is correct, the noise margins should be shifted by the same value. Considering this, the theory reveals:

$$V_{ILcorrected} = V_{IL} - \Delta V_{Ti} = 0.915\,V$$
$$V_{IHcorrected} = V_{IH} - \Delta V_{Ti} = 1.115\,V$$

Now the errors are reduced to 4.6 % for V_{IL} and 1.8 % for V_{IH}. This indicates that the off-currents and parasitic effects influence the shifting point of the inverter more than they influence the curvature.

Overall the results look very promising, the inverter can definitely be used as a logic gate. Although it is not symmetrical, still both the high and the low level are in the positive regime and well within the input voltage range of $0 - 3\,V$.

3.3 Organic ring oscillators

The final goal of this work is to present a ring oscillator, demonstrating the dynamic switching capabilities of inverters. From the frequency of the oscillation it is also possible to determine the average switching time of the inverters in the circuit. Theoretically three inverters are sufficient for oscillation, but practically at least a fourth "uncoupling stage" is needed, to prevent influences of the measurement on the oscillation. Typically these influences would be capacitances from the metal prober, reducing the oscillation frequency. At the end of each circle the signal from the last inverter is taken to both the first and the uncoupling inverter (see figure 1.13).

Since the ring oscillator is averaging it's frequency over all stages, the more inverters used, the better the result represents the capability of the devices (compare equation 1.38). The number of used inverters is limited by technical considerations. On the one hand as already stated in chapter 3.2, our sample size is limited to the size of a glass slide. On the other hand, as the fabrication is still highly experimental and the organic semiconductors functionality is not fully understood, yield is an important issue. A working ring oscillator is only achievable, if all transistors work and show sufficiently good parameters to allow for good inverter characteristics. It is crucial that the high and low levels are both well established within the input voltage range of $0\,\mathrm{V} - \mathrm{V_{Sup}}$, to prevent undefined logic states at the inverters output. We decided to design a five stage ring oscillator with a sixth inverter as uncoupling stage.

3.3.1 p-type ring oscillators

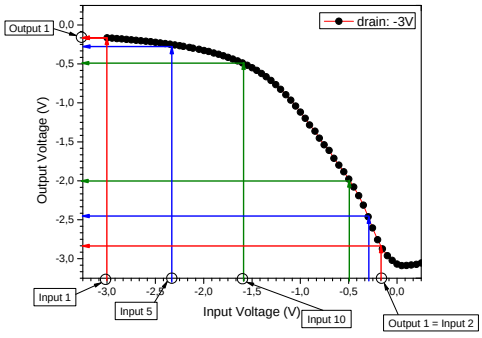


Figure 3.9: Signal dampening of the unipolar inverter

With the devices from chapter 3.2.1 ring oscillators are fabricated and measured. Unfortunately despite various efforts no oscillation could be observed, the measured signal was constant at $\mathrm{V_{Sup}}/2$. After checking whether all transistors are working we realized that the problem had to come from the inverter's performance. Due to the low gain, the high and low levels of the inverters are not fully established within the input voltage range. This firstly leads to logically undefined inverter output levels

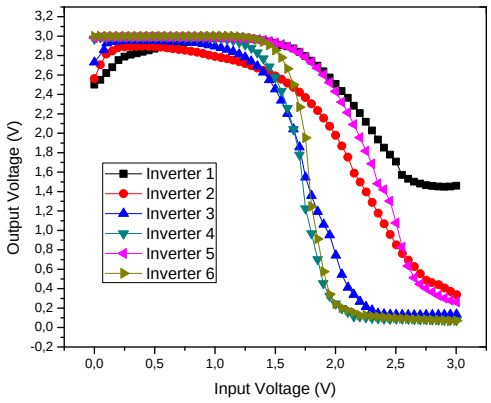


Figure 3.10: Inverter transfer characteristics of all inverters in a ring oscillator

and ultimately to a constant signal of $V_{Sup}/2$. Figure 3.9 demonstrates the signal dampening through the ring oscillator. Presuming that the high level input at the first stage is V_{Sup} and all inverters are identical, it can be shown that after only 10 stages (or 2 rounds through the ring oscillator) the difference between the high and low level has decreased from $\Delta V_{high/low} = 2.8\,V$ to $\Delta V_{high/low} = 1.5\,V$.

Rather than trying to improve the unipolar inverters, we decided to fabricate ring oscillators from the much better performing complementary inverters.

3.3.2 Complementary ring oscillators

Chapter 3.2.2 showed inverters performing well enough, that a working ring oscillator should be achievable. The gain is high enough to prevent the dampening effect from the p-type oscillators.

Again we are not able to report a working oscillation. As stated above, the inverter characteristics are good enough to allow for a working ring oscillator. Thorough measurements reveal that the yield of the transistors is simply not high enough in terms of comparable device performance (figure 3.10). The transistors are either short circuited or show weak mobilities due to bad semiconductor growth. This results in big current differences between the transistors, leading to strongly shifted inverter thresholds, low gain. In some cases also a high hysteresis can be observed, indicating that exposure to ambient conditions is effecting circuits with a lot of transistors more than single devices or inverters are influenced.

Further investigation of this issues is necessary and needs to be performed in the future in order to achieve a working ring oscillator. Also the electrical measurement should be performed under inert conditions.

3.4 Nanoimprint lithography

3.4.1 Inverters

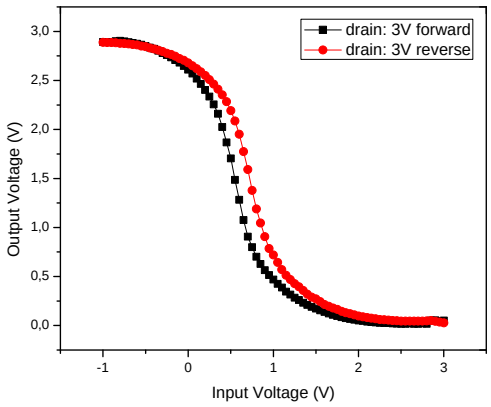


Figure 3.11: Electrical measurements of the complementary NIL inverter

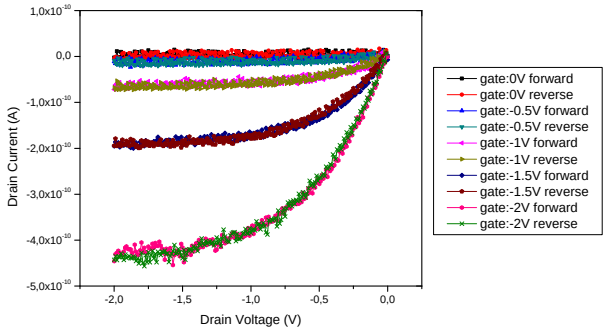
Using the nanoimprint lithography we were able to fabricate a first p-type as well as n-type transistor with the characteristics shown in figures 3.12 and 3.13. Both have a channel length of L = 900nm, while their widths were again used for mobility compensation, being $W_p = 10\,\mu m$ and $W_n = 100\,\mu m$. The substrate used is a polyimide foil which resists the temperatures necessary for the fabrication of the BCB dielectric layer.

The mobilities reveal $\mu_p = 0.002\,cm^2/Vs$ and $\mu_n = 0.004\,cm^2/Vs$, which results in very low currents of $I_{on} = 4.4 \cdot 10^{-10}\,A$ and $I_{off} = 2.95 \cdot 10^{-12}\,A$ for the p-type and $I_{on} = 2.15 \cdot 10^{-9}\,A$ and $I_{off} = 2.23 \cdot 10^{-10}\,A$ for the n-type.

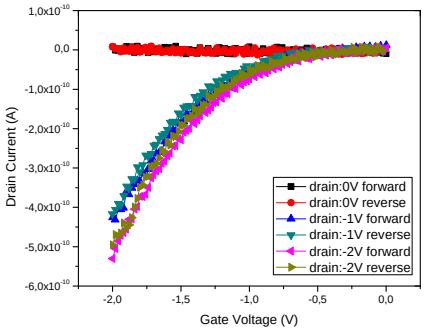
With this two transistors also a complementary inverter is measured, revealing the transfer characteristics of figure 3.11. The low level is $V_{OL} = 20\,mV$ at $V_I = 3\,V$, which is comparable to the shadow masking device of chapter 3.2.2. The high level of $V_{OH} = 2.9\,V$ is only reached at negative input voltages of $V_I = -1\,V$. The reason for this is the threshold voltage of the n-type transistor, which reveals $V_T = -1.5\,V$, making the device normally-on (compare chapter 1.2.2).

The gain of 4.2 can also be contributed to the weak performing n-type transistor. The output characteristics show that saturation is not reached within the inverter voltages (figure 3.13(c)). Also the threshold voltage has a negative influence on the inverter gain.

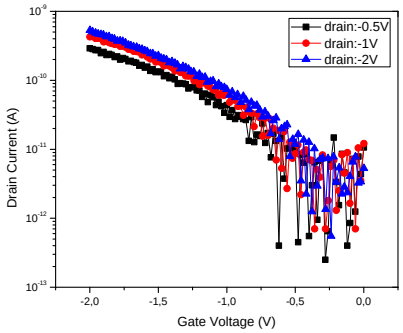
It can be concluded that in order to improve the nanoimprint inverter performance further studies concerning especially the n-type transistor are required.



(a) Output characteristics

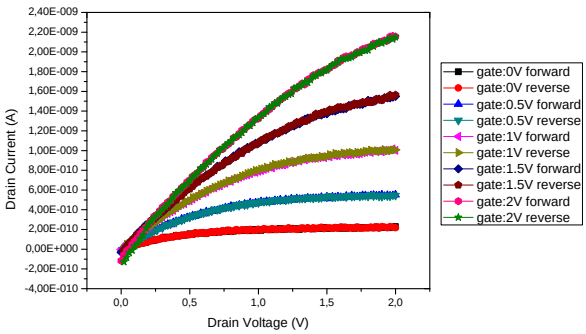


(b) Transfer characteristics

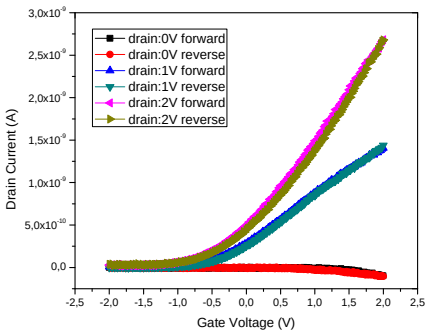


(c) Subthreshold characteristics

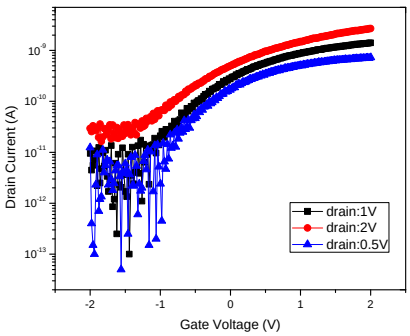
Figure 3.12: NIL inverter: electrical measurement results of the p-type transistor



(a) Output characteristics



(b) Transfer characteristics



(c) Subthreshold characteristics

Figure 3.13: NIL inverter: electrical measurement results of the n-type transistor

4. Conclusions and Outlook

The results of this work are:

- We are able to fabricate working organic thin film transistors by shadow masking with p-type as well as with n-type performance.
- Working unipolar inverters can be realized from these transistors, though their inverter transfer characteristics does not meet the requirements for a working ring oscillator.
- Shadow masking complementary inverters are realized with a very good gain of over 50 and good high and low levels.
- Ring oscillators are fabricated from these complementary inverters. The yield of the single transistors prevented the measurement of oscillation.
- Process transfer to nanoimprint lithography and the realization of sub micrometer channel length OTFTs is possible, also complementary inverters with a gain of over 4 have been fabricated.

Further research should be put in the NIL-devices to improve the inverter performance. Saturation of the single transistors as well as a better on/off current ratio are crucial to increase the gain as well as the high and low levels of the inverters. Furthermore the fabrication of NIL ring oscillators is a next logic step. This makes it necessary to invent a new technology to structure the dielectric layer, as far as the source and drain of one stage have to be electrically connected to the gate of the following stage.

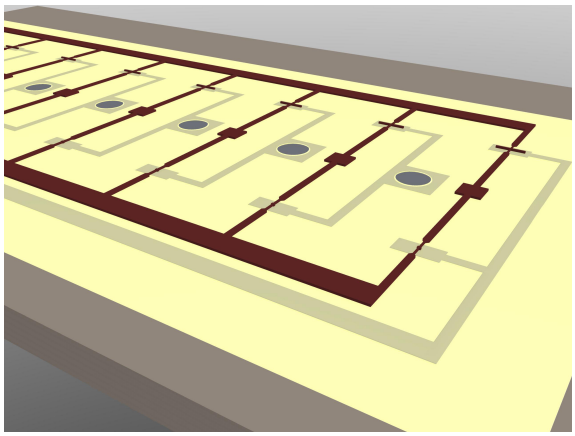


Figure 4.1: Schematics of a nanoimprinted ring oscillator

We propose the usage of a resist, which is structured on the substrate by ink-jet printing prior to the dielectric layer. A simple liftoff step should be sufficient to allow for good conductivity. Figure 4.1 shows this possible solution.

Abbreviations

C	...	capacitance
C'	...	specific capacitance
e	...	elementary charge
f_0	...	cutoff frequency
G	...	inverter gain
γ	...	sputter yield
I_D	...	source drain current
I_{Ion}	...	Ion current density
L	...	channel length
μ	...	mobility
μ_{FET}	...	device mobility
t_f	...	fall time
t_r	...	rise time
V_D	...	drain voltage
V_G	...	gate voltage
V_I	...	input voltage
V_{IH}	...	minimum input voltage recognized as high
V_{IL}	...	maximum input voltage recognized as low
V_O	...	output voltage
V_T	...	threshold voltage
W	...	channel width

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