Diploma Thesis

Eva-Maria Hanzl

Analog Front End for a Contactless Desktop Reader supporting ASK and PSK modulation techniques

Master's Thesis
(DA656)

at

Graz University of Technology

submitted by

Eva-Maria Hanzl

Institute of Electronics (IFE),
Graz University of Technology
A-8010 Graz, Austria

Assessor: Ass.-Prof. Dipl.-Ing. Dr. techn. Peter Söser
Supervisor: Dipl.-Ing. Josef Gruber (Infineon Technologies Austria AG)

June 21st, 2010

© Copyright 2010 by Eva-Maria Hanzl

TU Graz
Graz University of Technology

infineon

Analog Front End for a Contactless Desktop Reader supporting ASK and PSK modulation techniques

Diplomarbeit
(DA656)

an der

Technischen Universität Graz

vorgelegt von

Eva-Maria Hanzl

Institut für Elektronik (IFE),
Technische Universität Graz
A-8010 Graz, Austria

Begutachter: Ass.-Prof. Dipl.-Ing. Dr. techn. Peter Söser
Betreuer: Dipl.-Ing. Josef Gruber (Infineon Technologies Austria AG)

21. Juni 2010

© Copyright 2010, Eva-Maria Hanzl

Diese Arbeit ist in englischer Sprache abgefasst.

Abstract

In recent years, RFID has become a large success in nearly every industry sector. This is, due to RFID systems' opening up of various possibilities of automatisation in the areas of state recording and flow control. By the time, new demands were made on RFID systems concerning higher data rates and the feasibility of reading a higher number of RFID tags at the same time.

For the purpose of object- and itemidentification, the ISO/IEC 18000-3 standard was specified. Whilst mode 1 of this standard is similar to the ISO/IEC 15693 vicinity standard, mode 2 comprises another standard approach. In that, stackability is achieved using Phase Jitter Modulation (PJM) and because of the feasibility of multichannel replies a high number of RFID tags can be identified quickly. Up to 1500 tags per second can be identified via this mode [1]. Since mode 1 and mode 2 are using different technology, there does not yet exist a reading device which unites both modes.

The instant thesis deals with the integration of both modes 1 and 2 of the ISO/IEC 18000-3 standard embedded into one reading device. Collaborating with the thesis 'Transceiver design for a contactless desktop reader supporting MODE 1 and MODE 2 of ISO/IEC 18000-3' of Selma Skoljic, a demonstration reader was developed which enables the communication between a PC and a transponder based on the ISO/IEC 18000-3 standard.

On the basis of established technology, the analog frontend of a contactless reading device is developed in this thesis. This involves a usable structuring of the overall system, the investigation of several system segments and component parts and the integration of the system segments into one complete system. To finalise the work, the resulting system is verified and the results are summarized in this thesis.

Kurzfassung

In den letzten Jahren hielten RFID Systeme aufgrund der durch sie gebotenen Möglichkeiten im Hinblick auf Automatisierung von Zustandserfassungen und Abläufen in vielen verschiedenen Anwendungsbereichen Einzug in fast jedem Industriezweig. Dabei wird, neben der Forderung nach einer schnellen Übertragung immer größerer Datenmengen, auch der Bedarf an einer schnellen Identifikation einer immer größeren Menge von Transpondern immer höher.

Der Standard ISO/IEC 18000-3 wurde speziell im Hinblick auf Objekt- und Artikelidentifikation spezifiziert. Während Mode 1 der Vicinity-Norm ISO/IEC 15693 entspricht, wird in Mode 2 ein weiterer Standard festgelegt, in dem mittels Phase Jitter Modulation (PJM) eine Stapelbarkeit der Transponder erzielt und durch Multichannel-Reply eine hohe Identifikationsrate für Tags erreicht wird. Mittels dieses Mode 2 können bis zu 1500 Tags in der Sekunde identifiziert werden [1].

Mode 1 und Mode 2 sind in ihrer Technologie sehr unterschiedlich, daher steht noch kein Lesegerät zur Verfügung, welches diese beiden Modi in sich vereint. Die vorliegende Diplomarbeit beschäftigt sich mit der Integration der beiden Modes 1 und 2 des ISO/IEC 18000-3 Standards in einem RFID Lesegerät. Zusammenwirkend mit der Diplomarbeit „Transceiver design for contactless desktop reader supporting MODE 1 and MODE 2 of ISO/IEC 18000-3“ von Selma Skoljic wird eine Demonstrationsplattform entwickelt, die die Kommunikation auf Basis des ISO/IEC 18000-3 Standards zwischen einem PC und einem Transponder ermöglicht.

Aufbauend auf bestehenden Technologien wird in der vorliegenden Arbeit das analoge Frontend eines kontaktlosen Lesegerätes entwickelt. Das beinhaltet die Erstellung einer passenden Struktur für das Gesamtsystem, die Untersuchung verschiedener Systemkomponenten und einzelner Bauelemente und die Implementierung der verschiedenen Segmente zu einem Gesamtsystem. Zum Abschluss erfolgt die Verifikation des resultierenden Systems.

Statutory Declaration

I declare that I have authored this thesis independently, that I have not used other than the declared sources / resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

Place	Date	Signature

Eidesstattliche Erklärung

Ich erkläre an Eides statt, dass ich die vorliegende Arbeit selbstständig verfasst, andere als die angegebenen Quellen/Hilfsmittel nicht benutzt, und die den benutzten Quellen wörtlich und inhaltlich entnommene Stellen als solche kenntlich gemacht habe.

Ort	Datum	Unterschrift

Danksagung

Diese Arbeit bietet mir nicht nur die Möglichkeit, meine interessante interdisziplinäre Arbeit der letzten Monate zu dokumentieren, sondern eröffnet mir vielmehr die Gelegenheit, den Menschen zu danken, die zum Erfolg dieser Arbeit beigetragen haben.

Mein Dank gilt der Infineon Technologies Austria AG, insbesondere Herrn Peter Raggam für die Möglichkeit, in seiner Arbeitsgruppe diese Diplomarbeit anzufertigen.

Ich danke Herrn Peter Pirc für die Leitung des Projekts. Bedanken möchte ich mich außerdem bei Herrn Josef Gruber, der mir immer mit Rat und Tat zur Seite stand. Nicht zuletzt durch die freundliche und engagierte Betreuung hat mir diese Arbeit viel Freude bereitet.

Weiterhin bedanke ich mich bei Prof. Peter Söser, der mir auf der Suche nach Lösungswegen immer Rede und Antwort stand.

Ich möchte mich an dieser Stelle auch bei meinen Kollegen bedanken - für die herzliche Aufnahme im Team und die Hilfsbereitschaft, mit der mir über die diversen kleinen Hürden jeglicher Art hinweggeholfen wurde.

Mein besonderer Dank gilt meinen Eltern und Großeltern für ihre uneingeschränkte Unterstützung, denn ohne sie wäre dieses Studium niemals möglich gewesen.

Eva-Maria Hanzl
Graz, Juni 2010

Contents

List of Figures

List of Tables

Chapter 1

Introduction

In the last decade, the automatic identification of objects and animals has more and more become a relevant topic in business and industry. Initially there was a general tendency for bar codes, but in the recent years the trend has turned to data mining and higher functionality. Therefore it becomes obvious to turn to smartcards to fulfill the more complex requirements. Since you further have the possibility of locating an object contactless, the need of radio frequency identification systems (RFID-Systems) arises.

An RFID system always consists of a reading device, in our case called *vicinity coupling device* (VCD), and one or more contactless data media, called *vicinity integrated circuit card* (VICC). It is distinguished between various types of RFID systems, depending on the operating frequency, the range of operation, the type of coupling between the reader and the tag, active or passive transponder, and so on.

This thesis focuses exclusively on vicinity coupling cards which are defined in the ISO/IEC 18000-3 standard. The operating frequency is 13.56 MHz and the maximum range of operation amounts to 1 meter.

The ISO/IEC 18000-3 standard consists of two modes: While mode 1 refers in most cases to ISO/IEC 15693, mode 2 significantly differs. Very noticeable in this context are the modulation of the data on the carrier via phase jitter modulation (PJM) at the transmission from VCD to VICC and the response of the VICC on one of the eight provided operating channels (subcarrier frequency channels).

Based on the ISO/IEC 18000-3 standard, the instant thesis deals with the (conceptual) design and the prototyping of a contactless desktop reader which combines both mode 1 and mode 2 of the referred standard, whereas in mode 2 only channel B is implemented. Based on this concept it will be easy to expand the reading path to the full eight channels defined in the ISO/IEC 18000-3 standard. The reader can be connected to a computer by USB cable and is also solely powered via this interface. It is possible to switch between the two modes of the ISO/IEC 18000-3 standard by software. Another special core issue for the development of this reading device is the requirement of a low budget concept.

In general, the designed reading device consists of an analog front-end part which performs on the one hand the modulation of the 13.56 MHz signal and emits this modulated signal via an antenna as magnetic field into the surrounding area and picks up on the other hand the load modulated signal (formed by the VICC) from the surroundings and executes the carrier demodulation. In this analog front-end there is an embedded microcontroller (STM32F103 - 'Cortex-M3' - from STMicroelectronics) which incures digital calculations like demodulation of the subcarrier, signal decoding and the communication with the affilated computer or database. The programming of this microcontroller was done by Selma Skoljic in the course of her thesis 'Transceiver

design for contactless desktop reader supporting MODE1 and MODE2 of ISO/IEC 18000-3', while the instant thesis treats the development of the analog frontend part.

All the needed information to understand the entire analog frontend of the developed RFID reader is given in this thesis. Therefore, each chapter of the thesis builds on its predecessors. In chapter 2, the basics of RFID systems (according to [8]) are explained. It is shown of which components an RFID system consists and how RFID systems are classified. In this chapter it is also illustrated how the power supply of the transponder is accomplished and how the data is generally transmitted from VCD to VICC and vice versa. In chapter 3 the communication fundamentals of RFID systems explained. They will be needed to understand the special coding and modulation techniques specified in the ISO/IEC 18000-3 standard. In chapter 4, the ISO/IEC 18000-3 standard will be explained in greater detail, whereas the modulation and the coding of the data in both modes is catered to. Furthermore, the specification of the signal characteristics is introduced. The function of the used CSPC (carrier-suppressing pickup coil) antenna is explained according to [14] in chapter 5. Chapter 6 shows the realisation of the reading device. At the outset, the transmit path and the receive path are handled separately. Thereby different alternative basic concepts with their advantages and disadvantages are presented. Afterwards one concept is chosen to work on further. At the end of the chapter, the jointed overall system is outlined. The measuring results of the realised prototype can be found in chapter 7. Finally, you can find a summary of the gained perceptions in chapter 8, followed by a short outlook on future works.

Chapter 2

Fundamentals of the RFID Technology

2.1. Introduction to RFID Systems

Among other systems like optical character recognition (OCR), barcode systems or biometric measurements, RFID belongs to the group of Automatic Identification Systems. There exists especially a very close relation to the smartcard sector, where the smartcards consist of a data storage and optionally additional computing capacity. These smartcards are inserted into plastic cards of the size of a credit card.

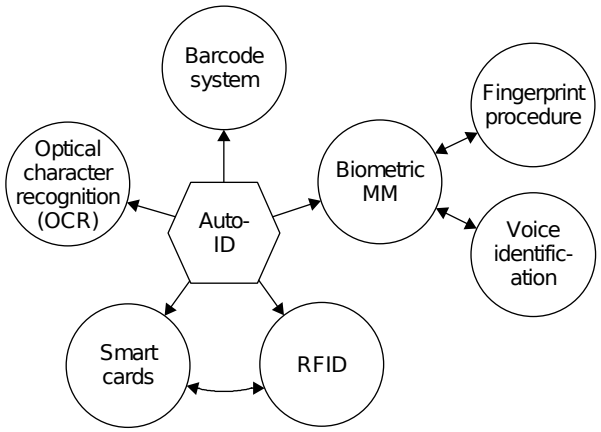


Figure 2.1.: Overview of the most important automatic identification systems [8]

To operate the integrated smartcard, the plastic card has to be inserted into a reading device which establishes a galvanic connection to the mating surface of the smartcard package. Through this connection the smartcard can be powered, clocked and communicated with through serial I/O interfaces. A disadvantage of the contact-based smartcards is the risk of malfunction caused by contaminated surfaces or abrasion.

Just like smartcards, RFID systems store data in an electronic data storage. The only difference is the way of how to establish a connection. In contrast to the galvanic connection which is established at smartcard systems, RFID systems use magnetic or electromagnetic fields to supply the data-carrying device and achieve a communication link.

RFID systems are used for contactless identification and location of objects or creatures. Sample applications would be time recordings at sports competitions, e-passports, automotive immobiliser systems or contactless timekeeping in companies.

2.2. Components of an RFID System

As you can see in figure 2.2, an RFID system generally consists of an RFID reader (interrogator) and one or more transponders.

The reader comprises a control unit, a radio frequency module and a coupling element (i.e. an induction coil) which initiates an electromagnetic field in its close ambience. Furthermore, most of the reading devices also contain an interface to allow data interchange to external systems (data exchange with databases or control systems).

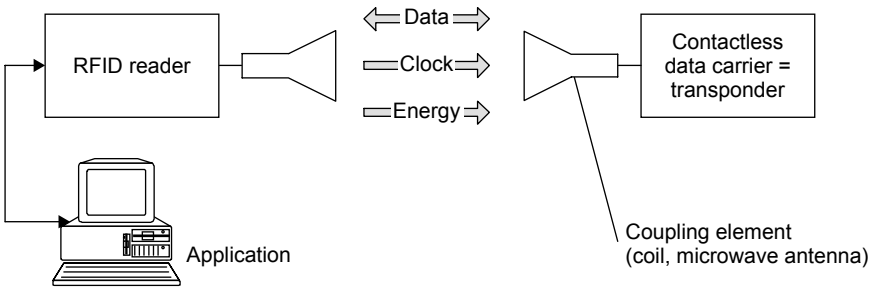


Figure 2.2.: Basic components of RFID Systems [8]

A transponder implies a coupling element and an electronic smartcard. Although also transponders with an attached power supply exist, there is usually no inbuilt battery joined. All the supply energy for driving the smartcard is gained from the magnetic or electromagnetic field produced by the reading device.

2.3. Classification of RFID Systems

Since the technology of RFID has become a true success story, an innumerable amount of different options in this field has evolved. This chapter will give you a slight overview of how to distinguish between many varieties of RFID systems.

2.3.1. Full- and Halfduplex Systems, Sequential Systems

Among RFID systems, it is distinguished between the following types of operation: fullduplex (FDX), halfduplex (HDX) and sequential systems (SEQ).

At full- and halfduplex systems, the RF-field is kept online whilst the transponder transmits data to the reader. In contrast, the RF-field is switched off cyclically when operating with sequential systems. In this case the transponder uses the time slots without the external field to transmit data to the interrogator. The disadvantage of this method is that the power supply of the transponder is periodically interrupted, so that additional backup capacities or batteries are needed.

2.3.2. Power Supply

Another important attribute of RFID systems is the power supply of the transponder. Two different types of transponders exist: passive and active transponders.

A passive transponder has no proper power supply attached. It takes all the power it needs in order to operate reliably via a fixed antenna from the surrounding magnetic or electromagnetic field. If the transponder is beyond the range of the interrogator, it does not receive any energy and is therefore not able to do any operations or send any signal.

On the contrary, an active transponder has its own power supply (i.e. a battery or a solar cell) attached, which provides the chip with energy. Since the transponder has no necessity to get all the energy to operate from the surrounding magnetic or electromagnetic field, the range of communication increases in comparison to a passive transponder.

2.3.3. Operating Frequency

RFID systems are driven by a huge variety of different operating frequencies, beginning at less than 135kHz and lasting up to 5.8 GHz. As you can see in table 2.1, there are four different frequency spectra, in which it is allowed to implement RFID systems.

Description	**Frequency range**	**Allowed frequencies**
Long wave (LF)	30 kHz ... 300 kHz	9 kHz ... 135 kHz
Short wave (HF/RF)	3 MHz ... 30 MHz	6.78 MHz, 13.56 MHz, 27.125 MHz, 40.680 MHz
Ultrahigh frequency (UHF)	300 MHz ... 3 GHz	433.920 MHz, 869 MHz, 915 MHz, 2.45 GHz
Microwaves	> 3 GHz	5.8 GHz, 24.125 GHz

Table 2.1.: Classification of frequency ranges and typical RFID operating frequencies (adapted from [8])

2.3.4. Range

RFID systems typically achieve ranges of some millimeters up to more than 15 meters. For classification of RFID systems according to their range see Table 2.2.

System		**Typical Maximum Range**
Close coupling		1 cm
Remote coupling	Proximity	15 cm
	Vicinity	100 cm
Microwaves		>>1 m

Table 2.2.: RFID ranges

2.3.5. Coupling

The physical coupling occurs either by electric (capacitive), magnetic (inductive) or electromagnetic fields. In most cases, the chosen coupling mode depends on the operating frequency and the required range.

Close coupling systems are either electrically or magnetically coupled, remote coupling systems are mostly magnetically, but in some cases also electrically coupled and long range systems are solely electromagnetically coupled.

2.3.6. Classification of the Examined System

The instant thesis treats the RFID system specified in the ISO/IEC 18000-3 standard. This standard deals with halfduplex systems comprising exclusively passive transponders with vicinity coupling cards. The operating frequency is 13.56 MHz. The coupling occurs magnetically.

2.4. Power Supply

Since the examined system uses passive transponders, one task of the transponder is to gain the needed energy to operate the attached chip from the surrounding electromagnetic field emitted by the reader. In our case, the reader emits a magnetic field of 13.56 MHz, which accords to a wavelength of 22.1 m. Because the wavelength is in our case much bigger than the distance between the reader and the transponder (vicinity coupling), the transponder moves within the near field of the readers' antenna. In this near field distance we can treat the electromagnetic field as a simple alternating magnetic field. The part of the emitted magnetic field which flows through the transponder's coil induces a certain voltage in it. This voltage can be commutated and used as power supply.

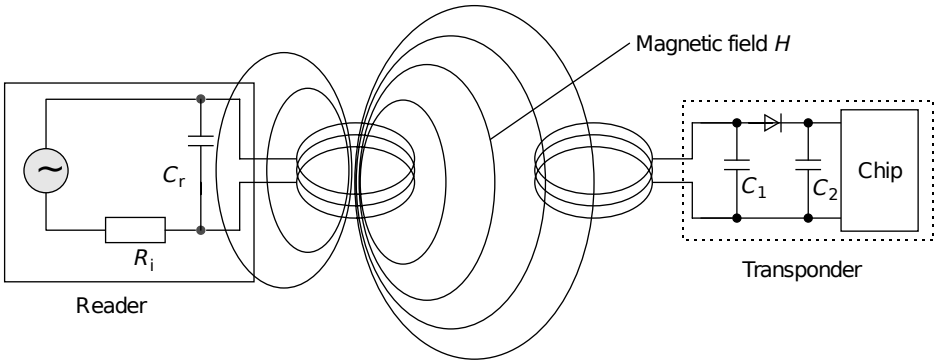


Figure 2.3.: Power supply to an inductively coupled transponder from the energy of the magnetic alternating field generated by the reader [8]

As you can see in figure 2.3, there is for both, reader and transponder, a capacitor connected to form a parallel resonant circuit together with the inductance of the antenna coil. This brings the advantage of a resonance magnification to produce on the one hand high currents in the antenna (to gain high field strengths), and on the other hand a high collected voltage (to power the transponder's chip).

2.5. Data Transfer from VCD to VICC

For the transmission of data from the reader to the transponder the magnetic field, which is used to power the VICC, is modulated. There are generally three types of modulation used:

- ASK: amplitude shift keying
- FSK: frequency shift keying
- PSK: phase shift keying

They are employed independently from the operating frequency, the way of coupling or whether the instant system is a full- or halfduplex system. Nevertheless, in most cases amplitude shift keying is implemented because of its easy way of demodulation.

2.6. Data Transfer from VICC to VCD

Generally, it can be shown that the used system of two coils which are linked via a magnetic field in the range of their near field can be considered as a transformer.

If a resonant transponder is brought into the magnetic alternating field of a reading device, the transponder detracts energy from this field. By the attenuation of the field, the current in

the readers' antenna decreases. The reason for this is the induced current in the transponder's coil, which retroacts to the readers' antenna via the mutual inductance M.

To model the influence of the mutual inductance, we use an additional imaginary impedance, the *transformed impedance Z_T'*, which we can insert as a structural element into our primary serial resonant circuit that represents the readers' antenna (figure 2.4). This imaginary impedance behaves in fact like a usual discrete element. If there is a present mutual inductance (transmitter in the near field), Z_T' has a value of $|Z_T'| > 0$, otherwise Z_T' has the value of $|Z_T'| = 0$.

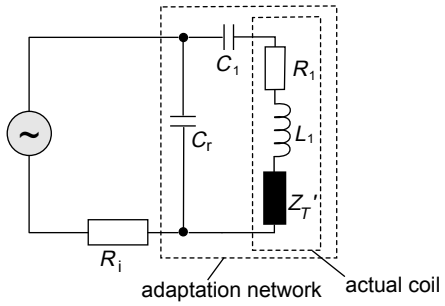


Figure 2.4.: Equivalent circuit of a reader including transformed impedance Z_T' (adapted from [8])

R_1 comprises in figure 2.4 the coil resistance and L_1 the inductance of the antenna. C_1 is inserted to define, in combination with L_1, the resonance frequency.

By switching an additional parallel load at the transponder's antenna (see figure 2.5), the transformed impedance Z_T' in the reader's circuit can be altered, which induces voltage changes in the reader's antenna. The effect of the switching is an amplitude modulation of the voltage V_L over the antenna coil in the reading device evoked by the transponder. This voltage can be surveyed and evaluated by the reading device.

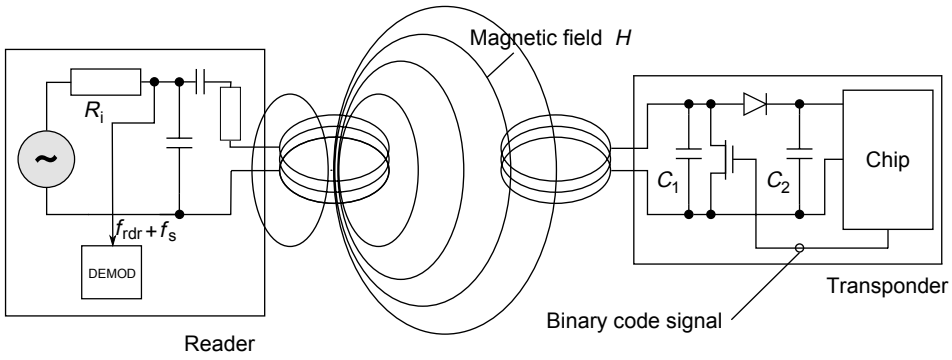


Figure 2.5.: Generation of a load modulation in the transponder by switching the drain-source-resistance of a FET on the chip (adapted from [8])

In this way it is also possible to transmit data from the transponder to the reader. To do so, the switching of the parallel load (load modulation) has to be related anyhow to the transmitted data. This relation can be a direct switching of the FET synchronously to the data, but for a better SNR it is recommended to use a modulated subcarrier to produce modulation sidebands, which are easier to detect and to demodulate for the reader.

In figure 2.6, the spectral diagram of a received load modulated signal is illustrated. The sidebands are symmetrically aligned around the carrier frequency f_c with the distance of the subcarrier frequency f_s. The actual information comes out of the subcarrier sidebands which arise from the modulation of the subcarrier itself.

For more details about the used modulation techniques refer to chapter 3, for the characterization of the particular system blocks please refer to chapter 4.

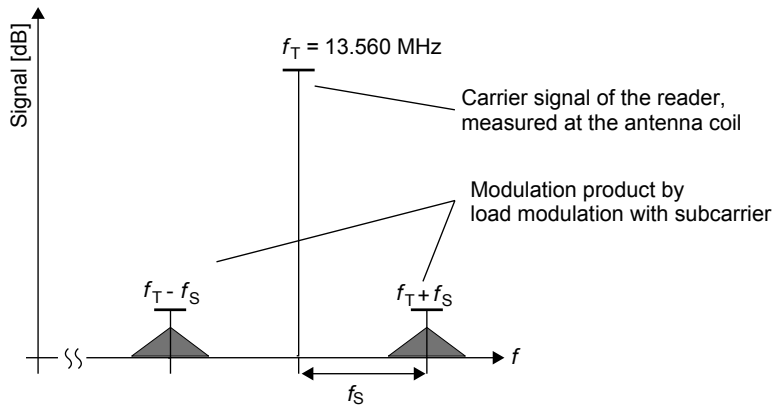


Figure 2.6.: Spectral diagram of a received load modulated signal (adapted from [8])

Chapter 3

Coding and Modulation

The following chapter describes the communication fundamentals of RFID systems. It is held tight to the category groups which will be deployed to engineer the reading device meeting the requirements of the ISO/IEC 18000-3, so only that part of a huge amount of modulation and coding techniques is treated which is applied in the following chapters. This chapter was composed referring to [14], [5], [8] and [12].

An RFID system can basically be depicted as a general digital communication system consisting of three common functional blocks as shown in figure 3.1.

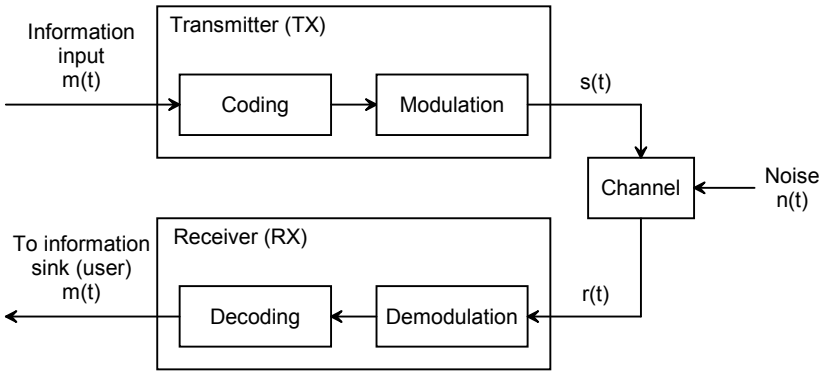


Figure 3.1.: Signal and data flow in a basic digital communication system [14]

Signal Coding:
The main item of signal coding is to adapt the description of the transmitted signal best possible to the characteristics of the communication channel. The aim of doing this is to make the signal robust against disturbances and collisions during the transmission. Signal coding does not alter the frequency range of the transmitted signal, therefore it is often referred to as *baseband encoding*.

Modulation:
To modulate a signal (usually a high-frequency carrier) means to change one of its parameters (amplitude, phase or frequency) according to the modulating signal, the so-called baseband signal. The modulation is used to shift the data's baseband frequency to a frequency matching the channel characteristics and to utilise the entire bandwidth of the channel.

Channel:
The channel represents the distance passed through the transmission medium. Usually the signal is distorted during the transmission and noise is added. So the signal received at

the demodulator is an imperfect signal. For RFID systems, the transmission media are exclusively magnetic fields or electromagnetic waves.

Demodulation:
The aim of demodulation is the recreation of the baseband signal from the received modulated carrier signal.

Decoding:
The reconstruction of the original information and, where applicable, the detection and correction of transcription errors is done in the signal decoding unit.

3.1. Baseband Signal and Coding Functions

In order to understand the frequency spectra which are induced by the modulation techniques presented in chapter 3.2, the characteristics of the baseband signal are discussed preparatively below.

Digital information is stored in the form of bits. If transmission of these bits is necessary, they firstly need to be expressed in some kind of waveform. A digital waveform is a time representation of bits. By the definition of an adequate coding function it is possible to develop a time function out of a bit stream. An easy coding function for example was the definition of the high-state of a bit by 1V and the low-state by 0V. Additionally, the time of one bit T_b (called *bit duration* $[\frac{s}{bit}]$) has to be fixed. With these two specifications it is already possible to do a sample coding of a given bit string '01001011010'. The resulting waveform can be found in figure 3.2. Further coding functions are used in the ISO/IEC 18000-3 standard. They will be introduced according to the applying modes in chapter 4.

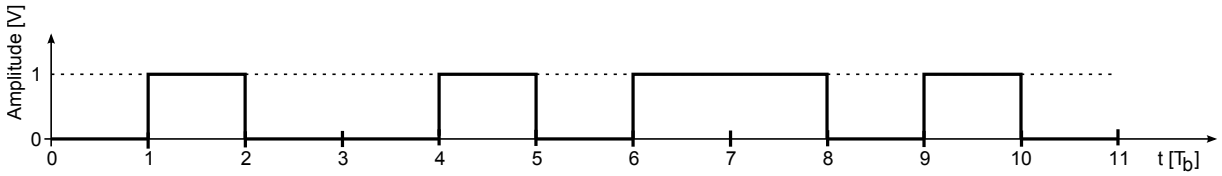


Figure 3.2.: Time function representing the coded bit string '01001011010'

The reciprocal value of the bit duration is the *bit rate* r_b $[\frac{bits}{s}]$.

Generally, a rectangular pulse signal is defined by its amplitude A and the pulse width T_b. From this information we can evaluate the spectrum of the signal by calculating its Fourier transform:

$$s(t) = A \cdot rect(\frac{t}{T_b}) \qquad \circ\!\!-\!\!- \qquad S(f) = A \cdot T_b \cdot sinc(\pi f T_b) \tag{3.1}$$

Where $sinc(\pi f T_b)$ is obtained as:

$$sinc(\pi f T_b) = \frac{sin(\pi f T_b)}{\pi f T_b} \tag{3.2}$$

Since a *sinc*-function is infinitely long, the same is valid also for the spectrum of a rectangular pulse. A sample pulse and its corresponding frequency spectrum is depicted in figure 3.3. Using this spectral representation, we can determine the bandwidth until the first null amplitude, the so-called *first null bandwidth*. For a perfect pulse with a duration of T_b, the first null bandwidth of the baseband signal B_{LF} is:

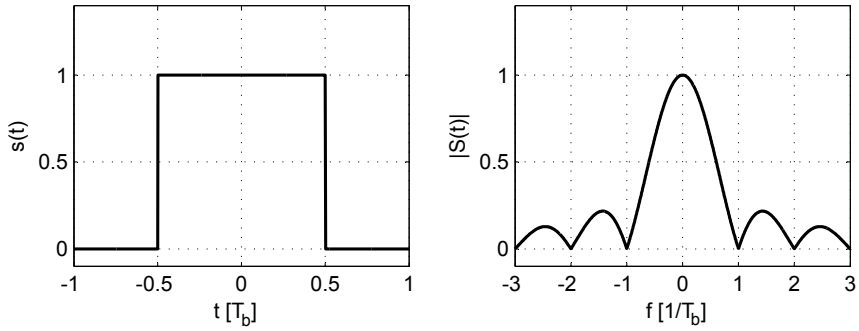


Figure 3.3.: Rectangular pulse and its Fourier transform [12]

$$B_{\mathrm{LF}} = \frac{1}{T_{\mathrm{b}}} \tag{3.3}$$

Derived from equation 3.3 it can be summarized that the shorter the symbol duration gets, the greater the claimed bandwith becomes. The above quoted null bandwidth is only valid for baseband signals. For bandpass modulated signals whose spectral centers are shifted to carrier's frequencies the first null bandwidth is doubled. This is because by the modulation and thereby the shifting of the spectral center the negative frequencies of the spectrum are getting visible. In that case the bandpass first null bandwidth B_{HF} calculates to:

$$B_{\mathrm{HF}} = \frac{2}{T_{\mathrm{b}}} \tag{3.4}$$

For optimal channel bandwidth utilisation the aim of each designer is to keep the used bandwidth of a data transmission as small as possible. A common possibility to optimize the used bandwidth of a signal is *pulse shaping*. Pulse shaping is implemented by the use of special filters which remove the high frequency parts of the signal. There are various different filters with different filter characteristics in use, although the *raised cosine filter* is the most common one. The effect on the baseband signal in the time domain is a smooting of its envelope.

3.2. Digital Modulation Techniques

In an RFID system complying to ISO/IEC 18000-3 the reader generates an alternating magnetic field to supply the transponder with energy. This magnetic field is represented by a sinusoidal, high-frequency waveform s(t) which can be generally described by equation 3.5. This waveform can be used as a carrier signal to transmit data by altering one of its signal parameters according to a baseband signal representing the information.

$$\begin{aligned} s(t) &= A_0(t) \cdot cos(\omega_0(t)t + \varphi_0(t)) \\ \omega_0(t) &= 2\pi f_0(t) \\ \mathrm{A}_0 \quad &... \quad \text{carrier amplitude} \\ \mathrm{f}_0 \quad &... \quad \text{carrier frequency} \\ \varphi_0 \quad &... \quad \text{carrier phase} \end{aligned} \tag{3.5}$$

As you can see in equation 3.5, there are the three signal parameters amplitude, frequency and phase which can be altered accordingly to the data to be transmitted. Consequently, there exist three basic modulation principles according to the altered parameter in order to transmit

information: *amplitude*, *phase*, and *frequency modulation*. All the other modulation processes are derived from these analog basic types. For RFID systems, the digital modulation processes *amplitude shift keying (ASK)*, *frequency shift keying (FSK)*, and *phase shift keying (PSK)* are used. For each modulation process there arise modulation products, so-called *sidebands*, which are located symmetrically around the carrier as shown in figure 3.4. The spectrum and the amplitude of these sidebands are influenced by the spectrum of the code signal in the baseband and by the type of modulation.

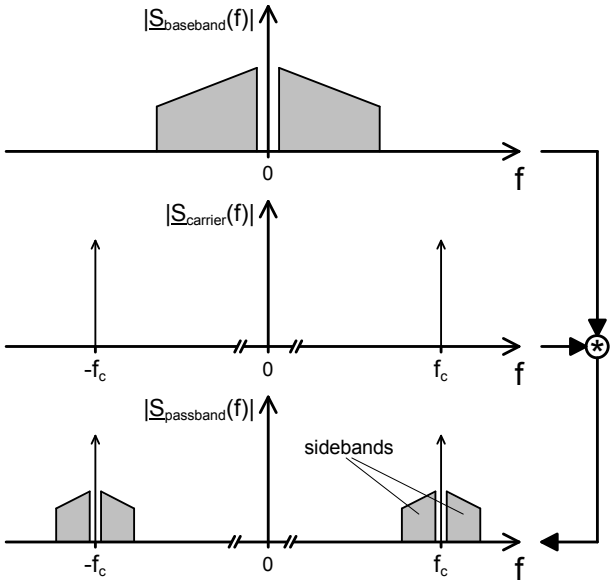


Figure 3.4.: Modulation sidebands arisen by the modulation of a sine shaped carrier [14]

In the following chapters, the modulation types relevant for the ISO/IEC 18000-3 standard will be elaborated in more detail.

3.2.1. Amplitude Shift Keying (ASK)

3.2.1.1. Features and Modulation Process

At amplitude shift keying the amplitude of a high-frequency carrier signal is switched between the states of a coded signal. The relation between the baseband signal and the coded signal depends on the coding function, as mentioned in chapter 3.1. In the simplest case, the amplitude is just switched between the two states of a binary coded signal.

In equation 3.6, an abstract carrier signal is described. In this formula, the amplitude modulation arises from the time dependence of the signal's amplitude A(t). The amplitude is varied by the time depending on the modulating signal's state.

$$s(t) = \underbrace{A(t)}_{\text{baseband information}} \cdot \underbrace{cos(\omega_0 t + \varphi_0)}_{\text{constant oscillation}} \tag{3.6}$$

A parameter of the amplitude modulation is the modulation depth, characterized by the *modulation index m*. This modulation index is a measure for the ratio of the amplitude levels. The most simple type of amplitude modulation is On-Off-Keying (OOK), which accords to a 100 % ASK modulation (see figure 3.5(a)). OOK is for example used for data transmission from VCD to VICC in mode 1 of the ISO/IEC 18000-3 standard. But there are also other modulation indices possible. Assuming the carrier signal is a voltage signal, m is calculated by equation

$$m = \frac{\widehat{u}_{HI} - \widehat{u}_{LO}}{\widehat{u}_{HI} + \widehat{u}_{LO}} \cdot 100\,\% \tag{3.7}$$

and ranges from 0 % to 100 %, whereby 0 % means no modulation and 100 % intends one amplitude state to be zero.

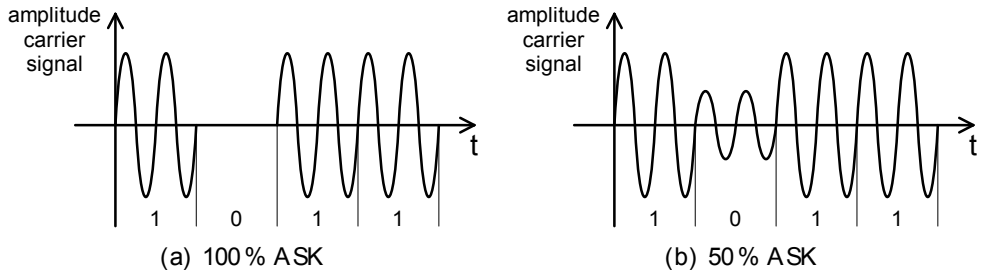


Figure 3.5.: ASK modulation indices [14]

A binary code signal consists of a sequence of high- and low-states. Mathematically, ASK-modulation results from the multiplication of a code signal $u_{code}(t)$ and the carrier signal $u_{carrier}(t)$, depicted in figure 3.6. The modulation index depends on the levels of the baseband signal. For example, an 100 % OOK carrier is achieved by setting the low level of the baseband signal to zero.

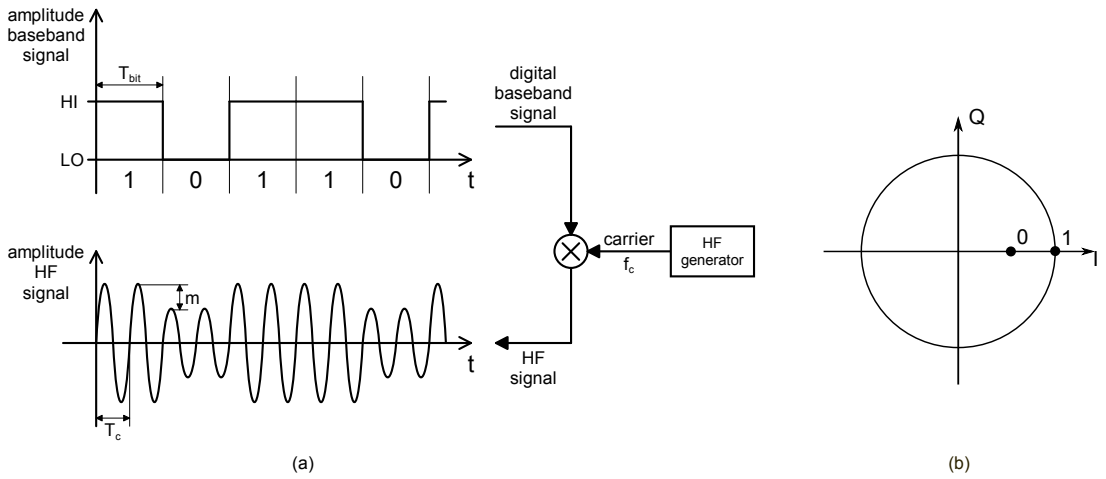


Figure 3.6.: Process of an ASK modulation and constellation diagram [14]

To examine the modulation process in the frequency domain, we have to do the Fourier transform on the time domain signals. Assuming a sinusoidal high-frequency carrier is modulated by a coded baseband signal, the mathematical evaluation of this proceeding would look like equations 3.8 to 3.11.

Baseband Signal:

$$s_{bb}(t) \circ\!\!-\!\!-\, \underline{S}_{bb}(f) = \mathcal{F}\left[s_{bb}(t)\right] \propto sinc(\pi f T_{bit}) \tag{3.8}$$

Carrier signal:

$$s_c(t) = cos(2\pi f_c t) = \frac{1}{2}(e^{j2\pi f_c t} + e^{-j2\pi f_c t}) \circ\!\!-\!\!-\, \underline{S}_c(f) = \frac{1}{2}[\delta(f - f_c) + \delta(f + f_c)] \tag{3.9}$$

Passband signal:

$$s_{pb}(t) = s_{bb}(t) \cdot s_c(t) \circ\!\!-\!\!-\, \underline{S}_{pb}(f) = \underline{S}_{bb}(f) * \underline{S}_c(f) \tag{3.10}$$

$$\underline{S}_{pb}(f) = \frac{1}{2}[\underline{S}_{bb}(f - f_c) + \underline{S}_{bb}(f + f_c)] \tag{3.11}$$

Since the modulated signal is gained in the time domain by multiplication of the carrier signal and the code signal, the result in the frequency domain is obtained by the convolution of the two signal spectra. The graphical result is shown in figure 3.7. As mentioned before, the signal spectrum of a modulated, sinusoidal carrier shows that the modulation causes sidebands which are located symmetrically around the carrier frequency and characterized dependent of the modulation technique and the spectrum of the modulating baseband signal.

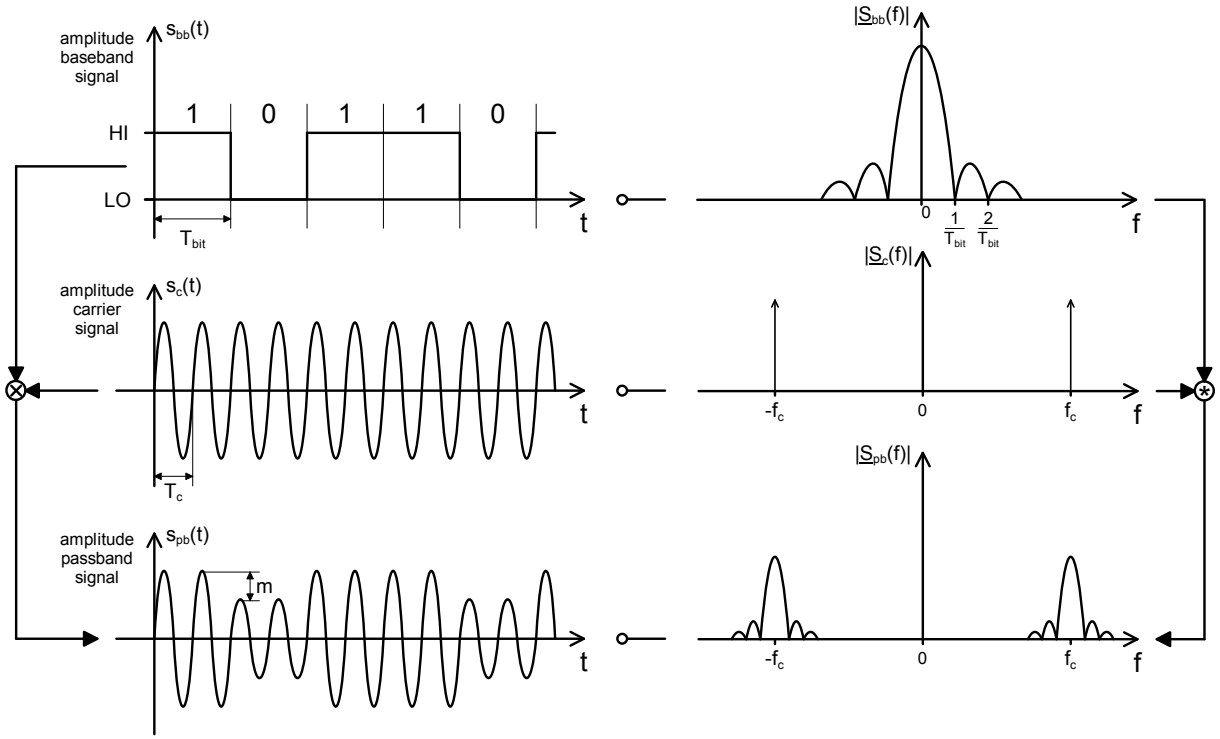


Figure 3.7.: Spectrum of an ASK modulated carrier [14]

3.2.1.2. Demodulation Process

The aim of demodulation is generally to reclaim the code signal (and out of this the data-carrying baseband signal) from a modulated carrier signal. Whilst the modulation process can be considered as baseband-passband transformation, the demodulation of a modulated signal is used to shift the passband signal back into the baseband frequency range. During the signal transmission through the channel, several channel characteristics like noise and damping are influencing the transmitted signal. Due to this fact the demodulated baseband signal does not perfectly equal the emitted, rectangular baseband signal. Therefore, in order to restore the emitted baseband signal it will be necessary to continue processing the demodulated signal by sampling it and assigning it to a high and a low baseband signal level, according to an appropriate decision level.

ASK modulation is used to transmit data from the reader to the transponder by 10 % or by 100 % modulation of the emitted magnetic field (for mode 1 of the ISO/IEC 18000-3), but also for data transmission from the transponder to the reader, carried out by load modulation, and can be interpreted as a form of amplitude shift keying.

When a carrier is amplitude modulated, the baseband information is packed directly onto the amplitude of the carrier signal. Therefore, it is obvious that the approach is considered to determine just the envelope of the received signal for demodulation. This approach is called 'incoherent ASK demodulation' due to the somewhat nonconformist proceeding. A more conformist proceeding was the 'coherent ASK demodulation', also referred to as *synchronous demodulation*. The following section will enlarge upon these two demodulation techniques.

Incoherent ASK Demodulation In case of incoherent ASK demodulation, so-called *envelope detectors* are used. Basically, these envelope detectors are rectifying the received, modulated HF signal and then suppress the carrier and thereby flatten the curve by applying an appropriate low-pass filter to the rectified signal (see figure 3.8).

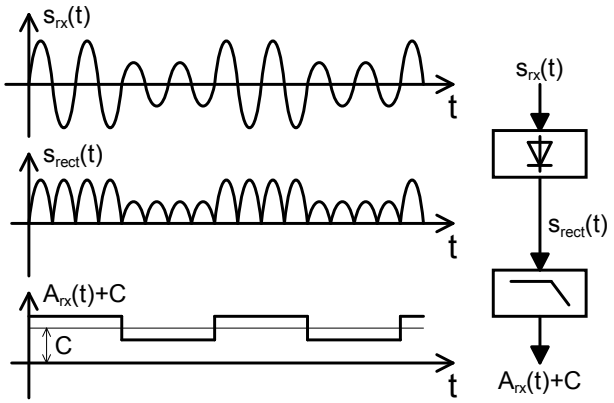


Figure 3.8.: Incoherent ASK demodulation [14]

Coherent ASK Demodulation In case of coherent ASK Demodulation, the received modulated carrier signal s_{rx} is multiplied by a signal of the same frequency and phase s_{lo}. This signal is gained for example by a local oscillator in the receiver.

$$\text{Transmitted Signal:} \quad s_{tx}(t) = A_{tx}(t) \cdot cos(\omega_c t + \varphi_c) \tag{3.12}$$

$$\text{Received Signal:} \quad s_{rx}(t) = A_{rx}(t) \cdot cos(\omega_c t + \varphi_c) \tag{3.13}$$

$$\text{Local Oscillator:} \quad s_{lo}(t) = cos(\omega_{lo} t + \varphi_{lo}) \tag{3.14}$$

Ideally, the frequency of the local oscillator's signal equates the carrier frequency. In practice, the two frequencies are slightly different, but commonly these differences are negligible. In order to ease mathematics, the frequency of the local oscillator at this point is defined to exactly equate the carrier frequency.

$$
\begin{aligned}
\widetilde{s}_{rx}(t) &= s_{rx}(t) \cdot s_{lo}(t) = \\
&= A_{rx}(t) \cdot cos(\omega_c t + \varphi_c) \cdot cos(\omega_c t + \varphi_{lo})^{1} = \\
&= \frac{1}{2} A_{rx}(t) \cdot cos(\omega_c t + \varphi_c - \omega_c t - \varphi_{lo}) + \frac{1}{2} A_{rx}(t) \cdot cos(\omega_c t + \varphi_c + \omega_c t + \varphi_{lo}) = \\
&= \frac{1}{2} A_{rx}(t) \cdot [cos(\varphi_c - \varphi_{lo}) + cos(2\omega_c t + \varphi_c + \varphi_{lo})]^{2} = \\
&= \frac{1}{2} A_{rx}(t) \cdot [cos(\varphi_c - \varphi_{lo}) + cos(2\omega_c t) cos(\varphi_c + \varphi_{lo}) - sin(2\omega_c t) sin(\varphi_c + \varphi_{lo})] = \\
&= \underbrace{\frac{1}{2} A_{rx}(t) cos(\varphi_c - \varphi_{lo})}_{\text{demodulated baseband signal}} + \underbrace{\frac{1}{2} A_{rx}(t) cos(2\omega_c t) cos(\varphi_c + \varphi_{lo})}_{\text{signal of double carrier frequency}} - \underbrace{\frac{1}{2} A_{rx}(t) sin(2\omega_c t) sin(\varphi_c + \varphi_{lo})}_{\text{signal of double carrier frequency}}
\end{aligned}
\tag{3.15}
$$

As you can see from equation 3.15, the resulting product consists of two components whose frequencies amount to the double of the carrier frequency and one component that is statically related to the amplitude of the modulated signal. This latter component complies with the transmitted baseband signal. To isolate this baseband signal from the double-frequenced part, the output of the carrier-frequency mixture has to be filtered by a lowpass filter.

Special attention has to be paid to the multiplicative term $cos(\varphi_c - \varphi_{lo})$ associated with the demodulated baseband signal. This term declares that the demodulation will be most effective if the phase between the incoming carrier signal and the local oscillator signal aspires to zero. If this phase amounts to exactly 90 degrees or an odd-numbered multiple of it, the amplitude of the output baseband signal will be zero. Therefore, measures (like for example synchronization procedures) have to be applied to obtain control over the phase deviation between the two mixed signals.

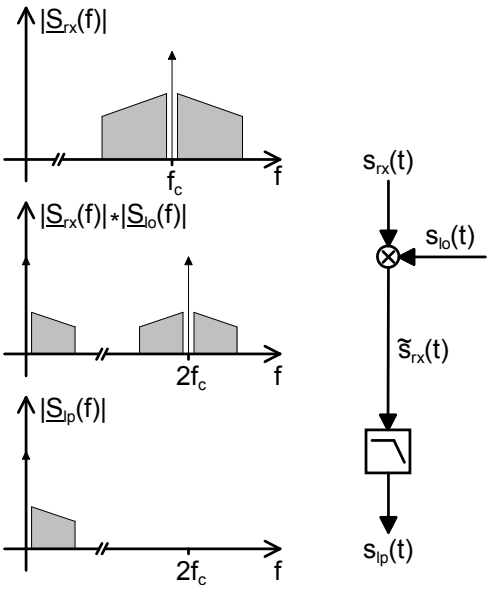


Figure 3.9.: Coherent ASK demodulation [14]

[1] $cos(a)cos(b) = \frac{1}{2}[cos(a+b) + cos(a-b)]$
[2] $cos(a+b) = cos(a)cos(b) - sin(a)sin(b)$

3.2.2. Binary Phase Shift Keying (BPSK)

3.2.2.1. Features and Modulation Process

Phase shift keying means that a sine carrier is modulated in discrete phase stages by a digital baseband signal. Mathematically, the modulated carrier can be expressed as

$$s(t) = A_0(t) \cdot cos(\omega_0 t + \varphi(t))$$

In the easiest case, the baseband consists of only two states which implies that the phase of the carrier will just take two states and switch between them. If so, one talks of binary phase shift keying (BPSK). BPSK can be described as a multiplication of a bipolar baseband and a (usually sinusoidal) high-frequency carrier signal. Usually, the baseband signal is coded the way that the state '1' accords to '1' and the state '0' accords to '-1'. In this case, the multiplication of the carrier results in a switching between the original and the inverted carrier signal, which can also be considered as a phase shift of 180° between the two phase states of the carrier signal. The modulator itself is assembled identically to the amplitude shift keying modulator.

Figure 3.10 shows the BPSK modulation procedure with an absolute initial phase of 0° and the adequate spectral diagram. Since the rectangular baseband signal equals the baseband signal of the ASK modulation, also spectrum stays the same. By the multiplication with the carrier frequency the same spectrum result is achieved, as it is with amplitude modulation.

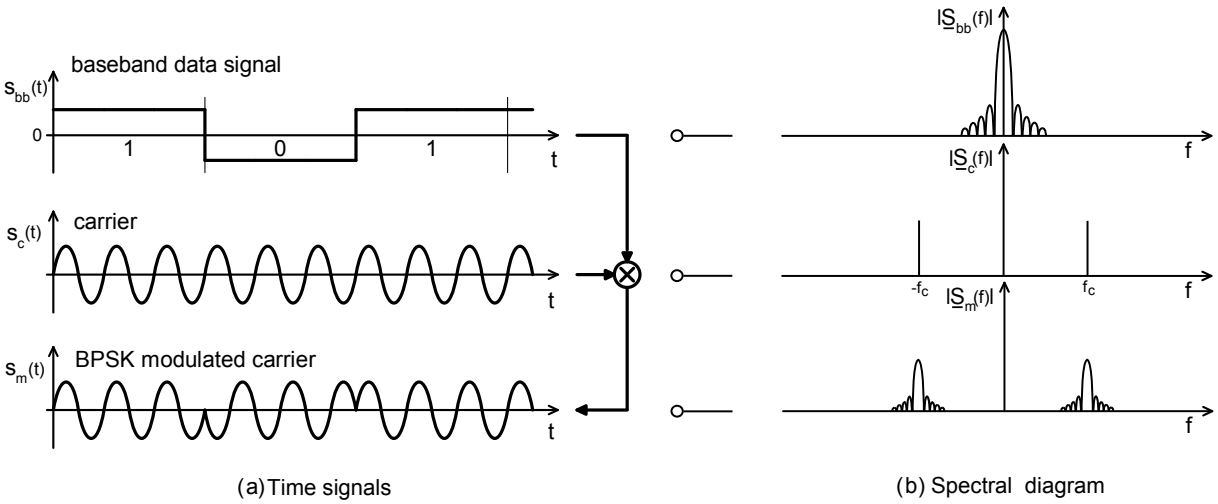


Figure 3.10.: BPSK modulation of a sinusoidal high-frequency carrier signal (modified from [14])

At the instant thesis, BPSK is used with the modulation of the subcarrier (see chapter 3.3) at data transfer using load modulation, according to the chapters 4.2.2 and 4.3.2. With having this application area in mind, a short disquisition of BPSK modulation on a subcarrier will follow. Since the subcarrier is a permanent rectangular waveshape, its spectrum consists of spectral lines on the subcarrier frequency and its odd-numbered multiple. The baseband function consists of a rectangular waveform in time domain and is represented by a sinc-function in the spectral domain. When building the product of the two functions in the time domain there occurs a convolution in the spectral domain, as shown in figure 3.11.

For BPSK of a rectangular subcarrier signal, the baseband signal and the subcarrier signal have to be exactly synchronized.

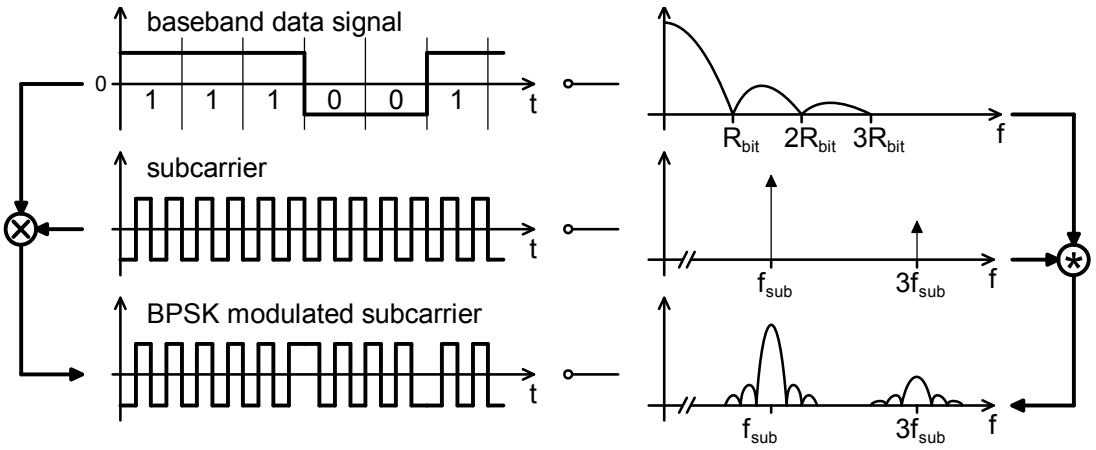


Figure 3.11.: BPSK modulation of a rectangular subcarrier signal [14]

3.2.2.2. Demodulation Process

There exist several ways to demodulate PSK modulated signals. Recent proximity cards exclusively use coherent demodulation techniques, so in this thesis only these types of demodulation will be considered. What all the coherent demodulation techniques have in common is the necessity of a synchronized carrier signal.

The first introduced BPSK demodulation scheme follows the same scheme like for coherent demodulation of ASK. Though, the BPSK signal is multiplied with the carrier waveform to reobtain the baseband signal (see figure 3.12). If the multiplied carrier signal is perfectly synchronized, no further filtering is necessary.

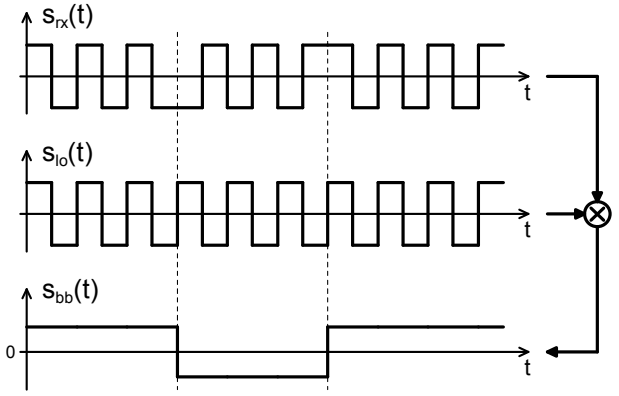


Figure 3.12.: Coherent demodulation of a BPSK modulated rectangular signal [14]

A second method for demodulating BPSK is the I/Q-demodulation method. This very general method of demodulating PSK signals uses the in-phase and the quadrature component concept (see figure 3.13). This method relies on the correlation between the modulated signal and the signals generated by the local oscillator. The integrators are measuring the correlation (over the duration of one period) of the in-phase and the quadrature output, and from that result the actual phase angle of the modulated signal can be determined by the arctan function. The I- and Q- fractions of the signal before and after the integration are depicted in figure 3.14.

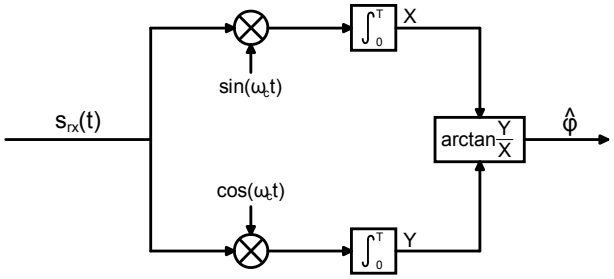


Figure 3.13.: Coherent demodulation of a general PSK modulated signal [14]

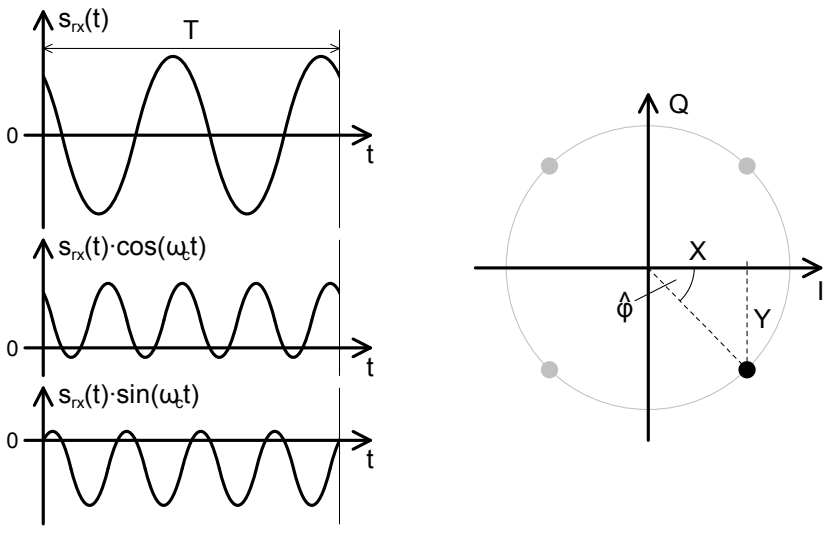


Figure 3.14.: Phase determination out of I- and Q-fractions [14]

3.2.3. Phase Jitter Modulation (PJM)

The basic fundamentals for Phase Jitter Modulation are gathered from [7]. Phase Jitter Modulation is a phase modulation with only very small phase jumps in the carrier signal. For the implementaion of PJM, the phase of the carrier signal f_c is altered for up to four degrees between the modulated and the unmodulated state (see figure 3.15).

$$s(t) = \underbrace{A_0}_{\text{constant amplitude}} \cdot cos(\underbrace{\omega_0 t}_{\text{constant frequency}} + \underbrace{\varphi(t)}_{\text{baseband information}}) \tag{3.16}$$

The time-dependent phase $\varphi(t)$ is composed of a constant initial phase and a positive or negative phase offset of about two degrees, depending on the state of the baseband signal.

$$\varphi = \underbrace{\varphi_0}_{\text{constant initial phase}} \pm \underbrace{\varphi_{bb}}_{\text{phase-offset}} \tag{3.17}$$

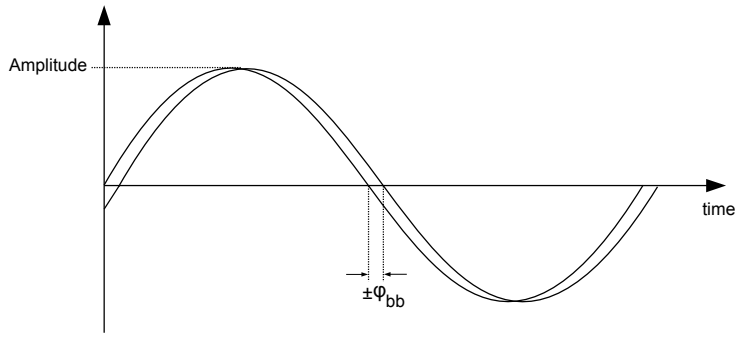
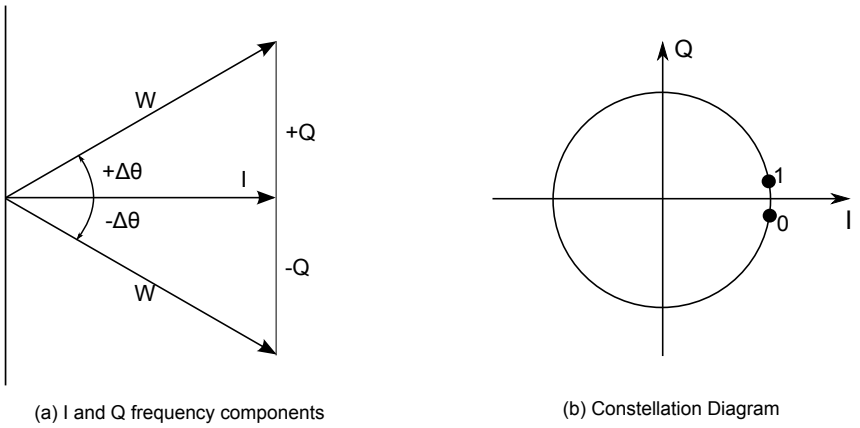


Figure 3.15.: Phase Jitter Modulation, time diagram [7]

Another view would be from the perspective of the frequency domain: Thereby the PJM signal can be split up into two components: An in-phase (0°) powering signal I and a low level quadrature (90°) data signal ±Q. The PJM waveform is the sum of these two signals. The outcome of this addition is shown in figure 3.16(a), the adequate constellation diagram can be found in figure 3.16(b). Because of the free choice of the zero-phase in the constellation diagram,it is also possible to define the unmodulated carrier signal to be on the real axis. In this case, the modulated carrier signal would get settled on the unit circle with four degrees of deviation to the unmodulated signal.



(a) I and Q frequency components (b) Constellation Diagram

Figure 3.16.: PJM signal in the frequency domain [7]

The spectral diagram of the signals during the modulation process is shown in figure 3.17. As already noted at BPSK modulation, the spectrum of the modulation behaves equally to the ASK spectrum.

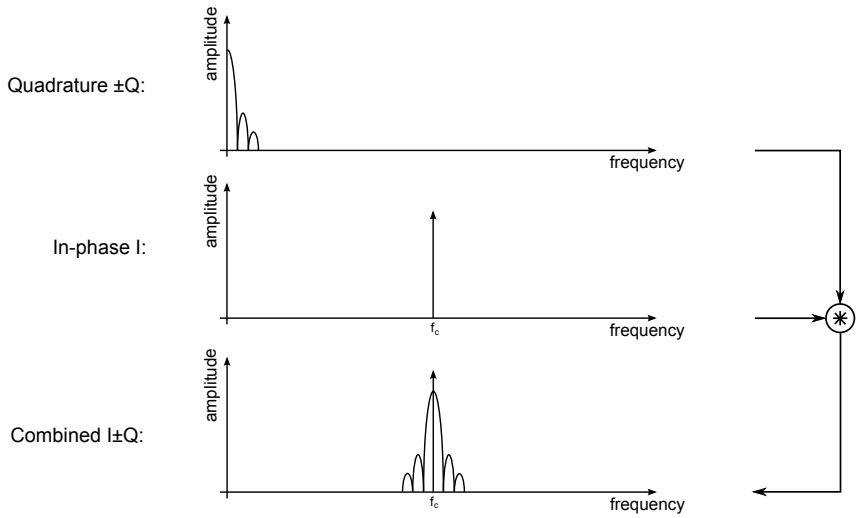


Figure 3.17.: PJM generation - frequency spectrum [7]

Features of PJM are:

- Constant amplitude signal with constant power transfer
- The sideband levels are independent of the data rate and can be adjusted to suit regulations
- Very high speed data can be transmitted because the PJM bandwidth is no wider than the original doublesided data bandwidth
- Narrow bandwidth antennas do not limit high speed PJM signals. PJM can be pre-compensated to cancel for the effect of antenna bandwidth.

3.3. Modulation with Subcarrier

As specified in the chapters 4.2.2 and 4.3.2, the ISO/IEC 18000-3 standard states a two-stage modulation of the carrier signal for the data transfer from VICC to VCD, which will then be transmitted by load-modulation.

This means that, instead of activating and deactivating the load resistance directly in the cycle of the baseband signal, this baseband signal first modulates a subcarrier by ASK, FSK or PSK modulation. The modulated subcarrier is then used to modulate the carrier signal.

Figure 3.18 shows a concrete example of how it is done. The baseband data, which is usually a sinc-function in the spectral domain, is modulated via BPSK on the subcarrier signal. Since the subcarrier is a steady, rectangular waveform, its spectral lines are arranged on the fundamental frequency of the rectangular shape and on its odd-numbered multiple. By that, the baseband spectrum gets arranged around the spectral lines of the subcarrier signal. This baseband modulated subcarrier then modulates the high-frequency carrier. As you can see, that places the data in the distance of $\pm f_{sub}$ around the carrier frequency f_c.

In contrast, without the subcarrier interstage, the data were located directly around the carrier frequency.

The arrangement of the two-stage modulation implicates the advantage of easier demodulateability of the signal, because the created frequency gap between the carrier and the sidebands eases the filtering process significantly.

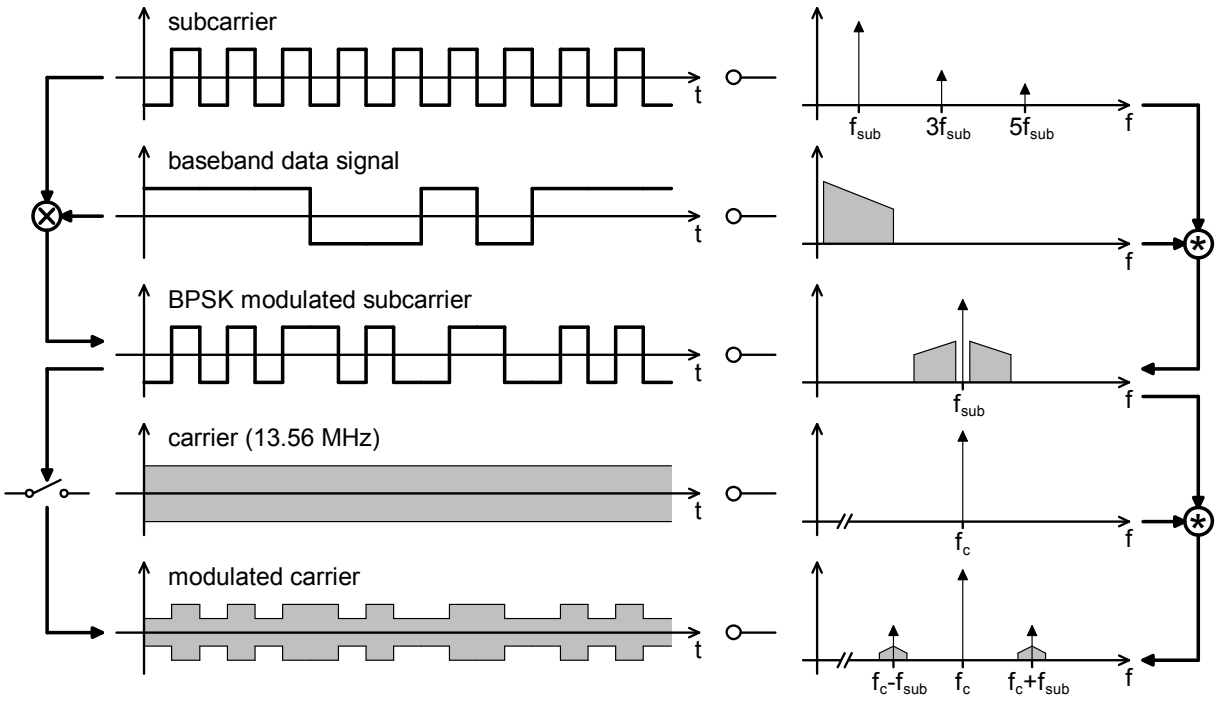


Figure 3.18.: ASK with subcarrier [14]

Chapter 4

ISO/IEC 18000-3 Standard

4.1. Introduction

The ISO (International Organization for Standardization) together with the IEC (International Electrotechnical Commission) form the instrument which develops the international technical standards. The aim of these standards is to regulate protocols and interfaces, to minimize software and implementation costs and to enable system management and control in order to reduce integration and migration problems between different systems.

The ISO/IEC 18000, entitled 'Information technology - Radiofrequency identification for item management', has been prepared to provide a framework to define common communications protocols for internationally useable frequencies for Radio Frequency Identification (RFID). It consists of the following parts:

- Part 1: Reference architecture and definition of parameters to be standardized
- Part 2: Parameters for air interface communications below 135 kHz
- Part 3: Parameters for air interface communications at 13.56 MHz
- Part 4: Parameters for air interface communications at 2.45 GHz
- Part 5: Parameters for air interface communications at 5.8 GHz
- Part 6: Parameters for air interface communications at 860 MHz to 960 MHz
- Part 7: Parameters for active air interface communications at 433 MHz

The instant thesis was developed according to part 3 of the ISO/IEC 18000 standard (ISO/IEC 18000-3), at which the frequency f_c (carrier frequency) of the RF operating field is 13.56 MHz ± 7 kHz. This standard generally consists of three modes: Mode 1 agrees on many points with ISO/IEC 15693, while mode 2 and mode 3 are defined very independently. The three modes are not interoperable, but they are expected to operate without causing any significant interference with each other.

The developed reading device has to perform exclusively with mode 1 and mode 2 of operation. Anyhow, there are a few constrictions defined for mode 2, which will be dwelt on in chapter 4.3.

Something all modes have in common is the wakeup-process of the VICC: The tag cannot respond unless it receives a valid command from the interrogator.

The initial dialogue between the VCD and the VICC (one or more VICCs may be present at the same time) is conduced through the following consecutive operations:

- activation of the VICC by the RF operating field of the VCD,
- the VICC waits silently for a command from the VCD,
- transmission of a command by the VCD,
- transmission of a response by the VICC.

At data interchange, frames are used for ease of synchronisation and independence of protocol. Frames shall be delimited by a start of frame (SOF) and an end of frame (EOF) and are implemented using code violation. Since the topic of framing is not an involved topic for the development of the analog part of the developed reading device, there will be no further focus on framing specifications.

The operating field generated by the VCD is limited both upwards and downwards: The minimum operating field H_{min} has a value of 150 mA/m (rms), the maximum operating field H_{max} has a value of 5 A/m (rms). A VICC shall operate as intended continuously between H_{min} and H_{max}.

The specifications provided in the following sections are according to [7] and [6].

4.2. Mode 1

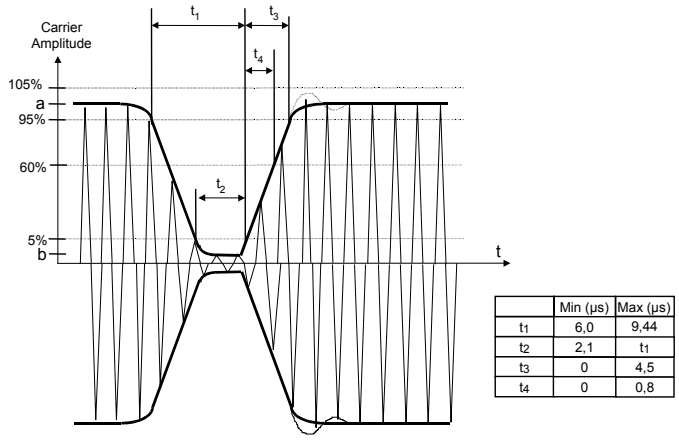
4.2.1. Data Transfer from VCD to VICC

Generally it is distinguished between the type of modulation and the coding of the data. From the different modes specified below, any data coding can be combined with any modulation process.

4.2.1.1. Modulation Process

The transmission of the data occurs by ASK (see chapter 3.2.1) of the carrier signal. There are two modulation indices possible: 10 % and 100 %. The VCD selects which index is used. Both modulation indices have to be supported by the VICC.

In the figures 4.1 and 4.2 the characteristics of each modulation index, which have to be observed by the reader, are illustrated.



	Min (µs)	Max (µs)
t_1	6,0	9,44
t_2	2,1	t_1
t_3	0	4,5
t_4	0	0,8

Figure 4.1.: Modulation of the carrier for 100 % ASK [6]

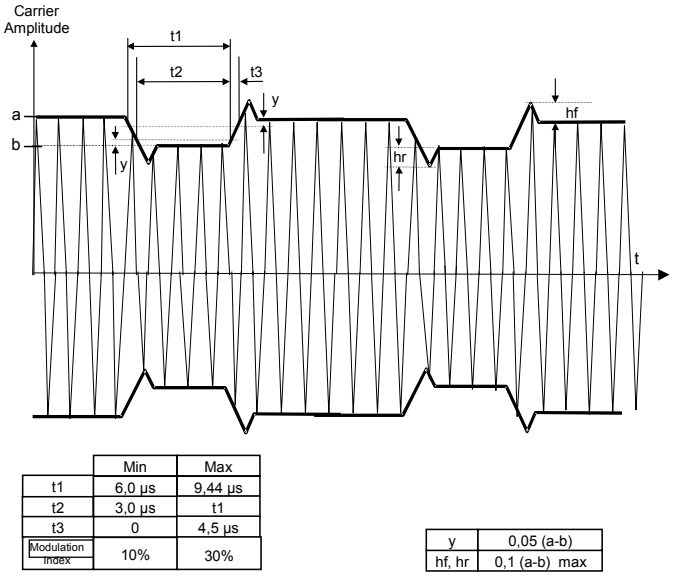


Figure 4.2.: Modulation of the carrier for 10 % ASK [6]

4.2.1.2. Data rate and Coding

The coding of the data is done by pulse position modulation. There are two coding modes provided: 1 out of 256 coding and 1 out of 4 coding. The VCD determines which coding type is used, the VICC has to be able to decode both.

1 out of 256 As shown in figure 4.3, the value of a single byte is communicated by the position of a single pause in a successive string of 256 time periods, where one period lasts

$$\frac{256}{f_c} = 18.88\,\mu s$$

In this case the resulting data rate is:

$$\frac{8 \cdot f_c}{256^2} = 1.65\,[\frac{kbits}{s}]$$

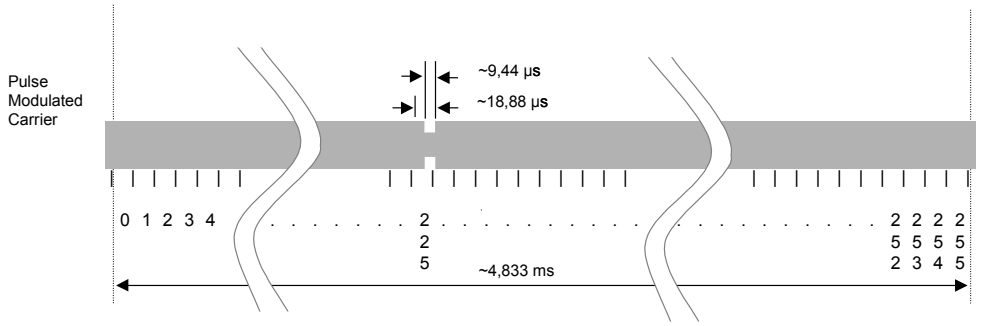


Figure 4.3.: 1 out of 256 coding mode [6]

1 out of 4 In this mode, the position of the pause in a 75.52 μs string ($1024/f_c$) determines two bits at a time (see figure 4.4). Hence there are four pairs of bits needed to form a byte.

The data rate obtained is:

$$\frac{2 \cdot f_c}{1024} = \frac{f_c}{512} = 26.48\,[\frac{kbits}{s}]$$

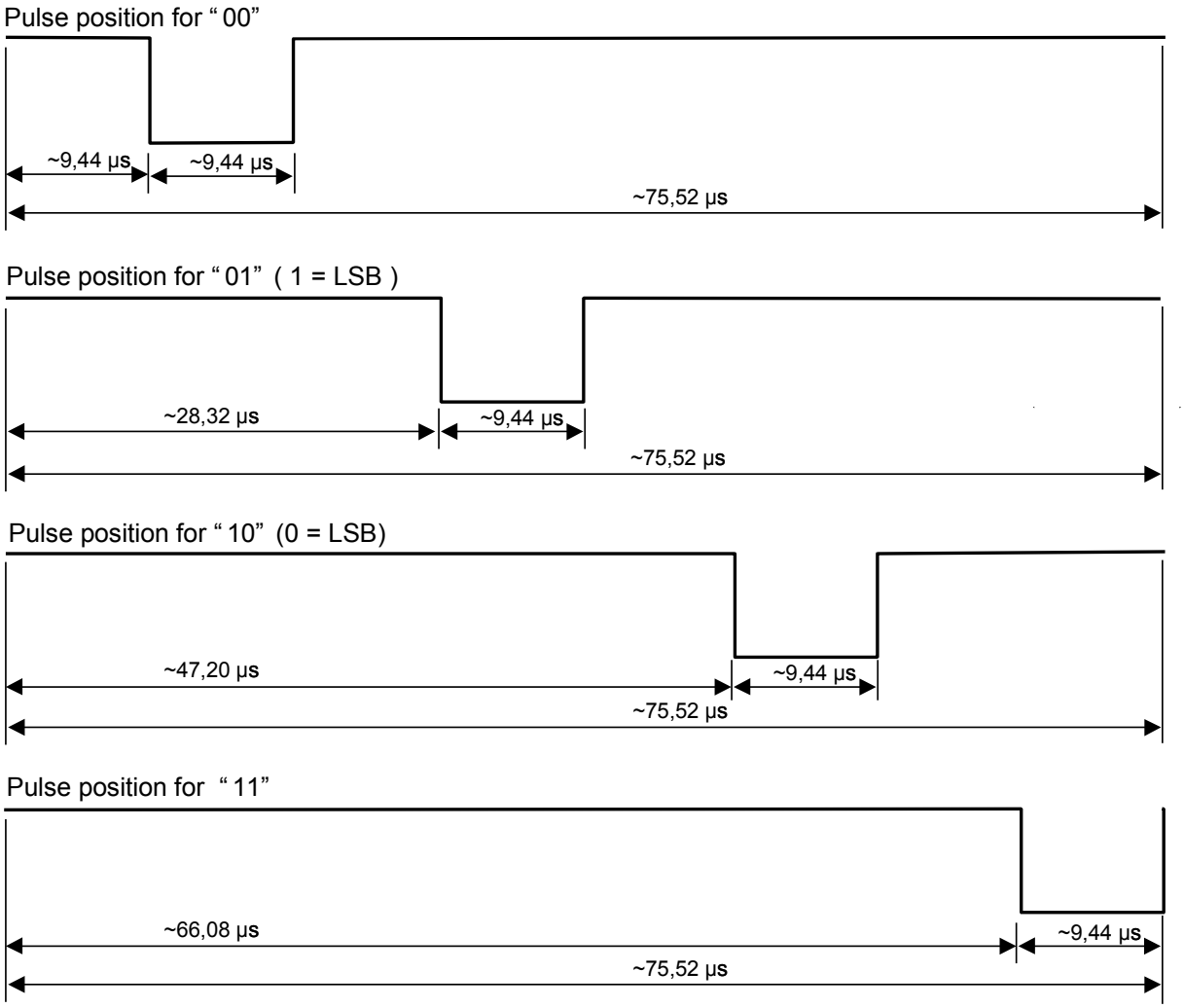


Figure 4.4.: 1 out of 4 coding mode [6]

4.2.2. Data Transfer from VICC to VCD

For some parameters there are several modes defined in order to allow the choice of the most convenient parameter depending on the noise environments and application requirements.

4.2.2.1. Modulation Process

The modulation is implemented by load modulation (see chapters 2.6 and 3.3). Therefor, the subcarrier frequency f_s is established in the VICC by the division of the carrier frequency f_c. In the ISO/IEC 18000-3 standard there are two modulation types defined: The data transmission using one and the transmission using two subcarriers.

If one subcarrier is used, the frequency f_{s1} of the subcarrier load modulation shall be $f_c/32$ (423.75 kHz). If two subcarriers are used, the frequency f_{s1} shall be $f_c/32$ (423.75 kHz), and the frequency f_{s2} shall be $f_c/28$ (484.28 kHz). The VCD decides whether the VICC uses one or two subcarriers.

Although the analog frontend design of the instant contactless desktop reading device would generally be able to demodulate both versions, it is soleley verified for the modulation with one subcarrier.

4.2.2.2. Data Rates and Coding

In the ISO/IEC 18000-3 standard there are a high and a low data rate specified. The VCD appoints which data rate is used. The VICC shall support the data rates shown in table 4.1.

Data Rate	Single Subcarrier	Dual Subcarrier
Low	6.62 kbits/s ($f_c/2048$)	6.67 kbits/s ($f_c/2032$)
High	26.48 kbits/s ($f_c/512$)	26.69 kbits/s ($f_c/508$)

Table 4.1.: Data rates [6]

For the encoding of the data, Manchester coding is used (see figures 4.5 to 4.8). All timings shown refer to the high data rate from the VICC to the VCD. For the low data rate the same subcarrier frequency is used, in this case the number of pulses and the timing shall be multiplied by 4.

If two subcarriers are used for data encoding, logic '0' (shown in figure 4.7) consists of 18.88 μs of the lower subcarrier frequency, followed by 18.58 μs of the higher frequency. In contrast, logic '1' (shown in figure 4.8) consists of 18.58 μs of the higher subcarrier frequency, followed by 18.88 μs of the lower frequency.

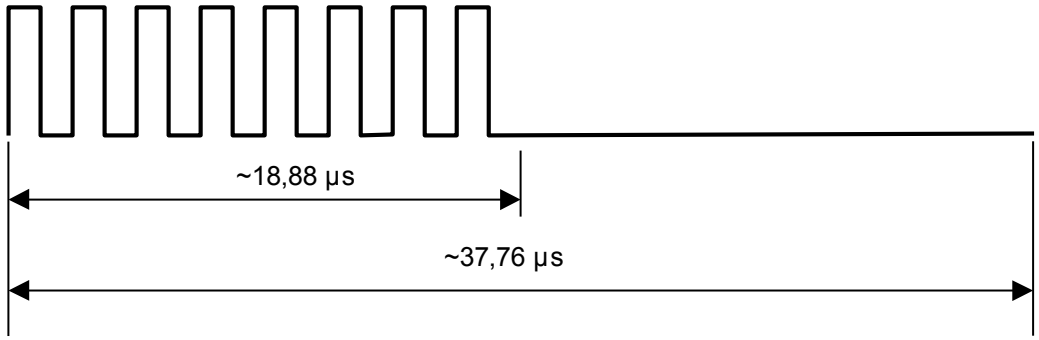


Figure 4.5.: One subcarrier - Logic 0 [6]

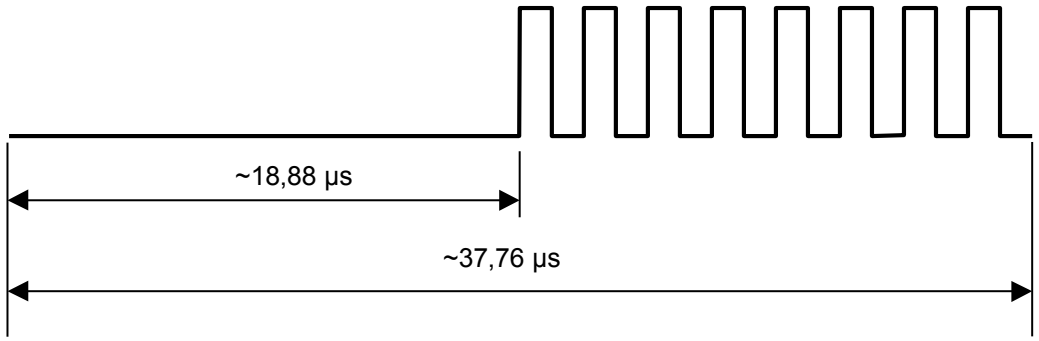


Figure 4.6.: One subcarrier - Logic 1 [6]

This thesis, in combination with the thesis of Selma Skoljic, deals only with the decoding of a single subcarrier signal, but an extension of this constraint can be implemented by software.

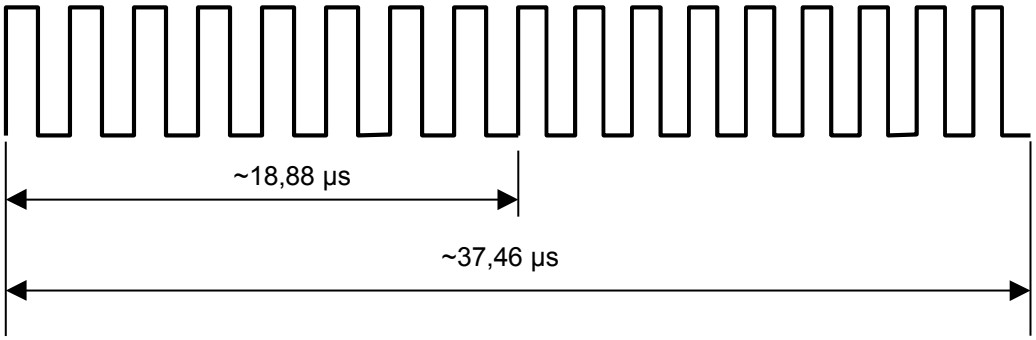


Figure 4.7.: Two subcarriers - Logic 0 [6]

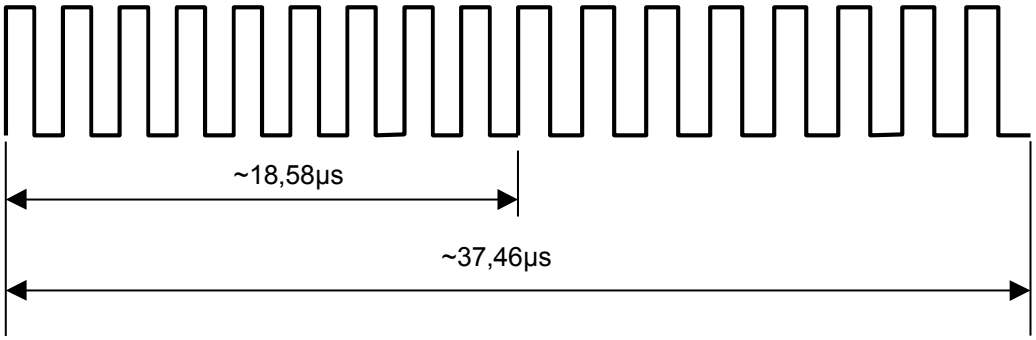


Figure 4.8.: Two subcarriers - Logic 1 [6]

4.3. Mode 2

4.3.1. Data Transfer from VCD to VICC

4.3.1.1. Modulation Process

The transmission of the data occurs by PJM (Phase Jitter Modulation) of the carrier signal. This modulation technique is enlarged on in chapter 3.2.3.

The time to complete an interrogator command phase transition is less than or equal to 1.18 μs, see figure 4.9.

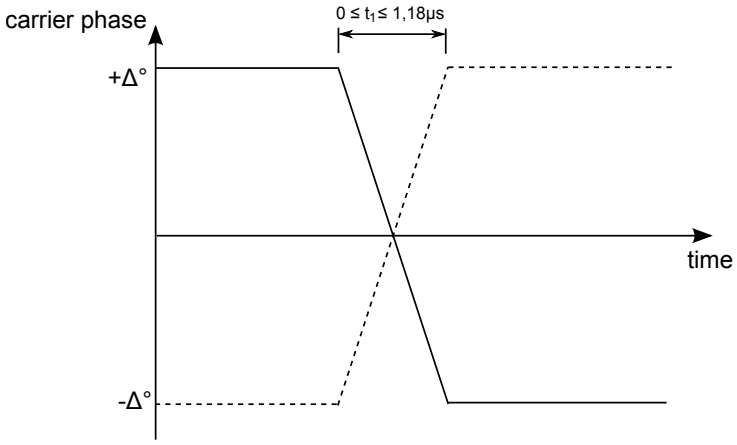


Figure 4.9.: Timing of the PJM Phase Shift [7]

4.3.1.2. Data Rate and Coding

The data rate of the encoded command is 423.75 kbit/s ($f_c/32$). Therefrom, the required period for the transmission of one bit is $32/f_c = 2.36\,\mu s$.

All commands are encoded using Modified Frequency Modulation (MFM) encoding rules. MFM has the lowest bandwidth occupancy of the binary encoding methods. The bit value is defined by a change in state. These encoding rules are defined as follows:

- A bit 1 is defined by a state change in the middle of a bit interval.
- A bit 0 is defined by a state change at the beginning of a bit interval.
- Where a bit 0 immediately follows a bit 1 there is no state change.

An example of command MFM encoding of the binary string 000100 is shown in figure 4.10.

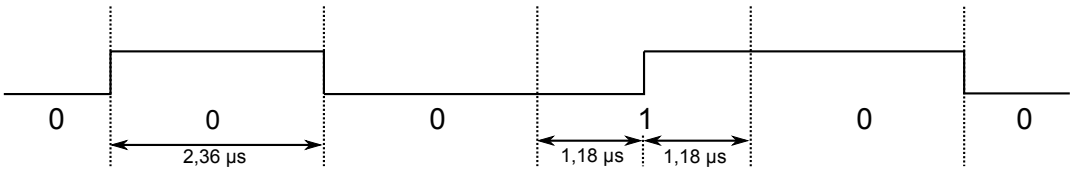


Figure 4.10.: Example to MFM encoding of the string 000100 (modified from [7])

4.3.2. Data Transfer from VICC to VCD

4.3.2.1. Modulation Process

The modulation of the tag replies is implemented by load modulation (see chapter 2.6). For its response, a tag uses one of the eight specified subcarrier channels. All of the channel frequencies are derived by division of the powering field's frequency. An overview of the available channels, their frequencies and division ratios is given in table 4.2.

Channel	Frequency [kHz]	Division Ratio
A	969	14
B	1233	11
C	1507	9
D	1808	7.5
E	2086	6.5
F	2465	5.5
G	2712	5
H	3013	4.5

Table 4.2.: Channel frequencies [6]

The scope of the instant thesis is limited to a VICC's reply on channel B. The intention was to design an analogue receiving path which can also be used to demodulate all the other channels just by doing some slight adoptions (adjustment of the filters).

The encoded data is modulated on the subcarrier as BPSK modulation.

4.3.2.2. Data Rate and Coding

The encoded reply data rate is independent of the reply channel and amounts to 105.9375 kbit/s ($f_c/128$). Therefrom, the required period for the transmission of one bit is $128/f_c = 9.4395\,\mu s$.

Replies are encoded using MFM (see figure 4.11) and modulated onto the subcarrier of the particular channel as BPSK. In contrast to the VICCs response in Mode 1, by this modulation the subcarrier is never turned off during data transmission.

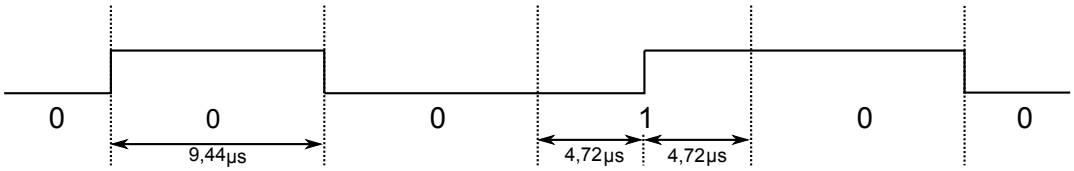


Figure 4.11.: Example to MFM encoding and timing of the string 000100 (modified from [7])

Chapter 5

Carrier-Suppressing Pick-Up Coil (CSPC)

As expressed in chapter 2.3, the instant thesis deals with halfduplex systems, which means that the VICC transmits the data to the VCD whilst the supplying 13.56 MHz RF-field is kept online. Typically, the VICC's response will be received by the VCD through the same antenna whereby the RF-field is emitted. Thus, the little response signal will be overlaid by the comparatively huge supply signal.

To demodulate the VICC's signal it is first of all necessary to separate it from the carrier signal. As already stated in [14], for the demodulation of a VICC's signal, a maximised signal-to-carrier ratio (SCR) is beneficial. With the objective of easing the demodulation of the response signal, Infineon Technologies Austria has developed a reader antenna that is suppressing the carrier signal and therefor increasing the SCR. This antenna is called *Carrier-Suppressing Pick-Up Coil* (CSPC).

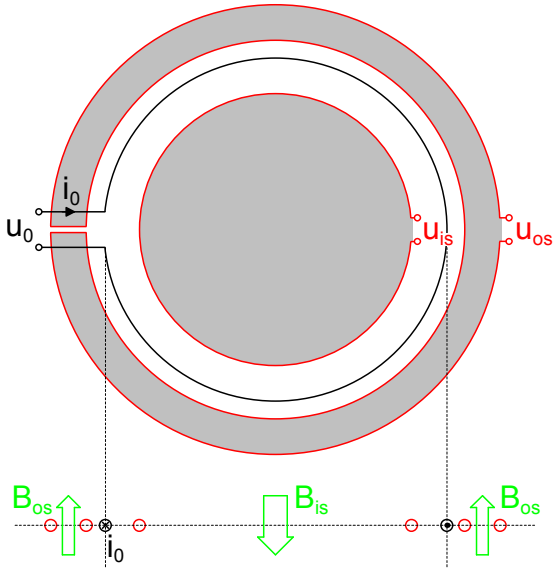


Figure 5.1.: Schematic view of the CSPC [14]

Figure 5.1 shows the CSPC's functionality. The black coil is the field generating coil. This coil is encircled by two additional coplanar aligned coils, one internal and one external. They are dimensioned and placed so that the parts of the magnetic field interfusing them are equal according to amount. The sense in which the inner coil is interfused by the reader's magnetic

field is directly opposed aligned to the interfusing of the outer coil. From this it follows that if the two coils are interfused by the same flux density B and have the same size, the voltages induced in the two coils are equal but have the same size:

$$B_{is} = B_{os} \wedge A_{is} = A_{os} \qquad \Rightarrow \qquad u_{is}(B_{is}, A_{is}) = -u_{os}(B_{os}, A_{os}) \tag{5.1}$$

In order to cancel out the voltage induced by the reader's magnetic field, the inner and the outer coil are connected serially, which means that the two voltages u_{is} and u_{os} are summed up. If there is no transponder in the response area of the VCD, due to their opposed signs but equality according to amount the summation of the two voltages equals zero.

If a transponder is located within the reader's field, a coupling between the antennas occurs: On the one hand a voltage is induced in the transponder's coil (and therefor a current flows in it), and on the other hand a flowing current in the transponder's coil is causing a magnetic field which is counteracting the magnetic field generated by the reader (see figure 5.2). In this case, the magnetic field around the reader's coil is not balanced any more, and the flux density between the inner and the outer coil differs. The voltages induced in both coils do not cancel out.

This is the effect on which the carrier-suppressing functionality of the CSPC is based: If the transponder is ideally placed so that its response only influences the flux through the inner coil, the voltages induced in both CSPC coils by the reader's field still cancel out, but the voltage induced by the transponder's magnetic field is causing an additional voltage induced in the inner coil, which will not be canceled out by the summation. Therefore the voltage at the CSPC's terminals is proportional to the current flowing in the transponder's antenna.

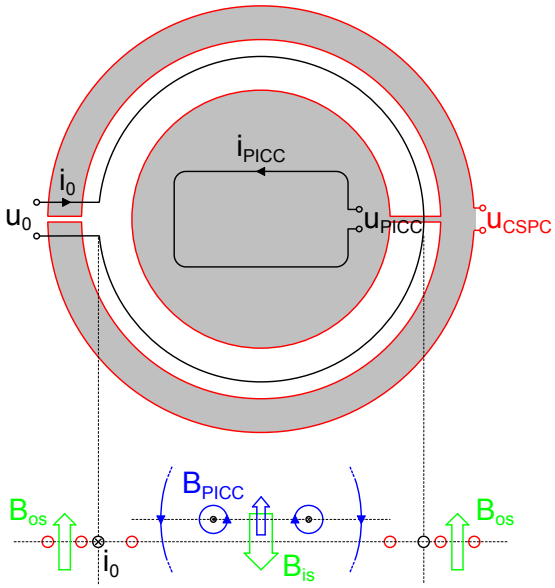


Figure 5.2.: CSPC with transponder [14]

Concerning the CSPS's equivalent circuit it can be seen that it generally consists of two serially connected inductors. If there is a transponder located within the reader's field, the transponder's influence will be considered as another transformed impedance.

In figure 5.3 the equivalent circuit of the CSPC's loaded and unloaded state is shown. Mathematically they are describable by

$$u_{CSPC,unloaded} = u_{is,r} + u_{os,r} \tag{5.2}$$

when there is no transponder loading the reader's magnetic field, and by

$$u_{CSPC,loaded} = u_{is,r} + u_T + u_{os,r} \tag{5.3}$$

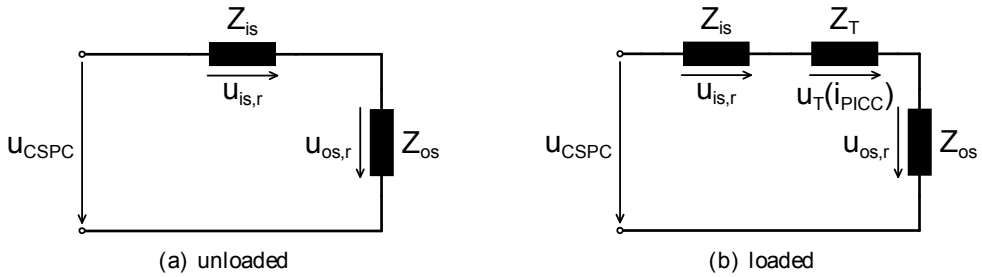


Figure 5.3.: CSPCs equivalent circuit (r indicates that these voltages are induced by the readers magnetic field) [14]

when a transponder is located directly above the CSPC's inner coil. If the condition formulated in equation 5.1 is valid, equation 5.2 shows that the CSPC's voltage equals zero in absence of a transponder, whereas equation 5.3 indicates the proportionality of u_{CSPC} to the current flowing in the transponder's coil, if a transponder is located within the reader's magnetic field.

Figure 5.4 shows the coupling situation between the three antennas (VICC's antenna, VCD's transmitting and CSPC receiving aerial). To achieve a high SCR, the coefficient of coupling between the VCD's sending antenna and the VCD's receiving antenna has to be minimised. In the ideal case it aspires to zero.

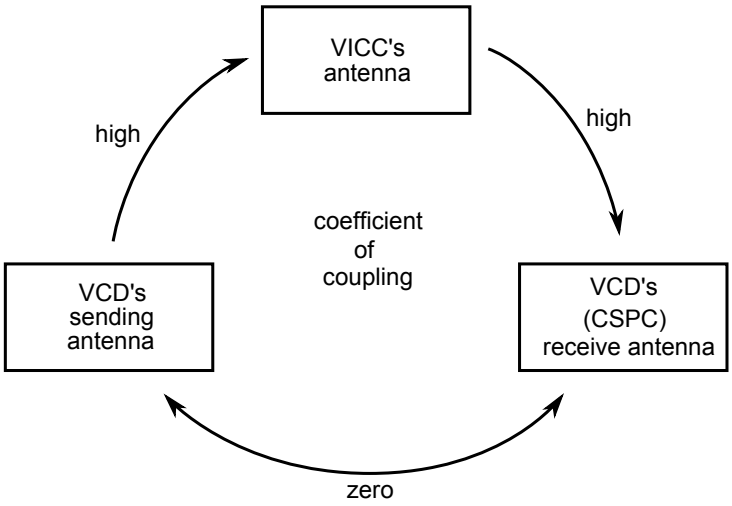


Figure 5.4.: Coefficients of coupling by the use of a CSPC antenna

For the implementation of the reading device within the scope of the instant thesis, a CSPC is used due to the benefits gained for the SCR.

Chapter 6

Realisation of the Reading Device

6.1. Miscellaneous

For the realisation of the reading device there were some basic conditions which had to be followed. On the one hand, there were the demands specified in the ISO/IEC 18000-3. As described in chapter 4, timings, signal characteristics, different modulation types and field strength parameters were claimed. On the other hand, the requirement of an economical implementation of the developed reader was pointed out by the employer.

The supply concept of the reader is based on the USB 2.0 standard. The developed desktop reader shall be powered exclusively through an USB connection to the controlling computer, so the design is restricted to a voltage supply of 0 V to 5 V with a maximum current consumption of 500 mA. The circuit board developed within this thesis is integrated in the digital environment of the Cortex-M3 evaluation board, which provides the developed board with three supply signals: 0 V, 3.3 V and 5 V. The 3.3 V supply is used to drive the digital parts of the board, the 5 V supply drives the analog circuitry including the operational amplifiers. Internally, a 2.5 V supply is generated to deliver a symmetrical ground level (between 0 V and 5 V) for the analog circuits.

The first prototype of the reading devices' receive path was done using a block concept dividing the overall product in smaller blocks which then were integrated by using connector strips with a defined pin assignment. This guaranteed an easy exchangeability of the different blocks and improved the testability of the block concept approaches within the whole systems.

As you can see in figure 6.1, the pins are aligned in the way that the strip is adjusted symmetrically around its center. The advantage of this configuration is the possibility of flipping one block without changing anything except the swap between the I- and the Q- channel of the device.

Figure 6.1.: Frame connector of the demodulation path prototype

The I-channel and the Q-channel pin hold the analogue I and Q data, whose signal shapes differ during the signal processing procedure depending on the demodulation stage respectively on the current evaluation block the actual connector belongs to. The I-select and Q-select pins are used for the signal processing of the channel desision, while the Channel pin represents the output of the channel decision circuitry.

The disadvantage of this block concept was the arising of disproportional long wired distances which evoked reflections and electromagnetic interferences between the lines. This necessitated

the early integration of the system onto one circuit board. The schematics of this board can be found in appendix A.

Figure 6.2 shows the developed RFID system. This system includes, as already mentioned in figure 2.2, an application (running on a PC), an RFID reading device (consisting of a digital (Cortex-M3) and an analog circuit board), coupling elements (antennas) and one or more transponder.

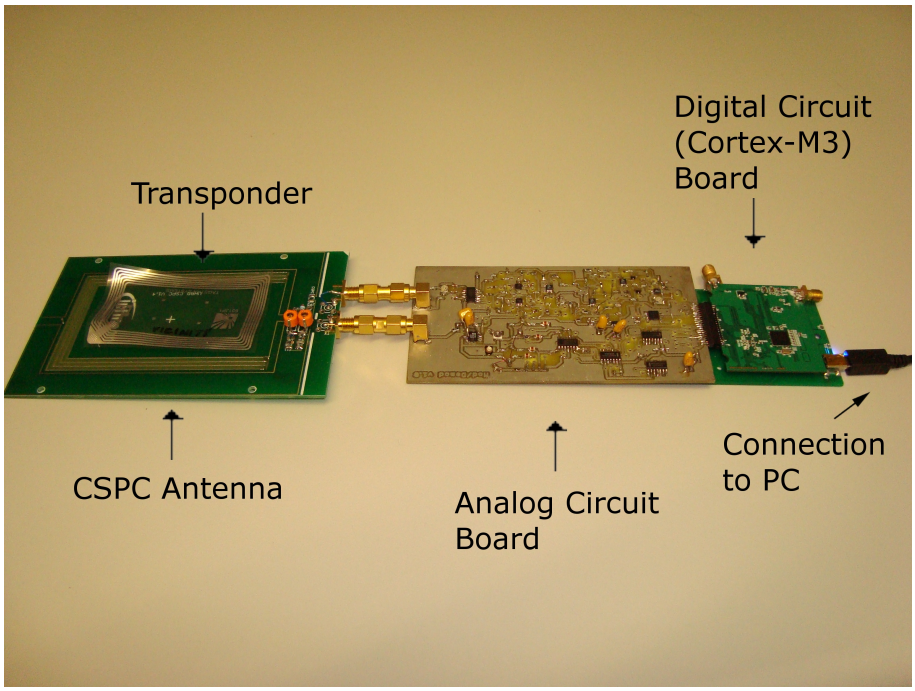


Figure 6.2.: Developed RFID System

The interface between the digital environment of the Cortex-M3 board and the board developed in the instant thesis is shown in figure 6.3. As you can see, the power supply of 5 V, 3.3 V and GND is provided by the Cortex-M3 board, as well as the carrier signal of 13.56 MHz and the frequency-doubled carrier signal of 27.12 MHz. The data for the commands are gained via the pin *SPI_MOSI* and the demodulated responses are returned via the pin *SPI_MISO*. There are pins reserved for the choice of the used mode and for the control of the multiplexer in the receive path. For the exact pinning please refer to appendix A.

The modulation scheme divides the system into the modulation/demodulation of the data on the subcarrier and the modulation/demodulation on the carrier. Data transmission only requires the data coding in the microcontroller, no additional subcarrier modulation is needed. The modulation on the carrier occurs in the analog part of the reader. For the received data the carrier demodulation is done in the analogue part, while the demodulation of the subcarrier and the decoding is carried out in the microcontroller.

As already mentioned, the schematic data for circuit board assembling can be found in appendix A. On this board, the whole transmit path (for mode 1 and mode 2) and the receive path for mode 1 are integrated. Due to time reasons, mode 2 is treated rather theoretically and not practically proven.

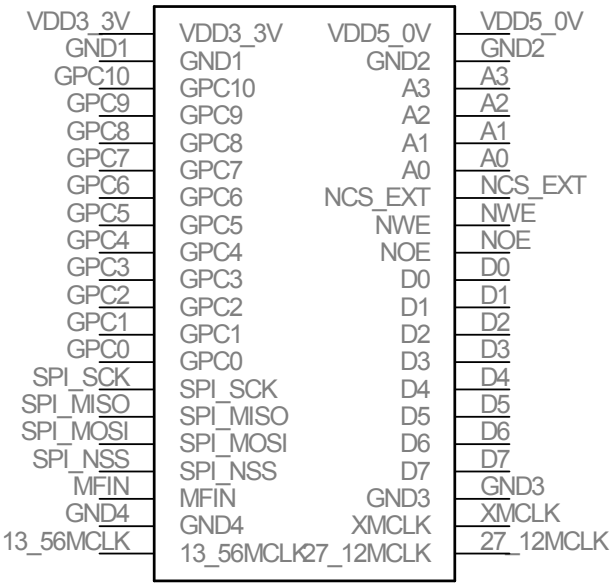


Figure 6.3.: Pinning of the interface between the Cortex-M3 board and the new developed circuit board

6.2. Transmit-Path

Two requirements for the transmit path are an applicable concept and the selection of a proper output driver. The driver has to deliver the highest possible output currents (but without disappearing of the maximum allowed field strength from the sight). Furthermore it has to be fast enough to deliver neat signals also for frequencies at about 13.56 MHz, preferably independent from the external load (the attached antenna). Coinstantaneous, the adjusted modulation index shall remain stable, also independent from the external load. Besides that, the ouput driver, respectively the output driver concept, shall be construed as a low-budget solution.

Another important item for the functionality of the modulator is the switching between a 10 %/100 % modulation for mode 1 and the phase jitter modulation for mode 2. This switching shall be done by software. There were two ideas of how to realise the switchability between the different modes. The first one was to pull out three signals from the microcontroller from the reader's digital part - in each case with the coded data for one appointed modulation type. In this case, each data line would operate the appropried driver, so that only one data line could be active at the same time. However, a limiting fact was that the MOSI (Master Out Slave In) pin from the microcontrollers SPI-Interface was chosen as the output pin for transmitting the data to the modulator. This was because that pin provides the possibility to just write the transmitted data to a buffer, even byte-by-byte, which are then autonomously and sequentially transmitted. In comparison to that, a conventional output pin depicts only a signal output for bit-by-bit transmission, which is much more complicated to realise. Since there exists only one single MOSI pin at the SPI-Interface, we were forced to launch the second alternative described hereafter. For this, we use two signal lines leading through the microcontroller to select the desired modulation type, which can then be encoded to identify which modulation type is meant. The denotation of these two signals is specified in table 6.1.

These two signals may be sent through a slow output pin, because they will not be toggled during the whole communication procedure. The fast SPI-output can now be used to send the transmitted data to the carrier modulation appliance.

Special attention was paid to the compatibility of the logic voltage levels between the microcontroller's output and the logic input of the reader's analog part. Since the 'High'-Level of the

PJM signal	90 % signal	Modulation Type Selected
0 V	0 V	100 % modulation
0 V	3.3 V	10 % modulation
3.3 V	0 V	phase jitter modulation
3.3 V	3.3 V	forbidden state

Table 6.1.: Signals for modulation type control and their signification

microcontroller's output is represented by 3.3 V, a logic series had to be elected which especially supports these low voltage levels and detects the correct logic level. Because of this feature, the logic series 74LVC was chosen.

6.2.1. Concept

Due to the demand of modulation index steadiness, the decision was made for using an operational amplifier actuated in the inverting amplification mode. The advantage of this configuration is the intrinsic regulation of the modulation index independent from the external load. For the driving device itself, the operational amplifier AD8017AR from Analog Devices was chosen after several tests.

Figure 6.4 shows a primary block diagram of the modulation unit. Ranked first there is the already discussed decoder for the channel selection. The result of this decoding procedure then has to be linked with the data obtained by the fast SPI interface. For example, if a 100 % modulation is appointed, no data signal will be guided through to the PJM modulator/driver. In this step, the data signal is broken up into distinct branches, depending on the requirements of the summing unit at the end of the signal processing sector.

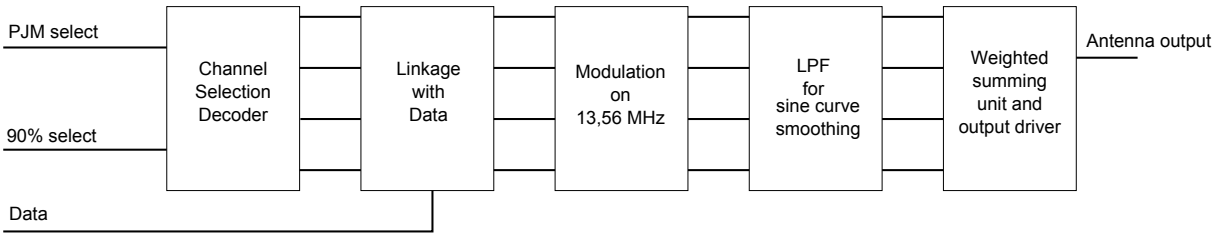


Figure 6.4.: Block diagram of the modulator concept

The next step is a data modulation on the carrier frequency f_c. Since the output signal of this modulation is still a rectangle, the necessity of signal rounding arises to gain a sinusoidal characteristic. In this case this is done by a second order lowpassfilter. Finally, we will need some kind of summing/driver unit to merge the signals for 10 %/100 % modulation and output the resulting signal to the antenna.

Before immersing in the individual circuitry blocks of the reader, the cooperation of the blocks shall be described in a rough overview. Starting from the mode choice signals PJMselect and 90 %select sent by the microcontroller, the incoming baseband signal is split up into four signal branches - with the aim of fusing them in the summing unit at the end of the signal branches, straight before driving the antenna by the passband signal. The construction of the particular signal branches is shown in figure 6.5.

As you can see, the four generated baseband signals are used to switch the particular 13.56 MHz clocked signal branches on or off. The branches are handled differently, depending on their function. To get an adequate modulated output signal it takes the combination of at least two coupled branches.

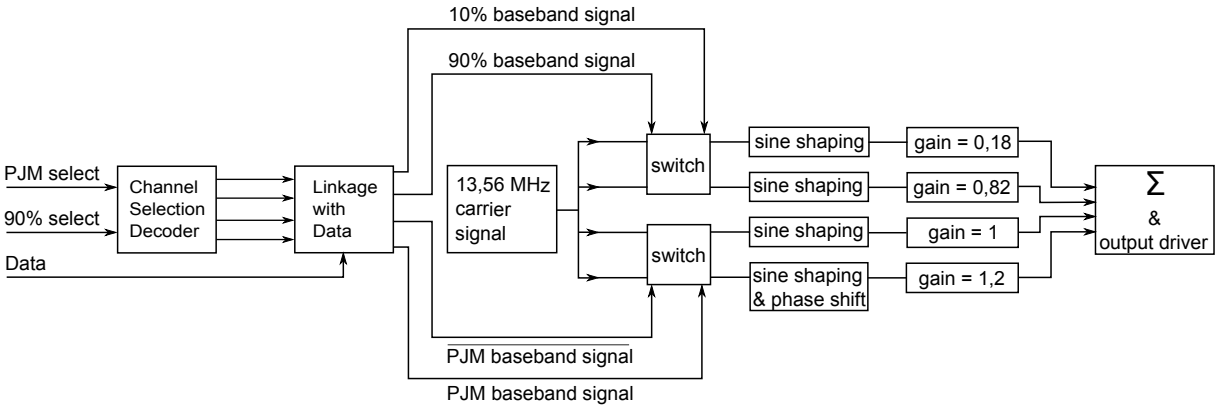


Figure 6.5.: Modulator concept in detail

For a 100 % modulation, the first two signal branches are switched on and off synchronously corresponding to the data cycles. In this case, the output signal amounts to an either 13.56 MHz signal with the amplitude of 100 % or a 13.56 MHz signal with the amplitude 0. For a 10 % modulation, the second path is statically enabled, while the first path (less amplified than the second path) is switched on and off in the cycle of the data. Both signals are in-phase signals, so when they are summed up there is a 13.56 MHz signal formed with an amplitude varying between the full signal amplitude and 82 % of the full amplitude, which accords to a modulation index of $m = \frac{100-82}{100+82} = 10\,\%$.

For the creation of a PJM signal there exist two branches. The first branch is a 13.56 MHz in-phase signal, while the second branch is a phase-shifted 13.56 MHz signal with the phase shift of about four degrees. These two signals are alternately switched on, again depending on the data cycle. The overall output is a 13.56 MHz signal which switches between the full amplitude and a phase of 0° and the full amplitude and a phase of about 4°. The reason for the output amplitude being equal in both switching cases despite different gain factors in the branches will become ever more clear after discussing chapter 6.2.2.4.

6.2.2. Realisation

6.2.2.1. Channel Selection Decoder and Linkage with Data

The inputs of the channel selection decoder are the two mode choice signals received from the microcontroller (*PJM_SIG* via *GPC5* ('PJM select') and *90_SIG* via *GPC4* ('90 % select')). These two signals are logically decoded to detect the used mode and, in combination with the data signal gained from the microcontroller (*DATA_CMD* via *SPI_MOSI*), used to activate the adequate signal branches at the right times. By the truth table below (table 6.2), the development of the designed combinatorial circuit can be retraced.

		branch			
PJM select	**90 % select**	**1**	**2**	**3**	**4**
0	0	Data	Data	0	0
0	1	Data	1	0	0
1	0	0	0	Data	$\overline{\text{Data}}$
1	1	X	X	X	X

Table 6.2.: Truth table for channel selection decoding

As you can see, for a 100 % modulation in mode 1 the first two signal branches are enabled if the input signal on the 'Data' line equals '1'. Otherwise, all signal branches are disabled. For a 90 % modulation in mode 1, the second signal branch is statically enabled, while the first signal branch's state depents on 'Data'.

If the 'PJM select' signal is received as being '1', the first two signal branches will be disabled and the third and fourth signal branch will alternately be activated or deactivated, depending on the state of the data input. Therefore, branch three and four will never be enabled concurrently.

The 'X' in the table means that the state of the output is indifferent. This is, because the state '1' for both input select signals 'PJM select' and '90 % select' is defined as a forbidden state and will never occur on the output of the microcontroller. For ease of the selection decoding circuit testabilit, the outputs of this state are defined as being equal to the outputs of the selected PJM mode.

After in table 6.2 the 'Data' signal behaves equally to a variable, we can reclassify it as an input signal and combine it logically with the channel select inputs. This leads us to table 6.3. In this table, the case 'PJM select' = '90 % select' = '1' is also considered, which equals the case 'PJM select' = '1' and '90 % select' = '0'.

			branch			
PJM select	**90 % select**	**Data**	**1**	**2**	**3**	**4**
0	0	0	0	0	0	0
0	0	1	1	1	0	0
0	1	0	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	0	0	1
1	1	1	0	0	1	0

Table 6.3.: Truth table for channel selection decoding

Representative for all four signal branches, in figure 6.6 you can find an example of logic simplification by Karnaugh map done for branch 2. The two arbitrarily chosen values for the last two lines in table 6.3 are yet entered by two X, they will be discussed afterwards in further detail.

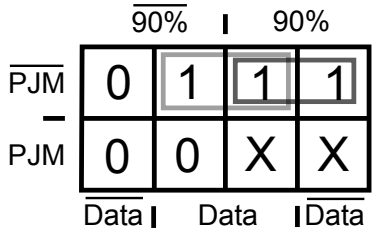


Figure 6.6.: Karnaugh map for signal branch 2

If the two X are replaced by the values charted in 6.3, we can find two block pairs. In the form of logic terms these blocks can be expressed as

$$\begin{aligned} Branch2 &= \overline{PJM} \cdot Data + 90\,\% \cdot \overline{PJM} \\ &= \overline{PJM} \cdot (Data + 90\,\%) \end{aligned} \tag{6.1}$$

which results in the need of one 'and' and one 'or' gate. Alternatively, it is possible to fill the two X by the value '1'. In this case we can find one pair and one quadruple block, which leads us to the formula

$$Branch2 = 90\,\% + Data \cdot \overline{PJM} \tag{6.2}$$

For the realisation of this expression there is one 'or' and one 'and' gate necessary. As you can see, this simplification does not bring any reduction of gates along, so we can agree to the values in table 6.3 for branch 2.

This procedure can be repeated for the other tree branches as well. This leads us to the resulting combinatorial circuit shown in figure 6.7.

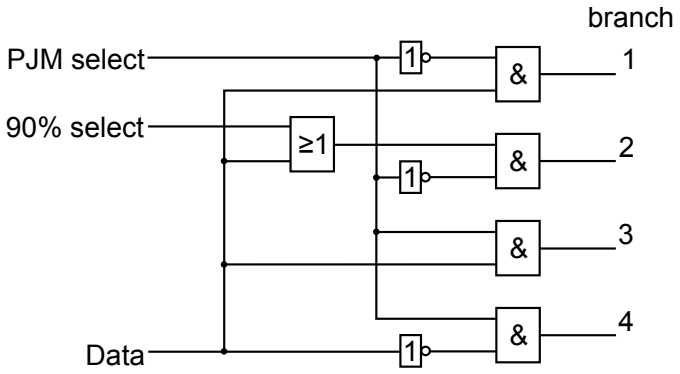


Figure 6.7.: Channel decoder and linkage with data - combinatorial circuit

6.2.2.2. 13.56 MHz Oscillator

The information for this chapter is extracted from [4], [16] and [3].

For the first hardware prototype of the transmit path, the source of the 13.56 MHz signal could be chosen by a jumper between an internal 13.56 MHz oscillator and an external 13.56 MHz source. In the modulation unit schematic enclosed in appendix A, this oscillator is no longer integrated, because in this state the clock signal has already been gained by the attached Cortex-M3 board as mentioned in 6.1. Nevertheless, for the sake of completeness the design of the 13.56 MHz oscillator is explained in this chapter.

For the internal oscillator of the prototype, a 13.56 MHz crystal of the ABM3 series from Abracon (ABM3-13.560MHZ-B2-T) was used and connected as a Pierce circuitry (see figure 6.8). The two inverters were in this case realised by 74LVC04AD gates. The resistor R_{GK} was needed to linearise the gate between the input and the output and adjusts the DC operating point at the input. The value of R_{GK} was uncritical and depended on the used logic family (see table 6.4). Randomly, for this project the value of 1 MΩ was chosen for R_{GK}.

logic family	**TTL**	**(A)LS TTL**	**S-TTL**	**AS-TTL**	**(H,A) CMOS**
R_{GK} (ω)	390...2.2 k	680...4.7 k	270...1 k	560...3.3 k	100k...22 M
typ. R_{GK} (ω)	1k	2.2 k	680	1.5 k	10 M

Table 6.4.: R_{GK} value depending on the logic family [4]

To calculate the capacities C_{X1} and C_{X2}, the load capacity of the crystal and the input and output capacities of the 'not' gates had to be known. These values could be read from the datasheets. C_L of the crystal amounted to 18 pF. The input (C_i) and output (C_o) capacities of the gate were 5 pF. The load capacitance could be calculated according to [4] by

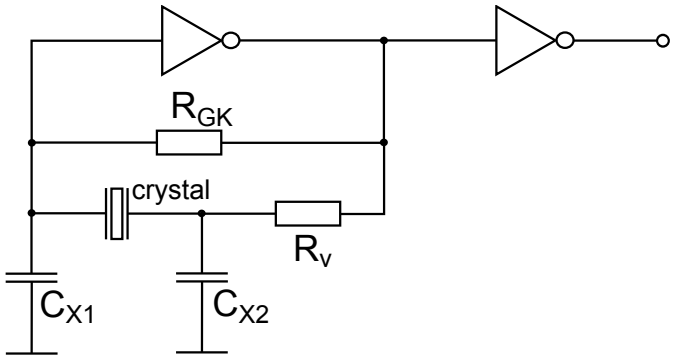


Figure 6.8.: Pierce circuitry for assembly of the 13.56 MHz clock (modified from [4])

$$C_L = \frac{C_{X1}' \cdot C_{X2}'}{C_{X1}' + C_{X2}'} \tag{6.3}$$

with

$$\begin{aligned} C_{X1}' &= C_{X1} + C_i \qquad \text{and} \\ C_{X2}' &= C_{X2} + C_o \end{aligned} \tag{6.4}$$

The relation between C_{X1}' and C_{X2}' was given by

$$C_{X2}' = (1...2) \cdot C_{X1}' \tag{6.5}$$

Generally, C_{X1}' and C_{X2}' might be of the same value, but choosing C_{X1}' a bit smaller than C_{X2}' eased oscillation build-up. Based on the formulas 6.3 to 6.5, the value calculated for C_{X1} was 27 pF and the value for C_{X2} equaled 33 pF.

The resistor R_V was used to adjust the PI-element (consisting of C_{X1}, C_{X2} and the crystal) to the oscillation level (fundamental or 3rd overtone) to eliminate unwanted harmonics. Together with C_{X2}, R_V formed a lowpass filter. For a given C_{X2}, R_V was dimensioned the way that the lowpass filter's cut-off frequency was arranged between the fundamental frequency f_0 of the crystal an its third harmonic (see equations 6.6 and 6.7).

$$f_T = 2 \cdot f_0 \tag{6.6}$$

$$R_V = \frac{1}{2 \cdot \pi \cdot f_T \cdot C_{X2}} \tag{6.7}$$

Above the frequency of 4 MHz there is, according to literature, no serial resistance necessary. However, experiments have shown that the duty cycle has been significantly improved by inserting the serial resistance anyway. For the frequency of 13.56 MHz and a C_{X2} of 33pF, the calculated resistance value was 1.77 kΩ. In the designed circuit, a resistor of 1.6 kΩ was inserted.

6.2.2.3. Switching of the 13.56 MHz signal

In the next step, the 13.56 MHz signal has to be switched by the signals created in chapter 6.2.2.1. This is done by using a switchable buffer. One important feature of this buffer is that the outputs are set to tristate when the buffer is disabled.

For this application, the 74LVC126AD module was selected. There are four buffer gates needed - one for each signal branch. The circuit arrangement can be seen in figure 6.9.

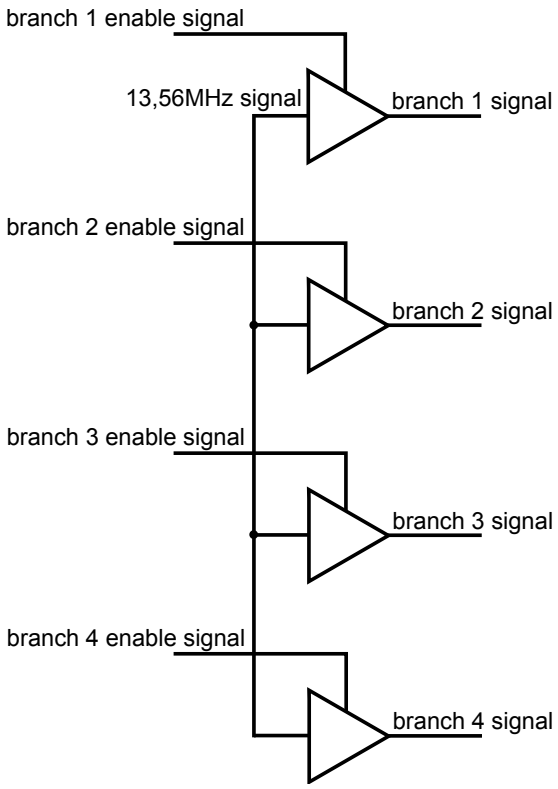


Figure 6.9.: Linkage between the carrier signal and the data signals

6.2.2.4. Lowpassfilter for Sine Curve Smoothing

Up to this point, all the signals were processed digitally and therefore are rectangular signals in the time domain. But to create ideal emitting conditions, we have to form sine shaped signals from it.

As generally known, a rectangular time signal can be integrated to generate a delta signal. One further integration of this delta signal delivers a sine shaped signal. This procedure accords to a double integration of the rectangular input signal. In analogue signal processing a double signal integration can be implemented by the use of a second order lowpass filter, if it its resonance frequency is in the range of the input signal's frequency. Precondition for a successful integration straight from the first signal period is an inexistent constant component of the input signal. Otherwise, if the capacity of the lowpass filter is uncharged, there will have to be faced transient effects until a symmetrical output signal is delivered.

For the realisation of the lowpassfilter, a passive RLC-oscillator was elected because of its economies compared to an active filter. Besides, it is not easy to find a low priced operational amplifier for higher frequencies like 13.56 MHz to realise an active filter.

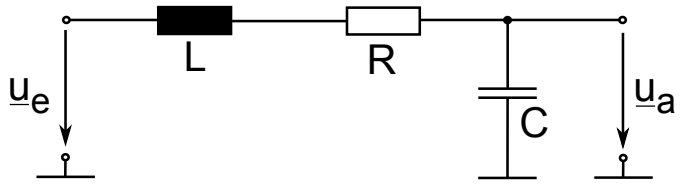


Figure 6.10.: Realisation of a passive second order lowpass filter

The transfer function of this circuit can be calculated by equation 6.8.

$$\begin{aligned}\underline{H}(s) &= \frac{\underline{u_a}(s)}{\underline{u_e}(s)} = \\ &= \frac{\frac{1}{sC}}{R + \frac{1}{sC} + sL} = \\ &= \frac{1}{1 + sRC + s^2LC}\end{aligned} \tag{6.8}$$

The expression in 6.8 would be for a pure stationary signal

$$\begin{aligned}\underline{H}(j\omega) &= \frac{1}{1 + j\omega RC - \omega^2 LC} = \\ &= \frac{1}{(1 - \omega^2 LC) + j\omega RC} \cdot \frac{(1 - \omega^2 LC) - j\omega RC}{(1 - \omega^2 LC) - j\omega RC} = \\ &= \frac{1 - \omega^2 LC}{(1 - 2\omega^2 LC + \omega^4 L^2 C^2) + \omega^2 R^2 C^2} - j \cdot \frac{\omega RC}{(1 - 2\omega^2 LC + \omega^4 L^2 C^2) + \omega^2 R^2 C^2}\end{aligned} \tag{6.9}$$

After partitioning the transfer function into a real and an imaginary part, the phase between the input and the output signal (equation 6.10) and the amplification (equation 6.11) can be calculated.

$$\begin{aligned}tan(\varphi) &= \frac{\text{Im}\,\{\underline{H}(j\omega)\}}{\text{Re}\,\{\underline{H}(j\omega)\}} = \\ &= -\frac{\omega RC}{1 - \omega^2 LC} \\ \Rightarrow \varphi &= \arctan(-\frac{\omega RC}{1 - \omega^2 LC})\end{aligned} \tag{6.10}$$

$$\begin{aligned}|\underline{H}(j\omega)| &= \sqrt{\text{Im}\,\{\underline{H}(j\omega)\}^2 + \text{Re}\,\{\underline{H}(j\omega)\}^2} \\ &= \sqrt{\frac{(1 - \omega^2 LC)^2 + (\omega RC)^2}{(1 - 2\omega^2 LC + \omega^4 L^2 C^2 + \omega^2 R^2 C^2)^2}} \\ &= \frac{1}{\sqrt{1 - 2\omega^2 LC + \omega^4 L^2 C^2 + \omega^2 R^2 C^2}}\end{aligned} \tag{6.11}$$

The lowpass effect can be demonstrated for equation 6.11 by evaluating it for the following limit values of ω :

$$\begin{aligned}\omega \to 0 &: |\underline{H}(j\omega)| \to 1 \\ \omega \to \infty &: |\underline{H}(j\omega)| \to 0\end{aligned} \tag{6.12}$$

The cut-off frequency is the frequency for which the relation between the output and the input voltage becomes $\frac{1}{\sqrt{2}}$ respectively the gain becomes -3 dB. For equation 6.11, the cut-off frequency can be calculated by equation 6.13.

$$|\underline{H}(j\omega_c)| = \frac{1}{\sqrt{2}}$$

$$\Rightarrow \omega_c = \frac{\sqrt{\frac{\sqrt{C^2R^4-4CLR^2+8L^2}}{C} - R^2 + \frac{2L}{C}}}{\sqrt{2}L} \tag{6.13}$$

In our case, the cut-off frequency shall be 13.56 MHz, which accords to an angular frequency $\omega = 2\pi 13.56\,\text{MHz} = 85.2{\cdot}10^6$. An inductance of L=820 nH and a resistor of R=100 Ω are chosen. For these values, the required capacity can be determined. By inserting the given values into equation 6.13, a capacity of C=166 pF is evaluated, which comes as close as possible to the E12 standard value of 180 pF.

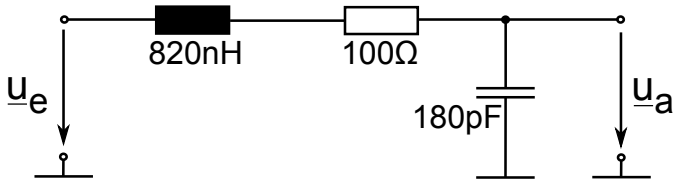


Figure 6.11.: Lowpass filter with a resonance frequency of about 13.56 MHz

Applying this filter to the buffer outputs, a smoothing of the signal waveform will be obtained which converts the rectangular shaped signals into sine shaped signals. In figure 6.12, the 90 degree phase shift and the attenuation of the amplitude for a 13.56 MHz input signal become obvious.

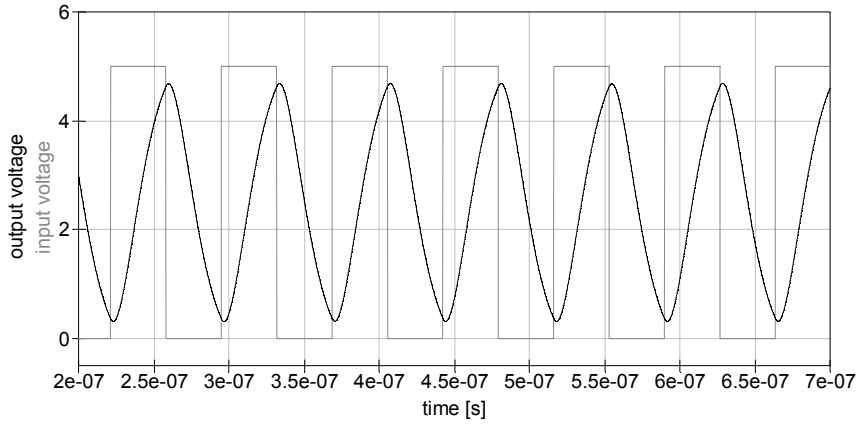


Figure 6.12.: Time diagram of the second order lowpass filter

The changes in the amplitude and the phase are comprehensible mathematically and by simulation (see figure 6.13). Referring to equation 6.10, φ can be calculated by

$$\varphi = \arctan(-\frac{\omega RC}{1-\omega^2 LC}) = 87.33° \pm k \cdot 180°$$

Since the arctan function is 180°-periodic, the result can also be written as

$$\varphi = -92.67°$$

The amplitude of the output signal is calculated by

$$|\underline{H}(j\omega)| = \frac{1}{\sqrt{1 - 2\omega^2 LC + \omega^4 L^2 C^2 + \omega^2 R^2 C^2}} = 0.651$$

which conforms to

$$|\underline{H}(j\omega)|_{dB} = 20 \cdot \log(|\underline{H}(j\omega)|) = -3.72dB$$

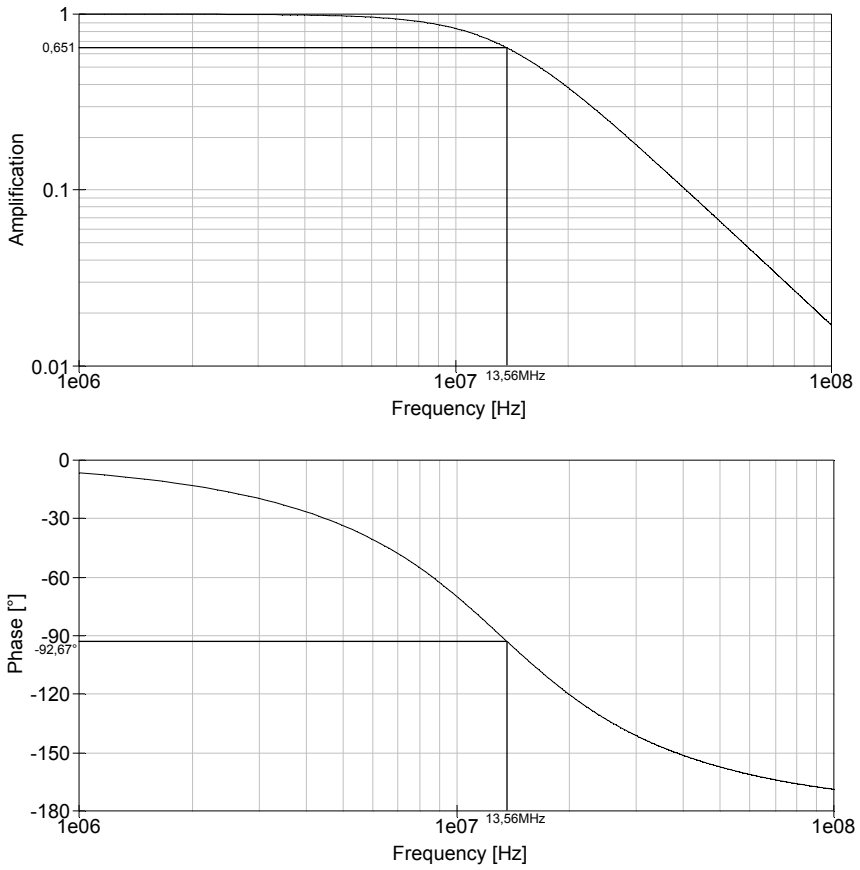


Figure 6.13.: Bode diagram of the second order lowpass filter

With the used circuitry, the signal waveform can on the one hand be altered, but on the other hand it is also possible to change the phase state of the output signal. This attribute will be capitalised in branch four, where we will generate a phase shift of about four degrees. Thereby the chosen resistor and the inductance shall remain stable, which means that for branch four a new capacity value has to be calculated.

Since the phase shift of branch 1-3 is $\varphi_1 = -92.66°$, the phase state of branch four shall become $\varphi_2 = -92.66° + 4° = -88.4°$. From equation 6.10, the new capacitance can be calculated as C_2 = 161.5 pF. The next E12 standard value equals in this case 150 pF, which is the new value of C_2.

For this value the actual gain (see equation 6.11) and phase shift (see equation 6.10) can be calculated as

$$|\underline{H}(j\omega)| = 0.780 \qquad \text{resp.}$$

$$|\underline{H}(j\omega)|_{dB} = -2.16dB$$

and

$$\varphi_2 = -85.21^\circ$$

A comparison of the two bode and time diagrams can be found in the figures 6.14 and 6.15.

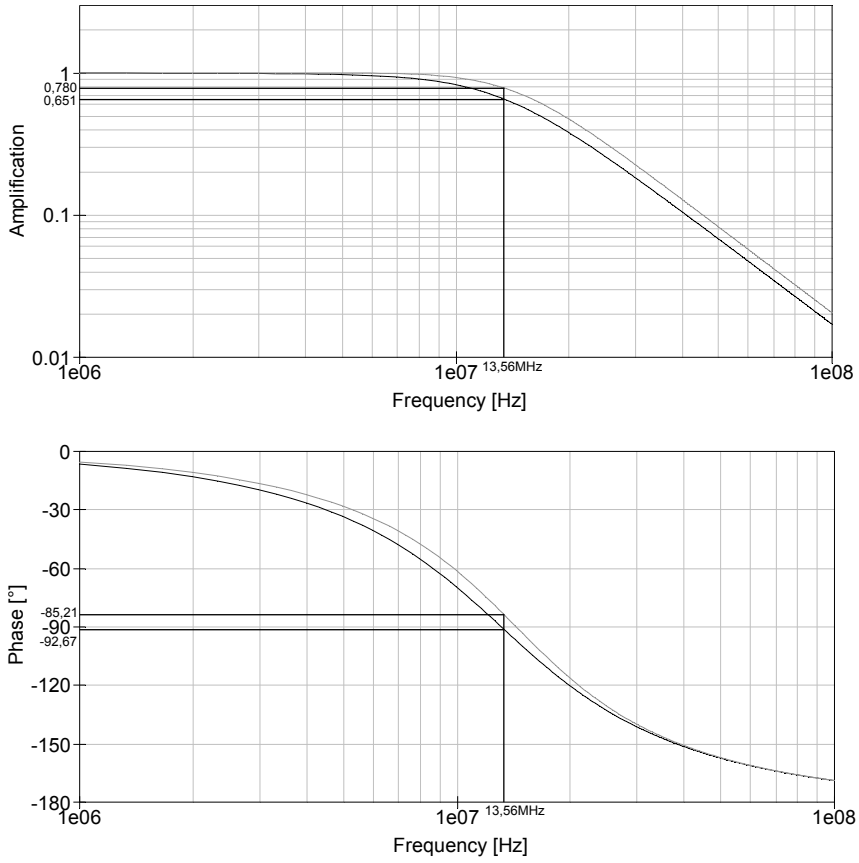


Figure 6.14.: Bode diagram comparison of the second order lowpass filters - with a capacity of 180 pF (black curve) and a capacity of 150 pF (grey curve)

6.2.2.5. Weighted Summing Unit and Output Driver

At this point, all the signal preprocessing has been done and the four branches just have to be amplified, summed up and sent to the antenna. As already stated in chapter 6.2.2.1, the first two signals are intended for establishing the 10 % and the 100 % modulation in mode 1, while for PJM in mode 2, the third and the fourth signal are provided.

The weighted summing unit is implemented by an inverting amplifier circuit, consisting of an operational amplifier and resistors. Because of its high performance (-3dB bandwidth of typically 120 MHz), its high slew rate (typically 800 $\mathrm{V}/\mu\mathrm{s}$), and especially because of its high output

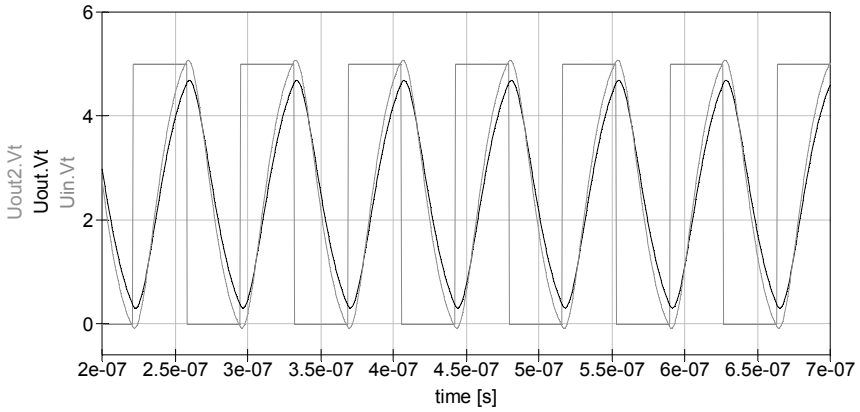


Figure 6.15.: Time diagram of the second order lowpass filters - with a capacity of 180 pF (black curve) and a capacity of 150 pF (grey curve)

current (typically 120 mA at a 10 Ω load resistor), the Analog Devices' AD8017AR amplifier was elected for this application. The advantage of choosing an operational amplifier as an output driver is that the modulation index stays constant, independent of the attached load (antenna). Another advantage of the inverting amplifier circuit in combination with the output driver is its ability to do a summation of different signals, of which each single can be amplified independently. Attention should be paid that the gain may not become too high because by increasing gain, the supported bandwidth decreases (see figure 6.16).

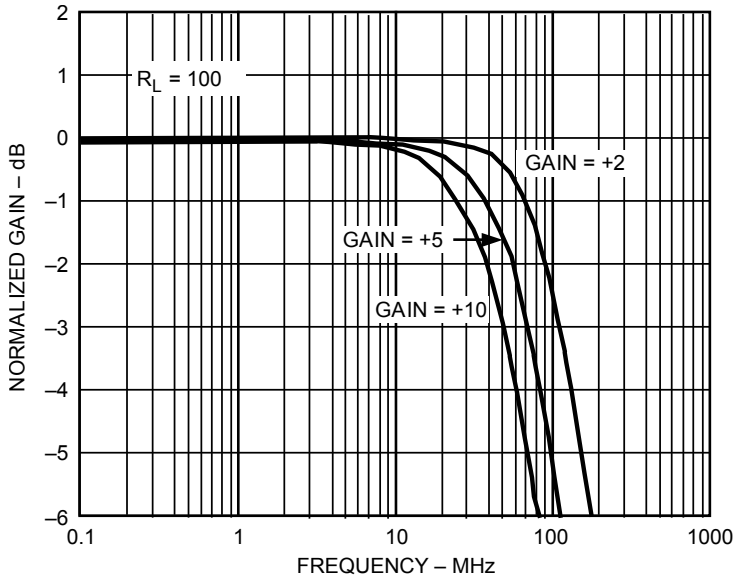


Figure 6.16.: Frequency Response of the AD8017AR; V_S=±2.5 V [2]

The schematics of the summing unit can be found in figure 6.17.

The output voltage of this circuitry is

$$u_a = -(\frac{R_F}{R_{01}} \cdot u_{e1} + \frac{R_F}{R_{02}} \cdot u_{e2} + \frac{R_F}{R_{03}} \cdot u_{e3} + \frac{R_F}{R_{04}} \cdot u_{e4}) \tag{6.14}$$

Mode 1 Following equation 6.15, gaining a modulation index of 10 % requires the ratio between branch 1 and branch 2 to become 82:18.

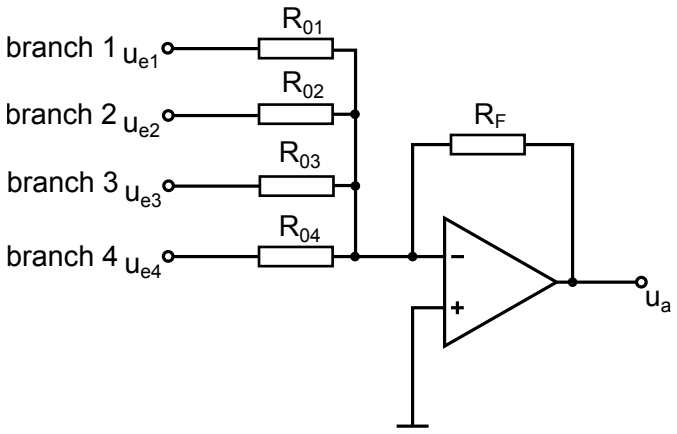


Figure 6.17.: Schematics of the summing unit

$$m = \frac{\widehat{u}_{HI} - \widehat{u}_{LO}}{\widehat{u}_{HI} + \widehat{u}_{LO}} \cdot 100\,\% = \frac{100 - 82}{100 + 82} \cdot 100\,\% = 10\,\% \tag{6.15}$$

$$\frac{R_{01}}{R_{02}} = \frac{82}{18} \tag{6.16}$$

Since for a 100 % modulation the overall gain shall not become bigger than about 10, equation 6.17 can be formulated.

$$\frac{R_F}{R_{01} \parallel R_{02}} = \frac{R_F}{\frac{R_{01} \cdot R_{02}}{R_{01} + R_{02}}} \leq 10 \tag{6.17}$$

For the implementation of the reading device, an overall gain of about 1 and an R_F of 1 kΩ was chosen. From the equations 6.15 and 6.17, the values of the resistors R_{01} and R_{02} can be calculated:

$$R_{01} = 6.2k\Omega$$
$$R_{02} = 1.2k\Omega$$

From these values, the correct modulation index and overall gain are evaluated:

$$m = 8.823\,\%$$
$$G = 0.9946$$

Mode 2 For PJM, branch 3 and 4 are differently diminished because of the unequal cut-off frequencies of the two lowpass filters. Since the two PJM levels at the antenna may only differ in the phase but have to be equal in the amplitude, they have to be amplified by different factors. This is done at the summing unit.

The aim of amplifying the PJM branches is to leave one branch unchanged, while adapting the other branch to the needed amplitude. The ratio between the resistors R_{03} and R_{04} equals the ratio between the two attenuations of the two lowpass filters determined in chapter 6.2.2.4:

$$\frac{R_{03}}{R_{04}} = \frac{0.780}{0.651}$$

If the amplification factor for the third branch is chosen to be one, the two resistors will be valued as

$$R_{03} = 1k\Omega$$
$$R_{04} = 1.2k\Omega$$

6.2.2.6. Antenna

Inductively coupled RFID systems use coils as coupling elements to allow interchanges between readers and transponders. These coils are taking over the function of antennas and therefore the equivalent circuit's components are called *antenna parameters*. Figure 6.18 shows the equivalent circuit of a non-ideal coil.

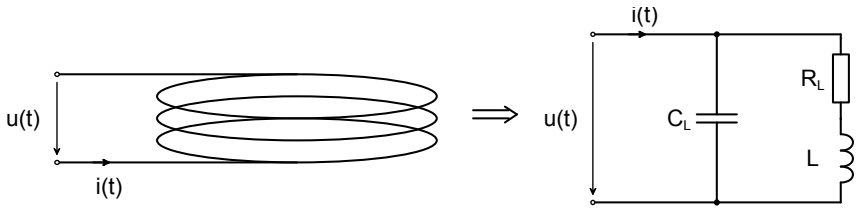


Figure 6.18.: Equivalent circuit of a coil [14]

Some approximated equivalent circuit values of a common reader and a common transponder antenna for vicinity coupling systems are given in table 6.5.

Antenna	L	R_L	C_L
VCD	360 nH	480 mΩ	22.6 pF
VICC	2.26 mH	1.67 Ω	5 pF

Table 6.5.: Exemplary values for equivalent circuit's components of a reader and a transponder coil

Generally a reader's antenna is powered by a voltage source with a certain internal resistance. Usually this resistance is about 50 Ω, in our case this value has decreased due to the driving capabilities of the selected output driver.

The magnitude of the magnetic field generated by the reader's coil is proportional to the power of the voltage source. So in order to use the power of the source efficiently, the losses due to reflection when connecting the antenna to the source are minimised by matching the coil resistance to the internal resistance of the source using a parallel and a serial capacitance. This procedure is called *antenna matching*.

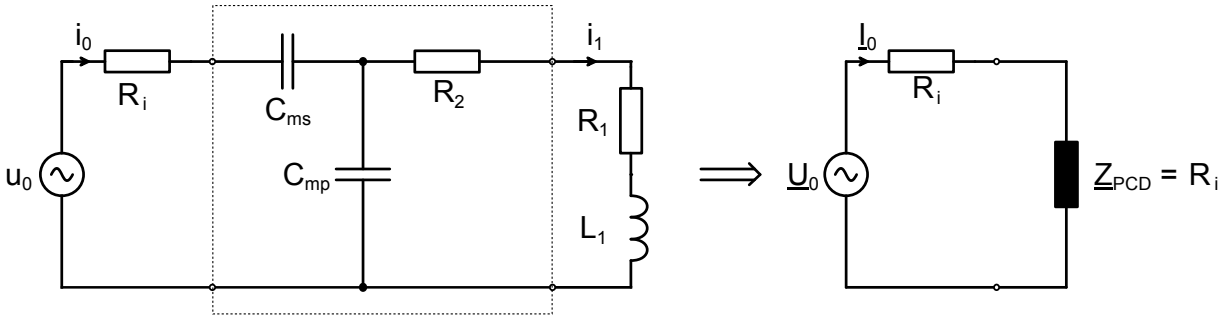


Figure 6.19.: Equivalent circuit of a PCD considering antenna matching (modified from [14])

As stated in [14], the values of the capacitors are determined by equating the internal resistance of the voltage source and the equivalent network impedance $\underline{Z}_{PCD}(j\omega)$ and solving the equations for C_{mp} and C_{ms}.

$$\underline{Z}_{PCD} = \mathrm{Re}\,(\underline{Z}_{PCD}) + j \cdot \mathrm{Im}\,(\underline{Z}_{PCD})$$

For the real and the imaginary part of the antenna impedance, the following equations shall be valid:

$$\mathrm{Re}\,(\underline{Z}_{PCD}) \stackrel{!}{=} R_i$$

$$\mathrm{Im}\,(\underline{Z}_{PCD}) \stackrel{!}{=} 0$$

From which it follows:

$$C_{mp} = -\frac{\sqrt{R_i(R_1+R_2)^3 - R_i^2(R_1+R_2)^2 + \omega^2 L_1^2 R_i(R_1+R2)} - \omega R_i L_1}{\omega R_i((R_1+R_2)^2 + \omega^2 L_1^2)} \tag{6.18}$$

$$C_{ms} = -\frac{\omega^2 C_{mp}^2(R_1+R_2)^2 + \omega^4 C_{mp}^2 L_1^2 + 2\omega^2 C_{mp} L_1 + 1}{\omega^2 C_{mp}(R_1+R_2)^2 + \omega^4 C_{mp} L_1^2 - \omega^2 L_1} \tag{6.19}$$

The reader's quality factor mainly depends on the quality factor of its antenna. In the equivalent circuit according to figure 6.19, the antenna coil is represented by the inductance L_1 and the resistance R_1. Thus, the quality factor of the coil is calculated by

$$Q_{coil} = \frac{\omega_{res} \cdot L_1}{R_1} \tag{6.20}$$

The quality factor of the coil including the adjustment circuit can be calculated by

$$Q_{adj} = \frac{\omega_{res} \cdot L_1}{(R_1+R_2)} \tag{6.21}$$

For the whole reader, the quality factor can be calculated to

$$Q_{PCD} = \frac{\omega_{res} \cdot L_1}{(R_1+R_2+R_i)} \cong \frac{Q_{adj}}{2} \tag{6.22}$$

According to [15], for a higher quality factor the inertia of the system increases. From this context, the quality factor requirements of the developed reader can be derived. From the time law in communications engineering, which says that equation 6.23 is valid, we can connect the quality factor with the required rise time (see equation 6.21). In the following equations, B stands for the bandwidth, T for the maximum rise time of the system, Q is the quality factor of the antenna and f_c is the carrier frequency of the transmitted signal.

$$B \cdot T = 1 \tag{6.23}$$

$$Q = \frac{f_c}{B} = f_c \cdot T \tag{6.24}$$

For vicinity coupled systems, the maximum rise time is 4.5 μs (cf. chapter 4.2.1), so the quality of the antenna is theoretically delimited by 61. In practice, a target quality of the antenna of about 30 is lined up for vicinity.

For PJM, the maximum rise time (phase transition time) is 1.18 μs, which leads to a maximum antenna quality of 16.

In the following, a dimensioning example for the antenna's adjustment circuit assuming the values for the antenna from table 6.5 is given. The calculated values are first approximation values and used as a starting point for further adjustment iterations.

Since the connection between the reading device and the affilated antenna is short in comparison to the wavelength of the 13.56MHz carrier, the internal resistor R_L becomes needless. From the elected antenna quality the value of R_2 can be calculated from 6.21 by

$$\begin{aligned} R_2 &= \frac{\omega_{res} \cdot L_1}{Q_{adj}} - R_1 \\ &= \frac{2\pi \cdot 13.56\,MHz \cdot 360\,nH}{16} - 480\,m\Omega \\ &= 1.437\,\Omega \end{aligned}$$

For the dimensioning of the capacitors C_{mp} and C_{ms}, the freeware tool SMITH, created by the Berne University of Applied Sciences, was used. The aim was to achieve an overall ohmic resistance of 10 Ω. Therefor, the first step is to calculate the starting point of the antenna. This is done by evaluation of the overall impedance of the circuit shown in figure 6.18 with applied component values of table 6.5:

$$\begin{aligned} X_L &= \frac{(R_L + j\omega L) \cdot (-\frac{j}{\omega C_L})}{R_L + j\omega L - \frac{j}{\omega C_L}} \\ &= (1.979 + j32.6)\,\Omega \end{aligned}$$

This complies with an ohmic part of 1.98 Ω ($R_1 + R_2$) and an inductive part of 32.6 Ω at 13.56 MHz. This conforms to point 1 in figure 6.20. Starting from this point, a parallel capacitor is appended to bring the ohmic part of the antenna to the value of 10 Ω at 13.56 MHz (see step 2 in figure 6.20). Therefore, a parallel capacitance C_{mp} of 201 pF is necessary. After including this capacitor in the network, the ohmic part of the antenna has already been achieved, but there is still a certain inductive part left which will be compensated by a serial capacitor C_{ms} in the next step. As you can see in figure 6.20, the value of this capacitor has to be 160 pF. After including this component, the antenna should be tuned to the required 10 Ω. A further fine-tuning will be done online by affilating the antenna including the adjustment circuit to a network analyser and turning the trim capacitor manually.

6.2.2.7. Overall System Implementation

The modulator was crafted by using the CadSoft EAGLE Layout Editor and milling of the engineered circuit board. The schematics generated in EAGLE can be found in attachment A.

The input signals (clock, data and mode choice signals) are provided by the Cortex-M3 microcontroller and applied to the developed system by the interface introduced in section 6.1.

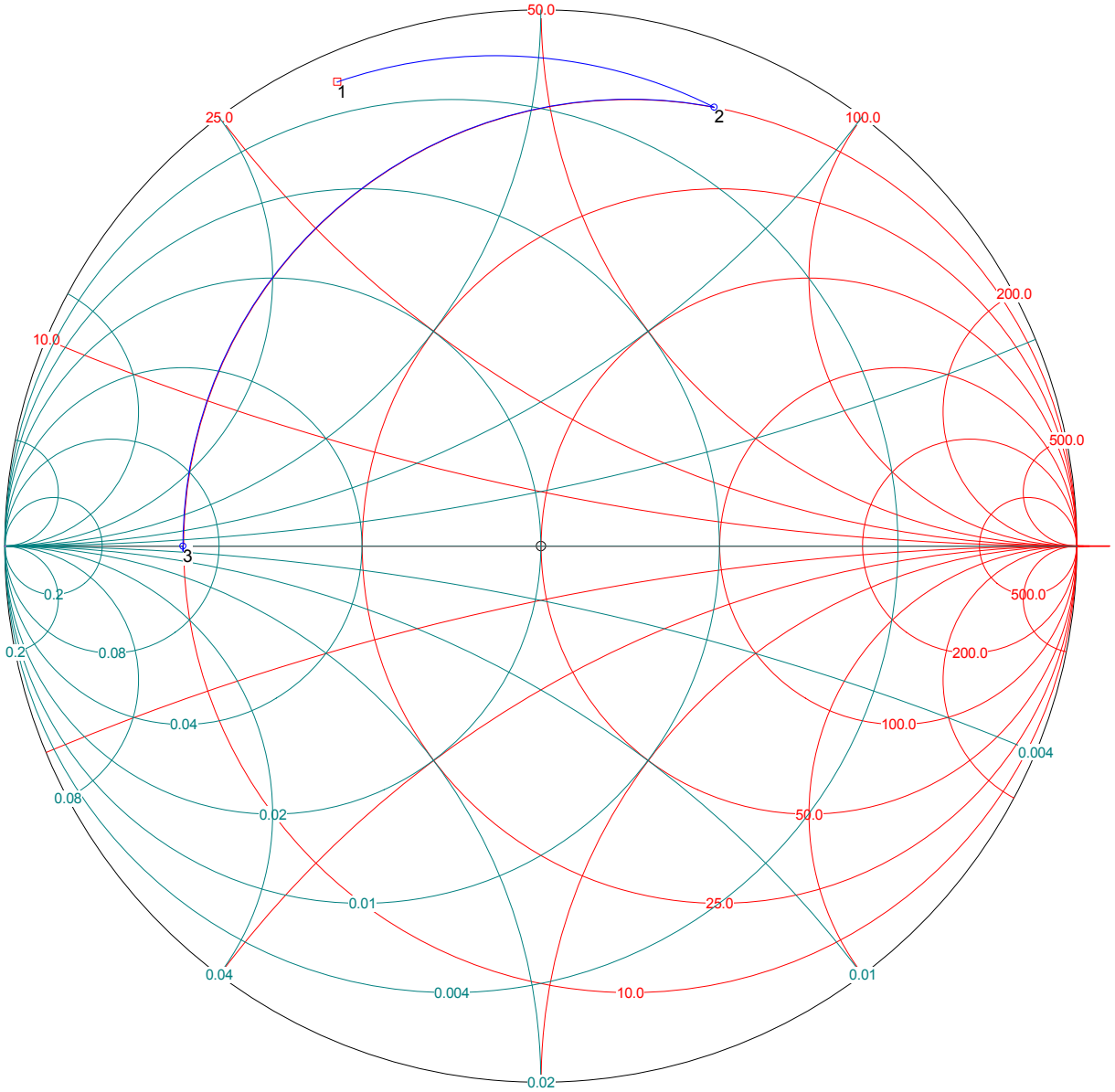


Figure 6.20.: Antenna adjustment procedure

The power supply is also gained by the Cortex-M4 microcontroller board. There exists a 5 V (VCC), a 3.3 V and a GND level. The digital component parts (74LVCxx components) are supplied by 3.3 V and GND, while the analog circuitry is supplied by 5 V and GND. The internal analog ground level is lifted from 0 V to 2.5 V by a voltage regulator, so that the signals provided by the digital part (74LVC126AD outputs) can be processed symmetrically. In this case, the original, digital ground level represents the -2.5 V of the analog part, whilst the original VCC level represents +2.5 V.

The summing unit requires a signal which is located symmetrically around the analog ground level. Because of this, a highpass filter is inserted directly behind the buffers' outputs (i.e. formed by C11 in combination with R1 for branch 1) with a barrier frequency of 15.9 kHz. The capacities for this highpass are dimensioned by a value of 10 nF, which amounts to a serial resistance in the branch of $\frac{1}{\omega C} = 1.17\,\Omega$ at the frequency of 13.56 MHz and therefore causes only a minor RF voltage drop over the capacities.

Since the input of the second order lowpass filter is adjusted around 2.5 V, also its output is symmetrically centered around this voltage level. It does not matter that the ground of the lowpass filter equals the digital ground level, because once the capacity is charged, it keeps the voltage level and stays at this value.

Between the output driver and the SMA socket to operate the antenna, one resistor and one capacitor are inserted. Their aim is generally to adjust the output resistance to the resistance of the attached antenna or oscilloscope. Since the antenna is in our design directly attached to the reading device (input lead short in comparison to 13.56 MHz), the values of these components can be set to zero.

The verification results of the entire assembled modulator can be found in chapter 7.

6.3. Receive-Path

For the receive path, a few different realisation concepts were considered. All of them apply to the carrier demodulation whose output then is digitised and fed into the microcontroller. Four different demodulation concepts for carrier demodulation will be examined in this chapter and evaluated concerning their advantages and handicaps. Then one concept will be chosen and realised for both, mode 1 and mode 2.

6.3.1. Functional Basic Concepts

6.3.1.1. Passive Rectification with Diodes

As already described in section 3.2.1.2, the rectification and lowpass filtering of a received RF signal for demodulation of an amplitude modulated signal is an incoherent demodulation procedure. The circuitry itself is facile to implement and low-priced.

However, in practice it was shown that the amplitude modulated signal received from the VICC is not always an ideally amplitude modulated signal. In the last resort, the supposed amplitude modulated RF signal is not received as an amplitude modulated signal at all; it can be exclusively modulated in its phase. Certainly, this modulation type can not be demodulated with this circuitry. To exclude the possibility of an exclusive phase modulation, the input signal has to be single-sideband filtered before it is fed into the demodulation circuitry.

Functionality The capacities C1 and C2 are needed to ensure the operation of the rectifier. For the negative half cycle of the input signal the circuit is closed above C1, C2 and D1. From

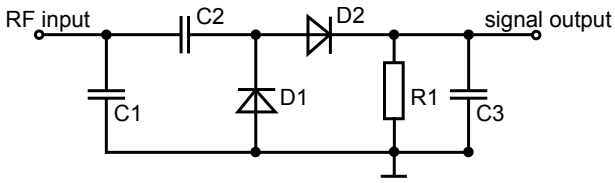


Figure 6.21.: Demodulation by half-wave rectifier

another point of view, C1 can be considered as smoothing capacitor, whilst C2 cuts off the constant component of the signal. After C1 has depicted a circuit to bulk, one has to bear in mind to keep the impedance of this capacity big (for example, $Z_{C1} = 1\,k\Omega@13.56\,MHz$). In contrast, the impedance of C2 shall be small for 13.56 MHz (for example, $Z_{C2} = 1\,\Omega$).

D1 and D2 are used for the rectification of the signal itself. The diode D2 forwards the positive half cycle to discharge to bulk over R1, C3 and R2. D1 forwards the negative half cycles, the circuit is closed above C1 and C2.

R1 and C2 form a lowpass filter to flatten the output signal. For the cut-off frequency, imperatively equation 6.25 is valid:

$$R_1 = \frac{1}{\omega C_3} = \frac{1}{2\pi f_C C_3} \tag{6.25}$$

From this it follows that the cut-off frequency is

$$f_C = \frac{1}{2\pi R_1 C_3} \tag{6.26}$$

Since a flattening of the carrier signal (without damping the subcarrier signal too much) is desired, the cut-off frequency has to be selected following these requirements (for example, $f_C = 160\,kHz$).

Simultaneously it has to be considered that the parallel resistance may not become too small.

$$Z = R_1 \parallel C_3 = \frac{R_1 \cdot \frac{1}{j\omega C_3}}{R_1 + \frac{1}{j\omega C_3}} = \frac{R_1 - j\omega C_3 R_1^2}{1 + \omega^2 C_3^2 R_1^2}$$

$$|Z| = \frac{\sqrt{R_1^2 + \omega^2 C_3^2 R_1^4}}{1 + \omega^2 C_3^2 R_1^2} \tag{6.27}$$

For example, the value of $|Z| = 1k\Omega$ would be feasible. From the equations 6.26 and 6.27 the two unknowns R_1 and C_3 can be calculated.

Signal processing A signal demodulation circuit following the principle of a passive rectification with diodes would for example consist of the blocks shown in figure 6.22. The single-sideband filter impedes phase-only modulation, the gain is needed to drive the diodes (cut-off voltages have to be excessed), the half-wave rectifier does the rectification.

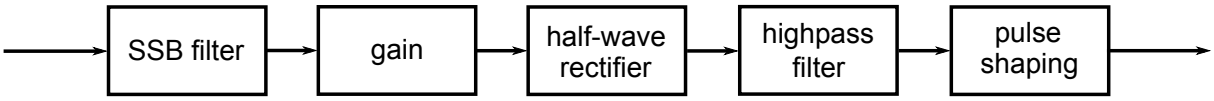


Figure 6.22.: Block diagram of the passive rectification analog signal processing

The rectifier then has to be followed by a highpass filter to cut off the constant component. This is a preparatory work done because the following pulse shaper needs signals adjusted around its bulk levels.

The requirements for the highpass filter are as follows:

- high input resistance
- low output resistance
- high bandwidth
- a high slew rate is advantageous but not inalienable, since the next block is a pulse shaper
- a certain gain is advantageous

According to these requirements, the highpass filter was decided to be implemented as an active filter. I chose an active highpass filter of a second order with a single positive feedback loop (see figure 6.23). The dimensioning is done according to [16]. For ease of dimensioning, A_∞=1 and C_4=C_5=C was assumed. In this case, R_2 and R_3 can be calculated by

$$R_2 = \frac{1}{\pi f_g C a_1}$$

and

$$R_3 = \frac{a_1}{4\pi f_g C b_1}$$

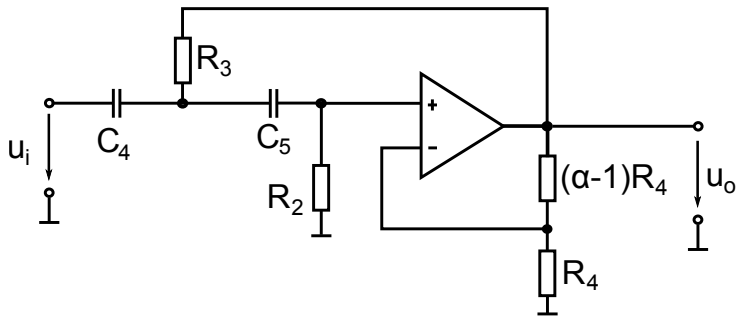


Figure 6.23.: Second order active highpass filter with a single positive feedback loop

For example, a cut-off frequency of 5kHz, capacities of C=1nF and a resistor R_4 of 1 kΩ may be chosen. The coefficients a_1 and b_1 are picked from coefficient tables for example in [16] and depend on the filter characteristics and the filter order.

An example of a pulse shaper is shown in figure 6.24. This pulse shaper reacts on the edges of the input signal. Clear, steep edges are though an advantage.

The elements R_5/C_6 and R_6/C_7 are forming lowpass filters with differing time constants. While the R_5/C_6 lowpass is very fast, the lowpass filter built of R_6/C_7 delays the input signal. The output switches at the intersection point of these two signals. Additionally, since this pulsformer is an inverting circuit, the feedback resistor R_7 attenuates the signal at the positive input, so that for a noisy signal the probability of intersections between the positive and the negative inputs are minimised. Figure 6.25 may make the different signal wave shapes plainer.

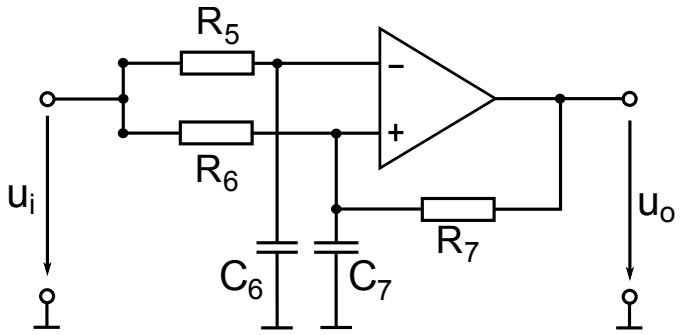


Figure 6.24.: Pulse shaper circuit

Advantages

- economically feasible

Disadvantages

- needs a minimum input voltage to excess the diode's cut-in voltage
- single-sideband filter at the input necessary to avoid an exclusively phase modulated signal

6.3.1.2. Active Rectification

An alternative to the demodulation by passive rectification is the use of an active rectifier. Therefore, the block diagram of the signal flow generally stays the same, the only difference is the exchange of the passive rectification block for an active rectification block, and that is also the reason for the omission of the gain prior to the rectification block (see figure 6.26).

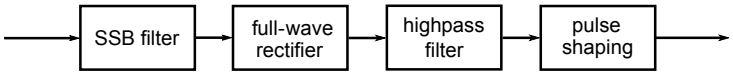


Figure 6.26.: Block diagram of the demodulation signal flow by the use of an active full-wave rectifier)

The schematic diagram (see figure 6.28) for this realisation is extracted from [9]. This circuit consists of a half-wave rectifier which rectifies both, the positive and the negative half-wave. Then the difference between the two signals is calculated. For illustration, see figure 6.27.

Once one of the diodes works in its transmission range, IC1 operates as an inverting amplifier. The gain levels are $g_{u+} = -\frac{R_2}{R_1}$ for the positive half-wave and $g_{u-} = -\frac{R_3}{R_1}$ for the negative half-wave.

If the output of IC1 becomes smaller than the diode's forward voltage, the operational amplifier readjusts, so that already for minimum input voltages one of the diodes is working in its transmission range. Ideally, the operational amplifier does this correction already for an input voltage of 0 V. In this case, the diode's flux voltage is reduced to the value of the open loop gain G:

$$u_F{}' = \frac{u_F}{G} \qquad \overset{G\to\infty}{\longrightarrow} \qquad u_F{}' = 0\,V$$

Therefore, also the least input voltages are precisely rectified. If G descents for higher frequencies, a nonlinearity is observed for smaller input voltages because of the increasing $u_F{}'$.

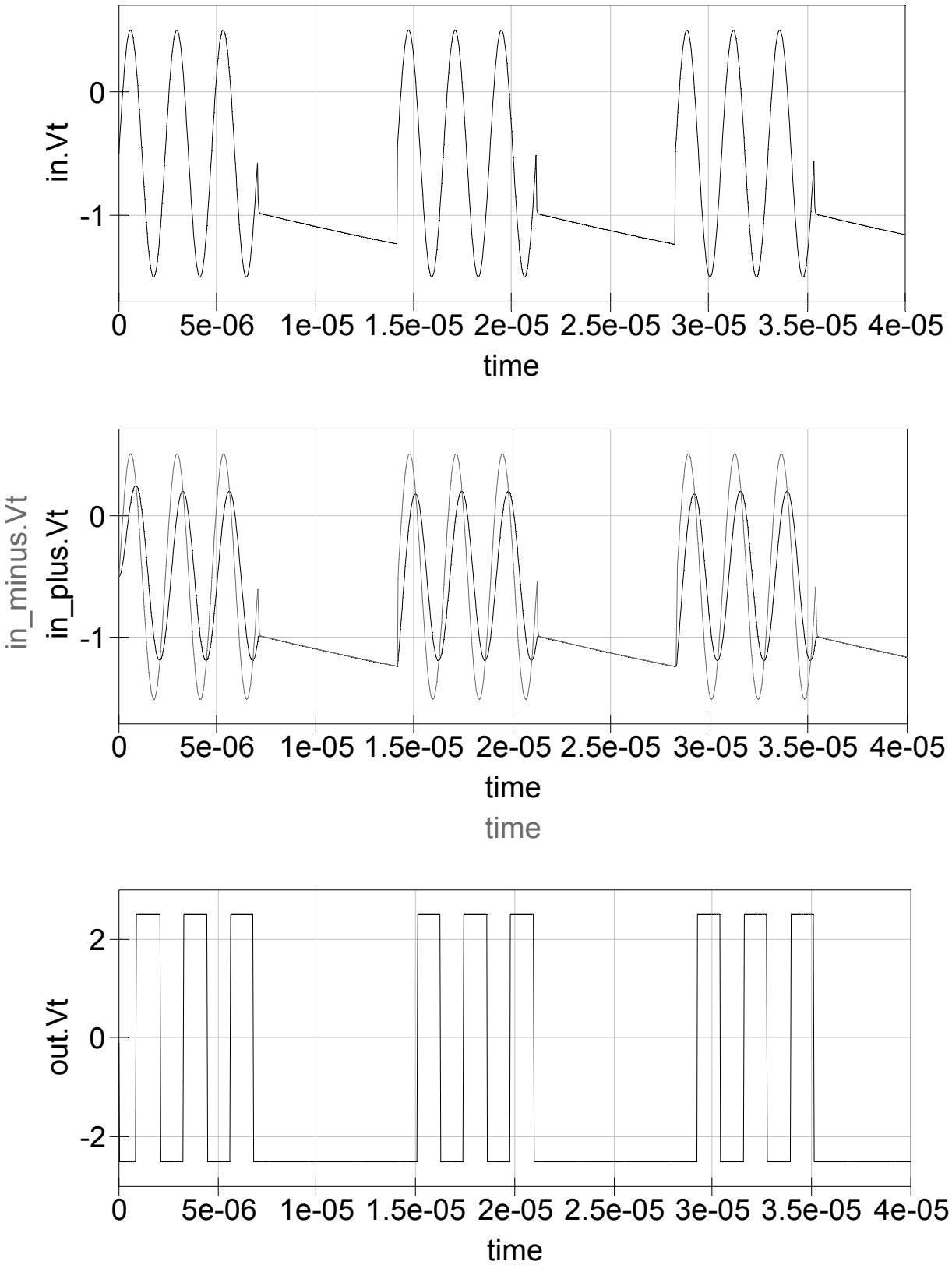


Figure 6.25.: Pulse shaper signals

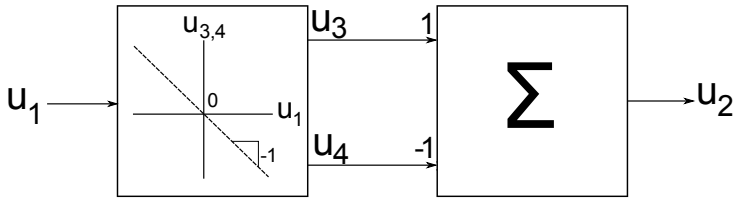


Figure 6.27.: Block diagram of an active full-wave rectifier (modified from [9]

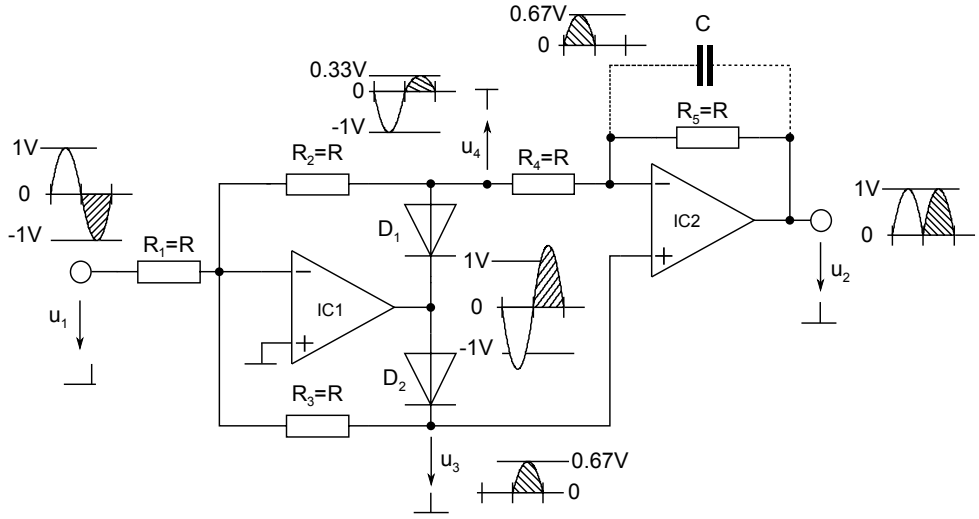


Figure 6.28.: Full wave rectification circuit (modified from [9])

Problems using operational amplifiers for signal rectification For higher frequencies, active rectification may cause problems because of the limited gain-bandwith-product and the finite slew-rate. If the open loop gain decreases for higher frequencies, nonlinearities due to the increasing $u_F{}'$ may occur for small input-voltages (see figure 6.29).

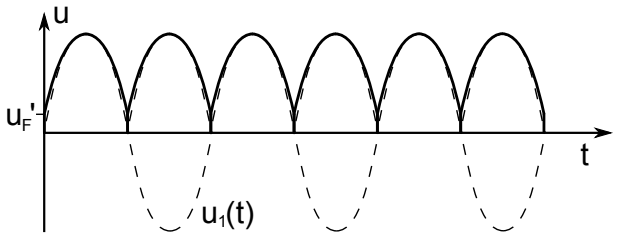


Figure 6.29.: Distortion of the output signal at higher frequencies caused by the decreasing, finite GBP (modified from [9])

For a too small slew rate, the operational amplifier may not be able to follow the signal waveform. The output signal seems to be distorted in this area. For sine shaped signals this is found around the zero crossings. For bigger input signals, the maximum level may no longer be achieved (see figure 6.30).

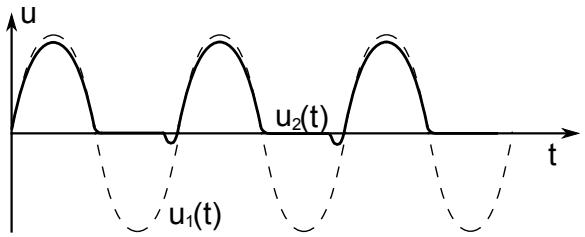


Figure 6.30.: Distortion of the output signal at big amplitudes and frequencies caused by the too small slew rate (modified from [9])

These characteristics can be upgraded by a neatly choice of the circuit resistors and the load.

Advantages

- the gain before the rectifier may omit

Disadvantages

- the input voltage amplitude must stay under a certain value
- single-sideband filter at the input necessary to avoid an exclusively phase modulated signal
- two operational amplifiers with a high GBP and slew rate and low-capacity diodes are necessary for the rectification

6.3.1.3. I/Q Demodulation by ring mixers

For the use of ring mixers to demodulate the incoming RF signal, two transducers are necessary for potential separation. The configuration of the ring mixer itself can be seen in figure 6.31.

Generally, signal mixing can be done by the multiplication of two signals. This process will become especially simple if the high frequency local oscillator signal is a rectangular signal. In the case of a unipolar rectangular signal, the multiplication becomes a switching (multiplication by 0 and 1), in the case of a bipolar rectangular signal the multiplication becomes a switching between the original signal and its inverted signal (multiplication by -1 and 1).

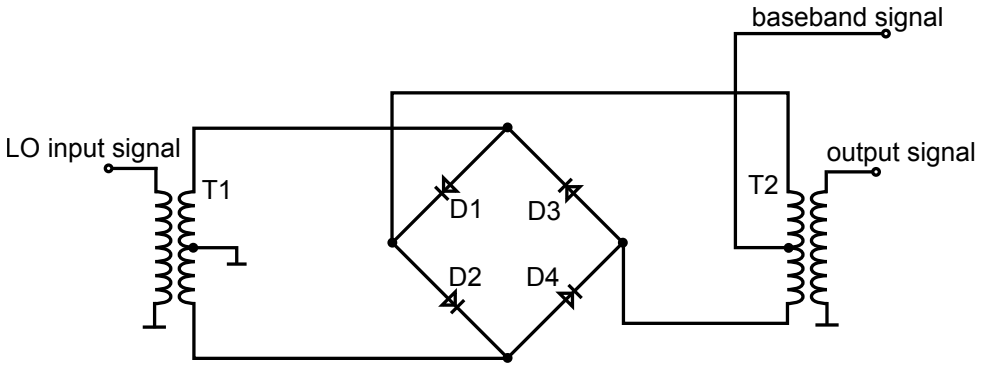


Figure 6.31.: I/Q BPSK demodulator composed of transducers and diodes

In figure 6.31, the LO input signal activates ('switches on') either the diodes D1 and D2 or D3 and D4, depending on whether the LO signal is positive or negative. In this case, the LO input signal was a high-frequency bipolar, rectangular signal. Now an additional current caused by the voltage of the baseband signal can flow through the activated diodes. The transducer

couples this current from its primary to the secondary coil. There a voltage proportional to the baseband voltage but multiplied with the sign of the LO's input is induced.

This modulator can also be used to demodulate an RF signal after a slight modification and expansion. A resulting I/Q demodulator can be found in figure 6.32.

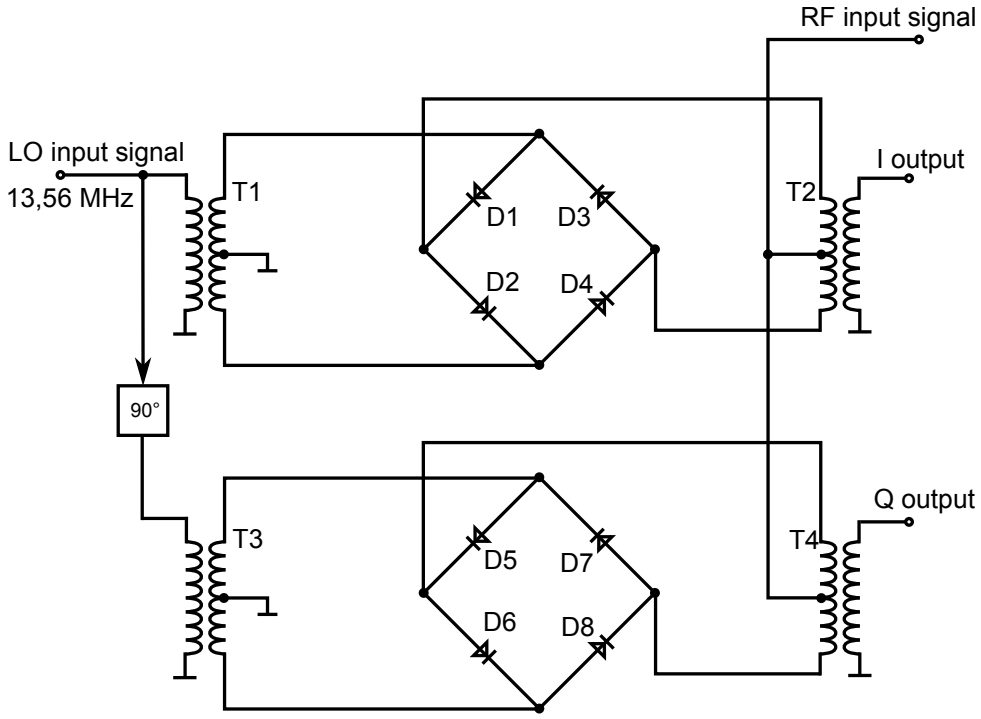


Figure 6.32.: Demodulator composed of two modulators

Signal processing Figure 6.33 shows a block diagram of the signal flow for this realisation. In this case, the I/Q branch decision seems to become problematic to be realised from the circuit technology point of view.

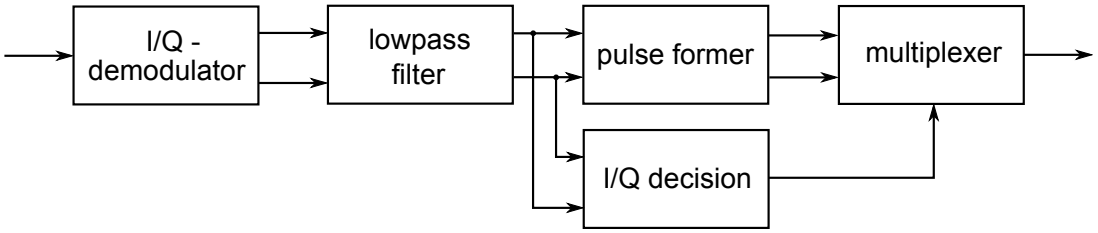


Figure 6.33.: Signal flow of a demodulation by the use of an I/Q demodulation by ring mixers

Advantages

- the single sideband filter is not applicable

Disadvantages

- the transducers are big components which need lots of space
- two channels (I and Q channel) have to be processed separately, a decision unit is needed in the end

6.3.1.4. I/Q-Demodulation by an integrated circuit

Ulrich Tietze and Christoph Schenk write in their book [16] in chapter 'I/Q Mixers with Double Push-Pull Modulators' that an I/Q mixer will work only correctly, if the mixing gains of the two mixers are equal and the phase shift between the local oscillator's signals is 90°. These demands can, without any adjustment, only be fulfilled by implementing both mixers inclusive of the components for the generation of the LO signals in **one** integrated circuit.

An example of an I/Q mixer's block diagram is given in figure 6.34. There, the two signals $\cos(\omega_T t)$ and $-\sin(\omega_T t)$ are the 90° phase shifted local oscillator's signals. Their frequency equals the carrier frequency f_c of the received signal $s_T(t)$.

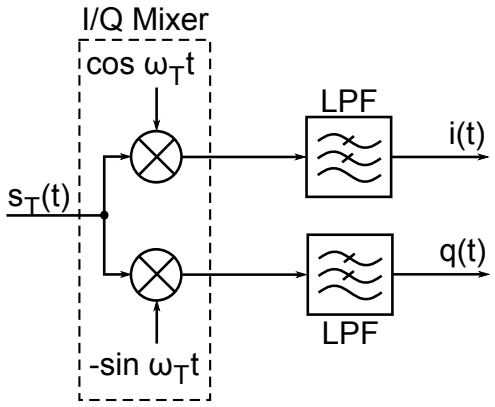


Figure 6.34.: I/Q demodulator composed of a digital I/Q mixer (modified from [16])

Signal processing According to the signal demodulation path implemented by ring mixers, the signal demodulation realised by an integrated circuit needs a circuitry to determine the superioriority of the demodulated I- respectively Q-path.

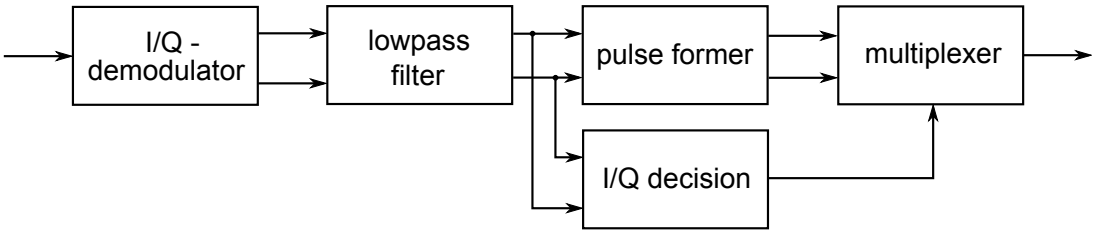


Figure 6.35.: Signal flow of a demodulation by the use of an I/Q demodulator

Advantages

- the single sideband filter is not applicable
- works without any adjustment
- straightforward demodulation

Disadvantages

- two channels (I and Q channel) have to be processed separately, a decision unit is needed in the end

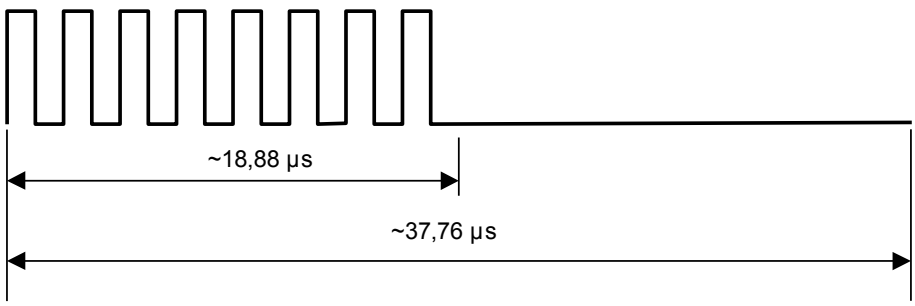
6.3.1.5. Comparison of the Basic Concepts and Selection of a Perpetuated Concept

All of the four introduced possibilities of demodulating the received signals have their particular drawbacks. For the demodulation by active or passive rectification, the single sideband filter is not easy to realise because of the requested filter sheerness. For the demodulation by an I/Q demodulator, the I/Q channel decision may turn out to be a challenge.

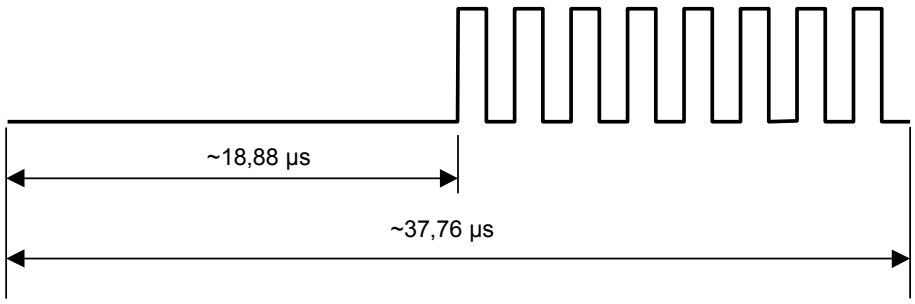
Because of the straight-forward demodulation by using an integrated I/Q demodulator, the decision was made to implement the fourth introduced alternative.

6.3.2. Receive Path for Mode 1

The subcarrier demodulation and signal decoding is done in the microcontroller. The output of the readers' analog part, the carrier-demodulated baseband signal, is digitised and ushered into the Cortex-M3 microcontroller through its pin SPI_MISO. Each positive slope on this pin causes an interrupt in the microcontroller, whose routine provides the time passed since the last interrupt triggered on SPI_MISO. These trigger-times can differ between 2.36 µs (if a toggling subcarrier is received), 18.88 µs+2.36 µs = 21.24 µs (if a pause is received) or 2·18.88 µs+2.36 µs = 40.12 µs (if two consecutive pauses are received), depending on the transmitted data. If the received trigger times equal for example 7x2.36 µs, followed by 1x18.88 µs, the received bit equals a logic '0' (cf. figure 6.36a).



(a) Logic 0



(b) Logic 1

Figure 6.36.: Mode 1 - RX: Coding with one subcarrier [6]

Since the decision was made to realise the signal demodulation both for mode 1 and mode 2 by an integrated I/Q demodulator, the block diagram in figure 6.37 is valid. Since the I/Q demodulator delivers two output signals from which we do not know which is the major one, both signals are equally processed in a parallel way. The lowpass filter cuts off the high frequency signal parts while the puls shaping unit prepares the analog signals for a digital postprocessing. Parallel to that, the two signal branches are evaluated concerning their baseband signal concentration. The signal with the more significant baseband waveshape is connected through to the microcontroller board. The following subsections will cater to the particular blocks of this block diagram.

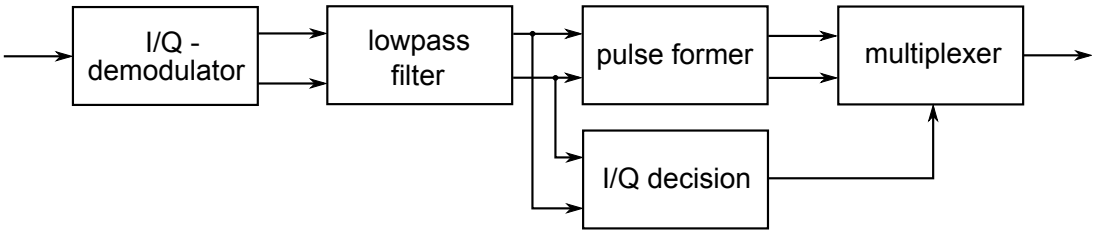


Figure 6.37.: Signal flow of a demodulation by the use of an I/Q demodulator

6.3.2.1. I/Q Demodulator

For the I/Q-demodulation of the incoming signal, the monolithic integrated quadrature modulator RF2713 from RF micro devices was chosen. It is based on the gilbert cell principle and used to recover the I and Q baseband signals from the amplified and filtered Intermediate Frequency (IF). The unit operates from a single 3 V to 6 V power supply, demodulates IF frequencies ranging from 100 kHz to 250 MHz and supports baseband signals from DC to 50 MHz whereby it meets the requirements of our system. As shown in figure 6.38, the IC contains all of the required components to implement the modulation/demodulation function and contains a digital divider type 90° phase shifter, two double balanced mixers, and baseband amplifiers designed to interface with Analog to Digital Converters (ADCs).

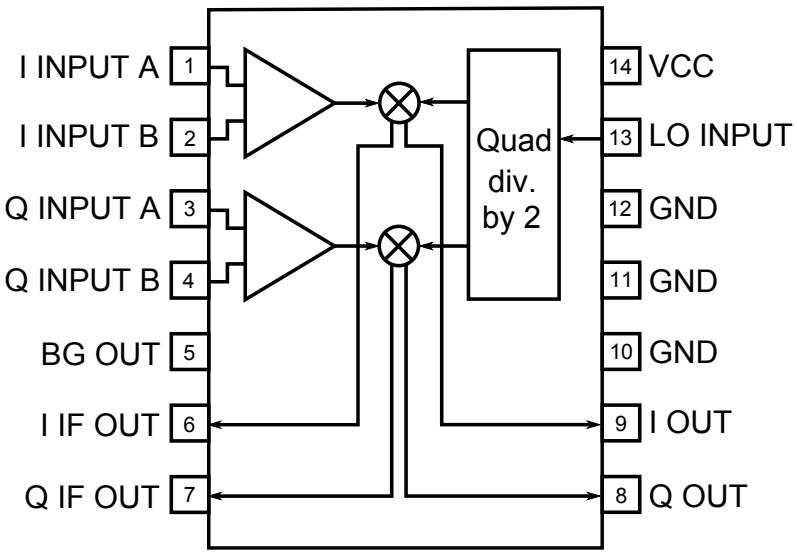


Figure 6.38.: Functional Block Diagram of an RF2713 (modified by [11])

The demodulation by an I/Q demodulator is based on the coherent ASK demodulation principle. During this procedure, the incoming signal is multiplied by a local oscillator signal equalling the IF. As stated in chapter 3.2.1.2, if the phasing between the LO and the IF signal equals 90°, the demodulation component related to the transmitted baseband signal approaches zero. The remedial measure for this phenomenon is to multiply the incoming IF signal twice: Once by the original LO signal and once by the 90° phase shifted LO signal. At least one of the two originating products contains fractions of the baseband signal.

The circuit of the RF2713 (see figure 6.39) follows, with little modifications, the application schematic of the demodulator configuration in [11]. Since the frequency gained by the LO input (pin 13) is divided between 2, the signal connected to this pin must twice of the IF, which results in 27.12 MHz. A signal of this frequency is delivered by the Cortex-M3 microcontroller board via pin 27_12MCLK.

The A input of the RF2713 is connected to the first pin of the CSPC antenna. The antenna is driven differentially, which means that the B input of the RF2713 is not grounded as proposed in the datasheet but rather connected to the second pin of the CSPC antenna. The circuit at the antenna input is a signal attenuation circuit which allows to prevent the RF2713 from overdriving. By this circuit, the two antenna outputs are affilated over the three input resistors (100 Ω, 4.7 kΩ and 100 Ω). The delivered signal is pending on these resistors. The amount of the received signal fed into the RF2713 depends on the tuning of the 4.7 kΩ potentiometer:

$$u_{1.2} = \frac{R_x}{100\Omega + R_x + 100\Omega}$$

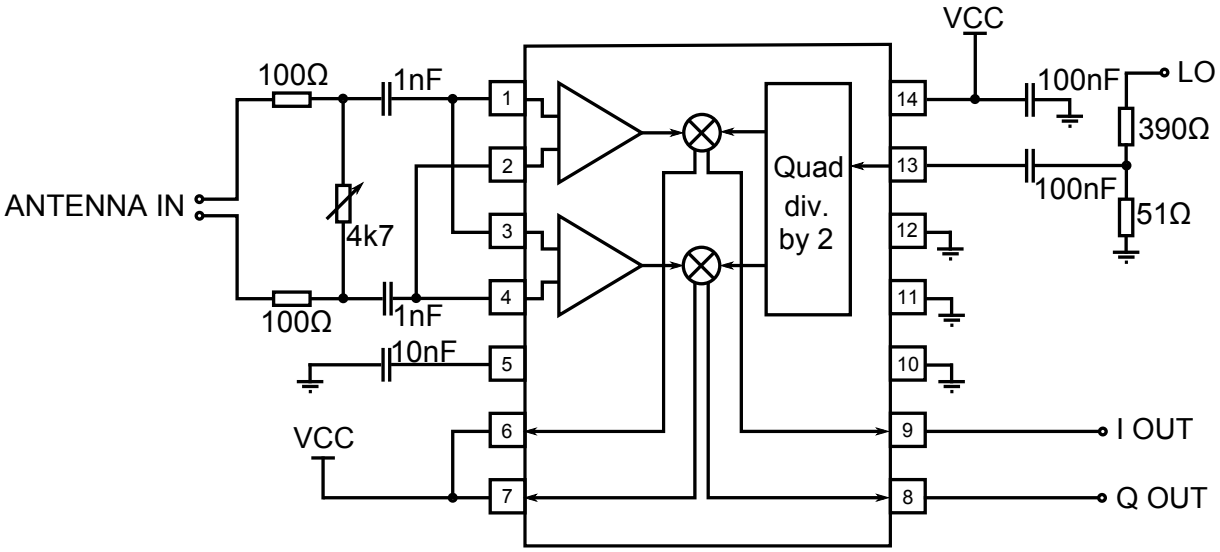


Figure 6.39.: Demodulator Configuration of an RF2713 (modified by [11])

The outputs of this circuitry are the I and the Q output resulting from the multiplications of the IF signal by the local oscillator and by the phase shifted local oscillator. These signals consist of a mixture of the baseband signal and higher frequency components, like for example 27.12 MHz signals.

6.3.2.2. Lowpass Filter

To filter the usable baseband signal from the output delivered by the RF2713, there is an active second order lowpass filter with a single positive feedback loop applied (*Sallen-Key structure*). This circuit is gathered from [16]. The schematic of the used circuitry can be found in figure 6.40.

The general transfer function of lowpass filters can be found in 6.28

$$A(s_n) = \frac{A_0}{\prod_i (1 + a_i s_n + b_i s_n^2)} \tag{6.28}$$

which is particularly for a second order lowpass filter

$$A(s_n) = \frac{A_0}{1 + a_1 s_n + b_1 s_n^2} \tag{6.29}$$

The transfer function of the lowpass filter circuit shown in figure 6.40 reads as follows:

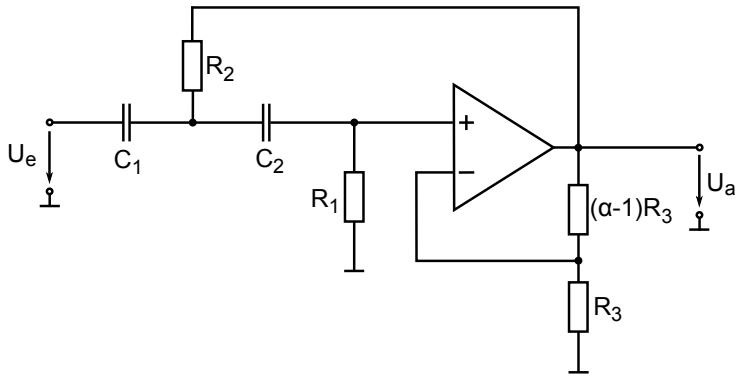


Figure 6.40.: Second order active highpass filter of Sallen-Key structure [16]

$$A(s_n) = \frac{\alpha}{1 + \omega_g[C_1(R_1 + R_2) + (1-\alpha)R_1C_2]s_n + \omega_g^2 R_1 R_2 C_1 C_2 s_n^2} \tag{6.30}$$

For simplification of the dimensioning the specialisation of $R_1 = R_2 = R$ and $C_1 = C_2 = C$ is chosen. To realise different filter types (Bessel, Butterworth, 3db-Tschebyscheff, Critical), in this case the inner amplification factor α has to be varied. The transfer function in this case is

$$A(s_n) = A(s_n) = \frac{\alpha}{1 + \omega_g RC(3-\alpha)s_n + (\omega_g RC)^2 s_n^2} \tag{6.31}$$

Equating coefficients to the general transfer function of lowpass filters delivers

$$RC = \frac{\sqrt{b_1}}{2\pi f_g} \tag{6.32}$$

$$\alpha = A_0 = 3 - \frac{a_1}{\sqrt{b_1}} = 3 - \frac{1}{Q_1} \tag{6.33}$$

It can be seen that the inner amplification α just depends on the pole quality and is independent of the cut-off frequency f_g. The filter type is in this case defined by the inner amplification α. The filter coefficients a_i and b_i can be gained from [16]. For this thesis, the filter characteristic of a Bessel filter was chosen because of its optimal characteristics concerning the propagation of rectangle signals. The coefficients of a second order Bessel filter are

$$\begin{aligned} a_1 &= 1.3617 \\ b_1 &= 0.6180 \\ f_{g1} &= f_g = 1 \\ Q_i &= 0.58 \end{aligned}$$

For these coefficients, the internal gain α can be calculated to

$$\alpha = 3 - \frac{a_1}{\sqrt{b_1}} = 3 - \frac{1.3617}{\sqrt{0.618}} = 1.268$$

So if R_3 equals $1\,k\Omega$, $(\alpha - 1)R_3 = 268\,\Omega$.

Assuming a capacitance for $C_1 = C_2 = C$ of 82 pF and a cut-off frequency f_g of 1 MHz (this cut-off frequency still allows multiples of the baseband frequency of 424 kHz), the resistance of $R_1 = R_2 = R$ can be calculated by

$$R = \frac{\sqrt{b_1}}{2\pi f_g C} = \frac{\sqrt{0.6180}}{2\pi \cdot 1 \cdot 10^6 \cdot 82 \cdot 10^{-12}} = 1.526k\Omega$$

This dimensioning leads us to the circuit shown in figure 6.41.

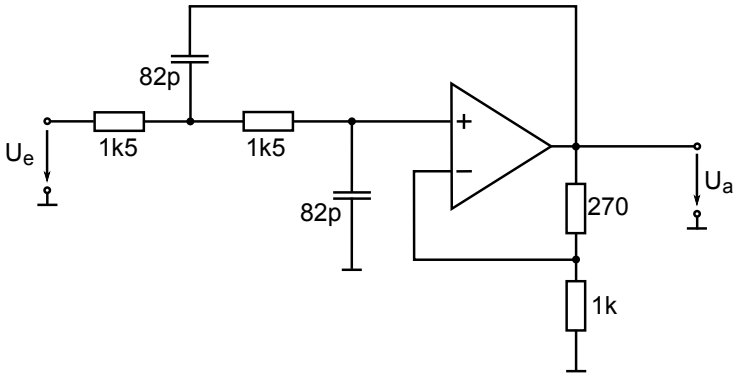


Figure 6.41.: Dimensioned Sallen-Key lowpass filter (modified from [16])

Figure 6.42 shows the simulation results for the calculated circuit. The all-over gain for low frequencies is, as calculated, about 1.2. The cut-off frequency is located at about 1 MHz, smaller deviations are resulting from the adjustment of the dimensioned resistors to the resistor standard series.

The damping of the 27.12 MHz signal part is

$$d = 20 \cdot \log \frac{0.0022}{1.2} = -54.7\,dB$$

in comparison to the 424 kHz signal.

This lowpass filter is applied twice in the receive path: once for the I-, and once for the Q-branch. For the realisation of the filter the operational amplifier AD8021 was chosen because of its possibility to do a phase adjustment. Very important for the circuit of the AD8021 are the smoothing capacitors for the supply lines. If these capacitors are neglected, the AD8021 tends to oscillations.

The input signals have to be centered around the 2.5 V supply, which serves as analog ground potential. This is done by an upstream highpass filter with a cut-off frequency of 140 Hz.

6.3.2.3. Amplifier

Before a further processing of the signal is carried out, the output of the lowpass filter is amplified since the signal levels at this stage are rather low and may fail in driving the input stages of the following processing circuits. For this reason, an amplification factor of 4, resp. 12.04 dB, was chosen (see equation 6.34).

$$A = 1 + \frac{R_f}{R_0} \tag{6.34}$$

$$= 1 + \frac{300}{100} = 4 \tag{6.35}$$

The circuit is composed as an ordinary non-inverting amplifier using the operational amplifier LT1819 from Linear Technologies. Figure 6.43 examplifies the used circuitry.

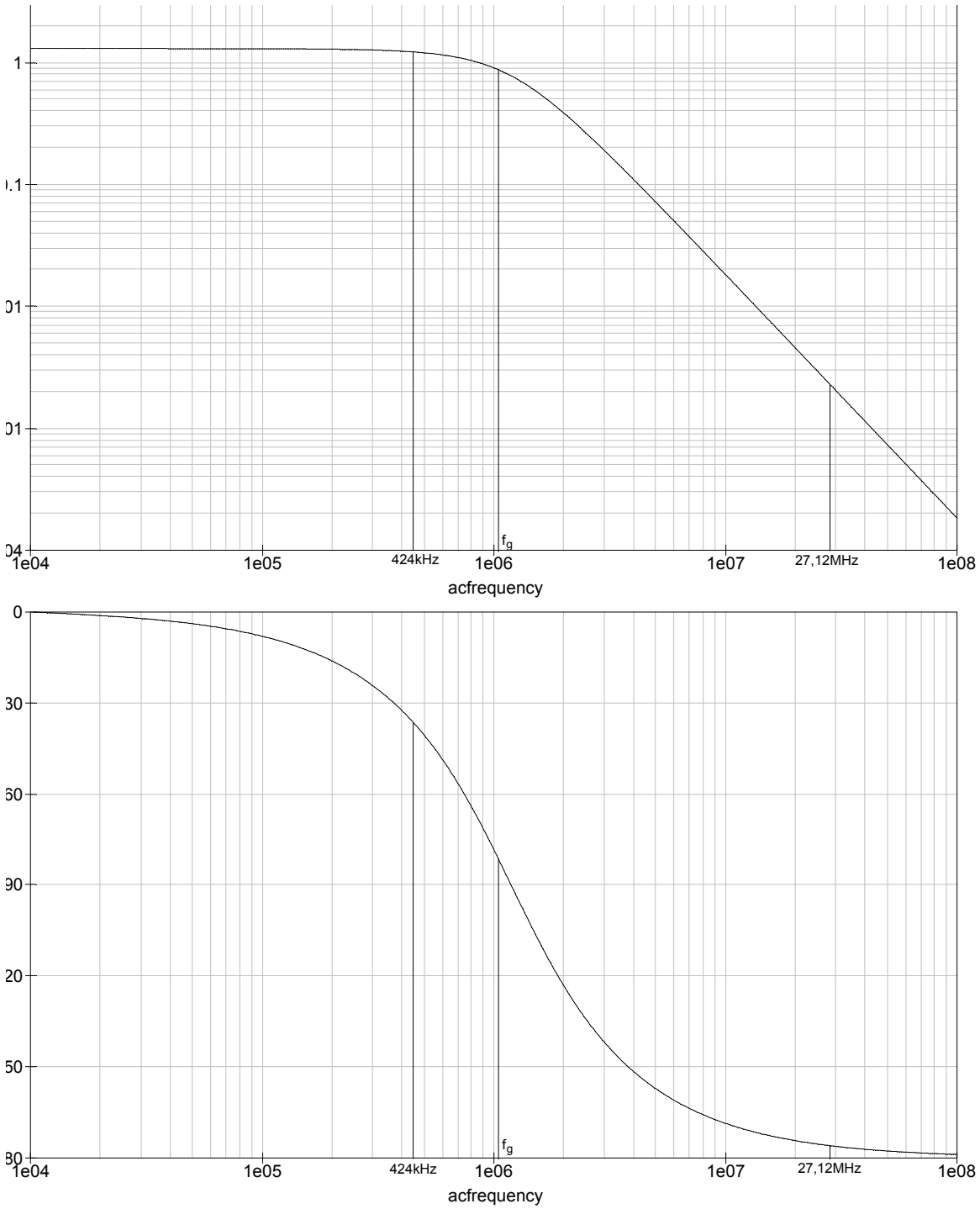


Figure 6.42.: Simulation result for dimensioned Sallen-Key filter

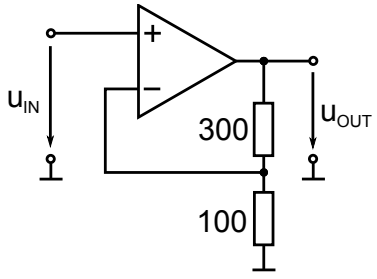


Figure 6.43.: Schematic diagram of the amplification circuit

Of course, the amplification is again carried out twice, once for the I- and once for the Q-channel (in parallel). The updated block diagram of the mode 1 receive path can be found in figure 6.44.

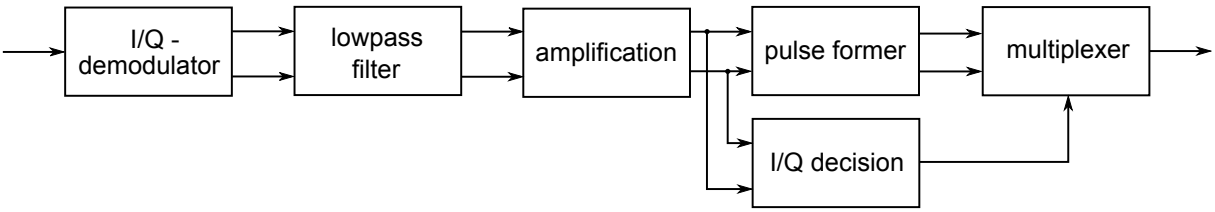


Figure 6.44.: Updated signal flow of the mode 1 receive path

6.3.2.4. Pulse Shaper

Until this point, the signals of the receive path were processed as analog signals. The next step is to feed the carrier-demodulated and filtered input signal into the Cortex-M3 microcontroller to do the subcarrier demodulation and the communication to the computer. But before that the signal has to be digitised. For this step, the pulse shaping unit shown in figure 6.45 was developed.

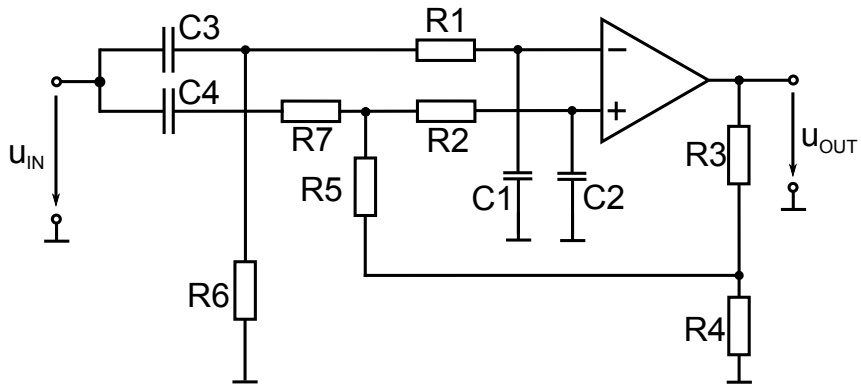


Figure 6.45.: Schematic diagram of the pulse shaping circuit

Since the (modulated) subcarrier is a rectangular waveshape, it generally consists of two states. Due to this fact, the modulated subcarrier can entirely be described by a one-bit signal.

This circuitry above operates in the following way: The incoming signal is split up in two paths which are processed with little differences, before the two paths arrive at the operational amplifier's inputs. The operational amplifier generally works in a comparator mode. Its output signals are therefore limited to the states of the positive and the negative operational amplifier supply. Straight before the positive and the negative input pins, there is in each case one high-pass filter (formed by R_1 and C_1 resp. R_2 and C_2) located to even the incoming signals and cancel out arising spikes. The cut-off frequency of the lowpass filters was chosen to be 1 MHz, and for the resistors 1 kΩ was selected. Therefrom, the value of the capacitance can be calculated by

$$\begin{aligned} C &= \frac{1}{2\pi f_g R} \\ &= \frac{1}{2\pi 10^6 1000} = 150\,pF \end{aligned} \tag{6.36}$$

C_3 in combination with R_6, and C_4 in combination with R_4, R_5 and R_7, are operating as high-pass filters. They cut off the constant component of the signal and balance it around the 2.5 V (analog ground) potential. Here, the difference between the two paths is realised. While the first path consists of one highpass and one lowpass filter, the second path features the two extra components R_4 and R_7.

To achieve a higher robustness of the pulse shaper against glitches and noise, the inverting output is attenuated (R_3 and R_4) and coupled back to the input path of the positive input signal. By this, the coupled analog ground level is varied for the positive input signal dependent on the state of the operational amplifier's output. A hysteresis is built which gives additional reliability of a sudden, unmeant switching of the operational amplifier's output. The magnitude of the hysteresis is calculated in equation 6.37.

$$\begin{aligned} h &= \frac{R_4}{R_3 + R_4} \cdot VCC \\ &= \frac{11\,\Omega}{1000\,\Omega + 11\,\Omega} \cdot 5\,V = 54.4\,mV \end{aligned} \tag{6.37}$$

Additionally, the amplitude of the second signal is varied to prevent a spontaneous switching of the operational amplifier's output in the high-state of the signal. This is done by the resistor R_7 which has the effect of a voltage drop in series in comparison to the voltage drop over R_4 and R_5. In contrast to the voltage drop over R_4 and R_5, a serial voltage drop will not abut on the positive input of the operational amplifier. Hence, the function of R_7 is to attenuate the amplitude of the second signal path. The amount of attenuation (damping) is calculated in equation 6.38, which says that the signal after the damping has an amplitude of 82.5 % of the input signal's amplitude.

$$\begin{aligned} d &= \frac{R_7}{R_4 + R_5 + R_7} \\ &= \frac{1\,k\Omega}{11\,\Omega + 4.7\,k\Omega + 1\,k\Omega} = 17.5\,\% \end{aligned} \tag{6.38}$$

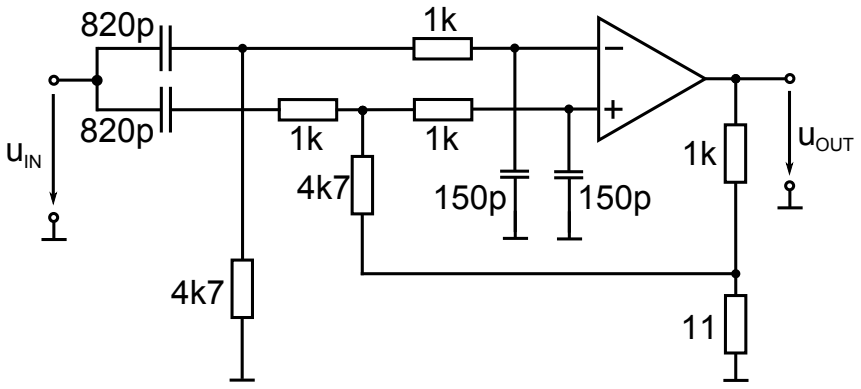


Figure 6.46.: Schematic diagram of the fully dimensioned pulse shaping circuit

In figure 6.47 you can find the simulation outputs of the pulse shaping unit. The input signal is a signal of an arbitrary amplitude and constant component. As you can see, the input signal

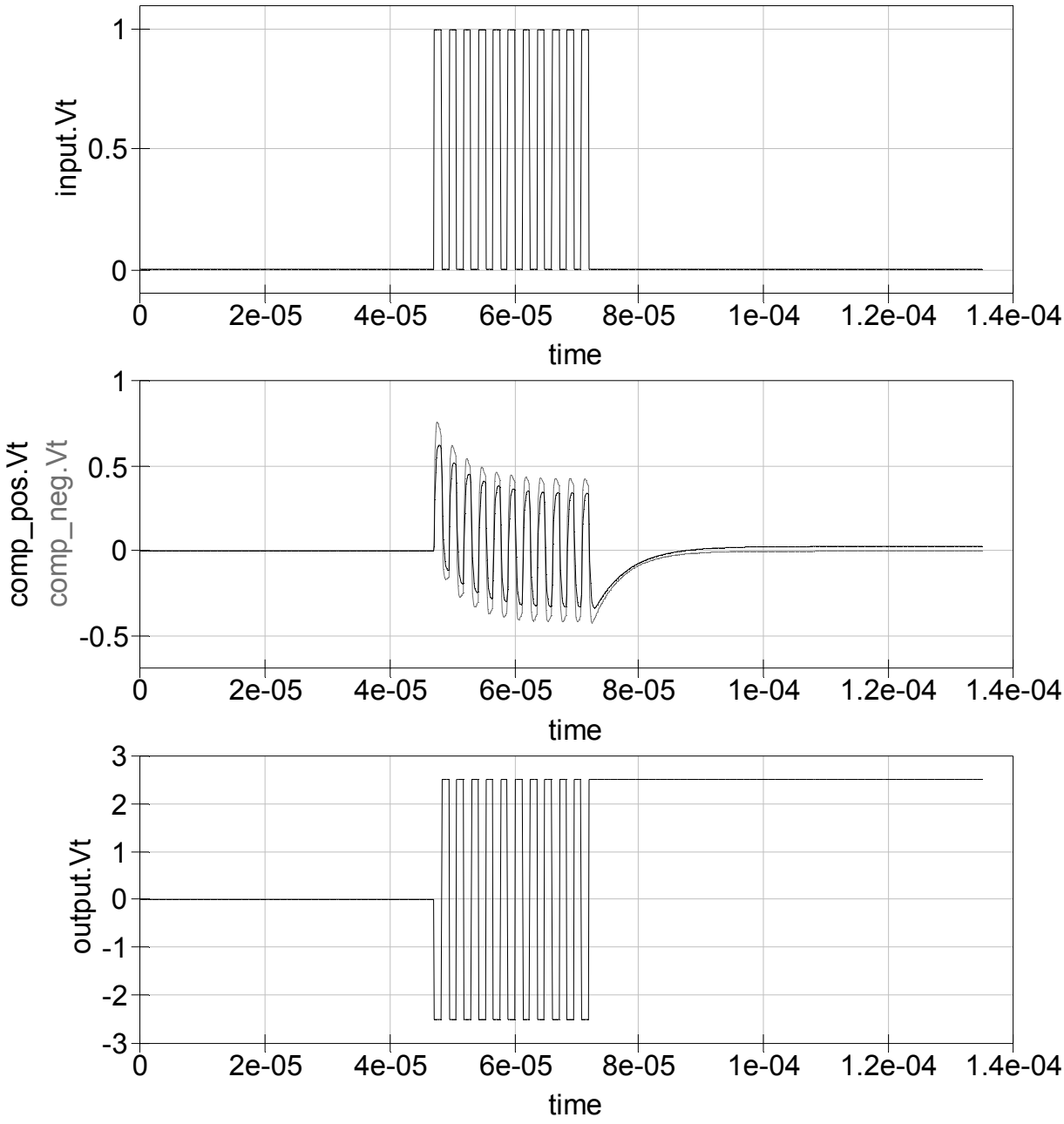


Figure 6.47.: Results of the simulated pulse shaper circuit

at the operational amplifier's positive input is attenuated and has, for zero input signal, a certain offset in comparison to the signal at the negative input pin.

It is not easy to find a suitable adjustment for the offset between the input for a DC input signal (this occurs when the subcarrier stops toggling). On the one hand, the offset has to be large enough to suppress a certain noise on the paths, on the other hand the offset may not become so large that effective switching operations can be missed.

This pulse shaping unit is again inserted twice into the reading device: Once for the I- and once for the Q- branch. Therefore, also two digitised output signals exist. Since there exists only one input into the microcontroller, in the next step an arrangement has to be found to forward the branch carrying the major signal and to block the branch comprising the inferior signal.

6.3.2.5. Channel Decision

Since the received signal was, up to this point, processed within two parallel signal branches, a decider that selects the branch holding the better performing signal has to be implemented. This channel decision unit shall, for the currently introduced approach, determine the signal with the higher signal energy. Therefor, first the signal has (if it is not already) to be centered around the analog ground signal (2.5 V). Then it has to be rectified and averaged (see figure 6.48). After this procedure, the signal with the higher signal energy carries the more negative voltage level (because of the inverting function of the rectifier). Therefore, in a final step the two signals are compared and the signal with the more negative voltage level indicates the channel with better signal quality.

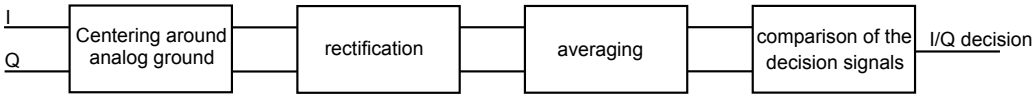


Figure 6.48.: Block diagram of the channel decision process

One important decision is the definition where to take a reading of the input signal. It has to be done on the one hand before the digitalisation of the signal, on the other hand already some processing of the input signals has to be done before (demodulation, filtering). For this implementation, the decision was made to get the signal directly from the amplifier's output.

The schematic diagram of the rectifier can be found in figure 6.49. In this case, a half-wave rectifier was chosen because of historical reasons, a further improvement of the circuitry for the future was to choose a full-wave rectifier circuitry to flatten the output and to ease the adjacent averaging of the signal. For the realisation of the rectifier, an LT1819 operational amplifier and BAS70-04W diodes were chosen after several combinatorial trials with different constellations between operational amplifiers and diodes. The challenge at this point was to develop a fast system by choosing diodes with low parasitic capacities and operational amplifiers with a high driving capability. The LT1819 and the BAS70-04W are perfectly colluding for rectification applications so it may be possible to consider this configuration also for a two-way rectification even up to frequencies of about 15 MHz.

One important item accounted for dimensioning of this rectification circuit is to select a low resistance value for the circuit resistors. This allows a quick reloading of the diode's parasitic capacitances and therefore enables the circuit to exhaust its potential as a fastly readjusting solution in terms of signal changes. For figure 6.49, the resistors R_1 and R_2 are dimensioned by equation 6.39. Since the incoming signal is already of a magnitude in the state of the optimum signal range, no further amplification is done in this stage.

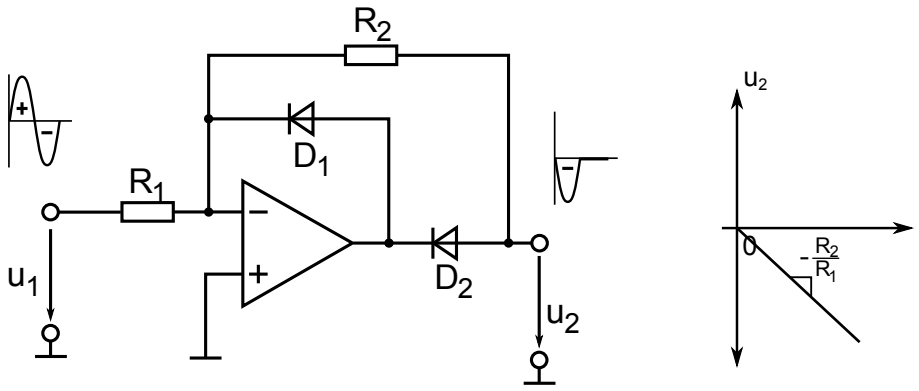


Figure 6.49.: Schematic diagram of a half-wave rectifier and amplification characteristic [9]

$$A = -\frac{R_2}{R_1} = -1 \tag{6.39}$$

$$\Rightarrow R_1 = R_2 = 50\Omega$$

You can find the signals associated with these calculations as oscilloscope screenshots in chapter 7.

Subsequent to the rectifier you can find a passive lowpass filter with a cut-off frequency of 720 Hz. It was decided to keep this frequency that low because an averaging over several subcarrier cycles is intended to occur. The input resistance of the lowpass filter is kept high to minimise the influence on the feedback current of the rectification circuit. Therefor, the value of the resistor was chosen to be 47 kΩ. You can find the dimensioning of this lowpass filter in equation 6.40.

$$\begin{aligned} C &= \frac{1}{2\pi f_b \cdot R} \\ &= \frac{1}{2\pi \cdot 720\,Hz \cdot 47\,k\Omega} = 4.7\,nF \end{aligned} \tag{6.40}$$

The components for these filters can be found as R_{37}, R_{38}, C_{48} and C_{49} in the schematics attached in appendix A. The two lowpassed signals are then fed into an LT1819 operational amplifier operating as comparator. In the assembled circuit, it was seen that the output of this comparator is still toggling too much to deliver a reliable decision signal, so one more lowpass filter was inserted behind the comparator output. Based on the block diagram shown in figure 6.48, one more lowpass filter and one comparator are added to produce a stable output signal (see figure 6.50).

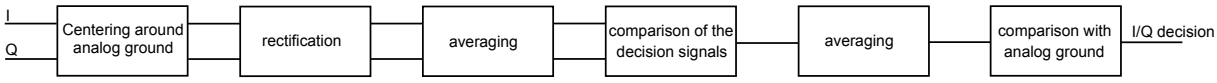


Figure 6.50.: Extended block diagram of the channel decision process

Since the output of the first comparator switches between 0 V and 5 V, the average for a symmetrical function would be 2.5 V resp. the analog ground level. By reason that the output of the first comparator is not exactly 2.5 V but tends to either 0 V or 5 V, the average of the output

is either lower or higher than the analog ground level. Because of this, the passive lowpass filter is added after the first comparator's output and the output signal of this filter is again fed into a comparator which checks this signal against analog ground. The lowpass filter's cutoff frequency is 96.4 kHz which leads to a capacity of 1.5 nF and a resistor of 1.1 kΩ. These components can be found in appendix A as C_{54} and R_{39}. R_{39} is, in this first version for test purposes, implemented as a potentiometer to vary the cut-off frequency of the filter.

All in all, the channel decision is held steady at the channel decision output at about 11 subcarrier periods after the start of receiving a VICC's respond. This duration is an acceptable delay since the start of frame (SOF) at the transmission from the VICC to the VCD contains a sequence of 24 subcarrier pulses which can be used for synchronisation purposes.

6.3.2.6. Multiplexer

The function of the multiplexer is to connect the path holding the superior signal (either I- or Q-branch) through to the microcontroller's response input. The challenge was in this case that the signal received from the channel decision may change during the reception of the VICC's response. If a multiplexer was used to switch the path, it would also acknowledge a branch change which can evoke an additional unwanted change of the signal's phase state. For this reason, a 'locking circuit' has to be implemented which impedes a change of the branch interconnection during a transmission procedure.

This problem was solved by passing the channel selection down to the microcontroller, which is able to appoint the desired channel only once at the beginning of the transmission and then leaves it unchanged for the rest of the time. As you can see in attachment A, the signal after the decision unit is directly sent to the microcontroller via *GPC8* (*CHANNEL_SEL*). After the eleventh incoming subcarrier pulse the microcontroller reads the CHANNEL_SEL signal and copies it to the *DATA_SEL* signal defined on pin *GPC7*. This signal controls the multiplexer via its SELECT-input. For illustration, refer to figure 6.51.

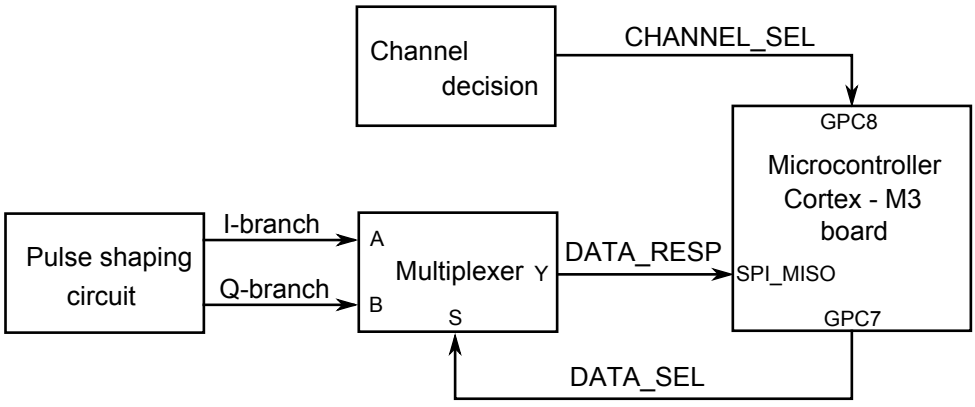


Figure 6.51.: Block diagram of the multiplexer embedded in the system

The multiplexer's output carries the digitised response signal of the superior signal branch. This signal is lead into the microcontroller through the pin *SPI_MISO* (*DATA_RESP*), where its processing is continued.

For the realisation, the multiplexer SN74LVC157AP was chosen. The advantage of this element is that it is a part of the LVC series and therefore can be controlled by the 3.3 V output level of the microcontroller. One disadvantage is that this component contains not only one, but four multiplexer gates, all controlled by the same *SELECT*-input pin. This means that the circuit board's area is not optimally utilized.

For mode 1, just gate A is used. A reuse of this integrated multiplexer IC can, for example, take place by using the gates of multiplexer B for the receive-signal of mode 2. For further information on this possibility, please refer to section 6.3.3.6.

6.3.2.7. Overall System Implementation

The voltage concept of the receive path complies to the concept of the transmit path. The digital component (74LVC157) is operated by 3.3 V and GND gained by the Cortex-M3 microcontroller board. The analog part (operational amplifiers and RF2713) are supplied by 5 V and GND. There exists, similar to the transmit path, an analog ground level which is set to 2.5 V, fixed by the voltage regulator already mentioned in section 6.2.2.7.

Additionally to the detailed explanation of the individual system parts in the instant chapter, a few notes are left to be stated. On the one hand, the RFMD2713 works best with an amplitude of about 300 mV (600 mV peak-peak) of the LO_INPUT pin's addressing signal. Since the 27.12 MHz signal received from the Cortex-M3 board has an amplitude of about 2 V (4 V peak-peak), a voltage divider was implemented (resistors R54 and R55) to damp the incoming signal.

Another remark recorded at this point is the location of the individual circuit units in the appendix. On the schematic page entitled *Receive Path I* you can find the RF2713 with its associated circuit, the two lowpass filters (for the I- and the Q-Path) composed of AD8021 operational amplifiers and the amplification unit utilising an LT1819 operational amplifier. On the schematic page entitled *Receive Path II*, the pulse shaping unit (upper part of the page), the channel decider (lower part of the page) and the signal multiplexer (on the right hand side) are chartered.

6.3.3. Receive Path for Mode 2

Representatively for the different channels available in mode 2, channel B with the subcarrier frequency of 1233 kHz was implemented in the developed reading device. The intention during the design of the signal processing path was to develop a system which is easily extendable for the additional implementation of the other stated channels as well. This extension shall be done by insertion of further signal processing paths in the reader's analog part according to the scheme of channel B, whereas especially filter adaption has to be handled. Furthermore, an adaption of the microcontroller's software has to be performed.

As for mode 1, the subcarrier demodulation and the decoding is done in the microcontroller. A difference between the resulting carrier-demodulated signals of mode 1 and mode 2 is the higher-frequency subcarrier of mode 2. The frequency of the subcarrier in the current mode is higher than the frequency the Cortex-M3 microcontroller is able to process. Because of this reason, only every fourth edge of the signal is processed. The subcarrier demodulation is carried out by time measurements and evaluation.

Since many characteristics of the received signal are quite similar to the input signal of mode 1, the same approach, namely the implementation by the use of an I/Q demodulator, is used. For the implementation of the receive path for mode 2 you will see that many parts of the system resemble the according parts of mode 1. Moreover, the I/Q demodulator of mode 2 is even shared with the I/Q demodulator of mode 1. Not till then the paths of the two modes are separated and treated unequally.

At the end of the processing string, the demodulation paths of the two modes have to be consolidated again because only one data input pin exists at the microcontroller which has to receive the carrier demodulated input signal of exclusively the one selected transmission mode. This is

done by the circuitry of two multiplexers. For further details on the multiplexer interconnection please refer to section 6.3.3.6.

In figure 6.52, a block diagram of the receive path is displayed. Due to the narrow bonding of the receive paths between mode 1 and mode 2, the signal processing path of mode 2 is depicted as an extension of the mode 1 receive path.

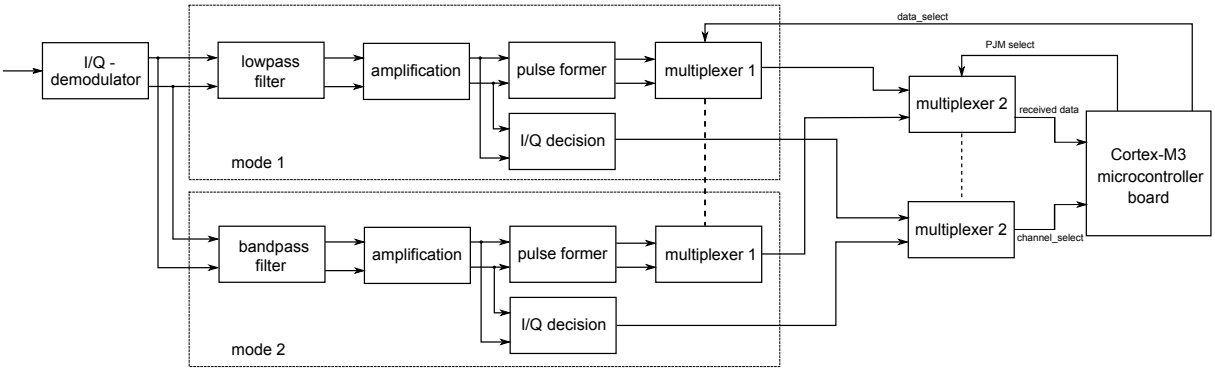


Figure 6.52.: Block diagram of the receive path as a combination of mode 1 and mode 2

Due to time reasons, the physical implementation of the mode 2 receive path was not done. Some blocks of this path are equal or similar to physically proven blocks of the mode 1 receive path, other blocks are just explained theoretically and supported by simulations.

6.3.3.1. I/Q demodulator

For mode 2, the selfsame I/Q demodulator as for mode 1 is used.

6.3.3.2. Bandpass Filter

The task of the bandpass filter is to boost the subcarrier frequency of the assigned channel. In the case of the instant thesis, channel B and therefore the frequency of 1.233 MHz has to be culled. Near by the frequencies of the other channels, especially the frequencies 969 kHz and 1.507 MHz of the adjacent channels A and C shall be suppressed as well as possible. In addition, the frequency part of 27.12 MHz (the double carrier frequency) shall be attenuated significantly.

The approach for the filter design was a bandpass filter with a single positive feedback loop according to [16] as shown in figure 6.53. Through the negative feedback by the resistors R_1 and (k-1)R_1, the inner gain is limited to the value of k.

For the derivation of the dimensioning provision, a first look has to be thrown at the general transfer function of a second order bandpass filter. It can be found in equation 6.41.

$$A(s_n) = \frac{(A_r/Q)s_n}{1 + \frac{1}{Q}s_n + s_n^2} \tag{6.41}$$

For the given filter, the transfer function reads as follows:

$$A(s_n) = \frac{kRC\omega_r s_n}{1 + RC\omega_r(3-k)s_n + R^2C^2\omega_r^2 s_n^2} \tag{6.42}$$

Equating the coefficients of 6.41 and 6.42 results in the dimensioning rules for the given bandpass shown in the equations 6.43 to 6.45.

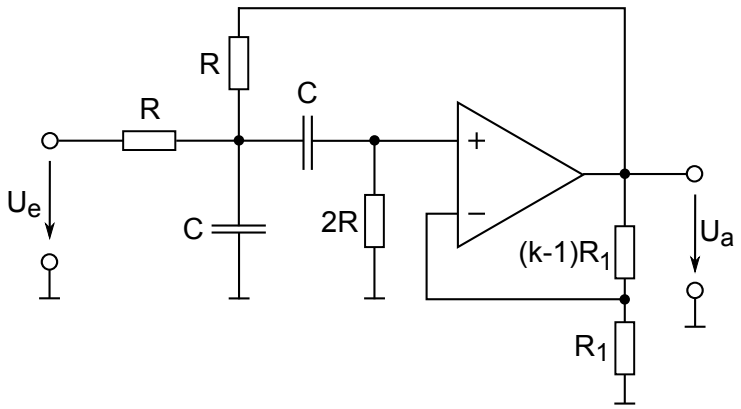


Figure 6.53.: Schematic of a bandpass filter with a single positive feedback loop (modified from [16])

$$\text{Resonance frequency: } f_r = \frac{1}{2\pi RC} \tag{6.43}$$

$$\text{Amplification: } A_r = \frac{k}{3-k} \tag{6.44}$$

$$\text{Quality: } Q = \frac{1}{3-k} \tag{6.45}$$

As you can see, a disadvantage of this bandpass realisation is that the quality Q and the amplification A_r cannot be chosen independently. Anyhow, the quality can be varied through modification of k without a coincidential change of the resonance frequency's value. Theoretically, for a k of 3, the amplification is virtual infinity. For this reason, the adjustment of the circuit becomes the more critical, the closer k converges to 3. In practice, an infinitely high amplification can, of course, not occur.

For dimensioning the bandpass, first the needed quality of the circuit has to be determined. The quality is defined as

$$\begin{aligned} Q = \frac{f_r}{B} &= \frac{f_r}{f_{max} - f_{min}} \\ &= \frac{1}{\omega_{n,max} - \omega_{n,min}} = \frac{1}{\Delta\omega_n} \end{aligned} \tag{6.46}$$

which leads us to a quality of

$$Q = \frac{f_r}{B} = \frac{1233kHz}{1356kHz - 1121kHz} = 5.23 \tag{6.47}$$

Basing upon equation 6.45, the k-factor and by that R_1 and (k-1)R_1 can be calculated (and picked from E24 standard row) to

$$\begin{aligned} k &= 3 - \frac{1}{Q} = 2.81 \\ \Rightarrow R_1 &= 1.5k\Omega \\ \Rightarrow (k-1)R_1 &= 2.7k\Omega \end{aligned} \tag{6.48}$$

For a chosen capacity of C=100 pF, the value of the resistors R can be established

$$R = \frac{1}{2\pi f_r C} = 1.29\,k\Omega \xrightarrow{E24} 1.3k\,\Omega \tag{6.49}$$

Based on these calculations, a simulation has been done. The result can be found in figure 6.54.

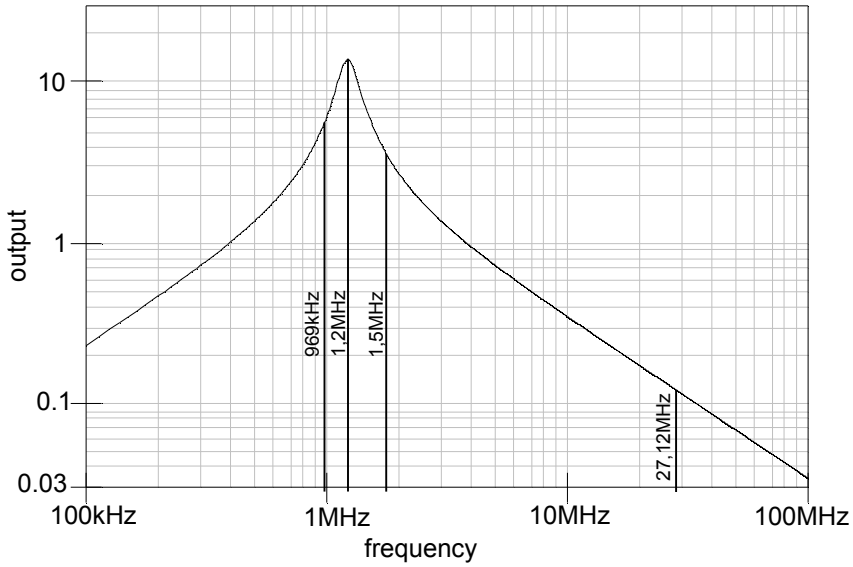


Figure 6.54.: Simulation result of the dimensioned bandpass filter for channel B

The calculated gain at the resonance frequency is

$$A_r = \frac{k}{3-k} = 14.8 \tag{6.50}$$

The gain values received from the simulation are summarized in table 6.6

frequency	**gain (out/in)**	**damping (f/f_r)**
969 kHz	5.3	7.8 dB
1233 kHz	13	0 dB
1507 kHz	3.3	11.9 dB
27.12 MHz	0.12	40.69 dB

Table 6.6.: Bandpass amplifications and damping for several selected frequencies

Before the signal is fed into the bandpass filter it has to be assured that it is centered around the analog ground signal (2.5 V). This is done in exactly the same way as in mode 1, namely by inserting a passive lowpass filter between the I/Q demodulator's output and the bandpass filter's input. Its cut-off frequency is chosen to be 140 Hz.

6.3.3.3. Amplification

The amplification is implemented identically to mode 1. For further information, please refer to section 6.3.2.3.

6.3.3.4. Pulse Shaper

Generally, the pulse shaper for mode 2 is composed pursuant to the concept of the pulse shaper in the mode 1 receive path. All the protective mechanisms against glitches and noise are perpetuated. The only modification at this stage is the alteration of the cut-off frequency of the lowpass filter prior to the operational amplifier's input. The new cut-off frequency is 2.9 MHz which leads us to the new resistance value calculated in equation 6.51.

$$\begin{aligned} R &= \frac{1}{2\pi f_g C} \\ &= \frac{1}{2\pi \cdot 2.9 \cdot 10^6 \cdot 150 \cdot 10^{-12}} \\ &= 365\,\Omega \qquad \xrightarrow{E24} 360\,\Omega \end{aligned} \tag{6.51}$$

The new pulse shaping circuit can be found in figure 6.55, the simulation results are presented in figure 6.56.

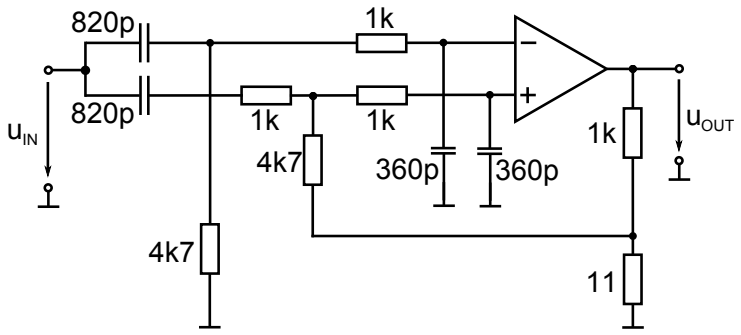


Figure 6.55.: Pulse shaper schematics for mode 2

For mode 2, the pulse shaping procedure is less susceptible to faults than the pulse shaping operation for mode 1. This results from the different coding of the subcarrier signal. While in mode 1 the subcarrier toggling is regularly interrupted (because of Manchester encoding), there are no interruptions at all in mode 2 because of the use of BPSK modulation for the subcarrier. Since most of the failures occur during the subcarrier toggling pauses, the pulse shaping process becomes more stable by the novel coding technique.

6.3.3.5. Channel Decision

For the channel decision it is similar to that of the other blocks in the demodulation path: For the channel decision unit in mode 2 there is a strong analogy to the channel decision unit of mode 1. The block diagram from section 6.3.2.5 (figure 6.57) is still unreservedly valid.

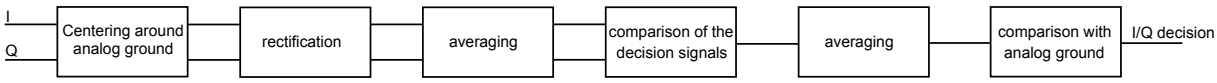


Figure 6.57.: Block diagram of the pulse shaping unit

Differences in the design just occur in the two averaging blocks. All the other blocks remain unchanged: The centering of the input signal around the analog ground level is still implemented

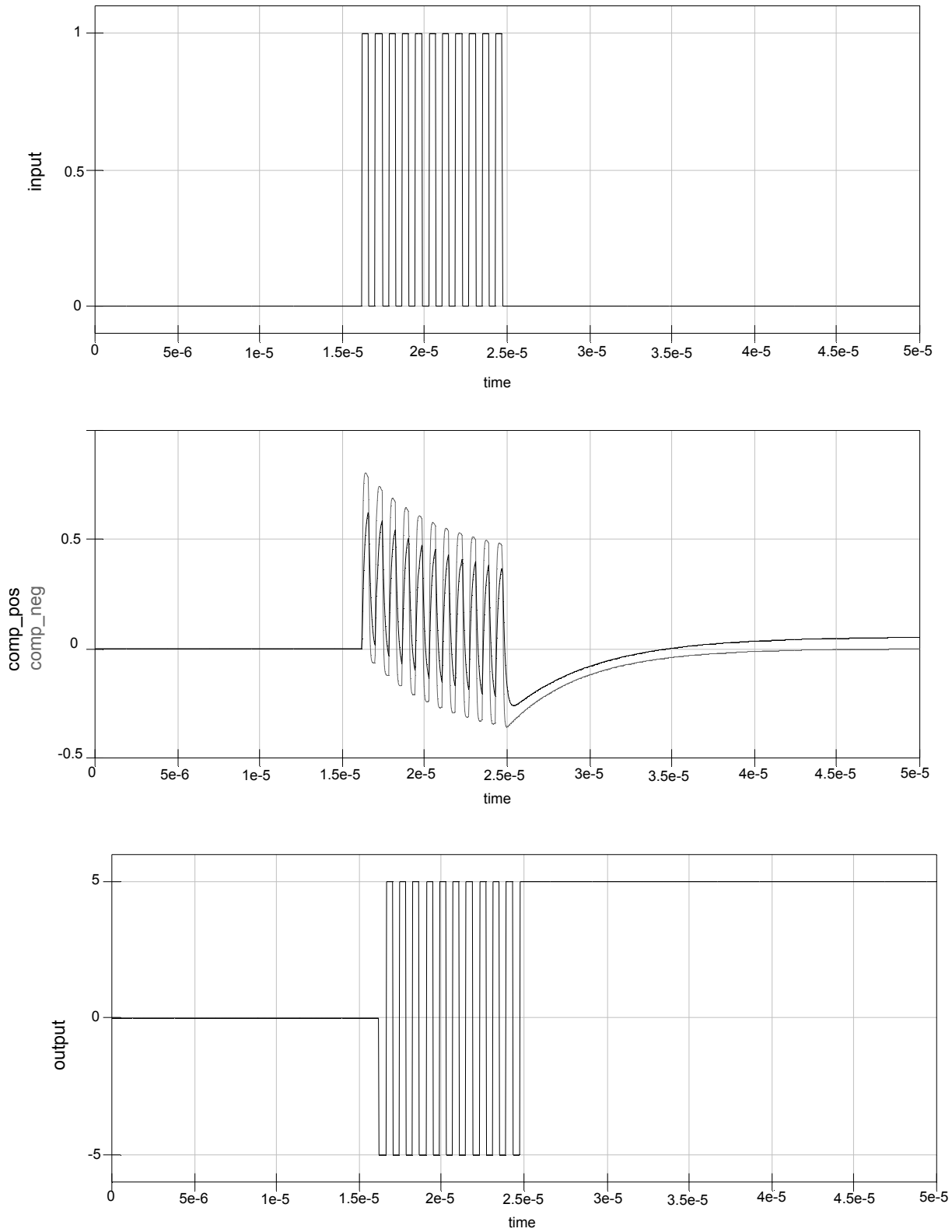


Figure 6.56.: Simulation result of the pulse shaper for mode 2

by a passive highpass filter, the rectification unit from mode 1 is already physically proved up to 15 MHz, and the comparator-interconnected operational amplifiers work well for mode 2 either.

After the subcarrier frequency has changed from 424 kHz in mode 1 to 1233 kHz in mode 2, the cut-off frequencies of the lowpass filters have to be adapted. Based on the cut-off frequency of 720 Hz of the first filter in mode 1, the new cut-off frequency is derived to

$$\begin{aligned} f_{g1,mode2} &= f_{g1,mode1} \cdot \frac{f_{sub2}}{f_{sub1}} \\ &= 720\,\text{Hz} \cdot \frac{1233\,\text{kHz}}{424\,\text{kHz}} = 2094\,\text{Hz} \end{aligned} \tag{6.52}$$

When leaving the resistor's value unchanged by 74 kΩ, the new value of the lowpass capacitor amounts to

$$\begin{aligned} C_1 &= \frac{1}{2\pi f_{g1,mode2} \cdot R_1} \\ &= \frac{1}{2\pi 2094\,\text{Hz} \cdot 74\,\text{k}\Omega} = 1.6\,\text{nF} \end{aligned} \tag{6.53}$$

Furthermore, the second lowpass filter also has to be adapted. This is done by the same method as for the first filter.

$$\begin{aligned} f_{g2,mode2} &= f_{g2,mode1} \cdot \frac{f_{sub2}}{f_{sub1}} \\ &= 96.4\,\text{kHz} \cdot \frac{1233\,\text{kHz}}{424\,\text{kHz}} = 280\,\text{kHz} \end{aligned} \tag{6.54}$$

For the calculation of the capacitance, the value of the resistor stays the same:

$$\begin{aligned} C_2 &= \frac{1}{2\pi f_{g2,mode2} \cdot R_2} \\ &= \frac{1}{2\pi 280\,\text{kHz} \cdot 1.1\,\text{k}\Omega} = 516\,\text{pF} \xrightarrow{E24} 510\,\text{pF} \end{aligned} \tag{6.55}$$

For the implementation of the second lowpass filter in the first prototype it was advantageous to implement the resistor R_2 as potentiometer, because the exact adjustment for an undisturbed output signal can be done best by a practical approach. The reason for that is that the input signal is difficult to emulate mathematically and therefore theoretical calculations are not very conducive.

The output of the channel decision block can be tapped after the second bit of the synchronising string of the transmission protocol from transmissions from VICC to VCD.

6.3.3.6. Multiplexer

For mode 2, the multiplexer system of mode 1 is expanded. For the choice between the I- and the Q-branch, gate B of the multiplexer used for this decision of mode 1 can be used. The activation of the multiplexer's input stays the same (DATA_SEL via GPC7 - see figure 6.58).

The state of DATA_SEL is determined, like for mode 1, by copying the state of CHANNEL_SEL at the beginning of the transmission from the VICC to the VCD. In contrast to mode 1, this copying needs not to be done in a hurry because of the longer synchronising string (9 bits of valid MFM data) in comparison to mode 1. A reasonable option was to copy the signal state 2 bits after the transmission from VICC to VCD started.

Since two gates of the first multiplexer are used, two outputs of this multiplexer may hold a valid response signal. Because only one mode can be used simultaneously, one additional multiplexer has to be inserted between the first multiplexer's output and the microcontroller's data input to interconnect the response signal of the currently used mode. The select pin of this second multiplexer can be accessed by the PJM_SIG signal which we already know from the modulator section (6.2.2.1). This signal carries the information whether mode 1 or mode 2 is used at the moment.

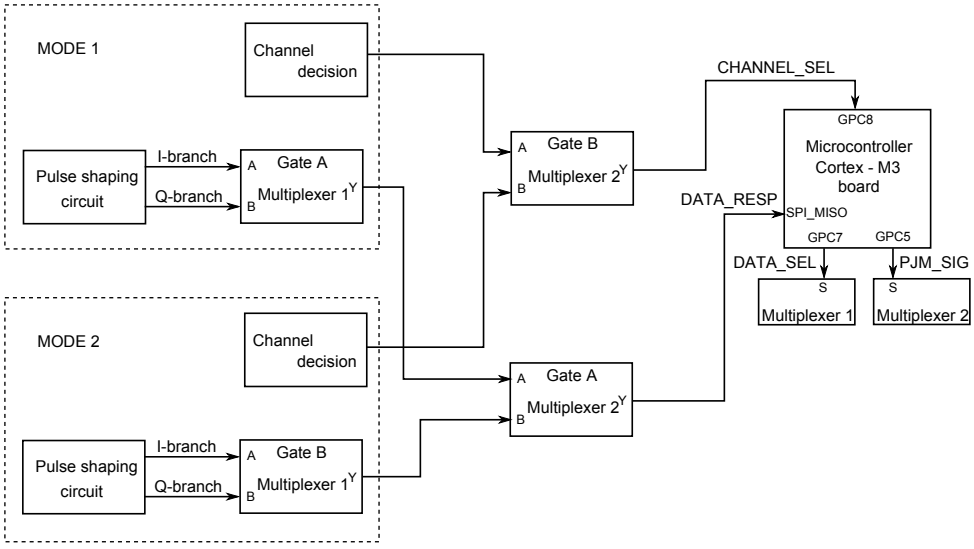


Figure 6.58.: Block diagram of the multiplexer system combining mode 1 and mode 2 in one reader

One further item to bear in mind is that by the use of two modes, also two different channel decision units are in use. Of course, also for the output signals of these channel decision units the decision on the correct mode has to be made. Simplifying for this demand is the fact that the same signal (PJM_SELECT) can be used for the interconnection of the right channel decision unit as is used for the choice of the received VICC response. This means that for this function simply gate B of the second multiplexer may be used.

6.3.3.7. Overall System Implementation

Due to time reasons, no physical implementation of the second mode's receive path took place.

Chapter 7

Verification Results of the Entire System

7.1. Modulation

7.1.1. Clock Generation

The 13.56 MHz oscillator works on a frequency of 13.56 MHz and an amplitude of 4.88 V. The rise time of the positive edge amounts to 2 ns, as denoted in the datasheet of the 74LVC04AD inverting gate.

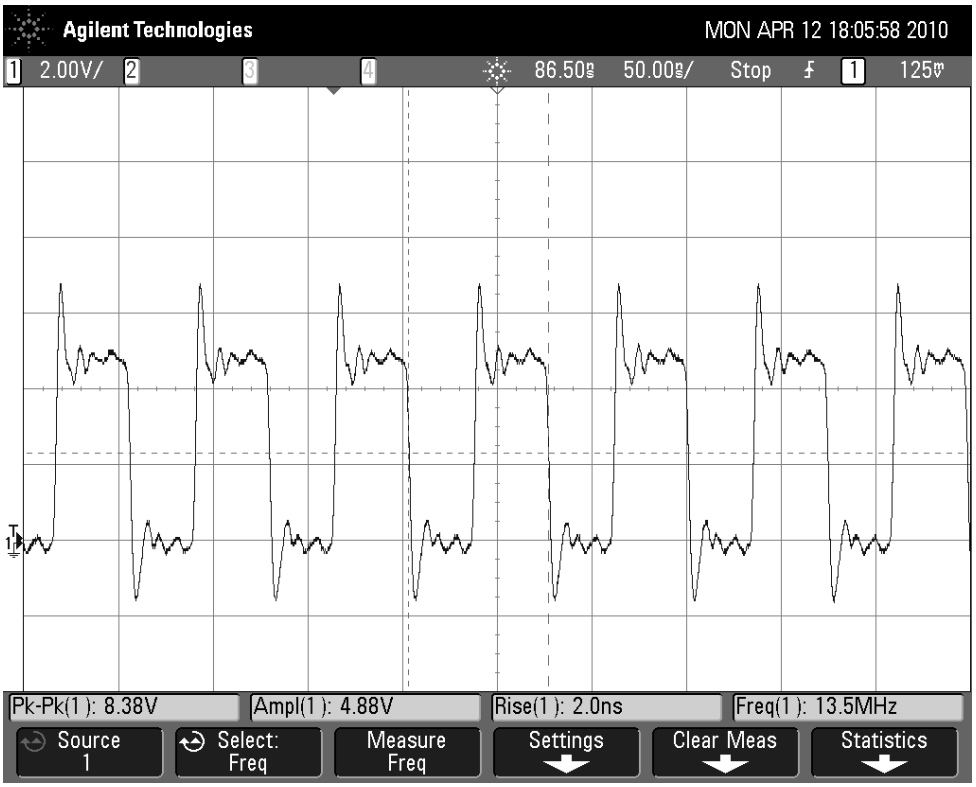


Figure 7.1.: Output of the 13.56 MHz oscillator

7.1.2. Buffer Output

Figure 7.2 shows how the clock signal is switched to pass or block, depending on the value of the data signal. In this figure, the upper signal constitutes the data waveform, while the lower signal corresponds to the switched clock signal.

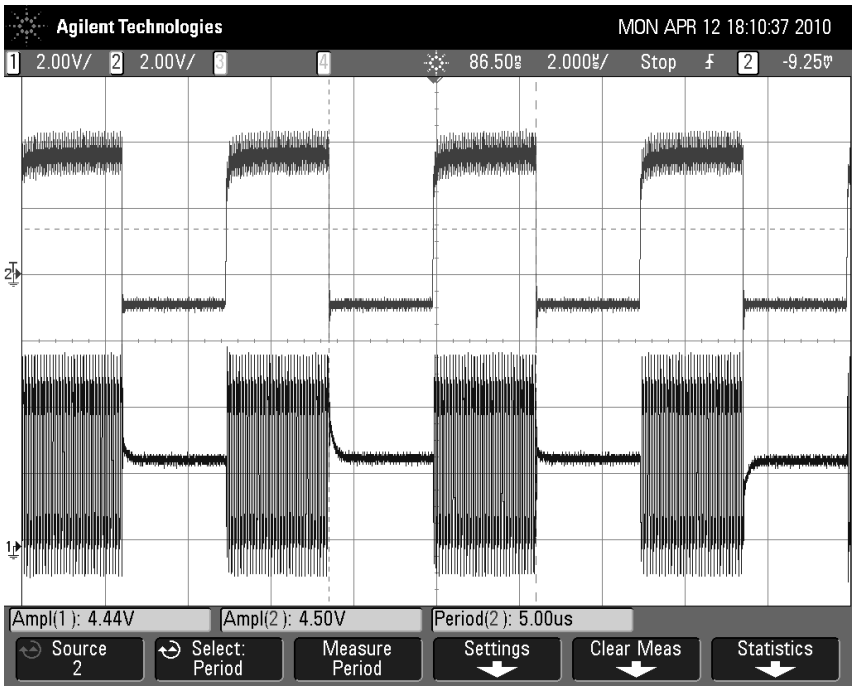


Figure 7.2.: Output of a buffer which is switched by data

The delay between the actuation of the enable pin and the activation of the gate's output amounts to 32 ns (see figure 7.3).

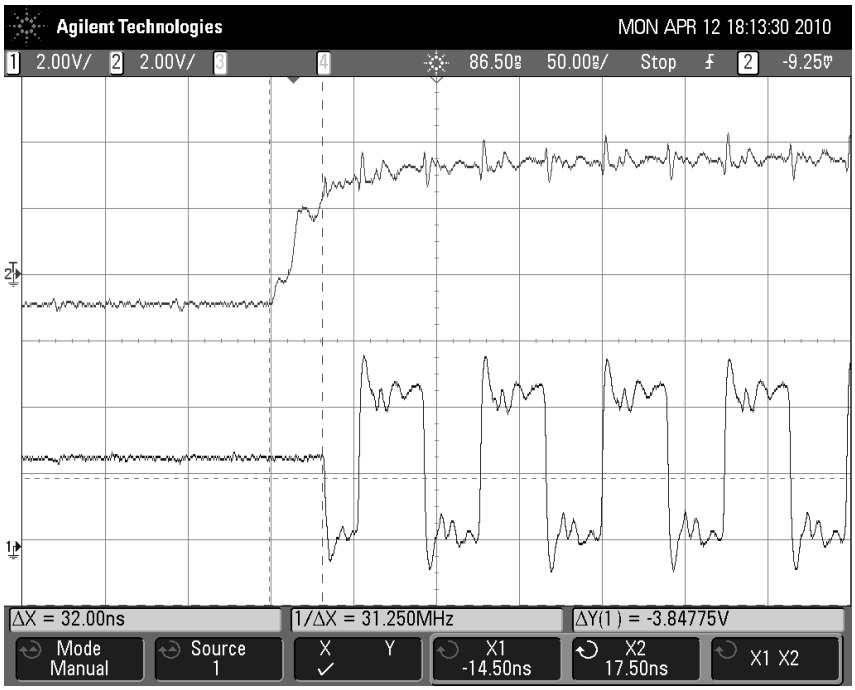


Figure 7.3.: Output of a buffer which is switched by data

7.1.3. Output of the second order lowpass filter

The following pictures show the outputs of the lowpass filters. The first two figures depict one output representative for all three of the 180pF lowpass filters, the subsequent figures compare the two PJM filter outputs.

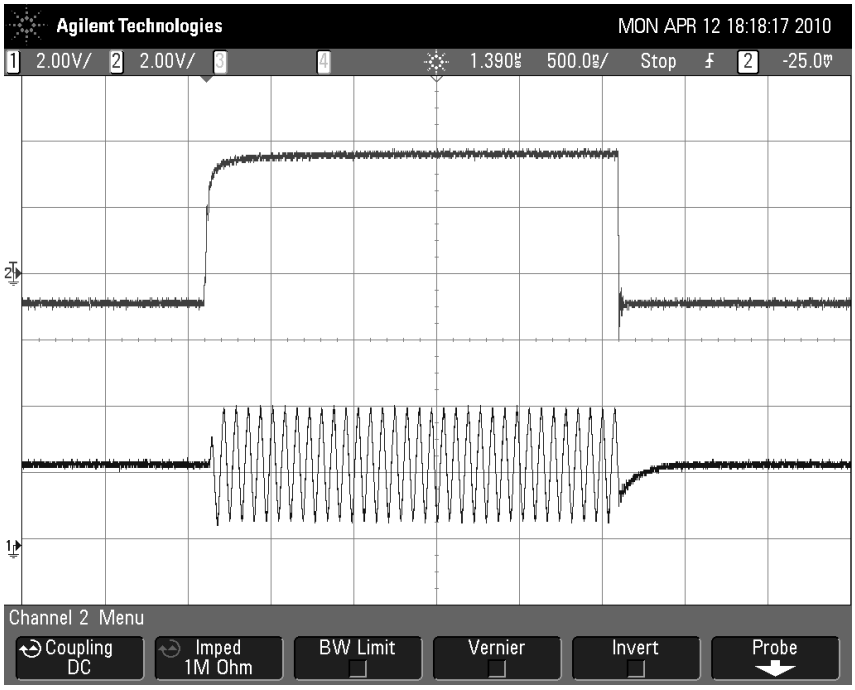


Figure 7.4.: Output of one 180 pF lowpass filter corresponding to the data signal

Figure 7.5 shows the output of the designed lowpass filter including the 180 pF capacity.

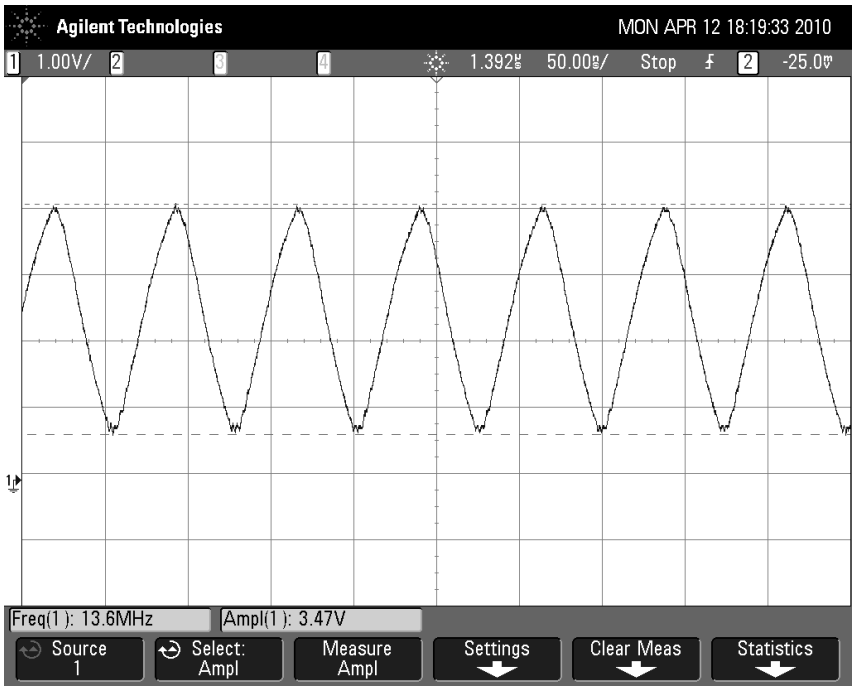


Figure 7.5.: Wave shape of the 180 pF lowpass filter output

In figure 7.6, the lowpass filter outputs between branch3 and branch4 are juxtaposed. In this illustration channel 1 of the oscilloscope corresponds to the LPF output of the modulator's branch3 and channel 2 corresponds to the LPF output of branch4. The amplitudes of these outputs are differing because of the varying attenuations accompanying the unequal phase shifts generated (see chapter 6.2.2.4).

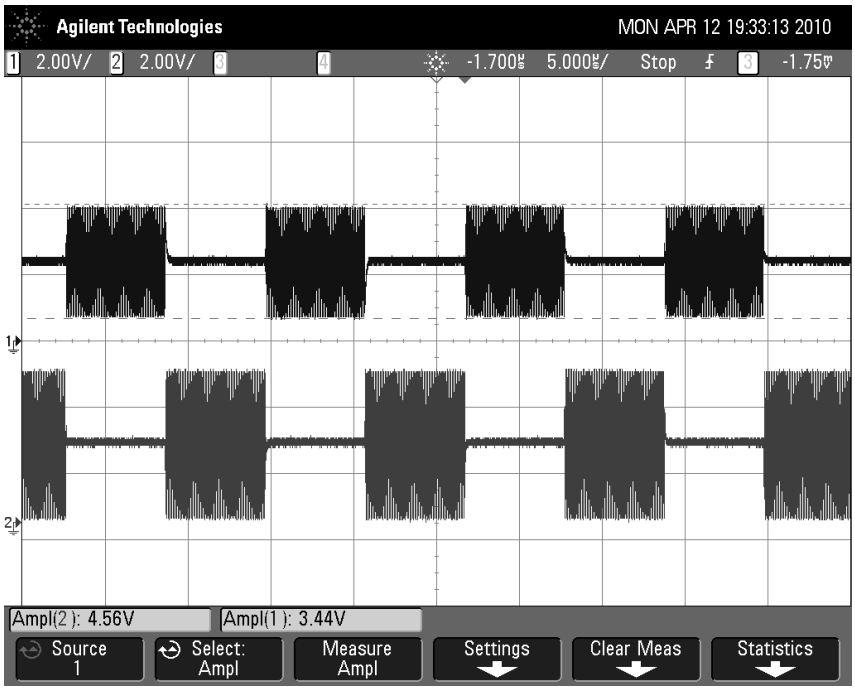


Figure 7.6.: Output of the two PJM lowpass filters

Figure 7.7 strings the LPF of branch3 and branch4. It becomes obvious, that for elimination of amplitude variations at the summed output different gain factors have to be chosen (see 6.2.2.5).

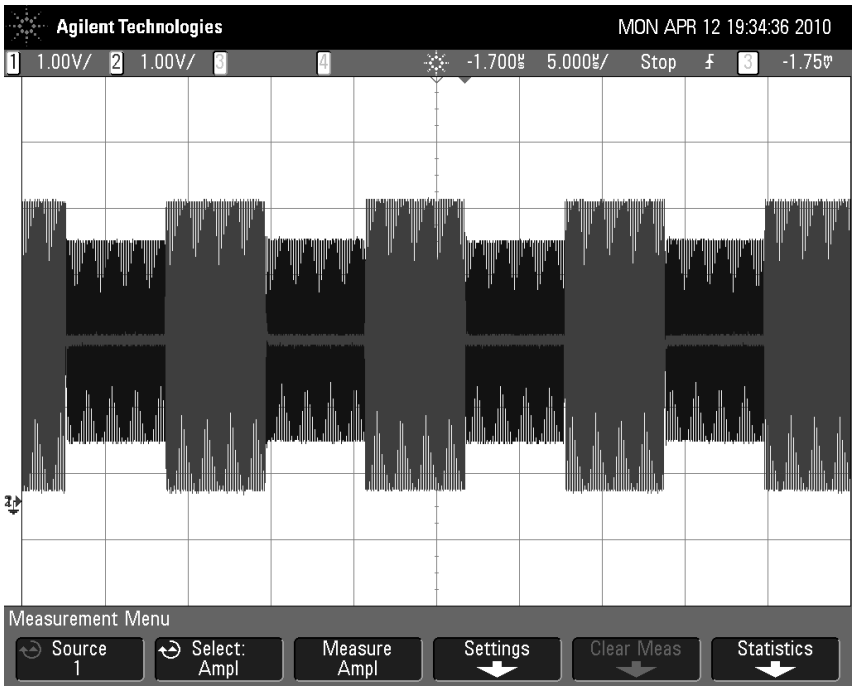


Figure 7.7.: Output of the two overlapped PJM lowpass filters

In figure 7.8 the phase transition (signal overlapping) has been zoomed in.

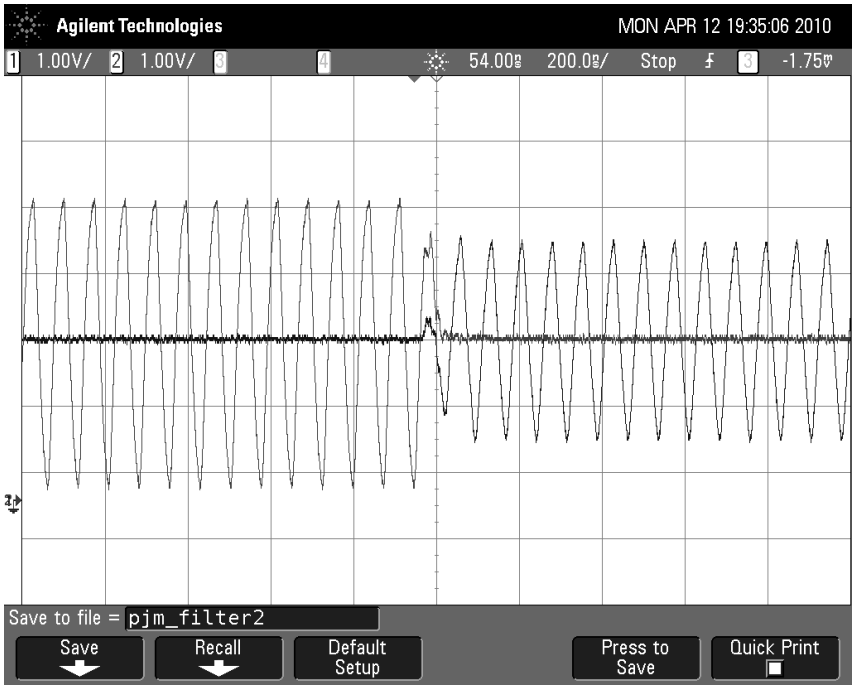


Figure 7.8.: Phase transition of the two overlapped PJM lowpass filters

7.1.4. Output of a 100 % modulation without antenna

In this chapter the overall output of the modulator, but without attached antenna, is recorded.

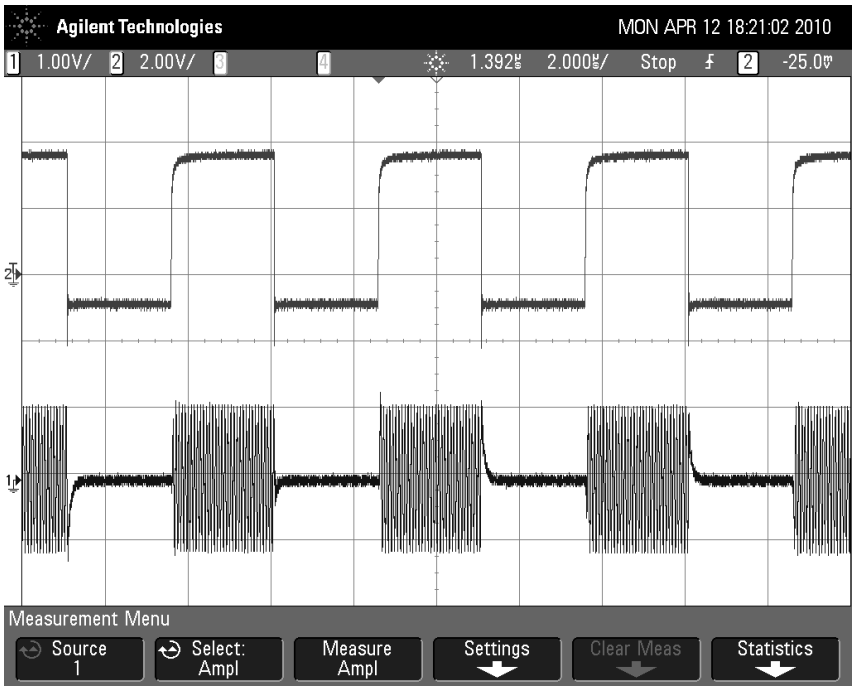


Figure 7.9.: Output of a 100 % modulation

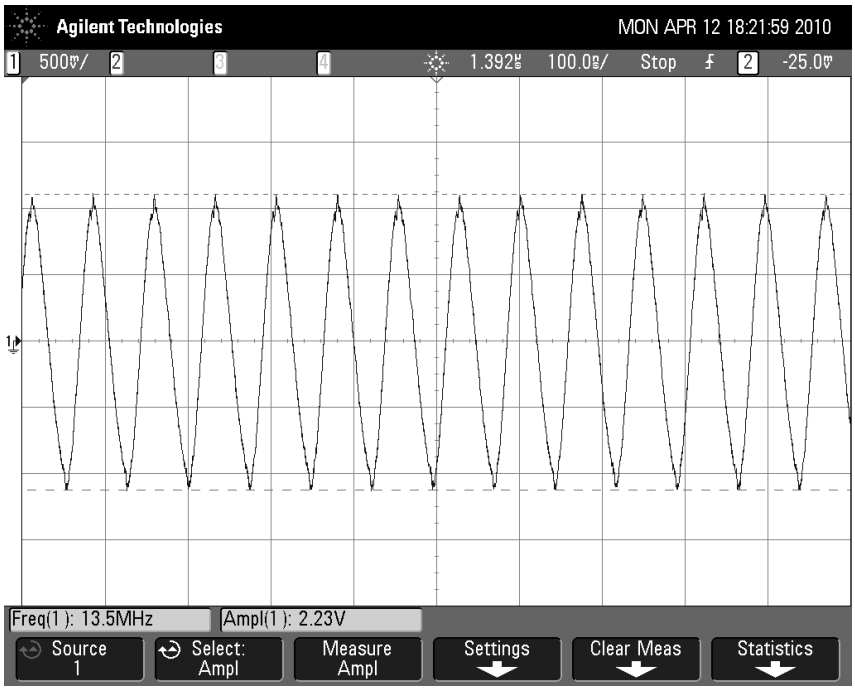


Figure 7.10.: Waveform of a 100 % modulation

Figure 7.11 shows the transient oscillation behaviour of the modulator output from the full amplitude to the theoretical zero amplitude. The required time amounts to about 200 ns.

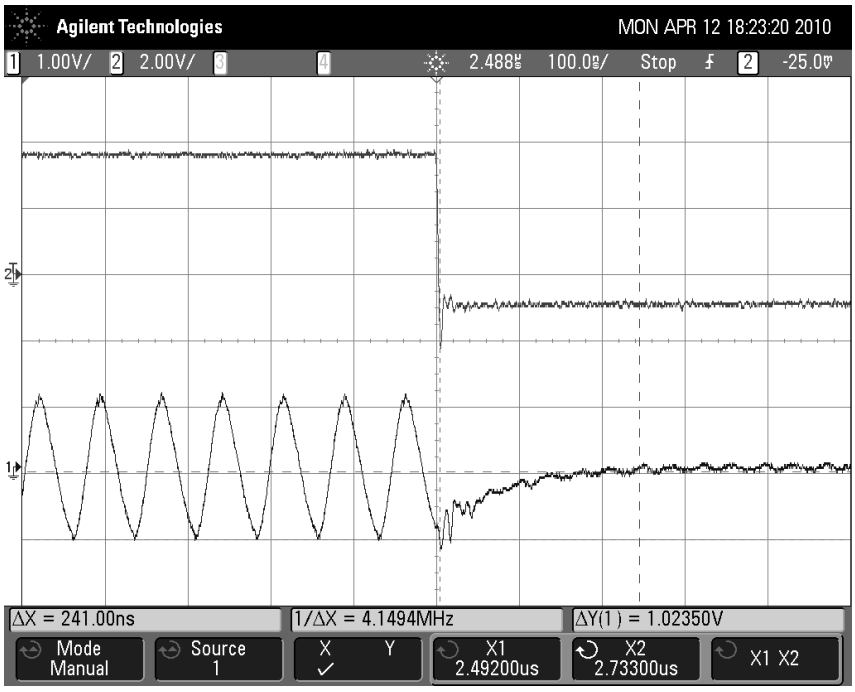


Figure 7.11.: Output of a 100 % modulation in comparison to the received data signal

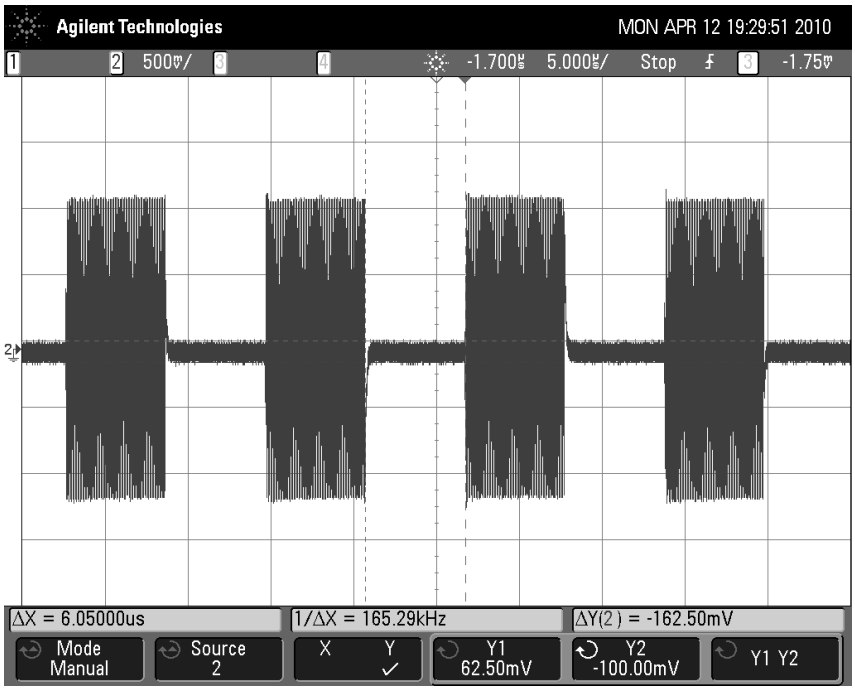


Figure 7.12.: Output of a 100 % modulation

These wave shapes are not yet the final wave shapes, they will be lowpassed afterwards with the use of the antenna.

7.1.5. Output of a 10 %-Modulation without antenna

Figure 7.13 shows the overall output of the 10% modulation circucitry.

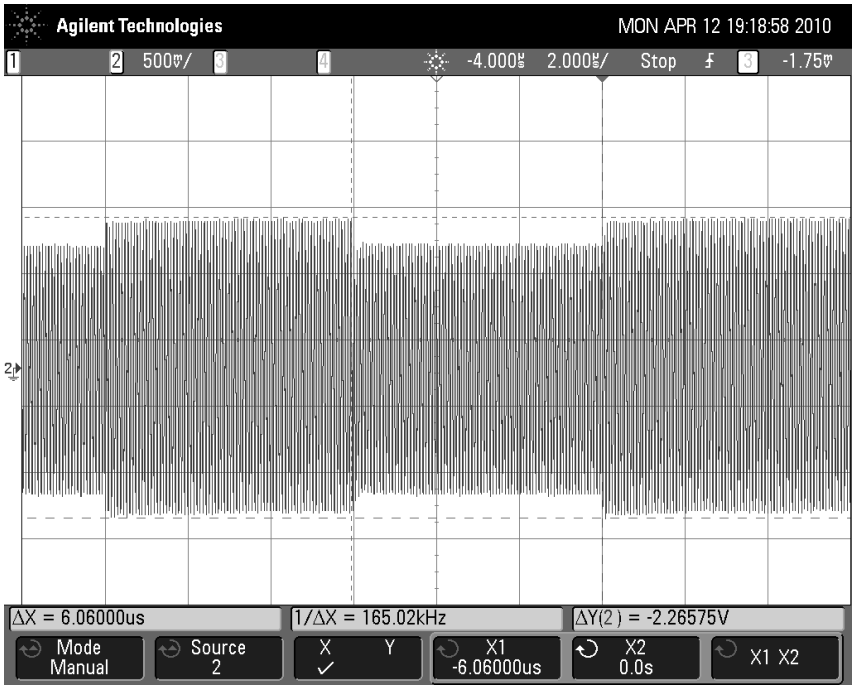


Figure 7.13.: Output of a 10 % modulation

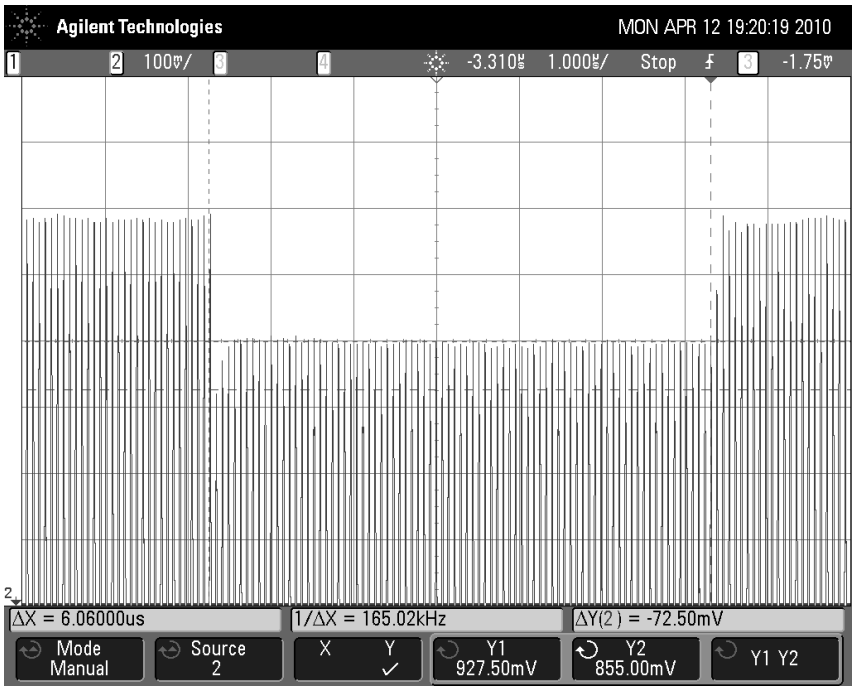


Figure 7.14.: Undershoot at the 10 % modulation

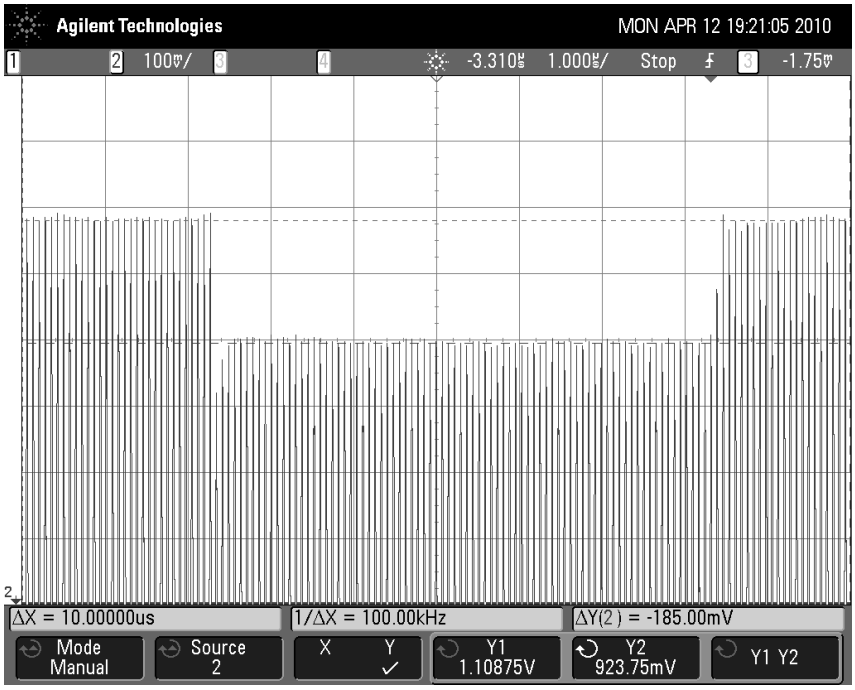


Figure 7.15.: Potential difference at the 10 % modulation

These wave shapes are not yet the final wave shapes, they will be lowpassed afterwards with the use of the antenna.

7.1.6. Output of a PJM signal without antenna

In figure 7.16 the output of the summing unit vs. the data signal gained from the Cortex-M3 board is shown. You can see transient effects correlative with the switching activities of the data

signal. These effects will be eliminated in a large part after attaching the antenna to the output driver (bandpass filter).

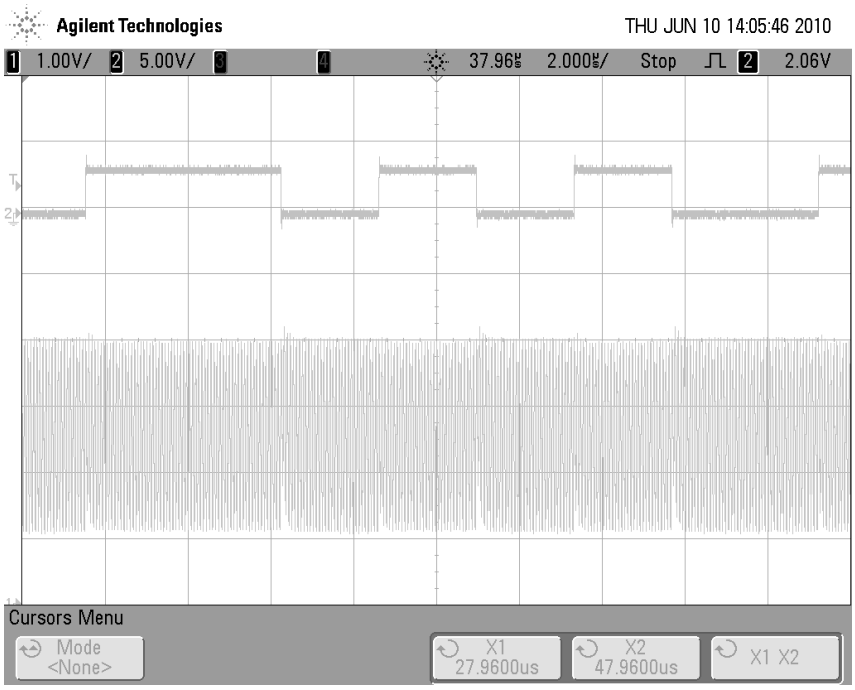


Figure 7.16.: PJM modulation

Figure 7.17 shows a switching activity in detail.

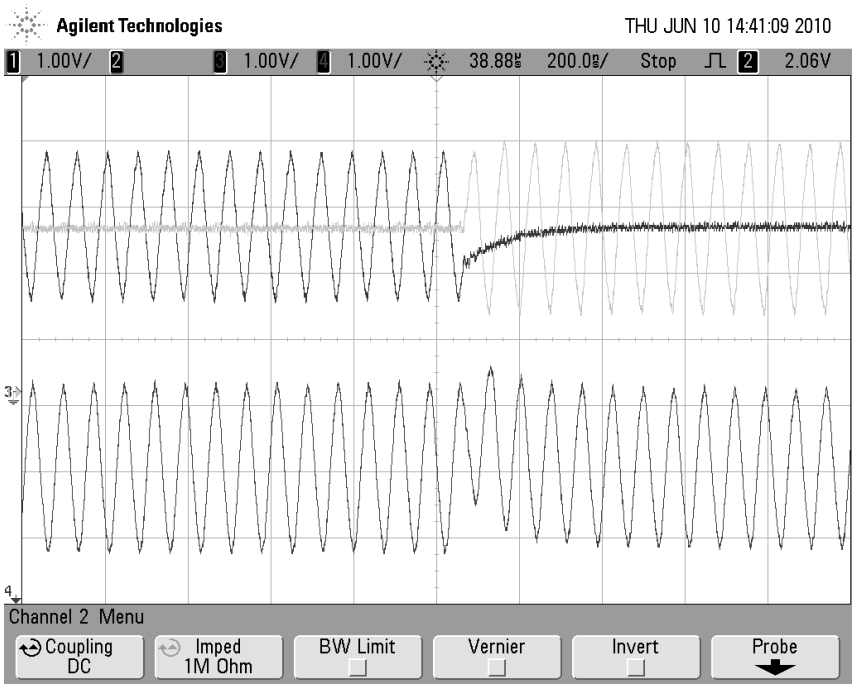


Figure 7.17.: PJM modulation single switch

Figure 7.18 shows the summing unit's output in comparison to the lowpass filter outputs of the signal branches 3 and 4. As you can see, the differences in the amplitude between the signals are nearly compensated in this stage. A further smoothing of the wave shape will be done by attaching an antenna to the output driver.

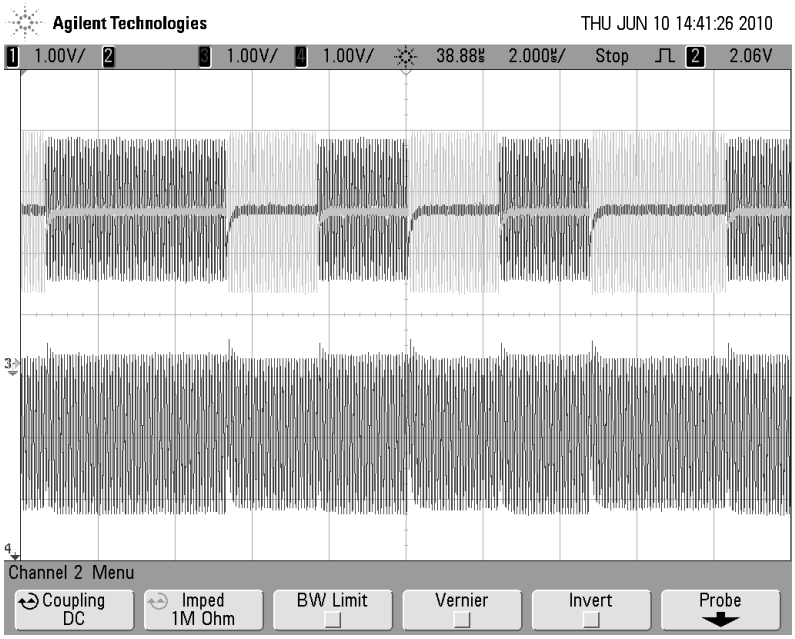


Figure 7.18.: PJM modulation composed of lowpassfiltered waveforms

7.1.7. Output of a 100 % modulation with antenna

In the following subchapters the transmitted magnetical field of the reader is illustrated by the use of an additional test coil whose induced voltage is displayed on the monitor of an oscilloscope. This test coil is located in parallel to the CSPC antenna with a minimum pitch between the two antennas.

Figure 7.19 shows the measured magnetic field produced by the modulator in combination with the adjusted antenna.

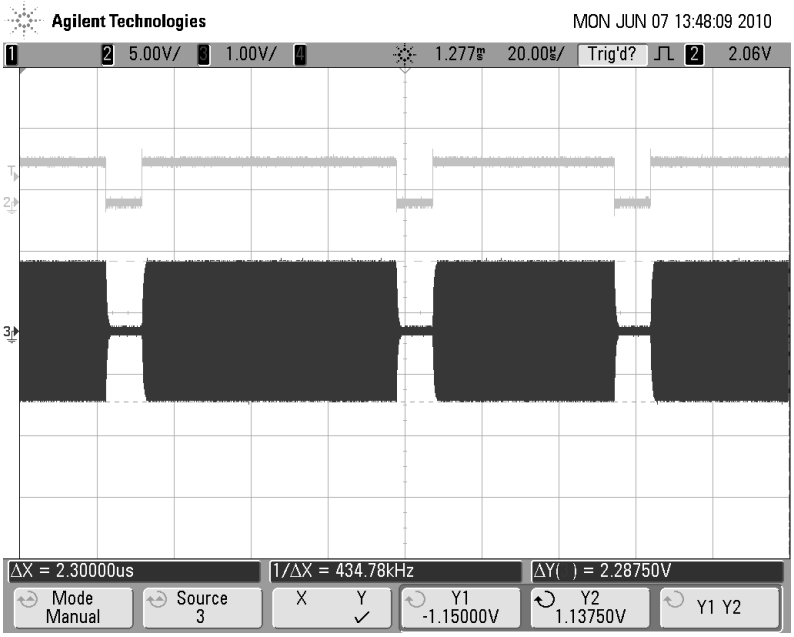


Figure 7.19.: 100 % modulation

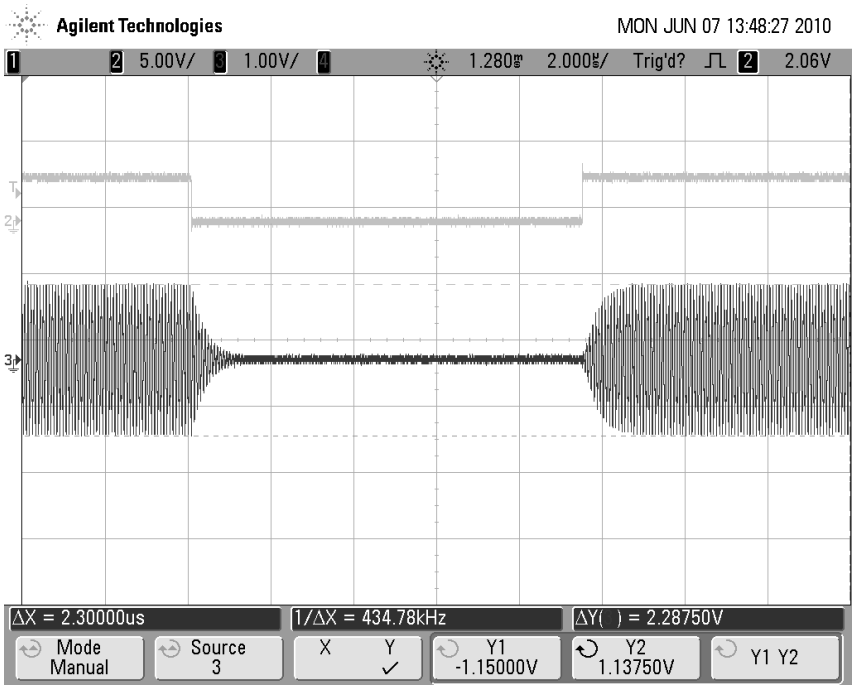


Figure 7.20.: 100 % modulation single state

As you can see, the settling time is now longer than without attached antenna and amounts to about 1 µs. The field strength gained is up to 2.516 A/m (factor 1.1 between the voltage measured to the field strength obtained).

Figure 7.24 shows the transponder response on the request sent in the figures 7.19 and 7.20.

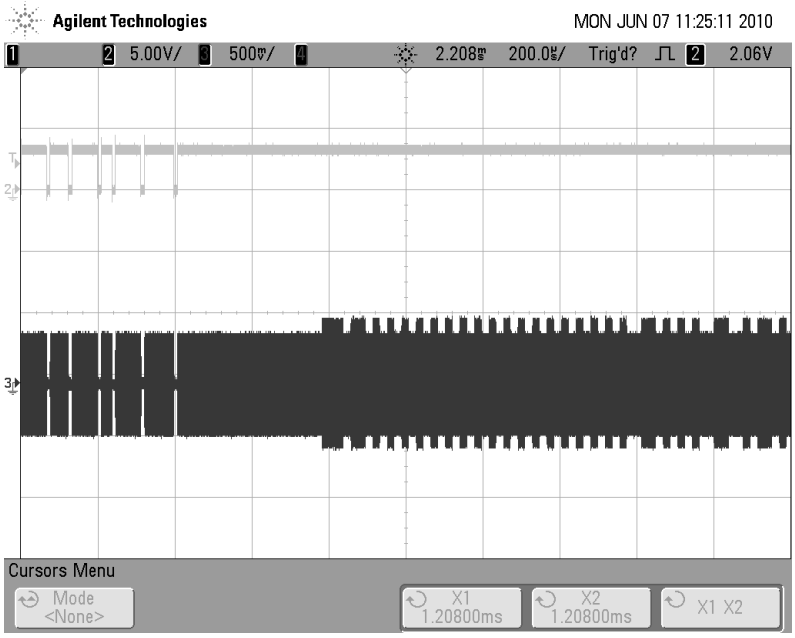


Figure 7.21.: Response of the transponder on a 100 % modulation

7.1.8. Output of a 10 % modulation with antenna

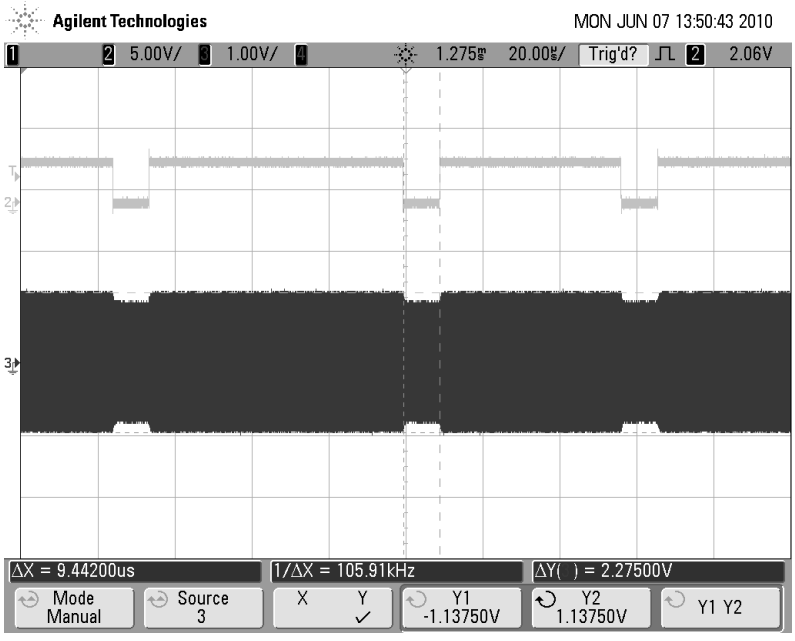


Figure 7.22.: 10 % modulation

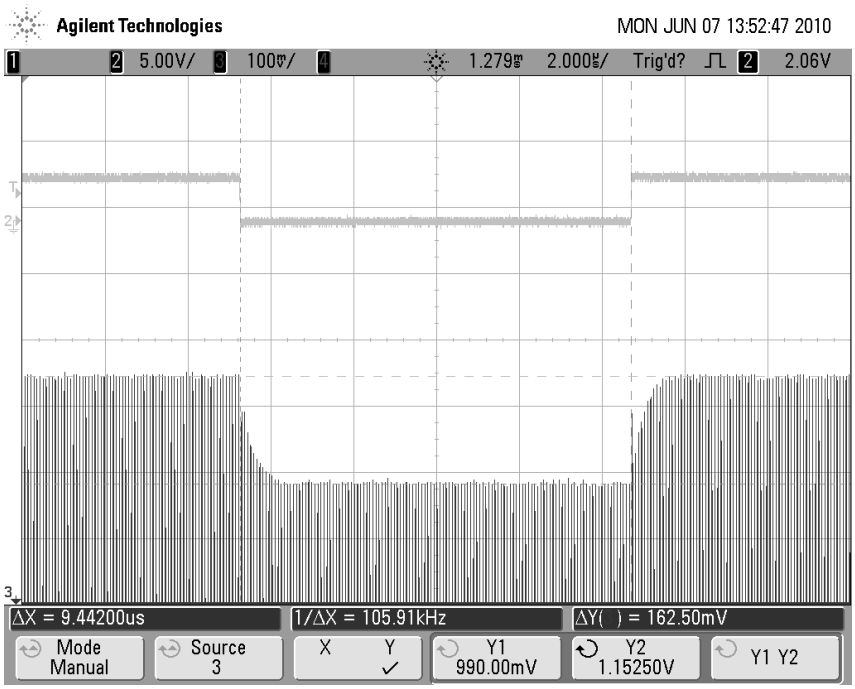


Figure 7.23.: 10 % modulation single switch

The transient effect in the switching point takes, in this case, about 0.7 µs.

In figure 7.24, you can see the request of the VCD and subsequently the response of the VICC.

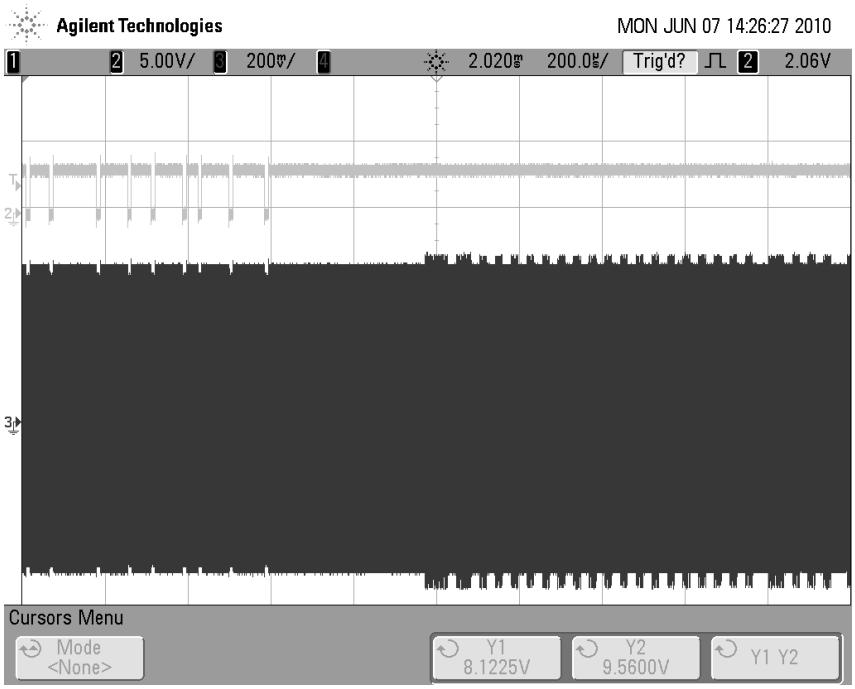


Figure 7.24.: Response of the transponder on a 10 % modulation

7.1.9. Output of a PJM signal with attached antenna

The topmost wave shape of figure 7.25 shows the coded data received from the Cortex-M3 circuit board. Below you can find the outputs of the sine curve smoothing filters. At the bottom the waveform of the transmitted magnetic field is depicted.

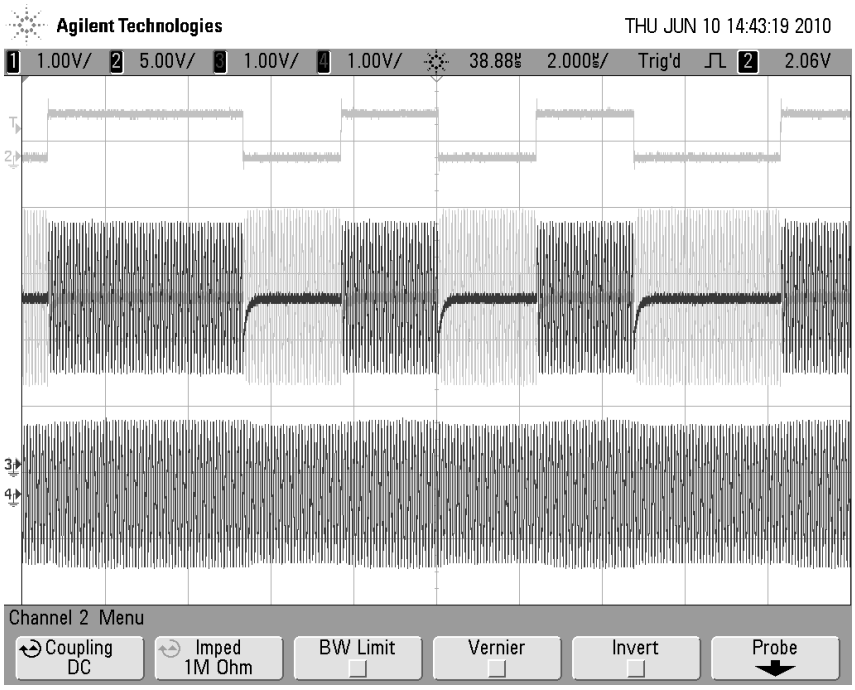


Figure 7.25.: PJM modulation

In figure 7.26 one single switch is taken out of the reader's request.

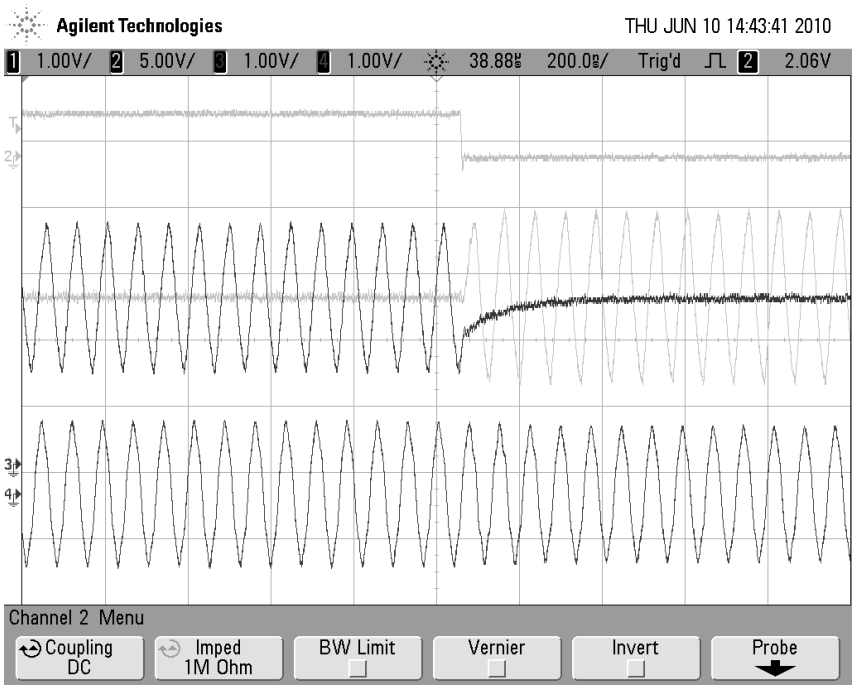


Figure 7.26.: PJM modulation single switch

7.2. Demodulation Mode 1

7.2.1. Transponder response

Figure 7.27 shows an optimal received transponder response. The amplitude is not in each case modulated as optimal as it is shown in this figure.

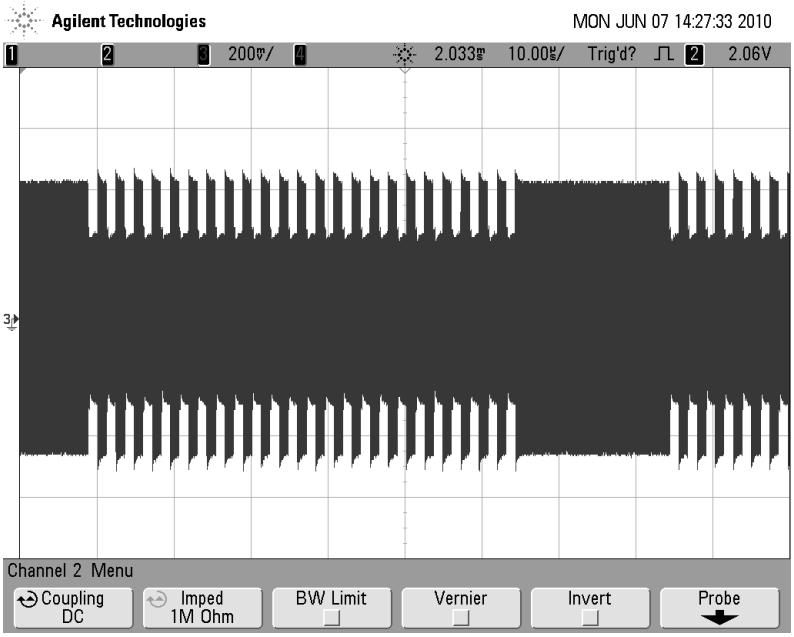


Figure 7.27.: Response of the transponder - mainly amplitude modulated signal

An alternative received transponder response is shown in figure 7.28. In this case the most part of the response signal is modulated on the carrier by phase modulation.

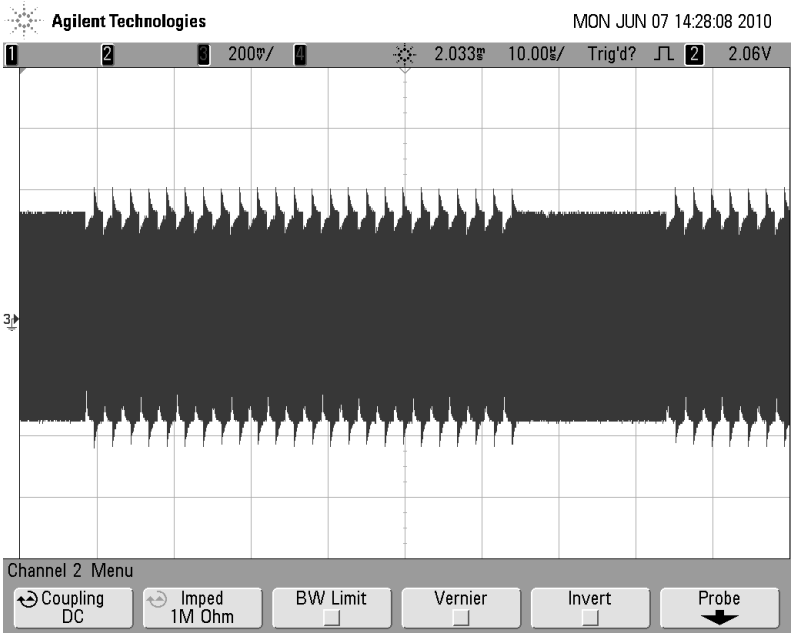


Figure 7.28.: Response of the transponder - mainly phase modulated signal

7.2.2. I/Q-Demodulation

Figure 7.29 shows the outputs of the I/Q demodulator RF2713. The upper channel (channel 4) represents the I channel, whilst the lower channel represents the Q channel.

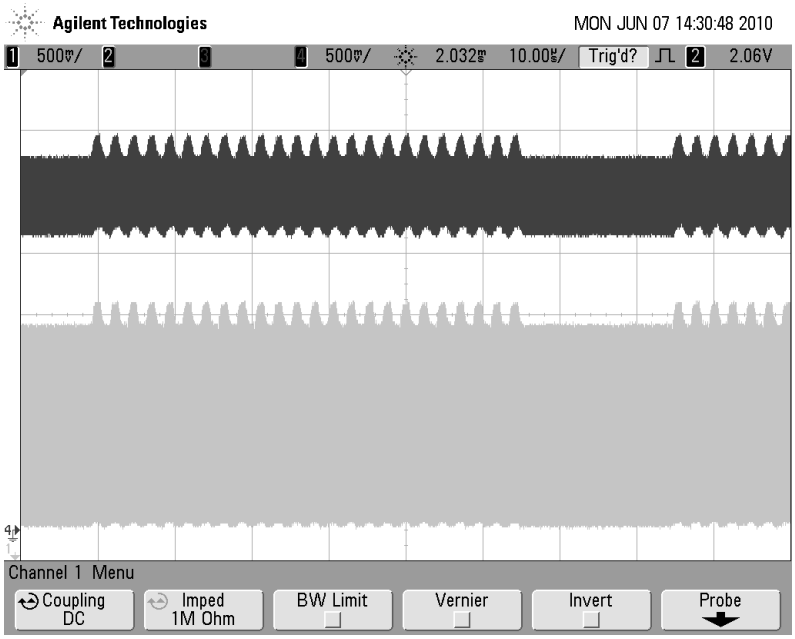


Figure 7.29.: Output signal of the I/Q demodulator

7.2.3. Filter

Figure 7.30 shows the filtered, demodulated I and Q channel signal tapped on the input pin of the amplifier.

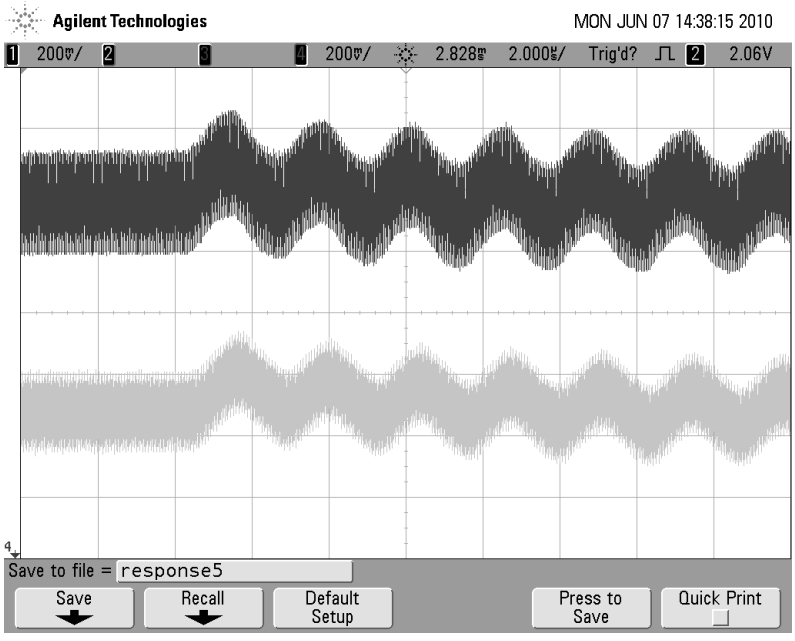


Figure 7.30.: Input signal of the amplifier

7.2.4. Pulse shaper

Figure 7.31 shows the output of the pulse shaping unit. The upper signal represents the output of the I channel, whilst the lower signal represents the output of the Q channel.

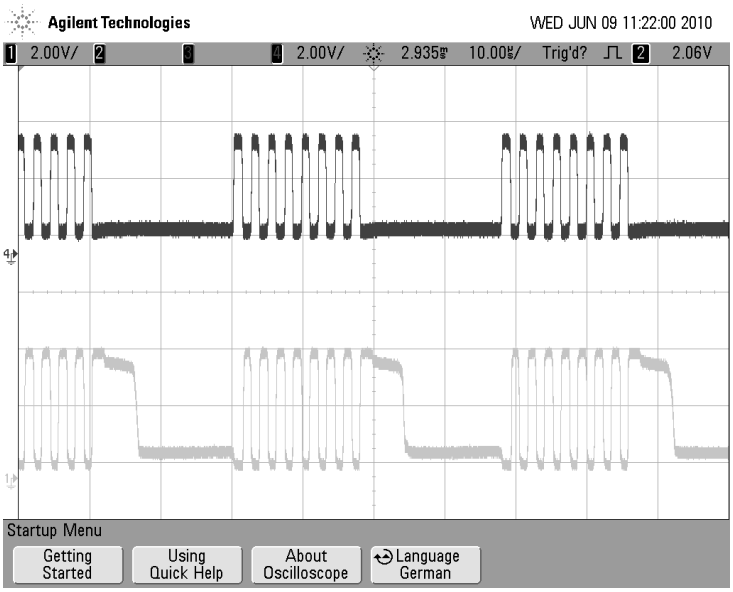


Figure 7.31.: Output signal of the pulse shaper

7.2.5. Channel Selector

In figure 7.32, the output of the multiplexer for selecting the correct channel is shown. In this case, the edges are steeper with a remarkable overshoot of about 1 V. These high-frequency overshoots would cause ESD problems in the whole circuitry, the remedy for that was the insertion of capacitances on the supply lines close to the multiplexer and the inserted ground plane (impedes electromagnetic radiation).

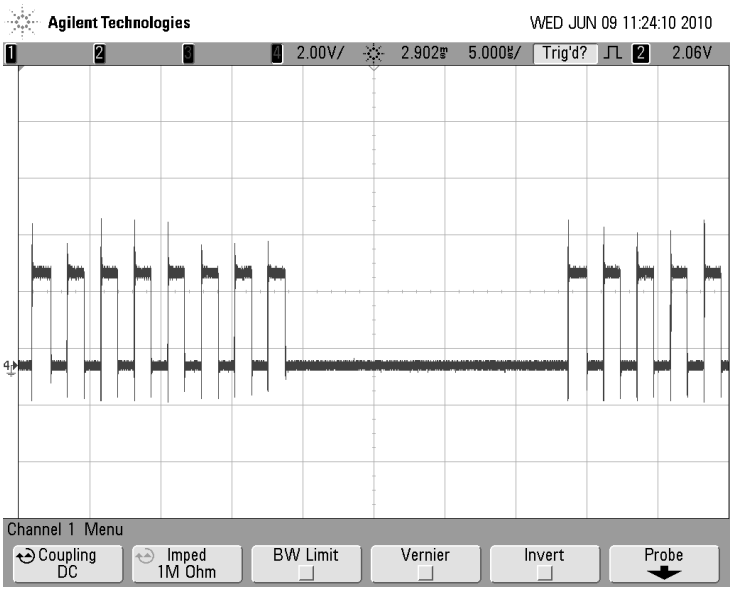


Figure 7.32.: Output signal of the multiplexer

Chapter 8

Conclusion

The aim of this thesis was to develop the analog frontend of an RFID reading device merging mode 1 and mode 2 of the ISO/IEC 18000-3 standard. In combination with the digital part of the reading device, specified in [13], it shall allow the communication between a PC and one or more VICCs.

In a first step, theoretical research was done. At the beginning, the fundamentals of RFID systems, especially of vicinity coupled cards, were explored. Then, the basics of communication engineering, such as modulation/demodulation and coding techniques, were aquired. In addition, the definitions and system informations given in the ISO/IEC 18000-3 standard were impropriated.

With this knowledge, sundry approaches for the overall system structuring were found, whereas the system introduced in this thesis caught on.

Generally, the system was divided in three main parts: A modulator, a demodulator for mode 1 and a demodulator for mode 2. For each elementary circuit block of the main parts a simulation was done using the program QUCS (Quite Universal Circuit Simulator). The first prototype of the modulator circuit was already a printed circuit board and worked as specified. For the demodulation path all the introduced functional basic concepts were prototyped and examined concerning their particular characteristics. After choosing the I/Q demodulation solution realised by the use of an integrated circuit a prototyping of all the elementary circuit blocks using the block concept introduced in chapter 6.1 started. This prototyping also included a checking of the interface between the elementary circuit blocks by connecting them through the above specified frame connector (figure 6.1). In the end, this system was functionally alright, some problems were caused by the long dimensions resulting from the block concept realisation which brought along some EMC problems.

The next step was to integrate the modulator and the demodulation path for mode 1 to one printed circuit board. The shorter distances and the achieved ground plain attenuated the EMC problems which occured with the test construction mentioned above. In the next stage, the analog circuit board and the digital Cortex-M3 board were tied together. After some integration work transponders could be read up to a distance of 2 cm.

Room for improvement still exists for the channel decision unit. In practice, it was shown that the I- and the Q-channel output of the I/Q-demodulator are not built symmetrically. Therefore, it is possible that the signal with the higher signal amplitude is coincidentally the signal with the lower signal-to-noise ratio (SNR). Because of this reason, it may not be reasonable to configure the I- and Q-paths, especially for the I/Q-decision unit, symmetrically.

Altogether, the transmit path worked satisfying for both, mode 1 and mode 2, as well as the receive path for mode 1 delivered a plain signal to the Cortex-M3 board. A further step was now

to implement also the receive path for mode 2, for which the preliminary work has already been done in the course of this thesis.

Appendix A

EAGLE Data

A.1. Trasmit-Path

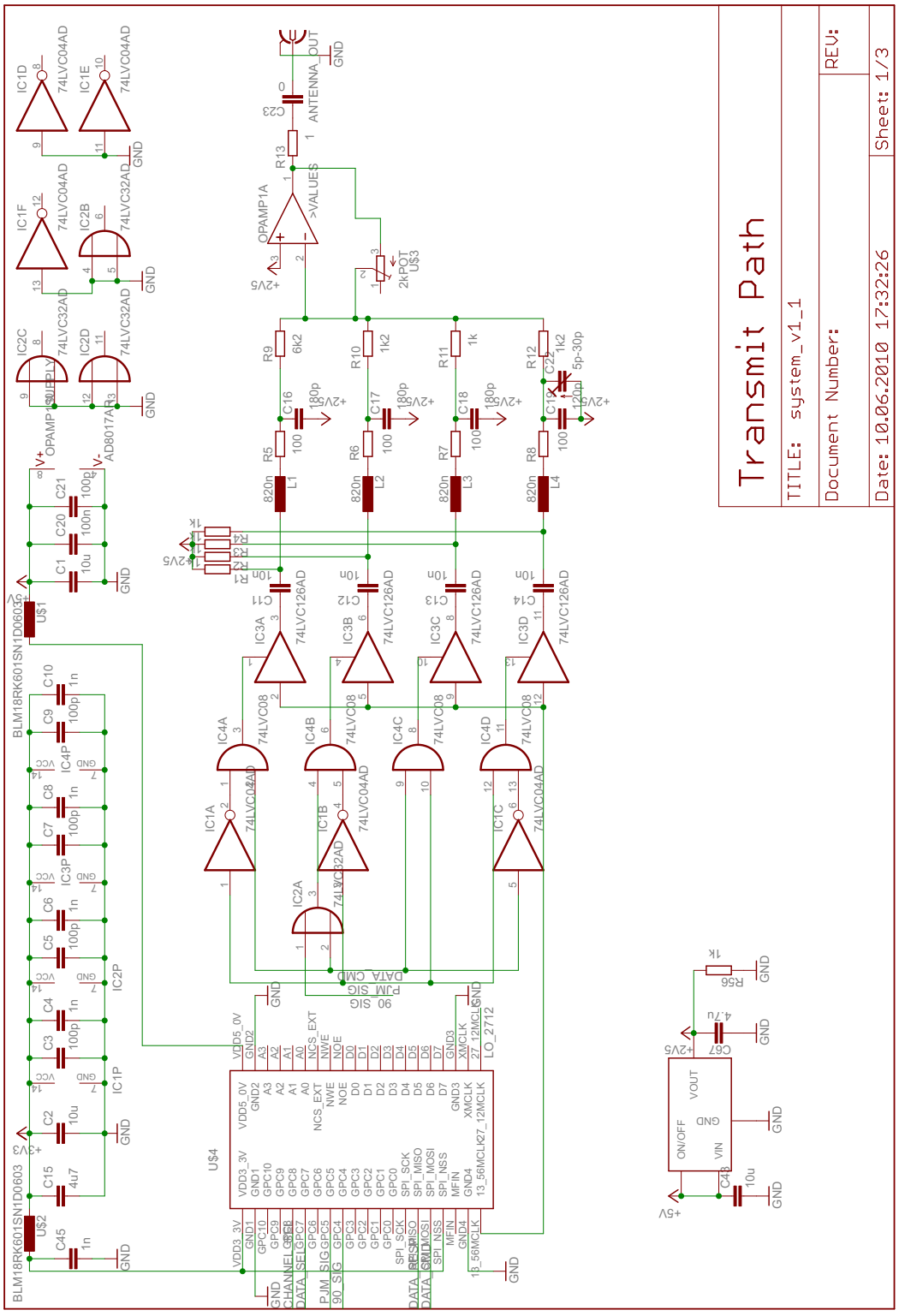


Figure A.1.: EAGLE schematics of the modulator

A.2. Receive-Path Mode 1

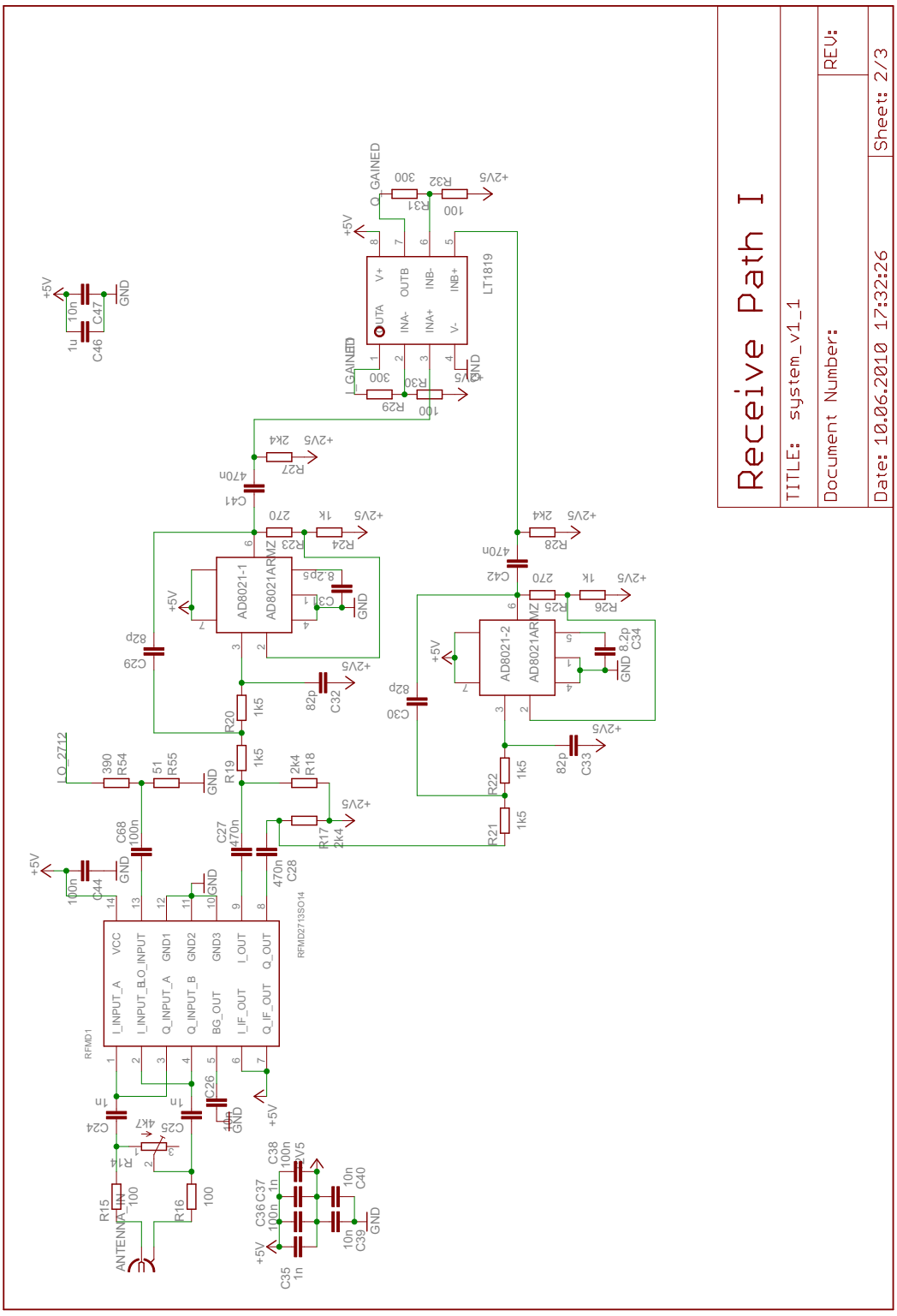


Figure A.2.: EAGLE schematics of the demodulator (1/2)

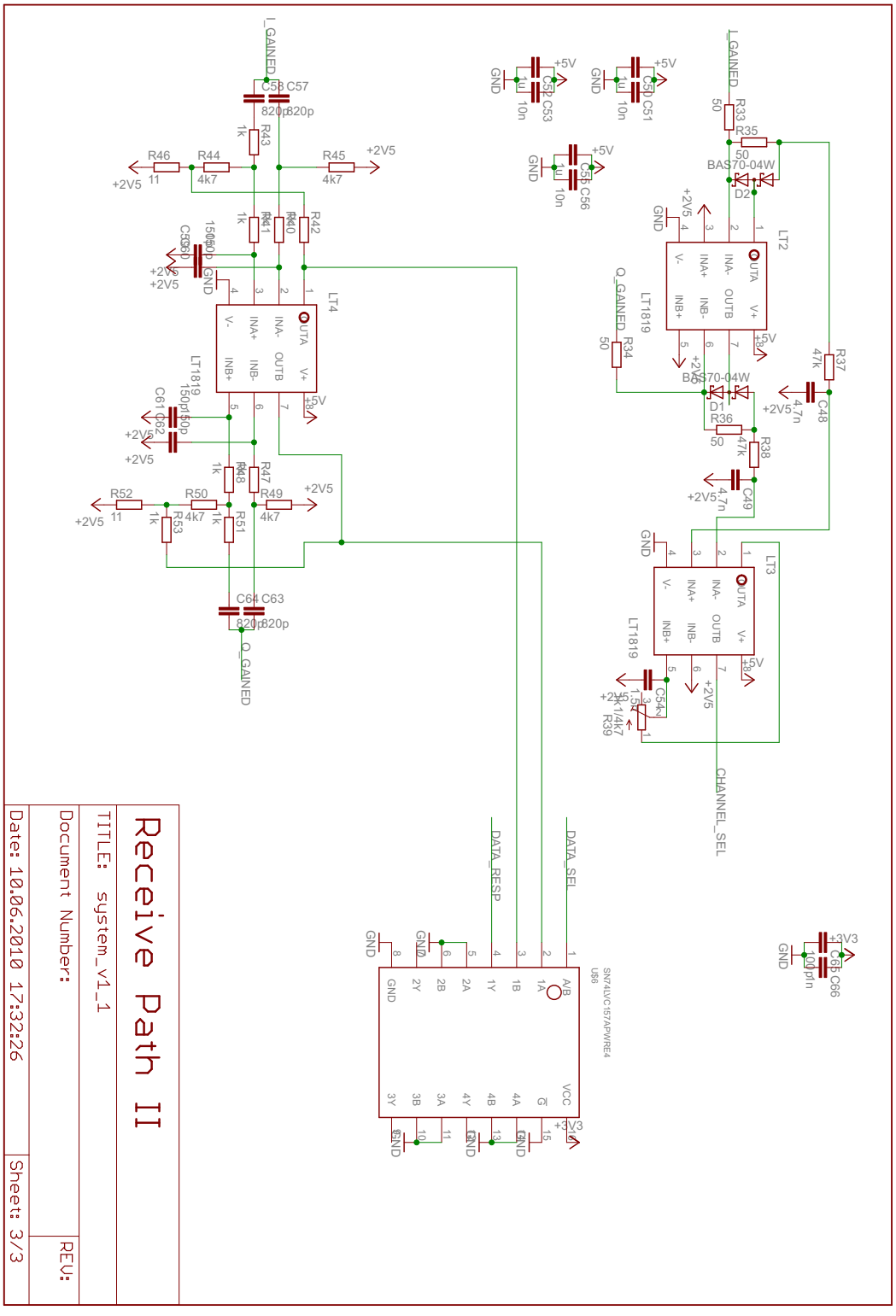


Figure A.3.: EAGLE schematics of the demodulator (2/2)

Bibliography

[1] Rfid news roundup. RFID Journal, November 2008.

[2] Analog Devices. *AD8017 Datasheet*. Analog Devices, 2000.

[3] Arnold Harnau. Schwingquarz oder Quarzoszillator - wie einsetzen? *elektronik industrie*, 3:64–65, 2006.

[4] Bernd Neubig and Wolfgang Briese. *Das große Quarzkochbuch*. Franzis Verlag GmbH, 2002.

[5] Daniel Kusternigg. Contactless Demonstration Reader Decoder Optimization for Receiving Very High Bit Rates. Master's thesis, TU Graz, May 2009.

[6] ISO/IEC. ISO/IEC FDIS 15693-2: Identification cards - Contactless integrated circuit(s) cards - Vicinity cards - Air interface and initialization, 05 2000.

[7] ISO/IEC. ISO/IEC FDIS 18000-3: Information technology - Radiofrequency identification for item management - Parameters for air interface communications at 13,56MHz, 2004.

[8] Klaus Finkenzeller. *RFID Handbuch*. Carl Hanser Verlag München, fifth edition, 2008.

[9] G. Krucker. Operationsverstärker Begriffe, Grundschaltungen, nichtlineare Schaltungen, Funktionsnetzwerke. Script for Analog Systems 2, Bern University of Applied Sciences, http://www.krucker.ch/Skripten-Uebungen/AnSys/ELA5-OpAmp.pdf, August 2004.

[10] Ludger Overmeyer. RFID: Grundlagen und Potenziale. *Logistics Journal*, 1(1860-5923):12, March 2005.

[11] RFMD, editor. *RF2713 Quadrature Modulator/Demodulator*. RF Micro Devices, 2006.

[12] Rudolf Mäusl and Jürgen Göbel. *Analoge und digitale Modulationsverfahren*. Number ISBN 3-7795-2886-6. Hüthing GmbH & Co. KG, 2002.

[13] Selma Skoljic. Transceiver design for contactless desktop reader supporting MODE1 and MODE2 of ISO/IEC 18000-3. Master's thesis, TU Graz, June 2010.

[14] Stephan Rampetzreiter. Very High Bit Rate Communication Channel Modeling on Inductive Coupled Systems. Master's thesis, TU Graz, September 2009.

[15] Thomas Leutgeb. Magnetische Antennen - Theoretische Untersuchung. Technical report, Infineon Technologies Austria AG, 08 2007.

[16] Ulrich Tietze and Christoph Schenk. *Halbleiter-Schaltungstechnik*. Springer Verlag, 2002.