# A highly linear amplifier chain for a delta-sigma analogue-to-digital converter

**Diploma thesis**

by

**Gerhard Martin Landauer**

Submitted to the Faculty of Electrical and Information Engineering in partial fulfilment of the requirements for the degree

Diplom-Ingenieur

of the Electrical Engineering diploma programme

at

Graz University of Technology

Supervisors:

Graz University of Technology:
Dr. Mario Auer

Lille University of Science and Technology:
Prof. Nathalie Rolland

Graz, October 2010

**Statutory declaration**

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## Abstract

In this diploma thesis, which has been made during a stay abroad at Lille University of Science and Technology, an amplifier chain is developed. This chain is operated differentially and has a voltage gain of 40 dB, high linearity and low group delay. It serves as a building block of a high-performance delta-sigma analogue-to-digital converter, which will be used in a radar application.
The main focus of this work is the high requirements of the amplifiers concerning the low limit for signal degradations due to nonlinear distortion. Based on a survey of existing literature, possible bipolar differential amplifier topologies are described. Notably, their linearity properties and eventual distortion compensation mechanisms are analysed. The topologies, which are most adapted to the given problem, are designed with the Cadence's Virtuoso Platform software package in combination with Agilent's GoldenGate simulator. A SiGe topology of Infineon is used for this schematic design process.
Afterwards, the performance of the designed circuits is analysed. The single amplifier stages, as well as the overall amplifier chain, are regarded with the help of nominal and statistical simulations to finally determine their conformance to the desired specifications.



## Kurzfassung

Im Rahmen dieser Diplomarbeit, die während eines Auslandsaufenthaltes an der Université des Sciences et Technologies de Lille durchgeführt wurde, wird eine Verstärkerkette entwickelt. Diese Kette wird differenziell betrieben und weist eine Spannungsverstärkung von 40 dB, hohe Linearität sowie eine niedrige Gruppenlaufzeit auf. Sie dient als einer der Grundblöcke eines hochperformanten Delta-Sigma Analog-Digital-Umsetzers, der wiederum in einem Radargerät zur Anwendung kommen wird.
Ein Hauptaugenmerk dieser Arbeit liegt auf den hohen Anforderungen an die einzelnen Verstärkerstufen sowie die gesamte Verstärkerkette hinsichtlich des niedrigen Limits für Signalverzerrungen durch nichtlineare Effekte. Basierend auf einer intensiven Literaturrecherche werden mögliche bipolare differentielle Verstärkertopologien beschrieben und insbesondere ihre Linearitätseigenschaften und eventuellen Mechanismen zur Störungskompensation beleuchtet. Die Topologien, die die gegebene Problemstellung am besten zu erfüllen geeignet sind, werden anschließend mit Cadence' Softwarepaket Virtuoso Platform in Kombination mit Aglient's GoldenGate-Simulator entworfen. Hierzu steht eine SiGe-Technologie von Infineon zur Verfügung.
Die Leistungsfähigkeit der entwickelten Schaltungen wird anschließend analysiert. Hierzu werden sowohl die einzelnen Verstärkerstufen, als auch die gesamte Verstärkerkette, nominellen und statistischen Analysen unterzogen, um letztendlich ihre Konformität zu den gegebenen Spezifikationen feststellen zu können.



## Résumé

Ce mémoire de maîtrise était effectuée pendant un stage à l'étranger, à l'Université des Sciences et Technologies de Lille. Le sujet de ce stage était le développement d'une chaîne d'amplificateurs. Cette chaîne est opérée de manière différentielle. Elle a un gain en tension de 40 dB, une linéarité élevée et un petit temps de groupe. Elle fait partie d'un convertisseur delta-sigma, qui lui-même sera utilisé dans une application radar.
Une attention particulière de ce travail a été portée aux différents étages ainsi qu'à la chaîne complète afin d'ètudier des limites de distorsion non-linéaire. Basées sur une recherche bibliographique, différentes topologies d'amplificateurs sont analysées. Les schémas des topologies les plus adaptées au problème sont ensuite développés en utilisant le logiciel Virtuoso Platform de Cadence en combinaison avec le moteur de simulation GoldenGate de Agilent. Une technologie SiGe de Infineon est à disposition pour le design.
La performance des circuits est analysée. Les étages et toute la chaîne sont regardés avec l'aide d'une étude nominale et une étude statistique, pour finalement pouvoir constater leur conformité aux spécifications.

To my parents, for their moral and financial support throughout my studies.

# Contents

# Chapter 1

# Introduction

## 1.1 Motivation and objectives of this work

This thesis describes the design and simulation of a highly linear fully-differential broadband amplifier chain, which forms part of a bandpass delta-sigma analogue-to-digital converter. The work of this thesis was performed during a stay abroad at Lille University of Science and Technology, France.

The foundation for this work was laid by an internationally active semiconductor company, which develops a high-end analogue-to-digital converter based on the delta-sigma concept. The main operating figures of this data converter are an effective number of bits (ENOB) equal to 9 bit and a conversion rate of 500 MSa/s. Its conversion speed and accuracy allow the converter to be used in a next-generation radar application.
The semiconductor company contracted the IRCICA research institute of the University of Lille, to develop one part of the converter, an amplifier chain. This choice was motivated by the expertise, which IRCICA already holds in the field of high-speed data converters. An example of former research activities at the institute is a 7 bit 40 GSa/s analogue-to-digital converter, which records transient events with a length of 5 ns [1, 2]. This project gave basic ideas of how to conceive the amplifiers of this work.

The amplifier chain to be designed for the converter is operated differentially. It consists of several individual differential amplifier stages, with one stage having variable gain. The chain needs to have high gain, very low non-linear distortion and a low noise figure. Low group delay is another crucial requirement and implies high bandwidth. Not many differential amplifier topologies are capable of fulfilling all these requirements at the same time, in particular high linearity is difficult to achieve. Therefore, an analysis of topologies with low signal distortion in addition to an analysis of standard amplifier topologies is one major part of this thesis and performed in Chapter 2, whereby an emphasis is put on the circuit functionalities concerning linearity. Appropriate fixed-gain and variable-gain amplifier types, which fit most accurately to the given problem, are identified.

The second major part of this thesis is the schematic design and simulation of the amplifiers and the overall amplifier chain. In Chapter 3, the schematics for the amplifiers chosen in the preceding chapter are designed. The used software package is Cadence's Virtuoso Platform in combination with Agilent's GoldenGate RFIC simulation engine. The circuits are implemented using Infineon's fast B7HF200 200 GHz SiGe technology. Afterwards, the single amplifier stages and the overall amplifier chain are simulated in detail in Chapters 4 and 5. With the help of these simulations their compliance to the given specifications is finally verified.

Having designed and simulated the amplifier chain within the framework of this thesis, the proposed circuits will undergo an extensive stability analysis and will be laid out in future design steps. Then they will be integrated into the overall delta-sigma converter system and implemented as a monolithic microwave integrated circuit (MMIC).

## 1.2 System overview

Before the requirements of the amplifier chain are described in more detail, the principle of the bandpass delta-sigma analogue-to-digital converter [3] is regarded to have an overview of the system, into which the amplifier chain of this work is included.

The converter contains an analogue-to-digital converter (ADC) and a digital-to-analogue converter (DAC) as subsystems, both with 7 bit resolution. However, the overall delta-sigma ADC has an ENOB of 9 bit and not 7 bit. This resolution enhancement of 2 bit is due to the delta-sigma principle, realised by high oversampling of the signal of interest by the internal ADC and a loop structure with noise-shaping properties.

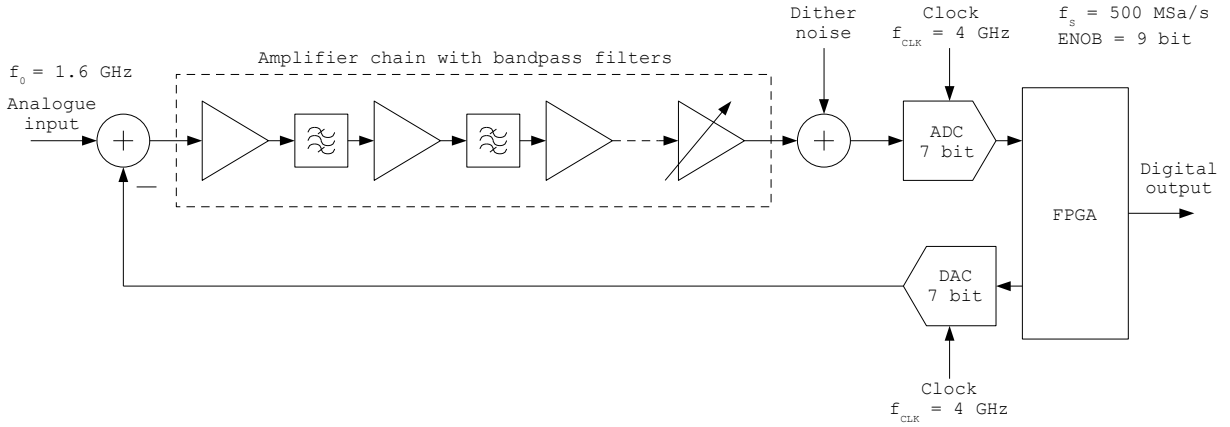


**Figure 1.1:** Block diagram of the delta-sigma analogue-to-digital converter. The amplifier chain is in the forward path of the converter's control loop. It consists of several fixed-gain amplifiers, a variable-gain amplifier and bandpass filters.

### Functional principle of the overall converter system

The name bandpass sigma-delta-converter reveals that the input signal is not provided in the baseband. Its spectrum is concentrated around an intermediate frequency $f_0$ of 1.6 GHz. This signal constellation is the result of a preceding receiver structure with downconversion of the received HF radar signal to this intermediate frequency. At the input of the converter, an error signal is built by subtracting the last conversion result from the input signal. This error signal is amplified by the highly linear chain and modified by its bandpass filters. Dither noise is added to prevent the circuit from generating idle tones, i.e. output oscillations occurring at low input signal levels. Next, the signal with 200 MHz bandwidth is sampled with a rate of 4 GSa/s by the 7 bit-ADC. Thus, the sampling rate is much higher than the signal bandwidth. Shannon's sampling theorem of the necessity of sampling the signal with a frequency of at least twice its bandwidth to avoid information loss is more than fulfilled due to this oversampling. The sampled data is reconverted to an analog signal and fed back to the subtractor circuit to build a new error signal, but is also fed to a decimation filter and a downconversion mixer, implemented on a field-programmable gate array (FPGA), and provided as a digital baseband signal at the output of the overall converter.

Normally the quantisation noise resulting from a conversion from the analogue to the digital domain has a white spectrum. The feedback loop of a delta-sigma converter with a bandpass loop filter, combined with oversampling, yields a noise power spectral density with the noise power concentrated at frequencies far away from $f_0$. This procedure is called noise-shaping. The signal band sustains less degradation due to noise and the signal-to-noise ratio (SNR) is increased compared to classical converters. This lower quantisation noise is reflected in a higher ENOB of the overall delta-sigma converter, gaining 2 bit of resolution in the case of the converter of this work.

### Amplifier chain requirements

In order to be able to ideally operate the delta-sigma converter, several demands are made on the amplifier chain:

- Linearity:

  The resolution enhancement of the converter is based on the high spurious-free dynamic range [1] (SFDR) after the nose-shaping process of the converter loop. Performance degradation due to non-linearities of the amplifier chain has to be avoided, as additional spectral components due to these non-linearities decrease the SFDR and consequently also the converter's resolution. To avoid this problem, the linearity requirements on the amplifier chain are stringent and the most challenging problem to be solved by this thesis.

- Gain:

  An optimal use of the input range of the internal 7 bit-ADC requires a certain amplifier chain gain.

- Speed:

  The 250 ns sampling time of the 7 bit-ADC requires a delta-sigma converter's control loop, which only introduces a short delay. Hence, the group delay of the amplifier chain, which forms part of the loop, must stay below certain limits. Thus, the group delay at the operating frequency 1.6 GHz is another major amplifier chain constraint apart from linearity and noise requirements.
  Group delay is inherently linked to bandwidth. The required low group delay implies high bandwidth of the amplifiers.

- Noise:

  The need for low noise is given due to the need for a low SFDR of the converter. Degrading the SFDR because of high noise levels would lead to a decrease in resolution.

- Output impedance magnitude:

  The amplifiers' output impedances must have certain values to guarantee correct adaptation and operation of the bandpass filters.

[1] The spurious-free dynamic range is defined as the ratio between the ADC's input signal and the strongest signal distortion at its output, be it the noise floor or additional spectral components due to non-linear effects.

## 1.3 Desired specifications

In this section the requirements on the amplifiers and the overall amplifier chain are described according to the specification sheets obtained by the contracting semiconductor company.

### 1.3.1 Variables used to describe the specifications

- Third-order harmonic distortion $HD_3$

  The linearity of the circuits is characterised by the third-order harmonic distortion, i.e. the ratio between the voltage magnitude $|V_{out_3}|$ of the third harmonic at 4.8 GHz and the voltage magnitude $|V_{out_1}|$ of the 1.6 GHz fundamental wave of the output signal.

$$HD_3 = \left| \frac{V_{out_3}}{V_{out_1}} \right| \tag{1.1}$$

- Voltage gain $A_d$

  Throughout this work the gain is defined as the ratio between the signals' voltage magnitudes at the output and input of an amplifier or the amplifier chain, whereby only their fundamental frequency of 1.6 GHz is considered. Due to the differential principle of operation of the amplifiers and the amplifier chain, the gain of primary interest is the differential voltage gain $A_d$.

$$A_d = \left| \frac{V_{out_1}}{V_{in_1}} \right| \tag{1.2}$$

- Group delay $\tau_g$

  The group delay of a network is obtained by differentiating the angular frequency $\omega$ by the phase shift $\phi$ between the input and output of the network.

$$\tau_g = -\frac{\partial \phi}{\partial \omega} \tag{1.3}$$

- Bandwidth B

  The standard 3 dB-bandwidth is used as the bandwidth measure.

- Output impedance magnitude $|Z_{out}|$

  As the imaginary part of the output impedance is virtually non existent, the output impedance is regarded by taking its magnitude value.

### 1.3.2 Exact definition of the specifications

The desired specifications are classified in two groups according to their priority. The first group is formed by necessary requirements, which must be complied with. Desirable requirements build the second group. It is aimed for their exact fulfilment, but small deviations from the given limits are acceptable. This prioritisation gives enough flexibility for a research project's design process, for which the linearity and speed requirements are high.

| Amplifier stage specification | | |
|---|---|---|
| Necessary requirements | | |
| $HD_3$ | $< -80\,\mathrm{dBc}$ | |
| Desirable requirements | | |
| | fixed gain | variable gain |
| $A_d$ | 6 or 9 dB | $3 \ldots 6\,\mathrm{dB}$ |
| $B$ | $\geq 10\,\mathrm{GHz}$ | |
| $\tau_g$ | $\leq 20\,\mathrm{ps}$ | |
| $\lvert Z_{out} \rvert$ | $200\,\Omega$ | |

**Table 1.1:** Desired specification for the amplifier stages

| Amplifier chain specification | |
|---|---|
| Necessary requirements | |
| $HD_3$ | $< -80\,\mathrm{dBc}$ |
| $A_d$ | 40 dB |
| $\tau_g$ | $< 180\,\mathrm{ps}$ |
| $F$ | $< 10\,\mathrm{dB}$ |

**Table 1.2:** Desired specification for the overall amplifier chain

All specification values are defined for 27 °C room temperature conditions. However, values at low and high temperatures should not differ strongly from the given specification, and are also regarded in the analyses of Chapters 4 and 5 to study temperature influence on the circuit behaviour.

The amplifier chain specification is defined for a chain without added bandpass filters.

The third-order harmonic distortion values of the amplifier stages and the overall amplifier chain have to be smaller than $-80\,\mathrm{dBc}$ for the whole output voltage range, especially for the maximum output voltage of $500\,\mathrm{mV_{pp}}$. To have some linearity margin, the maximum output voltage is chosen as $600\,\mathrm{mV_{pp}}$ throughout this thesis. In the case of variable gain, the $\mathrm{HD_3}$ criterion must be met for all possible gain values. If performance degradations due to statistical variations of the circuit components are considered, the number of complying circuits has to be at least 99%.

The voltage gain of the fixed-gain amplifier stages must be equal to 6 or 9 dB, so that eventually two 9 dB-stages could be used instead of three 6 dB-stages. Small gain deviations are tolerated, since the variable gain amplifier with its gain from 3 to 6 dB can compensate for these variations to a certain extent. However, the voltage gain of the overall amplifier chain has to be exactly 40 dB, also under consideration of statistical circuit variations.

Single amplifier stages should have a group delay in the order of 20 ps and a bandwidth of at least 10 GHz in order to easily obtain a group delay smaller than 180 ps for the overall filter-less amplifier chain.

The amplifier chain's noise figure must be less than 10 dB. At least the first stages of the chain need to have a noise figure considerably lower than 10 dB, to be able to fulfil this 10 dB-condition for the overall amplifier chain. As the noise figure of an amplifier is dependent on the signal source's output impedance, the source impedances also have to be defined along with the noise figures. The subtractor circuit of the delta-sigma converter has an output impedance of $100\,\Omega$, so the noise figure of the overall amplifier chain has to be considered for this source impedance. The source impedances for the single amplifier stages are $100\,\Omega$ for the first stage, and $200\,\Omega$ for all following stages.

The differential output impedances of all amplifiers of the chain should be equal to $200\,\Omega$. Due to resistor tolerances, this is only possible within the limits given by the component tolerances of the used technology.

Power consumption is only of secondary importance. Experience shows that the amplifier chain should not consume more than about 1 W of power.

# Chapter 2

# Differential amplifier topologies

One of the main tasks of this work was to find amplifiers, which are capable of fulfilling all the needed specifications, most notably the linearity limit of a third-order harmonic distortion of $HD_3 < -80\,dBc$. Before looking at the different topologies, the main advantages of differential amplifiers, common-mode rejection and suppression of even-order harmonics, are described. Then the basic emitter-coupled differential pair is analysed. The emitter-coupled pair is the basis for all the more sophisticated differential amplifiers, so importance is attached to its analysis, even if it is not usable for this work. All fixed gain topologies are regarded concerning their mechanisms of distortion correction, if existent, and the resulting linearity properties. Possible major drawbacks, which contradict their use in the amplifier chain, are indicated. The linearity analysis in analytical form is only done for the basic emitter-coupled pair, for all other topologies one relies on numerical simulations, because either closed form solutions for $HD_3$ do not exist, or their derivation would be too elaborate. To the authors best knowledge, there exist only two possible solutions for the variable gain amplifiers, so the choice of the best variable-gain solution is more easily made than for the fixed gain amplifiers. Finally, the properties of all amplifiers are summarised and the most appropriate topologies are chosen.

## 2.1 Advantages of differential structures

The main property of differential amplifiers is that a differential input signal is amplified and accessible at the output, whereas common-mode input signals are completely suppressed in the case of an ideal circuit and have no influence on the output. Many advantages result from the capability of rejecting common-mode input signals. Reduction of common-mode input distortion, reduction of noise, the suppression of even-order harmonics and insensitivity to temperature changes make the differential topology the first choice in the case of low-distortion design. Furthermore the possibility of directly connecting the output of a stage to the input of the next stage requires no additional coupling elements between the stages of amplifier cascades. Because of all these advantages the differential amplifier is an omnipresent element in analogue circuit design. For the amplifier chain of this work only differential topologies are chosen.

### 2.1.1 Gain and common-mode rejection ratio

The input signals, the gain and the measure common-mode rejection ratio (CMRR) are mathematically defined [4]. The CMRR is an important classification figure of the rejection of common-mode input signals of differential amplifiers and should ideally be infinitely high to strongly reduce distortions.

The differential-mode and common-mode input voltages of an amplifier are equal to

$$V_{id} = V_{in}^{+} - V_{in}^{-} \tag{2.1}$$

$$V_{ic} = \frac{V_{in}^{+} + V_{in}^{-}}{2} \tag{2.2}$$

$$\tag{2.3}$$

The differential gain is defined as the amplification factor of a differential input voltage, if the DC input level is kept constant.

$$A_d = \left.\frac{\partial V_{od}}{\partial V_{id}}\right|_{V_{ic}=0} \tag{2.4}$$

Its counterpart is the undesired but due to non-ideal components not completely avoidable common-mode gain. It can be obtained by exciting both inputs equally. The resulting change of the output voltage gives

$$A_c = \left.\frac{\partial V_{od}}{\partial V_{ic}}\right|_{V_{id}=0} \tag{2.5}$$

Now the ratio between common- and differential-mode gain is taken to calculate the CMRR as

$$CMRR = \frac{A_d}{A_c} \tag{2.6}$$

As already mentioned, a high CMRR means low-distortion behaviour of the circuit. Firstly, long leads feeding the input of the amplifier can sustain distortion. If the distortion affects both leads the same way, it can be seen as a change of the DC input level and is thus rejected. Because of the small distances between successive amplifier stages on the MMIC a strong diminution of influences of common-mode distortion can be expected. Secondly, temperature changes, acting on the transistor properties of the symmetrical structure of a differential amplifier in the same way, can be considered as a common-mode excitation of the input of the next stage. Therefore, differential structures are more robust against temperature variations. Thirdly, presumed that a single current source biases the amplifier's differential pair, the noise caused by this current source is also rejected for the same reason, notably the common-mode rejection of the next amplifier stage. Finally, one other important consequence of high CMRR is that successive stages can be connected directly without interstage coupling components. If the DC output level of one stage lies within the region of operation of the following input stage, no decoupling capacitances and no additional biasing circuits have to be used.

### 2.1.2 Suppression of even-order harmonics

Balanced circuits like differential amplifiers suppress even-order harmonics of a sinusoidal input signal. The spectral components at even-order frequency multiples, generated by non-linearities, do therefore not exist at the output of an ideal amplifier, excited by a single-tone signal at its input. This behaviour can be explained by looking at the power series of the output signals of the two branches of a differential pair [5]. Assuming a completely symmetrical topology, the coefficients of the power series, which describe the non-linear behaviour, are identical for both branches. Only the sign of the input voltage differs, as the inputs are excited differentially.

$$V_o^+ = \frac{k_0}{2} + \frac{k_1}{2} \cdot V_{id} + \frac{k_2}{2} \cdot V_{id}^2 + \frac{k_3}{2} \cdot V_{id}^3 + \frac{k_4}{2} \cdot V_{id}^4 + \ldots \tag{2.7}$$

$$V_o^- = \frac{k_0}{2} + \frac{k_1}{2} \cdot (-V_{id}) + \frac{k_2}{2} \cdot (-V_{id})^2 + \frac{k_3}{2} \cdot (-V_{id})^3 + \frac{k_4}{2} \cdot (-V_{id})^4 + \ldots \tag{2.8}$$

Raising the input voltages to their respective powers and building the difference of the output voltages of the two amplifier branches leads to the following expression for the differential output voltage.

$$V_{od} = V_o^+ - V_o^- = k_1 \cdot V_{id} + k_3 \cdot V_{id}^3 + k_5 \cdot V_{id}^5 + \ldots \tag{2.9}$$

The input voltage is assumed sinusoidal.

$$V_{id} = a \cdot \sin(\omega \cdot t) \tag{2.10}$$

If a sine function is exponentiated by an odd integer, the new function consists of a sum of sine functions with odd-order multiples of the fundamental frequency, as can be proven by calculating the Fourier series of the exponentiation result. Therefore the output contains the following frequency components.

$$V_{od} = a_1 \cdot \sin(\omega \cdot t) + a_3 \cdot \sin(3\omega \cdot t) + a_5 \cdot \sin(5\omega \cdot t) + \ldots \tag{2.11}$$

In the ideal case the ratio between the even harmonics and the fundamental frequency is equal to zero, they do not exist. Due to mismatches of the amplifier components and resulting asymmetry of the two branches, they are not completely suppressed, but normally they are small enough to be expected below the odd-order harmonics. The $HD_2$ value is lower than the $HD_3$ value, and as both even- and odd harmonics strongly decrease with increasing order, all harmonic distortion levels from order four upwards can normally be ignored. So the only prominent single-tone distortion measure in weakly nonlinear circuits is the $HD_3$ measure.

## 2.2 Fixed-gain topologies

All the differential amplifier topologies with constant gain, which have been found during the bibliographical research and which show promise to be used for this work, are mentioned in this section. The basic emitter-coupled pair is analysed as a theoretical example. The same pair with additional emitter-degeneration resistors is still a simple, but much more linear topology. If diodes are added to the emitter-degenerated differential pair, the distortion gets even lower. Another promising architecture is the compensated cascode amplifier, which has included a correction amplifier to lower distortion. The same is the case for an amplifier topology reported by Miki. To complete the list of candidates for the amplifier chain, the fast Cherry-Hooper circuit, the cross-coupled differential pair and the multi-tanh principle are analysed.

### 2.2.1 Basic emitter-coupled pair

The emitter-coupled pair in its most simple configuration [6, 4] consists of two identical transistors $Q_1$ and $Q_2$ with their emitters connected together (Figure 2.1). The shared emitter node is biased by a current source with ideally infinitely high output impedance. The input voltages at the bases of the transistors are converted to output collector currents, which cause a voltage drop-off at the collector load resistances, and the difference between these voltages represents the output voltage of the amplifier.

#### DC transfer characteristics and gain

The collector current of a bipolar transistor, using the standard large signal relations for the forward-active region and neglecting the Early-effect, can be expressed by the diode-law equation.

$$I_c = I_S \cdot \exp\left(\frac{V_{be}}{V_T}\right) \tag{2.12}$$

Building the ratio between the two collector currents of the pair under assumption of identical transistors and therefore identical saturation currents $I_S$ results in

$$\frac{I_{c1}}{I_{c2}} = \exp\left(\frac{V_{id}}{V_T}\right) \tag{2.13}$$

With application of Kirchhoff's current law at the emitter node we find that

$$I_{Tail} = \frac{I_{c1} + I_{c2}}{\alpha_F} \tag{2.14}$$

The combination of equations 2.13 and 2.14 leads to expressions for both collector currents.

$$I_{c1} = \frac{\alpha_F \cdot I_{Tail}}{1 + \exp\left(\frac{-V_{id}}{V_T}\right)} \tag{2.15}$$

$$I_{c2} = \frac{\alpha_F \cdot I_{Tail}}{1 + \exp\left(\frac{V_{id}}{V_T}\right)} \tag{2.16}$$

The differential output voltage is calculated by

$$V_{od} = (V_{CC} - I_{c1} \cdot R_C) - (V_{CC} - I_{c2} \cdot R_C) \tag{2.17}$$

By using the mathematical relation between the hyperbolic tangent and the exponential function we can finally express the DC characteristics of the emitter-coupled pair as

$$V_{od} = I_{Tail}\alpha_F R_C \tanh\left(-\frac{V_{id}}{2V_T}\right) \tag{2.18}$$

Thus the combination of the exponential transconductance characteristics of the two transistors leads to a hyperbolic tangent relation between the input and the output of the classical emitter-coupled pair. This is only valid for low-frequency signals, without consideration of parasitic capacitances, and under negligence of other second order effects.

The differential gain of the pair is only dependent on the biasing current, the common-base current gain and the collector resistance. At low input signals it is equal to

$$A_d = \left.\frac{\partial V_{od}}{\partial V_{id}}\right|_{V_{id}\ll} = -\frac{I_{Tail}\alpha_F R_C}{2V_T} \tag{2.19}$$

With the simple differential pair high gain is achievable at low signal levels. For instance, $\mathrm{I_{Tail}} = 20\,\mathrm{mA}$, $\alpha_\mathrm{F} = 0.99$ and $\mathrm{R_C} = 100\,\Omega$ give a differential voltage gain of $\mathrm{A_d} = 31.6\,\mathrm{dB}$.

**Harmonic distortion**

The analytic description of the DC characteristics can be used to calculate the second- and third-order harmonic distortions $\mathrm{HD_2}$ and $\mathrm{HD_3}$ by developing it into a power series.

$$V_{od} = k_1 V_{id} + k_2 V_{id}^2 + k_3 V_{id}^3 + k_4 V_{id}^4 + k_5 V_{id}^5 + \ldots = \tag{2.20}$$

$$= I_{Tail}\alpha_F R_C \cdot \left(-\frac{V_{id}}{2V_T} + \frac{V_{id}^3}{24V_T^3} + \frac{V_{id}^5}{240V_t^5} + \ldots\right) \tag{2.21}$$

Knowing the relations between the $\mathrm{n^{th}}$-order nonlinearity coefficients $\mathrm{k_n}$ and the $\mathrm{n^{th}}$-order harmonic distortions $\mathrm{HD_n}$ [7], the harmonic distortions of order two and three are given as

$$HD_2 = \frac{1}{2}\left|\frac{k_2}{k_1}\right| = 0 \tag{2.22}$$

$$HD_3 = \frac{1}{4}\left|\frac{k_3}{k_1}\right| = \frac{1}{48}\frac{\hat{V}^2}{V_T^2} \tag{2.23}$$

There exists no distortion of order two, as can be expected for a perfectly symmetrical differential amplifier, for which only odd-order distortion has to be considered.
The distortion of order three limits the maximum input voltage. The amplifier specifications only allow a $\mathrm{HD_3}$ of less than $-80\,\mathrm{dBc}$. With the help of the relation derived before, the maximum input voltage can be determined as approximately $3.60\,\mathrm{mV}_{pp}$.

In the analysis of weakly nonlinear behaviour of the bipolar emitter-coupled pairs done in [7], the relation between device mismatch and second-order distortion is derived. Assuming device mismatch of the transistors, their transconductances are not equal any more. The mismatch between the load resistors is considered as negligible, so due to simplifications the second-order harmonic is only expressed as a function of the difference $\Delta\mathrm{g_m}$ between the transconductances. Using elaborate calculations with Volterra series, the second-order harmonic distortion becomes approximately

$$HD_2 = \frac{1}{8}\cdot\frac{\Delta g_m}{g_m}\cdot\frac{\hat{V}}{V_T} \tag{2.24}$$

If the transconductance mismatch $\Delta\mathrm{g_m}$ between the two transistors of an emitter-coupled differential pair is known, the $\mathrm{HD_2}$ value can easily be calculated. Normally $\mathrm{HD_3}$ is larger than $\mathrm{HD_2}$.

### Common-mode rejection ratio

The CMRR is only equal to zero, if the tail current source is assumed to be ideal. If the source has a finite output resistance $R_{Tail}$, the emitter-coupled pair can be seen as two common-emitter amplifiers with emitter degeneration resistances of $2R_{Tail}$, as it is done by Gray [6]. For this approach of calculating the differential and common-mode gain of the emitter-coupled pair, the Equations 2.4 and 2.5 give

$$A_d = -g_m R_C \tag{2.25}$$

$$A_c = -\frac{g_m R_C}{1 + 2 g_m R_{Tail}} \tag{2.26}$$

Building the ratio between those two gains as given by equation 2.6, yields

$$CMRR = 1 + 2 g_m R_{Tail} \tag{2.27}$$

The quality of the current source is therefore the determining factor of CMRR. A standard current source should be favoured over a tail resistor, which would be a simpler but worse performing solution. A more complex current source with higher output resistance, like the cascode current source, would increase CMRR at the cost of higher circuit complexity. So a trade-off has to be made between common-mode rejection and complexity of the current source.

### Summary

It can be concluded, that the input voltage limit of 3.6 mV is two decades too low to give the simple emitter-coupled pair a perspective to be practically used for this work. It is impossible to achieve at least moderately linear behaviour with input voltages higher than some millivolts. Under consideration of other non-linearity sources than the low-frequency input-output relation, the voltage limit is expected to be even lower. The simple differential pair shall therefore only be seen as a theoretical basis for more complex topologies. Because of its simple design, it serves only as an example to show the basic properties of differential pairs in an analytical way.

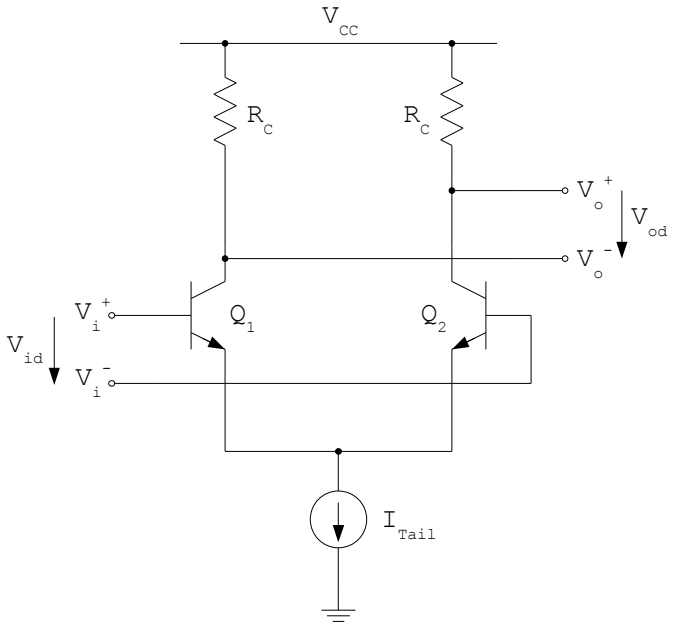


**Figure 2.1:** Scheme of the basic emitter-coupled pair

### 2.2.2 Emitter-coupled pair with emitter degeneration

If emitter degeneration resistors are added to the emitter nodes of the transistors, negative feedback is established. If the base-emitter voltage $V_{be}$ of a transistor is increased, the current through its emitter is also increased according to the transconductance of the transistor. This increase of current, however, leads to a higher voltage drop-off at the emitter degeneration resistor, which counteracts the original $V_{be}$ voltage increase. Due to the feedback, the linearity of the circuit is substantially higher than without emitter degeneration, whereas the voltage gain decreases with rising degeneration.
This amplifier topology is not just a theoretical example like the simple emitter-coupled pair, it is by contrast used in a vast number of electronic circuits. An example for an application using an emitter-coupled pair with emitter degeneration is a 50 GHz wideband amplifier for fibre-optic communications presented by Agarwal et al. [8], who use two of these amplifiers in an amplifier chain. Perndl et al. [9] also work with this topology and presented another broadband amplifier chain based on amplifiers with emitter degeneration.
Even if this topology still does not have a great complexity, there exists no explicit solution for its low frequency input-output relation. Therefore it is impossible to develop a power series out of the DC characteristics, to analytically express the harmonic distortion for instance. Nevertheless, the voltage gain of the circuit can approximately be expressed by accepting simplifications, and the $HD_3$ distortion can be evaluated with numerical methods.

#### DC transfer characteristics and gain

The differential input voltage between the bases of the transistors is equal to

$$V_{id} = V_{be1} + I_{c1}R_E - V_{be2} - I_{c2}R_E \tag{2.28}$$

The equations 2.15 and 2.16, which describe the collector currents of a simple emitter-coupled pair, are modified by adding the influence of the voltage drop-offs described by Equation 2.28. This gives the transcendental equations for the collector currents as

$$I_{c1} = \frac{\alpha_F \cdot I_{Tail}}{1 + \exp\left(\frac{-V_{id} - \left(I_{Tail} - \frac{2I_{c1}}{\alpha_F}\right)R_E}{V_T}\right)} \tag{2.29}$$

$$I_{c2} = \frac{\alpha_F \cdot I_{Tail}}{1 + \exp\left(\frac{V_{id} + \left(I_{Tail} - \frac{2I_{c2}}{\alpha_F}\right)R_E}{V_T}\right)} \tag{2.30}$$

These equations are numerically solved to obtain the DC transfer characteristic of the amplifier. Realistic numerical values are chosen for the tail current source $I_{Tail}$, the collector resistance $R_C$ and the common-base current gain $\alpha_F$. Different values are assigned to the emitter degeneration resistance to demonstrate its impact on gain and linearity range. The relations obtained between input and output are shown in Figure 2.3 for different degrees of degeneration.

The gain of the emitter-coupled pair with emitter degeneration can be estimated by taking Equation 2.28 and assuming that the base-emitter voltages $V_{be1}$ and $V_{be2}$ are equal [4]. With this approach the collector currents are given as

$$I_{c1} \approx \frac{I_{Tail}}{2\alpha_F} + \frac{V_{id}}{2R_E} \tag{2.31}$$

$$I_{c2} \approx \frac{I_{Tail}}{2\alpha_F} - \frac{V_{id}}{2R_E} \tag{2.32}$$

$$\tag{2.33}$$

Using 2.17 gives the differential output voltage

$$V_{od} \approx -\frac{R_C}{R_E} \cdot V_{in} \tag{2.34}$$

The differential voltage gain in the linear region is approximately equal to the ratio between the collector and the emitter degeneration resistance.

$$A_d \approx -\frac{R_C}{R_E} \tag{2.35}$$

### Harmonic distortion

The third-order harmonic distortion is numerically calculated by applying an input sine wave to the DC transfer function of the amplifier. The resulting slightly distorted output signal is transformed into the frequency domain, where the $HD_3$ value can easily be obtained (Figure 2.4). The third-order harmonic distortion for an amplifier with a voltage gain of $A_d = 2$ reaches the $-80\,\mathrm{dBc}$ limit at an input voltage of about $302\,\mathrm{mV}_{pp}$, which is a substantial improvement compared to the simple differential amplifier.

### Summary

It can be concluded, that the emitter-coupled pair with emitter degeneration resistors is able to obtain high linearity without unacceptably decreasing the gain by using too high degeneration resistors. According to the numerical simulation for a voltage gain of about two, the third-order harmonic distortion at $300\,\mathrm{mV}$ is approximately equal to the limit of $HD_3 = -80\,\mathrm{dBc}$. However, the numerical simulation does not consider other non-linearities, which exist without doubt, so the real voltage limit is below the calculated one.

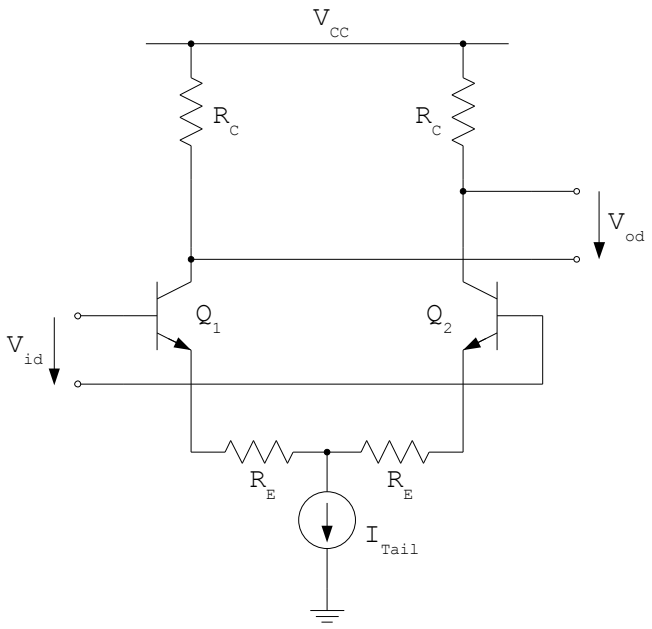


**Figure 2.2:** Scheme of the emitter-coupled pair with emitter degeneration

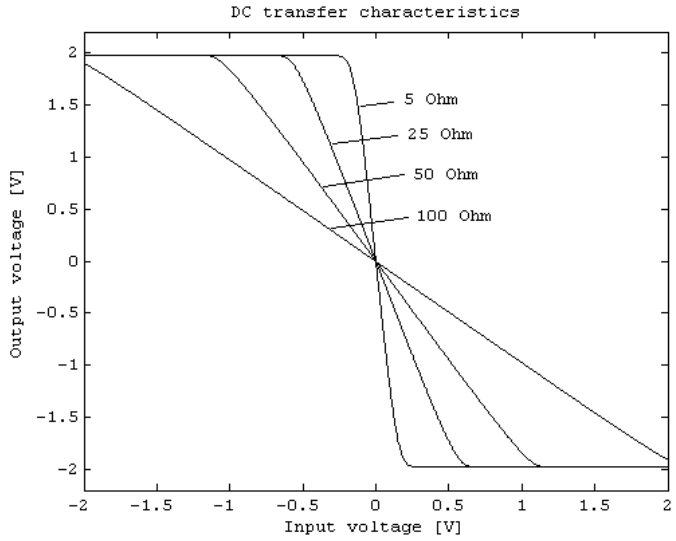


**Figure 2.3:** Plot of the DC input-output characteristics for an emitter-coupled pair with emitter degeneration resistances, calculated with MATLAB. The circuit is biased by a $I_{Tail}$ current of 20 mA, the common-base current gain is chosen as $\alpha_F = 0.99$ and the collector resistance $R_C$ is equal to 100 Ω. To show the influence of the emitter degeneration resistance, $R_E$ values of 5, 25, 50 and 100 Ω are applied. Increasing the emitter degeneration resistance leads to an extension of the linear region, but also to a decrease of voltage gain.

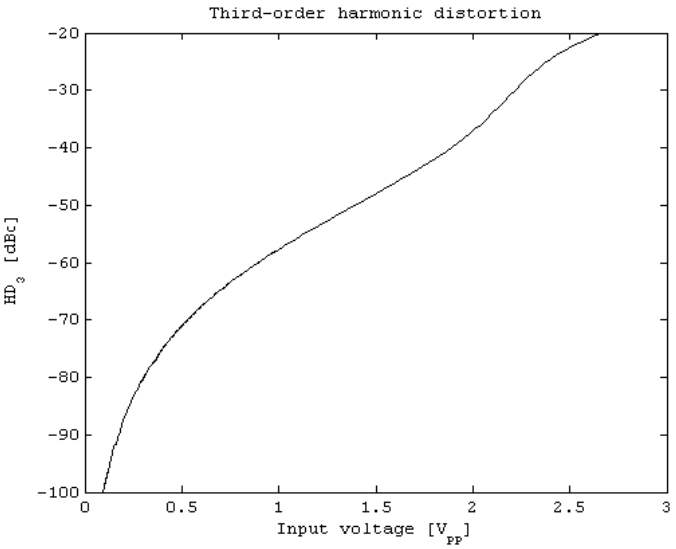


**Figure 2.4:** Plot of the third-order harmonic distortion $HD_3$ vs. input voltage for an emitter-coupled pair with emitter degeneration resistors, calculated with MATLAB. The emitter degeneration resistance is chosen as $R_E = 45\,\Omega$ to obtain a voltage gain of $A_d = 2$, otherwise the same conditions as for Figure 2.3 apply. $HD_3$ is equal to −80 dBc at an input voltage of about 302 $mV_{pp}$.

### 2.2.3 Emitter-coupled pair with diode-connected load

Despite emitter degeneration, the emitter-coupled pair with emitter degeneration resistors still lacks sufficient linearity, even if the region of operation is already improved by this measure. The main reason for the non-linearity is that the base-emitter voltages $V_{be1}$ and $V_{be2}$ do not change by same amounts when changing the differential input voltage. Thus, the effective emitter degeneration resistances on the two sides of the differential pair are not identical. This results in a non-constant mismatch of the circuit, which varies as a function of the input voltage, and which is the principal source of distortions. This distortion can be compensated by adding diodes in series to the collector resistors [10].

#### Linearisation method

The effective emitter degeneration resistance $\tilde{R}_E$ is composed of the degeneration resistor $R_E$, the differential emitter resistance $r_e$, the input signal source resistance $R_S$ and the base spreading resistance $R_{BB'}$ divided by the forward current gain, as well as a bulk resistor $R_{E\ conn}$ for the emitter connection.

$$\tilde{R}_E = R_E + R_{E\ conn} + \frac{R_S + R_{BB'}}{\beta_F + 1} + r_e \tag{2.36}$$

By assuming an input-independent forward current gain $\beta_F$, the influence of the resistances located on the base side of the transistor can be assumed to be constant, and can therefore be combined with the emitter connection resistance to a constant $R_A$. Hence, the effective emitter degeneration resistance can be presented as

$$\tilde{R}_E = R_E + R_A + r_e \tag{2.37}$$

The differential emitter resistance $r_e$ is dependent on the current flow through the transistor, and is therefore the only value, which is dependent of the input voltage. Its value is calculated by differentiating the diode law relationship.

$$I = I_S \cdot \exp\left(\frac{V}{V_T}\right) \tag{2.38}$$

$$\frac{dI}{dV} = \frac{1}{V_T} I_S \cdot \exp\left(\frac{V}{V_T}\right) = \frac{I}{V_T} \tag{2.39}$$

$$r_e = \frac{dV}{dI} = \frac{V_T}{I} \tag{2.40}$$

Applying a differential input voltage to the circuit causes a change in voltage drop-off of $\pm\frac{V_{id}}{2}$ across the two effective emitter degeneration resistances $\tilde{R}_{e1}$ and $\tilde{R}_{e2}$. This increases the current through one path by $\Delta I$, and decreases it by the same amount through the other path of the differential pair, yielding two different emitter currents and therefore two unequal differential emitter resistances

$$r_{e1} = \frac{V_T}{\frac{I_{Tail}}{2} + \Delta I} \tag{2.41}$$

$$r_{e2} = \frac{V_T}{\frac{I_{Tail}}{2} - \Delta I} \tag{2.42}$$

The current change $\Delta I$ is calculated by dividing the voltage change $V_{id}$ through the sum of the effective emitter degeneration resistors.

$$\Delta I = \frac{V_{id}}{\tilde{R}_{E1} + \tilde{R}_{E2}} \tag{2.43}$$

The sum $\tilde{\mathrm{R}}_{\mathrm{E1}} + \tilde{\mathrm{R}}_{\mathrm{E2}}$ should ideally be constant to have a constant relation between $\Delta$I and $\mathrm{V_{id}}$, but it is a function of $\mathrm{V_{id}}$ and therefore the relation between differential input voltage and differential emitter current is not constant.

$$\tilde{R}_{E1} + \tilde{R}_{E2} = 2R_E + 2R_A + r_{e1} + r_{r2} = \tag{2.44}$$

$$= 2R_E + 2R_A + V_T \cdot \frac{I_{Tail}}{\left(\frac{I_{Tail}}{2}\right)^2 - \left(\frac{V_{id}}{\tilde{R}_{E1}+\tilde{R}_{E2}}\right)^2} \tag{2.45}$$

The circuit can be linearised by adding n diodes to the collector resistances of the circuit. To obtain the same component properties for the diodes and the principal transistors $\mathrm{Q_1}$ and $\mathrm{Q_2}$ of the pair, the diodes should be built of transistor with the same dimensions as $\mathrm{Q_1}$ and $\mathrm{Q_2}$. When diodes are added, the collector resistor value $\mathrm{R_C}$ has to be n times the value of the emitter degeneration resistor $\mathrm{R_E}$ to obtain the optimal compensation of non-linearity.

$$R_C = nR_E \tag{2.46}$$

Assuming the simplification $\alpha_{\mathrm{F}} = 1$ and neglecting different values for the source resistance $\mathrm{R_S}$, the effective collector resistances, which include the resistors and the diodes, are equal to

$$\tilde{R}_{C1} = n\tilde{R}_{E1} = R_C + nR_A + nr_{e1} \tag{2.47}$$

$$\tilde{R}_{C2} = n\tilde{R}_{E2} = R_C + nR_A + nr_{e2} \tag{2.48}$$

The voltage gain obtained by this configuration is

$$A_d = \frac{V_{od}}{V_{id}} = \frac{\Delta I \cdot \left(\tilde{R}_{C1} + \tilde{R}_{C2}\right)}{\Delta I \cdot \left(\tilde{R}_{E1} + \tilde{R}_{E2}\right)} = n \tag{2.49}$$

To obtain the best linearity performance, the ratio between emitter and collector resistance needs to correspond with the number of diodes n. The voltage gain then is also equal to n. It can only have integer values, which may be a limitation in some applications.

If additional non-linearity sources did not exist and the simplifications taken had no influence, the circuit would be perfectly linear, always preconditioned that the input voltage is low enough to avoid clipping. Nevertheless, even under real conditions the circuit shows very high linearity.

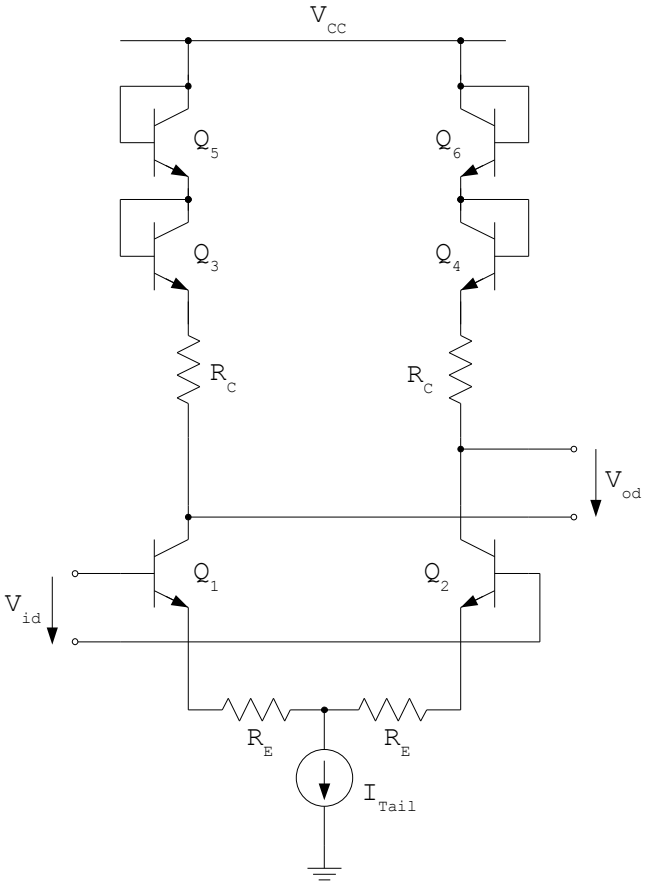


**Figure 2.5:** Scheme of the emitter-coupled pair with diode-connected load

### 2.2.4 Compensated cascode

The compensated cascode is a highly linear topology, presented by Quinn [11]. It is based on the simple cascode technology, improved by a compensation amplifier, which corrects the main non-linear effect of the cascode.

#### Cascode principle

The simple cascode configuration is a common-emitter common-base amplifier, as shown in Figure 2.6. The collector of the common-emitter transistor $Q_1$ is connected to the emitter of the common-base transistor $Q_3$. The base of the common-base transistor is biased at a fixed voltage level, thus the collector node of the common-emitter transistor is also fixed at a virtually constant voltage level, apart from small variations of the base-emitter voltage of $Q_3$. As the collector voltage of $Q_1$ is kept constant, the Early-Effect due to base-width modulation is avoided for this transistor, which leads to a reduction of non-linearity caused by this effect [12]. The ratio between the emitter and the collector current of $Q_1$ is nearly constant, thus the overall transconductance of the cascode amplifier is more linear, due to reduction of base-width modulation, than the transconductance of a simple common-emitter stage.

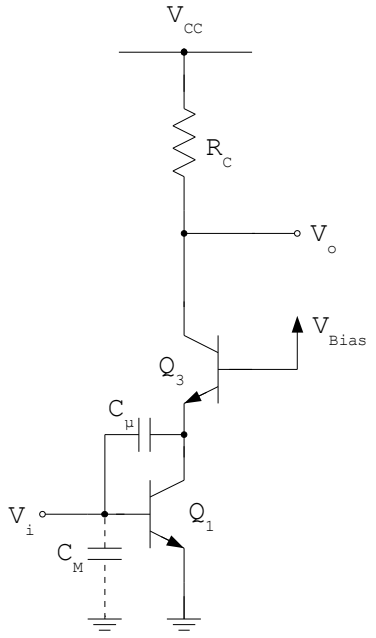


**Figure 2.6:** Cascode principle

Another positive effect of the cascode configuration is the increase of bandwidth. A simple common-emitter stage sustains bandwidth degradation because of the Miller effect. Seen from the input side of the common-emitter amplifier, the effect of the parasitic base-collector capacitance $C_\mu$ is multiplied by a factor nearly proportional to the voltage gain A, obtaining an increased input capacitance $C_M$.

$$C_M = C_\mu \cdot (1 + |A|) \tag{2.50}$$

The collector of the common-emitter transistor of the cascode topology is kept at a constant level, thus the Miller capacitance is strongly reduced to $C_M \approx 2C_\mu$. The common-base transistor is biased at a constant base voltage level, a priori avoiding the Miller effect. The result of the decrease of the Miller effect is an increase of bandwidth.

**Linearisation method**

The main source of non-linearity for emitter-coupled pairs with emitter degeneration resistors, which are based on the cascode topology, is the same as for the other emitter-coupled pairs presented. The base-emitter voltages of the principal transistors $Q_1$ and $Q_2$ do not have the same value, if the currents flowing through them are not equal due to a differential input voltage. The undesired difference $\Delta V_{be} = \Delta V_{be1} - \Delta V_{be2}$ between the emitters of the two common-emitter transistors $Q_1$ and $Q_2$ also exists as a nearly identical replica $\Delta V'_{be} = \Delta V_{be3} - \Delta V_{be4}$ between the emitters of the common-base transistors $Q_3$ and $Q_4$. This replica is sensed by another emitter-coupled pair $Q_5$-$Q_6$ with emitter degeneration, which builds the compensation amplifier with a certain transconductance $G_m$. The sensed error signal $\Delta V'_{be}$ is amplified and the error currents at the outputs of the compensation amplifier are subtracted from the inaccurate output currents of the cascode amplifier. The non-linearity caused by the systematic $\Delta V_{be}$ error is nearly completely compensated, if an appropriate value for $G_m$ is chosen.

The differential output current $\Delta I_o$ can be expressed by

$$\Delta I_o = \frac{V_{id}}{2R_E} - \frac{V_{be}}{R_E} + V_{be'} \cdot G_M \tag{2.51}$$

Thus, compensation is achieved, if the compensation amplifier transconductance $G_M$ is equal to the conductance value $R_E^{-1}$ of the emitter degeneration resistors of the principal differential pair. $G_M$ is determined by the emitter degeneration resistors $R_A$ of the correction amplifier. $R_A$ is therefore the variable, which has to be optimised to obtain a maximum of linearity.

After compensation there are still several systematic error sources. Sensing $\Delta V_{be'}$ and not $\Delta V_{be}$ is one of them. Moreover, the compensation amplifier itself is non-linear, but as the error signal is small, its non-linearity does not have a big impact. It also has finite bandwidth, causing lower non-linearity compensation at higher frequencies.
The disadvantages of the compensated cascode are an increased number of components and therefore increased noise, the need for a biasing voltage and two current sources, as well as the need for high supply voltage as with the current sources and the cascode there are at least three transistors connected in series. Nevertheless, the advantages of this topology outweigh the problems. A high gain, determined by the emitter degeneration resistors $R_E$, can be achieved by at the same time staying highly linear.

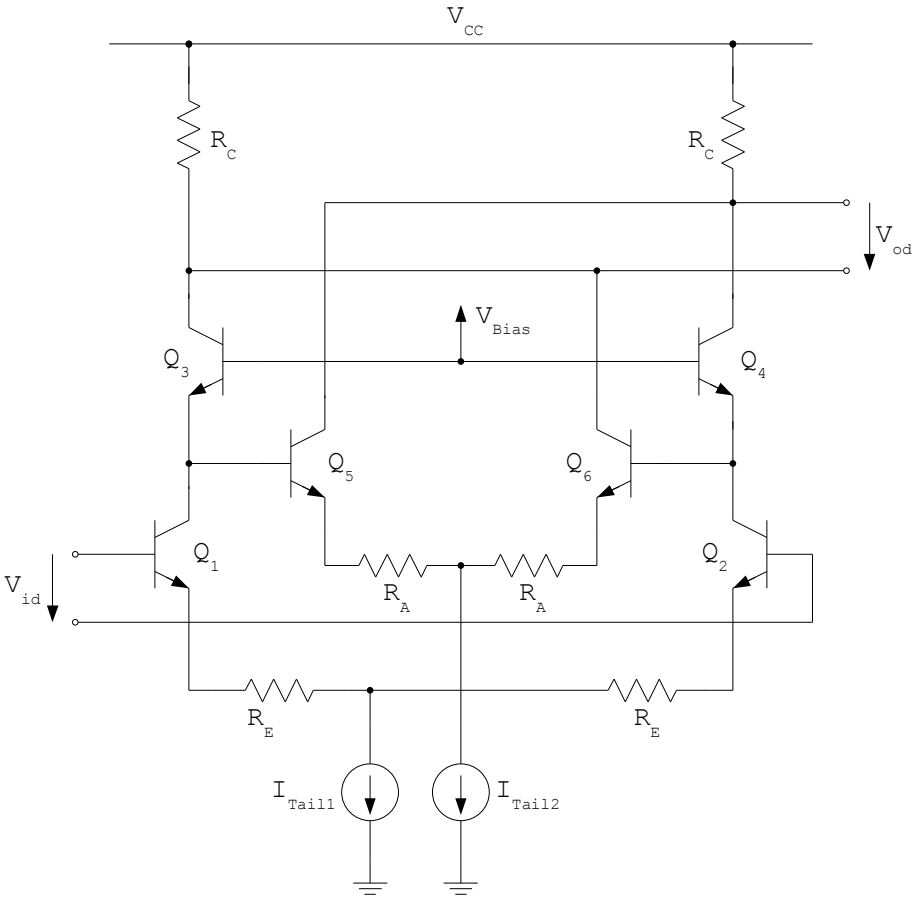


**Figure 2.7:** Scheme of the compensated cascode

### 2.2.5 Cherry-Hooper

This differential amplifier topology has a high gain-bandwidth product. Its functional principle, developed by Cherry and Hooper [13], is a strong impedance mismatch between successive amplifier stages, which acts as a decoupling mechanism and provides high bandwidth. Nowadays Cherry-Hooper amplifiers are widely used in high speed applications like amplifiers in fibre-optic systems. For instance, Baeyens et al. [14] proposed a 40 Gbit/s limiting amplifier chain with three Cherry-Hooper amplifiers, and Choudhury et al. [15] presented a 50 GHz bandwidth amplifier chain with four amplifiers.

A Cherry-Hooper amplifier consists of two stages, each one of them with feedback. A first transadmittance stage ($Q_1$ and $Q_2$) with optional series feedback in form of emitter degeneration resistors $R_{E1}$ converts the differential input voltage into an output current. This stage has high input and output impedance and is terminated by a stage with low input impedance, to obtain sufficient impedance mismatch. So the transadmittance stage is followed by a transimpedance stage, built by the transistors $Q_3$ and $Q_4$, which has low input and output impedance, and needs to be driven by a current source, which is the case as it is connected to the transadmittance stage. The shunt feedback of the second stage is realised by feedback-resistors $R_F$ and the emitter followers $Q_5$ and $Q_6$. Due to the low output impedance of the transimpedance stage, the load impedance of the overall Cherry-Hooper amplifier should be high. As a modification, the resistors $R_2$ have been added by Greshishchev and Schvan [16], to increase the voltage gain of the circuit.

The DC characteristics of the amplifier, which are derived in [17] for an amplifier without emitter degeneration, show several sources of non-linearity. The voltage at the output of the transadmittance stage respective of the input of the transimpedance stage is given by

$$V_2 - V_1 \approx R_1 I_{Tail2} \cdot \tanh\left(\frac{V_2 - V_1}{2V_T}\right) + R_F I_{Tail1} \cdot \tanh\left(\frac{-V_{id}}{2V_T}\right) + V_{be6}\left(V_{id}\right) - V_{be5}\left(V_{id}\right) \tag{2.52}$$

The first term represents the shunt feedback of the transimpedance stage, the second term the input voltage as it would be amplified, if only the transadmittance stage itself would exist. Both terms contain the hyperbolic tangent function, which creates odd-order harmonics as it has been described for the simple emitter-coupled pair. An additional disturbance factor is the non-linear relation between the base-emitter voltages and the collector currents of the feedback emitter-followers $Q_5$ and $Q_6$.
The solution for $V_2 - V_1$ has to be found numerically. Subsequently, the overall output voltage can be calculated by a hyperbolic tangent relation.

$$V_{od} \approx \left(R_1 + R_2\right) I_{Tail2} \cdot \tanh\left(\frac{V_2 - V_1}{2V_T}\right) \tag{2.53}$$

The focus of the widely used Cherry-Hooper amplifier definitely lies on bandwidth, it is not optimised for linearity. For sufficient linearity additional external feedback would be necessary, which substantially lowers gain and bandwidth and counteracts the advantages of this topology.

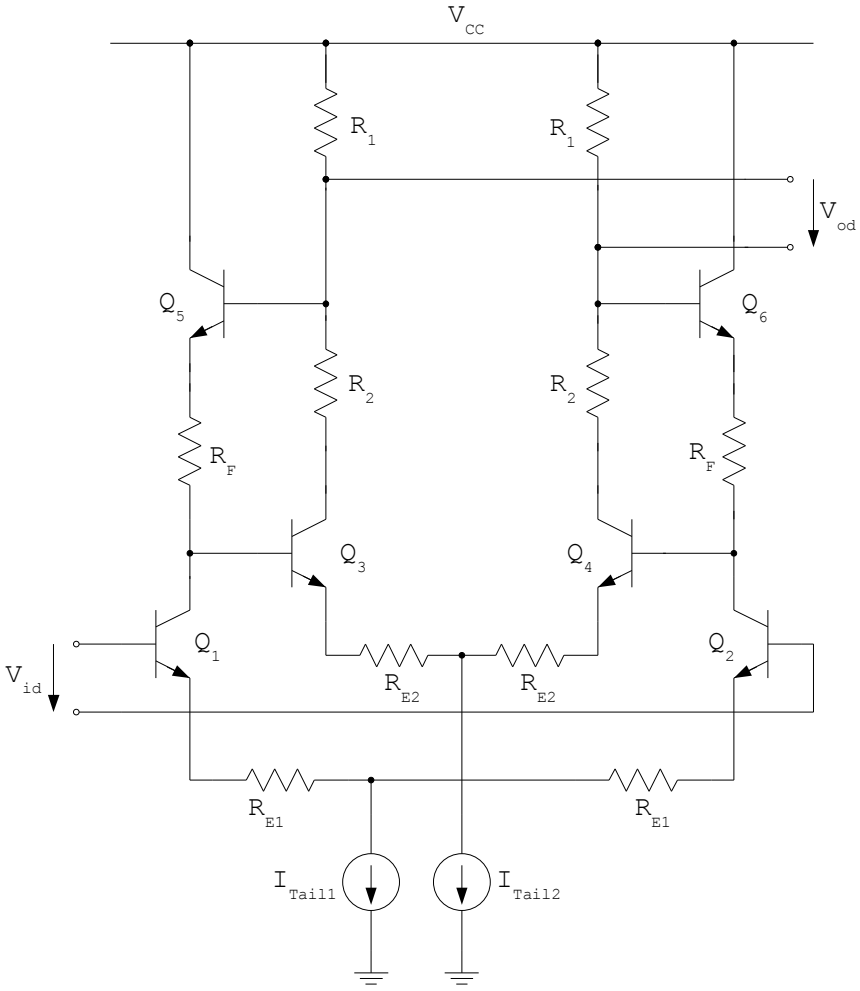


**Figure 2.8:** Scheme of the Cherry-Hooper differential amplifier

### 2.2.6 Miki

This is another topology based on the differential pair with emitter degeneration and linearisation by correcting the $\Delta V_{be}$ distortion. It was first presented by Miki et al., who used it as a signal buffer in a broadband analogue-to-digital converter [18].
The Miki configuration consists of two differential pairs with emitter degeneration (Figure 2.9). The inner differential pair $Q_1$-$Q_2$ acts as the gain section of the amplifier. The second differential pair $Q_3$-$Q_4$ creates replicas of the collector currents of the first differential pair. These currents create approximately the same $\Delta V_{be}$ distortions at the emitter followers $Q_5$ and $Q_6$, which counteract the nonlinear behaviour of the first differential pair $Q_1$-$Q_2$.
For a given configuration of $R_{E1}$ and $R_1$, the outer differential pair $Q_5$-$Q_6$ needs an appropriate value of resistor $R_{E2}$ to minimise distortions. The following derivation shows the functionality of the linearisation of this topology, as well as defining the ideal choice of $R_{E2}$.

#### Linearisation method

Using the diode-law equation and neglecting the Early-effect, the base-emitter voltages of the transistors $Q_1$ and $Q_2$ of the inner differential pair as functions of their collector currents are equal to

$$V_{be1} = V_T \cdot \ln\left(\frac{I_{Tail1} + \Delta I}{I_S}\right) = V_{be} + \Delta V_{be1} \tag{2.54}$$

$$V_{be2} = V_T \cdot \ln\left(\frac{I_{Tail1} - \Delta I}{I_S}\right) = V_{be} + \Delta V_{be2} \tag{2.55}$$

The current change $\Delta I$ caused by the differential input voltage $V_{id}$ is

$$\Delta I_1 = \frac{V_{id} - \Delta V_{be1} + \Delta V_{be2}}{2R_{E1}} \tag{2.56}$$

The differential voltage $V_{12}$ between the collectors of $Q_1$ and $Q_2$ can be calculated by

$$V_{12} = -2\Delta I_1 \cdot R_C = -\frac{R_C}{R_{E1}} \cdot (V_{id} - \Delta V_{be1} + \Delta V_{be2}) \tag{2.57}$$

Considering the unequal voltage drop-offs $V_{be5}$ and $V_{be6}$ at the emitter followers $Q_5$ and $Q_6$, the differential output voltage is equal to

$$V_{od} = -\frac{R_C}{R_{E1}} \cdot V_{id} + \frac{R_C}{R_{E1}} \cdot \Delta V_{be1} - \Delta V_{be5} + \frac{R_C}{R_{E1}} \cdot \Delta V_{be2} - \Delta V_{be6} \tag{2.58}$$

Compensation is reached, when the base-emitter voltage changes of the emitter followers $Q_5$ and $Q_6$ exactly counteract the amplified base-emitter voltage changes of $Q_1$ and $Q_2$.

$$\frac{R_C}{R_{E1}} \cdot \Delta V_{be1} = \Delta V_{be5} \tag{2.59}$$

$$\frac{R_C}{R_{E1}} \cdot \Delta V_{be2} = \Delta V_{be6} \tag{2.60}$$

The development of $V_{be}$ into a power series

$$V_{be} = V_T \cdot \ln\left(\frac{I_{Tail} + \Delta I}{I_S}\right) = V_T \cdot \left(\ln\left(\frac{I_{Tail}}{I_S}\right) + \frac{\Delta I}{I_S} + \frac{\Delta I^2}{2I_S^2} + \frac{\Delta I^3}{3I_S^3} + \ldots\right) \tag{2.61}$$

shows, that $\Delta V_{be}$ can be linearly approximated by

$$\Delta V_{be} \approx V_T \cdot \frac{\Delta I}{I_S} \tag{2.62}$$

Due to symmetry, only one of the Equations 2.59 and 2.60 has to be considered and can be expressed as

$$\frac{R_C}{R_{E1}} \cdot V_T \cdot \frac{\Delta I_1}{I_S} = V_T \cdot \frac{\Delta I_2}{I_S} \tag{2.63}$$

The current change $\Delta I_2$ in the outer differential pair has to be greater by the factor $\frac{R_C}{R_{E1}}$ than the current change $\Delta I_1$ in the inner pair. This factor is equal to the differential voltage gain $A_d$. As the same input voltage is applied to the outer and the inner pair, this can be reached by choosing the degeneration resistor $R_{E2}$ as

$$R_{E2} = \frac{R_{E1}}{R_C} \cdot R_{E1} = \frac{1}{A_d} \cdot R_{E1} \tag{2.64}$$

Applying this value for $R_{E2}$ leads to the compensation of non-linearity.

In summary, the amplifier topology presented by Miki et al. has high linearity due to the compensation and a gain, which can be chosen by the resistances $R_{E1}$ and $R_C$.

### Output resistance

Despite these advantages, this topology has a major drawback. Its output is formed by an emitter follower, thus it has low impedance. The output impedance cannot freely be defined according to the given specifications, meaning it cannot be adapted to the following filter stage. In addition, an emitter follower at the output of an amplifier stage leads to stability problems, if the input buffer of the succeeding amplifier stage is also built by an emitter follower.

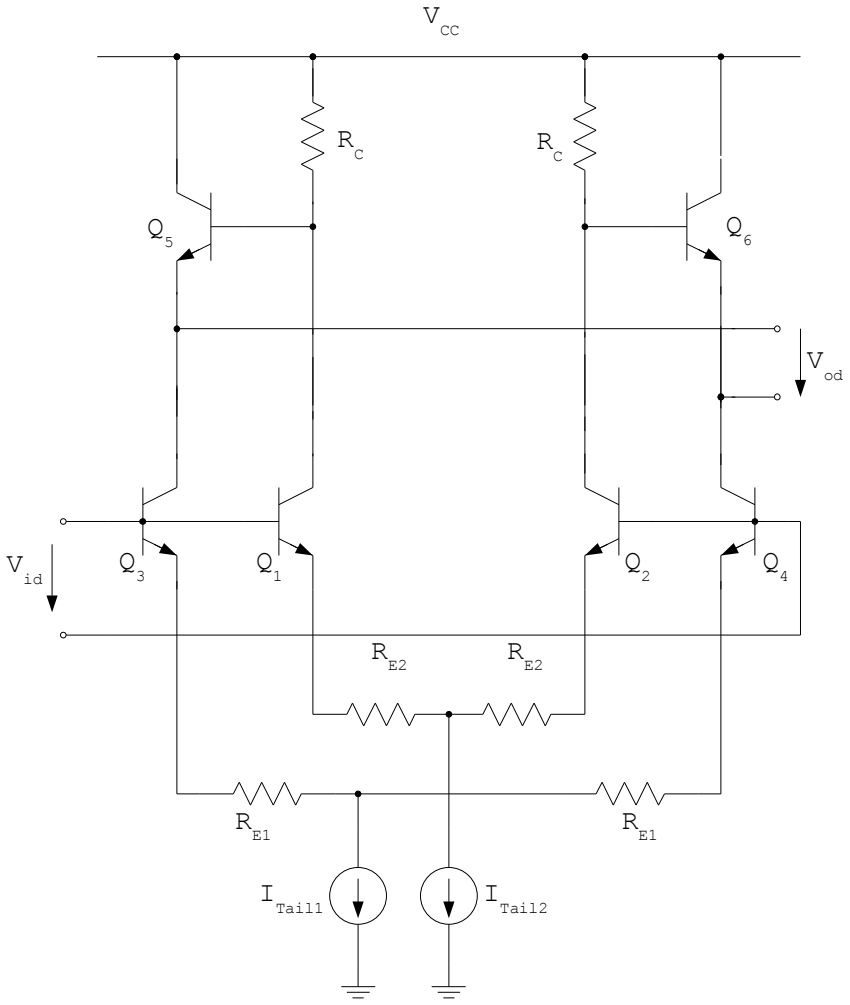


**Figure 2.9:** Scheme of the Miki topology

### 2.2.7 Cross-coupled differential pair

Figure 2.10 depicts a cross coupled differential pair. It is built of four transistors. The principal transistors $Q_1$ and $Q_2$ of the differential pair amplify the input signal. The correction transistors $Q_3$ and $Q_4$ have their bases cross-connected to the emitters of the principal transistors of the respective other path of the pair. The emitter degeneration resistor defines the voltage gain of the circuit. The first publication of this topology, also referred to as differential quartet, has been made by Pookaiyaudom et al. [19].
Like the emitter-coupled pair with diode-connected load or the compensated cascode, this circuit compensates the principal non-linearity of differential pairs, i.e. the non-linear relation between the collector current $I_c$ and the base-emitter voltage $V_{be}$ of the transistors. In the following description of the circuit's functionality, a common-base current gain $\alpha_F = 1$ is assumed, therefore no base currents have to be considered. However, this simplification is not needed if a base current compensation circuit is applied to the cross-coupled differential pair, as it is also proposed by Pookaiyaudom as an optional improvement of the topology.

#### Linearisation method

In the first path of the differential amplifier, the same current $I_{Tail} + \Delta I$ flows through the transistors $Q_1$ and $Q_3$, assuming that, as mentioned above, the base currents are negligible. The current through the second path, and therefore through transistors $Q_2$ and $Q_4$, is equal to $I_{Tail} - \Delta I$. The base-emitter voltages of transistors $Q_1$ and $Q_3$ are of the same value $V_{be1}$, when second order effects like base-width modulation are neglected and only a dependency on the collector current is presumed. The base-emitter voltages of the other two transistors are equal to $V_{be2}$. Due to cross-coupling, the voltage sums across the series-connections $Q_1$-$Q_4$ and $Q_2$-$Q_3$ are the same. Thus, the voltage at the emitter degeneration resistor is an exact replica of the differential input voltage, leading to a constant relation between the current through the resistor and the input voltage, and compensation is reached.

If base spreading resistances as well as emitter bulk and contact resistances are small, the transconductance $G_M$ of the circuit is approximately defined by the reciprocal value of the resistance $2R_E$ and is virtually constant over a large range of operation. The voltage gain of the overall circuit is

$$V_d = G_M \cdot 2R_C = \frac{R_C}{R_E} \tag{2.65}$$

#### Stability issues

The circuit has a major disadvantage. It uses positive feedback and it has a negative input resistance, which means that it is only conditionally stable. To stabilise the circuit, at the input a small positive resistor $R_S$ has to be put in parallel to the large negative input resistance to obtain an overall resistance nearly equal to the additional small positive resistor, which stabilises the circuit. The absolute value of the negative input resistance decreases with rising frequency, so a capacitor is needed in parallel to the small resistor, to assure stabilisation over the whole frequency range. This stabilisation leads to a undesired low input impedance of the circuit.
Because of the stability concerns and the resulting low input impedance, this approach was not pursued further.

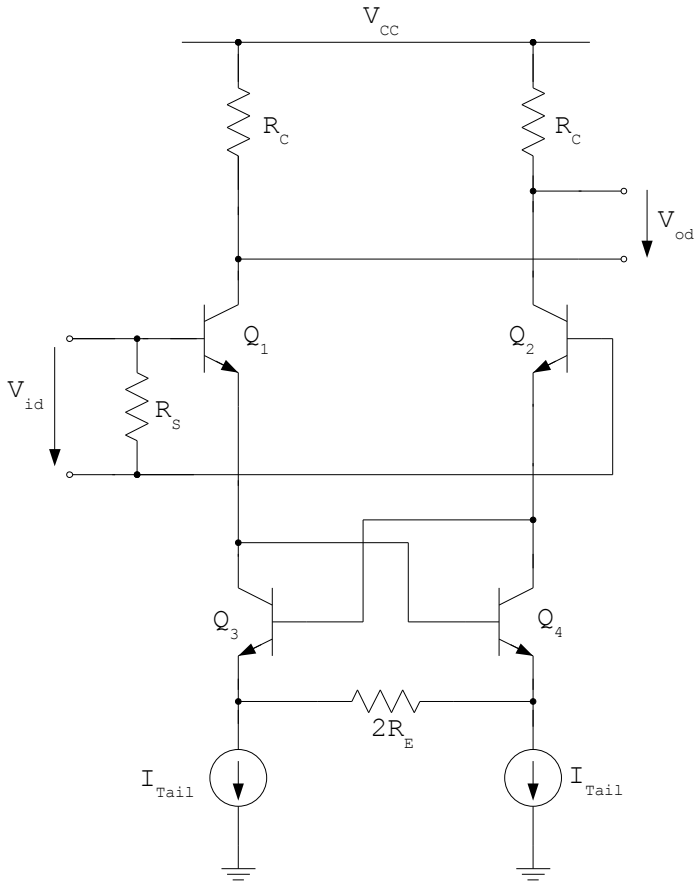


**Figure 2.10:** Scheme of the cross-coupled differential pair

### 2.2.8 Multi-tanh principle

Multi-tanh cells [20] are groups of emitter-coupled differential pairs with their inputs and outputs connected in parallel. The individual hyperbolic tangent DC characteristics are separated along the input voltage range and added together. The sum of the individual characteristics builds a more linear overall circuit. Multi-tanh cells of order n consist of n differential pairs with n tanh-functions, all with different offsets. Each of the differential pairs is fed by an individual biasing current stemming from one of the n tail current sources.

The overall output current is obtained by summing the individual characteristics.

$$\Delta I_o = \sum_{j=1}^{n} I_j \cdot \tanh\left(\frac{V_{id} - V_{off_j}}{2V_T}\right) \tag{2.66}$$

Differentiation yields the transconductance $G_m$ of the overall circuit.

$$G_m = \sum_{j=1}^{n} \frac{I_j}{2V_T} \cdot \operatorname{sech}^2\left(\frac{V_{id} - V_{off_j}}{2V_T}\right) \tag{2.67}$$

There are several ways of creating the offset of the tanh function. All of them are based on unbalancing the differential pairs. For cells with low order n the most simple method is the one of using unequal emitter areas of the two transistors of a pair. The emitter-area ratios and biasing currents of the pairs of the several stages of a multi-tanh cell have to be optimised to obtain a maximum of linearity. Offset voltages can also be introduced by connecting the bases of the different transistors by resistors. The resistors are also connected to current-sources, which cause the offset-voltage drop-offs across them. The emitter-area and offset-resistor methods can also be combined, which is useful for higher-order multi-tanh cells, which would otherwise need high emitter-area ratios to obtain the wanted shifts of the tanh-characteristics. To make the circuits more robust against emitter-area mismatches, slightly deviant tail currents or varying ohmic resistances at the accesses to the nodes of the transistors, emitter degeneration resistors can be added to the differential pairs.

The most simple application of the multi-tanh principle is the multi-tanh doublet. It is made of two differential pairs, each with an emitter-area ratio of A = 3.75 and both of them biased by the same tail current. According to the simulations of Gilbert [20], a $HD_3$ third-order harmonic distortion level of −80 dBc is reached at a sinusoidal input voltage of 28 mV peak-peak.
The multi-tanh triplet has two differential pairs with offsets, created by an emitter-area ratio of A = 13, and a third differential pair, which is symmetric and only fed by $K = \frac{3}{4}$ of the bias current of the other two pairs. With this topology, the $HD_3$ limit is reached for a sinusoidal input voltage of about 63 mV peak-peak.
To obtain higher linearity, higher order multi-tanh cells have to be used. Quadlets already have a maximum emitter-area ratio of A = 79, quintlets even need a maximum ratio of A = 190. While the complexity of the circuits is considerably increasing, the advantages in terms of linearity are not high.

#### Summary

For high linearity highly complex circuits with a high number of differential pairs are necessary. Even if the high number of necessary components would not pose problems, higher order *tanh*-cells are not easily realisable due to problems with circuit component tolerances. In addition, at higher frequencies parasitic elements take effect and degrade the circuit performance, limiting the theoretical benefit of higher-order cells. Thus, the use of the multi-*tanh* principle is mostly restricted to low-order cells, which do not provide sufficient linearity. Therefore this approach has not been pursued further.

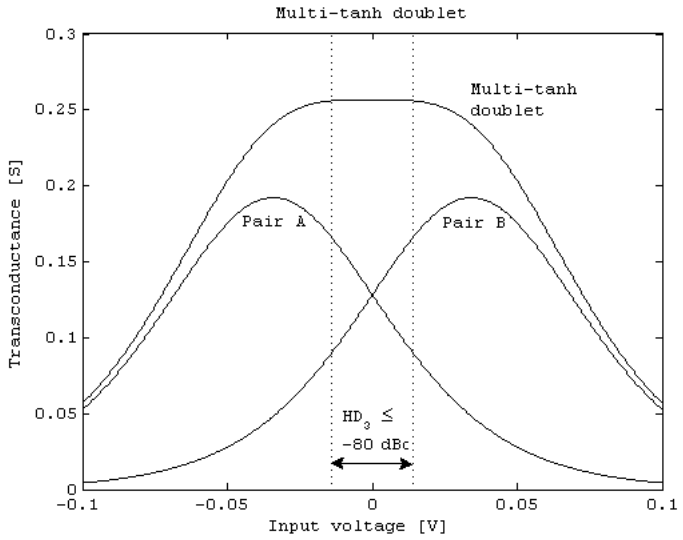


**Figure 2.11:** Transconductance plots of a multi-tanh doublet and its two emitter-coupled differential pair stages, calculated with MATLAB. The offset voltage of the differential pairs is $V_{Off} = \pm 34.2\,mV$, which is obtained by a emitter-area ratio of $A = 3.75$ for both differential pairs. Furthermore, they are both biased with a tail current of $I_{Tail} = 10\,mA$. The highly linear region with a third-order distortion of $HD_3 \leq -80\,dB$ is marked by dotted lines. The borders of this region are at $\pm 14\,mV$ input voltage.

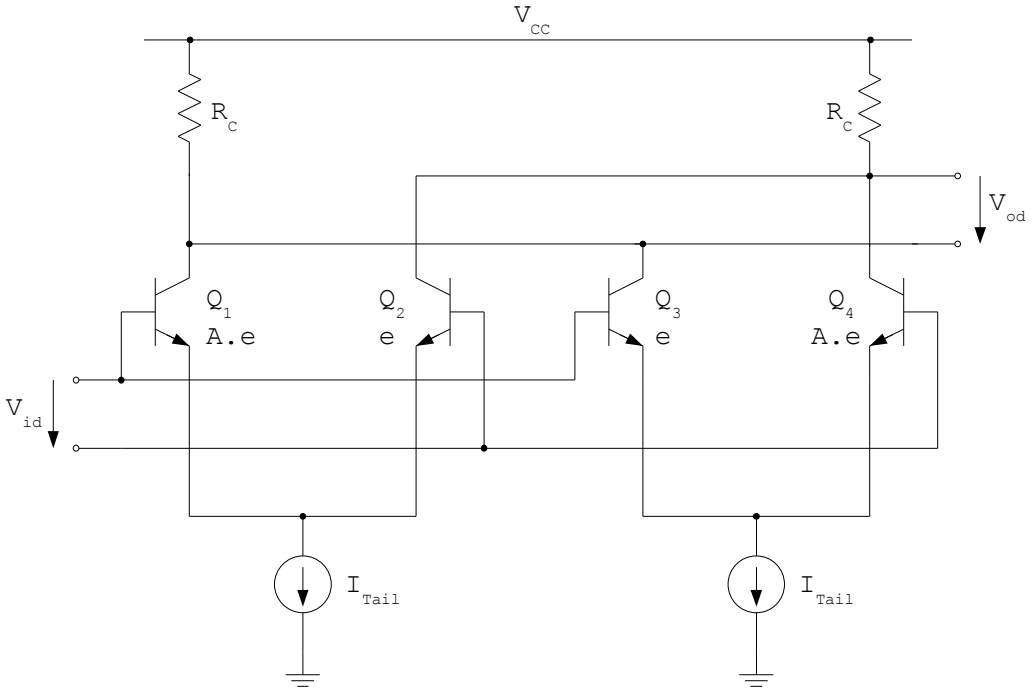


**Figure 2.12:** Scheme of a multi-tanh doublet

## 2.3 Variable-gain topologies

To the author's best knowledge, there do not exist many amplifier topologies, which are highly linear, have high bandwidth, are differential and have variable gain. A preponderant part of reported variable gain amplifiers is based on the Gilbert cell multiplier. An alternative to the Gilbert cell is the quarter-square architecture, however it is only shortly mentioned, because it does not fit the demands of this work.

### 2.3.1 Gilbert cell

The Gilbert cell [21] is an analogue four-quadrant multiplier. The differential output current of the cell is the scaled product of the differential base currents of the two inputs. The inputs can have both positive and negative signs. If the differential voltages and not the differential base currents are considered as the input signals, the output is the product of the hyperbolic tangents of the input voltages, so the Gilbert cell is only linear in case of small input voltages.
This topology is widely used in applications, which base on the principle of multiplication. A practical example is a mixer for frequency conversion in RF receiver front-ends [22, 23]. As the Gilbert cell can also be considered as an amplifier with variable gain, i.e. multiplying a signal with a gain value, it is used for automatic gain control amplifiers in high-bandwidth fibre-optic transmission systems [24, 25, 26]. In this work the cell is solely used as a variable gain amplifier.
The Gilbert cell has two stages (Figure 2.13). The first stage consists of the emitter-coupled pair $Q_1$-$Q_2$ and amplifies the first input signal. It is biased by a tail current source. The current outputs of the first stage are the tail currents of two other emitter-coupled pairs $Q_3$-$Q_4$ and $Q_5$-$Q_6$, who have their collectors cross-coupled. These two pairs build the second stage and amplify the second input voltage. The output currents of the second stage cause the overall output voltage drop-off at the collector resistors $R_C$.

#### DC transfer characteristics

The DC transfer characteristics of the Gilbert cell can be derived [6] by first looking at the relations between the current outputs and the differential input voltage of an emitter-coupled pair, as they have already been mentioned in equations 2.15 and 2.16. The output currents of the first stage are given by

$$I_{c1} = \frac{I_{Tail}}{1 + \exp\left(\frac{-V_{id1}}{V_T}\right)} \tag{2.68}$$

$$I_{c2} = \frac{I_{Tail}}{1 + \exp\left(\frac{V_{id1}}{V_T}\right)} \tag{2.69}$$

For the differential pair $Q_3$-$Q_4$, the tail current is the output current $I_{c1}$ of the pair $Q_1$-$Q_2$. For the pair $Q_5$-$Q_6$, the current $I_{c2}$ has to be taken.

$$I_{c3} = \frac{I_{c1}}{1 + \exp\left(\frac{-V_{id2}}{V_T}\right)} \tag{2.70}$$

$$I_{c4} = \frac{I_{c1}}{1 + \exp\left(\frac{V_{id2}}{V_T}\right)} \tag{2.71}$$

$$I_{c5} = \frac{I_{c2}}{1 + \exp\left(\frac{V_{id2}}{V_T}\right)} \tag{2.72}$$

$$I_{c6} = \frac{I_{c2}}{1 + \exp\left(\frac{-V_{id2}}{V_T}\right)} \tag{2.73}$$

Because of the cross-coupling of the collectors of the second stage, the overall differential output current of the cell is

$$\Delta I = (I_{c3} + I_{c5}) - (I_{c4} + I_{c6}) \tag{2.74}$$

After simplification we can express the differential output voltage as

$$V_{od} = I_{Tail} R_C \cdot \tanh\left(\frac{V_{id1}}{2V_T}\right) \cdot \tanh\left(\frac{V_{id2}}{2V_T}\right) \tag{2.75}$$

Thus, the differential output voltage of the Gilbert cell multiplier is the product of the hyperbolic tangents of the input voltages, resulting in the same linearity problems as already mentioned at the description of the simple emitter-coupled pair. Input voltages, which exceed the value of the thermal voltage $V_T$, already are strongly distorted. Even at fractions of the thermal voltage, the third-order harmonic distortion is too high to comply with the linearity requirements.

### Gilbert cell variations

For the application as an amplifier with variable gain, the two stages of the Gilbert cell have the functions of amplifying the input signal and controlling the gain. The signal amplifier has to be highly linear, whereas the linearity requirements of the gain control stage can be eased to a large extent. To linearise the signal amplifier, the stage consisting of the emitter-coupled pair with transistors $Q_1$ and $Q_2$ can be substituted by another, more linear transadmittance stage. Emitter degeneration is a common linearisation method with low complexity and performance. As an alternative the compensated cascode with its high gain and linearity can be used. There have also been reported class-AB input stages as linearisation methods [22], but they do not support fully differential operation and are therefore not considered as a possible topology for this work.
The gain variation stage cannot be linearised by simply adding emitter degeneration resistances or exchanging the whole emitter-coupled pairs by compensated cascodes, because its functionality is relying on its exponential characteristics. Adding emitter resistors would disturb the output signal. However, the gain does not have to depend linearly on the gain control voltage, and so the gain variation stage with its tanh-characteristic can be left unaltered.
The Gilbert cell can also be modified to obtain higher bandwidth, by applying the principle of the Cherry-Hooper amplifier and exchanging the collector resistances by a transimpedance stage. This costs extra headroom and implies high supply voltage.

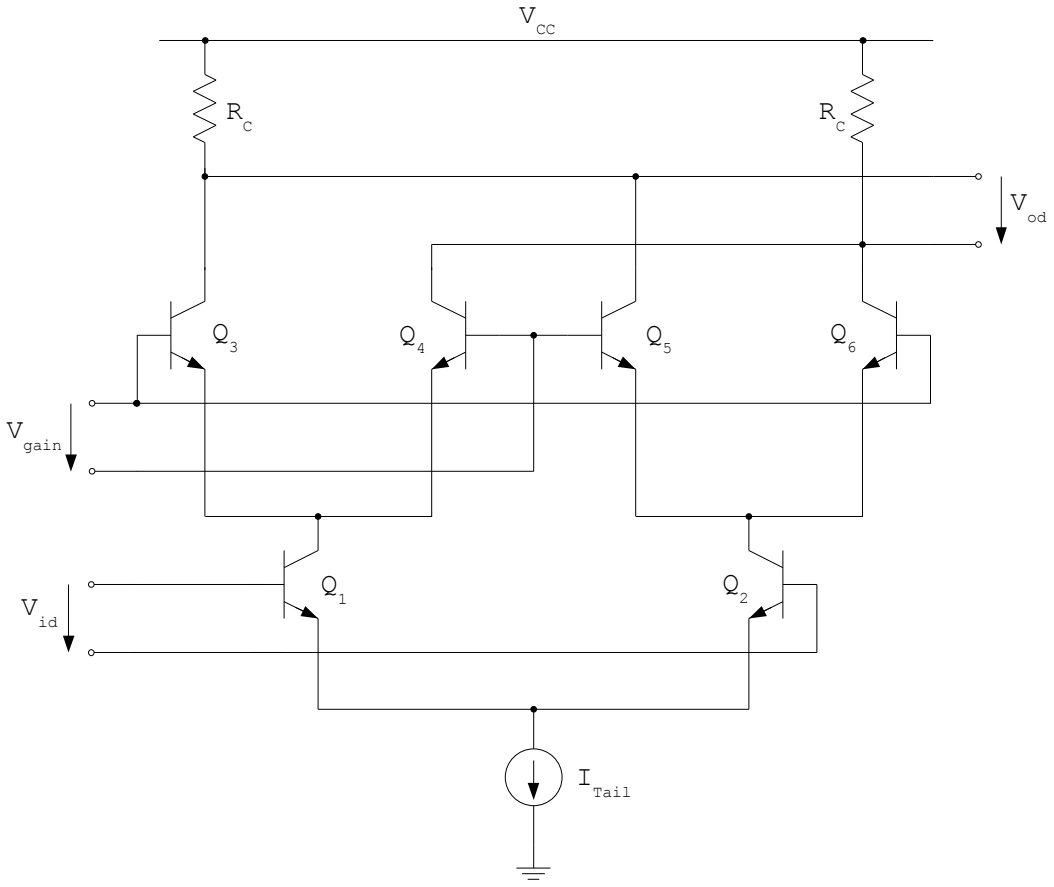


**Figure 2.13:** Scheme of the Gilbert cell topology

### 2.3.2 Quarter-Square Multiplier

Kimura presented an alternative to the Gilbert cell multiplier, based on the quarter-square technique [27], which can be seen in Figure 2.14. This quarter-square multiplier topology consists of two squaring circuits with cross-connected outputs. Each squaring circuit is built of two unbalanced emitter-coupled pairs with a given emitter area ratio. Therefore, the whole circuit has four unbalanced differential pairs.

The emitter area ratio K of an unbalanced differential pair leads to an offset $V_K$ of the DC transfer characteristic. Considering the additions and subtractions of the characteristics of the single differential pairs due to the cross-coupling of their outputs, and using the well-known hyperbolic tangent description of the emitter-coupled pair, the following input-output relation can be defined.

$$\Delta I = \alpha_F I_{Tail} \cdot \left( \tanh\left(\frac{V_1 + V_K}{2V_T}\right) - \tanh\left(\frac{V_1 - V_K}{2V_T}\right) - \tanh\left(\frac{V_2 + V_K}{2V_T}\right) + \tanh\left(\frac{V_2 - V_K}{2V_T}\right)\right) \tag{2.76}$$

Approximation by only considering the constant and linear terms of a power series extension yields

$$\Delta I = -\alpha_F I_{Tail} \frac{\ln K}{4V_T^2} \left(V_1^2 - V_2^2\right) \tag{2.77}$$

The input voltages are substituted.

$$V_1 = V_x - V_y \tag{2.78}$$
$$V_2 = V_x + V_y \tag{2.79}$$

This gives

$$\Delta I = -\alpha_F I_{Tail} \frac{\ln K}{V_T^2} V_x V_y \tag{2.80}$$

Not the multiplicands themselves, but their sum and difference have to be applied to the quarter-square multiplier to obtain their product. An additional adder and a subtractor are needed for correct operation. In addition, the linearity of the circuit is limited, as no non-linearity correction techniques are applied. Therefore this approach has not been pursued further.

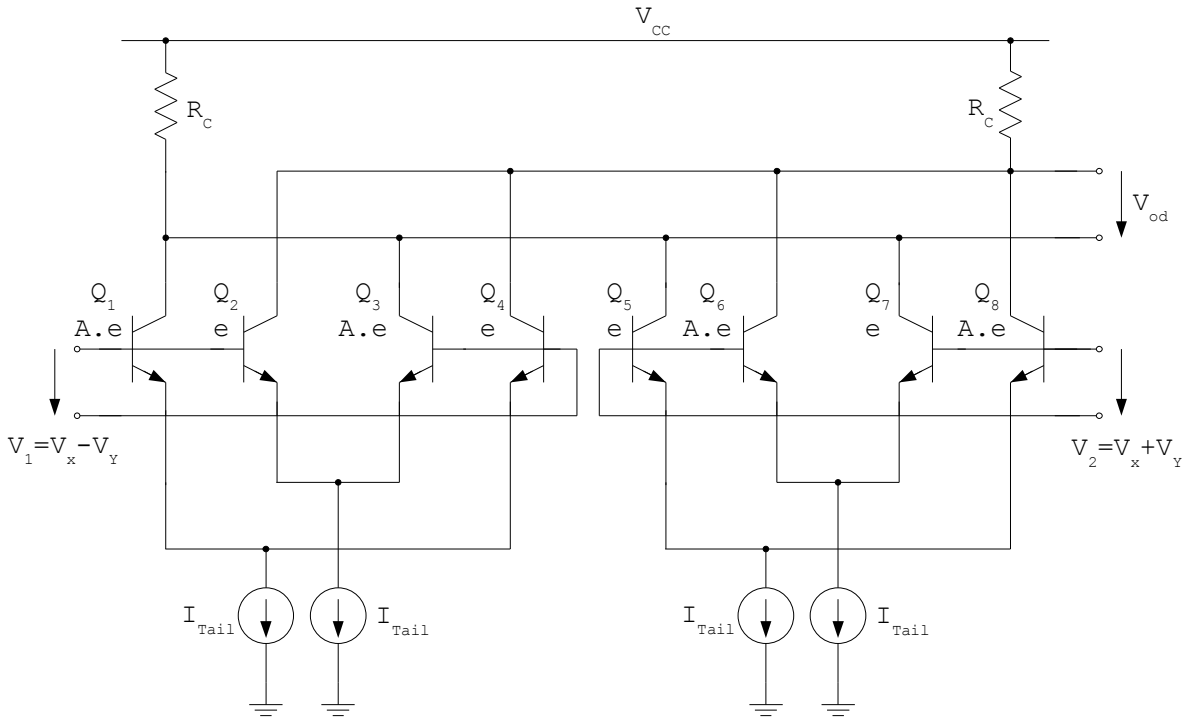


**Figure 2.14:** Scheme of the quarter-square multiplier

## 2.4 Equivalence of emitter degeneration topologies

Emitter degeneration can be implemented by two different topologies. Concerning their primary functionality of gain decrease and linearity increase they are completely equivalent [4].
The structure on the left side of Figure 2.15 consists of two emitter degeneration resistors $R_E$ and a single tail current source $2 \cdot I_{Tail}$. This topology has the advantage of low noise and high stability. The noise created by the current source is acting identically on both paths of the differential pair, which permits to suppress this common-mode noise by the next differential amplifier stage. In addition, simulations have shown that non-ideal current sources, which have finite output resistance, impose stability problems, if they are directly connected to the emitters of the transistors of the differential pair. The instability can be decreased or even avoided by the degeneration resistors connected between the current source and the differential pair transistors. The major disadvantage of this structure is a DC voltage drop-off of $I_{Tail} \cdot R_E$ across the degeneration resistors. Already having supply voltage restrictions, this means an even stronger limitation of available $V_{CE}$ for the transistors of both the current mirror and the amplifier, eventually causing current mirror functionality problems and a decrease in linearity.
The second topology, which is on the right side of Figure 2.15, has its differential pair transistors directly connected to the two $I_{Tail}$ current sources, causing stability issues. Unconditional stability can however be assured by adding additional resistors at the inputs of the differential pair. The differential pair transistor emitter leads are connected by a $2 \cdot R_E$ emitter degeneration resistor. Contrary to the other topology, the current source noise in the two paths of the pair is not correlated and cannot be suppressed by the succeeding amplifier stage. However, there is no voltage drop-off across the degeneration resistors, which provides more headroom for the transistors.

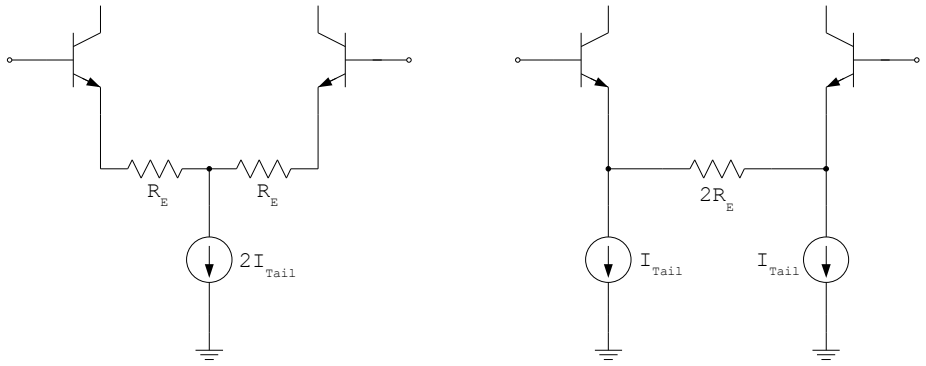


**Figure 2.15:** The principal functionality of the differential pair version on the left side is equivalent to the one on the right side, but differs in terms of noise, stability and required supply voltage.

Both of the topologies have been used in Sections 2.2 and 2.3. They can be substituted depending on the required noise, voltage headroom and stability properties.

## 2.5 Emitter follower

The emitter follower is a transistor in common-collector configuration, biased by a current source. Because of the constant current flow through the transistor, and if the Early effect is neglected, the base-emitter voltage of the transistor always rests constant, independent of the input voltage. The output is a copy of the input signal, only with a shift of the DC level of one $V_{be}$.
The emitter follower has high input impedance and low output impedance, so it can be used for the decoupling of successive amplifier stages. Its DC shift property can be usefully applied, if the output DC level of an amplifier is higher than its input level. The voltage drop-off at the emitter follower lowers the output level and simplifies cascading.

### Harmonic distortion

The third-order harmonic distortion of a single emitter follower transistor has been analysed by Wambacq [7]. The $HD_3$ relation derived by him can also be used for two emitter followers in differential operation.

$$HD_3 \approx \frac{1}{12} \cdot \frac{1}{(g_m R_E)^3} \cdot \frac{V_{id}^2}{V_T^2} \tag{2.81}$$

The emitter follower has local negative feedback, the factor $g_m R_E$ of the above equation is the gain of the feedback [6]. The higher the feedback gain, the more linear the circuit behaviour. Thus, a current source with high output impedance instead of a tail resistor is preferred to bias the emitter follower, and the input impedance of the successive stage should be as high as possible to obtain a high load resistance $R_E$. The transconductance $g_m$ should also be as high as possible. It is determined as

$$g_m = \frac{I_c}{V_T} \tag{2.82}$$

Therefore, a compromise has to be taken between linearity and power consumption. An increased biasing current implicates higher transconductance, feedback gain and linearity, but also causes more power dissipation.

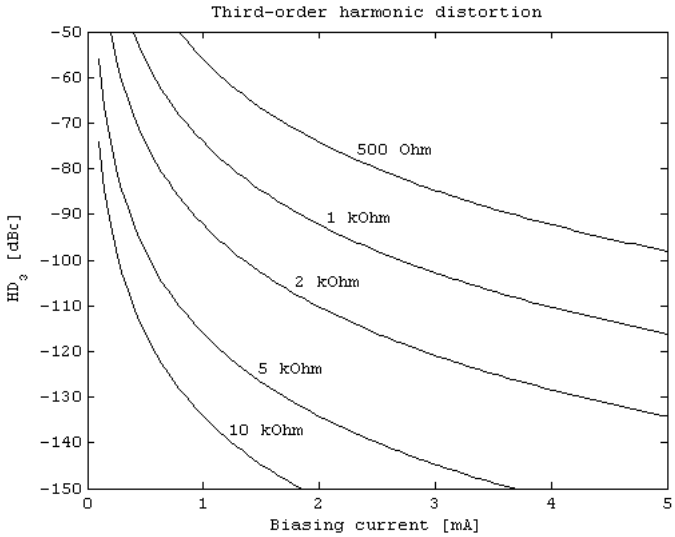


**Figure 2.16:** Plot of the third-order harmonic distortion $HD_3$ vs. biasing current for a varying load resistance $R_E$, according to equation 2.81 and calculated with MATLAB. The input signal is fixed to $600\,mV_{pp}$. For the typical value of $5\,k\Omega$ input resistance of each of the two transistors of the following stage at frequencies in the lower GHz range, a biasing current of $0.25\,mA$ is already sufficiently high for $HD_3 = -80\,dBc$.

### Stability issues

Cascading of multiple emitter followers has to be avoided in all circumstances because of stability problems. Even a single emitter follower has a negative input resistance and is only conditionally stable, therefore it should be stabilised by connecting its base to the power supply by a low resistance.

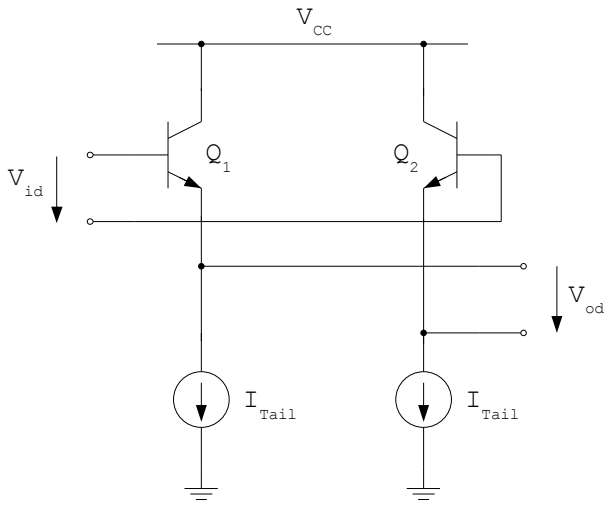


**Figure 2.17:** Scheme of the emitter follower

## 2.6 Selection of the most appropriate amplifier topologies

A first simulation with Cadence/GoldenGate is made to give an overview of the linearity of the fixed-gain amplifiers, which are not a priori excluded based on the precedent topology analysis. The circuits are still not fine-tuned, but the results are sufficiently accurate to be used as a decision support. Based on these simulations the most appropriate fixed-gain amplifier topologies are chosen. Then the topology of the variable-gain amplifier is determined by applying the same procedure as for the fixed-gain amplifier.

### 2.6.1 Fixed-gain topologies

After an analysis of their basic properties, which was done in Section 2.2, the following initially proposed amplifiers cannot be used for the amplifier chain of this work:

- Basic emitter-coupled pair
  Without modifications, the emitter-coupled pair has high gain, but very low linearity.
- Miki topology
  The compensation method of the topology presented by Miki leads to high linearity. Nevertheless this topology cannot be used, because its output consists of an emitter-follower with naturally very low impedance. This is an advantage for several applications, but it is not the case for this work. The filters, which follow the amplifier stages, expect 200 Ω differential output impedance. They are not adapted to the low output impedance of the Miki architecture and would sustain unacceptable changes of their characteristics.
- Cross-coupled differential pair
  The cross-coupling method gives high linearity, but also a negative input resistance due to positive feedback, and therefore it is just conditionally stable. To overcome the stability problems, a low resistance has to be connected in parallel to the input, which stabilises the circuit but also lowers the input impedance. Because of very low input impedance, this topology also has not been considered further.
- Multi-tanh topology
  To obtain high linearity, a large number of differential pairs with large ratios of their emitter areas is needed. The complexity of highly linear circuits is too high and so this approach remains a theoretical example.

The amplifier topologies, which are not yet excluded, are simulated to determine their third-order harmonic distortion. The basic emitter-coupled pair is added for comparison reasons. The emitter follower is simulated as well to prove its high linearity. To obtain comparable results, the simulation conditions are as equal as possible for all circuits. The transistors are biased with 10 mA DC current [1], a value which is high enough to guarantee highly linear operation of the transistors. The bias current is provided by ideal current sources to avoid the additional effects of inaccurate transistor-based current sources. The two collector resistors have values of 100 Ω to provide the 200 Ω differential output resistance demanded by the amplifier specifications. Furthermore, all amplifiers are supplied with a single 5 V source. The topologies are designed to have a voltage gain of 6 dB, and if possible, also versions with a gain of 9 dB are simulated. On a linear scale these are gains of 2.00 and 2.82, respectively.
The most important simulation output is the third-order harmonic distortion $HD_3$ at the maximum output voltage of 600 $mV_{pp}$. The input-voltages $V_{id}$, for which a $HD_3$ of −80 dBc is reached, are also determined. Additionally, the ratios between these voltages and the desired input ranges $V_{id\,lim}$ are also expressed to obtain a normalised measure for comparison purposes. The ratios are calculated based on the following equation, a result greater than one signifies a sufficiently high input range.

$$\frac{V_{id}}{V_{id\,lim}} = \frac{V_{id} \cdot A_d}{V_{od\,max}} = \frac{V_{in} \cdot A_d}{600\,\mathrm{mV}_{pp}} \tag{2.83}$$

[1] An exception is the correction amplifier of the compensated cascode. Its two transistors are biased with 5 mA, to obtain the 2:1 current ratio suggested by Quinn [11] for a maximum of distortion reduction. Another one is the emitter follower with bias currents of 2 mA.

The simulation results are presented in the following table:

| | $HD_3$ [dBc] for $V_{od} = 600\,\mathrm{mV_{pp}}$ | $V_{id}$ [$\mathrm{mV_{pp}}$] for $HD_3 = -80\,\mathrm{dBc}$ | $\frac{V_{id}}{V_{id\,lim}}$ [1] for $HD_3 = -80\,\mathrm{dBc}$ | $A_d$ [dB] |
|---|---|---|---|---|
| D. p. with emitter degeneration | −79.4 | 291 | 0.97 | 6.00 |
| | −75.9 | 158 | 0.74 | 9.00 |
| D. p. with diode-connected load | −86.5 | 436 | 1.45 | 5.96 |
| Compensated cascode | −84.5 | 388 | 1.29 | 6.00 |
| | −86.4 | 289 | 1.36 | 9.00 |
| Cherry-Hooper | −58.4 | 91.2 | 0.30 | 6.00 |
| Basic emitter-coupled d. p. | −46.2 | 7.4 | 0.29 | 27.4 |
| Emitter follower | −136 | > 1000 | > 1 | −0.03 |

**Table 2.1:** Simulation of third-order harmonic distortion of the different fixed-gain amplifier topologies

- Emitter-coupled pair with emitter degeneration
  Two versions with different gains are regarded by choosing different emitter degeneration. With $\mathrm{HD_3} = -79.4\,\mathrm{dBc}$, the 6 dB version exceeds the linearity limit. This distortion level is slightly higher than the theoretical results presented in Figure 2.4. Statistical deviations of the components are assumed to degrade the result even further. A strong increase of the bias current would increase the linearity to an acceptable value, however this means excessive power consumption. The 9 dB version clearly fails the linearity criterion.

- Emitter-coupled pair with diode-connected load
  It is a simple topology with high linearity. Due to the limited supply voltage of 5 V, only two diodes can be used. So this topology is limited to a gain of 6 dB. Three diodes connected in series need too much headroom, because they already cause a voltage drop-off of 2.5 V.
  The version with two diodes shows an excellent linearity of $\mathrm{HD_3} = -86.5\,\mathrm{dBc}$, which is high enough to provide sufficient margin for degradations due to statistical variations of the circuit components.

- Compensated cascode
  This topology is sufficiently linear both for a gain of 6 dB and a higher gain of 9 dB. This topology is an alternative to the differential pair with charge diodes.

- Cherry-Hooper
  As already presumed, the Cherry-Hooper circuit is too non-linear due to the lack of distortion compensation mechanisms.

**Result of the selection process**

Finally, the topologies listed below are selected as fixed gain amplifiers. In the following chapters their design will be optimised and their performances will be exactly analysed.

- Emitter-coupled pair with diode-connected load
  Differential voltage gain $\mathrm{A_d} = 6\,\mathrm{dB}$

- Compensated cascode
  Differential voltage gain realisable in a range of $\mathrm{A_d} = 6$ to 9 dB

These amplifiers can be cascaded by adding emitter followers between the stages. With a $\mathrm{HD_3}$ of less than −130 dBc the emitter followers have virtually no influence on the overall linearity.

### 2.6.2 Variable gain topology

The complex and low-performing quarter-square multiplier is not considered further as a possible topology for the variable gain amplifier. So the used topology is the prevalent Gilbert cell. It consists of a signal amplification stage and a gain variation stage. The gain variation stage reduces the linearity of the signal amplification stage by approximately 3 dB. The topology of the signal amplification stage can be freely chosen, as long as it is a transadmittance stage, i.e. with voltage input and current output. The original Gilbert cell uses the basic emitter-coupled pair and in some publications degeneration resistances are added to improve linearity. However, those two topologies do not provide enough linearity. The highly linear emitter-coupled pair with diode-connected load cannot be utilised, because it provides its output signal only in voltage form. In this work, a compensated cascode is used as the signal amplifier. It is able to securely provide the required third-order distortion $HD_3$ of $-80\,\mathrm{dBc}$ for a gain up to $A_d = 6\,\mathrm{dB}$ for the required output voltage of $600\,\mathrm{mV_{pp}}$, even under consideration of statistical deviations.

| | $HD_3$ [dBc] for $V_{od} = 600\,\mathrm{mV_{pp}}$ | $V_{id}$ [$\mathrm{mV_{pp}}$] for $HD_3 = -80\,\mathrm{dBc}$ | $\frac{V_{id}}{V_{id\,lim}}$ for $HD_3 = -80\,\mathrm{dBc}$ | $A_d$ [dB] max. |
|---|---|---|---|---|
| Gilbert cell with comp. cascode | −81.1 | 323 | 1.07 | 6.00 |
| Simple Gilbert cell | −36.3 | 6.8 | 0.22 | 25.7 |

**Table 2.2:** Simulation of third-order harmonic distortion of the variable-gain topology Gilbert cell. Simulations are made for maximum gain.

#### Result of the selection process

The Gilbert cell in the following configuration is used as the variable-gain amplifier of this work.

- Gilbert cell with a compensated cascode as its signal amplifier
  Maximum differential voltage gain $A_d = 6\,\mathrm{dB}$

# Chapter 3

# Schematic design of the amplifier stages

In this chapter, a description is given of the whole schematic design process for the three amplifiers, which were chosen in the previous chapter to be most adequate for the given problem.
First, the available circuit components provided by a SiGe technology of Infineon are regarded and the properties and possible variants of the heterojunction bipolar transistors and the different provided resistor and capacitor types are listed. In addition, transistor biasing conditions for low-distortion design are discussed.
Then, an emitter follower circuit is designed. It is used as an input buffer for all of the designed amplifier stages, and is in the first instance responsible for decreasing the DC voltage level. By decreasing the DC level by subtracting one base-emitter voltage, it compensates for the inevitable voltage rise caused by the differential pairs of the amplifier stages. This permits direct coupling and simple cascading of successive stages.
The two fixed-gain amplifiers, notably the emitter-coupled pair with diode-connected load and the compensated cascode, are also designed. The compensated cascode is not only used as a fixed-gain amplifier stage, but also as a highly linear signal amplifier for the Gilbert cell four-quadrant multiplier, which is designed last and serves as the variable-gain amplifier.
The results of this design process are the complete schematics for all the three amplifiers. In the next chapter their performance numbers will be accurately simulated to verify their compliance to the given specifications.

## 3.1 Circuit components provided by the Infineon B7HF200 SiGe technology

The B7HF200 SiGe technology of Infineon [28] is a 0.35 µm bipolar process, fabricated on a 200 mm wafer, and intended for analogue and mixed-signal high-speed applications. With this technology full-custom RF circuits like the amplifiers of this work are designable. The technology provides a set of different heterojunction bipolar transistors (HBTs) with arbitrary emitter area sizes, varactor diodes, two types of polysilicon resistors, other resistors made of tantalum nitride or silicided polysilicon, metal-insulator-metal and junction capacitors, fuses and transmission lines. Due to the free scalability of most of the component sizes, a high degree of design freedom is given.

### 3.1.1 Transistors

The HBT transistor models are based on Cadence's Spectre Circuit Simulator's implementation of the Berkeley-Spice Gummel-Poon model [29].

The Infineon technology provides four different basic types of HBT transistors:

- High speed NPN transistors (HS)
- Ultra high speed NPN transistors (UHS)
- High voltage NPN transistors (HV)
- Vertical PNP transistors

#### Transistor size and contact configuration

The emitter area of the NPN transistors can be chosen within a wide range. The selectable emitter mask widths are 0.35 and 0.55 µm, the emitter mask length can be in the range from 1 to 10 µm with a step of 0.3 µm. In addition, different contact configurations are provided. The BEC, BEBC, CBEC, CBEBC, CEBEC and CBEBEBC configurations differ in the number of their emitter, base and collector contact stripes.
Vertical PNP transistors can have the emitter area sizes $2.1 \times 2.9$ or $2.1 \times 11.7$ µm$^2$. They are only provided in BEC configuration.

The choice of transistor size and the number of contact stripes is always a trade-off between bandwidth on the one side and transconductance $g_m$ as well as noise performance on the other one. The bigger the transistor, the bigger the capacitive parasitics, which lets decrease the bandwidth. On the other hand the supportable current is higher, which means higher transconductance. By increasing the transistor size, the base resistance is also reduced and with it the noise of the transistor.

#### Breakdown voltages

Breakdown can occur at the different junctions of a bipolar transistor if excessive voltages are applied [6, 4]. The collector-base junction is the most critical one. In practice, not the collector-base, but the collector-emitter voltage limit is given in data sheets. It is characterised by the two values $BV_{CE0}$ and $BV_{CES}$. $BV_{CE0}$ is the more critical value, and has to be applied if the emitter current is equal to zero, which means an open emitter. $BV_{CES}$ is higher than the former value and represents the collector-emitter breakdown voltage with the base short-circuited with the emitter. The actual breakdown voltage $BV_{CE}$ lies between these two values.

$$BV_{CE0} \leq BV_{CE} \leq BV_{CES} \tag{3.1}$$

In the case of NPN transistors, there also have to be considered the base-substrate and the collector-substrate junction. However, these $BV_{BS}$ and $BV_{CS}$ values are clearly higher than the $BV_{CE0}$ and $BV_{CES}$ values, as the following table shows.

| | $BV_{CE0}$ [V] $I_C = 1$ µA | | $BV_{CES}$ [V] $I_C = 1$ µA | | $BV_{CS0}$ [V] $I_C = 1$ µA | | $BV_{BS0}$ [V] $I_B = 1$ µA | |
|---|---|---|---|---|---|---|---|---|
| | min. | typ. | min. | typ. | min. | typ. | min. | typ. |
| HS | 1.4 | 1.7 | 5.8 | 6.5 | 10 | 58 | 10 | 35 |
| UHS | 1.2 | 1.5 | 4.8 | 5.8 | 10 | 40 | 10 | 40 |
| HV | 3.3 | 4.0 | 11.5 | 14.5 | 10 | 35 | 10 | 35 |

**Table 3.1:** Breakdown voltages of the different NPN transistor versions. The technology data sheet gives these breakdown voltages for transistors with $0.35 \times 2.8$ µm$^2$ emitter area and BEC configuration.

The PNP transistors are embedded in an N-well and not like their NPN counterpart directly into the substrate. Thus, the junction notation for this transistor type differs from the one of the NPN type.

| | $BV_{CE0}$ [V] $I_C = 1\,\mu A$ | | | $BV_{CES}$ [V] $I_C = 1\,\mu A$ | | | $BV_{NC0}$ [V] $I_N = 1\,\mu A$ | | |
|---|---|---|---|---|---|---|---|---|---|
| | min. | typ. | max. | min. | typ. | max. | min. | typ. | max. |
| PNP | | -10 | -6.5 | | -16 | -10 | 6.5 | 16 | |

| | $BV_{EB0}$ [V] $I_E = 1\,\mu A$ | | | $BV_{NB0}$ [V] $I_N = 1\,\mu A$ | | | $BV_{SN0}$ [V] $I_S = 1\,\mu A$ | | |
|---|---|---|---|---|---|---|---|---|---|
| | min. | typ. | max. | min. | typ. | max. | min. | typ. | max. |
| PNP | | -5 | -3 | 5 | | | | -50 | -10 |

**Table 3.2:** Breakdown voltages of the PNP transistor version. The technology data sheet gives these breakdown voltages for an emitter area of $2.1 \times 2.9\ \mu m^2$.

### Dynamic behaviour

The two characteristic values transition frequency $f_T$ and maximum oscillation frequency $f_{max}$ are commonly used to describe the dynamic properties of bipolar transistors.
The transition frequency $f_T$ is defined as the frequency, at which the current gain of a transistor with short-circuited output is equal to unity. $f_T$ increases with increasing collector current density and shows a maximum at the density $j_C$. Above this density value, which is given in the technology's data sheet, $f_T$ strongly falls off. This is due to the decrease of the current gain $\beta$ caused by high-injection [6] and the increase of transit time $\tau_T$ caused by the Kirk effect [6, 30]. To avoid a strong performance degradation of the transistor, current densities higher than $j_C$ are avoided during the whole schematic design process by choosing adequate numbers of contact stripes and emitter area sizes. The second dynamic performance measure is the frequency $f_{max}$. This value is defined as the frequency at which the power gain of the transistor is equal to 0 dB. It also marks the maximum oscillation frequency of the component.

| | max. $f_T$ [GHz] | @ $j_c$ [mA µm$^{-2}$] | max. $f_{max}$ [GHz] |
|---|---|---|---|
| HS | 170 | 5 | 250 |
| UHS | 200 | 6.5 | 250 |
| HV | 35 | 0.5 | 120 |
| PNP | 3.5 | | |

**Table 3.3:** Transition frequencies $f_T$ and maximum oscillation frequencies $f_{max}$ for the different types of transistors.

### Used transistor type

Because of its insufficiently low transition frequency of 3.5 GHz, the PNP transistor type is clearly not fast enough to be used in this work. This leads to certain limitations in circuit design. For instance, it is not possible to use active loads for the differential amplifiers. Differential pairs based on PNP transistors would decrease the DC level and could substitute the emitter followers, which are responsible for this function in this work, but they cannot be realised either. Amplifiers based on the high voltage version HV are also too slow for the given specifications, so only the high speed and ultra high speed types can provide the needed bandwidth. The UHS transistor has lower breakdown voltages than the HS transistor, but only slight speed advantages compared to its already sufficiently fast HS counterpart. Therefore it can be concluded, that the high speed transistor type is the only type which can be used for the amplifiers of this work.
Operation without junction breakdown would be guaranteed by always keeping the $V_{ce}$ voltage lower than the $V_{CE0}$ limit. However, this would mean stringent design limitations. Most notably, high linearity could not be achieved. Practical experience has shown that with an emitter current higher than zero, $V_{ce}$

voltages up to 2 V can be applied to the transistors without danger. The only transistors of this work, which can be without emitter current, are the gain regulation transistors of the variable-gain amplifier. For these transistors, the minimal $V_{ce}$ of 1.4 V is not exceeded.
The the $V_{ce}$-$I_c$ transistor output characteristics for all designed circuits are plotted in Annex A and show, that the rules avoiding junction breakdown are respected for all amplifier designs.

### 3.1.2 Resistors

The B7HF200 SiGe technology provides three different types of resistors, which differ in their sheet resistance value and tolerance. They also have different temperature coefficients, a property which however was not considered for the amplifiers of this work. For the design it can be from the following resistor types:

- Polysilicon [31]
  This type of resistor is made of thin films based on doped polycrystalline silicon. With this material high value transistors can be produced. A lightly doped $P^-$-version and a stronger doped $P^+$-version are available. They have high and medium sheet resistance, respectively.
- Tantalum nitride [6]
  TaN resistors have lower sheet resistance than polysilicon resistors as well as better manufacturing tolerances.
- Silicided polysilicon [28]
  This material is for instance used in the base of the NPN transistors and provides an additional low resistance, low tolerance type of resistor to the circuit designer.

| | Sheet resistance [$\Omega/\square$] | Tolerance [%] | Max. current density [mA µm$^{-1}$] |
|---|---|---|---|
| Sil | 3 | +100/−50% | 0.65 |
| TaN | 20 | ±10% | 0.80 |
| $P^+$-Poly | 150 | ±20% | 0.65 |
| $P^-$-Poly | 1000 | ±20% | 0.20 |

**Table 3.4:** Summary of the different resistor types provided by the Infineon B7HF200 SiGe technology with their typical sheet resistance values, manufacturing tolerances and maximally permitted current densities.

In the design of differential circuits, matching of components is always desired. Therefore, for the design of the amplifiers of this work the TaN resistor is always the preferred type of resistor. If high resistor values contradict its use, polysilicon devices with lower manufacturing tolerance have to be used to avoid excessive resistor lengths. Silicide resistors are not very accurate and are only used for very small resistor values.

### 3.1.3 Capacitors

It is possible to choose between fixed-value and variable-value capacitors.

- Metal-insulator-metal (MIM) capacitor
  This device consists of the second and third metal layer of the process, which form the electrodes of the capacitor, as well as the isolating dielectric material between these metal layers. The obtained capacitance is equal to 1.4 fF µm$^{-2}$ and has a tolerance of ±10%.
- Junction capacitor
  For variable capacitance values a junction capacitor is provided. It can be freely scaled in its size. Depending on the junction voltage, different capacitances can be obtained. For a $10 \times 30$ µm$^2$ device, a variation of the junction voltage from 0 to −5 V yields capacitance values from 605 to 227 fF.

As no variation of capacitance is needed for the amplifiers, only MIM capacitors are used in this work.

## 3.2 Transistor biasing for low non-linear distortion

The main source of non-linearity of bipolar transistors is their exponential relation between the input voltage $V_{be}$ and the output current $I_c$. As described in Section 2.2.1, the DC transfer characteristics of a differential pair based on these transistors is a tanh-function. In the following sections of Chapter 2 amplifier topologies are presented, which reduce or even avoid this effect and have more linear transfer characteristics.
Apart from this non-linearity, a transistor has several other non-linear elements, which for instance lead to a degradation of the theoretically perfect distortion-compensation of the emitter-coupled pair with diode-connected load. Some of these non-linearities are dependent on the transistor's bias conditions. Hence, appropriate biasing is indispensable for a low-distortion design.

A basic rule is that a high collector-emitter voltage $V_{CE}$ improves the linearity of transistors. Increasing collector current $I_C$ also results in higher linearity. However, beyond a linearity maximum further current increase leads to performance degradation.

#### Collector-emitter voltage

The need for high $V_{CE}$ can be explained by its influence on the parasitic collector-base capacitance $C_\mu$ [32, 33, 34]. If $V_{CE}$ is high, a large reverse bias is applied to the collector-base junction and the collector is more fully depleted. Because of this, $C_\mu$ is less dependent on the $V_{CB}$ voltage, which results in a linearity improvement.
At high biasing current levels, the Kirk effect [30] leads to a decrease in gain and a strong increase of nonlinear distortions. Another positive effect of high $V_{CE}$ is that it increases the current limit for the onset of the Kirk effect.
The performance improvements due to high $V_{CE}$ are limited by the collector-base breakdown voltage and the supply voltage.

#### Collector current

Another nonlinear parasitic capacitance is the base-emitter capacitance $C_\pi$ [32, 33, 34]. Higher biasing current decreases the non-linearity due to this capacitance, which yields substantial performance improvements. However, at high currents the influence of $C_\mu$ increases, which counteracts the $C_\pi$-effect and increases distortion. In addition, an excessive current level may lead to the onset of the Kirk effect.

## 3.3 Emitter follower

All three amplifier topologies of this work have in common that without additional circuitry the amplifiers' output DC level is higher than the input level. The increased output voltage of the amplifier stages is due to the fact that low distortion design implies high collector-emitter biasing voltages of the amplifier transistors. This contradicts direct coupling of successive stages, decoupling and biasing are necessary. To avoid the need for large decoupling capacitances after each amplifier stage, emitter followers are used as input buffers for each of the designed amplifiers.
In practice, the $V_{CE}$ of the amplifier transistors has to be significantly higher than $V_{BE}$ to be able to obtain sufficiently low distortion. The use of one emitter follower causes an additional voltage drop of one $V_{BE}$, permitting a $V_{CE}$ of two times the $V_{BE}$ voltage, i.e. 1.7 V. The use of multiple emitter followers would allow even higher $V_{CE}$ and less distortion, but is not possible because of stability problems.

### Choice of the used transistors depending on their noise performance

In accordance with Friis's formula for noise figures [35], the first amplifier stage contributes the most to the overall noise figure. In the case of both the fixed and variable gain amplifiers of this work, the gain stages are preceded by emitter followers, which have to show good noise performance in order to keep overall noise of the amplifier low. One major noise source of the emitter follower transistors is the thermal noise of their base resistance. Keeping the base resistance low is a basic low-noise design technique. It reduces thermal noise, consequently it improves the noise performance. To obtain this desired low base resistance the emitter area, and thereby the base area of the transistor, are chosen as high as possible. Furthermore a high number of base stripes also reduces the base resistance. To be able to choose the most adequate transistor configuration, a noise analysis of the emitter-follower circuit depicted in Figure 2.17 is carried out.

| Configuration | Noise figure [dB] at $Z_{in} = 50\,\Omega$ | Noise contribution | |
|---|---|---|---|
| CBEBEBC | 3.11 | $I_{C\ shot}$ | 56.2% |
| | | $R_{B\ therm}$ | 42.8% |
| CEBEC | 3.28 | $I_{C\ shot}$ | 52.4% |
| | | $R_{B\ therm}$ | 46.8% |
| CBEBC | 4.03 | $I_{C\ shot}$ | 40.7% |
| | | $R_{B\ therm}$ | 58.1% |
| CBEB | 4.03 | $I_{C\ shot}$ | 40.7% |
| | | $R_{B\ therm}$ | 58.1% |
| CBEC | 4.29 | $I_{C\ shot}$ | 37.0% |
| | | $R_{B\ therm}$ | 62.0% |
| CBE | 4.29 | $I_{C\ shot}$ | 37.0% |
| | | $R_{B\ therm}$ | 62.0% |

**Table 3.5:** Simulation of the noise properties of two emitter follower transistors, operated differentially. The emitter area of the transistors is chosen as $10 \times 0.55\ \mu m^2$, which is the maximum possible area for the technology used. The biasing current of each of the two transistors is equal to 1 mA. Noise figures for different transistor configurations are simulated and the percentages of the main noise contributors collector shot-noise and base resistance thermal noise are listed.

The main noise contributors for the given operating frequency of 1.6 GHz and a transistor biasing current in the order of magnitude of milliamperes are the thermal noise of the base resistance and the shot-noise of the collector current, as shown in Table 3.5. The thermal noise is due to statistical movements of the electrons dependent on the temperature of the resistor and is directly proportional to the resistance. The shot-noise represents statistical fluctuation of the number of discrete charge carries passing the base-collector junction. The absolute contribution of the shot-noise to the overall noise stays approximately the same for the different transistor configurations. By contrast, the thermal noise is strongly dependent on the number of base strips. Its relative influence rises with higher base resistance, i.e. with less base strips.

The noise simulation shows, that the best noise performance can be obtained by the most complex transistor configuration. The CBEBEBC configuration has three base stripes, resulting in low base resistance and a noise figure of 3.11 dB. However, this advantage comes with high parasitic capacitances. Although these parasitics limit the bandwidth of the emitter-follower, it still stays in the range of tens of GHz. All the other simulated transistors have less base strips and higher noise figures. For instance, the noise figure of the BCE configuration, which is the most simple configuration, is equal to 4.29 dB. As the result of these considerations, CBEBEBC transistors with an emitter area of $10 \times 0.55\ \mu m^2$ are chosen for the emitter followers.

### Relation between noise and biasing current

The noise figure of the emitter follower topology decreases with increasing biasing current, as the following simulation result shows.

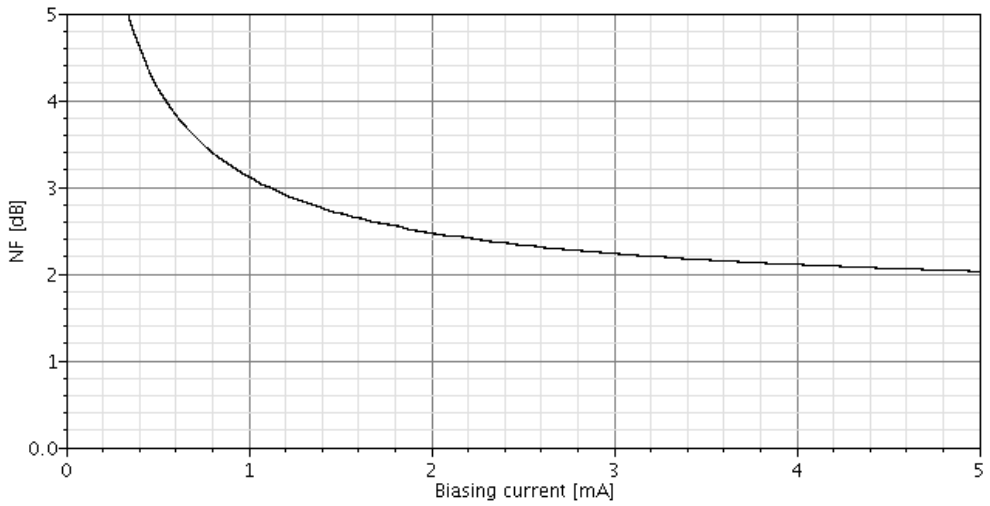


**Figure 3.1:** Simulation of the noise figure of a differential emitter follower for varying biasing current. The used transistors have CBEBEBC configuration and an emitter area of $10 \times 0.55\ \mu m^2$.

Shot noise, one of the main noise contributors, is directly proportional to the biasing current. The other main noise source, thermal noise, is independent of current. However, the noise figure presented in Figure 3.1 is not directly proportional to the biasing current. By contrary, it sinks with increasing current. This effect can be explained by using equivalent noise sources [4].
The thermal noise caused by the base resistance, as well as the shot- and flicker-noise of the base and collector current, can be described by two equivalent noise sources. These are a voltage and a current noise source connected to the base of the noiseless transistor model. For biasing currents up to some milliamperes the current noise source can be neglected. Only the voltage noise source has to be taken into account. For medium frequencies [1], and for the given base resistance $R_B$ of $9.05\,\Omega$ of the before defined emitter follower transistors, the asymptotes for the spectral density of the voltage noise source are

$$v_n^2(f) = \begin{cases} 2kTV_T \cdot \frac{1}{I_C} & \text{for} \quad I_C < \frac{V_T}{2R_B} = 1.44\,\text{mA} \\ 4kTR_B & \text{for} \quad 1.44\,\text{mA} = \frac{V_T}{2R_B} < I_C < \frac{2\beta V_T}{R_B} \approx 0.5\,\text{A} \\ \frac{2qR_B^2}{\beta} \cdot I_C & \text{for} \quad I_C > \frac{2\beta V_T}{R_B} \approx 0.5\,\text{A} \end{cases} \tag{3.2}$$

For biasing currents smaller than 1.44 mA, the noise voltage sinks with increasing current. For biasing currents higher than this limit, the noise voltage rests constant up to high currents. This behaviour is in

[1] Here medium frequencies are defined as being in a frequency range between the flicker-noise knee frequency (some MHz maximum) and $\frac{f_T}{\sqrt{\beta}}$ (tens of GHz). The operating frequency of 1.6 GHz of the amplifiers of this work lies within this frequency range.

accordance with the simulation result of Figure 3.1. The higher the biasing current, the better the noise performance of the emitter follower.

### Third-order harmonic distortion

According to Formulas 2.81 and 2.82, the third-order harmonic distortion $HD_3$ of emitter-followers decreases with increasing biasing current and increasing load resistance. The following figure shows a simulation of the harmonic distortion dependent on these two factors. The main difference to the theoretical analysis presented in Figure 2.16 is the limit of obtainable linearity at about $-130\,\mathrm{dBc}$. In practice, values significantly lower than this limit are hardly achievable due to additional sources of non-linearity, which have not been considered in the theoretical approach leading to the above mentioned formulae.

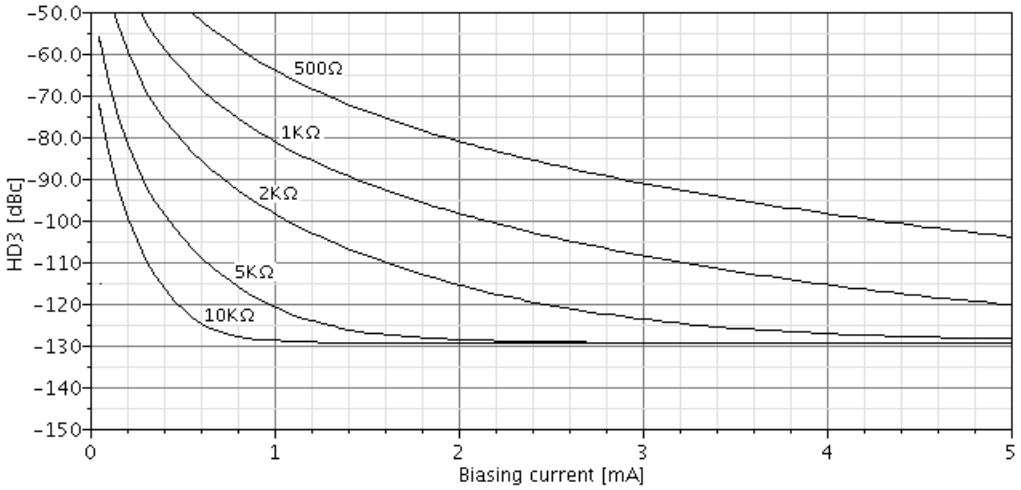


**Figure 3.2:** Simulation of the third-order harmonic distortion $HD_3$ of a differential emitter follower for varying biasing current and load resistances. The two load resistances are each connected to one of the transistor emitters and ground. The input voltage is equal to $300\,\mathrm{mV_{pp}}$.

Between the base of the principal transistors of the amplifiers and ground, the lowest expectable single-ended input impedance is about $2\,\mathrm{k\Omega}$. Referring to the non-linearity simulation, a biasing current of at least half a milliampere is necessary to obtain a $HD_3$ of $-80\,\mathrm{dBc}$. A current of $1\,\mathrm{mA}$ or higher guarantees negligible distortion.

### Stability

Emitter followers can easily become unstable if they are charged by certain source and load impedances. Inductive source impedances are transformed to inductive-resistive emitter follower output impedances with negative real part. Capacitive load impedances result in capacitive-resistive emitter follower input impedances, also with negative real part [4]. Negative resistances imply stability issues, so care has to be taken if the emitter follower input is inductively charged or the output is capacitively charged. Within this work, the emitter follower output is connected to the transistors of the gain stage, which show capacitive behaviour. In this case, the source impedance, by which the input is charged, must avoid certain values in order to guarantee stability. The zone with permitted source reflection coefficients can be determined by displaying source stability circles on a Smith chart [35].

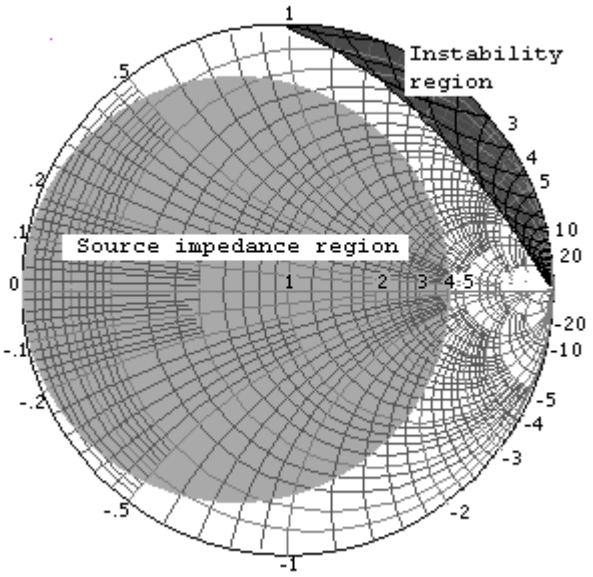


**Figure 3.3:** Simulation of the region of possible source impedances and the region of possible instability. The instability region is obtained by source stability circles for the whole frequency range up to $f_T$. The emitter follower transistors of this simulation are both biased with a current of 1 mA

.

The source impedance is equal to 200 Ω differential output resistance of the preceding amplifier stage in parallel with the impedance of a noise shaping filter. The filters reduce the real part of the source impedance due to the parallel circuit connection. They can also add all kinds of imaginary values dependent on the sort of filter and the frequency, so the filter impedance can reach from strongly inductive to strongly capacitive behaviour. The region of the possible source impedance values is shown as a light-grey area on the Smith chart.
A source stability circle marks a region of source impedances, which cause instability at a certain frequency. The dark-grey region is built of the sum of all source stability circles for a frequency range from DC up to transit frequency $f_T$. All source impedances situated in this region can result in instability and have to be avoided.
In Figure 3.3, the two regions are clearly separated from each other. For all possible frequencies, the source impedance does not lie in the region of instability. However, it has to be considered that the region of instability is dependent on the biasing current. This simulation is made with a current of 1 mA. With increasing biasing current, the region of instability expands. For a current of about 2 mA it already gets in touch with the source impedance region and stability cannot be guaranteed any more. Thus, the biasing current must be kept low to avoid stability issues.

### Current sources

A current of 1 mA is chosen for biasing the transistors. With this value the following properties are obtained:

- With 3.11 dB at 50 Ω source impedance, the noise figure is acceptably low
- With a $HD_3$ value of about −100 dBc, the linearity is high enough to neglect performance degradation due to the use of emitter follower stages
- The circuit is unconditionally stable for all output impedances, if the input is charged by a preceding stage in parallel with a bandpass filter

The two necessary current sources are realised with a simple current mirror. The transistors $Q_3$ to $Q_5$ of the current mirror only have BCE configuration. The noisy biasing current does not strongly influence the noise level at the emitter follower output, because the $V_{BE}$ voltage of the emitter follower transistors $Q_1$ and $Q_2$ only depends logarithmically on the biasing current. Thus, noise created by the current mirror is not a critical factor and taking CBEBEBC transistors would improve the noise figure only by some hundredths of dB. The current mirror includes emitter degeneration resistors, which lead to a high output resistance as well as better current matching between the two current sources [6]. The degeneration resistors are chosen low enough to have sufficiently high $V_{CE}$ voltage at the current mirror transistors to guarantee their functionality.

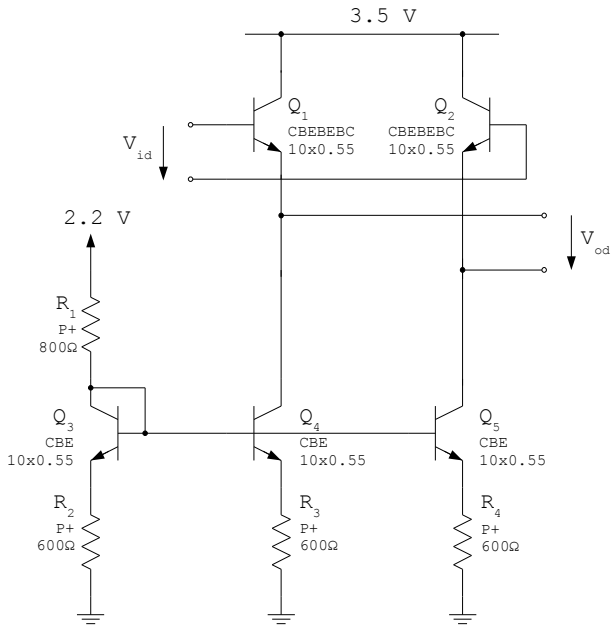


**Figure 3.4:** Schematic design of the emitter follower

## 3.4 Fixed-gain amplifiers

In this section the emitter-coupled pair and the compensated cascode are designed. The first amplifier has a voltage gain of 6 dB. The second one is designed for a gain of 6 and of 9 dB. All circuits have the emitter follower of the previous section connected to their input.

### 3.4.1 Emitter-coupled pair with diode-connected load

#### Emitter degeneration topology

For the realisation of the differential pair, a topology with one emitter degeneration resistor and two current sources is used. This variant with a degeneration resistor of $2R_E$ and two $I_E$ current sources is equivalent to the circuit proposed in Section 2.2.3, which has two degeneration resistances of $R_E$ and a single tail current source $2I_E$. This principle of equivalence, which is in more detail described in Section 2.4, can be used to avoid a voltage drop-off at the emitter degeneration resistors, caused by the biasing current. Saving unnecessary voltage drop-off at these resistors gives more headroom for the transistors. Therefore, higher $V_{CE}$ can be obtained, which leads to higher linearity. A disadvantage of two current sources is their uncorrelated noise, which causes different noise voltages at the two collector resistances. This noise cannot be suppressed by the common-mode rejection of the successive amplifier stage, which increases the overall noise level of the circuit. But as the main design focus lies on linearity, higher noise is accepted.

#### Input and output DC level

The DC input and output voltages of the fixed-gain stages are fixed at 2.4 V. At the output of the emitter follower $Q_{10}$-$Q_{11}$ respectively the input of the differential pair $Q_1$-$Q_2$, the DC level is equal to approximately 1.6 V. Subtracting the $V_{BE}$ of the principal transistors $Q_1$ and $Q_2$ results in a DC level of 0.75 V at the collectors of the current mirror. Considering the emitter degeneration resistors of the current mirror, the $V_{CE}$ voltage of the current mirror transistors $Q_8$ and $Q_9$ is equal to 0.55 V. In the case of the maximum differential input voltage of 0.3 V, the lowest current mirror $V_{CE}$ voltage is obtained. This collector-emitter voltage of 0.4 V is still high enough to have a correctly working current mirror and to bias the transistor in a region, where its mathematical model can be assumed to be highly accurate. Biasing points with $V_{CE}$ voltages lower than 0.4 V are close to the saturation region, and for these low voltages accurate transistor modelling cannot be presumed. If the DC input would be lower than 2.4 V, the current mirrors could not work properly. If if would be higher, it would decrease linearity due to decreasing $V_{CE}$ voltage of the principal transistors $Q_1$ and $Q_2$.

#### Resistor values and biasing current

The two linearisation diodes require a high supply voltage for the circuit. With a 5 V supply, and subtracting the current-dependent base-emitter voltages of the two diodes, a voltage of about 0.9 V is needed across each of the collector resistances to obtain a DC level of 2.4 V at the output. Collector resistors of 93.5 Ω in series with the diodes can iteratively be found to lead to the needed differential output resistance of 200 Ω of the amplifier, if a biasing current of 10.25 mA is applied to each of the emitter-leads of the two principal transistors of the circuit. According to Formula 2.46, the emitter degeneration resistor must have the same value of 93.5 Ω as the collector resistors, to obtain optimal distortion compensation.
The theoretical derivation of the non-linearity compensation mechanism predicts a perfectly linear circuit (Section 2.2.3). In practice, this infinitely low level of distortion cannot be reached, because the linearity of the circuit is also influenced by other factors (Section 3.2), which are not taken into account in the theoretical analysis. With the above defined value of 10.25 mA, the biasing current is high enough to obtain sufficiently linear operation of the transistors.

### Current mirror

The current mirror for the differential pair consists of transistors with CBEBEBC configuration and an emitter area of $10 \times 0.55$ µm$^2$, because the noise of the current sources has to be kept low. Degeneration resistors are added to the emitter leads of the transistors, because by their use several positive effects can be obtained. Firstly, even if these degeneration resistors act as additional thermal noise sources, they reduce the overall noise generation of the current mirror, because they reduce the influence of the transistor's noise. Secondly, the degeneration resistors increase the output resistance of the current mirror. Thus, they also positively influence the common-mode rejection of the amplifier. Finally, they reduce the mismatch between the two current sources built by the current mirror. However, due to limited supply voltage, the resistors need to be small to avoid large voltage drop-offs across them.

### Stability

The designed differential pair is only conditionally stable, depending on its source impedance it is able to oscillate. As the source of the differential pair is always the emitter follower, which has a clearly defined output impedance, one can determine the stability of the differential pair. Stability issues only exist for a certain inductive source impedance region. The emitter follower has a capacitive output impedance, therefore the combination of the two circuits is stable.

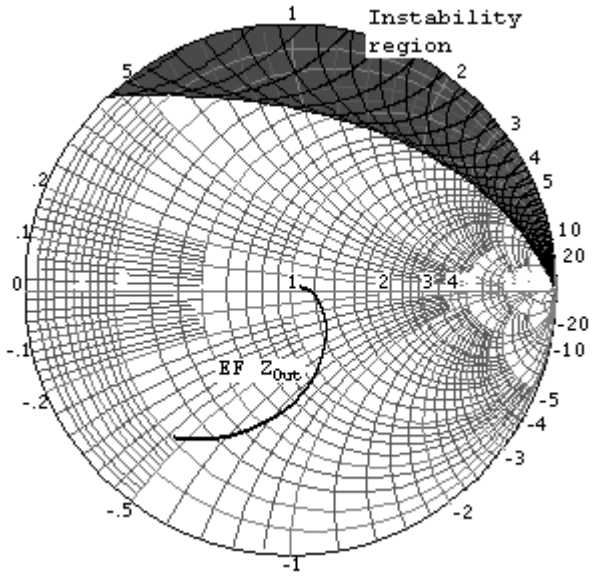


**Figure 3.5:** Instability region of the differential pair and output impedance of the preceding emitter follower from low frequencies up to $f_T$. No stability problems occur.

To make the differential pair unconditionally stable, small resistors could be added to the base leads of the transistors. However, this limits bandwidth and in particular increases the noise figure. For this circuit, these resistors are not necessary. Even if the circuit is only conditionally stable, it poses no stability problems.

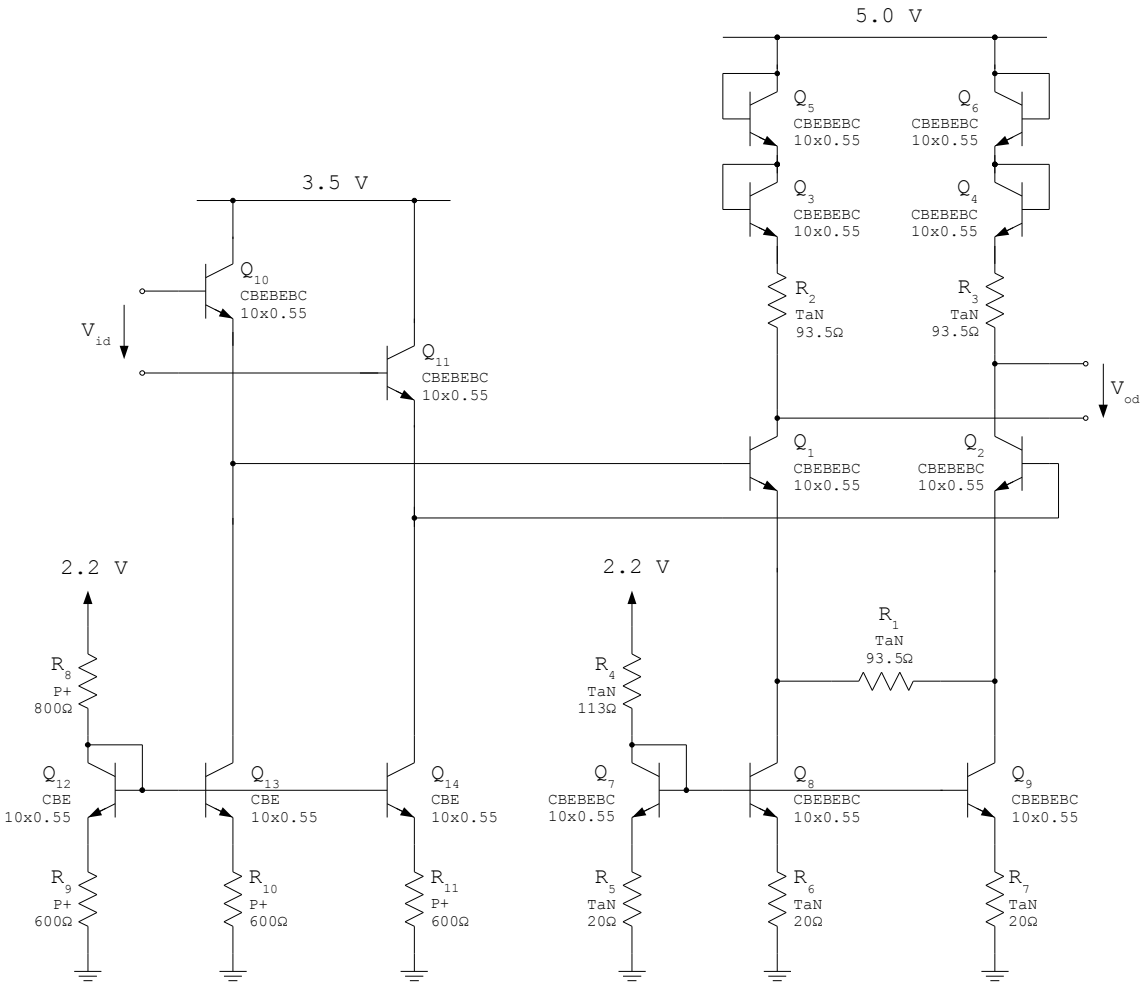


**Figure 3.6:** Schematic design of the differential pair with diode-connected load

### 3.4.2 Compensated cascode

The compensated cascode has several advantages over the emitter-coupled pair with diode-connected load. Its voltage gain is freely selectable during the design phase, which allows to have higher gain than the restricting 6 dB of the emitter-coupled pair. In view of the complete amplifier chain, three emitter-coupled pairs can be substituted by two compensated cascodes with 9 dB gain each, which decreases the total power consumption of the chain. The disadvantages of the compensated cascode are a more complex circuitry and the resulting increased noise figure.

#### Transistor configuration

If transistor contact configurations with low-noise properties like the CBEBEBC or the CEBEC configuration are used, the circuit is too slow and its bandwidth is significantly below 10 GHz. So the fast BEC transistors are chosen, which increase the already high noise figure even more.

#### Collector resistors

According to the specifications, the amplifiers need to have 200 Ω differential output impedance. The two collector resistors $R_4$ and $R_5$ have values of 100 Ω to fulfil this requirement. As the collector resistors and the output DC level of 2.4 V are predetermined, the collector currents are also given as fixed values and cannot be used as a variable to optimise the linearity of the cascode.

#### Supply voltage

Concerning the supply voltage, a choice has to be taken between the 5.0 and the 3.5 V supply. By looking at the power consumption, the lower supply voltage turns out to be the only practicable choice.

| $V_{CC}$ | $I_C$ | $P_{Diss}$ |
|---|---|---|
| 3.5 V | 11 mA | 102 mW |
| 5.0 V | 26 mA | 307 mW |

**Table 3.6:** Estimation of the power consumption $P_{Diss}$, dependent on the supply voltage $V_{CC}$ of the compensated cascode and the current $I_C$ through each of its collector resistors. The dissipated power is composed of the power necessary for the current mirrors, the emitter follower and the compensated cascode.

A power consumption of 307 mW is clearly too high for a single amplifier stage, so the 3.5 V supply is used for the compensated cascode. However, this is accompanied by a loss of linearity compared to the analysis depicted in Table 2.1, which has been made for a supply voltage of 5 V. With the higher supply voltage third-order distortions of −84.5 and −86.4 dBc have been listed for the two different compensated cascode versions. With the actual supply voltage $HD_3$ is significantly lower.

#### Cascode biasing voltage

The bias voltage for the cascode transistors $Q_3$ and $Q_4$ has to be high enough to guarantee sufficient $V_{CE}$ for the current mirror transistor $Q_{10}$, which is the most critical current mirror transistor from this point of view. The 2.2 V supply voltage leads to a $V_{CE}$ of 0.4 V for this transistor and is therefore the lowest possible biasing voltage. The lower the bias voltage, the higher the linearity of transistors $Q_5$ and $Q_6$ because of their higher $V_{CE}$. 2.2 V is therefore the optimal choice concerning linearity, and it is easily realisable, because it exists as a supply voltage and no voltage divider is needed to provide it.

### Emitter degeneration topology

The topology for each of the two differential pairs $Q_1$-$Q_2$ and $Q_5$-$Q_6$ must be chosen from the two possible degeneration topologies, which are described in Section 2.4.
The compensation amplifier is realised with one current source $Q_{10}$ and two emitter degeneration resistors $R_2$ and $R_3$. The resistors are both equal to $R_A$. This differential pair topology is chosen because of its good noise performance and because of the low voltage drop-off across the small degeneration resistors, which does not influence the functionality of the current source.
By contrary, $R_E$ is much larger than $R_A$. Using the topology, where a biasing current is flowing through the two resistors, is not possible in this case. So the topology with one resistor $R_1$ equal to $2R_E$ and two current sources is taken. This allows the current source transistors $Q_8$ and $Q_9$ to work correctly.

### Emitter degeneration resistances

Two versions of the compensated cascode amplifier are regarded, which differ in their voltage gain. A 6 and a 9 dB version are designed by varying the emitter degeneration resistors $R_1$ to $R_3$. The degeneration resistance $R_E$ of the principal transistor pair $Q_1$-$Q_2$ of the cascode primarily define the gain of the amplifier. The second design variable is the degeneration resistance $R_A$ of the compensation amplifier $Q_5$-$Q_6$. Both $R_E$ and $R_A$ have to be optimised to achieve a minimum of third-order distortion for the wanted voltage gain. This process is depicted in Figures 3.7 to 3.10. The insights resulting from this optimisation are:

- For a gain of 9 dB the linearity of the circuit is not high enough to fulfil the specifications. With a minimum of $-79.6$ dBc, the third-order distortion clearly lies above the $-80$ dBc limit, so this variant cannot be realised. However, the higher gain would have been the most important advantage of the compensated cascode over the emitter-coupled pair with charge diodes.
- The version with 6 dB gain has a smallest possible $HD_3$ of $-80.4$ dBc. This value is obtained for a $R_E$ of 65 Ω and a $R_A$ of 1.1 Ω.

### Stability

Simulations have shown, that with ideal current sources the circuit has a Rollet's stability factor greater than one, which indicates unconditional stability [35]. With current sources realised by real transistors, which have capacitive parasitics, the circuit can become unstable. By contrary to the emitter-coupled pair with emitter degeneration, the output impedance of the preceding emitter follower does not lie within the zone of stability of the compensated cascode. To avoid stability problems, the additional series resistors $R_{15}$ and $R_{16}$ are connected to the input of the compensated cascode. This makes the circuit unconditionally stable, but also degrades the noise performance.

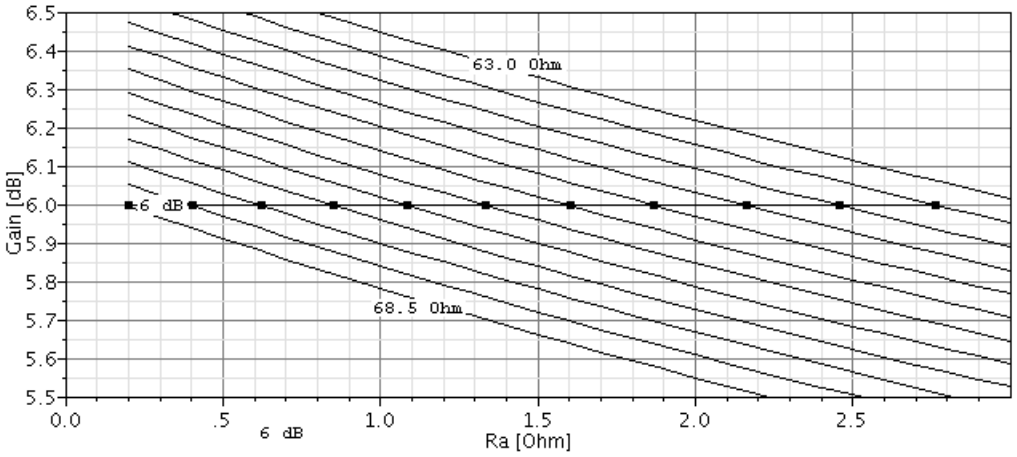


**Figure 3.7:** Voltage gain of the whole amplifier vs. resistance $R_A$ of the compensation amplifier $Q_5$-$Q_6$ for different resistances $R_E$ of the principal transistors $Q_1$-$Q_2$. The resistance combinations with a gain of 6 dB are marked with squares.

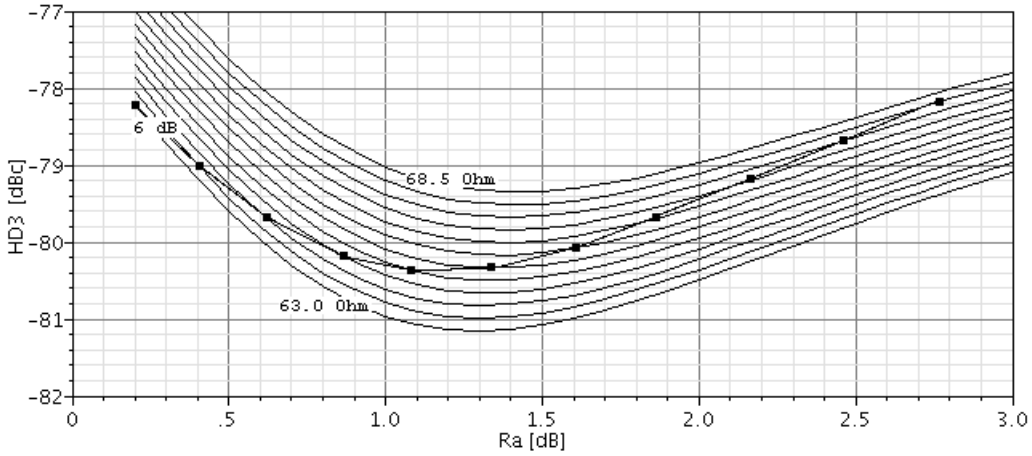


**Figure 3.8:** Third-order harmonic distortion of the whole amplifier vs. resistance $R_A$ of the compensation amplifier $Q_5$-$Q_6$ for different resistances $R_E$ of the principal differential pair $Q_1$-$Q_2$. The resistance combinations with a gain of 6 dB are marked with squares. This allows to find the minimum distortion for the given voltage gain. The lowest distortion is equal to $-80.4$ dBc and obtained for $R_A = 1.1\,\Omega$ and $R_E = 65\,\Omega$.

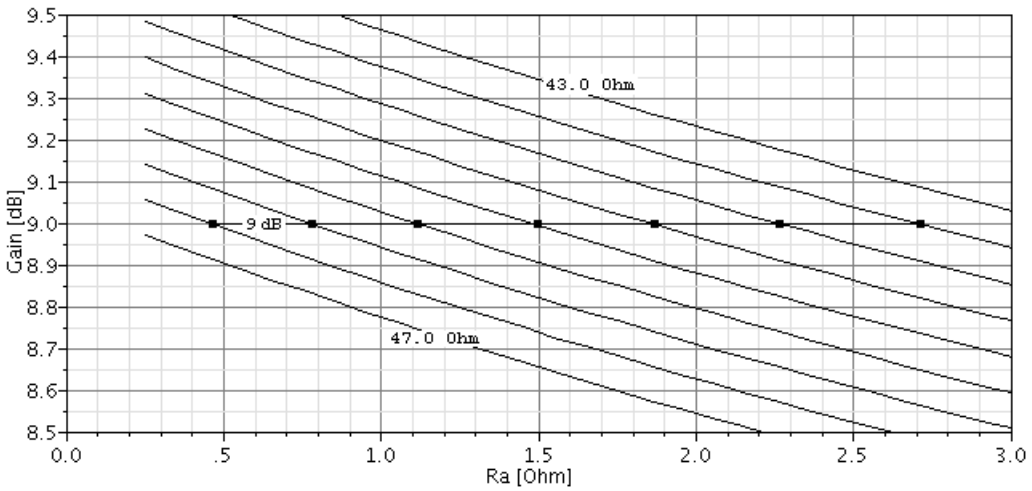


**Figure 3.9:** Voltage gain of the whole amplifier vs. resistance $R_A$ of the compensation amplifier $Q_5$-$Q_6$ for different resistances $R_E$ of the principal transistors $Q_1$-$Q_2$. The resistance combinations with a gain of 9 dB are marked with squares.

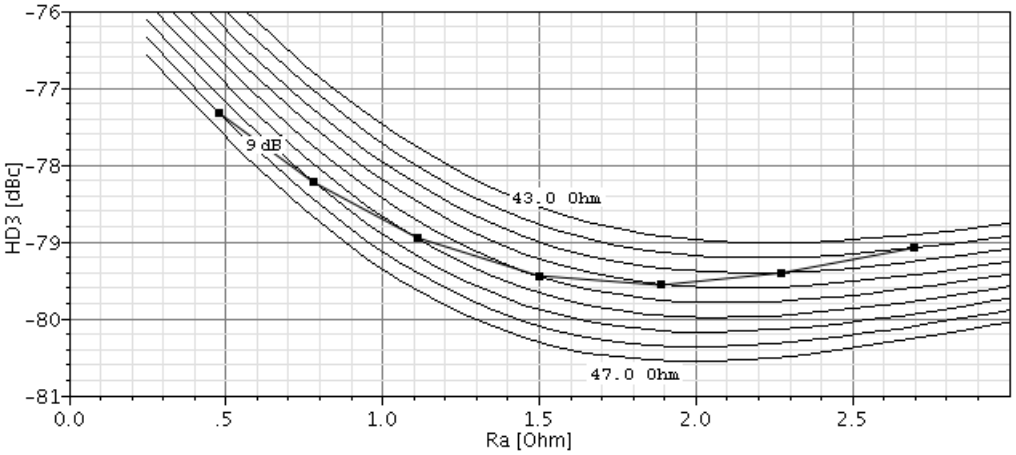


**Figure 3.10:** Third-order harmonic distortion of the whole amplifier vs. resistance $R_A$ of the compensation amplifier $Q_5$-$Q_6$ for different resistances $R_E$ of the principal differential pair $Q_1$-$Q_2$. The resistance combinations with a gain of 9 dB are marked with squares. This allows to find the minimum distortion for the given voltage gain. The lowest distortion is equal to $-79.6$ dBc and obtained for $R_A = 1.9\,\Omega$ and $R_E = 44.5\,\Omega$. This is not sufficiently low to fulfil the requirement of a $HD_3$ inferior to $-80$ dBc.

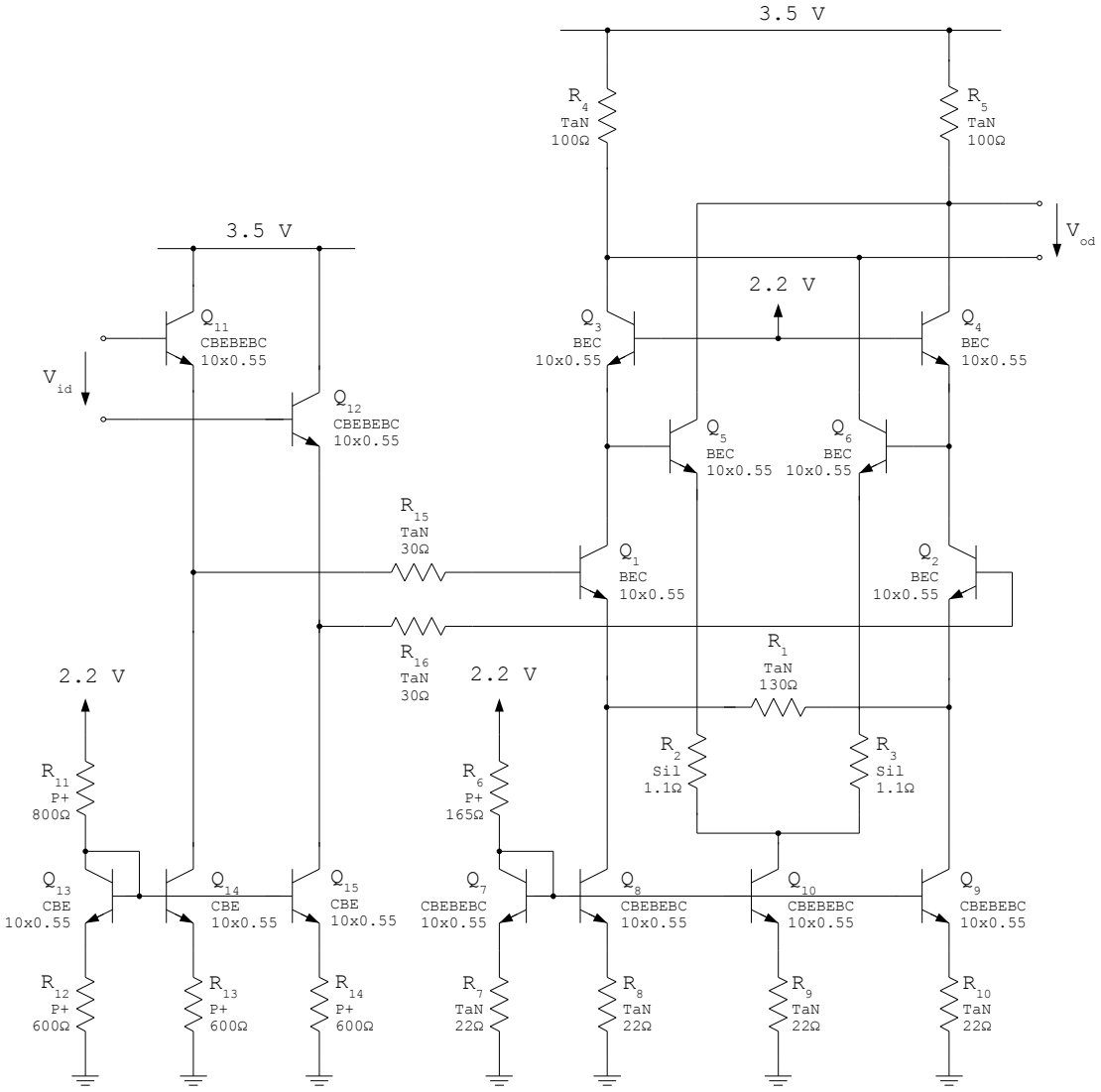


**Figure 3.11:** Schematic design of the 6 dB gain version of the compensated cascode

## 3.5 Variable-gain amplifier

### 3.5.1 Gilbert cell

The variable-gain amplifier is based on a Gilbert cell four-quadrant multiplier. The maximum gain of the amplifier is 6 dB, and the variation range of the gain is aimed to be at least 3 dB. To obtain sufficiently low distortion, the signal amplification part of the multiplier is a compensated cascode like the one described in Section 3.4.2. The collector resistors of the cascode are substituted by the gain variation circuitry. This gain variation part of the multiplier is realised by two cross-coupled differential pairs. As there is no measure taken to linearise these differential pairs, the gain variation is non-linear. More exactly, a variation of the gain control voltage $V_{Gain}$ causes a tanh-variation of the linear gain and a log (tanh)-variation of the gain on a dB-scale. However, this gain variation non-linearity does not influence the capability of the circuit to amplify signals with high linearity.

#### Transistor configuration

As this amplifier stage contains a high number of noise sources, the overall noise figure is high. To keep the noise from an excessive level, a low-noise contact configuration should be used for the transistors. The best noise performance is obtained by a CBEBEBC configuration. However, this strongly limits the bandwidth of the stage due to parasitics, so the CEBEC configuration is chosen. It provides better speed performance and degrades the noise performance only slightly compared to the former configuration. The highest speed would be obtained by BEC transistors, but with a noise figure higher than 20 dB at 200 Ω source impedance, this configuration type is not used for this circuit.
With CEBEC transistors, the bandwidth is still below the 10 GHz mark of the specifications. Since only one variable-gain stage is used in the overall amplifier chain, the impact of one amplifier with decreased bandwidth and increased group delay on the overall group delay of the chain is acceptable.

#### DC decoupling

Between an input and the corresponding output of the variable-gain amplifier there are always three transistors connected in series. The voltage rise due to their three collector-emitter voltages $V_{CE}$ cannot be compensated with the single emitter follower at the input. Multiple input emitter followers would cause the necessary larger voltage drop-off at the input, but are not realisable due to stability problems. Thus, the rise of the DC level between input and output must be avoided by adding DC decoupling capacitors to the output of the amplifier stage. To provide the input transistors of the successive stage with bias current and the correct DC voltage level, potential divider resistors are added after the decoupling capacitors. The principle of this circuit is shown in Figure 3.12.
The decoupling capacitors $C_1$ and $C_2$ form a high-pass filter with the input impedance of the following stage and the biasing network resistors $R_{17}$ to $R_{20}$. With 2 pF, the capacitance values are chosen high enough to have a cut-off frequency of 45 MHz, which is well below the 1.6 GHz operating frequency of the system. The resistor values chosen are high enough to avoid strong attenuation of the signal coming from the amplifier stage. On the other side they are low enough to provide stable biasing for the successive stage.

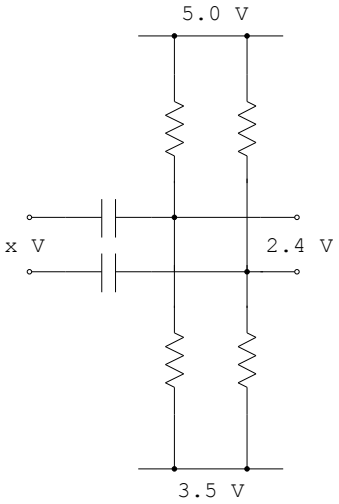


**Figure 3.12:** Principle of the DC decoupling circuit, consisting of DC blocking capacitors and a biasing resistor network.

### Collector resistors and biasing current

The collector resistors $R_4$ and $R_5$ are in parallel with the decoupling network. With a value of 94.5 Ω they yield the required differential output resistance of 200 Ω. In contrast to the fixed-gain amplifiers, the value of the collector resistors does not determine the value of the biasing current, because of the freely selectable DC level at the output of the Gilbert cell. At the decoupling network output the DC voltage is always equal to 2.4 V. Thus, the bias current is another variable, which can be used to optimise the linearity of this circuit. There exist two opposing effects, which lead to an increase of the third-order distortion at low and high currents. At low current levels the transistors' $C_\pi$ capacitances show higher non-linearity. At high current levels the $V_{CE}$ of the gain variation transistors is not high enough due to increased voltage drop-off across the collector resistors. This also leads to higher distortion, in this case due to the non-linearity of the $C_\mu$ capacitances. The simulation result (Figure 3.13) shows, that a biasing current of 13.8 mA leads to a minimum of third-order harmonic distortion.

### Biasing voltages

An emitter follower is used as the input buffer of the circuit and has a input DC level of 2.4 V. The resulting input DC level of 1.6 V of the principal transistor pair $Q_1$-$Q_2$ results in sufficiently high $V_{CE}$ voltage for the current mirror. The cascode transistors $Q_3$ and $Q_4$ are biased with a base potential of 2.2 V, which is the same value as for the fixed-gain compensated cascode. Together with the 2.4 V input voltage, all the cascode transistors are correctly biased.
The DC level of the gain command voltage at the bases of the transistors $Q_7$ to $Q_{10}$ is chosen as 2.7 V. This value allows enough space for the cascode transistors to work correctly. It is also low enough to provide sufficient headroom for the gain variation transistors $Q_7$ to $Q_{10}$ to have low distortion, which depends on the transistor's $V_{CE}$ voltages.

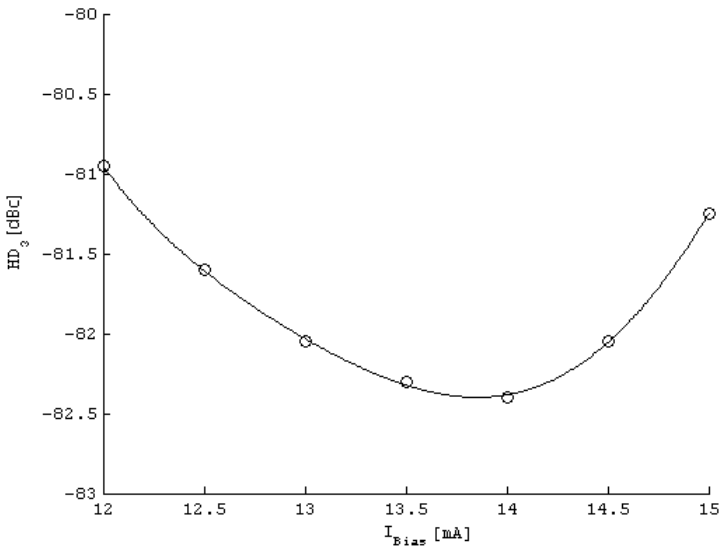


**Figure 3.13:** Simulation of the third-order harmonic distortion $HD_3$ of the whole amplifier vs. biasing current $I_{Bias}$ of the principal transistors $Q_1$ and $Q_2$. The maximum gain control voltage of 150 mV is applied. For each of the simulated points the emitter degeneration resistors $R_A$ and $R_E$ are chosen for highest possible linearity and a maximum gain of 6 dB. The highest linearity is obtained for a biasing current of 13.8 mA.

### Emitter degeneration resistances

As for the fixed-gain compensated cascode, the emitter degeneration resistors $R_E$ and $R_A$ of the principal transistor pair $Q_1$-$Q_2$ respectively the compensation amplifier $Q_5$-$Q_6$ are chosen to obtain the required gain and a minimum of $HD_3$. $R_E$ is mainly defining the voltage gain of the whole circuit, whereas $R_A$ mainly defines the gain of the compensation amplifier. Thus, $R_A$ is used to optimise the linearity. Figures 3.14 and 3.15 are used to determine a $R_E$ of 53 Ω and a $R_A$ of 0.7 Ω as the optimal choice. With these values, a gain of 6 dB is obtained for maximum $V_{Gain}$, which is equal to 150 mV. The third-order harmonic distortion is equal to −82.4 dBc, thus the major requirement of a $HD_3$ of −80 dBc is clearly fulfilled.

### Gain variation

The DC level at the input of the gain control part of the circuit is equal to 2.7 V and is constant, thus independent of the required voltage gain. The gain control voltage $V_{Gain}$ is the differential voltage across the gain control input, and influences the gain. The overall voltage at the base leads of the gain control transistors is equal to $2.7\,V \pm \frac{V_{Gain}}{2}$. Figure 3.16 depicts the log (tanh)-dependence of the logarithmic voltage gain of $V_{Gain}$. Figure 3.17 shows, that the third-order harmonic distortion over the whole gain range is approximately equal to or particularly at low gains smaller than the $HD_3$ value at maximum gain. In every case it is smaller than −80 dBc.

### Stability

As the signal amplification part of the variable-gain amplifier is based on the compensated cascode topology, it has the same stability problems as the fixed-gain cascode amplifier. The current sources do not have an infinitely high output resistance, and the capacitive coupling of the principal transistors to the ground leads to potential instability. As before, the output impedance of the emitter follower $Q_{15}$-$Q_{16}$ is not in the zone of stability of the cascode input. However, a stable behaviour is obtained by adding the small series resistors $R_{15}$ and $R_{16}$ to the input of the variable-gain amplifier. The gain control part of the amplifier is unconditionally stable, every possible impedance can be applied to its input. Thus, for this second input no additional stability measures are necessary.

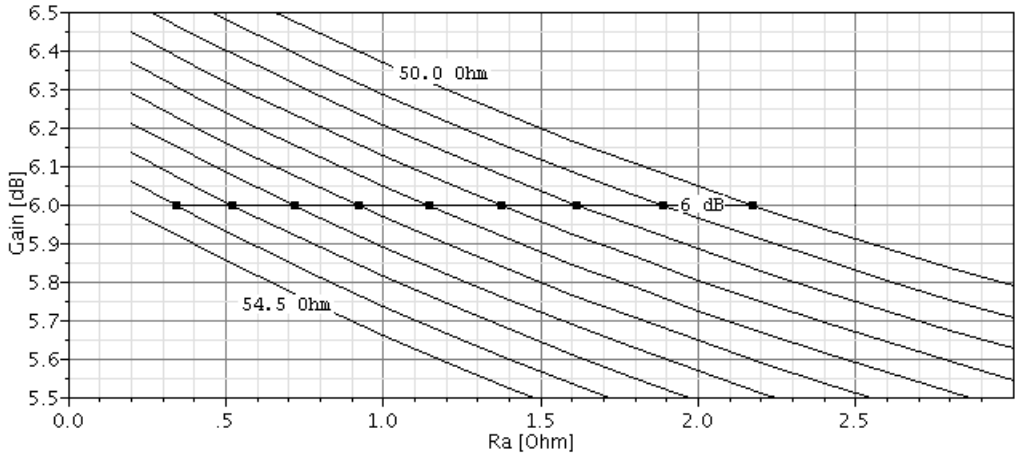


**Figure 3.14:** Maximum voltage gain of the whole amplifier vs. resistance $R_A$ of the compensation amplifier $Q_5$-$Q_6$ for different resistances $R_E$ of the principal transistors $Q_1$-$Q_2$. The maximum gain control voltage 150 mV is applied to the circuit. The resistor combinations with a gain of 6 dB are marked with squares.

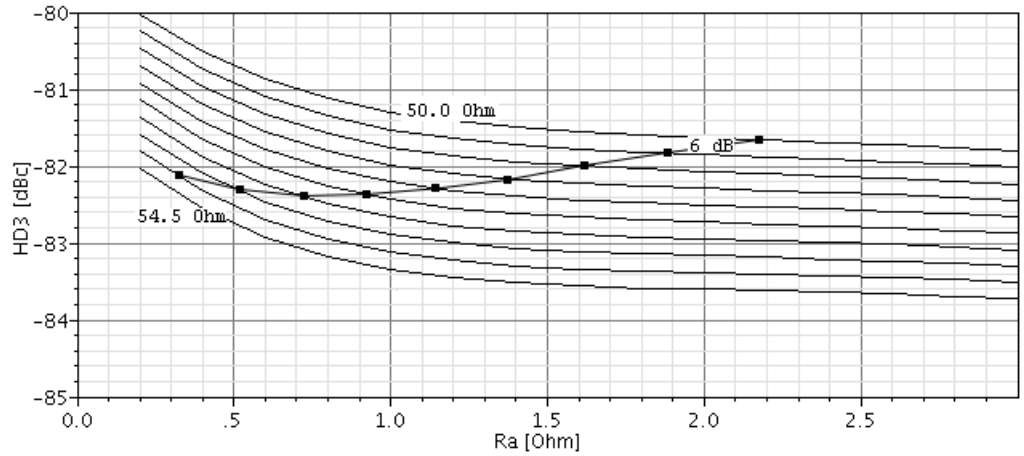


**Figure 3.15:** Third-order harmonic distortion of the whole amplifier vs. resistance $R_A$ of the compensation amplifier $Q_5$-$Q_6$ for different resistances $R_E$ of the principal differential pair $Q_1$-$Q_2$. The maximum gain control voltage 150 mV is applied to the circuit. The resistor combinations with a gain of 6 dB are marked with squares. The lowest distortion is equal to $-82.4$ dBc and obtained for $R_A = 0.7\,\Omega$ and $R_E = 53\,\Omega$.

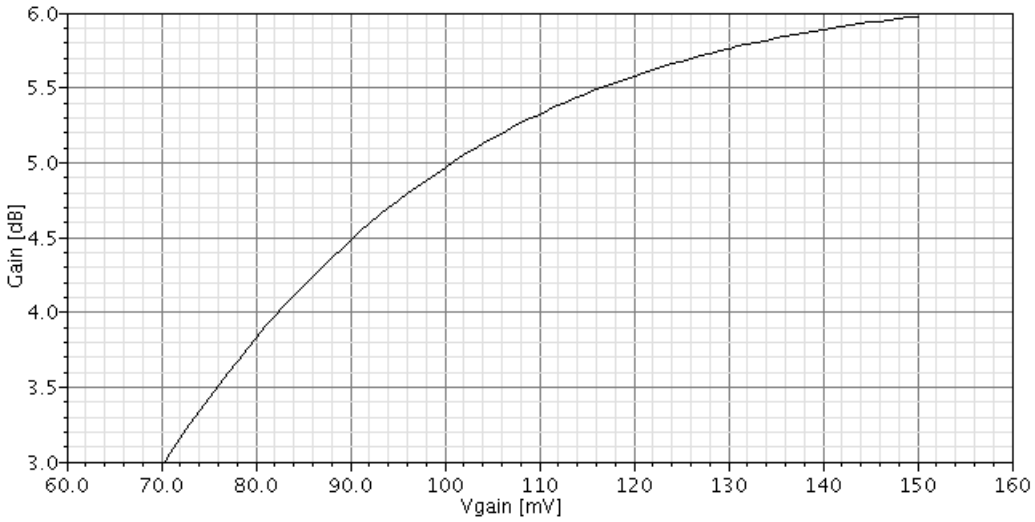


**Figure 3.16:** Logarithmic voltage gain vs. gain control voltage $V_{Gain}$. There is a log (tanh)-relation between these two variables.

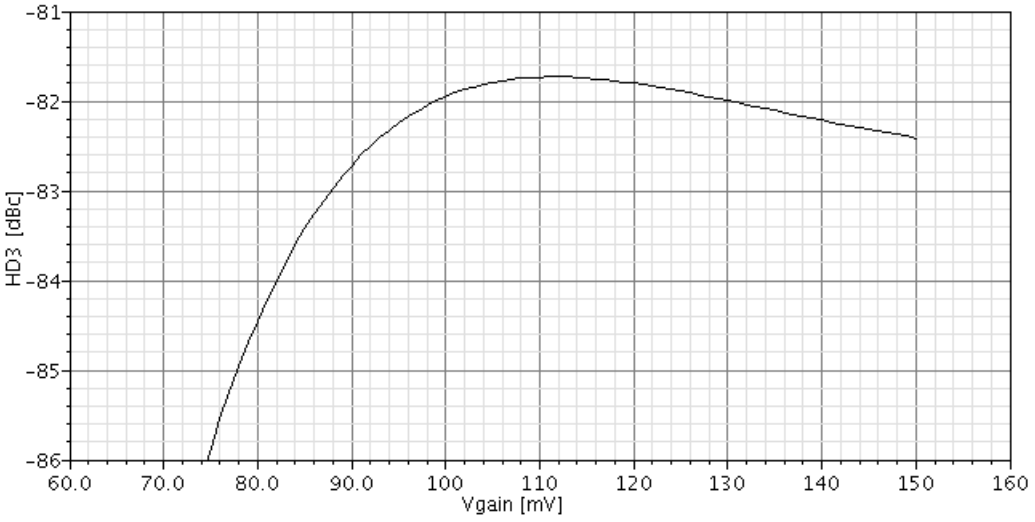


**Figure 3.17:** Third-order harmonic distortion vs. gain control voltage $V_{Gain}$. For all scenarios it stays below the required $-80\,\mathrm{dBc}$ limit.

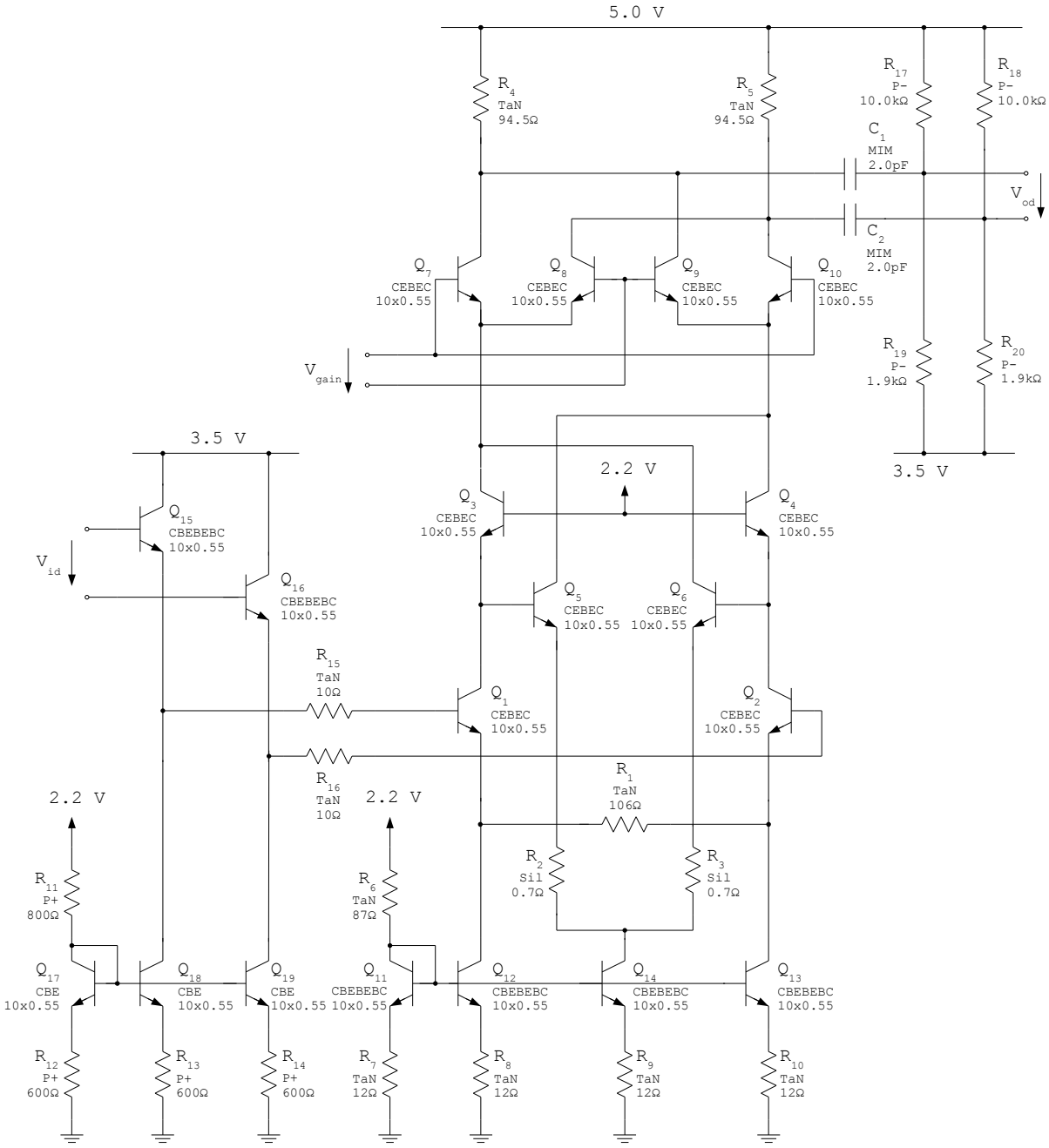


**Figure 3.18:** Schematic design of the variable gain amplifier, based on a Gilbert cell

# Chapter 4

# Performance analysis of the amplifier stages

The two fixed-gain amplifiers and the one variable-gain amplifier, which were designed in the preceding chapter, are analysed on the following pages.
At first the methods used for the simulations are described. The four principal circuit simulators provided by the GoldenGate simulation engine are mentioned. The circuit biasing and load impedance conditions are described and the measurement variables, which are determined by the following analyses, are listed.
In the main part of this chapter, simulations with nominal component values as well as Monte-Carlo analyses with consideration of statistical deviations are executed, and the results are presented in tabular and graphical form.
Finally, the simulation results for each of the designed topologies are discussed. It is determined whether the amplifiers comply with the desired specification.

## 4.1 Simulation methods

### 4.1.1 Simulation engine

The used GoldenGate RFIC simulation engine and analysis software from Agilent provides a range of time- and frequency-domain simulators. DC, AC, transient, harmonic balance, multi-tone, small- and large-signal scattering parameter, envelope and noise simulations can be performed by this simulation engine. If statistical data is provided by the technology library, which is the case for the used B7HF200 technology, statistical Monte-Carlo analyses can be made to consider global process manufacturing variations as well as mismatch between single circuit components. The influence of temperature is also considered by the simulations.

For this work, the following simulators are used:

- DC simulator
  This basic simulator calculates the quiescent bias point of a circuit. It provides the initial conditions for more sophisticated simulations.

- AC simulator
  The whole circuit is linearised by first calculating the DC operating points of the circuit elements, and then substituting the characteristic functions of these components by the tangents at their operation point [4]. Simulation results of such a linearised network are only completely valid for infinitely small excitations at the input, but are a good approximation for small input signals. As an AC simulation is only linear, no non-linear effects like the generation of higher-order harmonics can be studied.

- Scattering parameter simulator
  With this method, the circuit is first linearised and then an S-parameter matrix of the given linear n-port network is calculated. The matrix contains the voltage reflection coefficient for each port and transmission coefficients between all the different ports. Signal stimuli and power measurement capabilities are provided by so-called S-probes with $50\,\Omega$ impedance. The number of S-probes is equal to the number of network ports, an example of their application is depicted in Figure 4.1.
  Lots of useful measures deviated from the S-parameters are available. Rollet's stability factor (also known as K-factor), noise figure analyses, circles of constant gain and circles of constant noise as well as source impedance stability and load impedance stability circles are some of them. All these forms of microwave analyses are described in detail in [35].

- Harmonic balance simulator
  With the above mentioned methods only linear analyses can be performed. The harmonic balance method also covers the non-linear behaviour of the circuit. It provides the steady state response of the circuit to a sinusoidal input signal. The circuit response contains all higher-order harmonics up to a defined order, which are caused by the circuit's non-linearity. For the simulations of this work the order limit is set to the fifteenth harmonic, which provides sufficient accuracy and avoids overwhelming computational effort.
  To calculate the non-linear steady state response of a circuit, a transient analysis could be performed by solving the differential equations, which describe the system. However, tf the circuit contains elements with high time constants, it has to be integrated over a large number of input signal periods to obtain the wanted transient-free result. This transient analysis method is not efficient from a computational point of view and due to the long integration time, accuracy errors are summarised. A more efficient approach is the harmonic balance analysis [36]. It cuts the network into linear and non-linear parts. The linear parts are solved in the frequency domain, whereas the non-linear parts are solved in the time-domain with following Fourier transformation. With iterative calculation steps, the difference between the voltages at the ports of the linear and non-linear networks is minimised. When the voltages at the interfaces between the networks are identical, the steady state solution is found.

### 4.1.2 Biasing, load impedance, input and output voltage

#### Biasing circuit

The inputs of the devices under test have to be biased appropriately. A polarisation circuit consisting of DC-blocking capacitors for the signal path and signal-blocking polarisation inductors in series with a biasing voltage source is needed for all analyses. The following circuit is a biasing example for an S-parameter simulation, the same principle is also applied for the other simulations.

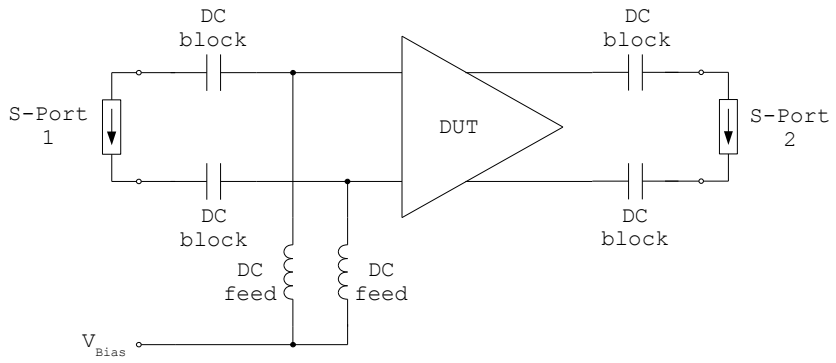


**Figure 4.1:** S-parameter analysis example including S-probes and a biasing circuit.

**Load impedance**

In the case of AC and harmonic balance simulations, the output of the device under test is charged by a successive emitter follower with open output, which builds the amplifier's load impedance. So additional distortion by the non-linear behaviour of the input impedance of the following amplifier stage can be considered. Furthermore, its capacitive behaviour reduces the bandwidth of the devices under test and leads to realistic bandwidth results.

**Input and output voltages**

The harmonic balance simulations are the only ones, where the signal input voltage level has to be defined. The input voltages of these analyses are fixed to a level, which yields $600\,\mathrm{mV_{pp}}$ output voltage for the fixed-gain amplifiers as well as the variable-gain amplifier at maximum gain. This allows comparable simulation results, independent of gain variations due to different simulation temperatures.

### 4.1.3 Simulation variables

In the next two sections of this chapter the following simulation variables are determined with the help of the listed simulators, to verify the amplifiers' conformance to the specifications:

| Variable | Simulator |
|---|---|
| Third-order harmonic distortion $HD_3$ | Harmonic balance |
| Differential voltage gain $A_d$ | Harmonic balance |
| Bandwidth B | AC |
| Group delay $\tau_g$ | AC |
| Output impedance magnitude $\lvert Z_{out}\rvert$ | S-Parameter |
| Noise figure F | S-Parameter |
| Power dissipation $P_{Diss}$ | DC |

**Table 4.1:** Simulation variables and the used simulation engines.

## 4.2 Fixed-gain amplifiers

In this section the values obtained by the simulations of the emitter-coupled pair with diode-connected load and the compensated cascode are presented. The simulations with nominal component values are made for 27 °C room temperature [1], as well as for −20 and 70 °C. The statistical Monte-Carlo simulations consider process variations and component mismatch. Its simulation results are given as mean value $\mu$, standard deviation $\sigma$ as well as smallest and largest value. If not indicated separately, 1000 trials are calculated for each statistical simulation.

### 4.2.1 Nominal simulation

| Topology | D. p. with diode-connected load | | | Compensated cascode | | |
|---|---|---|---|---|---|---|
| Temperature [°C] | −20 | 27 | 70 | −20 | 27 | 70 |
| $HD_3$ [dBc] | -84.21 | **-88.60** | -86.08 | -80.55 | **-80.33** | -80.72 |
| $A_d$ [dB] @ 1.6 GHz | 5.92 | **5.88** | 5.84 | 6.10 | **6.00** | 5.87 |
| $B$ [GHz] | 12.58 | **11.47** | 10.65 | 10.12 | **9.72** | 9.35 |
| $\tau_g$ [ps] @ 1.6 GHz | 14.5 | **15.8** | 17.1 | 18.0 | **19.5** | 21.1 |
| $\lvert Z_{out}\rvert$ [Ω] | 198.7 | **199.7** | 200.6 | 199.0 | **198.3** | 197.6 |
| $F$ [dB] @ 50 Ω | 9.6 | **10.3** | 11.0 | 18.0 | **18.1** | 18.2 |
| $F$ [dB] @ 100 Ω | 7.0 | **7.7** | 8.2 | 15.1 | **15.1** | 15.2 |
| $F$ [dB] @ 200 Ω | 4.8 | **5.4** | 5.8 | 12.0 | **12.2** | 12.1 |
| $P_{Diss}$ [mW] | 131.2 | 134.5 | 137.2 | 105.4 | 102.6 | 100.3 |

**Table 4.2:** Results of the nominal simulation of the fixed-gain amplifier circuits.

In Annex B.1.1 there are result plots for the nominal analysis at room temperate. They are complementary to the tabular data and shall give deeper insight into the amplifier behaviour. Plots for −20 and 70 °C are not included, to keep the annex at a reasonable size.

[1] Room temperature results are written in bold letters

### 4.2.2 Statistical simulation

#### Third-order harmonic distortion

| $HD_3$ [dBc] | | | | | | |
|---|---|---|---|---|---|---|
| Topology | D. p. with diode-connected load | | | Compensated cascode | | |
| Temperature [°C] | −20 | 27 | 70 | −20 | 27 | 70 |
| $\mu$ | -84.60 | **-89.09** | -86.17 | -80.18 | **-80.13** | -80.45 |
| $\sigma$ | 2.09 | **3.76** | 2.37 | 0.90 | **1.55** | 2.07 |
| min. | -96.43 | **-102.4** | -93.73 | -82.32 | **-74.99** | -73.47 |
| max. | -80.65 | **-82.01** | -80.59 | -76.82 | **-85.86** | -86.75 |
| $> -80$ dBc [%] | 0.0 | **0.0** | 0.0 | 42.0 | **43.3** | 41.4 |

**Table 4.3:** Statistical simulation of the third-order harmonic distortion of the fixed-gain amplifiers. Histograms with the statistical distribution of the $HD_3$ value for room temperature conditions are shown in Annex B.1.2.

#### Voltage gain

| $A_d$ [dB] @ 1.6 GHz | | | | | | |
|---|---|---|---|---|---|---|
| Topology | D. p. with diode-connected load | | | Compensated cascode | | |
| Temperature [°C] | −20 | 27 | 70 | −20 | 27 | 70 |
| $\mu$ | 5.92 | **5.88** | 5.83 | 6.10 | **6.01** | 5.87 |
| $\sigma$ | 0.01 | **0.01** | 0.02 | 0.11 | **0.10** | 0.10 |
| min. | 5.89 | **5.80** | 5.70 | 5.75 | **5.69** | 5.55 |
| max. | 5.94 | **5.92** | 5.88 | 6.50 | **6.36** | 6.21 |

**Table 4.4:** Statistical simulation of the differential voltage gain of the fixed-gain amplifiers.

#### Bandwidth

| $B$ [GHz] | | | | | | |
|---|---|---|---|---|---|---|
| Topology | D. p. with diode-connected load | | | Compensated cascode | | |
| Temperature [°C] | −20 | 27 | 70 | −20 | 27 | 70 |
| $\mu$ | 12.73 | **11.61** | 10.77 | 10.22 | **9.81** | 9.43 |
| $\sigma$ | 0.69 | **0.63** | 0.59 | 0.49 | **0.46** | 0.43 |
| min. | 11.12 | **10.18** | 9.45 | 9.03 | **8.68** | 8.36 |
| max. | 14.73 | **13.49** | 12.56 | 11.53 | **10.98** | 10.57 |

**Table 4.5:** Statistical simulation of the 3 dB-bandwidth of the fixed-gain amplifiers.

### Group delay

| $\tau_g$ [ps] @ 1.6 GHz | | | | | | |
|---|---|---|---|---|---|---|
| Topology | D. p. with diode-connected load | | | Compensated cascode | | |
| Temperature [°C] | −20 | 27 | 70 | −20 | 27 | 70 |
| $\mu$ | 12.7 | **15.6** | 16.9 | 17.6 | **19.1** | 20.7 |
| $\sigma$ | 0.7 | **0.7** | 0.8 | 0.7 | **0.7** | 0.8 |
| min. | 11.1 | **13.6** | 14.7 | 15.8 | **17.2** | 18.5 |
| max. | 14.7 | **17.6** | 19.0 | 19.5 | **21.2** | 22.8 |

**Table 4.6:** Statistical simulation of the group delay of the fixed-gain amplifiers.

### Output impedance magnitude

| $\lvert Z_{out}\rvert$ [Ω] | | | | | | |
|---|---|---|---|---|---|---|
| Topology | D. p. with diode-connected load | | | Compensated cascode | | |
| Temperature [°C] | −20 | 27 | 70 | −20 | 27 | 70 |
| $\mu$ | 198.4 | **199.4** | 200.2 | 199.5 | **198.7** | 198.0 |
| $\sigma$ | 6.2 | **6.2** | 6.2 | 6.3 | **6.2** | 6.2 |
| min. | 178.0 | **178.9** | 179.7 | 178.7 | **178.0** | 177.4 |
| max. | 217.4 | **218.3** | 219.1 | 218.3 | **217.5** | 216.7 |

**Table 4.7:** Statistical simulation of the output impedance magnitude of the fixed-gain amplifiers.

### Noise figure

| $F$ [dB] @ 50 Ω | | | | | | |
|---|---|---|---|---|---|---|
| Topology | D. p. with diode-connected load | | | Compensated cascode | | |
| Temperature [°C] | −20 | 27 | 70 | −20 | 27 | 70 |
| $\mu$ | 9.64 | **10.39** | 11.01 | 18.16 | **18.09** | 18.08 |
| $\sigma$ | 0.10 | **0.10** | 0.11 | 0.37 | **0.35** | 0.34 |
| min. | 9.31 | **10.05** | 10.67 | 16.90 | **16.92** | 16.99 |
| max. | 9.95 | **10.7** | 11.35 | 19.56 | **19.39** | 19.31 |

**Table 4.8:** Statistical simulation of the noise figure of the fixed-gain amplifiers.

### 4.2.3 Performance analysis summary

#### Third-order harmonic distortion

Basically, $HD_3$ distortion increases with increasing input respectively output voltage level. The voltage gain of the amplifiers varies with temperature, so for different temperatures a fixed input voltage level leads to different output voltage levels, which influences the distortion measurement. Because of this, the output level is fixed to $600\,mV_{pp}$, independent of temperature, to obtain comparable $HD_3$ results. The input voltage is adapted to obtain this output voltage for all simulated temperatures.
The emitter-coupled pair has an excellent room temperature $HD_3$ of $-88.6\,dBc$. Even under degrading influence due to temperature and statistical variations, the $-80\,dBc$ limit is never exceeded. Therefore, the emitter-coupled pair fulfils the linearity specifications under all simulated conditions.
By contrary, even under nominal conditions the compensated cascode is only slightly below the distortion limit. When statistical variations are taken into account, this topology clearly fails the requirements. For nearly half of the simulated cases, the linearity requirement cannot be fulfilled. The relative $HD_3$ histogram (Figure B.6) underlines this major drawback of the compensated cascode circuit.

#### Differential voltage gain

Under standard conditions, the emitter-coupled pair with diode-connected load has a voltage gain of 5.88 dB. This is slightly lower than the desired 6 dB and caused by component imperfections like parasitic impedances. However, this small gain degradation is within acceptable limits. The voltage gain of the compensated cascode is exactly adjusted to 6.00 dB, which is made possible with the right choice of the emitter degeneration resistors.
Temperature has a small influence on the gain of both amplifier types. At high temperatures the gain is increased, at low temperatures decreased by some hundredths of a dB. The statistical analysis shows, that with a standard deviation of 0.01 dB the gain of the emitter-coupled pair is virtually insensible to statistical deviations of the circuit components. The gain of the compensated cascode shows stronger statistical deviations and has a standard deviation of 0.1 dB. These deviations are assumed to be small enough to be compensated by the variable-gain amplifier.

#### Speed performance

With 11.47 and 9.72 GHz, both amplifiers are near the 10 GHz-mark and have acceptable bandwidth. The emitter-coupled pair with diode-connected load easily obtains this value, even under the use of the slow CBEBEBC transistor configuration. The compensated cascode has approximately 2 GHz less bandwidth, in spite of using the faster and noisy CBE transistors.
As higher amplifier bandwidth results in lower group delay, the emitter-coupled pair is also better performing from this point of view. At 1.6 GHz the emitter-coupled pair has a $\tau_g$ of 15.8 ps, the substantially higher $\tau_g$ of the compensated cascode is equal to 19.5 ps.
Statistical deviations of about 1 ps are quite probable, maximal speed degradations of 2 ps can be expected under the worst conditions. Temperature also influences the dynamic performance of the amplifiers. Rising temperature means lower bandwidth respectively higher group delay. For both circuits a change from room temperature to 70 °C increases the $\tau_g$ of about one and a half pico-second. A temperature decrease to $-20\,°C$ decreases $\tau_g$ of about the same amount. These possible group delay variations may increase the delay of the compensated cascode above the desirable value of 20 ps.

#### Output impedance magnitude

The nominal output impedance of both amplifier types is approximately equal to the desired value of $200\,\Omega$. The data sheet of the used technology gives a course relative tolerance of $\pm 10\%$ for the used TaN collector resistors. Consequently, this high tolerance results in a statistically strongly varying output impedance. Simulations show, that the minimum and maximum values obtained by the Monte-Carlo simulations are nearly equal to relative tolerance of 10% given in the data sheet.
The biggest uncertainty factor for the output impedance is not the variation of the transistor properties, but the one of the resistors. The equal standard deviation for the two different amplifiers shows that

the diodes of the emitter-coupled pair do not perceptibly influence the statistical properties of its output impedance magnitude.

**Noise figure**

The first stage of the amplifier chain is connected to a signal source with 100 Ω output impedance. Except for the first amplifier stage, the source impedances for all the other amplifiers are fixed to 200 Ω. Therefore, the noise figures of interest are the ones for these two source impedance values. Smith charts with circles of constant noise (Figure B.4) give values of 7.7 and 5.4 dB for the emitter-coupled pair diode-connected load. The compensated cascode has much higher noise figures with values about twice as high.
A slight temperature dependence leads to a noise variation of some tenths of dB in the given temperature range. Higher temperature leads to higher noise. The noise figure change due to statistical variations is in the same order of magnitude.

**Power consumption**

Due to its lower supply voltage, the compensated cascode power dissipation is only three quarters of the dissipation of the emitter-coupled pair, even with a higher biasing current.

### 4.2.4 Specification conformity of the fixed-gain amplifier topologies and final selection

The emitter-coupled pair with diode-connected load is performing equally or better concerning all simulated variables then the compensated cascode, except for the higher power consumption. In contrast, the compensated cascode has a major drawback. Under consideration of statistical variations, the third-order distortion is not reliably lower than the −80 dBc limit. Statistical simulations show that in more than 40% of the simulated cases the compensated cascode does not fulfil the linearity requirement. Other drawbacks are the excessive noise level of this circuit, which does not allow to use it for the first stages of the amplifier chain, and its reduced speed.

| Fixed-gain amplifiers | | |
|---|---|---|
| | D. p. with diodes | Comp. cascode |
| Necessary requirements | | |
| $HD_3$ | + | - |
| Desirable requirements | | |
| $A_d$ | + | + |
| $B$, $\tau_g$ | + | ○ |
| $\lvert Z_{out}\rvert$ | + | + |
| Other properties | | |
| $F$ | + | ○ |
| $P_{Diss}$ | ○ | + |

**Table 4.9:** Overview of the fixed-gain amplifiers' performances

Regarding the required amplifier properties, the emitter-coupled pair with diode-connected load is always within the allowed limits. The compensated cascode is not linear enough, has a high noise figure and is slower than its counterpart. Therefore the emitter-coupled pair circuit is the preferred fixed-gain amplifier design for this work.

## 4.3 Variable-gain amplifier

Like for the fixed-gain amplifier stages, the variable-gain amplifier behaviour is simulated under nominal conditions as well as under consideration of statistical variations. The simulations are again made for −20, 27 and 70 °C. Compared to the preceding section, an additional variable to be chosen is the gain control voltage. Simulations show, that the amplifier has a distortion maximum for $V_{Gain}$ of 110 mV. This critical value as well as maximum and minimum gain control voltages 70 mV and 150 mV are used for the simulations.

### 4.3.1 Nominal simulation

| Topology | Gilbert cell | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 110 | 150 | 70 | 110 | 150 | 70 | 110 | 150 |
| $HD_3$ [dBc] | -82.66 | -81.48 | -82.14 | **-87.76** | **-81.73** | **-82.41** | -91.45 | -82.74 | -82.88 |
| $A_d$ [dB] @ 1.6 GHz | 4.04 | 5.74 | 6.07 | **2.95** | **5.31** | **5.97** | 1.73 | 4.56 | 5.55 |
| $B$ [GHz] | 5.44 | 6.29 | 6.50 | **5.09** | **5.95** | **6.32** | 4.89 | 5.65 | 6.09 |
| $\tau_g$ [ps] @ 1.6 GHz | 34.5 | 31.3 | 30.5 | **37.5** | **33.9** | **32.6** | 40.0 | 36.6 | 34.8 |
| $\lvert Z_{out}\rvert$ [Ω] | 201.2 | 200.7 | 200.6 | **200.5** | **200.2** | **200.0** | 200.0 | 199.8 | 199.5 |
| $F$ [dB] @ 50 Ω | 19.8 | 18.1 | 18.0 | **21.3** | **18.5** | **18.2** | 22.8 | 19.1 | 18.4 |
| $F$ [dB] @ 100 Ω | 16.8 | 15.1 | 15.0 | **18.3** | **15.5** | **15.2** | 19.8 | 16.1 | 15.4 |
| $F$ [dB] @ 200 Ω | 13.8 | 12.1 | 12.0 | **15.3** | **12.5** | **12.2** | 16.8 | 13.1 | 12.4 |
| $P_{Diss}$ [mW] | 238.0 | 237.9 | 237.9 | 243.5 | 243.5 | 243.5 | 248.3 | 248.2 | 248.2 |

**Table 4.10:** Results of the nominal simulation of the variable-gain amplifier circuit.

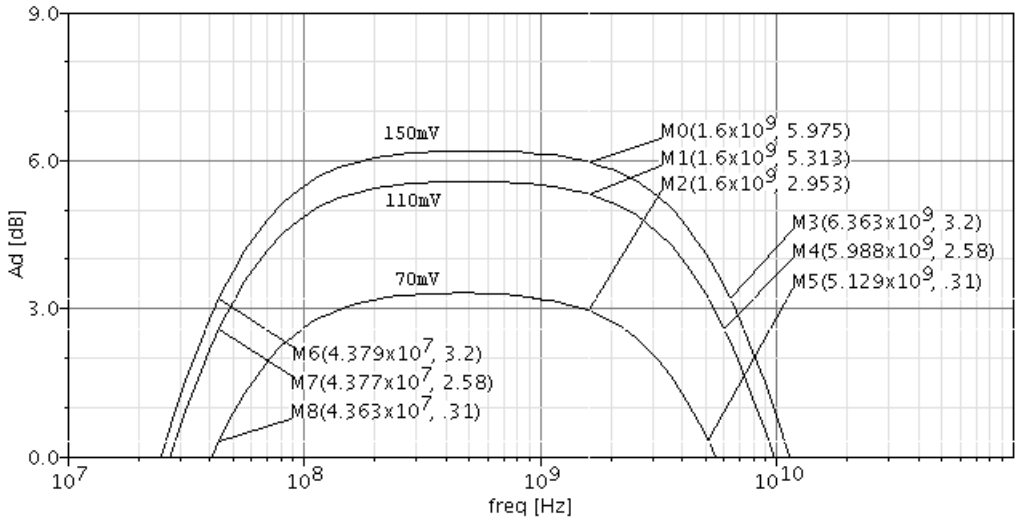


**Figure 4.2:** Nominal simulation of the amplifier's frequency response at room temperature. The differential voltage gain $A_d$ is plotted over the frequency axis. The gain control voltage is varied between three values. Markers $M_0$, $M_1$ and $M_2$ display the voltage gain at 1.6 GHz. Markers $M_3$, $M_4$ and $M_5$ are positioned 3 dB below maximum voltage gain and give the upper cut-off frequency of the circuit. The lower cut-off frequency is marked with $M_6$ to $M_8$.

### 4.3.2 Statistical simulation

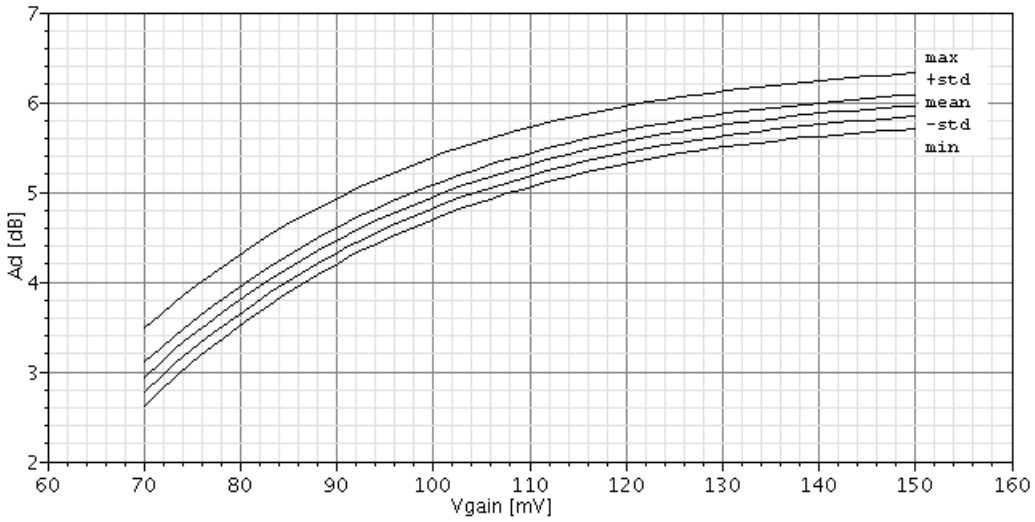


**Figure 4.3:** Statistical simulation of the differential voltage gain $A_d$ vs. gain control voltage $V_{Gain}$. Lines with the mean value, mean value plus/minus standard deviation, as well as the absolute maximum and minimum value are displayed. The simulation contains 100 trials.

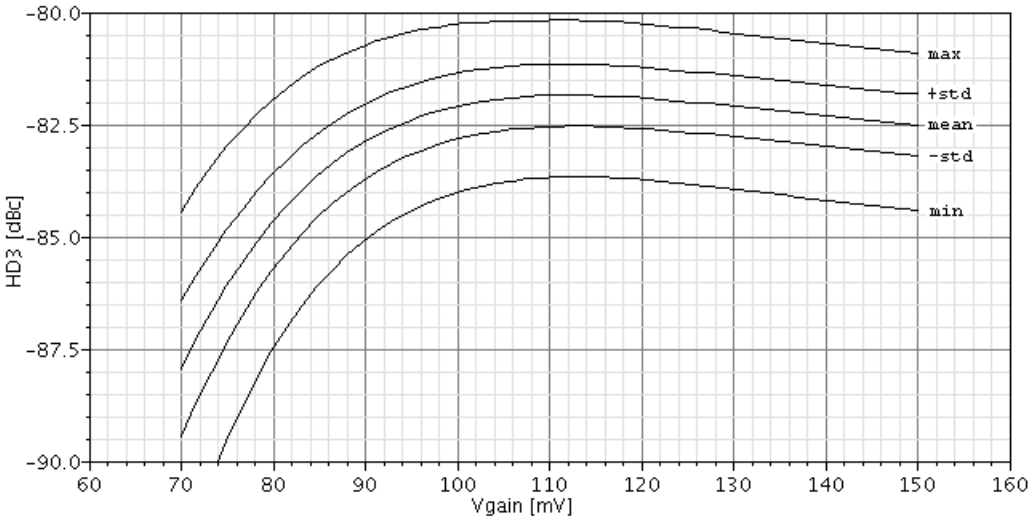


**Figure 4.4:** Statistical simulation of the third-order harmonic distortion $HD_3$ vs. gain control voltage $V_{Gain}$. Otherwise, conditions as above apply.

### Third-order harmonic distortion

| $HD_3$ [dBc] | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Topology | Gilbert cell | | | | | | | | |
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 110 | 150 | 70 | 110 | 150 | 70 | 110 | 150 |
| $\mu$ | -82.59 | -81.39 | -82.06 | **-87.92** | **-81.78** | **-82.45** | -90.81 | -82.91 | -83.03 |
| $\sigma$ | 0.48 | 0.46 | 0.46 | **1.61** | **0.73** | **0.73** | 3.19 | 1.53 | 1.52 |
| min. | -83.69 | -82.71 | -83.34 | **-95.14** | **-84.87** | **-85.6** | -112.9 | -90.01 | -90.54 |
| max. | -80.73 | -79.55 | -80.35 | **-83.23** | **-78.83** | **-79.78** | -82.59 | -77.87 | -78.02 |
| $> -80$ dBc [%] | 0.0 | 0.3 | 0.0 | **0.0** | **0.8** | **0.1** | 0.0 | 2.5 | 1.9 |

**Table 4.11:** Statistical simulation of the third-order harmonic distortion of the variable-gain amplifier. Histograms with the statistical distribution of the $HD_3$ value for room temperature conditions are shown in Annex B.2.2.

### Voltage gain

| $A_d$ [dB] @ 1.6 GHz | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Topology | Gilbert cell | | | | | | | | |
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 110 | 150 | 70 | 110 | 150 | 70 | 110 | 150 |
| $\mu$ | 4.13 | 5.85 | 6.18 | **2.94** | **5.31** | **5.96** | 1.79 | 4.63 | 5.63 |
| $\sigma$ | 0.159 | 0.134 | 0.133 | **0.181** | **0.140** | **0.132** | 0.209 | 0.158 | 0.139 |
| min. | 3.67 | 5.40 | 5.74 | **2.41** | **4.85** | **5.51** | 1.07 | 4.08 | 5.11 |
| max. | 4.71 | 6.42 | 6.76 | **3.51** | **5.84** | **6.48** | 2.37 | 5.16 | 6.14 |

**Table 4.12:** Statistical simulation of the voltage gain of the variable-gain amplifier.

### Bandwidth

| $B$ [GHz] | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Topology | Gilbert cell | | | | | | | | |
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 110 | 150 | 70 | 110 | 150 | 70 | 110 | 150 |
| $\mu$ | 5.37 | 6.21 | 6.44 | **5.03** | **5.88** | **6.25** | 4.81 | 5.57 | 6.03 |
| $\sigma$ | 0.21 | 0.26 | 0.28 | **0.20** | **0.24** | **0.27** | 0.20 | 0.22 | 0.25 |
| min. | 4.93 | 5.67 | 5.82 | **4.62** | **5.39** | **5.68** | 4.41 | 5.12 | 5.51 |
| max. | 6.04 | 6.97 | 7.23 | **5.68** | **6.61** | **7.02** | 5.44 | 6.28 | 6.78 |

**Table 4.13:** Statistical simulation of the 3 dB-bandwidth of the variable-gain amplifier.

### Group delay

| $\tau_g$ [ps] @ 1.6 GHz | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Topology | Gilbert cell | | | | | | | | |
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 110 | 150 | 70 | 110 | 150 | 70 | 110 | 150 |
| $\mu$ | 34.4 | 31.3 | 30.6 | **37.4** | **33.9** | **32.7** | 39.9 | 36.6 | 34.8 |
| $\sigma$ | 1.0 | 1.0 | 1.0 | **1.1** | **1.1** | **1.1** | 1.2 | 1.2 | 1.2 |
| min. | 31.6 | 28.7 | 28.0 | **34.3** | **31.1** | **29.9** | 36.6 | 33.4 | 31.8 |
| max. | 36.7 | 33.5 | 32.8 | **39.8** | **16.3** | **35.0** | 42.5 | 39.1 | 37.4 |

**Table 4.14:** Statistical simulation of the group delay of the variable-gain amplifier.

### Output impedance magnitude

| $\lvert Z_{out}\rvert$ [Ω] | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Topology | Gilbert cell | | | | | | | | |
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 110 | 150 | 70 | 110 | 150 | 70 | 110 | 150 |
| $\mu$ | 201.0 | 200.5 | 200.3 | **200.3** | **199.9** | **199.7** | 199.7 | 199.5 | 199.3 |
| $\sigma$ | 5.5 | 5.6 | 5.7 | **5.5** | **5.6** | **5.6** | 5.5 | 5.5 | 5.5 |
| min. | 184.5 | 184.0 | 183.8 | **183.9** | **183.5** | **183.3** | 183.4 | 183.1 | 182.9 |
| max. | 217.7 | 217.4 | 217.3 | **216.9** | **216.7** | **216.5** | 216.2 | 216.1 | 216.0 |

**Table 4.15:** Statistical simulation of the output impedance magnitude of the variable-gain amplifier.

### Noise figure

| $F$ [dB] @ 50 Ω | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Topology | Gilbert cell | | | | | | | | |
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 110 | 150 | 70 | 110 | 150 | 70 | 110 | 150 |
| $\mu$ | 19.83 | 18.09 | 17.95 | **21.43** | **18.53** | **18.15** | 22.93 | 19.17 | 18.41 |
| $\sigma$ | 0.18 | 0.26 | 0.27 | **0.17** | **0.22** | **0.24** | 0.20 | 0.19 | 0.23 |
| min. | 19.24 | 17.38 | 17.21 | **20.79** | **17.93** | **17.45** | 22.25 | 18.62 | 17.77 |
| max. | 20.32 | 18.89 | 18.79 | **21.94** | **19.18** | **18.90** | 23.51 | 19.68 | 19.09 |

**Table 4.16:** Statistical simulation of the noise figure of the variable-gain amplifier.

### 4.3.3 Performance analysis summary

#### Third-order harmonic distortion

The $HD_3$ distortion is small for low gains, i.e. low output voltage, and increases with increasing gain. For a gain control voltage of about 110 mV, the distortion is maximal. After this maximum it is slightly decreasing, until the maximum gain is reached. At the critical gain control value of 110 mV and room temperature, 0.8% of the statistical cases do not fulfil the linearity criterion of a $HD_3$ smaller than $-80$ dBc. This is an acceptable number of failing circuits and according to the specifications. At 70 °C this number grows up to 2.5%, which lies above the 1%-limit. However, this 1%-requirement is only defined for room temperature, so the slightly elevated number of insufficiently linear circuits at high temperatures has only minor relevance and does not mean inacceptable behaviour of the variable-gain amplifier.

#### Differential voltage gain

By varying the gain control voltage from 70 to 150 mV, the gain is varied between 2.95 dB and 5.97 dB, nominal conditions and room temperature assumed. This is close to the desired variation between 3 and 6 dB. The variation of the logarithmic gain between these two values is not linearly related to control voltage variation, but follows a log (tanh) law. Increasing the gain control voltage to values far beyond 150 mV would increase the gain to about 6.2 dB. However, this is not advisable, because of the small sensibility of the circuit to gain control voltage changes in this high gain region.
The gain value of the variable-gain amplifier is more dependent on statistical variations than the one of the emitter-coupled pair with diode-connected load. The standard deviation is about 0.15 dB, which leads to maximal deviations from medium gain of $\pm 0.5$ dB. However, this difference to the desired gain value is only given in very rare cases.
Temperature strongly influences the gain, notably at low gain levels. As this variation at low gain can easily be compensated by adapting the gain control voltage, the highest gain value is more critical. In a temperature range from $-20$ to 70 °C, 6.07 to 5.55 dB maximum gain are obtained. Knowing this fact, the amplifier should not be used at maximum gain at room temperature, to allow temperature variation compensation.

#### Speed performance

Due to the high number of transistors and their low-noise CEBEC configuration, this circuit is slower than the fixed-gain amplifiers. At nominal temperature it has a bandwidth between 5.13 and 6.36 GHz in its gain range from 2.95 to 5.97 dB. This low bandwidth is accompanied with an accordingly high group delay of 37.5 to 32.6 ps.

#### Output impedance magnitude

The output impedance magnitude behaviour of the variable-gain amplifier is equal to the one of the fixed-gain amplifiers. The main factor of uncertainty is statistical deviation, which leads to a maximal relative deviation of the mean value of about $\pm 10\%$.

#### Noise figure

At maximum gain, 200 Ω source impedance and room temperature, the amplifier has a noise figure of 12.2 dB. A decrease in amplifier gain can be seen as an attenuation. The noise figure increases at about the same amount, as the attenuation increases. At 3 dB gain, the amplifier has a noise figure of 15.3 dB. Therefore, this circuit has a high noise level.
As for the fixed-gain amplifiers, temperature influences the noise figure. Assuming the same gain control voltage for higher temperatures, the noise figure increases even more.

#### Power consumption

Due to the high biasing currents and the high supply voltage of 5 V, this amplifier is the most consuming circuit, which has been designed. It is equal to 0.24 W.

### 4.3.4 Specification conformity of the variable-gain amplifier

With the Gilbert cell 4-quadrant multiplier with a compensated cascode as the signal amplifier it is possible to vary the differential voltage gain in a range from 3 to 6 dB, as it is given in the specification. The $HD_3$ distortion is acceptably low for the whole gain range, so this critical requirement is fulfilled. The amplifier has a high noise figure, so it cannot be positioned at the beginning of the amplifier chain, to avoid high overall noise. The most problematic property of the circuit may be its limited bandwidth and the high group delay resulting from this fact. But as this amplifier stage is used only once in the overall amplifier chain, its high group delay. The same argument can be applied to justify the elevated power consumption.

| Variable-gain amplifier | |
|---|---|
| Necessary requirements | |
| $HD_3$ | + |
| Desirable requirements | |
| $A_d$ | + |
| $B$, $\tau_g$ | ○ |
| $\lvert Z_{out}\rvert$ | + |
| Other properties | |
| $F$ | ○ |
| $P_{Diss}$ | ○ |

**Table 4.17:** Overview of the variable-gain amplifier's performances

The variable-gain amplifier works in an acceptable manner concerning the given amplifier specification.

# Chapter 5

# The overall amplifier chain

Having designed the fixed-gain and variable-gain amplifier stage, the overall amplifier chain can be conceived. Under consideration of the required properties, the single stages need to be arranged in an appropriate manner to form the chain. Then several analyses of its behaviour are completed, i.e. linearity, gain, power consumption, noise and dynamic behaviour. The methodology for these analyses is the same as for the single amplifier stages. The obtained simulation results are regarded and discussed. It is determined whether the amplifier chain can fulfil the specification.

## 5.1 Topology of the overall amplifier chain

The configuration of the overall amplifier stage is firstly determined by the required maximum voltage gain of 40 dB. Evidently, this leads to the use of six fixed-gain amplifier stages with a gain of 5.88 dB. Together with the variable-gain amplifier with a gain range from 2.95 to 5.97 dB, a gain of from 38.23 to 41.25 dB can be expected from the amplifier chain. This gain value is higher than demanded in the specification and gives margin for gain degradations due to statistical variations and high circuit temperatures. The desired gain value of 40 dB is therefore obtained with a gain control voltage lower than the maximal voltage of 150 mV. In case of non-nominal conditions the gain control voltage can be adjusted to always have the desired 40 dB.

The positioning of the different amplifier types in an amplifier chain determines the noise figure of the chain. According to Friis' formula for noise figures, low-noise amplifiers have to be the first elements of an amplifier chain, in order to obtain a low overall noise figure. The Friis formula contains the noise figures $F_n$, the power gains $G_{p_n}$ and the impedance mismatches $M_n$ for the different amplifier stages:

$$F = F_1 + \sum_{n=2}^{N} \left( \frac{F_n - 1}{\prod_{i=1}^{n-1} G_{p_i}} \cdot \frac{M_n}{M_1} \right) \tag{5.1}$$

The formula shows, that the high-noise variable-gain amplifier should be at the end of the amplifier chain. However, the amplifier's decoupling capacitors and biasing network are optimised for the designed emitter follower as their load. As the variable-gain amplifier expects the input impedance of an emitter follower at its output, it is positioned at the last but one position of the chain. The last stage is a fixed-gain amplifier, whose output is more flexible concerning load impedances than the decoupling circuit of the variable-gain amplifier.

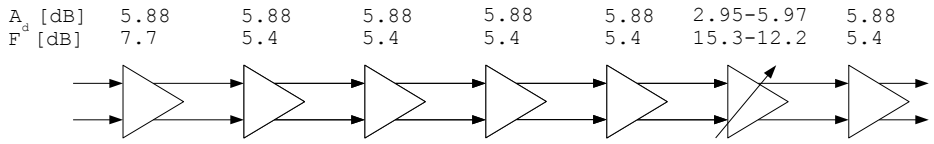


**Figure 5.1:** Amplifier chain configuration. The variable-gain amplifier stage is at the penultimate position. The differential voltage gains and noise figures of the individual stages are indicated.

With the voltage gain and noise figure simulation results of Chapter 4, the noise figure of the overall amplifier chain is calculated. It is determined whether an overall noise figure smaller than 10 dB can be obtained with the designed amplifier stages.

First the reflection coefficients $\Gamma_{\mathrm{in_n}}$ and $\Gamma_{\mathrm{out_{(n-1)}}}$ are determined, which enable the calculation of the mismatches $M_n$ at the input of the $\mathrm{n^{th}}$ amplifier stage. $\Gamma_{\mathrm{in_n}}$ stands for the input reflection coefficient of the emitter follower input buffer of the $\mathrm{n^{th}}$ amplifier stage. Simulations yield a $\Gamma_{\mathrm{in_n}}$ of $1.00156 \cdot e^{-j1.296^\circ}$. $\Gamma_{\mathrm{out_{(n-1)}}}$ is the output reflection coefficient of the preceding amplifier. Knowing its output impedance, it is calculated by

$$\Gamma_{out_{(n-1)}} = \frac{Z_{out_{(n-1)}} - 50\,\Omega}{Z_{out_{(n-1)}} + 50\,\Omega} \tag{5.2}$$

The source impedance of the first amplifier is equal to 100 Ω, so $\Gamma_{\mathrm{out_0}}$ is 0.33. For all other amplifiers the source impedance is 200 Ω, so the $\Gamma_{\mathrm{out_n}}$ for n-values from 2 to N are equal to 0.6. Knowing these reflection coefficients, the mismatches are calculated with

$$M_n = \frac{\left(1 - \left|\Gamma_{out_{(n-1)}}\right|^2\right)\left(1 - \left|\Gamma_{in_n}\right|^2\right)}{\left|1 - \Gamma_{out_{(n-1)}}\Gamma_{in_n}\right|^2} \tag{5.3}$$

The mismatch $\mathrm{M_1}$ at the first amplifier input is $-6.219 \cdot 10^{-3}$, the mismatches $\mathrm{M_2}$ to $\mathrm{M_N}$ are $-12.57 \cdot 10^{-3}$.

The power gain $\mathrm{G_p}$ is defined as the ratio between the power delivered to the load and the power consumed by the input of the amplifier. As the load impedance and the input impedance of each amplifier stage are equal, the power gain is equal to the ratio between the squared voltages at the amplifier output and input, thus the squared voltage gain.

$$G_{p_n} = A_{d_n}^2 \tag{5.4}$$

The voltage gain of the fixed-gain amplifiers is 5.88 dB. The voltage gain of the variable-gain amplifier is set to 4.72 dB to obtain 40 dB overall gain. At this gain level, this amplifier has a noise figure of 13.3 dB. Linear values are used for all variables. Having determined the values for all variables, the Friis formula is applied and yields

$$F = 8.84\,\mathrm{dB} \tag{5.5}$$

This calculation shows, that the amplifier chain structure presented in Figure 5.1 is expected to fulfil the amplifier chain's noise figure specification $\mathrm{F} < 10\,\mathrm{dB}$.

## 5.2 Analysis of the filter-less amplifier chain's performance

The filter-less amplifier chain is simulated for minimum voltage gain, a voltage gain of 40 dB and maximum voltage gain. These gains are obtained by gain control voltages equal to of 70, 90.5 and 150 mV. Apart from different $V_{Gain}$, the same simulations are done as for the variable-gain amplifier stage (Section 4.3). This includes a nominal analysis of the chain as well as an analysis under consideration of statistical variations of the circuit components.

### 5.2.1 Nominal values

| Topology | Amplifier chain | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 90.5 | 150 | 70 | 90.5 | 150 | 70 | 90.5 | 150 |
| $HD_3$ [dBc] | -84.00 | -82.21 | -81.41 | **-88.23** | **-85.40** | **-83.62** | -90.68 | -85.93 | -82.38 |
| $A_d$ [dB] @ 1.6 GHz | 39.84 | 41.03 | 41.88 | **38.45** | **40.00** | **41.46** | 37.06 | 38.83 | 40.88 |
| $B$ [GHz] | 3.575 | 3.730 | 3.871 | **3.349** | **3.493** | **3.657** | 3.118 | 3.228 | 3.417 |
| $\tau_g$ [ps] @ 1.6 GHz | 121.8 | 119.6 | 117.9 | **134.9** | **132.7** | **130.0** | 146.8 | 144.4 | 141.6 |
| $F$ [dB] @ 100 Ω | 8.1 | 8.1 | 8.1 | **8.8** | **8.8** | **8.8** | 9.5 | 9.5 | 9.5 |
| $P_{Diss}$ [mW] | 1025 | 1025 | 1025 | 1051 | 1051 | 1051 | 1074 | 1074 | 1074 |

**Table 5.1:** Results of the nominal simulation of the amplifier chain.

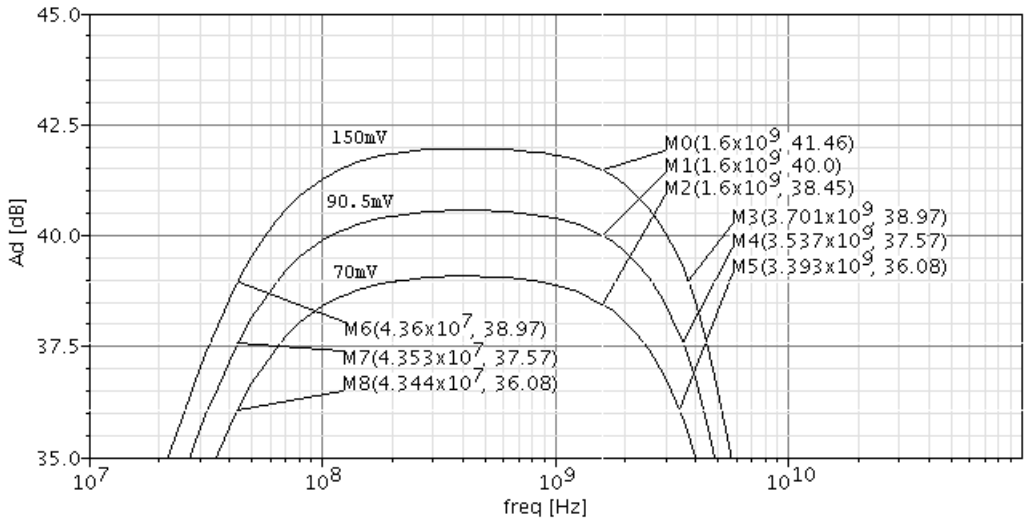


**Figure 5.2:** Nominal simulation of the amplifier chain's frequency response at room temperature. The differential voltage gain $A_d$ is plotted over the frequency axis. The gain control voltage is varied between three values. Markers $M_0$, $M_1$ and $M_2$ display the voltage gain at 1.6 GHz. Markers $M_3$, $M_4$ and $M_5$ are positioned 3 dB below maximum voltage gain and give the upper cut-off frequency of the circuit. The lower cut-off frequency is marked by $M_6$ to $M_8$.

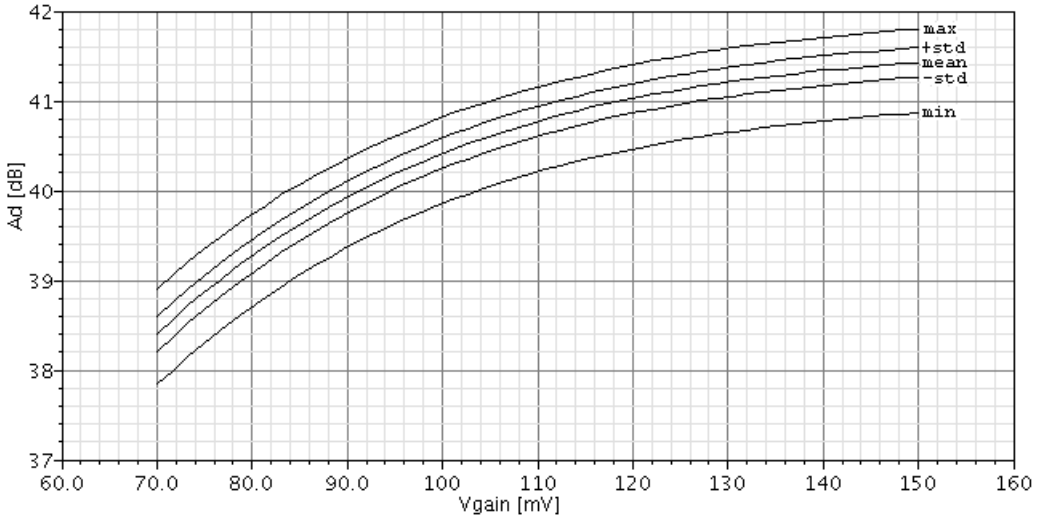


**Figure 5.3:** Statistical simulation of the differential voltage gain $A_d$ vs. gain control voltage $V_{Gain}$. Lines with the mean value, mean value plus/minus standard deviation, as well as the absolute maximum and minimum value are displayed. The simulation contains 100 trials.

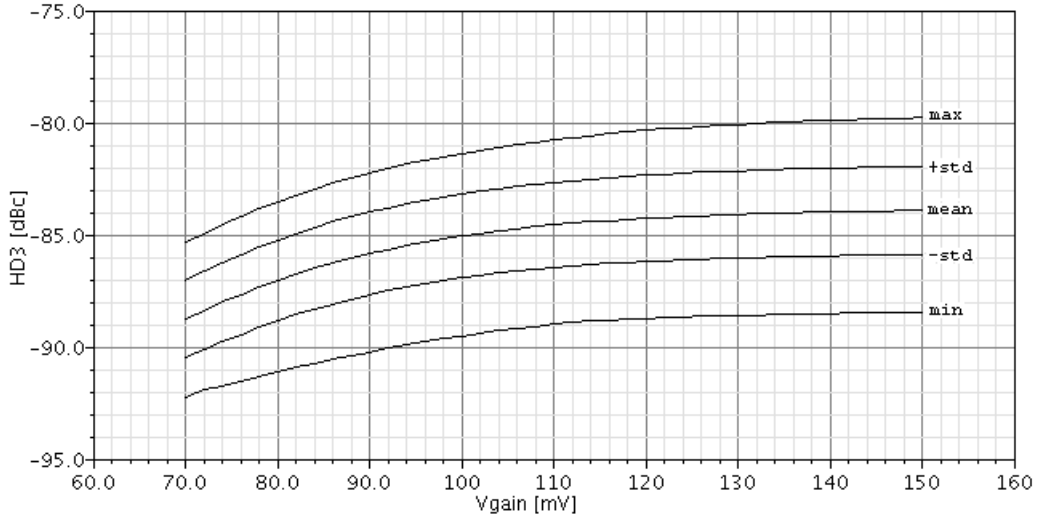


**Figure 5.4:** Statistical simulation of the third-order harmonic distortion $HD_3$ vs. gain control voltage $V_{Gain}$. Otherwise, conditions as above apply.

### 5.2.2 Statistical analysis

#### Third-order harmonic distortion

| $HD_3$ [dBc] | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Topology | Amplifier chain | | | | | | | | |
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 90.5 | 150 | 70 | 90.5 | 150 | 70 | 90.5 | 150 |
| $\mu$ | 84.29 | -82.49 | -81.67 | **-88.87** | **-85.88** | **-84.07** | -91.07 | -86.31 | -82.68 |
| $\sigma$ | 1.21 | 1.28 | 1.46 | **1.76** | **1.85** | **1.96** | 2.63 | 2.19 | 1.98 |
| min. | -88.73 | -87.29 | -86.98 | **-94.41** | **-92.81** | **-90.70** | -101.5 | -93.83 | -89.43 |
| max. | -81.83 | -79.84 | -78.72 | **-84.93** | **-81.91** | **-79.78** | -86.34 | -82.34 | -78.93 |
| $> -80$ dBc [%] | 0.0 | 0.8 | 2.3 | **0.0** | **0.0** | **0.3** | 0.0 | 0.0 | 2.1 |

**Table 5.2:** Statistical simulation of the third-order harmonic distortion of the amplifier chain. Histograms with the statistical distribution of the $HD_3$ value for room temperature conditions are shown in Annex C.2.

#### Voltage gain

| $A_d$ [dB] @ 1.6 GHz | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Topology | Amplifier chain | | | | | | | | |
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 90.5 | 150 | 70 | 90.5 | 150 | 70 | 90.5 | 150 |
| $\mu$ | 39.81 | 40.98 | 41.86 | **38.40** | **39.94** | **41.43** | 36.96 | 38.75 | 40.81 |
| $\sigma$ | 0.16 | 0.15 | 0.14 | **0.23** | **0.19** | **0.18** | 0.29 | 0.27 | 0.23 |
| min. | 39.42 | 40.66 | 41.48 | **37.71** | **39.36** | **40.84** | 35.99 | 37.92 | 40.23 |
| max. | 40.29 | 41.37 | 42.20 | **38.85** | **40.47** | **41.74** | 37.47 | 39.42 | 41.20 |

**Table 5.3:** Statistical simulation of the voltage gain of the amplifier chain.

#### Bandwidth

| $B$ [GHz] | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Topology | Amplifier chain | | | | | | | | |
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 90.5 | 150 | 70 | 90.5 | 150 | 70 | 90.5 | 150 |
| $\mu$ | 3.591 | 3.747 | 3.885 | **3.328** | **3.466** | **3.642** | 3.132 | 3.244 | 3.431 |
| $\sigma$ | 0.193 | 0.206 | 0.219 | **0.180** | **0.191** | **0.207** | 0.171 | 0.179 | 0.196 |
| min. | 3.172 | 3.297 | 3.414 | **2.942** | **3.058** | **3.201** | 2.772 | 2.862 | 3.021 |
| max. | 4.125 | 4.307 | 4.473 | **3.819** | **3.984** | **4.180** | 3.586 | 3.709 | 3.951 |

**Table 5.4:** Statistical simulation of the 3 dB-bandwidth of the amplifier chain.

### Group delay

| $\tau_g$ [ps] @ 1.6 GHz | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Topology | Amplifier chain | | | | | | | | |
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 90.5 | 150 | 70 | 90.5 | 150 | 70 | 90.5 | 150 |
| $\mu$ | 119.9 | 118.0 | 116.2 | **134.9** | **130.9** | **130.1** | 146.7 | 142.8 | 141.5 |
| $\sigma$ | 5.7 | 5.7 | 5.7 | **6.4** | **6.3** | **6.4** | 7.0 | 6.9 | 6.9 |
| min. | 105.9 | 104.0 | 102.4 | **119.4** | **115.6** | **114.7** | 129.7 | 126.2 | 124.4 |
| max. | 131.8 | 129.0 | 128.1 | **148.3** | **143.9** | **143.3** | 160.7 | 156.8 | 155.4 |

**Table 5.5:** Statistical simulation of the group delay of the amplifier chain.

### Noise figure

| $F$ [dB] @ 50 Ω | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Topology | Amplifier chain | | | | | | | | |
| Temperature [°C] | −20 | | | 27 | | | 70 | | |
| $V_{Gain}$ [mV] | 70 | 90.5 | 150 | 70 | 90.5 | 150 | 70 | 90.5 | 150 |
| $\mu$ | 10.81 | 10.80 | 10.80 | **11.60** | **11.58** | **11.57** | 12.24 | 12.24 | 12.27 |
| $\sigma$ | 0.11 | 0.10 | 0.10 | **0.11** | **0.11** | **0.12** | 0.12 | 0.12 | 0.11 |
| min. | 10.56 | 10.55 | 10.55 | **11.35** | **11.33** | **11.32** | 12.00 | 11.96 | 11.95 |
| max. | 11.03 | 11.03 | 11.02 | **11.83** | **11.81** | **11.80** | 12.51 | 12.48 | 12.47 |

**Table 5.6:** Statistical simulation of the noise figure of the amplifier chain.

### 5.2.3 Performance analysis summary

#### Third-order harmonic distortion

Under nominal conditions, the $HD_3$ measure is always lower than the $-80\,dBc$ limit. Statistical simulations show a quite high standard deviation value. Due to this statistical spread, at low and high temperatures more than 1% of the simulated cases have distortions. However, at room temperature this rate is at only 0.3%. As the analysis under extreme temperatures only has minor relevance, the linearity requirement is fulfiled.

#### Differential voltage gain

The differential voltage gain of the complete chain can be varied between 38.45 and 41.46 dB by varying the voltage gain from 70 to 150 mV. The desired gain value of 40.00 dB is obtained for a gain control voltage of 90.5 mV.
Higher temperature leads to lower gain, and the statistical variation of circuit components leads to a gain uncertainty of about $\pm 0.5\,dB$. These two factors combined yield a highest minimum gain of 40.29 dB and a lowest maximum gain of 40.23 dB, as Figure 5.3 shows. The lowest maximum gain does not pose problems, as the desired 40 dB can be obtained by reducing the gain voltage from its maximum level of 150 mV. The highest minimum gain occurs at low temperature, because under this condition the circuit has increased gain. At 70 mV gain control voltage, the voltage gain is equal to 40.29 dB. This means, that $V_{Gain}$ has to be slightly lower than the lowest specified value to obtain the desired voltage gain. However, this does not lead to operation problems.

#### Speed performance

The group delay of the chain varies between the maximum values 102.4 and 160.7 ps. With variations of about 5 ps, there is a slight dependence of the group delay on gain variation. The obtained delay is however definitely lower than the stringent 180 ps limit.

#### Noise figure

Simulations show that with 8.8 dB the noise figure of the overall chain is appoximately equal to the value calculated before (Formula 5.5). It is virtually non-dependent on the gain. The influence of the rising noise figure of the variable-gain amplifier due to a gain lower than the maximum value is not high enough to strongly influence the overall noise figure. High temperature increases the noise figure up to 9.5 dB. However, it always stays below the limit of 10 dB.

#### Power consumption

With approximately 1.05 W, the power consumption is at the limit of the acceptable range.

### 5.2.4 Specification conformity of the amplifier chain

Simulations have shown that the third-order distortion of the amplifier chain is sufficiently low over the whole gain range. Even with statistical variations, the −80 dBc limit is hardly ever exceeded. The gain of the amplifier chain can reliably be fixed to 40 dB. By varying the gain control voltage, this desired value can always be obtained, even under performance degradation due to statistical variations and temperature influence. The group delay requirement is also met, as the $\tau_g$ at the operation frequency is never higher than 180 ps. As the noisy variable-gain amplifier is at the rear part of the chain, the overall noise figure is always smaller than 10 dB. Thus, this last requirement is also fulfilled.

| Amplifier chain | |
|---|---|
| Necessary requirements | |
| $HD_3$ | + |
| $A_d$ | + |
| $\tau_g$ | + |
| $F$ | + |
| Other properties | |
| $P_{Diss}$ | ○ |

**Table 5.7:** Overview of the amplifier chain's performances

The amplifier chain completely complies to the given specifications.

# Chapter 6

# Conclusion and extensions

## 6.1 Conclusion

This thesis described the design of the schematics of a highly linear amplifier chain, which is part of a high-performance delta-sigma analogue-to-digital converter. Requirements for this chain are not only low non-linear distortion, but also high gain, low group delay and low noise. The amplifier chain is expected to reliably fulfil these requirements, even under consideration of statistical component variations due to the manufacturing process.

Based on a research of previously developed differential RF amplifiers, an overview was given of fixed-gain and variable-gain amplifier topologies. In particular, their linearity properties were analysed and eventual mechanisms for the compensation of non-linearities were described. With the help of the thereby identified topology properties and additional simulations, the emitter-coupled pair with diode-connected load and the compensated cascode were identified as the best performing fixed-gain amplifier topologies. In contrast to the fixed-gain topologies, there does not exist a wide range of variable-gain topologies, the Gilbert cell was the only viable choice for this part of the amplifier chain. Its linearity was increased by using a compensated cascode as its signal amplification stage.

The design process resulting in the schematics for these three amplifier topologies was described in detail. A key element to consider was the appropriate biasing of the used bipolar transistors. High collector currents and high collector-emitter voltages were necessary to obtain sufficiently linear transistor behaviour. However, while the circuits were optimised for linearity, no less importance was given to the other necessary requirements. The right choice of the contact configurations of the circuits' transistors lead to viable compromises between the circuits' bandwidths and noise performances. For all circuits K-factor stability analyses were done to avoid unstable behaviour.

Extensive simulations of the amplifier stages were made in order to be able to choose between the two designed fixed-gain amplifiers. These simulations showed that the emitter-coupled pair with charge diodes is the most appropriate choice for the given problem. The compensated cascode is not sufficiently linear, and in addition has low bandwidth and a high noise figure. Apart from the fixed-gain amplifiers, the compliance of the the Gilbert cell to the desired specification was also investigated.

As the result from these design and analysis steps, the following amplifiers were conceived and comply to the desired specification:

- Fixed-gain amplifier:
  Emitter-coupled pair with diode-connected load
- Variable-gain amplifier:
  Gilbert cell with a compensated cascode as its signal amplification stage

After having designed the single amplifier stages, they were cascaded to the overall amplifier chain. Putting the variable-gain amplifier on the penultimate position yielded the lowest possible noise figure. Except for the variable-gain amplifier, no additional interstage coupling elements were necessary. Finally, simulations as for the single amplifier stages were executed to verify the chain's specification compliance.

Both the amplifier stages and the overall amplifier chain, which were designed in this thesis, meet the stringent specifications given by the contracting semiconductor company. It was therefore possible to participate in the development of a delta-sigma converter by delivering the schemas of the circuits of one of its major subsystems.

## 6.2 Future research steps

- Transistor model accuracy:
  For this work it has been assumed that the transistor model is sufficiently accurate to be used to simulate highly linear circuits with a difference of more than 80 dBc between the signals' first and third harmonics. If not, it is expected that the linearity maxima obtained by the design process will subsist, but the absolute $HD_3$ may differ by several dB. It should be verified in practice, that the transistor models are sufficiently accurate.

- Amplifier chain filters:
  Unfortunately the amplifier chain's bandpass filters were not available for this work, but the filters may have an influence on the amplifiers' linearity performances. It is advisable to resimulate the overall amplifier chain with added filters, considering the third-order intercept point as an additional linearity measure.

- Amplifier stability and layout:
  Even if stability analyses were made in this work by using the classical K-factor approach, the author's successor in the framework of this project will perform further work on the stability aspect. The nonlinear determinant function (NDF) method presented by Mons [37] provides a robust stability analysis method for circuits with multiple active components. This method considers possibly unstable internal loops, which cannot be detected by simply analysing the circuit at its input and output ports.
  Having ensured stable behaviour, the amplifier chain will be laid out and the properties of the transmission lines between the circuit components will be determined.
  Finally the NDF analysis will be executed once more under consideration of the transmission lines to definitely guarantee the circuits' stability.

- Practical measurements:
  Only testing a fabricated prototype will definitely approve the correct functionality of the designed amplifier chain.

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# Appendices

# Appendix A

# Transistor output characteristics

This annex chapter contains the $V_{ce}$-$I_c$ curves of all used transistors. The amplifiers are simulated for the maximum output voltage swing of 600 mV. As the emitter follower circuit is identical for all amplifiers, it is only plotted once.

## A.1 Emitter follower

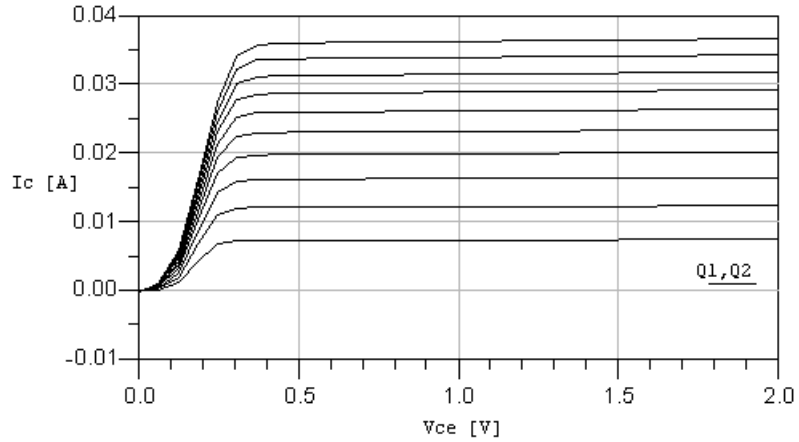


**Figure A.1:** Output characteristics of the emitter follower transistors $Q_1$ and $Q_2$. The according circuit schematic is shown in Figure 3.4.

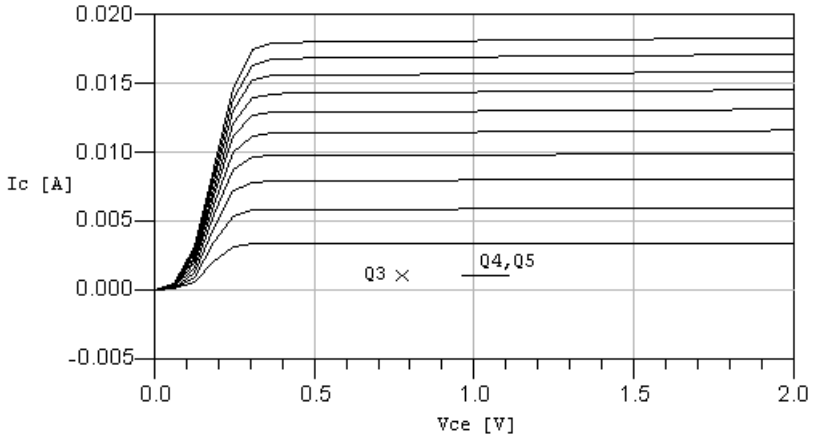


**Figure A.2:** Output characteristics of the emitter follower's current mirror transistors.

## A.2 Emitter-coupled pair with diode-connected load

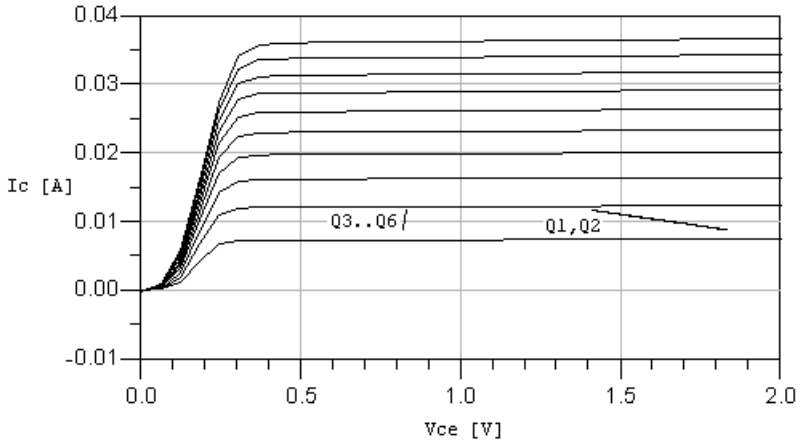


**Figure A.3:** Output characteristics of the transistors of the emitter-coupled pair with diode-connected load. $Q_1$ and $Q_2$ are the principal transistors of the gain stage, $Q_3$ to $Q_6$ the transistors in diode connection. The according circuit schematic is shown in Figure 3.6.

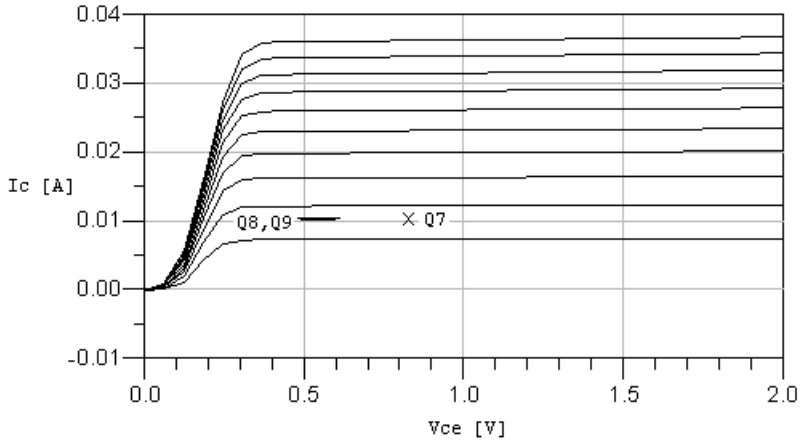


**Figure A.4:** Output characteristics of the emitter-coupled pair's current mirror transistors.

## A.3 Compensated cascode

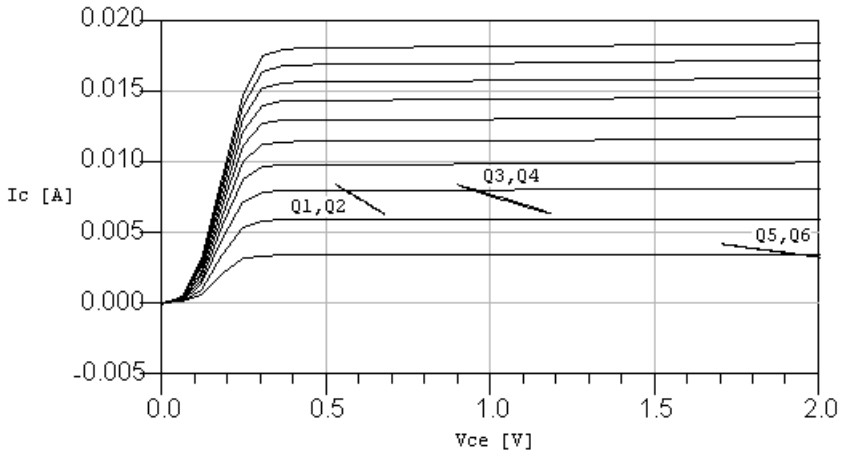


**Figure A.5:** Output characteristics of the transistors of the compensated cascode. $Q_1$ and $Q_2$ are the principal transistors of the gain stage, $Q_3$ and $Q_4$ the cascode transistors, $Q_5$ and $Q_6$ the transistors of the compensation amplifier. The according circuit schematic is shown in Figure 3.11.

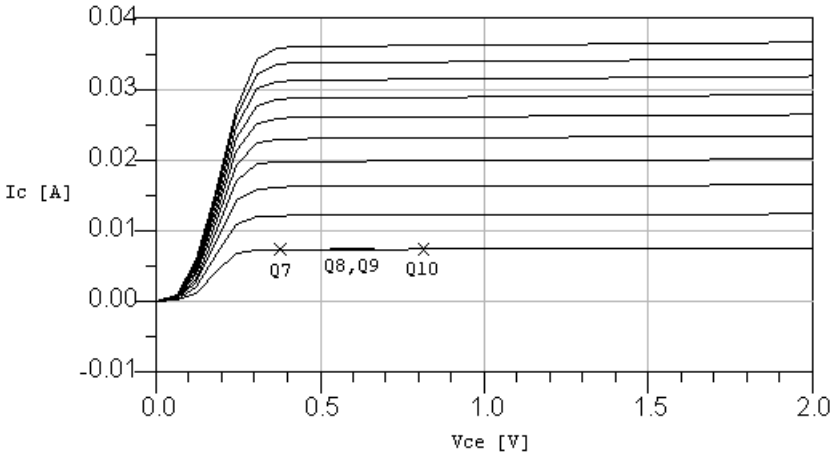


**Figure A.6:** Output characteristics of the compensated cascode's current mirror transistors.

## A.4 Gilbert cell

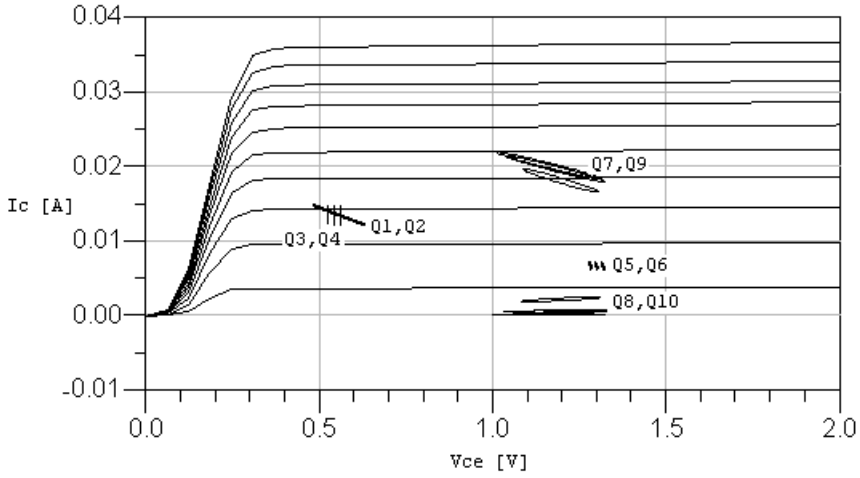


**Figure A.7:** Output characteristics of the transistors of the variable-gain amplifier. $Q_1$ and $Q_2$ are the principal transistors of the signal amplification stage, $Q_3$ and $Q_4$ the cascode transistors, $Q_5$ and $Q_6$ the transistors of the compensation amplifier, and $Q_7$ to $Q_{10}$ the transistors of the gain variation stage. The according circuit schematic is shown in Figure 3.18.

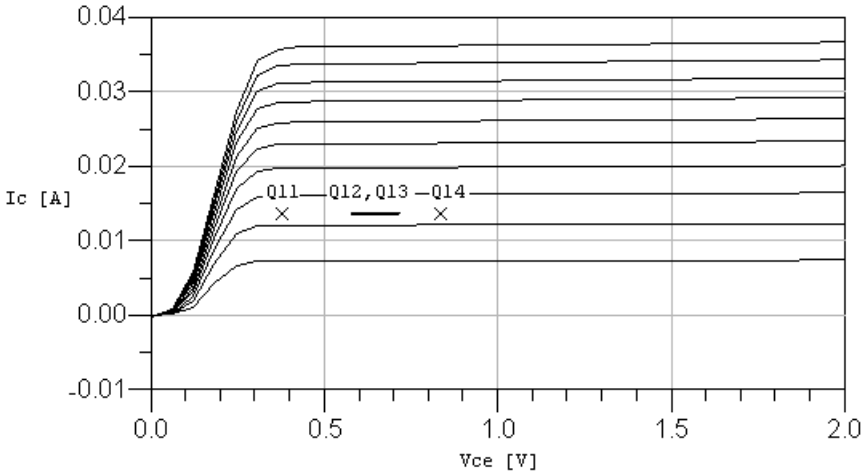


**Figure A.8:** Output characteristics of the Gilbert cell's current mirror transistors.

# Appendix B

# Simulation results for the amplifier stages

This annex chapter contains additional plots of nominal and statistical simulation results concerning the amplifier stages.

## B.1 Fixed-gain amplifiers

### B.1.1 Nominal simulation results

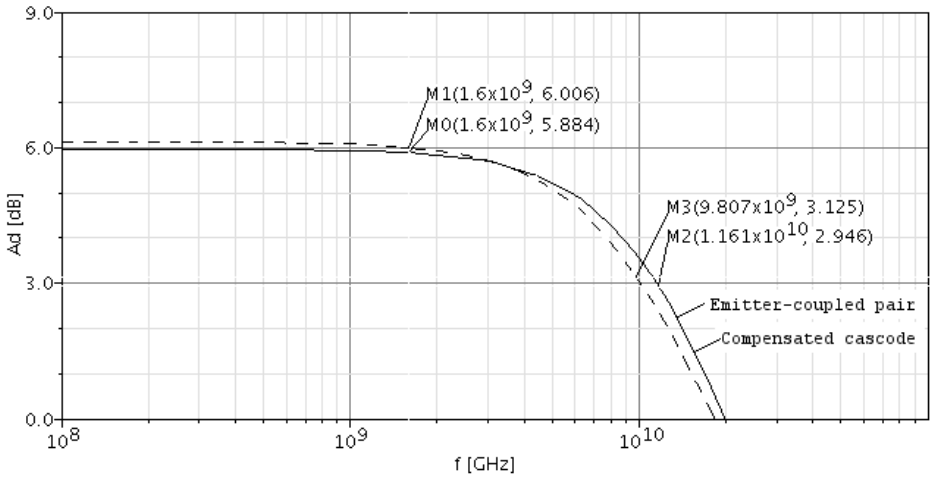


**Figure B.1:** Nominal simulation of the fixed-gain amplifiers' frequency response at room temperature. The differential voltage gain $A_d$ is plotted over the frequency axis. Markers $M_0$ and $M_1$ display the voltage gain at 1.6 GHz. Markers $M_2$ and $M_3$ are positioned 3 dB below maximum voltage gain and give the bandwidth of the circuit.

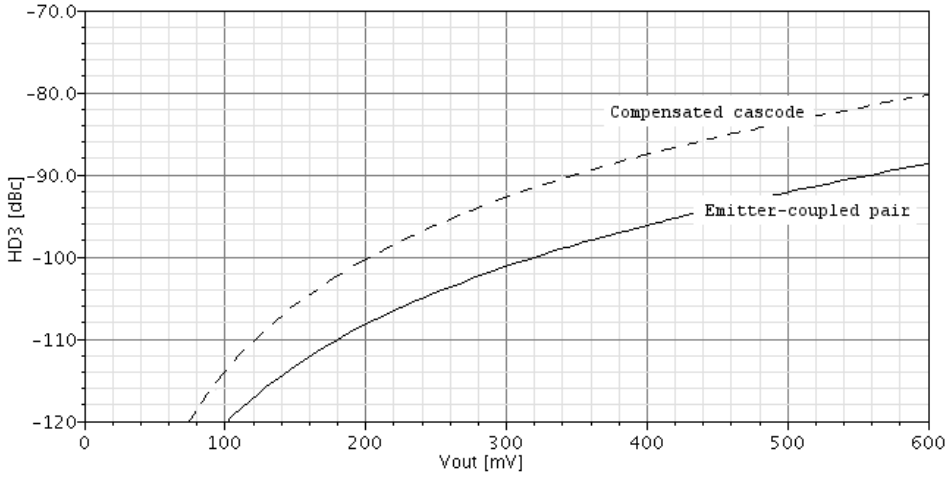


**Figure B.2:** Nominal simulation of the fixed-gain amplifiers' third-order harmonic distortion $HD_3$ vs. output voltage $V_{Out}$ for room temperature conditions.

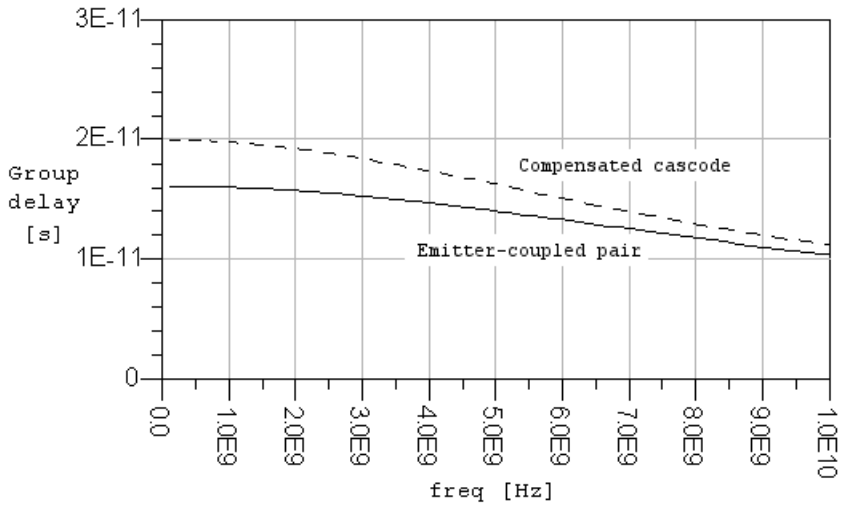


**Figure B.3:** Nominal simulation of the fixed-gain amplifiers' group delay $\tau_g$ vs. frequency for room temperature conditions.

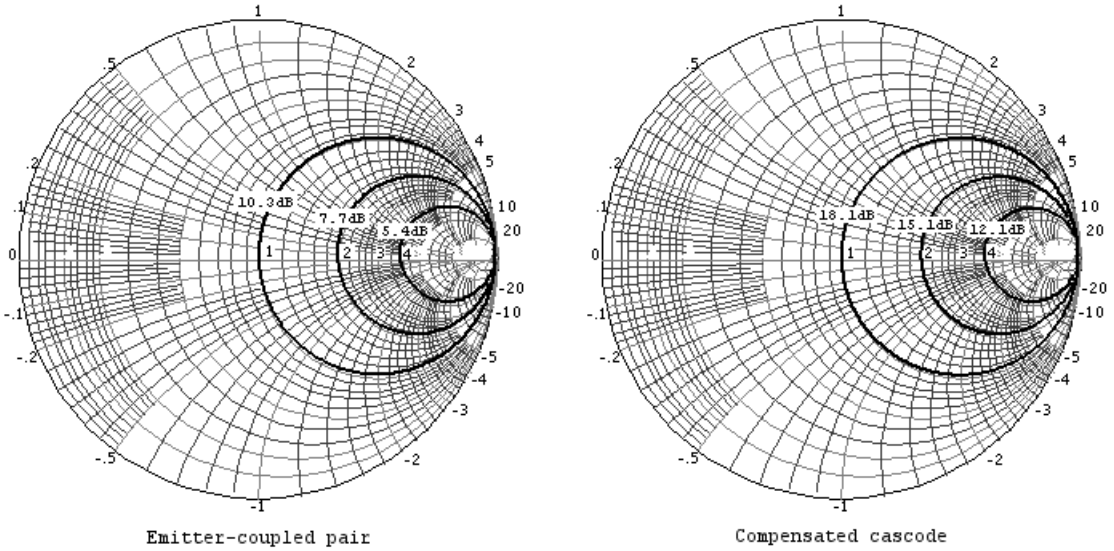


**Figure B.4:** Nominal simulation of the fixed-gain amplifiers' circles of constant noise figure for room temperature conditions. The circles cross the real axis at resistances of 50, 100 and 200 Ω.

### B.1.2 Statistical variation of the third-order distortion

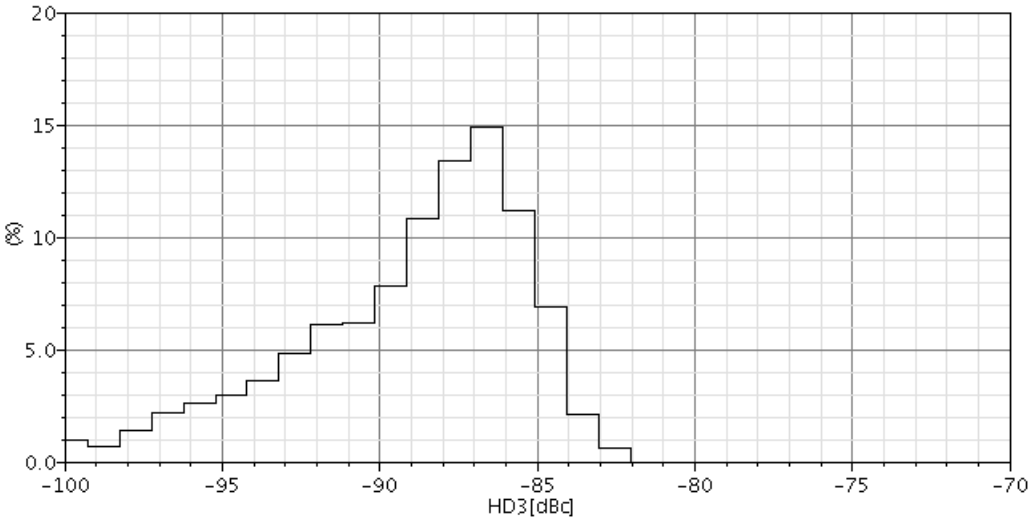


**Figure B.5:** Histogram of the third-order harmonic distortion of the emitter-coupled pair with charge diodes. Room temperature conditions are applied.

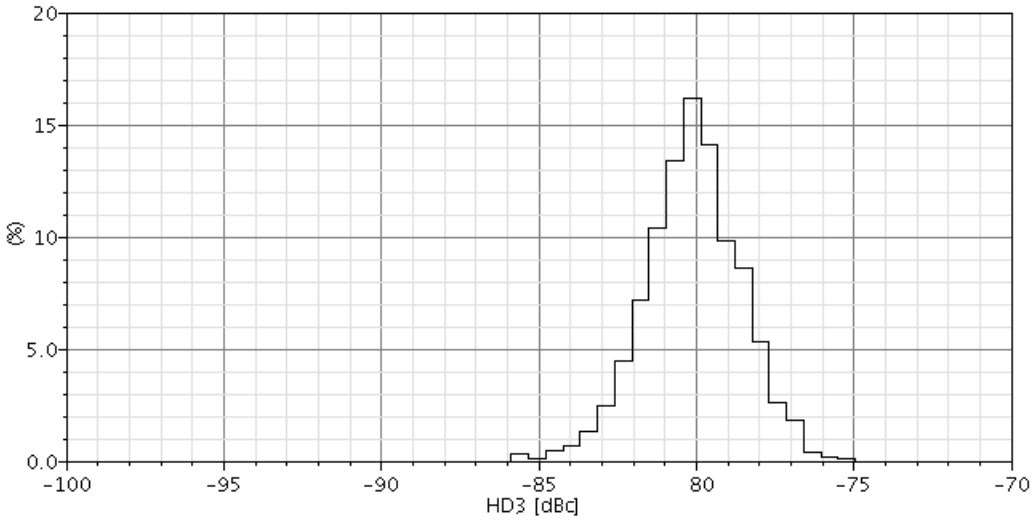


**Figure B.6:** Histogram of the third-order harmonic distortion of the compensated cascode. Room temperature conditions are applied.

## B.2 Variable-gain amplifier

### B.2.1 Nominal simulation results

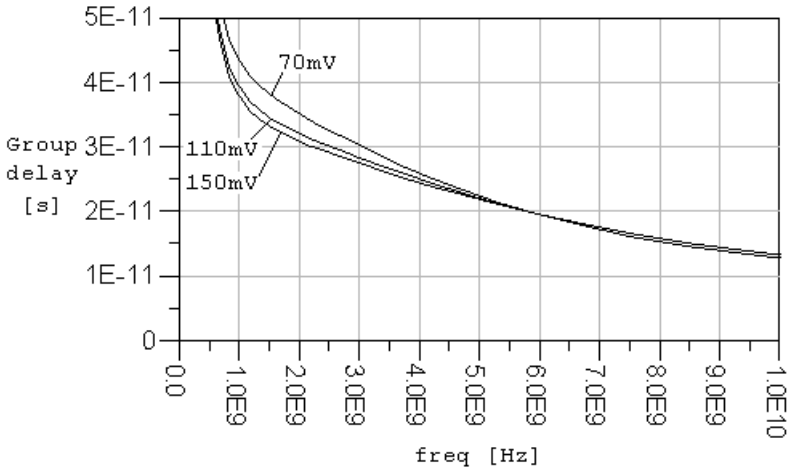


**Figure B.7:** Nominal simulation of the variable-gain amplifier's group delay $\tau_g$ vs. frequency for room temperature conditions. The gain control voltages 70, 110 and 150 mV are applied to the circuit.

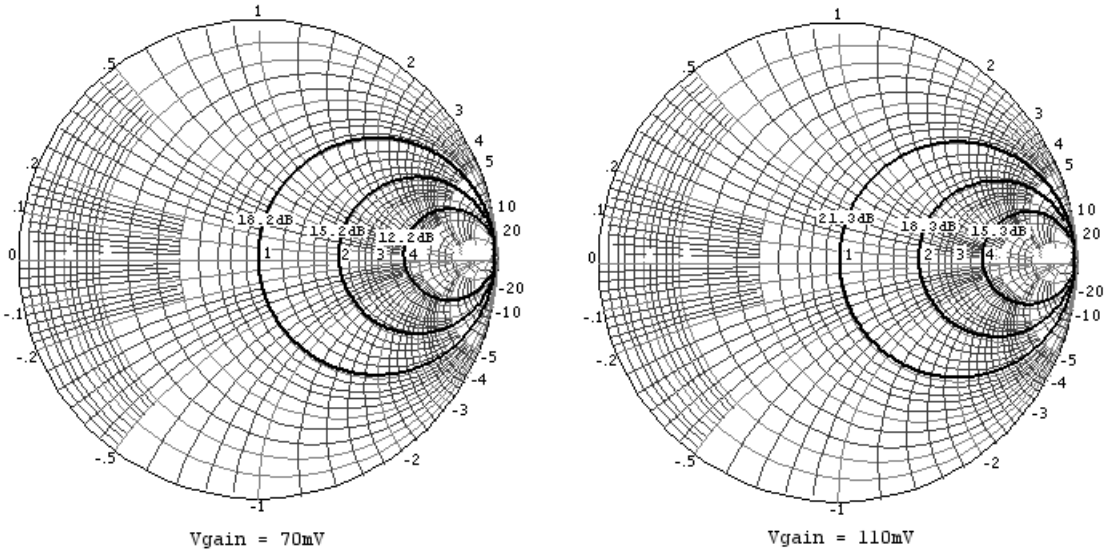


**Figure B.8:** Nominal simulation of the variable-gain amplifier's circles of constant noise figure for room temperature conditions. The circles cross the real axis at resistances of 50, 100 and 200 Ω. The gain control voltages 70 and 150 mV are applied to the circuit.

### B.2.2 Statistical variation of the third-order distortion

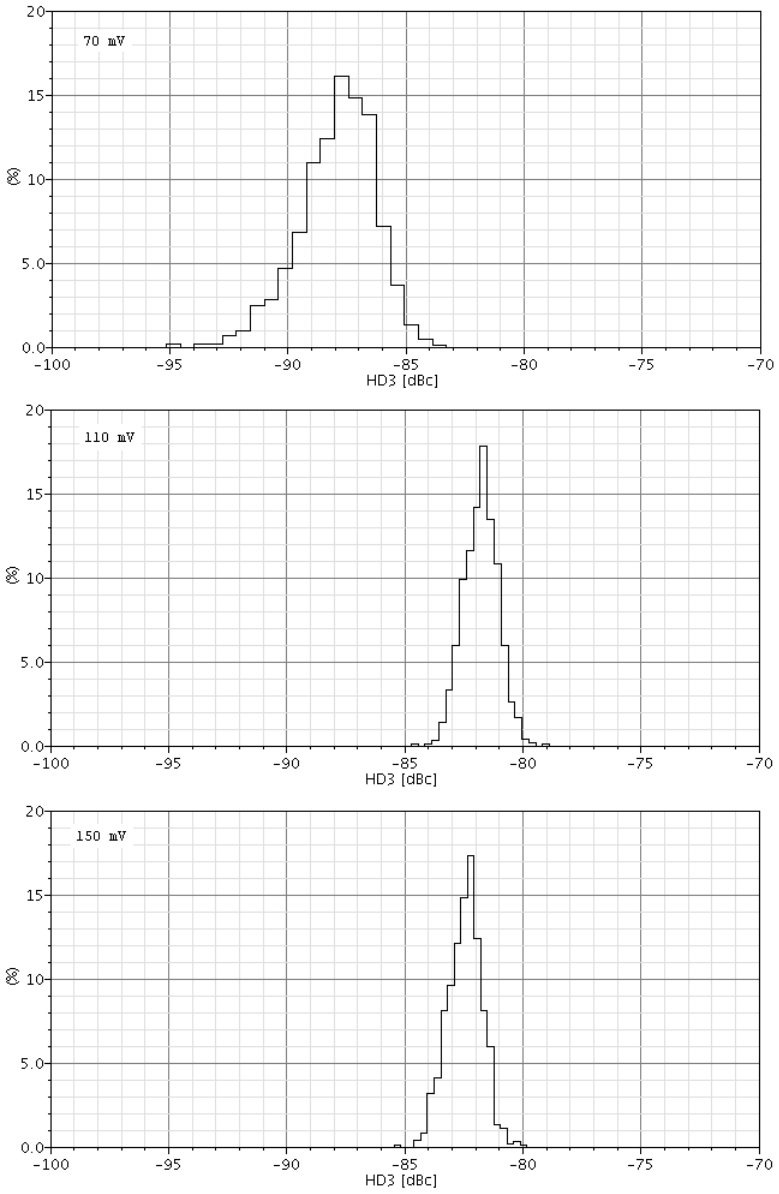


**Figure B.9:** Histogram of the third-order harmonic distortion of the variable-gain amplifier for room temperature. The gain control voltages 70, 110 and 150 mV are applied to the circuit.

# Appendix C

# Simulation results for the overall amplifier chain

This annex chapter contains additional plots of nominal and statistical simulation results concerning the overall amplifier chain.

## C.1 Nominal simulation results

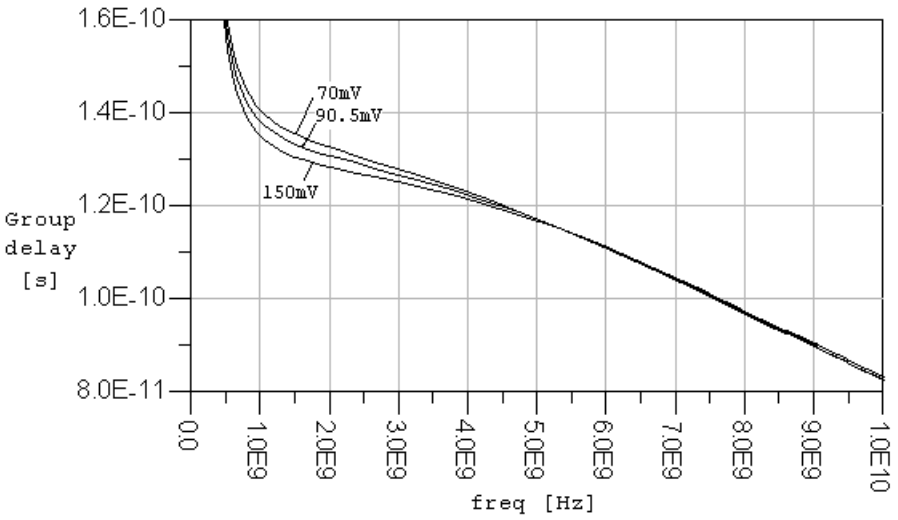


**Figure C.1:** Nominal simulation of the amplifier chain's group delay $\tau_g$ vs. frequency for room temperature conditions. The gain control voltages 70, 110 and 150 mV are applied to the circuit.

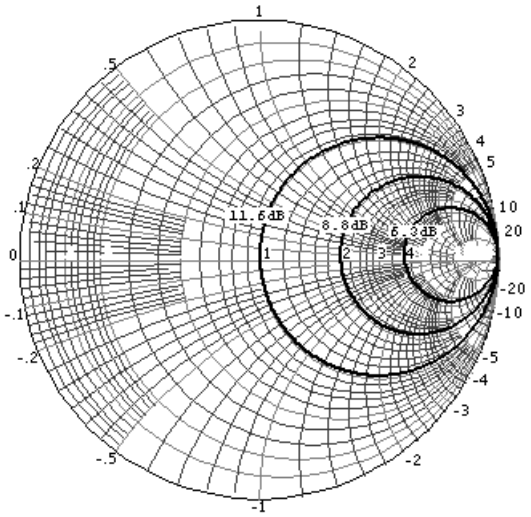


**Figure C.2:** Nominal simulation of the amplifier chain's circles of constant noise figure for room temperature conditions. The circles cross the real axis at resistances of 50, 100 and 200 Ω.

## C.2 Statistical variation of the third-order distortion

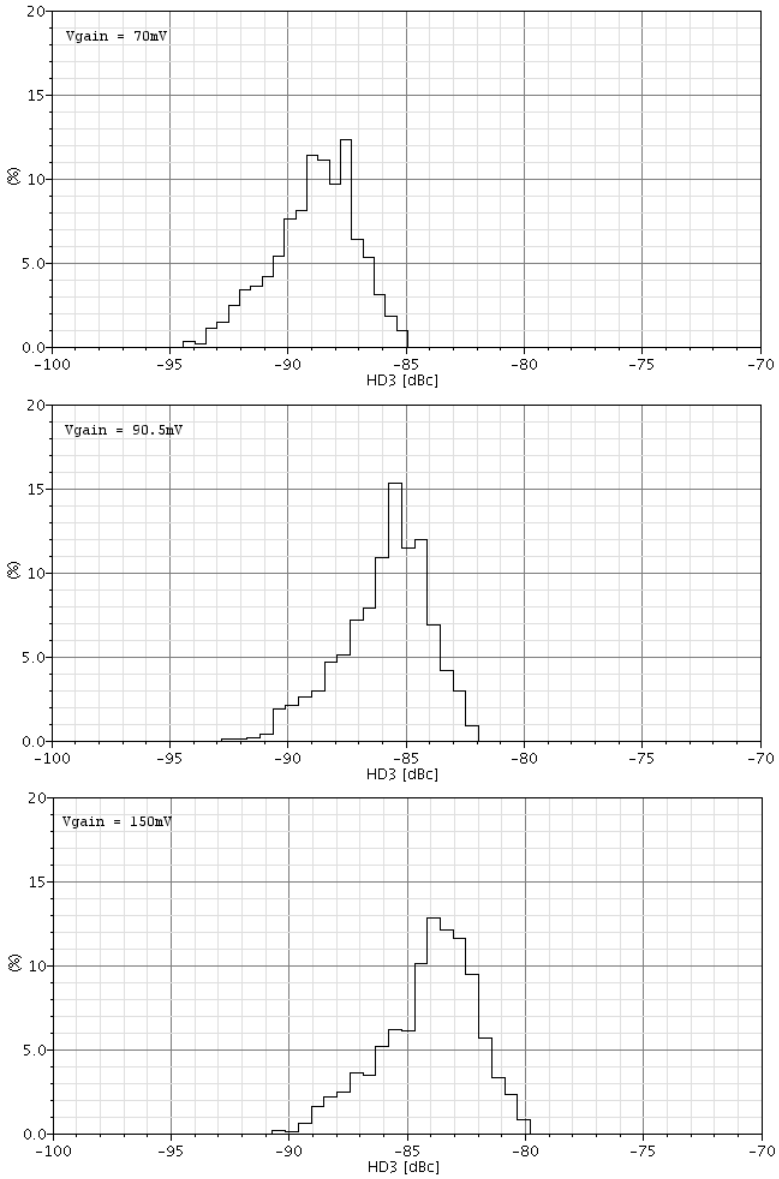


**Figure C.3:** Histogram of the third-order harmonic distortion of the amplifier chain. Room temperature conditions are applied.