Thomas Obermüller

Temperature dependent Bias-Stress Measurements on Organic Thin Film Transistors

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Abstract for
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Temperature dependent Bias-Stress Measurements on Organic Thin Film Transistors

Thomas Obermüller
Institute of Solid State Physics, University of Technology, Graz
8010 Graz, Austria

In the present work, bias stress effects in pentacene organic thin film transistors in top contact, bottom gate device configuration are investigated. While there are numerous works on the occurrence of a threshold shift in current literature, detailed descriptions and explanations of the impacts on other parameters, such as the mobility or the contact resistance, are rare. In order to monitor all crucial device parameters, transistors of two different channel length have been exposed to constant gate bias stress, which has been interrupted in equidistant time steps for transfer characteristics measurements. Various parameter extraction methods which have been present in literature are critically evaluated and their reliability is tested. Furthermore, the bias stress measurements have also been performed at a temperature of 200K.
From the measurements it can be concluded that, firstly, both mobility and threshold voltage change under bias stress and, secondly, that the effect decreases with decreasing temperature. Additionally, the appearance of inverted hysteresis at low temperatures has been investigated and can be explained by the dynamics of channel formation in the transistors.

Abstrakt
Diplomarbeit

Temperaturabhängige Bias-Stress Messungen an organischen Dünnschichttransistoren

Thomas Obermüller
Institut für Festkörperphysik, Technische Universität Graz
8010 Graz, Austria

Das Ziel der vorliegenden Arbeit war die Untersuchung von "Bias-Stress" Effekten in auf Pentacen basierenden organischen Dünnschicht-Transistoren. Der Schwerpunkt der Arbeit lag dabei in der Untersuchung und experimentellen Beschreibung der zeitlichen Entwicklung von Größen wie Ladungsträgermobilität und Kontaktwiderstand von Bauelementen im Betrieb. Während die Verschiebung der Schwellspannung im Betrieb der Bauteile in der Literatur schon ausführlich diskutiert wurde, wurde die Auswirkung auf die oben genannten Größen bisher kaum diskutiert. Um das zeitliche verhalten von Kontaktwiderstand und Ladungsträgermobilität zu studieren wurden Transistoren mit zwei unterschiedlicher Kanallängen bei Raumtemperatur unter bei konstantem "Bias-Stress" vermessen. Dieser musste für die Messung der Transfer-Charakteristiken in äquidistanten Zeitintervallen unterbrochen werden. Die mannigfaltigen in der Literatur beschrieben Methoden zur Auswertung der Transistorkennlinien wurden in dieser Arbeit auf ihre Verlässlichkeit und Aussagekraft hin überprüft. In den oben beschriebenen Experimenten wurde nicht nur eine Verschiebung der Schwellspannung sondern auch eine Änderung der Ladungsträgermobilität beobachtet. Weiters wurde eine Abnahme der beobachteten Effekte bei einer Temperatur von 200K festgestellt. Darüber hinaus wurde die häufig beobachtet Umkehr der Hysterese bei tiefen Temperaturen erklärt.

Contents

1. Introduction

The invention of field effect transistors in the first half of the past century has changed our daily life in a way that is comparable to other great technological inventions of mankind like the wheel or the combustion engine. At this time, computers driven by the cathode ray tube filled entire halls, were extremely expensive and very limited in their performance and speed. But the new metal-oxide-semiconductor field-effect-transistor (MOSFET) allowed scientist to design smaller, faster and cheaper computers. Since them, computers have infiltrated almost all everyday devices and became omnipresent in our environment. But at the beginning of the century a new invention revolutionized again our daily life, the Internet. It connects people via the cyber space to any imaginable thing, provides access to an incredible amount of information and collects any kind of information in data bases. This changes are often called the digital revolution. Through that the computerization of our world reached a degree that engineers and visionaries consider to equip also the simplest things in our life with electronic devices, such as food packages and clothes. Here the technology of conventional semiconductors reached its limits. Therefore, the alternative technology of organic semiconductors have gained interests. Organic semiconductors have properties which would fulfill these new requirements, such as light weight, flexibility and low cost of fabrication. Additionally, they would allow for new applications. For example, organic electronic circuits can be printed by commercial ink-jet printers.

In recent years, great progress has been made in the field of organic electronics. However, there are still unsolved problems which limit their practical applicability, namely low mobility, large contact resistance and bias stress effects. The latter result in electronic properties changing with operation time. The reasons for bias stress effects have not yet been fully understood. Thus, the investigation of its temperature dependence could provide an improved insight into the underlying microscopic origins.

In the first part of this work, general aspects regarding the operation of field effect transistors are presented. Difference between the MOSFETs and the organic thin-film transistors are pointed out and charge transport in organic materials is discussed.

The second part introduces and discusses the know parameter extraction methods present in the literature. Additionally, a reliable algorithm for parameter extraction is developed.

In the finial part, possible bias stress phenomena are studied in detail and the obtained measurement results are presented and discussed. A measurement routine for exploring bias stress phenomena is developed and applied. Measurements are performed at room temperature as well as at low temperatures.

Part I.

General Aspects

2. Basic concepts

In this chapter, the most important physical fundamentals of a field-effect transistor are discussed. In the first part, the charge carrier mobility and the schematic structure of an organic field-effect-transistor are introduced. In the last part, a short derivation of the basic device characteristic is presented.

2.1. Charge Carrier Mobility

The mobility of charge carriers is of particular interest in semiconductor physics. For a crystalline material, it is largely determined by phonon-electron and electron-dopant scattering, which is again determined by the basic properties of the atomic and lattice structure. In the case of organic materials more complex models are needed to describe charge transport and, as a consequence the number of quantities increases that mobility depends on. Therefore, it is worth including a short derivation of the mobility from a classical point of view.

The classical definition of the current density is given by the following equation

$$\vec{j} = nq\vec{v_d} \tag{2.1}$$

where n is the charge carrier density, q the elementary charge and v_d the average drift velocity. On the other hand the vectorial ohmic law is

$$\vec{j} = \sigma\vec{E} \tag{2.2}$$

where σ is the conductivity and E the electric field. When we combine equation 2.1 and equation 2.2, we come to the expression

$$\sigma = nq\frac{|\vec{v_d}|}{|\vec{E}|} = nq\mu \tag{2.3}$$

where μ is the carrier mobility. As we can see, the charge carrier mobility is the ratio of average drift velocity and the applied electric field.

$$\mu = \frac{|\vec{v_d}|}{|\vec{E}|} \tag{2.4}$$

This is a macroscopic quantity and consequently it can be measured easily. However, it is very important for identifying transport mechanism.

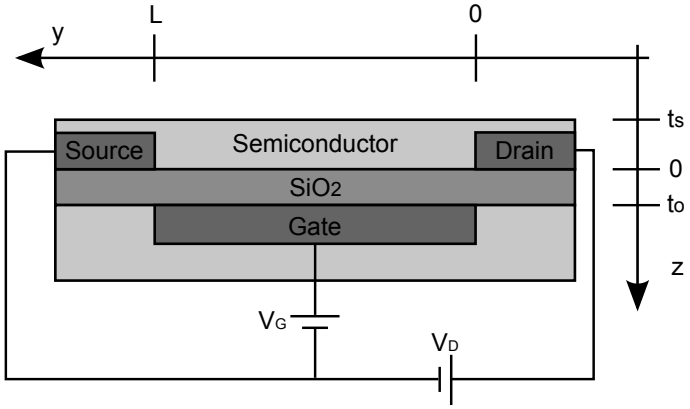


Figure 2.1.: Schematic structure of an field-effect transistor and applied voltages: L = channel length, t_s = semiconductor thickness, t_o = oxide thickness, V_G = Voltage between source and gate, V_D = Voltage between source and drain

2.2. Schematic Structure of an Organic Thin Film transistor

In Figure 2.1 all components which an organic thin film transistor requires are shown: a semiconducting layer of thickness t_s, which is separated from the gate electrode by an insulating layer of thickness t_o. Source and Drain electrodes need to be in contact with the semiconductor and must be insulated from the gate as well. The distance between source and drain is called the channel length L and perpendicular to it, the size of the electrodes is called the channel width W. The channel length is normally much smaller than the channel width.

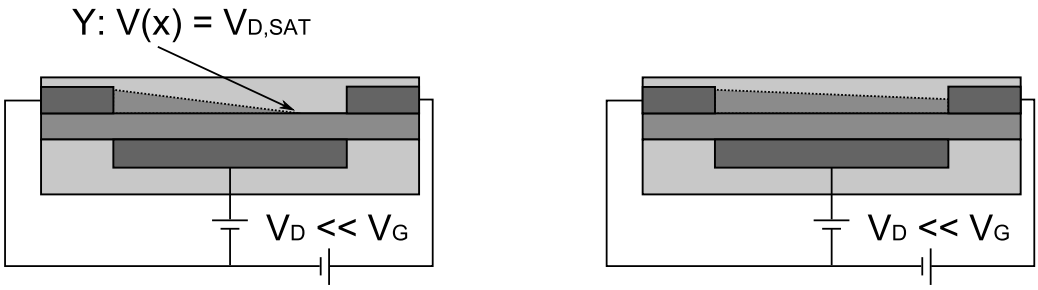
Usually, the source electrode is grounded ($V_S = 0$) and voltages are applied to the gate (V_G) and drain (V_D) electrodes. When a gate bias is applied, charge carriers accumulate near the semiconductor-insulator interface and the channel becomes conductive. Then a current driven by the drain voltage can flow from source to drain.

If the transistor consists of a thin semiconduting layer, it is called thin-film transistor (TFT). The main physical differences is that TFTs have no chemical doping regions and, thus, they operate in the accumulation mode. The accumulation mode is discussed in detail in section 5.1. Further, in TFTs, the accumulated charges at the interface come from the source and drain electrodes and not like in FETs from the bulk.

2.3. Basic Device Characteristics

The following section is inspired by the works of Sze and Golubkov [1, 48]. The device characteristic of TFTs cannot be correctly described by a single equation. Therefore, it has been separated in two well-distinguishable working regimes. But before we establish basic quantitative relations, we shall first present a qualitative discussion of device operation.

When a gate bias is applied, charge carriers accumulate at the interface and the channel becomes conductive. Without drain bias, the charge carrier distribution at the interface is uniform. When we now start to apply a drain bias, a current starts to flow and the



(a) (b)

Figure 2.2.: (a) saturation regime (b) linear regime; the shaded areas in the channel indicates the charge carrier distribution

charge density distribution change from uniform to one that decreases from source to drain. ($V_G < V_D$). This region is called *linear regime* (figure 2.2(b)). The drop of carrier density can be easily understood when one consider that the absolute voltage between drain and gate is lowered through the drain bias, while the voltage between source and gate stays constant. Since the charge density is proportional to the potential relative to the gate electrode and this potential decreases from source to drain, also the charge density decreases from source to drain.

When the drain bias is further increased, a certain voltage ($V_{D,sat}$) is reached, where the drain current becomes independent of the drain voltage. From now on the transistor operates in the *saturation regime* (figure 2.2(a)). At the transition point the local potential relative to the gate at the drain electrode is zero ($V_G \simeq V_D$) and, thus, a depletion region forms next to the electrode. The channel is "pinched-off". The pinch-off point Y moves away from the drain electrode with the V_D-to-V_G ratio, but potential there stays at the constant value $V_{D,sat}$. This means that the number of carriers arriving at point Y remains the same and they will be injected there into the depletion zone. Between Y and the drain electrode a space-charge limited current flow. In figure 2.3 a typical output and transfer characteristic of a TFT are plotted.

In both regimes, the channel acts as a resistor. The differential resistance of the channel is given by

$$dR = \frac{dy}{W \int \sigma(z,y) dz} \tag{2.5}$$

where σ is the channel conductivity and W is the channel width. The channel conductivity can be approximated by

$$\sigma = qn(z,y)\mu \tag{2.6}$$

with charge carrier density n and carrier mobility μ. Here the mobility is not assumed to be constant, rather the dependence of gate bias on mobility do not play a role at this point of the derivation. When a gate bias is applied, *surface charges* accumulate on both sides of the insulator. In the bulk material are no mobile carriers, which would contribute to the integral in equation 2.5. The number of accumulated charges is proportional to

the gate bias. Hence the integral in equation 2.5 can be expressed as

$$\int \sigma(z,y)dz = Q(y)\mu = C_i(V_G - V_T - V(y))\mu \tag{2.7}$$

$Q(y)$ are the free charges, C_i is the capacitance of the insulator, V_G is the applied gate bias, V_T is the threshold voltage. V_T includes, that in most cases a certain voltage needs to be applied before first free charges are accumulated at the interface. Hence, $V_G - V_T$ is often referred to as the *effective gate bias*. The term $V(y)$ takes into account that, the surface-potential is not constant across the channel, if a drain bias is applied. When we substitute equation 2.7 into equation 2.5 and multiply it with drain current, we find

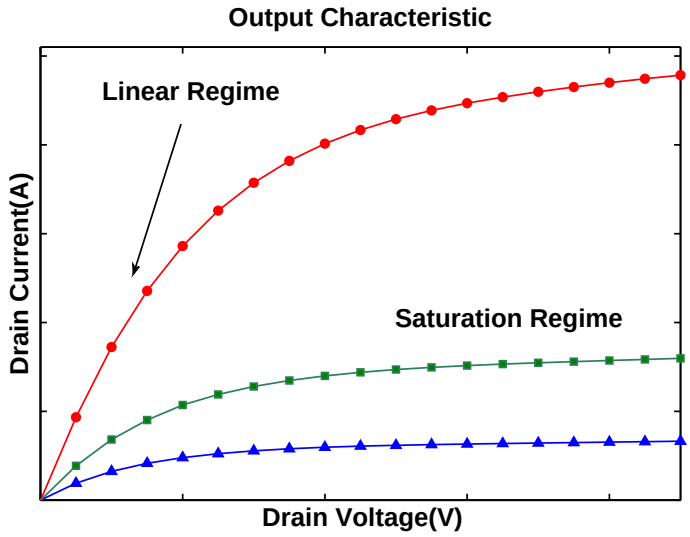
$$dV = I_D dR = \frac{I_D dy}{W\mu C_i(V_G - V_T - V(y))} \tag{2.8}$$

Now we can separate the variables and integrate along the channel, which yields to a general form of voltage-current characteristic of an OFET.

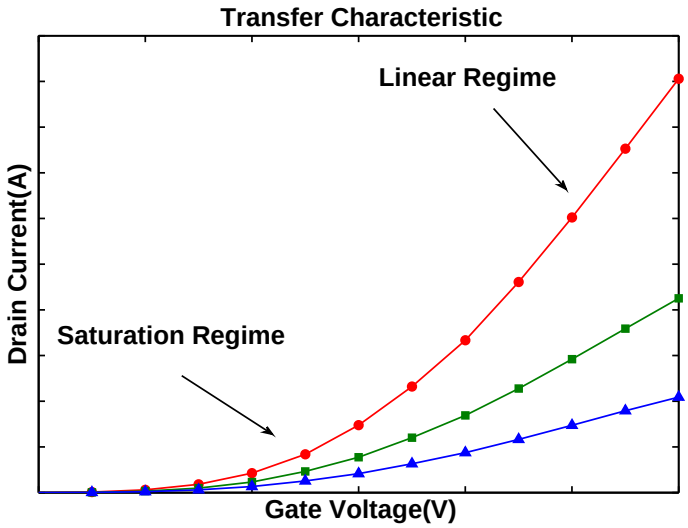
$$I_D = \frac{W}{L}\int_0^{V_D} \mu C_i(V_G - V_T - V)dV \tag{2.9}$$

The mobility can be considered as constant only under the condition, that it is gate field and charge carrier density independent. In inorganic single crystals the assumption of a constant mobility along the channel is justifiable, however, in polycrystalline and amorphous materials a charge carrier density dependent mobility is observed.

The drawback of this derivation is that no contact resistance and no bulk conductivity have been taken in account. Therefore, it would be more correct to speak of a general form of the channel resistance than of a general voltage-current characteristic. Anyhow, equation 2.9 gives us the starting point for any further derivations and considerations in this work.



(a)



(b)

Figure 2.3.: Current-voltage characteristics of a pentacene OTFT :(a) Output characteristics; here one sweeps drain voltage at fixed values of gate voltage; (b) Transfer characteristics; here one sweeps gate voltage at fixed values of drain voltage

3. Metal-Oxide-Silicon FET

The primary reason to study the Metal-Oxide-Silicon-Field-Effect-Transistor (MOSFET) is to compare its operation principles with that of an OTFT and thereby improve the understanding of both. We will primarily consider the n-type or n-channel MOSFET in this section. The schematic structure of a MOSFET is shown in figure 3.1. It consists of a lightly p-doped silicon substrate into which two highly n-doped wells are formed. This section is largely based on Ref. [1, 3].

First we illustrate the situation at zero gate bias. The silicon is in fact insulated from the metal by the oxide, but a charge redistribution occurs between the silicon-oxide interface and the gate metal through a connected wire between source and gate. The redistribution is caused by the work function difference between semiconductor and metal. Generally, this current flow leads to recombination and causes space charges at the interface. Also at the p-n barriers space charges form through diffusion. In other words the p-n barriers constitute two diodes connected back to back.

3.1. Different Bias Modes

Basically, one can identify three different gate bias regimes, which are separated by two specific gate voltage values, as illustrated in figure 3.2.

3.1.1. Accumulation

When a negative gate bias is applied, the space charge layer at the interface will be removed, until no space charges are present at semiconductor - insulator interface. This point is referred to as the *flat band voltage* $V_{FB} = q(\Phi_M - \Phi_S)$, which is proportional to the work function difference between metal and semiconductor. Applying a gate bias more negative than V_{FB} leads to an accumulation of holes at the semiconductor-insulator interface. In this regime the FET is not conductive, due to the diode at source electrode.

3.1.2. Depletion

When a positive gate bias is applied, electrons are attracted to the interface and recombine with holes and produce thereby ionized lattice atoms. The number of holes close to the interface decreases. Therefore, the region next to interface is called *depleted*. When the positive gate bias is further increase, the depletion layer at the interface grows until all dopants are ionized. This point is called *threshold voltage*. In the depletion regime only space-charges and holes are present at the interface.

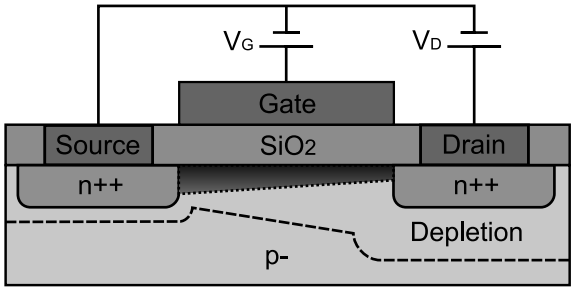


Figure 3.1.: Cross-section of an Metal-Oxide-Silicon-Field-Effect-Transistor

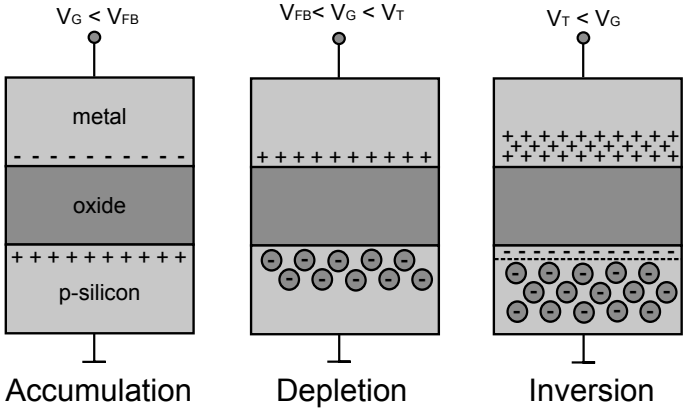


Figure 3.2.: Charges in an Metal-Oxide-Semiconductor structure under accumulation, depletion and inversion conditions. Encircled charges are space-charges.

3.1.3. Inversion

As one further increases the positive gate bias, electrons are accumulated at the semiconductor - insulator interface. Now the channel can be consider to be a n-type semiconductor and together with the n-type wells forms a n-n-n structure. The formerly mentioned diodes disappear and channel becomes conductive. The accumulation layer is isolated from the bulk by the depletion layer. The conductivity of the channel depends on the number of accumulated electrons.

3.2. Working Regimes

Here, the considerations of section 2.3 for the MOSFET are finished.

In single silicon crystals, the charge transport is dominated by band transport. This means that the carrier mobility is largely determined by phonon-electron interaction. The more phonons, the lower is the mobility. In General, there is no reason why the phonon density should not be uniformly distributed in an ideal crystal. So it can be assumed that the mobility is constant along the channel.

For the MOSFET, bulk currents do not need to be taken into account, because channel, source and drain are isolated from the bulk by the depletion layer. The metal-

semiconductor contact is typically considered as a Schottky contact[1]. The two highly doped n++ wells under the metal electrodes minimize the Schottky barrier. Thus, the contact can be treated as a ohmic contact with a negligibly small contact resistance.

The MOSFET operates in the linear regime until the channel is pinched off. This happens, when the effective gate potential and drain potential are equal. From this point on it operates in the saturation regime. Consequently, the condition for operating in the saturation regime can be written as

$$V_D > V_G - V_T \tag{3.1}$$

With these assumptions, it is possible to solve the integral in equation 2.9 and thereby complete the estimation of the I-V characteristic for MOSFETs.

3.2.1. Linear Regime

When constant μ is assumed, equation 2.9 can be integrated and the I-V characteristic for the linear regime is obtained:

$$I_D = \frac{W}{L} C_i \mu (V_G - V_T - \frac{V_D}{2}) V_D \tag{3.2}$$

At very small drain voltages V_D the charge carrier density can be assumed as uniform. Hence the channel can be treated as a tunable resistor.

$$I_D = \frac{W}{L} C_i \mu (V_G - V_T) V_D \qquad \text{for} \qquad V_D \ll V_G - V_T \tag{3.3}$$

At high V_D, but still below $V_G - V_T$, the increased gradient of the charge carrier density avoids a proportional increase of the drain current with drain bias.

3.2.2. Saturation Regime

The drain current becomes independent of the drain bias, when the saturation point is reached (equation 3.1). Therefore, we replace V_D with $V_G - V_T$ in equation 3.2, and get the value of the saturated drain current by following equation:

$$I_{D,sat} = \frac{W}{2L} C_i \mu (V_G - V_T)^2 \tag{3.4}$$

However, the measured drain current in saturation is not constant as predicted by 3.4. Instead it increases with drain-source voltage due to channel length modulation, drain induced barrier lowering or two-dimensional field distributions [3].

3.3. Threshold Voltage

The physical origin of the threshold voltage in organic FETs differs from that of the silicon one. In general, the threshold voltage in MOSFETs designates the transition point from weak to strong inversion. For this reason, the operation-mode of a MOSFET

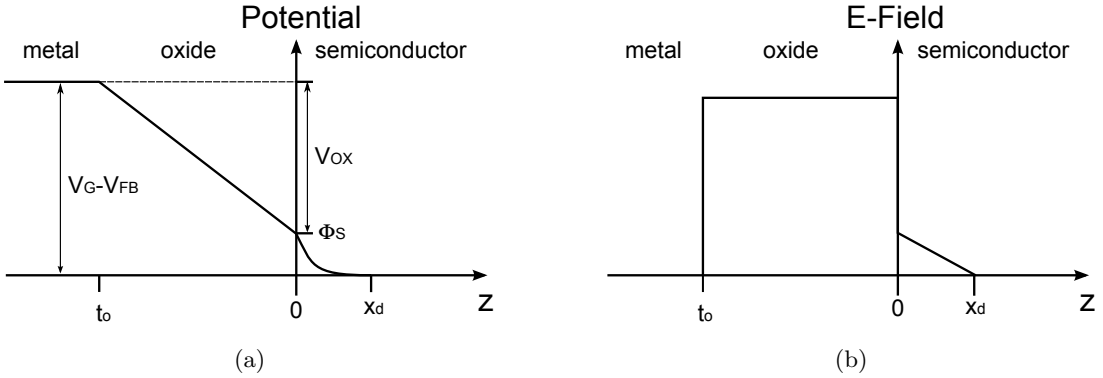


Figure 3.3.: Electrostatical analysis of an MOS structure: (a) the potential, (b) the electric field

is often called inversion-mode. In this section, we briefly derive an expression for the threshold voltage in MOSFETs.

In the depletion regime a gate bias below the threshold is applied. Minority charges are induced and recombine with the dopants. A depletion layer forms with a thickness z_d:

$$Q_d = qN_d z_d \tag{3.5}$$

where N_d is the dopant density and Q_d the depletion layer charge. The formation of space charges at the interface creates an electric field inside the semiconductor (figure 3.3(b)). As a consequence not the whole potential drops across the oxide (figure 3.3(a)). The remaining surface potential Φ_s is given by

$$\Phi_s = \int_0^{z_d} E dz = \int_0^{z_d} \frac{Q_d}{\epsilon_s} dz = \int_0^{z_d} \frac{qN_d z}{\epsilon_s} dz = \frac{qN_d z_d^2}{2\epsilon_s} \tag{3.6}$$

Note, for a gate bias below the threshold voltage ,Φ_s dependents on the depletion layer thickness z_d. The surface potential leads to a band bending in the band diagram (figure 3.4(b)). According to figure 3.3(a), the induced charge can be expressed by

$$Q = -(Q_d + Q_{inv}) = V_{ox} C_{ox} = (V_G - V_{FB} - \Phi_S) C_{ox} \tag{3.7}$$

where, Q_{inv} is the inversion layer charges. Because we are still considering the depletion regime, the inversion layer charge Q_{inv} is approximately zero. When we rewrite equation 3.7 and substitute with equation 3.5, we obtain

$$V_G = V_{FB} + \Phi_S - \frac{Q_d + Q_{inv}}{C_{ox}} = V_{FB} + \Phi_S - \frac{qN_d z_d}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} \tag{3.8}$$

If a lager bias is applied, the depletion layer and the surface potential grows and consequently the bands bend downward even more. At a certain gate bias, the intrinsic level E_i crosses over the Fermi level E_F. At this point, when the Φ_S equals the bulk potential Φ_B, weak inversion starts (figure 3.4(b)). Strong inversion begins when the density of induced charges equals the dopant density. This is the case when the surface

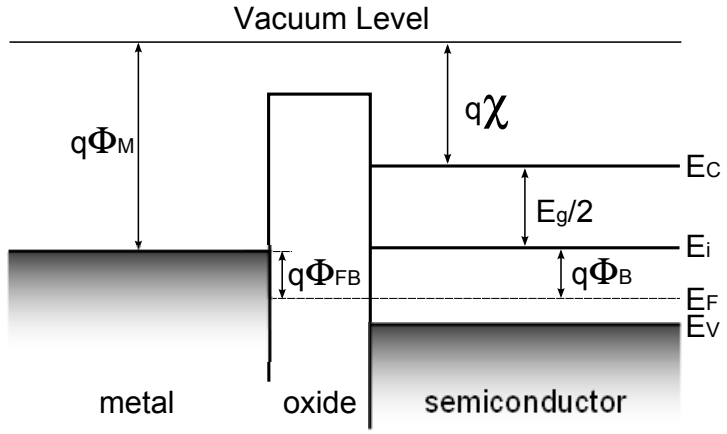
potential equals twice the bulk potential Φ_B. Then the conduction band starts to fill with minority carriers. As stated before, this gate voltage is defined as threshold voltage. Beyond the threshold voltage the inversion layer charge increases exponentially with the surface potential. The inversion layer charges can be consider as surface charge. Hence, an increased gate voltage yields to a larger potential drop across the oxide, while the surface potential Φ_S remains almost at $2\Phi_B$. Therefore we can substitute Φ_S with $2\Phi_B$ in equation 3.8 for gate bias above the threshold.

$$V_G = V_{FB} + 2\Phi_B - \frac{qN_d z_d}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} = V_T - \frac{Q_{inv}}{C_{ox}} \tag{3.9}$$

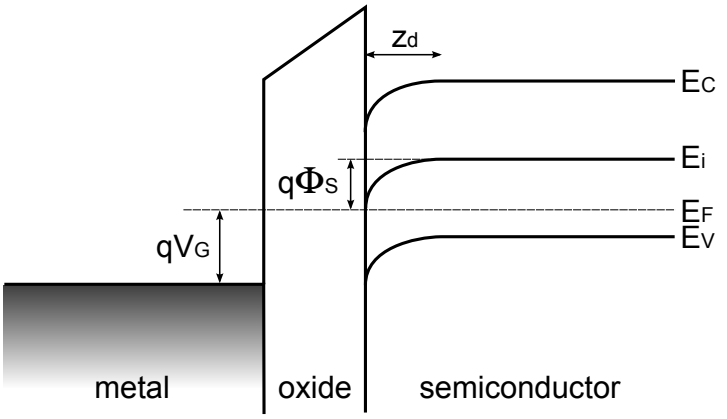
The depletion layer thickness can be estimated, when we again substitute Φ_S with $2\Phi_B$ in equation 3.6. We obtain the following expression for the threshold voltage:

$$V_T = V_{FB} + 2\Phi_B - \frac{\sqrt{4\epsilon_s q N_d \Phi_B}}{C_{ox}} \tag{3.10}$$

As we can easily see, the threshold voltage in MOSFETs can be varied with the doping density N_d. The flat-band voltage is determined as mentioned before by the work function difference between gate metal and the semiconductor.



(a)



(b)

Figure 3.4.: Band diagrams of an MOS structure: (a) at flat band voltage and (b) at transition from depletion to weak inversion; E_i is the Fermi level of an undoped semiconductor. The difference of Fermi level E_F and E_i is proportional the bulk potential Φ_B. χ is the electron affinity in the semiconductor. E_g labels the energy gap between conduction band edge E_C and valence band edge E_V.

4. Charge Transport in Organic Materials

Charge transport in metals and conventional semiconductors is associated with band transport. Band transport is governed by *delocalized* states and it is limited by the scattering of the carriers. Carriers are mainly scattered by phonons, which are thermally induced lattice deformations. This would predict an increasing charge carrier mobility with decreasing temperature. In organic materials the opposite case has often been observed, namely a decreasing mobility with decreasing temperature[5, 6]. Additionally, simple estimates show that the mean free path of carriers is shorter than the mean atomic distance [4]. Therefore, the band model is no longer valid in low conductivity materials such as amorphous or organic semiconductors and alternative models had to be developed to describe charge transport in these materials.

All of these models include *localized* states. Basically, the underlying physical principles of charge transport can be classified in two groups: carrier hopping/tunneling between localized states and band-like transport in delocalized state through thermal activation of localized carrier. Both transport models do not exclude each other and can appear combined. Hence, the resulting temperature dependencies of these models are of particular interest as they can bear information about the dominating process in the investigated organic semiconductor. However, the applicability of these model is still not satisfying and, therefore, the models need to be further improved.

4.1. Hopping Transport

Hopping transport is associated with amorphous semiconductors. Conduction happens by hopping/tunneling between localized states. All carriers are localized at any given time. Charge transport is highly dependent on number and distribution of trap sites. Various models have been developed, such as variable-range hopping by Mott[8], the Bässler model[9] and the Vissenberg-model[10]. In most cases, the temperature dependence of mobility follows a law of the form:

$$\mu = \mu_0 e^{-\frac{T_0}{T}\frac{1}{\alpha}} \tag{4.1}$$

where α is an integer between 1 and 4.

4.2. The Multiple Trapping-and-Release Model

The multiple trappping-and-release model (MTR) [12] is associated to semiconductors with more or less crystalline properties. It combines band-like transport with localized states. Unlike in metals, not all carriers contribute to charge transport. Charge carriers are divided into two classes: mobile and trapped ones. The mobility for mobile carriers is

related to the *intrinsic mobility* μ_0. On the other hand, the mobility of trapped carriers is zero. Hence, the observed *effective mobility* μ_{eff} is determined by the mobile-to-total carrier ratio. Similar concepts are used for other models like the mobility edge model [6]. Here, only the MTR model will be discussed. In that a delocalized conduction band as well as localized electronic states close to the band edge exists. Trapped carriers can change into the conduction band through thermal activation. The spatial distribution of the trap sites is uniform all over the channel. The following subsections are based on Ref. [7].

4.2.1. Single Trap Energy

A first good approximation is to assume a single trap energy E_t with a density of states (DOS) N_t. The conduction band edge is at energy E_c. If the trap density N_t is much larger than the induced charge carrier density $n_f + n_t$, we can estimate the free carriers density n_f and trapped carries density n_t with simple Boltzmann statistics:

$$n_f = N_c e^{-\frac{E_c - E_F}{k_b T}} \tag{4.2}$$

$$n_t = N_t e^{-\frac{E_t - E_F}{k_b T}} \tag{4.3}$$

N_c and N_t are the densities of states associated with the conduction band edge and the trapped states, respectively. The observed effective mobility is then given by the ratio of mobile to induced carriers:

$$\mu_{eff} = \mu_0 \frac{n_f}{n_f + n_t} = \mu_0 \frac{1}{1 + \frac{N_t}{N_c} e^{\frac{E_c - E_t}{k_b T}}} \approx \mu_0 \frac{N_c}{N_t} e^{-\frac{E_c - E_t}{k_b T}} \tag{4.4}$$

The approximation in equation 4.4 is justified, because the trap energy is lower than the conduction band edge energy and consequently the number of trapped charges is higher than the number of free charges. The resulting temperature dependence of the mobility shows Arrhenius-like behavior. Note that no gate voltage dependence of the mobility is obtained.

When the number of trap sites is smaller than the induced charge, Boltzmann statistics do not hold anymore. In this case Fermi, statistics must be applied. Another effect that has to take into account, is that the conduction band and the single trap level are shifted towards the Fermi level due to the immobile (fixed) trapped charges. Consequently, a nonzero surface potential V_S arises and affects the statistic. Free and mobile carriers are then given by:

$$n_f = \frac{N_c}{1 + e^{-\frac{E_c - E_F - qV}{k_b T}}} \tag{4.5}$$

$$n_t = \frac{N_t}{1 + e^{-\frac{E_t - E_F - qV}{k_b T}}} \tag{4.6}$$

The important outcome of this model is that mobility is gate bias dependent. The more charges are accumulated, the more the energetic distance between Fermi energy E_F and E_C decreases and, therefore, the free-to-mobile carrier ratio increases (figure 4.1(b)).

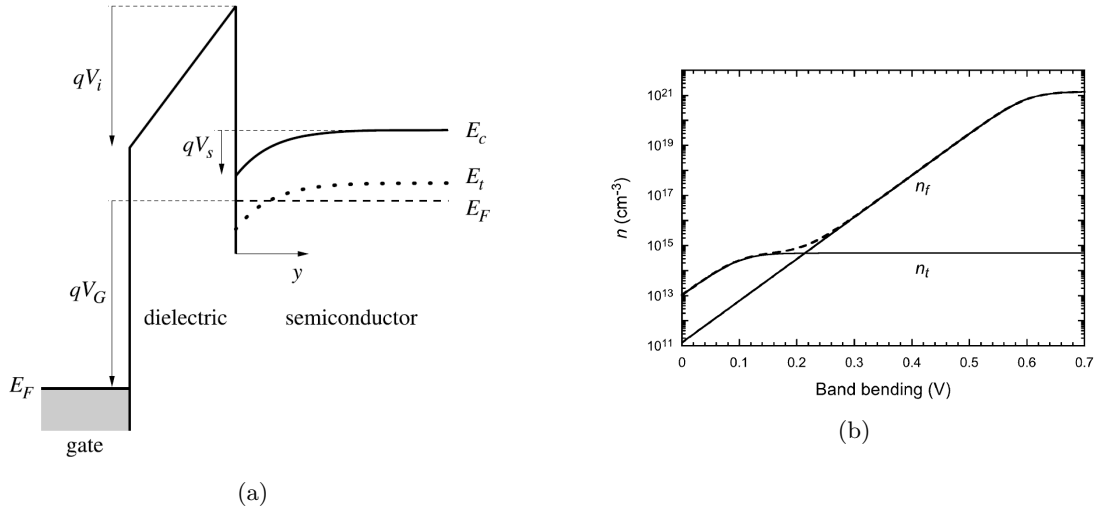


Figure 4.1.: (a) band diagram of a single shallow trap (b) free(n_f) and trapped(n_t) charge distribution as a function of the accumulation band bending; Pictures taken from Braga et al.[11]

4.2.2. Distributed Trap Energy

In real systems, the energies of the trap sites are distributed in a certain way. In hopping models, the preferred DOS is a Gaussian distribution, because the trap distribution represents the conduction band in terms of hopping transport. In the case of MTR the trap distribution is often considered as a diffuse conduction band edge and, therefore, the appropriate approximate distribution is an exponential band tail:

$$D(E) = \frac{N_t}{k_b T_c} e^{-\frac{E}{k_b T_c}} \tag{4.7}$$

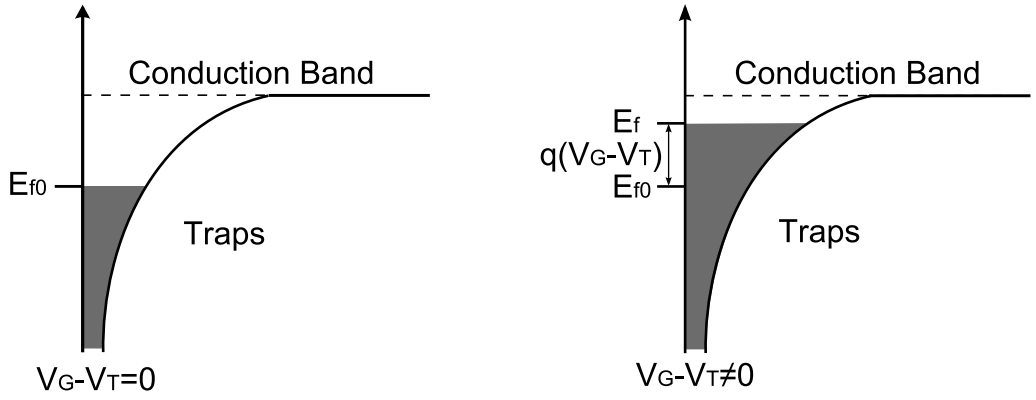
Here, T_c is the characteristic temperature that accounts for the shape of the distribution. The conduction band energy is set to zero for simplicity. One crucial assumption in this approach is that the density of free charges is a lot smaller than that of the trapped ones $n_f \ll n_t$, meaning that almost all induced carriers are trapped and shifting down the conduction band (figure 4.2). Then, the trapped charge carrier density can be expressed as:

$$n_t = \int_{-\infty}^{\infty} D(E) f(E) dE = \int_{-\infty}^{E_f} D(E) dE = N_t e^{-\frac{E_f}{k_b T_c}} = \frac{C_i (V_G - V_0)}{q} \tag{4.8}$$

where V_0 is the applied gate voltage. Here we assumed that $D(E)$ is a slowly varying function and therefore we could approximate the Fermi-Dirac distribution $f(E)$ by a step function. The band shift can be now expressed as follows:

$$E_f = E_{f0} + q(V_G - V0) = k_b T_c \ln\left(\frac{C_i (V_G - V_0)}{q N_t}\right) \tag{4.9}$$

We now need to estimate the free charge density. As indicated before, the distance between E_f and the band edge is large enough to approximate the Fermi-Dirac distribution



(a) (b)

Figure 4.2.: (a) band diagram at zero bias (b) band diagram at nonzero bias

by the Boltzmann distribution. Together with equation 4.9, the free carriers are then given by

$$n_f = \int_{-\infty}^{E_f} D(E) e^{-\frac{E}{k_b T}} dE = \int_{-\infty}^{E_f} \frac{N_t}{k_b T_c} e^{-\frac{E}{k_b T_c}(1+\frac{T_c}{T})} dE = \tag{4.10}$$

$$= N_t \left(1 + \frac{T}{T_c}\right) e^{-\frac{E_f}{k_b T_c}(1+\frac{T_c}{T})} = N_t \left(1 + \frac{T}{T_c}\right) \left(\frac{C_i(V_G - V_0)}{qN_t}\right)^{\frac{T_c}{T}-1} \tag{4.11}$$

The effective mobility is again calculated from the ratio of free to induced charges. For $n_t \gg n_f$:

$$\mu_{eff} \approx \mu_0 \frac{n_f}{n_t} = \mu_0 \left(1 + \frac{T_c}{T}\right) \left(\frac{C_i(V_G - V_0)}{qN_t}\right)^{\frac{T_c}{T}-2} \tag{4.12}$$

Through this analytical derivation we obtained a gate bias mobility dependence as well as an Arrhenius-like temperature dependence. Another feature of this model is that the shape of the measured gate bias mobility dependence can give information about the trap distribution.

5. Organic TFT

The derived models for MOSFETs cannot be transfered to describe organic thin-film transistor(OTFT) characteristics in a straight forward way. Reasons for this are: OFETs operate in the accumulation-mode, the different underlying charge transport mechanism and the increased role of the contact resistance.

5.1. Accumulation Mode

OTFTs do not have chemical doping regions. In other words, in OTFTs we cannot distinguish between majority carriers, which originate form the dopants, and minority carriers, which are the intrinsic free carriers of the semiconductor. Moreover, organic materials do not have any intrinsic free carriers. The free charges that are accumulated at the semiconductor-insulator interface, when a gate voltage is applied, are injected from the electrodes. This has following the consequences for the gate bias regimes:

1. Minority carriers cannot outnumber majority carriers at the interface, but that is the definition of the inversion-regime in MOSFETs. In other words the inversion case cannot occur in OTFTs and consequently no inversion regime can exist.

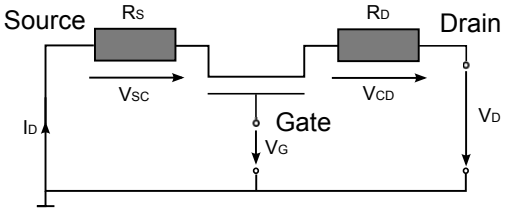
2. Generally spoken, a depletion region forms when minority carriers recombine with majority carriers. As a result of the recombination, ionized lattice atoms are created and both free carrier species are depleted. In MOSFETs the depletion regime is the gate voltage range, where this kind of recombination is observed at the semiconductor-insulator interface. Since there are no free intrinsic carriers in OTFTs, the depletion regime does not exist either.

Assuming that charge carriers injection at the source and drain electrodes works for both sorts of carriers, it can be said that the gate bias regimes reduce to only two distinguishable regimes: electron accumulation and hole accumulation. Below the flatband voltage holes are accumulated at the interface and above the flatband voltage electrons are accumulated.

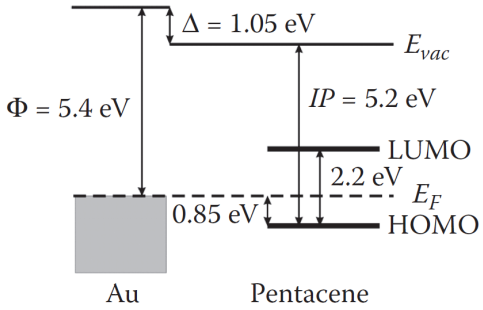
The previous analysis of the gate bias regimes makes the conventional definition of the threshold voltage as transition point from depletion to inversion obsolete. A new definition for the threshold voltage must be found. Horowitz et al. have already pointed out the difficulty of defining a threshold voltage in OTFTs [17]. Generally, the threshold voltage is used in FET or TFT equations to determine the amount of induced mobile charge at the semiconductor-insulator interface for a specific gate voltage value:

$$Q = C_i(V_G - V_T) \tag{5.1}$$

Hence, a more abstract definition of the threshold voltage is, that it is the point in the gate bias spectrum, where first mobile charges emerge at the interface. In the sense of



(a) Equivalent circuit diagram of an OTFT with contact resistance



(b) Energy level alignment in the Au-pentacene junction, taken from Ref. [15]

this definitions the threshold voltage in OTFTs equals the flatband voltage:

$$V_T = V_{FB} \tag{5.2}$$

A similar version of this definition is used by Meijers et al. [24].

Further consequences of missing doping regions are that no p-n junctions and no depletion layers exist. The p-n junctions disable charge transport for one charge carrier species and establish in this way the unipolar charge transport character of MOSFETs. This is not the case in OTFTs. Here, the p-polar device character of most OTFTs origins form several factors: the HOMO bandwidth is typically larger than the LUMO bandwidth [13], a stronger trapping of n-type polarons [14], and a larger Schottky barrier for electron injection into organic semiconductors from the most commonly used high work function metals.

The depletion layer in MOSFETs isolates the inversion channel from the bulk. It is therefore justified to treat the inversion layer as surface charges. In OTFTs, we need to take into account that the channel has a spatial extension perpendicular to the semiconductor-insulator interface, especially for gate voltages slightly beyond the flatband voltage. In the case of charge carrier concentration dependent mobilities, this fact has a profound effect on the gate bias dependence of mobility.

At zero bias, the situation at the semiconductor-insulator interface is similar to that of MOSFETs. The work function difference causes a charge rearrangement, but in OTFTs no space charge layers are formed at the interface. In fact, these accumulated charges are already mobile charges and could permit current flow along the channel.

5.2. Contact Resistance

Contact resistance constitutes one of the great challenges in OTFT technology and organic material analysis. In the case of low carrier mobilities and consequently high channel resistance, the role of contact resistance is comparatively low. But with increasing mobilities, which is one requirement for commercial use, the performance of OTFTs is increasingly limited by the contact resistance. Currently, a lot of groups are developing new process technologies to minimize the impact of the contact resistance on the OTFT performance[27].

The contact resistance is usually considered to be composed of two separate parts[18]: An injection barrier at the metal-semiconductor interface and charge transport through a low conductivity region close to the contact. The magnitude of the latter strongly dependents on the devices structure. In a top contact device structure, it is associated with the undoped region between the metal contact and the accumulation layer[19]. In contrast, in bottom contact structures it is often assigned to the region next to the electrodes, which is less conductive due to structural defects[20, 21]. In both cases a strongly gate bias dependent resistance is observed[18, 19]. The underlying physical reasons for the gate bias dependence are still debated.

The injection resistance at the metal-semiconductor interface originates from the energy level difference of the Fermi level of the contact metal and HOMO or LUMO of the organic semiconductor [15]. However, the barrier height is not only given by the work function difference as the Schottky-Mott model predicts[19]. Instead the interface exhibits an additional dipole barrier that tends to lower the metal work function(figure 5.1(b)).

5.3. Operation Regimes

Frist, the derivation of section 2.3 is finished for OTFTs.

First, we have to take into account a gate bias dependent mobility in our equations. We, therefore, introduce a semi-empirical law suggested by Horowitz and coworkers[15, 16]:

$$\mu = \mu_0 (V_G - V_T)^\gamma \tag{5.3}$$

where V_G is the gate voltage, V_T is the threshold voltage and μ_0 and γ are empirical parameters. μ_0 equates to the mobility at 1 V gate bias.

Furthermore, the impact of an increased contact resistance must be included [23, 22]. The equivalent circuit diagram of an OTFT with contact resistance is shown in figure 5.1(a). First of all, we have to correct the drain bias for the voltage drop across both resistors $R_{SD} = R_S + R_D$. This is done by replacing V_D by

$$V_{DS} = V_D - I_D R_{SD} \tag{5.4}$$

Additionally, the contact resistance effects the carrier distribution, when current flows. The source electrode is actually grounded. Once a drain bias is applied and a current flows, the potential next to the electrode inside the channel differs from ground potential due to the voltage drop across the resistor R_S. On the drain electrode we face the same situation. The corrected relative potentials inside the channel relative to the gate are:

$$V_{GS} = V_G - V_T - I_D R_S \tag{5.5}$$

$$V_{GD} = V_G - V_T - V_D + I_D R_D \tag{5.6}$$

Evidently, the contact resistance shifts the transition point from linear regime to saturation regime. Therefore, the condition 3.1 need to be modified. The saturation regime is reached, when V_{GD} becomes zero. We, therefore, replace V_{GD} in equation 5.6 with zero to obtain the new condition for saturation in OTFTs. The new condition is then

give by:

$$V_D > V_G - V_T + I_D R_D \tag{5.7}$$

Note that the actual operating regime now is not exclusively determined by the applied voltages. Compared to negligible contact resistance, the necessary absolute drain bias for reaching the saturation regime is lowered.

5.3.1. Linear Regime

Before we continue to adapt the equations for device characteristics, it must be clarified that although the contact resistance is gate bias dependent in real OTFTs, it would not lead to an useful expression, if the gate bias dependence was included into the derivation. Firstly, as stated in the previous section, the underlying physics of it is not well-understood and hence the specific form of the dependence is not known. Secondly, a additionally gate bias dependent factor in the I-V characteristic would make the model too complex for identifying the single parameters.

Anyhow, a first good approach is to consider a constant contact resistance and gate-bias dependent mobility simultaneously. The following derivation is based on the report of Natali et al. [23]. By substituting equation equation 5.3 into 2.9 and integrating it, we come to the following I-V characteristic for the linear regime:

$$I_D = \frac{W \mu_0 C_i}{L(\gamma+2)} \left[(V_{GS} - V_{DS})^{\gamma+2} - (V_{GS})^{\gamma+2} \right] \tag{5.8}$$

$$I_D = \frac{W \mu_0 C_i}{L(\gamma+2)} \left[(V_G - V_T - I_D R_S - V_D + I_D R_{SD})^{\gamma+2} - (V_G - V_T - I_D R_S)^{\gamma+2} \right] \tag{5.9}$$

One problem with equation 5.9 is, that it cannot be rewritten to express I_D explicitly. An explicit expression for the drain current is, however, preferred, because it could be used to interpret a measured I-V characteristics. In order to avoid this problem, we must restrict the regime to very low drain voltages. At very low V_D the charge carrier density distribution at the interface becomes uniform and we can treat the channel as a typical resistor and can avoid integrating along it:

$$R_C = \frac{L}{A}\frac{1}{\sigma} = \frac{L}{W}\frac{1}{H\sigma} = \frac{L}{W}\frac{1}{\mu C_i (V_G - V_T)} \tag{5.10}$$

An additional advantages of this restriction is, that for $V_D \ll V_G - V_T$, the voltage drops across the contact resistance, which are introduced in equation 5.5 and equation 5.6, are very small compared to the gate voltage and can be neglected. With the use of equation 5.10, the I-V characteristic then can be written as:

$$I_D = \frac{V_D}{R_{tot}} = \frac{V_D}{R_C + R_{SD}} = \frac{V_D}{\frac{L}{W}\frac{1}{\mu C_i (V_G - V_T)} + R_{SD}} \tag{5.11}$$

With respect to equation 5.3, we get a gate-bias dependent drain current

$$I_D = \frac{V_D}{\frac{L}{W}\frac{1}{\mu_0 C_i (V_G - V_T)^{\gamma+1}} + R_{SD}} = \frac{\frac{W}{L} C_i \mu_0 V_D (V_G - V_T)^{\gamma+1}}{1 + \frac{W}{L} C_i \mu_0 R_{SD} (V_G - V_T)^{\gamma+1}} \tag{5.12}$$

Figure 5.1 shows the effect of the contact resistance R_{SD} and the empirical constant γ on the electrical characteristics of OTFT devices. It can be easily seen that impact of the contact resistance increases with the drain current. Another noticeable point is that for a gate bias dependent mobility the performance of the OTFT is limited by the contact resistance.

5.3.2. Saturation Regime

When we apply the saturation condition equation 5.7 on equation 5.8 and we obtain for the saturated drain current

$$I_{D,sat} = \frac{W\mu_0 C_i}{L(\gamma+2)}(V_{GS} - V_T)^{\gamma+2} = \frac{W\mu_0 C_i}{L(\gamma+2)}(V_G - I_D R_S - V_T)^{\gamma+2} \tag{5.13}$$

Again, it is not possible to derive an explicit expression for I_D. In contrast to the linear regime we cannot simplify the problem and hence, it is very difficult to extract parameters from measurements in the saturation regime. Anyhow, equation 5.13 can be used for an investigation of the effects of R_S an γ on the electrical characteristic (figure 5.2), as it is done in Ref. [23, 22]. As it can be seen Figure 5.1, the contact resistance decreases the slope of the transfer curve and its influence become stronger at high drain currents.

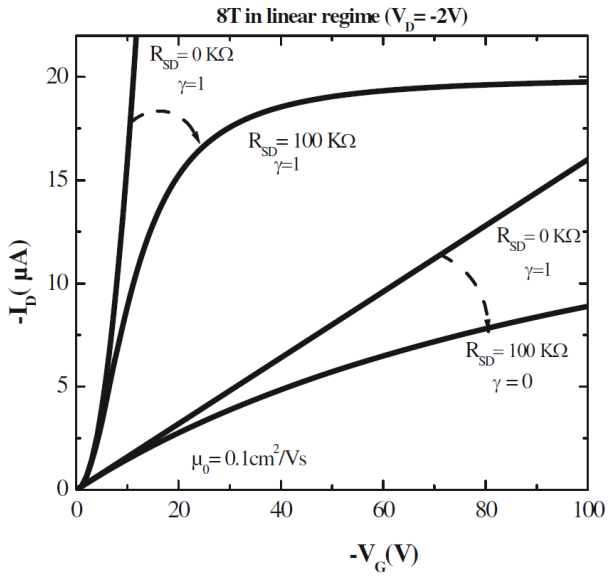


Figure 5.1.: Simulation of transfer characteristics in the linear regime according to equation 5.12; Picture take from Ref. [22]

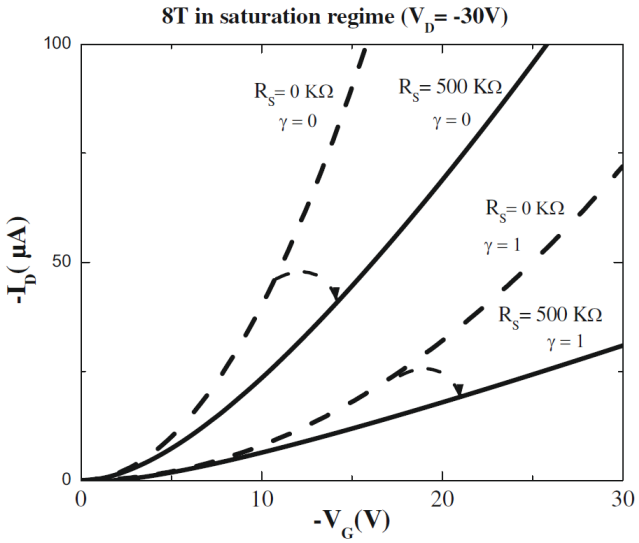


Figure 5.2.: Simulation of transfer characteristics in the saturation regime according equation 5.13; Picture take from Ref. [22]

Part II.

Experimental Methods

6. Sampel Preparation

A schematic structure of the device setup used in this work is shown in figure 6.1. This device structure is called top-contact bottom-gate structure. Highly p-doped silicon wafers with thermally grown SiO_2 in pre-cut substrates of 2x2 cm act as gate electrode and insulator.The sequence of process steps is as following:

1. Previous to any material deposition, the surface of the substrates is cleaned. Therefore, the dusty on the surface is blown away and afterwards the samples are O_2-plasma etched for 30 seconds.

2. Next, a pentacene layer with an average thickness of 35nm is evaporated at a base pressure of $1x10^{-5}$mbar. Afterwards, an atomic force microscope (AFM) picture of the pentacene surface is made. Figure 6.2 shows the typical look of the pentacene surface from a sample used in this work. The pentacene evaporation and the AFM picture are made by Anja Haase in the Institute of Nanostructured Materials and Photonics in Weiz. For the transport, the samples are placed in a transport box under high vacuum.

3. In order to be able to contact the device from the top, the SiO_2 is scratched away by a diamond cutter at the later location of the gate electrode.

4. Finally, 50 nm thick layers of Au are deposited through a shadow mask, whereby the channel is realized by tungsten wires of diameters of 25μm and 50μm. A sketch of the shadow mask is shown in figure 6.3. The pressure during the evaporation is typically around $4x10^{-6}$mbar. Two finial channels of 25μm and 50μm lengths are depicted in Figure 6.4. The actual channel lengths are slightly small than the diameters of the tungsten wires, but still in passable range of tolerance. The pictures are taken by an optical microscope of the type OLYMPUS BX51.

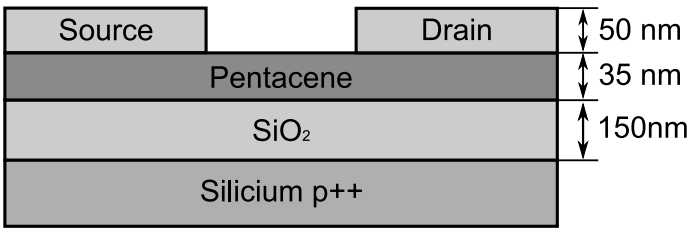


Figure 6.1.: Schematic structure of the samples used in this work.

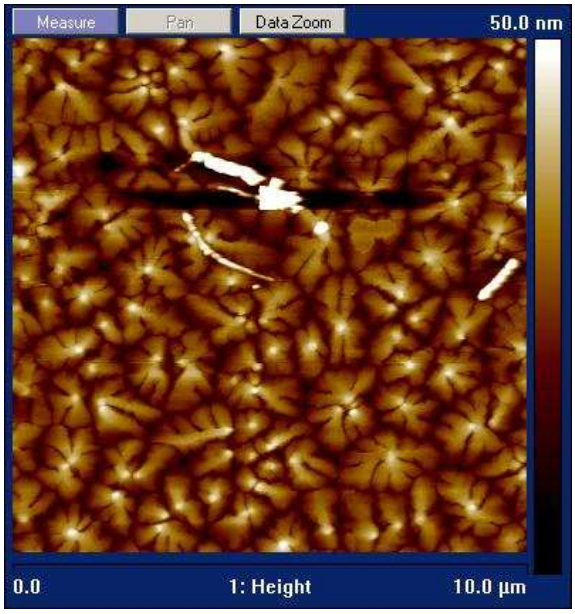


Figure 6.2.: AFM picture of the pentacene surface. Picture made by Anja Haase at NMP Weiz.

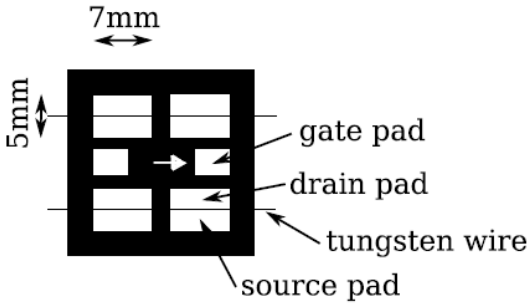
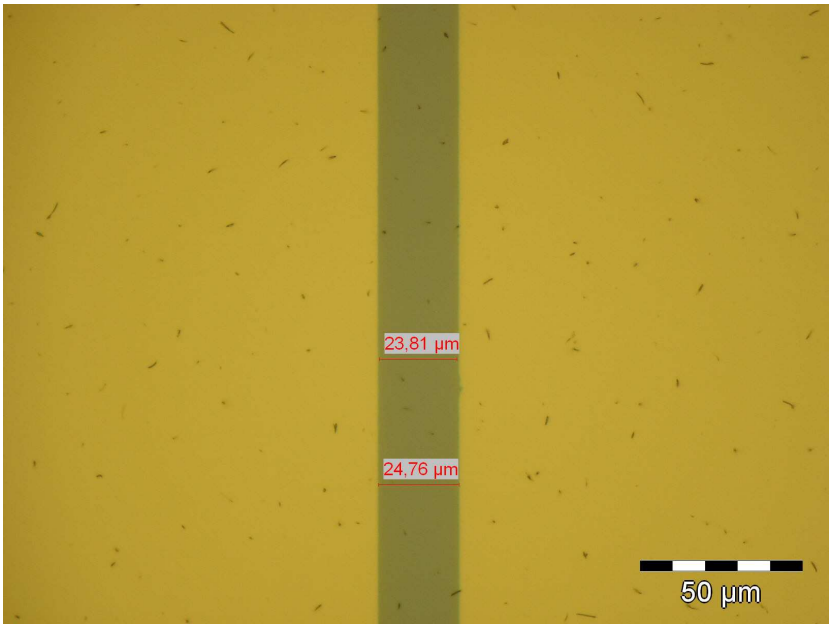
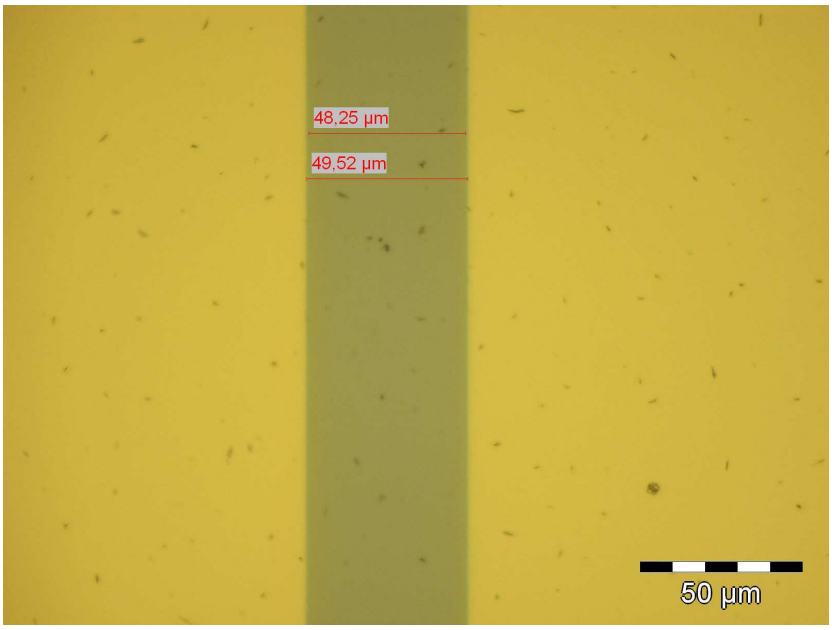


Figure 6.3.: Shadow mask through which gold contacts were evaporated on top of the semiconductor. Four devices with two common gate contacts were realized in this setup.



(a)



(b)

Figure 6.4.: Top view of the channels (a) $L = 25\mu m$ and (b) $L = 50\mu m$. Picture made with an optical microscope of the type OLYMPUS BX51.

7. Measurement setups

For the electrically characterization, two different measurement setups were used. The main features of both setups is presented in the following two section.

7.1. Glovebox setup

Here, the device can be continuously kept under inert conditions after the evaporation of the gold electrodes. The source, drain and gate are contacted with needles and the device are then electrically characterized with an Agilent E5262A parametric analyzer. The parametric analyzer is driven by a software supplied by agilent. The source current cannot be measured because the parametric analyzer have only two source measure units available.

7.2. Cryostatic setup

For measurements below room temperature, a cryostat from Oxford instruments of the type "Continuous Flow Cryostat CF 1204" is used. A sketch of the overall setup is shown in figure 7.1. The exact functionality of the cryostatic setup is described in Ref. [48] under chapter 10.

When the sample is transfered from the glove box to the cryostat, it is exposed to ambient air. To ensure that the oxygen doping of the semiconductor has no impact on our measurements, we performed a row of test measurements while the croystat is evacuated. It turned out that transfer characteristics returns to its original shape previously measured in the glove box.

In this setup, the devices are electrically characterized by a KEITHLEY 2636 dual-channel source meter. The advantage of the dual-channel source meter is that it can be simply controlled by a Labview program and, thus, special measurement routines can be easily realized. During this work a labview program for transfer and output characteristic measurement have been developed and installed in our lab and, additionally, a program for time dependent measurements. Figure 7.2 shows the Labview front panel of the program for transfer and output measurements.

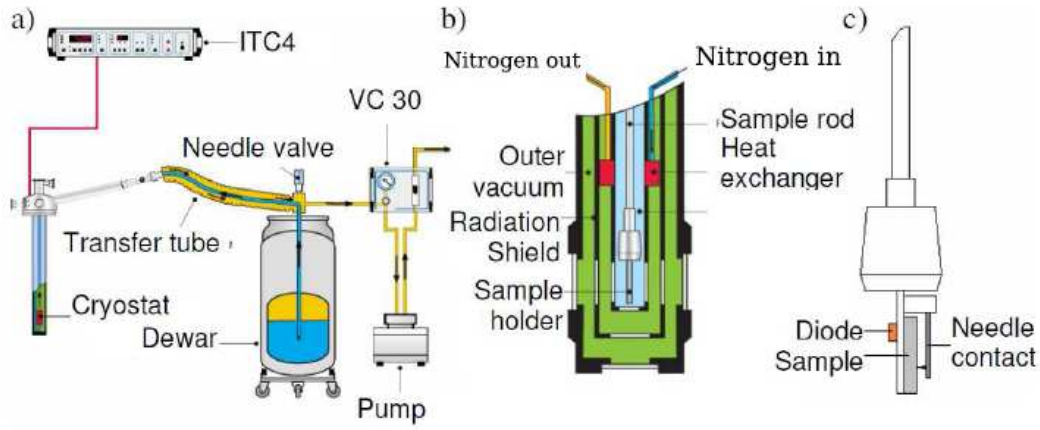


Figure 7.1.: (a) overview of the cryostatic setup. (b) Cross section of the sample space in the cryostat. (c) Sample holder. Picture taken from Ref. [48].

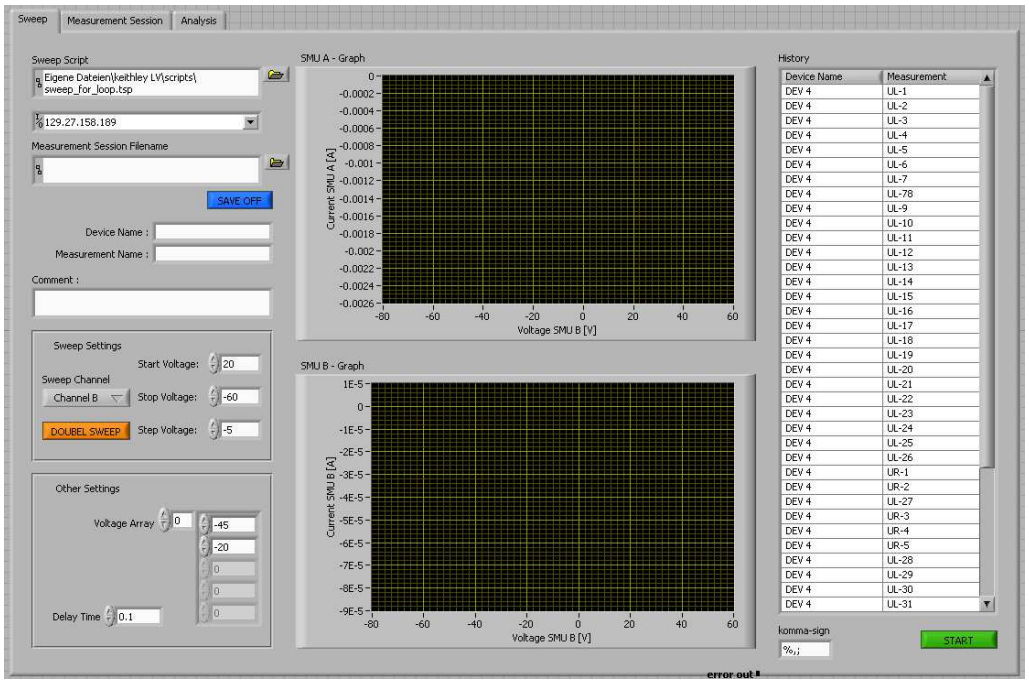


Figure 7.2.: Front panel of the Labview program for transfer and output characteristics measurement.

Part III.

Critical Evaluation of Parameter Extraction Methods

8. Standard FET model

The standard FET model (SFM) have been developed for parameter extraction on conventional inorganic semiconductors. As discussed in chapter 3.2, it is based on justified assumptions. In practice, this yields to reproducible measurement results, which indicates real physical quantities. In the case of organic transistors, these assumptions are basically false or in some cases valid only to a very limited extent. Therefore, the extracted parameters are just fit parameters without any physical meaning. However, the resulting parameters can be used to describe very roughly the shape of the characteristic transistor curves and/or to point out tendencies for the fabrication process. Nevertheless, one has to interpret the extracted parameters very carefully.

Using SFM, one can extract the threshold voltage, the carrier mobility and with reservations the contact resistance form the transfer characteristic. The exact procedure will be explained in the following subsection.

8.1. Linear Regime

For parameter extraction in the linear regime we use a similar version of equation 2.9:

$$I_D = \frac{W}{L} C_i \mu_A (V_G - V_{AT} - \frac{V_D}{2}) V_D \tag{8.1}$$

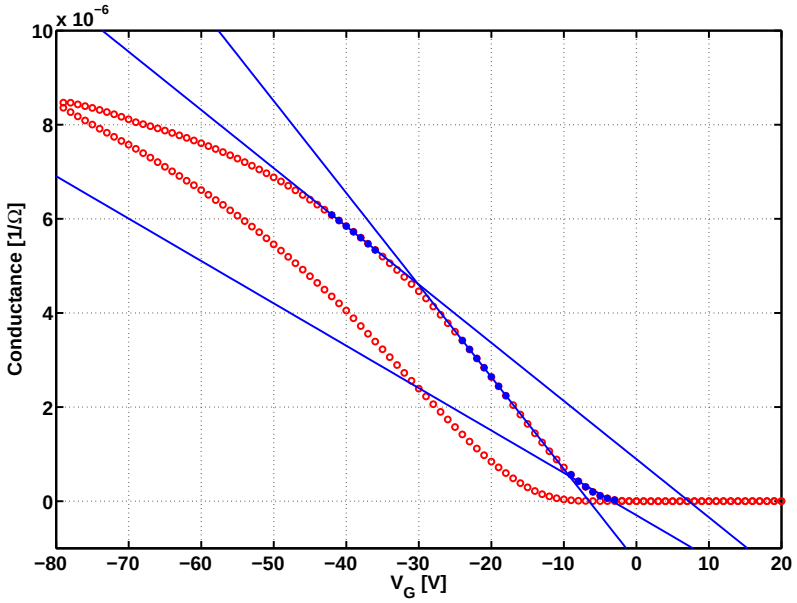
Because of the lack of physical meaning, mobility μ_A and threshold V_{AT} are often referred to as *apparent mobility* and *apparent threshold*.

According to equation 8.1 the measured data should result in a straight line that crosses the V_G axis at $V_G = V_T - V_D/2$. A linear fit performed on the data, measured in the on-state, gives us the mobility and the threshold voltage. Because of the various arguments presented previously, the actual measured transfer curve will not be a real straight line. Instead, the curve shows an upward curvature at low gate voltages and downward curvature at high gate voltages. In order to come to a consistently procedure, only data from a pre-defined voltage range are used for the linear fit. On this kind of procedure, the extracted parameters largely depend on the position and size of the voltage range (figure 8.1(a)). Usually, the linear regression curve is centered between the area of upward curvature at low gate voltages and the area of downward curvature at high gate voltages. The motivation for doing so is purely empirical.

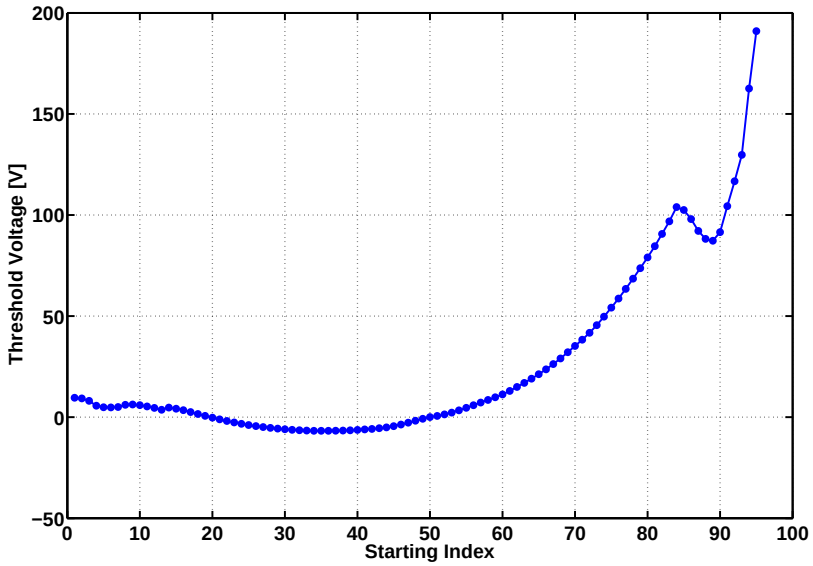
8.2. Saturation Regime

For parameter extraction in the saturation regime, we extract the root on both sides of equation 3.4:

$$\frac{\sqrt{I_D}}{C_i} \frac{L}{W} = \sqrt{\mu_A}(V_G - V_{AT}) \tag{8.2}$$



(a) Linear transfer line characteristic at $V_D = -0.5V$ of a pentacene OTFT. All measurement points in the on-state are located in the linear regime. Fits are performed on three different fitting windows, according to equation 8.1;



(b) Threshold voltage with respect to starting index i of the fitting window

Figure 8.1.: Parameter extraction in the linare regime

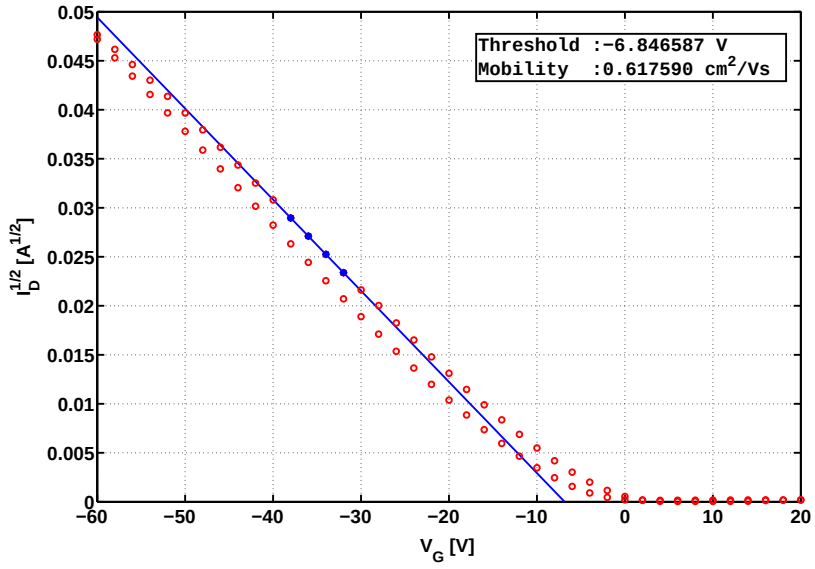


Figure 8.2.: Square root current as a function of the gate voltage. Transfer line record at $V_D = -45V$. Blue line represents the linear fit according to equation 8.2.

where μ_A and V_{AT} are the apparent mobility and the apparent threshold voltage, respectively.

With equation 8.2 one can extract the same parameters in saturation regime as extracted with equation 8.1 in the linear regime. When the square root of the saturation current is plotted as a function of the gate voltage, the model predicts a straight line, where the intersection point with the V_G-axis yields V_{AT} and the squared slope of the line is proportional to the mobility. The problems of parameter extraction in the saturation regime are more or less the same as in linear regime. The actually measured curve is again affected by the contact resistance and the gate bias dependent mobility and we again need to pick out a carefully chosen voltage range from the transfer curve to minimize the impact on the parameters. The manner of voltage range choice is exact the same as it is in the linear regime.

8.3. Range Selection Algorithm

In order to address the non-trivial problem of choosing the voltage range, a algorithm have been developed. The requirements were that it selects a voltage range of a fixed size in a way that it leads to the most reliable and reproducible extracted parameters. One problem in parameter extraction with the SFM is to use only measurement points, which belong to the appropriate regime. Normally, this cannot be tested until the value of the threshold is known (equation 3.1). Therefore, it is important for this kind of analysis to evaluate the choice of the measurement points after a value for the threshold voltage has been obtained.

The exact procedure of the algorithm will be presented in the following: (1) according

to the pre-selected voltage range size, fitting windows from i to $i+n$ are defined, where i is the index of the first measurement point and n the number of measurement points, which are used for the linear fit, (2) linear fits are performed for each voltage window, (3) the fit with the lowest slope (highest mobility) is chosen, (3) threshold voltage and mobility is estimated, (4) it is tested whether all measurement points are located in the appropriate regime, (5) if the test succeed the procedure ends here, otherwise the index i of the fitting window is increased or decreased (depending on whether the extraction is performed on the linear or saturation regime) and the cycle restarts from point 3. In figure 8.1(b) the threshold voltage as a function of the start index is shown.

We can avoid the step of testing, when we choose profitable drain voltage values for the transfer line measurement. The size of the saturation regime is always as large as the drain voltage value:

$$V_D + V_T > V_G > V_T \tag{8.3}$$

Hence, for drain voltages, smaller than the gate voltage step width of the sweep, it can be assumed that all points are located in the linear regime. The same applies to the saturation regime for drain voltages, much higher than the highest absolute gate voltage of the sweep.

8.4. Gate Bias Dependent Mobility and Constant Contact Resistance Model

The main drawback of both of the above discussed methods is that they provide only an average value for the mobility in the fitted voltage range. It is normally overestimated due to the contact resistance and, as a consequent, the absolute threshold voltage is underestimated. We can improve the accuracy of these values, when we restrict the parameter analysis to very low drain voltages. As explained in section 5, we can then treat the channel as a typical resistor, which allows us to include contact resistance and a semi-empirical model for the mobility (equation (5.3)). For simplicity we rewrite equation (5.12) to

$$I_D = \frac{KV_D(V_G - V_T)^{\gamma+1}}{1 + KR_{SD}(V_G - V_T)^{\gamma+1}} \tag{8.4}$$

where $K = \mu_0 C_i W/L$ and R_{SD} is the contact resistance. Equation 8.4 provides an improved fitting model.

One option is to perform a least-square fit according using equation (8.4) directly with the measured transfer characteristics. For various reasons, the conditions for the model are not well-fulfilled for all gate voltage values. For example, direct contact resistance measurements show a strongly dependent contact resistance at low gate voltages that saturates at higher voltages [19, 25, 26]. Also the mobility will follow the semi-empirical power law only in limited gate voltage range. Thus, when a least-square fit is performed to the measured transfer curve without excluding these parts, where the model cannot be applied, the extracted parameters can strongly deviate from the actual quantities.

To avoid this problem, Natali et al. [23] have shown that the unknown parameters in equation 8.4 can be stepwise reduced until only the empirical constant γ and V_T are

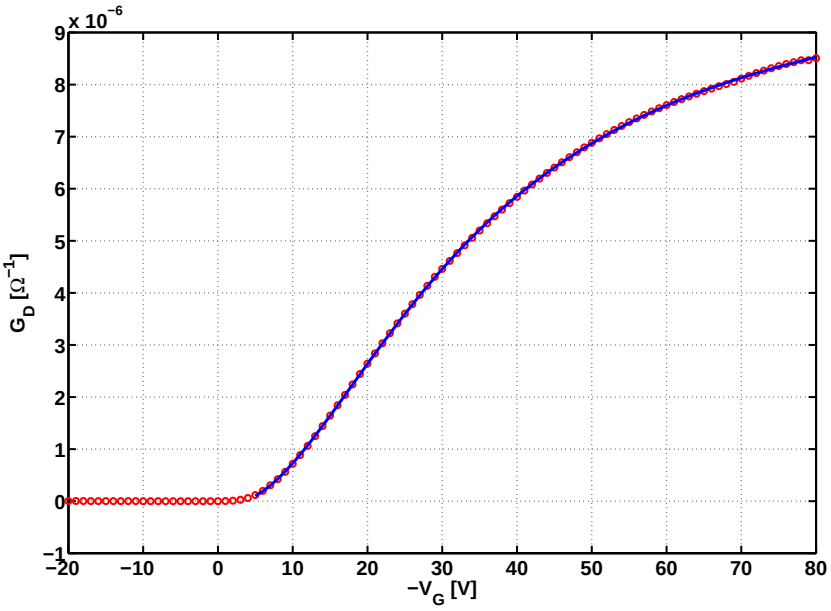


Figure 8.3.: Conductance versus absolute gate voltage. The solid line represents a least-square fit to equation 8.4.

left. When equation 8.4 is manipulated in the following way:

$$z = \frac{I_D^2}{\frac{dI_D}{dV_G}} = \frac{K}{\gamma + 1}(V_G - V_T)^{\gamma+2} V_D \tag{8.5}$$

$$w \simeq \frac{\int_0^{V_G} z dV_G'}{z} = \frac{1}{\gamma + 3}(V_G - V_T) \tag{8.6}$$

one obtain the function w and z, which can be used for the parameter extraction. It can be easily seen, that now the fitting procedure consists of only two linear fits. Furthermore, if all conditions for the applicability of the method are met, namely the mobility in from of equation 5.3 and constant resistance, the measured w function has to be a straight line with a slope between 0 and 1/3. In other words this method permits identifying directly the data ranges where it can be applied. As shown in figure (8.4), this is the case at high gate voltage values for P3HT transistors.

Additionally, the method allows us to extract a contact resistance by the following equation

$$R_{SD} = R_{tot} - R_{ch} = \frac{V_D}{I_D} - \frac{1}{K(V_G - V_T)^{\gamma+1}} \tag{8.7}$$

where R_{tot} is the total resistance and R_{ch} is the channel resistance. Equation 8.7 gives us values for the contact for the whole gate voltage range (figure 8.5). The values outside of the area of validity must be understood as extrapolation and do not necessarily reflect real physics.

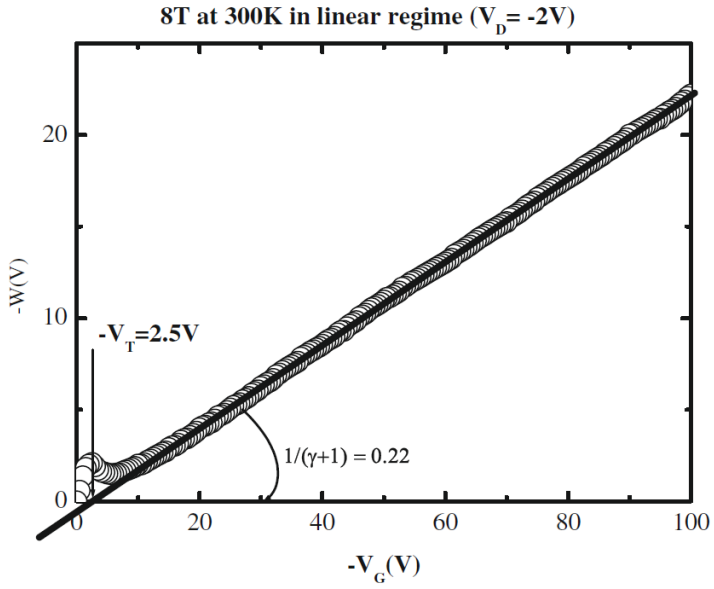


Figure 8.4.: Quantity w calculated using equation (8.6). For gate voltage higher than $15V$, w shows linear behavior and can be therefore fitted in this range. Picture take from Ref. [22].

8.5. Comparison

In this section, we apply all SFM methods on transfer lines, measured on the same device. Afterwards we compare the extracted parameters.

Two transfer characteristics at drain voltages of $-0.5V$ and $-25V$ have been measured on a pentacene OTFT with channel length of $25\mu m$ and a channel width of $7mm$. For the transfer characteristic at $V_D = -0.5V$, a fit according to equation 8.4 and equation 8.1 has been performed and the method after Natali et al. has been applied. The transfer characteristic at $V_D = -25V$ has been fitted with the linear model (equation 8.1) and the saturation model (equation 8.2). For the linear and saturation model fits, the Range Selection Algorithm has been used. The obtained parameters are listed in Tab. 8.1.

Table 8.1.: Comparison of extracted parameters for different methods. The least-square fit according to equation8.4 and the Natali Method have been applied for the voltage range between $-60 < V_G < -20$. The obtained contact resistance of the Natali Method is the average value of all contact resistance values in the voltage range. The exact contact resistance values are depicted in figure 8.5.

Methode Name	V_D $[V]$	V_{AT} $[V]$	μ_A $[cm^2/Vs]$	μ_0 $[cm^2/Vs]$	γ	R_{SD} $[\Omega]$
Saturation Model	-25	-15.3	0.039			
Linear Model	-25	-15.8	0.039			
Linear Model	-0.5	-15.4	0.030			
Fitting equation 8.4	-0.5	-9.6		0.0025	0.79	85.3 K
Natali et al	-0.5	-7.0		0.0017	0.84	106.0 K

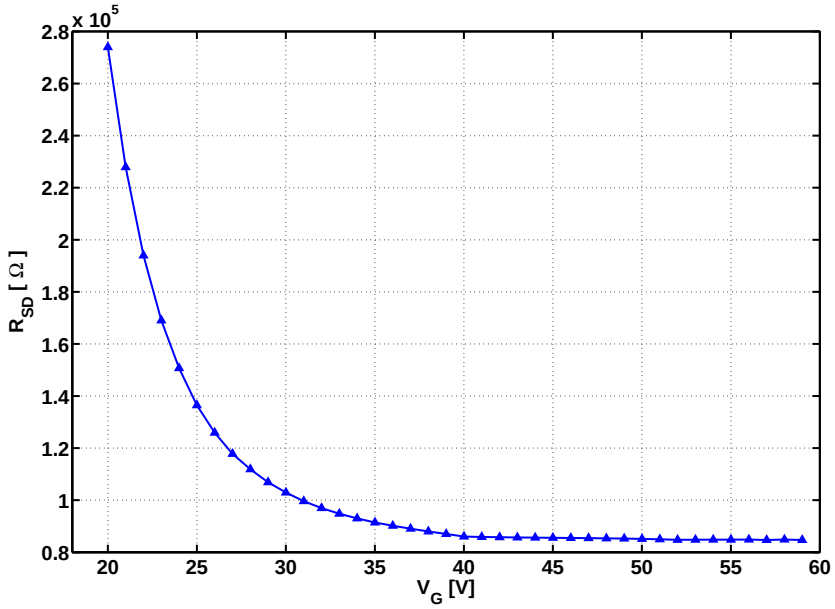


Figure 8.5.: Contact resistance versus gate voltage. Values obtained by the Natali method with equation 8.7. Transfer characteristic of a pentacene OTFT has been measured at $V_D = -0.5V$.

9. Contact Resistance Measurement

As already mentioned, the contact resistance affects the transfer characteristic in most cases in a not ignorable way. Furthermore, the gate bias dependent nature of the contact resistance does not allow a direct determination simply from transfer curves. Too many parameters would have to be introduced and would make a fitting the procedure problematic. For these reasons, direct measurement of the contact resistance seems to be unavoidable to identify the real physical quantities. In the following sections we introduce two methods for direct contact resistance measurements.

9.1. The Transfer Linie Method

One technique to separate channel resistance from contact resistance is the transfer line method [28, 27, 19]. This classical method for contact resistance estimation has already been adapted for amorphous silicon TFTs, and can be transfered in a straight forward manner to OTFTs. This method requires a series of transistor of different channel lengths, which are supposed to be produce under identical process conditions.

In the linear operating regime of the transistor, the channel resistance varies linearly with the channel length (equation 5.10). The contact resistance at source and drain is assumed to be independent of the channel length. The total resistance can be expressed as

$$R_{Total} = \frac{V_D}{I_D} = R_{Ch}(L) + R_S + R_D \tag{9.1}$$

where R_{Ch} is the channel resistance, and R_S and R_D are the contact resistances at the corresponding electrodes. When we now plot the total resistance as a function of the channel length, an extrapolation to zero gives us the sum of both contact resistance (figure 9.1).

This method is based on the assumption that all used samples have equal device parameters such as mobility, threshold voltage and contact resistance. Considering the fact that the parameter distribution of OFET processing is still not satisfying, the results of this methods must be treated very carefully. In addition, it cannot be excluded completely that the channel length has no impact on the contact resistance. For example, if the injection resistance does not exhibit a strictly linear V-I curve, it would change for a higher current caused by a smaller channel length. Therefore, it is recommend to proof the results with alternative methods of direct contact resistance measurements.

9.2. Four-Point Probe Method

An example of an alternative method is the Four-Point Probe Method (FPPM). The advantage over the TLM is, that only one sample is needed.

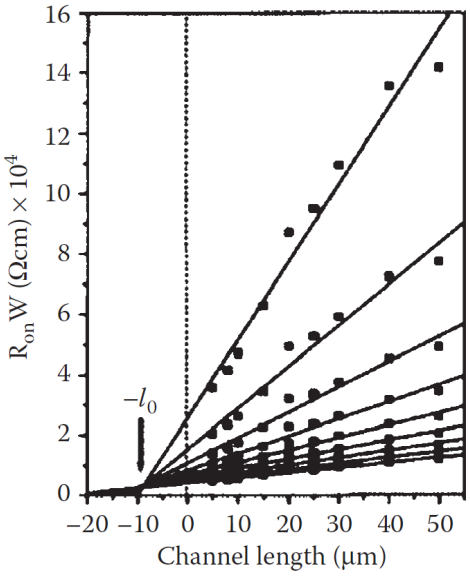


Figure 9.1.: Illustration of the transfer line method. Each line corresponds to a give gate voltage. Picture taken from Ref. [7].

The FPPM is realized by introducing two additional electrodes with distance D into the conducting channel [7, 45]. When a transfer curve is recorded, the voltage drop over the two additionally electrodes is measured as well. Assuming that the voltage drop across the channel is linear, the contact resistance can be estimated by:

$$R_{SD} = \frac{V_D}{I_D} - \frac{L}{D}\frac{V_{4w}}{I_D} \tag{9.2}$$

where L is the channel length and V_{4w} is the voltage drop between the electrodes placed inside the channel.

Another advantage of this method is, that drain contact resistance R_D and source contact resistance R_S can now be estimated independently, as illustrated in Fig 9.2.

9.3. Extracting Parameters from Channel Resistance Curves

In this section, we present two methods for extracting the mobility from the channel resistance curve. Because of the arguments presented in sections 5.3.1 and 5.3.2, it is not possible to derive an analytical expression for the channel resistance in the saturation or linear regime, except for very low drain voltages. Therefore, the transfer characteristic measurements are supposed to be performed at very low drain voltages. Once the contact resistance has been measured or estimated, the channel resistance follows directly by

$$R_C = R_{total} - R_{SD} = \frac{V_D}{I_D} - R_{SD} \tag{9.3}$$

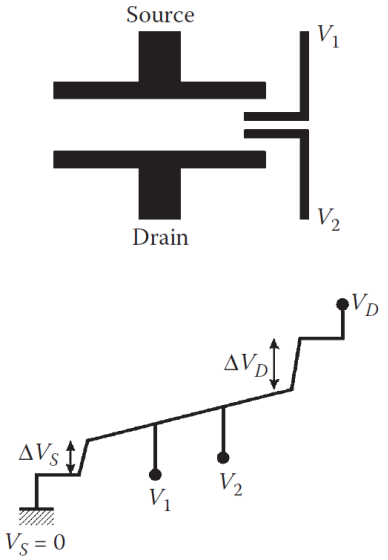


Figure 9.2.: Principle of the four-point probe method. Picture taken from Ref. [7]

where R_{total} is the total resistance and R_{SD} is the contact resistance at both electrodes. Moreover, at very low drain voltage the channel resistance is given by (see section 5.3.1):

$$R_{Ch} = \frac{L}{W}\frac{1}{\mu(V_G)C_i(V_G - V_T)} \tag{9.4}$$

Note, in this equation the mobility is gate bias dependent.

One way to extract the mobility is to rewrite equation 9.4 to

$$\mu(V_G) = \frac{L}{W}\frac{1}{R_{Ch}C_i(V_G - V_T)} \tag{9.5}$$

For this method the threshold voltage must be determined before the mobility. The critical point is that this method is very sensitive to the threshold voltage value. A threshold voltage slightly deviating from the real physical value would strongly affect the obtained mobility values; but how the threshold voltage can be precisely extracted is still a controversy debated field. The author of this work recommends to take the on-set voltage, i. e. that gate voltage in the log plot of the transfer line, where the drain current abruptly increases. In figure 9.3 mobility values estimated with three different threshold voltage values are plotted. Note that the gate bias dependent mobility obtained with the SFM threshold voltage exhibits a decreasing mobility with increasing gate bias. This confirms the statement that the SFM threshold voltage has nothing to do with the real threshold voltage.

Another method to extract the mobility out of the channel resistance is to differentiate both sides of equation 9.4:

$$\frac{d}{dV_G}\left(\frac{L}{R_{Ch}WC_i}\right) = \frac{d}{dV_G}\Big(\mu(V_G)(V_G - V_T)\Big) \tag{9.6}$$

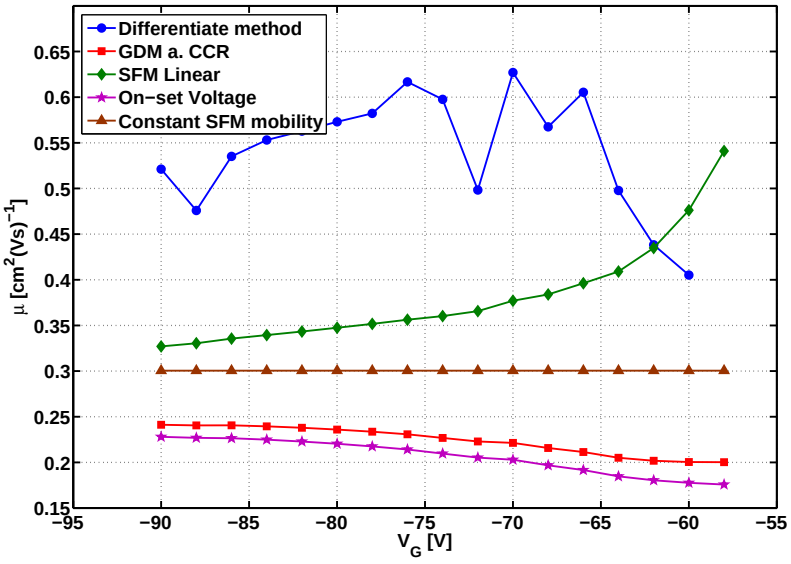


Figure 9.3.: Mobility dependence of gate voltage extracted from a channel resistance curve of pentacene OTFT with different methods. The diamond, square and star lines indicate mobility values obtained by equation 9.5, using different threshold voltages. The values obtained by the differentiate method (equation 9.8) shows a overestimation due to the negative term $d\mu/dV_G$. For comparison only, the constant mobility value obtained by the SFM linear method presented in section 8.1 is plotted (triangle).

$$\frac{L}{WC_i}\frac{d}{dV_G}\left(\frac{1}{R_{Ch}}\right) = \mu(V_G) + \frac{d\mu}{dV_G}(V_G - V_T) \tag{9.7}$$

If it is assume that gate voltage dependence of the mobility is very low, the second term on the right side in equation 9.7 can be neglected and the mobility becomes

$$\mu(V_G) = \frac{L}{WC_i}\frac{d}{dV_G}\frac{1}{R_{Ch}} \tag{9.8}$$

Figure 9.3 shows mobility values obtained from this method together with the constant mobility value obtained from the SFM linear method presented in section 8.1. Normally, the mobility values are overestimated, because the term $d\mu/dV_G$ is negative. Unfortunately, the gate voltage dependence cannot be neglected in all voltage ranges. Hence, this method must be applied very carefully. Nevertheless, it provides a way to extract the mobility without knowing the threshold voltage.

Part IV.

Bias Stress Measurements

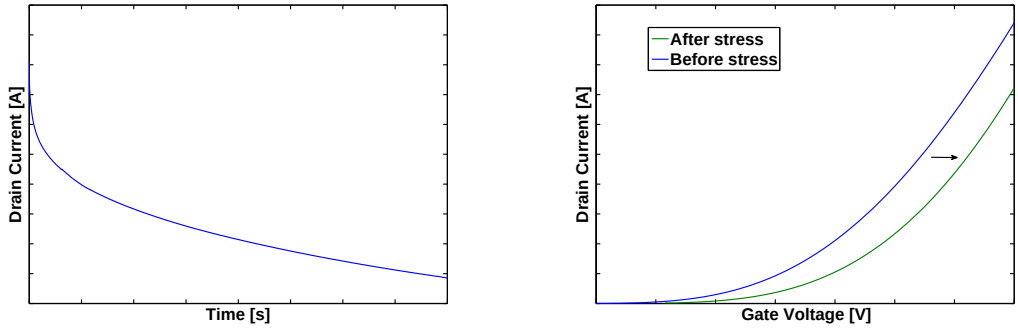
10. Bias Stress Effects

One of the greatest problems in OFET technologies, beside low mobilities and large contact resistance, is, that device parameters are not stable under operation. More precisely, the device parameters start to shift under applied gate bias. These phenomena are called *Bias Stress Effects* (BSEs). In general, the device parameter shift leads to a degradation of drain current over time, as shown in figure 10.1(a). BSEs are observed for most of the currently used organic semiconductors.

The drain current degrades mainly due to a shift of threshold voltage towards the applied gate voltage. A macroscopic explanation for BSE is, that when a carrier channel is created in a OFET by applying a gate voltage, some of the mobile charge in the channel will be trapped in deep trap sites and becomes immobile. These charges can no longer contribute to the current flow, even though they are still present in the channel and contribute to the charge balance. If then the gate voltage is switched off, the trap charges will not be released instantly. In fact, the release of the charge happens on a longer time scale. This results in a shift of the transfer characteristic after the stress compared to one measured before the device was stressed, as illustrated in figure 10.1(b). After infinite time of bias stress, an equilibrium state is reached. In the equilibrium state the charge trapping rate, that is how fast mobile charges transform to immobile ones, becomes zero. In most cases not all induced carriers are trapped in the equilibrium state, which indicates that also detrapping must occur during bias stress. An additional argument for detrapping are the measurements of Ucurum et al. in Ref. [36]. It was shown that the drain current increases under gate bias, when previously the device is stressed long enough with higher gate bias (figure 10.2). A detailed discussion about the time dependence of bias stress behavior will be presented in sections 10.2 and 10.3.

The degradation of drain current happens faster at high gate bias values. Hence, the charge trapping rates have to be dependent on the charge concentration. Also an applied drain bias changes the charge distribution at the semiconductor-insulator interface from uniform to decreasing from source to drain. The charge concentration at the drain electrode is decreased, while it stays constant at the source electrode. Consequently, applying drain bias also affects the BSE behavior. Recent measurements from Zschieschang at el. have shown that under applied drain bias the equilibrium state is reached much faster and that in the equilibrium state the number of trapped charges is lowered compared to unbiased case [34]. Zschieschang suggests that the applied drain bias does not only reduce the number of charge carries available for bias stress-induced trapping, but in addition creates a pathway for the fast release of trapped carriers. In contrast, Mathijssen at el. [39] have reported a drain bias independent bias stress behavior and that all charges are trapped in the equilibrium state.

Yet, the microscopic reasons of BSEs are not fully understood. Mostly, more than one microscopic reason is mentioned for bias stress-induced charge carrier trapping. Currently, the following possible microscopic reasons have been proposed:



(a) (b)

Figure 10.1.: Bias stress effect over 10 hours, measured on a top contact pentacene OFET: (a) Current degradation over time under inert conditions (b) the transfer curve shifts towards the applied voltage

- Measurements of different groups have shown the BSEs are stronger under ambient conditions [29, 30, 32]. It is assumed that oxygen and hydroxyl radicals generate new trap sites during the bias stress and thereby accelerate the trapping process.
- Apart from the environmental influences, impurities and structural properties of the organic material have an impact on the bias stress behavior [31].
- Raman spectroscopy measurements suggests that in organic molecule crystals also a deformation of the microscopic lattice happens during bias stress [37]. The deformation of the lattice affects the bias stress behavior as well.
- Finally, Paasch et al. stated in Ref. [38], that trapping are associated with the formation of biplarons. Thus, it should be an intrinsic phenomenon of the charge carrier transport in organic materials.

A threshold voltage shift has also been observed, when the transistor is deeply biased into the off-state (i.e., when a positive gate voltage is applied to a p-channel transistor). Knipp et al. have shown that for positive bias stress the equilibrium state is reached much faster than for negative bias stress [32].

Although, all measurements indicates, that the dominating effect in BS is the threshold voltage shift, caused by charge trapping, it cannot be excluded, that these trapped charges affect also other device parameters, such as the mobility.

10.1. Hysteresis

One consequence of BSEs is the appearance of hysteresis in measured device characteristics curves (figure 10.3). Hysteresis in OTFTs denotes the effect, that when a measurement is composed of a forward and backward voltage sweep, the current values of the two sweeps do not match. In most cases, the absolute current values of the first sweep are higher. The formation of hysteresis can be explained in the following way.

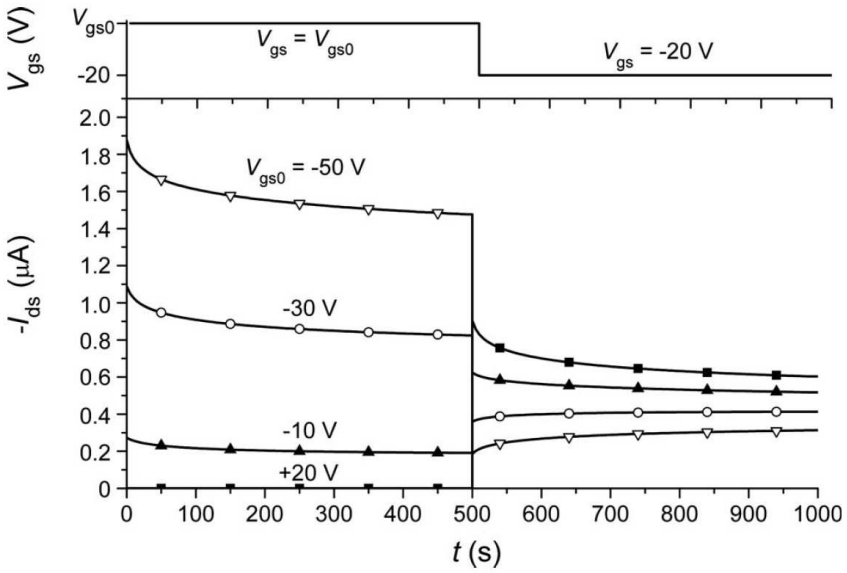
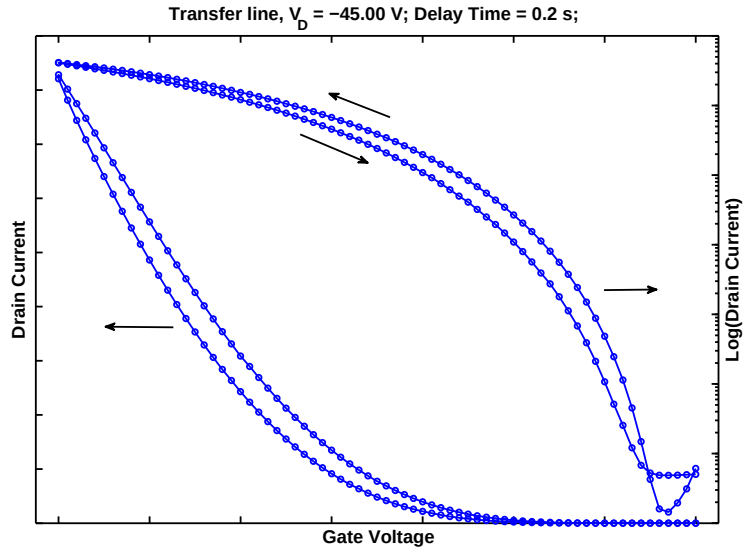


Figure 10.2.: Time dependent drain current under different gate bias stress. At $t = 500s$ the gate bias was switched to $V_G = -20V$. It can be easily seen, that the equilibrium state is lying approximately at $I_D = -0.5\mu A$. Picture taken from Ref. [36]

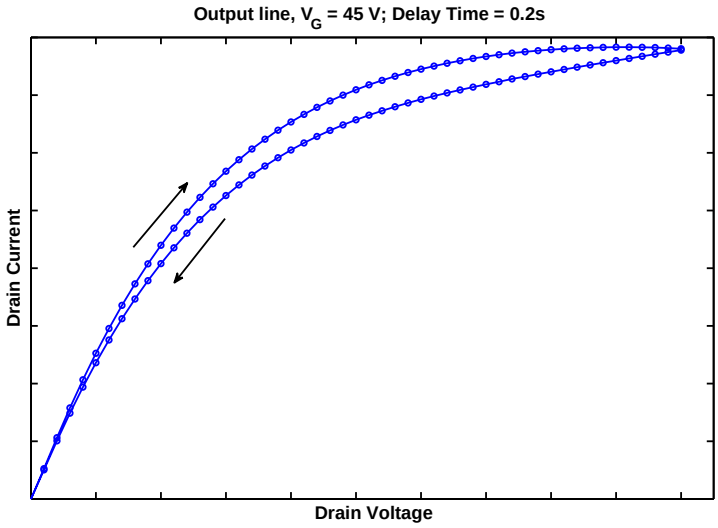
Every single measurement point in a transfer line needs a certain time to be measured by the measurement device. A lot of time passes between the measurements at equal gate voltage in the forward sweep and the backward sweep. During this time, the device is exposed to gate bias stress and the threshold voltages shifts due to charge trapping or detrapping at the semiconductor interface.

When an output characteristic is measured, the device is constantly stress during the full measurement cycle and the time evolution of threshold shift behaves as stated in the next sections. In the case of a transfer characteristic the situation turns out to be more complex. Generally, the device is stressed negatively and positively during the measurement cycle. Positively, when current values are measured at gate voltage values more positive than the threshold voltage and negative, when current values are measured at gate voltage values more negative than the threshold voltage. Hence, in some parts of the measurement cycle trapping occurs and in others detrapping. In what part detrapping and trapping occurs is strongly dependent on the sequence of the applied gate voltages. In order to provide an improved insight, we want to describe the most common measurement sequence, as it is depicted in figure 10.3(a). In that case, the measurement starts at gate voltages above the threshold voltage, goes in equidistant gate voltage steps to values deeply into the on-state, turns around and returns with the same step width to the starting point. For the description, the measurement cycle is separated into 4 parts:

1. In the voltage range between the starting point and the threshold voltage, the device is stressed positively and the traps will be discharged. This leads to degradation of current until the threshold voltage is reached.



(a)



(b)

Figure 10.3.: Hysteresis in a) transfer characteristics and b) output characteristics. Both characteristics measurement have been performed on pentacene OTFT.

2. From threshold voltage trough the highest gate voltage the number of induced carriers increases at each measurement point. Hence, the trapped-to-free charge ratio stays low in this part of the measurement. A low trapped-to-free charge ratio means that at every measurement step additional charge carriers are trapped. The threshold voltage shift and the measurement are in same directions. This leads to a continuous reduced of the slope of the transfer characteristics.

3. The next section ranges from the highest gate voltage back to the threshold voltage. At the beginning of this section, trapped-to-free charge ratio is still low and therefore the number of trapped carriers still increases. But with every single gate voltage step down, the number of total induced charge reduces. Therefore, the trapped-to-free charge ratio increases and at some point it reaches a certain level, where the trapping rate inverses and detrapping occurs. The detrapping causes a increase of the drain current and therefore the slope of the transfer curved shape is reduced in this range.

4. In the last section, a higher current in the backward sweep than in the forward sweep is observed. This is because charges are still detrapped and, thus, result in a current flow. A further noticeable point is that the threshold is shifted to more negative values meaning that in the whole measurement more charges has been trapped than detrapped.

In conclusion it can be said that the eventually measured shape of the transfer line is strongly dependent on the measurement sequence. The hysteresis phenomena make parameter extraction from a measured transfer characteristics more complicated. The device parameters, especially the threshold voltage, are not constant during the measurement of the transfer curve. Currently, there are no proposals in literature to meet this problem.

10.2. Stretched Exponential Model

The bias stress effect is also observed in α-Si and there has been investigated for two decades [40, 41, 42]. The threshold shift was found to be dominated by metastable state creation through diffusion of hydrogen atoms. The change of the trap density ΔN_s obeys following rate equation

$$\frac{d\Delta N_s}{dt} = -AD(t)\Delta N_s \tag{10.1}$$

where A is a constant of proportionality, and $D(t)$ is the time-dependent hydrogen diffusion coefficient. The detailed derivation of this rate equation is presented in Ref. [41]. The time dependence is due to the trapping and detrapping of the hydrogen with anomalously wide range of dwell times as it diffuses through the network. The dispersive diffusion coefficient is given by

$$D(t) = D_{00}(wt)^{-\alpha} \tag{10.2}$$

where D_{00} is a microscopic diffusion, w is a hydrogen attempt frequency, and α is the temperature-dependent dispersion parameter which is given by $\alpha = 1 - \beta = 1 -$

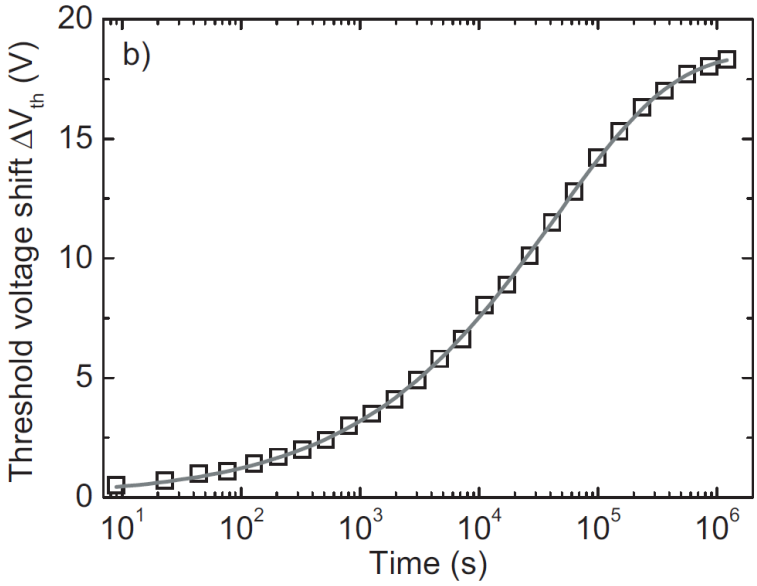


Figure 10.4.: Threshold voltage shift over time. The solid line represents a least-square fit to the stretched exponential model. Here, it is assumed that the threshold voltage shift after infinite time is equal to the applied voltage. Picture taken from Ref. [39].

T/T_0. The quantity $k_b T_0$ is the characteristic energy of the exponential distribution of trapping sites, and T is the measurement temperature. Solving equation 10.1 yields the characteristic stretched exponential

$$\Delta N_s(t) = \Delta N_s(0) e^{-(\frac{t}{\tau})^{\beta}} \tag{10.3}$$

with

$$\tau = \omega^{-1} e^{\frac{E_a}{k_b T}} \tag{10.4}$$

A stretched exponential model has been also applied to the threshold voltage shift in OTFTs [39, 43, 44]. Figure 10.4 shows an excellent fit of the model applied to the threshold voltage shift in PTAA transistors. Unfortunately, the underlying physic is still not well understood.

10.3. Analytical Discussion

In this section, we present an analytical investigation of the time dependence of the bias stress phenomena. We therefore establish the rate equation for free charge carrier according to observed measurement results and basic physical considerations. The solution of the rate equation shows the time dependence of free charge carriers under previously formulated assumptions.

10.3.1. Constant Rate Coefficient

First, we consider constant rate coefficients. The physical meaning of constant rate coefficients is that the trapping and release probability for each free charge carrier is not effected by any dynamic parameter during the whole process. The rate equation is then given by

$$\frac{dn_f}{dt} = -\lambda_1 n_f(t) + \lambda_2 n_t(t) \tag{10.5}$$

where n_f and n_t are the densities of free charges and trapped charges, respectively. The coefficients λ_1 and λ_2 represents probabilities of charge carrier trapping and releasing. For solving equation 10.5 we need to introduce the induced charge carriers density

$$n = n_f + n_t \tag{10.6}$$

The rate equation becomes

$$\begin{aligned} \frac{dn_f}{dt} &= -\lambda_1 n_f(t) + \lambda_2 \left(n - n_f(t)\right) && (10.7)\\ &= -\lambda_1 n_f(t) + \lambda_2 n - \lambda_2 n_f(t) && (10.8)\\ &= \underbrace{-\left(\lambda_1 + \lambda_2\right)}_{a} n_f(t) + \underbrace{\lambda_2 n}_{b} && (10.9) \end{aligned}$$

The solution for this differential equation can be easily found by the separation of variables method.

$$\begin{aligned} \int \frac{dn_f}{an_f + b} &= \int dt && (10.10)\\ \frac{1}{a}\ln\left|an_f + b\right| &= t + K && (10.11)\\ n_f &= \frac{Ke^{at} - b}{a} && (10.12)\\ n_f &= \frac{Ke^{-(\lambda_1+\lambda_2)t} - \lambda_2 n}{-(\lambda_1 + \lambda_2)} && (10.13) \end{aligned}$$

where K is the constant of integration. With the initial condition of $n_f(0) = n$, the constant becomes

$$\begin{aligned} n &= \frac{K - \lambda_2 n}{-(\lambda_1 + \lambda_2)} && (10.14)\\ \Rightarrow K &= -\lambda_1 n && (10.15) \end{aligned}$$

The time dependent free charge carrier density is then given by

$$n_f(t) = \frac{n}{\left(\frac{\lambda_1}{\lambda_2} + 1\right)}\left(\frac{\lambda_1}{\lambda_2}e^{-(\lambda_1+\lambda_2)t} + 1\right) \tag{10.16}$$

The relative free charge carrier density n_f/n for constant rate coefficients is plotted in figure 10.5.

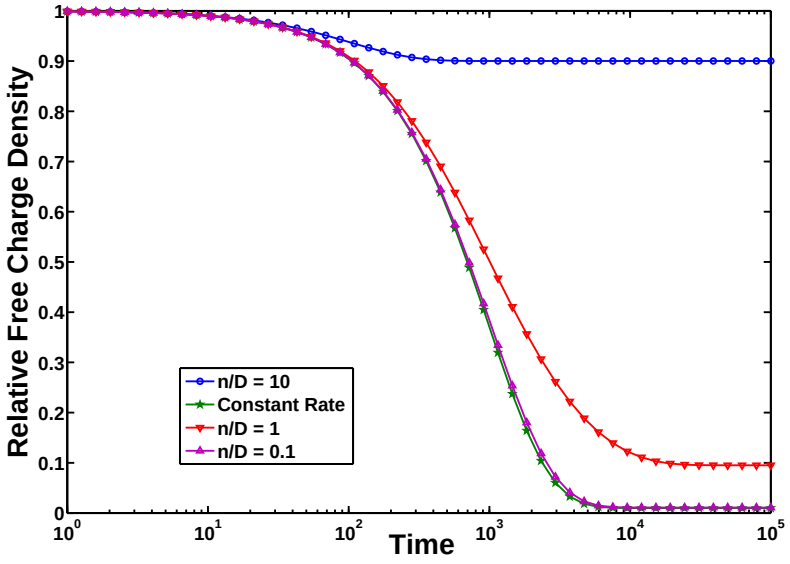


Figure 10.5.: Time dependence of the relative free charge density n_f/n for dynamic rate coefficients at different values of n/D, according equation 10.24, and for constant rate coefficients, according equation 10.16. The λ_1/λ_2 ratio was set to 100.

With equation 10.16 we can obtain information about the equilibrium state and its dependencies. After infinite time of bias stress, the density of free charge carriers is given by

$$n_f(\infty) = \frac{\lambda_2}{\lambda_1 + \lambda_2} n \tag{10.17}$$

Thus, when we assume constant rate coefficients, the number of free charge carriers in equilibrium state is proportional to the number of induced charge carriers, at which the proportional factor is determined by the ratio of trapping and detrapping probability.

10.3.2. Dynamic Rate Coefficient

Next, we assume that the number of trap sites are from the same or less order of magnitude than the number of induced charge carriers. In this case the probability for trapping is expected to be influenced by the number of trapped charges, i.e. the number of vacant trap sites. If all trap sites are occupied the probability for trapping tends to zero. Thus, the rate coefficient for trapping in equation 10.5 becomes time dependent. The detrapping probability is again assumed to be constant. The rate equation is then give by

$$\frac{dn_f}{dt} = -k(t) n_f(t) + \lambda_2 n_t(t) \tag{10.18}$$

where $k(t)$ is the dynamic rate coefficient. The more trap sites are occupied, the lower is the probability that a free charge carrier meets a unoccupied trap site. We therefore

postulate a simple proportional relation between the number of free trap sites and the probability:

$$k(t) = \lambda_1 \frac{D - n_t(t)}{D} \tag{10.19}$$

where D is the density of trap sites and λ_1 the constant probability of trapping when all trap sites are unoccupied. Subsituting equation 10.19 and equation 10.6 into equation 10.18, the rate equation becomes

$$\frac{dn_f}{dt} = -\left(\lambda_1 \frac{D + n + n_f(t))}{D}\right) n_f(t) + \lambda_2(n - n_f(t)) \tag{10.20}$$

$$\frac{dn_f}{dt} = \underbrace{-\frac{\lambda_1}{D}}_{a} n_f(t)^2 + \underbrace{\left(\frac{\lambda_1 n}{D} - \lambda_1 - \lambda_2\right)}_{b} n_f(t) + \underbrace{\lambda_2 n}_{c} \tag{10.21}$$

Again we solve the differential equation with the separation of variables method.

$$\int dt = \int \frac{dn_f}{an_f^2 + bn_f + c} \tag{10.22}$$

$$t + K = -\frac{2}{\sqrt{b^2 - 4ac}} \tanh^{-1} \frac{2an_f + b}{\sqrt{b^2 - 4ac}} \qquad \text{for} \qquad 4ac - b^2 < 0 \tag{10.23}$$

where K is constant of integration. The condition $4ac - b^2 < 0$ is always fulfilled, since λ_1 and λ_2 are positive and therefore the term $4ac$ becomes always negative. For simplicity we set $\beta = \sqrt{b^2 - 4ac}$. When we rewrite equation 10.23, the time dependent free charge carrier density has the following form

$$n_f(t) = \frac{\beta}{2a}\left(1 - \frac{2}{Ke^{-\beta t} + 1}\right) - \frac{b}{2a} \tag{10.24}$$

With the inital condition $n_f(0) = n$, we obtain for the constant of integration:

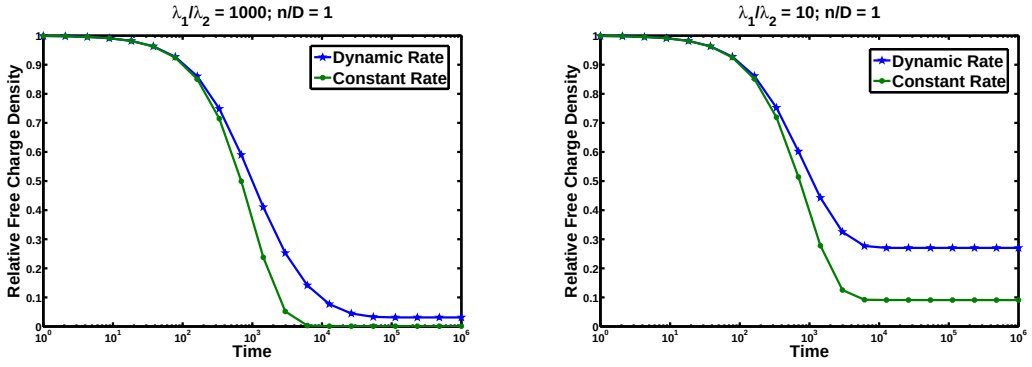
$$n = \frac{\beta}{2a}\left(1 - \frac{2}{K + 1}\right) - \frac{b}{2a} \tag{10.25}$$

$$\Rightarrow K = -\frac{2\beta}{2an - \beta - b} - 1 \tag{10.26}$$

This function is plotted for different ratios of n/D in figure 10.5. It turns out that for a small trap site density, i.e. one magnitude lower or equal than the induced charge carrier density, the time evolution of free charge density for dynamic rate differs strongly from that of constant rate. When the trap site density is increased, the curves becomes almost identical. Hence, the actual number of trap sites only plays a crucial role, when it is on the order of the number of induces carries or smaller. Figure 10.6 illustrates the influence of different ratios of λ_1/λ_2 on the time evolution curve.

Now, we again investigate the free charge carrier density at infinite time of bias stress.

$$n_f(\infty) = -\frac{\beta}{2a} - \frac{b}{2a} \tag{10.27}$$



(a) (b)

Figure 10.6.: Relative free charge density n_f/n with respect to the bias stress time for different λ_1/λ_2 ratios.

$$n_f(\infty) = \frac{D}{2\lambda_1}\left(\sqrt{\left(\frac{\lambda_1 n}{D} - \lambda_1 - \lambda_2\right)^2 + \frac{4\lambda_1\lambda_2 n}{D}} + \left(\frac{\lambda_1 n}{D} - \lambda_1 - \lambda_2\right)\right) \quad (10.28)$$

Unfortunately, the complexity of this expression prevent any qualitative statements, in what way the free charge carrier density in the equilibrium state is dependent of D and n. In order to still come to a conclusion, the equation 10.28 is used for the plot in figure 10.7. As expected, the number of free charges in the equilibrium state is increased, when the relative number of trap sites decreases.

At the moment, no experimental data concerning free charge carrier density in the equilibrium state are available in the literature. Measurements on this field could benefit informations about the underlying physical origins of the trapping process. A possible way to extract the free charge carrier density in the equilibrium state, without spending a lot of time for one measurement cycle, would be to perform a series of measurement as it was done by Ucurum et al. and is depicted in figure 10.2, and extrapolate the measured data to infinity.

10.3.3. Hysteresis Simulation

Here, we present a simple simulation of hysteresis by using equation 10.26 and 5.12.

The threshold voltage value changes during a measurement cycle of a transfer curve. Consequently, each measurement point i is assigned to a threshold voltage $V_T(i)$. The number of trapped charge carriers after the measurement of point i can be estimated by equation 10.24 with a given measurement time Δt, the induced charges $n = V_G(i)/C_i$ and the initial condition

$$n_f(0) = C_i(V_G(i) - V_T(i)) \quad (10.29)$$

The trapped carriers after the measurement point i and consequently for the next measurement point $i+1$ are then

$$n_t(i+1) = n - n_f(\Delta t) \quad (10.30)$$

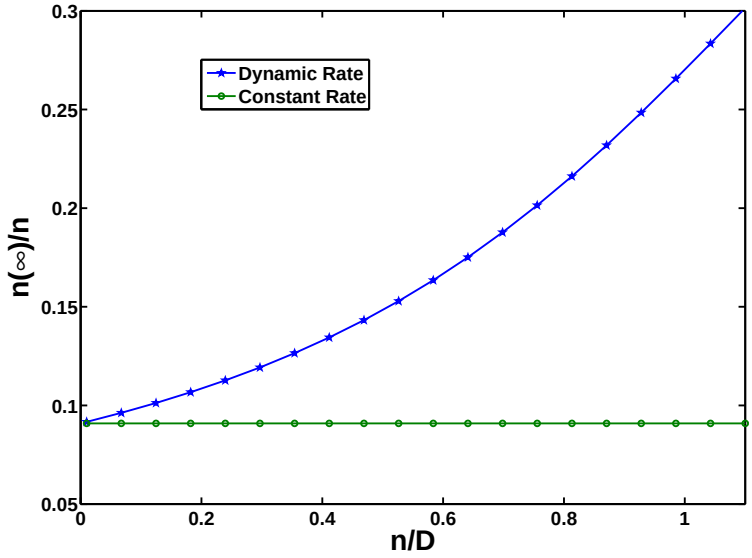


Figure 10.7.: Free charge density in the equilibrium state with respect to the trap site to induced charge ratio, according to equation 10.17 and equation 10.28.

The threshold voltage shift at measurement point i can be estimated by

$$\Delta V_T(i) = \frac{n_t(i)}{C_i} \tag{10.31}$$

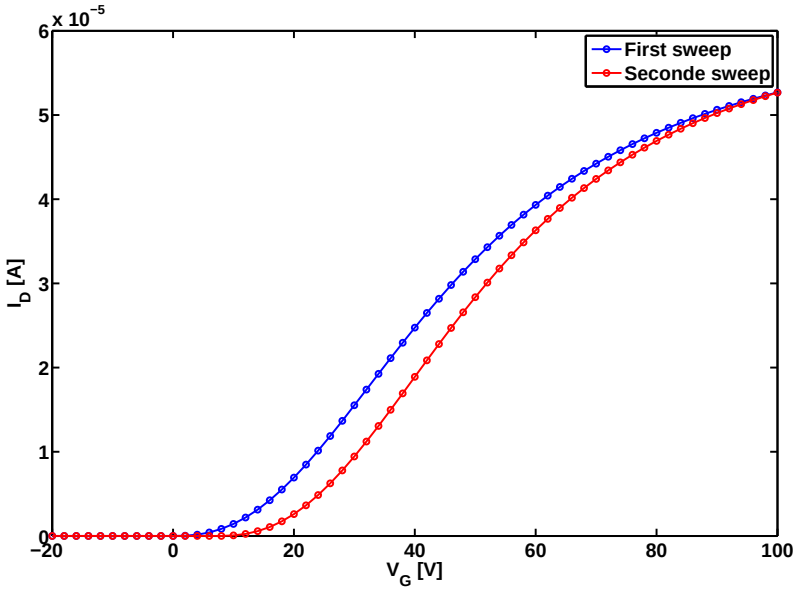
where $n_t(i)$ is the number of carriers trapped in the previous part of the measurement cycle. When equations 10.30 is divided by C_i, we come to a recursive equation for threshold voltage at measurement point $i+1$:

$$V_T(i+1) = V_G(i) - \frac{n_f(\Delta t)}{C_i} \tag{10.32}$$

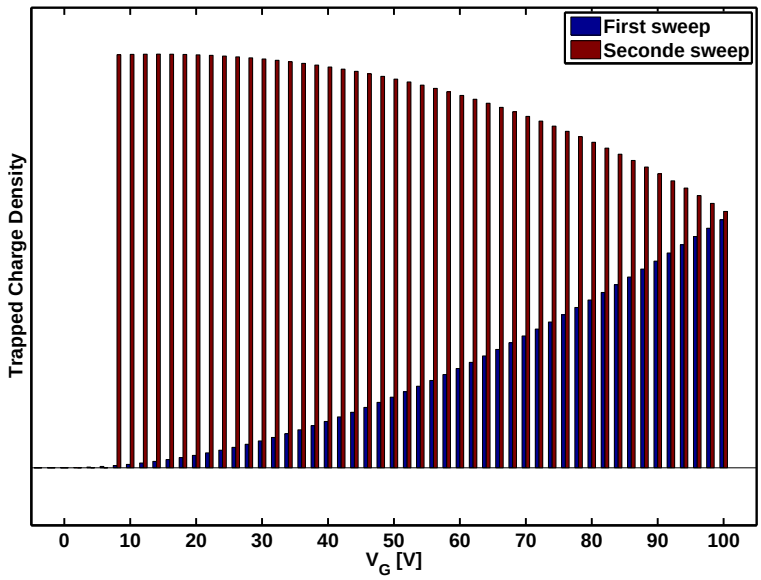
When now a sequence of gate voltages $V_G(i)$ is defined, the drain current value $I_D(i)$ can be estimated by substituting the corresponding threshold voltage $V_T(i)$ into equation 5.12. Figure 10.8 shows the result of a simulation. The parameter values chosen for the simulation are listed in table 10.1. The initial threshold voltage value was set to zero.

W/L	$\mu_0[/cm^2(Vs)^{-1}]$	γ	$C_i[nF/cm^2]$	$R_{SD}[\Omega]$	D/n_{max}	$\Delta t[s]$
280	0.011	1.5	24	8000	0.1	2

Table 10.1.: Chosen values for the simulation.



(a) Drain current vs gate voltage.



(b) Trapped charge density vs gate voltage.

Figure 10.8.: Hysteresis Simulation. Parameter values chosen for the simulation are listed in table 10.1. Note, in the gate voltage range from V_T to $-20V$ of the second sweep, detrapping dominates the trapping process and thus, the shift of threshold voltage is smaller in the second sweep.

11. Bias Stress Measurements at Room Temperature

This chapter deals with the general characteristics of the bias stress effect in pentacene OTFTs not yet considering its temperature dependence. In the first part of the chapter, the reversibility and the effect of the stress history is investigated. In the second part, it is inspected whether the charge trapping at the interface has an impact on device parameters other than the threshold voltage.

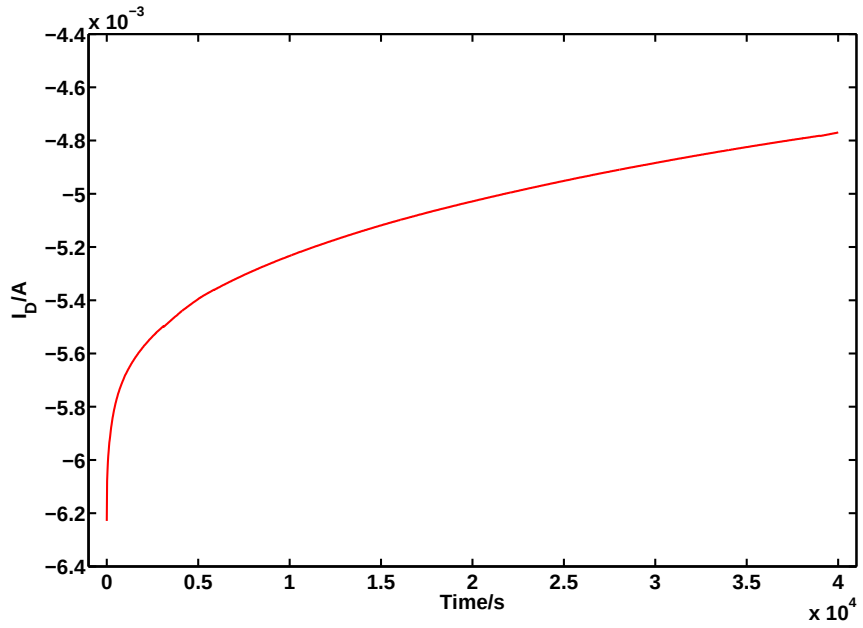
11.1. Evolution of Drain Current with Time

The first question that needs to be addressed is whether the bias stress behavior of the devices fabricated in our lab is similar to the behavior found in literature. Therefore, it has been decided to perform first simple drain current over time measurements under gate bias stress, before more sophisticated measurement procedures are established. Furthermore, it was investigated whether the stressed devices return to the initial state under inert conditions. In that context, it was also analyzed whether the bias stress behavior is affected by the stress history, that is the number and duration of the previous stress cycles.

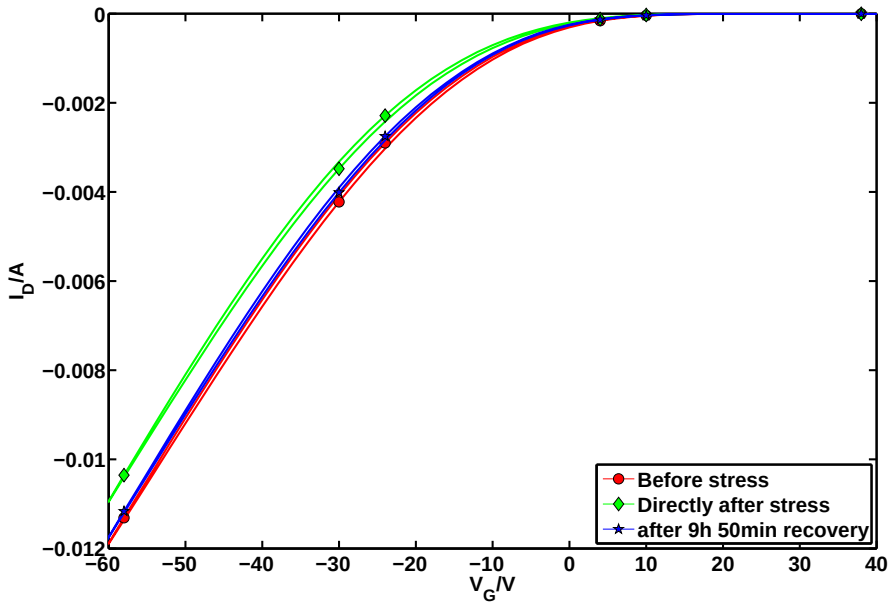
11.1.1. Reversibility

In the following a first long term bias stress measurement on a pentacene OTFT is presented (figure 11.1). The measurements were performed with an Agilent E5262A parametric analyzer. The electrodes were contacted with needles. The first problem that arises was that the electrical contact established by the needles was not stable enough for a long term measurement. In order to ensure a stable electrical contact, a drop of conductive silver was applied to the gold electrodes. This could not be done without exposure of the sample to air. The rest of the measurement took place in an argon glove box.

Previous to the bias stress measurement a transfer characteristic was recorded (figure 11.1(b)). Then a constant gate bias of $V_G = -40V$ and a constant drain bias of $V_D = -40V$ was applied for 40000 seconds, whereby the drain current value was measured every 20 seconds. The resulting time evolution of the drain current (figure 11.1(a)) matches well with that reported in Refs. [39, 37, 36]. Directly after the stress, another transfer curve has been measured. This curve exhibits a parallel shift towards more negative gate voltage values, as expected. Here, it has to take into account that the measurement of transfer characteristic consists of measurements of the drain current at various gate voltages. Hence, the obtained curve does not reflect the state of the OTFT at the end of the bias stress. In order to proof if the OTFT returns to its initale state,



(a) Drain current over time. Bias stress behavior is similar to that reported in Refs. [39, 37, 36].



(b) Transfer characteristics at $V_D = -45V$. After 10 hours of recovery the transfer characteristic has almost returned to the initale state.

Figure 11.1.: Bias stress measurement on a pentacene OTFT at $V_D = -40V$ and $V_G = -40V$ for 40000 seconds.

the sample has been stored under inert conditions and in darkness for almost 10 hours before the next transfer curve was recorded. The transfer curve after the recovery and the transfer curve before the stress are almost identical. The deviation from the initial curve lies in the area of the measurement inaccuracy, which is caused by the pressure of the glove box and the light in the lab. All transfer curves are depicted in figure 11.1(b).

11.1.2. Impact of Stress History

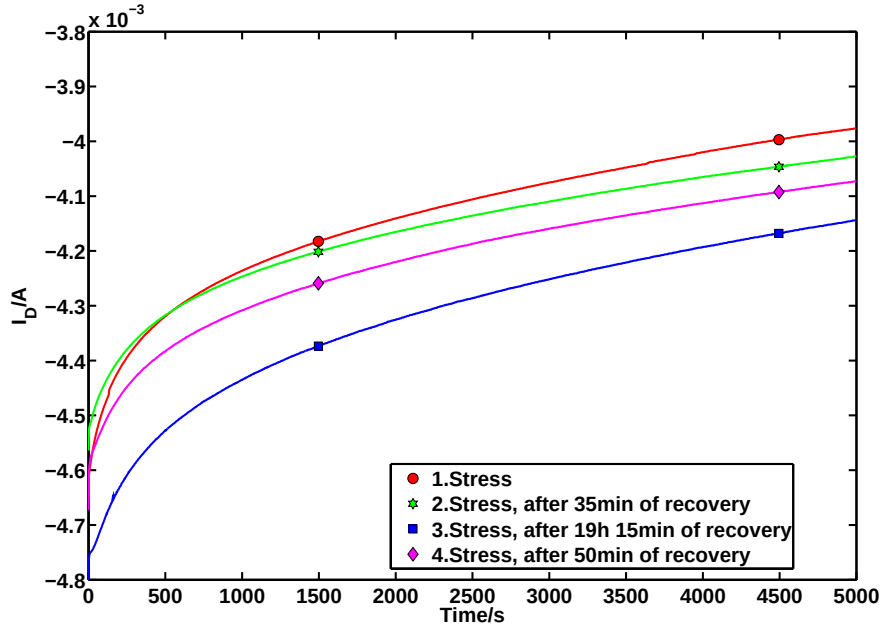
Next, it was investigated whether the stress history affects the time evolution of the drain current. In figure 11.2, four measurements are presented where again the drain current degradation over time is monitored. The measurement set up and the sample preparation were identical to the previous measurement. All measurements were performed on the same device. Between the bias stress measurements, the device was stored under inert conditions and in darkness. The stress parameters were again $V_D = -40V$ and $V_D = -40V$.

The red curve indicate the bias stress measurement of the pristine device, the rest of the curves display a series of measurements performed after different times of recovery. The recovery times for the second and fourth measurement were very short. As a result, the drain current degradation is visibly slower. For the third measurement, the duration of recovery for this measurement took more than 19 hours, the degradation was as fast as it was for the pristine device. This suggests that the short recovery time previous to measurement 2. and 4. was not enough for full recovery, in contrast to the third measurement. The similar result of the first and the third measurement justifies the assumption that the bias stress behavior is not affected by the stress history as long as one allows for sufficient recovery times. Additionally, it is observed that the drain current degradation at the beginning of the measurements is not exclusively dominated by the gate bias stress (figure 11.3(a)). Here, the superposed charging current affects the measured curve and/or the non-uniform progress of the drain current within the first 50 seconds suggests different underlying bias stress mechanism. In order to find a way to evaluate the measurement result quantitatively, a purely empirical model was used. The form of the model is

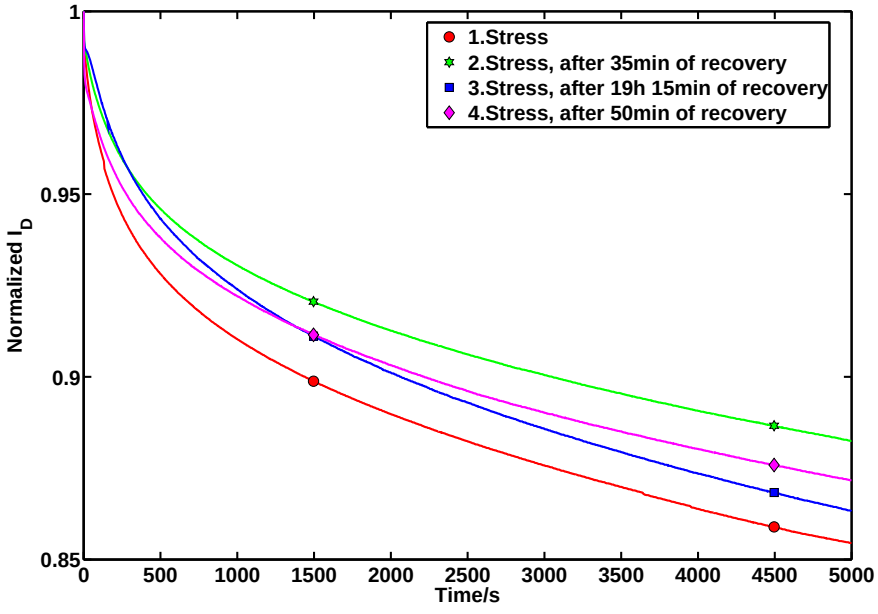
$$I_D = Ae^{-(t/\tau)^\beta} \tag{11.1}$$

where A, τ and β are empirical constants. A least-square fit was performed to all measured curves according to equation 11.1 (figure 11.3(b)). The obtained values are listed in Tab. 11.1. Because of the non-uniform progress at the beginning of the measurements, the first 100 seconds have not been used for the fit. The obtained values confirm the previous analysis. Parameter β is hardly effected by the history. In contrast, parameter τ is higher than the initial value for short recovery times and more or less equal for long recovery times. It seems that it contains information about the degree of recovery.

Unfortunately, the bias stress measurements have been performed in the saturation regime. It turned out that because of the complex situation we face in the saturation regime, it is not possible to apply one of the models from chapter 10.

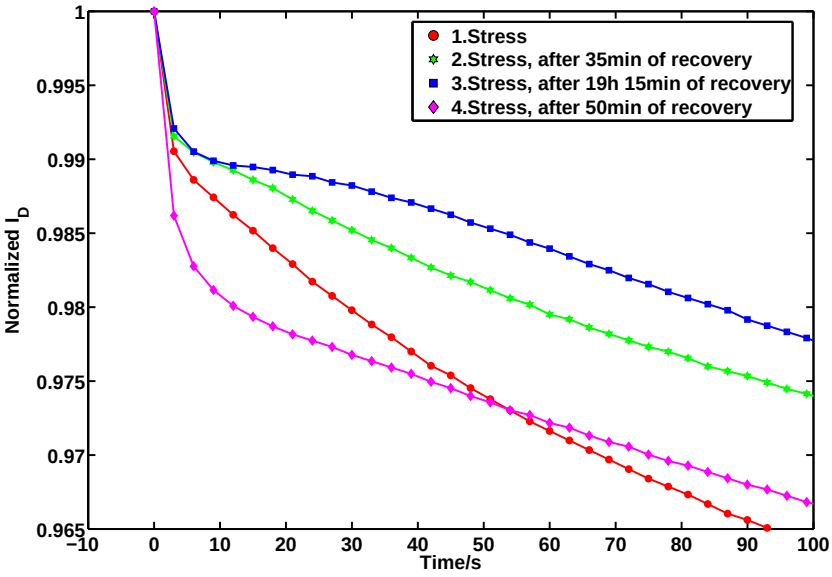


(a) Drain current over time.

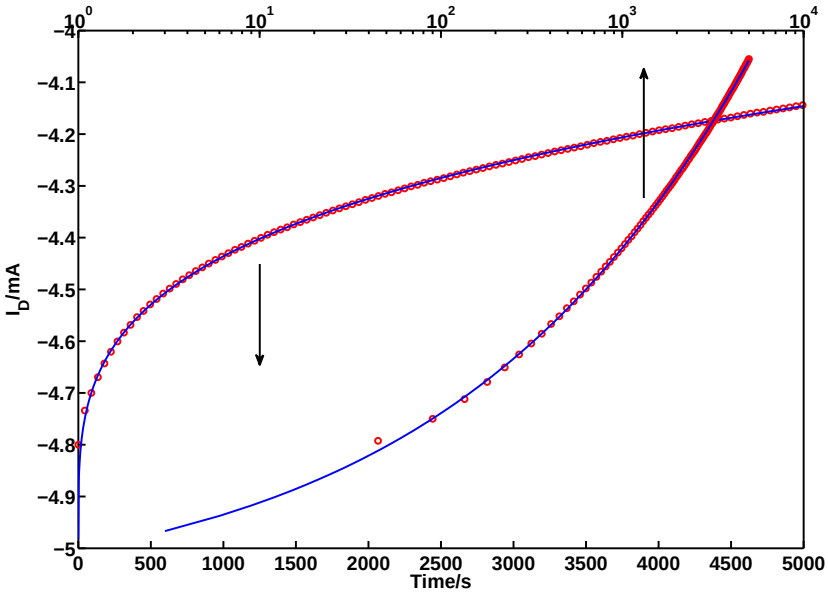


(b) Normalized drain current value over time

Figure 11.2.: Four bias stress measurements on the same device after different times of recovery. Stress parameters were $V_D = 40V$ and $V_G = 40V$.



(a) Normalized drain current values within the first 100 seconds. At the beginning the drain current degradation is not exclusively dominated by the bias stress effect.



(b) Drain current over time on a linear and logarithmic scale. The solid line represents a fit to equation 11.1.

Figure 11.3.: Fitting equation 11.1 to observed drain current degradation curves. Measurement points within the first 100 seconds have been ignored.

	$I_D = A\exp(-(t/\tau)^\beta)$		
Stress Nr.	A [A]	$\tau[10^4/s]$	β
1	-0.0047	266	0.27
2	-0.0046	550	0.27
3	-0.0049	190	0.28
4	-0.0047	387	0.28

Table 11.1.: Fit parameters according to equation 11.1. The first 100 seconds have been ignored.

11.2. Transfer Curve Measurement over Time

The next step was to analyze the total characteristics including the contact resistance of the OTFT during the bias stress. In other words, the effect of bias stress on the individual parameters of the OTFT should be monitored and ,consequently, it can be analyzed whether only a parallel shift of the transfer curve occurs. In order to meet this new requirements, a new measurement routine was designed:

- Interrupt the constant bias stress in equidistant time steps in order to measure a transfer characteristics. In the following we call this kind of bias stress measurement: Transfer Curve Measurement over Time (TCMT).
- For TLM contact resistance extraction, perform a TCMT measurement on samples with different channel lengths.

The drawback of this measurement routine is that the transfer curve measurement disturbs the time evolution of bias stress effect. The models presented in chapter 10 are only applicable if a constant gate bias is applied, but for a transfer curve measurement the gate voltage values need to be varied. Figure 11.4 illustrates the effect of transfer curve measurements on the bias stress behavior.

Two device with channel length of $25\mu m$ and $50\mu m$ were fabricated on the same substrate with a common gate. The software of the Aglient E5262A parametric analyzer was not capable enough to implement the new measurement routine. Hence, a LABVIEW program for controlling a KEITHLEY 2636 dual-channel source meter had to be developed. The whole experiment took place in a cryostat. The substrate is stored there in darkness and under high vacuum. For each device a TCMT measurement was performed. The transfer curves were recorded at $V_D = -0.5V$. The time interval between the transfer curve measurements was 300 seconds. The TCMT measurement were first preformed on the $50\mu m$ device. Because of the common gate the second device is stressed as well by the gate bias. Hence, before the TCMT measurement was performed on the $25\mu m$ device, it was waited until the device was fully recovered. In figure 11.5 some transfer curves gained by the TCMT measurement are depicted.

11.2.1. Time Evolution of Threshold Voltage and Mobility

First, the time evolution of the threshold voltage value and threshold voltage shift is investigated. For the extraction, the standard FET model (SFM) in linear regime and

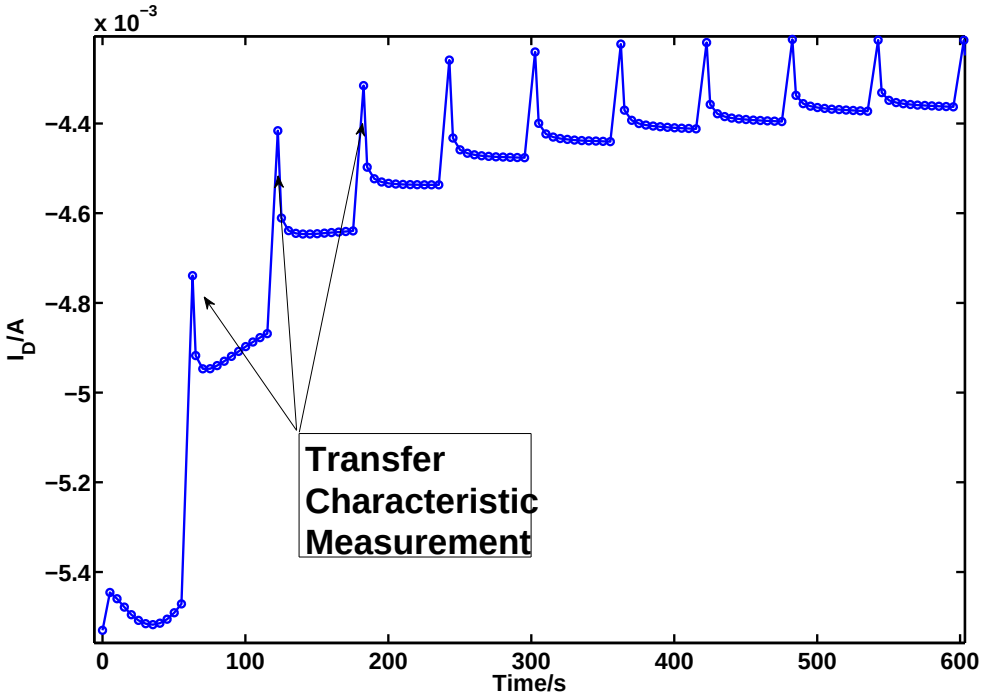


Figure 11.4.: Drain current dependence of time. Measuring transfer curves obviously affects the time dependence of the bias stress effect.

the gate bias dependent mobility and constant contact resistance model (GDM a. CCR) are used.

Additionally, a alternative method for extracting the absolute threshold shift has been developed. The idea behind this method is to shift one of two transfer curves along the gate voltage axis in very small steps until the best match of both transfer curve is reached. Therefore, a function of a gate voltage shift is defined by

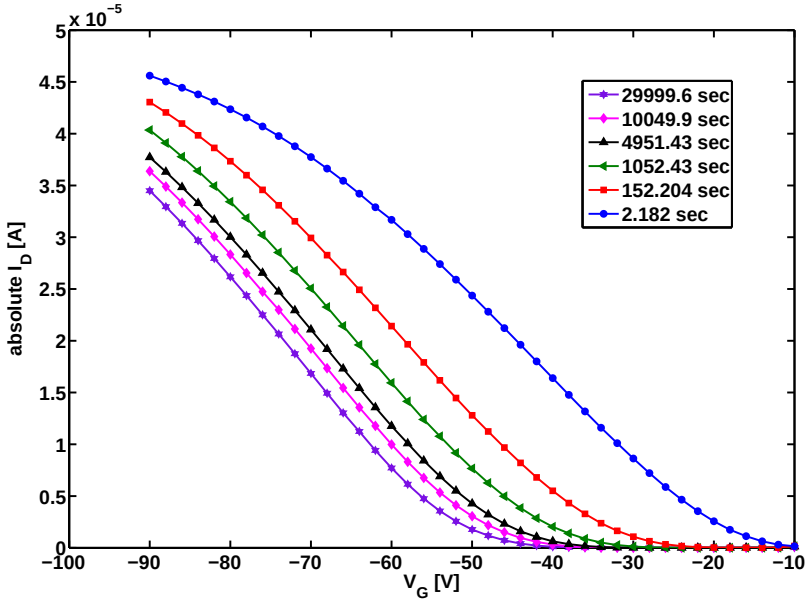
$$f(\Delta V) = \sum_{V_G} \left(I_{D,1}(V_G) - I_{D,2}(V_G - \Delta V)\right)^2 \tag{11.2}$$

where $I_{D,1}(V_G)$ and $I_{D,2}(V_G)$ are the measured transfer characteristics. The minimum of this function represents the voltage shift where the best match is obtained and, consequently, it is defined as the absolute threshold voltage shift between two transfer characteristics

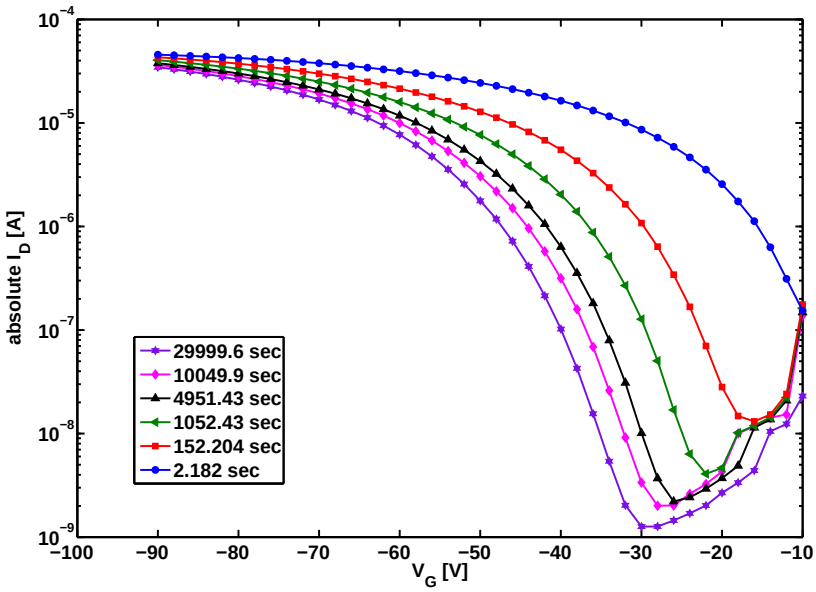
$$\Delta V_T = \min \left[\sum_{V_G} \left(I_{D,1}(V_G) - I_{D,2}(V_G - \Delta V)\right)^2 \right] \tag{11.3}$$

Note that this method gives only the threshold shift. In the following this method is called the least square method (LSM).

The obtained time evolution of the threshold voltages V_T is shown in figure 11.7 and figure 11.8 for channel length $L = 50\mu m$ and $L = 25\mu m$, respectively. The time evolution



(a) Linear plotted transfer curves.



(b) Logrithmic plotted transfer curves.

Figure 11.5.: Shift of the transfer curves during a constant gate bias of $V_G = -60V$. Measurement was performed on the device with channel length $L = 25\mu m$. The legend values indicates the time when the transfer curve measurement ends.

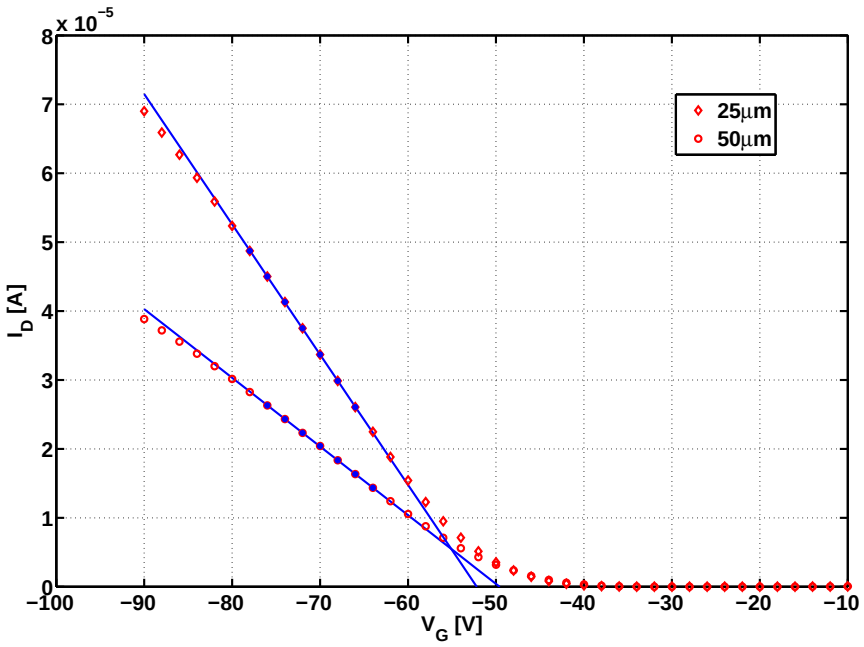


Figure 11.6.: Two fits with SFM linear method for two different channel lengths. Both transistors are fabricated on the same substrate and exhibit the same on-set voltage. However, the threshold voltages, which are extracted with SFM method linear, are not the same.

of relative threshold voltage obtained from the GDM a. CCR method interpolates very good the relative values of the on-set voltage. The threshold voltage shift ΔV_T is depicted in figure 11.9 and figure 11.10. For the on-set voltage the threshold shift cannot be estimated, because the on-set of the first transfer line is not located in the gate voltage sweep range (figure 11.5). Here, the SFM method shows very good agreement with the LSM method.

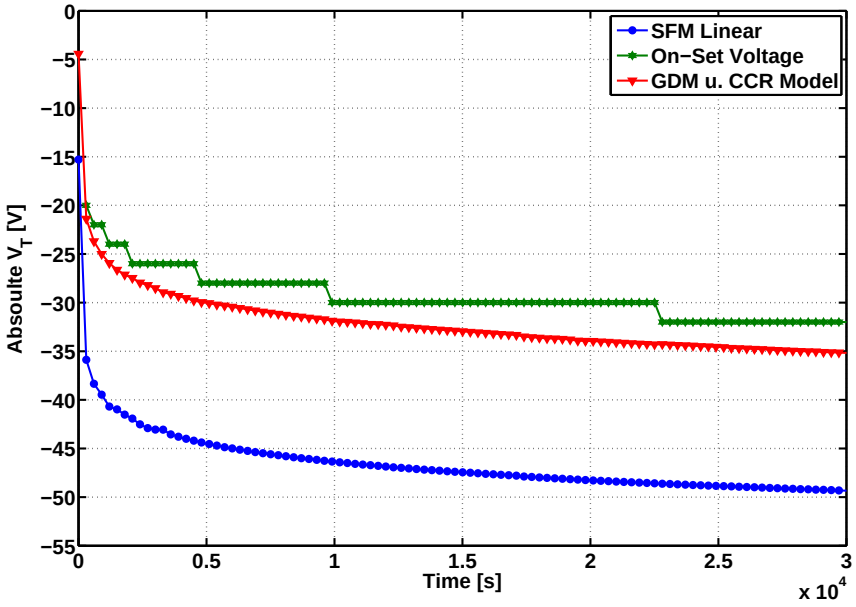
In figure 11.11 and figure 11.12 the values for both channel lengths are combined. The on-set voltage and the threshold shift determined by the LSM are almost equal for the different channel lengths during the TCMT measurement, which suggests that the threshold is equal and shifts with the same rate in both devices. For the SFM and GDM u. CCR methods, the obtained values deviate from each other. This deviation illustrates the channel length dependent of both methods. A smaller channel length leads to a higher threshold voltage, as shown in figure 11.6. For the GDM u. CCR method we face a similar situation. The logarithmic plots (figure 11.11(b), figure 11.12(b)) show that the shifts follows a logarithmic law.

Next, it is investigated whether the shift of the transfer curve is only parallel or the shape of the transfer curve changes as well during the bias stress. In figure 11.15 transfer lines shifted about the threshold voltage are plotted, whereby the threshold value form the GDM a. CCR method is used. In the logarithmic plot (figure 11.15(b)) it can be seen that all on-set voltages match each other, which confirms the obtained values of the

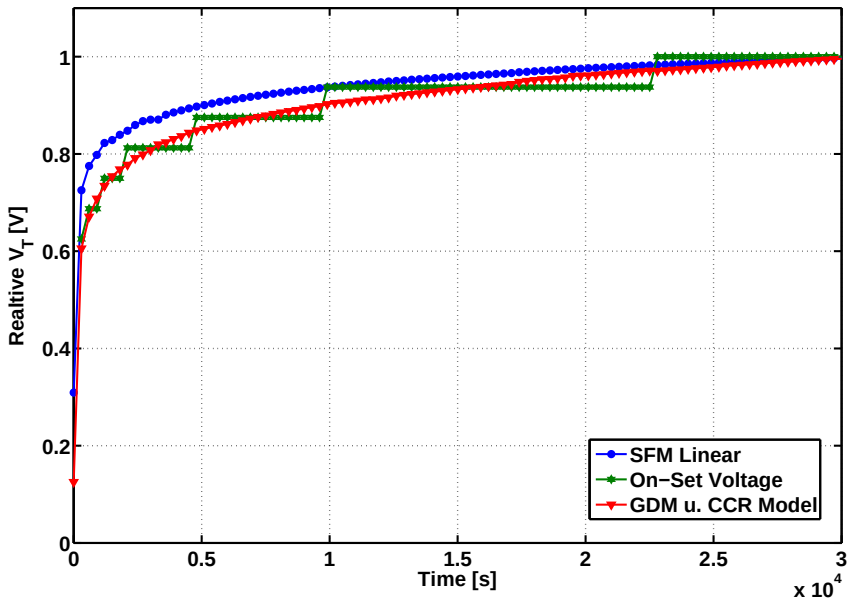
threshold shift. Similar results are obtained for the SFM method. The accuracy of the match is better for threshold values obtained from the $L = 50\mu m$ device. In the linear plot it can be seen that the shape of the transfer line changes (figure 11.15(a)). The slope of the transfer line increases with increasing time of the stress. Figure 11.13 shows the time evolution of the mobility of the both devices. The mobility values are obtained form the SFM and GDM u. CCR method. From the SFM method, an average value for the fitting range is obtained. In the case of the GDM u. CCR method, the fit provides the parameter of equation 5.3. In order to compare these methods, a mobility value for $V_G - V_T = -45V$ was estimated with equation 5.3.

The constant contact resistance values obtained from the GDM a. CCR method are plotted in figure 11.14. The values deviate strongly for the different channel lengths. Since the rest of the parameters provided by the GDM a. CCR method matches very well, this could indicate that the contact resistance depends on the drain current and consequently on the channel length. Also the obtained values support this assumption. The drain current of the 25 μm device is higher, but the contact resistance is smaller. Another noticeable point is that the first contact resistance value is overestimated for both channel lengths. This is because the threshold voltage shift in the first measurement leads to an downward bending of the transfer curve. The fitting routine interprets this as higher contact resistance.

Summarizing the results of these measurements, it is found that under bias stress, the transfer curve shifts to more negative gate voltage values and its slope increases. This agrees with reported results form Refs. [34, 35]. While the shift parallel to the gate voltage axis is caused clearly by the threshold voltages shift, the increased slope of the transfer curve can have two different reasons: increase of the mobility and/or decrease of the contact resistance. In order to resolve the exact process, measurements, which allows to separate channel and contact effects, are needed.

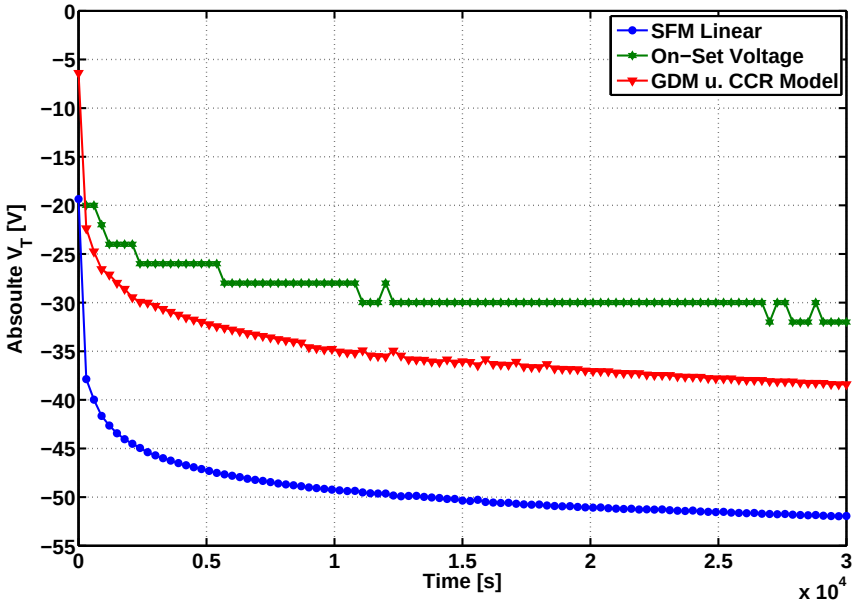


(a)

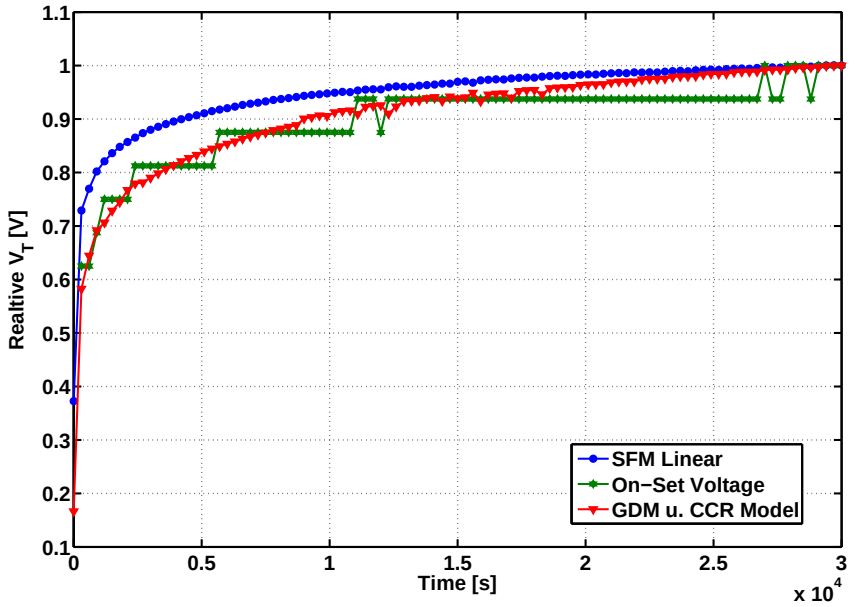


(b)

Figure 11.7.: Time evolution of (a) absolute threshold voltage and (b) relative threshold voltage measured in the pentacene OTFT with channel length $L = 50\mu m$. The discontinuities of the on-set voltage arises because, the on-set voltage can be determined as accurate as the steps in the gate voltage sweeps.

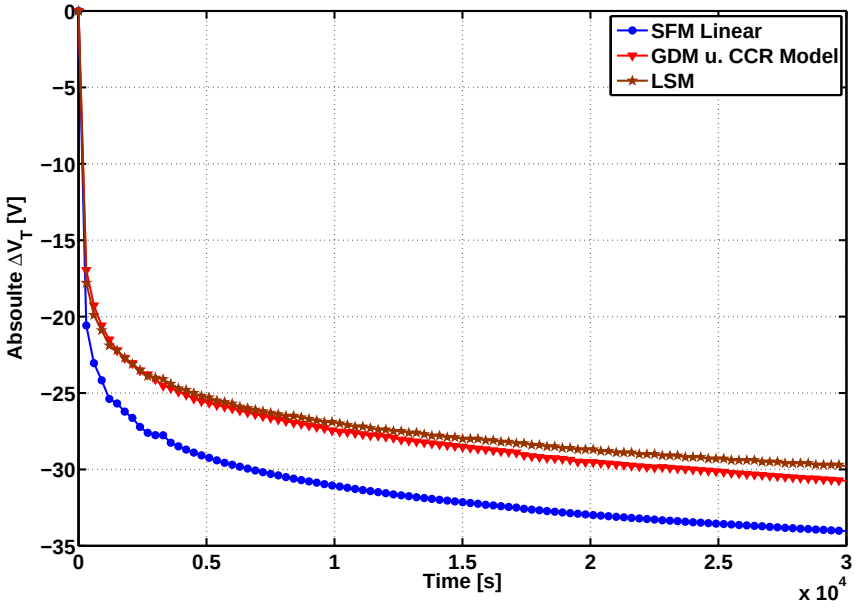


(a) Absolute threshold values vs. Time.

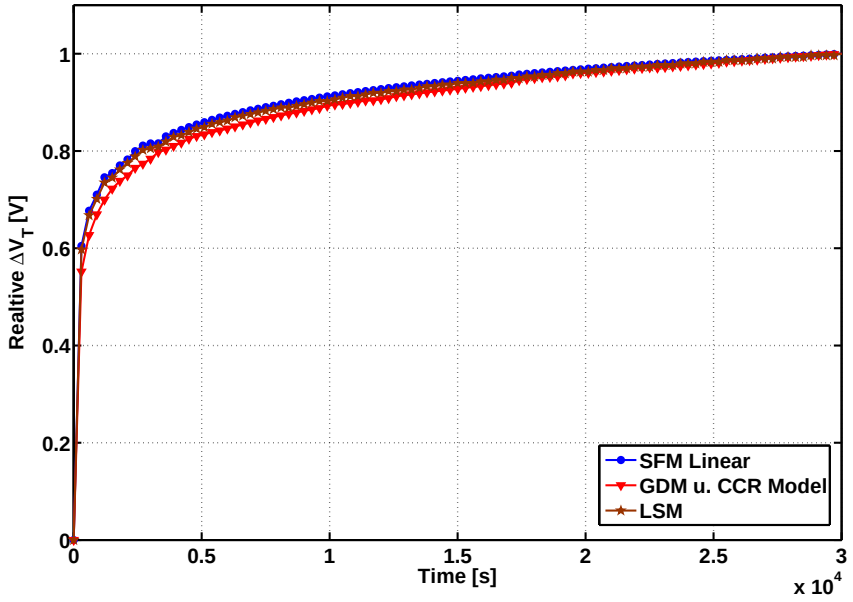


(b) Relative threshold values vs. Time.

Figure 11.8.: Time evolution of (a) absolute threshold voltage and (b) relative threshold voltage measured in the pentacene OTFT with channel length $L = 25\mu m$. The discontinuities of the on-set voltage arises because, the on-set voltage can be determined as accurate as the steps in the gate voltage sweeps.

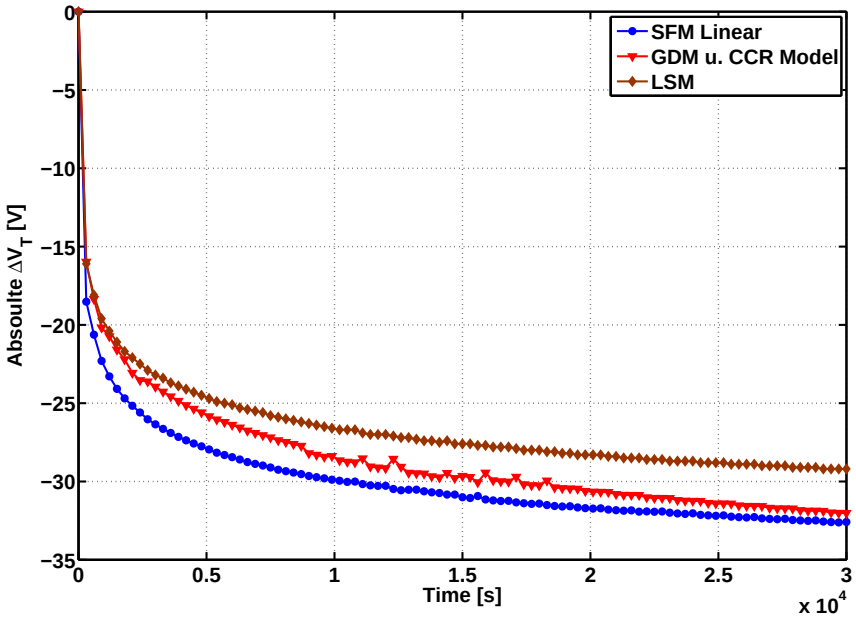


(a)

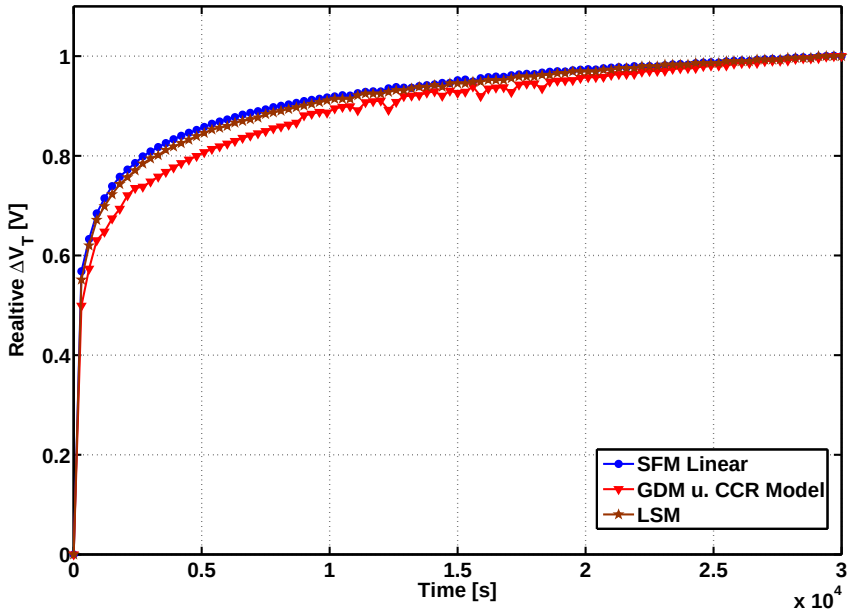


(b)

Figure 11.9.: Time evolution of (a) absolute threshold voltage shift and (b) relative threshold voltage shift measured in the pentacene OTFT with channel length $L = 25\mu m$.

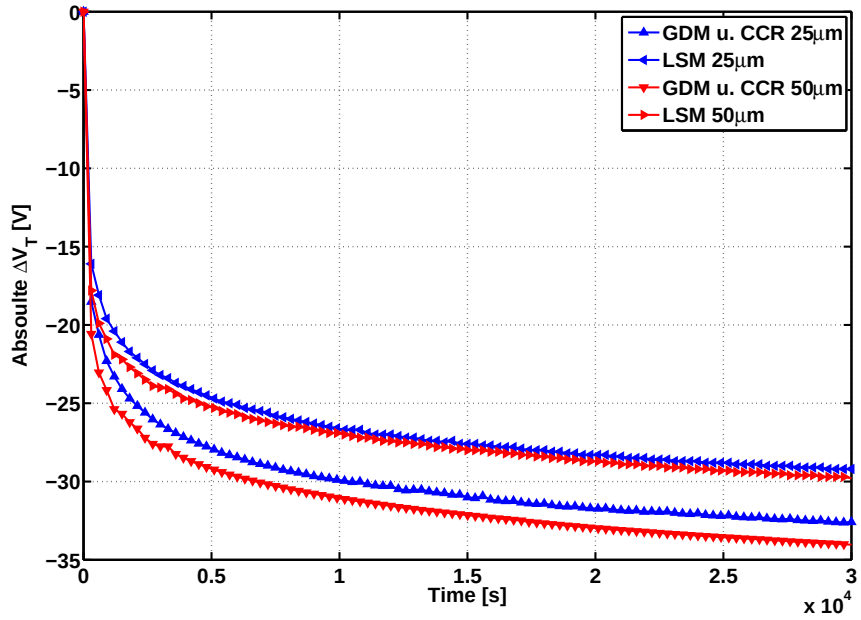


(a)

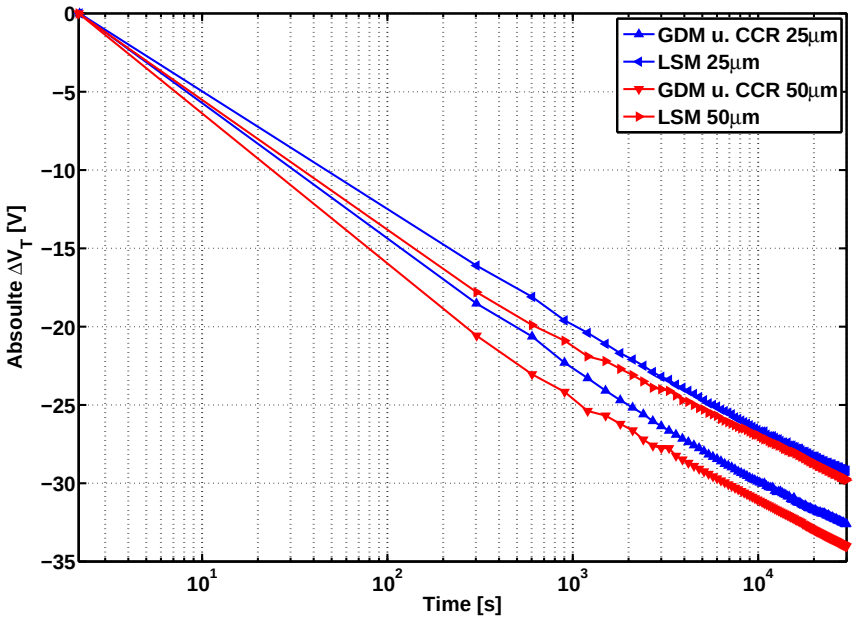


(b)

Figure 11.10.: Time evolution of (a) absolute threshold voltage shift and (b) relative threshold voltage shift measured in the pentacene OTFT with channel length $L = 25\mu m$.

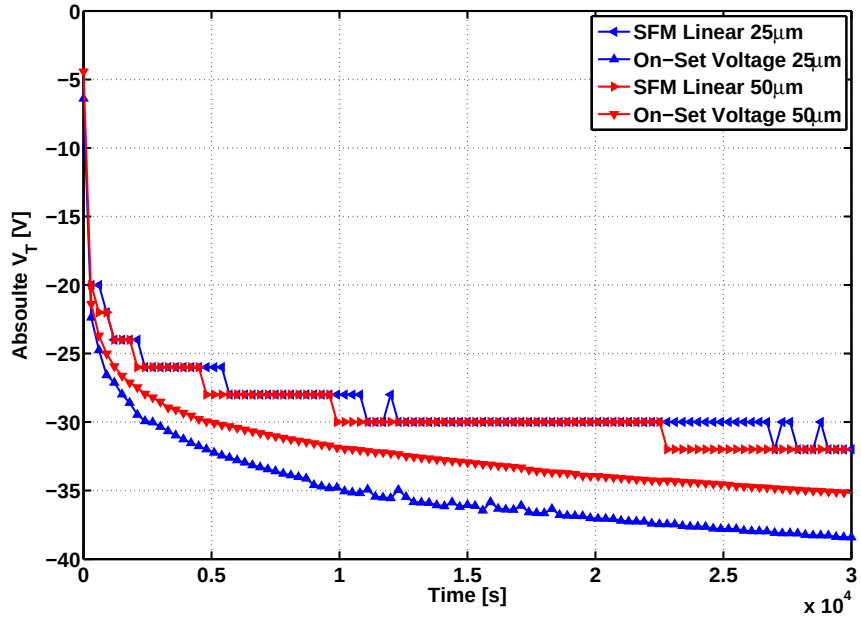


(a) Linear plot of absolute threshold shift vs. Time.

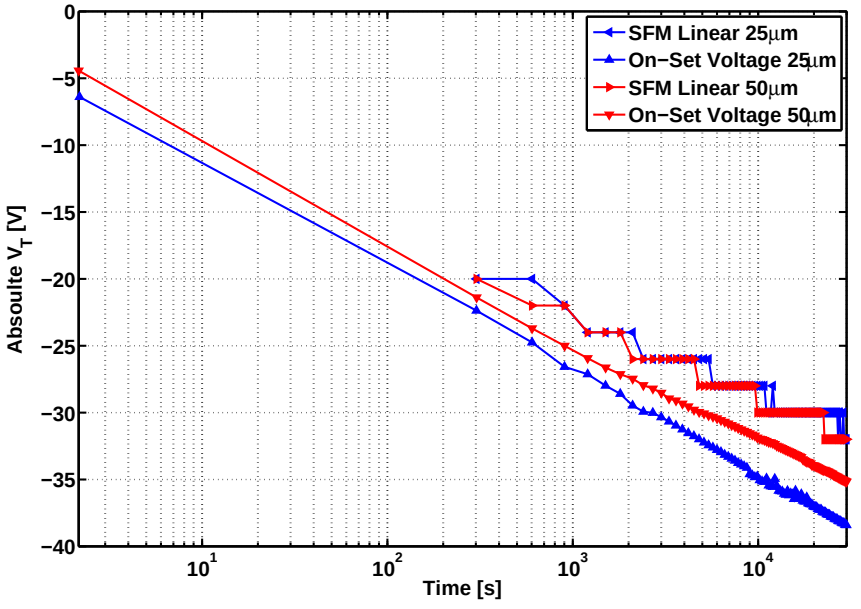


(b) Logarithmic plot of absolute threshold shift vs. Time.

Figure 11.11.: Threshold shift for channel length $L = 25\mu m$ and $L = 50\mu m$, extracted with LSM and GDM u. CCR Model.



(a) Linear plot of absolute threshold shift vs. Time.



(b) logarithmic plot of absolute threshold shift vs. Time.

Figure 11.12.: Threshold voltage and on-set voltage for channel length $L = 25\mu m$ and $L = 50\mu m$, extracted with SFM linear model.

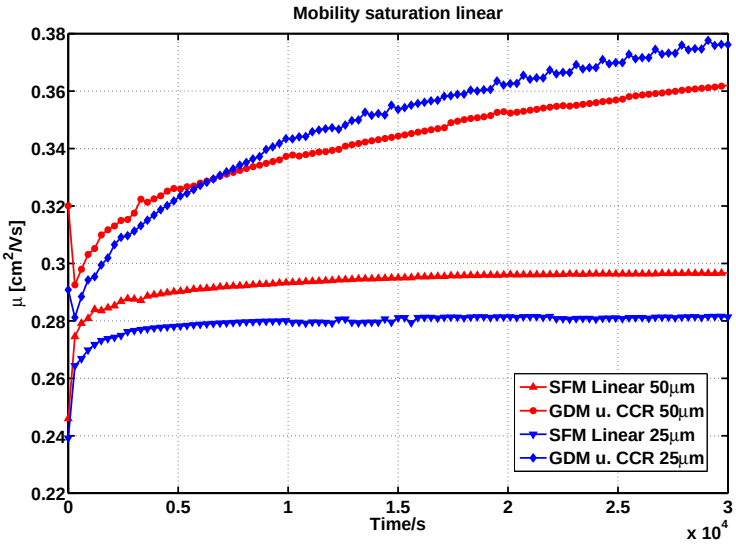


Figure 11.13.: Mobility vs Time; Comparison of the mobility values of GDM a. CCR and SFM linear method. Mobility values obtained from the GDM a. CCR method are estimated by $\mu = \mu_0(-45V)^{\gamma}$. Note that the mobility increases during the bias stress.

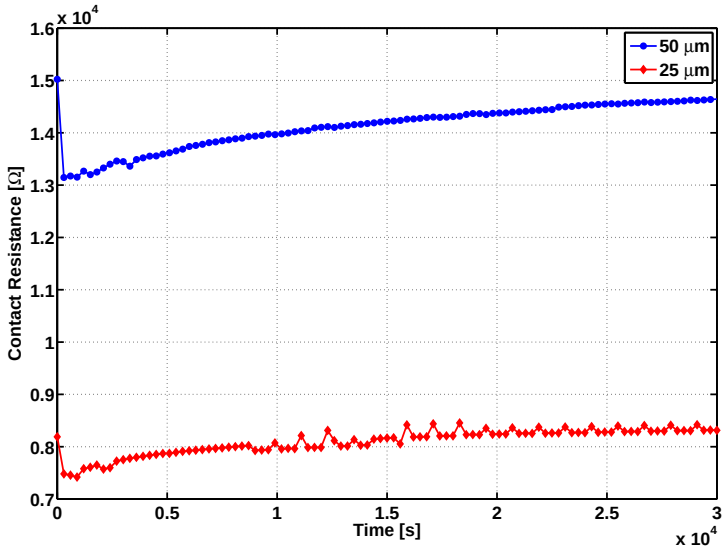
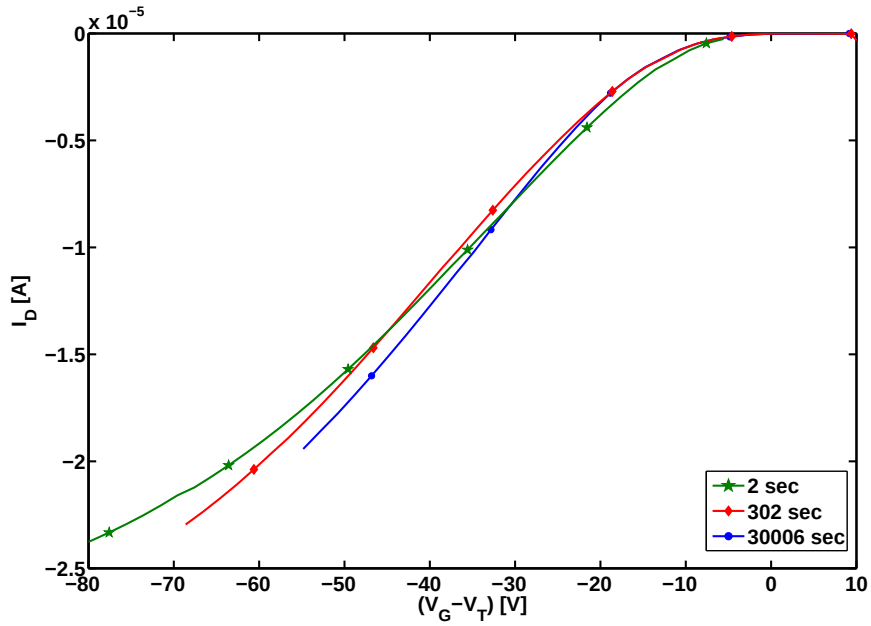
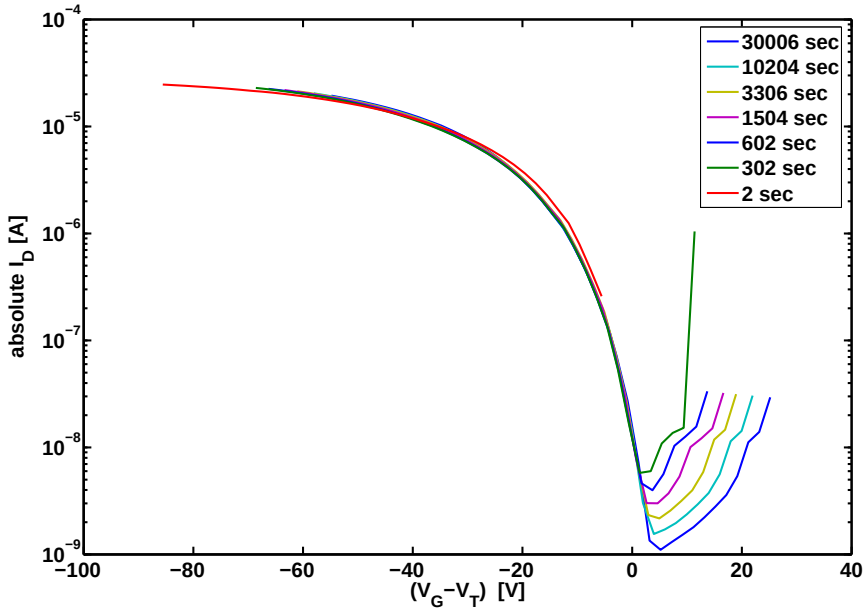


Figure 11.14.: Constant contact resistance obtained from the GDM a. CCR method for both channel lengths. Although the other parameters



(a) Linear plot of drain current vs. $(V_G - V_T)$ at different times. Shift of transfer line is not parallel.



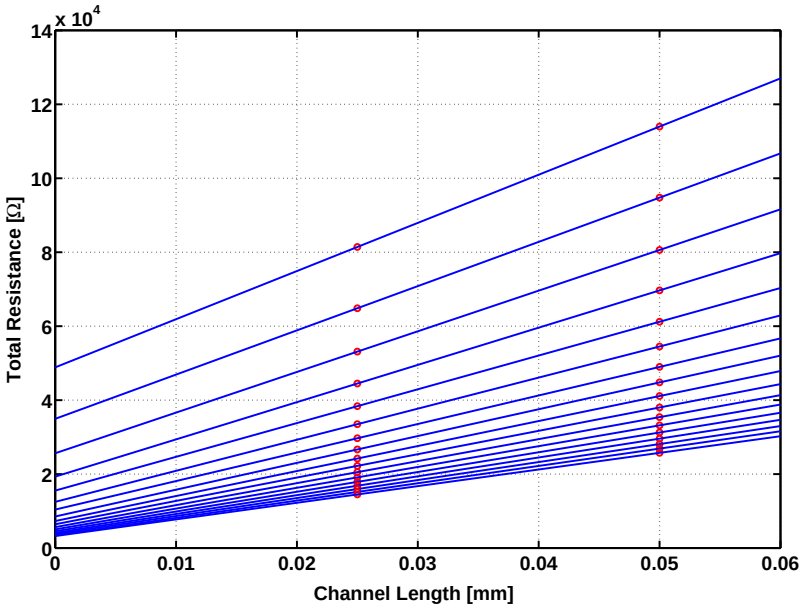
(b) logarithmic plot drain current vs. $(V_G - V_T)$ at different times. Onset Voltages match each other.

Figure 11.15.: Transfer lines shifted about the threshold voltage for channel length $L = 50\mu m$.

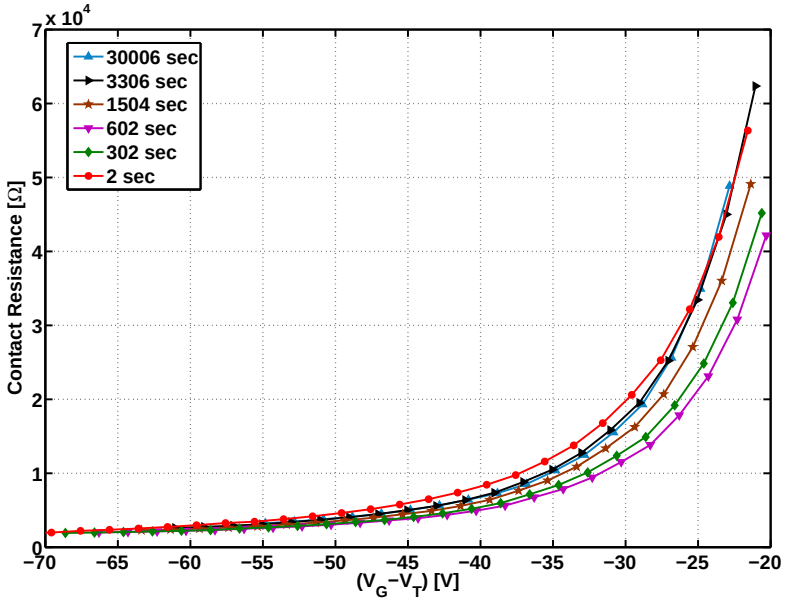
11.2.2. Transfer Line Method

The TCMT measurements for devices with different channel lengths allow to apply the TLM and consequently to observe the contact resistance during the bias stress. The results obtained using the TLM are very questionable concerning their accuracy, because devices with only two different channel lengths were available.

Figure 11.16(a) illustrates the extrapolation to zero length for different gate voltages. The TLM extracted contact resistances do not exhibit a clear trend regarding their bias-stress dependence (figure 11.16(b)). Using the contact resistance, the channel conductance can be determined. Figure 11.17(b) shows the channel conductance. The first curve measured after 2 seconds of bias stress differs strongly form the others. This is because the threshold voltage change during the first transfer curve measurements on the pristine device is still very strong. Mobility values estimated by using the channel conductance and the threshold voltage obtained from the GDM a. CCR method are plotted in figure 11.17(a). Apart from the first curve, the channel conductance and the mobility exhibit an increase with increasing time, which agrees with results of the single channel lengths methods (figure 11.13). For further and more exact statements the measurements have to be repeated with a bigger set of channel lengths.

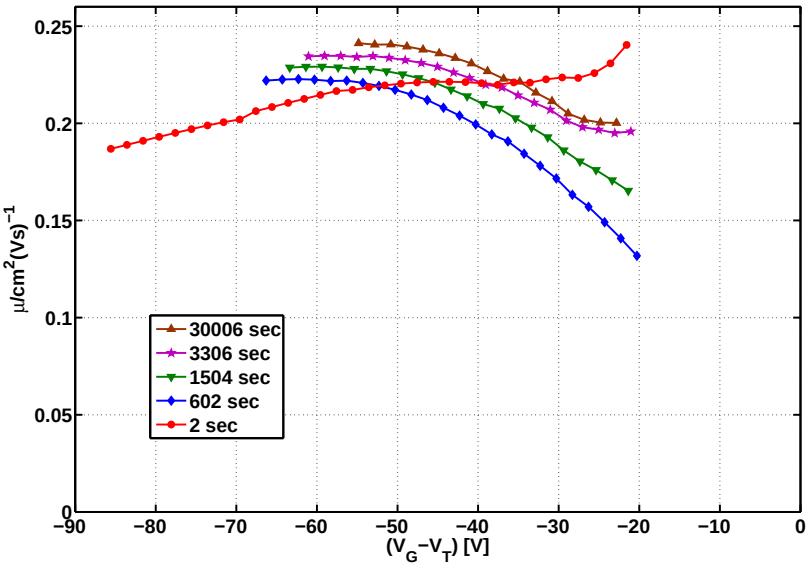


(a) Total Resistance vs channel length for different gate voltage. The extrapolation to zero length gives the contact resistance.

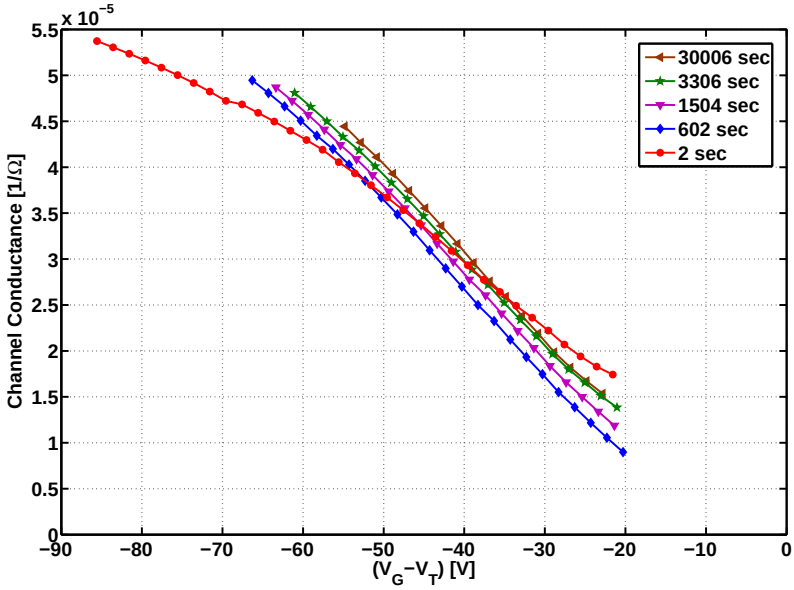


(b) Contact Resistance vs gate voltage for different progress times of the bias stress.

Figure 11.16.: Mobility and corresponding channel conductance at different progress of bias stress obtained from TLM.



(a) Mobility vs. gate voltage minus threshold voltage at different times



(b) Channel conductance vs. gate voltage minus threshold voltage at different times

Figure 11.17.: Mobility and corresponding channel conductance at different progress of bias stress obtained from TLM.

12. Bias Stress Measurements at Low Temperatures

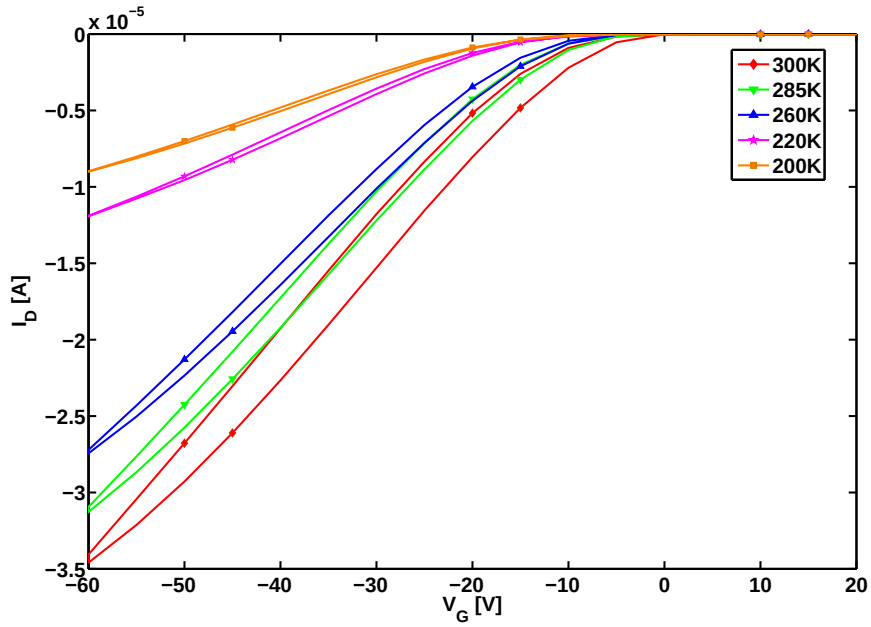
In this section, the temperature dependence of the bias stress effect is investigated. The first part of this chapter deals with the temperature dependence of the threshold voltage. Next, measurements concerning the time evolution of different device parameters at low temperature are shown. In the last part, the observed appearance of inverted hysteresis at deep temperatures is investigated and a possible explanation is presented. The used measurement setup was the same as for the experiments in section 11.2. Also the same $25\mu m$ sample was used again.

12.1. Temperature Dependence of Threshold Voltage

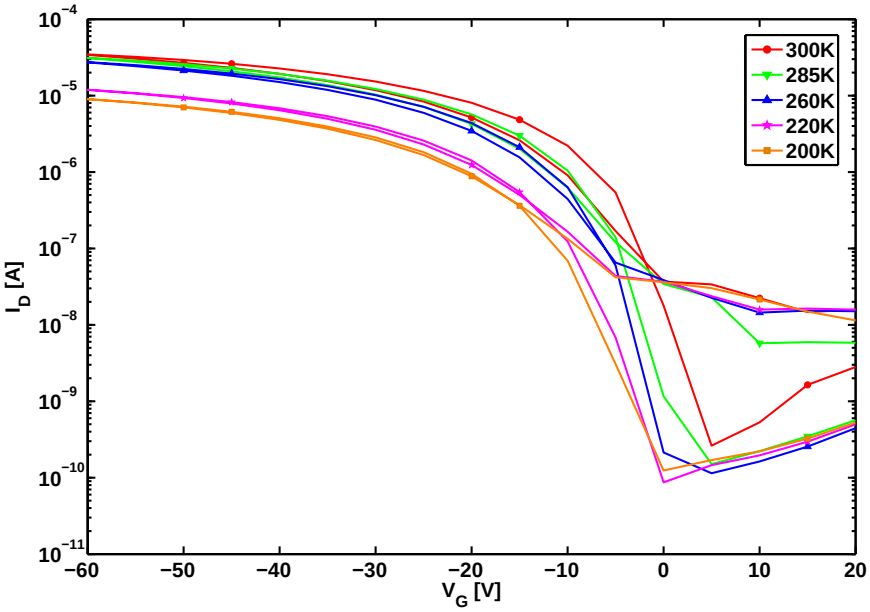
Previous to any bias stress measurement at low temperatures, a detailed discussion about the temperature dependence of the threshold voltage is required. Because, when the threshold voltage value changes with temperature, two bias stress measurements at different temperatures but with equal gate bias cannot be compared directly with each other. A lot of questions would rise up, e.g., the influence of the electric field or how an exact value of the threshold voltage can be extracted. Therefore, transfer characteristics at different temperature were measured.

Figure 12.1 shows five transfer characteristics at different temperatures. The standard FET model (SFM) linear and gate bias dependent and constant contact resistance model (GDM a. CCR) methods were applied to extract the threshold voltages. The obtained threshold voltage values are listed in table 12.1. Both methods give a threshold voltage shift to more negative values with decreasing temperature. This trend is also observed by Horowitz et al. [5]. In contrast, the on-set voltage of the device remains independent of temperature, as can be easily seen in the logarithmic plot (figure 12.1(b)). This is in agreement with the reported results of Salleo et al. and Meijer et al. [6, 24]. Further, they associated the on-set voltage with the flatband voltage and consequently as the characteristic parameter of the OTFT concerning the induced mobile charge carriers. In chapter 5 it was already pointed out that the most reasonable definition of the threshold voltage is to identify it with the flatband voltage. Moreover it was explained in section 8 that the threshold voltage values obtained form the SFM methods are just fit parameters. Hence, the observed threshold voltage shift is a artifact of the applied extraction methods.

Summarizing the results of this subsection, we do not observe a temperature dependence of threshold voltage and consequently the density of free carriers at the semiconductor-insulator interface induced by a specific gate bias is equal for different temperatures. Under the assumption that only the free carrier density determines the bias stress trapping rate, its temperature dependence can be investigated.



(a) Linear plot of transfer curves at different temperature.



(b) Logarithmic plot of transfer curves at different temperature.

Figure 12.1.: Transfer curves at different temperatures. Measurements were performed at $V_D = -0.5V$.

Table 12.1.: Threshold Voltages obtained from SFM and GDM a. CCR method at different temperatures.

Temperature	300K	285K	260K	220K	200K
SFM Linear V_T [V]	-9.3	-12.3	-13.3	-16.1	-17.0
GDM a. CCR V_T [V]	-0.1	-3.1	-4.5	-6.8	-7.2

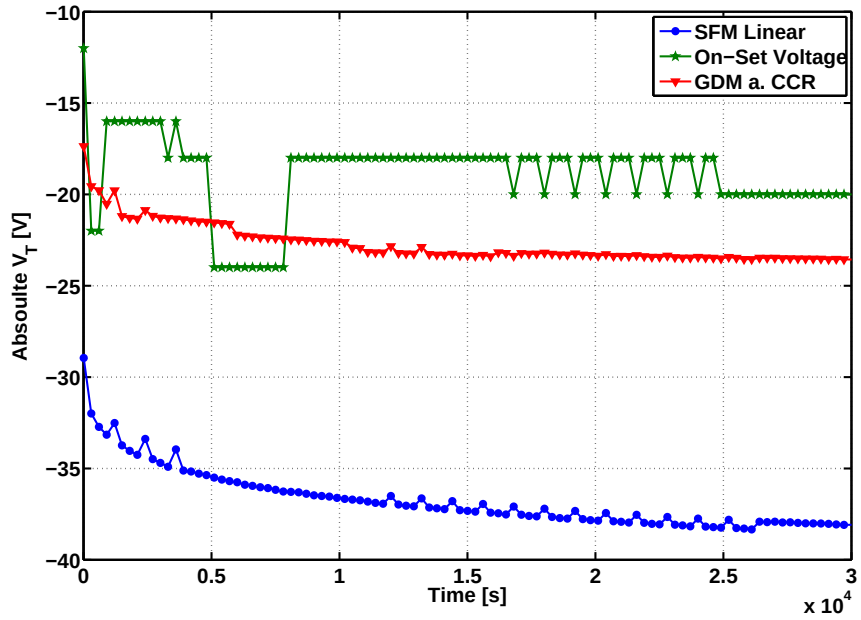
12.2. Transfer Curve Measurement over Time

Here, bias stress behavior at low temperatures is investigated using the TCMT measurement routine. The TCMT measurement was performed at 200K.

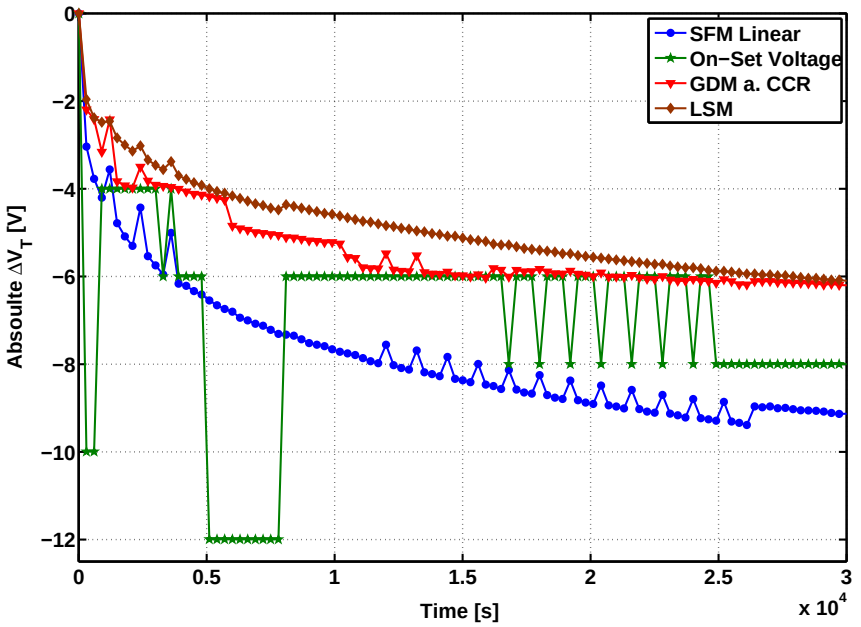
Threshold voltage values are obtained form the LSM, the GDM a. CCR and the LSM Method. In figure 12.2 the results of all methods together with the evolution of the on-set voltage are plotted. The threshold voltage shift is significant lower than at room temperature. Again the SFM linear method shows a high overestimation of the threshold voltage. In contrast to the measurement at room temperature the values obtained by GDM a. CCR method are strongly questionable, because of the following reasons. The trend of threshold voltage values do not exhibit a logarithmic profile as it was observed for the other methods. Moreover, the mobility increases with increasing time (figure 12.3(a)), while the contact resistance decreases (figure 12.3). There is no plausible physical explanation for this behavior. In contrast, the mobility values obtained from the SFM method show a slightly increase of the mobility during the bias stress (figure 12.3(a)). The observed spikes in the figures 12.2-12.3 are no artifacts of the extraction methods. Rather the transfer curves, measured at this times, deviate from the others. At the moment, no plausible explanation have been found for this phenomenon.

Figure 12.4 shows the transfer curve shifted about the threshold voltage. A good match of the transfer curve is only achieved with the LSM values for ΔV_T. This confirms that the SFM and GDM a. CCR method values do not reflect the real threshold shift. In the linear plot (figure 12.4(a)), it can be seen that the bias stress changes again the shape of the transfer curve. The shifted curve match good except at high gate voltages. In this range, the transfer curves measured at the beginning of the bias stress exhibit a stronger bending. There are two possible reasons for this phenomenon: (1) The bending could be caused by a decreasing contact resistance with increasing time, but there is no physical basis for this assumption and (2), the more likely reason, mobility degradation at high gate voltages. Mobility degradation was already reported by Mottaghi et al. [47]. Also for mobility values at room temperature obtained form TLM method shows a similar behavior (figure 11.17(a)). Furthermore, the fail of the GDM u. CCR are model could be explained, if it is assumed that mobility saturates at a certain gate voltage. Such a saturation behavior cannot be represented by the semi-empirical mobility law (equation 5.3). Therefore, the fitting routine increases the contact resistance to minimize the errors.

From this measurement, it can be concluded that the threshold voltage shift under gate bias stress increases with increasing temperature. The shape of the transfer curve is again affected by the gate bias stress, whereby it cannot be determined whether the contact resistance or the mobility function changes during the bias stress.

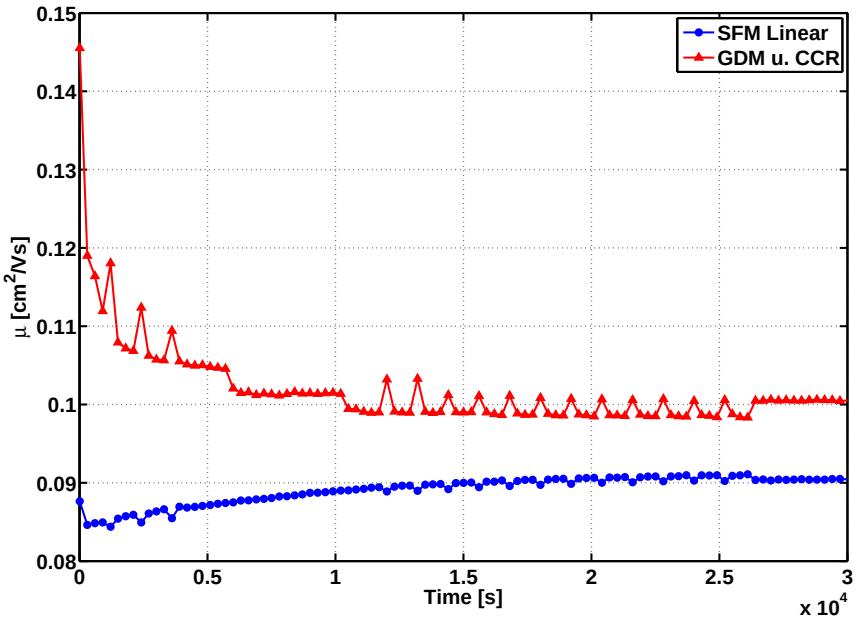


(a) Time evolution of the threshold voltage V_T.

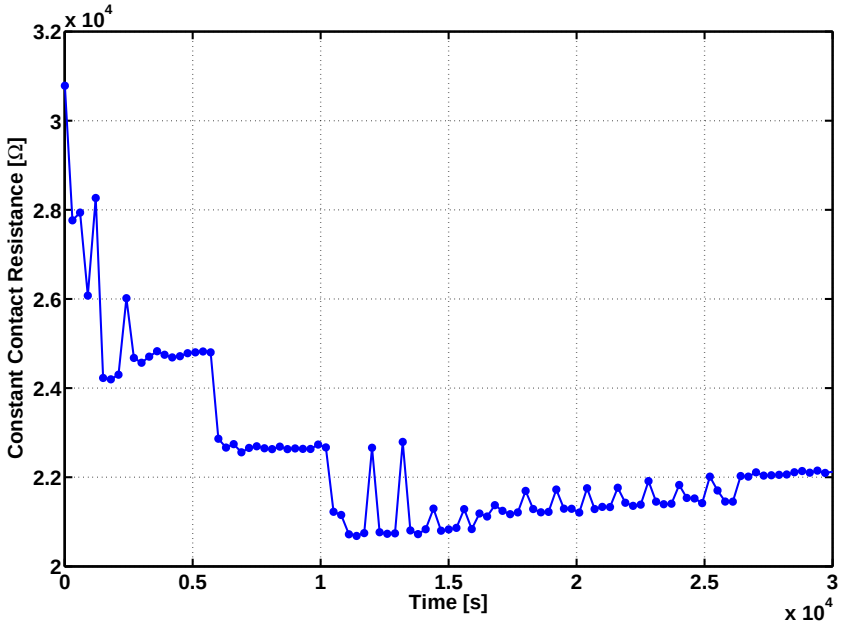


(b) Absolute threshold voltage shift ΔV_T vs Time.

Figure 12.2.: TCMT measurement at 200K. Only the LSM method gives reasonable values for the threshold voltage shift.

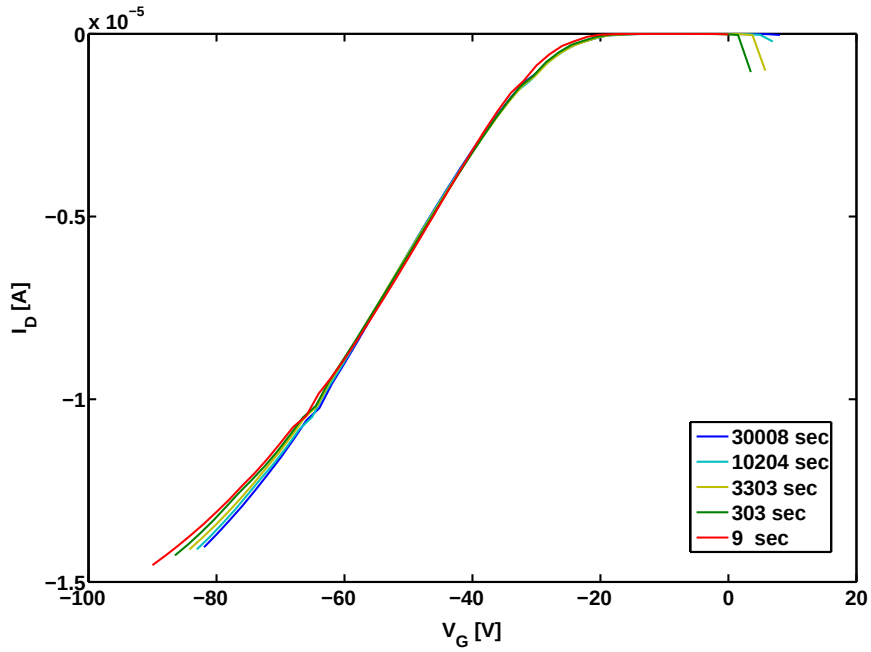


(a) Mobility vs Time. Mobility obtained from the GDM a. CCR method decreases with time.

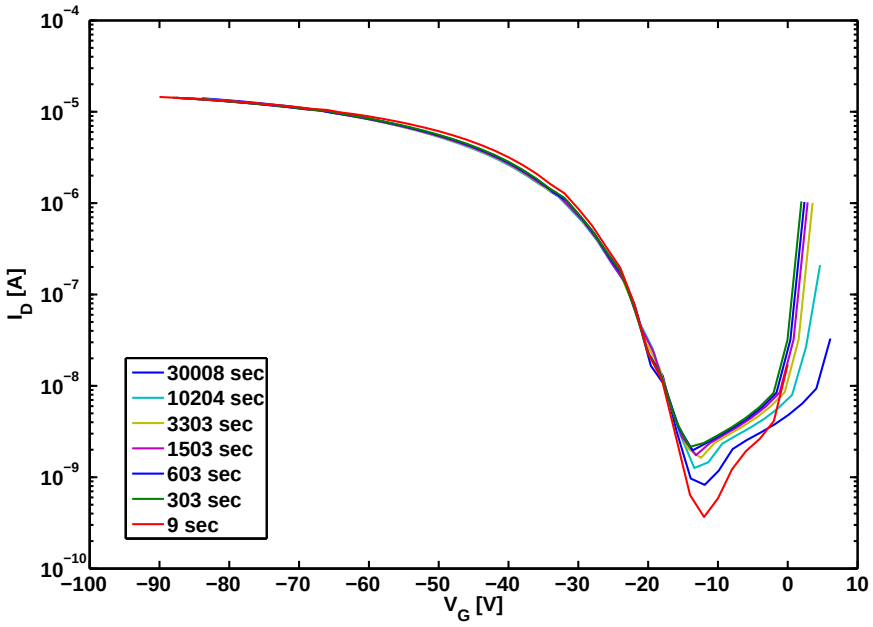


(b) Constant contacted resistance obtained from GDM a. CCR method.

Figure 12.3.: Mobility and Constant contact resistance evolution during the TCMT.



(a) Linear plot of drain current vs. $(V_G - V_T)$ at different times. Shift of transfer line is not parallel.



(b) Logarithmic plot of drain current vs. $(V_G - V_T)$ at different times.

Figure 12.4.: Transfer lines shifted about the threshold voltage at 200K.

12.3. Inverted Hysteresis

In this section the phenomenon of inverted hysteresis at low temperature is analyzed.

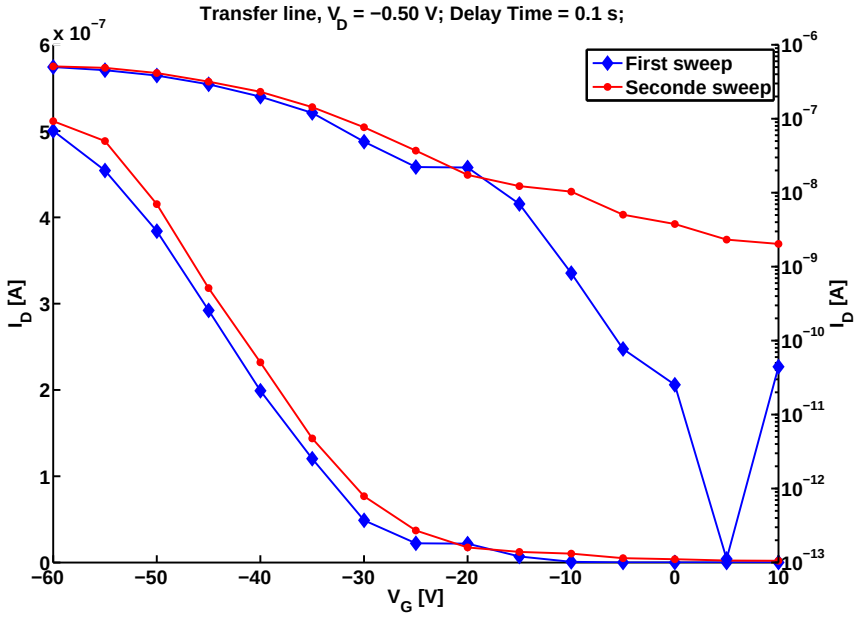
The temperature dependence of the hysteresis of devices fabricated in our lab were already investigated by Golubkov et al. [48]. It has been shown that the hysteresis becomes smaller with decreasing temperature, meaning that the difference between the threshold voltage of the first and second sweep decreases. Interestingly, at a certain temperature the hysteresis is inverted, i.e. it seems that the current increases with time (figure 12.5(a)). A possible explanation is that because of the low drain currents at low temperatures, the charging time for the capacitor increases. The capacitance of the channel could be neglected, but because of the common gate structure, the drain electrode forms a capacitor together with the silicon gate. The charging current is superposed on the channel current and is measured at drain electrode as well.

In order to test the hypothesis, two transfer curves with different delay times were measured at 150K. Both transfer curves are plotted in figure 12.5. The inverted hysteresis disappears for a longer delay time, which suggests the correctness of the hypothesis. Also first drift-diffusion simulation by Gruber et al. supports the explanation [46].

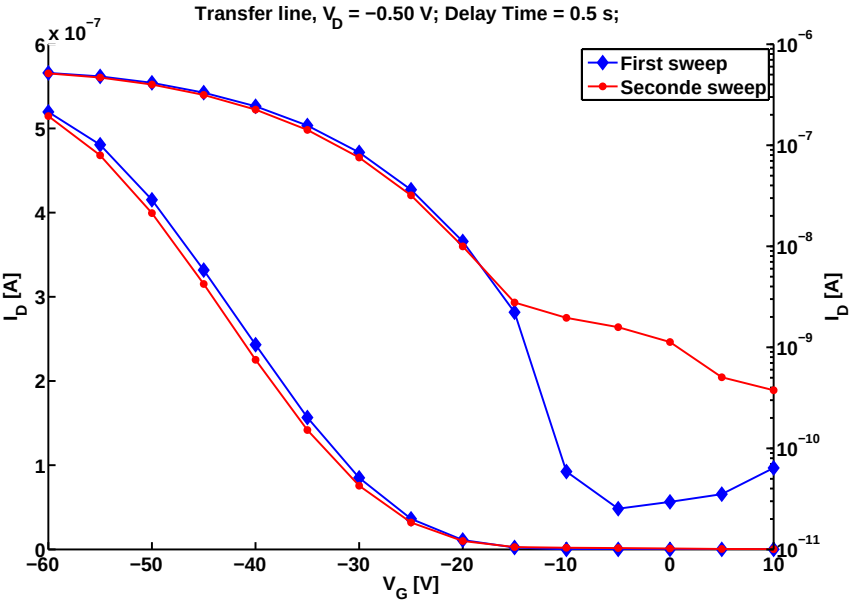
Anyhow, a simple estimation should be presented here. The RC time constant indicates the time required to charge a capacitor to 63.2 percent of full charge. When it is assumed that the drain current is equal to the charging current, meaning that the channel current is zero, the minimal time for charging can be estimated. In our case it is estimated in the following way

$$\tau = RC = \frac{\Delta V_G}{I_D} C_i W L_P \tag{12.1}$$

where W is the channel width, L_P the pad length and ΔV_G the gate voltage step of the sweep. ΔV_G is taken, because it is assumed that the capacitor was fully charged in the previous step. We now estimate the time constant for the highest gate voltage of the transfer current. The gate voltage is increased about $\Delta V_G = 5V$ and the drain current value is $I_D = 5$ x $10^{-7}A$. For a $Ci = 24$ x $10^{-9}C/cm^2$, $W = 0.7cm$ and $L_P = 0.5cm$, the time constant is $\tau = 0.09s$. In other words for a delay time of 0.1s the capacitor is at least slightly more charged than 63.2 percent of full charge.



(a) Drain current vs gate voltage. Delay time between each measurement point was 0.1 seconds.



(b) Drain current vs gate voltage. Delay time between each measurement point was 0.5 seconds.

Figure 12.5.: Transfer curve measured with two different delay times at 150K. For the longer delay time the inverted hysteresis disappears.

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