Design of a Bandwidth Calibration Unit for a PLL

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Abstract

The bandwidth of a phase locked loop (PLL) influences its characteristics greatly, e.g. the phase noise performance or the maximum possible data rate for a modulator. The open loop gain is an important factor which determines the bandwidth, and therefore also the small signal gain of the voltage controlled oscillator (VCO), which can vary greatly over different operating points. To guarantee the fulfillment of all specifications, parts of the circuit have to be overdesigned, which wastes chip area and power. This diploma thesis presents a bandwidth calibration concept based on a time to digital converter (TDC), which allows the bandwidth to stabilize over different conditions, and therefore the amount of overdesign can be reduced. The functionality of the concept is shown with a transient simulation, and a short introduction to the topic time-to-digital conversion is given.

Kurzfassung

Die Bandbreite einer Phasenregelschleife beeinflusst ihre Eigenschaften stark, z.B. das Phasenrauschen, oder die maximal mögliche Datenrate bei einem Modulator. Die Schleifenverstärkung der offenen Schleife hat einen großen Einfluss auf die Bandbreite, und deshalb auch die Kleinsignalverstärkung des spannungsgesteuerten Oszillators, welche stark über verschiedene Betriebspunkte variiert. Um die Erfüllung aller Spezifikationen garantieren zu können, müssen Teile der Schaltung überdimensioniert werden. Dies bedeutet einen erhöhten Verbrauch an Fläche und Leistung. Diese Diplomarbeit stellt ein, auf einem Zeitquantisierer basierendes, Konzept vor, mit dessen Hilfe die Bandbreite über die verschiedenen Konditionen stabilisiert werden kann, und somit verringert sich der notwendige Grad an Überdimensionierung. Die Funktionalität wird in einer Transienten-Simulation demonstriert, und es wird eine kurze Einleitung in die Thematik der Zeitquantisierung gegeben.

Acknowledgements

I would like to thank my supervisor Dipl.-Ing. Dr. techn. Mario Auer for his kind help and motivation, and for being the mouthpiece towards the Graz University of Technology. I also want to thank him very much for his help regarding the text itself.

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Contents

1 Introduction

1.1 Aim of this thesis

- The aim of this thesis is to find a concept for the measurement of the PLL closed-loop bandwidth, which then, if necessary, allows a calibration of the bandwidth. If the bandwidth is stabilized, then chip area and power dissipation will be saved. The final concept introduced in this thesis is able to determine the absolute value of the closed-loop transfer function at different frequencies, and therefore delivers the bandwidth. Furthermore, if the bandwidth calibration is only needed, then the $test$ frequency can be fixed, simplifying the concept even more. Then the concept delivers a value which is proportional to the bandwidth.

- The concept found in this thesis is based on a time-to-digital converter. This allows the implementation of two additional features. The first feature is the ring oscillator in the TDC core, which can be used as a second on-chip frequency source, enabling the transceiver to receive its own transmitted data. This loopback functionality allows additional tests to be carried out. The second feature is a time-to-digital converter at the PLL output, which can be used to measure the output period time jitter.

- This thesis also proposes a concept for the time-to-digital converter. The TDC core consists of a ring oscillator, to allow it to be used as a second frequency source. Allong with the TDC core, the prescaler and the coarse counter, all other components are normal digital logic blocks, and therefore easy to implement. The resulting TDC concept allows a typical maximum measurement time interval of $33\ ns$.

1.2 Motivation

The demand for analog integrated circuits which utilize a transmitter or a receiver is growing every year. In a modern car, an increasing amount of wireless technology can be found. One example are tire pressure sensors. Different topologies (Figure 1.1) can be used to connect these wireless devices.

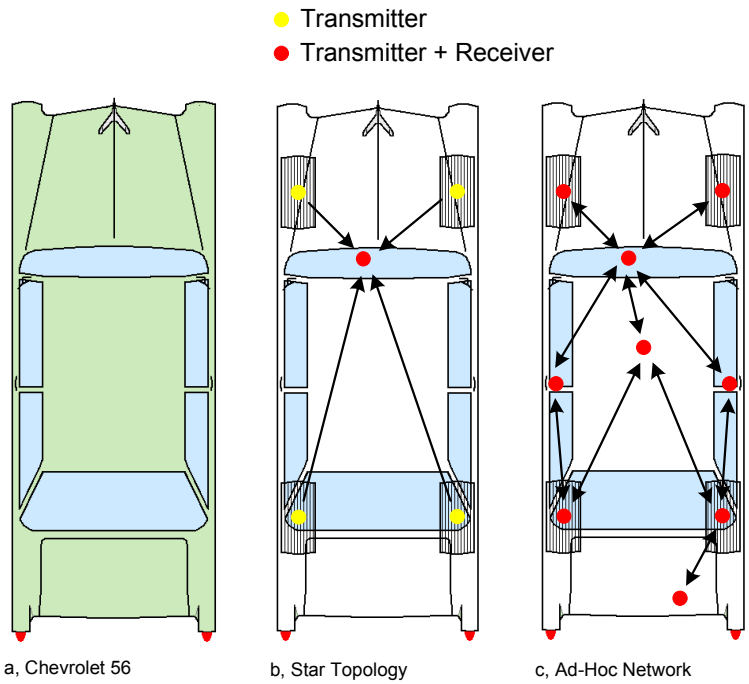


Figure 1.1: Two Wireless Network Topologies

An Ad-Hoc network topology has the advantage that between all nodes a physical connection does not have to be possible, and if the distance for a direct communication is too great then the message can be forwarded by other nodes. This increases reliability, and the bridgeable distance. The downside is that now at least the central nodes have to be transceivers, and this does increase the complexity.

A transceiver structure which is presented in Figure 1.2 utilizes a phase locked loop as a frequency synthesizer for generation of the carrier, the modulator, a power amplifier, an antenna, a mixer for the receive path, and the receiver block itself. The output frequency generated by the phase locked loop is digitally settable, and stabilized by the crystal oscillator.

The modulator shapes the carrier signal in dependence of the current data input

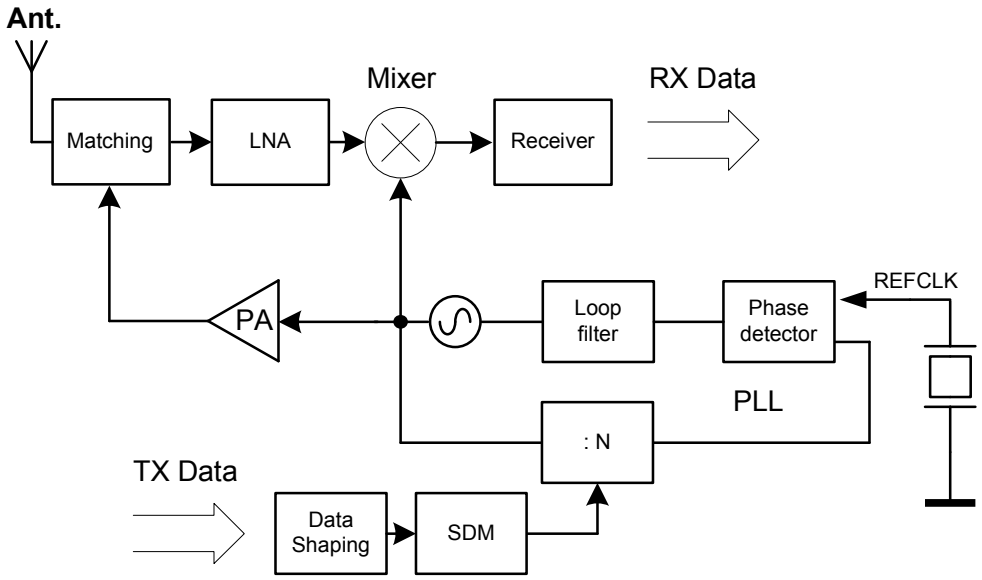


Figure 1.2: Basic Transceiver Architecture

bit. Which signal parameter is altered depends on the used modulation method. If the frequency of the transmission is changed between defined values according to the data signal level, then this is called frequency shift keying (FSK). It can be easily implemented by changing the feedback divider setting of the phase locked loop (1.3) according to the data stream [1].

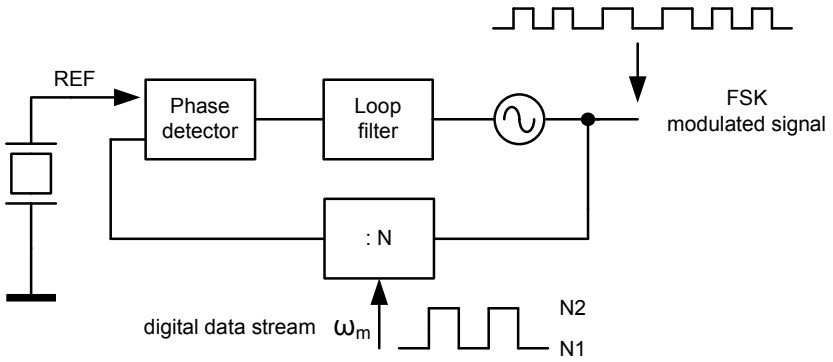


Figure 1.3: Frequency Shift Keying (FSK)

For this modulation, the closed-loop bandwidth of the PLL must be set according to the data rate of the transmission. If it is too low then the shape of the modulated output signal is increasilly falsified (Figure 1.4), and the quality of the transmission decreases. The closed loop bandwidth depends on many parameters, which have a statistic nature or are not constant. For example the small

signal gain of the voltage controlled oscillator can change its value by 100 percent over different samples or different operating points. Hence it follows that the bandwidth will also not be fixed, but can vary greatly. That means the PLL must be designed to provide enough bandwidth for the specified data rate also in the worst case scenario.

If the PLL bandwidth is overdesigned to guarantee the function in the worst case scenario, it gets increasingly difficult to obtain a low enough PLL output signal phase noise, and this specification has again be meet. To be sure that the phase noise specification is fulfilled, again overdesign could be needed. This again wastes area and power.

An on-chip closed loop bandwidth measurement circuit would allow the correction of an initial deviation from the specified value. The correction of a wrong loop gain can be done with a variation of the charge pump current. For example if the VCO gain is to small, then the charge pump current is increased to cancel this effect. This stabilizes the closed loop bandwidth of the PLL, and as a result much overdesign is not needed anymore, therefore some area and power could be saved.

1.3 Concept based on TDC

Two additional applications are possible if the built-in-self-calibration concept is based on a time-to-digital converter which utilizes a ring-oscillator.

Built-in-self-test (BIST) for a Period-Time-Jitter Measurement of the PLL on-Chip

The time-to-digital converter at the output of the phase locked loop can be used to measure the period time of a lot of periods of the PLL output signal. If a histogram is made on-chip from this data, then the period-time-jitter can be measured [2]. The structure of such a test can be seen in Figure 1.5. This would allow to benchmark the phase noise performance of the phase locked loop in a fast an easy manner.

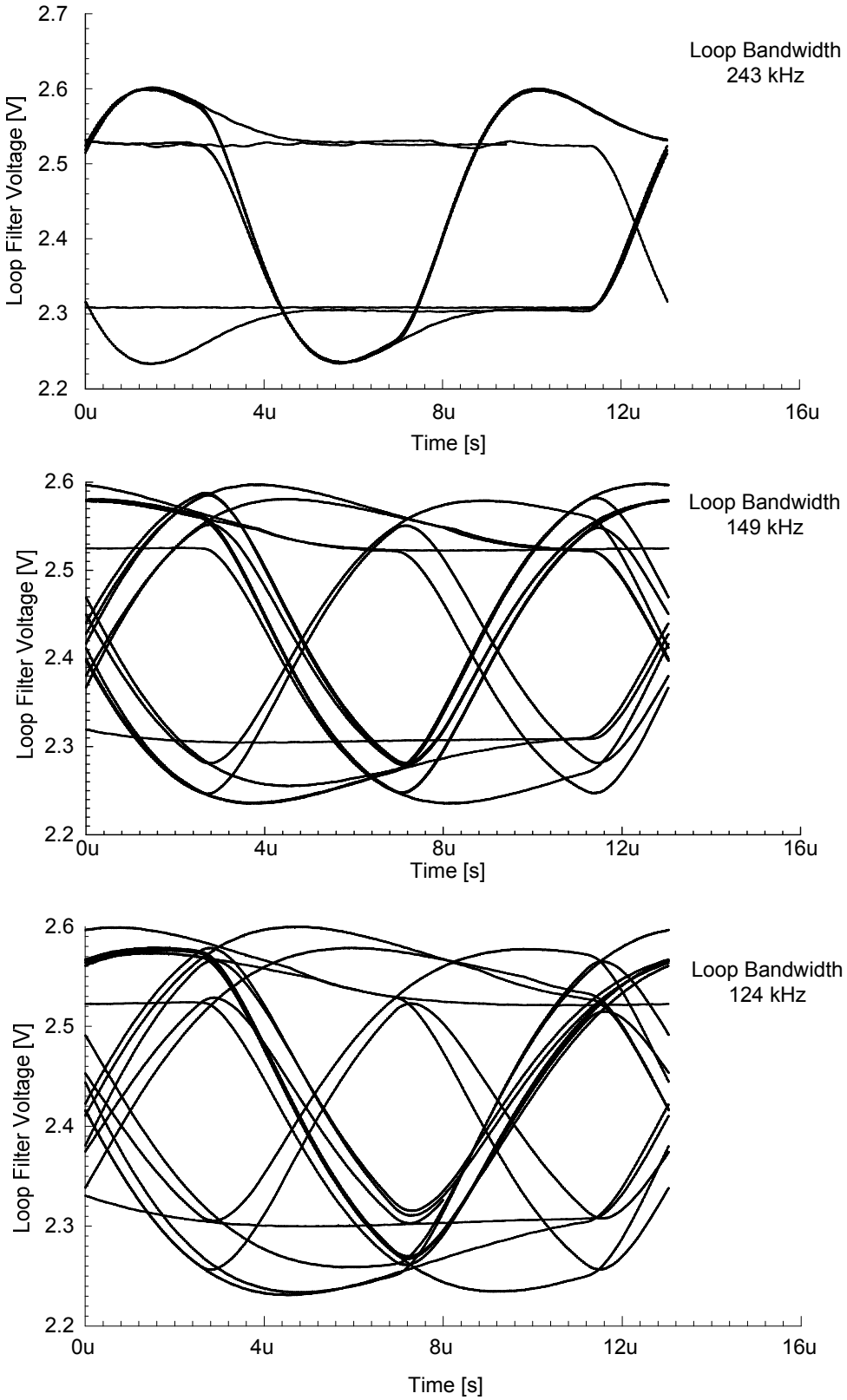


Figure 1.4: Loop bandwidth impact on a FSK modulation $(230\ kHz)$, if the loop bandwidth is too small then the output signal quality worsens

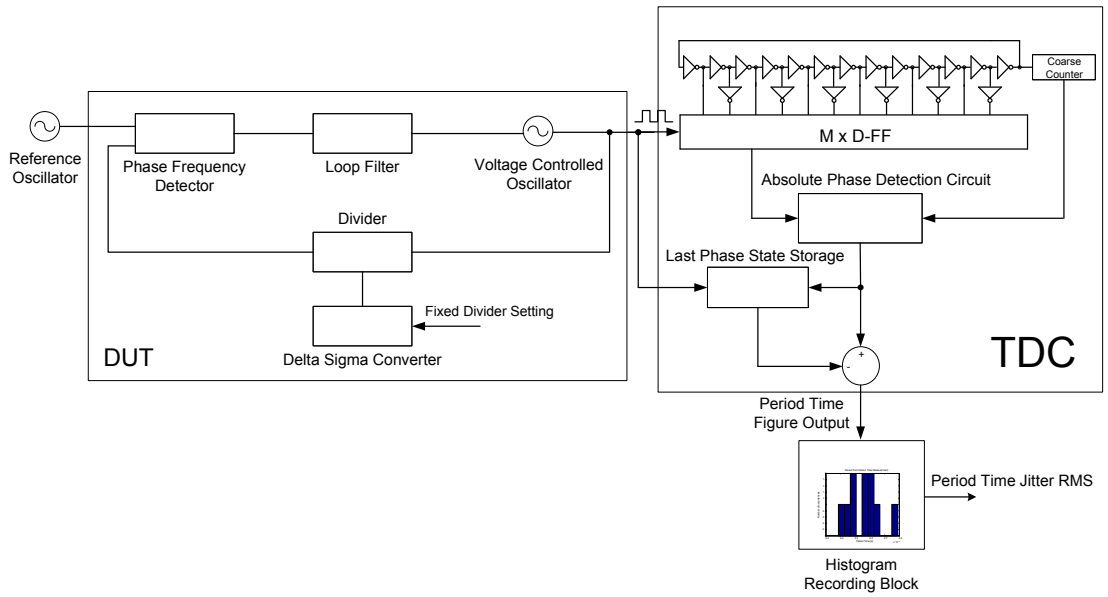


Figure 1.5: Period Time Jitter Measurement, a time-to-digital converter will allow to measure the period time jitter at the PLL output

Second Frequency Source on-Chip

The TDC core ring oscillator could be used as a second frequency source (Figure 1.6). If the inverters in the ring are built tuneable, then the output frequency can also be set in a specific range. To make a coarse selection of the output frequency the following method could be used in combination with the on-chip PLL:

- Set the PLL to the new wanted output frequency of the ring oscillator
- The output word of the time-to-digital converter is used to tune the ring oscillator
- If the output word is bigger than twice the number of inverters in the ring, then its output frequency is to high. Via tuning of the ring supply voltage the propagation delay of the inverters is increased.
- If the output word is smaller than twice the number of inverters in the ring then the output frequency is to low. Again tuning is done.
- If the output word is exactly twice the number of inverters then the second output frequency is tuned to the current output frequency of the phase

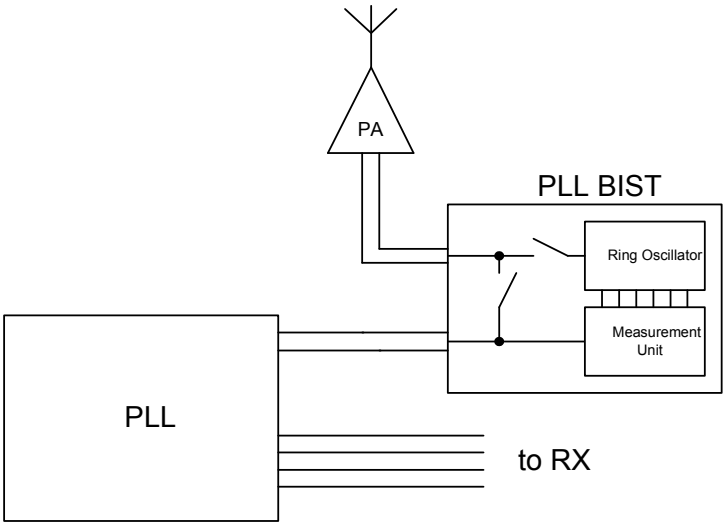


Figure 1.6: Second frequency source. This source will allow an additional loopback mode

locked loop. Now the PLL output can be disconnected from the TDC input, and the ring oscillator serves as a second frequency source.

Two independently setable frequency sources on-chip would allow a transceiver to receive its own transmissions. Normally this would not be possible, if only one frequency source is integrated, and the second frequency can not be derived from the first frequency source. As an example this would allow loopback tests.

2 Phase-locked-Loop (PLL)

2.1 Fields of use

Phase-Locked-Loops are used in many different applications. These include [3]:

- Frequency synthesis: Clock signals or carriers must have a stable frequency like a crystal oscillator provides, but the output frequency must also often be digitally settable. A phase-locked-loop offers both: stabilized by a crystal oscillator, and a digitally settable output frequency.
- Clock recovery [4]: Many new data communication standards use a serial transmission scheme for the data path, with the drawback that the data clock from the transmitter is now missing at the receiver, and has to be restored first from the data stream. This can be done with a PLL. As long as the time interval between subsequent signal edges in the received data stream are short enough, the PLL restores the clock which was used for sending the data.
- Usage of a PLL for de-skewing: When using more parallel high frequency signal data paths for a data transmission, not every path is exactly as long as the others in the electrical sense. At the receiver all of the different data paths are not delayed by the same time, and sampling without insuring this can yield to wrong received data. On a complex and high frequency board, e.g. a computer mainboard skewing is an important topic, and a phase-locked-loop can be used to ensure that all the data paths are delayed the same amount of time.
- Jitter and noise reduction: The output signal which is constructed with the help of the PLL circuit follows the input signal frequency deviation over time, and so the wanted signal is conserved. But because of the finite bandwidth

of the phase-locked-loop the new output signal cannot follow very fast deviations of the input signal, thus the jitter and noise of the input signal can be filtered out using the PLL.

- Modulation and demodulation in various applications [1]

2.2 Architecture

A basic architecture of a PLL is shown in Figure 2.1:

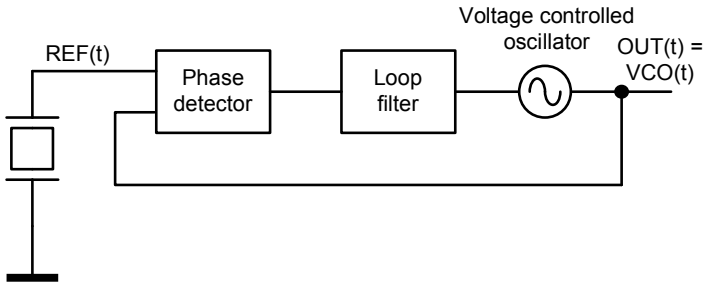


Figure 2.1: Basic PLL Architecture [3]

An important part of the phase-locked-loop is the voltage controlled oscillator (VCO), which generates an output signal with a frequency that is controlled by a voltage at the control input. The second basic block is the phase detector, which compares the input signal from the reference oscillator with the current output signal of the VCO. In many cases, the reference signal comes from a crystal oscillator.

2.3 Components

2.3.1 Voltage Controlled Oscillator (VCO)

Ring Oscillator

The voltage controlled oscillator is often realised in form of a ring or an LC oscillator [3]. A ring oscillator is very small, but normally does not offer a comparable high Q-factor as the LC oscillator. Therefore the ring oscillator generally has a higher phase noise at the output as a comparable LC oscillator [5]. Also ring

oscillators tend to have a bad power supply rejection ratio (PSRR) which means fluctuations on the supply voltage will translate to changes in the output frequency. A single-ended ring oscillator structure is shown in Figure 2.2.

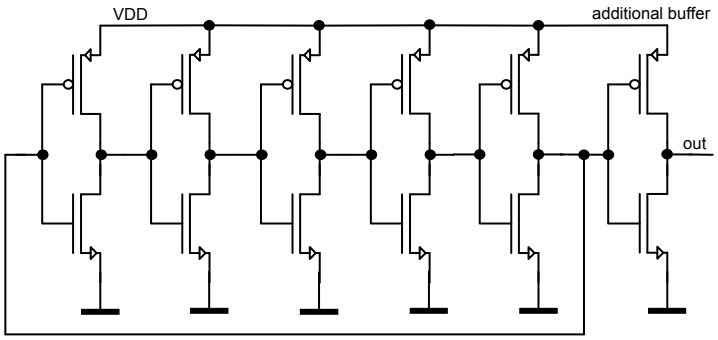


Figure 2.2: Single-ended Ring Oscillator

A single-ended ring oscillator consists of a chain of an uneven number of inverters [6]. The last inverter output is fed back into the input of the first one. No stable operating point can be found in this circuit. The output frequency can be found with [6]:

$$f_{out} = \frac{1}{2 \cdot M \cdot t_d} \tag{2.1}$$

where M denotes the number of inverters in the chain, and t_d is the typical propagation delay of a single inverter. This equation acts on the assumption that the propagation delay of a high-to-low transistion equals exactly the delay for a low-to-high transition [7]. For a standard inverter used in a digital circuit this is normally not the case.

For tuning the single-ended ring oscillator firstly the amount of capacity on every output node can be controlled in dependence of the control voltage. For example a varactor could be used as a variable capacitance, but a drawback is the increased power dissipation for smaller output frequencies. The second possibility is to tune the supply voltage of the ring oscillator core. The third realisation of a VCO uses a steered supply current for either the whole oscillator core, or for every single stage. The advantage of these methods is that for a smaller output frequency the supply current drops.

LC Oscillator

A basic element of any LC oscilator is a resonance tank formed by an inductor L and a capacitor C. This kind of oscillator offers a good jitter and phase noise performance, but needs normally a lot of space for the implementation of the inductor. Also there is parasitic coupling from the inductor to the surrounding circuits. An often used differential circuit is shown in Figure 2.3 [3].

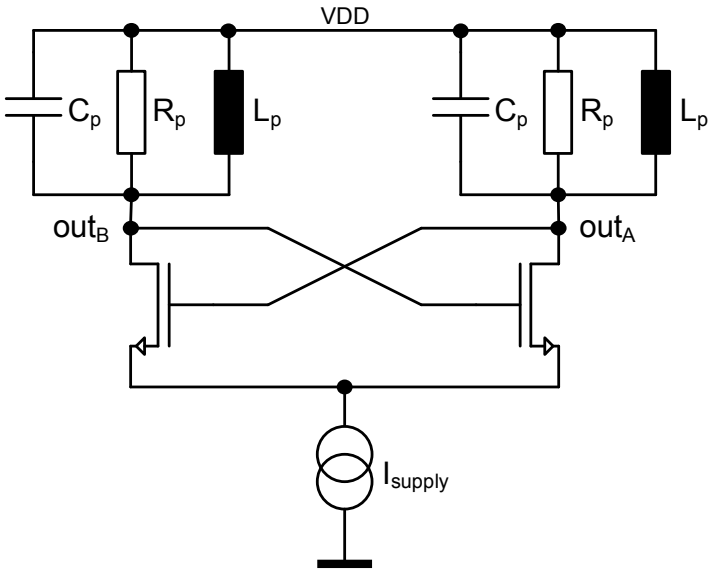


Figure 2.3: Differential LC Oscillator

Two resonance tanks are the load for the two transistors, and if the overall gain is high enough then noise in the circuit is amplified continually, and the oscillation starts. In the steady state condition the tail current I_{supply} is switched periodically between the two sides [3].

To make this oscillator tunable (Figure 2.4) [3] one can change the value of the inductor or the capacitance. The inductor is fixed by its physical layout, and therefore the capacitance has to be controlled, e.g. with a varactor device, which changes its capacitance with the voltage across its terminals.

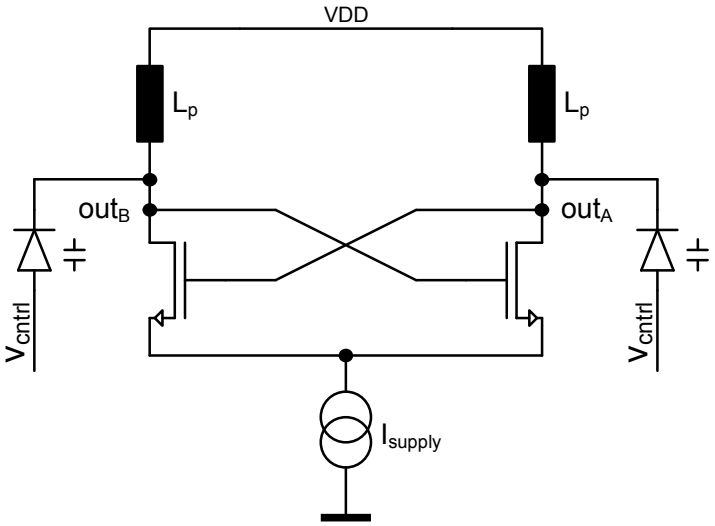


Figure 2.4: Differential Voltage Controlled LC Oscillator [3]

2.3.2 Phase Detector

Analog Multiplier

Analog multipliers are often realised in the form of a gilbert cell or as a four-quadrant multiplier. They allow very high frequency operation, and are often used with sinusoidal or near sinusoidal input signals.

Example for a reference signal [4]:

$$s_1(t) = A \cdot sin(\omega_1 \cdot t + \varphi_1) \tag{2.2}$$

The feedback signal from the divider can also be rectangular (fourier series):

$$s_2(t) = B \cdot [\frac{4}{\pi} \cdot cos(\omega_2 \cdot t + \varphi_2) + \frac{4}{3 \cdot \pi} \cdot cos(3 \cdot \omega_2 \cdot t + \varphi_2) + \frac{4}{5 \cdot \pi} \cdot cos(5 \cdot \omega_2 \cdot t + \varphi_2) + ...] \tag{2.3}$$

These two input signals are also shown in Figure 2.5. These signals are now multiplied together, to form the output signal. If the loop is in the locked state then the frequency of both input signals is equal.

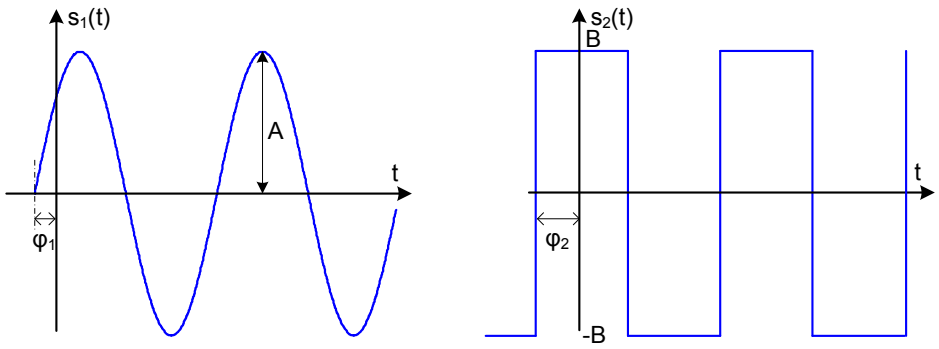


Figure 2.5: Possible Input Signals [4]

$$s_{out}(t) = s_1(t) \cdot s_2(t) = A \cdot B \cdot sin(\omega_1 \cdot t + \varphi_1) \cdot [\frac{4}{\pi} \cdot cos(\omega_2 \cdot t + \varphi_2) + \frac{4}{3 \cdot \pi} \cdot cos(3 \cdot \omega_2 \cdot t + \varphi_2) + \frac{4}{5 \cdot \pi} \cdot cos(5 \cdot \omega_2 \cdot t + \varphi_2) + ...] \quad (2.4)$$

Further simplification with

$$sin(x) \cdot cos(y) = \frac{1}{2} \cdot [sin(x - y) + sin(x + y)] \quad (2.5)$$

$$s_{out}(t) = A \cdot B \cdot \frac{4}{2 \cdot \pi} \cdot [sin(\omega_1 \cdot t + \varphi_1 - \omega_2 \cdot t - \varphi_2) + sin(\omega_1 \cdot t + \varphi_1 + \omega_2 \cdot t + \varphi_2) + \frac{1}{3} \cdot sin(3 \cdot \omega_1 \cdot t + \varphi_1 - 3 \cdot \omega_2 \cdot t - \varphi_2) + \frac{1}{3} \cdot sin(3 \cdot \omega_1 \cdot t + \varphi_1 + 3 \cdot \omega_2 \cdot t + \varphi_2) + ...] \quad (2.6)$$

$$s_{out}(t) = A \cdot B \cdot \frac{4}{2 \cdot \pi} \cdot [sin(\varphi_1 - \varphi_2) + sin(2 \cdot \omega_1 \cdot t + \varphi_1 + \varphi_2) + \frac{1}{3} \cdot sin(\varphi_1 - \varphi_2) + \frac{1}{3} \cdot sin(6 \cdot \omega_1 \cdot t + \varphi_1 + \varphi_2) + ...] \quad (2.7)$$

The first DC term in the brackets is the term we wanted to obtain with the analog

multiplier. It carries the information about the phase error. All other high frequency terms in the brackets are unwanted, and therefore are filtered out in the loop filter.

$$s_{out}(t) = A \cdot B \cdot \frac{2}{\pi} \cdot [sin(\varphi_1 - \varphi_2) + ...] = A \cdot B \cdot \frac{2}{\pi} \cdot [sin(\varphi_{error}) + ...] \tag{2.8}$$

If we set

$$Kpd = A \cdot B \cdot \frac{2}{\pi} \tag{2.9}$$

the so called phase detector gain can be introduced [4]. Also the high frequency terms are now left out. The detector output can be written in a new form:

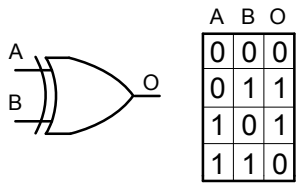
$$s_{out}(t) \simeq Kpd \cdot [sin(\varphi_{error})] \tag{2.10}$$

If the value of φ_{error} is very small, the sin function can be further approximated, so we can get the linear model of the phase locked loop.

$$s_{out}(t) \simeq Kpd \cdot \varphi_{error} \tag{2.11}$$

This output signal of the analog multiplier is now used to control the voltage controlled oscillator after it has passed the loop filter.

XOR Gate



A	B	O
0	0	0
0	1	1
1	0	1
1	1	0

Figure 2.6: XOR Gate

A single XOR gate can be used as a phase detector [4, 3] (Figure 2.6). It

outputs a waveform whose width of the output pulses are proportional to the difference of the phases of both input signals (=phase error), as can be seen in Figure 2.7. A low pass filter creates the mean value from the output signal, and the filtered DC voltage is proportional to the phase error. An attribute of the XOR gate is the creation of pulses on both the rising and falling edges.

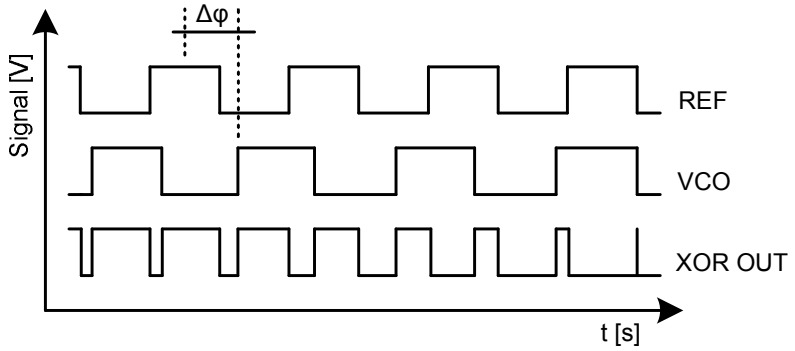


Figure 2.7: XOR Phase Detector Time Behaviour

A drawback of the XOR gate is that it can only handle small phase errors, because its transfer function is ambiguous for a phase error bigger than $\pm\pi$. The transfer function is illustrated in Figure 2.8.

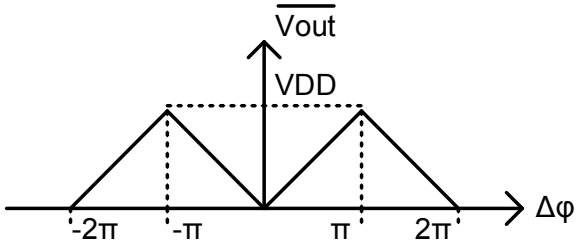


Figure 2.8: XOR Linear Transfer Function [3]

JK Flip Flop

A second possibility for a phase detector is the usage of a JK flip flop [4] (Figure 2.9). In this case the phase detector is sensitive on the rising edge of both of the input signals. The falling edges of the signals do not play a role in this type of PD.

With zero phase error the two input signals have opposite phase alignments. The rising edge of the reference signal sets the flip flop output to high, and the

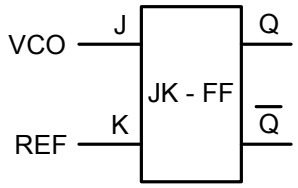


Figure 2.9: JK Flip Flop Phase Detector

next rising edge from the VCO output sets the output back to low. That means with zero phase error, the output signal from the phase detector has a duty cycle of 50 percent, and the average DC output voltage is half the supply voltage. If a small phase error is introduced, e.g. the voltage controlled oscillator falls behind the reference phase, then the duty cycle starts to grow above 0.5, because the logical high level time of the output is now longer than the low level time, and so the average DC output voltage starts also to rise. This increases the VCO output frequency, and the phase error is minimized again. Figure 2.10 illustrates the operation.

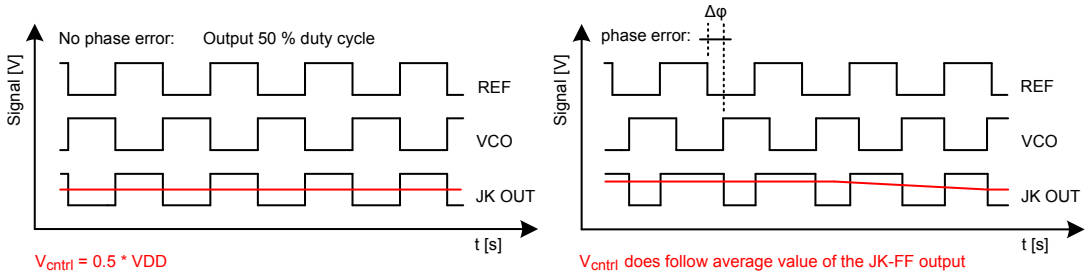


Figure 2.10: JK FF Phase Detector Time Behaviour

The transfer function can be seen in Figure 2.11, which describes the average output voltage as a function of the input phase error. This function is again ambiguous outside the region $\pm\pi$.

PFD, Phase Frequency Detector + Charge Pump

A modern and frequently used detector is the phase frequency detector (PFD) [3]. It offers advantages in comparison to the other phase detectors, especially when both input frequencies are not equal, and the loop is in an unlocked state. The other phase detectors can not work well, if the phase error gets to big, because of their ambiguous behaviour for large phase errors. The phase frequency detector

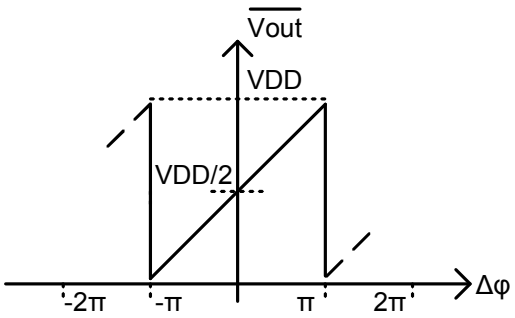


Figure 2.11: JK FF Transfer Function [4]

not only can compare the phase alignment, but it also has the ability to compare both of the input frequencies together (frequency detector), which helps to find lock easily.

A typical PFD and charge pump circuit can be seen in Figure 2.12 [4, 3, 1].

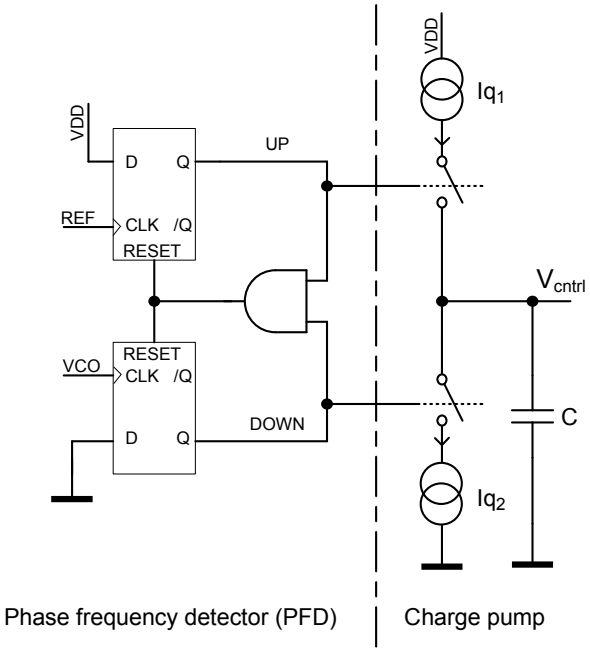


Figure 2.12: Phase Frequency Detector and Charge Pump Architecture [3]

The circuit is sensing edges at the signal inputs, e.g. rising edges. The PFD circuit has an internal state which can be changed when input signal edges are arriving. With the two digital inputs four different states are possible, but one of the states (UP = high, DOWN = high) is prevented with the use of an additional AND gate which resets both flip flops when this state is arising. The possible

states are shown in Figure 2.13.

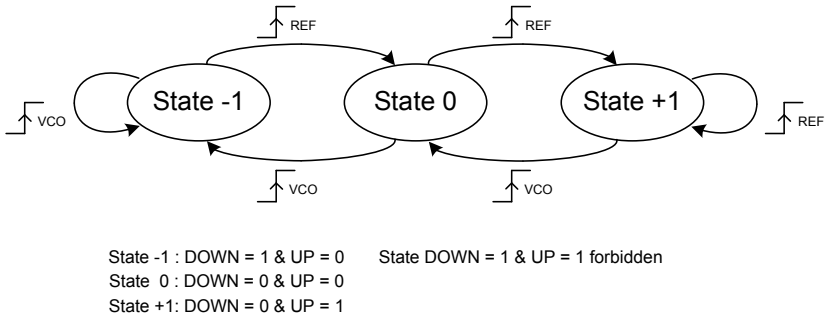


Figure 2.13: PFD State Diagram [8]

Frequency Detector We assume the loop is not locked, and the reference frequency is much higher than the divided output frequency, and so more rising edges are sensed by the PFD on the REF input before a rising edge on the VCO input occurs. With every rising edge on REF, the state is increased from -1 to 0, from 0 to $+1$ and so on. If we reach state $+1$ every additional edge also yields state $+1$. State $+1$ does also mean the UP output is activated (logical high), the switch in the UP branch of the charge pump is closed, and so the capacitor is charged by a constant current Iq_1, and therefore its voltage is rising. This increases the output frequency of the VCO until the point where both input frequencies of the PFD are almost identical (Figure 2.14) [3].

As the difference between both frequencies gets smaller and smaller less rising edges on the REF input are sensed before a rising edge on the VCO input occurs, and so the probability to reach state $+1$ gets smaller and smaller, while the probability for state 0 rises. For almost identical frequencies, the state is periodically changed between state 0 and state $+1$. In this way the frequency detector functionality stops, because the frequencies are identical, and the phase frequency detector will work as a phase detector.

Phase Detector If both input frequencies are equal the PFD does phase detection (Figure 2.15) [3]. If for example on the REF input a rising edge is sensed, then the UP output is activated until a rising edge on the VCO input is found, which then sets the second flip flop output to high. The AND gate detects the two activated outputs, and resets both flip flops. The time between the two rising

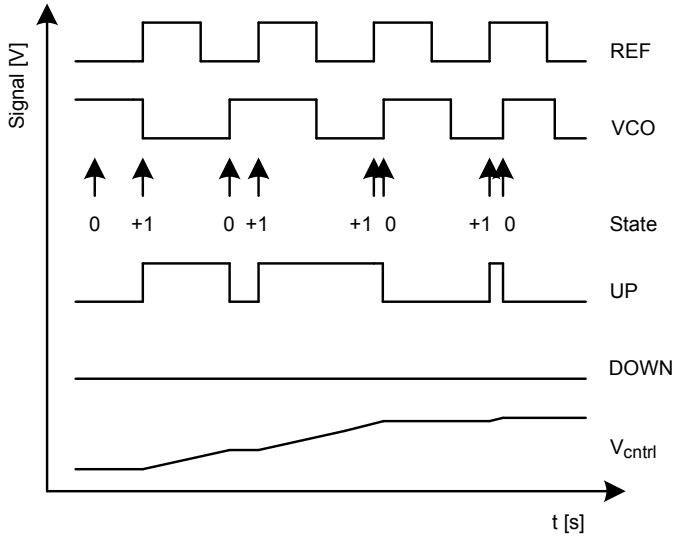


Figure 2.14: PFD Frequency Detector Time Behaviour

edges on the inputs determines the duty cycle of the switching signals UP/DOWN to the current sources, which are then charging or discharging the capacitor. The phase difference (=phase error) determines the output voltage after the loop filter.

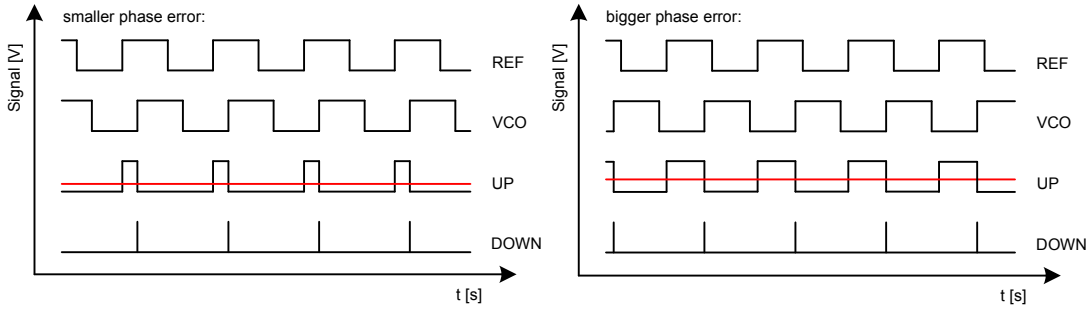


Figure 2.15: PFD Phase Detector Time Behaviour

The average loop filter DC output voltage as a function of the input phase error can be seen in Figure 2.16. The well-defined area of the transfer function is for the PFD $\pm 2 \cdot \pi$ [3].

2.3.3 Loop Filter

The loop filter filters out high frequency signal parts from the phase detector output signal, and creates the DC average voltage for the VCO control input. The loop filter and its parameters have a huge impact on the PLL behaviour.

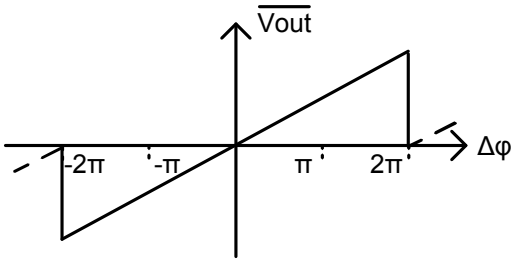


Figure 2.16: PFD Transfer Function

Very Basic PD + no Filter

A phase locked loop with an order of one is only possible without a loop filter, or if the loop filter is frequency independent [8]. So the loop filter transfer function equals $H(s) = A$. The setup is shown in Figure 2.17.

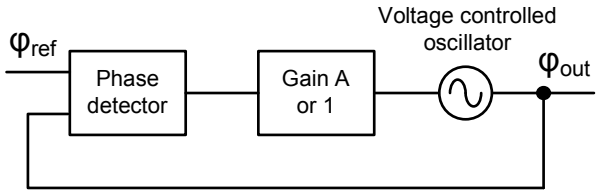


Figure 2.17: Order One Phase Locked Loop

The open loop transfer function is:

$$G(s) = \frac{Kpd \cdot Kvco \cdot A}{s} \tag{2.12}$$

The closed loop transfer function is:

$$T(s) = \frac{\varphi_{out}(s)}{\varphi_{ref}(s)} = \frac{G(s)}{1 + G(s)} \tag{2.13}$$

$$T(s) = \frac{Kpd \cdot Kvco \cdot A}{s + Kpd \cdot Kvco \cdot A} \tag{2.14}$$

The highest occurring power of s in the closed loop transfer function denominator is one, and so is the order. Often $A(s)$ equals 1, and so the gain remaining in the open loop transfer function is Kpd and $Kvco$. If the loop is closed, the only pole

moves from its zero position to the new position [8]

$$p1 = -Kpd \cdot Kvco \cdot A \tag{2.15}$$

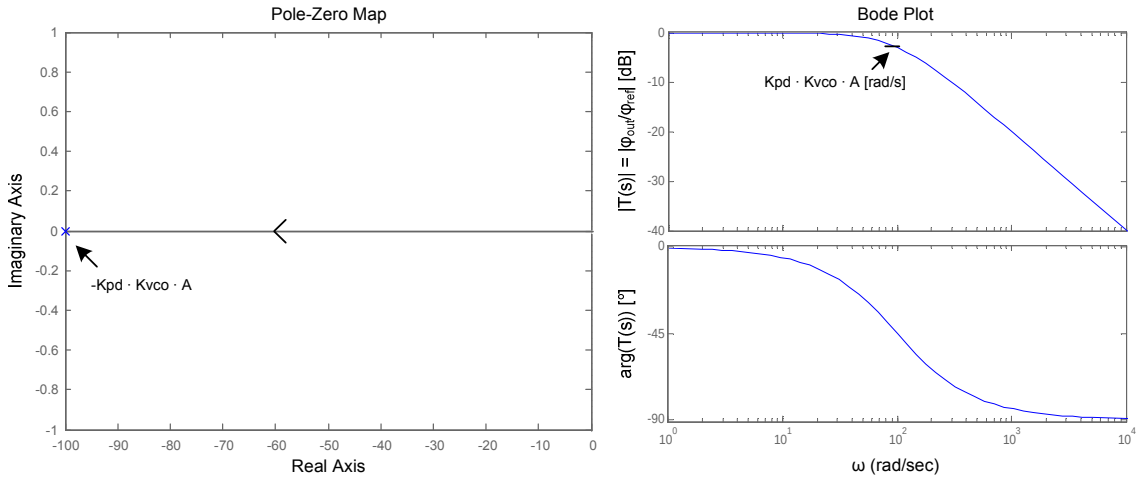


Figure 2.18: Order One PLL Bode Plot and s-Plane [8]

The closed phase locked loop has the $-3dB$ bandwidth of $Kpd \cdot Kvco \cdot A\ [rad/s]$, and behaves like a low pass filter, as can be seen in 2.18.

Very Basic PD + RC Lowpass Filter (Lag)

The loop filter consists of a resistor R and a capacitance C [8]. The phase detector in this case is a simple XOR or a JK flip flop type. The only integrator in the loop is the voltage controller oscillator, and so the loop will be of type I, but also of order 2. The circuit is illustrated in Figure 2.19.

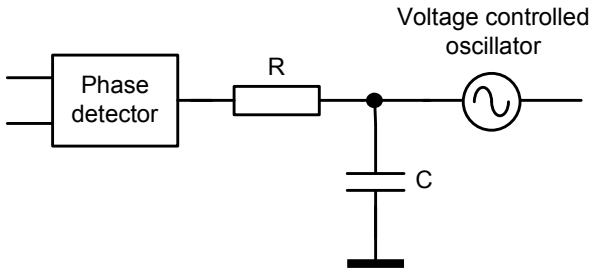


Figure 2.19: RC Lowpass Loop Filter

The loop filter transfer function is

$$H(s) = \frac{1}{1 + s \cdot R \cdot C} \tag{2.16}$$

With the gain of the phase detector and the voltage controlled oscillator one can find the whole open loop transfer function:

$$G(s) = \frac{Kpd \cdot Kvco}{(1 + s \cdot R \cdot C) \cdot s} \tag{2.17}$$

The second order of s under the fraction comes from the integrating behavior of the voltage controlled oscillator in the phase model. To get the closed loop transfer function we calculate

$$T(s) = \frac{G(s)}{1 + G(s)} \tag{2.18}$$

$$T(s) = \frac{Kpd \cdot Kvco}{(1 + s \cdot R \cdot C) \cdot s \cdot (1 + \frac{Kpd \cdot Kvco}{(1+s \cdot R \cdot C) \cdot s})} \tag{2.19}$$

$$T(s) = \frac{Kpd \cdot Kvco}{Kpd \cdot kvco + (1 + s \cdot R \cdot C) \cdot s} \tag{2.20}$$

$$T(s) = \frac{Kpd \cdot Kvco}{s^2 \cdot RC + s + Kpd \cdot Kvco} \tag{2.21}$$

The highest occurring power of s in the closed loop transfer function denominator is two, and so this loop is second order. Using an often used equation form in the control theory this equation can be rewritten as [3]:

$$T(s) = \frac{\omega_n^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2} \tag{2.22}$$

with

$$\omega_n = \sqrt{\frac{1}{R \cdot C} \cdot Kpd \cdot Kvco} \tag{2.23}$$

$$\zeta = \frac{1}{2} \cdot \sqrt{\frac{1}{R \cdot C \cdot Kpd \cdot Kvco}} \tag{2.24}$$

Expression ω_n is called natural frequency, and ζ is the damping ratio. Depending on these two parameters, the behaviour of the phase locked loop changes completely. If $\zeta > 1$ then the system is overdamped, which means the transient response of the loop has the form of two exponentials, and no overshooting occurs. Otherwise if $\zeta < 1$ then the system is called underdamped, and overshooting occurs, but the loop transponse will be very fast [3]. So with these two parameters a trade between settling speed and overshooting can be done. Two different example frequency step reponses with different damping ratios of the loop are shown in Figure 2.20.

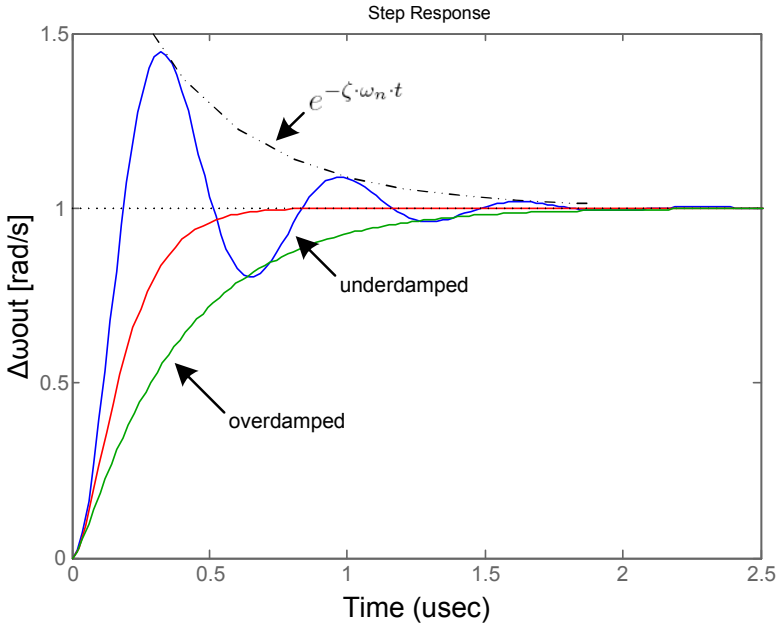


Figure 2.20: Possible Frequency Step Responses [3]

Very Basic PD + Lead-Lag Filter

An additional resistor in the lowpass filter adds a zero to the transfer function, and with it the behaviour of the loop can be further changed [8]. The expanded loop filter is shown in Figure 2.21.

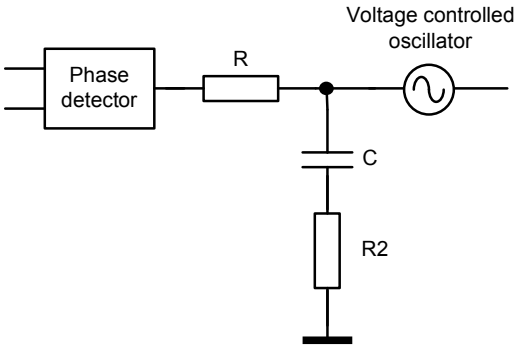


Figure 2.21: Additional Zero implemented (Lead-Lag Filter)

The new transfer function is

$$H(s) = \frac{1 + s \cdot C \cdot R2}{1 + s \cdot C(R + R2)} \tag{2.25}$$

PFD + a single capacitor and an optional resistor

For a type two PLL, two integrators are needed in the open loop so the loop filter must also contain an integrator. In the case of a voltage output phase detector an additional integrator is only possible with an active filter [8], which means more power dissipation. If a phase detector with a charge pump (=current output) is used, a single capacitor at the output delivers an additional integrator [3], and so with a passive filter, a type two PLL is possible.

If the capacitance $C2$ in Figure 2.22 is inserted, and R has a value of zero, then the filter has the transfer function of an integrator, and we have realized a type two PLL. But two integrators in a control system without additional corrective actions are unstable [3]. To obtain stability only a resistor R is needed in series to the capacitor, and it creates an additional zero in the transfer function. Its position can be set, so that we get enough phase margin at the gain crossover frequency to make the loop stable.

A drawback of this resistor is that every current impulse into or from the filter creates a voltage ripple at the loop filter output, which then translates to a ripple in the VCO output frequency [3]. A little change to the filter can attenuate this effect as presented in Figure 2.23. A part of the old capacitance $C2$ from the last filter variant is now put into a new capacitor $C1$. In this way less ripple is produced, because in the first moment of a new current pulse into or from the

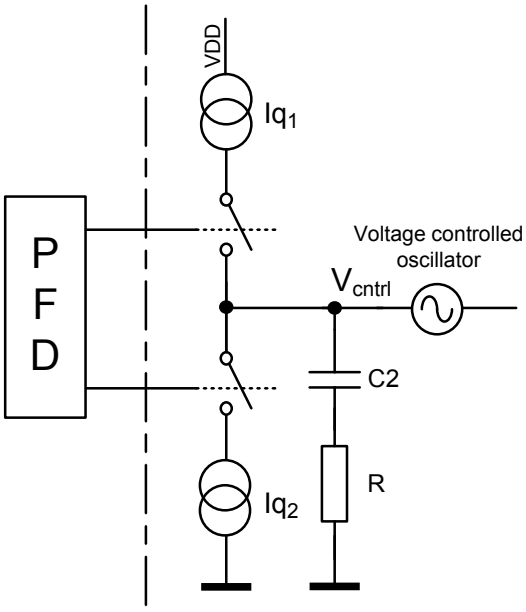


Figure 2.22: Simple Loop Filter (with Integrator)

filter this current can pass capacitor $C1$, and does not introduce a troublesome voltage at R.

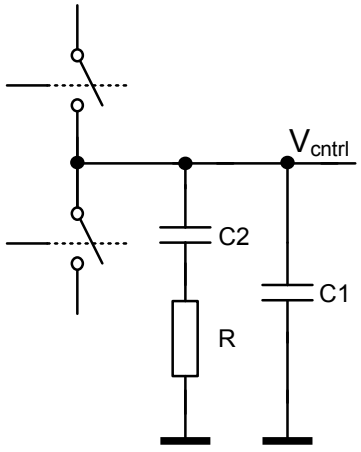


Figure 2.23: Improved Voltage Ripple Performance

PFD + 3rd Order Loop Filter

The order can be increased again by adding a low pass filter to Figure 2.23. The result is shown in Figure 2.24 [1]. This loop filter is used in this diploma thesis, and so its transfer function should also be presented here.

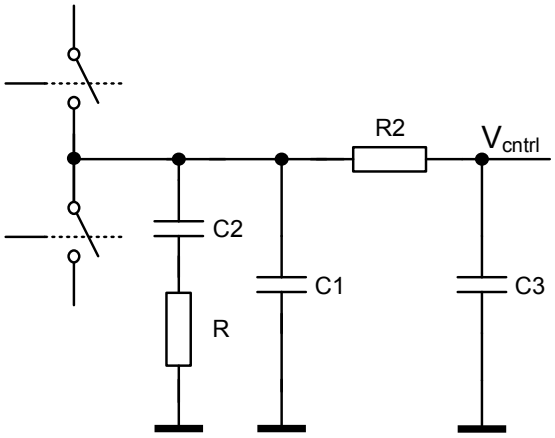


Figure 2.24: 3rd Order Loop Filter

The following equations can be found in [1]:

$$H(s) = \frac{1 + s \cdot R \cdot C2}{s \cdot (A2 \cdot s^2 + A1 \cdot s \cdot A0)} \tag{2.26}$$

with

$$A0 = C1 + C2 + C3 \tag{2.27}$$

$$A1 = C2 \cdot R \cdot (C1 + C3) + C3 \cdot R2 \cdot (C1 + C2) \tag{2.28}$$

$$A2 = C1 \cdot C2 \cdot C3 \cdot R \cdot R2 \tag{2.29}$$

2.3.4 Feedback Divider

Division by an integer value

It is sufficient for many applications if the output frequency can be set in integer multiples of the reference frequency, and this can be achieved with a frequency divider N in the feedback path [3, 1]. If the reference frequency is not small enough to achieve the needed output frequency resolution, a fractional PLL can be used instead. An integer PLL has the advantage that it is less complex.

Frequency division is often achieved with flip flops in toggle configuration, if the division factor is fixed, and the frequency can be divided by a factor of 2^b, where

b equals the number of devices. A implementation which can be synchronious or asynchronious is seen in Figure 2.25.

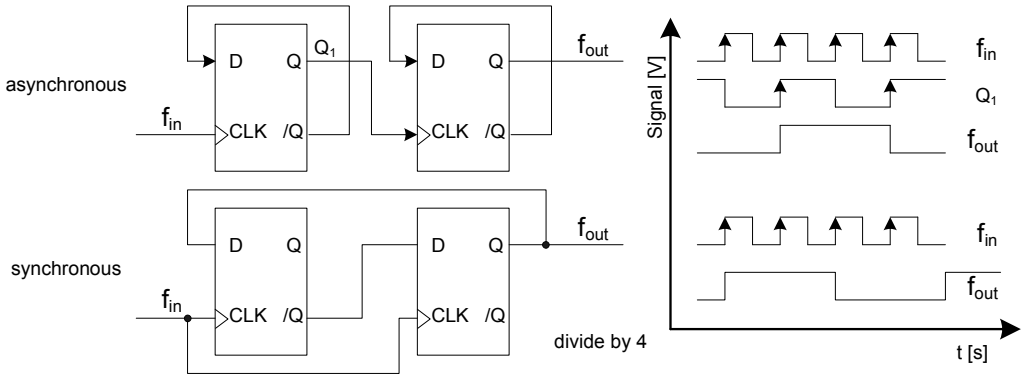


Figure 2.25: Fixed Frequency Divider

Should the output frequency be digitally programmable often binary counters are used. It counts every time a rising or a falling edge occurs. After $b = 2^n - r$ input signal edges it overflows, where n is the number of bits of the counter, and r is the value which is reloaded to the counter after every overflow. So the frequency is divided by a factor of b. In comparision to binary counters a flip flop divider saves power and area, and so they are used as a prescaler in front of programmable binary counters.

Delta-sigma fractional-N phase locked loop

If the frequency resolution of a integer PLL is not enough, a fractional-N phase locked loop (Figure 2.26) can be used, which allows the multiplication of the reference frequency with a configurable rational number [1]. Its feedback divider can divide the output frequency by N or by $N + 1$, and the active divider setting is changed over time. For example, 9 periods of the input reference signal the output frequency is divided by 300 (=N), and then one period it is divided by 301 (=$N+1$). The average of the divider settings is $(9 \cdot 300 + 1 \cdot 301)/10 = 300.1$. So the output frequency is $300.1 \cdot fref$. The loop filter filters out the higher frequencies which are generated at the output of the PDF because of the switching action.

A downside of a fractional-N PLL is that the periodic change of the divider does generate fractional spurs, which increases the noise inside the phase locked loop [1].

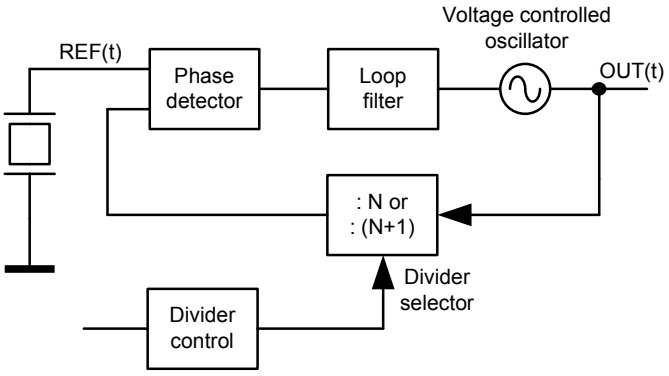


Figure 2.26: Fractional-N PLL Architecture

If the divider setting of a fractional-N PLL is not changed periodically, but is controlled by a delta-sigma converter, therefore set in a random manner, the problem with the fractional spurs can be improved. The noise at the PFD output is moved to higher frequencies, and so the lowpass loop filter can filter out more of it. So the delta-sigma converter helps to improve the performance [1].

2.4 Operation

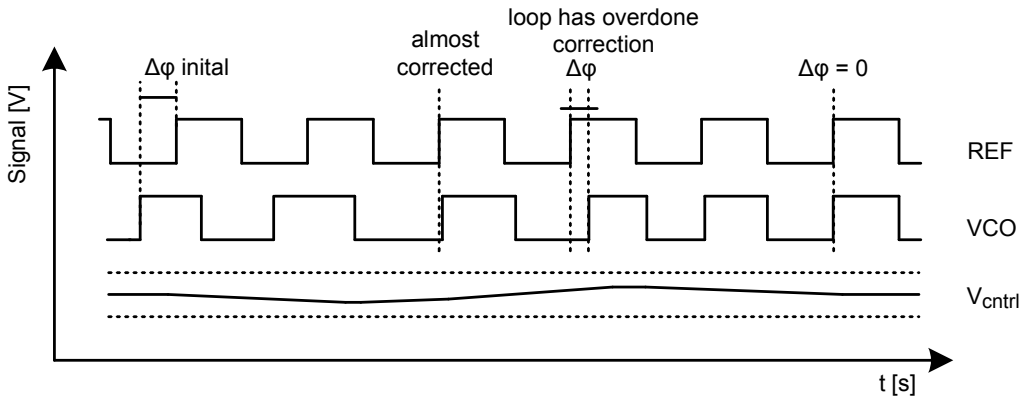


Figure 2.27: Typical PLL Time Behaviour

The function of a phase locked loop should be described based on an example which is shown in Figure 2.27. If for example the output signals phase does lead in time in comparison to the reference signal, then the phase detector decreases the VCO control voltage, and with it also the output frequency a little bit. This small frequency drop is enough to allow the phase of the reference signal to catch up,

and the phase error gets smaller with time. While the error decreases, the VCO slowly speeds up. At some point a phase error of zero would be reached, but it is most likely that the loop will not respond fast enough to this zero phase error, and will overdo the correction of the initial error.

Now the reference signals phase is leading, and the phase detector has to speed up the VCO until the phase of both signals is equal again. Some time later the loop will reach a stable operating condition where both signals have the same phase state, or are only misaligned by a phase error which is constant over time, and this is called the ”locked state”. From then on the loop will try to follow slower phase changes of the reference signal with the phase of the output signal.

2.5 Models

2.5.1 Phase Model

In the locked state the phase detector behaves like a linear block, because the phase error never grows above the boundaries where the phase detector transfer function gets ambiguous, thus there is a linear relationship between the phase error and the output of the phase detector [4].

This linear relationship allows to describe the PLL and its behaviour in a phase model [9]. A basic model is shown in Figure 2.28. Instead of using a voltage or current of a real signal inside the PLL, the phase of all signals is used as the information parameter. At the PLL input, the phase of the reference signal is injected and at the output the phase of the output signal can be derived.

The advantage of such a simplified model is that the phase model delivers the time response of a PLL, which we are interested in, without doing a very time and resource consuming transient simulation of the whole circuit in the time domain [9]. We do not get the value of all the voltages and currents inside the circuit over time from this model.

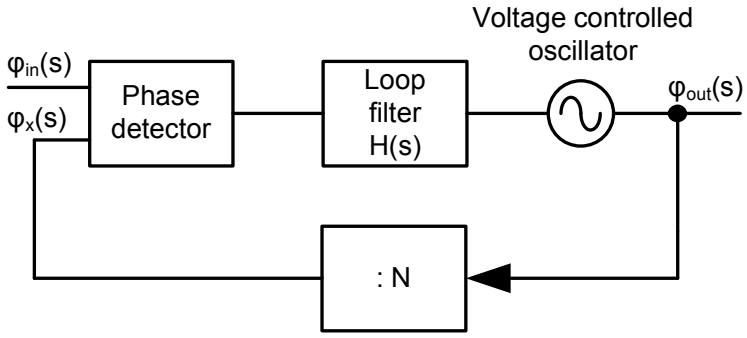


Figure 2.28: Linear PLL Phase Model [3]

Building Blocks

Phase Detector Because our model is in the phase space, the modelling of the phase detector can be simply done as a subtracter, which calculates the phase difference between both inputs 2.29 [3]. The so called gain of the phase detector (=Kpd) describes how steep the relationship between the phase error and the average VCO input voltage is (Figure 2.30).

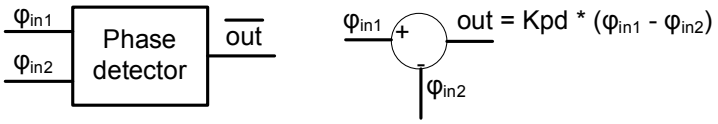


Figure 2.29: Phase Detector Model

The output of the phase detector can be calculated with:

$$\overline{Vout} = (\varphi_{in1} - \varphi_{in2}) \cdot Kpd \tag{2.30}$$

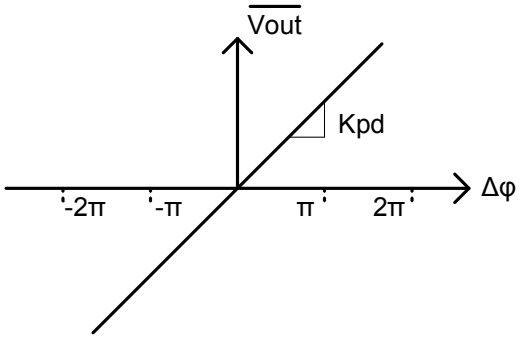


Figure 2.30: Phase Detector Transfer Function [3]

Loop Filter The output signal from the phase detector is translated into the input control voltage of the VCO by the loop filter [3]. Figure 2.31 shows the loop filter.

Figure 2.31: Loop Filter Model

The transfer function of the loop filter is:

$$H(s) = \frac{Y(s)}{X(s)} \tag{2.31}$$

with $Y(s)$...output signal, $X(s)$...input signal

Voltage Controlled Oscillator The output frequency is controlled by the control voltage at the input of the VCO, and in the ideal case this relationship is perfectly

linear. To get the phase of the output signal for the phase model we use the following equation:

$$\varphi(t) = \int_0^t \omega(\tau)\, d\tau \tag{2.32}$$

To derive the phase of the output signal we integrate over the output frequency $\omega(\tau)$ of the VCO [3]. So in the phase model the VCO is working as an integrator, and the relationship between the input control voltage and the frequency deviation of the output frequency is called the gain of the VCO (=$Kvco$ [$\frac{Hz}{V}$]). See Figure 2.32 for details.

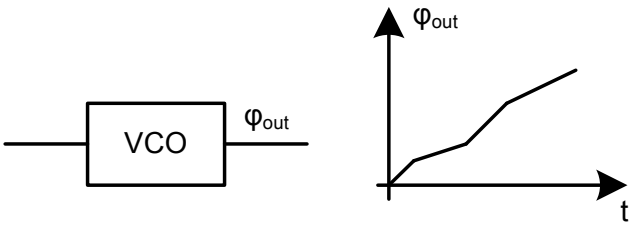


Figure 2.32: Voltage Controlled Oscillator Model

Transfer function of a VCO [3, 9]:

$$H_{vco}(s) = \frac{\varphi_{out}(s)}{v_{cntrl}} = \frac{Kvco}{s} \tag{2.33}$$

with v_{cntrl}...input control voltage signal of the VCO

Frequency Divider To find the model for a divider with a division factor of N in the phase space, we can use equation 2.5.1. If we divide the frequency through a constant value N over time, this constant value can be prescind from the integral, and the phase of this signal is divided by the same value.

$$\varphi(t) = \int_0^t \frac{\omega(\tau)}{N}\, d\tau = \frac{1}{N} \cdot \int_0^t \omega(\tau)\, d\tau \tag{2.34}$$

The model for a feedback divider is therefore (Figure 2.33)

$$H_{Divider}(s) = \frac{\varphi_{out(s)}}{\varphi_{in(s)}} = \frac{1}{N} \tag{2.35}$$

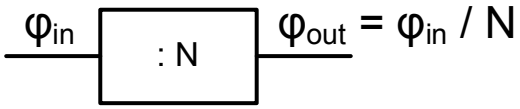


Figure 2.33: Frequency Divider Model

Reference Oscillator Because we need to feed the phase of the reference signal into the phase detector, we firstly have to do a frequency-to-phase space conversion as we did with the VCO. So we integrate the frequency.

PLL Characterization

- Order of a PLL

  The order of a PLL is found with the highest occurring power of the variable s in the closed loop transfer function denominator of the phase-locked loop [8].

- Type of a PLL

  The PLL type is found by the number of integrators in the open loop transfer function [8]. Because every VCO is itself an integrator in the phase model, all PLL types are at least one.

Transfer Functions

The open loop transfer function $G(s)$ is

$$G(s) = \frac{Kpd \cdot Kvco \cdot H(s)}{s} \tag{2.36}$$

For calculation of the output response of the loop to an input signal variation, the closed loop transfer function is important. It tells us how the phase at the ouput

node of the loop responds to a phase signal at the reference input of the loop. The closed loop transfer function is derived from the open loop transfer function.

$$T(s) = \frac{G(s)}{1 + \frac{G(s)}{N}} = \frac{\varphi_{out}(s)}{\varphi_{in}(s)} \tag{2.37}$$

$$T(s) = \frac{Kpd \cdot Kvco \cdot H(s)}{s \cdot (1 + \frac{Kpd \cdot Kvco \cdot H(s)}{s \cdot N})} = \frac{Kpd \cdot Kvco \cdot H(s)}{s + \frac{Kpd \cdot Kvco \cdot H(s)}{N}} \tag{2.38}$$

The bode plot of $T(s)$ (Figure 2.34) tells us how the closed loop responds to sinusoidal signals at the reference input. For low frequencies $\omega \ll \longrightarrow T(s)$ becomes N. In this case the output phase follows the input phase(see also [3]), and the relationship between the output and input equals N. For $\omega \gg \longrightarrow T(s)$ becomes zero, and the input phase changes can not be seen anymore at the output of the system. At a specific frequency the output signal is attenuated by $-3dB$, and this frequency is called the $-3dB$ bandwidth. A typical bode plot for $T(s)$ is presented in Figure 2.34.

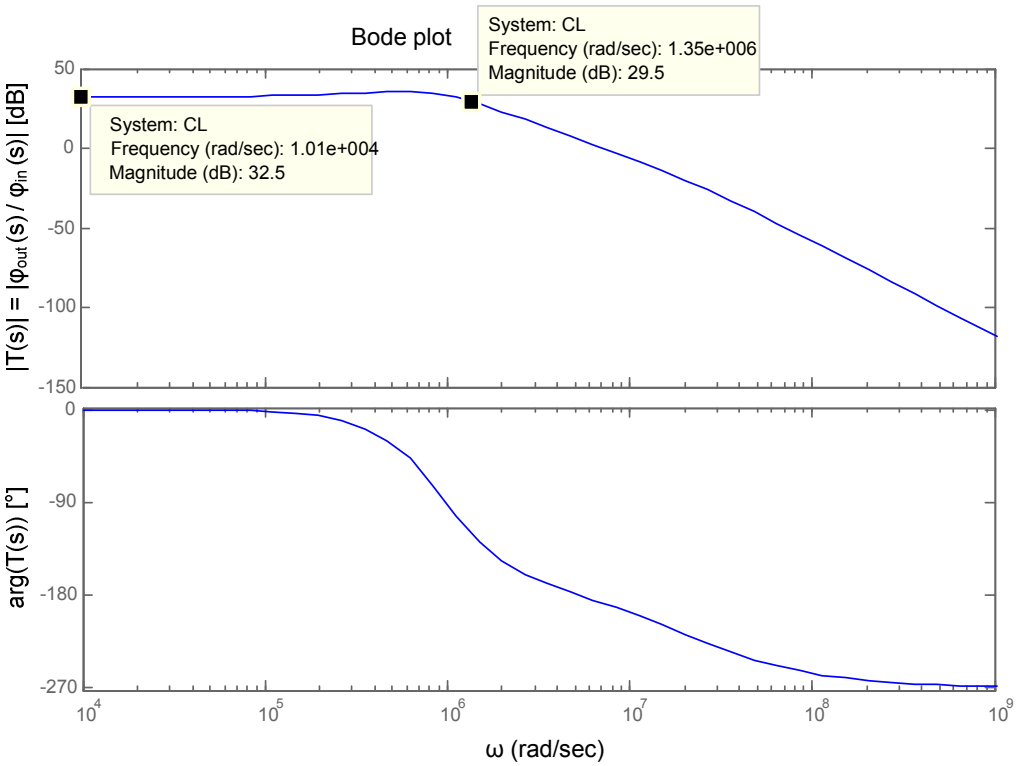


Figure 2.34: Closed Loop Transfer Function Bode Plot with Bandwidth

2.5.2 Voltage Model

The voltage model was created to gain the ability to run a transient simulation for the whole system consisting of the PLL and the bandwidth calibration circuit. In the voltage model, voltages and currents are used as the information parameters, thus information, which is not delivered by a phase model [9], about these variables over time is gained. All input and output signals are now time domain signals with a specific frequency, and so for example a time-to-digital converter can be used directly on the output of the PLL circuit to measure the output period in a simulation. A downside to this model is the higher amount of computing power which is needed.

Phase Frequency Detector

The phase frequency detector is constructed with digital gates, and its basic architecture is introduced in Figure 2.12. The circuit used in the transient simulation is more complicated, in order to get better accordance with the implemented circuit. The two output signals UP and DOWN of the phase frequency detector switch on or off two ideal current sources which represent the charge pump. This output current is then fed into the $3rd$ order loop filter.

Loop Filter

The loop filter is constructed with passive elements (Figure 2.24).

Voltage Controlled Oscillator

The voltage controlled oscillator is described in Verilog-A [9], and it does accept a voltage at its control input. The Verilog-A code does create the corresponding rectangular output signal. This signal is then feed into the feedback divider.

Feedback Divider

The divider is also a Verilog-A model. The divider allows the division of the input frequency by the integer N. The integer N is controlled by the voltage of a control input signal. In this way the divider can be used as a division by N or $N + 1$ circuit for the use in a fractional-N phase locked loop. The divider itself has an

internal variable which counts the rising edges from the frequency input signal. If this variable reaches the value of N, then the output signal state is changed and the internal variable is set back to zero.

$\Delta\Sigma$ Converter

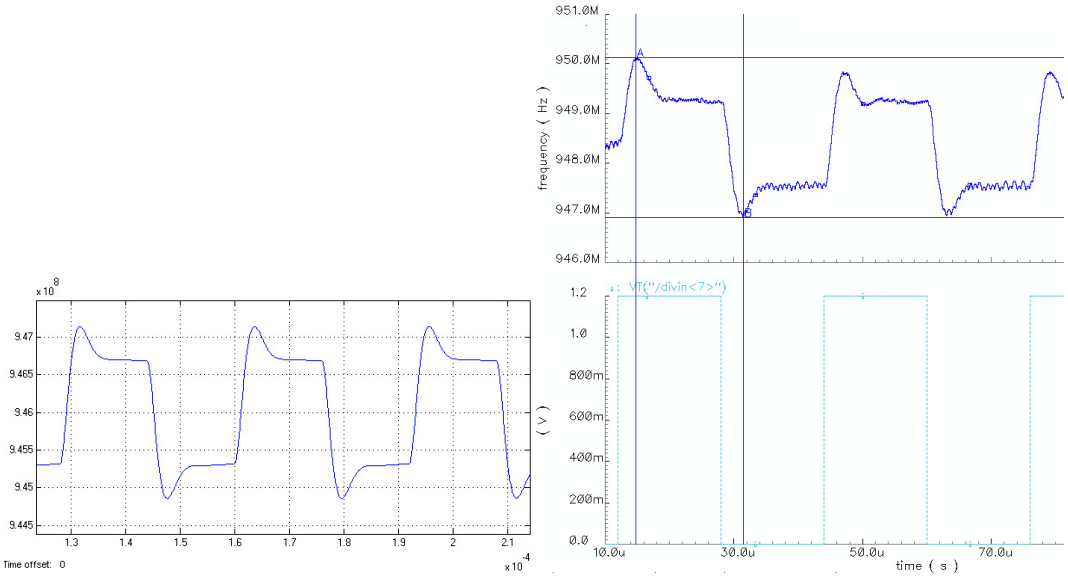
Because the phase locked loop which is used in this diploma thesis is a delta-sigma fractional-N PLL, a model for a converter was also necessary. The converter is also a Verilog-A model, which allows the output frequency of the PLL to be set in steps smaller than the reference frequency.

2.5.3 Comparison

A comparision between the phase and voltage model was done. The phase model was simulated in Simulink, and the voltage model in a transient simulation in Spectre. First the loop responses to a single output frequency change were compared, and it is important that the amount of overshoot, the settling time, and the final output frequency are equal. Both models fit well together.

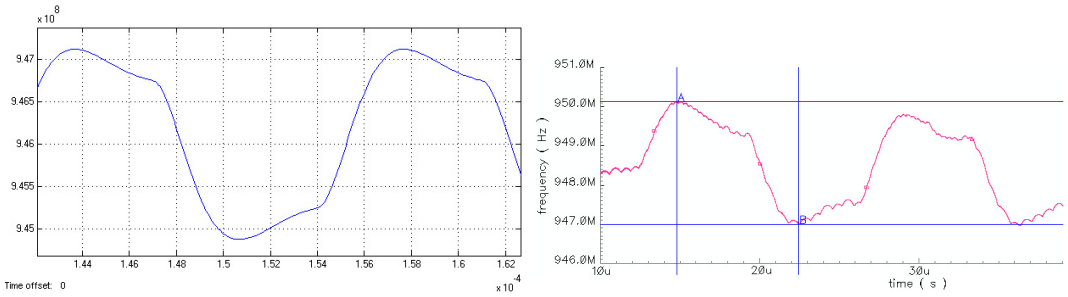
In a second step the feedback divider was periodically modulated in a rectangular manner, and for both models the output frequency trend was derived. Both results do fit together for all used divider switching frequencies. Because the reference frequency was slightly different in the Spectre simulation, the absolute value of the output frequency is not exactly the same as in Matlab, but the time behaviour is equal.

The waveforms in Figure 2.35b 2.35d 2.35f 2.35h are the result of transient simulations of the voltage model with different modulation frequencies fm. For comparision reasons in Figure 2.35a 2.35c 2.35e 2.35g the same results from SimuLink are shown.



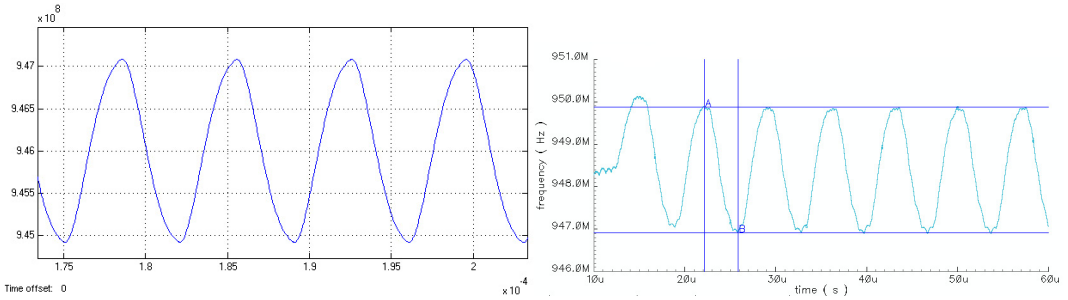
(a) Phase Model (b) Voltage Model

Figure 2.35: $fm = 31\ kHz$



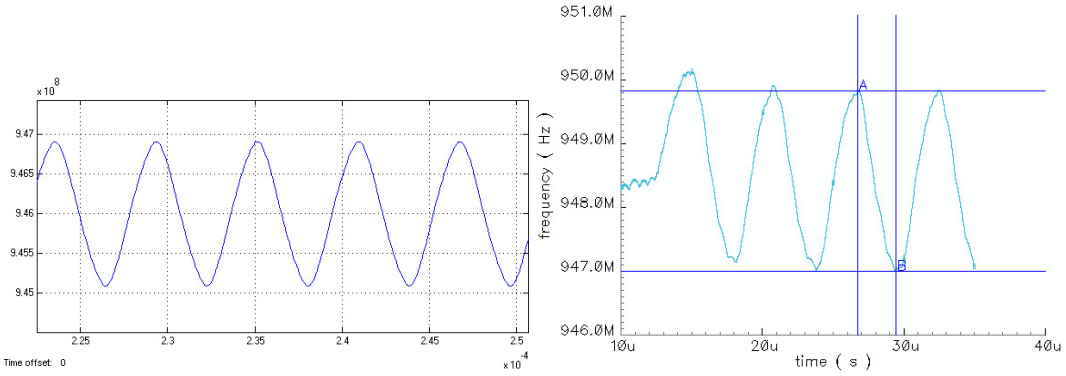
(c) Phase Model (d) Voltage Model

Figure 2.35: $fm = 72\ kHz$



(e) Phase Model (f) Voltage Model

Figure 2.35: $fm = 142\ kHz$, PLL output frequency vs. time results for the phase and voltage model



(g) Phase Model

(h) Voltage Model

Figure 2.35: $fm = 172\ kHz$

3 Time-to-digital Conversion

The time-to-digital converter is used in this concept to observe the output signal period time of the phase locked loop and to obtain a digital number for the closed loop bandwidth of the PLL under test. An introduction to this topic is given in this chapter.

3.1 Typical Applications

TDC circuits are often used [10] in science [11, 12, 13, 14], especially in particle detectors [15] or time-of-flight detectors [16, 17]. Examples of such uses are how distance can be measured with the help of a laser device, or more exotic applications like time correlated imaging, which uses an array of a lot of smaller time-to-digital converters can be found [18]. Other applications use a TDC as a very fast analog-to-digital converter [19], or for the measurement of time jitter [2]. And also in the field of phase locked loops they are used as phase frequency detectors in newer architectures [20, 21].

3.2 Methods

Different possibilities are shown in [22, 10].

3.2.1 Analog Time Stretching

This technique allows the measurement of small time intervals with a relatively simple circuit (Figure 3.1) [22]. During the unknown time interval T, a capacitor C is charged with a constant current of $I_1 - I_2$, and the voltage over C is increased in a linear manner. Afterwards C is discharged again by a constant current I_2 which is smaller than I_1, and its voltage decreases again. A fast comparator enables a

counter for the discharge time. The counter counts with a reference frequency, and from the final counter output the now stretched time interval $T + Tr$ can be found.

The time stretching factor is given by [22]:

$$K = \frac{I_1 - I_2}{I_2} \tag{3.1}$$

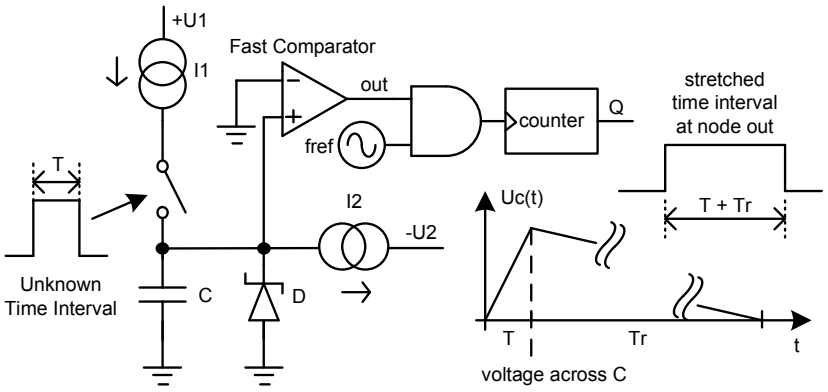


Figure 3.1: Analog Time Stretching [22]

This technique is now rarely used in favor of digital time stretching (e.g. vernier oscillators), because it is more difficult to implement the needed high precision current sources in small analog circuits [22].

3.2.2 Time to Voltage Conversion

This method also uses a capacitor C which is charged with a constant current during the unknown time interval, but instead of discharging it again, the voltage at the capacitor is held and digitized by an analog-to-digital converter [22]. The duration of the time interval is found by the digital output word. The performance depends greatly on the analog-to-digital converter.

3.2.3 Tapped Delay Line

A line of matched delay elements is used to measure a time interval [22, 10, 12, 17]. A signal is applied to the first element when the start signal arrives, and it

propagates from element to element until the end of the line. If all delay element outputs are evaluated after the unknown time interval T at the stop event, then T can be measured from the number of elements with a changed output state in this interval. Time T equals the propagation delay through a delay element multiplied with the number of elements. To get the absolute value of the time interval T the delay time of all elements have to be known exactly. Buffers or inverters are often used delay elements. A typical configuration is shown in Figure 3.2.

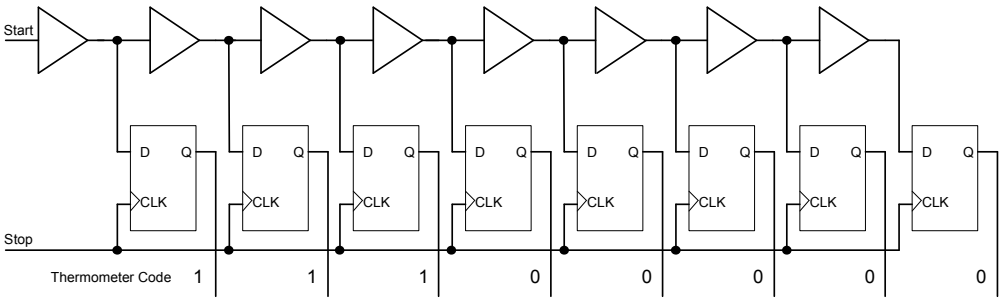


Figure 3.2: Tapped Delay Line [22]

The propagation delay changes with temperature, process parameters, or with the supply voltage. Stabilizing the delay over all operating conditions is not an easy task. Often the delay elements are embedded in a delay-locked-loop which stabilizes the propagation delay through the whole chain [17, 12]. Another possibility is to correct the measurement results digitally, without stabilizing the propagation delay. The needed reference can be gained by the measurement of a signal with a well known time duration. The resolution of this time measurement method is given by the delay of a single element.

3.2.4 Pseudo-Differential Delay Line

If two single ended delay lines are laid out parallel and an impulse is fed at the same time into both of the lines differentially, a pseudo-differential delay line can be built [20]. Differential flip flops can be used to monitor the state of the output nodes. The advantage is a better immunity against supply and substrate noise.

3.2.5 Vernier Delay Line

The vernier delay line [22] is related to the vernier caliper or micrometer which is used to measure mechanical dimensions accurately. It uses two delay lines, one with slower delay elements (in this case latches, delay tp_a), and a second one with slightly faster elements (here buffers with smaller delay tp_b). The start signal is sent into the slow line, and the stop signal into the slightly faster line. Both signals propagate with a small delay difference of $tp_a - tp_b$, and so over time the faster travelling stop signal which was started later catches up with the slower start signal. Between opposite nodes of the two lines, so called arbiters (in this example also the latches) compare their states, and if a first transition occurs it remembers which node it happened at. Until the point in the line where the faster signal catches up the slower one, the outputs of the latches can be set to high, but behind it the propagation in the slower line is stopped. A thermometer code is generated at the output of the arbiters, from which the time interval between the start and stop signal can be measured. The circuit in Figure 3.3 translates the thermometer code to a single high output bit at the stopping position, because every activated latch resets the previous one. The resolution is $tp_a - tp_b$. The drawback is that for a longer time interval a huge amount of delay elements are needed. The increase in resolution is paid with increased complexity. Also a well defined delay difference has to be maintained.

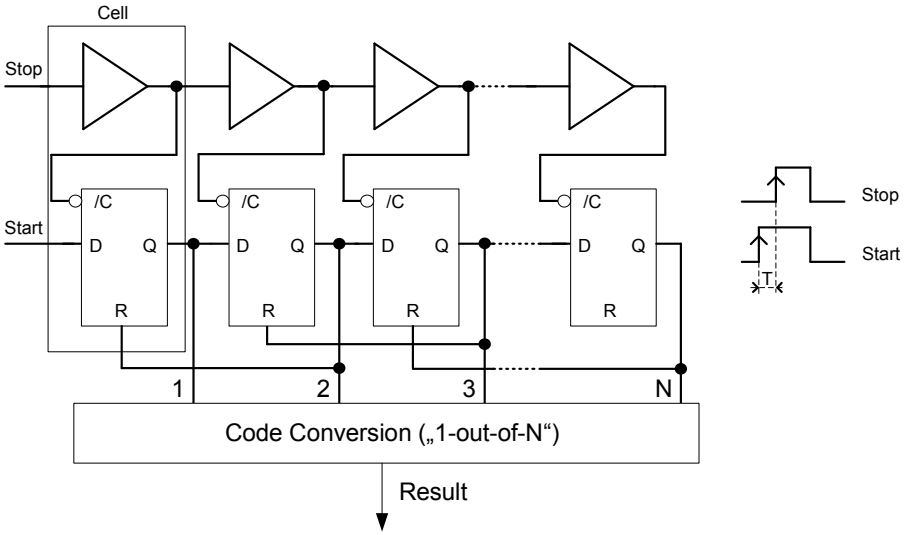


Figure 3.3: Vernier Delay Line [22]

3.2.6 Vernier Oscillators

Vernier oscillators (Figure 3.4) [2, 23, 22] offer increased resolution like a vernier delay line, but with less area needed. They also utilize the vernier scale like the vernier delay line, but instead of a large amout of delay elements in a line they use two oscillators with a small output frequency difference $fout_1 - fout_2$ to measure the unknown time interval. The start signal enables the first oscillator with a defined output signal phase state, and the stop signal the second oscillator with the same start phase state as the first one. Because both oscillators are started at another point in time, their output signal phase states are not equal; but because of the slightly different output frequencies, the phase difference between both outputs varies over time and at one point this difference will get zero. How much the phase difference does change with every output period of the oscillators is controlled by the output frequency difference. A coincidence detector (phase detector) compares both output signals of the oscillators, and if they reach the same output phase state, then both oscillators are stopped immediately. At both oscillator outputs a counter counts the output periods until the coincidence.

From both counter values the unknown time interval is derived [22]. The following equation ignores the quantization error:

$$T = (n_1 - n_2) \cdot T_1 + (n_2 - 1) \cdot r \tag{3.2}$$

with
n_1, n_2...counter output after measurement
T_1...$\frac{1}{fout_1}$, T_2...$\frac{1}{fout_2}$

The resolution of this measurement method is $r = T_1 - T_2$. Building two oscillators with a stable and only small output frequency difference is a challenge. Additional area is needed, if calibration effort has to be done.

3.2.7 Pulse Shrinking

An impulse with a duration of the unknown time interval is injected into a ring of pulse shrinking elements. Every time the impulse has passed the complete ring

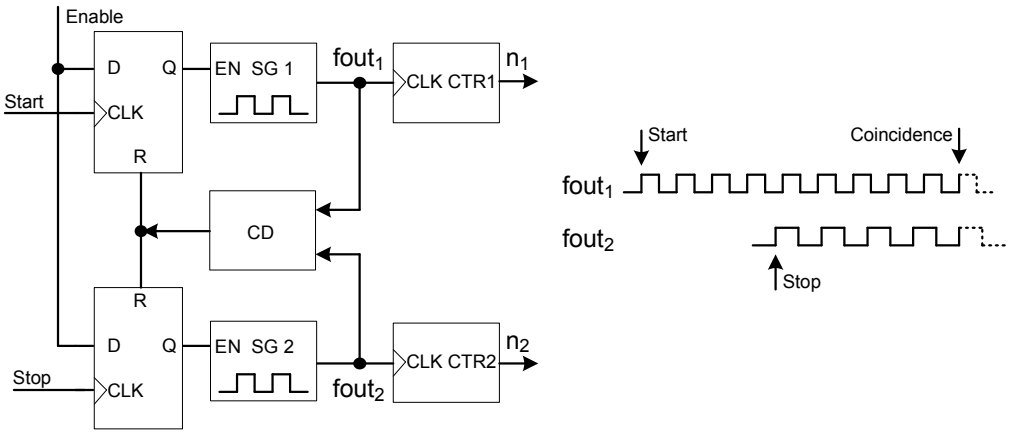


Figure 3.4: Vernier Oscillator Time Interval Measurement Method [22]

and starts a new cycle, its impulse width is shrunk by a certain and well defined amount. So with every cycle the width decreases, and subsequently the impulse fades away. A counter counts the number of full cycles the initial impulse does travel through the shrinking line until it disappears. From the counter value the initial impulse width can be derived [24].

3.2.8 Ring Oscillator

This architecture is related to the tapped delay line [22]. Examples for papers which use this kind of TDC setup are [16, 18, 11, 19, 13, 15]. An advantage is, that the inverters are scaled very well with the used technology.

3.3 Implementation

A ring oscillator architecture is used for the time-to-digital conversion in this diploma thesis. The TDC block (Figure 3.5) is composed of the ring oscillator, two coarse counters, the absolute phase detection circuit, and a calculation unit. The TDC unit measures the time interval between two rising edges of the CLK_{in} input signal.

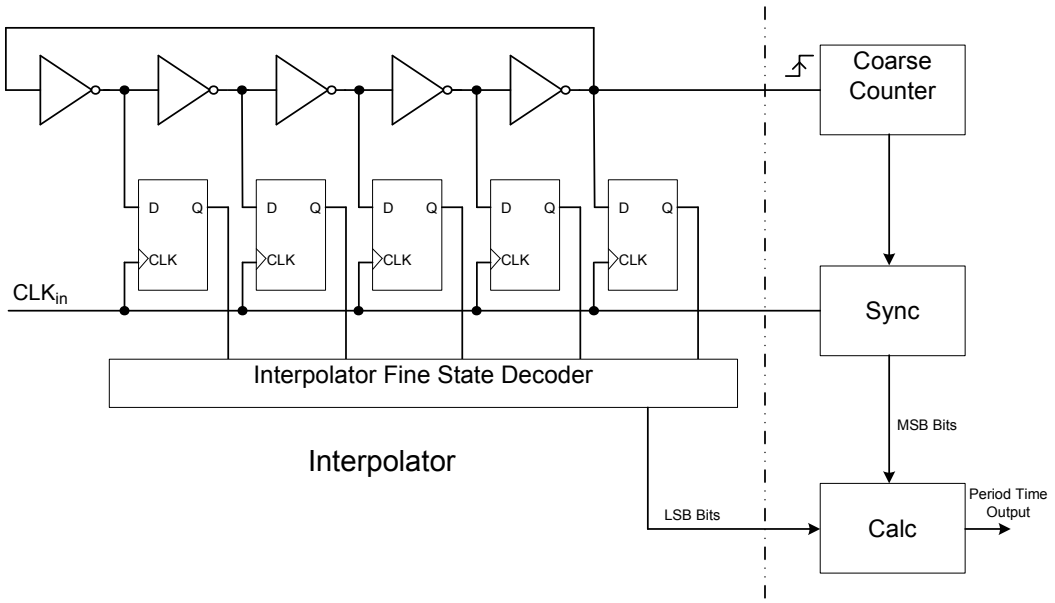


Figure 3.5: Used TDC Unit System Overview

3.3.1 Interpolator

The interpolator (ring oscillator) allows the measurement of a time interval with a resolution equal to the typical inverter delay (=t_d). If the ring uses M inverters then the longest time interval which can be measured without a coarse counter is $2 \cdot M \cdot t_d$. After this time the state of the ring oscillator repeats and is ambiguous. All possible states of a example ring oscillator are shown in Figure 3.6. In the figure every second node of the oscillator is drawn inverted, because this is also done in the circuit.

The differential nonlinearity (DNL) and the integral nonlinearity (INL) [14] depend on the statistic dispersion of the delays of the single inverters from the typical and specified delay. One can build a very high resolution TDC, but if the delay from the inverters is not very well controlled, then the DNL and INL errors inhibit the successful usage of the high resolution. Additional errors are created if the inverters do not have the same propagation delay for both signal transitions. The power supply of the ring oscillator must be filtered, to be as noise free as possible, to obtain a time constant propagation delay.

Determination of the TDC Core Inverter Size The inverter (Figure 3.7) [25] delay depends on the load capactiance at the output, its transistor sizes, and

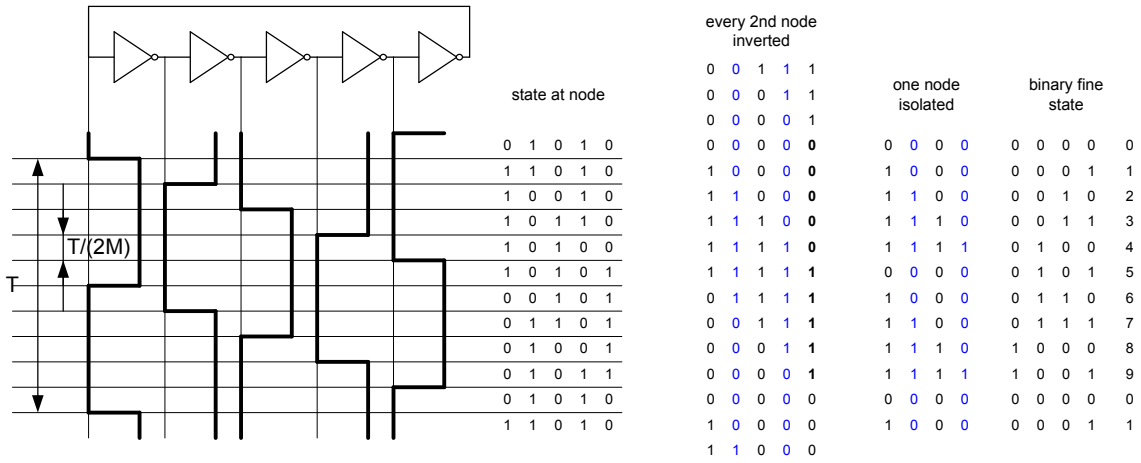


Figure 3.6: Possible Interpolator Fine States

from the process parameters [26]. The load capacity can be divided into a part C_{int}, which consists of the input capacity of the next inverter in the line, and a second part C_{ext}. C_{ext} consists of parasitic capacitors from the output node to GND [25]. Two important examples for C_{ext} are the capactiance from the path which is used to couple the state out from every ring node, and also the input capactiance of the output buffer element. The buffers minimize adverse effects from the output back to the ring oscillator.

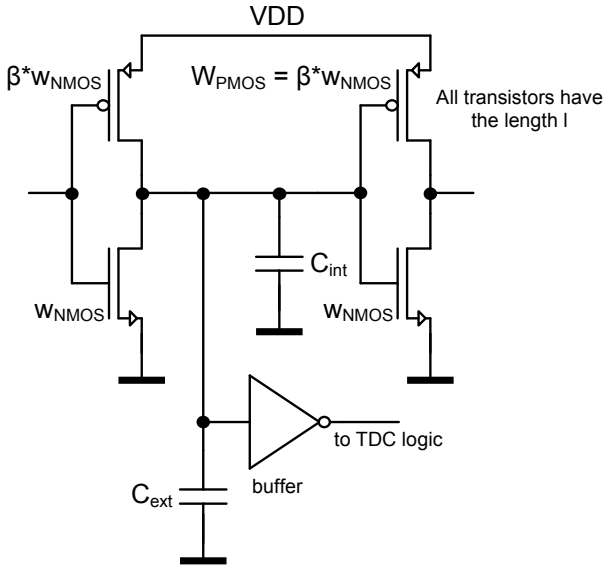


Figure 3.7: TDC Ring Oscillator Output Node Capacity Model [25]

Main part of C_{int} are both gate-source capacities of the inverter transistors. The

length of the transistors is minimized to maintain a very low delay. To cancel the reduced mobility in the PMOS transistor its size W_{PMOS} was selected beta times wider than the size W_{NMOS} of the NMOS counterpart. The value of β was chosen that the propagation delays for both transitions are identical.

C_{int} can be approximated by (see [26]):

$$C_{int} = Cgs_{NMOS} + Cgs_{PMOS} \sim W_{NMOS} \cdot L \cdot C_{ox} + W_{PMOS} \cdot L \cdot C_{ox} \tag{3.3}$$

$$C_{int} \sim L \cdot C_{ox} \cdot (W_{NMOS} + \beta \cdot W_{NMOS}) \sim L \cdot C_{ox} \cdot W_{NMOS} \cdot (1 + \beta) \tag{3.4}$$

C_{int} is proportional to the width of the transistors, and also the current through the transistor I_{ds} in both operating regions [3].

”Linear” Region:

$$I_{ds} = \frac{K \cdot W}{L} \cdot [(U_{gs} - U_{th}) \cdot U_{ds} - (\frac{U_{ds}^2}{2})] \tag{3.5}$$

”Saturation” Region:

$$I_{ds} = \frac{K \cdot W}{2 \cdot L} \cdot (U_{gs} - U_{th})^2 \tag{3.6}$$

If C_{ext} were 0, an increased width of the transistors would increase the output current and the output capactiance by the same factor. In this case the propagation delay does not change, but the power dissipation is increased. This is discussed in [25].

If C_{int} is 0, but C_{ext} is accounted then C_{ext} does not depend on the width of the transistors in the inverter, but with increased width more current is available

for charging and discharging of C_{ext}. So in this case, the propagation delay is inversely proportional to the width of the transistors. In the practical realization both C_{int} and C_{ext} are non zero.

For very small transistors C_{ext} is big in comparision to C_{int}. If the width is increased at this point the propagation delay can be decreased by a large amount. With the growing width of the transistors C_{int} becomes dominant in comparision to C_{ext}, and so the possible propagation delay decreases per width step do become smaller and smaller [25]. Only the dissipated energy in the ring oscillator increases with every step at the end.

This is a tradeoff between the delay and the power dissipation. The width of the transistors was selected in a way that a short delay was reached, but without increasing the power consumption of the ring oscillator too much. A plot of the propagation delay versus the NMOS transistor width is presented in Figure 3.8.

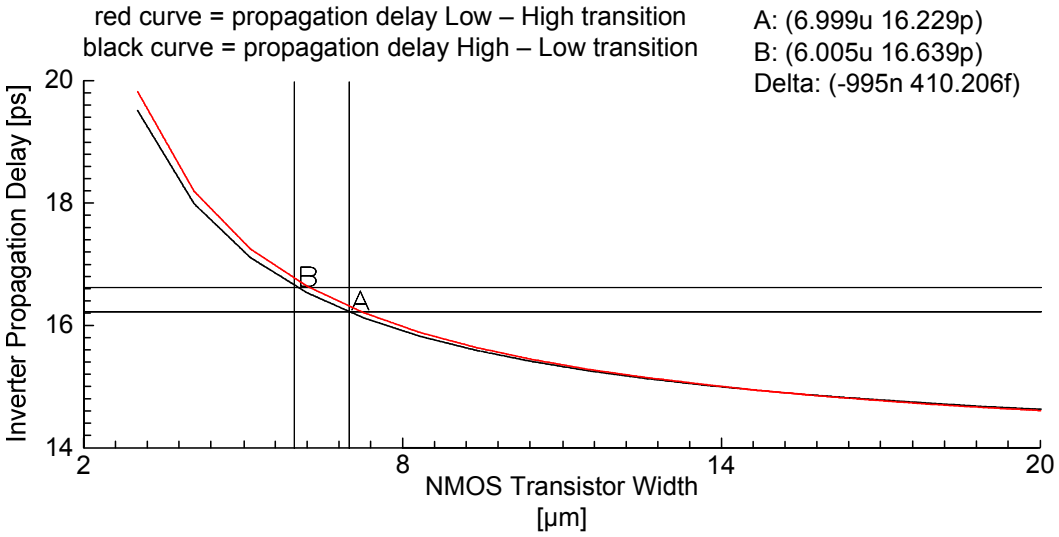


Figure 3.8: NMOS Width Inverter Propagation Delay Dependence

Dissipated Energy per Node While the inverter output node is charged fully from GND to VDD, as much power is dissipated in the PMOS transistor as is stored in the output capactiance at the end [27]. This dissipated energy can be found by

$$C_{node} = C_{int} + C_{ext} \tag{3.7}$$

$$W_{dis} = \frac{1}{2} \cdot Vdd^2 \cdot C_{node} \tag{3.8}$$

At the end of a charge-recharge cycle, the capacitor is discharged again by the NMOS transistor and the whole stored energy in C_{node} is dissipated again. So in a single cycle the dissipated energy is [25]

$$Wdis_{cycle} = 2 \cdot W_{dis} = vdd^2 \cdot C_{node} \tag{3.9}$$

If f cycles occur every second, that means the node is charged and discharged with a frequency of f, then the whole dissipated energy is

$$Wdis_{all} = vdd^2 \cdot C_{node} \cdot f \tag{3.10}$$

This equation does not account for crowbar and leakage currents.

In terms of noise, the effect of the supply voltage on the propagation delay of the delay elements is unwanted [6], because it introduces small variations of the delay over time. In terms of calibrating the delay of the elements by variation of the supply voltage this effect is positive. In this way, delay changes because of process variations or the temperature dependence can be canceled. Figure 3.9 shows the effect of the supply voltage on the delay.

To find out how big or how small the propagation delay of an inverter could be, a corner simulation was done with minimum and maximum temperatures, and slow and fast process parameters (Figure 3.10).

The positive result is, that the propagation delay for both transitions stays almost the same, also over different temperatures or process parameters, as long as both transistors behave equally. Bad is that the delays have a very strong dependence on the temperature and process parameters. Care has to be taken on this topic, because the result of the bandwidth measurement also depends on this delay.

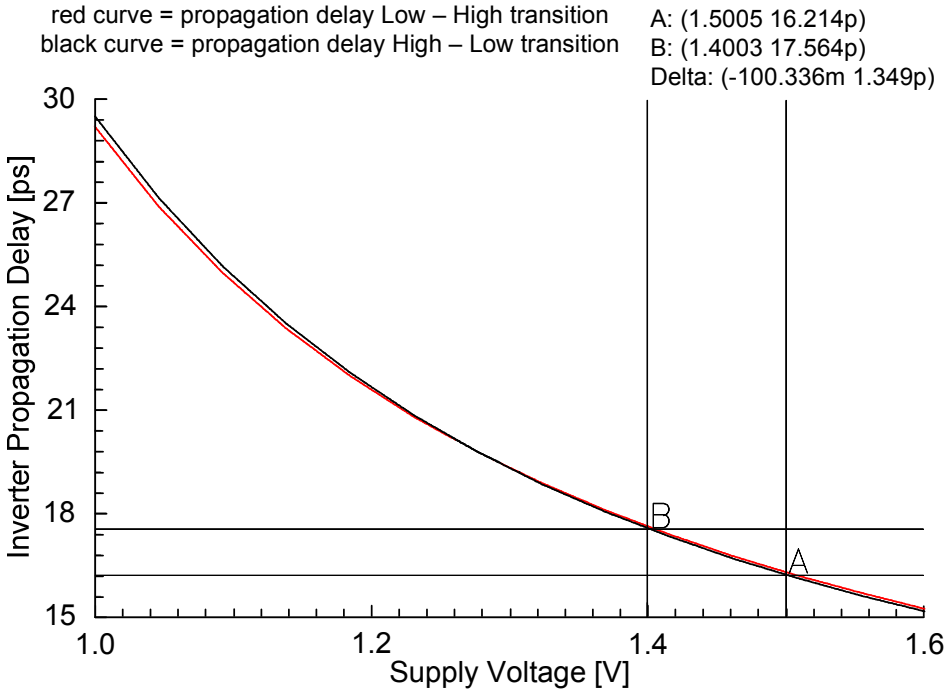


Figure 3.9: Supply Voltage Inverter Propagation Delay Dependence

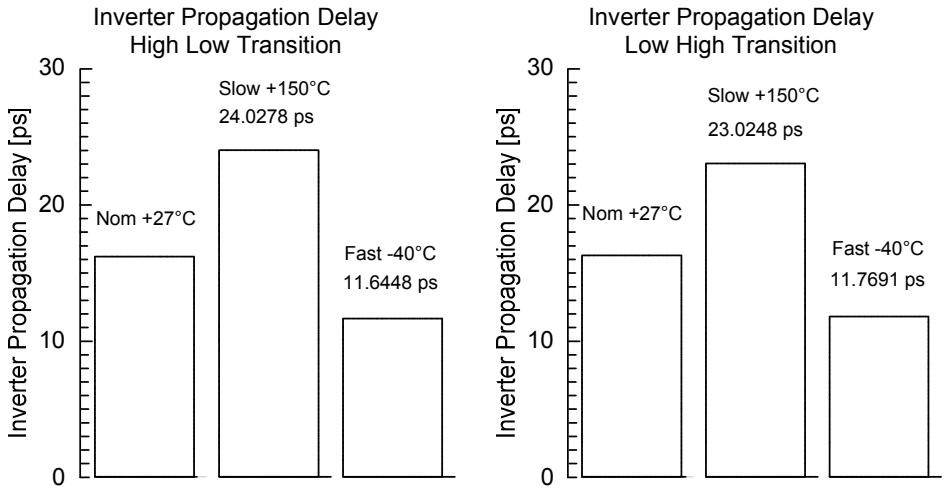


Figure 3.10: Inverter Propagation Delay Corner Simulation

Ring Oscillator current State Sampling Every rising edge of the CLK_{in} signal triggers M rising edge triggered flip flops [11] at the same time, and a snapshot of the current ring oscillator state is done. If this does not happen concurrent for every node code bubbles can occur later in the thermometer code. Metastability can occur, because the CLK_{in} signal is asynchronous to the signals from the oscillator nodes, and so the setup and hold times of the flip flops can be violated any time [28, 29]. If this happens the propagation delay of the flip flop is greatly increased, and how much is a random process. The probability for a metastable state is minimized by using flip flops with a small setup and hold time. Because in this application the time duration between sampling the ring oscillator state is high, a metastable state do not introduce a big problem. This duration is high enough to allow the digital TDC logic to finish its work, also when a metastable state had occurred.

Additionally the metastable state will always occur at the current ring oscillator transient position which we want to obtain. If the result is altered by the metastable state a big error is not introduced to the fine result. Master slave flip flops are used for the sampling, and to be sure that all devices sample at the same time, and the propagation delay is equal, only one type of flip flop was used. Also the signal paths from the ring oscillator to the flip flops, and the flip flop layout has to be done carefully.

Current Fine Position Decoding In the first half of the possible ring oscillator states (Figure 3.6) it looks like a falling edge propagates through the inverter chain, and in the second half a rising edge. To get the fine position in the ring, the correct edge has to be located. If a single node of the oscillator is viewed isolated from all the other nodes, you get two almost equal tables for all the other nodes (one is the inversion of the other), depending on the isolated node. If in one case (e.g. when the isolated node is high) all other nodes are inverted, we now get two equal tables. In principle we have only M different states with M inverters in the chain, one time with the isolated node at high, and one time at low. This reduces the needed logic, and also now only one type of edge propagates through the inverter chain for both oscillation periods. This allows the use of NAND gates for the edge detection and for a single bubble correction, which increases the reliability of the whole circuit. The interpolator circuit is shown in Figure 3.11. A likewise decoding method is illustrated in [12, 13].

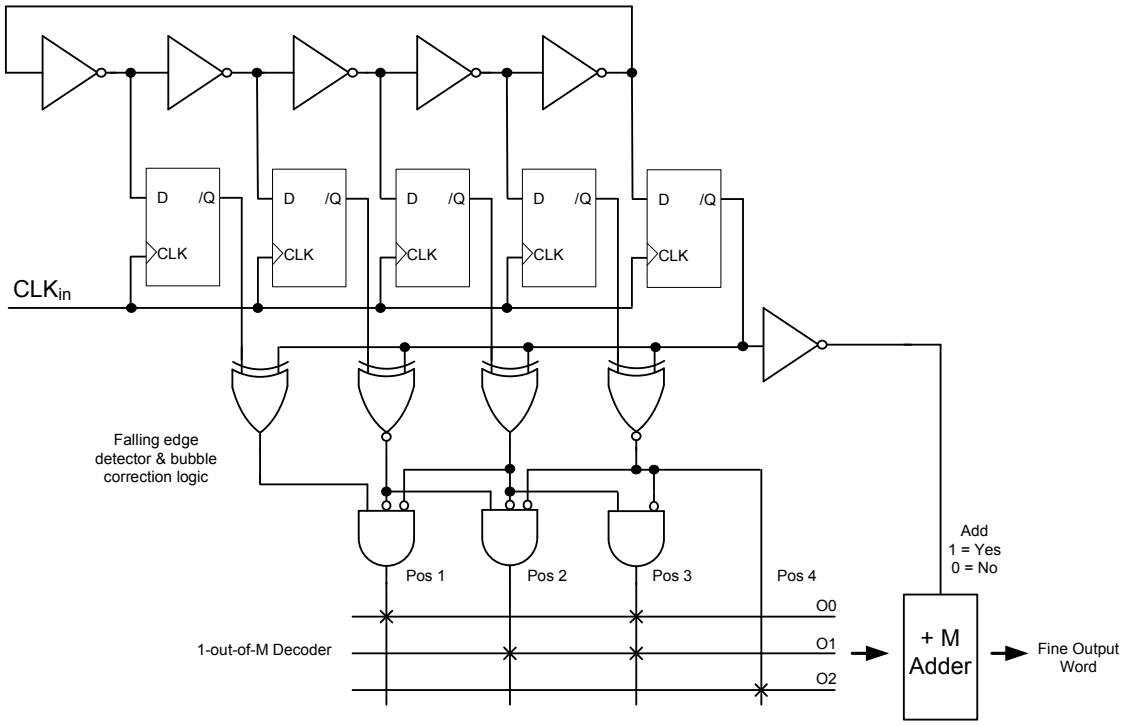


Figure 3.11: Interpolator Fine Decoder Logic

Every edge position in the interpolator has its own NAND gate, which checks if the left neighbour node is high, and that its input node, and the right neighbour are both low (bubble correction). Only in this case does the NAND gate output get high, and mark the current ring oscillator state. The activated output line is decoded by a $1 - out - of - M$ decoder, and a digital word for the current state is created. If the oscillator is in the second period, then an adder adds M to this word, otherwise the value is not altered. The XOR gates in front of the edge and bubble correction NAND gates do the inversion of all of the first $M - 1$ nodes for one of the two states of the isolated node. All the logic after the sample flip flops is later implemented in VHDL.

3.3.2 Coarse Counters

Because the measurement time interval exceeds the period time of the ring oscillator, an additional coarse counter is needed. At the first view a single counter which counts the number of full periods of the oscillator is enough. The counter value can always be increased by 1 if the output of the last inverter from the ring

oscillator changes its state in every second run through the ring oscillator. So when the interpolator state again equals the state at the beginning, after a full period of oscillation, we do not lose this information because of the increased coarse counter value. Every increase in the counter value equals $2 \cdot M$ inverters which were propagated.

After this single counter is triggered, it needs time to settle again. If the second edge of the CLK_{in} signal arrives in that moment, no current counter state would be ready to read out, and so a single counter is not enough. Again we do not know when the second edge will arrive. Two counters can be used as a solution, which are triggered with a 180 degree phase shift [12, 17, 30]. So one counter settles while the other one is ready for readouts. The phase shift is done with a buffer instead of an inverter in one of both signal paths to the counters. At the rising edge of the CLK_{in} signal both counter states are sampled by D-flip flops. To select which counter is ready for readout first the fine position in the ring oscillator is decoded, and from this position now the decision is made.

Figure 3.12 shows an example of a 7-stage ring oscillator with both course counters. The same concept is applicable to the 31-stage oscillator. After the reset both counters start with a state of zero, and with the first rising edge at the counter control node of the ring counter A is triggered at state 7. Until this state, the counter can be used for readout, but to be sure that a stable value is read again already one state before counter B is used as the data source. The same is true for the next edge for counter A in state 0. Here again one fine state before the trigger event the change of the data source is done. If in fine state 13 counter B is used instead of counter A one can see by comparision between the two counters that here counter B leads counter A by a value of 1. To correct this, one is substracted from the read value from the counter B. For all other fine states no correction has to be done, and a continuous and steady readout can be accomplished with this two counters.

Initialization of Two Coarse Counters The relationship between both coarse counter values must stay correct the whole time, otherwise an error at the TDC output up to $2 \cdot M$ inverters is possible, and so care has to be taken to reset both counters in a correct way. To be sure that after the release of the asynchronous reset signal both counters have the correct relationship a synchronizer consisting of two flip flops, and a additional flip flop for the second counter is used. The first

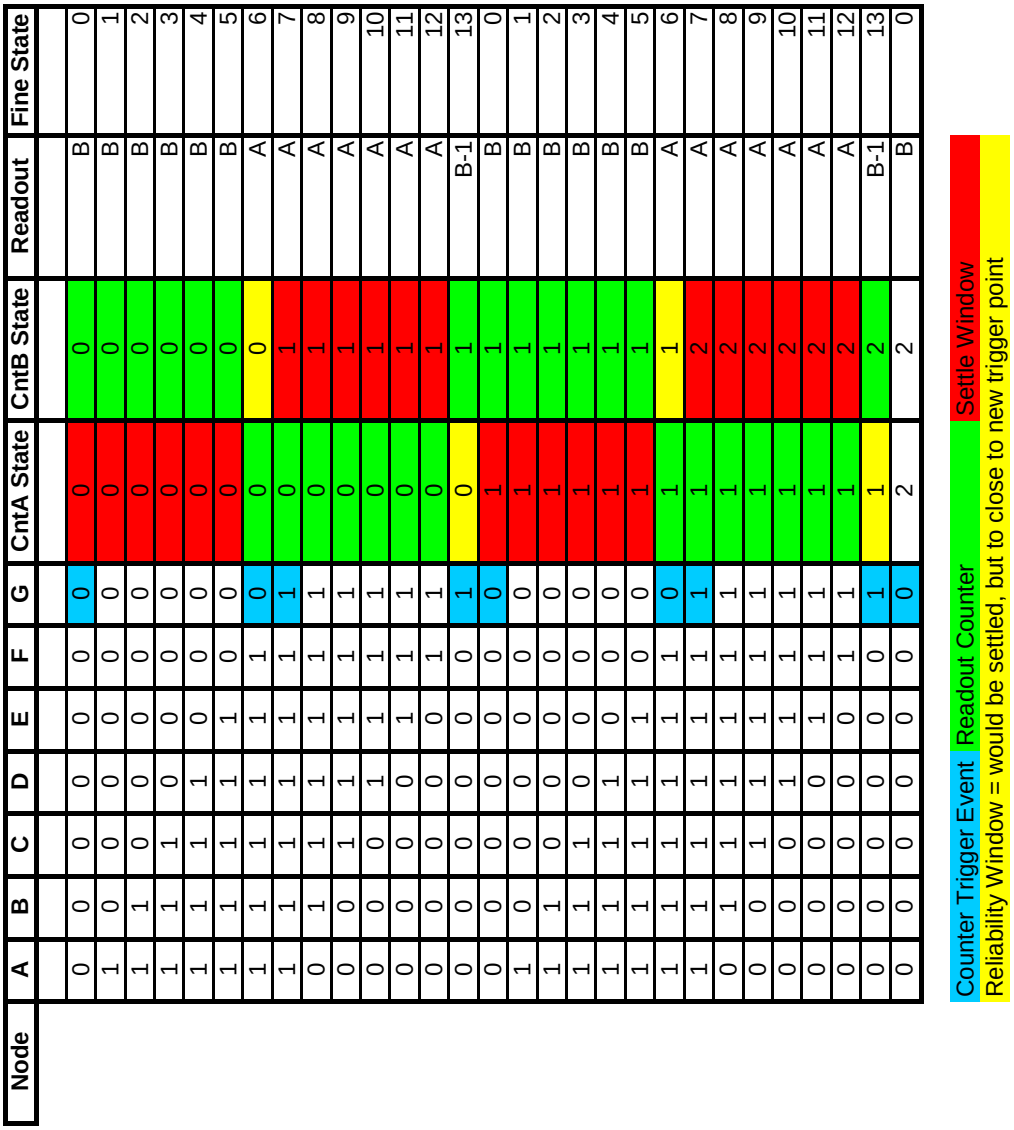


Figure 3.12: Fine State Table for two Coarse Counters

two flip flops release the reset signal from counter 1 (=counter B) in the moment when its trigger edge arrives, and so this reset signal is synchronous now to the ring oscillator. Because the propagation delay $tclkq$ of the flip flop is longer than the length of the rising edge after the release of the reset signal from the counter, the counter state is not increased in this first period. Because the third flip flop can only release the reset signal from the second counter (=counter A) after the first counter was released, it is always secured that counter 1 starts to count, and after that counter 2 follows. The second counter is also released with its active counting edge. The circuit for the counter reset can be seen in Figure 3.17, and a simulation from the initialization process is presented in Figure 3.13.

Coarse Counter Implementation After the trigger edge at the CLK input, the coarse counter must settle in a time which is defined by the typical propagation delay of an TDC core inverter, and the number of stages in the TDC oscillator, because one half oscillation period later the triggered counter is needed for readout. This time interval is shortened by the coarse counter sample flip flop setup time (t_{setup}) to prevent metastability. The settling time window is decreased further (by $b \cdot t_d$) if the active coarse counter for readout is changed b interpolator fine steps before the next coarse counter trigger impulse. So the maximum possible settling time is

$$ts_{max} = M \cdot t_d - b \cdot t_d - t_{setup} \tag{3.11}$$

The window ts_{max} was so small, that an asynchronous counter could not settle fast enough, and so a synchronous counter (Figure 3.14) had to be chosen.

The XOR and AND gates determine the next output value for the next rising clock edge. The settling time (=ts), which is determined by the clk-to-output propagation delay (=tp_{clkq}) of the counter state flip flops is found by:

$$ts = tp_{clkq} \tag{3.12}$$

Care has to be taken when designing the XOR and AND gates. It has to be assured that the setup times of the coarse counter state flip flops (=tc_{setup}) are always maintained under all possible circumstances [29]. The maximum time

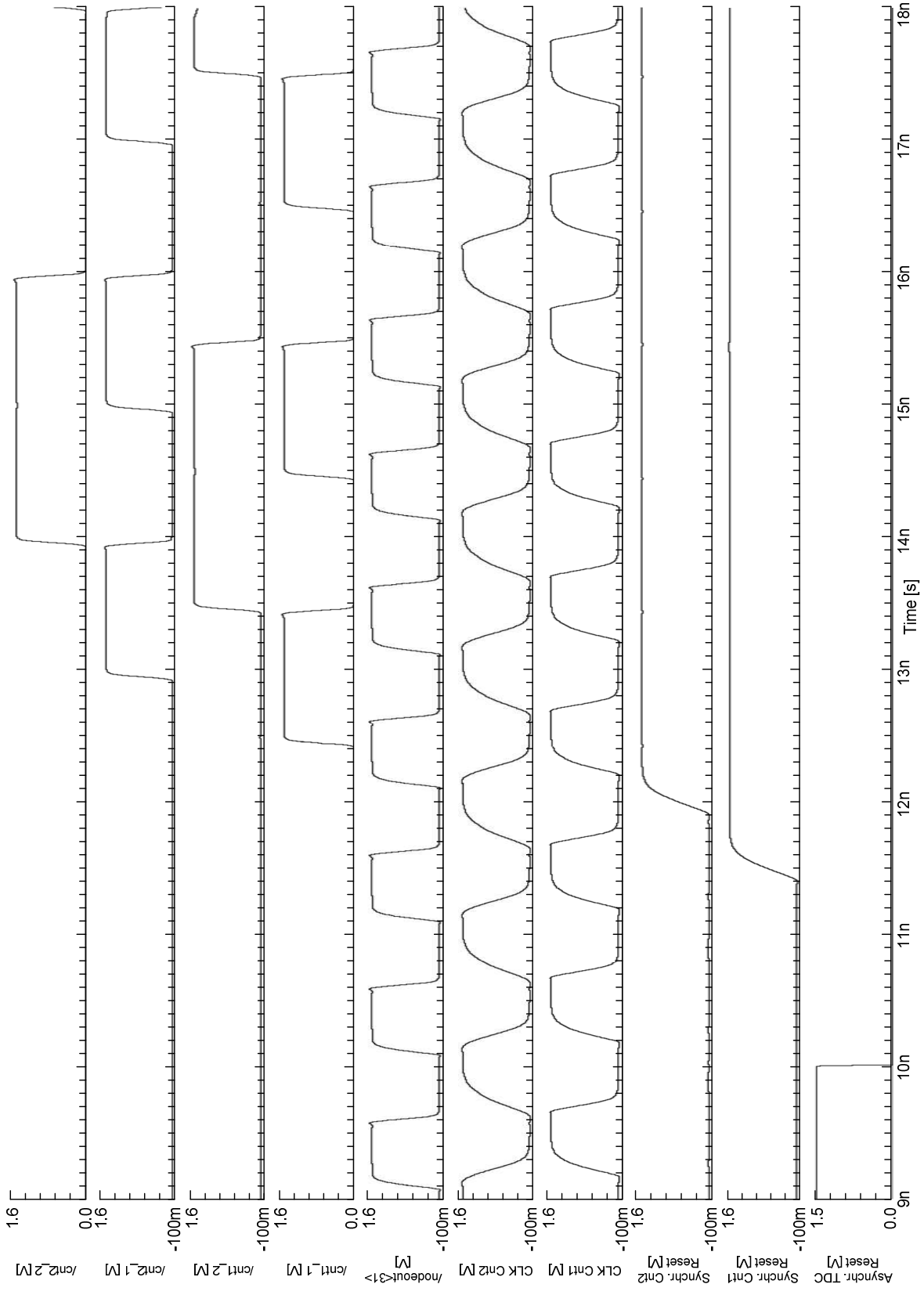


Figure 3.13: Coarse Counter Initialization Process Transient Simulation

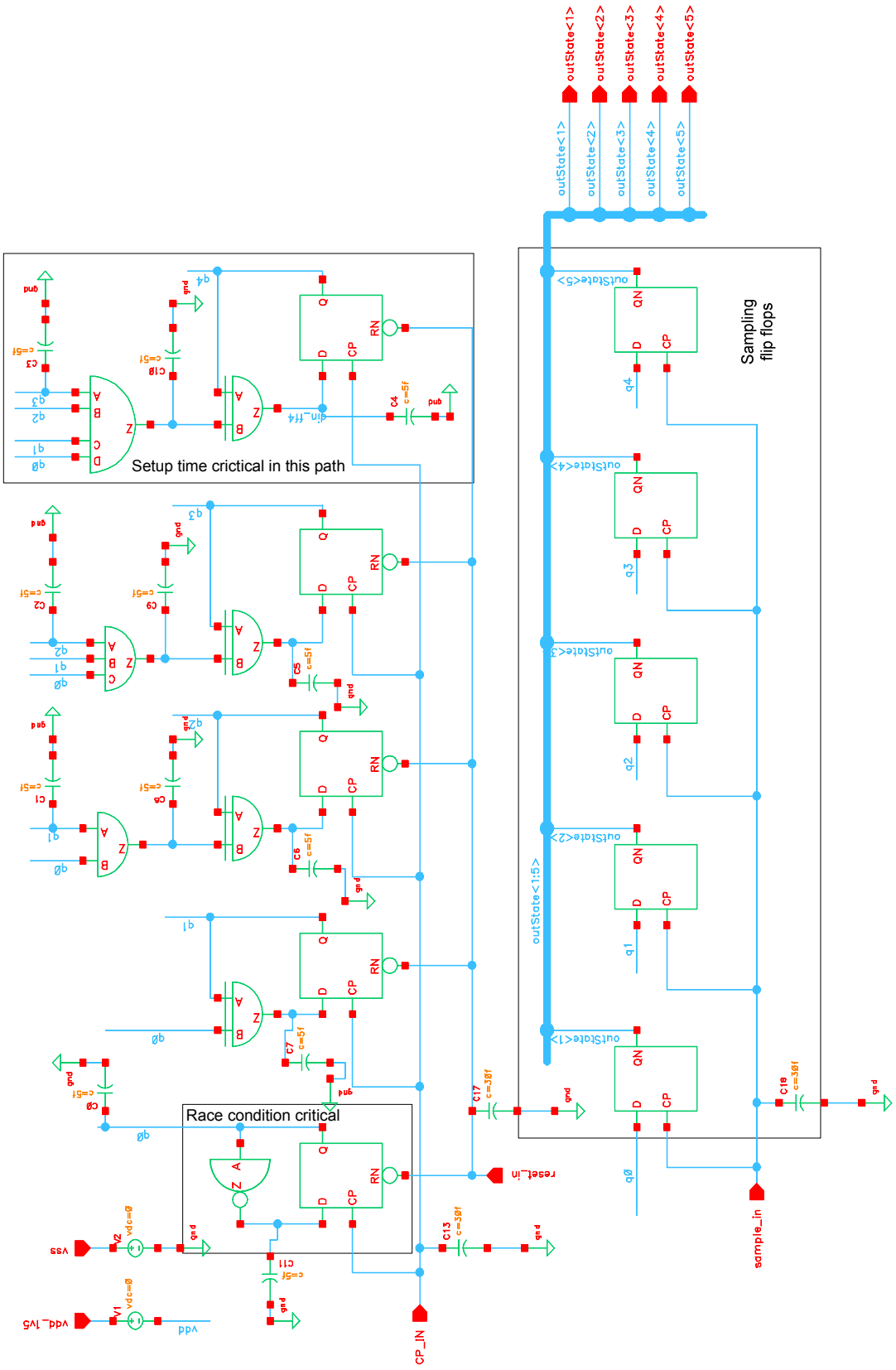


Figure 3.14: Coarse Counter Schematic

interval (=t_{max}) which is available for the signal to travel from the output of the counter to the D-input of the state flip flops is

$$t_{max} = 2 \cdot M \cdot t_d - tc_{setup} \tag{3.13}$$

The maximum propagation delay (=t) of all feedback signals is found in the most significant bit of the counter. This time consists of

$$t = tp_{clkq} + tp_{and} + tp_{xor} \tag{3.14}$$

In the least significant bit of the counter another problem can arise. Its feedback path is the shortest one of all, and the hold time of the flip flop has to be assured, because otherwise a race condition can occur. This happens if the feedback signal propagates faster than the hold time of the coarse counter state flip flop (=t_{hold}). So the following inequation has to be true to prevent a race condition [29]:

$$tp_{clktoD} > t_{hold} \tag{3.15}$$

The problematic path tp_{clktoD} only consists of the propagation delay of the XOR gate, and the clock-to-output propagation delay of the coarse counter flip flop. So the inequation is

$$tp_{xor} + tp_{clkq} > t_{hold} \tag{3.16}$$

A transient simulation was done to determine the saftey time margins for the coarse counter. The results are demonstrated in Figure 3.15.

3.3.3 Output Calculation

The current absolute phase state of the TDC consists of the coarse counter value multiplied by the number of stages in the ring oscillator, and the added current fine position in the interpolator. If the new coarse counter state is bigger than the

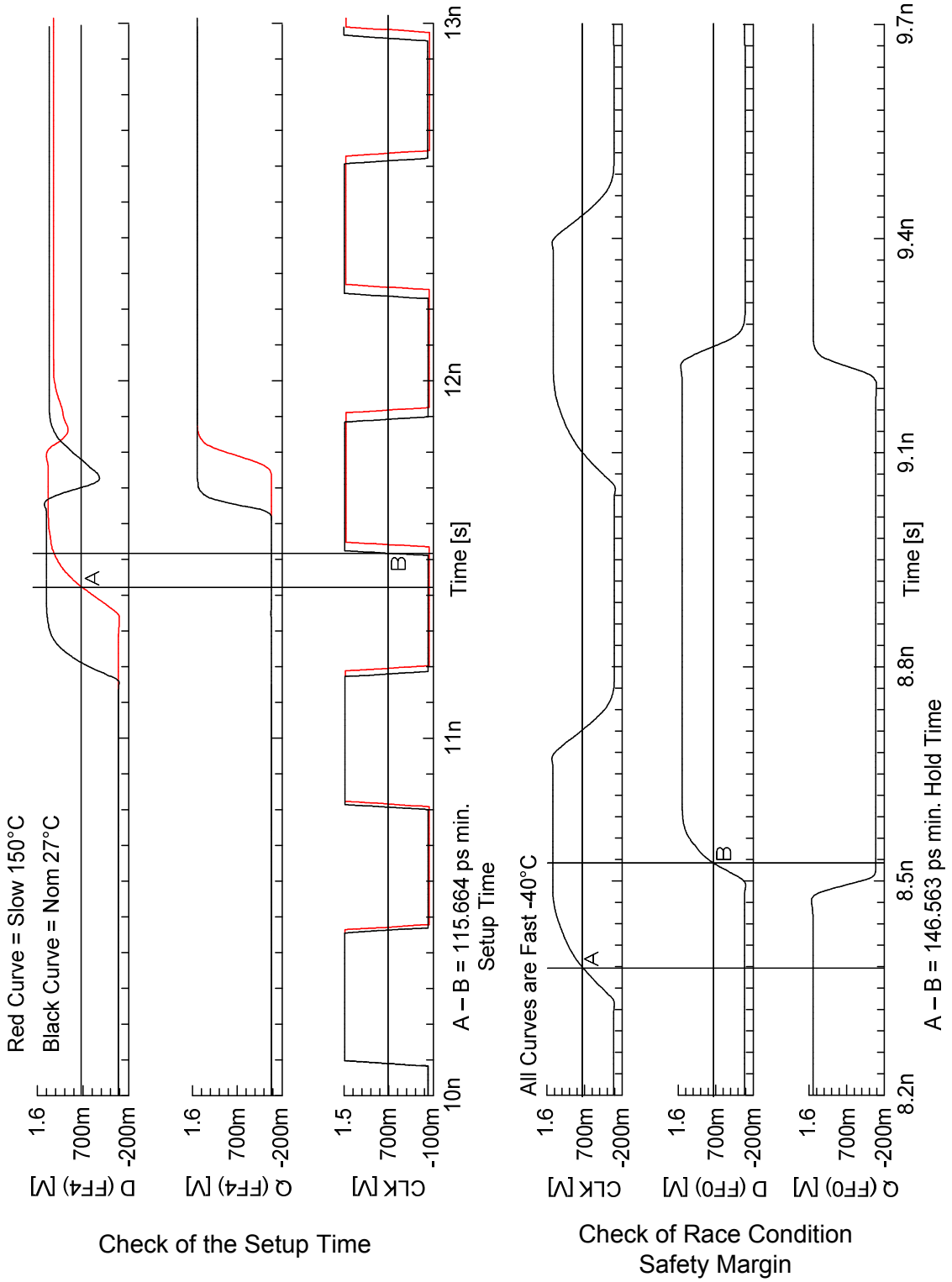


Figure 3.15: Coarse Counter Saftey Margin Transient Simulation (Race Condition and Setup Time

last one the period time between two CLK_{in} signal edges is simply the difference between the current and the last absolute phase state (case 1). If in the second case the new coarse counter state is smaller than the old one (coarse counter has overflown), then the period time equals the number of inverters which have changed their state before the overflow, and after it. So in this case the period time digital word equals $TI_q = state_{n+1} + 2 \cdot M \cdot 2^i - state_n$ where i is the number of bits of the coarse counters, and M is the number of stages in the ring oscillator.

Period time case 1:

$$TI_q = absstate_{n+1} - absstate_n \tag{3.17}$$

Period time case 2:

$$TI_q = absstate_{n+1} + 2 \cdot M \cdot 2^i - absstate_n \tag{3.18}$$

The data flow in the calculation block is presented in Figure 3.16.

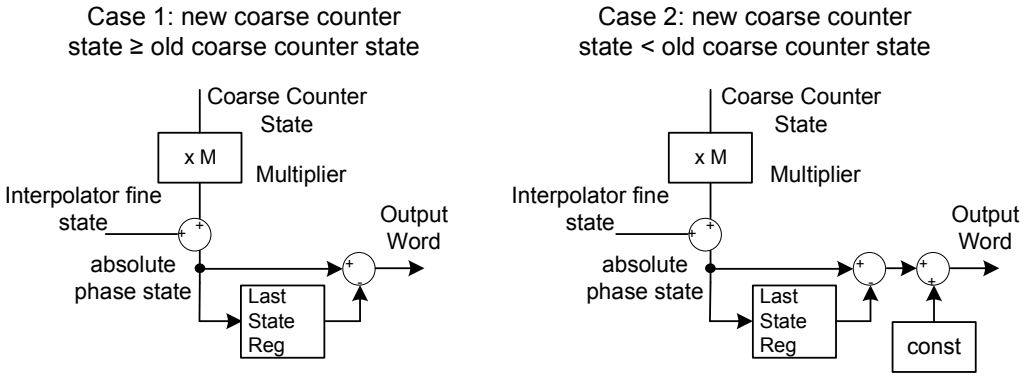


Figure 3.16: TDC Output Word Calculation

Top Schematic The top schematic of the TDC block in Cadence is demonstrated in Figure 3.17.

Possible Ring Oscillator TDC Simplifications for other Applications If the TDC does not need to quantize every period of the measurement input signal, and

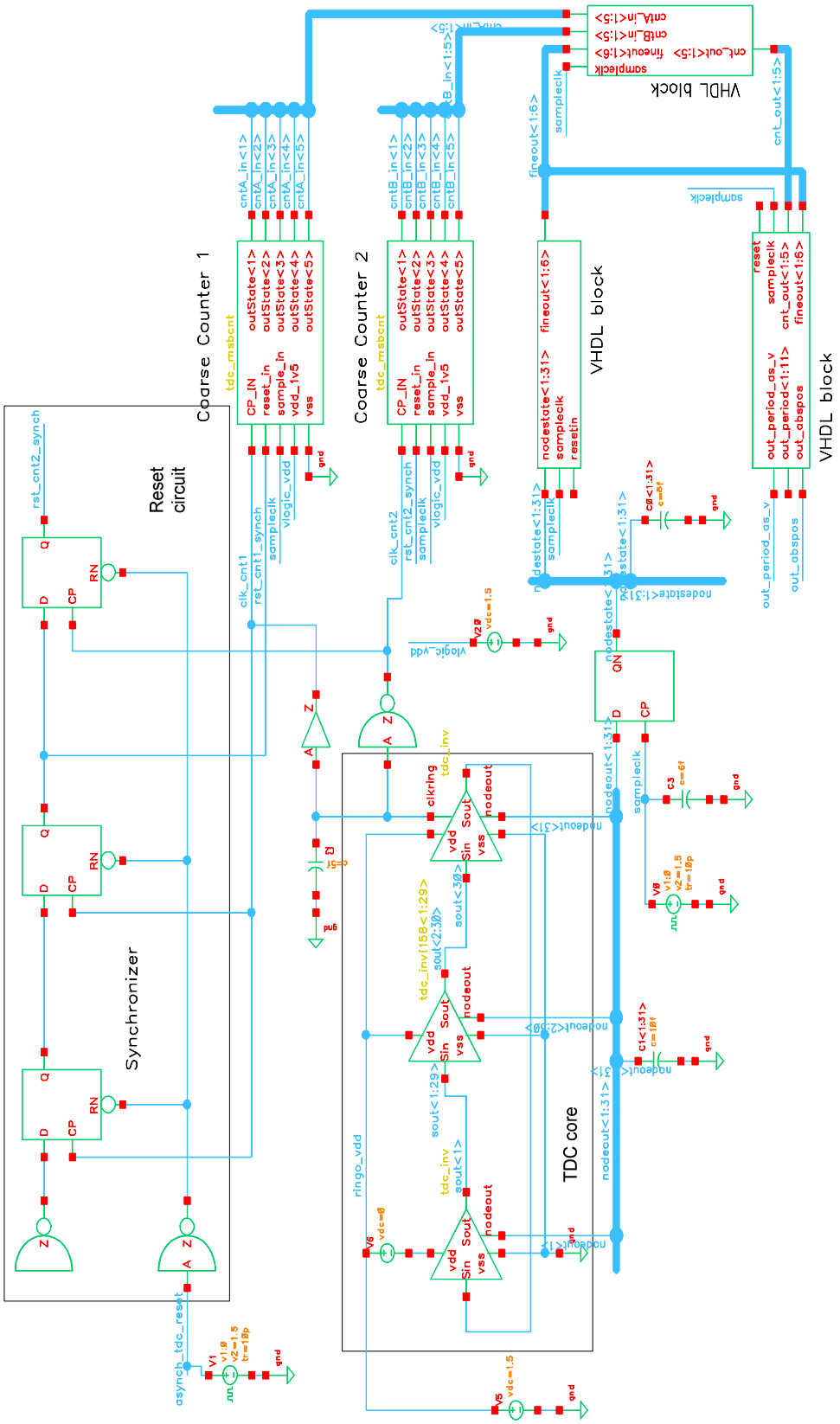


Figure 3.17: Time to Digital Conversion Unit Top Schematic

there is a long enough idle time between the conversions, then the ring oscillator can be stopped in between. So some power can be saved, and possibilitly a single ripple counter can be now used as the coarse counter, if the settle time window is wide enough. Examples are [16, 18].

If the number of delay elements in the interpolator is even, and a number which is a power of two, then the MSB bits from the coarse counter can be simply added from the left to the bits from the fine interpolator decoder circuit, to create the absolute phase state of the TDC. This is not possible with a uneven number of stages, or a number of stages which is not a power of two, because then by simply add the MSB bits to the left of the fine part bits, an error is made with every coarse counter count.

To get an even number of delay elements differential oscillators are often used. With a special asymetric ring oscillator design [11, 13] this can also be done. But it should be noted that such a design for an asymetric oscillator is also possibly associated with some risks. See document [31] for example.

If the maximum measurement time interval is smaller than the ring oscillator period time ($2 \cdot M \cdot t_d$), then firstly no coarse counters are needed, and secondly the decoding of the fine part can be simply done with XOR gates [19]. These gates compare the node outputs from the last rising edge of the measurement input signal with the current output node states of the ring oscillator. The number of XOR gates with an high output signal shows how much inverters have changed their state in the last period.

3.4 Simulation

A transient simulation example of the whole time-to-digital converter unit is presented in Figure 3.18.

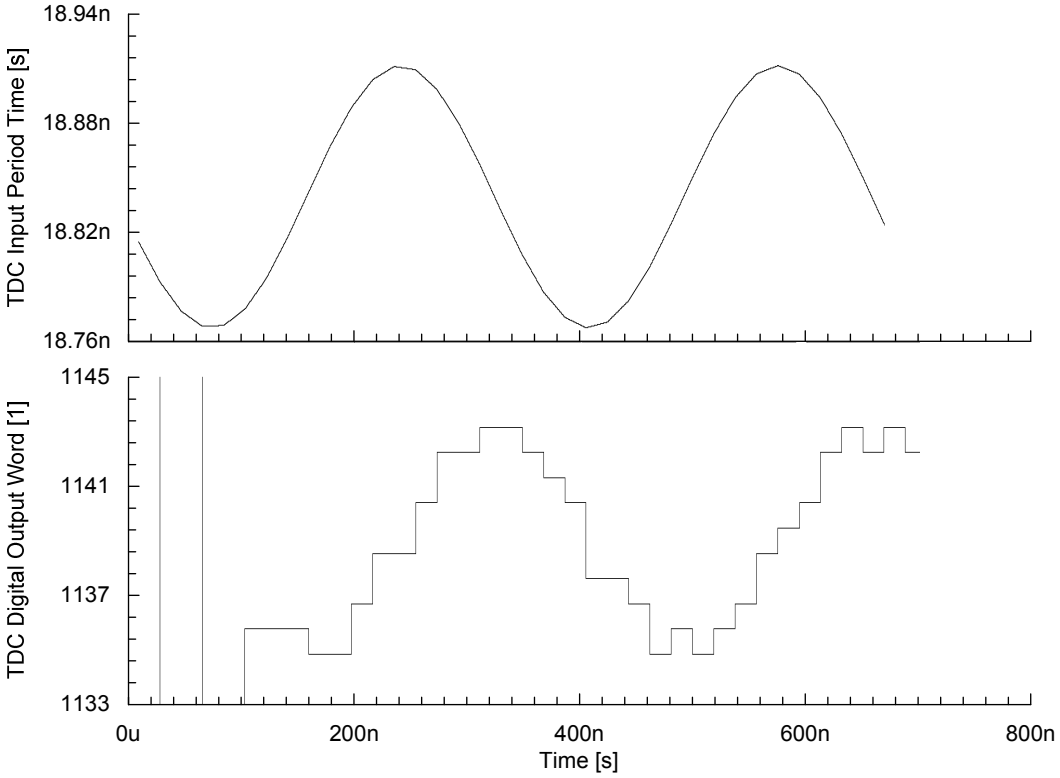


Figure 3.18: TDC Transient Simulation: Input Signal with Sinusoidal Frequency Progression

4 Bandwidth Calibration of a Phase Locked Loop (PLL)

4.1 Principle

A way to practically measure the closed-loop bandwidth of a phase locked loop is described in [4], and it is based on the measurement of the transfer function of the loop. The $-3dB$ bandwidth is found if the gain of the transfer function is decreased by -3 dB. The author describes two basic approaches to find the transfer function:

- Phase-Modulation (PM) [32]: A phase modulated signal is applied to the reference input of the loop. If the amount of phase-modulation is small enough for the phase detector, then this method has the advantage that the phase error can never grow to high, and the loop is always linear. To find the gain of the transfer function at the used $test$ frequency the output of the loop is observed. A drawback of this method is its higher complexity.
- Frequency-Modulation (FM): A possible test setup is shown in Figure 4.1 [4]. A frequency modulated frequency generator at the reference input of the loop generates the following signal:

$$\omega_{ref} = \omega_0 + \Delta\omega \cdot sin(\omega_m \cdot t) \tag{4.1}$$

The center frequency of the reference signal is denoted ω_0, $\Delta\omega$ is the frequency deviation, and ω_m is the modulation frequency. The voltage signal at the loop filter is also sinusoidal (see explanation below), and the amplitude of this signal is proportional to the absolute value of the closed-loop transfer function at ω_m. If ω_m is changed over all frequencies, the gain of the bode

plot can be obtained. For the following considerations the feedback divider value is set to one, and therefore no frequency multiplication is done.

Loop filter voltage vs. time [4]: The reference input phase signal is:

$$\varphi_{ref}(t) = -\frac{\Delta\omega}{\omega_m} \cdot cos(\omega_m \cdot t) \tag{4.2}$$

Therefore its amplitude is:

$$|\varphi_{ref}|(j \cdot \omega_m) = \frac{\Delta\omega}{\omega_m} \tag{4.3}$$

This amplitude scaled with the closed loop transfer function of the PLL gives us the amplitude of the output signal.

$$|\varphi_{out}|(j \cdot \omega_m) = T(j \cdot \omega_m) \cdot |\varphi_{ref}|(j \cdot \omega_m) \tag{4.4}$$

$$\frac{|\varphi_{out}|(j \cdot \omega_m)}{V_{cntrl}(j \cdot \omega_m)} = \frac{Kvco}{j \cdot \omega_m} \tag{4.5}$$

From this equations the absolute value of the transfer function can be derived:

$$|T(j \cdot \omega_m)| = \frac{V_{cntrl}(j \cdot \omega_m) \cdot Kvco}{\Delta\omega} \tag{4.6}$$

Care has to be taken when using the frequency-modulation method, because the phase error at the phase detector is not limited [4]. Under all circumstances the phase error has to stay below the values which are allowed by the used phase detector. So the frequency deviation $\Delta\omega$ must stay below a certain value, because the phase error is proportional to it.

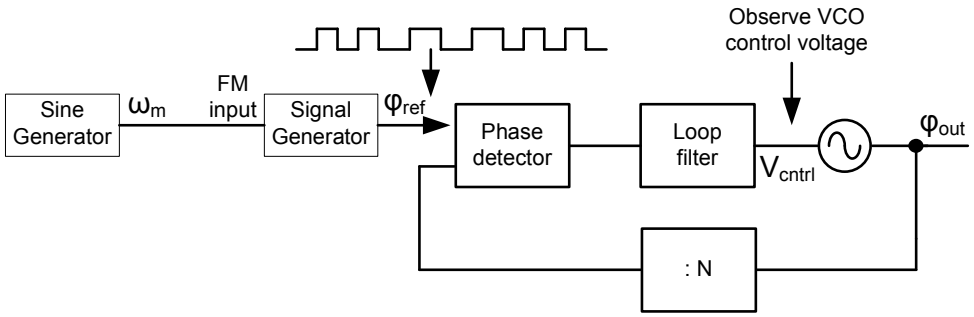


Figure 4.1: Frequency Modulation (FM) based PLL Transfer Function Measurement Setup [4]

4.1.1 TDC as Observer

The output frequency of the VCO is used as a measure for the current loop filter output voltage [33]. Additionally the digital output word of the TDC circuit, which represents the current period time of the PLL output signal is used as a metric for the PLL output frequency (see 4.1.1). The modified measurement setup is presented in Figure 4.2.

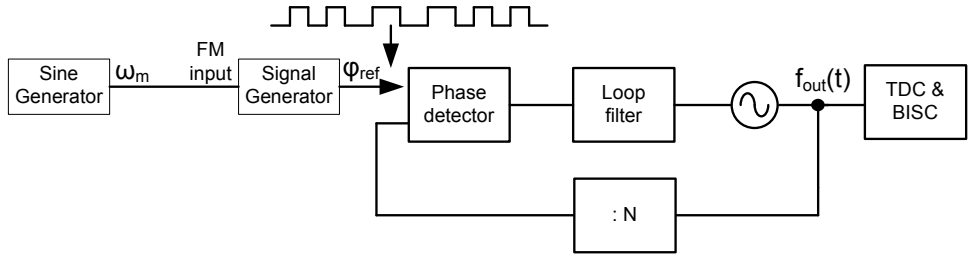


Figure 4.2: TDC Period Time Measurement based Loop Filter Voltage Observation

Period Time vs. Frequency

The current TDC output word is proportional to the period time, but it should be used as a metric for the output frequency. The relationship between these two quantities is derived in this section.

While measuring the loop bandwidth the output frequency is modulated:

$$f_(t) = f_{out}(t) = f_0 + \Delta f(t) \tag{4.7}$$

The PLL output signal period time can be found as:

$$T(\Delta f) = \frac{1}{f_0 + \Delta f} \tag{4.8}$$

with f_0...center output frequency of the PLL, and Δf... output frequency deviation

Now a taylor series can be found for this expression:

$$Pf(x) = f(a) + \frac{f^{'}(a)}{1!} \cdot (x-a) + \frac{f^{''}(a)}{2!} \cdot (x-a)^2 + ... + \frac{f^n(a)}{n!} \cdot (x-a)^n + R \tag{4.9}$$

In this case a is set to zero, and two elements are calculated for the series.

$$\frac{dT(\Delta f)}{d\Delta f} = -(f_0 + \Delta f)^{-2} \cdot 1 = -\frac{1}{(f_0 + \Delta f)^2} \tag{4.10}$$

$$\frac{dT^2(\Delta f)}{d^2\Delta f} = 2 \cdot (f_0 + \Delta f)^{-3} \cdot 1 = \frac{2}{(f_0 + \Delta f)^3} \tag{4.11}$$

$$T(\Delta f) = T(\Delta f)|_{\Delta f=0} + \left.\frac{dT(\Delta f)}{d\Delta f}\right|_{\Delta f=0} \cdot \Delta f + \left.\frac{dT(\Delta f)^2}{d^2\Delta f}\right|_{\Delta f=0} \cdot \Delta f^2 + ... + R \tag{4.12}$$

$$T(\Delta f) = \frac{1}{f_0} - \frac{1}{f_0^2} \cdot \Delta f + \frac{1}{f_0^3} \cdot \Delta f^2 + R \tag{4.13}$$

$$T(\Delta f) = T_0 + \Delta T + R \tag{4.14}$$

with ΔT:

$$\Delta T(\Delta f) = -\frac{1}{f_0^2} \cdot \Delta f + \frac{1}{f_0^3} \cdot \Delta f^2 \tag{4.15}$$

If $\frac{\Delta f}{f_0} \ll 1$ then the quadratic term of Δf can be ignored. The output signal period

time deviation is proportional to the output signal frequency time deviation.

$$\Delta T(t) = -\frac{1}{f_0^2} \cdot \Delta f(t) \tag{4.16}$$

The period time deviation which is measured depends very heavily on the center output frequency f_0. If we want to make the measurement sensitive, a low value of f_0 is needed. A drawback of a low f_0 is that the time-to-digital converter has to be able to measure a longer time interval. This increases the number of needed bits in the MSB bit counter. This counter is driven with a high frequency, and so this increases the power dissipation heavily. To increase $\Delta T(\Delta f)$ to get more sensibility, Δf can also be increased, but then the errors also increase, due to the greater influence of the quadratic term in the above equations. A comparision of $\Delta T(\Delta f)$ with and without the quadratic term is shown in Figure 4.3.

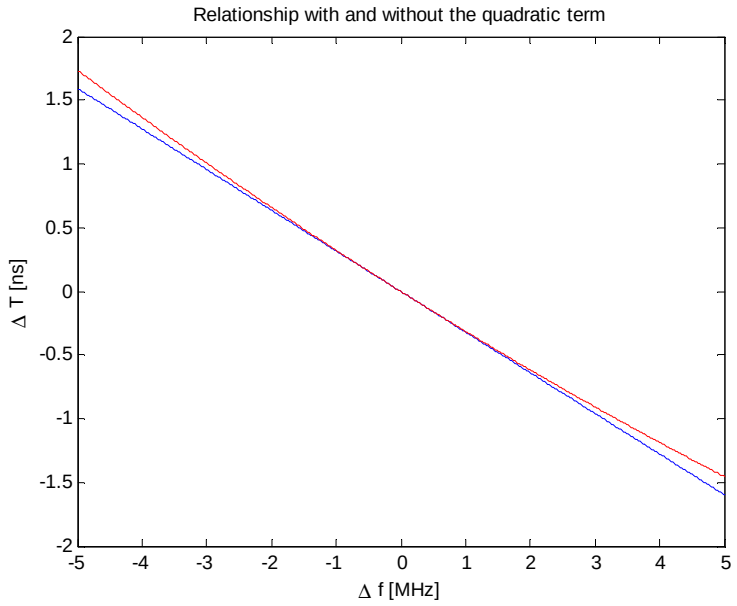


Figure 4.3: Quadratic Term Effect on $\Delta T vs. \Delta f$

4.1.2 Stimulus Generation

Instead of a frequency modulated frequency generator in the original measurement setup [4] to generate the input signal to the phase detector, now the feedback divider setting of the loop is periodically changed [1]. The change of the

divider setting for modulating the loop is so small in comparision of the absolute value, that the transfer function of the loop only changes very slightly, and therefore the loop behaviour before and after the change can be seen as equal. If this would not be the case the problem gets nonlinear. The phase detector does not care if the signal is fed in at the reference input or the feedback path, if we ignore the negative sign in the transfer function at the feedback input [34]. The size of the frequency step must be constricted. See also 4.1.2. Figure 4.4 shows the new setup.

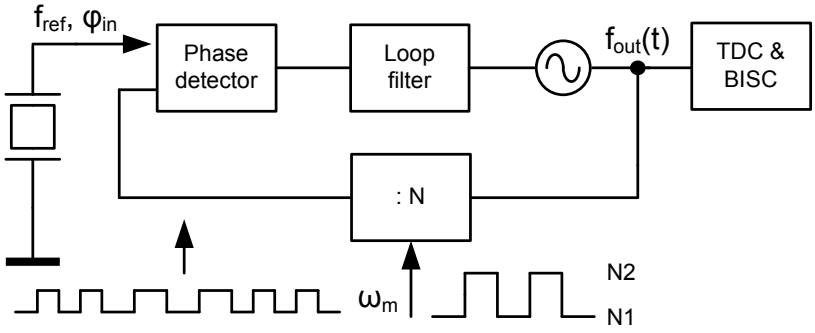


Figure 4.4: Digital Divider Modulation for Stimulus Generation

Maximum Divider Step

The phase error is not bounded while the frequency modulation takes place and must stay below a certain limit. The maximum allowed divider ratio change step dependends on many different parameters:

- The loop filter type and specification: the smaller the bandwidth of the loop filter is, the smaller the allowed divider ratio change is, because the loop can only correct phase errors very slowly
- The type of used phase detector: depending on the type of phase detector used, the linear operating region has a different size. A phase-frequency-detector allows a phase error of $2 \cdot \pi$.
- How the divider ratio is changed over time: if the ratio changes from the starting value N_{old} to the end value N_{new} suddenly (step) the maximum phase error can be seen (worst case scenario). But it is also possible to change from ratio N_{old} to N_{new} with some intermediate steps. In this case

the phase locked loop has time between the steps to correct the phase error, and so it does not grow as high as in the worst case scenario.

The maximum allowed divider ratio change is derived using the worst case scenario, which means a suddenly frequency step. For the calculation the phase model is used (Figure 4.5).

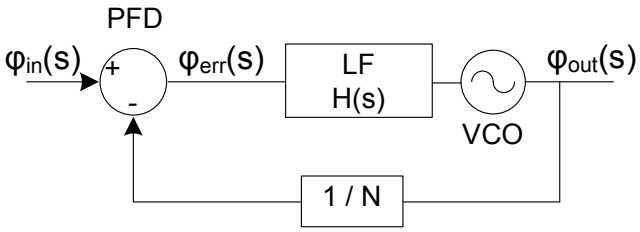


Figure 4.5: Phase Error Approximation Model

The phase error is shown as φ_{err} in the diagram. First the open loop transfer function of the phase locked loop can be found:

$$G(s) = \frac{Kpd \cdot H(s) \cdot Kvco}{s} \tag{4.17}$$

with $H(s)$...transfer function of the loop filter

This then yields the following closed loop transfer function:

$$T(s) = \frac{G(s)}{1 + \frac{1}{N} \cdot G(s)} = \frac{G(s) \cdot N}{N + G(s)} \tag{4.18}$$

$$T(s) = \frac{Kpd \cdot H(s) \cdot Kvco \cdot N \cdot \frac{1}{s}}{N + \frac{Kpd \cdot H(s) \cdot Kvco}{s}} = \frac{\varphi_{out}(s)}{\varphi_{in}(s)} \tag{4.19}$$

This transfer function now tells us how the output of the PLL develops, if there is a signal at the input of the loop. If we want to know how the phase error develops over time when a stimulus at the reference input happens, then we can use the same method, but this time with the error transfer function.

$$H_{error}(s) = \frac{\varphi_{err}(s)}{\varphi_{in}(s)} \tag{4.20}$$

The feedback input signal of the phase detector is now called $\varphi_x(s)$

$$\varphi_x(s) = \frac{1}{N} \cdot \phi_{varout}(s) \tag{4.21}$$

$$H_{error}(s) = \frac{\varphi_{in}(s) - \varphi_x(s)}{\varphi_{in}(s)} = 1 - \frac{1}{N} \cdot T(s) \tag{4.22}$$

We have to assume that the change of the divider ratio ΔN is very small in comparision of the absolute value of N, and so the transfer function of the loop only changes very slightly. So the PLL loop behaviour before and after the change can be seen as equal. If this assumption had not been applicable, the whole problem would have been nonlinear.

So $\Delta N \ll N$

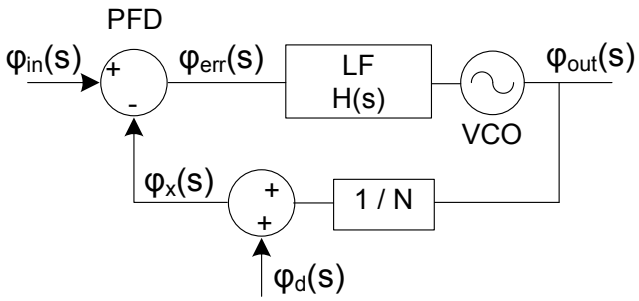


Figure 4.6: Divider Modulation Model

A divider ratio setting change introduces a frequency error to the negative feedback signal input of the phase detector, and because of the low pass behaviour of the loop filter the VCO output frequency cannot change at the same moment. This produces a growing phase error, and this error is named $\varphi_d(s)$ in Figure 4.6, which is then used as a stimulus signal. After some time the VCO output frequency can follow the new situation, and the phase error is decreased again.

The phase frequency detector handles both its inputs in the same way (apart from the sign), and so there is no difference if the stimulus is created at the reference input, or using the feedback input. Only the sign in the transfer function is changed [9, 34]. We can model the divider ratio change as a frequency jump

of the reference frequency at the reference input of the phase detector. And for this case we have already found the error transfer function $H_{error}(s)$.

$$\frac{\varphi_{out}(s)}{\varphi_d(s)} = -\frac{\varphi_{out}(s)}{\varphi_{in}(s)} \tag{4.23}$$

$$\varphi_{in}(s) = -\varphi_d(s) \tag{4.24}$$

The laplace transformation of the frequency step is $\frac{\Delta\omega_{step}}{s}$. Phase is defined as integrated frequency, thus for the input signal we get $\varphi_{in}(s)$ [35]:

$$\varphi_{in}(s) = \frac{\Delta\omega_{step}}{s^2} = -\varphi_d(s) \tag{4.25}$$

Now we know the input signal $\varphi_{in}(s)$, the error transfer function $H_{error(s)}$, and so the phase error $\varphi_{err}(s)$ is:

$$\varphi_{err}(s) = H_{error}(s) \cdot \frac{\Delta\omega_{step}}{s^2} \tag{4.26}$$

Initial frequency error $\Delta\omega_{step}$:

All the frequencies before and after the divider change are presented in Figure 4.7.

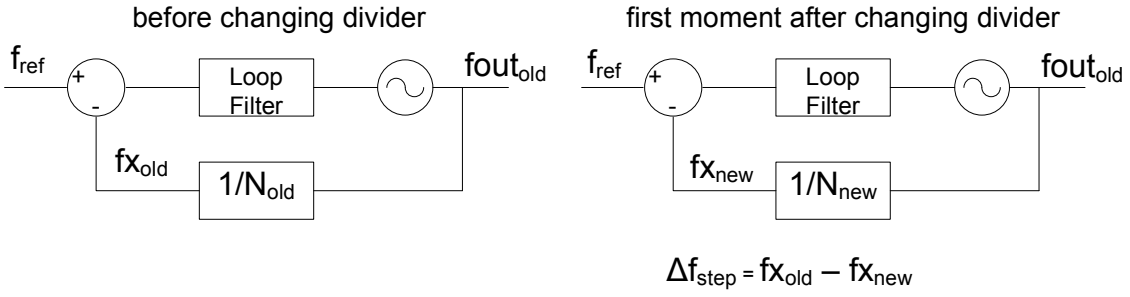


Figure 4.7: Initial Frequency Error Step Approximation

Before the switching process, the phase locked loop is settled and so the output frequency of the voltage controlled oscillator is given by:

$$fout_{old} = N_{old} \cdot f_{ref} \tag{4.27}$$

$$fx_{old} = \frac{fout_{old}}{N_{old}} = \frac{f_{ref} \cdot N_{old}}{N_{old}} = f_{ref} \tag{4.28}$$

Now the divider is changed to $N_{new} = N_{old} + \Delta N$

The output frequency of the VCO can not change quickly because of the loop filter. In the first moment it stays the same ($fout_{old}$).

$$fx_{new} = \frac{fout_{old}}{N_{new}} = f_{ref} \cdot \frac{N_{old}}{N_{new}} \tag{4.29}$$

$$\Delta f_{step} = fx_{old} - fx_{new} = fx_{old} - \frac{f_{ref} \cdot N_{old}}{N_{new}} = f_{ref} - \frac{f_{ref} \cdot N_{old}}{N_{old} + \Delta N} \tag{4.30}$$

$$\Delta f_{step} = f_{ref} \cdot (1 - \frac{N_{old}}{N_{old} + \Delta N}) = f_{ref} \cdot \frac{N_{old} + \Delta N - N_{old}}{N_{old} + \Delta N} \tag{4.31}$$

$$\Delta f_{step} = f_{ref} \cdot \frac{\Delta N}{N_{old} + \Delta N} \tag{4.32}$$

Already made assumption: $\Delta N \ll N_{old}$

$$\Delta f_{step} \sim f_{ref} \cdot \frac{\Delta N}{N_{old}} \tag{4.33}$$

Now we know the value of the frequency step at the input:

$$\Delta \omega_{step} = \Delta f_{step} \cdot 2 \cdot \pi [rad/s] \tag{4.34}$$

If this information is inserted in a single equation the laplace transform of the

phase error signal can be found.

$$\varphi_{err}(s) = [1 - \frac{Kpd \cdot H(s) \cdot Kvco \cdot \frac{1}{s}}{N + \frac{Kpd \cdot H(s) \cdot Kvco}{s}}] \cdot \frac{\Delta f_{step} \cdot 2 \cdot \pi}{s^2} \tag{4.35}$$

with $H(s)$...transfer function of the loop filter

To get the phase error over time, the inverse laplace operation must be used on $\phi_{err}(s)$. Because this would be complicated in a analytical way (the order of the denominator is four) a closed solution is not presented here. Instead Matlab was used to analyse the phase error over time.

A result is shown in 4.8. For this plot the following parameters where used: $N = 42$, $\Delta N = 0.3$, $fref = 22\ MHz$. The maximum phase error is $1.1535\ rad$, which is far below the limit $2 \cdot \pi$ of a phase frequency detector. This parameter set guarantees that the loop remains in the linear region. The same result for the phase error is found with the phase model in Matlab, where the divider is periodically changed. The result in Figure 4.8 and the result from the Matlab simulation (Figure 4.9) do not differ very much.

A simulation was done in Spectre using the presented PLL voltage model and two different settings for the ΔN parameter. The divider switching frequency is $300\ kHz$, $fref = 22\ Mhz$, $N = 43.5$, the divider change waveform is rectangular (worst case).

- Setting 1: $\Delta N = 1$, the maximum calculated phase error is $5.23\ rad$, which is below $2 \cdot \pi$ rad. So the loop remains linear, and no additional cycle slipping can be seen in the loop filter output voltage Figure in 4.10, after the loop has settled from the startup condition. The modulation was started a little bit to soon, and the first cycles of the waveform are overlapping with the settling process.
- Setting 2: $\Delta N = 2$, The maximum phase error is $10.45\ rad$, which is too much. Additional cycle slipping [1] occurs, and the behaviour of the loop is not linear anymore, which can be seen in Figure 4.11. The top graph shows the control voltage of the VCO, and the bottom graph is the divider setting.

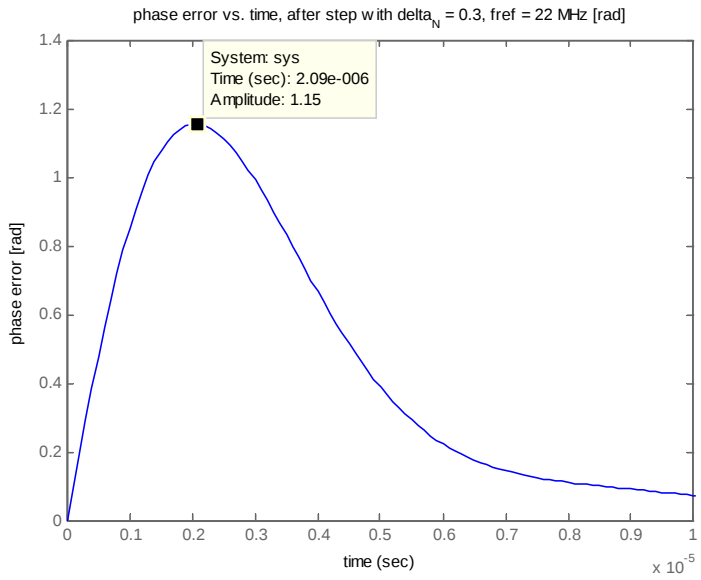


Figure 4.8: Matlab Phase Error Result

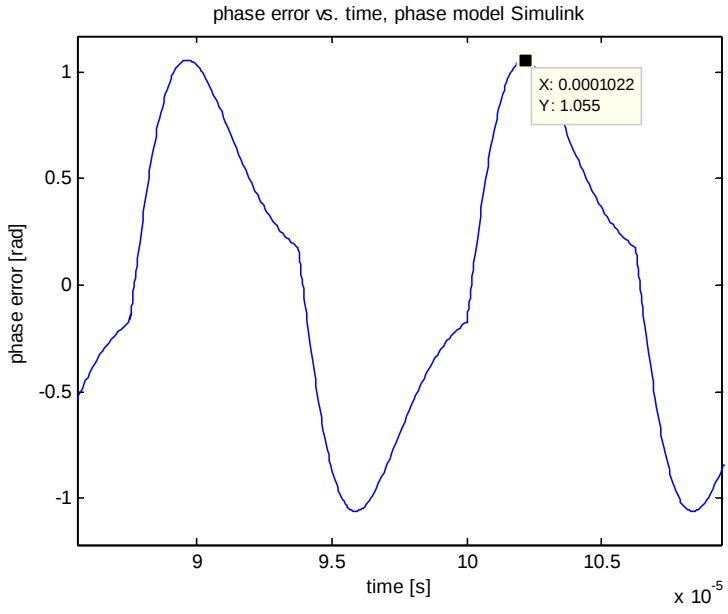


Figure 4.9: Matlab Model Phase Error Result

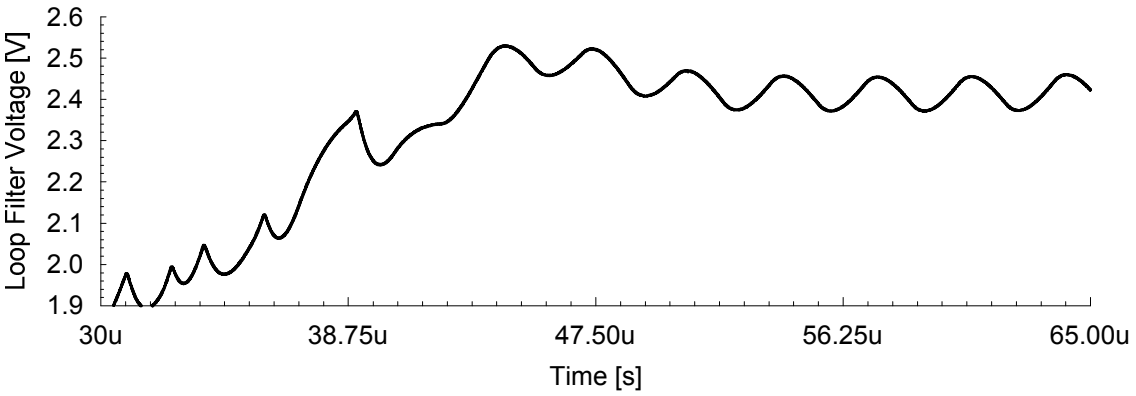


Figure 4.10: Modulated Voltage Model Loop Filter Output Voltage Time Behaviour Simulation (Phase Error bordered)

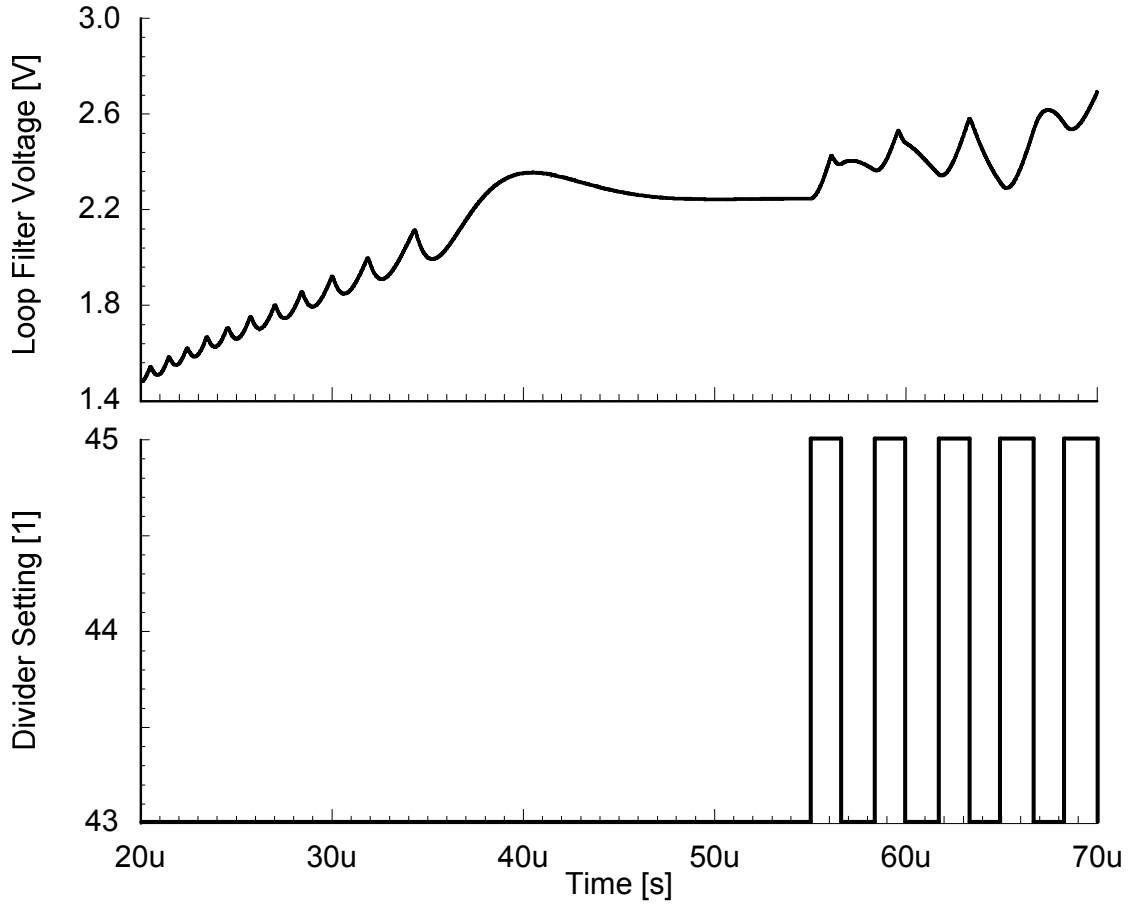


Figure 4.11: Modulated Voltage Model Loop Filter Output Voltage Time Behaviour Simulation (Phase Error to big)

Output Frequency vs. Time

Every divider change excites a step response from the PLL at the output. If the system remains linear all the system responses for all single divider changes can be summed up. The linearity is guaranteed through a limit for ΔN. For the calculation of the response to a single divider change the closed loop transfer function is used. Here a result from 4.1.2 is used.

$$T(s) = \frac{Kpd \cdot H(s) \cdot Kvco \cdot N_{old} \cdot \frac{1}{s}}{N_{old} + \frac{Kpd \cdot H(s) \cdot Kvco}{s}} = \frac{\varphi_{out}(s)}{\varphi_{in}(s)} \tag{4.36}$$

The divider is changed to $N_{new} = N_{old} + \Delta N$, with $\Delta N \ll N_{old}$. This means the transfer function of the loop can be handled like a constant.

So the output phase signal can be found with:

$$\varphi_{out}(s) = T(s) \cdot \varphi_{in}(s) \tag{4.37}$$

The divider change again creates a sudden frequency step Δf_{step} on the feedback input of the phase detector, and this equates to a phase ramp input signal [35].

$$\Delta f_{step} \sim f_{ref} \cdot \frac{\Delta N}{N_{old}} \tag{4.38}$$

$$\varphi_{in}(s) = \frac{2 \cdot \pi \cdot \Delta f_{step}}{s^2} \sim \frac{2 \cdot \pi \cdot f_{ref} \cdot \frac{\Delta N}{N_{old}}}{s^2} \tag{4.39}$$

$$\varphi_{out}(s) = \frac{Kpd \cdot H(s) \cdot Kvco \cdot N_{old} \cdot \frac{1}{s}}{N_{old} + \frac{Kpd \cdot H(s) \cdot Kvco}{s}} \cdot \frac{2 \cdot \pi \cdot f_{ref} \cdot \frac{\Delta N}{N_{old}}}{s^2} \tag{4.40}$$

We are interested in the output frequency versus time, and not in the output phase versus time, so we have to differentiate the output phase. We multiply the equation with s. The input signal has now become a step function.

$$f_{out}(s) = \frac{Kpd \cdot H(s) \cdot Kvco \cdot N_{old} \cdot \frac{1}{s}}{N_{old} + \frac{Kpd \cdot H(s) \cdot Kvco}{s}} \cdot \frac{2 \cdot \pi \cdot f_{ref} \cdot \frac{\Delta N}{N_{old}}}{s} \tag{4.41}$$

A resulting step response of $T(s)$ can be seen in Figure 4.12. This waveform shows the deviation of the output frequency due to a divider change. A step of $\Delta N = 0.3781$ was used for this example, and a reference frequency of $22\ MHz$, which yields an expected frequency deviation of $\Delta N \cdot fref = 8.3182\ MHz$. In radian, this equals to $52.3\ Mrad$ per second, which matches with the response in 4.12.

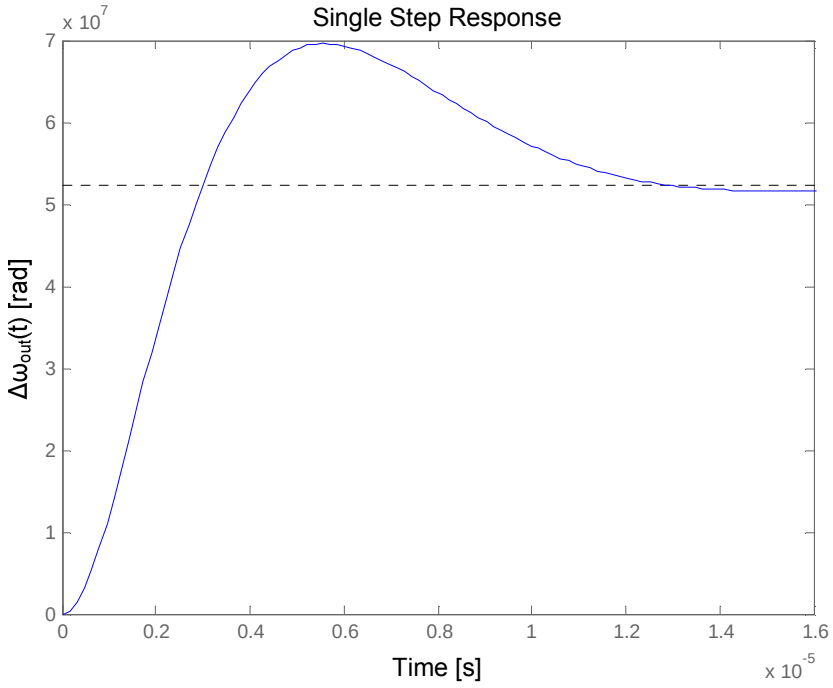


Figure 4.12: Single Divider Step Output Frequency Response

All single divider change responses can be added. So a periodically change, like in the measurement cycle, yields to a loop filter output voltage vs. time waveform like in Figure 4.10.

4.1.3 Procedure

First the phase locked loop is set to a mean frequency, and after it has settled the feedback divider setting is periodically changed. One possible implementation could use the waveform in Figure 4.13 for the divider ratio, which has the $test$ frequency $ftest$. The output frequency of the phase locked loop will swing around the mean frequency. The following waveforms in Figure 4.14a 4.14b 4.14c 4.14d

are a result of a transient simulation of the voltage model with the stimulus in Figure 4.13.

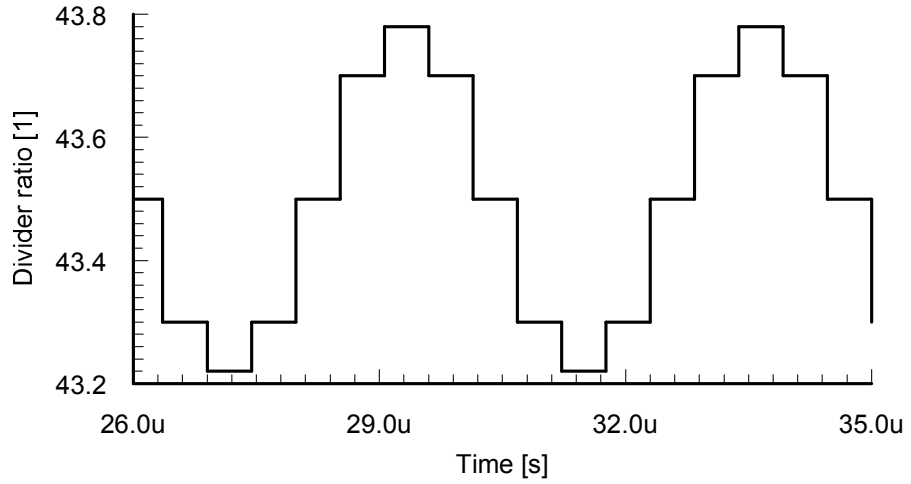
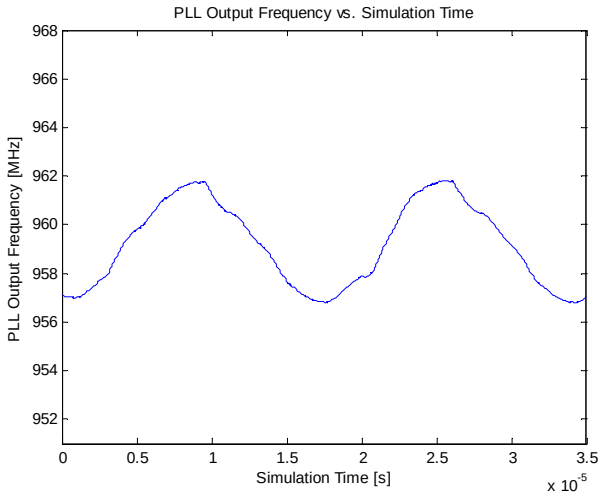


Figure 4.13: Divider ratio [1] vs. time [s]

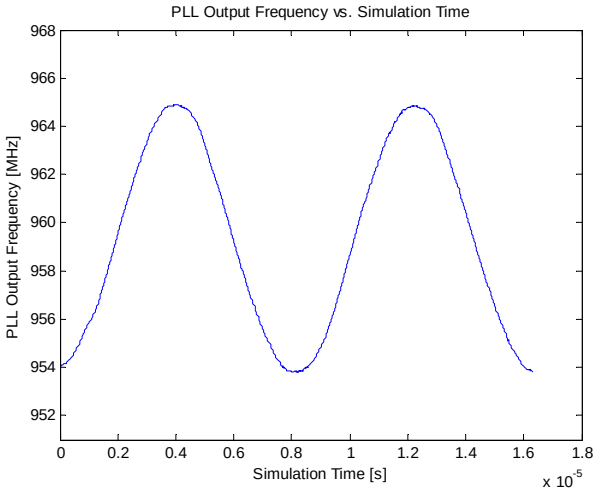
If the high frequency components of the stimulus are higher than the PLL bandwidth, then these signal components are filtered out in the loop filter and the PLL system itself, and so the output frequency change over time will be close to a sinusoidal shape [36, 1]. This is not the case in Figure 4.14a, and with this type of waveform which is not at least an approximation of a sinusoidal curve the concept is not working very well. If the concept should be used to measure the transfer function of the PLL below the current bandwidth, the divider ratio can be changed more often in a $test$-signal period time (e.g. 8 times in a period) in a near sinusoidal shape over time. With this a near sinusoidal modulation waveform is generated, and the measurement principle does also now work below the current bandwidth of the PLL.

The marked area A under the waveform (Figure 4.15) is proportional to the amount of phase which is the modulated output phase leading or lagging behind the output phase, if there had been no modulation, after a half period of the $test$ frequency.

In the proposed implementation, the divider ratio change amplitude (frequency deviation) is increased proportional with increasing divider switching frequency ($ftest$, data rate). The effect of this is, that the amount of phase deviation of the input stimulus signal is constant over different $test$ frequencies. Therefore as long as the PLL can follow this modulation, the area A (=phase deviation) in the

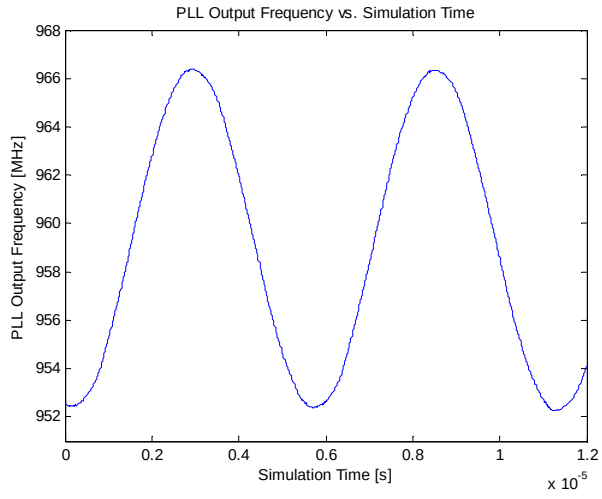


(a) $ftest = 60\ kHz$, Output Frequency Deviation = $1.66\ MHz$

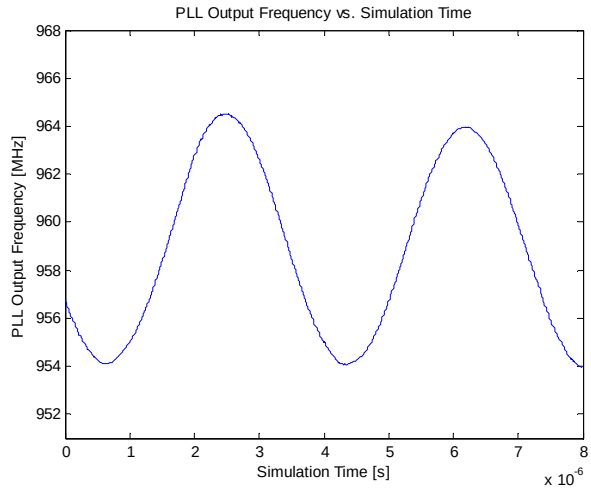


(b) $120\ kHz$, $3.32\ MHz$

Figure 4.14: Voltage Model Transient Simulation Results



(c) $180\ kHz$, $4.98\ MHz$



(d) $270\ kHz$, $7.47\ MHz$

Figure 4.14: Voltage Model Transient Simulation Results

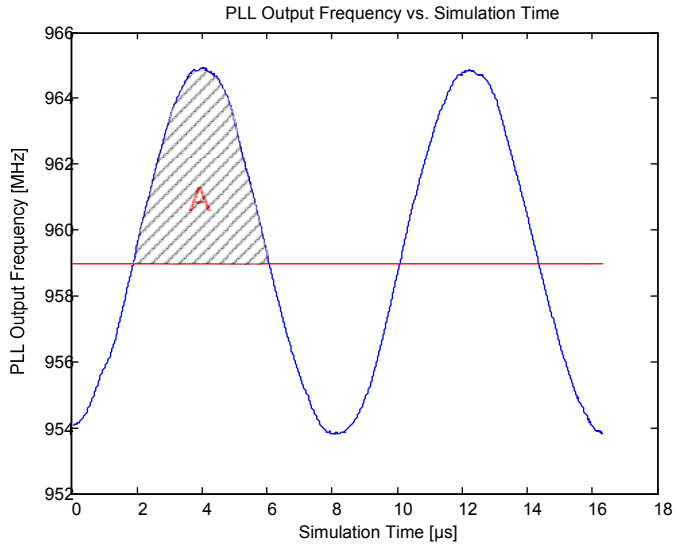


Figure 4.15: Output Frequency [MHz] vs. time [μs]

waveform shown in Figure 4.15 is constant. If the $test$ frequency exceeds the PLL bandwidth the area A starts to drop.

The basic principle is to measure the phase deviation with a time-to-digital conversion based on a ring oscillator (Figure 4.16). For this the current phase state of the TDC ring oscillator is sampled at a rising edge of the PLL output signal. By subtracting the previous phase state from the current one, a digital value proportional to the output period time of the PLL is found. These digital values are then used to numerically integrate and obtain the value for the area A.

Because the area A is defined between the output frequency curve and the mean output frequency line, a DC cancellation unit calculates the difference between these two curves, and the differences are then numerical integrated.

Figure 4.18 shows the accumulated number of inverters, which have changed their state. This waveform is created by the numerical integration at a $test$ frequency of $260\ kHz$. The difference between a local minimum value and a subsequent local maximum value of this curve, or vice versa, is proportional to the phase deviation, and equals to the value of A.

Figure 4.17 shows a transient simulation result: on the y-axis the number of inverters which have changed their state in R periods (prescaler divide by R in front of the TDC) of the PLL output signal is shown. This is a metric for the period time and for the output frequency of the PLL respectively. The sinusoidal signal

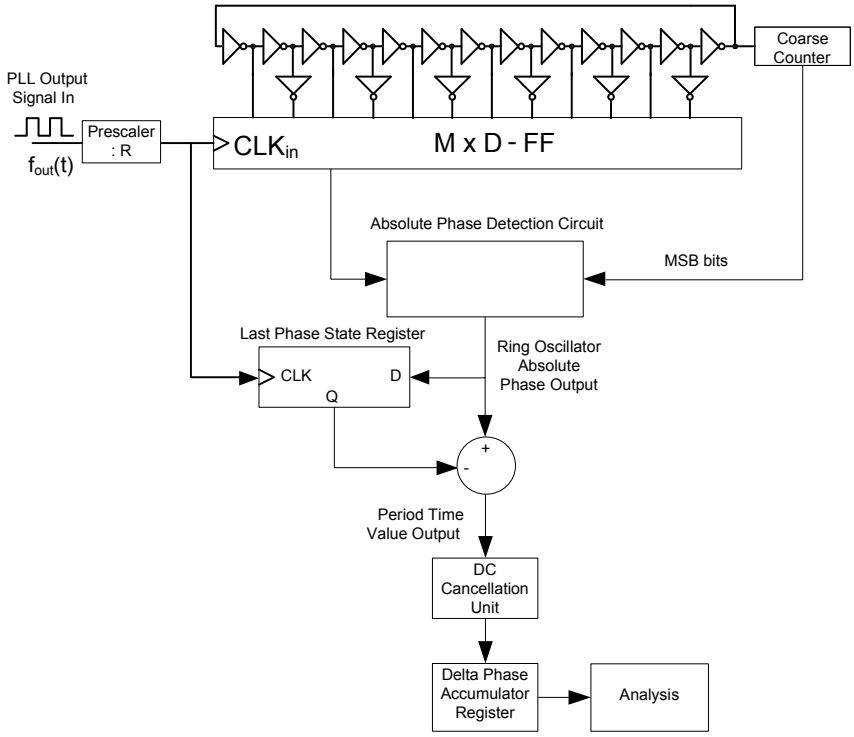


Figure 4.16: Measurement Setup Structure

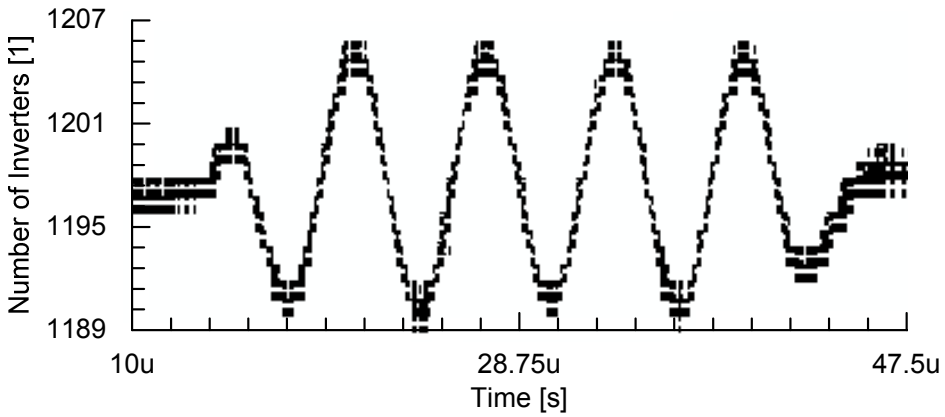


Figure 4.17: TDC Output Period Time [Number of Inverters] Simulation Result

part in the middle shows a test signal stimuli.

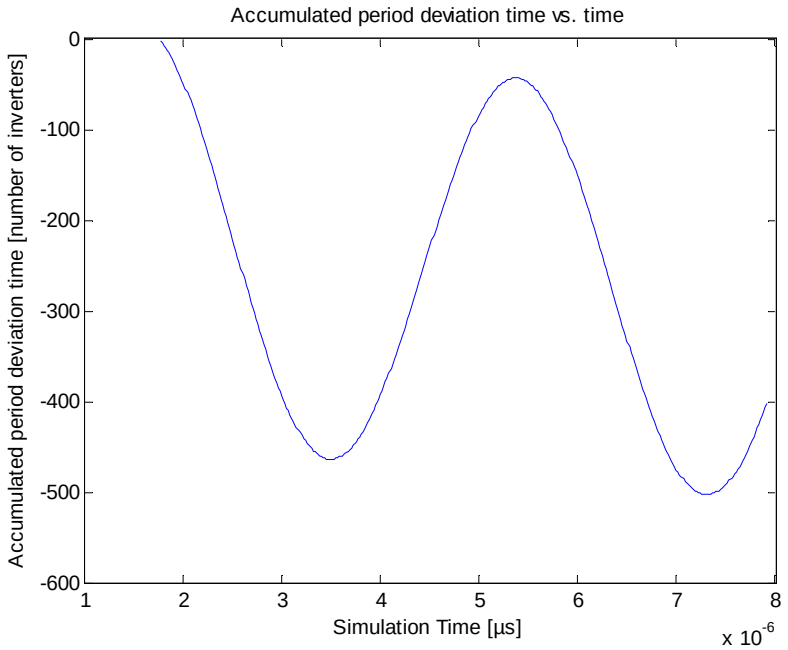


Figure 4.18: Accumulated Period Deviation Time [Number of Inverters] vs. time [μs]

PLL Transfer Function Measurement Example In Figure 4.20 the closed loop transfer function gain plot of a PLL is presented, which had been acquired by this measurement principle. It shows the phase deviation (=area A value) for a lot of different divider switching frequencies (=$test$ frequency) in the range of 70 up to $240\ kHz$. The overshoot at approximately $125\ kHz$ is due to peaking of the loop, and the $-3dB$ bandwidth of the loop is approximately at a frequency of $210\ kHz$. For comparison, Figure 4.19 shows the same part of the bode plot taken from the linear model in Matlab.

Bandwidth Calibration This basic principle could also be used for on-chip PLL bandwidth calibration. A possible implementation could, for example measure the $-3dB$ bandwidth of the phase locked loop, and then tune this parameter to the specified value. To obtain the bandwidth the value for A is measured at a low enough $test$ frequency. After this measurement cycles with increasing $test$ frequency are done, until a point with an area A result is found, which equals the

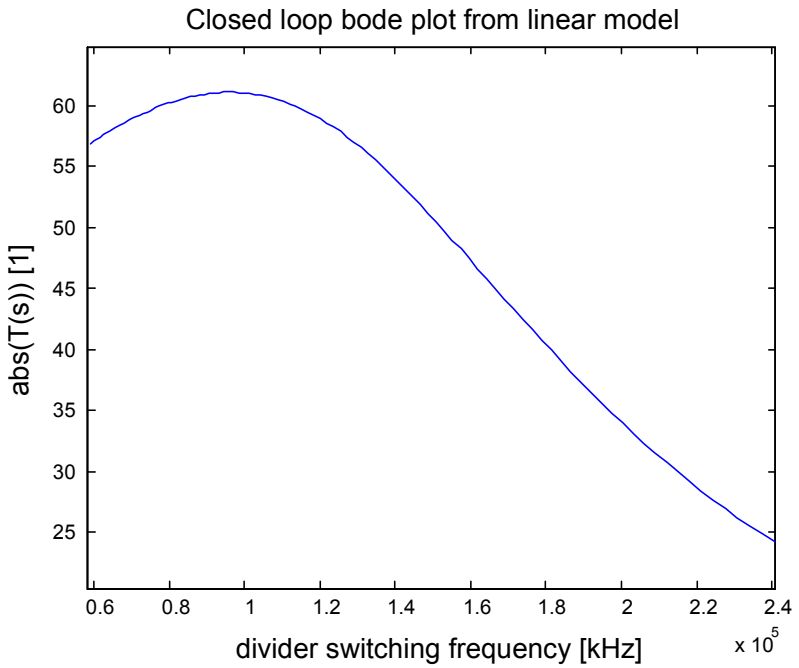


Figure 4.19: Phase Model Bode Plot (MatLab)

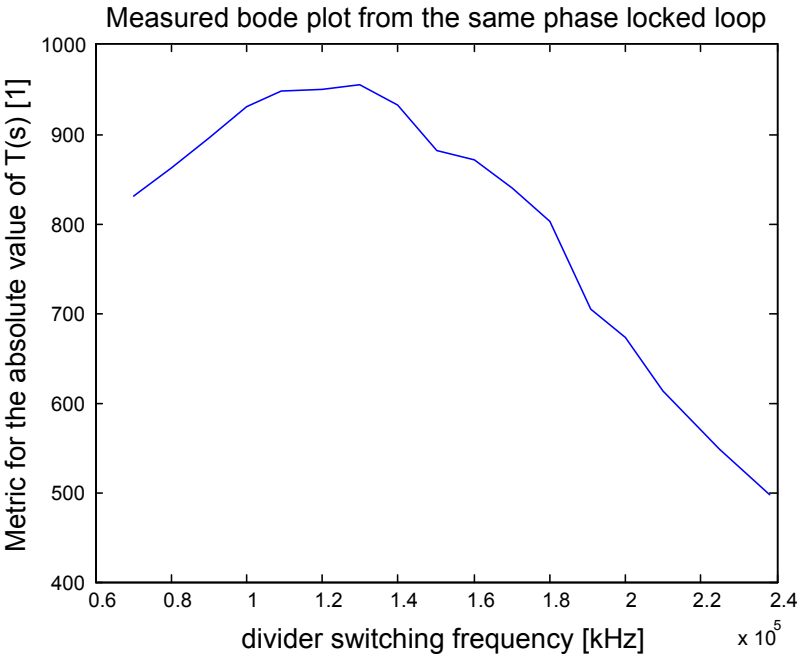


Figure 4.20: Proposed Measurement Method gained Bode Plot

inital value of A at the low $test$ frequency divided by $sqrt(2)$. The $test$ frequency where this specific value for A is found, equals then the bandwidth of the phase locked loop.

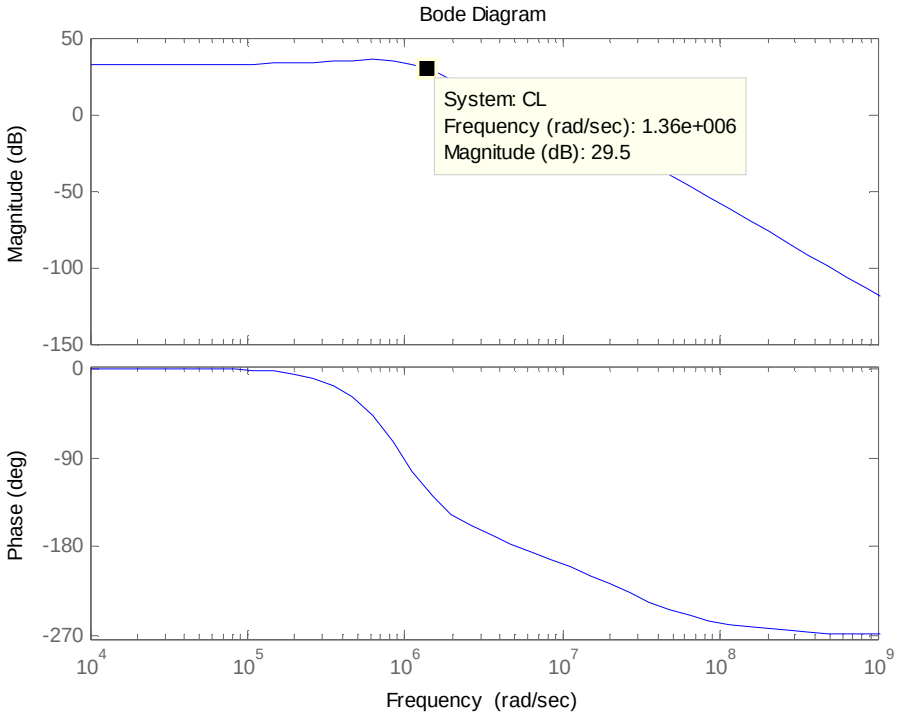


Figure 4.21: Linear Phase Model derived Bandwidth

For bandwidth calibration an easier way is also possible. The divider switching frequency ($ftest$) can be fixed to any point in the bode plot, and then cyclic measurements can be done until the area A result matches a specified value. If not, the charge pump current can be adjusted. Because a variation of the gain in the loop alters the whole closed loop transfer function, a single and fixed $test$ frequency is enough. The value of A is proportional to the gain in the loop.

4.1.4 Measurand Approximation

This section repeats the idea of this measurement principle in terms of equations. The resulting equation approximates the value of the bandwidth metric result number A, depending on the setup and the device under test.

The mean input frequency after the prescaler R at the input of the TDC block is

$$f_0 = \frac{N \cdot f_{ref}}{R} \tag{4.42}$$

Until now the variable N had been used to describe the absolute feedback divider setting from which then a step was done to another new setting. From this point on now N does denote the mean divider setting. This new definition is choosen, because it does fit with the definition used in the transient simulation model. If we use equation 4.16 the period time peak deviation ΔT_p the time-to-digital converter unit measures can be calculated, if the output frequency has a peak deviation of Δf_p while modulating the PLL.

$$\Delta T_p = -\frac{\Delta f_p}{f_0^2 \cdot R} = -\frac{\Delta f_p \cdot R}{N^2 \cdot f_{ref}^2} \tag{4.43}$$

The peak deviation Δf_p is proportional to $T(s)(ftest)$ of the closed loop at the current $test$ frequency. While the modulation does take place, periodically frequency steps are generated at the input of the phase detector, and therefore at the input of the PLL phase model. The size of this steps can be calculated with Equation 4.33 and 4.38. This input stimulus can be seen at the output of the PLL scaled by $|T(s)(ftest)|$.

Therefore Δf_p is found with

$$\Delta f_{step} \sim f_{ref} \cdot \frac{\Delta N}{N} \tag{4.44}$$

$$\Delta f_p = f_{step} \cdot |T(s)(ftest)| \tag{4.45}$$

$$\Delta f_p = \frac{\Delta N}{N} \cdot f_{ref} \cdot |T(s)(ftest)| \tag{4.46}$$

If t_d denotes the typical mean propagation delay of an inverter in the time-to-digital converter block (=TDC resolution), then the peak deviation ΔI_p in number of inverters that will not turn over or will turn over additionally in case of Δf_p can

be found with:

$$\Delta I_p = \frac{\Delta T_p}{t_d} = -\frac{\Delta N \cdot |T(s)(ftest)| \cdot R}{N^3 \cdot f_{ref} \cdot t_d} \tag{4.47}$$

A small enough resolution t_d of the time-to-digital converter would make ΔI_p big enough, to reach the necessary sensitivity for the measurement of $T(s)(ftest)$. This is not the case, and so the area A value was introduced, which is derived by a numerical integration over one half period of the modulation signal.

The duration of a half period of the modulation (test) signal is

$$T_m = \frac{1}{2 \cdot ftest} \tag{4.48}$$

In this time interval T_m the sinusoidal shaped waveform $\Delta I(t)$ with its peak value ΔI_p is sampled X times with the TDC unit, and a new value is added to the delta phase accumulator register. Because the output period time of the PLL does change slightly while the modulation does take place, the calculated value of X is also an approximation. For the rest of this calculation the assumption is made, that the time distance between all samples of the TDC will remain constant, and that only a small error is generated.

$$X \simeq \frac{T_m}{\frac{1}{f_0}} = \frac{T_m \cdot N \cdot f_{ref}}{R} \tag{4.49}$$

What should be found in this calculation is an approximation for the value of the bandwidth metric A. The value of A equals the area below the waveform in the first half of the period. Because the amplitude ΔI_p of the sinusoidal shaped waveform is known, a property of sinusoidal signals can be used to derive A.

The average rectified value is defined by

$$\overline{|\Delta I(t)|} = \frac{1}{2 \cdot T_m} \cdot \int_0^{2 \cdot T_m} |\Delta I(t)| \, dt \tag{4.50}$$

This definition of the average rectified value does look at a full period of the input

waveform. Because the rectified input signal is already periodic after a half period, it is enough to calculate the average rectified value over the first half period. Because the input waveform is always positive over the first half period also the absolute value operation can be ignored.

We now get

$$\overline{|\Delta I(t)|} = \frac{1}{T_m} \cdot \int_0^{T_m} \Delta I(t)\, dt \tag{4.51}$$

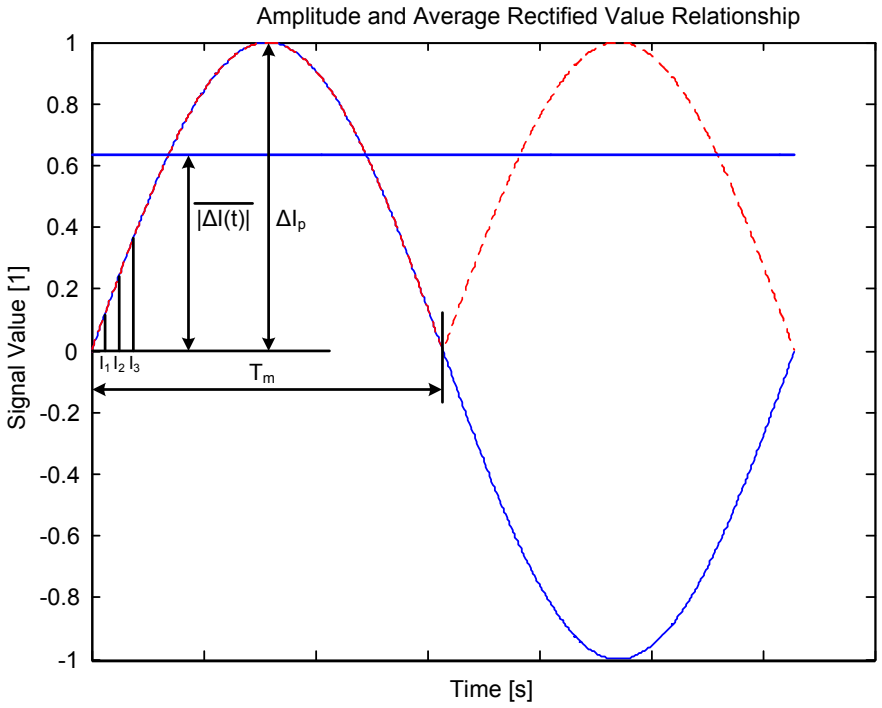


Figure 4.22: Amplitude and Average Rectified Value Relationship

Only the values at specific time points (=samples) are delivered by the converter and the DC cancellation unit, and therefore this definition is rewritten to

$$\overline{|\Delta I(t)|} \simeq \frac{1}{X} \cdot \sum_{k=1}^{X} \Delta I_k = \frac{1}{X} \cdot (\Delta I_1 + \Delta I_2 + ... + \Delta I_X) \tag{4.52}$$

It can be seen that the result of the sum equals the value of A. The relationship for a sinusoidal signal between the amplitude and the average rectified value is

given by (Figure 4.22)

$$\overline{|\Delta I(t)|} = \frac{2}{\pi} \cdot \Delta I_p = \frac{1}{T_m} \cdot \int_0^{T_m} \Delta I(t)\, dt \simeq \frac{1}{X} \cdot \sum_{k=1}^{X} \Delta I_k \tag{4.53}$$

$$\overline{|\Delta I(t)|} \simeq \frac{1}{X} \cdot A \tag{4.54}$$

$$A \simeq X \cdot \overline{|\Delta I(t)|} = X \cdot \frac{2}{\pi} \cdot \Delta I_p \tag{4.55}$$

After insertion of X and ΔI_p a result for the area A value is gained

$$A \simeq -\frac{\frac{1}{2 \cdot ftest} \cdot N \cdot f_{ref}}{R} \cdot \frac{2}{\pi} \cdot \frac{\Delta N \cdot |T(s)(ftest)| \cdot R}{N^3 \cdot f_{ref} \cdot t_d} \tag{4.56}$$

$$A \simeq -\frac{\Delta N \cdot |T(s)(ftest)|}{N^2 \cdot \pi \cdot t_d \cdot ftest} \tag{4.57}$$

This equation can be used to get an approximation for A at a specific $test$ frequency. The value of A does not only depend on $|T(s)(ftest)|$, but also on the current modulation (=test) frequency $ftest$. For a bandwidth calibration with a fixed frequency $ftest$ this is no problem, but if the bode plot should be measured at different frequencies, then this dependence is unwanted. The solution is to increase ΔN proportional with $ftest$.

$$\Delta N(ftest) = ftest \cdot \frac{\Delta N_{refpnt}}{f_{refpnt}} \tag{4.58}$$

Variables ΔN_{refpnt} and f_{refpnt} define a value for ΔN at a chosen reference point.

$$A \simeq -\frac{\Delta N_{refpnt} \cdot |T(s)(ftest)|}{N^2 \cdot f_{refpnt} \cdot \pi \cdot t_d} \tag{4.59}$$

Now that the dependency of A on $ftest$ is gone, the result depends only on $|T(s)(ftest)|$. A small value of N and t_d is used, to make the measurement more

sensitive (Equation 4.61).

$$\frac{dA}{dt_d} = \frac{\Delta N_{refpnt} \cdot |T(s)(ftest)|}{N^2 \cdot f_{refpnt} \cdot \pi} \cdot \frac{1}{t_d^2} \tag{4.60}$$

$$\frac{dA}{d|T(s)(ftest)|} = -\frac{\Delta N_{refpnt}}{N^2 \cdot f_{refpnt} \cdot \pi \cdot t_d} \tag{4.61}$$

$$\Delta A = -\frac{\Delta N_{refpnt}}{N^2 \cdot f_{refpnt} \cdot \pi \cdot t_d} \cdot \Delta|T(s)(ftest)| + \frac{\Delta N_{refpnt} \cdot |T(s)(ftest)|}{N^2 \cdot f_{refpnt} \cdot \pi} \cdot \frac{1}{t_d^2} \cdot \Delta t_d \tag{4.62}$$

Conclusions for the Implementation Beside the absolute value of the closed loop transfer function, t_d also has an influence on the result (Equation 4.60). There are two possibilities to stabilize or cancel the effect of t_d:

- Tune t_d: The inverters in the TDC core are tuned at the startup to obtain a specified propagation delay t_d.
- Measure t_d: Measure t_d at the startup, but no tuning, and digital correction of the results.

To measure the current time t_d in both cases, a time-to-digital conversion of a well-known and stable reference frequency can be done [16]. This reference frequency is created by the PLL itself for the startup of the calibration unit.

4.2 Implementation

4.2.1 System Overview

The top architecture of the bandwidth calibration unit is presented in Figure 4.23.

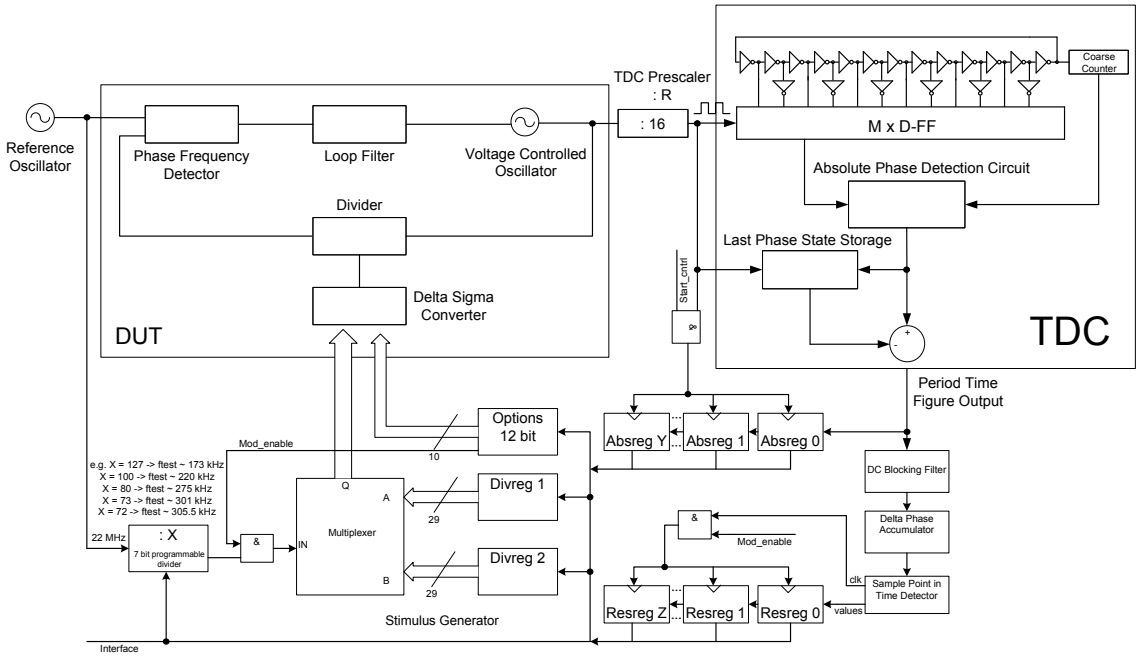


Figure 4.23: Bandwidth Calibration Unit Structure

4.2.2 TDC Converter

The used converter is introduced at 3.3. The TDC prescaler, with its division factor R in Figure 4.23 allows a lower mean TDC input frequency, and therefore also the clock frequency of the complete data processing block of the bandwidth calibration unit is decreased, which saves a high amount of energy. The value of R has no effect on the measurement result, as is demonstrated in chapter 4.1.4. The downside of a huge value for R is that it increases the amount of bits needed in the TDC coarse counters, because the measurement time interval gets longer. This means more power dissipation. So there is a tradeoff when selecting R.

4.2.3 DC Cancelling

The TDC unit delivers a digital number which is proportional to the PLL output period time. Interesting for us is the difference between the current and the mean output period time while modulating the divider, and so the DC component of the TDC output signal has to be canceled out. The DC cancellation unit estimates the mean output period time value from the TDC output signal with the help of averaging over a amount of P output period time samples, while the loop is unmodulated and settled. The structure of this unit and the delta phase accumulator register is shown in Figure 4.24. This DC cancellation is effective, because it only needs an adder and a register in which a amount of P samples are summated. Afterwards the register value bits are simply shifted to the right by $ld(P)$ bits.

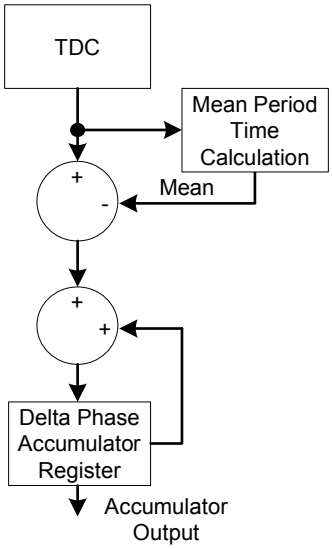


Figure 4.24: Implemented DC Cancellation Unit Structure with Delta Phase Accumulator Register

Because this calculated mean period value is used for all the calculations afterwards, this kind of DC component cancellation does not provide tracking ability. If the mean output period time drifts away from the precalculated one while the modulation does take place, which it very likely will, then we get a systematic error, which will be added to the delta phase accumulator with every new sample. If so the delta phase accumulator value drifts away from the zero line, and the subsequent analysis block must consider that. Also the finite resolution of the precalculated mean output period time can introduce a small error, that will have

the same effect on the delta phase accumulator curve.

It is important that the delta phase accumulator register is wide enough to handle the worst case situation for this kind of error without overflowing, and the delta phase accumulator is cleared from time to time, where it does not disturb the measurement, e.g. at the beginning of a new measurement cycle.

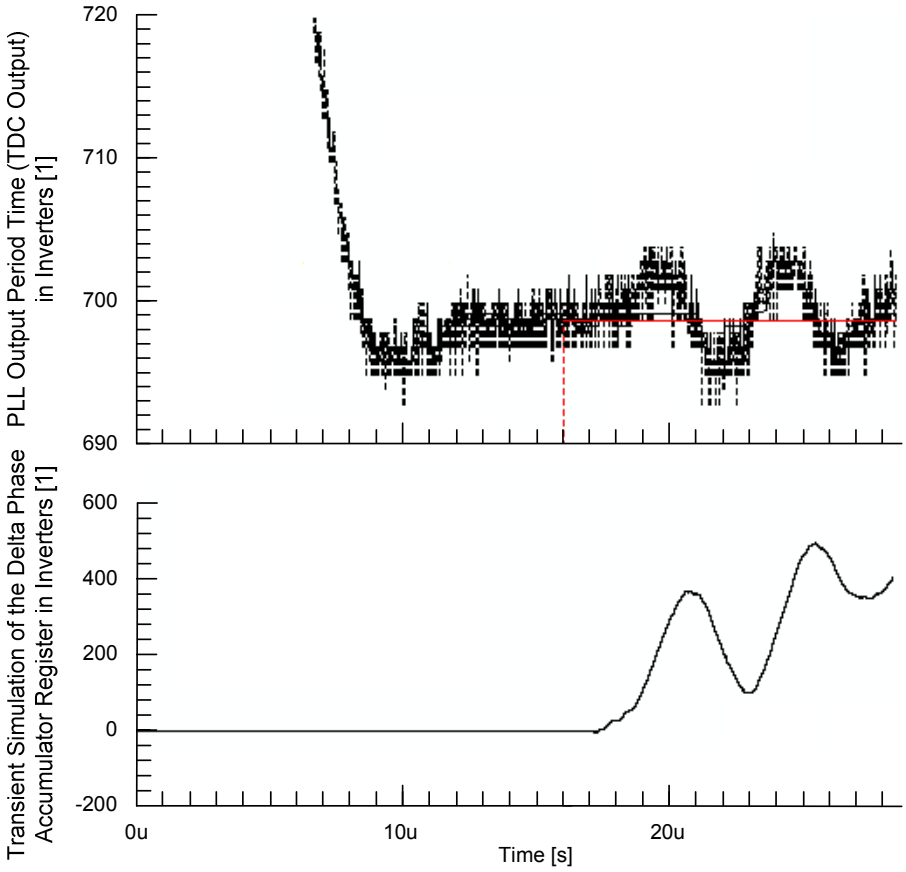


Figure 4.25: TDC Output Signal Mean Value driven Mean Period Time Cancellation

Figure 4.25 shows a Spectre simulation result from the PLL voltage model and the TDC which quantizes the PLL output signal period time, while the feedback divider is modulated with a frequency of $225\ kHz$. The mean period time is estimated with 64 TDC samples before the modulation, and the result is drawn in red in Figure 4.25. The black plot equals the TDC output value. While modulating the loop, the mean period time of the output signal drifts away from the estimated DC value (red curve), and so a systematic error has a big impact on the curve of the delta phase accumulator value which is drawn in the diagram below. Due to the

systematic error, this curve tends to drift away from the zero line over time, and this error is handled by the local minimum maximum detector and the analysis block.

4.2.4 Sample Point in Time Detector

Searching and extracting local minimum or maximum values of the delta phase accumulator register is done by a small logic unit. It monitors the register, and if a local extreme is found, a clock pulse for the following data processing unit is generated, and the associated value is provided at the output.

The circuit has two different operation modes which are alternately used. The first mode searches for a local maximum, and in this case, the currently found maximum value is stored in the register MREG. If a bigger input value is found then the MREG register is updated. This process repeats as long as the first operation mode is activated. An example for the variation in time of the delta phase accumulator register and the current mode of the circuit is shown in Figure 4.26.

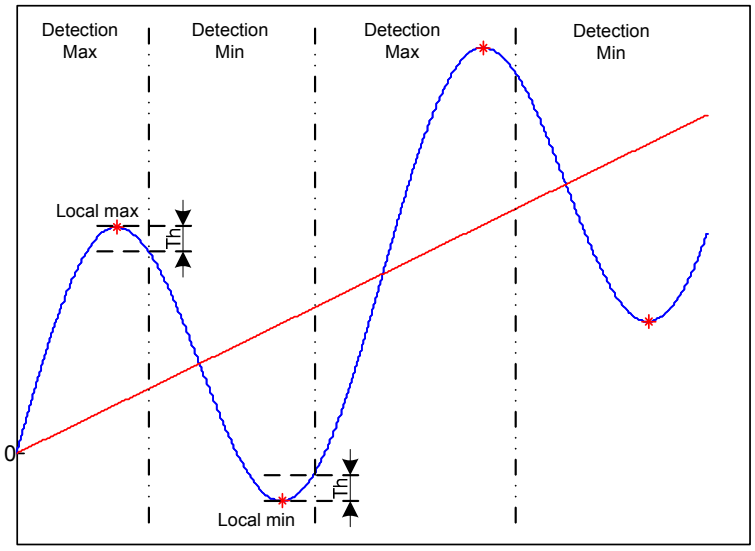


Figure 4.26: Delta Phase Accumulator Register Time Variation Example

The operation mode changes from state one to state two if a new input value is smaller than the currently maximum value stored in MREG minus a hysteresis called Th. In this case the maximum value stored in MREG is sent to the output, therefore to the further data processing blocks. The hysteresis inhibits a situation

in which a lot of changes of the state would occur, if the input value oscillates around a specific value. In operation mode two a local minimum is searched for and the currently minimum value is stored again in the MREG register. The circuit itself is slightly modified. If the local minimum is found its value is emitted again, and mode one is activated. This process repeats until the current measurement cycle is finished. The principle structure of the detector is presented in Figure 4.27.

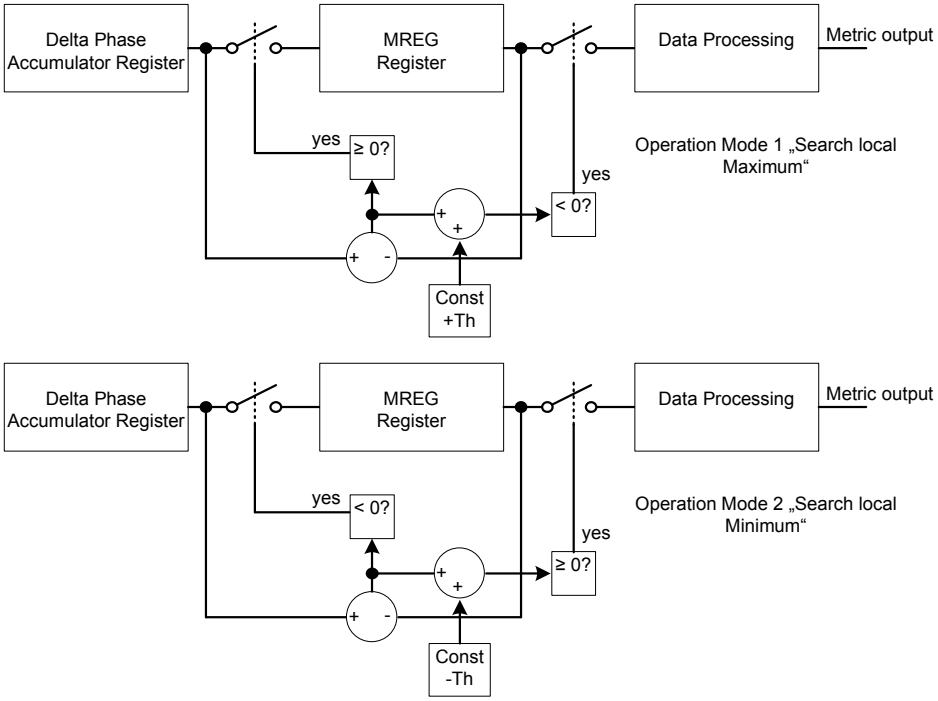


Figure 4.27: Sample Point in Time Detector Structure

Figure 4.27 shows the changes in the circuit between the two operation modes, which are two inversions of the comparator outputs, and a changed sign of the hysteresis constant value Th. In Figure 4.28 the idea of this circuit is developed a step further, and this implementation was also used for the simulation as a Verilog-A module.

4.2.5 Phase Deviation Processing

Ideally the local extreme values we get from the delta phase accumulator are taken from a sinusoidal signal which is centered around the zero line, because

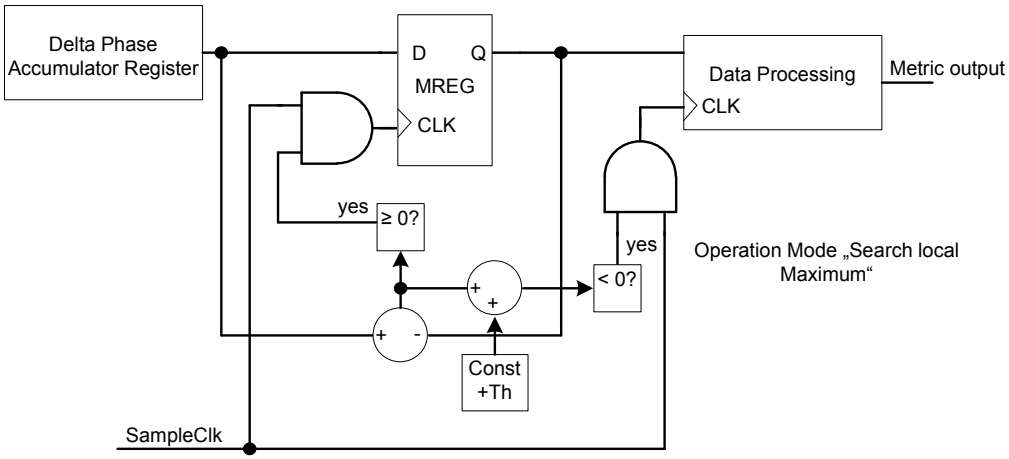


Figure 4.28: Clock Control Principle

the area below and above the mean period time (DC value), and the modulated output period time curve in a $test$ frequency period are equal. In this ideal case it is easy to derive the phase deviation, which is proportional to the metric of the bandwidth, because it can simply be found by subtracting the last local extreme value from the current one, and apply the absolute value. The number we get is then the area A value we are searching for.

Figure 4.29 shows this ideal case, and here the result for the (area A) value is 2. Normally the areas below and above the mean period time and the modulated output period time curve are not completely equal. This means the integration over the next period of the $test$ frequency starts already with a non zero initial value, and so the delta phase accumulator curve is wandering away from the zero line. This behaviour can be seen in Figure 4.25. Figure 4.30 shows this effect in a simplified way.

This effect makes the calculation of the bandwidth metric more complicated. If the absolute value from the difference of the current and last local extremum is only taken, we end up with a wrong result. This can only be corrected if we approximate the slope of the line which is underlying the sinusoidal signal for the last samples.

Figure 4.31 shows how the last three local extreme value samples from the delta phase accumulator register are combinded to approximate the slope K of the line. The value K is then used to correct the result for the bandwidth figure (=area A) again, and the effect of a slope K unequal to zero can be weakend.

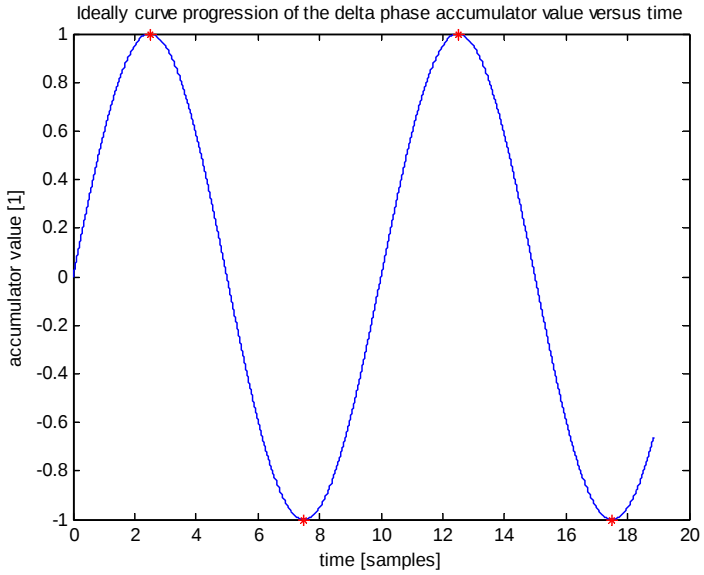


Figure 4.29: Ideal Delta Phase Accumulator Register Time Behaviour

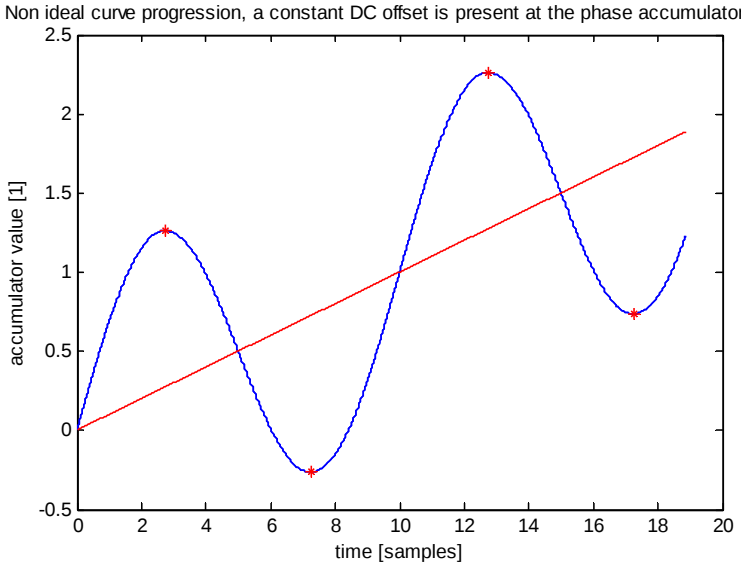


Figure 4.30: Nonideal Delta Phase Accumulator Register Time Behaviour

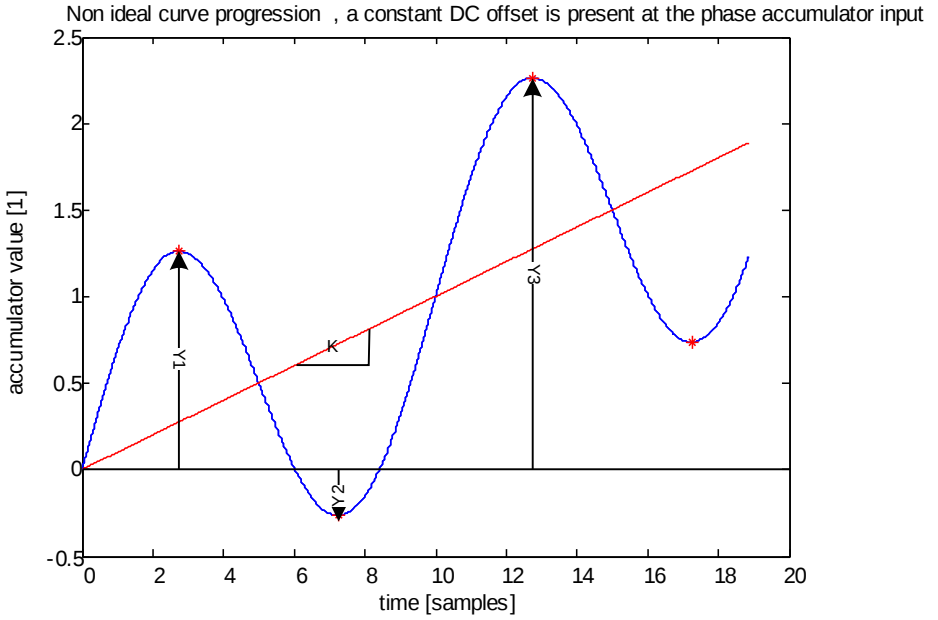


Figure 4.31: Nonideal Case Bandwidth Figure Calculation Principle

Slope of the line:

$$K = y_3 - y_1 \tag{4.63}$$

Metric A:

$$A = y_3 - \frac{K}{2} - y_2 = y_3 - y_2 - \frac{y_3}{2} + \frac{y_1}{2} \tag{4.64}$$

And so

$$A = 0.5 \cdot y_3 - y_2 + 0.5 \cdot y_1 \tag{4.65}$$

The multiplication of y_3 and y_1 with 0.5 is efficiently done with a single shift right operation. Afterwards these results are summed up with y_2 and the correction is finished. For the absolute value of this digital number the MSB bit can be discarded. If the two's complement digital representation is used for the calculation this is possible.

For the first two samples we process one or two needed values are missing,

that means the are set to 0, and the correction does not deliver us the correct figures. So the first calculated values for the bandwidth figure at the beginning of the test period are thrown away. Also after we start to modulate the phase locked loop we have to wait a little bit anyway, to give the circuit enough time to behave periodically.

In the end, all remaining single bandwidth figures of a measurement cycle are averaged to decrease the amount of statistical noise in the result, and can then be used to decide on the current bandwidth.

4.3 Other Measurement Techniques

If no time-to-digital converter is used for the measurement, other ways for the bandwidth measurement are possible. Because a TDC unit is used, this methods are not used in this thesis.

4.3.1 Bandwidth Measurement based on Crossover Time

Paper [37] shows a bandwidth measurement concept using the single step response crossover time of the closed loop PLL system, which is measured with a single counter. The phase step is induced with a short feedback divider value change. The peaking of the loop is also determined. An overshoot in the step response is necessary, but practically most phase locked loops will be useable with this technique. This paper demonstrates that the crossover time is inversely proportional to the bandwidth of the loop, and that its dependence on the step size of the input stimulus is not very strong.

4.3.2 Bandwidth Measurement based on Natural Frequency

In [35] the natural frequency of the phase locked loop is measured, and so this technique needs a underdamped phase locked loop. This result can then be used to tune the PLL in a way that the output behaviour fits with the specified one. The stimulus is done with a change of the divider value of the loop feedback divider, or the reference frequency divider if one is present. This introduces a frequency step to the PLL, and the behaviour of the loop can be observed. With a auxiliary PFD and a additional counter the natural frequency of the loop is measured, which depends on the gain of the loop.

4.3.3 Phase Transfer Function Measurement

In [36] the transfer function is determined. The stimulus is generated by a digitally controlled oscillator (DCO) at the input of the phase locked loop. A frequency counter at the loop output is used to measure the response.

4.3.4 Jitter Transfer Function Measurement

In [38] a PLL jitter transfer function measurement technique is presented. For the stimulus generation two different possibilities are shown. An input digital phase modulation with delay elements and a multiplexer is the first option, and a low-pass delta-sigma modulator with a additional charge pump which injects the test signal into the input of the loop filter another one. The measurement is done with sampling, and comparision of the sampled data. In this way the jitter transfer function is found.

4.4 Results

The bandwidth calibration principle is conducted in a transient simulation of the PLL voltage model (Figure 4.32). The time to digital converter consists of a 31-stage ring oscillator, and a Verilog-A processing block (Figure 4.33). The mean value DC cancellation block, the delta phase accumulator register, and the whole data processing blocks are also described with Verilog-A. The operation of the calibration is controlled with additional control logic. This logic introduces a delay before the modulation of the PLL starts, to give the PLL time to settle before the measurement is started. It also compares the measured bandwidth metric with the specified value, and if there is a discrepancy a corrective action is done before the next measurement cycle. In this way, the basic function of the principle can be demonstrated. The control blocks are presented in Figure 4.34.

First Simulation Run The first simulation uses the nominal charge pump current (=nominal PLL bandwidth setting) to demonstrate how the values for the calculation of the bandwidth metric A are generated. The nominal configuration of the phase locked loop has the following closed loop transfer function near the $-3dB$ bandwidth point (see Figure 4.35). The cursor shows the magnitude at a test frequency of $160\ kHz$.

Other parameters which were used in this simulation are a divider coarse part of $N = 43.5$, a reference frequency of $22\ Mhz$ ($Tref = 45.45\ ns$), and a TDC prescaler value of $R = 16$. Schematic 4.32 shows a coarse divider setting of only 43, but the $\Delta\Sigma$ converter is controlled in a way that it modulates around 0.5. In this way we get a setting of $N = 43.5$. The applied divider stimulus signal is drawn in Figure 4.36.

Figure 4.37 shows the data which was collected in the first transient simulation.

The first diagram shows the charge pump current setting, which can be set between 1 and 20. A value of 10 equals the nominal setting, and every single step equals 10 percent.

The second diagram shows the unfiltered output of the time-to-digital converter. In the time windows, where no modulation does takes place, the control logic gives the PLL time to settle and afterwards the mean output period time value is measured. The mean value result is drawn with the color red.

The third diagram from the top shows the delta phase accumulator register

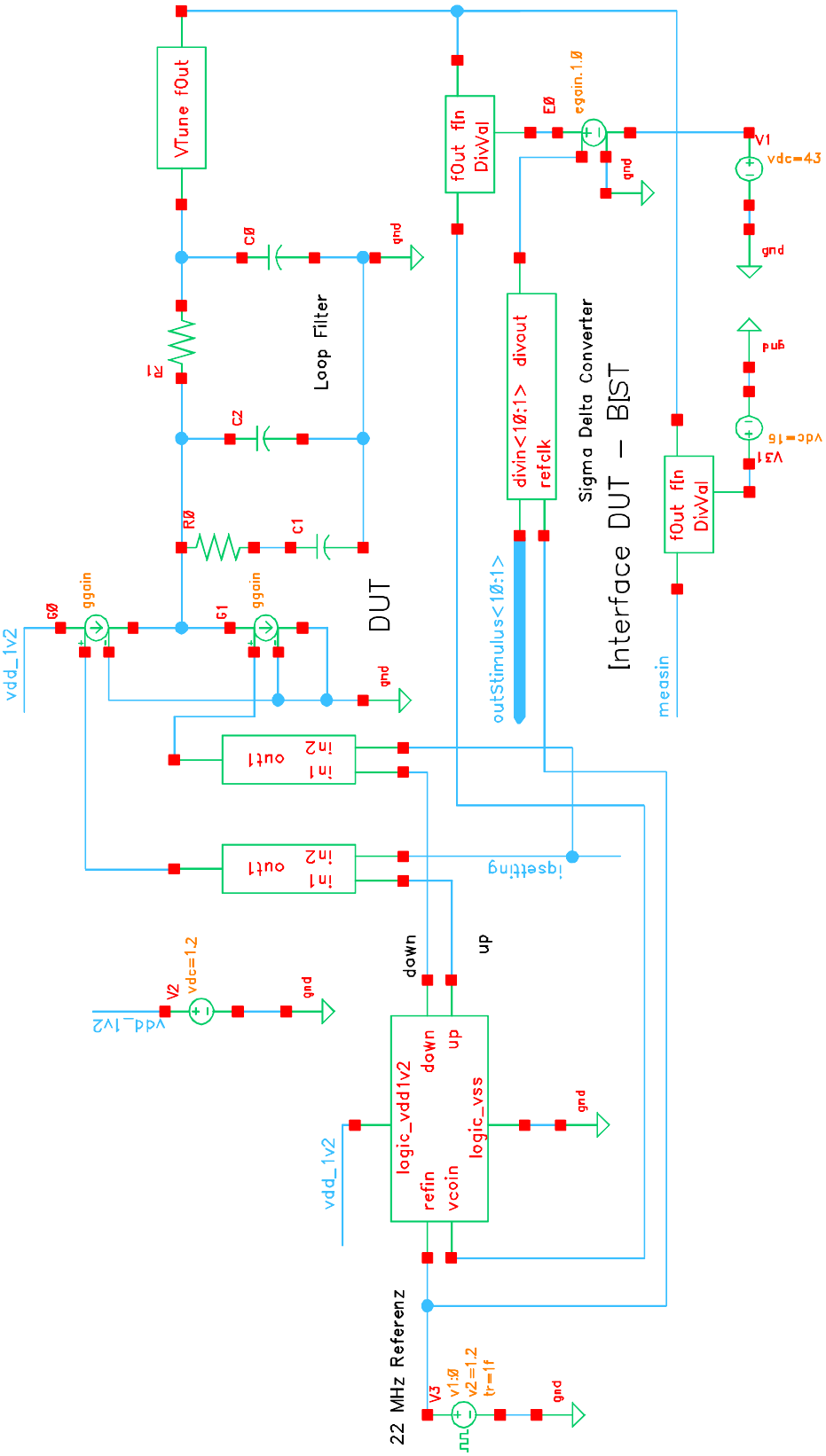


Figure 4.32: Voltage Model Setup

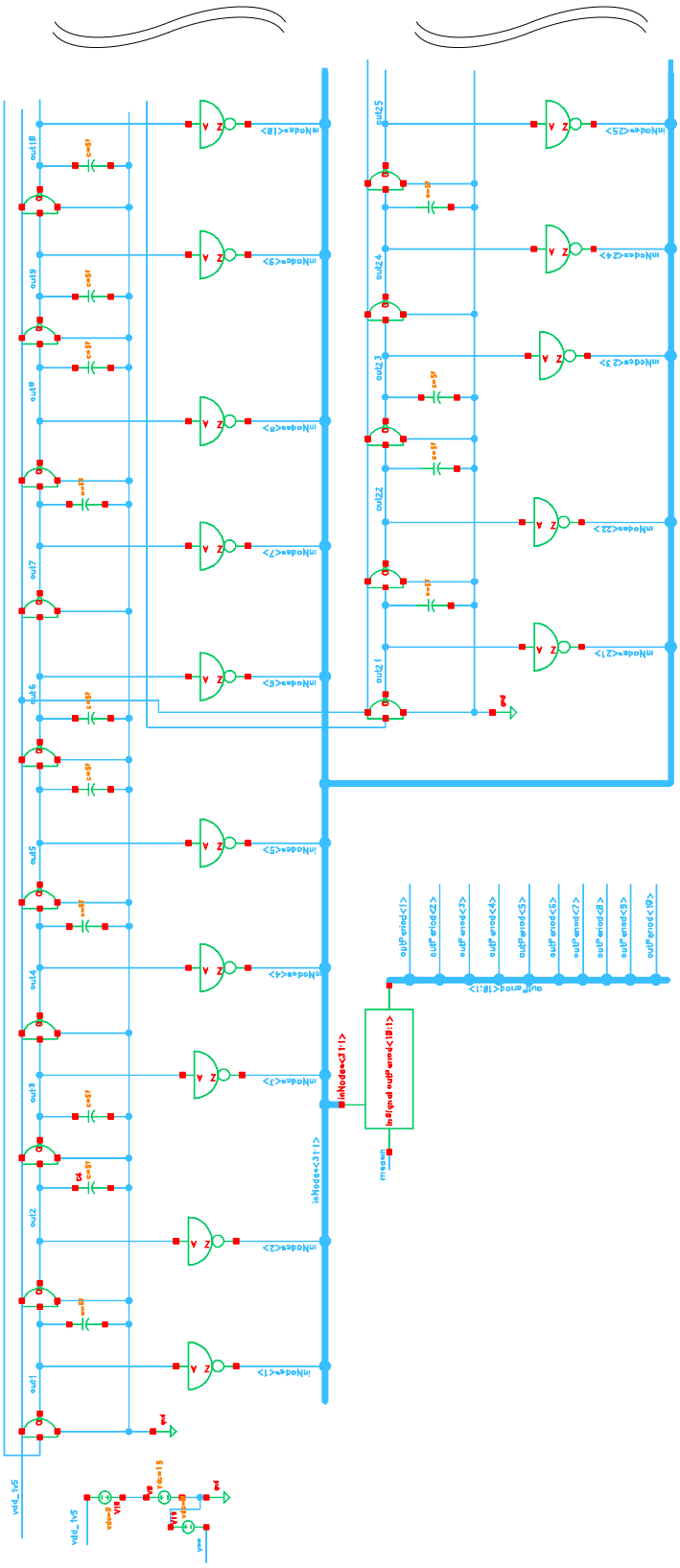


Figure 4.33: Time to Digital Converter Structure

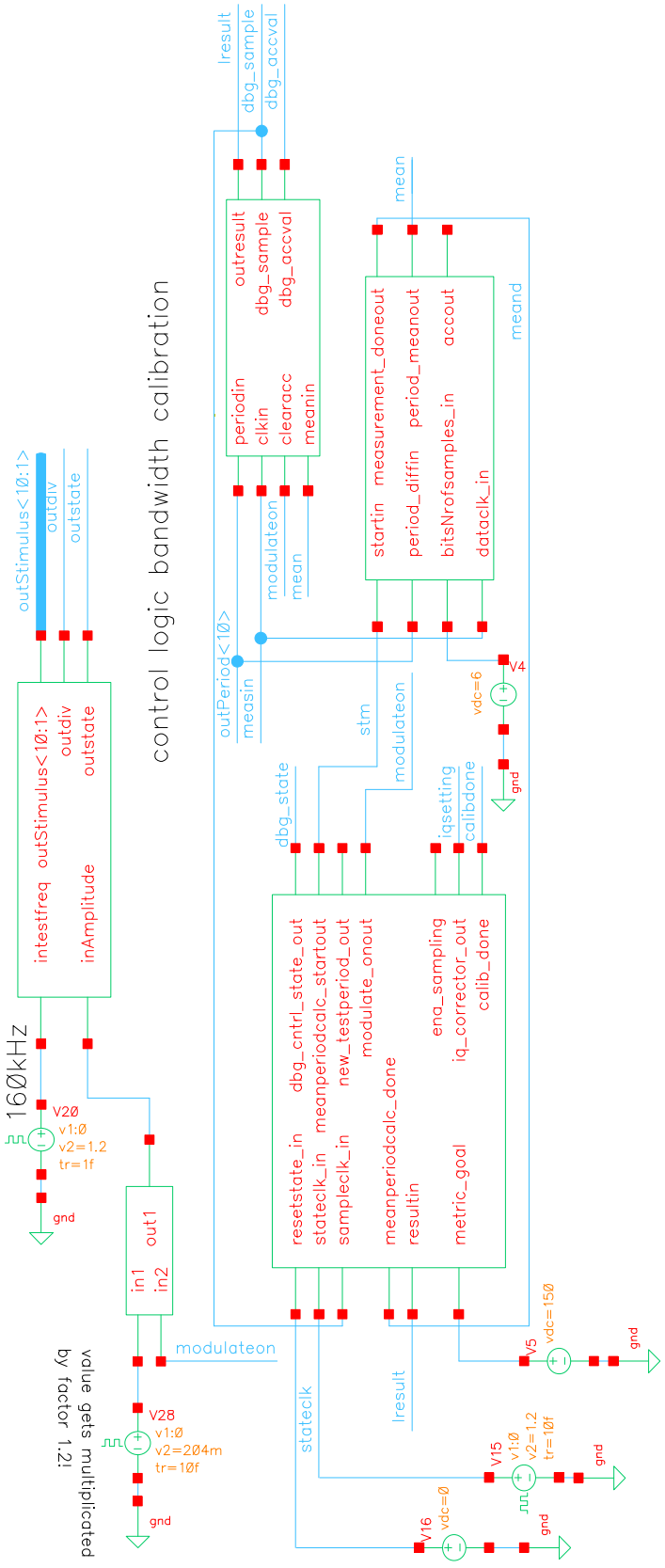


Figure 4.34: Bandwidth Calibration Unit Control Block

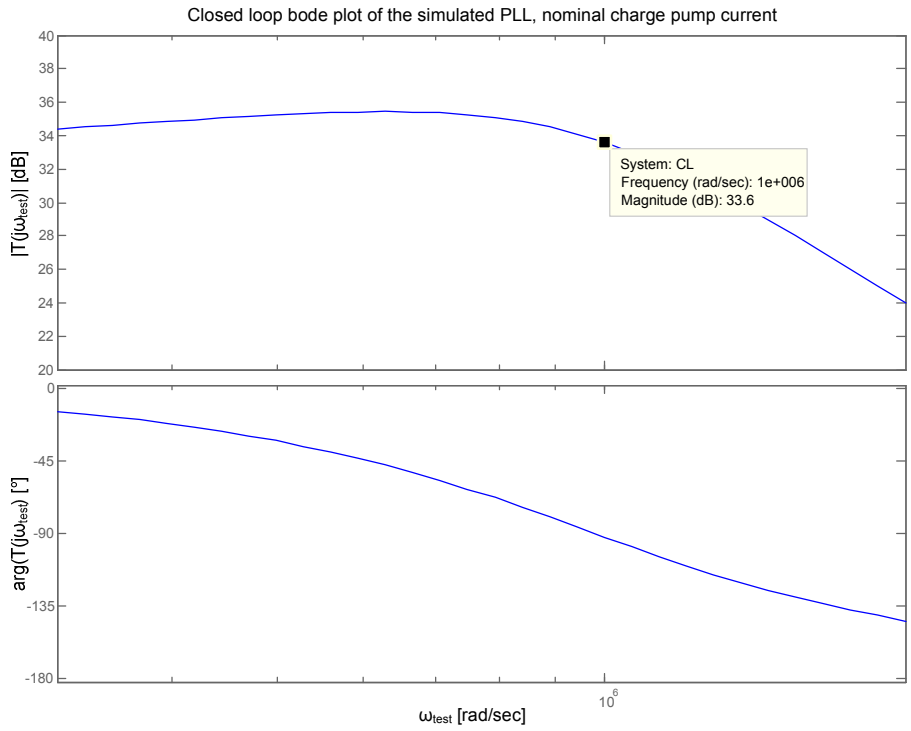


Figure 4.35: First Simulation: Nominal Charge Pump Current Setting PLL Transfer Function

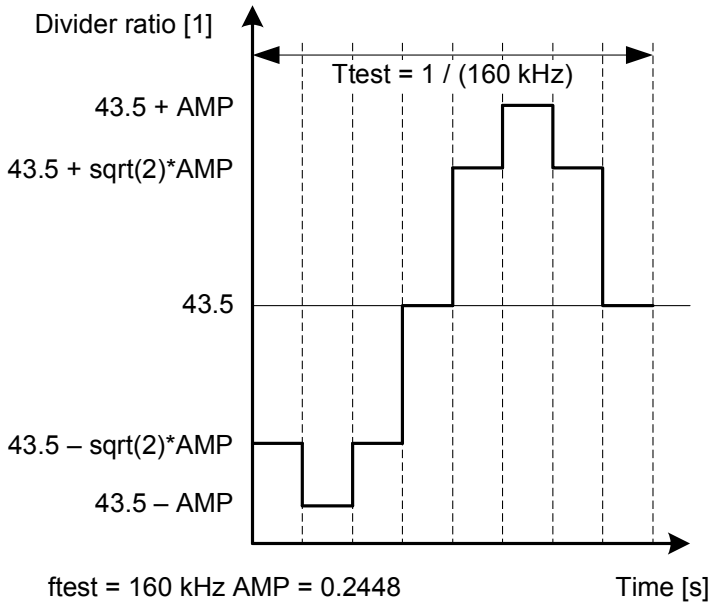


Figure 4.36: First Simulation: Feedback Divider Setting Variation in Time

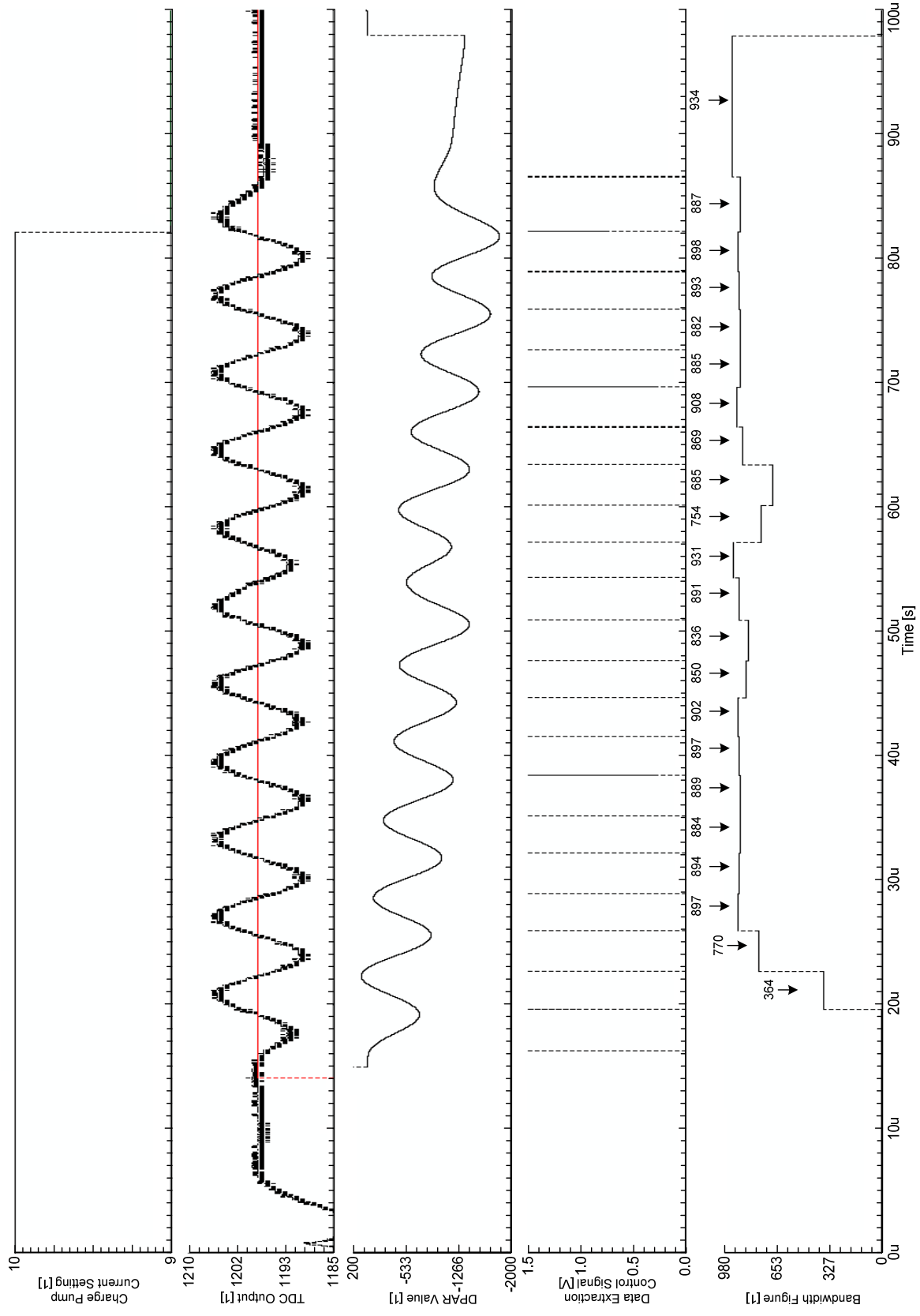


Figure 4.37: First Simulation Results

value, which value is reset at the beginning of a new measurement cycle by the control logic, to prevent that this register can easily overflow. If the local min/max detector finds a new local extremum then this value is sampled from the delta phase accumulator register, and is processed. When this happens is drawn in the fourth diagram.

The last diagram shows the results from the analysis process. Because this is the raw data which is sent to the control logic, this waveform does not show the finished metric figures. Instead it shows the single results which later form the bandwidth metric A after their mean value is calculated. The first samples are not used for the calculation of the metric figure, because here the phase locked loop has not engaged to the divider switching signal yet, and so the first results may not be correct. The single bandwidth metric results can be seen in Figure 4.37.

Analysis of the First Simulation Run results: nominal charge pump current All single result values have an average value of $A = 873$. This is the finished metric figure for the bandwidth of the loop for this measurement cycle with the nominal charge pump current. For comparision purposes here is the result from the equation (Equation 4.57) which was derived earlier: $|T(s)(ftest)| = 33.6\ dB$, $td = 14.6\ ps$ (typical delay of a TDC inverter).

$$A \simeq -\frac{\Delta N \cdot |T(s)(ftest)|}{N^2 \cdot \pi \cdot td \cdot ftest} = -\frac{0.244 \cdot 47.863}{43.5^2 \cdot \pi \cdot 14.6 * 10^{-12} \cdot 160 * 10^3} \tag{4.66}$$

$$A \simeq 841 \tag{4.67}$$

The measured bandwidth metric value in the simulation is 3.8% bigger than the estimated value from the equation.

Second Simulation Run The main idea for the second simulation run is to use a $test$ frequency of $270\ kHz$, which is far away from the peaking in the transfer function. With the new $test$ frequency we have to adopt the input stimulus of the divider. The now adapted stimulus is presented in Figure 4.38.

At the $test$ frequency of $270\ kHz$ the magnitude of the transfer function has already fallen by approximately $8\ dB$ (Figure 4.39). Now the result from the first run can be used to precalculate the values we should get from this new simulation

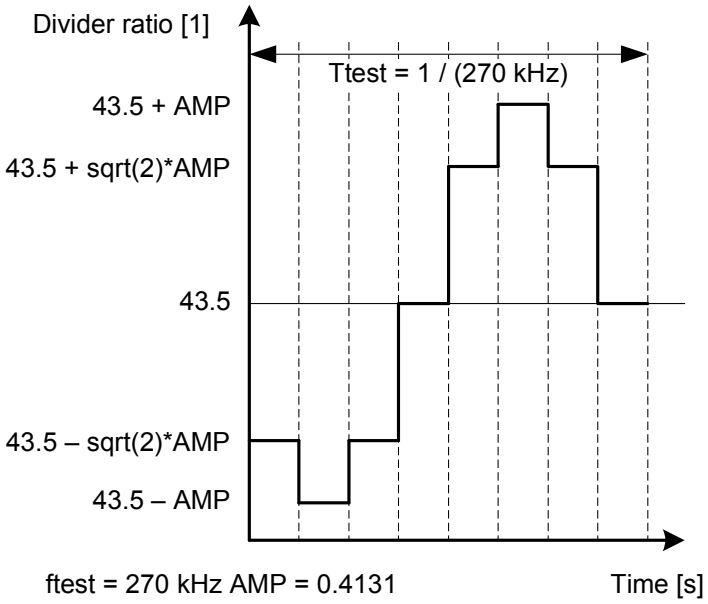


Figure 4.38: Second Simulation: Feedback Divider Setting Variation in Time

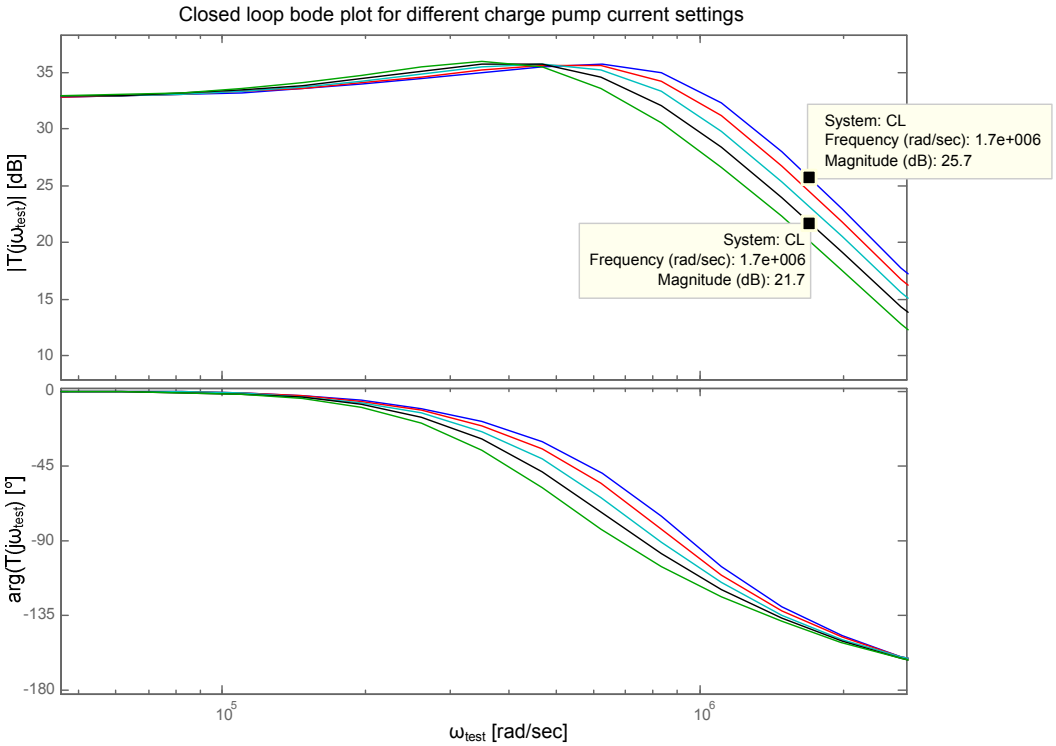


Figure 4.39: PLL Transfer Functions for Different Charge Pump Current Settings

with different charge pump current settings. The result of the first simulation run tells us that with a nominal charge pump current setting and a $test$ frequency of $160\ kHz$, a bandwidth metric of 873 is achieved. The new $test$ frequency will be $ftest = 270\ kHz$, and a charge pump current which is initially decreased by 30 percent is used.

First simulation run PLL transfer function gain: $|T(j \cdot 2 \cdot \pi \cdot 160kHz)| = 10^{\frac{33.6dB}{20}} = 47.863$ (nominal iq setting, Figure 4.35)

Extracted from bode plot in Figure 4.39: $10^{\frac{21.7dB}{20}} = 12.1619$ (at new $ftest = 270\ kHz$, nominal iq setting - 30%)

Second run expected bandwidth figure result = $873 \cdot \frac{12.1619}{47.863} = 222$ at $iq_{nom} - 30\%$ ($iqsetting = 7$)

The same calculation is also done for the other charge pump current settings:

Table 4.1: Second Simulation Run: Approximated Metric Results from Equation/Bode Plot

Iq	$iqsetting$	$Bodeplot\|T(s)(ftest)\|$	Approx. metric result
$Iq_{nom} - 40\%$	6	20.1	185
$Iq_{nom} - 30\%$	7	21.7	222
$Iq_{nom} - 20\%$	8	23.1	261
$Iq_{nom} - 10\%$	9	24.5	306
Iq_{nom}	10	25.7	352

The expected result for A at the nominal charge pump current is now specified as the wanted goal for the bandwidth metric for this calibration run. At the beginning of the simulation the charge pump current setting is set to 6 ($Iq_{nom} - 40\%$), to simulate a wrong value of $Kvco$. This deviation should be corrected by the bandwidth calibration block, after the fifth measurement cycle. The results are presented in Figure 4.40.

The bandwidth metric figure grows with every new measurement cycle, as does the bandwidth of the phase locked loop while the correction is done. The data is also visualized in Figure 4.41. The red plot shows the expected value, and the blue plot the measured results from the simulation. What also can be seen from

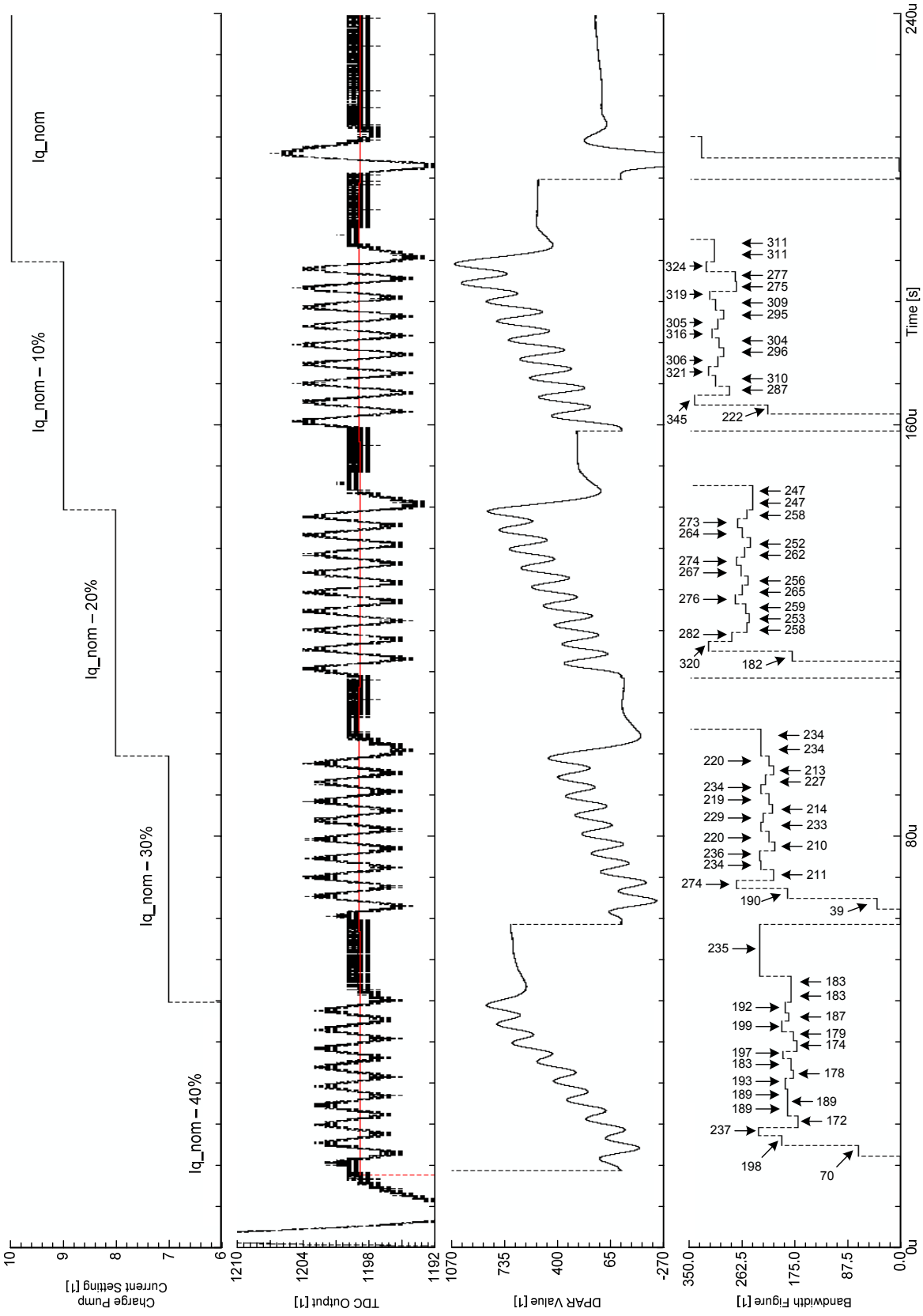


Figure 4.40: Second Simulation Results

Table 4.2: Second Simulation Run: Transient Simulation Results

Cycle	Iq	Expected	Average Sim	-3 dB bandwidth [kHz]
1	$Iq_{nom} - 40\%$	185	186	143
2	$Iq_{nom} - 30\%$	222	225	164
3	$Iq_{nom} - 20\%$	261	262	181
4	$Iq_{nom} - 10\%$	306	304	199
5	Iq_{nom}	352	-	215

this second simulation run is, that with a higher $test$ frequency in respect to the bandwidth of the PLL the sensitivity of the measurement principle decreases, because the absolute value of closed loop transfer function is already much smaller.

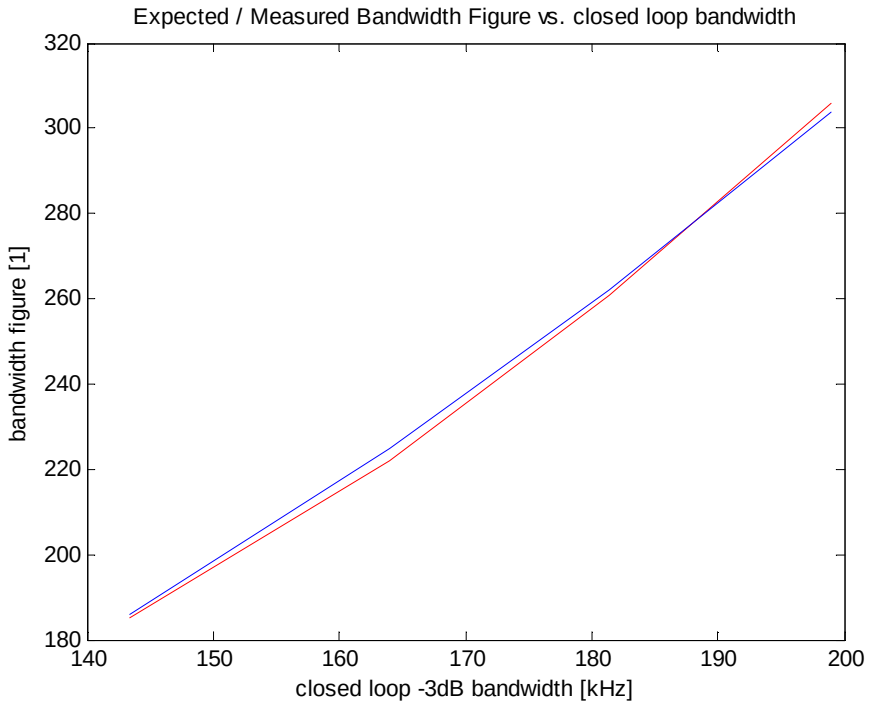


Figure 4.41: Second Simulation Result: Bandwidth Figure vs. Bandwidth, Red Line = Expected, Blue Line = Simulated

Third Simulation Run For higher $test$ frequencies well above the PLL $-3dB$ bandwidth a rectangular waveform for the divider stimulus can be used instead of the sinusoidal curve. The second simulation was repeated again, but this time with a rectangular stimulus signal. This new signal is illustrated in Figure 4.42. All other loop settings stayed the same as in the second simulation. Output of the

simulation in Spectre is illustrated in Figure 4.43.

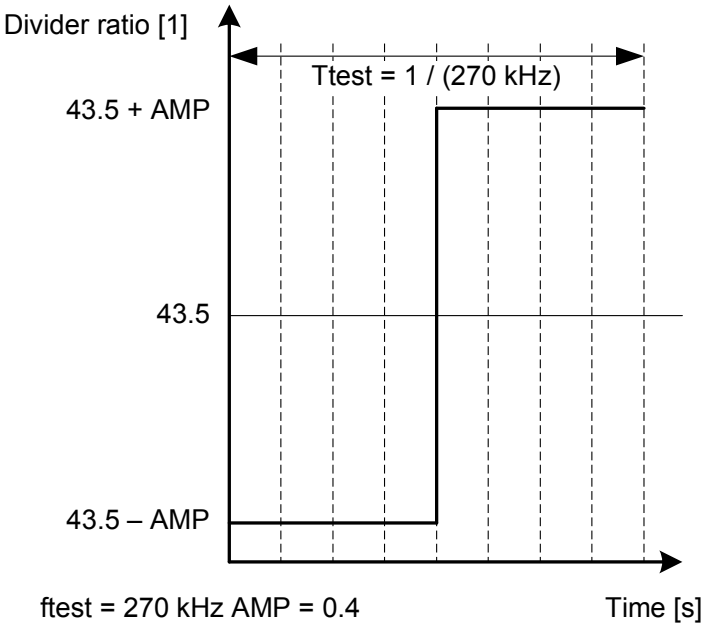


Figure 4.42: Third Simulation: Feedback Divider Setting Variation in Time

Table 4.3: Third Simulation Run: Transient Simulation Results

Cycle	Iq	$iqsetting$	Average Sim	Sim2 Result	Offset (%)
1	$Iq_{nom} - 40\%$	6	236	186	21.2
2	$Iq_{nom} - 30\%$	7	282	225	20.2
3	$Iq_{nom} - 20\%$	8	336	262	22.0

Because of the large simulation time for the third simulation run, the last two charge pump current settings were not finished. But as seen, the result is again dependent on the bandwidth of the phase locked loop, and therefore also from the charge pump current. If the results are compared with the second simulation a constant offset can be seen. Therefore the bandwidth figure is again proportional to the bandwidth of the closed loop.

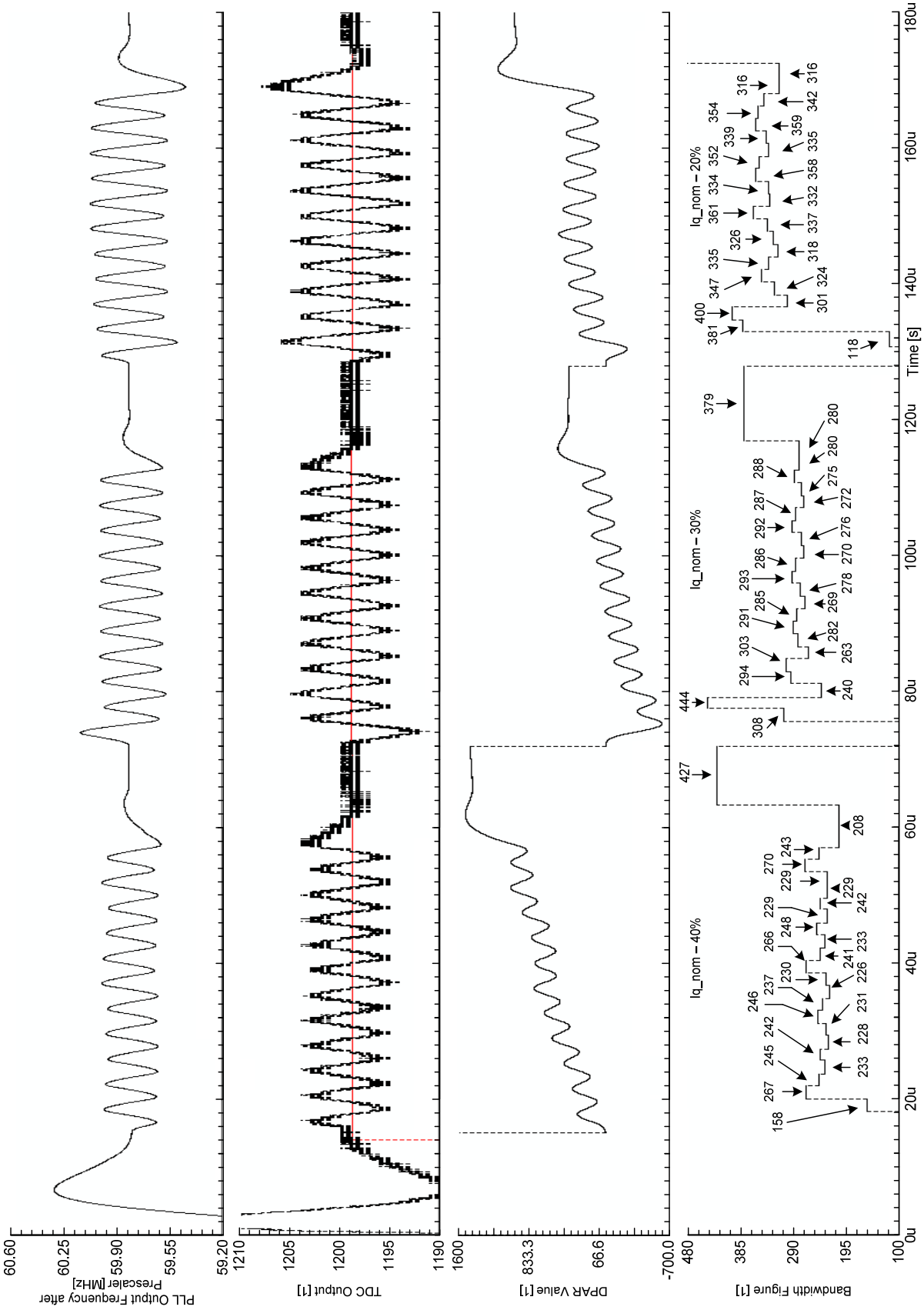


Figure 4.43: Third Simulation Results

5 Conclusion

This diploma thesis has shown a way in which the bandwidth of a phase locked loop can be measured and calibrated. The starting point for this method is a well known setup for the measurement of the closed loop transfer function of a PLL, which was then adopted in mainly two steps. The first one is the usage of the digital feedback divider setting for stimulus generation. The second step is the usage of a time-to-digital converter unit to monitor the modulation process, and therefore to collect the data. A time-to-digital converter which utilizes a ring oscillator was found. If the bandwidth is not correct, then the charge pump current setting is adjusted until the specification is met. The presented method for the measurement and calibration of the closed-loop bandwidth of a phase locked loop was tested and simulated in a transient simulation in Cadence/Spectre, and it has shown that the concept works.

Beside the time-to-digital converter core circuit and the coarse counter, all other parts of the bandwidth calibration unit can be implemented in VHDL, and therefore the implementation should be possible in an efficient way.

Bibliography

[1] D. Banerjee, *PLL Performance, Simulation and Design, Fourth Edition*. Dog Ear Publishing, LLC, 2006. [Online]. Available: http://www.national.com/appinfo/wireless/files/deansbook4.pdf

[2] S. Sattler, D. Oberle, and J. Eckmueller, "PLL built-in-self-test jitter measurement integration into 0.18u CMOS technology."

[3] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Science/Engineering/Math, 2000.

[4] R. Best, *Phase-Locked Loops, Design, Simulation, and Applications, Sixth Edition*. The McGraw-Hill Companies, Inc., 2007.

[5] B. Razavi, "A study of phase noise in CMOS oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 31, no. 3, pp. 331–343, 1996.

[6] G. Jovanovic and M. Stojcev, "A method for improvement stability of a CMOS voltage controlled ring oscillators." [Online]. Available: http://es.elfak.ni.ac.rs/Papers/A%20Method%20for%20Improvement%20Stability%20of%20a%20CMOS%20Ring%20VCO%20-%20Jovanovic&Stojcev.pdf

[7] M. Groezing and M. Berroth, "Reduction of CMOS inverter ring oscillator close-in phase noise by current mode instead of voltage mode supply." [Online]. Available: http://www.uni-stuttgart.de/int/forschung/CMOS/pdf/PRIME_2006_ReduktionPN_Paper.pdf

[8] T. Sailer, "Relaxationsoszillator Integer-N PLL für die ISM Bänder 315/434/868/915 MHz," Diplomarbeit, Graz University of Technology, 2005.

[9] K. Kundert, "Predicting the phase noise and jitter of PLL-Based frequency synthesizers," 2003. [Online]. Available: www.designers-guide.com

[10] A. Maentyniemi, “An integrated CMOS high precision time-to-digital converter based on stabilised three-stage delay line interpolation,” Ph.D. dissertation, University of Oulu, 2004.

[11] Y. Arai and M. Ikeno, “A time digitizer CMOS gate-array with a 250 ps time resolution,” *Solid-State Circuits, IEEE Journal of*, vol. 31, no. 2, pp. 212 –220, feb 1996.

[12] O. Bourrion and L. Gallin-Martel, “An integrated CMOS time-to-digital converter for coincidence detection in a liquid xenon PET prototype,” *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 563, no. 1, pp. 100 – 103, 2006, proceedings of the 7th International Workshop on Radiation Imaging Detectors - IWORID 2005. [Online]. Available: http://www.sciencedirect.com/science/article/B6TJM-4J90V05-K/2/259dee79648447a1df35917317d8cfd6

[13] Y. Arai, M. Ikeno, M. Sagara, and T. Emura, “Time memory cell VLSI for the PHENIX drift chamber,” in *Nuclear Science Symposium, 1997. IEEE*, 9-15 1997, pp. 8 –12 vol.1.

[14] Acam Mess Electronic, “Das TDC-Kochbuch,” 1998. [Online]. Available: http://www.mikrocontroller.net/attachment/690/TDC-Kochbuch.pdf

[15] Y. Arai and J. Christiansen, “TDC architecture study for the ATLAS muon tracker”.”

[16] I. Nissinen, A. Mantyniemi, and J. Kostamovaara, “A CMOS time-to-digital converter based on a ring oscillator for a laser radar,” in *Solid-State Circuits Conference, 2003. ESSCIRC ’03. Proceedings of the 29th European*, 16-18 2003, pp. 469 – 472.

[17] M. Mota, J. Christiansen, S. Debieux, V. Ryjov, P. Moreira, and A. Marchioro, “A flexible multi-channel high-resolution time-to-digital converter ASIC,” in *Nuclear Science Symposium Conference Record, 2000 IEEE*, vol. 2, 2000, pp. 9/155 –9/159 vol.2.

[18] J. Richardson, R. Walker, L. Grant, D. Stoppa, F. Borghetti, E. Charbon, M. Gersbach, and R. Henderson, “A 32x32 50ps resolution 10 bit time to

digital converter array in 130nm CMOS for time correlated imaging," in *Custom Integrated Circuits Conference, 2009. CICC '09. IEEE*, 13-16 2009, pp. 77 –80.

[19] M. Straayer and M. Perrott, "A 12-Bit, 10-MHz Bandwidth, Continuous-Time Sigma-Delta ADC with a 5-bit, 950-MS/s VCO-Based quantizer," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 4, pp. 805 –814, april 2008.

[20] R. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. Balsara, "1.3 v 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 53, no. 3, pp. 220 – 224, march 2006.

[21] M. Straayer and M. Perrott, "An efficient high-resolution 11-bit noise-shaping multipath gated ring oscillator TDC," in *VLSI Circuits, 2008 IEEE Symposium on*, 18-20 2008, pp. 82 –83.

[22] J. Kalisz, "Review of methods for time interval measurements with picosecond resolution," *Metrologia*, vol. 41, no. 1, p. 17, 2004. [Online]. Available: http://stacks.iop.org/0026-1394/41/i=1/a=004

[23] Y. Park and D. Wentzloff, "A cyclic vernier time-to-digital converter synthesized from a 65nm CMOS standard library," may. 2010, pp. 3561 –3564.

[24] P. Chen, S.-I. Liu, and J. Wu, "A low power high accuracy CMOS time-to-digital converter," in *IEEE International Symposium on Circuits and Systems, 1997*, 6 1997.

[25] A. Chandrakasan, S. Sheng, and R. Brodersen, "Low power CMOS digital design," *IEEE Journal of Solid State Circuits*, vol. 27, 1992.

[26] S. Joeres, A. Kruth, O. Meike, G. Ordu, S. Sappok, R. Wunderlich, and S. Heinen, "Design of a ring-oscillator with a wide tuning range in 0.13 m̆ CMOS for the use in global navigation satellite systems."

[27] A. Chandrakasan and R. Brodersen, "Minimizing power consumption in digital CMOS circuits," *Proceedings of the IEEE*, vol. 83, no. 4, pp. 498 –523, apr. 1995. [Online]. Available: http://bwrc.eecs.berkeley.edu/publications/1995/Min_pwr_consump_CMOS_crct/paper.fm.pdf

[28] J. Smith and F. Cady, “Metastability,” 2002. [Online]. Available: http://www.inf.ufrgs.br/~fglima/meta-estabilidade.pdf

[29] D. Markovick, “Analysis and design of low-energy clocked storage elements,” EECS Department, University of California, Berkeley, Tech. Rep. UCB/ERL M00/64, 2000. [Online]. Available: http://www.eecs.berkeley.edu/Pubs/TechRpts/2000/3927.html

[30] C. Ljuslin, J. Christiansen, A. Marchioro, and O. Klingsheim, “An integrated 16-channel CMOS time to digital converter,” *Nuclear Science, IEEE Transactions on*, vol. 41, no. 4, pp. 1104 –1108, aug 1994.

[31] Y. Arai, “TMC304(TMC-TEG3) trouble report,” 1996.

[32] Hewlett Packard HP, “New techniques for analyzing phase lock loops (AN 164-3) 5952-8142 June 1975,” 1975.

[33] K. Seongwon and M. Soma, “An all-digital built-in self-test for high-speed phase-locked loops,” *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 48, no. 2, pp. 141 –150, feb 2001.

[34] B. Veillette and G. Roberts, “Stimulus generation for built-in self-test of charge-pump phase-locked loops,” in *Test Conference, 1998. Proceedings., International*, 18-23 1998, pp. 698 –707.

[35] M. Cassia, P. Shah, and E. Bruun, “A calibration method for PLLs based on transient response,” in *Circuits and Systems, 2004. ISCAS ’04. Proceedings of the 2004 International Symposium on*, vol. 4, 23-26 2004, pp. IV – 481–4 Vol.4.

[36] M. Burbidge, J. Tijou, and A. Richardson, “Techniques for automatic on chip closed loop transfer function monitoring for embedded charge pump phase locked loops,” in *Design, Automation and Test in Europe Conference and Exhibition, 2003*, 2003, pp. 496 – 501.

[37] D. Fischette, R. DeSantis, and J. Lee, “An on-chip all-digital measurement circuit to characterize phase-locked loop response in 45-nm SOI,” in *Custom Integrated Circuits Conference, 2009. CICC ’09. IEEE*, 13-16 2009, pp. 609 –612.

[38] B. Veillette and G. Roberts, “On-chip measurement of the jitter transfer function of charge-pump phase-locked loops,” *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 3, pp. 483 –491, mar 1998.