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DA 708

Power Metering with Hall-based Current Sensor

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Abstract

As a consequence of the growing energy demand and increased use of renewable energy sources a smart control for an efficient utilization of the grid is becoming more and more important. Unfortunately, local generation of renewables through photovoltaics or wind power can not be controlled directly, nor can energy be stored in large quantities. This problem can be solved by continuously adapting the demand to the availability of electrical power provided in the grid. By means of Wireless Sensor Networks (WSNs), whose nodes measure the power consumption of the respective consumers (lighting units, washing machines, etc.), the grid can be made "smart" enough to distribute the power provided in the grid on demand.

The problem is that energy management systems which ensure an economical utilization of the grid are expensive and only affordable for industry and large scale commercial customers. The objective of this thesis is the development of a cost-efficient low-power power metering unit of small size, to enable integration in home appliances, suited for application in households as well as in small commercial buildings. The thesis is part of a project referred to as SmartCoDe[1] with a focus on precisely this challenge.

The development of the power metering unit is carried out by evaluating the architecture of a sensor node which enables cost-efficient low-power power measurement with little hardware. These specific requirements were fulfilled by using a test chip of an innovative current sensor TLI4970 and a transceiver Application-Specific Integrated Circuit (ASIC), both developed by Infineon Technologies AG.

[1] EU Project within the 7th Framework Program (CT-2009-247473)

Kurzfassung

Im Zuge des ständig wachsenden Energiebedarfs und dem zunehmenden Einsatz erneuerbarer Energien gewinnt eine intelligente Regelung zur effizienten Netzauslastung immer mehr an Bedeutung. Bedauerlicherweise kann die lokale Erzeugung elektrischer Energie aus erneuerbaren Ressourcen wie Photovoltaik oder Windanlagen nicht direkt beeinflusst werden, noch kann sie effizient in großen Mengen gespeichert werden. Durch eine Anpassung der Nachfrage an die zur Verfügung stehenden Leistung kann dieses Problem gelöst werden. Mit Hilfe von Wireless Sensor Networks (WSNs), dessen Sensorknoten den Leistungsverbrauch der jeweiligen Verbraucher (Beleuchtung, Waschmaschine, ...) messen, kann das Stromversorgungsnetz "'intelligent"' genug gemacht werden um die zur Verfügung stehende Leistung bedarfsgerecht zu verteilen.

Das Problem ist, dass Systeme, die eine ökonomische Auslastung des Energieversorgungsnetzes gewährleisten meist teuer und somit nur für Großkunden aus Wirtschaft und Industrie erschwinglich sind. Ziel dieser Arbeit ist es nun, ein kostengünstiges miniaturisiertes Leistungsmessgerät mit geringem Stromverbrauch zu entwickeln, das eine Integration in Haushaltsgeräte ermöglicht und für den Einsatz in Privathaushalten sowie kleineren öffentlichen Gebäuden geeignet ist. Diese Arbeit ist Teil eines Projektes mit dem Namen SmartCoDe[2], das sich mit genau dieser Herausforderung beschäftigt.

Im Laufe des Entwicklungsprozesses wird eine Architektur eines Sensorknotens evaluiert, die mit geringem Hardwareaufwand, geringem Stromverbrauch und hohem Miniaturisierungspotential eine Leistungsmessung ermöglicht. Diese speziellen Anforderungen des Leistungsmessgerätes werden mit einem Testchip des innovativen Stromsensors TLI4970 und einem Transceiver Application-Specific Integrated Circuit (ASIC), beide entwickelt von Infineon Technologies AG, erfüllt.

[2]EU Projekt innerhalb des 7th Framework Program (CT-2009-247473)

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List of Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
AMUX	Analog MUX
ASIC	Application-Specific Integrated Circuit
ASIP	Application-Specific Instruction-set Processor
ASK	Amplitude Shift Keying
DC	Direct Current
DIVT	Dynamic Interrupt Vector Table
DSP	Digital Signal Processor
ESR	Equivalent Series Resistance
EUP	Energy Using Product
FELV	Functional Extra Low Voltage
FIFO	First In, First Out
FSK	Frequency Shift Keying
GPRAM	General Purpose RAM
HF	High Frequency
HVAC	Heating, Ventilation, and Air Conditioning
IO	Input / Output
ISM	Industrial, Scientific and Medical
LED	Light-Emitting Diode
LSB	Least Significant Bit
MUX	Multiplexer
PCB	Printed Circuit Board
PFC	Power Factor Correction
PMU	Power Management Unit
PPU	Protocol Processing Unit
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RISC	Reduced Instruction-Set Computer
ROM	Read-Only Memory

RX	Receiver
SFR	Special Function Register
SOC	System On Chip
SPI	Serial Peripheral Interface
SRAM	Static RAM
SRD	Short-Range Devices
TRX	Transceiver
TX	Transmitter
UHF	Ultra-High Frequency
WLB	Wafer Level Ball Grid Array
WSN	Wireless Sensor Network

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Chapter 1

Introduction

This diploma thesis was carried out at the Institute of Electronics at the Graz University of Technology in cooperation with the Contactless and Radio Frequency Exploration (CRE) Department at Infineon Technologies Austria AG.

The first chapter introduces the motivation leading to the topic of power measurement embedded in a wireless sensor node. While the economic and industrial background considerations are covered in section 1.1, the conceptual formulation of the objective of this thesis is presented in section 1.2. Finally, a brief outline of the project is given in section 1.3.

1.1 Motivation, the SmartCoDe Project

The project SmartCoDe is a 7th Framewok Program funded by the European Union, with the objective of handling the volatility of renewables and supporting the transition from centralized to distributed local energy production. [FP7 b]

"Future buildings and neighborhoods are expected to combine a manifold of Energy Using Products (EUPs) ranging from electrical lighting to Heating, Ventilation, and Air Conditioning (HVAC) with locally available renewable energy sources and energy storages. Until now, advanced techniques for energy management are not yet applicable in an economically reasonable way in the smaller entities like in energy-positive buildings and neighborhoods" [Mahlknecht *et al.* 2010].

A major challenge of our society is to reduce carbon dioxide emissions. To achieve this ambitious goal, we are in the process of replacing coal and gas-driven power plants with photovoltaics and wind power plants. This does not directly affect information technology. The problem is that electrical energy can not be stored in an efficient way in large quantities. To solve this problem we have to continuously adapt the demand to the generation of

electrical power provided in the grid. Unfortunately, the generation of electrical energy from renewables such as photovoltaics and wind power plants can not be controlled directly. For this reason, we need information technology to make the grid “smart” enough to handle the volatility of renewables and to support the transition from centralized to distributed local energy production. [FP7 b]

The problem is that energy management systems which ensure an economical utilization of the grid are expensive and only affordable for industry and large commercial customers. In addition the energy demand of consumers (lighting units, washing machines, etc.) varies greatly. Matching the increasing demand of the end user approaching peak consumption is already expensive and will become more so in future. In order to adapt the demand to the availability of electrical power, the project SmartCode is trying to enable a low cost application for demand side management and smart metering in households and small commercial buildings as well as neighborhoods. The result is a new architecture for wireless sensor/energy management nodes that specifically considers the requirements of EUPs, building up a fine grained infrastructure. [Mahlknecht *et al.* 2010]

Among others, one approach of the project SmartCoDe is to promptly schedule the use of energy or switch EUPs into standby if the customer process allows that. To enable the application of advanced energy management techniques in energy-positive buildings and neighborhoods, infrastructure and methods are needed which fulfill the following requirements:

- No additional costs
- No new wires
- Small size
- Wireless communication infrastructure
- Information security

Lastly, intelligent management of energy contains a financial benefit for the end user and contributes to the stability of the grid. Things become even more advantageous if local energy production such as a small scale wind power plant becomes available. The varying energy demand of EUPs, and accordingly households or neighborhoods, can possibly be partially met with local energy production. [Mahlknecht *et al.* 2010]

1.2 Objective of this Thesis

The objective of this thesis was the development of a low-power power metering unit of small size for $230\,V$ grid connected devices. The power metering unit will be part of a wireless monitoring node, supposed to be integrated into any given home appliance (for example lighting units, fridges, washing machines, dishwashers or intelligent power plugs).

The power metering unit shall be based on an available test chip developed by Infineon Technologies AG, which is able to perform both current and voltage digital sampling with high sampling rate. A transceiver Application-Specific Integrated Circuit (ASIC) including a programmable protocol processor shall be used for digital signal processing of the captured current and voltage samples for subsequent power calculation.

In the theoretical part of this, thesis among others, the mathematical definitions of active power and apparent power has to considered. An analysis of algorithms to be implemented have to be performed in order to calculate the power of a sampled signal.

A first prototype and the corresponding firmware have to be developed in the practical part of this thesis. In order to enable a voltage measurement hardware has to be designed which steps down line voltage. The calculation of active power and apparent power as well as the implementation of the single-wire communication interface between the transceiver and the test chip have to be implemented.

An integration of the power metering unit into a wireless node and the realization of the required radio communication protocol handler have to be supported.

1.3 Thesis Outline

The first chapter introduces the topic of power measurement and the associated economical and industrial aspects. Considering the requirements to enable a fine-grained infrastructure, and subsequent integration into a Wireless Sensor Networks (WSN), a first prototype was developed. Design challenges as well as simulation results and measurement results of the developed unit are presented.

Chapter 2 – Fundamentals of Power Calculation

The mathematical basics, including the definitions of active power, and apparent power are discussed. Taking into account the sampling theorem, power calculation from a discrete signal is introduced. Among others, this chapter also presents the physical background underlying the Hall effect.

Chapter 3 – System Overview of Power Metering Unit

A description of the current and voltage sensor and the applied transceiver with its programmable protocol processor is presented. A description of the single-wire operation and external wiring of the single-wire communication interface of both is depicted. The sequence used to perform current and external voltage measurement as well as the arising time delay between sensing the current and voltage value are introduced.

Chapter 4 – Hardware Design of Power Metering Unit

The current and voltage sensor presented in chapter 3 has its limitations. Enabling a measurement of line voltage by the sensor, it has to be stepped down using a capacitive voltage divider. An overview of capabilities realizing the required voltage divider with its advantages and drawbacks is given. The chapter gives insight into hardware design issues and implementation details and concludes with simulation results.

Chapter 5 – Software Design of Power Metering Unit

An insight into the designed firmware architecture including an example in the form of a pseudo code is given in this chapter. The transceiver presented in chapter 3 has a very limited language subset of the C compiler. The apparent power calculation demands a way to extract the square root, considering the limitations of the C compiler. Based on the characteristic number representation caused by the division operation, a floating point representation with mantissa and exponent was established. In order to achieve the highest accuracy of the measurements, a cascaded multiplication algorithm was implemented.

Chapter 6 – Measurements with Power Metering Unit

Power metering is performed by sampling over 10 line voltage periods with a sampling rate of $400\,Hz$, leading to eight samples per line voltage period. Using the Gaussian distribution an assessment of accuracy can be determined. 50 measurements were carried out on a $60\,W$ light bulb, resulting in an accuracy of the apparent power of approximately $\pm 4.4\,\%$.

Chapter 7 – Conclusion

Results and findings of this thesis are summarized and a prospective on future work is given in this chapter.

Chapter A – Appendix

In this chapter, among others illustrations of the small Printed Circuit Board (PCB) of the power metering unit as well as the demonstrator are presented. An integration into an LED[1] module which can perform power metering as well as dimming is shown as well.

[1] Light-Emitting diode

Chapter 2

Fundamentals of Power Calculation

This chapter covers the theoretical and mathematical background of power metering using a Hall-based current sensor. Section 2.1 explains the basic principle of Hall-based sensors and the physical background underlying the Hall effect. Section 2.2 gives an overview of the mathematical basics of power metering, the definition of individual powers and how power can be calculated from sinusoidal currents and voltages. The transition from continuous signals to time-discrete signals and the sampling theorem are covered in section 2.3. Furthermore, the calculation of active and accordingly apparent power of digital signals can be found in section 2.4.

2.1 Hall Effect, Hall-based Current Sensor

The Hall effect is a physical phenomenon which was discovered by American physicist E. H. Hall in 1879 as part of his doctoral thesis [Bridgman 1939]. It describes and explains the occurrence of a voltage transversely to the current flow in a current carrying conductor through the action of a perpendicular magnetic field. Further details concerning the Hall effect and its underlying Lorentz force can be found in [Renhart 2011] and [Hoffmann 2002].

The basic physical principle underlying the Hall effect is the Lorentz force, the force acting on moving charged particles due to a magnetic field. The effect is particularly prevalent in semiconductors as a result of the high mobility of charge carriers. A particle of charge $\vec{q}$ with instantaneous velocity $\vec{v}$ experiences a force

$$\vec{F} = q(\vec{E} + \vec{v} \times \vec{B})$$

due to the presence of an electrical field $\vec{E}$ and a magnetic field $\vec{B}$. This relationship is referred to as Lorentz's equation. The first term $q\vec{E}$ is contributed by the electrical field called Coulomb force, describing the action on unmoved charges due to electrical fields. The second term $q(\vec{v} \times \vec{B})$ describes the magnetic force referred to as the Lorentz force,

the force experienced by a moving charge in a magnetic field. Accordingly the magnetic force acting on a moving charge is expressed by the following equation.

$$\vec{F} = q(\vec{v} \times \vec{B}) \tag{2.1}$$

This force has a direction perpendicular to both the velocity of the charge and the magnetic field. [Renhart 2011]

When a current flowing semiconductor plate is laying in an applied magnetic field which is not parallel to the direction of the moving charge carriers, the magnetic force given by equation 2.1 leads to a deflection of these charge carriers. Figure 2.1 illustrates the force on charge carriers in a conductor in a magnetic field.

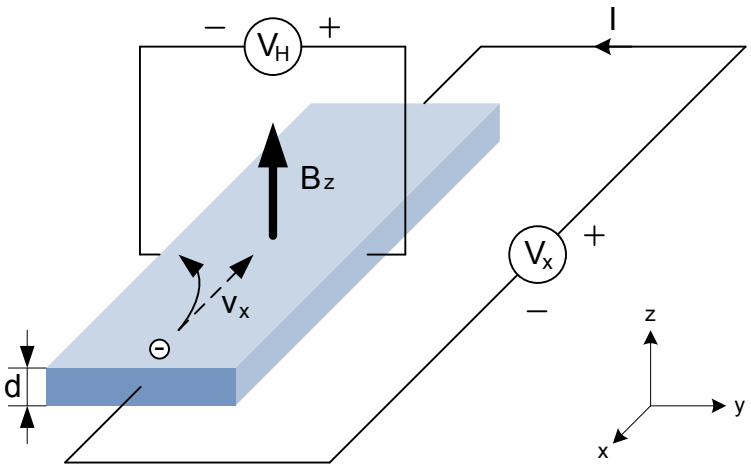


Figure 2.1: Illustration of the Hall Effect
Adapted from [Wikipedia 2012]

As a result charge carriers pile up on one side of the material and deplete from the opposite side. This separation of charge creates an electrical field acting on charge carriers which compensates the effect of the Lorentz force. Accordingly, for the resulting force acting on charge carriers, the following equation has to be applied.

$$0 = q(\vec{E} + \vec{v} \times \vec{B})$$

The separation of charge stops and a steady electrical potential is established, as long as the charge is flowing. This so-called Hall voltage, V_H, that develops across a conductor can be calculated by

$$V_H = c_h \frac{IB}{d}, \tag{2.2}$$

where c_h is the Hall constant, I is the current across the plate, B is the magnetic field, and d is the thickness of the plate. The Hall voltage is directly proportional to the current, to the magnetic field, the nature of the particle conducting material itself, and inversely proportional to the thickness of the material. [Hoffmann 2002]

2.2 Mathematical Basics of Power Metering

An instrument measuring electrical currents is referred to as an ammeter, those instruments measuring electrical voltages are referred to as voltmeters, instruments measuring electrical power are referred to as wattmeters. The principle mode of operation of ammeters, voltmeters and wattmeters is based on the force acting on a current carrying conductor in a magnetic field. Generally both direct quantities and alternating quantities have to be measured. [Brasseur 2004]

Generally power metering is carried out either indirectly by simultaneous measurement of current and voltage or directly by using a active power meter such as a wattmeter for example. As we have a current sensor which is also able to measure voltages, power metering is carried out indirectly. The following sections are describing terms and definitions and how power can be calculated of continuous sinusoidal signals.

2.2.1 Terms and Definitions

In electrical engineering a distinction is made between direct quantities and alternating quantities. Direct quantities are characterized by their temporally constant electrical quantities, for example currents and voltages. Accordingly, the magnetic field, with corresponding magnetic quantities to its connected electrical field, is constant as well. Time variable quantities describing the electromagnetic phenomenon are called alternating quantities. Another distinction is made between the periodic and non-periodic. In this thesis it is assumed that all alternating quantities are periodic quantities. Periodic quantities take the same value in every specific subsequent time segment. [Weißgerber 2013]

Direct (DC) Current and Direct (DC) Voltage

DC current and DC voltage are electrical quantities whose momentary values are constant at all times.

Alternating (AC) Current and Alternating (AC) Voltage

AC current and AC voltage are electrical quantities whose momentary values are repetitive after time segment T, called period, and whose average values are zero. [Hoffmann 2002]

In electrical engineering alternating quantities take on a narrow meaning, as in the physical definition mentioned above. A further distinction is made between sinusoidal and non-sinusoidal quantities. Under the assumption that AC current and AC voltage have a sinusoidal shape, signals can be clearly identified by specifying **peak value**, **frequency** and **phase shift**. Sinusoidal quantities represent a special case in periodic signals. They are not only described as a function in time, but also as a function of angle $\varphi = \omega t$. The transition from the two notations is carried out by multiplying the time axis with the angular frequency ω. Period T on time axis passes into angle $\omega t = 2\pi$ on ωt-axis. [Albach 2005], [Renhart 2011]

Peak Value $\hat{U}$

The peak value of a signal is defined by the maximum deviation from the neutral.

Period T

The time between two points of a signal with the same value is called period. Sinusoidal functions repeat themselves after expiry of an angle of $360\,^\circ$ or $2\pi\,rad$.

Frequency f

The frequency of a signal specifies the number of oscillations from a signal per second. Frequency can be computed by using the reciprocal of the period.

$$f = \frac{1}{T}$$

In addition to these fundamental terms of electrical oscillations, there are other terms describing the physical effects of electrical alternating quantities. For these, it is more expedient to work with terms regardless of the signal shape. [Albach 2005], [Hartl 2008]

Average Value $\bar{U}$

According to its definition, the average value of a time-dependent periodic signal is the integral of the signal over period related to period. The average value of an electrical alternating signal equates to the containing direct component. It is equal to zero for pure sinusoidal quantities, symmetrically with respect to zero level.

$$\bar{U} = \frac{1}{T}\int_{t_0}^{t_0+T} u(t)dt \tag{2.3}$$

Rectified Value $\left|\bar{U}\right|$

The rectified value of a signal is defined as the average value (equation 2.3) of the absolute value of the signal. It describes an intended DC current which transports the same charge as the rectified AC current.

$$\left|\bar{U}\right| = \frac{1}{T}\int_{t_0}^{t_0+T} |u(t)|\,dt$$

For sinusoidal quantities the rectified value can be calculated by

$$\left|\bar{U}\right| = \frac{2}{\pi}\hat{U}.$$

Root Mean Square Value (rms-value)

The square root of the average value of the square of a signal is defined as the root mean square value of a signal. The root mean square value of an AC current or AC voltage causes the same effect on a resistance as a comparable value of DC current or DC voltage causes on the same resistance.

$$U_{eff} = \sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} u^2(t)dt} \tag{2.4}$$

For sinusoidal quantities the root mean square value can be calculated by

$$U_{eff} = \frac{\hat{U}}{\sqrt{2}}. \tag{2.5}$$

The definitions of these two values were shown using the voltage as an example; they were calculated in the same way for currents. With regard to all considerations in connection with powers, rms-values are used. For example, in charge and discharge processes in batteries the transported charge is the crucial factor. In this case, average value or rectified value has to be considered.

As we are subsequently using principally rms-values at alternating quantities, the index $_{eff}$ is omitted, rectified values and average values are marked for distinction. [Hartl 2008]

2.2.2 Power at AC Current Voltage

This section considers linear network stored or consumed power, in cases where the circuit is connected to an AC current voltage source. For the sake of simplicity the network is set up with individual two terminal networks. As the stored or consumed power of the entire network consists of the linear superposition contributed by the individual two terminal networks, the consideration is restricted to one linear two terminal network. At the linear two terminal network, active resistance and reactance are independent of the current through the components. The time dependent quantities are represented generally by equations 2.6.

$$\begin{aligned} u(t) &= \hat{U}\cos(\omega t + \varphi_u) \\ i(t) &= \hat{I}\cos(\omega t + \varphi_i) \end{aligned} \tag{2.6}$$

with angular frequency $\omega = 2\pi f$, phase shift φ_u of voltage and φ_i of current compared to any reference value.

The electrical power is expressed by the product of current and voltage. Consequently, at the time dependent signals $u(t)$ and $i(t)$ as depicted in equation 2.6 the momentary value $p(t)$ of the output power performed at the two terminal network is calculated by

$$p(t) = u(t)i(t) = \hat{U}\hat{I}\cos(\omega t + \varphi_u)\cos(\omega t + \varphi_i).$$

The calculated power can have both positive or negative values, depending on the instant of time. When $p(t) > 0$, the two terminal network absorbs power and is acting as a consumer load, at purely resistive loads the condition is fulfilled at any time. On the other hand, in the event of $p(t) < 0$, the two terminal network delivers power and is acting as a source. This case occurs when reactive power is oscillating between the source and two terminal device.

First of all an examination is made of the special cases, where the two terminal network contains one of the components R, L and C. Later on the results are generalized on a arbitrary composed two terminal network. Due to the fact that the considered two terminal networks do not include a current source or voltage source, they are referred to as passive two terminal networks. The dissipated power time-averaged over an entire period of a passive two terminal network always is greater than or equal to zero. [Albach 2005]

Active Power

At an ohmic resistance, electrical current and voltage are always in phase. Because of the connection $\varphi_i = \varphi_u$, the time-dependent power is composed of a time-independent expression and an expression oscillating with double frequency.

$$p(t) = \hat{U}\hat{I}\cos^2(\omega t + \varphi_u)) = \frac{\hat{U}\hat{I}}{2}\left[1 + \cos(2\omega t + 2\varphi_u)\right] = UI\left[1 + \cos(2\omega t + 2\varphi_u)\right]$$

The result is describing the power dissipated by a resistor, in other words the power converted into heat.

$$p(t) = UI\left[1 + \cos(2\omega t + 2\varphi_u)\right] = UI\left[1 + \cos(2\omega t + 2\varphi_i)\right]$$

Of particular importance is the dissipated time-averaged power on a resistor, referred to as **active power**. By integrating over the entire period, the expression with cosine function resolves, leaving the time-independent expression.

$$P = \frac{1}{T}\int_{t_0}^{t_0+T} p(t)dt \tag{2.7}$$

With pure ohmic resistance, the active power is calculated by the product of the rms-value of current and voltage. [Albach 2005]

$$P = \frac{1}{T}\int_{t_0}^{t_0+T} p(t)dt = UI$$

Reactive Power

At an inductance the current is lagging behind the voltage by $\pi/2$. With the existing phase relationship $\varphi_i = \varphi_u - \pi/2$ and by means of addition theorems the time-dependent power can be described with the following equation.

$$\begin{aligned} p(t) &= \hat{U}\hat{I}\cos(\omega t + \varphi_u)\cos(\omega t + \varphi_u - \pi/2) = \hat{U}\hat{I}\cos(\omega t + \varphi_u)\sin(\omega t + \varphi_u) \\ &= \frac{\hat{U}\hat{I}}{2}\sin(2\omega t + 2\varphi_u) = UI\sin(2\omega t + 2\varphi_u) = -UI\sin(2\omega t + 2\varphi_i) \end{aligned} \tag{2.8}$$

The resultant power just consists of the expression oscillating with double frequency, the average value disappears. This back and forth oscillation of the power is referred to as **reactive power**.

At capacitance the conditions are similar to the inductance. In that case the current is leading the voltage by $\pi/2$. Accordingly, the sign of current and therefore the time-depending power is changing.

$$p(t) = -UI\sin(2\omega t + 2\varphi_u) = UI\sin(2\omega t + 2\varphi_i) \tag{2.9}$$

In principle, no losses occur during the energy exchange between the AC current voltage source and inductance, and accordingly capacitance. The energy temporarily extracted from the source is used for building up the magnetic field and the electrical field, respectively. On the other side, by decreasing the field energy is returned to the source. [Albach 2005]

Apparent Power and Power Factor

Having discussed special cases with only one component, now the two terminal network is composed of any combination of the components R, L and C. This means the phase shift between current and voltage can take any value in a range of $-\pi/2 \leq (\varphi_u - \varphi_i) \leq +\pi/2$. By means of addition theorems the time-dependent power is rearranged to

$$\begin{aligned} p(t) &= \hat{U}\hat{I}\cos(\omega t + \varphi_u)\cos(\omega t + \varphi_i) = \frac{\hat{U}\hat{I}}{2}\left[\cos(\varphi_u - \varphi_i) + \cos(2\omega t + \varphi_u + \varphi_i)\right] \\ &= UI\cos(\varphi_u - \varphi_i) + UI\cos(2\omega t + \varphi_u + \varphi_i). \end{aligned}$$

In this as well case the time-dependent power is comprised of a time-independent expression and an expression oscillating with double frequency. A further conversion of the oscillating expression

$$\begin{aligned}\cos(2\omega t + \varphi_u + \varphi_i) &= \cos\left[(2\omega t + 2\varphi_u) - (\varphi_u - \varphi_i)\right] \\ &= \cos(2\omega t + 2\varphi_u)\cos(\varphi_u - \varphi_i) + \sin(2\omega t + 2\varphi_u)\sin(\varphi_u - \varphi_i)\end{aligned}$$

leads to a first representation of the momentary power

$$p(t) = UI\cos(\varphi_u - \varphi_i)\left[1 + \cos(2\omega t + 2\varphi_u)\right] + UI\sin(\varphi_u - \varphi_i)\sin(2\omega t + 2\varphi_u), \qquad (2.10)$$

where the argument of the time-dependent functions includes only the phase shift of the voltage φ_u. In the same way a transformation of the expression oscillating with double frequency

$$\begin{aligned}\cos(2\omega t + \varphi_u + \varphi_i) &= \cos\left[(2\omega t + 2\varphi_i) + (\varphi_u - \varphi_i)\right] \\ &= \cos(2\omega t + 2\varphi_i)\cos(\varphi_u - \varphi_i) + \sin(2\omega t + 2\varphi_i)\sin(\varphi_u - \varphi_i)\end{aligned}$$

yields a second representation of the momentary power

$$p(t) = UI\cos(\varphi_u - \varphi_i)\left[1 + \cos(2\omega t + 2\varphi_i)\right] - UI\sin(\varphi_u - \varphi_i)\sin(2\omega t + 2\varphi_i), \qquad (2.11)$$

where the argument of the time-dependent functions includes only the phase shift of the current φ_i.

Setting the phase shift between current and voltage to zero, $\varphi_u - \varphi_i = 0$, due to the relation $cos(0) = 1$ the first summand in both equation 2.10 and equation 2.11 corresponds to the momentary active power and the second summand resolves. In the other case, where current and voltage are shifted by $\pm\pi/2$, the first summand drops out and the second summand simplifies to equation 2.8 with inductors and equation 2.9 with capacitors, respectively. Obviously the fist summand in equation 2.10 and equation 2.11 is describing the momentary power percentage irreversibly transformed into another form of energy (heat) corresponding to the active power, while the second summand is describing the momentary power percentage responsible for the changing of the stored energy in the magnetic field, and accordingly in the electrical field corresponding to the reactive power.

In general, at a linear two terminal network with current and voltage according to relation 2.6 and phase shift between these quantities in a range of $-\pi/2 \leq (\varphi_u - \varphi_i) \leq +\pi/2$, the active power given by equation 2.3 can be calculated by integration of the expressions

2.10 and 2.11 over an entire period. Due to trigonometric identity $\cos\varphi = \cos -\varphi$ the value of the active power is independent of whether the current leads or lags.

$$P = UI\cos(\varphi_u - \varphi_i)$$

Consequently the active power is dependent on both the amplitude of current and voltage and the phase shift between these quantities. The coefficient $\cos(\varphi_u - \varphi_i)$ is typically abbreviated with $\lambda = \cos(\varphi_u - \varphi_i)$ and referred to as **power factor**. When the two terminal network only consists of ohmic resistances, the relation $\varphi_u = \varphi_i$ applies and the power factor contains the value $\lambda = \cos(0) = 1$. At pure reactances the phase shift is given by $\varphi_u - \varphi_i = \pm\pi/2$ and $\lambda = \cos(\pm\pi/2) = 0$ then applies for the power factor. Based on the definition of active power, the amplitude of the second summand

$$Q = UI\sin(\varphi_u - \varphi_i)$$

is referred to as **reactive power**. Therefore the active power at two terminal networks, consisting of the components R, L and C, is always taking positive values. The reactive power is accordingly reaching both positive and negative values, depending on whether the two terminal network is acting inductively or capacitively and the current is leading or lagging the voltage.

Viewing these powers as a vector diagram, the catheti correspond to the active power and the reactive power. The hypotenuse

$$S = UI = \sqrt{P^2 + Q^2} \tag{2.12}$$

is referred to as **apparent power**. Accordingly the apparent power is given by the vector product of active power and reactive power or by multiplying the rms-values of current and voltage, disregarding the power factor. The term is associated with the fact that it represents no power in the physical sense, as current and voltage occur in various instants of time.

With this definition the power factor can be calculated by the ratio of active power and apparent power.

$$\lambda = \cos(\varphi_u - \varphi_i) = \frac{P}{S}$$

The units for powers P, Q and S always result from the product of $[U] \cdot [I] = V \cdot A$. Instead of Watt (W) as it is used for active power, Volt-ampere reactive (Var) is used for reactive power and Volt-ampere (VA) for apparent power. [Albach 2005]

2.3 Sampling and Quantization

Generally, in analog electronics, continuous quantities were processed. In modern digital electronics these continuous quantities have been discretized; in other words they can only take specified values and accordingly they are only defined at specified instants of time. In digital processing these discrete signals are now used for computing. Accordingly there are four different possible types of time signals, depending on whether the discretization is carried out in the time domain or in the value domain. The continuous parameter t is replaced by an integer index variable k. A digital signal is discretized in the time domain referred to as sampling as well as in the value domain referred to as quantization and can be described with integer values. [Hartl 2008]

2.3.1 Sampling of Continuous Signals, Sampling Theorem

Discretization in the time domain means that a signal is sampled at a specified, exactly defined instant of time. In other words a continuous signal $x(t)$ can be converted into a sequence of discrete values x_k by taking samples of the signal in equidistant instants of time $t_k = kT_s$.

$$x_k = x(kT_s), \text{ for } k \epsilon \mathbb{Z}$$

with T_s referring to as sampling interval. The information on the signal sequence between the specific sampling points will get lost. If the signal is sampled often enough, then no loss of information occurs at discretization in the time domain leading to the sampling theorem. [Brasseur 2004], [Hartl 2008]

Sampling Theorem

The theoretical foundations for a discretization in the time domain are given by the following sampling theorem. By sampling a continuous signal, the signal is discretized in the time domain.

$$x(t) \longrightarrow x_k, \text{ for } k \epsilon \mathbb{Z}$$

This is carried out with the sampling rate f_s, the reciprocal of sampling interval T_s. Afterwards, the value of the signal is only known at specified, exactly defined instants of time.

The sampling theorem states that, if a continuous band-limited signal is sampled with at least twice the highest frequency f_{max} of the signal, then at discretization in the time domain no loss of information occurs and the signal can be reconstructed completely.

$$f_s > 2f_{max} \tag{2.13}$$

Sampling Theorem

Violating the sampling theorem, referred to as undersampling, leads to loss of information as well as seemingly occurring components in the time-discrete signal referred to as aliasing. [Hartl 2008]

2.3.2 Quantization in Value Domain

A quantization in the value domain means that the signal value can be described with integer values. For that, the amplitude range is divided into equal intervals, referred to as quantizing intervals, and each interval is assigned to a value. After conversion into the binary system, the signal value can be represented by multiple bivalent variables independent of the range of values, referred to as encoding.

Further details concerning the quantizing intervals and the binary representation of the current and voltage values are given in section 3.2. A closer look at discretization in the time domain as well as in the value domain and the sampling theorem can be found in [Hartl 2008] and [Brasseur 2004].

2.4 Power Calculation from a Digital Signal

This thesis deals with the subject of power measurement of any of the loads connected to the line voltage concerning active power and apparent power. The rms-value of the line voltage is $230\,V$. It is assumed that the grid provides a continuous pure sinusoidal quantity with its maximum frequency of $f_{max} = 50\,Hz$. As can be seen from section 2.2.2, power measurement can be done indirectly by simultaneous measurement of current and voltage. Timer-averaged power converted in the load is referred to as active power and can be expressed by equation 2.7. Referring to equation 2.12, apparent power can be calculated by multiplying the rms-values of current and voltage. This leads to the following equations for continuous signals.

$$P = \frac{1}{T}\int_{t_0}^{t_0+T} p(t)dt = \frac{1}{T}\int_{t_0}^{t_0+T} u(t)i(t)dt \tag{2.14}$$

$$S = UI = \frac{1}{T}\sqrt{\int_{t_0}^{t_0+T} u^2(t)dt \int_{t_0}^{t_0+T} i^2(t)dt} \tag{2.15}$$

Concerning the definition of an integral by Riemann sums, a definite integral can be defined as the area between the x-axis and the graph of a function. Choose a real-valued function $f(x)$ which is defined on the interval $[a, b]$. For the purpose of describing an integral as a sum, the interval is subdivided into n partial intervals. In the limit of $n \to \infty$ the sum of the individual areas describes exactly the area under the curve. In conclusion the definite integral of the function is equal to the limiting value of the sum of all rectangular areas

under the curve. The signed area under all the rectangles is referred to as the Riemann sum.

$$\int_a^b f(x)dx = \lim_{n\to\infty} \sum_{k=1}^{n} f(x_k)\Delta x, \text{ for } \Delta x = \frac{b-a}{n}$$

Decreasing the spacing between the samples and accordingly increasing the amount of partial intervals, the total area of the rectangles converges to the integral of the function.

By sampling the continuous quantities current $i(t)$ and voltage $u(t)$ with a frequency of $fs = 400\,Hz$, the signal value at each sampling point is assigned to the corresponding quantizing interval and depicted as a binary value. According to this, current and voltage are converted into a sequence of discrete values u_k and i_k.

$$u(t) \longrightarrow u_k, \text{ for } k \,\epsilon\, \mathbb{Z}$$

$$i(t) \longrightarrow i_k, \text{ for } k \,\epsilon\, \mathbb{Z}$$

Considering the sampling theorem in equation 2.13, the requirement of sampling with at least twice the highest frequency of the signal is satisfied. From these digital signals u_k and i_k, which are discretized in the time domain and the value domain, active power and apparent power can be calculated by equation 2.16 and equation 2.17.

$$P = \frac{1}{n} \sum_{k=1}^{n} u_k i_k \tag{2.16}$$

$$S = \frac{1}{n} \sqrt{\sum_{k=1}^{n} u_k^2 \sum_{k=1}^{n} i_k^2} \tag{2.17}$$

Chapter 3

System Overview of Power Metering Unit

In this chapter an overview of used hardware which was made available is presented. A description of the main building blocks of the system is given in section 3.1. Section 3.2 refers to the test chip of the high-precision digital current sensor TLI4970, concerning its application for external voltage, current measurement and single-wire connection and operation. A short description of the multi-channel transceiver ASIC and the containing protocol processor can be found in section 3.3.

3.1 System Architecture

The developed power metering unit measures the power consumption in single-phase systems as part of a WSN. This wireless digital communication system operates in the Industrial, Scientific and Medical (ISM) radio bands. The term communication is always linked with the transport process of information from one point (the information source) to another (the destination or sink). The transmission medium (the channel) illustrates the physical medium over which the modulated information signal is transmitted. While wired channels imply the requirement of a direct connection in the form of a wire (copper, fiberglass etc.) between sending and receiving units to transmit information, wireless transmission channels rely on the effect of wave propagation over free space. [Proakis and Salehi 2004], [Finkenzeller 2010]

ISM bands are referred to as frequency ranges used for industrial, scientific and medical applications. ISM frequency ranges are internationally reserved for applications using High Frequency (HF) devices. The wave propagation in this Ultra-High Frequency (UHF) frequency range is quasi-optical. Buildings and other obstacles cause a strong dampening and reflection of the incident electromagnetic wave. The frequency range $868\,MHz$ up to

$870\,MHz$ has been available for Short-Range Devices (SRDs) in Europe since the end of 1997. [Finkenzeller 2010]

The basic block diagram of the power metering unit is shown in figure 3.1. Power metering discussed in this thesis is carried out indirectly by current and voltage measurement. The main building blocks of the unit are the so-called matching network, the current and voltage sensor, a protocol processor and a transceiver (TRX) front end. The main task of the protocol processor is to stand-alone handle the radio communication protocols (MAC protocols) with a base station or gateway. This proprietary radio communication protocol will not be covered in this thesis.

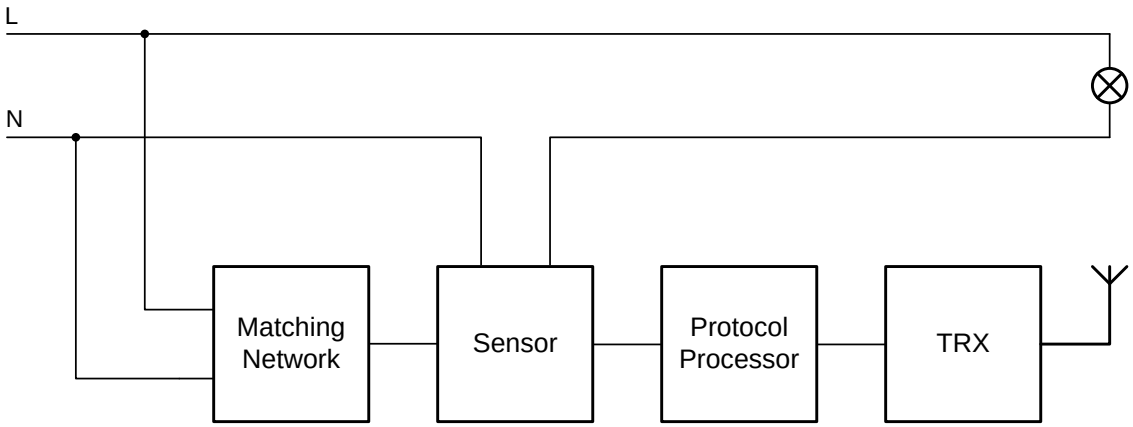


Figure 3.1: Basic Block Diagram of the Power Metering Unit

The so-called matching network is required to comply with characteristics required for external voltage measurement. Because the sensor has its limitations on the external voltage Analog to Digital Converter (ADC) input, the line voltage to be measured has to be stepped down using a voltage divider. Thus, the external voltage ADC input is able to measure an single-ended voltage with respect to GND[1]; the stepped down voltage is amplified by an instrumentation amplifier and fed into the external voltage ADC input. The voltage measured by the ADC is multiplied by firmware with a constant factor in order to correspond to the line voltage. A detailed description concerning the matching network and the instrumentation amplifier can be found in chapter 4.

[1] Ground

In order to perform current and voltage measurement, a test chip of the digital current sensor TLI4970 is used. In addition to current measurement, the test chip is also able to measure external voltages by the DOUT[2] pin. Single-wire communication between the sensor and the transceiver is carried out by the FOC[3] pin.

The entire controlling functionality is taken over by the protocol processor, consisting of a programmable state machine and Random Access Memory (RAM) for saving configurations. In addition to its main task of stand-alone handling the radio communication protocols, the protocol processor is also used to sequentially control the single-wire communication with the sensor as well as the calculation of the desired power ratings. Thus, the transceiver is supporting both three-wire SPI and four-wire SPI; single-wire communication with the sensor is carried out by connecting the FW_SDO[4] pin and the FW_SDI[5] of the SPI module. More information about the single-wire communication interface is given in figure 3.5 and in section 3.3.4.

As a result of the capacitive voltage divider used and its characteristics, the entire power metering unit must be operated as floating. The unit can be supplied either by batteries or by a potential-free (floating) voltage source. More details concerning the capacitive voltage divider can be found in section 4.2.

3.2 Current and Voltage Sensor, Test Chip of the TLI4970

The TLI4970 is a high-precision miniature coreless magnetic current sensor based on Infineon's well-established Hall technology, allowing galvanic isolation between the primary (current rail) and the secondary (interface to control unit) side. Using a coreless concept without a flux concentrator allows significant miniaturization and shows no hysteresis effects. As a result of the differential measurement principle and the implemented stray field suppression, the TLI4970 is extremely robust against external magnetic fields. There is no need for any external calibration of the sensor in manufacturing nor during application. The functionality of the TLI4970 is comparable to open- or closed-loop current measurement systems with a magnetic core, but enables a significantly smaller footprint (illustrated in figure 3.2) and consumes less power. [Technologies 2011d]

The implementation of digital temperature and stress compensation provides outstanding long-term stability of the output signal. Compared to a shunt resistor, for current measurements using the Hall effect there is no resistor immersed into the primary circuit and accordingly no voltage drop happens nor is there any power lost. [Technologies 2011d]

[2] SPI Data Out
[3] Fast Overcurrent Detection Output
[4] Serial Data Out
[5] Serial Data In

Due to the digital concept, there is no need for any external calibration and additional parts such as ADCs, operational amplifier (op-amps) or reference voltage, reducing the overall implementation effort, PCB space and cost significantly. The TLI4970 is suitable for AC as well as DC current measurement applications such as photovoltaic inverters, Power Factor Correction (PFC) power supplies, chargers and drivers. The contact-free measurement principle causes no additional power loss and is therefore perfectly suited for systems with high efficiency. It is also suitable for fast overcurrent detection with a configurable threshold level, allowing the control unit to switch off and protect the affected system from damage, independently of the main measurement path. [Technologies 2011d]

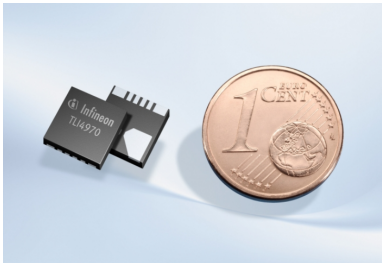


Figure 3.2: Sensor in Comparison with 1 Cent Coin
[Mann 2012]

In addition to the current measurement, the test chip of the TLI4970 is also able to perform external voltage measurement on the DOUT pin against GND, which is normally used to carry out three-wire Serial Peripheral Interface (SPI) communication. This is done by using the second internal Sigma-Delta-ADC; in conventional operation this ADC is used for temperature and stress compensation.

3.2.1 Pin Configuration

Pin configuration and description of the sensor in order to perform current and external voltage measurement are depicted in figure 3.3 and table 3.1.

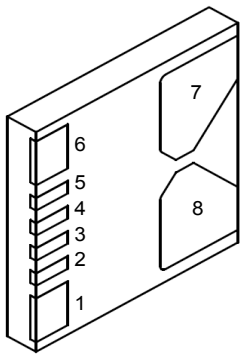


Figure 3.3: Pin Configuration PG-TISON-8-1
[Technologies 2011d]

Pin No.	Symbol	Function
1	GND	Ground
2	VDD	Supply voltage
3	DOUT	**External voltage ADC input**
4	SCLK	Serial clock input
5	CS	Chip select input (low-active)
6	FOC	**Single-wire communication interface**
7	IP+	Positive current terminal pin (current-in)
8	IP-	Negative current terminal pin (current-out)

Table 3.1: Pin Definition and Function
Adapted from [Technologies 2011d]

3.2.2 Functional Description

"The current flowing through the current rail on the primary side induces a magnetic field, which is measured by two differential Hall probes. The signal from the two Hall probes is directly digitized by a Sigma-Delta-ADC. After the programmable digital low-pass filter, the raw current signal is fed into the Digital Signal Processor (DSP). The differential measurement principle of the magnetic field provides a very good suppression of any ambient stray magnetic field." [Technologies 2011d]

"The temperature (T) and the mechanical stress (S) of the chip are measured and converted independently of the primary current by a second ADC. The DSP unit uses both temperature and stress information to compensate the raw current signal according to internally stored calibration tables." [Technologies 2011d]

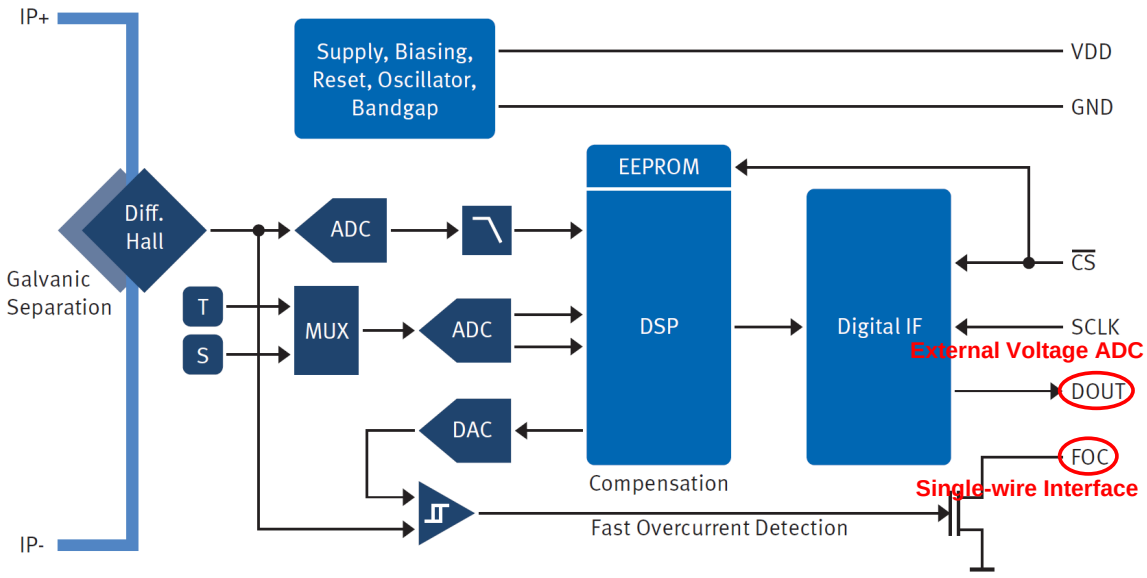


Figure 3.4: Functional Block Diagram of the Current and Voltage Sensor
Adapted from [Technologies 2012a]

In addition, the test chip of TLI4970 is able to perform an external voltage measurement on the DOUT pin. In order to to perform this feature the test chip of TLI4970 has to be switched in a so-called "test" mode. The signal applied on the DOUT pin is digitized by the second Sigma-Delta-ADC; in conventional operation this ADC is used for temperature and stress compensation. The digital interface unit (IF) transmits the fully compensated current value and accordingly the voltage value by the single-wire communication interface available on the FOC pin; in conventional operation this pin is used to detect an overcurrent in the measurement path.

3.2.3 Single-wire Connection and Operation

This interface is used to read out the measured current and voltage values as required for power metering used in this thesis. It is available and always functional on the FOC pin using a pull-up resistor of $4.7\,k\Omega$ illustrated in figure 3.5. [Technologies 2011b]

The transmission is based on transmitting a single bit to the sensor and immediately receiving a bit. These bits form a 16 bit communication similar to a SPI interface. The interface is bit-synchronous and very flexible in timing within quite large boundaries. Sensor and Protocol Processing Unit (PPU) must use an open-drain output, so they can actively pull only a $0\,V$ level. The $3.3\,V$ level is achieved by an external pull-up resistor, about $4.7\,k\Omega$ or larger.

Sequential control of the single-wire communication with the sensor is taken over by the protocol processor generating the requested timing. Timing is implemented in firmware, resulting in a possible bit transmission rate of $143\,\frac{kbit}{s}$. Consequently, the required time for the transmission of 16 bit takes $112\,\mu$s.

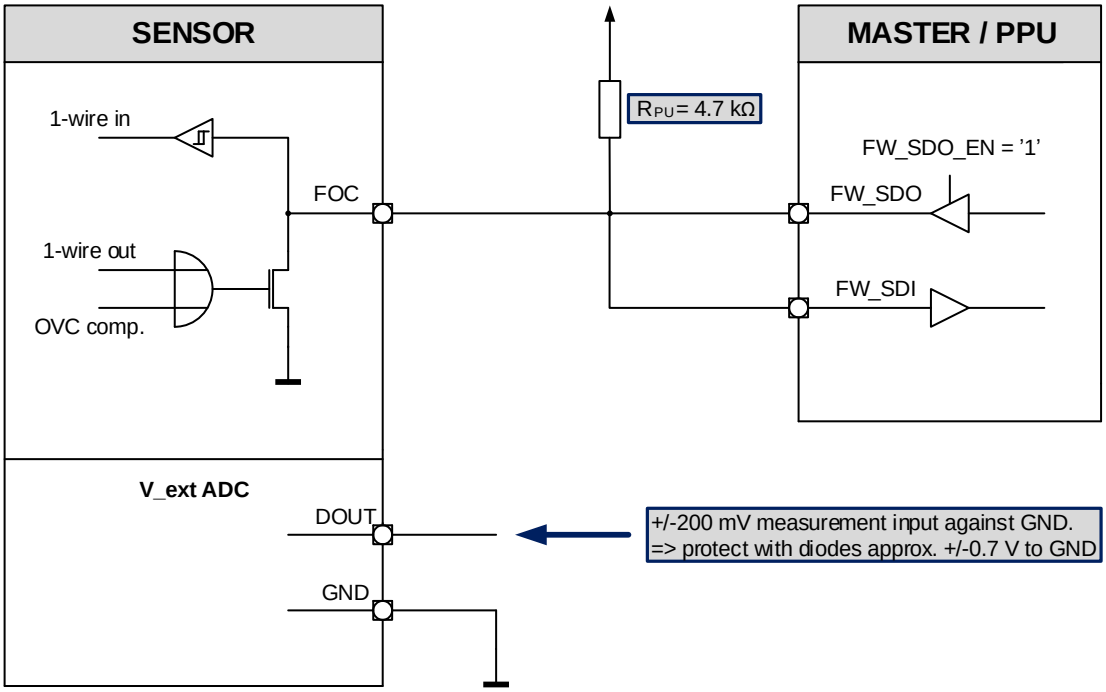


Figure 3.5: Single-wire Connection of the Current and Voltage Sensor
Adapted from [Technologies 2011b]

3.2.4 Flowchart for Current and Voltage Measurement by Single-wire

Figure 3.6 basically illustrates the sequence used to perform current and external voltage measurement, obtaining one value of current and the corresponding voltage. After the voltage value has been read out the system waits until the next current value read-out, to get an integer number of samples within a period of the line voltage. This pause is used to perform the on-the-fly power calculation. More details concerning the on-the-fly calculation can be found in section 5.1.

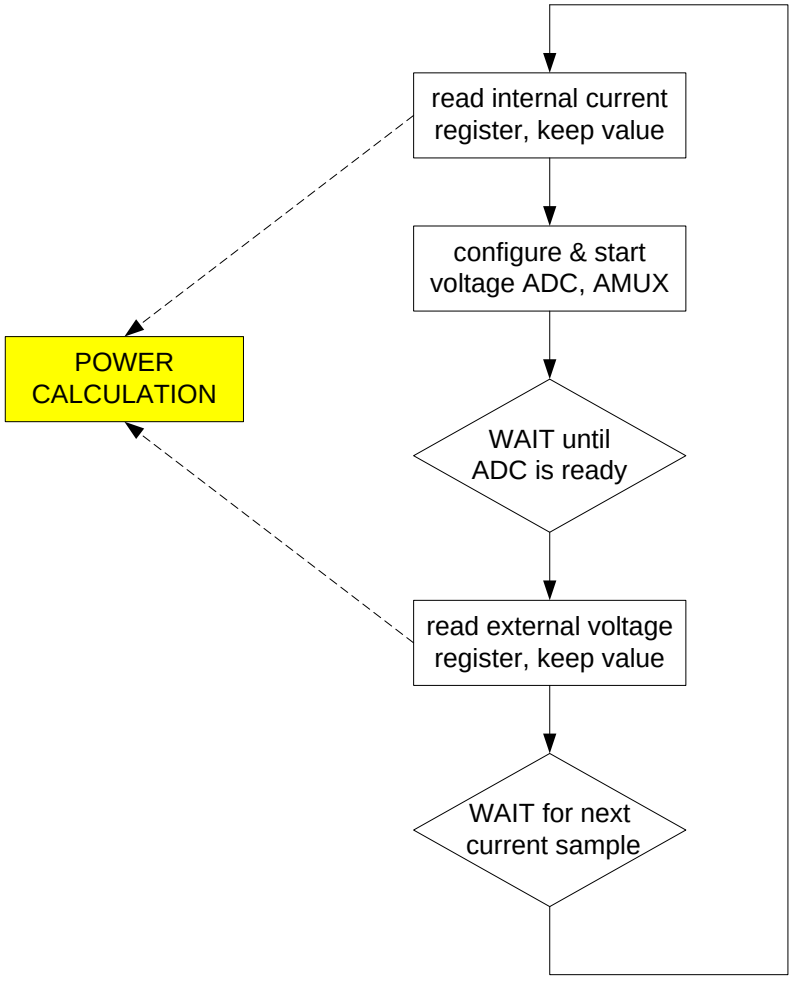


Figure 3.6: Current and Voltage Measurement Sequence

Read Internal Current Register, "1"

A current register read-out is executed by transmitting the appropriate commands. Thus, the single-wire communication is based on transmitting a single bit and immediately receiving a bit, the second command is used to set the sensor in a so-called "freeze" state and simultaneously receive the updated current value. To ensure that the signal processing activities do not interfere with test activities, the internal algorithm processing can be frozen. In this mode the ADCs are still functional and update its data, but the compensation algorithm is no longer executed.

Configure and Start Voltage ADC, "2"

In this block certain configurations were executed in order to perform external voltage measurement on the DOUT pin, followed by a pause until the external voltage ADC is ready. These configurations include:

- Enable "test" mode
- Enable Analog Multiplexer (AMUX) operation on DOUT
- Enable "low common" mode
- Enable "input" mode on DOUT
- Enable ADC channel

Read External Voltage Register, "3"

An external voltage register read-out is executed by transmitting appropriate commands alike. The last "unfreeze" command starts algorithm processing again and simultaneously saves the updated voltage value.

Power Calculation, "4"

The last command of the sequence is followed by a pause until the next current value read-out, used to perform power calculation. Calculating one value of active power and apparent power takes about $500\,\mu s$. After a time of $2.5\,ms$ the sequence repeats itself again, eight times within a period of the line voltage.

Figure 3.7 shows the same sequence used to perform current and external voltage measurement with a bit transmission of $143\,\frac{kbit}{s}$. As can be seen from figure 3.7 the sequence is repeated every $2.5\,ms$; the outcome of this is a sampling rate of $400\,Hz$.

Note that due to the time delay of approximately $1.8\,ms$ between sensing the current and voltage values a virtual phase shift is introduced into the calculation of real and apparent power ratings. Further details are discussed in chapter 6.

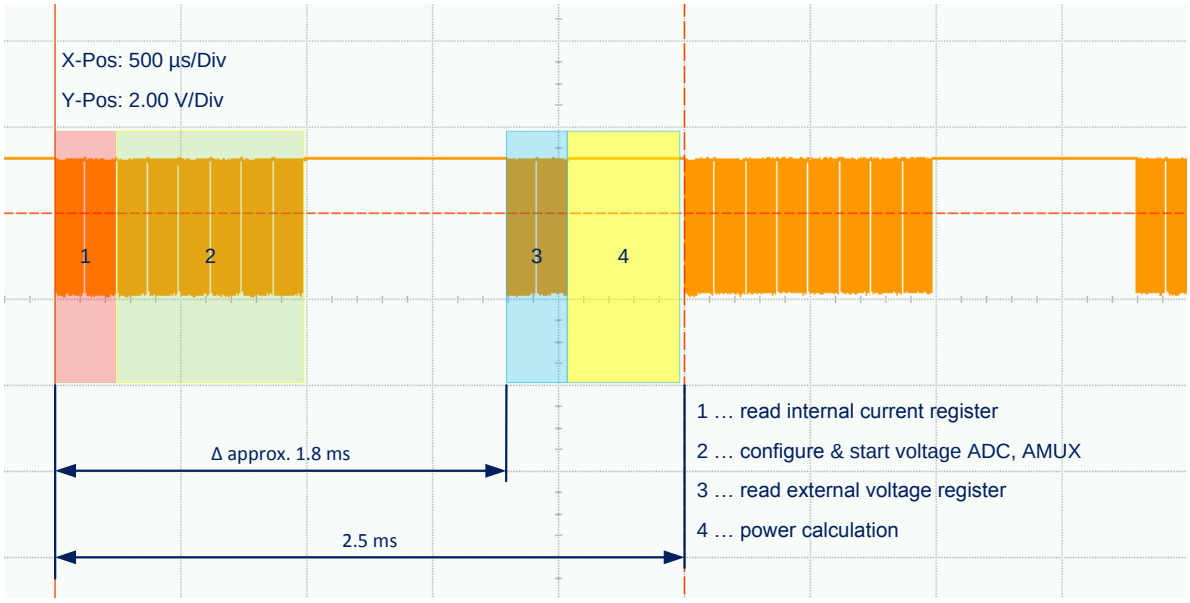


Figure 3.7: Captured Current and Voltage Measurement Sequence

3.2.5 Mapping of the Current Value

As mentioned before, the single-wire transmission form a 16 bit communication, but the value read from the internal current output register has two more Least Significant Bits (LSBs). After a data read from the internal current output register, the value thus has to be shifted 2 bits to the right to scale it similarly to table 3.2. [Technologies 2011b]

Primary current value	**Typical decimal current value (16 bit signed)**	**Note**
+50 A	4000	Maximum allowed limit
+20 A	1600	
+5 A	400	
0 A	0	Zero-point
-5 A	-400	
-20 A	-1600	
-50 A	-4000	Minimum allowed limit

Table 3.2: Relationship between Analog Current Value and its Internal Binary Representation [Technologies 2011b]

3.2.6 Mapping of the Voltage Value

The binary representation of the external voltage value is given in table 3.3.

External voltage value	**Typical decimal current value (16 bit unsigned)**	**Note**
+0.2 V	45667	Maximum allowed limit
+0.1 V	39000	
0 V	32333	Zero-point
-0.1 V	25666	
-0.2 V	18999	Minimum allowed limit

Table 3.3: Relationship between Analog Voltage Value and its Internal Binary Representation [Technologies 2011b]

3.2.7 Electrical Characteristics

Electrical characteristics of the current and voltage sensor are given in table 3.4. Note that because the line voltage has to be stepped down using a voltage divider, the sensitivity of the voltage values are specified to the full-scale voltage measurement range of $\pm 200\,mV$.

Parameter	**Value**			**Unit**
	Min.	Typ.	Max.	
Supply voltage	3.1	3.3	3.5	V
Current consumption	5	12	25	mA
Full-scale primary current measurement range	-50		+50	A
Update rate		80		kS/s
Sensitivity of current value		12.5		mA/LSB
Full-scale voltage measurement range	-200		+200	mV
Update rate		1.2		kS/s
Sensitivity of voltage value		15		μV/LSB

Table 3.4: Electrical Characteristics of the Sensor Adapted from [Technologies 2011d]

3.3 Multi-channel Transceiver, *CHOSeN SmartTransceiver*

The multi-channel transceiver ASIC is a System On Chip (SOC) outcome of the project CHOSeN[6]. Main objective of the project CHOSeN project was to develop application-specific adaptable communication technologies using smart wireless sensor networks in application fields like the automotive and the aeronautic. The CHOSeN SmartTransceiver is enabling a wireless communication interface of a low power sensor node in order to establish a cooperative and heterogeneous sensor network. [FP7 a]

3.3.1 Overview

The ASIC is a low power Amplitude Shift Keying (ASK) and Frequency Shift Keying (FSK) transceiver for low data rate communication in the sub $1\,GHz$ frequency bands. For SRDs the frequency range of $868\,MHz$ up to $870\,MHz$ has been available. A basic block diagram of the multi-channel transceiver is shown in figure 3.8. The main building blocks of the transceiver are the receiver (RX) and transmission (TX) front end, the digital baseband unit, the protocol processor, and the Power Management Unit (PMU). A quartz crystal is used for generating the reference frequency, and optionally an external ceramic filter can be used to improve the robustness and sensitivity of the receiver. The matching network of the transceiver is off-chip and can also include an interface for a wake-up receiver. [Technologies 2011a]

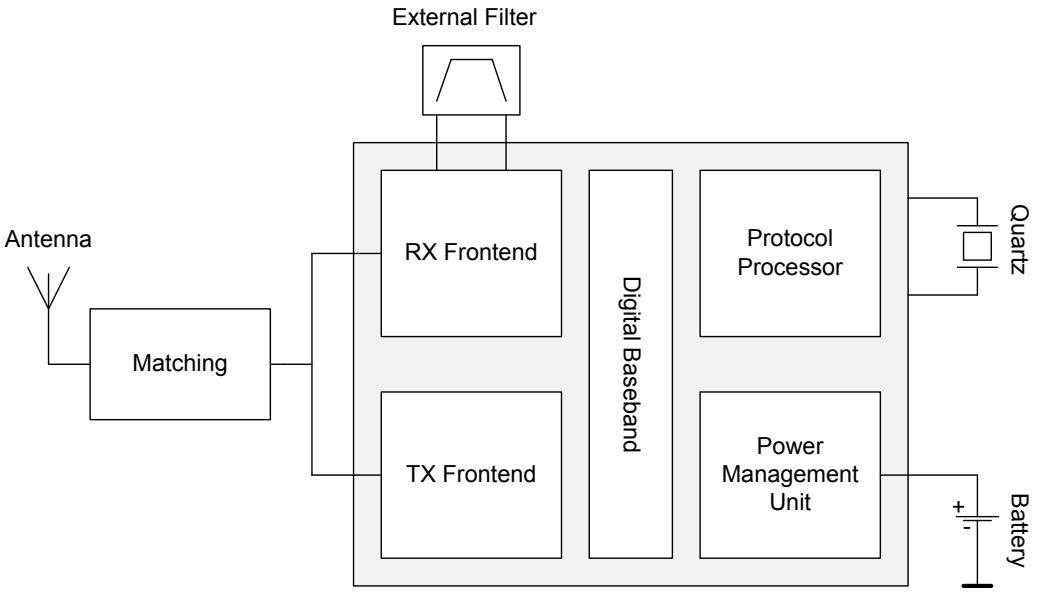


Figure 3.8: Block Diagram of the Transceiver [Technologies 2011a]

[6] EU Project within the 7th Framework Program (ICT-2007-224327)

Because the main objective of the thesis is the development of a low power metering unit of small feature size for line voltage devices further sections elaborate blocks which are relevant for this application, like the protocol processor including used modules and the power management unit. Analog receiver and transmission front end as well as the digital baseband unit are based on the TDA5340 developed by Infineon Technologies AG [Technologies 2011c]. Details and the external wiring of the matching network can be found in the manual [Technologies 2012b].

3.3.2 Protocol Processor

The protocol processor consists of a programmable state machine and RAM for saving configurations. The state machine is a small Application-Specific Instruction-set Processor (ASIP), designed as a Reduced Instruction-Set Computer (RISC). It can be programmed in a very limited *C* subset that can be translated into machine code by a special compiler. The data path width also used for receiving and transmitting is 16 bit. [Technologies 2011a], [Technologies 2011c]

Program Memory

This architecture contains eight physical Read-Only Memory (ROM) pages each containing 2048 instructions, directly addressable by the state machine through its program memory addressing output. Accordingly there are 16 kWords ROM available. Switching between these external ROM pages is done explicitly using a so-called Dynamic Interrupt Vector Table (DIVT) module. This can be done by either jumping into the vector table or by switching into low power modes and waking up upon specific interrupts. [Technologies 2011c]

Data Memory

The state machine can address a memory space of 512 words directly. The address space contains the Special Function Registers (SFRs) and two Static RAM (SRAM) blocks. The SFRs are used to control the peripheral modules and the front-end modules as well as to transport data. The SRAM blocks keep the channel configuration, the data First In, First Outs (FIFOs) and general purpose sections.

The General Purpose RAM (GPRAM) is a 128×16 bit SRAM cell located in the protocol processor domain. It is basically intended to be used for the transmit and receive data FIFOs as well as for general purpose variables required during state machine firmware processing. In this thesis the GPRAM is used for power calculation. [Technologies 2011c]

General Purpose Timer Modules

In the protocol processor there are three general purpose timers (Timer 0 to 2) available. The timer module implements a cyclic downward counter. After a new pre-load value has been written into the timer pre-load SFR T<n>PRE the timer starts decrementing the internal counter value with each positive pulse of the tick signal from the prescaler module. After the internal counter has reached zero it is re-loaded with the pre-load value and the timer starts over again. The internal counter value is accessible in the SFR T<n>VAL. In this thesis the timer is used to control the sequence for current and voltage measurement sequence, as mentioned in section 3.2.4. [Technologies 2011c]

PWM Timer Module

The Pulse Width Modulation (PWM) timer module implements a cyclic downward counter. After a new pre-load value has been written into the timer pre-load SFR T3PRE the timer starts decrementing the internal counter value with each positive pulse of the tick signal from the prescaler module. After the internal counter has reached zero it is re-loaded with the pre-load value and the timer starts over again. The internal counter value is accessible in the SFR T3VAL. The PWM functionality can be explicitly enabled by activating the PWM_EN field within the SFR T3C field. The PWM output clock signal of the PWM timer can be assigned to the general purpose output ports PP0 to PP3. The configuration of the output ports has to be done by configuring the PPCFG and PP2CFG SFR. [Technologies 2011c]

If the PWM functionality is disabled, the clock signal has a fixed duty cycle of $50\,\%$, starting with a logic high value when the timer counters are at the pre-load value. In this mode the PWM timer can be used as additional general purpose timer. In PWM mode the duty cycle can be varied by the SFR T3PWM. In case of `0 < T3PWM < T3PRE` the duty cycle varies linearly with the PWM compare value in the SFR T3PWM. The PWM timer module is used to control the single-wire communication to the sensor, as mentioned in section 3.2.3.

3.3.3 Power Management Unit

"Wireless sensor networks become more and more attractive due to their ongoing miniaturization and therefore decreasing costs. One of the major challenges concerning the design is the power consumption of the wireless sensor node. Low power consumption is mandatory to guarantee a long lifetime if a battery is used as a power source or to allow the use of an energy harvester. In this work a multi-stage power management for a wireless sensor node is presented. Energy-efficient power management is achieved by employing several state machines controlling different power domains which can be turned on and off separately depending on the operating mode of the wireless sensor node." [Unterassinger 2008]

The functionality of the transceiver is based on an innovative concept of a flexible power management unit to reduce power consumption in standby modes. The whole power management concept relies on a three-stage interaction concept of analog and digital control units, separated into different power and clock domains. Each stage has a finite-state machine controlling circuitry for its corresponding system state. An overview is given in figure 3.9. [Technologies 2011c]

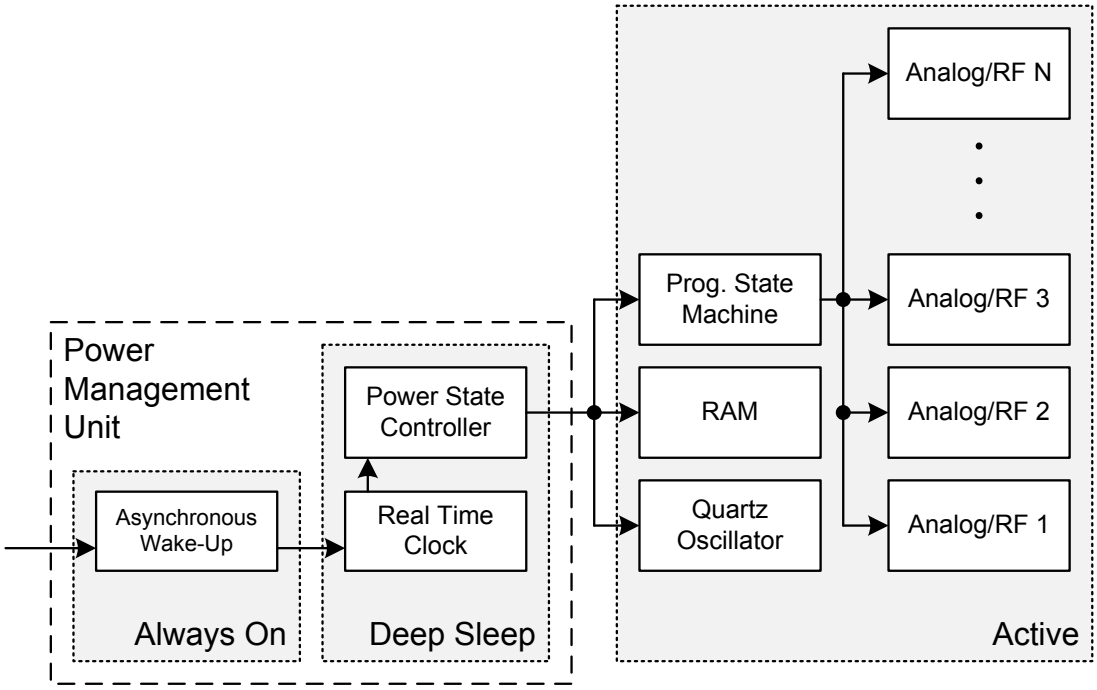


Figure 3.9: Power Domains of the Transceiver
[Technologies 2011a]

Beside the power domains, a number of power states can be identified, these states are shown in figure 3.10.

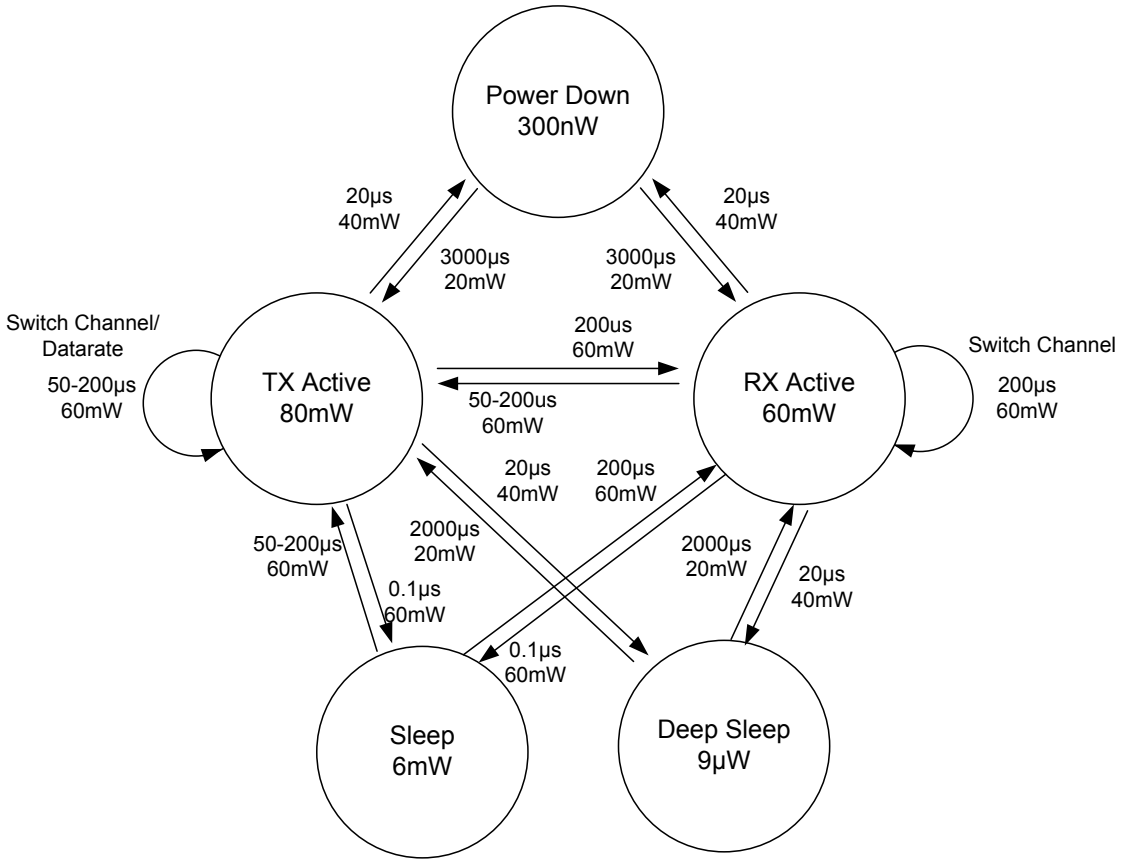


Figure 3.10: Power States of the Transceiver
[Technologies 2011a]

In power down state, only the asynchronous wake-up unit is active. It is able to detect edges on the NCS[7] and WURX[8] pins and wake up the power state controller in the case of an event. The power state controller then turns on the voltage regulators and gives control to the programmable state machine. The state machine manages the active states, and the sleep state is also under control of the programmable state machine. When all active tasks are finished, the state machine can decide to go into a deep sleep mode or into power down mode. In deep sleep, the real time clock is active, and an automatic wake up after a certain time is possible. From power down mode, only an external event can wake up the transceiver. The initial attachment of a battery is also detected as an event, which wakes up the power state controller. [Technologies 2011a]

[7] Not Chip Select
[8] Wake-up Receive

3.3.4 SPI Interface, Single-wire Connection

For the communication between the transceiver and other devices a three- and four-wire SPI is available. A three-wire interface can be accomplished because the output port FW_SDO can be set to high-impedance. Therefore FW_SDO and FW_SDI can be shortened externally to form the bidirectional FW_SDIO data line, illustrated in figure 3.11. However, the FW_SPI pins can also be used as arbitrary general purpose Input / Output (IO) pins. [Technologies 2011c]

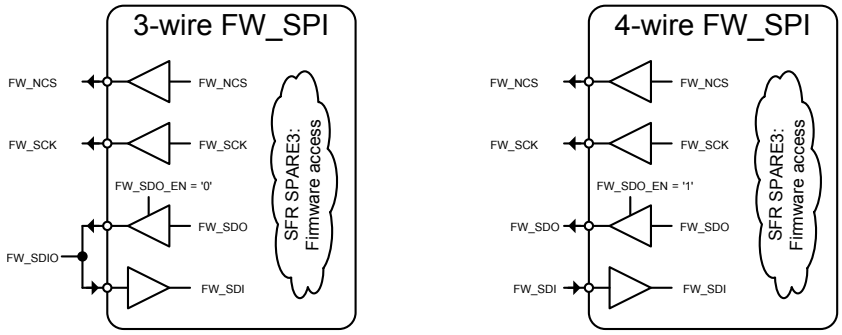


Figure 3.11: Three- and Four-wire SPI of the Transceiver
Adapted from [Technologies 2011c]

In order to perform communication with the sensor by single-wire interface the FW_SDIO of the three-wire SPI is used. The transceiver is able to receive data from the sensor by setting the FW_SDO_EN bit to “0” as well as to transmit data to the sensor by setting the FW_SDO_EN to “1”.

3.3.5 Number Representation

All arithmetic operation codes are 16 bit signed, except for the division which is 16 bit unsigned. The signed data path operation is transparent for the addition and subtraction operation codes and for the sequential multiplication operation codes so that these operation codes can be used in a 16 bit unsigned context as well. The result must be interpreted as a 16 bit signed or unsigned number, depending on the context, for example:

```
// ADD operation
 32512 +  32512 = 0x7F00 + 0x7F00 = 0xFE00 = 65024 (16bit unsigned)
(-256) + (-256) = 0xFF00 + 0xFF00 = 0xFE00 =  -512 (16bit signed)

// MUL operation
 240  * 240 = x00F0  * 0x00F0 = 0xE100 = 57600 (16bit unsigned)
(-64) * 124 = 0xFFC0 * 0x007C = 0xE100 = -7936 (16bit signed)
```

Both the 16 bit signed and the 16 bit unsigned results have identical bits but must be interpreted differently. [Technologies 2011c]

If the sequential division hardware option of the state machine is selected, hardware support for a division operation is implemented. Only unsigned numbers are allowed. Care must be taken when the division operator "/" is used in the C code because it is not fully translated into an operation code sequence that implements a division operation. Operand alignment must be done explicitly in the firmware before the division, so that:

```
a < 2 * b        // a = numerator, b = denominator
```

The division can be implemented as:

```
if (a < 2 * b)
    y = a / b;  //calculate division
else
    y = 0;      // overflow of above condition
```

Since `a` is less than `2*b`, the result `y` of the division is always smaller than `2`; accordingly only one bit is required for the digits to the left of the decimal point. All other bits represent the digits to the right of the decimal point. This means the representation of the result is:

```
y = a / b * (2^15)
```

If operand alignment was necessary before the division operation the result needs to be interpreted (shifted) again to achieve the correct value. As an example for a division let:

```
a = 0x0048;      // numerator    a = 72(dec)
a = 0x0040;      // denominator  b = 64(dec)
```

The condition `a < 2 * b` is fulfilled. The result of the division operation is expected to be `1.125` multiplied by `2^15`, for example:

```
y = 0x9000;      // result is 1.125 * 2^15
```

3.3.6 Electrical characteristics

The required supply voltages for the two power supplies can be found in table 3.5 below.

Parameter	**Symbol**	**Value**			**Unit**
		Min.	Typ.	Max.	
Main supply voltage	V_{BAT} 3V3	2.8	3.3	3.6	V
ROM supply voltage	V_{BAT} 1V5		1.5		V

Table 3.5: Supply Voltages of the Transceiver
[Technologies 2011c]

All listed current consumption values are measured at the main power supply pin ($25\,^{\circ}\mathrm{C}$) and do not include the additional current consumption of the ROM cells. Table 3.6 shows the current consumption at different system states.

Parameter	**Value**			**Unit**
	Min.	Typ.	Max.	
POWERDOWN, Shut-off mode		240		nA
SLEEP incl. fast wake-up		1.5		μA
RX/TX active, depending on activated RF components	2		22	mA

Table 3.6: Current Consumption of the Transceiver
[Technologies 2011c]

Chapter 4

Hardware Design of Power Metering Unit

In this chapter the hardware design of the proposed power metering unit is focused on the voltage ADC specification of the current and voltage sensor. A description of the full schematic can be found in section 4.1. This section covers the wiring of the current and voltage sensor, the so-called matching network with containing voltage divider and instrumentation amplifier, and the overall connection of the power metering unit to the grid. A closer look at the capacitive voltage divider used, including both its positive and negative aspects, can be found in section 4.2. This section also contains simulation results and a comparison to a resistive voltage divider.

4.1 Schematic

A full schematic of the designed hardware and the overall connection of the power metering unit on the line voltage is shown in figure 4.2. It just focuses on the capacitive voltage divider, the instrumentation amplifier, the wiring of the current and voltage sensor and an inverting charge pump. An evaluation board of the transceiver was made available, hence the wiring of the transceiver is not taken into consideration. Details concerning pin connection and external circuit can be found in the manual [Technologies 2011c].

The time-dependent behavior of the voltage divider configuration leads to a characteristic drawback, a phase shift. This phase shift is connected to the high-pass behavior of this voltage divider configuration. In this thesis a configuration is considered at which this phase shift can be neglected. However, an occurring phase shift can be corrected afterwards by firmware with little effort.

Figure 4.1 shows a first prototype of the power metering node. The above green PCB shows the evaluation board with the transceiver ASIC, supplied with $3.3\,V$ by the thin red and black cable. The designed hardware, including the sensor, can be seen in the same figure beneath the green PCB, corresponding to the schematic given in figure 4.2. Jumper $JP1$ and $JP2$ correspond to the grid connection and jumper $JP3$ and $JP4$ correspond to the connection of the load. Communication between the sensor and the transceiver is carried out by the TRX_SDIO wire, which is in accordance with the single-wire communication interface. The $3.3\,V$ level is achieved by an external pull-up resistor $R5$, so sensor and transceiver can actively pull a $0\,V$ level.

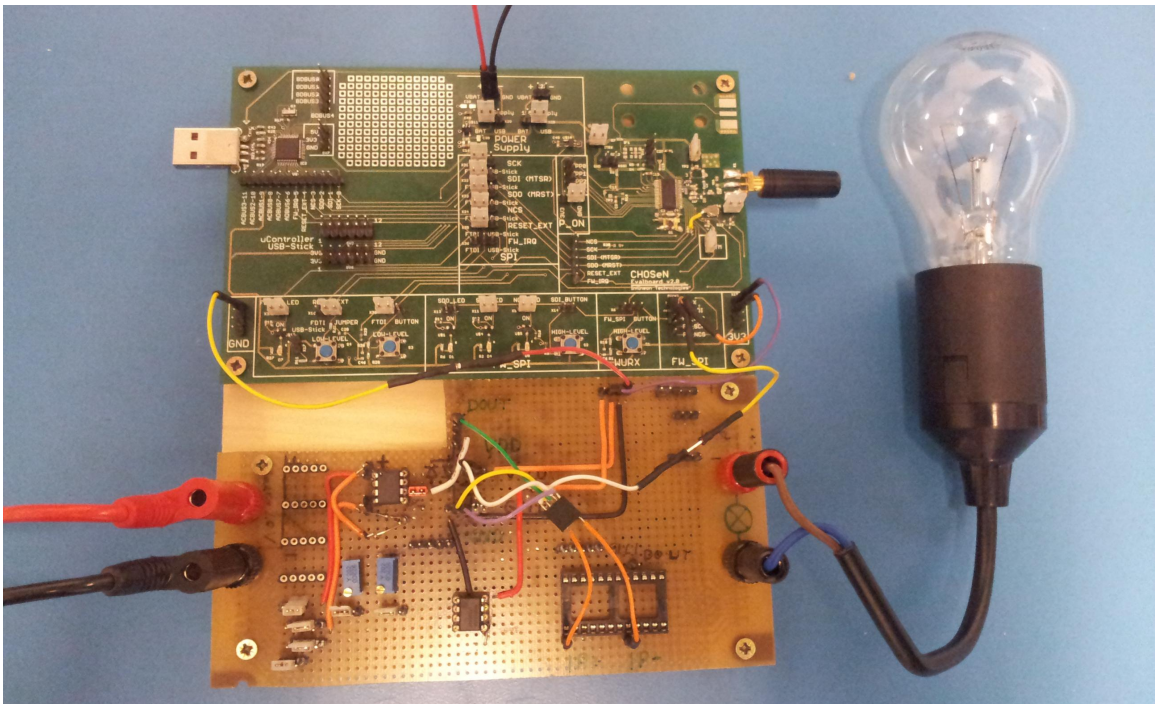


Figure 4.1: Setup of the First Prototype

The entire power metering unit must be operated as floating either by battery or by a potential-free voltage source. A reason is given in section 4.2.2.

Due to the limitations of the current and voltage sensor on the external voltage ADC input, line voltage has to be stepped down using a capacitive voltage divider. This voltage divider is shown in figure 4.2, represented by the capacitors C_1 to C_3. The capacitive voltage divider and its characteristics are discussed in the following section 4.2.

An instrumentation amplifier AD623 with a gain of $G = 1$ is used to generate a single-ended output signal, in order to comply with the required characteristics for the external voltage measurement. Resistors R_1 and R_2 are establishing a ground return path for the instrumentation amplifier corresponding to the data sheet [Devices 2008]. These input bias currents have to flow to bias the input transistor of the instrumentation amplifier when amplifying floating sources. The resistors R_3 and R_4 are representing an input protection for the instrumentation amplifier corresponding to the data sheet (referred to as R_{LIM}) covered in section 4.3.2. In addition to the resistors, the capacitors C_4 to C_5 are meant to discharge higher frequency interferences. More details concerning the input protection of the instrumentation amplifier can be found in the following section 4.2. [Devices 2008]

Diodes D_1 and D_2 protect the DOUT pin of the sensor with approximately $\pm 0.7\,V$ to GND. An inverting charge pump MAX868 generates a regulated negative supply voltage required by the instrumentation amplifier.

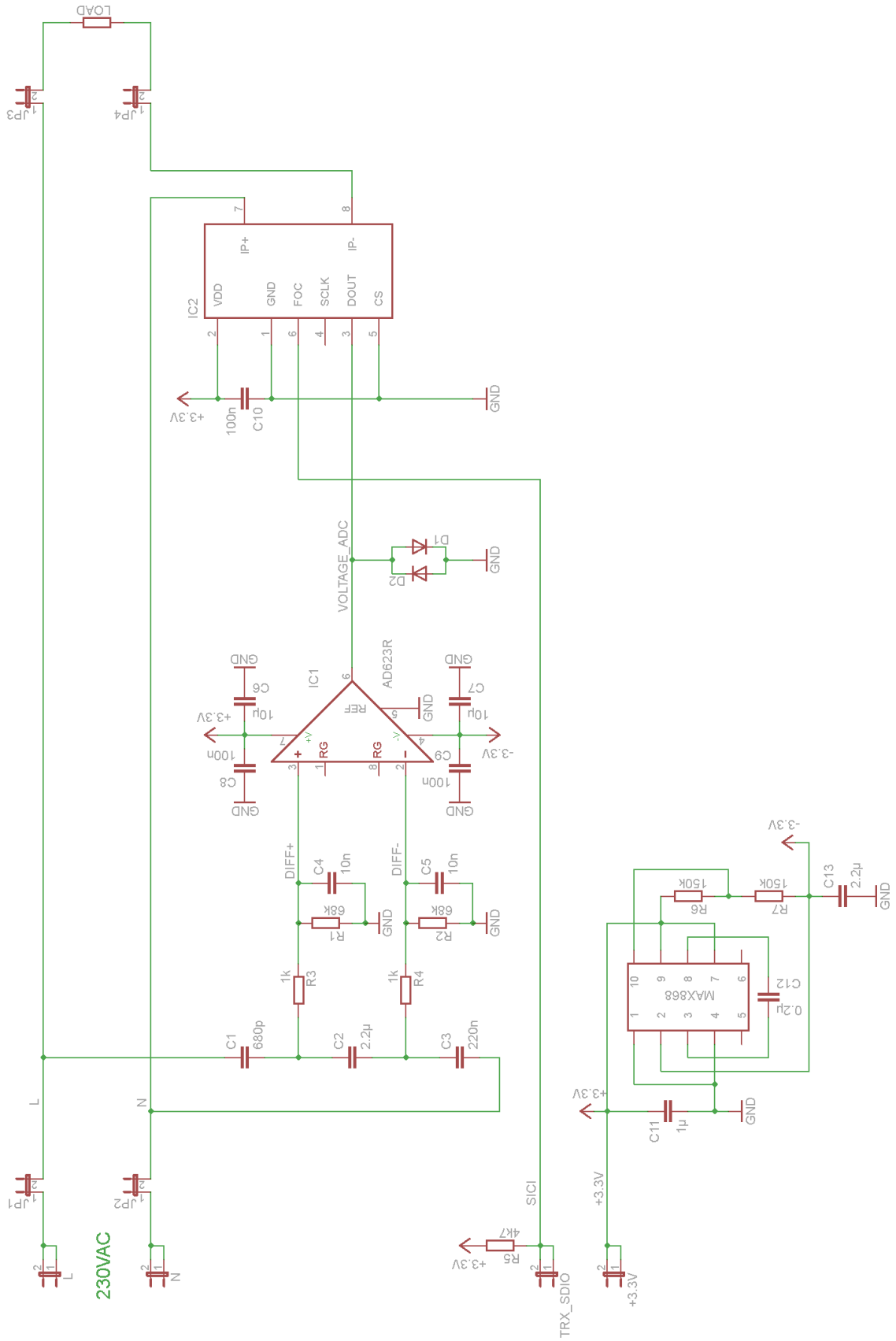


Figure 4.2: Full Schematic without Transceiver

4.2 Capacitive Voltage Divider

The voltage divider C_1 to C_3 is required to step down the line voltage to a range of $\pm 200\,mV$. This voltage is measured by the external voltage ADC of the sensor. The measured, digitized voltage level can easily be corrected afterwards by firmware in order to correlate to the line voltage.

Basically, there are two options to realize such a voltage divider, either a resistive or a capacitive voltage divider. Both have their advantages and drawbacks with respect to power consumption and phase shift. An additional benefit to using capacitors for Infineon Technologies AG as the chip manufacturer is that capacitors can be realized in embedded Wafer Level Ball Grid Array (eWLB) technology. Resistor components can be realized in eWLB technology as well, but are associated with significant costs due to missing specific material. Advantages and drawbacks to using resistors and capacitors are listed below. [Wojnowski *et al.* 2008], [Prashant *et al.* 2010]

Resistive Voltage Divider

- Pro:
  - No phase shift
- Con:
  - Active power consumption

Capacitive Voltage Divider

- Pros:
  - Available in eWLB
  - Apparent power consumption
- Con:
  - Phase shift

Power consumption for both resistive and capacitive voltage dividers is negligible. Simulations with a line voltage of $230\,V$ result a current consumption for a resistive voltage divider in the range of $20\,\mu A$ and a current consumption for a capacitive voltage divider in the range of $50\,\mu A$. However, in this thesis a capacitive voltage divider is used to step down line voltage. Figure 4.5 shows the capacitive voltage divider used.

4.2.1 Dimensioning the Voltage Divider

Regarding the dimensioning of the voltage divider for a line voltage of $V_{grid} = 230\,V$, the following parameters need to be considered:

- the line voltage with a peak value of $\hat{V}_{grid} = 325.27\,V$ and a frequency of $f = 50\,Hz$,
- the current $\hat{I}$ through the capacitors C_1 to C_3 and
- the maximum input voltage of the sensor $\hat{V}_{diff+} - \hat{V}_{diff-} = \pm 200\,mV$.

The voltages, whose difference is amplified by the instrumentation amplifier, are assumed to be

$$\hat{\boldsymbol{V}}_{\boldsymbol{diff+}} = \mathbf{1.1}\,\boldsymbol{V} \text{ and}$$
$$\hat{\boldsymbol{V}}_{\boldsymbol{diff-}} = \mathbf{1.0}\,\boldsymbol{V}.$$

Based on the current I, dimensioning of the voltage divider is carried out in two steps. First of all a series connection of two capacitors C_1 and C_2 as shown in figure 4.3 is assumed.

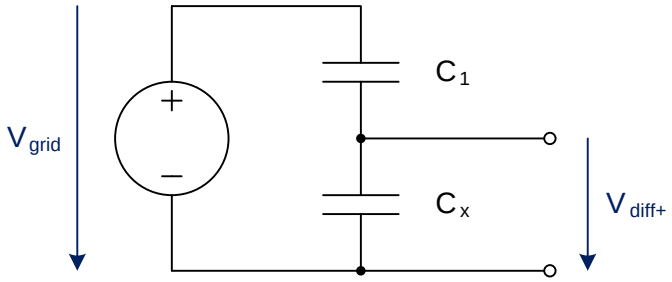


Figure 4.3: Series Connection of C_1 and C_x

For a given current of $\hat{I} = 70.71\,\mu A$ the total reactance of the voltage divider can be calculated by

$$X_C = \frac{\hat{V}_{grid}}{\hat{I}} = \frac{325.27\,V}{70.71\,\mu A} = 4.6\,M\Omega.$$

The reactance of a capacitor can be determined by

$$X_C = \frac{1}{2\pi f C}. \tag{4.1}$$

Equation 4.1 leads to the total capacitance of the series connection and can be calculated by

$$C_{total} = \frac{1}{2\pi f X_C} = \frac{1}{2\pi\ 50\,Hz\ 4.6\,M\Omega} = 691.98\,pF.$$

In a series connection the electric charge Q of all capacitors have the same value and following equation has to be applied

$$Q = C_{total}\, V_{grid},$$

where C_{total} corresponds to the capacitance and V_{grid} to the voltage drop at the capacitors. The total capacitance C_{total} of a series connection is determined by

$$C_{total} = \frac{C_1\, C_x}{C_1 + C_x}. \tag{4.2}$$

Out of equations

$$Q = C_{total}\, \hat{V}_{grid} \text{ and } Q = C_x\, \hat{V}_{diff+}$$

the capacitor C_x can be calculated by

$$C_x = \frac{C_{total}\, \hat{V}_{grid}}{\hat{V}_{diff+}} = \frac{691.98\, pF\ 325.27\, V}{1.1\, V} = 204.62\, nF.$$

Using the capacitance value of C_x calculated above, the capacitance of C_1 can be derived from equation 4.2 by

$$\boldsymbol{C_1} = \frac{C_{total}\, C_x}{C_x - C_{total}} = \frac{691.98\, pF\ 204.62\, nF}{204.62\, nF - 691.98\, pF} = \mathbf{694.33\, pF}.$$

In the second step of the capacitor C_x is replaced by a series connection of two capacitors C_2 and C_3. The resulting voltage divider is depicted in figure 4.4. Now then, the total capacitance $C_{2,3}$ is in accordance with the previous calculated capacitor C_x.

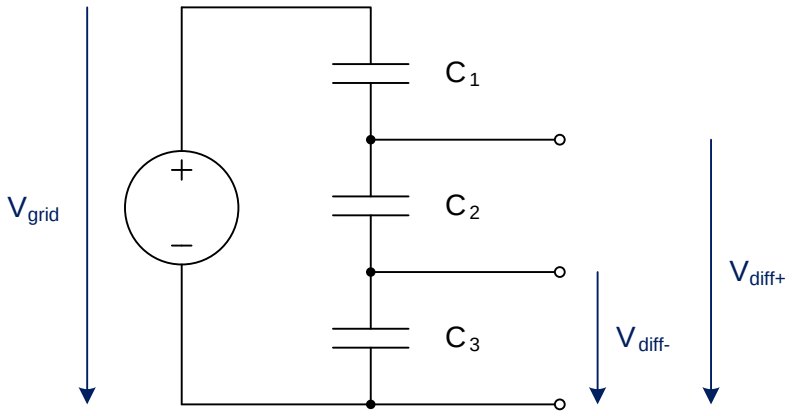


Figure 4.4: Series Connection of C_1, C_2 and C_3

The following parameters are applied:

$$\begin{aligned} \hat{V}_{diff+} &= 1.1\,V, \\ \hat{V}_{diff-} &= 1.0\,V \text{ and} \\ C_{2,3} = C_x &= 204.62\,nF. \end{aligned}$$

Because the capacitors C_2 and C_3 are connected in series the total reactance is given by

$$X_{C_2,C_3} = \frac{1}{2\pi f C_x} = \frac{1}{2\pi\ 50\,Hz\ 204.62\,nF} = 15.56\,k\Omega.$$

Both capacitors C_2 and C_3 can be determined by

$$\begin{aligned} \boldsymbol{C_3} &= \frac{C_{2,3}\,\hat{V}_{diff+}}{\hat{V}_{diff-}} = \frac{204.62\,nF\ 1.1\,V}{1.0\,V} = \boldsymbol{225.08\,nF} \text{ and} \\ \boldsymbol{C_2} &= \frac{C_{2,3}\,C_3}{C_3 - C_{2,3}} = \frac{204.62\,nF\ 225.08\,nF}{225.08\,nF - 204.62\,nF} = \boldsymbol{2.25\,\mu F}. \end{aligned}$$

The selected values for the capacitors are $\boldsymbol{C_1 = 680\,pF}$, $\boldsymbol{C_2 = 2.2\,\mu F}$ and $\boldsymbol{C_3 = 220\,nF}$.

Because most of the voltage drops at capacitor C_1, it is realized as X2/Y3 safety certified ceramic chip capacitor from Johanson Dielectrics Inc. Details concerning the capacitors can be found in the product catalog [Dielectrics 2010].

4.2.2 Time-dependent Behavior

Figure 4.5 depicts the full schematic of the so-called matching network and accordingly the capacitive voltage divider. The line voltage is stepped down by the capacitive voltage divider, represented by capacitors C_1 to C_3. With the selected capacitors a maximum differential voltage of approximately $\hat{V}_{diff+} - \hat{V}_{diff-} = \pm 100\,mV$ is adjusted, considering an rms-value of line voltage of $V_{grid} = 230\,V$. Basically, two cases need to be distinguished considering the operational conditions of the matching network. On one hand, the normal operational condition within the entire matching network is dividing conventional line voltage with an rms-value of $V_{grid} = 230\,V$ and a frequency of $f = 50\,Hz$. On the other hand, transient events during switching on the network need to be analyzed in particular. Simulations were carried out with an interference voltage peak of $1\,kV$, discussed more closely in section 4.2.3.

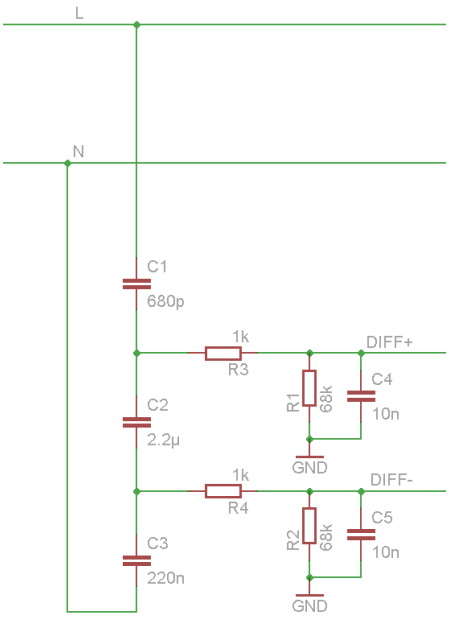


Figure 4.5: Schematic of the Capacitive Voltage Divider

Normal Operational Condition

An instrumentation amplifier, amplifying the differential voltage $V_{diff+} - V_{diff-}$ with a gain of $G = 1$, is used to establish a single-ended signal which can be measured by the sensor.

In the normal operational condition the designed voltage divider, in conjunction with the instrumentation amplifier, fulfills all requirements for the sensor in order to measure line voltage in a range of $\pm 200\,mV$. In case of an incorrect plugged unit (live wire L and neutral wire N are interchanged), the voltage between V_{diff+} and accordingly V_{diff-} and the neutral wire N may exceed FELV[1]. Details are covered in the following section 4.2.3.

The time-dependent behavior completely changes depending on whether the reference potential GND is connected to neutral wire N; that is the reason why the power metering unit has to be supplied by a floating source.

Power-on Transients

Simulations were made with an interference voltage peak of $1\,kV$ in case the power metering unit was plugged to the grid. In this case, resistors R_3 and R_4 limit the input voltage of the instrumentation amplifier to an admissible value corresponding to the data sheet [Devices 2008]. Because the protective effect of the circuit depends on the maximum frequency of the interference, additional capacitors C_4 and C_5 are needed in order to protect

[1] Functional Extra Low Voltage, $50\,V\,AC$ or $120\,V\,DC$ [Plaßmann and Schulz 2009]

the inputs of the instrumentation amplifier. Details concerning this special case are covered in following section 4.2.3.

In power-on condition the protective effect of the designed configuration is functional, whether live wire L and neutral wire N are connected correctly or not. In the same way as in normal operational condition, the voltage between V_{diff+} and accordingly V_{diff-} and the neutral wire N may exceed FELV when the unit is plugged incorrectly to the grid.

4.2.3 Simulation Results

In order to verify the desired characteristics of the designed matching-network and accordingly the capacitive voltage divider, simulations were carried out for normal operational conditions as well as for power-on transients. The simulation of the entire voltage divider is performed using LTspice IV ® ([Technology]).

In normal operational conditions the time-dependent behavior was simulated transiently with an rms-value of line voltage of $V_{grid} = 230\,V$ and a frequency of $f = 50\,Hz$. The frequency-dependent behavior of the voltage divider was accomplished with an AC simulation related to $AC = 1\,V$.

In order to ensure an input protection for the instrumentation amplifier, power-on transients were simulated by a transient simulation of a peak voltage of $\hat{V}_{grid} = 1\,kV$, a rise time of $t_{rise} = 1\,\mu s$ and a fall time of $t_{fall} = 1\,\mu s$. Generally, the protective effect depends on the maximum frequency of the interference voltage peak as well as on a parasitic capacitance between the floating ground and the neutral wire N. If the power metering unit is plugged correctly, the protective effect is independent of a parasitic capacitance for the most part. When the live wire L and N are interchanged, the protective effect is strongly influenced by a parasitic capacitance as well as the maximum frequency of the interference voltage.

Note, that in the simulation charts all traces are globally referred to GND (according to figure 4.6), but this is a different ground than that used in the schematic. In the simulation the COM symbol is in accordance with the floating ground of the schematic in 4.5.

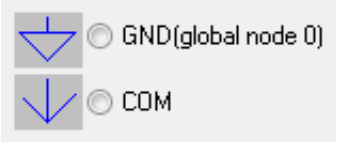


Figure 4.6: Legend for Simulation

Normal Operational Condition

Transient Simulation: plugged correctly, according to schematic 4.5

Figure 4.7 shows the simulation plot for the voltage divider with the calculated values from section 4.2.1. The traces V_{diff+} and V_{diff-} depicted in the chart are related to neutral wire N. As shown in the simulation result, at a line voltage of $V_{grid} = 230\,V$ a differential voltage of $V_{diff+} - V_{diff-} \approx 100\,mV$ is achieved.

- rms-value of line voltage $V_{grid} = 230\,V$
- frequency of $f = 50\,Hz$

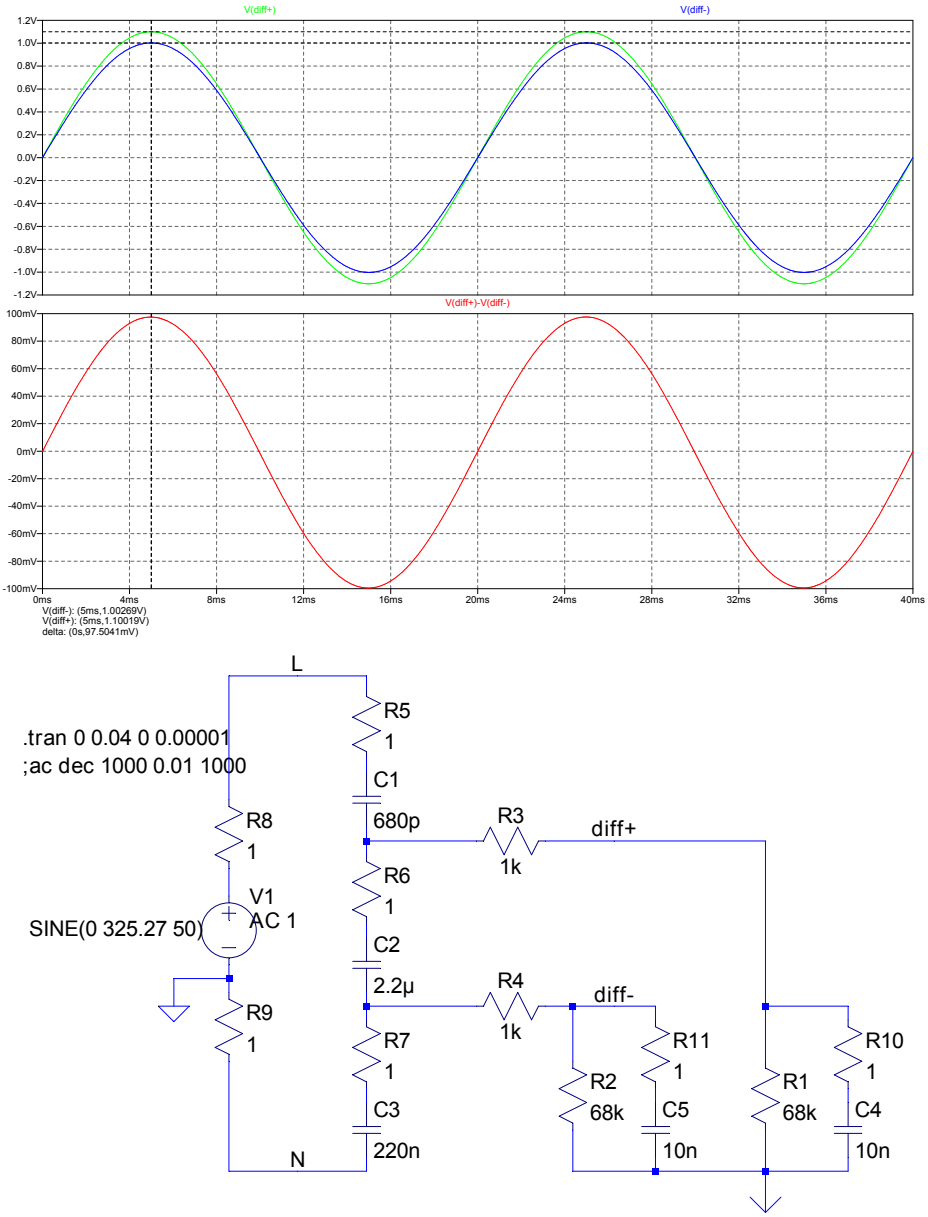


Figure 4.7: Transient Simulation with Sine

Transient Simulation: live wire L and neutral wire N are interchanged

The special case in which live wire L and neutral wire N are interchanged is depicted in figure 4.8. As shown in the figure, the differential voltage $V_{diff+} - V_{diff-}$ has not changed, though in contrast to a correct plugged unit the voltage between V_{diff+} and accordingly V_{diff-} and the neutral wire N exceeds FELV.

- rms-value of line voltage $V_{grid} = 230\,V$
- frequency of $f = 50\,Hz$

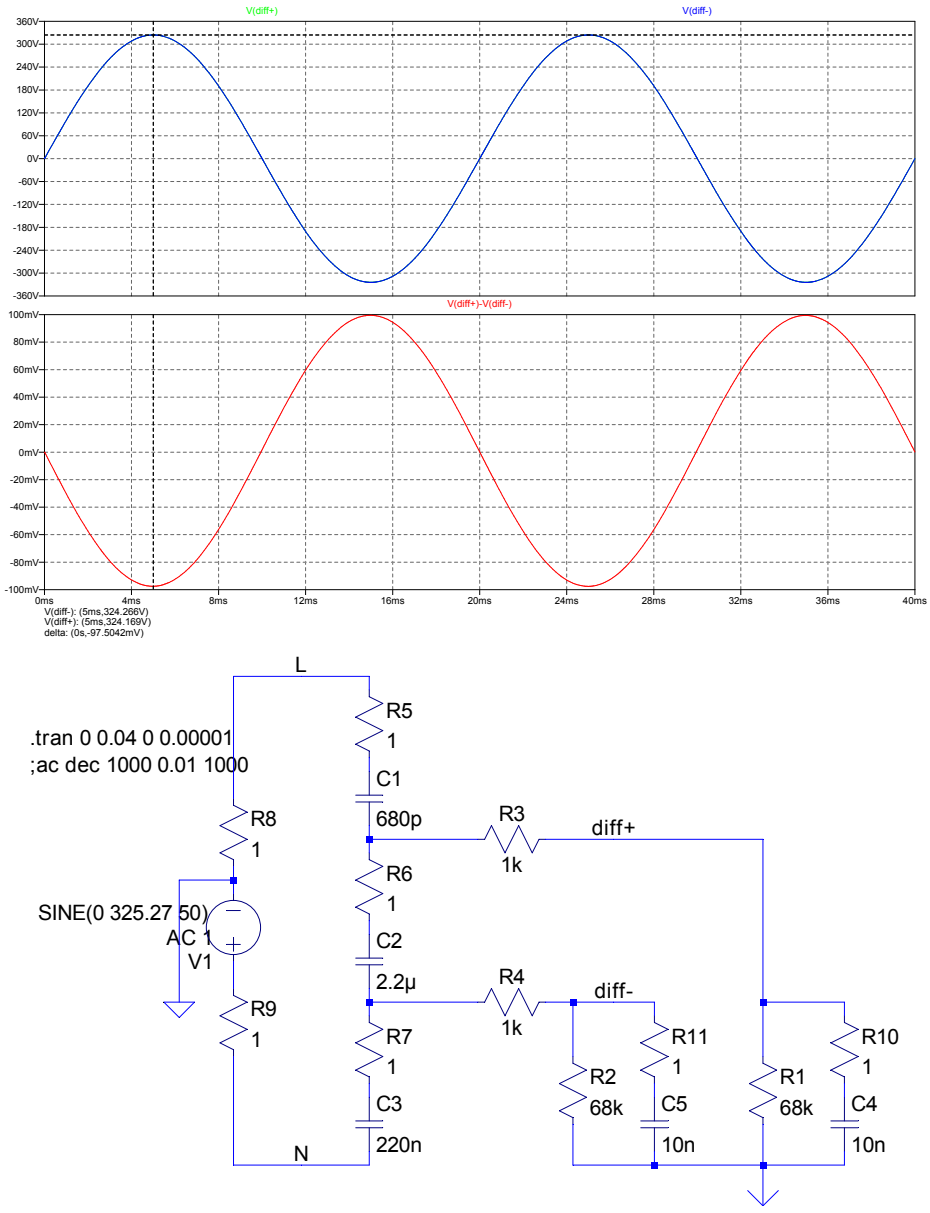


Figure 4.8: Transient Simulation with Sine (L and N interchanged)

Small Signal AC Simulation

The frequency-dependent behavior of the designed capacitive voltage divider is depicted in figure 4.9. The voltage divider shows high-pass characteristics up to approximately $1\,kHz$, as shown in the Bode diagram. With a cutoff frequency of $f_c \approx 500\,mHz$, the observed phase shift of $\varphi \approx 0.46\,^\circ$ for an operating frequency of $f = 50\,Hz$ can be neglected.

- amplitude of $AC = 1\,V$
- frequency from $10\,mHz$ up to $1\,kHz$

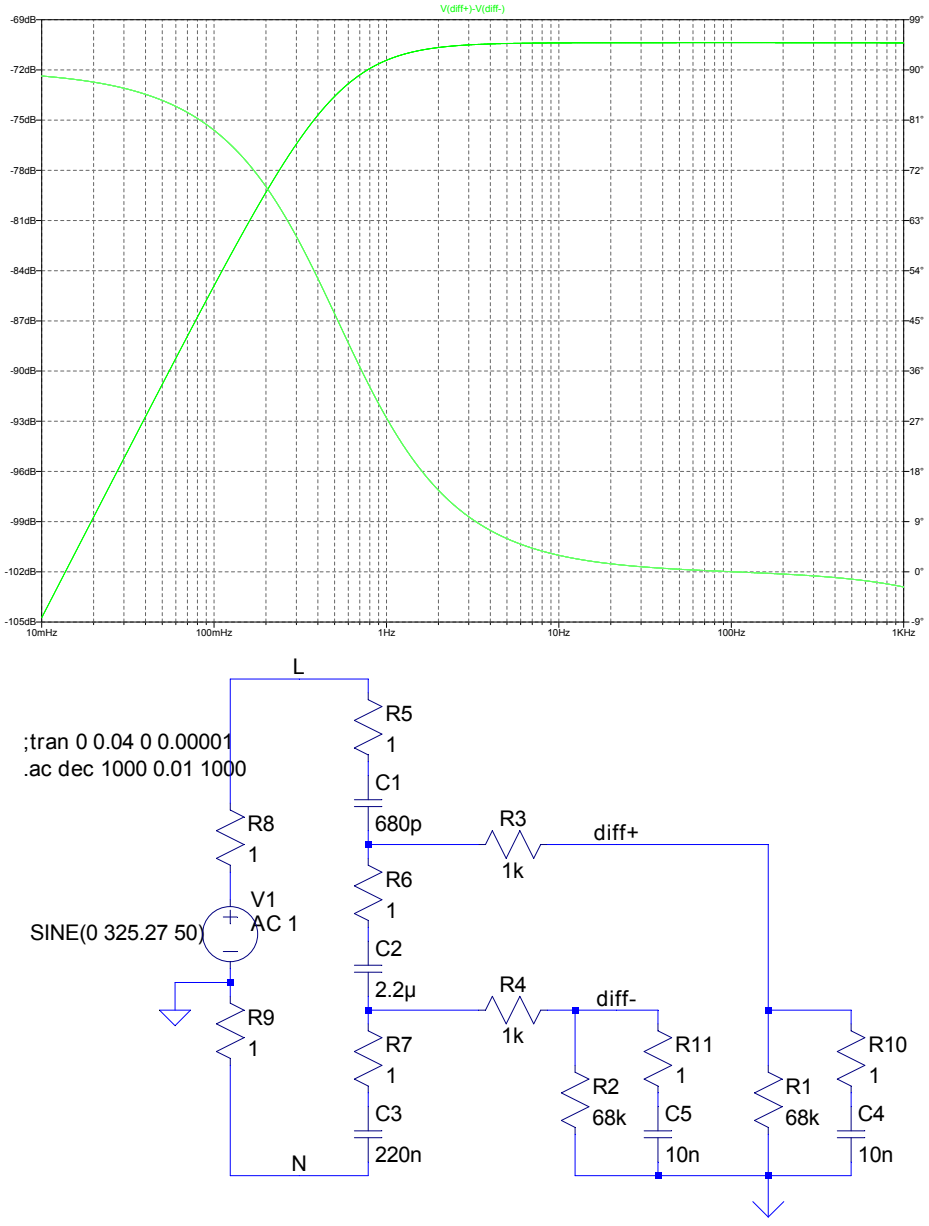


Figure 4.9: Small Signal AC Simulation

Power-on Transients

In order to estimate parasitic effects, an equivalent circuit with an assumed inductance of $L = 10\,mH$ per power cable and an Equivalent Series Resistance (ESR) of $1\,\Omega$ was simulated. As shown in figure 4.10 within a time of approximately $20\,\mu s$ the voltage level at live wire L may rise up to approximately $500\,V$. Considering a worst-case scenario of an charged capacitor, the following simulations were carried out with an interference voltage peak of $V_{on} = 1\,kV$.

- voltage pulse with $V_{on} = \hat{V}_{grid} \approx 330\,V$
- rise time $t_{rise} = 1\,\mu s$

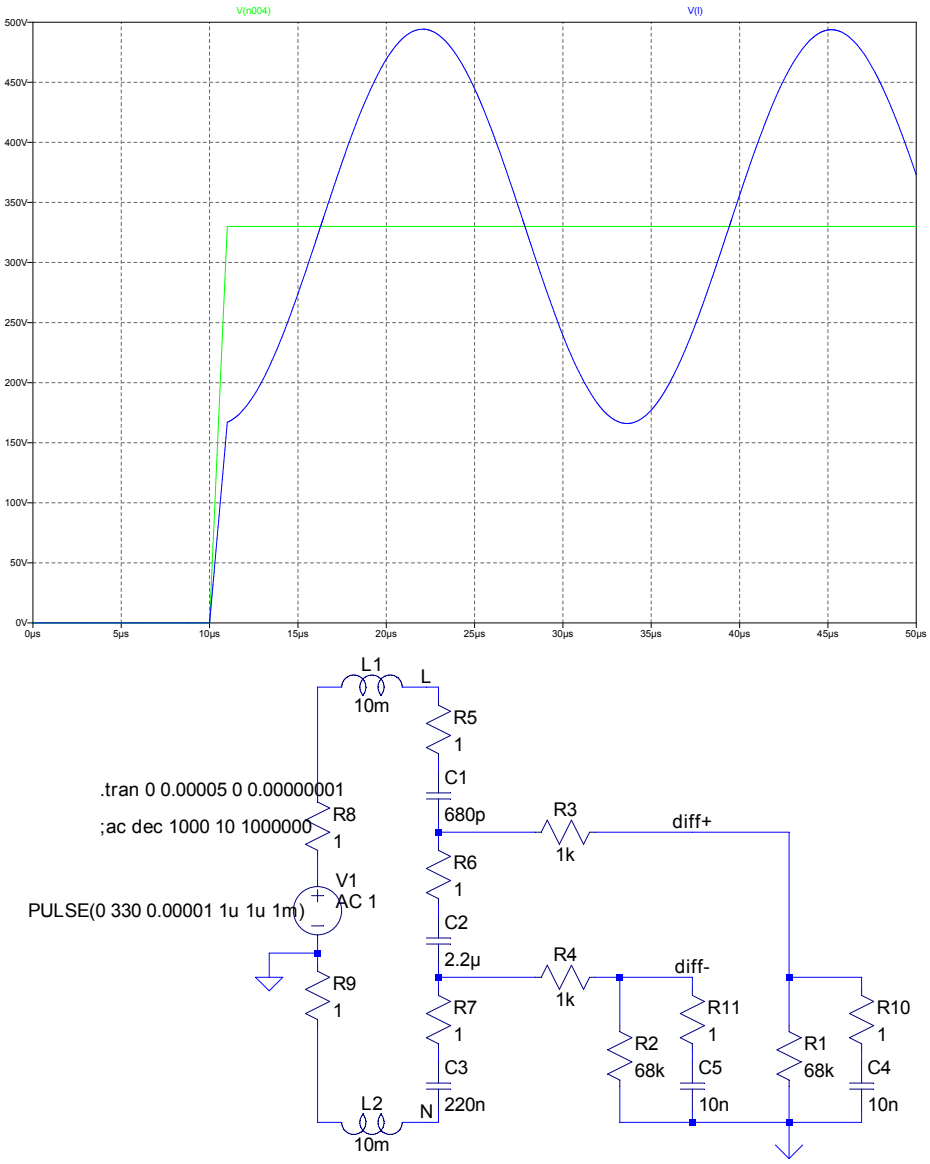


Figure 4.10: Transient Simulation of Equivalent Circuit

Transient Simulation: plugged correctly, according to schematic 4.5

Figure 4.11 shows the protective effect of $V_{diff+} - V_{com}$ and $V_{diff-} - V_{com}$ with an interference voltage peak of $1\,kV$, when the power metering unit is plugged correctly to the grid. As shown in the chart, the protective effect which will prevent permanent damage to the instrumentation amplifier is provided.

- switch-on voltage of $V_{on} = 1\,kV$
- rise time $t_{rise} = 1\,\mu s$
- fall time $t_{fall} = 1\,\mu s$

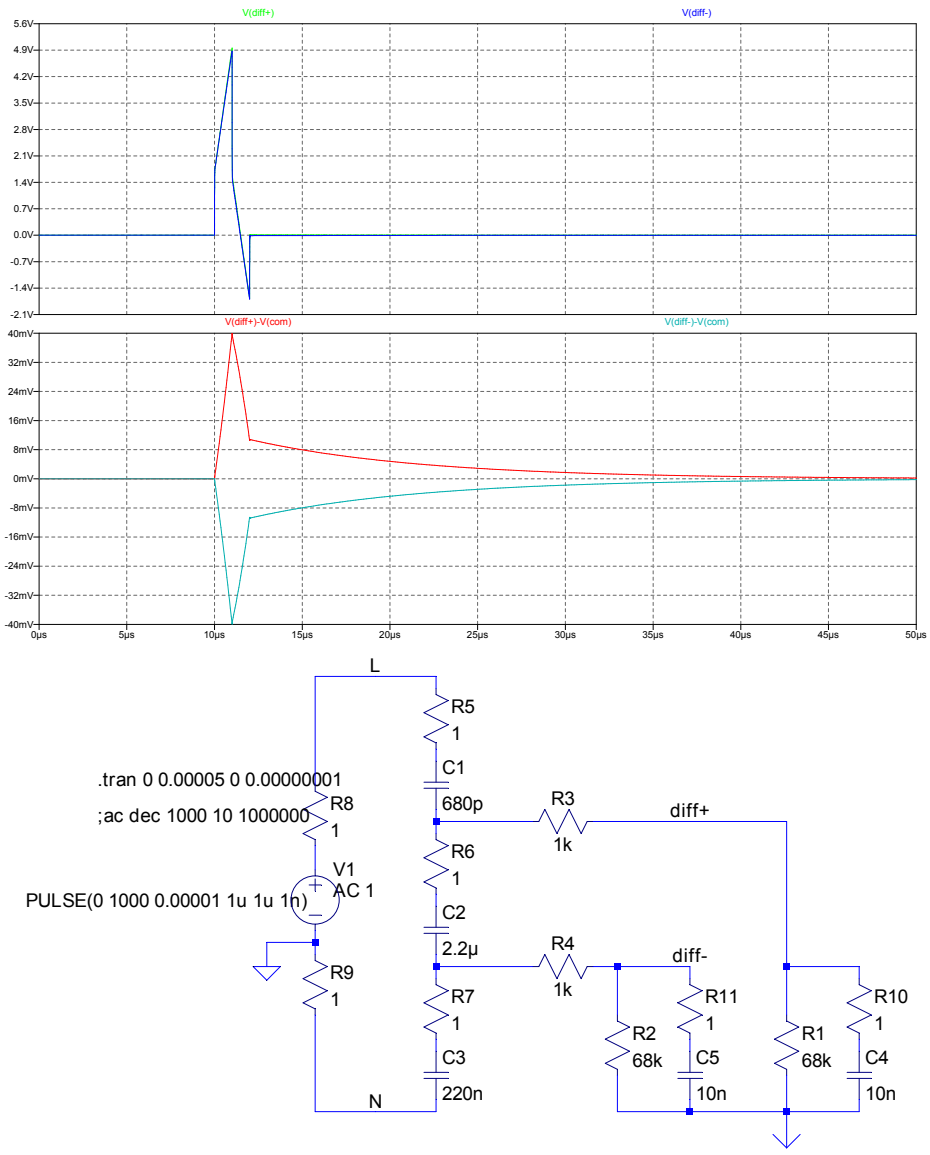


Figure 4.11: Transient Simulation with Interference Voltage Peak

Transient Simulation: live wire L and neutral wire N are interchanged

The simulation result in the case of an incorrect plugged power metering unit is shown in figure 4.12. As shown in the figure, protection for the inputs of the instrumentation amplifier is provided as well. Although as in normal operational conditions the voltage between V_{diff+} and accordingly V_{diff-} and the neutral wire N exceeds FELV,

- switch-on voltage of $V_{on} = 1\,kV$
- rise time $t_{rise} = 1\,\mu s$
- fall time $t_{fall} = 1\,\mu s$

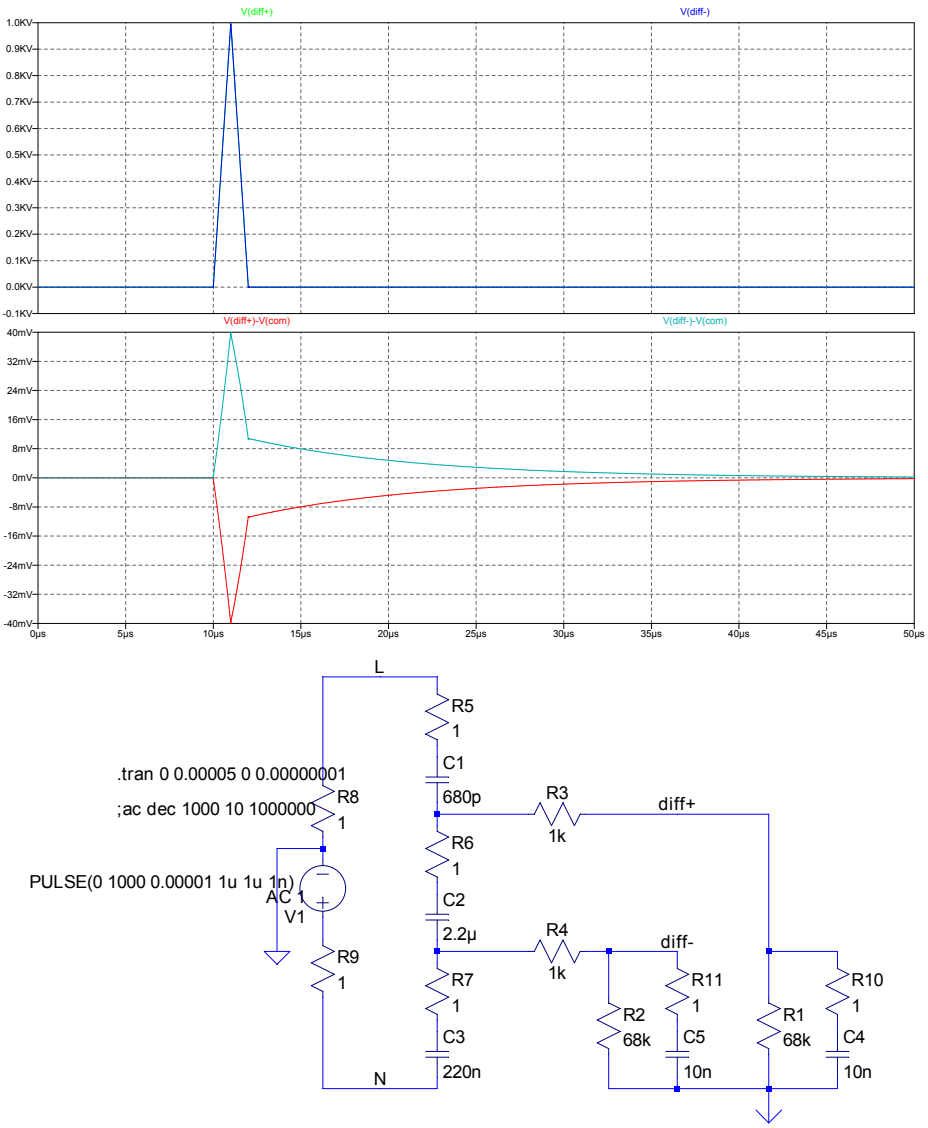


Figure 4.12: Transient Simulation with Interference Voltage Peak (L and N interchanged)

4.3 Instrumentation Amplifier

"The AD623 is an integrated single-supply instrumentation amplifier that delivers rail-to-rail output swing on a $3\,V$ to $12\,V$ supply. The AD623 offers superior user flexibility by allowing single gain set resistor programming and by conforming to the 8-lead industry standard pinout configuration. With no external resistor, the AD623 is configured for unity gain (G = 1), and with an external resistor, the AD623 can be programmed for gains up to 1000. [...]

Low power consumption ($1.5\,mW$ at $3\,V$), wide supply voltage range, and rail-to-rail output swing make the AD623 ideal for battery-powered applications. The rail-to-rail output stage maximizes the dynamic range when operating from low supply voltages. The AD623 replaces discrete instrumentation amplifier designs and offers superior linearity, temperature stability, and reliability in a minimum of space." [Devices 2008]

4.3.1 Basic Connection

"Figure 4.13 shows the basic connection circuit for the AD623. The $+V_S$ and $-V_S$ terminals are connected to the power supply. The supply can be either bipolar ($V_S = \pm 2.5\,V$ to $\pm 6\,V$) or single supply ($-V_S = 0\,V$, $+V_S = 3.0\,V$ to $12\,V$). Power supplies should be capacitively decoupled close to the power pins of the device. For the best results, use surface-mount $0.1\,\mu F$ ceramic chip capacitors and $10\,\mu F$ electrolytic tantalum capacitors.

The input voltage, which can be either single-ended (tie either $-IN$ or $+IN$ to ground), or differential is amplified by the programmed gain. The output signal appears as the voltage difference between the $OUTPUT$ pin and the externally applied voltage on the REF input. For a ground-referenced output, REF should be grounded." [Devices 2008]

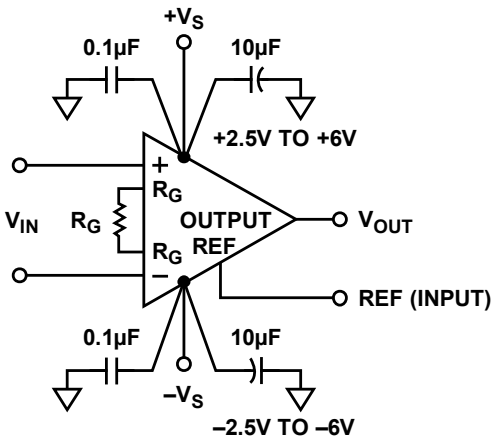


Figure 4.13: Dual-Supply Basic Connection
[Devices 2008]

Gain Selection

"The gain of the AD623 is resistor programmed by R_G, or more precisely, by whatever impedance appears between Pin 1 and Pin 8. The AD623 is designed to offer accurate gains using $0.1\,\%$ to $1\,\%$ tolerance resistors. [...] Note that for $G = 1$, the R_G terminals are unconnected ($R_G = \infty$)." [Devices 2008]

4.3.2 Input Protection

"Internal supply referenced clamping diodes allow the input, reference, output, and gain terminals of the AD623 to safely withstand overvoltages of $0.3\,V$ above or below the supplies. This is true for all gains and for power on and power off. This last case is particularly important because the signal source and amplifier may be powered separately.

If the overvoltage is expected to exceed this value, the current through these diodes should be limited to about $10\,mA$ using external current limiting resistors (see Figure 4.14). The size of this resistor is defined by the supply voltage and the required overvoltage protection." [Devices 2008]

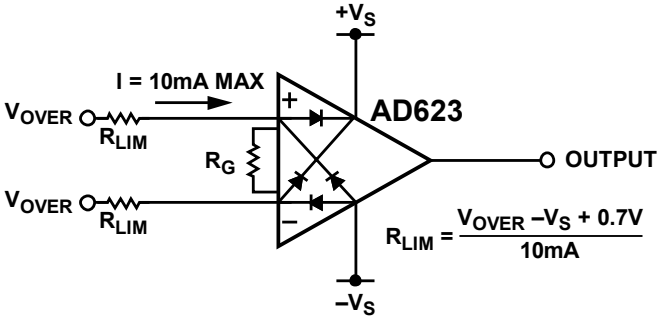


Figure 4.14: Input Protection
[Devices 2008]

4.3.3 Ground Returns for Input Bias Currents with AC-coupled Inputs

"Input bias currents are those DC currents that must flow to bias the input transistors of an amplifier. These are usually transistor base currents. When amplifying floating input sources, such as transformers or AC-coupled sources, there must be a direct DC path into each input in order that the bias current can flow." [Devices 2008]

Figure 4.15 shows how a bias current path can be provided for the case of capacitive ac coupling.

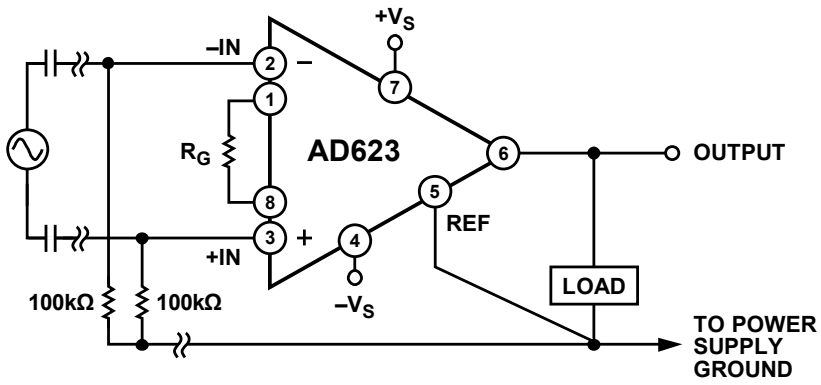


Figure 4.15: Ground Returns for Input Bias Currents
[Devices 2008]

More details concerning the instrumentation amplifier AD623 can be found in the data sheet [Devices 2008].

Chapter 5

Software Design of Power Metering Unit

In this chapter the firmware design of the proposed power metering unit is introduced. A rough overview of the firmware architecture as well as subroutines are presented in section 5.1. An example in the form of a pseudo code of how to calculate active power and apparent power is given in section 5.1.1 and section 5.1.2, in order to get familiar with the applied number representation. Furthermore, characteristics of calculating the square root as well as the multiplication algorithm are the focus in section 5.2 and section 5.3.

5.1 Firmware Architecture

Due to limitations caused by the limited language subset of the C compiler, a specific floating point representation was implemented based on the characteristic of the division operation (covered in section 3.3.5). Temporary variables required during firmware processing are located in the GPRAM.

The mantissas of the calculated current and voltage values are each stored in a 16 bit GPRAM register, namely `current_value` and `voltage_value`. The exponent and the sign bit of each value are stored in a third register named `current_voltage_exp`. The register content for this specific floating point representation by using mantissa, exponent and sign bit can be seen in figure 5.1.

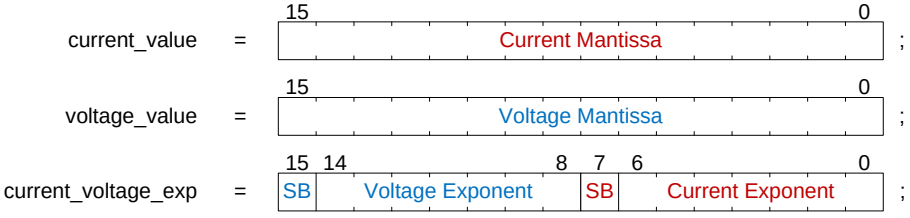


Figure 5.1: Current and Voltage Value Registers

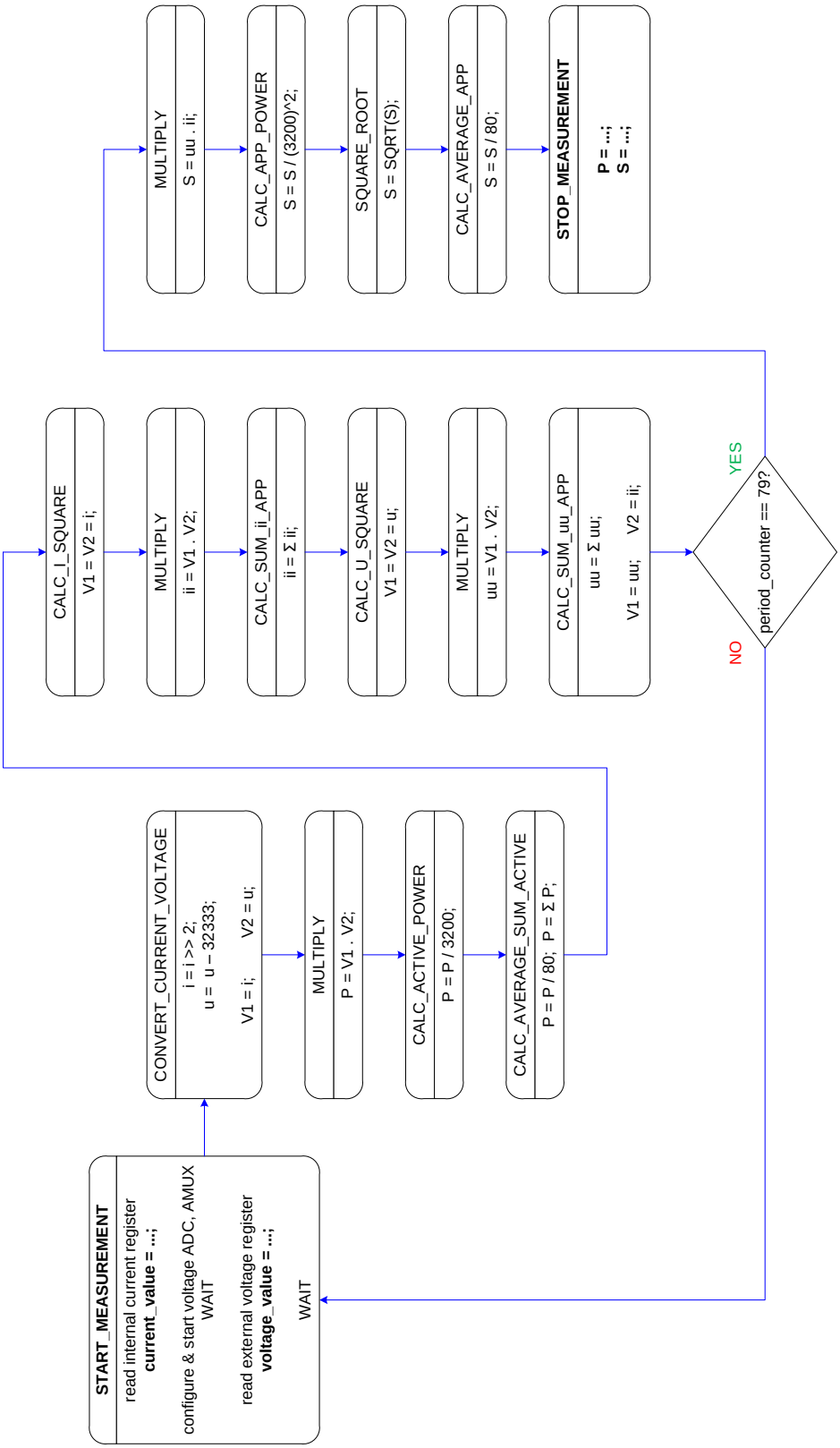


Figure 5.2: Flowchart of Power Calculation

Figure 5.2 illustrates the main building blocks of the firmware architecture. Each of these blocks represent a subroutine. The subroutine `START_MEASUREMENT` corresponds to the yellow box marked with number 4 from the current and voltage measurement sequence depicted in figure 3.6. Note, that calculating active power as well as apparent power takes approximately $500\,\mu s$ as a consequence of the complex square root implementation.

The entire power calculation is carried out over 10 periods with a sampling rate of $fs = 400\,Hz$, resulting in 8 samples per period of $T = 20\,ms$. Note, that the division ratio of the assembled voltage divider has to be calibrated individually for every power metering unit due to the high tolerances of the capacitors. In the following, an example in the form of a pseudo code is given with one value of current and voltage and a division ratio of the voltage divider of 3200 for clarification. In other words, a measured voltage of $100\,mV$ corresponds to $320\,V$ line voltage. After the sensor has finished the internal current and voltage measurement sequence, the transceiver has received one current value and the corresponding voltage value.

```
void START_MEASUREMENT()
{
    SEND_CMD(READ_CURRENT_REG);
    SEND_CMD(FREEZE);
    current_value = temp1;  // current_value = 0x0C80;
                            // 3200(dec) --> 10A
    ... // configure & start voltage ADC

    SEND_CMD(READ_VEXT_VOLTAGE_REG);
    SEND_CMD(UNFREEZE);
    voltage_value = temp2;  // voltage_value = 0x9858;
                            // 39000(dec) --> 320V
    ...
}
```

By using the relationship in table 3.2, the received binary value has to be edited to correspond to the analog value of the current. Thus, the reading from the internal current output register has two more LSBs, the value has to be shifted 2 bit to the right. The analog current value and accordingly the analog voltage value can be determined by following equations5.1.

$$\begin{aligned} current_{analog}\ [A] &= \frac{current_{binary}\ [16\,bit] >> 2}{80} \\ voltage_{analog}\ [V] &= \frac{voltage_{binary}\ [16\,bit] - 32333}{66670} \end{aligned} \tag{5.1}$$

Generally, only the 15 highest-order bits were processed in order to avoid complications with regard to signed and unsigned interpretation. This is carried out by shifting the mantissa by one to the right and incrementing the exponent of the related value. Depending on both the received value and whether the current or voltage value was involved, the sign bit of the corresponding value has to be set.

```
void CONVERT_CURRENT_VOLTAGE_VALUE()
{
    /* current_value 16bit: [0xC180/-50A ... 0x3E80/+50A] */
    if ((current_value & 0x8000) == 0x0000){ // positive value?
        current_voltage_exp = current_voltage_exp & 0x0000;
        current_value = current_value >> 2;
    }
    else{   // negative value
        current_voltage_exp = current_voltage_exp | 0x0080;
        current_value = (current_value >> 2) * (-1);
    }
    // current_value = 0x0320;          // 800*2^0(dec)
    // current_voltage_exp = 0x0000;    // 0(dec)
    // 800 * 2^0 / 80 = 10A

    /* voltage_value 16bit: [0x6442/-0.1V ... 0x9858/+0.1V] */
    voltage_value = (voltage_value >> 1) & 0x7FFF;
    current_voltage_exp = current_voltage_exp + 0x0100;
    if (voltage_value > 0x3F25){    // positive value?
        voltage_value = voltage_value - ZERO_VALUE;
    }
    else{   // negative value

        voltage_value = 0x3F26 - voltage_value;
        current_voltage_exp = current_voltage_exp | 0x8000;
    }
```

```
    // voltage_value = 0x0D06;          // 3334*2^1(dec)
    // current_voltage_exp = 0x0100;    // 1(dec)
    // 3334 * 2^1 / 66670 = 0.1V

    ...
}
```

The voltage value has to be divided by a denominator of 66670 in order to correspond to the relationship from table 3.3. As well as for the voltage value, the current value has to be divided by a denominator of 80 in order to correspond to the relationship from table 3.2. This takes place one iteration later when the voltage value and accordingly the power value has to be adjusted to the voltage divider. Actually, the modification/editing of the measured current and voltage values has to be executed anyway whether the active power or the apparent power is required.

The representation of the power value with the registers `active_power`, `apparent_power` and `power_exponent` is similar to the representation of the measured values, depicted in figure 5.3. The momentary value of the active power can take negative values. Consequently, a sign bit is provided for the active power value.

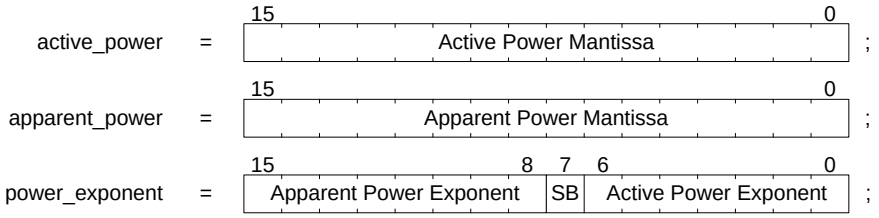


Figure 5.3: Power Value Registers

5.1.1 Active Power Calculation

Subsequently, after editing the received values, the 16×16 bit multiplication is executed. Details and characteristics considering multiplication can be found in section 5.3. The appropriate exponent has to be incremented each time one of the mantissas is shifted.

Now the 16 bit result represented by the mantissa and exponent has to be calibrated to the voltage divider with its division ratio of 3200. In the same step the value is divided by the denominator of $I\_scale = 80$ for the current value and by the denominator of $V\_scale = 66670$ for the voltage value. Out of equations 5.1 the total denominator can be calculated by

$$denominator_P = \frac{I\_scale \cdot V\_scale}{division\ ratio} = \frac{80 \cdot 66670}{3200} \approx 1667.$$

As the division is carried out with integer values the denominator is represented likewise.

```
void CALC_ACTIVE_POWER()
{
    /* after multiplication of: current_value * voltage_value */
    // 0x0320*2^0 * 0x0D06*2^1 = 0x0028B2C0*2^1
    // multiplication_mantissa = 0x5165;    // 20837(dec)
    // multiplication_exponent = 0x0008;    // 8(dec)

    /* division by 1667 */
    temp1 = multiplication_mantissa;
    temp2 = multiplication_exponent;
    temp3 = DENOMINATOR_P_MANTISSA; // 1667*2^0(dec)
    temp4 = DENOMINATOR_P_EXPONENT; // 0(dec)
    ...
    DIVISION();
    active_value = div_result_m;
    value_exponent = div_result_e;
    // active_value = 0x63FE;   // 25598(dec)
    // value_exponent = 0x000C; // 12(dec)
    // 25598 * 2^12 / 2^15 = 3199.75W

    ...
}
```

Note that every time the division operation is executed the result is represented to be multiplied by `2^15`.

Finally, the power values are divided by 80 and added up by subroutine CALC_AVERAGE_SUM_ACTIVE. Due to the representation of the result after the division operation the value 80 has to be represented as multiplied by 2^15 in the same way.

```
void CALC_AVERAGE_SUM_ACTIVE()
{
    /* active power / 80 */
    temp1 = active_value;
    temp2 = value_exponent;
    temp3 = AVERAGE_MANTISSA;    // 20480*2^7(dec)
    temp4 = AVERAGE_EXPONENT;    // 7(dec)
    // 20480 * 2^7 / 2^15 = 80
    ...
    DIVISION();
    active_value = div_result_m;
    value_exponent = div_result_e;
    // active_value = 0x4FFE;    // 20478*2^6(dec)
    // value_exponent = 0x0006; // 6(dec)
    // 20478 * 2^6 / 2^15 = 40.00W

    /* power[n] = power[n-1] + power[n] */
    temp1 = (power_exponent >> 7) & 0x0001; // sign bit summand 1
    temp2 = (value_exponent >> 7) & 0x0001; // sign bit summand 2
    temp3 = active_power;    // mantissa summand 1
    temp4 = active_value;    // mantissa summand 2
    temp5 = power_exponent; // exponent summand 1
    temp6 = value_exponent; // exponent summand 2
    ADDITION();
    active_power = sum_result_m;
    power_exponent = sum_result_e | (power_exponent & 0xFF00);
    // active_power = 0x4FFE;    // 20478*2^6(dec)
    // power_exponent = 0x0006; // 6(dec)
    // 20478 * 2^6 / 2^15 = 40.00W

    ...
}
```

In the course of this example with one value, the addition will lead to the same result as calculated by the division before. The entire power metering is averaged over 10 periods. With a sampling rate of $fs = 400\,Hz$, this cycle is therefore carried out 80 times.

5.1.2 Apparent Power Calculation

Generally, the calculation of the apparent power is based on adding the squares of current and voltage and finally extracting the square root. From a mathematical point of view, the product of the rms-values of current and voltage is obtained.

First of all, the current values as well as the voltage values have to be squared and added up. Due to the fact that the `MULTIPLY` subroutine is used more often, the registers to be multiplied have to be set before by the subroutine `CALC_I_SQUARE`. In the course of this example with one value, the result of subroutine `MULTIPLY` will be the same as for subroutine `CALC_SUM_ii`.

```
void CALC_SUM_ii()
{
    /* after multiplication of: current_value * current_value */
    // 0x0320*2^0 * 0x0320*2^0 = 0x0009C400*2^0
    // multiplication_mantissa = 0x4E20;    // 20000*2^5(dec)
    // multiplication_exponent = 0x0005;    // 5(dec)

    /* i^2[n] = i^2[n-1] + i^2[n] */
    ...
}
```

The same procedure takes place for the squares of voltages by the subroutines `CALC_U_SQUARE`, `MULTIPLY` and `CALC_SUM_uu`.

```
void CALC_SUM_uu()
{
    /* after multiplication of: voltage_value * voltage_value */
    // 0x0D06*2^1 * 0x0D06*2^1 = 0x00A99C24*2^B
    // multiplication_mantissa = 0x54CE;    // 21710*2^11(dec)
    // multiplication_exponent = 0x000B;    // 11(dec)

    /* u^2[n] = u^2[n-1] + u^2[n] */
    ...
}
```

The adding up of the individual values of current to the power of two and voltage to the power of two takes place according to the sequence in subroutine CALC_AVERAGE_SUM_ACTIVE.

After this cycle has been carried out over 10 line voltage periods, the product of the squares of current and voltage has to be calculated. In the course of this example the product of the squares is calculated immediately. In the same way as for the active power, the apparent power has to be calibrated to the voltage divider as well. The total denominator in order to calculate the apparent power is given by

$$denominator_S = denominator_P{}^2 = 1667^2 = 2778889. \tag{5.2}$$

The calibration of the apparent power takes place with the subroutine CALC_APP_POWER. After the division operation is executed the result is expected to be multiplied by 2^15.

```
void CALC_APP_POWER()
{
    /* after multipl. of: current_value^2 * voltage_value^2 */
    // 0x4E20*2^5 * 0x54CE*2^B = 0x19E15DC0*2^10
    // multiplication_mantissa = 0x6785;    // 26501*2^30(dec)
    // multiplication_exponent = 0x1E;  // 30(dec)

    /* division by 2778880 = 21710*2^7 */
    temp1 = multiplication_mantissa;
    temp2 = multiplication_exponent;
    temp3 = DENOMINATOR_S_MANTISSA; // 21710*2^7(dec)
    temp4 = DENOMINATOR_S_EXPONENT; // 7(dec)
    ...
    DIVISION();
    temp1 = div_result_m;
    temp2 = div_result_e;
    // div_result_m = 0x4E1E;   // 19998*2^24(dec)
    // div_result_e = 0x0018;   // 24(dec)
    // 19998 * 2^24 / 2^15 = 10238976(VA^2)

    ...
}
```

Afterwards, the root of the calculated value has to be extracted by the subroutine SQUARE_ROOT. A closer look is given in section 5.2.

Finally, the apparent power value has to be divided by 80 by using subroutine CALC_AVERAGE_APP, which corresponds to an averaged power value over 10 periods with sampling rate of $fs = 400\,Hz$. As it took place at the calculation of the active power, the denominator for calculating the apparent power is represented as multiplied by 2^15 as well.

```
void CALC_AVERAGE_APP()
{
    /* after extracting the square root */
    // 19998(dec)*2^(24)
    // sqrt_mantissa = 0x31FF;  // 12799*2^14(dec)
    // sqrt_exponent = 0x000D;  // 13(dec)
    // 12799 * 2^13 / 2^15 = 3199.75VA

    /* apparent power / 80 */
    temp1 = sqrt_mantissa;
    temp2 = sqrt_exponent;
    temp3 = AVERAGE_MANTISSA;   // 20480*2^7(dec)
    temp4 = AVERAGE_EXPONENT;   // 7(dec)
    // 20480 * 2^7 / 2^15 = 80
    ...
    DIVISION();
    apparent_value = div_result_m;
    value_exponent = div_result_e;
    // apparent_value = 0x4FFE; // 20478*2^6(dec)
    // value_exponent = 0x0006; // 6(dec)
    // 20478 * 2^6 / 2^15 = 40.00VA

    ...
}
```

Now the calculation of active power and apparent power has finished and subroutine `STOP_MEASUREMENT` saves the calculated values.

```
void STOP_MEASUREMENT()
{
    apparent_power = apparent_value;
    power_exponent = power_exponent & 0x00FF;
    power_exponent = power_exponent | (value_exponent << 8)

    // active_power = 0x4FFE;        // 20478*2^6(dec)
    // apparent_power = 0x4FFE;      // 20478*2^6(dec)
    // power_exponent = 0x0606;      // 6(dec) 6(dec)
    //   ACTIVE: 20478 * 2^6 / 2^15 = 40.00W
    // APPARENT: 20478 * 2^6 / 2^15 = 40.00VA

    ...
}
```

To summarize, receiving the appropriate command for power metering, the transceiver starts transmitting the commands in order to receive two 16 bit values of current and voltage. After the sensor has finished transmitting the data, the sequence in figure 3.6 is initiated and the data are edited in order to correspond to table 3.2 for currents and table 3.3 for voltages. The entire power calculation/metering is carried out over 10 line voltage periods with a sampling rate of $fs = 400\,Hz$. After the values for active power and apparent power are calculated, the protocol processor buffers the metering values represented by the mantissa and exponent for a later pick-up by the base station. Subsequently, the protocol processor activates the RX front end of the transceiver and waits for further commands, in order to either re-initiate a power measurement sequence or transmit the calculated metering data.

5.2 Extracting Square Roots by Heron's Method

As mentioned in section 3.3.5 the transceiver has its limitations regarding arithmetical operations. Thus, a way has to be found to extract the square root using just addition, subtraction and division operations.

In connection with planimetry difficulties, particularly with land surveying, the Babylonians developed a method approaching the solution method of quadratic equations. The method was recorded by cuneiform inscriptions from the time about 1700 B.C. in the age of Hammurapi. This method was taken up later, about 100 A.D., by a Greek Heron of Alexandria, and is often referred to as Heron's method. [Ziegenbalg *et al.* 2007]

The fundamental idea of this Babylonian method is based on the geometrical illustration to construct a quadrant with an area of a. As, by a given area a the side length $\sqrt{a}$ is given too. Now the attempt is to step-by-step approach a quadrant starting from a rectangle. [Ziegenbalg *et al.* 2007]

Assuming one side x_1 of a new rectangle is equal to the average value of the two sides (x_0 and y_0) of the basic rectangle, the second side y_1 has to be adjusted so that the area a of the new rectangle does not change. Now, the new rectangle with sides of length is given by

$$x_1 = \frac{x_0 + y_0}{2} \quad \text{and} \quad y_1 = \frac{a}{x_1}.$$

Summarizing these two equations, this iteration can be written in equation 5.3. [Ziegenbalg *et al.* 2007]

$$x_{n+1} = \frac{x_n + \frac{a}{x_n}}{2} \tag{5.3}$$

An example of the convergence of the square root of $a = 9$ with a start value of $x_0 = 4$ and three iterations is depicted below.

$$\begin{aligned}
x_1 &= \frac{4 + \frac{9}{4}}{2} = \frac{\frac{25}{4}}{2} = \frac{25}{8} = 3.125 \\
x_2 &= \frac{\frac{25}{8} + \frac{9}{\frac{25}{8}}}{2} = \frac{\frac{25}{8} + \frac{72}{25}}{2} = \frac{1201}{400} = 3.0025 \\
x_3 &= \frac{\frac{1201}{400} + \frac{9}{\frac{1201}{400}}}{2} = \frac{\frac{1201}{400} + \frac{3600}{1201}}{2} = \frac{2882401}{960800} \approx 3.
\end{aligned}$$

The algorithm to extract the square root is implemented in firmware with seven iterations with regard to the value representation with the mantissa and exponent. The calculation of the initial value x_0 is carried out simply by shifting the exponent by one bit to the right. This shifting operation is equivalent to halving the value $x_0 = \frac{a}{2}$ to be calculated.

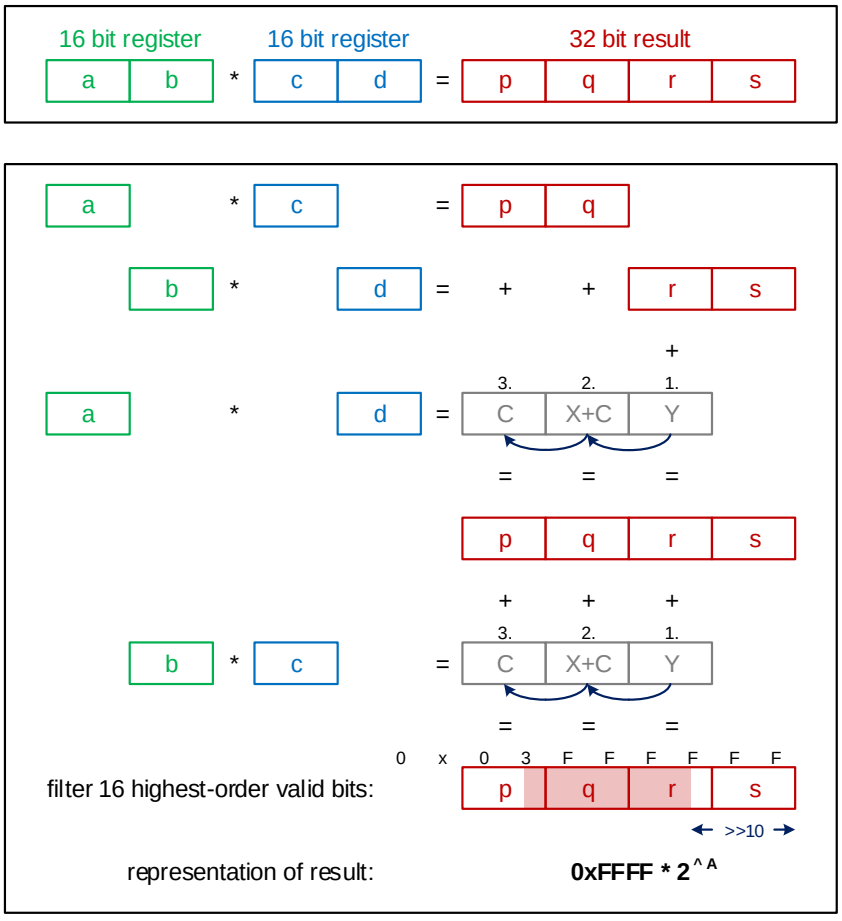
5.3 Implementation of Multiplication Algorithm

The transceiver has 16 bit wide internal registers. In the course of this illustration only integer values are observed. Generally for an integer multiplication the following applies.

factor 1	*	factor 2	=	product
m bit	*	n bit	=	(m + n) bit

Consequently, only 8 bit values can be multiplied with the built-in parallel multiplier without saturation. Therefore, every factor has to be shifted to the right until only eight valid bits are left.

In order to achieve the highest accuracy the multiplication is carried out by cascading the built-in multiplication operation. The fundamental idea is illustrated in figure 5.4 below.



a:b, c:d = factors, p:q:r:s = products, X:Y = intermediate, C = carry bit

Figure 5.4: Cascading of the Multiplication

A multiplication using powers of two is carried out by shifting the value, in other words the value is added to itself. The same applies for dividing by the powers of two, merely by shifting to the right. Finally, the 16 highest-order bits have to be filtered, corresponding with the mantissa. The amount of shifts are corresponding to the exponent. [Chemnitz 2004]

This cascaded multiplication leads to a 32 bit result. In order to save the calculated value in a 16 bit register, the 16 highest-order bits have to be filtered and accordingly shifted to the right. In the course of an example depicted in figure 5.4, a result of `0x03FFFFFF` has to be shifted 10 bit to the right and is represented by using mantissa `mantissa = 0xFFFF` and exponent `exponent = 0x000A`.

An example where two factors `0xAABB` and `0xCCDD` are multiplied this way is illustrated in figure 5.5 below.

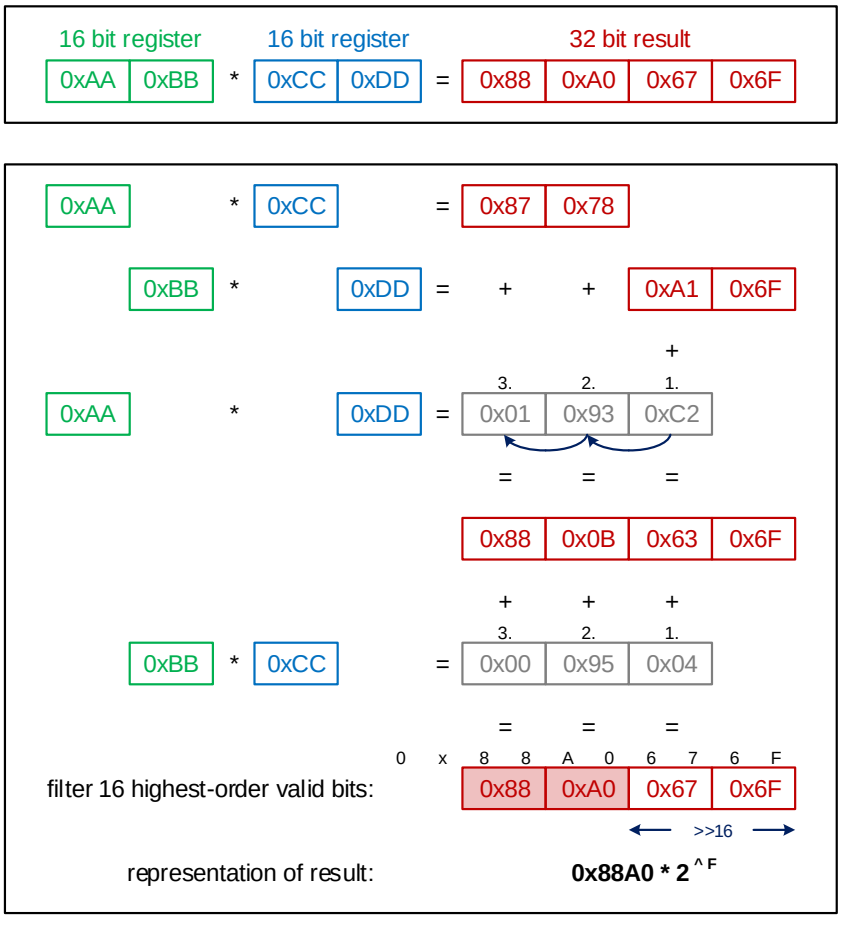


Figure 5.5: Cascading of the Multiplication, Example

In the first and second iteration a 8×8 bit multiplication of `0xAA*0xCC` and `0xBB*0xDD` takes place. These multiplications lead to a temporary result of `p:q:r` and to an end result of `s = 0x6F` (8 lowest-order bits). In the third iteration the multiplication of `0xAA*0xDD` is executed, leading to an intermediate of `X = 0x92` and to`Y = 0xC2`.

Afterwards, the following additions take place successively. In case a carry occurs at the operation `r = r+Y = 0xA1+0xC2 = 0x163`, the new temporary result for `q` has to be incremented `q = q+X+C = 0x78+0x92+0x01 = 0x10B`. The same applies for the addition of the new temporary result `p`. When, as in this case, a carry occurs again, the new temporary result for `p` has to be incremented `p = p+C = 0x87+0x01` in the same way.

Finally, the sequence with the intermediates `X` and `X` mentioned above has to be executed for the multiplication of `0xBB*0xCC`. The temporary results of `q = 0x0B` and `r = 0x63` are added by the intermediate of `X = 0x04` and `Y = 0x95`.

In the form of a pseudo code, the algorithm for cascading the multiplication can be described as follows:

```
void MULTIPLY()
{
    // factor1 * factor 2 = product
    // 16bit * 16bot = 32bit
    // a:b * c:d = ((a*c * 256) + a*d + b*c) * 256 + b*d

    p:q=a*c r:s=b*d
    X:Y=a*d r+=Y    q+=X+C  p+=C
    X:Y=b*c r+=Y    q+=X+C  p+=C

    // a:b, c:d = factors; p:q:r:s = product
    // X:Y = intermediate; C = carry bit
}
```

This principle works for floating point numbers as well, with regard to the value representation with the mantissa and exponent based on the law of mathematics.

Chapter 6

Measurements with Power Metering Unit

In this chapter a description of the measurement condition as well as measurement results are given. Section 6.1 focuses on the measurement conditions, including supply and the characteristics of the measuring object. In section 6.2 measurement results with regard to interpretation and accuracy are presented.

6.1 Measurement Condition

In order to perform measurements with the designed power metering unit, some issues have to be addressed. The unit has to be supplied as illustrated in figure 4.5, connecting live wire L to the side with the small $680\,pF$ safety certified capacitor. Only in this case is it ensured that the voltage between V_{diff+}, and accordingly V_{diff-} and the neutral wire N, may not exceed FELV. The entire unit has to be supplied as floating, either by battery or by potential-free voltage source.

Measurements were carried out with a $60\,W$ light bulb, assuming purely ohmic load. The instantaneous rms-values of current and voltage, for the sake of simplicity named I and V, were metered and the apparent power calculated. It has to be observed that the power dissipated by the load depends on the line voltage in accordance to the Ohm's law. The captured values, as well as the resulting dissipated apparent power S_{calc}, are depicted in table 6.1 below.

Light bulb $60\,W$		
$V\ [V]$	$I\ [A]$	$S_{calc}\ [VA]$
223	0.268	59.76

Table 6.1: Dissipated Apparent Power on $60\,W$ Light Bulb

The voltage values, measured by the external ADC of the sensor, were multiplied by firmware with a factor of 3200 (division ratio of the voltage divider) in order to correspond to line voltage.

At purely ohmic loads the active power should be equal to the apparent power, in other words the power factor should contain the value $cos(\varphi) = 1$. However, due to the time delay between sensing the current and voltage value (section 3.2.4), a virtual phase shift is introduced which leads to a mismatch between the active power and the apparent power, and consequently to a power factor $cos(\varphi) < 1$.

6.2 Measurement Results

In order to obtain information about the attainable accuracy and reliability of the captured power values, 50 measurements were acquired. Therefore, disturbing influences like the variance of line voltage and the involved voltage dependent power dissipation of the light bulb have to be observed. Additionally, note that statements about accuracy are related to a $60\,W$ light bulb. The reason for this is that measurements on a $100\,W$ light bulb would lead to a different accuracy because of the sensor resolution of $12.5\,\frac{mA}{LSB}$.

To summarize, the following implications of the measurement conditions are taken into account when looking at the measurement results:

- Variance of line voltage
- Voltage dependent power dissipation of the $60\,W$ light bulb
- Sensor resolution with $12.5\,\frac{mA}{LSB}$ and $48\,\frac{mV}{LSB}$ (including division ratio of voltage divider)
- Algorithm accuracy (measurement over 10 periods with $f_s = 400\,Hz$)

In 50 measurements, the minimum value x_{min}, the average value $\bar{x}$ and the maximum value x_{max} were calculated; they are presented in table 6.2 below. The power factor $cos(\varphi)$ was calculated by dividing the active power value by the apparent power value.

Light bulb $60\,W$			
Value	$P\ [W]$	$S\ [VA]$	$cos(\varphi)$
x_{min}	55.03	58.10	0.92
$\bar{x}$	56.60	60.04	0.94
x_{max}	58.56	62.88	0.95

Table 6.2: Minimum, Maximum and Average Value of 50 Measurements

Due to the fact that the calculation of the active power is not carried out correctly because of the entailed phase shift, statements according to accuracy are related to the apparent power.

The standard deviation or mean squared deviation s of the average value of apparent power $\bar{x}$ can be calculated by using following equation.

$$s = \sqrt{\frac{1}{n-1}\sum_{k=1}^{n}(x_k - \bar{x})^2} = 0.958\,VA$$

$$\pm 3s = \pm 2.874\,VA$$

Now, an assessment of accuracy can be estimated by using Gaussian distribution in combination with the standard deviation s. In metrology the Gaussian distribution describes the variance of the metered values. [Brasseur 2004]

According to the Gaussian distribution, $99.73\,\%$ of the metered values have an accuracy of at most $\pm 3s$ from its average value. [Brasseur 2004] In other words, with a light bulb of $60\,W$ the accuracy of the apparent power is approximately $\pm 4.4\,\%$.

The metered values of active power and apparent power can be seen in table 6.3; the power factor $cos(\varphi)$ is calculated by dividing the active power value by the apparent power value.

No.	$P\ [W]$	$S\ [VA]$	$cos(\varphi)$
1	57.18	60.14	0.95
2	55.85	59.16	0.94
3	56.70	61.51	0.92
4	56.64	61.42	0.92
5	55.47	59.71	0.93
6	55.55	59.66	0.93
7	56.90	60.08	0.95
8	56,76	60.05	0.95
9	55,70	59.68	0.93
10	57.82	60.78	0.95
11	55.88	59.84	0.93
12	56.49	59.71	0.95
13	57.32	61.44	0.93
14	55.27	58.54	0.94
15	56.64	60.04	0.94
16	57.09	60.22	0.95
17	55.74	59.11	0.94
18	56.58	59.71	0.95
19	56.13	59.35	0.95
20	56.35	59.41	0.95
21	55.99	59.22	0.95
22	55.27	61.36	0.93
23	58.36	61.53	0.95
24	56.59	59.86	0.95
25	56.96	60.25	0.95

No.	$P\ [W]$	$S\ [VA]$	$cos(\varphi)$
26	56.32	59.57	0.95
27	56.73	59.94	0.95
28	55.81	59.89	0.93
29	57.33	61.34	0.93
30	55.57	58.51	0.95
31	56.37	59.38	0.95
32	56.70	59.46	0.95
33	58.56	61.72	0.95
34	57.97	61.09	0.95
35	56.34	59.23	0.95
36	56.66	59.68	0.95
37	56.13	59.32	0.95
38	55.58	59.07	0.94
39	57.10	60.23	0.95
40	57.72	61.57	0.94
41	56.83	60.55	0.94
42	58.38	62.88	0.93
43	55.03	58.10	0.95
44	57.49	60.74	0.95
45	55.40	58.31	0.95
46	56.37	59.36	0.95
47	56.23	59.53	0.94
48	56.38	60.05	0.94
49	57.34	60.62	0.95
50	56.56	59.85	0.95

Table 6.3: Measurement Results of Active Power and Apparent Power

Chapter 7

Conclusion

This thesis is about the topic of power metering with a Hall-based Current Sensor, with focus on the hardware as well as the software design. This chapter summarizes the most important findings and provides a prospective on future work.

7.1 Summary and Results

The target of this thesis was the development of a power metering unit for $230\,V$ grid connected devices, embedded in a wireless monitoring node. The technical challenges are found in dividing the line voltage to a range the sensor can handle, implementing the single-wire interface to be as fast as possible and an algorithm in order to calculate the active as well as the apparent power.

First, a theoretical part, including the definition of the active power as well as the apparent power and how power can be calculated from a sampled signal, was introduced. A brief overview of the entire system architecture was given with focus on the current and voltage sensor and the multi-channel transceiver ASIC with its programmable protocol processor. The external wiring of the sensor and the flowchart are presented in order to perform current and voltage measurement. An introduction to the protocol processor and its limited language subset of the C compiler was given. The entire controlling functionality is taken over by the protocol processor containing the sequential control for single-wire communication, the calculation of the required power and additionally the stand-alone handling of the radio communication protocol.

The realization of the hardware design fulfills all requirements to measure the voltage. A first prototype PCB was developed, as can be seen in figure 4.1. The line voltage is stepped down by using an asymmetrical capacitive voltage divider with a division ratio of approximately 3200, with the advantage that the voltage may not exceed FELV. The drawback of this asymmetrical voltage divider configuration is that live wire L and neutral

wire N have to be known. A differential amplifier is used in order to provide a single-ended signal for the external voltage ADC of the sensor. Based on the simulation results further improvements according to requirements can be implemented with low effort, for example leading to a symmetrical configuration.

The implementation of the firmware presents special challenges in terms of the limited language subset of the C compiler and the characteristic number representation. The following main tasks were implemented:

- Single-wire communication interface with a bit transmission rate of $143\,\frac{kbit}{s}$
- On-the-fly calculation of active power and apparent power
  - Heron's method to extract square roots
  - Cascading the built-in multiplication operation
- Radio communication protocol handler

Power metering is carried out with a maximum sampling rate of $fs = 400\,Hz$ over 10 periods. Measurement results show an accuracy of $\pm 4.4\,\%$ at a light bulb of $60\,W$. The implemented algorithm can be adapted with low effort to related tasks (for example energy monitoring).

Using this first version of the sensor has its drawback. Power calculation is only performed correctly for the apparent power. The reason for this is because this algorithm calculates the rms-values of current and voltage. Due to the time consuming communication to the sensor (switching between current and voltage measurement) a virtual phase shift is introduced. This leads to an incorrect result of the active power. In the case of a constant phase shift the result could be corrected by a correction factor. In a different phase shift this correction factor would lead to an incorrect result as well. Due to lack of time no further observations took place regarding the correction of the metered apparent power values, and accordingly, the entailed phase shift by firmware.

Appendix A

Appendix

A.1 Small PCB of the Power Metering Unit

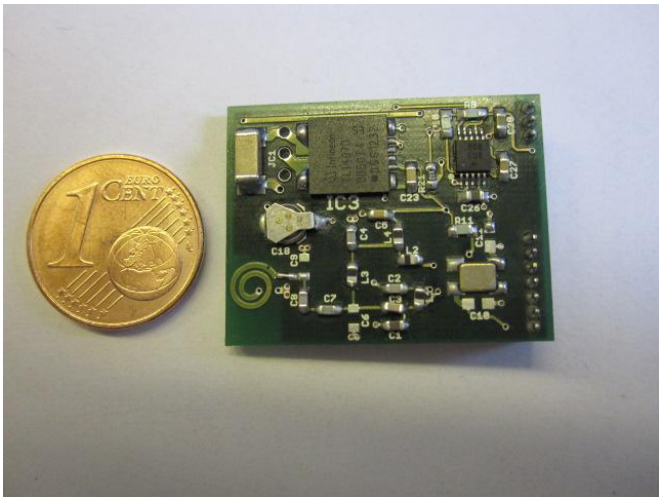


Figure A.1: Small PCB of the Power Metering Unit

A.2 AC Plug Demonstrator

Base Station: PIC32 μC and Power Metering Node with TRX only

- Serial Interface to PC: Transmits Commands to Power Metering Node via RF link

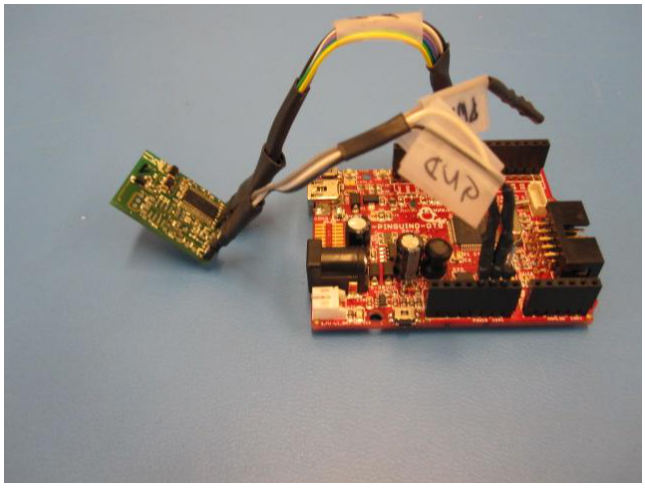


Figure A.2: Base Station

Power Metering Node fully equipped: waiting for Commands from Base Station

- TRX $+$ Sensor
- $60\,W$ "heat bulb"

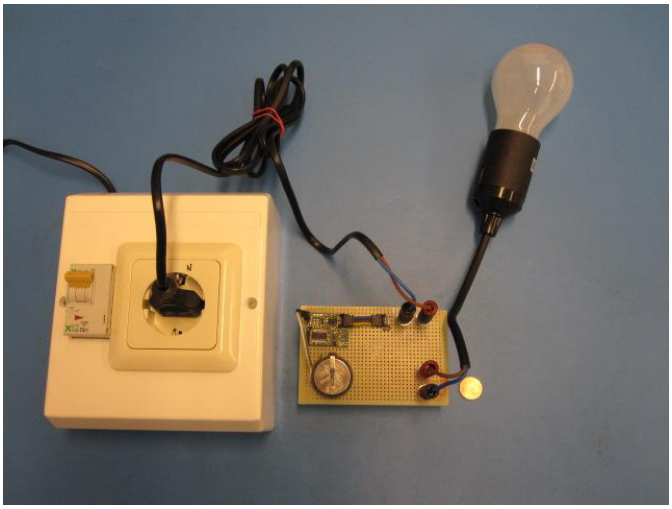


Figure A.3: Power Metering Node

A.3 AC Plug Demonstrator - Results

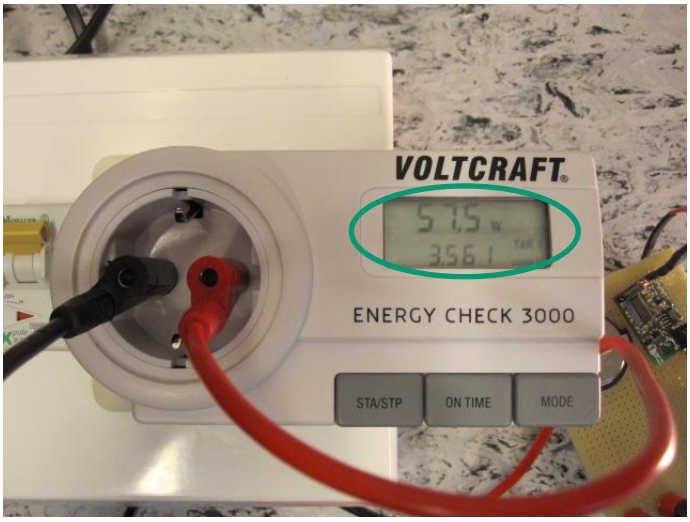


Figure A.4: Measured Power at Plug

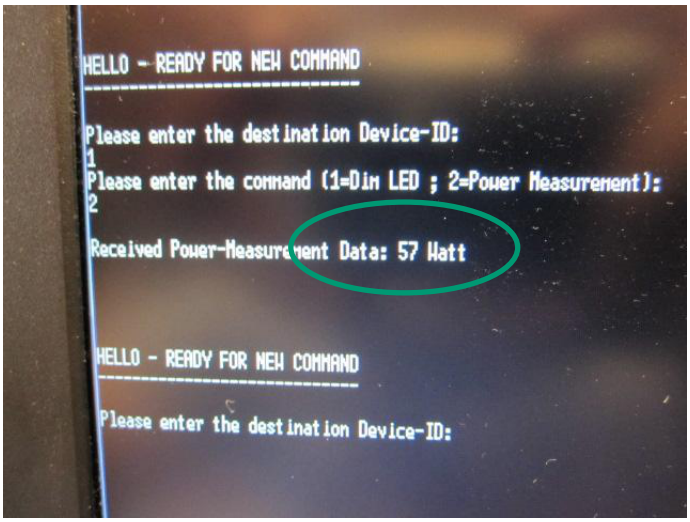


Figure A.5: Monitored Power from Metering Node

A.4 LED Module

Figure A.6: Power Metering Node integrated into a LED Module, with Power Metering and Dimming Functionality

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