A 100 kHz Voltage Controlled Oscillator Embedded in a Power Management Unit for Ultra Low Power Sensor Nodes

Peter Unterkircher

F 716 - 0430203

Institute for Electronics

Graz University of Technology

Head: Univ.-Prof. Dipl.-Ing. Dr. techn. Wolfgang Pribyl

Supervisor: Dipl.-Ing. Dr.techn. Mario Auer

External Supervisor: Dipl.-Ing. Markus Dielacher

Graz, Oct 2010

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Die Entwicklung von gesteuerten Oszillatoren in Smart Transceivern spielt eine wichtige Rolle während des Entwurfs von Low Power Wireless Sensor Networks. In dieser Arbeit wird eine Topologie für einen RC-Oszillator vorgestellt, der mit einer geeigneten Schaltung zur Kalibrierung der Frequenz ausgestattet ist. Die Kalibrierung dient dem genauen Aufwecken einer State Machine und eines Quarz Oszillators nach einer einstellbaren Zeit. Die Frequenz des RC-Oszillators kann mit Hilfe eines digitalen 6-bit Codewortes eingestellt werden.

Der Oszillator soll als Real Time Clock eine kleine State Machine takten. Die angepeilte Frequenz ist 100 kHz und der Oszillator darf über einen Temperaturbereich von -40°C bis 125°C nicht mehr als ±7% von dieser Frequenz abweichen. Die Versorgungsspannung ist 1.5 V und der Oszillator wird in einer 0.13 μm CMOS Technologie realisiert. In dieser Arbeit werden verschiedene Topologien auf ihre Tauglichkeit für diese Applikation untersucht und verglichen.

Abstract

The design of controlled oscillators in smart transceivers plays an important role in the design process of low power wireless sensor networks. In this work an oscillator topology is presented, which includes a mode to calibrate the frequency of the oscillator. The calibration enables precise wake-up cycles of a state machine and a quartz oscillator. The frequency of the oscillator can be adjusted using a digital 6-bit code word.

The oscillator clocks a small state machine. The target frequency is 100 kHz and the oscillator is not allowed to drift by more than $\pm 7\,\%$ of this frequency in a temperature range from -40°C to 125°C. The supply voltage is 1.5 V and the oscillator is implemented in a 0.13 μm CMOS technology. In this thesis several oscillator topologies are investigated and compared in order to find a topology suitable for the application.

Acknowledgement

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Peter Unterkircher

Contents

1 Introduction

This work emerges from the framework of the project **C**ooperative **H**ybrid **O**bjects **Se**nsor **N**etwork (CHOSeN). The objective of CHOSeN is to develop innovative sensor network structures with associated sensor nodes. In particular these sensor networks should be adapted to system health monitoring.

1.1 Motivation and Main Idea

System health monitoring is an approach to optimize maintenance of products, making their operation and usage safer, more cost effective, and more predictable. The underlying idea is that components are monitored continuously during their life time, their condition is estimated and decisions on maintenance schedules are derived based on a system-wide joint decision making process. For these characteristics to work, system health monitoring enables a predictive maintenance [1].

Efficient and effective system health monitoring needs to be integrated at different levels and to different systems and system configurations.

The aim of CHOSeN is to improve system health monitoring by providing a wireless communication infrastructure that is flexible, easy to program and deploy, reliable, scalable solutions and works on low-power [1].

1.2 Wireless Sensor Networks (WSN) for Automotive

Wireless Sensor Networks (WSN) have attracted increasing attention in recent years. The application range of these WSNs is very wide, including environmental monitoring, structural health monitoring in buildings, health and fitness monitoring, and automotive and aeronautic applications (just to name a few) [2]. The sensors and actuators in automotive environments have to fulfill the main requirements:

- Low cost
- Low power consumption
- High robustness

- High reliability

The approach of utilizing WSN technology seems to be promising for the following reasons:

- A non negligible impact in the reduction of the amount of in-vehicle wires and thus on costs, due to materials and maintenance.
- The extra-cost due to the increase of nodes is much less than the one required for standard wired technologies.
- Wireless energy transfer or local energy scavenging gives rise to a perspective of completely wireless networks (both data and power).

1.3 Scientific and Technical Objectives

The scientific and technical objective of the project is the development and realization of market conform, adaptive wireless network topologies and "data per energy" optimizing communication devices.

The platform of smart wireless transceivers is focused on significantly improving the major shortcomings of state of the art WSN architectures. The goal is to bridge the existing gap between platform abilities and application-requirements in terms of:

- Flexibility
- Responsiveness
- Reliability and robustness of communication
- Energy autonomy

Sensor nodes are highly heterogeneous Systems on Chip (SoCs) or Systems in Package (SiPs) with a variety of tightly interacting HW/SW, digital, analogue/mixed signal and radio frequency (RF) sub-systems. A state of the art ZigBee [3]-type node is shown in Fig. 1.

The integrated sensor node will provide significantly more flexibility, with the results of the CHOSeN project.

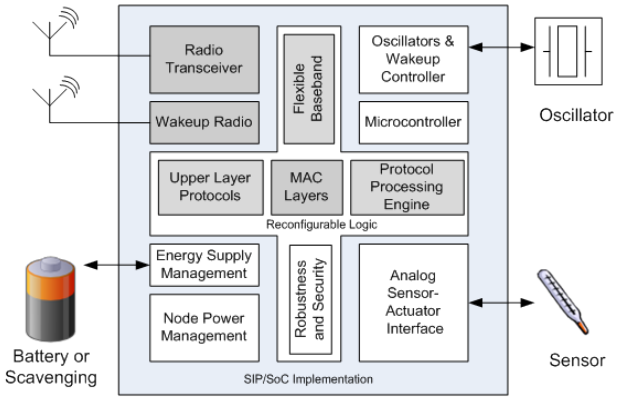

Figure 1: CHOSeN sensor node [1]

Our first objective is to develop an ultra low power scalable and reconfigurable transceiver, which has to fulfill requirements that are not satisfied by state of the art wireless sensor node platforms. The gray blocks which are highlighted in Fig. 1 are within the main project objectives and are significantly beyond state of the art WSNs.

In this work the main focus is put on the design of the real time clock (RTC), which is responsible for precise wake up cycles of the transceiver. The main objective of this "wake up" is saving power of the tranceiver. Therefore the RTC should consume as little power as possible while showing an adequate time resolution.

2 Low Power Design

One of the major challenges in the design of a sensor node is its power consumption. A sensor node has to be cheap and small, while the required lifetime is very high. After it is deployed, a sensor node should work for up to ten years without changing its battery. This requirement is obvious for sensor nodes which are installed for example inside the walls of a building to detect cracks or monitor the structural integrity of the building. In such a case it is impossible to change batteries and other energy sources have to be considered. The power delivered by energy harvesting devices which convert different sources of energy into electrical energy is only in the range of a few μW [4]. That is why a sophisticated power management is mandatory in order to keep the average power consumption below this limit [5].

2.1 Power Management Unit

The developed transceiver is divided into different power domains. An overview is given in Fig. 2. Every power domain can be switched off or on separately when needed. In this way it is possible to implement very energy efficient *Power Down* and *Deep Sleep* states. The supply voltage of the ASIC is 3.3 V, however some of the building blocks require a supply of 1.5 V. For this purpose a number of voltage regulators are integrated on chip and activated when the corresponding power domains are active. In *Power Down* only the asynchronous wake-up unit is active. This block is able to detect external events and wakes up the transceiver. In addition in *Power Down* the chip can only be woken up by an external event since every other part is off. Additionally the attachment of a battery is detected as an event which activates the transceiver. Besides the *Power Down* state, the transceiver supports four different *Deep Sleep* states in which the power consumption is also only in the range of a few μW as shown in Table 1. In *Deep Sleep*, not only the asynchronous wake-up unit, but also a power state controller (PSC) is active. The PSC is a small state machine, which can wake up the main state machine of the transceiver after a defined *Deep Sleep* time. In *Sleep* Mode the main state machine keeps control over the system, and only the RF parts

State	RTC	RAM	Power Consumption
Deep Sleep 1	*on*	*on*	$<2.5\,\mu$W
Deep Sleep 2	on	off	$<2.2\,\mu$W
Deep Sleep 3	off	on	$<1.3\,\mu$W
Deep Sleep 4	off	off	$<1\,\mu$W
Power Down	off	off	$<0.3\,\mu$W

Table 1: *Deep Sleep* states with anticipated power consumption[5]

are switched off. Of course the power consumption in *Sleep* is much higher than in *Deep Sleep* Mode. The PSC is clocked by a low power real time clock (RTC), which is the core of this work and described in Chapter 4. Besides the RTC also the RAM of the transceiver is in the same power domain as the PSC. In this way the state of the transceiver is retained in *Deep Sleep.* Thus, the transceiver can resume its operation after *Deep Sleep* mode. RTC and RAM can be switched on and off separately, resulting in four different *Deep Sleep* states which are shown in Table 1. From a functional point of view, *Deep Sleep 4* is equivalent to *Power Down*, however the power consumption is different. In *Deep Sleep 4* a low power bandgap and a low power voltage regulator are active, which are deactivated in *Power Down.* That is why *Deep Sleep 4* is only used for measurement purposes and does not have any relevance for the application [5].

2.2 This Work

This work describes the implementation of the ultra low power RTC to clock the PSC. The RTC should consume less than 1 μA at a frequency of 100 kHz. An important feature is the long term stability of the frequency. The phase jitter is of secondary concern. To calibrate this clock to the more precise quartz oscillator a register is used.

The tuning word stored in this register switches current sources or capacitors (or any kind of tuning apparatus) to guarantee the right frequency. When the quartz is running, it stores a calibrated digital word in this register, which is processed by the RTC. Another important feature is the defined start-up behavior of the oscillator, because it clocks an asynchronous counter

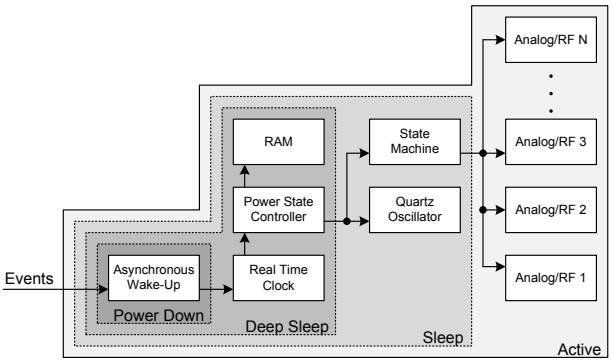

Figure 2: Power Management Unit [5]

and a synchronous control-logic which is susceptible to spikes on the clock input [5].

Requirements

- Temperature Range: -40°C - 125°C
- Frequency: 100 kHz ±7% over Temperature Range
- Current consumption: $<1\,\mu A$
- Long-term-stability: ±7 % over Temperature and Supply
- Trim-error: ±2 % (with a Process and Temperature Error of ±30 % we need a register of at least 5bits).
- Time-error: ±2 % in timing error (or ±1.2 seconds over one minute)

2.3 Weak Inversion, Subthreshold Conduction

The subthreshold region has attracted increasing attention in finding the limits of MOS transistor circuits. Packaging densities and refresh times in dynamic memory circuits have also been investigated [6]. A main issue in electronic industry has become low power consumption for many product areas such as cellular telephones, portable personal computers, biomedical implants all battery powered devices.

If we reduce V_{GS} voltage of a MOS transistor below the threshold voltage defined by the strong-inversion, the channel current decreases approximately exponentially. This so-called subthreshold region, is defined by a weakly inverted channel [6]. For long-channel devices, the subthreshold drain to source current can be expressed as [7].

$$I_{\mathrm{D}} = I_{\mathrm{D0}} \cdot (exp\frac{V_{\mathrm{GS}} - V_{\mathrm{B}}}{n \cdot \phi_{\mathrm{T}}}) \cdot (1 - exp\frac{-V_{\mathrm{DS}}}{\phi_{\mathrm{T}}}) \quad (1)$$

where I_{D0} denotes the saturation current of the transistor in weak inversion, $\phi_{\mathrm{T}} = k \cdot T/q$, and $n = 1 + C_{\mathrm{Dep}}/C_{\mathrm{ox}}$ [8]. Eq. 1 shows interesting properties of the weak inversion. First if V_{DS} exceeds a few ϕ_{T}, I_{D} becomes independent of the drain source voltage and with $V_{\mathrm{B}} = 0$ Eq. 1 reduces to Eq. 2. The second property, under this condition the slope of I_{D} on a logarithmic scale equals [8]

$$\frac{\partial(log_{10} I_{\mathrm{D}})}{\partial V_{\mathrm{GS}}} = (log_{10} e) \cdot \frac{1}{n \cdot \phi_{\mathrm{T}}}.$$

The inversion of this term is often called the "subthreshold slope S", [8]:

$$\begin{aligned} S &= 2.3 \cdot \phi_{\mathrm{T}} \cdot (1 + \frac{C_{\mathrm{Dep}}}{C_{\mathrm{ox}}}) \; [V/Dec] \\ I_{\mathrm{D}} &= I_{\mathrm{S}} \cdot \frac{W}{L} \cdot e^{\frac{V_{\mathrm{GS}}}{n \cdot \phi_{\mathrm{T}}}}. \end{aligned} \quad (2)$$

Eq. 2 strongly reminds of the behavior of a bipolar transistor. Indeed it is similar to the $I_{\mathrm{C}}/V_{\mathrm{BE}}$ relationship of this device, except for the nonideality factor n which comes from the capacitive voltage divider between C_{Dep} and C_{ox} as seen in Fig. 3 which divides the gate-voltage to be effectively used in Eq. 2.

$$n = \frac{C_{\mathrm{Dep}} + C_{\mathrm{ox}}}{C_{\mathrm{ox}}}.$$

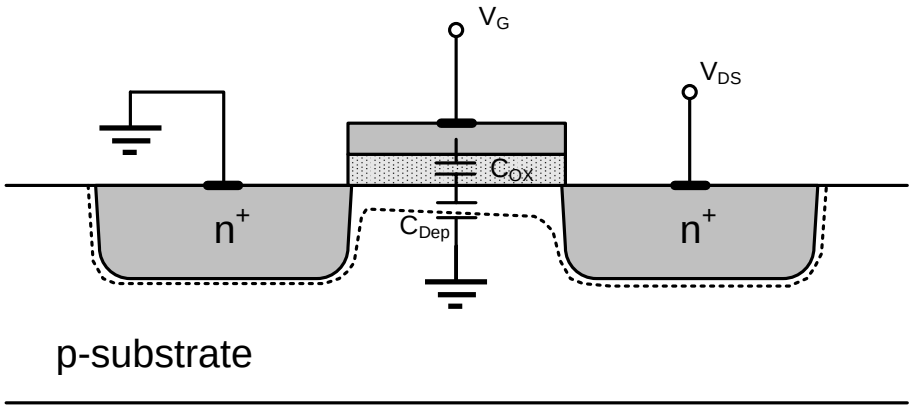

Figure 3: Indication of the factor n

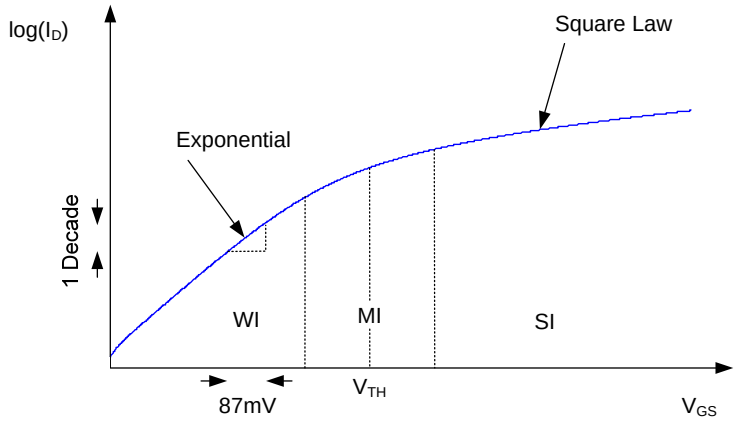

Figure 4: Drain-current of a MOS-transistor sweeped over the gate-source voltage [8]

Typically n lies in the range between 1 and 1.5. A key point here is that as V_{GS} falls below V_{TH}, the drain current drops at a finite rate. If we assume typical values of n, at room temperature V_{GS} must decrease by about 80 mV for I_{D} to decrease by one decade.

For example in a certain process to allow low-voltage operation a threshold of 0.3 V is given. If we reduce V_{GS} to zero the drain current decreases by only a factor of $10^{0.3/0.08} = 10^{3.75} \approx 5623$ [8].

Weak inversion operation in MOS transistors can be used to implement interesting circuits, especially for low power application. In this work the main focus lies on building such circuits with transistors biased in weak

inversion. For this reason matching has also to be considered.

2.4 Matching in Weak Inversion

Due to the fact that we are operating with low currents in this work, about 10nA, it is really difficult to bias a transistor in strong-inversion. For example if we take a $K' = 160\,\frac{\mu A}{V^2}$ and an overdrive voltage $V_{\mathrm{ov}} = 200\,mV$ [8],

$$I_{\mathrm{D}} = \frac{K'}{2} \cdot \frac{W}{L} \cdot V_{\mathrm{ov}}^2$$

we would need a $\frac{W}{L}$ ratio of 0.003125 or if we use a width $W = 1\,\mu m$ a length of $313\,\mu m$ has to be chosen. This means there is a huge dissipation in area and on top of that we receive a big capacitor build by the transistor. Therefore it is better to let the transistor operate in weak inversion. To get a feeling for the mismatch in the drain currents of different transistors we can use the first-order Taylor approximation of a drain-current model [9]:

$$I_{\mathrm{D}} = f(P_1, P_2, \cdots) \tag{3}$$

$$\frac{\Delta I_{\mathrm{D}}}{I_{\mathrm{D}}} = \frac{1}{I_{\mathrm{D}}}\frac{\partial I_{\mathrm{D}}}{\partial P_1}\Delta P_1 + \frac{1}{I_{\mathrm{D}}}\frac{\partial I_{\mathrm{D}}}{\partial P_2}\Delta P_2 + \cdots . \tag{4}$$

$\Delta I_{\mathrm{D}}/I_{\mathrm{D}}$ is the relative difference of the drain currents of two devices. Parameters $(\Delta P_1, \Delta P_2, \dots)$ describe the mismatch in the drain-current model parameters.

2.4.1 Threshold Voltage Mismatch

Together with Eq. 4 we obtain two formulas [9]:

$$\left.\frac{\Delta I_{\mathrm{D}}}{I_{\mathrm{D}}}\right|_{\Delta V_{\mathrm{TH}}} = \frac{1}{I_{\mathrm{D}}}\frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{TH}}}\Delta V_{\mathrm{TH}} = -\frac{g_{\mathrm{m}}}{I_{\mathrm{D}}} \cdot \Delta V_{\mathrm{TH}}$$

$$\left.\frac{\Delta I_D}{I_D}\right|_{\Delta V_{GS}} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_{GS}}\Delta V_{GS} = \frac{g_m}{I_D} \cdot \Delta V_{GS}.$$

The mismatch in weak inversion is calculated using Eq. 2 :

$$\left.\frac{\Delta I_{\mathrm{D}}}{I_{\mathrm{D}}}\right|_{\Delta V_{\mathrm{GS}}} = \frac{1}{I_{\mathrm{D}}}\frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{TH}}}\Delta V_{\mathrm{GS}} = \frac{I_{\mathrm{D}}}{I_{\mathrm{D}}}\cdot\frac{1}{n\phi_t}\cdot\Delta V_{\mathrm{GS}} = \frac{1}{n\phi_t}\cdot\Delta V_{\mathrm{GS}}.$$

This result means that the relative mismatch in weak inversion is about a factor 3 higher than in strong inversion, if we assume $1/(n\phi_T) = 30$ in weak inversion and $g_m/I_D = 10$ in strong inversion. Thus to get the same mismatch between the drain currents of two devices of these two regions we have to enlarge the area of a transistor by a factor of 9. This is also evident when the exponential curve is considered in weak inversion, a voltage mismatch results in an exponential current mismatch [9].

3 Oscillators

Oscillators are essential part in electronic systems. The application ranges from clock generation in digital circuits to carrier synthesis in RF-tasks. The requirements are vastly different from application to application, therefore a need for different oscillator topologies and performance parameters is evident. Robust, high- performance oscillator design in CMOS technology continues to reveal interesting challenges. The focus in this work lies on an oscillator design with medium frequency and excellent temperature-independency. To accomplish such an oscillator, the circuit must interact with the bias-current. In our case, to perfectly cancel the temperature-behavior of the bias-current we have to produce a term that cancels for that temperature-response.

One of the most commonly used oscillators in todays microelectronics is the ring oscillator. It is described in Section 3.2. The slower version the current starved ring-oscillator is presented in Section 3.2.1. Another promising oscillator is the relaxation oscillator presented in [10] in Section 3.4. The oscillator presented in [11] was actually used in a former design at Infineon Design Center Graz, therefore its ability for this application was investigated in Section 3.3. But the oscillator based on the relaxation principle presented in [5] seemed to be the most promising topology for the application of a temperature stable RTC.

3.1 General Considerations

An oscillator is a kind of feedback amplifier. It produces a periodic output, usually in the form of voltage. As found by Barkhausen [12] a feedback system must feed back an adequate signal with the right phase shift to sustain oscillation. Consider the feedback system illustrated in Fig. 5 [8],

$$\frac{V_{\text{out}}(s)}{H(s)} = V_{\text{in}}(s) - V_{\text{out}}(s)$$

which gives a unity gain response [8]

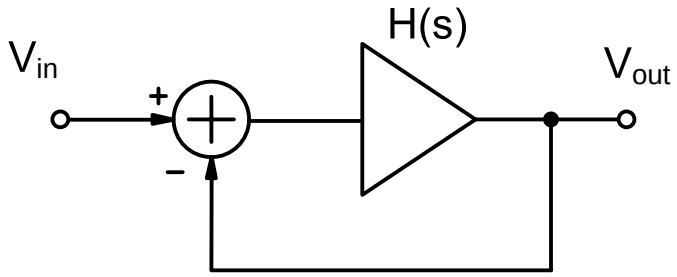

Figure 5: Feedback system [8]

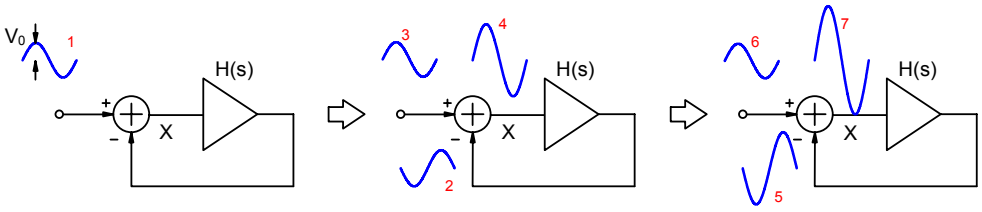

Figure 6: Conceptual evolution of oscillation [8]

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) \quad = \quad \frac{H(s)}{1+H(s)}.$$

If at high frequency the amplifier experiences sufficient phase shift that the overall feedback becomes positive, then oscillation may occur. Precisely speaking, if for $s = j\omega_0$, $H(j\omega_0) = -1$, then the closed-loop gain approaches infinity at ω_0 . At this frequency the amplifier reinforces any noise component at the input of the amplifier or any other noise source in the signal path thus can trigger oscillation. In fact, as conceptually shown in Fig. 6 a noise component is fed back with unity gain and a phase-shift of 180°, returning to the substractor as a negative replica of the input. The substractor then gives a larger difference which in addition is also phase-shifted and fed back. Thus, the circuit continues to "regenerate," allowing the component at ω_0 to grow. For the oscillation to begin, the loop gain has to be unity or greater. Let us express the substractor's output in Fig. 6 by V_x as a geometric series (if $\angle H(j\omega_0) = 180°$) [8]:

$$
\begin{aligned}
V_{x0} &= V_0 \\
V_{x1} &= V_{x0} \cdot H(s) + V_0 \\
V_{x2} &= V_{x1} \cdot H(s) + V_0 \\
V_{x3} &= V_{x2} \cdot H(s) + V_0 \\
&\vdots \\
V_x &= V_0 + \mid H(j\omega_0) \mid \cdot V_0 + \mid H(j\omega_0)^2 \mid \cdot V_0 + \mid H(j\omega_0)^3 \mid \cdot V_0 + \cdots
\end{aligned}
$$

if $\mid H(j\omega_0) \mid > 1$, the above summation diverges however if $\mid H(j\omega_0) \mid < 1$, then

$$
V_x = \frac{V_0}{1 - \mid H(j\omega_0) \mid} < \infty.
$$

To put all together in the famous "Barkhausen criteria", the loop gain of a negative-feedback amplifier satisfies two conditions [8]:

$$
\begin{aligned}
\mid H(j\omega_0) \mid &\geq 1 \\
\angle H(j\omega_0) &= 180^\circ
\end{aligned} \tag{5}
$$

therefore oscillation may occur at ω_0. According to the "Barkhausen criteria" these conditions are necessary but not sufficient. To account for temperature variation and process variation we typically choose the gain at least twice or three times the required value. We may state that Eq. 5 is valid for amplifiers which have an inherently negative feedback at DC as in Fig. 5. But as depicted in Fig. 7 the overall phase-shift is always 360° to sustain oscillation. All three feedback-systems sustain oscillation and thus are equal in terms of the second criterion. The difference between the latter two systems in Fig. 7 is that the second open-loop amplifier contains enough stages to produce a phase-shift of 360° at ω_0, whereas the third one provides no phase-shift at ω_0 [8].

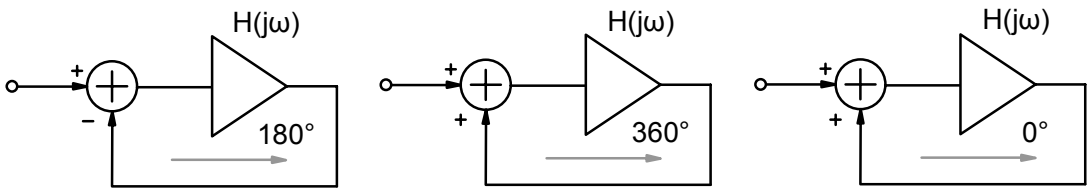

Figure 7: Various feedback systems [8]

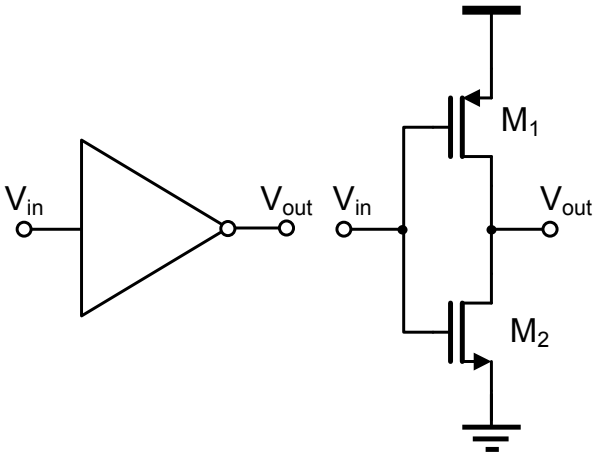

Figure 8: Inverter Symbol and simple implementation

3.2 Ring Oscillator

A popular way of realizing digital-output MOS Voltage Controlled Oscillators (VCOs) is to use a ring oscillator and add an apparatus for voltage control. A single-ended ring oscillator is realized by placing an odd number of inverting amplifiers in a feedback loop. A rather simple type of amplifier to be used is a digital inverter. This circuit is a form of negative feedback. Since a digital inverter, as seen in Fig. 8, has approximately 90° phase-shift at its unity-gain frequency it can be used as one element of a ring oscillator. A ring oscillator with three CMOS inverters is shown in Fig. 9. Assuming all loads of the stages are matched and at least three stages in the ring, a phase-shift of 180° can be established at a finite frequency.

The conceptual evolution of an oscillation in a ring oscillator using CMOS inverters is shown in Fig. 10. First, a noise component is introduced in the circuit and the oscillation can start. The circuit at first introduces only little

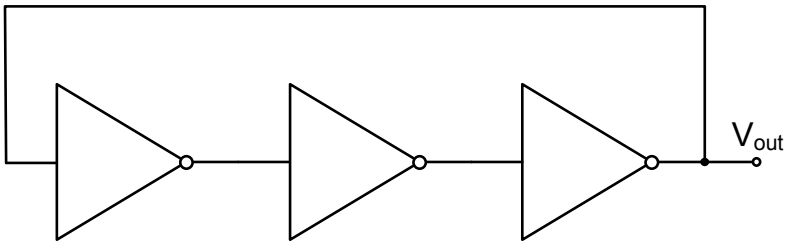

Figure 9: Ring oscillator realized using three digital inverters

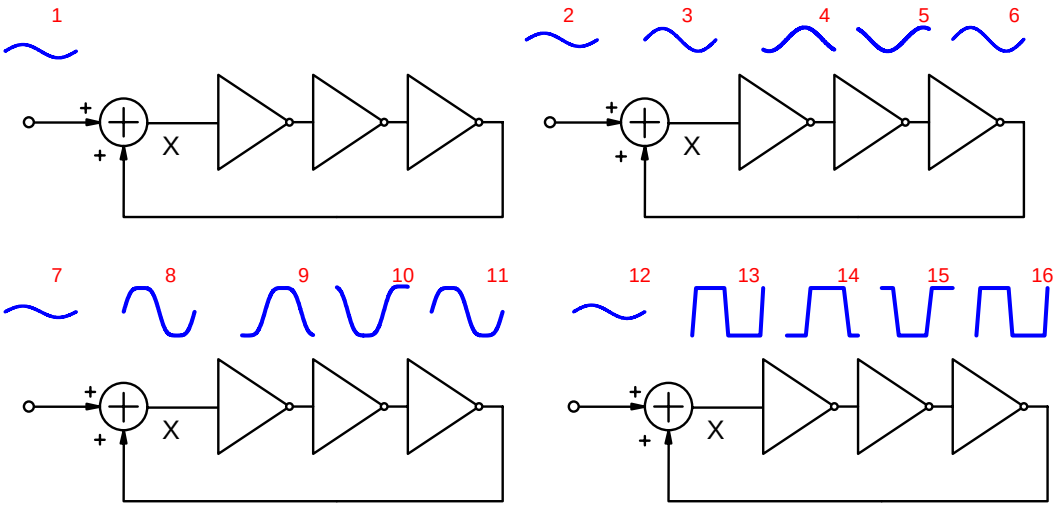

Figure 10: Evolution of oscillation in a ring oscillator using CMOS inverters

distortion due to vibrating around the operating point. But as oscillation is beginning to grow some distortion is introduced. Finally as we do not use an "anti-clip circuit", the wave introduces much distortion and an almost rectangular wave appears due to clipping or reaching the supply rails, respectively.

By analyzing the criteria in this circuit we see that the three inverters inherently have a dc-phase-shift of 180° but to reach the required 360° as seen in Fig. 7 we need "high-frequency phase-shift" of another 180°. To reach this it is seen that each of the inverters has to pay 60° of phase-shift (assuming the inverters load capacitors are matched). The number of stages in a ring oscillator is determined by a number of requirements, including power dissipation, speed, noise immunity, phase jitter, etc.

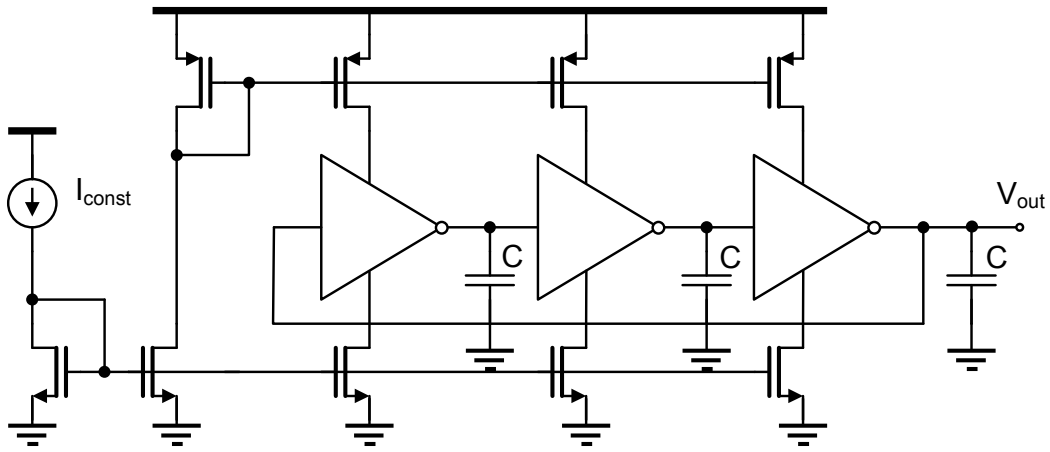

Figure 11: Current starved ring oscillator

3.2.1 Current Starved Ring Oscillator

In most applications three to five stages provide optimum performance, considering differential implementation. But in our case we want a ring-oscillator oscillating at a much lower frequency than $1/(2 \cdot n \cdot T_D)$ where n defines the number of stages and T_D the delay time of one CMOS inverter, respectively. Hence a ring-oscillator with current-starved inverters is implemented as seen in Fig. 11. The circuit works as follows: The current I_{const} is loading the capacitor C and hence defines the delay time through the ring.

$$\begin{aligned} V_{DD} \cdot C &= T_D \cdot I_{const} \\ T_D &= \frac{V_{DD} \cdot C}{I_{const}}. \end{aligned}$$

As seen in Fig. 11 a current which is temperature independent is used to obtain an almost cancelation of the temperature. But since our whole system should work with a small area and little current, we do not have space for a bandgap reference which offers a temperature-independent current, due to additional resistors which lie in the range of $M\Omega$ and hence consume a lot chip area. Therefore we have to search for alternative solutions to obtain a temperature-independent oscillator.

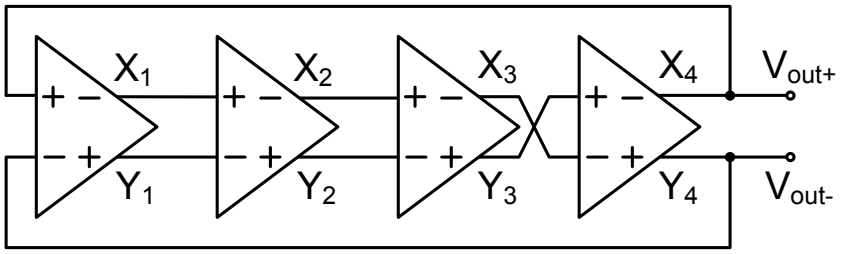

Figure 12: Differential ring oscillator using four stages

3.2.2 Differential Ring Oscillator

Ring oscillators with more than three stages are also feasible to implement. With single ended inverters the number of stages has to be odd. But if we are able to choose one stage which is not inverting we can also use an even number of stages. This can be achieved in a differential oscillator, seen in Fig. 12 where the last stage is crossed coupled and does not have a dc-inversion.

3.3 Popovic Oscillator

This Section describes an oscillatior based on a Fabre-Normand current conveyor as is presented in [11].Before we can study the behavior of the oscillator, we have to get a feeling for the Current Conveyor, the underlying circuit for this oscillator. To adapt the oscillator in [11] for this work we have to investigate how it works and how an oscillation frequency can be made temperature stable.

Fundamentals of Realization of Current Conveyor Type II (CCII) The CCII can be considered as an ideal transistor, either bipolar or MOS. To get a feeling for it, consider the NMOS transistor shown in Fig. 13. [13] If it is ideal its V_{GS} can be zero and its g_{m} is almost infinite. To make such a circuit work it needs some kind of feedback. The Current Conveyor can be compared to a voltage controlled current source (VCCS). But the differences are that a current supplied to terminal Y is conveyed directly to terminal Z, thus the impedance level of Y and Z are vastly different, as in a bipolar transistor. However in a VCCS the same current flows from Z to Y and the

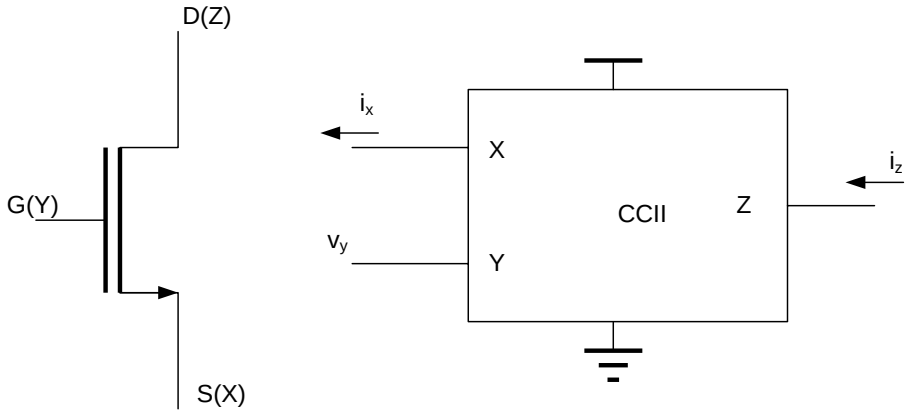

Figure 13: Comparison of a NMOS transistor and Current conveyor type two (CCII) [13]

impedance levels are also the same. Whereas in a Current Conveyor a copy of the current in Y flows in terminal Z. A bipolar transistor can be seen as a current conveyor but with the difference that its input differential voltage V_{GS} is not zero and its transconductance g_{m} is not infinity.

A Voltage applied to the gate of a current conveyor results in an equal voltage at its source.The gate terminal would result in an open terminal, but the source terminal would exhibit zero input impedance, this is because the gate is steering the source, while the source is steering current through from drain to source. Important to note, that a current injected at the source would be conveyed to the drain where the impedance level would be infinite (just as the terminal Z in the conveyor). This means that an ideal transistor behaves as a negative current conveyor (CCII) [13].

3.3.1 Current Conveyor

Fabre-Normand and Smith-Sedra have found circuits that operate as translinear current conveyors which have a wide frequency range and can be integrated easily.[11] The relaxation oscillator described in this section is based on the Fabre-Normand Current Conveyor, since it is not that dependent on device-parameter changes due to symmetry of the circuit. The Fabre-Normand Current Conveyor belongs to the class of second-generation current

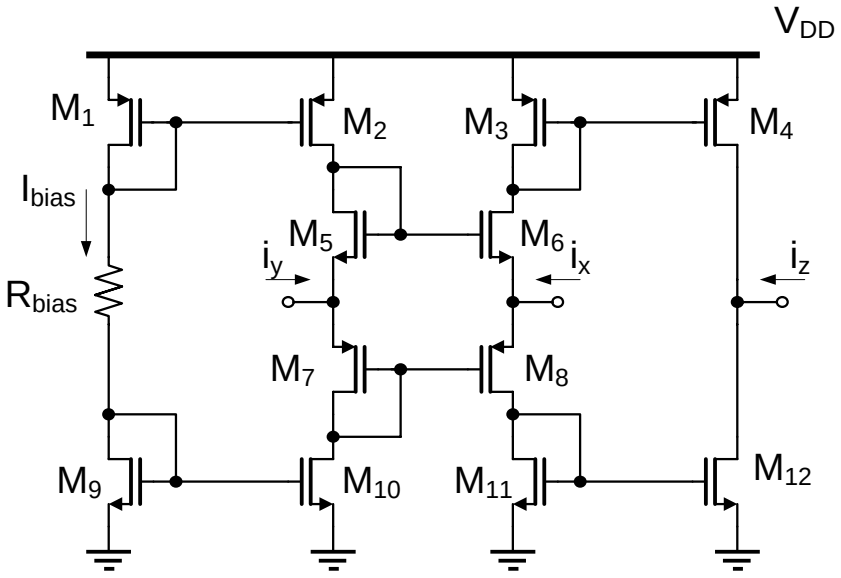

Figure 14: Schematic of the translinear current conveyor [11]

conveyors (CCII) defined by the following set of equations [11]:

$$\text{Condition I } v_{\mathrm{x}} = v_{\mathrm{y}} \tag{6}$$

$$\text{Condition II } i_{\mathrm{y}} = 0 \tag{7}$$

$$\text{Condition III } i_{\mathrm{z}} = \pm i_{\mathrm{x}} \tag{8}$$

The sign of current i_{x} is determined by either the positive or negative type of the CCII. In our case we describe the negative current conveyor. The CCII described in [11] consists of two voltage mirrors M5, M6 and M7, M8 and four current mirrors M1-M4 and M9-M12 depicted in Fig. 14.

If transistors M5-M6 and M7-M8 have matched characteristics and infinite output resistance and M2, M10 have equal currents, then transistors M5, M6 and M7,M8 have equal gate-source voltages.

$$\begin{aligned} i_{\mathrm{D5}} &= i_{\mathrm{D7}} = I_{\mathrm{bias}} \\ v_{\mathrm{GS5}} &= v_{\mathrm{GS6}}. \end{aligned}$$

This means that $i_{\mathrm{y}} = 0$ and Condition II is fulfilled. Since voltage mirrors M5 to M8 form a translinear cell containing a closed loop [11]

$$v_{\mathrm{GS5}} - v_{\mathrm{GS6}} - v_{\mathrm{GS8}} + v_{\mathrm{GS7}} = 0$$

we can apply the translinear principle to the voltage mirrors because M5 to M8 are in the subthreshold region and obtain [11]

$$i_{\mathrm{D5}} \cdot i_{\mathrm{D7}} = i_{\mathrm{D6}} \cdot i_{\mathrm{D8}}.$$

If we combine the above principles, the following equations for currents and voltages of M6 and M8 are obtained [11]

$$I_{\mathrm{bias}}^2 = i_{\mathrm{D6}} \cdot i_{\mathrm{D8}} \tag{9}$$

$$v_{\mathrm{GS6}} = v_{\mathrm{GS8}} \tag{10}$$

when current i_{x} is zero then the drain currents i_{D6}, i_{D8} are equal to the current I_{bias}. That means that all gate-source voltages in the translinear loop are equal. Thus, v_{x} and v_y are equal $v_{\mathrm{x}} = v_{\mathrm{y}}$ and Condition I is fulfilled. In the small-signal behavior if $i_{\mathrm{x}} \neq 0$ then [11]

$$i_{\mathrm{D6}} + i_{\mathrm{x}} = i_{\mathrm{D8}}. \tag{11}$$

Thus it follows, from 9 and 11 if $i_{\mathrm{x}} \ll I_{\mathrm{bias}}$, that [11]

$$\begin{aligned} i_{\mathrm{D6}} &\approx I_{\mathrm{bias}} - \frac{1}{2} \cdot i_{\mathrm{x}} \\ i_{\mathrm{D8}} &\approx I_{\mathrm{bias}} + \frac{1}{2} \cdot i_{\mathrm{x}}. \end{aligned}$$

Because $i_z = i_x$, Condition III is also fulfilled. Thus this circuit is a current conveyor of the second type. The current conveyor finds wide application

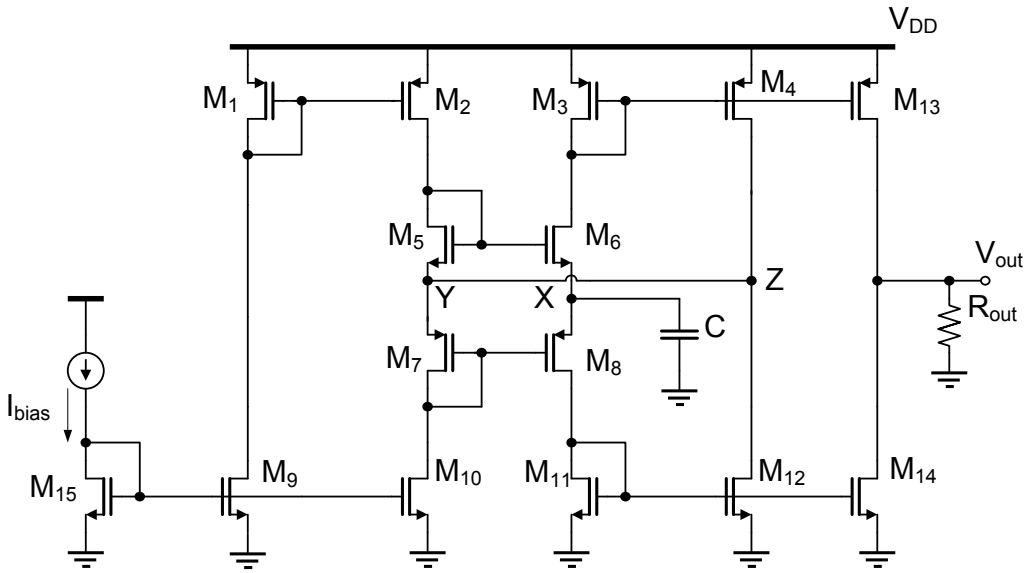

Figure 15: C/g_m- Oscillator based on the Fabre-Normand Current Conveyor [11]

especially to perform the function of a negative impedance converter (NIC), which is useful for the active part of a relaxation oscillator.

They also consume less power than a conventional operational amplifier due to their inherent capability of working in current mode not in voltage mode. [11]

3.3.2 C/g_{m}- Oscillator

The C/g_{m}- Oscillator based on the Fabre-Normand current conveyor is seen in Fig. 15. The timing is adjusted through the capacitor C and the transconductance g_{m} of the transistors. The output of the oscillator is formed by M_{13}, M_{14} and R_{out}. This part of the circuit can be replicated to obtain several outputs of the system, isolated from each other.

The static behavior can be seen in Fig. 16. The part where the negative resistor works is clearly seen and can be adjusted by M2 to M9 in Fig. 14. As seen in Fig. 17 the resistor R is obsolete since a circuit working with currents in the nano-Ampere range has resistors in the MΩ-range.

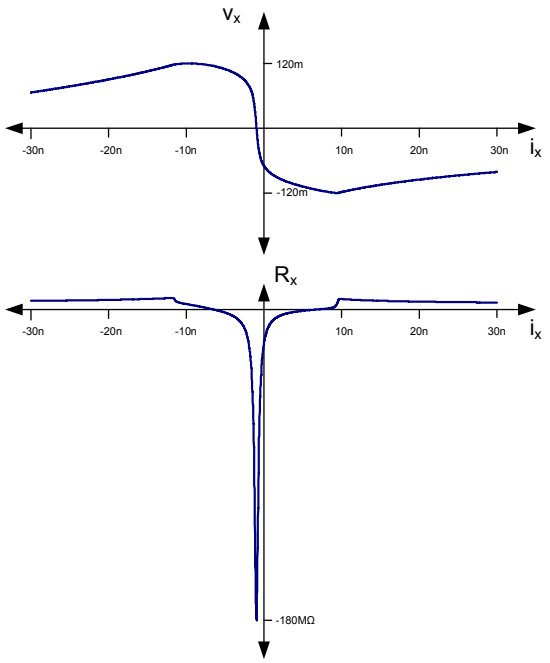

Figure 16: Static behaviour of the Negative impedance converter (NIC) with current conveyors

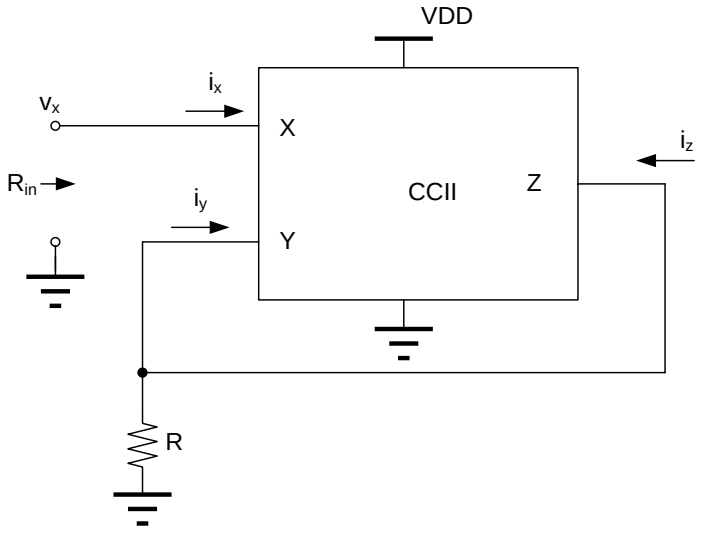

Figure 17: Negative impedance converter based on current conveyor [11]

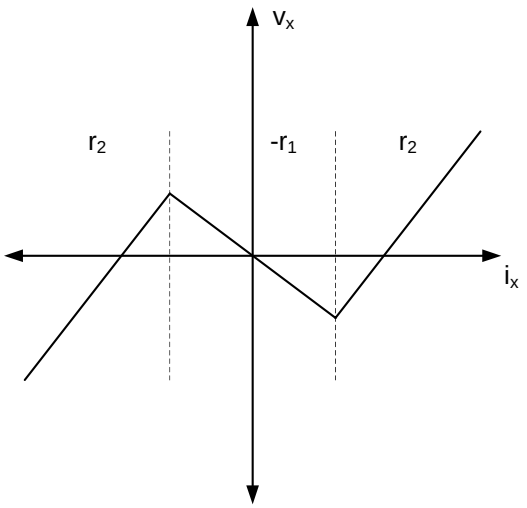

Figure 18: $v_x - i_x$ response [11]

3.3.3 An Attempt to Understand the Oscillator's Behavior

In the operating point the small signal analysis indicates a negative resistance as depicted in Fig. 18. The capacitor interacts with the circuit which has a sawtooth characteristic. The circuit, in Fig. 15 is used to obtain the discussed $v_\mathrm{x} - i_\mathrm{x}$ graph seen in Fig. 18. While the negative resistance is shown to be $-r_0/4$, the positive is about $1/g_\mathrm{m}$. Hence it is not a real RC-Oscillator but more an C/g_m-Oscillator as the title of the section indicates. The oscillation is explained next:

The capacitor in Fig. 15 is charged and X ramps up. Therefore M6 cuts off and M3 mirrors a smaller current to M4. Since current mirror M11-M12 is still working, points Z and hence Y ramp down. Since M2 and M10 work as current sources M5 and M7 are shifted due to Y. Since the gate of M5 ramps down M6 is cut off even faster. At this point the capacitor is charged to its highest point and Z is low. Now C is immediately discharged by M11. Then M3 is conducting and C ramps down even more till M8 cuts off and the current through M11 sinks hence also the current through M12 and Z rises. The rise of Z causes M8 to cut off earlier, since the gate of M8 follows Z. When M8 is cut off the current through M3 is delivered to the capacitor and hence X ramps up again.

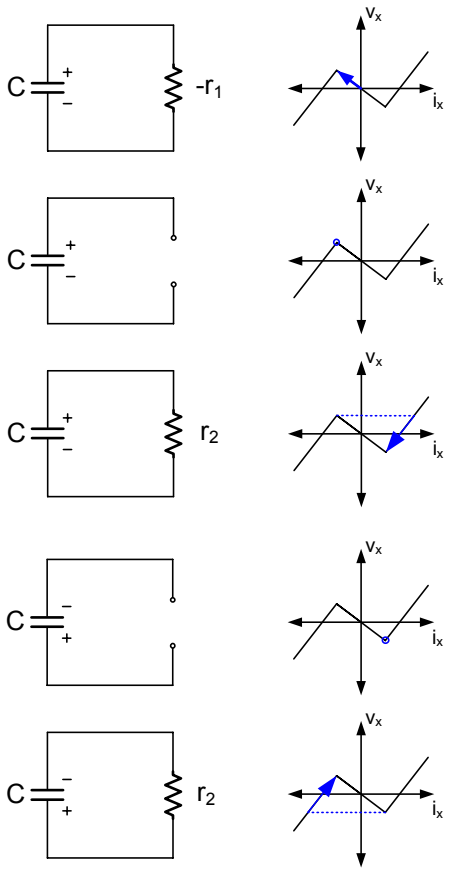

Figure 19: Graphical explanation of the operation mode

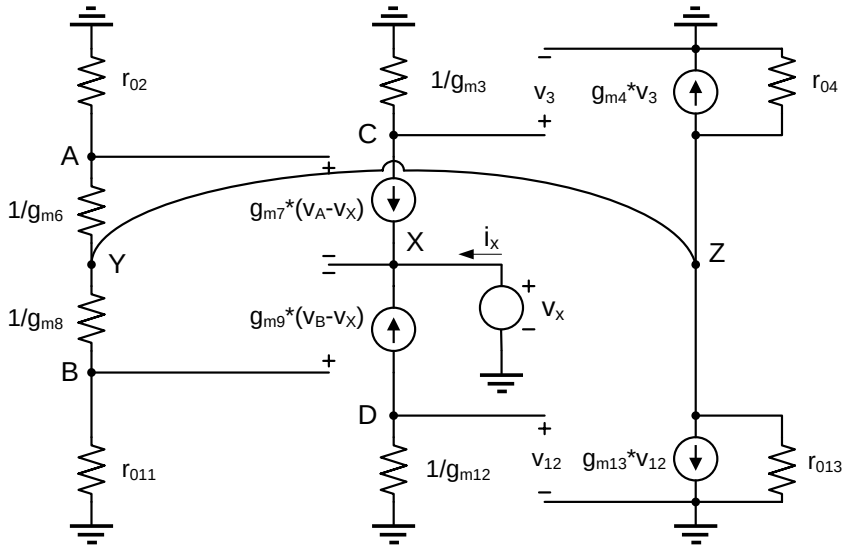

Figure 20: Small signal equivalent of the current conveyor

The crucial point is that Z switches abruptly from low to high and therefore determines the actual thresholds of the circuit. In other words when I_{M4} becomes equal to I_{M12} then Z switches and this changes the charging direction of the capacitor.

Another way to describe the behavior of the oscillator is shown in Fig. 19. In the first graph the capacitor C is charged by a negative resistor $-r_1$ up to the threshold of the Current Conveyor. At this point the capacitor is charged to its highest voltage as seen in the second graph. Next, as seen in the third graph the capacitor is discharged by r_2 until it reaches the lower threshold. As seen in the fourth graph C is charged to its lowest value. In the fifth graph the capacitor is again discharged by r_2 until it reaches its highest point. This is possible because we consider a small signal behavior in Fig. 19.

3.3.4 Small Signal Equivalent of the Fabre Normand Current Conveyor CCII

As depicted in Fig. 20 we use the small signal equivalent to show how the negative resistor is built.

With some rearrangement of the small signal devices Fig. 21 is obtained.

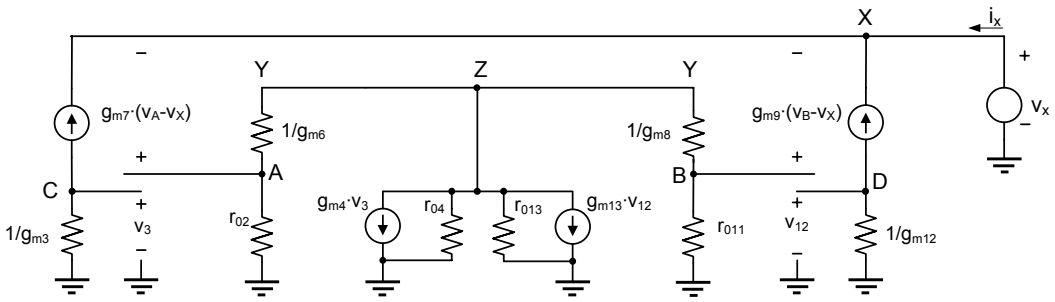

Figure 21: Rearrangement of the small signal equivalent

In the following calculation the negative resistance of the CCII is examined:

$$\begin{aligned} 0 &= g_{\mathrm{m7}} \cdot (V_{\mathrm{A}} - V_{\mathrm{X}}) + g_{\mathrm{m9}} \cdot (V_{\mathrm{B}} - V_{\mathrm{X}}) + i_{\mathrm{X}} \\ i_{\mathrm{X}} &= g_{\mathrm{m7}} \cdot (V_{\mathrm{X}} - V_{\mathrm{A}}) + g_{\mathrm{m9}} \cdot (V_{\mathrm{X}} - V_{\mathrm{B}}). \end{aligned}$$

Now the missing voltages V_{A} and V_{B} are calculated. As shown in Fig. 21 these voltages are subdivided from V_{Z}. But since $1/g_m$ is much smaller than r_0 these voltages are almost equal to V_{Z}

$$\begin{aligned} V_{\mathrm{A}} &= \frac{r_{02}}{r_{02} + 1/g_{m6}} \cdot V_{\mathrm{Z}} \\ V_{\mathrm{A}} &\approx V_{\mathrm{Z}}. \end{aligned}$$

the next step is to calculate V_{Z} to obtain V_3 in a next step. Since these two voltages are in a loop, V_{Z} has to be calculated.

$$\begin{aligned} V_{\mathrm{Z}} &= -(g_{\mathrm{m4}} \cdot V_3 + g_{\mathrm{m13}} \cdot V_{12}) \cdot (r_{04} \parallel r_{013} \parallel \approx r_{02} \parallel \approx r_{011}) \\ V_3 &= g_{\mathrm{m7}} \cdot (V_{\mathrm{X}} - V_{\mathrm{A}}) \cdot 1/g_{\mathrm{m3}} \\ V_{12} &= g_{\mathrm{m9}} \cdot (V_{\mathrm{X}} - V_{\mathrm{B}}) \cdot 1/g_{\mathrm{m12}}. \end{aligned}$$

As pointed out earlier $V_{\mathrm{A}} \approx V_{\mathrm{Z}}$

$$
\begin{aligned}
V_3 &\approx \frac{g_{m7}}{g_{\mathrm{m3}}} \cdot (V_X - V_{\mathrm{Z}}) \\
V_{12} &\approx \frac{g_{m9}}{g_{\mathrm{m12}}} \cdot (V_X - V_{\mathrm{Z}})
\end{aligned}
$$

Now V_{Z} can easily be calculated:

$$
\begin{aligned}
V_{\mathrm{Z}} &= -\left(g_{\mathrm{m4}} \cdot \frac{g_{m7}}{g_{\mathrm{m3}}} \cdot (V_X - V_{\mathrm{Z}}) + g_{\mathrm{m13}} \cdot \frac{g_{m9}}{g_{\mathrm{m12}}} \cdot (V_X - V_{\mathrm{Z}}) \right) \cdot (r_{04} \parallel r_{013} \parallel\!\approx r_{02} \parallel\!\approx r_{011}) \\
V_{\mathrm{Z}} &= -\left(g_{\mathrm{m4}} \cdot \frac{g_{m7}}{g_{\mathrm{m3}}} + g_{\mathrm{m13}} \cdot \frac{g_{m9}}{g_{\mathrm{m12}}} \right) \cdot (r_{04} \parallel r_{013} \parallel\!\approx r_{02} \parallel\!\approx r_{011}) \cdot (V_X - V_{\mathrm{Z}}). \qquad (12)
\end{aligned}
$$

Note the negative sign in Eq. 12. After some rearrangement of the variables we obtain:

$$
\begin{aligned}
V_{\mathrm{Z}} &= \frac{-\left(g_{\mathrm{m4}} \cdot \frac{g_{m7}}{g_{\mathrm{m3}}} + g_{\mathrm{m13}} \cdot \frac{g_{m9}}{g_{\mathrm{m12}}} \right) \cdot (r_{04} \parallel r_{013} \parallel\!\approx r_{02} \parallel\!\approx r_{011})}{1 - \left(g_{\mathrm{m4}} \cdot \frac{g_{m7}}{g_{\mathrm{m3}}} + g_{\mathrm{m13}} \cdot \frac{g_{m9}}{g_{\mathrm{m12}}} \right) \cdot (r_{04} \parallel r_{013} \parallel\!\approx r_{02} \parallel\!\approx r_{011})} \cdot V_X \\
i_{\mathrm{X}} &= g_{\mathrm{m7}} \cdot (V_{\mathrm{X}} - V_{\mathrm{A}}) + g_{\mathrm{m9}} \cdot (V_{\mathrm{X}} - V_{\mathrm{B}}) \qquad (13) \\
i_{\mathrm{X}} &\approx g_{\mathrm{m7}} \cdot (V_{\mathrm{X}} - V_{\mathrm{Z}}) + g_{\mathrm{m9}} \cdot (V_{\mathrm{X}} - V_{\mathrm{Z}}). \qquad (14)
\end{aligned}
$$

Now we can insert V_{Z} in Eq. 14:

$$
\begin{aligned}
i_{\mathrm{X}} &\approx g_{\mathrm{m7}} \cdot \left(V_{\mathrm{X}} - \frac{-\left(g_{\mathrm{m4}} \cdot \frac{g_{m7}}{g_{\mathrm{m3}}} + g_{\mathrm{m13}} \cdot \frac{g_{m9}}{g_{\mathrm{m12}}} \right) \cdot (r_{04} \parallel r_{013} \parallel\!\approx r_{02} \parallel\!\approx r_{011})}{1 - \left(g_{\mathrm{m4}} \cdot \frac{g_{m7}}{g_{\mathrm{m3}}} + g_{\mathrm{m13}} \cdot \frac{g_{m9}}{g_{\mathrm{m12}}} \right) \cdot (r_{04} \parallel r_{013} \parallel\!\approx r_{02} \parallel\!\approx r_{011})} \cdot V_{\mathrm{X}} \right) \\
&+ g_{\mathrm{m9}} \cdot \left(V_{\mathrm{X}} - \frac{-\left(g_{\mathrm{m4}} \cdot \frac{g_{m7}}{g_{\mathrm{m3}}} + g_{\mathrm{m13}} \cdot \frac{g_{m9}}{g_{\mathrm{m12}}} \right) \cdot (r_{04} \parallel r_{013} \parallel\!\approx r_{02} \parallel\!\approx r_{011})}{1 - \left(g_{\mathrm{m4}} \cdot \frac{g_{m7}}{g_{\mathrm{m3}}} + g_{\mathrm{m13}} \cdot \frac{g_{m9}}{g_{\mathrm{m12}}} \right) \cdot (r_{04} \parallel r_{013} \parallel\!\approx r_{02} \parallel\!\approx r_{011})} \cdot V_{\mathrm{X}} \right) \\
i_{\mathrm{X}} &\approx (g_{\mathrm{m7}} + g_{\mathrm{m9}}) \cdot \left(\frac{V_{\mathrm{X}}}{1 - \left(g_{\mathrm{m4}} \cdot \frac{g_{m7}}{g_{\mathrm{m3}}} + g_{\mathrm{m13}} \cdot \frac{g_{m9}}{g_{\mathrm{m12}}} \right) \cdot (r_{04} \parallel r_{013} \parallel\!\approx r_{02} \parallel\!\approx r_{011})} \right).
\end{aligned}
$$

If we consider all tranconductanes g_{m} almost equal and all output resistances r_0 almost equal we obtain:

$$
\begin{aligned}
i_{\mathrm{X}} &\approx 2g_{\mathrm{m}} \cdot \left(\frac{V_{\mathrm{X}}}{1 - 2g_{\mathrm{m}} \cdot \frac{r_0}{4}} \right) \\
\frac{V_{\mathrm{X}}}{i_{\mathrm{X}}} &= \frac{1 - g_{\mathrm{m}} \cdot \frac{r_0}{2}}{2g_{\mathrm{m}}}.
\end{aligned}
$$

If $g_{\mathrm{m}} \cdot r_0 \gg 1$ we can write

$$
\frac{V_{\mathrm{X}}}{i_{\mathrm{X}}} \approx - \frac{g_{\mathrm{m}} \cdot \frac{r_0}{2}}{2g_{\mathrm{m}}}
$$

and it follows:

$$
\frac{V_{\mathrm{X}}}{i_{\mathrm{X}}} \approx -\frac{r_0}{4}. \tag{15}
$$

Therefore with Eq. 15 we have provided proof that the CCII in this configuration shows a negative resistance assuming that all transistors are in saturation.

3.3.5 Determination of the Period of Oscillation

The static characteristic of the current-controlled NIC can be approximated by three linear segments of appropriate slope as shown in Fig. 22 [14]. The period of oscillation is obtained when the operating point goes once through the limit cycle. The jumps of the operating point, as seen in Fig. 22 are almost instant and they are neglected in the calculation of the oscillation. To determine the oscillation period we just take the time when the quiescent point is on the parts of the characteristic with a large positive slope (r_2).

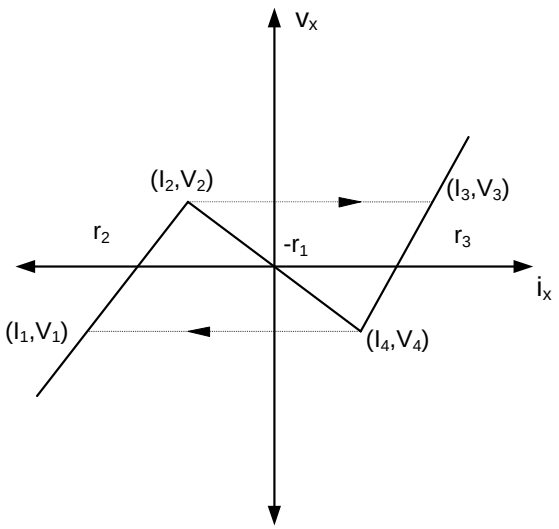

Figure 22: The current-voltage NIC characteristic, three segment approximation [14]

$$
\begin{aligned}
i_1 &= -C \cdot \frac{dv_{\mathrm{X}}}{dt} = -C\frac{d}{dt}(r_2 \cdot i_1) \\
dt &= -C \cdot r_2 \frac{di_1}{i_1} \\
\int dt &= -C \cdot r_2 \frac{di_1}{i_1} \\
\Delta t|_0^{T/2} &= -C \cdot r_2 \cdot \left[\ln\left(i_1|_{T/2}\right) - \ln\left(i_1|_0\right)\right] \\
\Delta t|_0^{T/2} &= -C \cdot r_2 \cdot \left[\ln\left(I_2\right) - \ln\left(I_1\right)\right] \\
\Delta t &= C \cdot r_2 \cdot \ln\left(\frac{I_1}{I_2}\right) \\
T &= C \cdot r_2 \cdot \ln\left(\frac{I_1}{I_2}\right) + C \cdot r_3 \cdot \ln\left(\frac{I_3}{I_4}\right). \qquad (16)
\end{aligned}
$$

Eq. 16 [14] shows that the period depends on the capacitor C and the shape of the NIC static characteristic: the slope of segments r_2 and r_3, and the location of the turning points. Thus this oscillator is not suitable for temperature cancelation technique because it is not easily foreseen how a temperature compensation would work on the frequency of oscillation.

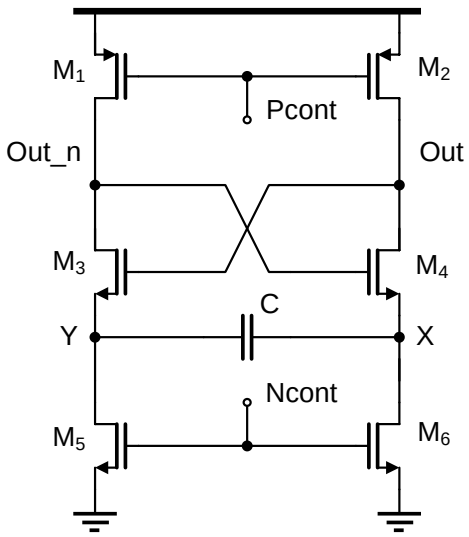

Figure 23: Schematic of the CMOS relaxation oscillator [10]

3.4 CMOS Relaxation Oscillator with Current Reuse

Source coupled multivibrators are easily implemented in CMOS-Technology and hence suitable for a wide range of applications in the field of very large scale integration. Other advantages are that they can provide high frequency output waveforms. Fig. 23 shows an implementation of the relaxation oscillator. It consists of a cross coupled pair M3, M4, current sources M5, M6 and two transistors M1, M2 working in the deep triode region.

Fig. 24 reveals the operation of this circuit. When the cross coupled pair is steered in such direction, that M4 is in deep triode and in exchange M3 is off, the capacitor C is charged by the current I. Since $R \cdot I$ is the voltage drop across M2 working in deep triode X is defined as $V_{\mathrm{DD}} - I \cdot R$ and hence Y ramps down. This means the capacitor is charged until v_{GS3} is high enough to switch on M3 and turn off M4 while forcing Y to $V_{\mathrm{DD}} - I \cdot R$ and charging the capacitor in the other direction, hence X ramps down. This all happens just with one current while the other one is wasted. The frequency is given by

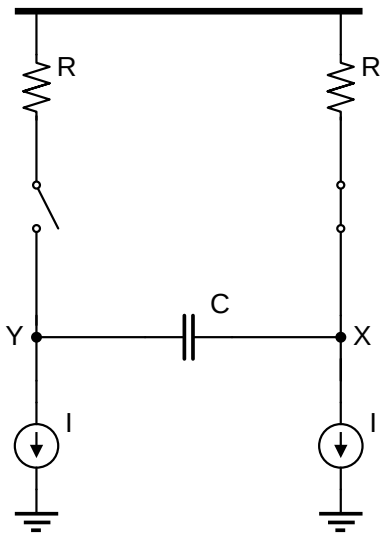

Figure 24: Illustration of the operational principle [10]

$$f \propto \frac{I}{C \cdot V_{\text{Swing}}} \propto \frac{1}{2 \cdot C \cdot R}.$$

Thus as found in [10] we can improve the power dissipation by about 50% ideally and 30% in reality by using a similar approach as explained next.

Fig. 25 shows the detailed circuit schematic of the relaxation oscillator proposed in [10]. In this case only one current source has been used. Transistors M3, M4 act as a gain stage, the cross coupling of these two transistors ensures that only one of the two is turned on. This gain stage also controls the operation of the differential pair formed by transistors M5 and M6. These two gain stages M3, M4 and M5, M6 determine the charging direction of the capacitor. As in the former circuit the transistors M1, M2 operate as approximately linear resistors and with capacitor C this R defines the operating frequency.

Assuming M3 is on and M4 is off as supposed in Fig. 25 then Out_n is $V_{\text{DD}} - 2I \cdot R$ and Out is V_{DD} where $2I$ is the value of the tail current. Since Out is higher than Out_n the differential pair M5, M6 is steered to the right and the current flows from M1 over M3 over the C and M6 to the current

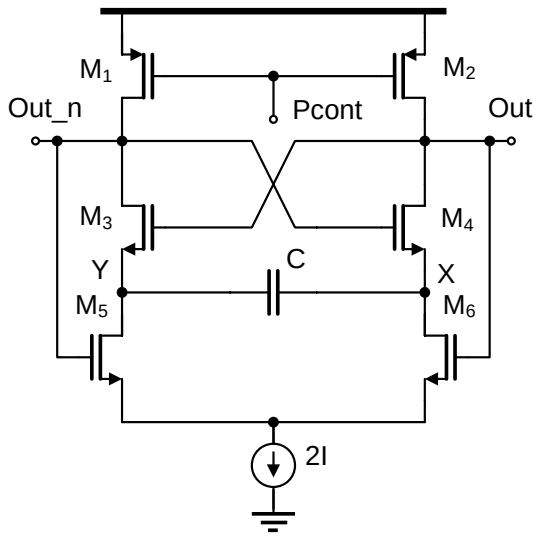

Figure 25: The CMOS relaxation oscillator realised by [10]

source as seen in Fig. 26. This causes the voltage X to ramp downwards until M4 turns on due to the down ramp of its source and hence Out falls and switches off M3. This in return changes the bias points of the capacitor. Now Out_n is V_{DD} and Out is $V_{\mathrm{DD}} - 2I \cdot R$ and hence Diff Pair M5, M6 is switched to the left and current is flowing from M2 over M4 over C and M5 to the current source $2I$. In both phases the voltage across the capacitor increases with a constant slope of $2I/C$.

$$f \propto \frac{2I}{C \cdot V_{\mathrm{Swing}}} \propto \frac{1}{R \cdot C}.$$

The oscillator in Fig. 25 has no elements to limit the voltage swing since the linear resistors are not regulated and the common mode point of Out is not regulated. Hence some kind of swing control has to be implemented. One attempt is to use the replica bias circuit which is seen in Fig. 27 and to regulate V_{min} to V_{ref} and hence with the current flowing through M8 and the voltage drop $V_{\mathrm{DS}} = V_{\mathrm{DD}} - V_{\mathrm{min}}$ over M8 we can define R_{on8}. Attention has to be paid to the ratios M1/M8 and M7/M11. These two ratios have to be made the same to guarantee that the regulation works properly because otherwise two regulations, one from M1 and M8 and the other one coming from I_7 would

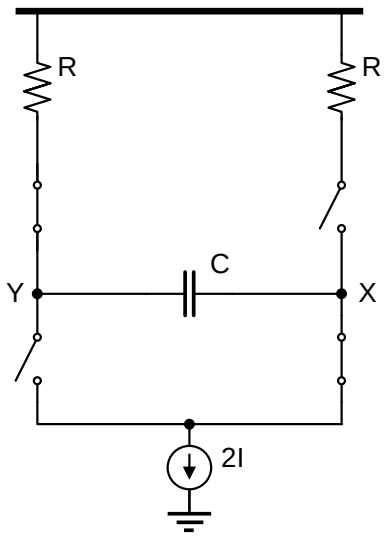

Figure 26: Illustration of the operational principle in [10]

cause a kind of chaotic response of the output voltage, thus the circuit is not operating properly. But if these obstacles are overcome the circuit oscillates properly. We also have to pay attention to the stability of the regulating operational transconductance amplifier. Since its regulated point $V_{\min}$ is very susceptible to oscillating we have to compensate this point by means of a capacitor. As simulations have pointed out the calculated temperature coefficient (TC) is approximately TC $\approx$ 800ppm/°C. A minimum TC, only dependent on a poly-R used in a bandgap circuit, can be achieved, as shown in the next Section.

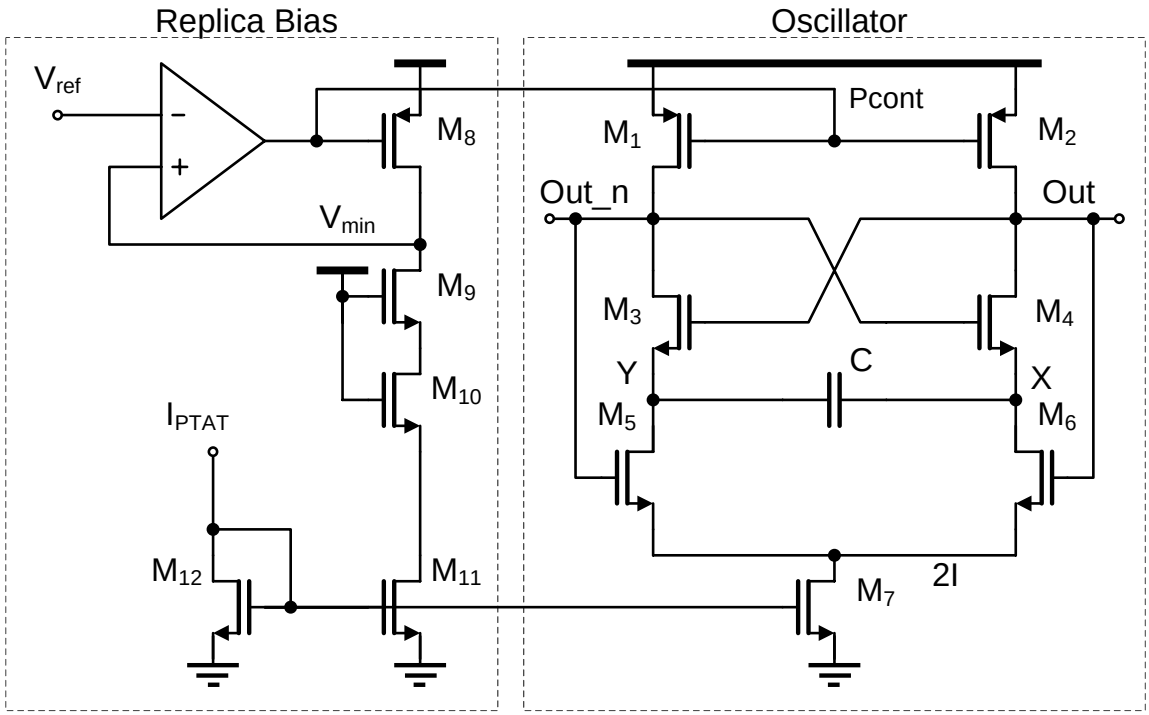

Figure 27: Design of the oscillator using replica biasing [10]

4 Actual Implementation

As shown in Fig. 2 the power state controller (PSC) is active in all *Deep Sleep Mode*s. In these modes the power consumption is in the range of μW as shown in Table 1. Thus the requirements for the real time clock (RTC) differ significantly from the requirements of the quartz oscillator which is used to clock the master state machine and for generating a precise RF carrier of the transceiver. For the described RTC low power consumption, long term stability, and temperature stability are the most important parameters, whereas phase noise and jitter are very important for the quartz oscillator. The RTC is calibrated by the quartz oscillator, frequency accuracy is passed down from the quartz oscillator to the RTC. Due to the tradeoff between power consumption and time resolution in the power management unit (PMU), described in Section 2.1, the best oscillation frequency has been found to be 100 kHz. This low frequency allows for low power consumption but its time resolution is high enough to define precise wake-up cycles.

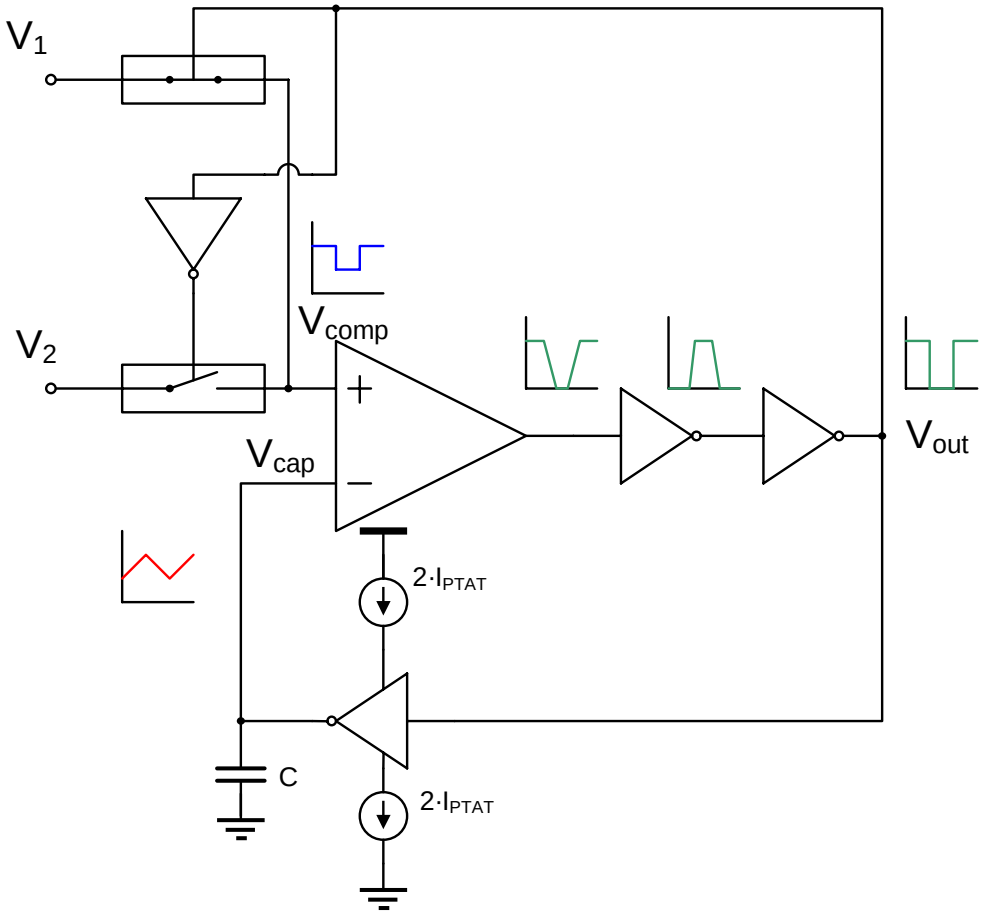

Figure 28: Oscillator Design [5]

To guarantee precise wake-up taking process variation and mismatch into account, a mechanism for calibrating the RTC has been implemented [5].

4.1 Oscillator Topology

The oscillator is based on the relaxation principle. A comparator compares the voltage across a capacitor C to two defined threshold voltages V_1 and V_2, respectively. Depending on the state of the oscillator, the higher or the lower threshold is chosen and the capacitor is charged or discharged accordingly. The topology of the oscillator is depicted in Fig. 28. The capacitor is charged by a current starved inverter with a proportional-to-absolute-temperature (PTAT) current coming from a bandgap cell. The voltage across the capacitor

is compared to the voltage on the positive input of the comparator. The latter one can be switched either to V_1 or V_2, respectively. Section 4.3 presents how these voltages can be generated. The period of the pure (ideal) oscillator T_P can be obtained by equating:

$$2I_\mathrm{PTAT} \cdot \Delta t \;=\; C \cdot \Delta V$$

where the factor 2 arises because the current generated in the bandgap is doubled for the oscillator, $\Delta t = T_\mathrm{P}\,/2$, and $\Delta V = V_1 - V_2$.

$$T_\mathrm{P} \;=\; \frac{C \cdot \Delta V}{I_\mathrm{PTAT}}. \tag{17}$$

4.2 Comparator

The comparator topology, shown in Fig. 29, has been selected because it shows a good tradeoff between power consumption and delay time (T_D). The implementation consists of a two stage operational tranconductance amplifier (OTA) followed by three inverters. The OTA needs no compensation (e.g. Miller compensation) since stability is not a severe issue in comparators if we also take capacitive feedback loops into account which occure in the layout. A proper delay time is obtained if the capacitance at the gate of M5 is minimized and the current through M6 and M7 is maximized. The major constraint therefore is the power consumption of the comparator. The three CMOS inverters are implemented in order to increase the slew rate of the comparator. To allow for minimum delay time the inverters should increase in size by a factor of approximately three. In this work the power consumption has to be considered and a tradeoff between power consumption and delay time has to be made. In this case a reasonable delay time is achieved by cascading three inverters. To account for the power consumption all three inverters have the same size, but at the expense of delay time.

In the conceptual graph of the period, shown in Fig. 30, the period is clearly visible. It consists of the period of an ideal oscillator (T_P) received

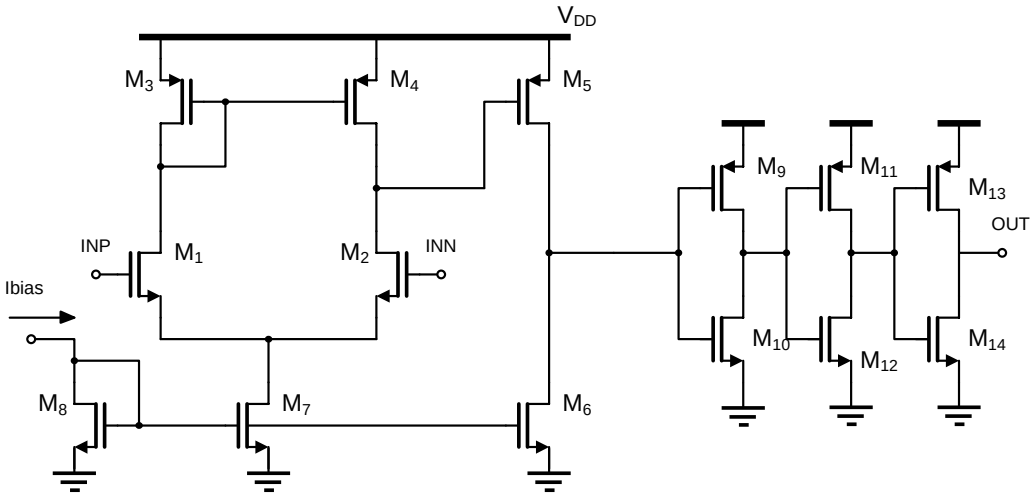

Figure 29: The proposed comparator [5]

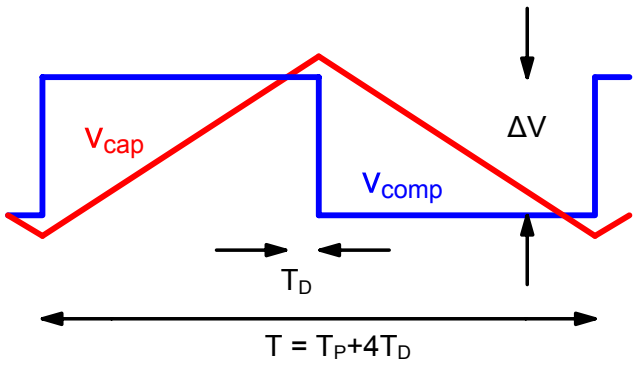

Figure 30: Period of the oscillator including the delay time of the comparator [5]

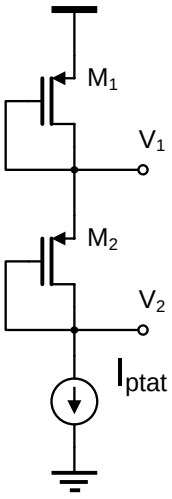

Figure 31: Threshold voltage generation with stacked diodes [5]

from Eq. 17 and the delay time (T_{D}) caused by the comparator. Since T_{D} is not well defined it is advisable that the delay time of the comparator is small compared to T_{P} . Therefore the ratio T_{P} /T_{D} has been chosen to be approximately 100.

$$T = \frac{C \cdot \Delta V}{I_{\mathrm{PTAT}}} + 4 \cdot T_{\mathrm{D}}. \tag{18}$$

4.3 Threshold Voltage Generation

This section presents six different approaches how the threshold voltages V_1 and V_2 can be generated. A major constraint is that the difference between V_1 and V_2 has to be PTAT. Thus the solutions are selected by these constraints.

4.3.1 Two Stacked Diodes

The first approach is stacking two diodes supplied by a current source as depicted in Fig. 31. The current source accounts for the supply independence of the two diodes. Since ΔV is equal to one V_{GS} the current required for charging the capacitor would be too high for the application. Another disadvantage is that its ΔV is not PTAT and therefore cannot cancel the

PTAT current.

4.3.2 Cascoded Transistors

An enhancement to the solution shown in Fig. 31 is the use of stacked diodes in a cascode configuration as shown in Fig. 32. The basic idea is to bias transistors M1 and M2 at different gate-source voltages V_{GS} . This approach uses the fact that two different transistors biased by the same current and using different aspect ratios produce a voltage difference. It has to be ensured that transistor M2 stays in the saturation region. Unfortunately this condition cannot be established easily. If a huge aspect ratio is used between the W/L of M1 and M2 this can be guaranteed. But this would increase the ΔV which is not desired. The following derivations are made in weak inversion since the transistors in this work are supplied with currents in the nano-Ampere range.

$$
\begin{aligned}
I_{\mathrm{D1}} &= I_{\mathrm{S}} \cdot k \cdot (W/L)_1 \cdot e^{V_{\mathrm{GS1}}/(n \cdot \phi_{\mathrm{t}})} \\
I_{D2} &= I_{\mathrm{S}} \cdot (W/L)_2 \cdot e^{V_{\mathrm{GS2}}/(n \cdot \phi_{\mathrm{t}})} \\
I_{D1} &= I_{D2} \\
k \cdot e^{V_{\mathrm{GS1}}/(n \cdot \phi_{\mathrm{t}})} &= e^{V_{\mathrm{GS2}}/(n \cdot \phi_{\mathrm{t}})} \\
k &= \frac{e^{V_{\mathrm{GS2}}/(n \cdot \phi_{\mathrm{t}})}}{e^{V_{\mathrm{GS1}}/(n \cdot \phi_{\mathrm{t}})}} \\
k &= e^{(V_{\mathrm{GS2}} - V_{\mathrm{GS1}})/(n \cdot \phi_{\mathrm{t}})} \\
\Delta V &= V_{\mathrm{GS2}} - V_{\mathrm{GS1}} \\
\Delta V &= \phi_{\mathrm{t}} \cdot n \cdot \ln(k).
\end{aligned}
$$

If both transistors were in saturation and matched we would get a voltage difference which is not dependent on current neither on process parameters. But since transistor M2 is constantly on the edge to the triode region the ΔV is dependent on current and temperature rather then just temperature and an aspect ratio. Simulation pointed out a 7mV change in the ΔV while the temperature is changed from -40°C to 125°C. This means that ΔV is not

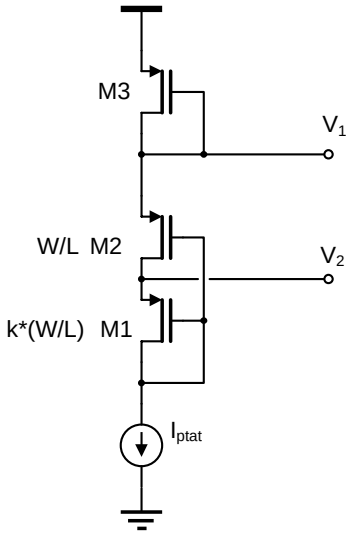

Figure 32: Threshold voltage realization using stacked transistors in diode configuration [5]

PTAT but between independent of temperature and PTAT. This is due to the fact that transistor M2 is not on the edge of triode but is slightly in the triode region which is not desired. Due to this fact we have to insert a poly resistor and we obtain a bias-dependent voltage drop.

4.3.3 Cascoded Transistors with Resistor

Another enhancement to the topology described in Section 4.3.2 is simply inserting a resistor. This means that the PTAT voltage is split into two different parts. One part generated by M1 and M2, while the other one is produced by $R_{\mathrm{Poly}} \cdot I_{\mathrm{PTAT}}$. The advantage is that the resistor must not be dimensioned ample and hence area can be saved. But since this topology has the same disadvantages as explained in the former Section we still search for a better approach. The equation which describes the behavior of Fig. 33 is shown in Eq. 19.

$$\Delta V \quad = \quad \phi_{\,\mathrm{t}} \cdot \ln(k) + R_{\mathrm{Poly}} \cdot I_{\mathrm{PTAT}}. \tag{19}$$

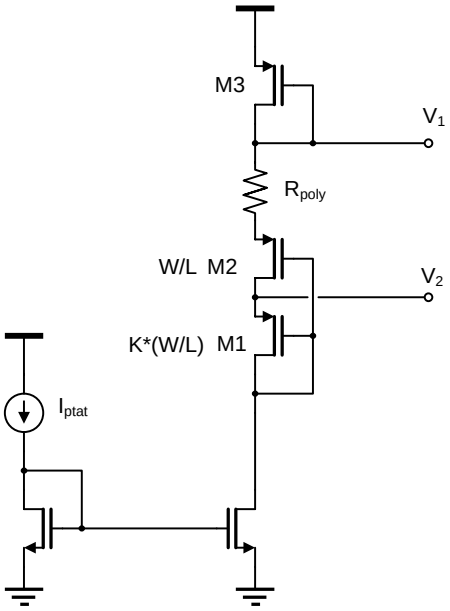

Figure 33: Threshold voltage realization with added Poly resistor

As Eq. 19 reveals the steepness of the PTAT voltage can be adjusted. This means a possiblity exists to cancel out the temperature dependency of the oscillation frequency. Unfortunately in practica this will not work due to fact that the temperature response of a poly resistor does not match the temperature response of a cascoded transistor pair.

4.3.4 Unbalanced Differential-Pair

If we could use the same method as in Section 4.3.2, going one V_{GS} down and going up another one, but not forcing one transistor in the triode region we could also compensate the threshold voltages and get a ΔV which is not dependent on process parameters. This can be established using a differential pair and slightly unbalancing it as depicted in Fig. 35. If transistors M2 and M3 are biased in weak inversion we get similar formulas to those derived in Section 4.3.2, but with the advantage that all transistors are in saturation. The following derivations show two calculations, one made in strong inversion and the second one in weak inversion.

If both transistors are in strong inversion and in saturation then $V_{gs1} =$

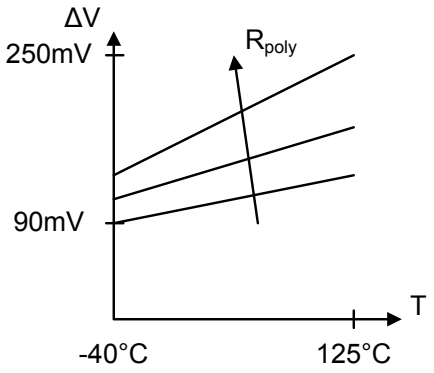

Figure 34: ΔV Change over Temperatur with varying R_{poly}

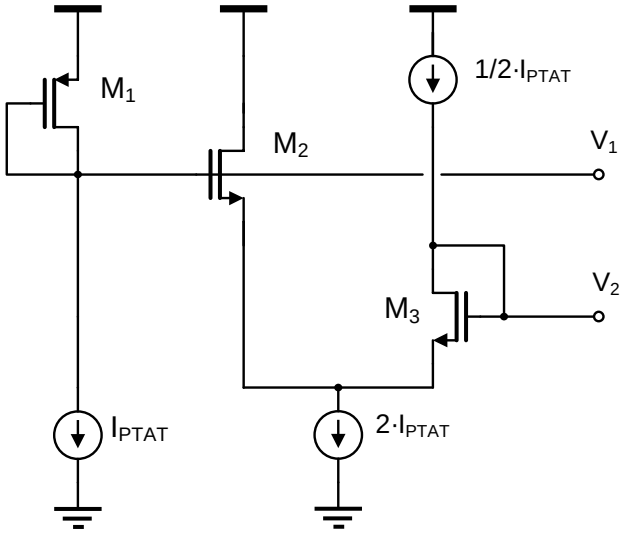

Figure 35: Threshold voltage generation with an unbalanced Differential Pair [5]

$V_{th1} + \sqrt{\frac{2 \cdot I_{D1}}{K' \cdot (W/L)_1}}$

$$\Delta V = V_{th1} + \sqrt{\frac{2 \cdot I_{D1}}{K' \cdot (W/L)_1}} - V_{th2} - \sqrt{\frac{2 \cdot I_{D2}}{K' \cdot (W/L)_2}}.$$

And since $V_{th1,2}$ is assumed to be equal we can write:

$$\Delta V = \sqrt{\frac{2 \cdot I_{D1}}{K' \cdot (W/L)_1}} - \sqrt{\frac{2 \cdot I_{D2}}{K' \cdot (W/L)_2}} \tag{20}$$

This means we have 2 parameters to adjust the level-shift. The current and the aspect ratios of the 2 transistors [7]. The second approach shows a similar result but the only process parameter in Eq. 21 is the factor n which comes from the capacitive voltage divider explained in Section 2.3. This means that it is less susceptible to process parameter changes than Eq. 20.

$$\begin{aligned}
I_{\mathrm{D1}} &= I_{\mathrm{S}} \cdot (W/L)_1 \cdot e^{(V_{\mathrm{GS1}})/(n \cdot \phi_t)} \\
I_{\mathrm{D2}} &= I_{\mathrm{S}} \cdot (W/L)_2 \cdot e^{(V_{\mathrm{GS2}})/(n \cdot \phi_t)} \\
V_{\mathrm{GS1}} &= \phi_t \cdot n \cdot \ln(\frac{I_{\mathrm{D1}}}{I_{\mathrm{S}} \cdot (W/L)_1}) \\
V_{\mathrm{GS2}} &= \phi_t \cdot n \cdot \ln(\frac{I_{\mathrm{D2}}}{I_{\mathrm{S}} \cdot (W/L)_2}) \\
\Delta V &= \phi_t \cdot n \cdot \ln(\frac{I_{\mathrm{D1}}}{I_{\mathrm{S}} \cdot (W/L)_1}) - \phi_t \cdot n \cdot \ln(\frac{I_{\mathrm{D2}}}{I_{\mathrm{S}} \cdot (W/L)_2}) \\
\Delta V &= \phi_{\mathrm{t}} \cdot n \cdot \ln(\frac{I_{\mathrm{D1}} \cdot (W/L)_2}{I_{\mathrm{D2}} \cdot (W/L)_1}).
\end{aligned} \tag{21}$$

In our case $I_{D1} = 15nA$, $I_{D2} = 5nA$, $(W/L)_1 = 0.1$,$(W/L)_2 = 1$ and if we assume $\phi_{\mathrm{t}} = 26mV$ and $n = 1.2$ than we get a $\Delta V = 106.1mV$, compared to a value of $105.2mV$ in the simulation.

4.3.5 Bandgap-Reference

Since the oscillation frequency is dependent on a simple RC-product as will be shown in Section 4.3.9, it has a temperature-coefficient (TC). Namely, that

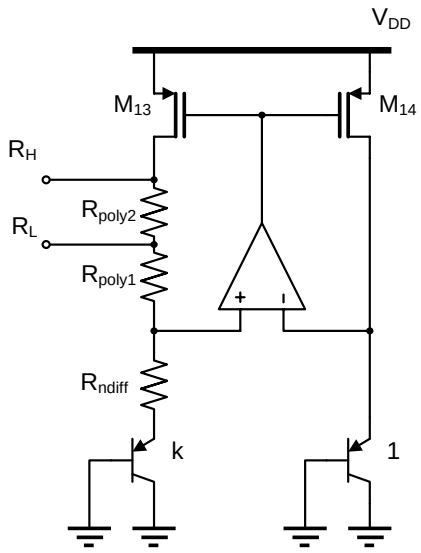

Figure 36: Bandgap-Reference Circuit [12]

of the R_{Poly2} resistance and that of the capacitor C. To cancel out the TC we have to calculate the exact PTAT current which we get from the bandgap-circuit first. As depicted in Fig. 36 we obtain a rather simple PTAT-Current by biasing two PNP-transistors with different areas. This kind of bandgap circuit has also been used in this work.

In Fig. 37 the V_{BE}-biasing of an NPN and PNP transistor is shown. In principle both approaches are the same. But in the CMOS process used in this work, only a parasitic PNP transistor is available. The urge to use par-

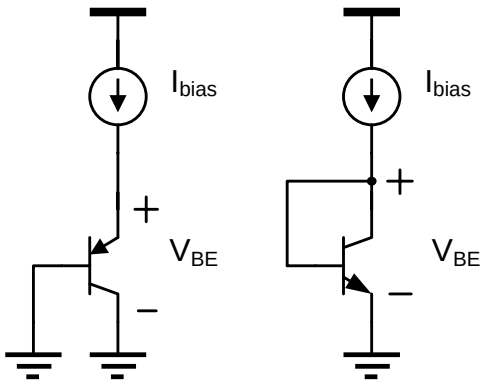

Figure 37: V_{BE}-biasing npn and pnp transistor [12]

asitic PNP transistor rather than MOS transistors biased in weak inversion is shown next. One essential difference between a bipolar transistor and a MOS transistor in weak inversion is, that the bipolar does not have a factor n in the formula given below

$$\begin{aligned} \text{Bipolar} \quad I_{\mathrm{C}} &= I_{\mathrm{S\_Bip}} \cdot A \cdot e^{\frac{V_{\mathrm{BE}}}{\phi_{\mathrm{t}}}} \\ \text{MOS} \quad I_{\mathrm{D}} &= I_{\mathrm{S\_MOS}} \cdot \frac{W}{L} \cdot e^{\frac{V_{\mathrm{GS}}}{n \cdot \phi_{\mathrm{t}}}}. \end{aligned}$$

This is why CMOS-Processes will still use hidden bipolar transistors in bandgap- circuits. As seen in Fig. 36

$$V_{\mathrm{BE2}} + I_{\mathrm{PTAT}} \cdot R_{\mathrm{Poly1}} = V_{\mathrm{BE1}} \tag{22}$$

$$V_{\mathrm{BE}} = \phi_{\mathrm{t}} \cdot \ln(\frac{I_{\mathrm{C}}}{A_{\mathrm{E}} \cdot I_{\mathrm{S}}}). \tag{23}$$

from Eq. 22 follows:

$$\begin{aligned} I_{\mathrm{PTAT}} &= \frac{V_{\mathrm{BE1}} - V_{\mathrm{BE2}}}{R_{\mathrm{Poly1}}} \\ I_{\mathrm{PTAT}} &= \frac{\phi_{\mathrm{t}} \cdot \left[\ln(\frac{I_{\mathrm{C1}}}{A_1 \cdot I_{\mathrm{S}}}) - \ln(\frac{I_{\mathrm{C2}}}{k \cdot A_1 \cdot I_{\mathrm{S}}})\right]}{R_{\mathrm{Poly1}}} \end{aligned} \tag{24}$$

and if $A_2 = k \cdot A_1$ and $I_{\mathrm{C1}} = I_{\mathrm{C2}}$ then we can reduce Eq. 24 to:

$$I_{\mathrm{PTAT}} = \frac{\phi_{\mathrm{t}} \cdot \ln(k)}{R_{\mathrm{Poly1}}}.$$

The voltage drop across R_{Poly2} seen in Fig. 36 is:

$$\begin{aligned} \Delta V_{\mathrm{R}} &= I_{\mathrm{PTAT}} \cdot R_{\mathrm{Poly2}} \\ \Delta V_{\mathrm{R}} &= \phi_{\mathrm{t}} \cdot \ln(k) \cdot \frac{R_{\mathrm{Poly2}}}{R_{\mathrm{Poly1}}}. \end{aligned} \tag{25}$$

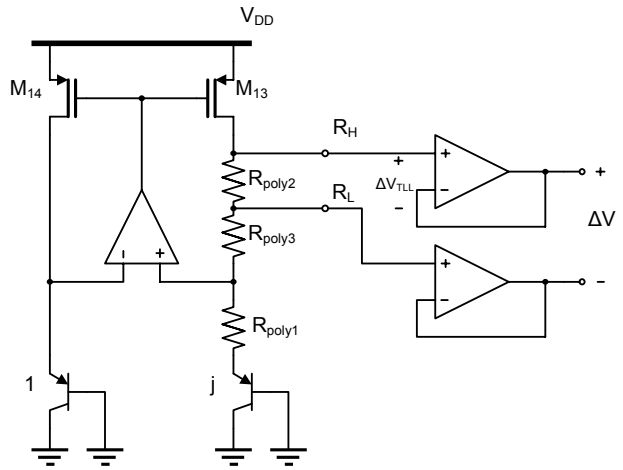

Figure 38: Bandgap with buffered thresholds

4.3.6 Bandgap with Buffers

As shown in Fig. 38 the voltage drop across R_{Poly1} is not the only voltage drop which can be used as thresholds. Instead we can use an OTA with a specified ΔV_{TLL}. TLL stands for translinear loop. This means the OTA is used as a follower. But to obtain advantage of the TLL it is unbalanced as explained next:

To obtain a certain ΔV_{TLL} a look has to be taken into the design of the OTA. Basically it is a simple CMOS OTA with two diodes as source degeneration as depicted in Fig. 39.

Since this circuit forms also a translinear loop

$$\begin{aligned}
\Delta V_{\mathrm{TLL}} &= V_{\mathrm{P}} - V_{\mathrm{N}} \\
\Delta V_{\mathrm{TLL}} &= V_{\mathrm{GS1}} + V_{\mathrm{GS3}} - V_{\mathrm{GS4}} - V_{\mathrm{GS2}} \\
\Delta V_{\mathrm{TLL}} &= \phi_{\mathrm{t}} \cdot n \cdot \ln(\frac{I_1}{S_1 \cdot I_{\mathrm{S}}}) + \phi_{\mathrm{t}} \cdot n \cdot \ln(\frac{I_1}{S_3 \cdot I_{\mathrm{S}}}) - \\
&= \phi_{\mathrm{t}} \cdot n \cdot \ln(\frac{I_2}{S_4 \cdot I_{\mathrm{S}}}) - \phi_{\mathrm{t}} \cdot n \cdot \ln(\frac{I_2}{S_2 \cdot I_{\mathrm{S}}})
\end{aligned}$$

where $S_{\mathrm{x}} = (\frac{W}{L})_{\mathrm{x}}$

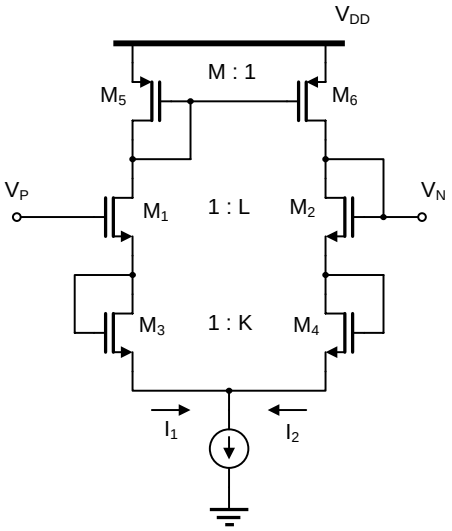

Figure 39: OTA with enhanced ΔV generation

$$\Delta V_{\mathrm{TLL}} = \phi_{\mathrm{t}} \cdot n \cdot \ln(\frac{I_1 \cdot S_2}{S_1 \cdot I_2}) + \phi_{\mathrm{t}} \cdot n \cdot \ln(\frac{I_1 \cdot S_4}{S_3 \cdot I_2})$$

where $S_2 = L \cdot S_1$ and $S_4 = K \cdot S_3$ and $I_1 = M \cdot I_2$

$$\begin{aligned}
\Delta V_{\mathrm{TLL}} &= \phi_{\mathrm{t}} \cdot n \cdot \ln(\frac{I_1 \cdot S_2}{S_1 \cdot I_2} \cdot \frac{I_1 \cdot S_4}{S_3 \cdot I_2}) \\
\Delta V_{\mathrm{TLL}} &= \phi_{\mathrm{t}} \cdot n \cdot \ln(\frac{M \cdot I_2 \cdot L \cdot S_1}{S_1 \cdot I_2} \cdot \frac{M \cdot I_2 \cdot K \cdot S_3}{S_3 \cdot I_2}) \\
\Delta V_{\mathrm{TLL}} &= \phi_{\mathrm{t}} \cdot n \cdot \ln(M^2 \cdot L \cdot K).
\end{aligned}$$

This has the advantage to get higher factors in the logarithm as been explained. To put it in other words we enhance the term $\phi_T \cdot n$ by a logarithmic factor which depends on the ratios of the opposed transistors.

4.3.7 Temperature Compensation with the Translinear Loop (TTL)

Without the ΔV_{TLL} we obtain a frequency which depends only on an RC-Product as explained in Section 4.3.9. Because of ΔV_{TLL} we get a dependency

on two added RC-Products as explained next:

$$\begin{aligned} C \cdot \Delta \mathrm{V} &= 2 \cdot I_{\mathrm{PTAT}} \cdot \Delta t \\ T_{\mathrm{P}} &= 2 \cdot \Delta \mathrm{t} \\ T_{\mathrm{P}} &= \frac{C \cdot \Delta V}{I_{\mathrm{PTAT}}}. \end{aligned} \tag{26}$$

The factor two under the fraction bar arises from the fact that we use twice I_{PTAT} to charge the capacitor.

$$\begin{aligned} \Delta V &= \Delta V_{\mathrm{R}} - \Delta V_{\mathrm{TLL}} \\ \Delta V &= \phi_{\mathrm{t}} \cdot \ln(k) \cdot \frac{R_{\mathrm{Poly2}}}{R_{\mathrm{Poly1}}} - \phi_{\mathrm{t}} \cdot n \cdot \ln(M^2 \cdot L \cdot K) \end{aligned}$$

if $\Delta V_{\mathrm{TLL}} = 0$ then it follows from Eq. 26

$$\begin{aligned} T_{\mathrm{P}} &= \frac{C \cdot \phi_{\mathrm{t}} \cdot \ln(k) \cdot \frac{R_{\mathrm{Poly2}}}{R_{\mathrm{Poly1}}}}{\frac{\phi_{\mathrm{t}} \cdot \ln(k)}{R_{\mathrm{Poly1}}}} \\ T_{\mathrm{P}} &= R_{\mathrm{Poly2}} \cdot C. \end{aligned}$$

Since the capacitance has a small temperature coefficient, only the TC of the R_{Poly2} has to be considered. This TC lies in the range between -100 to 300 ppm/K. If $\Delta V_{TLL} \neq 0$ we obtain a period which depends on two added RC products.

$$\begin{aligned} T_{\mathrm{P}} &= 2 \cdot \frac{C \cdot \Delta V}{2 \cdot I_{\mathrm{PTAT}}} \\ T_{\mathrm{P}} &= \frac{C \cdot [\phi_{\mathrm{t}} \cdot \ln(k) \cdot \frac{R_{\mathrm{Poly2}}}{R_{\mathrm{Poly1}}} - \phi_{\mathrm{t}} \cdot n \cdot \ln(M^2 \cdot L \cdot K)]}{\frac{\phi_{\mathrm{t}} \cdot \ln(k)}{R_{\mathrm{Poly1}}}} \\ T_{\mathrm{P}} &= C \cdot R_{\mathrm{Poly2}} - C \cdot R_{\mathrm{Poly1}} \cdot n \cdot \frac{\ln(M^2 \cdot L \cdot K)}{\ln(k)}. \end{aligned}$$

If we want a period which is temperature independent we have to make the derivation with respect to temperature equal to zero $\frac{d(T_\mathrm{P})}{d(Temp)} = 0$

$$T_\mathrm{P} = C \cdot [R_\mathrm{Poly2}(1 + TC_2 \cdot \Delta T)] - C \cdot [R_\mathrm{Poly1}(1 + TC_1 \cdot \Delta T)] \cdot n \cdot \frac{\ln(M^2 \cdot L \cdot K)}{\ln(k)}$$

where ΔT is the temperature difference between the actual temperature and 27°C, $\Delta T = T - 27°\mathrm{C}$

$$\begin{aligned} \frac{d(T_\mathrm{P})}{d(Temp)} &= C \cdot [R_\mathrm{Poly2} \cdot TC_2 - R_\mathrm{Poly1} \cdot TC_1 \cdot n \cdot \frac{\ln(M^2 \cdot L \cdot K)}{\ln(k)}] \\ 0 &= R_\mathrm{Poly2} \cdot TC_2 - R_\mathrm{Poly1} \cdot TC_1 \cdot n \cdot \frac{\ln(M^2 \cdot L \cdot K)}{\ln(k)} \\ M^2 \cdot L \cdot K &= e^{\frac{R_\mathrm{Poly2} \cdot TC_2}{R_\mathrm{Poly1} \cdot TC_1 \cdot n} \cdot \ln(k)}. \end{aligned}$$

If we can find a resistor R_Poly1 which has a much higher TC than the resistor R_Poly2 we are able to cancel the temperature coefficients and get a frequency which is temperature independent. A huge disadvantage for our purpose is that we have to use two poly resistors to get a Bandgap voltage which is fairly temperature and process independent. Due to matching issues we cannot use two different types of resistors e.g. a poly resistor and a diffusion resistor.

4.3.8 Bipolar Transistors Biased by PTAT Current

To get a precise PTAT voltage two bipolar transistors can be biased with a PTAT current generated in a bandgap cell. This approach, as shown in Fig. 40, has the advantage that the PTAT voltage is more precise than in the last approaches due to the fact that there is not a factor 1/n in the exponential curve of a bipolar transistor. Therefore a voltage as described in Eq. 27 is obtained. Note the difference between Eq. 21 and Eq. 27.

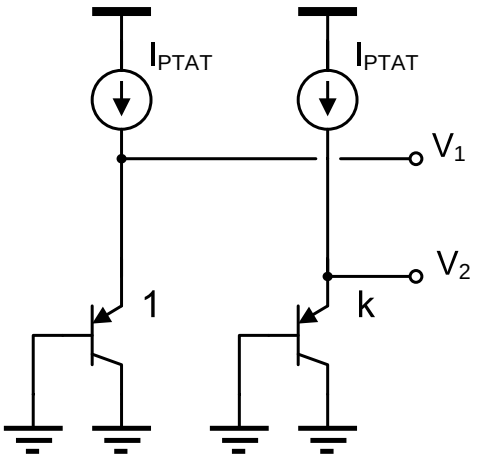

Figure 40: ΔV generation with two pnp bipolar transistors

$$\Delta V = \phi_t \cdot \ln(\mathrm{k}) \tag{27}$$

4.3.9 Bandgap with Multiple Output Voltages

The last presented method for generating the threshold voltages, which is also the one that has been selected for the oscillator, is described in this Section. Since low power consumption is a main focus, the bias currents have to be in the nano-Ampere range, and the resistors in the bandgap-reference, as shown in Fig. 41, are in the range of several MΩ and therefore consume a lot of area on the chip. In order to allow for good matching the resistors are split into a ladder of unity resistors. To avoid the need for an additional resistor to generate ΔV, the threshold voltages V_1 and V_2 are directly tapped from the bandgap resistor. In order to calibrate the oscillator, R_{Poly2} in Eq. 30 is varied by taking V_2 from different taps of this resistor ladder as shown in Fig. 41.

The voltages at R_{H} and R_{L} are buffered so as not to influence the bandgap circuit, for example charge injection from the oscillator to the bandgap causes the latter one to fail. As shown in Eq. 29 the ΔV can be used as a PTAT voltage for the oscillator circuit depicted in Fig. 28,

$$
\begin{aligned}
I_{\mathrm{PTAT}} &= \frac{V_{\mathrm{BE1}} - V_{\mathrm{BE2}}}{R_{\mathrm{Poly1}}} \\
I_{\mathrm{PTAT}} &= \frac{\phi_{\mathrm{t}} \cdot \left[\ln(\frac{I_{\mathrm{C1}}}{A_1 \cdot I_{\mathrm{S}}}) - \ln(\frac{I_{\mathrm{C2}}}{k \cdot A_1 \cdot I_{\mathrm{S}}})\right]}{R_{\mathrm{Poly1}}} \\
I_{\mathrm{PTAT}} &= \frac{\phi_{\mathrm{t}} \cdot \ln(k)}{R_{\mathrm{Poly1}}}. \qquad (28)
\end{aligned}
$$

The voltage drop across R_{Poly2} seen in Fig. 36 is:

$$
\begin{aligned}
\Delta V_{\mathrm{R}} &= I_{\mathrm{PTAT}} \cdot R_{\mathrm{Poly2}} \\
\Delta V_{\mathrm{R}} &= \phi_{\mathrm{t}} \cdot \ln(k) \cdot \frac{R_{\mathrm{Poly2}}}{R_{\mathrm{Poly1}}}. \qquad (29)
\end{aligned}
$$

If Eq. 28 and 29 are applied in Eq. 17 a period is obtained which is only dependent on R and C. Therefore the minimum obtainable temperature coefficient (TC) can be approximated by the addition of the TC of R_{Poly2} and C, as shown in Eq. 31.

$$
\begin{aligned}
T_{\mathrm{P}} &= \frac{C \cdot \phi_{\mathrm{t}} \cdot \ln(k) \cdot \frac{R_{\mathrm{Poly2}}}{R_{\mathrm{Poly1}}}}{\frac{\phi_{\mathrm{t}} \cdot ln(k)}{R_{\mathrm{Poly1}}}} \\
T_{\mathrm{P}} &= R_{\mathrm{Poly2}} \cdot C \qquad (30) \\
T_{\mathrm{P}} &= R(1 + \alpha \cdot Temp) \cdot C(1 + \beta \cdot Temp) \\
T_{\mathrm{P}} &= R \cdot C \left[1 + (\alpha + \beta) \cdot Temp + \alpha \cdot \beta \cdot Temp^2\right] \qquad (31) \\
f_{\mathrm{P}} &= \frac{1}{R_{\mathrm{Poly2}} \cdot C}.
\end{aligned}
$$

Eq 32 and 33 are obtained if the comparator delay is included in the calculations for the period. The delay is responsible for an additional TC of the oscillation frequency. This is not desired but can hardly be avoided.

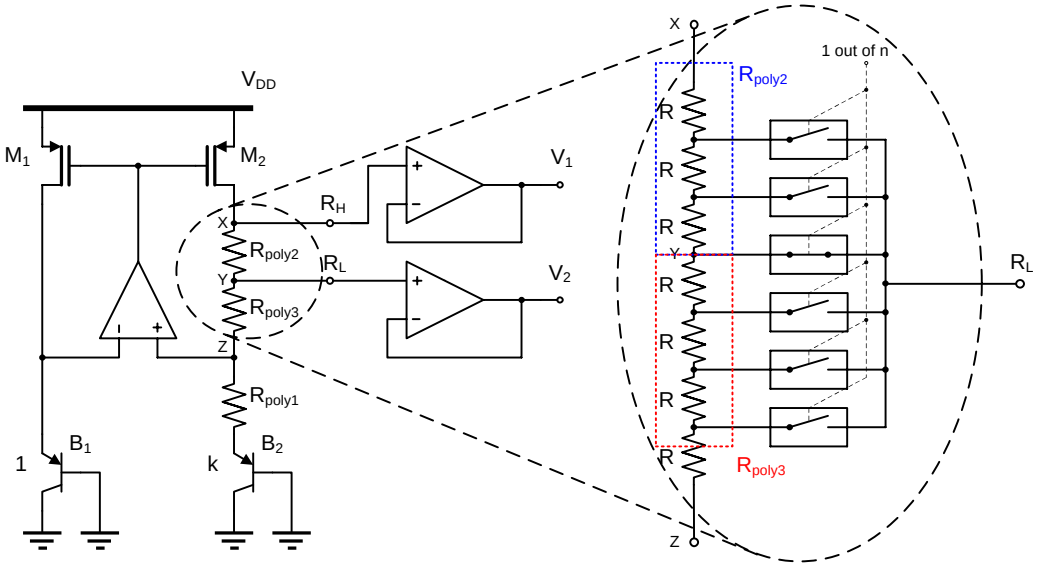

Figure 41: Resistor ladder to generate a variable V_{PTAT} for the oscillator [5]

$$T = R_{\mathrm{Poly2}} \cdot C + 4 \cdot T_{\mathrm{D}} \tag{32}$$

$$f = \frac{1}{R_{\mathrm{Poly2}} \cdot C + 4 \cdot T_{\mathrm{D}}}. \tag{33}$$

4.3.10 Tuning

In the design of a discretely controllable oscillator, tuning is an important issue. The oscillation frequency in a discrete tuning environment can be set by using a digital word and hence only a certain number of frequencies can be generated. There are two possibilities to tune the frequency of an oscillator. The most obvious is to vary the capacitance, the second approach which has been supported in this work is to vary the resistor in Eq. 30.

Capacitor Array To tune or control the frequency of Eq. 30 the capacitor can be varied. As seen in Fig. 42, this can be established by adding binary weighted capacitors to a given main cap. To switch the binary weighted capacitors transmission gates have been used. The transmission gates are bi-

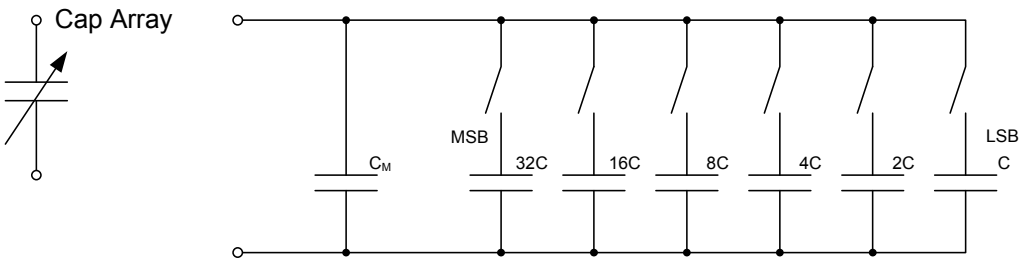

Figure 42: Capacitor Array

nary weighted too. This accounts for the parasitic capacitor introduced from the transmission gate and therefore a better linearity is obtained. In this attempt metall-insulator-metall (MIM) capacitors are chosen. This choice was made because MIM-capacitors have good linearity, a small parasitic capacitor and most important show the best matching behavior of the available capacitors.

The LSB is calculated to be 10 fF. This value has been chosen because a frequency resolution of <2kHz/LSB is desired. This is in fact a very small value. Therefore also a problem can occur in the layout since the parasitic capacitor of the connection line is not included and can cause frequency jumps which lead to a non-monotonic behavior of the frequency tuning of the oscillator. A $\sigma_{10\mathrm{fF}} = 0.1\,\%$ has been calculated using Eq. 34, and the values $A_{\Delta\mathrm{C/C}} = 0.5\,\%\mu m$ and C=10 fF have been chosen to obtain a W = L = 5 μm.

$$\sigma_{\Delta C/C} = \frac{A_{\Delta C/C}}{\sqrt{W \cdot L}}. \tag{34}$$

The diagram in Fig. 43 shows the area of the capacitance versus its matching. It means the larger the area the better is the mismatch of two adjacent capacitors. With this in mind the current to be used can be calculated with $I \cdot \Delta t = C \cdot \Delta V$

$$I \cdot \frac{T}{2} = C \cdot \Delta V$$

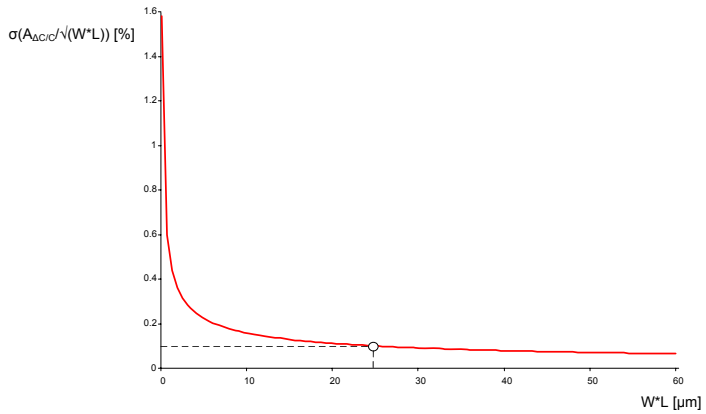

Figure 43: Diagramm Mismatch versus Area

$$\frac{I}{2 \cdot f} = C \cdot \Delta V.$$

Since the range which can be spanned with the cap-array is 640 fF, we can use ΔC to get the current which flows in the capacitor.

$$\begin{aligned} \Delta C &= \frac{I}{2 \cdot \Delta V} \cdot \left(\frac{1}{f_{min}} - \frac{1}{f_{max}}\right) \\ I &= \Delta C \cdot 2 \cdot \Delta V \cdot \frac{f_{min}(f_{min} + \Delta f)}{\Delta f}. \end{aligned} \tag{35}$$

Eq. 35 shows how to reduce the current flowing in the oscillator. As shown in Section 4.3 reducing ΔV decreases the current needed to charge the capacitor.

Resistor Tuning Resistor tuning is the preferred method to tune the oscillator. The resistor in Eq. 30 is varied in order to change the frequency. An inherently monotonic tuning behavior is obtained by using tapped voltages from a resistor as shown in Fig. 41. To activate the correct switch in the zoomed section in Fig. 41, a decoder has been designed. This decoder selects one of 64 switches according to the corresponding 6-bit code word, as shown

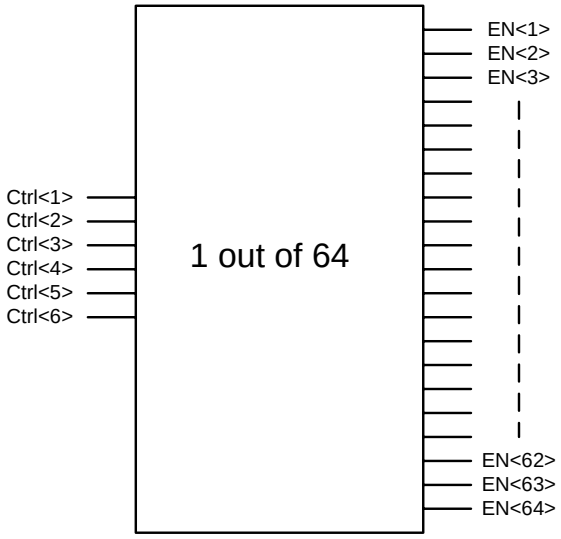

Figure 44: Decoder to select one out of 64 switches [5]

in Fig. 44. Therefore an inherently monotonic tuning curve is obtained. The resolution of 6 bits has been chosen to obtain a step size of $<2\,\mathrm{kHz/LSB}$. The conceptual design of the one hot decoder is shown in Fig. 45. It consists of AND-gates which steer the output high if the right code word is put at its input. The supply voltage allows just for an AND-gate with four inputs, hence two AND-gates one with three and one with four inputs have been cascaded to get an AND-gate with six inputs [5].

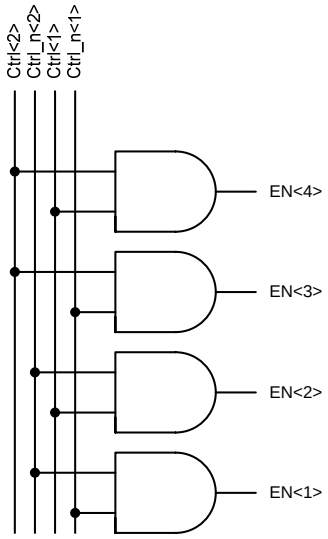

Figure 45: Conceptual Design of the decoder [5]

5 Simulation Results

For the oscillator, described before, various simulations have been carried out. The results are presented in this chapter. The simulations include tuning curves, transient curves, Monte Carlo simulations and extracted simulations.

To investigate the behavior of the oscillators with respect to variations in temperature and process parameters, simulations were made that the oscillator frequency can be adjusted in order to guarantee a frequency of 100 kHz. Five different parameter sets were used: fast, fastslow (nmos = fast and pmos = slow), nominal, slowfast (nmos = slow and pmos = fast) and slow, and the temperature may vary from -40°C to 125°C.

In Fig. 46 we see three important curves to understand the oscillator and its real behavior. The V_{cap} is simply compared to V_{comp} and when exceeding the latter one the switches in Fig. 28 toggle, hence V_1 is changed to V_2. The main current flows when the inverters are switching. Since it is not desired that the oscillator consumes much current it is helpful to use several equal inverters in a chain to obtain a high slew rate but reducing the power dissipation. If we were going for minimum delay-time of the inverters we would have to increase the size of the following inverters by about a factor

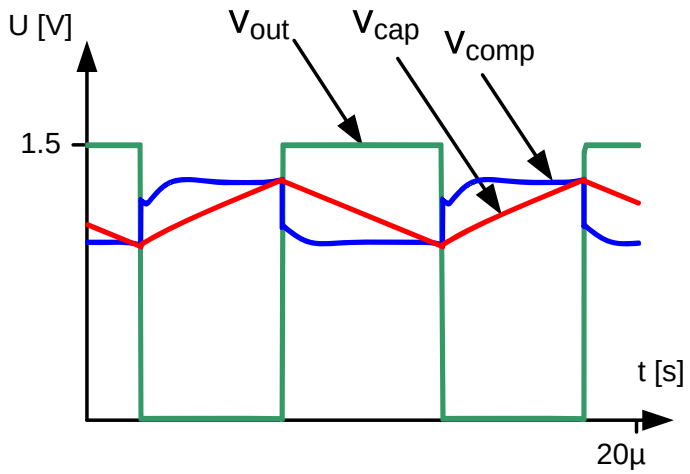

Figure 46: The three most important signals in the oscillator

of three (theoretically its e but the maximum is very flat). In Fig. 48 we see the frequency tuning and the discrete frequency steps of the tuning. The corner simulations reveal interesting properties of the circuit. The circuit is tuned with a digital word from 13 to 52. Fig. 49 and 50 show the frequency tuning at -40°C and 125°C, respectively. With this data in mind we can calibrate the oscillation frequency to 100 kHz at 27°C and sweep through the temperature range as shown in Fig. 51. This is also made for -40°C and 125°C, as shown in Fig. 52 and 53. Now we easily obtain the maximum derivation of the frequency. It is about 10kHz at a calibrated temperature of -40°C. The comparator delay is shown in Fig. 54. The Monte Carlo analysis is shown in Fig. 55. It shows a σ of the frequency of about 10 kHz. The supply dependency is shown in Fig. 56. It shows a dependency of about 15 %/V. But since the oscillator is supplied by a regulator this supply dependency is of secondary concern. The measured and simulated tuning curve is shown in Fig. 57. It is in good agreement with the simulation. The measured frequency drift is shown in Fig. 58. It is 2.3 % over a temperature range of 165°C, i.e. from -40°C to 125°C.

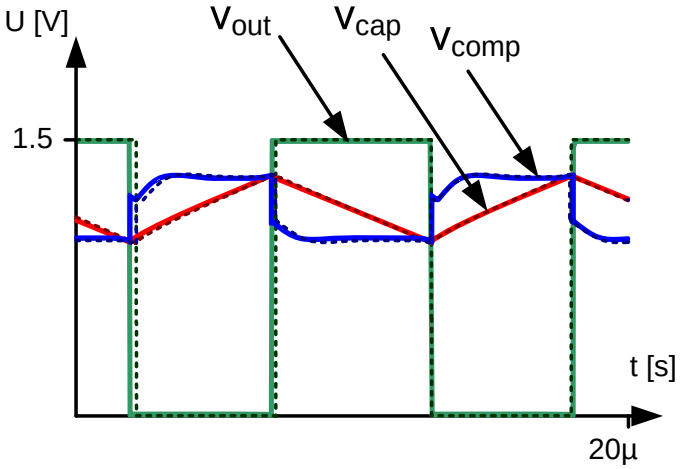

Figure 47: Original circuit (continues line) versus backannotated circuit (dashed line)

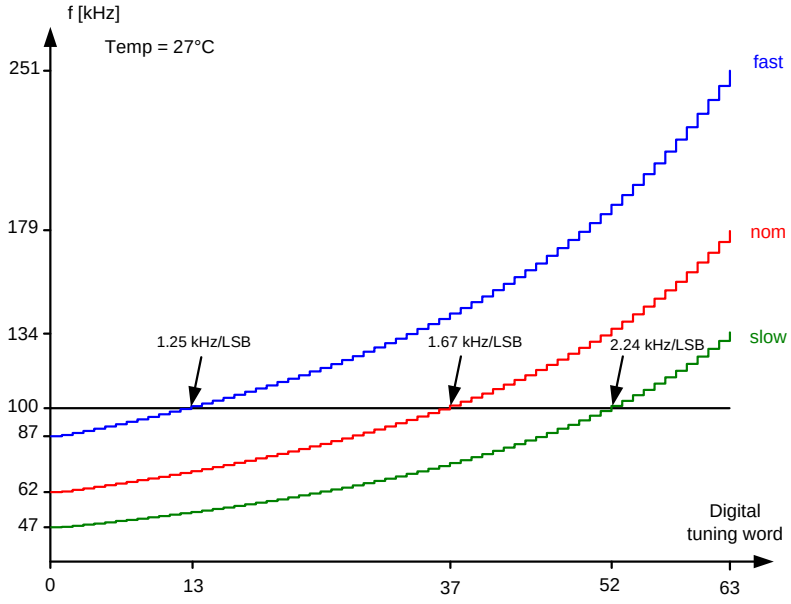

Figure 48: Frequency tuning in the presence of process variations at 27°C

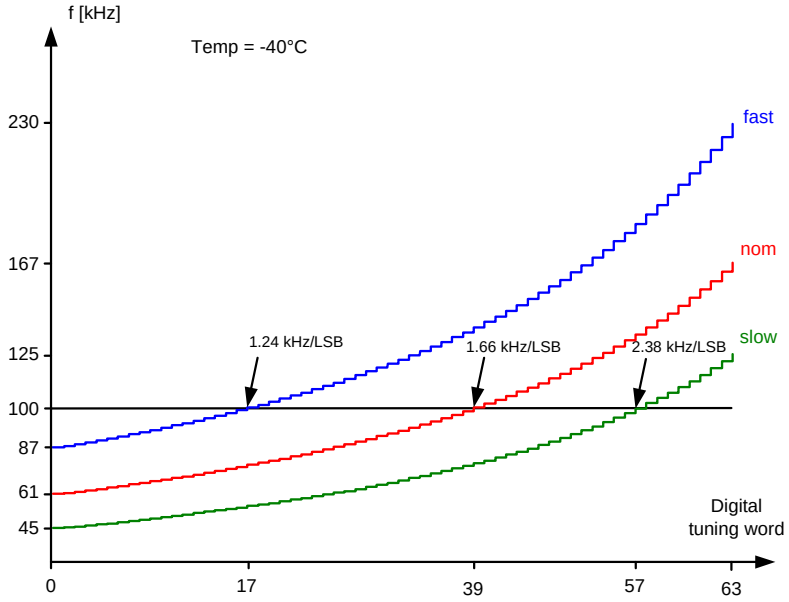

Figure 49: Frequency tuning in the presence of process variations at -40°C

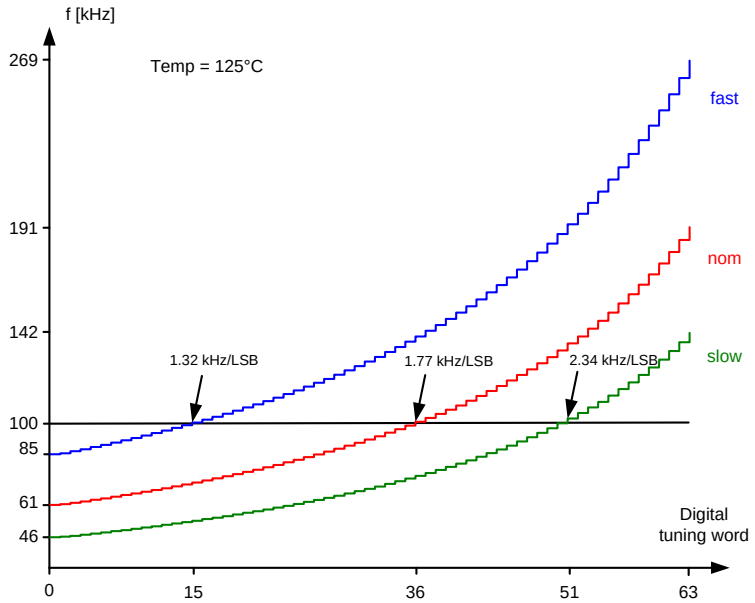

Figure 50: Frequency tuning in the presence of process variations at 125°C

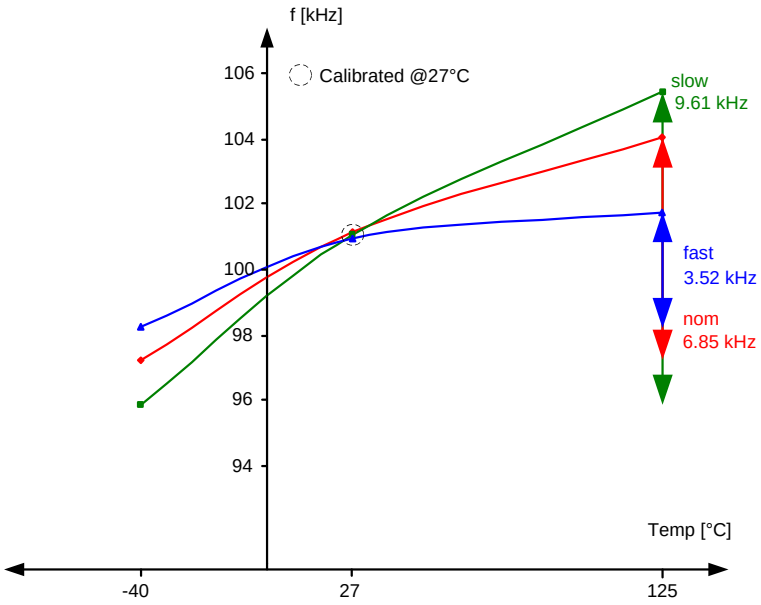

Figure 51: Frequency variation over temperature when calibrated to 27°C

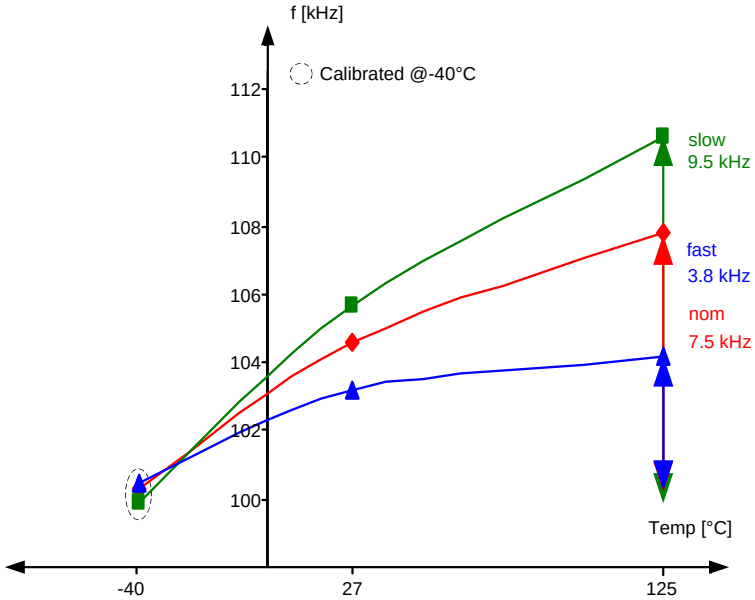

Figure 52: Frequency variation over temperature when calibrated to -40°C

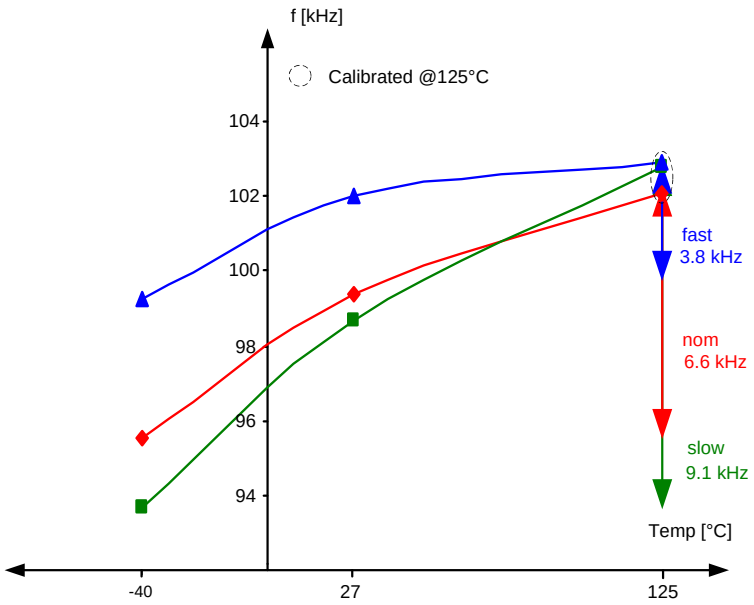

Figure 53: Frequency variation over temperature when calibrated to 125°C

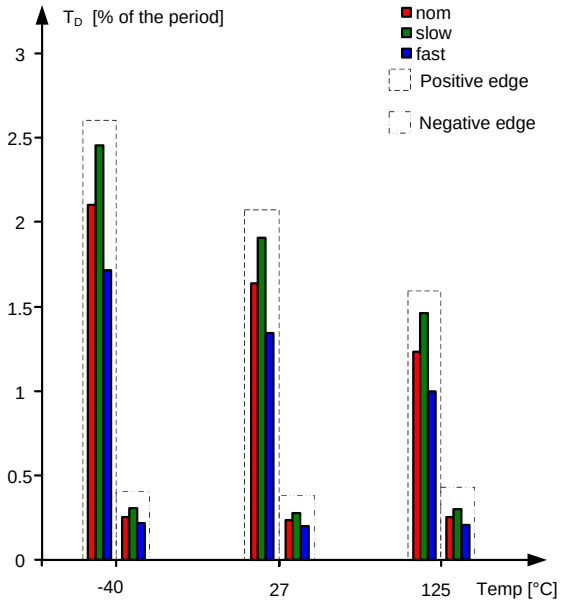

Figure 54: Comparator delay (T_D) in the presence of process variations from -40°C to 125°C

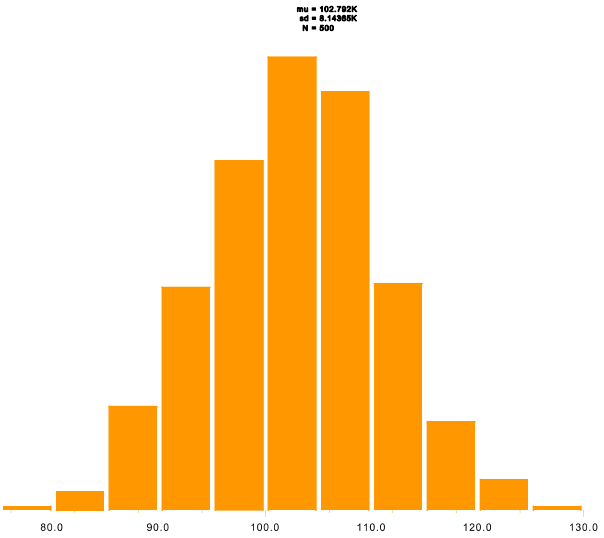

Figure 55: The monte carlo analysis of the oscillator's frequency

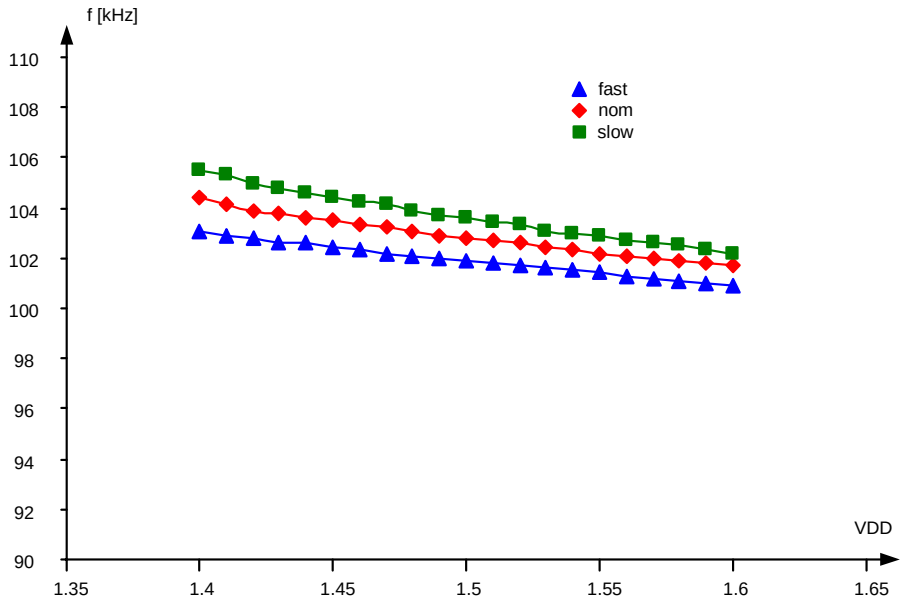

Figure 56: Frequency of oscillation in dependency of the Supply Voltage

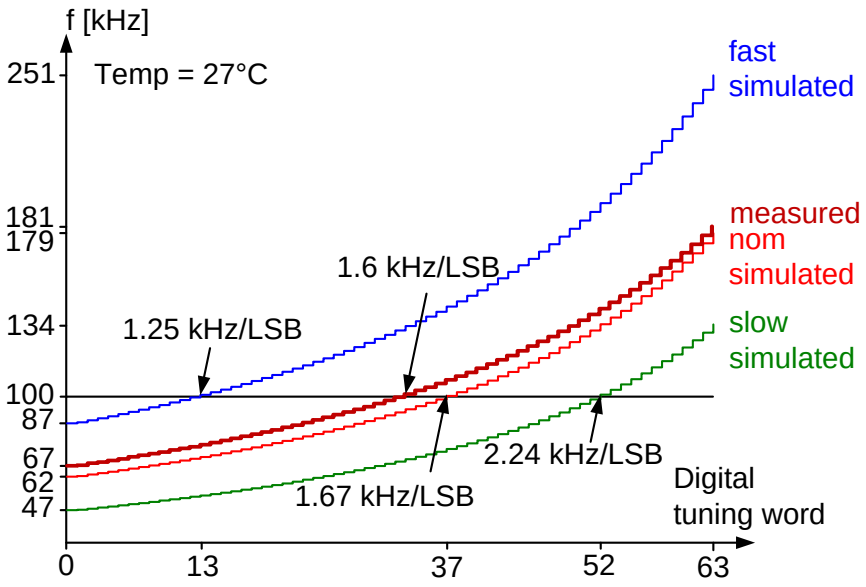

Figure 57: Frequency tuning, measured and simulated

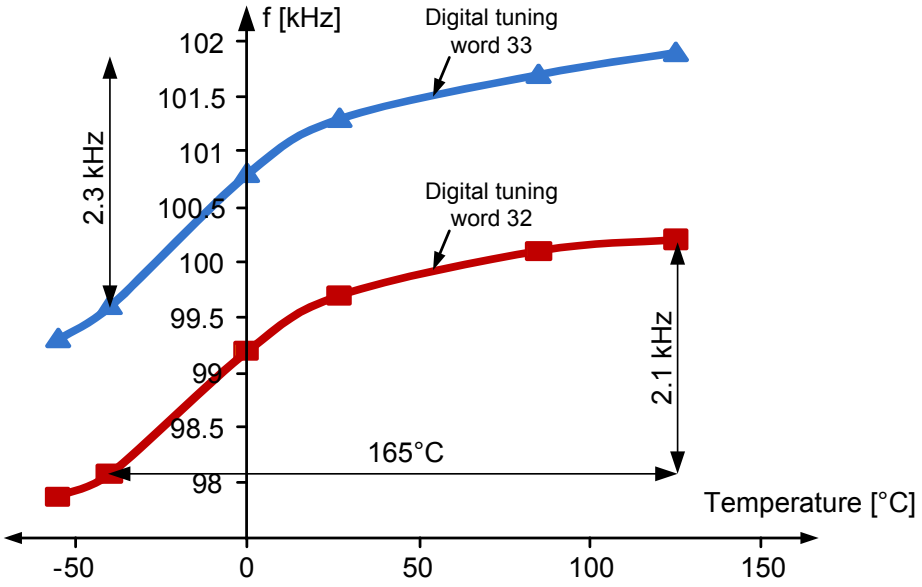

Figure 58: Measured frequency drift over temperature

6 System Power Up

The oscillator is embedded in an environment consisting of a bandgap and a voltage regulator. The latter one is necessary to get a low power supply for the digital state machine. This state machine is powered in the *Deep Sleep* modes and hence should have a very low power consumption. Therefore different power domains (PD) are introduced, namely 3.3 V and 1.5 V. The regulated 1.5 V are also used in the oscillator. The analog system is shown in Fig. 59. The different power domains are clearly visible. The focus in this picture is on the inverters which switch the transmission gates of the oscillator to tune it. If the 1.5 V PD is turned on before the bandgap reference voltage has started up properly, the voltage regulator cannot work, then the inverters in the section of the oscillator as shown in Fig. 59 are not working. This would cause all PMOS transistors in the transmission gates to be on, and hence would short resistor R_{2_2}. Therefore at the output of the bandgap a false bandgap voltage would occur and hence the voltage regulator cannot regulate to the required 1.5 V.

To circumvent this problem NMOS transistors are included between, as shown in Fig. 60, the resistor tapped voltages from the bandgap reference and the transmission gates of the oscillator. Important to note that these NMOS transistors are switched in the PD 3.3 V and hence are not influencing the proper operation of the system because they can be switched before the voltage regulator has started up.

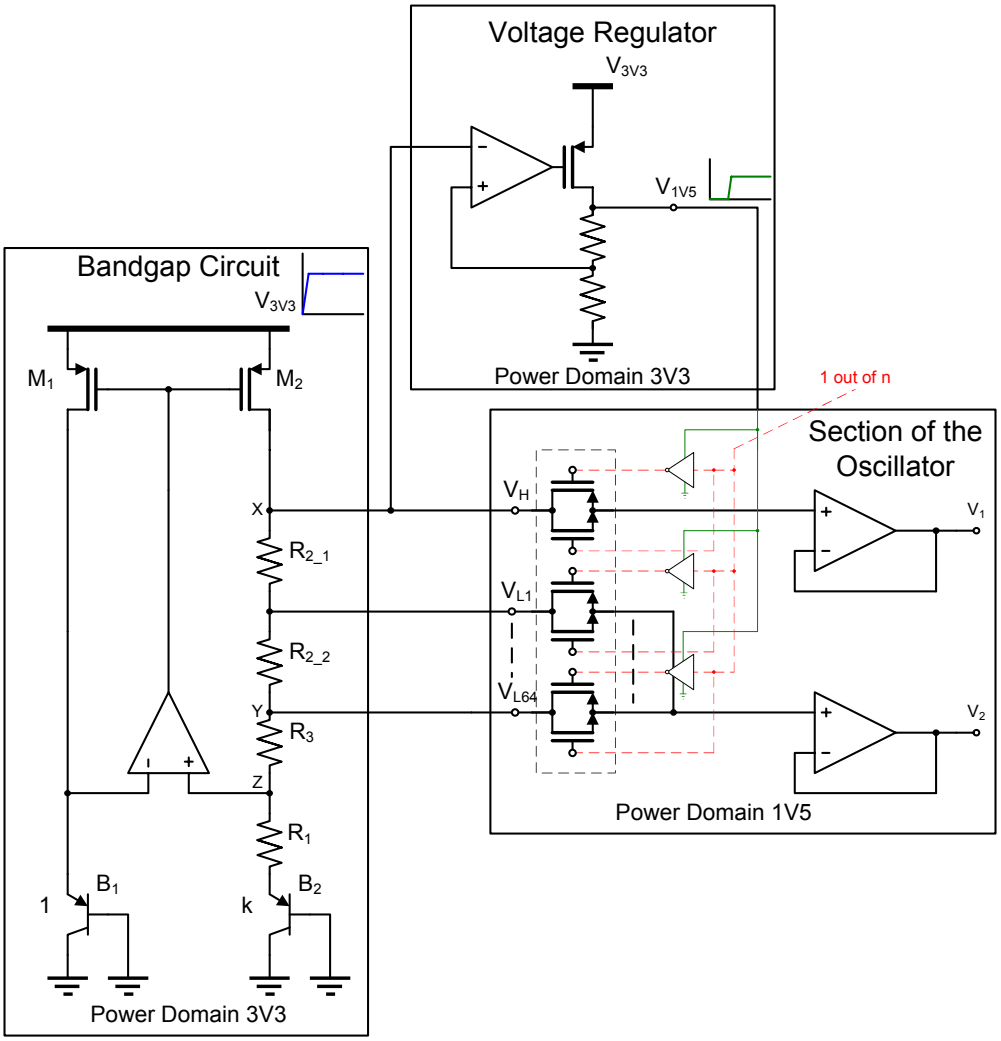

Figure 59: System of the power managment unit (PMU)

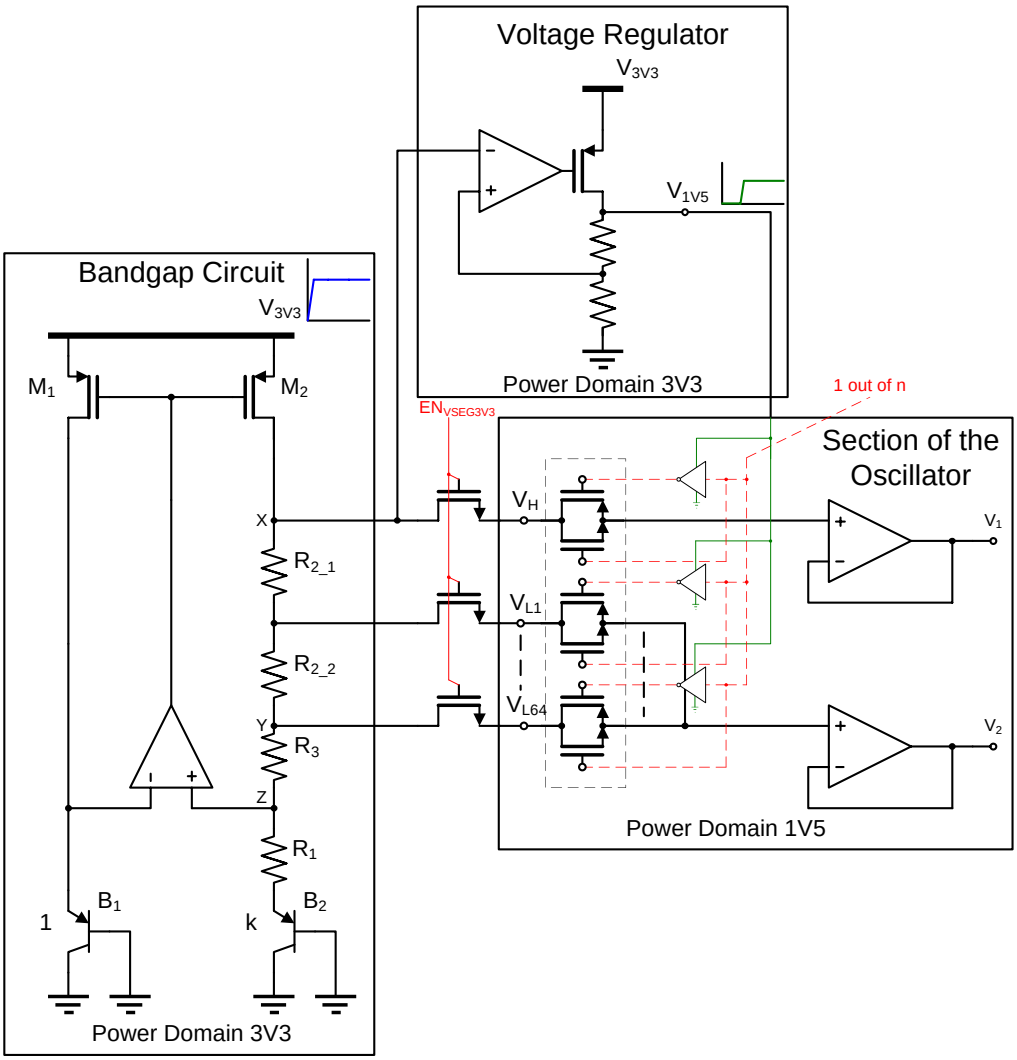

Figure 60: System of the PMU with NMOS transistors to ensure proper starting of the oscillator

7 Layout

In an integrated circuit the layout is a very important part. All geometries and shapes of all devices of the circuit are determined by the layout process, positioning and connecting the devices properly. The result is the structure of the masks used in the fabrication process determined by the geometric shapes in layout.

Inaccuracies during the fabrication process lead to variations in device parameters. Therefore a set of design rules have to be considered which have the task to guarantee the functionality of the circuit with respect to fabrication tolerances. These design rules include minimum spacing of metal lines, minimum width and length of shapes, diffusion spacings, various layers, i.e analog layer dual gate oxide layer, p-implant layer. With the layout versus schematic rules we can check if the devices have the correct shapes and geometries and if the connections between these devices are joined correctly.

7.1 Layout of the RTC with the Decoder and Bandgap

For this thesis the layout of the oscillator explained in Section 4.1 was build. The schematics are depicted in Fig. 28 and 41 and the layout is shown in Fig. 61.

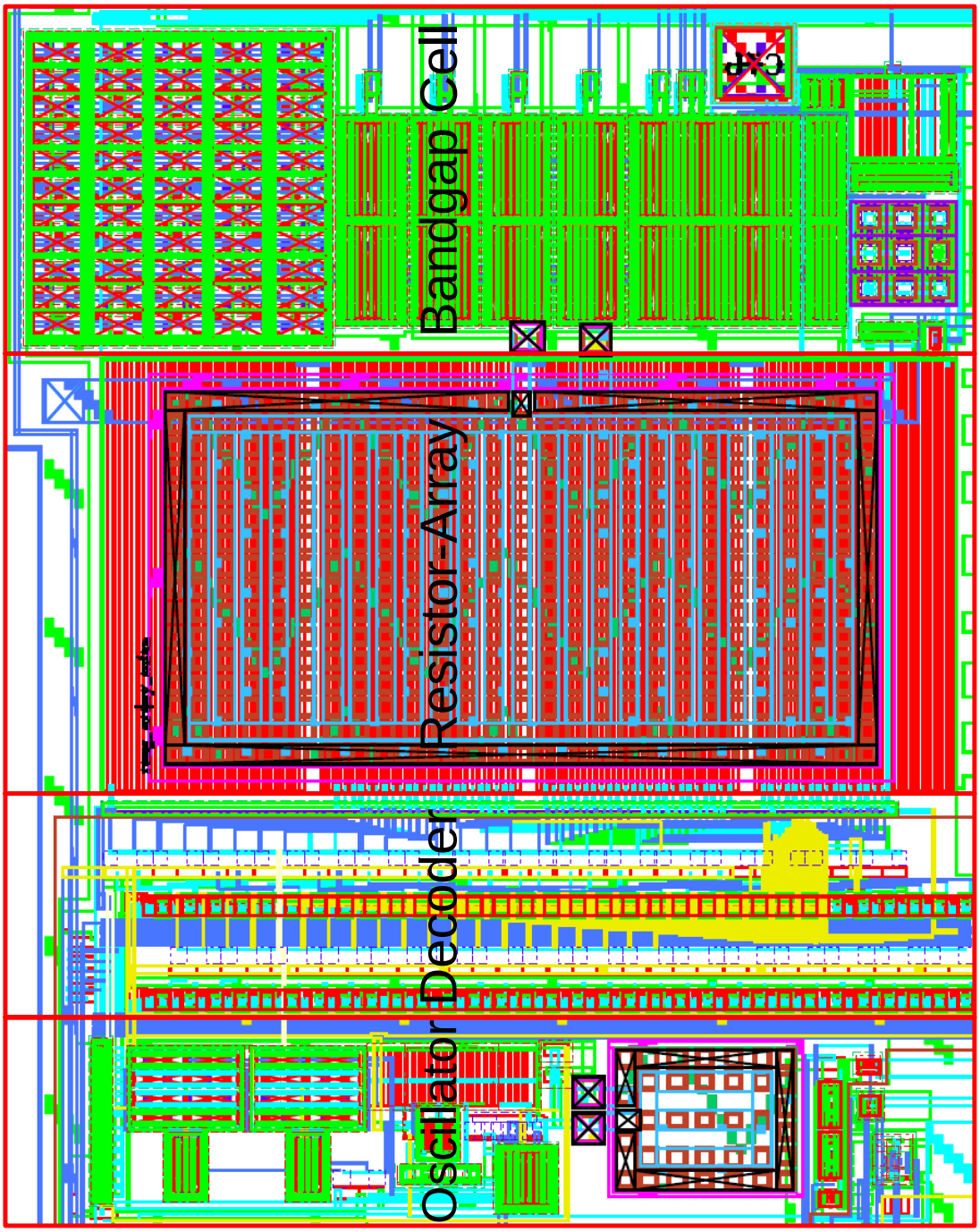

Figure 61: Layout of the oscillator proposed in this thesis for the project CHOSeN

Key figures	This work	De Vita [15]
Supply voltage	1.5 V	1 V
Current consumption (simulated)	min 156n typ 320 nA max 1070 nA	1140 nA (typ.)
Oscillation frequency	100 kHz	80 kHz
Tuning range	87 kHz - 134 kHz	N/A
Frequency steps	2.24 kHz/LSB	N/A
Measured frequency drift	2.3 %/165°C	
	140 ppm/°C	842 ppm/°C
Area	0.05 mm²	0.24 mm²
Process	CMOS 130 nm	CMOS 350 nm

Table 2: Measured and simulated oscillator key figures

8 Conclusion and Future Work

8.1 Summary

The aim of this thesis was to find a topology of a voltage controlled oscillator embedded in a power management unit (PMU) of a smart transceiver. An oscillator is presented using an RC product to define its frequency. With this approach a simulated frequency of 100 kHz is obtained while consuming a simulated current of typ 320 nA from a 1.5 V Supply as listed in Tab. 2. The frequency can be adjusted from 87 kHz to 134 kHz by using a 6 bit register as shown in Fig. 57.The oscillator is used to define precise sleep cycles and to drive a small digital state machine. Thus here we have another application of polling.

8.2 Future Work

If the oscillator characteristics are considered, there is still some room for improvements. For example the comparator of the implemented oscillator shows some discrepanies when the simulated and the backannotated circuit is considered. Optimization concerning the simulated delay time and the backannotated is still a grave issue, because it alters the temperature stability of the frequency.

In order to get a more precise tuning behavior a tuning can be imple-

mented which take both resistor and capacitor in account. Therefore a smaller decoder could be used and instead some of the capacitors could be binary weighted.

A Appendix A VerilogA Model of a 6bit Decoder: One out of 64 Switches

A VerilogA model of the decoder was developed in order to carry out simulations of the oscillator in a reasonable time. It was modeled with a 6 bit input and a 64bit output. Sometimes such a decoder is called “one out of n” or “one hot” decoder.

```
// VerilogA for LIB_UNTERKIRCHER, Decoder, veriloga
`include "constants.vams"
`include "disciplines.vams"
//Decoder 6 bit to 64 bit 1 out of 64
//
//ctrl[1:6]: [V,A]
//EN[1:64]: [V,A]
//
//INSTANCE parameters
//       tdel, trise, tfall = {usual} [s]
//       vlogic_high = [V]
//       vlogic_low = [V]
//
module Decoder(EN, ctrl);
output [1:64] EN;
electrical [1:64] EN;
input [1:6] ctrl;
electrical [1:6] ctrl;
integer code;
real vd[1:64];
integer i;
parameter real vhigh=1.4;
parameter real vlow=0.1;
parameter real tdel=0 from [0:inf);
parameter real trise=0 from [0:inf);
parameter real tfall=0 from [0:inf);
analog begin
        code=(V(ctrl[1])+2*V(ctrl[2])+4*V(ctrl[3])+8*V(ctrl[4])
                +16*V(ctrl[5])+32*V(ctrl[6]))/1.5;
        code=code+1;
//the code should run from 1 to 64 and not from 0 to 63
```

```
                for (i=64;i>=1;i=i-1) begin
                        if (i==code) begin
                                vd[i]=vhigh;
                        end else begin v
                                vd[i]=vlow;
                        end
end

generate i (64,1) begin V(EN[i]) <+ transition(vd[i],tdel,trise,tfall) ;
end

end
endmodule
```

References

[1] "http://www.chosen.eu."

[2] M. Kuorilehto, M. Kohvakka, J. Suhonen, P. Hï¿œmï¿œlï¿œinen, M. Hï¿œnnikï¿œinen, and T. D. Hamalainen, *Ultra-Low Energy Wireless Sensor Networks in Practice: Theory, Realization and Deployment*. Wiley, 2008.

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