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Novel interconnect technologies for packaging of microelectronic power devices

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Engineering - this is where the semi-skilled workers realize the work of better minds.

(Dr. Sheldon Cooper)

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Abstract of the thesis

In order to function a microelectronic chip has to be connected to the macroscopic world and at the same time it has to be protected from harmful environmental influences. For this purpose the chip is packaged, which in most cases involves the attachment of the bare silicon chip to a metal substrate that provides the necessary mechanical stability, electrical connection and cooling. This thesis deals with novel interconnect technologies to create this joint between the silicon chip and the carrier substrate.

One method extensively studied in this work is diffusion soldering. It allows the formation of soldering joints with a thickness in the range of a few micrometers which can withstand service temperatures much higher than the soldering temperature. The formation of intermetallic phases during the process was investigated by various methods including in-situ X-ray diffraction and focused ion beam microscopy. Based on these results a semi-empirical model was found to describe the temperatures dependence of the reaction speed for various material systems.

An important factor for the quality of such a joint is next to the process parameters the condition of the used materials. It was found that during sputtering of the eutectic gold/tin alloy, which is commonly used as a solder, significant amounts of the discharge gas can be incorporated in the film. This causes voids in the joint affecting its properties negatively. The effect is described by a model of elastic collisions and can be avoided by replacing the lighter discharge gas argon with the heavier xenon.

As an alternative to soldering the sintering of silver nanoparticles is explored. The nanoparticles form interconnects at low temperatures without the transition to a liquid phase or the necessity of a wafer backside metallization. The produced joints were tested in terms of the mechanical adhesion and their electrical performance. The results make this backside metallization-free die attach seem unsuitable for the attach of power device but it may find applications with logic chips, which do not require such high electrical conductivities.

Kurzfassung der Dissertation

Damit ein mikroelektronischer Chip voll funktionsfähig ist, muss er einerseits mit der Makroskopischen Welt in Verbindung stehen und andererseits aber auch vor schädlichen Umwelteinflüssen geschützt sein. Zu diesem Zweck wird der Chip verpackt, was in den meisten Fälle die Fixierung auf einem metallischen Substrat miteinschließt, welches für die notwendige mechanische Stabilität, elektrischen Anschlüsse und Kühlung sorgt. Diese Dissertation beschäftigt sich mit neuartigen Fügetechnologien um diese Verbindung zwischen dem Silizium Chip und dem Trägersubstrat herzustellen.

Ein großer teil dieser Arbeit behandelt die Methode des Diffusionslötens, mit welcher Lötverbindungen mit Dicken von nur wenigen Mikrometern hergestellt werden können. Diese Verbindungen können Temperaturen aushalten die deutlich über der Löttemperatur liegen. Mittels verschiedener Methoden wie in-situ Röntgen Diffraktometrie und Fokussierter Ionenstrahl Mikroskopie wurde die Dynamik der Bildung der intermetallischen Phasen während des Prozesses untersucht. Basierend auf diesen Ergebnissen wurde ein halb-empirisches Modell erstellt um die Temperaturabhängigkeit der Reaktionsgeschwindigkeit für verschiedene Materialsysteme beschreiben zu können.

Neben der richtigen Wahl der Prozessparameter ist der Zustand der Ausgangsmaterialien ein wichtiger Faktor für die Qualität der Lötverbindung. Während des Sputterns der eutektischen Gold/Zinn Legierung, die oft als Lot verwendet wird, kann es zum Einschluss von Entladungsgas in den Film kommen. Dies führt weiter zu Hohlräumen in der Fügestelle, die deren Eigenschaften negative beeinflussen. Der Effekt kann vereinfacht durch ein elastisches Stoßmodell beschrieben werden. Wird das leichte Entladungsgas Argon durch das schwerere Xenon ersetzt wird der Gaseinschluss vermieden.

Als Alternative zum Löten wurde das Sintern von Silber-Nanopartikeln getestet. Mit Hilfe der Nanopartikel können Verbindungen hergestellt werden ohne den Übergang zur flüssigen Phase und daher auch ohne die Notwendigkeit einer Metallisierung der Waferrückseite. Die hergestellten Verbindungen wurden auf ihre mechanische Haftung und elektrische Leitfähigkeit getestet. Durch die erzielten Resultate erscheint es unwahrscheinlich das diese Methode für Leistungshalbleiter zum Einsatz kommt. Ein möglicher Anwendungsbereich sind jedoch logische Schaltungen die weniger gute elektrische Leitfähigkeit vorraussetzen.

1 Introduction to semiconductor manufacturing

The development of microelectronics is considered one of the most important achievements of our times, comparable to the invention of the steam engine or the discovery of electricity. It has revolutionized the fields of communications, information processing, and computing and the technology is still evolving rapidly. It has become an almost invisible part of our everyday lives, and yet our modern life style wouldn't be possible without it. Microchips are in everything from mobile phones to vacuum cleaners. A modern medium-sized car for instance contains more than 1,000 chips and up to 80 networked electronic systems.

Electronic devices are often used for vital tasks such as the trigger of an airbag, the control system of a plane or a cardiac pacemaker. Thus reliability is a very important theme and a lot of engineering effort and money is spent to prevent untimely failures that might have fatal consequences.

The reduction of power consumption has not just recently become another important issue. The internet is based on server farms around the world which consume electric power and transform it into heat. All this energy is lost due to the inefficiency of electronic devices, from the power converter to the processor. Including the energy necessary for cooling of the servers about 14 GW worldwide are consumed for only this purpose. [1] This example is to illustrate that the increase of the efficiency of microelectronic devices has great potential to contribute to an economical handling of energy.

Because electronic devices are used so much it is becoming increasingly important that they are environmentally friendly not only in their function but also by the materials they are made of. The cycle life time of electronic products is becoming shorter and more and more electronic scrap is disposed in landfills. Often these parts contain hazardous materials such as heavy metals or

halogens, which over time can leak out and poison ground water and people. Thus there are governmental regulations in many countries that ban the use of these harmful materials in electronics manufacturing.

This thesis considers one small aspect of the total semiconductor manufacturing process: the bonding the silicon that contains the transistors to the metal frame that holds the silicon in the final product, the die attach. Traditionally the silicon was soldered to the frame using Pb/Sn solder. The lead has been banned due to environmental concerns. Here alternatives to the traditional soft soldering using Pb/Sn are described and it is shown that they have better performance and greater reliability than the traditional soldering.

In the first chapter a short review of semiconductor processing is given so that the reader can get an impression of the place of the die attach among the many processes involved in the production of a microelectronic device. The production line starts with the preparation of the raw materials, the growth of the semiconductor crystals, which are cut into the raw wafers. The electrical functionality is given to the semiconductor in the planar process, involving many unit processes. In the last processing block, the back end of line, the raw chips are packaged to form functioning electrical circuits.

The material presented in this chapter was in parts obtained during the work of this thesis but is not of scientific novelty. Its purpose is to serve as an introduction for the reader, to make him familiar with the topic of semiconductor packaging.

1.1 Crystal growth

The vast majority of semiconductor devices are based on silicon due to its great abundance, electronic properties and relatively easy processing. Elementary silicon is won by the reduction of quartz sand with carbon at temperatures just below the melting point of silicon. Iron is added to the reaction chamber to prevent the formation of silicon carbide. [2] To be used for electronics manufacturing the silicon has to be further purified. The silicon is reacted with hydrofluoric acid to form trichlorosilane, which is liquid at room temperature and thus can be separated from

impurities by distillation. Then the process is reversed. The trichlorosilane is heated together with hydrogen to a temperature of 1100°C and elementary silicon is precipitating from the gas phase in polycrystalline form. The so called electronic grade silicon has only one impurity atom every one billion silicon atoms, but often this is not enough for the production of devices. [3]

To be used as a substrate in semiconductor technology the silicon has to be in a single crystalline form. The majority of the single crystal silicon ingots are grown by the Czochralski method. The polycrystalline silicon is melted in a rotating quartz crucible and dopant atoms are added to achieve the desired electronic properties. A silicon seed crystal is dipped into the melt and slowly withdrawn. The liquid silicon solidifies upon contact with the seed crystal, adopting its crystalline orientation. This way a cylindrical silicon single crystal (ingot) is made. The ingot can be grown at a speed of $2 - 20$ cm/s, where its diameter is the smaller the faster the pulling speed is. [4] A disadvantage of the Czochralski method is that impurities from the walls of the crucible like oxygen, carbon or boron can get into the silicon. Thus for the production of ultrapure silicon the floating zone process is applied. This process relies on the fact that most impurities have a higher solubility in the melt than in the crystalline material. A cylinder of polycrystalline silicon is mounted vertically, so that its upper end is touching the seed crystal. The top of the cylinder is locally melted by a high frequency magnetic field so that the liquid can wet the seed. The disc shaped liquid zone is moved from one end of the cylinder to the other, taking the impurities with it and concentrating them on one end of the crystal. This way, single crystals with impurity concentrations down to 10^{10} cm^{-3} can be grown. [2]

Next the ingots are sliced into thin wafers by an annular diamond blade or a wire saw. The wire saw inflicts less damage to the wafer surface but has also a lower cutting speed. The surfaces produced by the cutting process are rough; defects in the crystal lattice have been introduced. Thus about 50 µm of the surface of the silicon wafer have to be removed by mechanical and chemical methods, so that the undisturbed crystal surface is exposed. [5] Currently the standard diameter of silicon wafers is 200 mm, but 300 mm are already being implemented. An increase in wafer diameter is connected to significant reduction in production costs of the semiconductor devices as the number of chips that can be made from a single wafer is roughly proportional to the square of its diameter.

1.2 Planar manufacturing technology

The basis of the fabrication of highly integrated circuits on silicon is the planar process. It consists of a series of unit processes which are applied to the complete wafer surface. In most cases their effect is limited by suitable masks to specific locations on the semiconductor enabling the processing of hundreds of billions of transistors on a single wafer at the same time. By sequentially applying hundreds of these unit processes, the electrical functionality is given to the semiconductor material. Generally the wafer processing can be subdivided in two parts: The front-end-of-line refers to the patterning of the individual devices directly in the semiconductor, whereas the back-end-of line includes the interconnection of the devices with metal wiring on the wafer.

1.2.1 Oxidation

A typical unit process sequence starts with the oxidation of the silicon. The silicon oxide layer can serve as an insulator, e.g. the gate oxide of a transistor, a mask to protect the underlying silicon locally from a subsequent process, a diffusion barrier to inhibit the diffusion of dopants out of the silicon, or simply as a passivation layer to protect the surface of the wafer. The oxide layers used in the planar process are either generated by thermal oxidation or chemical vapor deposition. Thermal oxidation can be split into dry and wet oxidation. Dry oxidation uses oxygen as the reactive gas, which produces high quality oxide layers at low speed which have a higher resistivity to electrical stress whereas for wet oxidation water is added to the oxygen gas. This speeds up the reaction, but decreases also the layer quality. If there is not silicon available for oxidation, for instance on an aluminum metallization, the oxide can be deposited directly. The most important methods for this process are the tetraethyl orthosilicate (TEOS) deposition or the low temperature oxidation of silane. The high quality and superior electrical properties of silicon oxide is the most important reason why silicon is still the dominant material in semiconductor industry.

1.2.2 Lithography

To pattern the silicon oxide layer a lithography step is applied. In this process the layout information is transferred from a mask onto the wafer. The layout is recorded on a set of masks which defines the specific patterns necessary for the device fabrication, e.g. the gate area of a transistor. They are recorded on a radiation sensitive film, the resist, which the wafer is coated with. This resist is usually an organic compound that changes its properties upon exposure to radiation. The resist can be either positive or negative. Positive resist is dissolved during the development where it has been illuminated and the not illuminated areas stay covered. The kind of radiation used mainly determines the minimum feature size that can be transferred as it is limited by the wavelength. Standard lithography tools work with ultra violet light at wavelength of 436 nm and 365 nm which is the G- and I-line of the mercury spectrum or with a deep UV laser at 248 nm and 193 nm. [3] The minimum feature sizes that can be resolved on planar surfaces with this technology are 0.8 µm and 0.4 µm respectively. Advanced technologies like X-ray lithography (XRL), electron projection lithography (EPL), and ion projection lithography (IPL) are currently introduced into commercial semiconductor production allowing the generation of feature sizes down to 32 nm. [6]

1.2.3 Etching

To transfer the patterns of the resist layer to the underlying material, an etching process is applied. In semiconductor processing the most common materials to be etched are silicon oxide, silicon nitride, silicon, aluminum, tungsten and titanium. The etching can be achieved chemically by wet etching, physically by dry etching or by a combination of both.

Wet etching transforms the solid material into a liquid compound by the application of an acidic or alkaline solution. The wet etching is generally very isotropic and selective, which means that the etch rate is similar along all directions, but it depends strongly on the material that is removed. The process suffers from poor reproducibility because the etch rate is very unstable and extremely difficult to control. The isotropy of the process also limits its applicability as it results in a so-called under etching effect which can lead to a partial or full detachment of the mask from

the underlying material and makes it unsuitable to transfer patterns with sub-micron features. [7] Furthermore the devices are often contaminated by etching agents. Thus wet etching is mainly used for the removal of whole unpatterned layers.

With dry etching in contrast, reproducible and homogenous etching of most materials used in the planar process is achievable. In this technique the material is removed by momentum transfer between plasma particles and the target material. The etching can be isotropic as well as anisotropic depending on the process parameters like the pressure in the plasma chamber. The lower the pressure the higher is the resolution but the lower is the selectivity. With the right parameter set it is possible to transfer structures with sub-micron features.

1.2.4 Implantation

The patterns produced this way can again be used as masks to locally introduce dopant impurities into the crystal. Typically a masking layer of 1 µm thickness is sufficient to absorb the ions. Apart from silicon dioxide also silicon nitride, polysilicon, aluminum or some photo resists are suitable as masking layers. [6] The dopants can enhance, attenuate or inverse the substrate doping in specific areas as needed for the functionality of the device. As acceptors elements of the third group, i. e. boron, aluminum, gallium and indium are available. Of these only boron has a sufficient solubility in silicon to achieve a high conductivity. As donors elements of the fifth group could be used in principle, but only phosphor and arsenic have a sufficient solubility and antimony can be used only for weak doping. Historically the impurities were introduced by alloying and diffusion, but due to reason of reproducibility nowadays in industry mainly ion implantation is used. [2] A beam of ionized dopant atoms is accelerated in an electrical field towards the wafer. The ions penetrate into the target and dissipate their kinetic energy by elastic and inelastic collisions with the atoms of the substrate material. The penetration depth of the ions is proportional to their acceleration voltage, which can be controlled very accurately. The absolute dose of ions can be controlled by the charge introduced to the substrate. Thus it is possible to generate very well controlled doping profiles, which is necessary for achieving the desired electrical functionality. The bombardment with the high energy ions damages the lattice

of the semiconductor crystal and thus alters its electrical properties. Furthermore the dopants introduced by implantation initially reside on interstitial lattice site where they are electrically inactive. To heal the crystal and electrically activate the dopants, a high temperature anneal is necessary after implantation.

1.2.5 Deposition

The completed semiconductor wafer is composed of many layers with different properties and functions. They are either part of the integrated circuit or serve as sacrificial layers that are removed in a later processing step. These layers have to be deposited on the substrate with temperature and intrinsic stress as low as possible. They can be single crystalline, polycrystalline or amorphous. Most often deposition is used to produce on-chip interconnections of the single circuit elements. If those interconnections would be done on the same level as the active elements they would consume up to 80 %of the surface area of the chip. [8] Therefore multilevel structures have been developed, consisting of patterned conducting layers and silicon dioxide as insulator in between. As conductor aluminum, copper and also polycrystalline silicon are available. The latter is only used for short interconnections with low current densities due to its high resistivity. The conducting layers are connected with each other by vertical interconnect areas (vias). Generally there are two lower levels of polycrystalline silicon and 2 to 6 levels of metal on top. [3] Especially power devices require an electrical connection not only on the front side but also on the back side, which often has to carry large currents. Usually this backside metallization is not patterned and has to provide and mechanically stable connection with a low thermal and electrical resistivity. Often all of this cannot be achieved by a single metal layer. Therefore a multilayer stack, consisting of a contact layer, a diffusion barrier, a wetting layer and an oxidation protection layer is applied. The contact layer has to provide good ohmic contact and adhesion to the semiconductor; the diffusion barrier prevents intermetallic compound formation between the contact layer and the cover layer, which would have a negative influence on their performance and the cover layer provides the interface to the package and has to be chosen according to the chip-package interconnection technology used.

The different technologies which are available for deposition can be divided in chemical vapor deposition (CVD), electrochemical deposition (ECD), and physical vapor deposition (PVD).

1.2.5.1 CVD

CVD is mainly used to deposit polysilicon, silicon oxide or silicon nitride. It is based on the thermal dissociation of chemical compounds in the gas phase upon contact with the hot substrate. The precursor gas contains all components necessary for the growth of the layer. The substrate itself does not take part in the reaction. The gas molecules are split in a solid part that attaches to the substrate surface and a gaseous part which is removed by convection. [9] This process requires a high temperature of the substrate which is not always acceptable. A technology to overcome this problem is the plasma enhanced chemical vapor deposition (PECVD), where the dissociation of the molecules is enhanced by high-frequency gas discharge. PECVD can be done in the temperature range between 250 °C and 350 °C, whereas for standard CVD often 900 °C are necessary. [10]

1.2.5.2 ECD

Electrochemical deposition or simply electroplating is another process widely used in semiconductor industry for the deposition of metal layers.[11] It has several advantages compared to PVD and CVD due to its low cost, low processing temperature, and good ability to fill structured surfaces. [12] Simplified, the deposition of the metal layer is achieved by putting a negative charge on the wafer and immersing it into a solution which contains a salt of the metal, called the electrolyte. The wafer acts as the cathode of the electrolytic cell and the positive metal ions in the electrolyte are attracted to it. Upon contact with the wafer the ions are reduced and converted into their metallic form. The ions can be supplied directly from the anode, which is in this case consumed over time, or they can be added directly to the electrolyte and the anode is made from an inert metal like platinum. A requirement for ECD is a conducting substrate. The bare silicon wafer cannot be plated directly but a conducting seed layer is needed, which has to be applied in a separate process step by PVD.

For industrial application it is important to achieve a good thickness uniformity of the deposited layer as well as high deposition rate. Therefore commercial electroplating is a very sophisticated operation with means for agitation, filtration, electric field shaping, temperature control, and multistep or pulsed current programs. Organic additives are added to the electrolytes to improve the film morphology and surface roughness. The right part of Figure 4 shows an industrial scale plating line for deposition of multilayer metal stacks as it was used for the work in the thesis.

1.2.5.3 PVD

Physical vapor deposition involves the condensation of a vapor from of atoms, molecules or clusters on a substrate surface. The material physically adsorbs to the surface without any chemical reactions and thereby forms a solid film. Typical PVD processes include evaporation, molecular beam epitaxy (MBE) and sputtering.

The simplest and oldest method to deposit metal layers is thermal **evaporation**. The metal is heated either by resistance heating in a tungsten carrier or by an electron beam in high vacuum (HV) so that the atoms escape into the gaseous phase. In the vacuum there are only little particles so that the mean free path of the metal atoms is larger than the distance between the evaporation source and the wafer. The particles travel on strait trajectories towards the wafer and condense on its cooler surface in polycrystalline form. Because their kinetic energy is so low (~0.1 eV) they cannot damage the substrate surface. [13] Due to the straight trajectories of the metal atoms the method has very poor side wall coverage on structure wafer front sides. Thus it is most suitable for cheap coating of planar wafer backsides.

MBE is mainly used to deposit thin layers of doped silicon or other semiconductor materials. Pure silicon or another semiconductor is evaporated by an electron beam in an ultra high vacuum (UHV) chamber. At the same time dopants can be added to the beam by resistance heated Knudsen effusion cells. The atoms hit the surface of the substrate where they form homoepitaxial, single crystalline layer. [10] The deposition temperature of about 700°C is too low for significant diffusion of the dopants. Thus it is possible to achieve very well defined pn-junctions with this method. A major drawback is the slow layer growth of only 1 µm/h and the necessary UHV.

Only about 10 wafers can be processed per tool per day and it is therefore not suitable for mass production. [3]

To overcome the disadvantages of thermal evaporation, **sputtering** is widely used for metallizations in semiconductor manufacturing. [14] Typically in sputtering, inert gas ions are accelerated towards a target. These ions knock atoms of the target loose which diffuse in the gas phase over to the substrate where they condense and form a solid film. This process is not affected by the temperature and therefore it is possible to produce a gas phase from a cold solid. [15] The interaction between the high energy inert gas ions and the atoms of the solid can be seen as an elastic collision. For this case the momentum transfer between two particles is most efficient when the particles have similar mass. The atoms in the sputtered target, are not isolated but they are rather within a matrix of metal atoms. Thus the impact of high energy ions does not only sputter atoms, but also causes damage to the target. The dependence of the sputtering efficiency on the energy of the ions, the involved materials and other factors is complicated. It can be described by a quantity named sputtering yield, which is defined as the ratio of emitted atoms of the target material to the number of incident particles. A schematic of the sputtering process is shown in Figure 1.

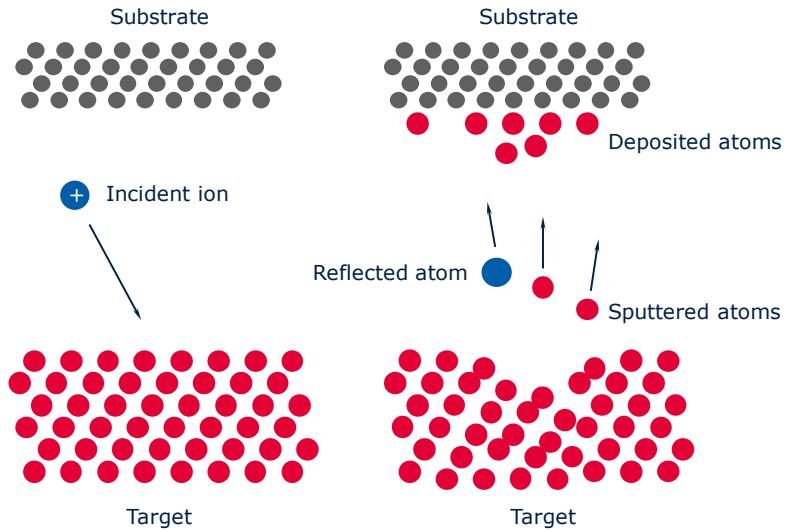

Figure 1: Schematic of the sputtering process. An incident high energy ion transfers momentum to atoms of the sputter target, vaporizing the matter. The sputtered atoms condensate on the substrate.

Once the atoms are in the gas phase they readily condense on any surface available as they are not in thermal equilibrium with the surroundings. A wafer is positioned in closed distance to the target, so that most of the depositing atoms can form thin homogeneous films on its surface. When the atoms condensate on the wafer surface, their kinetic energy as well as their energy of recrystallization is converted to heat. Therefore the wafer is heated during the process until it reaches a radiative equilibrium with its surroundings. The final temperature depends very much on the deposition rate.

The most prevailing method for sputtering in semiconductor industry is discharge sputtering. In this setup the sputtering chamber is designed like a discharge tube. It is composed of two facing electrodes in the sputter chamber. The wafer resembles the anode which is grounded and on the cathode, to which the target is fixed, a high negative voltage is applied. The space in between the electrodes is filled with a noble gas, usually argon. Electrons are emitted from the target and accelerated in the electrical field towards the wafer. They collide with the Argon atoms and ionize them. The generated ions and electrons are accelerated themselves, hit other Argon atoms and cascade is started. Eventually the ions hit the target surface, where the generate secondary electrons and free neutral atoms. The secondary electrons are necessary to sustain the plasma and the neutral atoms make up the deposited material. [15]

In order to achieve a high deposition rate which is a requirement for an industrial process, a high plasma density and a high gas pressure of about 100 Pa is required, but this in turn hinders the sputtered neutral atoms to reach the wafer. Additionally the secondary electrons that are accelerated in the electrical field are heating the target material and it can ultimately exceed its melting point. For this reasons a magnetic field parallel to the target surface is applied, which forces the electrons on a cycloid path close to target surface. The ion generation is strongly enhanced in this very limited space and sufficient ions are generated even at gas pressures down to 10^{-2} Pa. [13] This allows the sputtered atoms to travel from the target to the wafer without being scattered by the discharge gas atoms. The method of sputtering using an electrical and a magnetic field is called magnetron sputtering. For reasons of conformity the electrical field is often rotated around an axis perpendicular to the wafer surface at low frequencies. Figure 2 shows the setup of the wafer in the magnetron sputtering chamber.

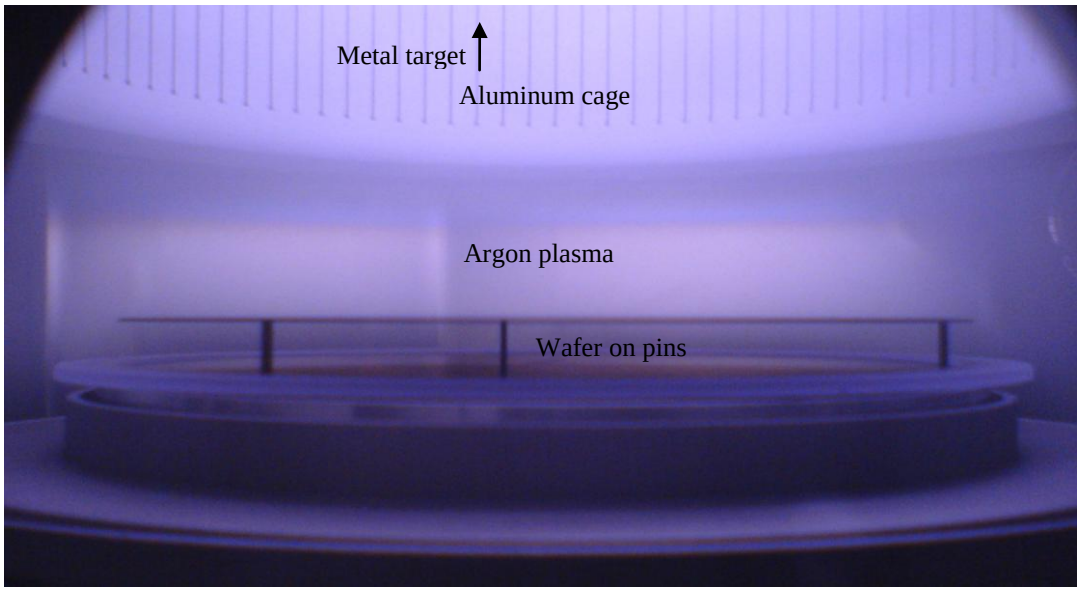

Figure 2: Argon plasma inside a vacuum chamber during plasma etching. The wafer is resting on three pins underneath the target in the loading position. For sputtering it is lifted up closer to the target. (Courtesy of Mark Harrison)

Some of the noble gas ions that hit the target get implanted but most of them are reflected. Their charge is neutralized upon impact and they are no longer affected by the electrical field. For an acceleration voltage of about 1 keV, their energy is in the range of several tens to a few hundreds of electron volts. This energy strongly depends on the target material and the discharge gas used. The more similar the atomic masses of the two elements are, the more energy can be transferred from the discharge gas atom to the sputtered atom and the less energy is left for the reflected atoms. These atoms can collide with the deposited film and hinder its growth. They can directly hit already deposited metal atoms and hammer them inside the deposited film. These atoms reside then on interstitial sites inside the crystal lattice expanding it and causing a compressive stress in the deposited film. [16] This effect is called the “peening effect”.

The reflected noble gas atoms can also be incorporated in the deposited film themselves. They have a kinetic energy high enough to be implanted directly into the metal. [17] An incorporation of the noble gas atoms by simple adsorption is very unlikely, because the adsorption energy of the gas atoms on metal surfaces ranges only from 0.05 to 0.35 eV. [15]

Additionally to these properties, sputtered thin films have a very distinctive columnar structure. [18] The transmission electron microscope (TEM) image in Figure 3 shows a cross section of a

typical sputtered thin film. The eutectic Au/Sn film on top of a titanium film was prepared by magnetron sputtering. Single crystalline columns grow perpendicular to the film surface. As a general rule of thumb the columns are wide and well defined at high temperatures and low discharge gas pressures. At increasing temperature and lower pressure the columns become smaller and thinner and the film surface becomes rougher. [19]

Industrial scale metallization tools often include multiple deposition chambers for different metals together with an automatic wafer handling system. With this setup it is possible to deposit multiple metal layers on top of each other without exposing their surface to the atmosphere before the complete stack is finished. In the left part of Figure 4 a magnetron sputter tool with six chambers that was used for the film preparation in this thesis is shown.

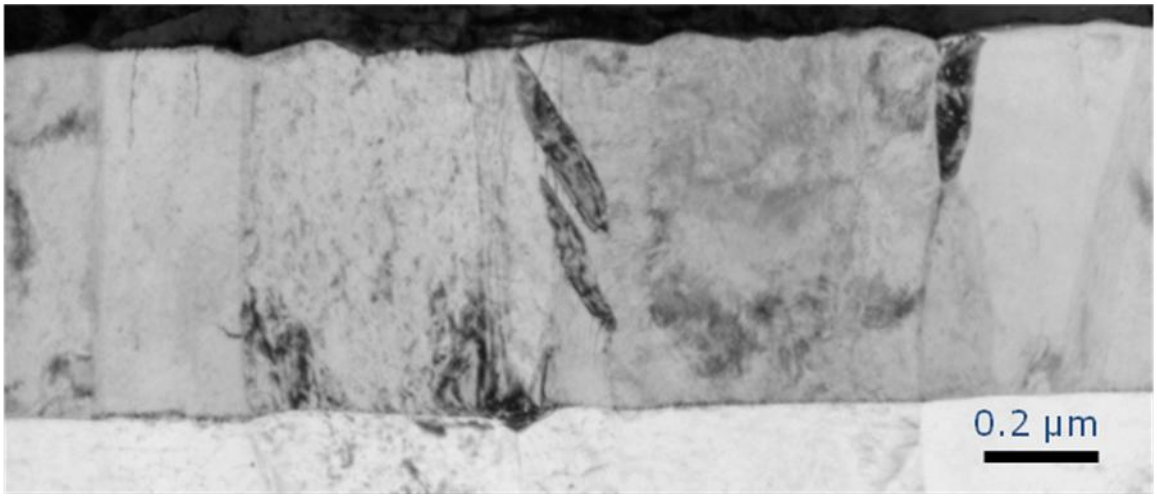

Figure 3: Transmission electron microscope image of a eutectic Au/Sn film on top of a titanium layer. The films were prepared by magnetron sputtering and show the typical columnar structure.

Figure 4: Technical scale equipment used for deposition of metal layers. Left: Sputter tool Oerlikon Clusterline 200 with six sputtering chambers. Right: NEXX Stratus 200 electrochemical plating line

1.2.6 Singulation

After the wafer has gone through all the processes of the planar technology it contains from hundreds to hundred thousands of chips which themselves can consist of one to one billion transistors. The single chips are separated from each other by a 50 to 100 µm wide area, the "scribe line". In this area there are except from test structures no circuit elements, as it is destroyed when the wafers are cut into single chips, the so called dies. In a conventional processing flow, the wafers are mounted on a dicing tape and clamped into a rigid frame. The dicing can be done either by laser cutting or by mechanical sawing, which is the prevailing method with a market share of more than 90 %. [20] For sawing, a diamond blade rotating at high speed with a thickness ranging from 20 to 50 µm is used. The process is abrasive, similar to grinding and produces chipping and cracks at the die edges. To achieve smoother edges and narrower dicing streets a high power Nd:YAG laser is employed. In this technology the material is removed by ablation. The material is locally evaporated and partially deposited on the wafer surface and the sidewalls of the die. To avoid this contamination the wafer surface can be protected by a coating that is washed off after the process. Another possibility is to use a water

guided laser. The laser is coupled into a water beam, tens of microns in diameter, which is washing off most of the generated debris and cools the dicing street (see Figure 5). [20]
After dicing, the chips are ready for the final electrical test and packaging (see Figure 6).

Figure 5: A pulsed high power Nd:YAG laser with a second harmonic generator emitting at a wavelength of 532 nm is guided by a narrow water beam to separate the individual dice.

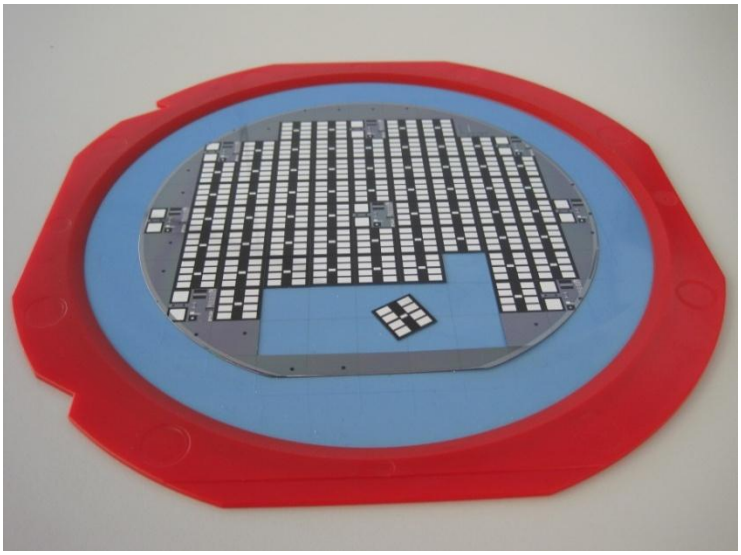

Figure 6: Wafer on dicing foil after singulation. The chips are fully functional and ready for packaging.

1.3 Chip packaging

Electronic packages can contain many electrical circuit components like transistors, diodes, resistors, capacitors and other components, all of which have to be connected with each other to form electrical circuits. To function, the electrical circuits have to be supplied with electrical energy which is partially converted heat. Because all circuits operate best within a certain temperature range, this heat has to be removed sufficiently fast. Thus the package has four major functions: It has to distribute signals; it has to provide connections for electrical power; it is responsible for the heat dissipation and it has to protect the bare dies from environmental influences. The electronic packaging technology significantly contributes to the overall performance of the whole system. It is considered to be the biggest bottleneck in the development of microelectronics, because it controls the system's electrical performance, cost, size and reliability. [21]

Electronic packaging is done on several levels (see Figure 7). All interconnections which are directly integrated on the chip are commonly not considered as packaging. It begins with the interface of the bare semiconductor chip. This is the first level or chip-level packaging. Modern first level chip packages can also contain more than one chip and are then referred to as multi chip modules. Typically these devices are soldered onto printed circuit boards. These cards make up the second level of packaging. In the example of a personal computer this is a graphics card or a random access memory card. The third level of packaging then provides sockets for these cards to be plugged in. In a personal computer this is the motherboard. Often the packaging hierarchy deviates though from this traditional order, depending on the application. [22]

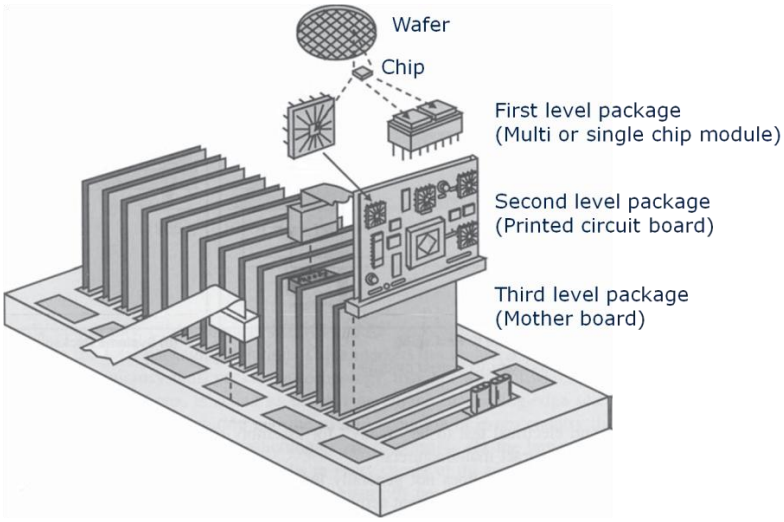

Figure 7: [21] Schematic of microelectronic packaging hierarchy

The first level involves the attachment of one or more bare dice to a substrate, the electrical connection from these chips to the package leads, and the encapsulation. Especially in power electronic systems, chip-level packaging plays an important role because it directly interfaces with the power chip not only electrically but also thermally and mechanically. The requirements to the power package are different from those to the package of a microelectronic integrated circuit. Larger cross-sectional areas are needed and it has to be able to support much higher current flow. Wide bandgap semiconductors, such as silicon carbide, which are currently developed for high power and temperature applications, drive the development of chip level packaging to improve its performance in heat dissipation and thermal management. Rapid progress in semiconductor manufacturing technology in the recent past has enabled the fabrication of smaller and thinner power electronic chips, with thicknesses in the order of only several micrometers. This imposes a serious challenge to the precision of the first level packaging technology. Furthermore power chips are usually installed in heavy machines like trains or windmills and thus a high lifetime of the first level power-interconnections is needed to ensure the long term reliability of the complete system.

1.3.1 Die attach

Most of the work done in this thesis is concerned with the characterization and development of the die attach process. It is only a small part in the production of a microelectronic device, but its quality significantly affects the performance and especially the reliability of the device. The die attach layer often provides an electrical connection, such as the drain of a power MOSFET or the emitter of an insulated gate bipolar transistor (IGBT). Thus it directly affects the electrical characteristics of the chip, such as the turn-on resistance of the device (R_{DSon}). In contrast, the electrical connections of an integrated circuit are usually only on the front side and the die attach layer merely holds the chip mechanically on the substrate. [23]

A low ohmic resistance is a central requirement for the die attach layer in power devices, but even more important is the thermal impedance. The majority of the heat generated by the device is dissipated through this layer. Due to its low thickness and the large area its thermal impedance is much lower than the one of the front side interconnections such as the wire bond or the ball grid array. With a constant power efficiency of the semiconductor device and a maximum operating temperature, the maximum power that can be dissipated by the chip is mainly determined by the thermal properties of the die attach layer. Also a thin chip is advantageous. Although the thermal resistance of silicon is quite low, a thinner layer has still a lower resistance.

Often the reliability of the complete system is highly related to the quality of the die attach layer. Due to the mismatch in the coefficients of thermal expansion between the semiconductor of the device and the metal of the lead frame, a considerable thermomechanical stress can occur during the assembly and operation. The die attach layer not only has to withstand this stress but also needs to cushion it in order to ensure a long lasting stability of the system. Good mechanical properties of the die attach material are essential for the reliability of the device.

Recent governmental restrictions that prohibit the use of potentially harmful substances in the production of electronics impose additional requirements on the die attach process. [24] Lead, which was often used as a die attach material due to its high ductility, was banned and new material systems have to be explored to find a suitable replacement.

Figure 8 depicts the Tresky T-3202 die bonder which was used for the work of this thesis. The diced wafer on the dicing frame is loaded into the machine. The chips are picked from the foil by a vacuum tool from the top. When the tool touches the chip, needles push it up from beneath at the same time, lifting it up from the sticky foil. Then it is moved over the lead frame and aligned with an accuracy of less than 10 µm by an optical camera. If necessary a solder paste or a conductive glue is applied on the position where the chip will be placed with a pneumatic needle dispenser. For soldering the lead frame is heated so that the solder is melted. The chip is then set down on the lead frame with a specified pressure and the connection to the substrate is formed. Figure 9 shows a chip soldered on a lead frame directly after the die attach. This kind of semiautomatic die bonder is design for maximum flexibility in terms of the process parameters and handling of various chip sizes. Fully automatic die bonders as they are used for high volume production are dedicated to a very limited range of products, but are capable of processing a chip in less than 170 ms. [25]

Figure 8: Tresky T-3202 semiautomatic die bonder. The chips are directly picked from the dicing foil and accurately placed on the lead frame.

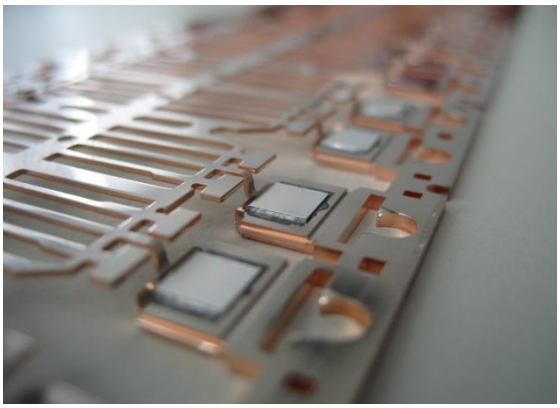

Figure 9: Transistor chips on a nickel plated copper lead frame. The chips have been attached with soft solder.

Several methods for die attach are currently used in industry which are applied for various products and can fulfill the requirements to a certain extend:

1.3.1.1 Conductive adhesives

Electrically conductive adhesives (ECA) are used as a die attach material due to the simple processing and the low curing temperature. [26] They mainly consist of an organic binder matrix and conductive metal fillers. The matrix is usually made of thermosetting polymers, which means that it can be solidified by a curing step and remains in the solid state even if it is subsequently subjected to higher temperatures.. In contrast, thermoplastic materials will reflow at high enough temperatures even if the curing has already been done. Because the polymers are bad electrical and thermal conductors, a large percentage of metal filler has to be added. Generally silver flakes and particles are selected for this purpose owing to their high conductivity. Initially the adhesives also contain solvents that lower the viscosity for easier application on the lead frame. These solvents are then decomposed with the help of catalysts during curing. The ECA can be divided into two types: isotropically conductive adhesives for which the conductivity is the same in all directions and anisotropically conductive adhesives, for which the conductivity is enhanced for one direction. This effect is caused by the application of the pressure from only one direction during the die attach. The metal particles mainly form interconnections in this direction of space. [27]

Compared to solder based technologies, ECA have several advantages. They are more environmental friendly as they don't use lead or flux cleaning. They offer a higher resolution capability and can be processed under milder conditions and in fewer steps which reduces the processing costs. [28] However currently commercialized ECAs are still limited in their properties. The majority of the electrical and thermal conduction is attributed to the metal filler particles. Under the mild processing conditions these cannot fuse together and are only in loose contact with each other. This small area of contact is responsible for the low conductivity of the ECAs. Moreover their performance also suffers significantly at elevated temperature or humidity because polymers tend to get unstable under these conditions. All of the qulaities that ECAs lack, high-temperature stability, high electrical and thermal conductivity, are essential for power semiconductor device attachment. Thus ECAs are rarely used in this field of industry.[29]

1.3.1.2 Soft soldering

Compared with ECAs soft solders have better electrical and thermal conductivity and are thus widely used for die attach. There are different methods used to apply the solder to the joint. In reflow soldering a sticky mixture of metal particles und solder flux is printed on the lead frame to temporarily hold the die in place. The entire assembly is then heated over the melting point of the solder. The liquid solder wets the joint surfaces and the bond is formed upon cooling when the solder solidifies.

Another method is to apply the solder directly to the hot lead frame in the form of a wire, a preform or a drop of solder paste. It is melted upon contact with the hot surface and the die is then placed on the liquid metal.

To minimize stress on the device, the melting temperature of the solder needs to be as low as possible. Thus solder alloys usually contain an element that has a low melting temperature such as tin, indium, lead or bismuth. [20] Lead-bearing solders, especially the eutectic and near eutectic tin-lead alloy have widely been used in the assembly of electronic circuits due to its good mechanical properties (e.g. low melting temperature, wettability, mechanical integrity, manufacturability, and affordable cost). [30] However increasing environmental concern about the

toxicity of lead has caused legislative restrictions on its use in electronics assembly. The European Union has banned lead from many electronic applications since 2006 [31], [32]. In the soldering process, the solder reacts with the substrate material to form the bond. The adhesion is initiated by the formation of an intermetallic compound, which is a chemical reaction. Therefore the soldering environment must provide the conditions that favor this reaction. Initially, the solder and the surfaces that need to be joined are covered with oxides. The melting temperature of these oxides is much higher than the soldering temperature and they cannot be melted in the process. [33] For instance Cu_2O melts at 1235°C and SnO at 1080°C. They also have a lower density than the solder which means that they can float on the surface of the melted solder, forming a barrier that prevents the contact of the joint surface and the solder. This contact is needed to start the chemical reaction and bonding cannot be achieved without the removal of the oxides. For this purpose fluxes are often used. They can reduce the oxides and prevent solder and base metal from further oxidation. In solder pastes they are mixed with the metal particles owing to its pasty consistency. Solder wires often have a hollow core filled with flux. The key components are resin acids, which can react with the oxides forming metal salts. The salt can be dissolved in the molten flux and thus doesn't hinder the soldering reaction.

In the following example the lead free eutectic tin-silver solder is used to attach dice with 500 nm thick nickel backside metallization to copper lead frames in a reflow soldering process. An addition of 3.5 wt.% Ag to the Sn reduces the melting point of the alloy by 11°C to 221°C (see phase diagram in Figure 10). This alloy is quite important as it is generally recognized as the first choice for a lead free solder. [30]

For soldering a 300 µm thick layer of the solder paste is stencil printed on a copper substrate. The dice are then placed on the paste and the whole assembly is then heated in a vacuum oven to the peak temperature of 240°C or 290°C, at which it is held for four minutes. The oven is kept under forming gas atmosphere (4 vol.% H_2, 96 vol.% N_2) to prevent the oxidation of the copper substrates. At the peak temperature, vacuum is temporarily applied to suck out gas bubbles in the liquid solder. During the soldering process, the liquid tin reacts with the copper of the substrate forming the Cu_6Sn_5 intermetallic compound (IMC) on the interface, which is known as the wetting action. This IMC has a melting temperature of 415°C and thus remains solid during a

typical soldering process (see Figure 11). On the other side at the interface of the solder with the nickel backside metallization of the die Ni_3Sn_4 is formed in a similar process. [34] This reaction is much slower though and the intermetallic layer formed is much thinner. The IMC layer links the solder and the substrate together and it is found in all known soldering systems. Without it a soldering process would not be successful. [20] The properties of the IMCs are significantly different from the parent materials. A property that virtually all intermetallic compounds have in common is that they are very hard and brittle materials. On one hand they are crucial for the success of the soldering operation and give strength and fatigue resistance to the joint. On the other hand, if they are abundant in excessive quantities they cause joint embrittlement. [35]

At the soldering peak temperature of 250°C and 290°C, 2 at.% and 4 at.% of copper are soluble in the liquid tin respectively. At room temperature the solubility of copper in tin is very low (0.007 at.%) [35] and so the amount that dissolves during soldering will segregate upon cooling in the form of Cu_6Sn_5 grains. The nucleation happens preferentially at interfaces where the energy barrier that has to be overcome for nucleation is minimal. As can be seen in Figure 12 the Cu_6Sn_5 IMC is not only found at the solder-lead frame interface but also at the interface between the solder and the die. The higher the temperature, the more IMC is formed. At a reflow temperature of 290°C, there is significantly more Cu_6Sn_5 on both interfaces compared to the sample reflowed at 250°C. The phases were identified by energy dispersive X-ray spectroscopy (EDX). The recorded spectra are shown in Figure 13.

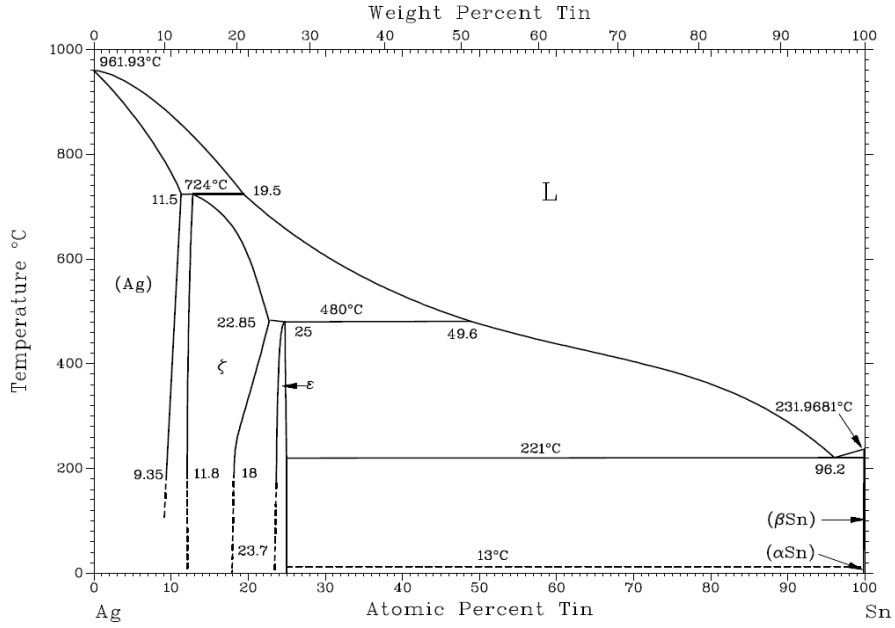

Figure 10: Binary phase diagram of silver and tin. [36] An addition of 3.5 wt.% silver to the tin is reducing the melting point of the alloy from 232°C to 221°C. (Reprinted with permission of ASM International. All rights reserved. www.asminternational.org)

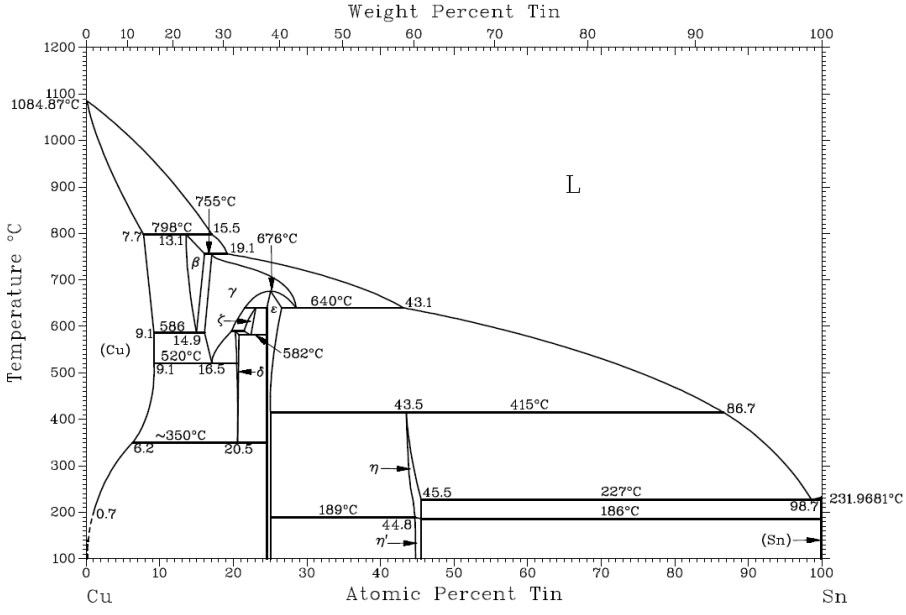

Figure 11: Binary phase diagram of copper and tin. [36] During the soldering reaction the η-phase (Cu_6Sn_5) is formed. (Reprinted with permission of ASM International. All rights reserved. www.asminternational.org)

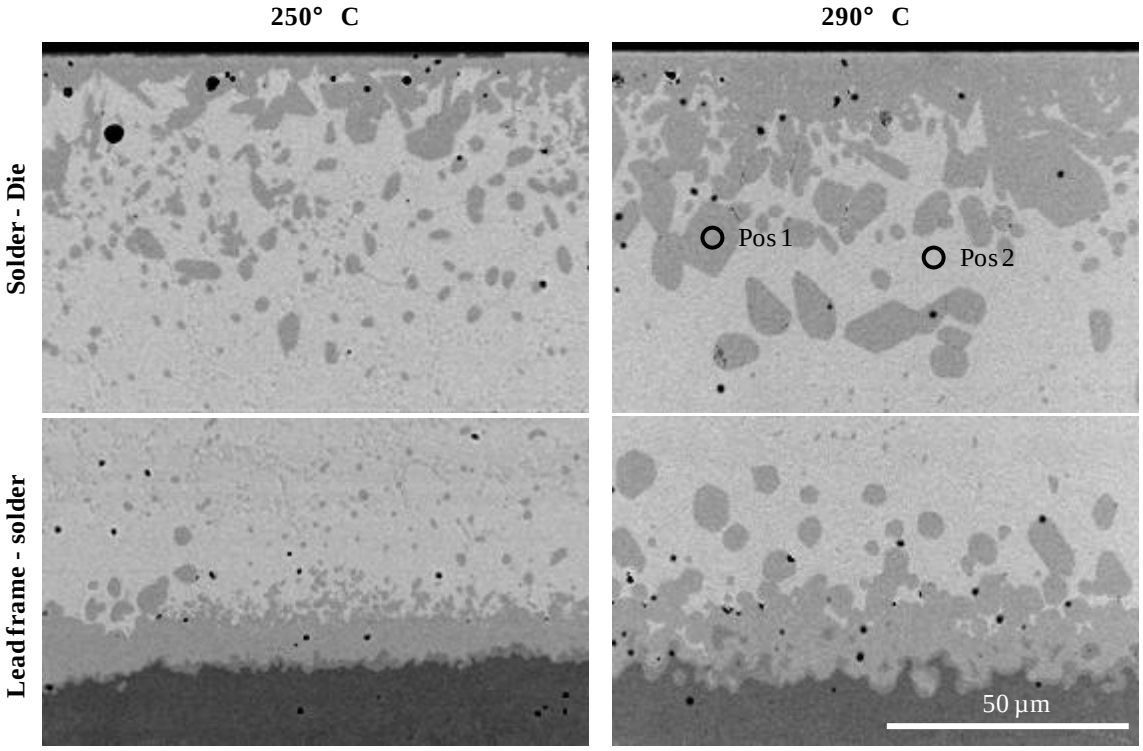

Figure 12: Scanning electron micrographs (SEM) of the solder-die (top) and the solder-lead frame interface. The solder was reflowed for 4 minutes at a peak temperature of 250°C (left) and 290°C (right). The positions where the EDX spectra shown in Figure 13 were recorded are marked.

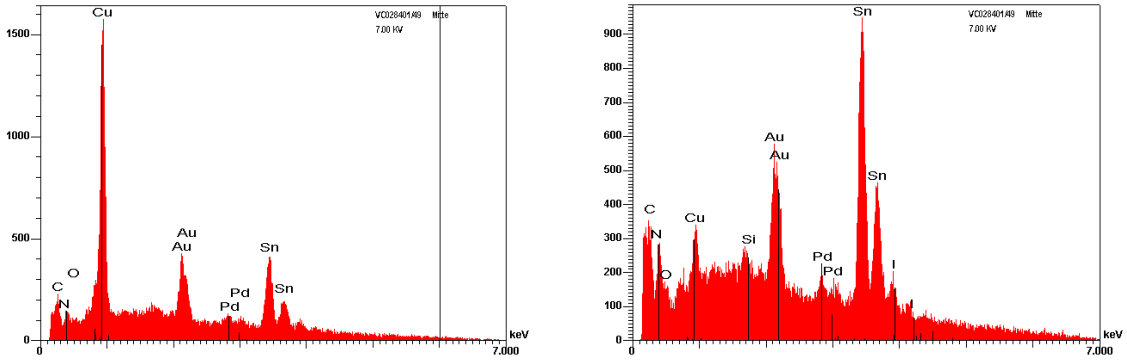

Figure 13: Energy dispersive X-ray spectra taken at positions marked in Figure 12. The left spectrum was taken at position 1. It clearly has a high copper content and can therefore be identified as the Cu_6Sn_5 phase. At position 2 only a small amount of copper is dissolved in the tin. The gold and palladium lines stem from the sample coating which was applied for SEM investigations.

A common failure mechanism in soft solder die attach is due to voids in the joint. A void is a gas or liquid filled volume in the die attach layer which drastically increases the thermal and electrical resistance between chip and package at that point. Voids can be built in directly during the die attach, be introduced later in the assembly or only occur during operation of the device. [37]

During the die attach, fluxes or other clean up agents form gases as reaction products which then get trapped in the joint. Also the fluxes themselves can be enclosed in the solder layer. In some cases there are areas on the joining surfaces where the solder does not wet because of the variable nature of the interfaces, e.g. dewetted areas may develop as portions of the metallization are leached away by the solder.

Built-in voids are difficult to control because of the many variables involved, but they can be detected effectively. Figure 14 shows an example of voids in the solder layer of chip detected by X-ray photography and Scanning Acoustic Microscopy (SAM).

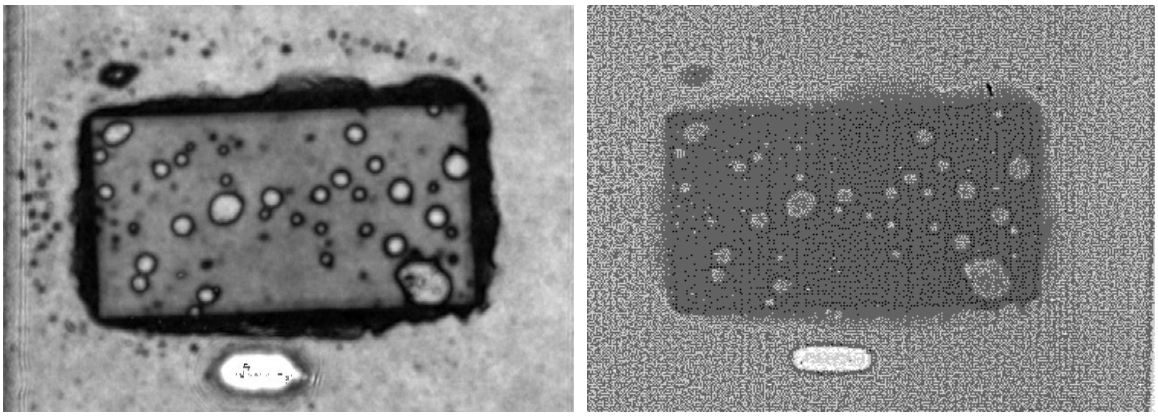

Figure 14: Voids in the die attach layer of a reflow soldered chip are detected X-ray photography (left) and by scanning acoustic microscopy (right).

In X-ray photography a void will stand out as brighter, non-absorbing area, especially if the solder contains heavy elements. SAM uses ultrasonic waves that are reflected at solid-gaseous interfaces. Thus voids appear bright in reflection mode and dark in transmission mode. The advantage of the SAM compared to the X-rays is that it is able to detect voids even if they are very thin such as cracks. Cracks are usually introduced after the die attach during cooling,

storage, or operation. They are caused by excessive mechanical stress between chip and package, or by metallurgical fatigue of the solder when the device is temperature or power cycled. Although a crack has almost only a two dimensional shape compared to other voids it still has an adverse effect on the thermal resistance.

A void in the die attach layer will result in a hot spot in the chip area directly above it during operation of the device. The heat generated by the power dissipated in the semiconductor above the void must flow laterally along the chip around the void, thus increasing the length of the thermal path. Even very thin voids usually dominate the thermal resistance completely. [37]

Generally voids can be divided into two groups: Hot voids and cold voids. For a cold void the power dissipation in the chip area above the void is also reduced. This is the case if the electrical resistance of the solder layer between the void and the chip is significant compared to the resistance of the semiconductor device, e.g. if the backside metallization of the chip has been leeched away by the solder.

For a hot void the metallization is sufficiently thick thus maintaining the same current density in the chip above the void as elsewhere. In this case the high thermal resistance of the void is not balanced by a reduced power dissipation which results in a hot spot and possibly in the failure of the whole device.

1.3.1.3 Diffusion soldering

Diffusion soldering or transient liquid phase joining (TLP), as it is sometimes also referred to, is an alternative joining method with several advantages compared to conventional soldering. [38] This technology uses a few micrometer thick layer of a filler metal that is deposited directly on the backside of the wafer. For die attach the die is pressed with its metalized backside on the preheated lead frame. The filler metal melts and fills the joint clearance. During the successive heating stage the filler and the metal of the lead frame diffuse into each other, forming intermetallic phases with higher melting points than the process temperature. This means that the joint is formed by isothermal solidification, having a remelt temperature much higher than the process temperature. Figure 15 illustrates the process. The dynamics of this process are investigated for several material systems in this thesis.

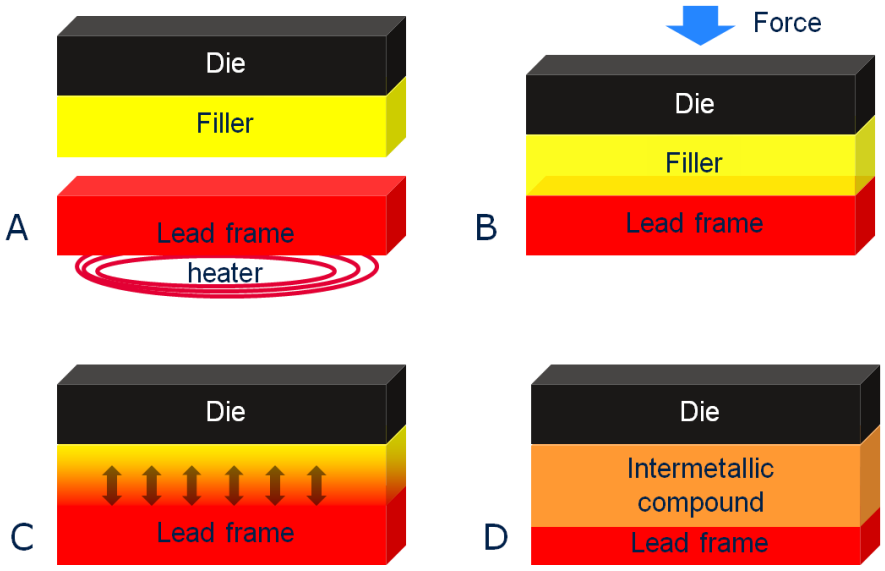

Figure 15: schematic of the diffusion soldering process. A: The backside of the die is coated with a thin layer of a low-melting-point metal. The lead frame consists of a high-meting-point metal and is heated to process temperature. B: The die is pressed on the lead frame and the filler melts upon contact. C: Filler and lead frame material diffuse into each other, forming intermetallic compounds which are solid at the process temperature. D: After the reaction is completed the joint has solidified isothermally and the layer entirely consists of high-melting-point intermetallic compounds.

The biggest advantage of this method is low processing temperature which is only limited by the melting temperature of the filler metal and the comparatively high service temperature with a difference of up to 600 °C depending on the material system. [39] This enables the formation of joints at mild process conditions, which protects the sensitive unpackaged die and minimizes the intrinsic stress; i.e. the stress that is arising during cooling after the die attach due to a difference in the coefficient of thermal expansion between the silicon of the die and the metal of the lead frame. During further processing or operation of the device the bond can withstand higher temperatures without weakening.

Another advantage lies in the precise control of the thickness of the filler material. This enables excellent joint filling of small and large area joints with high reproducibility. The obtained joints can be made very thin which is beneficial to the thermal and electrical conductivity. Furthermore edge spilling (squeeze out) is minimized because of the exact control over the amount of filler material applied. This is essential for thin wafer technologies, where the thickness of the silicon is

only a few tens of micrometers and a shorting of the chip from frontside to backside has to be avoided.

The resulting joints consist entirely of intermetallic compounds and are thus very hard and brittle. Stress arising between the lead frame and the chip is effectively transferred through the joint. For some applications this is desirable as silicon decreases its resistance under stress and the diffusion soldering die attach can have a positive effect on the electric parameters of the device. [40]

Several material systems for diffusion soldering, consisting of a low-melting-point filler material and a high-melting-point substrate material, have been studied. Some examples are Copper/Indium [41], Copper/Tin [42], Silver/Tin [43], Silver/Indium [43], Gold/Tin [44], Gold/Indium [45], and Platinum/Indium [46]. Many involve precious metals and their cost might be considered an impediment. However the metals are applied only in thin films and the quantities needed are very low. Furthermore they have the advantage of being resistant to corrosion and therefore easier to bond even in slightly oxidizing environment. The binary eutectic alloy of gold and tin as the filler metal has the advantage of the corrosion resistance of gold and the low melting point of the eutectic alloy of only 278 °C. Due to these advantageous properties, the eutectic gold/tin alloy is often used as a filler material for industrial diffusion soldering in combination with substrates like copper, silver or nickel and is discussed in detail in chapter 3.

Nevertheless a material system lower in cost, avoiding the use of precious metals, is desirable from an economic point of view. Thus a possible alternative is the copper/tin system, which is also discussed in chapter 2.

1.3.2 Chip front side connection

The chip front side connections provide the electrical path for signal and power distribution. In contrast to the backside of the chip, the front side is structured, having multiple pads for various input/output connections. Therefore the area available per contact is lower and the thermal resistance higher. The core requirements to the front side connection are low electrical resistance and high reliability, especially concerning electro migration. Figure 16 shows a power transistor with all electrical connections. Source and gate contact are made by wire bonding to the frontside

of the chip. The drain contact is formed on the backside by the die attach. The most commonly applied technologies for frontside connections for power devices are briefly discussed in the following.

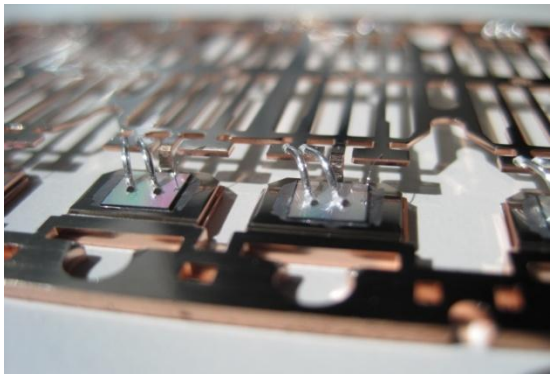

Figure 16: Single transistor chips on a lead frame with frontside connections made by wire bonding. Two thick wires connect the source pad to the corresponding lead and one thinner wire the gate pad. The drain contact is the backside of the die.

1.3.2.1 Wire bonding

In this technology a combination of heat, pressure and ultrasonic vibrations are used to connect the chip frontside to the lead frame by a thin metal wire. All wire bonding processes are similar in that they rub off the oxide layer on the wire and the substrate by applying pressure, heat and ultrasonic energy. The joining surfaces are brought in intimate contact, so that metal bonds can be formed and a stable joint is achieved. There are two basic wire bonding techniques: ball bonding and wedge bonding. Each of those can be applied in thermocompression, thermosonic or ultrasonic mode, depending on the energy supplied for the bonding process. [47]

For ball bonding the wire is passed through a thin capillary leaving a small portion of it extending beneath the capillary. An electric discharge is used to melt this part. The surface tension of the liquid metal forms the ball as it solidifies. The ball is then pressed onto the bond pad on the die with sufficient force to cause plastic deformation. Atomic interdiffusion of the wire and the underlying and the removal of surface contamination is enhanced by thermal and ultrasonic energy. This ensures an intimate contact between the two metal surfaces and forms the first bond (see Figure 17). Then the capillary is raised and moved over the second bond position,

the lead frame. The trajectory of the capillary tip gives the wire connection its shape. The second bond is formed by pressing the capillary against the lead frame and thereby breaking the wire. This so called stitch bond has a crescent shape caused by the imprint of the capillary. Then the tool is raised again leaving an exact wire length sticking out to form a new ball for the new bond. By the use of fully automated machines and precisely controlled process parameters it is possible to make more than ten wire connections per second. [48]

Wedge bonding is named after the shape of the bond tool. The wire is fed through a hole on the back of the wedge at a low angle. The main difference to ball bonding is that the wire is bonded on its side and not vertically on the bond pad (see Figure 18). This is a considerable advantage as it gives a smaller footprint than a ball bond and allows a denser placing of the wires. Still approximately 90 % of all semiconductor packages are manufactured using ball bonding, because of its unmatched speed. [48]

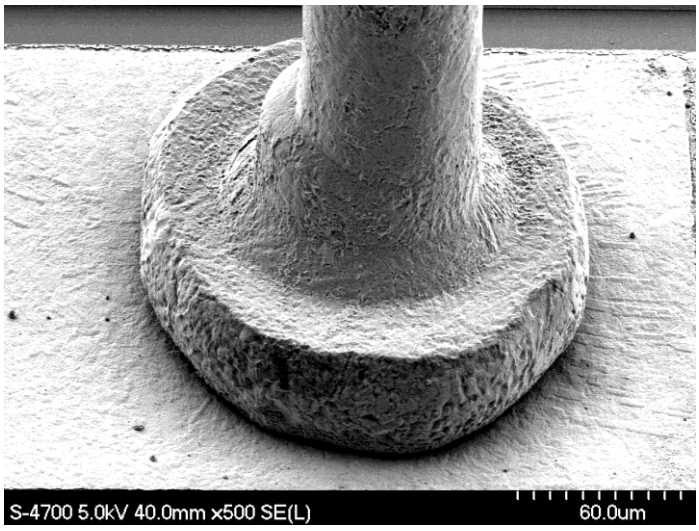

Figure 17: Ball bond of a 60 µm thick aluminum wire on an aluminum bond pad.

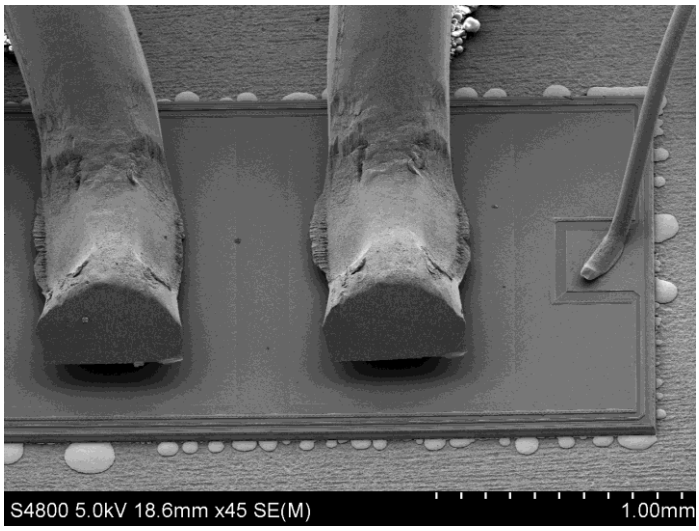

Figure 18: Wedge bonded aluminum wires as source (left and middle wire) and gate (right wire) connections on a power transistor.

1.3.2.2 Flip chip bonding

In flip chip bonding the chip is attached upside down. Solder or conductive polymer bumps between the chip contact pads and the substrate serve as a mechanical and electrical interconnection. This method requires the mirrored contact pad pattern of the chip frontside on the printed circuit board. The chip is placed upside down directly on the printed circuit board. In a reflow process the solder bumps are melted and establish the connection to the substrate. To prevent a spreading of the solder over the whole lead, the contact areas are surrounded by a non wetting material like glass or epoxy resin. Thus, in the case of a slight misalignment, the chip can be pulled in the correct position by the surface tension of the liquid solder.

The advantages of this relatively simple method are the relatively low footprint of the device on the circuit board as well as the low ohmic resistance and inductivity of the thin solder joints. A drawback though is small contact area of chip and substrate. The heat generated by the chip has to be dissipated completely over the connections of its frontside as the backside has no connection to a lead frame. To overcome this problem an additional heat sink can be attached to the chip backside. But this increases the footprint of the device and the major advantage of the flip chip method is lost. An example of such a technology is shown in Figure 19.

Figure 19: Examples of flip chip packages. CanPAK™ (left): A single transistor is equipped with a metal heat sink on the backside, which also acts as the drain contact. The two source contacts and the gate contact are covered with solder bumps on the frontside. Embedded Wafer Level Ball Grid Array (right): flip chip package of an integrated circuit. Solder balls are applied to all the contact pads on the frontside.

1.3.3 Encapsulation

To protect the chips from mechanical damage, humidity, corrosive gases and other external influences they are encapsulated in epoxy molding compounds (EMC). Various substances are added to the EMC so that it can meet the requirements on reliability, stability and moldability. Typically an EMC consists to 70 to 90 wt. % of silica filler (SiO_2) to achieve a coefficient of thermal expansion close to the silicon of the chip. [20] The epoxy resin makes up only 5 to 10 wt. %. Epoxy resins are used because they have high adhesion strength, small shrinkage during curing, good electrical properties and a superior resistance to chemicals, moisture and heat. Only 5 wt. % remain for other additives such as the hardener, the curing promoter, coupling agents and flame retardants. The amount and type of hardener mainly determines the melt viscosity of the EMC. A curing promoter is a catalyst which reduces the heat and time needed for curing of the EMC. Silane coupling agents ensure the adhesion between the epoxy resin and the filler particles. To fulfill the flammability rating, antimony based flame retardants such as antimony trioxide are added, but recently they have been replaced by halogen free substances due to environmental concerns.

In a typical transfer molding process, the lead frame with the chips is placed in a heated cavity (~180 °C) and the EMC is fed by a plunger under pressure into a single chamber for every die. After about two minutes when the EMC is sufficiently cured the cavity is opened and the molded lead frame is released. [20] To fully cure the EMC, the devices have to be annealed for up to 8

hours at elevated temperatures. In a so called deflash process, the redundant EMC at the edges of the devices is removed. Then the lead frames are plated with a thin layer of tin to improve the wettability during board assembly. The left part of Figure 20 shows a lead frame in this state. In the final process step before the electrical test the single devices are separated by punching. Up to this point the single leads have been connected for reasons of mechanical stability. Now the chip is ready for the assembly on a circuit board.

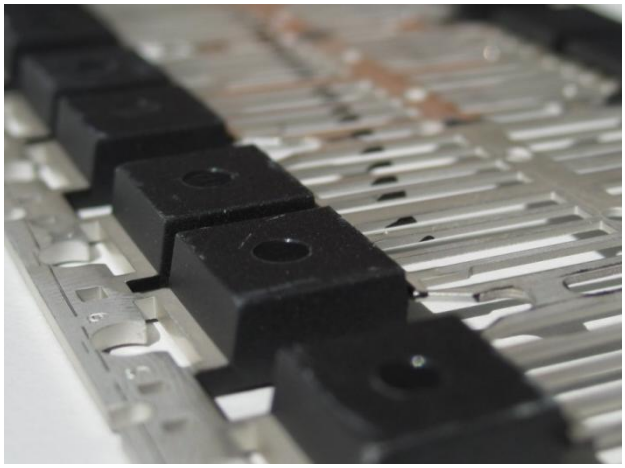

Figure 20: Lead frame after molding and tin plating.

1.4 References

[1] *J. G. Koomey, „EXECUTIVE SUMMARY“, 2007.*

[2] *W. C. O'Mara, R. B. Herring, und L. P. Hunt, Handbook of semiconductor silicon technology. William Andrew, 1990.*

[3] *U. Hilleringmann, Silizium-Halbleitertechnologie. Vieweg +Teubner, 2004.*

[4] *J. Czochralski, „Ein neues Verfahren zur Messung der Kristallisationsgeschwindigheit der Metalle“, Z. phys. Chemie., Bd. 92, S. 219–221, 1918.*

[5] *M. E. Levinshteĭn und M. Shur, Semiconductor technology: processing and novel fabrication techniques. Wiley, 1997.*

[6] *B. El-Kareh, Fundamentals of semiconductor processing technology. Springer, 1994.*

[7] *A. Hössinger, „Simulation of ion implantation for ULSI technology“, Tech. Univ. Vienna, Vienna, Austria, 2000.*

[8] *P. C. Andricacos, „Copper on-chip interconnections“, The Electrochemical Society Interface, S. 32–37, 1999.*

[9] P. V. Zant, *Microchip fabrication: a practical guide to semiconductor processing*. McGraw-Hill, 1997.

[10] C. Y. Chang und S. M. Sze, *ULSI technology*. McGraw-Hill, 1996.

[11] Y. D. Gamburg und G. Zangari, *Theory and Practice of Metal Electrodeposition*. Springer, 2011.

[12] S. Murarka und S. Hymes, „Copper metallization for ULSL and beyond“, *Critical Reviews in Solid State and Materials Sciences*, Bd. 20, Nr. 2, S. 87-124, 1995.

[13] *Praxiswissen Mikrosystemtechnik*. Wiesbaden: Vieweg+Teubner, 2006.

[14] C. S. Yoo, *Semiconductor manufacturing technology*. World Scientific, 2008.

[15] WILEY-VCH Verlag GmbH & Co KGaA, Hrsg., *digital Encyclopedia of Applied Physics*. Weinheim, Germany: WILEY-VCH Verlag GmbH & Co KGaA, 2003.

[16] J. A. Thornton, J. Tabock, und D. W. Hoffman, „Internal stresses in metallic films deposited by cylindrical magnetron sputtering“, *Thin Solid Films*, Bd. 64, Nr. 1, S. 111–119, 1979.

[17] H. F. Winters, „Gas Incorporation into Sputtered Films“, *Journal of Applied Physics*, Bd. 38, Nr. 10, S. 3928, 1967.

[18] S. D. Dahlgren, „Equilibrium phases in 304L stainless stell obtained by sputter-deposition“, *Metallurgical and Materials Transactions B*, Bd. 1, Nr. 11, S. 3095–3099, 1970.

[19] J. A. Thornton, „The microstructure of sputter-deposited coatings“, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, Bd. 4, Nr. 6, S. 3059–3065, 1986.

[20] D. Lu und C. P. Wong, *Materials for advanced packaging*. Springer Verlag, 2008.

[21] R. R. Tummala, *Fundamentals of microsystems packaging*. McGraw-Hill Professional, 2001.

[22] G. Bai, „Low-temperature sintering of nanoscale silver paste for semiconductor device interconnection“, Virginia Polytechnic Institute and State University, 2005.

[23] Z. Zhang, „Processing and Characterization of Micro-scale and Nanscale Silver Paste for Power Semiconductor Device Attachment“, Virginia Polytechnic Institute and State University, 2005.

[24] „Directive 2002/95/EC of the European Parliament and of the Council“. Official Journal of the European Union, 2003.

[25] „BE semiconductor industries“. [Online]. Available: http://www.besi.com/products-and-technology/die-attach/die-bonding/esec-2100-xp-3. [Accessed: 22-Juli-2011].

[26] Y. Li, C. P. Wong, und D. Lu, *Electrical Conductive Adhesives with Nanotechnologies*. Springer, 2009.

[27] D. D. Chang u. a., „An overview and evaluation of anisotropically conductive adhesive films for fine pitch electronic assembly“, *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on*, Bd. 16, Nr. 8, S. 828–835, 1993.

[28] H. Takezawa, M. Itagaki, T. Mitani, Y. Bessho, und K. Eda, „Development of solderless joining technologies using conductive adhesives“, in *Advanced Packaging Materials: Processes, Properties and Interfaces, 1999. Proceedings. International Symposium on*, S. 11–15.

[29] Y. Li und C. P. Wong, „Recent advances of conductive adhesives as a lead-free alternative in electronic packaging: Materials, processing, reliability and applications“, *Materials Science and Engineering: R: Reports*, Bd. 51, Nr. 1-3, S. 1-35, Jan. 2006.

[30] K. Suganuma, „Advances in lead-free electronics soldering“, *Current Opinion in Solid State and Materials Science*, Bd. 5, Nr. 1, S. 55–64, 2001.

[31] K.-H. Florenz, „Committee on the Environment, PublicHealth and Consumer Policy Draft Report“, *European Parliament*, Bd. 2001.

[32] C. o. t. E. Communities, „Proposal for a Directive of the European Parliament andthe Council on Waste Electrical and Electronic Equipment: Proposal for aDirective of the European Parliament and of the Council on the restriction of theuse of certain hazardous substances in electrical and electronic equipment“, *WEEE Directive Brussels*, Bd. 13, 2000.

[33] K. N. Chen, A. Fan, C. S. Tan, und R. Reif, „Bonding parameters of blanket copper wafer bonding“, *Journal of Electronic Materials*, Bd. 35, Nr. 2, S. 230-234, Feb. 2006.

[34] K. Zeng und K. N. Tu, „Six cases of reliability study of Pb-free solder joints in electronic packaging technology“, *Materials Science and Engineering: R: Reports*, Bd. 38, Nr. 2, S. 55–105, 2002.

[35] P. G. Harris und K. S. Chaggar, „The role of intermetallic compounds in lead-free soldering“, *Soldering & Surface Mount Technology*, Bd. 10, Nr. 3, S. 38-52, 1998.

[36] T. Massalski, „Binary alloy phase diagrams“. Materials Park: ASM International, 1996.

[37] A. Yerman, J. Burgess, R. Carlson, und C. Neugebauer, „Hot Spots Caused by Voids and Cracks in the Chip Mountdown Medium in Power Semiconductor Packaging“, *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Bd. 6, Nr. 4, S. 473-479, Dez. 1983.

[38] G. Humpston und D. M. Jacobson, *Principles of soldering*. Asm Intl, 2004.

[39] S. A. Sommadossi, „Investigation on Diffusion Soldering in Cu/In/Cu and Cu/In-48Sn/Cu Systems“, Universit\ätsbibliothek, 2002.

[40] P. W. Bridgman, „The effect of homogeneous mechanical stress on the electrical resistance of crystals“, *Physical Review*, Bd. 42, Nr. 6, S. 858, 1932.

[41] S. Sommadossi u. a., „Development of Cu/Cu interconnections using an indium interlayer“, *Metal Matrix Composites and Metallic Foams*, S. 214–218, 2000.

[42] F. Bartels, J. W. Morris, G. Dalke, und W. Gust, „Intermetallic phase formation in thin solid-liquid diffusion couples“, *Journal of electronic materials*, Bd. 23, Nr. 8, S. 787–790, 1994.

[43] G. Humpston und D. M. Jacobson, *Methods of joining components*. Google Patents, 1992.

[44] G. S. Matijasevic, C. Y. Wang, und C. C. Lee, „Void free bonding of large silicon dice using gold-tin alloys“, *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on*, Bd. 13, Nr. 4, S. 1128–1134, 1990.

[45] C. C. Lee, C. Y. Wang, und G. Matijasevic, „Au-In bonding below the eutectic temperature“, *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on*, Bd. 16, Nr. 3, S. 311–316, 1993.

[46] T. Studnitzky und R. Schmid-Fetzer, „Phase formation and diffusion soldering in Pt/In, Pd/In, and Zr/Sn thin-film systems“, *Journal of electronic materials*, Bd. 32, Nr. 2, S. 70–80, 2003.

[47] W. Menz, J. Mohr, J. Mohr, und O. Paul, *Microsystem technology*. Wiley-VCH, 2001.

[48] G. Harman, *Wire Bonding in Microelectronics*. McGraw Hill Professional, 2010.

2 Dynamics of diffusion soldering[1]

Diffusion soldering is a technology very commonly used in microelectronics packaging but still not well understood. Process parameters such as bond time, force and temperature are different for every chip type and are often defined only based on trial and error. This method has the disadvantage that a lot of effort has to be undertaken for the qualification of every new package, even if the material system is known from existing products. Slight variations in the processing conditions, which cannot be avoided in high volume production at multiple sites across the globe, can lead to a complete failure of the joint if the parameters are not chosen within a safe margin. Furthermore it is very difficult to predict the long term reliability of the package. Therefore a deeper understanding of the dynamics of diffusion soldering is desirable. This would at least reduce the amount of necessary trials and enable the design of a process that produces joints with the necessary quality.

Several studies have already been done on various combinations of filler and substrate materials. The evolution of the intermetallic phases involved in the soldering process has been studied so far mainly ex-situ by analysis of joint cross-sections or fractured joint surfaces [1–9]. The analysis of quenched samples can reveal the composition across the thickness of the joint and the phase structure at the fractured surfaces after certain reaction times. However, it is not possible by these methods to observe the course of the reaction at the elevated process temperatures directly. Therefore it is difficult to track the structural phase evolution, as some phases formed during the process might not be stable at room temperature. By microscopy, only a 2-dimensional area can be investigated which might not be representative for the whole volume of the sample. *In situ* X-ray diffraction (XRD) is an integral method enabling the direct investigation of the intermetallic phase evolution in a macroscopic volume at elevated temperatures. Gollas at al. [10] have

[1] *This chapter is based on material already published in previous journal articles. [11–14]*

reported *in situ* XRD studies of Ag/Sn and Ag/In samples, emphasizing the identification of the intermetallic phases involved in the reaction.

Some of the material presented in this chapter appeared in articles already published. [11–14] The experiment was conducted at the institute of solid state physics at the Graz University of Technology in cooperation with Jiri Novak who provided the tool setup and the necessary XRD expertise.

A full characterization of the dynamics of the phase evolution in four different thin film systems is presented. The first three are based on the eutectic gold tin alloy in combination with the most common lead frame platings: copper, silver and nickel. The forth is relies on pure tin as the filler on copper lead frames, eliminating the expensive gold. This is a prototype soldering system, not used for production and still under evaluation.

The soldering process is was investigated with the combination of *in situ* XRD, Focused Ion Beam microscopy (FIB), Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM) and Energy Dispersive X-ray spectroscopy (EDX). Fundamental parameters of the reactions like the rate of the intermetallic layer growth and the activation energy were extracted and thus enable an extrapolation of the observed dynamics to a wide range of temperatures. These results enable the calculation of the time necessary to form a stable diffusion soldered joint with high accuracy. It is necessary supply enough thermal budget to transform all of the filler material into an intermetallic compound of a high melting point in order to achieve a joint with the desired qualities. If there is still unreacted filler material left after the soldering process, it can remelt in subsequent process steps like the board assembly and the chip can get loose. Furthermore the reaction can proceed in the solid state during the operation of the device. This can lead to Kirkendall voids, which are caused by the density difference between the consumed and produced phases. [15] On the other hand, it is desirable to make the process as short and as cold as possible to save costs and to minimize the damage to the sensitive microelectronic chip.

2.1 Experimental

Films of the eutectic Au-20 wt.% Sn alloy, silver, copper and tin were sputtered on 200 mm silicon wafers in an Oerlikon Clusterline 200 magnetron sputtering tool with a target-substrate spacing of 4 cm. First a 100 nm titanium layer was sputtered to ensure that the surface of the wafer had a constant electrostatic potential. The layers were deposited at a constant rate and the sputtering power was chosen accordingly. The substrate was kept at a floating potential, while the voltage of the target was varied between -300 V and -500 V to keep the power constant.

Copper and tin films were electrodeposited on silver coated silicon wafers from industrial electrolytes in a NEXX Stratus 200 plating line at room temperature. Copper was deposited at a current density of 3 A/dm² which corresponds to a deposition rate of 0.66 µm/min. Tin was deposited at a current density of 2 A/dm² and a rate of 1 µm/min. Other deposition parameters were fixed at values, which have been determined through previous trials to yield stable and reproducible films of high quality.

The diffusion soldering was done on a Tresky T-3202 semiautomatic die bonder. Square silicon pieces with an edge length of 2.5 mm were pressed with the solder side against a metal lead frame with a pressure of 1.5 MPa under a forming gas atmosphere (95 at.% nitrogen, 5 at.% hydrogen). The pressure was applied for 500 ms and after a dwelling time the sample was cooled by pressurized nitrogen to a temperature below 320 K within 60 seconds.

Images of layer stack cross sections were taken in a FEI Vectra 200 focused ion beam (FIB) microscope. For cross-sectional imaging, the silicon wafer substrate was broken along a preferred orientation to produce a smooth edge. Thereafter the surface was polished with a gallium ion beam at an acceleration voltage of 30 kV and a beam current of 20 nA. This way the image could be taken perpendicular to the surface without distortions for an accurate thickness measurement. The acceleration voltage of the gallium ion beam used for imaging was also 30 kV with a beam current of 9 pA.

Lamellas for scanning transmission electron microscopy (STEM) analysis were cut from the previously prepared mechanical cross-sections with a thickness of 50 to 70 nm. STEM micrographs were taken with a FEI Tecnai F20 at an acceleration voltage of 200 kV. The TEM is

equipped with an EDAX Phoenix Si(Li) detector and analyzer for semi-quantitative energy dispersive X-ray spectroscopy (EDX) analysis and line scans.

The identification of the metallic phases was done in a Siemens D501 powder diffractometer in coupled Bragg-Brentano reflection mode with Cu Kα radiation. The X-ray beam passed through a graphite monochromator on the secondary side. As a detector, a scintillation counter with an entrance angle of 0.6° was used. The specimens were mounted symmetrically to the incident and to the diffracted beam. This method detects only (hkl) reflections of crystal planes parallel to the surface. The qualitative phase analysis was performed, using data from the Powder Diffraction File (International Center for Diffraction Data) and the Inorganic Crystal Structure Database (Fachinformationszentrum Karlsruhe).

The fiber texture of the intermetallic phases involved was examined by XRD pole figure analysis. The data was obtained using a Philips X'Pert System with Cr Kα radiation and a graphite monochromator on the secondary side. The diffractometer was equipped with an Eulerian cradle (four-circle goniometer) to allow tilting and rotating the specimen as required for texture measurements. The defocusing of the pole figures was corrected via powder normals.

For the in-situ XRD measurements, a Bruker D8 Discovery diffractometer with Cu Kα radiation was used. The primary beam was collimated and monochromatized by a parabolic graded multilayer mirror (Göbel mirror) and a slit. The primary beam size was 0.1 mm with a divergence of 0.04 degrees. Diffraction patterns were recorded by a linear position sensitive detector VANTEC-1, enabling the capture of an angular range of $2\Theta \approx 12°$ in one frame. The detector's angular resolution was approximately 0.04 degrees. The sample heating was performed in an Anton Paar DHS 1100 heating chamber covered with a hemispherical PEEK dome filled with a He or Ar protective atmosphere. The samples were annealed isothermally at various temperatures following a rapid ramp up. For slower processes at lower temperatures, a full 2Θ scan was recorded every 2 to 5 minutes. At higher temperatures, the angular range was reduced to only twelve degrees, so that the linear detector would not have to be moved and the time resolution could be improved to 15 seconds.

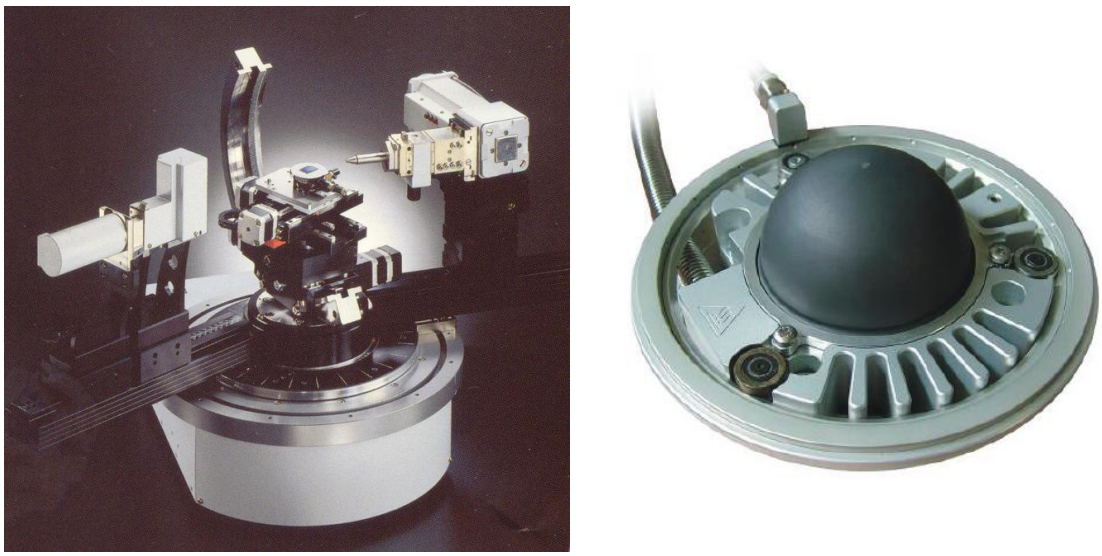

Figure 21. left: A Bruker D8 diffractometer with a linear position sensitive detector VANTEC-1 was used for in-situ XRD measurements. Right: The sample heating was performed in an Anton Paar DHS 1100 heating chamber covered with a hemispherical PEEK dome filled with a He or Ar protective atmosphere.

The individual peak intensities were obtained by integrating the intensity of every peak over a full width at half maximum (FWHM) range. All the peak intensities corresponding to a phase were summed up and normalized, i.e. the intensities of the products were divided by the maximum value reached in the final stable state after the anneal and the intensities of the educts were normalized relative to their initial value. Qualitatively all the peaks of one phase showed identical dynamics, i.e. they increased or decreased by the same rate as their sum. Thus a texture effect is very unlikely. Because the grains of the phase formed are small, the X-rays scattered in individual grains interfere incoherently and the intensity is directly proportional to the volume of the intermetallic compound. Therefore the normalized XRD peak intensities can be translated to a layer thickness by simply multiplying them by the maximum layer thickness, which was determined from the FIB images. To obtain a growth rate the layer thickness is divided by the reaction completion time determined by extrapolating linear progress of XRD peak intensities to their maximal values.

2.2 Gold/tin on copper

Copper is the most common lead frame material due to its high electrical and thermal conductivity as well as its mechanical properties. One of the drawbacks of copper as a lead frame surface is that it readily oxidizes and a good protective atmosphere is required throughout the die attach process. Bare copper lead frames are used for example in Transistor-Outline (TO) packages.

The eutectic Au/Sn alloy was sputtered on a silicon substrate with a thickness of 1.2 µm. According to the Au-Sn phase diagram, three intermetallic phases are stable at room temperature: The hexagonal ζ'-phase (Au_5Sn), the hexagonal δ-phase (AuSn), and the orthorhombic ε-phase ($AuSn_2$) (see Figure 22).

Qualitative XRD analysis shows that the gold tin layer consists predominantly of the ζ' and the δ-phase. No single metal phases and only insignificant traces of the ε-phase have been found (see Figure 23). This is also in good agreement with the theory for the solidification of a eutectic melt. Given these basic conditions, the ratio of ζ' to δ-phase can be determined according to the phase diagram to be 60:40. The δ-phase forms a lamellar structure in a ζ'-matrix as it can be seen in the top part of Figure 24.

To simulate the lead frame, a 1 µm thick layer of copper was electroplated on top of the Au/Sn filler. This is necessary because an actual lead frame is more than 300 µm thick and impenetrable for the X-rays. By depositing the copper directly on the clean Au/Sn surface it can be assured that no surface contaminations are inhibiting the reaction and there is perfect conformity of the surfaces without any pressure being applied. XRD polar scans show that neither the Au-Sn phases nor the copper have a preferred crystal orientation. The cold, electrochemical deposition of the copper leads to a smooth interface towards the Au-Sn, with no intermixing initially.

After annealing at 573 K for 10 minutes, half of the copper has dissolved in the Au-Sn layer forming an intermetallic compound layer with a thickness of 2 µm. (see lower part of Figure 24). In the annealed sample only one ternary phase was identified by qualitative XRD analysis. This τ_1-phase ($Au_2Cu_6Sn_2$) has a primitive cubic unit cell and the crystal structure is of the β-manganese type [16].

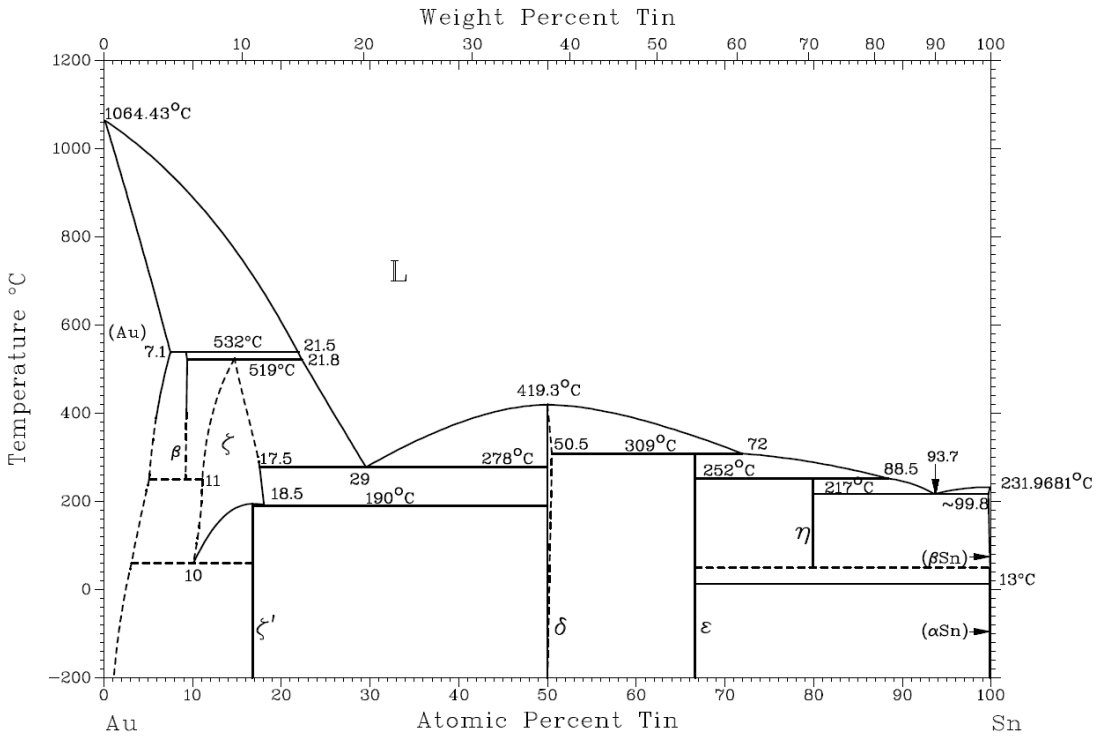

Figure 22: Binary phase diagram of Au/Sn. The hexagonal ζ'-phase (Au_5Sn), the hexagonal δ-phase (AuSn), and the orthorhombic ε-phase ($AuSn_2$) are stable at room temperature. (Reprinted with permission of ASM International. All rights reserved. www.asminternational.org)

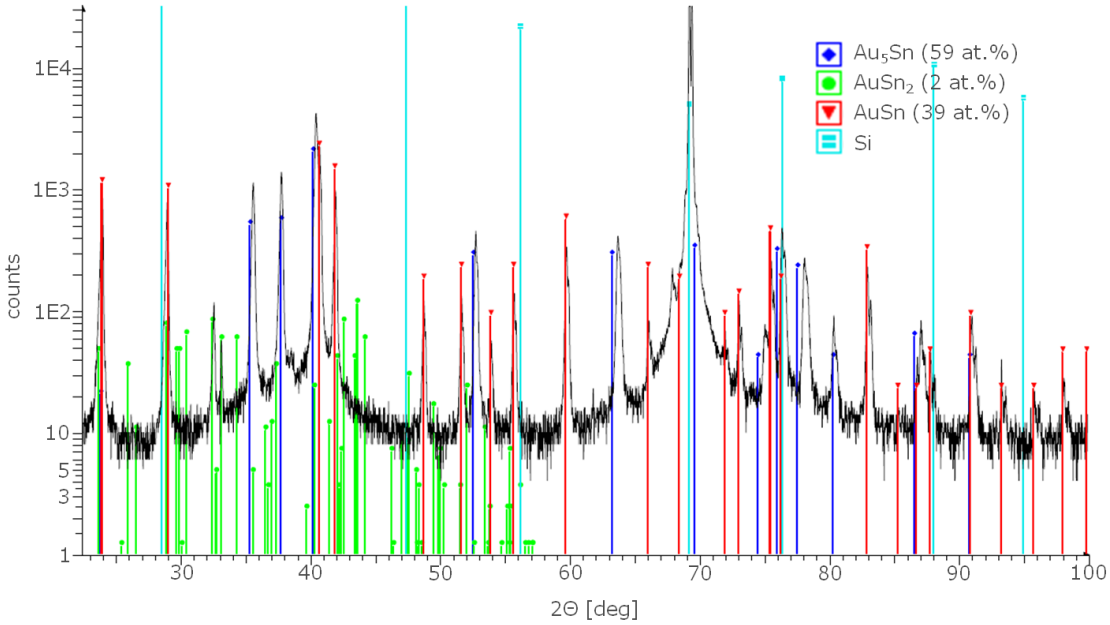

Figure 23: Specular XRD scan of the sputtered Au/Sn film on a silicon substrate. All three phases that are stable at room temperature are found, but the amount of $AuSn_2$ phase is only very small.

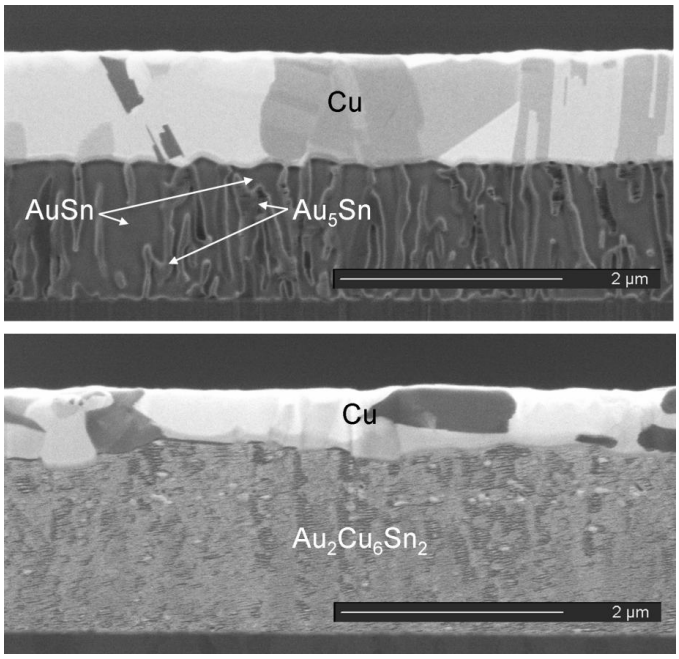

Figure 24: FIB micrograph. top: 1 µm of Cu was electrochemically deposited on a 1.2µm layer of sputtered Au/Sn eutectic alloy. δ and ζ'-phase form a lamellar structure in the Au/Sn layer. bottom: after annealing at 573 K for 10 minutes the Au/Sn has reacted with the copper forming the ternary $Au_2Cu_6Sn_2$ compound.

The dynamics of this reaction were followed by *in-situ* XRD. The samples were isothermally annealed in the diffractometer at temperatures of 483 K, 513 K, 543 K and 573 K. Figure 25 shows a representative example of the evolution of the XRD spectrum at 513 K.

The plots of the evolution of the intermetallic phases at all investigated temperatures were obtained by integration of the peak intensities as described in the experimental section. The plots at the different temperatures are qualitatively very similar, only differing in the time scale. The integral intensities for copper and the Au-Sn phases decrease linearly with time whereas the intensity for the ternary phase increases until all the Au-Sn has been consumed and the reaction is completed. During the reaction not all of the copper is used and the intensity saturates at about 20% of the initial value. Based on these facts we can propose the following reaction equations:

$$2\,AuSn + 6\,Cu \rightarrow Au_2Cu_6Sn_2$$
$$2\,Au_5Sn + 6\,Cu \rightarrow Au_2Cu_6Sn_2 + 8\,Au$$

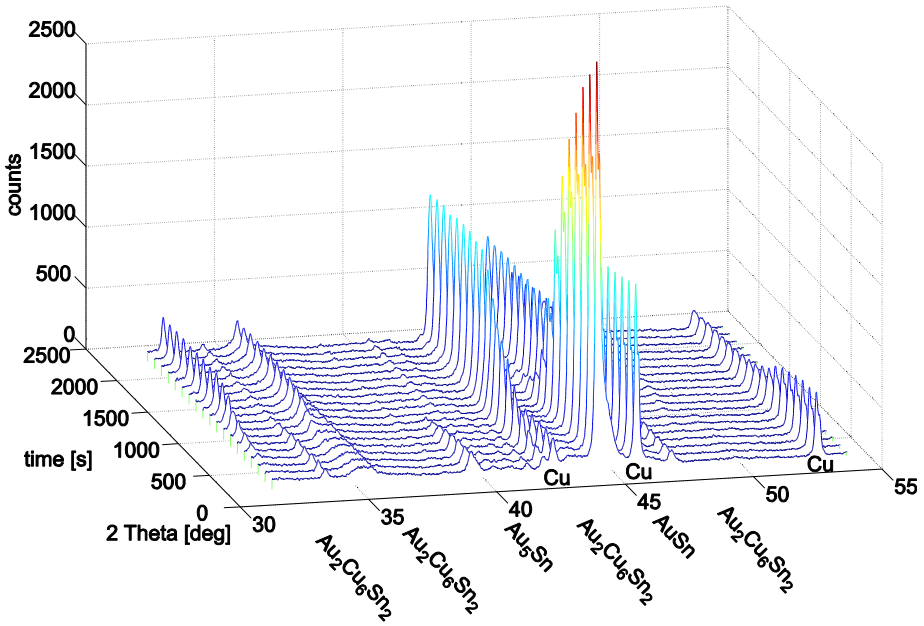

Figure 25: Detail of the XRD spectra taken during the isothermal anneal at 513 K of the Au-Sn/Cu thin film sample. Spectra were recorded in 5 min time intervals. The peaks of evolving intensity are marked with the phase they have been assigned to. The constant minor peaks at 33°, 35.3°, 37.6° and 40° stem from the silicon oxide substrate.

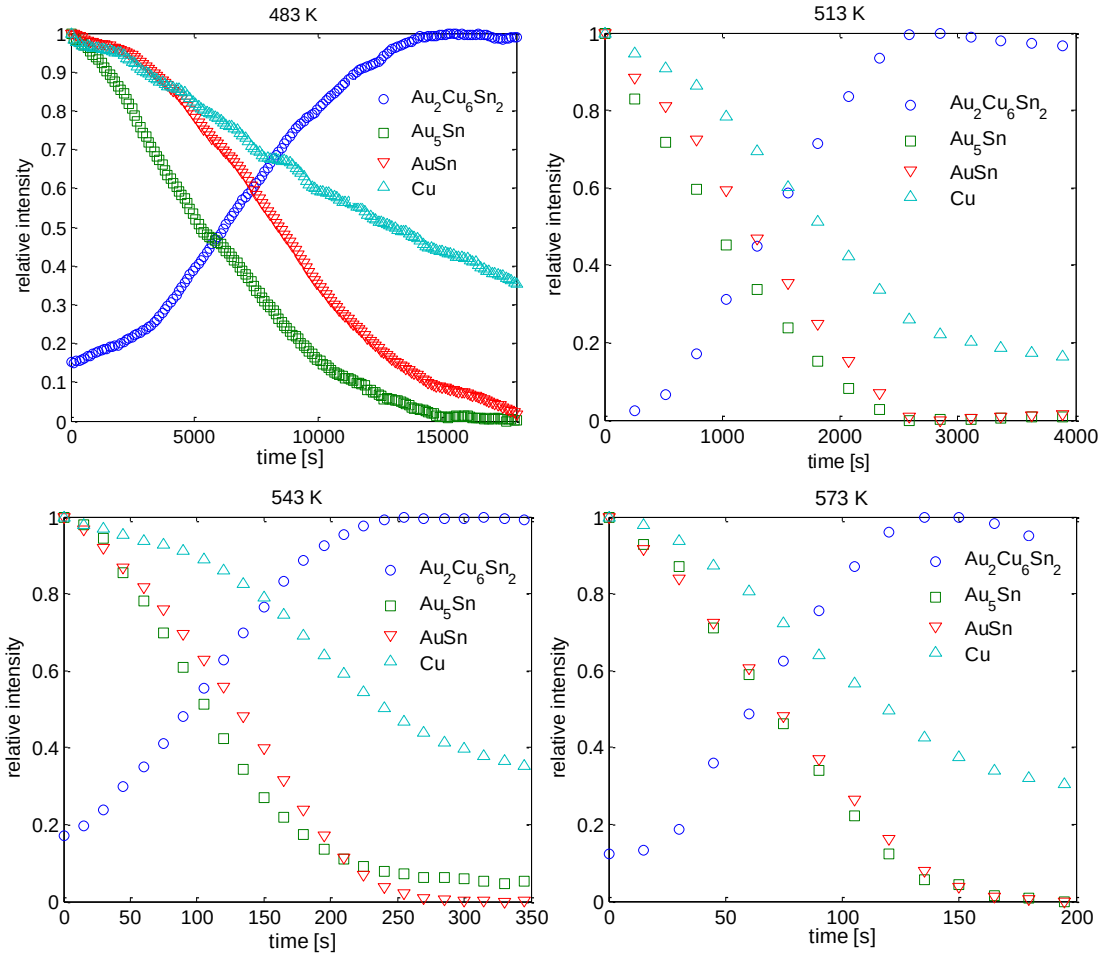

Figure 26: in-situ XRD. Evolution of the intermetallic phases in a Au/Sn – Cu thin film sample during an isothermal anneal at 483 K, 513 K, 543 K and 573 K. The initially present phases are transformed at a constant rate into the ternary $Au_2Cu_6Sn_2$ compound

The elemental gold which is a product of the reaction was not found by XRD. Therefore it cannot be present as a pure crystal, but rather as a solid solution with the remaining copper, which can dissolve a sufficient amount at room temperature [17]. For the other temperatures an equivalent reaction was found, with the reaction rate increasing with temperature.

Generally it is assumed that the thickness of an intermetallic compound layer increases proportional to the square root of time, as it is the case for a diffusion controlled process [5,7,9,18]. The *in-situ* XRD analysis reveals though, that the formation of binary or ternary compounds in the thin layer of an IDS joint progresses linearly with time. This is to be expected if the interfacial reaction barriers control the kinetics. Gösele et al. [19] gave a general treatment for the

influence of an interfacial reaction barrier on the growth kinetics of a compound phase. The atomic flux j crossing the interface between two intermetallic compounds is:

$$j = \kappa^{eff} \Delta C^{eq}$$

where κ^{eff} is the effective interfacial barrier conductivity and ΔC^{eq} is the time independent equilibrium value of the concentration difference between the two interfaces. For layers thinner than a critical thickness D/κ^{eff}, where D is the interdiffusion coefficient, the growth rate can be estimated to be constant in time

$$dx \;\; dt \approx V \Delta C^{eq} \kappa^{eff}$$

Here V is the volume of intermetallic compound formed per atom that crosses the reaction barrier. Furthermore we assume a classical Arrhenius equation for the temperature dependence of the interfacial barrier conductivity:

$$\kappa^{eff} = \kappa^{0} \cdot e^{-E_A \;\; k_B T}$$

with κ^{0} as a constant pre-exponential factor, E_A as the activation energy, k_B as the Boltzmann constant and T as the temperature. By combining the previous two equations we can describe the growth kinetics of the intermetallic layer by

$$dx \;\; dt \approx V \Delta C^{eq} \kappa^{0} \cdot e^{-E_A \;\; k_B T}$$

The evolution of the intermetallic phases follows this function until the educts become scarce. Then it deviates from linearity passing into an exponential curve and finally saturating at a constant value. Therefore we can extract the rate of the intermetallic growth at constant temperature from the XRD data by a linear fit to the evolution of the normalized diffraction peak intensity of the intermetallic phase formed and multiplying it with the final layer thickness as described in the experimental section.

The data is plotted for all four investigated temperatures in an Arrhenius plot ($ln\ (dx/dt)$ vs. $1/T$) in Figure 27. The data points lie on a straight line, with the activation energy E_A given by its slope. This yields an activation energy of 1.2 eV for the reaction. The product of the constants V, ΔC^{eq} and κ^0 was determined to be 970 m/s. For reasons of simplicity it will be referred to as pre-exponential constant a_0 in the following. Interestingly, the Arrhenius relations hold for temperatures above the eutectic point of the Au-Sn alloy as well as below.

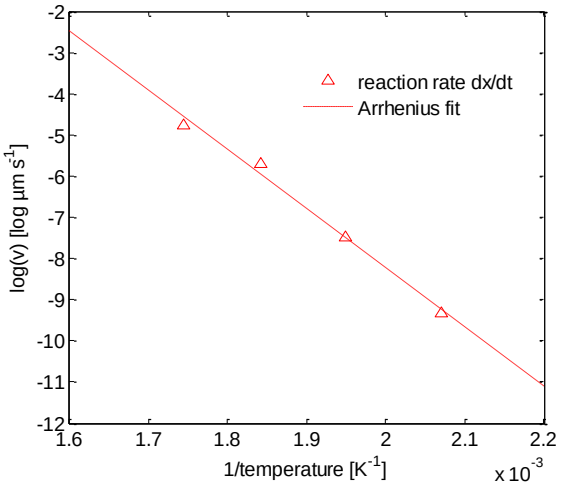

Figure 27: Arrhenius plot of the logarithm of the $Au_2Cu_6Sn_2$ growth speed versus the inverse temperature. The slope of the fit is proportional to the activation energy.

These parameters enable the calculation of the time necessary to transform a certain layer thickness of the Au/Sn alloy into the ternary compound at a given temperature and vice versa. For a temperature profile *T(t)* the thickness of the growing intermetallic layer x after a time t_x is given by

$$x = \int_0^{t_x} V\Delta C^{eq}\kappa^0 \cdot e^{-E_A\ k_B T(t)}\,dt$$

In practice the temperature profile *T(t)* is never just constant, because the lead frame has to be cooled with a limited rate after the attach. The cooling curve of the Tresky T-3202 die bonder used in this work can be best described by the right half of a Gaussian bell curve. By numerical integration the necessary time at the peak temperature to obtain a certain thickness of the

ternary compound was calculated. For example, it takes 100 s to transform half of the 1200 nm thick Au/Sn layer at 553 K or 40 s at 573 K. These parameter values have been used to bond actual chips for supporting the validity of the in-situ XRD measurements.

Figure 28 shows a cross-section of a joint solder with the former set of parameters. Only about half of the volume of the filler material has been transformed into the ternary phase as it is predicted by the in-situ XRD results. The unreacted regions of the eutectic Au/Sn alloy would be melted if it is heated to its melting point in subsequent process steps or during the operation of the device. The interfaces between the different intermetallic phases were made visible by ion polishing. EDX was used to attribute the differently shaded areas to the intermetallic phases. The resolution of the method is not good enough to measure the actual composition of the sample at an arbitrary position but it is good enough to detect rough differences. The interaction volume of the electron beam with the sample was estimated to have a diameter of approximately 500 nm. Thus the EDX spectrum sums the intensities stemming from a relatively large volume. For an identification of the phases one has to rely on XRD, but EDX can be used to localize them. Figure 29 shows a joint soldered with the second set of parameters. It has a similar morphology, also supporting the XRD results.

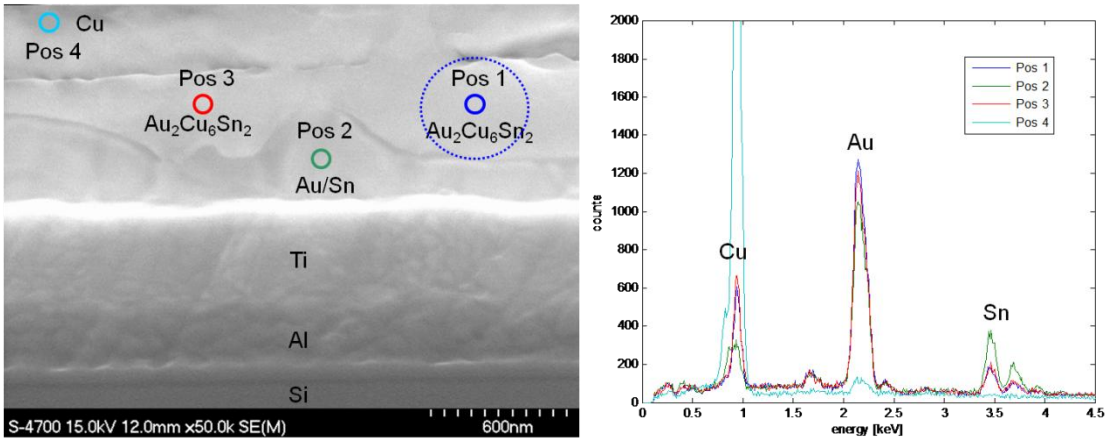

Figure 28: left: SEM of a cross-section of a joint soldered at 553 K for 100 s. right: EDX spectra recorded at the positions indicated in the SEM. Only half of the filler material has reacted with the substrate as it is predicted by the in-situ XRD results. The actual interaction volume of the electron beam is indicated by the dotted circle at position 1.

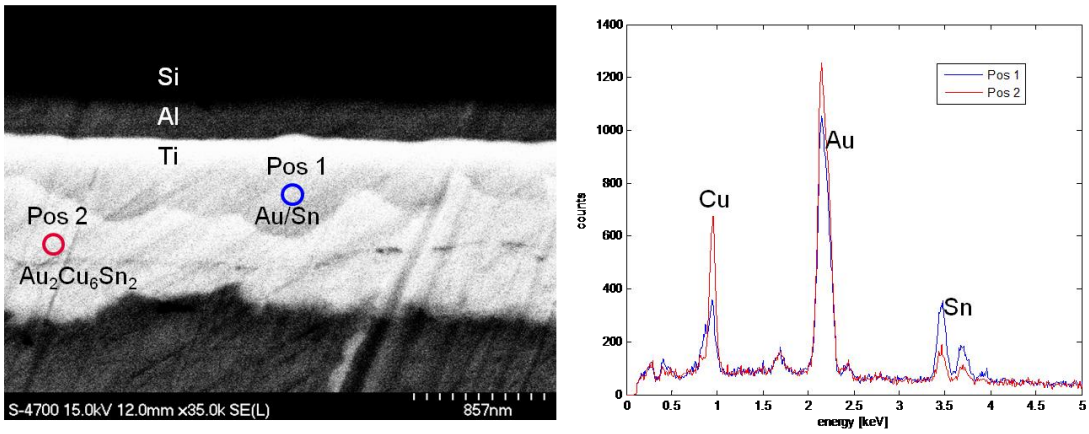

Figure 29 left: SEM of a cross-section of a joint soldered at 573 K for 40 s. right: EDX spectra recorded at the positions indicated in the SEM. The joint has a similar morphology as the one shown in Figure 28 as it is predicted by the in-situ XRD results.

The STEM image in Figure 30 shows the actual morphology of an incompletely reacted IDS solder joint which has been soldered in an industrial environment for high volume production. Dendrites of the ternary $Au_2Cu_6Sn_2$ phase extend from the copper substrate into the Au-Sn solder layer which is liquid during the soldering process. This was also confirmed by a semi-quantitative EDX line scan across the joint. In the areas where the electron beam is scanned over the dendrites, all three elements are detected with a signal intensity ratio that fits with the $Au_2Cu_6Sn_2$ phase measured by XRD. At the areas in-between no copper is found, but the signal intensity of gold and tin is increased. This corresponds to the eutectic Au-Sn alloy, a mixture of the ζ' and δ-phase. The single grains of these two phases can be distinguished in the close up of this area in the upper right corner of Figure 30. The grains of the δ-phase appear darker due to the higher content of the heavier gold. In contrast to the samples used for the XRD analysis, the reacting metals were not deposited in-situ on top of each other, but rather were brought into contact after deposition as described in the experimental section. Thus the system is more prone to contamination. The line visible at the original surface of the lead frame is a frequently occurring defect in soldering. The void is only a few nanometers thick but still acts as a diffusion barrier for the interaction between the Au-Sn-eutectic alloy with Cu and the reaction is slowed down. This is indicated by the fact that the areas of the single phases are not continuous across this defect. It is caused by an organic contamination of the copper lead frame as was confirmed by EDX (see Figure 31). A spectrum was recorded from an area along the seam line and another

one across it. By comparison of the two it was found that the voids contain carbon, nitrogen and oxygen. This points to an organic contamination of either the lead frame surface or the chip backside that is responsible for this diffusion barrier. The contamination could stem from the anti-tarnish coating of the lead frame or a leftover of the dicing foil on the chip.

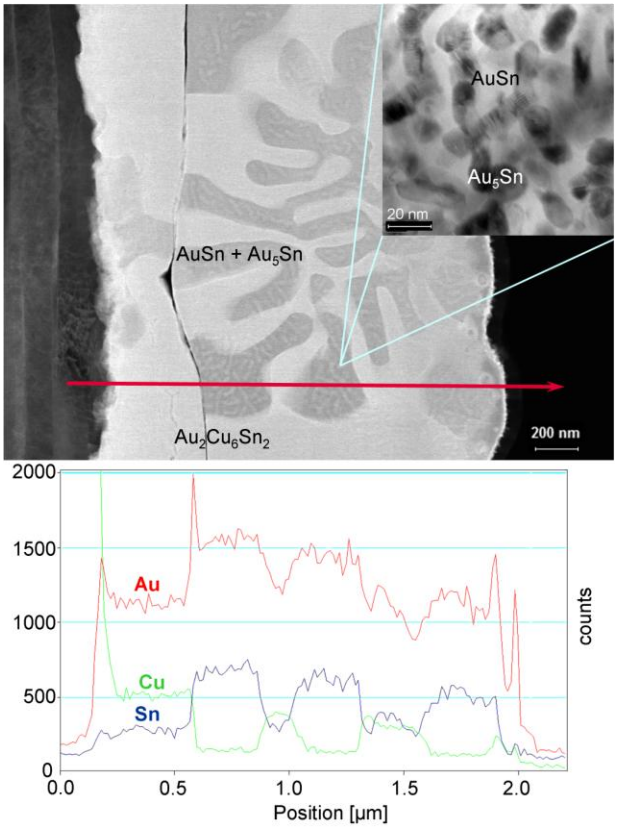

Figure 30: STEM and EDX. top: micrograph of an incompletely reacted IDS joint. The ternary $Au_2Cu_6Sn_2$ compound grows in a dentritic morphology from the copper on the left through the Au/Sn solder layer. The remaining unreacted solder is of the eutectic composition composed of the δ and the ζ'-phases. A close-up of the structure is shown on the top right. The ζ' grains appear darker due to the higher gold content. The crack at the original surface of the substrate is due to a contamination on the lead frame surface that acts as a diffusion barrier. The trace of the EDX line scan across the joint is marked by the red line. bottom: The EDX line scan qualitatively confirms the model of the morphology.

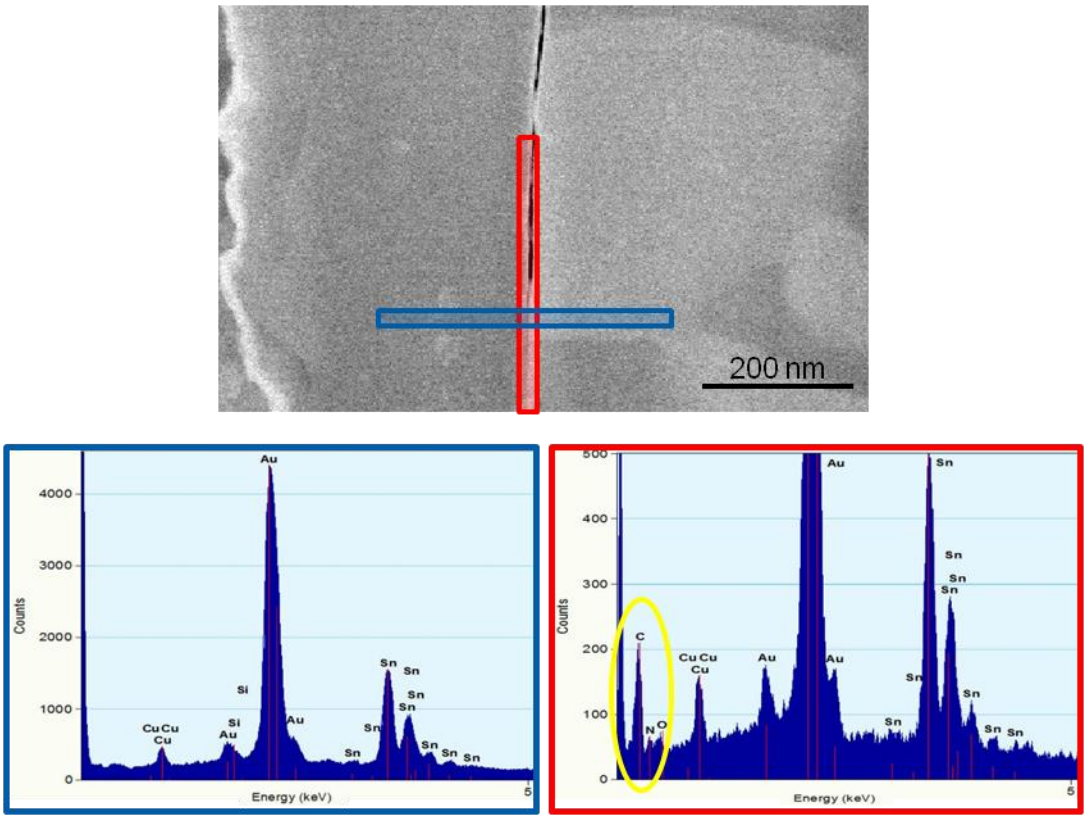

Figure 31: Identification of the seam line at the solder – lead frame interface. EDX spectra were recorded perpendicular to the interface (left, blue) and along it (right, red). Carbon, nitrogen and oxygen are found in the void, indicating an organic contamination.

2.3 Gold/tin on silver

Silver is commonly used to plate bare copper lead frames protecting the surface from oxidation. This causes higher costs of the lead frame, but can also stabilize the production process and improve the reliability. The silver layer is commonly applied by electrochemical deposition with a thickness of several micrometers directly on copper. E.g. the silver plating is used for Small-Outline-Transistor (SOT) packages.

The experiment for Au-Sn/Ag system was conducted in the same fashion as the experiment for the Au-Sn/Cu system so that the results can be compared directly. The sputtered layer stack for the silver system is shown as deposited in the top part of Figure 32. Due to the heating of the sample during deposition, the metals have already partially reacted. A layer of intermixing is

observed between the underlying Au-Sn and the silver on top before annealing. After annealing for 10 minutes at 573 K, most of the silver has reacted with the Au-Sn solder layer (see lower part of Figure 32).

In the qualitative XRD analysis of the initial sample, the ζ' and δ Au-Sn phases were found, as well as fcc silver and the orthorhombic Ag-Sn ε-phase (Ag_3Sn) [17]. During the anneal the silver and the Au-Sn δ-phase disappear, while the abundance of the other phases increases (see Figure 33). This indicates a reaction described by the following equation:

$$5\,AuSn + 12\,Ag \rightarrow 4\,Ag_3Sn + Au_5Sn$$

The tin-rich AuSn phase reacts with the silver to form a silver-tin binary compound and the gold-rich phase. The Au_5Sn phase which is present initially does not take part in the reaction. This was also confirmed in the *in-situ* XRD analysis which was conducted for the same temperature set as for the Au-Sn - copper system (483 K, 513 K, 543 K, 573 K). The evolution of the intermetallic phases during the isothermal annealing is plotted in Figure 34.

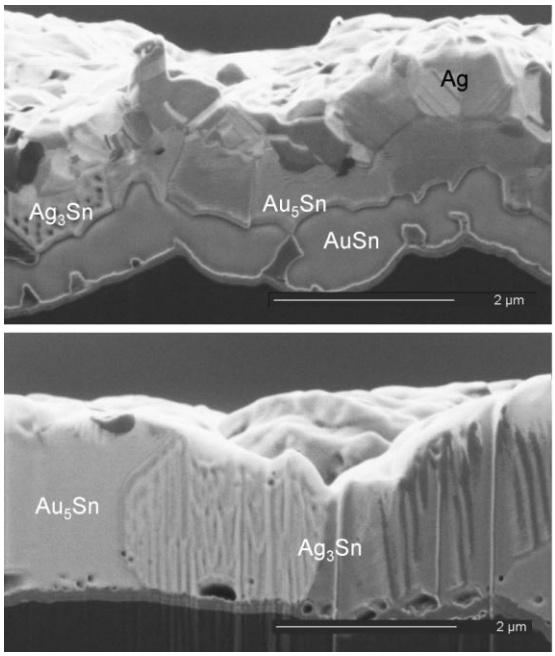

Figure 32: FIB micrograph. top: 1 µm of Ag was sputtered on top of a 1.2 µm layer of Au/Sn eutectic alloy. Due to the heating of the sample by the sputtering process the metals have already partially reacted. bottom: after annealing at 573 K for 10 minutes the Au/Sn has reacted with the silver forming the binary Ag_3Sn and the Au_5Sn compounds.

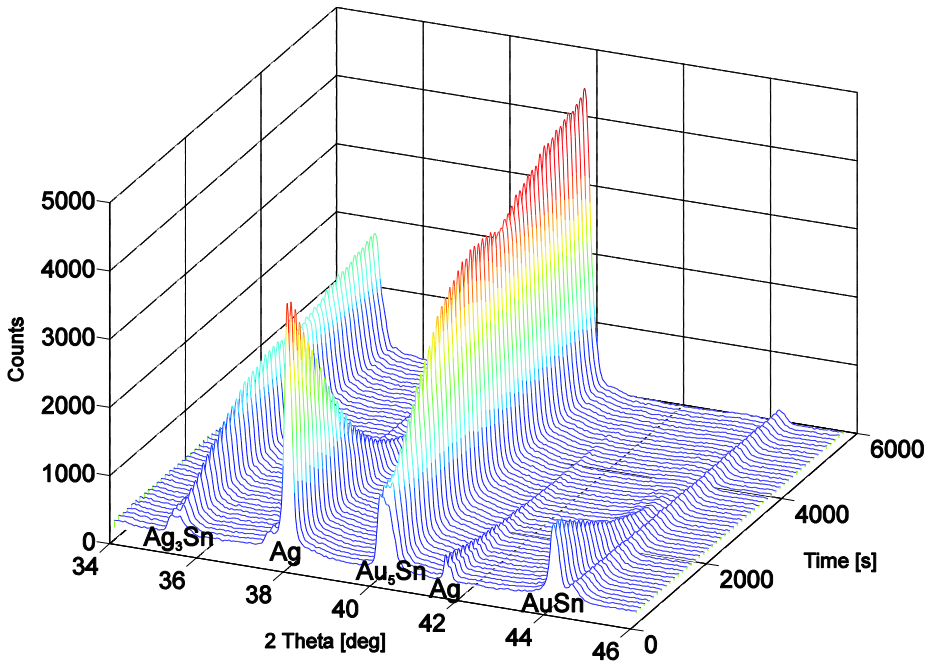

Figure 33: Detail of the XRD spectra taken during the isothermal anneal at 513 K of the Au-Sn/Ag thin film sample. Spectra were recorded in 5 min time intervals. The peaks of evolving intensity are marked with the phase they have been assigned to. The constant minor peaks at 35.3°, 37.6° and 44.5° stem from the silicon oxide substrate.

At the beginning of the anneal, the Ag_3Sn phase had already reached 20% of its maximum intensity and the Au_5Sn phasewas at 60%. During annealing the reaction takes place at a constant rate until the educts, Ag and AuSn, are close to depletion. Then it slows down, deviating from linearity and finally stops when all the silver is consumed. In this state, the layer thickness of the intermetallic phase was 1.8 µm, as it was determined from the FIB image in Figure 32.

During the 573 K anneal, the Au-Sn alloy was melted, as the eutectic point is at a temperature of 551 K. Therefore none of the Au-Sn phaseswas observed initially. During the anneal the tin from the eutectic melt reacts with the silver, forming Ag_3Sn and shifting the composition of the melt towards a more gold rich region. To compensate for that, the Au_5Sn phase precipitates from the liquid solder until all the material is solidified. At temperatures above the eutectic point the AuSn phase was not observed during the soldering process.

The growth of the intermetallic phases is linear over time for most part of the reaction until it passes over to an exponential function, just as it was observed for the reaction with copper. The reaction rates extracted by linear fits are entered in the Arrhenius plot in Figure 35. The

Arrhenius fit yields an activation energy of 1.2 eV and the product of the pre-exponential factors is 40 m/s.

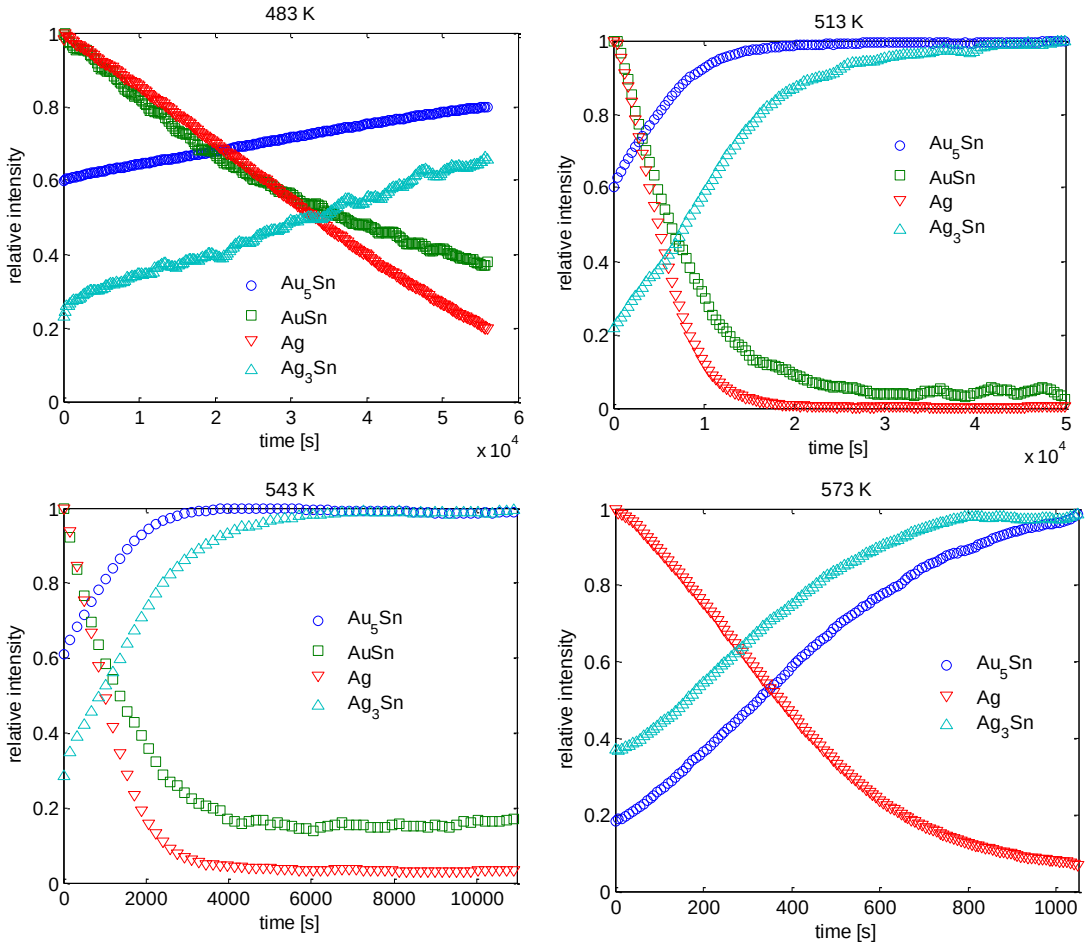

Figure 34: in-situ XRD. Evolution of the intermetallic phases in a Au/Sn – Ag thin film sample during an isothermal anneal at 483 K, 513 K, 543 K and 573 K. The tin-rich δ-phase (AuSn) is transformed into the gold-rich ζ'-phase (Au_5Sn) and the excess tin forms the ε-phase (Ag_3Sn) with the silver.

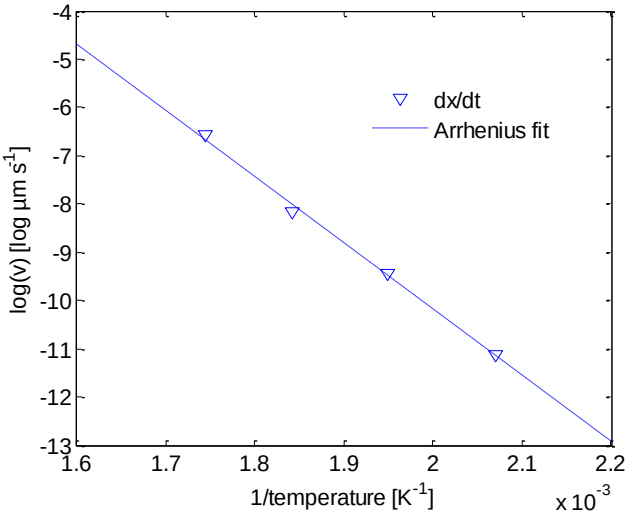

Figure 35: Arrhenius plot of the logarithm of the Ag_3Sn growth speed versus the inverse temperature. The slope of the fit is proportional to the activation energy.

To underpin the results of the in-situ XRD, two pairs of time and temperature values were calculated from the results, so that half of the filler material would be consumed by the reaction. At a temperature of 603 K this will be the case after 100 s and at 573 K after 300 s. The corresponding cross sections of the produced joints are depicted in Figure 36 and Figure 37. The phases were identified by EDX, and the recorded spectra are depicted in the right part of the figures. The resolution of the EDX does not allow a quantitative identification, but the difference in the silver content is enough to assign the different gray scales to the phases identified by XRD. Both joints have a similar morphology although different process parameters have been applied. Only about half of the filler material has reacted with the silver substrate. This agrees with the prediction based on the XRD results and confirms the model.

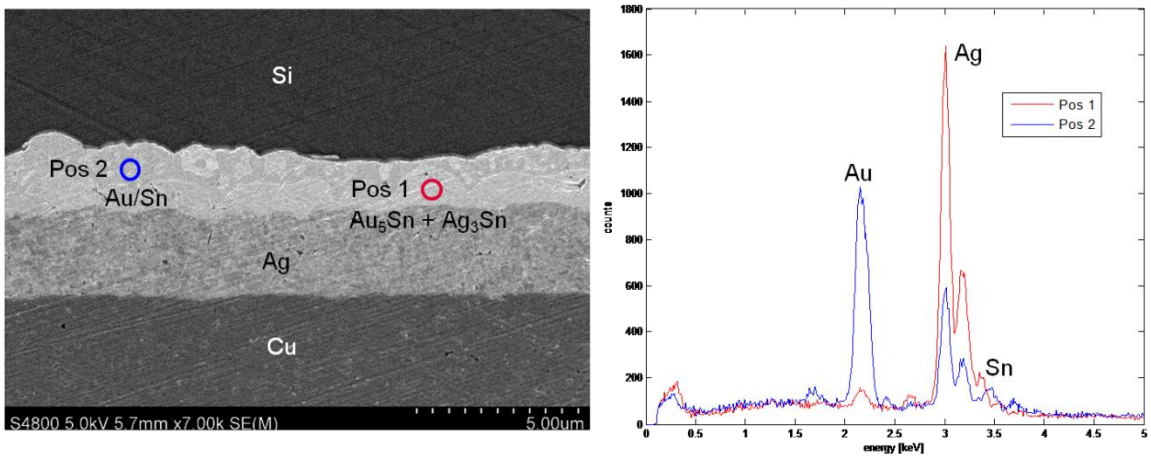

Figure 36: SEM of a cross-section of a joint soldered at 603 K for 100 s with eutectic Au/Sn solder on Ag. right: EDX spectra recorded at the positions indicated in the SEM. Only half of the filler material has reacted with the substrate as it is predicted by the in-situ XRD results.

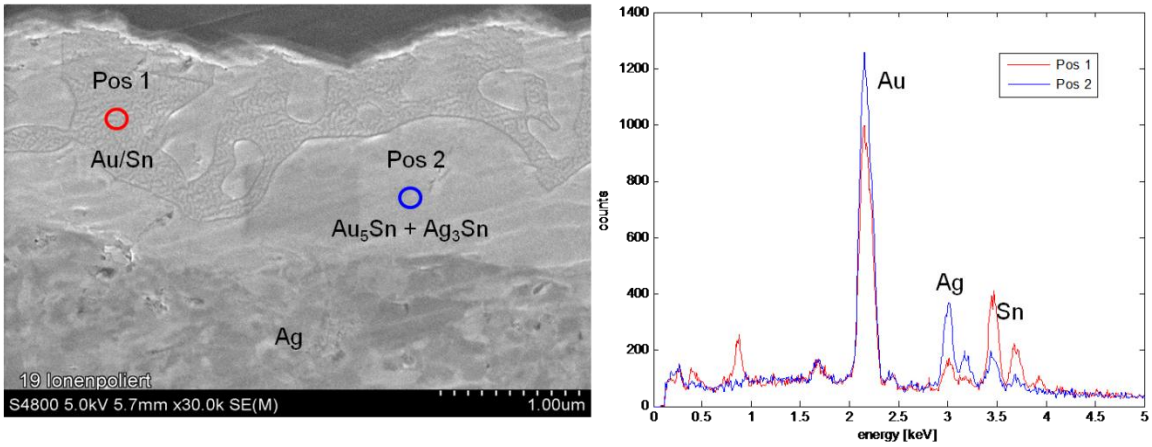

Figure 37: SEM of a cross-section of a joint soldered at 573 K for 300 s with eutectic Au/Sn solder on Ag. right: EDX spectra recorded at the positions indicated in the SEM. The morphology of the joint is similar to the one shown in Figure 36 although different process parameters were used.

2.4 Gold/tin on nickel

Nickel is the third commonly used surface finish for lead frames. It is a compromise between the expensive but relatively inert silver plating and the bare copper. Nickel is employed for Economy Thin Super Small Leadless packages (eTSSLP).

For in-situ XRD measurements a 1 µm thick layer of Nickel was deposited on top of the 1.2 µm thick Au/Sn layer. Nickel is a ferromagnetic metal and can therefore not be deposited by magnetron sputtering, because the nickel target would exert too much force on the rotating magnet. Therefore the nickel was evaporated in a vacuum chamber. A FIB micrograph of the produced layer stack is shown in the top part of Figure 38. Initially there was a smooth interface between the Au-Sn and the Ni. After an anneal at 533 K for 30 minutes, some of the Ni has dissolved in the Au-Sn and an additional layer has appeared at the interface (see lower part of Figure 38). In the annealed sample only the Au_5Sn phase, pure Ni and a Ni_3Sn_4 phase were found by qualitative XRD. Therefore a reaction of the following form can be assumed:

$$5\,AuSn + 3\,Ni \rightarrow Au_5Sn + Ni_3Sn_4$$

The tin rich phase (AuSn) of the eutectic Au-Sn alloy reacts with the Ni to form a Ni-Sn binary compound and the gold rich Au-Sn phase; a similar process to the reaction with silver. The monoclinic Ni_3Sn_4 compound is only one out of three Ni-Sn phases that are stable at room temperature but only this one is observed in the investigated reaction of Au-Sn with Ni. [15] It is well established that in thin film diffusion couples, not all of the compound phases predicted by the equilibrium phase diagram are present. [16] The suppression of the other two Ni-Sn phases indicates the significance of the kinetics in this reaction. Au and Ni on the other hand form no binary phases at all. [14] No ternary Au-Ni-Sn phase was found either, which is not surprising as the only genuine ternary phase in the system of the virtually stoichiometric composition $AuNi_2Sn_4$ exists at temperatures above 670 K. [17]

With in-situ XRD, the dynamics of this reaction can be observed in real time. Figure 39 shows a series of XRD specular scans taken of a Au-Sn/Ni layer stack at 533 K. The peaks corresponding to the educts of the reaction disappear over time, whereas the ones corresponding to the products

increase. Integrating the peak intensities and summing over all peaks matching a single phase yields the plots in Figure 40. The plots for the five investigated temperatures look qualitatively the same and differ only in the timescale. The reaction progresses at a constant rate in the beginning until about 40 % of the educts have been consumed. Thereafter the reaction slows down in an exponential manner because the educts are diluted by the products. After a sufficient anneal time, which is about 10 minutes at 533 K, the reaction is completed and the peak intensities remain constant. All the peaks of one phase show identical dynamics, i.e. they increase or decrease at the same rate as their sum. Thus a texture effect is very unlikely.

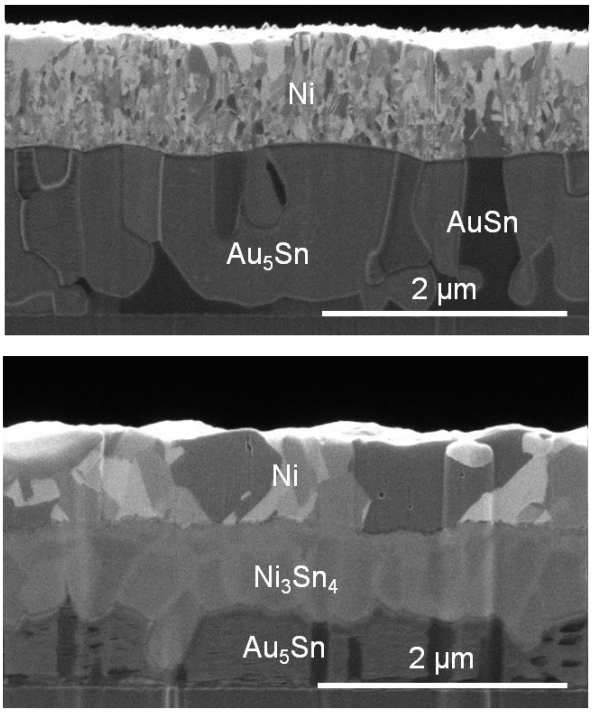

Figure 38: FIB micrograph; Top: A 1.2 µm thick layer of the eutectic Au/Sn alloy and a 1 µm thick Ni layer were deposited on a silicon wafer. The two different intermetallic compounds Au_5Sn and AuSn of the eutectic alloy can be clearly distinguished. Bottom: After annealing the sample at 533 K for 30 minutes the AuSn phase has reacted with the Ni to form a Ni_3Sn_4 layer.

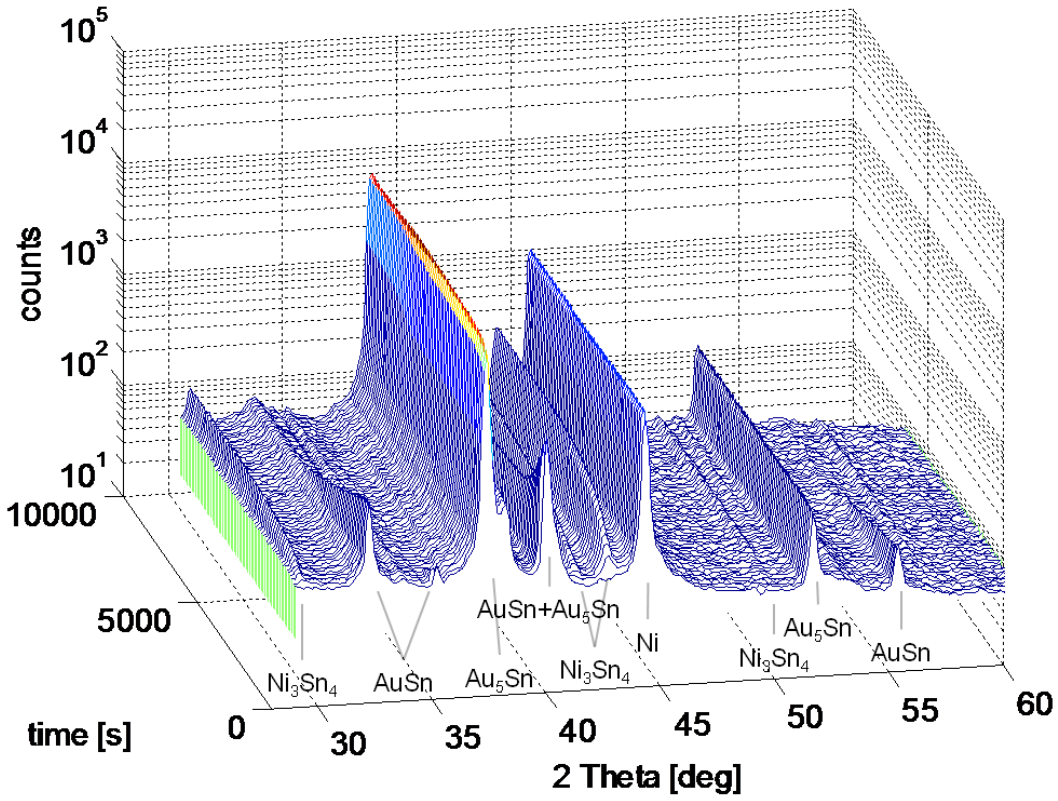

Figure 39: Detail of the in-situ XRD spectra taken during the isothermal anneal at 533 K of the Au-Sn/Ni thin film sample. Spectra were recorded in 10 s time intervals. The peaks of evolving intensity are marked with the phase they have been assigned to.

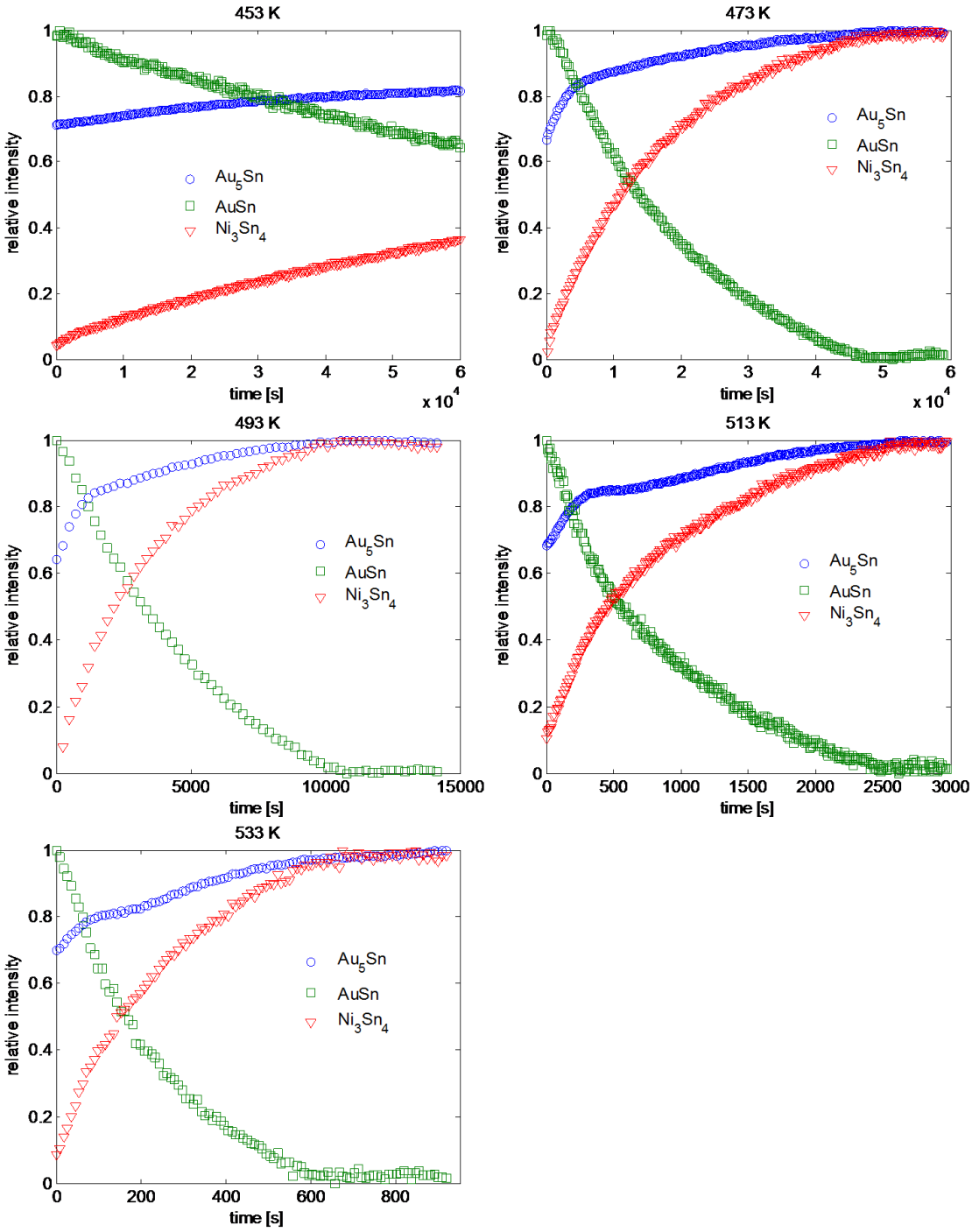

Figure 40: Evolution of the intermetallic phases in Au-Sn/Ni couple at temperatures of 453 K, 473 K, 493 K, 513 K and 533 K as it was obtained by in-situ XRD. The AuSn phase reacts with Ni to form the Au5Sn phase and the Ni3Sn4 phase. The plots are qualitatively very similar only differing in the time scale

Figure 41 shows the evolution of the primary reaction product, Ni_3Sn_4, during annealing at all investigated temperatures, 453 K, 473 K, 493 K, 513 K and 533 K in one plot for direct comparison.

In principle the reaction rate can be limited by two mechanisms: The diffusion of the products to the interface where the reaction is taking place, or the kinetics of the compound formation itself. [13] When the reaction is limited by diffusion, the compound formation will obey a square root law and when the kinetics of the compound formation limit the reaction, it is linear at first and then passes into an exponential function in the form of

$$x = x_0 \left(1 - e^{-at}\right) ,$$

Where x is the layer thickness of the reaction product, x_0 is the final layer thickness, a is the reaction rate and t is the time. [18] Data fits for both models are plotted in Figure 41. From this graph it is obvious that the reaction of Au-Sn with Ni is best described by equation above and is thus a reaction rate limited process.

For every temperature the fit parameter a can be extracted. This parameter is equivalent to the initial reaction rate as it is also the slope of the curve at t=0. The values obtained for the reaction rate at different temperatures are plotted in an Arrhenius plot in Figure 42. The temperature dependence of the reaction rate follows an Arrhenius law. From the Arrhenius fit the activation energy was determined to be 1.6 eV with a pre-exponential factor of $4.8 \cdot 10^6$ m/s.

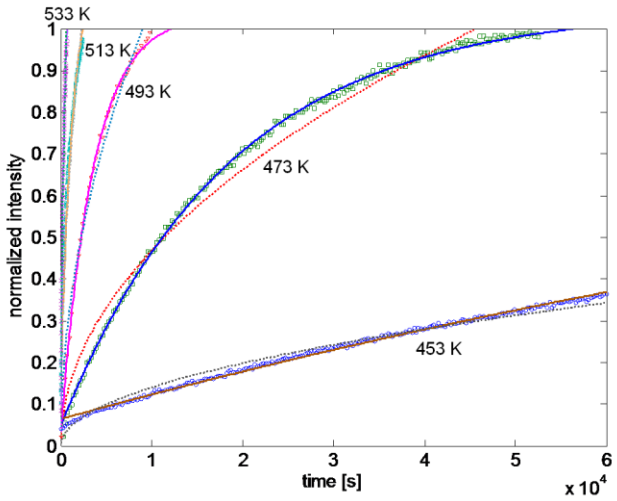

Figure 41: Evolution of the Ni_3Sn_4 phase in Au-Sn/Ni thin film diffusion couples at temperatures of 453 K, 473 K, 493 K, 513 K and 533 K. The data was fitted with a square root function as it is expected for a diffusion limited process (dotted line) and an exponential function as it is expected for a reaction limited process (solid line).

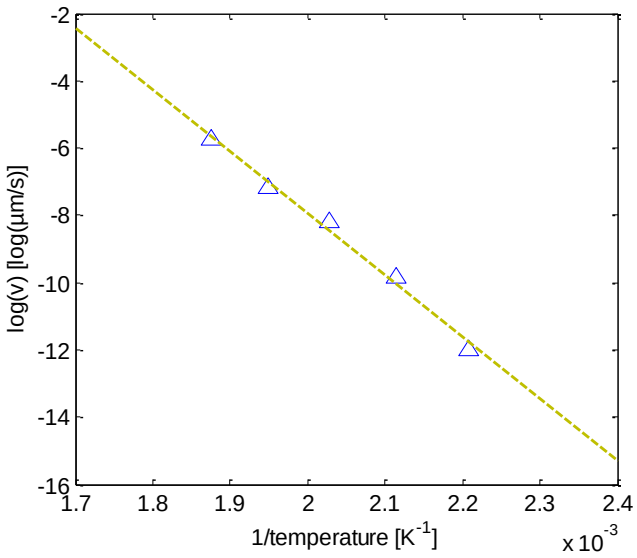

Figure 42: Arrhenius plot of the rate constants for the reaction of Au-Sn with Ni. The temperature dependence can be described by an Arrhenius equation with an activation energy of 1.6 eV.

2.5 Tin on Copper

Although alloys of copper and tin are known as bronze and are used since thousands of years, the combination of tin as a filler material and copper as a high melting point substrate for diffusion soldering has just recently been discovered and is still under evaluation to be used for packaging of microelectronic devices. The main benefits of using pure tin as a filler material instead of the eutectic gold/tin alloy are the cost savings. The gold price has constantly been rising over the last few centuries and no change to that is expected. Pure tin is very prone to oxidation and thus requires a thin protection layer of silver on the surface and an inert gas atmosphere has to be maintained throughout the die attach process. In contrast to the Au/Sn systems an additional layer of copper is deposited under the filler material, so that during the soldering the copper can diffuse into the liquid filler from the lead frame underneath and the copper layer on the side of the chip. This way the process can be accelerated.
In the following a complete investigation of the copper-tin system is described. In the first part the two possible deposition techniques for the backside metallization are compared. The electrochemical deposition method is associated with the aging effect, a problem which can be avoided with a simple annealing step as it is described in the second part. The last part deals with the dynamics of the soldering process itself, comparable to the Au/Sn systems.

2.5.1 ECD vs. PVD

In practice two methods are available to coat the wafer backside with the copper and tin layer: electrochemical plating and sputtering. Although both methods can produce nominally the same metal layer stacks, the products differ significantly in terms of the intermetallic compounds (IMC) formed and the orientation of the crystals in the polycrystalline thin films. The dynamics of diffusion and IMC formation are very sensitive to these properties. In order to understand the soldering process it is important know the composition of the original system.
Two intermetallic Cu/Sn phases are stable at room temperature. These are the Cu_3Sn (ε-phase) and the Cu_6Sn_5 (η'-phase). The former has an orthorhombic lattice with a=5.52 Å, b=38.16 Å, and c=4.33 Å and the latter has the ordered, hexagonal NiAs structure with a=4.20 Å and

c=5.09 Å.[20],[21],[5] The η'-phase is richer in tin content as compared to the ε-phase and grows in bimetallic Cu/Sn films below room temperature.[6] The copper rich phase in contrast was found only in samples annealed above 60°C [5]. The XRD spectra of an electrochemically plated specimen and a sputtered specimen, both having 1µm of tin on 5µm of copper, scanned one week after preparation, are shown in Figure 43. Reflections corresponding to the tin-rich Cu_6Sn_5 phase are found in both samples, whereas the Cu_3Sn peaks were only observed for the sputtered sample. This is can be explained by the circumstances of the deposition. Electrochemical deposition is a cold process. The temperature is buffered by the large thermal mass of the electrolyte and thus it does not exceed ambient temperature despite the high currents needed for deposition. During sputtering, in contrast, the wafer is heated significantly, as the sputtering power is dissipated on the wafer surface, which is thermally insulated by the low pressure atmosphere in the chamber. The higher temperature during the deposition process allows for the formation of the copper rich phase. Figure 44 shows FIB micrographs of a sputtered and an electroplated specimen. In the ECD specimen single grains of Cu_6Sn_5 penetrate into the tin layer. The PVD sample exhibits a more regular layered structure of the intermetallic phases. A fine grained layer of the copper rich phase is present, adjacent to the copper layer and a layer of the tin rich phase on top.

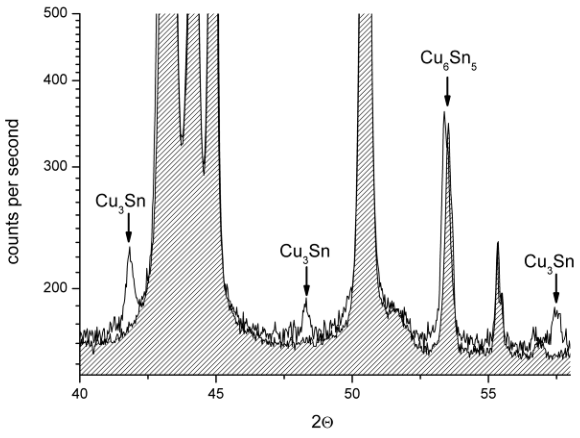

Figure 43: XRD patter of a electroplated sample (shaded) and a sputtered sample. The peaks corresponding to the Cu_3Sn are only observed in the sputtered sample, whereas the Cu_6Sn_5 phase is observed in both.

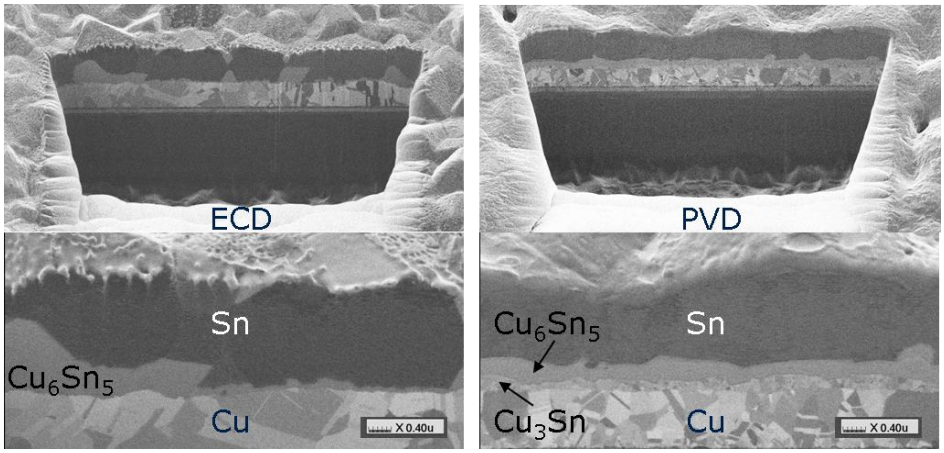

Figure 44:Focused ion beam micrograph of a electroplated (left) and a sputtered (right) copper/tin thin film couple. (tilt angle: 45°) In the electroplated sample only the copper rich η'-phase was found, whereas in the sputtered sample a layered structure of both, η'- and ε-phase, can be seen.

Plated and sputtered films do not only differ in the composition of intermetallic compounds, but also in the orientation of the grains. The film texture is of particular interest owing to the anisotropic property variations observed in copper and tin. For example, the elastic modulus of copper in the <111> direction is 2.9 times higher than in the <100> direction.[22] Reaction rates for oxide and silicide formation on copper are faster along the (100) face than the (111) face.[23]

The method of choice for the determination of the thin film texture is a XRD polar scan: In order to determine the orientation of a lattice plane the detector is first set to the proper Bragg angle, for the diffraction peak of interest. Then the sample is rotated in a goniometer in all directions of space. In the case of a polycrystalline sample, the intensity recorded at a certain sample orientation is proportional to the volume fraction of crystallites with their lattice planes in reflection geometry.[24]

Figure 45 shows the pole figures of the (200) reflex of copper and tin each deposited by PVD and ECD. These experimental pole figures were corrected for defocusing and displayed as a stereographic projection. For the copper specimen 1.8 µm of copper were deposited on a silver seed layer. For the Sn specimen 2.4 µm were deposited on top of the copper. The pole figures were recorded one week after deposition.

PVD copper exhibits a strong and sharp (111) fiber texture. The recorded (200) reflex only appears under an angle of 54.7° to the specimen surface normal. This angle corresponds to the

angle between the <200> and the <111> direction. This means that most of the crystallites in the sheet are oriented with their (111) plane parallel to the surface, but randomly oriented in the plane of the sample surface. As copper has a face centered cubic structure, the (111) plane is closest packed, and is therefore a very stable, low energy surface.[25]

ECD copper in contrast shows no texture at all. The intensity of the (200) peak is equal in all directions of space and the crystallites are oriented randomly in the sample. Lingk et al. have proposed a model, that multiple twinning, which is induced by electrolyte residuals in the layer, leads to the weakening of an original (111) fiber texture within hours after deposition.[26]

For PVD Sn the pole figures of the (200), (211) and (101) have been recorded, so that the texture could clearly be assigned. Two preferred orientations of the Sn crystallites were found: About 70% of the crystallites are oriented in <021> direction and the remaining 30% in <110> direction. The quantification of the orientation distribution was done by integrating the corrected intensity for each peak (see Figure 46).

ECD tin exhibits a strong (112) texture, which was identified by recording pole figures of the (200) and (211) reflex. The results of the texture analysis are summarized in Table 1.

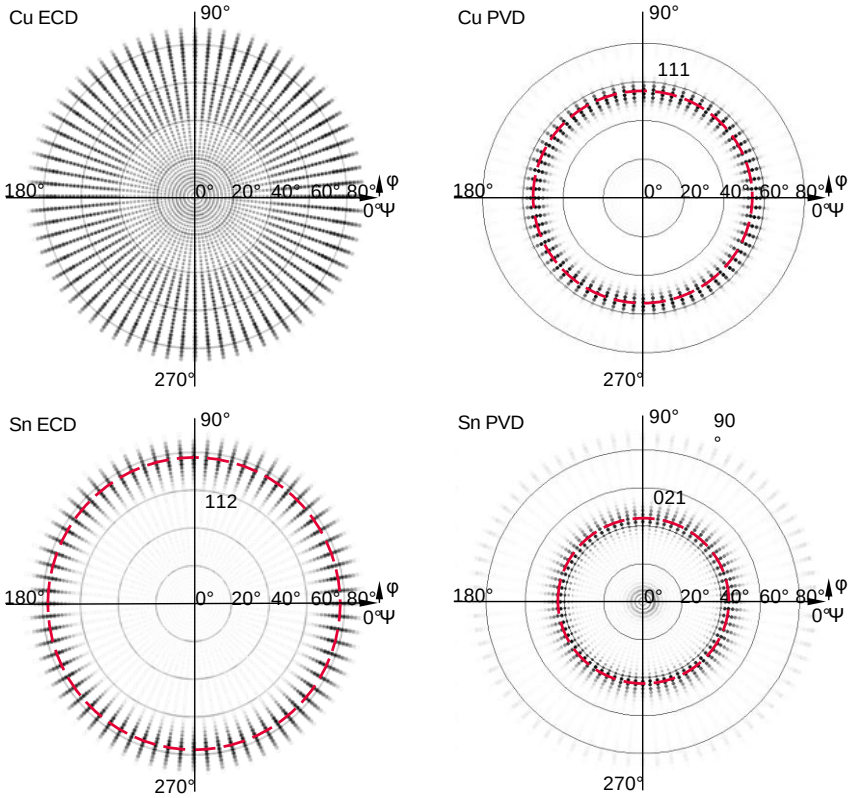

Figure 45: XRD pole figures of the (200) reflex of copper and tin, each deposited by PVD and ECD. The recorded intensity at a specific angle is proportional to the grayscale of the plotted data point. The identified preferred crystalline orientations are marked in the plots.

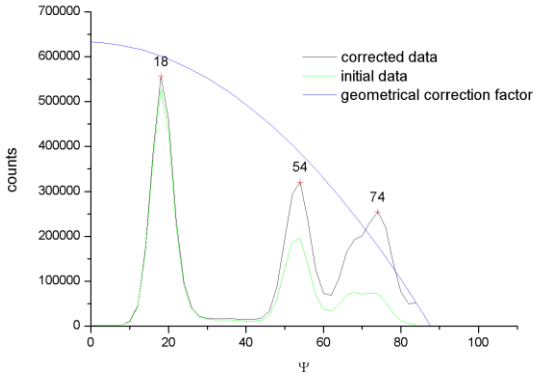

Figure 46: Integrated intensity of the (101) reflex of sputtered tin. The intensity has been corrected for geometrical distortions by a correction function obtained from a silicon powder normal, in order to quantify the distribution of crystalline orientations.

Metal layer	Preferred crystal orientation	Planar packing density
Cu PVD	(1 1 1)	17.8 nm^{-2}
Cu ECD	isotropic	-
Sn PVD	(0 2 1) 70% (1 1 0) 30%	2.0 nm^{-2} 7.7 nm^{-2}
Sn ECD	(1 1 2)	5.5 nm^{-2}

Table 1: Summary of the results of the texture analysis on electrochemically deposited and sputtered copper and tin films.

2.5.2 Aging effect in electroplated copper/tin couples

In practice it was observed that chips with electroplated copper/tin backside metallization have a limited storage life of about six month in contrast to sputtered chips. When more time has passed after the electrochemical deposition, the die attach could not be done without massive voids in the joints. In the electroplated film significant amounts of the Cu_6Sn_5 phase were found after six months but not in the sputtered films. This intermetallic phase is not melted during the die attach process and acts as a solid spacer, preventing the liquid tin from wetting the lead frame.

This observed difference between the ECD and the PVD layer stacks was attributed to the Cu_3Sn phase which is only found in the PVD metallization (see Figure 44). It is known that the Cu_6Sn_5 phase readily forms at room temperature, whereas the Cu_3Sn phase only forms at temperatures above 333 K. [5] Thus the ECD film was exposed to a one minute anneal at 473 K to obtain a phase composition similar to the PVD film.

Some representative micrographs are shown in Figure 47. Twenty four hours after deposition, some grains of Cu_6Sn_5 are observed along the grain boundaries of tin. This inhomogeneous growth can be explained by the fact that mass transport at moderate temperatures can be several orders of magnitude faster along grain boundaries than through the lattice. [27]

When the specimen was annealed at 473 K for one minute, there was enough thermal energy for both phases, Cu_3Sn and Cu_6Sn_5, to form. A 0.3 µm thick layer of the Cu-rich Cu_3Sn phase forms on the Cu-side and a 0.4 µm thick layer of the Sn-rich Cu_6Sn_5 phase formed on the Sn-side. At

473 K, the process is dominated by bulk diffusion rather than grain boundary diffusion, thus the IMCs grow in a more homogeneous manner.

Annealed and unannealed samples were stored at 323 K, a temperature that is low enough to prohibit the formation of the Cu_3Sn phase, but high enough to speed up diffusion. After two weeks, the Cu_6Sn_5 phase had grown significantly along the grain boundaries of tin in the unannealed sample, nearly reaching the surface. However in the annealed sample, the thickness of the IMC layers only increased marginally. The continuous Cu_3Sn layer slows down the diffusion of Cu along the grain boundaries of Sn thus inhibiting the aging of the Cu/Sn couple.

After four weeks of storage, Cu_6Sn_5 grains reached the surface in parts of the unannealed sample. This leaves insufficient pure tin for a proper wetting of the contact surface during soldering. The annealed sample on the other hand was hardly affected even after six weeks of storage at 323 K. The Cu_3Sn layer produced by the short anneal is an effective diffusion barrier and allows the use of ECD as a deposition method for backside metallizations for diffusion soldering.

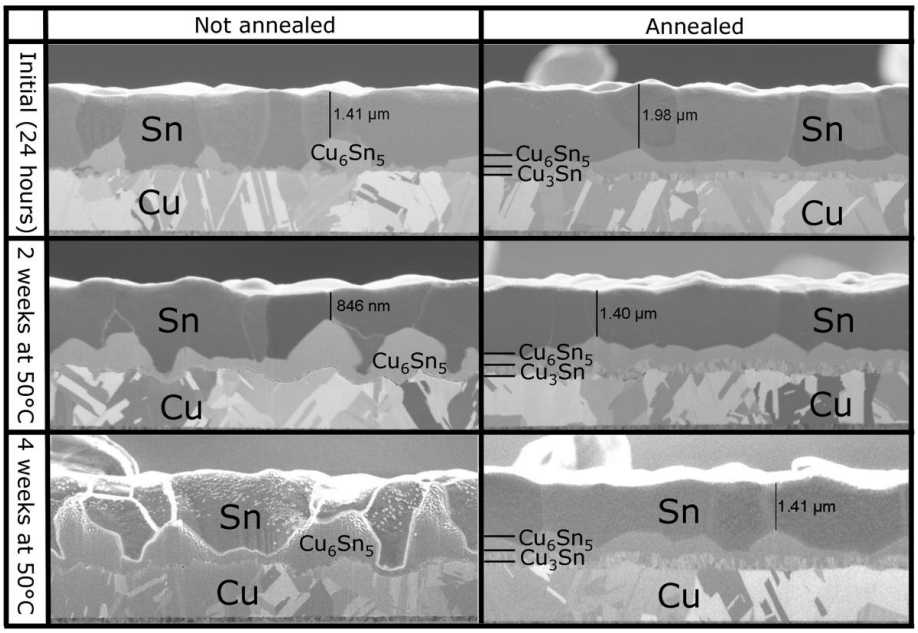

Figure 47: FIB micrographs of Cu/Sn-couples on a Ag seed layer. The left column shows the evolution of not annealed, as deposited, couples and the right column shows couples that were annealed at 473 K for one minute. The top row shows the couples after 24 hours. In the as deposited sample, the Cu_6Sn_5 phase is present and extends mainly along the grain boundaries into the Sn. The middle row shows couples after 2 weeks of storage at 323 K. The bottom row shows couples after 4 weeks of storage at 323 K. After 4 weeks, the Cu_6Sn_5 phase penetrates the Sn layer reaching the surface of the as deposited sample. The annealing produces a planar layer of Cu_3Sn at the Cu/Sn interface which inhibits the diffusion of Cu into the Sn. Consequently, the annealed sample is nearly unchanged after 4 weeks of storage at 323 K.

2.5.3 Soldering dynamics

For in-situ XRD investigations of the reaction dynamics, a 5 µm thick film of copper was electrodeposited on a silver coated silicon wafer and 1 µm of tin was deposited on top.

Upon heating the Cu/Sn thin film couples, the two metals react forming intermetallic phases. Figure 48 shows FIB micrographs of the evolving Cu/Sn interface upon annealing at 180°C. Initially the two metals are cleanly separated. During annealing the intermetallics grow in a layered structure in which the copper rich ε–phase forms adjacent to the copper and the tin rich η–phase adjacent to the tin. After 300 min most of the tin has been consumed and both intermetallic phases are present in similar abundances. By further annealing the Cu_6Sn_5 phase is transformed into Cu_3Sn which is the final state after prolonged annealing. This process could be verified by in-situ XRD. Figure 49 shows a series of XRD spectra recorded during an isothermal

anneal of a copper/tin thin film at a temperature of 453 K. The peaks corresponding to tin are disappearing quickly while the peaks of the Cu_3Sn phase are growing. The peak of the Cu_6Sn_5 phase at $2\Theta = 53°$ is growing at first and then shrinking.

Figure 50 shows the time evolution of the relative abundances of the intermetallic phases as measured by XRD at annealing temperatures of 293 K, 423 K, 453 K, 473 K and 573 K. The data was obtained from by integrating the intensities of several XRD peaks associated with each phase and normalizing to equilibrium intensity at the end of the annealing process. At the 623 K anneal, which is well above the melting temperature of tin of 505 K, a difference in the phase composition compared to lower temperature anneals was found. XRD peaks at 2Θ positions of 42.8° and 62.3° indicate the formation of a CuSn phase [20]. It is assumed that this is a metastable phase that forms temporarily at high temperatures. Its evolution is closely related to the stoichiometrically similar Cu_6Sn_5.

It was found that at all assayed temperatures, Cu_3Sn grows in a linear fashion independent of the abundance of tin or Cu_6Sn_5. The linear growth, which has also been observed before by Rutherford backscattering [7], is in contradiction to the standard diffusion limited model. This predicts a square root time dependence, as it has been found for thick films. [18] Since marker experiments show that copper is the dominant diffusing species, the growth of Cu_3Sn is taking place at the Cu_3Sn/Cu_6Sn_5 interface. [28] The growth requires the supply of copper atoms from the bulk copper and their diffusion through the Cu_3Sn layer to the Cu_3Sn/Cu_6Sn_5 interface where they react with Cu_6Sn_5. Since the growth speed of Cu_3Sn is constant even if a fraction of the copper atoms is used to form Cu_6Sn_5, the release of copper atoms cannot be the rate limiting factor. Therefore it can be assumed that the reaction of copper with Cu_6Sn_5 is the rate limiting step for Cu_3Sn formation in thin films. By a similar argument the rate limiting factor of the Cu_6Sn_5 growth is the reaction of copper and tin.

In Figure 51 the formation of the Cu_3Sn phase and the consumption of pure tin are plotted for different temperatures. Because the Cu_6Sn_5 phase forms adjacent to the tin, it is assumed that the consumption of tin is equivalent to the net growth of Cu_6Sn_5, excluding the transformation of Cu_6Sn_5 to Cu_3Sn. The slope of the linear fits is proportional to a reaction rate. The higher the temperature is, the faster the reaction happens. The temperature dependence can be described by an Arrhenius law and thus a plot of the logarithm of the growth speed versus the inverse

temperature yields a straight line with the activation energy E_a given by the slope (see Figure 52). The Arrhenius law holds very well even for temperatures above the melting point of tin. The activation energy for the formation of Cu_3Sn was determined to be 0.8 eV with a pre-exponential factor of a_0=1.7·10^{-2} m/s, which is in good agreement with previous studies. [18,29–32] The activation energy for the consumption of tin, which is equivalent to the formation of Cu_6Sn_5, is slightly lower with 0.75 eV (a_0=1.6·10^{-3} m/s). This also explains why at lower temperatures more Cu_6Sn_5 is formed than at higher temperatures.

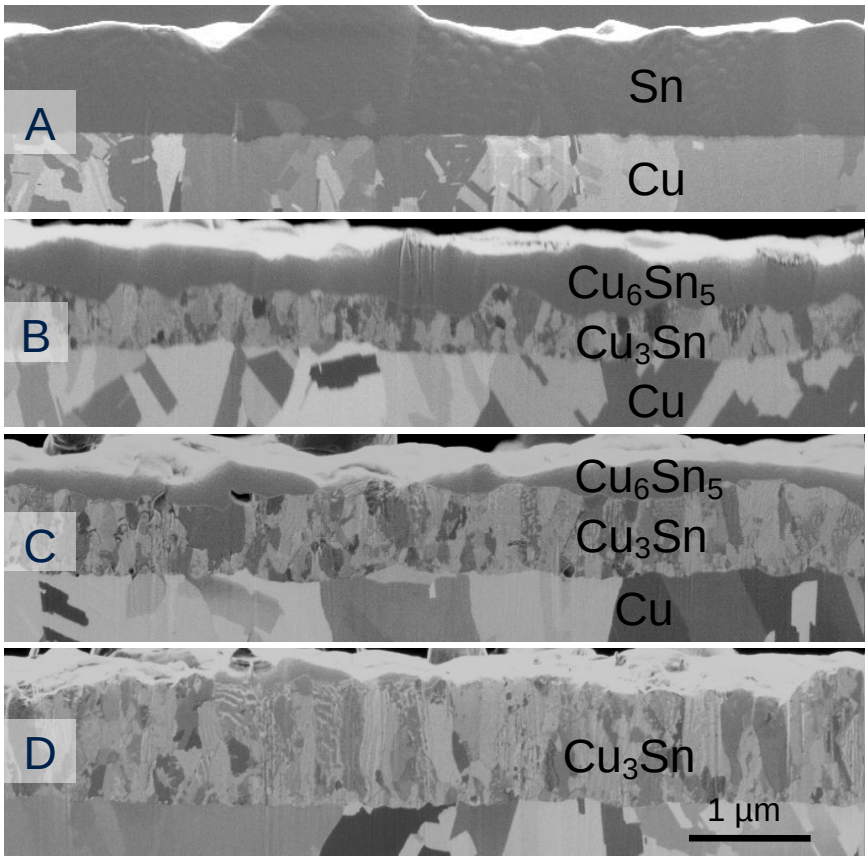

Figure 48: : FIB micrographs of the Cu/Sn thin film couples. (A) After electrodeposition. (B) After annealing at 453 K for 300 min. (C) After annealing at 453 K for 600 min. (D) After annealing at 453 K for 1000 min. The intermetallic phases grow in a layered structure in which the copper rich ε–phase forms adjacent to the copper and the tin rich η–phase adjacent to the tin.

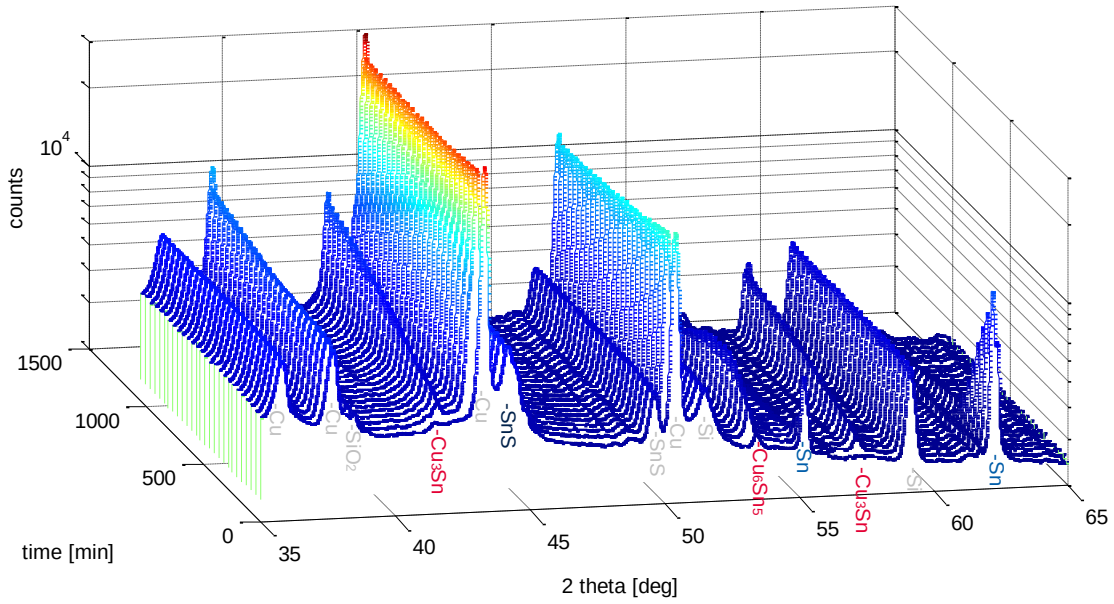

Figure 49: Detail of the in-situ XRD spectra taken during the isothermal anneal at 453 K of a copper-tin thin film couple. The peaks are marked with the phase they have been assigned to.

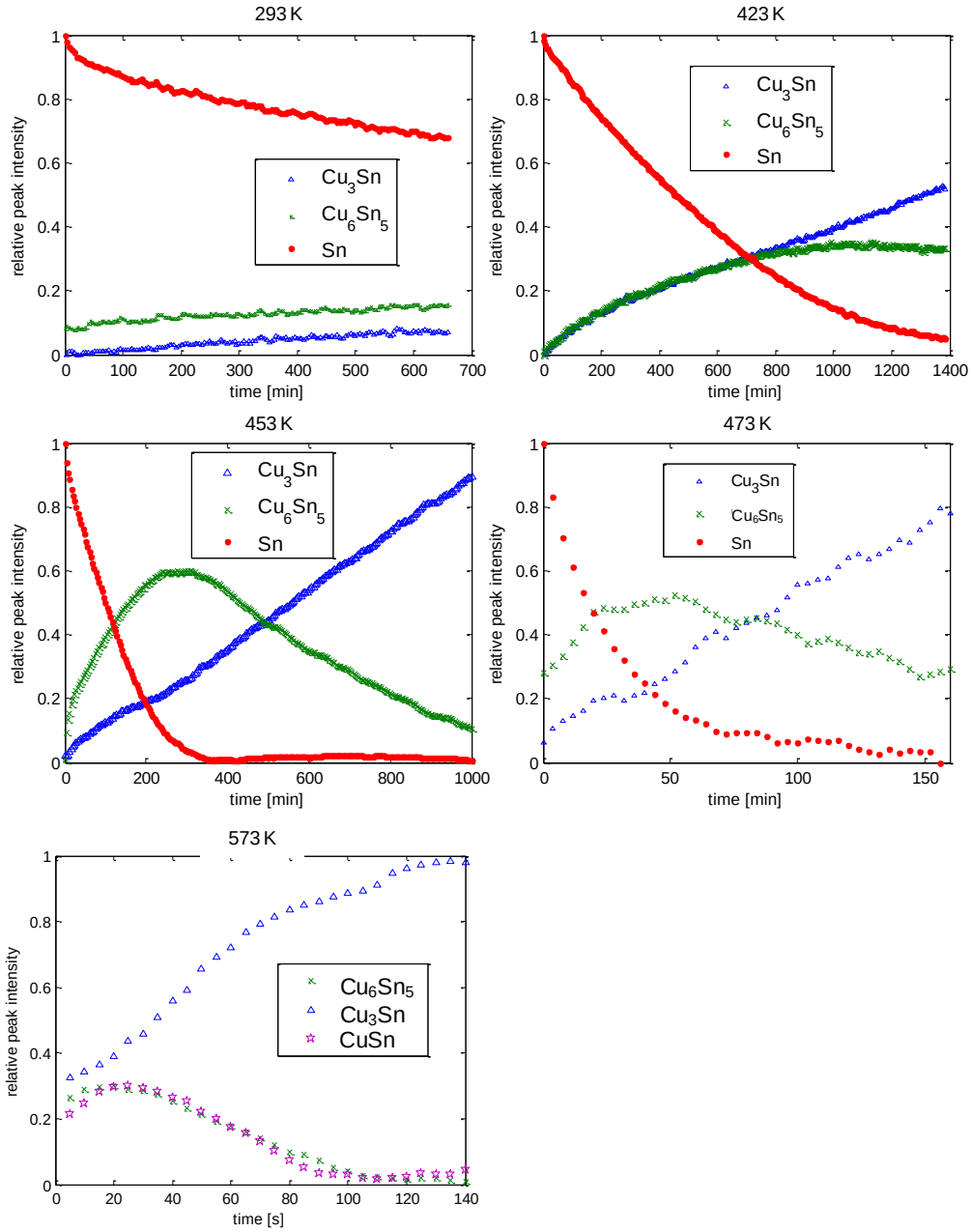

Figure 50: Evolution of the intermetallic phases in Cu/Sn couple at temperatures of 293 K, 423 K, 453 K, 473 K and 573 K as it was obtained by in-situ XRD. Copper and tin react to form the Cu_6Sn_5 phase at first which is then upon further annealing transformed into the Cu_3Sn phase. At a temperature of 573 K a metastable CuSn phase is observed.

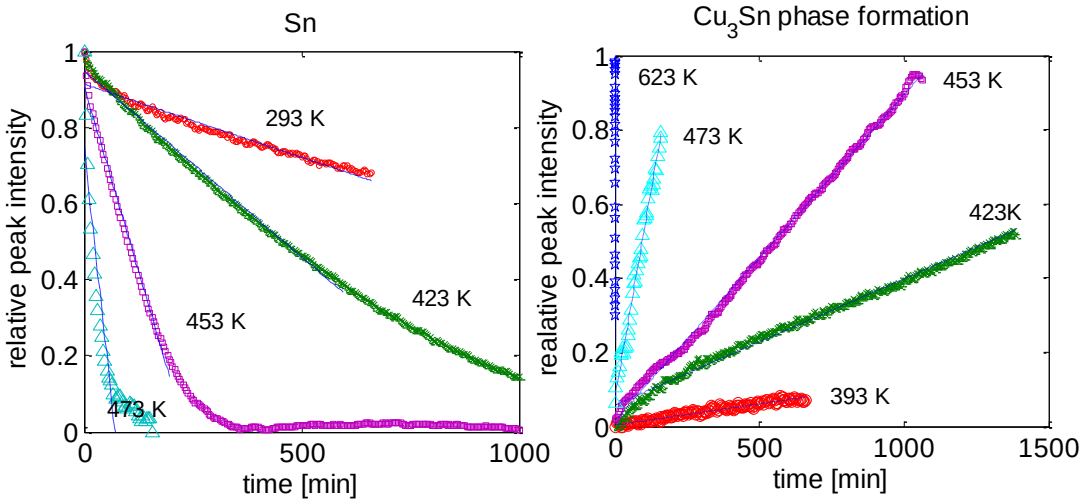

Figure 51: Consumption of Sn (left) and formation of Cu3Sn (right) at different temperatures. The phase evolution is linear over a wide range.

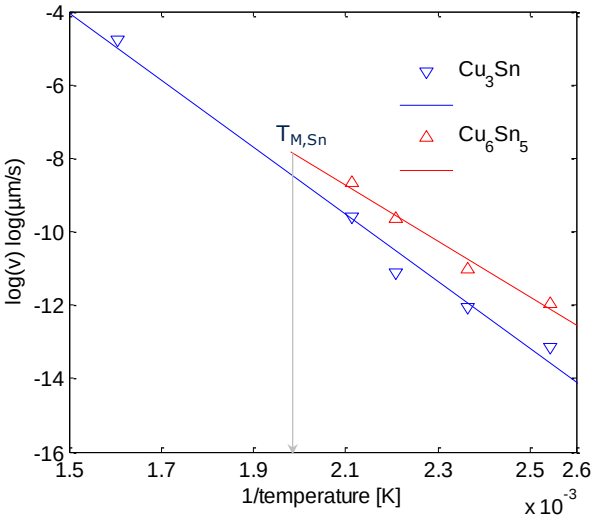

Figure 52: Arrhenius plot of logarithm of the growth speed of the Cu_3Sn and the Cu_6Sn_5 phase versus the inverse temperature. The slope of the linear fit is equivalent to activation energy.

Based on the results of the in-situ XRD one can calculate the time and temperature necessary to form a 500 nm thick Cu_3Sn layer. At a soldering temperature of 613 K this takes 100 s and 260 s at 573 K. To demonstrate the accuracy of the XRD results chips were bonded using these parameters. For this purpose wafers were plated with 1 µm of copper and 7 µm of tin. The wafers were cut with a diamond blade into 4 by 4 mm dice. These were pressed with 1.5 MPa onto a copper lead frame at the calculated temperature and time. Cross-sections of the joints were

produced by embedding the samples in epoxy resin, grinding and polishing. The surface of the cross-section was additionally ion polished to enhance the contrast between the different phases. For a qualitative phase identification, EDX spectra were recorded at the indicated positions. Figure 53 shows the cross-section of a joint soldered at 613 K for 100 s. All the Sn has been transformed into an intermetallic phase, but only an approximately 0.5 µm thick layer of the stable Cu_3Sn phase has grown on both interfaces to copper. The remaining volume of the joint is formed by the Cu_6Sn_5 phase. A joint like this would not melt if it is heated to the processing temperature, but the formation of the Cu_3Sn phase proceeds in the solid state after the die attach, during assembly and operation. Over time this leads to Kirkendall voids and ultimately the failure of the device. [15] The joint depicted in

Figure 54 has a similar morphology although it was soldered with different parameters (573 K, 260 s). This underpins the results obtained by XRD. Some parts of pure tin still remain in the joint after soldering. In the sample preparation the soft metal has been removed by ion polishing and has left behind cavities.

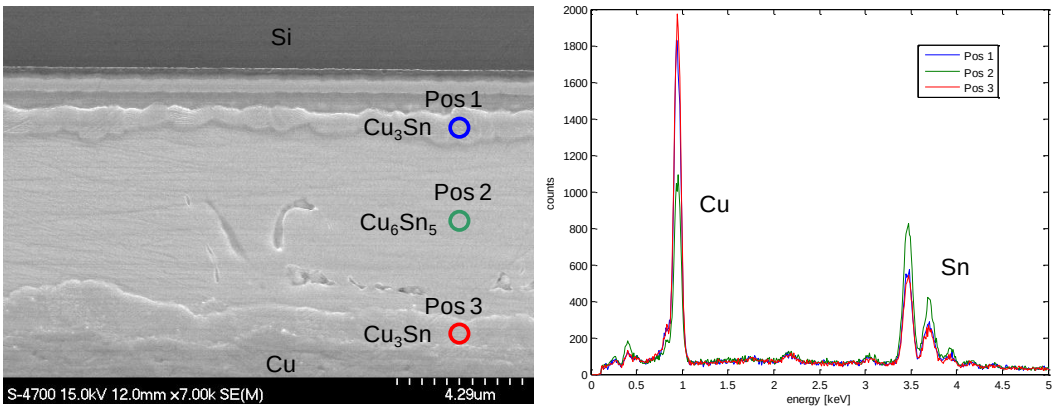

Figure 53: SEM of a cross-section of a joint soldered at 613 K for 100 s with a 7 µm thick tin layer as the filler metal between a 1 µm thick copper layer on top and a copper lead frame underneath. right: EDX spectra recorded at the positions indicated in the SEM. The joint has been completely transformed into Cu/Sn intermetallic phases, where the stable Cu_3Sn layer is only 0.5 µm thick on both sides.

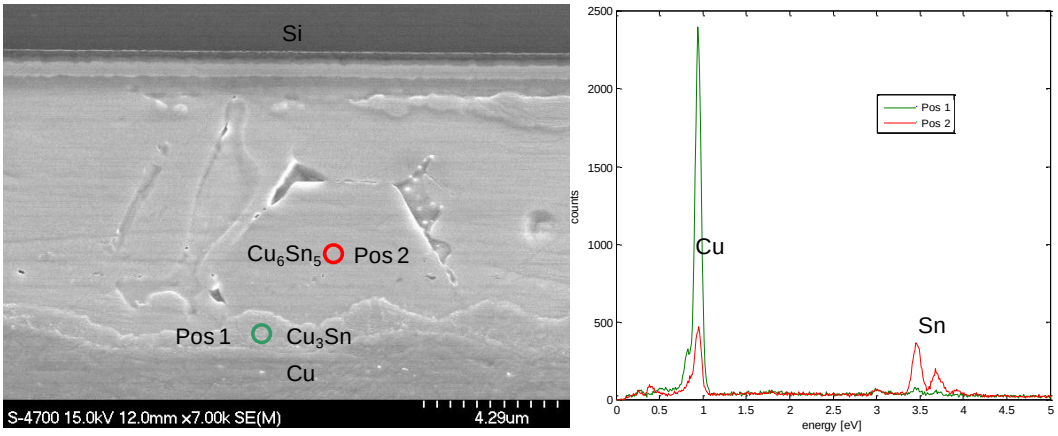

Figure 54: SEM of a cross-section of a joint soldered at 573 K for 260 s with a 7 µm thick tin layer as the filler metal between a 1 µm thick copper layer on top and a copper lead frame underneath. right: EDX spectra recorded at the positions indicated in the SEM. The joint has a similar morphology as the one depicted in Figure 53 although it was soldered with different parameters.

2.6 Conclusion

By the combination of *in-situ* XRD, FIB microscopy, SEM, STEM and EDX we were able to give an accurate description of the dynamics and morphology of the intermetallic phase evolution in isothermal diffusion soldering. The eutectic Au/Sn alloy was used as filler material on the three most common lead frame materials: Copper, silver and nickel. Copper reacts with the Au-Sn alloy to form a ternary compound, whereas silver and nickel only form binary compounds with tin. Additionally the combination of pure copper and tin was evaluated as a material system for diffusion soldering. These two metals form two intermetallic compounds of which the one richer in tin is only an interim reaction product and the copper rich phase is the stable end product.

The phase transformations progress initially linear in time, indicating a reaction controlled process, not limited by diffusion. The temperature dependence of the layer growth speed can be described by an Arrhenius law. The parameters of the activation energy and the pre-exponential constant for all investigated material systems are summarized in Table 2.

These parameters make it possible to predict with high accuracy the time necessary to form a stable IDS joint at all applied process temperatures. In Figure 55 the time to transform 90% of a

1200 nm thick filler layer is plotted versus the temperature. A graph like this is especially helpful for designing a die attach process.

The most significant point that was shown in this chapter is that the soldering reaction will not be completed in the time in which the chip is actively pressed on the substrate, which is typically in the range of 20 to 500 ms. This contradicts a common but false conception. The reaction proceeds afterwards while the whole assembly is still hot. Sufficient time has to be allowed for the reaction to complete in order to achieve a reliable joint.

Often the dies on a single lead frame do not experience the same temperature budget. It can take up to several hours to populate a lead frame, especially if the dice are very small. Thus the soldering reaction may be complete for the dice that have been attached the first but not for the last ones that were placed, just before the whole lead frame was demounted and cooled to room temperature.

The Cu/Sn soldering system which is still be tested on reliability for high volume production shows great potential from this study. Compared to the other material systems investigated the reaction is proceeding faster at common soldering temperatures. Furthermore it has a well-defined final state and all the initial phases are transformed during the process.

In general the presented results contribute to a better understanding of this advanced joining method extensively used in semiconductor packaging.

Reaction	Activation energy E_a [eV]	Pre-exponential factor a_0 [m/s]
6 Cu + 5 Sn → Cu_6Sn_5	0.75	$1.6 \cdot 10^{-3}$
Cu_6Sn_5 + 9 Cu → 5 Cu_3Sn	0.79	$1.7 \cdot 10^{-2}$
5 AuSn + 12 Ag → 4 Ag_3Sn + Au_5Sn	1.18	38
2 AuSn + 6 Cu → $Au_2Cu_6Sn_2$ 2 Au_5Sn + 6 Cu → $Au_2Cu_6Sn_2$ + 8 Au	1.24	$9.7 \cdot 10^{2}$
5 AuSn + 3 Ni → Au_5Sn + Ni_3Sn_4	1.60	$4.8 \cdot 10^{6}$

Table 2: Parameters of the reactions forming the intermetallic compounds in diffusion soldering. The temperature dependence of the growth speed is described by an Arrhenius equation.

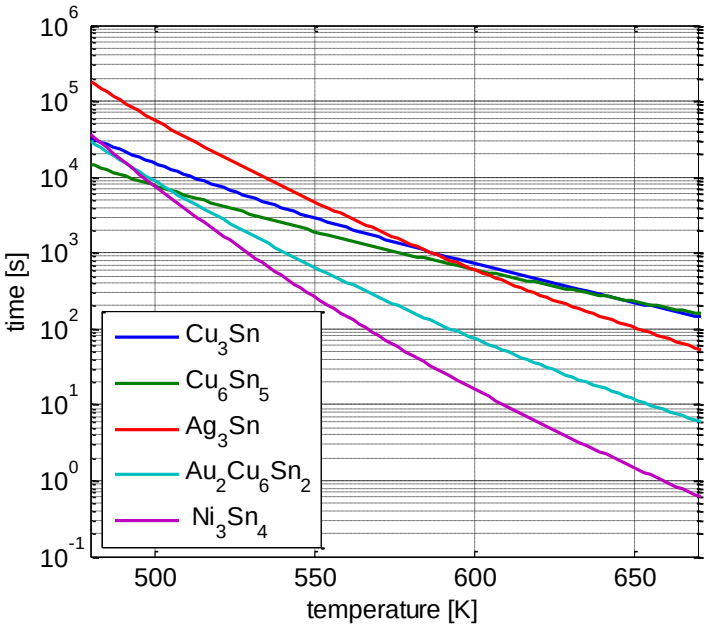

Figure 55: time to transform 90% of a 1200 nm thick layer of the filler material in the high melting point intermetallic phase. The graph was calculated based on the results of in-situ XRD.

2.7 References

[1] S. Sommadossi, W. Gust, E.J. Mittemeijer, Phase characterization and kinetic behaviour of diffusion soldered Cu/In/Cu interconnections, Materials Science and Technology. 19 (2003) 528–534.

[2] S. Sommadossi, A. Guillermet, Interface reaction systematics in the Cu/In–48Sn/Cu system bonded by diffusion soldering, Intermetallics. 15 (2007) 912-917.

[3] S. Sommadossi, W. Gust, E.J. Mittemeijer, Characterization of the reaction process in diffusion-soldered Cu/In-48 at.% Sn/Cu joints, Materials Chemistry and Physics. 77 (2003) 924–929.

[4] S. Sommadossi, L. Litynska, P. Zieba, W. Gust, E.J. Mittemeijer, Transmission electron microscopy investigation of the microstructure and chemistry of Si/Cu/In/Cu/Si interconnections, Materials chemistry and physics. 81 (2003) 566–568.

[5] K.. Tu, Interdiffusion and reaction in bimetallic Cu-Sn thin films, Acta Metallurgica. 21 (1973) 347-354.

[6] K.N. Tu, Cu/Sn interfacial reactions: thin-film case versus bulk case, Materials Chemistry and Physics. 46 (1996) 217-223.

[7] K.N. Tu, R.D. Thompson, Kinetics of interfacial reaction in bimetallic Cu---Sn thin films, Acta Metallurgica. 30 (1982) 947-952.

[8] K.N. Tu, A.M. Gusak, M. Li, Physics and materials challenges for lead-free solders, Journal of applied Physics. 93 (2003) 1335.

[9] S. Bader, W. Gust, H. Hieber, Rapid formation of intermetallic compounds interdiffusion in the Cu---Sn and Ni---Sn systems, Acta Metallurgica et Materialia. 43 (1995) 329-337.

[10] B. Gollas, J.H. Albering, K. Schmut, V. Pointner, R. Herber, J. Etzkorn, Thin layer in situ XRD of electrodeposited Ag/Sn and Ag/In for low-temperature isothermal diffusion soldering, Intermetallics. 16 (2008) 962-968.

[11] H. Etschmaier, M. Neuschitzer, P. Hadley, Reaction dynamics of the Au-Sn eutectic alloy with Ni in thin films, Materials Chemistry and Physics. to be published (2011).

[12] H. Etschmaier, J. Novak, H. Eder, P. Hadley, In-Situ XRD and FIB Microscopy Studies of the Dynamics of Intermetallic Phase Formation in Thin Layer Cu/Sn Films for Low-Temperature Isothermal Diffusion Soldering, MRS Online Proceedings Library. 1318 (2011).

[13] H. Etschmaier, J. Novak, H. Eder, P. Hadley, Reaction dynamics of diffusion soldering with the eutectic Au-Sn alloy on copper and silver substrates, Intermetallics. 20 (2012) 87-92.

[14] H. Etschmaier, H. Torwesten, H. Eder, P. Hadley, Suppression of interdiffusion in copper/tin thin films, Journal of Materials Engineering and Performance. to be published (2011).

[15] A. Paul, The Kirkendall effect in solid state diffusion, Doctoral Dissertation, Technical University of Eindhoven. (2004).

[16] O.B. Karlsen, A. Kjekshus, E. Rost, Ternary Phases in the System Au–Cu–Sn, Acta Chem. Scand. 44 (1990) 197–198.

[17] T. Massalski, Binary alloy phase diagrams, (1996).

[18] P.G. Harris, K.S. Chaggar, The role of intermetallic compounds in lead-free soldering, Soldering & Surface Mount Technology. 10 (1998) 38-52.

[19] U. Gösele, K.N. Tu, Growth kinetics of planar binary diffusion couples:''Thin-film case''versus''bulk cases'', Journal of Applied Physics. 53 (1989) 3252–3260.

[20] A. Westgren, G. Phragmen, X-ray analysis of copper-tin alloys, Z. anorg. Chem. 175 (1928) 80.

[21] J.D. Bernal, The Complex Structure of the Copper–Tin Intermetallic Compounds, Nature. 122 (1928) 54-54.

[22] D.P. Tracy, D.B. Knorr, Texture and microstructure of thin copper films, JEM. 22 (1993) 611-616.

[23] P.A. Flinn, G.A. Waychunas, A new x-ray diffractometer design for thin-film texture, strain, and phase characterization, J. Vac. Sci. Technol. B. 6 (1988) 1749-1755.

[24] H.-R. Wenk, P.V. Houtte, Texture and anisotropy, Rep. Prog. Phys. 67 (2004) 1367-1428.

[25] J.M.E. Harper, C. Cabral, P.C. Andricacos, L. Gignac, I.C. Noyan, K.P. Rodbell, u. a., Mechanisms for microstructure evolution in electroplated copper thin films near room temperature, J. Appl. Phys. 86 (1999) 2516.

[26] C. Lingk, M.E. Gross, W.L. Brown, Texture development of blanket electroplated copper films, J. Appl. Phys. 87 (2000) 2232.

[27] Y.-J. Oh, S.-Y. Oh, Inhomogeneous Consumption of the Electroless Ni-P Layer at the Solder Joint Formed with Sn-3.5Ag-0.7Cu, Journal of Elec Materi. 38 (2009) 2554-2562.

[28] B.F. Dyson, Interstitial Diffusion of Copper in Tin, J. Appl. Phys. 38 (1967) 3408.

[29] M.E. Warwick, S.J. Muckett, Observations on the Growth and Impact of Intermetallic Compounds on Tin-Coated Substrates, Circuit World. 9 (1993) 5–11.

[30] P. Kay, C.A. McKay, Barrier layer against diffusion, Trans. Inst. Met. Fin. 57 (1979) 169.

[31] P.J. Kay, C.A. McKay, The growth of intermetallic compounds on common basis materials coated with tin and tin-lead alloys, Trans. Inst. Met. Fin. 54 (1976) 68–74.

[32] C.J. Thwaites, Solderability of Coatings for Printed Circuits, Trans. Inst. Met. Fin. 43 (1965) 143.

3 Argon incorporation in sputtered Au/Sn films[2]

In the previous chapter the dynamics of the diffusion soldering process are treated. In order to achieve a reliable solder joint it is important to understand not only the process itself but also the characteristics of the involved materials and how to prepare them with the necessary properties. As mentioned before the most common alloy used as filler material for diffusion soldering is the eutectic Au/Sn alloy. In this chapter the effect of incorporation of discharge gas during sputtering in the deposited Au/Sn films and the consequences for the quality of the diffusion soldered joints are described.

3.1 Sputtering

The state of the art for the physical vapor deposition of thin metal films for various industrial applications is magnetron sputtering. [2] During sputtering, atoms are ejected from a solid target due to bombardment with energetic ions generated in a discharge plasma. A noble gas is commonly used as the discharge gas so it does not react with the deposited metals. Often Ar is chosen due to its availability and for economic reasons. It was shown experimentally that significant amounts of Ar can be incorporated into metal films during the sputtering process, especially in metals with high atomic mass. [3–7] Argon atoms are included into the growing film when high energy Ar ions are reflected from the sputtering target and get implanted into the sputtered film. Schmid et al. have found nanometer sized subsurface bubbles in sputtered aluminum after annealing related to incorporated Ar. [8,9] This has not been seen as an issue because no practical problems have been associated with this effect.

[2] The results presented in this chapter have been obtained in cooperation with Martin Sporn, Walter Lukesch and Adolf Winkler.

In this work metal films were deposited in an Oerlikon Clusterline 200 magnetron sputtering tool with a target-substrate spacing of 4 cm. First a 100 nm titanium layer was sputtered on the backside of (100) silicon wafers (diameter: 200 mm, thickness: 200 µm) to ensure that the surface of the wafer had a constant electrostatic potential. Then a 1.2 µm thick layer of the eutectic binary Au / 20wt.% Sn alloy was deposited by sputtering. Ar or Xe was used as the discharge gases. The flow of Ar and Xe through the sputter chamber was 95 sccm at a pressure of 0.2 Pa and 15 sccm at 0.6 Pa, respectively. The layers were deposited at a constant rate of 2 nm/s and the sputtering power was chosen accordingly; 360 W for Ar and 212 W for Xe. This reflects the increased sputtering yield for Xe. The substrate was kept at a floating potential, while the voltage of the target varied between -300 V and -500 V to achieve constant power.

After deposition, images of layer stack cross sections were taken in a FEI Vectra 200 focused ion beam (FIB) microscope (see Figure 56). For cross-sectional imaging, the silicon wafer was broken along a {100} plane to produce a smooth edge. Thereafter the surface was polished with a gallium ion beam at an acceleration voltage of 30 kV and a beam current of 20 nA. This way the image could be taken perpendicularly to the surface, yielding undistorted images for accurate thickness measurements. The acceleration voltage of the gallium ion beam used for imaging was 30 kV with a beam current of 9 pA. Figure 1a shows the cross section of a Au-Sn film deposited using Ar as sputter gas. According to the Au-Sn phase diagram, the eutectic alloy consists of two different intermetallic phases: the ζ'-phase (Au_5Sn) and the δ-phase (AuSn), which both have hexagonal lattices. [10] The δ-phase forms a lamellar structure in a ζ'-matrix and their ratio is about 2:3. Ar is known to reside on interstitial sites initially [11], but after annealing at 573 K for 7 min, the Au/Sn film was melted and large voids appeared (see Figure 56b). For the film sputtered with Xe as discharge gas (Figures 1c and 1d), this effect is not observed. In Figure 1d, the film exhibits a dense structure without voids after annealing. In both cases the melting and resolidification of the film leads to a phase separation and grain growth. The ζ' phase has a higher affinity to the titanium surface due to its similar lattice constant and thus precipitates preferentially underneath the δ-phase.

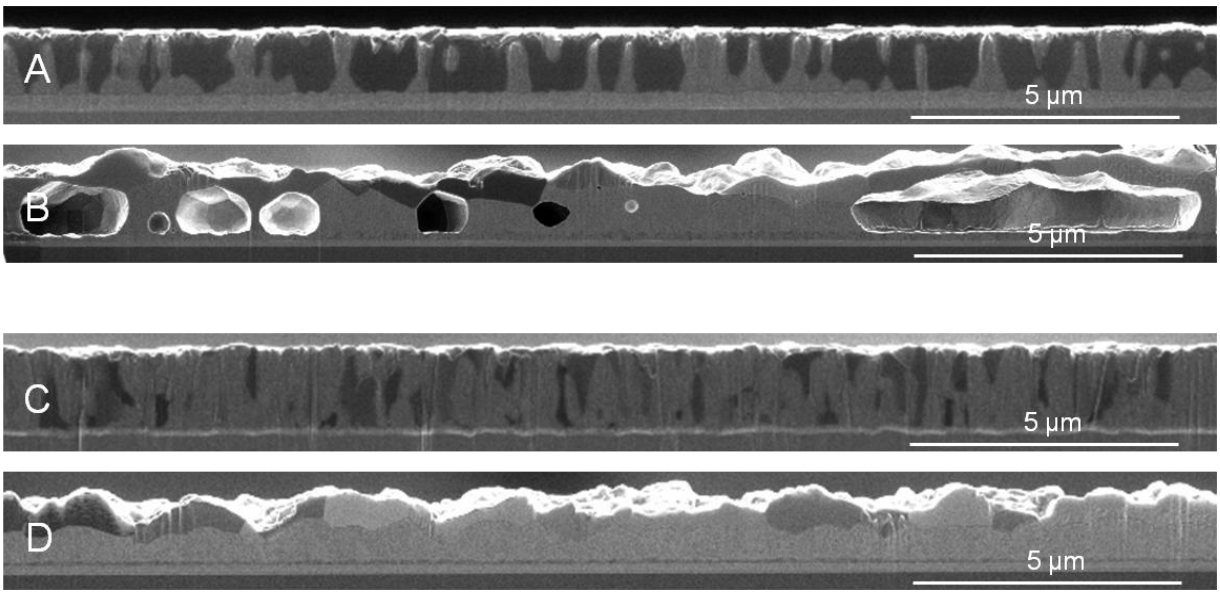

Figure 56: FIB micrographs of sputtered Au/Sn layers. A: sputtered with Ar, as deposited. B: sputtered with Ar, annealed for 7 min at 573 K. The incorporated Ar has agglomerated in large voids in the metal film. C: sputtered with Xe, as deposited. D: sputtered with Xe, annealed for 7 min at 573 K.

In the sputtering process, Ar ions in the discharge plasma are accelerated towards the target in the applied electrical field. The ions colliding with the target are partially implanted, but most are reflected as their charge is neutralized upon impact and they are no longer affected by the electrical field. [12] A part of their initial energy is transferred to the target causing the target material to be sputtered, the rest remains in the reflected neutral atoms. For an acceleration voltage of about 500 V, their energy is in the range of several tens to a few hundreds of electron volts. [3] This energy strongly depends on the target material and the discharge gas used. In a simplified but still very accurate model, the interaction between the gas ions and the target atoms can be described by an elastic collision where the ratio of the reflected energy E_r to the incident energy E_0 is

$$E_r/E_0 = ((m_2 - m_1)/(m_2 + m_1))^2$$

The more similar the atomic masses of the two elements are (m_1, m_2), the more energy will be transferred from the discharge gas atom to the sputtered atom and the less energy is left for the reflected atoms. Ar and Au have a ratio of atomic masses of 0.20 compared to 0.66 for Xe and Au.

This means that in a central, elastic collision of an Ar with a Au atom Ar is reflected with 44 % of its initial energy, whereas Xe only retains 4 % of its energy. At common pressures of the discharge gas, the mean free path of the atoms is much longer than the target-substrate spacing and they directly hit the substrate without any further collisions. [13] If their energy is sufficient to penetrate the growing film they get implanted. In contrast to Ar, the reflected Xe atoms do not have enough energy to penetrate the deposited metal film at commonly used DC sputtering voltages. An incorporation of the noble gas atoms by simple adsorption is very unlikely, because the adsorption energy of the gas atoms on metal surfaces ranges only from 0.05 to 0.35 eV. [2]

Thermal desorption spectroscopy was used to verify that Ar was indeed incorporated in the Au/Sn layer, while Xe was not. [14] For this purpose 10x10 mm^2 sized pieces of the differently processed samples were attached to a heated sample holder in an ultrahigh vacuum chamber (base pressure: $1x10^{-6}$ Pa). The samples were heated with a rate of 1 K/s and outgassing atoms were detected by a quadrupole mass spectrometer (QMS), which was positioned directly in front of the surface. The QMS was tuned to the masses 40 (for Ar) and 131 (for Xe). In Figure 57 the signal of the mass spectrometer is plotted versus the sample temperature. The Ar sputtered sample releases considerable amounts of Ar in several bursts, starting at temperatures around the melting point of the Au/Sn eutectic alloy of 551 K (trace Ar/Ar). We attribute these peaks to Ar bubbles bursting on the surface of the liquid film. The Xe sputtered film does not release a significant amount of gas in the investigated temperature range (trace Xe/Xe). Only some traces of Ar are detected that likely are expelled from the underlying titanium layer, which was prepared by Ar sputtering (trace Ar/Xe). For comparison the Xe signal of the Ar sputtered film is shown too (trace Xe/Ar).

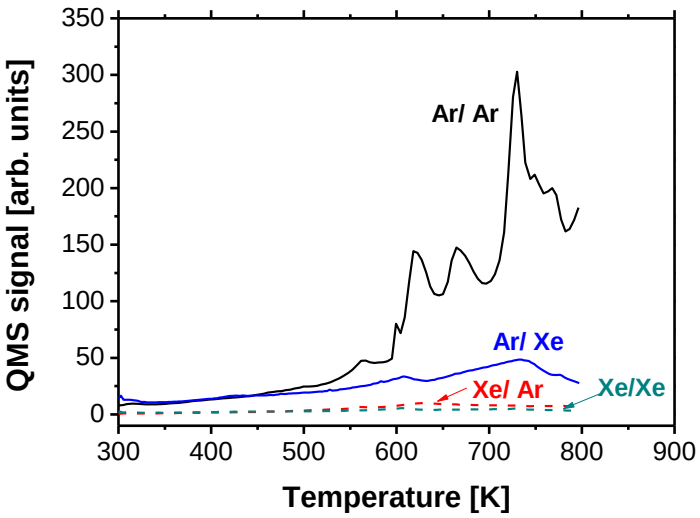

Figure 57: Quadrupole mass spectrometer signal vs. sample temperature for Au/Sn films sputtered with Ar and Xe as the discharge gas. Significant amounts of Ar are found only in the sample sputtered with Ar (trace Ar/Ar). Some traces of Ar in the sample sputtered with Xe stem from the titanium coating of the substrate (trace Ar/Xe). Xe desorption is negligible in either one of the samples (traces Xe/Ar, Xe/Xe). Courtesy of Walter Lukesch

Another consequence of the Ar incorporation is the increased wafer temperature during sputtering. Figure 58 shows the temperature measured at the center of the wafer with a pyrometer during sputtering of the Au/Sn films at a constant deposition rate of 2 nm/s. The temperature rises initially from the beginning of the deposition sequence until a radiative equilibrium with the surroundings is achieved. When Xe is used instead of Ar as the discharge gas, this equilibrium temperature is lower by 50 K. The wafer is mainly heated by the condensation, the kinetic energy of the metal atoms and the impact energy of the noble gas atoms that hit the surface. At a constant deposition rate of 2 nm/s, the power coming from the metal atoms is similar for Ar and Xe, but the reflected Xe atoms carry significantly less energy and therefore the wafer temperature reaches its thermal equilibrium at a lower value. Especially for the Au/Sn alloy which is deposited at temperatures close to its melting point this temperature difference has a major effect on the grain structure of the resulting film. The Xe sputtered film has initially finer grains than the Ar sputtered film (see Figure 56).

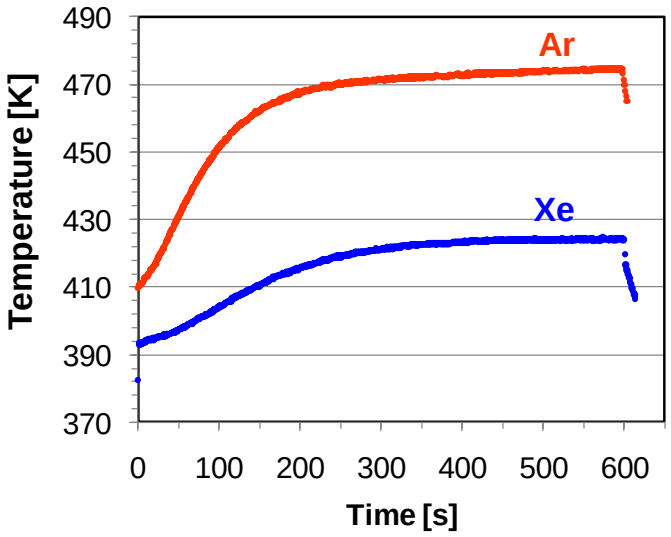

Figure 58: Temperature of the substrate wafer during sputtering at a constant deposition rate of 2 nm/s. The use of Xe instead of Ar as the discharge gas reduces the maximum temperature by 50 K.

3.2 Soldering

The experiment described in the previous paragraph was designed to simulate a diffusion soldering process as it is commonly applied in semiconductor packaging. In industry sputtering is used to deposit a thin layer of the eutectic Au/ 20wt.% Sn alloy on the backside of wafers, which serves as a filler material for soldering. [15] In this application, the Au/Sn film reacts with the metal of the lead frame to form intermetallic compounds. We find that voids are also formed under these conditions. The semiconductor chip is bonded on a metal lead frame for the purpose of mechanical stabilization, heat dissipation and current conduction. For die attachment, the die is pressed with its metallized backside on the preheated lead frame. The filler metal melts and fills the joint clearance. During the bonding, the filler and the metal of the lead frame mix and form intermetallic phases with higher melting points than the process temperature. This means that the joint is formed by isothermal solidification, having a remelt temperature much higher than the process temperature. The eutectic Au/Sn alloy is used because it has a low melting point of 551 K, is resistant to corrosion and forms ohmic contacts to silicon and GaAs. [16]

A typical failure mechanism for semiconductor devices is due to voids in the solder joint between die and substrate. A void is a gas filled volume that locally increases the thermal and electrical resistance between chip and package. It results in a hot spot in the chip area directly above it during the operation of the device. The heat generated by the power dissipated in the semiconductor above the void must flow laterally along the chip around the void, thus increasing the length of the thermal path. Even very small voids usually dominate the thermal resistance and can lead to a failure of the chip. [17]

For diffusion soldering, the wafer was cut in 0.3 by 0.3 mm dice with an industrial diamond saw. The silicon pieces were attached to a silver-plated copper lead frame using an Esec die bonder. The thickness of the Ag layer was 5 µm. During the bonding, the lead frame was heated to 613 K under a forming gas atmosphere. The die was pressed on the lead frame with a pressure of 1.5 MPa for 20 ms. After the bonding process, the assembly was kept under protective atmosphere while slowly cooling down to room temperature.

The die bonding process caused voids to form in the Ar sputtered films, which can be observed in the x-ray photograph of Figure 59a. In X-ray photography, the voids stand out as brighter non-absorbing areas, especially if the solder contains heavy elements like Au. The voids are even observable with optical microscopy. Figure 59b shows a cross-section of a solder joint made by embedding the samples in epoxy resin, grinding and polishing. The images of the Xe sputtered film show no evidence of voids either in the X-ray photograph (Figure 59c), or in the optical micrograph (Figure 59d).

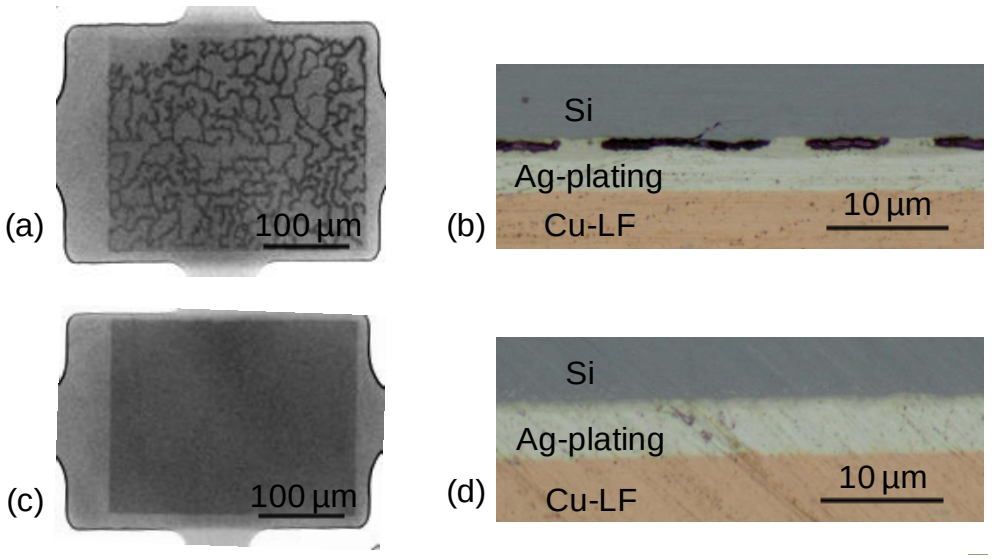

Figure 59: X-ray images (a,c) and optical micrographs of cross-sections (b,d) of the solder joints. The sample shown on top (a,b) was sputtered with Ar, the one at the bottom with Xe (c,d). The incorporated Ar in the filler material leads to significant voids in the joint. These can be seen as bright areas in the X-ray image (a) and as dark areas in the optical micrograph (b). The use of Xe as the discharge gas completely eliminates this effect.

3.3 Conclusion

It was shown by FIB cross sections that voids appear in sputtered Au/Sn film upon melting. When xenon was used as a sputter gas, no voids were observed. We presented an argument based on the conservation of energy and momentum to explain that the light argon atoms get implanted into the sputtered films while the heavier xenon atoms do not. Thermal desorption spectroscopy measurements and temperature measurements of the wafer during sputtering support the argument that xenon atoms do not get incorporated into the sputtered films.

Furthermore it is demonstrated that the voids also appear in diffusion soldered joints made with argon sputtered Au/Sn. This leads to considerable deterioration of semiconductor packages. These voids were observed in optical microscopy cross sections and x-ray photography. Also in this case the voids can be avoided by sputtering with xenon.

3.4 References

[1] G.L. Trigg, Encyclopedia of Applied Physics, The Classic Softcover Edition. 12 Volumes, Wiley-VCH, 2004.

[2] H.F. Winters, Gas Incorporation into Sputtered Films, J. Appl. Phys. 38 (1967) 3928.

[3] E.A. Fagen, R.S. Nowicki, R.W. Seguin, Effects of dc substrate bias on the properties of rf-sputtered amorphous germanium ditelluride films, J. Appl. Phys. 45 (1974) 50.

[4] W.W.Y. Lee, D. Oblas, Argon entrapment in metal films by dc triode sputtering, J. Appl. Phys. 46 (1975) 1728.

[5] D.W. Oblas, Determination of Argon in Thin Films by rf Spark-Source Mass Spectrography, J. Appl. Phys. 39 (1968) 6106.

[6] J.A. Thornton, J. Tabock, D.W. Hoffman, Internal stresses in metallic films deposited by cylindrical magnetron sputtering, Thin Solid Films. 64 (1979) 111–119.

[7] M. Schmid, W. Hebenstreit, P. Varga, S. Crampin, Quantum Wells and Electron Interference Phenomena in Al due to Subsurface Noble Gas Bubbles, Phys. Rev. Lett. 76 (1996) 2298.

[8] M. Schmid, S. Crampin, P. Varga, STM and STS of bulk electron scattering by subsurface objects, Journal of Electron Spectroscopy and Related Phenomena. 109 (2000) 71-84.

[9] K.A. Keller, E.L. Boyd, B.A. Calhoun, V.J. Folen, W. Gräper, et. al., Landolt-Bornstein: Numerical Data and Functional Relationships in Science and Technology-New Series, Springer, 1970.

[10] B. Window, G.L. Harding, Gas incorporation during ion-assisted deposition in bias sputtering, Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films. 11 (1993) 1447-1450.

[11] L.R. Shaginyan, M. Mišina, S. Kadlec, L. Jastrabík, A. Macková, V. Peřina, Mechanism of the film composition formation during magnetron sputtering of WTi, Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films. 19 (2001) 2554.

[12] R.E. Somekh, The thermalization of energetic atoms during the sputtering process, Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films. 2 (1984) 1285-1291.

[13] E. Fagen, Thermally stimulated argon release from amorphous alloy films, Materials Research Bulletin. 7 (1972) 279-284.

[14] H. Etschmaier, J. Novak, H. Eder, P. Hadley, Reaction dynamics of diffusion soldering with the eutectic Au-Sn alloy on copper and silver substrates, Intermetallics. 20 (2012) 87-92.

[15] B. Schwartz, Ohmic contacts to semiconductors, Electronics Division, Electrochemical Society, 1969.

[16] A. Yerman, J. Burgess, R. Carlson, C. Neugebauer, Hot Spots Caused by Voids and Cracks in the Chip Mountdown Medium in Power Semiconductor Packaging, IEEE Trans. Comp., Hybrids, Manufact. Technol. 6 (1983) 473-479.

4 Silver nano-paste metallization

In previous chapters adhesive bonding, soft soldering and diffusion soldering were described as technologies for the die attach. Another possible method for this process which has great potential is sintering. Sintering is already widely used in the manufacture of ceramics and metals for various applications ranging from turbine blades to dental implants, but so far it is not commonly applied for die attach. [1]

Generally, sintering is a processing technique to produce density controlled materials from metal or ceramic powders by applying heat and pressure. [2] It relies on solid state diffusion for mass transport to bond the microscopic particles together, resulting in significantly improved thermal, electrical and mechanical properties. Thus it offers an opportunity to form bonds below the melting temperature of interconnecting materials. The joint can be formed at mild processing temperatures and is still stable at higher operating temperatures, similar to diffusion soldering. Sintering has the further advantage that there is no liquid phase involved and thus the die cannot move on a liquid film, which enables an improvement of the placement accuracy.

4.1 Sintering

The sintering process can be divided into three stages, which in practice strongly overlap with each other. [3] In the first stage, an external force is applied that rearranges the particles by rotating and sliding them. This results in an overall shrinkage and an increase of the density. The contact of the particles improves and necks begin to form between them. The material transport necessary for the formation of necks can take place by diffusion, vapor transport, plastic flow or viscous flow. [4] The second stage begins when the neck radius has reached about have the particle size. The material can then be viewed as a bulk material with pores. The density is still low at this point and the pores are interconnected or continuous. The densification proceeds by a

reduction of the cross section of the pores. The final stage of sintering begins when the pores are pinched off from each other and become unstable. In this stage, the isolated pores are eliminated until the bulk density is reached. Here grain growth occurs by Oswald ripening, where larger grains increase in size at the expense of smaller grains.

The driving force for all these processes is the minimization of the free energy. Surfaces, interfaces and grain boundaries can be associated with energies depending on their curvature. Thus the energy of the system is minimized by eliminating these surfaces or reducing their curvature. Simply speaking, material is transported from high energy regions to low energy regions.

For a curved surface the additional chemical potential $\Delta\mu$ due to the curvature is given by

$$\Delta\mu = \gamma K V_m$$

where γ is surface energy, K is the curvature and V_m is the molar volume of the material. [5] The curvature is positive if the surface is convex and negative if it is concave. The difference of chemical potential between two surfaces of different curvature also causes a gradient in the vapor pressure above the interface P_K given by

$$P_K = P_0 e^{\Delta\mu \; k_B T}$$

where P_0 is the vapor pressure over a flat surface, k_B is the Boltzmann constant and T is the temperature. This means that atoms evaporate from regions of convex curvature and condense on concave regions to decrease the potential gradient and compact the material.

Another consequence of the difference in the chemical potential is that the material under a concave curvature is subjected to a tensile stress. [4] If this stress exceeds the yield strength of the material, microscopic viscous or plastic flow will set in.

Generally, the driving force for sintering increases with decreasing particle size as the curvature of the particles get larger. At particle sizes of several nanometers, the surface free energy dominates the total free energy of the system and the melting temperature of the particles is significantly reduced compared to the bulk melting point. Buffat et al. [6] have investigated this effect for gold particles. Particles with a diameter of 2 nm are liquid at room temperature, whereas the bulk material has a melting point of 1337 K.

Next to the particle size, the temperature is an important parameter for the sintering kinetics because all transport mechanisms are accelerated by elevated temperatures. The densification rate of the material can be approximated as the product of the driving force for sintering and the mobility, which is thermally activated.
Thus the best sintering result will be achieved from small particles at high temperatures.

4.2 Nanopaste formulation

Commonly used nanopastes that are suitable for stencil printing consist of nanoscale silver particles and organic components such as surfactants, binder and thinner.
To synthesize large quantities of nanoscale metal particles several techniques such as mechanical attrition, vapor deposition, and chemical precipitation have been developed. To prevent the particles from touching and agglomerating, surfactants are necessary. The surfactants have a polar acid function on one end and a hydrocarbon chain on the other. The polar acid group anchors to the hydrated silver particle surface and disperses them by a polymeric stabilization mechanism. [3] Typical surfactants include fatty acids, poly-diallyldimethylammonium chloride (PDDA), poly-acrylic acid (PAA), and polystyrene sulfonate (PSS). [4] To prevent cracks in the paste during printing or drying, a binder is added to the paste. The binder is a composite of polymers with long hydrocarbon chains such as simple wax, polyvinyl alcohol (PVA) or polyvinyl butyral (PVB). [1] Lastly a thinner is necessary to adjust the viscosity of the paste and make it suitable for printing. This can be a polymer with short hydrocarbon chains like texanol or terpineol. During the drying step at temperatures around 370 K, the thinner is evaporated from the paste, increasing its viscosity and stabilizing it on the substrate. In the sintering step at around 700 K the remaining organics are burned out and the silver particles agglomerate.
In this work, a hybrid Ag-nanopaste is used. This means that it does not solely rely on the sintering of the nano particles but also features an organic silver complex compound. This compound dissociates upon heating and acts as a silver source that supports the densification of the material.
Silver is chosen as it is the material with the best electrical conductivity and the second best thermal conductivity, only exceeded by diamond. Other noble metals like gold or platinum have

worse conductivity and are also much more expensive. Copper on the other hand is cheaper than silver but is also very reactive and readily oxidizes in air. This is a problem, especially if the particle size is so small and thus the reactive surface is greatly enlarged. The oxidation of copper is exothermal and fine copper powder can even be explosive.

The paste used in this work is commercially available from InkTec™ under the product name TEC-PA-020. It consists of silver nano particles (50 wt.%), an organic silver complex (45 wt.%), α-Terpineol as a thinner and PAA as a surfactant. The silver complex serves as a binder, and a silver source at same time. The Ag complex is synthesized by bonding an organic ligand, containing an amine group and a hydroxyl group with aliphatic silver carboxylate at an equivalent ratio of 2:1 (see Figure 60). The paste has excellent stability and is easily industrially applied.

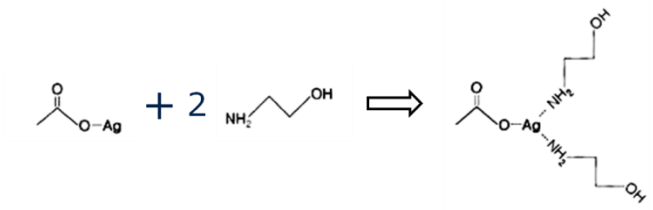

Figure 60: Syntheses of the organic silver complex for the hybrid silver nanopaste. Ag acetate and Ethanolamine form Ag(acetate)(ethanolamine)$_2$

4.3 Experimental and results

The die attach of regular semiconductor chips by sintering of nanoscale silver paste has been demonstrated successfully before. [1,4,7–9] The silver nanopaste is applied to the backside metallization of the chip and this stack is sintered on a metal substrate. In this work, we took the approach of leaving out the backside metallization completely and applying the Ag-paste directly to the silicon. Figure 61 shows a schematic of the assembly process.

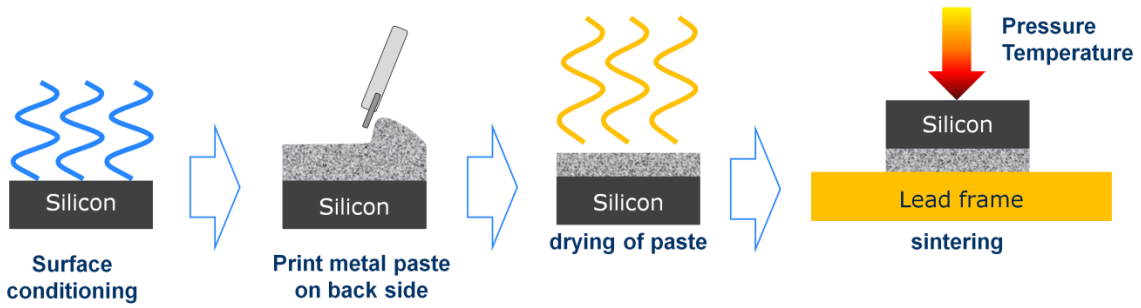

Figure 61: Schematic of the process for the backside metallization free die attach with Ag nanopaste. The surface of the silicon wafer is cleaned before the paste is printed and dried. After dicing the single dice are attached to a lead frame.

The primary purpose of a backside metallization is to form a good electrical and thermal contact to the silicon. It also has to provide a suitable surface for the interconnect material, e.g. it has to provide a wettable surface for soldering. Thus it often consists of multiple metal layers with silver as the uppermost metal to protect the surface from oxidation. This silver layer serves also as a perfect contact surface for the Ag-nanopaste.

The deposition of the wafer backside metallization is associated with large effort and costs, owing to the sophisticated tools and expensive raw materials. Furthermore the application of the metals is done at elevated temperatures and thus it introduces stress into the wafer as the metals have coefficients of thermal expansion different to that of silicon. This is a problem especially for the handling of thin wafers with thicknesses below 200 µm. The stress can bend the wafers to such an extent that they cannot be handled by standard production tools anymore.

The sintering of the silver nanopaste does not require a wettable surface, because the material is never in the liquid state. But still the interface between the silver paste and the silicon is critical. In theory silver forms an ohmic tunnel contact to highly doped silicon. In practice a clean interface is hard to achieve because of contaminations such as native oxide. Also the mechanical adhesion of the nanopaste to the smooth surface of a silicon wafer relies on a clean interface. Therefore several methods to condition the silicon surface were tested.

4.3.1 Surface conditioning

To investigate the mechanical adhesion of the nanopaste die attach, four standard 8 inch silicon dummy wafers with no electrical function were used. They were ground mechanically to a thickness of 200 µm. The damage introduced into the silicon crystal by this process can be removed chemically by isotropic etching. Using this so called "damage etch" either a flat surface can be produced or a microscopically rough surface. To obtain a smooth surface, one wafer was rinsed in a mixture of hydrofluoric acid, nitric acid, phosphoric acid, sulfuric acid and surfactants for 18 seconds. Thereby 10 µm of silicon were removed leaving a level and intact crystalline surface. On such a smooth surface it is difficult to achieve a good mechanical adhesion with a soft material. Therefore, the remaining three wafers were rough etched. To achieve a jagged surface, a similar etching solution was used but leaving out the phosphoric acid and the surfactants. This solution is thus more viscous and the gaseous hydrogen generated in the etching process cannot escape quickly enough from the liquid and agglomerates into bubbles on the surface, blocking the etching locally. This produces a crystalline surface with a roughness of about 2 µm root mean square.

As soon as the silicon is in contact with the atmosphere after the etching process, a layer of native oxide is formed on the surface. Therefore it has to be cleaned and passivated. Again there are several methods to achieve this. One of the rough etched wafers was dipped into hydrofluoric acid (50 %) for 10 seconds. This removes the oxides and terminates the open silicon bonds with fluorine, making the surface hydrophobic. This state of the surface is stable under atmospheric conditions for about 24 hours.

One rough and the smooth wafer were conditioned by plasma etching. Their surfaces were exposed to a hydrogen plasma for 30 seconds. This reduces the oxides present and also removes all organic contaminations. The open silicon bonds are terminated by hydrogen, making the surface hydrophilic.

The last remaining wafer was used as a reference and a standard backside metallization layer stack was sputtered on its backside. The uppermost metal layer to which the nanopaste was applied was silver.

The effects of all surface conditioning methods last only a limited time and therefore the printing of the nanopaste was done within 6 hours after the conditioning.

4.3.2 Nanopaste application

The hybrid nano silver paste was applied in an industrial DEK Horizon™ stencil printer. The wafers were positioned automatically under a stainless steel stencil. The stencil is 100 µm thick and has a round opening with a diameter of 196 mm. This covers an edge of 2mm of the wafer, which is necessary for handling. The paste was applied manually to the stencil and spread by a squeegee (see Figure 62). The squeegee consists of a pair of semi-round blades of which, depending on the movement direction, only one is pushed down on the stencil for printing. This way the printing can be done in both directions. The semi-round shape of the blades minimizes their bow over the diameter of the wafer and thus improves the thickness uniformity of the printed paste. Figure 63 shows a wafer directly after printing of the nanopaste. The paste was spread homogenously and has a shiny surface.

Right after printing the paste was dried in a belt furnace under nitrogen atmosphere at 378 K for two hours. Under these conditions, the thinner evaporates and the paste is fixed on the wafer. Figure 64 shows a SEM image of the paste in this state. The particle sizes range from 20 to 100 nm.

In this state the wafers were laminated with their nanopaste covered side onto a dicing foil and cut by a diamond blade into 2.7×3.6 mm^2 pieces.

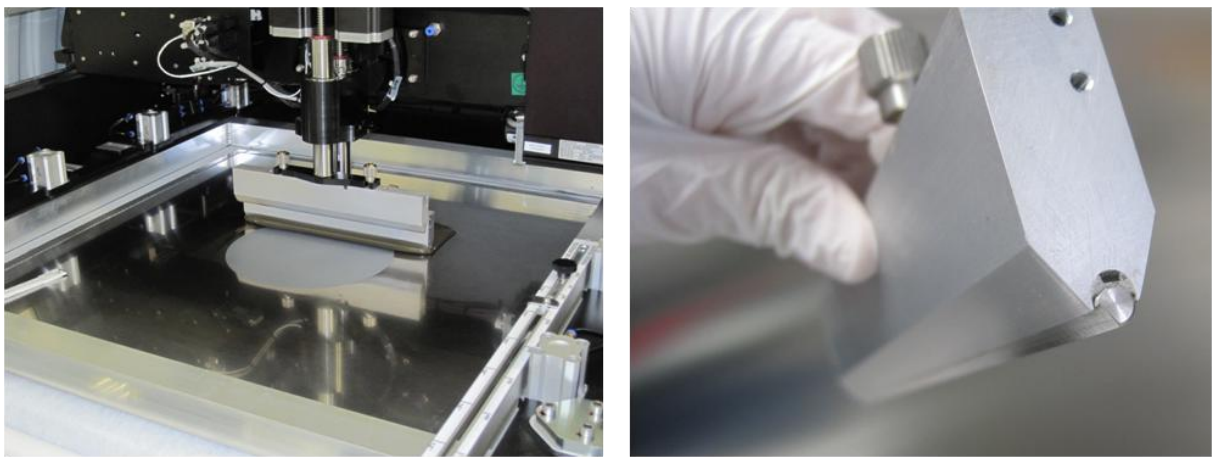

Figure 62: The nanopaste is applied in a DEK Horizon™ stencil printer (left). To minimize the bow over the wafer diameter the blades of the squeegee have a semi-round shape (right).

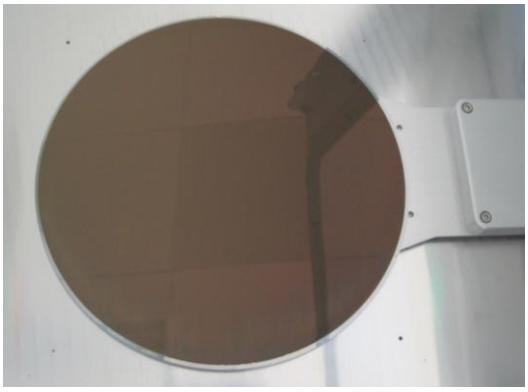

Figure 63: Ag nanopaste right after printing on a silicon wafer.

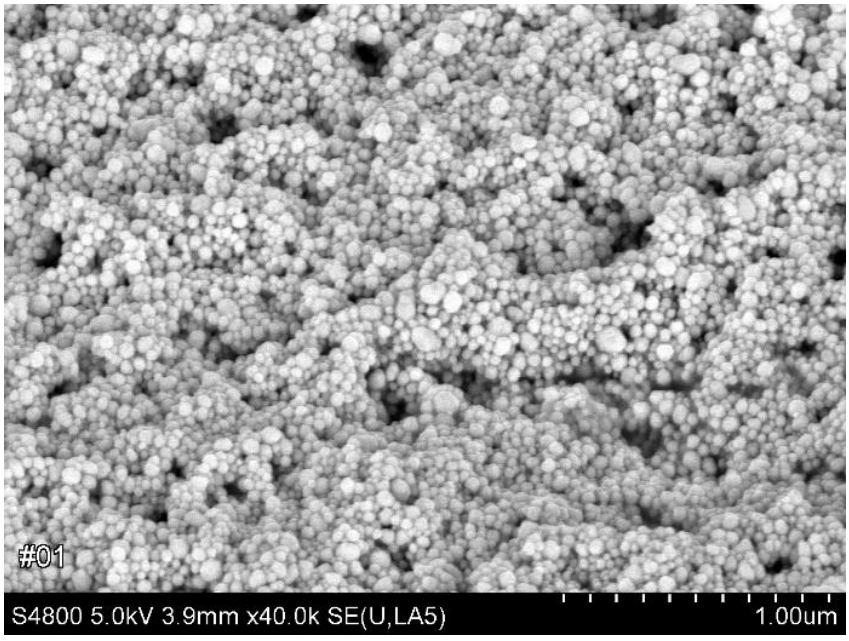

Figure 64: Ag nanopaste after drying. The size of the silver particles ranges from 20 to 100 nm.

4.3.3 Die attach

Direct Bonded Copper (DBC) which is commonly used in power modules, served as substrate for the die attach. These substrates are composed of a ceramic tile to which a sheet of copper is bonded on both sides, which makes them electrically insulating but at the same time an excellent thermal conductor. [10] The copper is bonded to the ceramic, usually aluminum oxide, by a high temperature oxidation process. The top copper layer is structured by etching to form an electrical circuit, whereas the bottom layer is kept plain. One of the main advantages of DBC is that its

coefficient of thermal expansion is close to that of silicon, which minimizes the stress on the die attach interconnect and the chip.

For sintering, the chips were placed manually on the substrate and a pressure of 0.2 MPa was applied by metal weights. The whole assembly was heated under nitrogen atmosphere in an oven to the sintering temperature and held for 30 minutes. The cooling was passive and it took several hours until the temperature was back to room temperature. Only then the substrates were removed from the protective atmosphere of the oven for testing.

Figure 65 shows a cross-section of such a joint. On top is the silicon chip with the roughly etched surface. The nanopaste has a sponge-like morphology, but is still very dense with only little empty volume between the silver. The sintered layer thickness was only about 20 µm compared to the 100 µm after printing, which means that it has shrunken by a factor of five. The soft paste deforms easily and compensates for the roughness of the lead frame. The pictures on the right of Figure 65 show details of the interfaces. On the critical interface towards the silicon some areas are not in close contact and some bright areas in the picture indicate silicon oxide.

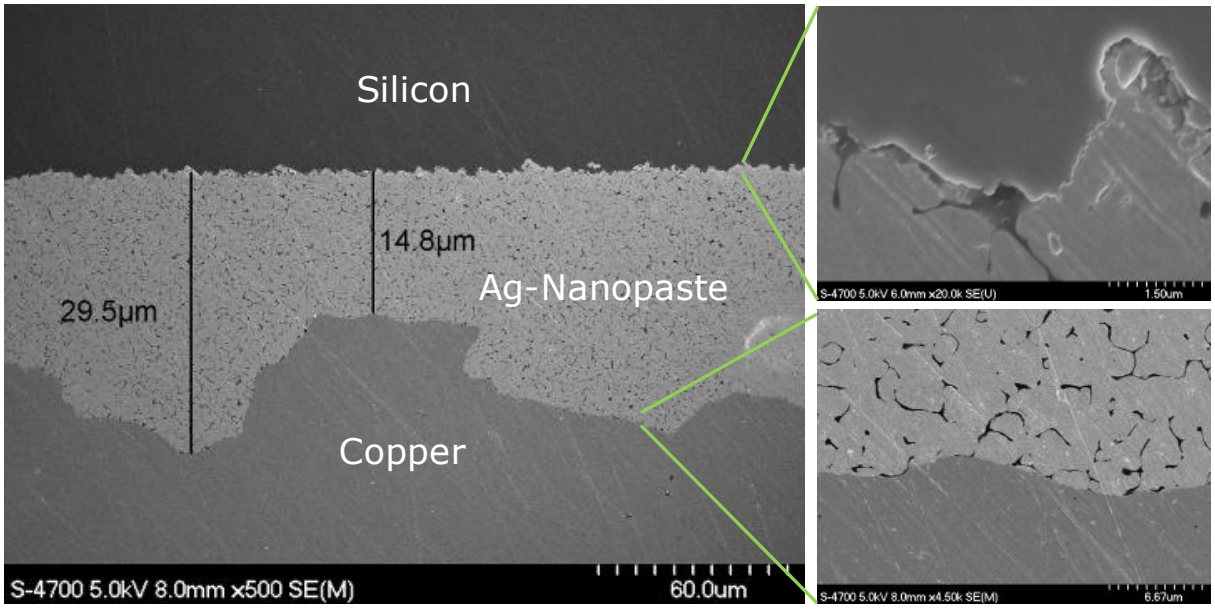

Figure 65: Cross-section of a joint made from sintered nanopaste. The sample was embedded with a tilt of 78° for a more detailed image. On top is the rough etched silicon of the chip, on the bottom the copper of the DBC and in between the sintered nanopaste. The paste has a sponge-like structure and compensates the roughness of the substrate very well. The layer thickness has shrunken form initially 100 µm after printing to about 20 µm after sintering. The picture on the top right is a magnification of the silicon – nanopaste interface, the one on the bottom right of the nanopaste – copper interface.

4.3.4 Mechanical characterization

Critical for a good die attach is the electrical and thermal conductivity as well as the strength of the mechanical adhesion. A requirement for a good thermal conductivity of the joint is a full contact without voids. Figure 66 shows a series of representative scanning acoustic microscopy (SAM) images of dice attached by nanopaste sintering at different temperatures. All chips shown have a rough silicon backside and were cleaned by hydrogen plasma. The other trial groups were also investigated by SAM, but are not shown here because the results are very similar for all of them. The images were recorded in transmission mode, which means that voids in the joint stand out as dark areas, as the sound is reflected at the open interfaces. Generally a good void free die attach was achieved for all sintering temperatures independent of the wafer backside treatment. In some cases voids were found for samples sintered at the highest tested temperature of 568 K.

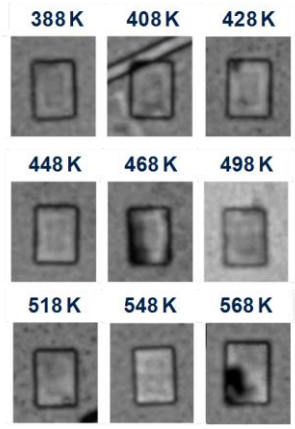

Figure 66: Transmission mode scanning acoustic micrographs of dice sintered at different temperatures with silver nanopaste on DBCs. In the bright areas of the image sound can pass unhindered through the sample indicating clean die attach. The dark spots indicate voids by which the sound is reflected.

To determine the mechanical strength, the die shear test is employed. A schematic of this test is shown in Figure 67. The die is subjected to a stress parallel to the plane of the substrate, which results in a shear stress between the two interfaces of the nanopaste. The force is increased until the joint fails. This value of the force divided by the area of the die is then recorded as the bond strength. To obtain reproducible values it is necessary that the edge of the die and the plane of the substrate are aligned parallel to the shear tool. This is achieved by enabling the specimen stage to have rotational freedom, which allows the sample to self-align with the tool. The testing for this work was done on a XYZTec Condor EZ ™ shear tester.

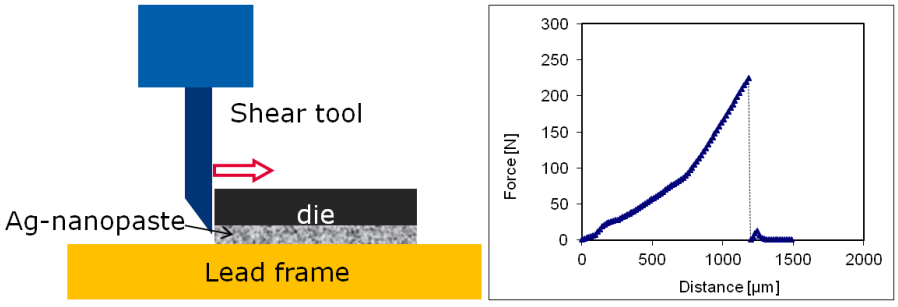

Figure 67: Schematic of the die shear test. An increasing force parallel to the plane of the substrate is applied to the die by a shear tool until the joint fails.

In Figure 68, the bond shear strength values are plotted for different surface conditioning methods and sintering temperatures. For all sintering temperatures, the reference group with the

backside metallization has the highest bond strength. The metallization free groups achieve only about half of the strength, independent of the method of surface conditioning. Nevertheless bond strength of more than 10 MPa at a process temperature of only 508 K are sufficient for most applications. Generally the bond strength increases with increasing sintering temperature due to the higher densification of the paste.

The mode of separation indicates the weakest link of the joint. For the metallization free dice, the fracture surface is in the majority of cases the interface between the paste and the silicon, whereas the metallized chips fracture in the nanopaste layer itself.

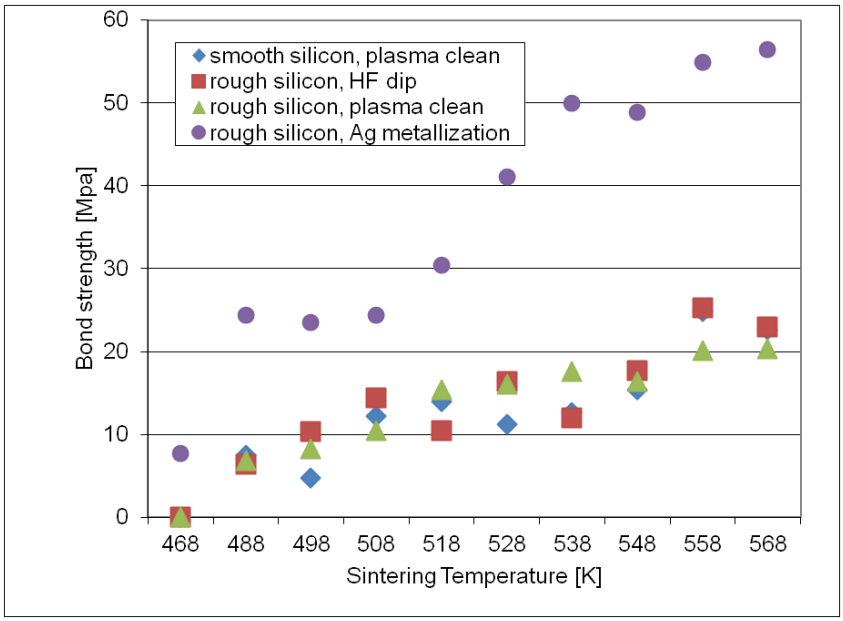

Figure 68: Bond shear strength for different sintering temperatures and surface conditioning methods. Every data point is the mean of ten tested dice. The highest shear strength is achieved by the reference with a Ag backside metallization. The metallization-less chips achieve only half the shear strength and do not differ much by the method of surface conditioning. There is also a trend of better adhesion for higher sintering temperatures.

4.3.5 Electrical characterization

To test the electrical conductivity of the nanopaste metallization, it was used for the die attach of a standard product, an Infineon OptiMOS™ power transistor. In the standard version of the transistor it has a sputtered backside metallization and is attached to the lead frame by

conductive adhesives. The electrical parameters of this product such as the resistance in the on-state are well known and serve as a reference for the performance achieved by the modified devices.

A highly phosphorous doped (10^{20} cm^{-3}) 8 inch silicon wafer serves as a base material for the transistors. The frontside of the prototype wafers, which contains the electrical circuits, was processed in the same way as standard wafers. On the backside the silicon was mechanically ground to a thickness of 200 µm and damaged etched to obtain a rough surface. After this process step, the wafers normally receive a sputtered backside metallization. The metallization was skipped for the prototype wafers and Ag-nanopaste was printed instead. The silicon surface was cleaned from oxides by hydrofluoric acid as described above. After printing a 100 µm thick layer of the paste, it was dried for 2 hours at 383 K under nitrogen atmosphere. Then it was sintered for 30 minutes at 533 K directly on the wafer. Subsequently the prototype wafer was processed like a standard product. Solder balls for the flip chip die attach were applied to the frontside, it was laminated on a dicing foil and the 3.25 × 2.54 mm^2 sized chips were singulated by a diamond blade. For packaging, the chips were mounted in the CanPAK™ package. It consists of a shallow metal trough as a lead frame to which the chip backside is attached by conductive adhesives (see chapter 1, Figure 19). The backside of the chip and thus the lead frame acts as the drain contact, whereas the source and gate contacts on the frontside are covered with solder balls for board assembly. For statistical reasons 560 chips with the nanopaste backside metallization were mounted in such a package. Figure 69 shows these devices as they are stored in a tape and reel spool, ready for assembly on the circuit board.

Figure 69: Infineon OptiMOS™ with Ag-nanopaste backside metallization in the CanPAK™ package. The devices are stored in a tape and reel spool.

The chips with the Ag-nanopaste metallization were fully functional so that they could be characterized by automated tools. Various parameters were determined for every chip. Among those is the resistance of the device in the on-state, at a gate voltage of +10V ($R_{DS,on\ 2}$). In the on-state of the transistor, most of the voltage drops across the drain contact, i.e. the backside metallization. Thus the $R_{DS,on\ 2}$ value reflects the contact resistance and the quality of the backside metallization. In Figure 70 representative IV-curves of three devices are plotted. The curves are strictly linear, indicating an ohmic tunneling contact between the silver and the highly doped silicon. The slope of the I-V curve is proportional to the resistance. The values of all 560 characterized devices are summarized in the histogram in Figure 71. The mean of the resistance is 53 mΩ with a standard deviation of 8 mΩ. The nanopaste has a specific resistance of only 5 µΩcm and thus its contribution to this value is negligible. The resistance is dominated by the contact resistance between the silicon and the nanopaste. At a chip size of 8.3 mm², the specific sheet resistance was 6.4 nΩ/m². The $R_{DS,on\ 2}$ value of the standard devices with a sputtered backside metallization is only 1.7 mΩ which is an order of magnitude lower.

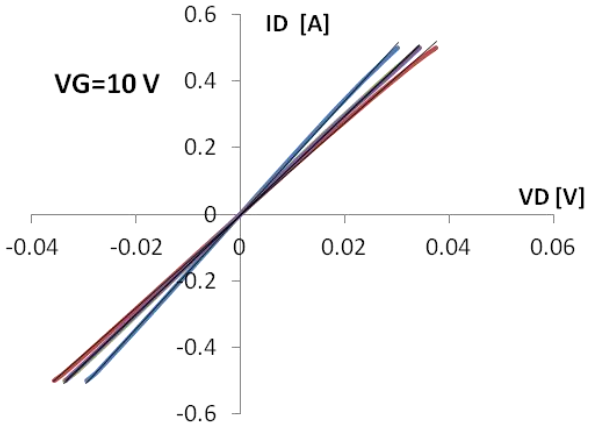

Figure 70: Drain current versus source-drain voltage of the packaged OptiMOS™ device in the on state at a constant gate voltage of +10V. The characteristic is strictly linear, indicating an ohmic contact.

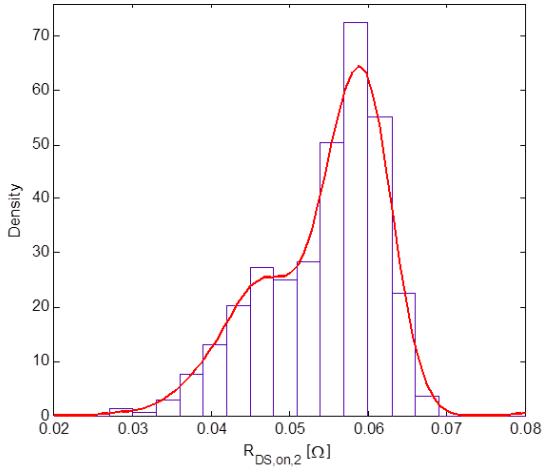

Figure 71: Distribution of the measured $R_{DS,on\ 2}$ values. The mean of the resistance is 54 mΩ with a standard deviation of 8 mΩ.

4.4 Conclusion and outlook

In this chapter the necessity of a backside metallization for a die attach with Ag-nanopaste was tested. It was shown that mechanically stable joints can be achieved by applying the paste directly onto the silicon. A bond strength of more than 20 MPa was achieved without any sputtered backside metallization. This is only half as good as for the metallized chips, bit still sufficient for a reliable die attach. Several methods of surface conditioning were tried but no significant influence on the bond strength was found.

The electrical contact of the nanopaste to the highly doped silicon is strictly ohmic, which is an important requirement for use in any semiconductor device. The resistance of an OptiMOS™ transistor in the on-state with a Ag-nanopaste backside coating was determined to be (54±8) mΩ, which is an order of magnitude higher than for the standard metallized devices.

A possible explanation for the ohmic characteristic and the high resistance of the contact is a partial coverage of the silicon surface with oxides or other contaminations. Before the application of the nanopaste the surface is properly cleaned. But due to the sponge-like morphology of the paste and its organic constituents, it is possible that the surface is contaminated afterwards and the area where there is a clean contact between silver and silicon is significantly reduced.

The good mechanical contact together with the weak electrical performance make this assembly method most suitable for devices which require a good thermal contact but do not carry large current, like logical ICs.

An application for power electronic devices might be realistic if the contact resistance could be reduced significantly. Further experiments could investigate the influence of the surface conditioning, sintering pressure or the type of doping of the base material. These investigations are beyond the scope of this thesis but might be treated in a specific technology development project.

4.5 References

[1] *Z. Zhang, Processing and Characterization of Micro-scale and Nanscale Silver Paste for Power Semiconductor Device Attachment, Virginia Polytechnic Institute and State University, 2005.*

[2] *S.-J.L. Kang, Sintering: densification, grain growth, and microstructure, Butterworth-Heinemann, 2005.*

[3] *M.N. Rahaman, Ceramic processing and sintering, M. Dekker, 2003.*

[4] *G. Bai, Low-temperature sintering of nanoscale silver paste for semiconductor device interconnection, Virginia Polytechnic Institute and State University, 2005.*

[5] *S.-J.L. Kang, Sintering: densification, grain growth, and microstructure, Butterworth-Heinemann, 2005.*

[6] *P. Buffat, J.-P. Borel, Size effect on the melting temperature of gold particles, Phys. Rev. A. 13 (1976) 2287.*

[7] *J.G. Bai, G.-Q. Lu, Thermomechanical Reliability of Low-Temperature Sintered Silver Die Attached SiC Power Device Assembly, IEEE Transactions on Device and Materials Reliability. 6 (2006) 436-441.*

[8] *J.G. Bai, J.N. Calata, G.-Q. Lu, Processing and Characterization of Nanosilver Pastes for Die-Attaching SiC Devices, IEEE Transactions on Electronics Packaging Manufacturing. 30 (2007) 241-245.*

[9] *G.Q. Lu, J.N. Calata, G. Lei, X. Chen, Low-temperature and Pressureless Sintering Technology for High-performance and High-temperature Interconnection of Semiconductor Devices, in: International Conference on Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems, 2007. EuroSime 2007, 2007: S. 1–5.*

[10] *P.C. Andricacos, Copper on-chip interconnections, The Electrochemical Society Interface. (1999) 32–37.*

5 Conclusion

The die attach is only one of many processes involved in the production of semiconductor devices, but still its quality and reliability are crucial for the whole device. The technological advances in microelectronics processing as well as governmental regulations demand innovative new technologies that can satisfy the changed requirements for packaging. The content of this thesis is the investigation and development of these technologies.

One of the most promising approaches is diffusion soldering. This technology uses a few micrometer thick layer of a filler metal that is deposited directly on the backside of the wafer. During the die attach, the filler and the substrate diffuse into each other forming intermetallic phases with higher melting points than the process temperature. This means that the joint is formed by isothermal solidification, having a remelt temperature much higher than the process temperature.

As for most novel technologies, the processes involved are generally not fully understood which leads to problems in process design and high volume production. In this work various methods of characterization like in-situ X-ray diffraction, focused ion beam microscopy, and scanning acoustic microscopy were used to gain insight in the underlying principles of diffusion soldering. The most common material systems are based on the eutectic Au/Sn alloy in combination with nickel, silver, or bare copper substrates. The eutectic Au/Sn alloy consists of two different intermetallic phases: the ζ' and the δ phase. Nickel and silver react only with the tin-rich δ phase forming a binary tin phase and additional δ phase. Copper on the other hand forms a ternary compound with gold and tin. Additionally the potentially low cost system of pure tin on copper, which is novel to diffusion soldering in semiconductor manufacturing, was investigated. In this case at first a tin-rich binary compound is formed, which is then upon further annealing transformed into a copper-rich compound.

Generally it was found that the speed of the soldering reaction is not limited by diffusion but rather by the kinetics of the reaction itself. This means that the time it takes for the joint to be completely transformed into the stable intermetallic compound is directly proportional to the thickness of the solder layer. The temperature dependence of the reaction rate can be described by an Arrhenius equation, for which the activation energies were determined for all investigated material systems. This enables an extrapolation of the measured rates to arbitrary temperatures and thus a specific choice of the process parameters. At standard process temperatures the reaction completion time is in the range of seconds to minutes and will be completed after the short time interval of several hundred microseconds in which the chip is pressed onto the lead frame.

Metal layers of the copper/tin system which have been deposited electrochemically or sputtered differ significantly in terms of their grain structure, intermetallic phase composition and crystallographic orientation. For the electroplated layer stack an “aging effect” was observed. The formation of the Cu/Sn η-phase progresses at room temperature at such a rate that six weeks after the deposition no void free die attach can be achieved anymore. By introducing an annealing step right after deposition, the formation of the ε-phase is promoted. This slows down the interdiffusion and increases the storage time of the devices.

For the material system based on the eutectic Au/Sn solder, a different effect detrimental to the quality of the solder joint was investigated. During sputtering, the discharge gas argon is incorporated in the growing film. When the material is melted during soldering, the argon agglomerates into bubbles which affect the properties of the solder joint negatively. The gas incorporation is caused by an inefficient transfer of energy from the light argon atoms to the heavy gold atoms upon elastic collision. The reflected argon atoms retain enough energy to penetrate the sputtered film and get implanted. By using xenon instead of argon as a discharge gas the gas incorporation can be avoided because xenon has a mass more similar to gold and the energy transfer is more efficient. This was shown in thermodesorption measurements and X-ray microscopy of solder joints.

An alternative to diffusion soldering is the sintering of silver nanoparticles. The sintered nanoparticles form interconnects at low temperatures without the transition to a liquid phase or the necessity of a wafer backside metallization. The achieved mechanical adhesion of metallization

free dice is only half as strong as for metallized reference samples, but still sufficient for most applications. The electrical conductivity of the reference group is lower by an order of magnitude. This can be attributed to the contact resistance between silicon and silver. Still the current-voltage characteristics are linear which indicates an ohmic tunnel contact. These results make this backside metallization-free die attach seem unsuitable for the die attach of power devices but it may find applications with logic chips, which do not require such high electrical conductivities.

The results documented in this thesis contribute to a better understanding of the principles and mechanisms involved in the die attach, a process of elementary importance to the fabrication of efficient and reliable semiconductor power devices.

Deutsche Fassung:
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Genehmigung des Senates am 1.12.2008

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