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A high efficiency modular wide input voltage range power supply

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AFFIDAVIT

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Abstract

The ever increasing number of data centers require huge amounts of electrical energy and the part of renewable energy sources in their energy mix is usually only a fraction of the total power consumption, requiring a lot of additional combustion or nuclear power plants. This increases further the carbon-dioxide pollution and with that the global warming problem and problematic waste where until today no solution for final storage was found. Additionally for big data centers in order to maximize their revenue with the increase in energy costs new designs for data centers aim to reduce the energy consumption. This can be achieved by powering down servers if the capacity is not needed at the moment and/or by increasing the efficiency of the supply chain from the mains to the servers, where one part is the conversion from a high AC voltage to a low DC voltage. Different standards around the world evolved over the last century about the attributes of the mains like the amplitude and frequency and today it is required that a modern Switched Mode Power Supply (SMPS) is compatible with all the different possible configurations. One way of distinguishing SMPS is to set efficiency and power factor requirements over the load range, which is done by the 80plus organization. They set up different requirements and publish the measured test results making the choice easier for customers. Due to the varying voltage of the mains ranging from 110 to 230 volts, for both, low and high line mains, separate categories for the classifications by the 80plus organization exist, where the requirements for high line can be stricter since for supplying the same amount of power only half the current is needed compared to low line, lowering the conduction loss at high line.

The aim of this thesis is to experimentally prove a new modular approach for a typical SMPS targeted for servers which can achieve the titanium certification by the 80plus organization and which enables independent of high or low line equal efficiencies. The key idea behind the solution is the utilization of low voltage MOSFETs by splitting the input voltage with a capacitively voltage divider if required. Therefore with this approach the input voltage for each module is independent of the line voltage, which is possible by either connecting the individual modules in series or in parallel. Further offer low voltage MOSFETs compared to high voltage MOSFETs a much better Figure of Merits (FOM). For the AC/DC conversion a Triangular Current Mode (TCM) Power Factor Correction (PFC) and for the further high voltage to low voltage DC/DC conversion the well known Phase Shifted Zero Voltage Switched (PS-ZVS) full bridge with a center tap configuration on the output was chosen, which both will be explained in detail. The results from simulation together with additional calculations for the non-simulated losses in the magnetic, capacitive and semiconductors obtained efficiency curve over the load was then compared with the measured results from the prototype. Additionally relevant waveforms and thermal images of the prototype will be presented.

Kurzfassung

Die immer höher werdende Zahl an Datenzentren benötigen riesige Mengen an elektrischer Energie und der Anteil an erneuerbaren Energien in ihren Energiemix beträgt für gewöhnlich nur einen Bruchteil ihrer verbrauchten Energie, was dazu führt, dass ein großer Anteil an zusätzlichen kalorischen oder nuklearen Kraftwerken notwendig ist, wobei die ersten durch den Kohlendioxid-Ausstoß die Klimaerwärmung weiter vorantreiben und die zweiten problematischen radioaktiven Müll produzieren, wofür bis heute noch keine Lösung zur Endlagerung gefunden wurde. Zusätzlich um für große Datenzentren die Erlöse und über einen längeren Zeitraum zu maximieren müssen die stetig steigenden Energiekosten in neuen Planungen für Datenzentren berücksichtigt werden, welche zukünftig eine immer größere Rolle spielen werden. Das Ziel neuer Planungen ist oft den Energieverbrauch zu reduzieren, was zum Beispiel einerseits durch das Abschalten von Servern, wenn ihre Rechenleistung nicht benötigt wird und andererseits durch eine Erhöhung der Effizienz in der Versorgungskette erreicht werden kann, wobei ein Teil der Versorgungskette die Umwandlung einer hohen Wechselspannung in eine niedrige Gleichspannung umfasst. Unterschiedliche Normen bildeten sich auf der gesamten Welt im letzten Jahrhundert in Bezug auf die Eigenschaften der Netzspannung, wie die Amplitude oder der Frequenz aus und dadurch ist es heutzutage notwendig, dass ein modernes Schaltnetzteil mit allen Konfigurationen aus Netzspannung und Netzfrequenz kompatibel ist. Um Schaltnetzteile zu unterscheiden wurden Kriterien bezüglich des erreichten Leistungsfaktors und der Effizienz über den gesamten Lastbereich von der 80plus Organisation eingeführt. Die 80plus Organisation stellt die Ergebnisse der geprüften Schaltnetzteile anschließend öffentlich zur Verfügung um die Wahl eines geeigneten Schaltnetzteils zu erleichtern. Aufgrund der unterschiedlichen Netzspannung von 110 bis 230 Volt in unterschiedlichen Teilen der Welt gibt es für beide Kategorien eigene Klassifizierungen für das erreichte Effizienzlevel, wobei die Kriterien bezüglich Effizienz für eine hohe Netzspannung strenger sein können, da für die gleiche gelieferte Leistung bei doppelter Eingangsspannung nur der halbe Strom notwendig ist, was die Leitungsverluste begünstigt.

Das Ziel dieser Dissertation ist die experimentelle Verifikation eines neuen modularen Konzepts für ein für Server typisch verwendetes Schaltnetzteil, welches die Titanium Zertifizierung der 80plus Organisation erreicht und welches unabhängig von der Netzspannung die gleiche Effizienz aufweisen kann. Die Schlüsselidee dahinter ist die Verwendung von Niederspannungs-MOSFETs indem die Eingangsspannung falls erforderlich mittels eines kapazitiven Spannungsteilers geteilt wird. Indem die Module entweder seriell bei hoher Netzspannung oder parallel bei niedriger Netzspannung betrieben werden ist die Eingangsspannung für jedes Modul unabhängig von der Netzspannung. Weiter zeichnen sich Niederspannungs-MOSFETs gegenüber den üblich verwendeten Hochspannungs-

MOSFETs durch eine bessere Gütezahl aus. Für die Umwandlung von Wechselspannung auf die hohe Zwischenkreisspannung wird eine TCM Leistungsfaktorstufe und für die Umwandlung der hohen auf eine niedrige Gleichspannung wird ein pulsweitenmodulierter Gleichspannungswandler mit Mittelanzapfung auf der Sekundärseite verwendet, welche beide erklärt werden. Die durch Simulationen gemeinsam mit zusätzlichen Berechnungen für die nicht-simulierten Verluste in den magnetischen, kapazitiven und Leistungshalbleiterelementen erlangte Effizienzkurve wird anschließend zur Verifizierung der Simulationsergebnisse mit Messergebnissen des Prototyps verglichen. Zusätzlich werden relevante Zeitsignale und thermische Bilder des Prototyps vorgestellt.

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Introduction

1.1 Motivation

High efficient power conversion is first a step for a sustainable future decreasing the necessary power plant count and with that greenhouse gases or nuclear waste and secondly a step for decreasing the increasing energy costs in data centers, which account for a huge part of the running costs and creating a new research area about designing cost-optimal data centers as for example shown in [1–3], where energy consumption plays an important role. The Natural Resources Defense Council (NRDC) claim in a paper that the electricity consumption in the year 2013 of data centers alone in the U.S. was estimated with 91 billion (10^9) kilowatt-hours, which is the equivalent of 34 large (500 MW) power plants and that the consumption should increase to 140 billion kilowatt-hours by 2020, an equivalent of 50 power plants, causing costs of 13 billion dollars a year for the electricity bills and causing a pollution 150 million tons of carbon annually, [4]. In [5] the energy consumption of a data center was categorized into a demand side, which includes the server, storage, communication and other IT systems, and a supply side, which has to deliver the power for the demand side, including cooling, UPS, MV transformer and so on. Their investigation concluded that the demand side accounts for 52 percent of the total power consumption versus 48 percent for the supply side. They show that through the cascading effect in case of 1 W of less power used on the demand side on the server component level (processor, memory, hard disk, etc.) saves in total 2.84 W of power, see Fig. 1.1. Since the AC/DC and the DC/DC conversion is the first thing in the chain after the server and handled by a SMPS, optimization of the efficiency there leads to greater overall savings due to the cascade effect, which is stated to be at twelve percent in [5] if no further action to save power is taken.

The 80 plus initiative [6] defines efficiency requirements for computer and server power supplies, which must have an efficiency above 80% for different load points and a power

factor above 0.9 at full load. Later this requirement got expanded with higher efficiency criteria and an even stricter power factor which must also be achieved at lower load points. The efficiency is a simple measurement from the measured output power divided by the measured input power. The missing power on the output is dissipated as heat, generating additional cooling costs which leads to at least double the amount of dissipated energy in server farms. With the decreasing semiconductor and server costs, energy cost is an increasing factor which contributes to the overall costs of an office or data center. A more efficient power supply therefore reduces noise due to less required cooling, increases reliability and reduces cost. A high power factor enables the supply to draw the maximum possible power from the grid minimizing as well the peak current, which is favorable for uninterruptible power supplies, lowering the maximum load. Approved supplies by the 80 plus initiative are public available listed with the achieved efficiency certification and the measurement protocol, where the efficiency certification can reach from just 80 plus certified to bronze, silver, gold, platinum and to the latest and currently highest titanium. To reach high efficiencies with traditional and well known silicon devices a soft switching topology is a must. Also to satisfy the engineer standards the power supply must fulfill some standards concerning Electromagnetic Interference (EMI). The motivation of the thesis is to design a power supply for computer or server with 1 kW of output power and an output voltage of 12 V, which are typical values of server power supplies. The main focus of the design and thesis was to achieve titanium level efficiency for the high line input criteria, introduced by the 80 plus initiative [6], for low and as well for high line input by the utilization of low voltage MOSFETs like the OptiMOS which have a better FOM than the usually used high voltage MOSFETs which is possible by a division of the line voltage with a capacitive voltage divider if needed and parallel/serial connection of modules. Fig. 1.2 visualizes the required efficiencies to receive titanium level for low and for high line. The requirements for low line are a bit lower due to the inevitable higher conduction losses at low line (higher current needed). Nevertheless for the thesis the goal was to reach the stricter high line efficiency independent of the present mains voltage.

1.2 Overview of currently available solutions

At this time there are already several power supplies listed at 80 plus which fulfill the titanium requirements for high line or for low line. But from all the listed power supplies none can achieve the high line titanium criteria at low line. The tripping point was always at 50% load with the required efficiency of 96%. The very best listed power supply for low line is currently from Super Flower with the name *SF-1300F14MT* achieving an extremely high efficiency of 95.03% at 50% load which is the only point where it has a lower efficiency than required to match the titanium high line criteria. Further, a closer look by disassembling

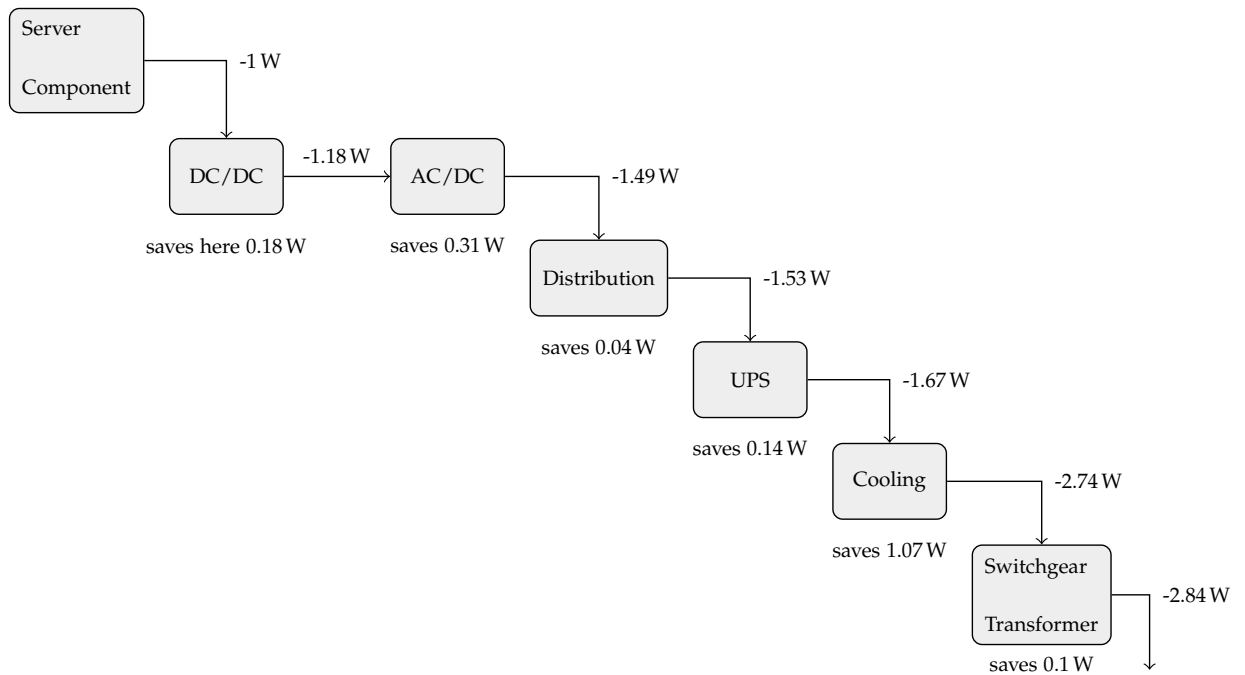


Figure 1.1: The cascade effect showing that a saving of 1 W at the server component side saves in total 2.84 W, [5].

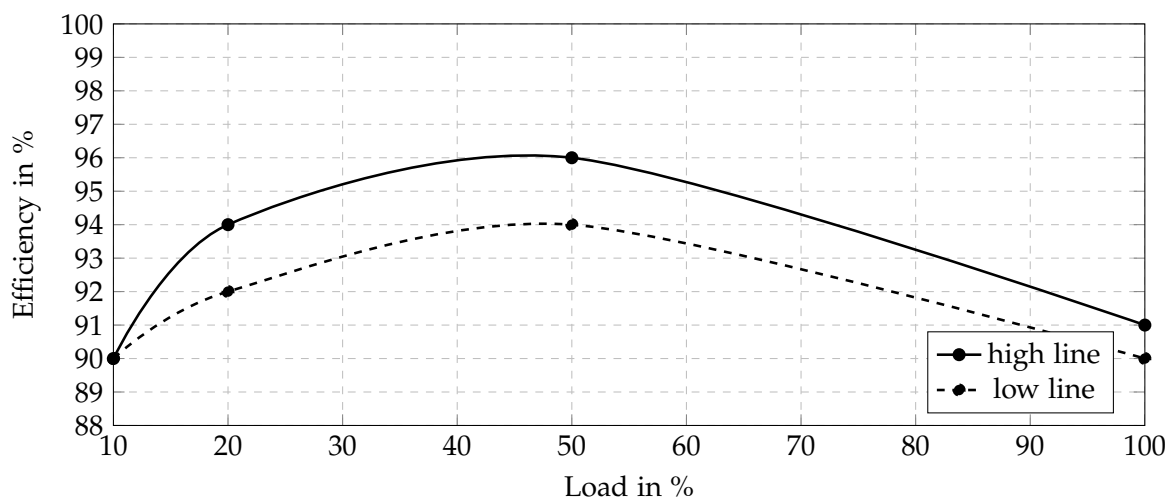


Figure 1.2: 80 plus efficiency requirements for titanium certification (black, solid) high line requirement; (black, dashed) low line requirement.

this power supply revealed that the DC/DC conversion is most likely handled by an LLC converter, which implies a relative complicated control. It is conceivable that by utilization of the here proposed solution to enable the use of low voltage MOSFETs with an LLC converter would show even better results, probably exceeding the high line criteria and opening the way for a new efficiency category.

Investigations for the PFC revealed that the bridgeless totem-pole version can achieve the highest efficiencies. In [7] a bridgeless or also double boost PFC in Continuous Conduction Mode (CCM) mode achieved an impressive efficiency of 99.1% for high line input at full load with traditional silicon devices and Silicone Carbide (SiC) boost diodes at a power density of 1.1 kW/dm^3 . A similar approach was presented by the company transphorm with new wide bandgap Gallium Nitride (GaN) devices, also operating in CCM at high line with boost diodes showing a peak efficiency of 98.56%. By replacing the boost diodes with GaN switches, their efficiency peaked at 99.00%, [8]. In [7, 9] another prototype for the PFC is presented, where the boost diodes are replaced with silicon MOSFETs which is then known under totem-pole PFC and the rectifier is running in TCM mode, which received its name from the shape of the current waveform, where a six phase prototype achieves a world record peak efficiency of 99.23% for high line input at 1.1 kW/dm^3 . Increasing the power density for the same type of PFC with an efficiency of 98.3% and a power density of 5.6 kW/dm^3 shows the trade-off between efficiency and power density. The prototype presented in this thesis has an overall power density for the whole SMPS of 1 kW/dm^3 . The PFC and the following DC/DC converter require about the same space. The here proposed TCM PFC rectifier achieves a maximum efficiency of 99.07% at 2 kW/dm^3 .

For the DC/DC converter again in [7] a PS-ZVS bridge achieving an efficiency of 98.5% and a power density of 3.3 kW/dm^3 is presented where the output voltage was for telecom with 48 V. Another highly efficient telecom DC/DC converter, utilizing a PS-ZVS bridge is presented in [10], presenting an efficiency at 50% load of 99.2% with a power density of 2.2 kW/dm^3 . In [11] again a PS-ZVS rectifier, this time with current doubler for secondary rectification and optimized for power density, a peak efficiency of 94.75% paired with a power density of 9 kW/dm^3 is presented. If instead of a PS-ZVS bridge an LLC converter with GaN devices is used, high efficiencies of 95.4% at 1 MHz switching frequency with a power density of 50 kW/dm^3 are achievable, [12, 13]. The PS-ZVS bridge used in this prototype peaks with an efficiency of 97% at 80% of the maximum rated load with a power density of 2 kW/dm^3 .

It looks like the latest research has picked up on the modular converter approach, to exploit the better FOM of low voltage MOSFETs for instance presented in [14–16], where a SMPS for telecom with a peak efficiency of 98% is presented paired with a power density

of 2.2 kW/dm^3 . These are outstanding results, showing that by division of a high input voltage to utilize low voltage devices can boost the efficiency even by shifting the silicon limit without necessarily using next generation wide bandgap devices.

A new idea which may be more common in the future is to convert the energy for a complete data center from AC to DC and then distributing the energy in the data center over DC buses, saving on conversion steps and increasing the efficiency. Here again several ideas exist, like a low voltage DC-distribution with 48 V on rack-level by Emerson, [17]. This solution has the advantage of higher reliability since the servers can be connected directly to the backup battery and fewer conversion steps than in a traditional data center are required but it has the disadvantage that the AC/DC conversion must be close to the point of use, else thick copper wires would be necessary. With that solution an increase in overall efficiency can be expected. Increasing the DC voltage to higher levels of 400 V throughout the whole facility decreases the required amount of copper for low cable losses and has the advantage that already available designs which convert 400 V DC to a lower DC voltage of 12 V, which is a typical value for the DC-link voltage in present SMPS, can be used. In [18] it is claimed that with a high voltage DC bus through the whole facility highest efficiencies are possible. They also propose to connect the backup batteries directly to the high voltage DC bus, which results in an increased reliability. By comparison of a traditional solution with the AC/DC conversion directly at the server versus the new approach of a high voltage DC bus facility wide they showed that 7% of energy can be saved. A disadvantage of all the presented DC distribution solutions is the requirement of DC circuit breakers instead of AC circuit breakers. Nevertheless the principal design of big data centers might change to a high voltage DC distribution in the future opening new research areas.

1.3 New contributions

The thesis presents a new idea with experimental verification of a demonstrator for the utilization of low voltage MOSFETs by dividing the mains voltage if necessary. Depending on the present mains voltage the modules can be connected in serial or in parallel with the result that the input voltage for each module becomes independent of the mains voltage. This makes it possible that the MOSFETs always operate in a optimal region of their maximum possible blocking voltage and further the advantages of low voltages MOSFETs compared to high voltage MOSFETs can be exploited, opening the way for highly efficient power supplies with traditional silicon devices without the need for wide bandgap devices. For dividing the mains voltage and balancing the input voltages for each module a new control concept is presented, which can be extended if necessary for multiple modules. Further, the

possibility of achieving titanium certification with a traditional PS-ZVS bridge for DC/DC conversion is shown and that more sophisticated converter like for instance LLC converter or expensive and still not widely available wide bandgap devices are not required. This new concept would also work with new wide bandgap devices, especially GaN devices look promising for the future which might further increase the overall efficiency.

1.4 Overview of the thesis

The first chapter of the thesis will give a quick introduction to the basic knowledge required to build a SMPS and finally the new idea with the prototype is presented.

Chapter 1 covers the motivation behind the thesis and the goal of the thesis with the required specifications. Additionally state-of-the-art solutions which already exist are presented.

Chapter 2 gives a basic introduction to the two most common used semiconductor devices for SMPS, the power diode and the power MOSFET. Later in the chapter a short introduction to charge compensated devices and how they work is given, since they changed power electronics significantly in the past years.

Chapter 3 presents an overview of typical AC/DC and DC/DC conversion topologies and covers the advantages and disadvantages for each presented topology. The need for a PFC, a EMI filter and soft switching is further explained.

Chapter 4 envelopes the control concept of the PFC and the PS-ZVS bridge with a detailed explanation of their operation. Simulation results are then compared with measured results from the prototype, validating the idea and the simulations.

Chapter 5 gives a quick summary with a conclusion about the work and possible future research topics.

The appendix lastly shows how extra losses, which were not possible to simulate, were calculated to make the results more precise. These extra losses cover the core losses in magnetics, the skin and proximity effect in the wires of the magnetics, additional losses in real capacitors and switching losses in MOSFETs.



Semiconductor basics

This section provides a quick introduction about semiconductor devices which are nowadays used in typical SMPS covering the attributes of power diodes and MOSFETs and in the following as well the charge compensation principle. Section 2.1 describes the basics about power diodes, section 2.2 the basic about the most common used switch in SMPS the MOSFET and section 2.2.1 describes the basics of the charge compensation principle, which broke the limit of silicon and enabled converters with higher efficiency and power density since they were made available for the mass market. It also presents how a comparison between MOSFETs by comparing FOM is possible in section 2.2.2 and shows the differences of conventional grown high voltage MOSFETs (above 600 V) with lower voltage devices, typically produced in trench technology.

2.1 Power Diodes

A power diode is the simplest semiconductor device with only two terminals, the anode noted with A and the cathode noted with C in Fig. 2.1. The characteristic of a power diode is the same as of a traditional diode, conducting when forward biased with a small forward voltage drop U_F of around 1 V due to the potential barrier from the charge distribution in proximity of the junction and other effects, [19], or if the diode is reverse biased it blocks and only a small current is flowing through the diode in reverse direction, called the leakage current. Therefore it can be categorized as an uncontrolled switch working only in one quadrant, where the state of the diode, conducting or blocking, is determined by the applied voltage only. If the applied reverse voltage is increased further to the reverse breakdown voltage the device breaks down and a large current can flow again, see Fig. 2.2, leading typically to a thermal destruction of the device.

The most important DC properties of the diode are the *forward voltage drop* U_F occurring when forward biased between the anode and the cathode, the *breakdown voltage* U_{BD} ,

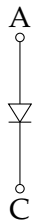


Figure 2.1: Symbol for a diode.

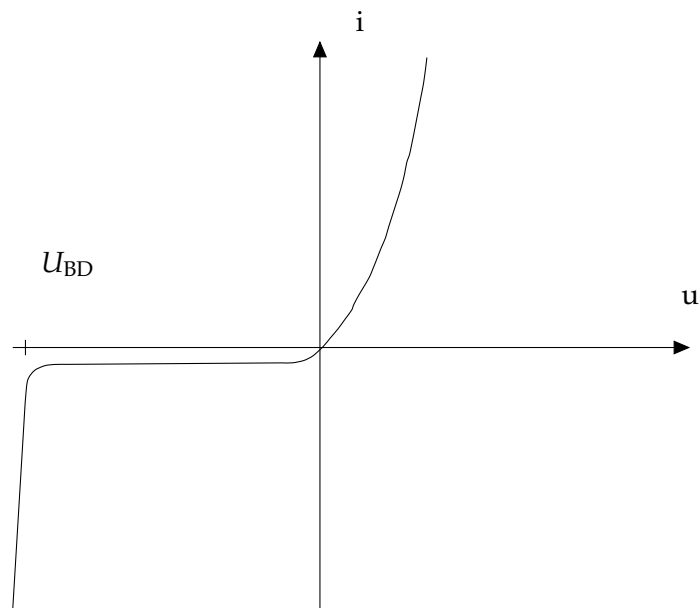


Figure 2.2: Static characteristic of a diode, [20].

defining the maximum allowed reverse voltage before the avalanche effect occurs, and the *reverse current*, which is flowing if the diode is under reverse bias and the reverse voltage is lower than the breakdown voltage.

The most important AC parameters of power diodes are the *forward recovery time* t_{FR} , which is the required time the forward voltage drops to a defined level after a forward current started flowing and the more important *reverse recovery time* t_{rr} , which is the time the diode requires after the transition from being forward biased to reverse biased before the diode regains its blocking capability.

In typical applications diodes are often used for the *rectification of an AC voltage*, either directly connected to the grid with a full bridge rectifier or after a transformer. Another area of application is for *voltage clamping* used in snubber or other protection circuits, which is often needed in switch mode power supplies. [19]

Taking a closer look at the semiconductor physics of a silicon power diode shows that a power diode consists of a p-doped layer, a low doped n layer and then a high doped n layer, they are often called Positive intrinsic Negative diode (PiN-diode), forming a so called abrupt p-n junction, where the impurity concentration changes abruptly from acceptor impurities N_A to donor impurities N_D . In case of the PiN-diode diode, where $N_A \gg N_D$ it is more precise called a one-sided abrupt junction. The breakdown voltage depends on the construction of the diode which is shown in Fig. 2.3. For higher blocking voltages the peak value for the electrical field increases between the p and n- junction. To prevent a breakdown the electrical field E must always be smaller than the critical electrical field E_c . If E_c is reached by applying a too high voltage, the breakdown voltage in reverse direction,

free charge carriers can accelerate in the electrical field to a level which enables them to release new electron-hole pairs when they collide with other electrons and the whole crystal becomes conducting generating a lot of heat which usually ends in the destruction of the device. This effect is known under the avalanche effect. [19, 20]

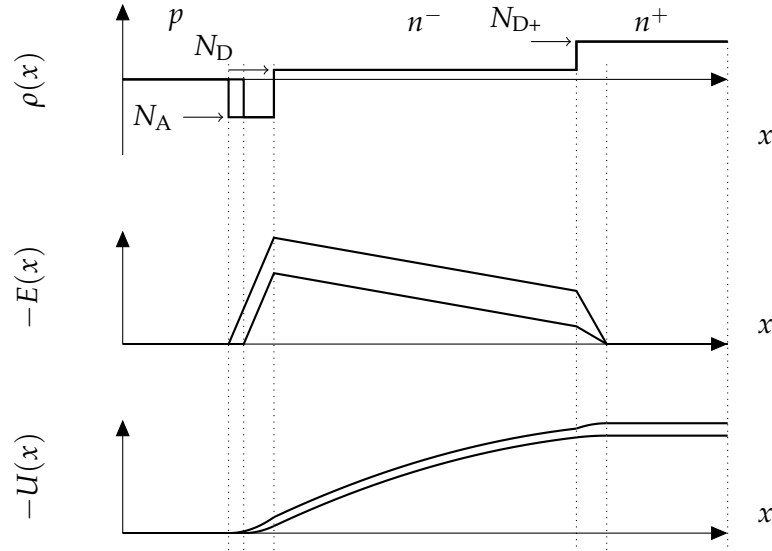


Figure 2.3: Blocking state of a PiN diode with the electric field and voltage distribution, [20].

The electrical field \mathbf{E} and the voltage in Fig. 2.3 can be described with the one-dimensional poisson equation, see eq. (2.1),

$$\frac{d^2U}{dx^2} = -\frac{d\mathbf{E}}{dx} = -\frac{\rho}{\epsilon}, \quad (2.1)$$

where ρ is the space charge density and ϵ the permittivity in As/Vm, which can be calculated with the vacuum permittivity and the relative permittivity $\epsilon = \epsilon_0\epsilon_r$. If the electrical field has a triangular shape, the breakdown voltage U_{BD} can be approximated with eq. (2.2),

$$U_{BD} = \frac{1}{2}\mathbf{E}_c w_D, \quad (2.2)$$

where w_D is the width of the depletion region, here the n- layer. If the PiN-diode diode is forward biased the on-resistance is not defined by the doping concentration of the n-drift layer due to high injection. High injection states that the drift region is flooded with minority carriers and the concentration of minority carriers exceeds the concentration of majority carriers opposed to low injection where there are much fewer minority carriers than majority carriers. [20–22]

Another commonly used diode in power electronics is the schottky diode which consists of a metal and typically a n-doped semiconductor which has the advantage of a lower

forward voltage drop compared to the PiN-diode and faster switching capability due to nearly no reverse recovery effect but at the disadvantage of lower possible breakdown voltages if silicon is used as semiconductor, since by trying to go for higher blocking voltages the reverse current would increase too much. Since the minority carriers in the drift region have a very low concentration it enables the device to switch fast from on-state to the blocking state making them popular for rectification purposes in switch mode power supplies. Nowadays also SiC schottky diodes are commercially available with blocking voltages of up to 1200 V and with nearly no reverse recovery effect. [21]

At the turn-off a power-diode, like the PiN-diode diode, has to reduce the stored minority charge in the drifting region via recombination, preventing the diode from instantly blocking. This is shown in Fig. 2.4, with the reverse recovery time t_{rr} . The reverse recovery charge Q_{rr} is represented by the area when the current i is below zero to approximately 20% of the maximum reverse current I_{RRM} . The reverse recovery charge is always lost at turn-off, therefore for high frequency converters fast recovery diodes or diodes with no reverse recovery effect, like SiC schottky diodes should be used to minimize the off-switching loss. [20]

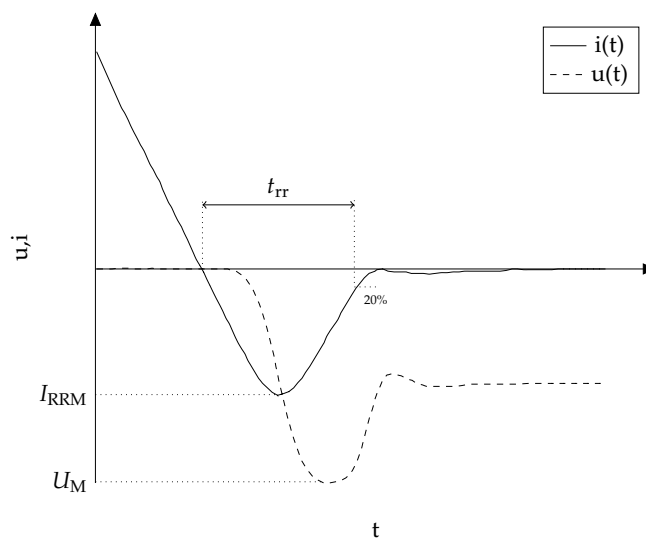


Figure 2.4: Voltage and current waveforms of a PiN-diode during switch off with the reverse recovery charge, [20].

2.2 MOSFETs

MOSFETs are the most important device for high-density integrated circuits like microprocessors and semiconductor memories. The basic principle was first proposed in the early 1930s but the first quality $Si - SiO_2$ device was not produced before 1960, where also

the first power MOSFETs were introduced and with that a new field of switched mode power supplies emerged, continuously introducing improvements and better devices until today. By adopting the processing methods of integrated circuits, it was in the 1980 possible to integrate MOS and BJT technologies on the same chip, introducing the Insulated Gate Bipolar Transistor (IGBT) and MOS controlled thyristor (MCT). With further improvement the last years in semiconductor processing technology, manufacturing and packaging techniques attributes like the switching speed, power handling capability, voltage and the currents rating improved further. The MOSFET is an unipolar device, since in conduction only the majority of carriers is used. For the channel p- and n- types can be distinguished and further two types, the depletion and the enhancement type are possible, resulting in four different possibilities. In powerelectronics the most common type is the n-channel enhancement type, since the carrier mobility of the n-type is higher resulting in a lower R_{DSon} and the device is normally off. The basic structure is shown in Fig. 2.5, which is a n-channel device in lateral structure consisting of a p-type substrate where two $n+$ regions, the source and the drain, are formed. Between the gate contact and the p-substrate exists an SiO_2 isolation and the gate usually consists of heavily doped polysilicon. If a high enough voltage is applied between the gate and the source a surface conducting n-channel is formed between the source and drain $n+$ regions, turning the MOSFET on. [19, 20, 22]

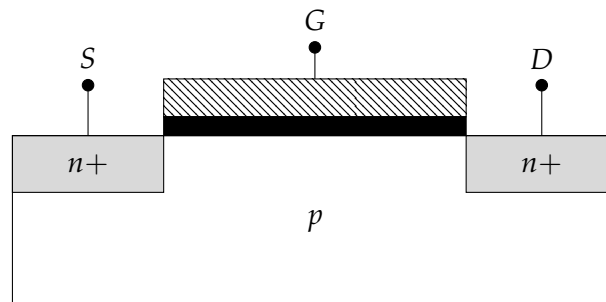


Figure 2.5: Schematic diagram of a lateral MOSFET.

The idealized output characteristic of a MOSFET over increasing U_{GS} is shown in Fig. 2.6, where no channel is formed for a gate-source voltage U_{GS} of zero. With increasing U_{GS} the saturation current increases. In switch mode power supplies semiconductor devices are typically operated in the linear region, to minimize the voltage drop across the device and therefore the conduction loss.

Fig. 2.7 shows the MOSFET with its parasitics and the internal body diode. A power MOSFET can block voltage only in one direction, in the other direction the body diode is reverse conducting, which demands for bidirectional blocking capability a back-to-back configuration of two MOSFETs. The parasitic capacitors between each of the terminals of the MOSFET have great effect on the switching properties and losses. Further all these ca-

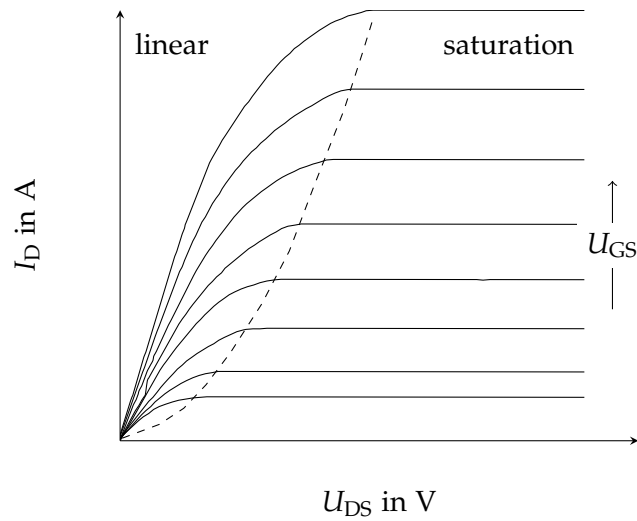


Figure 2.6: Idealized output characteristic for a MOSFET.

capacitors have a non-linear voltage dependency. To turn the MOSFET on, the gate capacitors must be charged and during this time a current is flowing. After the gate capacitors are charged no current is flowing anymore and as long as a gate-source voltage higher than the threshold voltage U_{th} is present, the device conducts. [19]

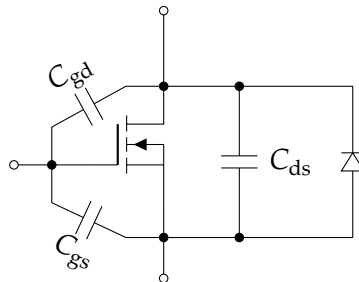


Figure 2.7: Schematic symbol with parasitic capacities and internal body diode.

The in Fig. 2.5 shown structure is rather used for integrated circuits. For higher powers typically a vertical structure is used to increase the power rating of the device, where the drain is located on the bottom of the wafer and the source is with the gate contact on top. [19]

2.2.1 Charge compensation principle

With the commercially availability since 1998 of mass-producible charge compensated devices or *Superjunction devices* which broke the silicon limit [23], a new era for switch mode power supplies began. For reducing the R_{DSon} a high doping is necessary, which on the other side decreases the maximum possible blocking voltage. In a conventional power

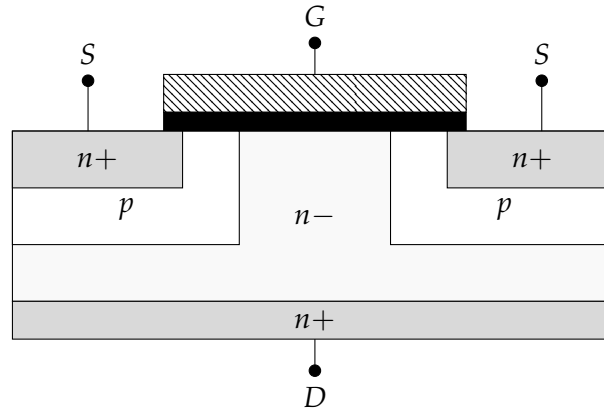


Figure 2.8: Vertical structure of a power MOSFET (simplified).

MOSFET the silicon limit for an optimum doping profile which delivers the optimum R_{DSon} can be calculated, [24]. With a constant doping the on-resistance can be calculated with eq. (2.11) and it scales with the breakdown voltage with the power of 2.5, [20]. A high breakdown voltage needs a thicker epi-layer and therefore increases the R_{DSon} , or respectively the area specific resistance. The characterization of the devices can be done with a FOM $R_{DSon} \cdot A$, which shows the possible resistance with an area of 1mm^2 for a specific breakdown voltage. This resistance is only the resistance of the epi-layer. For high voltage MOSFETs, 95% of the total resistance, for low voltage MOSFETs only 40% are from the epi-layer resistance. With constant doping of the drift zone with N_D the area specific $R_{DSon} \cdot A$ can be calculated, with eq. (2.3)

$$R_{DSon} \cdot A = \frac{w_v}{e_0 \mu_n N_D}, \quad (2.3)$$

where e_0 is the elementary charge, μ_n the electron mobility and w_v the width of the n -drift zone, where it is stated clearly that to reduce the area specific resistance the doping N_D can be increased or the width w_v of the drift zone is decreased, which also deteriorates the possible blocking voltage. The slope of the electric field is according to the poisson equation determined with the doping N_D

$$\frac{dE}{dx} = -\frac{e_0 N_D}{\epsilon}, \quad (2.4)$$

where ϵ is the dielectric constant for silicone with 11.3. The critical electrical field strength E_{crit} in the n - area is around 200 kV/cm if the device is blocking. The breakdown voltage is the integral of the electrical field over the length of the drift zone. In case of a maximum electric field the end values for the electrical field are E_{crit} and $E_{crit} - e_0 N_D w_v / \epsilon$ and by integration or with the formula for calculating the area of a trapezoid the breakdown voltage U_{BD} can be calculated, see eq. (2.5).

$$U_{\text{BD}} = \frac{w_v}{2} \left(\mathbf{E}_{\text{crit}} + \mathbf{E}_{\text{crit}} - \frac{e_0 N_D w_v}{\epsilon} \right). \quad (2.5)$$

By solving eq. (2.5) for N_D and combination with eq. (2.3) the doping factor N_D for the area specific on-resistance can be eliminated,

$$R_{\text{DSon}} \cdot A = \frac{w_v^3}{2\epsilon\mu_n(\mathbf{E}_{\text{crit}} \cdot w_v - U_{\text{BD}})}. \quad (2.6)$$

Derivation of eq. (2.6) with respect to w_v delivers an extrema for,

$$w_v = \frac{3U_{\text{BD}}}{2\mathbf{E}_{\text{crit}}}. \quad (2.7)$$

With the solution for an extrema above inserted into eq. (2.6) the optimum area specific on-resistance in dependence of the maximum blocking voltage and the maximum allowed critical field can be calculated,

$$R_{\text{DSon}} \cdot A = \frac{27U_{\text{BD}}^2}{8\mu_n\epsilon\mathbf{E}_{\text{crit}}^3}. \quad (2.8)$$

From [22] a formula for the critical electrical field strength in dependence of the blocking voltage is given,

$$\mathbf{E}_{\text{crit}} = 8.2 \cdot 10^5 \cdot U_{\text{BD}}^{-0.2} \frac{\text{V}}{\text{cm}}. \quad (2.9)$$

The carrier mobility μ_n also depends on the blocking voltage,

$$\mu_n = 710 \cdot U_{\text{BD}}^{0.1} \frac{\text{cm}^2}{\text{Vs}}, \quad (2.10)$$

and both dependencies are shown in Fig. 2.9.

Combining the equation for the critical electrical field strength and the carrier mobility with the area specific on-resistance, see eq. (2.11), shows that the area specific on-resistance increases with the power of 2.5 with the required blocking voltage.

$$R_{\text{DSon}} \cdot A [\Omega\text{mm}^2] = 8.3 \cdot 10^{-7} \cdot V_{\text{BR}}^{2.5} \quad (2.11)$$

An optimum doping profile, like shown in [24], requires a continually increasing doping profile from source to drain. This hard to manufacture solution only reduces the R_{DSon} from eq. (2.11) only by 11%. [20]

In case of blocking the voltage no carriers are necessary and in the case of conduction a lot of carriers are necessary. By separating both carrier types (holes and electrons) in space,

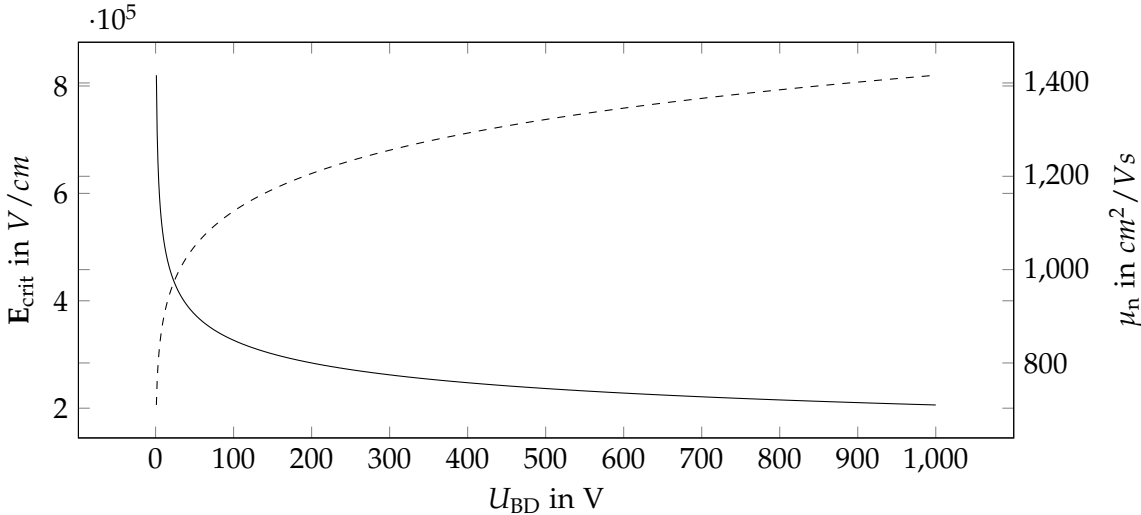


Figure 2.9: Critical field strength and carrier mobility over the required blocking voltage.

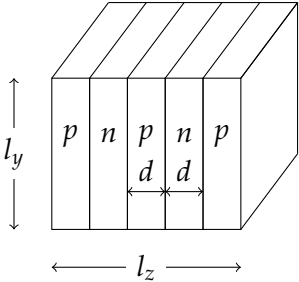


Figure 2.10: Simplified schematic for the compensation structure.

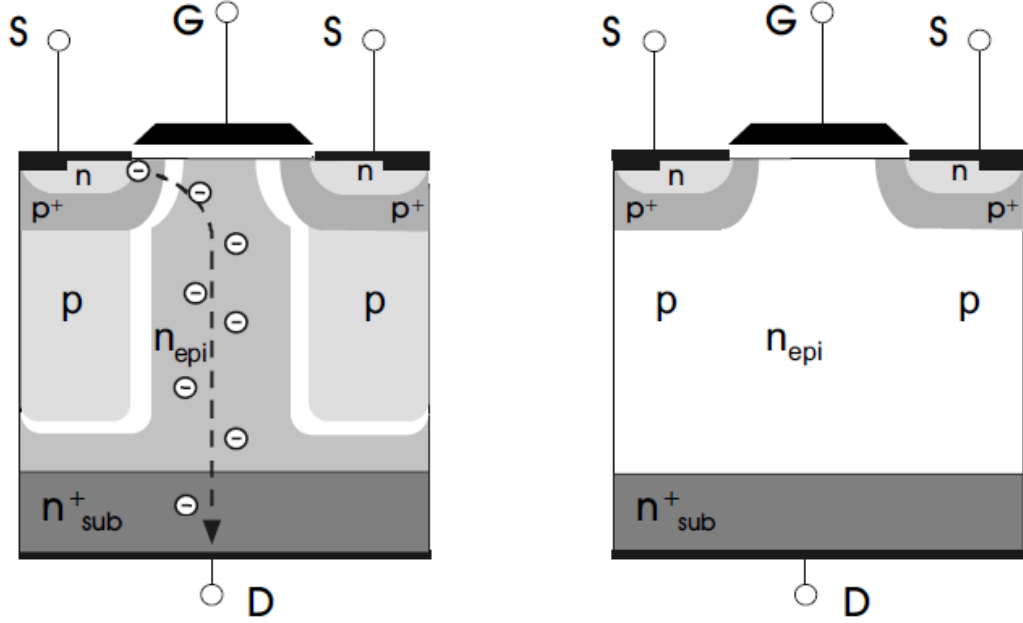


Figure 2.11: Charge compensated device; (left) on-state; (right) blocking state, [20].

so that in the blocking state the total charges are nearly compensated to zero and in the on-state the carriers of one type are available for the current transport.

With charge compensation it is possible to reduce the on-resistance by increasing the doping of the conducting zones without decreasing the blocking voltage. The structure for a compensation device is shown in Fig. 2.10, where the source is located on top of the p-wells (for comparison see Fig. 2.11) which is just stacked many times to achieve the compensation effect. By imagining the column width d very small, then a charge in the p-zone is compensated by a charge in the n-zone, appearing like the area has a doping of zero, which states that the slope of the electrical field in y- and z- direction is also zero, see eq. (2.4), resulting in a rectangular electrical field between drain and source. In case of a turned-on device, the on-resistance R_{DSon} is lower, since the doping of the n-zones can be higher revoking the coupling between the maximum possible blocking voltage and the on-resistance. In the schematic of Fig. 2.10 exists an electrical field in the y- and in the z-direction. The electrical field in the z-direction has a negative slope in the n-doped zones and a positive slope in the p-doped zones and it is due to symmetry zero in the middle of every zone, which allows to write down the solution for the p- and n-zones,

$$\begin{aligned} \mathbf{E}_z &= \frac{e_0 N_A}{\epsilon} (z - z_p) & \text{for } 0 \leq z \leq z_p \\ \mathbf{E}_z &= -\frac{e_0 N_D}{\epsilon} (z - z_n) & \text{for } 0 \leq z \leq z_n \end{aligned} \quad (2.12)$$

and with the assumption that the doping of the p- and n- zones is identical, the maximum electrical field in z-direction,

$$|\mathbf{E}_z|_{\max} = \frac{e_0 \cdot N_D \cdot d}{2 \cdot \epsilon} \quad (2.13)$$

which must be smaller than the critical field strength \mathbf{E}_{crit} . The critical electrical field strength is the sum of the electrical field in the y- and the z- direction, where the partitioning is not yet known, therefore it is described with an additional parameter α ,

$$e_0 N_D d = 2 \cdot \epsilon \cdot |\mathbf{E}_z|_{\max} = 2 \cdot \alpha \cdot \epsilon \cdot \mathbf{E}_{\text{crit}}. \quad (2.14)$$

If the switch is blocking it is assumed that the p- and n- zones clear themselves first and the electrical field is then increasing in the drain-source direction, which only depends on the voltage applied between drain and source, in the case of perfect compensation, this is valid, and the drain source voltage U_{DS} can be written with eq. (2.15),

$$U_{\text{DS}} = \frac{d \cdot |\mathbf{E}_z|_{\max}}{2} + |\mathbf{E}_y|_{\max} \cdot l_y, \quad (2.15)$$

where the channel length is l_y . Perfect compensation would be if the p- and n- zones are infinite thin, which would make the electrical field in z-direction to zero and the breakdown voltage U_{BD} to

$$U_{\text{BD}} = |\mathbf{E}_y|_{\max} \cdot l_y. \quad (2.16)$$

Due to symmetry the electrical field in x-direction is zero, therefore the border for the maximum electrical field in y-direction can be written with eq. (2.17).

$$|\mathbf{E}_y|_{\max} = (1 - \alpha) \mathbf{E}_{\text{crit}}. \quad (2.17)$$

With eq. (2.3), where w_v is now replaced with the length of the channel l_y and by replacing N_D with help of eq. (2.14), and keeping in mind that the current only flows through the n-zone, therefore the resistance has to be doubled, the area specific on-resistance can be calculated,

$$R_{\text{DSon}} \cdot A_y = \frac{d \cdot l_y}{\alpha \cdot \mu_n \cdot \epsilon \cdot \mathbf{E}_{\text{crit}}}, \quad (2.18)$$

where the area of the n-zone normal to the current is A_y . The length l_y can be replaced with eq. (2.15) and eq. (2.16),

$$R_{\text{DSon}} \cdot A_y = \frac{1}{\alpha(1 - \alpha)} \frac{d \cdot U_{\text{BD}}}{\mu_n \cdot \epsilon \cdot \mathbf{E}_{\text{crit}}^2}. \quad (2.19)$$

By derivation of eq. (2.19) with respect to α an extrema for $\alpha = 0.5$ can be found, concluding that the area specific on-resistance is optimal if the electrical field components are equal in

y- and z- direction. By combination of eq. (2.9), eq. (2.10) and eq. (2.19) the area specific on-resistance for a specific column width d , or pitch size can be calculated, see eq. (2.20). The result shows that the area specific on-resistance rises only with the power of 1.3 of the blocking voltage, compared to the power of 2.5 with the optimal doping profile. [20]

$$R_{\text{DSon}} \cdot A_y \quad [\Omega \text{mm}^2] = 8.09 \cdot 10^{-1} \cdot d \cdot V_{\text{BR}}^{1.3}. \quad (2.20)$$

Fig. 2.12 compares the area specific on-resistance over the blocking voltage for a traditional power MOSFET with optimum doping profile with charge compensated devices of different generations, where it can be investigated, that an increase in blocking voltage the area specific on-resistance increases quickly (to the power of 2.5) for the traditional power MOSFET compared here with the third and seventh generation of CoolMOS. Since for charge compensated devices the area specific on-resistance increases only with the power of 1.3 of the blocking voltage, huge improvements for higher blocking voltages are possible, where the available technology is the limiting factor of how thin the n and p-zones can be made.

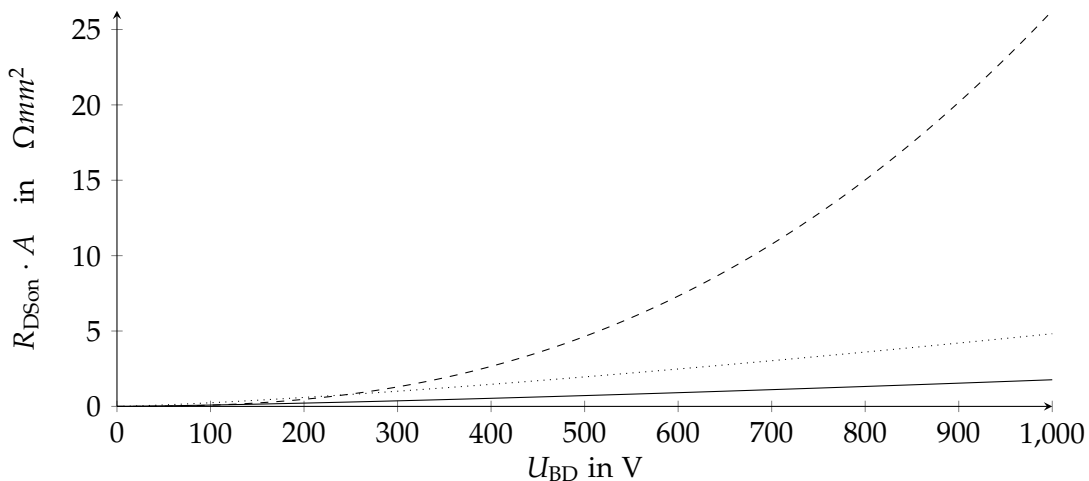


Figure 2.12: Comparison of a traditional power MOSFET with optimal doping (dashed); a charge compensated device with $d=7.5\mu\text{m}$ (Coolmos C3, dotted), and a charge compensated device with $d=2.75\mu\text{m}$ (Coolmos C7, solid).

2.2.2 Figure of merit

For comparing MOSFETs of the same voltage class different properties of the device are typically multiplied and the result which is called FOM, allows a quick comparison between different technologies or different manufacturers. For example one definition is the product of $R_{\text{DSon}} \cdot Q_G$, where R_{DSon} is the drain source channel resistance when the device

is on and Q_G the gate charge, which is usually used as the FOM in a soft switched topology. For a specific technology process and voltage class it can be stated that the FOM is constant which implies that a lower R_{DSon} leads to a higher Q_G . Another definition for FOM could be the Baliga High Frequency Figure of Merit (BHFFOM) [25], which states that the losses at high frequency switching come mainly from the charging and discharging of the input capacitance C_{ISS} , see eq. (2.21),

$$BHFFOM = \frac{1}{R_{ON,sp} \cdot C_{in,sp}}, \quad (2.21)$$

with $R_{ON,sp}$ as the specific on-resistance and $C_{in,sp}$ as the specific input capacitance. This FOM is similar to the above mentioned one, where the gate charge is multiplied with the on-resistance.

There is also another definition called New High Frequency Figure of Merit (NHFFOM) [26], which states that the major switching loss is due to the charging and discharging of the output capacity C_{OSS} , see eq. (2.22),

$$NHFFOM = \frac{1}{R_{ON,sp} \cdot C_{OSS,sp}}, \quad (2.22)$$

where $C_{OSS,sp}$ is the specific output capacitance. This FOM considers the output capacitance of the MOSFET, therefore it is better for a comparison if the MOSFETs are hard-switched, since then the losses from the output capacity outweigh the gate charge losses. In hard switching topologies the output capacitance (C_{OSS}) matters, due to the added extra loss $\Delta P_{sw-on} = U_{sw}^2 / 2 \cdot C_{OSS}$ at every turn-on event. In a resonant circuit the output capacitance is not important for the efficiency since the MOSFETs are always switched on under zero voltage condition, not losing their output charge therefore reducing significantly the switching loss.

Fig. 2.13 shows a comparison, where the FOM was calculated with $R_{DSon} \cdot Q_G$ for MOSFETs with different voltage classes and different generations of technologies. For the 650 V class a huge improvement of the FOM can be examined between the at the moment latest generation C7 and the older C6. Still the OptiMOS 3 with 250 V has a by far better FOM than the high voltage MOSFETs. Also the improvement in the 40 V class between OptiMOS 3 and 5 is shown, which also reduces the FOM by a factor of 2.8. It can be investigated that the FOM improves with the available technology and with the required voltage rating.

2.3 High voltage charge compensated MOSFETs

To mass produce charge compensated devices the challenge is the accuracy of the manufacturing process to compensate the charges. This is done with equal p- and n- doped

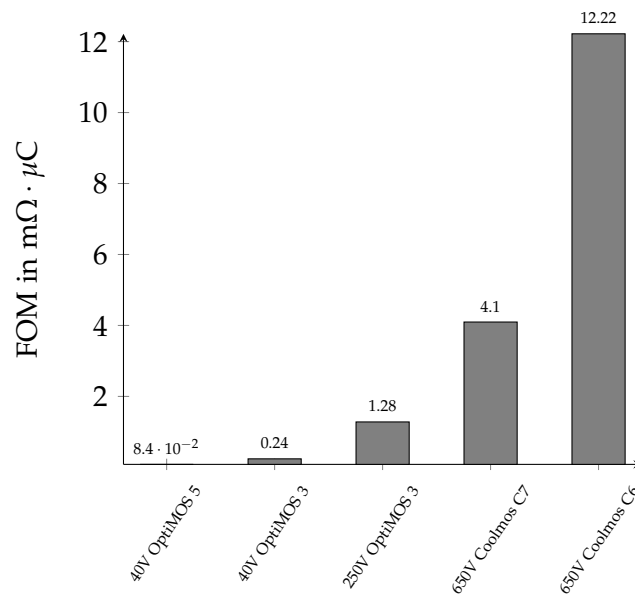


Figure 2.13: Comparison of the FOM for different LV and HV technologies.

columns. For high voltage MOSFET the multi-epitaxy process is usually used, where the MOSFET is slowly grown on an n^+ substrate wafer, see Fig. 2.14. If the compensation is not perfect, the excess carriers add to the space-charge region, reducing the maximum possible blocking voltage. To lower the R_{DSon} further in a charge compensated device the distance of the p-columns has to be minimized, increasing also the need of epitaxial steps and increasing cost. [27]

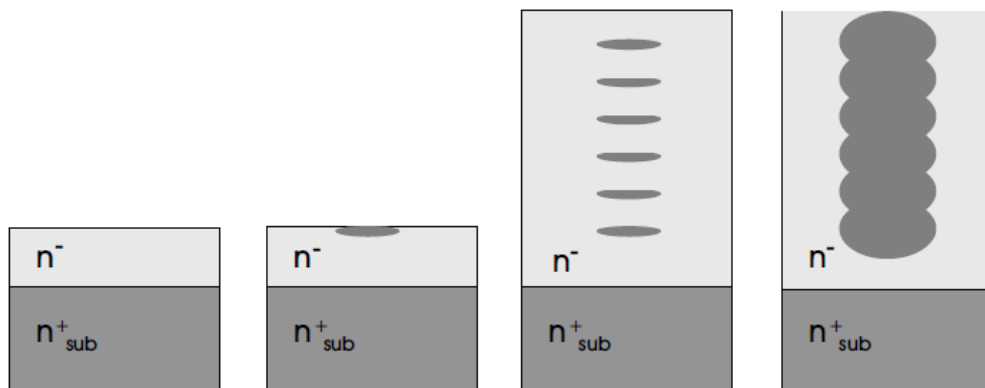


Figure 2.14: Construction steps for a charge compensated device; (1) n^+ Wafer with a n^- drift zone; (2) masked bor implantation in the n^- layer; (3) Repeated process of the bor implantation; (4) Diffusion, [20].

2.4 Trench structure for low voltage charge compensated devices

Trench devices are usually low voltage devices, manufactured by etching a trench in the silicon. Then the trench is coated with Silicon Oxide SiO_2 and for the newest devices electrodes are implemented. The lower one is the shield electrode, which is connected to the source and is used for the charge compensation or superjunction principle. The upper electrode is the gate electrode which also forms the conducting channel. The shield electrode additionally helps to reduce the size of the gate-source capacity C_{GS} with the longer trench extension, reducing the gate losses and the switching speed.

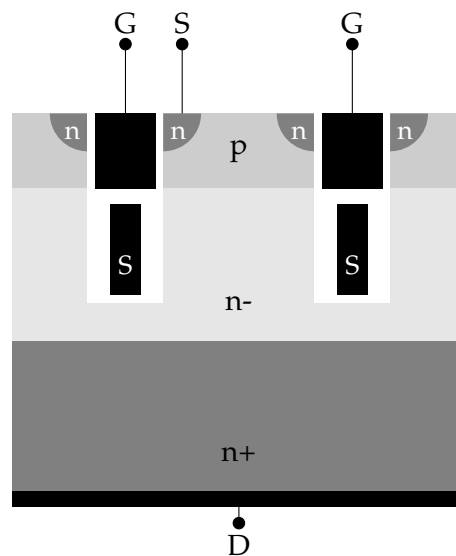


Figure 2.15: Double gate trench MOSFET structure, with gate contact and a second shield contact (below the gate contact), which is connected to source.

For low voltage MOSFETs the main contributors for the R_{DSon} are not like for the high voltage counterparts in the n^- -epi layer, they are more distributed, see Tab. 2.1. With a trench technology the accumulation layer resistance can be eliminated. [28]

Trench technology is usually only used for LV MOSFETs, since the SiO_2 isolation layer would get to thick to isolate against higher voltages and has the advantage of cheaper mass production.

2.5 Conclusion

A quick introduction for modern power semiconductors which are often used in SMPS was given with an explanation of the revolutionary charge compensation principle. Later the structural difference between HV and LV MOSFETs was shown and as well how the

Table 2.1: Contributors to R_{DSon} for MOSFETs with different blocking voltages, [28]

		$V_{DS}= 30\text{ V}$	$V_{DS}= 600\text{ V}$
		(%)	(%)
R^{S*}	Package	7	0.5
R_{n+}	Source Layer	6	0.5
R_{CH}	Channel	28	1.5
R_a	Accumulation Layer	23	0.5
R_{epi}	n^- -layer	29	96.5
R_{Sub}	Substrate	7	0.5

performance of power MOSFETs can be compared using the FOM, where it was clearly shown that LV MOSFETs can outperform HV MOSFETs and a solution for utilizing LV MOSFETs and profiting from the improved FOM can enable SMPS with higher efficiency and a higher power density.



Introduction and topologies

3.1 Introduction

Today modern power supplies are usually switched mode power supplies, which are cheaper, more efficient, smaller, and lighter than power supplies which utilize a low frequency transformer in combination with a linear voltage controller. In addition to that semiconductor power switches experienced a big improvement with the charge compensation principle a few years ago and are still constantly improved, pushing the efficiency and power density limits further. A quick overview of the different loss sources in a SMPS and how they influence the efficiency is given in section 3.2.

Nowadays digital control loops often replace analog ones due to the improvement of microcontrollers in speed and cost, enabling more complex control strategies for an even higher performance of the SMPS for instance by being able to utilize soft switching techniques, which is a requirement for a high efficient SMPS and is explained in section 3.3.

The generation of a high voltage DC by direct rectification of the grid voltage, for instance with a bridge rectifier, leads to a high harmonic distortion, since the capacitor is only charged when the line voltage is around its peak value, as will be shown later in this chapter. These harmonics may produce higher line rms currents, which don't add any real power to the actual load therefore increase the losses, may cause oscillations and endanger the stability of the system operation, may mistrigger protection circuits or may cause EMI problems, which will be shortly covered in section 3.4.

In the past the grid quality was deteriorated from pollution until the 1980s, then the first technical standard, the IEEE519-1981 was released, which aimed to help engineers with technical design references and started the research in the area of PFC to reduce the harmonic content produced by electronics which are connected to the grid. In the 1990s switch mode power supplies began to replace the bulky linear power supplies, increasing efficiency and power density of a power supply, but with the increasing popularity of SMPS

and their increased harmonics the research into the topic PFC became further strengthened. [19]

A typical modern power supply runs on the grid, delivers one or more regulated DC output voltages, where the output has to be isolated from the input and it has to satisfy regulations in terms of harmonic distortion of the current drawn from the mains, which is today achieved with an extra, often mandatory, PFC stage that shapes the current sinusoidal and furthermore the PFC stage must be able to handle different sinusoidal main voltages, which may vary in frequency from usually 50 to 60 Hz and in voltage from 110 V to 230 V. Fig. 3.1 shows an overview of possible electronic voltage converters.

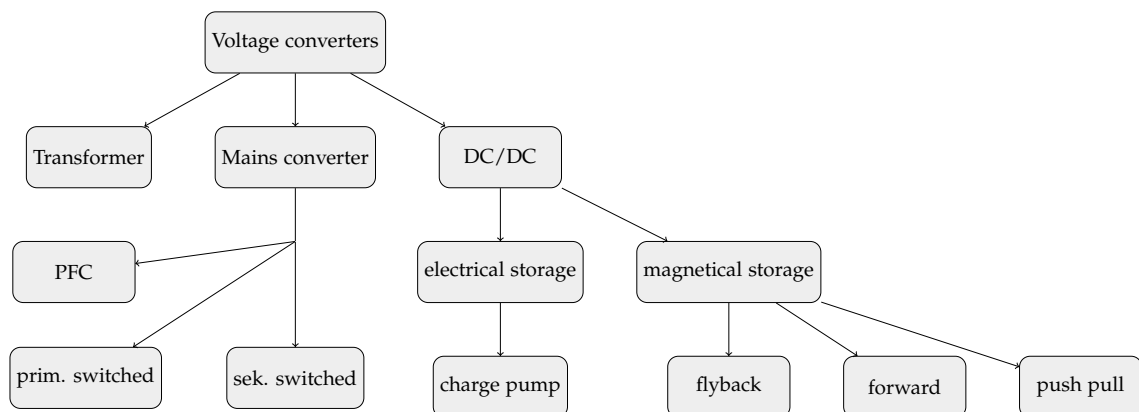


Figure 3.1: Overview of voltage converters. [29]

In the following different hard and soft switched topologies for PFC and DC/DC converter systems, which are typically and often encountered in modern power-supplies are explained. The switches of the presented topologies are all MOSFETs, which is standard today. These switches are either on or off and do not operate in their active region, leading to a significant reduction in power loss, [30].

To show the need for a PFC the difference between a direct AC/DC conversion with a full bridge rectifier, a full bridge rectifier with a passive PFC and an active PFC with different control methods for the standard boost and more advanced bridgeless topologies in section 3.5 are shown, including the spectrum of the harmonics.

Since the output voltage for a server supply is usually much lower than the DC-link voltage of the PFC a DC/DC conversion stage is needed afterwards. On top regulations for power supplies require that the output of the power supply is isolated from the mains, therefore only solutions with isolation were investigated in section 3.6. Based on the following comparisons the topologies for the prototype were chosen.

3.2 Loss characteristic and efficiency

For a system the efficiency is defined as output power over input power, see eq. (3.1), where P_{in} is the total input power, P_{out} the output power and P_v the power lost, which can be approximated for small P_v with the Taylor series. For a real system the efficiency is always smaller than one.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_v} = \frac{1}{1 + \frac{P_v}{P_{out}}} \approx 1 - \frac{P_v}{P_{out}}. \quad (3.1)$$

The composition of the lost power P_v is shown with eq. (3.2),

$$P_v = P_{v,0} + P_{v,I} + P_{v,II} = k_0 + k_I \cdot P_{out} + k_{II} \cdot P_{out}^2, \quad (3.2)$$

where $P_{v,0}$ is constant lost power independent from the output power for powering the auxiliary systems comprising the control and measurement circuitry, gate drive standby power and maybe cooling power for fans. Additionally $P_{v,0}$ also includes lost power from capacitive switching loss of the power semiconductors and core losses which are by a first approximation for the boost inductors only dependent on the switching frequency, the duty cycle and the output voltage. For the transformer of the DC/DC converter the losses also mainly depend on the switching frequency, the input voltage and also the leakage current especially for electrolytic capacitors. The part $P_{v,I}$ depends linearly on the output power P_{out} and covers switching loss which can be approximated as a current dependent loss and loss from bipolar semiconductors causing an approximated current independent forward voltage drop, like diodes. The last part $P_{v,II}$ describes current dependent losses, which increase with the square of the current, including conduction loss of switches, magnetics and capacitors.

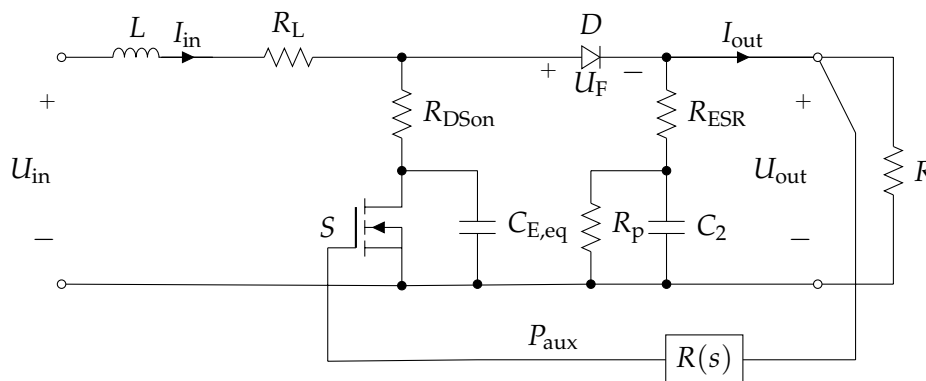


Figure 3.2: Power losses in a DC/DC boost converter, [7].

For shaping the efficiency curve and for being able to choose a point for highest efficiency, the above mentioned loss components are now closer investigated.

For a constant power loss, the efficiency

$$\eta_0 = \frac{1}{1 + \frac{P_{v,0}}{P_{out}}} = \frac{1}{1 + \frac{k_0}{P_{out}}} \approx 1 - \frac{k_0}{P_{out}}, \quad (3.3)$$

improves with increasing output power. For very low output powers the efficiency tends to zero therefore at zero output power the efficiency is zero. The constant loss has great influence on the partial load efficiency.

Linear output power dependent loss $P_{v,I}$ lowers the efficiency constantly,

$$\eta_I = \frac{1}{1 + \frac{P_{v,I}}{P_{out}}} = \frac{1}{1 + k_I} \approx 1 - k_I = \text{const.} \quad (3.4)$$

The quadratic part of the losses has no influence for zero output power but an increased influence for full output power,

$$\eta_{II} = \frac{1}{1 + \frac{P_{v,II}}{P_{out}}} = \frac{1}{1 + k_{II}P_{out}} \approx 1 - k_{II}P_{out}. \quad (3.5)$$

For maximizing the efficiency at a certain operating point, the total efficiency can be rewritten,

$$\eta = \frac{1}{1 + \frac{k_0}{P_{out}} + k_I + k_{II}P_{out}} \approx 1 - \left(\frac{k_0}{P_{out}} + k_I + k_{II}P_{out} \right), \quad (3.6)$$

and with eq. 3.1,

$$\frac{P_v}{P_{out}} = \frac{k_0}{P_{out}} + k_I + k_{II}P_{out} \rightarrow \min, \quad (3.7)$$

and with eq. 3.2 results in

$$-k_0 \frac{1}{P_{out}^2} + k_{II} = 0 \rightarrow P_{v,0} = P_{v,II,\eta_{\max}}, \quad (3.8)$$

showing that the efficiency is highest for a certain point if the quadratic and constant losses are equal. The output power with the highest efficiency can then be calculated with

$$P_{out,\eta_{\max}} = \sqrt{\frac{k_0}{k_{II}}}, \quad (3.9)$$

and the maximum efficiency with

$$\eta_{\max} = 1 - k_I - \sqrt{k_0 k_{II}}. \quad (3.10)$$

Showing that the linear losses $P_{v,I}$ have an influence on the maximum achievable efficiency η but they have no influence for the output power with maximum efficiency. [7]

3.3 Soft switching

In a hard switched topology the switches are turned off under current and turned on under voltage, resulting in high stress for the switches and high power loss, which respectively increases linearly with the switching frequency. Additionally high di/dt and dv/dt transitions occur producing lot of unwanted EMI. For achieving highest efficiencies and a high power density a soft switched topology is required. Soft switching implies that the switch is turned on under zero voltage and turned off under zero current, which is done by exploiting LC resonance transitions. In a hard switched topology there are not only losses caused due to the overlap of voltage and current during the switching transition additionally the output charge of a MOSFET is dissipated as heat at every turn on, reducing the efficiency drastically for increasing switching frequencies. The associated switching waveforms and the calculation of the switching loss are closer investigated in section A.1. These losses depend mainly on the switching speed, where switches consisting of new materials like GaN or SiC offer a much higher switching speed and therefore lowering switching losses by an order of magnitude compared to traditional silicon devices. On the other hand due to the steeper slopes of voltage and current transitions also EMI is increased. The device stress during a hard switched transition is compared to a soft-switched transition, relatively high because of the high current or voltage and therefore the switch must be operated in a Safe Operating Area (SOA), see Fig. 3.3, where the SOA is inside the dotted outlines. The area beneath the curves is also equal the lost power during the switching transition. Due to the parasitic inductances of the circuit and the device itself the demands on the switch are often further increased. In power electronics a compromise between efficiency and power density has always to be made, [31, 32]. With resonant topologies higher switching frequencies are possible, since the switching loss is significantly reduced, resulting in a higher possible power density. [30]

3.4 Electromagnetic Interference

EMI is caused from high dv/dt and di/dt values and may cause disturbances to other equipment or to the equipment itself. Two different forms of EMI are known, radiated and conducted, where radiated EMI is found at higher frequencies and it spreads by radiation and conducted EMI travels over the wiring and is usually below 10 MHz. Power electronic circuits usually produce EMI noise with a broad frequency range from the switching frequency up to several megahertz, where the low frequency range, ranging from 10 to 150 kHz has received the most attention by several standards. EMI issues can be the reason for an erroneous turned on switch, when it should not be turned on leading to a shoot-through which can destroy one or more devices, or it interferes with measurements making

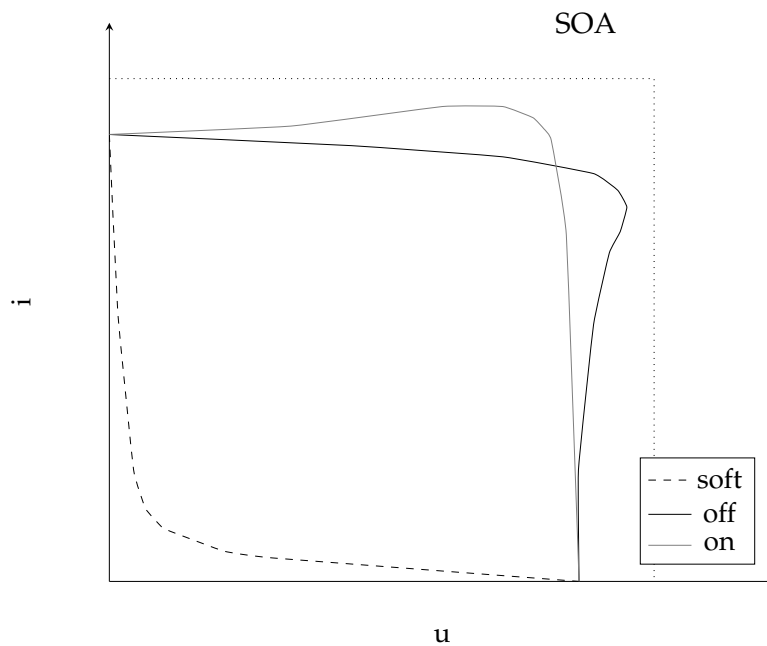


Figure 3.3: Switching transitions for soft switching and hard switching with the Safe Operating Area of the switch, [30].

the control less reliable or unstable. Radiated EMI can be reduced with metal shielding, for example by enclosing the whole power supply in a metal case to reduce the radiated EMI for other equipment. For the power supply itself a careful layout design can reduce the cross-talk significantly. The conducted EMI can further be split into common mode and differential mode noise, where the differential mode noise is a measured current or voltage between the main lines and common mode noise is measured between the main line and ground. To reduce this noise generated by the switching of the power supply a filter is usually needed to satisfy the regulations. The common mode occurs because of parasitic elements like stray capacitors and stray electric and magnetic fields. Several regulations exist for the conducted EMI for different kinds of equipment, which state a certain limit of allowed noise. The differential and common mode noise is always measured over a Line Impedance Stabilization Network (LISN) network, which is a low pass filter with a known impedance that is placed between the grid and the Device Under Test (DUT). The conducted EMI is then measured as voltage over EMI receivers. To be able to compare EMI measurements, detailed specifications for the detectors exist, where the most common types are peak, quasi-peak and average detectors, which are based on RC circuits with different defined charging/discharging constants. A peak detector for example has a very short charging constant and a long discharging constant. The quasi-peak detectors were primarily developed for emulation of the human ear, where the charging constant is 1 ms and the discharging constant is 160 ms. The average detector averages over a long

time period of one second. In soft switched topologies the EMI noise is already reduced, lowering the requirements for the filter and saving further on cost and volume. In case of a hard switched topology good designed snubber circuits can also lower the EMI and are as well most of the time needed to lower the device stress. To reduce magnetic fields already during the layout design the enclosed area by a current loop should be kept as small as possible, which means that the conductors should run always as close as possible to the return wire. In order to reduce stray capacitances and with that the common mode noise the area of exposed metal at the switching potential should be as far away from ground as possible. Nevertheless even if everything mentioned above has been taken care of, a EMI filter is often still necessary to satisfy regulations. A typical filter for that is shown in Fig. 3.4, where L_{DM} is the inductance for the differential mode, L_{CM} for the common mode, C_{DM} the capacitor for the differential mode and C_{CM} for the differential mode. The common mode inductor is an inductor wrapped on a single core in opposite direction generating flux only for common mode noise. For differential mode noise the flux is canceled. For the capacitors used in the EMI filter it is important that the series inductance is low, that the dielectric and ohmic losses are low and that the capacitance is stable over the frequency. [19, 30]

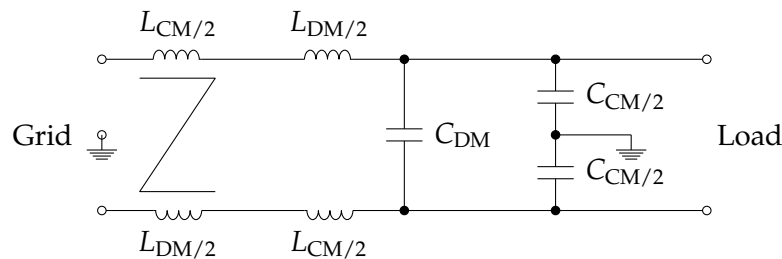


Figure 3.4: Typical schematic of a single stage EMI filter for common and differential mode.

3.5 Power factor correction

Today active PFC circuits are required by international regulations to limit the harmonic distortions on the mains, like the „EN 61000-3-2“ which states that an active PFC circuit is required if more than 75 W are drawn from the grid. This number is subjected to be even lower in the near future. A PFC also maximizes the real power that can be drawn from the grid by equalizing the shape of the current with the mains voltage and therefore emulates a resistive load. To measure how good a PFC performs this emulation, the calculation of

the power factor can be used, which is the ratio of real power over apparent power, see eq. (3.11),

$$PF = \frac{\text{real Power}(W)}{\text{apparent power (VA)}}, \quad (3.11)$$

where the real power is calculated over a period of the instantaneous current multiplied with the instantaneous voltage $i(t) \cdot u(t)$ and the apparent power is the effective value of the input voltage multiplied with the effective value of the input current, [30, 33], which should result in a value of one for a perfect PFC. Only the fundamental component increases the real power and harmonics contribute to the apparent power. For a power factor of one no harmonics are allowed which means the input current has the same shape as the input voltage and is in phase with the input voltage. This can also be expressed with the Total Harmonic Distortion (THD) of the current, see eq. (3.12),

$$THD = 100 \cdot \sqrt{\sum_{h=2}^{\infty} \frac{I_h^2}{I_1^2}}, \quad (3.12)$$

where I_h is the sum of the quadratic harmonic currents and I_1 is the fundamental current. Vice versa the distortion power factor can be calculated from the THD, see eq. (3.13). [34, 35]

$$DPF = \sqrt{\frac{1}{1 + THD^2}}. \quad (3.13)$$

The DPF describes the distortion of the current from an ideal sinus. The power factor PF also considers the phase angle ϕ between the line voltage and the current and is defined with eq. (3.14). [7]

$$PF = \sqrt{\frac{1}{1 + THD^2}} \cdot \cos(\phi). \quad (3.14)$$

3.5.1 Uncontrolled passive PFC

Fig. 3.5 shows a standard bridge rectifier circuit without PFC and Fig. 3.6 shows it with an additional inductor as passive PFC. Additionally, Fig. 3.7 shows the according waveforms. Passive PFC are still used because of their high reliability and power handling capability for heavy loads like arc furnaces, metal rolling mills, electrical locomotives, etc., [19]. Without a PFC a high inrush current like in Fig. 3.7a can be observed, which is also causing a lot of harmonic distortions, which is shown in Fig. 3.7c. By introducing a filter inductor the input current shape is more sinusoidal as well the peak current is lowered, see Fig. 3.7b, which also reduces the harmonic content, see Fig. 3.7d. Due to an additional voltage drop across the inductor the output voltage of the rectifier is lower compared to just a full bridge rectification, but also the ripple of the output voltage is reduced. Due to the lowered peak

current with the inductor the efficiency is approximately the same, since also the diodes losses are lower, compared to a fullbridge rectifier without PFC. To satisfy the „EN 61000-3-2“ a passive PFC requires often huge and expensive magnetic components, if its possible to fulfill the requirements at all. [30]

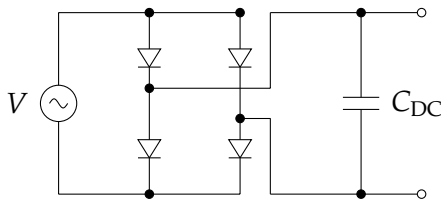


Figure 3.5: Standard bridge rectifier without PFC.

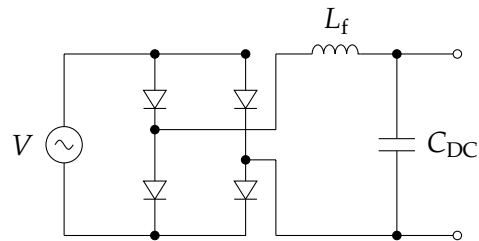


Figure 3.6: Standard bridge rectifier with passive PFC.

Since passive PFC are expensive, bulky and limit the achievable power factor, active PFC circuits are required. The next sections will present the most common used active PFC topologies followed with a comparison of their advantages or disadvantages.

3.5.2 Active PFC

Active PFC circuits are always controlled and are able to draw sinusoidal currents from the grid by emulating a pure resistive load. If the drawn current is sinusoidal and in phase with the mains voltage the drawn reactive power is zero and only real power is drawn and the power factor then is one making the THD zero. The emulation of a resistive load can be accomplished with an increased DC-link voltage, making a boost topology viable.

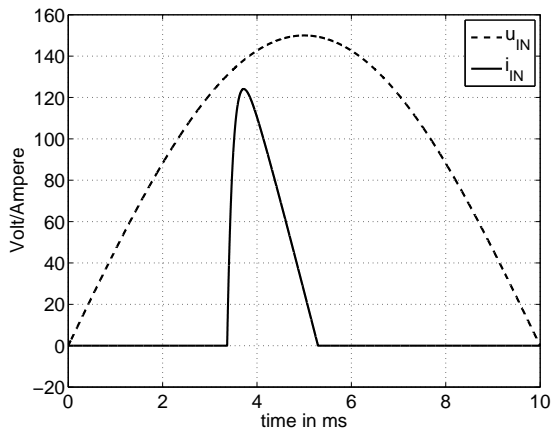
3.5.2.1 Standard PFC Boost

One of the simplest and widely used active PFC circuits is a full bridge rectifier followed with a boost converter [36], shown in Fig. 3.8. This circuit can operate in CCM, Discontinuous Conduction Mode (DCM) or Boundary Conduction Mode (BCM), as shown in Fig. 3.9. In CCM, see Fig. 3.9a, the ripple of the inductor current i_L is the lowest and the control is done with a fixed frequency. In DCM (see Fig. 3.9b) the inductor current always goes down to zero and stays there until the next switching cycle begins. In BCM (see Fig. 3.9c) the switch is turned on as soon as the inductor current reaches zero.

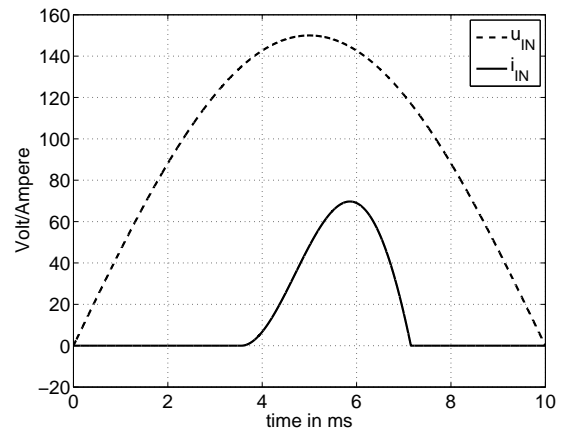
Tab. 3.1 shows the advantages and disadvantages for the three possible operating modes for the boost PFC.

Advantages:

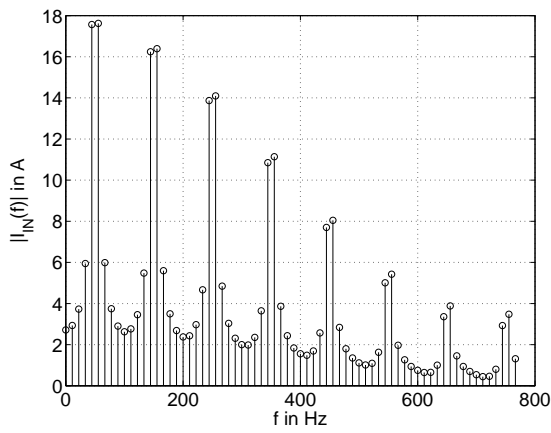
The standard boost has the advantage of simplicity, both in control and components and it



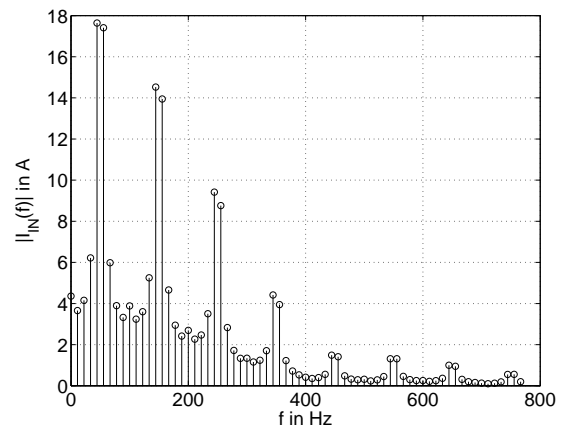
(a) No PFC.



(b) passive PFC.



(c) Spectrum of the input current if no PFC is used.



(d) Spectrum of the input current for a passive PFC.

Figure 3.7: Comparison of no PFC and a passive PFC.

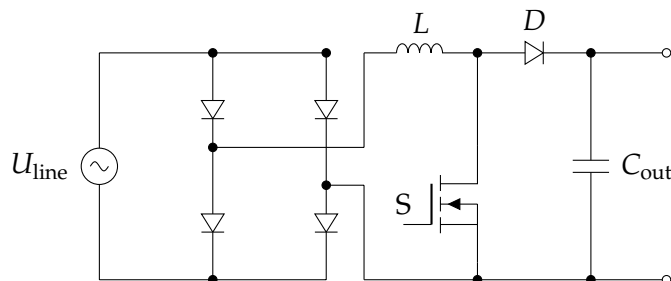


Figure 3.8: Standard Boost PFC with full bridge rectifier.

Table 3.1: Comparison of CCM, DCM and BCM operation modes of the PFC.

	Advantages	Disadvantages
CCM	lowest rms current, fixed frequency	largest inductor value, always hard switching
DCM	fixed frequency, lower inductor value, zero voltage and current turn on	highest rms current
BCM	lower inductor value, zero current turn on,	variable frequency

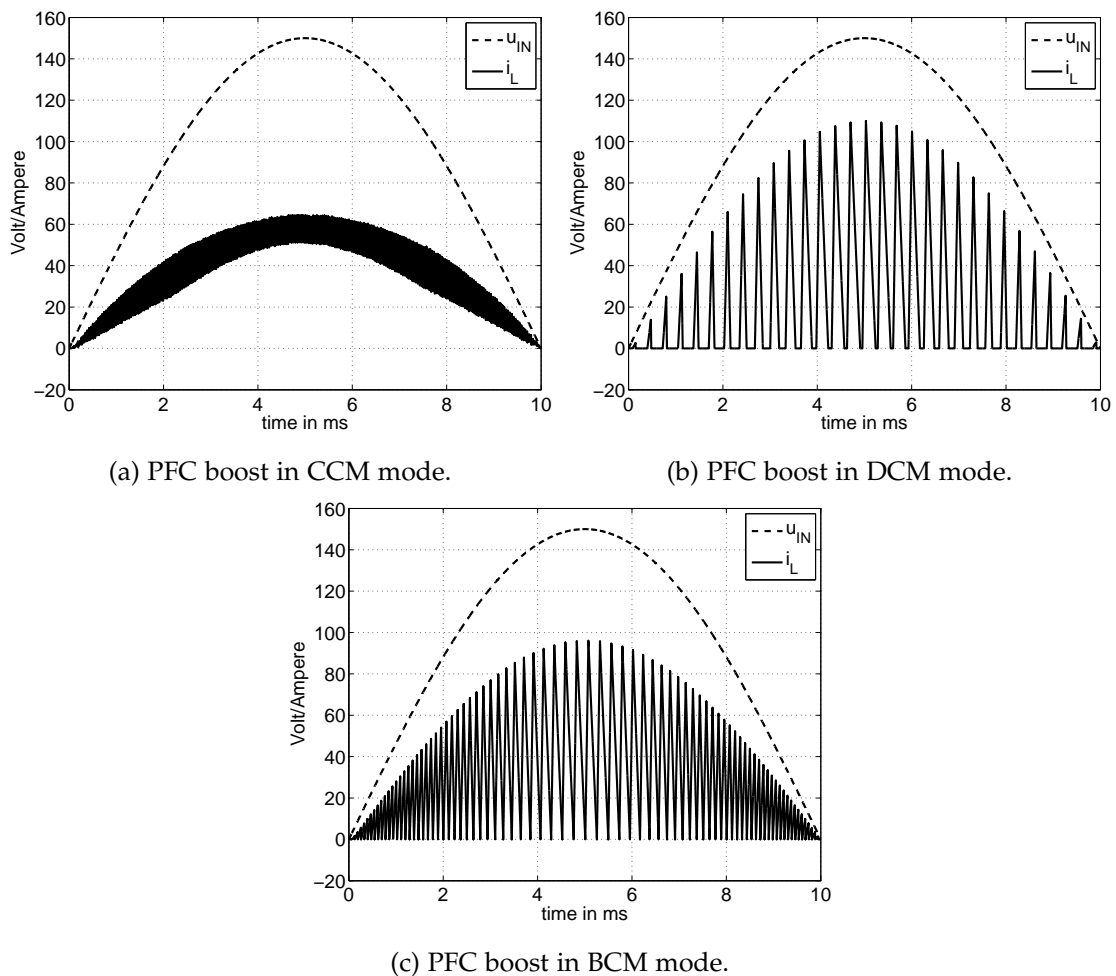


Figure 3.9: Different PFC operating modes.

can achieve a good power factor.

Disadvantages:

The greatest disadvantages are the rectifier diodes on the input. In this circuit the current has to flow through at least two diodes, producing a high and constant loss, especially at higher output powers. Especially for low line input (110 V) high efficiencies (98% and more) are therefore unreachable. The second drawback is the boost diode, which reduces the efficiency further by the forward voltage drop and the reverse recovery loss. By replacing the boost diode with a SiC diode, the reverse recovery loss gets negligible small, boosting the efficiency, but increasing cost heavily. Also the forwards voltage drop of SiC diodes is higher compared with a PiN-diode diode.

3.5.2.2 Bridgeless Boost

To achieve a higher efficiency the passive full bridge rectifier are replaced with active switches. One idea is the bridgeless boost PFC, see Fig. 3.10, which requires two active switches instead of one like in the standard boost. In this topology the current also only flows through two semiconductor devices at a time which makes high efficiency designs possible.

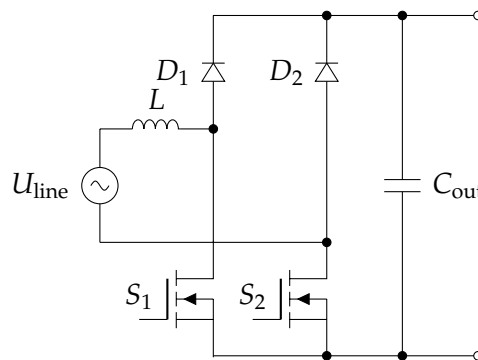


Figure 3.10: Bridgeless boost PFC.

Advantages:

This topology is a bridgeless topology without the input rectifier. This enables high efficiencies with minimum components and simple control.

Disadvantages:

The drawback in the shown configuration is the increased Common Mode (CM) noise by charging the parasitic capacitors between the AC ground and the output ground [37, 38]. This can be reduced by splitting the boost inductor into two inductors, half of the required

inductance is then connected to each AC grid line. But there is still a boost diode which causes a forward voltage drop and in case of no SiC device, a reverse recovery loss.

3.5.2.3 Bridgeless Totem Pole

This topology, see Fig. 3.11, replaces the boost diode with another semiconductor switch, eliminating the forward voltage drop and the reverse recovery loss and promises highest efficiency. This topology may be operated in CCM, which requires devices with a very low reverse recovery charge like GaN and a low parasitic output capacitance [8], or in a sort of BCM with traditional silicon superjunction devices, called TCM mode.

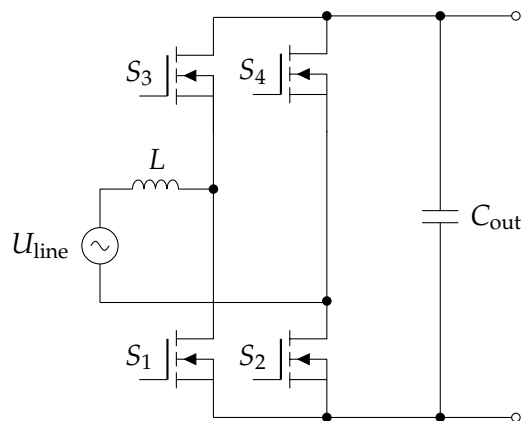


Figure 3.11: Totem pole boost PFC.

Advantages:

The current flows only through two semiconductors at any time, and both are switches which have a lower voltage drop than diodes due to a low on-resistance R_{DSon} . With new next generation power devices like GaN the circuit can be operated in CCM with a fixed frequency, making the control again simple.

Disadvantages:

If operating in TCM mode with either GaN or traditional silicon devices the control is a bit more complicated, since the switching frequency varies. Additionally for the control, information about the current through the inductor is needed, like the inductor zero current crossings, which requires additional circuitry.

3.5.2.4 Triangular Current Mode Resonant PFC

For the prototype chosen topology is the totem pole boost PFC running in TCM mode, [39–43]. If the switches are switched in a triangular current pattern which is similar like in BCM, its possible to switch them always on in a zero voltage condition, resulting in nearly no turn-on losses. This topology shows most advantages for a high efficiency PFC

with traditional silicon devices. Further to minimize conduction loss and the input current ripple multiple phases can be implemented and operated parallel but out of phase to each other, see Fig. 3.12 for a TCM PFC with three phases.

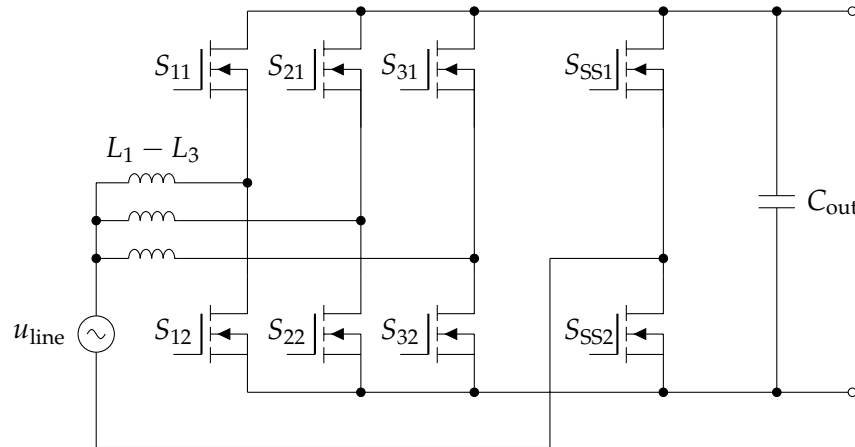


Figure 3.12: TCM PFC with three phases.

Advantages:

As already described for the bridgeless totem pole PFC this topology offers low conduction loss and if switched in a TCM pattern the on-switching loss is greatly reduced. There is only a off-switching loss left, since the switches have to be turned off under current. The small turn-on loss, due to the non-ideal parasitic output capacitance where it is not possible to recover again 100% of the stored energy, can be neglected. The switches S_{SS1} and S_{SS2} switch relatively slow with the line frequency and can be devices with a very low R_{DSon} .

Disadvantages:

For every phase additional circuitry for current measurement is needed. The control is due to the changing switching frequency more complex.

3.6 DC/DC Conversion

For DC/DC conversion it has to be distinguished between non-isolated and isolated solutions. Safety requires for a SMPS which is connected to the mains, that the output is isolated from the input (e.g. „DIN EN 61558-2-16“). Respectively this section will describe only topologies for DC/DC conversion topologies which offer isolation.

The PFC is followed by a DC/DC conversion which transforms the high DC-link voltage down to a smaller regulated DC voltage usually suited for computers and servers (12 or 5V). It can be differentiated between flyback, forward and push pull topologies. In a flyback topology the energy is stored in a magnetic component and later released to the

load, using the magnetics like an inductor. In a forward and push pull DC/DC converter the energy goes directly through the magnetics to the load without using the magnetics components as an intermediate storage. Another criteria for the DC/DC converter is the acceptable range of the input voltage. The wider the possible range to guarantee operation, the fewer DC-link capacitors are required, which saves on space and cost, but it might but limitations on the design of the converter. A wider input range is required to satisfy the hold-up time criteria, which means that even if there is no power from the mains for a specific timeframe, the converter has to keep up the output power. During that time the energy stored in the DC-link capacitors is utilized resulting in a decreasing voltage across the DC-link capacitors, while the output voltage still has to be maintained at full load for the required hold-up time.

3.6.1 Flyback converter

The flyback converter is similar to the buck-boost converter just with two windings on the inductor to provide isolation, see Fig. 3.13. The simplicity and low component count make the flyback a frequent used topology for the lower power ranges. For higher powers the flyback is usually not a good choice and other topologies are therefore chosen. Reason for this is the stored energy in the leakage inductance, which also increases the stress for the primary switch. The operation principle is to store energy in the magnetics during the time when the switch is on, while reverse biasing the diode. If the switch is off, the current can not flow on the primary, but the current must continue to flow, so the diode on the secondary becomes forward biased and the energy is transferred to the output. The operation is similar to the operation of a buck-boost converter with the difference of the coupled inductor. Together with the stray inductance of the tracks, the transformer leakage inductance and the output capacitance of the switch a LC series resonance circuit is formed, which might lead to high voltage spikes at the turn off introducing the need for a snubber circuit to protect and lower the stress of the primary switch. To limit the loss in the snubber circuit the frequency cant get too high, which on the other hand increases the size of the magnetic component to store more energy. Usually flyback converters are only used for power supplies up to 250 W of output power due to the above mentioned reasons and the cost factor. By replacing the diode on the secondary side with a switch it is even possible to operate in a quasi-resonant operation reducing the on-turning loss further by valley switching or even zero voltage switching by reversing the current on the secondary side. This operation is also possible for the standard configuration of the flyback in Fig. 3.13 by replacing the diode with an active controlled switch. There exists another solution of a dual flyback converter, which works if the output voltage is lower than the primary side voltage [30, 44], see Fig. 3.14 for the schematic of the primary side. The secondary side

is not drawn since its identical to the conventional flyback in Fig. 3.13. This configuration allows to feed the energy stored in the leakage inductance back to the source.

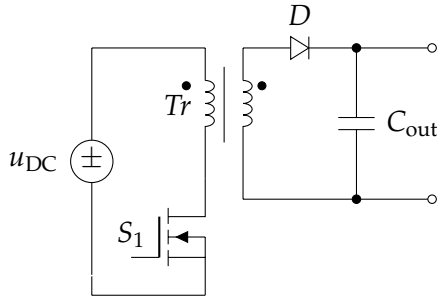


Figure 3.13: Schematic of a flyback converter.

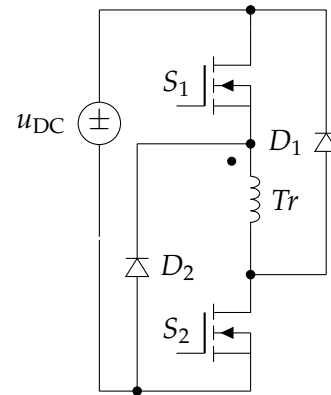


Figure 3.14: Dual switch flyback converter (primary side only).

Advantages: The flyback is simple to control and has the lowest component count, which makes it cheap and also offers isolation. Additionally no output inductor for filtering is required.

Disadvantages: It is only viable for lower output powers due to the too high cost compared with other topologies at higher power levels. If synchronous rectification should be used, special care has to be taken for the voltage spike at the turn-off event.

3.6.2 Forward converter

The forward converter is also called the working horse of power electronics. It passes contrary to the flyback converter the input energy directly to the output without using the magnetics components as an intermediate energy storage. The schematic is shown in Fig. 3.15 where it can be observed that it looks similar to the dual switch flyback converter. The additional diode D_4 on the secondary side is needed as freewheeling diode for the output filter.

For the time equivalent of the duty cycle both switches are switched on building up a magnetizing current in the transformer and are then switched off again. During the off-time of the switches the magnetizing current flows back into the source, which is here the DC-link capacitor, bringing the magnetizing current again down to zero therefore preventing the transformer from running into saturation. The diodes on the secondary side can be replaced with MOSFETs for synchronous rectification to increase the efficiency. The drawbacks of this converter are the only uni-directional utilization of the transformer and due to the hard switching of the primary switches the switching frequency and therefore the

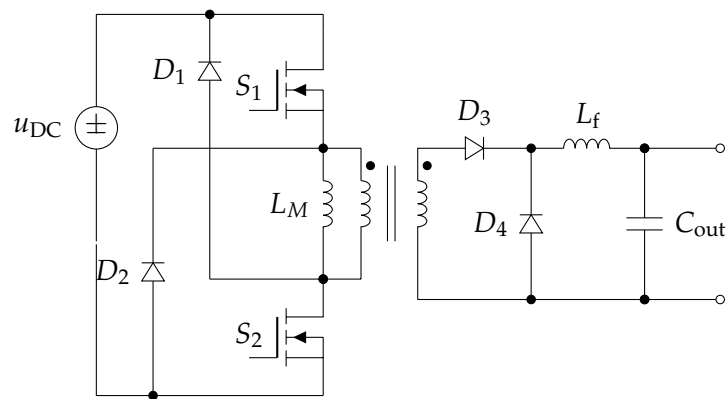


Figure 3.15: Two transistor forward converter.

power density is limited.

Advantages: Again as the flyback the advantage of a simple control and it can also be used for higher powers.

Disadvantages: The two transistor forward converter has a higher switch count than the flyback converter and an output filter is needed. Also the transformer is only utilized uni-directional.

3.6.3 Phase-shifted Zero-Voltage-Switched bridge

The PS-ZVS bridge is a push pull converter, which is similar to the forward converter. It can be build in a half bridge configuration, saving two switches in addition of a capacitive voltage divider, which is usually done for lower powers, since then only half the voltage can be applied across the transformer, but requiring double of the current, or in a full bridge configuration with four switches on the primary side, see Fig. 3.16. The name of the circuit derives of the possibility to switch every switch on at zero voltage, resulting in low turn-on loss even at high switching frequencies. The secondary side can be in a center tap configuration, see Fig. 3.16 or in a current doubler configuration , see Fig. 3.17.

The current doubler configuration has the disadvantage of requiring two output inductors, but the current through each inductor is only half the current of the center tapped configuration. Also the frequency of the current through the inductors is the switching frequency, compared to the center tap configuration, where the current through the output inductor has double the switching frequency. Usually the current doubler configuration is more efficient for high output current applications (greater than 100 A) and since there is no center tap for the transformer needed, the transformer construction is easier and not so expensive.

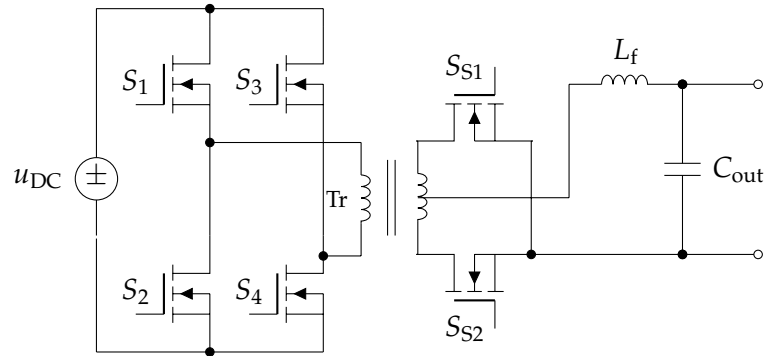


Figure 3.16: Schematic of a PSZVS bridge with center tap configuration on the secondary side.

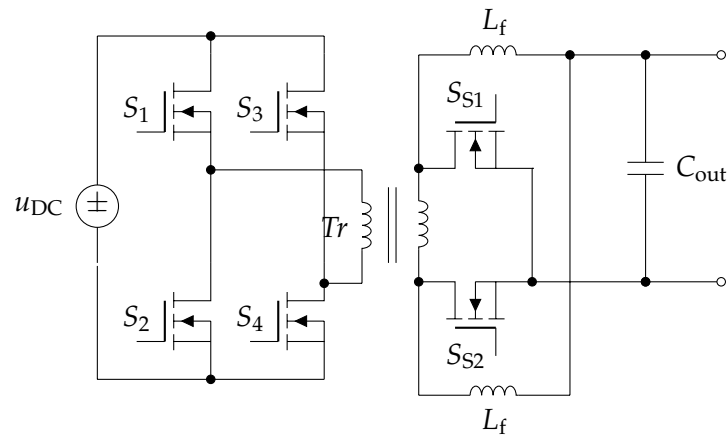


Figure 3.17: Schematic of a PSZVS bridge with current doubler configuration on the secondary side.

A big advantage for the PS-ZVS bridge is the relatively simple implementation of a fixed frequency control, therefore it is well known and widely distributed in industry. The PS-ZVS bridge can achieve high efficiencies at medium to high loads. At low loads the stored energy in the leakage inductance of the transformer might not be high enough to achieve full ZVS switching, failing to discharge the output capacitors of the MOSFETs, introducing turn-on losses at low load and voltage spikes across the switches. A solution for this is for example the introduction of an additional inductor in series with the transformer primary to be able to store more energy and to achieve zero voltage turn-ons even at low load. The price for this additional inductor is not only increased cost and additional required space but it also limits the slope of the current through the transformer every time the current polarity is changed, limiting the maximum power which can be transferred. Another possibility to achieve zero voltage turn-ons for the primary switches under lower load conditions is the utilization of MOSFETs with smaller chip size to lower the output capacitance, with the disadvantage of also increasing the on-resistance and thus also the conduction losses.

Advantages: The PS-ZVS bridge has a simple fixed frequency control scheme and promises high efficiency for the medium to high load range. Due to the soft on-switching of the primary MOSFETs higher operating frequencies are possible compared to the two transistor forward converter for example, which can shrink the magnetic components.

Disadvantages: The turn-off of the MOSFETs is still a hard turn off, so some losses are generated here. At low load conditions special care has to be taken to still achieve full ZVS switching. Also during the turn-off of the synchronous rectifier switches, like for the above mentioned topologies, over-voltage spikes occur, requiring a snubber network. For the hold-up time criteria some efficiency during normal operation is needed to sacrifice to widen the allowed voltage input range.

3.6.4 LLC converter

With an LLC converter, where the name derives from the series connection of a resonance inductance, a transformer magnetizing inductance and a capacitor, it is possible to achieve zero voltage turn-on over the whole load range and nearly zero current turn-off (around the magnetizing current, depending if its running over- or under-resonant), by utilizing all parasitic elements in the circuit. Since there is nearly no switching loss in a LLC converter, high efficiency in combination with a high power density is possible. Basically the LLC switches at its series resonance frequency by alternating turning on the primary switches with a 50% duty cycle (including a small dead time to prevent shoot-through). During the

dead time the voltage across the switch which will be turned on next, will resonate to zero, so it can be switched on under zero voltage and the synchronous rectifiers switches can be turned on and off under zero current, which also eliminates over-voltage spikes at turn-off events across the synchronous rectifier switches. The control of the secondary switches is easy as long as the circuit runs on its resonance frequency, which means that the DC link voltage has to be constant and no gain or attenuation is needed. Because of the hold-up requirement for computer and server power supplies it can not be guaranteed that the input voltage (the DC link voltage) for the LLC is always constant. In the case that the LLC has to work aside from its resonance frequency making the control for the correct timings of the secondary synchronous rectifiers difficult, which is also a problem for dynamic load changes or at start up. Various control schemes for the LLC converter exist already. A big difference to the above mentioned DC/DC converters is that the control must be done with a frequency modulation instead of pulse-width modulation, usually operated near its resonance frequency f_0 . One method for this is to model the LLC with an approximation, the First Harmonic Approximation (FHA), assuming that the circulating current has only a single frequency and that it is purely sinusoidal [45], which is a good approximation if the circuit runs at its resonance frequency. With this method the non-linear non-sinusoidal model can be simplified into a linear sinusoidal model and the load dependent gain M_g can be calculated dependent on the frequency. Other recently research about controlling the LLC converter, especially in terms of minimizing the device stress during dynamic load steps, was concluded about optimal trajectory control, where the author demonstrated the response during various dynamically events ranging from a soft startup to load steps and burst mode control, [46, 47].

Advantages: The LLC converter promises highest efficiency of all presented converters paired with high power density and a wide input voltage range capability.

Disadvantages: With all the above mentioned advantages, the LLC has the disadvantage that the control is by far the most complex. There exists already commercially available controllers for the LLC, but with fast dynamic load changes the LLC is still a challenge.

3.7 Conclusion

To reach the efficiency, especially for a high efficiency over the whole load range, soft switching is a required criteria for the PFC and for the following DC/DC stage. Further for the PFC stage a bridgeless topology looks most promising to reduce the amount of semiconductors through which the current flows at a time. Since diodes have a reverse recovery charge (in case of inexpensive SiC diodes) and a forward voltages drop, a topology

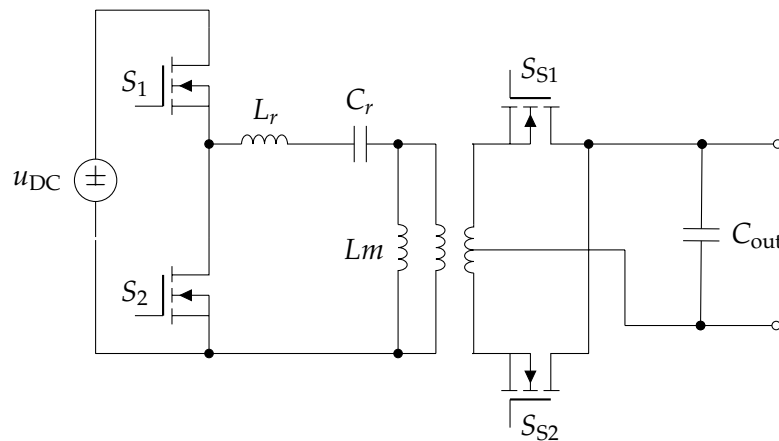


Figure 3.18: Schematic of a LLC half bridge converter with center tap at the secondary.

with just MOSFETs is preferred. Therefore for the PFC stage the TCM topology was chosen, since the current always flows through only two MOSFETs at a time and a ZVS turn-on is always possible. For the DC/DC stage the LLC is probably in terms of efficiency and power density the best choice but it is also the most complicated topology in terms of control and is therefore not so reliable. For a more reliable and simpler demonstrator therefore the PS-ZVS full bridge was chosen. Simulations before building the demonstrator promised furthermore that the PS-ZVS bridge is adequate to achieve the desired efficiencies for titanium level over the whole load range.



Proposed solution for a wide-range input power supply

4.1 Introduction

The key idea behind the thesis is the utilization of low voltage MOSFETs like the OptiMOS™ [48], which offer a better FOM in comparison with high voltage MOSFETs like CoolMOS™. This idea picked up lately more attention in the research to further increase the limits of efficiency and power density [15, 16, 49, 50]. Here two identical modules are re-configured dependent on the mains voltage, either both operating in serial and capacitively dividing the grid voltage for high line input or operating in parallel for low line input. To keep the power density as high as possible with this approach only two modules were chosen each being able to deliver 500 W of output power at 12 V. The parallel configuration at low line input when both stages operate in parallel is illustrated in Fig. 4.1 and for high line input both are stacked in series, see Fig. 4.2. In this configuration the efficiency of one module is equal to the total efficiency, since every module always works with the same input voltage. Each module consists of a TCM resonant PFC circuit [39–43] (TCM-PFC) with a PS-ZVS full bridge as an isolating DC/DC converter afterwards which has a center tap rectification on the secondary side. To supply the gate driver, control and measurement circuits with all the required different and isolated voltages an auxiliary supply in form of a quasi-resonant flyback was chosen, which is as well integrated into each module. The schematic for a single module, as shown in Fig. 4.3, shows the circuit comprises of an interleaved TCM PFC, a DC Link capacitor and a PS-ZVS bridge for DC/DC conversion. The input capacitor used for the capacitive voltage division is relatively small (here 4.7 μF) to minimize the phaseshift between the line voltage and the input current and as well save space and cost. Fig. 4.4 shows an image of the prototype for one module. It is constructed in a way that two modules can be stacked into each other, minimizing the total required volume.

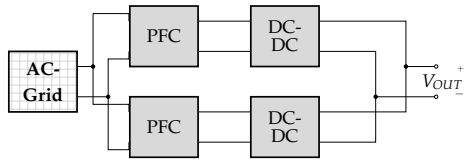


Figure 4.1: Proposed principle schematic for low line input.

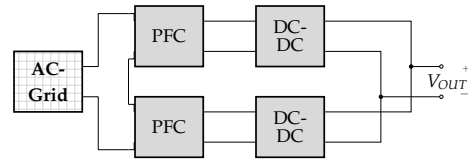


Figure 4.2: Proposed principle schematic for high line input.

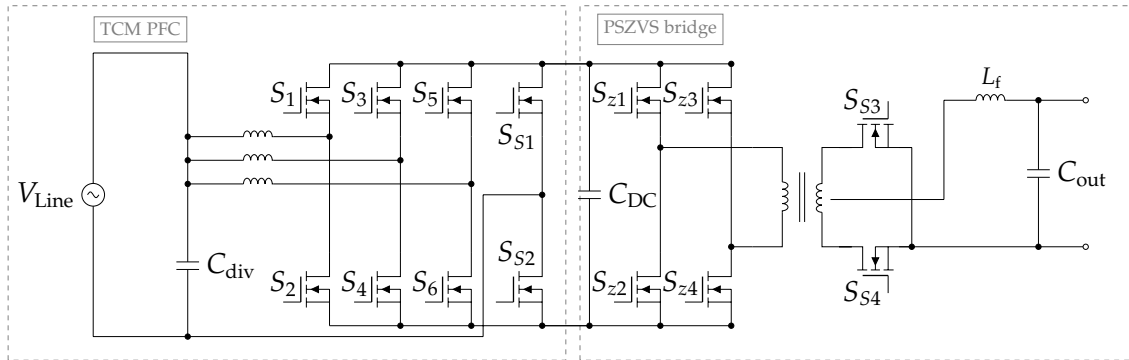


Figure 4.3: Basic schematic for a single module consisting of the resonant triangular current mode PFC and a PS-ZVS bridge with center tapped rectification on the secondary side.

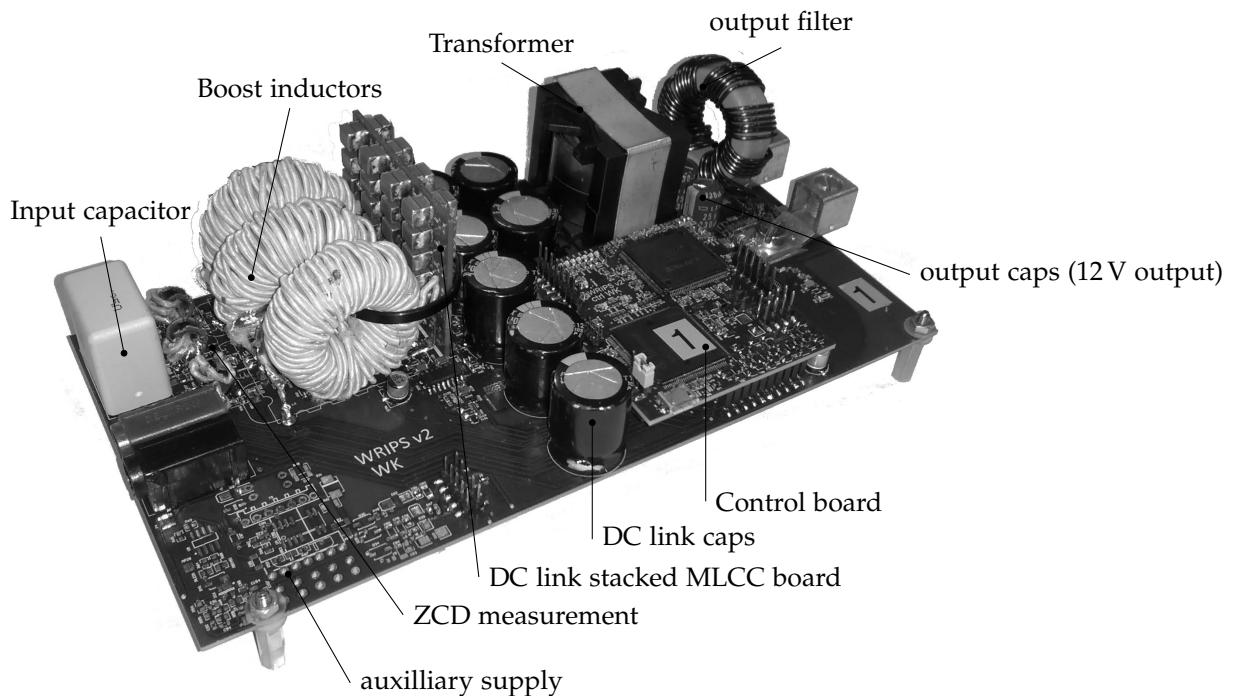


Figure 4.4: Image of the prototype (one module).

For the re-configuration between high and low-line input, relays or semiconductor switches can be utilized, which requires a minimum of three bidirectional blocking switches. In case of relays the switches add nearly zero additional conduction loss. The schematic for this is shown in Fig. 4.5, [51].

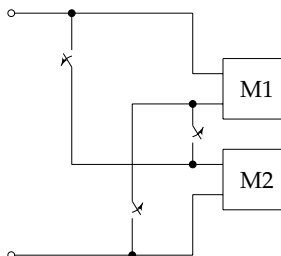


Figure 4.5: Schematic for switching the modules between serial and parallel connection.

The operation principle of the TCM PFC with the possible switch states and their equations, as well how a zero voltage turn-on can be achieved will be presented in section 4.2 followed with details about the control implementation, explained on the basis of block diagrams. At the end of the chapter measured results from the prototype in contrast to simulated results are shown. For the DC/DC converter the PS-ZVS bridge is explained in section 4.3 starting with its basic operation and explaining the different possible phases. To reduce conduction loss, which is essential for a high efficiency power supply with a low voltage output, synchronous rectification on the secondary side is mandatory followed with an explanation of the overvoltage spikes at the turn-off of the synchronous rectification switches and how to reduce them to be able to use lower voltage devices with a better FOM. For preventing a run-away of the flux in the transformer of the DC/DC converter from unequal excitation the used method is presented in section 4.3.4.1 and details about the transformer construction and how to increase the stray inductance to achieve zero voltage turn-ons down to low loads is illustrated in section 4.3.5.

4.2 Triangular current mode PFC rectifier

Regulations require that the input current has the same sinusoidal waveform shape as the line input voltage, therefore a PFC is mandatory for SMPS. In this chapter the required specifications for the PFC and the basic operation of the TCM PFC is presented with a way to pre-calculate the switch timings to control the converter in a predictive way. The individual control loops are explained with a short explanation how it was implemented inside the microcontroller and the Field Programmable Gate Array (FPGA). Since the converter can operate in series with another module all the voltage measurements are required to be isolated. The zero current events from the boost inductors, which are required by the control method, are measured naturally isolated with saturating transformers [52].

4.2.1 Introduction and basic operation

The basic operation of the TCM PFC is shown on the basis of the switching pattern for the current through the boost inductor in Fig. 4.6 with the equivalent simplified circuit with only one phase and a DC input source in Fig. 4.7.

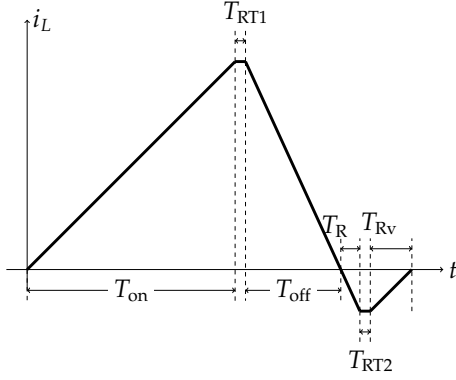


Figure 4.6: Basic triangular current waveform of the PFC [39].

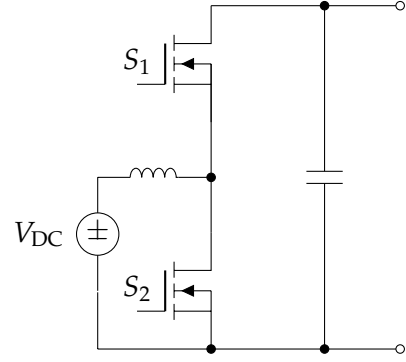


Figure 4.7: Equivalent simplified circuit for the TCM PFC.

One switching cycle consists of a charging period of the inductor (T_{on}, T_{Rv}), two resonant transitions (T_{RT1}, T_{RT2}) and a discharging period (T_{off}, T_R). The MOSFETs have a nonlinear voltage dependent output capacity C_{OSS} , see Fig. 4.9. During the resonant transitions the voltages across the switches decrease or increase (depending on the resonant transition and switch) in an S-shape, see Fig. 4.8, because of the nonlinear output capacitance C_{OSS} . When the output capacitor is discharged, the voltage across the MOSFET is zero and it is possible to turn it on without losing the stored charge in the output capacitance, which would be lost in a hard switched topology. [42]

1. At the beginning switch S_2 is on and the boost inductor is charging.
2. After T_{on} , S_2 is switched off and both switches are off for the resonant time T_{RT1} . During the resonant time the inductor current charges both parasitic nonlinear voltage dependent output capacitors C_{OSS} of the MOSFETs. During T_{RT1} , the voltage across S_2 is increasing and the voltage across S_1 is decreasing to zero like a S-shape.
3. When the voltage reaches zero, S_1 is switched on for the duration of T_{off} and T_R de-energizing the boost inductor and reversing the current after T_{off} .
4. After the time T_R switch S_1 is switched off. For input voltages below half the DC-link output voltage no negative current is required to achieve zero voltage switching (ZVS) and S_1 can be switched off at zero current, while it is still possible to discharge the output capacitor of S_2 for a zero voltage turn on. For input voltages higher than half

the DC-link voltage, S_1 is on for an additional time T_R energizing the boost inductor with a negative current in resulting that a ZVS turn-on can be achieved again.

5. After switching off S_1 , the second resonant transition starts, which increases the voltage across S_1 like a S-shape (see Fig. 4.8) and decreases the voltage across S_2 like a S-shape.
6. S_2 is turned on again, energizing the boost inductor. After T_{RV} the current in the boost inductor is zero again. From here on the phases 1 to 6 are repeated again.

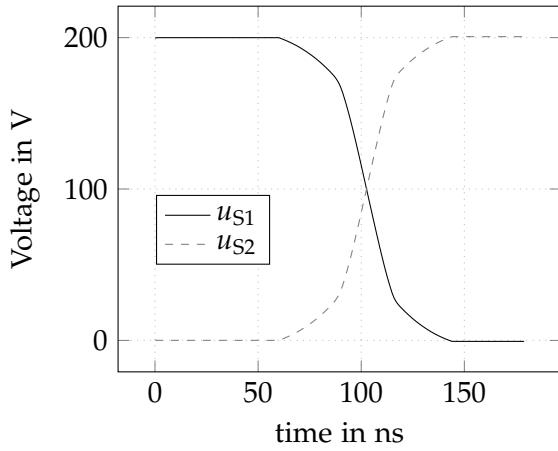


Figure 4.8: S-shape like voltages across the MOSFETs for a resonant transition (S_2 was on and is switched off).

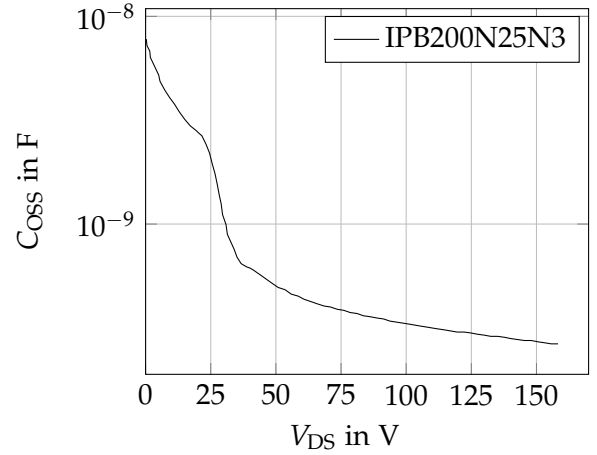
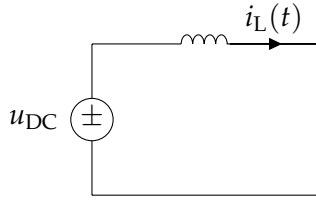


Figure 4.9: Output capacity over V_{DS} from an 250 V Optimos 3 ($20\text{ m}\Omega$).

The mathematical description of the different phases during the operation of the PFC explained above is given below. This equations show how the timings can be pre-calculated by the control. [42]

4.2.1.1 Phase 1

In phase 1 the lower switch S_2 is turned on. The current rises in a linear way energizing the inductor. The input and output voltage during this phase are assumed to be constant, which is also a true assumption later in case of a sinusoidal input voltage, since the switching frequency is much higher than the line frequency. Neglecting the inductor resistance and the on-resistance of the switch S_2 the equation for the inductor current can be written with eq. (4.1). After the specific time T_{ON} the current i_L in the inductor has reached its peak value.

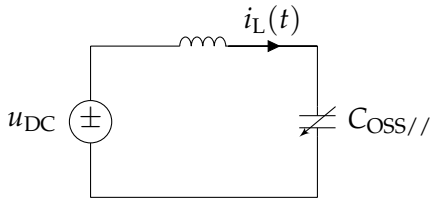


$$i_L(t) = \frac{u_{DC}}{L} \Delta t + i_L(t = 0). \quad (4.1)$$

Figure 4.10: Equivalent circuit for energizing the boost inductor in phase 1.

4.2.1.2 Phase 2

After T_{ON} the lower switch S_2 is switched off and both switches are in blocking state. Due to the energy stored in the inductor the output capacitor of the lower switch S_2 is charged and the output capacitor of the upper switch S_1 is discharged, as is described with eq. (4.2), which is the equation for a series resonance circuit, see Fig. 4.11 for the equivalent circuit. This is the first resonant transition where the output capacitance C_{OSS} is non-linear and voltage dependent, it can only be solved iteratively for an exact solution. The capacitor $C_{OSS//}$ is the equivalent output capacitance of the two output capacitors of the upper and lower MOSFET in parallel, but the capacity gets a shape like a cup, because as the voltage across one switch increases, it decreases across the other switch, see Fig. 4.12. The initial conditions for the second order nonlinear differential equation in this phase are the peak inductor current i_{LP} which is stored in the inductor after phase 1 and the voltage across $C_{OSS//}$, which is assumed to be zero.



$$u_{DC} = L \cdot \frac{di_L(t)}{dt} + u_C(t) \quad (4.2)$$

$$i_L(t) = C_{OSS}(u_C(t)) \cdot \frac{du_C(t)}{dt}.$$

Figure 4.11: Equivalent circuit for the first resonant transition in phase 2.

4.2.1.3 Phase 3

In this stage the boost inductor is de-energizing itself to the DC-link and the current is falling linearly. To reduce the conduction loss due to the forward voltage drop of the internal body diode and the reverse recovery charge the upper switch S_1 is turned on, optimally right before its body diode starts to conduct. In case that the input voltage is lower than half the DC-link voltage a zero-voltage turn-on after a resonant time can be

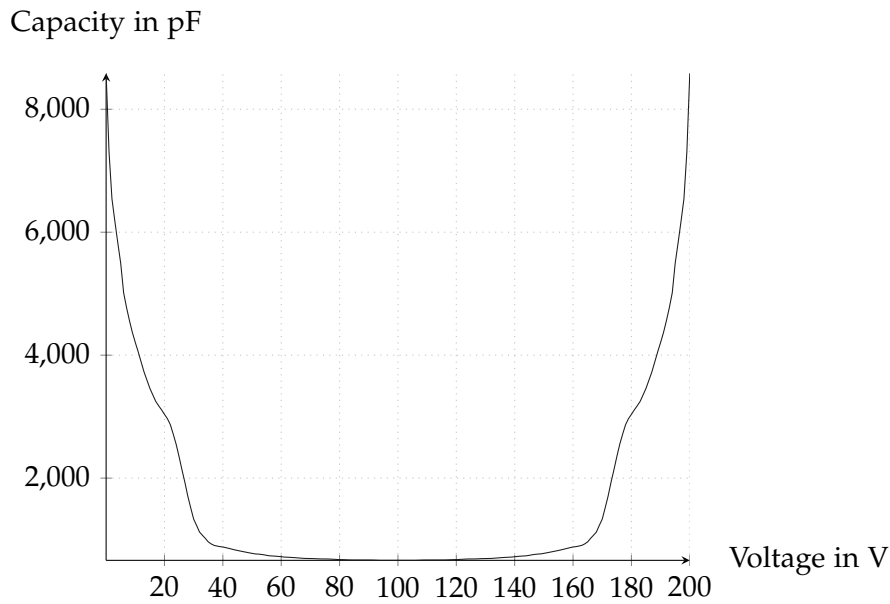
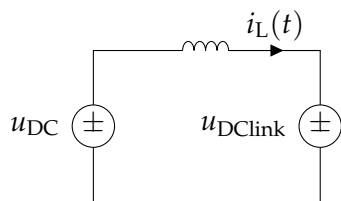


Figure 4.12: Equivalent capacity $C_{OSS//}$ for the differential equation, with the shape of a cup (250 V OptiMOS 3, 20 m Ω).

achieved. In case of a higher input voltage than half the DC-link voltage the T_{OFF} time has to be extended for a time T_R until a specific negative current flows through the inductor to enable later a zero-voltage turn-on of S_2 . The minimum required negative current and with that the minimum time T_R is an optimization problem which can be calculated as is shown later in this section. The equivalent circuit is shown in Fig. 4.13 and the differential equation is similar to the one of phase 1, see eq. (4.3). The initial condition for the inductor current is the current in the inductor after phase 2.



$$u_{DC} - u_{DClink} = L \cdot \frac{i_L(t)}{dt}. \quad (4.3)$$

Figure 4.13: Equivalent circuit for phase 3 where the boost inductor is de-energized.

4.2.1.4 Phase 4

In this phase, where the second resonant transition occurs, both switches are switched off again to discharge the output capacitor of the lower switch for a zero-voltage turn-on later.

The equivalent circuit and the differential equations are identical to phase 2, see Fig. 4.11, except that the initial conditions differ from phase 2. Dependent on the off-time the initial inductor current is either zero or negative and the voltage across the non-linear output capacitor is now the DC-link voltage.

4.2.1.5 Phase 5

Phase 5 is identical to phase 1 from the equations and from the equivalent circuit. It just defines the time needed from phase 4 to reach again an inductor current of zero, which changes the initial condition of the inductor current to the value it has after phase 4.

The average current of the PFC for one phase \bar{i}_{ph1} is the average current through the boost inductor, which can be expressed with the period T_P , the positive peak current after energizing the inductor \hat{i}_p and the negative peak current after the time T_R before the second resonant transition \hat{i}_N . Since the resonant transitions are very short they can, for simplicity, be neglected, see eq. (4.4).

$$\bar{i}_{\text{ph1}} = \frac{1}{T_P} \left(\frac{\hat{i}_p \cdot T_{\text{on}}}{2} + \frac{\hat{i}_p \cdot T_{\text{off}}}{2} + \frac{\hat{i}_n \cdot T_R}{2} + \frac{\hat{i}_n \cdot T_{Rv}}{2} \right). \quad (4.4)$$

The average current \bar{i}_{ph1} is always proportional to the line voltage and the calculation of the required timings T_{on} , T_{off} and T_R is presented in section 4.2.3.5, where time T_{Rv} is included into T_{on} . [53]

4.2.1.6 Optimal (minimum) negative inductor current

As mentioned previously for input voltages greater than half the output voltages a negative current after phase 3 is needed to achieve a ZVS turn on of switch S_1 for the simplified DC case here. A minimum required negative current can be calculated, which helps especially at higher load conditions to reduce the conduction loss by minimizing the average current through the PFC. To calculate the minimum required current for the equivalent circuit of Fig. 4.11 differential equation eq. (4.5) can be solved.

$$-u_{\text{DC}} + LC \frac{d^2 u_c(t)}{dt^2} + u_c(t) = 0. \quad (4.5)$$

Solving this second order linear differential equation and replacing the non-linear output capacity with a charge-equivalent linear one C_{qe} , see eq. (4.6), the voltage across the capacitor leads to eq. (4.7) with the initial conditions at $t = 0$ of $i(t = 0) = i_{L0}$ and $u_c(t = 0) = u_{\text{DC}}$.

$$C_{qe}(U_{DC}) = \frac{1}{U_{DC}} \int_0^{U_{DC}} C_{OSS}(u_{DS}) du_{DS}. \quad (4.6)$$

$$u_c(t) = (u_{DC} - u_N) \cos(\omega t) + \frac{i_{L0}}{\omega C_{qe}} \sin(\omega t) + u_{DC} \quad (4.7)$$

with $\omega = \frac{1}{\sqrt{LC_{qe}}}$.

The minimum negative current to reach zero voltage across the capacitor can be now written as an optimization problem, where the goal is to minimize the voltage across the capacitor to zero with an minimum initial current i_{L0} , which is the negative current before the resonant transition.

$$\begin{aligned} & \underset{i_{L0}}{\text{minimize}} && u_c(t)^2 + i_{L0}^2 \\ & \text{subject to} && u_c(t) = (u_{DC} - u_N) \cos(\omega t) + \frac{i_{L0}}{\omega \cdot C_{qe}} \sin(\omega t) + u_{DC} \\ & && i_{L0} \geq 0. \end{aligned} \quad (4.8)$$

This optimization problem cannot be solved online because of the limited computational power of the microcontroller. One idea was to solve it in advance and store the results for the required minimum negative current in a 3D - Look Up Table (LUT) (see Fig. 4.14) with interpolation. It can be investigated that the optimum negative current depends only on the DC-link voltage and the input voltage.

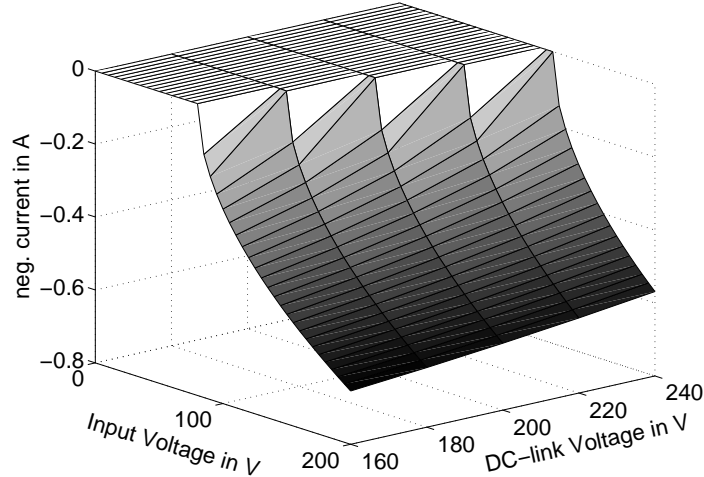


Figure 4.14: LUT for the minimum required negative current over the input voltage and DC-link voltage, calculated for a $20 \text{ m}\Omega$ OptiMOS 3, 250 V.

Using these values for the negative current would minimize the conduction loss and the switching frequency. The only drawback is the additional needed computation power

for looking up and interpolating the required negative currents. Using always a constant negative current which is high enough for the worst case (highest input voltage and minimum DC-link voltage) skips this calculation/interpolation and saves computation power. To reduce the switching frequency especially at low load conditions the negative current over half a main period can be increased or decreased in dependence of the actual load which requires a higher negative current for low load to decrease the switching frequency which creates a better balance between conduction and switching loss. Further it has to be mentioned that a small negative current is in reality always required since the zero current measurements of the boost inductor with the saturable transformer core would not work reliable enough otherwise.

4.2.2 PFC component selection

For the PFC three components which cover the DC-link capacitor, the boost inductors and the MOSFETs have to be selected to deliver high efficiency and additionally design requirements like a minimum hold-up time have to be met. For selecting the boost inductors a maximum viable inductance is calculated and with that inductance and the peak current through the inductor cores can be found and optimized. The main requirement for the DC-link capacitor is to store enough energy to achieve the hold-up time, which is also connected to the minimum allowed input voltage for the following DC/DC converter. Secondary goals are a low Equivalent Series Resistance (ESR), low leakage current loss, low volume and high ripple current capability. For the switches low voltage MOSFETs were selected and it was differentiated between the fast switching MOSFETs for the boost operation and the slow switching MOSFETs for the rectification of the line voltage.

4.2.2.1 Boost inductors

For selecting the boost inductor the core losses and the copper losses have to be considered. The core losses depend on the frequency of the current and the see eq. (4.9). A good guess for the value of inductor is possible by defining the minimum allowed switching frequency, see Fig. 4.15.

$$\Delta i_L = \hat{i}_p + \hat{i}_n. \quad (4.9)$$

The average input current $i_{in}(t)$ can be defined with eq. (4.10).

$$\hat{i}_{in}(t) = \frac{\hat{i}_p - \hat{i}_n}{2}. \quad (4.10)$$

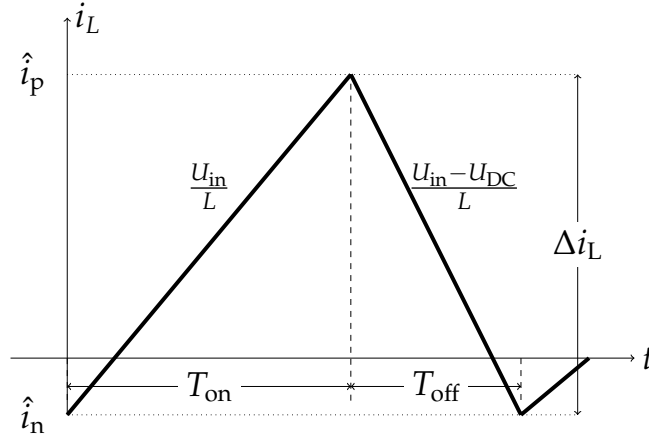


Figure 4.15: Sketch for calculating the boost inductor value for limiting the minimum allowed switching frequency.

The period can be calculated by neglecting the relative short resonant timings, leaving only t_{on} and t_{off} for the total period T_p , see eq. (4.11).

$$T_p = \frac{\Delta i_L \cdot L}{U_{in}} + \frac{\Delta i_L \cdot L}{U_{DC} - U_{in}}. \quad (4.11)$$

With the combination of eq. (4.10), eq. (4.9) and eq. (4.12) and inserted into eq. (4.11) the maximum allowed inductance for a specific minimum switching frequency can be calculated, see eq. (4.13). The minimum switching frequency was selected to be well out of range of the audible frequency. This lowest switching frequency is reached during the condition of the highest load per phase and during the time of the highest mains voltage

$$P_{in} = \frac{P_{out}}{\eta} = U_{in} \cdot I_{in} = U_{in} \cdot \frac{\hat{I}_{in}}{\sqrt{2}} \quad (4.12)$$

$$L_{max} \leq \frac{\eta U_{in}^2 (U_{DC} - U_{in})}{2U_{DC} \cdot f_{min} (P_{out} \sqrt{2} + \hat{I}_{in} \cdot U_{in} \cdot \eta)}, \quad (4.13)$$

where the for the voltages U_{in} and U_{DC} their effective values are inserted, η is the expected (guessed) efficiency, f_{min} is the minimum allowed switching frequency, P_{out} is the maximum output power for one phase and \hat{I}_{in} is the peak negative current. With the calculated value for the chosen inductance the current waveforms for each load were calculated and with them it is possible to select a suitable core. For the core the material of choice was Molypermalloy Powder (MPP) and for a few selected cores, which were able to support the required ampere-turns without a too high drop of inductance at peak current, the losses were compared. The magnetomotive force θ can be calculated with eq. (4.14), where N is

the amount of required turns, \hat{i}_p is the calculated peak current through the inductor and A_L is the core specific inductance constant in nH/T²,

$$\theta = N \cdot \hat{i}_p \leq 0.8 \cdot A_L. \quad (4.14)$$

After some suitable cores were found for each one the expected copper and core losses were calculated and compared as shown in chapter A.

4.2.2.2 DC-link capacitors

The DC-link capacity defines first the amplitude of the DC-link voltage ripple, especially at higher loads, and secondly the hold-up time. The hold-up time is the time the power supply can supply full power to the output during an interruption of the mains, usually measured in milliseconds. The hold-up time requirement for the prototype was set to 10 ms, meaning during a missing half-wave of the mains at full load the output power can still be maintained. The DC-link capacity defines how fast the DC-link voltage drops when no input power is supplied and the second stage DC/DC converter can not deliver the maximum output power, if the DC-link voltage falls below a certain level. The DC/DC converter was designed to be able to deliver full output power down to a DC-link voltage of U_{DCmin} . This constraint from the DC/DC converter defines automatically the minimum required capacitance from the DC-link capacitors. By solving the differential equation for a RC circuit eq. (4.15) can be derived, which delivers the minimal value for the DC-link capacitor

$$C_{DClink} = \frac{t_{Hold-up}}{R \cdot \ln\left(\frac{U_{DCmin}}{u_{DC}}\right)}, \quad (4.15)$$

where $t_{Hold-up}$ is the required hold-up time, R is the equivalent resistance seen at the DC-link for dissipating the full load energy, U_{DCmin} is the minimum allowed DC-link voltage where the DC/DC converter is still able to deliver full output power and u_{DC} is the DC-link voltage during normal operation. To improve further the efficiency by reducing the ESR the DC-link capacitor is divided into electrolytical capacitors and Multi Layer Ceramic Capacitor (MLCC)s. The MLCCs help firstly to reduce the ESR and additionally they help to reduce the stress due to the ripple current for the electrolytical capacitors. If MLCCs are used the voltage dependent capacity has to be considered, since the capacity drastically reduces with the voltage, see Fig. 4.16.

For incorporating a larger number of MLCC an additional board like a ram-stick was constructed, where a larger number of MLCC can be located without using up much volume. MLCC have beside the lower ESR compared to electrolytic capacitors also a much lower leakage current and can withstand much higher ripple currents.

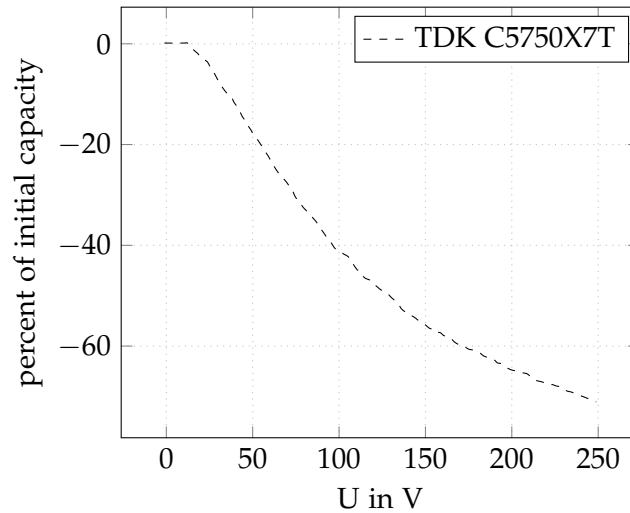


Figure 4.16: Loss of initial capacitance in percent over the DC-bias voltage for MLCC.

4.2.2.3 MOSFETs

For the switches criteria like the maximum blocking voltage, the on-resistance and the gate charge are the most important factors. Usually a power supply which has to operate at high and low line uses at least 500 V MOSFETs. The advantages of utilizing low voltage MOSFETs instead of high voltage MOSFETs were already shown in chapter 2. The new approach enables the usage of 250 V MOSFETs. This alone dramatically restricts the choice due to available MOSFETs for that voltage class, as shown in Tab. 4.1.

Table 4.1: Available MOSFETs for the required breakdown voltage from Infineon.

Device	R_{DSon}	Q_g
OptiMOS 250 V	20 m Ω	64 nC
OptiMOS 250 V	60 m Ω	22 nC

The lower the on-resistance the higher is the output capacitance and the gate charge of the MOSFETs. With the output capacitance of the device the required negative current can be calculated, see chapter 4.2.1.6. Knowing the minimum required negative current to achieve a zero voltage turn-on at times of the largest input voltage and knowing as well the inductance of the boost inductor, the waveform for a period of the mains for all possible loadpoints can be calculated and the MOSFET which suits better can then be selected, see chapter A.1. For the rectification of the low frequency sine wave two switches are needed for synchronous rectification which switch with the line frequency that is relatively low compared to the switching frequency of the fast switching MOSFETs. To reduce the conduction loss of the synchronous rectifier switches, several switches were paralleled.

Theoretically a large number of switches can be paralleled and the efficiency would get better and better, the only limiting factors are cost and space. The optimum number of paralleled switches can be found by comparing the conduction loss with the gate loss. Due to the low switching frequency the gate loss, which is load independent, is relatively low compared to the conduction loss therefore the worst-case scenario is for the 10% load condition, where the conduction loss is the lowest. With the current waveform from Fig. 4.15 the effective value for the current inductor current, dependent on the required negative current can be calculated, see eq. (4.16), where the peak-current i_p can be calculated with eq. (4.17).

$$i_{Leff} = \sqrt{\frac{1}{T_p} \int_0^{T_p} i_L(t)^2 dt} = \sqrt{\frac{1}{T_p} \left[\int_0^{t_{on}} \left(\frac{U_{in}}{L} t - \hat{i}_n \right)^2 dt + \int_0^{t_{off}} \left(\frac{U_{DC} - U_{in}}{L} t + \hat{i}_p \right)^2 dt \right]}. \quad (4.16)$$

$$\hat{i}_p = \frac{P_{out}}{\eta U_{in}} \sqrt{3} + \hat{i}_n. \quad (4.17)$$

The total losses can be calculated with eq. (4.18), where n is the amount of paralleled devices and f_N is the line frequency and the loss graph is shown in Fig. 4.17.

$$P_{vSR} = i_{Leff}^2 \frac{R_{DSon}}{n} + 2Q_g \cdot U_{Gate} \cdot n \cdot f_N. \quad (4.18)$$

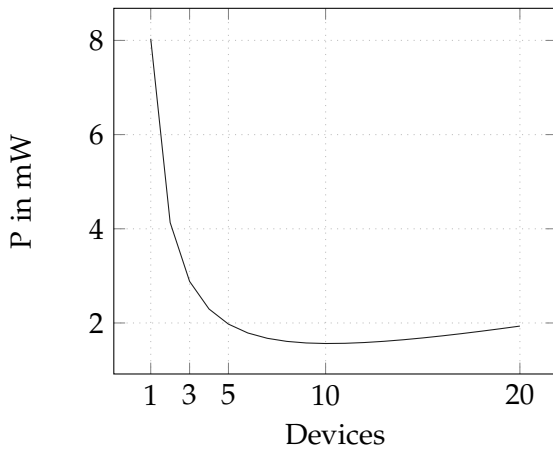


Figure 4.17: Loss of the PFC synchronous rectifier loss over the switches for 10% load.

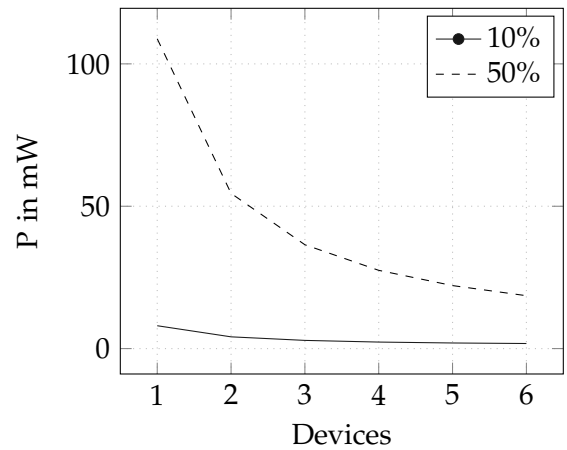


Figure 4.18: Loss of the PFC synchronous rectifier loss over the switches for 10% and 50% load.

Fig. 4.17 shows that the optimum number for the synchronous rectifier switches is already at 10 devices for 10% load, which would require alone for the synchronous rectification switches in total already 20 switches. Since the required space and cost have to be accounted as well, the amount of paralleled switches were chosen to only three. Fig. 4.18 compares the losses of the synchronous rectifier switches for 10% load and 50% load and shows that the higher the load the higher the number of switches can be chosen for lower losses, leaving the economic optimum aside.

For the fast switching MOSFETs the effective current per phase for each load was obtained from simulation and the turn-on events of the fast-switching MOSFETs were counted for the gate losses. With eq. (4.16) and $n = 1$ the $60\text{ m}\Omega$ and $20\text{ m}\Omega$ MOSFETs were compared and the result with the losses over the load are shown in Fig. 4.19. The $60\text{ m}\Omega$ device has steeper loss slopes due to the higher conduction losses, but the gate losses are only about a third compared to the $20\text{ m}\Omega$ device, which makes these two MOSFETs relatively identical. In the end the $20\text{ m}\Omega$ device was chosen, since the overall losses at the critical points of 20% and 50% were better. The advantage of the $60\text{ m}\Omega$ device at 10% is relatively small. Due to the relatively high switching frequency and therefore high gate loss, paralleling devices does not pay off here.

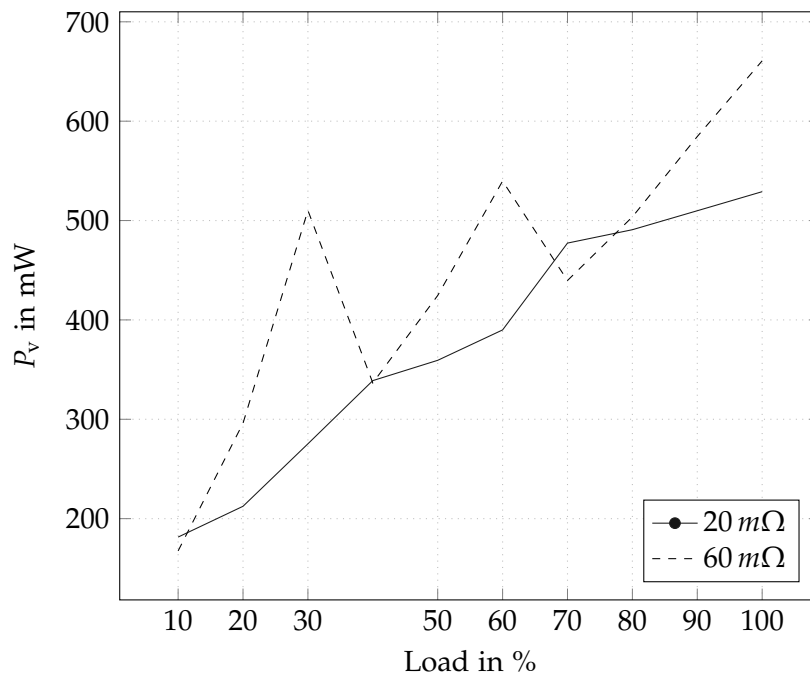


Figure 4.19: Loss of the PFC fast switches over the entire load.

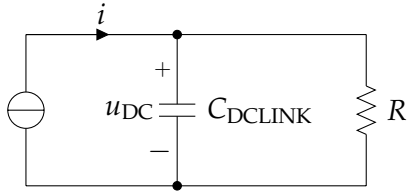


Figure 4.21: Schematic of the DC-link controller state space model.

$$\frac{du_{DC}}{dt} = -\frac{1}{R \cdot C_{DC}} u_{DC} + \frac{1}{C_{DC}} i. \quad (4.19)$$

Fig. 4.22. For stabilizing the DC-link voltage at the desired voltage, the desired DC-link voltage is subtracted from the actual DC-link voltage before it is multiplied with k_D . This control runs at 10 ms where the zero-crossings of the mains is used as the time base.

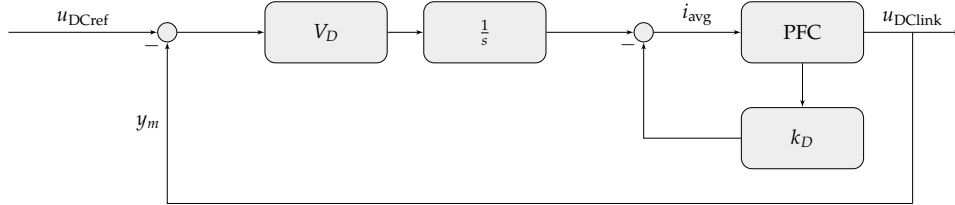


Figure 4.22: PFC DC-link voltage state space control scheme.

4.2.3.2 Phase shedding

In order to stay in a high efficiency region phases are added or removed depending on the load, which can reduce the amount of switching operations especially at low load conditions if the number of active phases is reduced. This is realized with a state machine which can add or remove one phase at a time at every zero crossing of the input voltage, which is done if the average input current i_{avg} multiplier exceeds a specified high or a low threshold. In case of exceeding the high threshold another phase (if available) is added and in case of exceeding the lower threshold a phase (if more than one is active) is removed. The thresholds are chosen to turn on the phases according to Tab. 4.2.

Table 4.2: Active phases for different loads.

Load in %	Phases
10-30%	1
30-60%	2
70-100%	3

4.2.3.3 Interleaving control

Since the input current for one phase consists of a high frequency triangular current modulated with the low frequency of the line voltage, a bigger EMI filter might be required to satisfy the regulations. In order to make the current more sinusoidal at higher loads when also more than one phase is active, a phaseshift between the active phases is introduced. The optimum phaseshift depends on the amount of active phases and can be formulated with eq. (4.20), where n is the number of currently active phases.

$$\phi = \frac{360}{n}. \quad (4.20)$$

The control scheme for achieving the phaseshift is outlined in Fig. 4.23. The reference phaseshift depends on the currently active phases, see eq. (4.20). The actual phaseshift between the first phase and the second or third phase i_{PhMeas} is measured inside the FPGA with a counter. The control is a P-controller which adds a limited signal u_{limit} to the required negative current, slowing down the phase to change the phaseshift in reference to the first phase which is also the master phase. This control concept has the limitation that it only works if the master phase has a slightly lower inductivity then the two slave phases, since then its running faster and the slaves can be slowed down compared to the master phase. To be able to control the phaseshift independent of the inductivities, the control had to be modified a bit more. The limiter limits the controller output u_{limit} to values between zero and $u_{limitMAX}$. In case that u is negative it would mean that the slave needs to be made faster, but this is not possible since it would reduce the negative current which is, to prevent failures by not achieving a zero voltage turn on, not allowed. In this case the master phase must be slowed down by increasing the negative current for the master phase. With this method the phaseshift between the phases can be controlled independently of the inductivities.

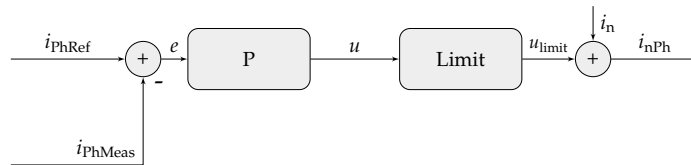


Figure 4.23: Phaseshift control for the PFC.

4.2.3.4 Capacitor voltage balancing

At high line input the modules operate in series where the voltage is divided capacitively with small input capacitors. Since each module has its own controller it can not be guaran-

ted that the capacitor voltages are always balanced, which mandates a control to balance the capacitor voltage and prevent failures due to voltage imbalances.

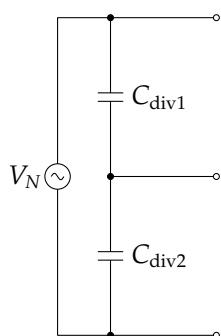


Figure 4.24: Capacitive voltage divider for high line.

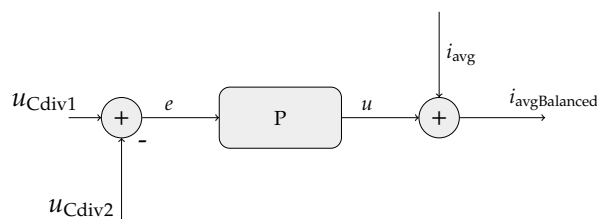


Figure 4.25: Voltage balancing control.

The balancing control (see Fig. 4.25) needs to measure the voltage across the second module which is the slave module. If the capacitor voltages are equal the balanced average current $i_{\text{avgBalanced}}$ is unmodified and equal to i_{avg} . If the voltages differ from each other the average current i_{avg} can be increased to decrease the voltage across the input capacitor and the other way the voltage can also be increased by reducing the average current. This adjustment of the average current is executed with every controller call cycle, which is for the demonstrator set to $50 \mu\text{s}$, which gives the possibility for a fast adjustment of the voltage across the capacitors to prevent any big imbalances. Fig. 4.25 shows that at least one controller must know the input voltage of both modules, which requires either some communication between the controllers to exchange the data of the input voltage measurement or an additional isolated voltage measurement. It is enough if only one module takes care about the voltage balancing, therefore only the master module has that control loop active in the demonstrator. During the development of the prototype it turned out that it is really important that both modules start and end the switching operation of the PFC synchronized at the same point of the input sine wave, to prevent a voltage difference across the input capacitors from the beginning of the operation. Without synchronization of the modules one module would start or stop a few microseconds earlier at the beginning or the end of the input sine wave due to measurement errors and not in synch running controllers, discharging the input capacitor where the module is active and charging the capacitor of the inactive module causing a non-controllable voltage difference at the start of each half-wave. Since the used sensors had to be isolated and shouldn't be too expensive the measurement itself is not accurate enough for a self-synchronized start of both modules. In fact the used error amplifiers had big non-linearity's which could be partly compensated with a first order polynomial but even with the compensation the solution with

just measuring the input voltage is not accurate enough. Another factor was that both controllers run independent from each other with a controller frequency of 20 kHz resulting in a period T_d of $50\mu s$ and the phaseshift between the controller calls varies randomly to each other, as pointed out in Fig. 4.26, where the rising flank represents the controller call. The initial phaseshift between both of the controllers varies randomly dependent only when they are powered up. Afterwards they still can change slightly since its not guaranteed that both crystal oscillators have the exact same frequency.

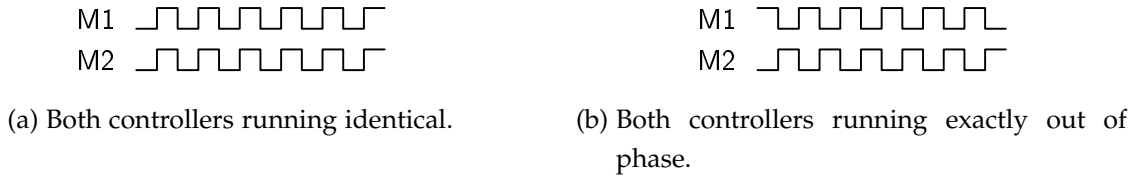


Figure 4.26: Controller call signals for both modules where the rising flank represents the controller call.

During each controller call the microcontroller sends the timings for the PFC to the FPGA. After the FPGA received valid switch timings it starts right afterwards with the switching operation. Therefore the worst case situation that can happen, under the assumption that the measurements are perfect, is that the start signal for the FPGA is up to the time T_d apart. To start the switching with both modules synchronously and to solve the here mentioned problems one module must be a master module and one module is the slave module. The operation of the master module is unchanged, except that its FPGA sends a high signal to the FPGA of the slave module. For the slave module some changes were done, firstly, the switch timings are always calculated and send to the FPGA of the slave module but the decision for activating the switches does not only depend on valid timings signals (a CRC check has to be passed and the timings must be greater than zero) from the slave microcontroller but additionally it only starts when the enable switching output from the master FPGA is high, see Fig. 4.27.

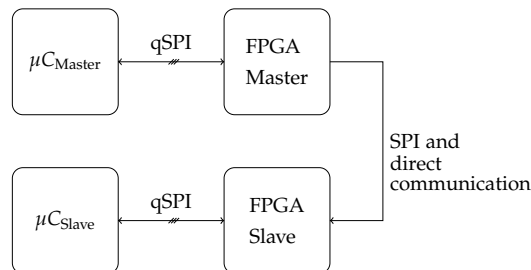


Figure 4.27: Required connection between the modules for synchronization of the PFC.

Additionally the phase shedding control is only active on the master module, since it must be guaranteed, that both modules always operate with the same amount of phases to draw equal power, only one control can be active and the output of the control is then shared. The slave must know already from the start of each half-wave how much phases should be active. For this the FPGA of the master communicates the amount of active phases to the FPGA of the slave module. Additionally a SPI communication between the two FPGAs is implemented for load sharing purpose, explained later.

4.2.3.5 Switch timing pre-calculation

With respect to the output values of the above mentioned control loops, the timings (T_{on} , T_{off} , and T_R , see Fig. 4.6) for each phase can be calculated, where T_{delay} is a constant time delay needed because of the Zero Current Detection (ZCD) which was experimentally found, L is the value of the boost inductors, u_{in} is the line voltage, u_{out} is the DC-link voltage, i_n is the negative current and i_{LP} is the peak inductor current.

$$\begin{aligned}
 T_{on} &= \frac{L \cdot (i_{LP} + i_n)}{u_{in}} \\
 T_{off} &= \frac{L \cdot i_{LP}}{u_{DC} - u_{in}} \cdot 1.2 \\
 T_R &= \frac{L \cdot i_n}{u_{DC} - u_{in}} - T_{delay}.
 \end{aligned} \tag{4.21}$$

T_{on} is the necessary time to reach the desired peak inductor current i_{LP} , but here including the time T_{Rv} , see Fig. 4.6. T_{off} is the time which is needed until the inductor current reaches zero again. This value is multiplied in eq. (4.21) with a safety factor of 1.2, which gives time to synchronize the statemachine running inside the FPGA with the zero current detections in reality to prevent a run-away of the inductor current. The statemachine enters the next state after detecting a zero current or after the calculated time T_{off} with the added safety margin was reached. The synchronization using the ZCD signals is here always during the off-phase (de-energizing of the boost inductor). This ensures switching even in case of no ZCD event. For safety reasons on top a fail counter is implemented inside the FPGA. If T_{off} has been consecutively reached for a definable amount of times without zero crossing detections in between, all switches are switched off and the state machine goes into an error state. T_R is the time required to reach the negative current i_n and is reduced with constant definable delay T_{delay} . This delay was evaluated on the prototype and consists of the propagation delays of the zero-current detection, the logic inside the FPGA and it also takes the non-linear output of the zero-current detection into account, which slightly changes over the line voltage under the assumption of a constant DC-link voltage, since with the line voltage the slope of the current through the saturable transformer is changed.

The peak inductor current i_{LP} is calculated from the required average current i_{avg} , derived from the individual controller outputs and the input voltage $u_{in}(t)$ which is used as a sinusoidal reference.

4.2.3.6 Switching state machine

The FPGA receives the three necessary timings for each phase (T_{ON} , T_{OFF} , T_R) from the microcontroller with the duty cycle for the PS-ZVS-bridge and transmits the period of the master phase as well the phaseshifts between the currents as count values back to the microcontroller during one communication cycle. Additionally CRC information from the microcontroller is send to the FPGA to ensure data integrity. In case of corrupt data the data is thrown away by the FPGA and the last received valid timings are used. The master phase period and the phaseshift between the phases are measured with the zero crossing information from the inductor currents. For each phase a individual state machine is running, see Fig. 4.28, which transitions from charging the coil to a resonant waiting state, to discharging the coil and waiting for the zero current crossing to synchronize again with reality, to the required negative current, then to the second resonant transition and then finally to charging again. The whole statemachine for one phase is presented in Fig. 4.28. Starting point is the state *standby* from where it enters state s_0 if all timings are valid. In s_0 the statemachine stays for T_{on} and then transitions into s_1 where it waits with both switches off for the time of the first resonant transition. After T_{res} the statemachine enters s_2 . Here it stays until either the time T_{off} has passed (which is calculated 20% higher than it should be in reality) or until the occurrence of a ZCD event. The 20% safety factor gives the state machine the possibility to synchronize to the ZCD events, in case the real current behaves differently than the model. After s_2 it transitions to s_3 either because of a zero current detection or because the time T_{off} has passed. There it waits for T_R until the desired negative current has been reached following with s_4 for the second resonant transition. After s_4 it transitions back into s_0 to charging the inductor again. For the reduction of input current spikes due to the addition of the current of multiple active phases at the beginning and the end of the input sine, the phases start already out of phase to each other with a pre-defined starting phaseshift.

4.2.3.7 Zero current detection

To measure the zero current crossing events of the boost inductors a solution with a saturable transformer core was chosen for demonstrator, [9, 52]. Another solution would be to measure the current with the voltage drop over a shunt-resistor, but with the inherit inductivity of the shunt either relatively large ohmic shunts are required (high loss) or special care must be taken for a low inductive shunt resistor design and the whole design

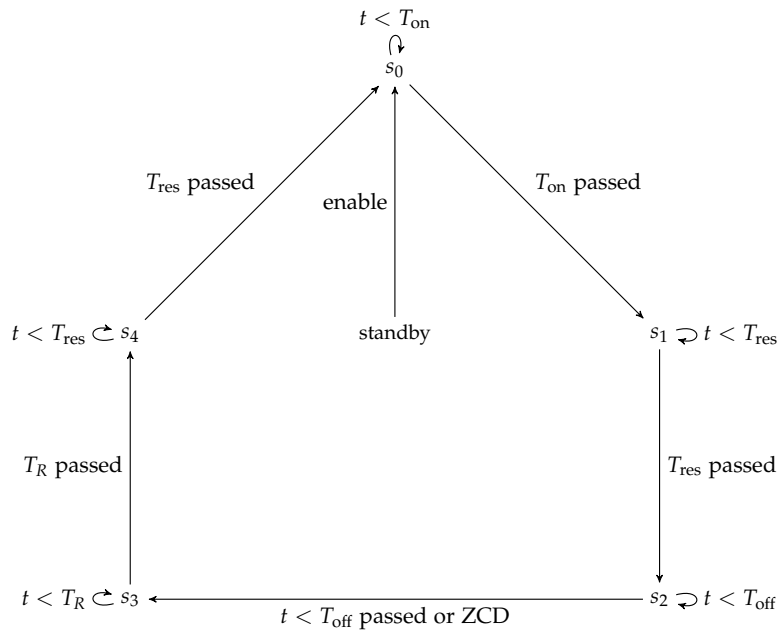


Figure 4.28: State machine for each phase inside the FPGA.

would then still require galvanic isolation. An example B-H loop for explaining the current detection with a saturable transformer core is shown in Fig. 4.29. The transformer consists of primary (N_p) and secondary (N_s) turns; the material is Vitroperm 500f, which has a relative high permeability and will therefore saturate already at low currents. As long as there is a change in the flux density caused by a changing primary current and therefore a changing magnetic field, a voltage is induced into the secondary winding (Faraday's law of induction). Since the effective area A_{Fe} is very small for the current during normal operation the saturation point where B_{max} is reached is already at a low current of a few mA. After the core is in saturation the relative permeability μ_r can be approximated with 1, therefore the flux density is no longer rising with a rising primary current and no voltage is induced anymore on the secondary side. If the primary current has a triangular shape it will start at zero current at the remanence flux point B_r and up to the point I_{sat} a voltage is induced on the secondary. After that the core is in saturation and the flux density no longer changes with the primary current and no voltage is anymore induced on the secondary side. This short voltage spike at the secondary side

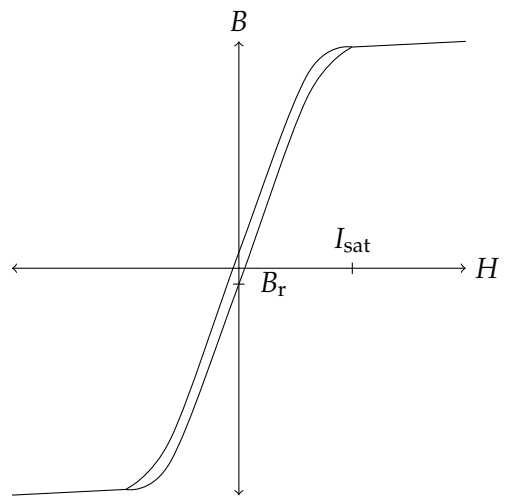


Figure 4.29: Typical BH curve.

can be used to detect the zero current events with a circuit like shown in Fig. 4.30.

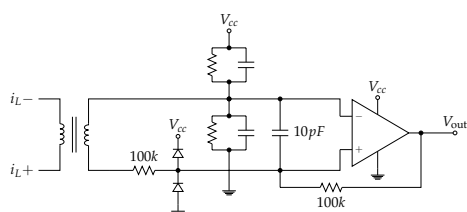


Figure 4.30: Inductor current zero crossing detection circuit with a saturable transformer and a fast comparator with positive feedback.

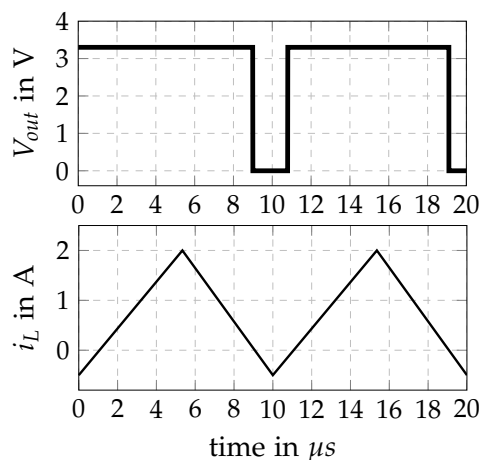


Figure 4.31: Simulated output signal of the ZCD circuit; (above) output voltage of the ZCD circuit; (below) current through the transformer primary.

The core will saturate already at a small current of a few mA so a voltage to the secondary side is induced, when the current approaches zero. The core material Vitroperm 500F from Vacuumschmelze saturates at around 1 T (100 °C) and with $B = \mu H$ and $H = \frac{NI}{l_e}$, where N_p is the number of primary turns, I_p is the current through the primary and l_e is the magnetic path length, it can be shown that by increasing the primary turns the core reaches saturation already at a smaller primary current. For the demonstrator four turns were used on the primary side and 13 turns were used on the secondary side. A higher amount of secondary turns increases the secondary voltage and with it the reaction speed of the comparator can be adjusted, since the small input capacitor has to be charged over a big resistor. The delay between the zero crossing of the boost inductor current and the comparator output is not constant, since the induced voltage depends on the slope of the flux density dB/dt which is proportional to the primary current slope, which is changing over the mains period, as mentioned already earlier. The amount of secondary turns was found by measurement, see Fig. 4.34. Since a voltage is already induced to the secondary side before the primary current actually reached zero, the output of the ZCD circuit delivers a ZCD event before the primary current actually reached zero. A higher amount of secondary turns actually makes the ZCD output signal more leading towards the real zero current event but also increases the induced voltage on the secondary

side, which must be handled by the parts as well. The two diodes after the 100 k resistor provide some protection for the input of the comparator against too high voltages.

To reduce the losses of the zero-current detection the original core from Vacuumschmelze was modified by reducing its volume which reduces the core loss linearly. The core losses are the main loss source of the zero-current detection. The smallest core offered from Vacuumschmelze with the material Vitroperm 500F has a thickness α of approximate 1.4 mm, see Fig. 4.33. This core was reduced by cutting the core down to a thickness α of 0.3 mm and thus reducing the losses by a factor greater than 4 compared to the unmodified core. The difference of the cores is shown in Fig. 4.32.

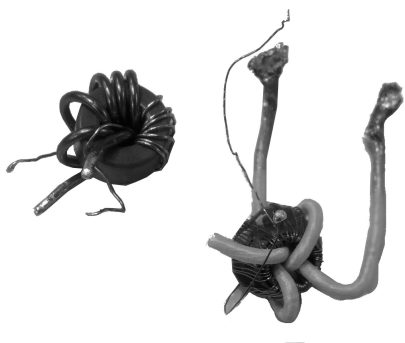


Figure 4.32: Zero crossing detection inductors; (left) with the unmodified core from Vacuumschmelze; (right) with the core thickness reduced to approximately 0.3 mm.

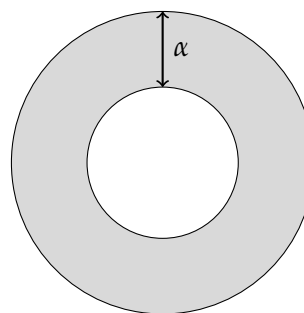


Figure 4.33: Cross-sectional drawing of the zero current detection core.

Fig. 4.34 shows the measured response of the ZCD circuit over a changing amount of secondary turns. It is shown, that the delay is actually negative, which means, that a ZCD impulse is received *before* the current is zero in reality. This is because the flux inside the core can change again once B is lower than B_{sat} , which induces a voltage in the secondary. This was measured for a DC-link voltage of 180 V and a DC input voltage of 30 V for a ZCD core with a thickness $\alpha = 0.5\text{mm}$ and with a constant of 4 primary turns. For the final core the thickness α had 0.3 mm, where the response time was measured with -80 ns. The response time is non-linear and depends on the slope of the current through the primary side, the higher current slope the smaller is the response time. The current slope through the primary and therefore through the boost inductor depends on the input voltage changing slightly over the mains period.

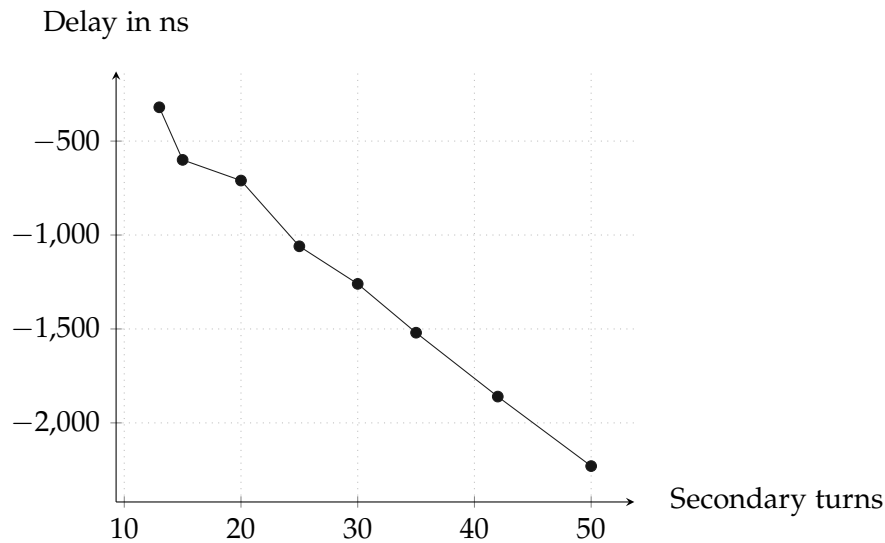


Figure 4.34: Measured ZCD response times over varying secondary turns.

4.2.4 Component selection

The components of the prototype for the PFC and the control are shown in Tab. 4.3. For the switches 250 V MOSFETs with an on-resistance F_{DSon} of 20 m Ω were utilized. To reduce the conduction loss and the overall losses the synchronous rectification switches, which only switch with the line frequency are each paralleled three times. The fast switching legs were realized with only one switch. For the boost cores MPP seemed a good choice for the core material and cores from magnetics-inc were chosen, for details see Tab. 4.3. All the measurements are obtained with galvanic isolation using either the error amplifier ADuM3190 or saturable transformer cores for the ZCD detection. For the DC-link capacitors a combination of cheap electrolytic capacitors and MLCC capacitors mounted on a ram-stick similar board were chosen.

4.2.5 Measurement and simulation results

The PFC was simulated with Gecko, a powerelectronics simulation software by ETH Zürich [54], and the additional losses (Gate driver, core loss, off switching loss, capacitor loss and the zero-current detection loss) were calculated afterwards with Matlab. Furthermore the simulated efficiency of the PFC was compared with measured results, as shown in Fig. 4.36. The measurements were executed with a Norma 5000 poweranalyzer. At low load the measured and simulated efficiency differ a bit but for the rest a good coincidence is shown. The efficiency drops at 40% and 70% load are caused by the fact that another phase was added, which results in additional losses. The peak efficiency was measured at full load with 99.07%. The loss breakdown of the PFC is shown in Fig. 4.37, which shows that

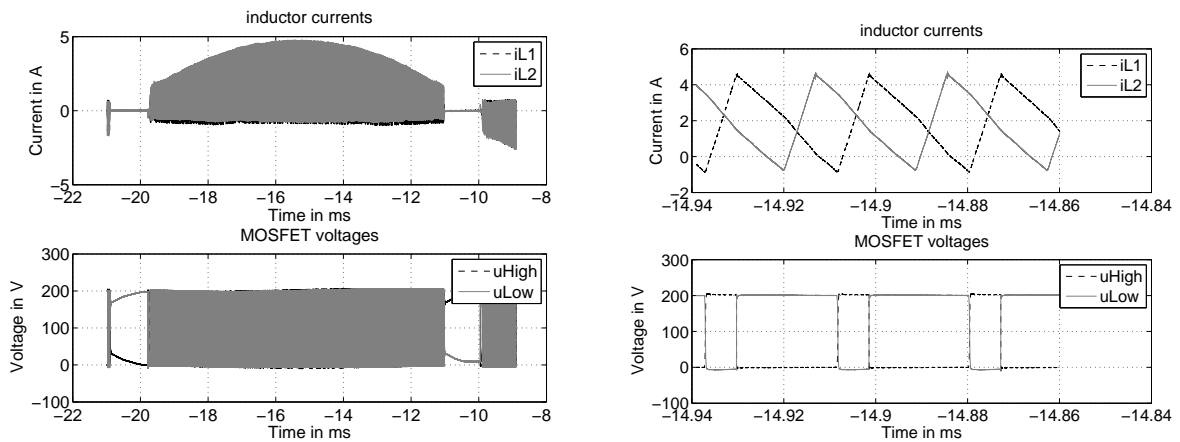
Table 4.3: Components for the PFC and the control.

PFC components	
primary switches	OptiMOS 3, 250 V, 20 mΩ
boost inductors	Magnetics 55550A2, 180 μH, 81 turns (litz wire)
ZCD saturation transformer	Vacuumschmelze T60006-L2009-W914, 4:13 turns ratio, thickness $\alpha = 0.3$ mm
DC link capacitors	MLCC 80x2.2 μF and aluminium electrolytic 7x120 μF
Control components	
Microcontroller	Infineon XMC4500-F144F1024 AC
FPGA	Lattice iCE40HX4k
isolated measurements	ADuM 3190
Gate driver	Si8238

the dominating losses come from the magnetics (boost inductor core loss and conduction), the MOSFET off-switching loss and the capacitor losses. Measured results showing the currents through the inductors and the voltages across the low and high side switches are presented in Fig. 4.35. The zoomed picture shows that the currents are out of phase of each other, due to the interleaving control.

4.2.5.1 Serialization of modules

For verification of the serialization concept and proof that the chosen control method works, two PFC's of the modules were tested at 20% of the rated load with one active phase for each module, see Fig. 4.38 for a comparison of the total input current and the input current through one of the boost inductors. It can be investigated that the input current has a more sinusoidal shape than the current through the boost inductor since the phaseshift between both of the boost currents varies randomly, which looks similar like running one module with two phases active and disabling the phaseshift control. To show the resonant switching behaviour the voltages across the lower boost switches are shown in Fig. 4.39, where no voltage overshoot exists. The small difference of the input voltages is due to the inaccurate measurement of the input voltages for each module and the slightly differing DC-link voltage is due to the imbalances in the modules, like input capacitor tolerances or the actual connected resistive loads. The PFC can either equalize the input voltage of the modules, where then the DC-link voltage can vary or it can equalize the DC-link voltage,



(a) Two phase interleaving (measured); (top) inductor currents i_{L1}, i_{L2} (bottom) MOSFET voltages u_{High}, u_{Low} .

(b) Two phase interleaving (measured, zoomed); (top) inductor currents i_{L1}, i_{L2} (bottom) MOSFET voltages u_{High}, u_{Low} .

Figure 4.35: Phase currents (top) and input current (below) for two phase interleaving.

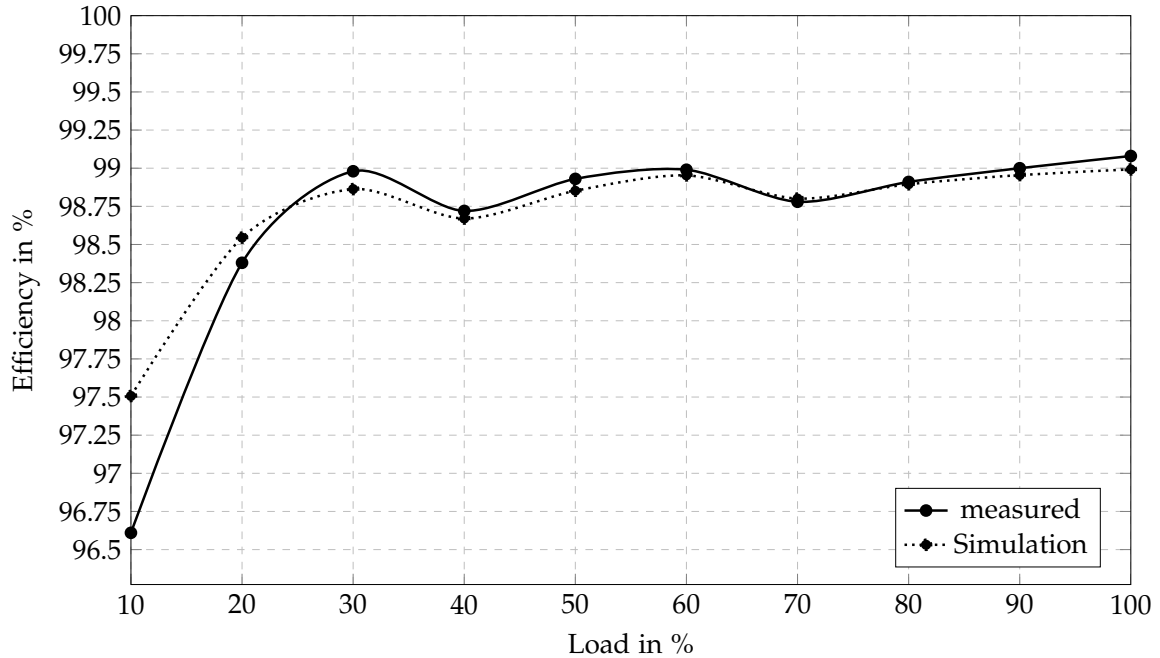


Figure 4.36: PFC efficiency over the load measured from 10% load up to 100% (500 W) compared with simulation, peaking at 99.07% at full load.

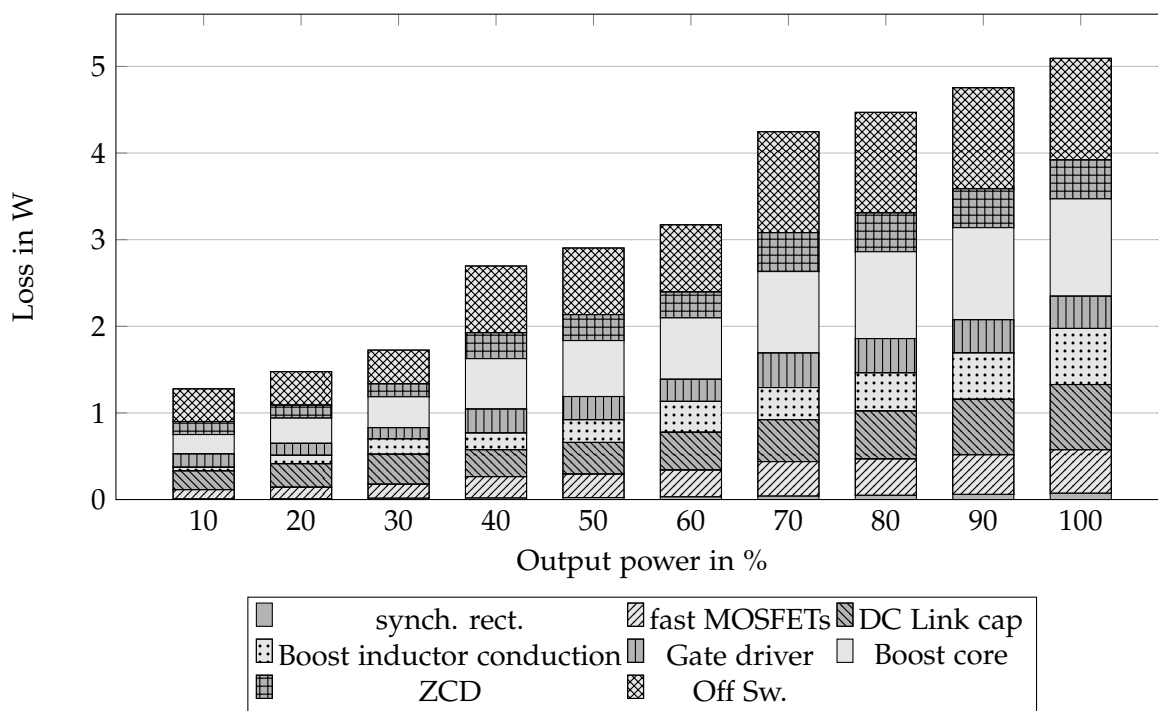
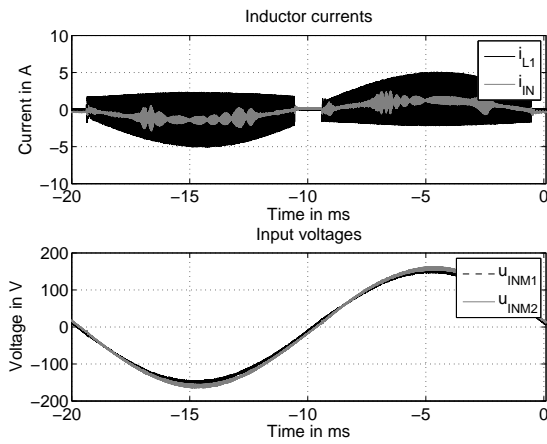


Figure 4.37: PFC loss breakdown for a single stage with phase shedding over different load points (100% load correspond to 500 W).

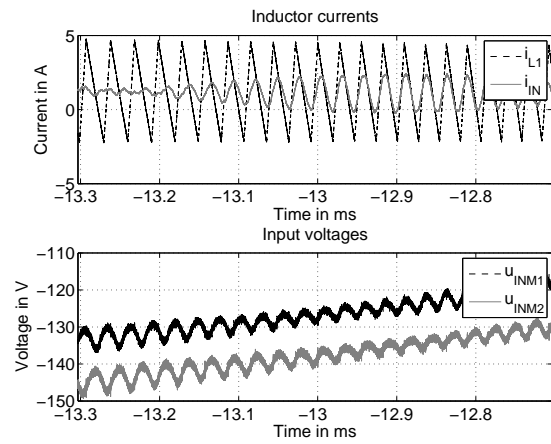
which leads to an unequal input voltage, both are not possible simultaneously, except both modules are completely identical.

4.3 Phase shifted zero voltage switched bridge

The PS-ZVS bridge is widely used in industry because of its soft switching capability, excellent efficiency for medium to high loads and the simple control, [55]. A lot of different integrated controllers are for this converter already available on the market, simplifying the control. Nevertheless for this thesis the control was implemented on a microcontroller and a FPGA since it was already used for controlling the PFC and this solution requires no additional hardware to control the PS-ZVS. The following section 4.3.1 will give a short introduction to the topology and explain why the center tap rectifier was chosen. In 4.3.2 the operation principle is explained. For further improvement in efficiency section 4.3.3 covers the topic of synchronous rectification and protection of the synchronous rectifier switches. To balance the flux in the transformer core section 4.3.5 shows various possibilities for that. In section 4.3.6 is explained how the required magnetic components for the PS-ZVS bridge were constructed. Finally, section 4.3.7 compares results obtained from simulation with the measured results.

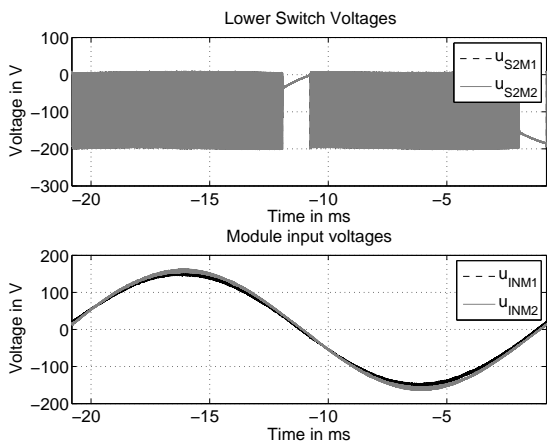


(a) Serial connection of two modules (measured); (top) inductor currents i_{L1}, i_{IN} (bottom) module input voltages u_{INM1}, u_{INM2} .

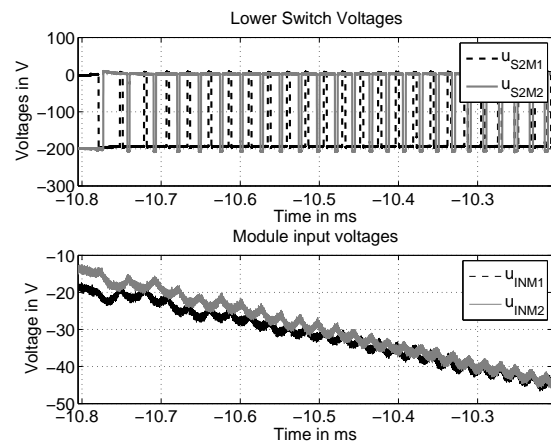


(b) Serial connection of two modules (measured, zoomed); (top) inductor currents i_{L1}, i_{IN} (bottom) module input voltages u_{INM1}, u_{INM2} .

Figure 4.38: Currents and voltages for the serial connection of the PFC.



(a) Serial connection of two modules (measured); (top) voltages across the lower MOSFETs u_{S2M1}, u_{S2M2} (bottom) module input voltages u_{INM1}, u_{INM2} .



(b) Serial connection of two modules (measured, zoomed); (top) voltages across the lower MOSFETs u_{S2M1}, u_{S2M2} (bottom) module input voltages u_{INM1}, u_{INM2} .

Figure 4.39: Voltages for the serial connection of the PFC.

4.3.1 Introduction

This section outlines shortly the operation principle of the PS-ZVS bridge. Since the maximum output current for each module is around 42 A, the center tapped configuration was chosen, see Fig. 4.40. The current doubler configuration would be better for output currents from 50 A to 100 A and onwards. Due to the higher semiconductor count and therefore higher losses a full bridge rectifier on the secondary is not a viable solution. Synchronous rectification in center tap configuration on the secondary side is mandatory for achieving high efficiency at higher loads, since schottky rectifier diodes always have a nearly constant forward voltage drop, causing huge conduction losses at higher currents, which reduces the efficiency especially for power supplies with a low voltage output. To protect the synchronous rectifiers from the off-switching overvoltage spike a RCD-snubber is added, which also makes it possible to recover some of the off-switching loss. For balancing the volt-seconds across the transformer a capacitor is added in series to the transformer.

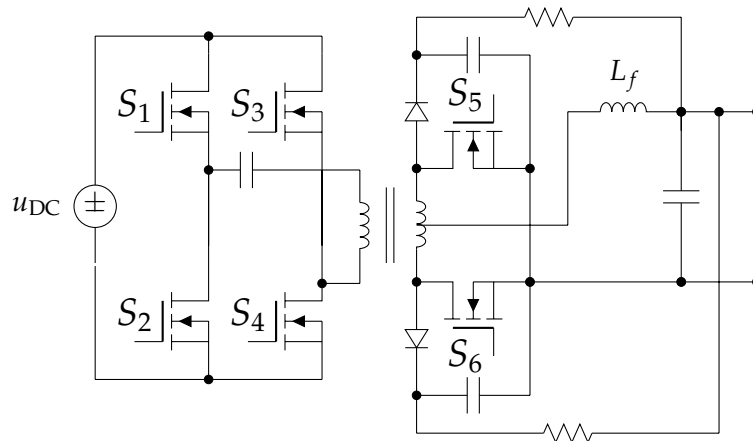


Figure 4.40: Detailed schematic for the PS-ZVS bridge with center tap configuration on the secondary side with RCD-snubber for the synchronous rectification switches.

4.3.2 Basic operation principle

The basic switching pattern is shown in Fig. 4.42. The operation of the PS-ZVS bridge can be divided into five phases. The duty cycle D defines the simultaneous on-time of the diagonal switches (S_1 and S_4 or S_2 and S_3) to deliver power to the secondary side, this phase is called the power delivering phase. Before power can be transferred to the secondary, the primary current through the transformer must be reversed and the time it takes until the current has changed polarity depends on the inductance in the primary path and the applied DC-link voltage to the primary. The power delivering phase is followed by a freewheeling phase, which is needed to control the output voltage for different loads.

Between the power delivering and the freewheeling phase is always a short resonant transition phase, in which the voltage across the next switch, which is supposed to turn on, resonates to zero.

Interval t_0 to t_1 : (see Fig. 4.41a) At the beginning of this phase switch S_3 is switched off. Between t_0 and t_1 the current in the leakage inductance of the transformer is discharging the output capacitor of switch S_4 and charging the output capacitor of S_3 . After the output capacitor of switch S_4 is discharged, switch S_4 is turned on under zero voltage, resulting in the two diagonal switches S_1 and S_4 being on. Since the current drops after the power transfer time due to conduction loss in the switches and the primary of the transformer, this zero voltage turn on is harder to achieve at lower loads.

Interval t_1 to t_2 : (see Fig. 4.41b) No power is transferred to the secondary yet. In this time the primary transformer current changes its polarity and the needed time depends mainly on the DC-link voltage which is applied to the transformer primary and the total inductance in the primary path (transformer leakage inductance). If there is an additional inductor in series with the primary of the transformer to ensure zero voltage turn-on towards lower loads, this time becomes longer and there is less time available for the actual power delivery, reducing the maximum transferable power at a specific DC-link voltage. After t_1 the slope of the current is lower and the next phase the power delivering phase begins at t_2 .

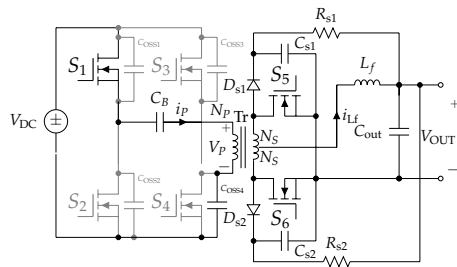
Interval t_2 to t_3 : (see Fig. 4.41b) In this time two of the primary diagonal switches are turned on for a time equivalent of the duty cycle D . During this power delivery phase the synchronous rectifier switch S_5 is turned off. If the other diagonal switches are on (switch S_2 and S_3) switch S_6 will be turned off. The secondary transformer voltage is equal to the input voltage times N_s/N_p and the primary current has a smaller slope compared to the slew phase due to the additional inductivity of the output filter L_f which is now added to the stray inductance L_{stray} thus limiting the current on the secondary side.

Interval t_3 to t_4 : (see Fig. 4.41c) At t_3 switch S_4 is turned off again to discharge the output capacitor of S_3 thus charging the output capacitor of S_4 . When the output capacitor of S_3 is discharged, it can be turned on under zero voltage again.

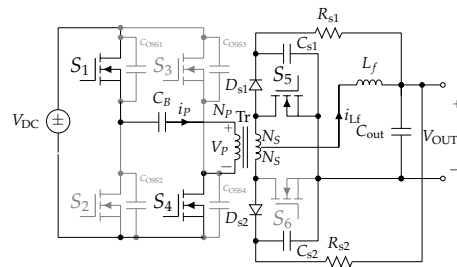
Interval t_4 to t_5 : (see Fig. 4.41d) At t_4 switch S_3 is turned on at zero voltage clamping the primary of the transformer to zero (either both upper or both lower switches are on) starting the freewheeling phase. With this state the output voltage of the DC/DC converter

can be regulated without changing the switching frequency. During this phase no power is transferred to the secondary side of the transformer.

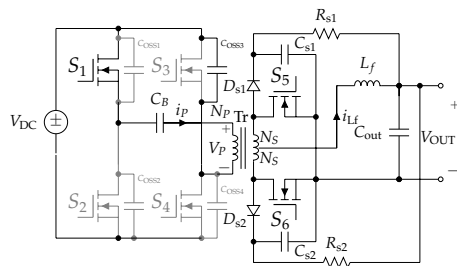
Interval t_5 to t_6 : At t_5 switch S_1 is turned off and charging it's output capacitor while discharging the output capacitor of switch S_2 . When the output capacitor of switch S_2 is discharged the switch can be turned on under zero voltage. This phase is identical to the phase from $t_0 \leq t \leq t_1$, just with a negative current. Here the same as above starts again, just that the current and voltages are negative.



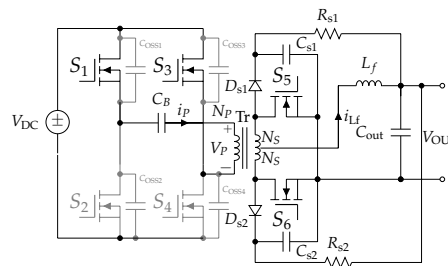
(a) Switching state for the left leg resonant transition between $t_0 \leq t \leq t_1$.



(b) Switching state for the slew and power delivery phase between $t_1 \leq t \leq t_3$.



(c) Switching state for the right leg resonant phase between $t_3 \leq t \leq t_4$.



(d) Switching state for the freewheel phase between $t_4 \leq t \leq t_5$.

Figure 4.41: Switching states for the PS-ZVS bridge; (black) currently used current paths; (gray) currently inactive current paths.

for the interval t_5 to t_6 and after the same switching pattern can be applied, in this case just the other two diagonal switches are switched on (S_2 and S_3) with the other synchronous rectifier switch being turned on during that time. [55–57]

4.3.3 Synchronous rectification

For high load currents synchronous rectification can dramatically boost the efficiency and it can be applied by replacing the schottky diodes with controlled switches, like in this case with MOSFETs. A big advantage of MOSFETs is that the forward voltage drop depends on the actual current through the device and the on-resistance R_{DSon} which is usually (see Fig. 4.43) lower then from a schottky diode. Also paralleling of more MOSFETs is easy be-

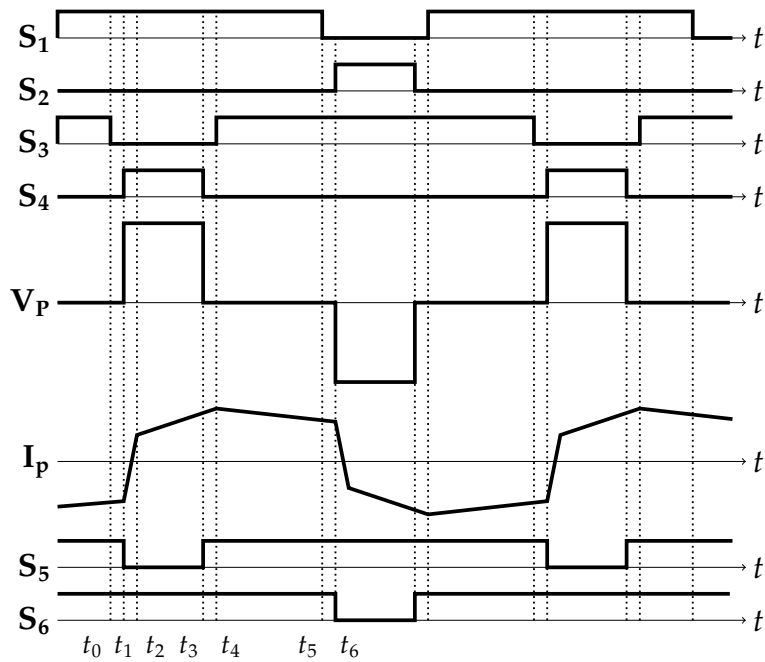


Figure 4.42: PS-ZVS bridge control signals and primary transformer voltage and current.

cause of their positive temperature coefficient and reduces further the voltage drop, which is not true for schottky diodes. Paralleling more diodes does not significantly decrease the forward voltage drop, it just increases the thermal rating. Fig. 4.42 shows the control signals for the synchronous rectification switches. The synchronous rectification switches are basically always on, except when two diagonal switches are turned-on simultaneously, which is outlined in Fig. 4.42 then only one synchronous rectification switch is turned-on at a time.

To reduce the over-voltage spikes at turn-off and prevent the MOSFETs from an avalanche breakdown due to the stored energy in the leakage inductance, a RCD-snubber is added. Fig. 4.47 shows the drain-source voltage across a synchronous rectifier switch and the snubber capacitor C_{snub} . For better understanding why there is an overvoltage spike at turn-off, the off-switching behaviour of the synchronous rectification will now be closer investigated. At the beginning the synchronous rectification switch is turned-on and the maximum gate-source voltage is applied. In this time the drain-source voltage u_{DS} is nearly zero and a current is flowing through the switch and the stray inductance L_{stray} . The stray inductance is the parasitic inductance from the transformer, the package inductance of the switch and the inductance of the PCB. At the time t_1 the gate is turned off closing the channel and the body diode starts to conduct at t_2 . At t_3 the current decreases and if the primary MOSFET switches fast, like in our case, the slope di/dt is constant and only limited by the loop stray inductance. Also there is a voltage drop across the stray inductance between t_3 and t_4 , which can be seen on the drain-source voltage u_{DS} . At t_4 the

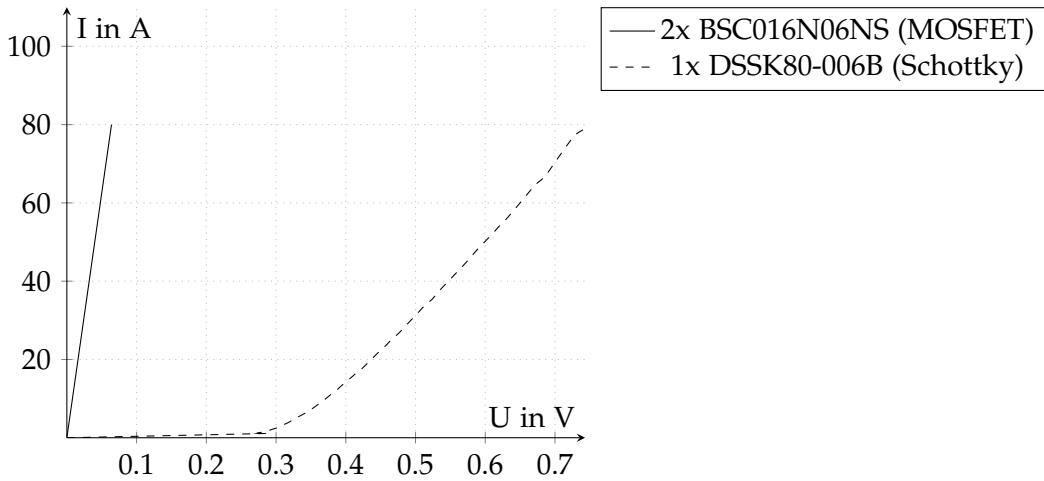


Figure 4.43: Diode forward voltage drop versus MOSFET; (MOSFET) 60 V, 1.6 mOhm, 2 parallel; (Schottky) 60 V, 40 A single.

current is zero and no current is flowing anymore through the body diode, therefore there is no forward voltage drop anymore, increasing u_{DS} . Because of the reverse recovery of the body diode the current keeps flowing with the same negative di/dt to remove the reverse recovery charge Q_{rr} and the parasitic output capacitance of the MOSFET C_{OSS} is charged to the transformer voltage u_T . At time t_5 the drain-source voltage u_{DS} is equal the transformer voltage and i_{DS} has reached its peak negative value. Ideally the drain-source voltage u_{DS} should stay at the transformer voltage u_T . [58]

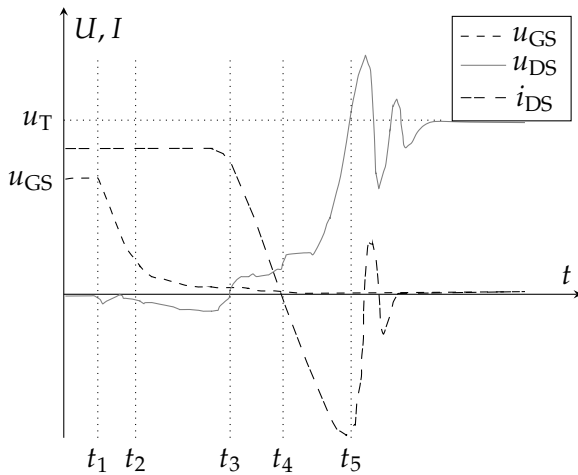


Figure 4.44: Turn-off waveforms for a synchronous rectifier switch, [58].

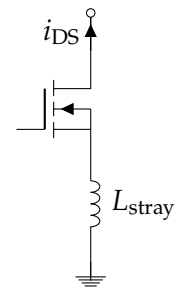


Figure 4.45: Equivalent circuit for the synchronous rectifier switch.

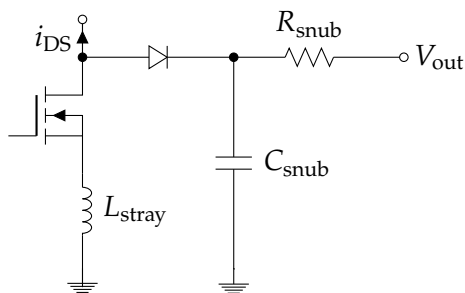


Figure 4.46: RCD snubber circuit to reduce the off-turning overshoot.

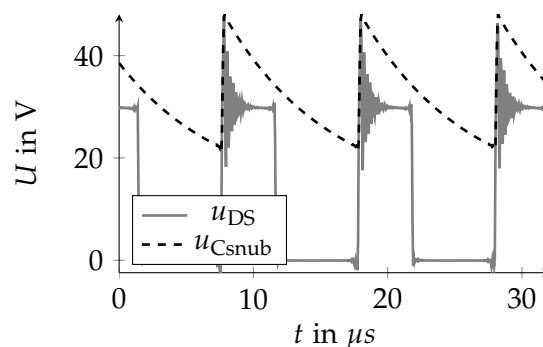


Figure 4.47: Voltage waveform across the snubber capacitor.

Due to the reverse recovery Q_{rr} from the body diode energy is stored in the stray inductance and an LC-resonant circuit together with the output capacity of the MOSFET is formed, de-energizing the stray inductance and charging the output capacitor of the MOSFET after t_5 over the transformer voltage u_T , which results in an overshoot accompanied with the oscillation. A part of the overshoot is transferred over the snubber diode into the snubber capacitor, see Fig. 4.46. The in the capacitor stored charge is partly recovered to the output of the converter over the snubber resistor. Ideally before the switch is switched off again, the capacitor voltage across C_{snub} is again close to the output voltage of the converter so at the next turn-off its again possible to store the energy of the off-switching voltage overshoot. The effectiveness of the snubber is limited by the loop inductance from the path of drain, diode and the snubber capacitor. Therefore it is recommended to place the capacitor and diode of the snubber close to the MOSFET and minimize the loop - MOSFET drain - snubber diode - snubber capacitor to ground to minimize the stray inductance. Further it is recommended that low inductive parts, like SMD parts, are used for the snubber. [58]

Overshoot reduction: To minimize the overshoots at turn-off it is possible to increase the on-time of the synchronous rectifier switches depending of the load to minimize the conduction time of the internal MOSFET body diode, which additionally reduces the reverse-recovery charge Q_{rr} and with that the stored energy in the stray inductance, see Fig. 4.48. The reverse-recovery charge is proportional to the expected voltage overshoot. The load dependent extended on-time could be implemented with a LUT, where the timings for an extended on-time of the synchronous rectifiers are stored dependent on the actual load. In this prototype this feature was not implemented, but due to the combination of a microcontroller and a FPGA it would be possible to do that increasing the efficiency towards higher

loads. For an accurate estimation of the load and to an optimization of the synchronous rectifier timings an output current measurement is required.

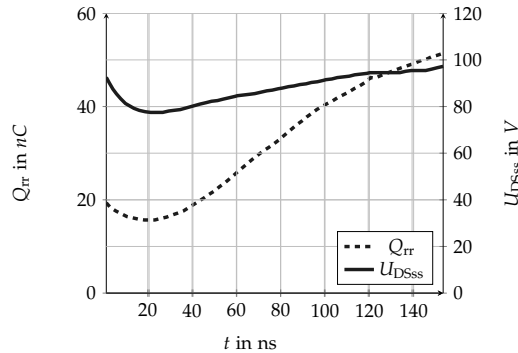


Figure 4.48: Reverse recovery charge Q_{rr} and voltage overshoot over the conduction time of the internal body diode, [59].

Another method for reducing the stored energy in the stray inductance is reducing the stray inductance itself. First, this should be done already in the layout, by carefully minimizing the stray inductance loop, see Fig. 4.49, and in the design by choosing devices with a low stray inductance due to the legs by reducing the package size, see Fig. 4.50. A reduction in the stray inductance results linearly in less stored energy in the stray inductance, less switch-off losses, reduced snubber requirements and maybe even MOSFETs with a lower rated breakdown voltage on the secondary side can be utilized.

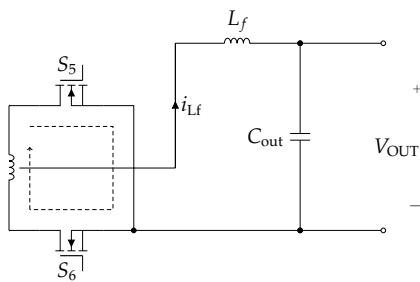


Figure 4.49: Secondary side of the ZVS bridge with the stray inductance loop (dashed).

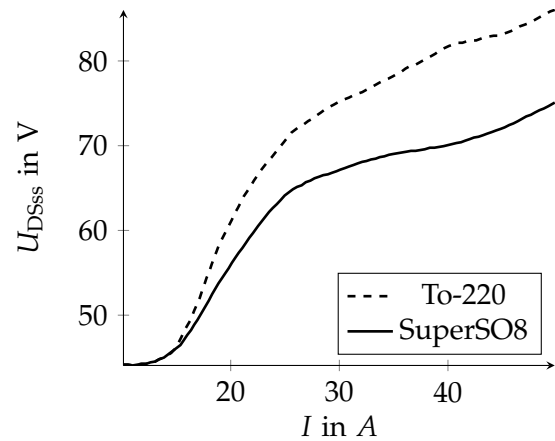


Figure 4.50: Synchronous rectifiers overshoot comparison between the traditional TO-220 package and SuperSO8, [59].

4.3.4 PSZVS component selection

The important components for the PS-ZVS bridge are the transformer, the primary and secondary MOSFETs and the output filter. For the transformer it is important to know the operating frequency, the maximum power to transfer at the minimum allowed DC-link voltage and the expected temperature range to choose a fitting core material and an appropriate core size and shape. With the chosen material certain parameters like the peak flux density are known and together with the required core size and the allowed peak flux density, which is usually loss limited, the minimum amount of primary turns can be calculated. Due to the low output voltage there is usually not much freedom in selecting the amount of required secondary turns, but fine adjustments in order to keep up with the hold-up time requirement to the amount of primary turns might be necessary.

4.3.4.1 Transformer

For selecting the transformer things like the core shape, the core material, the maximum transferable power, core loss and copper losses have to be considered. Today several suitable ferrite materials for high frequency transformers exist on the market. Higher frequency materials have a higher resistivity to minimize the eddy currents losses, but they have the disadvantage of lower permeability thus increasing the magnetizing current which increases the copper losses. For the core shape the PQ shape was chosen, which is specifically designed for switch mode power supplies, where the geometry provides an optimum ratio of volume to winding area and radiating surface minimizing the rise of temperature during operation. The different commercially available core materials are designed to provide their minimum core loss either at a specific switching frequency, a specific temperature or a combination of frequency and peak flux density. [60]

Fig. 4.51 shows the core loss for different core materials over a typical temperature range used for transformers in switch-mode power supplies for an operating frequency of 100 kHz and $\hat{B} = 100$ mT. There exist some temperate flat core materials like N95, N96 or 3C95 which have lower core losses already at low temperatures and materials which have their point of lowest core loss at the 100 °C region. Since the power supply must achieve high efficiency from low loads and onwards, a core material with a flat core loss over the temperature is preferred. For selecting the core size the area product $A_p [cm^4]$ can be considered for a rough estimation, which is the product of the window area W_a and the core cross section area A_c . Several approaches exist in literature for calculating the area product A_p , see eq. (4.22)

$$A_p = W_a \cdot A_c = \frac{P_{total} \cdot 10^4}{K_u K_f B_m f \cdot J'} \quad (4.22)$$

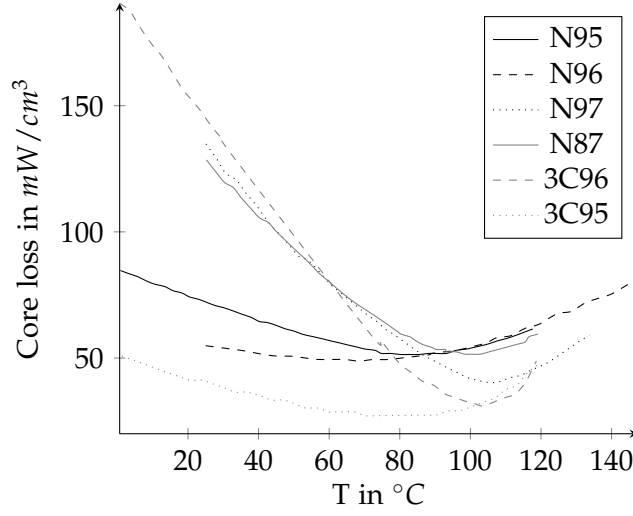


Figure 4.51: Comparing the core loss of different core materials with data from the datasheet over the temperature for $f=100$ kHz and $\hat{B}=100$ mT.

where W_a is the winding area in cm^2 , A_c is the core area in cm^2 , P_{total} is the sum of input and output power in W, K_u is the window utilization factor (chosen with 0.4), K_f the waveform coefficient, which is 4 for a square and 4.44 for a sinusoidal waveform, B_m the peak flux density in T, f the operation frequency in Hz and J the chosen current density in A/cm^2 . [61]

A transformer has two loss sources, the core loss and the copper loss, see eq. (4.23).

$$P_{\text{tr}} = P_{\text{Cu}} + P_{\text{Core}}. \quad (4.23)$$

The required number of turns for the primary side can be derived from Faraday's law of induction with eq. (4.24), which leads to eq. (4.25),

$$U_p = N_p \frac{d\phi}{dt} \quad \phi = \int_A \vec{B} d\vec{A}, \quad (4.24)$$

$$N_p = \frac{d_m \cdot U_p}{2 \cdot \Delta B_m \cdot A_c \cdot f'} \quad (4.25)$$

where d is the maximum duty cycle, where voltage to the primary is applied, U_p is the voltage on the primary side, which is the DC-link voltage and ΔB_m is the peak flux density, see also Fig. 4.52.

From eq. (4.25) can be concluded, that an increase of ΔB_m leads to higher core losses P_{Core} and lower copper losses and vice versa, where ΔB_m is usually limited by the core loss

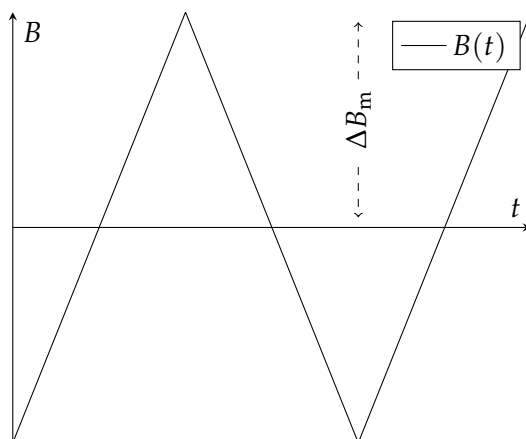


Figure 4.52: Definition of the peak flux density ΔB_m for eq. (4.25).

and not by the saturation limit of the material. With the primary and the secondary voltage a turns ratio, see eq. (4.26), can be calculated,

$$\frac{U_p}{U_s} = \frac{N_p}{N_s}, \quad (4.26)$$

where U_p and U_s are the primary and secondary voltages and N_p and N_s are the primary and secondary turns. This equation already limits the choice of the secondary turns, stating that for an output voltage of 12 V at least two secondary turns are necessary. By choosing the minimum required amount for the secondary turns, the copper losses are minimized and with eq. (4.25) the primary turns can be adjusted. Another subject is the hold-up time requirement which defines the minimum primary voltage or here the DC-link voltage, where operation an full load of the PS-ZVS is still possible. For fulfilling the hold-up time requirement the primary to secondary turns ratio has to be reduced, which increases the secondary voltage at the disadvantage of increasing the transformer core loss and the magnetizing current, which mainly lowers low load efficiency. With the equations above and some simulations, to respect the voltage drop from the output filter inductor, a primary turns ratio can be found and an approximation of the magnetic flux density in the transformer can be calculated as well. The duty cycle for the PS-ZVS bridge changes only slightly with the load, the by far bigger impact has the DC-link voltage. Since simulation data was available the copper and core losses for different transformer cores and constructions could be calculated and compared, see chapter A.

4.3.4.2 Output filter

For this topology the output filter is required to lower the output voltage and current ripple, where second is also important for the output capacitors, since the current ripple that electrolytic capacitors can withstand is limited.

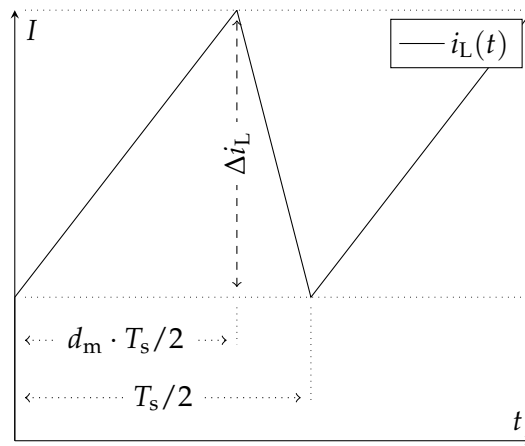


Figure 4.53: Waveform of the current through the output filter.

By defining a maximum allowed ripple current Δi_L and the known transformer ratio, the minimum required output inductance for full load can be calculated with eq. (4.27),

$$L_f \geq \frac{U_{DC} \cdot \frac{N_s}{N_p} \cdot d_m \cdot \frac{T_s}{2}}{\Delta i_L}, \quad (4.27)$$

where d_m is the maximum duty cycle at full load and $T_s/2$ is half the switching period. With this calculated inductor value a selection of MPP cores, which can handle the ampere-turns were selected, then for each the amount of necessary turns was calculated and then again for each load the total losses, consisting of copper and core losses, were calculated and compared.

Fig. 4.54 shows the calculation results for different MPP cores with different permeabilities and sizes shown with the outer diameter. It is shown that the losses of the cores are approximately equal at around 20% load, but there is only one combination which performs good at low and at high load at the same time, with the drawback that it also has the biggest outer diameter, so a compromise has to be found.

4.3.4.3 Primary and secondary MOSFETs

For the primary switches of the PS-ZVS bridge the same limited choices as already presented for the PFC are available. As shown later for achieving resonant switching down to very low loads, the output capacitance must be kept small, which increases in case of the same voltage class, the on-resistance and with that the conduction losses. Therefore the 60 mΩ devices were here chosen for the primary switches, which also helps at low load conditions due to the reduced gate losses compared with the 20 mΩ switches. For the synchronous rectifier switches on the secondary side the new OptiMOS 5 and a 60 V voltage

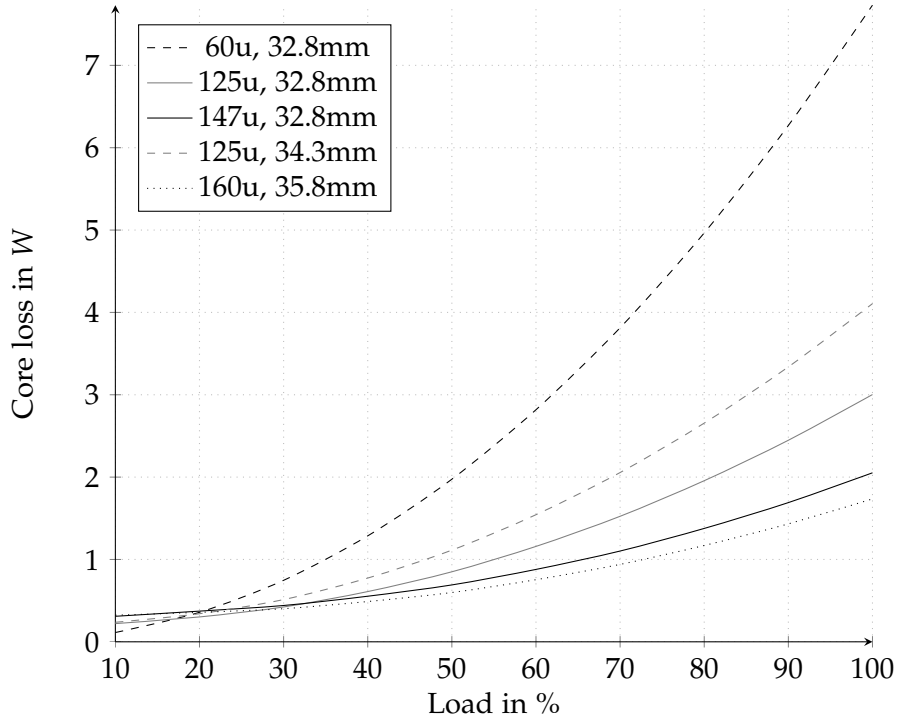


Figure 4.54: Total losses of some selected MPP cores over the load.

class were chosen since the required blocking voltage at nominal DC-link voltage is by calculation already at 32 V and due to the varying DC-link voltage with the mains and to have a higher margin the 40 V technology would be nice to use due to the even better FOM, but the safety margin of less than 8 V is too low. To minimize the loop inductance and therefore minimize the off-switching overshoot the decision for the package fell to Super-SO8, since the earlier available and better suited CANPAK for OptiMOS 3 was no longer available for OptiMOS 5. For the synchronous rectifier switches the losses consist of loss due to the output capacity, conduction loss, gate loss and reverse recovery loss. For an overall optimized efficiency choosing a device for the synchronous rectifier switches with a too low R_{DSon} would result in great performance for the DC/DC stage at high load conditions but it would perform poor at low load conditions and vice versa, requiring a balanced choice. By defining a voltage and technology class, the FOM parameters are constant within that class and the three above mentioned losses can be calculated, see eq. (4.28),

$$\begin{aligned}
 P_{\text{Cond}} &= R_{\text{DSon}} \cdot I_{\text{rms}}^2 \\
 P_{\text{Gate}} &= Q_G \cdot U_G \cdot f_{\text{sw}} \\
 P_{\text{Oss}} &= \frac{U_T \cdot f_{\text{sw}} \cdot Q_{\text{OSS}}(U_T)}{2},
 \end{aligned} \tag{4.28}$$

where I_{rms} is the effective output current on the secondary side, Q_G is the gate charge, U_G is the gate voltage, f_{sw} is the constant switching frequency, U_T is the secondary transformer voltage and $Q_{\text{OSS}}(U_T)$ is the charge stored in the output capacitance at the secondary transformer voltage U_T . The total loss P_{Vtotal} is therefore the sum of the three above described losses, but the two variables, respectively the gate charge Q_G and the charge in the output capacitance $Q_{\text{OSS}}(U_T)$ are inversely proportional to R_{DSon} , which allows to rewrite the equation for the total losses, see eq. (4.29) and searching for an extrema by derivation and setting to zero leads to eq. (4.30).

$$P_{\text{Vtotal}} = I_{\text{rms}}^2 \cdot R_{\text{DSon}} + \frac{Q_G \cdot U_G \cdot f_{\text{sw}}}{R_{\text{DSon}}} + \frac{U_T \cdot f_{\text{sw}} \cdot Q_{\text{OSS}}(U_T)}{2 \cdot R_{\text{DSon}}}. \quad (4.29)$$

$$\frac{dP_{\text{Vtotal}}}{dR_{\text{DSon}}} = I_{\text{rms}}^2 - \frac{Q_G \cdot U_G \cdot f_{\text{sw}}}{R_{\text{DSon}}^2} - \frac{U_T \cdot f_{\text{sw}} \cdot Q_{\text{OSS}}(U_T)}{2 \cdot R_{\text{DSon}}^2} \stackrel{!}{=} 0. \quad (4.30)$$

Solving eq. (4.30) to find a R_{DSon} which is an extrema leads to eq. (4.31).

$$R_{\text{DSonOPT}} = \frac{\sqrt{Q_G \cdot U_G \cdot f_{\text{sw}} + 0.5 \cdot U_T \cdot f_{\text{sw}} \cdot Q_{\text{OSS}}(U_T)}}{I_{\text{rms}}}. \quad (4.31)$$

To verify that the R_{DSonOPT} is a minimum and not a maximum, eq. (4.30) can be derived once more by R_{DSon} and evaluated at R_{DSonOPT} which leads to eq. (4.32), proving that it is a minimum. [59]

$$Q_G \cdot U_G \cdot f_{\text{sw}} + \frac{U_T \cdot f_{\text{sw}} \cdot Q_{\text{OSS}}(U_T)}{2} > 0. \quad (4.32)$$

To balance the efficiency over the full load range an effective current, for which the synchronous rectifier achieve minimum loss has to be chosen. For the prototype this current was chosen for the condition of 50% load with respect that at 50% load the highest overall efficiency is required. The synchronous rectifier switches will have their highest loss at full load and for this case with the known R_{DSonOPT} the number of required paralleled switches to limit the temperature per device, can be found, see eq. (4.33),

$$P_{\text{SO8max}} < \frac{P_{\text{Vtotal}}}{n}, \quad (4.33)$$

where P_{SO8max} is the maximum allowed loss for the Super-SO8 package, and n is the amount of parallel switches. The maximum allowed power dissipation of the Super-SO8 package can be calculated with the maximum for the design allowed temperature for the package $T_{\text{DesignMAX}}$ and the thermal resistance R_{thJA} , which defines the thermal junction to ambient resistance, see eq. (4.34).

$$\frac{P_{\text{Vtotal}}}{n} \cdot R_{\text{thJA}} \leq T_{\text{DesignMAX}}. \quad (4.34)$$

4.3.5 Transformer flux balancing

Since the DC-link voltage is slowly varying with the mains, slightly miss-timed switching signals and differences of the semiconductors, a DC component might be applied to the transformer causing a DC magnetic flux in the transformer, which increases the core loss and which even might drive the core into saturation due to Faraday's law of induction, which states that the flux is equal to the integral of volt-seconds applied to the transformer. The solution is that to prevent the flux from *walking* in saturation, the applied volt-seconds on average must be zero. Several methods for balancing the flux are already known to prevent this. The methods can be divided into passive and active methods. The simplest passive method is to insert a capacitor in series to the transformer to block any DC or to introduce an airgap requiring higher magnetic field strengths to reach saturation. Also switching under zero voltage helps in reducing the volt-second imbalance and to compensate for the device differences, as long as the the circuit timing mismatches are a fraction of the resonant transition timings, as shown in [62]. Active flux balancing requires some kind of flux measurement, like for instance measuring the magnetization current with an additional small transformer [63] or direct measurement of the flux with hall sensors [64], which requires an airgap in the transformer and therefore increases the magnetizing current. Also a new interesting solution was investigated, called the magnetic ear [65] which measures the flux indirectly over the inductivity of a small auxiliary transformer which is mounted on the main transformer and uses the information for feedback control. Since the primary switches of the PS-ZVS bridge turn on under zero volt conditions and the DC/DC converter is supposed to be simple the solution with a series capacitor in series to the transformer primary, as shown in Fig. 4.40 was chosen.

4.3.6 Transformer and output filter construction

The main goal was a transformer with low losses where the resonant inductance is already integrated to save space and cost. The loss sources of a transformer can be separated into copper loss, eddy current loss and core loss. The copper loss can again be separated in a pure DC-resistance loss and an additional skin-effect and proximity-effect loss, which depends mainly on the geometry of the conductor, the current and the frequency. The core loss combined with the eddy current loss are dependent on the material of the transformer, the geometry, the frequency and the magnetic flux density. To minimize the copper losses the primary turns were built with litz-wire and the secondary with thin copper foil. The detailed loss calculation for the transformer is shown in section A. To minimize the core losses, especially at the part load point of 50%, since at this point the highest efficiency is required, a ferrite material with low core losses at a relative low temperature (60°C) was chosen. For the output filter a low loss core material like MPP was chosen. A fourier

analysis of the current through the output filter showed that it is mostly DC-current with only a small AC ripple (see Fig. 4.55), therefore the skin-effect and the proximity effect are only small loss sources making the use of full copper wire attractive.

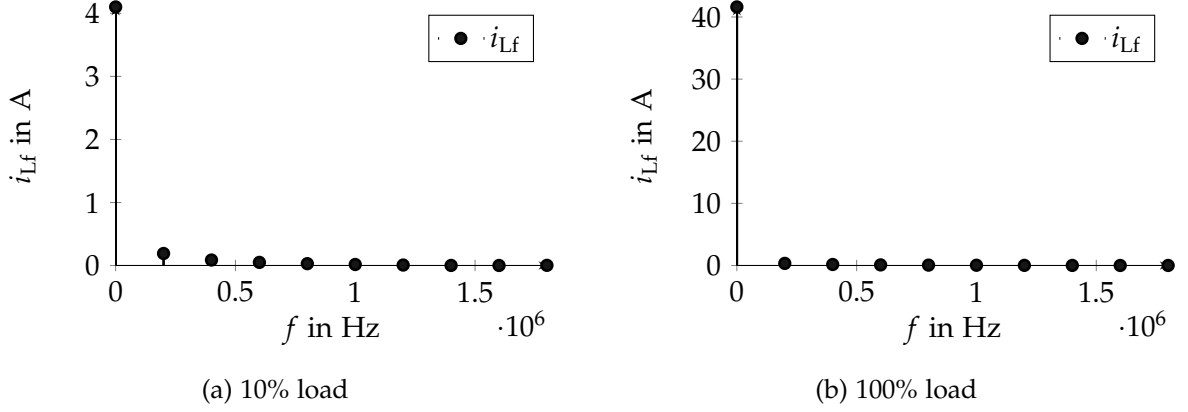


Figure 4.55: FFT Analysis for the current i_{Lf} through the output filter for a) 10% load and b) for 100% load (first 10 harmonics).

The details for the transformer and the output filter are shown in Tab. 4.4. The construction of the transformer with the arrangement of the windings is shown in Fig. 4.56, as well details of the used MOSFETs and the output filter and capacitors.

4.3.6.1 Integrated resonance inductance

Since it is necessary to achieve zero-voltage turn-ons down to 10% of the load, an additional inductor for storing the required energy for discharging the output capacitors of the MOSFETs is needed. This inductor can be the stray inductance of the transformer, but usually the stray inductance is not big enough to provide sufficient energy down to very low load conditions, where the required energy can be approximated with eq. (4.35), [56]

$$E = \frac{1}{2}L_{\sigma}I_p^2 > \frac{4}{3}C_{\text{MOS}}V_{\text{DC}}^2 + \frac{1}{2}C_{\text{Tr}}V_{\text{DC}}^2, \quad (4.35)$$

where I_p is the primary current before the resonant transition, L_{σ} is the transformer stray inductance, C_{MOS} is the output capacitance of the MOSFET, V_{DC} is the DC-link voltage and C_{Tr} is the transformer capacitance due to the windings. The primary current depends mainly on the load current and cannot be changed. By increasing the stray inductance of the transformer L_{σ} the stored energy in the series resonant circuit can be increased, enabling zero voltage turn on at lower load conditions. Increasing L_{σ} increases also the duty cycle loss, which limits the maximum transferable power, so the value cannot be made too large. By lowering the magnetic resistance between the primary and the secondary winding a

Transformer	
primary winding	25 turns, 120x0.1mm litz wire
secondary winding	2:2 turns, 2x200 μm thick copper foil, kapton tape for isolation
Core shape	PQ 35/35
Core material	Ferrite Epcos TDK PC95
primary leakage inductance	adjusted to 10 μH
Output filter	
core type	Magnetics 55547A2
outer core diameter	32.80 mm
core material	MPP
winding	7 turns, 1.2mm copper wire, 6 strands in parallel
Other	
primary MOSFETs	IPB600N25N3 G , 250 V, 60 $m\Omega$
secondary MOSFETs	BSC016N06NS, 60 V, 1.6 $m\Omega$, 2 parallel
output MLCC 12 V	AVX X7R 21x10 μF parallel
output electrolytic 12 V	Nippon Chemicon LXV series 3x330 μF

Table 4.4: Construction details of the PSZVS-bridge.

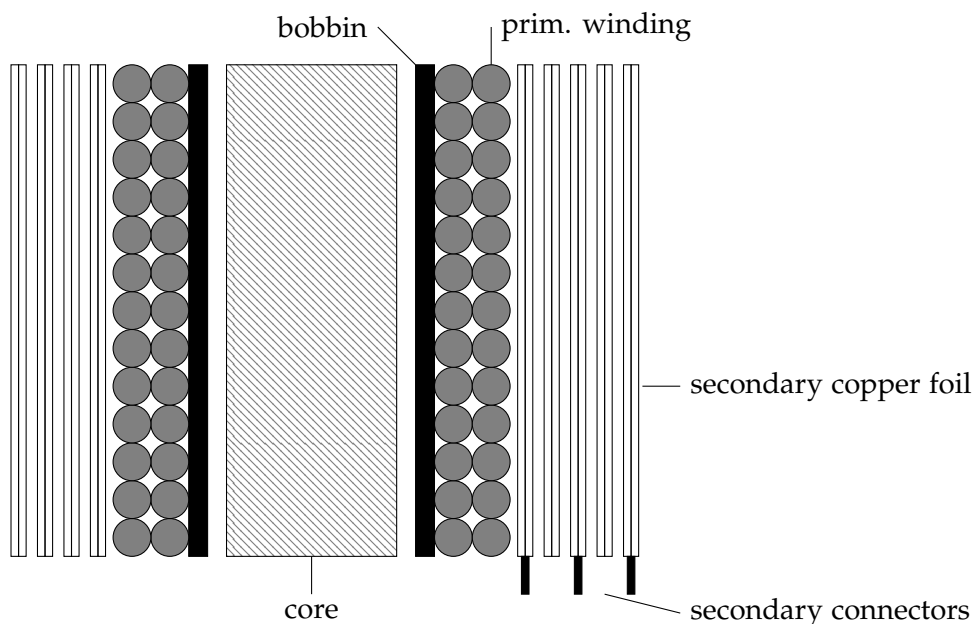


Figure 4.56: Cross-sectional drawing of the transformer; inner layers are the primary windings (litz) and the outer rectangle layers are the secondary windings ($2 \times 200 \mu m$ parallel) copper foil, isolated with kapton tape; on the inside is the core material surrounded by the bobbin (black).

flux will flow, which also increases the stray inductance. The magnetic resistance between the primary and secondary was lowered by putting a material with a high permeability in between the primary and secondary winding, as shown in Fig. 4.57. The measured stray inductivity of the transformer without modification was at around $6 \mu H$. To lower the overvoltage spikes of the primary MOSFETs at 10% load, a higher stray inductance was needed.

After the modification with Vitroperm 500f with a width of approximately 1 cm and a thickness of $100 \mu m$ around the whole bobbin, the leakage inductance was at $10 \mu H$ for up to 2 A of current. The saturation effect of the stray inductance is an additional nice feature since at higher loads where enough energy is stored in the stray inductance alone this additional inductance saturates and does not increase the duty cycle loss so much, which helps in achieving the hold-up criteria.

4.3.6.2 Extending the zero voltage switching range

At low load conditions even the increased leakage inductance is not enough for achieving zero voltage turn-on conditions on the primary side. The fact that the normal DC-link voltage is at 200 V and that the breakdown voltage of the primary MOSFETs is rated with 250 V leaves a room of only 50 V until the breakdown voltage of the MOSFETs is reached,

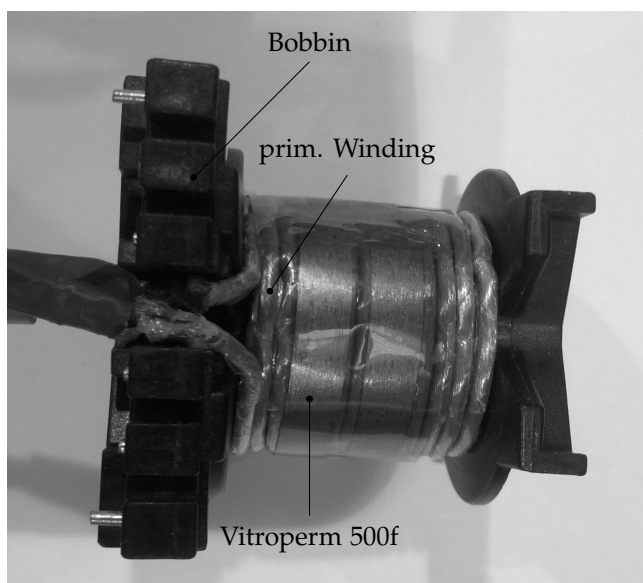


Figure 4.57: Increasing the leakage inductance by reducing the magnetic resistance between the primary and the secondary with Vitroperm 500f.

which is the case if the MOSFETs are not turned-on at zero voltage (valley switching or hard switching). At low load range (up to 30%), which can be roughly determined with the active phases of the PFC, the switching pattern of the synchronous rectifier switches is slightly changed, to further increase the stored energy in the leakage inductance. The current in the primary (and as well as in the secondary) is increased by turning one of the synchronous rectifier switches on a bit too early. This change in the switching pattern occurs during the power delivery phase, when two diagonal switches are turned on (either S_1 and S_4 or S_2 and S_3). During the power delivery phase normally only one synchronous rectification switch is turned on. In this presented modified switching pattern the second synchronous rectification switch is turned on as well, shortly before the power delivery phase ends, shortening the secondary of the transformer leading to a rapid increase of current in the transformer, as shown in Fig. 4.58, where the primary current I_p , which is shown as black solid for the current in normal operation and as a dashed line for this modified operation is compared. This short circuit happens only for a very short time and was for the presented prototype chosen with 20 ns, which is also the clock period for the FPGA. Finer adjustments are possible by adapting the relationship of the primary and synchronous rectifier gate resistors. During this short, the current in the primary and secondary of the transformer increases very fast resulting in a higher current after the freewheeling phase compared to how it would be in normal operation mode. The stored energy increases quadratic with the current and with this slightly different switching pattern it is possible

to achieve zero voltage turn-ons down to extremely low loads, minimizing the overvoltage spikes due to always achieving resonance and boosting efficiency.

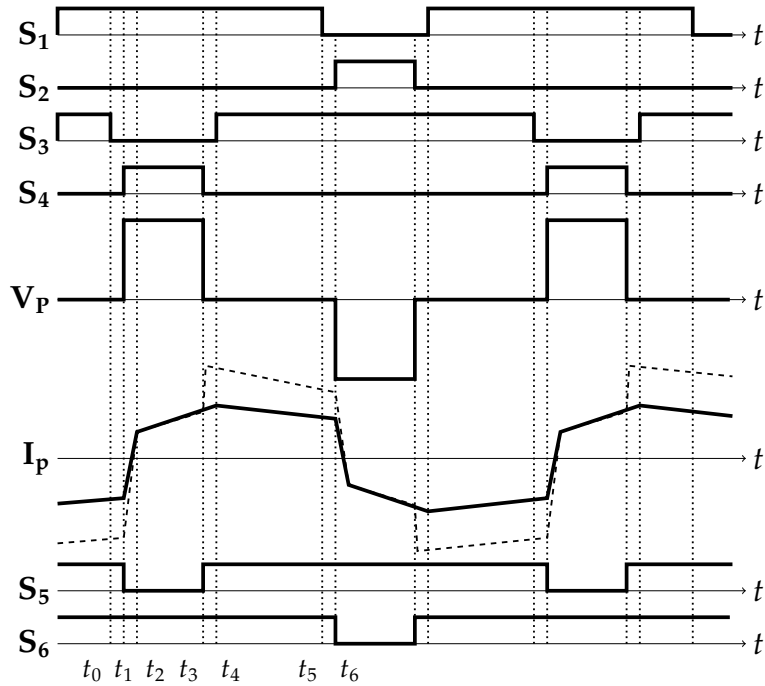


Figure 4.58: Extending the zero-voltage turn-on range by slightly changing the synchronous rectifier switching pattern to increase the current in the leakage inductance (dashed gray line for the primary current); (top) primary transformer current; (middle) voltages across S_1 and S_2 ; (bottom) digital signals for the switches from S_1 (top most) to S_6 (lowest).

To verify this non-standard operation mode it was tested on the prototype and the measured waveforms are shown in Fig. 4.59. The measurement was taken at 10% load and is very similar to Fig. 4.58. Further it is shown that across the switches S_1 and S_2 nearly no voltage overshoot exists, which indicates that the switching pattern for extending the zero voltage operation range is working.

4.3.6.3 Burst mode operation

Although its possible to operate the prototype with zero voltage turn-on's at very low loads, at 10% load an alternative operation mode was implemented to further boost the efficiency and to meet the titanium requirements by the 80plus organisation. In burst mode the primary switches are switched consecutively a few times with the standard switching pattern at maximum duty cycle and then there is a pause where all switching operation stops. This mode decreases the switching and the transformer core loss, enabling higher efficiencies at low loads at the cost of a higher output voltage ripple and some noise. If the

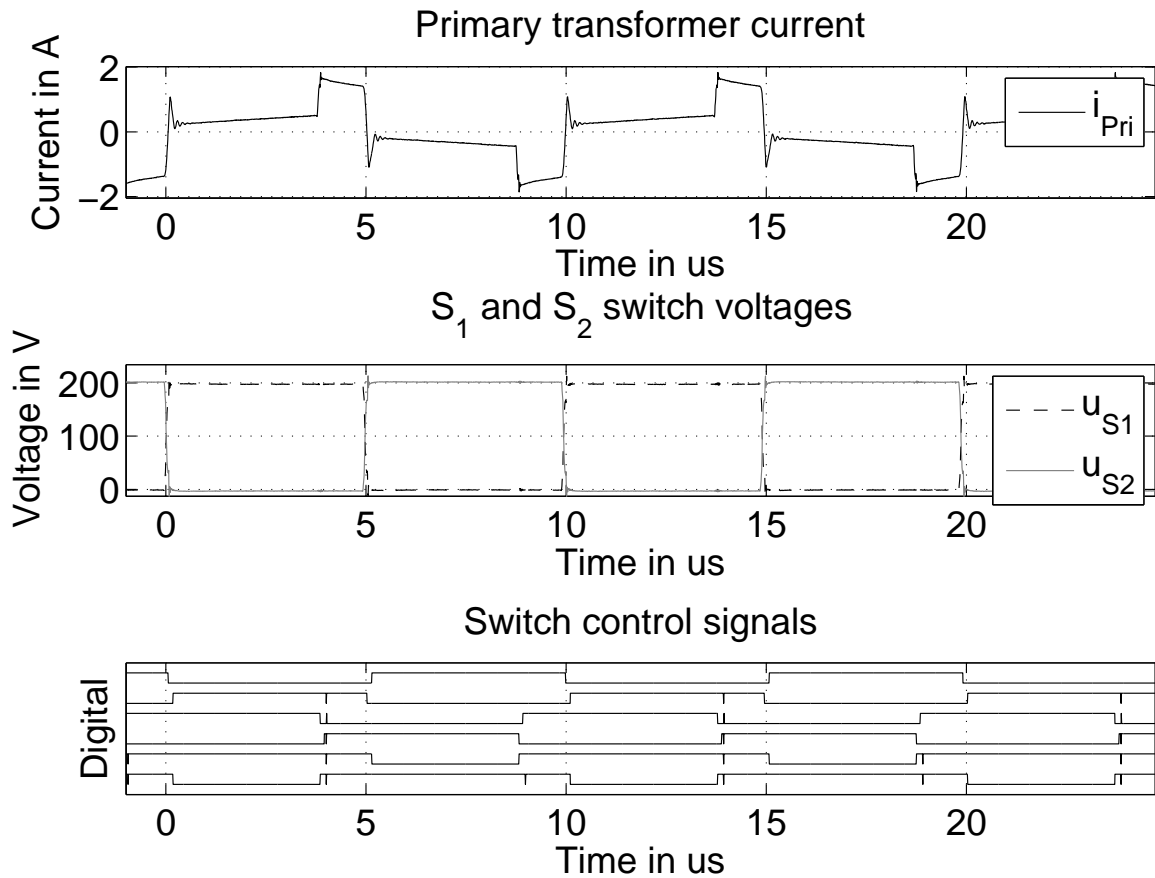


Figure 4.59: Measurement for normal operation with extended zero voltage switching at 10% load, (top) primary transformer current; (middle) voltages across S_1 and S_2 ; (bottom) digital signals for the switches S_1 (top most) to S_6 (lowest).

PS-ZVS bridge is not switching the voltages across the switches become half the DC-link voltage due to the capacitive voltage divider, which is formed with the parasitic output capacitors of the MOSFETs. In a traditional PS-ZVS application with a DC-link voltage of usually around 400 V and devices which have a breakdown voltage of 600 or 650 V, the voltage across one MOSFET during the pause in burst mode is at half the DC-link voltage at around 200 V and it is possible to just turn on the MOSFET, without reaching the breakdown voltage of the device, since there is enough headroom available. However in this proposed solution the headroom for reaching the breakdown MOSFETs is much smaller and a turn-on at half the DC-link voltages would hit the breakdown voltage of the device and may cause device failure or unwanted additional losses. In burst mode, when no switch is operating during the burst pause, the voltages across the switches settle at half the DC-link voltage and a turn-on of one MOSFET would destroy the other in series connected MOSFET due to a overvoltage spike because of the stray inductance and the high di/dt . Therefore some modification to the traditional burst-mode switching pattern is needed to reduce the voltage across the switches which should be turned on the first time after the pause in burst mode. After the inactive state of the PS-ZVS bridge, meaning no switch has switched for a longer time and all switches are in their off-state, one of the synchronous rectifier switches is switched on alone before any other switching operation happens. In case of an already established output voltage, energy is transferred back to the primary and it is possible to discharge nearly completely two of the output capacitor of the primary switches. This is shown and verified with measurement results in Fig. 4.60. It is shown that for example if the synchronous rectifier S_5 is switched on, the voltage across S_2 goes down and the voltage across S_1 goes up, this enables to turn on S_2 at nearly zero voltage and reducing the overvoltage spikes at the first turn-on after the burst break dramatically. During burst mode the measured output voltage ripple was measured with 700 mV at 10% load.

Fig. 4.60 further shows, that the primary current increases with each switching cycle. This is because the current in the output filter is dropping to zero during the pause in burst mode and it is necessary to build up the current again. Due to this the peak currents in burst mode are higher than in the normal operation mode causing higher resistive losses, which implies that for higher loads burst mode is no viable solution anymore since the resistive losses preponderate the switching and transformer loss. Another disadvantage of burst mode at higher loads is the ripple of the output voltage which might reach unacceptable values.

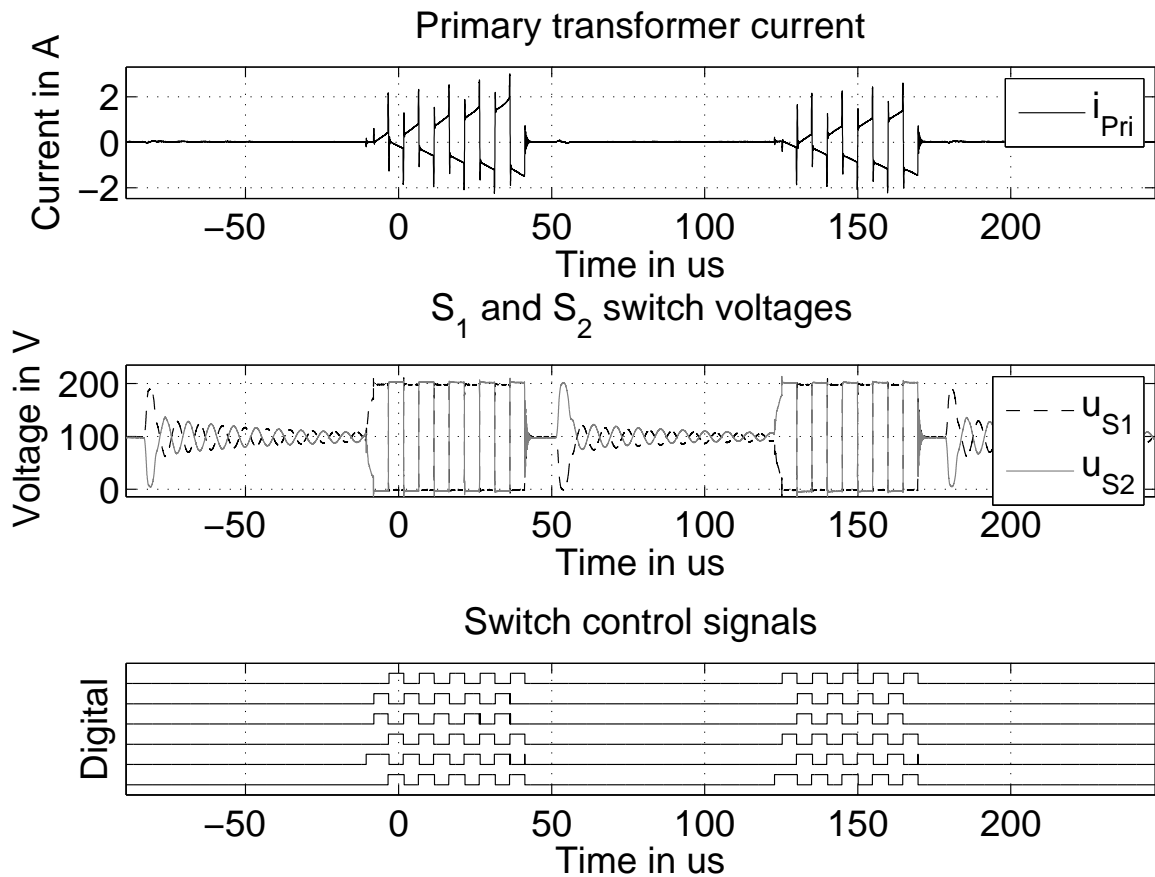


Figure 4.60: Measurement of the burst mode with the modified burst-mode pattern to reduce the voltage across the primary switches after the break; (top) primary transformer current; (middle) voltages across S_1 and S_2 ; (bottom) digital signals for the switches from S_1 (top most) to S_6 (lowest).

4.3.7 Measurement and simulation results

This section presents results obtained from simulation and measurements of the PS-ZVS bridge. Fig. 4.62 compares the simulated with the measured efficiency and additionally shows the advantage gained from changing to burst mode at low load. Burst mode is only viable at loads below around 10%. At 10% load it increases the efficiency by 1% compared to normal operation. For achieving the titanium criteria at low load burst mode is needed. The loss breakdown for the PS-ZVS bridge is shown in Fig. 4.61. At low load in normal operation the main losses are the off-switching loss and the transformer core loss. Towards higher loads the conduction losses increase, especially the conduction losses of the synchronous rectifier switches and from the transformer.

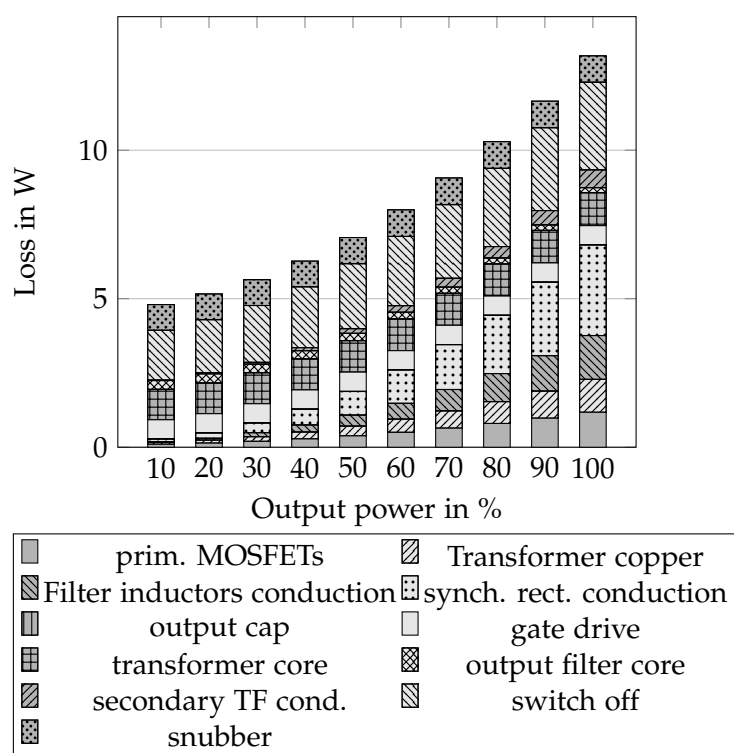


Figure 4.61: Phase shifted zero voltage switched bridge loss breakdown for 200 V DC link voltage over the load.

Another possible option to increase the low load efficiency was tested where the idea was to decrease the switching frequency at low loads, see Fig. 4.63. It can be seen that there is no gain in efficiency when the switching frequency is lowered. At half the normal switching frequency the switching losses and gate losses are reduced by half, but on the other hand the transformer core loss and the copper losses increase resulting in overall higher losses.

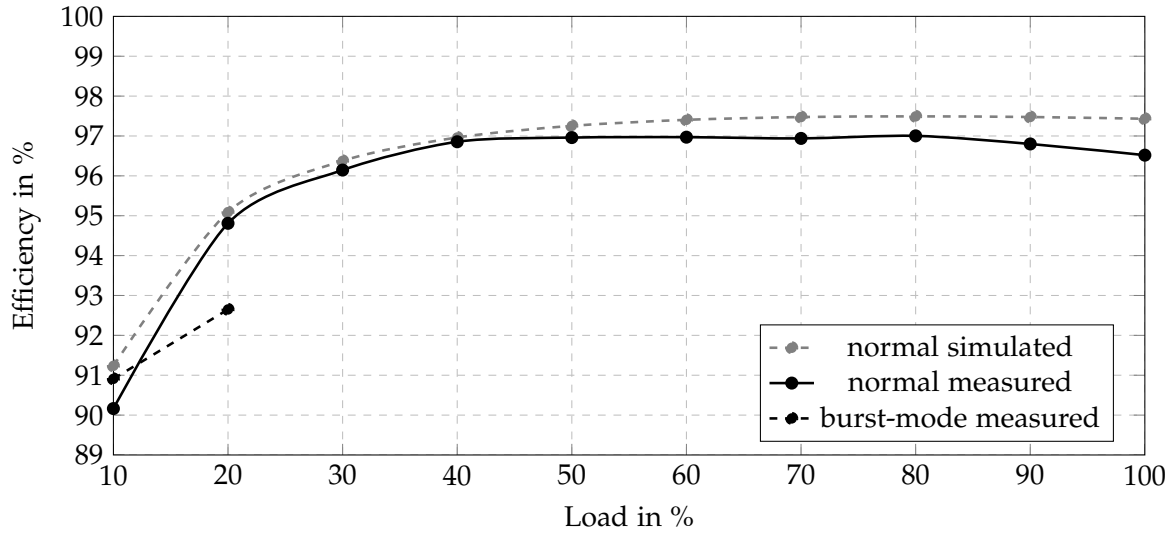


Figure 4.62: Simulated and measured PS-ZVS bridge efficiency over the load for normal operation and burst-mode operation.

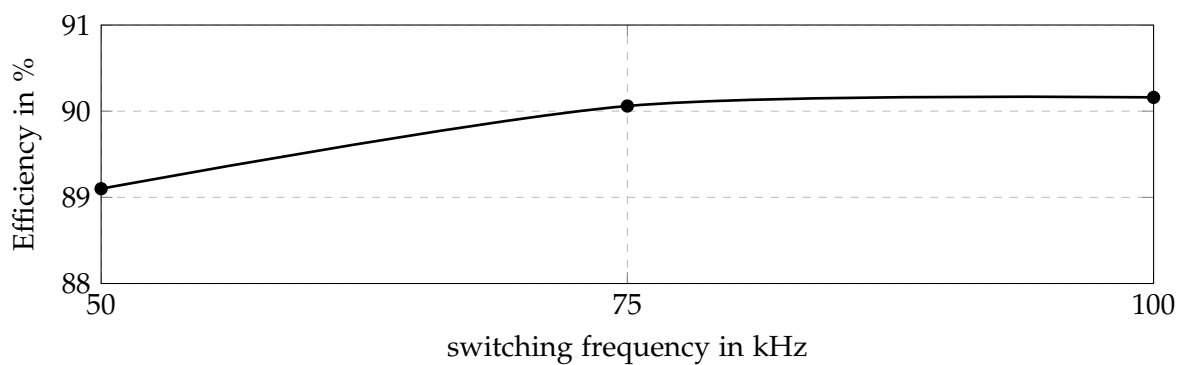
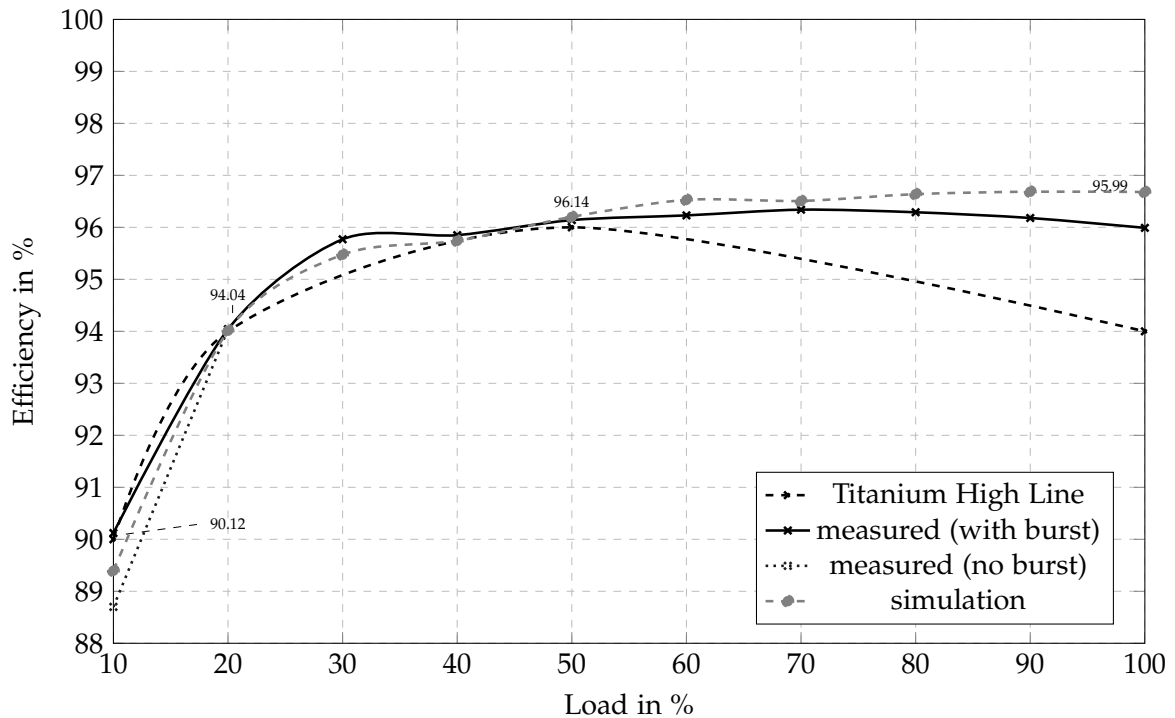


Figure 4.63: Measured PSZVS bridge efficiency at 10% load over the switching frequency.

4.4 Measurement results of a complete module

This section presents the obtained efficiencies for a complete module and compares the obtained efficiencies with the efficiencies required for achieving titanium certification. Fig. ?? presents the measured and simulated efficiencies for a complete module, which are in good agreement. It can be investigated, that it is necessary to switch to burst mode operation for achieving the titanium certification at light load, where it then achieves an efficiency of 90.12%, increasing the efficiency by more than one percent at 10% load. At 20% load burst mode is already counterproductive due to the increased rms currents, therefore the PS-ZVS bridge operates at 20% load again in normal operation, achieving 94.04% which is really close to the requirement. The 50% load point was measured with 96.14% also just slightly above the requirement where the efficiency is then nearly flat to full load. To further increase the efficiency a better transformer construction, especially for the secondary which is due to the center tap pretty difficult to assemble manually should help. Using professional machines to do so would for sure allow to put more copper inside the transformer which will reduce the losses.

Since every module always sees independent of high or low line the same input voltage, the total efficiency of both modules is always the same, which also proves that the power supply reaches at low line input the high line titanium requirements.



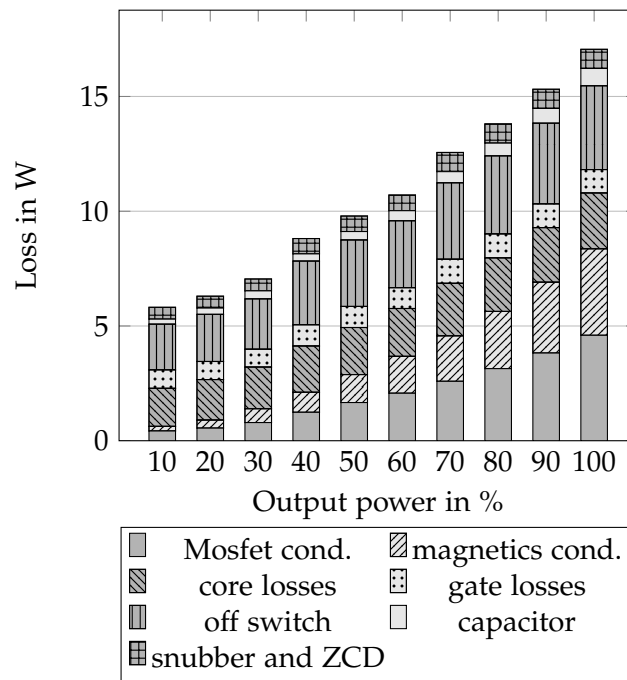


Figure 4.64: Loss breakdown over load for the complete module.

Fig. 4.65 shows the thermal images for the whole module in operation for half and full load. It can be seen that at half load one of the boost inductor is cooler compared to the other two since the third phase is inactive. At full load all three phases of the PFC are active and all have the same temperature. For both half and full load cases the transformer is the main hotspot, reaching over 90 °C at full load with natural convection.

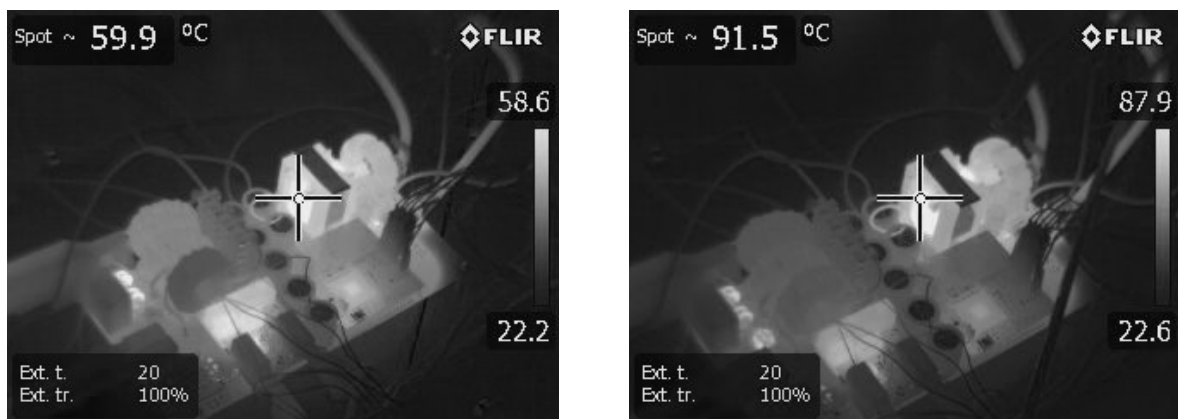


Figure 4.65: Thermal images of one module in operation; (left) at 50% load; (right) at 100% load.

4.5 Multiple modules sharing parameters

Theoretically for modular converter systems four different connection methods for the inputs and outputs are possible: Input Parallel Output Serial (IPOS), Input Parallel Output Parallel (IPOP), Input Serial Output Serial (ISOS) and Input Serial Output Parallel (ISOP), where the IPOP is today due to redundancy requirements in server power supplies the most common configuration [66]. All these modular converter concepts require for a stable operation that the input voltage is distributed equally among the modules, which is always true for IPOS and IPOP systems and depending on the output configuration that either the output voltage or the output current is shared equally [67], which often requires to measure either the output or the input current of the converter, [68–70]. The here proposed solution connects the outputs of the PS-ZVS-bridges in parallel, requiring of each PS-ZVS-bridge the full output voltage, but only half the current, resulting in an ISOP or in an IPOP system. Another possibility would be an ISOS system by connecting the PS-ZVS-bridge outputs in series, requiring then half the output voltage but double the current. In this ISOS configuration a different topology like the current doubler might be favorable for higher efficiencies, since the voltage is quite low and the output current is quite high, as shown in [71]. The ISOS configuration was analysed in [70] where it was stated that this configuration is naturally not stable and already small mismatches in the turns ratios of the transformers leads to instability. In [72] it is theoretically and experimentally shown that it has a weak rebalancing mechanism and further by including the magnetic losses and resistance of the transformer, which is true for every real transformer, another strong balancing mechanism was found in theory, if the converters are operated interleaved with the same duty cycles. In the practical circuit it was shown that interleaved operation of the converter is not really required for balancing, since a higher voltage for one module results in increased core losses and switching losses, naturally balancing the output voltage again, but the balancing speed is improved, if interleaving is used. In [67] it is analytically and experimentally shown that by balancing the input voltages of the modules, output current sharing for ISOP or output voltage sharing for ISOS modules is achieved without any current measurement, which is shown with eq. (4.36),

$$\begin{aligned} u_{inM1} i_{inM1} \eta_{M1} &= u_{outM1} i_{outM1} \\ u_{inM2} i_{inM2} \eta_{M2} &= u_{outM2} i_{outM2}, \end{aligned} \quad (4.36)$$

where η_{Mn} is the efficiency for the module. For an ISOP system the input currents and the output voltages are equal and it can further be stated eq. (4.37),

$$\frac{u_{inM1} \eta_{M1}}{u_{inM2} \eta_{M2}} = \frac{i_{outM1}}{i_{outM2}}, \quad (4.37)$$

showing that if the input voltages of the modules are equal, also the output currents will be equal under the assumption of similar efficiency of the modules [67]. The feedback value from the control of the PS-ZVS-bridge is then realized with only one module, the master module, which is measuring the output voltage and adjusting the duty-cycle. It is important that the output voltage is only measured with one module since the always present measurement error would make it impossible to equally share the current if every module measures its own output voltage and has its own control loop. The second module, or slave module, receives the duty-cycle from the master and then generates with that information its own switching-pattern. Another and more accurate possibility requires to measure the output current for each module and implement an additional control to equalize the currents between the modules. This can be done with various methods, where in one for example the output voltage decreases with increasing output current, also called droop method, see Fig. 4.66, which is done by adjusting the output impedance or with active current schemes, where the measured current is utilized in a control structure. For the droop method it can be stated that the higher the droop (or ΔU) the better the current sharing is. Droop methods can be realized by utilizing the inherent droop features of a converter, like present in a buck or boost in discontinuous conduction mode, which is the cheapest solution but it does not deliver a tightest output current sharing. Another possibility is to insert a resistor in series to the output, to generate the voltage droop with increasing output current, which is usually used only for small powers since the resistor will dissipate a lot of power at for higher ΔU . Another solution utilizing the droop method could be to measure the output current and reduce the output voltage proportional or also non-linear to the measured output current, reducing the output voltage for higher output currents. By eliminating the integrator in the feedback transfer function the DC-gain can be reduced which delivers also a droop of the output voltage. The droop method for sharing the output load amongst multiple converters has the advantage that no communication between the modules is required and its simplicity in implementation. The disadvantage is that the load regulation is not at an optimum and the current sharing can not be perfect. [73]

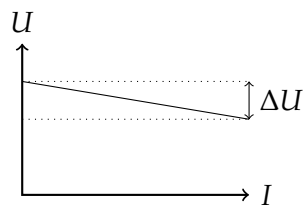


Figure 4.66: Droop method explanation; the higher the output current the lower the output voltage.

For active current schemes different control structures are possible with different current-programming schemes. It is possible to share the current equally with an inner loop regulation where the reference voltage feedback and compensator is shared across the modules, enabling a stable current sharing and precise output voltage regulation with the disadvantage of poor modularity and poor fault-tolerance. Opposed to the inner loop current regulation an outer loop regulation is another possibility where each converter has its own independent output voltage feedback, where the output voltage is regulated in the inner control loop. The outer loop regulation has advantages in a higher flexibility for expansion of the system, higher fault tolerance, in case a single module is failing, and a good modularity, but it might be unstable if the DC gain of the voltage feedback is infinite. The third possibility is the utilization of an external controller which compares all load sharing signals for each module and adjusts their feedback signals, requiring a lot of connections between the modules but has the advantage that interleaving of the modules is easy to implement to lower the output ripple at the cost of modularity and maybe reliability due to the required interconnections. [73]

For the active current sharing two methods exists for sharing the current equally, where one is the average current-programming method and the other is the master/slave current programming method. In the average current-programming method the factors μ_i in Fig. 4.67 are chosen to be one and the weighting factors $W_i(s)$ are the gain which is proportional to the current for each module. Each module provides a signal which relates to its own output current where the sum of all the output current related signals of the modules represents the average output current. Depending on the weighting factor the current sharing between the modules can be adjusted, in case of equal weighting factors, the current is shared equally between the modules. By subtracting the own output current with the weighted average output current the current sharing error i_{ei} is calculated and can be used to adjust the output of the converter. [73]

For the master/slave current-programming concept one u_i is one (which is the master) and rest are zero and all $W_i(s)$ are set to one. The output current of the master is then the reference for the other modules, achieving output current sharing. [73] For the prototype the master module transmits the average input current for the PFC and the duty cycle for the PS-ZVS bridge to the slave module which enables current sharing between the modules. The modules are always split into a master and a slave module, regardless of serial or parallel connection of the module inputs and the outputs of the modules are always connected in parallel. The communication between the modules is handled with the Serial Peripheral Interface (SPI) protocol. Additionally it is required, that the master module tells the slave module, when it starts the PFC operation and how many phases are active. If both PS-ZVS bridges are operating the DC-link voltage is shared automatically between the modules, which can go that far, that in case of no current sharing the output

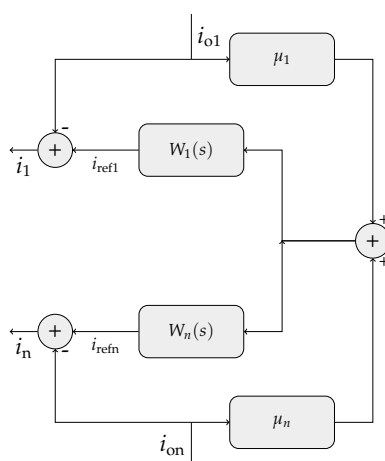


Figure 4.67: Block diagram for current-programming, where i_{oi} is the output current of the module and i_i is the adjusted current.

current of one module can reverse reversing also the power and transferring energy to its DC-link capacitor, which can be seen as an additional stabilizing effect.

4.5.1 Operation at low line input

At low line input both modules are operated with the inputs and outputs connected in parallel. It was experimentally investigated, that by slightly lowering or increasing the duty-cycle of the PS-ZVS bridge received from the slave module by a constant value, the degree of how the DC-link voltages equalize to each other can be set. The output current sharing is nearly un-affected by small duty-cycle changes. For changing the current sharing ratio between the modules, it is required to change the value for the average current of the PFC. The average current for the PFC is also transmitted to the slave so they equalize the drawn input power to each other which results then in an equalized output power.

4.5.2 Operation at high line input

At high line input the inputs of the modules are connected in series and the outputs in parallel. For the serial operation it is as well required to balance the input voltages, which requires, that the drawn input power of the modules are equal. To achieve this it is, as already mentioned, important that the operation of the PFC is synchronized and that both PFC always operate with equal amount of phases. The measurement results for high-line input (230 Vac) are shown in Fig. 4.68. The slight imbalance of the input voltages is due to the imperfect measurement due to the used error amplifiers.

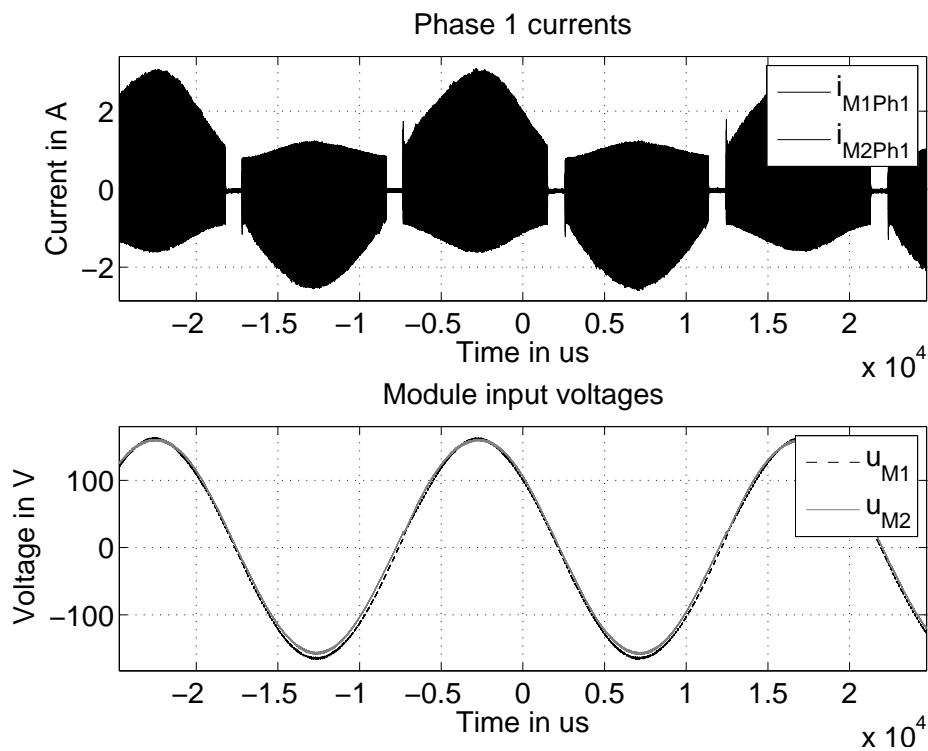


Figure 4.68: Measurement of both modules running at 230 V in series connection; (top) currents of phase 1 of module 1 and 2; (bottom) module input voltages.



Conclusion

5.1 Conclusion

This work proposes a new method of how low voltage MOSFETs can be utilized in high voltage applications by a new modular approach by connecting modules either in parallel for low input voltages or in series for high input voltages. The goal of this thesis is to demonstrate this new method and that the better FOM of low voltage MOSFETs compared to high voltage MOSFETs can be exploited and therefore opening a new way for achieving higher efficiencies to meet the today's highest efficiency requirements for SMPS, which is at the time of the thesis the titanium requirement by the 80plus organization. Incorporating this new concept allows to achieve independent from the mains voltage the same efficiencies, which is typically impossible in a standard configuration with high voltage MOSFETs for SMPS.

To prove the new concept the SMPS was simulated and experimentally verified with a demonstrator delivering 1 kW of power for an output voltage of 12 V and a power density of 1 kW/dm³. The SMPS consists of two identical modules, where each module comprises a PFC and a DC/DC conversion stage. For the verification the measured efficiencies over the whole load range are compared with simulated efficiencies and additionally important waveforms of the converter in operation are shown. The measured efficiencies are high enough to fulfill the up to today strictest requirement of titanium level for high line input by the 80plus organisation independently of a high or low line input voltage by reconfiguration of the connection of the modules either for parallel or serial operation. It is shown that with traditional silicon semiconductors and a well known DC/DC converter stage, a total peak efficiency of more than 96% can be achieved.

5.2 Outlook and possible improvements

Higher efficiencies can be achieved by replacing the PS-ZVS bridge with a more complicated DC/DC conversion stage like an LLC converter, opening the way for the next to come efficiency level by the 80plus organization, where the LLC converter promises especially for low load conditions an improvement in efficiency and a general improvement in power density. Another efficiency gain might be achievable by increasing the module count for the SMPS, which allows for even lower voltage MOSFETs. Further research in this area is, as already shown in a previous chapter, under progress and interested readers can read up the following papers, [14–16]. At the time of the thesis the 250 V switches were only available in the technology used for OptiMOS 3, where a newer technology from Infineon, used for OptiMOS 5, is already commercially available, but only up to 100 V. A further increase in efficiency is expected, when the next technology generation will also be available for 250 V.

For a tighter current sharing capability between the modules a current measurement, for instance on the outputs of the DC/DC conversion stages can be implemented, which allows for an active current sharing control between the modules. By measuring the output current for each module further the timings for the synchronous rectifier switches on the output of the PS-ZVS bridge could be realized with an adaptive delay improving the efficiency towards higher loads.

Utilization of wide bandgap devices, new topologies like the following mentioned multi cell topologies might allow to continue the trend in power electronics since 1970, where the power density of converters doubled every 10 years [74]. Along with advances in new magnetic materials (which are of limited speed) this seems possible and in the following a short overview of wide bandgap devices and multi cell topologies is given.

5.2.1 Future of Wide Bandgap Devices

For the near future new wide bandgap semiconductor materials like SiC or GaN are emerging offering new possibilities for converters as they promise a significant boost in performance viewed on the switch level. They promise to achieve an order of magnitude lower on resistance and break the superjunction Si-limit defined by [75], higher possible junction temperatures and the capability of extremely fast switching speeds. But along with those advantages new problems arise and research is still required. The possibility of higher junction temperatures requires the development of new packages. Optimizing costs strives to build GaN devices on a silicon substrate compared to a more expensive SiC or sapphire substrate, but the big difference of the temperature expansion coefficient between GaN and

silicon which is approximately two times lower than GaN is not yet completely solved. Today, switches made out of GaN or SiC are already commercially available but their reliability in field is not proven with the exception of SiC schottky diodes which are since 2001 on the market [76] and just replacing silicon switches with wide bandgap devices is usually not cost efficient. A comparison between SiC and silicon devices in [77] on a system level for instance showed that for low voltage inverter drives which switch with a low switching frequency SiC devices would not offer an advantage over silicon devices. In other areas like converters for photovoltaic where high conversion efficiencies save effectively the cost for additional panels SiC devices will pay for themselves over time. Although for increasing voltage and power levels SiC devices offer a much higher potential to replace silicon devices in the near future. For SMPS SiC devices offer a potential to improve the power density and/or efficiency or reduction of the chip area of approximately 35%, as shown for a PS-ZVS DC/DC converter in [77]. The opinion that SiC devices will offer an improvement over superjunction MOSFETs and IGBTs for higher voltage ranges like 1.2 to 1.7 kV and even higher is also represented in [76]. Even more promising than SiC devices are GaN devices which are more suited for SMPS due to their aimed voltage range of 200-900 V. They offer performance improvements for PFC, DC/DC, electric and hybrid electric vehicles and solar inverters just to name a few. A prototype of an LLC converter running at a switching frequency of 1 MHz utilizing GaN switches shows for example a possible efficiency of 95.4% with a power density of 50 kW/dm³, [12, 13]. It is expected that by 2018 GaN devices will be able to compete in terms of cost with silicon devices [78] and that SMPS as well as other converters will improve further in power density and/or efficiency.

5.2.2 Multi cell topologies

Another step to further improve the power density and efficiency or other aspects like an improved EMI behaviour of converters without the need of wide bandgap devices is possible with multi cell topologies. In multi cell converter topologies basic converter topologies can either be connected in series or in parallel. For converter cells which are connected in series the input voltage is shared equally between the cells reducing the input voltage for each cell. Additionally interleaved operation is possible, increasing the effective switching frequency of a cell with the number of cells and therefore decreasing the ripple of the input current. Further, since the input voltage is divided the necessary blocking voltage for the switches can be reduced enabling the utilization of devices with a lower on-resistance, which acts like a shift in the silicon limit towards lower specific on-resistances. Further, switching losses are reduced depending on the amount of cells in series [16]. For parallel operation of multiple converter cells again an improvement in conduction loss, switching loss and harmonic distortion compared with a typical *one cell* converter is achieved.

The above mentioned effects are valid for all semiconductors, not just for silicon devices making further research in this area even more interesting, especially for high voltage applications where it is then possible to use lower voltage devices. Another advantage of multi cell topologies is the possibility of higher efficiency during part load conditions. In parallel systems, like for instance a multi phase TCM PFC phases can be switched off at lower loads reducing the losses. In serial configured systems parts of the system like the DC/DC converter can be inactive for an ISOP system during partial load like suggested in [79] which again allows for an increase in efficiency. Another experimentally verified ISOP multi cell approach is shown in [80], where an efficient conversion with only one conversion stage from 54 V down to 1.8 V with 30 V MOSFETs was shown. For future research in SMPS it might be interesting to combine multi cell topologies with low voltage wide bandgap devices. This combination promises due to the higher switching speed capabilities and improved FOM of the devices even higher power densities and or higher efficiencies.



Loss Modelling and Simulation

A.1 Semiconductor losses

The used semiconductors in the power part of the prototype were entirely MOSFETs and power-diodes, where power-diodes have a forward voltage drop and a reverse recovery charge. The forward voltage drop depends partly on the conducted current, as can be seen in Fig. 4.43 for a power schottky diode. This forward voltage drop is in simulation for simplicity assumed to be constant. Secondly diodes have a reverse recovery charge Q_{rr} , which lets flow a current in the reverse direction for a short time t_{rr} . During this time the device loses its blocking capability. Since no real power diodes are used in the converter this effect is neglected from the loss calculation. For the converter only MOSFETs were used, but as already described in section 2, all power MOSFETs have a built-in body diode. This body diode was approximated with an ideal diode without reverse recovery charge and a constant forward voltage drop. The MOSFETs were modelled with an ideal switch, a parallel parasitic non-linear output capacitance C_{OSS} , see Fig. A.2, a parallel body diode and parasitic inductances, see Fig. A.1 for the here described equivalent circuit.

A.1.1 Conduction loss

The losses of the body diodes are calculated with eq. (A.1). As mentioned the forward voltage drop V_F is assumed to be constant.

$$P_{cDiode} = V_F \cdot i_F(t). \quad (A.1)$$

The on-resistance R_{DSon} of the MOSFETs is included in the ideal switch of Fig. A.1. The conduction losses when the MOSFET is switched on can be described with eq. (A.2).

$$P_{cMofset} = R_{DSon} \cdot i_{DS}(t)^2. \quad (A.2)$$

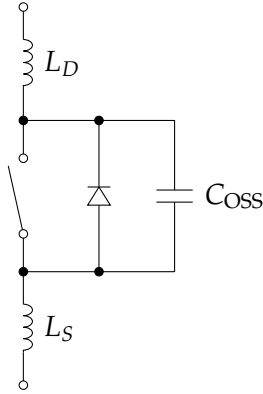


Figure A.1: Equivalent circuit in the simulation for a MOSFET.

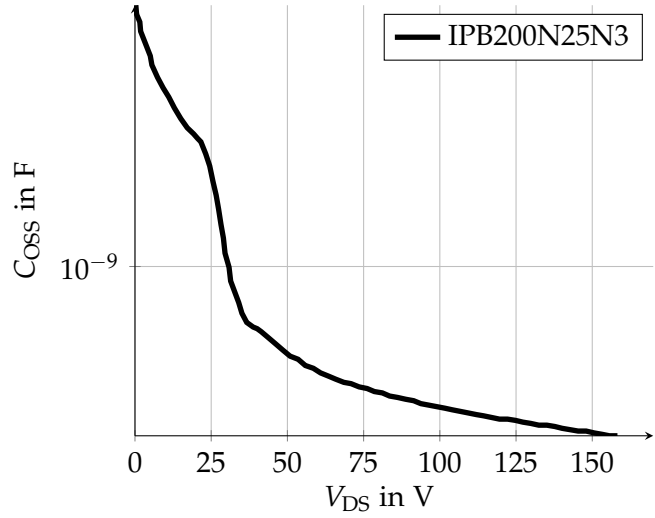


Figure A.2: Output capacity over V_{DS} from the used MOSFETs for the PFC and the primary side of the DC/DC converter.

A.1.2 Switching loss

Another loss source of MOSFETs is the switching loss. The switching loss can be divided into an on and an off-switching loss. In this converter every switch is always switching on under zero voltage conditions, therefore the on-switching loss can be assumed with zero. In reality a small portion of the charge, which is stored in the output capacity is lost even at a zero voltage turn on, but this has been neglected. In a hard switching topology the whole charge stored in the output capacitor is lost at every turn on, limiting the maximum switching frequency and therefore the power density of the converter. There is also an off-switching loss, when the MOSFET is switched off with a current still flowing in the moment of the turn-off, which generates losses and can be approximated with the assumption that at turn-off the current i_{DS} is falling linear to zero and the voltage u_{DS} is increasing linearly to the blocking voltage of the MOSFETs, see Fig. A.3.

The approximated off-switching loss visualized in Fig. A.3 can be calculated with eq. (A.3).

$$P_{\text{off-sw}} = \int_{t_1}^{t_2} u_{DS}(t) \cdot i_{DS}(t) dt = \frac{u_{DS}(t_2) \cdot i_{DS}(t_1) \cdot (t_2 - t_1)}{6}. \quad (\text{A.3})$$

The waveform in Fig. A.3 shows the waveform for switching a resistive load. Usually in converters inductive loads are switched and the waveform is different, see Fig. A.4.

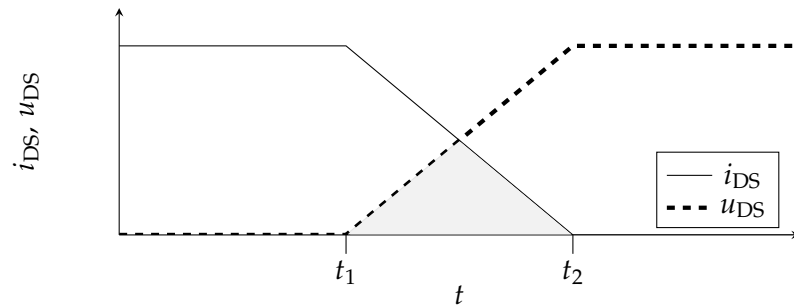


Figure A.3: Approximation for the off-switching loss of a MOSFET under current with a resistive load; the gray triangle where the current and the voltage overlap is the off-switching loss.

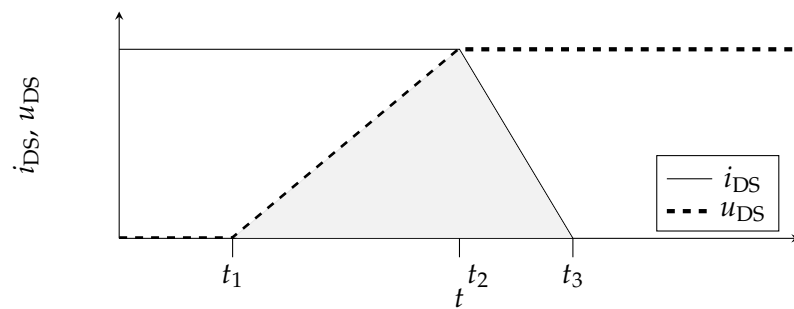


Figure A.4: Approximation for the off-switching loss of a MOSFET under current with an inductive load; the gray triangle where the current and the voltage overlap is the off-switching loss.

For an inductive load the off-switching loss can be approximated with eq. (A.4), and it can be seen, that for inductive loads the off-switching losses are three times bigger compared to the case with resistive load.

$$P_{\text{off-sw}} = \int_{t_1}^{t_3} u_{\text{DS}}(t) \cdot i_{\text{DS}}(t) dt = \frac{u_{\text{DS}}(t_2) \cdot i_{\text{DS}}(t_1) \cdot (t_3 - t_1)}{2}. \quad (\text{A.4})$$

For turning a MOSFET on a voltage between the gate and source is required to charge the gate capacitors. The MOSFET has a capacitor between the drain and the gate, C_{GD} and between source and the gate C_{GS} , see Fig. A.5 and the breakdown of the gate charge as shown in Fig. A.6.

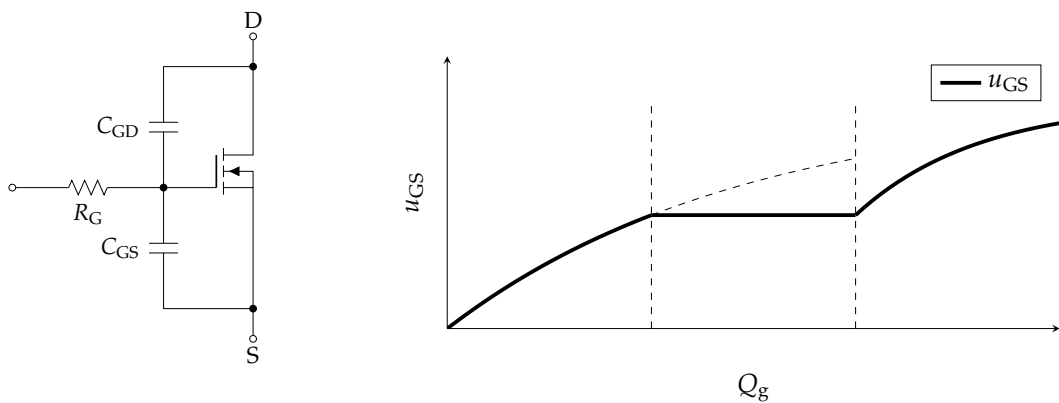


Figure A.5: Equivalent circuit for the capacities at the Gate of a MOSFET.

Figure A.6: Breakdown of the gate charge.

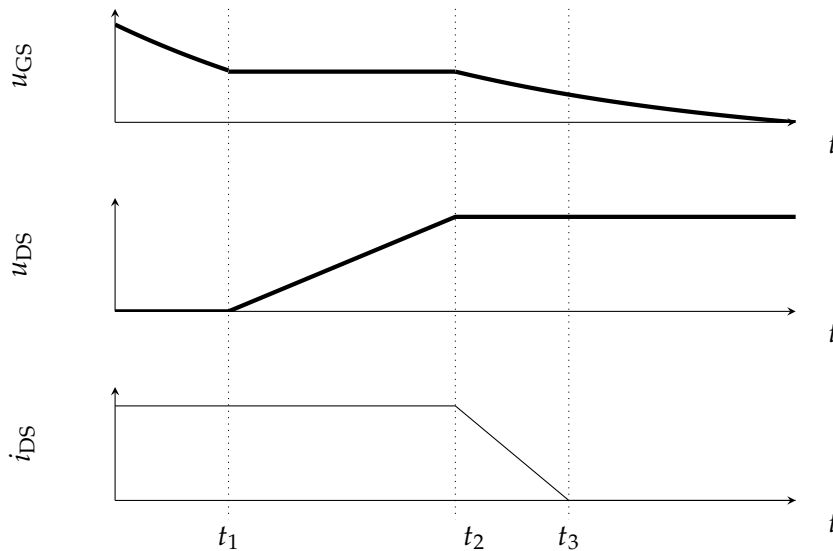


Figure A.7: Turn-off waveforms with the gate voltage of a MOSFET.

The switching times can be extracted from the data given in the datasheet, [21]. Therefore the timings which are needed for the drain-source voltage u_{DS} to rise and the drain-source current i_{DS} to ramp down can be calculated. When the gate capacitors are discharged over the gate resistor, at first no changes can be examined in u_{DS} or i_{DS} , until the gate voltage is so low that the MOSFET saturation current is the actual load current, see Fig. A.7. In this time also C_{GD} is constant since the drain-source voltage u_{DS} is still constant. The gate-source voltage u_{GS} decays exponentially and can be described with eq. (A.5), where it is also possible to calculate the time to reach the miller-plateau voltage U_{GP}

$$u_{GS}(t) = u_{GS} \cdot e^{\frac{-t}{R_G[C_{GS} + C_{GD}(on)]}}, \quad (\text{A.5})$$

where $C_{GD}(on)$ is gate-drain capacity when the MOSFET is turned on. This time required to discharge the gate-source voltage to the miller-plateau can be viewed as a turn-off delay. After the gate is discharged to the miller-plateau the drain-source voltage u_{DS} increases, while the current still remains constant. The time where u_{GS} is at the miller-plateau voltage U_{GP} and the drain-source voltage u_{DS} rises, can be calculated with eq. (A.6)

$$t_2 - t_1 = R_G C_{GD} \frac{U_{DSoff} + U_{FD} - U_{DSon}}{U_{GP}}, \quad (\text{A.6})$$

where R_G is the total gate resistance, $C_{GS,avg}$ is the constant averaged gate-source capacity, U_{DSoff} is the voltage across drain-source when the MOSFET is switched off, U_{DSon} is the conduction voltage when the MOSFET is turned on and U_{FD} is the forward voltage drop of the internal body diode. After this time the gate-source voltage u_{GS} can decrease down to the threshold voltage, where the channel is closed and the drain-source current i_{DS} is zero. This time can be calculated with eq. (A.7). After t_5 the gate-source voltage u_{GS} decreases further exponentially to zero.

$$t_3 - t_2 = R_G [C_{GS} + C_{GD}(u_{DS})] \ln\left(\frac{U_{GP}}{U_{th}}\right). \quad (\text{A.7})$$

Since in datasheets usually no values for C_{GS} and C_{GD} are given, the formulas have to be adapted for values which are available in the datasheets, [81]. This is done by replacing $C_{GD,avg}$ with $Q_{GD}/u_{DS}(t_2)$ (neglecting the diode forward voltage drop), and $C_{GS} + C_{GD}(u_{DS})$ with $C_{iss}(u_{DS}(t_2))$ and with the substitution of U_{GP} , under the assumption that the transfer characteristic is constant, with eq. (A.8)

$$u_{GP} = u_{th} + \frac{i_{DS}(t_2)}{g_{fs}}, \quad (\text{A.8})$$

where u_{th} is the gate threshold voltage and g_{fs} is the transconductance. By neglecting the diode forward voltage drop and the conduction voltage, since they are very small compared to the drain-source voltage u_{DS} , the equations for the times can be rewritten, see eq. (A.9)

$$t_2 - t_1 = \frac{R_G Q_{GD}}{U_{th} + \frac{i_{DS}(t_2)}{g_{fs}}} \quad (A.9)$$

$$t_3 - t_2 = R_G C_{iss}(u_{DS}) \ln\left(\frac{u_{th} + \frac{i_{DS}(t_2)}{g_{fs}}}{U_{th}}\right).$$

The timings from eq. (A.9) can be put into eq. (A.4) to calculate the off-switching loss. [21, 81]

A.1.3 Gate loss

To turn the MOSFET on it is necessary to apply a gate voltage to open the channel. With the applied gate-voltage U_G , first the gate-source capacitor is charged to the threshold voltage u_{th} at the time point t_1 where then the drain-source current starts to rise from zero, see Fig. A.8, to the maximum drain-source current when the gate-source voltage reaches the miller-plateau. During the miller plateau from t_2 to t_3 the gate-drain capacitor C_{GD} is charged and the drain-source voltage is decreasing. After the miller plateau at t_3 the drain-source voltage is constant at u_{DSon} and therefore the gate-drain capacity is constant. When the drain-source voltage is low the gate-drain capacity is bigger due to its non-linearity and the slope of the gate-source voltage u_{GS} is smaller compared to the period before the miller plateau, since C_{GS} has now a bigger capacitance in parallel. After t_3 an increase of the gate-source voltage just leads to a reduction of the on-resistance R_{DSon} . Due to the

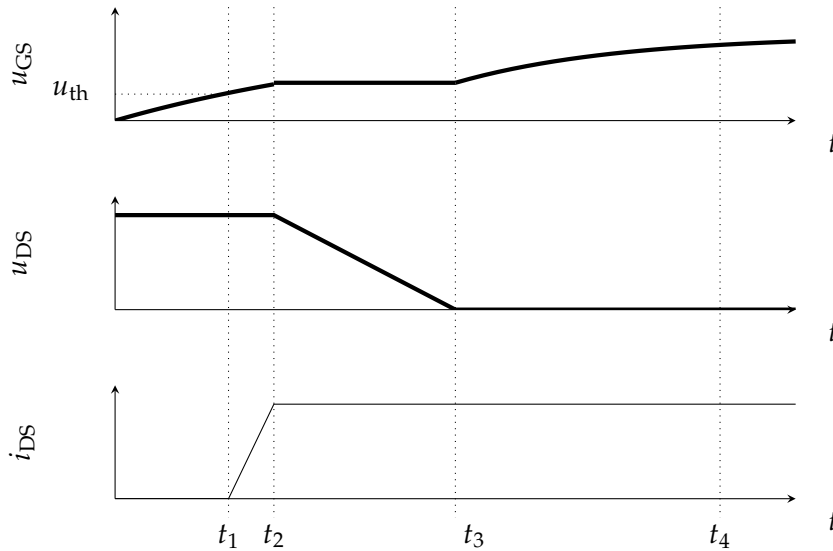


Figure A.8: Turn-on waveforms with the gate voltage of a MOSFET.

non-linearity of the gate-drain capacity C_{GD} datasheets usually also supply for designers the gate charge Q_g , which is the integral of C_{GS} and C_{GD} over the gate-source voltage V_{GS} , see eq. (A.10), while the drain-source voltage u_{DS} is at a constant value.

$$Q_g = \int_0^{t_4} u_{GS}(t) \cdot dt. \quad (\text{A.10})$$

The gate drive losses were estimated by counting the turn-on events of every switch and were then calculated with eq. (A.11) with Q_g as the gate charge and U_{Gate} as the gate driver supply voltage.

$$P_{Gate} = Q_g \cdot U_{Gate}. \quad (\text{A.11})$$

A.2 Core loss

Losses in the magnetic components must be considered in order to predict accurately the overall efficiency of a converter. To calculate the core loss various methods exist already. A widely used method is the empirical method by Steinmetz, see eq. (A.12), [82–84],

$$P_{VCore} = k \cdot f^\alpha \cdot \hat{B}^\beta, \quad (\text{A.12})$$

where k , α and β are called the Steinmetz parameters, which are often supplied from manufacturers. The problem with the Steinmetz equation is that it is only valid for sinusoidal flux waveforms, which is not often the case in power electronics leading to inaccurate results. For this an improved Generalized Steinmetz Equation (iGSE), is presented, [85]. With this method the accuracy for non-sinusoidal waveforms is more accurate. From the past up to today a lot of research to refine the Steinmetz equation for allowing even more accurate predictions of core loss was done. All this up to now mentioned methods only account for the hysteresis loss and the eddy current loss. The hysteresis loss is the energy needed to change the alignment of the atomic dipoles, when an external magnetic field is applied. When the atomic dipoles are aligned, most of them will stay aligned, even if the external magnetic field is removed. When an external magnetic field of the opposite direction is applied, they change their alignment, which causes losses. The losses increase linear with the frequency of the external magnetic field. Eddy current losses in magnetic materials are caused by the changing magnetic field, which induces electric currents in the material, called eddy currents. This losses are dependent on the conductivity of the core material, the geometry and also from the frequency of the applied magnetic field. They increase quadratically with frequency of the applied magnetic field. Ferrites or powder core materials have a low conductivity, therefore the eddy current losses are small. The third loss source represent the relaxation losses, which occur when the voltage across the magnetic component is zero which also implies that the magnetic flux is zero, [86]. Even

then losses occur in the magnetic material as shown in [86, 87], which differ from the iGSE especially if lower duty cycles are utilized. In [88] the relaxation losses are described as losses which occur if the thermal equilibrium of a magnetic system is suddenly changed, the system tries to reestablish the equilibrium with the relaxation process. To predict also the relaxation process in magnetic materials [86] added another factor to the iGSE, creating the i^2GSE (improved improved Generalized Steinmetz Equation) also showing a very good coincidence of the total losses from measurement and prediction. The method utilizes the already given Steinmetz parameters but also requires additional material specific parameters, which have to be measured. Since no measurement setup was available for measuring the magnetic materials for these additional parameters only the iGSE was used for the core loss prediction. The iGSE is shown in eq. (A.13)

$$P_{VCore} = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^\alpha (\Delta B)^{\beta-\alpha} dt, \quad (A.13)$$

where dB is the peak-to-peak flux density, α and β can be used directly from the given Steinmetz parameters and k_i can be calculated from the Steinmetz parameters, see eq. (A.14).

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^\alpha 2^{\beta-\alpha} d\theta}. \quad (A.14)$$

The factor k_i can also be approximated without solving the integral above by eq. (A.15), which is valid for values of α from 0.5 to 3.

$$k_i = \frac{k}{2^{\beta+1} \pi^{\alpha-1} (0.2761 + \frac{1.7061}{\alpha+1.354})}. \quad (A.15)$$

A limitation of the iGSE is the varying core loss with DC-bias, [89–91] which is not taken into account. A DC bias alters the Steinmetz parameters and only the frequency dependent parameter α is independent of the DC bias, at least up to measured values of 100 kHz, [90]. There is also mentioned, that the additional loss caused by DC bias is negligible for MPP and silicon steel materials. For ferrite and nanocrystalline materials the DC bias loss can be calculated, but to do so measured values under premagnetization are necessary to accurately predict the total losses.

A.2.1 Core loss in the boost cores

The losses in the boost cores were calculated with the iGSE, see eq. (A.13) and eq. (A.14). For the PFC stage the sinusoidal input line voltage waveform was split into n parts [92], [93], see Fig. A.9. For each time interval the actual value of the sine was approximated with a constant DC voltage and the triangular current shape according to Fig. 4.6, see section 4.2, for the specific DC input voltage is calculated. Then, for this triangular input current the magnetic field strength H and with the material specific $B - H$ curve the magnetic flux

density B was determined. Together with the Steinmetz parameters from the manufacturer and eq. (A.13) the core losses P_{cn} for this specific part of the sine are calculated. This has been done n times for every part of the first quarter of the line input voltage sine. Afterwards the total core loss is equal the average of all P_{cn} .

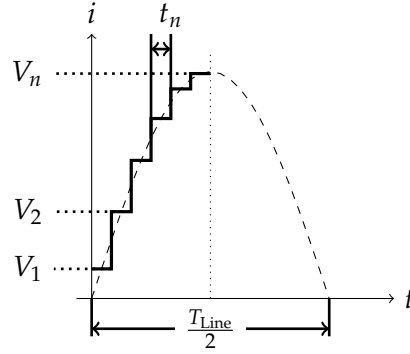


Figure A.9: Splitting of the input current sine for the PFC for a fast core loss estimation.

With the known parameter of the boost-inductor the magnetic field H can be calculated, see eq. (A.16)

$$H = \frac{N \cdot I}{l_e}, \quad (\text{A.16})$$

where N is the amount of turns, I the current and l_e magnetic length. With the corresponding material data the magnetic flux density B can be evaluated. Then for each step in the input sine-wave and the actual current the on and off-timings can be calculated, which are then used in the iGSE. The average of this losses across a quarter sine wave are then the total core losses. DC bias losses are not accounted with the iGSE, but are also negligible [90].

A.2.2 Core loss for the transformer

The material for the transformer is ferrite and no specific BH-curve was available from the manufacturer. In the datasheets only a material loss curve for a certain B and f is available. Eq (A.17) shows how the flux density can be calculated with

$$\Delta B = \frac{U_{DC} D}{f \cdot N_P A_C}, \quad (\text{A.17})$$

where D is the duty cycle, U_{DC} is the DC-link voltage which is approximate also the voltage across the transformer primary (neglecting the voltage drops across the MOSFETs), N_P are the number of primary turns and A_C is the cross-sectional area of the core. Any DC bias is again neglected, although here ferrite is the core material. Due to the blocking capacitor in series with the transformer a DC bias should not be the case.

A.2.3 Core loss of the output filter

The core loss calculation for the output filter is similar to the core loss calculation of the boost inductor of the PFC. Again the iGSE was used for the calculation. Due to the voltage ringing of the synchronous rectifier switches the current through the output filter was taken from simulation.

A.3 Copper and eddy current losses

If a high frequency current flows through a conductor with a large diameter additional losses to the DC copper losses, called eddy current losses, can be investigated. There are two causes for the eddy currents, the skin effect and the proximity effect.

Skin effect: An AC current in a conductor causes an AC magnetic field on the inside and outside of the conductor, inducing electrical fields inside of the conductor and therefore eddy currents, which reduce the current density on the inside of an inductor can flow. The higher the frequency the thinner the skin-depth and the more eddy currents are on the inside. It can be easier visualized that the current is nearly only flowing on the outside of the conductor.

Proximity effect: If in the proximity of the outside AC magnetic field of one conductor is a second conductor, an electrical field is induced into the second conductor, causing eddy currents. The effective current through the second conductor is not changed due to this effect, the eddy currents in the second conductor are in sum zero.

Both of the above mentioned effects can be calculated analytically for 1-dimensional problems. A more detailed calculation would be possible with finite element methods, but this is also much more time consuming, especially if a lot of different core shapes have to be modelled.

For DC current the resistance of the conductor can be calculated with eq. (A.18)

$$R_{DC} = \rho \frac{l}{A}, \quad (\text{A.18})$$

where l is the length of the conductor, ρ is the material specific resistance and A is the area of the conductor. For an arbitrary periodic current waveform and a conductor with the optimal area eq. (A.19) is valid, [94].

$$\left(\frac{R_{AC}}{R_{DC}}\right)_{\text{opt}} = \frac{4}{3}. \quad (\text{A.19})$$

The calculation of the skin and proximity effect losses are geometry dependent. In the calculation and construction, both solid round conductors, foil conductors and litz wires

were used. The AC losses in the litz wire were neglected in the calculation. Therefore in the following sections a 1-dimensional analytical solution for the skin and proximity effect loss for round and foil conductors is presented. It must be mentioned that these following analytical solutions are only valid for sinusoidal currents. In the simulation the DC resistances obtained from eq. (A.18) were used. Later the DC and AC losses were calculated with the simulated currents obtained from the simulation for every load point. With a FFT analysis the currents were separated in their frequency components and for each frequency component the AC losses were individually calculated. The increased losses can be described with a factor f_x , which describes how much higher the AC resistance due to for example the skin effect is, compared to just the DC resistance of the conductor.

A.3.1 Skin effect

The skin effect can be derived for a round conductor with amperes law, see eq. (A.20).

$$\oint \vec{H} d\vec{l} = \int \int J_z d\vec{A}. \quad (\text{A.20})$$

This results in a to the time varying current I proportional time varying magnetic field \vec{H} and therefore also a time varying magnetic flux \vec{B} with $\vec{B} = \mu_0 \mu_r \vec{H}$. Using Faraday's law from eq. (A.21) results in an electric field \vec{E} along the conductor around the integrated area and with Ohm's law $\vec{j} = \sigma \vec{E}$ can be shown that a current is therefore also flowing. On the inside of the conductor the current is flowing against the effective current in the conductor, reducing the effective current, and on the outside of the inductor the current is flowing with the effective current, increasing the effective current on the outside of the conductor or also at the skin. Therefore originates also the name skin effect.

$$\oint \vec{E} d\vec{l} = -\frac{d}{dt} \int \int \vec{B} d\vec{A}. \quad (\text{A.21})$$

For higher frequencies the current on the inside gets more and more reduced and the current density gets higher on the outside of the inductor. In [95] is also shown, that for a 2 mm round conductor for 100 kHz nearly no current is anymore flowing in the radius of 1 mm from the center of the conductor. The skin depth δ describes the distance, where the current has only $1/e$ of the peak value, and it can be calculated with eq. (A.22)

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}}, \quad (\text{A.22})$$

where δ is the conductivity of the conductor and μ_0 is the permeability of free space. The effective smaller area for the current results in a higher resistivity compared to the resistivity for DC current. [95]

Foil conductors: The skin effect is described with the factor F_{Sf} . The frequency components of the current were calculated an FFT analysis and the loss components were then calculated for each frequency with eq. (A.23)

$$F_{Sf} = \frac{R_{skin}}{R_{DC}} = \left(\frac{h}{\delta}\right) \left(\frac{\sinh(\frac{2h}{\delta}) + \sin(\frac{2h}{\delta})}{\cosh(\frac{2h}{\delta}) - \cos(\frac{2h}{\delta})}\right), \quad (A.23)$$

where h is the foil thickness, f the frequency, μ_0 the free space permeability and σ the electric conductivity of copper. [96]

Round conductors: For round conductors the Kelvin functions can be used to calculate the increased skin effect losses, see eq. (A.24).

$$F_{Sr} = \frac{R_{skin}}{R_{DC}} = \frac{d}{2\delta\sqrt{2}} \frac{K_{ber}(0, \xi)K'_{bei}(0, \xi) - K_{bei}(0, \xi)K'_{ber}(0, \xi)}{K'_{ber}(0, \xi)^2 + K'_{bei}(0, \xi)^2}, \quad (A.24)$$

with

$$\xi = \frac{d}{\sqrt{2}\delta}. \quad (A.25)$$

K_{ber} and K_{bei} are the Kelvin functions of the first kind for the order zero or two (first index). K'_{ber} and K'_{bei} are the derivatives of the original Kelvin functions. These equations are only valid for sinusoidal currents. To calculate the losses for non-sinusoidal currents a Fourier-transformation of the current waveform is needed. For each frequency component of the Fourier-transformation the skin and proximity effect losses are calculated and the sum is taken to obtain the total losses. [95, 97]

A.3.2 Proximity effect

The outer magnetic field of one conductor induces into the second conductor a magnetic field, which also results in electrical fields, which again can be calculated with Faraday's law. In case of two close conductors, the current induced from the first conductor into the second conductor has on the side of the second conductor, which is close to the first conductor, a current in the opposite direction of the current in the first conductor. The current in the far side of the second conductor flows in the same direction as the current through the first conductor. Due to eddy currents in the second conductor the magnetic field in the first conductor is changing and more power is needed to drive the same current through the first conductor.

Foil conductors: The proximity effect can be calculated for each layer individually and each additional layer increases the proximity effect. For the first layer the proximity effect

is assumed to be zero. For the second layer and second winding of the transformer the proximity effect was calculated with eq. (A.26)

$$F_{\text{Pf}} = \frac{R_{\text{prox}(n)}}{R_{\text{DC}}} = 2n(n-1)\left(\frac{h}{\delta}\right)\left(\frac{\sinh\left(\frac{h}{\delta}\right) - \sin\left(\frac{h}{\delta}\right)}{\cosh\left(\frac{h}{\delta}\right) + \cos\left(\frac{2h}{\delta}\right)}\right), \quad (\text{A.26})$$

where n is the layer, for which the proximity effect is calculated. [95, 96]

Round conductors: For the proximity effect the distance between the conductors (interwire distance ν) and the distance to the next layer (interlayer distance h) has as well to be considered, [98]. Since d/δ is in this case very big the Ferreira or Dowell methods show inaccuracies. The filter inductor consists only of one layer, therefore the interlayer distance h/d was used with the maximum distance available from the table published in [98]. Eq. (A.27) with the curve fitting coefficients from the FEM calculation was used to calculate additional losses caused by the proximity effect afterwards.

$$F_{\text{Pr}} = (1 - \omega)k_1 \sqrt{(k_2)} \frac{d}{\delta} \frac{\sinh(\sqrt{k_2} \frac{d}{\delta}) - \sin(\sqrt{k_2} \frac{d}{\delta})}{\cosh(\sqrt{k_2} \frac{d}{\delta}) + \cos(\sqrt{k_2} \frac{d}{\delta})} + \omega \hat{d}\left(\frac{d}{\delta}\right). \quad (\text{A.27})$$

with

$$\hat{d}\left(\frac{d}{\delta}\right) = \frac{K \cdot \frac{d}{\delta}}{\left(\left(\frac{d}{\delta}\right)^{-3n} + b^{3n}\right)^{\frac{1}{n}}}, \quad (\text{A.28})$$

where K is a constant of 0.096 and n , ω , k_1 , k_2 are interpolated from the curve fitting coefficients given in [98].

A.3.3 Eddy current reduction

To reduce eddy currents in conductors and therefore the overall power loss solutions for the PCB layout and also for the inductor and transformer cores exist. One solution is to use optimized wire diameters, where the sum of skin and proximity effect are lowest for the conductors. Another possible solution is the utilization of many thin and isolated conductors, also called litz-wire. This does not help if the isolated conductors are just parallel to each other, since then the proximity effect is again increasing the losses. If they are twisted the induced voltages cancel each other reducing or even canceling the eddy currents. For hundreds of isolated conductors it is therefore important that every conductor was at every possible position after a length of twist. To minimize the proximity effect as well as parasitic inductivities in the layout, it is recommended to reduce the current loops, which means that the forward path of the conductor should be as close as possible to the return path.

A.4 Capacitor losses

In the capacitor several loss sources exist, like the leakage current, the series resistance and also at higher frequencies inductive losses. The equivalent schematic for a capacitor with the parasitic elements is shown in Fig. A.10.

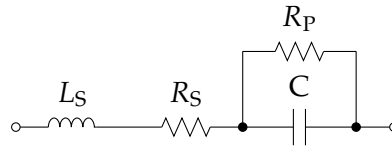


Figure A.10: Equivalent circuit for a capacitor with parasitics.

Leakage current: Especially electrolytic capacitors have a relatively high leakage current compared with other technologies, like foil or ceramic capacitors. Often for different technologies with lower leakage current a insulation resistance is given in the datasheet, which is basically the same as a definition of the leakage current. In Fig. A.10 the leakage current or insulation resistor can be represented with the resistor R_P parallel to the main capacitor C , constantly discharging the ideal capacitor. For electrolytic capacitors the leakage current is not constant, it depends a lot on the temperature and as well on the time the voltage has been applied to the capacitor. Increased temperature also leads to an increased leakage current. According to industrial standards, the leakage current is the current which is measured after 5 minutes of applying the rated DC voltage to the capacitor. Due to the self healing effects of electrolytic capacitors the leakage current decreases exponentially over time. For the leakage current various descriptions exist and they usually depend on the manufacturer, usually the equation is similar to eq. (A.29)

$$I_L = K_c \cdot C \cdot V, \quad (\text{A.29})$$

which gives the leakage current I_L in μA , K_c is a constant from the datasheet (usually between 0.01 and 0.02 for electrolytic capacitors), V the rated voltage and C the capacity in μF . With this formula the maximum leakage current after 5 minutes was calculated.

Series Resistance: The ESR R_S is frequency dependent. Usually the ESR is calculated for a certain frequency with the dissipation factor DF or also loss angle $\tan(\delta)$, see eq. (A.30),

$$ESR = \frac{DF}{2\pi f C}, \quad (\text{A.30})$$

where DF is the dissipation factor from the datasheet, f the frequency and C the capacity of the capacitor. The ESR over the frequency is shown in Fig. A.13, where it is shown that the ESR gets smaller for higher frequencies. The impedance decreases at first due to the capacitor ($\frac{1}{\omega C}$) but at a certain frequency the impedance increases due to the parasitic inductance L_S (ωL).

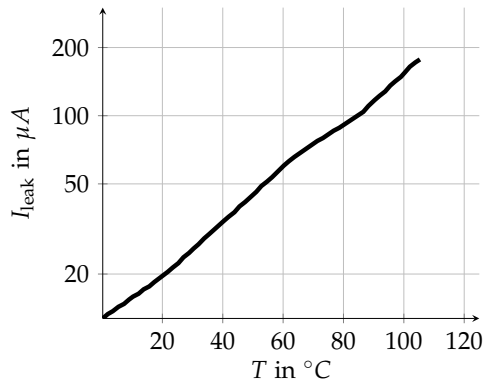


Figure A.11: Leakage current over temperature for a $470 \mu F$, $200 V$ capacitor, [99].

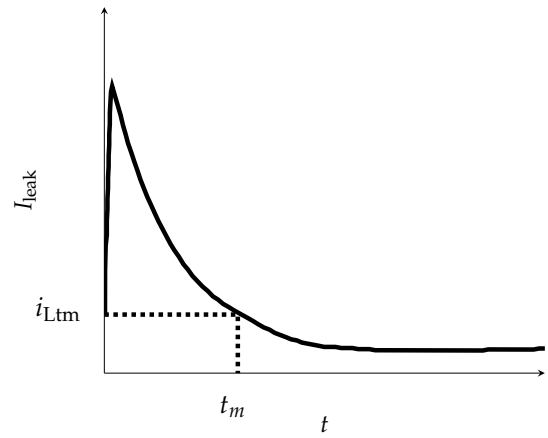


Figure A.12: Typical leakage current over time, [100].

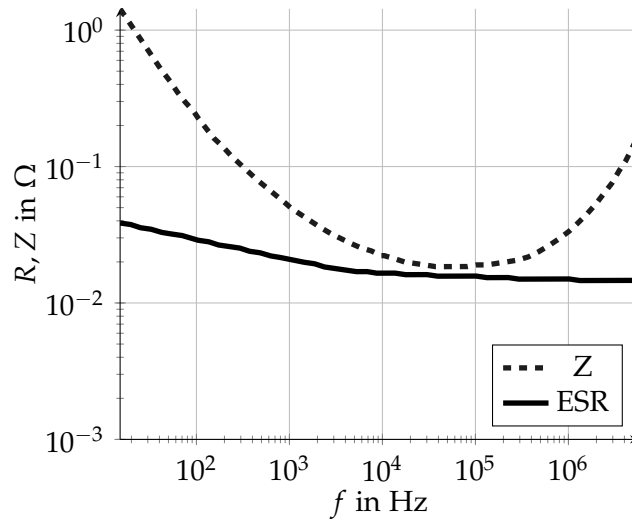


Figure A.13: ESR and impedance of a capacitor over the frequency for $25 ^\circ C$, [99].

Glossary

Glossary

BCM Boundary Conduction Mode. 34, 38, 39

BHFFOM Baliga High Frequency Figure of Merit. 20

CCM Continuous Conduction Mode. 4, 34, 38

CM Common Mode. 38

DCM Discontinuous Conduction Mode. 34

DUT Device Under Test. 31

EMI Electromagnetic Interference. 3, 7, 25, 29–32, 67, 120

ESR Equivalent Series Resistance. 58, 61, 136

FHA First Harmonic Approximation. 46

FOM Figure of Merits. IV, 3, 5, 8, 15, 20, 21, 24, 48, 51, 95, 117, 120

FPGA Field Programmable Gate Array. 51, 65, 68, 70–73, 80, 89, 102

GaN Gallium Nitride. 4–6, 38, 39, 119

IGBT Insulated Gate Bipolar Transistor. 12

iGSE improved Generalized Steinmetz Equation. 127–130

IPOP Input Parallel Output Parallel. 109, 111

IPOS Input Parallel Output Serial. 109, 111

ISOP Input Serial Output Parallel. 109, 111, 112, 120

ISOS Input Serial Output Serial. 109, 111, 112

LISN Line Impedance Stabilization Network. 31

- LUT** Look Up Table. 57, 89
- MCT** MOS controlled thyristor. 12
- MLCC** Multi Layer Ceramic Capacitor. 61, 77
- MPP** Molypermalloy Powder. 60, 77, 94, 98, 129
- NHFFOM** New High Frequency Figure of Merit. 21
- NRDC** Natural Resources Defense Council. 1
- PFC** Power Factor Correction. IV, 4, 7, 26, 27, 32–34, 36, 39, 40, 46, 48, 49, 51–53, 56, 58, 65, 67, 69, 70, 76–78, 80, 94, 101, 109, 114, 115, 117, 119, 120, 129, 130
- PiN-diode** Positive intrinsic Negative diode. 9–11, 36
- PS-ZVS** Phase Shifted Zero Voltage Switched. IV, 5–7, 43–45, 47–49, 51, 72, 80, 82, 83, 85, 86, 90, 93, 94, 98, 105, 107, 108, 111, 112, 114, 115, 118, 119
- PWM** Pulse Width Modulation. 65
- SiC** Silicon Carbide. 4, 11, 36, 38, 119
- SMPS** Switched Mode Power Supply. IV, 1, 4–8, 24–26, 40, 51, 117–120
- SOA** Safe Operating Area. 30
- SPI** Serial Peripheral Interface. 114
- TCM** Triangular Current Mode. IV, VII, 4, 38, 39, 46, 48, 49, 51, 65, 120
- THD** Total Harmonic Distortion. 33, 34
- ZCD** Zero Current Detection. 71–73, 75, 77
- ZVS** zero voltage switching. 52

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