Low Noise High Speed Analog Video Frontends for PC and HDTV Applications in 90nm and 65nm.

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Abstract

The emphasis of this thesis is on practical design aspects for high definition video frontends in deep submicron. High definition video frontends require low noise high speed pre-processing and analog to digital converter (ADC) topologies. Video frontends contain input buffer, gain stages and filter blocks to get the appropriate signal for the ADC. Moreover pseudo differential inputs were used to improve the performance and to be insensitive to digital and analog crosstalk. The gain characteristics can be switched easily by adding one resistor to the gain stage. The filter can be tuned to get the optimum picture performance for HDTV, PC or standard TV signals. The best speed and power compromise was achieved by using a pipeline ADC with 1.5bit/stage resolution. By skipping the S&H amplifier power and area was saved. Furthermore nested cascoded Miller compensation reduces area and power of the amplifiers in the different ADC stages. A comparison with state of the art ADCs was done to show the achieved low area and power number. The pipeline ADC was the right choice to result in an attractive figure of merit of 0.5pJ per conversion step at a sample rate of 165MS/s and signal bandwidth of 85MHz. For this thesis three ADC and pre-processing test-chips and one productive complete analog video frontend in 90nm and 65nm technologies were developed.

Kurzfassung

Der Schwerpunkt dieser Doktorarbeit liegt im Bereich der Entwicklung von hochauflösenden Videoeingangsstufen in nm-Technologien. Hochauflösende Videoeingangsstufen erfordern Verarbeitungseinrichtungen und Analog-Digital Umsetzer mit niedrigem Rauschen und hoher Geschwindigkeit. Diese Videoeingangsstufen beinhalten einen Entkoppler, Verstärkerstufen und Filterblöcke, um das passende Signal für den Analog-Digital Umsetzer zu generieren. Darüber hinaus wurden pseudodifferentielle Eingänge, zur Verbesserung der Leistungsfähigkeit und um unempfindlich gegenüber digitalem und analogem Übersprechen zu werden, verwendet. Die Verstärkungscharakteristik kann sehr einfach durch das Hinzufügen eines Widerstandes in der Verstärkerstufe geändert werden. Durch Abstimmung der Filterstufe kann eine optimale Bildqualität für HDTV, PC oder Analog TV Signale erreicht werden. Der beste Geschwindigkeits- und Leistungskompromiss wurde durch einen Parallelverarbeitungs-Analog-Digital Umsetzer mit einer Auflösung von 1.5bit pro Stufe realisiert. Durch das Weglassen des Folge- und Halteverstärkers konnte Leistung und Fläche gespart werden. Darüber hinaus reduzierte die verschachtelte, kaskadierte Millerkompensation die Fläche und Leistung der einzelnen Verstärker in den verschiedenen Analog-Digital Umsetzerstufen. Es wurde ein Vergleich mit Analog-Digital Umsetzern, die dem Stand der Technik entsprechen, getätigt, um die erzielten niedrigen Flächen und Leistungswerte zu veranschaulichen. Der Parallelverarbeitungs-Analog-Digital Umsetzer war die richtige Wahl, um eine sehr attraktive Leistungszahl von 0.5pJ pro Wandlungsschritt bei einer Umsetzerrate von 165MS/s und einer Signalbandbreite von 85MHz zu erzielen. Für diese Arbeit wurden 3 Analog-Digital Umsetzer- und Videoeingangsstufen-Testchips und eine komplette analoge Videoeingangsstufe in 90nm und 65nm Technologie entwickelt.

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Abbreviations

AC	Alternating Current
ADC	Analog–to–Digital Converter
AFE	Analog Frontend
AGC	Automatic Gain Control
BW	Bandwidth
CJ	Junction Capacitance of a MOS Switch
CMOS	Complementary Metal–Oxide–Semiconductor
CRT-TV	Cathode Ray Tube Television
CVBS	Color Video Baseband Signal
DAC	Digital–to–Analog Converter
DC	Direct Current
DNL	Differential Nonlinearity
DSM	Deep Submicron
DVD	Digital Versatile Disc
EBU	European Broadcasting Union
ENOB	Effective Number of Bits

FOM	Figure Of Merit
GBW	Gain Bandwidth
HDTV	High Definition Television
IEEE	Institute of Electrical and Electronics Enigineers
INL	Integral Nonlinearity
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MDAC	Multiplying Digital–to–Analog Converter
MOM	Metal Oxide Metal
MSB	Most Significant Bit
MUX	Mulitplexer
NBTI	Negative Bias Temperature Instability
NTSC	National Television System Committee
OP-AMP	Operational Amplifyer
OTA	Operational Transconductance Amplifier
PAL	Phase Alternation Line
PSR	Power Supply Rejection
PSSR	Power Supply Rejection Ratio
RGB	Red Green Blue
Ron	On-Resistance

SAR	Successive Approximation Register
SCART	Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs
SD	Standard Definition
SECAM	Séquentiel Couleur à Mémoire
SFDR	Spurious Free Dynamic Range
SNDR	Signal–to–Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SOC	System on chip
STI	Shallow Trench Isolation
THD	Total Harmonic Distortion
UXGA	Ultra Extended Graphics Array
VGA	Video Graphics Array
VHS	Video Home System

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Chapter 1

Introduction

In this chapter the development of analog video frontends depending on the technology and specification will be discussed. Furthermore the effect of the technology on the design will be explained. For deep submicron (DSM) technologies these effects can influence the reliability. The human eye receives the video picture so the physiological context must be understood. Finally the outcome of this thesis will be summarized and an overview of the thesis will be given.

1.1 Motivation

In the last decades TV sets with tubes were used to display movies and news. The resolution of these systems was always very low. The bandwidth for a VHS (video home system) video system is limited to 3.5MHz which corresponds only 400 lines. As the flat-panel displays appeared the picture size can be manufactured in very large dimensions. Hence the standard TV signal eg. PAL with 576 lines is not really dedicated to be displayed on this large panels. Therefore the processing has to be adapted to extrapolate this standard resolution signals. Moreover the processing of high definition signals must be able.

This requires large bandwidth circuits which consumes power and area. The target is to find topologies which can be adapted very easily for different display modes. This means that the power consumption must be adapted depending on the resolution of the picture. Additionally the video front end has to be integrated on a system on chip environment. There the whole video processing is integrated where only this system on chip is necessary to control a flat-panel display. The power consumption of this chip is very large and must be handled very intelligent to avoid the destroying due to heat.

The backplate of the chip can be used for transferring the waste heat and to contact the digital ground. The digital processing has to be realized in deep sub-

micron (DSM) technologies to fullfill the digital bandwidth requirements. Hence the PSRR of the analog circuits must be very large to minimize the influence of the digital crosstalk.

1.2 HDTV and Analog Video Processing

The development from the CRT-TV to Flat Panel displays required an adaption of the video signal processing. The resolution and bandwidth of video signals increased. So it is necessary to develop video frontends with 10 bit resolution and a sample rate up to 165MS/s to fulfill these tough requirements. HDTV pictures have a maximum static resolution of 1920*1080 pixels. Moreover the vertical resolution of an HDTV signal depends on the scanning of the image. For better motion portrayal the EBU Technical Committee recommends the emission of 1080 and 720 progressive scanned images. Therefore analog video frontends with a bandwidth of more then 200 MHz are necessary. The analog input signals consist of the alignment of voltage steps, where each step equals one pixel. A standard video frontend is shown in figure 1.1.

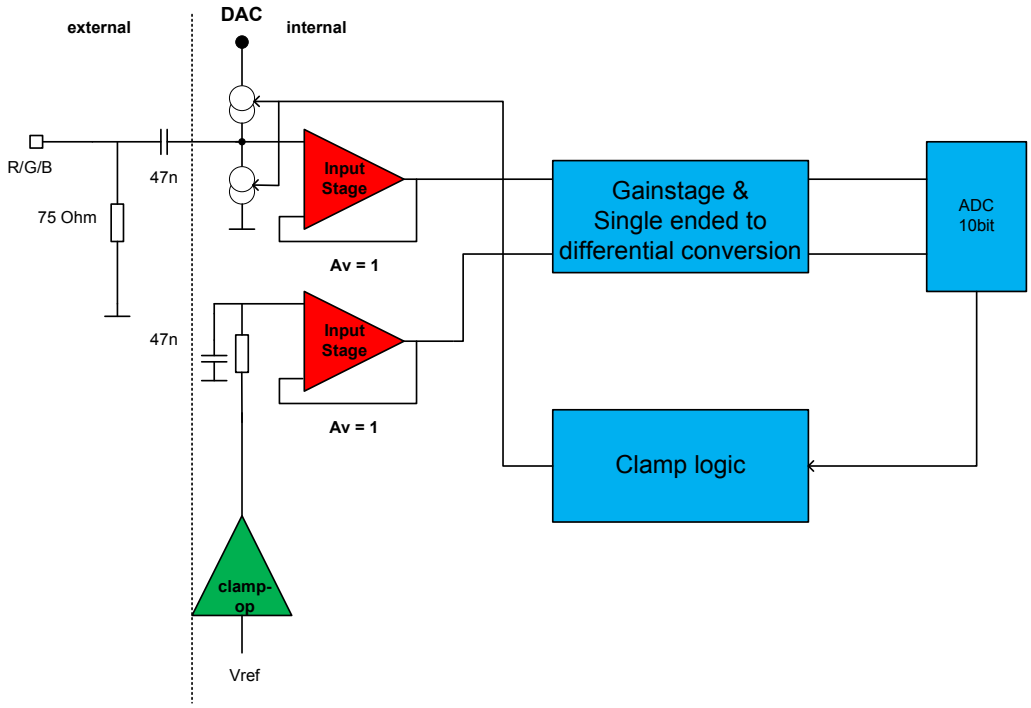

Figure 1.1: Principle Analog Video Frontend

The challenges of analog video processing are low noise, high bandwidth, low power and area. This can be handled by the right technology and topology.

1.3 Analog Video Frontends (SOC)

Analog Video frontends were realized at the beginning of the year 2000 in 180nm technologies with resolutions of 8 and 9bit for 100Hz CRT-TVs. 4 channels were used to convert standard analog video signals to the digital domain. The power consumption was about 144mW at 1.8V and the area about 0.4mm^2 for a 9bit system with a clock frequency of 40.5MHz. This ends up with a 10bit frontend with 74.5mW at 1.1V and an area of 0.175mm^2 in a 65nm technology with a clock frequency of 165MHz . The bound from 180nm to 65nm was very large regarding supply voltage and leakage current. Moreover the hot carrier effect, NBTI (negative bias temperature instability)[1], STI (shallow trench isolation)stress [2] and well proximity effect have to be considered in more detail.

Table 1.1: Analog video frontend power depending on technology

Technology / Power	180nm (mW)	130nm (mW)	90nm (mW)	65nm (mW)
Pre-processing	62	55	47.4	41
ADC	82	43	56	33
Channel	144	98	103	74

Figure 1.2 illustrates the reduction of power due to new topologies and decrease of the minimum channel length. The power is reduced by 60% which is reached by the very large transit frequencies of the MOS transistors. Otherwise the gm*rout is smaller which represents the gain of a single stage amplifier and the channel length modulation is larger. That´s why cascode structures are used to increase the gain. The thermal noise gets larger and can be reduced by increasing the current. The supply voltage is also decreased by 60% where the signal to noise ratio(SNR) decreases automatically by 4dB. Nevertheless the power reduction at same or better SNR was achieved by using the pipeline ADC architecture instead of a two step flash ADC. The pipeline ADC uses the increase of the transit frequency of the technology scaling.

The device matching is better but reduced due to a larger square resistance of the non silicided resistor. Due to the smaller transistor dimensions the W,L

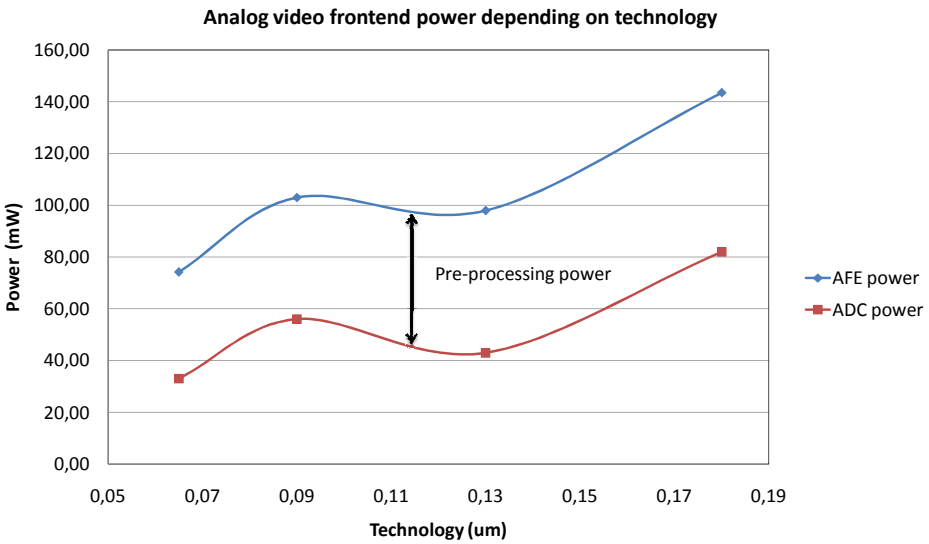

Figure 1.2: Analog video frontend power depending on technology

matching of a MOS transistor [3] gets lower which introduces a larger offset. This can be handled by the clamping loop in the frontend. A further drawback of the low supply voltage is the increased crosstalk from noisy digital logic gates at shared substrates. The red curve shows the power consumption of the ADC where the difference between the red and the blue curve corresponds to the power consumption of the pre-processing plus ADC. The power consumption is reduced from 62mW to 41mW for a calibrated filter bandwidth of 15MHz to 76MHz. Most of the power reduction was achieved by the pipeline 1.5bit per stage architecture.

Table 1.2: Analog video frontend area depending on technology

Technology / Area	180nm (mm^2)	130nm (mm^2)	90nm (mm^2)	65nm (mm^2)
Pre-processing	0.1	0.08	0.059	0.05
ADC	0.3	0.4	0.15	0.125
Channel	0.4	0.48	0.209	0.175

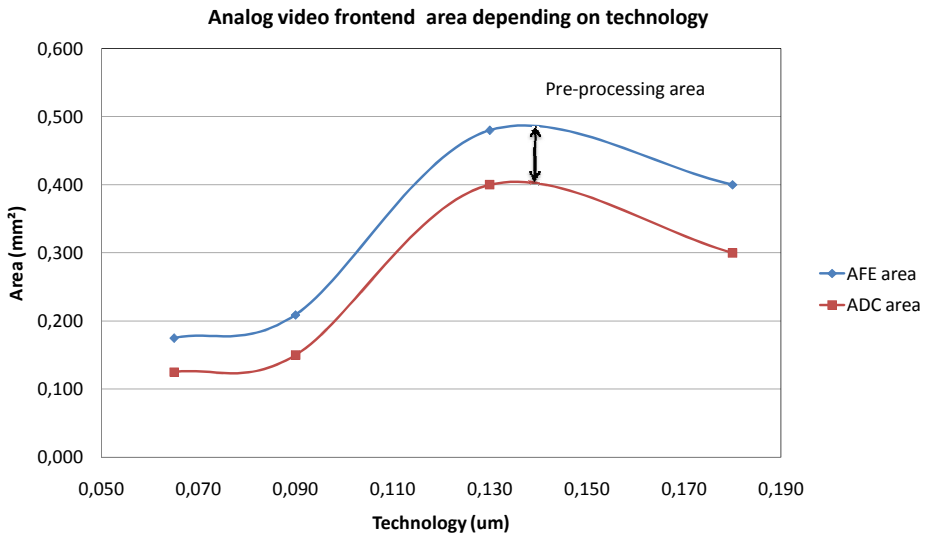

Figure 1.3: Analog video frontend area depending on technology

Figure 1.3 demonstrates the area reduction depending on the technology for the pre-processing plus ADC (blue curve)and the ADC (red curve). The area of the pre-processing was reduced by 50% by skipping one filter stage. Due to the noise requirement for 10bit resolution the resistors are chosen small, where the limitation is the LSB capacitor of the filter array. The 0.13u ADC area is increased by 0.1mm^2 because of the larger sample frequency of 130MHz. It was the first HDTV ADC. The two step flash ADC topology needs larger capacitor arrays compared to the pipeline ADC.

1.4 Process Option

Two deep submicron processes are used to develop this kind of high definition frontends. Special care on the reliability of these processes has to be taken to ensure a life time of more than 10 years. The oxide thickness of the core transistors are in the range of 16 angstrom which corresponds to 16 atom layers. This causes large gate tunneling current except at high temperatures which has to be considered in the design. A new material for silicide formation was used which results in larger resistance of silicided regions. 7 metal layers were used in 65nm to have more opportunities for power routing. Moreover MOM (Metal oxide Metal) capacitors were taken.

1.4.1 NBTI

PMOS threshold instability under negative gate bias could shift 2.5V PMOS threshold voltage up to 150mV in case of a gate overdrive of 3.47V. Even at lower gate voltages the threshold voltage shift can be expected in the range of 20mV. Hence all matched pairs must have the same gate source voltage.

1.4.2 Gate and Drain Overdrive

A gate overdrive of 1.2V is acceptable but the gate tunneling current can be very large. A drain overdrive of 1.3V still causes moderate degradation of e.g. Idsat by 10% after 10 years. Bootstrapping of NMOS core transistors is allowed as long the voltage across the gate oxide (Vgs,Vgd) and Vds are limited to the maximum allowed supply voltage. Gate overdrive of 2.5V I/O transistors to 3.3V is acceptable but the gate area must be below $3mm^2$. This was considered at the 3.3V input stage.

1.4.3 Well Proximity Effect

The well proximity effect is based on the distance to the N-well and causes a threshold shift of more than 150mV depending on the gate oxide thickness. It is recommended to let 1μm space from any point of the gate area to the well. With 1μm spacing the well proximity effect influences the threshold at most with 10mV. Averaging over the total helps to decrease this effect.

1.4.4 STI Stress

This effect influences also the threshold voltage and drain current of the MOS transistors. Hence the transistors should build up out of active area and gate fingers. It is recommended to extend the source/drain diffusion length of single transistors to 0.5μm.

1.4.5 Hot Carrier Stress

If the maximum drain source voltage is applied to a transistor and a large current is flowing at the same time through this transistor, the life time will be reduced. Therefore stacking of transistors could be necessary.

1.5 Simulation Environment

The Cadence schematic entry was used where the Cosmos Scope displays the simulation results. The overall simulations of the 90nm analog video frontend were performed with hspice and nanosim. The mathematical calculations were

done with matlab and mathcad. The bsim 4 model was employed by the simulator to include STI, NBTI and well proximity.

1.6 Visual Perception and Weber - Fechner's Law

The understanding of human visual perception and the optical properties of the human eye is necessary to develop image processing applications. Also the signal processing of the retina and the pattern recognition properties of the visual cortex must be considered. Generally it can be said that the human eye is the most important information receiver for mankind. It can receive 10 times more information than the ear. The levels of the visual processing are:

- Human optical system.
- Amplitude characteristics determined by the receptor cell.
- Spatio-temporal characteristics determined by the optical system and the retina processing.
- Higher level characteristics like pattern recognition in the visual cortex.

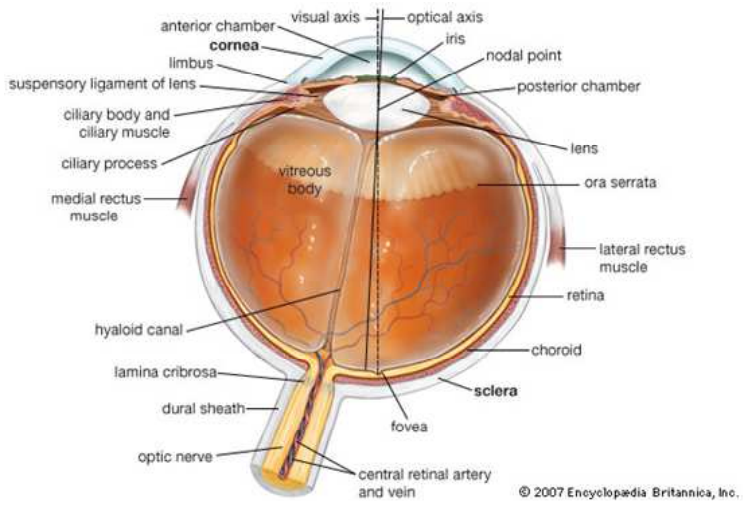

Figure 1.4: Horizontal cross section of the human eye (taken from Encyclopædia Britannica)

Figure 1.4 illustrates the horizontal section of the human eye where the cornea, the anterior chamber, the iris and the pupil can be seen. The pupil changes

adaptively the diameter depending on the illuminance of the retina. The spatio-temporal processing is performed in the retina to reduce the information which is send to the visual cortex because of the temporal resolution of the system of about 10 to 20 pictures per second. The maximum sensitivity of the visual system is given by spatial changes of the pictures (contours, edges) and for temporal changes (motion). There are only 10^6 fibres in the optical nerve.

The human visual system forms an image of an object and reduces the amplitudes of higher spatial frequencies where a low pass characteristic is achieved. The perceived brightness difference dH is proportional to the relative luminance where L is the mean object luminance:

$$dH = k \cdot \frac{dL}{L} \tag{1.1}$$

Therefore it can be observed that the perceived brightness difference increases the lower the luminance itself is. Integration of 1.1 leads to the Webner-Fechner's law.

$$\int_{H0}^{Hmax} dH = k \cdot \int_{L0}^{Lmax} \frac{1}{L} \cdot dL \tag{1.2}$$

Hence a logarithmic characteristics can be observed.

$$Hmax - H0 = k \cdot ln\left(\frac{Lmax}{L0}\right) \tag{1.3}$$

This was considered in the pre-processing specially in the input stage where the linearity at large input values (brightness large) can be lower. Therefore power and area can be saved. Moreover the spatio behavior favor edges and contours which can be increased by the peaking and fast impulse response of the filter. Also the group delay should be constant which is fulfilled by a Bessel filter characteristics.

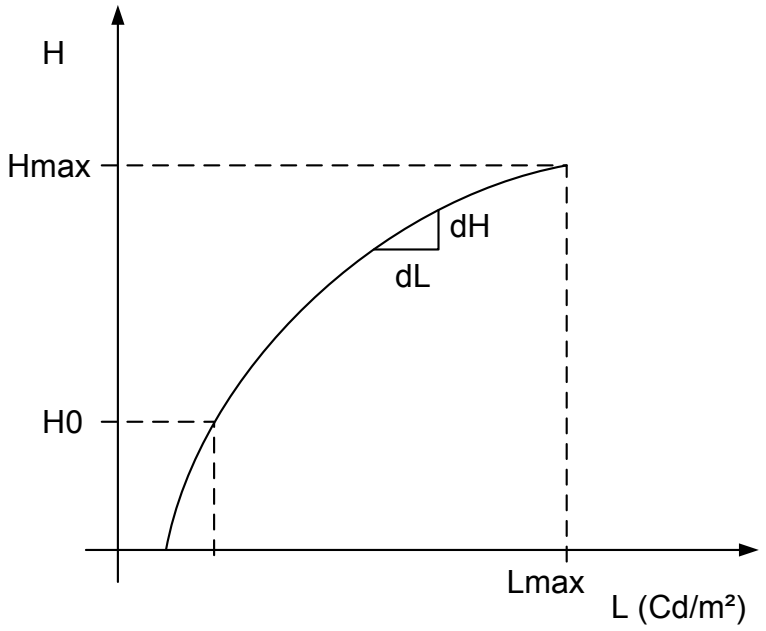

Figure 1.5: Weber-Fechner's law, perceived brightness depending on the luminance

1.7 Research Contribution

The issue was to develop a 90nm and 65nm analog video frontend for a SOC. The power and area was lower compared to the competitors. Therefore two 90nm test-chips and a 90nm productive 8 channel AFE were fabricated. The first testchip was done to verify the 40mW 200MHz 90nm analog pre-processing. The second was the 10bit 56mW 165MS/s 90nm pipeline ADC which can be used for high resolution and throughput. The 65nm test-shuttle contains the filter buffer of the 3^{rd} order Bessel filter and the 10bit 33mW 65nm pipeline ADC. Specific research contribution of this work include:

- Pseudo differential input structure [12].
- Two single ended input buffers which were used to drive the programmable gain amplifier [12].
- Implementation of an AGC with two gain characteristics which can be changed easily by adding one resistor [12].
- Investigation of different AGC topologies where the combination of filter and AGC provides a power efficient solution.

- Capacitive compensation technique of the combined 3^{rd} order Bessel filter and AGC.
- Design of low noise Miller op-amps with very high bandwidth of at most 3GHz where the corner of the technologies is reached.
- Usage of the existing Bessel filter for a bandwidth of 200MHz where parts of the capacitor array are used to get a pixel response with low overshoot comparable to the Bessel characteristic [12].
- A simple filter calibration technique by using two low-pass filter [10].
- Design of a 90nm pipeline ADC without dedicated sample and hold and single ended reference buffer loaded with a resistive divider [13].
- Special timing of the sub-ADC to increase speed and to save power.
- Optimization of the sampling network of the sub-ADC and the multiplying DAC to decrease the aperture error of the 65nm pipeline ADC [21].

1.8 Thesis Organisation

This thesis is divided into 7 chapters. The first chapter gives some introduction with motivation, development of video frontend at Micronas and structure of the thesis. Chapter 2 gives an overview of the different video signals, picture resolution and pipeline ADC basics. Different pre-processing topologies are discussed in chapter 3 where a 90nm and 65nm analog video channel is introduced . Chapter 4 deals with a 90nm pipeline ADC including architecture, basic building blocks and experimental results. In chapter 5 the simulation and testing results of a 65nm pipeline ADC are explained. Chapter 6 introduces an 8 channel analog video frontend fabricated in a 90nm process. The last chapter number 7 concludes the most important facts of this thesis and gives some future prospects.

Chapter 2

Basics

In this chapter the different types of video signals will be introduced and a typical PAL signal will be shown. Moreover the sampling process and aliasing will be explained. In addition to that the influence of the jitter on the analog to digital conversion will be investigated. At the end we take a look on the principle of the pipeline ADC and its error sources.

2.1 Video Signals and Resolutions

The video signal processing has a very long history. The first regular broadcast was started 1935 in Berlin. The frame rate was only 25 pictures per second which introduces flicker. Later the picture was split up in two fields and transmitted 50 times per second. Next different kind of broadcast standard systems like PAL (Phase alternation line), NTSC (National Televison System Committee), SECAM (Séquentiel couleur à mémoire) were developed. The picture quality was increased where the largest improvement was achieved by the start of the HDTV broadcast over satellite.

Table 2.1 shows a summary of the most important TV signal standards. The resolution increased by a factor of 6 which effected the picture quality dramatically. Also the quality of displaying motions was improved by using progressive broadcast of standard or high definition content. Progressive means that in Europe 50 pictures per second will be transmitted which gives more details for broadcasting of sport events. The sample rate of the converter must be adapted to the resolution of the pictures and corresponds to a maximum sample rate of 165MS/s for UXGA (Ultra eXtended Graphics Array with 1600 times 1200 pixels) signals of a graphics card adapter.

In the following figures the different input signal shapes are shown starting with a CVBS (composite video), RGB (Red Green Blue), YUV and the different types

Table 2.1: Different SDTV and HDTV video signals

Standard	Resolution	Pixels	Aspect Ratio	Sample rate (MS/s)
480p/i	720*480	345600	16:9/4:3	20
576p/i	720*576	414720	16:9/4:3	20
720p	1280*720	921600	16:9	80
1080p/i	720*576	2073600	16:9	147

of synchronization signals. The synchronization is normally performed by an extra ADC. The RGB signal is commonly used by VGA (Video Graphics Array)

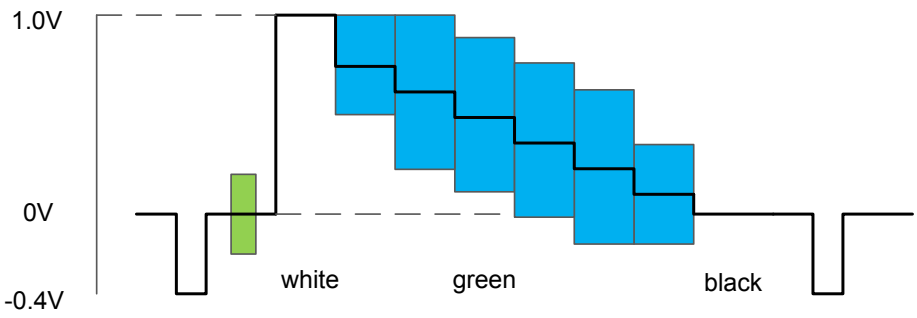

Figure 2.1: Composite signal with synchronization pulse and color burst

output with external synchronization signal. Also the SCART connection of a DVD player employs this signal form. The signal consists of voltage steps where the color and brightness depends on the levels of the three RGB signals. The voltage levels are around 1Vpp.

The YUV (YCrCb) signal corresponds to the differences of the luminance to the blue and red signal. In figure 2.3 the matrix for the conversion from RGB to YCrCb is shown. Usually the bandwidth of the color difference signal can be smaller.

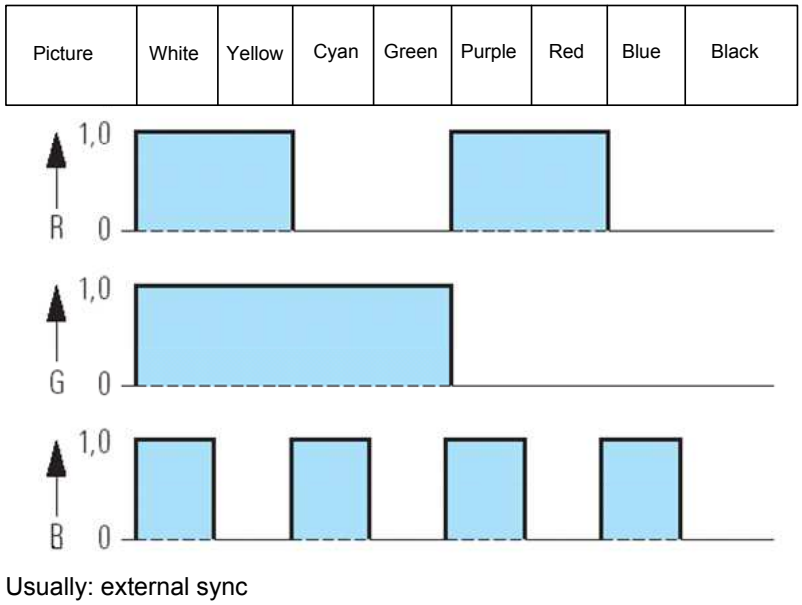

Figure 2.2: RGB signal with different color values

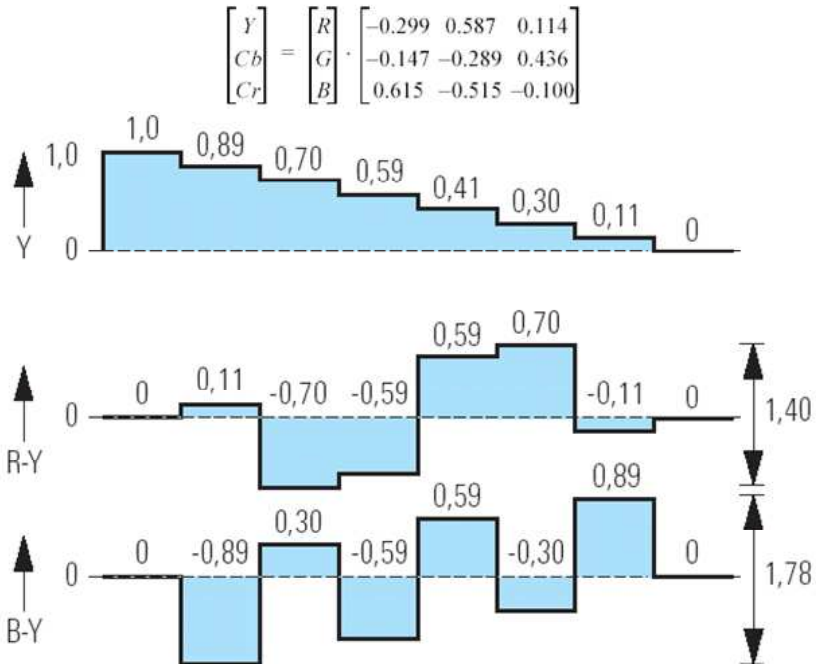

Figure 2.3: YUV signal with different color levels

Finally the various synchronization pulses are shown in figure 2.4 for VGA, PAL and HDTV.

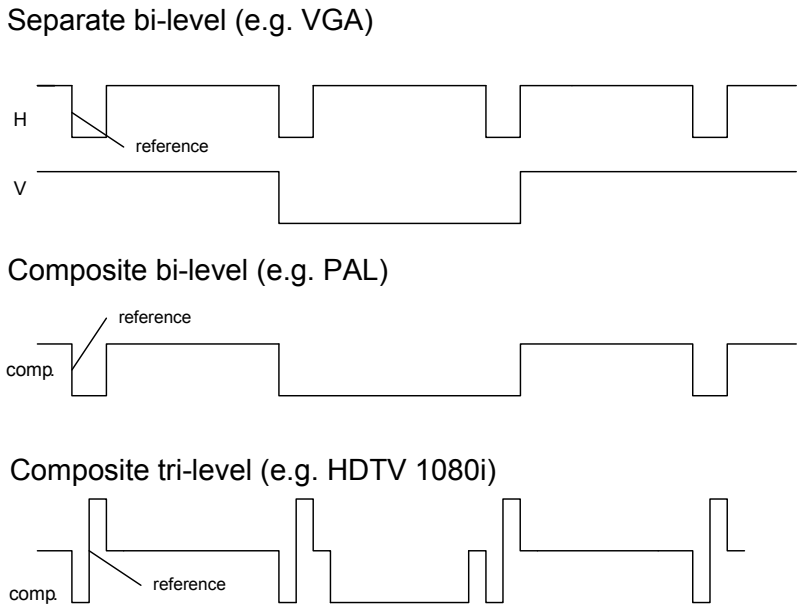

Figure 2.4: Synchronization depending on the TV system

2.2 Sampling and Quantization

Sampling and quantization are the basics for the analog to digital conversion which is a key function in modern systems. This is valid for each converter topology.

2.2.1 Sampling Function

The sampling function represents a sequence of equidistant Dirac impulses.

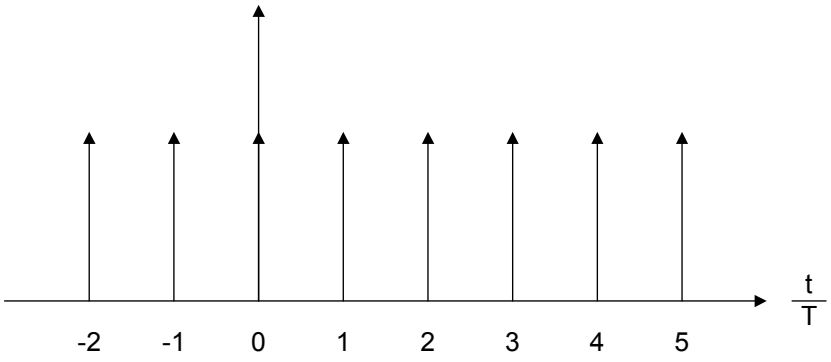

Figure 2.5: Sampling function

$$\triangle(t) = \sum_{n=-\infty}^{+\infty} \delta(t - n \cdot T) \tag{2.1}$$

The sampling function can be evaluated in the frequency domain, where a Fourier series expansion is performed. Hence the sampling function is interpreted by the sum of fundamental wave and harmonics. (fs = sampling frequency)

$$\triangle(t) = \sum_{n=-\infty}^{+\infty} Cn \cdot e^{j \cdot \omega s \cdot n \cdot t} \Longrightarrow t = \frac{2 \cdot \pi}{\omega s} \tag{2.2}$$

$$Cn = \frac{1}{T} \cdot \int_{-\frac{T}{2}}^{+\frac{T}{2}} \triangle(t) \cdot e^{-j \cdot \omega s \cdot n \cdot t} \cdot dt = \frac{1}{T} \cdot \int_{-0}^{+0} \delta(t) \cdot e^{0} \cdot dt = \frac{1}{T} \tag{2.3}$$

δ(t) is a Dirac pulse with infinitely short duration impulse and amplitude.

$$\triangle(t) = \frac{1}{T} \sum_{n=-\infty}^{+\infty} e^{j \cdot \omega s \cdot n \cdot t} \tag{2.4}$$

In equation 2.4 an infinite series of sine waves is shown. In the frequency domain it is given as:

$$\triangle(f) = \frac{1}{T} \sum_{n=-\infty}^{+\infty} \delta(f - n \cdot fs) \tag{2.5}$$

Next a transformation pair between time and frequency domain is obtained.

$$\triangle(t) = \sum_{n=-\infty}^{+\infty} \delta(t - n \cdot T) \Leftrightarrow \triangle(f) = \frac{1}{T} \sum_{n=-\infty}^{+\infty} \delta(f - n \cdot fs) \tag{2.6}$$

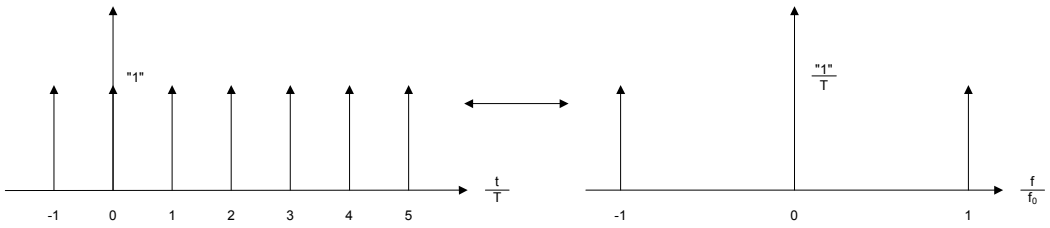

Figure 2.6: Transformation between time and frequency domain for the sampling function

Sampling means multiplication of the continuous time input signal x(t) with the sampling function $\triangle$(t). In time domain an impulse series is obtained which

is weighted by the input signal amplitude. A multiplication in time domain corresponds to a convolution in frequency domain, which results in a reproduction of X(f) at integer multiples of the sampling frequency. Therefore, a periodical spectrum is obtained illustrated in figure 2.7. In the frequency domain a convo-

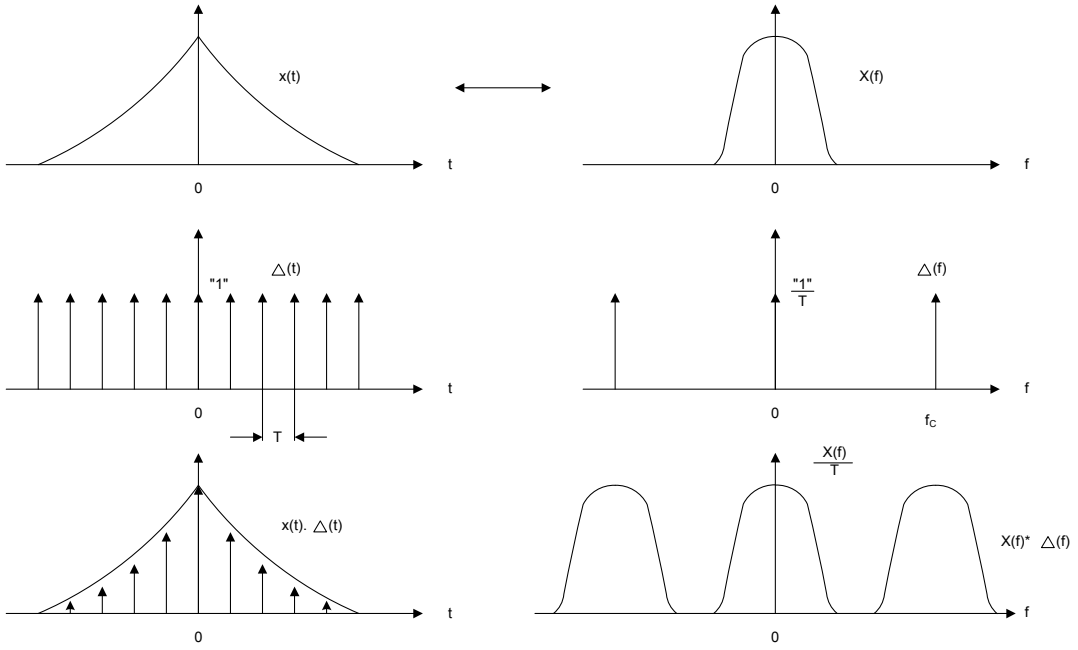

Figure 2.7: Sampling in time and frequency domain

lution of the analog signal spectrum and the spectrum of the sampling function is obtained. In equation 2.7 the sampling theorem is shown. If the bandwidth of X(f) increases then overlapping of the baseband and images occurs, which is called aliasing. Consequently, frequencies larger than the half sampling frequency must not present in the input signal, which can be realized by a low-pass filter.

$$X(f) * \triangle(f) = \frac{1}{T} \sum_{n=-\infty}^{+\infty} X\left(f - n \cdot fs\right) \tag{2.7}$$

2.2.2 Amplitude Quantization

The analog input samples are rounded to discrete values corresponding to a set of limited numbers, suitable for further digital modification. Although the quantization is non-linear, it can be approximated by a linear model. In many cases the rounding error is represented by a random signal, which is added to the ideal not quantized signal. The rounding error is assumed to be white and uncorrelated with the input signal. To meet these assumptions of the linear model, the input

signal must be "busy" and many quantization intervals must be occupied by the signal. In contrast, constant input signals result in non-zero correlation of the rounding error, and the white noise model is obviously not valid.
The noise signal has a constant probability density from -q/2 to +q/2. It is uncorrelated with the signal s(t) and has a wideband noise spectrum. From the

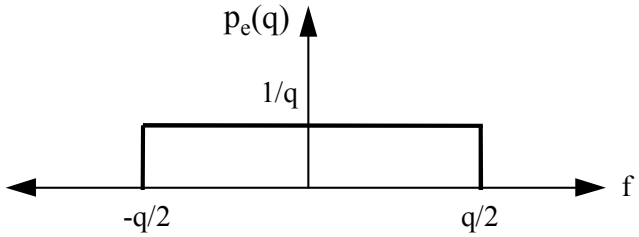

Figure 2.8: Equally distributed quantization noise

difference of the quantization noise power before quantization and after quantization the quantization noise power is obtained.

$$Pq = \frac{q^2}{12} \tag{2.8}$$

By sampling the power density spectrum the noise is concentrated to the range of 0 to fs/2. Consequently, the noise power is equally distributed shown in figure 2.9.

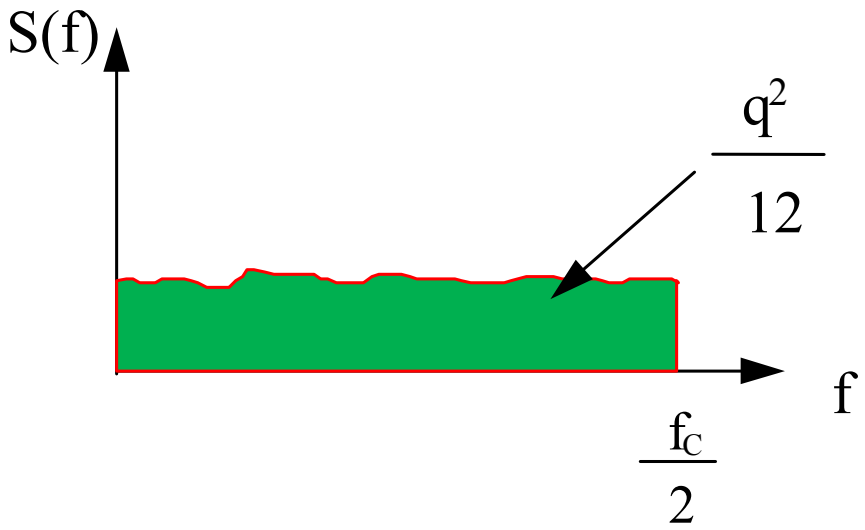

Figure 2.9: Noise density spectrum of the quantization noise

2.2.3 kT/C Noise

Every switch action contains resistive elements with thermal noise: This thermal noise is sampled on the capacitor each cycle. The overall noise power of the

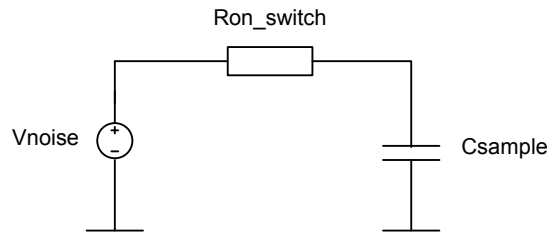

Figure 2.10: The equivalent circuit of a sample switch and capacitor

switch depends on the temperature, the Boltzmann constant k and the considered bandwidth.

$$Pnoise_{sw} = 4 \cdot k \cdot T \cdot R \cdot BW \tag{2.9}$$

For calculating the noise power of the sampling circuit the noise power of the resistor can be multiplied by the square of the low pass transfer function.

$$Pnoise = \int_{f=0}^{f=\infty} \frac{4 \cdot k \cdot T \cdot R \cdot \delta f}{1 + (2 \cdot \pi \cdot f)^2 \cdot R^2 \cdot C^2} = \frac{k \cdot T}{C} \tag{2.10}$$

2.3 SNR due to Jitter

The influence of the uncertainty of the sampling clock leads to a decreasing of the SNR. In figure 2.11 this uncertainty results in an error in the voltage amplitude du.

$$dt = \frac{dV}{SRmax} = \frac{2 \cdot Vinp}{Vinp \cdot 2 \cdot \pi \cdot f \cdot 2^{N+1}} = \frac{1}{\pi \cdot f \cdot 2^{N+1}} \tag{2.11}$$

If dt is an event from a Gaussian distributed jitter then equation 2.12 is valid. Moreover it can be seen that the signal amplitude doesn´t influence the signal to noise ratio.

$$SNR = \frac{\int (Vinp \cdot sin(\omega \cdot t))^2 \cdot dt}{\int \sigma_{dV}^2 dt} = \frac{1}{(\omega \cdot \sigma_{dt})^2} \tag{2.12}$$

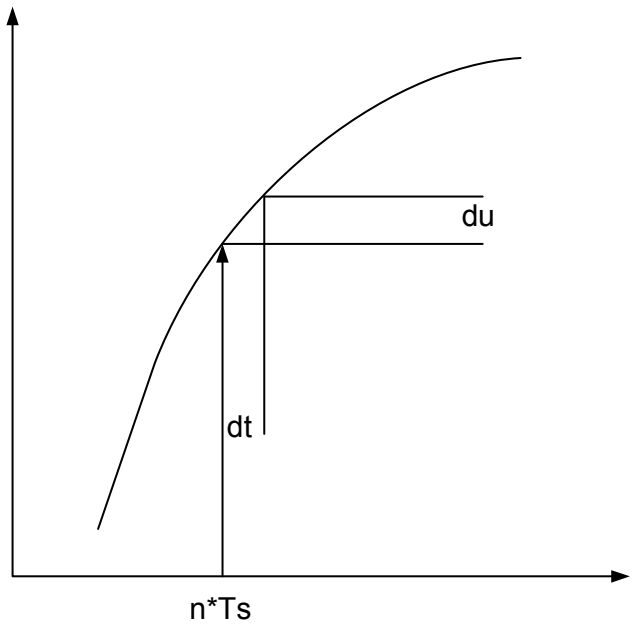

Figure 2.11: Jitter at the sampling process

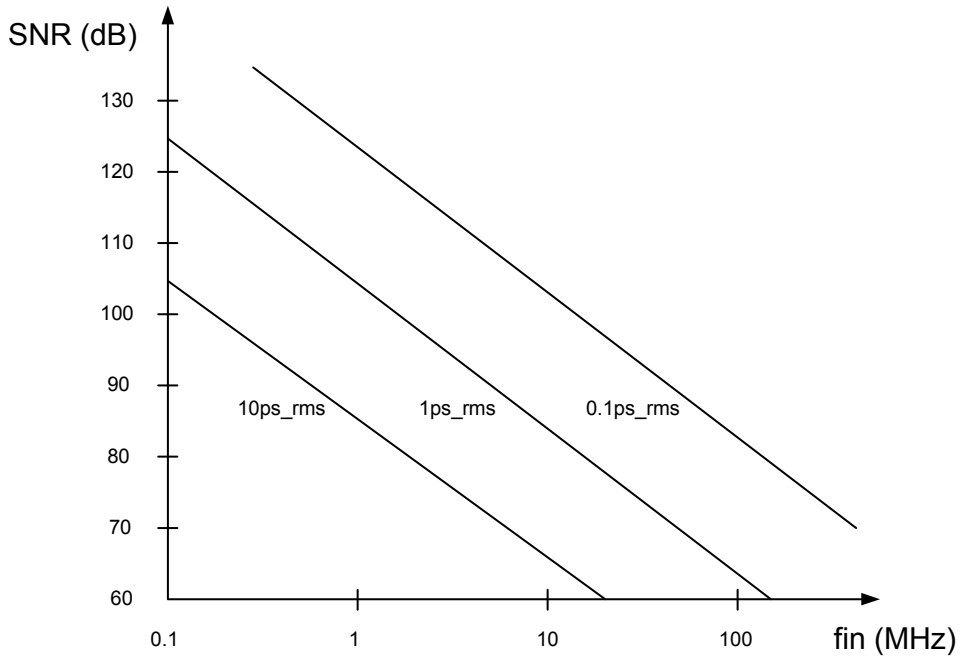

Figure 2.12: SNR due to jitter

2.4 Pipeline ADC and Error Sources

A pipeline ADC consists of similar ADC stages which are connected in a pipeline [4]. Each stage has a resolution of n-bit where a redundancy is used for error correction. The overall resolution of this ADC depends on the amount of stages and input reflected noise at the first stage. A maximum resolution of 16bit at medium sample rates like 100MS/s can be achieved by calibration. Figure 2.13 shows the principle topology of a pipeline stage. First the input is sampled and amplified by 2 for 1.5bit per stage architecture. The comparator which performs the analog to digital conversion can be connected in front or behind the sample and hold.

After the amplification the reference voltage must be subtracted or added depending on the result of the comparator. The analog output is led to the next pipeline stage where the same process is started again. Each stage works with the same sample rate. So the conversion speed is the same as for a Flash ADC but a delay is generated depending on the amount of pipeline stages. Compared to a two step Flash ADC the power consumption and the amount of comparators is smaller. Also from design point of view only one stage has to be developed and scaled for the following pipeline stages.

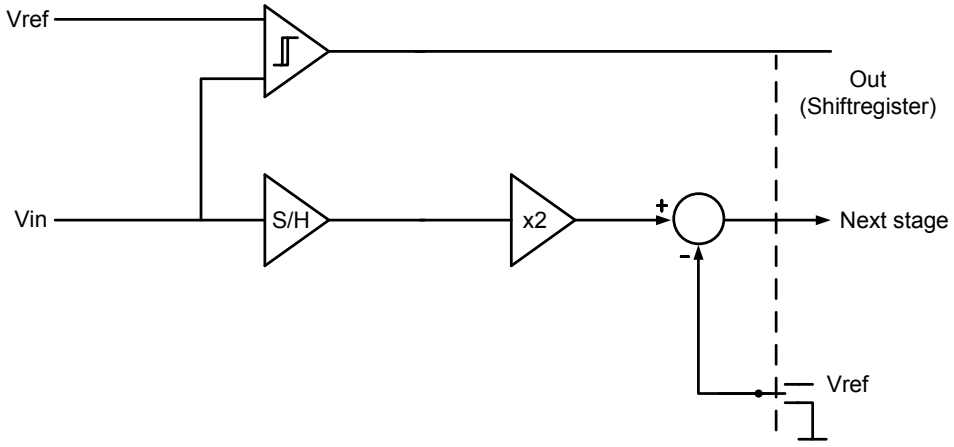

Figure 2.13: Pipeline ADC principle

The residue (analog output) of a 1 bit and 1.5bit stage is demonstrated in figure 2.14. The 1.5bit stage reduces the headroom by a factor of 2 for the output to use it for the correction of an error of the comparator. Therefore saturation of the multiplying DAC (MDAC) amplifier is avoided. The principle transfer function of the MDAC can be seen in equation 2.13 where D depends on the decision of the comparator and corresponds to -1, 0 or 1.

$$Vout = Vin \cdot 2 - D \cdot Vref \tag{2.13}$$

2.4.1 Offset in a Pipeline ADC

The maximum correctable offset Voff_{1st} of the first stage followed by an ideal stage corresponds to 1/8*vref. This can be explained by the comparator levels of +/- 0.25*vref of the second stage divided by 2. The maximum correctable offset of an N-bit ADC is calculated in equation 2.14. For a 10bit ADC this formula yields a maximum correctable offset of 0.25*vref. An increase of the bit count of the stages per one decreases the correction range by a factor of two. Figure 2.15 shows the residue of the first stage if the comparator performs a wrong decision.

$$Voff_{corr}(N) = \sum_{i=2}^{N} \frac{Voff_{1st}}{2^{i-2}} \tag{2.14}$$

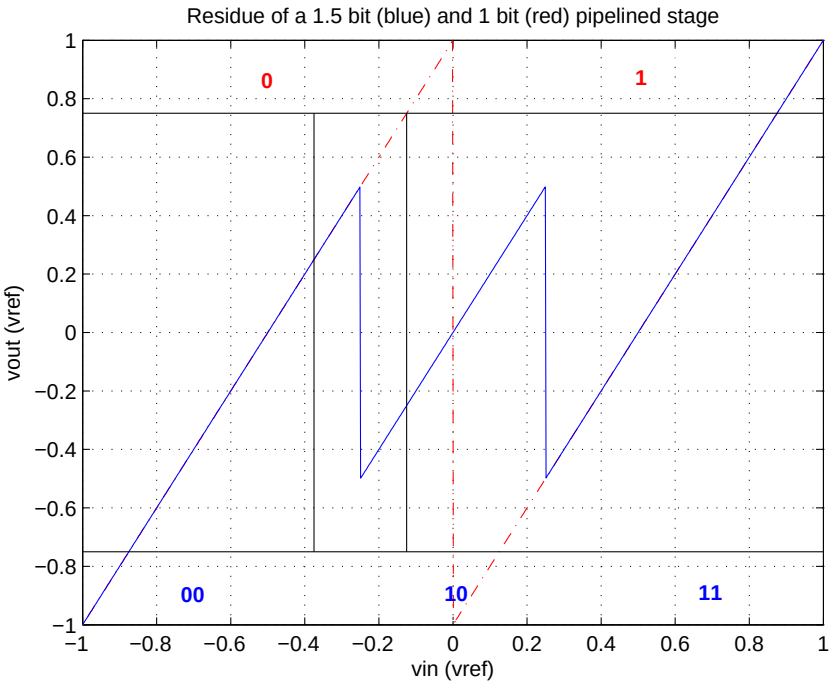

Figure 2.14: Residue of 1 bit and 1.5bit stage

2.4.2 DNL and INL

The DNL stands for the differential non-linearity (DNL)and corresponds to the deviation of the real to the ideal step width related on the ideal step width. For the evaluation of the ADC a ramp must be applied where the received characteristics are shown in figure 2.16. A DNL larger than 1LSB leads to a missing code which degrades the linearity very much.

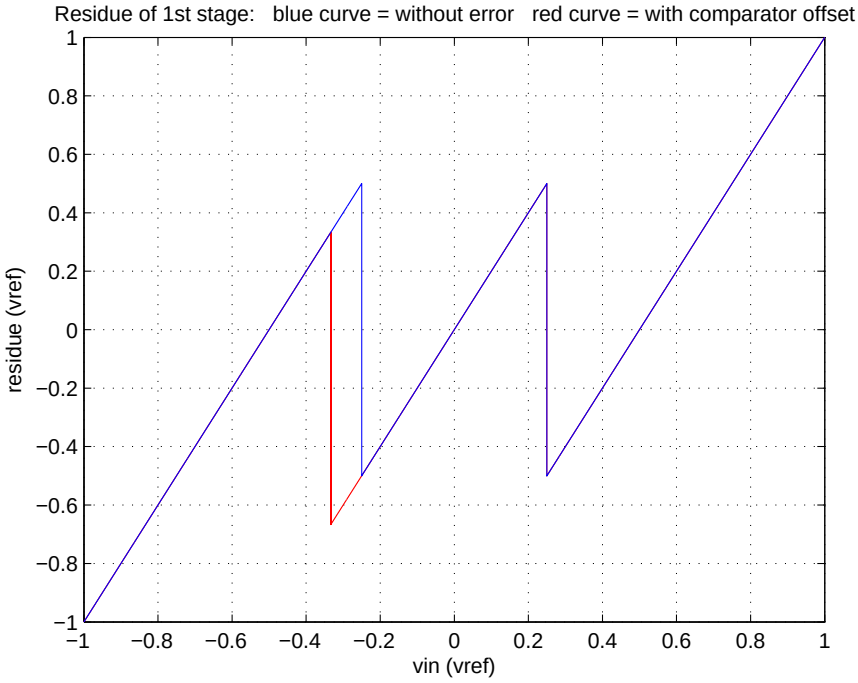

Figure 2.15: Residue of a 1.5bit stage with comparator offset

$$DNL_i = \frac{LSB_{real} - LSB_{ideal}}{LSB_{ideal}} \tag{2.15}$$

The integral non-linearity (INL) equals to the distance of the measured to ideal stepcurve related on the ideal step width. Additionally the INL is the integration of the DNL.

$$INL_i = \frac{x_{real} - x_{ideal}}{LSB_{ideal}} \tag{2.16}$$

In figure 2.16 the INL is demonstrated as the green difference of x_{real}-x_{ideal}. The difference can be calculated by measuring the center of each quantization step of the ideal and real step-curve.

2.4.3 Gain Error

The output voltage of a MDAC is calculated in 2.17 where the feedback capacitor of the inverting amplifier is C1. Figure 2.17 illustrates the bottom plate sampling process with a two phase non-overlapping clock signal where the input is disconnected after the sampling switch is opened. Hence the influence of clock

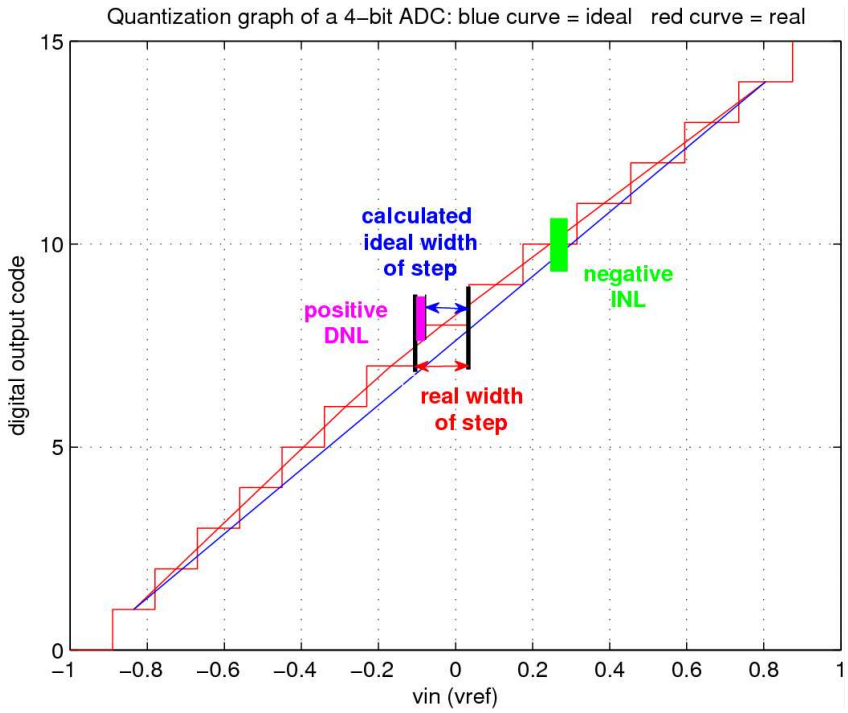

Figure 2.16: 4bit ADC characteristics with DNL and INL

feedthrough and charge redistribution of the input switch can be reduced. After sampling is finished the op-amp is used as inverting amplifier with gain one. There the charge from C2 is transferred to C1. Consequently the gain of two for the 1.5bit stage is realized. For a 2.5bit stage a gain of 4 will be get during amplification by one unity capacitor in the feedback and 3 at the input branch.

$$V_{out} = V_{in} \cdot \frac{C_1 + C_2}{C_1} - V_{ref} \cdot \frac{C_2}{C_1} \tag{2.17}$$

The gain error is caused by capacitor mismatch and low opamp gain. Due to a very large gain error the output of the first stage is smaller than the ideal value shown in figure 2.18. Therefore a shift of the comparator levels of the first stage in the overall ADC transfer characteristics occurs which is demonstrated in figure 2.19. Specially the accuracy of the first stage is essential for the overall converter performance.

The gain error of the first and second stage of pipeline ADC is shown in figure 2.20. Inspecting this figure it can be seen that a gain error in the first stage has a large impact on the residue of the second stage. Alternating gain errors of the pipeline stages lead to a larger decrease of the linearity than the same gain error in each stage [5]. The shown gain errors are not realistic and were chosen very large for demonstration.

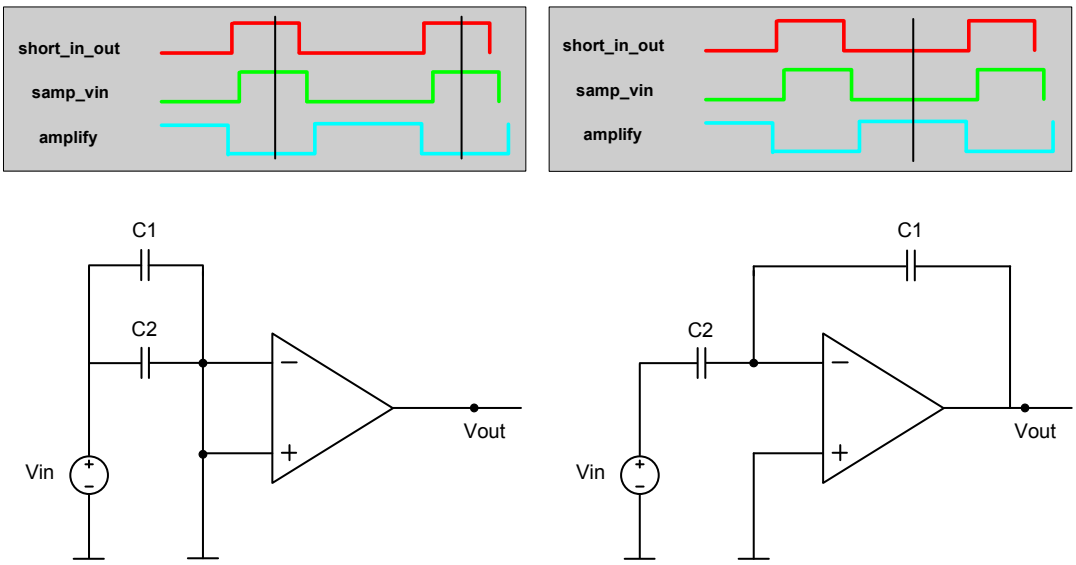

Figure 2.17: MDAC op-amp in sampling and amplification mode

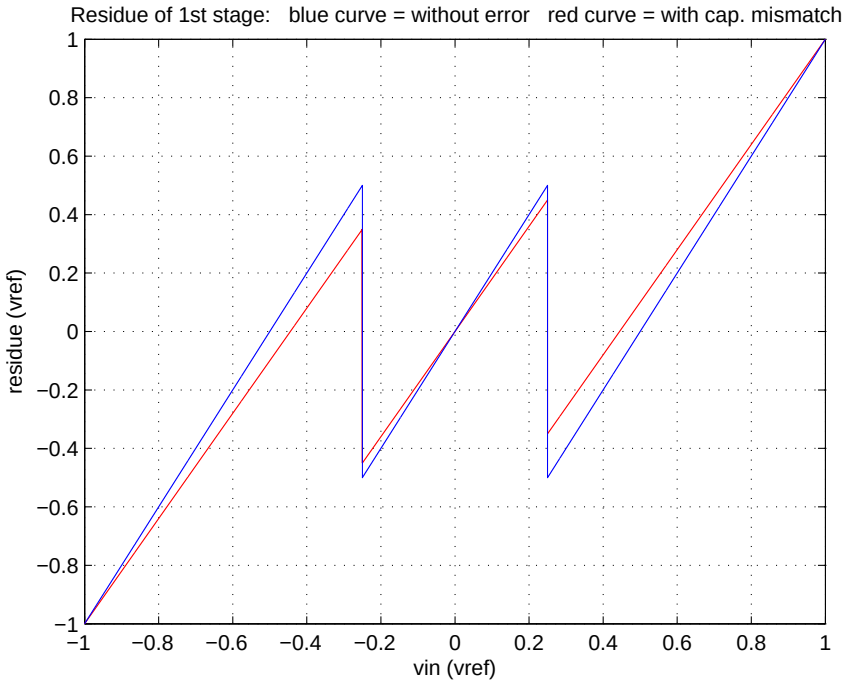

Figure 2.18: Residue of a 1.5bit stage with capacitor mismatch

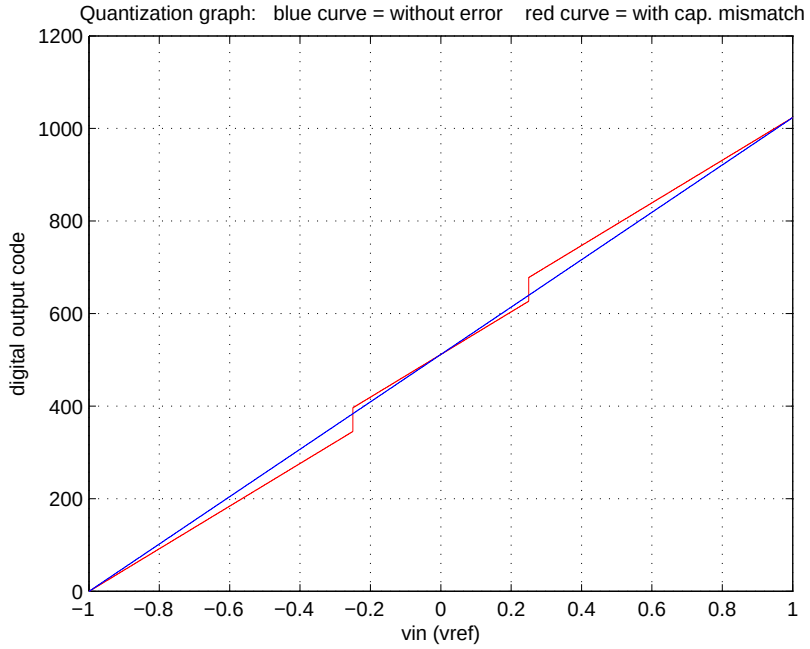

Figure 2.19: Residue of the first and second 1.5bit stage with capacitor mismatch

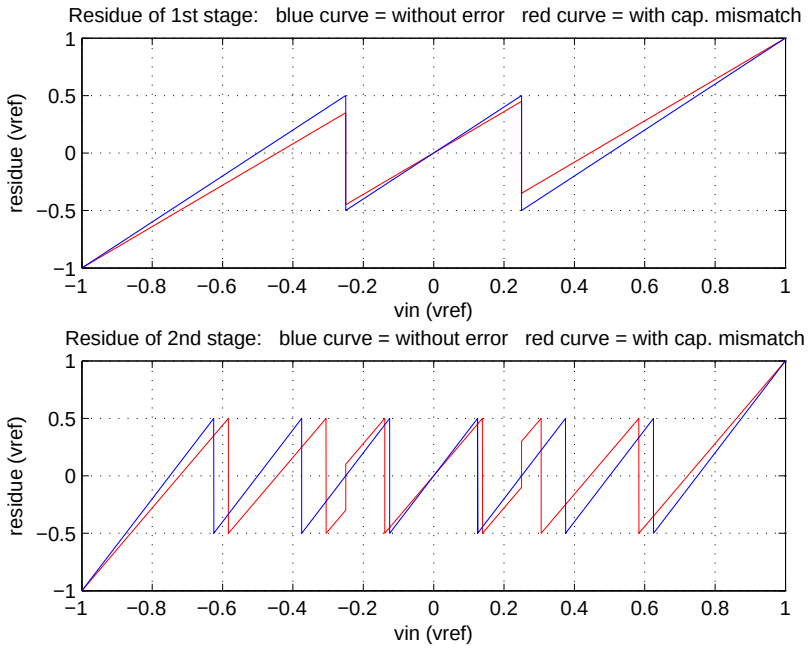

Figure 2.20: Residue of the first and second 1.5bit stage with capacitor mismatch

2.4.4 Total Harmonic Distortion

The total harmonic distortion (THD) 2.18 and the signal to noise ratio (SNR) are used to characterize an ADC. The THD is the ratio between the squared voltages of the signal and the tones. It measures the linearity which influences the picture quality. 5 to 10 harmonics are included in the THD and the rest is considered as noise.

$$THD(dB) = 10 \cdot log\left(\frac{V1^2}{V2^2 + V3^2 + V4^2..}\right) \tag{2.18}$$

2.4.5 Signal–to–Noise Ratio

The signal to noise ratio in dB corresponds for an ADC:

$$SNR(dB) = 1.76 + 6.02 \cdot N \tag{2.19}$$

N is the resolution of the ADC.

2.4.6 Signal–to–Noise and Distortion Ratio

Another important specific value is the signal to noise and distortion ratio (SNDR) which contains the distortion and thermal noise of a system. There the signal is referred to all unwanted components up to fs/2.

$$SNDR(dB) = 10 \cdot log\left(\frac{V1^2}{V2^2 + V3^2 + V4^2.. + \frac{V_{LSB}^2}{12} + thermalnoise}\right) \tag{2.20}$$

Moreover the spurious free dynamic range which is the difference in dB from the signal to the largest tone will be evaluated. Of course there are other error sources like noise, clock feedthrough and charge redistribution of the sample switches. They will be discussed in more detail in the pipeline ADC chapters.

2.5 Summary of Basics

This chapter gives an introduction of the different signal types. Starting with PAL and ending with HDTV RGB and YCrCb signals the requirement for the

processing was shown. Also the kind of synchronization for these signals was explained. Moreover the pipeline ADC and its error sources were discussed where the first stage is the most critical part of this ADC. Also the sampling of the MDAC and sub-ADC can be performed behind a 'Sample and Hold' or with separate sample networks. This will be explained in chapter 4.

Chapter 3

Analog Pre-Processing

The analog pre-processing is needed to amplify the input signal and to drive the ADC which converts the analog signal to digital. In this chapter different pre-processing architectures are investigated. Moreover the filter order will be challenged. Novel amplifier structures will be discussed in more detail. A combination of filter and AGC is compared to the two stages approach. Finally the experimental results are shown.

3.1 Pre-Processing Architecture

The pre-processing is used to amplify and filter the input signals for the ADC. But noise and distortion should not be emphasized. This is a hard requirement and can be managed by choosing the right topologies, transistor geometries and passive devices. A state of the art pre-processing consists of a single-ended input stage which drives directly the ADC. This requires low area and power but has a big drawback. The video source at the input must have low noise and distortion. Maybe the reader thinks in the age of digital broadcast and DVD-player the input source is no problem. But the very cheap DA converter at the output of a DVD-player or satellite receiver yields a lot of tones at out of band frequencies, which will introduce aliasing.

Another drawback of the single-ended input processing comprises the direct transfer of the environmental and switching noise of the digital outputs to the ADC. For standard video signals this was accepted, but for high definition video input signals with very high bandwidth the topology was improved. Also the usage of gm-C filters was considered. A dynamic range of 60dB can be achieved by this type of filters at input frequencies of 100MHz. The specification requires high linearity at low frequencies (10MHz) and 15dB lower linearity at high frequencies (60MHz). This is fulfilled for active RC filters with op-amps which have large loop-gain at low frequencies like a Miller op-amp [6]. However, the area

and power of the active RC filter approach is very low. In the next section two different approaches will be explained in more detail.

3.1.1 Pre-Processing with an 4^{th} order Bessel Filter

For suppression of noise and distortion a pseudo differential input and a 4^{th} order Bessel filter was chosen. Video signals are always single-ended. By converting them to differential the further processing becomes insensitive to noise and disturbances from substrate and supply. Figure 3.1 shows the principle topology of the 4^{th} order pre-processing. The input signal which covers a frequency range of 0 to 200MHz is applied to a single ended input buffer in unity gain configuration to achieve high input impedance. A 3.3V class AB stage is used to save power where the linearity requirements are also fulfilled. The shown capacitive coupling suppresses the DC component of the input signals. For clamping a current DAC is necessary to adjust the DC voltage at the input buffer to the black level of the video signal. The second input buffer amplifies the environmental noise and the switching noise of the digital outputs which is coupled by the substrate to the sensitive analog inputs. These disturbances at first order are cancelled out because of the pseudo differential concept.

The conversion from single ended to differential as well as the level-shift to 1.2V domain is performed in the AGC where two input ranges can be handled. In the AGC special care was taken on the harmonics. The best noise performance versus speed and power is achieved by using the AGC behind the input buffer. Only the noise of the input buffer is amplified. The 4^{th} order Bessel filter introduces a small overshoot and presents an adjustable cut off frequency varying from 28 to 96MHz. Moreover it drives the ADC input load at sampling rates up to 165MS/s. The second part of the Bessel filter has the lower cut off frequency than the first where the noise of the preceding stages will be damped. For reducing the area the first part of the Bessel filter can be realized by a Sallen-Key structure in the input stage shown in figure 3.2. Unfortunately it is necessary to do this structure two times because of the pseudo differential approach.

3.1.2 Pre-Processing with a 3^{rd} order Bessel Filter

A 3^{rd} order Bessel filter used in a video pre-processing can be a good trade-off between noise, power and area. For SD signals the harmonics of the color carrier must be attenuated. The difference between the 3^{rd} and 4^{th} order pre-processing corresponds to 5dB at three times of the cut off frequency. From the system point of view out of band tones of the input source must be filtered. Figure 3.3 shows the topology of a 3^{rd} order pre-processing. At the input there is the same structure as in the 4^{th} pre-processing. Only the first part of the Bessel filter was skipped where power and area were reduced. A drawback of this structure

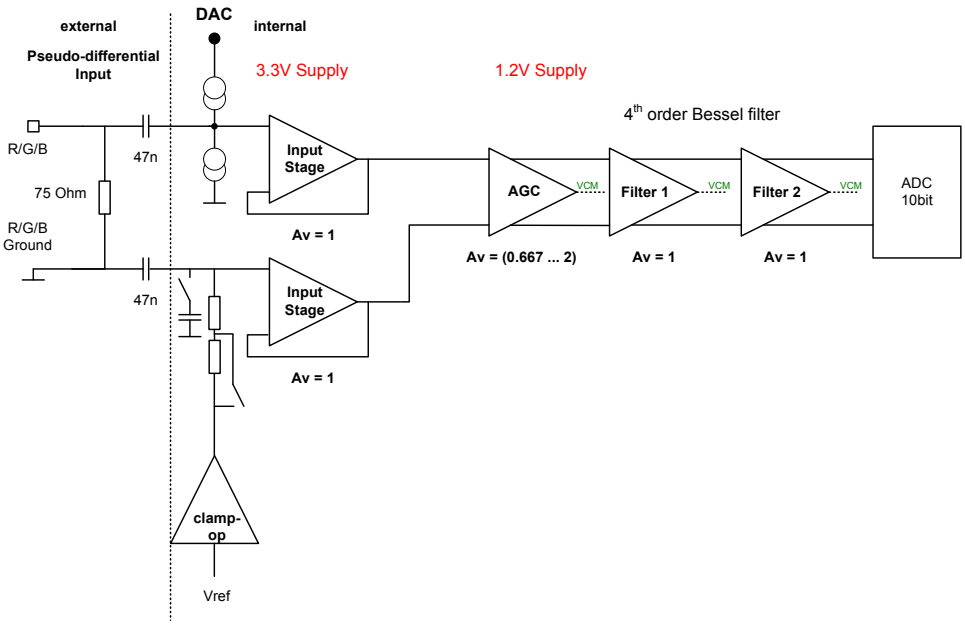

Figure 3.1: Principle Analog video Frontend with a 4^{th} order Bessel filter

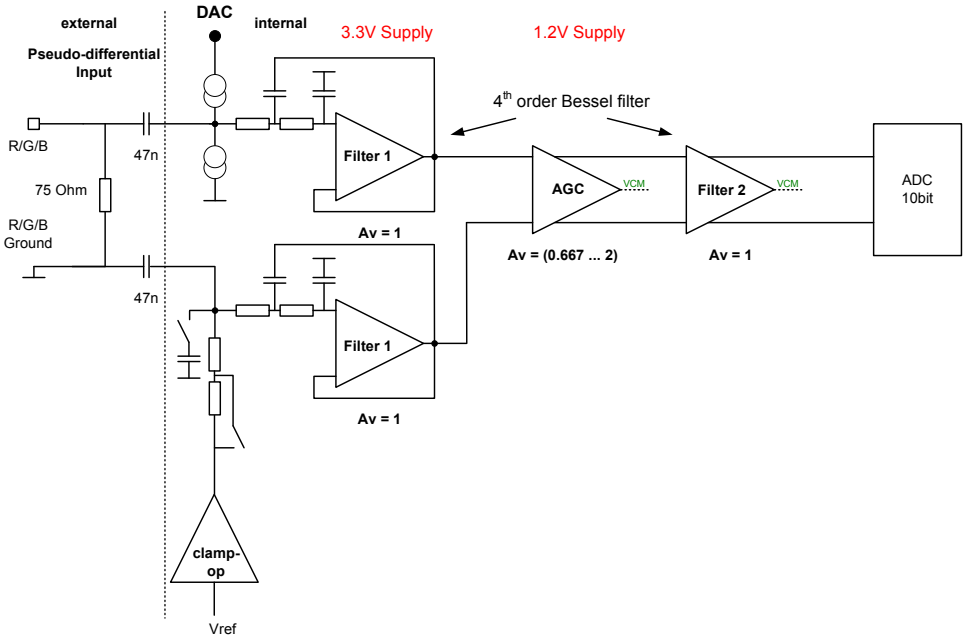

Figure 3.2: Principle Analog video Frontend with a 4^{th} order Bessel filter using a Sallen-Key input stage

is the high cut off frequency of the active part of the filter. This requires an

op-amp with a larger GBW than for a 4^{th} order pre-processing. Hence the power consumption of the op-amp is also increased. Moreover it is possible to combine the active part of the 3^{rd} order Bessel filter and the AGC in one stage. This is shown in figure 3.4 where the passive part of the filter is placed in front of the input stage.

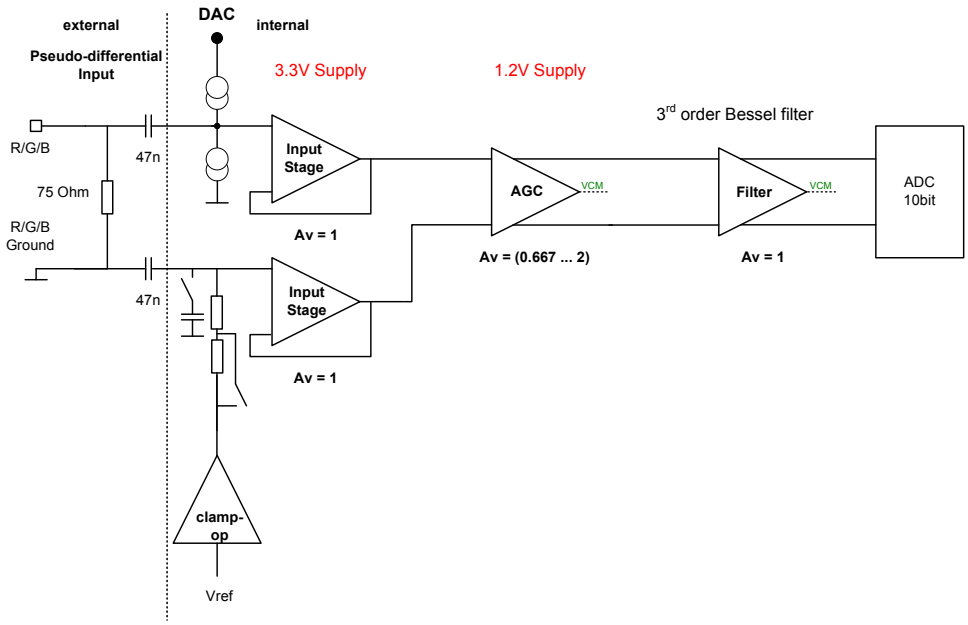

Figure 3.3: Principle Analog video Frontend with a 3^{rd} order Bessel filter

3.2 Area, Noise and Power Trade Off

Let us compare the different pre-processing's regarding area noise and power [7]. Also matching between the different RGB channels and the linearity is very important. Table 3.1 shows a comparison of the different approaches. Double upper arrow stands for extra large and single arrow means large. The right arrow shows acceptable. The 4^{th} order Bessel filter is the reference and starting point for the comparison and improvement. The linearity was measured for an input signal of 30MHz with an amplitude of 1Vpp. For power saving the 4^{th} order approach was the best choice and a good compromise for noise. But the silicon applied to a LCD Flat-panel TV shows some visible noise.

A drawback of the LCD display is its enhancement of noise due to its characteristic. In contrast to the old tube with its Gaussian luminance behavior the LCD amplifies existing noise. Depending on the filter programming the noise was decreased or increased.

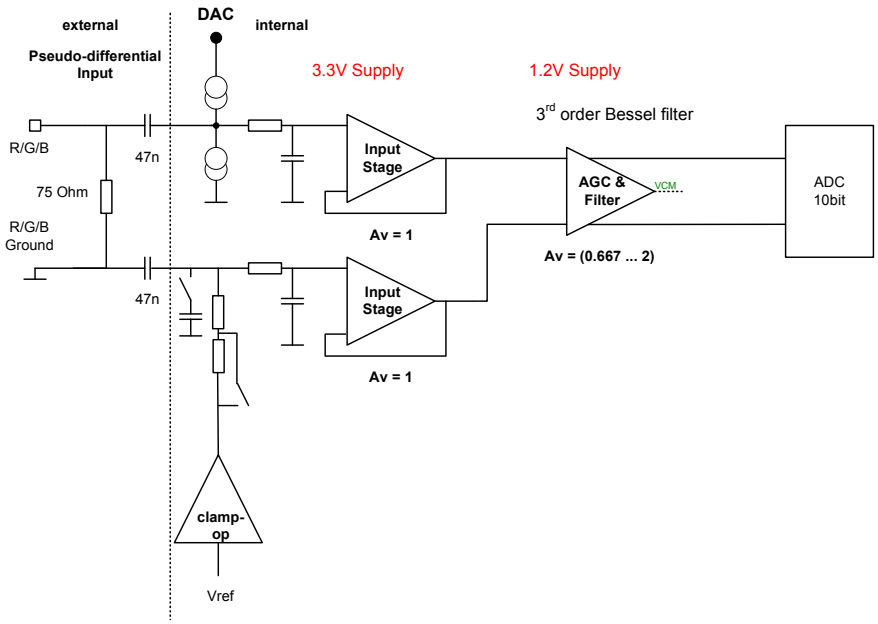

Figure 3.4: Principle Analog video Frontend with a 3^{rd} order Bessel filter and only 2 stages

Table 3.1: Comparison of different pre-processing topologies

Pre-Processing	Stages	THD	SNR	Matching	Power	Area
4^{th} order	4	$\Rightarrow$	$\Rightarrow$	$\Rightarrow$	$\Uparrow$	$\Rightarrow$
4^{th} order Sallen Key	3	$\Downarrow$	$\downarrow$	$\uparrow$	$\Downarrow$	$\Uparrow$
3^{rd} order	3	$\uparrow$	$\uparrow$	$\Rightarrow$	$\Rightarrow$	$\downarrow$
3^{rd} order AGC-Filter	2	$\Rightarrow$	$\Downarrow$	$\Uparrow$	$\Downarrow$	$\Downarrow$

For PC application the filter will be switched off to get a good sharp picture. Filter off means a 2^{nd} order filter with a cut off frequency of 200MHz. A part of the filter capacitor is used in the feedback branch of the op-amp to ensure

best settling results for an input step. Moreover the power consumption must be reduced to be competitive.
Therefore it was necessary to find a structure which has low power, area and noise. The compromise is the 3^{rd} order Bessel filter with 3 stages and low power consumption. The attenuation in the cut off range for multiples of the input frequency is lower than for the 4^{th} order Bessel filter.

3.3 Input Stage

The input stage has to buffer the input signal. Therefore two single ended low noise input buffers are used in unity gain configuration to operate the AGC. Pseudo differential inputs are used to decrease the sensitivity to digital and analog crosstalk which can be seen in figure 3.5. The input signal which covers a frequency range of 0 to 200MHz is applied to a single ended input buffer in unity gain configuration to achieve high input impedance. A 3.3V class AB stage is used to save power where the linearity requirements are also fulfilled. The shown capacitive coupling suppresses the DC component of the input signals.

For clamping a current DAC is necessary to adjust the DC voltage at the input buffer to the black level of the video signal. The second input buffer amplifies the environmental noise and the switching noise of the digital outputs which is coupled by the substrate to the sensitive analog inputs. These disturbances at first order are cancelled out because of the pseudo differential concept. The pseudo differential input can be switched off. In this case the reference voltage is filtered by an internal capacitor to reduce noise. If a signal is not applied the input buffer will be connected to common mode reference to get code 512 at the output of the 10bit ADC.

3.3.1 Coupling Effects

As shown in figure 3.5 digital outputs and digital processing generate current spikes on the supply and voltage spikes on ground. Due to capacitive coupling these spikes will be injected to the substrate. The substrate transmits this disturbance depending on its resistance to the analog input stages. There the transistors convert this substrate noise into a drain current by the bulk connection. For the differential structure only mismatch is the limitation for the PSRR. Moreover the crosstalk by the padring and pins was investigated and can be decreased by the pseudo differential input. This crosstalk is caused by the capacitive coupling of the pins. The mutual inductance of the bond-wires can be neglected. The on chip decoupling was optimized to shift the corner frequency of the bond-wire inductivities plus pin capacitance to a frequency larger than the clock frequency. Following measures were taken to decrease the coupling effects:

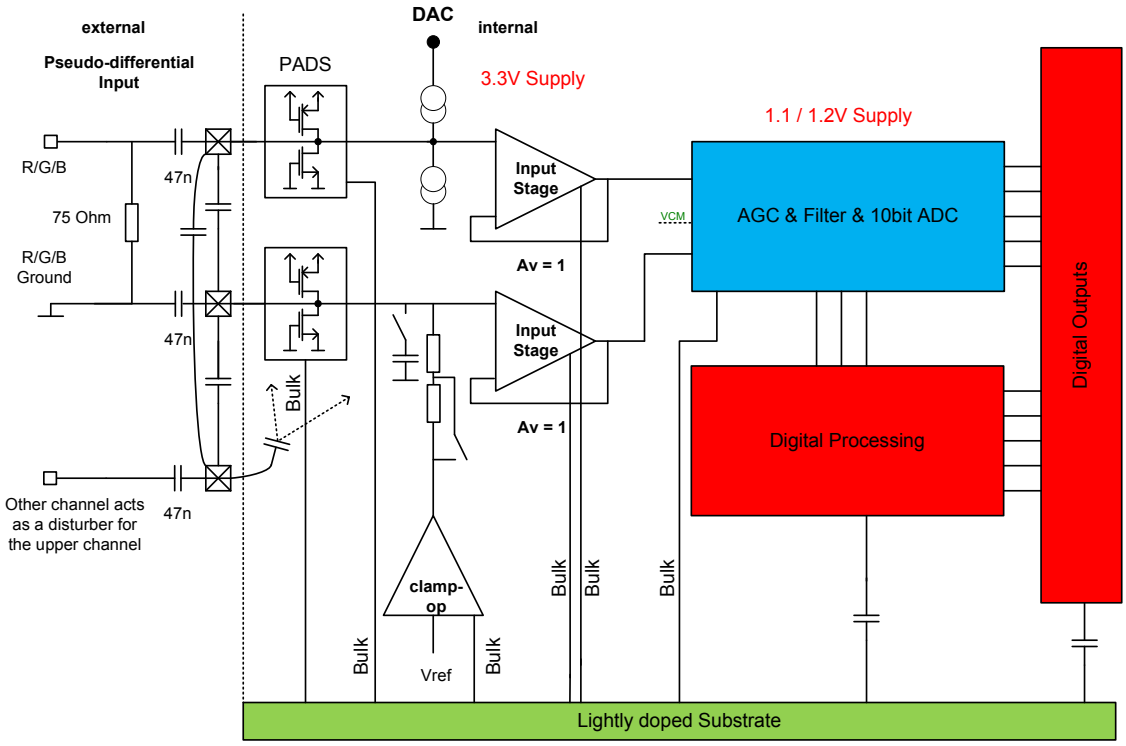

Figure 3.5: Principle topology of the pseudo differential input stage with its disturbance sources

- Large distance of the digital outputs to the analog inputs.
- Separate supplies for analog and digital.
- Several supplies.
- Orthogonal placement of analog input and output pin (no inductive coupling for very high frequencies).

3.3.2 Sallen Key

For the 2 stage prep the first filter was realized by a Sallen Key structure shown in figure 3.6. This filter can be used with a single ended op-amp connected as a follower. For optimal noise performance R1 and R2 of this filter must be equal. The parasitics can be compensated only by C1 (capacitor at the input of the opamp). A big drawback is the bad THD due to the positive feedback of the filter. Unsymmetrical switches and wiring show significant bad impact on the power supply rejection.

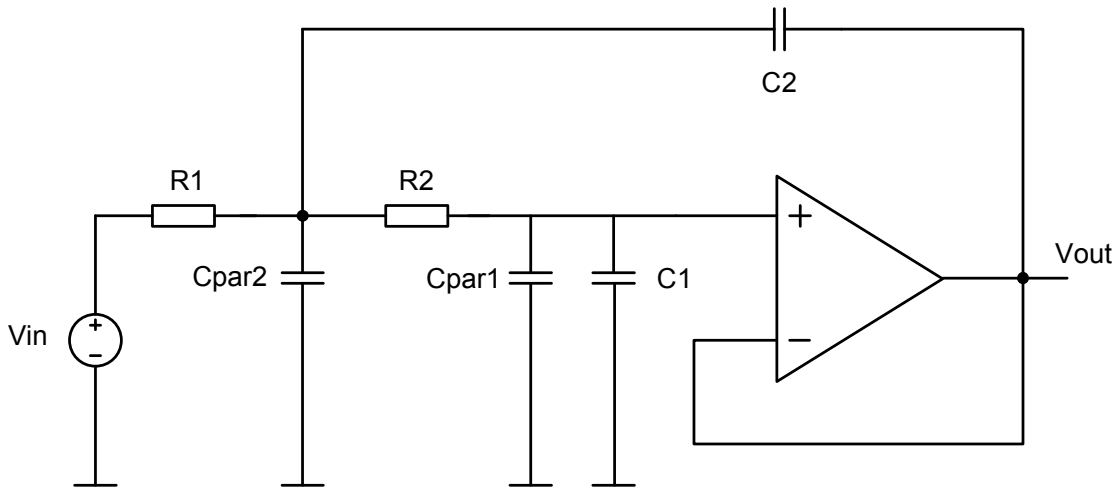

Figure 3.6: Principle topology of the Sallen Key filter

$$G(s) = \frac{1}{C2 \cdot R2 \cdot C1 \cdot R1 \cdot s^2 + (C1 \cdot R2 + C1 \cdot R1) \cdot s + 1} \tag{3.1}$$

3.3.3 Unity Gain Amplifier

A folded cascode op-amp with a class AB output stage [8] at a supply of 3.3V is used shown in figure 3.7. The quiescent current is about 1mA to get a very large unity gain bandwidth GBW of 1.5GHz and a slew rate of 1.4GV/s. The large PMOS input transistors yields low noise and offset where video signals can be handled down to 0.1Volt. The maximum input voltage is around 2V. M3 and M4 are used to adjust the biasing voltage for the output transistors. The impedance at the source is about 1/gm but can be neglected because the output transistors are driven with the same phase and amplitude. So no AC current can flow and the impedance between the output transistors is infinite. A drawback exists for large input voltages which limit the output current.

Special care was taken on the output transistors concerning the hot carrier effect. This will appear for large drain source voltage (VDD3V3) and very high currents. A measure was to increase the channel length and avoiding the connection of the output to ground in any condition. Also well proximity effects and negative bias temperature instability were considered.

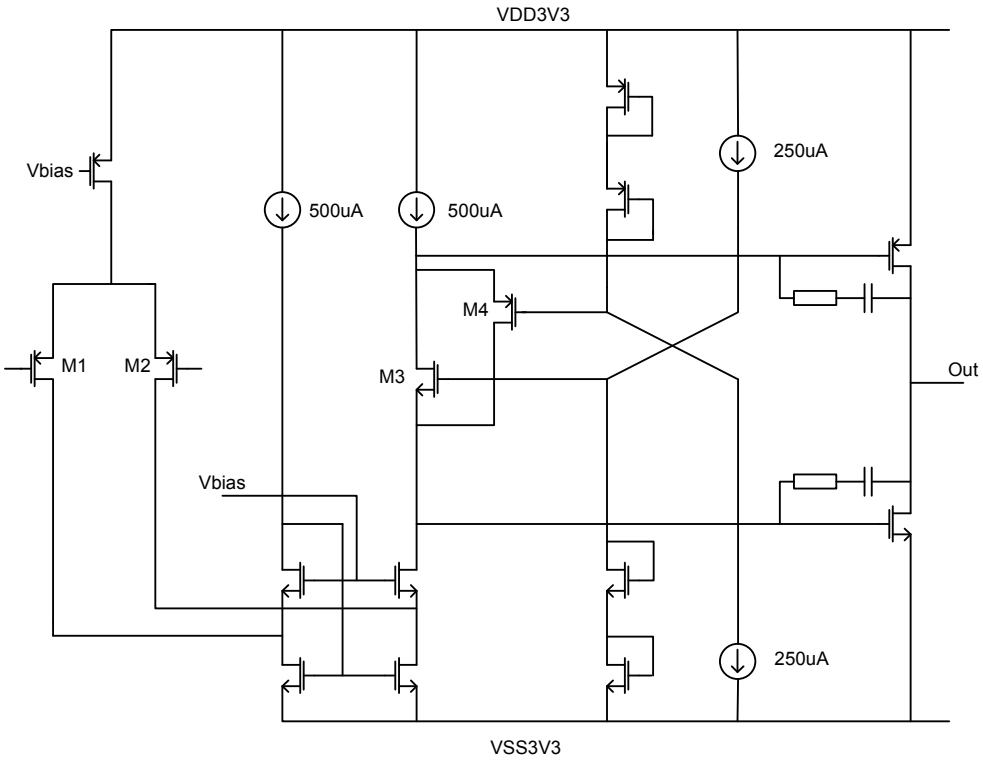

Figure 3.7: Principle schematic of the folded cascode class AB input buffer

3.4 Clamping and Clamp DAC

The clamping circuit adapts the DC part of an analog video signal to the processing range of the input stage. For the reconstruction of these DC levels reference levels in the video signals are used. Figure 3.8 shows a regular standard TV signal. For clamp reference level the back porch or the synchronization base can be applied. There exists two types of clamping methods $\Longrightarrow$

- Coarse clamping: Clamping to the bottom of the synchronization pulse.
- Fine clamping: This is done by current sources which are part of a control loop consisting of an ADC and logic.

In case of fine clamping current sources are used to generate a voltage step at the top plate of the coupling capacitor. In Equation 3.2 this voltage step is calculated depending on the clamp time, k amount of current sources and the clamp capacitor.
The reason for the clamp control loop is the occurrence of disturbances like $\Longrightarrow$

- Grid interference at 100Hz and 400mVpp (luminance modulation).

- Macrovision pulses.
- Pad leakage currents specifically at DSM technologies (50nA)

The LSB current of the clamp DAC must be chosen in the range of 2μA where the resulting voltage pulse is smaller than 1LSB of the 10bit ADC. Hence there is no luminance step during one line visible.

$$dU = \frac{\Delta Q}{C} = \frac{\Delta t \cdot I}{C} = \frac{\Delta t \cdot k \cdot I}{C} \tag{3.2}$$

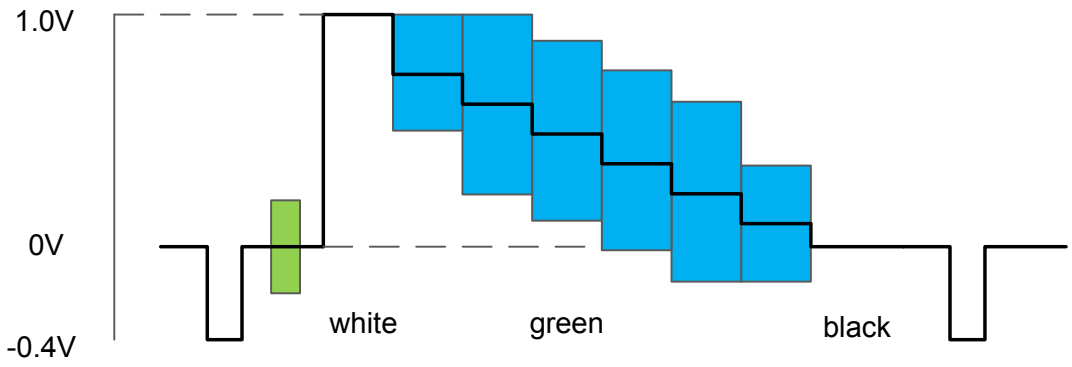

Figure 3.8: Standard video signal with synchronization pulse und black porch

The clamp DAC is a current steering DAC for a so called keyed clamping. During a measurement window the black level will be measured and after that during a clamp window the calculated clamp current applied. The clamp DAC is also used to compensate the voltage offset between three RGB channels. This offset was calculated and measured at the input of the channel. It corresponds to 50LSBs between two channels. The clamp DAC adjusts the input to a defined voltage level to get at the output of the ADC a defined digital level for the back porch. The worst case for clamping is a video line with much time between two clamp windows. For a PAL signal this would be 64us.

For DSM technologies like 90 and 65nm the leakage current around 50nA causes a big problem for the clamping. The induced LSB clamp charge during one line must be fine enough to compensate this leakage current. Equation 3.3 shows the dependency of the voltage increase on the leakage current, the time between two clamp windows and the coupling capacitor.

$$dU = \frac{I_{leakage} \cdot t}{C_{coupling}} \tag{3.3}$$

Figure 3.9 shows the topology of the binary weighted clamp DAC. This 9bit

clamp DAC consists of three parts. The first part represents the current sources k7 to k4 which are directly mirrored to the output current sources. The second part consists of the current sources k3 to k0, which are directly connected to the output. Only the up and down switches are in between. They are also used to switch the sign current of 2.5uA. This direct current source connection is necessary to generate current steps at the output without charging the large parasitic capacitors of the output current sources. Additionally for course clamping a very small current source is used to decrease the voltage at the input stage during one video line. At the beginning of the video line the MSB PMOS current source is switched on for several μs and increases the voltage at the coupling capacitor.

Moreover the current could be doubled to handle large clamp disturbances at coupling capacitors larger than 100nF. The requirements on INL and DNL is very low. Also the absolute accuracy of the LSB current could be very low. There is only the requirement for a given monotonicity which is fulfilled due to the current ratios. Spikes and glitches are filtered by the large coupling capacitor. The clamp DAC works at clock rates of 40MHz and is active after the synchronization pulse and before the effective video signal starts. Otherwise a disturbance in the picture would be visible.

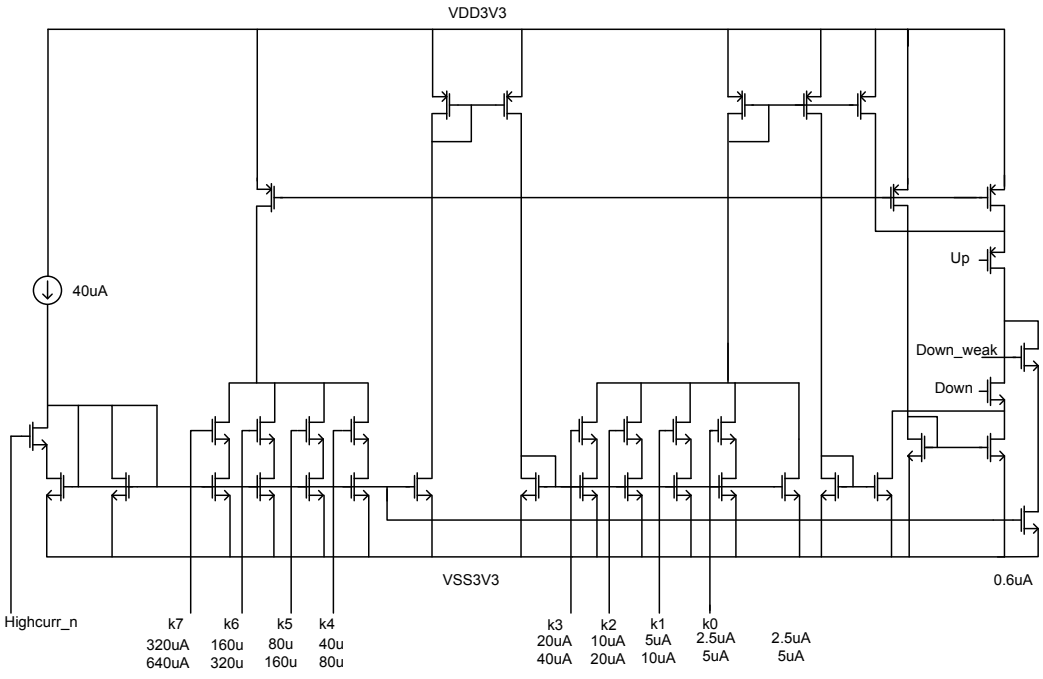

Figure 3.9: Principle schematic of the current steering clamp DAC

3.5 Automatic Gain Control (AGC)

Video frontends need an automatic gain control to get the optimum signal to noise ratio for the ADC and to get the correct brightness level of the picture. Of course this can be done also digital but in the analog domain we can increase the signal to noise ratio at the input of the ADC by this technique. The specification requires a fixed voltage at the input of the ADC which can be 100% or 80% of the reference voltage. The gain characteristic of the AGC can be changed between an input voltage of 1.8Vpp and 1.5Vpp to get the largest SNR at the input of the ADC. RGB signals are around 1.5Vpp where the lowest gain characteristics yields some headroom for overshoot at the input of the ADC.

So the AGC can be switched between best SNR or headroom for overshoot which depends on the signal quality of the source shown in figure 3.10. The switching of the AGC should not be visible in the picture where a resolution of 6bit comes out for the programming of the AGC. At the largest gain also the largest step size is achieved. The input voltage can be calculated depending on the minimum and maximum input voltage and on the programming of the AGC related to 63 for 6bits.

$$vin_{agccode} = vin_{min} + \frac{(vin_{max} - vin_{min}) \cdot agccode}{2^{bit} - 1} \tag{3.4}$$

The gain can be calculated for a constant output voltage vout which equals the ADC input voltage.

$$gain_{agccode} = \frac{vout}{vin_{agccode}} \tag{3.5}$$

The matching calculations base on the pair-wise mismatch of non silicided poly-p resistors. Equation 3.6 shows the deviation of the resistor depending on the mismatch factor of the technology k, the value of the resistor and its area. To get the absolute deviation of the resistor the pair-wise mismatch value must be divided by the square root of two. In the next sections various AGC architectures are investigated concerning noise, distortion, matching and power consumption.

$$dR = \frac{R \cdot k(\mu m)}{\sqrt{Area}} \tag{3.6}$$

3.5.1 AGC with Parallel Switching

As can be seen this architecture in figure 3.11 can be realized by switching in parallel binary weighted resistors. Hence, the required 1/x gain characteristic can be reached. It can be realized by using a fixed gain of 2 where the feedback

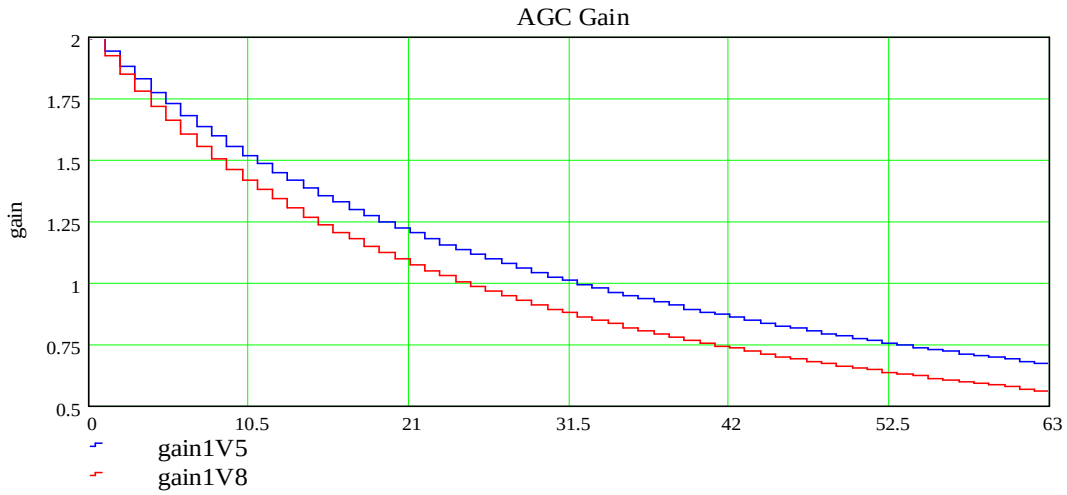

Figure 3.10: Characteristic of the AGC for two different input voltages

resistor is reduced to generate a minimum gain of 0.55. Care must be taken on the stability by using switched in parallel capacitors to the feedback resistors. This topology of switching resistors in parallel in the feedback path is easy to realize and has good linearity, noise performance and matching behavior. The linearity is improved by using a switch in the input branch. Only eight level-shifters are necessary to drive the 3.3V switching transistors. The 3.3V transistor were chosen to decrease the on-resistance and the parasitic capacitors compared to the low voltage transistors. A drawback is the varying loop gain of the op-amp which effects the stability. The switches in series of the unity resistor must be chosen large to avoid an influence on the gain.

The switching between the different required gain characteristics can be reached by reducing the feedback resistor with a shortcut by a closed switch. The gain matching is about 0.2% for the 65nm design. DSM technologies help to improve the matching because the structures are getting smaller and smaller. Hence the lithography must be more accurate but the resistor width stays nearly the same. Of course the square resistance increases but the mismatch factor decreases more.

The gain matching was calculated depending on the statistic variation of the resistors. It was assumed that the variation of each resistor is independent from each other resistor. Hence the error propagation calculation was used. The several deviations of the gain transfer functions are not shown in the following equations. The influence of the op-amp on the gain matching can be neglected if the open-loop gain is large enough.

$$R2t_{agccode} = R1t \cdot gain_{agccode} \tag{3.7}$$

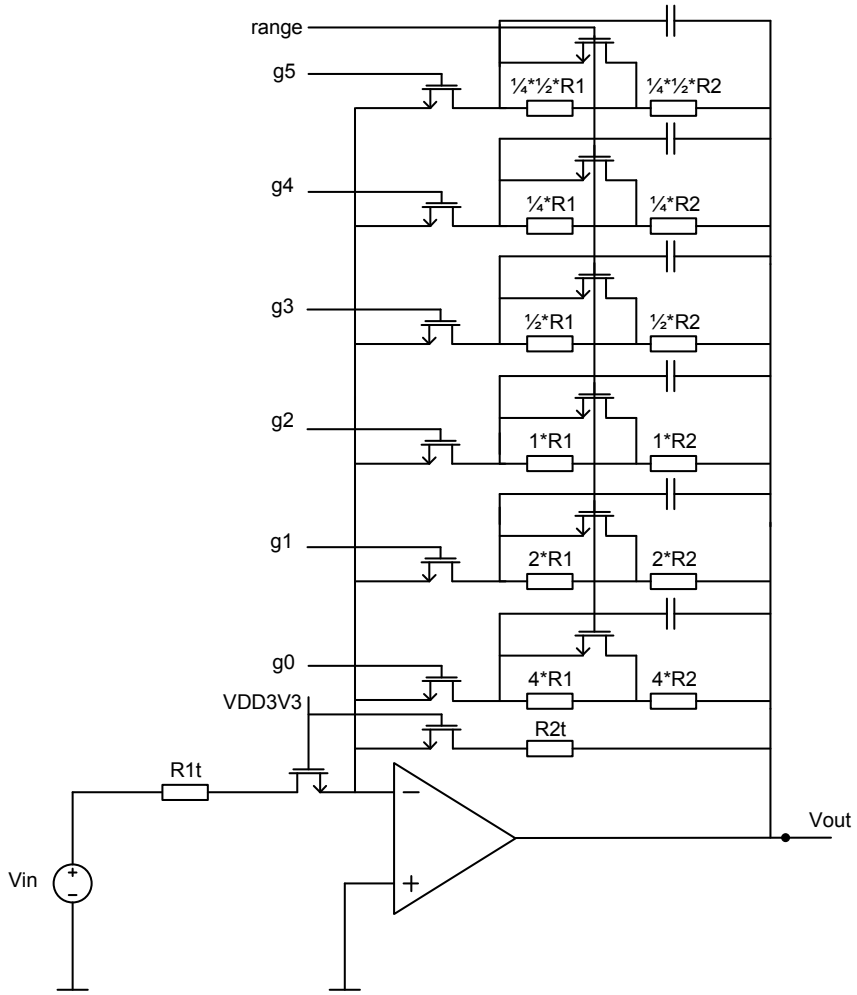

Figure 3.11: Principle topology of the AGC with binary weighted resistors in the feedback path

$$Rp = \frac{1}{\frac{1}{R2t(1)} - \frac{1}{R2t(0)}} \tag{3.8}$$

Rp is the LSB resistor of the parallel switched binary weighted resistor array. In figure 3.11 it can be seen that Rp corresponds to 4*R1 plus 4*R2. This comes out of the realization in the schematic.

$$R2 = \frac{1}{\frac{1}{R1t \cdot gain_{agccode(0)}} + \frac{kp}{Rp}} \tag{3.9}$$

Equation 3.9 shows the evaluation of R2 depending on the maximum gain of 2 at

agccode 0. Kp is varied from 0 to 63 where 1/R2 corresponds to a linear function. Thus binary weighted resistors can be switched in parallel.

$$dR2 = \frac{R2 \cdot k}{\sqrt{W^2 \cdot 2 \cdot \frac{R2}{Rsqr}}} \tag{3.10}$$

The absolute deviation of R2 was calculated where a factor of 2 is taken in the square root. For the area evaluation the square resistance of the resistor is considered which depends on the technology. This was also done for R1t.

$$dRp = \frac{Rp \cdot k}{\sqrt{(W \cdot kp)^2 \cdot 2 \cdot \frac{R2}{kp \cdot Rsqr}}} \tag{3.11}$$

The absolute deviation of Rp was calculated depending on kp. If two Rps are switched in parallel the resistor value will be divided by two and the width will be doubled.

$$dR2o_{kp} = \sqrt{\left(\frac{\left(\frac{Rp}{kp}\right)^2 \cdot dR2}{\left(R2 + \frac{Rp}{kp}\right)^2}\right)^2 + \left(\frac{R2^2 \cdot dRp}{\left(R2 + \frac{Rp}{kp}\right)^2}\right)^2} \tag{3.12}$$

By using the error propagation calculation the absolute deviation dR2o of R2 and Rp can be evaluated. R2 and dR2 were taken for an infinite Rp.

$$dgain_{kp} = \sqrt{\left(\frac{dR2o}{R2}\right)^2 + \left(\frac{dR1t}{R1t}\right)^2} \tag{3.13}$$

Equation 3.13 shows the relative gain error of the AGC which is also illustrated in figure 3.12. The gain error decreases for lower gain because of switching in parallel a lot of resistors.

3.5.2 AGC with T-Network at the Input

This is a very nice approach to get an AGC with less amount of resistors. Due to the required AGC characteristics a parallel switching of binary sized resistors is possible. The vertical branch of the T-structure in front of the AGC consists of 4 thermometer coded resistors and 4 binary weighted resistors switched in parallel shown in figure 3.13. Switching between a maximum input signal of 1.5Vpp and 1.8Vpp can be realized by reducing the value of the second to the eight resistor. This can be easily done by a switch. Unfortunately this switch has a large on resistance which influences the gain and depends on the size of the transistor. A

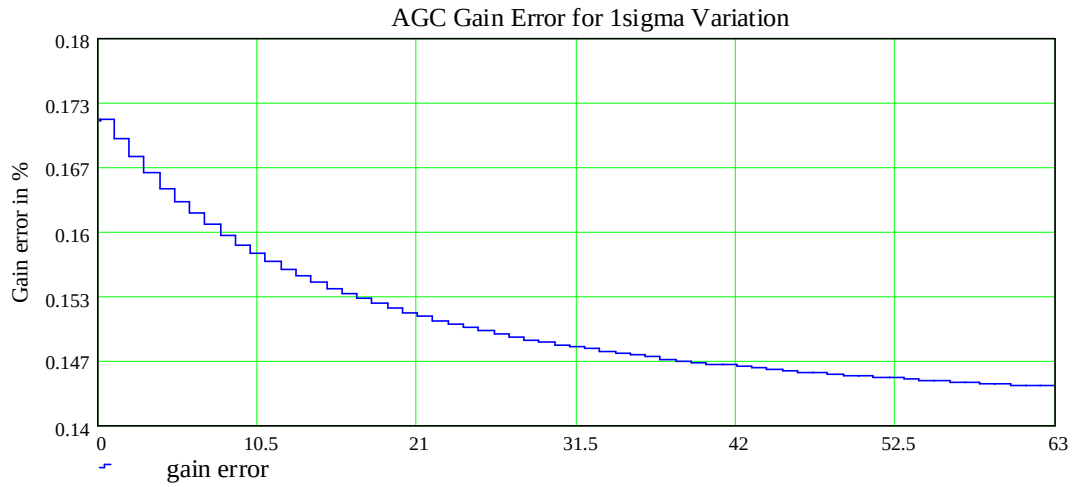

Figure 3.12: Gain error in % for one sigma variation of the resistors for 65nm technology

large transistor has large parasitics and can decrease the bandwidth of the whole AGC. This bandwidth must be much larger than the maximum filter corner frequency. One advantage is that there are no switches in the signal path which effects the linearity positively. The gain matching is in the range of 0.22% where the different AGC topologies were designed for the same area to be comparable. The linearity is fulfilling the specification and the noise is in the range of the topology with the binary weighted network in the feedback path. Only 9 level-shifters are necessary to drive the switches.

Due to the T-network the input will be damped and then amplified by an inverting amplifier with a fixed gain. The op-amp must have a unity gain bandwidth larger than an op-amp needed for the gain of 2 for the tapped AGC. This structure can be also used for a part of the Bessel filter. So area and power can be saved. Because of noise and area requirements the horizontal resistors of the T-structure must be lower than 1k. This has the drawback of a very low load resistance for the input stage in front of the AGC. Unfortunately the noise is increased if the AGC damp the input signal. This is a very essential drawback because most of the video signals are larger than 1Vpp.

For gain matching the resistors of the gain stage are calculated to get the basis for further calculations.

$$R1_{agccode} = \frac{R2}{gain_{agccode}} \tag{3.14}$$

R1t and R2t could be chosen different. Hence if R1t is smaller than R2t the input stage has to be designed to drive this resistor specifically at the lowest gain.

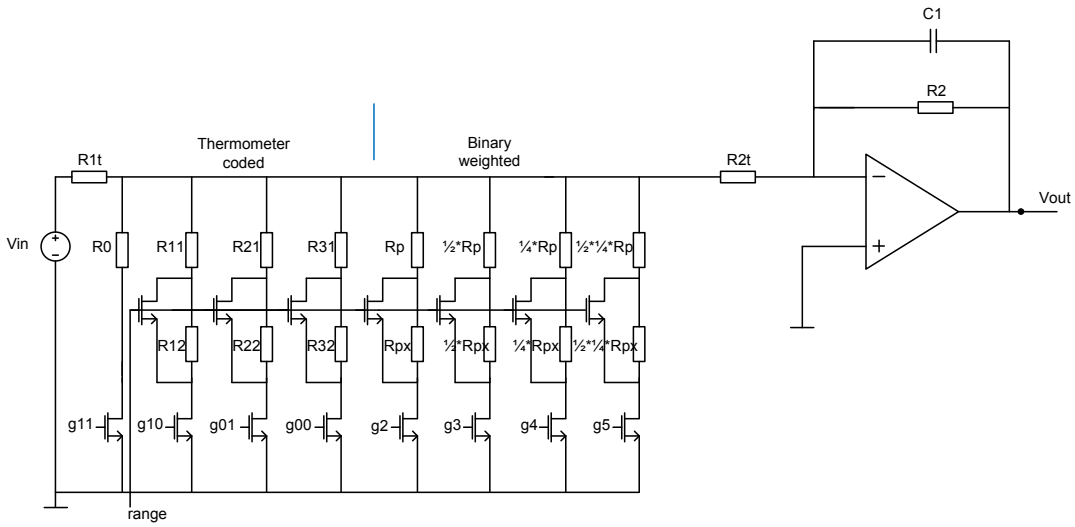

Figure 3.13: Principle topology of the AGC with binary weighted resistors in the input branch

There all resistors (R3) in the vertical branch are connected in parallel. A large R2t decreases the effective gain of the amplifier which corresponds to R2/R2t.

$$R3_{agccode} = \left(\frac{R1t \cdot R2t}{R1_{agccode} - R1t - R2t} \right) \tag{3.15}$$

In equation 3.15 the effective resistor of the vertical branch of the T-network is calculated.

$$Rp = \frac{1}{\left(\frac{1}{R3_{agccode(4)}} - \frac{1}{R3_{agccode(0)}} \right)} \tag{3.16}$$

Next the LSB resistor Rp of the 4 binary weighted resistors is calculated. The reason for 4 thermometer and 4 binary coded resistor is area and complexity.
For the only binary weighted solution the 64 parallel switched resistors consume a lot of area (Rp=2.6kΩ). Compared to the parallel switched architecture the damping and adjacent amplification needs a small R3 and thus also a small Rp. Out of the matching calculations the width of Rp must be large. However the parallel switching architecture can stay with very thin resistors in the feedback path for Rp (0.5μm).

$$agccode = 0..3 \tag{3.17}$$

$$kp = 0..15 \tag{3.18}$$

$$R3_{agccode,kp} = \frac{1}{\left(\frac{R1_{agccode} - R1t - R2t}{R1t \cdot R2t}\right) + \frac{kp}{Rp}} \tag{3.19}$$

Equation 3.19 shows the evaluation of R3 depending on the agccode and the amount of parallel switched resistors. The lowest effective R3 is around 140Ω. The best result for matching comes out for a very large width of R1t, R2t (6μm) and R2 (5μm). The width of R3 and Rp could be in the range of (1μm).

$$dR1t = \frac{R1t \cdot k}{\sqrt{W_{R1t}^2 \cdot 2 \cdot \frac{R1t}{Rsqr}}} \tag{3.20}$$

$$dR2t = \frac{R2t \cdot k}{\sqrt{W_{R2t}^2 \cdot 2 \cdot \frac{R2t}{Rsqr}}} \tag{3.21}$$

$$dR3 = \frac{R3 \cdot k}{\sqrt{W_{R3}^2 \cdot 2 \cdot \frac{R3}{Rsqr}}} \tag{3.22}$$

$$dRp = \frac{Rp \cdot k}{\sqrt{(Wp \cdot kp)^2 \cdot 2 \cdot \frac{Rp}{kp \cdot Rsqr}}} \tag{3.23}$$

$$dR3o_{kp} = \sqrt{\left(\frac{\left(\frac{Rp}{kp}\right)^2 \cdot dR3_{agccode}}{\left(R3_{agc_code} + \frac{Rp}{kp}\right)^2}\right)^2 + \left(\frac{R3_{agccode}^2 \cdot dRp}{\left(R3_{agccode} + \frac{Rp}{kp}\right)^2}\right)^2} \tag{3.24}$$

Equation 3.24 shows the evaluation of the variation of the overall R3 including the variation of Rp.

$$dR1_{agccode,kp} = \sqrt{\left(\left(1 + \frac{R1t}{R3_{agccode,kp}}\right) \cdot dR2t\right)^2 + \left(\left(1 + \frac{R2t}{R3_{agccode,kp}}\right) \cdot dR1\right)^2 + \\ + \left(\left(\frac{-R1t \cdot R2t}{R3_{agccode,kp}^2}\right) \cdot dR3o_{agccode,kp}\right)^2} \tag{3.25}$$

$$dgain = \sqrt{\left(\frac{dR1_{agccode,kp}}{R1_{agccode}}\right)^2 + \left(\frac{dR2}{R2}\right)^2} \tag{3.26}$$

The relative gain error is calculated in equation 3.26. The resistor R1 is evaluated for an agccode of 0 to 63 where the kp factor was skipped to simplify the equation. Figure 3.14 shows the dependency of the gain error on the programming. The lowest error is achieved at the maximum gain because of the large R3 which results in a low dR1.

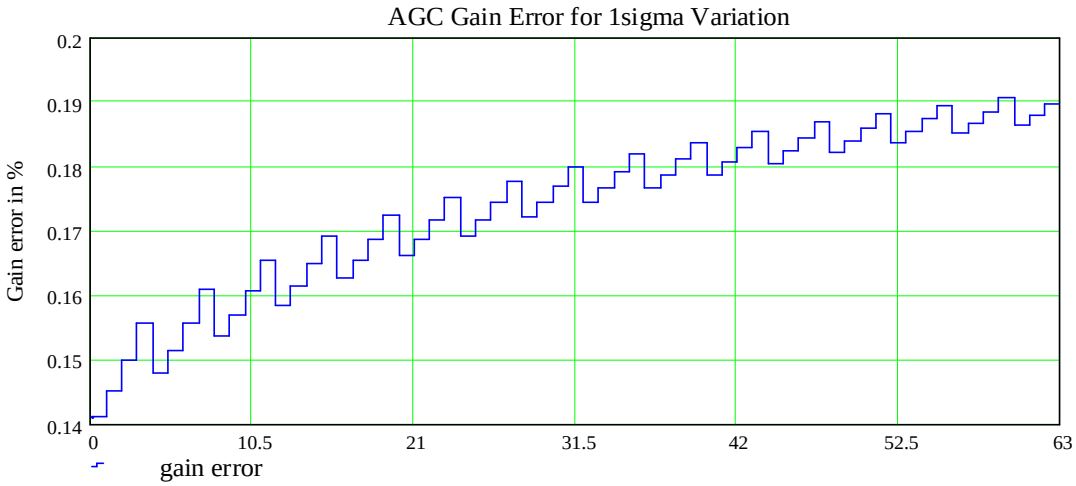

Figure 3.14: Gain error in % for one sigma variation of the resistors for 65nm technology

3.5.3 AGC with T-Network and Part of the Bessel Filter

The combination between AGC and filter yields a good tradeoff between power and area illustrated in figure 3.15. So the second part of the 3^{rd} order Bessel filter and the AGC can be realized in one stage. The first part is a passive RC low pass in front of the input buffer. A peaking in the frequency response occurs at the center node of the T-network. This peaking is influenced by R5 and is increased with larger values of R5. In addition to that a large R5 yields low noise at the output. The filter was calculated without the consideration of the voltage divider. Because of the matching requirements the width of the resistors is very large and thus the parasitic capacitors.

The parasitics of R1 and R3 increase the overall cut off frequency and produces peaking around the cut off frequency. The parasitic capacitor of R2 decreases the

overall cut off frequency. The 3dB frequency of this combined stage is 1.4 times higher than the overall corner frequency. Hence the op-amp must be fast enough to drive the ADC and does not effect the overall cut off frequency.

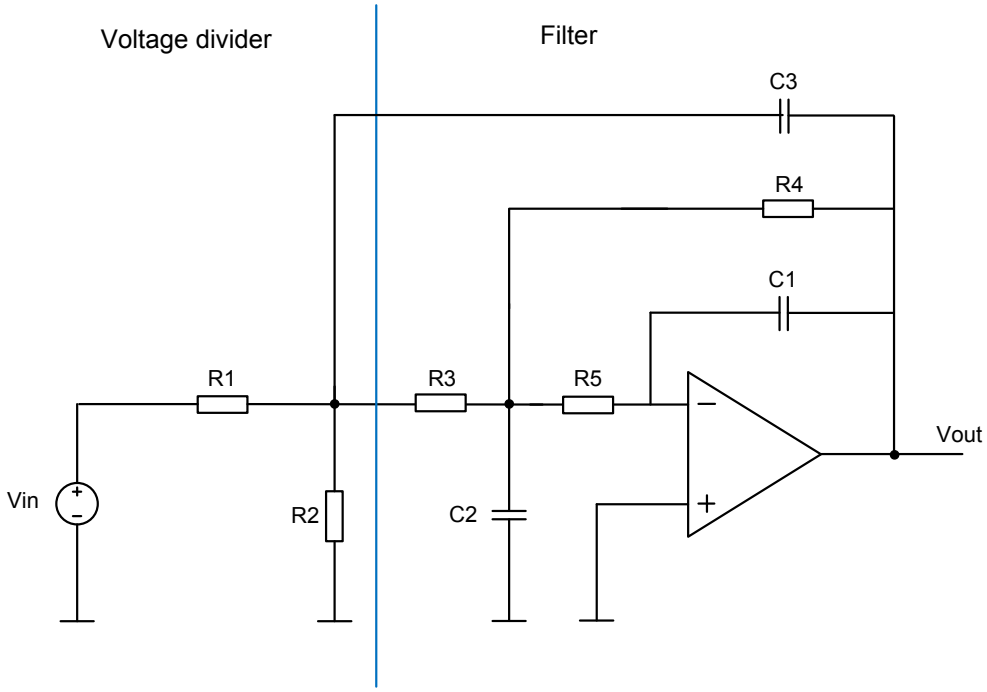

Figure 3.15: Simplified topology of the AGC with T-network in the input branch

The filter capacitors C1 and C2 are calculated for the active part of the combined stage. Therefore C3, R1 and R2 are neglected. Out of the ideal transfer function the 2 conjugated roots of this active part are evaluated.

$$G_{ideal}(f) = \frac{-\frac{R4}{R3}}{\left(s(f)^2 \cdot C1 \cdot C2 \cdot R4 \cdot R5 + s(f) \cdot C1 \cdot \left(\frac{R4 \cdot R5}{R3} + R4 + R5\right)\right)} \tag{3.27}$$

In the following equations the overall transfer function of the AGC plus second part of the 3^{rd}order filter is calculated. The capacitors C1 and C2 were inserted. First of all the coefficients of the transfer function are evaluated.

$$k0 = 1 \tag{3.28}$$

$$k1(C3) = \frac{C1 \cdot R2 \cdot R4 \cdot R5 + C1 \cdot R2 \cdot R3 \cdot R5 + C1 \cdot R2 \cdot R3 \cdot R4}{R2 \cdot R3 + R1 \cdot R3 + R1 \cdot R2} +$$

$$+\frac{C1\cdot R1\cdot R4\cdot R5+C1\cdot R1\cdot R3\cdot R5+C1\cdot R1\cdot R3\cdot R4+C1\cdot R1\cdot R2\cdot R5}{R2\cdot R3+R1\cdot R3+R1\cdot R2}+$$
$$+\frac{C1\cdot R1\cdot R2\cdot R4+C3\cdot R1\cdot R2\cdot R4+C3\cdot R1\cdot R2\cdot R3}{R2\cdot R3+R1\cdot R3+R1\cdot R2} \tag{3.29}$$

$$k2(C3)=\frac{C2\cdot C1\cdot R2\cdot R3\cdot R4\cdot R5+C2\cdot C1\cdot R1\cdot R3\cdot R4\cdot R5}{R2\cdot R3+R1\cdot R3+R1\cdot R2}+$$
$$+\frac{C2\cdot C1\cdot R1\cdot R2\cdot R4\cdot R5+C3\cdot C1\cdot R1\cdot R2\cdot R4\cdot R5}{R2\cdot R3+R1\cdot R3+R1\cdot R2}$$
$$+\frac{C3\cdot C1\cdot R1\cdot R2\cdot R3\cdot R5+C3\cdot C1\cdot R1\cdot R2\cdot R3\cdot R4}{R2\cdot R3+R1\cdot R3+R1\cdot R2} \tag{3.30}$$

$$k3(C3)=\frac{C3\cdot C2\cdot C1\cdot R1\cdot R2\cdot R3\cdot R4\cdot R5}{R2\cdot R3+R1\cdot R3+R1\cdot R2} \tag{3.31}$$

The overall transfer function will be shown in 3.32.

$$Gcomp(f)=\frac{\frac{R2\cdot R4}{R2\cdot R3+R1\cdot R3+R1\cdot R2}}{s(f)^3\cdot k3+s(f)^2\cdot k2+s(f)\cdot k1+k0} \tag{3.32}$$

An error function was evaluated where the roots of the ideal and real transfer function are calculated. In equation 3.33 the magnitude of the imaginary and real part of the ideal and real transfer function depending on C3 are subtracted to find the minimum.

$$error(C3)=||IM(roots_{ideal})|-|IM(roots_{comp})||$$
$$+||RE(roots_{ideal})|-|RE(roots_{comp})|| \tag{3.33}$$

C3 is varied from 0 to 700fF to generate a vector. Next the minimum is searched with a specific function of Mathcad. For different cut off frequencies different C3 are necessary. The gain programming has no influence on the cut off frequency. Figure 3.16 shows C3 depending on corner frequency for an R5 of 250Ω. The optimum R5 is around 1000Ω because of a voltage noise reduction of 50% compared to 250Ω. The compensation has less influence for low frequencies. Only three different compensation capacitors could be used for the whole range.
Two complex poles are identical with the ideal poles. The real pole in the negative domain can be neglected because it is very large shown in figure 3.17.

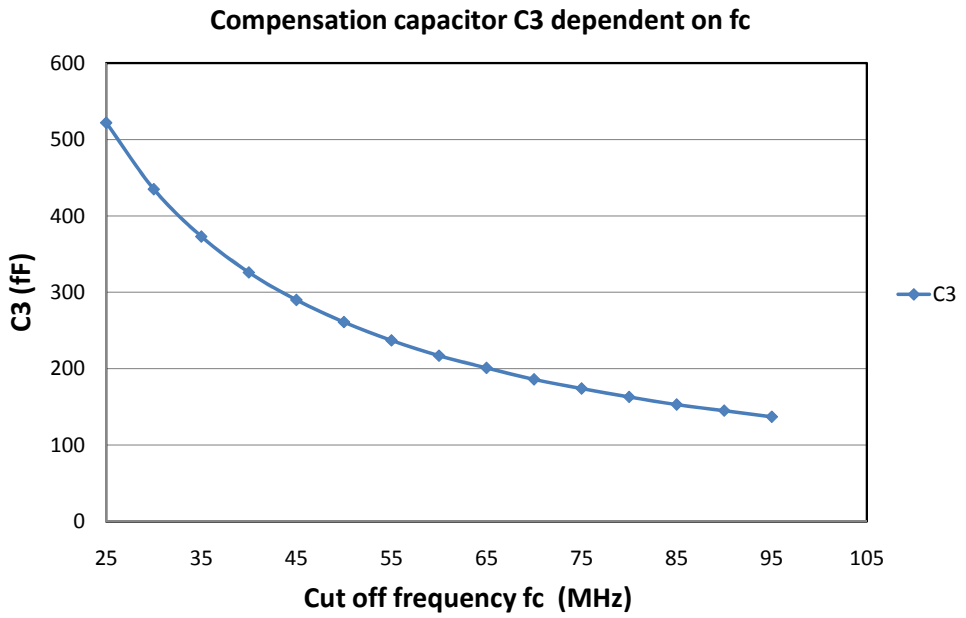

Figure 3.16: Calculation of the compensation capacitor C3 depending on the cut off frequency

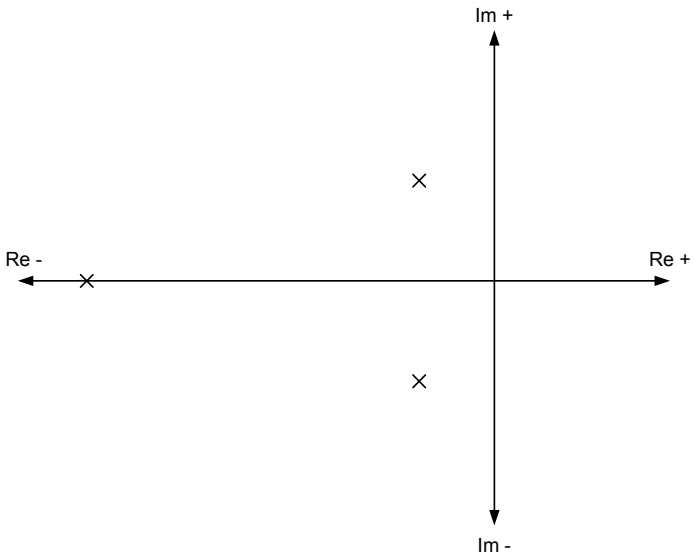

Figure 3.17: Pole zero plot of the compensated filter with 2 conjugated poles and one zero in the negative half plane

3.5.4 AGC with Tapped Resistor

A different approach to realize programmable gain and damping is the usage of a tapped resistor. In this case the feedback and input resistor is changed. There-

fore the stability of the op-amp must be large enough. The 63 gain steps are realized by using 32 resistors where the on resistance of the switches is used for averaging. From the gain characteristics it can be seen that the specific resistor has to be decreased with lower gain. The effective amount of resistors equals 63 where the first resistor of the 32 is not averaged. Therefore this LSB6 resistor was chosen on the maximum gain level where the largest gain step width occurs. Because of realizing the switches with 3.3V transistors the logic was done with 90nm standard logic. This requires 34 level-shifters, which need a lot of area. Hence for 65nm the logic was done with 3.3V transistors to decrease the area. Therefore only 7 level-shifters are necessary. The linearity is very good because of avoiding switches in the signal path.
The next equations show the calculation of the AGC resistors. R1x will be chosen and consists of R1 and Rx the whole tapped resistor.

$$R1x = R1 + Rx \tag{3.34}$$

R2 will be calculated out of R1x at the minimum gain.

$$R2 = R1x \cdot gain_{agccode(2^{bit}-1)} \tag{3.35}$$

$$Rx = \frac{R1x \cdot gain_{agccode(0)} - R2}{1 + gain_{agccode(0)}} \tag{3.36}$$

$$R1 = R1x - Rx \tag{3.37}$$

The gain characteristics can be switched easily by R3 shown in figure 3.18. First the resistor values are calculated for an input voltage of 1.5Vpp. For an input voltage of 1.8Vpp R2 divided by gainmin_{1V8} leads to Rx plus R1. Finally R3 (3.38) comes out and introduces a small damping for the input signal without influencing the maximum gain of 2. For gain matching lower than 2 LSB10 a proper resistor width must be chosen. The resistor values represent a tradeoff between matching, noise and bandwidth. The matching calculations show that the tapped poly non-silicided resistor Rx needs a width of 4um while R1, R2 can stay with 2um.

The frequency compensation for the 63 gain settings is challenging. Therefore the feedback capacitor was set directly between the output and input of the op-amp, where the switch for gain programming is also included in the feedback loop. The on resistance of this switch should be very low. This implies a large transistor which has parasitic capacitors. On the other hand a large on resistance

introduces more noise at the output shown in equation 3.39. In this case R2 and R1 include the tapped resistor Rx. The largest output noise is achieved at the maximum gain of 2.

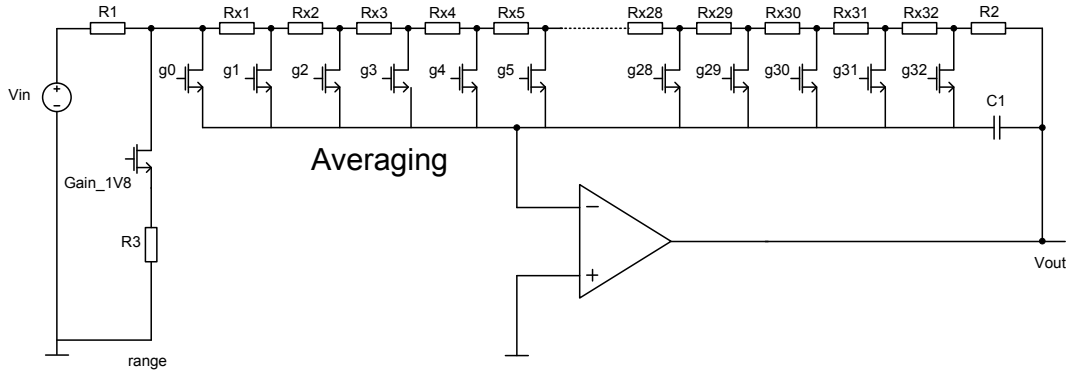

Figure 3.18: Simplified topology of the AGC with tapped resistor

$$R3 = \frac{R1_{1V5} \cdot Rx_{1V5}}{\frac{R2_{1V5}}{gainmin_{1V8}} - R1_{1V5} - Rx_{1V5}} \tag{3.38}$$

$$Vnoise_{Rsw} = \sqrt{\left| \frac{-\left(\frac{R2}{R1} + 1\right)}{s \cdot C1 \cdot \left(\frac{R2 \cdot Rsw}{R1} + Rsw + R2\right) + 1} \right|^2 \cdot 4 \cdot k \cdot T \cdot Rsw} \tag{3.39}$$

Figure 3.19 shows the noise at the output of the AGC depending on the different noise sources at gain 2. Also the gain matching was considered by calculating the absolute deviation of each resistor (3.40). The variable k comes out of the technology. By using the error propagation calculation the overall variation of the AGC gain (3.44) can be calculated. The part of the tapped resistor which is at the input of the AGC opamp Rx is considered. The same was done for the resistor in the feedback path $\mathrm{Rx}_{agccode}$. Together with R1 and R2 the gain is adjusted and the overall gain deviation is calculated. Figure 3.20 shows the deviation of the gain depending on the gain setting of the AGC. The whole pre-processing gain matching is lower than 2% for 3 sigma deviation.

$$dR1 = \frac{R1 \cdot k}{\sqrt{W1^2 \cdot 2 \cdot \frac{R1}{Rsqr}}} \tag{3.40}$$

$$dR2 = \frac{R2 \cdot k}{\sqrt{W2^2 \cdot 2 \cdot \frac{R2}{Rsqr}}} \tag{3.41}$$

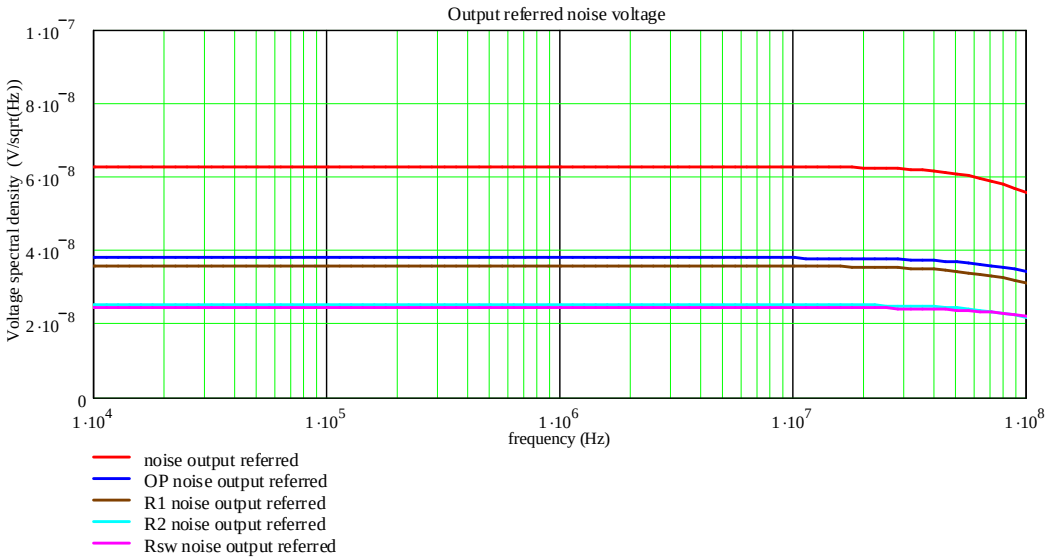

Figure 3.19: Noise of the different resistors at the output of the AGC

$$dRx_{agccode} = \frac{Rx_{agccode} \cdot k}{\sqrt{WRx^2 \cdot 2 \cdot \frac{Rx_{agccode}}{Rsqr}}} \tag{3.42}$$

$$dRxx_{agccode} = \frac{(Rx_{agccode(0)} - Rxagccode) \cdot k}{\sqrt{WRx^2 \cdot 2 \cdot \frac{(Rx_{agccode(0)} - Rxagccode)}{Rsqr}}} \tag{3.43}$$

$$dgain_{agccode} = \sqrt{\left(\frac{\sqrt{dR2^2 + dRx^2_{agccode}}}{R2 + Rx_{agccode}}\right)^2 + \left(\frac{\sqrt{dR1^2 + dRxx^2_{agccode}}}{R1 + Rx_{agccode(0)} - Rx_{agccode}}\right)^2} \tag{3.44}$$

In equation 3.44 the relative gain error is calculated. The first term shows the variation of R2 plus part of the tapped resistor which depends on agccode. The second term stands for the variation of R1 plus part of the tapped resistor. Rx has the maximum at agccode=0. In figure 3.20 the gain error depending on the agccode is displayed. The lowest one sigma gain error is achieved around gain=1 where the resistance is distributed equally on the feedback and input resistance.

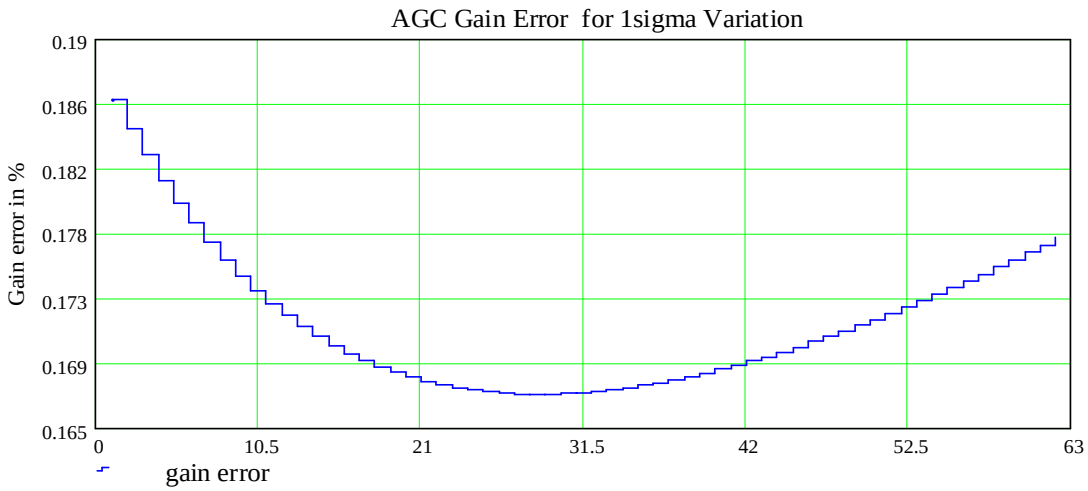

Figure 3.20: 1 sigma gain error of the AGC due to resistor mismatch for 65nm technology

3.5.5 AGC Op-Amp

The amplifier used is a folded cascode op-amp shown in Figure 3.21 with gain boosting and a continuous time common mode loop. Due to the low supply voltage of 1.1V it is not possible to use more than 4 transistors in one branch to achieve enough headroom to stay in saturation. The currents in the cascode and input branches have the same values. The GBW of the folded cascode op-amp must be around 2.3GHz to handle gain 2. Hence it does not influence the Bessel filter behavior and cut off frequency. For the lowest gainmin_{1V8} of 0.55 the stability of the differential and common mode loop (always connected in unity gain) was improved by increasing the gm of the common mode differential pair. Due to different gain settings the input common mode voltage of the op-amp can vary about 300mV. The solution was to use a NMOS differential pair at the input of the folded cascode op-amp.

The common mode voltage is used to bias a cascode which has a fixed ratio to the PMOS input of the differential amplifier. Therefore the same drain source voltage is generated for the current mirrors where the current is very exact specially for deep sub micron technologies like 65nm. Furthermore the common mode loop sees a higher load than the differential one where the bias current is in the range of the bias current for the input. The gain bandwidth GBW of the regulated cascode was calculated to be smaller than the overall GBW of the op-amp, but larger than the 3dB bandwidth of the op-amp with fixed cascodes [9]. The most critical noise sources of this op-amp are the input transistors and the current mirrors of the cascodes. For low noise requirements a standard miller

op-amp should be used. In this case a folded cascode was necessary because of the variable input common mode range.

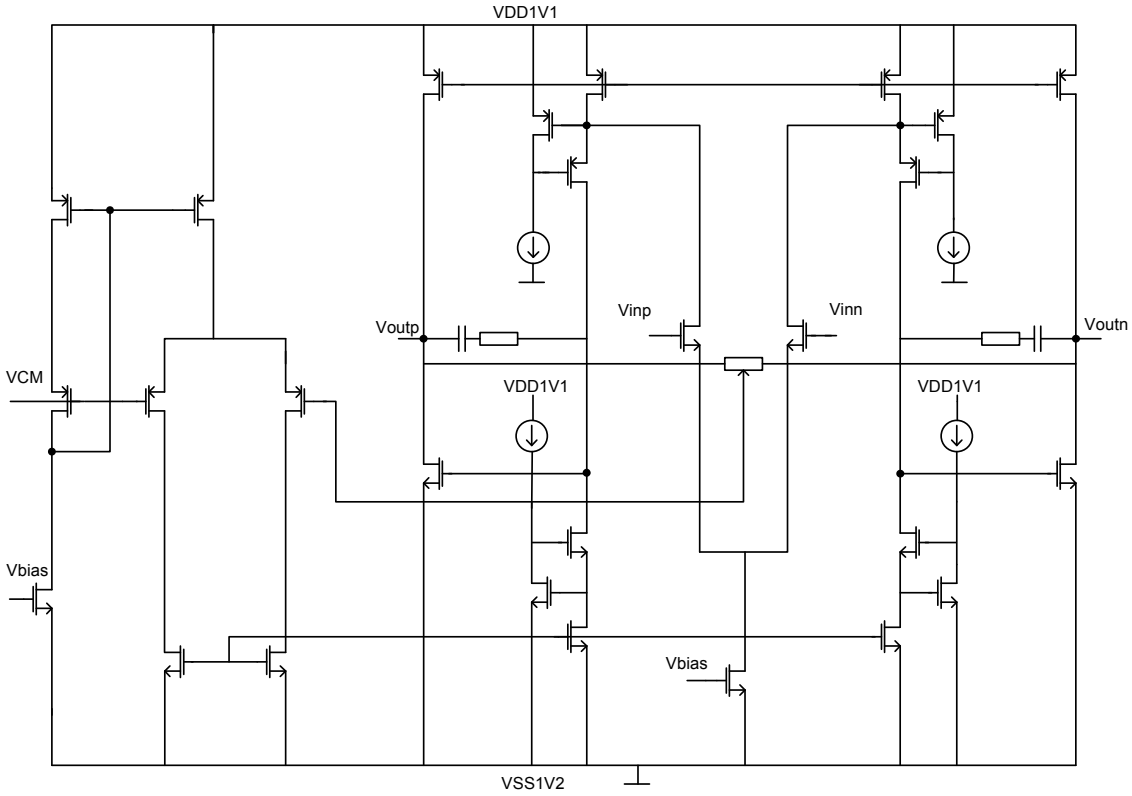

Figure 3.21: Topology of the AGC folded cascode op-amp

3.5.6 Comparison of the Different AGC Topologies

Let us compare the different types of AGCs which are considered for the different pre-processing's demonstrated in table 3.2. As mentioned before noise and linearity are a limiting factor. The power is the same because of the same used op-amp and the resistor widths were chosen to give the same area for the three topologies. It can be seen that the tapped AGC is a good trade off for matching, noise and THD. The simulations were done with 65nm process parameters. The noise was integrated from 0 to 1GHz and the power supply is about 1.1V for the 65nm design. The THD was simulated at a signal frequency of 60MHz with 1Vpp input level.

Table 3.2: Comparison of different AGC topologies

AGC	THD (dB)	Noise (μV)	Matching 90nm (%)	Matching 65nm (%)	Current (mA)	Area (μm^2)
PSW	50dB	550	0.2	0.17	5.7mA	11000
TSW	48dB	700	0.21	0.19	5.7mA	11000
Tapped	56dB	600	0.21	0.187	5.7mA	11000

3.5.7 Low Noise 2 Stage AGC plus Filter

The AGC is split up into the input stage and the 3^{rd} order Bessel filter. This was discussed in a previous section. At first glance, it seems to be very complicated but the improvement for noise and power consumption is large. Figure 3.22 illustrates the differential topology. The first part of the Bessel filter is included in the input stage. The second part is combined with the AGC. The separation has the advantage that the capacitors are smaller than for the combined filter. The gain setting for the first stage corresponds to 1 or 2 where the following AGC has to damp the signal. The capacitor at the voltage divider of the first stage is needed to stabilize the circuit for gain=2 and therefore to reduce peaking in the frequency domain.

Table 3.3 shows this connection depending on the gain setting. The very good noise performance is achieved by using the T-network AGC in the gain range with the best noise performance. This is valid for the gain setting of 0 to 39 where 6bit are necessary. The integrated noise over 1GHz of the op-amps is due to 150uV for the input stage and 200uV for the filter AGC. In practice, this is very low and hard to achieve.

Figure 3.23 demonstrates the T-network of this structure. It can be seen that the resistor values have to be changed for different gain settings. The larger resistors (Rp+Rpx) are used for gain=1 in the input stage.

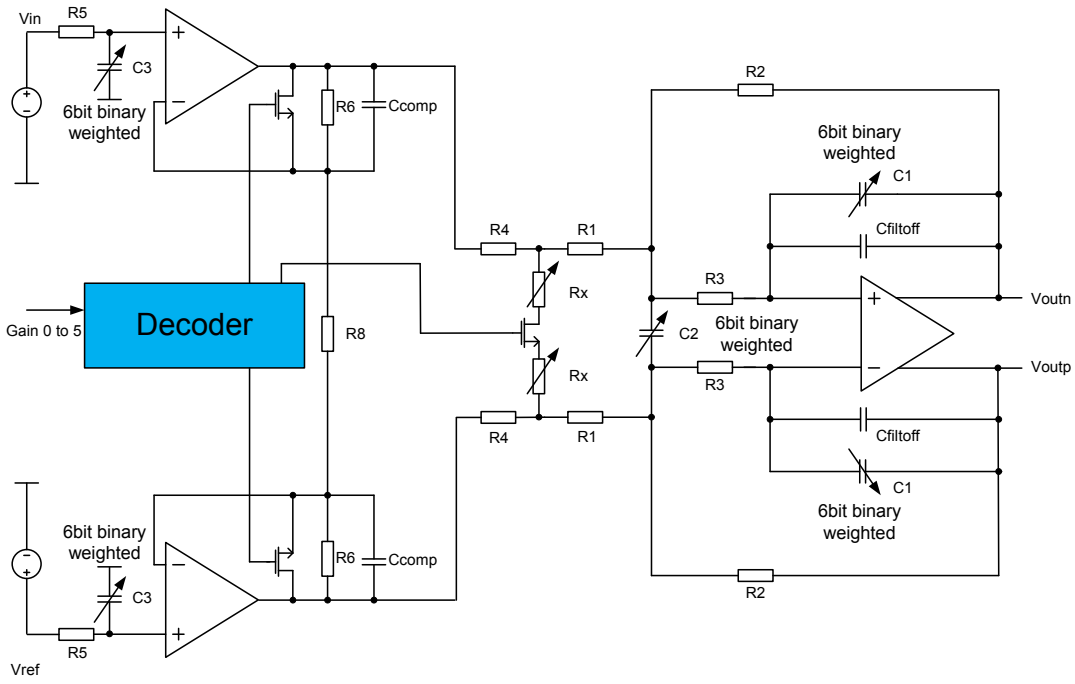

Figure 3.22: Low noise 2 stage 3^{rd} order pre-processing

Table 3.3: Gain and noise context

Input Stage	AGC code	Overall Gain	Noise int. to 1GHz (μV)	THD 60MHz (dB)
gain=2	0 to 23	2 to 1.026	422	48
gain=1	0 to 39	1 to 0.55	577	48

3.6 Bessel Filter

This filter is used to reduce aliasing and noise in front of the ADC. Also the picture quality could be affected which was applied by high end customers. Because of the processing of video pulses the group delay must be constant in the pass band. The video lines contain also a Teletext signal where the decoder is sensitive to group delay variations depending on the frequency of the filter. Hence a Bessel filter characteristic was chosen realized by an active RC filter. The requirement

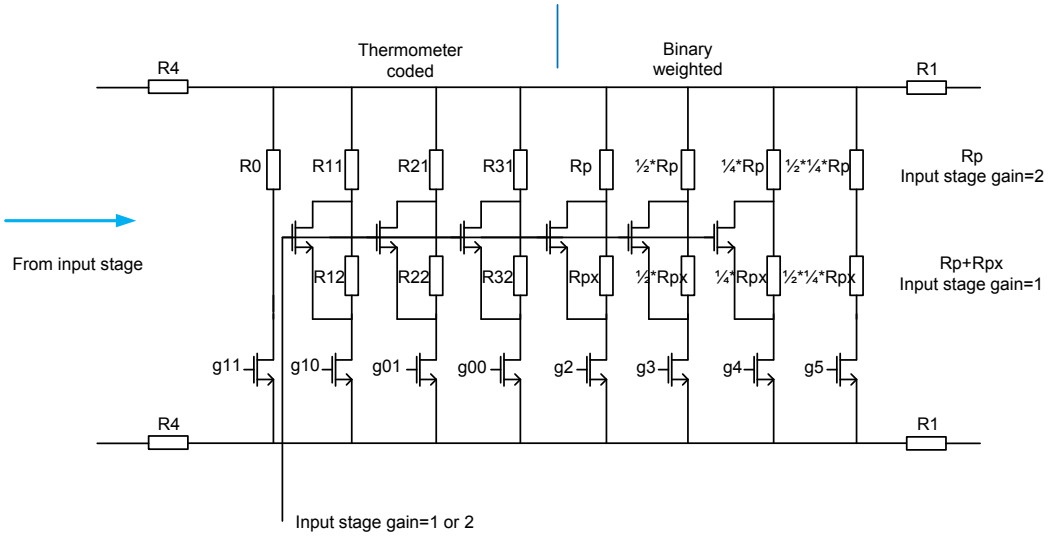

Figure 3.23: T-network of the low noise 2 stage 3^{rd} order pre-processing

is low noise, distortion, power and area. The limit for the capacitor area was the smallest possible unity cell available at the 90nm and 65nm process. The resistors were chosen small to reduce noise and parasitics. But gain matching must be fulfilled which was achieved by a resistor width larger than 1μm. The filter was designed for standard and high definition video signals which results in the difference of the corner frequency of nominal 7.5MHz and 38MHz or 76MHz. In addition to that, the slope of the filter must be high enough to suppress undesired tones. For standard video these tones are at multiples of the color carrier.

Moreover the filter in the DA converter, set-top box or DVD player are not sufficient enough. Figure 3.24 shows the difference between the different order of Bessel filter for a corner frequency of 96MHz. In figure 3.25 the group delay is compared. It can be seen that the 3^{rd} order filter is a good tradeoff between constant group delay and slope in the out of band. The lower the order the lower the group delay in the pass band which was considered for the matching with the fast blank path. The fast-blank path is used for processing the synchronization signals. The filter can be switched off to process the voltage pulses out of a graphics card adapter.
Another reason for the usage of the filter is that the ADC needs a bandwidth limiter in front of it. Because of the skipped S & H the rise and fall time has to be limited. If the filter is skipped the mismatch in the MDAC will end up with a wrong code which could not be corrected by digital correction logic. Measurements show the limitation of the rise and fall time from 2 to 3ns. But the filter will limit it even at the maximum bandwidth at the filter off mode.

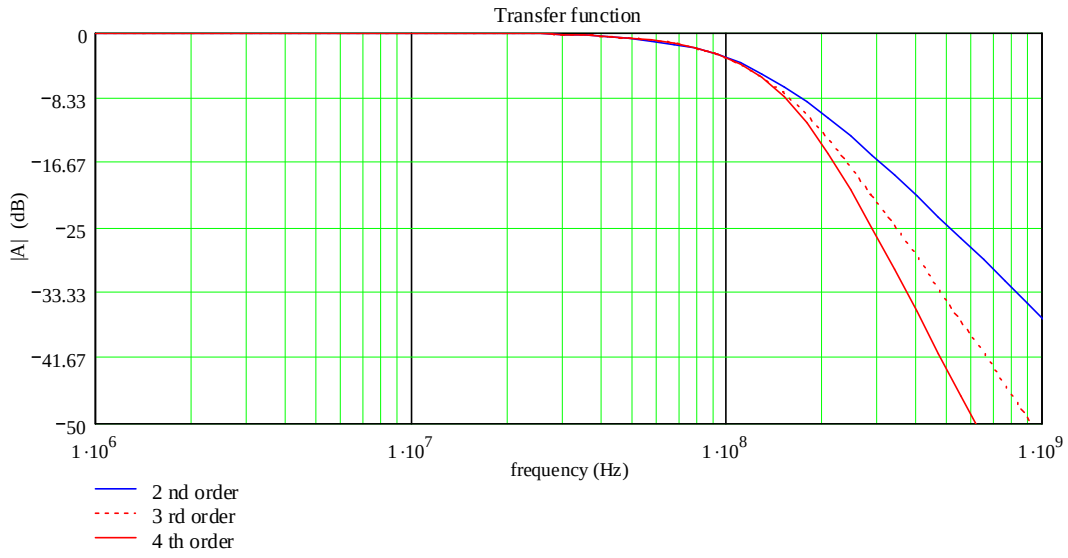

Figure 3.24: Comparison of the different Bessel filter orders for a cut off frequency of 96MHz

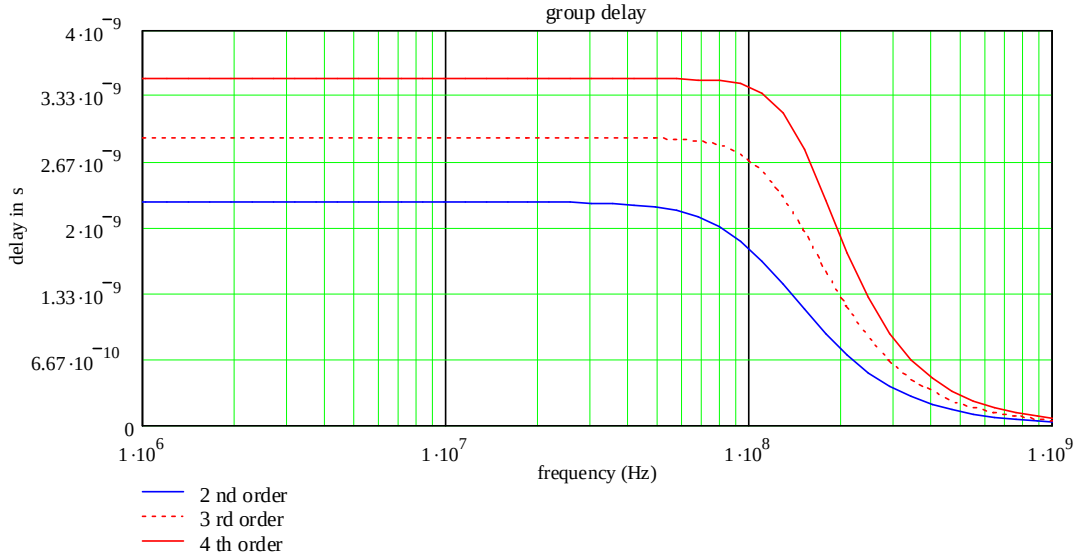

Figure 3.25: Comparison of the different group delays depending on the Bessel filter orders

3.6.1 4^{th} order Bessel Filter

The 4^{th} order Bessel filter was designed in the 90nm technology. Figure 3.26 shows the overall topology of the first and second part of the filter. This filter is used to cut the out of band noise and disturbers of the input signal. It consists of

2 stages where the first yields a cut off frequency 1.8 times larger than the overall cut off frequency. The second part has the lower cut off frequency where it is easier to design it for driving the sample capacitors of the ADC and reducing the noise. The Miller op-amp of the first Bessel stage has a unity GBW of 2.4GHz. The Bessel filter capacitors were calculated by considering the open loop gain of the op-amp. The capacitor array consists of unity MOM (metal oxide metal) capacitors which are used for binary weighted tuning. A corner frequency in the range of 30 to 78MHz can be tuned by 5% accuracy for an absolute deviation of 20% of resistors and capacitors. Moreover the group delay in the pass band is constant which is important for video signals. Furthermore a low overshoot emphasize the edges in the picture. Compared to gm-C filters the required linearity of 10 bit can be reached for 1Vpp signals at 1.2V supply. Also the area is small and limited by the capacitor accuracy.

As mentioned in the section of the AGC the resistor R3 in front of the AGC op-amp has a bad transfer function to the output of the filter. A reduction of this resistor increases the capacitor values specially C2. R3 was chosen to be in the same range from noise point of view as R2. A further reduction of R3 leads to an increase of noise because of peaking in the noise transfer function at frequencies around the filter cut off frequency. For RGB signals of a graphics adapter the filter must be switched off. RGB signals are voltage steps with a maximum bandwidth of 200MHz and a pixel frequency of 80MHz. For stability the overall Bessel filter is switched off by using only a part of C1 and C3.

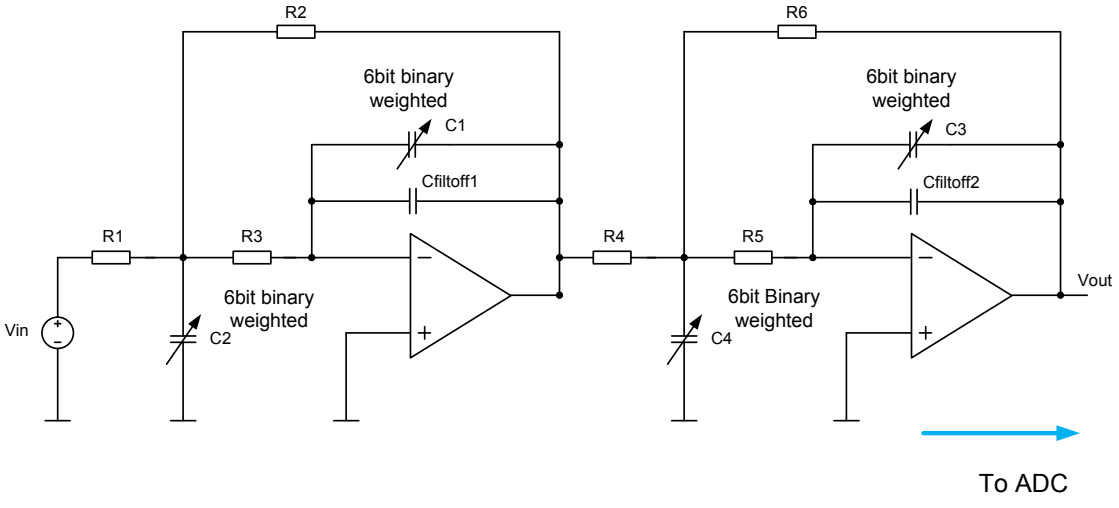

Figure 3.26: Topology of the 4^{th} order Bessel filter

The filter coefficients are shown in the following equations.

$$a14 = 1.339$$

$$b14 = 0.488$$

$$a24 = 0.774$$

$$b24 = 0.389$$

$$G(s) = \frac{1}{\left(1 + \frac{a14}{\omega g} \cdot s + \frac{b14}{\omega g^2} \cdot s^2\right) \cdot \left(1 + \frac{a24}{\omega g} \cdot s + \frac{b24}{\omega g^2} \cdot s^2\right)} \tag{3.45}$$

$$G_{ideal}(f) = -\frac{R2}{R1} \cdot \frac{1}{s(f)^2 \cdot C1 \cdot C2 \cdot R2 \cdot R3 + s(f) \cdot C1 \cdot \left(\frac{R2 \cdot R3}{R1} + R2 + R3\right) + 1} \tag{3.46}$$

The influence of the op-amp must be considered and differs for the different values of R5 and R3. The first pole of the op-amp was evaluated in 3.47. This leads to the calculation of the real coefficients and transfer function.

$$A(f) = A0 \cdot \frac{1}{1 + \frac{s(f)}{\omega p}} \tag{3.47}$$

$$k0 = \frac{R2}{R1 \cdot A(f)} + \frac{1}{A(f)} + 1 \tag{3.48}$$

$$k1 = C1 \cdot \left[\left(\frac{R2 \cdot R3}{R1}\right) \cdot \left(1 + \frac{1}{A(f)}\right) + R3 \cdot \left(1 + \frac{1}{A(f)}\right)\right] +$$

$$+ C1 \cdot \left[\left(\frac{C2 \cdot R2}{C1 \cdot A(f)}\right) + R2 \cdot \left(1 + \frac{1}{A(f)}\right)\right] \tag{3.49}$$

$$k2 = C1 \cdot C2 \cdot R2 \cdot R3 \cdot \left(1 + \frac{1}{A(f)}\right) \tag{3.50}$$

$$G_{real}(f) = -\frac{R2}{R1} \cdot \frac{1}{s(f)^2 \cdot k2 + s(f) \cdot k1 + k0} \tag{3.51}$$

Inspecting equation 3.51, the implied op-amp pole leads to a third pole in the transfer function. Hence the real and ideal poles are calculated. There exist two complex conjugated poles and one real pole in the left half plane. The complex conjugated poles must be corrected.

$$error(C2, C1) = ||IM(roots_{id})| - |IM(roots_{re})|| + ||RE(roots_{id})| - |RE(roots_{re})|| \tag{3.52}$$

Equation 3.52 shows the calculation of the error between the real and ideal poles. This was calculated for C1 and C2 where a 2-dimensional array was generated. The minimum of this array was found by a minimum search function and is illustrated in figure 3.27.

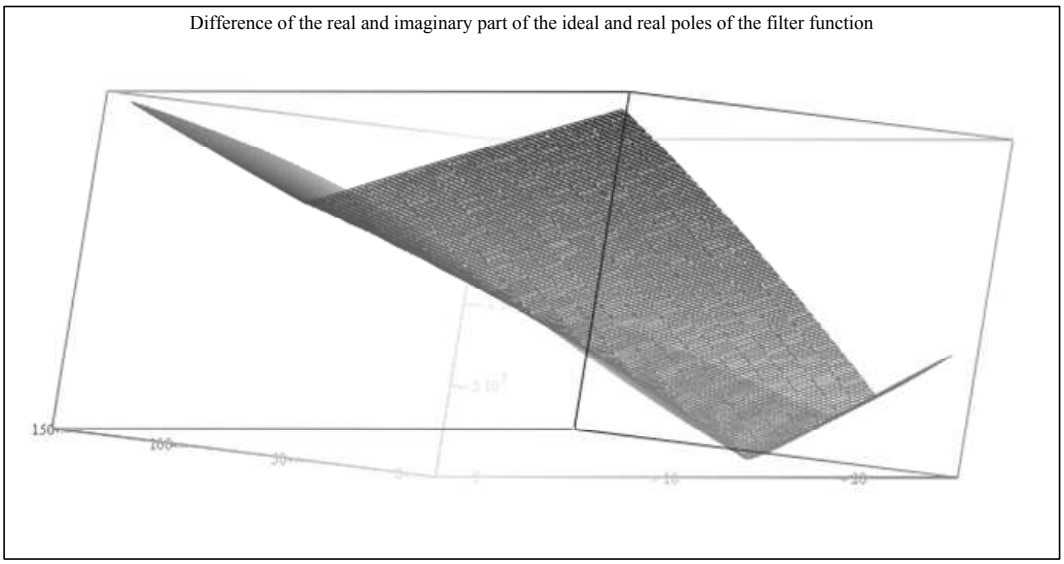

Figure 3.27: Illustration of the 3 dimensional poles error depending on C2 and C1

Figure 3.28 demonstrates this for the second part of the filter. The first part has a similar behavior. The area of the filter can be reduced if R5 is reduced. If the influence of the op-amp gets larger the variation of the cut off frequency will be increased. Moreover a low R5 introduces a peaking of the noise transfer function around the cut off frequency of the filter. Hence a tradeoff has to be found where R5 is in the range of 1500Ω for the second stage.

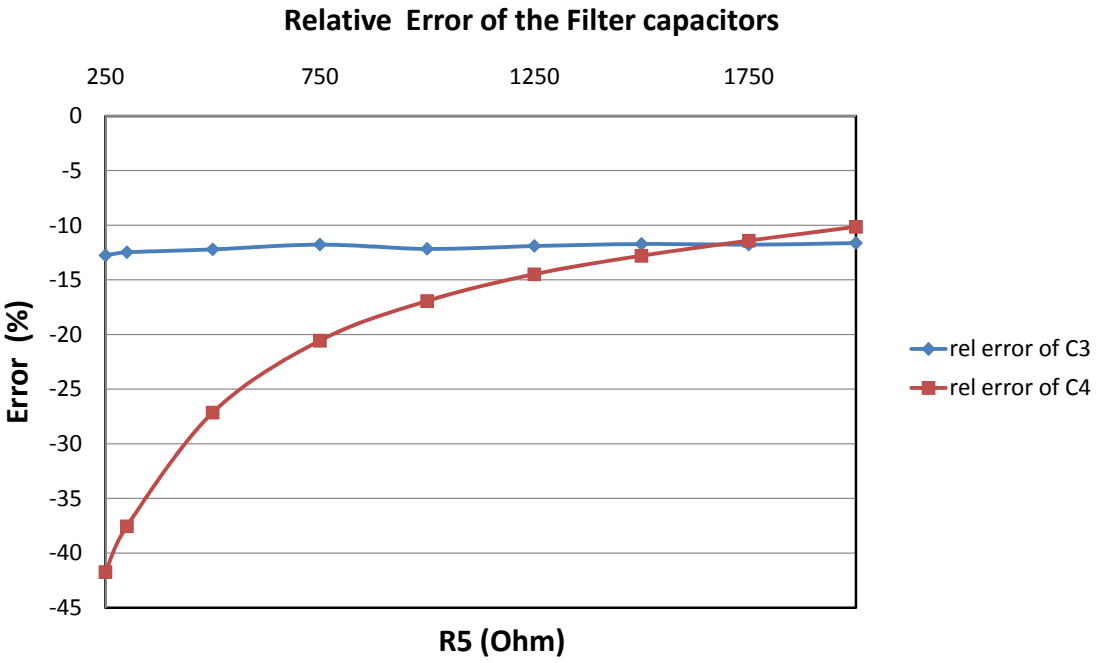

Figure 3.28: Relative error of the filter capacitors depending on R3 for correction of the op-amp

3.6.1.1 Op-Amp for the first Bessel Filter

The cut off frequency of the first part of the filter is 1.8 times of the nominal filter cut off frequency. The cut off frequency of the second part is around 0.98 times of the overall cut off frequency. This is a big advantage for the required GBW of the op-amp of the last stage to drive the ADC. Miller op-amps are used for both filters. The advantages are low power (5mA) and noise. The DC gain is larger than 50dB which is realized by cascodes at the differential pair. As mentioned before the cut off frequency of the first part is much higher than the second. This requires a very high transit frequency of 2.4GHz. Nevertheless the op-amp should not influence the filter characteristic but it will also do with very large GBW. Hence the first pole of the op-amp is considered for the filter calculation. The NMOS input transistors are calculated for a channel length of 160nm and the PMOS load channel length is in the range of 250nm.

This was necessary to reach high speed with low power. The transistor count was minimized to reduce the parasitics. The offset of the op-amps will be compensated by the clamping loop. The length of the input transistors of the common mode loop is smaller than the length of the input transistors of the input stage to reduce the gate capacitors. The slew rate must be in the range of 1.1GV/s due to the speed requirements for the PC connectivity. The current in the output

stage is 4 times larger than in the input stage to shift the non dominant pole to 3 times of the required transit frequency. Figure 3.29 shows this topology. It is a very simple but effective approach.

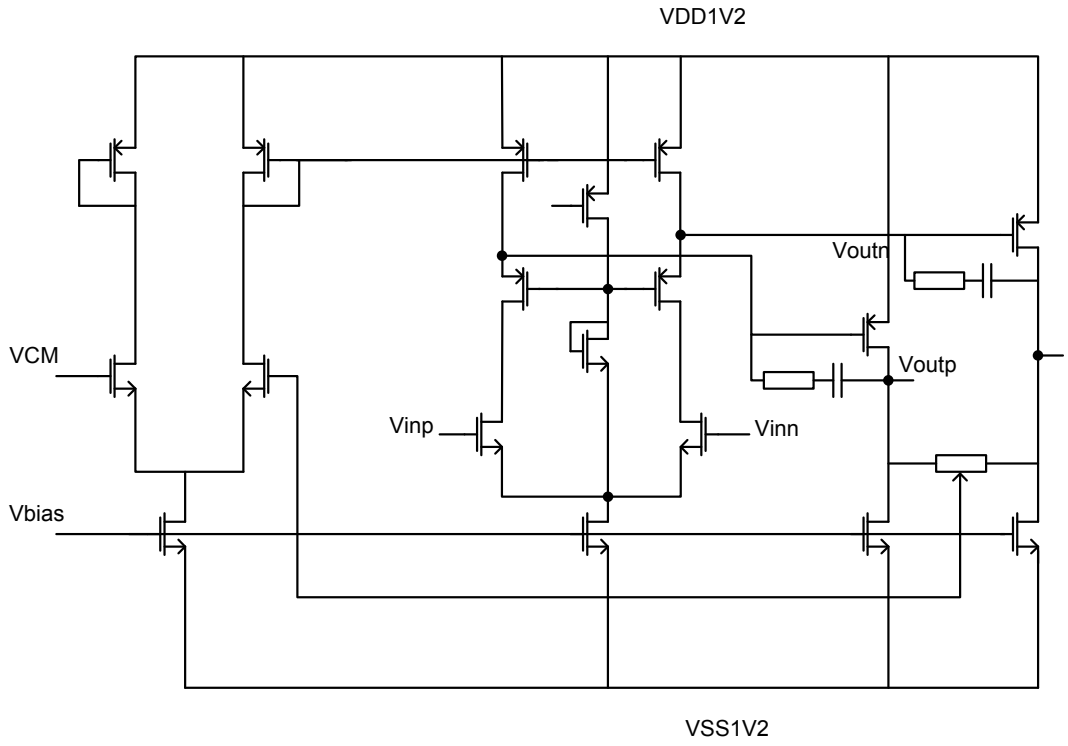

Figure 3.29: Op-amp of the first filter stage

3.6.1.2 Op-Amp for the second Bessel Filter

The op-amp of the second filter stage was designed to drive the ADC. It was laid out for a lower transit frequency because of the lower filter cut off frequency of the second filter stage. The channel length was lower than 120nm to decrease the parasitic capacitors. The transit frequency is about 1.88GHz for a supply current of 7.6mA. Figure 3.30 illustrates an additional stage for adding a shaped noise to the input of the ADC. This is needed to smooth the edges of slope in a video picture. Due to a shift register and a resistive divider shaped noise is generated and differentially added to the signal. The noise at the ADC input is in the range from sub LSB10 to 5 LSB10. This input branch has no direct feedback but is part of the overall feedback loop of the op-amp.

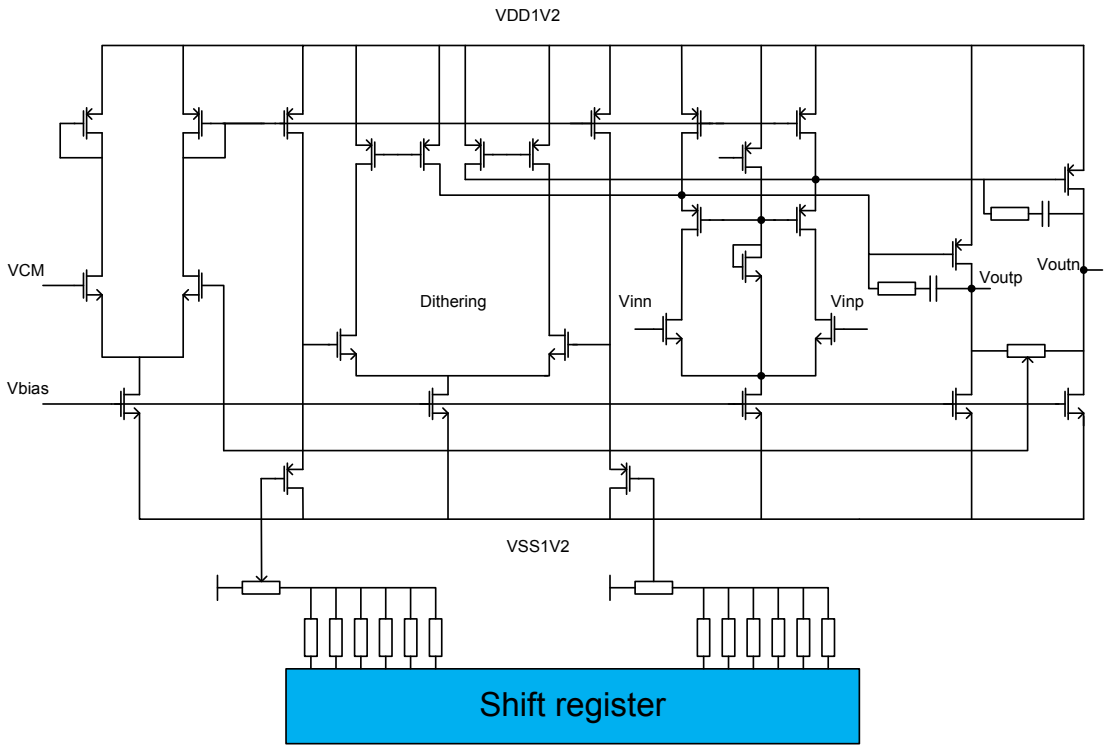

Figure 3.30: Op-amp of the second filter stage

3.6.2 3^{rd} order Bessel Filter

As mentioned in section 3.6 the attenuation of the 4^{th} and 3^{rd} order Bessel filter is different. From system point of view the attenuation of the 3^{rd} order approach can be accepted. For SD video the damping of the harmonics of the color carrier must be large enough. For HD video aliasing should not occur. The advantage compared to the 4^{th} order approach is that the power consumption is lower. The area of this filter is in the same range as for the 4^{th} order filter. The reason is the larger capacitors which are needed by the combined filter structure shown in figure 3.31. The cut off frequency of the passive part of the filter is about 1.323 times larger than the overall cut off frequency. The active part acts at a cut off frequency which is 1.414 times larger than the nominal frequency. This requires an op-amp which must have a larger transit frequency than the second op-amp of the 4^{th} order design.

The filter coefficients are shown in the following equations.

$$a13 = 0.75$$

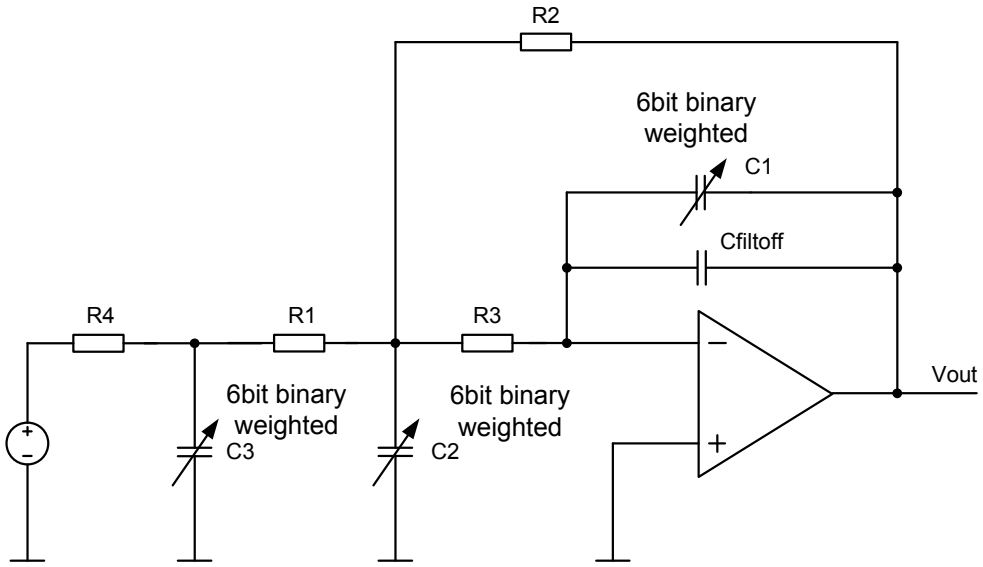

Figure 3.31: Combined topology of the 3^{rd} order Bessel filter

$$b14 = 0$$

$$a23 = 0.999$$

$$b23 = 0.477$$

For the combined topology the coefficients must be calculated.

$$a1 = a23 + a13$$

$$b1 = b23 + a13 * a23$$

$$c1 = a13 \cdot b23$$

$$G(s) = \frac{1}{\left(1 + \frac{a1}{\omega g} \cdot s + \frac{b1}{\omega g^2} \cdot s^2 + \frac{c1}{\omega g^3} \cdot s^3\right)} \tag{3.53}$$

For power saving in the 65nm technology the op-amp is designed for a feedback factor of 0.5. Therefore the stability is ensured for the 6dB point in the open loop analyses. There the current consumption equals 7.6mA at 1.1V supply. The transit frequency at 6dB corresponds to 1.48GHz. Of course this is very fast but needed for this type of filter. This filter structure uses the same type of op-amp as the 4^{th} order filter. The minimum channel length is about 120nm to reduce the parasitic capacitors which are increased with a thinner gate oxide at DSM technologies. Also care was taken on the current mirrors to have similar drain source voltages to avoid mirroring errors. The drain and gate leakage currents were also considered by the simulation.

3.6.3 Filter Calibration

The cut off frequency can vary depending on the resistor and capacitor process deviation by more than +/- 20%. This influences the picture quality specially for HDTV signals, where the filter is used for anti aliasing. The issue was to determine the R and C deviation by measuring the charge up time of an RC network with a precise time reference. The RC time constant can be evaluated by using an RC low pass which will be charged and discharged periodically. The time for charging to a defined value can be measured and compared to a reference value. The drawback is that the charging time is dependent on the voltage supply. This can be solved by two low pass networks where one is charged from VDD and the other from VSS shown in figure 3.32. Therefore the evaluation is nearly independent from the supply. The crossing of the two curves is used for measuring the time constant. Then the capacitors are discharged and charged again which is done several times to get an averaging effect and therefore an increasing of the accuracy.

This behavior can be modeled by the equalized equations of the charge up and down curves. The intersection of both charging curves is calculated by the following equations.

$$(V_{up} - VSS) \cdot e^{-\frac{tcross}{\tau}} + VSS = (VDD - V_{down}) \cdot \left(1 - e^{-\frac{tcross}{\tau}}\right) + V_{down} \tag{3.54}$$

$$tcross = \tau \cdot ln\left(1 + \frac{V_{up} - V_{down}}{VDD - VSS}\right) \cong \tau \cdot ln2 \tag{3.55}$$

In practice VDD - VSS do not correspond perfectly Vup - Vdown due to charge

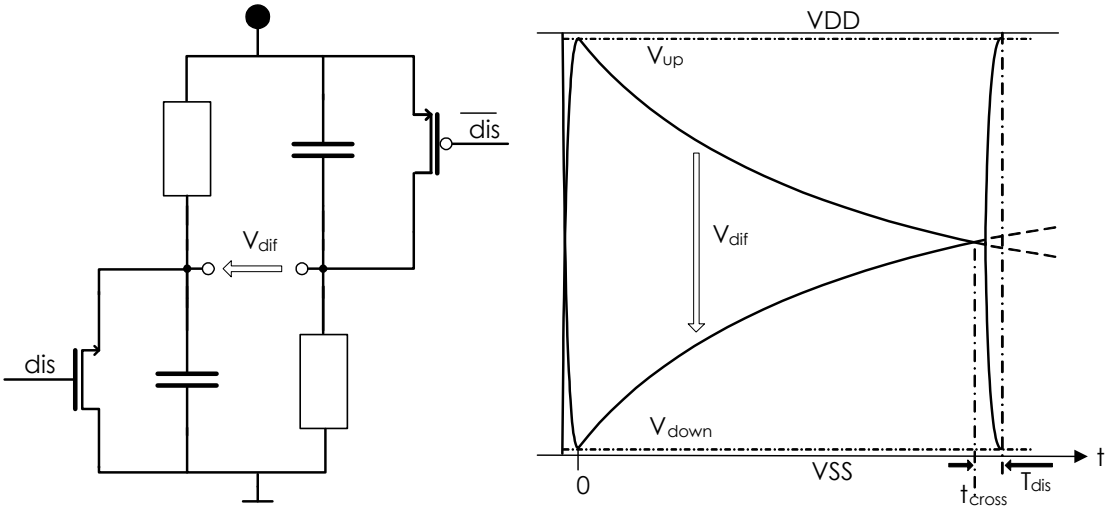

Figure 3.32: Calibration principle

injection or incomplete discharging.

$$V_{up} = VDD - dV$$

$$V_{down} = VSS + dV$$

$$tcross = \tau \cdot ln\left(2 - \frac{2 \cdot dV}{VDD - VSS}\right) \tag{3.56}$$

The offset dV does not represent a problem if it is much smaller than VDD-VSS. The discharge time can also be evaluated where the relation between the discharge time and tcross is 32. The discharge time can vary by +/- 20% which is represented by ktol. Ktol is influenced by the on resistance of the switch and the supply variation. The intersection is detected by an offset compensated comparator where the crossings are counted. The resolution of the counter corresponds to 12bit and for nominal conditions the counter stops at 1024 (n=10bit).

$$tdis = ktol \cdot ln2 \cdot 2^{-5} \tag{3.57}$$

The clock frequency is 4 times larger than the frequency of the relaxation oscillator where the oscillator clock will be related on the system clock (3.58).

$$Tclk_{norm} = \frac{Tclk}{Rnom \cdot Cnom} \tag{3.58}$$

$$stopvalue = 2^n \cdot \frac{tcross + tdis}{Tclk} \tag{3.59}$$

$$cross_{cnt} = stopvalue \cdot \frac{Tclk_{norm}}{tcross + tdis} \tag{3.60}$$

Inspecting equation 3.59 the maximum counter stop value is calculated. This was done with the nominal R and C values. A deviation of RC results in a variation of the cross count parameter. It can be seen that a variation of ktol has less influence on the counter value shown in figure 3.33. The maximum stop value is stored and compared to the real counter value which depends on the technology deviation of R and C. In equation 3.60 the sum of the crossings during the counting phase are demonstrated. There the charge and discharge time is also normalized on τ (RC).

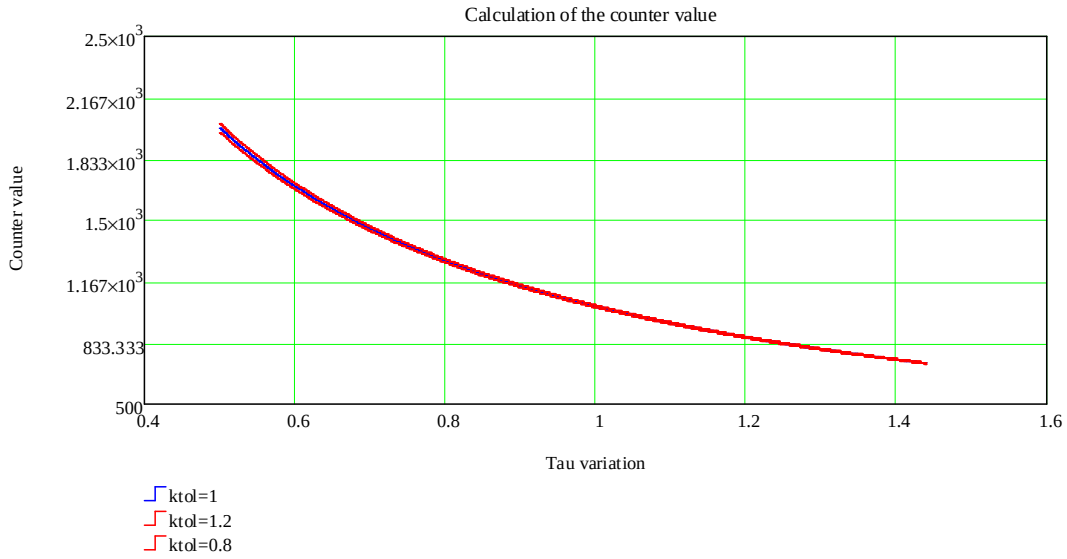

Figure 3.33: Calculation of the counter value depending on the RC deviation

Next the correction value will be calculated where the minimum capacitor C0 and the LSB capacitor dC are normalized. Figure 3.34 shows the correction value RC_{adjust} depending on the variation of τ at the minimum correctable cut off frequency of 31.6MHz. This corresponds to a nominal fcode of 7. A τ of 1.4 cannot be corrected anymore because the subtracted code is larger than 7. Hence the corner frequency error is increased. For an allowed cut off frequency error of +/- 5% the maximum cut off frequency is about 82MHz related to a τ variation

of +/- 20%.

$$RC_{adjust} = \left(\frac{cross_{cnt}}{2^n} - 1\right) \cdot \left(\frac{C0}{dC} + 31 - fcode\right) \tag{3.61}$$

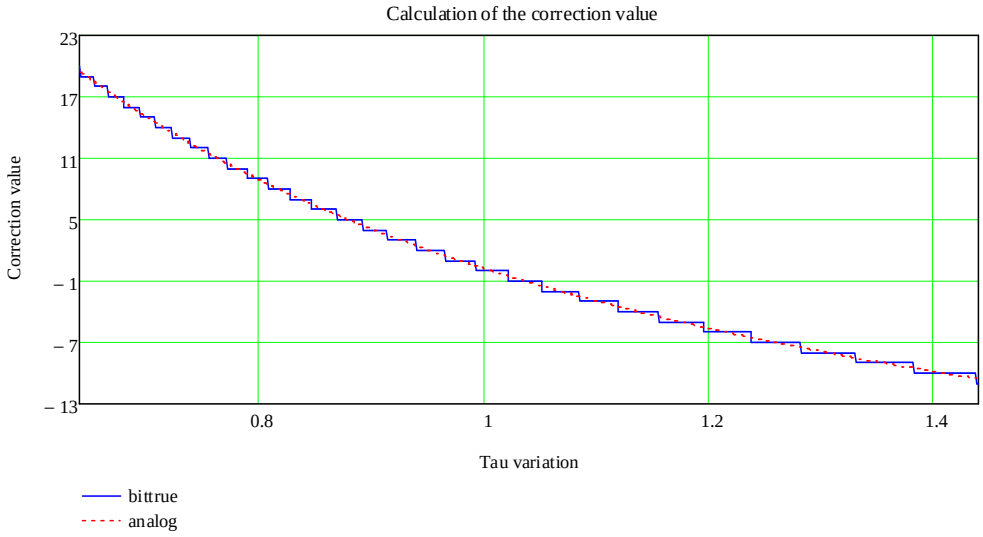

Figure 3.34: Calculation of the correction value depending on the RC deviation at fcode 7

$$C_{trim} = C0 \cdot dC \cdot (31 - fcode) \tag{3.62}$$

Equation 3.62 demonstrates the calculation of the trim capacitor where the code has to be subtracted because the lowest overall capacitor value yields the maximum cut off frequency.

$$f_{ideal} = \frac{96MHz}{R0 \cdot (C0 + C_{trim})} \tag{3.63}$$

The ideal cut off frequency of the 5bit (6bit with filter off) 4^{th}order Bessel filter can be calculated which is illustrated in figure 3.35. The capacitors are chosen to fulfill the accuracy of +/- 5% for 38 and 76MHz. The RC_{adjust} parameter is taken to correct the cut off frequency.

$$fcode_{new} = RC_{adjust} + 31 - fcode \tag{3.64}$$

$$Ccorr = C0 \cdot dC \cdot fcode_{new} \tag{3.65}$$

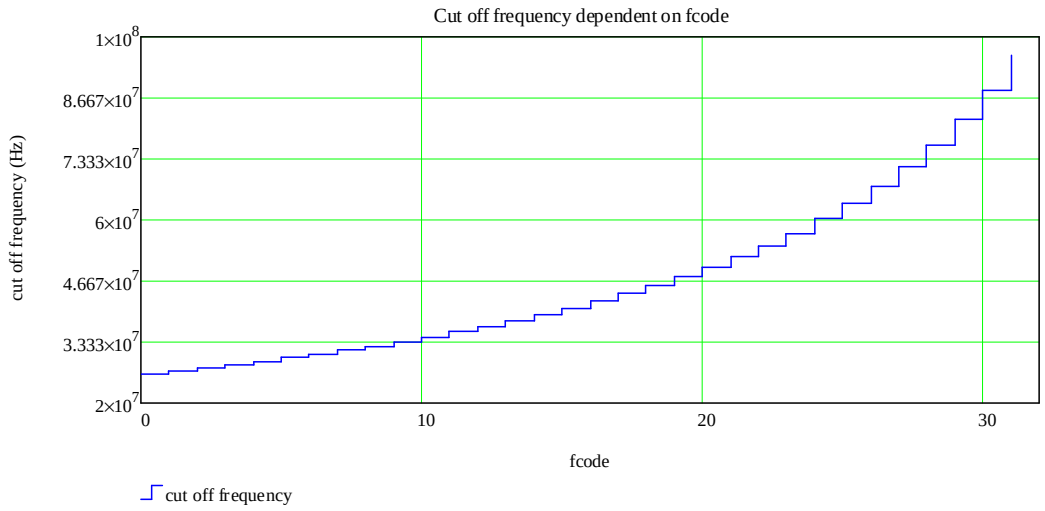

Figure 3.35: Cut off frequency of the 5bit capacitor array depending on fcode

$$fcorr = \frac{1}{R0 \cdot (C0 + Ccorr) \cdot \tau} \tag{3.66}$$

The corrected cut off frequency is calculated in equation 3.66. In figures 3.36 and 3.37 the relative cut off frequency error is illustrated for 38 and 76MHz depending on the process variation of R and C.

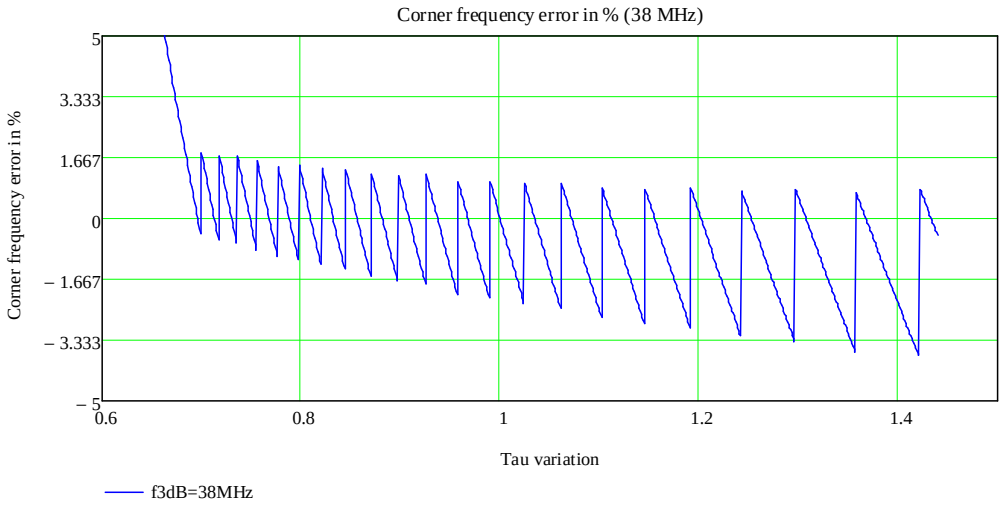

Figure 3.36: Cut off frequency error depending on the RC deviation at fc=38MHz

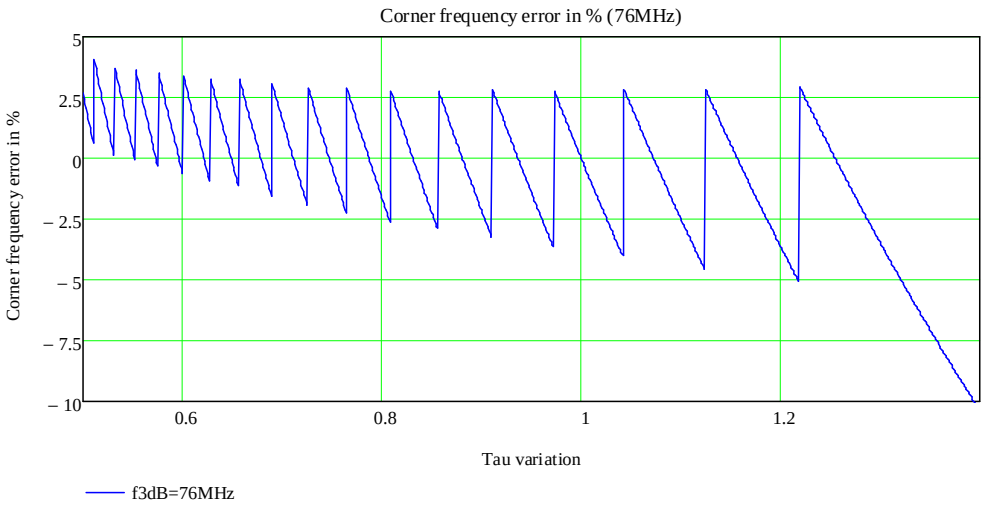

Figure 3.37: Cut off frequency error depending on the RC deviation at fc=76MHz

This very nice technique was developed by Achim Bauer [10]. He was responsible for the algorithm, the digital implementation and the analog comparator. I did the analog system analyses and filter implementation. Moreover the accuracy analyses of the cut off frequencies and the on chip integration were done by me.

3.7 Experimental Results

The measurement results were taken from a 90nm shuttle were the pre-processing and a 90nm pipeline ADC was manufactured. Some additional data was got from the productive analog video frontend which comprises 8 analog channels.

3.7.1 90nm Pre-Processing

The pre-processing is used in a noisy system environment, disturbed by digital processing and crosstalk from digital output pads, the power supply rejection (PSR) of the proposed video frontend must be large. High PSR is reached by using cascodes. Insulation and distance to adjacent noisy digital modules reduces the disturbance on the analog blocks. Two channels of pre-processing plus ADC were fabricated in a standard digital 90nm CMOS process and encapsulated in a QFP100 package where the digital outputs are close to the analog inputs but orthogonal. Two double bonded supplies were used for the 2.5V ADC outputs. The bias current and reference voltages are externally supplied. The layout of the two measured channels can be seen in figure 3.38. The two input stages are directly connected to the pads followed by the AGC and the two Bessel filters.

On top of the pre-processing the dithering block is placed.

The effect of pseudo differential inputs can be seen in figure 3.39. The crosstalk between the two channels was investigated. In single ended the crosstalk specification was violated for high signal frequencies. The suppression of the crosstalk from the aggressor pre-processing2 was improved from 5dB at 20MHz to 10 dB at 70MHz. This was measured at the output of ADC1. Most of the crosstalk occurs at the input pins (package) and PCB (printed circuit board).

The 10bit ADC is always used to measure the pre-processing. Its performance is included but the overall performance is dominated by the pre-processing. Also a step response with a rise time of 2ns and a plateau phase of 3ns is shown in figure 3.40 and can be compared to the specified step response shown in figure 3.41. This is used for filter off RGB application.

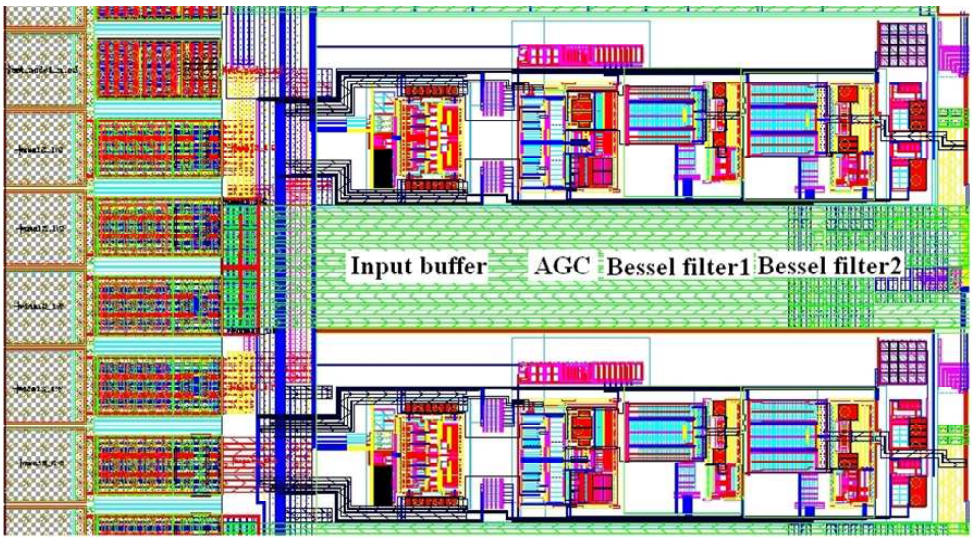

Figure 3.38: Layout of the two pre-processing's of the 90nm test-chip

At filter off mode the center of the plateau phase will be sampled to get the correct value of the pixel. This is done by a gradient detection circuit which yields the information of the edges and plateaus [11].

The power consumption of 40mW @ 165MS/s ADC sample rate was achieved by optimizing resistor and capacitor sizes at the low power mode. There the bias current is reduced by 30%. The performance degradation can be neglected. The limitation for the filter design was the smallest unity capacitor layout cell of the 90nm process and the parasitic capacitors. They should not dominate the cut off frequency of the filter. The SNDR corresponds to 54dB at a filter cut off fre-

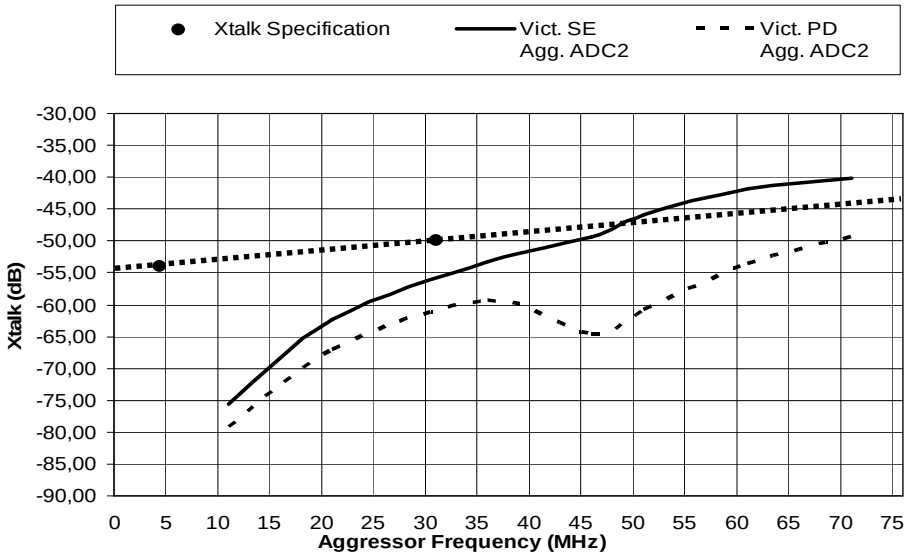

Figure 3.39: Crosstalk from pre-processing2 to ADC1 with and without pseudo differential input

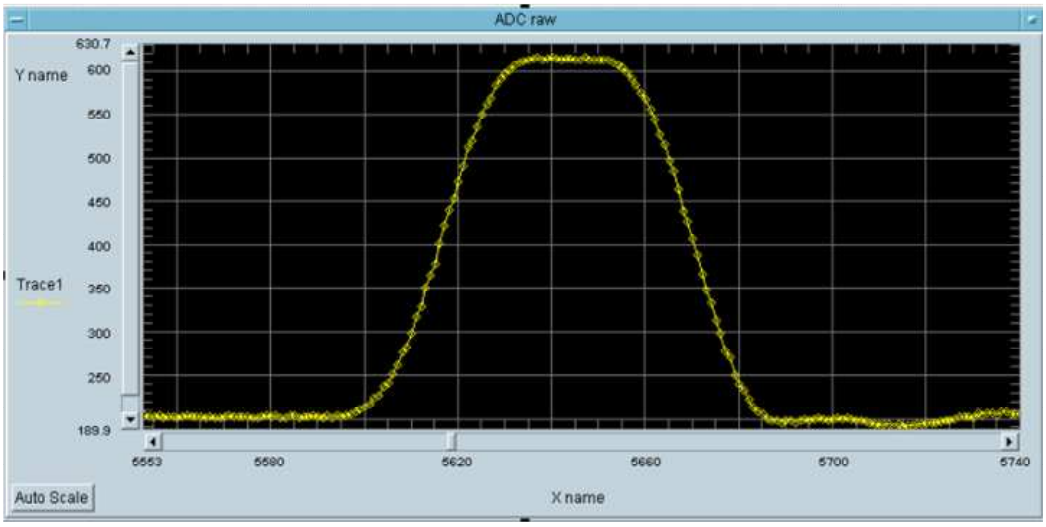

Figure 3.40: Step response of the pre-processing measured with a beat frequency test

quency of 26MHz and 46dB at 75MHz input frequency and a pre-processing cut off frequency of 200MHz shown in figure 3.42. The proposed pre-processing has been implemented in a 90nm standard digital CMOS process with an active area of 0.059mm^2. The area of the ADC corresponds to 0.15mm^2 and the power equals

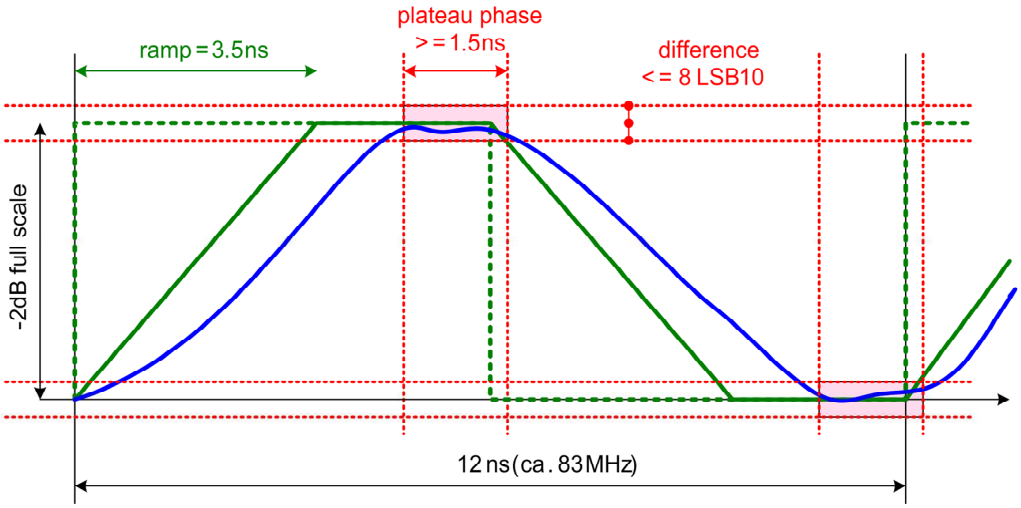

Figure 3.41: Specification of the step response for the filter off mode

56mW. The THD was also investigated for different input signal frequencies and depends on the filter programming. The filter off mode is the most critical mode as well for noise as for linearity shown in figure 3.43.

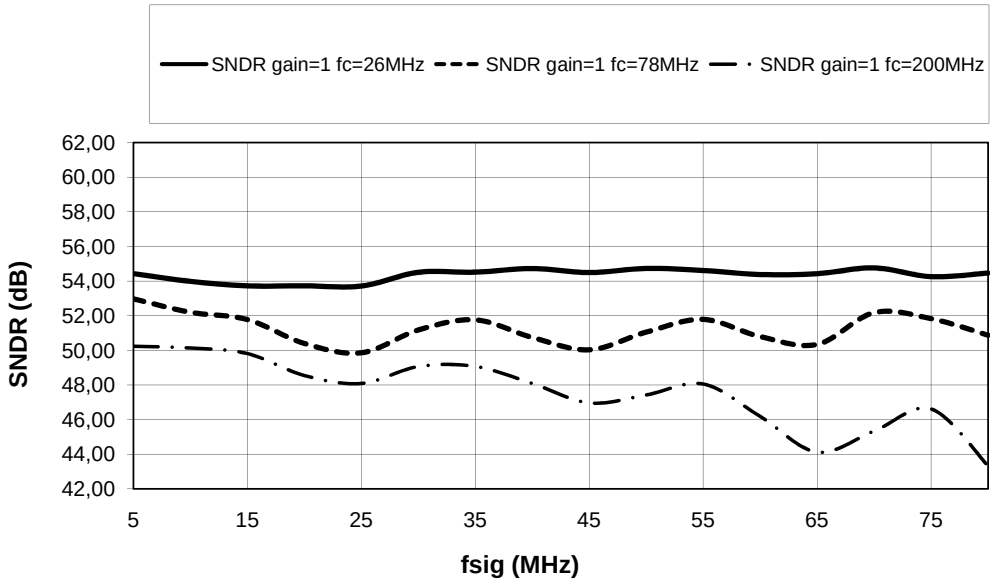

Figure 3.42: SNDR of the pre-processing at fstrobe=165MHz depending on the signal frequency

Moreover the gain matching of the pre-processing was evaluated. The test-shuttle pre-processing provides a differential input where a static DC voltage of

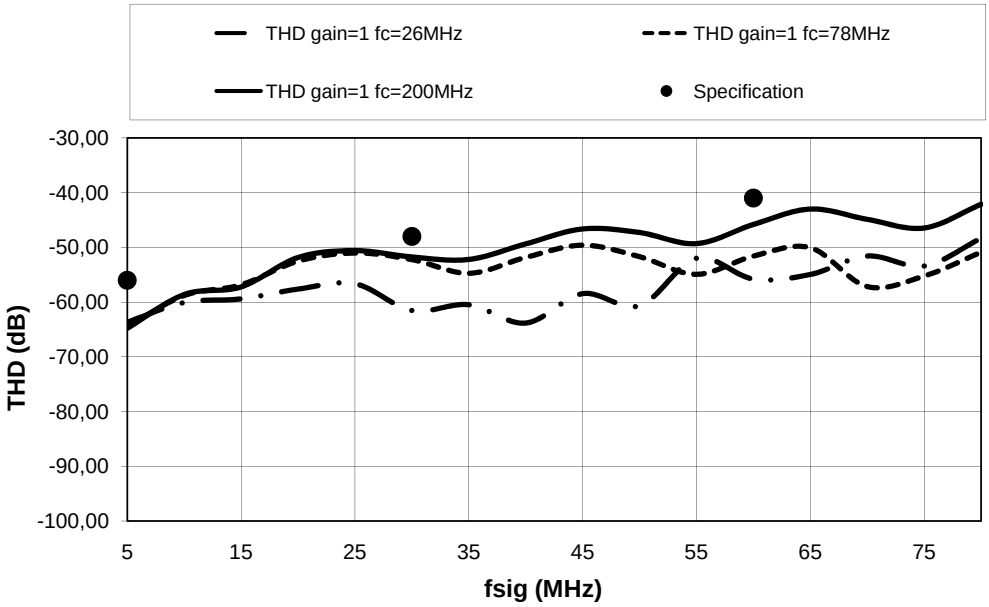

Figure 3.43: THD of the pre-processing at fstrobe=165MHz depending on the signal frequency

around 1 to 1.2V was applied. In addition to that the differential output was analyzed and hence the gain matching calculated.

$$gain_{error} = \frac{Vout1 - Vout2}{Vin1 - Vin2} \tag{3.67}$$

The measurement of the gain error was done with 19 samples to get a rough statistic sigma value for the standard deviation of two adjacent pre-processing circuits. The matching is in reality bad compared to the model where the op-amps and the input stage is neglected.
Table 3.4 shows a comparison of a two channel gain matching of the measured test-shuttle and the model.

3.7.2 65nm Pre-Processing

The 65nm pre-processing consists of only the filter buffer which is employed in inverting configuration. The very low resistors of 1kΩ are used to decrease the noise at the input of the 65nm pipeline ADC. This was necessary to measure only the ADC and not the filter buffer. The filter op-amp was designed for a feedback factor of 0.5 to save power and area. A feedback capacitor is needed to limit the bandwidth to 400MHz. This noise optimized circuit was needed to avoid any influence on the measurement of the pipeline ADC.

Table 3.4: Gain error of 90nm test-shuttle and model

2 channel gain matching	gain=0.55 (%)	gain=1 (%)	gain=2 (%)
σ gain error test-shuttle	0.55	0.56	0.72
σ gain error model	0.28	0.26	0.3

In figure 3.44 the layout of this filter op-amp is illustrated. The pipeline ADC is attached at the top of the filter where the digital outputs are far away from the analog inputs to minimize digital crosstalk. The SNDR of the ADC plus the filter corresponds to 56.5dB at 5MHz and 50 dB at 85MHz at a strobe frequency of 130MHz. This will be explained in more detail in the 65nm pipeline ADC chapter.

The simulation results for the overall 3^{rd} order pre-processing are about 64dB THD for a 6MHz 0.8Vpp and 45.5dB THD for a 60MHz 0.8Vpp input signal. These simulations were done at process option slow, temperature 130° and at a supply of 1V.

Table 3.5 shows a comparison of the noise simulations of the 65nm and the 90nm pre-processing. At filter off mode the SNR is 2dB better than the 90nm pre-processing. Moreover the lowest (27MHz), highest (96MHz) and filter off (200MHz) cut off frequencies are simulated depending on the process corners. It can be seen in figure 3.45 that the variation of the cut off frequency at filter off is much larger than for the lower cut off frequencies. This is influenced by the limited GBW of the op-amp at larger filter bandwidth. The rise time was also simulated at different filter cut off frequencies, gain settings and process corners. This was done for a small signal to see no slewing behavior. Figure 3.46 illustrates the step response for the 3^{rd} order Bessel filter where the typical slight overshoot is visible.

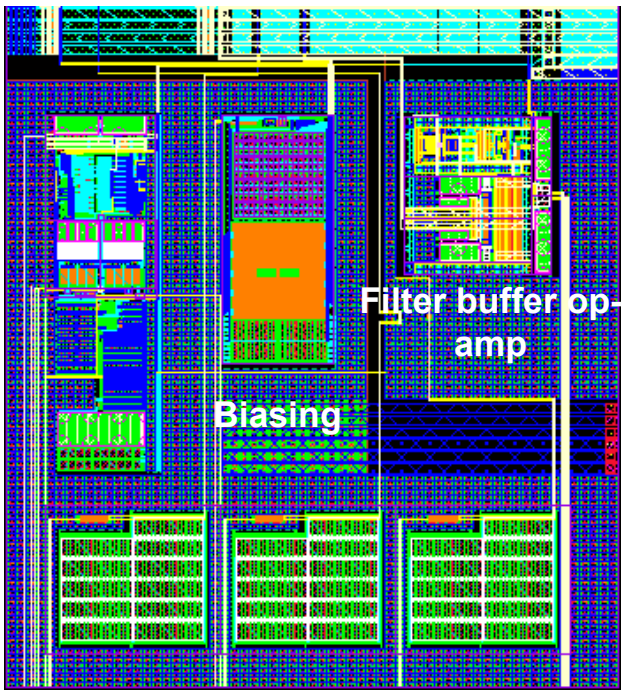

Figure 3.44: Layout of the filter buffer of the 65nm test-chip

Table 3.5: Comparison of the noise performance of the 65nm and 90nm pre-processing

	SNR(dB) fc=27MHz	SNR(dB) fc=96MHz	SNR(dB) fc=200MHz
65nm gain=1	59	54.6	53.4
90nm gain=1	59.5	54.5	51.5
65nm gain=2	57.6	53.4	52
90nm gain=2	58.4	53.4	50.7

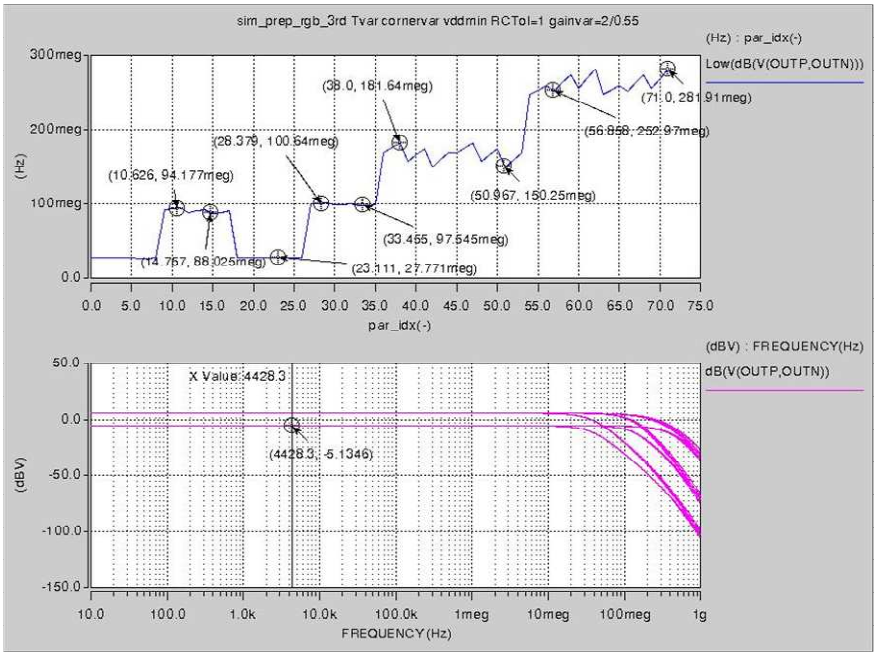

Figure 3.45: Variation of the cut off frequencies depending on the process corner

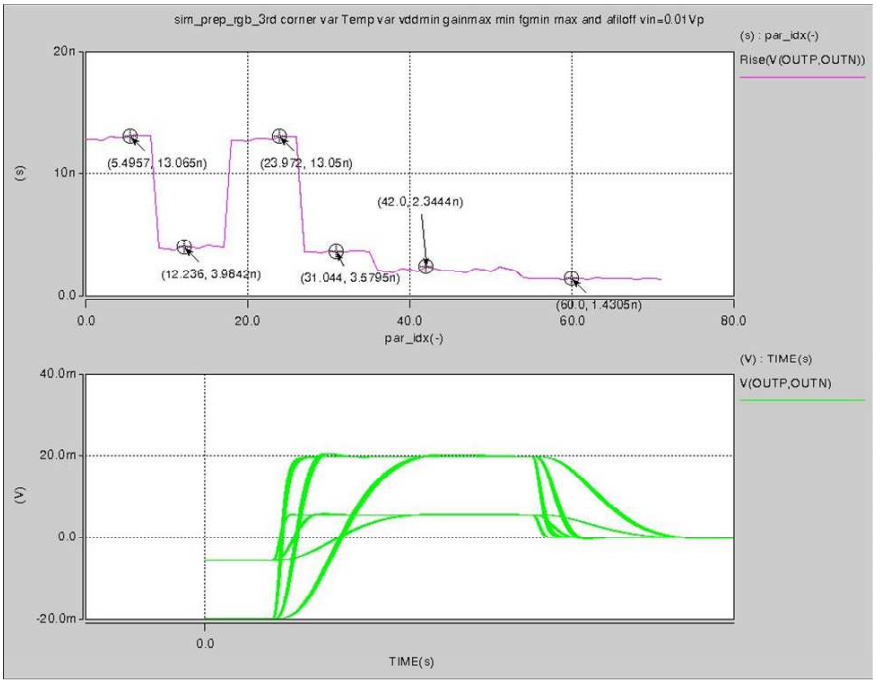

Figure 3.46: Rise time depending on the filter settings and process corners

3.8 Summary of Chapter 3

In this chapter 4 different pre-processing topologies were investigated. These structures differ in the amount of stages, THD, SNR, matching, power and area. As can be concluded in table 3.6 the 4^{th} order pre-processing has much higher linearity compared to the Sallen-Key structure. This is because of the positive feedback of the Sallen-Key topology. The noise is similar and the matching is slightly better of the Sallen-Key topology. Due to 3 stages used by the Sallen-Key pre-processing the power is decreased by 7mW. Nevertheless the area is larger because of the single ended dual capacitor arrays at the input-stage. The differential approach would half the capacitor size but limits the filter behavior because the input signal is related to ground.

The input-stage uses a single ended folded cascode class AB op-amp which yields the required linearity at input signals of 80MHz and 1.8Vpp. Two input stages are used for a pseudo differential amplification of the input signal. Hence a disturber can be eliminated and the signal to noise ratio is improved. Moreover three different types of AGCs are investigated where the tapped structure has the best performance and enables the opportunity to switch the gain characteristic with only one additional resistor [12]. A comparable solution was not found in the literature. The AGC with the T-network at the input is a compromise regarding noise and linearity but has the advantage of combining it with a 2^{nd} order filter which is a part of a 4^{th} or 3^{rd} order Bessel filter. The best noise performance can be achieved by splitting up the AGC on the input-stage and the combined AGC-Filter. With this structure a 3^{rd} order Bessel filter can be realized.

The 4^{th} order pre-processing was done in the 90nm technology with an SNR of 54.5dB and a THD of 52dB for a 30MHz 1Vpp signal at a filter cut off frequency of 78MHz. The power consumption is about 47.5mW for the regular power mode. In the low power mode it is reduced to 40mW at nearly the same performance. The filter can be switched off where the overall cut off frequency of 200MHz is determined by the feedback capacitor. This so called filter off mode is needed for the connection of RGB signals of a graphic card. There a plateau phase of minimum 2ns must be fulfilled. In contrast the biquad structure needs two more op-amps.

The noise on the flat screen was visible with the 90nm chip specially at the filter off mode but accepted by the customer. Therefore the 65nm pre-processing has to be improved concerning noise. Also power and area has to be reduced. That is why a 3^{rd} order Bessel filter and an extra AGC were taken. The performance of the 3 stage solution is better and the risk lower to follow this approach. The 2 stage topology can be used for the SD path where a lower bandwidth is required. The noise integrated from 0 to 1GHz is about 53.3dB for gain=1 and

filter off (200MHz). This is much better than the 90nm design with an SNR of 51.5dB for the same conditions. For fulfilling this requirement the resistors were chosen very small to get an effective smaller area than in 90nm. Because of the smaller resistors the matching is in the same range as in 90nm and the width was not increased to avoid large parasitic capacitors.
The mentioned calibration technique was patented and implemented for both types of pre-processing the 90nm and the 65nm.
The competitors and therefore state of the art pre-processing do not have this filter opportunity and large gain programming range which enhances the picture quality. Specially for high quality application this analog signal processing gives the system developer the right tool.

Table 3.6: Comparison of different pre-processing topologies

Pre-Processing	Stages	THD (dB)	SNR (dB)	Matching (%)	Power (mW)	Area (mm^2)
4^{th} order	4	52	54.5	0.36	47.5	0.059
4^{th} order Sallen-Key	3	36.7	54.2	0.32	38	0.076
3^{rd} order	3	52	54.7	0.36	38.7	0.05
3^{rd} order AGC-Filter	2	51	53.4	0.27	32.4	0.045

Chapter 4

90nm Pipeline ADC

For this chapter the research result of [13] was used. In this paper the most important scientific facts were presented. Video frontends of Micronas in 0.18μ and 0.13μ used two step Flash ADCs. The DSM technologies with its very small transistors with large transit frequencies provide the opportunity to use new ADC topologies like pipelining of x bit stages.

Another approach would be the integration of sigma delta ADCs [14]. Those kind of ADCs are used for low power communication ICs. Unfortunately the bandwidth of sigma delta ADCs is too low. Hence the best speed and power compromise for mid resolution (10bit) and high speed pipeline ADCs is the 1.5bit per stage topology [15], [16]. This architecture provides high throughput at low power. Moreover the constraints on the comparator offset voltage and DC op-amp gain are relaxed. This chapter shows the trade off design for consumer video application.

Area and power can be saved by accepting larger noise and distortion at signal frequencies larger than 60MHz. A 10 bit 165MS/s pipelined ADC without a dedicated 'Sample and Hold' [17] will be introduced. For RGB signals from graphic cards, where the pixel frequency can reach more than 60 MHz, the input bandwidth of the ADC must exceed more than 300MHz. This means that the ADC should follow the pulses of a graphic card. For video signals the specification must be done taking the behavior of the human eye and brain into consideration.

Also digital crosstalk must be taken into account because of the integration of the ADC on a digital system (system on chip). Many approaches were proposed to reduce power and area e.g. op-amp sharing [18], no dedicated S&H, time interleaving. The power consumption is determined by the op-amp in the MDAC (Multiplying DAC) and the reference buffer. The ADC uses a 1.5 bit per stage with op-amp sharing topology. That is why the amount of op-amps is reduced to 4. Moreover two types of op-amps were used for simplicity in layout. First

the nonidealities of a 'Sample & Hold' will be discussed. Second the op-amp sharing technique and the different building blocks will be explained. Finally the measurement results are presented.

4.1 Nonidealities of Sample and Hold Circuit

Typically track and hold circuits are used for analog to digital conversion. Also for this ADC a track and hold was used. The most difficulties using this circuitry are shown in the following:

4.1.1 Tracking Error

The tracking error is influenced by different effects like:

- The finite bandwidth which doesn't affect the linearity.
- The Ron of the switch increases nonlinearly with the input signal.
- The CJ (junction capacitance of MOS switch) decreases nonlinearly with an input signal which causes a nonlinear tracking error.

Therefore special care was taken to reduce the Ron, where bootstrapping was employed. Hence CJ is also small. The low ohmic Ron results also in a large input bandwidth.

4.1.2 Aperture Time Error

There exist three errors which were caused by an unstable sampling point. This will be discussed next:

- Aperture time error due to clock skew (affects only the sampling phase).
- Aperture time error due to clock jitter greatly affects the performance of the S & H which put stringent requirement on the clock network layout.
- Aperture time error due to the fact that the turning off instant of the switch is a function of the input signal magnitude (this is the most difficult component to calibrate out).

$$\Delta t \leq \frac{\Delta V}{SR_{max}} = \frac{\frac{V_{FS}}{2^{N+1}}}{SR_{max} \cdot 2 \cdot \pi \cdot f_{in}} \tag{4.1}$$

Equation 4.1 shows the aperture time error depending on the clock jitter. N was assumed with 10 bit where for the calculation a headroom of 11 bit was taken.

Hence an aperture time error of approximately 1ns is allowed.
Moreover the transition error due to channel charge injection and charge redistribution must be considered when the MOS switch is turned off. The fully differential approach can eliminate transition error to the first order, if the matching is perfect. The droop error due to leakage current of the switch and storage capacitor is not a problem for high frequency applications. The lowest sample frequency of the ADC can be around 10MHz.

4.2 ADC Architecture and Op-Amp Sharing

The ADC consists of eight 1.5 bit stages with 4 shared op-amps plus a 2 bit Flash converter shown in figure 4.1. Each stage implies a sub-ADC where the sub-ADC of the first stage performs the decision at the same time as the first MDAC samples the input signal. This is necessary in order to have the decision of the sub-ADC immediately after the sampling of the MDAC. Hence the sub-ADC samples the reference voltage during the amplification phase of the MDAC and follows the input signal during the sampling phase of the MDAC. In the MDAC the input is sampled on two capacitors where in the amplification phase one of these capacitors is flipped to the output of the op-amp. The matching of various control signals is difficult and requires a careful layout.

At the end of this pipeline a two bit Flash ADC converts the residue into digital. In the first stage boosted switches are used for the input signal. After delaying the digital outputs of each stage by shift registers, error correction is used for compensating the offset of the sub-ADC. The maximum corrected sub-ADC offset at the first stage equals 0.25 of the reference voltage vref after 8 stages. If the first stage samples the input signal the second will be in the amplification mode. The capacitors are chosen to fulfill the matching requirements. In the second stage they are scaled by a factor of two, so the load of the shared op-amp varies from phase to phase. Along with the third stage the capacitor values stay constant to simplify the layout.

Furthermore a feature of this ADC is the skipped 'Sample and Hold'. The sampling occurs in the sub-ADC and the MDAC at nearly the same. An aperture error depending on the input signal frequency and the maximum correction range is calculated in equation 4.2. For the 10bit 165MS/s ADC the maximum allowed aperture time error corresponds to 660ps for a 60MHz 0.4Vp input signal.

$$dt = \frac{du}{2 \cdot \pi \cdot f_{in} \cdot Vin_{max}} \tag{4.2}$$

For noise considerations the amount of noise sources must be referred to the input of the pipeline and summed up. Noise contributors are kT/C, reference,

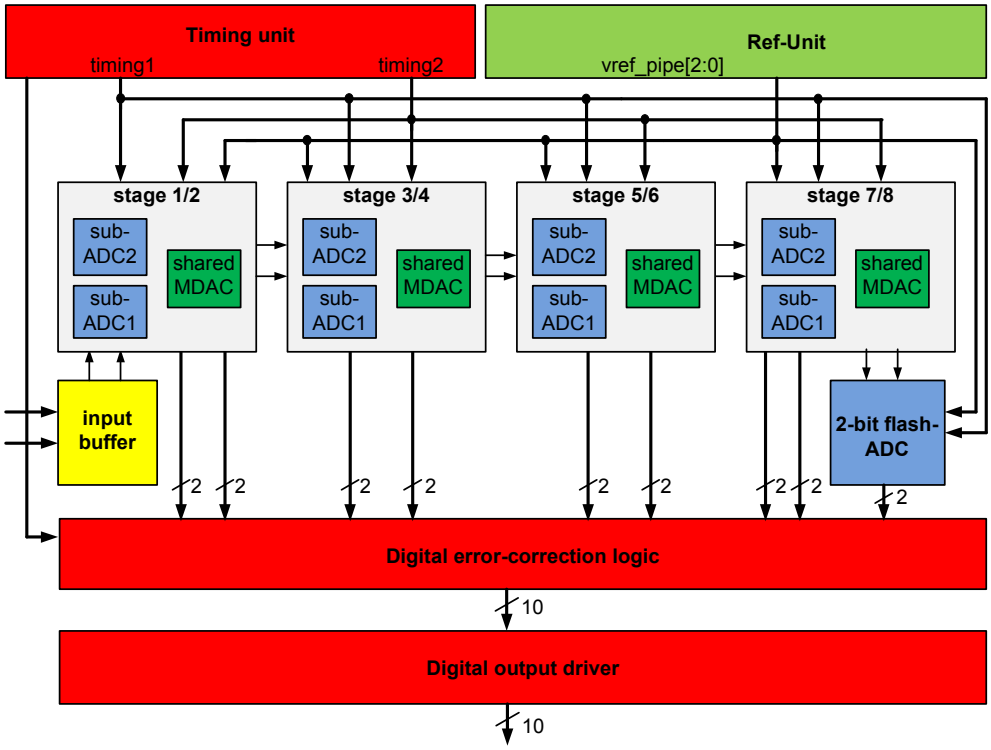

Figure 4.1: Principle architecture of the 90nm pipeline ADC

op-amp and switching noise. For this 10 bit ADC the quantization noise corresponds to 280μVrms shown in equation 4.3. Therefore the noise energy of the contributors should be lower than the quantization noise.

$$Noise_{input} = 2 \cdot \frac{k \cdot T}{C} + opamp^2_{noise} + ref^2_{noise} + switching^2_{noise} \qquad (4.3)$$

The idea of the op-amp sharing approach is to use one op-amp for two consecutive stages. Power and area can be saved where the op-amp can be scaled for the preceding stages. The op-amp sharing technique [18] has two drawbacks. The additional switches that implement op-amp sharing introduce series resistance and degrade the settling behavior of the pipelined stage. Moreover the op-amp is never reset and the residual signal effects the current input sample.

The principle topology of the first stage is shown in figure 4.2. The switch in front of the op-amp was designed very low ohmic to guaranty best settling performance. Due to this switch and the parasitic input capacitance of the op-amp an additional zero is generated at the output.

The same op-amp is used for two different loads. It is optimized for the first

stage load. The second stage load has the half capacitance so very slow settling will occur if the op-amp is used for the second stage. This can be allowed because the settling accuracy must be better than 8bit effective resolution.

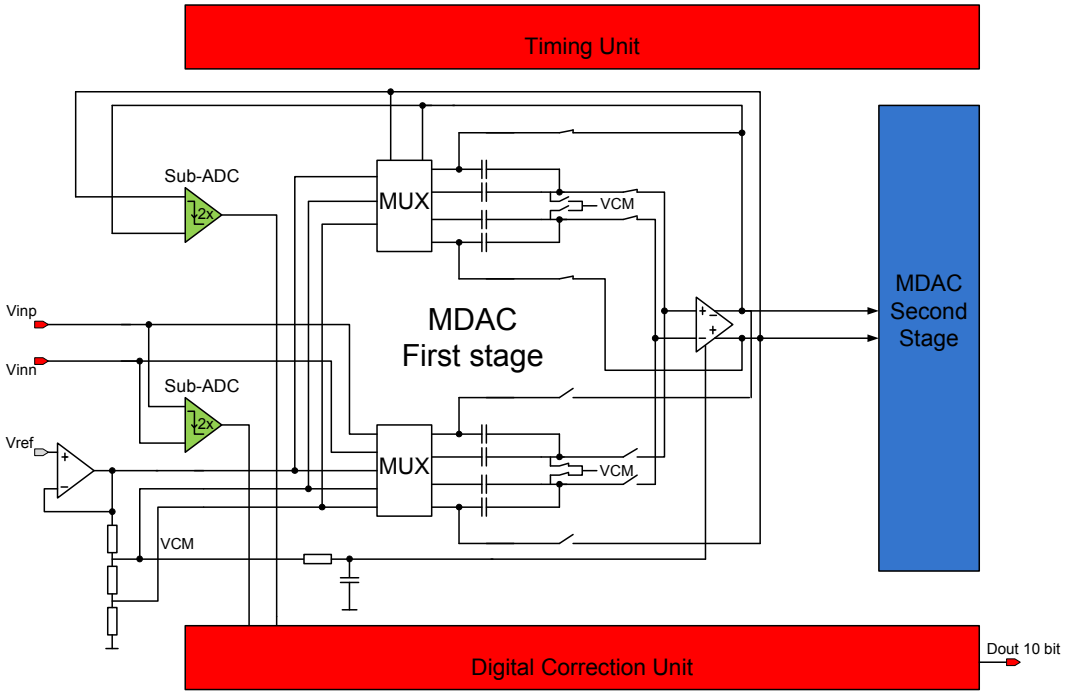

Figure 4.2: MDAC of the first stage with op-amp sharing

4.3 MDAC

Figure 4.3 presents the MDAC where the input signal is sampled on Cin_1 and Cfeed_1. During amplification Cfeed_1 is flipped to the output and the charge of Cin_1 is transferred to Cfeed by activating the switch at the input of the op-amp with 'samp inverted'. Hence a gain of 2 is realized. This switch has to be optimized for op-amp settling and parasitics. Also in the amplification phase Cin_2 and Cfeed_2 are charged by the residue of the first stage. Because of using one op-amp for two stages the parasitics are pre-charged in the preceding phase. Further the decision of the sub-ADC needs several picoseconds to adjust the right reference voltage for subtraction.

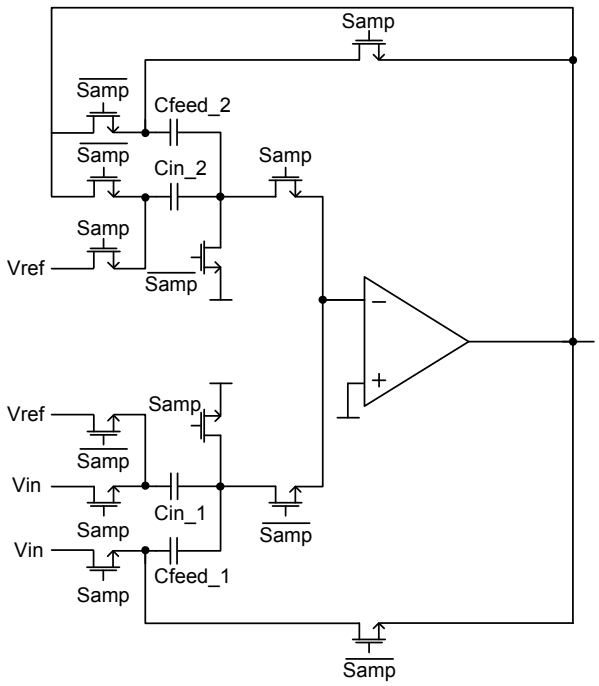

Figure 4.3: MDAC with shared op-amp

4.4 Sub-ADC Circuit Design

For the sub-ADC two charge distribution comparators are used. In figure 4.4 the dynamic latch stage of the comparator is presented where coupling capacitors are connected to the inputs. This topology shown in figure 4.4 is developed from the comparator published in [19]. The comparator requires a non overlapping two phase clock. During phase 'samp inverted' the reference is sampled on Cref and vcm is sampled on Cin. When the signal samp is released the charge in Cref is redistributed on both caps Cin and Cref and compared to the input voltage shown in equation 4.4. With 'samp inverted' M3 is active, M6 and M9 are off and the latch can perform the decision, whereby the load works as an inverter with positive feedback.

$$vin\_p - vin\_n = \frac{Cref}{Cin + Cref} \cdot (vref\_p - vref\_n) \tag{4.4}$$

Figure 4.5 illustrates the sampling network of the MDAC and sub-ADC [20]. It demonstrates, that Cfeed and Cin must be charged by a current flowing through Rs_boost1 and Rs_boost2 after applying an input step. The voltage at R_vcm decreases to zero after some nanoseconds defined by the on-resistance of the switches. At the same time the comparator inputs are following the divided input voltage of the capacitors Cs_comp and Cpar_comp. In these capacitors the

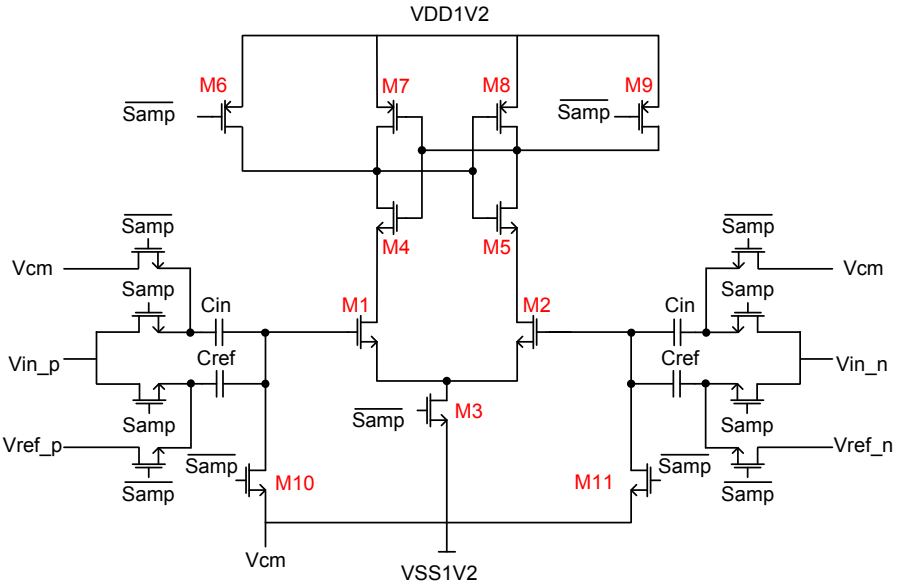

Figure 4.4: Comparator for the sub-ADC

reference voltage is stored and compared to the input. In that case little or no delay is generated because no current is flowing. Hence matching of the sample time is very difficult but could be reached by using a pre-amplifier in front of the comparator. Otherwise better matching could be achieved by sampling reference and input voltage at the same time in front of the comparator. The advantage of this technique compared to other solutions is that the comparator decision is done immediately after sampling occurs. Therefore the available time for settling is enlarged.

4.5 MDAC Folded Cascode Op-Amp

The DC gain of the MDAC is determined by the resolution (N-bit). The total error ϵtot at the input of an N-bit converter should be less than LSB/2, which corresponds to the condition $\epsilon tot \leq 1 \ / \ 2^{N+1}$. So this translates for the open loop DC gain:

$$A0 > 20\,(N+1)\,log2 \tag{4.5}$$

For settling to N bit accuracy, it is necessary that the settling error $\leq 1/2^N$ is fulfilled. The output has to settle to N-bit accuracy in the time period $1/3f_{Clk}$ which leads to the following requirement for the GBW (4.6) where the feedback factor is equal to 0.5.

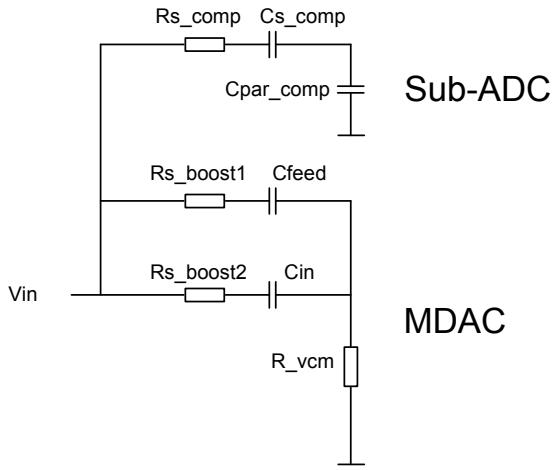

Figure 4.5: Sample network of sub-ADC and MDAC

$$GBW > \frac{3 \cdot N \cdot ln2}{2 \cdot \pi \cdot \beta} \cdot f_{clk} = 1.22GHz \tag{4.6}$$

The amplifier used is a folded cascode op-amp shown in figure 4.6 with gain boosting and a continuous time common mode loop. Due to the low supply voltage of 1.2V it is not possible to use more than 4 transistors in one branch to achieve enough headroom to stay in saturation. The currents in the cascode and input branches have the same values. The bias current for the common mode loop is mirrored by using the same drain source voltage. This is realized by using vcm also for the cascode of the current source. Furthermore the common mode loop sees a higher load than the differential one where the bias current is in the range of the bias current for the input. The gain bandwidth GBW of the regulated cascode was calculated to be smaller than the overall GBW of the op-amp, but bigger than the 3dB bandwidth of the op-amp with fixed cascodes [9].

4.6 Reference Buffer

For the reference generation a simple single stage miller op-amp with cascode load of the differential pair shown in figure 4.7 is used. In the output branch the PMOS transistor drives the current to three low ohmic resistors. These are used for generating the reference voltages for the ADC. The resistor width is chosen by fulfilling the matching and gain error requirements of the ADC. Also vcm is produced by the same resistor string, so the references are always symmetrical to vcm. The open loop gain is up to 40 dB and is enough. The great benefit is the low noise contribution.

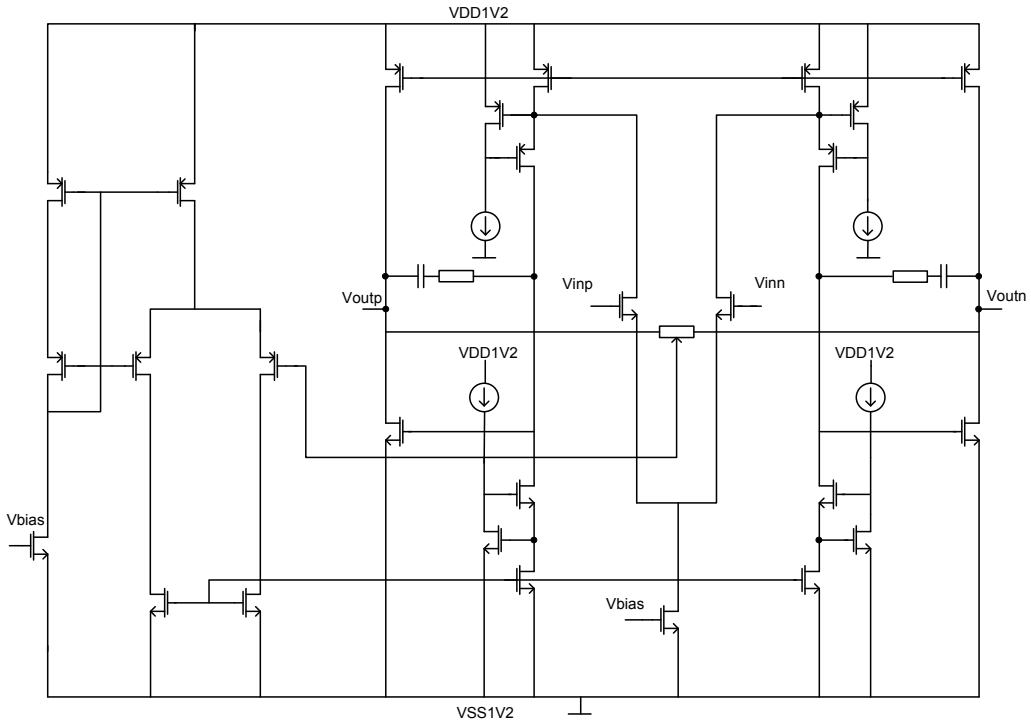

Figure 4.6: MDAC folded cascode op-amp Miller compensation

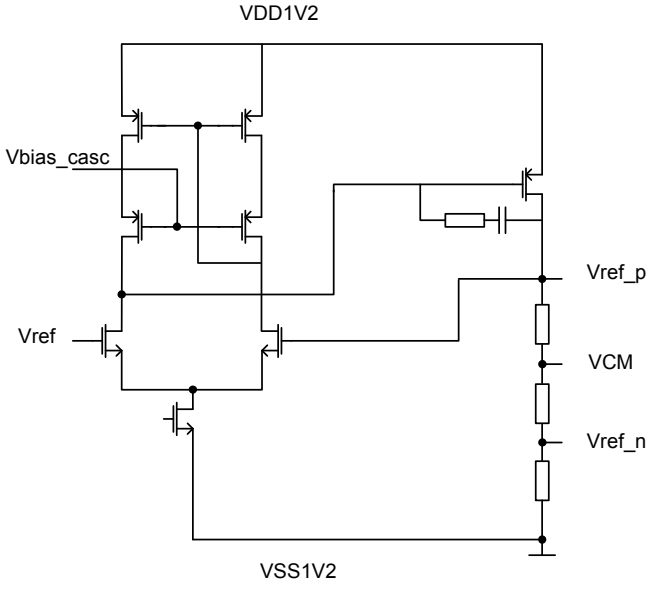

Figure 4.7: Single ended reference buffer

4.7 Layout of the ADC and Scaling

The layout shown in figure 4.8 was optimized for speed and low noise. Hence low parasitics were required. The wiring was always done on the highest possible metal layer. Special care was taken on the wiring of the sampling switch in the MDAC and sub-ADC. The wires have the same length to enable the sampling switch at the same time to reduce the aperture error. On the left the reference buffer is located which drives the 4 shared op-amp stages. On top there is the 2-bit Flash ADC and the error correction unit. The timing is placed on the right. For power reasons the capacitors were reduced by a factor of two. The lowest capacitor corresponds to one fourth of the unity capacitor of the first stage. A higher reduction does not make any sense because of the otherwise dominating parasitic capacitors. This ADC employs two kind of op-amps to simplify the design.

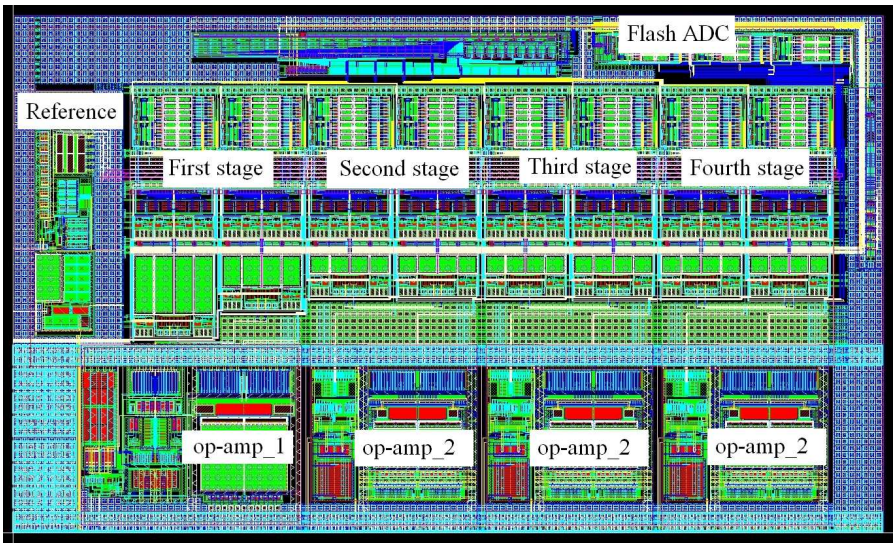

Figure 4.8: MDAC with shared op-amp

4.8 Experimental Results

A new measurement method is introduced in the next section. It is called pad noise suppression and was developed by Peter Pridnig to be able to evaluate the performance of the ADC and not the chip environment. The introduction of this technique is necessary to understand the measurement results.

4.8.1 Pad Noise Suppression

Although on IC and on test board level special care was taken to minimize the coupling of digital switching noise of the output pads into the sensitive analog input resulting in SNR degradation, further actions were taken in order to evaluate the ADC performance. The signal of the digital outputs was reduced from 3.3V to 1V and each ADC output signal was gated with a simple logic element shown in figure 4.9. As can be seen in figure 4.10, the stream of digital output words is disabled repetitively by applying the signal 'disable_pad' which results in active and inactive time periods of the digital output pads spaced by D data words. Due to latency of the digital ADC logic, the actual sample time of each data word occurs some cycles before.

If the suppressed time period is long enough, no disturbing pad rail action occurs at that time which leads to a stream of undisturbed data words. Storing only one sample out of D data words acquired in sequence leads to the concept of data decimation (1/D output decimation). The decimated sample rate now is a factor of D smaller (fstr/D, where fstr is the ADC strobe frequency). The overall time needed to sample the record of data now is a factor of D longer. This could lead to unwanted effects of additional SNR-degradation due to long-term jitter effects of the signal sources. By comparing data recorded with and without decimation, it should be ensured in advance that the test setup and the device under test are not prone to such kind of non-idealities. Notice that decimation involves loss of information which may hide relevant phenomena. In our case it was possible to ensure that the observed SNR degradation is truly related to digital pad noise as shown in figure 4.11.

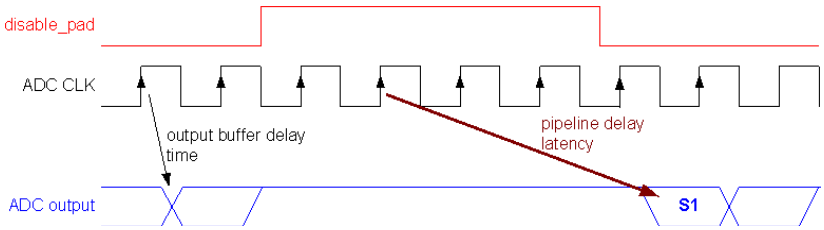

Figure 4.9: ADC output signal gating

4.8.2 SNDR, DNL, INL

In figure 4.11 the signal to noise and distortion ratio depending on the sampling frequency can be seen. Unfortunately the clock input is located 8 pins away from the signal inputs. Also there was no extra supply available for the clock inputs to reduce the current loop on the board. For the 1V output driver two double

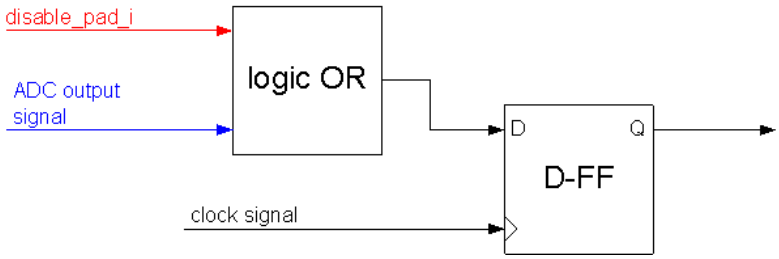

Figure 4.10: Control sequence

bonded supply pins were used. This driver was developed to decrease the voltage swing and the switching noise impact. The ADC gets the reference from a 3.3V bandgap, which is also used for bias current generation. Moreover the input signal is amplified with a 1.2V buffer to drive the sample capacitors of the ADC to avoid distortion due to the parasitics of the input pins. These measures were necessary to evaluate the ADC and not its environment.

The figure of merit (4.7) of the introduced ADC with reference buffer equals 0.78pJ per conversion step. The power consumption can be further optimized by reducing the current in the cascode and output branch of the op-amp. This is done in the 65nm pipeline ADC.

$$FOM = \frac{P}{2 \cdot BW \cdot 2^{ENOB}} = 0.78pJ/step \tag{4.7}$$

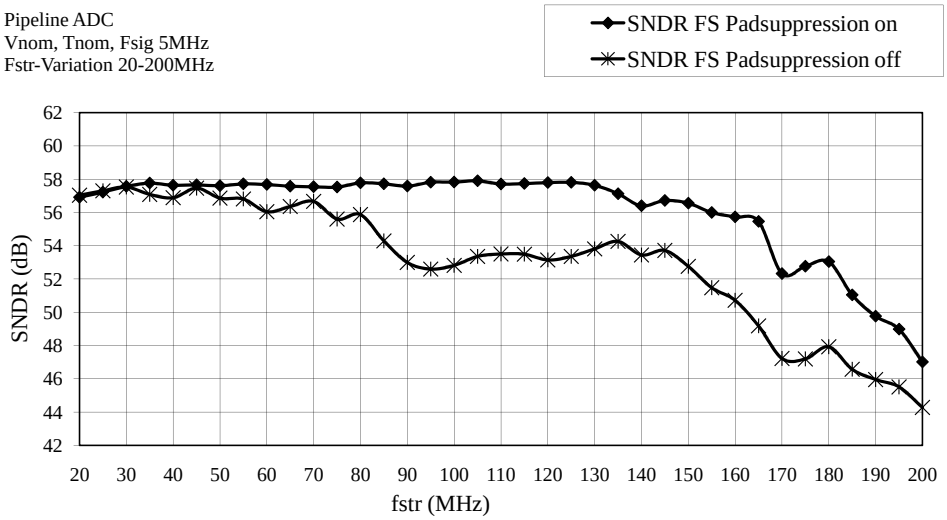

Figure 4.11: Signal to noise and distortion ratio with and without pad noise suppression technique

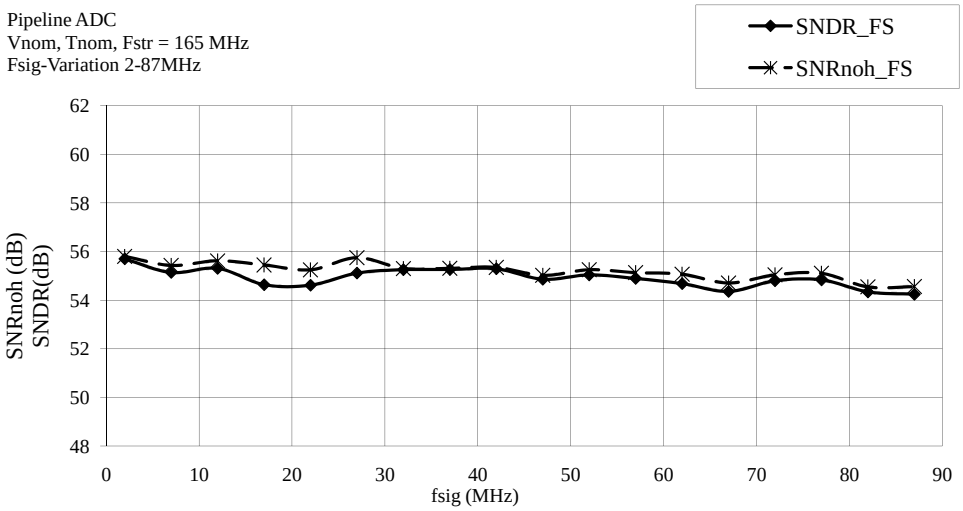

Figure 4.12: Signal to noise and distortion ratio depending on the signal frequency

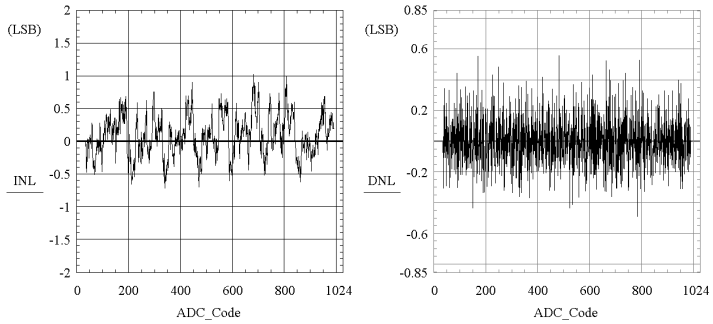

Figure 4.13: INL and DNL fsig=2MHz at fs=165MS/s

4.8.3 1V Digital Output Driver

This new digital pad was designed for driving the pin and input capacitance of the logic analyzer at a very low voltage swing of 1V. It is shown in figure 4.15 where three different inverters can be selected by the driver strength control signal. An inverter which can be enabled by the driver strength control signal is used to drive an inverter which is connected directly to the gate of the P or NMOS pad driving transistor. So the optimum transient behavior and low slew rate can be achieved. Ten metal wires were switched in parallel and connected to the digital empty output pad. With this topology the digital crosstalk to the analog input pins was further reduced.

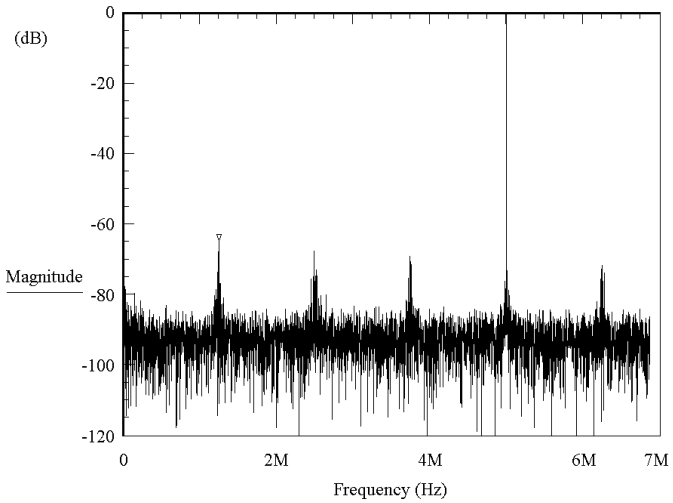

Figure 4.14: Decimated frequency spectrum at fsig=60MHz and -2dBFS

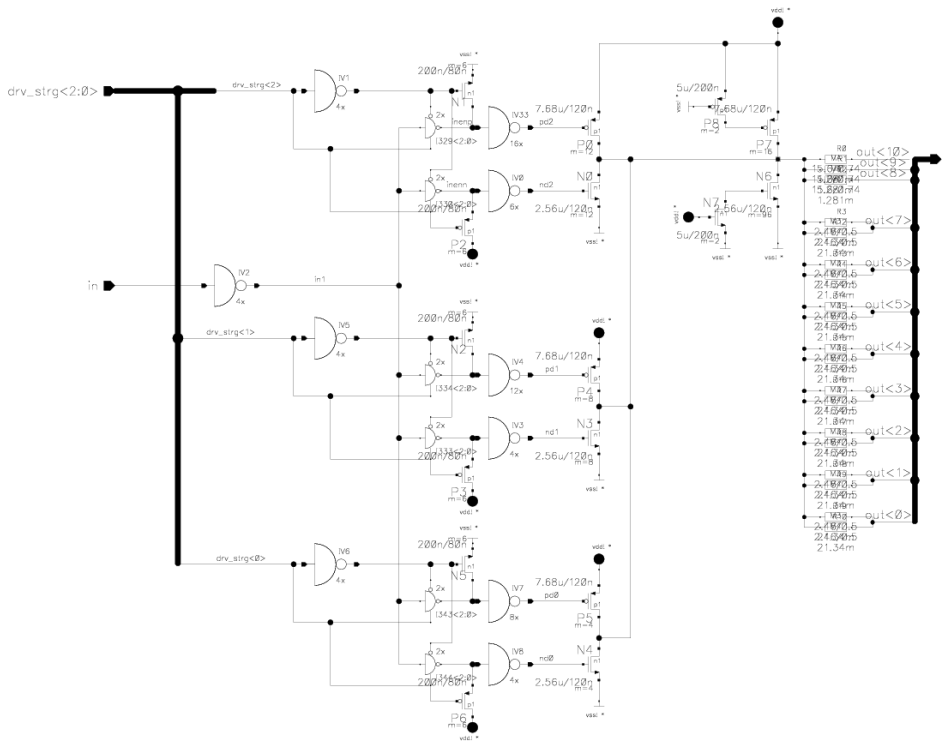

Figure 4.15: Schematic of the 1V digital output pad

4.9 Summary of Chapter 4

A pipeline ADC with op-amp sharing, dynamic latch with capacitive inputs and single ended reference buffer has been presented. Due to two different sampling networks for MADC and sub-ADC the problem of matching of the sample point has been discussed. Furthermore it has been demonstrated that by using a 'pad noise suppression' technique the performance measurement has been improved by nearly 5 dB. The DNL corresponds to +0.56/-0.49 LSB10 and the INL equals +1.03/-0.72 LSB10. The effective number of bits is 9 at 2 MHz input and 8.7 at 87 MHz input measured with a strobe frequency of 165MHz. The ADC consumes 46mA at 1.2V and occupies an area of 0.15 mm^2 in a 90nm CMOS process.

Chapter 5

65nm Pipeline ADC

For this chapter the research result of [21] was used. In this paper the most relevant scientific facts were presented. The 90nm pipeline ADC was improved and transferred to the 65nm process. The improvement was necessary to reduce power and area. The ADC does not use a dedicated 'Sample and Hold' stage and is built by means of the cascade of 8 pipeline stages and a 2-bit flash ADC. For aperture error reduction between the 'Sample and Hold' of the MDAC and the sub-ADC a preamplifier was placed in front of the sub-ADC. Due to its offset compensation technique the headroom for the aperture error can be increased. Moreover special care was taken and analyses were done on the parasitic capacitors of these stages to get nearly the same transient bahavior. Operational amplifier sharing technique is used in order to reduce power consumption. Nested cascoded miller compensation technique is employed to optimize speed and power of the first and second stage.

5.1 ADC Architecture

Figure 5.1 shows the principle schematic of the proposed ADC. The input is buffered by a 1.1V differential buffer used as inverting amplifier with gain one. This buffer consumes 8.8mW and limits the input bandwidth from 400MHz to 600MHz over process, temperature and voltage deviation. The ADC introduced here consists of eight 1.5bit stages where one amplifier is shared for 2 stages to save power. The 1.5bit per stage was chosen to realize the required high bandwidth for the amplifier due to a larger feedback factor than a stage with higher resolution. The power consumption was minimized by implementation of optimized amplifier architecture for the multiplying DAC (MDAC). Further a simpler digital correction circuit and a larger correction range of +/-0.25*vref (reference voltage) can be used. A high correction range is needed as the S&H was omitted resulting in a voltage error due to an aperture delay of 600ps at 60MHz input signal frequency and 130MHz strobe frequency. The sub-ADC employs 2

comparators which include a preamplifier but only in the first stage. At the end of the pipeline a 2bit Flash ADC converts the residue. The digital output of each stage is processed by the digital error correction logic. The timing unit generates the two non overlapping clock phases and the reference unit provides the bias currents and the reference voltages needed.

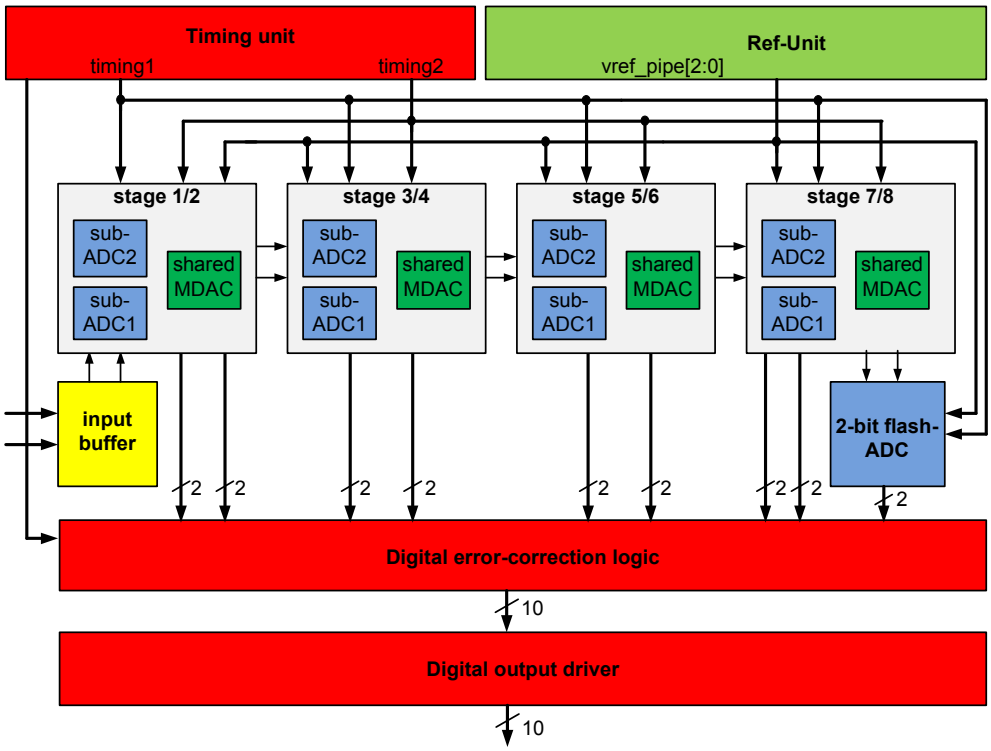

Figure 5.1: Principle architecture of the 65nm pipeline ADC

5.2 MDAC and sub-ADC sampling

If an RGB signal is processed by the ADC, the step response of the ADC must be fast enough that RGB pulses with a bandwidth of 200MHz can be sampled. Part of the previously mentioned correction range is used for these very fast input steps, because MDAC and the sub-ADC could sample at different points due to mismatch. The headroom for correction of the aperture error can be increased by an auto zeroing preamplifier in the sub-ADC of the first stage. Another reason for using this preamplifier is the different operating mode [16] of the MDAC and the sub-ADC. During the amplification phase of the MDAC the sub-ADC samples the reference voltage. In the sampling phase of the MDAC the sub-ADC tracks the input. After MDAC sampling the decision is immediately done by the

comparators. Figure 5.2 shows the sampling network with preamplifier in the sub-ADC and bottom plate sampling at the MDAC.

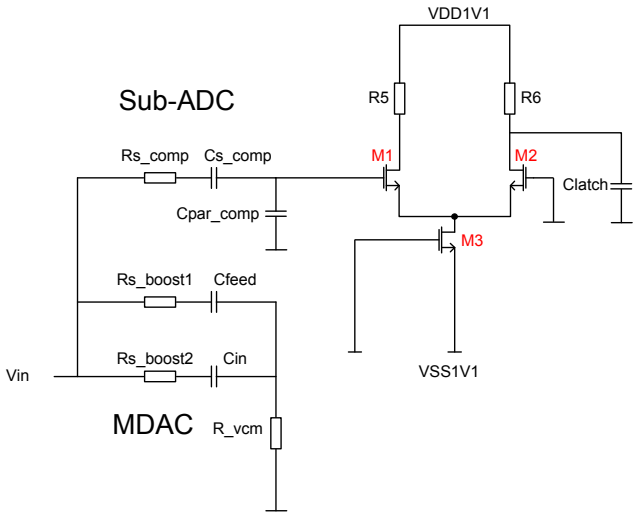

Figure 5.2: Sample network of the sub ADC comparator and the MDAC input

A further advantage of the preamplifier is the reduction of the kickback noise of the latch. Normally the time constant of the MDAC sampling network is larger than that of the sub-ADC without using a preamplifier. Specially in the case of using only latches for the sub-ADC, the MDAC sampling is much slower than the sub-ADC sampling. With very fast input steps a dynamic offset occurs. This can be seen in figure 5.3, where the falling edge of an input step leads to different sample points of MDAC and sub-ADC. The slower MDAC samples a smaller voltage than the sub-ADC.

The digital output code of the overall ADC is unsigned binary, where a zero input leads to code 511. The influence of these different sample points is shown in the residue of the first stage in figure 5.4. This difference leads to a shift of the decision level of the comparator. If this shift is lower than 0.25*vref it will be compensated. One reason to limit the input bandwidth of the MDAC is to reduce also the noise and harmonics of an input source, if no preamplifier is used. For a large input bandwidth the sample switches will become very large with big parasitic capacitors, which will lead to clock feedthrough and charge redistribution.

By matching the delay of the sampling network of the MDAC and the preamplifier of the sub-ADC the aperture error can be decreased. Additionally the wiring was done symmetrically for the MDAC sampling switches and the sub-ADC latch. Also the parasitic capacitors of the wiring were considered.
The matching of the MDAC and sub-ADC was verified in the lab. The output of

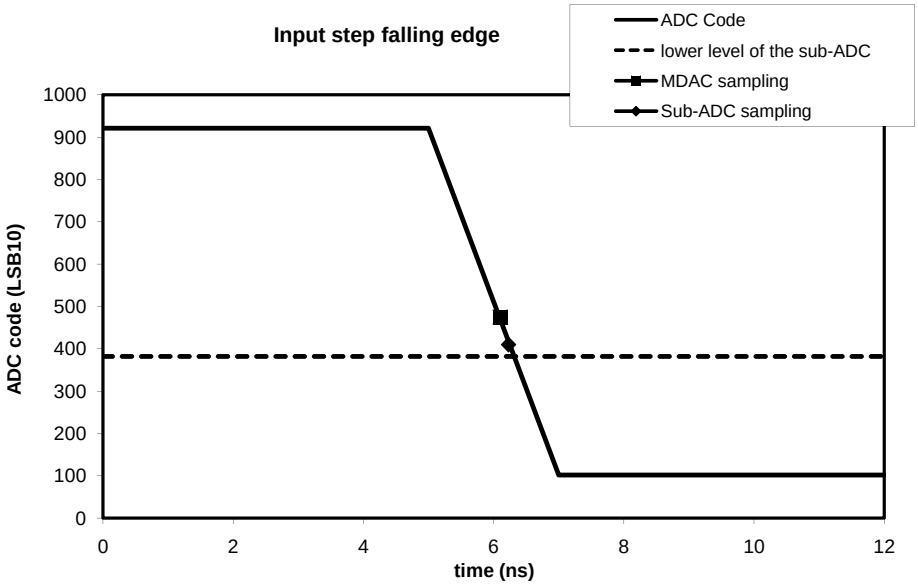

Figure 5.3: Input step at the output of the ADC with different sample points of the MDAC and the sub-ADC

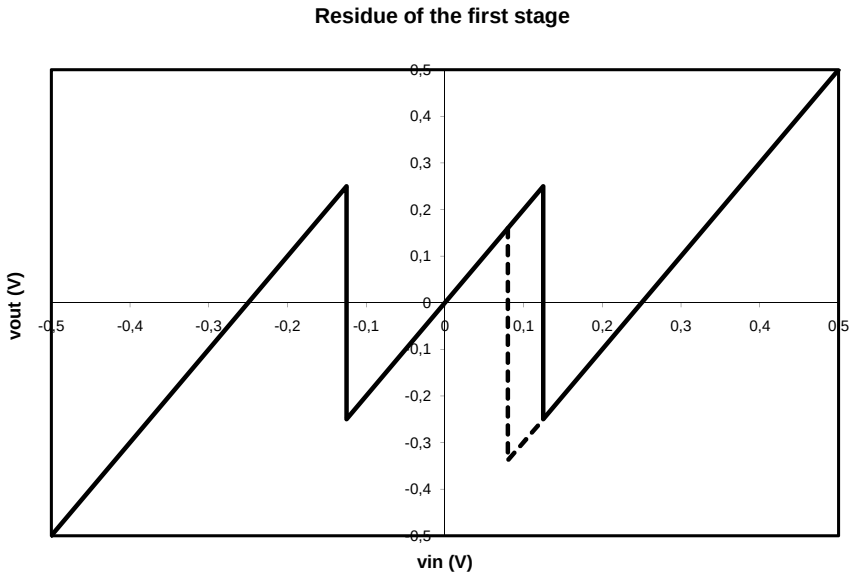

Figure 5.4: Residue of the first stage. The dotted line corresponds to an aperture error due to different sample times of MDAC and sub-ADC

the sub-ADC of the first stage is connected to a pad to access the time and level information of the comparators. An input step was applied to the ADC where the rise and fall time was changed from 1.8ns to 30ns. This was done at a sample

frequency of 20 MHz to eliminate the influence of the MDAC settling. Only the input sampling network was investigated. Figure 5.5 shows the measured sub-ADC output related to the ADC output depending on an input step. If a preamp is used the sub-ADC decision level stays constant even at 0.8Vpp falling and rising input steps of 2ns rise time. This is compared to an ADC without preamp, where the aperture error becomes larger than the correction range at 2ns rise time. The output offset will be stored, if the preamp input transistor is used in diode configuration. The offset at the output (5.1) due to threshold mismatch of the input transistors and resistive mismatch of the load resistor RL is stored. It is lower than the offset at the input (5.2) because of the finite gain (A=gm*RL) of the preamp. Therefore a minor offset will occur after offset compensation at the output of the preamp.

$$Voff\_out = \frac{Voff\_in}{1 + \frac{1}{A}} \tag{5.1}$$

$$Voff\_in = \Delta vth + \frac{VGS - vth}{2} \cdot \left(\frac{dRL}{RL} + \frac{dk'}{k'} + \frac{dW/L}{W/L} \right) \tag{5.2}$$

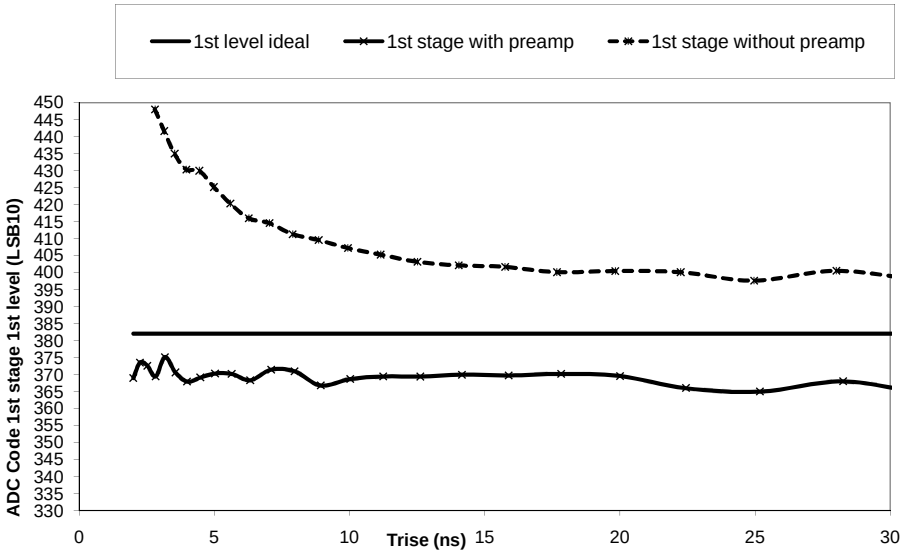

Figure 5.5: Sub-ADC output of the first stage with and without a preamp related to the ADC output measured with an input step of 0.8Vpp at 20MHz fstrobe

The bandwidth BW of the preamp was chosen to be in the same range as the MDAC input sample network. The rise time for an input-step corresponds to 300ps which can be calculated approximately as 0.35/BW, where BW equals 1/ 2*π*RL*CL; CL is the input capacitance of the latch.

5.3 MDAC Op-Amp with nested Miller compensation

Figure 5.6 shows the MDAC op-amp with nested cascoded miller compensation. Miller compensation would need more power at the same gain bandwidth product. In contrast the miller cascoded compensation could have bad settling time [22]. So the combination leads to a very good speed and power compromise. It is ideal if both Miller capacitors have the same value. In this case peaking in the frequency domain will never occur. Gain boosting is used in the MDAC amplifier to get more than 95dB open loop gain (5.3) and a gain bandwidth product of 1000MHz for N=10bit resolution of the ADC (5.4). The op-amp is used at a feedback factor of 0.5, where the phase margin reaches 65 degrees for 6dB gain. The op-amp employed by the first and second stage uses folded cascodes. Beginning with the third stage a simple miller op-amp was designed to decrease the power consumption.

$$A0 > 20\,(N+1)\,log2 = 66dB \tag{5.3}$$

$$GBW > \frac{3 \cdot N \cdot ln2}{2 \cdot \pi \cdot \beta} \cdot f_{clk} = 1GHz \tag{5.4}$$

5.4 Input buffer

The input buffer is used to drive the input capacitors of the ADC otherwise the input signal would be distorted by the inductances of the bond wire and the parasitic capacitances of the input pins. Especially at 1Vpp input steps high currents charging the sampling capacitors flow through the bond wire if using no input buffer. The input buffer is used for filtering the input. A diode biased cascode in the differential amplifier is employed to get an open loop gain of more than 50dB. In contrast to a folded cascode amplifier, the power consumption and noise is lower. The amplifier is operated at a feedback factor of 0.5.

5.5 Layout of the ADC

The layout shown in figure 5.7 was optimized for speed and low area. Hence low parasitics were required. The wiring was always done on the highest possible metal layer. Special care was taken on the wiring of the sampling switch in the MDAC and sub-ADC. The wires have the same length to enable the sampling switch at the same time to reduce the aperture error. On the right there is the reference buffer which drives the 4 shared op-amp stages. On top there is the

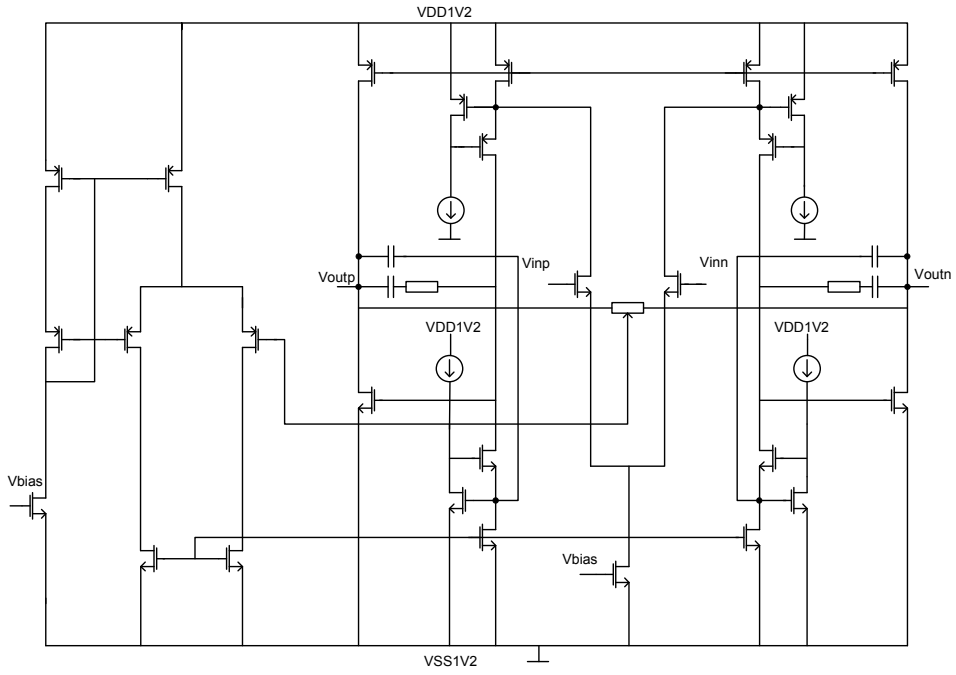

Figure 5.6: MDAC op-amp with nested cascoded miller compensation

2-bit Flash ADC and the error correction unit. The timing is placed on the left. The ADC was placed in the right corner where the inputs have maximum distance to the digital outputs. The clock input is on the right and directly transferred to a 1.1V buffer. Beside the clock input a digital ground was placed to enables the current flowing back.

5.6 Experimental results

As the ADC is used in a noisy system environment, disturbed by digital processing and crosstalk from digital output pads, the power supply rejection (PSR) of the proposed ADC must be large. High PSR is reached by using cascodes. Insulation and distance to neighboring noisy digital modules reduces the disturbance on the analog blocks. The ADC was fabricated in a standard digital 65nm CMOS process and encapsulated in a QFP100 package where the digital outputs are close to the analog inputs but orthogonal. A low voltage sine wave was used as clock signal, driving directly a 1 V buffer connected to an unused digital input pad. For closing the current loop a digital ground pin was set beside the clock input. Two double bonded supplies were used for the 2.5V ADC outputs. The bias current and reference voltages are externally supplied. Due to the low-power operation a low figure of merit is obtained.

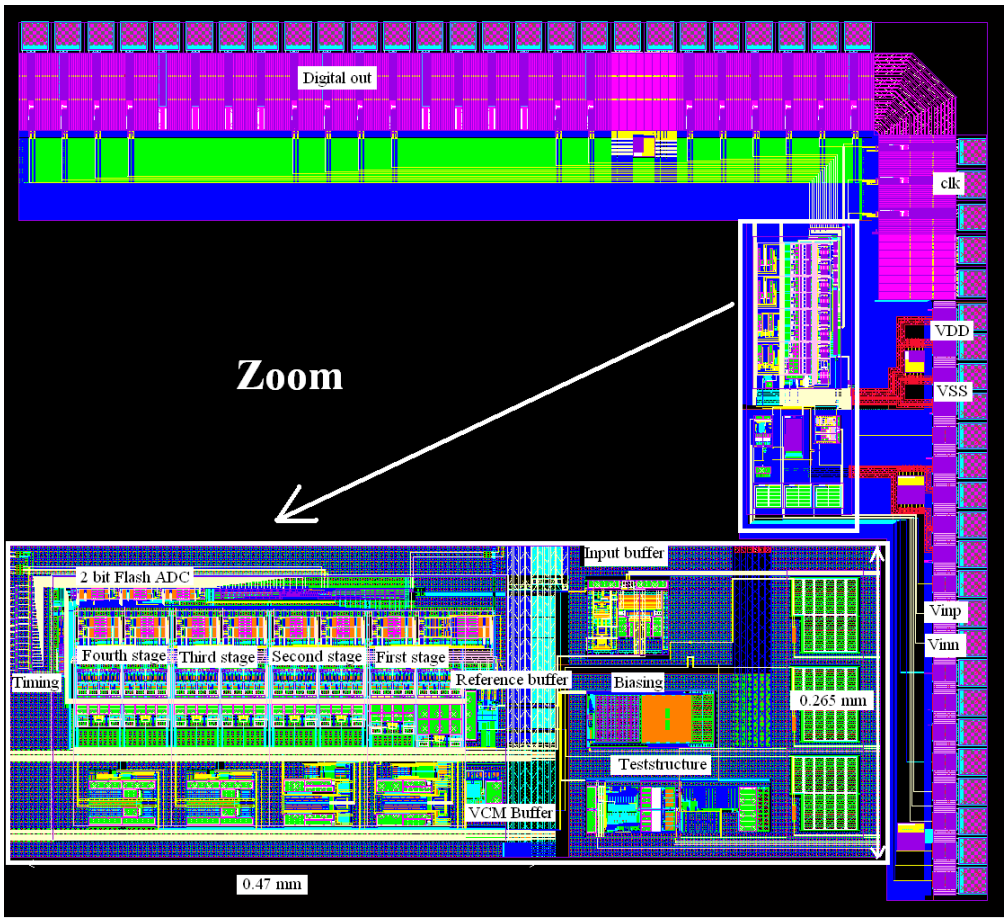

Figure 5.7: ADC and test-chip layout

$$FOM = \frac{P \cdot VDD}{2^{ENOB} \cdot Speed} = 0.5pJ/step \tag{5.5}$$

Figure 5.8 and 5.9 shows the SNDR depending on the strobe and signal frequency. Furthermore the INL and DNL is demonstrated in figure 5.10

5.7 Summary of Chapter 5 and Comparison of both Pipeline ADCs

A performance of 56.5dB SNDR at 5MHz and 50 dB at 85MHz input frequency is obtained at 130MS/s for full-scale. The occupied silicon area is 0.125mm^2, and the power consumption of 33mW from a 1.1V supply. A pipeline ADC without

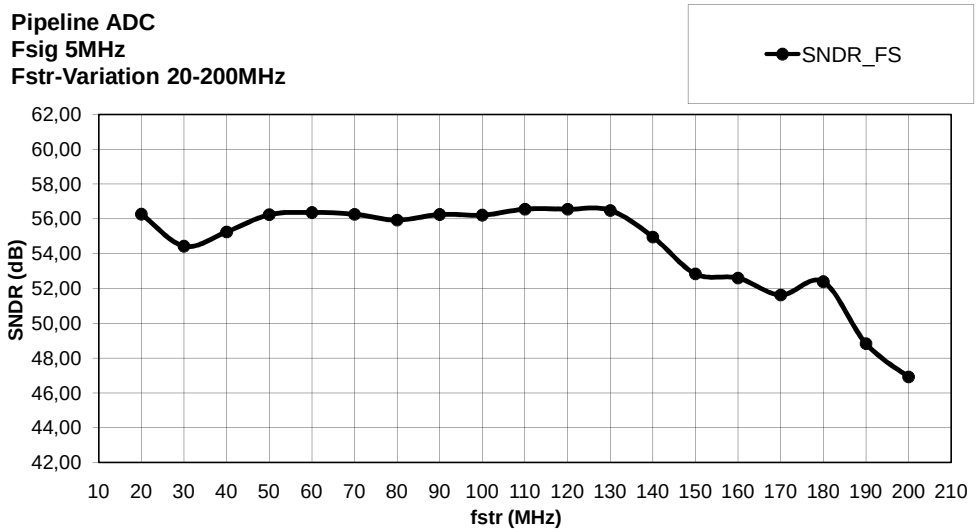

Figure 5.8: Signal to noise and distortion ratio depending on the strobe frequency

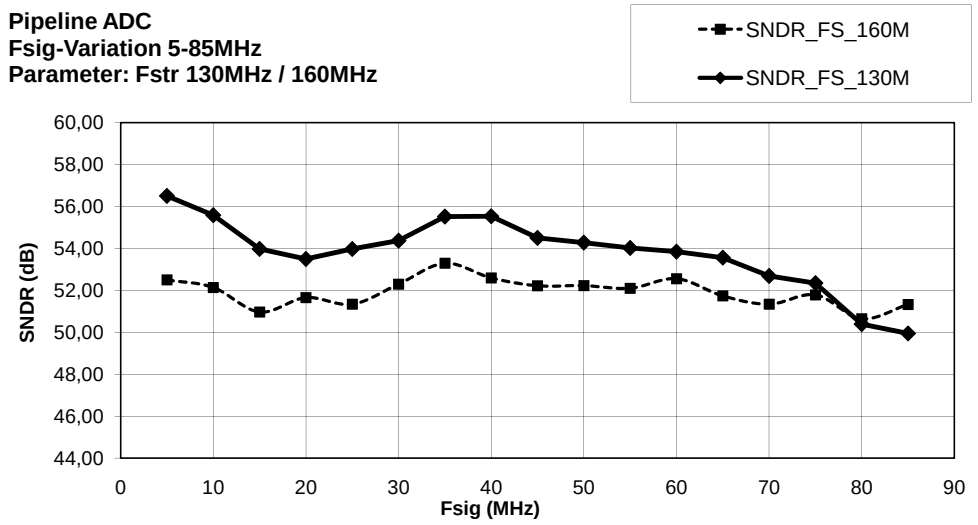

Figure 5.9: Signal to noise and distortion ratio depending on the signal frequency with 130 and 160 MHz fstrobe

dedicated S&H was presented. The aperture error between the sub-ADC and the MDAC was decreased by using a preamplifier in the sub-ADC. The power consumption of 33mW at 130MS/s was achieved by optimizing the compensation of the MDAC op-amp and scaling of the different stages. The DNL corresponds to +0.5/-0.5 LSB and the INL achieves +0.8/-1.6LSB measured at 5MHz at a strobe frequency of 130MHz. The SNDR/SFDR corresponds to 56.5dB/66dBc

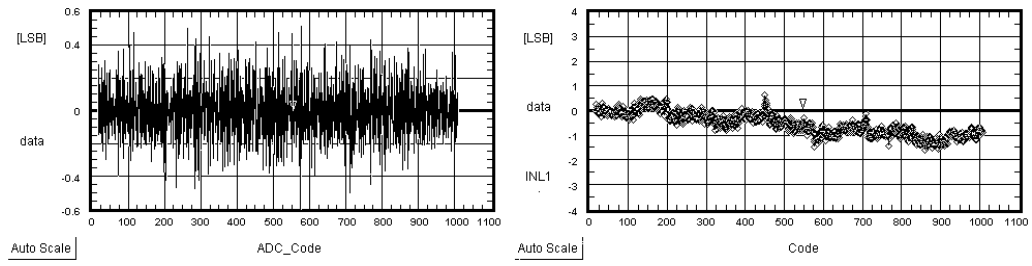

Figure 5.10: DNL and INL measured at fstrobe=130MHz

at 5MHz and 50dB/58.5dBc at 85MHz input frequency. The proposed ADC has been implemented in a 65nm standard digital CMOS process with an active area of 0.125mm^2 including the reference buffer. The area reduction of the 65nm pipeline ADC compared to the 90nm design came from architectural improvement like nested cascoded Miller compensation of the first two op-amps and using a preamplifier in front of the sub-ADC of the first stage.

For simplicity in the layout the scaling for the 90nm ADC was very simple. Only two types of op-amps were used. The sampling capacitors are scaled from 500f to 125f from the first to the third stage and stays constant at 125fF for the following stages. By using simple regular Miller compensation the compensation capacitors are two times larger than the compensation capacitors of the nested cascoded Miller compensated 65nm op-amps.
The area and power reduction is consequently achieved by reduction of the compensation capacitance and using 3 types of op-amps for the 65nm pipeline ADC. The current of the reference buffer stays constant for both pipeline ADCs. Table 5.1 demonstrates a comparison of the 65nm and 90nm pipeline ADC in terms of compensation and current consumption. Because of using op-amp sharing only 4 op-amps are employed by the 8 1.5bit stages. At the end of the pipeline a simple 2bit Flash ADC is connected.

Table 5.2 summarizes the overall ADC performance of the 65nm and 90nm pipeline ADC. It can be seen that the ADC from Singh [23] consumes lower power but at the doubled area than the 65 and 90nm pipeline ADC. Figure 5.11 shows a comparison with recently published pipeline ADCs considering the required area. The ADC with the lowest power and area is located in the upper right corner.

Table 5.1: Scaling of the 65nm and 90nm pipeline ADC in terms of the compensation capacitor and current consumption

Op 65nm	CC 65nm (fF)	IVDD 65nm (mA)	Op 90nm	CC 90nm (fF)	IVDD 90nm (mA)
op1	650	7	op1	1500	14
op2	470	4.5	op2	850	7.4
op3	600	3	op2	850	7.4
op3	600	3	op2	850	7.4

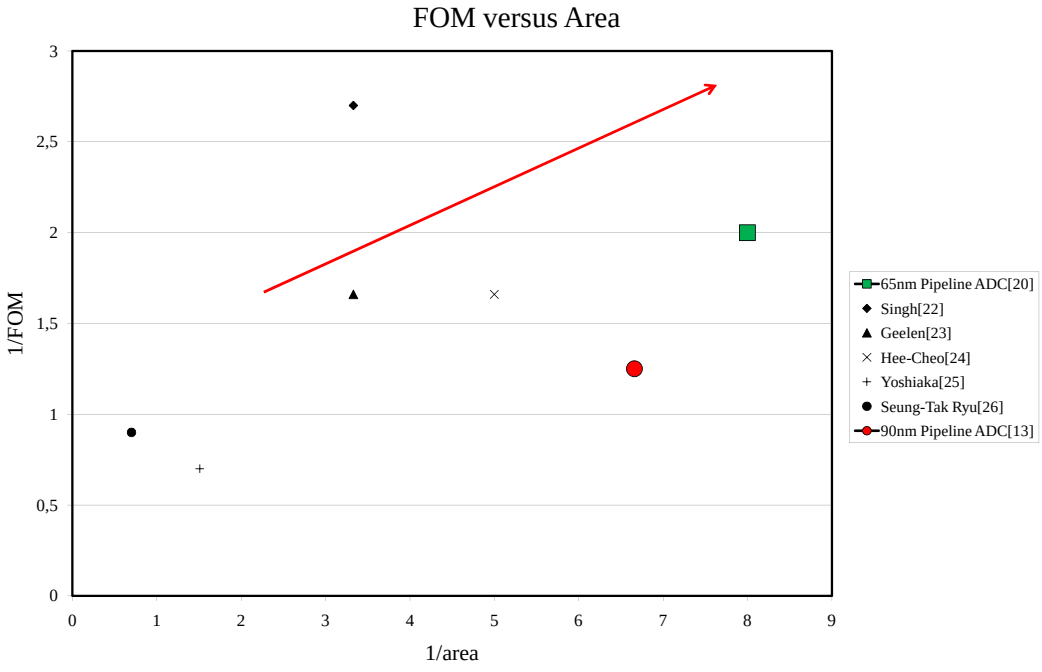

Figure 5.11: 1/FOM versus 1/area of the 65nm and 90nm pipeline ADC compared to state of the art ADCs

Table 5.2: Comparison of the FOM of the 65nm and 90nm pipeline ADC with state of the art ADCs

Tech. (nm)	Speed (MS)	Power (mW)	SNDR (dB)	FOM (pJ)	Area (mm^2)	Design (year)	Ref.
65	130	33	56.5	0.5	0.12	2008	This work [21]
65	100	23	59.1	0.37	0.3	2008	Singh [23]
90	120	36	57	0.6	0.3	2006	Geelen [24]
130	50	15	58	0.6	0.2	2006	Hee Cheol [25]
180	125	40	53.7	1.44	0.66	2005	Yoshiaka [26]
180	50	18	56.9	1.1	1.43	2006	Ryu [27]
90	165	56	56	0.8	0.15	2007	This work [13]

Chapter 6

90nm Analog Video Frontend with 8 Channels

6.1 Introduction

This chapter shows the application of the 90nm pre-processing in a SOC. An overview of the topology will be given and the solution for the problems will be explained. Special care was taken on crosstalk, wiring, power supply routing and clock distribution. Moreover the supply change from one channel or one domain to the next was considered. Therefore level-shifters and clamp diodes are inserted.

6.2 Toplevel

The input signals are processed and converted to digital by the top-level which stands for the overall analog video frontend. For HDTV signals always 4 channels are needed. This quadruple is necessary for RGB and YCrCb signals where the synchronization signal is separated and converted by the fast-blank ADC. Figure 6.1 illustrates the principle schematic of the analog video frontend. The analog ground was connected to the digital by PNP diodes. PNP diodes yield better results for crosstalk suppression.

6.2.1 Input Multiplexer

On the left of the principle top-level 19 input signals can be chosen by the multiplexer. There T-switches are employed to get less crosstalk and high linearity. If there are a lot of switches connected together at the output the linearity will be decreased because the parasitic capacitor of the switched off T-switches is voltage dependent. The analog and digital part of the multiplexer was done by full custom design to optimize area and parasitic capacitors. A standby of the channels

forces the input of the pre-processing to common mode. This must be done from reliability point of view to reduce NBTI and hot carrier stress. At the input of the multiplexer the clamp capacitor is connected. If any channel is connected to an input it will be biased to the common mode level. Therefore the clamp capacitor is precharged by a buffer for startup of the SOC and disconnection of the signal plug. The input signals can be directly aligned to the output buffer to support a DVD recorder.

6.2.2 Pre-Processing and Pipeline ADC

The 90nm pre-processing is used in combination with the 90nm pipeline ADC. To improve the channel gain matching specifically for the HDTV pre-processing the analog VSS of the RGB channel is connected. The net for ESD reliability must be large enough which was also a reason for the connection. Moreover the reference voltage of the pipeline ADCs is bonded for the tough channel gain matching requirement. The requirement for the fast-blank ADC is relaxed. The pre-processing in the fast-blank path (DC coupled) was designed for a filter bandwidth of at most 20MHz. But the filter-off cut-off frequency should match with the RGB-channel for the filter off mode. In the time domain the delay between these two filters must be lower (10ns) than the time needed for one pixel.

This depends on the resolution of the picture and thus on the horizontal frequency. For processing a green signal which includes also a synchronization pulse, the signal must be connected to the green and fast-blank channel. The green channel performs the clamping also for the fast-blank channel. The offset between these channels must be compensated. This is done by a constant DC shift in the input stage of the fastblank ADC. So the synchronization signal does not saturate. The clamp logic was outsourced to the digital to be more flexible in the analog part. The ADC supply was wired by aluminum and copper to the double bonded supply pad to reduce the voltage drop. For standard video different pre-processing's are used than for HD-signals to save power and area. The ADC is the same and the VSS is also connected for gain matching.

6.2.3 Interface and Logic

The interface was designed to provide the optimal connection to the digital part. The ADC data is registered with the incoming digital clock. This incoming clock is also buffered and lead to the different channels. Moreover the control and test signals are buffered. A special logic was required for the multifunctional pads which are used for digital test reasons and the limited pin count. Moreover the calibration logic can be tested digitally.

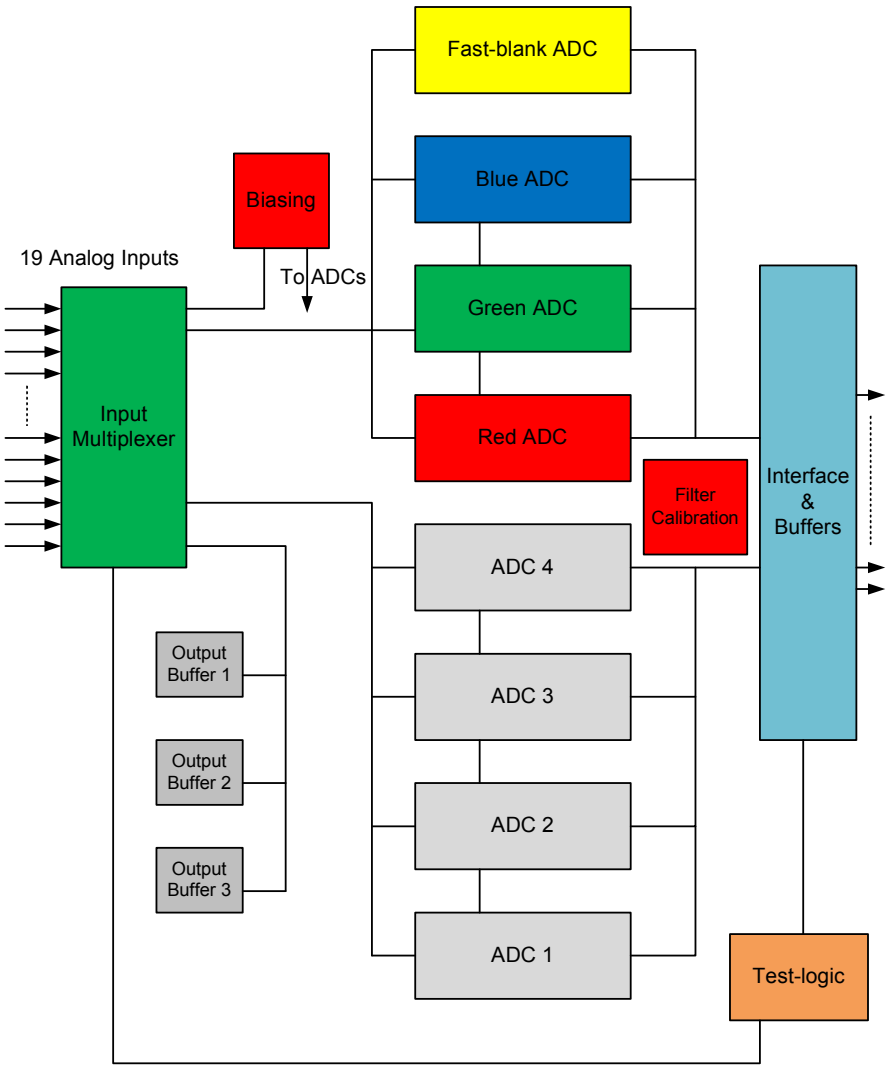

Figure 6.1: Principle top-level of the whole analog video frontend

6.3 Experimental Results

Several measurements are done like SNDR, SNR and THD. Only the results of the HD ADCs are shown in the following figures 6.3, 6.4, 6.5. It can be seen that the performance is better than the test-shuttle pre-processing. This is achieved because of the large distance of the digital outputs to the analog inputs. Additionally low voltage digital outputs are used to drive the flat panel display. Each channel has its own double bonded low ohmic supply. A supply or ground pin was placed in between two input pins to reduce crosstalk. One sense ground was used for 4 inut pins to reduce the pin count. The power consumption can reach 1W and the area is about $2mm^2$. A SNDR of 55dB was obtained at the

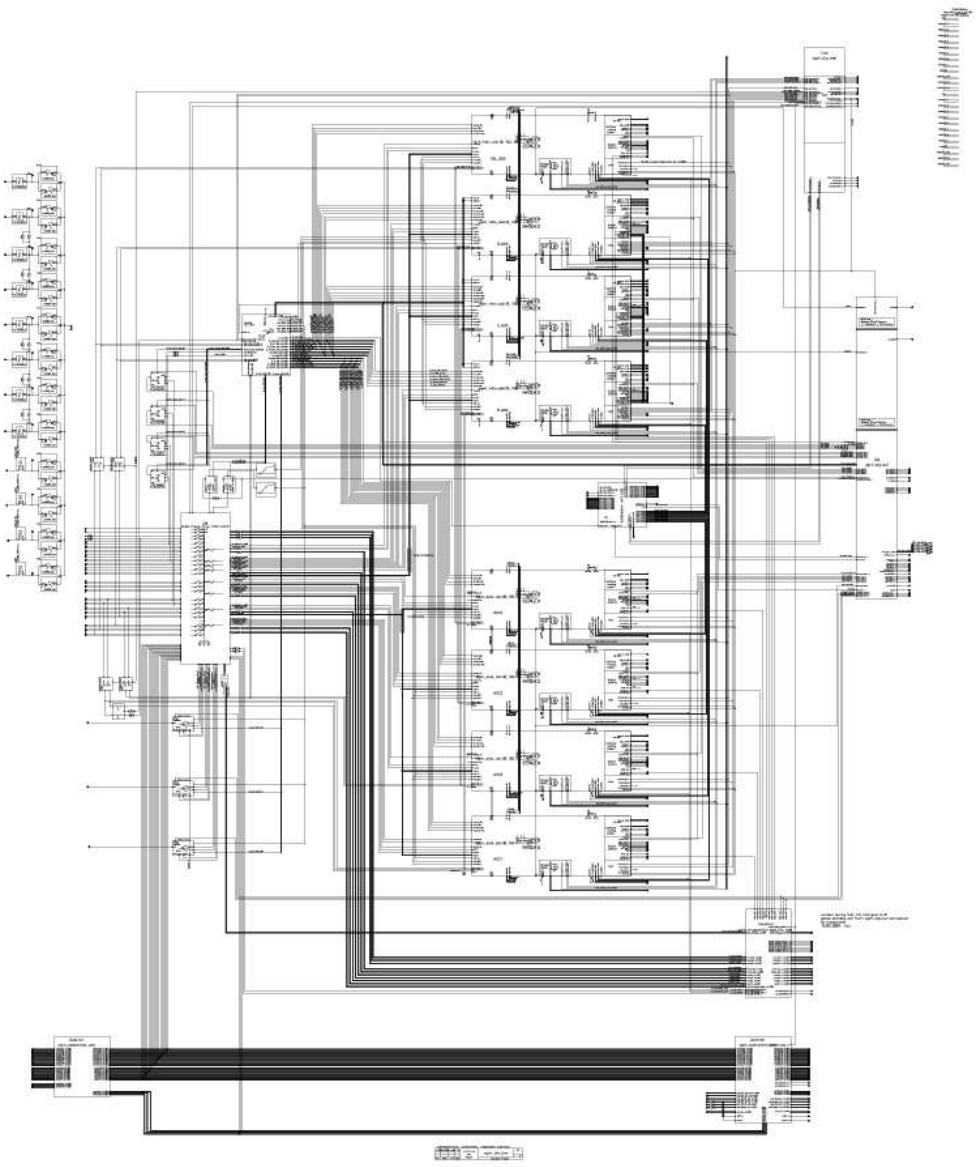

Figure 6.2: Top-level schematic of the whole analog video frontend

minimum filter cut off frequency. Nevertheless at filter off a SNDR of 50 dB is achieved for an input signal of 2MHz.

6.4 Summary of Chapter 6

The 90nm analog video frontend was designed for flat-panel displays. A power management is necessary to reduce the power waste and thus temperature on the

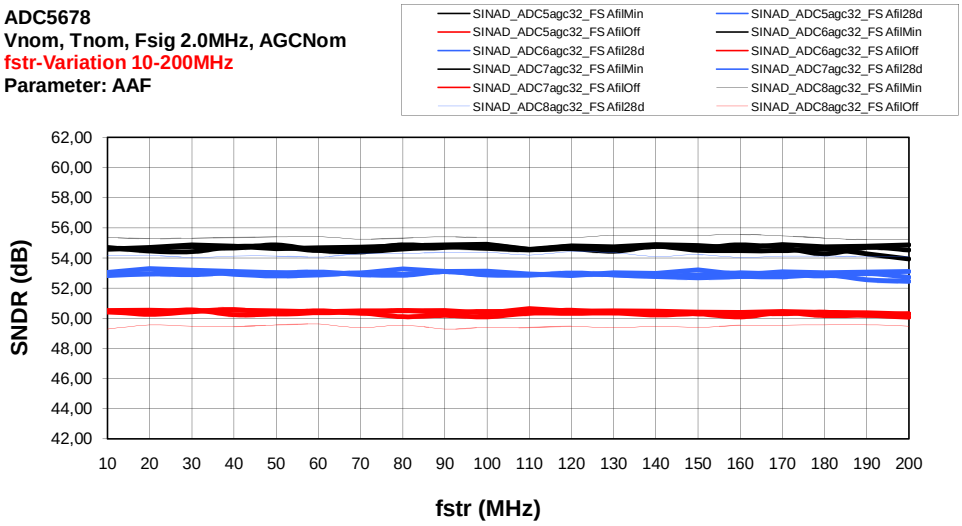

Figure 6.3: SNDR of the HD channels depending on fstrobe

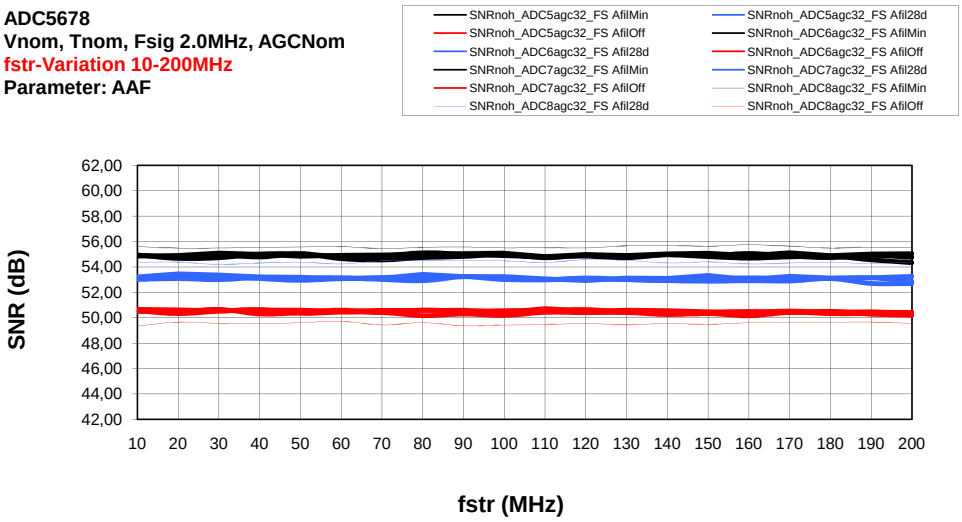

Figure 6.4: SNR of the HD channels depending on fstrobe

die. The performance was achieved by

- One sense ground for 4 inputs.
- One VSS or VDD in between two signal pins.
- Large distance from the digital to the analog inputs.
- Each channel has its own power supply.

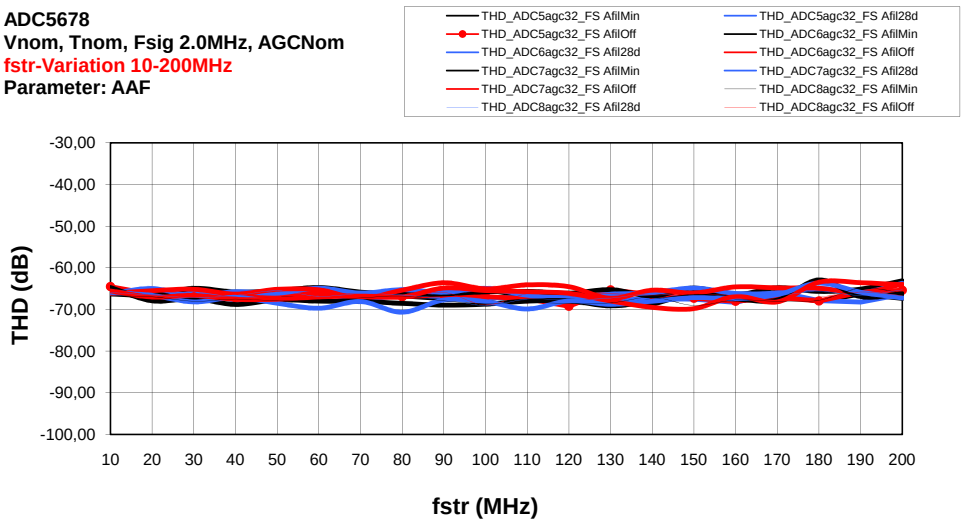

Figure 6.5: THD of the HD channels depending on fstrobe

Chapter 7

Conclusion

7.1 Research Work Overview

New architectures for analog video frontends were investigated. Amplifying and filtering of standard and high definition signals is required to improve performance and picture quality. Four different pre-processing topologies were evaluated. These structures differ in the amount of stages, THD, SNR, matching, power and area. The 4^{th} order pre-processing has much higher linearity compared to the Sallen-Key structure. This is because of the positive feedback of the Sallen-Key topology.

The input-stage uses a single ended folded cascode class AB op-amp which yields the required linearity at input signals of 80MHz and 1.8Vpp. Two input stages are used for a pseudo differential amplification of the input signal. Hence a disturber can be eliminated and the signal to noise ratio is improved. Moreover three different types of AGCs are investigated where the tapped structure has the best performance and enables the opportunity to switch the gain characteristic with only one additional resistor [12]. A comparable solution wasn´t found in the literature. The AGC with the T-network at the input is a compromise regarding noise and linearity but has the advantage of combining it with a 2^{nd} order filter which is a part of a 4^{th} or 3^{rd} order Bessel filter. The best noise performance can be achieved by splitting up the AGC on the input-stage and the combined AGC-Filter. With this structure a 3^{rd} order Bessel filter can be realized.

The 4^{th} order pre-processing was done in the 90nm technology with an SNR of 54.5dB and a THD of 52dB for a 30MHz 1Vpp signal at a filter cut off frequency of 78MHz. The power consumption is about 47.5mW for the regular power mode. In the low power mode it is reduced to 40mW at nearly the same performance. The filter can be switched off where the overall cut off frequency of 200MHz is determined by the feedback capacitor.

This so called filter off mode is needed for the connection of RGB signals of a graphic card. There a plateau phase of minimum 2ns must be fulfilled.

Further improvement was realized by designing a 65nm 3^{rd} order pre-processing with better noise, power and area. The performance of the 3 stage solution is better and the risk lower to follow this approach. The noise integrated from 0 to 1GHz is about 53.3dB for gain=1 and filter off (200MHz). This is much better than the 90nm design with an SNR of 51.5dB for the same conditions. For fulfilling this requirement the resistors were chosen very small to get an effective smaller area than in 90nm. Because of the smaller resistors the matching is in the same range as in 90nm.

The mentioned calibration technique [10] was patented and implemented for both types of pre-processing the 90nm and the 65nm. The competitors and therefore state of the art pre-processing don´t have this filter opportunity and large gain programming range which enhances the picture quality.

A 90nm and a 65nm pipeline ADC with op-amp sharing, dynamic latch with capacitive inputs and single ended reference buffer has been designed. It converts the pre-processed 1Vpp signal to the digital domain. Due to two different sampling networks for MDAC and sub-ADC the problem of matching of the sample point has been discussed. An auto zeroing pre-amplifier in front of the sub-ADC in the first stage increases the headroom for the aperture error. Furthermore it has been demonstrated that by using a 'pad noise suppression' technique the performance measurement has been improved by nearly 5 dB. For the 65nm ADC nested cascoded miller compensation technique is employed to optimize speed and power of the first and second stage. Figure 7.1 shows a comparison with recently published pipeline ADCs considering the required area. The ADC with the lowest power and area is located in the upper right corner.

7.2 Outlook on Future Work

An analog video frontend will be always required by a TV-set. By using DSM technologies speed and power can be reduced. The advantages of the technology can be used to develop ADCs with clock rates in the range of 2GHz. Analog parts can be reduced and the most of the processing like calibration has to be done in the digital domain. Only an input buffer which is used to drive the ADC will be employed. With very high clock rates it would be possible to use only the first stage of a pipeline ADC several times during a sampling phase. This is a so called cyclic ADC [28] topology.

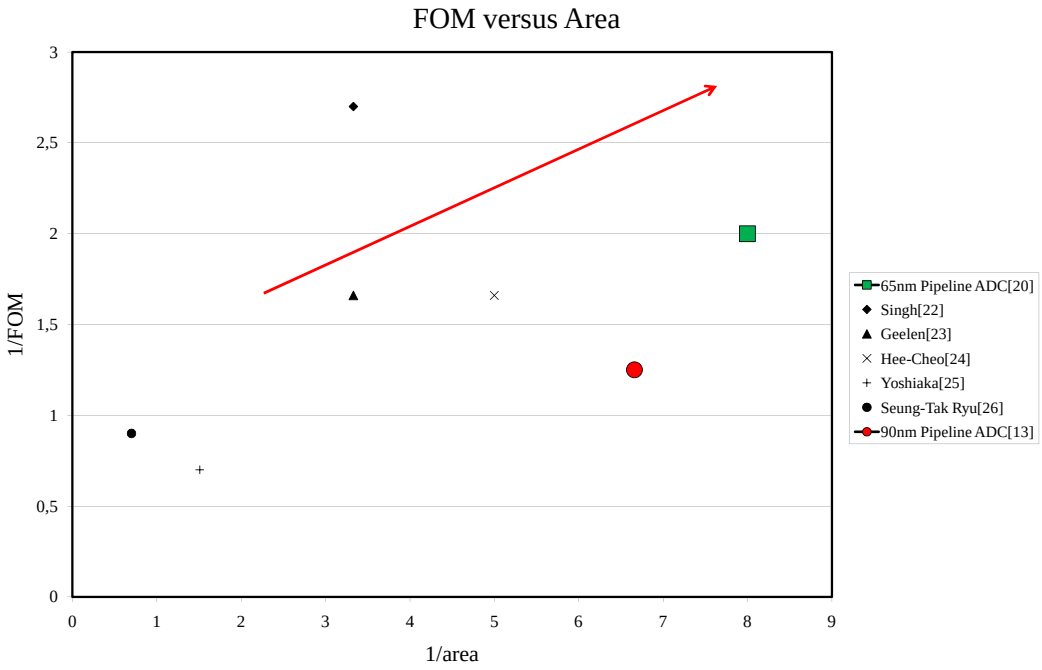

Figure 7.1: 1/FOM versus 1/area of the 65nm and 90nm pipeline ADC compared to state of the art ADCs

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