Ultra Low Power Electro-Magnetic Energy Harvesting for a Wireless Sensor Node Enhanced with RFID Functionality

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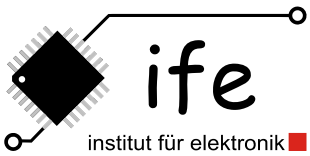

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Abstract

Evolutionary as well as revolutionary advances in miniaturization, integration, sensors, semiconductor technologies, and energy management lay the foundation for future Wireless Sensor Nodes (WSNs). There is one thing these devices will always need – energy – which nowadays mostly comes from batteries. Of course, state-of-the-art WSNs can also be supplied by harvesting energy from the ambient background, which comes with its benefits and drawbacks. The drawbacks are mainly limited power, cost and size of the harvesting device, and the absence of ambient energy sources depending on the environments in which the WSNs should operate. Thus, the upcoming challenge for future WSNs is clearly defined: get rid of the battery without losing functionality and applicability.

This thesis focuses, on the one hand, on a new approach to an electro-magnetic energy harvester and challenges with the limited power available from the RF field and its impact on the Integrated Circuit (IC) design to provide a battery-less solution for an in-tire sensor node. On the other hand, novel multifrequency Radio Frequency Identification (RFID) modules are designed to enhance this remotely powered WSN. All ICs are fabricated in an Infineon 0.13 µm low-cost CMOS process.

A Power Scavenging Unit (PSU) that converts the incoming energy from the electro-magnetic RF field into DC is the core of every remotely powered device presented in this thesis. Different structures, methods to reduce the voltage drop from the input to the output, and the influence of the number of stages on the Power Conversion Efficiency (PCE) are investigated and analyzed in detail to find the best solution for the desired applications. Furthermore the input sensitivity, a key parameter of every PSU, is determined using novel measurement methods focusing on non-expensive laboratory equipment.

In order to power an in-tire WSN from the electro-magnetic RF field new concepts are unavoidable. The only way is to cut the direct connection between the device that should be powered by the energy harvester and the output of the PSU and store the energy in an energy reservoir as long as it is sufficient to power the device. Novel design methodologies, in combination with ultra low power and energy aware design, are reflected in a power consumption of just 190 nW of the circuitry that senses the voltage in the energy reservoir and controls the desired operations. This leads to an input sensitivity of −19.7 dBm.

To enable tire identification all over the globe, an RFID tag that is capable of both HF and UHF is needed. To save chip area and costs an innovative multifrequency solution is presented. The IC is fully EPC HF and EPC Class 1 Gen 2 UHF compatible, requires only two interface pins for antenna connection and its input sensitivity of −13.5 dBm is at least comparable to a stand-alone UHF RFID transponder despite the multifrequency option.

Some slight adaptions, the combination of the energy harvester with the multifrequency RFID tag, and the integration of some already available blocks like a power management unit, an on-chip senor plus sensor interface, and an active transmitter finally lead to a remotely powered WSN enhanced with RFID functionality. This WSN fulfills all the requirements for an in-tire remotely powered WSN, while measurements have shown full operation and promising results.

Kurzfassung

Der ständig wachsende Integrationsgrad von Halbleitertechnologien, die stetige Miniaturisierung, neuartige Methoden der Integration und bahnbrechende Fortschritte im Energiemanagement legen den Grundstein für die Wireless Sensor Nodes (WSNs) der Zukunft. All diese Sensorknoten haben etwas gemeinsam – sie benötigen Energie, welche heutzutage meistens von Batterien bereitgestellt wird. Selbstverständlich können modernste WSNs mittels Energie aus ihrer direkten Umgebung versorgt werden. Jedoch hat dieses sogenannte Energy Harvesting nicht nur Vorteile. Die Nachteile spiegeln sich wider in begrenzter Leistung, Kosten und Größe des Energy Harvesting Moduls und vor allem darin, dass nicht immer die passende Energiequelle am Einsatzort verfügbar ist. Somit ist die bevorstehende Herausforderung klar definiert – Ersetzen der Batterie ohne Einbußen der Funktionalität und Anwendbarkeit.

Die vorliegende Arbeit richtet einerseits ihr Augenmerk auf die Entwicklung eines elektromagnetischen Energy Harvesters. Dabei besteht die Herausforderung darin, mit der begrenzten Leistung des elektromagnetischen Feldes auszukommen und die damit auftretenden Einflüsse auf das Integrated Circuit (IC) Design zu behandeln. Andererseits werden neuartige Multi Frequency Radio Frequency Identification (RFID) Module entworfen, um damit den WSN zu erweitern. Alle ICs sind in einem Infineon 0.13 µm CMOS Prozess gefertigt.

Herzstück eines jeden in dieser Arbeit präsentierten ICs ist die sogenannte Power Scavenging Unit (PSU), welche die Energie des elektromagnetischen Feldes in Gleichspannung umsetzt. Unterschiedliche Strukturen, Methoden um den Spannungsabfall von Eingang zu Ausgang zu verringern und der Einfluss der Anzahl der Spannungsvervielfacherstufen auf die Effizienz werden untersucht und analysiert, um die beste Lösung für die gewünschte Anwendung zu finden. Darüber hinaus werden neuartige Messmethoden für die Ermittlung der Eingangsempfindlichkeit unter Anwendung von erschwinglichem Laborequipment vorgestellt.

Neue Konzepte sind unvermeidbar, um einen WSN im Autoreifen durch das elektromagnetische Feld versorgen zu können. Es ist notwendig, die direkte Verbindung zwischen dem Gerät, das vom Energy Harvester versorgt wird, und der PSU zu trennen. Darüber hinaus muss die Energie in einem Speicher so lange gesammelt werden, bis diese ausreicht um das Gerät zu versorgen. Innovative und energiebewusste Designmethoden ermöglichen es, die Leistungsaufnahme jener Schaltung, welche die Spannung im Energiespeicher überwacht und abhängig von dieser die gewünschte Operationen steuert, auf nur 190 nW zu senken. Somit ergibt sich eine Eingangsempfindlichkeit der Schaltung von −19.7 dBm.

Um eine weltweite Reifenidentifikation zu ermöglichen wird in dieser Arbeit ein RFID-Transponder präsentiert, der sowohl HF- als auch UHF-tauglich ist. Dies innovative Lösung spart Chipfläche und Kosten, ist EPC HF und EPC Class 1 Gen 2 UHF kompatibel, benötigt nur zwei Interfacepins und verfügt über eine Eingangsempfindlichkeit von −13.5 dBm, welche trotz der Multifrequenzoption mit alleinstehenden UHF-RFID-Transpondern auf jeden Fall vergleichbar ist.

Geringfügige Anpassungen, die Kombination des Energy Harvesters mit dem Multifrequenz-RFID-Transponder und die Integration einiger schon vorhandener Blöcke – einer Powermanagement-Unit, eines Sensors plus Sensorinterface und eines aktiven Transmitters – haben letztendlich zu einem WSN mit RFID-Funktionalität geführt, der obendrein rein aus dem elektromagnetischen Feld versorgt wird und alle Anforderungen für den Einsatz innerhalb des Autoreifens erfüllt. Messungen zeigten volle Funktion und erfolgversprechende Ergebnisse.

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Hannes Reinisch

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Acronyms

ABS	Anti-lock Braking System
AC	Alternating Current
AC/DC	Alternating Current to Direct Current
ADC	Analog to Digital Converter
ASK	Amplitude Shift Keying
BAW	Bulk Acoustic Wave
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital to Analog Converter
DC	Direct Current
DC/DC	Direct Current to Direct Current
DNL	Differential Nonlinearity
DUT	Device Under Test
EIRP	Effective Isotropically Radiated Power
EMH	Electro-Magnetic Energy Harvester
ENOB	Effective Number of Bits
EPC	Electronic Product Code™
ESC	Electronic Stability Control
FOM	Figure of Merit
HF	High Frequency
I-VTC	Internal Threshold Voltage Cancellation
I-VTC-B	Internal Threshold Voltage Cancellation biased by a bias cell
I-VTC-R	Internal Threshold Voltage Cancellation biased by resistors
IC	Integrated Circuit
IEC	International Electrotechnical Commission
INL	Integral Nonlinearity
IQ	In-phase/Quadrature
ISM	Industrial–Scientific–Medical
ISO	International Organization for Standardization
LDO	Low-Dropout
LDU	Level Detection Unit
MEMS	Micro-Electro-Mechanical System
MIM	Metal-Insulator-Metal

MOS	Metal Oxide Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	n-channel MOSFET
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PCE	Power Conversion Efficiency
PMOS	p-channel MOSFET
PNP	Positive Negative Positive
PSP	Periodic S-Parameter
PSRR	Power Supply Ripple Rejection
PSS	Periodic Steady-State
PSU	Power Scavenging Unit
PTAT	Proportional To Absolute Temperature
Q Factor	Quality Factor
RC	Resistor-Capacitor
RF	Radio Frequency
RFID	Radio Frequency Identification
RS-FF	Reset-Set-Flip-Flop
RSSI	Received Signal Strength Indication
S-RAM	Static Random-Access Memory
S-VTC	Self Threshold Voltage Cancellation
SAR	Successive Approximation Register
SC	Switched Capacitor
SC-VTC	Switched Capacitor Threshold Voltage Cancellation
SMA	Sub Miniature version A
SMD	Surface Mount Device
SOC	System On Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
T-Gate	Transmission-Gate
TID	Tag Identifier
TPMS	Tire Pressure Monitoring System
TX	Transmitter
UHF	Ultra High Frequency
USA	United States of America
UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator
VSWR	Voltage Standing Wave Ratio
VTC	Threshold Voltage Cancellation
WSN	Wireless Sensor Node

Chapter 1

Introduction

Thanks to the evolution of semiconductor technologies, fully integrated Systems On Chips (SOCs) with high complexity can be developed nowadays. Also integrating a battery to supply these SOCs opens the door for a huge variety of novel applications. Fully integrated small Wireless Sensor Nodes (WSNs) realize ubiquitous computing [91].
Distributed sensor networks formed by a large number of sensor nodes – also known as Smart Dust motes – require both evolutionary and revolutionary advances in miniaturization, integration, sensor technologies and energy management [52, 110]. These advancements allow a growing number of low-cost sensor nodes and an increase of their market potential.
Micro-Electro-Mechanical System (MEMS) technology utilized to develop small sensors [109], picowatt processors [102] and voltage references [103] combined with several other ultra low power building blocks enable the design of cubic-millimeter sensor nodes that are even implantable into the human body if biocompatible enclosures are used [12, 13]. It is obvious that the applications of WSNs are manifold.

1.1 The Need for Energy Harvesting – Motivation

Despite all the revolutionary advancement of WSNs, those fully integrated and miniaturized SOCs still have a monkey on their back – the battery – which is mostly required because of the power demand of various sensors. By using energy harvesting, the lifetime of the battery can be extended. But even if this integrated battery is rechargeable, such battery powered systems are not maintenance free and therefore limited in their field of applications. On top of that, batteries are rather big, mostly toxic and expensive.

Energy harvesting has enabled the design of remotely powered systems* which are certainly already available and can be almost everywhere in our lives. From Radio Frequency Identification (RFID) tags used for access control, to those implanted in the family pet or embedded in the e-passport, to WSNs that monitor a few physical or environmental conditions – the list goes on and on and on. But nowadays these remotely powered systems offer very limited sensor capability if at all, due to the lack of power that can be extracted from the surroundings.

* Remotely powered systems do not contain a battery.

The resulting upcoming challenge is to replace the battery of a WSN by some kind of energy harvester without losing complexity of functionality. Energy harvesters can be classified by the form of energy they use to scavenge the power. A lot of energy sources are available for several types of energy harvesters or generators, whereas typical ambient energies are wind, sunlight, thermal gradient, human motion and body heat, vibration, and ambient RF energy [11, 89]. If the ambient energy is sufficient for operation a battery is not needed any longer which leads to cheaper, smaller, environment friendly and maintenance free devices.

1.2 Goals and Focus of this Work

The goal of the project iTire is to develop a remotely powered Tire Pressure Monitoring System (TPMS) including HF as well as UHF RFID applicability.

The goals of this thesis are to develop the energy scavenging unit for the remotely powered TPMS as well as the analog building blocks for RFID functionality including the concept of the interaction of the building blocks of the energy scavenger and the RFID tag.

It is evident that the energy sources of wind, sunlight, the thermoelectric effect and mechanical vibrations are not present in a non-rotating tire, thus they do not fit as power sources. Developing a WSN powered by electro-magnetic energy harvesting thus enables the deployment of a battery-less WSN in a car tire which can fit for the project iTire (see Section 1.4). A major drawback to using electro-magnetic energy harvesting to supply a TPMS is that the power which can be converted from the electro-magnetic field in a car tire is very limited as can be deduced from the channel coefficient determined by means of the channel model in [60] and channel measurements in [61], especially done for the feasibility study of supplying an in-tire WSN by extracting the power from the electro-magnetic field. For these reasons a circuit is needed to scavenge energy, as well as a circuit that releases the stored energy of an energy reservoir on demand, because the continuous power from the RF field is not sufficient to supply common pressure sensors with a power consumption in the milliwatt range.

This thesis focuses, on the one hand, on a new approach to an electro-magnetic energy harvester and challenges with the limited power available from the RF field and its impact on the Integrated Circuit (IC) design to provide a battery-less solution for an in-tire sensor node. On the other hand two different novel solutions for a two pin input multifrequency RFID transponder are developed to enable identification with the well established HF and UHF RFID readers. Furthermore one of these transponders is also combined with a part of the electro-magnetic energy harvester. The resulted remotely powered multifrequency sensing tag features an off-chip sensor interface which can be controlled using standardized EPC commands to be as flexible and easy to integrate into existing RFID systems as possible.

1.3 Chapter Outline

The first chapter introduces the project iTire and the iTire chip, which is an advanced TPMS chip mounted in the inner liner of the tire. A system overview of the iTire chip with a brief description of the building blocks is given here. The following main part of this thesis is divided into four parts:

Chapter 2: Power Scavenging Units for Wireless Sensor Nodes and RFID Transponders

As the energy scavenging unit is implemented as an electro-magnetic energy harvesting system, different electro-magnetic Power Scavenging Units (PSUs) are investigated and analyzed. So this chapter introduces into different input structures of PSUs and explains their distinctive features and operations. As it is necessary for the design of an electro-magnetic PSU, the whole system including the antenna and its matching is considered. Design challenges regarding input voltage, Power Conversion Efficiency (PCE), Quality Factor (Q Factor), and active area as well as their tradeoffs are presented. The effect of a different number of stages on the voltage multiplier is discussed and it is shown which challenges have to be accepted to design a PSU that fulfills the requirements by having the best possible performance. Furthermore, a CMOS transistor-based voltage multiplier is analyzed in detail, where AC, DC, power, and power dissipation analysis are performed. Even the main parasitics are considered to calculate the PCE. Of course, simulation as well as measurement methodologies and their challenges are presented too. The acquired knowledge is then utilized in the design of the PSUs for the Electro-Magnetic Energy Harvester (EMH) and the Multifrequency RFID tags.

Chapter 3: The Electro-Magnetic Energy Harvester

One of the major problems of remotely powered devices is the constant lack of energy. The power which can be converted from the electro-magnetic field at UHF is in the microwatt range and thus not sufficient to operate common pressure sensors or active transmitters. This chapter presents the EMH which harvests the energy from the electro-magnetic field and stores it in an energy reservoir. To achieve an adequate operating distance it is necessary to cut the direct connection between the device that should be powered by the energy harvester and the energy scavenging unit. Instead, the energy is stored in an energy reservoir as long as it is sufficient to power the load (e.g. the sensor or transmitter). The principle sounds rather easy, nevertheless a lot of problems need to be tackled when using nanoampere currents, no static supply voltages, and a standard CMOS process. Having some ultra low power building blocks beside the PSU, a time limited DC output power which is a multiple of the IC's average RF input power can be provided. Thus, WSNs performing operations where milliampere currents are necessary can be supplied just by the energy that is harvested out of the electro-magnetic field by featuring adequate operating ranges.

Chapter 4: Multifrequency for RFID

Conventional RFID systems operate at a single carrier frequency and therefore do not fit for the project iTire. As worldwide tire identification with only one chip should be possible a multifrequency solution is necessary. For this reason this chapter presents a multifrequency RFID transponder that is capable of the two mainstream frequency

ranges in passive RFID systems, HF and UHF. The presented solution is a combination of a differential HF rectifier and a single-ended UHF rectifier with the benefit of a separate optimization of each rectifier. Every RFID transponder requires several building blocks which are designed as combined ones for HF and UHF if possible. These analog blocks and their function are explained based on the chosen design implementation. HF and UHF measurements complete this chapter.

Chapter 5: The Multifrequency Sensing Tag

Equipping WSNs with RFID functionality not only enables identification and logistic applications but also an easy integration of the sensing tag into existing RFID systems. Due to the limited power which can be converted from the electro-magnetic field, state-of-the-art WSNs are mostly battery-based. As already explained before, batteries should be avoided for several reasons. Using the principle of the EMH presented in Chapter 3 as power source for the sensing functionalities and integrating it in an RFID transponder leads to the passive RFID sensing tag presented in Chapter 5. This sensing tag is also capable of both HF and UHF, whereas in this IC a differential multifrequency full-wave rectifier is implemented. Compared to the multifrequency tag presented in Chapter 4 some new building blocks need to be designed, whereas all design challenges and considerations are explained in detail. An innovative combination of two methods to lower the forward voltage drop of the rectification devices leads to a high input sensitivity of $-10.3\,\mathrm{dBm}$ (embedding the measurement losses) and a power consumption of just $7.9\,\mu\mathrm{W}$ with the on-chip temperature sensor enabled at UHF ($f = 900\,\mathrm{MHz}$).

1.4 The Project iTire and the iTire Chip

In this work different modules for the iTire chip are developed. The iTire chip is the outcome of the FIT-IT program, project iTire – Intelligent Tire. The objectives of the project iTire are to advance current TPMSs. TPMSs can be divided into two groups:

- Indirect systems and
- Direct systems.

The difference between these systems is that direct systems measure the pressure, the acceleration and the temperature with dedicated sensors. Indirect systems use information provided by the Anti-lock Braking System (ABS) and Electronic Stability Control (ESC) to calculate the tire pressure. It is clear that indirect systems are much cheaper than direct systems. Nevertheless, direct systems provide additional features which make them advantageous compared to indirect systems. For these reasons in the iTire project a direct TPMS is developed with the chip mounted on the inner liner of the tire as in [34]. According to [34], state-of-the-art direct TPMSs are wireless sensor nodes mounted on the rim. Attaching the node on the inner liner of a tire allows sensing of additional technical parameters, such as road condition, tire wearout, temperature, tire friction, side slip, wheel speed and vehicle load. They may be used for improved tracking and engine control, feedback to the power train and car-to-car communication purposes.

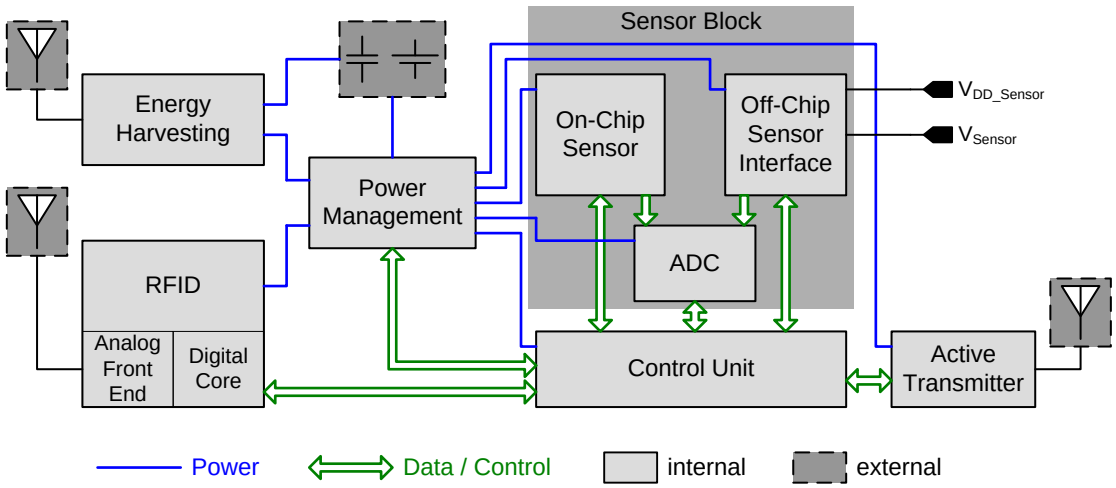


Figure 1.1: System architecture of the iTire chip

The major differences to the system presented in [34] are the communication scenarios between chip and base station and the supply of the IC. The iTire chip is a battery-less sensor node for a direct TPMS containing RFID functionality and is suitable for mounting on the inner liner of the tire.

Due to the various functions the iTire chip has a lot of building blocks. Figure 1.1 shows a system architecture of the iTire chip with the following building blocks:

- Energy harvesting
- RFID
- Power management
- Sensor block
  - On-chip sensor
  - Analog to Digital Converter (ADC)
  - Off-chip sensor interface
- Control unit
- Active transmitter

1.4.1 Brief System Description of the iTire Chip

This section briefly introduces the iTire chip and the functions of the main building blocks. Due to the different mounting position compared to state-of-the-art TPMSs, new design challenges emerge. Mechanical stress, temperature conditions and the limited allowed weight are reasons

why the chip cannot be powered by battery. Furthermore, the commonly used crystal as off-chip frequency reference for the active transmitter also cannot be used for the same prohibiting reasons as for the battery. Therefore a Bulk Acoustic Wave (BAW) resonator is used as frequency reference.

Although a battery cannot be used in its dedicated operation, the chip can also be powered by battery for test purposes. So, as power source, the battery and nearly any kind of harvesting device is possible. However, this work focuses on supplying the chip from the electro-magnetic field. Therefore the energy that can be converted from the electro-magnetic field using an energy harvester has to be sufficient to operate the IC. Due to this power limitation all designed blocks have to be as energy-aware as possible.

1.4.1.1 Energy Harvesting

The energy harvester is one way to power the chip. It has two interface pins to an external antenna which is matched to the input impedance of the EMH. The implemented energy harvesting interface is an AC/DC converter designed for ultra low power. The basic functionality of the EMH is to harvest energy from the electro-magnetic RF field and to store it in a buffer capacitor. The energy stored in this buffer capacitor is then used to power a DC/DC charge pump which transfers charge from its input to its output by means of capacitors. A local oscillator powered by the AC/DC converter clocks this charge pump and so the output voltage of the DC/DC charge pump increases and a further buffer capacitor is charged. With the energy charged in this buffer capacitor, blocks of the iTire chip, like the active transmitter, are powered to perform the dedicated operation. The functionality as well as interesting design considerations are explained in more detail in Chapter 3.

1.4.1.2 RFID Functionality

The advanced TPMS chip includes RFID functionality for tire identification. This enables easier supply chain management for the manufacturer and tire type identification in the car. If the tire can be identified by the car, important parameters for ABS, ESC or other systems can be adjusted for various tire types.

Furthermore, the chip can be supplied by the PSU of the RFID frontend. Depending on the desired operating mode, the sensor data is transmitted by back-scattering or by the active transmitter.

To enable worldwide identification with only one chip and to be as flexible as possible, a multifrequency solution is chosen. That means the chip is capable of both HF and UHF, which are the mainstream frequencies in passive RFID systems. To be compatible with commonly used systems, the chip supports the EPC HF [23] and the EPC Class 1 Gen 2 UHF [22] standards. More information about the RFID functionality and the combination of HF and UHF are given in Chapter 4.

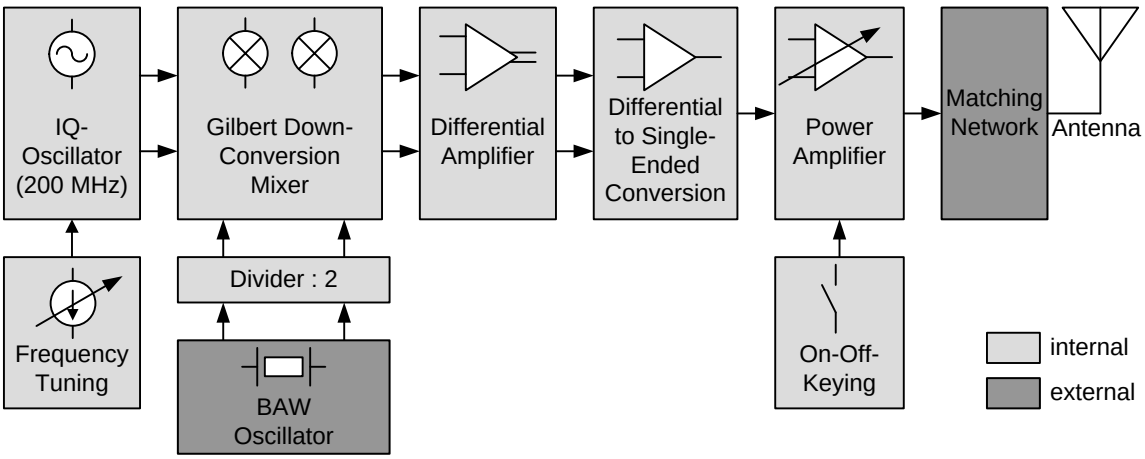


Figure 1.2: Architecture of the active transmitter

1.4.1.3 On-Chip Sensor and ADC

As stated in Section 1.4 the TPMS chip measures additional parameters. Therefore an on-chip temperature sensor is implemented. The on-chip temperature sensor uses the principle of comparing a temperature dependent to a temperature independent voltage for temperature measurement. These analog voltages have to be converted into digital to be transmitted to the base station, and thus an ADC is implemented too. Of course the design of the temperature sensor and the ADC is critical in terms of power consumption, as both have to operate if the chip is powered from an RFID base station. The on-chip sensor as well as the ADC are not in the focus of this thesis. Nevertheless they are introduced briefly in Chapter 5 to explain the basic operation principle and to name important design considerations.

1.4.1.4 Off-Chip Sensor Interface

An external MEMS device is used to measure the pressure. To supply this pressure sensor a so-called off-chip sensor interface is implemented. The energy stored in a buffer capacitor that is charged by DC/DC charge pump included in the EMH is used to supply the pressure sensor. The off-chip sensor interface is controlled by the control unit to enable the power consuming pressure sensor only if needed. The data from the external sensor is passed to the internal ADC and processed there. Of course this operating sequence is also managed by the control unit. More information on this off-chip sensor interface is provided in Chapter 3 and Chapter 5.

1.4.1.5 Active Transmitter

The purpose of the active transmitter is the transmission of the sampled sensor data. To save weight and reduce the startup time of the oscillator used in the active transmitter a BAW

BAW Transmitter	
Frequency BAW	2.1 GHz
Supply voltage	1.5 V
Output frequency	868 MHz
Supported data rates	31.25 kHz, 62.5 kHz, 125.0 kHz, and 250.0 kHz
Supported output power levels	−6.4 dBm, −1.5 dBm, 4.0 dBm, and 5.4 dBm
Current consumption	5.7 mA - 9.6 mA

Table 1.1: Key figures of the BAW-based transmitter

resonator with a frequency of 2.1 GHz is used. The active transmitter is also not in the focus of this thesis. Thus only an overview of the system architecture and a rudimentary functional description is given below.

Figure 1.2 shows the architecture of the active transmitter as explained in [38]: The external BAW resonator, a tunable source coupled multi-vibrator, which runs at approximately 200 MHz, and a down-conversion Gilbert mixer are used to generate the carrier frequency. The frequency of the external BAW resonator is 2.1 GHz and is divided by two. This signal and the output of the tunable IQ oscillator are fed to the Gilbert mixer. Frequency translation by mixing the two input signals is performed and a carrier frequency of 868 MHz is generated. The IQ oscillator can be tuned to compensate the temperature drift of the BAW and shift the carrier frequency. The mixer output is amplified, converted from differential to single-ended and then transmitted via a power amplifier. Manchester encoded data can be transmitted at an output frequency of 868 MHz. On-off-keying is used as the modulation scheme. The transmitter supports four different output power levels and four different data rates as shown in Table 1.1.

1.4.1.6 Control Unit

Contrary to common control units of SOCs, which are either represented by microcontrollers or designed in hardware description language and then synthesized in synchronous logic, the controlling of this chip is done by a state machine that is implemented in asynchronous logic. Due to the fact that the control unit is out of the focus of this thesis the complete circuit design of the control unit is omitted and its operation principle is just rudimentarily explained here.

The state machine controls the blocks of the iTire chip dependent on different voltage levels in the system. The input voltages of the different blocks are monitored and if the voltage level of a block is too low, the operating mode is also changed. The state machine can switch between five different states. These are:

- Power down,
- Idle,
- Sensor,
- Transmit data, and
- RFID.

In power down mode the input power is too low to operate the chip in one of the above listed modes. If the chip is in power down mode and excited by a sufficiently strong electromagnetic field including correct RFID commands, the RFID mode is activated. In this case the synchronous digital logic from the RFID block takes over the controlling and the asynchronous logic is turned off. The sensor, the ADC, and the active transmitter can be controlled by the RFID block.

For the following considerations no RFID signal is present, which means the RFID mode can be neglected. At low input power the chip is in idle mode. Only the EMH operates and stores some energy in the buffer capacitor as long as the energy in this buffer capacitor is sufficient to start the sensor. If the measurement procedure was successful the sensor data is stored in an on-chip memory. If the power rises even more, so that the energy in the buffer capacitor becomes sufficient to perform data transmission, the active transmitter is enabled and sensor data is transmitted to the base station. Then the whole sequence starts from the beginning. If for any reason the energy for an operation is insufficient the chip is reset and the operation starts from the beginning.

As stated in Section 1.4.1 energy awareness is very important. Therefore unused blocks are turned off completely and so no leakage can occur.

1.4.1.7 Power Management

The power management of the iTire chip ensures that the necessary power is available at the respective block and time with the required voltage level. To keep the power consumption low, the different blocks run on different supplies. Hence, four different voltage regulators are available to power the:

- Control unit,
- ADC
- Carrier generation, and
- Power generation of the active transmitter.

These different regulators are needed because the blocks listed above have different requirements by means of dynamic response, load current, Power Supply Ripple Rejection (PSRR), efficiency, and power consumption. As the power management is also out of the focus of this thesis its brief introduction ends here. More information about the power management is available in [39].

Chapter 2

Power Scavenging Units for Wireless Sensor Nodes and RFID Transponders

The original publication related to Section 2.1, 2.2, 2.3, and 2.7 is [97] (own publications). ■

This chapter presents different types of Power Scavenging Units (PSUs), shows their distinctive features, their key facts, explains how they operate and points out for which application which PSU is best suitable. Different input structures and designs with their advantages, disadvantages and areas of application are presented. Design considerations are discussed regarding the Quality Factor (Q Factor), the Power Conversion Efficiency (PCE) and the operating range. The PSU is a key block in every remotely powered device. It harvests the incoming RF power and converts it into DC power. Due to the fact that the incoming AC signal is converted into a DC signal, the PSU is also called AC/DC converter or rectifier.

2.1 Distinctive Features

The design of the PSU depends on the desired application and constraints. PSUs can be classified according to the following key features:

- Input structure: balanced or unbalanced
- Converter structure: The main differences are in the design of the converter itself – a simple rectifier whose output voltage is lower than its input voltage or a voltage multiplier with a different number of stages can be employed.
- Minimum necessary input voltage
- Minimum necessary input power – input sensitivity
- Input frequency
- Output voltage
- Output load
- Type of rectification: half-wave or full-wave

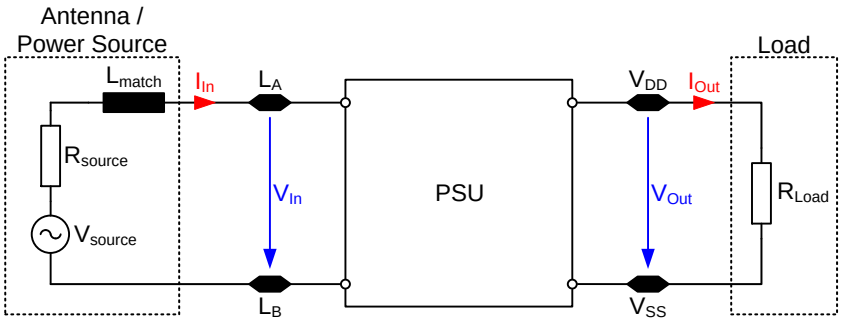


Figure 2.1: Pinout and wiring of the PSU

The features listed on the previous page depend on each other, which makes it difficult to compare PSUs. Depending on the different areas of applications the PSU can be designed with a balanced or an unbalanced input structure and a different number of stages. A balanced input is also known as differential input and an unbalanced input is known as single-ended input. These two kinds of input structures have different characteristics that can be utilized to achieve a high quality design of the PSU. The most relevant differences can be discerned in the impedance of the analog frontend and the input sensitivity of the chip. Further important factors for the decision on whether a differential or a single-ended frontend should be used are the desired operating frequency, the load conditions, and the available devices in the used process.

2.1.1 System Characteristics

In this section frequently used definitions and system characteristics are explained based on Figure 2.1. For simplicity the PSU is depicted as black box. As the PSU is used in Wireless Sensor Nodes (WSNs) the energy necessary for operation is provided by an antenna. Of course, the PSU can also be powered contact-based as is done for measurement purposes.

Input Frequency

The input frequency is the frequency of the RF input signal. Usually the input voltage is sinusoidal.

Input Voltage

V_{in} is the voltage between the input pins (usually labeled with L_A and L_B) of the PSU. The minimum necessary input voltage is defined as the voltage necessary to operate the chip. It depends mainly on the load and the design of the PSU.

Input Current

I_{in} is the current that flows into the PSU. It is usually provided by a power source or a receiving antenna.

Input Power

P_{in} is the power consumed by the PSU and can be calculated as:

$$P_{in} = V_{in} \cdot I_{in} = P_{source} \cdot (1 - |S_{11}|^2) \tag{2.1.1}$$

To provide sufficient power at the input of the PSU, the matching between the receiving antenna (or the power source) and the PSU has to be considered.

Input Sensitivity

The input sensitivity or minimum input power is the amount of RF input power sufficient to operate the chip. This operating point is also known as chip sensitivity threshold [83].

Output Voltage

V_{out} is the DC output voltage of the PSU. This voltage depends, like V_{in}, mainly on the load and the design of the PSU.

Output Current

I_{out} is the DC output current of the PSU and is of course defined by the output load and the voltage available at the output of the PSU.

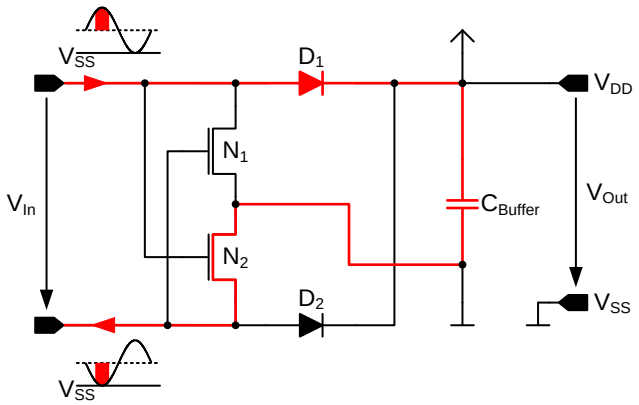
Output Load

The output load of the PSU is composed of the load caused by internal controlling circuitry and the devices or blocks supplied by the PSU.

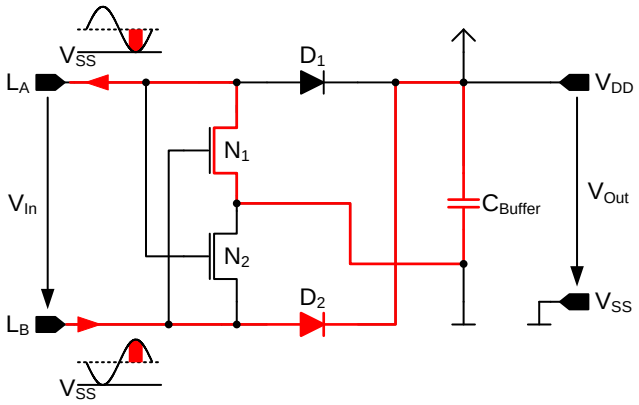
Output Power

The output power is the power consumed by the load of the PSU and therefore it can be calculated as:

$$P_{out} = {I_{out}}^2 \cdot R_{load} = \frac{{V_{out}}^2}{R_{load}} = V_{out} \cdot I_{out} \tag{2.1.2}$$



(a) Current flow during the positive phase of the input signal



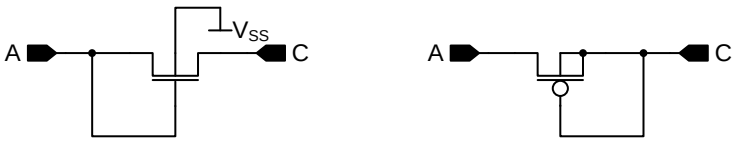
(b) Current flow during the negative phase of the input signal

Figure 2.2: Principle of the differential rectifier

2.2 Differential Input Structure

A PSU with a differential input structure is designed symmetrically. This means that the inputs L_A and L_B of the rectifier can be exchanged without influencing the function and behavior of the circuit. Figure 2.2 shows a conventional balanced rectifier that is used in state-of-the-art Radio Frequency Identification (RFID) transponders. In silicon the input structure is not fully differential due to unwanted parasitic components and effects during fabrication. The variation can be kept small by a high quality symmetrical layout with special care given to parasitics so that the influence on the circuit is marginal.

The two cross-coupled NMOS transistors N_1 and N_2 generate V_{SS}. V_{SS} is directly connected to the chip substrate and is the common mode potential of the differential input signal. The V_{SS} generation is needed to avoid substrate currents by always keeping the chip substrate at the lowest potential. The diodes D_1 and D_2 rectify the alternating input voltage and can be realized as diode-connected transistors as shown in Figure 2.3. The current flows into the buffer capacitor C_{Buffer} during both phases of the input signal, thus the designed rectifier performs



(a) NMOS (b) PMOS

Figure 2.3: Diode-connected transistors

a full-wave rectification. The current flows during the positive and the negative phase of the input signal are depicted in Figure 2.2a and Figure 2.2b, respectively.

For the following considerations V_{SS} is the reference. When the RF input signal L_A is in its positive phase, N_2 is conductive and the input pin L_B is directly connected to V_{SS}. This means V_{SS} follows the input signal L_B. The diode D_1 rectifies the positive half-wave at the input pin L_A. The current flows from the input pin L_A through D_1, charges the buffer capacitor C_{Buffer} and then flows back to the pin L_B through N_2. During the negative phase of the input signal, the complementary part of the circuit is working. The current flow is: $L_B - D_2 - C_{Buffer} - N_1 - L_A$.

The advantage of the rectifier shown in Figure 2.2, besides its simplicity, is that it works for a huge frequency range because it is developed without coupling capacitors. The disadvantage of this rectifier is that the DC output voltage is lower than the input peak voltage. Differential rectifiers based on the principle shown in Figure 2.2 are mainly used for HF RFID tags because the input voltage of the rectifier is usually higher than the required output voltage. These HF RFID tags work in the near field at 13.56 MHz. Due to the lower input frequency compared to UHF RFID systems it is advantageous to perform a full-wave rectification. Furthermore it is useful to have a structure without a coupling capacitor because the lower the frequency the higher the value of the coupling capacitor and the higher the parasitic losses. It is also not reasonable to integrate coupling capacitors with several picofarads to operate a voltage multiplier at 13.56 MHz.

PSUs with a differential input structure that need no coupling capacitors at the input and perform a voltage multiplication can be built like in [7], [30, 31], or [79]. A differential rectifier converts the RF voltage into DC and supplies a DC/DC charge pump that pumps the output voltage of the differential rectifier up to a higher potential.

A commonly used rectifier for HF using MOS devices is shown in Figure 2.4. The NMOS transistors N_3 and N_4 are diode-connected and operate as rectification diodes. The advantage of using NMOS transistors is that the source bulk diode never conducts and so no current flow is established. The drawback comes with the body effect (see (2.5.17) on page 46) which is responsible for the increase of the threshold voltage and thus the forward voltage drop.

As long as the input voltages of the diode-connected transistors N_3 and N_4 exceed their output voltage (here V_{DD}) around their threshold voltage, these rectifying transistors are conductive

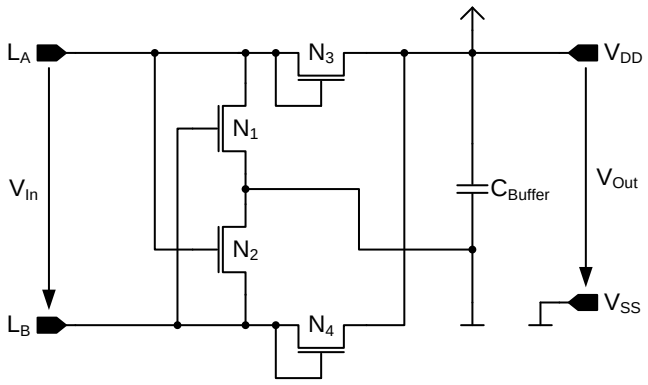


Figure 2.4: Principle of a differential state-of-the-art HF rectifier with NMOS transistors

and charge the buffer capacitor. That means the threshold voltage is directly reflected in the forward voltage drop of the diode-connected transistor. The higher the threshold voltage the lower the DC output voltage and thus the performance of the rectifier. The output voltage of a differential rectifier is calculated as:

$$V_{out} = \widehat{V_{in}} - (V_{D_{N3}}, V_{D_{N4}})_{min}\,, \tag{2.2.1}$$

where $\widehat{V_{in}}$ is the input peak voltage and $(V_{D_{N3}}, V_{D_{N4}})_{min}$ is either the forward voltage drop of N_3 or N_4, depending on which forward voltage drop is lower.

It is also possible to use PMOS transistors for the rectification, which lowers the forward voltage drop. But due to the fact that the bulk is not connected to the highest potential, a part of the charging current of the buffer capacitor is also drawn by the source-bulk-diode. It is important to take care that the current through the source bulk diode does not get too high. The higher the current through the source bulk diode, the higher the current through the vertical parasitic PNP transistor. The current gain of this vertical PNP transistor is around 100. To prevent latchup, guardrings have to be utilized in the layout.

Schottky diodes as rectification devices are also popular due to their low forward voltage drop. In a standard CMOS process additional masks are usually necessary, which makes the process more expensive. Schottky diodes are not available in the low-cost CMOS process used, and therefore the rectification devices are designed with NMOS and PMOS transistors.

2.3 Single-Ended Input Structure

A single-ended or unbalanced input structure can be identified by having one input pin connected to V_{SS}, which is the chip's substrate. Figure 2.5 shows the simplest single-ended rectifier. In contrast to the differential structure this rectifier has an asymmetrical input structure. The diode can be realized as a diode-connected PMOS transistor. An NMOS transistor as rectification diode cannot be used because the bulk of the NMOS transistor is equal to the chip

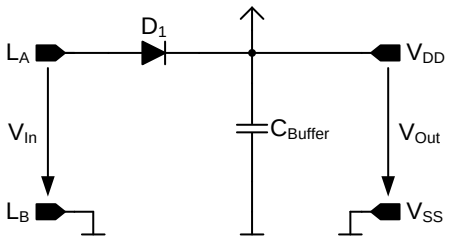


Figure 2.5: Principle of the single-ended rectifier

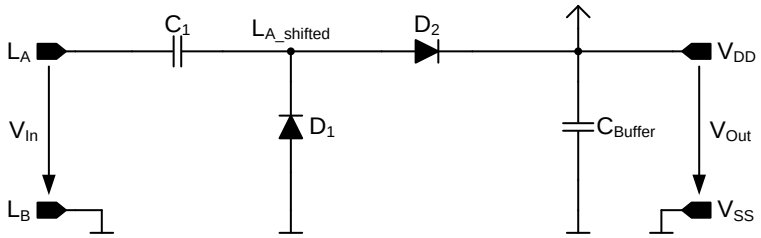


Figure 2.6: Principle of a single-ended state-of-the-art UHF Greinacher rectifier

substrate and the input voltage is alternating around the chip substrate. If the negative peak of the input voltage is too high the bulk diode conducts and so current is driven through the substrate. Figure 2.6 shows a one-stage voltage multiplier based on the Greinacher principle [36]. This circuit is the basis structure in many state-of-the-art WSNs or UHF RFID tags [3, 5, 18, 53]. The chip input L_B is directly connected to the internal reference V_{SS}. Thus the chip substrate is forced by L_B or in the other way around. The input voltage is alternating around the reference V_{SS}.

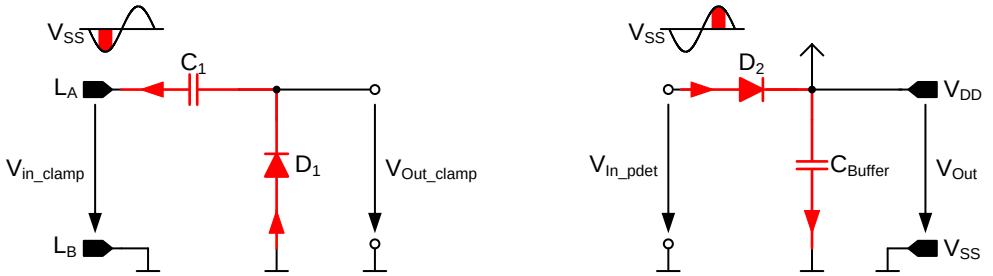
The voltage multiplier depicted in Figure 2.6 operates as a charge pump clocked by the input signal. The coupling capacitor C_1 decouples the source from the node where D_1 and D_2 are connected. To explain the basic operating principle the circuit can be separated into two subcircuits: a positive unbiased clamper (Figure 2.7a) and a peak detector (Figure 2.7b) [4]. The current flows during the positive and the negative phase of the input signal are also depicted in Figure 2.7a and Figure 2.7b, respectively. The voltages of the circuits in Figure 2.7 can be defined as:

$$V_{in_{clamp}} = V_{in} \tag{2.3.1a}$$

$$V_{out_{clamp}} = V_{in_{pdet}} \tag{2.3.1b}$$

$$V_{out_{pdet}} = V_{out} \tag{2.3.1c}$$

The vertical diode D_1 and the coupling capacitor C_1 of the clamper are used to pump the voltage to a higher potential. During the negative phase of the input signal D_1 becomes conductive. The current flows from V_{SS} through D_1, charges C_1 and then flows back to the input pin L_A. So a DC level shift is performed and $V_{out_{clamp}}$ increases. The residual negative voltage (voltage below V_{SS}) of $V_{out_{clamp}}$ lowers the theoretical maximum of the level shift. This



(a) Positive unbiased clamper (b) Peak detector

Figure 2.7: Dividing the single-ended Greinacher rectifier into two sub-circuits

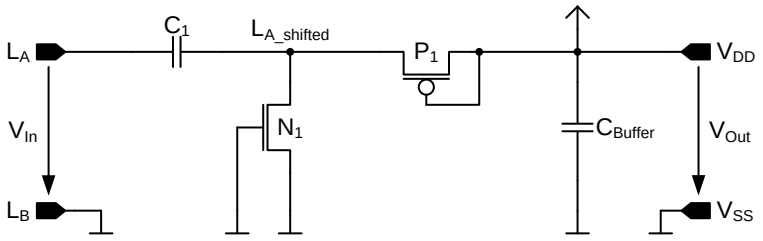
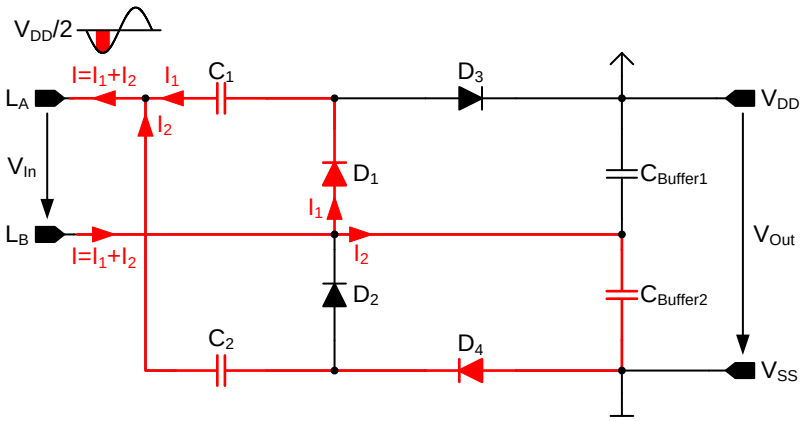


Figure 2.8: Principle of a single-ended state-of-the-art UHF Greinacher rectifier with MOS transistors

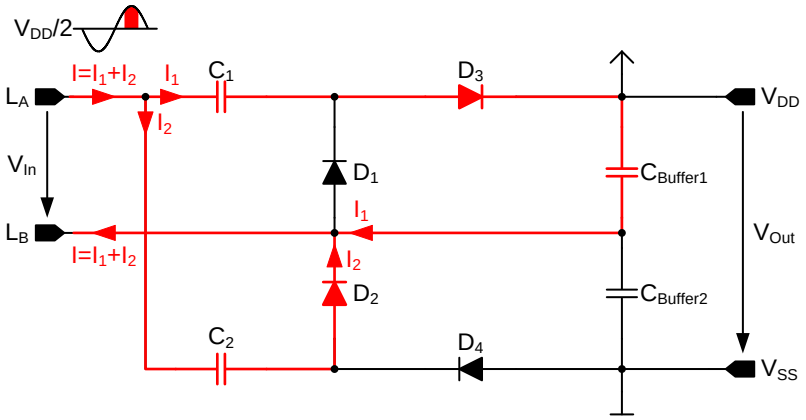
negative voltage equals the forward voltage drop of D_1 and is primarily caused by the threshold voltage of D_1. Due to this level shift substrate currents are avoided if MOS transistors are used, because the maximum residual negative voltage is in the range of a threshold voltage.
The output of the clamping circuit equals the input of the peak detector (see (2.3.1b)). The horizontal diode D_2 is conductive as long as its input voltage ($V_{in_{pdet}}$) exceeds its output voltage ($V_{out_{pdet}}$). D_2 rectifies its input signal during the positive phase of the input signal. The current flows from the input pin L_A trough C_1 and D_2 and charges the buffer capacitor C_2. The difference between the desired and the achieved $V_{out_{pdet}}$ equals the forward voltage drop of D_2. Therefore the forward voltage drop of the clamper as well as of the peak detector limits the overall performance.
Due to the fact that the buffer capacitor C_{Buffer} is charged only during the positive phase of the input signal the Greinacher rectifier in Figure 2.6 performs a half-wave rectification. The output voltage of this single-ended half-wave Greinacher rectifier is calculated as:

$$V_{out} = 2 \cdot \widehat{V_{in}} - V_{D_1} - V_{D_2}, \tag{2.3.2}$$

where $\widehat{V_{in}}$ is the input peak voltage and V_{D_X} is the forward voltage drop of the respective diode or diode-connected transistor. Figure 2.8 shows a one-stage Greinacher voltage multiplier with MOS transistors. The vertical diode is formed by a diode-connected NMOS, the horizontal diode by a PMOS transistor. This structure is often used for UHF RFID transponders whereas the number of the rectifier stages varies dependent on the DC output load [32, 108, 115].



(a) Current flow during the negative phase of the input signal



(b) Current flow during the positive phase of the input signal

Figure 2.9: Principle of a single-ended full-wave Greinacher rectifier

Of course it is possible to build a full-wave rectifier based on the circuit depicted in Figure 2.9 by using one rectifier for the positive half-wave and one for the negative half-wave of the input signal like it is done in [15, 20, 70, 82]. Of course, diode-connected MOS transistors can also be used instead of diodes. The resulting circuit is depicted in Figure 2.10.

The operating principle of the full-wave Greinacher rectifier can be explained with the help of Figure 2.9a and Figure 2.9b which depict the current flows during the negative and the positive phase of the input signal, respectively.
During the negative phase of the input signal, the vertical diode D_1 is conductive and pumps the voltage of the coupling capacitor C_1 to a higher potential. Simultaneously the horizontal diode D_4 rectifies the input signal shifted by the voltage charged in the coupling capacitor C_2 and so $C_{Buffer2}$ is charged. During the positive phase the contrary part of the circuit is working. That means the coupling capacitor C_2 is pumped to a lower potential and $C_{Buffer1}$ is charged. The resulting output voltage is the difference between the highest and lowest pumped potential. V_{SS} is connected to the lowest pumped potential to avoid substrate currents. The

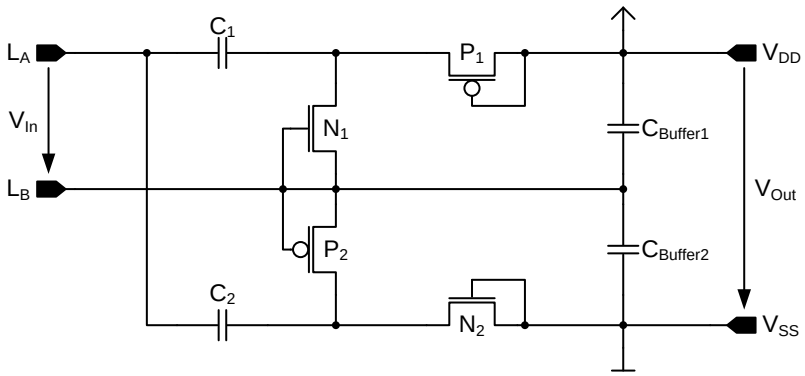


Figure 2.10: Principle of a single-ended full-wave Greinacher rectifier with MOS transistors

circuit performs a full-wave rectification and the input voltage is theoretically quadrupled because the voltage charged in the two buffer capacitors is summed up. In reality, the DC output voltage is lowered by the forward voltage drop of the four diodes. The output voltage of a single-ended full-wave Greinacher rectifier is calculated as:

$$V_{out} = 4 \cdot \widehat{V_{in}} - V_{D_1} - V_{D_2} - V_{D_3} - V_{D_4}, \tag{2.3.3}$$

where $\widehat{V_{in}}$ is the input peak voltage and V_{D_X} is the forward voltage drop of the respective diode or diode-connected transistor.

The drawback of such a full-wave voltage multiplier is that parasitic capacitances have more influence than those of a half-wave voltage multiplier with twice as many stages, because the two input pins are decoupled from the chip substrate V_{SS}, as in the case of the differential rectifier shown in Figure 2.4.

To overcome this problem a two-stage half-wave single-ended version of the PSU that produces the same output voltage can be designed using the same number of devices. Hence one pin can be saved, because one input pin is directly connected to V_{SS} and the circuit is less sensitive to parasitics.

The ripple of the output voltage is doubled compared to a differential PSU, but due to the fact that load current is in the range up to a few microampere only, it is sufficient to charge the buffer capacitor only during the positive phase of the input signal. The ripple of the output voltage of the PSU is thus negligible.

2.4 Design Considerations

For the design of a PSU, many different factors have to be considered as listed in Section 2.1. Depending on the area of application, the design limiting factors vary. In the proposed work PSUs operating from 1 MHz up to 2.45 GHz are developed to supply WSNs and RFID transponders at HF and UHF.

Usually the operating range of WSNs and RFID transponders should be maximized to increase their applicability and flexibility. In the near field the magnetic field is dominant and its field strength decays in inverse proportion to the distance R from the transmitting antenna taken to the power of three (see (2.4.1)).

$$H \propto \frac{1}{R^3} \tag{2.4.1}$$

In the far field the electro-magnetic field strength decays inversely proportional to the distance R from the transmitting antenna (see (2.4.2))[69].

$$E, H \propto \frac{1}{R} \tag{2.4.2}$$

It is obvious that the lower the field strength the less power can be extracted from the electro-magnetic field. For this reason systems with a high operating range function in the far field.

The rectifier supplying the RFID transponder at HF (13.56 MHz) is powered by the energy transferred via magnetic coupling from the reader antenna to the transponder antenna. Due to the fact that for the desired application the maximum operating range at HF is secondary and the Q Factor is between 20 to 30, the input voltage is not a limiting factor for this rectifier.

2.4.1 The Quality Factor

The rectifiers used for WSNs and RFID transponders at UHF should achieve high operating distances. UHF (860 MHz to 965 MHz and 2.45 GHz) RFID transponders suffer from a permanent lack of energy. The loaded Q (Q of the transponder antenna connected to the chip) is usually low (< 10) and therefore not only the power that can be extracted from the electromagnetic field but also the voltage available at the input are limiting factors. Rectifiers for the use in WSNs are also limited by the available input power and input voltage due to the mostly desirable maximum operating distance.

With regard to the Integrated Circuit (IC) itself, the unloaded Q can be calculated by the equivalent circuit of the IC. It depends on the input impedance of the IC, which is dominated by the impedance of the analog frontend, mainly by the PSU. The Q nomenclature comes from the matching theory where the unloaded Q Factor (Q_0) is the Q Factor of the resonator (capacitor and/or inductor) itself, the external Q Factor (Q_{ex}) is the Q Factor of the circuitry connected to the resonator and the loaded Q Factor (Q_L) is the resulting Q Factor. (2.4.3) shows this behavior.

$$\frac{1}{Q_L} = \frac{1}{Q_0} + \frac{1}{Q_{ex}} \tag{2.4.3}$$

When talking about the Q Factor, the loaded Q Factor (Q_L) is most often referred to:

$$Q = Q_L \tag{2.4.4}$$

The higher Q the higher the voltage gain of the input signal and the higher the peak voltage present at the input of the PSU. Due to the fact that a distinct RF input voltage is necessary

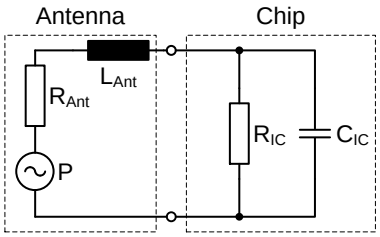


Figure 2.11: Equivalent circuit of the transponder

to operate the PSU, the Q Factor of the PSU should be maximized by keeping parasitics, and thus losses as low as possible. The most fundamental definition of the Q Factor as stated in [63] is:

$$Q = \omega \cdot \frac{\text{energy stored}}{\text{average power dissipated}} \tag{2.4.5}$$

However the higher Q the lower the bandwidth of the system. Due to the fact that a distinct RF input voltage is necessary to operate the system the Q Factor of the harvesting unit should be maximized by keeping the parasitics and thus the losses as low as possible.

With respect to the whole system, the source, which is an antenna or a power source, is connected to the load, which is the IC. The equivalent circuit of the source can be built up by a power source in series with a resistor and an inductor, representing the antenna's or the source's impedance. A resistor in parallel with a capacitor represents the IC. To achieve resonance at HF an additional capacitor is needed that is in parallel with the IC's capacitor. This is because the capacitance is too big and therefore cannot be integrated.
The equivalent circuit of an antenna connected to the PSU is shown in Figure 2.11.

Computing the energy stored in the energy reservoir and the average power dissipated by the resistor results in (2.4.6) for Q:

$$Q = \frac{R_{IC}}{X_{C_{IC}}} = \omega_0 \cdot R_{IC} \cdot C_{IC} \tag{2.4.6}$$

The lower the current consumption of the PSU the higher the parallel resistor R_{IC} is and thus the higher the Q Factor is. One drawback of a high Q is the inversely proportional relation to the operating bandwidth as stated in (2.4.7).

$$Q = \frac{f_c}{f_2 - f_1} \tag{2.4.7}$$

The Q Factor of an inductively coupled system usually has to be limited by an additional resistance. At UHF the Q Factor of the transponder antenna dominates the loaded Q Factor due to the low Q Factor of the used material.

symbol	description
P_r	available power at the receiving antenna
P_t	powered delivered to the transmitting antenna
$G_t(\theta, \varphi)$	gain of the transmitting antenna in the direction (θ, φ)
$G_r(\theta, \varphi)$	gain of the receiving antenna in the direction (θ, φ)
λ	wavelength of the transmitted signal
R	distance between the transmitting and the receiving antenna

Table 2.1: List of symbols for (2.4.9)

2.4.2 Power Conversion Efficiency and Operating Range

The main aim in the design of a PSU is a high PCE which is defined by the ratio of output power to input power as shown in (2.4.8).

$$PCE = \frac{P_{DC\_out}}{P_{RF\_in}} \tag{2.4.8}$$

The PCE is one of the performance parameters of a PSU which depend on various factors like:

- Available input voltage
- Available input power
- Loaded Q factor
- Input frequency
- Used process: available components, breakdown voltage, threshold voltage
- Desired output voltage
- Output load

The PCE mainly depends on the circuit design, the operating frequency, the output load and the output voltage of the circuit.

As stated in (2.4.2) the electro-magnetic field strength decreases with the distance between the transmitting antenna and the receiving antenna. The available power at the receiving antenna can be calculated by the Friis transmission equation (see (2.4.9)) if the system operates in the far field.

$$P_r = P_t \cdot G_t(\theta, \varphi) \cdot G_r(\theta, \varphi) \cdot \left(\frac{\lambda}{4\pi R}\right)^2 \tag{2.4.9}$$

A description of the symbols is given in Table 2.1.

The input power can be split into the power consumption by the DC load and the power dissipation by the losses caused by the high-frequency switching and by additional circuitry (for instance biasing).

$$P_{RF\_in} = P_{DC\_out} + P_{loss} \tag{2.4.10}$$

Inserting (2.4.10) in (2.4.8) results in (2.4.11).

$$PCE = \frac{P_{DC\_out}}{P_{DC\_out} + P_{loss}} \tag{2.4.11}$$

It is obvious that the lower the DC output power the more the PCE depends on this power dissipation (P_{loss}). The DC output power is calculated using (2.4.12).

$$P_{DC\_out} = V_{out} \cdot I_{out} = \frac{V_{out}^2}{R_{load}} = (n \cdot V_{in} - V_D) \cdot I_{out} = \frac{(V_{in} - V_D)^2}{R_{load}} \tag{2.4.12}$$

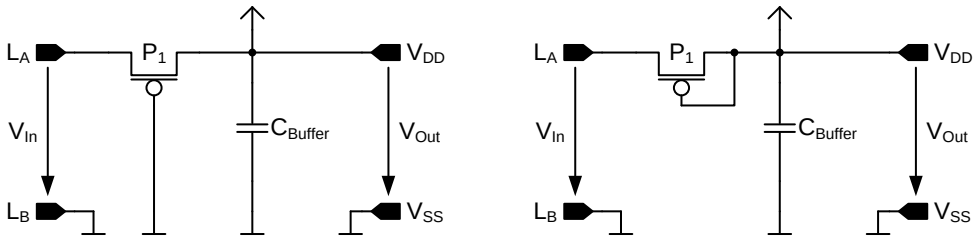
In (2.4.12) V_D symbolizes the forward voltage drop of the rectification devices and n symbolizes the multiplication factor of the input voltage if a charge pump or voltage multiplication circuit is applied.

What can be seen from (2.4.9) is that the lower the power necessary for operation the lower the transmitted power and/or the higher the operating range can be. If the base station transmits at a distinct operating frequency, assumed to be the maximum power allowed by national regulations, the operating range depends only on the antenna gains and the power necessary for operation. Hence what can be done in the chip design to maximize the operating range is to minimize the power necessary for operation. That means the PCE increases again. So this is the reason why the PCE is often used as the key parameter. But due to the fact that the PCE strongly depends, among other things, on the output load and output voltage, the performance of a PSU cannot be specified with the PCE alone.

For the design of a PSU the necessary input power at a desired output voltage and output load is significant. The influence of additional devices of the chip also has to be considered. The shunt that is used to protect the circuit from harmful voltages is usually (also in this work) placed in parallel to the input pins L_A and L_B. It has a major influence on the input impedance. The parallel chip resistance decreases and the parallel chip capacitance increases. Thus the Q Factor decreases and the input sensitivity too. Additionally, due to the fact that this remotely powered chip cannot be designed without considering the whole system, which is in this case the chip connected to the antenna, care has to be taken that a suitable antenna design (matching, Q Factor, bandwidth) is possible.
The only thing one can do is to design the rectifier with the highest efficiency to meet the specification.

2.4.3 Transistor Size and Forward Voltage Drop

To achieve a high performance of the PSU the parasitics and the forward voltage drops of the rectification devices have to be small.
One important tradeoff in rectifier design for high frequencies is the size of the transistors versus the parasitic capacitance [15]. The smaller the transistor's size, the smaller its parasitic capacitance. The parasitic capacitances cause losses because a part of the incoming power is required to charge and discharge these parasitic capacitances. The higher the input frequency



(a) gate of the PMOS transistor at V_{SS} (b) gate of the PMOS transistor at V_{DD}

Figure 2.12: Simplest single-ended rectifier with PMOS transistor

the higher the losses. Decreasing the transistor size causes a higher channel resistance. That means the higher the output current the higher the voltage drop of the particular rectification device. The forward voltage drop of a diode-connected transistor depends on its threshold voltage, its size, and its layout. Size and layout are responsible for the parasitics. The forward voltage drop effects the PCE and thus the input sensitivity. For this reason designers modify rectifiers with various techniques to lower the forward voltage drop of the diodes in the rectifiers or voltage multipliers.

2.4.4 Methods to Lower the Forward Voltage Drop of the Diode-Connected Transistors

There are a few possibilities to lower the forward voltage drop of diode-connected transistors. It starts with the correct choice of the devices used for rectification. The devices should have low leakage, few parasitics, a low on-resistance and a low threshold voltage. Then the trick is to bias the gate of the transistor, which should operate like a diode in such a way that the forward voltage drop is minimized.

Methods to lower the forward voltage drop of the diode-connected transistors are named differently. In this work these methods are all indicated with the generic term Threshold Voltage Cancellation (VTC) and different prefixes as well as suffixes.

It is obvious that every additional circuit to control the gates of the transistors operating like diodes draws some current. In a system where every nanoampere is crucial for the PCE, complex input sensitivity control circuitries are not feasible.

2.4.4.1 Gates of the Diode-Connected Transistors at a Fixed Potential

To keep the current consumption of the circuitry used to lower the forward voltage drop low, designers sometimes connect the gates of the transistors operating like diodes to a fixed potential, as done in [56]. This scheme is named S-VTC which stands for **S**elf **VTC**. In fact the transistors are operating as switches and not as diodes anymore. Taking the simplest single-

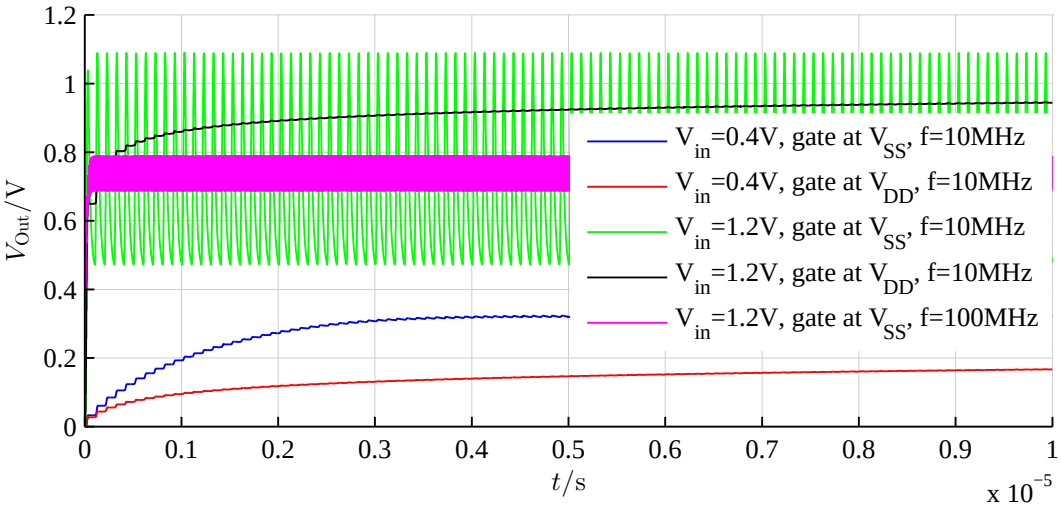


Figure 2.13: Transient behavior of the single-ended rectifiers of Figure 2.12

ended rectifier as an example, where the gate of the PMOS transistor is connected to V_{SS}, it becomes apparent that this rectifier, shown in Figure 2.12a, is advantageous in terms of PCE and forward voltage drop as long as the input amplitude is in the range of the threshold voltage of the transistor that should operate like a diode (P_1). Figure 2.13 shows the transient behavior of the output voltages of two single-ended rectifiers with PMOS transistors, one with the gate connected to V_{SS} and the other with the gate connected to V_{DD} as shown in Figure 2.12a and Figure 2.12b, respectively. The rectifiers are excited with a sinusoidal signal with amplitudes of 400 mV & 1.2 V and frequencies of 10 MHz & 100 MHz. The values of the buffer capacitors and the load resistors are chosen to be 100 pF and 1 MΩ, respectively. The red, blue, and black curves in Figure 2.13 show values plotted at 10 MHz. These curves would have less ripple if plotted at 100 MHz because the lower the frequency of the input signal, the higher the ripple of the output voltage.

Depending on the input voltage of the chip the transistor P_1 of the rectifier shown in Figure 2.12a behaves either like a diode as long as the input voltage is in the range of the threshold voltage or like a switch if the input voltage is significantly higher than the threshold voltage. If the input amplitude of this rectifier depicted rises significantly higher than the threshold voltage of P_1, P_1 is still conductive if the input amplitude decreases after its peak again (see green and magenta curves in Figure 2.13). That means that current is drawn out of the buffer capacitor again due to the high gate overdrive voltage of P_1. As a consequence, the DC output voltage decreases and thus the average DC output voltage does not rise anymore, which in addition to the losses produced by the non-ideal devices and connections causes a lower PCE (compare (2.4.11) and (2.4.12)). Thus, for higher input voltages (in Figure 2.13 1.2 V) the average output voltage of the rectifier in Figure 2.12a is always lower than the average output voltage of the rectifier in Figure 2.12b.

Going one step further and applying this S-VTC to the Greinacher voltage multiplier the scenario gets even worse. An NMOS transistor is used as a vertical diode and a PMOS

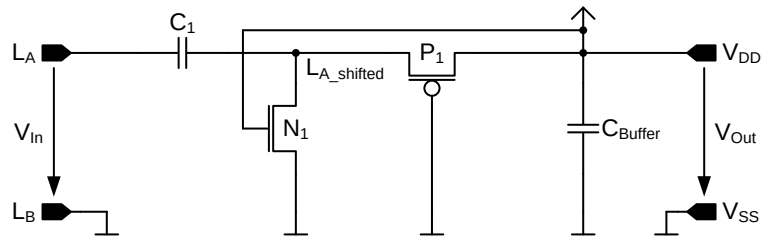


Figure 2.14: Principle of the single-ended Greinacher rectifier with S-VTC

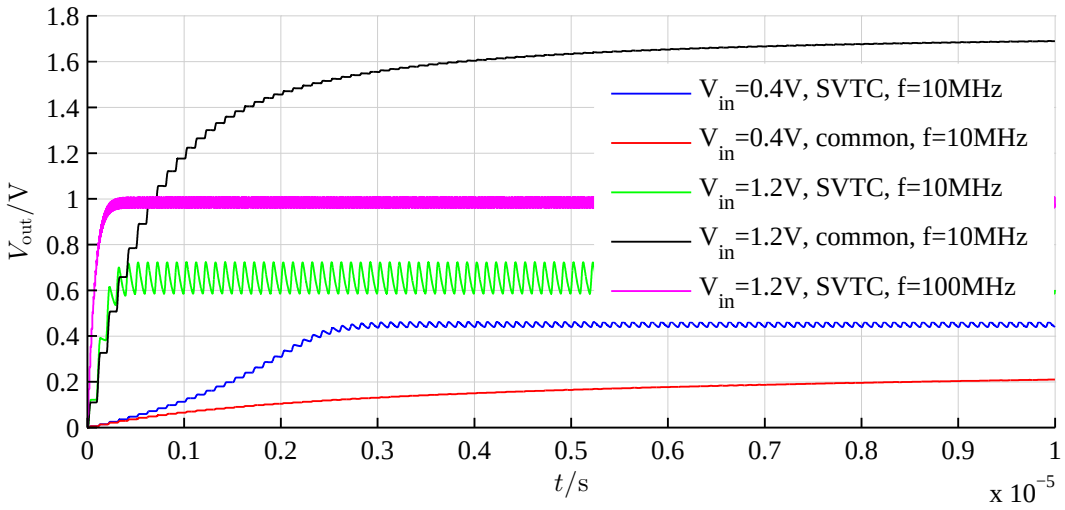


Figure 2.15: Transient behavior of the single-ended rectifiers of Figure 2.8 and Figure 2.14

transistor is used as a horizontal diode. The circuit shown in Figure 2.8 is the common configuration of a voltage multiplier for the simple reason that this configuration of NMOS and PMOS achieves good performance without complexity. Applying the S-VTC proposed in [56] to the Greinacher rectifier in Figure 2.8 results in Figure 2.14. Figure 2.15 shows the transient behavior of the output voltages of two Greinacher voltage multipliers, one with the common configuration of the gates of the MOS transistors as shown in Figure 2.8 and one with the gate of the NMOS transistor connected to V_{DD} and the gate of the PMOS transistor connected to V_{SS}. The rectifiers are also excited with a sinusoidal signal with amplitudes of 400 mV & 1.2 V and frequencies of 10 MHz & 100 MHz. The values of the buffer capacitors and the load resistors are chosen to be 100 pF and 1 MΩ, respectively. Comparing the red and the blue curves it can be seen that for low input voltages (in Figure 2.15 400 mV) the S-VTC configuration performs better. As in the case of the simple one transistor rectifier in Figure 2.12, the red, blue, and black curve in Figure 2.15 show values plotted at 10 MHz. These curves would have less ripple if plotted at 100 MHz because the lower the frequency of the input signal, the higher the ripple of the output voltage.

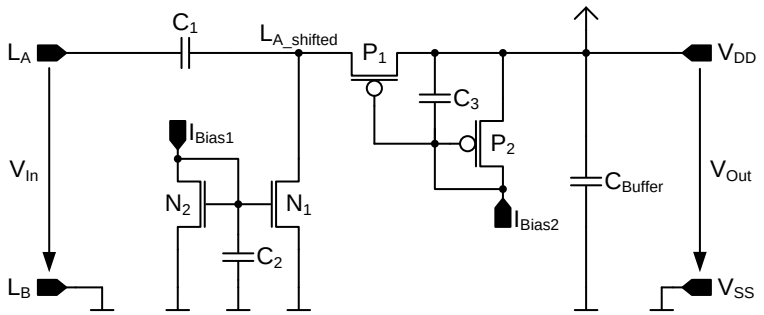


Figure 2.16: Principle of the single-ended Greinacher rectifier with I-VTC

If the amplitude of the input signal rises significantly higher than the threshold voltage of the transistors used, P_1 as well as N_1 in Figure 2.14 are conductive, even if it is not desired. P_1 behaves like P_1 of the common Greinacher rectifier presented in Section 2.3 and shown in Figure 2.8, and N_1 is also conductive during the positive phase of the input signal if V_{DD} exceeds its V_T. So there is a direct path between the two input pins and excessive energy is dissipated. Of course this behavior can be utilized as a self voltage limiting circuit as in [56]. But the DC output voltage has a huge ripple at high input voltages, and its absolute value is very inaccurate and frequency dependent, which becomes evident by comparing the green and magenta curves in Figure 2.15. Generally, for higher input voltages the common configuration (black curve in Figure 2.15) achieves a higher DC output voltage than the S-VTC configuration (green and magenta curves in Figure 2.15). It is common knowledge that the threshold voltage changes due to drain current, temperature and process variation. So it becomes obvious that except for those applications where the input voltage stays in the range of the threshold voltage of the transistors operating like diodes, this S-VTC is applicable but not useful for mass production.

2.4.4.2 Gates of the Diode-Connected Transistors Biased Depending on their Input Signal

Another technique is to bias the gates of the transistors operating like diodes related to the signal they rectify. The trick is to get a diode that is conductive as soon as the input is higher than the output. Assuming that a transistor becomes conductive if V_{GS} reaches its V_T the forward voltage drop of a diode-connected transistor can be significantly reduced by biasing the gate with $V_{GS} = V_T$. This idea is not new, different principles are published in [81, 82, 107, 108]. Therefore the designation is also adopted from the published material. Due to the fact that the VTC is done by additional devices that have to be placed near the rectifying transistors, the scheme is named I-VTC which stands for **I**nternal **VTC**.

Biasing the gate with $V_{GS} = V_T$ can be done quite easily. An additional biased diode-connected transistor is matched to the transistor whose forward voltage drop should be lowered. As depicted in Figure 2.16, the gate potential of the NMOS transistor is increased by one V_T and the gate potential of the PMOS transistor is decreased by one V_T compared to the conventional

diode-connected transistor. At startup performance is similar to the conventional rectifier because a supply voltage of a few hundred millivolts is necessary for this technique to become effective, and then the performance is boosted. The gate potential of the NMOS transistors rises only if V_{DD} rises. The gates of the PMOS transistors are at V_{SS} at startup. If the buffer capacitor C_3 is applied between the PMOS gates and V_{SS} the PMOS gate potential increases much more slowly than V_{DD}, and so the forward voltage drop is lowered only if V_{DD} begins to increase.

Generation of the Bias Currents of the Diode-connected Transistors

As published in [82], high ohmic resistors are used to limit the current through the bias transistors (P_2, N_2 in Figure 2.16). This technique is named I-VTC-R which stands for **I**nternal **VTC** biased by **r**esistors. It works quite well but high ohmic resistors either occupy a lot of chip area or a process with high ohmic polysilicon is necessary. Thus, it is not feasible to implement high ohmic resistors in a low-cost product like an RFID transponder.

The best matching of N_1 to N_2 and P_1 to P_2 is achieved if the transistor's geometries and drain currents are equal. These bias currents have to be considered in the PCE and therefore they have to be much lower than the load current. That means there is no perfect matching, however the PCE, which is of course affected by the currents drawn by the bias transistors, increases. For a typical power consumption of an RFID transponder, which is in the range of 2 µW to 10 µW DC load at a typical supply voltage of 1 V, bias currents in the range of 10 nA to 100 nA are sufficient.
It is also obvious that this VTC consumes additional power (P_{VTC}) and so it is only advantageous as long as the PCE is increased at the desired specifications. Considering P_{VTC} the PCE can be calculated using (2.4.13).

$$PCE = 1 - \frac{P_{loss} + P_{VTC}}{P_{DC\_out} + P_{loss} + P_{VTC}} \tag{2.4.13}$$

To get rid of the high ohmic resistors in this work a bias cell is used to provide the bias currents for the VTC as done for one rectifier, which is described in Chapter 4. Using a bias cell yield the identifier I-VTC-B, which means **I**nternal **VTC** biased by a **b**ias cell.

Particularly in those cases where a bias cell is required for system operation anyway, it is reasonable to use this bias cell to provide the current for the bias transistors. Of course, the rectifier provides the supply for the bias cell, which means that an output voltage of at least a few hundred millivolts ($V_{D\_sat} + V_T$) in the process used are necessary for this technique to become effective. Nevertheless, as long as the bias cell is not working there is nearly no additional power consumption.

The PSU behaves similarly no matter if the I-VTC-R or the I-VTC-B is applied, because the diode-connected transistors (N_2 and P_2) need a $V_{GS} = V_T$ to become conductive. Additionally, V_{D_sat} is needed for the bias transistors.
The voltage across the bias resistor determines the current through the bias transistor. A typical value for a bias resistor is approximately 10 MΩ. That means to a achieve a current of 10 nA through the bias resistor, which is the least amount necessary to notice an improvement

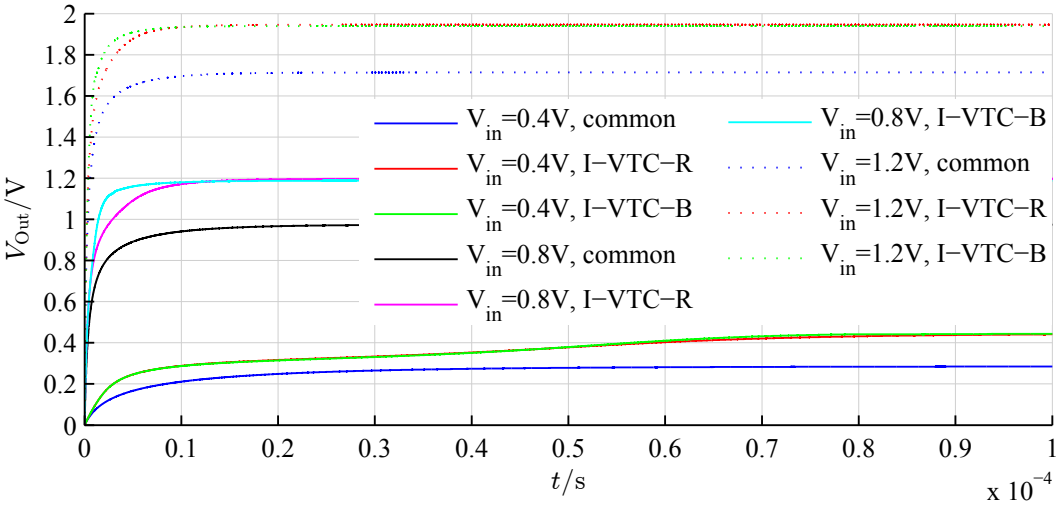


Figure 2.17: Transient behavior of the single-ended rectifiers of Figure 2.8 and Figure 2.16

of the forward voltage drop, the voltage across the bias resistor has to be 100 mV. So the supply voltage necessary to operate the VTC is nearly the same, no matter if a bias cell or high ohmic resistors are used to limit the current through the bias transistors.

Figure 2.17 shows the transient behavior of the output voltages of the Greinacher voltage multipliers in common configuration as shown in Figure 2.8 and with the I-VTC-R & I-VTC-B scheme according to Figure 2.16. The rectifiers are excited with a sinusoidal signal with amplitudes from 400 mV to 1.2 V and a frequency of 100 MHz. The values of the buffer capacitors and the load resistors are chosen to be 100 pF and 1 MΩ, respectively. To do a reliable comparison between the I-VTC-R and the I-VTC-B scheme the value of the bias resistor is changed for every input voltage in such a way that the bias currents are equal for both schemes. Thus, the value of the bias resistor is set to: 2.5 MΩ at $V_{in} = 400$ mV, 12 MΩ at $V_{in} = 800$ mV, and 22 MΩ at $V_{in} = 1.2$ V. Therefore the output voltages in steady state are also nearly equal. At higher input voltages (800 mV & 1.2 V in Figure 2.17) the output voltages of the voltage multipliers with I-VTC-B (magenta and dotted green curves) increase faster because the gate of P_1 is at a lower voltage level compared to the voltage multiplier with I-VTC-B.

Due to the linear behavior between voltage across the resistor and current through it compared to the nearly supply voltage independent current provided by the bias cell, the PCE at higher output voltages decreases if resistors instead of a bias cell are used to bias the transistors P_2 and N_2 in the circuit shown in Figure 2.16. However, if the bias cell is not in need of any other circuitry from the system the PSU is operating in, the power consumption of the bias cell, especially at startup, has to be taken into account. In this case a higher input sensitivity can be reached using high ohmic bias resistors. Nevertheless, area-consuming resistors are not an option either for the RFID transponders or the WSNs presented in this work.

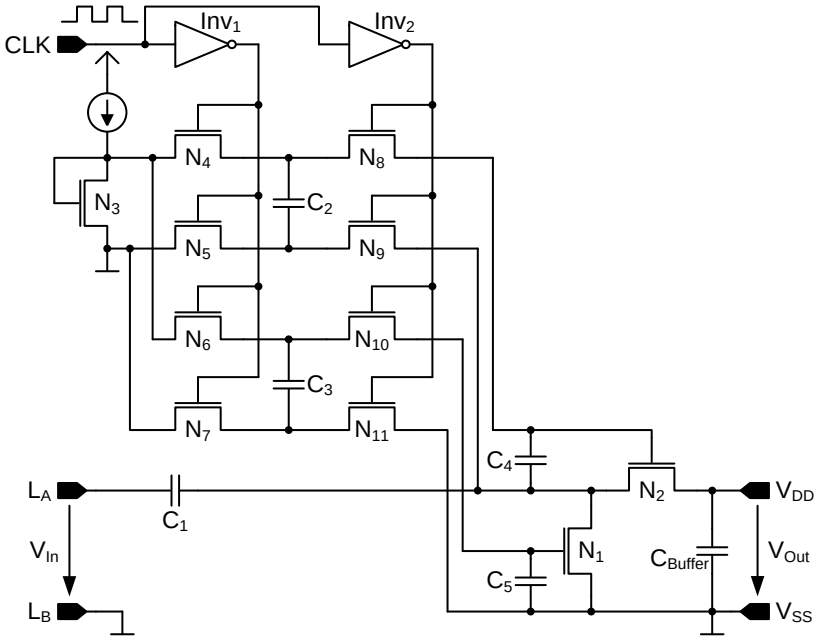


Figure 2.18: Principle of the single-ended Greinacher rectifier with SC-VTC

2.4.4.3 Gates of the Diode-Connected Transistors Biased Using a Switched Capacitor Technique

In [107] and [108] a switched capacitor technique was proposed which biases the rectifying transistors with $V_{GS} = V_T$. The principle of this scheme, published in [107], is shown in Figure 2.18 and named SC-VTC, which means **S**witched **C**apacitor **VTC**, because a switched capacitor technique is used to apply a bias voltage (in [107] and [108] externally generated) at the gates of the rectifying transistors.

Figure 2.18 shows the principle of a one-stage voltage multiplier with the switched capacitor bias voltage distribution circuit. In this circuit the horizontal diode is also built up by an NMOS transistor because a single generated bias voltage to lower the forward voltage drops is distributed to all rectifying transistors. For every stage eight pass transistors (N_4 to N_{11}) and four capacitors (C_2 to C_5) are necessary to provide the bias voltage at the gates of the horizontal and vertical transistors (N_1 and N_2). If the input signal CLK is "low", C_2 and C_3 are charged to the threshold voltage of N_3. This charge is then transferred to C_4 and C_5 if the signal CLK changes from "low" to "high".

The bias current for N_3 is also generated by a bias cell as in the I-VTC-B scheme. The measurement results in [108] are determined using an external pulse generator and a DC voltage generator. That means the power consumption of the bias cell and the pulse generator are not considered. This scheme works for supply voltages that are one V_T higher than the bias voltage. However, if supplying this circuit by the rectifier itself, the results will dramatically worsen compared to the results determined in [107, 108]. The function and startup behavior is like that of the I-VTC scheme.

The power consumption of the I-VTC increases with the number of rectifier stages because one additional bias transistor drawing bias current is necessary for each transistor operating as diode. The power consumption of the SC-VTC presented in [108] is nearly constant because the bias voltage is generated by only one biased diode-connected transistor and distributed by the switched capacitor circuit with a frequency of 100 Hz whose current consumption is marginal. The leakage of the distributing capacitors should be also low compared to the bias current. In summary, for a high number of stages the SC-VTC can be advantageous with regard to PCE but it is a lot of overhead, an additional oscillator is needed and every additional frequency in a system induces noise.

2.4.5 Number of Stages

The number of stages mainly depends on:

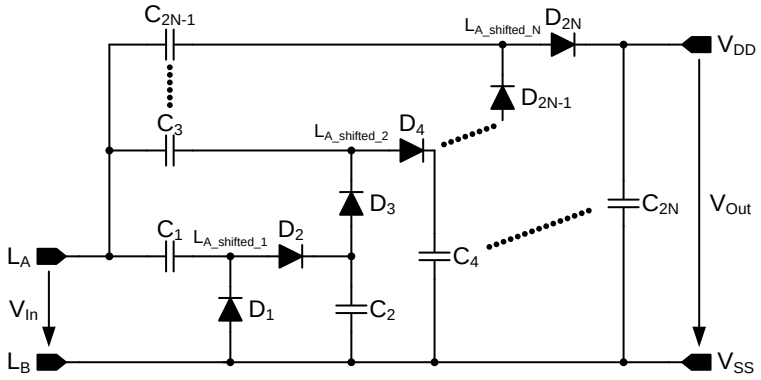
- Available input voltage
- Loaded Q Factor
- Input frequency
- Forward voltage drop
- Desired output voltage
- Output load

Generally, the higher the number of stages, the higher the output voltage. Thus, if a distinct output voltage is desired the input voltage can be reduced by using more stages. As explained in Section 2.4.1 the available input voltage depends on the loaded Q Factor which depends again on the chip impedance.

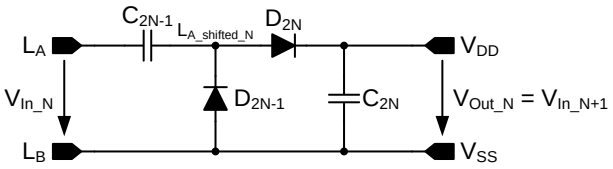
Hence it is important to know how the number of stages influences the chip impedance as well as the PCE. For simplicity the following considerations are based on single-ended half-wave voltage multipliers. Figure 2.19 shows the architecture of a single-ended n-stage voltage multiplier based on the Greinacher principle. Considering that the output voltage of the previous stage is the input voltage of the next stage, Figure 2.19a can be redrawn to Figure 2.19b. Neglecting parasitics the output voltage of the voltage multiplier with n stages can be calculated using:

$$V_{Out} = 2 \cdot n \cdot \widehat{V_{In}} - \sum_{i=1}^{2 \cdot n} V_{D_i} \tag{2.4.14}$$

By analyzing one stage of the voltage multiplier (for simplicity the indices of the first stage are taken) the theory behind (2.4.14) can be explained as follows:
The coupling capacitor C_1 is charged to the input peak voltage during the negative phase of the input signal. This voltage is added to the input voltage and stored in the buffer capacitor



(a) Detailed schematic



(b) Simplified schematic

Figure 2.19: n-stage single-ended voltage multiplier

C_2 during the positive phase of the input signal. Thus, in steady-state the output voltage is theoretically doubled with every voltage multiplier stage. Due to the fact that the diodes D_1 and D_2 have each a forward voltage drop, the voltage level at which C_1 as well as C_2 are charged to is lowered just by these voltage drops V_{D_1} and V_{D_2}, respectively. The horizontal and vertical rectification devices and their controlling are identical only if their voltage drops are also identical.

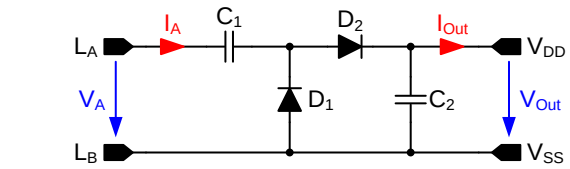
2.4.5.1 One Stage versus Two Stages

Neglecting the parasitics and the forward voltage drop of the diodes, and considering an equal DC output voltage and load for a one-stage and a two-stage voltage multiplier, the input voltage of the one-stage voltage multiplier has to be twice the input voltage of the two-stage voltage multiplier. Thus, the input current of the one-stage voltage multiplier is half of the input current of the two-stage voltage multiplier. In this ideal example the currents of the first and second stage of the two-stage voltage multiplier are also equal. Figure 2.20 shows the two voltage multipliers with depicted voltage and current arrows. The power conditions can be simply described as:

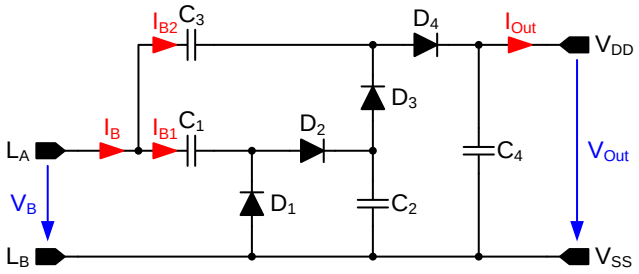
$$V_B = \frac{V_A}{2} \tag{2.4.15a}$$

$$I_B = 2 \cdot I_A \tag{2.4.15b}$$

$$I_{B_1} = I_{B_2} = \frac{I_B}{2} = I_A \tag{2.4.15c}$$



(a) one-stage



(b) two-stage

Figure 2.20: Voltage multipliers with voltage and current arrows

symbol	description
V_A	input voltage of the one-stage voltage multiplier
V_B	input voltage of the two-stage voltage multiplier
I_A	input current of the one-stage voltage multiplier
I_B	input current of the two-stage voltage multiplier
I_{B_1}	input current of the first stage of the two-stage voltage multiplier
I_{B_2}	input current of the second stage of the two-stage voltage multiplier
P_{in}	input power of the voltage multipliers
V_{out}	output voltage of the voltage multipliers
I_{out}	output current of the voltage multipliers
P_{out}	output power of the voltage multipliers

Table 2.2: List of symbols for (2.4.15)

$$P_{in} = V \cdot I = V_A \cdot I_A = 2 \cdot V_B \cdot \frac{I_B}{2} = V_B \cdot I_B \tag{2.4.15d}$$

$$I_{out} = \frac{V_{out}}{R_{load}} \tag{2.4.15e}$$

$$P_{out} = V_{out} \cdot I_{out} \tag{2.4.15f}$$

A description of the symbols in (2.4.15) is given in Table 2.2.

2.4.5.2 Power Dissipation in the Voltage Multiplier

As stated in Section 2.4.2 the power dissipated in the voltage multiplier affects the PCE as shown in (2.4.11). Charging the capacitors plays an important role in the power dissipation of the voltage multiplier.

The charge stored in a capacitor depends on the capacitance and the voltage across the capacitor. This voltage cannot change instantaneously, thus the charge also varies as a function of time. Considering a constant capacitance, the charge of a capacitor is defined as:

$$q(t) = C \cdot v(t) \tag{2.4.16}$$

That means the capacitance is the proportionality factor between charge and voltage. Using infinitesimal time intervals yields:

$$C = \frac{\frac{dq}{dt}}{\frac{dv}{dt}} = \frac{dq}{dv}\bigg|_{q=q(t),v=v(t)} \tag{2.4.17}$$

The variation of the charge with respect to time is the capacitor current. Taking the derivate of (2.4.16) yields the capacitor current, which of course also varies as a function of time:

$$i(t) = \frac{dq(t)}{dt} = C \cdot \frac{dv(t)}{dt} \tag{2.4.18}$$

The voltage across the capacitor can be calculated from (2.4.16) and (2.4.18):

$$v(t) = \frac{1}{C} \cdot q(t) = \frac{1}{C} \cdot \int_{to}^{t} i(\tau)d\tau + v(to) \tag{2.4.19}$$

Work has to be done to move charge in the capacitor. The capacitor is a storage element that stores but does not dissipate energy. The applied energy by means of charge transfer is again available for the load. However, in the charging circuit the same amount of energy is consumed. To calculate the power consumption caused by charging capacitors the energy stored in the capacitor has to be calculated first. The energy relationship of a capacitor can be easily derived by integrating the power equation of the capacitor. Using (2.4.16), (2.4.18), and (2.4.19) yields:

$$p(t) = v(t) \cdot i(t) = \frac{1}{C} \cdot q(t) \cdot \frac{dq(t)}{dt} \tag{2.4.20}$$

From (2.4.16) and (2.4.20) the energy stored in the capacitor as function of time can thus be calculated as:

$$\begin{aligned} w(t) &= \int_{-\infty}^{t} p(\tau)d\tau = \int_{-\infty}^{t} \frac{1}{C} \cdot q \cdot \frac{dq}{dt}d\tau\bigg|_{q=q(t)} \\ &= \int_{q(-\infty)}^{q(t)} \frac{1}{C} \cdot qdq\bigg|_{q=q(t)} = \int_{v(-\infty)}^{v(t)} C \cdot vdv\bigg|_{v=v(t)} \\ &= \frac{1}{C} \cdot q^2\Big|_{q(-\infty)}^{q(t)} = C \cdot v^2\Big|_{v(-\infty)}^{v(t)} \end{aligned} \tag{2.4.21}$$

Considering that the capacitor is uncharged at $t = -\infty$ ($q(-\infty) = v(-\infty) = 0$) and has a charge of Q and a voltage of V at the time t the energy stored in the capacitor is:

$$W = \frac{1}{C} \cdot q^2 \Big|_0^Q = C \cdot v^2 \Big|_0^V = \frac{1}{2} \cdot \frac{1}{C} \cdot Q^2 = \frac{1}{2} \cdot C \cdot V^2 \tag{2.4.22}$$

If the capacitor is precharged with V_1 at t_1 and has a voltage V_2 at t_2 the energy stored in the capacitor can be calculated as:

$$\begin{aligned} W &= \int_{v(t_1)}^{v(t_2)} C \cdot v dv \Big|_{v=v(t)} = \frac{1}{2} \cdot C \cdot v^2 \Big|_{v(t_1)}^{v(t_2)} \\ &= \frac{1}{2} \cdot C \cdot v^2 \Big|_{V_1}^{V_2} = \frac{1}{2} \cdot C \cdot \left({V_2}^2 - {V_1}^2 \right) \end{aligned} \tag{2.4.23}$$

2.4.5.3 Power Consumption of Capacitor Charging

Now the power consumption caused by charging the capacitors can be determined. For simplicity the following explanations are based on a one-stage voltage multiplier with ideal diodes (no forward voltage drop) as shown in Figure 2.20a.
At startup the coupling capacitor is charged to $-\widehat{V_{in}}$ during the negative phase because the node $L_{A\_shifted}$ is connected to V_{SS}. During each positive phase, charge stored in the coupling capacitor is transferred to the buffer capacitor, which implies that the coupling capacitor is discharged. As shown in (2.4.17) the voltage across the buffer capacitor depends on its capacitance and the transferred charge. Nevertheless the maximum voltage across the buffer capacitor can be $2 \cdot \widehat{V_{in}}$. Typically the capacitance of the buffer capacitor is a multiple of the capacitance of the coupling capacitor. So it takes a couple of periods till the buffer capacitor is charged to $2 \cdot \widehat{V_{in}}$. During this time the whole charge of the coupling capacitor is transferred to the buffer capacitor every period, which means that the voltage across the coupling capacitor is charged to $2 \cdot \widehat{V_{in}}$ each period. As stated above, charging a capacitor consumes power. Accordingly the coupling capacitor causes power consumption during the negative and the buffer capacitor causes power consumption during the positive phase of the input signal.

ΔV is the voltage a capacitor has to be charged to every period. At startup $\Delta V = 2 \cdot \widehat{V_{in}}$ in the worst case. The voltage across the capacitors is lowered with every period till it depends only on the output load in steady-state. In steady-state ΔV is defined by the DC output current and capacitance of the capacitor and the duration of discharge as the following equation shows:

$$\Delta V = V_2 - V_1 = \frac{I_{out} \cdot t}{C} = \frac{I_{out}}{f_{in} \cdot C} = \frac{V_{out}}{f_{in} \cdot C \cdot R_{load}} \tag{2.4.24}$$

As stated above, the same amount of energy that is stored in the capacitor is consumed by the charging circuit. Due to the fact that the charging process is repeated every period the power consumed by the charging circuit can be calculated using:

$$P_{C_i} = W \cdot f_{in} = \frac{1}{2} \cdot f_{in} \cdot C_i \cdot \left(V_{2_i}^2 - V_{1_i}^2 \right), \tag{2.4.25}$$

symbol	description
$P_{C_{Couple}}, P_{C_{(2N-1)}}$	power consumption caused by charging one couple capacitor
$P_{C_{Buffer}}, P_{C_{(2N)}}$	power consumption caused by charging one buffer capacitor
$P_{C_{Couple\_total}}$, $P_{C_{Couple\_total\_n\ stage}}$	power consumption caused by charging all couple capacitors of an n-stage voltage multiplier
$P_{C_{Buffer\_total}}$, $P_{C_{Buffer\_total\_n\ stage}}$	power consumption caused by charging all buffer capacitors of an n-stage voltage multiplier
n	number of stages
N	number of the current stage
P_{in}	RF input power of the voltage multiplier
P_{out}	DC output power of the voltage multiplier

Table 2.3: List of symbols for (2.4.26), (2.4.27), and (2.4.28)

where the index i is the number, V_{2_i} the maximum voltage, and V_{1_i} the minimum voltage of the respective capacitor (see Figure 2.19b).
It is obvious that the energy stored in the coupling capacitor is used to charge the buffer capacitor, and again the energy stored in the buffer capacitor is then used to power the load. Consequently, during the positive phase the buffer capacitor is reloaded and the output load is powered. The energy for that comes from both, the coupling capacitor and the source.

The higher the number of stages the lower the necessary input voltage. (2.4.15) shows that the input voltage of a two-stage voltage multiplier needs to be only half that of a one-stage voltage multiplier. However, the power needed to charge the coupling and buffer capacitors increases with the number of stages because the lower the input amplitude the higher the potential the charge has to be transferred to. Nevertheless, the amount of charge that is transferred is still equal. Simulation and numerical analysis based on the previous considerations lead to (2.4.26) and (2.4.27). A description of the symbols is given in Table 2.3.

$$P_{C_{Couple}} = P_{C_{(2N-1)}} = \frac{P_{out}}{2 \cdot n} \cdot (2 \cdot N - 1) \tag{2.4.26a}$$

$$P_{C_{Buffer}} = P_{C_{(2N)}} = \frac{P_{out}}{n} \cdot N \tag{2.4.26b}$$

$$P_{C_{Couple\_total}} = \sum_{N=1}^{n} P_{C_{(2N-1)}} = \sum_{N=1}^{n} \frac{P_{out}}{2 \cdot n} \cdot (2 \cdot N - 1) = \frac{n}{2} \cdot P_{out} \tag{2.4.26c}$$

$$P_{C_{Buffer\_total}} = \sum_{N=0}^{n-1} P_{C_{(2N)}} = \sum_{N=0}^{n-1} \frac{P_{out}}{n} \cdot N = \frac{n-1}{2} \cdot P_{out} \tag{2.4.26d}$$

Looking at (2.4.26c) it can be seen that the power consumption caused by charging the coupling

capacitors increases with the number of stages. By calculating the total power consumption caused by charging the coupling capacitors for a different amount of stages using (2.4.26c), it becomes apparent that this power consumption increases proportional to the number of stages:

$$P_{C_{Couple\_total\_1stage}} = \frac{1}{2} \cdot P_{out} \tag{2.4.27a}$$

$$P_{C_{Couple\_total\_2stage}} = 2 \cdot P_{C_{Couple\_total\_1stage}} = P_{out} \tag{2.4.27b}$$

$$P_{C_{Couple\_total\_3stage}} = 3 \cdot P_{C_{Couple\_total\_1stage}} = \frac{3}{2} \cdot P_{out} \tag{2.4.27c}$$

The same can be done using (2.4.26d). The energy stored in the buffer capacitor which is placed at the DC output of the voltage multiplier is used to power the DC load. Therefore the power consumption caused by charging this capacitor is not included in $P_{C_{Buffer\_total}}$. This is also the reason why the upper bound of summation in (2.4.26d) is the number of stages (here also number of buffer capacitors) lowered by one.

$$P_{C_{Buffer\_total\_2stage}} = \frac{1}{2} \cdot P_{out} \tag{2.4.28a}$$

$$P_{C_{Buffer\_total\_3stage}} = 2 \cdot P_{C_{Buffer\_total\_2stage}} = P_{out} \tag{2.4.28b}$$

$$P_{C_{Buffer\_total\_4stage}} = 3 \cdot P_{C_{Buffer\_total\_2stage}} = \frac{3}{2} \cdot P_{out} \tag{2.4.28c}$$

From (2.4.26), (2.4.27), and (2.4.28) it becomes apparent that for a number of stages greater than one the total power consumed by charging the capacitors is a multiple of the DC output power. However it has to be considered that the energy stored in $C_{2N\text{-}1}$ is used to charge C_{2N}. Only the additional power that is needed to transfer the charge to a higher potential is provided by the source. Nevertheless, as stated above, charging capacitors causes power consumption. Even if this power is also provided by the previous capacitor(s), the higher the total consumed power caused by charging capacitors the higher the power dissipated in the voltage multiplier. Therefore the highest PCE can be achieved with a one-stage voltage multiplier.

That part of the incoming power which is not transferred to the output is dissipated in the charging circuitry. In the voltage multiplier circuit shown in Figure 2.19 the diodes dissipate exactly that amount of the incoming power. Thus, for equal diodes the dissipated power can be calculated using:

$$P_{D_{total}} = P_{in} - P_{out} = 2 \cdot n \cdot P_D \tag{2.4.29a}$$

$$P_D = P_{D_{(2N\text{-}1)}} = P_{D_{(2N)}} = \frac{P_{in} - P_{out}}{2 \cdot n}, \tag{2.4.29b}$$

where P_D is the dissipated power of each diode. Thus, (2.4.11) can be rewritten as:

$$PCE = \frac{P_{out}}{P_{out} + 2 \cdot n \cdot P_D} = \frac{P_{in} - 2 \cdot n \cdot P_D}{P_{in}} = 1 - \frac{2 \cdot n \cdot P_D}{P_{in}} \tag{2.4.30}$$

A description of the symbols in (2.4.29) and (2.4.30) is given in Table 2.4.

symbol	description
PCE	power conversion efficiency
$P_{D_{total}}$	total dissipated power of the voltage multiplier
P_D	dissipated power of one diode
$P_{D_{(2N-1)}}$	dissipated power of a horizontal diode
$P_{D_{(2N)}}$	dissipated power of a vertical diode
n	number of stages
N	number of the current stage
P_{in}	RF input power of the voltage multiplier
P_{out}	DC output power of the voltage multiplier

Table 2.4: List of symbols for (2.4.29) and (2.4.30)

2.4.5.4 Conclusion

Section 2.4.5 discussed the effects of the number of stages of voltage multipliers. Important for the PCE is the power consumption caused by charging the capacitors in an n-stage voltage multiplier. From (2.4.30) it becomes apparent that the PCE is lowered with every additional stage and that the highest PCE can be achieved with only one stage. Nevertheless the choice of the number of stages has to be made taking the values of the loaded Q Factor into account. Furthermore, there exists a tradeoff between the physically achievable loaded Q Factor and manufacturing costs.

2.5 Analysis of the CMOS Transistor-Based Voltage Multiplier

The symbols used in this section are defined in Table 2.5.

Some publications deal with modeling and/or analysis of voltage multipliers for the use in RFID transponders. An RF to DC conversion model to calculate the DC output voltage as a factor of the RF power available from the antenna is given in [6]. Some power analyses are done in [17], [53], and [117]. In [71] separate DC and AC analysis are performed to gain equations for power analysis. Unfortunately, in this publication are several inconsistencies and some losses are neglected. Therefore, based on the analysis in Section 2.4.5 and inspired by the publications stated above, a CMOS transistor-based voltage multiplier is analyzed in detail by using the following approach:

The analysis of the n-stage voltage multiplier is split into an AC and a DC analysis. It is assumed that a sinusoidal voltage V_{in} is applied at the input, which is defined by (2.5.1).

$$V_{in} = V_0 \cdot \cos(2\pi \cdot f \cdot t) = V_0 \cdot \cos(\omega \cdot t) \tag{2.5.1}$$

To ensure a small ripple of the DC output voltage and to be able to transfer a reasonable amount of charge to the output buffer capacitor, the capacitors have to be dimensioned to

symbol	description
V_{in}	input voltage of the voltage multiplier
V_{out}	output voltage of the voltage multiplier
I_{out}	output current of the voltage multiplier
V_0	amplitude of the input voltage of the voltage multiplier
f	operating frequency of the voltage multiplier
V_D	drain source voltage of the MOS transistor
$V_{D_{AC}}$	AC drain source voltage of the MOS transistor
$V_{D_{DC}}$	DC drain source voltage of the MOS transistor
V_T	threshold voltage of the MOS transistor
P_{in}	RF input power of the voltage multiplier
P_{out}	DC output power of the voltage multiplier
P_D	dissipated power of one MOS transistor
n	number of stages
N	number of the current stage

Table 2.5: List of symbols used in Section 2.5

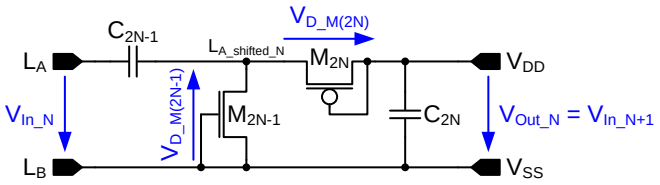


Figure 2.21: n-stage single-ended voltage multiplier with MOSFETs

achieve a time constant which is much larger than the period of the input signal. The time constant τ of a capacitor is defined as:

$$\tau = R \cdot C = \frac{1}{2\pi \cdot f_c} \tag{2.5.2}$$

For the analyzed voltage multiplier $R = \Delta V_{out}/\Delta I_{out}$, so:

$$C >> \frac{\Delta I_{out}}{2\pi \cdot f \cdot \Delta V_{out}} \tag{2.5.3}$$

In this case the voltage across all capacitors can be considered to be a DC voltage.

2.5.1 DC and AC Analysis

These analyses are based on an n-stage voltage multiplier built with MOSFET transistors operating as diodes as shown in Figure 2.21. In this example NMOS transistors operating as vertical diodes and PMOS transistors as horizontal diodes, respectively. Nevertheless, different configurations of transistors have no effect on the following analysis.

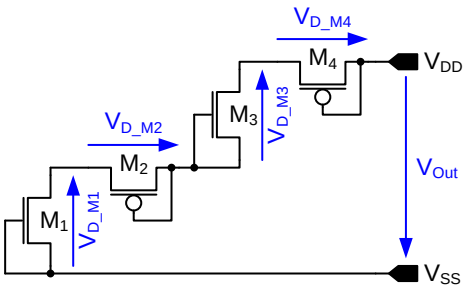


Figure 2.22: DC equivalent circuit of a two-stage voltage multiplier

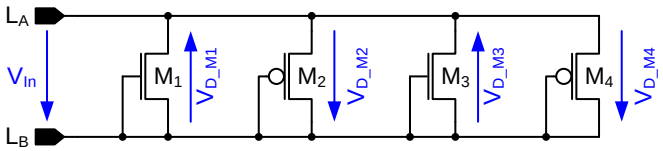


Figure 2.23: AC equivalent circuit of a two-stage voltage multiplier

In the DC analysis capacitors can be considered as open circuits, therefore all transistors are connected in series as shown in Figure 2.22. For simplicity a two-stage version of Figure 2.21 is taken for these considerations. As a consequence, the DC voltage across a diode can be calculated to be:

$$V_{D_{DC}} = -\frac{V_{out}}{2 \cdot n} \tag{2.5.4}$$

In the AC analysis capacitors can be considered as short circuits as shown in Figure 2.23, therefore the vertical and horizontal transistors are antiparallel and parallel to the input, respectively. (2.5.5) describes this correlation.

$$V_{D_{AC}} = \mp V_{in} \tag{2.5.5a}$$

$$V_{D_{AC\_vertical}} = V_{D_{AC\_M(2N-1)}} = -V_{in} \tag{2.5.5b}$$

$$V_{D_{AC\_horizontal}} = V_{D_{AC\_M(2N)}} = V_{in} \tag{2.5.5c}$$

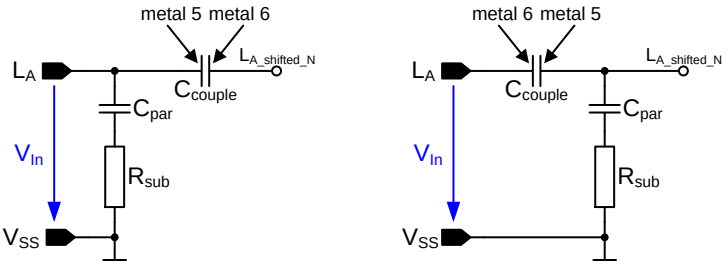
Using the superposition principle the voltage drop across a transistor can be calculated to be:

$$V_D = V_{D_{AC}} + V_{D_{DC}} = \mp V_{in} - \frac{V_{out}}{2 \cdot n} = \mp V_0 \cdot \cos(\omega \cdot t) - \frac{V_{out}}{2 \cdot n} \tag{2.5.6a}$$

$$V_{D_{vertical}} = V_{D_{M(2N-1)}} = -V_0 \cdot \cos(\omega \cdot t) - \frac{V_{out}}{2 \cdot n} \tag{2.5.6b}$$

$$V_{D_{horizontal}} = V_{D_{M(2N)}} = V_0 \cdot \cos(\omega \cdot t) - \frac{V_{out}}{2 \cdot n} \tag{2.5.6c}$$

The voltage across the horizontal transistors (M_{2N}) has the same direction as the input as well as the output voltage. Therefore the output voltage of an n-stage voltage multiplier can be



(a) metal 5 connected to the input

(b) metal 6 connected to the input

Figure 2.24: Parasitic capacitance of the coupling capacitor

calculated using (2.5.6c) to be:

$$V_{out} = 2 \cdot n \cdot (V_{in} - V_{D_{horizontal}}) = 2 \cdot n \cdot \left(V_0 \cdot \cos(\omega \cdot t) - V_{D_{M(2N)}}\right) \tag{2.5.7}$$

In this case the parasitic effects are neglected.

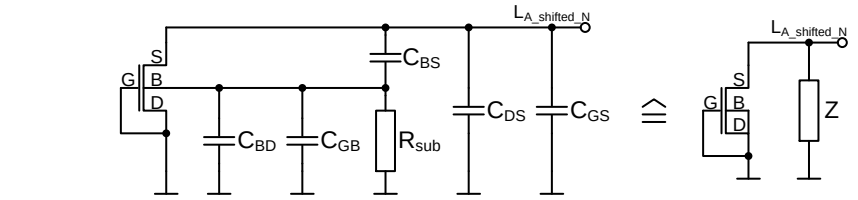
2.5.1.1 Parasitic Effects

Now the major parasitic effects are taken into account. Every capacitor has parasitic capacitors connected between the terminals and chip substrate. In this work the coupling capacitors are designed as metal-metal capacitors between the 5^{th} and 6^{th} (last) metal layer. That terminal of the coupling capacitor which has the higher parasitic capacitance to substrate (lower metal plane) is connected to the input. The metal 1 plane is implemented as V_{SS} plane to achieve a parasitic capacitor with a high Q Factor. Thus, parasitic capacitors with low losses (R_{sub} <<) are in parallel with the source as depicted in Figure 2.24a.

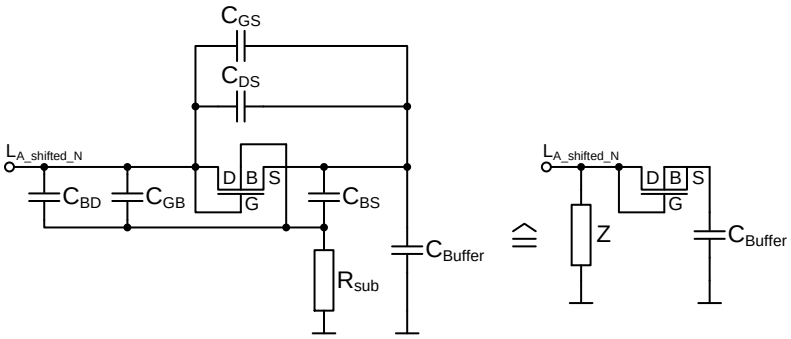
If the terminals of the coupling capacitors are interchanged an unwanted voltage divider as depicted in Figure 2.24b lowers the voltage at the nodes $L_{A\_shifted_N}$ (see Figure 2.21). The buffer capacitors are implemented in the lower metal plane to also use the parasitic capacitance as buffer. Of course it is also advantageous to have high Q Factors here.

Dependent on the type and placement of the MOSFETs in the circuitry the parasitics vary. Typically voltage multipliers are built only with NMOS transistors or with NMOS and PMOS transistors operating as vertical and horizontal diodes, respectively. Figure 2.25 shows the parasitics of these four configurations.

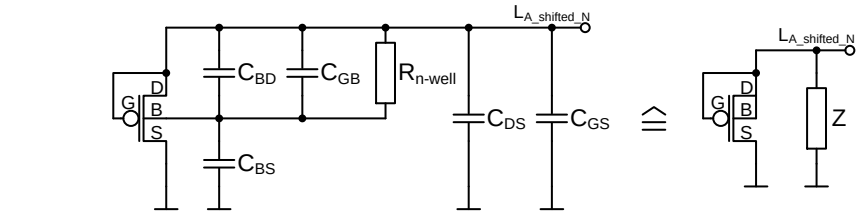
The parasitics cause losses as well as a voltage division at the nodes $L_{A\_shifted_N}$ (see Figure 2.21). Looking at Figure 2.21 and Figure 2.25 it becomes obvious that the higher the parasitic capacitances the lower the voltage at the nodes $L_{A\_shifted_N}$. Assuming that the buffer capacitors are much larger than the parasitics the voltage drop across this capacitors can be considered as a DC voltage. Thus, the buffer capacitors can be considered as short circuits. The respective equivalent impedance Z in Figure 2.25 can be calculated using (2.5.8).



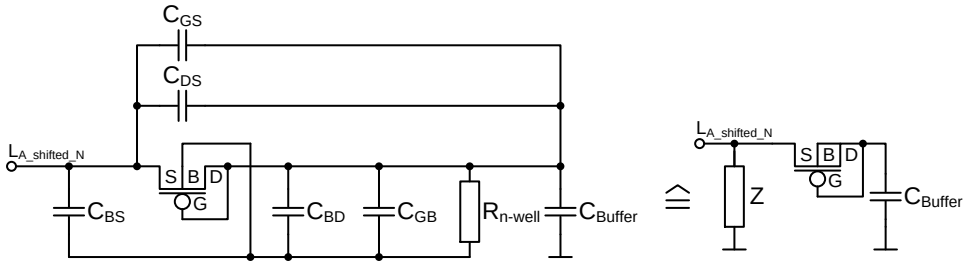
(a) NMOS vertical



(b) NMOS horizontal



(c) PMOS vertical



(d) PMOS horizontal

Figure 2.25: Parasitic capacitances of the diode-connected transistors

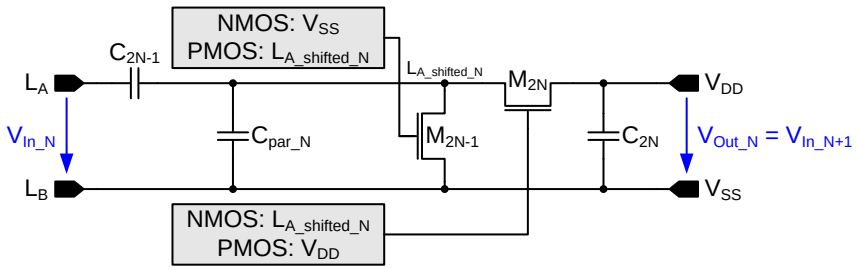


Figure 2.26: n-stage single-ended voltage multiplier with MOSFETs and main parasitic capacitance C_{par_N}

$$Z = \frac{1}{\jmath\omega C_{GS}} \Big\| \frac{1}{\jmath\omega C_{DS}} \Big\| \left[\frac{1}{\jmath\omega C_{BS}} + \left(\frac{1}{\jmath\omega C_{BD}} \Big\| \frac{1}{\jmath\omega C_{GB}} \Big\| R_{sub} \right) \right] \quad \text{Figure 2.25a} \quad (2.5.8a)$$

$$Z = \frac{1}{\jmath\omega C_{GS}} \Big\| \frac{1}{\jmath\omega C_{DS}} \Big\| \left[\left(\frac{1}{\jmath\omega C_{BD}} + \frac{1}{\jmath\omega C_{GB}} \right) + \left(\frac{1}{\jmath\omega C_{BS}} \Big\| R_{sub} \right) \right] \quad \text{Figure 2.25b} \quad (2.5.8b)$$

$$Z = \frac{1}{\jmath\omega C_{GS}} \Big\| \frac{1}{\jmath\omega C_{DS}} \Big\| \left[\frac{1}{\jmath\omega C_{BS}} + \left(\frac{1}{\jmath\omega C_{BD}} \Big\| \frac{1}{\jmath\omega C_{GB}} \Big\| R_{n\text{-}well} \right) \right] \quad \text{Figure 2.25c} \quad (2.5.8c)$$

$$Z = \frac{1}{\jmath\omega C_{GS}} \Big\| \frac{1}{\jmath\omega C_{DS}} \Big\| \left[\frac{1}{\jmath\omega C_{BS}} + \left(\frac{1}{\jmath\omega C_{BD}} \Big\| \frac{1}{\jmath\omega C_{GB}} \Big\| R_{n\text{-}well} \right) \right] \quad \text{Figure 2.25d} \quad (2.5.8d)$$

The influences of the substrate and the n-well resistance on the capacitive voltage divider are marginal. Thus, they can be neglected for this consideration. So the equivalent impedance Z has only capacitive components, and therefore an equivalent parasitic capacitor C_{par} connected to one terminal of the coupling capacitor can be calculated as shown in (2.5.9).

$$\jmath\omega C_{par_{(2N\text{-}1)}} = \frac{1}{Z|_{R_{sub}=0}} = \jmath\omega \cdot (C_{GS} + C_{DS} + C_{BS}) \quad \text{NMOS vertical} \quad (2.5.9a)$$

$$\jmath\omega C_{par_{(2N)}} = \frac{1}{Z|_{R_{sub}=0}} = \jmath\omega \cdot (C_{GS} + C_{DS} + C_{BD} + C_{GB}) \quad \text{NMOS horizontal} \quad (2.5.9b)$$

$$\jmath\omega C_{par_{(2N\text{-}1)}} = \frac{1}{Z|_{R_{n\text{-}well}=0}} = \jmath\omega \cdot (C_{GS} + C_{DS} + C_{BS}) \quad \text{PMOS vertical} \quad (2.5.9c)$$

$$\jmath\omega C_{par_{(2N)}} = \frac{1}{Z|_{R_{n\text{-}well}=0}} = \jmath\omega \cdot (C_{GS} + C_{DS} + C_{BS}) \quad \text{PMOS horizontal} \quad (2.5.9d)$$

The voltage at the nodes $L_{A\_shifted_N}$ can be calculated to be:

$$V_N = V_{in} \cdot \frac{Z_N}{Z_N + \frac{1}{\jmath\omega C_{(2N\text{-}1)}}}, \quad (2.5.10)$$

where Z_N is the equivalent impedance connected between the node $L_{A\_shifted_N}$ and V_{SS} and

$C_{(2N\text{-}1)}$ is the respective coupling capacitor. Using (2.5.9) yields to:

$$V_N = V_{in} \cdot \frac{\frac{1}{\jmath\omega C_{par_N}}}{\frac{1}{\jmath\omega C_{par_N}} + \frac{1}{\jmath\omega C_{(2N\text{-}1)}}} = V_{in} \cdot \frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}} \tag{2.5.11}$$

C_{par_N} is the parallel circuit of the parasitic capacitances of the vertical and horizontal diode-connected transistors and can be calculated using (2.5.12).

$$C_{par_N} = C_{par_{(2N\text{-}1)}} \| C_{par_{(2N)}} = C_{par_{(2N\text{-}1)}} + C_{par_{(2N)}} \tag{2.5.12}$$

Knowing C_{par_N}, the equivalent circuit of the n-stage voltage multiplier can be redrawn as in Figure 2.26. Now the voltages across the diode-connected transistors can be calculated. As stated above in the high frequency analysis all the diode-connected transistors are in parallel or antiparallel. Thus, the voltage at the node V_N is in antiparallel with the vertical and in parallel with the horizontal diode-connected transistors. Therefore, the AC voltage across one transistor is:

$$V_{D_{AC}} = \mp V_N = \mp V_{in} \cdot \frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}} \tag{2.5.13a}$$

$$V_{D_{AC\_vertical}} = V_{D_{AC\_M(2N\text{-}1)}} = -V_N = -V_{in} \cdot \frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}} \tag{2.5.13b}$$

$$V_{D_{AC\_horizontal}} = V_{D_{AC\_M(2N)}} = V_N = V_{in} \cdot \frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}} \tag{2.5.13c}$$

The DC voltage remains the same and so the voltage across one transistor can be calculated using (2.5.4) and (2.5.13) while the ohmic losses are neglected.

$$V_D = V_{D_{AC}} + V_{D_{DC}} = \mp V_{in} \cdot \frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}} - \frac{V_{out}}{2 \cdot n} \tag{2.5.14a}$$

$$= \mp V_0 \cdot \frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}} \cdot \cos(\omega \cdot t) - \frac{V_{out}}{2 \cdot n} \tag{2.5.14b}$$

$$V_{D_{vertical}} = V_{D_{M(2N\text{-}1)}} = -V_0 \cdot \frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}} \cdot \cos(\omega \cdot t) - \frac{V_{out}}{2 \cdot n} \tag{2.5.14c}$$

$$V_{D_{horizontal}} = V_{D_{M(2N)}} = V_0 \cdot \frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}} \cdot \cos(\omega \cdot t) - \frac{V_{out}}{2 \cdot n} \tag{2.5.14d}$$

The higher the parasitic capacitances the lower the voltage across one transistor and thus the lower the output voltage as obvious from (2.5.15):

$$\begin{aligned} V_{out} &= 2 \cdot n \cdot \left(V_{in} \cdot \frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}} - V_{D_{horizontal}} \right) \\ &= 2 \cdot n \cdot \left(V_0 \cdot \frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}} \cdot \cos(\omega \cdot t) - V_{D_{M(2N)}} \right) \end{aligned} \tag{2.5.15}$$

Furthermore the output voltage is lowered by the sum of the voltages that drop across each transistor. In (2.5.15) the voltage drop of each transistor and the sizes of the coupling and parasitic capacitances are assumed to be identical to make the equation more readable. To get the output voltage of a voltage multiplier the voltage drops of the transistors have to be determined.

Transistor Current and Forward Voltage Drop

A diode-connected transistor operates in saturation and $V_{DS} = V_{GS}$. Therefore, the equation for the drain current from the Shichman–Hodges model [105] which is given in (2.5.16) can be used to calculate the drain-source voltage V_{DS} which is equal to the voltage drop V_D of the diode-connected transistor.

$$\begin{aligned} I_D &= K \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \\ &= \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \,, \end{aligned} \tag{2.5.16}$$

where the channel-length modulation parameter λ is inversely proportional to channel length L.

If the bulk and the source of a transistor are not connected, the body effect has to be taken into account. The threshold voltage increases if the source and drain junctions remain reversed biased. Depending on the position of the transistor in the voltage multiplier the body effect varies. If PMOS transistors are utilized in the CMOS process used, the source and bulk can but need not be shorted.
The bulk of an NMOS transistor is substrate. Therefore the source and bulk of an NMOS transistor only have the same potential if it is utilized as the vertical diode in the first stage. If the body effect takes effect V_T can be calculated using (2.5.17).

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|} \right) \tag{2.5.17a}$$

$$V_{T0} = V_{FB} + |2\Phi_F| + \frac{\sqrt{2 \cdot q \cdot \epsilon_{si} \cdot N_{sub} \cdot |2\Phi_F|}}{C_{ox}} \tag{2.5.17b}$$

where V_{T0} is the threshold voltage if $V_{SB} = 0$ and the body effect coefficient is expressed as:

$$\gamma = \frac{\sqrt{2 \cdot q \cdot \epsilon_{si} \cdot N_{sub}}}{C_{ox}} \tag{2.5.18}$$

Having a look at (2.5.17a) it is apparent that the higher the V_{SB} the higher the threshold voltage of the respective transistor. So, if NMOS transistors are used for a high number of stages the voltage drop across each transistor increases with the number of stages, and therefore the performance decreases.

A description of the symbols in (2.5.16), (2.5.17), and (2.5.18) is given in Table 2.6.

Neglecting the channel-length modulation for simplicity, (2.5.16) can be rewritten as:

$$V_D = V_{DS} = V_{GS} = \sqrt{2 \cdot I_D \cdot \frac{1}{\mu \cdot C_{ox}} \cdot \frac{L}{W}} + V_T \tag{2.5.19}$$

symbol	description
I_D	drain current
K	transconductance parameter
W	effective channel width
L	effective channel length
V_{DS}	drain source voltage
V_{GS}	gate source voltage
V_{SB}	source bulk voltage
V_T	threshold voltage
V_{T0}	threshold voltage at $V_{SB} = 0$
γ	body effect coefficient
$\lvert 2\Phi_F \rvert$	surface potential
q	electron charge
ϵ_{si}	dielectric constant of silicon
N_{sub}	doping concentration of substrate
C_{ox}	capacitance per unit area of gate oxide

Table 2.6: List of symbols for (2.5.16), (2.5.17), and (2.5.18)

From (2.5.17) it can be assumed in a first order approximation that V_T is a technology parameter. Thus, for a constant I_D the voltage across the diode-connected transistor (V_D from (2.5.19)) can be lowered by increasing the channel length and decreasing the channel width. However to drive a certain I_D a sufficient aspect ratio ($\frac{W}{L}$) is needed. Thus, V_D decreases with higher channel width and length but the parasitic capacitances increase. The higher the parasitic capacitances the lower the voltage at the node $L_{A\_shifted_N}$. The parasitic capacitances considered show the following behavior:

$$\begin{aligned} C_{BD} &\propto W \\ C_{BS} &\propto W \\ C_{DS} &\propto \frac{W}{L} \\ C_{GB} &\propto L \\ C_{GD} &\propto W \\ C_{GS} &\propto W \cdot L \end{aligned} \tag{2.5.20}$$

Therefore, as stated in Section 2.4.3, there exists a tradeoff between transistor size and parasitic capacitance. The dimensioning of the voltage divider has to be done with respect to the PCE and output voltage of the voltage multiplier.

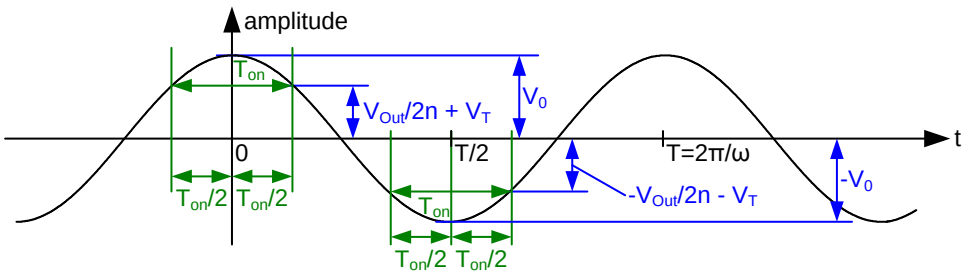


Figure 2.27: Switching behavior of the voltage multiplier

2.5.2 Power Analysis

In the following analysis it is assumed that the drain source voltage, the drain current and threshold voltage of every transistor are equal. Therefore, the conduction angle is equal for all transistors and so all transistors are conductive for T_{on}.
The horizontal transistors $M_{(2N)}$ are conductive in the positive phase of the input signal from $-\frac{T_{on}}{2}$ to $\frac{T_{on}}{2}$ where the vertical transistors $M_{(2N\text{-}1)}$ are conductive in the negative phase of the input signal from $\frac{T}{2} - \frac{T_{on}}{2}$ to $\frac{T}{2} + \frac{T_{on}}{2}$ as shown in Figure 2.27.

$$T_{on_{horizontal}} = \frac{T_{on}}{2} - \left(-\frac{T_{on}}{2}\right) = T_{on} \tag{2.5.21a}$$

$$T_{on_{vertical}} = \frac{T}{2} + \frac{T_{on}}{2} - \left(\frac{T}{2} - \frac{T_{on}}{2}\right) = T_{on} \tag{2.5.21b}$$

T is the period of the input signal:

$$T = \frac{1}{f} = \frac{2 \cdot \pi}{\omega} \tag{2.5.22}$$

2.5.2.1 Transistor Current

The drain current through every transistor can be calculated using (2.5.16) and the assumptions made above:

$$\begin{aligned} I_D &= \frac{1}{2} \cdot \beta \cdot (V_D - V_T)^2 \\ \beta &= \mu \cdot C_{ox} \cdot \frac{W}{L} \end{aligned} \tag{2.5.23}$$

where (2.5.6) or (2.5.14) is used for V_D if parasitic capacitances are neglected or taken into account, respectively.
To simplify this analysis the parasitic capacitances are neglected, but if they are taken into account, the amplitude of the input voltage (V_0) has only to be multiplied by the capacitive voltage divider caused by $C_{(2N\text{-}1)}/(C_{(2N\text{-}1)} + C_{par_{(2N\text{-}1)}} + C_{par_{(2N)}})$ in every following equation of this power dissipation analysis. That means the input voltage has to be increased by the factor $(C_{(2N\text{-}1)} + C_{par_{(2N\text{-}1)}} + C_{par_{(2N)}})/C_{(2N\text{-}1)}$ to gain the same output voltage and thus the same

output power as would be achieved if there were no parasitics. Of course the dissipated power increases and thus the PCE decreases.

Inserting (2.5.6a) in (2.5.23) yields to:

$$I_D = \frac{\beta}{2} \cdot \left(\mp V_0 \cdot \cos(\omega \cdot t) - \frac{V_{out}}{2 \cdot n} - V_T \right)^2 \tag{2.5.24}$$

From the trigonometric equations shown in (2.5.25) (2.5.26) can be expressed.

$$\begin{aligned} \cos(x+y) &= \cos(x) \cdot \cos(y) - \sin(x) \cdot \sin(y) \\ \sin(x)^2 + \cos(x)^2 &= 1 \end{aligned} \tag{2.5.25}$$

$$\cos^2(x) = \frac{1}{2} + \frac{1}{2} \cdot \cos(2 \cdot x) \tag{2.5.26}$$

Thus (2.5.24) can be rewritten as:

$$\begin{aligned} I_D &= \frac{\beta}{2} \cdot \left[V_0^2 \cdot \cos^2(\omega \cdot t) \pm 2 \cdot V_0 \cdot \cos(\omega \cdot t) \cdot \frac{V_{out}}{2 \cdot n} \right. \\ &\qquad \left. \pm 2 \cdot V_0 \cdot \cos(\omega \cdot t) \cdot V_T + \left(\frac{V_{out}}{2 \cdot n} \right)^2 + 2 \cdot \frac{V_{out}}{2 \cdot n} \cdot V_T + V_T^2 \right] \\ &= \frac{\beta}{2} \cdot \left[\frac{V_0^2}{2} + \left(\frac{V_{out}}{2 \cdot n} + V_T \right)^2 \right. \\ &\qquad \left. + \frac{V_0^2}{2} \cdot \cos(2 \cdot \omega \cdot t) \pm 2 \cdot V_0 \cdot \left(\frac{V_{out}}{2 \cdot n} - V_T \right) \cdot \cos(\omega \cdot t) \right] \end{aligned} \tag{2.5.27}$$

2.5.2.2 DC Output Current

From (2.5.27) the AC and DC components are clearly evident where the DC component is equal to the load current I_{out} as shown in (2.5.28).

$$I_{out} = \frac{\beta}{2} \cdot \left[\frac{V_0^2}{2} + \left(\frac{V_{out}}{2 \cdot n} + V_T \right)^2 \right] \tag{2.5.28}$$

2.5.2.3 DC Output Power

Knowing the load current, the power consumed by the load can be easily calculated using (2.5.29).

$$P_{out} = V_{out} \cdot I_{out} = \frac{\beta}{2} \cdot V_{out} \cdot \left[\frac{V_0^2}{2} + \left(\frac{V_{out}}{2 \cdot n} + V_T \right)^2 \right] \tag{2.5.29}$$

2.5.3 Power Dissipation Analysis

Next the power dissipated by the diode-connected transistors should be determined. Therefore, the average power dissipated by every transistor during one period has to be summed up.

$$\begin{aligned} P_{D_{total}} &= n \cdot \frac{1}{T} \cdot \int_{-\frac{T_{on}}{2}}^{T-\frac{T_{on}}{2}} V_D(t) \cdot I_D(t) dt \\ &= n \cdot \frac{1}{T} \cdot \int_{-\frac{T_{on}}{2}}^{\frac{T_{on}}{2}} V_D(t) \cdot I_D(t) dt + n \cdot \frac{1}{T} \cdot \int_{\frac{T}{2}-\frac{T_{on}}{2}}^{\frac{T}{2}+\frac{T_{on}}{2}} V_D(t) \cdot I_D(t) dt \\ &= n \cdot P_{D_{horizontal}} + n \cdot P_{D_{vertical}} \end{aligned} \tag{2.5.30}$$

As stated at the beginning of Section 2.5.2 the transistors are assumed to have equal conditions. Thus, the total dissipated power is:

$$\begin{aligned} P_{D_{total}} &= 2 \cdot n \cdot P_D = 2 \cdot n \cdot P_{D_{horizontal}} = 2 \cdot n \cdot P_{D_{vertical}} \\ &= 2 \cdot n \cdot \frac{1}{T} \cdot \int_{-\frac{T_{on}}{2}}^{\frac{T_{on}}{2}} V_D(t) \cdot I_D(t) dt = 2 \cdot n \cdot \frac{1}{T} \cdot \int_{\frac{T}{2}-\frac{T_{on}}{2}}^{\frac{T}{2}+\frac{T_{on}}{2}} V_D(t) \cdot I_D(t) dt, \end{aligned} \tag{2.5.31}$$

where P_D is the dissipated power of every transistor:

$$P_D = \frac{1}{T} \cdot \int_{-\frac{T_{on}}{2}}^{\frac{T_{on}}{2}} V_D(t) \cdot I_D(t) dt = \frac{1}{T} \cdot \int_{\frac{T}{2}-\frac{T_{on}}{2}}^{\frac{T}{2}+\frac{T_{on}}{2}} V_D(t) \cdot I_D(t) dt \tag{2.5.32}$$

First of all $P(t)$ has to be calculated.

$$\begin{aligned} P(t) &= V_D(t) \cdot I_D(t) \\ &= \frac{\beta}{2} \cdot \left(V_0 \cdot \cos(\omega \cdot t) - \frac{V_{out}}{2 \cdot n} - V_T \right)^2 \cdot \left(V_0 \cdot \cos(\omega \cdot t) - \frac{V_{out}}{2 \cdot n} \right) \\ &= \frac{\beta}{2} \cdot \left\{ V_0^3 \cdot \cos^3(\omega \cdot t) - V_0^2 \cdot \cos^2(\omega \cdot t) \cdot \left(3 \cdot \frac{V_{out}}{2 \cdot n} + 2 \cdot V_T \right) \right. \\ &\quad + V_0 \cdot \cos(\omega \cdot t) \cdot \left[\left(\frac{V_{out}}{2 \cdot n} + V_T \right)^2 + \left(\frac{V_{out}}{2 \cdot n} \right)^2 + V_T \cdot \frac{V_{out}}{2 \cdot n} \right] \\ &\quad \left. - \left(\frac{V_{out}}{2 \cdot n} + V_T \right)^2 \cdot \frac{V_{out}}{2 \cdot n} \right\} \end{aligned} \tag{2.5.33}$$

Those frequency components of the voltage and current that match contribute to real power. Due to the fact that only the real power causes power dissipation, exactly these frequency components are of interest. Using (2.5.26) and (2.5.34) leads to (2.5.35).

$$\cos^3(x) = \frac{1}{4} \cdot \cos(3 \cdot x) + \frac{3}{4} \cdot \cos(x) \tag{2.5.34}$$

$$P(t) = \frac{\beta}{2} \cdot \left\{ \frac{1}{4} \cdot V_0^3 \cdot \cos(3 \cdot \omega \cdot t) - \frac{1}{2} \cdot V_0^2 \cdot \left(3 \cdot \frac{V_{out}}{2 \cdot n} + 2 \cdot V_T \right) \cdot \cos(2 \cdot \omega \cdot t) \right.$$
$$+ V_0 \cdot \cos(\omega \cdot t) \cdot \left[\frac{3}{4} \cdot V_0^2 + \left(\frac{V_{out}}{2 \cdot n} + V_T \right)^2 + 2 \cdot \left(\frac{V_{out}}{2 \cdot n} \right)^2 + 2 \cdot V_T \cdot \frac{V_{out}}{2 \cdot n} \right] \tag{2.5.35}$$
$$\left. - \frac{1}{2} \cdot V_0^2 \cdot \left(3 \cdot \frac{V_{out}}{2 \cdot n} + 2 \cdot V_T \right) - \left(\frac{V_{out}}{2 \cdot n} + V_T \right)^2 \cdot \frac{V_{out}}{2 \cdot n} \right\}$$

The dissipated real power can thus be calculated as:

$$P_D(t) = P_{D_{DC}}(t) + P_{D_{AC}}(t) \tag{2.5.36a}$$

$$P_{D_{DC}}(t) = -\frac{\beta}{2} \cdot \left\{ \frac{1}{2 \cdot n} \cdot V_{out} \cdot \left[\frac{V_0^2}{2} + \left(\frac{V_{out}}{2 \cdot n} + V_T \right)^2 \right] + V_0^2 \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T \right) \right\}$$
$$= -\frac{1}{2 \cdot n} \cdot P_{out} - \frac{\beta}{2} \cdot V_0^2 \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T \right) \tag{2.5.36b}$$

$$P_{D_{AC}}(t) = \frac{\beta}{8} \cdot V_0 \cdot \cos(\omega \cdot t)$$
$$\cdot \left[3 \cdot V_0^2 + 4 \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T \right)^2 + 8 \cdot \frac{V_{out}}{2 \cdot n} \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T \right) \right] \tag{2.5.36c}$$

From (2.5.36) the average dissipated power by one transistor can be determined to be:

$$P_D = \frac{1}{T} \cdot \int_{-\frac{T_{on}}{2}}^{\frac{T_{on}}{2}} P_D(t) dt \tag{2.5.37}$$

The diode-connected transistors are conductive if the input voltage is $\frac{V_{out}}{2 \cdot n} + V_T$ or higher. To solve (2.5.37) the time in which the transistors are conductive (see Figure 2.27) is required. This time can be determined as follows: From the assumptions above the input voltage at $\frac{T_{on}}{2}$ is $\frac{V_{out}}{2 \cdot n} + V_T$ as shown in Figure 2.27. This condition can be described by:

$$V_0 \cdot \cos\left(\omega \cdot \frac{T_{on}}{2} \right) = \frac{V_{out}}{2 \cdot n} + V_T \tag{2.5.38}$$

(2.5.38) can thus be rewritten to express T_{on}:

$$T_{on} = \frac{2}{\omega} \cdot \arccos\left[\left(\frac{V_{out}}{2 \cdot n} + V_T \right) \cdot \frac{1}{V_0} \right] \tag{2.5.39}$$

Inserting (2.5.36) in (2.5.37) leads to (2.5.40), which is the power dissipated by one diode-connected transistor.

$$P_D = \frac{1}{T} \cdot \int_{-\frac{T_{on}}{2}}^{\frac{T_{on}}{2}} P_{D_{DC}}(t) dt + \frac{1}{T} \cdot \int_{-\frac{T_{on}}{2}}^{\frac{T_{on}}{2}} P_{D_{AC}}(t) dt$$

$$= -\frac{T_{on}}{T} \cdot \left[\frac{P_{out}}{2 \cdot n} + \frac{\beta}{2} \cdot V_0^2 \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T \right) \right] + \frac{\beta}{8 \cdot \pi} \cdot V_0 \cdot \sin\left(\omega \cdot \frac{T_{on}}{2} \right) \tag{2.5.40}$$
$$\cdot \left[3 \cdot V_0^2 + 4 \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T \right)^2 + 8 \cdot \frac{V_{out}}{2 \cdot n} \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T \right) \right]$$

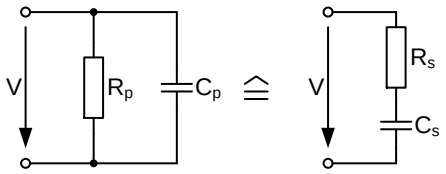


Figure 2.28: Correlation between parallel and series configuration

$$\sin\left(\omega \cdot \frac{T_{on}}{2}\right) = \sin\left\{\arccos\left[\left(\frac{V_{out}}{2 \cdot n} + V_T\right) \cdot \frac{1}{V_0}\right]\right\} = \frac{1}{V_0} \cdot \sqrt{V_0^2 - \left(\frac{V_{out}}{2 \cdot n} + V_T\right)^2} \tag{2.5.41}$$

Now the term $\sin(\omega \cdot \frac{T_{on}}{2})$ is substituted by (2.5.41) and so (2.5.40) can be rewritten as:

$$\begin{aligned} P_D = &-\frac{T_{on}}{T} \cdot \left[\frac{P_{out}}{2 \cdot n} + \frac{\beta}{2} \cdot V_0^2 \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T\right)\right] + \frac{\beta}{8 \cdot \pi} \cdot \sqrt{V_0^2 - \left(\frac{V_{out}}{2 \cdot n} + V_T\right)^2} \\ &\cdot \left[3 \cdot V_0^2 + 4 \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T\right)^2 + 8 \cdot \frac{V_{out}}{2 \cdot n} \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T\right)\right] \end{aligned} \tag{2.5.42}$$

(2.5.42) shows the dissipated power of one diode-connected transistor, neglecting the losses caused by parasitic capacitances, where P_{out} and V_{out} are determined using (2.5.29) and (2.5.7), respectively. As stated in Section 2.5.2.1, if parasitic capacitances of the transistors are taken into account V_0 has to be multiplied by the factor $C_{(2N\text{-}1)}/(C_{(2N\text{-}1)} + C_{par_{(2N\text{-}1)}} + C_{par_{(2N)}})$. Furthermore P_{out} also changes, because the amplitude V_0 used to determine P_{out} changes too.

The dissipated power considering the parasitic capacitances of the transistor is shown in (2.5.43), where V_{out} and C_{par_N} are calculated using (2.5.15) and (2.5.12), respectively.

$$\begin{aligned} P_D = &-\frac{T_{on}}{T} \cdot \left[\frac{P_{out}}{2 \cdot n} + \frac{\beta}{2} \cdot V_0^2 \cdot \left(\frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}}\right)^2 \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T\right)\right] \\ &+ \frac{\beta}{8 \cdot \pi} \cdot \sqrt{V_0^2 \cdot \left(\frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}}\right)^2 - \left(\frac{V_{out}}{2 \cdot n} + V_T\right)^2} \\ &\cdot \left[3 \cdot V_0^2 \cdot \left(\frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}}\right)^2 + 4 \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T\right)^2 \right. \\ &\left. + 8 \cdot \frac{V_{out}}{2 \cdot n} \cdot \left(\frac{V_{out}}{2 \cdot n} + V_T\right)\right] \end{aligned} \tag{2.5.43}$$

$$P_{out} = \frac{\beta}{2} \cdot V_{out} \cdot \left[\frac{V_0^2}{2} \cdot \left(\frac{C_{(2N\text{-}1)}}{C_{(2N\text{-}1)} + C_{par_N}}\right)^2 + \left(\frac{V_{out}}{2 \cdot n} + V_T\right)^2\right]$$

If substrate and n-well losses are considered the dissipated power can be calculated by transforming the series capacitor and resistor in a parallel configuration. Thus, the power dissipation

due to these losses can be easily calculated using (2.5.45) where R_p is:

$$R_p = \frac{\left(\frac{1}{\omega \cdot C_s}\right)^2 + R_s^2}{R_s} \tag{2.5.44}$$

$$P_{D_{\text{ohmic losses}}} = \frac{V^2}{R_p} = \frac{V_0^2}{2} \cdot \frac{R_s}{R_s^2 + (\omega \cdot C_s)^{-2}}, \tag{2.5.45}$$

where V_0 is the amplitude of the input voltage V, C_s and R_s are the capacitor and its ohmic loss in series, and C_p and R_p are the capacitor and its ohmic loss in parallel, respectively. Figure 2.28 shows this correlation.
Due to the fact that the resistivity of the substrate and the n-well are low enousgh that $\omega \cdot C_s \cdot R_s << 1$, the following approximation can be done as shown in [53]:

$$P_{D_{\text{ohmic losses}}} \approx \frac{V_0^2}{2} \cdot (\omega \cdot C_s)^2 \cdot R_s \tag{2.5.46}$$

As clearly evident from (2.5.46) the power dissipation caused by substrate and n-well losses increases with the frequency, parasitic capacitances and their ohmic losses.

The total power dissipation caused by substrate and n-well losses of an n-stage voltage multiplier can thus be calculated using (2.5.47).

$$P_{D_{total\,\text{ohmic losses}}} = n \cdot \left(P_{D_{R\_M(2N\text{-}1)}} + P_{D_{R\_M(2N)}}\right), \tag{2.5.47}$$

where $P_{D_{R\_M(2N\text{-}1)}}$ and $P_{D_{R\_M(2N1)}}$ differ depending on the transistor type as shown in (2.5.48). $P_{D_{R\_M(2N\text{-}1)}}$ is calculated using (2.5.48a) for an NMOS and (2.5.48c) for a PMOS transistor. In the same way $P_{D_{R\_M(2N)}}$ is calculated using (2.5.48b) for an NMOS and (2.5.48c) for a PMOS transistor. For these calculations the major parasitic capacitance of the respective transistor is considered.

$$P_{D_{NMOS\ vertical\ \text{ohmic losses}}} = \frac{V_0^2}{2} \cdot \frac{R_{sub}}{R_{sub}^2 + (\omega \cdot C_{BS})^{-2}} \tag{2.5.48a}$$

$$P_{D_{NMOS\ horizontal\ \text{ohmic losses}}} = \frac{V_0^2}{2} \cdot \frac{R_{sub}}{R_{sub}^2 + (\omega \cdot C_{BD})^{-2}} \tag{2.5.48b}$$

$$P_{D_{PMOS\ vertical\ \text{ohmic losses}}} = P_{D_{PMOS\ horizontal\ \text{ohmic losses}}} = \frac{V_0^2}{2} \cdot \frac{R_{n\text{-}well}}{R_{n\text{-}well}^2 + (\omega \cdot C_{BS})^{-2}} \tag{2.5.48c}$$

The dissipated power of an n-stage voltage multiplier considering the major parasitics effects (index $_{\text{incl. par.}}$), which are caused by parasitic capacitances, substrate and n-well losses can thus be calculated using (2.5.49). For P_D (2.5.43) and for $P_{D_{R\_M(2N\text{-}1)}}$ and $P_{D_{R\_M(2N)}}$ (2.5.48) are used, respectively.

$$\begin{aligned} P_{D_{total\,(\text{incl. par.})}} &= 2 \cdot n \cdot P_D + P_{D_{total\,\text{ohmic losses}}} \\ &= n \cdot \left(2 \cdot P_D + P_{D_{R\_M(2N\text{-}1)}} + P_{D_{R\_M(2N)}}\right) \end{aligned} \tag{2.5.49}$$

As obvious from (2.4.29a), the input power can be calculated as:

$$P_{in} = P_{out} + P_{D_{total}} \tag{2.5.50}$$

Using (2.5.49) leads to the necessary input power considering the major parasitics effects:

$$P_{in\,(\text{incl. par.})} = P_{out} + n \cdot \left(2 \cdot P_D + P_{D_{R\_M(2N\text{-}1)}} + P_{D_{R\_M(2N)}}\right) \tag{2.5.51}$$

Now the PCE, often labeled with η and defined in (2.4.8) and (2.4.11), can be calculated by:

$$PCE = \eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{D_{total}}} = 1 - \frac{P_{D_{total}}}{P_{in}} \tag{2.5.52}$$

Depending on how accurately the PCE should be determined, more or fewer parasitic effects have to be taken into account. The fewer parasitics are considered the higher the PCE.

The PCE considering the major parasitics effects $PCE_{(\text{incl. par.})}$ can be determined to be:

$$\begin{aligned} PCE_{(\text{incl. par.})} &= \frac{P_{out}}{P_{out} + n \cdot \left(2 \cdot P_D + P_{D_{R\_M(2N\text{-}1)}} + P_{D_{R\_M(2N)}}\right)} \\ &= 1 - \frac{n \cdot \left(2 \cdot P_D + P_{D_{R\_M(2N\text{-}1)}} + P_{D_{R\_M(2N)}}\right)}{P_{in}} \end{aligned} \tag{2.5.53}$$

As evident from (2.5.53), the PCE decreases with the number of stages and of course with the amount of power dissipated per diode-connected transistor. This power dissipation again depends on various factors like the transistor design itself (type, geometry, gain, threshold voltage), the output characteristics, the operating frequency and the maximal achievable loaded Q Factor. Furthermore these factors are more or less interrelated. So it seems to be very tricky to design a reasonable voltage multiplier. However, the best one can do is to use as few as possible stages to achieve the required specification, taking the maximal achievable loaded Q Factor into account.

2.6 Simulation of Power Scavenging Units and Non-Linear Circuits

In this section simulation techniques for circuits with large signal behavior are presented. Due to the size of the input amplitudes and voltage differences in a PSU, large signal excitation has to be considered. To achieve reasonable simulation results it is necessary to sufficiently feed the power from the source to the chip. Therefore the matching conditions have to be determined. Small signal simulation methods achieve inaccurate or even incorrect results especially for the input impedance. This shows the need for a simulation method that covers the large signal behavior of the circuit. The important parameters can only be correctly determined if a large signal simulation is performed.

2.6.1 Periodic Steady-State Analysis

As stated in [24], the rectifying characteristic of the diode-connected transistors is based on the positive resistive nonlinear effect [86]. This large signal behavior has to be considered in the design and dimensioning of the PSU. Due to the also nonlinear characteristic of the transistor-based AC/DC converter the steady-state response of the circuit is of interest. Of course this result can be achieved with transient analysis, but due to the high operating frequency many of time steps are necessary, which increases the simulation time. Additionally interesting parameters like the input power of the voltage multiplier or the complex reflection coefficient and the complex source impedance to achieve matching are very difficult to determine. Therefore the Periodic Steady-State (PSS) analysis in combination with the Periodic S-Parameter (PSP) analysis coming with Spectre® circuit simulator of Cadence® design systems is used. The PSP analysis is a periodic small signal analysis that is performed after the PSS analysis. This analysis starts by linearizing the circuit about the periodically time varying operating point computed by the preceding PSS analysis. Then this operating point is used to predict the response of the circuit to a small sinusoidal excitation at an arbitrary frequency [9].

Spectre® uses either the Shooting Method or the Flexible Balance Method to compute the PSS response of a circuit. If the Flexible Balance Method is selected in the PSS analysis a harmonic balance analysis is performed. The Spectre® harmonic balance engine supports frequency domain harmonic balance analyses and provides efficient and robust simulation for linear and weakly nonlinear circuits [9].

2.6.1.1 Harmonic Balance

The harmonic balance simulation is based on the principle of partitioning the circuit into its linear and nonlinear parts and analyzing the linear sub-circuit in the frequency domain and the nonlinear sub-circuit in the time domain, respectively. A system of n nonlinear ordinary differential equations represents the circuit in the simulator, where n is the number of node voltages and branch currents in the circuit.

The harmonic balance algorithm can be explained as follows [40]: The frequency domain independent variables are defined as $x(t)$ in the time domain and as $X(f)$ in the frequency domain respectively. These independent variables are current (voltage) phasors for impedance (admittance) type elements, while the dependent variables are voltage (current) phasors respectively. $y(t)$ and $Y(f)$ are used to define the dependent variables in the time and frequency domain respectively. By using the index n, the independent and dependent variables, which are the currents and voltages in the circuit, can be allocated a specific node in the circuit. That means, the independent variables are denoted with $x_n(t)$ and $X_n(f)$, while the dependent variables are denoted with $y_n(t)$ and $Y_n(f)$, respectively.

The objective of the harmonic balance procedure is to "balance" the response of the linear elements ($\widetilde{Y}$) with that of the non-linear elements (Y). Therefore Fourier analysis is utilized.

Relations between the currents and voltages in the frequency and time domain are shown in (2.6.1).

$$x_n(t) = \mathscr{F}^{-1}\{X_n(f)\} \quad \leftrightarrow \quad X_n(f) = \mathscr{F}\{x_n(t)\} \tag{2.6.1a}$$

$$y_n(t) = \mathscr{F}^{-1}\{Y_n(f)\} \quad \leftrightarrow \quad Y_n(f) = \mathscr{F}\{y_n(t)\} \tag{2.6.1b}$$

$$y_n(t) = h(x_n(t)) \tag{2.6.1c}$$

The algorithm uses Kirchoff's current law in the frequency domain. At each node n which is common to both the linear and nonlinear part of the circuit, the voltage of the linear part in the frequency domain ($\widetilde{Y}_n(f)$) is determined. For the same node in the nonlinear part the current ($X_n(f)$) is inverse Fourier transformed (see (2.6.1a)) into the time domain ($x_n(t)$). Hence $y_n(t)$ can be determined as shown in (2.6.1c). Now $y_n(t)$ is Fourier transformed (see (2.6.1b)) into the frequency domain ($Y_n(f)$) and compared with the result of the linear part.

$$Y_n(f) - \widetilde{Y}_n(f) < \epsilon \tag{2.6.2}$$

Usually the results of the linear and non-linear part of the circuit do not match after the initial calculation. Thus the error function shown in (2.6.2), which is the mismatch between the results of the dependent variables of the linear and non-linear part of the circuit, is minimized by an iterative process. In this process better estimates for all independent variables are iteratively selected, as long as a defined residual is achieved. Different iterative processes can be used to solve (2.6.2), usually the Newton-Raphson method is utilized [21]. Newton's method generates a linear system of equations at each iteration which is solved using the Jacobian matrix.

Circuits with multiple input sources require a multitone excitation. Thus, a multidimensional truncated Fourier series is used to approximate the steady state solution. The harmonic balance algorithm follows the same principle as explained above for circuits with a single input source.

2.6.1.2 Shooting Method

The Shooting Method is a time domain method that operates by efficiently finding an initial condition that directly results in steady state [9, 10]. As stated in [9] and in [10], the Spectre® Shooting Method can be used to simulate strongly nonlinear circuits. Due to the fact that this method exceeds the accuracy of harmonic balance simulators, it is used to simulate the energy harvesting system.

The PSS analysis used consists of two phases as explained in [10]: The first phase is the initial transient phase. In this phase a standard transient analysis is performed to initialize the circuit.
The second phase is the shooting phase. In this phase the PSS solution is computed.
For strongly nonlinear circuits it might be necessary to move the shooting interval starting point by adding additional stabilization time. That means the shooting method is started after this time. This has to be done if the shooting method does not converge or if it converges

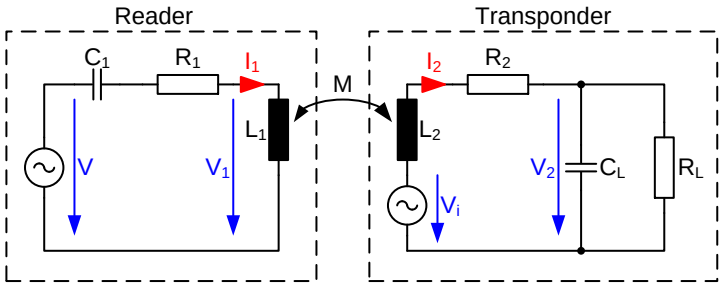


Figure 2.29: Equivalent circuit of an HF RFID system

to incorrect and unreasonable results. Increasing the additional stabilization time usually leads to faster and easier convergence of strongly nonlinear circuits.
To prove that a correct simulation solution is achieved, a transient check simulation and/or several PSS analyses can be performed that differ only in the additional stabilization time. The results of the different simulations should be quite similar. If not, the additional stabilization time has to be varied and/or the simulator accuracy parameters are not set sufficiently tight.

2.6.2 Test Bench

To simulate a PSU some kind of energy source is required. Usually a power source or an antenna are used. The antenna collects the energy from the electro-magnetic field and provides it at the input of the PSU. To gain a simulation setup that behaves almost like the real system, an equivalent circuit of the chip as well as of the receiving antenna is developed. Thus, the interface between the antenna, which is the source, and the chip, which is the load of the antenna, has to be emulated.

Usually chips are simulated with different test benches at HF and UHF due to different operating principles concerning the interface between transmitting and receiving antenna (near and far field propagation) and different strategies in the antenna design.

2.6.2.1 HF Considerations

Figure 2.29 shows the equivalent circuit of an HF RFID system that is also used as the basis for circuit simulation and measurement. The equivalent chip capacitor including the tuning capacitor (C_L) and the coil of the transponder antenna (L_2) form a resonant circuit tuned to the excitation frequency of the source. R_1 and R_2 are the coil resistances. In RFID systems the reader is the source. Of course this HF RFID reader can be used to power HF RFID transponders as well as every PSU operating at HF. To maximize the emitted magnetic field at fixed antenna dimensions the current delivered to the antenna has to be maximized. In order to obtain the maximum current in the reader antenna coil, it must resonate at the excitation frequency provided by the reader circuit. Therefore a series resonant circuit is created by the

symbol	description
V_i	induced coil voltage
V	electric voltage
I	electric current
N	number of coil loops of same size
Ψ	total magnetic flux
Φ	magnetic flux through one loop
B	magnetic flux density
H	magnetic field strength
A	coil area over which the field is integrated
r	radius of the conductor loop
M	mutual inductance
k	coupling coefficient
μ_0	magnetic constant
μ_r	relative permeability (in air ≈ 1)

Table 2.7: List of symbols for equations in Section 2.6.2.1 and 2.7.1

serial connection of the capacitor C_1 to the reader antenna coil, which generates the magnetic alternating field.

If performing a simulation using the equivalent circuit shown in Figure 2.29, the reader including the reader antenna, the inductive coupling to the transponder, and the transponder antenna are considered. Due to the fact that input voltage of the chip depends on the transponder antenna parameters and the loaded Q Factor (Q Factor of the transponder antenna connected to the chip), the input voltage of the chip at HF is more meaningful during the design phase. Thus the simulations at HF can be performed using the same test bench developed for UHF and shown in Section 2.6.2.2. Nevertheless the important equations to calculate some key parameters, like the field strength in simulation or the input voltage of the chip using the measured field strength, are given below. The concerning background and information are given in more detail in [33, 55, 64].

Analysis of the Inductive Coupled System

A description of the symbols in Section 2.6.2.1 and 2.7.1 is given in Table 2.7.

In general the inductance is defined as the ratio of the magnetic flux induced by the current flowing through the inductor to the amount of the current itself as shown in (2.6.3).

$$L = \frac{\Psi}{I} \tag{2.6.3}$$

Mutual inductance occurs in an HF RFID system because the change of the current in the conductor loop L_1 induces a voltage in the conductor loop L_2, which is placed in the vicinity of L_1 as shown in Figure 2.30. Similarly to the definition of the inductance, the mutual inductance M_{21} (see (2.6.4)) of the conductor loop L_2 in relation to the conductor loop L_1 is

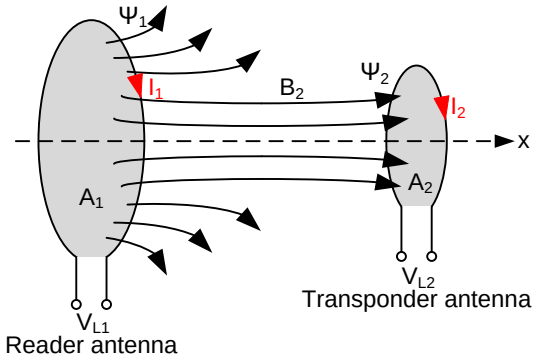


Figure 2.30: Illustration of the mutual inductance

defined as ratio of the magnetic flux Ψ_2 enclosed by the conductor loop L_2 to the current I_1, which generates Ψ_2.

$$\begin{aligned} M_{21} &= \frac{\Psi_2}{I_1} \\ \Psi_2 &= f(I_1) \end{aligned} \tag{2.6.4}$$

$$\Psi = \oint_A \frac{B}{I} \cdot dA \tag{2.6.5a}$$

$$B = \mu \cdot H = \mu_0 \cdot \mu_r \cdot H \tag{2.6.5b}$$

Assuming $\mu_r = 1$ and inserting the definitions of the magnetic flux and the magnetic flux density (see (2.6.5)) in (2.6.4) leads to:

$$\begin{aligned} M_{21} &= \oint_{A_2} \frac{B_2}{I_1} \cdot dA_2 = \frac{\mu_0 \cdot H_2 \cdot N_2 \cdot A_2}{I_1} \\ H_2 &= f(I_1), B_2 = f(I_1) \end{aligned} \tag{2.6.6}$$

Due to the fact that the mutual inductance from loop 2 to loop 1 is the same as the mutual inductance from loop 1 to loop 2 the following relationship applies:

$$M_{21} = M_{12} = M \tag{2.6.7}$$

Using the Biot-Savart law the magnetic field strength along the symmetries axis (x axis) of the conductor loops can be calculated as:

$$H = \frac{I \cdot N \cdot r^2}{2 \cdot \sqrt{(r^2 + x^2)^3}}, \tag{2.6.8}$$

where x is the distance between the two inductor loops on the same plane as shown in Figure 2.30. Replacing A_2 with the $r_2^2 \cdot \pi$ and H_2 with (2.6.8) leads to:

$$M = \frac{\mu_0 \cdot N_1 \cdot N_2 \cdot r_1^2 \cdot r_2^2 \cdot \pi}{2 \cdot \sqrt{(r_1^2 + x^2)^3}} \tag{2.6.9}$$

(a) Antenna (b) IC

Figure 2.31: Equivalent circuits of the impedances of an RFID transponder

The mutual inductance also has a relationship with the coupling coefficient, which is used to specify the coupling between a certain orientation of the conductor loops with arbitrary inductance. The coupling coefficient is defined as:

$$k = \frac{M}{\sqrt{L_1 \cdot L_2}} \tag{2.6.10}$$

To calculate the input voltage of the chip (transponder) Kirchhoff's Voltage Law is applied.

$$V_2 = V_i - L_2 \cdot \frac{dI_2}{dt} - R_2 \cdot I_2 \tag{2.6.11}$$

$$V_i = M \cdot \frac{dI_1}{dt} = \jmath\omega M \cdot I_1 \tag{2.6.12a}$$

$$I_2 = \frac{V_2}{Z_T} \tag{2.6.12b}$$

$$Z_T = \frac{1}{\frac{1}{R_L} + \jmath\omega C_L} \tag{2.6.12c}$$

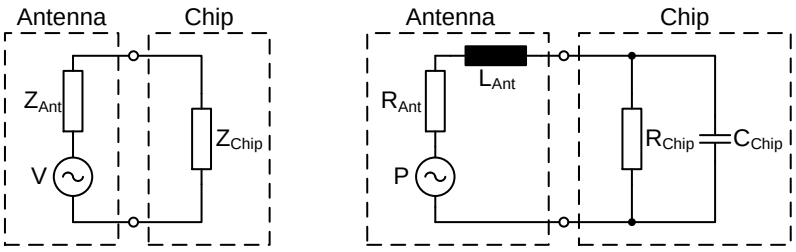
Replacing V_i by the factor responsible for its generation and using Ohm's Law to express the current I_2 as shown in (2.6.12) leads to:

$$V_2 = \frac{\jmath\omega M \cdot I_1}{1 + (\frac{1}{R_L} + \jmath\omega C_L) \cdot (R_2 + \jmath\omega L_2)} \tag{2.6.13}$$

To calculate the field strength from the input voltage of the chip, only M in (2.6.13) has to be replaced with (2.6.6).

The last important key parameter listed here is the Q Factor of the chip connected to the antenna. The Q Factors of the antenna and the chip can be calculated separately and then the overall Q Factor can be achieved by:

$$Q = \frac{1}{\frac{1}{Q_A} + \frac{1}{Q_C}} \tag{2.6.14}$$



(a) Simplified circuit (b) Detailed circuit

Figure 2.32: Equivalent circuits of an RFID transponder

Q_A and Q_C can be calculated using the equivalent circuits shown in Figure 2.31 to be:

$$Q_A = \frac{\omega L_2}{R_2} \tag{2.6.15a}$$

$$Q_C = \frac{R_L}{\frac{1}{\omega C_L}} = \omega R_L C_L \tag{2.6.15b}$$

At resonance (2.6.16) is valid.

$$\omega C_L = \frac{1}{\omega L_2} \tag{2.6.16}$$

To obtain resonance frequencies around 13 MHz the additional tuning capacitor C_2 is needed in parallel to the chip, which is already considered in (2.6.15):

$$C_L = C_2 + C_{Chip} \tag{2.6.17}$$

Inserting (2.6.16) and (2.6.15) in (2.6.14) leads to the loaded Q Factor of the chip connected to the antenna:

$$Q = \frac{1}{\frac{R_2}{\omega L_2} + \frac{\omega L_2}{R_L}} \tag{2.6.18}$$

2.6.2.2 UHF Considerations

As stated in [85], the equivalent circuit of the receiving antenna is represented by a Thévenin equivalent generator and an equivalent antenna impedance. This Thévenin equivalent generator is the open-circuit voltage at the antenna terminals. In this case the chip can be seen as the loaded PSU. Figure 2.32a shows this simplified equivalent circuit. The chip impedance can be represented in a parallel or serial way by an equivalent circuit consisting of a resistor and a capacitor. In this work the equivalent circuit of the chip is built up by a resistor and a capacitor in parallel as shown in Figure 2.32b. This representation is also more meaningful for

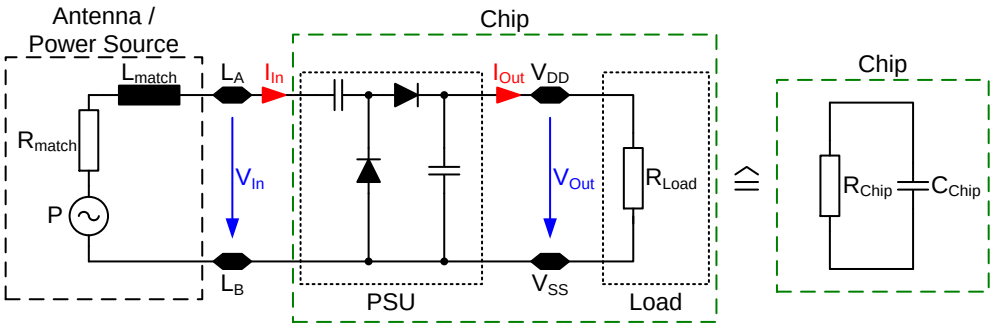


Figure 2.33: Testbench of a UHF RFID system

RFID transponders, especially if the shunt behavior is analyzed. The conversion from parallel to series is described by (2.6.19) [8]:

$$Q_P = \frac{R_P}{X_P} \tag{2.6.19a}$$

$$Q_S = \frac{X_S}{R_S} \tag{2.6.19b}$$

$$R_S = \frac{R_P}{1 + Q_P^2} \tag{2.6.19c}$$

$$R_P = R_S \cdot (1 + Q_S^2) \tag{2.6.19d}$$

$$Q = Q_P = Q_S \tag{2.6.19e}$$

As stated in Section 2.4.2 the main aim in the design is a high PCE for the desired operating conditions. To determine the PCE the input power as well as the output power of the PSU have to be known. Furthermore the developed chip is tested and verified using measurement equipment.

An important key parameter for remotely powered devices, especially for RFID transponders, is the input sensitivity which is the minimum input power sufficient to operate the chip. Determining the minimum input power is a key issue in simulation as well as in measurement. For the reasons listed above, the equivalent circuit shown in Figure 2.32a thus has to be modified as shown in Figure 2.32b. The Thévenin voltage source is replaced by a power source in which output power is equivalent to the power received by the antenna. Depending on the matching between the source (antenna) and the chip between 0 and 100 % of the power available at the source (antenna) is delivered to the chip.
The frequency variant antenna impedance is represented by an ohmic resistor and an inductor in series. The resistor is used to match the real part of the source impedance to the real part of the chip impedance. Due to the capacitive behavior of the chip, inductive matching is used to also achieve imaginary matching by the series inductor. The equivalent matching approach is also applied in the antenna design.

With an equivalent circuit emulating the behavior of the source (antenna) and the chip sufficiently, it is possible to use it as test bench in circuit simulation. For the simulation of a PSU

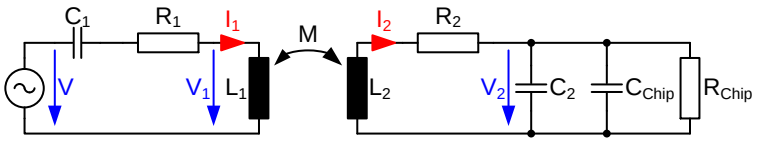


Figure 2.34: Equivalent circuit of the measurement setup of an HF RFID system

the load can be represented by an ohmic resistor connected to the DC output of the PSU. The test bench is shown in Figure 2.33. As stated above a power source with sinusoidal output voltage is used as the source (antenna). The matching network is built by a resistor and an inductor in series to the power source. With conjugate matching ($\underline{Z}_{Chip} = \underline{Z}^*_{Ant}$) the maximum power is delivered to the input of the PSU.

Due to the fact that the equivalent parallel capacitor (see Figure 2.32b), representing the chip capacitance, hardly changes with the input amplitude, the AC (small signal) analysis can be used to approximate the inductance used for imaginary matching before the large signal analysis is performed. The solution of the PSS analysis is compared with the solution of the transient analysis to check if the results of the PSS analysis are reasonable.

2.7 Measurement Methods of Power Scavenging Units and Non-Linear Circuits

In this section methods to perform measurements on PSUs and passive RFID transponder chips are presented.
Due to the significantly different operating frequencies at HF (13.56 MHz) and UHF (860 MHz to 960 MHz and 2.45 GHz) different measurement methods and setups are utilized. Systems operating at HF work in the near field and employ inductive coupling of the transponder to the reactive energy circulating around the transmitting antenna. In contrast those systems operating at UHF work in the far field and couple to the real power contained in free space propagating electromagnetic plane waves [64].

2.7.1 Determination of the Minimum Electrical Field Strength at HF

At HF the minimum electrical field strength is determined by using the measurement setup and methods described in [44]. The measurement setup is contactless, which means the chip is connected to an antenna. A source (in RFID systems the reader antenna coil) generates an electromagnetic field with a frequency of 13.56 MHz. A part of the emitted field penetrates the receiving antenna coil (in RFID systems the transponder antenna coil). Due to the inductive coupling between the transmitting and receiving antennas, a voltage is induced in the transponder antenna coil.

The optimization criterion for the transponder antenna is to deliver maximum voltage to the chip input. This can be achieved by creating a parallel resonant circuit which is built up by the

transponder antenna coil, the input impedance of the chip, and an additional capacitance C_2 which is, as usual, realized by an external trimming capacitor mounted on the antenna's PCB. Figure 2.34 shows the equivalent circuit of the measurement setup. L_1 and L_2 are magnetically coupled conductor loops. R_1 and R_2 are the coil and wiring resistances. As already explained in Section 2.6.2.1, C_1 is used to form a series resonant circuit that corresponds with the transmission frequency of the reader.

One of the key parameters of passive HF RFID transponders is the minimum field strength H_{min}. H_{min} is defined as the minimum interrogation field strength of a transponder at a maximum distance between the reader and the transponder at which the chip input voltage (V_2 in Figure 2.34) is just sufficient for operation [33]. V_2 is rectified by the PSU of the chip and provides the DC voltage necessary for operation. It is obvious that it does not matter whether an RFID transponder or a stand-alone PSU is connected to the transponder antenna.

For the measurement procedure it is necessary to determine the chip input voltage that is just sufficient for operation.
If measuring a stand-alone PSU is it useful to define a distinct DC output load and voltage at which H_{min} is going to be determined. It is obvious that the higher the load the higher H_{min}. An HF RFID transponder operates correctly as long as it responds correctly to the reader commands. Thus, the minimum input field strength necessary for correct operation can be determined by observing the response of the chip. Therefore the method defined in [44] to determine the response of the chip is utilized. The electromagnetic field strength is lowered as long as the chip responds. Now it is of interest to determine this minimum field strength H_{min}.

The Faraday's law states that the induced voltage (electromotive force) in any conductor loop is equal to the time rate of change of the magnetic flux through the circuit [92]:

$$V_i = -\frac{d\Psi}{dt}, \tag{2.7.1}$$

where Ψ is the magnetic flux through the circuit.

$$V_i = -N \cdot \frac{d\Phi}{dt} \tag{2.7.2a}$$

$$\Phi = B \cdot A \tag{2.7.2b}$$

$$B = \mu \cdot H = \mu_0 \cdot \mu_r \cdot H \tag{2.7.2c}$$

For a coil consisting of N loops the total induced voltage can be calculated using (2.7.2).

From (2.7.2) the induced voltage in the coil can be derived as:

$$V_i = \omega \cdot N \cdot \mu_0 \cdot \mu_r \cdot H \cdot A \tag{2.7.3}$$

Using a sense coil as defined in [44], the voltage induced is this coil can simply be measured using an oscilloscope. Assuming a homogeneous, sinusoidal magnetic field in the air (consideration:

$\mu_r = 1$) and inserting the sense coil data ($A = 3000\,\mathrm{mm}^2, N = 1$) at an operating frequency of 13.56 MHz ($\omega = 2\pi f$), the field strength can be calculated as:

$$H = \frac{V_i}{\omega \cdot N \cdot \mu_0 \cdot A} = \frac{V_i}{0.32} \tag{2.7.4}$$

To obtain the root mean square of the field strength using the peak to peak value derived from the oscilloscope, (2.7.5) has to be used, thus H_{rms} follows as:

$$H_{rms} = \frac{V_i}{\omega \cdot N \cdot \mu_0 \cdot A \cdot 2 \cdot \sqrt{2}} = \frac{V_{i_{pp}}}{0.91} \tag{2.7.5}$$

2.7.2 Determination of the Power Requirements at UHF

As the input sensitivity is one of the most important parameters characterizing UHF RFID tags, recent publications cover this topic. Sensitivity and impedance measurements that also consider the influence of the RFID-specific commands are presented in [84]. A novel procedure to determine the impedance by using three characterized impedances is presented in [58]. In [114], a reader and a tunable attenuator are used to supply the chip while observing the communication. The output power of the reader lowered by the tunable attenuator corresponds with the input power of the chip, which is determined by a power meter. All these presented procedures only work as long as the chip impedance leads to an acceptable reflection coefficient if connected to 50 Ω. In addition to it the nonlinear behavior is not considered.

Depending on the impedance of the Device Under Test (DUT) and thus the resulting measurement error, impedance matching may or may not be required to achieve an acceptable reflection coefficient. For the presented ICs in Chapter 3 and 4 impedance matching is necessary.

For the sake of completeness it is mentioned here that large signal measurements and nonlinear characterization of an analog frontend are performed in [24, 28], whereas this method came up two years after the publication of the methods presented in this section [37].

This section focuses on the use of non-expensive laboratory equipment for measuring the input sensitivity. Nevertheless, the proposed methods provide accurate results. The nonlinear behavior of a PSU and the fact that its input impedance is usually far away from 50 Ω complicate the measurement. Therefore losses and behavior of the setup are calculated and analyzed in detail. As explained in at the beginning of this chapter, the PSUs distinguish in their input structure. Depending on this input structure, the measurement setup also varies. Thus, single-ended and differential structures are treated separately. Since the antenna plays an important role, its behavior is also considered. Still, in contrast to the measurement setup at HF, this setup is contact-based.

The input sensitivity or chip sensitivity threshold was already defined in Section 2.1.1 as the amount of RF input power sufficient to turn on the chip. This means first a suitable method to determine whether the chip operates or not is necessary. Different methods are utilized for the different types of chips:

- Whether a UHF RFID transponder is turned on or not can be determined by observing its input impedance. Usually a so-called power-on reset signal enables the digital core if the supply voltage is sufficiently high. Due to the higher current consumption, the input impedance changes significantly. This significant change can be observed using a vector network analyzer performing a power sweep.
- If additional signals like the power-on reset or the supply voltage are accessible from outside (e.g. via pins), these signals can also be used to indicate whether the input power is sufficient or not.
- Especially for stand-alone PSUs, it is useful to define an output voltage and current (usually the input power characteristics of the device(s) supplied by the PSU) at which the necessary RF input power should be determined. As a matter of course the output voltage and current have to be observed during the determination of the input power.

As already introduced in Section 2.6.2.2, the equivalent circuit of the chip connected to a receiving antenna can be represented by a resistor and a capacitor in parallel emulating the chip and a power source with a source impedance represented by an ohmic resistor and an inductor in series. This frequency variant antenna impedance is used to achieve matching between the antenna (power source) and the chip. In a more general case, the impedances between the antenna and the chip are mismatched. Thus, the power delivered to the load can be calculated by using the reflection coefficient $\underline{S}_{11}$:

$$P_r = P_{r,max} \cdot \left(1 - |\underline{S}_{11}|^2\right) \tag{2.7.6}$$

The operating range or the necessary output power of the transmitting antenna can be calculated by the Friis transmission equation (see (2.4.9) on page 23).

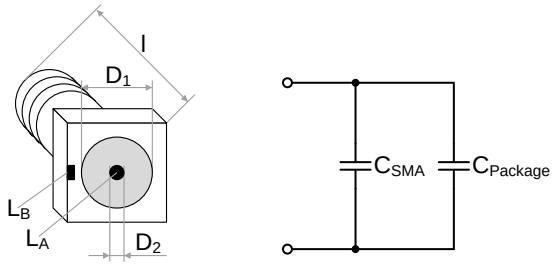
Knowing that the antenna consists of a power source and a matching circuit, it is possible to emulate its behavior by using measurement equipment. Using a network analyzer which represents the power source with a $50\,\Omega$ resistor and an external matching network leads to the required structure. A so-called tuner is utilized as matching network. This device is represented by a L-, Π-, or T-section network of passive components [85].

Certainly, the ohmic impedance of the network analyzer differs from the ohmic impedance of the antenna. Assuming that the tuner is lossless, the maximum power ($P_{r,max}$) is delivered in the matching case. Nevertheless, if the system's achievable bandwidth is examined, the difference in the ohmic impedances does matter. The impedance of the network analyzer or of the antenna is directly represented by the loaded Q Factor. As the Q Factor is inversely proportional to the bandwidth, the achievable frequency range is changed. If the real part of the chip impedance is smaller than the impedance of the used network analyzer, the bandwidth in the measurement system will be larger than in the real system. This can be easily approved by:

$$BW_{-3\,\mathrm{dB}} = \frac{f_0}{Q} = \frac{f_0}{\frac{\Im\{\underline{Z}_{IC}\}}{\Re\{\underline{Z}_{IC}\} + R_{Ant/NA}}} \tag{2.7.7}$$

symbol	description
$BW_{-3\,\mathrm{dB}}$	-3 dB bandwidth
f_0	center frequency
$\underline{Z}_{IC}$	chip impedance
$R_{Ant/NA}$	resistance of the antenna / network analyzer

Table 2.8: List of symbols for (2.7.7)



(a) SMA connector (b) Equivalent circuit

Figure 2.35: Test fixture

A description of the symbols in (2.7.7) is given in Table 2.8. This behavior has to be taken into account if multiple frequencies occur in the measurement system, e.g. if modulation takes place.

2.7.2.1 Characterization of the Measurement Setup

Different measurement setups with several advantages and disadvantages are possible to determine the input power and/or the input impedance of the IC. Depending on the input structure and the input impedance of the chip, the complexity and accuracy of the measurement methods vary. The following considerations are based on unbalanced input structures.

At first a text-fixture is needed because the bare die or the die bonded into a package (in this case a plastic P-DSOF-8-1 package) cannot be connected to the coaxial measurement device. Of course, this fixture must influence the measurement results as little as possible. Due to the fact that the current consumption of the IC is very small, the equivalent series resistor is very small and thus the real part of the IC's impedance is very small. As it will be shown, the capacitance of the measurement fixture and the package transforms the equivalent resistor further to smaller values and thus causes many problems for the measurement process. The farther away the impedance of the DUT from the $50\,\Omega$ (impedance of the network analyzer) the higher the reflection coefficient and thus the measurement error. If a matching network like a stub tuner is used, large Voltage Standing Wave Ratios (VSWRs) are necessary, which may not be available.

Test Fixture

There is no need for an expensive fully RF-characterized fixture. A simple self-made fixture can be used. However, some characterization is necessary. Although the package and the fixture can be considered as lossless, their capacitance must be determined. The simplest fixture is an SMA connector on which the package is soldered. To get an accurate measurement result, the influence of the package and the fixture have to be characterized by developing an equivalent circuit of both. A sketch of the SMA test fixture is depicted in Figure 2.35a. If the top surface is kept as flat as possible, the capacitance of the fixture can be calculated as:

$$C' = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln\frac{D_1}{D_2}} \tag{2.7.8}$$

For a standard SMA connector with a length of 10 mm and Teflon-FEP ($\varepsilon_r = 2.1$) used as isolator, the capacitance is $C_{SMA} = 720\,\text{fF}$. Since the SMA connector has a characteristic impedance of $Z_0 = 50\,\Omega$, the inductance can be calculated using (2.7.9).

$$Z_0 = \sqrt{\frac{L'}{C'}} \tag{2.7.9}$$

As the fixture is very short, the inductance is very small ($L_{SMA} = 1.8\,\text{nH}$). Thus, the fixture's inductance can be neglected.

Package

The characterization of the package can be done by measurement because the SMA test fixture is already characterized. An empty package soldered on the SMA test fixture is used as DUT. Figure 2.35b shows the equivalent circuit. The result of the impedance measurement of the network analyzer is the capacitance of the package and the fixture. De-embedding the fixture's capacitance leads to the capacitance of the package. Thus, the capacitance of the used P-DSOF-8-1 package is determined to be: $C_{Package} = 400\,\text{fF}$.

2.7.2.2 Conventional Measurement Setup

A fast, simple, and widespread measurement method is to connect the DUT (IC bonded into a package and soldered onto the SMA test fixture) to a network analyzer. While observing the supply voltage of the chip or the chip impedance, the power of the network analyzer has to be increased. The power consumed by the DUT can then be calculated with (2.7.6). However the determined value of input power is very inaccurate. As already mentioned, the higher the reflection coefficient the higher the measurement error. Using this measurement setup results in a high reflection coefficient because the large capacitance of the package and the test fixture transforms the real part of the impedance of the DUT to very small values far away from $50\,\Omega$ (characteristic impedance of the network analyzer).

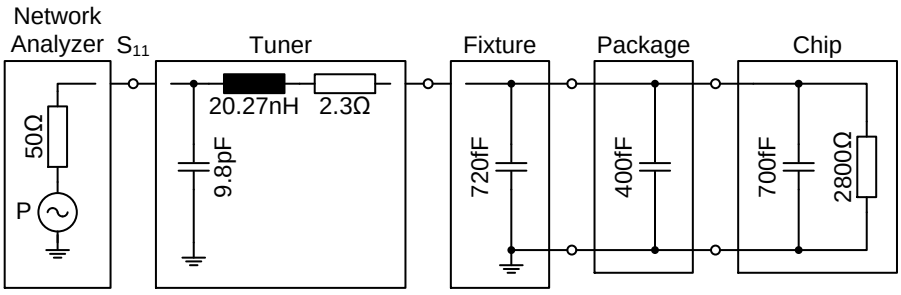


Figure 2.36: Equivalent circuit of a conventional measurement setup

Measurement Error

A typical impedance would be $\underline{Z}_{DUT} = (3 - \jmath 80)\Omega$. Using (2.7.10), the reflection factor results in $S_{11} = 0.967$.

$$\underline{S}_{11} = \frac{\underline{Z} - \underline{Z}_0^*}{\underline{Z} + \underline{Z}_0} \tag{2.7.10}$$

That means nearly 99.9 % of the output power of the network analyzer is reflected back to its port, and therefore the measurement error becomes dramatically high, as will be shown now. The error of the R&S® ZVL network analyzer used is specified as $\tilde{f}_{NA} = 0.4\,\mathrm{dBm}$ for S_{11}.

$$f_{NA} = 10^{\frac{\tilde{f}_{NA}}{20}} - 1 \tag{2.7.11}$$

To calculate the relative error for the power at the DUT depending on S_{11}, the error of the network analyzer has to be converted into a linear unit as shown in (2.7.11), and can then be inserted into (2.7.10):

$$P_{DUT} = \left\{1 - \left[(1 - f_{NA}) \cdot S_{11}\right]^2\right\} \cdot P_{Source} \tag{2.7.12}$$

From (2.7.12) the relative error for the power at the DUT is given by:

$$f_{P_{DUT}} = \frac{(1 - f_{NA})^2 - 1}{1 - \frac{1}{S_{11}^2}} \cdot 100\,\% \tag{2.7.13}$$

For the above discussed example, the measurement error for $f_{NA} = 5\,\%$ is $f = 140\,\%$, which is certainly not acceptable.

2.7.2.3 Measurement Setup Used to Determine the Minimum Input Power at the DUT

To achieve acceptable measurement results a tuner, as proposed in [75], is connected between the network analyzer and the DUT to achieve impedance matching. Like in the conventional setup, the DUT is the IC bonded into a package and soldered onto the SMA test fixture. The handling is simple because the network analyzer, the tuner, and the DUT have SMA connectors. The equivalent circuit of this measurement setup is depicted in Figure 2.36. The tuner has to be set in a way that the reflection coefficient measured by the network analyzer gets minimized. If all devices used were lossless and the tuner set to the correct parameter,

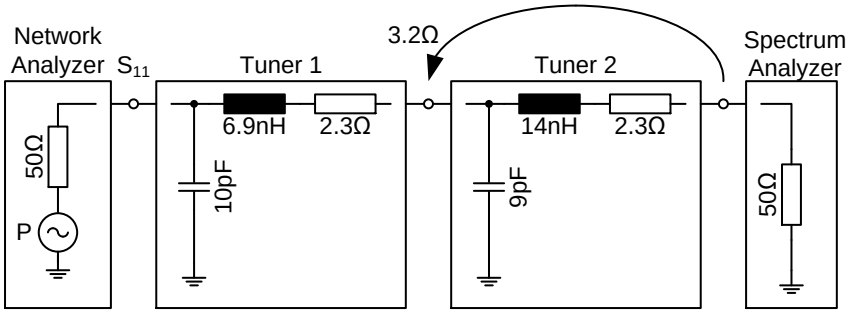


Figure 2.37: Equivalent circuit of the test setup with two tuners

the chip would consume the power generated by the network analyzer. However, in reality all devices used have losses which lower the power available at the chip. To specify the input power of the chip, these losses have to determined.

Reference Plane

As already published in [59], the Open-Short-Load calibration method allows an accurate calibration till the reference plane is reached. In the measurement setup used the reference plane is in front of the tuner. Behind the tuner the impedances vary depending on the tuner parameters, thus the reference plane cannot be moved to the back of the tuner. Consequently, the system behind the reference plane has to be characterized.

Losses Caused by the Tuner

The test fixture and package have already been investigated in Section 2.7.2.1. Even though the fixture and the package can be considered as lossless, the losses of the tuner have to be taken into account because these losses depend on the set tuner parameters. This behavior can be illustrated by connecting two tuners in series, where one port of the first tuner is connected to the network analyzer and one port of the second tuner is connected to a spectrum analyzer. The tuners used, sold by the company Microlab with the identification SF-11F [78], are specified with a maximum loss of 0.2 dB. However, it cannot be said that the losses in the tuner will not exceed the specified 0.2 dB, as this value is only valid in a 50 Ω-system. Therefore the parameters of both tuners are set to obtain impedances far away from 50 Ω each. Despite this, the measured S_{11} at the network analyzer port is zero. Consequently, all power generated by the power source of the network analyzer is fed into the system. According to the conception that each tuner introduces a loss of 0.2 dB, a total loss of 0.4 dB in the system would be expected. Due to the fact that the impedances are nowhere near 50 Ω, the measured losses in the system are 2.54 dB. This measurement result can easily be proved by calculations. Figure 2.37 shows the equivalent circuit of this test setup including the tuner parameter settings. Each tuner can be represented by a parallel capacitor, a series inductor, and a series resistor, which is used to emulate the losses. The value of the series resistor is given by (2.7.14), where IL are the losses of a tuner and Z_0 is the reference impedance with a value of 50 Ω.

$$R_{Loss} = Z_0 \cdot 10^{\frac{\mathrm{IL}}{10}} - Z_0 \tag{2.7.14}$$

Because of the high capacitance of tuner 2, the impedances of the spectrum analyzer and the loss resistor of tuner 2 are transformed into a relatively small value of 3.2 Ω. Consequently the power is shared by the transformed resistor of the spectrum analyzer and the loss resistor in tuner 1. The resulting loss in tuner 1 can be calculated as:

$$\mathrm{IL} = 10\log\left\{\frac{\Re\left\{\underline{Z}_{Transform}\right\} + R_{Loss}}{\Re\left\{\underline{Z}_{Transform}\right\}}\right\} \tag{2.7.15}$$

The losses of tuner 2 have to be added to the calculated losses above. These are simply 0.2 dB because this tuner is operating in a 50 Ω-system. This effect can also be seen in S_{22} differing to zero. Depending on the tuner setup, these losses can either be increased or decreased. Certainly, this problem concerns the measurement setup presented in Figure 2.36 as well. Since only a one-port measurement is possible, S_{22} can not be measured and thus this parameter cannot be used to determine the losses induced by the tuner 1. But these losses can be calculated if the chip impedance is known. Otherwise they can be measured by emulating the chip with a second tuner and an appropriate termination.

Calculation of the Tuner Losses:

As already mentioned, the chip impedance has to be known. It can be attained by simulation or by measuring the unbonded die. Knowing the impedance makes it possible to develop the values of the equivalent circuit of the measurement setup shown in Figure 2.36. This values are valid for $S_{11} = 0$, thus it is important to set S_{11} as close to zero as possible (perfect matching may not be possible because of a limited maximum VSWR at a tuner) to obtain accurate results for this loss estimation method. The capacitances of the package and the fixture transforms the real part of the chip impedance to $R_{Transform} = 3.37\,\Omega$. Using (2.7.15) results in a loss of 2.26 dB.

Using the measurement setup shown in Figure 2.36, the minimum input power of the chip can now be determined by matching the chip as close as possible to the minimum operating point* and subtracting the losses caused by tuner 1 and the cables from the output power of the network analyzer considering the reflection coefficient as shown in (2.7.16).

$$P_{min} = P_{source}\cdot\left(1 - \left|\underline{S}_{11}\right|^2\right) - 10\log\left\{\frac{\Re\left\{\underline{Z}_{Transform}\right\} + R_{Loss}}{\Re\left\{\underline{Z}_{Transform}\right\}}\right\} - P_{Loss_{cables}} \tag{2.7.16}$$

Measurement of the Tuner Losses:

As introduced above, the losses of the measurement setup caused by the tuner can be measured by emulating the chip with a second tuner and an appropriate termination. This procedure starts with matching the chip to its minimum operating point using the same measurement setup shown in Figure 2.36 as for the first method. Then the DUT is removed and a second tuner is connected directly to the first tuner to emulate the chip. Therefore the tuner parameters of the second tuner have to be set so that the impedance of the second tuner is the same

* The minimum operating point is defined as the operating point at which the performance of the chip is optimal.

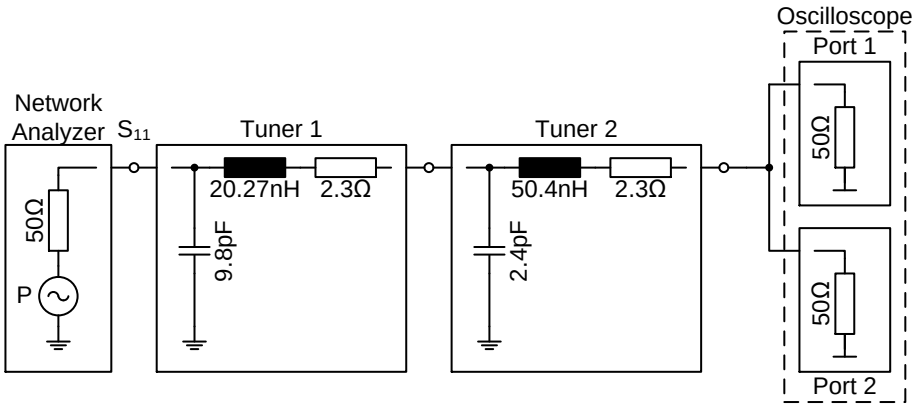


Figure 2.38: Equivalent circuit of the test setup with two tuners

as the one of the DUT. This can be achieved when S_{11} is set to the value which could be measured while the chip was connected. It is very important that the impedances are equal, as the losses are directly connected to these impedances. Unfortunately, because of the limited VSWR and the forbidden regions (see [68]), the same impedance and thus the same S_{11} is not possible with a termination of 50 Ω. If a termination of 25 Ω is used, S_{11} can be roughly set to the desired value. The requested termination resistance of 25 Ω is achieved by using two parallel inputs of an oscilloscope as shown in Figure 2.38. Additionally, the power transferred to the 25 Ω termination can be easily determined using (2.7.17).

$$P_{osc} = 10 \cdot \log \left\{ \frac{V_1^2 + V_2^2}{50} \right\} \tag{2.7.17}$$

V_1 and V_2 are the root mean square values of the voltages at the inputs of the oscilloscope. Knowing the power transferred to the oscilloscope, the losses can also be calculated. As the second tuner is terminated with 25 Ω, the power dissipated is increased from 0.2 dB to 0.3 dB. As shown in (2.7.18), the losses can be calculated by the difference of the output power from the network analyzer and the power transferred to the oscilloscope where the losses of the cables between the oscilloscope and the tuner have to be subtracted.

$$IL = P_{source} \cdot \left(1 - |\underline{S}_{11}|^2\right) - P_{Osc} - P_{Loss_{cables}} \tag{2.7.18}$$

Using (2.7.18) results in a loss of 2.4 dB. The losses are a little bit higher than the losses calculated in Section 2.7.2.3. This is due to the fact that the chip impedance could not be emulated exactly with the second tuner.

The minimum input power of the chip has already been determined. It is the same as the power transferred to the oscilloscope considering the losses of the cables:

$$P_{min} = P_{osc} - P_{Loss_{cables}} \tag{2.7.19}$$

	Simulation	**Calculation**	**Measurement**
P_{source}	−15.5 dBm	−12.8 dBm	−12.8 dBm
P_{losses}	0 dB	2.26 dB	2.4 dB
S_{11}	0	0.143	0.11
P_{min}	−15.5 dBm	−15.15 dBm	−15.2 dBm

Table 2.9: Comparison between the results of the different methods

Comparing the Different Methods:

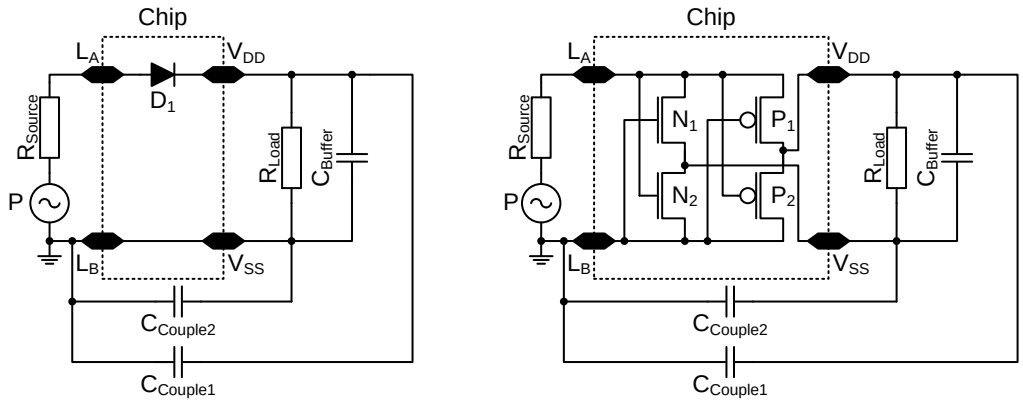
The results of the calculation and measurement of the tuner losses and the achieved values of the minimum input power P_{min} are compared in Table 2.9. Certainly the outcome of the Simulation Program with Integrated Circuit Emphasis (SPICE) simulation is also shown in this table. The small deviations can be referred to small measuring inaccuracies. Anyhow P_{min} determined by the calculation and measurement method is higher than the simulated value. These methods have worst case (pessimistic) behavior, which means that P_{min} cannot be lowered due to measurement errors or inaccuracies. As already stated in Section 2.6, PSUs have nonlinear behavior. For the measurements a linear network analyzer was used, thus the input impedance cannot be correctly determined in the calculation method. Nevertheless the resulting error is acceptable. For the measurement of the tuner losses it is not necessary to determine the chip impedance. Instead it is important to find the operating point at which the performance of the device is optimal. Therefore a source pull measurement is performed to find the optimum source impedance [74]. As a result, the proposed method can be used with a clear conscience for the determination of the minimum input power of PSUs.

2.7.2.4 Measurement of Balanced (Differential) Input Structures

As already discussed in Section 2.7.2.2, a simple measurement method is to connect the packaged chip to a network analyzer. To achieve acceptable measurement results, a tuner, as explained in Section 2.7.2.3, is also needed.

Usually it does not matter if one input pin of the chip is connected to the ground of the network analyzer regardless of whether a balanced or an unbalanced input structure is present. But every chip has parasitic coupling to the global ground. Due to the fact that the ground of the network analyzer is connected again to the global ground, a network analyzer supporting the differential mode or a specific measurement setup are necessary.

As it should be possible to determine the minimum input power of the chip using non-expensive measurement equipment like the R&S ™ ZVL network analyzer, as used for the single-ended measurement, the output signal of the single-ended network analyzer should be converted in a differential signal. The equivalent circuits of a single-ended as well as a differential input structure connected to a network analyzer with the parasitics coupling to the global ground are shown in Figure 2.39.



(a) Single-ended (b) IC

Figure 2.39: Rectifiers with coupling to ground

symbol	description
l	length of the line
r	radius of the line
h	distance to global ground
ϵ_0	vacuum permittivity

Table 2.10: List of symbols for (2.7.20)

Parasitic Coupling

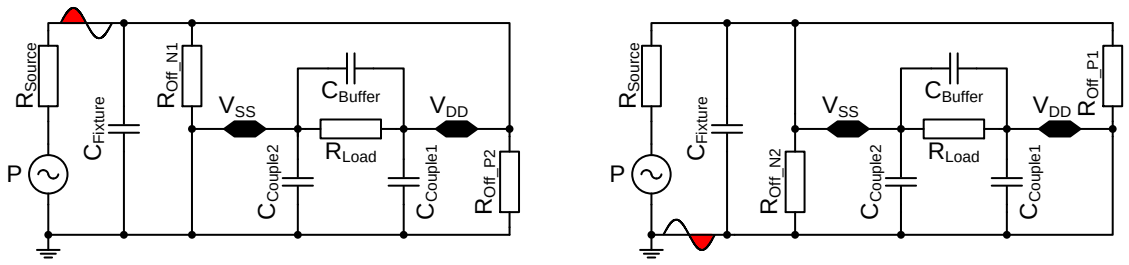
The capacitances C_{Couple_1} and C_{Couple_2} represent the parasitic couplings such as they occur in the chip, in the package and due to the measurement connection for the observation of the supply voltage of the chip. The originated coupling by the measurement connection of V_{DD} and V_{SS} can be estimated as:

$$C_{Couple} = \frac{2 \cdot \pi \cdot \epsilon_0}{\ln \frac{2h}{r}} \cdot l \tag{2.7.20}$$

A description of the symbols in (2.7.20) is given in Table 2.10. For a typical measurement setup C_{Couple} is in the range of a few picofarads. If the chip is packaged, the parasitic coupling can only be influenced by modifying the supply voltage measurement connection.

Single-Ended PSU Connected to a Single-Ended Network Analyzer:

If a single-ended structure ($L_B = V_{SS}$) is connected, the parasitic coupling to the global ground does not have negative effects. Looking at Figure 2.39a, it is obvious that C_{Couple_1}, connected between V_{DD} and ground, works like an additional buffer capacity. In the simplified equivalent network, the parasitic capacitance between V_{SS} and ground seems to be shorted. But in the real measurement setup the IC's V_{SS} is connected via a bond wire which acts



(a) Positive half-wave

(b) Negative half-wave

Figure 2.40: Equivalent circuits of the differential rectifier

like an inductor with ohmic losses. So C_{Couple_2} improves the connection between V_{SS} and ground.

Differential PSU Connected to a Single-Ended Network Analyzer:

The differential structure depicted ($L_B \neq V_{SS}$) in Figure 2.39b achieves the highest performance if the DC output signals are decoupled. If the differential structure is connected to the single-ended network analyzer, this performance is lowered because both output signals, V_{DD} as well as V_{SS}, are coupled to the global ground by parasitic capacitances. The DUT is influenced negatively in two major ways. On the one hand there is, as explained above, the parasitic coupling and on the other hand there is the unsymmetrical driving of the input. C_{Couple_2} connects the input pin L_B with V_{SS}. In contrast to the single-ended structure, L_B is not at a fixed potential. There is still a small swing compared to L_A. Nevertheless, the differential rectifier is not driven in the appropriate way. This fact can be explained for each half-wave of the input signal by dumping down the differential structure to an equivalent circuit as depicted in Figure 2.40.

For the following consideration L_B is directly connected to the ground. During the positive half-wave of the input L_A, V_{SS} is connected to the ground as shown in Figure 2.40a. During the negative half-wave, V_{DD} is connected to the ground as can be seen in Figure 2.40b. This fact causes a big potential difference in the parasitic coupling capacitances between the positive and the negative half-wave. The parasitic capacitances have to be reloaded twice a period, which induces losses depending on the value of the parasitic capacitances and the transconductance of the transistors. Thus it seems, that the performance of a differential PSU compared to a single-ended PSU is enormously lower. In reality, such a measurement setup delivers false results. To get rid of this problem, the parasitic coupling should be kept as small as possible. Furthermore, it is mandatory that the input L_B oscillates. If the phase between the signals at $L_A$and L_B is 180° and if the amplitude of L_A and L_B is the same, C_{Couple_1} and C_{Couple_2} are loaded to the same level at each half-wave. Thus, the equalizing current between each half-wave is substantially reduced and in that case the lowest influence of the parasitic coupling can be achieved. That means for the measurement of differential PSUs a differential input signal is mandatory. How this can be accomplished will be explained in the following section.

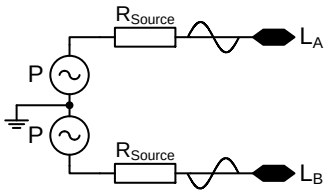
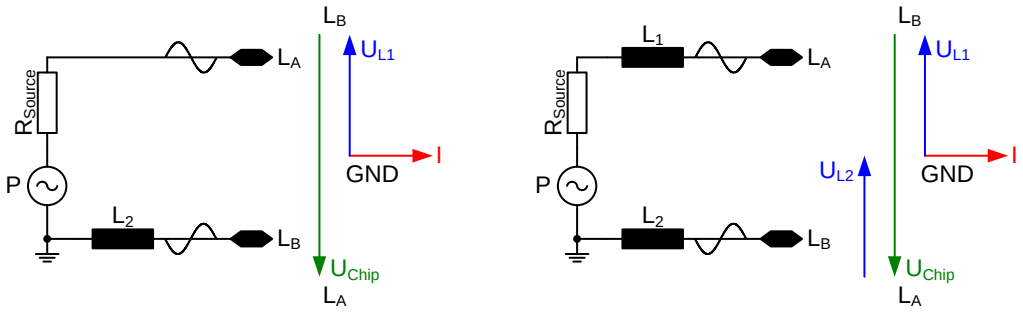


Figure 2.41: Principle of a true differential network analyzer



(a) One inductor version

(b) Two inductors version

Figure 2.42: Generation of the pseudo-differential signal

2.7.2.5 Generation of the Differential Input Signal

A true differential network analyzer feeds the DUT with differential input signals at L_A and L_B simultaneously as shown in Figure 2.41. Since differential network analyzers are expensive, the single-ended output signal of the non-expensive single-ended network analyzer used has to be converted in a differential signal. This so-called pseudo-differential signal can be generated in two ways as depicted in Figure 2.42.

Differential Input Signal Using One Inductor

An inductor is joined up between ground of the network analyzer and L_B. To reach a phase difference of 180° between L_A and L_B, the value of the inductor must be in the range of (2.7.21).

$$0 < L_2 \leq \frac{1}{(2\pi f)^2 \cdot C_{DUT}} \tag{2.7.21}$$

To achieve the same amplitude at L_A and L_B as depicted in Figure 2.42a, the inductance can be calculated to be:

$$L_2 = \frac{1}{2} \cdot \frac{1}{(2\pi f)^2 \cdot C_{DUT}} \tag{2.7.22}$$

C_{DUT} is calculated using (2.7.23).

$$C_{DUT} = C_{Fixture} + C_{Package} + C_{Chip} \tag{2.7.23}$$

Differential Input Signal Using Two Inductors

Here, the previously described circuit is extended by a second inductor $L_1 = L_2$ between L_A and the network analyzer as depicted in Figure 2.42b. Hence the circuit is in resonance, which causes a smaller S_{11} and lowers the measurement error. The vector diagrams in Figure 2.42 help to explain that the signals at L_A and L_B are differential. Arising from the network analyzer's ground, the voltage drop over L_2 is in opposite phase to the voltage drop over C_{DUT}. Due to the fact that the impedance value of L_2 is half of the impedance value of C_{DUT}, it is trivial that the voltage drop over L_2 is also halved. If the second inductor L_1 is used too, the voltage drop over L_1 is in phase and also as big as the voltage drop over L_2. To reach completeness, the voltages of the circuits in Figure 2.42 have to be multiplied with the different quality factors. This means that a differential structure can be measured either with a differential network analyzer or with a single-ended network analyzer and the depicted circuit in Figure 2.42. However, in both cases the parasitic coupling to the global ground should be kept as small as possible. Besides saving costs, a significant advantage of the pseudo-differential signal is that the same test fixture as with single-ended structures can be used. The measurement setup is like that described in Section 2.7.2.3 without the tuner. Instead two SMD inductors with high quality factor (copper-plated ceramic core) are soldered on the input pins of the package. This induces additional losses depending on the quality factor of the inductors. Indeed, these losses cannot be measured with inexpensive measurement devices and thus they can roughly be estimated in the range of the losses of the measurement setup of single-ended structures described in Section 2.7.2.3.

Certainly an additional tuner between the inductors and the DUT can be used to achieve full matching. This is not necessary because S_{11} is due to inductors small enough to achieve accurate measurement results. Using a tuner here leads to some drawbacks: The input signals of the chip will not have the same amplitude values and the tuner losses have to be determined. Therefore it is advisable to determine the minimum input power and fulfill measurements on differential input structures without a tuner.

2.8 Conclusion

Different types of PSUs used for electro-magnetic energy harvesting were presented in this chapter. As the PSU is a key block in every remotely powered device, detailed investigations and analysis have been performed. Basically PSUs can be divided into two different groups by means of their input structure. On the one hand there are balanced PSUs which perform a full-wave rectification as shown in Section 2.2. On the other hand, Section 2.3 shows unbalanced PSUs which have one input pin connected to the chip's substrate and perform a half-wave rectification.

The goal of the PSU design is to minimize its input sensitivity for a given output load, which means in other words to maximize the PCE. The PCE depends again on various factors which are unfortunately interdependent. To achieve this goal it was necessary to consider not only the PSU itself, but also the whole system including the antenna and its matching. It has been shown how and why the loaded Q Factor, the voltage drop from the input to the output, and

the power dissipation of the rectifying components influence the PCE. The lower the forward voltage drop of the rectifying components, the higher the PCE. Thus several methods to lower these forward voltage drops are analyzed with the caution that these methods also require power. So, depending on the desired application whether and which method should be used has to be decided based on calculations presented in Section 2.4.

Voltage multiplier structures are necessary to deal with low input voltages. These voltage multipliers operate like charge pumps that are clocked by the input signal. Based on the comparison of a one-stage with a two-stage voltage multiplier, it is shown that the power consumption caused by charging the capacitors increases with the number of stages because the lower the input amplitude the higher the potential the charge has to be transferred to. Nevertheless, the amount of charge that is transferred is still equal.

Detailed AC, DC, power, and power dissipation analyses based on an n-stage voltage multiplier built with MOSFET transistors operating as diodes have been performed in Section 2.5, where the major parasitic effects were taken into account. It has been shown how the current and size of the transistor influence the forward voltage drop and thus the output voltage. Many equations have been derived to calculate, among others, the forward voltage drop, the transistor current, and consequently the output voltage and output power of the voltage multiplier. The average power dissipated by the transistors has been calculated considering the switching behavior and the ohmic losses of the substrate and the n-well. All this resulted in the final equation for the PCE including the major parasitic effects.

Simulation techniques for circuits with large signal behavior, an appropriate testbench considering the matching conditions, and important equations to calculate some key parameters like the field strength in simulation or the input voltage of the chip as a factor of the measured field strength have been presented in Section 2.6.

Measurement setups to evaluate the minimum electrical field strength at HF as well as the input sensitivity at UHF have been presented in Section 2.7. A novel and accurate measurement method has shown that it is possible to determine the losses of the measurement setup at UHF in two different ways. Knowing these losses, the input sensitivity can be calculated. Furthermore, methods to generate a differential input signal for the measurement of differential input structures (see Section 2.2) by using a single-ended network analyzer have been presented. Thus, the same inexpensive network analyzer can be used for single-ended and differential input structures.

Chapter 3

The Electro-Magnetic Energy Harvester

The original publications related to this chapter are [95, 96] (own publications). ■

In this chapter the problem of the constant lack of energy in remotely powered devices is first explained. Then it comes to the point, how to develop devices powered by the electro-magnetic field at Radio Frequency Identification (RFID) frequencies that can drive e.g. pressure sensors or active transmitters with a power consumption in the milliwatt range. A key issue is the design of the power critical blocks and their simulation methods. Relying on the detection of voltage levels, many problems come up in a design with varying supply voltage. The design gets even more difficult if the power consumption of the harvester frontend itself should be in the nanowatt range. All these design issues are explained in detail with a solution for each of these challenges.

3.1 The Lack of Energy

The input power P_{in} is the power needed to operate the Integrated Circuit (IC). The better the matching between the receiving antenna and the IC, and the higher the gain either of the transmitting or the receiving antenna, the more power is delivered to the IC. The relationship between the power received by the IC's receiving antenna and P_{in} is described by (3.1.1), where P_r is the available power at the receiving antenna and $\underline{\Gamma}$ is the reflection coefficient.

$$P_{in} = P_r \cdot \left(1 - |\underline{\Gamma}|^2\right) \tag{3.1.1}$$

Furthermore, as explained in Section 2.4.2 the lower the necessary input power of the IC the higher the operating range, as can be seen from (2.4.9) on page 23.

Additionally, the higher the antenna gain the bigger the operating range. If the system is designed to achieve the maximum operating range the source usually emits the maximum power allowed by national regulations. Therefore only the gain of the receiving antenna can be increased without breaching regulations. Due to the fact that the whole energy harvester, which is the receiving antenna connected to the IC, should be a low-cost product the performance is limited in production by the following two factors:

- It is not reasonable and especially not cost effective to develop a receiving antenna with high gain.
- The matching between the receiving antenna and the IC is mostly not ideal due to the connection process of the antenna to the IC and the variation of the antenna's impedance during production.

The proposed Electro-Magnetic Energy Harvester (EMH) is used to work not exactly at one dedicated operating frequency which implies that the harvester antenna should be more or less (dependent on the application) broadband. Such an antenna has a low Quality Factor (Q Factor) by means of the broadband design as well as due to low Q Factors of the default used materials, which enables better matching between the receiving antenna, in this case called the harvester antenna, and the IC or the EMH.

So the only way to increase the operating range and the applicability of the EMH is to lower the input power of the IC. This can be done by maximizing the Power Conversion Efficiency (PCE), which means that the losses as well as the power consumption of the so-called control circuitry have to be minimized. From (2.4.9) it is also obvious that the power consumed by the load limits the operating range.

From the Friis transmission equation ((2.4.9) on page 23) the following assumption can be made:
For transmitted power in the order of 4 W Effective Isotropically Radiated Power (EIRP), which is the maximum power allowed by national regulations, and a frequency of 900 MHz, an output power in the range from 2.8 mW to 11 µW can be received in an operating range from 1 m to 16 m, if the gain of the receiving antenna is neglected. Looking at these numbers it becomes clearly evident that remotely powered devices are limited in complexity and working range due to the constant lack of energy.

Taking the efficiency of the RF to DC conversion circuit into account, the power which can be converted from the electro-magnetic field at UHF using common RFID technology is not sufficient to operate pressure sensors or active transmitters with a power consumption in the milliwatt range. To overcome this problem, an ultra low power energy harvesting system has been developed.

3.2 The Principle of the Electro-Magnetic Energy Harvester

The basic function of the EMH is to harvest energy from the electro-magnetic RF field and to store it in a buffer capacitor. The energy stored in the buffer capacitor is then used to power the system. Therefore, in addition to the Power Scavenging Unit (PSU), at least one Level Detection Unit (LDU) and an output switch are necessary to connect and disconnect the device powered by the EMH as shown in Figure 3.1. The LDU senses the output voltage of the PSU and controls the output switch that is used to feed the power to the device connected to the EMH.

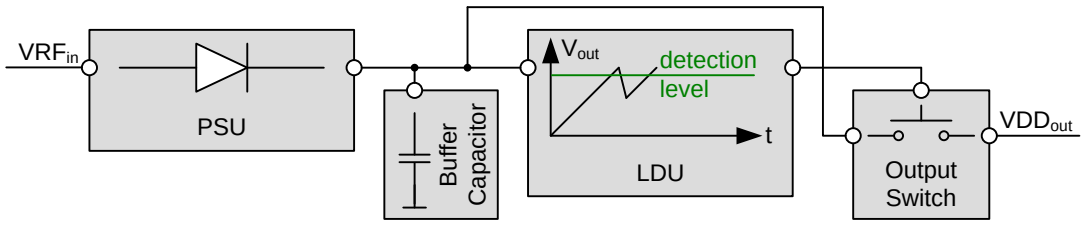


Figure 3.1: Principle of the electro-magnetic energy harvester

Using such a principle cuts the direct connection between the load and the output of the PSU. Thus the load does not continuously draw current from the PSU, which lowers the average DC power consumption of the PSU and thus decreases the necessary input power P_{in}. So it becomes possible to provide a time limited DC output power which is a multiple of the IC's average RF input power.

3.3 System Description

In this section the system architecture, including the required design specifications, the system characteristics and the dimensioning are explained. Since the basic principle is introduced in Section 3.2, the function of the building blocks is explained in this section. Furthermore, a timing diagram is presented to show the system behavior in different operating modes.

3.3.1 Design Specifications

- The proposed Wireless Sensor Node (WSN) is designed for maximum input sensitivity. An input sensitivity of at least $-13\,\mathrm{dBm}$ is necessary to achieve a suitable operating range and to be competitive with state-of-the-art RFID sensing tags as published in [116] and [118].
- The analog frontend is capable of frequencies from 100 MHz up to 2.45 GHz to achieve an operating range of at least five meters.
- The energy harvester is able to power an on-chip temperature sensor and an active transmitter as used in the iTire chip. Therefore an output power of the energy harvester of approximately 10 mW for approximately 400 µs has to be guaranteed.
- The output of the energy harvester is enabled at 3 V and disabled at 1 V.
- The external sensing voltage has to be in the range (a) 0 to 600 mV or (b) 300 to 900 mV. These two input voltage ranges of the Analog to Digital Converter (ADC) can be selected via a control signal.

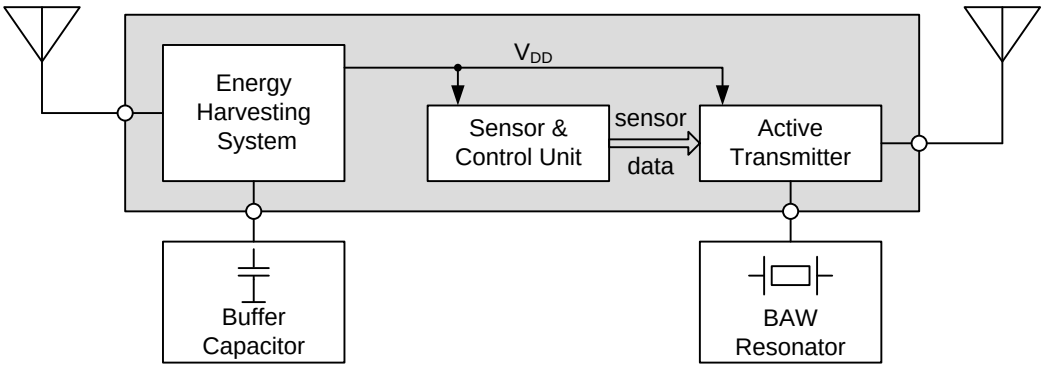


Figure 3.2: Block diagram of the wireless sensor node

3.3.2 System Architecture

To test some blocks of the iTire chip as explained in Section 1.4 in a useful configuration, the on-chip sensor block, including the control unit and the active Bulk Acoustic Wave (BAW)-based transmitter are connected to the EMH. That means the sensor block and the transmitter are powered by the EMH. Thus, this built-up system is operating like a stand-alone remotely powered WSN.

Figure 3.2 shows the block diagram of the proposed WSN. The receiving antenna is matched to the input of the energy harvesting system that provides the energy needed by the sensor and the active transmitter. The harvested energy is stored in an energy reservoir. If the voltage level of this energy reservoir reaches 3 V the sensor and a control unit are powered. The sensor data is converted into digital values and then the active transmitter is started to transmit the data. The RF to DC converter is decoupled from the power amplifier of the active transmitter by using a separate transmitting antenna.

Figure 3.3 shows the block diagram of the proposed EMH used to supply the WSN. It consists of:

- The PSU,
- Two off-chip buffer capacitors,
- Two LDUs,
- A Voltage Controlled Oscillator (VCO),
- A DC/DC charge pump, and
- An optional Low-Dropout (LDO) regulator.

To be able to collect the energy from a multitude of sources the input frequency range of the harvesting unit should be as wide as reasonably practicable. Therefore the PSU is designed to be capable of input frequencies from 100 MHz up to 2.45 GHz. It rectifies the incoming RF signal from and provides a DC voltage $V_{DD_{RF}}$ on the buffer capacitor C_{Buffer_1}.

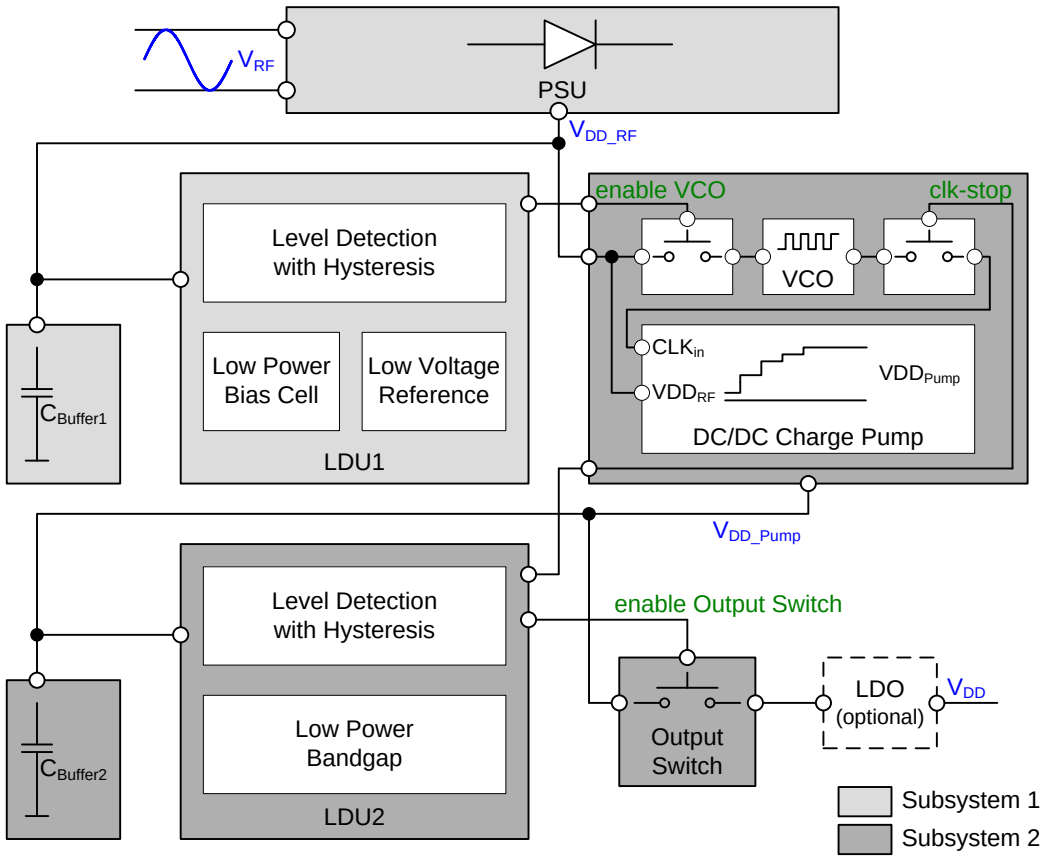


Figure 3.3: Detailed block diagram of the energy harvesting system

The LDU1 includes a bias cell, low voltage references, and voltage level detectors. Since the LDU1 is supplied by the PSU, its current consumption needs to be minimized because it is directly related to the input sensitivity. The lower the current consumption of the LDU1 the lower the load of the PSU in idle mode (see Section 3.3.3), and thus the lower is the input power necessary to operate. As stated in (2.4.9), the lower the required input power the higher the operating range.
The LDU1 enables the VCO and thus the DC/DC charge pump between two defined voltage levels. 1.1 V for the on-level and 0.7 V for the off-level are chosen to reach reasonable values in terms of input power and number of stages of the DC/DC charge pump. $V_{DD_{RF}}$ is the power supply of the LDU1, the VCO, and the DC/DC charge pump. To reach high operating ranges and to enable the charging of C_{Buffer_1} at low output currents of the PSU, the VCO is power gated by the LDU1. This VCO provides the clock for the DC/DC charge pump.

The DC/DC charge pump generates an output voltage $V_{DD_{Pump}}$ which is higher than $V_{DD_{RF}}$. If the VCO is switched off, the DC/DC charge pump stops its operation. The second buffer capacitor C_{Buffer_2} stores the energy required for the circuit supplied by this energy harvesting system.

The LDU2 enables the output depending on the voltage level of $V_{DD_{Pump}}$. If the output voltage has to be constant, an optional LDO regulator provides the desired output voltage as long as the voltage level at C_{Buffer_2} is high enough.

As can be seen in Figure 3.3, the energy harvesting system can be divided into two subsystems. These two subsystems operate asynchronously to increase the input sensitivity. The first subsystem is built by:

- The PSU,
- C_{Buffer_1}, and
- The LDU1.

The second subsystem is formed by:

- The VCO,
- The DC/DC charge pump,
- C_{Buffer_2},
- The LDU2, and
- The output switch.

This principle makes it possible to power gate the VCO and the DC/DC charge pump. If the VCO and the DC/DC charge pump are switched off, the PSU is loaded only with the LDU1. The power consumption in this state is approximately 20 times lower than if the VCO and the DC/DC charge pump were permanently powered by the PSU. To make this principle operable two buffer capacitors are needed. C_{Buffer_1} is charged by the PSU and stores a certain amount of energy. A part of this energy (E_1) is then used to power a VCO and a DC/DC charge pump which charges C_{Buffer_2}. Due to the losses, produced by the VCO and the DC/DC charge pump, a part of E_1 is transferred to C_{Buffer_2} and stored there as energy E_2. So the energy E_2 in the energy reservoir C_{Buffer_2} increases. If E_2 is high enough the sensor and the active transmitter are powered.

3.3.3 System Characteristics

To simplify the following considerations and explanations, some characteristics are defined in this section.

Input Sensitivity – Minimum Input Power

As stated in Section 2.1.1 the input sensitivity or minimum input power identifies the point at which the RF input power is sufficient to operate the chip. In this work the input sensitivity of the EMH refers to the point where the output voltage of the PSU reaches 1.1 V in idle mode (see next characteristic).

Idle Mode

Idle mode is the state in which the VCO and thus the DC/DC charge pump do not operate.

Idle Mode Current Consumption

Idle mode current consumption is the current consumption of the energy harvesting system in idle mode. The PSU is loaded only with the current consumption of the LDU1. The leakage of C_{Buffer_1} is also considered.

Continuous Mode

In continuous mode the RF input power is high enough that the VCO operates. Depending on the output voltage $V_{DD_{Pump}}$, the DC/DC charge pump either runs or does not. (If $V_{DD_{RF}}$ is equal to or greater than 3.3 V a clock-stop signal stops the DC/DC charge pump.) Once the output voltage of the PSU reaches 1.1 V, the LDU1 turns on the VCO, and then the VCO is never turned off as long as the output voltage of the PSU stays higher than 0.7 V.

Discontinuous Mode

In discontinuous mode the RF input power is not sufficient to operate the VCO continuously. That means once the output voltage of the PSU reaches 1.1 V, it decreases again down to 0.7 V because the current drawn from $V_{DD_{RF}}$ is higher than the output current of the PSU.

3.3.4 Timing

A timing diagram of the essential signals is shown in Figure 3.4 to explain the operating principle with the two operating modes, which are the discontinuous and the continuous mode, respectively.

The lower the RF input power the lower the output voltage of the PSU $V_{DD_{RF}}$. $V_{DD_{RF}}$ depends on the RF input power, on the RF input voltage V_{RF} and on the value and the charge of C_{Buffer_1}.
At startup all voltages are zero. The higher V_{RF} the faster the rise of $V_{DD_{RF}}$ and the faster the VCO and the DC/DC charge pump will be enabled. At $V_{RF_{in}} = 1.1\,\text{V}$ the VCO is powered and the DC/DC charge pump starts to operate and pumps $V_{DD_{Pump}}$ to a higher potential.

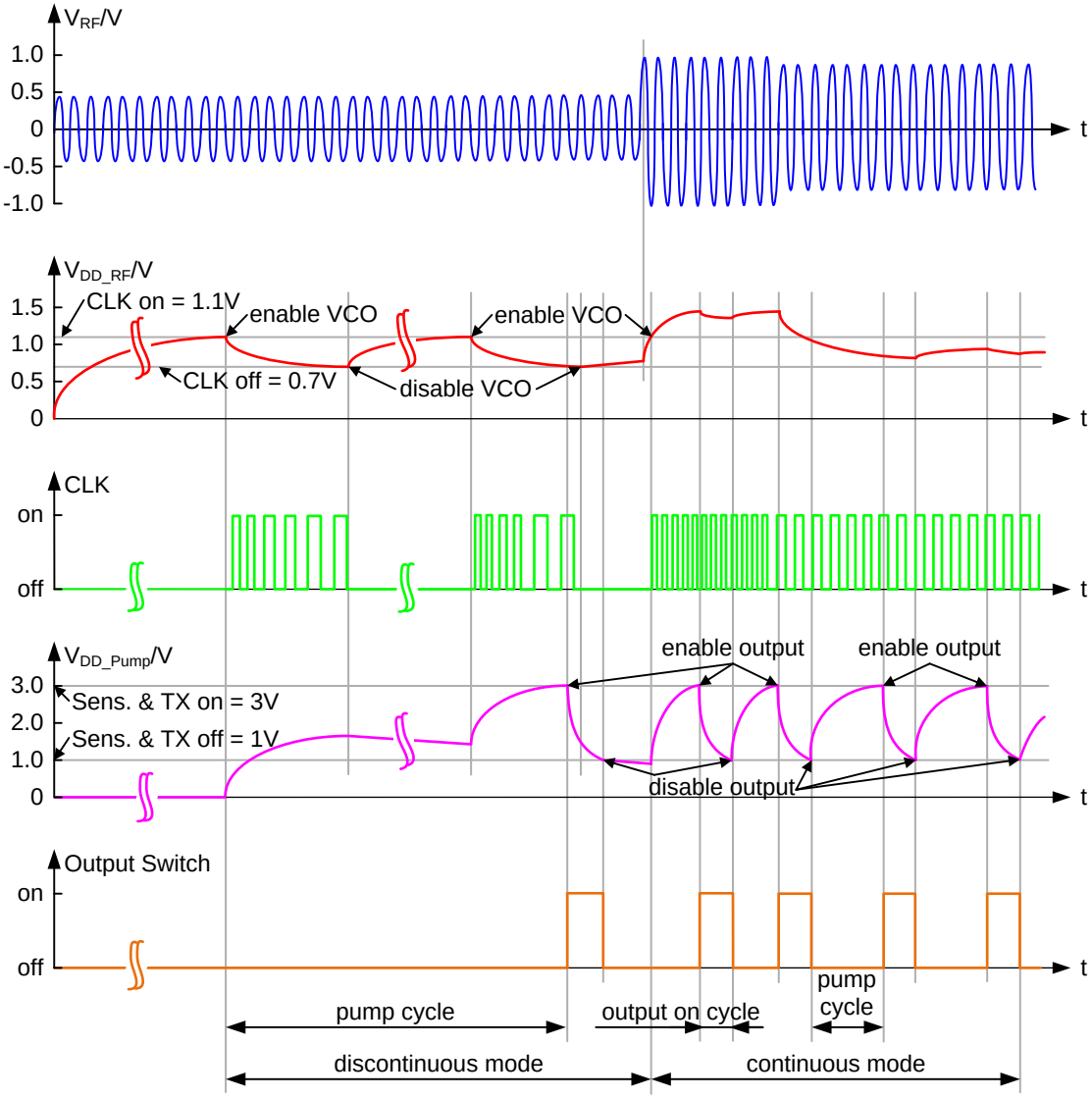


Figure 3.4: Timing diagram of the energy harvesting system

At low input power $V_{DD_{RF}}$ decreases again down to 0.7 V. Then the VCO is power gated again and the DC/DC charge pump stops working. The same procedure occurs repeatedly. After a couple of cycles, $V_{DD_{Pump}}$ reaches 3 V. So the power switch is closed to power the sensor and the active transmitter. Current is drawn out of C_{Buffer_2}. Consequently $V_{DD_{Pump}}$ decreases to 1 V if the average current drawn by the connected device is higher than the average current provided by the DC/DC charge pump. Then the whole process starts again.

At high input power $V_{DD_{RF}}$ remains higher than 0.7 V once 1.1 V are reached, so the VCO runs in continuous mode. Depending on the current consumption of the device connected to the energy harvester, $V_{DD_{Pump}}$ alternates between the on-level (3 V) and off-level (1 V) of

the harvester, or the power switch is always closed. If $V_{DD_{Pump}}$ reaches 3.3 V the clock-stop signal stops the DC/DC charge pump to the protect the circuitry from device destructive voltages.

3.3.5 Dimensioning

The values of the buffer capacitors depend on the desired application. The capacity of C_{Buffer_2} can be calculated by the amount of power and the duration of operation of the system powered by the energy harvester. Knowing the capacity of C_{Buffer_2}, the capacity of C_{Buffer_1} can be calculated considering the requested operation mode and expected RF input power. The smaller the size of C_{Buffer_1} the more pump cycles (see Figure 3.4) are necessary to pump C_{Buffer_2} up to the level, at which the output is enabled. During the switching phase a level detector consumes more power than in idle mode. Thus, the smaller C_{Buffer_1} the more frequently the level detectors switch and the worse the overall efficiency of the harvesting system.

Due to the fact that C_{Buffer_2} is loaded by the LDU2, the PSU must provide the power that is needed by the LDU2 considering the efficiency of the DC/DC charge pump. Furthermore, the power consumption caused by the leakage of the buffer capacitors has to be covered. Current is only delivered from the output of the PSU (node labeled $V_{DD_{RF}}$) to the output of the DC/DC charge pump (node labeled $V_{DD_{Pump}}$) if the DC/DC charge pump is enabled. Therefore buffer capacitors with very low leakage (in the nanoampere range) are very important. The two buffer capacitors can be internal or external depending on the amount of energy that is needed by the connected device for one operation cycle.

Instead of the PSU a thin film battery or other harvesters like thermo-electric, mechanic or solar energy harvesters can be connected to C_{Buffer_1} to provide time- limited high output power. Due to these various possibilities the harvester can be utilized in different applications.

In the iTire chip C_{Buffer_2} is charged to supply a temperature sensor, a pressure sensor, and an active transmitter. If the transmission of the data is finished a signal opens the output switch and C_{Buffer_2} is then pumped up to 3 V again to start the next sensing and transmission cycle.

The average current consumption of the internal temperature sensor is approximately 2.7 µA. The measurement process takes around 350 µs. The active transmitter has a supply voltage of 1.5 V and an average current consumption of approximately 7 mA for approximately 400 µs. The capacity of C_{Buffer_2} can be calculated using (3.3.1).

$$C = \frac{i(t)}{\frac{dv(t)}{dt}} \tag{3.3.1}$$

For the proposed application C_{Buffer_2} has to be 2 µF and the size of C_{Buffer_1} is determined by simulation and measurement to be 20 µF to charge C_{Buffer_2} to 3 V in one pump cycle (see Figure 3.4). In one pump cycle means that the energy stored in C_{Buffer_1} must be sufficient to

charge C_{Buffer_2} to 3 V once the output voltage of the PSU reaches 1.1 V (at 1.1 V the DC/DC charge pump starts to operate).

An output load must always be connected to the energy harvester in order to avoid overvoltages at the output of the PSU because the PSU is built with transistors with lower electrical strength. This makes it possible to omit the shunt because at high RF input power the voltage controlled oscillator is running fast and draws a lot of current. Also the losses in the DC/DC charge pump caused by fast switching (parasitic capacitances have to be recharged) increase. C_{Buffer_2} is charged faster and thus the sense and transmit operation is performed more frequently. This principle works like a shunt circuit. If it cannot be guaranteed that a load is always connected to the energy harvester, a shunt circuit has to be implemented. A shunt transistor between the input pins as commonly used in RFID tags or a DC shunt are possible solutions.

3.4 Design of the Analog Components

This section presents the design of the most important analog building blocks of the developed WSN that are the focus of this thesis. Circuit schematics are depicted to discuss the most important findings in the chip design. The main challenge in the design phase is the permanent lack of energy that leads to ultra low power design, which again causes several serious problems. To achieve a low current consumption the bias and cross currents have to be lowered to a few nanoampere which makes circuits slow. Moreover, these small currents imply very high ohmic nodes, which are sensitive to cross-talk. Compared to conventional analog circuits, parasitic capacitances have a larger influence in this kind of design. Another important fact is that devices like transistors and especially resistors enlarge if the circuit is operating with currents in the nanoampere range. As active chip area is reflected in chip costs, it is not feasible to integrate high ohmic (upper megaohm range) resistors. Therefore new concepts are applied to avoid exceeding chip size limits in ultra low power design. Nevertheless the tradeoff between current consumption and robustness still has to be found separately for each block.

3.4.1 RF to DC Conversion

The PSU is a key block in every remotely powered device. It generates the power supply for the whole chip. The WSN extracts the power needed for operation from the electromagnetic field. Frequencies from approximately 100 MHz up to 2.45 GHz are possible, nevertheless the AC/DC converter is optimized for 860 MHz to 965 MHz, which is the frequency range used in UHF RFID systems.

Since full chip operation starting from just a few hundred millivolts at the input pins of the PSU is needed, a voltage multiplier as explained in Section 2.3 is developed. As presented in [53], the Greinacher principle (see [36]) can be used to build a voltage multiplier to supply a UHF RFID transponder. The principle of this state-of-the-art voltage multiplier has already been shown in Figure 2.6 (Section 2.3, page 17). The proposed voltage multiplier is shown

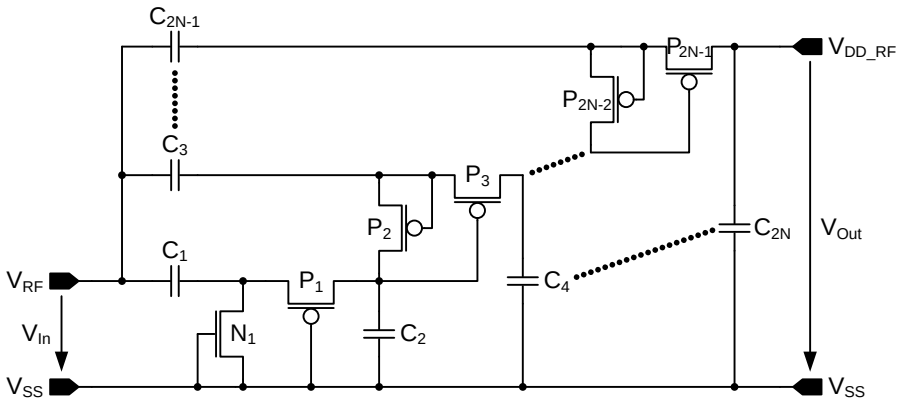


Figure 3.5: Modified single-ended n-stage voltage multiplier

in Figure 3.5. This single-ended voltage multiplier based on Greinacher topology is modified to lower the forward voltage drop of the used transistors. The number of used stages and an explanation for it is given in Section 3.4.1.1.

Using a single-ended frontend, V_{SS} is directly connected to one input pin of the chip. This means that the chip substrate is forced by this input pin. As explained in Section 2.3, the vertical diode-connected transistor N_1 and the coupling capacitor C_1 are used to pump the voltage to a higher potential. The horizontal diode-connected transistor P_1 rectifies the input voltage added by the voltage of the coupling capacitor C_1. The next stages work according to the same principle. Due to the fact that the current only flows during the positive half-wave of the input signal in the buffer capacitor C_{Buffer1}, the designed circuit works as a half-wave rectifier. It is also obvious that this input structure is unsymmetrical.

As shown in Section 2.4.5, the output voltage of the proposed voltage multiplier, neglecting the influence of the parasitic capacitances, can be calculated as:

$$V_{\text{Out}} = 2 \cdot n \cdot \widehat{V_{\text{In}}} - n \cdot \left(V_{D_{horizontal}} + V_{D_{vertical}}\right), \tag{3.4.1}$$

where n is the number of stages, $\widehat{V_{\text{In}}}$ is the input peak voltage and V_D is the forward voltage drop of the particular diode-connected transistor. Looking at (3.4.1) it is obvious that the lower V_D, the higher the output voltage is and the less stages are needed to obtain a distinct output voltage.

Designers modify rectifiers with various techniques to lower the forward voltage drop of the diodes in the rectifiers or voltage multipliers. Most of those circuits have drawbacks, like additional external components or additional current consumption. For PSUs with a low output load this additional current consumption is a significant limitation of the PCE. The PSU has a distinct power dissipation caused by the high frequent switching and by additional circuitry (for instance biasing). The lower the output load the more the PCE depends on this power dissipation.

Different methods to lower the forward voltage drop, with their advantages and disadvantages, are presented in detail in Section 2.4.4. Hence only a brief summary is given here.

In [56, 57] the gates of the vertical NMOS and the horizontal PMOS transistors are connected to V_{DD} and V_{SS} respectively. This increases the output voltage and the PCE at low input voltages. At higher input voltages this scheme has a negative effect because the gate potentials of the diode-connected transistors are not directly related to the input signal. In [32] a micro battery driven switched capacitor technique is used to lower V_D but in the technology used micro batteries are not available. Another method to lower V_D is the use of additional diode-connected transistors as threshold voltage references that provide a bias voltage in the range of the threshold voltage of the diode-connected transistors used [79, 81, 82, 107, 108]. But this method needs some kind of biasing and becomes efficient if the load current is higher than the current used for biasing. Furthermore, the bias cell needs a distinct supply voltage to start its operation and a three-stage voltage multiplier needs one additional diode-connected transistor and approximately 50 nA bias current for each of its six rectification devices. This method also occupies additional chip area and is thus a lot of overhead for a marginal improvement in the desired application.
Hence the voltage multiplier of the EMH is designed with a modification of the diode-connected transistors compared to state-of-the-art voltage multipliers as presented in [49, 53, 71, 115, 117] where Schottky diodes or diode-connected NMOS transistors are used. A PMOS transistor with the gate connected to V_{SS} is used as a horizontal diode of the first stage. The horizontal diodes of the following stages are PMOS transistors whose gates are connected to the respective output voltage of the previous stage. A diode-connected NMOS transistor as vertical diode for the first stage and diode-connected PMOS transistors for the further stages lower the necessary minimum input voltage, which also decreases the necessary minimum input power. No additional devices are needed, which keeps the parasitics small.

The threshold voltages of the MOS transistors have a big influence on the minimum input power for a given output characteristic. Schottky diodes providing low forward voltage drops are often used in rectifiers for RFID tags [49, 53]. Also, floating gate transistors are used to reduce the threshold voltage loss of the MOS transistor [72].

Due to the fact that the PSU is developed in a low-cost CMOS technology (without Schottky diodes, floating gate transistors and zero V_t devices), the design depends on the input voltage where the PSU delivers sufficient output voltage for the energy harvester to start its operation. This voltage is approximately 380 mV and depends on the parasitics of the circuit, the threshold voltages and forward voltage drops of the used transistors. Therefore the necessary input power to operate the energy harvester is higher compared to Schottky diodes used as rectification devices [53], because Schottky diodes have much lower forward voltage drops. Nevertheless the minimum input power is -19.7 dBm, which is very low for the PSU.

3.4.1.1 Simulation of the PSU

The important tradeoff between the transistor's size and its parasitic capacitance is explained in Section 2.4.3. From (3.4.1) it is obvious that the input voltage, and thus the input power, has to be increased if the voltage drops of the rectification devices increase. These voltage drops again depend on the transistor's size. Hence the goal of the design is to minimize the required input power for a given output characteristic.

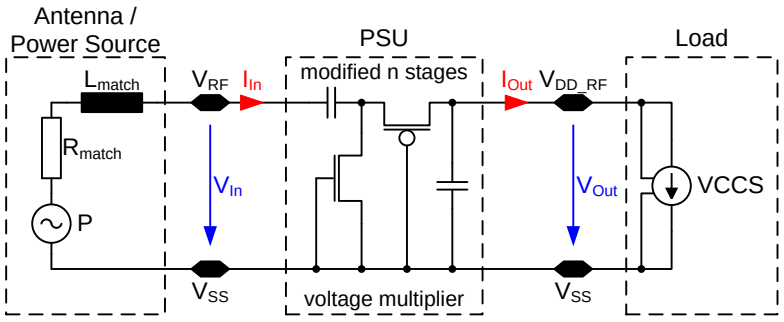


Figure 3.6: Test bench of the PSU

To determine the optimal number of stages and the transistor geometries, the test bench shown in Figure 3.6 is used. The test bench is based on the considerations from Section 2.6.2. The power source provides the power for the PSU. The resistor and the inductor are used to ensure matching between the power source and the PSU. As explained in Section 2.6, large signal excitation has to be considered for the analysis of the PSU. An important fact is that the input impedance of the PSU varies with the input power and the load. Thus sufficient matching with acceptable effort is only possible for one input impedance and thus for one operating point. To maximize the operating range and thus the input sensitivity, the matching is done at the minimum input power sufficient to operate the PSU. The same principle is also used in the antenna design. Thus the impedances between the source and the EMH are mismatched most of the time. The necessary source power can be calculated using (3.4.2), where $\underline{\Gamma}$ is the reflection coefficient between the source and the EMH and P_{in} is the required input power to ensure the desired operation.

$$P_{source} = \frac{P_{in}}{1 - |\underline{\Gamma}|^2} \tag{3.4.2}$$

In this case $\underline{\Gamma} = S_{11}$. That means in the unmatched case the source power has to be increased depending on $\underline{\Gamma}$.

The simulation procedure can be explained as following, where the used identifiers are declared in Section 3.3.3): As explained in Section 2.6.2, the AC analysis is used to approximate the inductance used for imaginary matching. With the Periodic Steady-State (PSS) analysis followed by a Periodic S-Parameter (PSP) analysis (see Section 2.6.1) reactive matching is also achieved. The input impedance of the EMH at a distinct input power and load can be determined from the solutions of the PSP analysis. From the PSS analysis further important data, like the DC output power and the DC output voltage are made available. To prove the correctness of the simulation results a transient simulation is performed. Then the DC output voltages of the PSU (achieved by both the PSS and the transient analysis) are compared with each other. If the results noticeably differ the stabilization time of the PSS analysis has to be varied and/or the simulator accuracy parameters have to be set tighter. To determine the input sensitivity, the DC output voltage and current of the PSU which are sufficient to operate the energy harvesting system have to be known. Thus, for the design of the PSU, the current consumption of the blocks supplied by the PSU has to be known. Hence these blocks have to

be designed before the PSU is optimized. Knowing the current consumption of all the blocks in the output voltage range of the PSU, the load of the PSU can be simulated by a voltage controlled current source that sinks current, as depicted in Figure 3.6.

As explained in Section 3.3.2, the on-level and the off-level of the LDU1 is 1.1 V and 0.7 V respectively. The DC/DC charge pump is active between these two levels. To achieve a high operating range the on-level should be reached with as little input power as possible. Therefore the input sensitivity of the EMH refers to the point where the output voltage of the PSU reaches 1.1 V in idle mode. To determine the input sensitivity by simulation the source power is adjusted as long as $V_{DD_{RF}}$ reaches 1.1 V, taking the matching into account.

To optimize the PSU, the procedure explained above is repeated while the number of voltage multiplier stages and the transistor geometries are varied ,with the goal of achieving the best performance for a desired DC voltage and load range.

The number of stages and the transistor's geometries vary depending on the load. A high PCE is the main aim in the PSU design. As shown in Section 2.4.1, the lower the load of the PSU the higher the equivalent parallel resistor of the IC and thus the higher the Q Factor. The higher the Q Factor the higher the voltage gain at the input of the PSU and hence the less stages are necessary. The highest possible PCE is achieved with only one stage as shown in Section 2.4.5. But due to the limited Q Factor and the specifications of this energy harvesting system developed for the iTire chip, the simulation results in the best performance with a three-stage voltage multiplier built up using the principle depicted in Figure 3.5.

The PSU is optimized for an output voltage up to 1.1 V. The current consumption in this range is from approximately 100 nA up to a few µA (if the DC/DC charge pump is active). A three-stage voltage multiplier is the best tradeoff between the input power that is needed to achieve an output voltage of the PSU of 1.1 V in idle mode and the input power needed to deliver an output power of approximately 5 µW.

For the implementation of the energy harvester in the proposed WSN, the highest input sensitivity can be achieved if the stored energy in the buffer capacitor C_{Buffer_1} is high enough to pump C_{Buffer_2} to the desired voltage level in one cycle. Therefore the power consumption of the circuit powered by the PSU should be as low as possible in idle mode.

3.4.2 Level Detection Unit 1

The LDU1 senses the output voltage of the PSU and controls the VCO and the DC/DC charge pump. There are two big challenges in the design of the level detection unit:

- Keep the current consumption as low as possible because it is directly related to the operating range of the energy harvester.
- Ensure that the output signal is always correct.

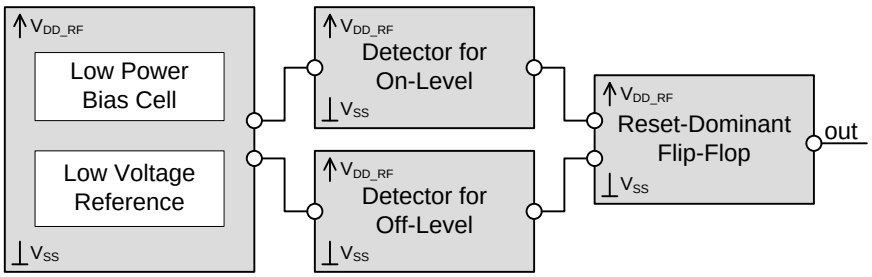


Figure 3.7: Principle of the LDU1

For instance, inverters do not operate correctly until a specific supply voltage is reached. For lower supply voltages the output signal might, but is not necessarily correct. This behavior has to be considered.

If the LDU1 enables the DC/DC charge pump too early the necessary input power of the wireless sensor node strongly increases, for the simple reason that the load of the PSU is approximately 20 times higher than in idle mode. In this implementation the LDU1 has a nominal supply range of 0 to 1.2 V. Of course, the on-level is designed to be 1.1 V, but due to process and temperature variations there is a deviation of approximately 100 mV from the typical detection level.

At very high power at the input of the PSU the DC output voltage can exceed the on-level. As soon as the on-level is reached the VCO and the DC/DC charge pump operate and so the current drawn from the output of the PSU strongly increases with $V_{DD_{RF}}$, which is thus self-limited.

The requirements explained above lead to a compromise between size, current consumption, speed, and accuracy. The LDU1 operates correctly if the rise and fall times of the supply are greater or equal 10 µs. Due to the power characteristics (which depend mainly on the size of the used buffer capacitors) the power consumption of the building blocks and the load of this energy harvesting system, the LDU1 need not be capable of fast rise and fall times. Thus, the values specified above are sufficient and so an ultra low power design is possible.

The supply voltage of the LDU1 depends on the RF input power, the charge of C_{Buffer_1}, and the load of the PSU. The load of the PSU depends again on the charge of C_{Buffer_2} and varies if the VCO and/or the DC/DC charge pump are enabled or disabled. Depending on the level of $V_{DD_{Pump}}$, the load of the DC/DC charge pump and thus the load of the PSU also vary. The level of $V_{DD_{RF}}$ rises as long as the output current of the PSU is higher than the leakage current of C_{Buffer_1} and the current drawn by the LDU1. This condition is described by (3.4.3).

$$I_{PSU_{out}} > I_{Buffer_{1\ leakage}} + I_{LDU_1}\Big|_{V_{DD_{RF}}<1.1\,\mathrm{V}} \tag{3.4.3}$$

Figure 3.7 shows the principle of the LDU1. The LDU1 has two level detectors, one for the on-level and the other for the off-level. A low current consumption is very important and a deviation of approximately 100 mV of the exact level has no influence on the correct function

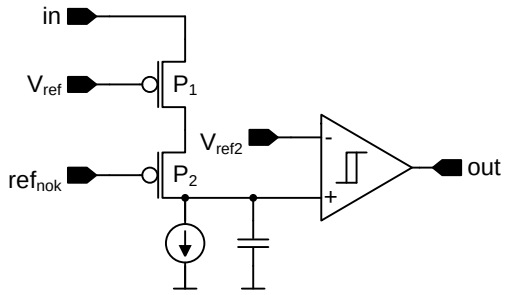
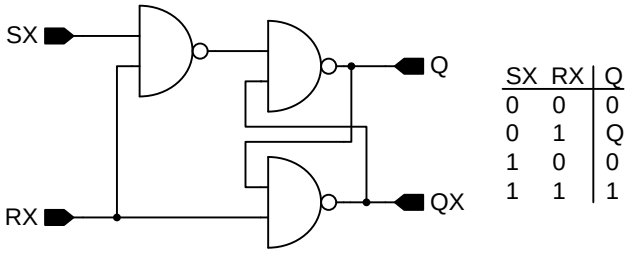


Figure 3.8: Simplified architecture of the level detectors



SX	RX	Q
0	0	0
0	1	Q
1	0	0
1	1	1

Figure 3.9: Reset-dominant RS-FF

of the energy harvester. These conditions make it possible to use a low power Proportional To Absolute Temperature (PTAT) bias cell based on the principle shown in [93] to bias threshold voltage references which are not very accurate. Anyhow the maximum reference voltage deviation is lower than 60 mV in a temperature range from −40 °C to 125 °C. The output voltage $V_{DD_{RF}}$ of the PSU is compared to these reference voltages.

The level detectors are built as in the simplified schematic shown in Figure 3.8. Bias currents of a few nanoamperes and very high ohmic nodes, transient behavior and permanently varying supply voltage complicate the design. P_1 and the current sink operate as a current comparator. The block labeled comparator is a hysteresis comparator with NMOS input. The output of the comparator is buffered to provide a digital output signal. The output signal ref_{nok} of the low power bias cell goes to "low" if the bias cell is in steady-state. That means P_2 is conductive if the reference has its correct level. P_1 is conductive if V_{DD_RF} is one V_T higher than the voltage V_{ref}. The drain of P_2 is connected to the positive input of the hysteresis comparator. The negative input of the comparator is connected to a threshold reference. The hysteresis comparator is used to avoid ringing which can especially occur if a level detector switches and $V_{DD_{RF}}$ decreases a little bit. The output of the comparator is "high" if the positive input is higher than the negative input. That means the output of the comparator is "high" if the bias cell is in steady-state and $V_{DD_{RF}}$ is one V_T higher than the voltage V_{ref}. The difference between the on-level detector and the off-level detector is simply the value of the reference voltage V_{ref}. The outputs of the two level detectors are the inputs of a reset-dominant RS-FF. Figure 3.9 shows the circuit of the reset-dominant RS-FF whose output is "low" as long as the output of the off-level detector is "low" independent of the output of the on-level detector.

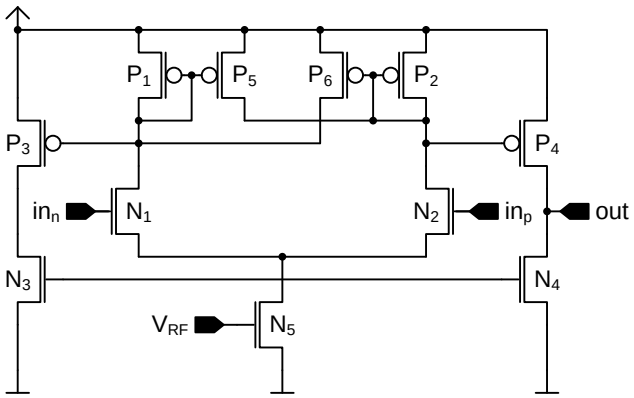


Figure 3.10: NMOS comparator with hysteresis

3.4.2.1 The Deadlock Prevention

Level detectors that are supplied with the same voltage they should observe can easily have a deadlock problem which has to be taken care of. Of course, this problem can be fixed by using a separate voltage regulator for the supply of the LDU1. The voltage regulator also draws some current from C_{Buffer_1}, which makes a current consumption in the nanoampere range impossible. A design like this also has to be insensitive to line variations and transients. For that reason the LDU1 is supplied directly by the PSU. If the rising $V_{DD_{RF}}$ reaches the detection levels of the LDU1 (0.7 V, 1.1 V) and the output current of the PSU is only a little bit (up to a few hundred nanoampere) higher than the leakage current of C_{Buffer_1} plus the idle mode current of the LDU1, a deadlock can occur when the level detector starts to change its output. If the signal changes from "low" to "high" or the other way around, all the capacitances at the affected nodes have to be recharged. Cross currents also flow from V_{DD} to V_{SS} in every inverter or buffer. During this time additional current is drawn from C_{Buffer_1} and as a result $V_{DD_{RF}}$ decreases again. If the current that is needed during the switching phase is too high a deadlock occurs. The higher $V_{DD_{RF}}$ the higher the current in the switching phase. Thus the probability of a deadlock increases with the supply voltage. So $V_{DD_{RF}}$ can increase more and more, but the level detector will not switch before the output current of the PSU is high enough to supply the LDU1 without a decrease in $V_{DD_{RF}}$. To avoid a deadlock situation peak currents of a few microampere are necessary.

The switching phase of the level detector should be as short as possible to keep the current consumption as low as possible. Slow transitions cause high cross currents. So it has to be taken care that the conversion from the analog to the digital signal (fast transitions between "low" and "high") is effective by means of current consumption. Often current starved inverters are used to reduce the cross currents and thus the overall current consumption during the transitions, but at the end of such a chain a common inverter is again necessary to provide a digital signal.

To prevent this deadlock problem, in this work a comparator with hysteresis as shown in Figure 3.10 is used to increase the slew rate of the input signal of the output buffer. So

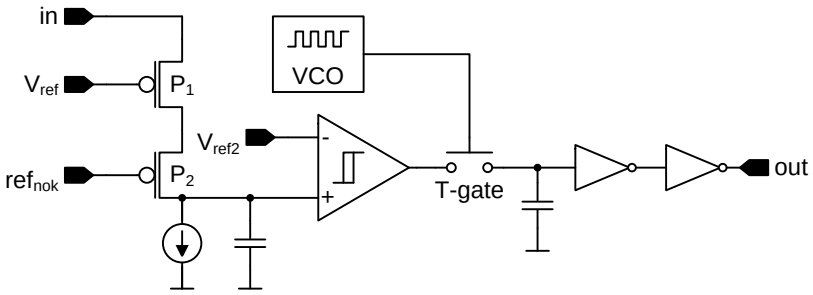


Figure 3.11: Simplified architecture of the switched level detector

the cross currents in the output buffer that provides the digital output signal are limited. Furthermore, buffer capacitors are located close to the output buffers of the level detectors to provide the necessary peak currents for the switching phases.

The deadlock prevention can be improved using the circuit shown in Figure 3.11. The principle is to cyclically connect the detection signal (output of the comparator) to an S-RAM cell. Between the output of the comparator and the S-RAM a T-Gate is inserted that is controlled by an oscillator with low output frequency and low duty cycle. To decrease the current consumption of the LDU even further a time domain comparator as in [1] can be used. Of course it has to be taken care that the S-RAM is set to the correct value at startup. Depending on the desired switching times of the circuit, the oscillator frequency and the duty cycle have to be chosen.

3.4.3 Level Detection Unit 2

The LDU2 works according to the same principle as the LDU1. The current consumption should also be as low as possible and a correct output signal is always guaranteed. It senses the output voltage of the DC/DC charge pump and controls the output power switch of the harvester system.

A simplified block diagram of the LDU2 is depicted in Figure 3.12. The LDU2 has three level detectors. The additional level detector realizes an overvoltage protection. The output of this level detector is a signal controlling the DC/DC charge pump, the so called clock-stop signal. As the name implies, this signal stops the clock for the DC/DC charge pump if the voltage $V_{DD_{Pump}}$ reaches a distinctive level. Thus clock gating is implemented. In this implementation it is ensured that the level detector for the clock-stop has always a higher voltage reference than the level detector for the on-level. To achieve fast startup and stop of the DC/DC charge pump, only the clock output of the VCO is disabled.

The LDU2 has a supply voltage range of 0 to 3.6 V. Detection up to 3.6 V using stacked diode-connected transistors causes inacceptable results. Therefore a low power bandgap cell based on the principle shown in [93] provides a bandgap voltage $V_{ref_{BG}}$ of 1.28 V. The principle of a voltage regulator with a PMOS pass device is used to multiply the bandgap voltage to achieve the correct reference voltage V_{ref} for the input transistor P_1 of the level detector.

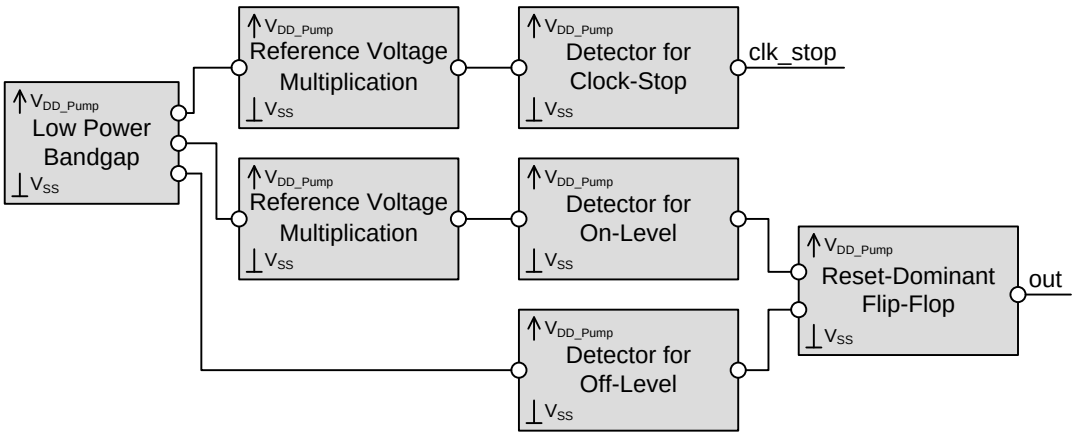


Figure 3.12: Principle of the LDU2

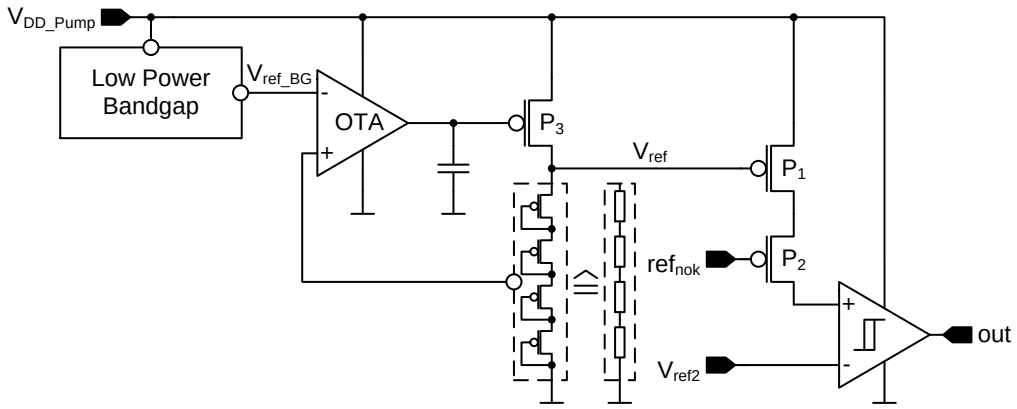


Figure 3.13: Reference voltage generation

The level detector itself is based on the same principle shown in Figure 3.8 like used for the LDU1.

In this implementation the on-level is 3 V and the off-level is 1 V. To generate the correct reference voltage for the on-level detector $V_{DD_{Pump}}$ is divided by a factor of two. That means the reference voltage of the bandgap $V_{ref_{BG}}$ is doubled. Figure 3.13 shows the principle to generate the correct reference voltage. The sensing voltage equals the output voltage of the DC/DC charge pump ($V_{DD_{Pump}}$). $V_{DD_{Pump}}$ is also the supply voltage of the LDU2 and is connected to the source of the PMOS pass device P_3. The drain of the pass device is connected to a transistor-based voltage divider. This voltage divider acts at low voltages like a capacitive voltage divider. The voltage at the drain of the pass device equals the input voltage of the voltage divider. If this voltage reaches $n \cdot V_T$, where n is the amount of the transistors used to built the voltage divider, the voltage divider acts like a resistive one. To limit the current consumption a long transistor length is chosen. Due to the fact that the threshold voltage decreases with the temperature the highest cross current occurs at high temperature. Nevertheless the simulated value of the cross current through the voltage divider is approximately 11 nA at 125 °C.

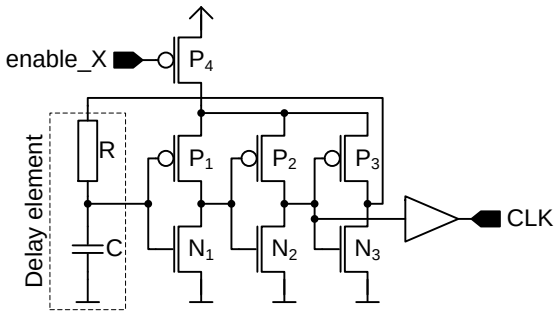


Figure 3.14: Architecture of the VCO

As long as the supply voltage of the Operational Transconductance Amplifier (OTA) is approximately one V_T lower than the desired reference voltage V_{ref} for the level detector, the voltage regulator (OTA plus PMOS pass device) does not operate correctly. Starting from 0 V, V_{ref} rises with $V_{DD_{Pump}}$ till the two inputs of the OTA are equal. This happens when $V_{DD_{Pump}}$ reaches $2 \cdot V_{ref_{BG}}$. From this moment on the voltage regulator operates in its common function. In general the output of the OTA is "low" as long as its positive input is lower than its negative one. If the output of the OTA is at V_{SS} the transistor P_3 is conductive and the input of the voltage divider is connected to $V_{DD_{Pump}}$. The OTA regulates its output in order to achieve equal input voltages. This occurs if $V_{ref} = 2 \cdot V_{ref_{BG}}$. So, if $V_{DD_{Pump}} \geq 2 \cdot V_{ref_{BG}}$, V_{ref} is regulated to be $2 \cdot V_{ref_{BG}}$.

The off-level detection works according to the level detection in the LDU1. The overvoltage protection works like the on-level detection where a higher reference voltage instead of $V_{ref_{BG}}$ for the negative input of the OTA is used. The clock-stop signal is "high" if $V_{DD_{Pump}}$ is higher than 3.3 V.

The outputs of the on- and the off-level detectors are fed into a reset-dominant RS-FF like in the LDU1. The output of the LDU2 is buffered and controls the output switch that is used to power the system connected to the electro-magnetic energy harvester.

3.4.4 Voltage Controlled Oscillator

A three-stage ring oscillator with a single Resistor-Capacitor (RC) stage acting as a delay element is used to clock the DC/DC charge pump. The advantages of the architecture shown in Figure 3.14 are the low voltage characteristics and its simplicity [55]. The frequency of the VCO must be high enough that the DC/DC charge pump is able to provide the current for its output load and to charge C_{Buffer_2}. If the supply voltage of the VCO is 1.1 V or higher and the output current of the PSU is high enough to keep the VCO running in continuous mode the frequency of the VCO should be high enough to provide an output current in the lower microampere range. The frequency of the VCO must be at least high enough that the DC/DC charge pump drives an output current that is higher than the leakage current of C_{Buffer_2} (6 nA) and the current consumption of the LDU2 (310 nA). An output current of a few microampere

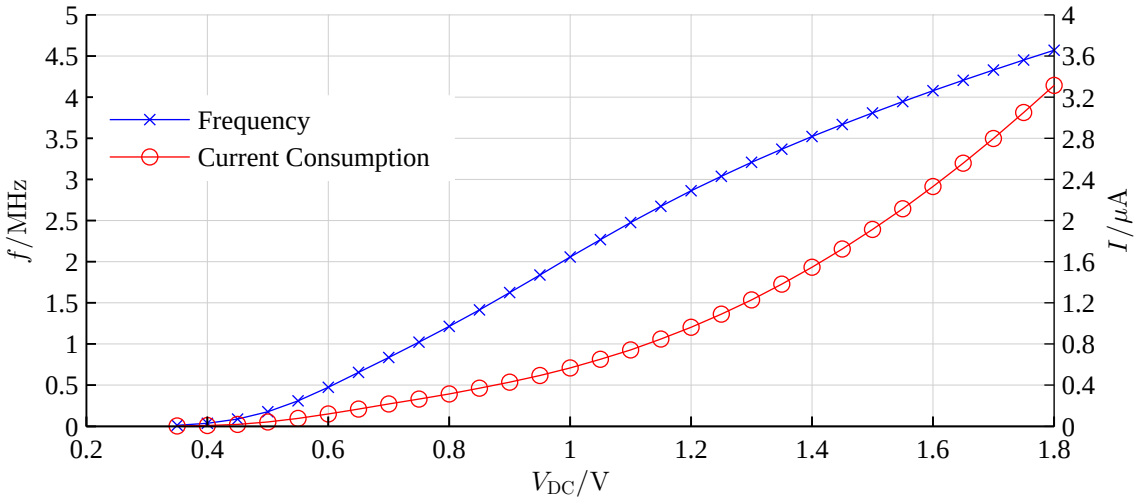


Figure 3.15: Simulated frequency and current consumption of the VCO over supply voltage variation

is chosen to be able to charge C_{Buffer_2} in a few seconds. At high input power the energy harvester can then power sensors or other circuits continuously.

Figure 3.15 shows the oscillator frequency and current consumption as a function of supply voltage. The higher the supply voltage $V_{DD_{RF}}$ the higher the oscillating frequency is and the faster the on-level of the LDU2 will be reached. Due to the fact that the output voltage of the DC/DC charge pump should reach the on-level of the LDU2 (3 V) even if its input voltage is near the off-level of the LDU1 (0.7 V), the oscillating frequency is designed to be approximately 700 kHz at 0.7 V. As can be seen from Figure 3.15 the current consumption is only 216 nA at 0.7 V. The VCO can operate at a supply voltages higher than approximately 0.3 V although the lowest supply voltage of the VCO is 0.7 V in the proposed wireless sensor node.

3.4.5 DC/DC Charge Pump

Capacitive DC/DC charge pumps transfer charge from the input to the output by means of capacitors. The DC/DC charge pump is based on the Dickson topology [19] and depicted in Figure 3.16. Packets of charge are pumped along the diode chain. The coupling capacitors are charged and discharged during the positive and negative cycle of the VCO's clock signal respectively. So the voltage increases with every stage of the charge pump. The diodes are realized with PMOS transistors and the capacitors are realized with Metal-Insulator-Metal (MIM) capacitors which provide very low leakage. The tradeoff between transistor geometries and parasitic capacitances is also important here. Using PMOS transistors as diodes reduces the forward voltage drop compared to NMOS transistors because their body effect (see (2.5.17) on page 46) increases with every stage. PMOS transistors can only be used for low output currents because the highest potential of the PMOS transistors is one V_T higher than the bulk

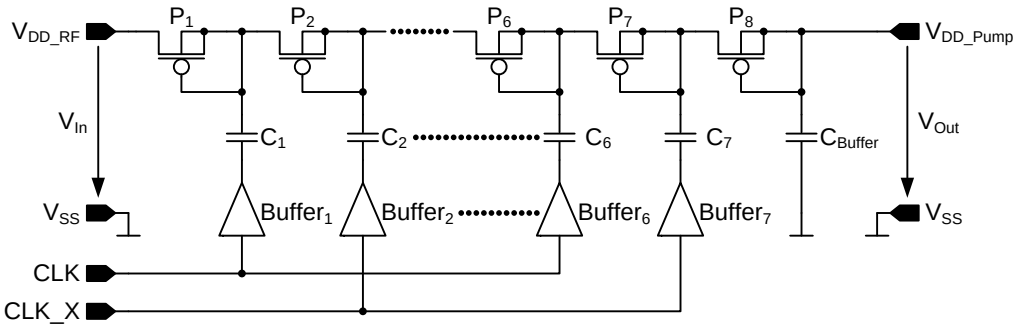


Figure 3.16: Architecture of the DC/DC charge pump

potential. To avoid substrate currents the PMOS transistors are designed with guard rings to connect the n-well and the p-substrate low ohmic. The number of stages depends on the input voltage, the amplitude of the clock signal, the desired output voltage, and the desired output load. The average current consumption of the DC/DC charge pump is about 1.5 µA. In this work seven stages are necessary to be able to charge C_{Buffer_2} to 3 V from an input voltage and a supply voltage of the buffers in the DC/DC charge pump of approximately 700 mV even in worst case conditions.

3.4.6 On-Chip Sensor

As written in Section 1.4.1.3 the on-chip sensor is not the focus of this thesis. Nevertheless, in this section the architecture is shown and based on that, the general operating principle is explained.

As the sensing operation is sensitive to supply voltage variations a separate low power voltage regulator is used to supply the sensor block. The wireless sensor node includes an on-chip temperature sensor. Other sensors or monitoring devices can be connected to the output of the energy harvesting system, where the sensing voltage has to be in the range (a) 0 to 600 mV or (b) 300 to 900 mV. These are the two input voltage ranges covered by the ADC.

Figure 3.17 shows the architecture of the sensor block including a control unit, an oscillator, a switched capacitor bandgap voltage reference, a multiplexer and an ADC. The oscillator provides a clock of 1 MHz for flow control, the bandgap and the ADC.

The operating principle of the sensor itself is as follows: The internal temperature sensor compares a temperature dependent voltage to a temperature independent reference which both are generated by a low power switched capacitor bandgap cell based on the principle presented in [14]. Temperatures between −40 °C to 125 °C can be measured. These two voltages are buffered and then fed to the input of an ADC whose block circuit is shown in Figure 3.18. The ADC uses a Successive Approximation Register (SAR), a split capacitive Digital to Analog Converter (DAC) and a time-domain comparator according to the principle in [1] with two equally sized 5 bit arrays to keep the current consumption low.

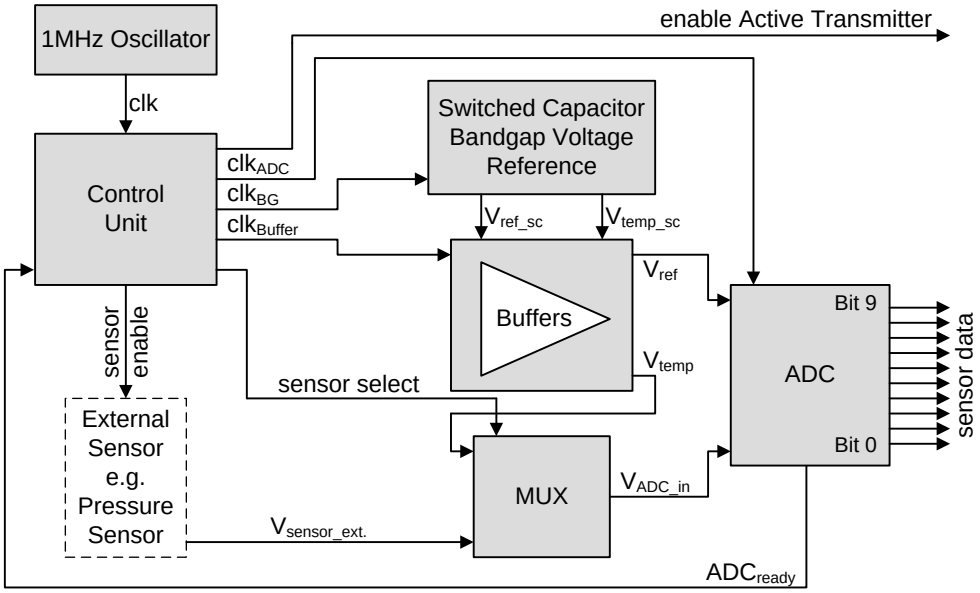


Figure 3.17: Block diagram of the on-chip sensor block

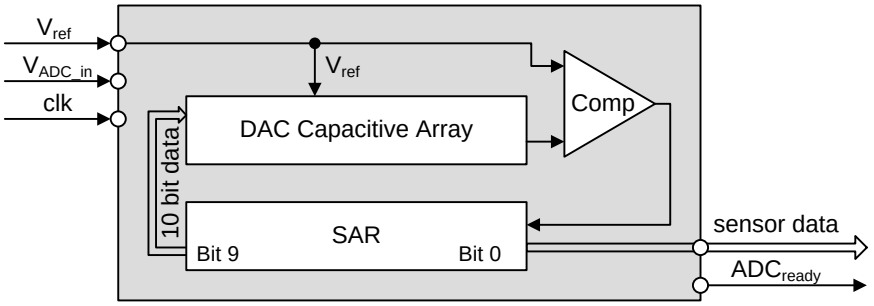


Figure 3.18: Block diagram of the ADC

3.4.6.1 Measuring Sequence

The typical operation of a measurement cycle can be explained as follows: If the output of the DC/DC charge pump reaches 3 V the output switch is enabled and thus the sensor block is supplied. If the supply voltage is high enough the control unit starts the sense operation which can be divided in three subsequences.

- First the switched capacitor bandgap cell is enabled and after settling it provides the temperature dependent and the temperature independent voltages.

- After a constant time the buffers for the two above stated voltages are activated and subsequently the ADC starts to convert the analog input voltage into digital data, where the temperature independent voltage is used as reference for the ADC.

- After successful conversion the signal ADC_{ready} changes to "high". If the supply voltage is still high enough, the control unit enables the active transmitter and the sensor data is sent to the base station.

3.4.6.2 Voltage Supply

To protect this block from harmful voltages and to ensure proper operation its supply voltage is regulated to be 1.2 V using an NMOS regulator. Due to the low current consumption of the on-chip temperature sensor and the ADC a high Power Supply Ripple Rejection (PSRR) of the regulator is necessary [39]. This regulator is also capable of low-drop operation and therefore it includes a charge pump. More information about this regulator is available in [39].

3.4.7 Active Transmitter

The sampled sensor data can be transmitted via an active transmitter which uses a BAW resonator instead of the commonly used crystal as frequency reference. With this approach the startup time of the oscillator used in the active transmitter is reduced by a factor of up to 1000 compared to conventional crystal oscillator systems [90]. That means the transmitter needs less time to be ready for transmission. Due to the fact that the transmitter uses the energy stored in C_{Buffer2}, a smaller capacitor can be used if the on-time of the transmitter is reduced.

The basic architecture of the active transmitter is shown in Figure 1.2 in Section 1.4.1.5 on page 7. Furthermore, a brief introduction is also given there. The active transmitter is not directly connected to the output of the EMH. For the same reason as for the sensor, the supply voltage of the active transmitter is also regulated.

During the transmission of the sensor data, a decent load regulation for the power amplifier is desired but not easy to achieve. For a better decoupling, the power amplifier is supplied by a separate voltage regulator. Thus, two voltage regulators, one for the so called carrier generation unit and one for the power amplifier are implemented for the active transmitter. Both regulators provide a supply voltage of 1.5 V. The purpose of the carrier generation unit is to mix the output of the local IQ oscillator with the output of the BAW oscillator. The power amplifier is used to transmit the generated data at four different power levels as described in Table 1.1 on page 8.

Both supply voltages are regulated using PMOS regulators explained in [39]. Comparing the stabilization methods, the two architectures are quite different. The supply of the power amplifier has to be available off-chip. The power amplifier is of Class E and uses an off-chip inductor which is connected between the output of the power amplifier and the voltage regulator. This fact is exploited to use an off-chip capacitor for dominant-pole compensation. In contrast, the supply voltage for the carrier generation is not available via a pin. That means no off-chip components are available for compensation. To prevent oscillation in the control

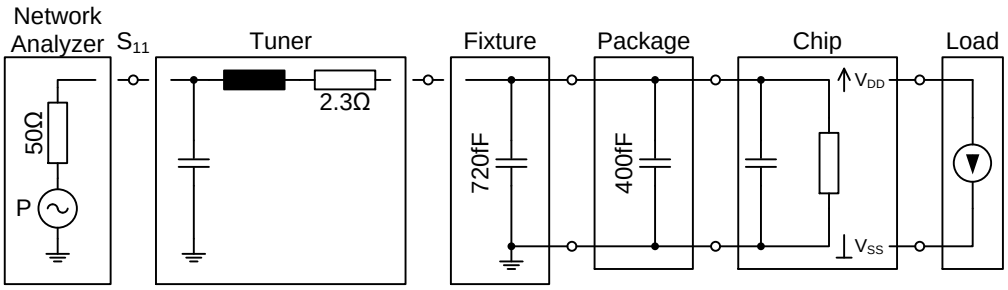


Figure 3.19: Contact-based measurement setup for the PSU of the EMH

loop, a zero has been introduced in the s-domain for compensation. More information about the regulators for the active transmitter are available in [39].

3.5 Measurement Results and Comparison

This section discusses the measurement results of the EMH and includes a comparison to recent publications and state-of-the-art products operating at the mainstream frequency ($f \approx 900\,\text{MHz}$) of passive RFID systems. Measurements are done to determine the input sensitivity of the energy harvester, the leakage currents of the buffer capacitors, the current consumption of the blocks accessible from the outside and the switching levels of the level detectors. For testing purposes some control signals are accessible from outside. The different power domains can also be separated to measure current consumptions and detection levels separately.

3.5.1 Determination of the Input Sensitivity

A key parameter for a WSN is the input sensitivity (definition see Section 2.1.1). To determine the input sensitivity an appropriate measurement setup is necessary. Furthermore, the losses of the measurement setup itself have to be considered.

The input sensitivity of the EMH is defined in Section 3.3.3. This definition is chosen to realize a meaningful comparison with other remotely powered systems. How the input sensitivity can be measured using non-expensive measurement equipment has already been explained in Section 2.7.2.3. Based on these considerations the contact-based measurement setup depicted in Figure 3.19 is utilized. The package of the chip and the test fixture used to connect the packaged chip to the coaxial measurement equipment are identical with those used and explained in Section 2.7.2.1.

The measurement procedure can be explained as follows:
A network analyzer is used to power the chip. To tap the full potential, the power has to be fed to the chip properly, thus a tuner is used. The drawbacks and behavior of such a tuner

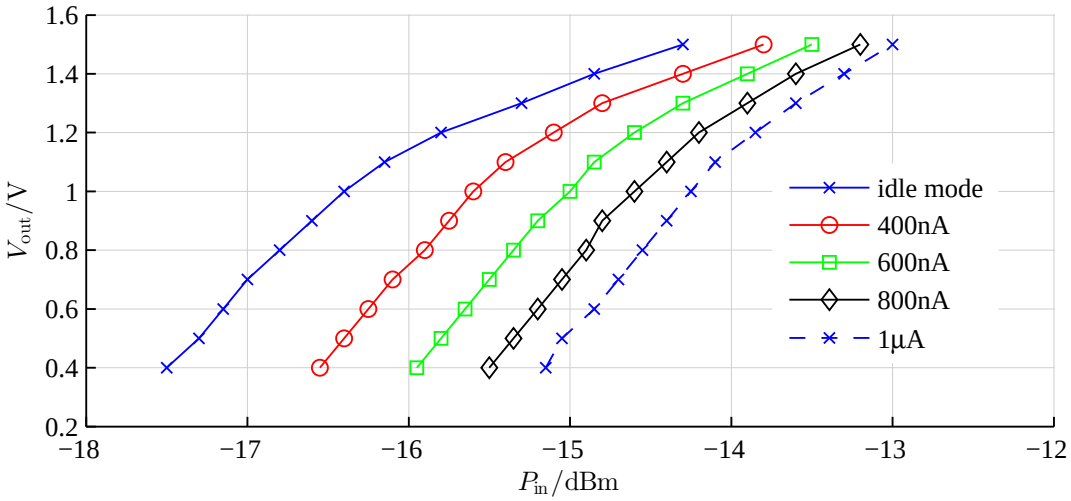
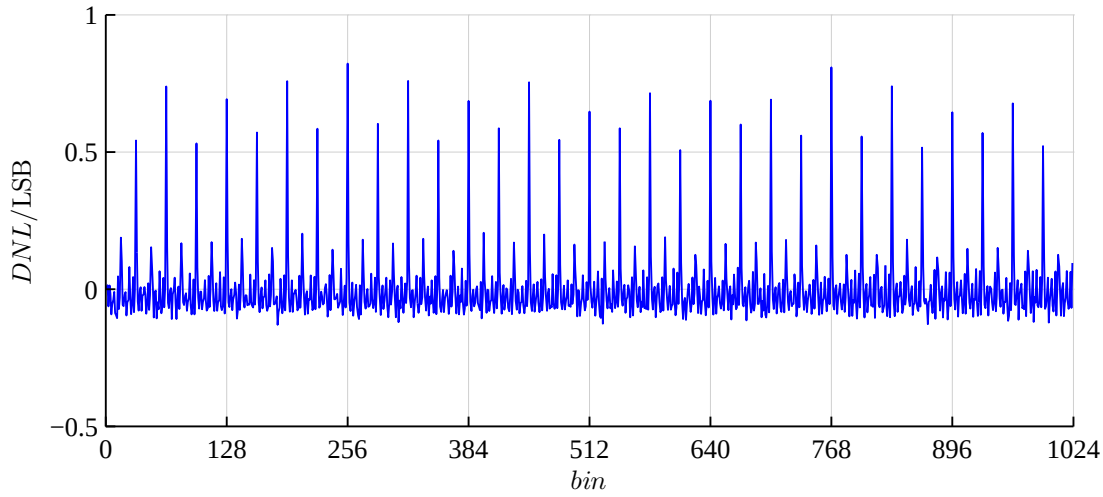


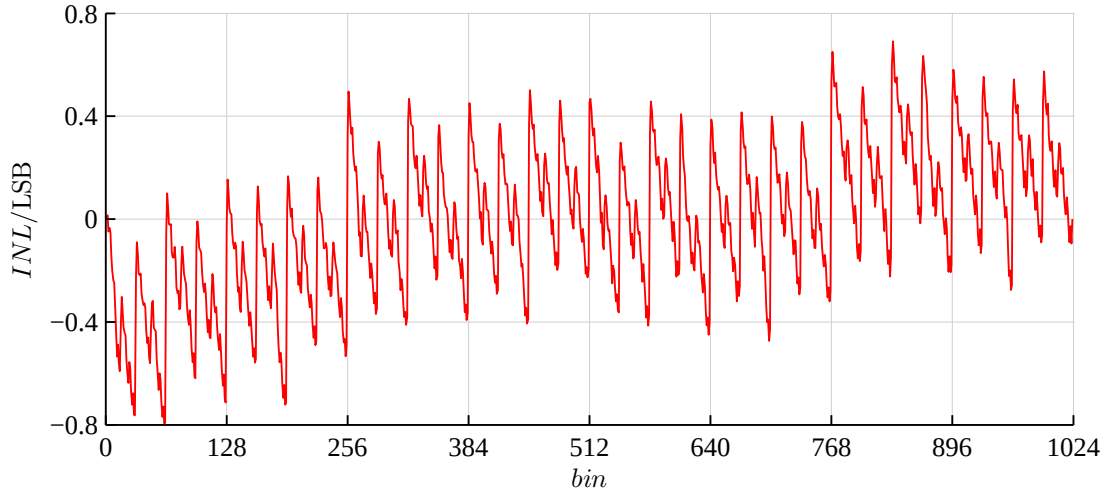
Figure 3.20: Measured V-P characteristic of the PSU at $f = 900\,\text{MHz}$

are also explained in detail in Section 2.7.2. To also consider the impedance mismatch between the power source and the PSU if the LDU1 switches at its worst case switching point ($V_{DD\_\text{RF}} \approx 1.2\,\text{V}$), the chip is matched to reach the maximum sensitivity when the DC output voltage of the PSU is sufficient for the LDU1 to enable the VCO and the DC/DC charge pump ($V_{DD\_\text{RF}} \approx 1.1\,\text{V}$).
Before the input sensitivity of the EMH can be determined, the current consumption of the LDU1 has to be measured. Therefore the LDU1 is separated from the other blocks by setting the correct configuration inputs that are implemented for testing purposes. Knowing the current consumption of the LDU1 in its supply voltage range, the worst-case input sensitivity regarding the switching behavior can be determined. Therefore the PSU is now separated from the other blocks and a current source which is set to sink 172 nA at 1.2 V is used as load. $V_{DD_{RF}} = 1.2\,\text{V}$ is chosen because this is the worst-case switching point of the LDU1 and so the operating point with the highest current consumption. The output power of the network analyzer is increased until the settings of the current source are reached in consideration of the fact that the tuner parameters are permanently set to minimize S_{11}. At $V_{DD_{RF}} = 1.2\,\text{V}$ an input sensitivity of $-15.8\,\text{dBm}$ is measured at a frequency of 900 MHz neglecting all measurement losses. Using the method explained in Section 2.7.2.3, the losses caused by the matching circuit can be calculated to be 3.9 dB. This leads to a corrected input sensitivity of $-19.7\,\text{dBm}$.

To give an impression of how the current consumption of the LDU1 in idle mode influences the input sensitivity, the DC output voltage of the PSU is measured at different RF input power levels at a frequency of 900 MHz. The load of the PSU is varied from the idle mode current consumption of the harvester system up to 1 mA. The values in Figure 3.20 are not corrected by the losses of the measurement system, which is the same as used to determine the input sensitivity.



(a) DNL



(b) INL

Figure 3.21: Static characteristics of the ADC

3.5.2 System Measurements

The static characteristics of the ADC are measured and plots of both the Differential Nonlinearity (DNL) and the Integral Nonlinearity (INL) are shown in Figure 3.21.

The buffer capacitors used for $V_{DD_{RF}}$ and $V_{DD_{Pump}}$ must have low leakage currents because they are directly related to the input sensitivity. The measured leakage current of the external capacitors is less than 6 nA.

Taking the power consumption of the VCO into account, the average efficiency of the DC/DC charge pump is 32 % for an output current of a 310 nA, which is the current consumption of

Energy harvester	
Technology	0.13 µm CMOS
Input sensitivity	−19.7 dBm
Output voltage	3.0 V - 1.0 V
LDU1	
Maximum supply voltage	1.6 V
Current consumption: total	172 nA @ 1.2 V
Current consumption: PTAT bias cell	103 nA @ 1.2 V (simulated)
LDU2	
Maximum supply voltage	3.6 V
Current consumption	310 nA @ 3.0 V
External buffer capacitors	
$C_{Buffer1}$	20 µF
$C_{Buffer2}$	2 µF
Sensor block	
Supply voltage	1.0 V
Current consumption: total	2.7 µA
Current consumption: SC bandgap	497 nA
Current consumption: Control logic	85 nA (simulated)
Temperate range	−40 °C - 125 °C
ADC	
ENOB	8.2 bit @ 36 ksamples/s
FOM	419 fJ/conversion step

Table 3.1: Key figures of the wireless sensor node

the LDU2 at a supply voltage of 3 V. When the output switch is open the current consumption from the DC/DC charge pump is only the current used by the LDU2 plus the leakage current of $C_{Buffer2}$ plus the charging current of $C_{Buffer2}$.

The maximum deviations from the simulated detection levels are 58 mV for the level detectors in the LDU1 and 14 mV for the clock-stop-detector and 3 V-detector in the LDU2. Six samples were measured at 27°.

The measured average consumption of the sensor block is 2.7 µA whereas the switched capacitor bandgap consumes only 497 nA. The Effective Number of Bits (ENOB) of the ADC is 8.2 @ 36 kS/s and its Figure of Merit (FOM) is 419 fJ/conversion step.

The key figures of the building blocks of the WSN are summarized in Table 3.1, whereas the key figures of the active transmitter can be found in Table 1.1 on page 8.

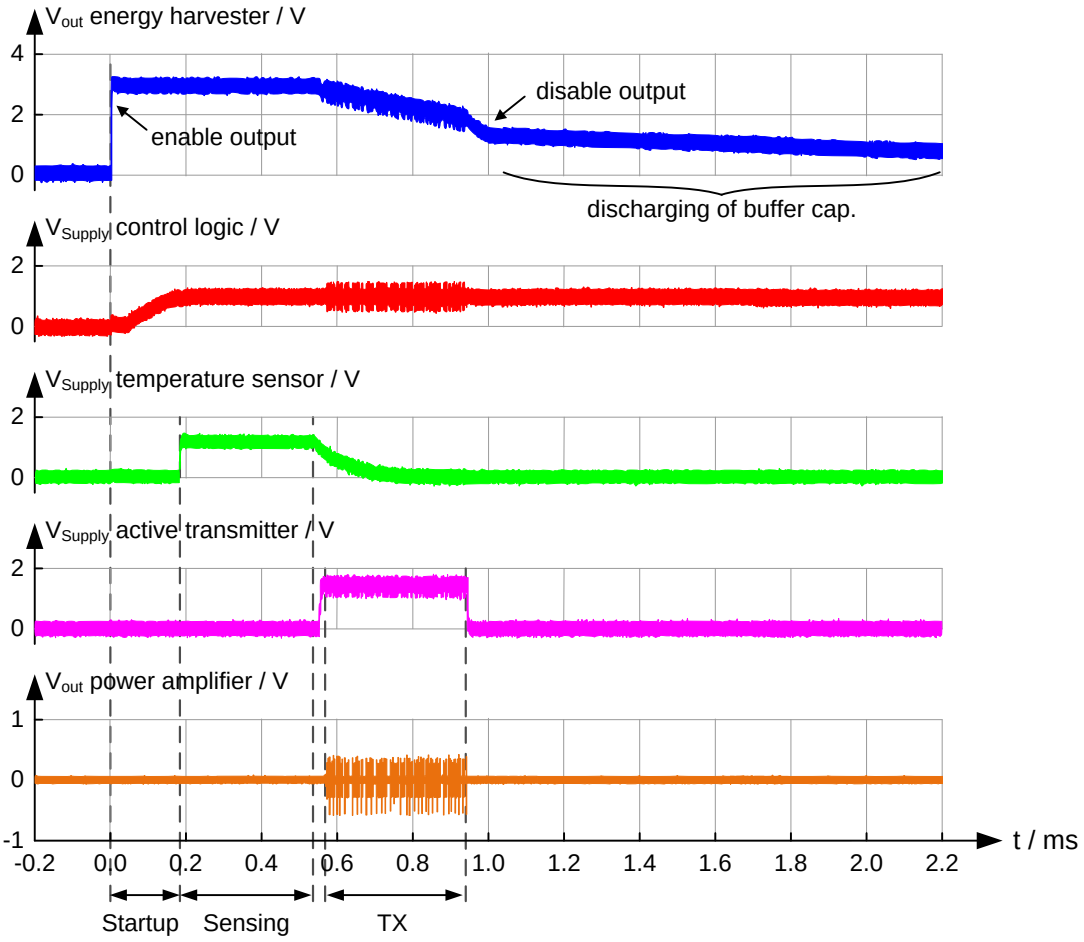


Figure 3.22: Transient behavior of the WSN during a typical temperature measurement and transmission cycle

3.5.3 Transient Behavior

To create an impression of how the energy harvesting system performs in a typical temperature measurement and transmission cycle, the transient behavior of the important signals is determined by measurement and depicted in Figure 3.22. If the voltage of $C_{Buffer2}$ (V_{out} energy harvester) reaches 3 V the output switch becomes conductive and the control unit in the sensor block (see Section 3.4.6) is powered. After startup (approximately 180 µs), the temperature sensor is enabled. 340 µs later the temperature measurement, including the conversion of the analog data into digital is finished. Then the active transmitter (see Section 3.4.7) is enabled, and after startup of the oscillator for carrier generation, the sensor data is transmitted.

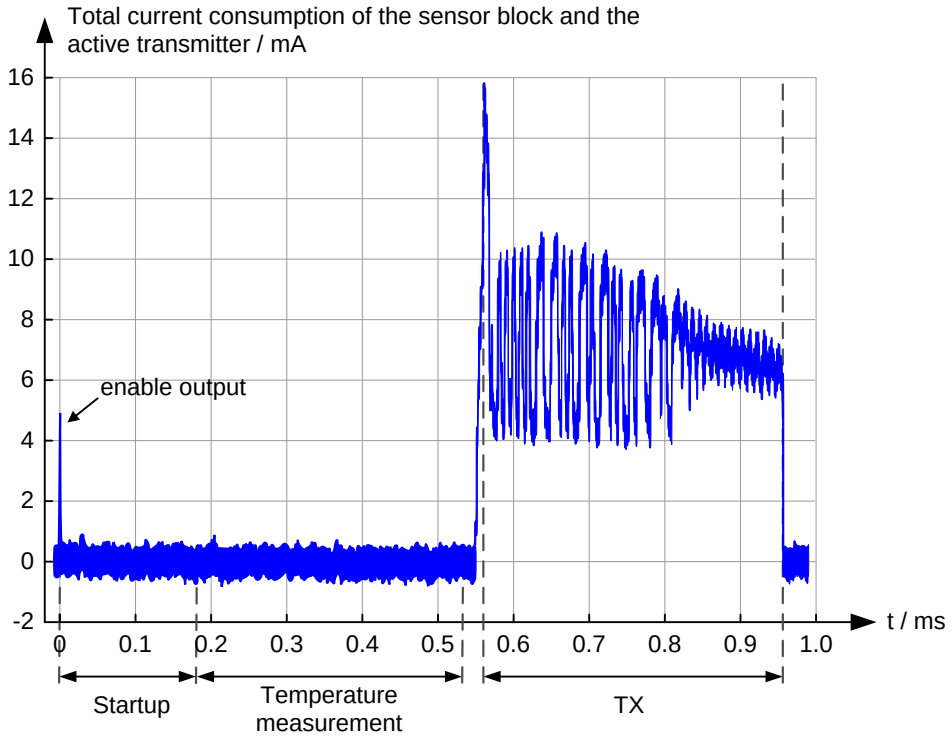


Figure 3.23: Current profile of the WSN during a typical temperature measurement and transmission cycle

3.5.3.1 Current Profile

The measured current profile is shown in Figure 3.23. As can be seen from Figure 3.23 the current consumption of the active transmitter dominates. The first peak at startup is caused by the switching of the LDU2 which enables the output of the energy harvesting system. The peak at approximately 560 µs is caused by the charging phase of the buffer capacitor of the power amplifier in the test arrangement.

3.5.4 Comparison with State of the Art

The majority of publications in the field of electro-magnetic energy harvesting deal with circuits dedicated for use in RFID transponders, which usually require at least ten times more DC power than the EMH in idle mode. Hence, Table 3.2 shows a comparison with state-of-the-art publications that cover investigations near or in the output load range of the presented EMH. The output power of all ICs in Table 3.2 is always lower than the input power as there is no mechanism implemented that operates as shown in this chapter. Thus, only the performance of the PSUs can be compared.

In [87] as well as in [104] the RF to DC conversion is performed by a PSU with an on-chip matching network. Even if the input sensitivity is given with −24 dBm for an open output

Chip	Technology	Area	Frequency	Sensitivity	AC/DC type
this work	0.13 µm	0.32 mm^2	900 MHz	−19.7 dBm @ 1.2 V/172 nA	3-stage se. mult.
[87] by G. Papotto	90 nm deep n-well	1.35 mm^2	915 MHz	−19.0 dBm @ 1.2 V/400 nA −21.5 dBm @ 1.2 V/no load	17-stage se. mult.
[104] by A. Shameli	0.18 µm	0.80 mm^2	920 MHz	−16.5 dBm @ 1.2 V/120 nA	4-stage se. mult. on-chip inductor
[66, 67] by T. Le	0.25 µm floating gate	0.40 mm^2	906 MHz	−21.5 dBm @ 1.2 V/214 nA	36-stage se. mult.
[42] by P. Hsieh	0.18 µm	0.28 mm^2	830 MHz	−17 dBm for startup	diff. rect. + DC/DC CP
[107, 108] by T. Umeda	0.30 µm	0.64 mm^2	950 MHz	−14.0 dBm @ 1.5 V/400 nA	6-stage se. mult.
[53] by U. Karthaus	0.50 µm Schottky	–	869 MHz	−20.1 dBm @ 1.5 V/950 nA	mult.

Table 3.2: Comparison with state of the art

in [87], the values in Table 3.2 can be derived from the measurement curves, which leads to a comparable sensitivity. As 17 stages are used in [87], the losses of the rectifying transistor seem to be very low in the 90 nm CMOS process used with deep n-well option. The drawback that comes with an on-chip matching circuit is the limited bandwidth which prohibits multi-frequency operation.
In [66, 67] floating gate transistors are used to tremendously reduce the threshold voltage. Thus it is possible to implement 36 multiplier stages and operate from 50 mV input voltage. It seems that there is no overvoltage protection implemented in [66, 67], [87], and [104].
In [42] a differential rectifier with subsequent DC/DC converter is implemented, which leads to a high efficiency. Due to the fact that a standard 0.18 µm CMOS process is used, the sensitivity is moderate.
A six-stage single-ended voltage multiplier using the SC-VTC method as presented in Section 2.4.4.3 is shown in [107, 108]. The achieved input sensitivity is measured while an external DC voltage generator generates the bias voltages.
A well known and older publication is the UHF RFID transponder with very low input power presented in [53]. As there is no EPC compatible digital core implemented, the DC load is lower than in common UHF RFID transponders, so this publication is also considered. A simple voltage multiplier is used but implemented with Silicon-Titanium Schottky diodes with low series resistance and low Schottky junction capacitance. Assuming that the measurement values in [53] are correct this leads to an input sensitivity of −20.1 dBm for the load characteristics shown in Table 3.2.

This work was implemented in a low-cost process, thus the achieved sensitivity is a promising result. As is obvious from this comparison, the input sensitivity of a PSU can be enormously increased if devices with low threshold voltages and low losses are available. Nevertheless the consumed DC power of the control circuit is directly related to the input sensitivity, no matter which process is used. A power consumption of the EMH of just 190 nW in idle mode lays the foundation for future work.

3.6 Conclusion

This chapter presented an electro-magnetic energy harvesting system designed to operate as WSN. The target operating frequency ranges from 100 MHz up to 2.45 GHz, while the energy harvesting system is optimized and investigated for the 900 MHz range, which is a mainstream and widespread UHF RFID frequency range.

The presented WSN includes an on-chip temperature sensor and a BAW-based active transmitter to reach higher transmission ranges. Thus the functionality of the EMH and the applicability for the iTire chip can be proved. Usually remotely powered devices are limited in complexity and working range due to the constant lack of energy. The innovative concept of dividing the energy harvesting system into two subsystems makes it possible to decouple the input sensitivity from the load of the system. In addition this concept makes it possible to provide a time limited DC output power which is a multiple of the IC's average RF input power. Systems with a power consumption up in the milliwatt range can be powered using the presented EMH. Not even a battery is required, which makes the system cost-effective, maintenance free, and environmentally friendly.

The EMH features a PSU, two LDUs, a VCO and a DC/DC charge pump. Due to the usually low Q Factor of the broadband antennas used, full chip operation is needed from just a few hundred millivolts between the input pins of the PSU. Thus an adopted voltage multiplier design was chosen. As the current consumption of the LDU1 is directly related to the operating range, it is very low. The design of the LDUs is done with awareness of the deadlock problem that can easily occur due to the supply voltage conditions. The supply voltage of the LDUs is also the same voltage that should be observed. The current consumption of the VCO, the DC/DC charge pump, and the LDU2 is not directly related to the operating range. The higher the current consumption the bigger C_{Buffer_1} and/or the more cycles it takes to charge C_{Buffer_2}. So there is still room for improving the efficiency of the DC/DC charge pump and the current consumption of the VCO and the LDU2.

The presented concept is verified by measurement at different operating frequencies, whereas the reported values refer to an operating frequency of 900 MHz. Using the 900 MHz RF field as power source enables an easy integration of the WSN in commonly existing systems. The EMH combines both high input sensitivity and high output power to increase the applicability of systems powered from the electro-magnetic field. A power consumption of only 190 nW in idle mode results in an input sensitivity of -19.7 dBm. Compared to state-of-the-art published work in Table 3.2 and UHF RFID transponders commercially available and measured in [84], this is a promising improvement.

Chapter 4

Multifrequency for RFID

The original publications related to this chapter are [97, 99] (own publications). ■

In this thesis two solutions for a multifrequency frontend for Radio Frequency Identification (RFID) transponders are presented, while in this chapter the multifrequency RFID transponder using the Power Scavenging Unit (PSU) published in [99] is presented. This multifrequency RFID transponder is capable of HF as well as UHF, which are the two mainstream frequency ranges in passive RFID systems.
This chapter starts directly with the motivation for a multifrequency design followed by the system architecture, including an explanation of the basic functionality of the multifrequency RFID transponder. The main part of this chapter covers the design considerations and the implementation, while the main building blocks, like the multifrequency rectifier, the combined V_{DD} limiter and modulator block, the demodulator, the frequency detection unit, and the clock generation and control are presented. The multifrequency RFID transponder chip is measured at HF (13.56 MHz) as well as at UHF (860 MHz to 2.45 GHz) and the key parameters and measurement results are shown.

4.1 The Need for Multifrequency

Conventional RFID systems operate at a single carrier frequency. Such systems can hardly handle the great variety of shapes and materials that occur in products and packaging [69]. Of course, depending on the national regulations and on the area of application, this carrier frequency varies from kilohertz up to gigahertz. The two widespread groups of passive RFID systems are HF and UHF RFID systems. HF RFID systems are much more widespread in Europe than in the USA. Which of the two RFID systems is utilized depends mainly on the environment, because it considerably affects the tag's characteristics. Also the operating range of HF and UHF RFID systems differs strongly. Of course there are application areas where HF as well as UHF RFID systems fulfill their work reliably. State-of-the-art passive RFID transponders can not operate in different frequency ranges, thus separate transponders are needed for HF and UHF RFID systems.

As explained in Section 1.4 the advanced Tire Pressure Monitoring System (TPMS) chip contains RFID technology. As tires are available in different countries with different national frequency regulations, an RFID transponder operating at a single carrier frequency or in a

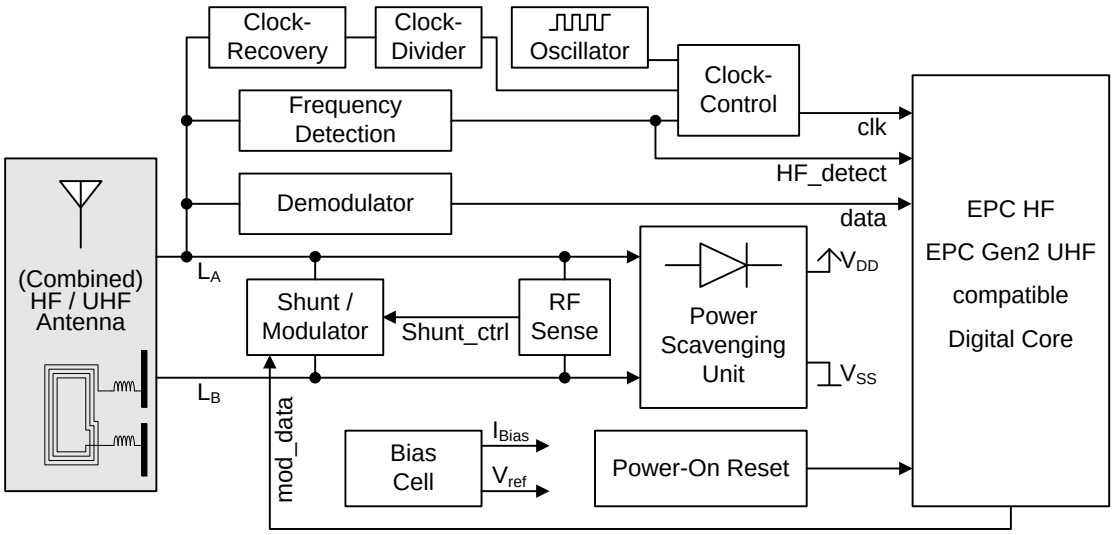


Figure 4.1: System architecture of the remotely powered multifrequency transponder

small frequency range cannot fulfill the requirements of the advanced TPMS chip. This shows that there is a need for a multifrequency design.

A multifrequency design increases the flexibility and applicability of RFID systems. The different characteristics of HF and UHF RFID systems, namely the large operating range in UHF and the high available power in HF, can be exploited for a high quality design for a variety of applications. New applications arise, RFID transponders can easily be enhanced with a wide range of sensing and security applications. The transponder or Wireless Sensor Node (WSN) can be supplied by inductively coupling whereas the data can be transmitted at UHF.

A multifrequency transponder enables worldwide identification with only one tag, which is desired for the advanced TPMS chip of the iTire project. Additionally, the multifrequency approach increases the flexibility and applicability of RFID systems and remotely powered devices.

4.2 System Description

To understand the function and receive an overview, this section introduces the system architecture with the basic operating principle of the multifrequency RFID transponder. Then some system characteristics are explained, which specify the chip. The presented multifrequency RFID transponder chip fulfills the requirements of the iTire chip and can thus be implemented to perform identification.

4.2.1 System Architecture

Figure 4.1 shows the system architecture of the remotely powered multifrequency transponder. The PSU converts the incoming AC power into DC power to supply the chip. The PSU has to cope with different input power levels and different modulation depths at HF and UHF. Therefore a special concept is utilized requiring only two input pins for the antenna connection. To ensure correct operation and prevent false output signals the power-on reset block enables and disables the digital core depending on the supply voltage. The bias cell provides the bias currents and threshold voltage references. The demodulator recovers the information from the Amplitude Shift Keying (ASK) modulated carrier emitted by the reader. The data is then fed into the digital core to be processed there. The combined shunt and modulator protects the chip against overvoltage. If the shunt is active the resistance between the input pins is lowered. This also results in a mismatch, which lowers the incoming power. The remaining excessive input power is converted into thermal energy. The tag communicates with the reader by load modulation in HF mode or backscatter modulation in UHF mode. Switching a load resistance between the input pins on and off causes voltage changes at the tag antenna as well as at the reader antenna. So load modulation is performed. The backscatter modulation is achieved by varying the impedance of the frontend in accordance with the data being sent. The frequency detection unit detects which field (HF or UHF) is applied to the tag. With this information the correct blocks are powered and the correct parameters are set. Of course, the digital core is also controlled by the frequency detection unit. The clock recovery extracts the carrier signal from the field transmitted by the HF reader. This clock is divided by the clock divider and then fed into the clock control unit. At UHF a clock recovery cannot be used due to power consumption reasons and a modulation index of up to 100 %. Therefore a local oscillator is implemented which is enabled by the frequency detection unit in UHF mode. The clock control unit selects the clock from the clock recovery or the local oscillator depending on the operating frequency and connects it to the digital core.

4.2.2 Antenna

Every RFID transponder needs some kind of antenna to operate. To tap the full potential of the Integrated Circuit (IC), a dual band antenna that is capable of both HF and UHF is convenient. Some novel dual or multiband antenna solutions are presented in [16, 41, 65, 77].

The design of a dual band antenna comes with one or the other challenge as described in [76]. Some requirements desired at one frequency band may have a strong impact in the other band. To achieve resonance at HF an large shunt capacitor is needed that is in parallel with the IC's input to tune the HF transponder coil to its resonant frequency. This shunt capacitor will short circuit any currents at UHF and inhibit operation. For that reason it must not be implemented in a dual band IC. Also, many antenna structures that are often found in conventional UHF transponders are ruled out by the HF antenna coil, which manifests itself similarly to a closed loop at UHF.

In [76] L. Mayer and A. Scholtz designed a dual band antenna that was dedicated for the use within the project *Comprehensive Transponder System*. L. Mayer developed modified versions of this antenna to match it to the analog frontends of the presented IC's in this work. The dual band antenna consists of a shorted loop slot antenna [69] serving the UHF band combined with a printed spiral operating as an air coil in the HF band. As a tuning capacitor would inhibit operation at UHF, the HF antenna coil has to be resonant on its own, which is achieved by substrate capacitors. Two HF antenna coils result from re-using the UHF loop slot antenna. The combined antenna is developed using a very thin and flexible laminate. More information is given in [69].

4.2.3 System Characteristics

To simplify the following considerations and explanations, some characteristics are defined in this section.

Input Sensitivity – Minimum Input Power

As stated in Section 2.1.1, the input sensitivity identifies the point where the RF input power is sufficient to operate the chip. The input sensitivity in the design phase refers to the point where the output voltage of the PSU reaches 1 V at the simulated DC load of the analog building blocks and the digital core. To determine the input sensitivity by measurement, the chip's reply is observed. So in the measurement the input sensitivity is determined by decreasing the input power as long as the chip responds. Then the set input power equals the input sensitivity.

For HF transponders the input sensitivity is better known as minimum operating field strength and is specified with the unit "$\mathrm{A\,m^{-1}}$" instead of using "dBm" as done for UHF transponders.

Minimum DC Operating Voltage

The minimum DC operating voltage is the supply voltage of the digital core if the chip is powered with the minimum input power, the RF input signal is in unmodulated state and the chip does not backscatter any data.

Overall DC Current Consumption

The overall DC current consumption is the total load current of the PSU. The DC load current can be split in the current consumed by the analog blocks and those consumed by the digital core.

Operating Frequency

The operating frequency is the frequency of the input signal of the RFID transponder. RFID transponders operate with frequencies from kilohertz up to gigahertz, where frequency bands that have been reserved specially for industrial, scientific or medical applications can be used. These are the frequencies classified worldwide as Industrial–Scientific–Medical (ISM) frequency ranges [33]. The multifrequency RFID transponder can operate in the HF band of 13.56 MHz and in the UHF bands at 860 MHz to 960 MHz and at 2.45 GHz.

4.3 Design of the Analog Components

To save area and thus chip costs, the analog building blocks are designed to operate at HF as well as UHF instead of designing separate blocks for the particular frequency range. Nevertheless, some tuning of the blocks for the different operating modes is necessary, although overhead is low. The maximum output power of the reader is limited and the overall efficiency, attributable to the high free space losses in the far field, is bad. To achieve high performance and operating range of the RFID system low power building blocks are developed. Neglecting the antenna gains and the matching considerations, the rectifier's input structure and its overall DC current consumption are the major influences on the performance of an RFID system. Due to different characteristics at HF and UHF, the specifications of the PSU, the data detector and the overvoltage protection circuit differ considerably. Furthermore the clock for the digital core can not be generated using the same principle for both HF and UHF.

Combined RFID transponders for 13.56 MHz, 860 MHz to 960 MHz, and 2.45 GHz are novel. In 2008 a balanced two-pin input structure was presented in [79]. More information about this IC is also available in [80].
In contrast to the work presented in [79], where a balanced rectifier is used for HF and UHF, a new concept was chosen. A balanced HF rectifier and an unbalanced UHF rectifier are combined by a combining device. This rectifier was invented in the author's previous master thesis [94] in 2008. The multifrequency rectifier protected by an overvoltage protection circuit and its verification are published in [99]. In 2009 a three-pin multistandard frontend was developed in [29] (prior work [26]) based on the principle presented in [94]. This three-pin multistandard frontend was then enhanced in [24], [25], and [27].

Designing a circuit that should operate in a wide frequency range makes it difficult to achieve the best performance in the whole frequency range. So the design of the multifrequency frontend leads to a tradeoff between the performance in HF and UHF.

4.3.1 Multifrequency Rectifier Structure

The rectifier, AC/DC converter or PSU converts the incoming RF power into DC power and supplies the whole RFID chip. As explained in Chapter 2, at least the input voltage, the desired output voltage and the expected output load have to be taken into account for the design of the rectifier. All these parameters vary for HF and UHF which leads to different

designs for the rectification at HF and UHF to cope with different input power levels and modulation depths.

4.3.1.1 Design Considerations

A robust communication between the tag and the base station is fundamental for an RFID system. The operating range is also an important quality criterion, especially for UHF RFID transponders. The transponder performs a load modulation to transfer data to the reader. That means the information for the reader can be found in the modulation sidebands, while each sideband contains the same information. As stated in [54], the load modulation sideband amplitude values decoupled at the reader are representative for the tag to reader communication link quality. The higher the delta voltage between unmodulated and modulated state the higher the effective power of the sidebands and thus the efficiency in the uplink case [101].

As introduced in Section 4.2.1 the multifrequency RFID transponder extracts the clock from the 13.56 MHz carrier at HF. That means the modulation index must be lower than 100 % in HF mode, the inputs cannot be shorted like in UHF mode because the input voltage needs to be high enough to extract the clock out of it. This leads to a tradeoff between supply and communication range. In this work a robust communication with the reader at HF is achieved by reaching high delta voltages during load modulation and by an intentional voltage drop from the input to the output of the rectifier. Additionally, thick oxide transistors (with higher V_t) used for the shunt/modulator and the HF rectifier allows an input voltage up to $4\,\mathrm{V_{peak}}$.

In UHF RFID systems the operating range is limited by the supply range. That means the bottleneck is the RF power consumption of the tag and not the backscattered signal to the reader [83]. So the main aim is to lower this power consumption. The lower the minimum input power necessary to operate the chip, the higher the input sensitivity. To achieve a high input sensitivity in UHF mode a voltage multiplier is designed which makes the chip operative from just a few hundred millivolts input voltage. The designed voltage multiplier is based on the principle of a single-ended Greinacher voltage multiplier [36] explained in Section 2.3. The number of stages depends on the characteristics of the CMOS process used on the RF input voltage, the desired DC output voltage and the current consumption of the analog frontend and the digital core. As the rectifier can only be optimized for a small input power and output load range this optimization is done with respect to the chip sensitivity threshold [83].

To increase the performance at UHF, native devices with lower threshold and lower electrical strength can be used because the UHF rectifier is decoupled from the HF input signal. At UHF a high input voltage swing is necessary to improve the RF to DC power conversion. This input voltage swing is limited by the Quality Factor (Q Factor). The higher the frequency the bigger the influences of the parasitic capacitances and thus the lower the Q Factor. A reasonable Q Factor is achieved by keeping the parasitics as small as possible. As explained in Section 2.4.3, there exists a tradeoff between transistor size and parasitic capacitance. Transistors with

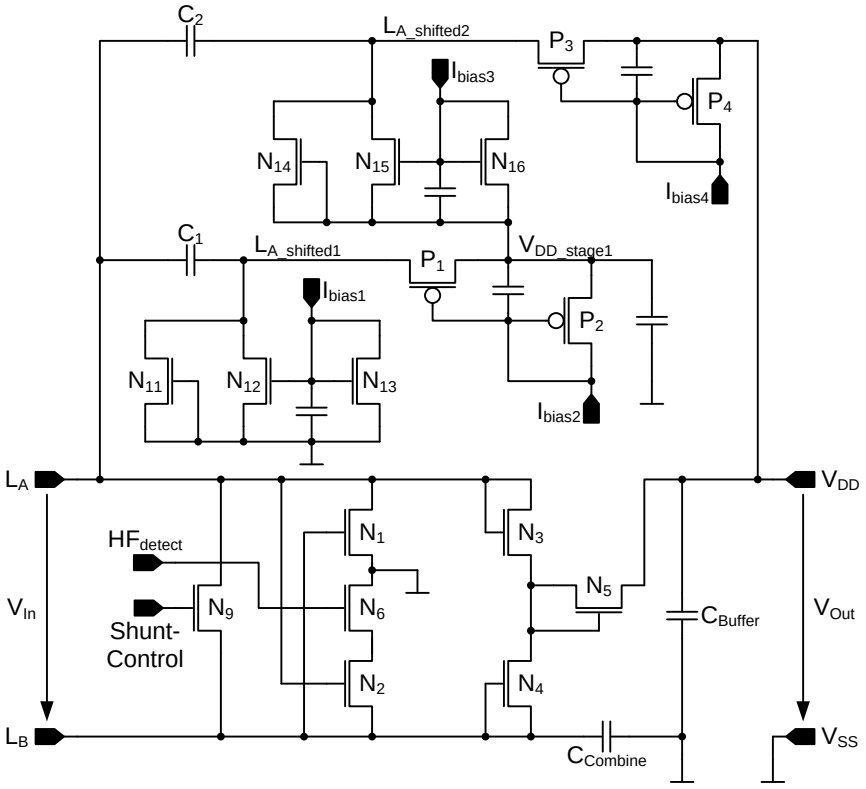


Figure 4.2: Simplified schematic of the multifrequency PSU [99]

smaller geometry have smaller parasitics and therefore lower losses but drive less current to the load. So there is an optimum which is determined by simulations.

The implemented multifrequency rectifier is a combination of a differential HF rectifier and a single-ended UHF rectifier. A big advantage of this combination is the separate optimization of each rectifier. Figure 4.2 shows the multifrequency rectifier. The differential HF rectifier and the single-ended UHF rectifier are combined by the capacitor $C_{combine}$. The value of $C_{combine}$ is 2.5 pF and depends on the frequencies at which the differential or the single-ended rectifier should rectify the input signal.

4.3.1.2 HF Mode

At an input frequency of 13.56 MHz, the multifrequency RFID transponder operates in HF mode. Therefore the rectification of the input signal is done by the differential rectifier, while the four transistors N_1 to N_4 perform the main operation. Since the operating principle, including the current flow and design considerations of a differential rectifier, is already explained in detail in Section 2.2, a brief description of the function of each transistor is given in this section to emphasize some additional functionality that is necessary due to the combination of the differential HF and the single-ended UHF structure.

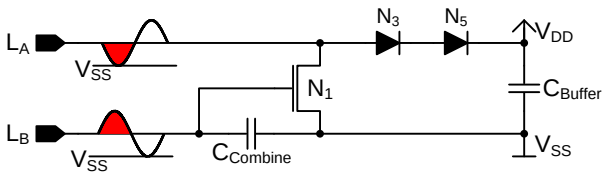


Figure 4.3: Principle of the secondary negative charge pump

Compared to the common structure shown in Section 2.2, one additional transistor is N_6. It is used to raise the performance in UHF mode as explained in the following Section 4.3.1.3. In this mode N_6 is conductive and thus connects the sources of N_1 and N_2 to V_{SS}. N_1 and N_2 are cross-coupled with respect to the input signals and generate the reference V_{SS}. The differential input signal is rectified by the two diode-connected transistors N_3 and N_4, where N_3 rectifies the positive and N_4 the negative half-wave of the input signal, respectively. Accordingly a full-wave rectification is performed. N_5 causes an additional voltage drop of the rectified voltage for the simple reason that the gap between the input peak voltage and the DC supply voltage and thus the quality of the load modulation increases.

The high impedances of $C_{combine}$ and the two coupling capacitors C_1 and C_2 in HF mode protect the UHF path from the high input voltage at the inputs L_A and L_B that is harmful for native devices.

4.3.1.3 UHF Mode

If excited with frequencies from 860 MHz to 960 MHz and at 2.45 GHz, the multifrequency RFID transponder operates in UHF mode. If the multifrequency rectifier is excited with the frequencies specified above the input voltage is too low to operate the HF rectifier in a useful way at low input power levels. Therefore the voltage multiplier shown in the upper section of Figure 4.2 is implemented. Due to the high frequency of the input signal the impedances of $C_{combine}$, C_1 and C_2 are low enough to ensure the operation of the UHF rectifier as a voltage multiplier.

Moreover $C_{combine}$ and N_1 form a secondary charge pump operating at the negative half-wave at the input pin L_A. The resulting secondary charge pump is depicted in Figure 4.3. For this functionality the transistor N_6 is implemented. In UHF mode the signal HF_{detect} is "low" and thus N_6 disconnects the source of N_2 from V_{SS}. Otherwise, during the positive half-wave at the input pin L_A, $C_{combine}$ would be shorted by N_2 and thus the charge stored in $C_{combine}$ would be dissipated because it would be converted into thermal energy.

The common mode potential of L_A and L_B is equal whereas the amplitude of L_A and L_B with reference V_{SS} is divided by the capacitive voltage divider built by the capacitances between L_A and V_{SS} and L_B and V_{SS}. Certainly the HF rectifier is also driven in UHF mode, but at low input power levels the HF rectifier cannot operate due to the low input voltage and so its influence on the chip characteristics is negligible.

As can be seen in Figure 4.2, the UHF rectifier is designed as a two-stage single-ended voltage multiplier based on the Greinacher principle. This voltage multiplier is already explained in Section 2.3 and various analyses are done in Section 2.5.

To decrease the minimum input power in UHF mode even further, a Threshold Voltage Cancellation (VTC) method is used to reduce the forward voltage drop of the diode-connected transistors in the voltage multiplier. Therefore the I-VTC technique presented in Section 2.4.4.2 is adapted as shown in Figure 4.2.
The operating principle can be explained for the first stage: N_{13} is in weak inversion and provides a static bias voltage that is one V_{GS} higher than V_{SS}. V_{GS} of N_{13} is in the range of V_T of N_{12}. Consequently N_{12} is conductive if L_A is lower than V_{SS}. At startup the bias cell is not operating correctly and so the gate of N_{12} is high ohmic and follows $L_{A\_shifted_1}$ due to capacitive coupling until V_{DD} is high enough that N_{13} provides the correct bias voltage. So the gate of N_{12} is lower than V_{SS} at startup. During this phase the diode-connected transistor N_{11} is used to take over the function of N_{12} to enhance the performance of the VTC.

The VTC for the PMOS transistors works according to the same principle. P_2 is also in weak inversion and provides a static bias voltage that is approximately one V_T lower than the node $V_{DD\_stage_1}$. Therefore P_1 is conductive if $L_{A\_shifted_1}$ is higher than $V_{DD\_stage_1}$.

The voltage multiplication can be described as follows: During the negative phase of the input signal the coupling capacitor C_1 is charged by N_{11} and N_{12}. During the positive phase of the input signal P_1 is conductive if the node $L_{A\_shifted_1}$ is one V_T higher than its gate potential and hence rectifies the incoming RF signal. The output of the first stage is pumped to a higher level according to the principle described above.

4.3.2 Combined Shunt and Modulator Block

In state-of-the-art RFID transponders shunt and modulator are two separate devices more often than not to simplify the control circuitry. In this work only one transistor between the input pins is utilized to fulfill HF as well as UHF requirements by keeping the chip sensitivity high. Thus chip area is saved and the parasitics are kept as small as possible. Figure 4.4 presents the combined shunt and modulator block. The NMOS transistor N_9 operates as combined shunt and modulator in UHF mode and as shunt in HF mode. For modulation in HF mode only one additional transistor is used which is located behind the rectification devices and labeled N_{22}. So the big advantage of this method is that N_{22} has only a marginal influence on the chip impedance. The combined shunt and modulator block includes circuits for generating the sensing voltages in HF and UHF mode and a regulation scheme that controls the gate of the combined shunt and modulation transistor.

4.3.2.1 Generation of the Sensing Voltages

To ensure that no device destructive voltage occurs, the sensing voltages are simultaneously generated by both the HF and UHF rectification path. V_{DD} is limited to a maximum of 1.1 V so that overshoots can not destroy the used low voltage devices. The loads of the V_{DD} sensing

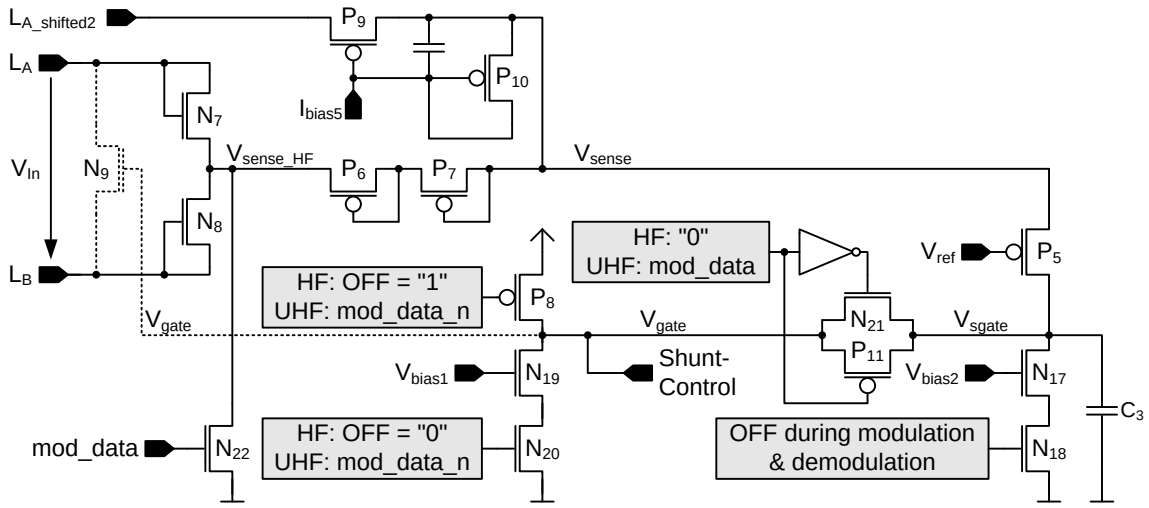


Figure 4.4: Combined shunt and modulator module for HF and UHF

circuits should be very low to make these circuits very sensitive to changes of the RF input signal. For that reason loads of only about 150 nA are chosen to ensure a fast reaction. The diode-connected transistors N_7 and N_8 generate the sense voltage V_{sense_HF} dedicated for HF mode.

In UHF mode a sensing voltage that is decoupled from the DC load has to be generated. This is solved by applying a separate peak detector (see Section 2.3) which is connected to the node $L_{A\_shifted_2}$ of the second stage of the voltage multiplier. This peak detector is formed by P_9, P_{10}, and a buffer capacitor. Because the same VTC method as applied at the voltage multiplier is utilized, P_{10} is diode-connected and biases P_9, which generates the sensing voltage V_{sense} in UHF mode. In UHF mode the sensing voltage generated by P_9 is higher than V_{sense_HF}. In HF mode V_{sense_HF} is higher than V_{sense}. Furthermore, the outputs of the sensing circuits are not equal at a distinct V_{DD} due to the different rectification techniques in HF and UHF mode. To use the same reference voltage of the pass device V_{sense_HF} is decreased by two diode voltages and connected to V_{sense}. V_{sense} is the input of the pass device P_5 which controls the voltage V_{sgate}. If V_{sense} rises, the current through P_5 increases according to its gm. So the capacitor C_3 is charged very quickly and the potential V_{sgate} increases with the RF input signal.

4.3.2.2 The Control of the Shunt/Modulator

The control of the shunt/modulator is different for HF and UHF mode. In HF mode N_9 is used as shunt to dissipate the excessive power and the additional transistor N_{22} is used to draw additional current from the node V_{sense_HF} to V_{SS} during the high cycle of the modulation pulse (mod_data = "1"). The RF input signal is thus lowered during the high cycle of the modulation pulse and so load modulation is implemented. As obvious from Figure 4.4 at modulation in HF

mode the amplitude of the input signal is approximately a threshold plus a saturation voltage. This enables the extraction of the clock by the clock recovery.

In HF mode the current sinks N_{17} and the capacitor C_3 are used to define the time constant for the shunt operation (performed by N_9), whereas in UHF mode a different time constant is defined by the additional current sink N_{19}.

Before the modulation starts, the voltage stored in C_3 is that voltage necessary at the gate of N_9 to ensure correct overvoltage protection and supply voltage for the chip. For that reason the same voltage has to be applied to the gate when the modulation is finished. That means the voltage stored in C_3 has to be kept at approximately the same level during modulation, and so N_{17} is switched off by N_{18} to freeze V_{sgate} during data receiving and modulation or backscattering. Furthermore, a T-Gate formed by the transistors N_{21} and P_8 is implemented which decouples V_{sgate} from V_{gate} during the high cycle of the modulation pulse in UHF mode. In all other states the T-Gate is conductive. This decoupling is necessary because otherwise C_3 would be charged to V_{DD} in UHF mode if mod_data = "1" and and thus the gate of N_9 would still be at V_{DD} if mod_data returns to "low". In this case too much power would be dissipated in N_9 and V_{DD} would decrease even more, and the chip would run in a deadlock.

In HF mode P_9 and N_{20} are switched off and so is the current sink N_{19}. In UHF mode P_9 pulls the potential V_{gate} to V_{DD} if mod_data = "1" to short the two input pins L_A and L_B. N_{20} enables the current sink N_{19} during the low cycle of the modulation pulse ($mod\_data = 0$) in UHF mode to discharge the parasitic capacitances. Simultaneously the T-Gate closes and so the former V_{sgate} is restored at the gate of the shunt transistor N_9 (potential V_{gate}). Due to the fact that the shunt/modulator changes its resistance during operation the chip impedance is transformed, which results in a mismatch between antenna and chip. So the shunt operation is performed in two steps: First, the incoming RF power is lowered due to the mismatch and second, the excessive input energy is transformed into thermal energy.

4.3.3 Demodulator

The data transmission should not be the limiting factor in an RFID system, therefore the demodulator must operate at low input power levels (worst case behavior). As for the shunt and modulator, the demodulator is also combined for HF and UHF. The data detection is done by comparing the moving average of the input signal to the envelope of the input signal. Figure 4.5 shows the simplified schematic of the demodulator. The envelope detector works by exploiting the principle of a single-ended one-stage voltage multiplier using the VTC scheme. As long as the RF input signal is not modulated the moving average value is approximately one threshold voltage below the envelope value.

The envelope signal equals the output of this voltage multiplier and is buffered with only 100 fF (C_3) in UHF mode and with 200 fF in HF mode. Therefore N_3 is used, which is conductive in HF mode and thus switches C_4 in parallel to C_3. The moving average signal equals the gate potential of the rectifying transistor P_1 and is buffered by the capacitor C_5. The time constants for correct operation are defined by the current sources N_4 and N_5 and the capacitors C_3 and

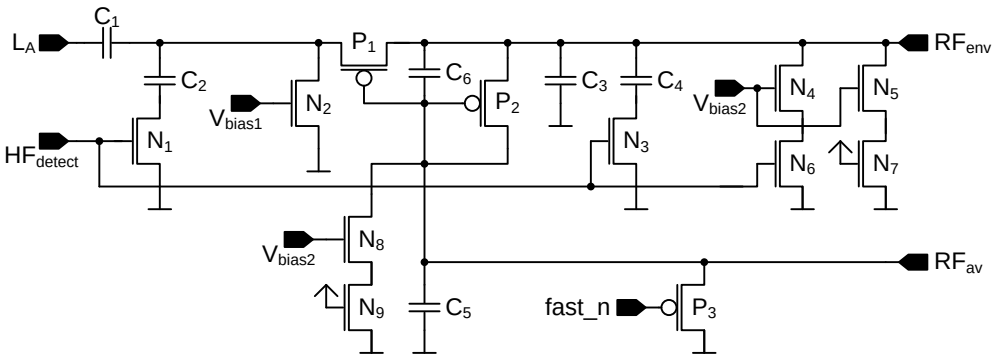


Figure 4.5: Combined demodulator module for HF and UHF

C_4 for the envelope signal in HF mode. In UHF mode N_3 and N_6 are non-conductive, thus the time constant for the envelope signal is defined only by N_5 and C_3. The current sink N_8 and the capacitor C_5 define the time constant for the moving average signal, independent of the operating mode. N_7 and N_9 function as switches that are conductive during normal operation and are used for better matching of the current sinks N_4, N_5, and N_8 by providing nearly the same source potentials.

During the startup phase P_3 draws additional current from the node RF_{av} to V_{SS} to prevent false demodulation data till the voltage limiter is settled. Due to the fact that the envelope signal has to follow the RF input signal much faster than the moving average signal, the current sink at RF_{av} is weaker and the value of the buffer capacitor is bigger.

The demodulator is also designed using thin oxide transistors. Therefore a capacitive voltage divider is implemented which is activated in HF mode. If HF_{detect} = "1", the transistor N_1 is conductive and the voltage divider with a ratio of 1:1 is activated to prevent circuit destructive voltages. Due to the different timing constants in HF and UHF mode the current drawn by the current sink operating at RF_{env} also varies. The envelope signal and the moving average signal are then fed into a comparator with a bias current of 100 nA. The output of this comparator is the demodulated signal and is only enabled if the digital core is in data receiving mode to reduce the average power consumption of the chip.

4.3.4 Frequency Detection Unit

Circuitry is needed to detect the frequency range at which the chip is excited, because the analog blocks as well as the digital core have to operate differently in HF and UHF mode. The information if the tag is operating in HF or UHF mode is important to tune, select, enable or disable some of the analog blocks and to set the digital core to the correct standard (mode). The frequency detection can be easily performed by the circuit shown in Figure 4.6, which includes a lowpass filter the cutoff frequency of which is set to approximately 30 MHz ($R_1 = 100\,\mathrm{k\Omega}$, $C_1 = 50\,\mathrm{fF}$).

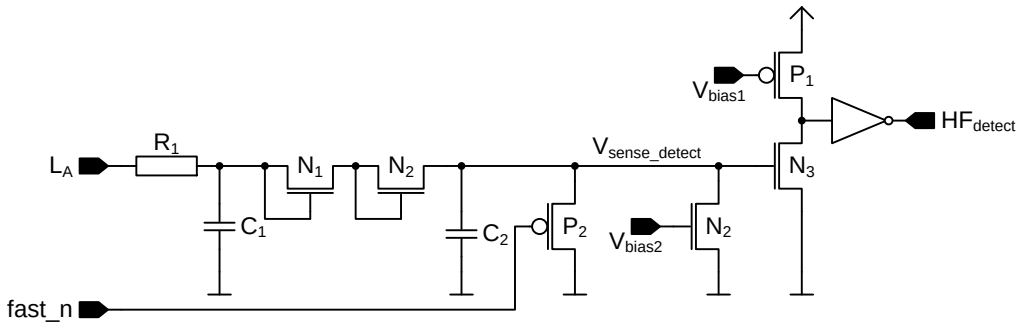


Figure 4.6: Frequency Detection Unit

As explained in Section 4.3.1, the rectifier performs a level shift on the inputs L_A and L_B in UHF mode. The output of the low pass filter is the average DC value of the input voltage at L_A with reference V_{SS}. To avoid a wrong decision at high input voltages in UHF mode, the two diode-connected NMOS transistors N_1 and N_2 are added to lower the DC potential, because in UHF mode $C_{combine}$ performs a DC level shift. In HF mode the amplitude of the AC input signal is much higher than in UHF mode. So the voltage drop caused by the two diode-connected NMOS transistors has no effect in HF mode. The time constant of the node V_{sense_detect} is defined by the current sink N_4 and the capacitor C_2.

Due to the fact that during the startup phase V_{sense_detect} could achieve too high levels, P_2 draws additional current so that the frequency detection operates reliably until the system is settled. The lowpass output lowered by two diode voltages (V_{sense_detect}) is then connected to the gate of N_3. P_1 and N_3 form a current starved inverter to limit the cross current caused by the usually slow slope of V_{sense_detect}. Of course, the output of this current starved inverter has to be buffered. If V_{sense_detect} is higher than the threshold of N_3 the HF mode is detected. Conversely, the tag is operating in UHF mode. As can be seen from Figure 4.6 the chip will start in UHF mode as HF_{detect} is "low" during startup independent of the input frequency.

4.3.5 Clock Recovery

In HF mode the clock signal is extracted from the carrier by the simplified circuit shown in Figure 4.7 to achieve a clock for the digital core that is associated with the frequency of the RF input signal. This principle is usually utilized due to the sufficiently available DC power in HF mode and the absolute timing values defined in the ISO/IEC 14443 [45] and the ISO/IEC 15693 [46] protocols. The extracted clock is then divided by a factor of eight and fed into the digital core.

The circuit works as follows: The input signal L_A is fed to the source of N_3. The two PMOS transistors P_1 and P_2 operate as current sources. The two diode-connected NMOS transistors N_1 and N_2 bias the gate of N_3 at two threshold voltages. N_3 is switched on as long as the

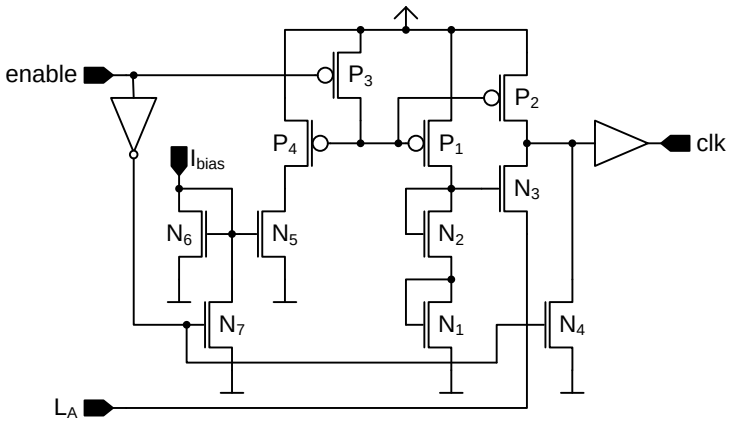


Figure 4.7: Clock Recovery for HF mode

input is lower than one threshold voltage and thus the node *clk* is at V_{SS}. When the input signal L_A achieves at least a threshold voltage, N_3 is switched off and the current source P_2 pulls the node *clk* to V_{DD}. So the clock for the digital core is extracted. The transistors P_3, N_4 and N_7 are used for power gating. To define the input of the buffer, the node *clk* is pulled to V_{SS} if the input *enable* is "low".

4.3.6 Local Oscillator

In UHF mode, the available DC power is usually lower than in HF mode. Therefore the generation of the clock signal has to be power efficient. Dividing 900 MHz or even 2.45 GHz down to approximately 2 MHz to clock the digital core is ineffective, first because it consumes a great deal of energy, and second due to the fact that the clock recovery designed for HF mode cannot be used for a modulation index up to 100 %. Relaxed timing constraints allow the implementation of a local relaxation oscillator based on the principle published in [79].

The frequency must be high enough to meet the specifications of the EPC Gen 2 standard [22] but should not be too high, because the faster the oscillator the higher the current consumption of the oscillator itself and the digital core. As explained in [43], the minimum clock frequency has to be 1.92 MHz. The frequency of the relaxation oscillator shown in Figure 4.8 is defined by a poly resistor and a Metal-Insulator-Metal (MIM) capacitor.

The circuit operates by the principle of charging and discharging a capacitor with the same current. The voltage at the positive node of the capacitor is then fed to a common source amplifier that is acting as current comparator.

The output signal *clk* of the relaxation oscillator is connected to the gates of P_3, N_3, and N_8. At startup *clk* is at V_{SS} and therefore C_1 is charged by P_3 and P_4. The node $V_{compare}$ follows V_{DD} up to the voltage defined by the diode-connected transistor N_6. The higher the gate

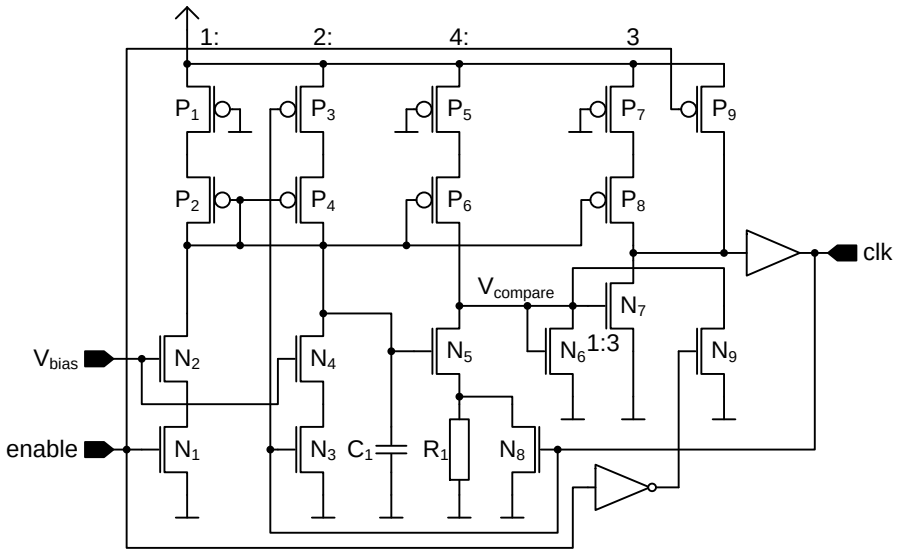


Figure 4.8: Relaxation oscillator for UHF mode

potential of N_5 the more it conducts. Therefore, the current through N_5 and R_1 increases as long as the current through N_5 is higher than the current provided by the current source P_6. So the node $V_{compare}$ is discharged with a current limited by R_1. N_8 is non-conductive until the current comparator P_8/N_7 toggles. As a consequence the node *clk* is pulled to V_{DD}, thus the switches N_3 and N_8 close and the source of N_5 is pulled to V_{SS}. The gate of N_5 is still high enough that the node $V_{compare}$ is discharged to V_{SS}. Simultaneously the current sink N_4 discharges C_1 as long as the current through N_5 is lower than the current through P_6. That means $V_{compare}$ rises again, the current comparator toggles, the node *clk* is pulled to V_{SS} again and the procedure starts from the beginning.

The local oscillator operates from a supply voltage of approximately 600 mV. The current consumption is 1.3 µA at 1 V. The output frequency as a function of supply voltage at different temperatures is shown in Figure 4.9. The maximum frequency variation at worst case (fast 125 °C) is 624 kHz between 0.6 V and 1.6 V. This frequency variation is mainly caused by the bias current variation due to V_{DD} changes and the transistor N_7 of the current comparator. As can be seen from Figure 4.9, the frequency dependency over temperature is small. For the operation in the RFID chip the frequency variation of the oscillator is only important during communication. During this short duration the temperature changes are negligibly small, and the V_{DD} variation is small enough that the frequency variation of the oscillator fulfills the requirements stated in [22]. Depending on TRcal and the link frequency (see [22]), the frequency tolerance is allowed to be between ±22 % and ±2.5 %.

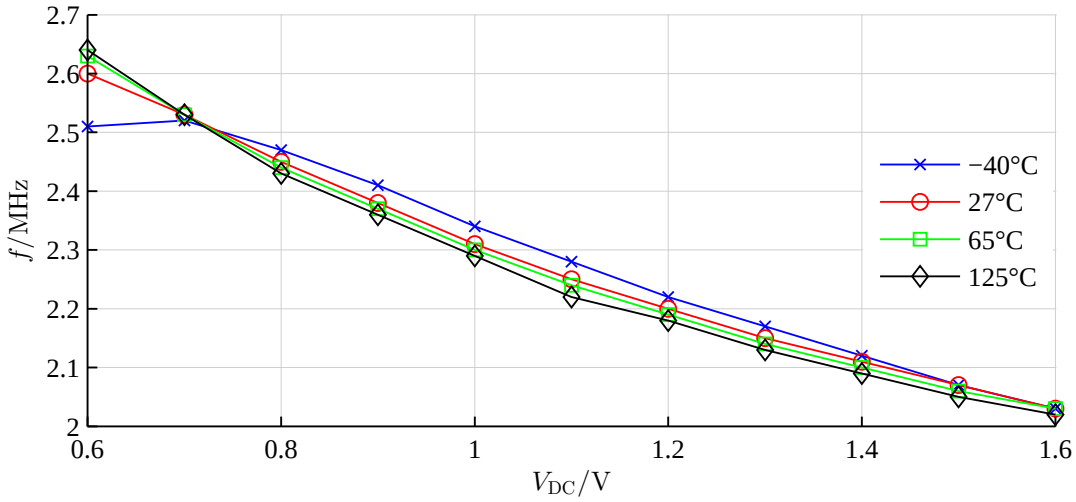


Figure 4.9: Simulated output frequency of the relaxation oscillator over supply voltage at different temperatures

4.3.7 Clock Control Unit

During power up the frequency detection unit detects the operation mode (HF or UHF). The signal HF_{detect} is latched in the digital core only after the $resetn$ signal, which is generated by the power-on reset block, switches to "high" ($resetn = 1$). Depending on the signal HF_{detect}, either the clock from the local oscillator ($HF_{detect} = 0$) or the clock extracted by the clock recovery ($HF_{detect} = 1$) is fed to the digital core. As explained in Section 4.3.4, $HF_{detect} = 0$ at startup. Thus the clock recovery is disabled and does not draw current from the supply during startup which is necessary to achieve a high input sensitivity in UHF mode.

4.4 Experimental Results

This section discusses the measurement results of the multifrequency passive RFID tag using the concept of combining a single-ended and a differential rectifier. The tag is measured at HF as well as at UHF, while the input sensitivity at UHF is compared to recent publications and state-of-the-art products operating at the mainstream frequency ($f \approx 900\,\text{MHz}$) of passive RFID systems.

4.4.1 HF Measurements

The minimum field strength H_{min}, which is one of the key parameters of passive HF RFID transponders, is determined by using the measurement setup and method described in Section 2.7.1. A correct chip response was detected down to 48.5 mV measured as a peak to peak

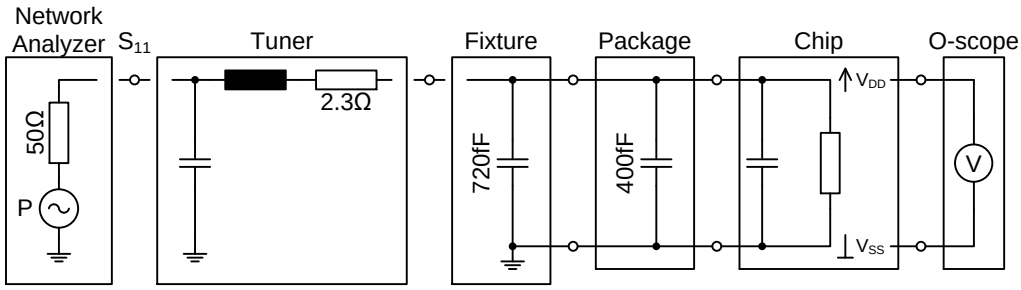


Figure 4.10: Contact-based measurement setup for UHF

value with the sense coil shown in Section 2.7.1. This results in a field strength of $53\,\mathrm{mA\,m^{-1}}$ using (2.7.5) on page 65.

4.4.2 UHF Measurements

The input sensitivity in UHF mode is determined by using the contact-based setup shown in Figure 4.10. The measurement principle, which uses a network analyzer as power source and a tuner to ensure matching, is already explained in Section 2.7.2.3. As stated in Section 2.7.2, a suitable method to determine whether the tag operates or not is necessary.

The input power necessary to turn on the tag need not be the same as to process an inventory command. During communication from the reader to the transponder less power is transmitted to the chip due to ASK modulation. In addition, if the chip communicates with the reader by backscattering the emitted RF signal, no RF power can be converted into DC because the two input pins are shorted. For these reasons, a higher input power is necessary to process a command. Thus, the input sensitivity is determined when the chip responds to the reader. In addition to the measurement devices used in Section 2.7.2.3 a signal generator is utilized.

The measurement procedure can be explained as follows:
Again the same package and test fixture as introduced in Section 2.7.2.1 are utilized to connect the chip to the tuner. At first the Device Under Test (DUT) is matched to the network analyzer at $V_{DD} = 1\,\mathrm{V}$. The reflection coefficient is thus very small, almost no power is reflected to the measurement device and so acceptable measurement results are achieved. Then the matched DUT is disconnected from the network analyzer and connected to the signal generator which powers the chip. The chip is excited with the inventory command (query) and replies by backscattering the emitted RF signal. By observing the supply voltage it can be determined if the chip responds or not. The RF output power of the signal generator is lowered as long as the chip responds correctly. During this process the chip always has to be matched as well as possible. Observing the output voltage while the tuner parameters are changed is usually sufficient.

The input sensitivity is determined to be $-11.4\,\mathrm{dBm}$ (worst case) at a frequency of $868\,\mathrm{MHz}$, neglecting all losses produced by the measurement setup. Using the method explained in

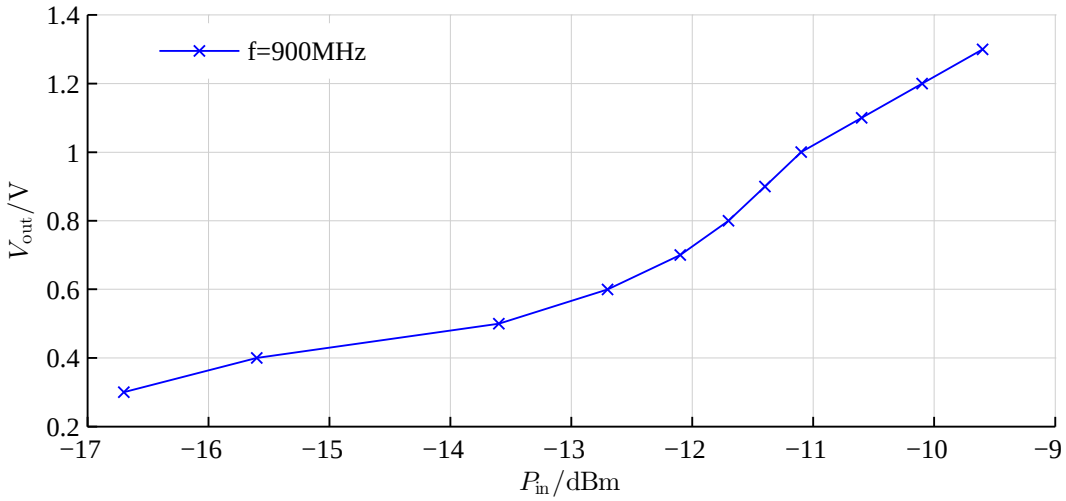


Figure 4.11: Measured VP-characteristic of the multifrequency rectifier

Section 2.7.2.3, the losses caused by the matching circuit can be calculated to be 2.1 dB. This leads to a corrected input sensitivity of −13.5 dBm.

4.4.3 PSU Measurements

The overall current consumption of the multifrequency RFID transponder is approximately 4.1 µA at $V_{DD} = 0.9$ V in UHF mode. Figure 4.11 shows the DC output voltage of the rectifier versus the RF input power measured at 900 MHz and loaded with the analog frontend and the digital core (4.1 µA at $V_{DD} = 1$ V). As can be seen in Figure 4.11 and 4.12, the chip is operative from 0.9 V. The values in the graph are not corrected by the losses of the measurement system. During data transmission the supply voltage can decrease down to approximately 0.5 V, as can be seen in Figure 4.12.

4.4.4 Transient Behavior

Figure 4.12 shows the measured transient behavior of the chip during one inventory command. The upper curve depicts the baseband signal of the signal generator. The inventory command sequence stored in the signal generator is modulated with the 868 MHz carrier. The lower curve depicts the supply voltage of the transponder. As can be seen, the command from the reader as well as the chip's response are clearly evident in the supply voltage. During the query command less power is transmitted to the chip due to ASK modulation. The higher the modulation index the lower the power that can be converted into DC. A modulation index of 100 % was chosen for this measurement. Furthermore, the chip is not perfectly matched during modulation, because the matching is done when the chip is excited with the unmodulated carrier. These are the two major reasons why the supply voltage of the transponder decreases during the query command.

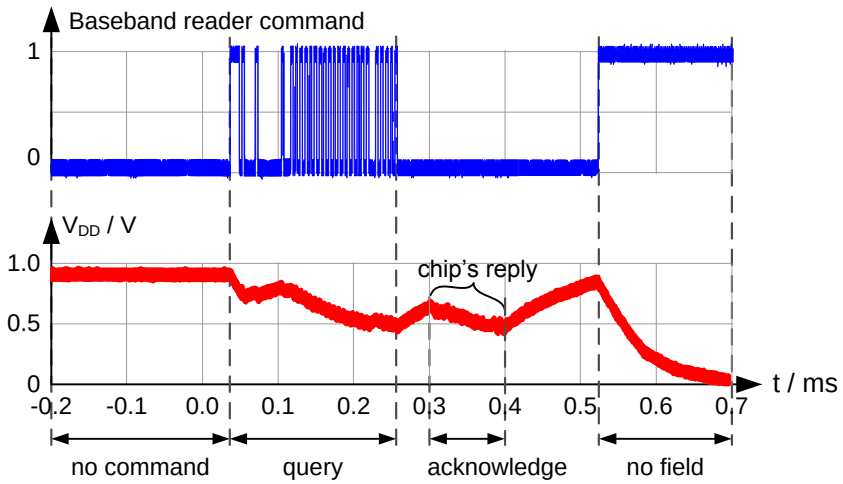


Figure 4.12: Transient behavior of the chip during one inventory command

A similar behavior can be observed when the chip responds. As already explained, the communication from the chip to the reader is performed by backscattering the emitted reader signal. This is done by shorting the two input pins. While the input pins are shorted no RF power can be converted into DC, and therefore the supply voltage decreases too. Measurements have shown that the lack of energy is during the chip's response.

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Chip	Technology	Area	Frequency	Sensitivity	Type
this work	0.13 µm	0.39 mm^2	13.56 MHz, 860 MHz to 2.45 GHz	53 mA/m, −13.5 dBm @ 0.9 V/4.1 µA	EPC HF & Class 1 Gen 2 UHF RFID
[107, 108] by T. Umeda	0.30 µm	0.64 mm^2	950 MHz	−11.0 dBm @ 1.0 V/3 µA	6-stage se. rectifier
[115] by Y. Yao	0.35 µm zero Vth	0.38 mm^2	900 MHz	−14.7 dBm @ 2.1 µW	RFID frontend
[32] by T. Feldengut	0.35 µm Schottky	–	868 MHz	−11.3 dBm @ 1.5 V/5.0 µA	6- & 8-stage rectifier
[117] by J. Yi	0.18 µm zero Vth	0.24 mm^2	900 MHz	−11.1 dBm @ 1.0 V/5.2 µA	24-stage rectifier
[5] by R. Barnett	0.13 µm	0.55 mm^2	860 MHz to 960 MHz	−14.0 dBm	EPC Class 1 Gen 2 RFID
[27] by J. Essel	0.13 µm	–	13.56 MHz, 860 MHz to 960 MHz	−4.0 dBm(HF), −11.0 dBm @ 1.0 V/10 µA	HF & HF rectifier

Table 4.1: Comparison with state of the art

4.4.5 Comparison with State of the Art

Several publications deal with rectifiers for RFID transponders, frontends for RFID transponders, and RFID transponders themselves. Table 4.1 shows a comparison with some state-of-the-art publications, while different process technologies are considered. The performance of an RFID transponder depends on all building blocks. Assuming that the sensitivities of the modulator and demodulator are sufficient, the performance depends mainly on the power consumption of the building blocks and the rectifier characteristics.

Unfortunately a power breakdown is not available in [5] which uses a six-stage voltage multiplier for supply generation in a standard CMOS process. As the tag is EPC Class 1 Gen 2 compatible it can be assumed that the DC power is similar to this work.
In [115] an RFID frontend is presented which is built with zero threshold transistors and consumes 2.1 µW. Thus it can be assumed that the input sensitivity decreases if a digital core is supplied too.
The six-stage single-ended voltage multiplier presented in [107, 108] is also included in this comparison because the measurements done in [108] comprise also the load range of an RFID transponder or frontend.
In [32] a secondary rectifier consisting of an eight-stage Schottky diode rectifier generates the compensating voltages for the main rectifier which is a six-stage transistor-based rectifier. Considering the input sensitivity, which is moreover just a simulation value, this overhead and complexity of design do not pay off.

The triple output rectifier presented in [117] is also built with zero threshold transistors. The output voltage of 1.0 V is generated by the 14^{th} stage of the 24-stage voltage multiplier and is used to power the RF frontend. This output is loaded with 200 kΩ and thus fits for the comparison with this work.
An RFID rectifier that is capable of HF as well as UHF is presented in [27]. It is assumed that the complete RFID chip will consume 10 µW. In contrast to this work three input pins instead of two are necessary to connect a combined HF and UHF antenna.

This work was implemented in a low-cost process. The chip size is small compared to the other publications despite the two additional pads for test purposes and the fixed layout size. The achieved input sensitivity in UHF mode is comparable to state-of-the-art stand-alone UHF designs as shown in Table 4.1 despite the combination of HF and UHF.

4.5 Conclusion

This chapter presented a multifrequency passive RFID chip supporting both the EPC HF and the EPC Class 1 Gen 2 UHF standard. The PSU operates from a few hertz up to several gigahertz with optimization for HF (13.56 MHz) and UHF (860 MHz to 960 MHz and 2.45 GHz). The chip can be used as a stand-alone HF or UHF transponder and as a combined HF & UHF transponder.

Novel concepts for shunt, modulator, demodulator, and frequency detection circuitry enable an area- and cost-saving chip design. The combination of the shunt and modulator lowers the losses and thus increases the input sensitivity and the operating range. Furthermore, this design makes it possible for only two input pins to be necessary to connect the chip to an antenna that can but need not be broadband. Due to supporting the commercial RFID standards, state-of-the-art RFID readers can be used to operate the multifrequency RFID chip, which enables an easy integration in existing RFID systems.

High operating ranges at UHF are achieved by ultra low power design of the analog building blocks. Bias currents between ten and 50 nanoampere are chosen which are generated by a Delta-Vth-Biasing circuit to minimize the current consumption. To keep the influence on the chip impedance and input sensitivity low, only one transistor between the input pins is utilized to fulfill HF and UHF requirements. Additionally the modulation in HF mode is performed on the DC side. All these design steps result in an input sensitivity of −13.5 dBm in UHF mode. This value considers the measurement losses calculated to be 2.1 dB and is in the range of state-of-the-art RFID transponders despite the combination of HF and UHF. Using separate rectifiers with a differential input structure for HF built with thick oxide transistors with high electrical strength and a single-ended input structure for UHF designed with native devices enables universal applicabilities and enhancements of the developed chip.

Chapter 5

The Multifrequency Sensing Tag

The original publications related to this chapter are [98, 100] (own publications). ■

Low cost, small size and weight, batteryless operation, and maintenance friendliness are among others reasons why passive Radio Frequency Identification (RFID) tags have attracted increasing attention. State-of-the-art passive RFID tags are limited in terms of functionality and operating range due to the limited power that can be converted from the electromagnetic field. That is the reason why state-of-the-art Wireless Sensor Nodes (WSNs) are mostly battery-based if a high operating range and/or complex functionalities are required. Nevertheless, there is growing interest in enhancing this technology with sensor functionality. Equipping sensor nodes with RFID functionality not only enables identification and logistic applications but also an easy integration of the sensing tag into existing RFID systems. Regarding the reasons explained in Section 4.1 the proposed multifrequency sensing tag is also capable of both HF and UHF, which are the mainstream frequencies in passive RFID systems.

5.1 Enhancing Passive RFID Tags with Sensor Functionality

The most commonly used passive RFID systems are HF RFID systems operating at 13.56 MHz and UHF RFID systems operating at a frequency range from 860 MHz to 960 MHz and at 2.45 GHz.
HF RFID systems, working in the near field, have a typical working range from several centimeters to about only one meter, but provide sufficient power at the tag to supply power hungry sensors [33, 50].

UHF RFID systems, working in the far field, have a larger working range of up to several meters [88]. The higher the distance between the base station and the tag the lower the power that can be converted from the electro-magnetic field.
The Friis transmission equation (see (2.4.9) on page 23), which is valid for free space and does not consider influences of the environment in which the systems operate, is used to calculate the power available at the tag P_r depending on the distance R and the power delivered to the transmitting antenna (matched case) P_t. Assuming that the base station emits 4 W (maximum power allowed by national regulations) Effective Isotropically Radiated Power (EIRP) in the UHF frequency band at 900 MHz, the output power that can be converted from the electromagnetic field is not sufficient to supply devices with a power consumption in the milliwatt

range (for example pressure sensors) in a useful operating distance. For example, at a distance R of 5 m an input power of only 113 µW can be received. This RF input power P_r has to be multiplied with the Power Conversion Efficiency (PCE) of the Power Scavenging Unit (PSU), then the power consumption of the chip itself (biasing, controlling,...) has to be subtracted and the resulting reduced power is the power available for the sensing operation as shown in (5.1.1)).

$$P_{Sensor} = P_r \cdot PCE_{PSU} - P_{Chip} \tag{5.1.1}$$

So it seems to be impossible to develop a remotely powered sensor node which achieves a high operating distance, but this chapter proposes two ways to get around this problem:

1. If the current consumption of the sensor itself is in the lower microwatt range the sensor unit has to be designed to consume as little power as possible. So the sensor and the control unit can be supplied directly by the RFID tag.
2. If the power consumption of the sensor itself is higher than the DC power that can be converted from the RF source in the desired operating distance, a circuit harvests the energy and stores it in an energy reservoir. This energy is then used to supply the sensor block. That means the sensor block is supplied periodically. The harvesting circuit mentioned above is based on the second subsystem of the Electro-Magnetic Energy Harvester (EMH) explained in Chapter 3.

The proper way should be selected depending on the sensor type, especially on the power consumption of the sensor.

5.2 System Description

The sensing tag is usable as a WSN, especially under those conditions where batteries cannot be replaced or where it is not possible to supply the sensor system by wire or by thermal or photovoltaic energy harvesting. To be very flexible the proposed sensing tag is operable at 13.56 MHz and 860 MHz to 2.45 GHz. It is EPC HF [23] and EPC Class 1 Gen 2 UHF [22] compatible and contains an on-chip temperature sensor and an interface for external sensors or related devices with a power consumption up to the milliwatt range.

This section begins with a list of the required design specifications, followed by the system architecture which is explained by means of the block diagram. Then the typical system characteristics are listed.

5.2.1 Design Specifications

- The chip is capable of frequencies from 13 MHz up to 2.45 GHz to be operable in HF RFID systems at 13.56 MHz and in UHF RFID systems in the frequency band from 860 MHz to 960 MHz and at 2.45 GHz to enable worldwide identification with only one chip.

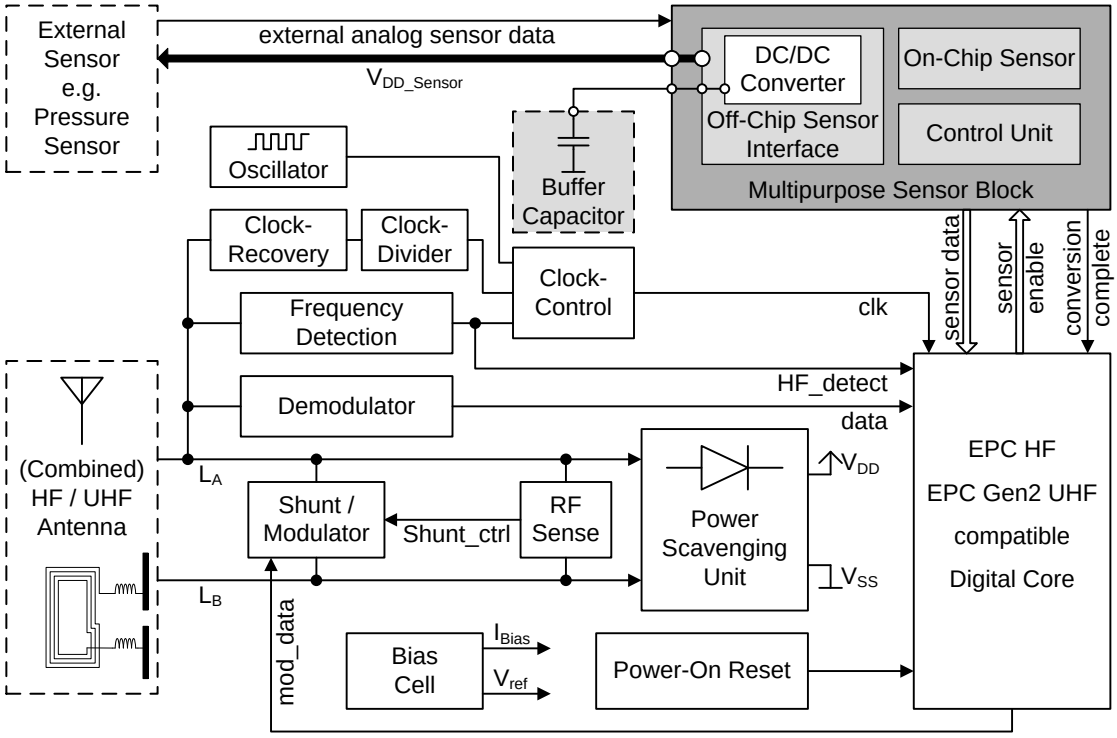


Figure 5.1: System architecture of the remotely powered multifrequency sensing tag

- To keep the chip costs small only two interface pins to connect the antenna are available. Therefore only one analog frontend can be used, which is capable of both HF and UHF.

- To also fulfill the ISO 14443 [45] and ISO 15693 [46] standards the chip has to be operative if an unmodulated field of 150 mA m^{-1} or less is applied. Nevertheless the standard used in HF mode is the EPC HF version 2 [23].

- The off-chip sensor interface is able to deliver an output power up to the milliwatt range for a few microseconds.

- To keep the external buffer capacitor at a useful size the off-chip sensor interface is first enabled at 3 V and disabled at 1 V.

- If used as a wireless temperature sensor the on-chip temperature sensor is operative at a supply voltage of 1 V and its current consumption is lower than 5 µA to reach a practicable operating distance. (The lower the DC power the lower the necessary input power and thus the higher the operating distance.)

- The proposed passive sensing tag is designed for maximum input sensitivity in UHF mode. The maximum input power is allowed to be 10 dBm.

5.2.2 System Architecture

This section explains the operating principle of the multifrequency sensing tag mainly consisting of the blocks shown in Figure 5.1. The chip is connected to an antenna that can but need not be a combined antenna for HF and UHF as developed in [76] via two interface pins to the input pins L_A and L_B. As can be seen from Figure 5.1 the blockdiagram looks similar to the blockdiagram of the multifrequency RFID transponder presented in Chapter 4. It was possible to reuse the frequency detection unit, the clock recovery, the clock divider, the local oscillator and the clock control unit. The digital core was adapted to process the data from the multipurpose sensor block, which is the enhancement of a common RFID transponder. Further necessary modifications have to be made on the PSU, the shunt, the modulator, and the demodulator. As already stated in Chapter 4, two different solutions of a multifrequency frontend for RFID transponders are presented in this thesis. In contrast to state-of-the-art RFID transponders as presented in [2, 5, 17, 32, 81, 106, 115] and in contrast to the implementation of the multifrequency rectifier in Section 4.3.1, a different approach is used. Instead of a combined balanced HF rectifier and an unbalanced UHF rectifier a balanced rectifier is designed which operates in the HF as well as UHF frequency range. The background of this decision is explained in Section 5.3.1.

5.2.2.1 Operating Principle of the RFID Functionality

The operating principle of the RFID functionality of the multifrequency sensing tag is nearly identical with that of the multifrequency tag presented in Chapter 4. For the sake of completeness it is also explained briefly in this paragraph.
The AC/DC converter or so called PSU rectifies the impinging RF signal and supplies the chip with power. Shunt and modulator are combined in one device and controlled by the RF sense block and the digital core. The shunt protects the chip against overvoltage. A frequency detection unit distinguishes between HF (13.56 MHz) and UHF (860 MHz to 2.45 GHz) mode, controls some blocks and sets additional parameters. The modulated data emitted by the RFID reader is translated into digital values by the demodulator and processed in the digital core. The power-on reset prevents erroneous signals from the digital core. The clock-generation block includes a clock recovery and a local oscillator and clocks the digital core and the multipurpose sensor block.

5.2.2.2 Operating Principle of the Multipurpose Sensor Block

The multipurpose sensor block includes the on-chip temperature sensor and the off-chip sensor interface where a DC/DC charge pump is used to pump the output voltage of the AC/DC rectifier up to 3 V and charge the buffer capacitor C_{Buffer}. Depending on the amount of energy that is needed by the connected device for one operation cycle, this buffer capacitor can be either internal or external. A separate control unit selects the dedicated sensors and controls the operating sequences. The analog measurement signals are converted into digital data. Due to the fact that the on-chip sensor as well as the off-chip sensor interface can be used and

thus can provide analog data, the converted digital data are stored in different memory banks. Via different EPC read commands, according to the EPC HF [23] or the EPC Class 1 Gen 2 UHF [22] standard, the data are read out.

5.2.3 Matching Considerations

The greatly different chip input impedances yield different antenna impedances at HF and UHF. If the transponder should be operative at HF as well as UHF with the same configuration, a combined HF and UHF antenna is needed that has different impedances and behavior at HF and UHF.

At HF the optimization criterion for the antenna is to deliver maximum voltage to the chip input. For maximum chip input voltage it is advantageous to create a parallel resonant circuit that consists of the transponder antenna coil, the input impedance of the chip and an additional capacitance that tunes the resonant frequency to 13.56 MHz. The voltage step-up of this circuit allows to significantly improve the read range of HF transponders [69].

The better the matching between the antenna and the chip the more power is delivered to the chip input at UHF. The maximum power can be picked up from the electro-magnetic field in the case of conjugate matching ($\underline{Z}_{Chip} = \underline{Z}^*_{Antenna}$). The bandwidth of the UHF antenna should be sufficient to operate in the frequency bands used in different countries. In the 900 MHz frequency band frequencies from 860 MHz to 960 MHz are possible. This bandwidth limits the Quality Factor (Q Factor) of the antenna. The matching has to be done for that mode in which the highest input sensitivity is desired. For the measurements the chip is matched in UHF EPC only mode.

5.2.4 System Characteristics

To simplify the following considerations and explanations, some characteristics are defined in this section.

Input Sensitivity – Minimum Input Power

Of course, the input sensitivity is defined identically as in Section 2.1.1, 3.3.3, and 4.2.3. The multifrequency sensing tag has different input sensitivities depending on the desired operation mode. The input sensitivity refers to the point where the chip is able to supply the selected blocks and communicate with the base station.

HF Mode

At a frequency in the range of 13.56 MHz the chip is operating in HF mode. The digital core and the multipurpose sensor block are clocked by the clock recovery circuit. The local oscillator is disabled. The digital core operates using a preliminary version of the EPC HF standard [23].

UHF Mode

If an RF field in a frequency range between 860 MHz and 960 MHz or in the range of 2.45 GHz is present, the frequency detection unit switches to UHF mode. The local oscillator is enabled and the digital core works according to the EPC Class 1 Gen 2 standard [22, 47, 48].

EPC-Only Mode

In EPC-only mode the chip is operating as a mainstream RFID transponder. The multipurpose sensor block is either disabled or in idle mode (waiting for instructions) depending on V_{DD}.

EPC & Sensor Mode

In EPC & sensor mode V_{DD} is equal to or greater than 1 V and the DC output power of the AC/DC rectifier is sufficient to supply the on-chip temperature sensor. The on-chip temperature sensor or the monitoring of various internal signals are enabled with EPC write commands. The data can be read out using appropriate EPC read commands.

EPC & Off-Chip Sensor Mode

In EPC & off-chip sensor mode V_{DD} is equal to or greater than 1.2 V. The DC/DC charge pump pumps C_{Buffer} up to 3 V. Then the off-chip sensor is enabled and performs its operation. Afterwards the acquired data is ready to be read out. The captured data is refreshed as long as a read out command is present.

5.3 Design of the Analog Components

An RFID transponder usually consists of the same building blocks. Depending on the area of application, the design of the building blocks may vary. As already stated in Section 5.2.2, the frequency detection unit, the clock recovery, the clock divider, the local oscillator, and the clock control unit are reused from the frontend of the multifrequency RFID transponder presented in Chapter 4. The implementation of the remaining important building blocks is discussed

in this section. For the same reasons as explained in Section 4.3 the blocks are designed to operate at HF as well as UHF, to be as energy-aware as possible, and to be efficient in terms of area consumption and thus production costs.

5.3.1 Differential Multifrequency Rectifier

As the behavior, characteristics, application areas, design considerations, advantages and disadvantages of differential and single-ended PSUs have already been explained in detail and various analyses performed in Chapter 2, this section gives a brief summary of the most important design considerations before the actual design of the differential multifrequency rectifier is presented.

5.3.1.1 Design Considerations

Rectifiers for HF RFID transponders are usually designed as single-stage rectifiers with a differential input structure [51, 73]. In contrast, voltage multipliers with several stages are used in UHF RFID transponders [53, 72, 117]. These rectifiers are often based on the Greinacher principle [36]. The multifrequency RFID transponder presented in Chapter 4 features a rectifier which is based on the principle of combining the two rectifiers stated above.

Designing a rectifier for HF and UHF leads to a tradeoff between the performance at HF and UHF. The larger the transistor's $\frac{W}{L}$ the higher the current the transistor can deliver, the lower its on-resistance and the lower the voltage drop. However, the parasitic capacitances increase. Its influence on performance is almost negligible at HF but considerable at UHF. Therefore the transistor size is smaller and thus the performance of the multifrequency rectifier at HF is worse compared to a stand-alone HF RFID rectifier.

At HF the bottle neck for the operating range is usually the quality of the load modulation and not the available input voltage for the desired application. Hence the performance reduction due to the higher on-resistances and voltage drops is marginal.

At UHF the limiting factors are input power and input voltage. That is the reason why UHF RFID rectifiers typically use a multi-stage approach as explained in Section 2.3. These so-called voltage multipliers utilize coupling capacitors to achieve a higher DC output voltage than their AC input amplitude. As can be seen from Figure 2.6 (page 17), the coupling capacitors are in the signal path of the voltage multiplier. The lower the operating frequency the higher the value of these coupling capacitors and the higher the parasitic losses of a voltage multiplier. Of course, it is not reasonable to integrate coupling capacitors with several picofarads to operate a voltage multiplier at HF. Therefore this multifrequency rectifier is implemented as a differential single-stage rectifier with some modifications to be competitive with the state of the art. Hence many parasitics that are present in a multi-stage approach do not exist and the necessary input power at UHF is only a bit higher compared to a two-stage voltage multiplier.

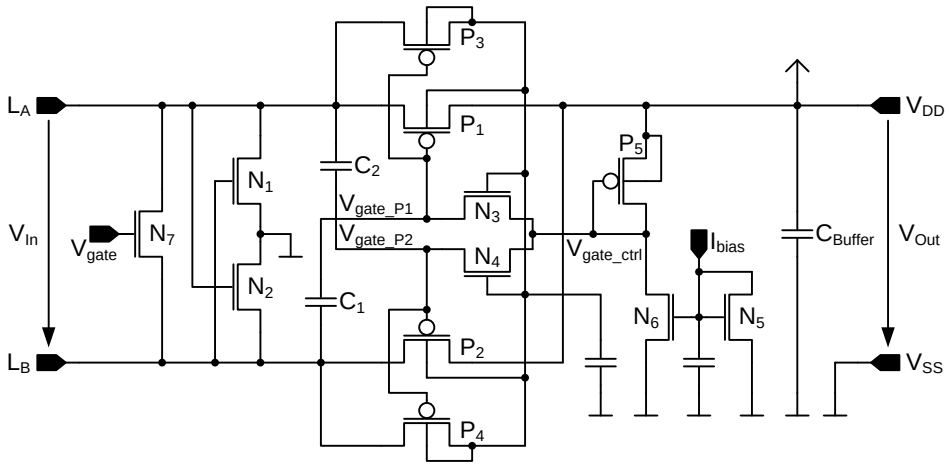


Figure 5.2: Differential multifrequency full-wave rectifier

An essential but unavoidable negative influence is caused by the shunt transistor that is placed between the two input pins. It has to be stronger due to the high possible field strength at HF. Compared to a stand-alone UHF RFID transponder the input sensitivity is lowered by approximately 2 dB. Thus, all in all, the input sensitivity of a multifrequency tag is always lower than those of separate HF or UHF tags, however the difference in this work is marginal for both the tag presented in Chapter 4 and the one presented in this chapter.

5.3.1.2 Implementation

Figure 5.2 shows the single-stage full-wave multifrequency rectifier which is used to power the multifrequency sensing tag. L_A and L_B are the differential inputs with the common mode potential V_{SS} which is generated by the two-cross coupled transistors N_1 and N_2. V_{SS} is directly connected to the chip substrate and is the reference for further considerations.

To use the same rectifier for both HF and UHF, a special circuit is needed to lower the forward voltage drop of the rectification devices to achieve full operation from input power levels of about -12 dBm in UHF mode.
Various techniques to lower the forward voltage drop of the rectification diodes are presented in Section 2.4.4. For this rectifier the I-VTC scheme (see Section 2.4.4.1) and the Threshold Voltage Cancellation (VTC) scheme applied in [79] at HF are used as basics. The resulting VTC circuitry consists mainly of N_6, P_5, N_3, N_4, C_1, and C_2 as shown in Figure 5.2. In contrast to [79], no switches controlled depending on the operating frequency are used to improve performance even in the startup phase, because the signal that provides the information on which mode the rectifier is operating is first available if a sufficient supply voltage is present.
Using the transistors N_3 and N_4 not only saves one biasing path but also improves the startup behavior. Due to the fact that high efficiency is desired between approximately 3 µW and 10 µW, the additional current consumption of 50 nA to bias the diode-connected transistor P_5,

which lowers the gate voltage of the rectification transistor, is negligible, in contrast to the PSU of the EMH in Chapter 3, which is designed for maximum sensitivity at an output load of 190 nW.

The combined two methods to lower the forward voltage drop of P_1 and P_2 are:

1. P_5 is diode-connected and provides a static bias voltage at the node V_{gate_ctrl} that is 1 V_{GS} below V_{DD}. N_3 and N_4 are used to feed V_{gate_ctrl} to V_{gate_P1} and to V_{gate_P2}.

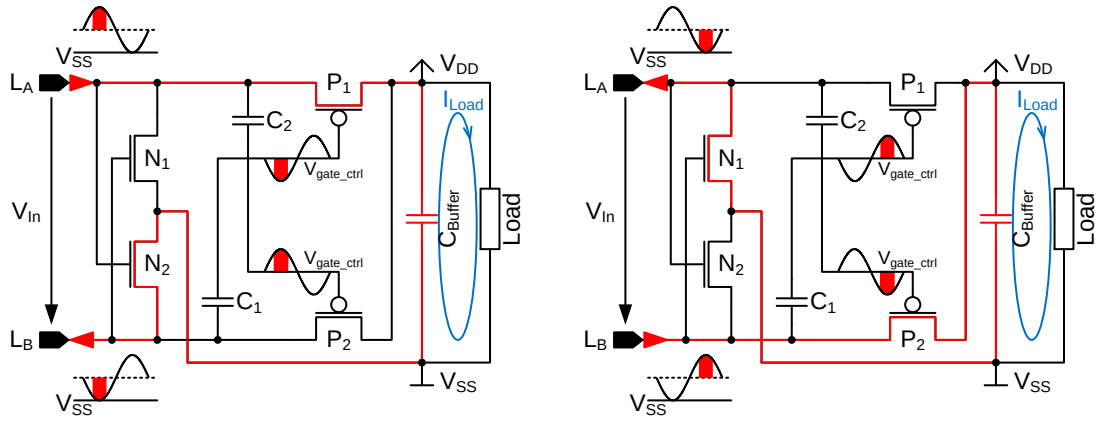
2. The gates of the rectification devices P_1/P_2 are superimposed with the complementary AC signal (L_B/L_A), which they rectify (L_A/L_B) by the coupling capacitors C_1/C_2. The value of C_1 and C_2 is 50 nF.

L_A and L_B are complementary with the reference V_{SS}. The gates of N_3 and N_4 are at V_{DD}, the voltage level at the node V_{gate_ctrl} is one V_t below. The nodes V_{gate_P1} or V_{gate_P2} are forced by L_B or L_A to values above and below $V_{DD} - V_t$. If the nodes V_{gate_P1} or V_{gate_P2} are forced by L_B or L_A to values below $V_{DD} - V_t$ an AC current flows from V_{gate_ctrl} to V_{gate_P1} or V_{gate_P2}. This AC current is limited due to the high on-resistances of N_3 and N_4.

L_A is in positive phase and P_1 is conductive when the amplitude of L_A is one V_t higher than its gate potential. In this phase the gate potential of P_1 (V_{gate_P1}) is lowered due to coupling to L_B (L_B is in negative phase). Therefore the gate overdrive of P_1 increases and the transistor conducts earlier. Simultaneously, L_B is in negative phase and the gate potential of P_2 (V_{gate_P1}) is increased due to coupling to L_A (L_A is in positive phase). This method prevents the direct path between L_A and L_B and thus reduces losses.

Some VTC schemes cause a hysteresis in the minimum input power necessary for a distinct DC load. This hysteresis can be understood in that more input power is necessary to achieve the same output power if the input power is increased. The explanation for this behavior can be found in the fact that some VTC schemes need a distinct V_{DD} to function. Usually the bottleneck is the bias cell which provides the necessary bias currents.

In this work there is no hysteresis in the input sensitivity to turn on the tag because the AC coupling by C_1 and C_2 of V_{gate_P1} and V_{gate_P2} has a higher impact than the DC biasing by P_5 especially during the startup. Additionally, the DC voltage needed to operate is higher than the DC voltage necessary for the bias cell to operate correctly. At startup all nodes are at V_{SS}. So during the positive half-wave at L_A, V_{gate_P1} becomes lower than V_{SS}, P_1 becomes conductive and V_{DD} rises. In the next phase of the input signal the opposite part of the circuit is working. This sequence repeats itself. The node V_{gate_ctrl} rises due to capacitive coupling like V_{DD}. When V_{DD} is high enough the bias cell starts to operate and so V_{gate_ctrl} starts to remain one threshold below V_{DD}. The current flow is depicted in Figure 5.3 and is in the positive phase of the input signal: $L_A - P_1 - C_{Buffer} - N_2 - L_B$. Conversely P_2 conducts when L_B is in positive phase and its amplitude is one V_t higher than its gate potential, and the other part of the circuit works according to the same principle. The current flow in the negative phase of the input signal is: $L_B - P_2 - C_{Buffer} - N_1 - L_A$. So P_1 and P_2 are working as switches instead of diodes like in conventional rectifiers, which increases the efficiency and lowers the voltage drop.



(a) Positive phase of V_{In}

(b) Negative phase of V_{In}

Figure 5.3: Current flow of the differential multifrequency full-wave rectifier

5.3.2 Combined Shunt and Modulator Block

As already mentioned in Section 4.3.2, usually two separate devices are implemented for the shunt and the modulator to simplify the control circuitry. Depending on the breakdown voltage of the devices used and the rectifier topology, it is possible to connect the shunt transistor between the two input pins (AC side – AC shunt) and/or between V_{DD} and V_{SS} (DC side – DC shunt).

In common HF RFID transponders the shunt is placed on the AC side as well as on the DC side of the rectifier [62, 120]. The rectification devices have a larger $\frac{W}{L}$ than in this work and so a DC shunt can draw enough current to limit the input voltage. In this work a DC shunt would lower the sensitivity at UHF enormously because devices with a larger aspect ratio would be necessary, which implicate higher losses. Hence the shunt has to be on the AC side, like in conventional stand-alone UHF RFID tags [5, 26, 118].

As modulation scheme load modulation is performed at HF, at UHF the electro-magnetic waves are backscattered. Possible circuits for stand-alone load and backscatter modulators are published in [53, 120]. The modulator can also be placed either on the AC or DC side, however at UHF it is typically at the AC side for simplicity and performance. If the shunt is on the AC side it is reasonable to use the same shunt transistor also as modulator as in [79] and in Section 4.3.2, thus parasitics are kept as small as possible.

The proposed shunt and modulator block is a combination for HF and UHF with the major advantage that only one transistor is needed at HF and UHF, which keeps the losses low. This transistor N_7 operates as shunt and as modulator at HF and UHF. Therefore the control circuitry depicted in Figure 5.4 is needed. In contrast to the block presented in Section 4.3.2, no additional device is needed.

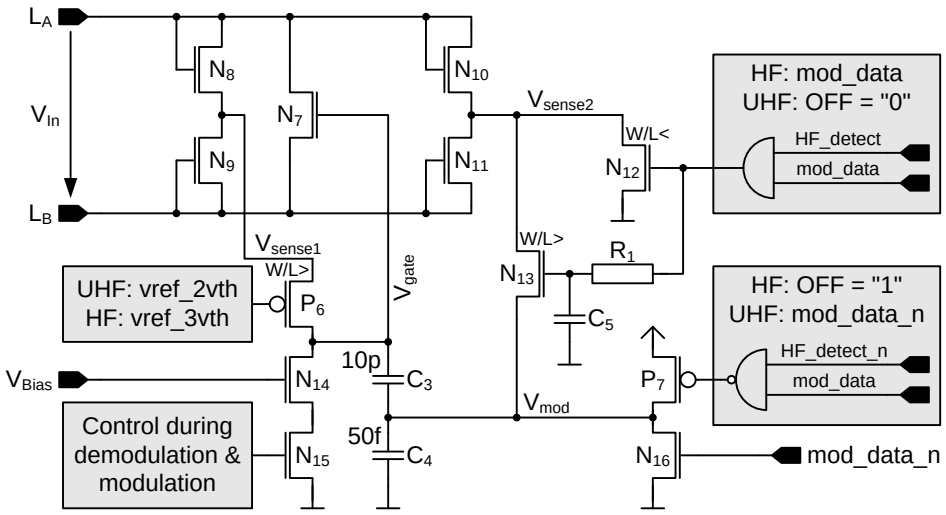


Figure 5.4: Combined shunt and modulator module for HF and UHF

5.3.2.1 Operating Principle

The combined shunt and modulator block operates differently depending on the input frequency. The shunt and modulator operation can be explained separately although they are operating simultaneously. The transistors N_8 and N_9 are diode-connected and generate the sense voltage V_{sense1}. V_{DD} is limited to a maximum of 1.2 V in UHF and 1.6 V in HF mode by connecting the gate of P_6 to two or three thresholds respectively. The gate potential V_{gate} depends on the gate potential of P_6 and the sense voltage V_{sense1}. P_6 is sensitive to changes in its V_{GS}, so V_{gate} changes quickly and overshoots are prevented. At high field strength, N_7 dissipates not only the excessive power, but also transforms the chip impedance which results in a mismatch between antenna and chip and so a part of the impinging power is reflected.

For load modulation in HF and backscattering in UHF mode, the control of N_7 is different:

- In UHF mode N_{12} and N_{13} are switched off and P_7 and N_{16} work as inverter. That means the modulation pulse mod_data pulls V_{mod} to V_{DD}. Due to the coupling by C_3, V_{gate} increases and so the incoming RF signal is backscattered by shorting the chip's input pins.
- In HF mode V_{in} cannot be shorted as in UHF mode, because a V_{in} of at least 600 mV is needed to keep the clock recovery working during modulation. The transistors N_{10} and N_{11} provide the sense voltage V_{sense2}. During the modulation pulse ($mod\_data = 1$), N_{13} charges V_{mod} to V_{sense2} and so V_{gate} increases, due to coupling by C_3. If $mod\_data = 0$, N_{16} restores the former V_{gate}.

This circuit is self regulated. If V_{gate} is too high, the current through N_7 is too high and V_{in} decreases too much. Simultaneously, V_{sense2}, V_{mod}, and V_{gate} decrease, and therefore V_{in} reaches

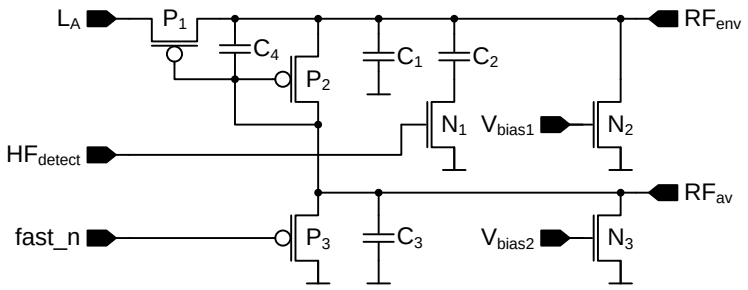


Figure 5.5: Combined demodulator module for HF and UHF

the desired value again. To keep V_{gate} at the same potential during receiving and transmitting, the current source N_{14} is switched off by N_{15}.

5.3.3 Demodulator

As already stated in Section 4.3.3, the demodulator must be operative at minimum V_{DD} so as not to be the limiting factor in the RFID system. To save area, only one demodulator operating at both HF and UHF is developed. Figure 5.5 shows the combined demodulator. The incoming data from the base station is detected by generating the moving average and the envelope value of the input signal and comparing these two values. The principle is similar to that of the demodulator explained in Section 4.3.3, however in this approach the input signal of the demodulator is not capacitively coupled.

Looking at Figure 5.5 it can be seen that the demodulator is based on the principle of a single diode rectifier. P_1 rectifies the incoming RF. P_2 is diode-connected and therefore the moving average value is approximately one threshold below the envelope if the incoming RF signal is not modulated. Due to different timing constraints, depending on the operating frequency, the envelope signal is buffered with 150 fF and 250 fF in UHF and HF mode respectively. The moving average signal is buffered with 8 pF. The envelope and the moving average signal are loaded with current sinks. C_1, C_2 and C_3 are charged from the input signal at L_A and discharged by the current sinks N_2 and N_3 respectively. The factor between the load of the envelope is ten times higher than the load of the moving average signal to ensure that the nodes RF_{env} and RF_{av} follow the RF input signal with the correct transient behavior. P_3 is controlled from the digital core and operates as additional load to avoid false modulation data till the shunt is settled.

5.3.4 Multipurpose Sensor Block

The multipurpose sensor block enables on-chip temperature sensing, on-chip voltage monitoring of dedicated nodes and the utilization of various off-chip sensors or related devices. Figure 5.6 shows the architecture of the multipurpose sensor block which includes an on-chip temperature sensor, the off-chip sensor interface and a control unit that is clocked by the halved system clock.

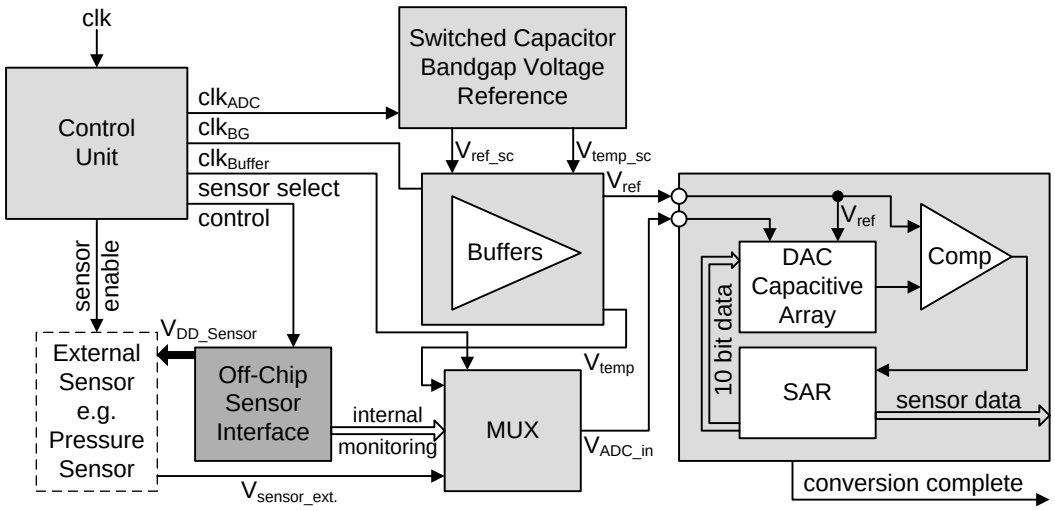


Figure 5.6: Architecture of the multipurpose sensor block

5.3.4.1 On-Chip Sensor

The multipurpose sensor block uses the principle presented in Section 3.4.6. The on-chip temperature measurement is done by comparing a temperature dependent to a temperature independent voltage. How this operation is performed is also explained in Section 3.4.6.

In contrast to the implementation in the EMH (see Chapter 3), where the on-chip sensor is enabled by a Level Detection Unit (LDU), the on-chip temperature sensor is controlled by the RFID interface in the multifrequency sensing tag. Therefore the digital core of the sensing tag, as well as the control unit of the multipurpose sensor block, feature special functionalities. Of course, the temperature measurement can not be performed before the supply voltage is sufficiently high.

Typical Operation Sequence

A typical operation sequence of an on-chip temperature measurement cycle is to request a temperature measurement process via an EPC write command.

The tag memory is divided into four distinct banks (for further information see [22]).

1. The reserved memory contains kill and/or access passwords.
2. The EPC memory contains the electronic product code.
3. The TID memory contains identifying information.
4. The user memory allows storing user-specific data. A write command at a distinct address in this user memory enables the sensor block. Depending on the address, either the on-chip temperature sensor or the off-chip sensor interface is requested.

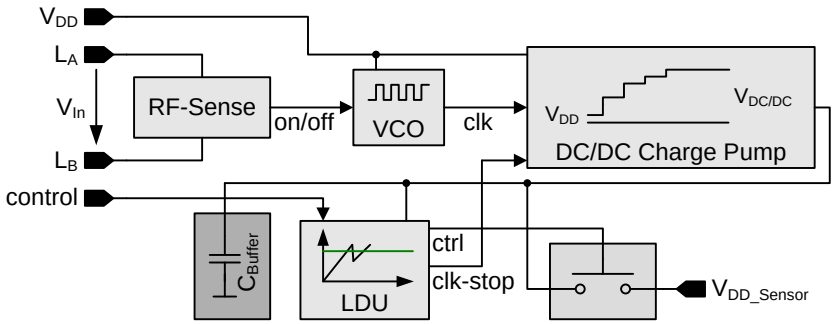


Figure 5.7: Architecture of the off-chip sensor interface

If the on-chip sensor operation is requested and if the output voltage of the AC/DC rectifier is high enough the control unit starts the Switched Capacitor (SC) bandgap reference. So the reference of the Analog to Digital Converter (ADC) is the temperature independent voltage and the input signal is the temperature dependent voltage. After settling of the SC bandgap reference, the ADC starts the sampling process. After the conversion, the signal *conversion_complete* (see Figure 5.1) goes to "high", which signals valid data at the output of the ADC. This data is then latched into the user memory at the next clock cycle. The stored data can then be read out with an EPC read command on the address in the user memory where the sensor data is stored. The binary sensor data is then interpreted by a demonstrator system.

5.3.4.2 Off-Chip Sensor Interface

Considering the efficiency of the AC/DC rectifier, the power which can be converted from the electro-magnetic field in a useful operating range is not sufficient to continuously drive sensors or related devices with a power consumption in the milliwatt range. Therefore the EMH, presented in Chapter 3, is implemented in the off-chip sensor interface of the multifrequency RFID tag with slight adaptions.

Figure 5.7 shows the architecture with the following main blocks: an RF input power detector, a Voltage Controlled Oscillator (VCO), a DC/DC charge pump based on the Dickson topology and built with thin oxide PMOS transistors and a LDU. As already explained in detail in Chapter 3, the basic functionality is to harvest the energy and store it in an energy reservoir. An on-chip or off-chip buffer capacitor can be used as an energy reservoir. If enough energy is stored the connected system is powered.

Operating Principle

The RF-sense block senses the RF input voltage by means of signals generated in the shunt and modulator block. If this voltage is sufficient the VCO is enabled and thus V_{DD} is pumped up to V_{DCDC}. The output of the DC/DC charge pump is buffered by C_{Buffer} and observed by the LDU. If V_{DCDC} reaches 3 V the output switch is closed and the system connected to the off-chip sensor interface is supplied as long as V_{DCDC} falls below 1 V or the output switch is

opened by a control signal. To limit V_{DCDC} a clock-stop signal stops the DC/DC charge pump if V_{DCDC} reaches 3.3 V.

5.4 Experimental Results

This section discusses the measurement results of the multifrequency passive sensing tag. Various performance measurements and functional verification are presented. The DC current consumption and the RF input power at different output voltages of the AC/DC rectifier and at different operating modes are presented and compared with the corresponding simulation results. Of course, the key parameters, minimum electrical field strength at HF and input sensitivity at UHF are determined too. Furthermore, the multipurpose sensor block is investigated and the important key figures are reported. A demonstrator system proves the functionality of the sensing tag, while the temperature data is transmitted to an HF and a UHF RFID reader to verify the multifrequency applicability.

5.4.1 HF Measurements

As stated above, the minimum field strength H_{min} is determined. For a reasonable comparison to HF RFID transponders the chip is set to EPC-only mode (see Section 5.2.4). That means the multipurpose sensor block is permanently disabled. By using the same contactless measurement setup and method as in Section 4.4.1 (which is described in Section 2.7.1) results in a minimum field strength of 36 mA m^{-1} at a frequency of 13.56 MHz. That means H_{min} is lower than the multifrequency tag presented in Chapter 4. This is because the DC voltage is differently generated and not lowered by one additional diode-connected transistor as intentionally done in Chapter 4. Furthermore, a different modulation scheme and thus different DC voltage levels in the shunt and modulator block are used to improve the performance.

5.4.2 UHF Measurements

The input sensitivity and the different operating modes of the multifrequency sensing tag is defined in Section 5.2.4. Regarding performance, the focus is put on 868 MHz. Therefore the input sensitivity is determined at all three operating modes – the EPC-only mode, the EPC & sensor mode, and the EPC & off-chip sensor mode.

This chip has a differential input structure, thus it has to be taken care how the input of the chip is excited. That means either a network analyzer and a signal generator with differential output or a network analyzer and a signal generator with single-ended output and a single-ended to differential to conversion is needed. Section 2.7.2.4 comprises the background information addressing this topic. How these differential input structures can be handled using non-expensive measurement equipment – especially using a single-ended network analyzer – has already been explained in Section 2.7.2.5. Based on these considerations the contact-based

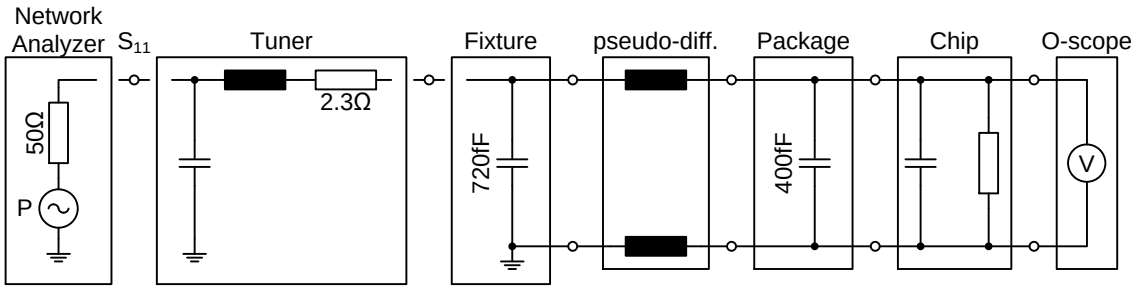


Figure 5.8: Contact-based measurement setup including the single-ended to differential conversion for UHF

measurement setup depicted in Figure 5.8 is utilized. Due to the single-ended to differential conversion the same package and test fixture as introduced in Section 2.7.2.1 can be used.

The measurement procedure is similar to the procedure in Section 4.4.2 and can be explained as follows:
At first the packaged chip (Device Under Test (DUT)) is directly connected to the single-ended network analyzer to achieve a rough estimation of the capacitance. Knowing the capacitance, the value of the two inductors of the measurement setup shown in Figure 5.8 can be calculated as:

$$L = \frac{1}{2} \cdot \frac{1}{(2\pi f)^2 \cdot C}\bigg|_{C=C_{SMA\text{-}Fixture}+C_{Package}+C_{Chip}} \tag{5.4.1}$$

As a matter of course the Q Factor of these inductors has to be high to achieve low losses. Now the two inductors are soldered between the package and the SMA connector and the reflection coefficient is measured again at $V_{DD} \approx 1\,\mathrm{V}$. Depending on S_{11}, it might be necessary to adopt the value of the two inductors to achieve acceptable measurement results. The network analyzer is replaced by a signal generator, which is connected to the DUT and excites the chip with the inventory command. The power of the signal generator is lowered as long as the chip responds correctly. At this setting of the signal generator the supply voltage in idle mode is metered. Then the network analyzer is connected and set to achieve the same supply voltage again. Knowing the output power of the network analyzer and the reflection coefficient, the input power of the DUT can be calculated using (2.7.12) on page 69. Embedding all measurement losses (worst case), the input sensitivity in EPC-only mode is determined to be $-12.5\,\mathrm{dBm}$ at a frequency of 900 MHz.

Using the same matching (maximum sensitivity in EPC-only mode), input sensitivities of $-10.3\,\mathrm{dBm}$ and $-7.9\,\mathrm{dBm}$ for operation in EPC & sensor mode and EPC & off-chip sensor mode, respectively, are measured at a frequency of 900 MHz. This means the input sensitivity in these two modes can be increased if a different matching is used. An even better input sensitivity in EPC & off-chip sensor mode can be achieved by lowering the detection levels at which the off-chip sensor interface is enabled considering the available input power, because the measurement process has shown that there is still potential left.

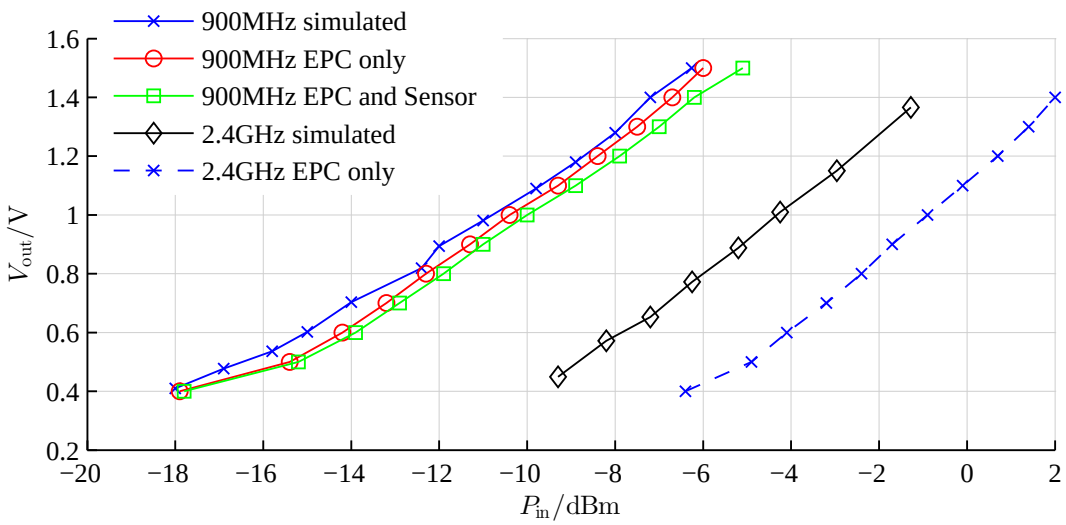


Figure 5.9: V-P characteristic of the multifrequency rectifier

5.4.3 Performance Tests

Figure 5.9 shows the DC output voltage of the AC/DC rectifier as a function of the RF input power. The chip was simulated at 900 MHz and 2.45 GHz with an adapted test bench including the losses caused by the measurement setup at 900 MHz. Comparing the simulation data with the corresponding measurement it is evident that measurement and simulation match well at 900 MHz.

At 2.45 GHz the deviation between measurement and simulation is approximately 2 dB. This is because of the frequency behavior of the measurement setup for minimum input power. The measured input sensitivity at 2.45 GHz is lower compared to the simulation due to higher losses of the measurement setup. The losses are between approximately 1.5 dB and 5 dB depending on the input impedance and thus the input power and operation mode of the chip. Determining these losses has to be done using the same principle as applied to determine the losses caused by the tuner in Section 2.7.2.3.

At the measurement setup depicted in Figure 5.8, the losses are caused by the limited Q Factor of the inductors used. The losses have to be determined separately for every measuring point. Furthermore, some assumptions have to be made and therefore the values in Figure 5.9 are not corrected for losses. That means all measurement values are worst case values.

To show the influence of the shunt on the input sensitivity the VP-characteristics are also simulated with doubled and halved $\frac{W}{L}$ of the shunt. The results are shown in Figure 5.10. The one-stage differential rectifier is compared with a two-stage voltage multiplier designed with the same devices for an operating frequency of about 900 MHz. The forward voltage drops of the rectification devices of the two-stage voltage multiplier are also lowered by statically biasing the gates of the transistors in an appropriate way, as in the first method explained in

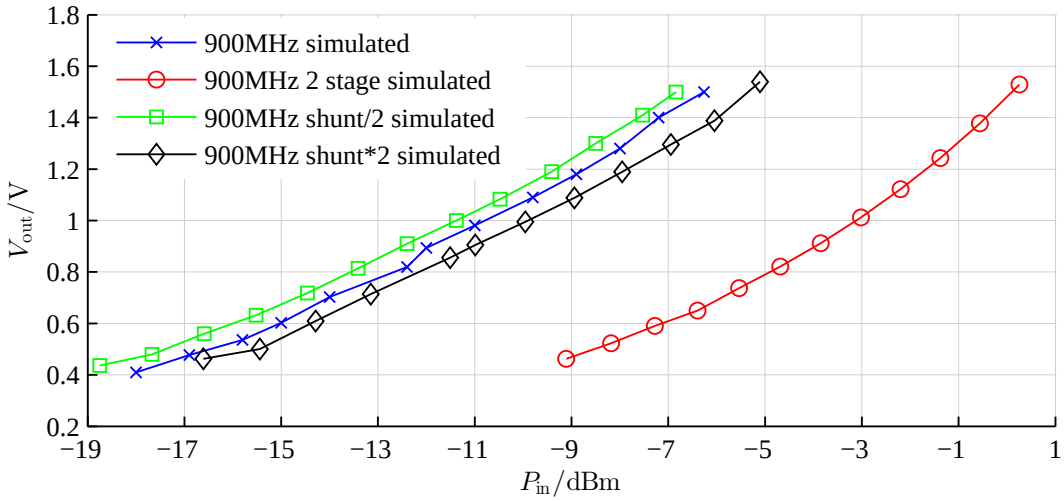


Figure 5.10: Comparison of the V-P characteristic of the multifrequency rectifier with different shunt geometries and a two-stage voltage multiplier

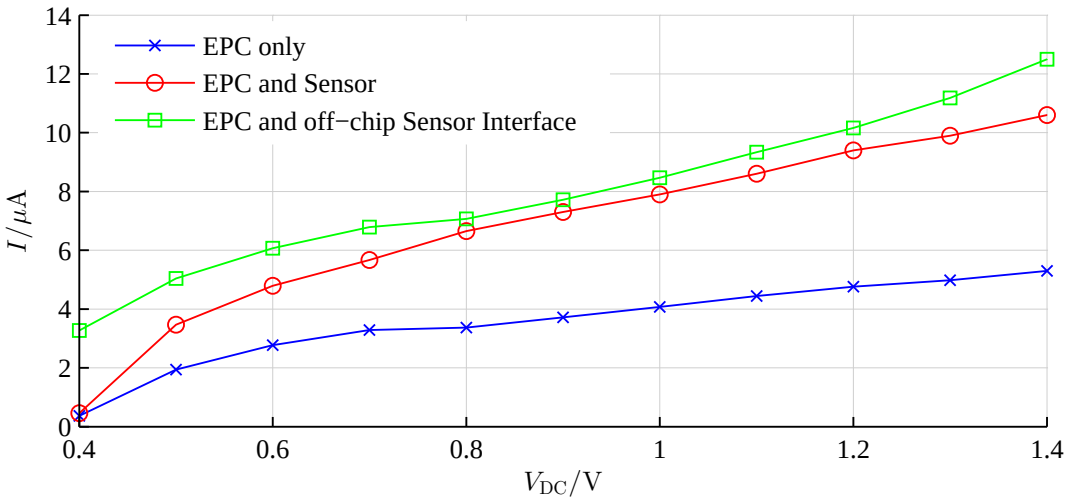


Figure 5.11: Measured I-V characteristic of the multifrequency rectifier at $f = 900\,\mathrm{MHz}$

Section 5.3.1.2. The results are also visualized in Figure 5.10. From Figure 5.10 it becomes evident that different rectifier structures need different devices to achieve good performance. Compared to the two-stage multifrequency rectifier used in the multifrequency RFID tag in Chapter 4, the performance differs by only a few percent.

Figure 5.11 shows the load current of the AC/DC rectifier at different output voltages and operating modes. From Figure 5.9 and 5.11 the efficiency of the rectifier in EPC-only mode at an input power of $-12.5\,\mathrm{dBm}$ can be calculated to be 7.5 % embedding all measurement losses. Assuming that the measurement losses are 3 dB, which is a reasonable value, the efficiency is doubled to be 15 %. The efficiency of the rectifier depends on the input power, the output

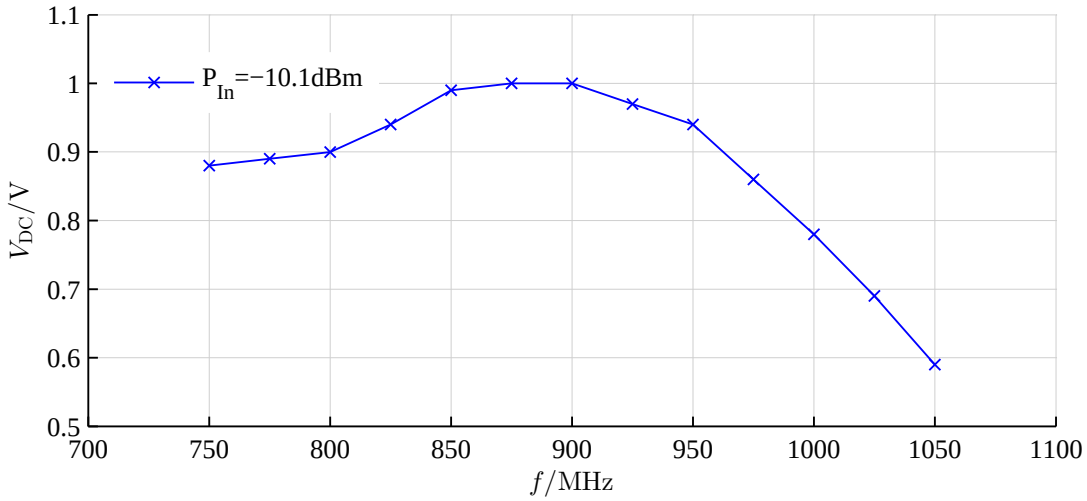


Figure 5.12: Measured V-f characteristic of the multifrequency rectifier at $P_{In} = -10.1\,\mathrm{dBm}$

voltage and the output load.

Figure 5.12 shows the output voltage of the AC/DC rectifier at different input frequencies at an input power of −10.1 dBm and an output load of 250 kΩ.

5.4.4 System Measurements

At 13.56 MHz, 868 MHz and 2.45 GHz functionality tests were performed that confirm correct chip operation. The chip was also measured with a prototype of an UHF antenna up to an operating distance of 7.2 m at 868 MHz.

The multipurpose sensor block has a total average current consumption of 2.7 µA at a supply voltage of 1 V with the off-chip sensor interface disabled. The additional gates used for the sensor block draw approximately 1.1 µA additional current. The current consumption of the off-chip interface depends on the output voltage of the AC/DC rectifier and the load of the DC/DC charge pump and is in a range of a few microwatts. As long as the output switch is not enabled, the level detection unit has a maximum average current consumption of 310 nA, which is the current consumption of the LDU2 of the EMH presented in Chapter 3. The key figures of the sensing tag are summarized in Table 5.1. Table 5.2 gives an overview of the current consumption of the different RFID blocks at a supply voltage of 1 V. The clock recovery operates only in HF mode. In UHF mode it draws no current because all bias currents are disabled.

5.4.4.1 Demonstrator System

A demonstrator system is built up with commercially available HF and UHF RFID readers. Figure 5.13 shows this system developed to demonstrate the temperature measurement. The

Interface	
Technology	0.13 µm CMOS
Active area	0.95 mm^2
Antenna interface	2 Pin
Frequency range	HF(13.56 MHz), UHF(860 MHz to 2.45 GHz)
Protocol standard	EPC HF, EPC Gen2 UHF
Operating distance	7.2 m @ 868 MHz, 4 W EIRP
Input sensitivity	
HF EPC-only mode	36 mA/m
UHF mode (900 MHz):	
EPC-only mode	−12.5 dBm
EPC & sensor mode	−10.3 dBm
EPC & off-chip sensor mode	−7.9 dBm
DC loading power	
UHF EPC-only mode	3.1 µW
UHF EPC & sensor mode	7.9 µW
UHF EPC & off-chip sensor mode	10.2 µW
Multipurpose sensor block	
On-chip sensor	
Supply voltage	1.0 V
Current consumption: total	2.7 µA
Current consumption: SC bandgap	497 nA
Control logic	84.7 nA (simulated)
Off-chip sensor interface	
Output voltage	3.0 V
Current consumption LDU	310 nA
ADC (@ $f = 1$ MHz):	
ENOB	8.2 bit @ 36 ksamples/s
FOM	419 fJ/conversion step

Table 5.1: Key figures of the multifrequency sensing tag

HF and the UHF RFID reader are consecutively controlled by a program developed in the system design software LabVIEW. The temperature data are read out using EPC commands as explained in Section 5.3.4.1. A one point calibration is necessary to calibrate the temperature offset, which is done in software. If the sensing tag is moved from one reader antenna to the other the chip operates in that mode in which more power is received. That means if more power is received at HF the chip operates in HF mode and vice versa.

Module	Current consumption
Rectifier: biasing for P_5	50 nA
Shunt & TX module	260 nA
Demodulator:	
generation of av. and env. signal	275 nA
buffer	100 nA
comparator	100 nA
Frequency detection unit	75 nA
Clock recovery:	
clock extraction	2.15 µA
clock division	1.1 µA
Local oscillator	0.9 µA
Digital core	3.5 µA

Table 5.2: Current consumption of the RFID blocks at $V_{DD} = 1\,\mathrm{V}$

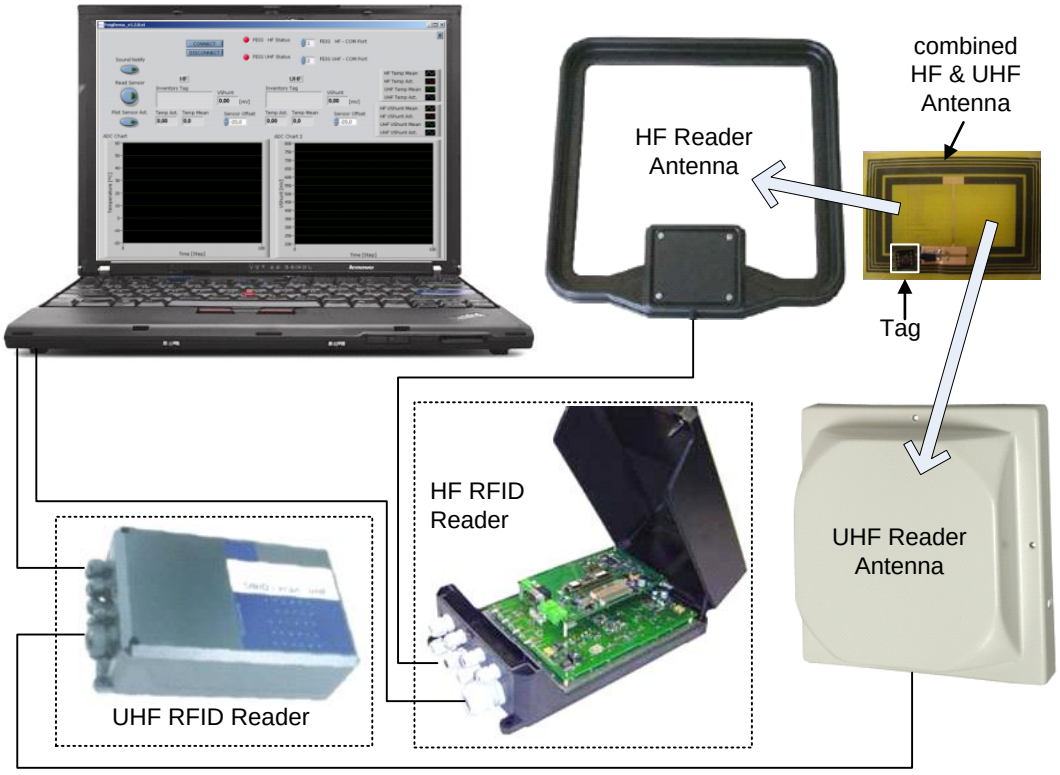


Figure 5.13: Block diagram of the demonstrator system

	this work	**[116] by D. Yeager**	**[118, 119] by J. Yin**	**[27] by J. Essel**	**[79] by A. Missoni**
Technology	0.13 µm	0.13 µm zero Vth	0.18 µm	0.13 µm	0.12 µm
Interface	2 Pin	2 Pin	2 Pin	3 Pin	2 Pin
Area	0.95 mm^2	2.0 mm^2	1.1 mm^2	–	0.29 mm^2
Frequency	13.56 MHz, 860 MHz to 2.45 GHz	900 MHz	860 MHz to 960 MHz	13.56 MHz, 860 MHz to 960 MHz	13.56 MHz, 860 MHz to 2.45 GHz
Standard	EPC HF & Class 1 Gen 2 UHF	EPC Class 1 Gen 2 UHF	EPC Class 1 Gen 2 UHF	EPC HF & Class 1 Gen 2 UHF	EPC HF & Class 1 Gen 2 UHF
Sensitivity UHF	−12.5 dBm −10.3 dBm	−12.0 dBm	−6.0 dBm	−11.0 dBm	−12.5 dBm
DC load UHF	3.1 µW 7.9 µW	9.2 µA 1.8-3.6 V	12 µW	10 µW	–
Sensor type	on&off-chip, RSSI, temp.	temp.	temp.	temp.	–
Rectifier type	1-stage full-wave	6-stage	22-stage half-wave	diff. HF, 2-stage half-wave UHF	1-stage full-wave

Table 5.3: Comparison with state of the art

5.4.5 Comparison with State of the Art

There are more and more publications arising in the field of wireless sensing by means of exploiting RFID technology. Mostly the frontends of these sensor functionality enhanced RFID transponders operate only at UHF. However, in this work a multifrequency solution is presented which features, besides the on-chip sensor, also an interface to connect any desired off-chip sensor to the RFID transponder. A comparison to some selected state-of-the-art publications is given in Table 5.3.

In [116] an EPC Class 1 Gen 2 compatible UHF RFID tag for biosignal acquisition is presented. The tag was mounted on a hawkmoth to measure in-flight core body temperature. The DC power generation is performed by a six-stage voltage multiplier built with zero threshold transistors. The overall tag current consumption is given with 9.2 µA, while linear voltage regulators provide different supply voltage levels for this system.
A passive UHF RFID tag with embedded temperature sensor is presented in [118, 119]. A 22-stage triple output rectifier powers the Integrated Circuit (IC). An injection-locked frequency divider and a ring oscillator are integrated to clock the IC. The frequency divider consumes 19.5 µW, which is more than the overall power consumption of a common RFID tag. If only

the ring oscillator is enabled the power consumption is given with 12 µW. However the input sensitivity is just −6 dBm, probably due to the 22-stage approach in combination with a power consumption in the microwatt range.
In [27] a multistandard frontend for an RFID sensor tag is designed by integrating a differential rectifier for HF and a single-ended rectifier for UHF as done in Chapter 4. Due to the fact that the PSU in [27] is designed with three pads for antenna connection, it is possible to separate the HF from the UHF rectifier. Thus the HF rectifier does not influence the UHF rectifier anymore. Also, separate HF and UHF voltage limiters are necessary, which do not interact. As a consequence a higher input sensitivity and easier control are possible with a three-pad design. Nevertheless, three pads are one more than necessary, as shown in [79] and this work. As area reflects in production costs, a two-pad solution would be the preferable one.
The first multifrequency tag is presented in [79]. A full-wave rectifier operates at HF. At UHF also two secondary AC/DC charge pumps deliver voltage potentials for a DC/DC converter.

This work does not need any secondary charge pumps, DC/DC converters, or more than two pins for the AC/DC conversion. A differential multifrequency full-wave rectifier with an innovative combination of two methods to lower the forward voltage drop of the rectification devices operates from 13.56 MHz up to 2.45 GHz. If operated as a normal RFID tag an input sensitivity of −12.5 dBm is achieved, which is equal to [79], even higher than in [27] and [118, 119], and comparable to stand-alone UHF RFID as shown in Table 5.3 and Table 4.1.

5.5 Conclusion

This chapter presented a multifrequency passive sensing tag which includes an on-chip temperature sensor and an off-chip sensor interface. The novel concept of combining a multifrequency EPC compatible RFID tag with an energy harvesting system based on the principle shown in Chapter 3 makes it possible to control sensors by standardized EPC commands. The controlling of the sensor functionality and the transmission of all sensor data are done by exploiting RFID technology. Even though the tag is remotely powered, it can drive sensors with a power consumption up to the milliwatt range, which increases the applicability of passive RFID systems. The multipurpose sensor block features an on-chip temperature sensor, on-chip voltage monitoring and can handle various off-chip sensors by just drawing 2.7 µW (off-chip sensor interface disabled). The sensing tag operates in any HF and UHF RFID system in a frequency range from 13 MHz up to 2.45 GHz according to the EPC HF and UHF standard. Compared to the multi-standard frontends presented in [29] and [27], the proposed sensing tag needs only two interface pins instead of three, which keeps the costs small. Nevertheless, the input sensitivity is in the same range despite the combined HF and UHF rectifier. To save chip area the blocks of the analog frontend are capable of both frequency ranges instead of implementing separate blocks for HF and UHF. An HF, a UHF or a broadband (combined HF & UHF) antenna can be connected to the sensing tag. With the chip connected to a broadband antenna, the temperature measurement is demonstrated by using commercially available HF and UHF RFID readers with an operating frequency of 13.56 MHz and 868 MHz, respectively. Due to the innovative

combination of two methods to lower the forward voltage drop of the rectification devices, it is feasible to use the same differential one-stage rectifier from 13.56 MHz up to 2.45 GHz by achieving high performance. An input sensitivity of −10.3 dBm (embedding the measurement losses) and a power consumption of 7.9 µW in UHF EPC sensor mode (f = 900 MHz) are obtained. Despite the additional functionality and the extended operating frequency range, these values are comparable to the state of the art as listed in Table 5.3.

Chapter 6

Conclusion and Research Summary

In this thesis the topic of *Ultra Low Power Electro-Magnetic Energy Harvesting for a Wireless Sensor Node Enhanced with RFID Functionality* was discussed. The work is divided in five different chapters addressing an introduction, different Power Scavenging Units (PSUs), an Electro-Magnetic Energy Harvester (EMH) which is part of a Wireless Sensor Node (WSN), a Multifrequency Radio Frequency Identification (RFID) Transponder and a WSN including RFID applicability.

Chapter 1 started with an introduction into fully integrated WSNs including their benefits and drawbacks, which pointed out the need for energy harvesting – saving the battery to achieve cheaper, smaller, environmentally friendly and maintenance-free WSNs. The project iTire, which made it possible to research in the field of electro-magnetic energy harvesting, and the iTire chip are also introduced in this chapter.

Based on the decision that the WSN dedicated for use in an advanced Tire Pressure Monitoring System (TPMS) should be supplied from the RF field, different structures of PSUs are investigated and analyzed in detail in Chapter 2 to find the best solution for the desired applications. In Section 2.4 all challenges when it comes to the Integrated Circuit (IC) design are discussed. Beginning with the antenna and its matching to the IC, it is explained how the loaded Quality Factor (Q Factor) influences the performance and thus the design. Different methods to lower the forward voltage drop of the diode-connected transistors are analyzed and compared. The influence of the number of stages of a voltage multiplier on the Power Conversion Efficiency (PCE) is investigated, with the outcome that the highest PCE can be achieved with only one stage. Section 2.5 contains a detailed AC, DC, power, and power dissipation analysis, where it is shown how and which parasitic effects influences the PCE. Appropriate simulation methods like Periodic Steady-State (PSS) and Periodic S-Parameter (PSP) analysis and the development of a suitable simulation testbench are presented in Section 2.6, followed by the measurement methods focusing on the use of non-expensive laboratory equipment explained in Section 2.7. A novel and accurate measurement method for the input sensitivity, a key parameter of every PSU, is developed by means of determining the losses of the measurement setup in two different ways. Furthermore, the generation of a differential input signal by using a single-ended network analyzer is presented.

Chapter 3 addressed the concept and design of an electro-magnetic energy harvesting system. As the only useful way to increase the operating range of a electro-magnetic powered WSN is to minimize the input power of the IC, an ultra low power design and new concepts are

unavoidable. To lower the power consumption down to 190 nW requires cutting the direct connection between the load and the output of the PSU. Bias and cross currents have to be lowered to a few nanoampere, which makes circuits slow and implicates very high ohmic nodes which are sensitive to cross-talk. Furthermore, transistors and resistors become larger, and parasitics capacitors have greater influence compared to conventional analog circuit designs. As active chip area is reflected in chip costs it is not feasible to integrate high ohmic resistors, thus new ideas are applied to avoid exceeding chip size limits in ultra low power design. Instead of a resistor-based voltage divider, a circuit featuring a bias cell, an Operational Transconductance Amplifier (OTA) and a comparator with nanoampere biasing in combination with a transistor-based voltage divider is used for reference voltage generation. As can be seen in Section 3.3.2, the trick is to separate the harvesting system into two subsystems and connect the load only if enough energy is stored. All the thereby arising design challenges are treated in detail in this chapter. Experimental results have shown that it was possible to design an Level Detection Unit (LDU) with a current consumption lower than 170 nA.

Chapter 4 presented a multifrequency RFID transponder that can be used to enhance the advanced TPMS with RFID functionality to enable worldwide tire identification. As a combined single-ended and differential AC/DC converter that fits for the multifrequency requirements was available, it was decided to convert novel concepts for shunt, modulator, demodulator, and operating frequency detection into circuit design. The arising benefit was a fully EPC HF and EPC Class 1 Gen 2 UHF compatible IC with only two interface pins for antenna connection and an input sensitivity comparable to a stand-alone UHF RFID transponder despite the multifrequency option.

The novel concept of combining a multifrequency EPC compatible RFID tag with an energy harvesting system made it possible to operate sensors by means of standardized EPC commands. Thanks to the principle shown in Chapter 3, no battery is needed for power supply, which makes the WSN presented in Chapter 5 lighter, smaller, cheaper, environmentally friendly and maintenance free. In addition to it, common RFID systems can be exploited for control of the sensor functionality and transmission of all sensor data. Novel building blocks are designed which are capable of both frequency ranges to save active area. The AC to DC conversion is done by a differential full-wave rectifier where an innovative combination of two methods lowers the forward voltage drop of the rectification devices as shown in Section 5.3.1. A multipurpose sensor block was integrated that features an on-chip temperature sensor, on-chip voltage monitoring, and can handle various off-chip sensors by just drawing 2.7 µW. Summing up, this WSN is applicable especially under those conditions where batteries cannot be replaced or where it is not possible to supply the sensor system by wire or by thermal or photovoltaic energy harvesting. For that reason this concept fits perfectly for the advanced TPMS IC of the iTire project.

6.1 Building them Together

The different blocks of the iTire chip have already been introduced in Section 1.4. In this work the energy harvesting unit, the RFID analog frontend module and the off-chip sensor interface,

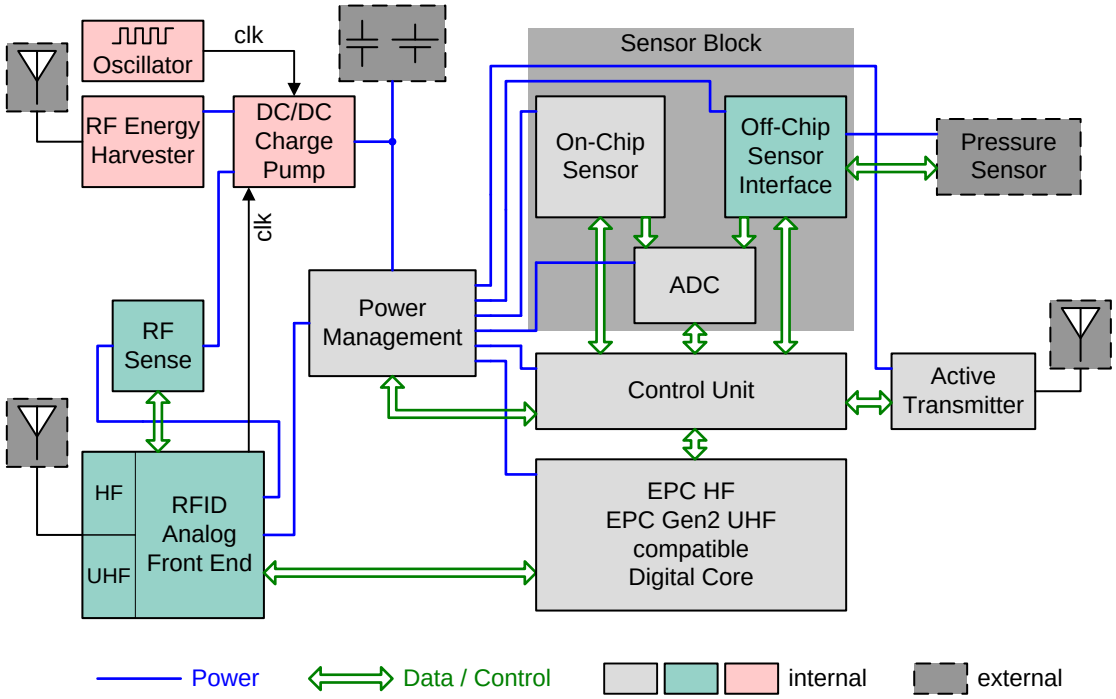


Figure 6.1: System architecture of the iTire chip showing the integrated blocks

including the concept of the interaction of the blocks, were developed. The on-chip sensor, the Analog to Digital Converter (ADC) and their controlling were developed and extended to a generic low voltage, ultra low power sensor interface by Martin Wiessflecker [111], low power and low drop DC/DC converters were designed by S. Gruber [39], and the active transmitter was implemented by H. Unterassinger as shown in [38].

The blocks of the developed IC's in this work are marked in cyan and light red. They are integrated into the iTire chip (system architecture see Figure 1.1 on page 5) as shown in Figure 6.1. The energy harvesting unit is built up by the EMH presented in Chapter 3. The multifrequency RFID transponder from Chapter 4 as well as the multifrequency sensing tag from Chapter 5 can be utilized as an RFID module, whereas the analog frontend, the digital core, and the sensor block of the multifrequency sensing tag are integrated. All the necessary control functions had already been implemented in the digital core, so just a few modifications had to be done.

As already stated in Section 1.4.1 and obvious from Figure 6.1 there are three possible power sources for the iTire chip:

- Energy harvester,
- RFID, and
- Battery.

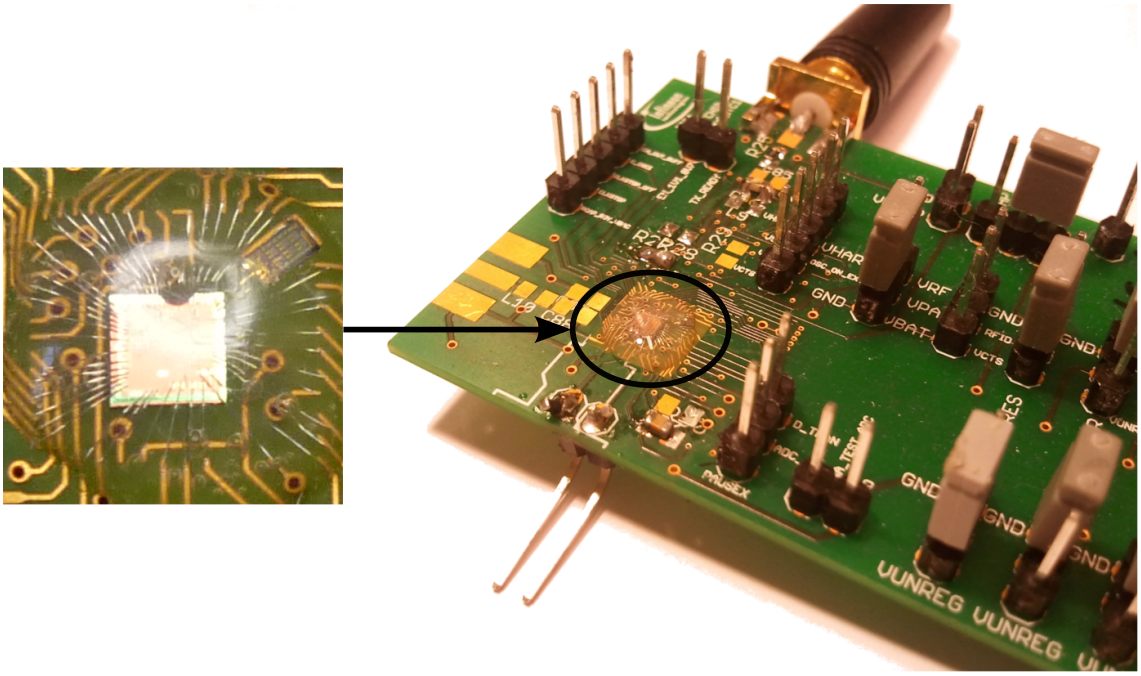


Figure 6.2: iTire die bonded onto the iTire test PCB

So from the power management's point of view there are different possible power flows. If the chip operates in harvesting mode, the PSU of the RF energy harvester converts the incoming AC signal into a DC voltage. This voltage is fed to the DC/DC charge pump which transfers charge to the off-chip buffer capacitor. If the voltage level at this buffer capacitor exceeds a certain limit, the control unit of the IC starts to operate and enables or disables the different functional blocks depending on the available energy in the buffer capacitor.
In RFID mode the PSU of the RFID module is used to generate the DC power for tire identification. If the power gained by the RFID interface is more than required to operate the control unit and the on-chip sensor, the power path through the DC/DC charge pump is enabled and thus the excess energy is transferred into the off-chip buffer capacitor. This enables full chip functionality with each of the mentioned power sources. Whenever the available energy in the capacitor is sufficient and an active data transmission is required by means of RFID commands, the transmitter is enabled.
The chip can also be configured in polling mode. Therefore the off-chip buffer capacitor has to be replaced by a battery. In this case a polling oscillator with a frequency of approximately 1.3 kHz takes care of a periodic data transmission using the active transmitter. More details on the implemented low power and low drop DC/DC converters used in the power management are available in [39].

Figure 6.2 shows the iTire chip bonded directly onto a PCB to keep the parasitics and losses for the interfaces as small as possible. The chip can also operate using a solar cell that replaces the function of the PSU of the energy harvester.

6.2 Outlook

The presented ultra low power electro-magnetic energy harvester will increase the applicability of systems powered from the electro-magnetic field. A power consumption lower than just 190 nW of the circuitry that senses the voltage in the energy reservoir and controls the desired operations lets the dream of a battery-less WSNs achieving adequate operating distances come true.

Both the flexible design and the clearly separated modules simplify the reusability of the developed circuits. For this reason among others, several blocks presented in this thesis have been utilized in subsequent designs and developments. The analog frontends of the EMH as well as of the RFID tag are implemented in *A Remotely Powered Multi Frequency RFID Sensing Tag with Integrated Impedance Measurement Interface* [113], which performs an impedance measurement [112] of an interdigitated electrode structure sensor by exciting the sensor with a sinusoidal current. Another application of the EMH can be found in *A Passive Ultra Wideband Tag for Radio Frequency Identification or Wireless Sensor Networks* [35], where a tiny on-chip antenna is connected to the input pins of the EMH to supply the Ultra Wide Band (UWB) frontend.

The presented architectures of the WSNs can also be used in different technologies, while the input sensitivities of the PSUs will noticeably increase if using Schottky diodes or transistors with low threshold voltages and few parasitics.

Appendix A

Test Chip Layouts and Chip Micrographs

Each circuit presented in this thesis has been fabricated in an Infineon 0.13 µm CMOS process. This chapter gives an overview of the layouts of the various test chips containing these circuits.

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A.1 The Electro-Magnetic Energy Harvester

Figure A.1 shows the layout of a stand-alone version of the Electro-Magnetic Energy Harvester containing only the energy harvesting system as shown in Figure 3.3 on page 83.

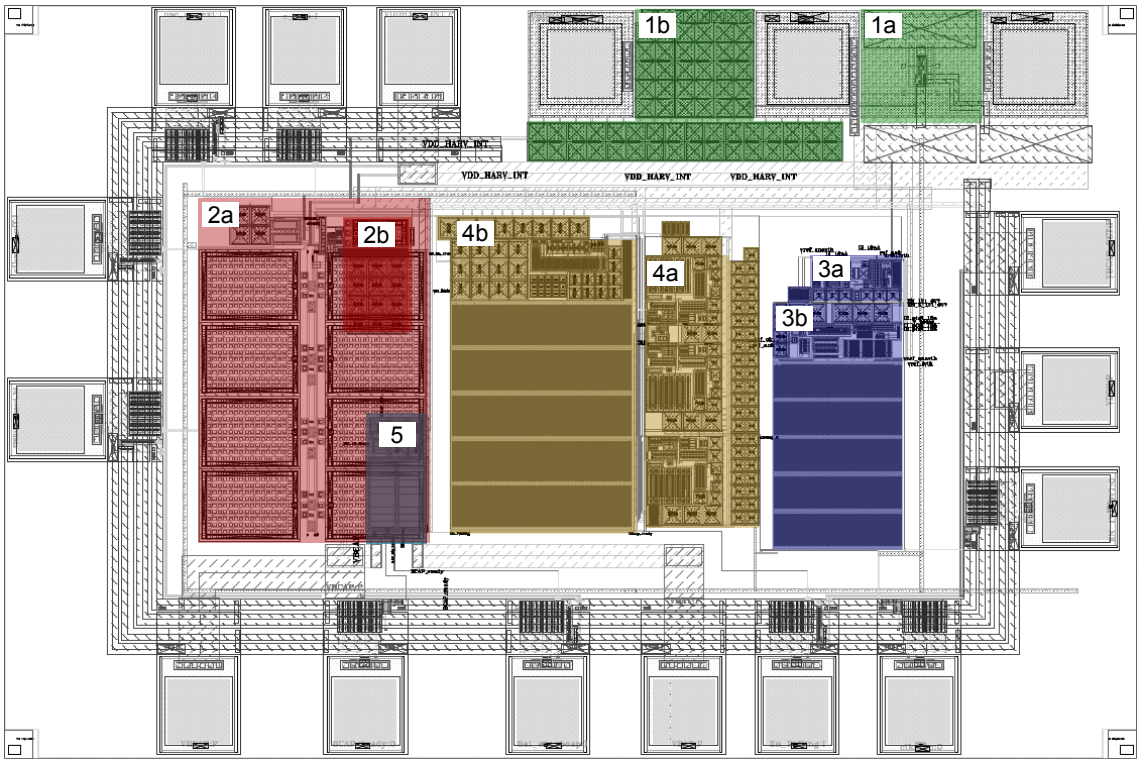

Figure A.1: Layout of the stand-alone version of the Electro-Magnetic Energy Harvester

1	**Power scavenging unit**
1a	3-stage single-ended rectifier
1b	Buffer capacitors
2	**DC/DC converter**
2a	Charge pump
2b	Voltage controlled oscillator
3	**Level detection unit 1**
3a	Level detectors
3b	Bias cell and reference
4	**Level detection unit 2**
4a	Level detectors
4b	Bandgap
5	**Output switch**

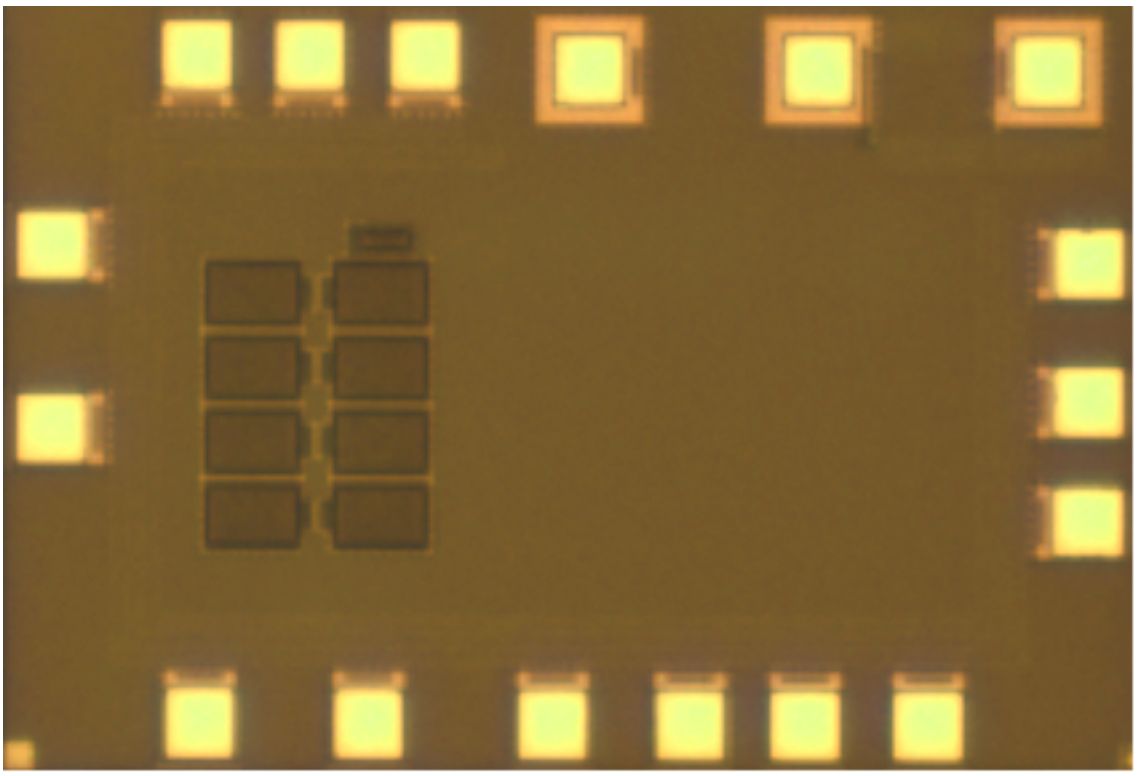

Figure A.2: Chip micrograph of the stand-alone version of the Electro-Magnetic Energy Harvester

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A.2 The Multifrequency Tag

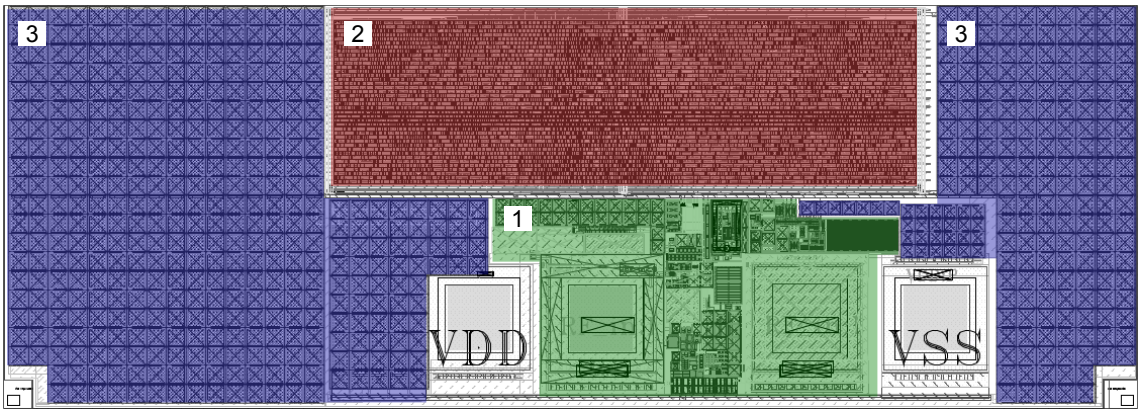

Figure A.3: Layout of the Multifrequency RFID Transponder

1	. . . . .	Analog frontend
2	. . . . .	Digital core
3	. . . . .	Buffer capacitors

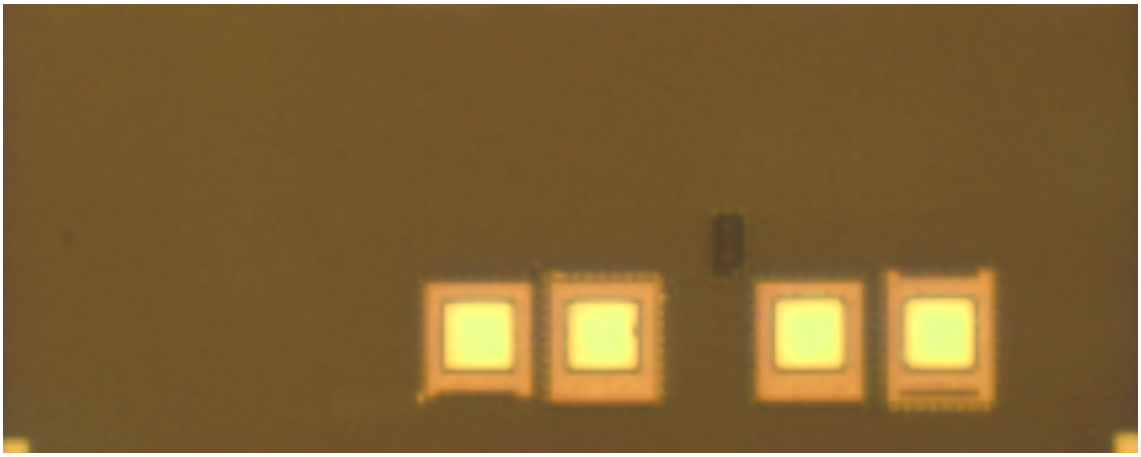

Figure A.4: Chip micrograph of the Multifrequency RFID Transponder

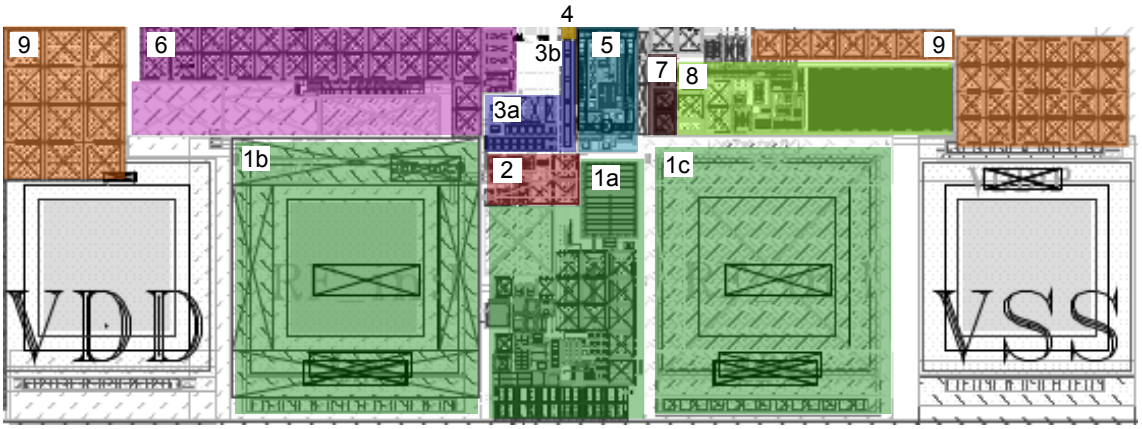

Figure A.5: Detailed layout of the analog frontend of the Multifrequency RFID Transponder

1	**Power scavenging unit, TX**
1a	HF & UHF rectifier, TX, shunt
1b	Coupling capacitors below L_A pad
1c	Coupling capacitors below L_B pad
2	**Frequency detection unit**
3	**HF clock unit**
3a	Clock recovery
3b	Clock divider
4	**Clock control unit**
5	**UHF clock oscillator**
6	**Demodulator**
7	**Power-on reset**
8	**Bias cell**
9	**Buffer capacitors**

A.3 The Multifrequency Sensing Tag

For test purposes the Multifrequency Sensing Tag has also been developed including just the on-chip sensor block as can be seen in Figure A.6. The layout of the Multifrequency Sensing Tag, as presented in Chapter 5, is shown in Figure A.9.

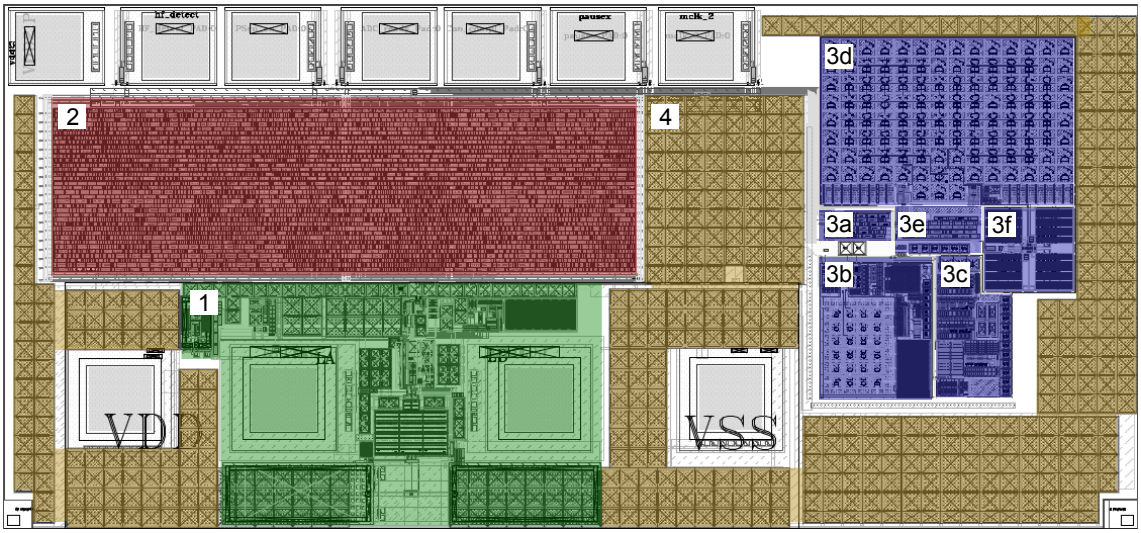

Figure A.6: Layout of the Multifrequency Sensing Tag without Off-Chip Sensor Interface

1	.....	**Analog frontend**
2	.....	**Digital core**
3	.....	**On-chip sensor, ADC**
3a	.....	Control unit
3b	.....	SC bandgap
3c	.....	Buffers
3d	.....	DAC capacitive array
3e	.....	SAR
3f	.....	Comparator
4	.....	**Buffer capacitors**

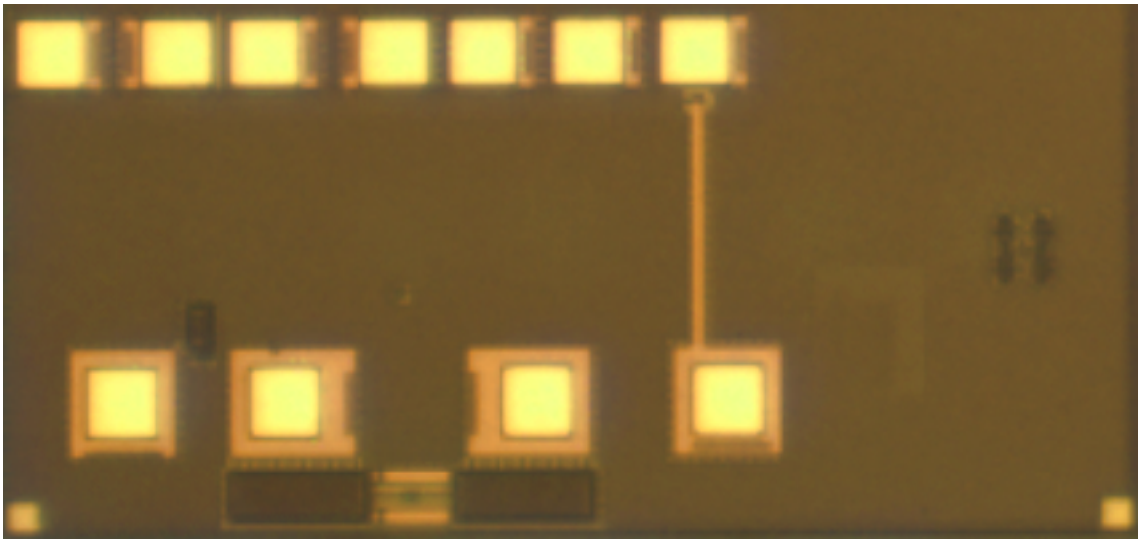

Figure A.7: Chip micrograph of the Multifrequency Sensing Tag without Off-Chip Sensor Interface

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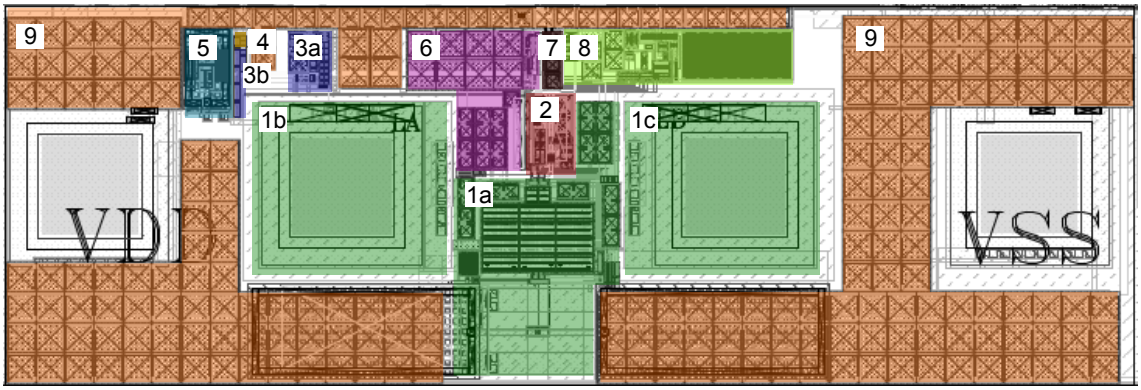

Figure A.8: Detailed layout of the analog frontend of the Multifrequency Sensing Tag

1	**Power scavenging unit, TX**
1a	HF & UHF rectifier, TX, shunt
1b	Coupling capacitors below L_A pad
1c	Coupling capacitors below L_B pad
2	**Frequency detection unit**
3	**HF clock unit**
3a	Clock recovery
3b	Clock divider
4	**Clock control unit**
5	**UHF clock oscillator**
6	**Demodulator**
7	**Power-on reset**
8	**Bias cell**
9	**Buffer capacitors**

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A.4 The iTire Chip

The layout shown in Figure A.9 contains the Electro-Magnetic Energy Harvester presented in Chapter 3 as well as the Multifrequency Sensing Tag presented in Chapter 5. Depending on external settings, the IC behaves either like the Electro-Magnetic Energy Harvester, or the Multifrequency Sensing Tag, or the iTire chip.

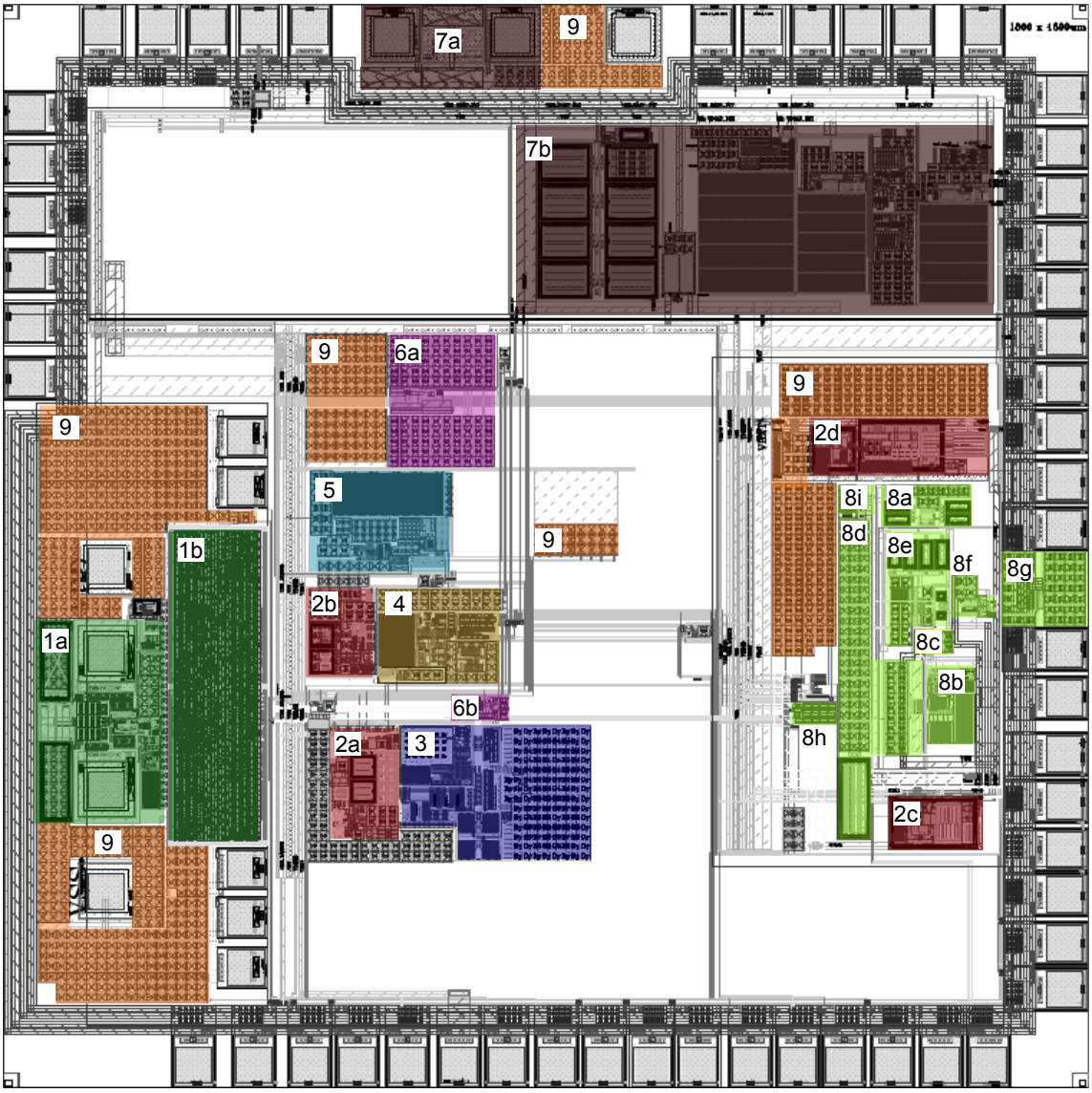

Figure A.9: Layout of the Multifrequency Sensing Tag without Off-chip Sensor Interface

1	**Multifrequency RFID interface**
1a	Analog frontend
1b	Digital core
2	**Voltage regulators**
2a	Regulator for the on-chip temperature sensor along with the ADC
2b	Regulator for the control unit
2c	Regulator for the carrier generation unit
2d	Regulator for the power amplifier
3	**Bandgap, ADC (details see Figure A.6, block 3)**
4	**Control unit**
5	**Bias cell**
6	**Power control unit**
6a	Supply distribution unit
6b	Isolation logic
7	**Energy harvester (details see Figure A.1)**
7a	Power scavenging unit
7b	DC/DC converter, LDU 1 & 2, Output switch
8	**Active transmitter**
8a	IQ oscillator
8b	BAW oscillator
8c	Frequency divider
8d	Frequency tuning
8e	Down-conversion mixer
8f	Differential amplifier and differential to single-ended conversion
8g	Power amplifier
8h	Serial data generation
8i	Bias cell
9	**Buffer capacitors**

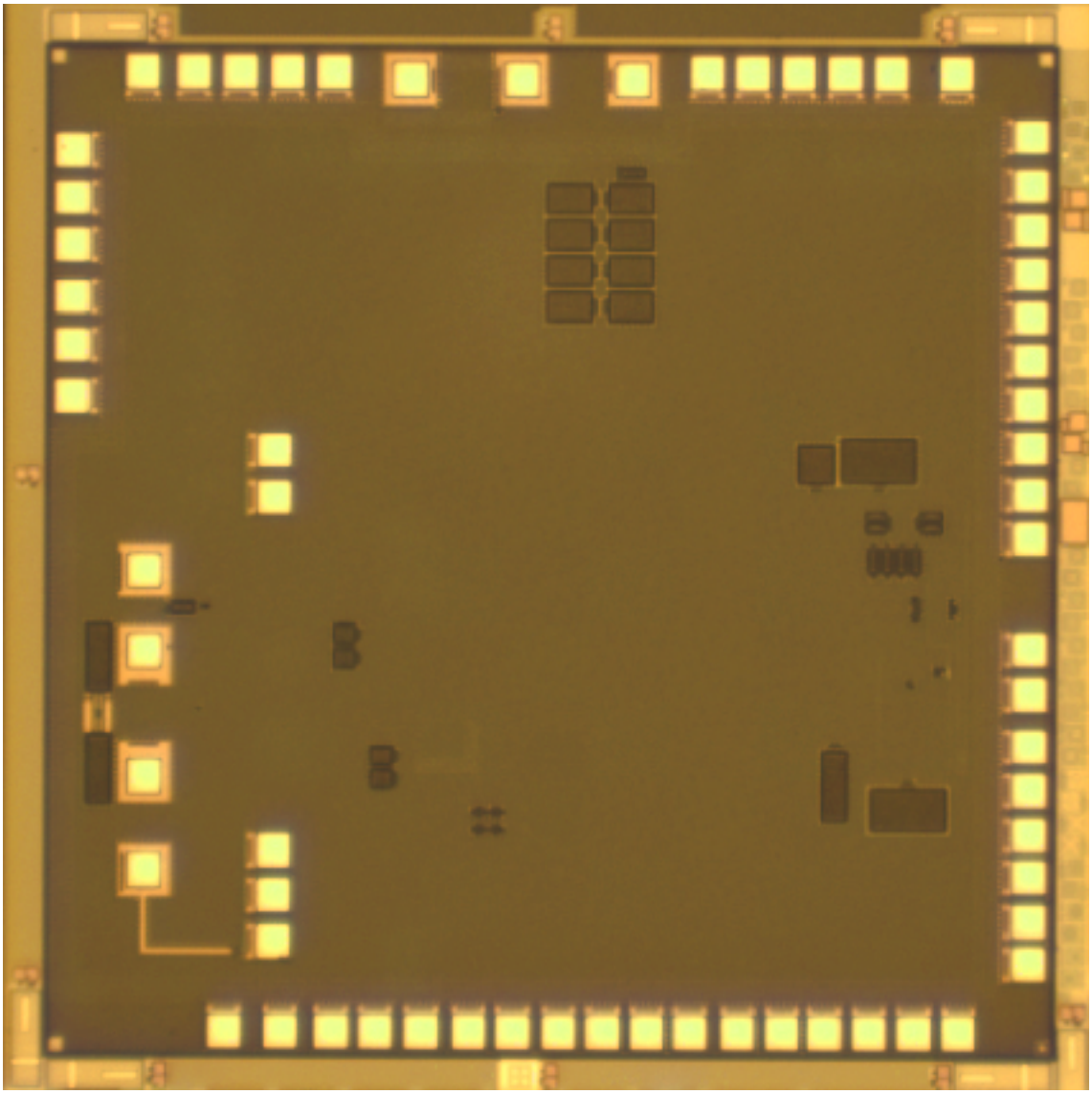

Figure A.10: Chip micrograph of the Multifrequency Sensing Tag without Off-chip Sensor Interface

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