Digital Demodulator Architecture of a Contactless Reader System for HF RFID Applications Supporting Data Rates up to 13.56 Mbit/sec

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Kurzfassung

Die *Radio Frequency Identification* (RFID) Technologie wird heutzutage bereits in sehr vielen unterschiedlichen Bereichen des alltäglichen Lebens erfolgreich eingesetzt, sei es im Warentransport (Objektidentifikation), bei der personenbezogenen Identifikation oder im Automobilbereich. Für konkrete Anwendungen, wie beispielsweise dem elektronischen Reisepass oder der *Near Field Communication* (NFC) Technologie (Nahfeldkommunikation), gibt es Bestrebungen, den Datendurchsatz und somit die Datenrate zu erhöhen. Konventionelle Kontaktlossysteme sind nach dem aktuellen Stand der Technik nicht in der Lage, hohe Baudraten (ab 848 kbit/sec) zu verarbeiten, da sowohl die analogen als auch die digitalen Komponenten eines Lesegerätes dafür nicht ausgelegt sind.

Die vorliegende Dissertation beschreibt die Konzeption und den Aufbau eines Lesegerätes für Kontaktlosanwendungen mit der primären Zielsetzung, höhere Datentransfers in kürzeren Übertragungszeiten zu ermöglichen. Das Lesegerät wurde durch ein FPGA-basierendes Prototypensystem realisiert, wodurch eine besonders hohe Flexibilität bezüglich der Implementierung und Validierung von unterschiedlichen Kodierungs- und Modulationsverfahren gegeben ist. Ein wichtiger Aspekt bzgl. hoher Baudraten ist die richtige Wahl der verwendeten Kodierungs- und Modulationsmethode. Diesbezüglich gibt es unterschiedliche Ansätze, wobei in dieser Arbeit neue Übertragungsmethoden für RFID-Systemen ausgearbeitet und erprobt wurden.

Ein weiteres Ziel der vorliegenden Arbeit war die Konzeption und Implementierung einer readerseitigen Empfangseinheit zur Verarbeitung hoher Datenraten. Ein wesentliches Konzeptionskriterium war, eine möglichst flexible und energieeffiziente Empfängereinheit zu entwickeln. Speziell der Einsatz in portablen Geräten (z.B. Mobiltelefon) für NFC-Anwendungen macht ein energieeffizientes Design unabdingbar. Die Flexibilität der Empfangseinheit bzgl. diverser Modulationsverfahren wurde erreicht, indem die gesamte Signalverarbeitung und die damit verbundene Demodulation des empfangenen Signals ausschließlich in der digitalen Domäne erfolgen. Die digitale Demodulation basiert einerseits auf einem im Rahmen dieser Dissertation entwickelten Algorithmus und andererseits auf der Unterabtastung. Diese Abtastmethode verletzt zwar die Regeln des Nyquist-Shannon'schen Abtasttheorems, jedoch kann das Verfahren auch bewusst zum Diskretisieren des Eingangssignals eingesetzt werden. Unter Verwendung eines A/D-Umsetzers wurde ein digitaler Abwärtsmischer realisiert. Zur Verbesserung der Signalqualität des empfangenen Signals wurde eine adaptive Regelung basierend auf einem *Least-Mean-Squares* (LMS) -Algorithmus implementiert. Die dadurch erzielte Trägerunterdrückung führte zu einer deutlichen Verbesserung der Empfangseigenschaften. Des Weiteren wurde eine Messmethode bzw. ein Auswerteverfahren für die Charakterisierung des Empfangssignals ausgearbeitet und beschrieben.

Laut aktuellen Forschungsberichten erreichen derzeitige Prototypensysteme Datenraten bis maximal 6,78 Mbit/sec. In dieser Arbeit wurde dank der ausgearbeiteten und implementierten Übertragungsmethode eine Verdoppelung der Datenrate erreicht. Somit werden mit dem aufgebauten Prototypen-Reader Übertragungsraten von bis zu 13,56 Mbit/sec zwischen Transponder und Lesegerät erreicht. Der Performancegewinn entspricht einer 16-fachen Erhöhung der derzeit standardisierten maximalen Datenrate von 848 kbit/sec.

Abstract

Nowadays the *Radio Frequency Identification* (RFID) technology is already used in a lot of different areas of everyday life. Especially HF-technologies have been successful in high volume applications for identification in access-control, for object identification and for automotive industry. Contactless applications like the electronic passport or the *Near Field Communication* (NFC) technology demand *Very High Data Rates* (VHDR) to increase the communication speed for higher volumes of exchanged data. However, higher data rates are currently a field of research. Conventional contactless systems are not able to support VHDR (above 848 kbit/sec), because the analog as well as the digital components of the contactless reader are not designed for these requirements.

This PhD thesis describes the design and development of the contactless prototyping reader system with the primary goal to support a higher data throughput within reduced transmission time. For the investigation of VHDR the prototyping reader system is based on a new concept of an FPGA-based reader prototyping system. This concept ensures a high level of flexibility regarding implementation and validation of different modulation and encoding schemes. An important aspect concerning VHDR is the correct selection of the implemented coding and modulation method. In this regard, various approaches can be taken. In the course of this thesis, new transmission concepts for RFID systems were developed and tested.

Another aim of this PhD thesis was the design and implementation of a reader side receiving unit for processing VHDR. An essential concept criterion was to design a very flexible and energy efficient digital receiver unit. Reduced power consumption is essential for portable battery powered devices like mobile phones which have integrated a contactless reader and support the NFC technology. The flexibility of the receiving unit concerning various modulations and coding schemes has been achieved insofar as the entire signal processing and the associated demodulation of the received signal take place exclusively in the digital domain. The digital demodulation is, on the one hand, based on an algorithm developed within the framework of this thesis and, on the other hand, on the undersampling. Certainly, this sampling method violates the rules of the Nyquist-Shannon sampling theorem; however, the procedure can be used consciously to process the input signal. The digital down conversion of the received HF signal (from passband to baseband) is realised by an A/D converter without any analog mixer. For the improvement of the signal quality of the received signal, an adaptive regulation was implemented which is based on *Least-Mean-Squares* (LMS) algorithm. The resulting carrier suppression will lead to a definite improvement of the receiving characteristic. Furthermore, a measuring and evaluation method was worked out for the characterization of the received signal.

According to current research reports, present contactless prototyping systems reach data rates up to 6.78 Mbit/sec. Due to the transmission method that was elaborated and implemented as part of the thesis, a duplication of the baud rate was reached. With the contactless prototyping reader system, transmission rates up to 13.56 Mbit/sec are reached between transponder and reader. Consequently, the performance gain concerning the data rate is 16 times higher than the currently standardized maximum data rate.

Acknowledgments

I would like to thank my supervisor Univ.-Prof. Dipl.-Ing. Dr.techn. Wolfgang Pribyl for his guidance and for giving me the opportunity to do this interesting and challenging research.

Especially, I thank Dipl.-Ing. Gerald Holweg from Infineon Technologies AG Austria, Graz, for his sustained support and for giving me the chance to complete my PhD thesis.

My most sincere thanks go to my mentor and advisor at Infineon, Dipl.-Ing. Walter Kargl, whose inspiring ideas and helpful discussions enhanced my research. I thank him for his guidance and continuous support during the development of this thesis.

I am really grateful to my colleagues Dipl.-Ing. Dr. Albert Missoni and Dipl.-Ing. Helmut Koroschetz for their valuable inputs. Furthermore, I would like to thank my project members and colleagues Dipl.-Ing. Matthias Emsenhuber, Dipl.-Ing. Matthias Pichler, Dipl.-Ing. Markus Auer and Udo Bachernegg for their helpful discussions and technical support.

Finally, I would like to express my deepest gratitude to my parents Anna and Edmund for providing me with love, a good education, support and inspiration. This thesis is dedicated to the memory of my father, Edmund Ehrlich.

Graz, July 2011 Edmund Ehrlich

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Nomenclature

100BASE-FX Fast Ethernet Standard (Optical Fiber)

100BASE-TX Fast Ethernet Standard (Cable)

4B5B 4 Binary, 5 Binary Coding

8-PSK Phase Shift Keying with eight phase states

ADC Analog Digital Converter

AFE Analog Front End

AFNOR Association francaise de normalisation

AGC Automatic Gain Control

ARM Advanced RISC Machine

ASK Amplitude Shift Keying

BER Bit Error Rate

BPSK Binary Phase Shift Keying

CDIP Ceramic Dual In-Line Package

CEA French Atomic Energy Commission

CEA Leti Electronics and Information Technology Laboratory of the CEA in French

CEPT Committee on European Postal Regulation

CMOS Complementary Metal Oxide Semiconductor

CRC Cyclic Redundancy Check

DAC Digital Analog Converter

DFT Discrete Fourier Transformation

DSP Digital Signal Processing

DUT Device Under Test

ECC Electronic Communications Committee

ECC Error Correction Code

ECMA European Computer Manufactures Association

EDC Error Detection Code

EMC Electromagnetic Compatibility

EMD Electromagnetic Disturbance

EOF End of Frame

EPC Electronic Product Code

ERC European Radiocommunications Committee

ETSI European Telecommunications Standards Institute

ETU Elementary Time Unit

EVM Error Vector Magnitude

FFG Oesterreichische Forschungsfoerderungsgesellschaft

FIFO First In First Out

FIR Finite Impulse Response

FPGA Field Programmable Gate Array

HDL Hardware Description Language

HF High Frequency

HPA High Power Amplifier

IEC International Electrotechnical Commission

IP Intellectual Property

ISI Intersymbol Interference

ISM Industrial, Scientific and Medical

ISO International Organization for Standardization

JTAG Joint Test Action Group

LF Low Frequency

LMA Load Modulation Amplitude

LMS Least Mean Square

LNA Low Noise Amplifier

LO Local Oscillator

LUT Look Up Table

MASK M-ary Amplitude Shift Keying

MER Modulation Error Ratio

MFM Modified Frequency Modulation

MPSK M-ary Phase Shift Keying

NFC Near Field Communication

NFCIP-1 Near Field Communication - Interface and Protocol

NRZ None Return to Zero

NRZ-L None Return to Zero Level

PCB Printed Circuit Board

PCD Proximity Coupling Device

PICC Proximity Integrated Circuit Card

PJM Phase Jitter Modulation

PLD Programmable Logic Device

PLL Phase Looked Loop

PLR Packet Loss Rate

PSK Phase Shift Keying

QAM Quadrature Amplitude Modulation

QPSK Quadrature Phase Shift Keying

RFID Radio Frequency Identification

RISC Reduced Instruction Set Computer

RMS Root Mean Square

RRC Filter Root Raised Cosine Filter

RSSI Received Signal Strength Indication

RX Receive

SDR Software Defined Radio

SDRAM Synchronous Dynamic Random Access Memory

SFR Special Function Register

SNR Signal to Noise Ratio

SOF Start of Frame

SRAM Static Random Access Memory

SRD Short Range Device

TX Transmit

UART Universal Asynchronous Receiver Transmitter

UHF Ultra High Frequency

USB Universal Serial Bus

VCO Voltage Controlled Oscillator

VGA Variable Gain Amplifier

VHBR Very High Bit Rates

VHDL Very High Speed Integrated Circuit Hardware Description Language

VHDR Very High Data Rates

VSA Vector Signal Analyzers

1 Motivation

1.1 Overview

For identification and personal tagging, the contactless smart card and the electronic passport are used very successfully in our everyday lives. Those passive applications work at the carrier frequency of 13.56 MHz, as standardized in ISO/IEC 14443, including data rates up to 848 kbit/sec and their typical operation distance ranges up to 10cm. In communication systems the tendency goes towards much higher data rates, but passive contactless applications nowadays have the big disadvantage of very low data rates and, therefore, do not satisfy the requirements for large amounts of data. To enable higher data transfers (in MByte area) in a shorter transmission time, efforts have been taken to increase the data rate for passive contactless applications. Data rates above 848 kbit/sec are called *Very High Bit Rates* (VHBR), or rather *Very High Data Rates* (VHDR). The VHBR subject is also discussed by the corresponding *Working Groups* (WG) of the ISO. Other semiconductor- and chip-card manufacturers like NXP or Gemalto have also been working on the same topic. As mentioned before, the topic VHDR in passive contactless applications is a current field of research. An important aspect concerning very high bit rates is the correct choice of the implemented coding and modulation method. In this regard, various approaches can be found and the main objective will be to find a common solution for the standardization regarding very high bit rates.
Two possible applications for VHDR are the *electronic passport* (e-Passport) and the *Near Field Communication* (NFC) technology. The e-Passport has already been used successfully for several years. Last year the new security passport with fingerprints was released, which is why more personal information has to be stored on the passport chip. Here, the introduction of VHDR would be very useful. Another interesting application field for very high data rates is the NFC technology, which preferably can be used in portable battery powered devices like mobile phones, cameras or notebooks. The near field technology enables a contactless data exchange via an electromagnetic field, without any kind of mechanical linkage. Due to the NFC technology a mobile phone can, for example, have the functionality of a contactless smart card and, consequently, can be used for transport ticketing, access control, payment etc. In addition, NFC also demands VHDR to increase communication speed for higher volumes of exchanged data. The problem of the existing contactless infrastructure (rather, the conventional reader) is that this does not support very high data rates (above 848 kbit/sec), because neither the analog nor the digital components of the contactless reader are designed to meet these requirements. However, as mentioned before, higher data rates are currently a field of research and there are already a lot of papers about this topic. All known prototyping systems are restricted to a communication speed of maximum 6.78 Mit/sec. It seems the upper limit and state of the art, because currently there is no real system known that is able to process higher data rates.
One thesis objective was the research and analysis of technical bottlenecks in passive contactless applications for both communication directions. This PhD thesis was a part of the research project *ReadRF*. This was a co-operation project between the Graz University of Technology and

Infineon Technologies Austria, Development Center Graz, subsidized by FFG (Oesterreichische Forschungsfoerderungsgesellschaft). The goal of the *ReadRF* project was the investigation of very high data rates in contactless systems by applying different coding and modulation methods. Figure 1.1 shows a very abstract and simplified block diagram of a contactless proximity coupled system. Within the framework of the *ReadRF* project three PhD theses, two diploma theses and one electronic project were carried out. A short description and assignment of the two diploma theses are given in chapter 3. The contactless proximity coupled system (in figure 1.1) is divided into three blocks, which are the main topics of the mentioned PhD theses. The first block comprises the *Contactless Reader* system, which is treated within this PhD thesis. The *Transmission Channel* was the topic of the PhD thesis of Walter Kargl, which covered different aspects of the air interface, e.g. the characteristics and behavior of the electro-magnetic coupling between the reader and the transponder system. The *Contactless Transponder* was realized via a prototype system, composed of a digital logic and a phase demodulator test chip, which was integrated into silicon. These activities were carried out as part of the PhD thesis by Markus Auer.

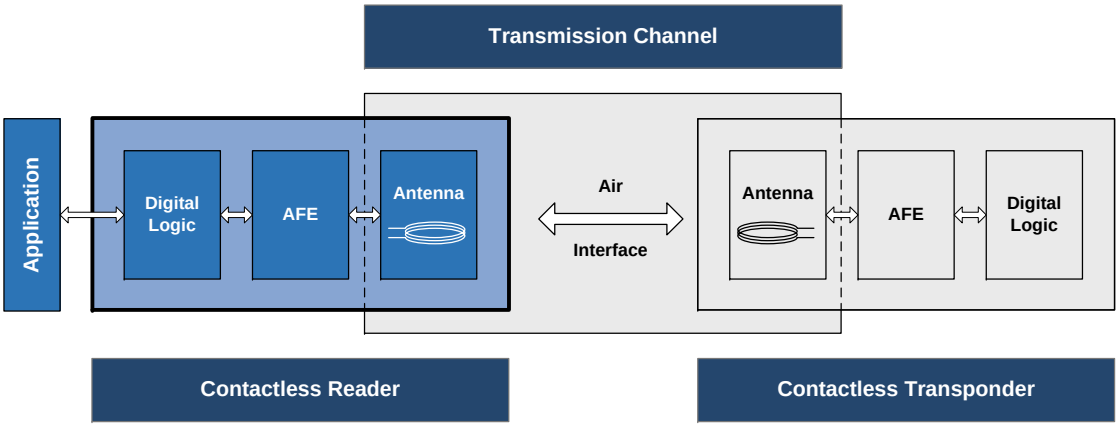


Figure 1.1: Block diagram of a contactless proximity coupled system

The aim of this PhD thesis was the design and development of a contactless prototyping reader system which supports VHDR. An essential concept criterion was the design of a very flexible and energy efficient digital receiver unit. Reduced power consumption is essential for portable battery powered devices like mobile phones which have integrated a contactless reader and support the NFC Technology as mentioned above. A digital receiving unit was designed and developed, which is based on the principle of undersampling and a specially elaborated algorithm.
With this method, a simple and energy efficient receiving method was developed. In addition, the support of various protocol standards was also a very important design and development criterion. The exploration makes use of an FPGA-based prototyping and evaluation board for the emulation of the contactless reader system. From the outset it was agreed that no silicon would be produced. However, already existing silicon from Infineon could be reused for this research project (especially ADC and DAC components), in the course of which several feasibility studies were conducted. Due to the elaborated and implemented uplink communication concept, the newly developed VHDR prototyping reader is able to receive bit rates up to 13.56 Mbit/sec, which is still 16 times faster than the currently defined standard. However, the prototyping reader should also be able to handle the current standardized data rates. Consequently, a downward

compatibility to the already existing RFID infrastructure is given. So far, no contactless proximity reader system has been known which supports the data rates mentioned above.

1.2 Thesis Outline

Chapter 2 (*Introduction to RFID Technology*) gives a short introduction of the RFID technology and shows the basic components of an RFID system. Additionally, a comparison of an RFID system and a passive contactless proximity system like a contactless smart card is given.

Chapter 3 (*System Overview*) describes the physical fundamentals of a contactless proximity system and gives the necessary background knowledge for the understanding of the problems and solutions as discussed in this PhD thesis. This chapter also presents an improved reader antenna concept for contactless proximity systems and its implementation.

Chapter 4 (*Transmission and Communication Concept*) describes the standardized transmission and communication methods which are used in passive contactless proximity systems. After a detailed discussion of some new proposals concerning higher data rates in contactless systems the elaborated and implemented transmission concept for very high data rates is presented.

Chapter 5 (*Transceiver Concepts and Architectures*) gives an overview and description of different applicable transmitter and receiver architectures in contactless proximity reader systems. The core topic of this paper, the digital design of a receiving unit, is explicitly described in this chapter. The implemented digital demodulation method is based on undersampling and a specially elaborated algorithm, to provide a simple and energy efficient receiving method. A detailed explanation of the implemented demodulation concept will be given in this chapter.

Chapter 6 (*Concept and Design of an FPGA-based prototyping Reader System*) gives a detailed description of the design of the implemented contactless reader hardware architecture. In addition, several hardware components and IP modules of the reader are discussed. A detailed explanation of the implemented demodulator and the algorithm for the demodulation process will be given.

Chapter 7 (*Simulation, Verification and System Measurements*) presents the verification results of the proposed and implemented contactless prototyping reader system, especially of the digital demodulation unit. However, this is preceded by a description of the simulation and measurement setup. In addition, a method for the characterization and evaluation of the received load modulated signal (for VHBR) , which was also elaborated, will be described in this chapter.

Chapter 8 (*Research Summary, Conclusion and Outlook*) gives a final summary and conclusion of the research work which was done in this PhD thesis. This section also addresses the five invention disclosures and patent applications which were elaborated within the framework of this thesis. In addition, the key facts of the PhD thesis are pointed out and a performance comparison to other prototyping systems is given.

2 Introduction to RFID Technology

This chapter gives a short introduction of the RFID technology and shows the basic components of an RFID system. Additionally, a comparison of an RFID system and a passive contactless proximity coupled system like a contactless smart card is given. Furthermore, descriptions and explanations of often used technical terms and abbreviations are given. The RFID technology encompasses an extremely wide range of different technical topics like analog and digital chip design and communication engineering. There is a whole body of relevant literature on RFID like books, conference papers and journal papers [27], [86].

2.1 Components of an RFID System

RFID technology represents the contactless and automatic identification of objects and living creatures by exchange of data via electromagnetic fields, without any kind of mechanical linkage. Contactless identification systems are already in use in different areas like transport of goods (e.g. logistics or individual transport), personal tagging (e.g. e-Passports or animal tracking), the automotive industry (e.g. remote control keys or immobilizers), access controls or contactless smart-cards. Basically, conventional RFID systems consist of a background system (e.g. PC or Terminal), a contactless reader and at least one transponder (label, tag or contactless Smart Card) which is attributed to a specific object or person.

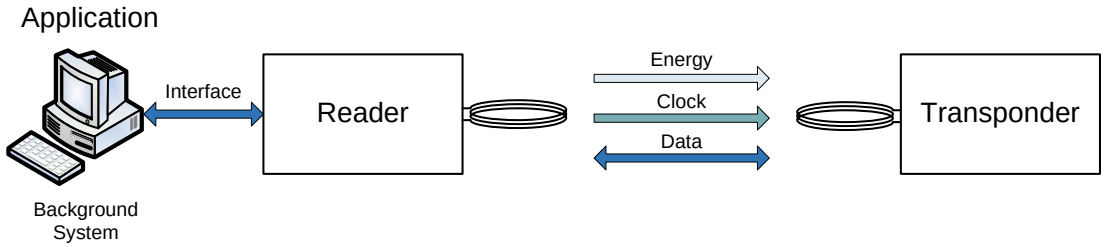


Figure 2.1: Components of an RFID System [27]

2.2 Fundamental Differentiation of RFID Systems

The RFID technology can be used in various applications, with the choice of the correct RFID system depending on the respective operational area. Beside the operating range, the carrier frequency and the coupling between reader and transponder are the main criteria for the distinction of RFID systems. In this section only the mentioned essential characteristics are discussed. The physical coupling between reader and transponder is based on electric, magnetic

and electromagnetic coupling and propagation. There are three *Industrial, Scientific and Medical* (ISM) frequency bands available for the RFID system: *Low Frequency* (LF, near 125 kHz), *High Frequency* (HF, 13.56 MHz) and *Ultra High Frequency* (UHF, 860-956 MHz). The achievable operating range depends on the coupling principle and the working frequency. Finally, the operating range is divided into three groups: *Close coupling*, *remote coupling* and *long range coupling*. Systems with a very small operating distance (up to 1cm) are known as close coupling systems. They are primarily used in applications with higher security requirements, as for electronic passport or contactless smart cards with payment functionality. Systems with operating ranges up to 1m are known as remote coupling or mid-range systems. They include proximity coupling systems (ISO 14443, contactless chip cards) and vicinity coupling systems (IOS 15693, smart label and contactless chip cards). The mentioned systems for the LF and HF ranges are based on magnetic coupling and use a carrier frequency of 125 kHz or 13.56 MHz. The third group are the long range systems which work with a carrier frequency of 868/915 MHz (Europe/USA) and have an operating range from 1m to approximately 10m.

2.3 Passive Contactless Proximity Systems Based on 13.56 MHz

The main differentiation criteria between the conventional RFID system and a contactless proximity system (e.g. contactless smart card or e-Passport) are shown in the following comparison:

RFID		**CL Smart Card**
up to 10m	**Read Range**	$<$10cm
LF, HF, UHF	**Frequencies**	HF
ISO15693, ISO18000,...	**Standards**	ISO14443
$\approx 0.2mm^2$	**Chip Area**	$\approx 2mm^2$
μW	**Power Consumption**	mW
No	**Security**	Yes

Table 2.1: RFID versus Contactless Smart Card [95]

Another important differentiation factor of RFID systems is the power supply of the transponder. Active transponders have a battery which supplies the power for the operation of the chip. By contrast, passive transponders do not have their own power supply and therefore all power must be drawn from the electromagnetic field of the reader. Passive contactless proximity applications in the HF (13.56 MHz) area, with a range up to 10 cm, are based on the product standard ISO/IEC 14443 [42] . All activities within the scope of the present PhD thesis are based on passive contactless proximity systems. According to the standard ISO/IEC 14443, the term *Proximity Coupling Device* (PCD) denotes the contactless reader and the term *Proximity Integrated Circuit Card* (PICC) defines the contactless transponder. Another term which is quite often used in this paper is the word *Downlink*. This describes the data communication from the reader to the contactless transponder. The opposite data communication direction is called *Uplink*. The physical coupling between PCD and PICC is based on electromagnetic coupling with the carrier signal being used to transmit clock and power. The carrier frequency shall be $13.56\,MHz \pm 7\,kHz$

and the operating field lies between $H_{min} = 1.5A/m$ and $H_{max} = 7.5A/m$. Figure 2.2 shows the basic components of a passive contactless proximity system. Beside the background system (Terminal/Host) and the block diagram of the reader, a simplified equivalent circuit diagram of the reader antenna circuit and the transponder is represented. Detailed information concerning the mentioned topics is given in the following chapters.

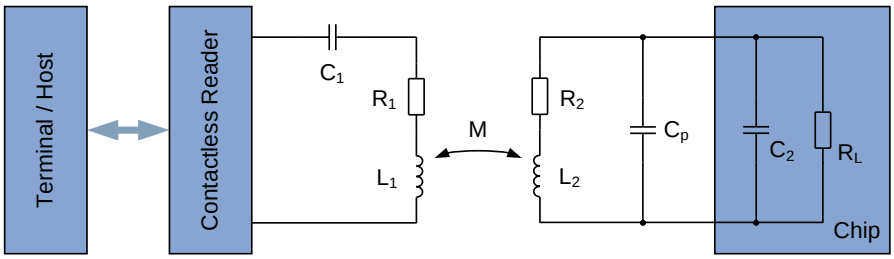


Figure 2.2: Simplified equivalent circuit diagram of a passive contactless proximity system [27]

3 System Overview

Figure 3.1 displays a block diagram of the complete contactless prototyping system, including the reader, the sending and receiving circuits as well as the contactless transponder. In the diploma thesis of Matthias Emsenhuber [23], the physical interface of readers was dealt with and new analog receiver concepts were investigated. Furthermore, antennas, power amplifiers, sending and receiving circuits were realized in hardware. The passive contactless transponder was also realized via a prototype system, composed of a digital part *Field Programmable Gate Array*(FPGA) and a phase demodulator test chip which was integrated into silicon. These activities were carried out as part of the PhD thesis by Markus Auer [10], [8]. The diploma thesis of Matthias Pichler [79] describes the implementation of a digital demodulation unit which supports data rates up to 6.8 Mbit/sec. The aim of this PhD thesis was the design and development of a contactless prototyping reader which supports very high data rates up to 13.56 Mbit/sec. The activities of Matthias Emsenhuber and Matthias Pichler were a great and helpful support for the present PhD thesis. This chapter provides the physical fundamentals of the contactless technology and thus give background knowledge for the understanding of the problems and solutions which are discussed in this PhD thesis.

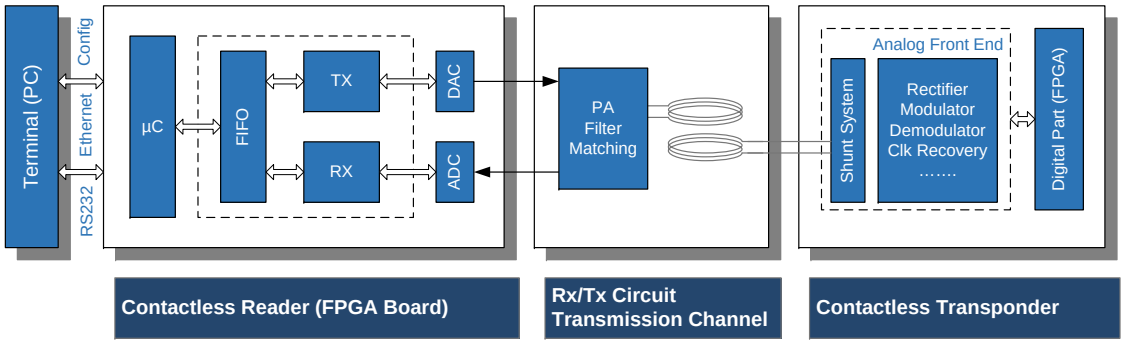


Figure 3.1: System Architecture

3.1 Air Interface

The air interface comprises the reader antenna as well as the transponder antenna. The energy transfer from reader to transponder and the data transmission in both communication directions are carried out across the transmission channel. An improvement of the energy supply (increase the operating range) is contrary to the data rate performance. To accomplish a larger operating range, a better energy transfer is required. Therefore, the reader antenna circuit is extended to a resonant circuit with a higher quality factor. However, an increase of the quality factor will

cause a limitation of the bandwidth and, consequently, a reduction of the achievable data rate. This chapter addresses the mentioned fundamentals like resonance and quality factor to promote understanding of the problems and elaborated concepts discussed in the present thesis. For further information concerning the air interface I would like to refer to the diploma thesis of Matthias Emsenhuber [23].

3.1.1 Resonant Circuit

Figure 3.2 shows a simplified equivalent circuit diagram of a reader antenna which consists of an inductance L_1 and a resistor R_1. For a maximum current the equivalent circuit is extended by the serial capacitance C_1 to obtain a second order serial resonant circuit. The serial resonant circuit is tuned to a resonance frequency which is equal to the carrier frequency of 13.56 MHz.

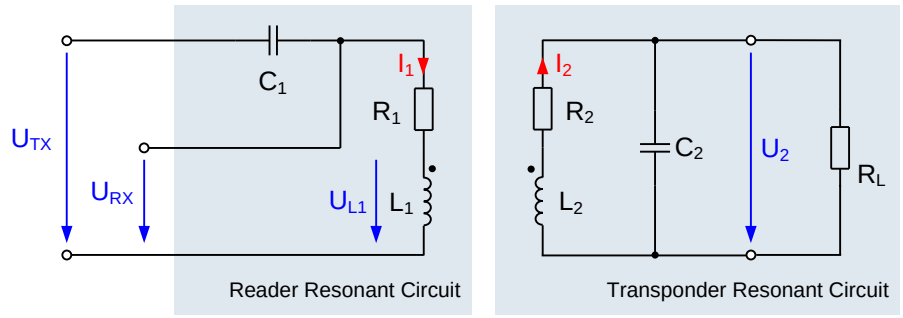


Figure 3.2: Equivalent circuit diagram of the PCD and PICC [23],[27]

$$Z_{ant} = R_1 + i \cdot \omega \cdot L_1 + \frac{1}{i \cdot \omega \cdot C_1} \tag{3.1}$$

In the case of resonance the voltages U_{L1} and U_{C1} have the same value and, consequently, the resistor R_1 is the only limited element:

$$i \cdot \omega \cdot L_1 = \frac{1}{i \cdot \omega \cdot C_1} \Rightarrow Z_{ant} = R_1 \tag{3.2}$$

A minor part of energy is lost across the resistor R_1 by thermal dissipation. The remaining energy portion oscillates between the inductance L_1 and the capacitance C_1. The ratio of those portions is denoted by the quality factor Q:

$$Q = \frac{\omega_r \cdot L_1}{R_1} \tag{3.3}$$

If $U_{L1} = U_{C1}$ (Resonance):

$$Q = \frac{1}{\omega_r \cdot C_1 \cdot R_1} \tag{3.4}$$

Due to the resonance magnification, an improvement of the energy efficiency (energy transfer from reader to transponder) and, consequently, of the operating range is achieved. A resonant circuit is specified by the resonance frequency and the quality factor Q. The resonance magnification of the voltage is proportional to the quality factor Q. Figure 3.3 shows the bode diagram

(Voltage and Phase) of a serial resonant circuit for the quality factors Q =10, Q= 20 and Q=30. The quality factor and, consequently, the resonance magnification can be limited by the series resistance R_1.

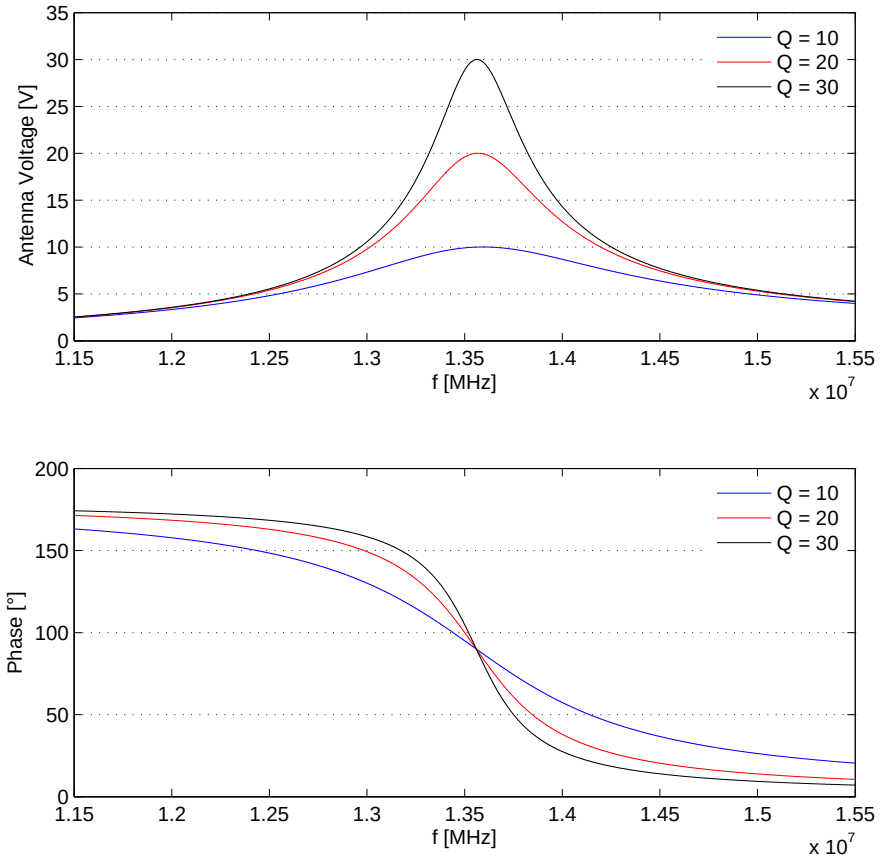


Figure 3.3: Voltage and Phase Characteristic at the Transmit Antenna for Q=10, Q=20 and Q=30

An increase of the quality factor results both in improvement of the energy supply (operating range) and in a reduction of the bandwidth. A detailed description of the quality factor and the correlation between energy supply, operation range and achievable bandwidth will be given in the next section.

3.1.2 The Quality Factor Q

One of the most important parameters of the resonant circuit (reader antenna) is the quality factor Q. The maximum achievable data rate is defined by the frequency regulations of the respective standards and the quality factor of the reader antenna. This factor influences the transmission behavior and, hence, affects the main properties of the system (energy coverage, data coverage, bandwidth, spectrum, and data rate). It is defined as:

$$Q = \frac{2 \cdot \pi \cdot Energy\ Stored}{Average\ Energy\ Dissipated\ per\ Cycle} \tag{3.5}$$

That means that the factor Q is $2 \cdot \pi$ times the ratio of the total energy stored divided by the energy lost within one cycle [49], [95]. Quality factor and reachable bandwidth are linked by indirect proportional coherence

$$Q = \frac{f_{res}}{B} \tag{3.6}$$

which means that high quality implicates low bandwidth, hence a smaller frequency spectrum. In case of modulation, the amplitude envelope (in the time domain) of the serial resonant circuit (reader antenna) can be described by an exponential function [28], [29], [30]. The falling and rising edges of the envelope are described by:

$$u_F(t) = U \cdot e^{\frac{-t}{\tau}} = U \cdot e^{-t \cdot \frac{2 \cdot f_C \cdot \pi}{Q}} \tag{3.7}$$

$$u_R(t) = U \cdot \left(1 - e^{\frac{-t}{\tau}}\right) = U \cdot \left(1 - e^{-t \cdot \frac{2 \cdot f_C \cdot \pi}{Q}}\right) \tag{3.8}$$

$$Q_B = \tau \cdot 2 \cdot \pi \cdot f_C \tag{3.9}$$

The mentioned transient behavior of the voltage U_{L1} (pulse shapes) can be seen in figure 3.4 for the quality factors Q =10, Q= 20 and Q=30. The figure shows that resonant circuits with higher quality factors need more time to reach the steady state. A reduction of the quality factor of the PCD is recommended in [99].

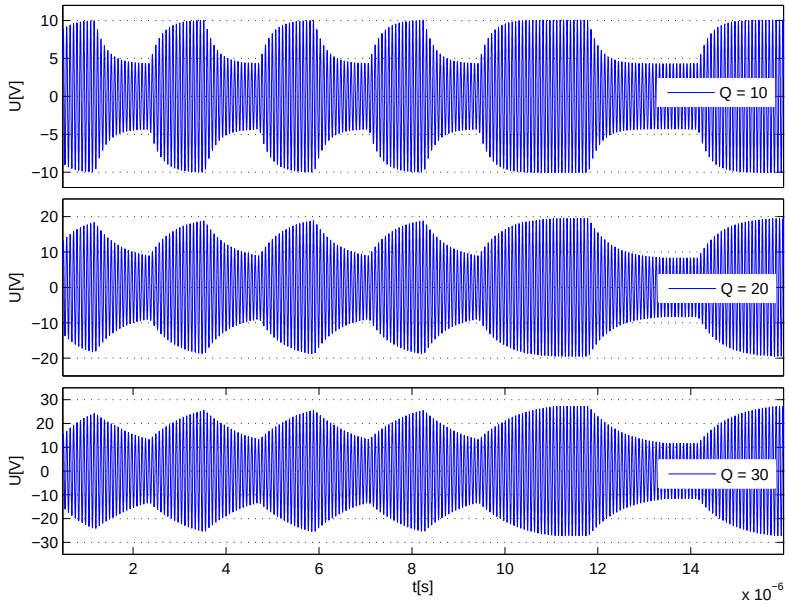


Figure 3.4: ASK modulation with 40% modulation index (Q=10, Q=20 and Q=30)

3.1.3 Characteristic of the Magnetic Field

Short cylindrical coils or conductor loops are used as reader antennas to generate the magnetic field. The positioning of reader and transponder antenna to each other can be *coplanar* or *coaxial*. Further considerations are based on the *coaxial* arrangement, which means that the reader and transponder antenna are parallel to each other and the center of both antennas is on the same axis (x-axis). Figure 3.5 shows the path of the magnetic field strength H depending on the distance in the x-direction. Additionally, the transition from near to far field is depicted. The field which is generated by the conductor loop begins at the antenna and at first is a purely magnetic field. With increasing distance a transformation into an electromagnetic field takes place. The transition point from near to far field can be calculated as follows:

$$d_{Near-Field/Far-Field} = \frac{\lambda}{2 \cdot \pi} = \frac{c}{2 \cdot \pi \cdot f} = \frac{3 \cdot 10^8}{2 \cdot \pi \cdot 13.56 \cdot 10^6} = 3.521m \tag{3.10}$$

At this distance, the electromagnetic field leaves the reader antenna and wanders into space in the form of an electromagnetic wave. Subsequently, a magnetic feedback of the transponder to the reader antenna is not possible any longer, i.e. the transition point from near to far field represents an upper range limit for inductive coupled systems.

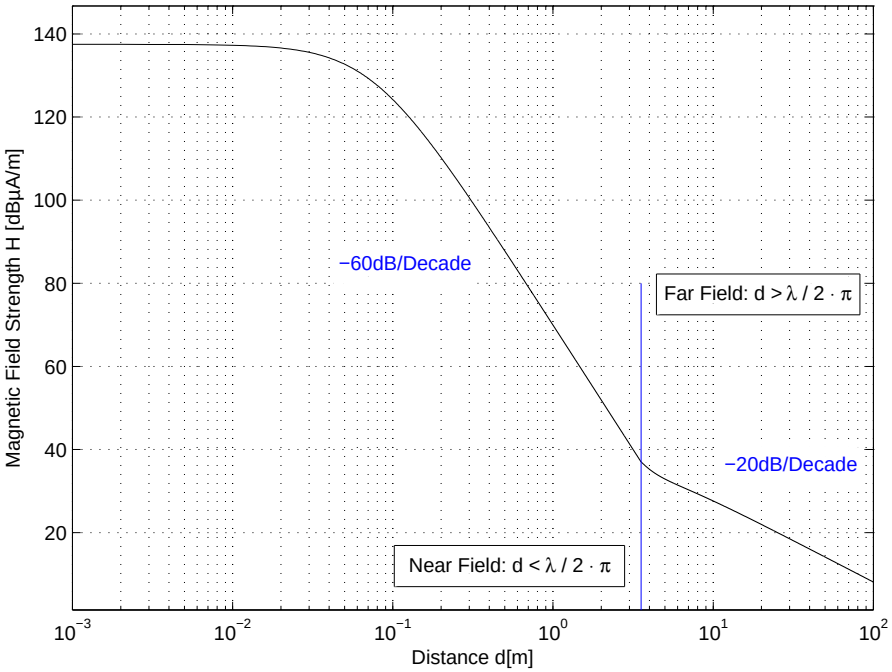


Figure 3.5: Graph of the magnetic field strength H depending on the distance (x-axis)

According to figure 3.5 the magnetic field remains constant up to a certain distance and then the field strength declines with 60dB/decade within the near field area. Afterwards, the decay in the far field area is 20dB/decade. Basically, there are two methods for the analytic calculation of the magnetic field:

- Magnetic Moment
- Biot - Savart's Law

For detailed information let me refer to the relevant literature [27], [28], [97]. An approximation of the magnetic field for the near field is given by

$$H_{NearField} = \frac{N \cdot I}{2} \cdot \frac{r^2}{(\sqrt{r^2 + d^2})^3} \tag{3.11}$$

N: Number of windings of the reader antenna [-]
I: Current through the reader antenna [A]
r: Radius of the reader antenna [m]
d: Distance from the center of the reader antenna in the x direction [m]

The electromagnetic field in the far field can be calculated the following way:

$$H_{FarField} = \frac{A \cdot I}{4 \cdot \pi} \cdot \sqrt{\left(\frac{1}{d^3} - \frac{\omega^2}{d \cdot c^2}\right)^2 + \left(\frac{\omega}{c \cdot d^2}\right)^2} \tag{3.12}$$

A: Area of the reader coil [m^2]
I: Current through the reader antenna [A]
c: Speed of light [m/s]
d: Distance from the center of the reader antenna in the x direction [m]
ω: Angular frequency [1/s]

Those two formulas are used in section 3.4 to calculate the graph of the magnetic field. This is relevant for the emission limitations of RFID reader systems as regards the magnetic field strength.

3.2 Load Modulation

The data communication from PICC to PCD is based on a so-called *Load Modulation*. Figure 3.6 shows the equivalent schematic of a reader antenna circuit and a contactless transponder. The coupling of those two antenna circuits are based on the magnetic field, which is described by the mutual inductance M. The reader antenna generates a magnetic field which induces a voltage U_{Q2} in the transponder coil. Consequently, this voltage causes a current i_2 which generates a magnetic field in the transponder coil. This magnetic field feedbacks to the field of the reader.

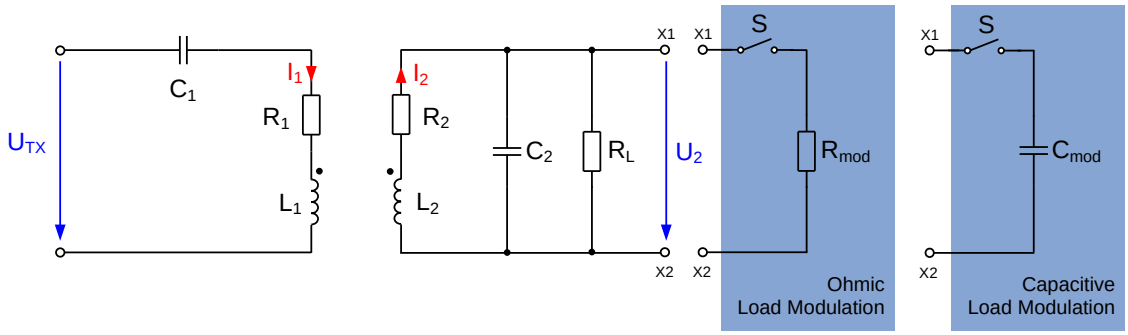


Figure 3.6: Equivalent circuit diagram with ohmic and capacitive load modulation [27]

The load modulation is performed by a variation of circuit parameters at the transponder, which causes a variation of the transponder impedance. Usually, a distinction of an *ohmic* and a *capacitive* load modulation takes place, with use of an ohmic load modulation in a passive proximity system. Due to the mutual inductance M a variation of the current i_2 also causes a variation of the current i_1 which can be detected by the receive unit of the reader. Because of the loose coupling between the transponder antenna and the reader antenna the detected signal on reader side is significantly smaller than the carrier signal. The ratio of carrier signal to the received signal amounts to 80dB, which represents a great challenge to the receive unit. For this reason,

the load modulation in proximity systems is based on a *subcarrier* which represents a two stage modulation. Figures 3.7 and 3.8 show this principle in the time domain as well as in the frequency domain. In the present product standard for contactless proximity systems (ISO/IEC 14443 [42]), a subcarrier frequency of 847.5 kHz ($f_c/16$ with $f_c = 13.56MHz$) is used, which makes it possible to separate the respective wanted signal (data) better from the carrier signal. In the first step, the subcarrier is modulated by the coded baseband data. Afterwards, the load modulation of the carrier with the modulated subcarrier takes place. The load modulation process generates two spectral lines which are symmetrically placed around the spectral line of the carrier. The sidebands of the subcarrier contain the baseband data. The separation of the subcarrier (with the related sidebands) from the carrier signal will relax requirements for the receive unit of the reader enormously [27], [60].

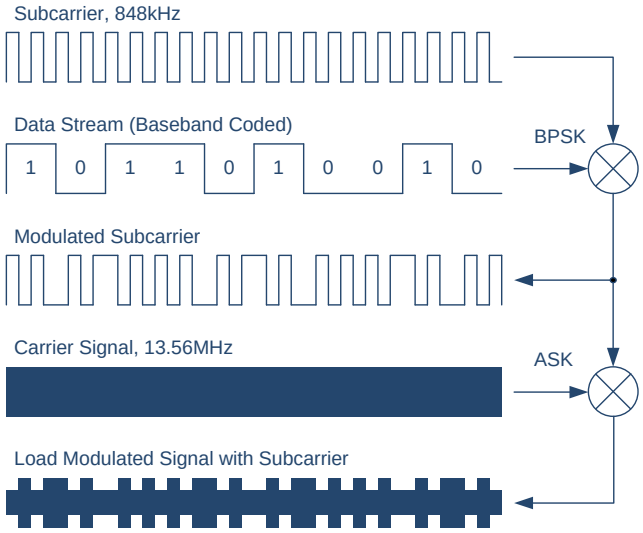


Figure 3.7: Principle of load modulation in the time domain (Two stage modulation) [27]

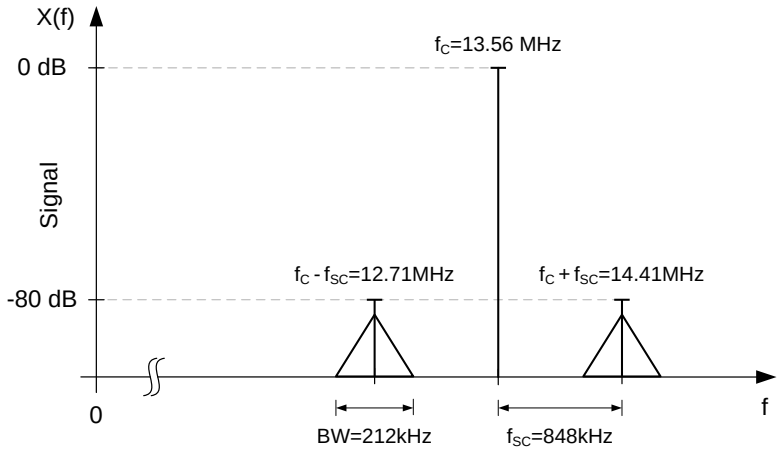


Figure 3.8: Principle of load modulation in the frequency domain (Two stage modulation) [27]

3.3 Reader Antenna

This chapter addresses the antenna concept of a contactless reader system. Due to the reader antenna, the electromagnetic field for energy supply of the transponder is generated as well as the data transmission in both communication directions is performed. There are two challenges concerning the uplink. Firstly, as mentioned above, the loose coupling between the transponder antenna and the reader antenna causes a receive signal strength which is significantly smaller than the carrier signal. And secondly, a higher quality factor Q of the resonant circuit influences the reception behavior of the receive path. Especially the latter will be discussed in this chapter; moreover, two different concepts will be introduced whereby a comparison of a conventional and an improved antenna concept will be given.

3.3.1 Conventional Antenna Concept

In a conventional reader system the antenna voltage U_{RX} (see figure 3.2) is used for the demodulation of the load modulated carrier signal. At first the carrier signal at 13.56 MHz is suppressed by a notch filter and the remaining sidebands, which contain the baseband data, are amplified. This method suppresses the carrier signal; however, the influence of the quality factor will not be eliminated. Afterwards the sidebands are demodulated by an extended envelope detector or an I/Q demodulator to obtain the baseband data [23]. Figure 3.9 shows the reader reception signal (time and frequency domain) as it can be found in conventional reader systems. Nevertheless, the antenna arrangements of those conventional contactless readers are not applicable for reader systems which should support very high data rates [23].

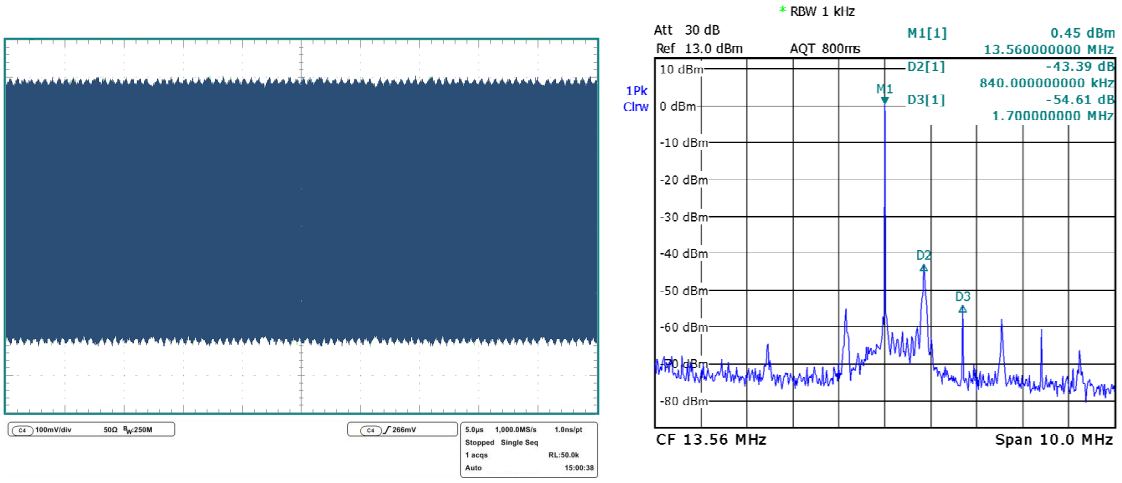


Figure 3.9: Measurements of a load modulation with a conventional antenna arrangement (time and frequency domain)

3.3.2 Improved Antenna Concept

There exist several concepts and solutions to optimize the communication performance of the air interface, especially the signal quality of the received antenna signal. A carrier suppression realized by a very narrow band-stop filter can be found in [99]. With those crystal based band-stop filters a stop-bandwidth of 6 kHz is achievable. This filter approach and further methods like the use of coil antennas or separate receiver antennas are published in [97]. The provision of VHBR requires the elimination of the influence of the quality factor caused by the resonant circuit (reader). This topic was investigated in the diploma thesis of Matthias Emsenhuber [23]. An increased quality factor of the resonant circuit results in *Inter Symbol Inference* (ISI), which limits the data rates enormously. Different concepts also were implemented and the basic principle will be discussed hereafter [53]. To eliminate the influence of the quality factor, an antenna arrangement with two sense coils was elaborated. The fundamental concept is based on measurement methods for PICC, standardized in ISO/IEC 10737-6 [43]. The measurement and characterization of the load modulation caused by a PICC is carried out by a measurement tower, which consists of a transmission, a sense and calibration coil (see figure 3.10, left side). Figure 3.10 on the right shows the equivalent circuit diagram of the test assembly which equals a measurement bridge.

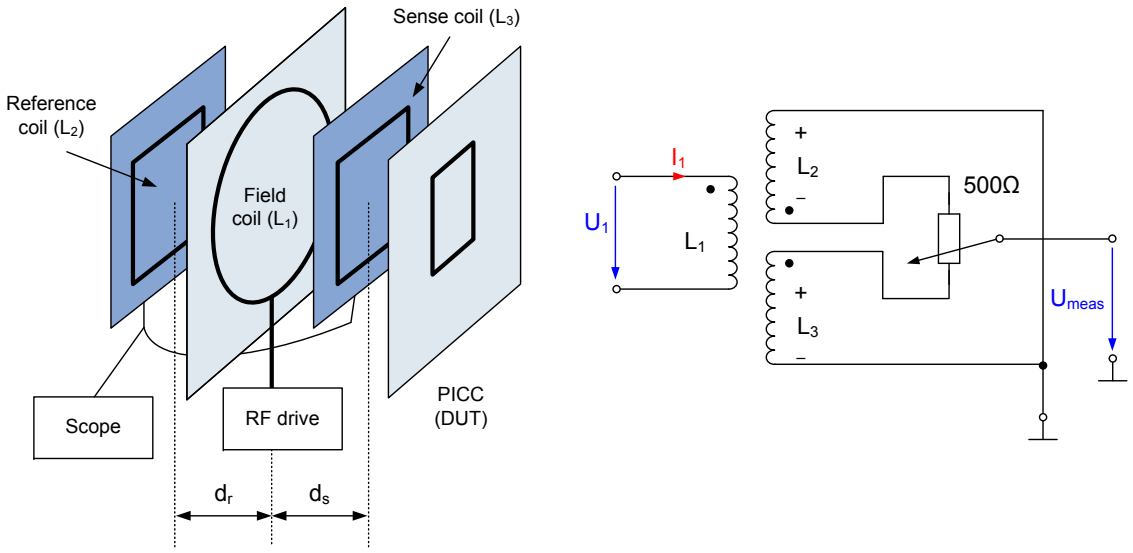


Figure 3.10: Mechanical arrangement and equivalent circuit diagram of the measurement bridge for measuring the load modulation of a PICC [27]

The reference coil and sense coil are placed at the same distance around the transmission antenna. If no PICC is placed within the operation range, the two coils are induced by the equal magnetic field and, consequently, the strong carrier is compensated. This compensation also happens if a PICC is placed inside the operating range near the sense coil. Due to the load modulation, the PICC generates a magnetic field which induces a voltage into the sense coil. However, the reference coil is not influenced by the magnetic field generated by the PICC. Because of the symmetrical arrangement of the measurement bridge, an improved signal quality of the load modulation is reached. The concept of the test assembly (measurement tower) is

adapted for the prototyping contactless reader, whereby the three coils (transmit, reference and sense coil) are placed on one plane. Figure 3.11 shows the described antenna arrangement whose functionality is based on the same principle as the measurement tower. This does not represent the final solution, as the second sense coil was eliminated for geometrical reasons. Instead of the voltage induced by the eliminated second sense coil, another measurement quantity is required for compensation. For instance, the current through the transmission antenna (measured indirectly via the voltage drop across a resistance) can be used for compensation. Instead of the antenna current also the antenna voltage can be used. A detailed description can be found in [23].

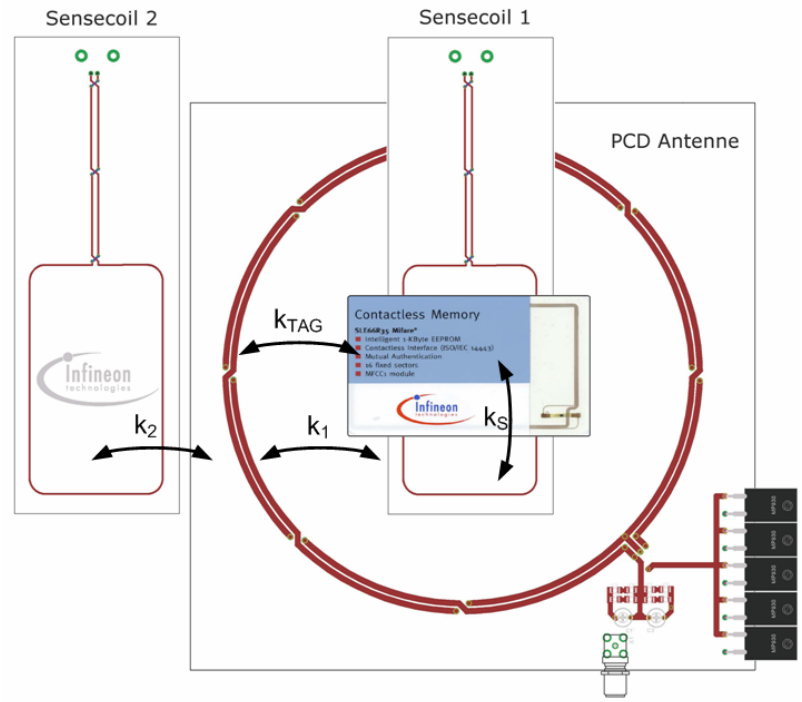


Figure 3.11: New, improved antenna arrangement placed on one plane [23]

Figure 3.12 shows the receive signal which was achieved by the new, improved reception circuit and antenna arrangement. A satisfactory improvement of reception quality, not only time-wise but also frequency-wise, could be achieved. With the presented method the receive path will neither be influenced by the resonant circuit nor by the quality factor. Effective carrier suppression (carrier cancellation) is carried out by an adaptive control technique which is based on a *Least Mean Square* (LMS) algorithm. The functionality and implementation of LMS algorithms is discussed in chapter 6.6.

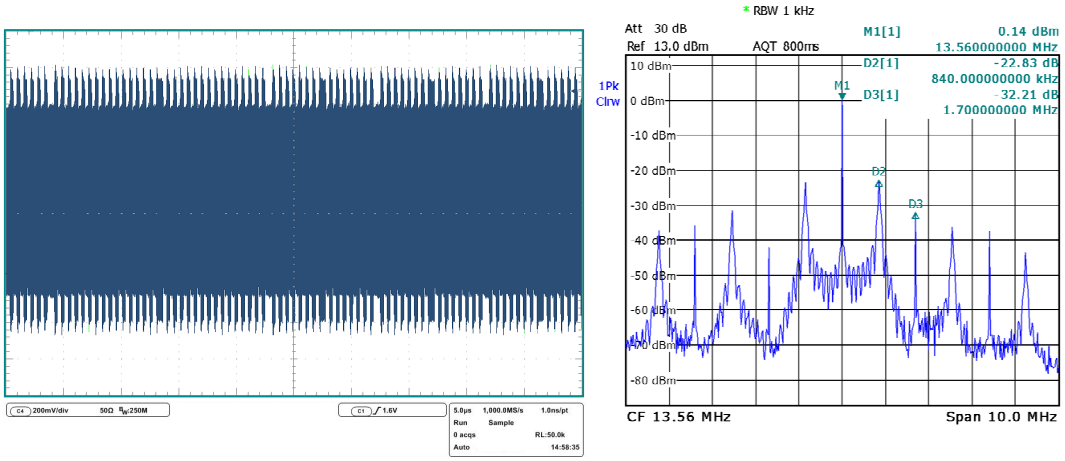


Figure 3.12: Measurements of a load modulation with an improved antenna concept (time and frequency domain)

3.4 Standards and Regulations

As mentioned before, the maximum achievable data rate is defined by the quality factor of the reader antenna and, furthermore, by the frequency regulation. The electromagnetic waves which are sent out by the reader are limited by regulative norms. For particular ISM frequency bands, the maximum radiation of radio waves is defined by the utilization of frequency masks. These normative restrictions present great challenges for basic circuit technology. The thresholds (spectral bandwidth, power limits, duty cycle or channel spacing etc) for RFID reader systems (*Short Range Device*, SRD) are specified in the harmonized standard TR 70-03 (CEPT/ERC REC) [16]. Accordingly, the measuring principles are defined under the EN 300 330 norm (ETSI) [25]. Figure 3.13 shows the emission limits of the HF field (for ISO/IEC 14443, ISO/IEC 15693 or ISO/IEC 18000-3). For the carrier signal at 13.56 MHz, a maximum electromagnetic field strength of $60\,dB\mu A/m$ (at a distance of 10 meters) is allowed. An appropriate frequency mask limits the emitted side bands which result from the modulation by the PCD. Both the modulation index of the ASK and the phase shift of the PSK modulation directly affect side bands. Consequently, the multilevel/M-ary ASK (MASK) or rather, the PSK modulation and, therefore, the very high data rates are restricted.

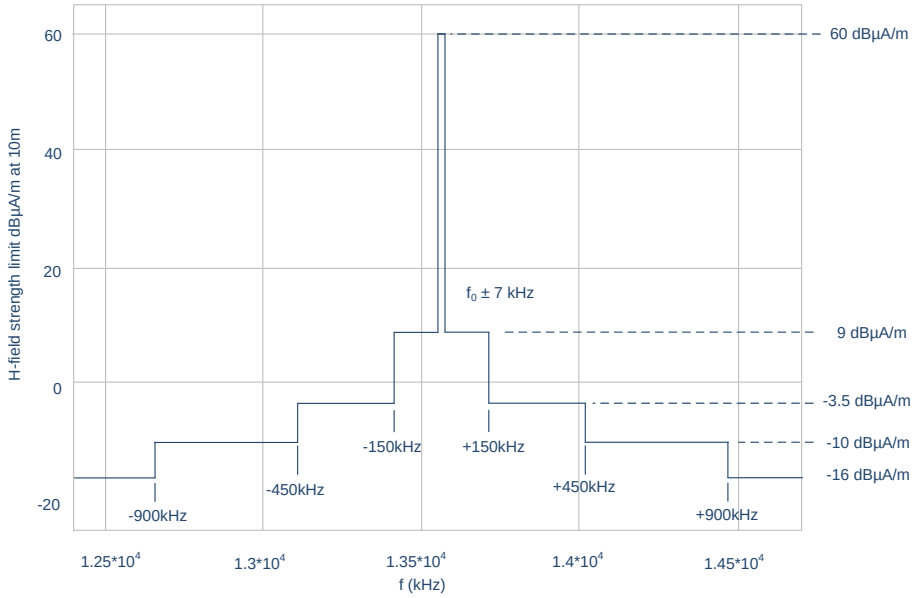


Figure 3.13: Emission Limits for HF

The nature of the magnetic field in the near and far field (see section 3.1.3) is essential for the field regulation of RFID reader systems. For this reason, two important calculations are presented in the following:

Calculation of the Maximal Antenna Current for a Given Antenna Geometry

First of all, the magnetic field strength $H_{(d=3.521m)}$ is calculated for the distance d=3.521m, which is the transition point from *near* to *far* field [59].

$$\begin{aligned} H_{(d=3.521m)} &= H_{(d=10)} + 20 \cdot [log(10) - log(3.521)] \\ &= 60dB\mu A/m + 9.066679dB\mu A/m \\ &= 69.066679dB\mu A/m \\ &= 0.00284A/m \end{aligned}$$

The geometry of the reader antenna (radius r = 0.075m) is given. With the following equation the maximum antenna current can be calculated. The resulting field strength fulfils the spectrum regulation regarding the standard TR 70-03.

$$\begin{aligned} N \cdot I &= \frac{2 \cdot H_{(d=3.521)} \cdot (\sqrt{r^2 + d^2})^3}{r^2} \\ &= \frac{2 \cdot 0.000284 \cdot (\sqrt{0.075^2 + 3.521^2})^3}{0.075^2} \\ &= 44.10979A \end{aligned}$$

For a distance d = 0 the magnetic field strength is:

$$\begin{aligned} H_{(d=0)} &= \frac{N \cdot I}{2 \cdot r} = \frac{44.10979A}{2 \cdot 0.075m} \\ &= 294.0653A/m = 169.36887dB\mu A/m \end{aligned}$$

The reader antenna with a radius r = 7.5 cm and an antenna current I = 44.109 A (N=1 Windings) radiates an electromagnetic field strength of $60\,dB\mu A/m$ at 10 metres distance. This represents the maximum antenna current to fulfil the spectrum regulations.

Calculation of the Magnetic Field Strength in a Distance of 10 Meters for a Given Antenna Geometry and Antenna Current

The magnetic field strength in a distance of 10 metres is calculated for an antenna current of I=1.125 A (H=7.5 A/m) as well as I=2.25 A (H=15 A/m) at a given antenna geometry.

I = 1.125 A;r = 0.0075 m;H = 7.5 A/m

$$\begin{aligned} H_{(d=0)} &= 7.5A/m \\ &= 20 \cdot \log(7.5 \cdot 10^6) \\ &= 137.5dB\mu A/m \end{aligned}$$

$$\begin{aligned} H_{(d=3.521)} &= \frac{N \cdot I}{2} \cdot \frac{r^2}{\left(\sqrt{r^2 + d^2}\right)^3} \\ &= \frac{1.125}{2} \cdot \frac{0.075^2}{\left(\sqrt{0.075^2 + 3.521^2}\right)^3} \\ &= 72.43\mu A/m = 37.2dB\mu A/m \end{aligned}$$

$$\begin{aligned} H_{(d=10)} &= H_{(d=3.521)} - 20 \cdot [\log(10) - \log(3.521)] \\ &= 37.2dB\mu A/m - 9.066679dB\mu A/m \\ &= 28.132dB\mu A/m = 25.5\mu A/m \end{aligned}$$

I = 2.25 A;r = 0.0075 m;H = 15 A/m

$$\begin{aligned} H_{(d=0)} &= 15A/m \\ &= 20 \cdot \log(15 \cdot 10^6) \\ &= 143.52dB\mu A/m \end{aligned}$$

$$
\begin{aligned}
H_{(d=3.521)} &= \frac{N \cdot I}{2} \cdot \frac{r^2}{\left(\sqrt{r^2 + d^2}\right)^3} \\
&= \frac{2.25}{2} \cdot \frac{0.075^2}{\left(\sqrt{0.075^2 + 3.521^2}\right)^3} \\
&= 144.87 \mu A/m = 43.22 dB\mu A/m
\end{aligned}
$$

$$
\begin{aligned}
H_{(d=10)} &= H_{(d=3.521)} - 20 \cdot [\log(10) - \log(3.521)] \\
&= 43.22 dB\mu A/m - 9.066679 dB\mu A/m \\
&= 34.152 dB\mu A/m = 51.01 \mu A/m
\end{aligned}
$$

The graphic results of the calculations above are shown in figure 3.14. The maximum field strength characteristic is illustrated by the red curve and observes the spectrum regulation. The black and the blue curves show the field characteristic for field strength of 15 A/m and 7.5 A/m. Figure 3.15 shows the characteristic of the field strength for a different antenna geometry. The curves in both plots are based on the two equations 3.11 and 3.12.

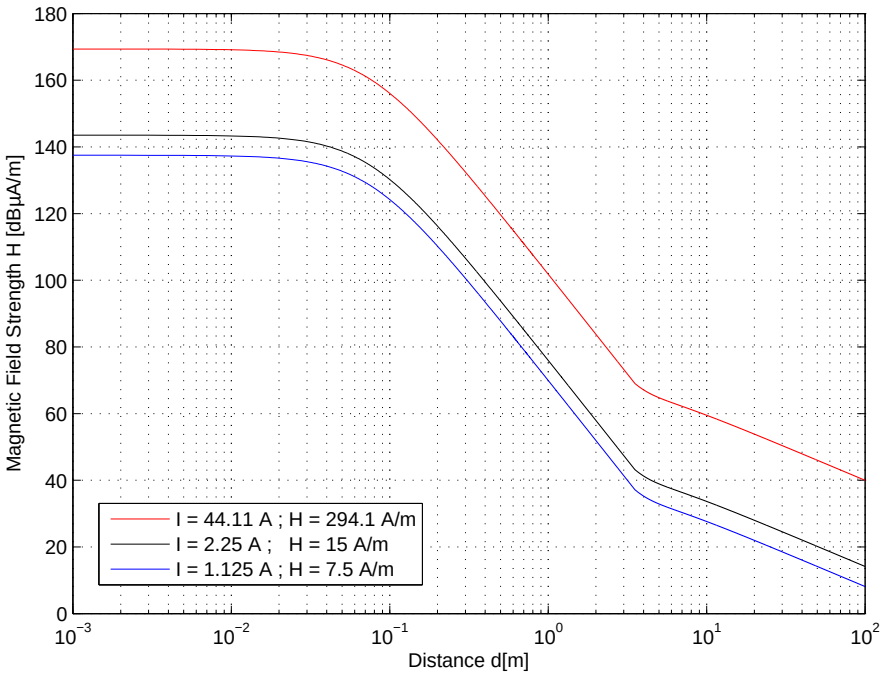


Figure 3.14: Magnetic field characteristic for different antenna currents

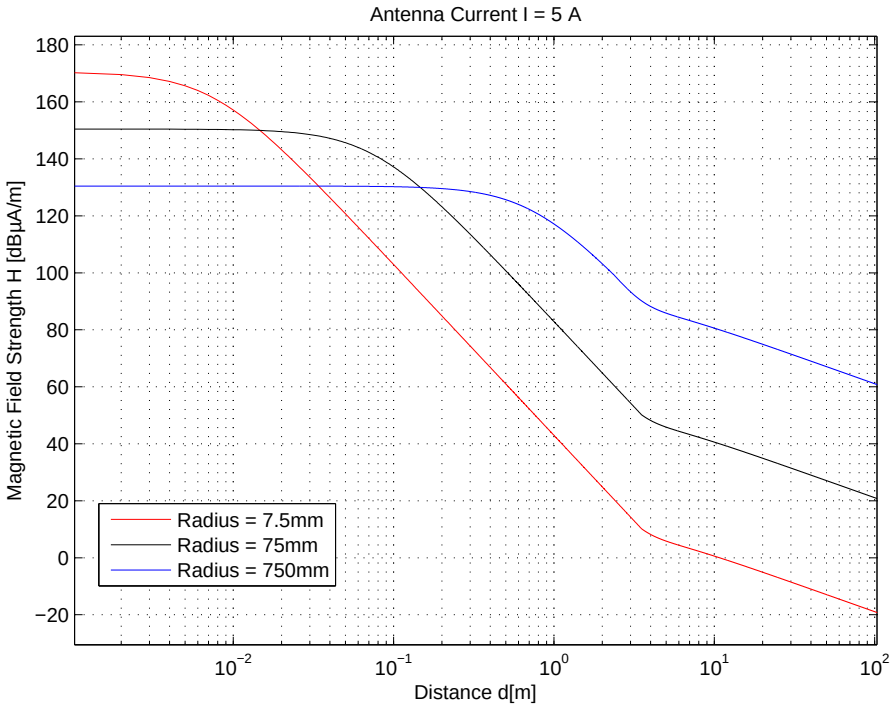


Figure 3.15: Magnetic field characteristic for different antenna geometry

4 Transmission and Communication Concept

This chapter discusses the transmission and communication concept which is used in passive proximity systems. As mentioned before, the communication between PCD and PICC is divided into the *downlink* and the *uplink*. First of all, a short introduction of the current product standard for contactless proximity systems is given; especially the coding and modulation methods are discussed. There are several ISO *Working Groups* (WG) which discuss new proposals and standards concerning very high data rates in contactless systems. This section will give a short overview of the proposed methods. The essential aim of the present thesis was the design and development of a contactless prototyping reader which supports VHDR. In addition, a new communication concept for the uplink had to be worked out. This section will concentrate on the PCD to PICC communication and describe the elaborated and implemented transmission concept for the uplink.

4.1 Downlink

4.1.1 State of the Art

Contactless applications like electronic passports are based on the product standard ISO/IEC 14443 [42]. The standard contains four parts and defines two different communication modes (Type A and B). Part 2 includes the current definition of the encoding and modulation methods for the data exchange between PCD and PICC. The relevant information concerning encoding and modulation methods for the downlink is summarized in table 4.1. The Type A communication interface uses a Modified Miller baseband encoding and a 100% ASK modulation with the mentioned coding scheme warranting a stable power supply of the PICC. However, the Type B interface is realized by a *Non Return to Zero* (NRZ) baseband encoding and a 10% ASK modulation. Today the standard defines data rates of 106/212/424 and 848 kbit/sec. As is standard, all values of data rates are rounded in this thesis. The clock frequencies for the different data rates are derived from the carrier frequency $f_c = 13.56\,MHz$. So the exact data rates are: 105.94 kbit/sec ($f_c/128$), 211.88 kbit/sec ($f_c/64$), 423.75 kbit/sec ($f_c/32$), 847.5 kbit/sec ($f_c/16$).

	Type A	Type B
Baseband Encoding	Modified Miller	NRZ
Modulation	ASK 100%	ASK 10%
Data Rate	106-848 kbit/sec	106-848 kbit/sec

Table 4.1: Coding and modulation methods for the downlink (ISO/IEC 14443)

4.1.2 ISO Proposals of Very High Data Rates

Japan Proposal (“WG8N859”)

This proposal [44] recommends a reduction of the bit time, which is a very simple and effective method to increase the data rate. Figure 4.1 shows the minimization of the bit time in the time domain and table 4.2 lists the associated possible data rates. A reduction of the bit time by factor two leads to a doubling of the data rate. However, now the rise and fall time must be calculated more exactly.

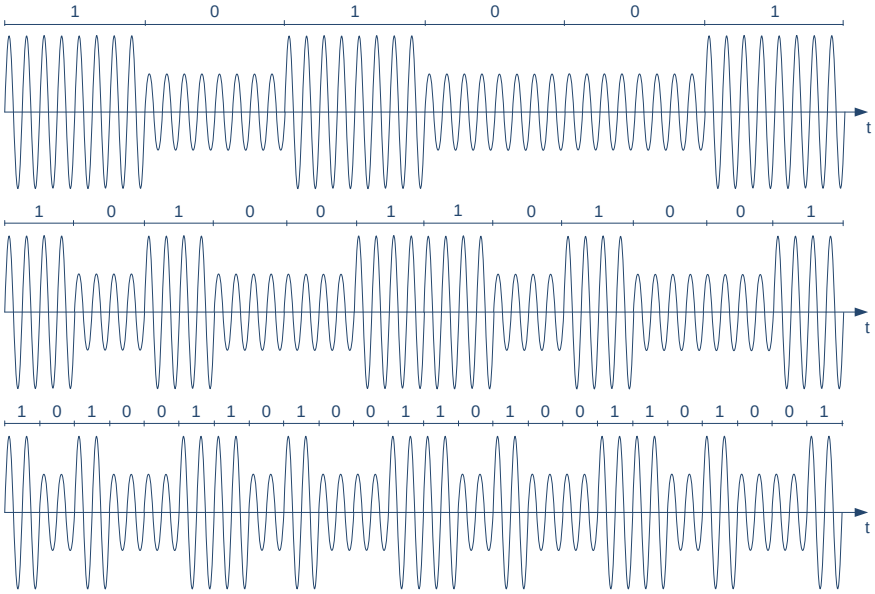


Figure 4.1: Bit time reduction (Japan Proposal)

Bit Duration	μsec	$128/f_c$ 9.44	$64/f_c$ 4.72	$32/f_c$ 2.36	$16/f_c$ 1.18	$8/f_c$ 0.59	$4/f_c$ 0.295	$2/f_c$ 0.147	$1/f_c$ 0.074
Data Rate(rounded)	kBit/sec	106	212	424	848	1 696	3 392	6 780	1 3560

Table 4.2: Bit time reduction (Japan Proposal)

Philips Proposal (“WG8N865”)

For the increase of the data rate this proposal suggests a phase modulation (*Phase Shift Keying*, PSK) directly on the 13.56 MHz carrier. Figure 4.2 shows an example of a *Binary Phase Shift Keying* (BPSK) modulation (180° phase changes) of the carrier signal. Table 4.3 illustrates different phase shifts in dependence on the symbol duration. It is shown that a higher number of phase states and reduction of the symbol time lead to a higher data rate. A reduction of the symbol time leads to a faster performance growth concerning VHDR than a higher number of

phase states. One advantage of the phase modulation technique is the relatively constant power transfer from reader to the transponder [78].

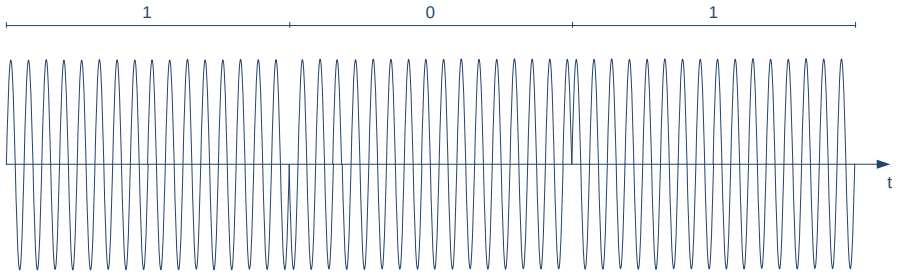


Figure 4.2: Phase modulation (Philips Proposal)

Symbol-Duration	Phase Shift							
μsec	180°	90°	45°	23°	12°	6°	3°	1,5°
128/f_c=9.44	106	212	318	424	530	636	742	848
64/f_c=4.72	212	424	636	848	1 060	1 272	1 484	1 696
32/f_c=2.36	424	848	1 272	1 696	2 120	2 544	2 968	3 392
16/f_c=1.18	848	1 696	2 544	3 392	4 240	5 088	5 936	6 784
8/f_c=0.59	1 695	3 390	5 085	6 780	8 475	10 170	11 865	13 560
4/f_c=0.295	3 390	6 780	10 170	13 560	16 950	20 340	23 730	27 120

Table 4.3: Phase modulation (Philips Proposal) — Data rate in kBit/sec (rounded)

AFNOR Proposal (“WG8N862”)

The present AFNOR (Association francaise de normalisation) proposal [1] suggests using more levels for the amplitude modulation instead of a 2-*Amplitude Shift Keying* (ASK) modulation, as it is defined in the ISO/IEC 14443 standard. With multilevel/M-ary ASK (MASK) (Figure 4.3) high data rates are also obtainable, but only in connection with some disadvantages. This modulation scheme is very sensitive concerning signal distortion and an increasing modulation index would reduce the energy supply of the transponder. To advance the communication speed of the air interface, it is necessary to increase the number of amplitude levels. A comparison between the data rate and the number of amplitude levels or bit duration is given by table 4.4.

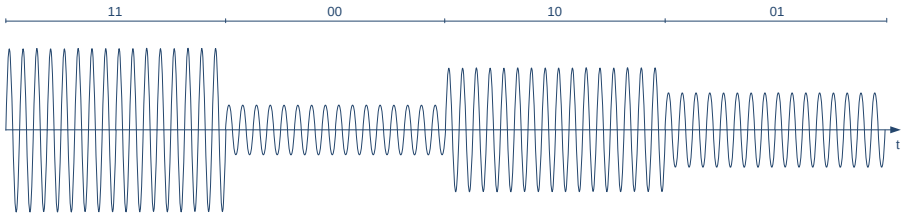


Figure 4.3: Multilevel ASK (AFNOR Proposal)

Number of Levels	Symbol Duration (μsec)				Coding
	128/f_c=9,44	64/f_c=4,72	32/f_c=2,36	16/f_c=1,18	
2	106	212	424	848	1 bit/symbol
4	212	424	848	1695	2 bit/symbol
8	318	636	1271	2543	3 bit/symbol
16	424	848	1695	3390	4 bit/symbol

Table 4.4: Multilevel ASK (AFNOR Proposal) — Data rate in kBit/sec (rounded)

Proposal from Gemalto, CEA Leti and Raisonance

The proposal recommends a multi-phase modulation of the carrier which yields to a good trade-off between channel bandwidth and remote energy capabilities. These two characteristics are significant for passive applications where a transfer of power and data takes place. The proposed method increases the data rate without increasing the required bandwidth. A phase modulation also causes a variation of the amplitude of the carrier. This kind of amplitude modulation is not desired because of the possible chip reset and clocking loss on PICC. To avoid high variations of the carrier amplitude, two modulation features have been introduced. The first one is the limitation of the phase excursion to $\pm 90°$ which, additionally leads to a reduction of the emitted frequency spectrum. The second is the subdivision of the phase shift over four carrier periods which yields to a smooth phase transition. Figure 4.4 shows the constellation diagram with a different number of phases.

A simulation result in figure 4.5 shows a comparison of a conventional PSK (phase shift within one carrier period) and the proposed PSK in which the phase shift is subdivided into four carrier periods. Simulation assumptions: Quality factor of the reader antenna Q = 5, N = 2 phase states, $\Delta\varphi = 90°$, symbol duration $t_{symbol} = 590nsec$ (8 carrier periods per symbol) and a symbol frequency – in that case also the data rate – of $f_{symbol} = 1.695MHz$ ($f_c/8$). Table 4.5 illustrates different phase shifts depending on the symbol duration, with a higher number of phase states leading to a higher data rate. With passive application, the symbol time is restricted to eight carrier periods. For active peer-to-peer application the phase excursion is not limited and the symbol time (*Elementary Time Unit*, ETU) could be reduced (marked gray in the table 4.5) [14].f

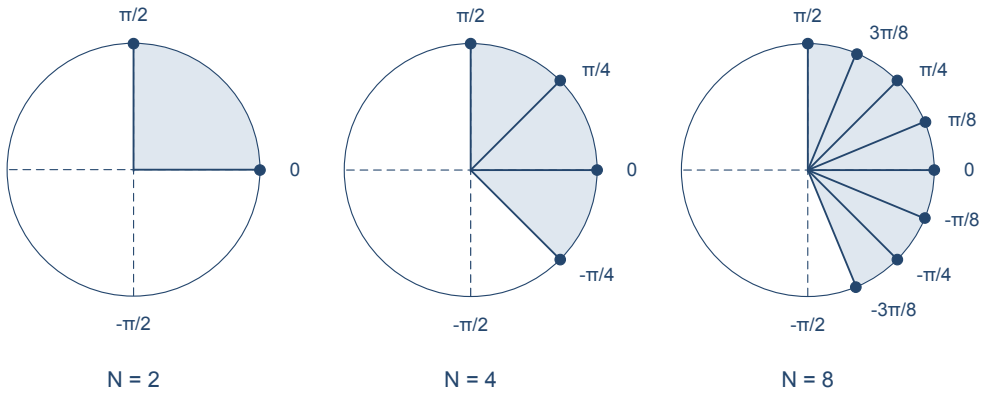


Figure 4.4: Constellation diagram with different number of phases [14]

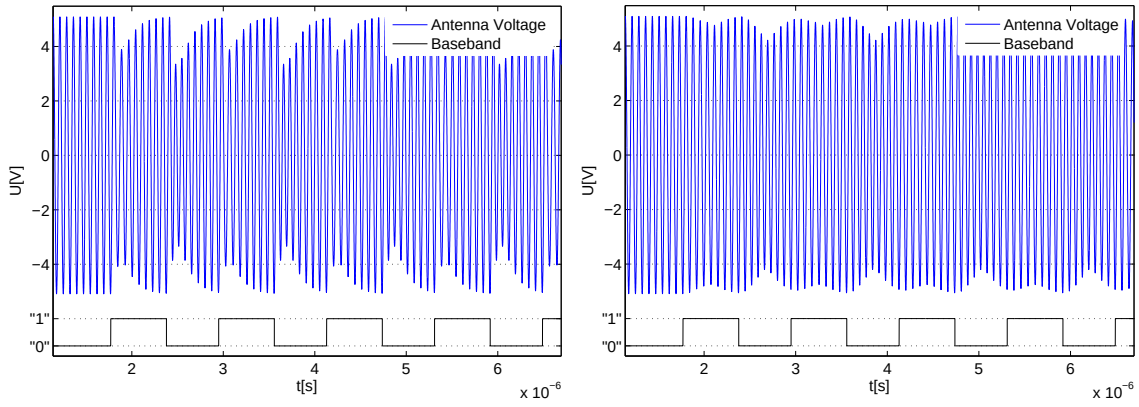


Figure 4.5: Comparison of a conventional and a proposed PSK
(a) PSK modulation with a phase shift $\varphi = 90°$ within one carrier period
(b) PSK modulation with a phase shift $\varphi = 90°$ subdivided into four carrier periods

Phase N Unitary $\Delta\varphi$ Degree	$2 = 2^1$ $\Delta\varphi = \pi/2$ $90°$	$4 = 2^2$ $\Delta\varphi = \pi/4$ $45°$	$8 = 2^3$ $\Delta\varphi = \pi/8$ $22.5°$	$16 = 2^4$ $\Delta\varphi = \pi/16$ $11.25°$
$1etu \cong 8/f_c$ = 590 ns	1 695	3 390	5 085	6 780
$1etu \cong 4/f_c$ = 295 ns	3 390	6 780	10 170	—
$1etu \cong 2/f_c$ = 147 ns	6 780	13 560	—	—
$1etu \cong 1/f_c$ = 74 ns	13 560	—	—	—

Table 4.5: Proposal from Gemalto, CEA Leti and Raisonance for the downlink — Data rate in kBit/sec (rounded)

4.2 Uplink

4.2.1 State of the Art

As mentioned in the previous chapter 3.2, the data transmission from PICC to PCD is based on the load modulation. This method uses a subcarrier which represents a two-stage modulation (see figure 3.7 in the previous chapter). Both communication interfaces (ISO/IEC 14443-Type A/B) use a subcarrier with a frequency of 847.5 kHz ($f_c/16$ with $f_c = 13.56\,MHz$), which makes it possible to separate the corresponding wanted signal (data) better from the carrier signal. The standard of the Type A communication interface defines a *On-Off Keying* (OOK) subcarrier modulation with the Manchester encoded baseband data stream. Afterwards the load modulation of the carrier signal with the modulated subcarrier takes place. The standard for the Type B communication interface defines a BPSK modulation of the subcarrier with an NRZ encoded baseband data stream. Afterwards the load modulation of the carrier signal takes place again. Today the standard defines data rates of 106/212/424 and 848kbit/sec (rounded). The relevant information concerning encoding and modulation methods for the uplink is summarized in table 4.6 [42].

	Type A	Type B
Baseband Encoding	Manchester	NRZ-L
Subcarrier Modulation	On-Off Keying	BPSK
Carrier Modulation	Load Modulation (ASK)	Load Modulation (ASK)
Data Rate	106-848 kbit/sec	106-848 kbit/sec

Table 4.6: Coding and modulation methods for the uplink (ISO/IEC 14443)

4.2.2 Parameters to Increase the Data Rate for the Uplink

The coding and modulation methods defined in the product standard ISO/IEC 14443-Type B provide a basis for further considerations concerning VHDR. In *Amendment 1* of the ISO/IEC 14443-Part 3 the term *elementary time unit* (etu) defines the symbol time and is calculated by the following formula:

$$1etu = \frac{1}{r_s} = \frac{128}{D \cdot f_c} \tag{4.1}$$

The divisor $D \in 1, 2, 4, 8$ is used for the selection of the symbol rate. In case of the standardized BPSK modulation the symbol rate is equal to the bit rate $r_s = r_b$, with the symbol rate being the reciprocal value of the *elementary time unit*. The initial value of the divisor D is 1, giving the initial bit rate $r_b = f_c/128 = 105.94\,kbit/sec$. The standard defines a subcarrier frequency f_{SC} of $f_c/16 = 847.5\,kHz$ which is derived from the carrier frequency f_c. With the configuration D = 8 a maximum bit rate of $847.5\,kbit/sec$ is possible. The definition in 4.1 is valid for a subcarrier frequency of $847.5\,kHz$. To change the subcarrier frequency the equation 4.1 must be extended

by the subcarrier divisor $D_{SC} \in 2, 4, 8, 16$.

$$f_{SC} = \frac{f_c}{D_{SC}} \Rightarrow D_{SC} = \frac{f_c}{f_{SC}} \tag{4.2}$$

According to the product standard the subcarrier divisor D_{SC} equals 16. An extension by factor 8 leads to:

$$8 \cdot \frac{f_c}{f_{SC}} = 8 \cdot D_{SC} = 128 \tag{4.3}$$

The symbol time (etu) in conjunction with the new introduced subcarrier divisor can be expressed as follows:

$$1etu = \frac{1}{r_s} = 8 \cdot \frac{D_{SC}}{D \cdot f_c} \tag{4.4}$$

and

$$r_s = \frac{D \cdot f_c}{8 \cdot D_{SC}} \tag{4.5}$$

with

$$D_{SC} = \frac{f_c}{f_{SC}} \tag{4.6}$$

If a higher order modulation is applied, the equation 4.4 is expanded by the value $ld(M)$ (logarithm to the basis 2) and the bit rate can be expressed as follows:

$$r_b = ld(M) \cdot r_s = ld(M) \cdot \frac{D \cdot f_c}{8 \cdot D_{SC}} \tag{4.7}$$

M defines the number of symbols which is a power of two. According to the equation 4.7 there exist three parameters (D, DSC and M) for the increase of the data transfer rate. Those options will be discussed in the following sections.

Reduction of the Number of Subcarrier Periods per Symbol

This method is already defined in the *Amendment 1* of the product standard ISO/IEC 14443 - Part 2 and Part 3 [47], [48]. The initial data rate equals 106kbit/sec and the associated symbol time (etu) consists of eight subcarrier periods. An increase of the divisor $D \in 1, 2, 4, 8$ in equation 4.1 enables a simple opportunity to increase the data rate. With the configuration D = 8 and $f_{SC} = 847.5kHz$ a maximum bit rate of 847.5kbit/sec is possible. Figure 4.6 illustrates the bit time reduction as a result of the decimation of subcarrier periods per symbol.

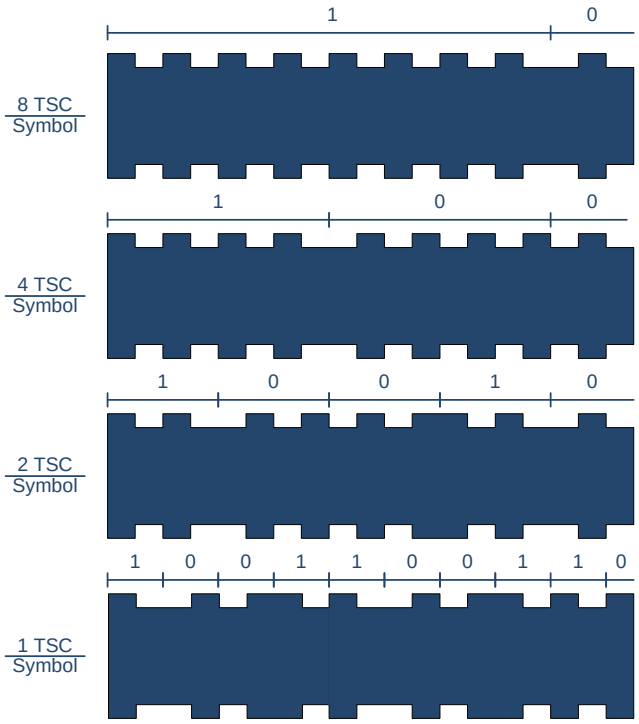


Figure 4.6: Reduction of the number of subcarrier periods per symbol [79]

Increase the Subcarrier Frequency

Because of the restriction of the subcarrier frequency (847.5 kHz) in ISO/IEC 14443 the maximum data rate is limited to 847.5kbit/sec. The subcarrier frequency is derived from the carrier frequency f_c and the corresponding divisor is 16. An improvement of the data rate performance can be achieved by the use of a higher subcarrier frequency. Figure 4.7 illustrates signal waveforms with a different subcarrier frequency f_{SC} = [$f_c/16$, $f_c/8$, $f_c/4$, $f_c/2$] = [847.5 kHz, 1.695 MHz, 3.39 MHz, 6.78 MHz] and a respective symbol time of two subcarrier periods per symbol. If a subcarrier frequency of 6.78 MHz is chosen and the symbol time consists of one subcarrier period, the maximum achievable data rate equals 6.78 Mbit/sec.

Higher Order Modulation Methods

The third method to increase the data rate performance is the use of a high level modulation, with several bits being combined to different symbols. *M-ary Phase Shift Keying* (MPSK) as well as *M-ary Amplitude Shift Keying* (MASK) are applicable modulation techniques. The character M denotes the number of modulation levels, i.e. the MPSK modulation uses M different phase states and the MASK modulation uses M different amplitude levels. The MPSK modulation is carried out on the subcarrier signal. Figure 4.8 shows a conventional BPSK modulation method which is standardized in ISO/IEC 14443-Type B. In addition, a *Quadrature Phase Shift Keying* (QPSK) modulation method with four phase states and an 8-PSK modulation method with eight

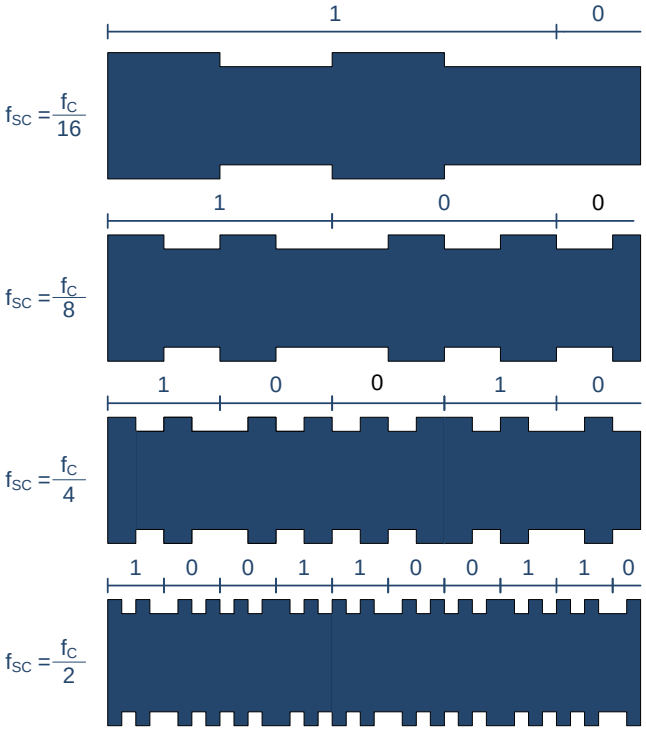


Figure 4.7: Increase of the subcarrier frequency [79]

phase states are represented. Only the modulated subcarrier waveforms are illustrated and the 13.56 MHz based carrier is not represented. With a QPSK modulation method two bits are merged into one symbol and in the 8-PSK modulation method three bits are merged into one symbol.
In the constellation diagram the four phase states (QPSK) are shifted 90 degrees to each other. As already mentioned, the phase shift keying is carried out on the subcarrier and then the carrier is load-modulated by the PSK modulated subcarrier waveform. The QPSK method needs one carrier period for a 90° phase shift, i.e. one symbol consists of four carrier periods, which limits the subcarrier frequency to 3.39 MHz $(f_c/4)$.

$$90° \hat{=} \frac{T_{SC}}{4} = T_c \Rightarrow f_{SC} = \frac{f_c}{4} = 3.39\,MHz \tag{4.8}$$

The corresponding data rate is:

$$r_b = ld(M) \cdot \frac{D \cdot f_c}{8 \cdot D_{SC}} = ld(4) \cdot \frac{8 \cdot f_c}{8 \cdot 4} = 6.78\,Mbit/sec \tag{4.9}$$

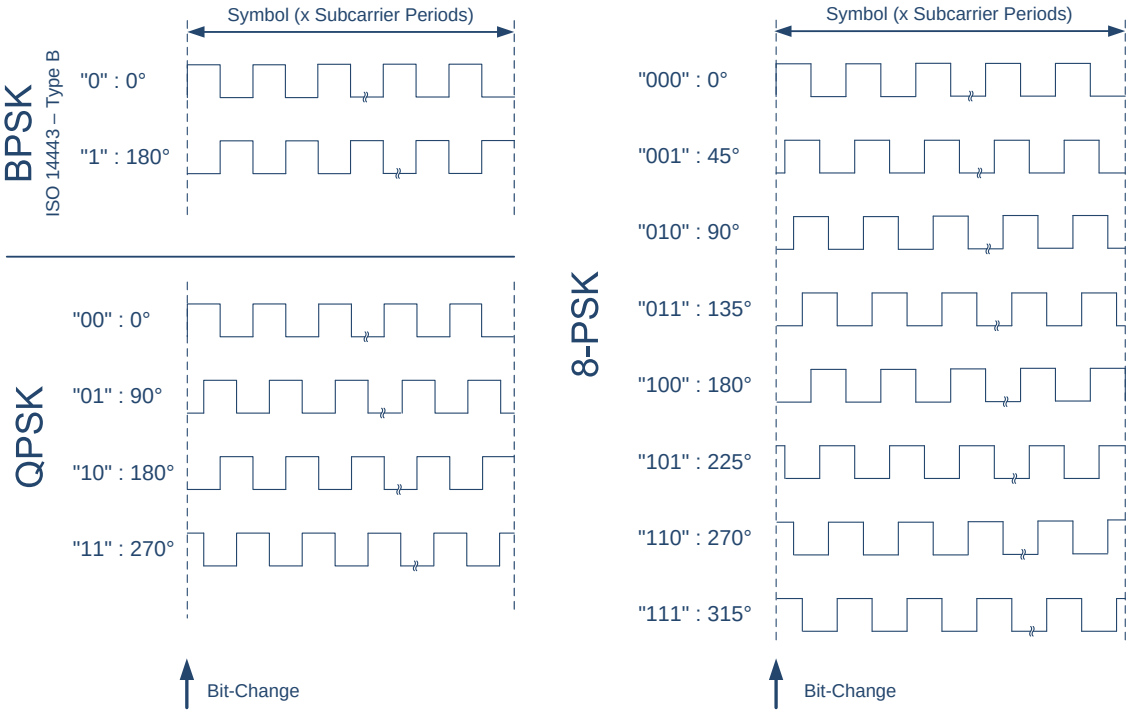


Figure 4.8: MPSK modulation on subcarrier

In the 8-PSK modulation, three bits are merged into one symbol. Consequently, one carrier period equals 45° and the subcarrier frequency is restricted to 1.7 MHz.

$$45° \hat{=} \frac{T_{SC}}{8} = T_c \Rightarrow f_{SC} = \frac{f_c}{8} = 1.695\,MHz \tag{4.10}$$

The corresponding data rate is:

$$r_b = ld(M) \cdot \frac{D \cdot f_c}{8 \cdot D_{SC}} = ld(8) \cdot \frac{8 \cdot f_c}{8 \cdot 8} = 5.085\,Mbit/sec \tag{4.11}$$

Table 4.7 lists the expected bit rates depending on the subcarrier frequency, symbol time and phase modulation scheme (BPSK, QPSK and 8-PSK). The gray highlighted entries in the table are not all realistic values, because one phase shift cannot be represented by one carrier period with the appropriate subcarrier frequency. Given an increase of the subcarrier frequency – the number of subcarrier periods for each symbol is constant – a reduction of symbol time is implicated, which causes an increase of the bit rate. The thus achievable data rate is also shown in table 4.7. Additional figure 4.9 shows a QPSK modulation on the subcarrier (upper graph), based on the carrier waveform. Obviously, an increase of the number of phase states ($M > 2$) reduces the required bandwidth. However, a better signal-to-noise ratio is required, because the symbols are closer to each other. Moreover, generating the MPSK ($M > 2$) is more difficult than the BPSK. Consequently, the BPSK modulation will be used for further considerations since a higher order PSK modulation will not lead to a better data rate performance. The MASK modulation

with multiple amplitude levels for the carrier load modulation presents a second method by which several bits are merged into symbols. (figure 4.9, lower graph). The position of the transponder in the operating range (of the reader) influences the amplitude of the load modulation significantly. Therefore, it is not guaranteed that during an uplink communication the amplitude level will remain constant. This is the reason why the MASK method is not considered anymore. The content of the discussed topic within this section is also partly published in [79].

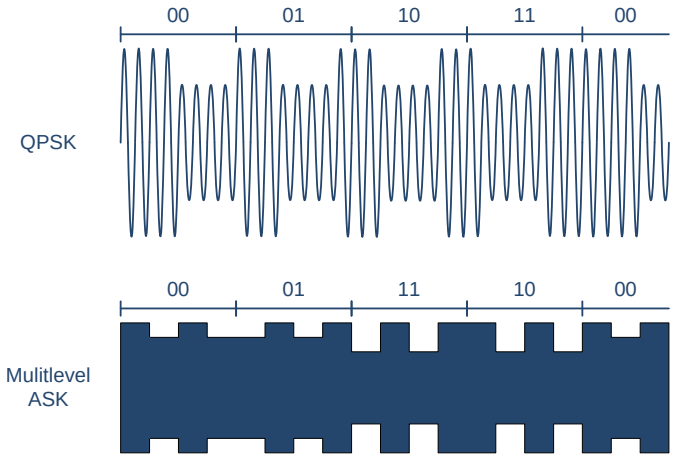


Figure 4.9: Multilevel modulation (QPSK and MASK) [79]

4.2.3 ISO Proposals of Very High Data Rates

Japan Proposal

For the uplink, the same method — bit time reduction — is suggested as for the downlink. The reachable bit times and associated possible data rates are shown in table 4.2.

Philips and AFNOR Proposal

Those two papers pursue the same approach to achieve very high data rates. Therefore, a phase shift keying of the subcarrier with more phase states is used, which was already treated in the previous section 4.2.2. The achievable data rates are also displayed in table 4.7.

f_{SC}		T_{SC}	No. of subcarrier periods per symbol	Symbol Time	BPSK	QPSK	8-PSK
-	kHz	sec	-	sec	kBit/sec	kBit/sec	kBit/sec
f_c/16	848	1.18E-06	8	9.44E-06	106	212	318
			4	4.72E-06	212	424	636
			2	2.36E-06	424	848	1 271
			1	1.18E-06	848	1 695	2 543
f_c/8	1 695	5.90E-07	8	4.72E-06	212	424	636
			4	2.36E-06	424	848	1 271
			2	1.18E-06	848	1 695	2 543
			1	5.90E-07	1 695	3 390	5 085
f_c/4	3 390	2.95E-07	8	2.36E-06	424	848	1 271
			4	1.18E-06	848	1 695	2 543
			2	5.90E-07	1 695	3 390	5 085
			1	2.95E-07	3 390	6 780	10 170
f_c/2	6 780	1.47E-07	8	1.18E-06	848	1 695	2 543
			4	5.90E-07	1 695	3 390	5 085
			2	2.95E-07	3 390	6 780	10 170
			1	1.47E-07	6 780	13 560	20 340
f_c/1	13 560	7.37E-08	8	5.90E-07	1 695	3 390	5 085
			4	2.95E-07	3 390	6 780	10 170
			2	1.47E-07	6 780	13 560	20 340
			1	7.37E-08	13 560	27 120	40 680

Table 4.7: MPSK modulation on subcarrier (data rate rounded)

Proposal from Gemalto, CEA Leti and Raisonance

This proposal recommends a communication concept for the uplink, in which no dedicated subcarrier is used. The baseband coding is carried out by symbol mapping which uses an especially defined set of pattern (depending on the data rate). After symbol mapping the load modulation of the carrier signal with the patterns/symbols takes place. The symbol time (etu) is restricted to eight carrier periods.

To obtain optimal patterns regarding energy consumption and bandwidth, the following methods are considered:

- Prevent long load modulation sequences (for minimization of the energy consumption)
- Maximize the pulse duration within a pattern (for reduction of the necessary bandwidth)
- Maximize the Hamming distance (for an advanced error detection)

Table 4.8 lists the achievable data rates and their associated number of patterns [14].

Phase N	$2^1 = 2$	$2^2 = 4$	$2^3 = 8$	$2^4 = 16$	$2^5 = 32$	$2^6 = 64$
$1etu \cong 8/f_c$ = 590 ns	1695	3390	5085	6780	8475	10170

Table 4.8: Proposal from Gemalto, CEA Leti and Raisonance for the uplink — Data rate in kBit/sec (rounded)

4.2.4 Implemented Communication Concept for the Uplink

Different approaches and concepts have been elaborated to achieve a maximum data rate for the uplink. One essential task of the present thesis was the elaboration and implementation of a VHBR transmission concept which supports data rates up to 13.56 Mbit/sec. The previously discussed proposals for data rates above 6.78Mbit/sec require quite complex encoding/modulation units on the transponder side and also complex decoding/demodulation units on the reader side. This especially applies to higher order modulation methods like M-ASK, M-PSK or QAM. For this reason, the aim was to develop a preferably simple coding and modulation technique to relax the requirements on the transponder as well as the reader architecture. Because of the influence of the quality factor Q, conventional contactless proximity systems are not able to support data rates above 1.7 Mbits/sec (see section 3.1.2). With the new, improved reception circuit and antenna arrangement (see chapter 3.3.2) the signal quality of the received antenna signal will not be influenced by the quality factor Q anymore. The diploma thesis of Matthias Pichler [79] describes the implementation of a digital demodulation unit which supports data rates up to 6.78 Mbit/sec. A description of the two implemented communication concepts (6.78 Mbit/sec and 13.56 Mbit/sec) is given in the subsequent sections.

4.2.4.1 Load Modulation with Subcarrier (up to 6.8 Mbit/sec)

This VHBR concept and it's implementation is based on the ISO/IEC standard 14443 Type B (already discussed in section 4.2.1) and the Philips proposal. Figure 4.10 on the left shows the two-stage modulation concepts standardized in ISO/IEC 14443 Type B. The transponder recovers the subcarrier from the electromagnetic field which is provided by the contactless reader. In the first step the subcarrier is BPSK modulated by the NRZ coded baseband data. Next, the load modulation of the magnetic field takes place, where the carrier is ASK modulated by the modulated subcarrier. Because of the defined subcarrier frequency of 848 kHz the maximum data rate is bounded to 848 kbit/sec.

To obtain a higher data rate (in this case up to 6.8 Mbit/sec) two parameters are modified:

- Decrease the number of subcarrier periods per symbol
- Increase the subcarrier frequency

The associated mathematical derivation of the following formula was already presented in section 4.2.2. The setting D = 8 reduces the number of subcarrier periods down to one period per symbol. Additionally, the adjustment of the subcarrier divisor $D_{SC} = 2$ increases the subcarrier frequency to $f_{SC} = f_c/D_{SC} = f_c/2 = 6.78\,MHz$. With M=2 (no higher order modulation method) and the other two settings the achievable data rate results in the following:

$$r_b = ld(M) \cdot \frac{D \cdot f_c}{8 \cdot D_{SC}} = ld(2) \cdot \frac{8 \cdot 13.56 \cdot 10^6}{8 \cdot 2} = 6.78\,Mbit/sec \tag{4.12}$$

This implemented method increases the communication speed up to 6.78 Mbit/sec, which is eight times higher than the maximum standardized data rates [79].

4.2.4.2 Load Modulation without Subcarrier (up to 13.56 Mbit/sec)

The elaborated and implemented communication concept is a simple and effective method to achieve very high data rates for the uplink. Thereby, the two-stage load modulation process is reduced to a single load modulation (ASK) of the carrier, i.e. no subcarrier is used for the uplink communication [50]. Conventional contactless proximity systems use a subcarrier for a better and easier separation (filtering) of the wanted baseband signal from the carrier signal. Because of the new, improved reception circuit and antenna arrangement, a subcarrier is no longer required. The carrier is modulated directly with the NRZ coded baseband data which is depicted in figure 4.10. If the NRZ coded data stream has a data rate of 13.56 Mbit/s also the uplink has this value. In this case, one single bit equals one carrier period of $1/f_c = 73.75nsec$.

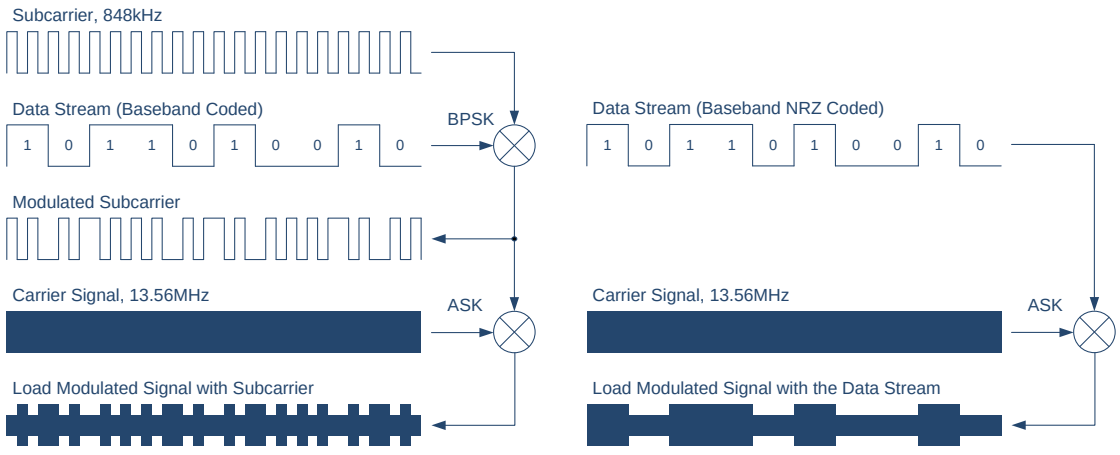


Figure 4.10: Load modulation with and without subcarrier

A contactless proximity technology already exists which does not need a dedicated subcarrier for the uplink. But there is a difference between that and the concept dealt with in this thesis.

FeliCa™ is a proprietary contactless card technology developed by Sony with a communication speed of 212 kbit/sec or 424 kbit/sec. In comparison to the communication method defined in ISO/IEC 14443 Type A/B no explicit subcarrier is used for the uplink. The carrier signal is modulated directly by a Manchester coded baseband. However, Manchester coding of the baseband signal implicates another type of subcarrier. Manchester coding guarantees a change of the signal level at every bit, but requires twice the bandwidth of an NRZ coding method.

The implemented coding and modulation method offers several advantages:

- No high phase resolution (i.e. high clock rate) will be necessary on the PICC
- Simple architecture of the digital part on PICC (no generation of MPSK signals)
- Simple architecture of the analog front end on PICC (adaptation to a higher load modulation frequency)
- Receive path of the PCD needs no complex demodulation and decoding unit to process the received modulated signal (reduced complexity compared to the MPSK demodulator)

The introduced communication concept is a simple and very effective method to achieve data rates up to 13.56 Mbit/sec so that a communication speed is provided that is 16 times faster than standardized in ISO/IEC 14443. Sections 7.4.1 and 7.4.3 present the measurement results of the implemented communication concept for the uplink.

4.3 Communication Sequence

In contactless proximity systems (standardized in ISO/IEC 14443 [42]) the reader always initiates the communication sequence with a command to the transponder. According to the product standard, there are different communication sequences for various operation states like for initialization, anti-collision process or plain data exchange. Figure 4.11 shows the sequential communication sequence with the alternating *Send/Receive* states of the reader and the transponder. The reader must poll periodically, in order to detect transponders which are entering the operating range. After each request command the reader waits for a predefined time. When a transponder enters the operating field, it must answer within this predefined time. Otherwise the reader sends a request command again, because it assumes that either no transponder is within the operating range or the communication was disturbed.

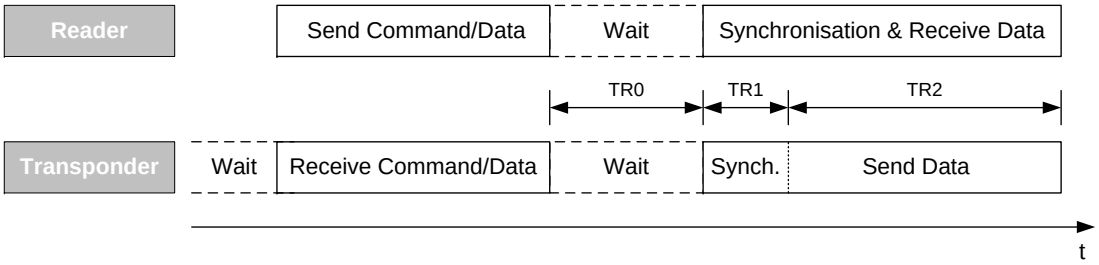


Figure 4.11: Communication sequence between reader and transponder

Depending on the respective product standard, there exist different timings and timeouts which must be strictly adhered to by both the reader and the transponder. For the contactless prototyping reader system three timeouts are defined. The minimal time period between the end of the *Send Command/Data* sequence (Reader) and the start of the *Synchronisation* sequence (Transponder) is defined by TR0. Within this time period, both the transponder and the reader can process the respective command/data. Then the transponder sends a synchronisation pattern to the reader during a time period TR1. If a subcarrier is used for the uplink, the synchronisation pattern equates to an unmodulated subcarrier. This pattern is very important for the correct reception of the data by the reader. If the end of a frame cannot be recognized by the reader, it leaves the *Receive* state after the timeout TR2, i.e. the maximal duration of one frame is restricted to TR2. Figure 4.12 shows a communication sequence which was measured in the prototyping reader system after the analog front end. Due to the improved antenna concept, the answer of the transponder can be seen much better than the load modulation measured by a sense coil, which is located between reader and transponder antenna. Each communication sequence can be clearly identified in figure 4.12 [79].

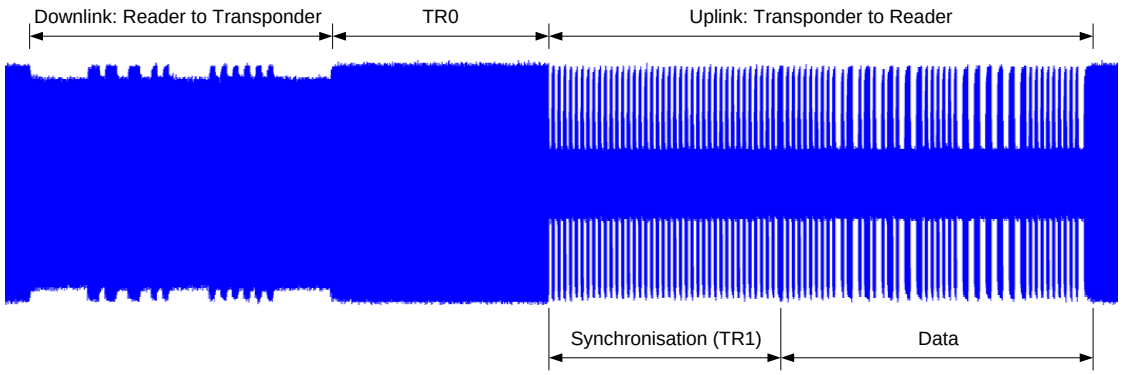


Figure 4.12: Measured communication sequence between reader and transponder

4.3.1 Start Sequence, Run-in Pattern, Character and Frame Size

Start Sequence

The theory within this section was not implemented in the PhD thesis, but it was published in the invention disclosure [50]. In this context, the term *Start Sequence* means the activation of the VHBR functionality. Therefore it must be kept in mind that the downward compatibility of a contactless proximity system which supports VHBR must be given. That means that the system should support the current standardized data rates, which are defined in the product standard ISO/IEC 14443 [42]. Part three of the mentioned product standard defines a so-called *Initialization and Anticollision* sequence, which describes the polling activity for PICC when entering the field of a contactless proximity reader. For the detection of PICCs in the operating range, the PCD sends repeated request commands. For Type A communication the reader sends *Request Command Type A* (*REQA*) and for Type B *Request Command Type B* (*REQB*). After the anticollision and selection of the specific PICC, the selected PICC is switched to layer 4. The whole communication/transaction within layer 3 always operates with a data rate of 106 kbit/sec. This will guarantee the downward compatibility with conventional PICCs. It is the idea first to activate the VHBR functionality in layer 4 of the ISO/IEC 14443 (Part 4) and then to make the PCD and PCC agree to a new, higher data rate for further data exchange. But an exact mechanism must be defined by the working groups of the ISO which deal with this topic. A detailed and exact explanation of the *Initialization and Anticollision* sequence is given in the product standard [42].

Run-in Pattern

The new elaborated and implemented communication concept, which enables data rates up to 13.56 MBit/sec, is based on load modulation without the use of a subcarrier signal (see 4.2.4.2). In conventional contactless systems, this subcarrier signal is typically used as run-in pattern and, consequently, for synchronization on the PCD. As this signal will not be used anymore in the new communication concept, a run-in pattern must be generated by the PICC. An appropriate synchronization sequence is e.g. an alternating *10* bit pattern with the highest possible bit rate (frequency).

4.3.2 Character and Frame Size

A new transmission protocol especially for big data volumes should also be developed. Part 4 (Transmission Protocol) of the product standard ISO/IEC 14443 [42] defines data packets with a size of maximal 256 bytes, which are too small for multimedia applications. A high data throughput for the uplink demands high bit rates and a compact and efficient data framing. Therefore, e.g. more than one byte can be combined to a character. The number of bytes per character as well as the bit/byte order have to be defined. Figure 4.13 shows a possible character format with a start and stop indication. This start and stop indication can be a simple bit sequence (one or more bits) or e.g. a parity bit, calculated over the entire character. Figure 4.14 shows a possible frame format, which is used for the transmission form PICC to PCD. The frame consists of a certain number of characters. As mentioned before, the current standardized frame size is certainly too small, consequently, frame sizes above 256 bytes are recommended. Every communication frame can be delimited by a start and stop sequence.

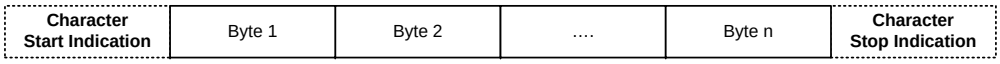


Figure 4.13: Character Format

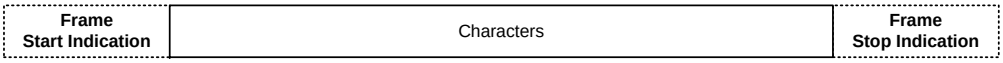


Figure 4.14: Frame Format

Another important issue is the occurence of long phases without any change in the load modulation. Figure 4.15 shows a double word (32 bit) representation for constant data (0x00 and 0xFF) and, consequently, without any phase change. Due to the dynamic behavior of the PICC (variation of the magnetic field strength according to the position) within the operating range of the PCD, extremely long sequences without any load modulation increase the complexity of the demodulation process on the PCD.

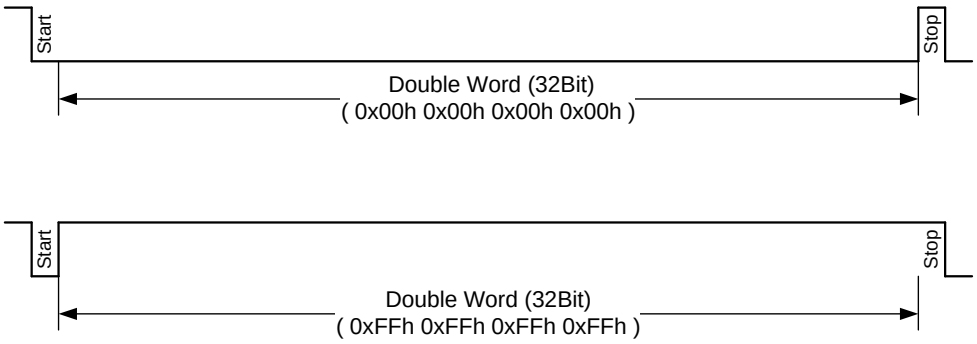


Figure 4.15: Double Word format with start/stop indication but without coding

Methods to avoid long sequences without a change in the load modulation are, for example, line codes, scrambling or bit stuffing. One applicable line code is the 4B5B encoding scheme, which is used in 100BASE-TX and 100BASE-FX Ethernet [26]. This code maps groups of four bits (*Nibble*) onto groups of five bits. The five bit words are predefined in an encoding table and are chosen to ensure that there will be at least one transition per word. The 4B5B code has a certain redundancy, although several 4B5B characters can be used for control or synchronization information, e.g. start/stop flag. Figure 4.16 shows an example of a 4B5B coded double word. In comparison to figure 4.15 the coding rule avoids long phases without a change in the load modulation. A disadvantage of this coding scheme is that five bits are used for the representation of only four bits and this leads to a data rate loss of 20%. For the transmission of a big amount of data, it would also make sense to add a corresponding *Error Correction Code* (ECC) to the usual *Error Detection Code* (EDC) like CRC or Parity Bit (defined in ISO/IEC 14443) would also make sense.

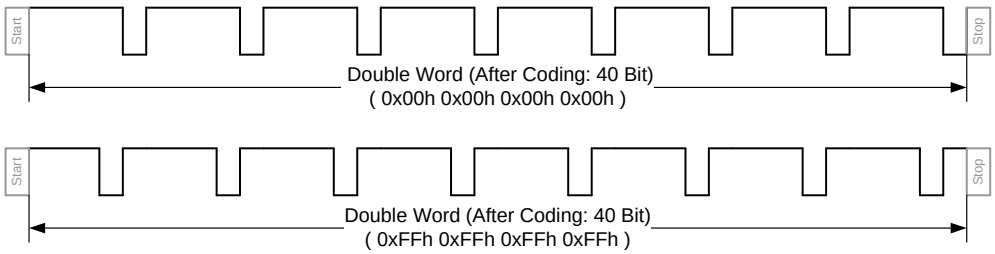


Figure 4.16: Double Word format with 4B5B coding

Another appropriate method to force alteration of the current load modulation state is bit stuffing. In regard to contactless proximity systems, the principle of bit stuffing was extended to symbol stuffing which was elaborated and published in the invention disclosure [50].
Figure 4.17 shows a generic example of symbol stuffing. The data sequence 4.17a before transmission contains two symbols *A* and *B* (e.g. 0 and 1). After *n* consecutive symbols *A* the coding rule inserts *k* symbols *X*. In addition, the coding rule inserts *r* symbols *Y* if more than *m* symbols *B* appear in the plain data sequence. The stuffed symbol sequence 4.17b is transmitted over the air interface and the PCD extracts the plain data and delivers the de-stuffed symbol sequence 4.17c. Symbol stuffing can also be applied to indicate the boundary of data frames, e.g. *Start of Frame* (SOF) and *End of Frame* (EOF). As mentioned before, the discussed theory within this section was not implemented in the PhD thesis, but it was published in the invention disclosure [50].

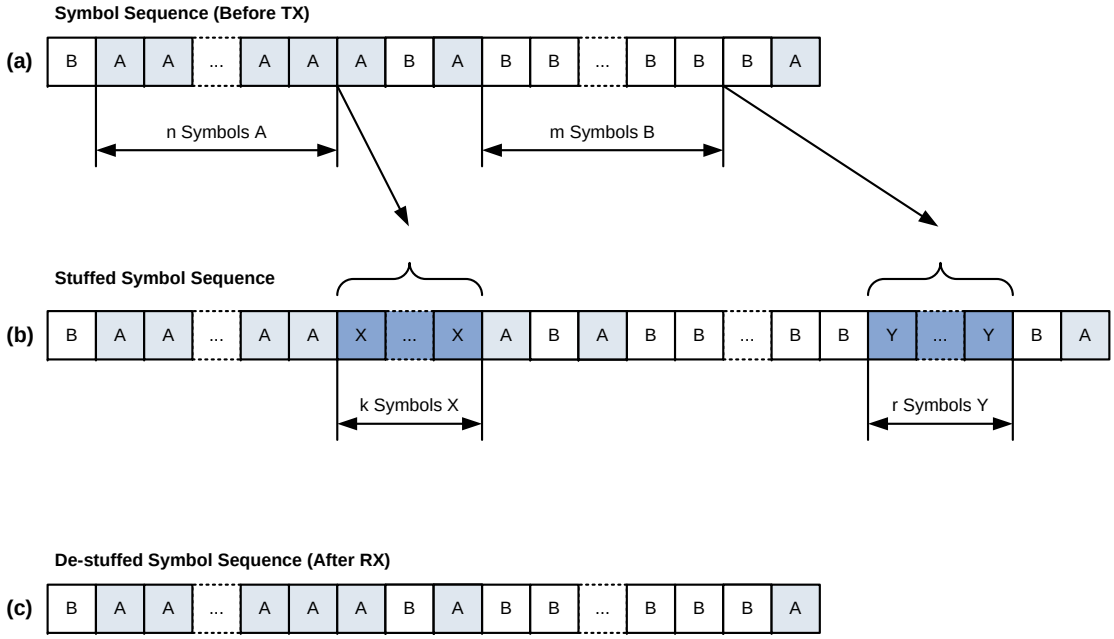


Figure 4.17: Symbol-Stuffing Rule

5 Transceiver Concepts and Architectures

This chapter gives a detailed overview and description of applicable transceiver architectures in contactless proximity reader systems. For further observations, a distinction of transmitter and receiver architectures is drawn. The essential aim of this thesis was the design and development of a contactless prototyping reader which supports very high data rates. In addition, the possibility of supporting various protocol standards was also a very important design and development criterion. For exploration of very high bit rates (modulation and encoding methods) and various transmission protocols, a flexible transmission unit with an associated digital modulation method was implemented. The core topic of the current thesis was the design of a digital receiving unit. The implemented digital demodulation method is based on under-sampling and a special elaborated algorithm to provide a simple and energy-efficient receiving method. A detailed explanation of the implemented modulation and demodulation concept will be given in this chapter. In addition, an overview and comparison of the current research status concerning VHBR transceivers for contactless proximity applications will be presented.

5.1 Transmit Architectures

The complexity of a transmitter architecture for contactless readers depends on the respective application area and the number of standards which must be supported by the reader. In conventional contactless systems (e.g. proximity or vicinity coupling systems), the downlink-communication is mostly based on ASK modulation of the carrier. This method is realized by a simple amplitude modulator which is shown in the next section. However, there are also RFID standards where no ASK modulation is applied for the downlink. For example, there exists an RFID product solution which uses a so-called *Phase Jitter Modulation* (PJM) for the reader-transponder communication. This technique can be regarded as a PSK modulation of the carrier with very small phase shifts between $\pm 1^\circ$ and $\pm 2^\circ$. PJM products made by Magellan Technology enable a very fast identification of a high number of transponders. The technique is standardized in ISO/IEC 18000-3 Mode 2 [45]. The phase jitter modulation with the fixed small phase shifts can be realized, for example, through a simple phase shifter such as an RC circuit [90]. However, the exploration of VHBR based on a higher order PSK modulation requires an advanced modulator. This will be dealt with in the following chapter.

5.1.1 Amplitude Modulator

Figure 5.1 shows a symbolic representation of a simple transmit circuit for ASK modulation which is based on switched CMOS transistors. The digital carrier clock (13.56 MHz) is applied to the respective gates of both transistors. The CMOS transistors symbolize an adjustable resistor which is realized by a parallel circuit of several transistors. Thus, the modulation depth (modulation index) can be adjusted by an impedance variation of the parallel switched transistors. The circuit

outputs a square wave signal which is converted to a sinusoidal waveform by a subsequently connected *Electromagnetic Compatibility*(EMC) filter [87], [95], [17].

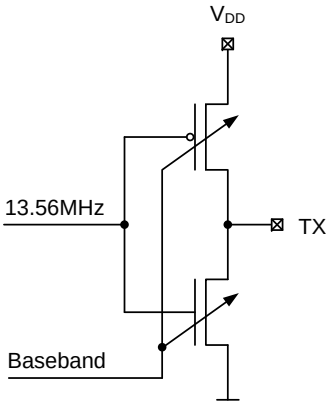


Figure 5.1: Simple transmit circuit for ASK modulation [95]

5.1.2 Polar Form of Modulation

There are various methods to represent digital modulated signals, such as a constellation diagram or an eye diagram (for detailed explanation see chapter 7.3.1). With the digital modulation process the bits of the baseband data are merged into data symbols. Those symbols are mapped into the constellation diagram at each symbol clock transition and described by a vector representation (see figure 5.2).

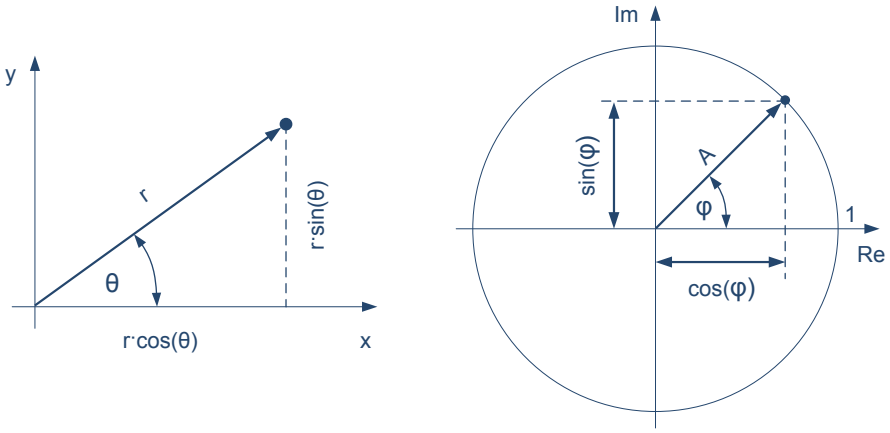


Figure 5.2: Vector representation and complex plane

There are two possible ways to describe a vector:

- Polar coordinates (Polar form)
- Cartesian coordinates (Cartesian form)

By means of the polar representation, the vector (i.e. point) is described by the magnitude r and the phase angle Θ relating to the point of origin $(0, 0)$. The following equation shows the conversion from polar coordinates (r, Θ) to Cartesian coordinates (x, y) using the trigonometric functions sine and cosine.

$$x = r \cdot \cos(\Theta) \tag{5.1}$$

$$y = r \cdot \sin(\Theta) \tag{5.2}$$

Conversion from Cartesian coordinates to polar coordinates is represented by the following equation:

$$r = \sqrt{x^2 + y^2} \tag{5.3}$$

$$\Theta = \begin{cases} 0 & \text{if } x = 0 \text{ and } y = 0, \\ \frac{3 \cdot \pi}{2} & \text{if } x = 0 \text{ and } y < 0, \\ \frac{\pi}{2} & \text{if } x = 0 \text{ and } y > 0, \\ \arctan\left(\frac{y}{x}\right) + \pi & \text{if } x < 0, \\ \arctan\left(\frac{y}{x}\right) + 2 \cdot \pi & \text{if } x > 0 \text{ and } y < 0, \\ \arctan\left(\frac{y}{x}\right) & \text{if } x > 0 \text{ and } y \geq 0 \end{cases} \tag{5.4}$$

The formulae for the conversion of the two representations are only valid if the Cartesian origin point is (0,0). The polar form of modulation (see figure 5.3) is one of the most straightforward methods but requires additional hardware components such as square root and multiplication units.

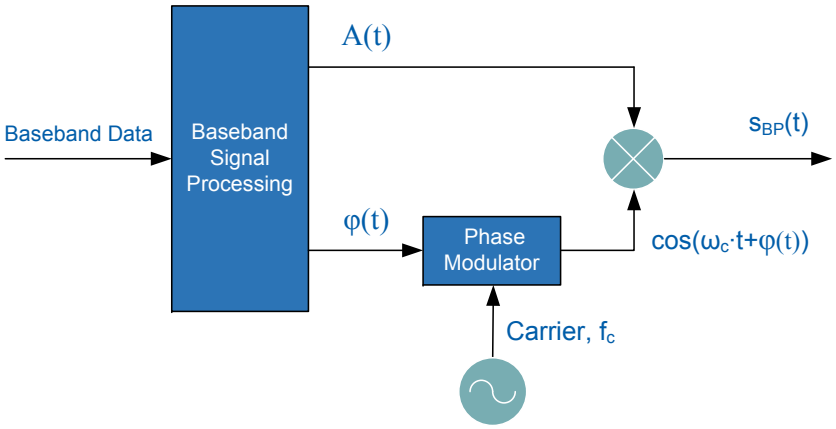


Figure 5.3: Polar form of modulation [61]

The *Baseband Signal Processing* unit comprises these modules which are necessary to calculate the magnitude and the phase angle [61], [88]. The polar form of modulation can be mathematically expressed as the bandpass signal:

$$s_{BP}(t) = A(t) \cdot \cos\left(\omega_C \cdot t + \varphi(t)\right) \tag{5.5}$$

5.1.3 Quadrature Form of Modulation

The constellation diagram equates to a complex plane whereas the symbol points are described by complex numbers (see figure 5.2). The representation of complex numbers can be carried out by Cartesian coordinates (rectangular form):

$$z = x + i \cdot y \tag{5.6}$$

An alternative notation for complex numbers is the representation in polar coordinates:

$$z = A \cdot (\cos\varphi + i \cdot \sin\varphi) = A \cdot e^{i \cdot \varphi} \tag{5.7}$$

Figure 5.4 shows the quadrature form of modulation which ensures a high level of flexibility regarding implementation of different modulation methods.

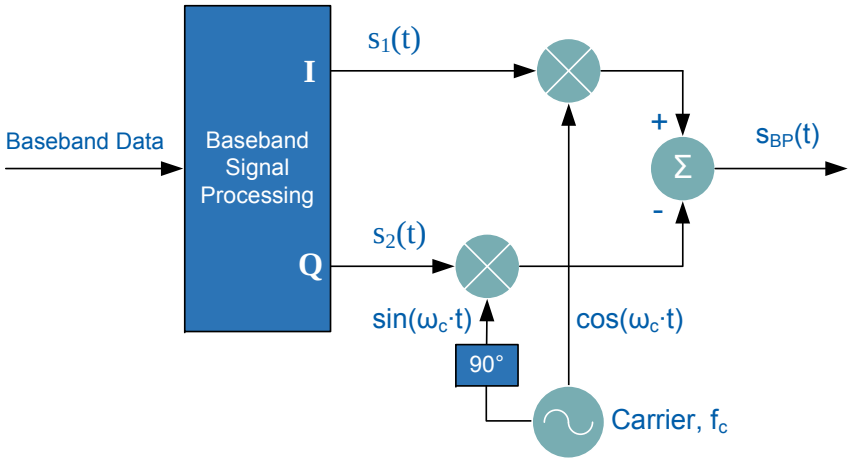


Figure 5.4: Quadrature form of modulation [61]

First of all, the baseband data is mapped to In-Phase(I) and Quadrature-Phase(Q) components and represented by symbols in the constellation diagram. The signals $s_1(t)$ and $s_2(t)$ on the In-Phase- and Quadrature-Phase-Channel are mixed with two signals (cosine and sinusoidal) which are separated by 90 degrees. They are orthogonal (independently) to each other and, consequently, the two signals $s_1(t)$ and $s_2(t)$ can be transmitted at the same time. The superposition of

the two single mixed In-Phase and Quadrature-Phase channels results in a real bandpass signal (Cartesian representation):

$$s_{BP}(t) = s_1(t) \cdot \cos(\omega_C \cdot t) - s_2(t) \cdot \sin(\omega_C \cdot t) \tag{5.8}$$

The reason for the negative term $s_2(t) \cdot \sin(\omega_C \cdot t)$ (also shown in the figure 5.4) will be discussed in the subsequent section. Because of the simple hardware implementation, the quadrature form of modulation is a commonly used technique[61], [83].

Complex Envelope

Basically, the quadrature modulation is a combination of two separated amplitude modulations. Due to the separated amplitude adjustment of the In-Phase- and Quadrature-Phase-Channel, a phase modulation is also possible. At the amplitude modulation, the baseband signal is mixed with a carrier signal and shifted to the higher frequency range. The complex envelope gives a relation between the signal in the baseband and the bandpass signal, which is located at the carrier frequency (see figure 5.5).

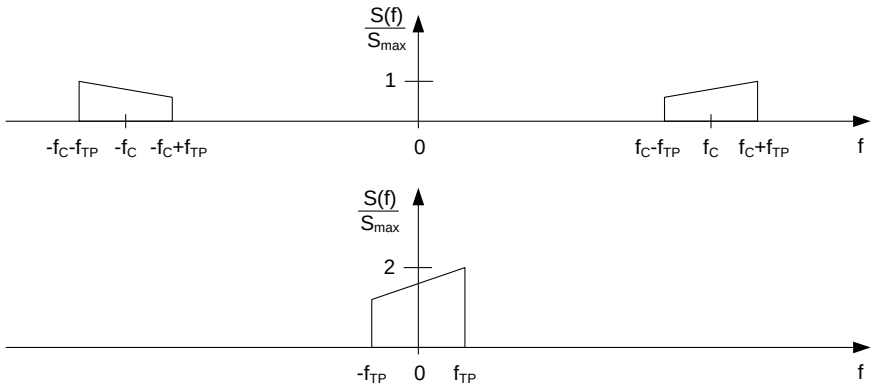


Figure 5.5: Frequency spectrum of a bandpass signal and the equivalent lowpass signal [77]

The mathematical representation of the quadrature form of modulation was shown in equation 5.8. A replacement of the abbreviations $s_1(t)$ and $s_2(t)$ by $I(t)$ and $Q(t)$ leads to the bandpass signal:

$$s_{BP}(t) = I(t) \cdot \cos(\omega_C \cdot t) - Q(t) \cdot \sin(\omega_C \cdot t) \tag{5.9}$$

In comparison to the polar representation (equation 5.5), the Cartesian expression comprises no explicit phase angle $\varphi(t)$. The phase factor is considered by the complex envelope:

$$g(t) = I(t) + i \cdot Q(t) = s_{TP}(t) \tag{5.10}$$

The complex envelope $g(t)$ of the bandpass signal is a complex low pass signal s_{TP}. A complex signal is also known as an *Analytic Signal*, which has no negative frequency parts in the frequency spectrum.

The complex bandpass signal can be expressed as follows:

$$\begin{aligned} s_{BP}^{+}(t) &= s_{TP}(t) \cdot e^{i \cdot \omega_C \cdot t} \\ &= [I(t) + i \cdot Q(t)] \cdot [\cos(\omega_C \cdot t) + i \cdot \sin(\omega_C \cdot t)] \\ &= \underbrace{[I(t) \cdot \cos(\omega_C \cdot t) - Q(t) \cdot \sin(\omega_C \cdot t)]}_{\Re\{s_{BP}^{+}(t)\} = s_{BP}(t)} + i \cdot \underbrace{[Q(t) \cdot \cos(\omega_C \cdot t) + I(t) \cdot \sin(\omega_C \cdot t)]}_{\Im\{s_{BP}^{+}(t)\}} \end{aligned} \tag{5.11}$$

The real bandpass signal $s_{BP}(t)$ can be represented by the real part $\Re\{\cdot\}$ of the complex value $g(t) \cdot e^{i \cdot \omega_C \cdot t}$:

$$s_{BP}(t) = \Re\left\{s_{BP}^{+}(t)\right\} = \Re\left\{s_{TP}(t) \cdot e^{i \cdot \omega_C \cdot t}\right\} \tag{5.12}$$

$$\begin{aligned} s_{BP}(t) &= \Re\{[I(t) + i \cdot Q(t)] \cdot [\cos(\omega_C \cdot t) + i \cdot \sin(\omega_C \cdot t)]\} \\ &= I(t) \cdot \cos(\omega_C \cdot t) - Q(t) \cdot \sin(\omega_C \cdot t) \end{aligned} \tag{5.13}$$

Figure 5.6 shows the block diagram of a complex I/Q modulator whose mathematical description is depicted in equation 5.12. After the complex multiplication only the real part is used, this is the reason why the quadrature modulator (see figure 5.4) uses the negative term $s_2(t) \cdot \sin(\omega_C \cdot t)$ for the modulation process. As regards equation 5.13, there is an accordance of the complex I/Q modulator and the real I/Q modulator.

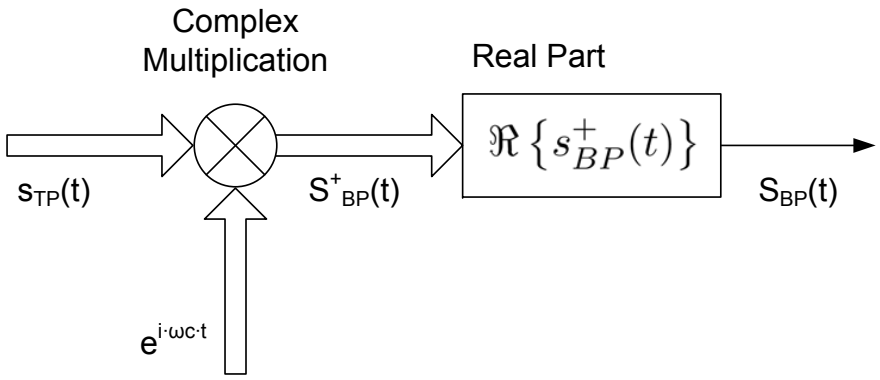
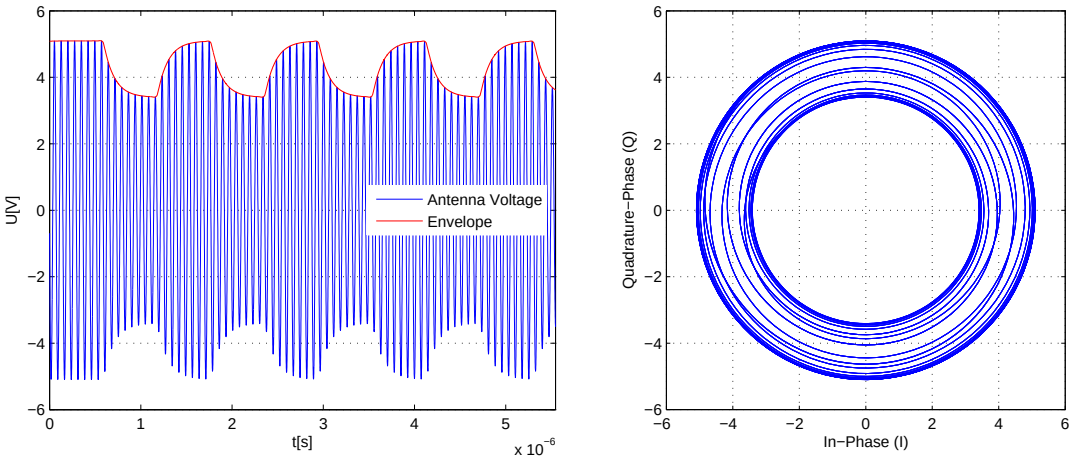


Figure 5.6: Block diagram of a complex I/Q modulator [83]

The imaginary part of an analytic signal is the Hilbert transformation of the corresponding real part. The envelope of the real time signal can be calculated by the magnitude of the analytic signal.

$$A(t) = |g(t)| = \sqrt{I^2(t) + Q^2(t)} \tag{5.14}$$

On the left, figure 5.7 shows a conventional ASK modulation (with a carrier signal $f_c = 13.56\,MHz$) and the dedicated envelope waveform (calculated by the previous equation 5.14). On the right side, figure 5.7 illustrates an X-Y representation of the $I(t)$ and $Q(t)$ signals. This represents the Nyquist plot (locus) of the complex envelope [61], [77], [83], [88] .



(a) (b)

Figure 5.7: ASK modulation with complex envelope and Nyquist plot
(a) ASK modulated carrier signal and the complex envelope (magnitude)
(b) Nyquist plot of the complex envelope

5.2 Receiver Architectures

The essential functionality of a contactless proximity receiving unit is the demodulation and decoding of the load modulated carrier signal which is caused by the transponder. By means of the demodulation process, the modulated signal is shifted backward from the bandpass range to the baseband range. Basically, a distinction between an *incoherent* and *coherent* demodulation takes place [93]. An overview of potential demodulation methods (*coherent/incoherent*) and various receiver architectures will be given. In addition, some conventional RFID reader ICs which have integrated the respective receiver architecture are shown. The mentioned reader ICs are designed for the *High Frequency* (HF, 13.56 MHz) domain and most of the well-established protocol standards (ISO/IEC 14443 A/B, ISO/IEC 15693, HF EPC, FeliCa™ etc.) are supported by these integrated circuits. In the following block diagrams only the receiving units and, in particular, the demodulation methods are depicted. The maximum data transfer rate which is supported by the reader ICs is 848 kbit/sec (standardized in ISO/IEC 14443 Type A/B). Information in datasheets about the exact receiver architectures and the integrated demodulation techniques are restricted by the respective semiconductor manufactures. For this reason only a rough and short description can be given.

5.2.1 Amplitude Demodulator

As mentioned in a previous chapter, the uplink is based on a load modulation which at first looks like a pure amplitude modulation. A simple method to demodulate the load modulated carrier signal is the use of an envelope detector. Because this method requires no carrier signal, it is also referred to as *incoherent* demodulation. Figure 5.8 shows a simple envelope detector consisting of a peak value rectifier and a highpass.

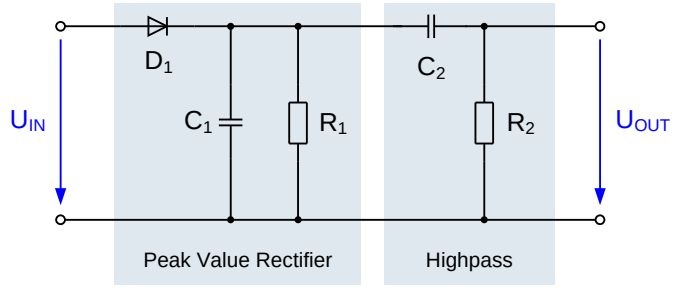


Figure 5.8: Envelope detector [91]

There are two reasons why this concept could not be used in the contactless prototyping reader. Firstly, a correct functionality of the envelope detector requires a significantly higher carrier frequency than the frequency (data rate) of the baseband signal. Consequently, this demodulation technique cannot be deployed in VHBR reader systems. Secondly, the load modulation is not only a pure amplitude modulation but also a phase modulation caused by the magnetic coupling of the two resonant circuits (variation of the distance between reader and transponder antenna). There are cases where the phase modulation predominates over the amplitude modulation. Thus, an envelope detector cannot be used for the present contactless VHBR reader system. However, contactless proximity systems which are based on an envelope detector are particularly used in Asian regions [77], [28]. Figure 5.9 shows a simple integrated receiver architecture whose functionality is based on an envelope detector, offset correction, variable gain amplifier and a comparator [38].

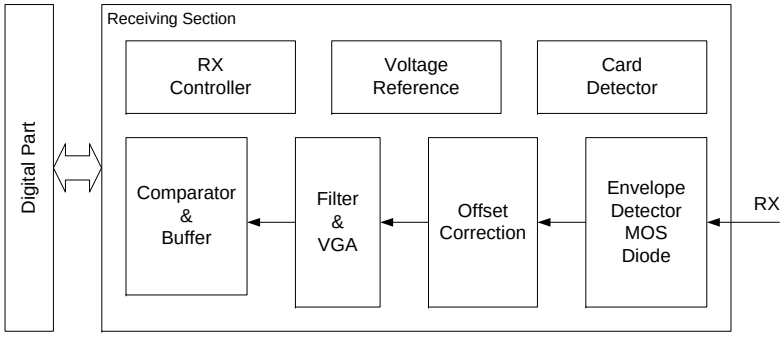


Figure 5.9: Receiver architecture of the reader IC TRH031M [38]

5.2.2 I/Q Demodulator

With the quadrature form of modulation (see section 5.1.3) the baseband data on the In-Phase- and Quadrature-Phase-Channel can be transmitted simultaneously over the transmission channel. For the correct reception of the baseband data (I- and Q-channel) the receiver must use an I/Q demodulator. The principle of load modulation is not based on a quadrature form of modulation (I- and Q-channel) but the I/Q demodulation concept can also be used in contactless proximity receivers. Especially the combination of the amplitude and phase modulation can be detected very effectively and accurately by an I/Q demodulator. Compared to the envelope detector (conventional amplitude demodulator), the I/Q demodulation process requires the carrier signal of the transmitter with the identical frequency and phase relation. For this reason, the I/Q demodulator is also referred to as *coherent* demodulator or *synchronous* demodulator. Figure 5.10 shows the block diagram of a conventional analog I/Q demodulator.

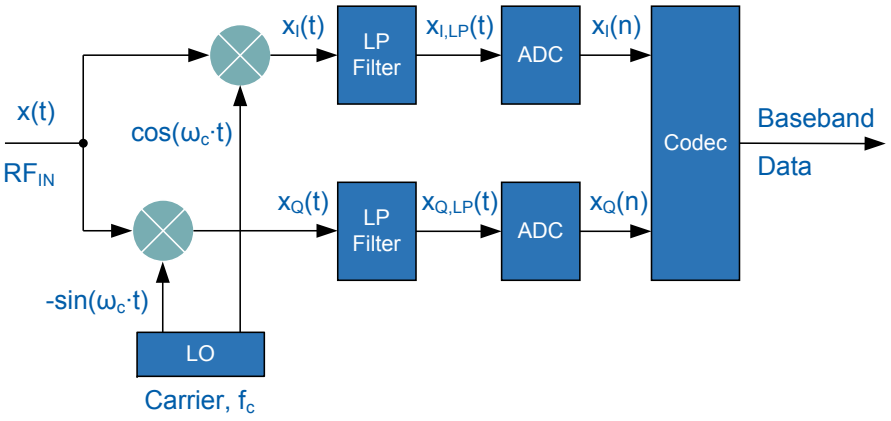


Figure 5.10: Block diagram of a conventional analog I/Q demodulator [19]

First of all, the received signal x_t is divided into the I/Q branches and mixed with the carrier signal (sine and cosine). The mixing process generates signals at double carrier frequency. After lowpass filtering and quantization (ADC) the In-Phase $X_I(n)$ and Quadrature-Phase $X_Q(n)$ components are processed by the *Codec* unit to obtain the baseband data. In the following an ideal mathematical description of the I/Q demodulation process is given, i.e. no noise or other influences are taken into consideration.

The input signal of the conventional analog I/Q demodulator equals the output signal of the quadrature modulator (see figure 5.4).

$$x(t) = s_{BP}(t) = I(t) \cdot \cos(\omega_C \cdot t) - Q(t) \cdot \sin(\omega_C \cdot t) \tag{5.15}$$

The mixing process generates the signals:

$$\begin{aligned} x_I(t) &= x(t) \cdot \cos(\omega_C \cdot t) \\ &= I(t) \cdot \cos^2(\omega_C \cdot t) - Q(t) \cdot \sin(\omega_C \cdot t) \cdot \cos(\omega_C \cdot t) \\ &= \frac{1}{2} \cdot I(t) \cdot [1 + \cos(2 \cdot \omega_C \cdot t)] - \frac{1}{2} \cdot Q(t) \cdot \sin(2\omega_C \cdot t) \\ &= \frac{1}{2} \cdot [I(t) + I(t) \cdot \cos(2 \cdot \omega_C \cdot t) - Q(t) \cdot \sin(2\omega_C \cdot t)] \end{aligned} \tag{5.16}$$

$$\begin{aligned} x_Q(t) &= x(t) \cdot (-\sin(\omega_C \cdot t)) \\ &= -I(t) \cdot \sin(\omega_C \cdot t) \cdot \cos(\omega_C \cdot t) + Q(t) \cdot \sin^2(\omega_C \cdot t) \\ &= -\frac{1}{2} \cdot I(t) \cdot \sin(2 \cdot \omega_C \cdot t) + \frac{1}{2} \cdot Q(t) \cdot [1 - \cos(2 \cdot \omega_C \cdot t)] \\ &= \frac{1}{2} \cdot [Q(t) - Q(t) \cdot \cos(2 \cdot \omega_C \cdot t) - I(t) \cdot \sin(2 \cdot \omega_C \cdot t)] \end{aligned} \tag{5.17}$$

For the conversion the following trigonometric relations are used:

$$\sin^2(x) = \frac{1}{2} \cdot [1 - \cos(2 \cdot x)] \tag{5.18}$$

$$\cos^2(x) = \frac{1}{2} \cdot [1 + \cos(2 \cdot x)] \tag{5.19}$$

$$\sin(x) \cdot \cos(x) = \frac{1}{2} \cdot \sin(2 \cdot x) \tag{5.20}$$

After lowpass filtering:

$$\begin{aligned} x_{I,LP}(t) &= \frac{1}{2} \cdot I(t) \\ x_{Q,LP}(t) &= \frac{1}{2} \cdot Q(t) \end{aligned} \tag{5.21}$$

The frequency spectra in figure 5.11 show the mixing process of the received signal $x(t)$ with the cosine reference signal (within the In-Phase channel).

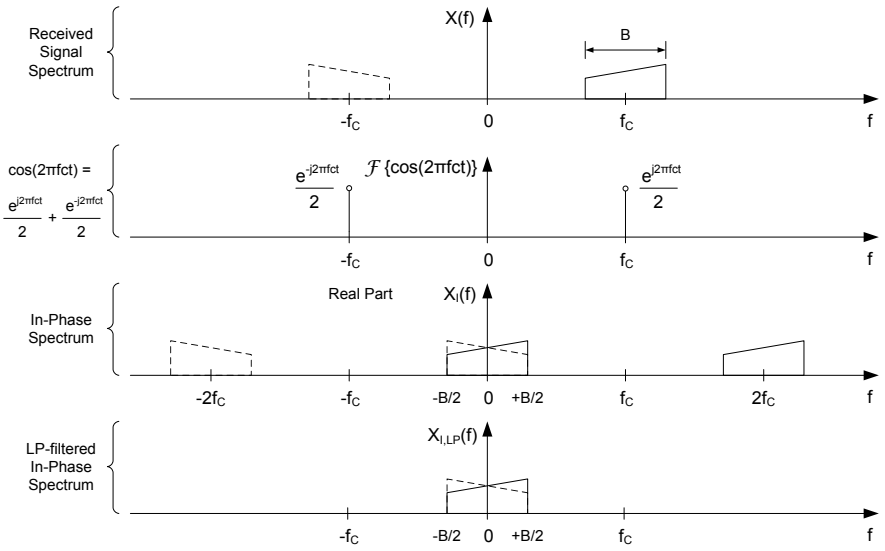


Figure 5.11: Frequency spectra of the mixing process of the received signal $x(t)$ with the cosine reference signal [66]

The mixing process of the signal $x(t)$ with the sinusoidal reference signal (within the Quadrature-Phase channel) is depicted by the frequency spectra in figure 5.12.

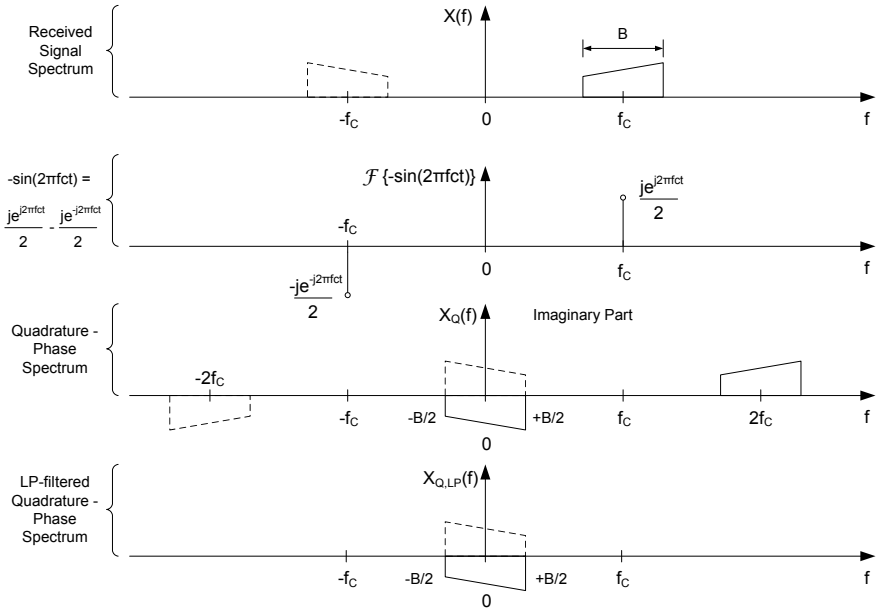


Figure 5.12: Frequency spectra of the mixing process of the received signal $x(t)$ with the sinusoidal reference signal [66]

The addition of the two spectra (one real, one imaginary part) in figure 5.13 results in the spectrum of the complex signal [66].

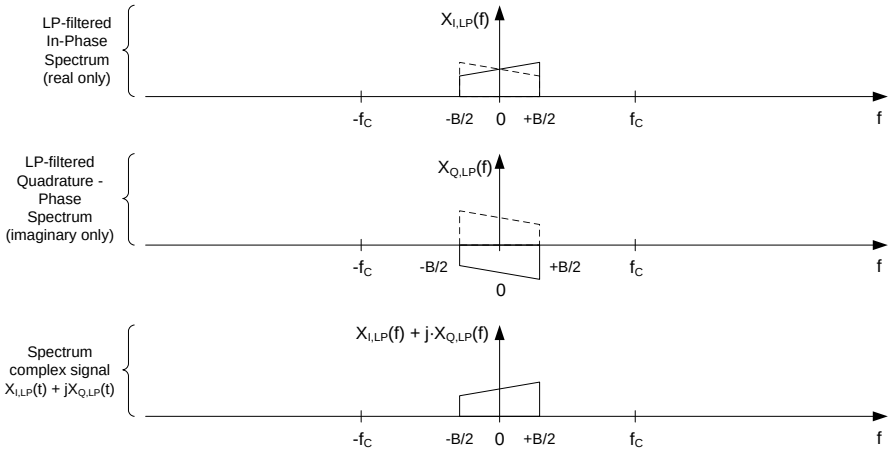


Figure 5.13: Combining the $X_{I,LP}$ and $X_{Q,LP}$ spectra to obtain the $X_{I,LP} + j \cdot X_{Q,LP}$ spectrum [66]

Conventional analog I/Q demodulators have some drawbacks. For correct demodulation the two branches (I- and Q-channel) must be closely matched. DC-offset, quadrature-phase balance or gain balance are possible sources of error and they can be eliminated by the implementation of a digital I/Q demodulation which is shown in figure 5.14. This digital approach is used in *Software Defined Ratio* (SDR) applications where the *Analog-to-Digital Converter* (ADC) is placed as close to the antenna as possible (see section 6.2). The bandpass filter limits the bandwidth of the received signal $x(t)$ to avoid aliasing. After the analog-to-digital conversion the discrete signal $x(n)$ is mixed with the discrete sine/cosine signals and the digital lowpass filter removes the higher frequency components. Especially in contactless receivers for very high bit rates, the adaptation of the digital filter to higher subcarrier frequencies is very simple in comparison to the analog I/Q demodulator [72], [77], [12].

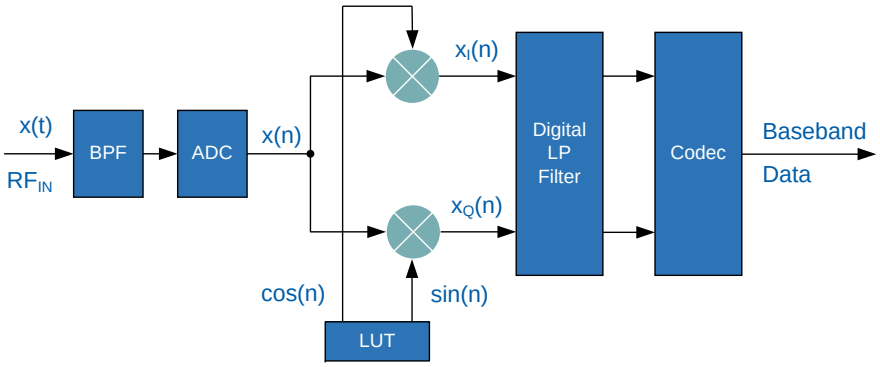


Figure 5.14: Block diagram of a digital I/Q demodulator [72]

Figure 5.15 shows an integrated receiver architecture of the transceiver IC *PN521* (NXP) whose functionality is based on an I/Q demodulation principle. After the demodulation and amplification for the I-branch and Q-branch, an analog-to-digital conversion takes place [74].

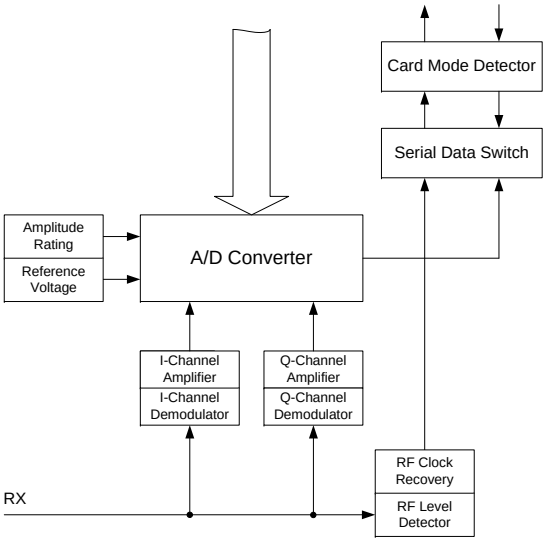


Figure 5.15: Receiver architecture of the reader IC PN512 from NXP [74]

Receiver Architecture Based on an Amplitude- and Phase-Detector

Two other receiver architectures comprise an Amplitude- and Phase-Detector (see figure 5.16). However, no further information concerning the detector principle is given in the respective data sheets [11], [32].

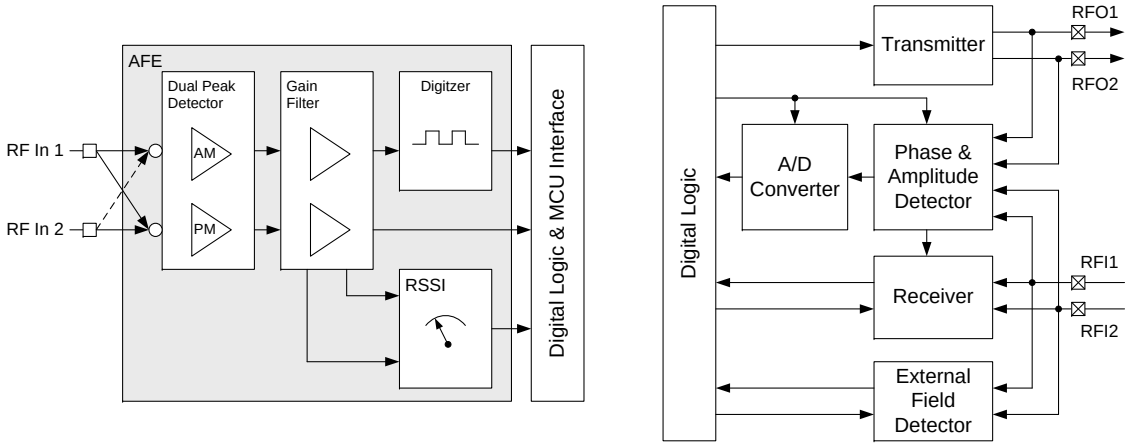


Figure 5.16: Receiver architectures based on an Amplitude- and Phase-Detector,
(a) Reader IC R13MP from IDS [32]
(b) Reader IC AS3910 from austriamicrosystems [11]

5.2.3 Heterodyne Receiver

Figure 5.17 shows the block diagram of a *Heterodyne Receiver*, which is also referred to as *Superheterodyne Receiver* or *IF-Receiver*. The demodulation process is subdivided into two steps. First, the signal band is translated down to an *Intermediate Frequency* (IF), which is much lower than the transmission frequency. After filtering (Anti-Aliasing Filter), amplifying and quantization (ADC), the IF signal is downconverted to the baseband by a complex down-conversion. Figure 5.18 shows the corresponding frequency spectrum [58].

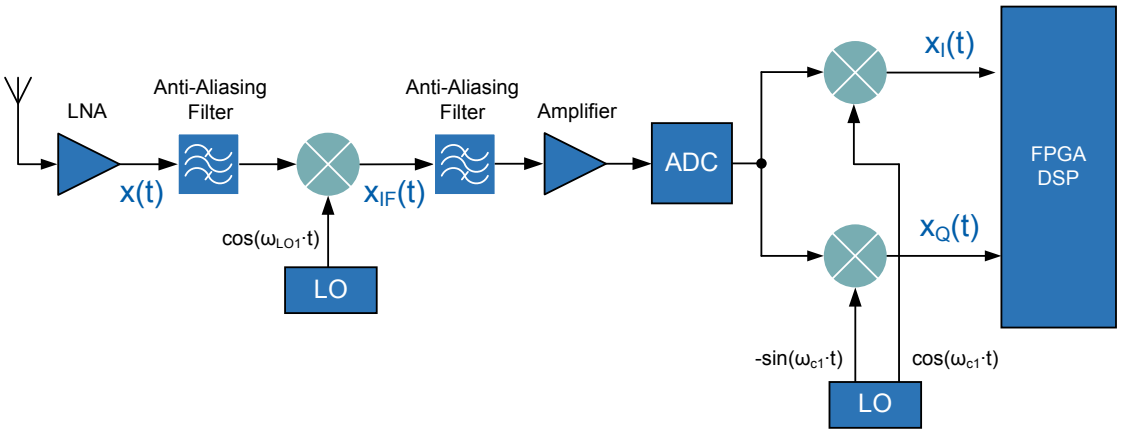


Figure 5.17: Block diagram of a Heterodyne Receiver [58]

Advantages:

- Easy adaptation to different receiver requirements
- Total gain is spread over several amplifiers operating in different frequency bands (i.e. higher stability)
- I/Q separation in digital domain
- Only one ADC required

Disadvantages:

- Higher complexity
- Several local oscillators needed, which cause higher phase noise
- Higher sampling rate of the ADC and more FPGA performance needed

The heterodyne architecture is deployed in UHF RFID reader systems which is shown in section 5.3.

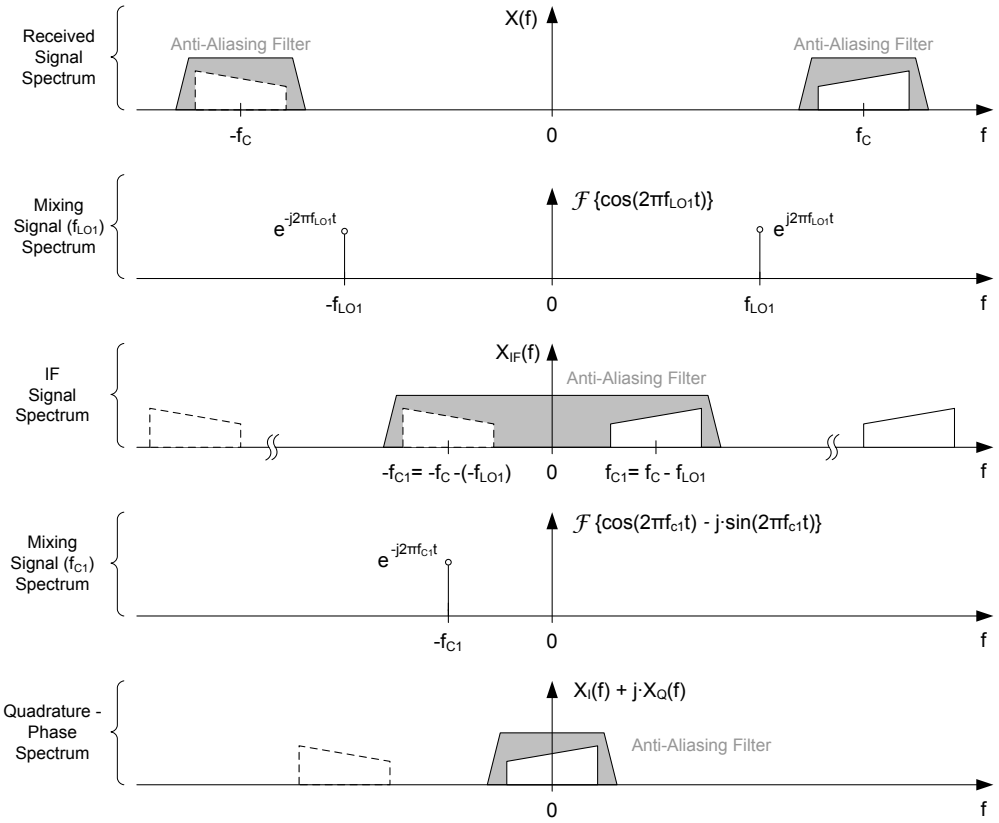


Figure 5.18: Frequency Spectrum of a Heterodyne Receiver [58]

5.2.4 Homodyne Receiver

Figure 5.19 shows the block diagram of a *Homodyne Receiver*, which is also referred to as *Direct Conversion Receiver* or *Zero IF-Receiver*. With the homodyne receiver a down-conversion from the RF bandpass to baseband takes place in a single stage [58]. The functionality is based on the I/Q demodulation principle and is described by the following frequency spectrum in figure 5.20. The homodyne architecture can be deployed in HF RFID reader systems, which is discussed in section 5.3.
Advantages:

- Low complexity
- Suitable for integrated circuits implementation
- Simpler filtering requirements

Disadvantages:

- Totally balanced ADC required
- I/Q imbalance
- DC offset problem

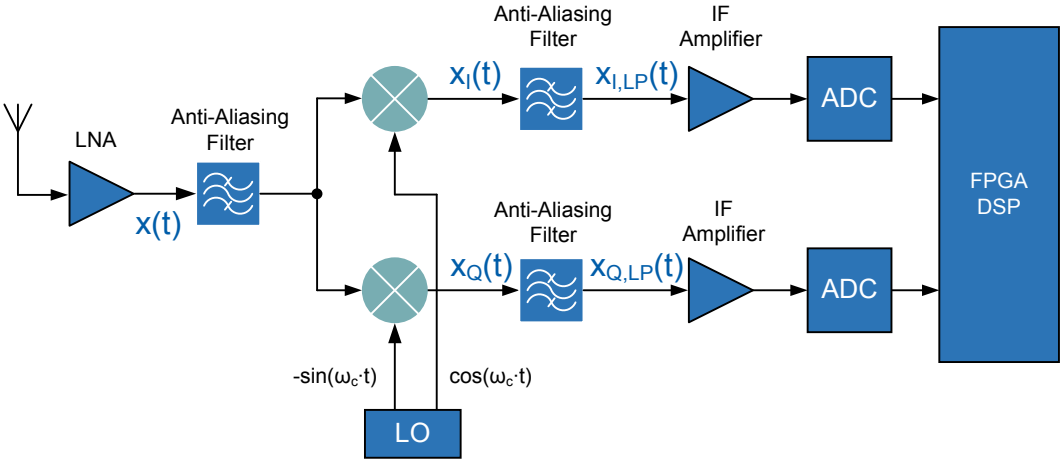


Figure 5.19: Block diagram of a Homodyne Receiver [58]

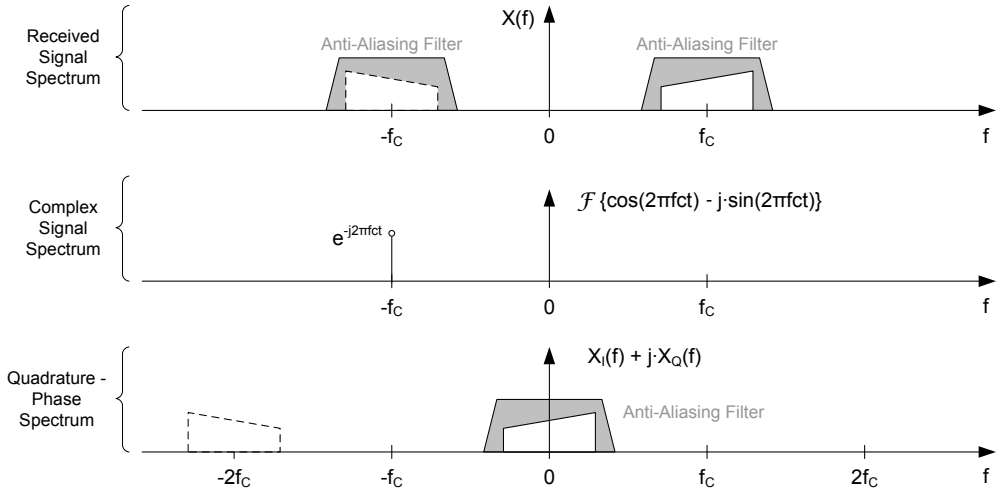


Figure 5.20: Frequency spectrum of a Homodyne Receiver [58]

5.2.5 Low IF Mixer

This receiving method comprises the advantages of the *Homodyne Receiver* and *Heterodyne Receiver*. Figure 5.21 shows the block diagram of the *Low IF-Receiver* architecture at which the analog part is identical to the homodyne receiver and the digital part equals the heterodyne receiver. First of all, the RF signal is downconverted to the intermediate frequency by an analog quadrature demodulator. Next, the down-conversion to the baseband is accomplished by another quadrature demodulator which is realized in the digital domain. The functionality is based on the I/Q demodulation principle for the IF mixing process as well as for baseband mixing. Figure 5.22 shows the corresponding frequency spectrum which describes the two-stage demodulation method [58], [67].

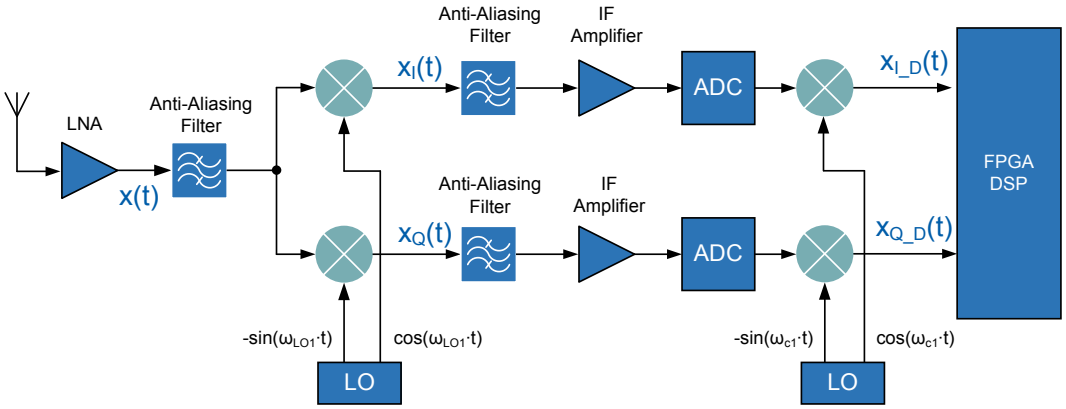


Figure 5.21: Block diagram of a Low IF Receiver [58]

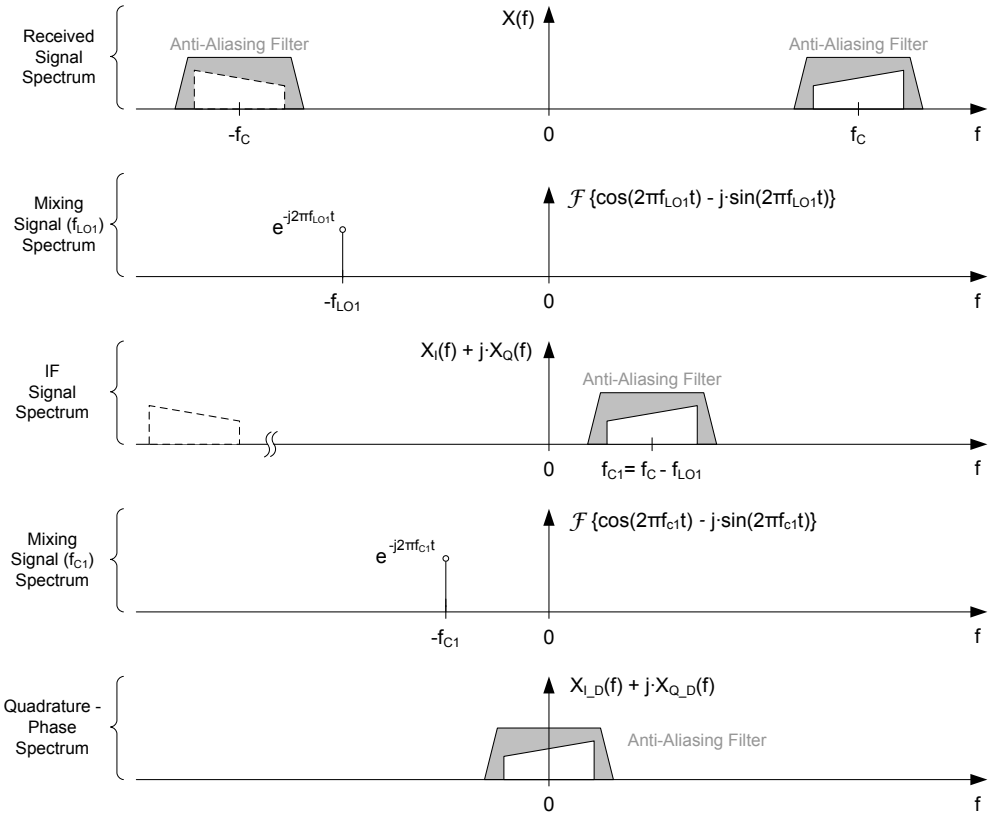


Figure 5.22: Frequency spectrum of a Low IF Receiver [58]

Advantages:

- Avoiding the DC problem of direct conversion
- Lower complexity in the analog domain

Disadvantages:

- Higher complexity in the digital domain
- Higher I/Q imbalance performance required

5.3 Current Research Activities Regarding RFID Transceivers Supporting VHDR

There are several research activities regarding very high bit rates in RFID systems, especially for contactless proximity systems. The VHBR subject is being dealt with by the *Working Groups* (WG) of the ISO and, in addition, companies like NXP Semiconductors or Gemalto are also currently working on the same topic. Different proposals concerning modulation und coding schemes have been elaborated (see chapter 4). The main objective is the elaboration of a common solution for the standardization regarding VHBR. During my literature research, I found several journal papers, articles and theses, all of which discussed VHBR relevant topics like transmission concepts or contactless reader architectures (prototyping systems). This section gives a brief overview of the current research activities regarding RFID transceivers which support standardized data rates (max. 848 kbit/sec in proximity systems) as well as VHBR.

In his master thesis, Ph. Oberstaller [75] presents a contactless demonstration reader front end for very high data rates. An already existing conventional contactless proximity reader is extended by a separate receive path, which processes the very high data rates for the uplink. The demonstration reader board comprises a standard reader unit, an FPGA, an ARM (Microcontroller) and an additional printed board which contains the analog front end. The architecture of the receive path corresponds to a modified Low IF mixer, i.e. the demodulation is realized by a two-stage demodulation process. First of all, the RF signal (13.56 MHz) is downconverted to the intermediate frequency (respective subcarrier frequency) by an analog I/Q demodulator. After filtering, amplifying and discretization by a comparator, the further frequency down-conversion to the baseband is accomplished in the digital domain. The realized demonstration reader supports data rates up to 3.39 Mbit/sec for the uplink, which is four times higher than the currently standardized maximum data rate. Due to the fixed analog components, it is not possible to increase the data rates above the mentioned value. A relevant drawback of the demonstration system is the fact that the reader can only receive VHDR, but is not able to send them.

Continuous and constructive work related to the previous thesis was done in D. Kusternigg's master thesis. [60]. The main objective was to improve the stability of an already existing demonstration reader, especially the optimization of the decoder unit. In this paper, instead of the comparators, two ADCs are used for digitalisation and the filter design is adjusted to a higher frequency range. The algorithm for further signal processing is based on a correlation technique of the received signal. With the improved demonstration reader, the achievable data rate is restricted to maximum 6.78 Mbit/sec, which is eight times higher than the currently standardized maximum data rate. A relevant drawback of the demonstration system is the fact that the reader can only receive VHDR, but is not able to send them.

M. Pichler's diploma thesis [79] describes the implementation of a digital demodulation unit which also supports data rates up to 6.78 Mbit/sec. This thesis as well as the current PhD thesis were part of a comprehensive research project concerning VHBR in contactless proximity systems. The prototyping reader system presented in this work provided a basis for M. Pichler's master thesis. A significant difference to Kusternigg's demonstration reader system is the very high flexibility concerning different modulation/coding methods and data rates. The three last mentioned theses were accomplished at the company Infineon Technologies.

Several journal and conference papers show that other companies like NXP Semiconductors have also been working on the same subject.

Witschnig et al. [37] show an implementation of a high speed RFID lab-scale prototype with a transmission rate up to 6.78 Mbit/sec. However, only the discrete circuit diagram of the PSK demodulator for the transponder is shown.

As far as NFC technology is concerned, also research activities concerning VHBR are under way. Their aim is to increase the currently defined and standardized data rates of 424 kbit/sec to a higher communication speed. Rinner et al. [21] point out physical parameters, limitations and concepts to enhance the data rate for NFC devices. The implemented lab-scale prototype is able to process data rates up to 6.78 Mbit/sec for the downlink. The paper only shows the transmit path of the NFC reader which is realized by an FPGA platform, a DA converter and an RF front end. For the transponder also an FPGA is used and, in addition, the demodulation is realized by an analog I/Q demodulator.

Patauner et al. [18] also show a lab-scale prototype for high speed RFID/NFC applications. Ongoing standardization activities at the ISO/IEC 14443 standard (contactless proximity system) concerning VHBR are pointed out. An implementation of a communication from transponder to reader is shown, with the upper limit of the communication speed again at 6.78 Mbit/sec.

Caucheteux et al. [15] present a fully asynchronous contactless system which provides high data rates, low power and dynamic adaptation. The downlink is realized by a phase modulation and the data rate is limited to 1.02 Mbit/sec. Compared to the other prototyping systems, this value is very low. But by means of the asynchronous event-based communication, a lower power consumption and higher distance range can be achieved.

Vacherand [92] proposes methods to enhance the transmission rate for both communication directions. For the downlink an amplitude modulation with several amplitude levels (up to 16 levels per symbol) is designated. A symbol rate of maximum 847.5 kHz and four bits per symbol leads to the data rate of 3.39 Mbit/sec. The uplink is realized by a multi-phase modulation on the subcarrier. With a 16-PSK and a subcarrier frequency of 1.7 MHz, a theoretical data rate of 6.78 Mbit/sec is possible. The uplink has been tested successfully at a maximum data rate of 1.7 Mbit/sec.

For this thesis, I have examined a number of different hardware architectures of RFID readers (HF and UHF). Although those systems do not support VHBR, a short overview of the research activities will also be given here.

Angerer et al. [4], [5], [6] developed a flexible dual frequency testbed for RFID applications. The testbed setup was realized by a rapid prototyping system which comprises a DSP, an FPGA, ADC, DAC and an RF front end for HF. The associated UHF reader front end is presented by Langwieser et al. [62]. Consequently, the system supports two frequency domains, the HF and UHF domain. The combination of the rapid prototyping system and the UHF reader front end corresponds to heterodyne receiver architectures. The modulation/demodulation process as well as the remaining signal processing for the HF domain is mostly realized in the digital domain. After an envelope detector, the carrier suppressed signal is demodulated with a conventional digital I/Q demodulator. This digital architecture makes the RFID testbed very flexible in regard to different product standards (e.g. EPC Global HF Ver.2 standard, EPC RFID Class-1 Gen2 UHF standard ISO/IEC 15693 standard).

Various articles, conference papers as well as journal papers have been published concerning RFID relevant topics. For the sake of completeness, these publications are referred to but not discussed in detail.

Han et al. [34] present a simulation environment in Matlab/Simulink of an entire RFID system to, discussing different effects like phase noise of the local oscillator, TX-RX coupling, DC offset, I/Q mismatch etc. As this is only a simulation model, no measurement results are presented.

Roy et al. [82] describe the design of an RFID reader architecture based on an FPGA, DSP and analog down-converter and quadrature up-converter. This article describes the partitioning of several tasks (e.g. Modulation/Demodulation, Encoding/Decoding) on the FPGA, DSP, back end processor and the analog components.

Kobayashi et al. [57] present an architecture of a novel dynamic Multi-Protocol RFID Reader/Writer which supports the protocols ISO/IEC 15693, ISO/IEC 18092 (NFCIP-1) and ISO/IEC 18000-4. The architecture is not based on SDR but parameterized hardware. Min et al. [71] present an analog front end circuit for ISO/IEC 14443-compatible RFID interrogators which comprises an analog demodulator.

Gelinotte et al. [31] present an RFID reader system based on an Atmel microcontroller. The reader features synchronous demodulation (In-phase and Quadrature-phase demodulation). By means of a *Programmable Logic Device* (PLD) a reference signal is generated and is mixed with the incoming tag answer. This RFID system is intended to be used in the LF domain (125 kHz), but the synchronous demodulation can also be deployed in HF applications.

The enormous number of references shows clearly that the topic of VHBR in proximity systems is highly relevant and a lot of time is invested in research activities. All referenced VHBR prototyping systems are restricted to a communication speed of maximum 6.78 Mit/sec. It seems the upper limit and state of the art, because there is currently no real system known which is able to process higher data rates. This thesis, however, shows that data rates above 6.78 Mbit/sec are indeed possible for the transponder to reader communication.

5.4 Implemented Modulation Concept (I/Q Modulator)

The conceptual design of the transmit path (for the reader to transponder communication) was uncomplicated and not the main focus of the present work. For this reason, no detailed description of the implementation of the I/Q modulator is given. The block diagram of the implemented I/Q modulator is depicted in figure 5.23.

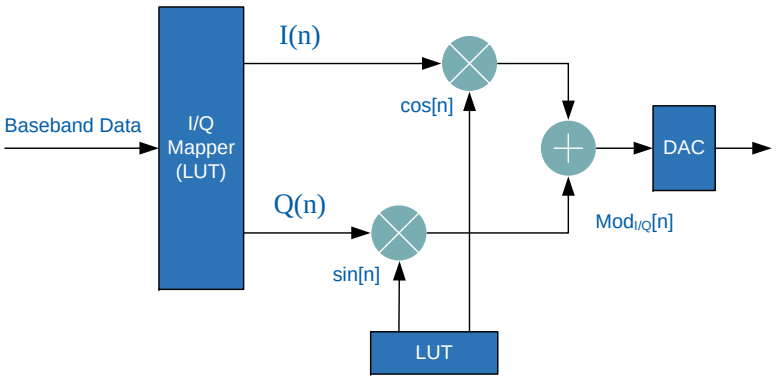


Figure 5.23: Implemented I/Q Modulator

The discrete I/Q modulated carrier is calculated by:

$$Mod_{I/Q}(n) = I(n) \cdot \cos(n) + Q(n) \cdot \sin(n) \tag{5.22}$$

The I/Q modulator is the last module within the transmission path of the reader system (see chapter 6.4). For the generation of the modulated carrier signal (13.56 MHz) two *Look Up Tables* (LUT) are used. Eight sample points per period are used and, therefore, the *Digital to Analog Converter* (DAC) operates with a sampling rate of $8 \cdot 13.56\,MHz = 108.48\,MHz$. The sinusoidal as well as the cosine signal are described with eight discrete values. Those two signals are weighted by the In-Phase and Quadrature-Phase components which are controlled by the baseband data. This task is carried out by the I/Q Mapper which also comprises a look-up table. In a conventional reader system the generation and modulation of the carrier is done in the analog domain. In the new reader concept, these tasks are completely done in the digital domain, which offers a high flexibility concerning exploration of VHDR and supporting various product standards [9].

Figure 5.24 on the left shows the principle of I/Q modulation in the complex plain. Every phase state is defined by one vector, whereas one vector is a geometrical addition of an In-Phase as well as a Quadrature-Phase value.

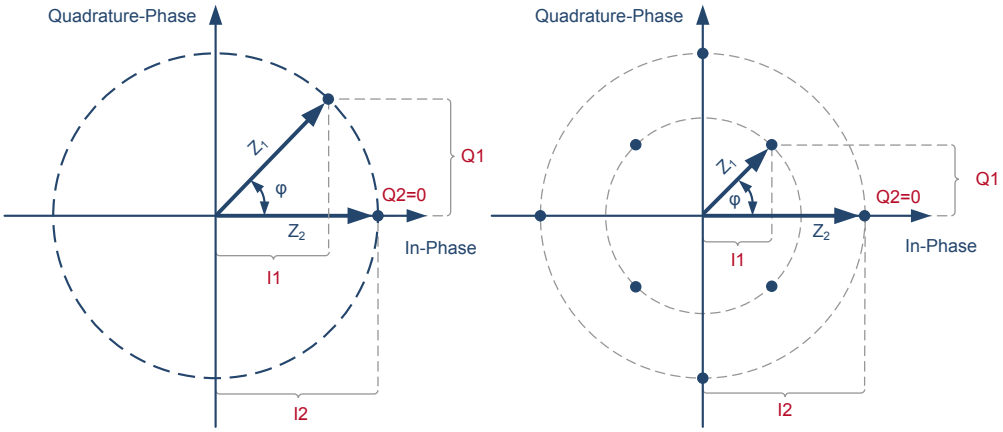


Figure 5.24: I/Q-Plane and constellation diagram of a QAM modulation

For a conventional *Amplitude Shift Keying* (ASK) modulation the Quadrature-Phase (Q=0) is set to zero. Only the In-Phase will be modified by the modulation data. This method is used to fulfil the ASK modulation (10% and 100%) as defined in ISO/IEC 14443 standard. For a *M-ary Phase Shift Keying* (MPSK) or *Quadrature Amplitude Modulation* (QAM) modulation, both the In-Phase as well as the Quadrature-Phase must be modified. Therefore, the encoder collects the data bits and generates the symbols. Figure 5.24 on the right shows an example of a constellation diagram section of a QAM.

5.5 Implemented Down-Conversion Concept

This chapter provides the theoretical consideration of the implemented demodulation concept. The hardware implementation will be explained in the next chapter 6. Conventional contactless proximity receivers are composed of analog components like mixers, oscillators and filters. The parameters and values of these components are defined by several transmission standards. Consequently, a limitation of the receiver concerning data rates, several modulations and coding schemes is given. As mentioned in a previous section, the data transmission from PICC to PCD is based on a load modulation of the carrier signal. This technique basically causes an amplitude modulation and, additionally, a phase modulation of the received carrier signal. For the demodulation of such a modulated signal, usually an analog I/Q demodulator is used which can detect the amplitude and phase information. Existing contactless receivers almost have an analog front end with fixed adjusted filter circuits and mixers for the demodulation. Therefore, the receiver has no ability to deal with high data rates. Additional drawbacks were discussed in section 5.2.2. An alternative to the analog I/Q demodulator is a digital I/Q demodulator architecture which was introduced in section 5.2.2 (see figure 5.14). After bandpass filtering, the carrier signal RF_{IN} is digitized by an ADC. This digital signal is multiplied by the discrete sinusoidal and cosine carrier to obtain the discrete In-Phase and Quadrature-Phase signals. After the digital filtering process (lowpass filter) the codec block outputs the baseband data. The integration of such a digital I/Q demodulator into a conventional contactless proximity reader system is possible. This solution needs an ADC with a higher sampling rate and also higher requirements regarding digital signal processing, i.e. increased complexity of the digital logic.

A substantial and important concept criterion in this thesis was the reduction of the requirements for ADC (sampling rate and resolution), low energy consumption and the reduction of the complexity of the digital and analog part. Reduced power consumption is essential for portable battery powered devices like mobile phones with an integrated contactless reader.

This thesis introduces a new demodulation scheme which can handle the modulation methods and coding schemes which are intended for very high data rates. The proposed receiver architecture of the developed prototyping reader is also very versatile concerning different RFID communication standards (e.g. ISO/IEC 15693, ISO/IEC 14443, ISO/IEC 18000-3 Mode 1 and Mode 2). To increase the flexibility of a contactless receiver, it is preferable to sample the incoming signal directly at the RF frequency. This concept corresponds to an ideal *Software Defined Radio* (SDR) philosophy (see section 6.2) whereas the ADC is positioned to the antenna as close as possible. This results in a minimization of the number of analog components. The load modulated carrier signal is directly converted by an ADC without any analog down-conversion. Instead of a high sampling rate, an undersampling of the load modulated carrier signal is carried out. In the presented architecture dedicated mixers or filters are neither used in the analog nor in the digital domain. The demodulation process translates the passband to the baseband and then usually the analog to digital conversion takes place. Some common techniques for down-conversions were previously discussed.

The down-conversion principle which is applied in the presented work is based on undersampling. Furthermore, this sampling technique is based on aliasing which is used deliberately for down-conversion in this paper. To understand this technique, it is necessary to review the fundamentals of the sampling process.

5.5.1 Fundamentals of Sampling

Sampling and quantization are essential processes of digital communication systems. The analog to digital converter represents the interface between the real system (analog signals) and the digital domain, which works with discrete values. For the mathematical description of an ideal sampling process a periodic sequence of Dirac-Impulses is used:

$$\delta_{periodic}(t) = \sum_{n=-\infty}^{+\infty} \delta\left(t - n \cdot T_S\right) \tag{5.23}$$

An ideal sampling unit can be represented by a multiplier whereas the ideally sampled signal $x_S(t)$ is the product of the analog input signal $x(t)$ and the sequence of Dirac-Impulses:

$$x_S(t) = x(t) \cdot \delta_{periodic}(t) = x(t) \cdot \sum_{n=-\infty}^{+\infty} \delta\left(t - n \cdot T_S\right) \tag{5.24}$$

The character T_S denotes the sampling period and $f_S = 1/T_S$ is the sampling rate. For a better understanding of the sampling process, a Fourier transformation of the sampled signal $x_S(t)$ is carried out, and, therefore, the entire sampling process is depicted in the frequency domain. First of all, a Fourier transformation of the Dirac-Impulse sequence takes place. The Fourier transformation of the Dirac-Impulse sequence in the time domain results in a Dirac-Impulse sequence in the frequency domain again:

$$\Delta_{periodic}(f) = \mathcal{F}\left\{\delta_{periodic}(t)\right\} = \frac{1}{T_S} \sum_{n=-\infty}^{+\infty} \delta\left(f - n \cdot f_S\right) \tag{5.25}$$

A multiplication in the time domain equals a convolution in the frequency domain:

$$x_S(t) = x(t) \cdot \delta_{periodic}(t) \longrightarrow \mathcal{F}\left\{x_S(t)\right\} = \mathcal{F}\left\{x(t)\right\} * \mathcal{F}\left\{\delta_{periodic}(t)\right\} \tag{5.26}$$

$$X_S(f) = X(f) * \Delta_{periodic}(f) \tag{5.27}$$

The spectrum of the sampled input signal $x_S(t)$ is

$$X_S(f) = \frac{1}{T_S} \cdot \sum_{n=-\infty}^{+\infty} \left(X(f - n \cdot f_S)\right) \tag{5.28}$$

The continuous analog signal is sampled at discrete time intervals T_S. If the sampling intervals are equidistant to each other, the sampling process is also called periodic sampling. To ensure an accurate representation of the original analog signal, the sampling intervals T_S and sampling rate f_S respectively must be chosen carefully. Shannon's information theorem and the Nyquist criterion define the right sampling rate. Shannon's theorem says that an analog signal with a limited bandwidth of f_a, must be sampled at a rate of $f_S > 2 \cdot f_a$ in order to avoid the loss of information. The bandwidth may either extend from DC to f_a (*Baseband Sampling* or *Lowpass Sampling*) or otherwise from f_1 to f_2, where $f_a = f_2 - f_1$ (*Undersampling*, *Harmonic Sampling*, *Bandpass Sampling*, *Super Nyquist Sampling* and *Direct IF to Digital Conversion*). Figure 5.25 shows the sampling process in the frequency domain, in which a convolution of the signal spectrum $X(f)$ and the spectrum of the Dirac-Impulse sequence $\Delta_{periodic}(f)$ takes place. The

sampling process for $f_S > 2 \cdot f_a$ results in shifted replicas of the spectrum $X(f)$ with a repetition rate of f_S which is depicted in Figure 5.25c. No overlapping occurs and the original signal can be recovered from the sampled signal $X_S(f)$.

Figure 5.25d shows the case for $f_S < 2 \cdot f_a$, whereas the resulting effect is called aliasing and an overlapping of the spectrum replica takes place. Most of the time, aliasing is undesirable, because a reconstruction of the original signal $X_S(f)$ is not possible anymore. For this reason the sampling rate and an appropriate anti-aliasing filter must be carefully chosen. Otherwise, the intended violating of the Nyquist criterion is a technique which is sometimes used in digital communication applications. The effect of aliasing is used to advantage in the undersampling technique which is discussed in the following. [55], [58], [69], [73]

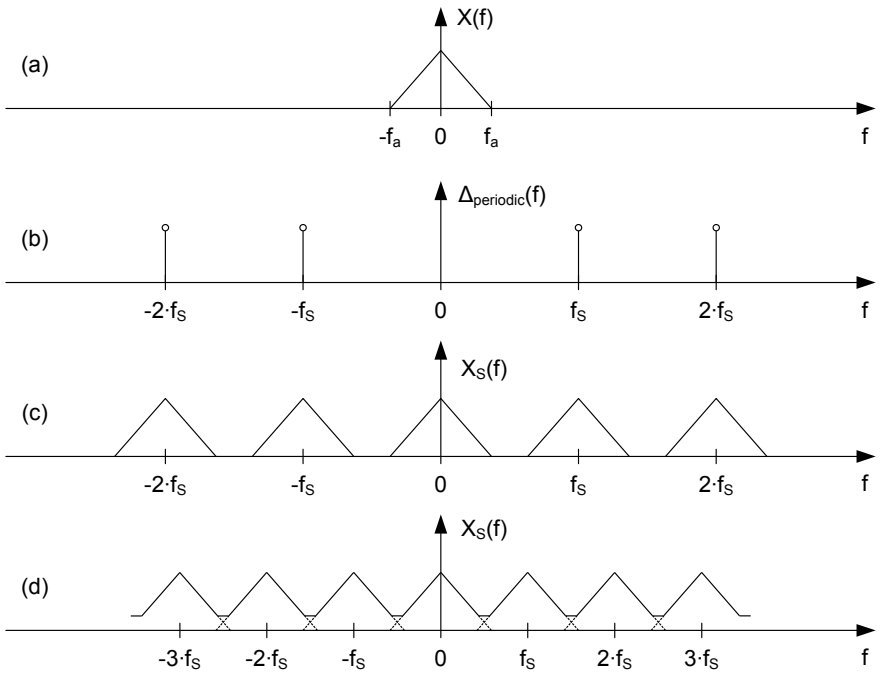


Figure 5.25: The sampling process in the frequency domain: (a) Spectrum of the analog signal with the bandwidth f_a, (b) Spectrum of the periodic Dirac-Impulse sequence, (c) Spectrum of sampled signal $X_S(f)$ with $f_S > 2 \cdot f_a$, (d) Spectrum of sampled signal $X_S(f)$ with $f_S < 2 \cdot f_a$

5.5.2 Analogy of Mixing and Sampling

This section describes the analogy of mixing and sampling, which is one of the crucial points within this thesis. In section 5.2.3 the functionality of a heterodyne receiver was discussed and the mixing (down-conversion) process is subdivided into two steps. The first mixing stage is of interest in which the original signal band at the frequency f_C is translated into an intermediate frequency f_{IF} (see figure 5.26). For mixing (down-conversion), a cosine reference signal with the frequency f_{LO} is used. Figure 5.26c shows the result of the mixing process.

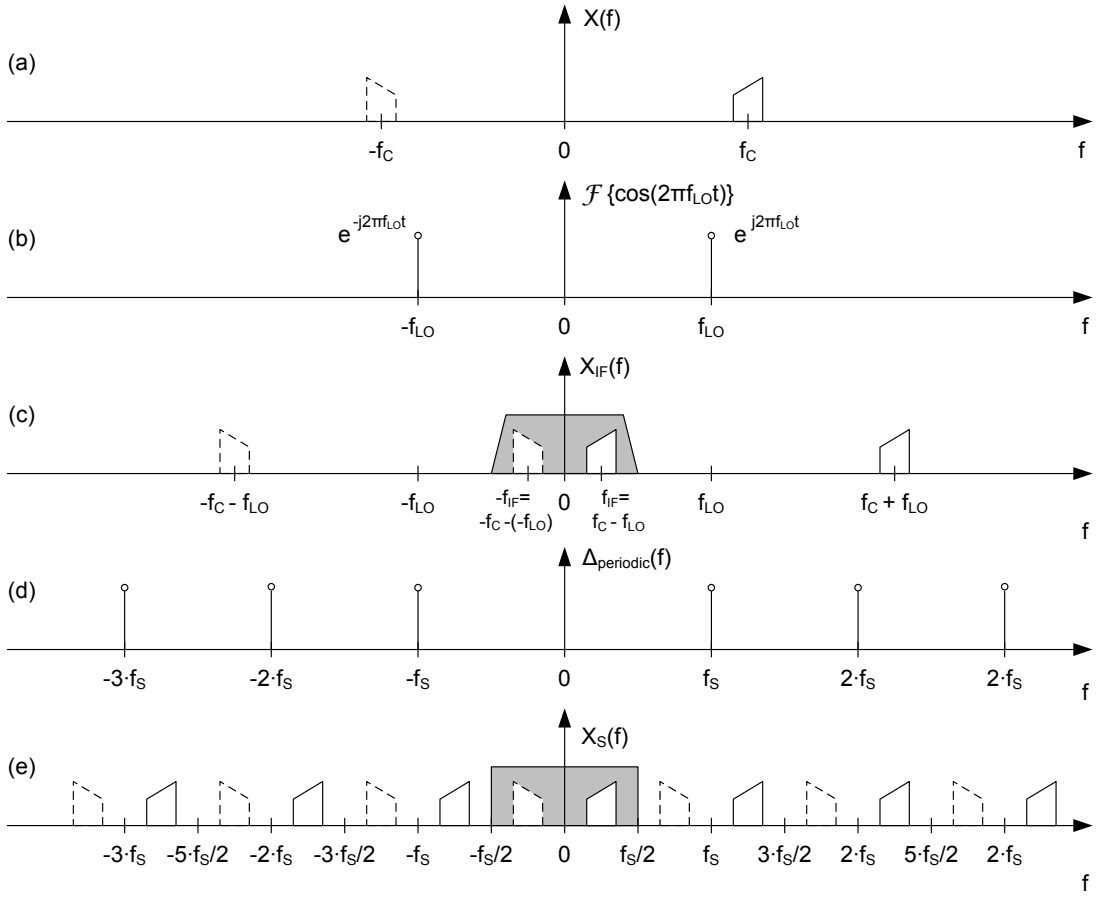


Figure 5.26: Analogy of mixing and sampling in the frequency domain: (a) Spectrum of the analog signal, (b) Cosine reference signal for the mixing process (f_{LO}), (c) Result of the mixing process (f_{IF}, (d) Periodic Dirac-Impulse sequence for the ideal sampling procedure, (e) Spectrum of the sampled signal with $f_S = f_{LO}$

In order to exemplify the analogy of mixing and sampling, the sampling method is also depicted in figure 5.26. Compared with the mixing technique, the sampling frequency f_S is equal to the mixing frequency f_{LO}. The sampling process results in shifted replicas of the spectrum $X_S(f)$ with a repetition rate of f_S (Figure 5.26e). Both, mixing and sampling translate the original signal band to the intermediate frequency. The spectrum replicas are not problematic because the ADC has a very useful characteristic. The ADC acts like an ideal lowpass filter with a cut-off-frequency

of $f_S/2$ and, consequently, the remaining spectrum replicas have no influence on further signal processing. This section has shown the analogy of mixing and sampling; in the next section the undersampling technique will be discussed in detail.

5.5.3 Down-Conversion by Means of Undersampling

This section reflects the fundamentals of the undersampling technique, which is implemented in the contactless prototyping reader. Undersampling and oversampling are opposite techniques. Oversampling uses a higher sampling rate of the ADC which, however, does not provide any additional information. Nevertheless, this technique is often used for digital receivers. If the bandwidth of the wanted signal is close to half of the sampling frequency, the requirements for the anti-aliasing filter concerning edge steepness are very high. Due to the oversampling technique the requirements for the filter can be reduced enormously. Further reading on the topic of oversampling can be found in [56].

As mentioned before, the baseband or lowpass sampling technique is limited to the first Nyquist zone, i.e. the signal bandwidth of the analog signal may extend from DC to $f_S/2$ which is called *Nyquist Bandwidth* (see figure 5.25). The sampling process above the first Nyquist zone is often referred to as *undersampling* (also known under the terms *Harmonic Sampling*, *Bandpass Sampling*, *Sub-Nyquist Sampling* or *Direct IF to Digital Conversion*). The sampling process either causes the spectrum of the actual signal or an aliased spectrum component which falls within the Nyquist bandwidth (first Nyquist zone). Thereby, the sampling frequency f_S of the signal must be at least twice the signal bandwidth $f_a = f_2 - f_1$ and additionally, f_S must be chosen in a way that there is no overlapping of the aliased spectrum replicas. The Nyquist theorem is also valid for the signal bandwidth. Figure 5.27 shows the discussed process of intended aliasing in the frequency domain, with the aliased spectrum component falling within the Nyquist bandwidth.

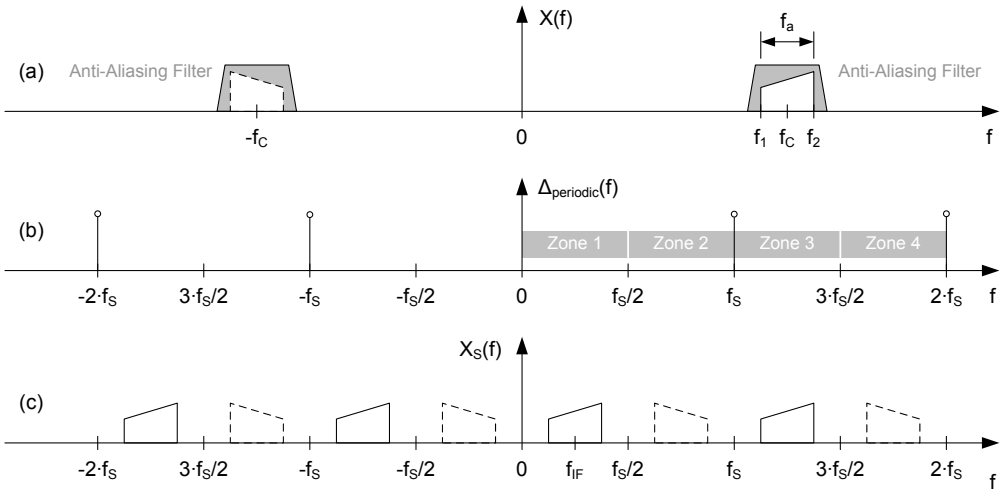


Figure 5.27: Undersampling - intended aliasing in the frequency domain, (a) Spectrum of the analog signal with the bandwidth f_a at f_c, (b) Spectrum of the periodic Dirac-Impulse sequence, (c) Spectrum of sampled signal $X_S(f)$

This process equates to a frequency conversion from the carrier frequency f_C to the intermediate frequency f_{IF}, i.e. undersampling is based on aliasing which is used deliberately for down-conversion and demodulation. The signal $x(t)$ is down-converted from RF to the baseband without external mixers or oscillators. The frequency down-conversion process and sampling task are performed simultaneously. On the one hand, the ADC is used for sampling/digitizing the received signal and on the other hand, it is deployed as down mixer, which means that it deviates from its intended use. This represented demodulation concept is already used in receiver applications, but so far has not been deployed in RFID receivers.

Figure 5.28a shows the already known baseband sampling and 5.28c the method of undersampling. Here, the sampled signal is restricted to the third Nyquist zone and the aliased spectrum image has no frequency reversal in the first Nyquist zone. Another case is depicted in figure 5.28b where the band of the sampled signal is located within the second Nyquist zone. It can clearly be seen that the aliased image has a frequency reversal in the first Nyquist zone. The reversed spectrum can easily be corrected by a *Digital Signal Processor* (DSP). Concerning undersampling two constraints must be considered. Firstly, the signal must be sampled at a rate at least twice as big as the signal bandwidth. Secondly, the band of sampled signals must be restricted to a single Nyquist zone, as to avoid an overlapping of the signal images in the spectrum. [55], [56], [58], [69], [73]

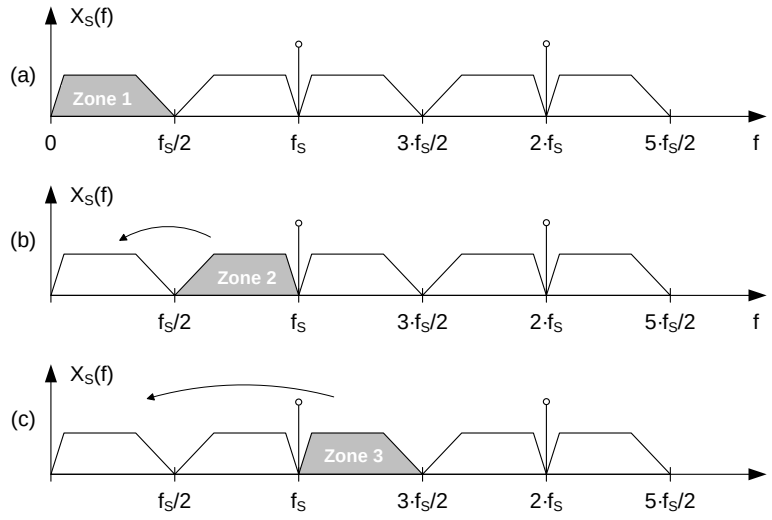


Figure 5.28: Nyquist Zone in the Frequency Domain, (a) Baseband sampling within the first Nyquist zone, (b) Undersampling with reversed Signal Image, (c) Undersampling with no reversed Image

5.5.4 Down-Conversion in the Contactless Prototyping Reader System

The implementations of the receiver architectures, demodulation schemes and sampling technique are all carried out in the frequency domain. Thereby, the frequency spectra always show a carrier signal that is directly modulated by the baseband data. Those spectra differ from the frequency spectrum of most of the RFID applications, because the carrier signal is load-modulated by a subcarrier signal and not directly by the baseband signal. Section 3.2 explains the generation of the two-stage modulation in the time and frequency domain.

5.5.4.1 Undersampling Based on the carrier frequency

First, the result of the load modulation in the frequency domain must be considered to achieve a correct down-conversion by the undersampling technique. This is shown in figure 5.29a at which a carrier signal with $f_c = 13.56\,MHz$ and a subcarrier frequency f_{Subc} is used. The subcarrier signal is modulated by the baseband data with the bandwidth B_D. Next, the load modulation of the carrier signal with the modulated subcarrier takes place. The load modulation process generates two spectral lines which are placed symmetrically around the spectral line of the carrier ($f_c - f_{Subc}$ and $f_c + f_{Subc}$). The sidebands of the subcarrier signal contain the baseband data.

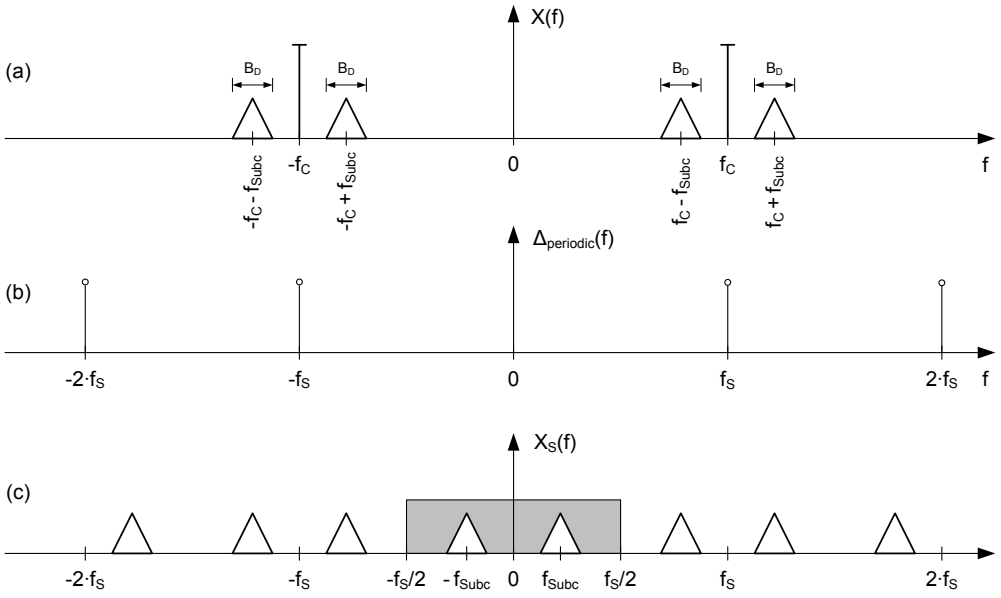


Figure 5.29: Undersampling based on the carrier frequency: (a) Spectrum of the load modulated carrier signal, (b) Spectral representation of the sampling function with $f_S = f_C$, (c) Spectrum of the sampled and down converted signal

Figure 5.29c shows the result of undersampling in the frequency domain, whereas the sampling frequency equates to the carrier frequency. The generated spectrum replicas are not problematic because the maximum frequency of the ADC output signal equals to the half frequency of the sampling signal, i.e. the ADC sampling process limits the frequency of the output signal like an

ideal lowpass filter. Since the load modulation is a two-stage modulation process, the undersampling method based on the carrier frequency results in the subcarrier waveform. In order to obtain baseband data, a further decimation step is necessary, which will be discussed later.
The upper graph of figure 5.30 shows the result of undersampling in the time domain. The carrier signal is load modulated by an unmodulated subcarrier signal with a frequency of 847.5 MHz ($f_c/16$) which is defined in the standard ISO/IEC 14443-Type B. One subcarrier period consists of 16 carrier periods. Once again, the sampling frequency equates to carrier frequency and, consequently, this method eliminates the carrier signal of 13.56 MHz.

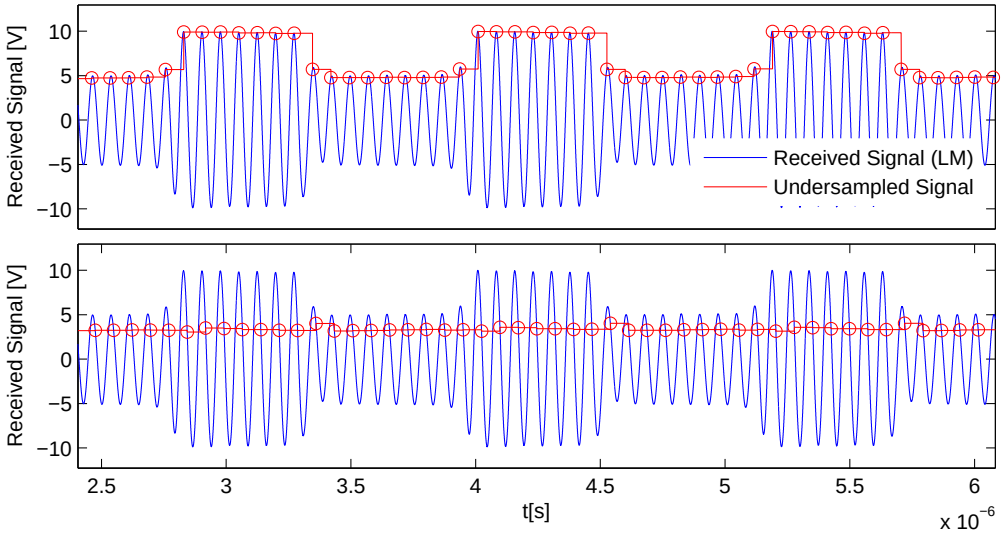


Figure 5.30: Undersampling of a load-modulated carrier signal based on the carrier frequency

The clock frequency for undersampling is derived from the carrier clock which is already used for the modulation unit of the contactless prototyping reader. Consequently, the downsampling frequency is synchronous to the carrier signal concerning the frequency. Moreover, the digital hardware logic of the transponder is provided with the clock signal which is derived from the carrier field clock, i.e. the subcarrier frequency and hence the answer of the transponder are also synchronous to the carrier clock concerning the frequency. However, the start point of the PICC response is not defined (with the exception of the Initialization- and Anticollision-Sequence in the standard ISO/IEC 14443-Type A) and therefore a synchronization concerning phasing is not given. The undersampling method is based on a *non-coherent* demodulation, i.e. the start point of the carrier can vary and then the sampling points are not in phase with the carrier frequency. There exist several demodulation schemes which require a frequency and phase synchronization (*coherent demodulation*) between the sampling signal and the carrier signal. But in the prototyping reader system no synchronization mechanism for the sampling process is implemented and so the timing of sampling is arbitrary.
The lower graph of figure 5.30 also shows the result of undersampling, but the start point of the sampling process differs from the graph above. It can clearly be seen that the result of undersampling is not suitable for further signal processing, because the down sampled signal contains no information, i.e. the timing of sampling (start point) is essential for the resulting signal quality. A single undersampling channel (based on carrier frequency) is not applicable

and, therefore, an extension of a second undersampling channel is necessary.

5.5.4.2 Non-Uniform-Sampling for I/Q Separation

The *non-uniform* sampling technique is an enhanced sampling method which provides an additional undersampling channel [58]. Undersampling based on only one channel is not the adequate solution for down-conversion, which should provide a sufficient and reliable signal quality. Figure 5.31 shows the method of *non-uniform* in which the In-Phase (I) and the Quadrature-Phase (Q) components of a harmonic signal are divided. For improved visualization, both the cosine signal (red curve) as well as the sinusoidal signal (blue curve) are depicted, which show the phase relation of $90°$ between the In-Phase and Quadrature-Phase component. Q_1 is the respective Quadrature-Phase component to the In-Phase component I_1; a conventional I/Q demodulator (see section 5.2.2) delivers those two values after mixing and filtering at the same time.

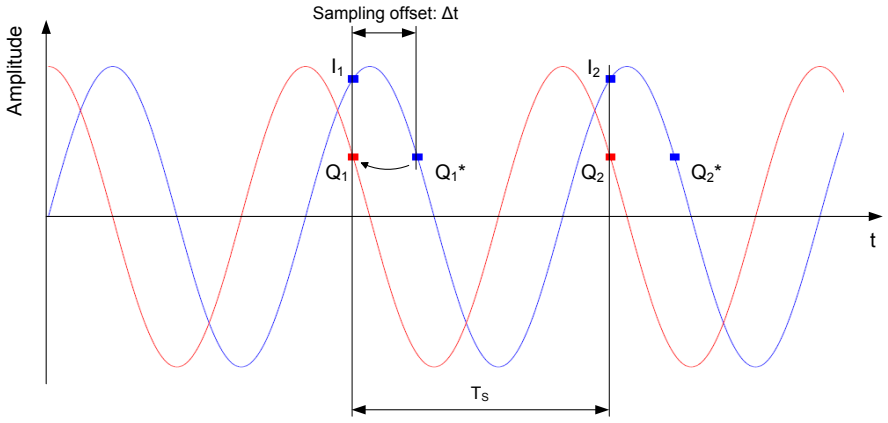


Figure 5.31: Non-uniform sampling - I/Q Separation [58]

$$\Delta t = \frac{\pi/2}{\omega_{Carrier}} = \frac{\pi/2}{2 \cdot \pi \cdot f_{Carrier}} = \frac{1}{4 \cdot f_{Carrier}} = \frac{T_S}{4} \mathrel{\widehat{=}} 90°$$

The non-uniform sampling technique uses a sequential sampling method for the I/Q separation, i.e. the values I_1 and Q_1^* are taken by the ADC with a time offset of $T_S/4$ which equates to $90°$ based on the carrier signal. The components Q_1^* and Q_1 have the same value and, consequently, the sampling value Q_1^* can be used for Q_1 which is the adequate quadrature component to I_1. The term *non-uniform* relates to the timing of taken sampling points, i.e. the time period between two consecutive sampling points are non-uniform. Due to the 90 degree sampling offset on the carrier signal, the method guarantees that at least one of the two channels always has an adequate signal quality. The sampling of the I-phase and Q-phase components is done by the ADC, i.e. the I/Q demodulation process is performed by the ADC.

There exist several digital demodulation schemes which are based on the similar I/Q separation method described above. A new approach for the I/Q demodulation in the digital domain can be found in R. Xue et al. [96]. This paper presents a demodulation method to minimize the hardware complexity and makes components like multiplier, filter or oscillator redundant. The disadvantage of the approach is the required frequency and phase synchronization between the sampling signal and the carrier signal. C. Ziomek et al. [98] present a two-stage demodulation architecture, in which an analog demodulator (first stage) shifts the received signal into the intermediate frequency domain. The second demodulation stage is realized in the digital domain, when the IF signal is sampled by an ADC which operates at a frequency of $4 \cdot IF$. Consequently, the time period between two consecutive samples corresponds to exactly $90°$ at the IF.

The upper graph of figure 5.32 is a detailed representation of the lower graph, which shows the result of the *non-uniform* sampling technique applied to a load-modulated carrier signal. In the lower graph the In-Phase and Quadrature-Phase channels are depicted. It can clearly be seen that the I/Q sampling process results in two channels (subcarrier waveforms) with a different signal quality respective.

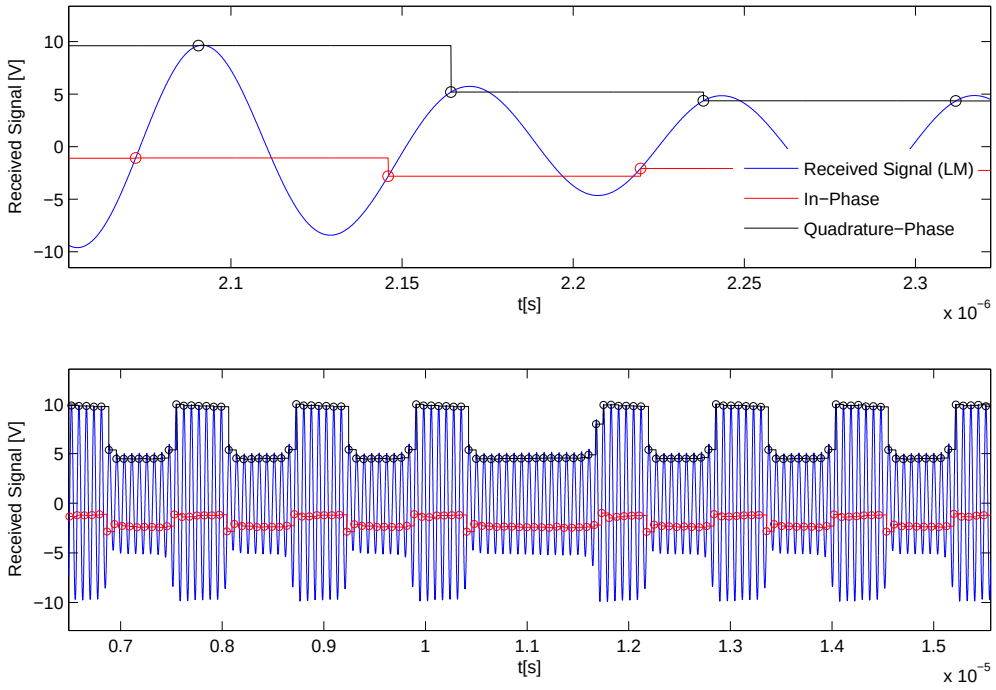


Figure 5.32: Non-uniform sampling technique applied to a load modulated carrier signal

The signal strength and hence the signal quality of each channel depends on the phase offset of the sampling points and the input signal. This offset between the sampling points and carrier signal is unknown. This fact must be considered by the further signal processing. The algorithm which is implemented in the prototyping reader system for further post processing will be introduced and explained in chapter 6.5.2. The load modulation is a combination of amplitude and unintentional phase modulation. The additional phase modulation is caused by the detuning of the two coupled reader and transponder resonant circuits, depending on the distance between

reader and transponder. The introduced and implemented digital I/Q separation technique offers the possibility of demodulating the amplitude as well as the phase modulated carrier signal. Since the load modulation is a two-stage modulation process, the non-uniform sampling method based on the carrier frequency results in the subcarrier waveform. However, the subcarrier waveform still has the time resolution of the carrier period. Either the redundant amount of data, caused by sampling, can be reduced by a further digital decimation or the sampling frequency is reduced from the carrier frequency to the respective subcarrier frequency. The next section describes this undersampling method based on the subcarrier frequency.

5.5.4.3 Undersampling Based on the Subcarrier Frequency

A modification of the undersampling frequency from the carrier to the respective subcarrier frequency reduces a lot of redundant sampling data. First of all, the method of undersampling based on the subcarrier frequency is shown in the frequency domain again. Figure 5.33a shows the spectral representation of a load-modulated carrier signal.

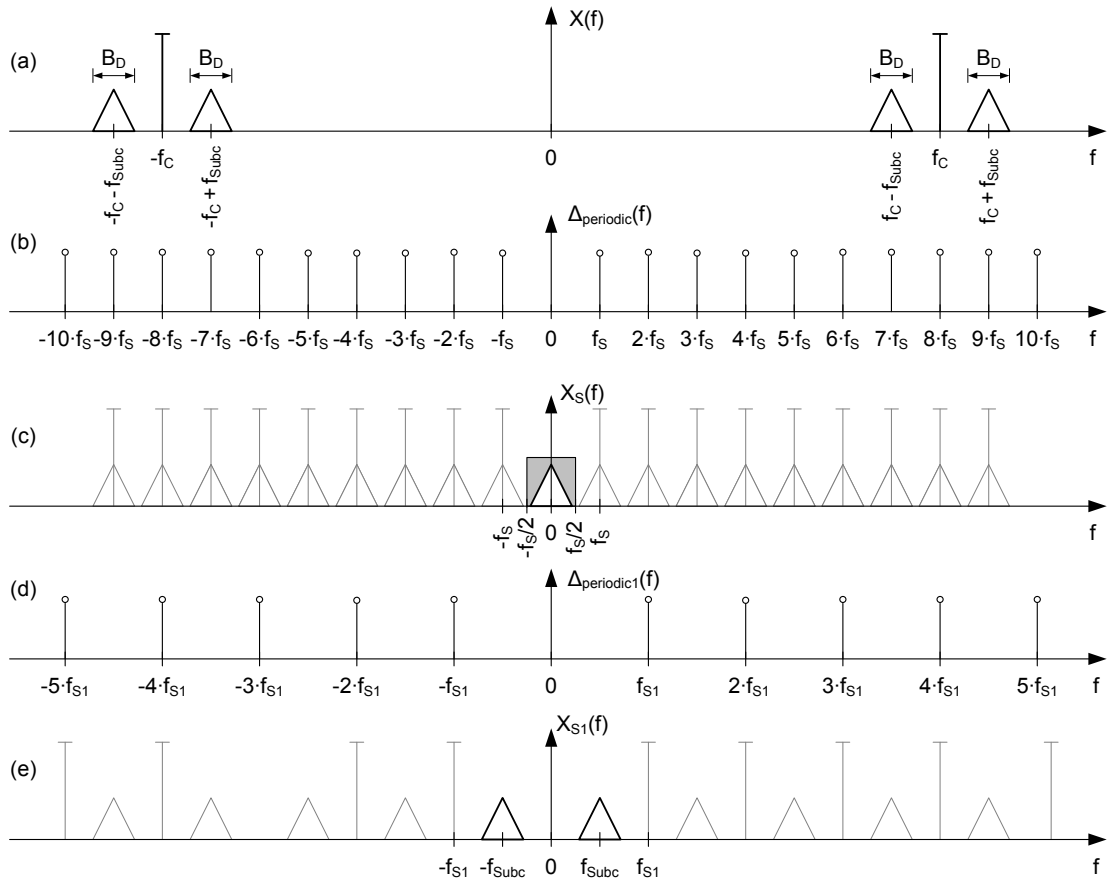


Figure 5.33: Undersampling based on the subcarrier frequency: (a) Spectrum of the load-modulated carrier signal, (b)(d) Spectral representation of the sampling function with $f_S = f_{Subc}$ and $f_{S1} = 2 \cdot f_{Subc}$, (c)(e) Spectrum of the sampled and down-converted signal for both sampling frequencies

Figure 5.33c shows the result of undersampling in the frequency domain. Here, the sampling frequency equates to the subcarrier frequency $f_S = f_{Subc}$. Because of intended aliasing, the passband around the subcarrier frequency is shifted downwards into the baseband. The upper graph of figure 5.34 shows the undersampling result in the time domain. It can clearly be seen that the obtained waveform (red curve) corresponds to the baseband data. Every phase change (BPSK) of the subcarrier signal corresponds to a state change of the baseband signal which is NRZ-L coded. This would be a simple solution to obtain the baseband directly, but it is not applicable because the further signal post processing unit requires a subcarrier waveform for synchronization and channel estimation.

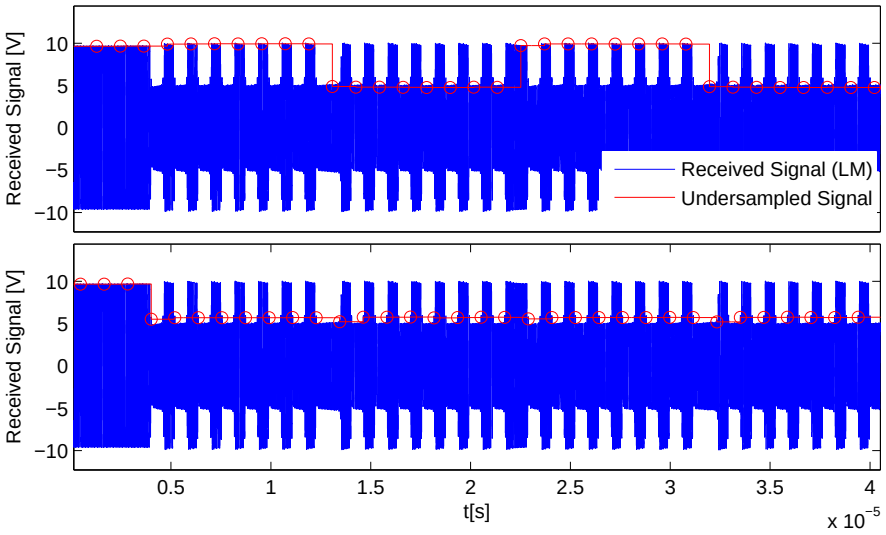


Figure 5.34: Undersampling of a load-modulated carrier signal based on the subcarrier frequency

Additionally, the lower graph of figure 5.34 also shows the result of undersampling based on the subcarrier frequency, but the start point of the sampling process differs from the graph above. The undersampling points are closely in the transition of load modulation *active* and load modulation *inactive*. At these transitions a settling behavior appears which is caused by the transient response of the resonant reader circuit (depending on the quality factor). The result is not suitable for further signal processing, because the downsampled signal contains no information. For this reason the undersampling frequency is increased to the double subcarrier frequency $f_S = 2 \cdot f_{Subc}$. Figure 5.33e shows the result of undersampling in the frequency domain. But only a doubling of the undersampling frequency is not sufficient, which shows the red waveform in the upper graph of figure 5.35. The undersampling points are closely in the transition of the load modulation and the result is not satisfactory, because, once more, the downsampled signal contains no information. Therefore, a second subcarrier channel was established based on an additional digital I/Q separation on the subcarrier signal. The upper graph of figure 5.35 is a detailed representation of the lower graph and both show the result of I/Q sampling on the subcarrier signal.

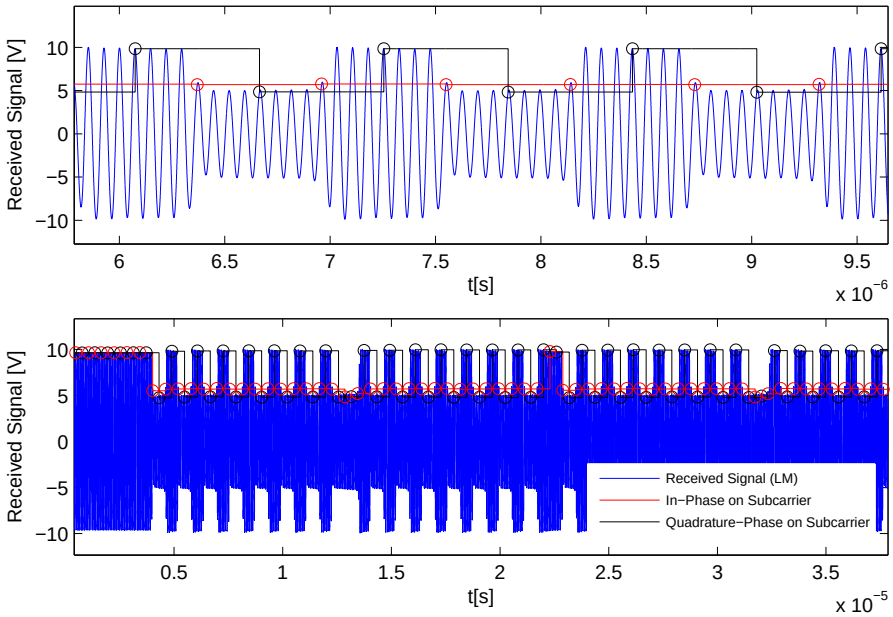


Figure 5.35: Undersampling and I/Q separation based on the subcarrier frequency

5.5.4.4 Undersampling and I/Q Separation on Carrier & Subcarrier Signal

The elaborated undersampling and I/Q separation method which was finally applied within the prototyping reader system is a combination of I/Q sampling based on the carrier signal as well as I/Q sampling based on the subcarrier signal. The I/Q sampling method based on the carrier signal is essential for a correct demodulation of the amplitude as well as the phase modulated carrier signal. Moreover, this method is required for the proper non-coherent demodulation, especially since no synchronization between the sampling signal and the carrier signal concerning phasing takes place. With the I/Q sampling method based on the subcarrier signal a reduction of the sampling rate as well as sampling data is given. The sampling rate for the I/Q separation on the subcarrier signal was doubled because the sampling rate would otherwise be too low. The clocking scheme and the result of the used undersampling and I/Q separation method is shown in figures 5.36 and 5.37.

The reason why the undersampling technique could be applied in the contactless prototyping reader system is described in the following. The carrier signal at a frequency of 13.56 MHz is load modulated by the transponder. For a complete and accurate reconstruction of the load modulated carrier, a sampling rate of $> 27.12\,MHz$ is necessary. But there is no need to determine and reconstruct the entire carrier signal at the receiver unit. Solely the correct recovery of the information which is modulated on the carrier signal is necessary and not the carrier itself. At a pure amplitude modulation the envelope of the carrier signal comprises the entire information. For our purpose, the envelope of the carrier which is caused by the load modulation is interesting. The simulation as well as the measurement results concerning the implemented undersampling and demodulation method are shown in chapter 7.4.1.

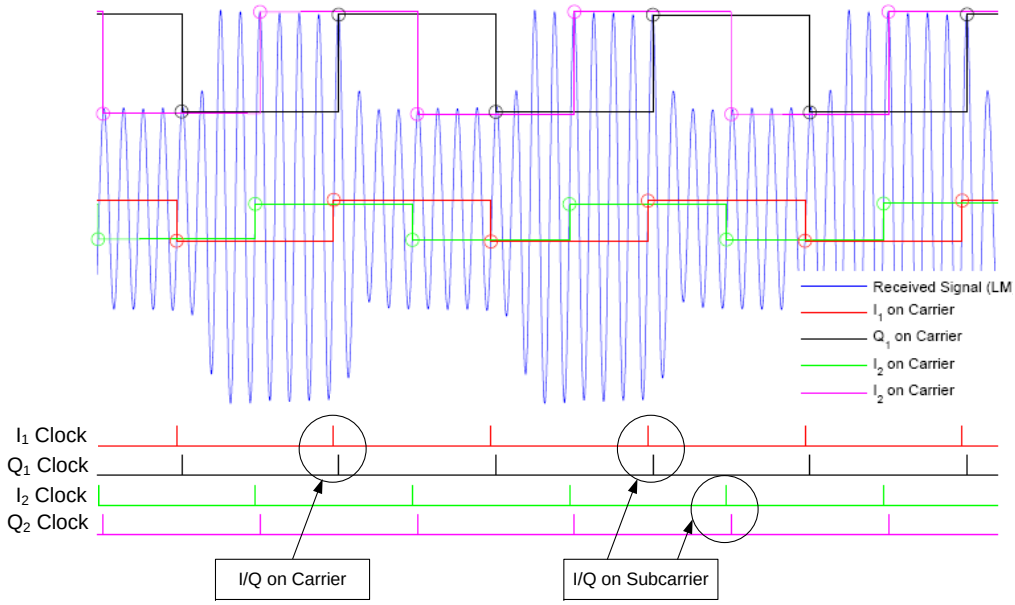


Figure 5.36: Clocking scheme for undersampling and I/Q separation (based on carrier & subcarrier signal)

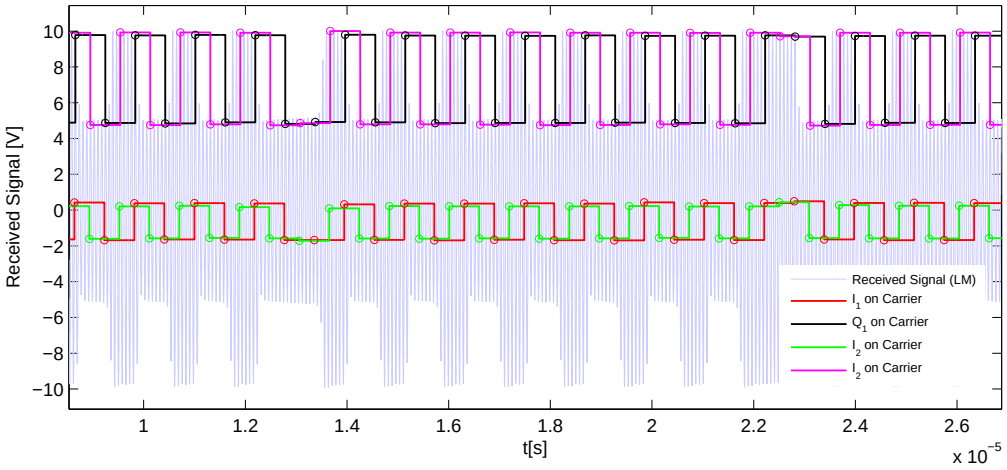


Figure 5.37: Undersampling and I/Q separation based on carrier and subcarrier frequency

5.5.4.5 Hardware Architecture for Undersampling

There are different solutions to implement the discussed methods for down-conversion. Figures 5.38 and 5.39 show two approaches for down-conversion: One is based on one and the other on two ADCs, which results in four channels CH1-CH4. The term D_{SC} was introduced in section 4.2.2 and denotes the subcarrier divisor. This factor is the ratio of carrier to subcarrier frequency $D_{SC} = f_C/f_{SC}$ and is used as downsampling factor. Figure 5.38 shows an example for downsampling and channel separation based on one ADC. The I/Q channel separation based on the carrier signal is achieved by the ADC. To obtain the $\pm 90^\circ$ resolution for the I/Q separation, the ADC must be provided with a clock frequency (54.24 MHz) four times larger than the frequency of the carrier signal. The I/Q channel separation based on the subcarrier signal is carried out by the downsampling units which use the downsampling factor D_{SC}.

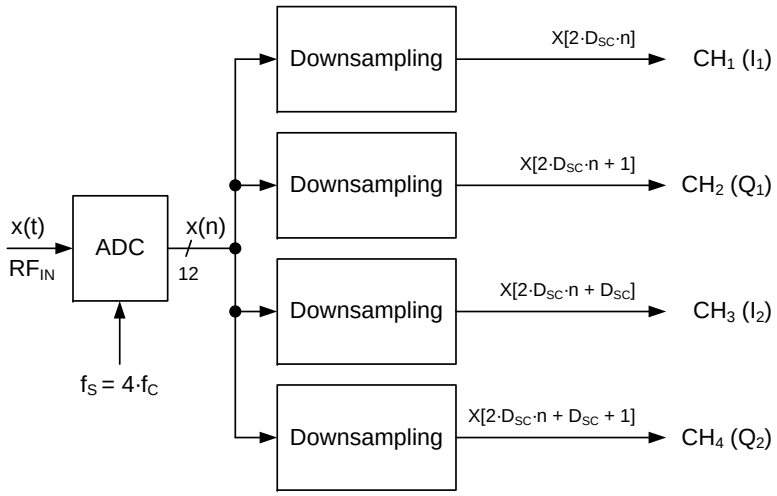


Figure 5.38: Downsampling and channel separation based on one analog-to-digital converter

Another approach for downsampling and channel separation is shown in figure 5.39. The sampling frequency can be reduced if a second ADC is used, because the sampling frequency of one ADC only needs a 90° resolution based on the respective subcarrier frequency [51], [52].

$$\begin{aligned} ch_1[n] &= x[2 \cdot D_{SC} \cdot n] \\ ch_2[n] &= x[2 \cdot D_{SC} \cdot n + 1] \\ ch_3[n] &= x[2 \cdot D_{SC} \cdot n + D_{SC}] \\ ch_4[n] &= x[2 \cdot D_{SC} \cdot n + D_{SC} + 1] \end{aligned} \tag{5.29}$$

The clocking schemes for the presented downsampling approaches are shown in figure 5.40. It is an adaptive sampling technique which is adapted to the respective data rate. An uplink communication which is based on the subcarrier establishes data rates up to 6.78 Mbit/sec. To reach data rates beyond the mentioned value, another method must be used for the uplink. The elaborated and implemented transmission concept for contactless proximity systems was

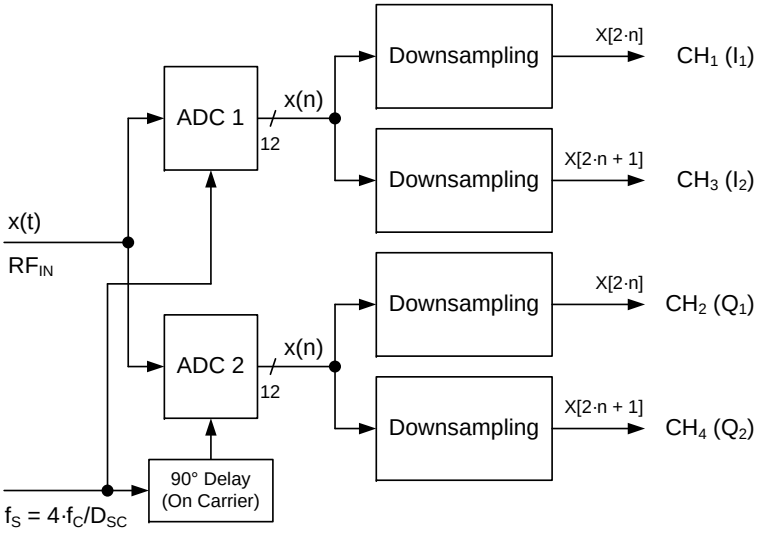


Figure 5.39: Downsampling and channel separation based on two analog-to-digital converters

introduced in section 4.2.4. With this method the carrier signal is load-modulated by the NRZ coded baseband directly.

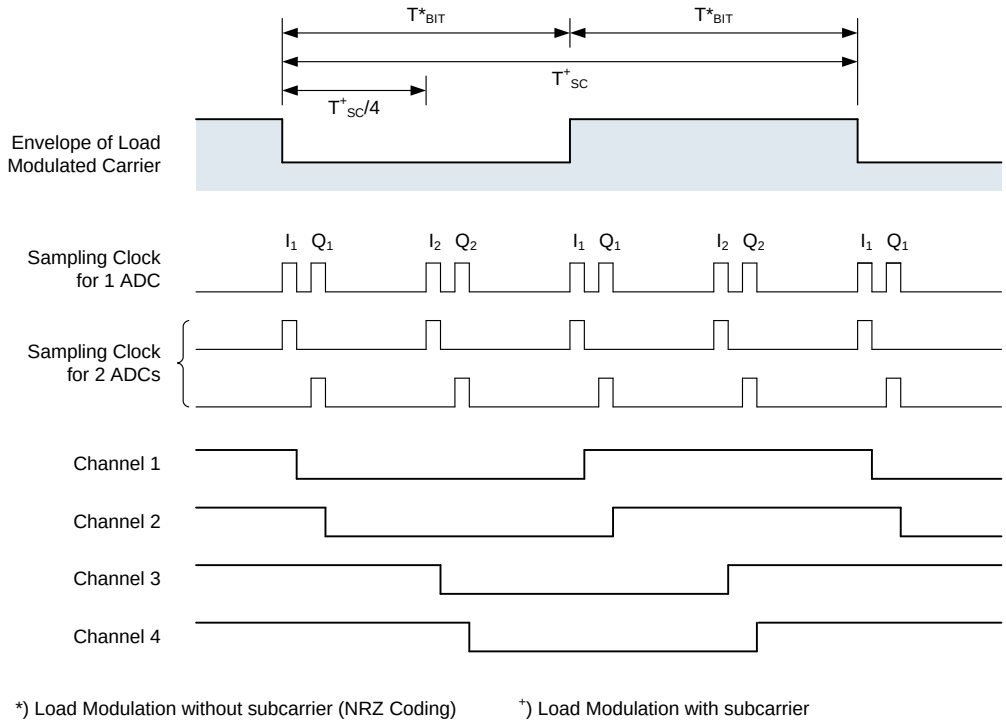


Figure 5.40: Clocking schemes for two different downsampling approaches

Both, the clocking scheme for the subcarrier as well as the NRZ based load modulation are de-

picted in figure 5.40. For 6.78 Mbit/sec one subcarrier period equates one symbol (one bit). If instead of the subcarrier signal only the NRZ coded signal is used for the load modulation, one carrier period equates one symbol (one bit). Therefore, one symbol (one bit) at the subcarrier based load modulation equates two symbols (two bits) at the NRZ based load modulation. Table 5.1 lists the required sampling frequencies for the subcarrier as well as for the NRZ based uplink communication. A detailed explanation of the algorithm for further signal post processing (after the down-conversion) is given in section 6.5.2.

	Method 1 (Subcarrier)			Method 2 (NRZ)
Data Rate	D_{SC}	f_{SC}	$f_{Sampling}$	$f_{Sampling}$
kbit/sec	-	kHz	kHz	kHz
848	16	848	3400	1700
1700	8	1700	6800	3400
3400	4	3400	13560	6800
6800	2	6800	27120	13560
13560	-	-	-	27120

Table 5.1: Comparison of the subcarrier and the NRZ based uplink communication (rounded values) in regard to required sampling frequencies (2 ADC approach)

5.6 Summary of Transceiver Concepts

The previous chapter gave a detailed overview and description of applicable transceiver architectures in contactless proximity reader systems. In addition, a comparison of the current research status concerning VHBR transceivers for contactless proximity applications was given. The focus of this thesis lies on the digital design of a receiving unit. The previous chapter introduces the usage of undersampling (intentional aliasing) in contactless prototyping reader systems and therefore, the implemented digital demodulation method, especially the down-conversion is based on undersampling to provide a simple and energy-efficient receiving method. Instead of a high sampling rate, an undersampling of the load-modulated carrier signal is carried out. This sophisticated technique uses a sampling frequency which is lower than the Nyquist frequency of the incoming RF signal and the method offers several advantages:

- The hardware concept of the proposed demodulator (especially the analog front end) is independent of the subcarrier frequency and the modulation scheme. This offers a great advantage compared with other demodulator concepts.
- The proposed solution requires no analog filter. In an analog demodulator design the filter must be adapted to the used subcarrier frequency
- Digital filters are not necessary either. A digital filter requires a higher sampling rate, i.e. needs a higher sample rate of the analogue-to-digital converter.

- No need for an analog mixer: This task is fulfilled by ADC sampling.
- By means of the adaptive sampling scheme, the demodulator already outputs the baseband modulated subcarrier.
- The undersampling technique implicates a low complexity of the digital logic. A high number of sampling points are already rejected at the ADC, consequently, the digital part does not have to process such a great amount of data.

6 Concept and Design of an FPGA-based Prototyping Reader System

This chapter gives a detailed description of the concept and design of the implemented contactless reader hardware architecture. First of all, a short overview of the *Field Programmable Gate Array* (FPGA) based prototyping system is given, which is used for the contactless reader system. The reader consists of several hardware components and *Intellectual Property* (IP) modules which are also described within this chapter. A detailed explanation of the receive path with the implemented demodulator and the elaborated algorithm for the demodulation process will also be given.

6.1 FPGA-Based DSP Development Board

A substantial part of the contactless reader is realized by an FPGA prototyping system, which can be seen in the respective block diagram in figure 6.1 [76]. The Altera Stratix II EP2S60 development board provides a hardware platform for high-performance *Digital Signal Processing* (DSP) designs. Figure 6.2 shows a top view of the board components and the interfaces [2].

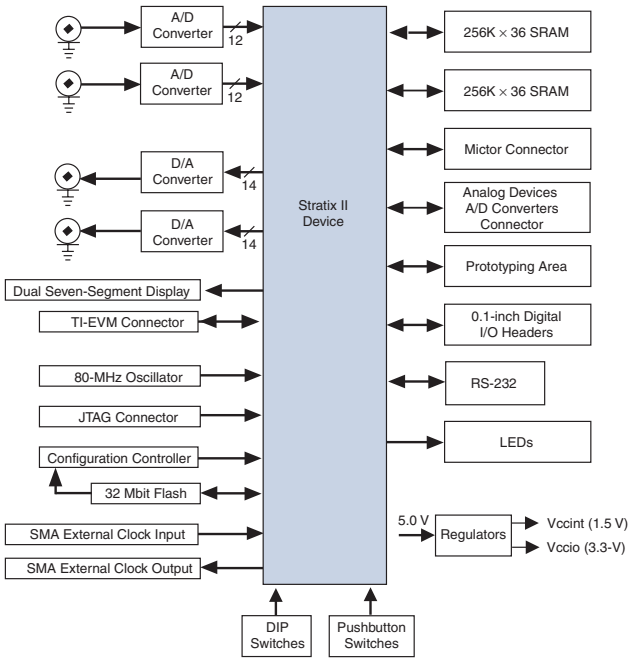


Figure 6.1: Block diagram of the Stratix II EP2S60 development board [2]

Main Components of the Altera - Stratix II EP2S60 DSP Development Board [2]:

- Analog I/O:
  - Two 12-bit 125-MHz A/D converters
  - Two 14-bit 165-MHz D/A converters
- Memory subsystem:
  - 1 MByte of 10-ns asynchronous SRAM configured as a 32-bit bus
  - 16 MBytes of flash memory configured as a 8-bit bus
  - 32 MBytes of SDRAM memory configured as a 64-bit bus
- 10/100 Ethernet MAC/PHY
- Socketed 100-MHz oscillator

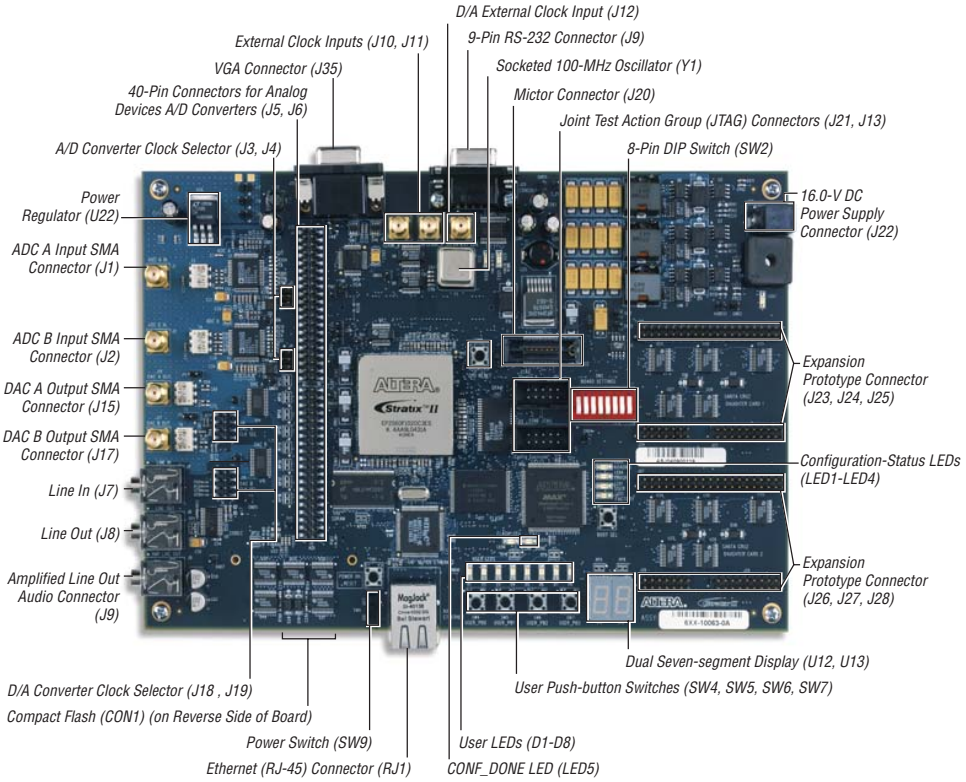


Figure 6.2: Stratix II DSP Development Board Components & Interfaces [2]

6.2 Reader Architecture

The reader system is based on a *Software Defined Radio* (SDR) concept and, therefore, ensures a high level of flexibility regarding the implementation of different modulation and encoding methods. The main advantage of such an SDR system is the nature of signal processing, which can

be carried out almost entirely in the digital domain. A differentiation is drawn between an ideal and an implementable software defined radio system: In an ideal SDR system, the analog/digital and digital/analog converter are placed directly behind the antenna (see figure 6.3) [13]. In addition, those components are directly connected to the FPGA or DSP. However, implementable SDR systems (see figure 6.4) like satellite receivers or mobile phones use analog up/down mixing stages for the down-conversion to an intermediate frequency. Because of the limitation of the ADC/DAC sampling frequency, the usage of an ideal SDR scheme is possible up to a certain frequency [58]. The architecture of the implemented contactless proximity reader system (figures 6.5 and 6.6) is equivalent to an ideal SDR system and consists of the following main components:

- Microcontroller (Nios®II Softcore Controller)
- Interface Modules to the Host/Terminal (JTAG, RS232 and Ethernet)
- Digital Hardware Modules (Send- and Receive-Path)
- Additional Analog Hardware Components (power amplifier, matching circuit and special antenna arrangements)

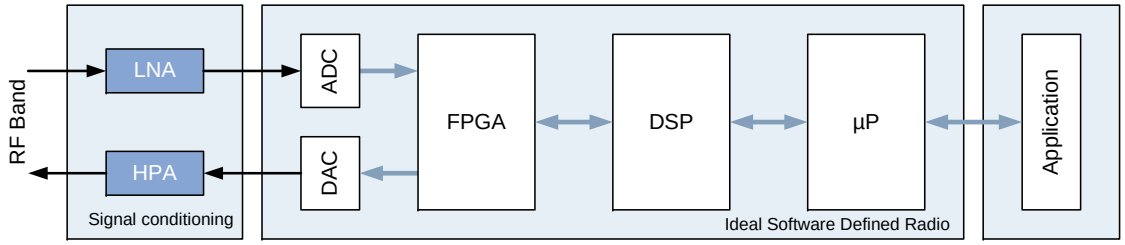


Figure 6.3: Block diagram of an ideal SDR System

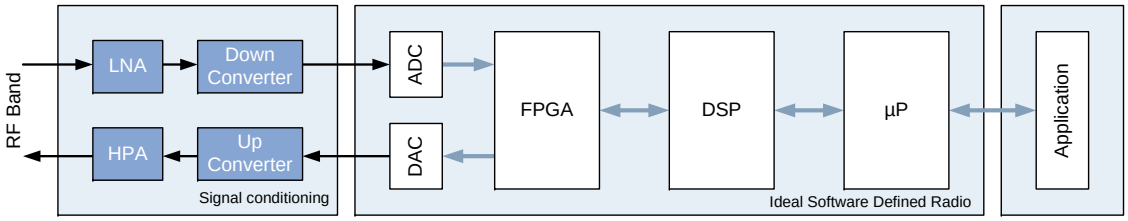


Figure 6.4: Block diagram of an implementable SDR System

A detailed VHDL system overview (top level module, CPU I/O module, transmit module and receive module) with all signal lines and signal names is given in the Appendix A. The Appendix A also includes a schematic of all pins within the FPGA design.
Altera offers a large selection of *Intellectual Property* (IP) cores. Some of them are used in the present reader system, for example the interfaces to the terminal or the microcontroller. The configuration of the FPGA and the programming of the micro controller occur via USB/JTAG interface. The JTAG interface is used for debug reasons (hardware and firmware) and for the recording of

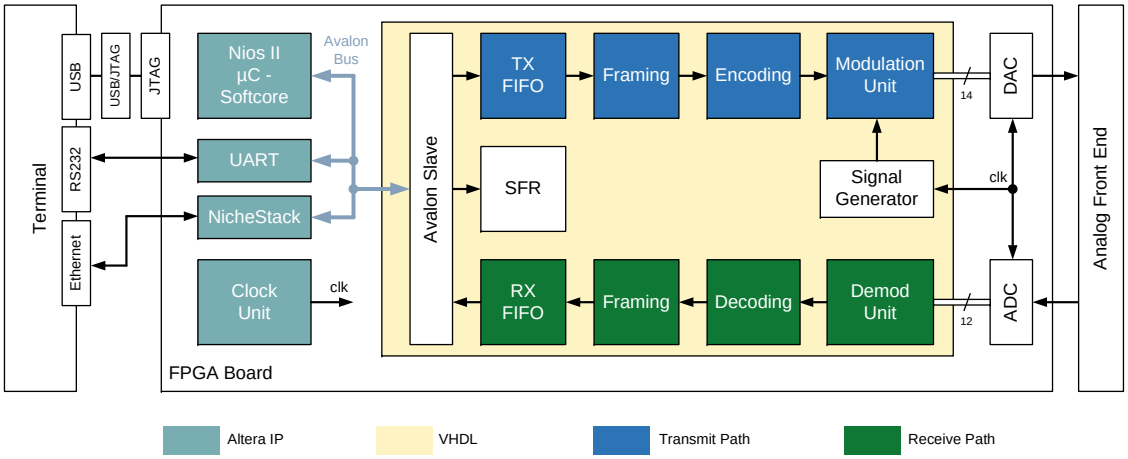


Figure 6.5: Block diagram of the implemented contactless reader

measuring signals. Measurements can therefore be carried out directly in the laboratory and the resulting measuring vectors are added to the simulations as real stimuli-data. The actual data transfer between terminal and reader is carried out by an RS232 connection on the one hand and an Ethernet connection on the other. The digital hardware modules for the sending and receiving path have been designed to enable a maximum degree of freedom regarding framing, coding and modulation. In the following, a short description of the implemented IP modules and the transmit path will be given. In addition, the receive (RX) path will be discussed in detail [9].

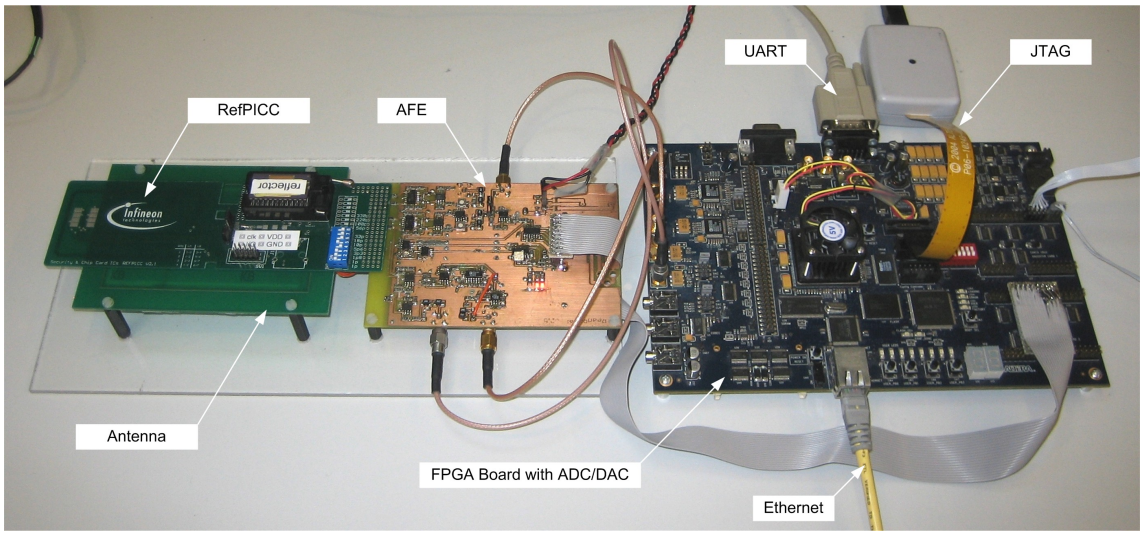


Figure 6.6: Implemented contactless prototyping reader system

6.3 Hardware Components and IP Modules

This section gives a short description of Altera IP cores, which are used in the present reader system.

Nios®II Microcontroller

The synthesized microcontroller Nios® II is a softcore module, which means that the controller is completely described in a *Hardware Description Language* (HDL). After synthesis the FPGA can be configured with the microcontroller. The firmware is written in the programming language C and is basically responsible for protocol-handling and data communication between host/terminal and the digital hardware modules. A detailed specification of the softcore controller can be found in the data sheet [3]. The configuration and interaction with the corresponding hardware modules are carried out by the *Special Function Registers*(SFR).

UART

The *Universal Asynchronous Receiver Transmitter* (UART, RS232) link offers an opportunity to connect the reader system to a terminal/host. Communication performance is limited to maximum 115.2 kbit/sec. The operation of the reader device is based on a textual console which runs in the microcontroller.

Niche Stack

A second method to connect the contactless reader to a terminal/host is the usage of an Ethernet link. The Niche Stack is an entire TCP/IP stack which is used for the transmission/reception of *User Datagram Protocol* (UDP) packets. For the physical connection to the network a 10/100 Ethernet *Media Access Controller* (MAC) core is on board.

Clock Unit

The clock unit is responsible for the clock distribution throughout the entire system. The FPGA development board obtains the clock source from the on-board crystal oscillator (100 MHz). Two *Phase Looked Loops* (PLL) are used which provide a 108.48 MHz (8·13.56 MHz) clock signal for the DAC and a 13.56 MHz clock signal for the microcontroller and the remaining digital logic modules. Reduced clock frequencies for the subcarrier, the various symbol frequencies and the ADC are generated by counter and divider. Figure 6.7 shows the clock distribution and the associated clock frequencies within the receive path.

Avalon Bus System

The Avalon IP is a bus system which is used for the connection of the microcontroller and the digital hardware modules. All IP modules from Altera are provided with an Avalon slave module.

Analog-to-Digital Converter

The Altera Stratix II development board has two A/D converters (AD9433) from Analog Devices. The pipeline converter uses a switched capacitor architecture with a maximum sampling rate of 125 MSPS and the input voltage range lies between $\pm 1V$. The representation of the output data is selected for a 12 bit two's complement coding. Further information can be found in the datasheet [1] [20].

Digital-to-Analog Converter

The Altera Stratix II development board has two D/A converters (DAC904) from Texas Instruments. The output of the converter consists of a current source with a maximum value of 20mA. The converter supports update rates of 165 MSPS and offering a 14 bit resolution (unsigned integer format). Further information can be found in the datasheet [2] [39].

6.4 Architecture of the Transmit Path

The concept and digital design of the transmit path was easily developed and not the main focus of the present work. For this reason, no detailed description of the transmission path takes place. The framing and encoder module in the TX path offers a high flexibility to investigate different frame structures and encoding methods. In the first step the baseband data is wrapped into a standardized frame format which includes additional information like *Start of Frame* (SOF), *End of Frame* (EOF), CRC or parity bits. Depending on the encoding and modulation method, the encoder generates an In-Phase and Quadrature-Phase signal and those signals are fed into the I/Q modulator (see section 5.4). This modulator enables a very high flexibility concerning different modulation techniques. The following methods are possible: MASK, MPSK and QAM. For the generation of the carrier signal (13.56 MHz) a *Lookup Table* (LUT) is used, in which the signals are described by discrete values. Eight samples per period are used and, therefore, the *Digital-to-Analogue Converter*(DAC) operates with a sampling rate of 8·13.56 MHz=108.48 MHz. In a conventional reader system, the generation and modulation of the carrier are done in the analog domain. In the new reader concept, these tasks are completely done in the digital domain, which offers a high flexibility concerning exploration and investigation of VHDR.

6.5 Architecture of the Receive Path

This section describes the architecture of the receive path (see figure 6.7) which consists the analog front end, the analog-to-digital converter and the implemented digital logic. Especially the architecture of the implemented digital demodulator, the associated algorithm for signal processing and the implemented adaptive control will be discussed in detail. However, a short overview of the remaining modules and components are given before.

[1] AD9433, 12-Bit, 105MSPS/125MPSP, IF Sampling ADC, Analog Devices
[2] DAC904, 14-Bit, 165MPSP, Digital-to-Analog Converter, Texas Instruments

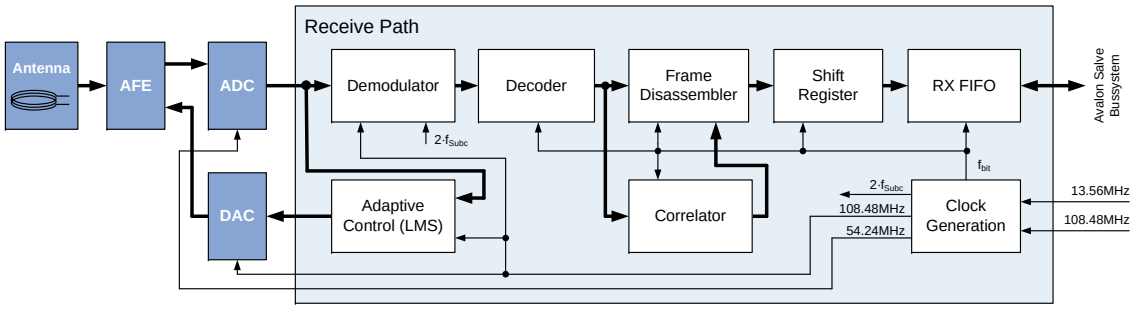


Figure 6.7: Receiver architecture

Analog Front End for the Receive Path

Figure 6.8 shows the essential components of the analog front end which are required for data reception. In Matthias Emsenhuber's diploma thesis [23], the physical interface of the reader was dealt with and new analog receiver concepts were investigated. Furthermore, the analog front end with the sending and receiving circuits was realized in hardware (*Printed Circuit Board*, PCB). As already described in section 3.3.2 an improved antenna concept for VHDR with two separate antennas (transmit and receive) is used. The first block after the antenna (see figure 6.8) is responsible for the conversion from differential signalling to a single-ended signal. The receive path must be disabled with the $RX/\overline{TX}$ signal if the reader is in the transmission state. The next block is used for carrier cancellation which is realized by an adaptive control. Therefore, the received signal is subtracted from a desired generated signal. In section 6.6 a detailed explanation of the implemented algorithm is given. The amplitude level of the received signal varies in accordance with the distance between the reader and transponder antenna. For the optimal saturation degree of the ADC, an *Automatic Gain Control* (AGC) is used. This method will also be discussed within this chapter. However, the amplitude level of the ADC input signal must be bounded by a limiter and the unwanted frequencies are removed by a lowpass filter (anti-aliasing filter).

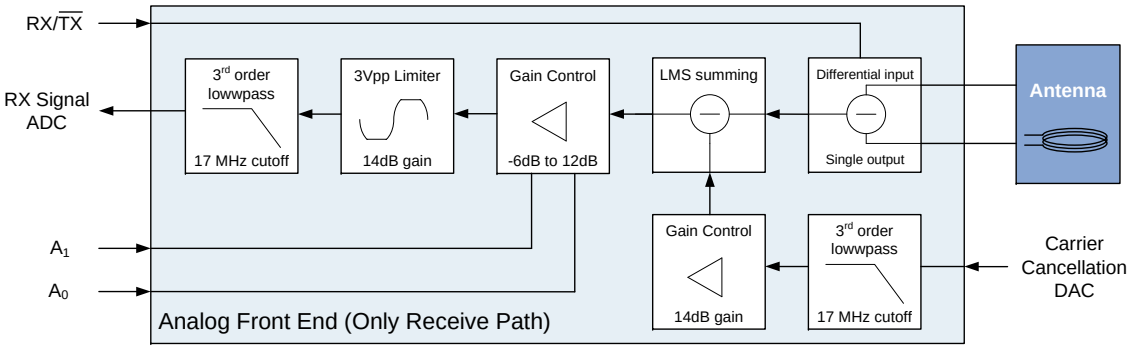


Figure 6.8: Analog front end (only receive path)

Clock Distribution

In figure 6.7 the clock distribution of the receive path is depicted. As mentioned before, an on-board crystal oscillator (100MHz), two on-board PLLs and a digital clock module (counter/divider) are used for the generation of different clock frequencies. The ADC, DAC, adaptive control and the digital demodulator require the higher clock frequencies of 54.24 MHz and 108.48 MHz. The remaining digital logic for binary signal processing needs the double subcarrier frequency and the bit clock.

Binary Data Processing

For the binary data processing the following modules are responsible: decoder, frame disassembler, correlator, shift register and RX FIFO. Detailed information concerning the functionality of each module can be found in the diploma thesis of Matthias Pichler [79].

6.5.1 Architecture of the Implemented Demodulator

Figure 6.9 shows a detailed block diagram of the digital demodulator which was completely implemented in the FPGA. The functionality of the downsampling unit was discussed in section 5.5.4.5. The four output channels CH1-CH4 of this unit provide the already downsampled waveforms (I_1, Q_1, I_2, Q_2) which are depicted in figure 5.37. The downsampling unit accomplishes a conversion down to the subcarrier frequency if a subcarrier based uplink-communication is applied as well as to the baseband if the carrier was directly load-modulated by the NRZ coded baseband data. But both transmission concepts require a further decimation step with an according signal post processing. Each signal is represented by a 12 bit (signed) number format. Due do the downsampling technique, every channel has its own DC offset. In addition, the signal quality against each other differs and depends on the corresponding sampling scheme, i.e. where the sampling takes place at the carrier signal. The main task of the demodulator is the demodulation and post processing of the four channels and the generation of a serial bit stream. In the following chapter, the architecture as well as the functionality/algorithm of the implemented demodulator will be discussed and explained in detail.

6.5.2 Implemented Algorithm for the Demodulation Process

As already mentioned, the entire signal processing is done in the digital domain, i.e. the undersampling process for the down-conversion and the algorithms for further signal processing are all implemented in VHDL. However, before the VHDL implementations are accomplished, the methods and algorithms are implemented and verified in Matlab. Most of the waveforms within this thesis result from Matlab simulations and measurements which where taken in the laboratory. The input and stimuli vectors for the Matlab simulations are measured directly by the ADC in the real contactless prototyping reader system. The FPGA based prototyping system and the associated development software offers the possibility to take these test vectors while the digital hardware design is running so that the answer of a transponder (load-modulated carrier signal) can be measured and used for the simulation. This measured signal waveform was used as stimuli input for the developed demodulation method algorithm/algorithm. The standardized communication sequence between reader and transponder was shown in figure 4.11 (Section 4.3). Figure 6.10 shows the uplink sequence again, but with additional information on timings for the demodulation

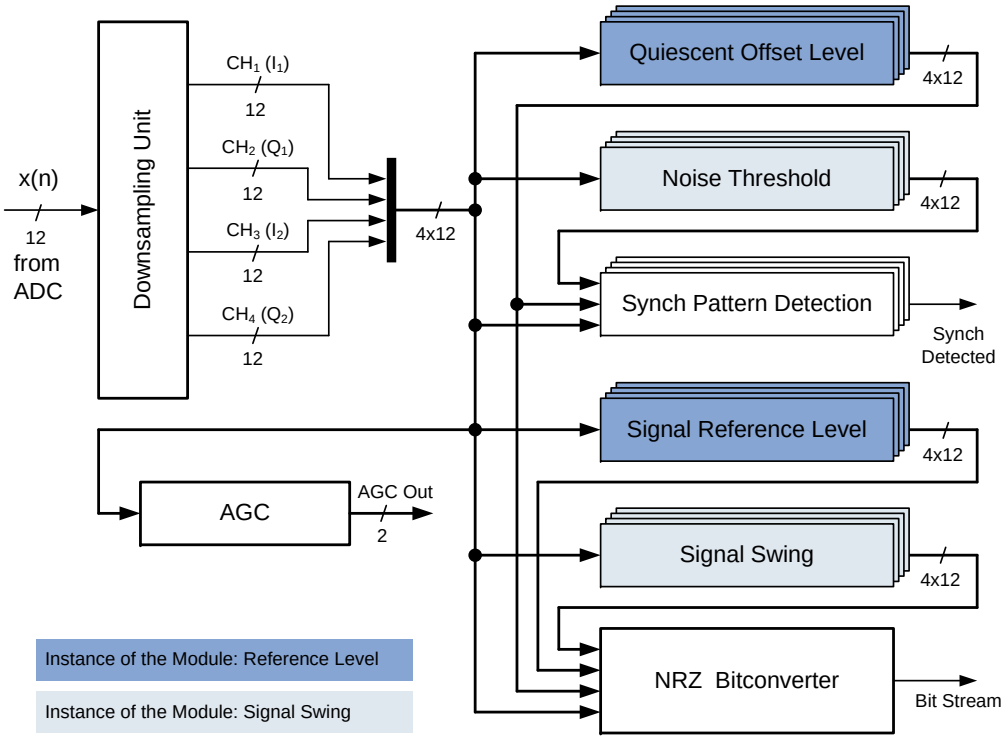


Figure 6.9: Signal path of the implemented demodulator unit

process. For a better understanding of the demodulation procedure, the respective tasks are depicted in the flow chart 6.11. After the end of the downlink communication and the expiration of a predefined time period t_{DEAF} the automatic gain control will be activated. During the time period t_{DEAF} the receiver path and consequently the demodulator unit are inactive. If the PICC must process computationally intensive tasks like fast cryptographic calculations, an unwanted form of load modulation may appear which is also called *Electro-Magnetic Disturbance* (EMD) [80]. If the receiver is not inactive during the time t_{DEAF}, the EMD could be misinterpreted as a real load modulation, which will lead to a breakdown in communication.

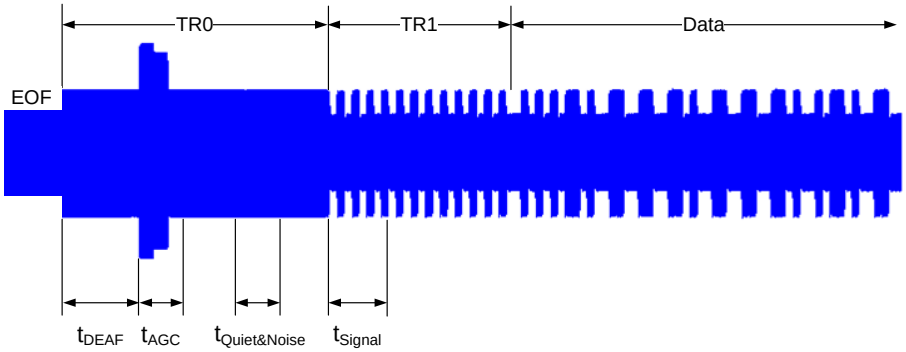


Figure 6.10: Receive sequence with timing information for the demodulation process

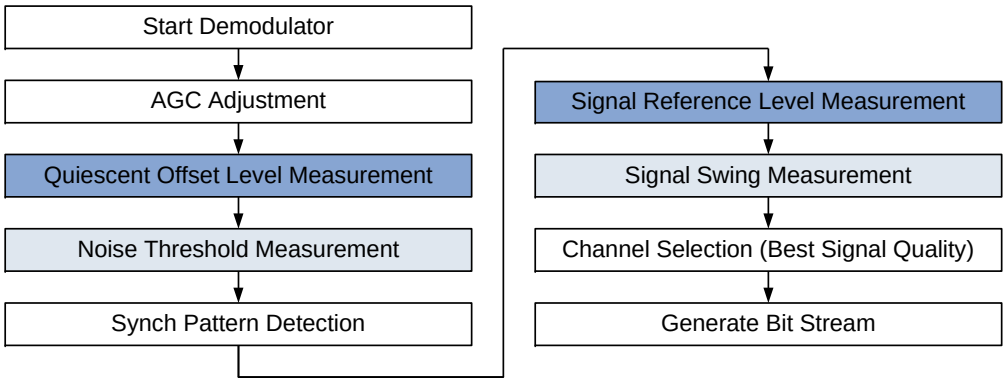


Figure 6.11: Flow chart for signal processing

Automatic Gain Control

For the optimal saturation degree of the ADC, an *Automatic Gain Control* (AGC) was deployed and the digital control mechanism was implemented in the FPGA. The AGC only enables an attenuation of the received signal and supports the following four gain steps: 1/8, 1/4, 1/2 and 1. The amplitude level of the received signal varies in accordance with the distance between the reader and transponder antenna. The smaller the distance, the higher the amplitude level of the received signal. This is why the AGC always starts with the gain factor 1. A digital peak value detector determines the maximum received value and the AGC unit compares this value with a predefined threshold value. Then, a stepwise (max. 3 steps) attenuation of the received signal takes place if the determined amplitude is still too high. Figure 6.12 shows the improvement of the signal quality if an AGC is used. Detailed measurement results of the AGC can be found in section 7.4.4.

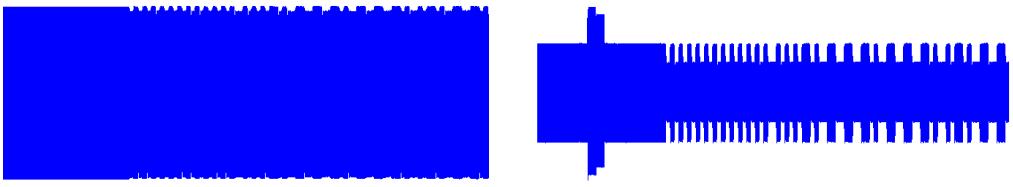


Figure 6.12: Received signal without and with AGC

Quiescent Offset Level

Each channel has its own *Direct Current* (DC) offset caused by the downsampling of the carrier signal. This offset is not eliminated but a quiescent level is calculated for every channel by means

of the *Reference Level* module. Therefore, an average determination over N sampling points is carried out for each channel (ch_1 *to* ch_4):

$$QRL(ch_x) = \left\lfloor \frac{1}{N} \cdot \sum_{k=1}^{N} ch_x(k) \right\rfloor \tag{6.1}$$

Figure 6.13 shows the ADC output signal (unsigned 12 Bit format), the four output signals of the downsampling unit, the measured quiescent sampling points (diamonds) and their quiescent offset levels (solid lines). In addition, the noise threshold for every channel is also depicted. This will be discussed in the following (dashed line).

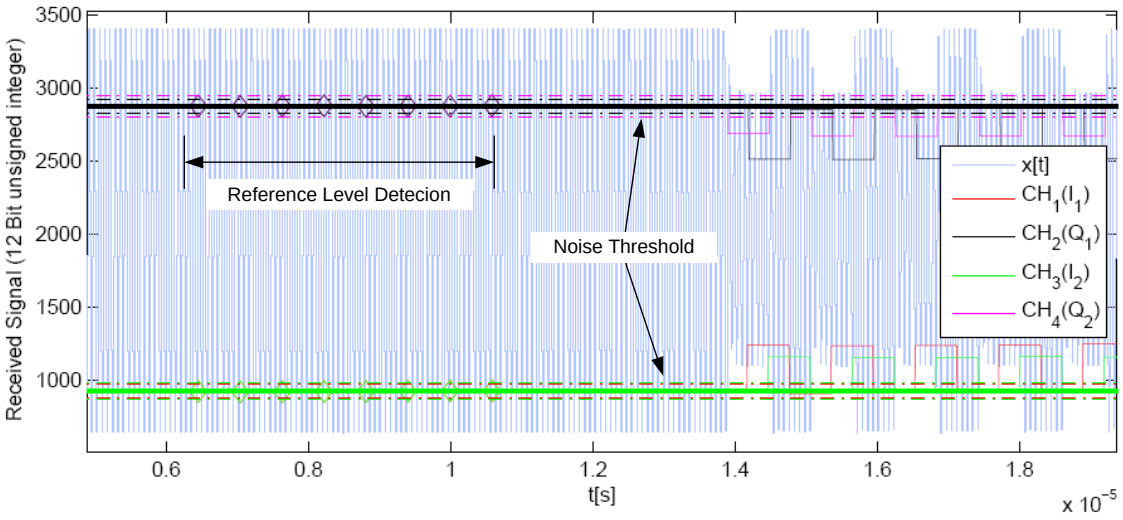


Figure 6.13: Quiescent Offset Level and Noise Threshold

Noise Threshold

During the determination of the quiescent reference level the noise threshold is also measured. Within the time period $t_{Quiet\&Noise}$, both, the maximum as well as the minimum sampling value are determined for every channel, and the difference is calculated by the module *Signal Swing*. In addition, the calculated difference is multiplied by an adjustable factor. The noise threshold is essential for the correct recognition of the synchronization pattern. This way, a faulty detection of a synchronization pattern caused by channel disturbances can be excluded. In figure 6.13 the corresponding noise thresholds are also depicted (chain-dotted line).

Synchronization

Before the description of the actually implemented synchronization method, a short definition of the term *Synchronization* is given. Synchronization can be seen as optimization problem which can be solved by an object cost function. For this, the minimum Euclidean distance or the maximum correlation peak between the received and the test signal will be determined. There are two different synchronization techniques. The first one is the *Acquisition* (initialization), which

will be executed each time before the uplink communication starts. During the complete uplink communication sequence the determined parameters for the signal processing remain constant. The second synchronization method is *Tracking* (controlling). As the name suggests, a permanent tracking/controlling of the parameters during the whole communication sequence is carried out [58]. Several RFID demodulation architectures based on the principle of correlation have been published. D. Kusternigg [60] (this work was already mentioned in section 5.3) presents a correlation algorithm for the synchronization of the internal sampling clock to the received subcarrier signal. Thereby the received signal is compared with an already known signal pattern (in that case the subcarrier waveform) for readjustment of the sampling-clock. The contactless proximity demonstration reader with the implemented correlation technique supports very high data rates, but only data rates up to 6.8 Mbit/sec. The correlation method can not handle data rates of 13.56 Mbit/sec. Y. Liu and C. Huang et al. [36], [65] present a correlation based demodulation design for UHF RFID applications. In UHF systems the tag has no reference clock and hence, the data rate of the backscattered response is continuously variable with a maximum frequency deviation of $\pm 22\%$. The synchronization and estimation of the input data frequency was realized by correlator banks. These banks comprise 12 correlators, which represents an enormous hardware effort. Ch. Angerer et al. [7] present a novel synchronization and decoding structure for UHF RFID reader receivers. The implemented algorithm is based on correlation with the main objective to optimize the hardware resource consumption.

As mentioned in a previous chapter, the start point of the PICC response is not defined. Therefore, a synchronization between carrier signal and sampling does not take place. The undersampling method is based on a *non-coherent* demodulation, i.e. the beginning of the carrier can vary and, consequently, the sampling points are not in phase to the carrier frequency. The synchronization topic discussed within this section relates to the synchronization of the data which is modulated upon the carrier signal. For a subcarrier based uplink communication an unmodulated subcarrier is used as synchronization (Synch) pattern. At the NRZ based uplink communication no dedicated subcarrier is used, but the synchronization pattern equates to an unmodulated subcarrier. Thereby the 'subcarrier frequency' corresponds to half of the bit rate. The implemented digital demodulator within the prototyping reader system requires no correlation. Instead of that, the four channels provided by the undersampling unit are used to obtain the correct baseband data. Figure 6.14 shows the method for the detection of the synchronization pattern for each channel. If the noise threshold (chain dotted line) is exceeded eight times in a row, it is assumed that the synchronization sequence has started. This is equivalent to four consecutive subcarrier periods. This way a faulty detection of a synchronization pattern caused by channel disturbances could be excluded. The exceeding of the noise thresholds is depicted by diamonds. The next step is the calculation of the *Signal Reference Level* for each channel.

Signal Reference Level and Signal Swing

After the synchronization sequence has been detected, a new *Signal Reference Level* is required as signal threshold for further signal processing. Figure 6.14 shows the sampling points (diamonds) which are used for the calculation of the *Signal Reference Level* (bold lines), whereas the first sampling point is not used. The upper graph of figure 6.15 shows an enlarged representation of one channel ($CH_2(Q_1)$) and the associated *Signal Swing*.

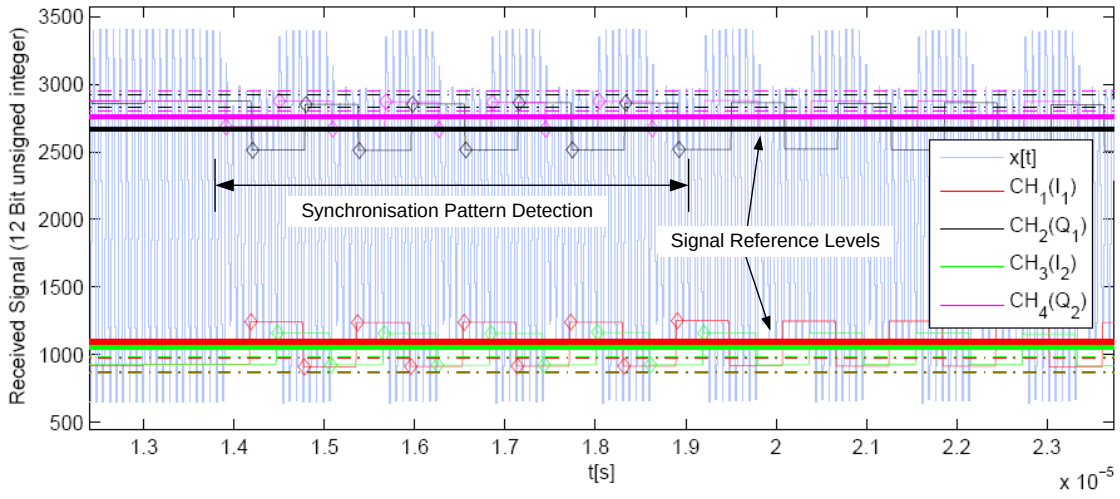


Figure 6.14: Detection of the synchronization sequence

Channel Selection and Signal Detection

As assessment criterion for the final channel selection, two quantities are used (see upper graph of figure 6.15). The first one is the *Signal Swing* (1) and the second one is the *Deviation* (2) of the signal reference level and the quiescent offset level. The channel with the greatest value of signal swing (1) and signal deviation (2) will be finally selected. This channel provides the best signal quality. The final process is the digitization of the selected signal. For this a comparator is used to compare the selected signal with the adequate signal reference level. The resulting bit stream is depicted in the lower graph of figure 6.15.

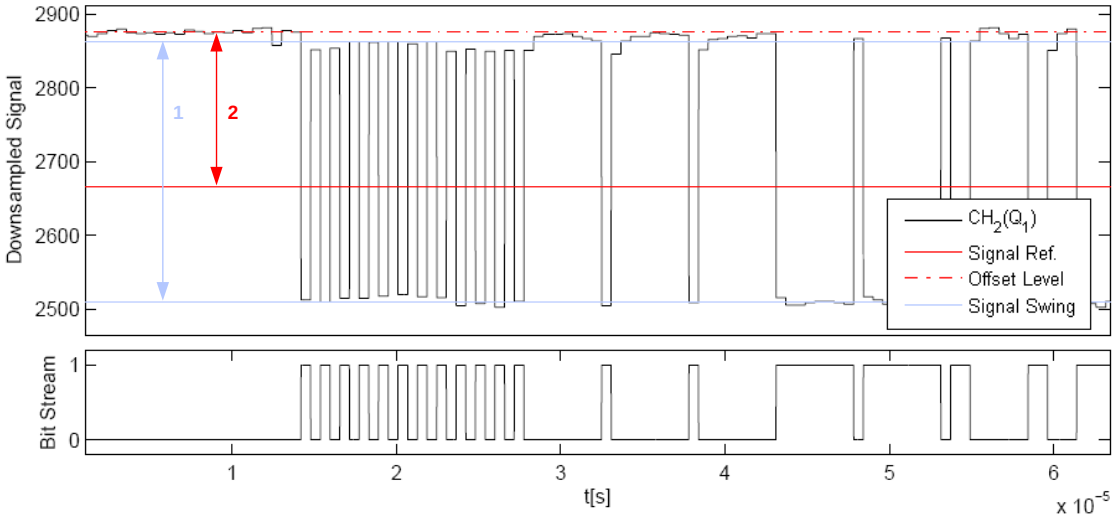


Figure 6.15:
Channel Selection Criteria: 1.) Signal swing, 2.) Signal deviation
Resulting Bit Stream

6.6 Adaptive Control for Carrier Cancellation

There are several concepts and solutions to optimize the communication performance of the air interface, especially the signal quality of the received antenna signal. Chapter 3.3.2 shows the implemented solution within the prototyping reader system for an optimized communication performance. This method is based on the antenna arrangement with two separated coils (transmit and receive) which eliminates the influence of the resonant circuit. Another reason of the low signal quality of the received signal is the loose coupling between the transponder antenna and the reader antenna. Thereby, the detected signal on the reader side is significantly smaller than the carrier signal. The ratio of the carrier signal to the received signal (load modulation amplitude) amounts to 80 dB. To optimize the signal quality of the received signal, a carrier cancellation is deployed. Especially to RFID systems which operate at a low *Load Modulation Amplitude* (LMA), this cancellation technique is very advantageous, e.g. the uplink at the *Phase Jitter Modulation* (PJM) [45], [90] is based on very low load modulation amplitudes. In comparison to proximity coupling systems the LMA is significantly smaller by a factor of up to 10. The carrier cancellation is carried out by an adaptive filter technique. This technique is characterized by the fact that the transfer function can be modified during the operation and the adaptation of the filter coefficients is done by an adaptation algorithm. Adaptive filters are used for echo cancellation, noise suppression or channel equalization. The channel equalization requires a training process which uses a training sequence at the beginning of each communication. The receiver knows this training sequence and by which it accomplishes the adaptation of the filter coefficients. Because of the dynamical behavior of the prototyping reader system, which depends on the distance between reader and transponder, an adaptive filter is the right technique for the mentioned problem. Figure 6.16 shows the block diagram of an adaptive filter. The description of the LMS algorithm is given in the next section.

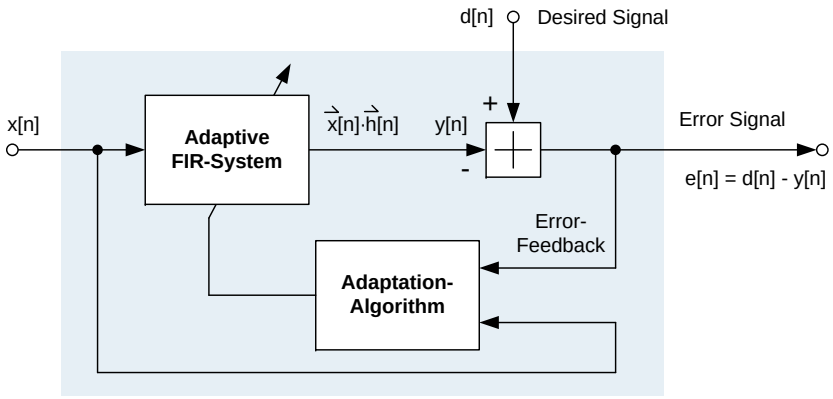


Figure 6.16: Architecture of an adaptive filter [94]

General Description of the LMS-Algorithm:

The input signal $x[n]$ is modified by the adaptive *Finite Impulse Response* (FIR) filter system and provides the estimated signal $y[n]$ (see block diagram 6.16). Thereby, a convolution of the input signal with the impulse response of the FIR filter takes place. The value $y[n]$ is compared to the desired signal $d[n]$ and the result is the error signal $e[n] = d[n] - y[n]$. The LMS adaptation algorithm tries to minimize the error signal by adaptation of the filter coefficients $\vec{h}$.

$$
\begin{aligned}
Given: \quad & \vec{x}[n] = [x[n], x[n-1], ..., x[n-M]] \\
& \vec{h}[n] = [h_0[n], h_1[n], ..., h_M[n]]^T ; d[n]
\end{aligned}
$$

$$
\begin{aligned}
Initalization: \quad & \mu = const. \\
& \vec{h}[0] = 0
\end{aligned}
$$

$$
\begin{aligned}
Algorithm: \quad & for\ n = 0, 1, 2, 3, ... \\
& e[n] = d[n] - \vec{y}[n] = d[n] - \vec{x}[n] \cdot \vec{h}[n] \\
& \vec{h}[n+1] = \vec{h}[n] + \mu \cdot e[n] \cdot \vec{x}^T[n]
\end{aligned}
$$

$$
\begin{aligned}
Symbols: \quad & \mu : Step\ Size \\
& M : Filter\ Order \\
& e : Error\ Signal \\
& h : Filter\ Coefficients \\
& d : Desired\ Signal \\
& x : Input\ Signal
\end{aligned}
$$

The vector $\vec{x}[n]$ contains the data at the sample points $n-M$ until n, and the vector $\vec{h}[n]$ contains the coefficients of the FIR filter with the filter order M at the time n. The step time μ defines the convergence time and stability of the LMS algorithm. A small μ prolongs the convergence, but if the step size is too large, the LMS algorithm may never converge. The $\vec{h}[n+1]$ contains the new coefficients of the FIR filter which are updated after every run. This is why the old filter coefficients, the input vector, the step size and the error signal are required. Further reading on the topic of LMS algorithm can be found in [22], [33], [64], [94].

Implemented Carrier Cancellation:

The implemented carrier cancellation based on the adaptive filter technique requires an ADC, DAC and a discrete circuit for the analog subtraction of the incoming signal and the estimated signal. This is realized by an operational amplifier, placed within the *Analog Front End* (AFE) (see figures 6.7 and 6.8). The adaptive filter technique which was implemented for carrier cancellation diverts somewhat from its intended use. Figure 6.17 shows a block diagram of the implementation, the nomenclature differs from the block diagram in the previous figure 6.16.

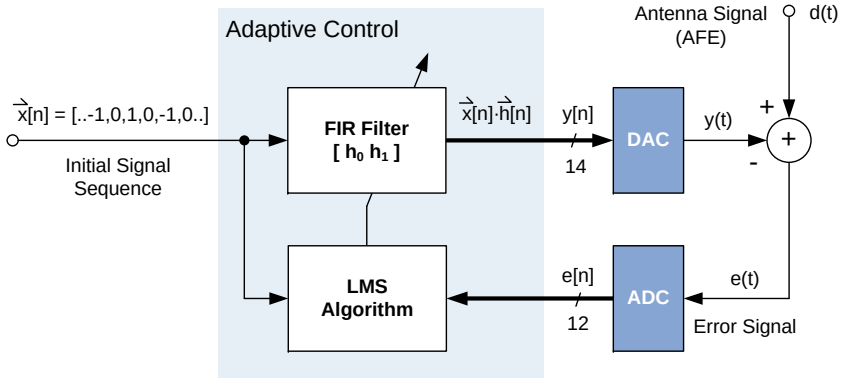


Figure 6.17: Implemented LMS algorithm for carrier cancellation

Not the incoming (received) signal is modified by the FIR (Transversal) filter system, but the internally generated signal $\vec{x}[n]$ is modified by the FIR filter and receives the same signal characteristic — amplitude as well as phase — as the incoming signal $d(t)$. Thereby a convolution of the signal $x[n]$ with the impulse response of the first order FIR filter (two tap, see figure 6.18) takes place.

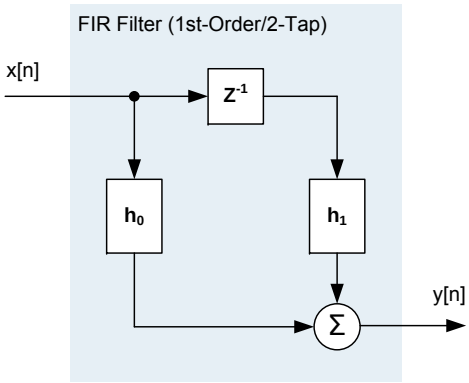


Figure 6.18: Block diagram of the FIR filter (1st-Order/2-Tap)

The value $y(t)$ is compared to the incoming signal $d(t)$ and the result is the error signal $e(t) =$

$d(t) - y(t)$ (after digitalization $e[n] = d[n] - y[n]$). For the adaptation of the filter coefficients a *Least Mean Square* (LMS) algorithm is used which tries to minimize the error signal. This algorithm uses an optimization criterion which is based on the least mean squares of the error signal for finding the right filter coefficients [22], [33], [64], [94].

Modified and Implemented LMS-Algorithm:

The algorithm was implemented in VHDL and works with a clock frequency of $4 \cdot f_c = 54.24\,MHz$. The calculation of the current error is done in the analog domain within the analog front end. The internally generated signal $x[n]$ describes a sinusoidal signal with four sample points per period which are the maximum and minimum points and two zero points:

$$x\left[n\right] = \left[\ldots -1\,,0\,,1\,,0\,,-1\,,0\,,1\,,0\,,\ldots\right]$$

Filter coefficients of the first order FIR filter (M=1):

$$\vec{h}\left[n\right] = \left[h_0\left[n\right],....,h_M\left[n\right]\right]^T = \left[h_0\left[n\right],h_1\left[n\right]\right]^T = \left[\begin{array}{c} h_0\left[n\right] \\ h_1\left[n\right] \end{array}\right]$$

Based on the first order filter (M=1) the internally generated signal $x[n]$ is separated into two values:

$$\vec{x}\left[n\right] = \left[x\left[n\right],....,x\left[n-M\right]\right] = \left[x\left[n\right],x\left[n-1\right]\right]$$

Convolution of the signal $x[n]$ with the impulse response of the FIR filter:

$$y[n] = \sum_{i=0}^{M=1} h_i \cdot x\left[n-i\right] = h_0 \cdot x\left[n\right] + h_1 \cdot x\left[n-1\right]$$

Explicit convolution for the four sample points of the sinusoidal signal:

$$\begin{aligned}
y[n] &= \vec{x}\left[n\right] \cdot \vec{h} = [0,-1] \left[\begin{array}{c} h_0 \\ h_1 \end{array}\right] = 0 \cdot h_1 - 1 \cdot h_2 = -h_2 \\
y[n+1] &= \vec{x}\left[n+1\right] \cdot \vec{h} = [1,0] \left[\begin{array}{c} h_0 \\ h_1 \end{array}\right] = 1 \cdot h_1 + 0 \cdot h_2 = h_1 \\
y[n+2] &= \vec{x}\left[n+2\right] \cdot \vec{h} = [0,1] \left[\begin{array}{c} h_0 \\ h_1 \end{array}\right] = 0 \cdot h_1 + 1 \cdot h_2 = h_2 \\
y[n+3] &= \vec{x}\left[n+3\right] \cdot \vec{h} = [-1,0] \left[\begin{array}{c} h_0 \\ h_1 \end{array}\right] = -1 \cdot h_1 + 0 \cdot h_2 = -h_1
\end{aligned}$$

Initialization:

$$\mu = const.\ and\ \vec{h}\,[0] = 0$$

Algorithm:

$$\begin{aligned} &for\ n = 0, 1, 2, 3, ... \\ &e\,[n] = d\,[n] - \vec{y}\,[n] = d\,[n] - \vec{x}\,[n] \cdot \vec{h}\,[n] \\ &\vec{h}\,[n+1] = \vec{h}\,[n] + \mu \cdot e\,[n] \cdot \vec{x}^{T}\,[n] \end{aligned}$$

Explicit update of the filter coefficients h_0 and h_1 concerning the four sample points of the sinusoidal signal:

$$\begin{aligned} \vec{h}\,[n+1] &= \vec{h}\,[n] + \mu \cdot e\,[n] \cdot \vec{x}^{T}\,[n] \\ &= \begin{bmatrix} h_0\,[n] \\ h_1\,[n] \end{bmatrix} + \mu \cdot e\,[n] \cdot \begin{bmatrix} 0 \\ -1 \end{bmatrix} = \begin{bmatrix} h_0\,[n] \\ h_1\,[n] - \mu \cdot e\,[n] \end{bmatrix} \end{aligned}$$

$$\begin{aligned} \vec{h}\,[n+2] &= \vec{h}\,[n+1] + \mu \cdot e\,[n+1] \cdot \vec{x}^{T}\,[n+1] \\ &= \begin{bmatrix} h_0\,[n+1] \\ h_1\,[n+1] \end{bmatrix} + \mu \cdot e\,[n+1] \cdot \begin{bmatrix} 1 \\ 0 \end{bmatrix} = \begin{bmatrix} h_0\,[n+1] + \mu \cdot e\,[n+1] \\ h_1\,[n+1] \end{bmatrix} \end{aligned}$$

$$\begin{aligned} \vec{h}\,[n+3] &= \vec{h}\,[n+2] + \mu \cdot e\,[n+2] \cdot \vec{x}^{T}\,[n+2] \\ &= \begin{bmatrix} h_0\,[n+2] \\ h_1\,[n+2] \end{bmatrix} + \mu \cdot e\,[n+2] \cdot \begin{bmatrix} 0 \\ 1 \end{bmatrix} = \begin{bmatrix} h_0\,[n+2] \\ h_1\,[n+2] + \mu \cdot e\,[n+2] \end{bmatrix} \end{aligned}$$

$$\begin{aligned} \vec{h}\,[n+4] &= \vec{h}\,[n+3] + \mu \cdot e\,[n+3] \cdot \vec{x}^{T}\,[n+3] \\ &= \begin{bmatrix} h_0\,[n+3] \\ h_1\,[n+3] \end{bmatrix} + \mu \cdot e\,[n+3] \cdot \begin{bmatrix} -1 \\ 0 \end{bmatrix} = \begin{bmatrix} h_0\,[n+3] - \mu \cdot e\,[n+3] \\ h_1\,[n+3] \end{bmatrix} \end{aligned}$$

The whole LMS algorithm, which contains the convolution of the signal $x[n]$ with the filter impulse response and the update of filter coefficients h_0 and h_1, was realized in VHDL. This LMS module is not part of the demodulator unit, but of the top module. During the time period t_{DEAF} (see figure 6.10) the adaptive control is active and the LMS algorithm calculates the right filter coefficients. Afterwards, the LMS algorithm is inactive and the adaptive control still uses the

determined filter coefficients. It is assumed that for the duration of the whole transmission, the channel characteristics stay the same. Another issue is the right choice of the step size μ which was also assumed for the implemented algorithm. As far as these two are concerned, there is still potential for improvement. The associated simulation (ModelSim) and measurement results of the implemented carrier cancellation are shown in chapter 7.4.2.

7 Simulation, Verification and System Measurements

This chapter shows the verification results of the proposed and implemented contactless prototyping reader system, especially of the digital demodulation unit. Verification was done by the comparison of simulations and measurement results. These are presented in the following sections. First, however, a description of the simulation and measurement setup will be given. In addition, a method for the characterization and evaluation of the received load-modulated signal (for VHBR) which has been elaborated will be described in this chapter. This method is based on the *Modulation Error Ratio* (MER) and *Error Vector Magnitude* (EVM). It is going to be submitted as a proposal to the ISO working groups.

7.1 Simulation Setup

The algorithm for down-conversion (undersampling) as well as the algorithms for further signal processing are all implemented in VHDL. However, before the VHDL implementations are accomplished, the methods and algorithms are implemented and verified in Matlab. After the correct verification of the algorithms in Matlab, an implementation in VHDL is carried out. The digital design was done in the Infineon design environment. For the simulation of the digital design the ModelSIM® SE PLUS 6.1f simulation environment was used. The digital design includes the whole reader system with an emulated Avalon-Bus system. For simulation purpose, those components were embedded into a testbench. In addition, an analog-to-digital converter was also emulated. The design of the testbench was supported by the activities of Matthias Pichler within the scope of his diploma thesis [79] and Udo Bachernegg. The input and stimuli vectors for Matlab as well as the ModelSim simulations are measured directly with the ADC in the real contactless prototyping reader system. The FPGA-based prototyping system and the associated development software offer the possibility to take these test vectors. Therefore the tool SignalTap® was used, which is a part of the design environment Quartus® II. This measured signal waveform, especially the answer of a transponder (load-modulated carrier signal), was used as stimuli input for the developed demodulation method and the algorithm.

7.2 Measurement Setup

Figures 7.1 and 7.2 show the laboratory measurement setup and the associated block diagram. Conventional contactless chip cards only support data rates up to 848 kbit/sec (both communication directions) which are standardized in ISO/IEC 14443 [42]. However, to achieve very high bit rates (above 848 kbit/sec) for the uplink, only the *Analog Front End* (AFE) of a chip card controller was used for the load modulation. This means that the digital part of the chip controller was disabled and the generation of the digital signal for the uplink (load modulation) was done by the FPGA board. The contactless chip card controller which is embedded in a *Ceramic Dual Inline Package* (CDIP), was placed on a *Reference Proximity Integrated Circuit Card* (RefPICC). The RefPICC offers the adjustment of the resonance frequency by variation of the capacitance and the number of coil windings.

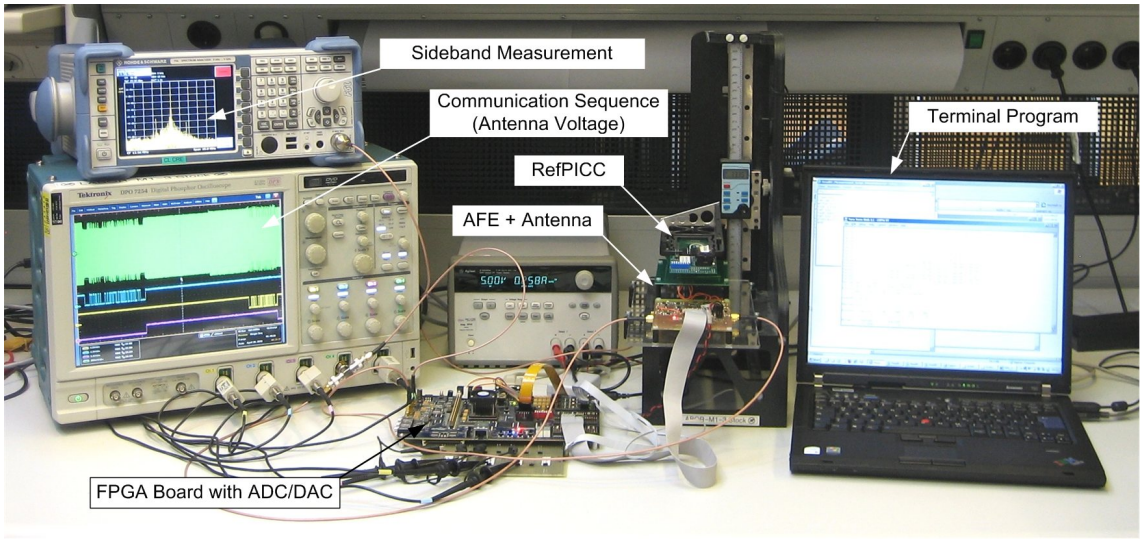


Figure 7.1: Measurement setup

The digital oscilloscope was used for the measurements in the time domain and the measurements of the sideband levels were performed by the spectrum analyzer. The communication between the terminal (PC) and the reader system was carried out by a serial RS232 connection on the one hand and by an Ethernet connection on the other. A command-line interpreter was running on the NIOS II microcontroller which was implemented on the FPGA. In case of the serial connection, a software terminal emulator (e.g. Tera Term) was used for the access to the command-line interpreter.

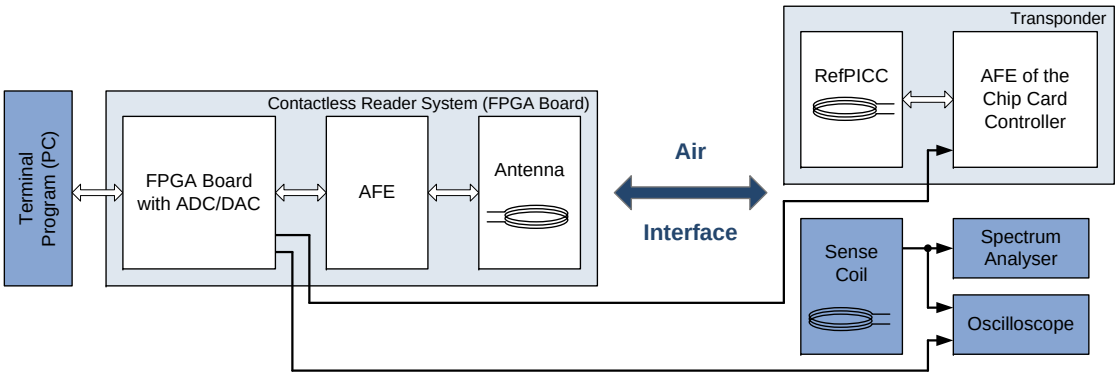


Figure 7.2: Block diagram of the measurement setup

Figure 7.3 shows an example of a console output. The communication mode was set to NRZ based load modulation, which means that no subcarrier was used for the data transmission. The data rate was adjusted to 13.56 Mbit/sec.

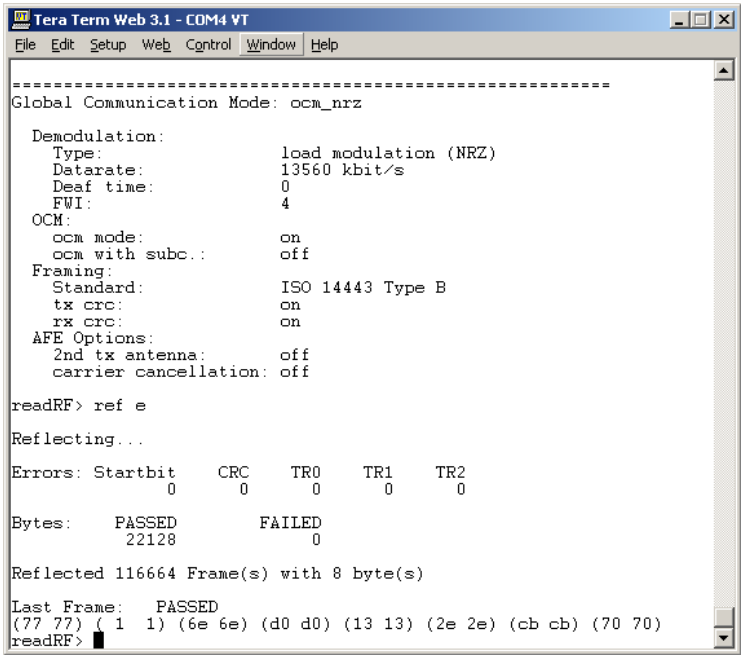


Figure 7.3: Console for the control of the reader

7.3 Measurement and Characterization Method of the Uplink

There is still no standard method to define very high bit rates in proximity systems. Thus, no characterization methods for the signal quality of the uplink concerning VHBR are standardized. The current test standard ISO/IEC 10373-6 [43] for contactless proximity cards (ISO/IEC 14443 [42]) cannot be used for this purpose, but the working groups of the ISO (participants are from Infineon, NXP, Gemalto etc.) are looking for an appropriate solution. Within this thesis a method based on the *Modulation Error Ratio* (MER) and *Error Vector Magnitude* (EVM) was elaborated, for the characterization and evaluation of the received load-modulated signal. This elaborated measurement method is intended as proposal in the ISO working groups. In the beginning of this chapter a short overview of different methods for representation and characterization of digitally modulated signals will be given [63].

7.3.1 Representation of Digitally Modulated Signals

There are various methods to represent digitally modulated signals. With the digital modulation process the bits of the baseband data are merged to data symbols. These complex symbols are displayed on the complex plain at each symbol-clock transition. This representation is also called *Constellation Diagram*.

7.3.1.1 Constellation Diagram

The number of symbols and their position within the constellation diagram depend on the respective modulation method. Figure 7.4a shows a constellation diagram of an ideal *Quadrature Phase Shift Keying* (QPSK) modulated signal. With this method four symbols are used to represent two data bits. The information is contained within the four different phase angles and not in the amplitude, because it is the same for all four data symbols.

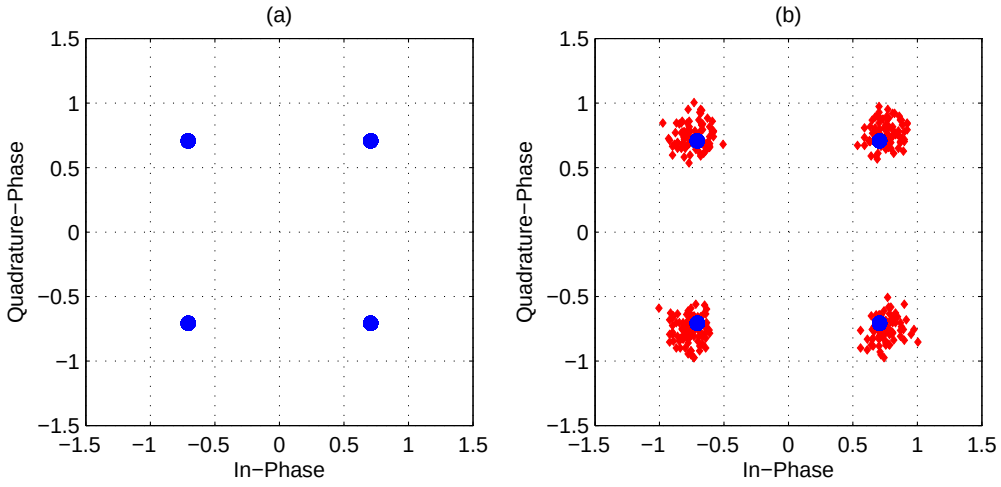


Figure 7.4: Constellation diagram: (a) ideal QPSK modulated signal, (b) RRC ($\alpha = 0.25$) filtered QPSK signal

In addition, a constellation diagram can also depict signal distortion in the form of clouds around the ideal symbol point within the complex plain. For illustration purposes the signal distortion in figure 7.4b was realized by a *Root Raised Cosine* filter (RRC) with a roll-off factor $\alpha = 0.25$. Such filters are normally used for pulse shaping in a transmitter or as matched filters in a receiver. The signal quality of a digitally modulated signal can be depicted in a constellation diagram by means of a visual representation. A method to obtain the quantitative measure of the signal quality of digitally modulated signals is shown in section 7.3.1.4 and 7.3.1.5 [63].

7.3.1.2 Vector Diagram

The constellation diagram only shows the signal state at each symbol clock. A *Vector Diagram* shows the complex symbol points and the signal trace (signal trajectory) between two symbols. Figure 7.5a shows a vector diagram of an ideal QPSK modulated signal with fast transitions from one symbol point to the other. Figure 7.5b shows a vector diagram of an RRC ($\alpha = 0.25$) filtered QPSK signal. Again, this filter was only used for illustration purposes. In the diagram the under- and overshoots next to the ideal symbol points can be seen clearly [63].

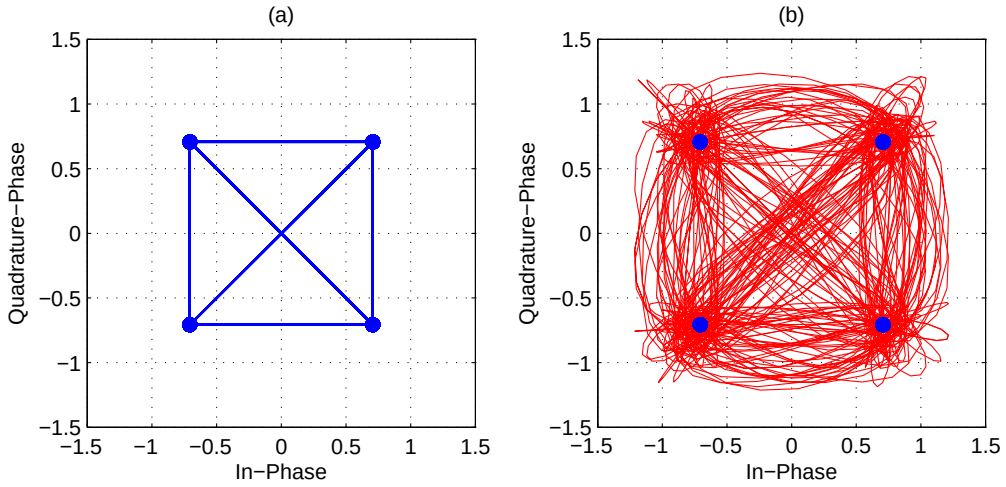


Figure 7.5: Vector diagram: (a) ideal QPSK modulated signal, (b) RRC ($\alpha = 0.25$) filtered QPSK signal

7.3.1.3 Eye Diagram

Another way to represent a digitally modulated signal is the usage of an *Eye Diagram*. For complex signals, the In-Phase- and Quadrature-Phase-Components are separated and displayed repeatedly over time. That means that this method also depicts the signal transitions from one symbol to the other. The eye diagram looks like an ”eye” by means of which many measurements can be done. The eye opening (peak-to-peak value) as well as the eye width reveal a lot about the signal quality. Figure 7.6 shows the In-Phase and Quadrature-Phase of a QPSK modulated signal which was filtered by a RRC filter ($\alpha = 0.25$) [63].

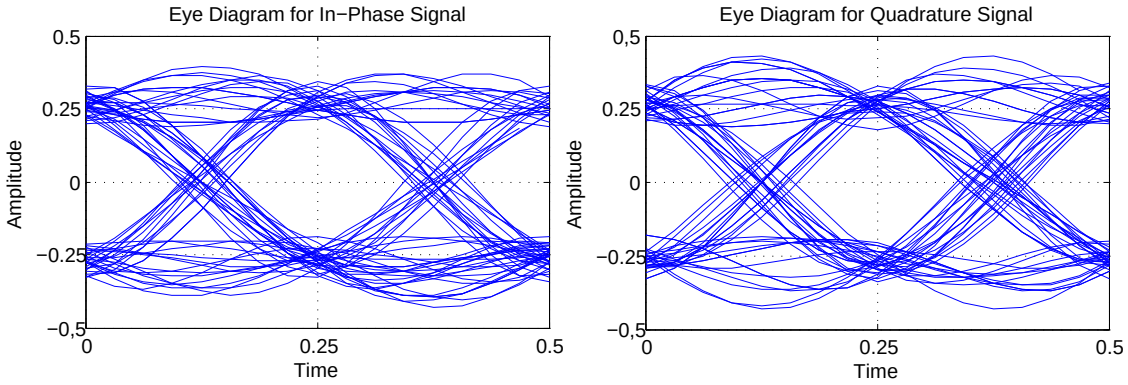


Figure 7.6: Eye Diagram of a RRC ($\alpha = 0.25$) filtered QPSK signal (In-Phase and Quadrature-Phase)

7.3.1.4 Error Vector Magnitude

The *Error Vector Magnitude* (EVM) is a figure of merit for quantifying the quality of digitally modulated signals. The representation of the error vectors takes place in a constellation diagram. Figure 7.7 on the left shows a part of a constellation diagram with an error vector which is the geometrical difference between the measured signal and the reference signal. This example only shows one measured symbol. In this case, the magnitude of the error vector equals the EVM. The EVM contains information about the phase error and magnitude error. Figure 7.7 on the right shows the error vector magnitude for more measured symbols (represented by a cloud around the corresponding ideal symbol point).

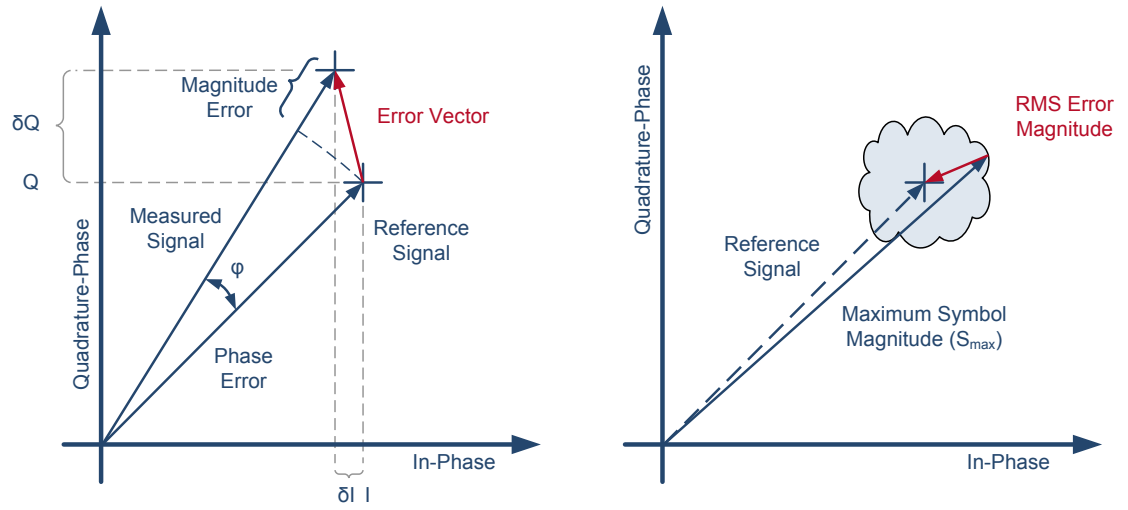


Figure 7.7: Error Vector and Error Vector Magnitude [35], [88]

The EVM_{RMS} is the sum of the magnitudes of all error vectors divided by the total number of acquired symbols. This number depends on the chosen normalization method. EVM mea-

surements are often realized by *Vector Signal Analyzers* (VSA) or instruments which capture a sequence in the time domain. The calculation of EVM is done by software but the signals are down converted and demodulated before [63], [88]. In literature, there are EVM calculations based on different normalization methods [89], [68]. The error vector magnitude is expressed in percent and the lower the EVM value the better.

EMV based on normalization according to the average power of the reference signal is defined by the following formula [70], [84]:

$$EVM_{RMS,Ref} = \sqrt{\frac{\frac{1}{N} \cdot \sum_{j=1}^{N} \left(\delta I_j^2 + \delta Q_j^2 \right)}{\frac{1}{N} \cdot \sum_{j=1}^{N} \left(I_j^2 + Q_j^2 \right)}} \cdot 100\% \tag{7.1}$$

The EMV calculation based on normalization of the peak constellation power is defined by the formula [35],[24]:

$$EVM_{RMS,Peak} = \sqrt{\frac{\frac{1}{N} \cdot \sum_{j=1}^{N} \left(\delta I_j^2 + \delta Q_j^2 \right)}{S_{max}^2}} \cdot 100\% \tag{7.2}$$

The last normalization method for the EVM calculation is based on average constellation power:

$$EVM_{RMS,Average} = \sqrt{\frac{\frac{1}{N} \cdot \sum_{j=1}^{N} \left(\delta I_j^2 + \delta Q_j^2 \right)}{S_{avg}^2}} \cdot 100\% \tag{7.3}$$

I, Q: In-Phase- and Quadrature-Phase-Coordinates of the reference signal
$\delta I, \delta Q$: In-Phase- and Quadrature-Phase-Parts of each error vector
N: Number of received symbols
S_{avg}: Magnitude of the vector to the average constellation power
$S_{max} = \max_{k \in [1....N]} \left\{ I_k^2 + Q_k^2 \right\}$: Magnitude of the vector to the outermost received symbol which belongs to the appropriate constellation

7.3.1.5 Modulation Error Ratio

In comparison to the EVM the *Modulation Error Ratio* (MER) is also a method to obtain the quantitative measure of the signal quality of digitally modulated signals. The MER can be seen as a digital complex baseband *Signal to Noise Ratio* (SNR) and it also has linkage to the *Bit Error Rate* (BER). For the calculation of the MER the error vector of each symbol is used, which is the geometrical difference between the measured signal and the reference signal (see constellation diagram in figure 7.7 and 7.8). The modulation error ratio is expressed in decibels and the higher the MER value the better. The MER can be calculated as follows [24], [35]:

$$MER = 10 \cdot \log_{10} \cdot \left[\frac{\sum_{j=1}^{N} \left(I_j^2 + Q_j^2 \right)}{\sum_{j=1}^{N} \left(\delta I_j^2 + \delta Q_j^2 \right)} \right] \tag{7.4}$$

I, Q: In-Phase- and Quadrature-Phase-Coordinates of the reference (ideal) signal
$\delta I, \delta Q$: In-Phase- and Quadrature-Phase-Parts of each error vector
N: Number of received symbols

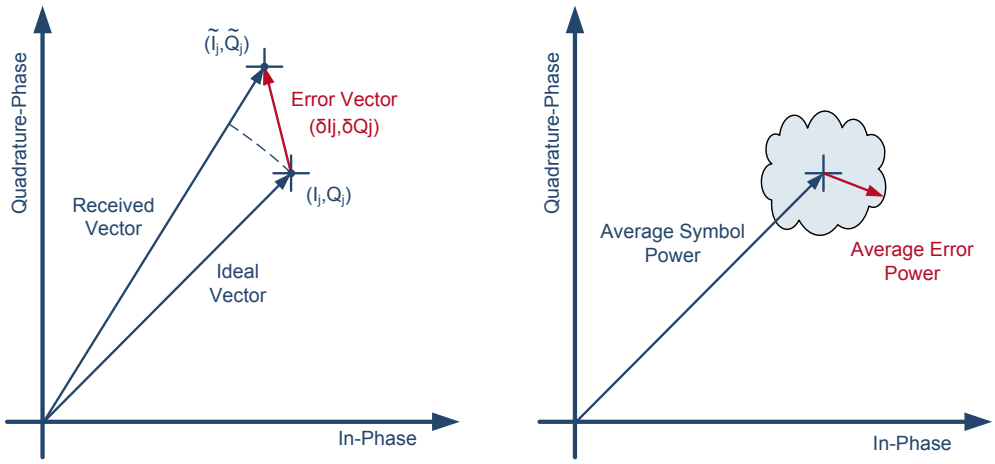


Figure 7.8: Modulation Error Ratio [35], [85]

7.3.1.6 Error Vector Magnitude vs. Modulation Error Ratio

The MER and EVM are closely related and the respective value can be computed by each other. For comparison, the two measurements are expressed as simple voltage ratios. The modulation error ratio expressed as simple voltage ratio MER_V is:

$$MER_V = \frac{\sqrt{\sum_{j=1}^{N}\left(I_j^2 + Q_j^2\right)}}{\sqrt{\sum_{j=1}^{N}\left(\delta I_j^2 + \delta Q_j^2\right)}} \tag{7.5}$$

The extension by the factor $\sqrt{\frac{1}{N}}$ will lead to:

$$MER_V = \frac{\sqrt{\frac{1}{N}\cdot\sum_{j=1}^{N}\left(I_j^2 + Q_j^2\right)}}{\sqrt{\frac{1}{N}\cdot\sum_{j=1}^{N}\left(\delta I_j^2 + \delta Q_j^2\right)}} \tag{7.6}$$

The error vector magnitude expressed as simple voltage ratio EVM_V is:

$$EVM_V = \sqrt{\frac{\frac{1}{N}\cdot\sum_{j=1}^{N}\left(\delta I_j^2 + \delta Q_j^2\right)}{S_{max}}} \tag{7.7}$$

The relation of MER_V (7.6) and EVM_V (7.7) looks as follows:

$$MER_V \cdot EVM_V = \frac{\sqrt{\sum_{j=1}^{N}\left(I_j^2 + Q_j^2\right)}}{S_{max}} = \frac{1}{V} = \frac{S_{RMS}}{S_{MAX}} \tag{7.8}$$

$$MER_V = \frac{1}{EVM_V \cdot V} \tag{7.9}$$

The character V denotes the ratio of the peak voltage level to the mean voltage level and is calculated over a large number of symbols. The EVM and MER are essentially the same methods to obtain the quantitative measure of the signal quality of digitally modulated signals. However, the MER is the preferred measurement method, because the MER can be seen as a form of signal-to-noise ratio measurement and gives information of the receiver performance which demodulates the incoming signal [24], [35].

7.3.2 Proposed Method for the Characterization of the Uplink Signal Quality

As mentioned before, the working groups of the ISO have been looking for an appropriate measurement and characterization method of the uplink signal quality in contactless proximity systems which support VHBR. The represented characterization method in this chapter is just a proposal and has not been elaborated completely. Concerning this matter, there is still work that needs to be done. The measurement method of the uplink signal based on signal vector analysis (e.g. MER) is nothing new in contactless proximity systems. The application note [80] shows a method to measure the *Electromagnetic Disturbance* (EMD) emitted by the PICC. EMD is an unwanted form of load modulation and a high EMD level degrades the signal quality and thus the communication performance. The unwanted form of load modulation is caused by load changes generated by switching of internal digital circuits within the PICC.

7.3.3 State of the Art

Waveform characteristics like modulation index, overshoots values, rise and fall times of the PCD field are defined by the ISO/IEC 14443 [42] product standard. However, the wave shape (rise and fall times) of the load-modulated carrier signal is not standardized. Only the *Load Modulation Amplitude* (LMA) (Modulation depth) of the side band levels within the operating range $H_{min} = 1.5A/m$ and $H_{max} = 7.5A/m$ is specified in the product standard [42]. The load modulation depth of the PICC must have at least the value $22/H^{0.5}mV$ and the PCD must be able to receive a load-modulated carrier signal with an amplitude greater than or equal to $18/H^{0.5}mV$. Both characteristic curves are depicted in figure 7.9.

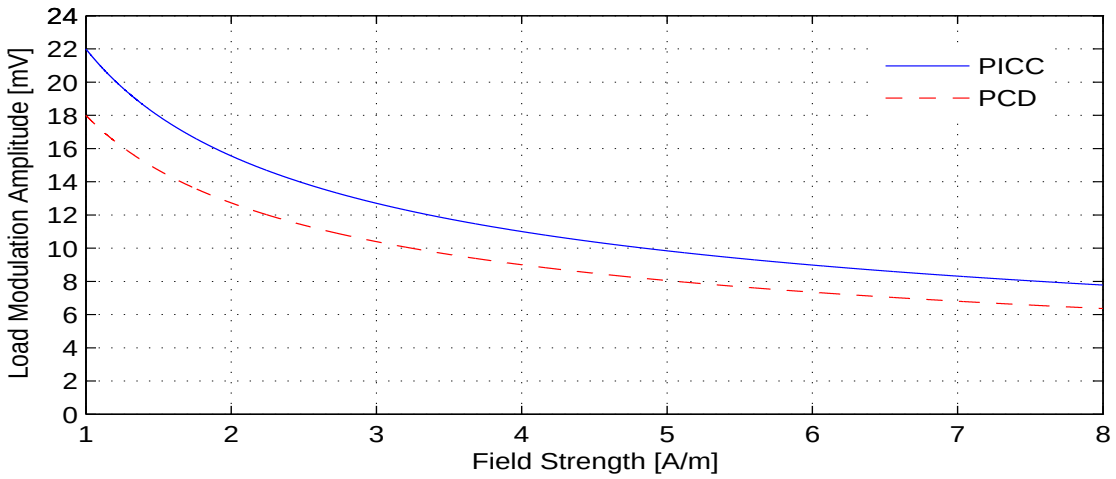


Figure 7.9: LMA as a function of field strength [81]

The current test standard ISO/IEC 10373-6 [43] for contactless proximity cards (ISO/IEC 14443 [42]) describes the measurement method of the LMA with a digital oscilloscope. The hardware test apparatus also includes a measurement tower which consists of two sense coils, a calibration coil and a PCD test assembly (see figure 3.10 in chapter 3.3.2). With this hardware setup the load-modulated carrier signal is measured and exactly two subcarrier cycles are used for the calculation of the *Discrete Fourier Transformation* (DFT). The DFT only delivers the amplitude

peaks of the upper and lower sidebands at $f_c + f_{sc}$ and $f_c - f_{sc}$, which should be above the standardized values. But in the product standard no additional information concerning transient effects (settling, overshoots, rise and fall times, etc.) is specified. For an NFC device in card emulation mode the load modulation amplitude is standardized in the product standard ISO/IEC 18092 (Near Field Communication Interface and Protocol, NFCIP-1) [46] and ECMA-340 [40]. The measurement and evaluation method is defined in the standard ECMA-356 (NFCIP-1- RF Interface Test Methods) [41] using also a DFT for the determination of the load modulation amplitude. The measurement of the side band levels can also be performed by a spectrum analyzer which can be used in the time domain as well as in the frequency domain [81].

The following section introduces a method for characterization of the load modulation of a proximity transponder in the complex plain. This characterization approach resembles the previously shown modulation error ratio method. The characterization requires a special measurement hardware as well as a software setup. For the hardware an existing contactless proximity reader realized by an FPGA rapid prototyping system (see chapter 6.2) and a special antenna setup (standardized in ISO/IEC 10373-6 [43]) are used. The analysis/evaluation software was written by the software tool Matlab and the input vectors for the scripts were measured directly by the ADC in the contactless prototyping reader system. The input vector equates to the sampled carrier signal sequence with the load modulation of the PICC. Another method for acquisition of the input vector is the usage of a digital oscilloscope.

Transformation from the Time Domain to the Complex Domain

For the illustration of the transformation principle (time domain to In-Phase and Quadrature-Phase plane) an uplink sequence with a subcarrier frequency of 847.5 kHz and a data rate of 847.5 kbit/sec are used (see figure 7.10). The uplink sequence was sampled with a sampling rate of $4 \cdot 13.56\,MHz = 54.24\,MHz$, which results in four sample points per carrier period. The I/Q separation on the carrier signal as well as the undersampling on the subcarrier signal (see chapter 5.5.4.4) are shown in the lower graph of figure 7.10 which is a detailed representation of the upper graph. The undersampling rate for the I/Q separation on the subcarrier signal was doubled because the sampling rate would otherwise be too low.

The next step is the transformation from the time domain to the complex domain. The sample points of the In-Phase sequence (red points in figure 7.10) are mapped on the X-coordinate of the constellation diagram in figure 7.11a. The same procedure is done for the sample points of the Quadrature-Phase sequence (black points in figure 7.10) which are mapped on the Y-coordinate of the same constellation diagram. As mentioned in a previous chapter, the start point of the PICC response is not defined and, therefore, a synchronisation concerning phasing of carrier and sampling is not given. The undersampling method is based on a non-coherent demodulation, i.e. the beginning of the carrier can vary and so the sampling points are not in phase with the carrier frequency. This behavior can also be seen in the constellation diagram 7.11a. The location of the I/Q sampling points within the diagram is not as precisely defined as shown in figure 7.4a and they depend on the start point of the sampling process. The two clouds represent the two symbols of the load modulation, which contains the information. For a joint and uniform presentation, the I/Q sampling points in figure 7.11a are shifted around the zero-point, the result is shown in 7.11b.

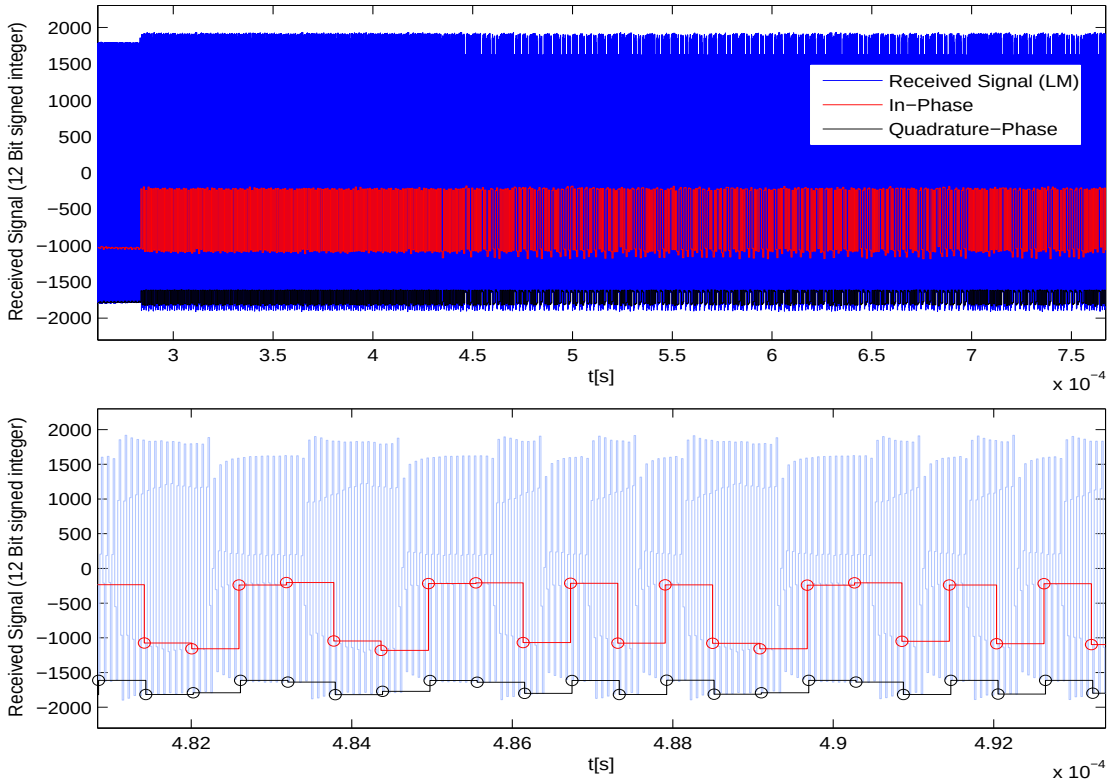


Figure 7.10: Load-modulated carrier signal in the time domain (In-Phase and Quadrature Phase)

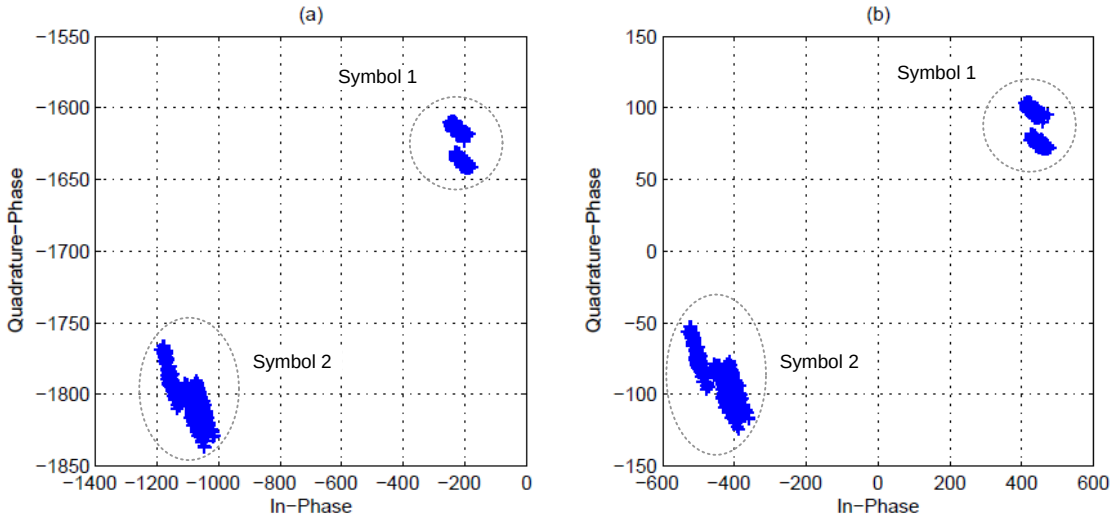


Figure 7.11: Constellation diagram: (a) I/Q Representation, (b) I/Q Representation shifted around the zero-point

The next step is the mapping of all I/Q sample points with a negative sign to the first quadrant. In this case all points within the fourth quadrant of the constellation diagram are mapped into the first one (see figure 7.12). The next section describes the calculation of the modulation error ratio.

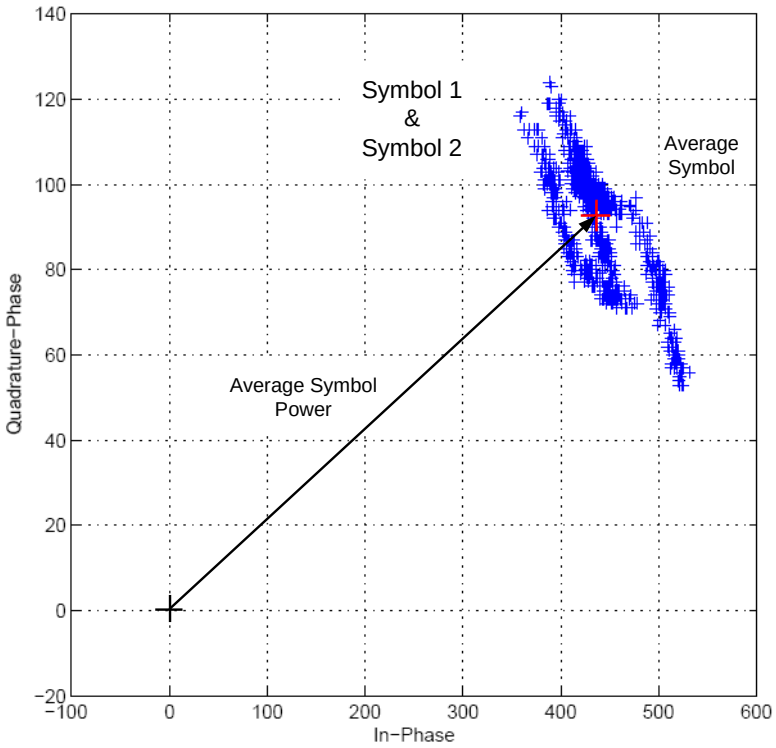


Figure 7.12: Constellation diagram: Mapped I/Q samples with average symbol

Calculation of the Modulation Error Ratio

In literature (chapter 7.3.1.5) the calculation of the MER is based on an ideal reference symbol-/vector (see formula 7.4). Due to the non-coherent demodulation (no synchronous sampling) the ideal reference symbol of the transmitter (PICC) is not available. An average constellation symbol is used instead. Thus, a mean average value is calculated for all I/Q sampling points (red marker in figure 7.12). Finally the MER (expressed in decibels) can be calculated as follows:

$$MER = 10 \cdot \log_{10} \cdot \left[\frac{\sum_{j=1}^{N} \left(I_{avg,j}^2 + Q_{avg,j}^2 \right)}{\sum_{j=1}^{N} \left(\delta I_j^2 + \delta Q_j^2 \right)} \right] \tag{7.10}$$

I_{avg}, Q_{avg}: In-Phase- and Quadrature-Phase-Coordinates of the calculated average symbol
$\delta I, \delta Q$: In-Phase- and Quadrature-Phase-Parts of each error vector
N: Number of received symbols

Modulation Error Ratio as a Function of the Operating Distance

Figure 7.13 shows the calculation of the MER as a function of the operating distance which is proportional to the field strength. For this, formula 7.10 was used. The uplink sequences which comprise the load modulation with a subcarrier frequency of 847.5 kHz and data rate of 847.5 kbit/sec were measured for different distances from zero to 70mm and with a granularity of five millimeters. The progressive form of the MER plot shows a decreasing behavior, which was also expected.

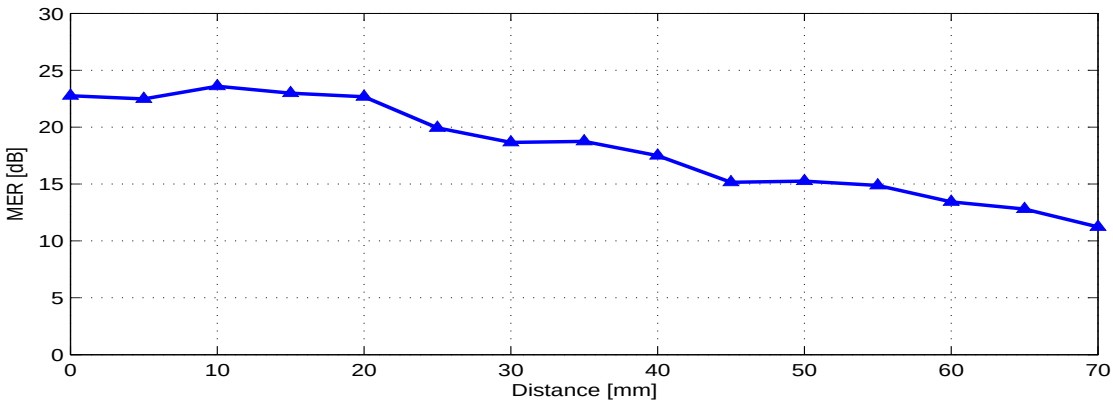


Figure 7.13: MER as a function of operating distance

Classification of the Load Modulation Quality

The last section of this chapter covers the classification of the load modulation quality. Due to the distribution of the I/Q samples in the constellation diagram a classification of the load modulation quality can be given. Figure 7.14 shows an uplink sequence which comprises the load modulation of the PICC (subcarrier frequency of 847.5 kHz and data rate of 847.5 kbit/sec) with a very distinctive transient behavior.

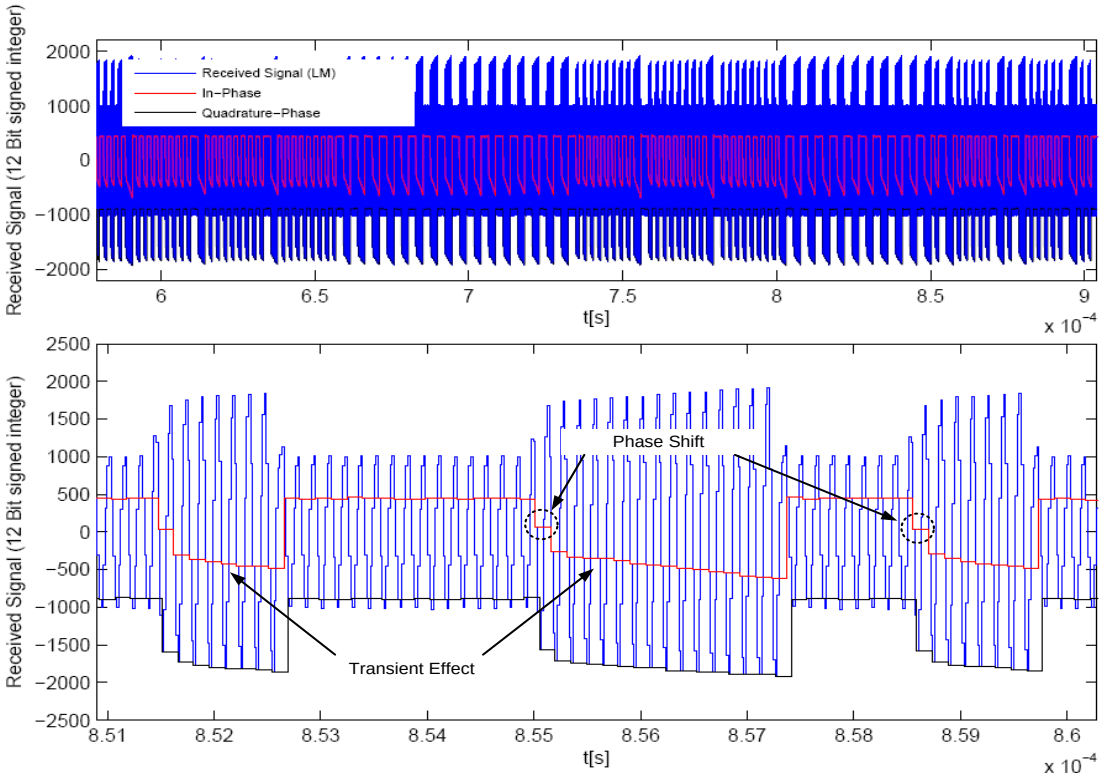


Figure 7.14: Load Modulated Carrier Signal in Time Domain (I/Q Phase)

The lower graph of figure 7.14 is a detailed representation of the upper graph and shows the transient signal behavior (settling effects) due to the quality factor of the resonant circuit (reader antenna). This factor influences the transmission behavior and hence affects the main properties of the system, e.g. energy transfer, bandwidth, spectrum, and the data rate (see chapter 3.1.2). In addition, the figure shows the phase shift caused by the load modulation of the PICC. Whenever a load modulation change appears, a dedicated small phase shift of the carrier signal takes place. To make these two effects visible, the sampling resolution was increased to $8 \cdot 13.56\,MHz = 108.48\,MHz$ and no undersampling technique based on the subcarrier signal was applied. Due to the short operation range of the contactless reader system ($< 10cm$) the influence of noise on the carrier signal is very small and, therefore, this quantity is irrelevant and can be neglected. By contrast, the quality of the receiving load-modulated carrier signal is important and relevant. This signal is influenced by the electro-magnetic coupling, operation distance, field strength and resonance frequency of the transponder and the quality factor Q of the reader antenna which was already mentioned before.

The transient behavior of the load-modulated carrier signal as well as the phase shifts can be seen in the complex domain. Therefore, a transformation from the time domain to the complex domain must take place. The sample points of the In-Phase sequence (red curve in figure 7.14) are mapped on the X-coordinate of the constellation diagram in figure 7.15. The same procedure is done for the sample points of the Quadrature-Phase sequence (black curve in figure 7.14) which are mapped on the Y-coordinate of the same constellation diagram.

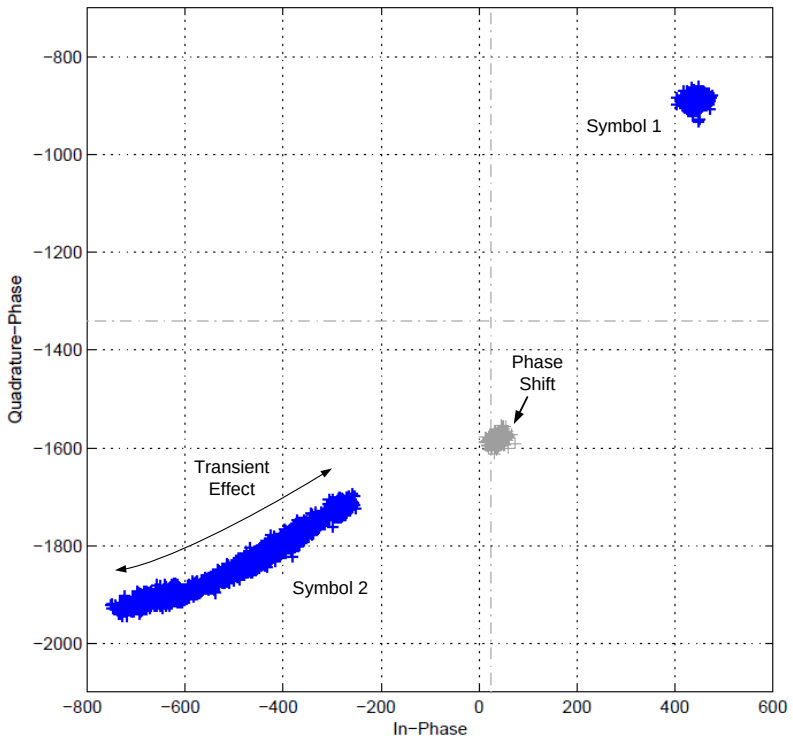


Figure 7.15: Classification of the Load Modulation in the Complex Domain

The In-Phase and Quadrature-Phase sequence is very stable when the load modulation is active (reduced LMA). When the load modulation is inactive (normal LMA), the In-Phase and Quadrature-Phase sequence have a transient behavior. These two states and their characteristics are also depicted in the scatter plot 7.15. *Symbol 1* represents the state *load modulation inactive* and *Symbol 2* the state *load modulation active*. Compared to symbol 2 the sample distribution of symbol 1 is marginal, because symbol 2 comprises the whole transient behavior. The phase shift is also depicted in the scatter plot and is represented by an additional cloud of sample points. For a better and uniform representation the I/Q sampling clouds can be shifted around the zero-point. In this figure the zero point is marked by a dotted line. The quantity of the modulation error ratio which was calculated in the previous section 7.3.3 will also be affected by the transient behavior as well as the phase shifts.

Another classification method of the load modulation quality is the representation of the I/Q samples in a histogram. This method shows the separated distribution of the In-Phase as well as the Quadrature-Phase samples. Figure 7.16 shows an example of a histogram for both the I-Channel and the Q-Channel in which the I/Q sample points were taken from the previously depicted figures 7.14 and 7.15. The sample range of the I-Channel lies between approx. -750 and 450 and the sample range of the Q-Channel lies between approx. -1950 and -900. But this sample range can vary and depends on the sampling start point. As depicted in the two histograms 7.16 this representation method also shows the transient behavior and the phase shift caused by the PICC.

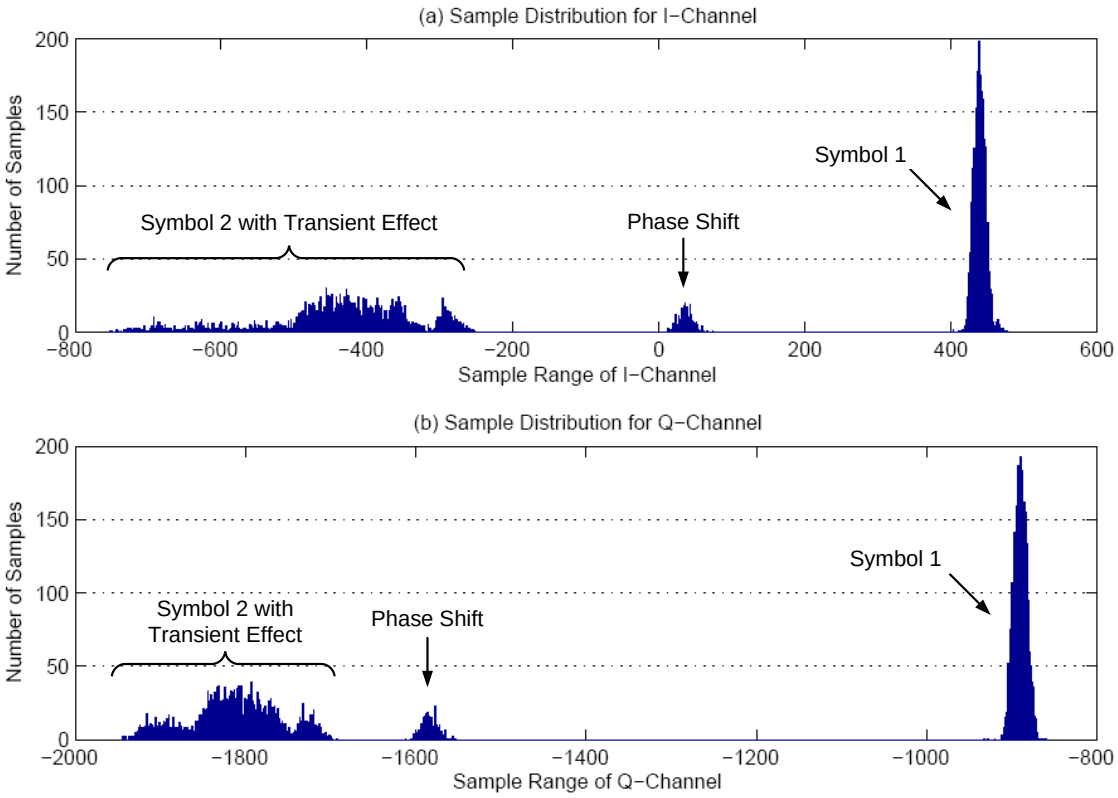


Figure 7.16: I/Q Sample distribution - Histogram

7.4 Simulation and Measurement Results

7.4.1 Uplink of 13.56 MBit/sec Based on NRZ Coding

Matlab Simulation

The Matlab simulation in figure 7.17 illustrates the demodulation process of the received communication sequence. The signal *x[t]* is the input waveform for the Matlab simulation which was measured directly in the reader system by means of the ADC. The waveform shows the load modulation with a NRZ coded baseband data and a data rate of 13.56 MBit/sec. According to the proposed undersampling method (I/Q separation on carrier and 'subcarrier' signal) four channels CH_1 to CH_4 are shown in the first plot. In addition, the quiescent offset level and noise threshold can be seen for every channel. The detection of the synchronization sequence is marked by diamonds. The plot in the middle of the figure represents the two channels with the best signal quality and the corresponding quiescent level and signal reference, which are used for further signal processing. The plot below shows the digitized bit stream. A detailed description of the demodulation process was already given in the chapters 5 and 6.

ModelSim Simulation

Figure 7.18 shows the ModelSim simulation results of the digital demodulator which was implemented in the hardware description language VHDL. The signal *adc_i* is the input waveform for the ModelSim simulation which has already been directly measured in the reader system. The waveform shows the load modulation with an NRZ coded baseband data and a data rate of 13.56 MBitsec. The receive unit and the downsampling process are activated by the enable signal *rx_enable_i*. The signals *channel_1* to *channel_4* are the result of downsampling and the further signal processing is based on the generated reference signals *ch1_ref_level* to *ch4_ref_level*. In addition, the digital control lines for the AGC (*agc_enable*), reference level calculation (*ref_level_enable*) and synchronization *synch_detection_enable* are shown. The digitized bit stream *nrz_bitstream* is the output of the demodulator unit.

Measurement

Figure 7.19 indicates the entire uplink communication sequence (Channel 4) and the associated demodulator output signal (Channel 1) measured by an oscilloscope. Channel 3 shows the NRZ coded baseband signal (13.56 Mbit/sec) for the load modulation which is generated by the FPGA. Figure 7.20 shows a detailed measurement of the load modulation and it can clearly be seen that every carrier period is modulated by one baseband data bit.

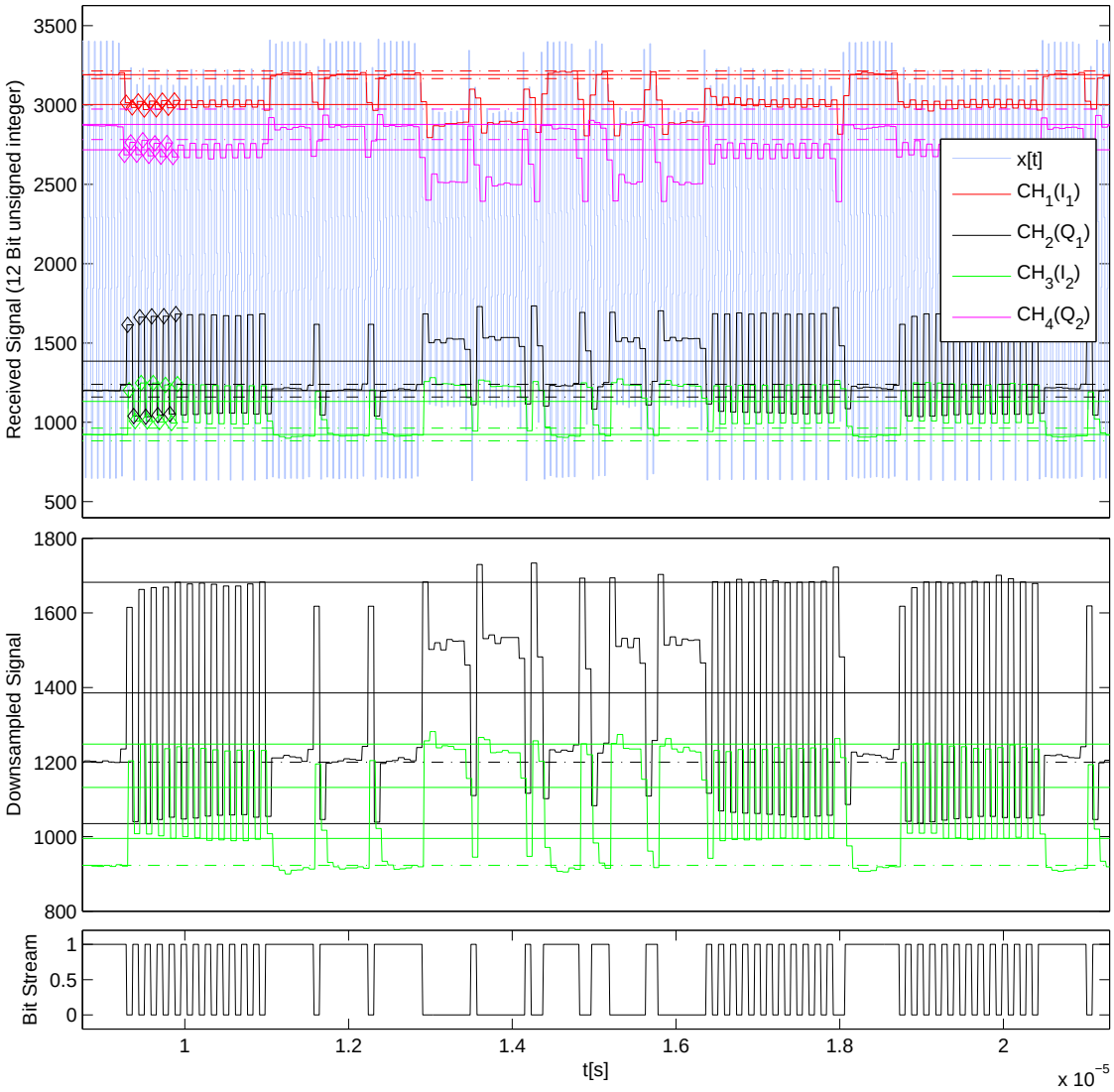


Figure 7.17: Demodulation process of the received communication sequence for 13.56 MBit/sec (Matlab Simulation)

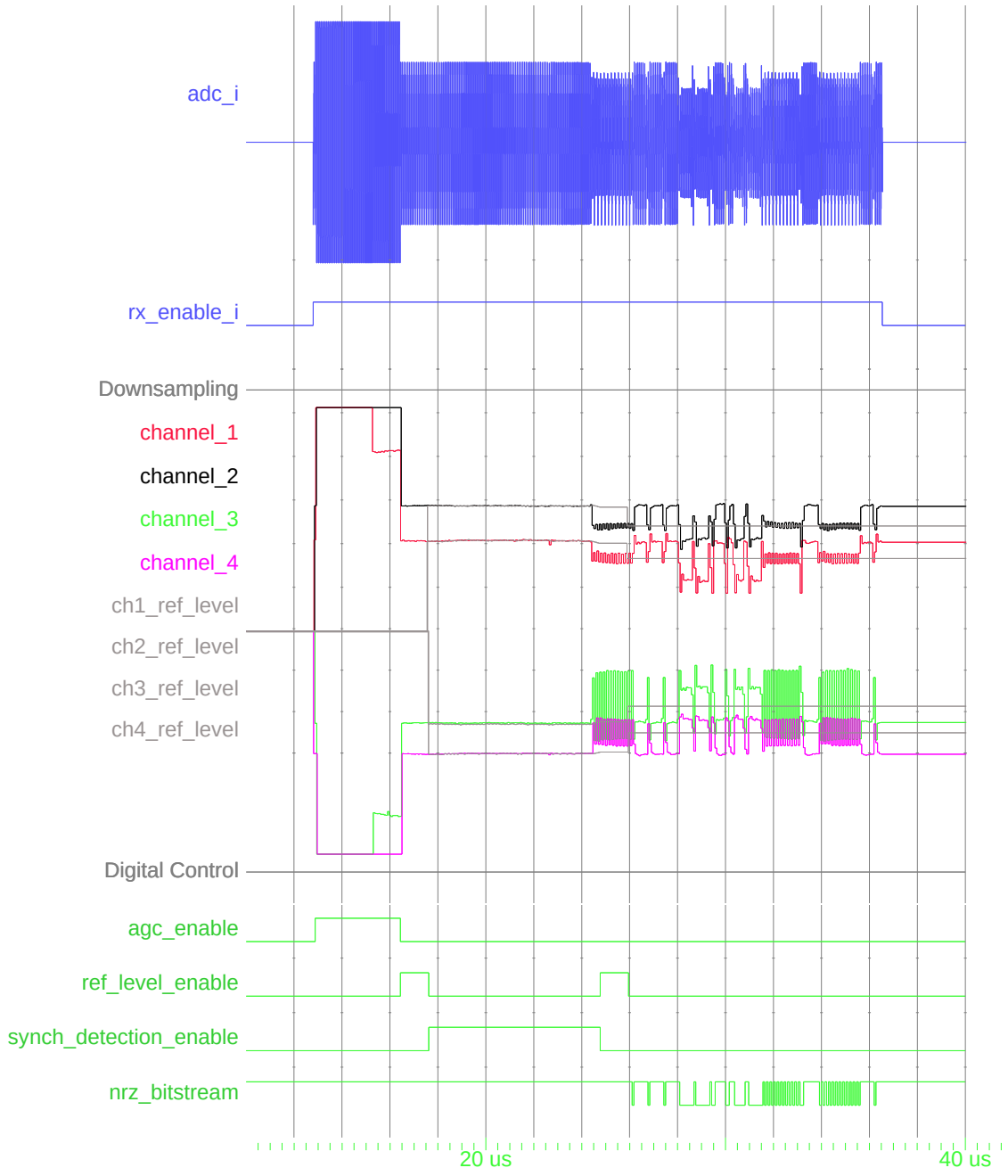


Figure 7.18: Demodulation process of the received communication sequence for 13.56 MBit/sec (ModelSim Simulation)

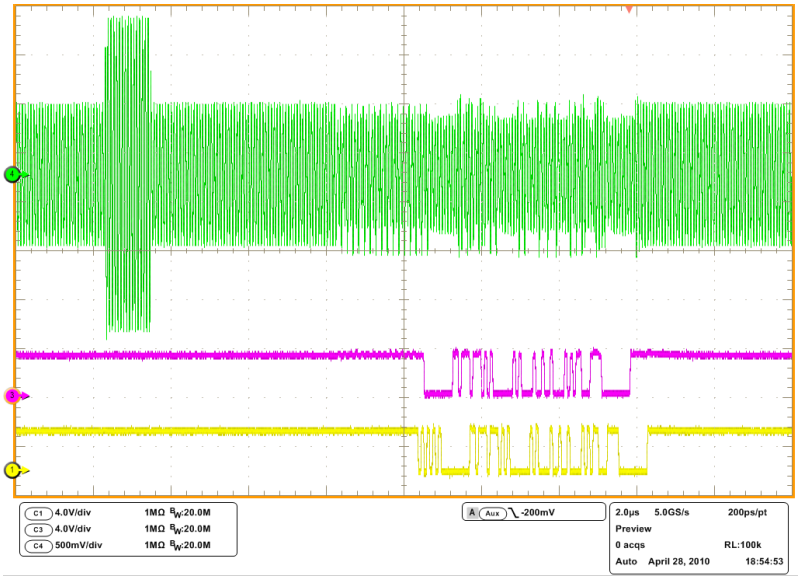


Figure 7.19: Received communication sequence and demodulator output for 13.56 MBit/sec (Measurement)

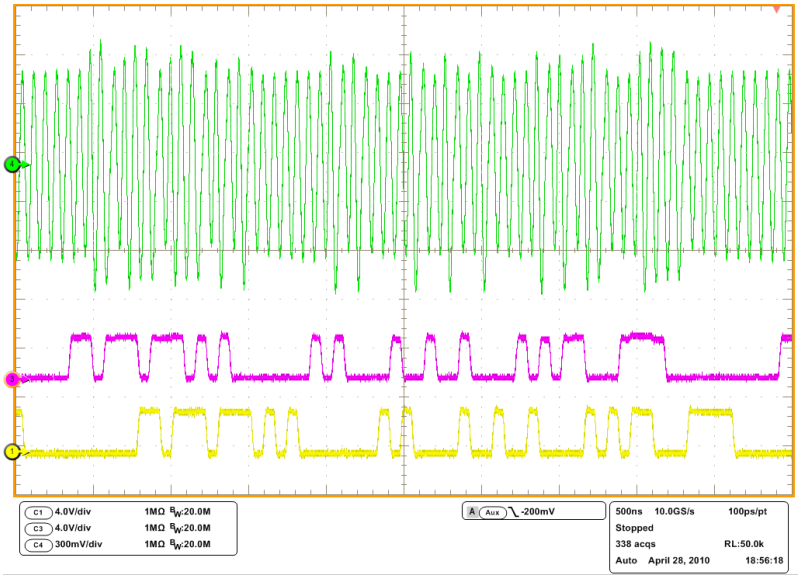


Figure 7.20: Demodulator output for 13.56 MBit/sec (Detailed Measurement)

7.4.2 Carrier Cancellation Based on the Least Mean Square Algorithm

ModelSim Simulation

The theory of the LMS algorithm for carrier cancellation was already discussed in chapter 6.6 and the algorithm was implemented in VHDL. A ModelSim simulation is depicted in figure 7.21 which shows the convergence behavior of the algorithm at the start-up phase. The sampling rate of the *tx_data* signal equals $8 \cdot 13.56 \cdot 10^6 = 108.48$ MSamples/sec. For the sake of completeness the adjusted convergence parameters *lms_adj_step_i* and *lms_update_period_i* are also depicted. The figure clearly shows the automatic adaptation of the filter coefficients *h1* and *h2*. First a repeated overflow of these two coefficients takes place and afterwards a convergence and settling of *h1* and *h2* occur. The waveforms *lms_in* and *lms_out* with a sampling resolution of $4 \cdot 13.56 \cdot 10^6 = 54.24$ MSamples/sec are the input and output signals of the LMS algorithm. In the case of convergence the LMS algorithm eliminates the error signal *lms_error* which is shown in the figure.

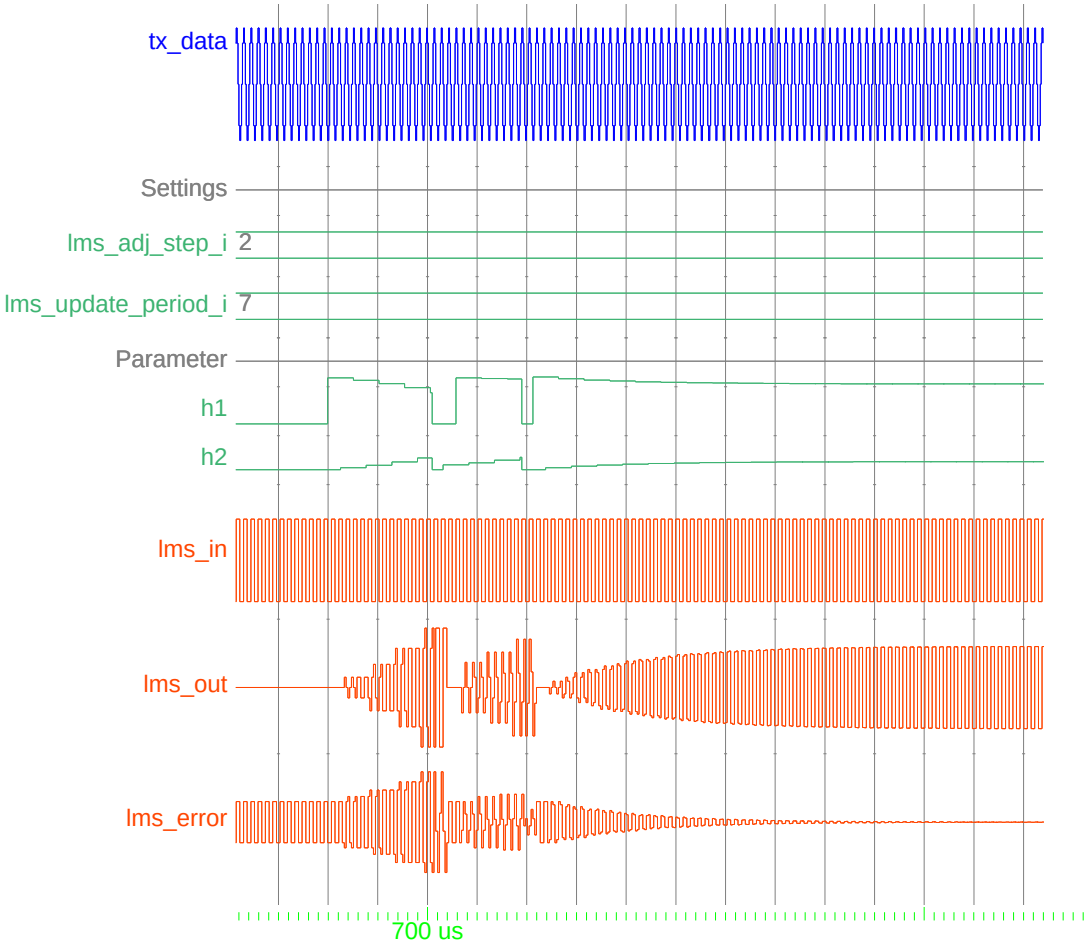


Figure 7.21: Convergence behavior of the LMS algorithm (ModelSim Simulation)

Measurement

Figure 7.22 shows the start-up sequence of the LMS algorithm which was measured within the prototyping reader system. The convergence behavior is the same as shown in the previous simulation. Channel 2 represents the output signal of the LMS algorithm and channel 4 shows the error signal which is used for further signal processing.

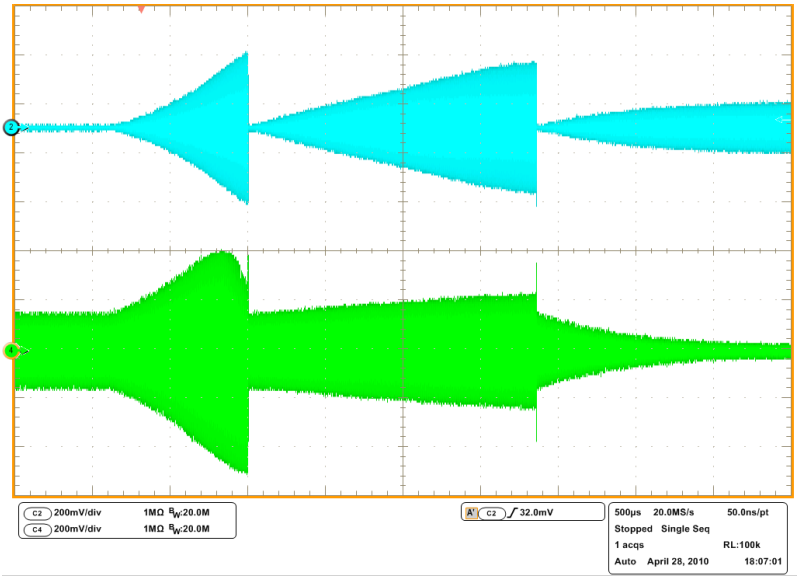


Figure 7.22: Convergence behavior of the LMS algorithm (Measurement)

Figure 7.23 and 7.24 show the difference between switched off and turned on carrier cancellation by means of a received communication sequence. Every figure shows the complete uplink sequence as well as a detailed representation of the load modulation. The improvement of the signal quality based on the LMS algorithm is shown in the second figure 7.24 and the benefit of the usage of the carrier cancellation can be clearly seen.

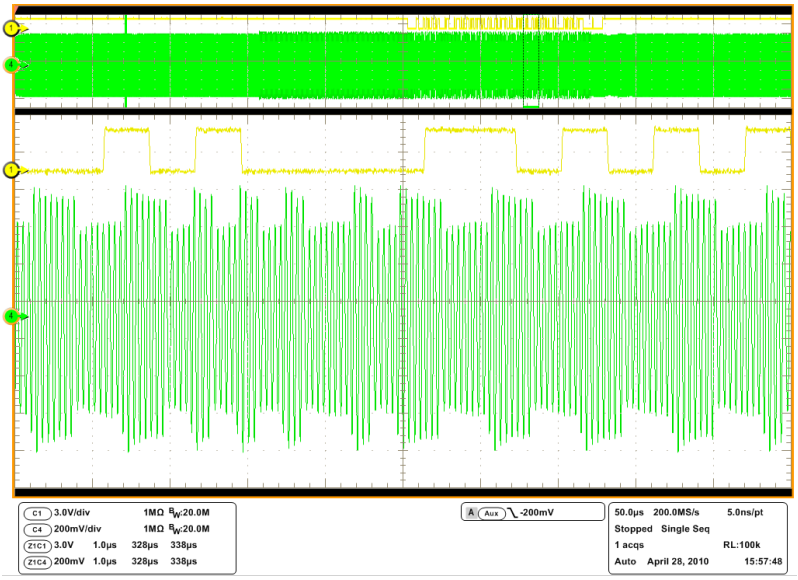


Figure 7.23: Receive sequence without carrier cancellation - LMS inactive (Measurement)

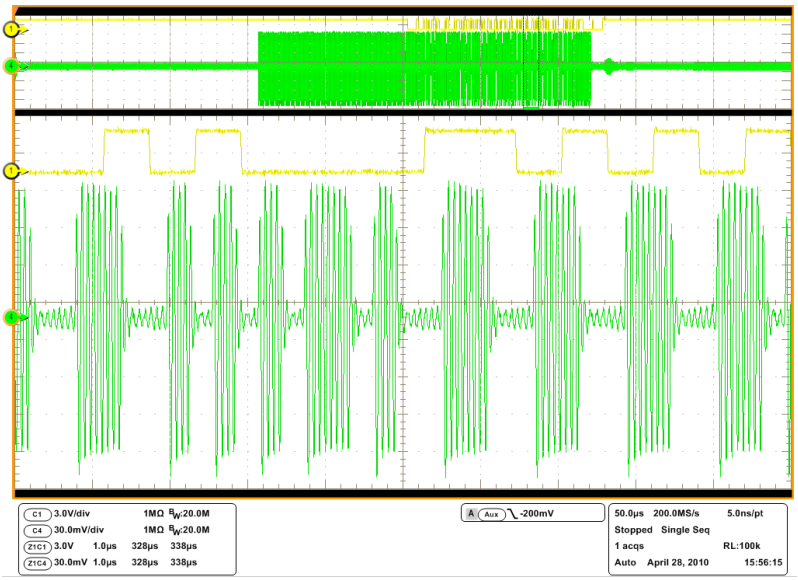


Figure 7.24: Receive sequence with carrier cancellation - LMS active (Measurement)

7.4.3 Comparison of a Conventional and an Improved Antenna Concept for the Reader by Means of the Signal Quality

As already mentioned in the theoretical part of the thesis, an improved antenna concept based on a two-antenna arrangement was used within the prototyping reader system (see chapter 3.3.2). One of the most important parameters of the reader antenna (incl. resonant circuit) is the quality factor Q. The maximum achievable data rate is defined by the quality factor of the reader antenna (reciprocally proportional to each other). The influence of Q on the transmission behavior of the load-modulated carrier signal is shown in the following figures 7.25, 7.27, 7.29, 7.31.
These measurements were carried out for four different data rates: 1.7 Mbit/sec, 3.4 Mbit/sec, 6.8 Mbit/sec and 13.56 Mbit/sec. Channel 1 represents the output signal of the demodulator unit and channel 3 shows the NRZ coded baseband signal for the load modulation which is generated by the FPGA. The quality factor Q of the used reader antenna is 4, which is quite low compared to conventional antenna systems (Q = 15 or 30).
Nevertheless, a substantial influence of the received signal by Q can be seen in the measurement results (Channel 4). In addition, the measurements 7.26, 7.28, 7.30, 7.32 illustrate the enhancement of the reception quality which was achieved by the new, improved antenna concept.

Measurement for Data Rate 1.7 Mbit/sec

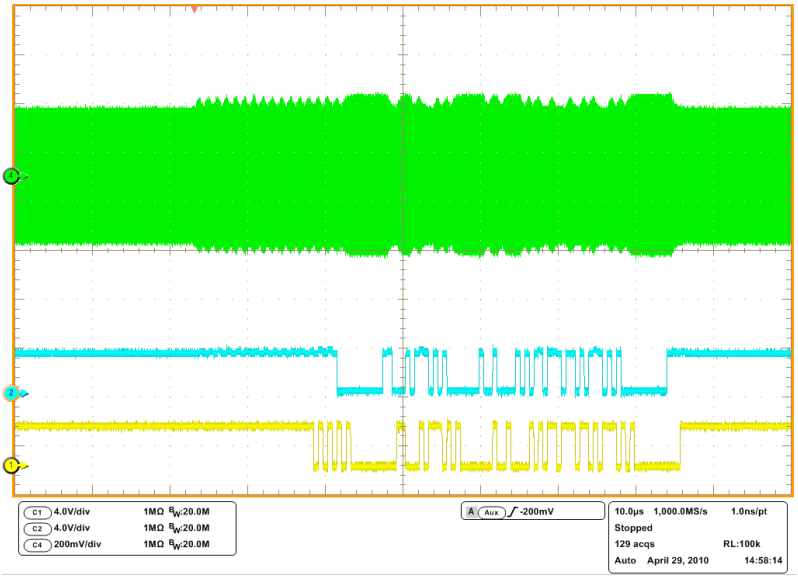


Figure 7.25: Measurement of a received communication sequence with a conventional antenna concept (data rate: 1.7 MBit/sec)

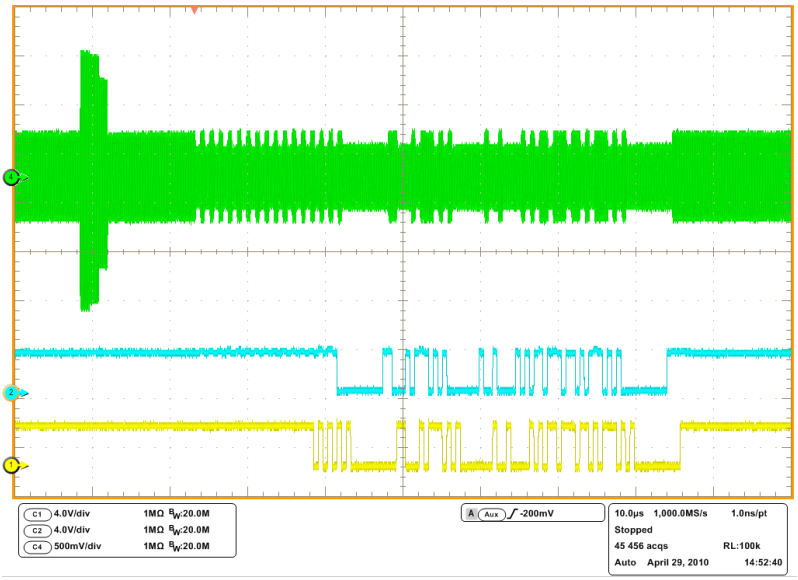


Figure 7.26: Measurement of a received communication sequence with an improved antenna concept (data Rate: 1.7 MBit/sec)

Measurement for Data Rate 3.4 Mbit/sec

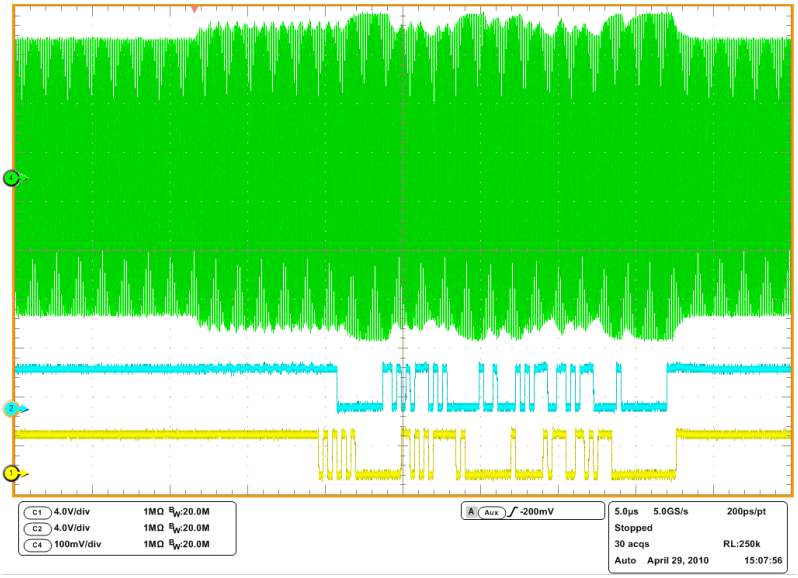


Figure 7.27: Measurement of a received communication sequence with a conventional antenna concept (data rate: 3.4 MBit/sec)

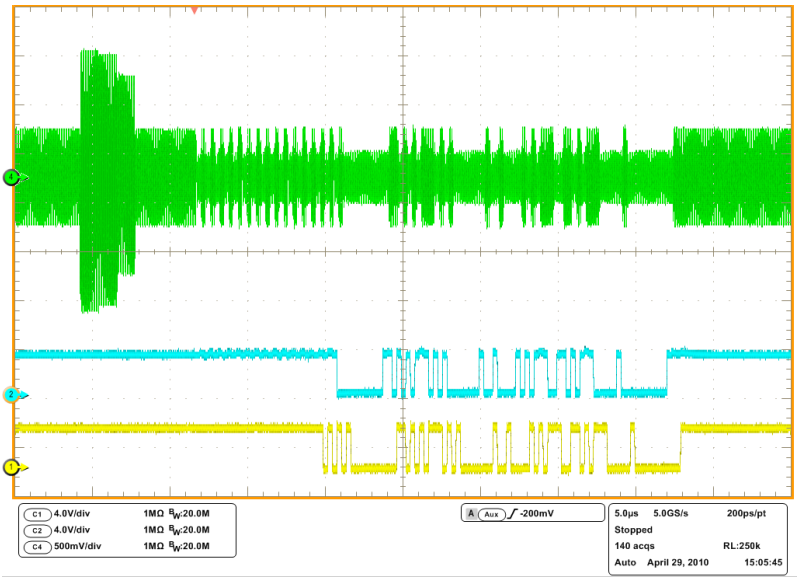


Figure 7.28: Measurement of a received communication sequence with an improved antenna concept (data rate: 3.4 MBit/sec)

Measurement for Data Rate 6.8 Mbit/sec

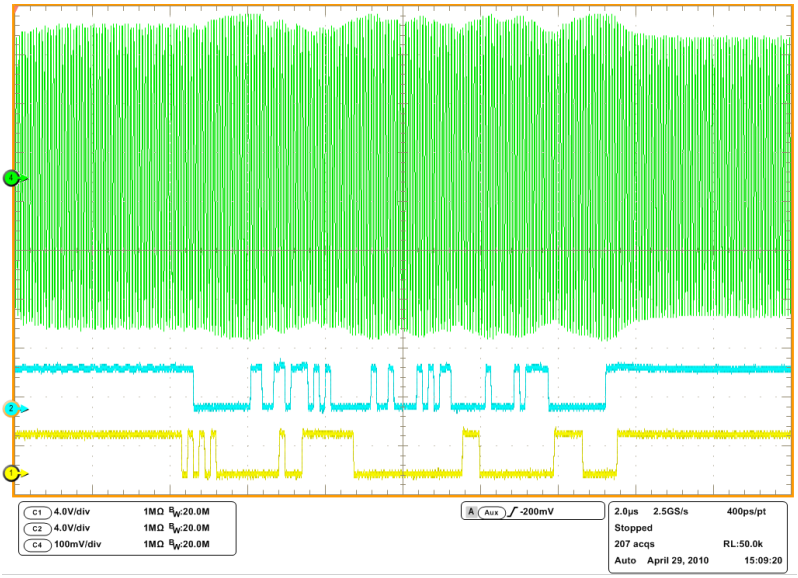


Figure 7.29: Measurement of a received communication sequence with a conventional antenna concept (data rate: 6.8 MBit/sec)

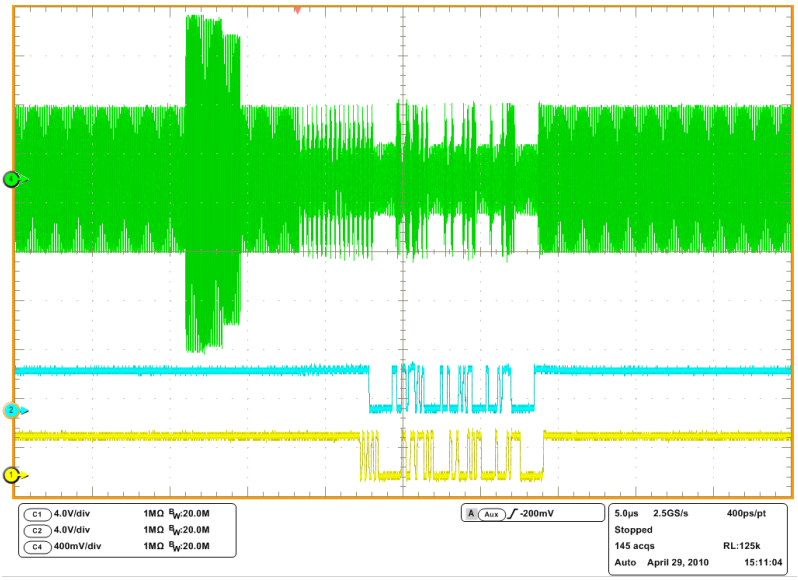


Figure 7.30: Measurement of a received communication sequence with an improved antenna concept (data rate: 6.8 MBit/sec)

Measurement for Data Rate 13.56 Mbit/sec

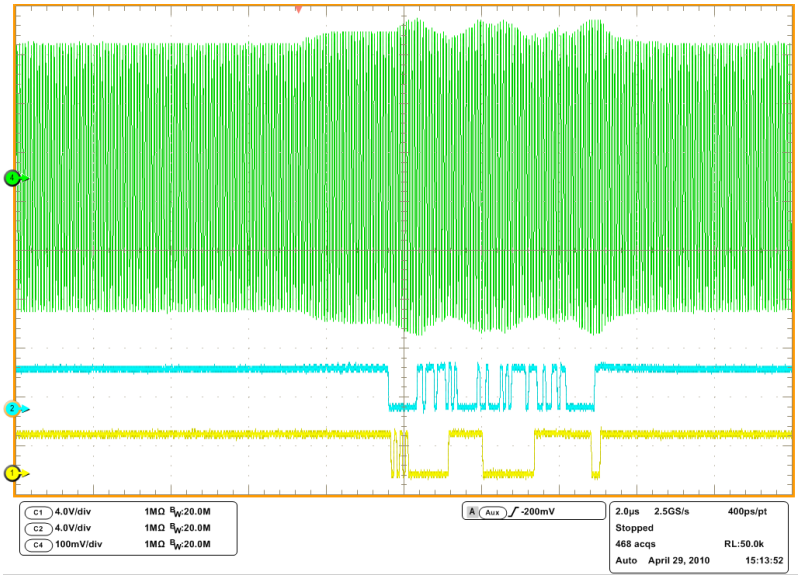


Figure 7.31: Measurement of a received communication sequence with a conventional antenna concept (data rate: 13.56 MBit/sec)

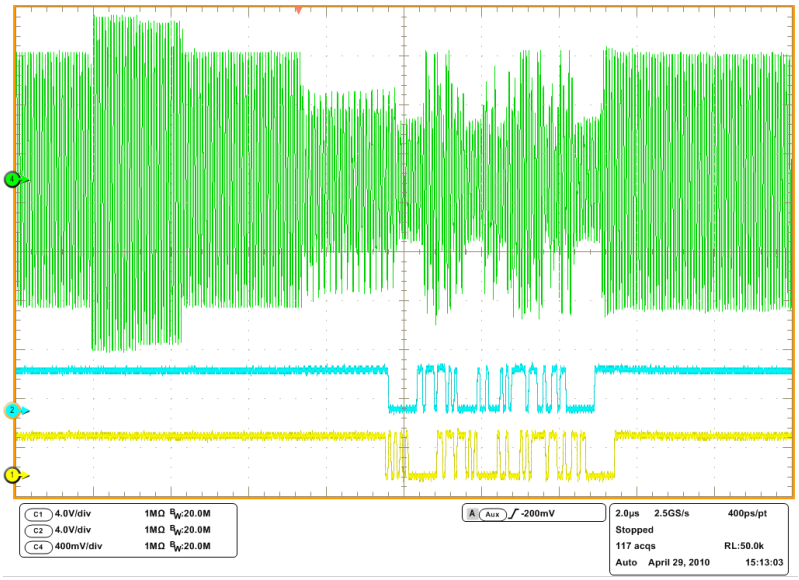


Figure 7.32: Measurement of a received communication sequence with an improved antenna concept (data rate: 13.56 MBit/sec)

7.4.4 Improved Received Signal Quality Based on an Automatic Gain Control Measurement

For a best possible saturation degree of the ADC an automatic gain control was deployed. The theoretical part of the AGC was already discussed in chapter 6.5.2. Figures 7.33 and 7.34 show the improvement of the signal quality if an AGC is used (Channel 4). For the measurements the transponder was placed directly at the reader antenna (distance equals zero). Channel 1 represents the output signal of the demodulator unit and channel 3 shows the NRZ coded baseband signal for the load modulation. As mentioned in a previous chapter, an ADC with a 12 bit resolution was used. This high resolution makes it possible to demodulate the right bit sequence also without the automatic gain control.

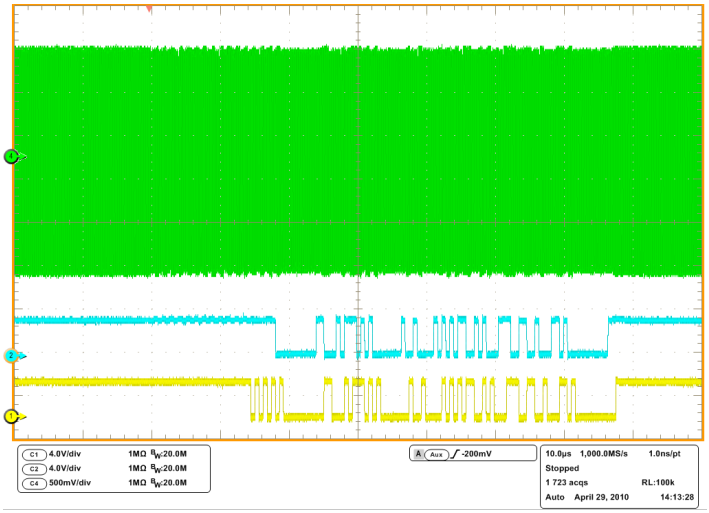


Figure 7.33: Received signal sequence without automatic gain control (AGC inactive)

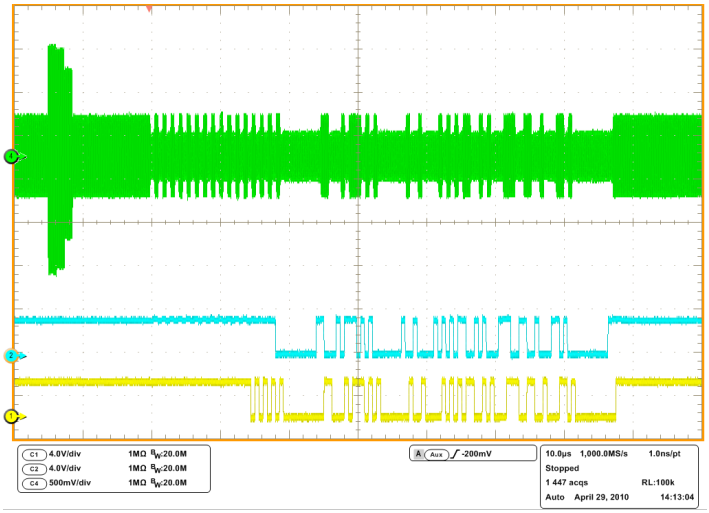


Figure 7.34: Received signal sequence with automatic gain control (AGC active)

7.4.5 Packet Loss Rate

The data exchange between PCD and PICC is based on data packets and data frames. In communication systems the *Bit Error Rate* (BER) is commonly used for quantifying the performance and transmission quality of the communication channel. Within this thesis the *Packet Loss Rate* (PLR) is used for quantifying the transmission performance. This is because of the implemented failure detection mechanism which checks the accuracy of the received data on packet granularity. A comparison between the entire received data packet and the transmitted data packet takes place. This is why the bit error rate cannot be determined by the implemented performance measurement method.

The packet loss rate can be calculated by the following formula:

$$PLR = \frac{Packets_{Lost}}{Packets_{Transmitted}} \tag{7.11}$$

Packet loss rate expressed in percent:

$$PLR_{\%} = \frac{Packets_{Lost}}{Packets_{Transmitted}} \cdot 100\% \tag{7.12}$$

The measurement setup with the prototyping reader system is described and depicted in section 7.2 (see figures 7.1 and 7.2). For measurement the *Reference PICC* (RefPICC) has three windings and is tuned to a resonance frequency of $f_{res} = 13.56\,MHz$. As mentioned before, only the analog front end of a chip card controller (which was placed on the RefPICC) was used for the load modulation and the generation of the digital signal for the uplink was carried out by the FPGA board. The packet loss can occur in the downlink as well as in the uplink, but with the described measurement setup the packet loss can be limited to the uplink. The PLR was determined for different data rates as a function of the communication distance. The following data rates with the corresponding subcarrier frequencies and coding schemes were used:

Data Rate	f_{SC}	etu	Baseband Coding	Subcarrier Modulation
kbit/sec	MHz	-	-	-
1 700	1.7	1	NRZ	BPSK
3 400	3.4	1	NRZ	BPSK
6 800	6.8	1	NRZ	BPSK
13 560	-	1	NRZ	-

Table 7.1: Adjustments for PLR Measurements (rounded data rates)

For each measurement run (per one data rate and communication distance) 10,000 packets were used and for every packet a randomized data set was generated. The results of the achieved packet loss rate is shown in figures 7.35 (100 bytes/packet) and 7.36 (255 bytes/packet).

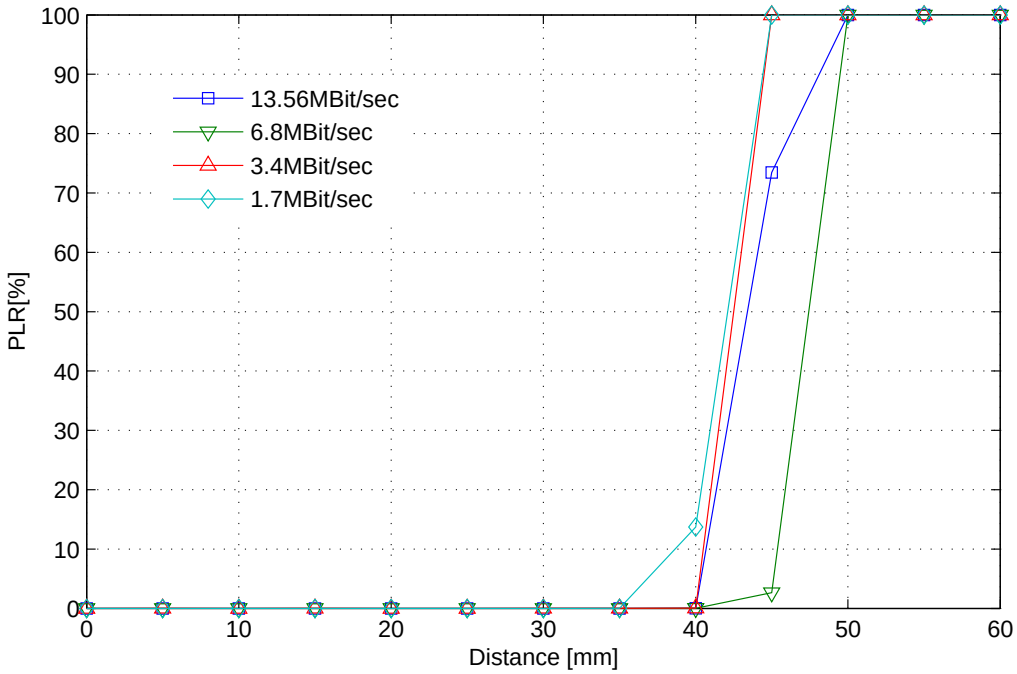


Figure 7.35: PLR for different data rates (10,000 packets and 100 bytes/packet)

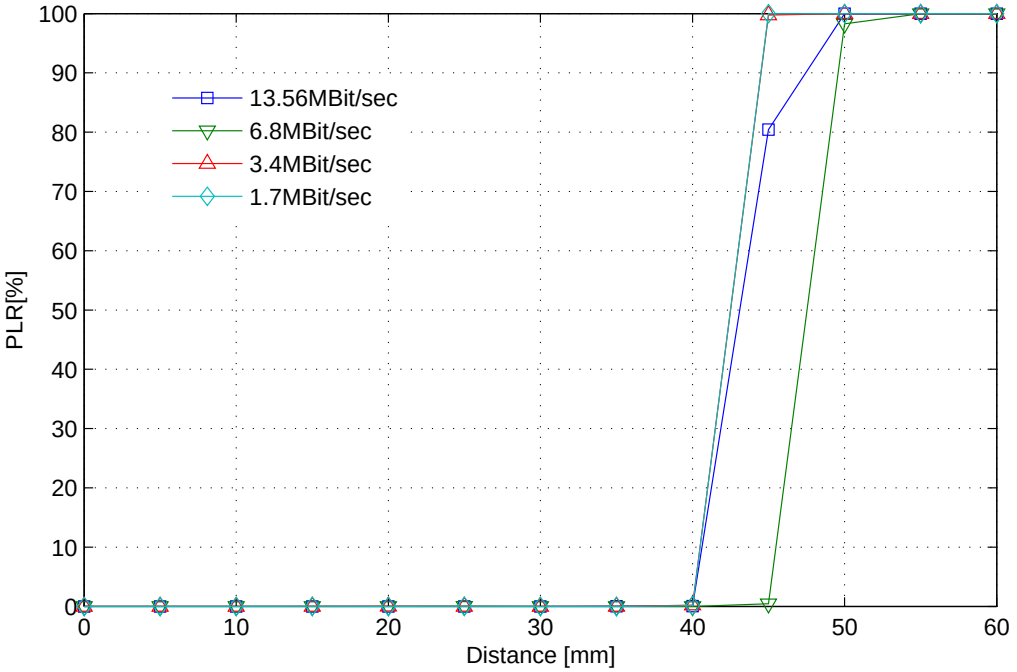


Figure 7.36: PLR for different data rates (10,000 packets and 255 bytes/packet)

8 Research Summary, Conclusion and Outlook

8.1 Conclusion

One of the essential research objectives in this PhD thesis was the elaboration and implementation of very high data rates in a contactless proximity system. According to current research reports, present contactless prototyping systems reach data rates up to 6.78 Mbit/sec. Due to the elaborated and implemented transmission method elaborated in this thesis (Chapter 4.2.4), a duplication of the baud rate was reached. Due to the contactless prototyping reader system, transmission rates up to 13.56 Mbit/sec are reached between transponder and the contactless reader. Consequently, the performance gain concerning the data rate is 16 times higher than the currently standardized maximum data rate. The measurement results correspond to the respective simulation outputs (chapter 7.4) and confirm the mentioned transmission rate of 13.56 Mbit/sec. As a result, the first contactless proximity prototyping reader system to support such high data rates was realized.

Within the scope of the ReadRF project and in collaboration with my dedicated project colleagues, five invention disclosures and patent applications have been worked out:

1. The provision of very high data rates in contactless proximity systems requires the elimination of the influence of the quality factor Q caused by the resonant circuit (reader antenna). This factor affects the transmission behavior and thus limits the maximum achievable data rate. The patent application [53] describes a solution to eliminate the influence of the quality factor. The solution includes an improved antenna concept based on a two-antenna arrangement which increases the communication quality significantly. The concept is described in the theoretical part of this thesis 3.3.2. The enhancement of the reception quality which was achieved by the new, improved antenna concept can be seen in chapter 7.4.3.

2. The data communication and power supply in contactless proximity systems are accomplished with only one reader antenna at the proximity coupling device. The data rate for the downlink (reader to transponder/card) is limited by the narrow bandwidth which again is limited by the resonant circuit of the antenna. The patent application [54] introduces a method to increase the bandwidth for the downlink in contactless reader systems. By use of an additional transmission antenna the negative effects of the resonant circuit are eliminated. The reader antenna (with a high quality factor Q) is used to transfer power and a second antenna (low quality factor Q) is used for data transmission. Furthermore, this antenna can also be used as pick-up coil for the reception of the load-modulated carrier signal (as described in the patent application [53]).

3. This invention disclosure [50] presents a coding and modulation concept for data communication from the *Proximity Integrated Circuit Card* (PICC) to the *Proximity Coupling Device* (PCD), which increases the uplink data rates in relation to the standardized methods by the factor 16. Data rates above 848 kbit/s are not standardized for contactless applications and so there are no coding or modulation schemes concerning these very high data rates. The invention disclosure shows a simple and effective method by which a two-stage load modulation process for the uplink is reduced to a single load modulation (ASK) of the carrier signal, i.e. no subcarrier signal is used and the carrier is modulated by the baseband data. If the NRZ coded data stream has a data rate of 13.56 Mbit/s, the uplink also has this value. The significant advantage to the M-PSK modulation, for example, is that for the PICC a lower clock rate resolution is already sufficient. The concept is described in the theoretical part of the thesis 4.2.4.2. Chapter 7.4.1 shows the associated simulation (Matlab and ModelSim) and measurement results.

4. This invention disclosure [52] establishes a non-coherent demodulator concept of a *Contactless Proximity Receiver* (PCD) which can handle different modulation and coding methods for *Very High Data Rates* (VHDR) as well as for standardized methods. The described demodulation process is realized by a special ADC I/Q sampling method on the carrier signal. The mixing process from HF to baseband and the sampling of the I/Q points are done by means of the ADC. The sampling process limits the frequency of the output signal like a lowpass filter. Consequently, no doubled frequency part occurs and thus, no analog or digital lowpass filter is necessary. With the adaptive sampling scheme, the demodulator already outputs the baseband modulated subcarrier. The proposed receiver architecture of a PCD is also very versatile concerning different communication standards (i.e. ISO/IEC 15693, ISO/IEC 14443, ISO/IEC 18000-3 Mode 1 and Mode 2). The concept is described in the theoretical part of the thesis 5.5.4. The architecture of the implemented demodulator is shown in chapter 6.5.1.

5. This invention disclosure [51] is an extension and refinement of the invention disclosure [52] which was described in the previous clause. Thereby, the I/Q demodulator is based on a non-coherent demodulation method, i.e. the beginning of the carrier can vary and, consequently, the sampling points are not in phase with the carrier frequency. The demodulator within this invention disclosure includes a sampler (ADC) and, in addition, a trigger unit. This unit detects a zero crossing or an extreme value (amplitude) of the carrier signal and provides a trigger signal to the sampler. The carrier signal is sampled by the sampler with a predefined phase shift concerning the detected zero crossing or the detected extreme value. With the ability to adjust the phase shift to a predefined value, the sampling points can be tuned to a fixed sampling grid to obtain an optimum sampling result. This demodulation concept can be seen as a coherent demodulation process, because the sampling clock is now synchronous to the carrier clock. The proposed method with an adjustable sampling scheme simplifies the post processing unit which was required in the previous invention disclosure. This demodulation concept was not implemented in the present PhD thesis.

Key Facts

The elaborated communication concept was the key to the significant increase of the uplink data rate. This uplink communication concept is a simple and effective method in which the two-stage load modulation process is reduced to a single load modulation (ASK) of the carrier signal, i.e. no subcarrier is used for the uplink communication [50]. The carrier signal is modulated directly by the NRZ coded baseband data and if the NRZ coded data stream has a data rate of 13.56 Mbit/s also the uplink has this value. In combination with the antenna concept [53] a transmission data rate up to 13.56 Mbit/sec for the uplink was reached. This concept eliminates the influence of the quality factor Q of the antenna resonant circuit which affects the transmission behavior and, consequently, the maximum achievable data rate. (Chapter 4.2.4)

For processing very high data rates on the reader side, a receiving unit was elaborated and implemented. An essential concept criterion was the design of a very flexible and energy-efficient digital receiver unit, which is essential for portable battery-powered devices like mobile phones. The flexibility of the receiving unit was reached by transfering the entire signal processing and the associated demodulation of the received signal exclusively to the digital domain. The digital demodulation, on the one hand, is based on an algorithm developed within the framework of this thesis and, on the other hand, on the undersampling. Obviously, this sampling method violates the rules of the Nyquist-Shannon sampling theorem; however, the procedure can be applied on deliberately to process the input signal. The non-coherent demodulation process was realized by a special ADC I/Q sampling method on the carrier signal. The mixing process (digital down-conversion) of the received HF signals (from passband to baseband) as well as the sampling of the I/Q points are done by the ADC without any analog mixer [52], [51].(Chapter 5.5)

In the previous paragraph the mixing as well as the sampling process based on an ADC were mentioned. To obtain the baseband data, the receiving concept required a further decimation step with an adequate algorithm for signal post processing. Therefore, this algorithm and the associated hardware architecture were developed and implemented within the framework of this thesis. (Chapter 6.5.2 and 6.5.1)

One of the main tasks was the design and development of a contactless prototyping reader system for HF RFID applications, with the primary goal to support a higher data throughput within reduced transmission time. For the exploration of very high data rates, the contactless reader was realized by means of an FPGA-based prototyping and evaluation board. The concept of the prototyping reader is based on a *Software Defined Radio* (SDR) system and this technology ensures a high level of flexibility as regards the implementation of different modulation and encoding methods. The main advantage of such an SDR system is the nature of signal processing, which can be carried out almost entirely in the digital domain. Among other things, the hardware design comprises the VHDL modules for the transmission- and reception path. These also includes the architecture for the undersampling process (down-conversion) and the algorithms for further signal processing. Before the implementation of VHDL, the methods and algorithms were implemented and verified in Matlab. (Chapter 6)

For the improvement of the signal quality of the received signal, an adaptive regulation was implemented which is based on *Least Mean Squares* (LMS) algorithm. The detected signal on the reader side is significantly smaller than the carrier signal and the ratio of the carrier signal to the received signal (load modulation amplitude) amounts to 80dB. To optimize the signal quality of the received signal, a carrier cancellation is deployed. The resulting carrier cancellation leads to a definite improvement of the receiving characteristic and is realized by an adaptive filter technique. This technique is characterized by the fact that the transfer function can be modified during the operation and the adaptation of the filter coefficients is done by an adaptation algorithm. (Chapter 6.6)

A method for the characterization and evaluation of the received load-modulated signal for very high data rates was worked out. The measurement method of the uplink signal is based on signal vector analysis i.e. *Modulation Error Ratio* (MER) and *Error Vector Magnitude* (EVM). The analysis/evaluation software was written by the tool Matlab and the input vectors for the scripts were directly measured by the ADC in the contactless prototyping reader system. It is planned to use this elaborated method as a standard measurement proposal (recommendation) for proximity coupled systems which are defined in the ISO standardization. (Chapter 7.3.2)

An increased data throughput for the uplink demands higher data rates as well as a compact and efficient data framing. Therefore, a possible character as well as frame format was elaborated. The occurrence of long phases without any change in the load modulation is also an important issue. Two appropriate methods to prevent those long phases were introduced. One of them is the line code 4B5B. Another appropriate method to force a change in the current load modulation state is bit stuffing. As far as contactless proximity coupling systems are concerned, the principle of bit stuffing was extended to symbol stuffing which was elaborated and published in the invention disclosure [50]. (Chapter 4.3)

Performance Comparison

There are several research activities on very high data rates for contactless proximity coupled systems. Some journal papers, articles and diploma theses were found in the course of literature research (see chapter 5.3). The literature discusses topics relevant to very high data rates like transmission concepts or contactless reader architectures (prototyping systems). This section gives a performance comparison with another proximity coupled prototyping system which also supports very high data rates (see table 8.1). Missing information within the journal papers, articles and diploma theses are indicated by a hyphen '—' in the table 8.1.

1. **Ph. Oberstaller**

   An already existing conventional contactless proximity reader was extended by a separate receive path (FPGA, ARM and an additional analog front end) which process very high data rates for the uplink (master thesis of Ph. Oberstaller [75]). The architecture of the receive path corresponds to a modified Low IF mixer, i.e. the demodulation is realized by a two-stage demodulation process. The RF carrier signal is down-converted to the intermediate frequency (respective subcarrier frequency) by an analog I/Q demodulator. After filtering, amplifying and discretization, the further frequency down-conversion to the baseband is accomplished in the digital domain. The demonstration reader supports data rates up to 3.39 Mbit/sec for the uplink which is four times higher than the currently standardized maximum data rate. Due to the fixed analog components it is not possible to increase the data rates above the mentioned value. A relevant drawback of the demonstration system is that the reader can only receive VHDR but is not able to send them.

2. **D. Kusternigg**

   Continuous and constructive work related to the previous thesis (Oberstaller [75]) was done in the master thesis of D. Kusternigg [60]. The main objective was to improve the stability of an already existing demonstration reader system, especially the optimization of the decoder unit. Instead of the comparators, two ADCs were used for digitalization and the filter design was adjusted to a higher frequency range. With the improved demonstration reader, the achievable data rate was restricted to maximum 6.78 Mbit/sec, which is 8 times higher than the currently standardized maximum data rate. The main disadvantage of this demonstration system, again, is the fact that the reader can only receive VHDR but is not able to send them.

3. **NXP**

   The fact that there are several journals and conference papers on this topic shows that other companies like NXP Semiconductors have also been working on the same topic. Witschnig et al. [37], Rinner et al. [21] and Patauner et al. [18] show an implementation of a high speed RFID lab-scale prototype with a transmission rate up to 6.78 Mbit/sec for both communication directions. The mentioned papers only show a block diagram of the transmit path of the lab-scale prototyping reader which is realized by an FPGA platform, a DA converter and an RF front end. For the transponder also an FPGA is used and, in addition, the demodulation is realized by an analog I/Q demodulator. But no detailed information concerning the implemented hardware concept/architecture of the lab-scale prototyping reader is given. The received path consists of a narrow band stop filter (for

carrier suppression), an ADC and an FPGA for further signal post processing. Again, the upper limit of the uplink communication speed is 6.78 Mbit/sec.

4. **Angerer**

   The rapid prototyping reader system by Angerer et al. [4], [5], [6] is not able to support very high data rates. Nevertheless, this system is mentioned here, because of its very flexible and modular concept. It is a dual frequency reader (for HF and UHF application) which supports various product standards like EPCGlobal HF Ver. 2, the EPC RFID Class-1 Gen-2 UHF standard and the ISO/IEC 15693 standard. The testbed setup was realized by a rapid prototyping system which comprises a DSP, an FPAG, ADC, DAC and a RF front end for HF and UHF.

8.2 Outlook

The topic of very high data rates in passive contactless proximity coupled applications has turned into a popular field of research lately, which working groups of the ISO have also been dealing with. Other semiconductor and chip-card manufacturers like NXP or Gemalto have also been working on this topic for quite some time. An important aspect of very high data rates is the correct choice of the implemented coding and modulation method. In this respect, there are different approaches and the main objective is to find a common solution for the standardization of very high bit rates. Very high data rates in proximity coupled systems require additional research activities and work on the transponder side as well as on the reader side. Within the framework of the PhD thesis, no silicon was produced, but this had already been decided before the project began. However, several feasibility studies were executed and also a lot of preparatory work was accomplished, e.g. various ideas concerning hardware concepts, transmission methods and algorithms for demodulation and signal processing on the reader side. An ISO contribution concerning very high data rates in contactless proximity coupled systems was submitted by Infineon Technologies Graz, which was also accepted by the ISO. The mentioned contribution, among other things, describes a modulation and coding method which enables a data rate of 6.78 Mbit/sec for the uplink (card-to-reader communication). Consequently, the performance gain concerning the data rate is eight times higher than the currently standardized maximum data rate of 848 kbit/sec (ISO/IEC 14443). The team members of the ReadRF project were also involved in the preliminary work for the ISO contribution.

	This Work	1.) Oberstaller	2.) Kusternigg	3.) NXP	4.) Angerer
Max. Uplink Data Rate [Mbit/sec]	13.56	3.39	6.78	6.78	—
Hardware Concept	SDR (FPGA, μC)	FPGA, ARM	FPGA, ARM	FPGA	FPGA, DSP
Supported Standards	ISO/IEC 14443	ISO/IEC 14443	ISO/IEC 14443	—	EPC-Global(HF,UHF), ISO/IEC 15693
Extension to Other Standards	Low effort	High effort	High effort	—	Low effort
Protocol Handling	μC	ARM	ARM	—	DSP
Extension to VHBR	Low effort	High effort	High effort	—	—
Modulator	Digital I/Q	Conventional Reader IC	Conventional Reader IC	—	Digital (DAC)
Demodulator and Signal Post Processing	ADC based I/Q mixing	Modified Low IF mixer	Modified Low IF mixer	Band-Stop Filter, ADC	Analog RF Front End,ADC
Interface to the Terminal	RS232, Ethernet	RS232,Ethernet, USB	RS232,Ethernet, USB	—	Ethernet

Table 8.1: Performance Comparison

A Module Specification of the Reader

Top-Level and CPU I/O Module

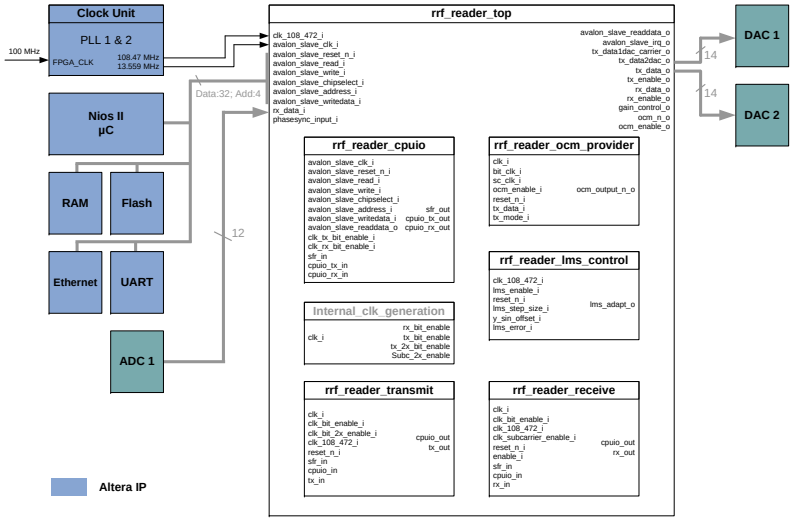


Figure A.1: Top-Level architecture with additional components

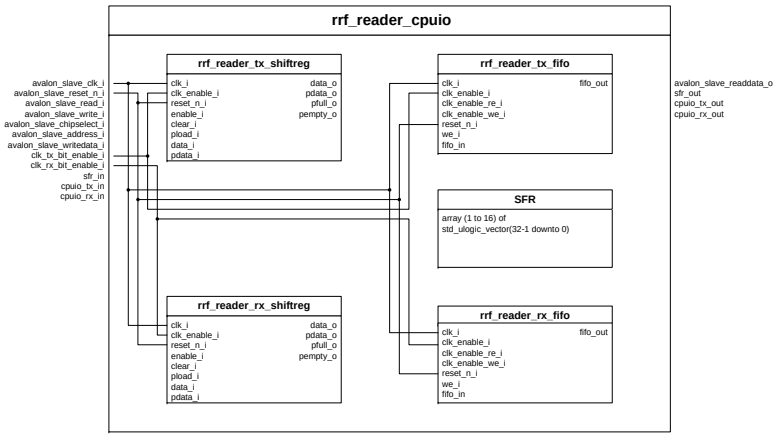


Figure A.2: CPU I/O Module Architecture

Transmit and Receive Module

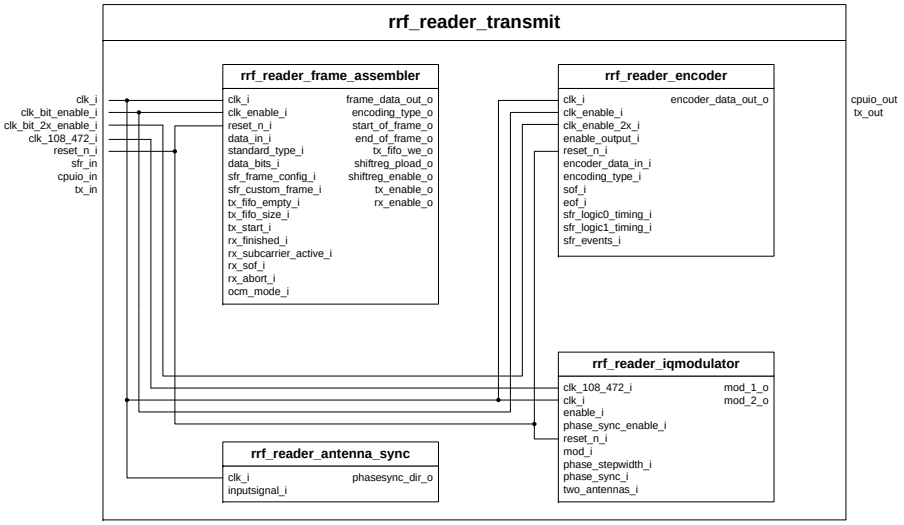


Figure A.3: Transmit Module Architecture

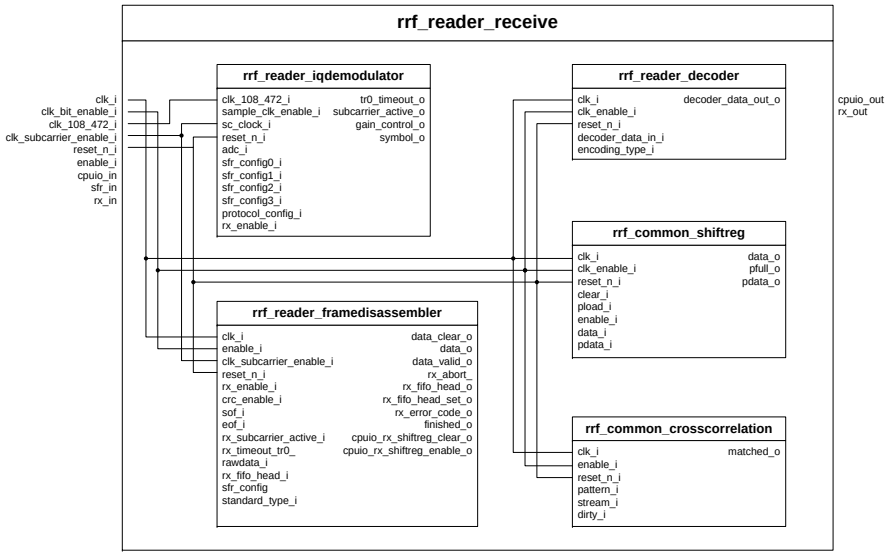


Figure A.4: Receive Module Architecture

Schematic of all Modules and Pins of the Design

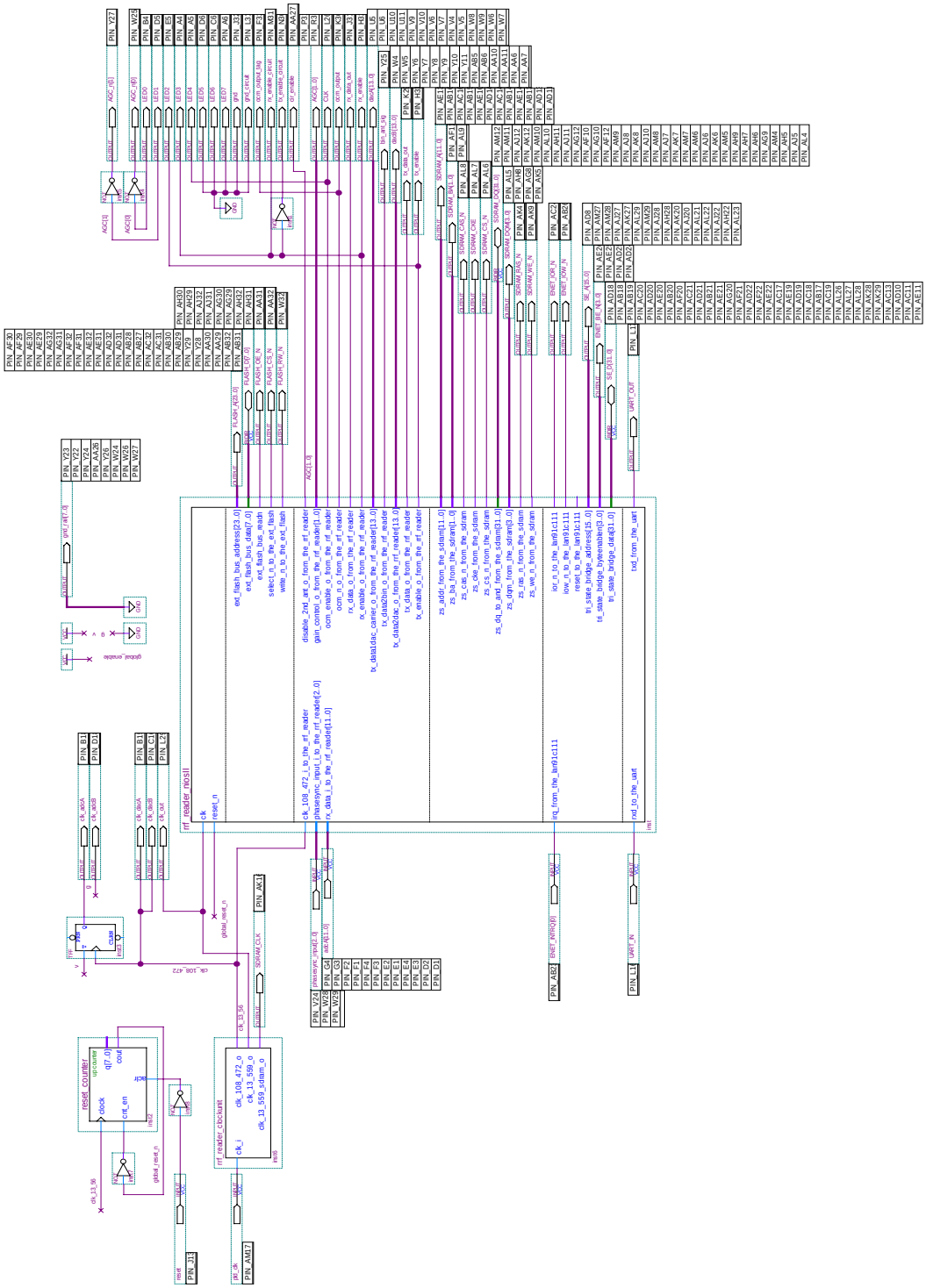


Figure A.5: Schematic of all modules and pins of the entire design

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Papers

- Markus Auer, Edmund Ehrlich, Albert Missoni, Walter Kargl, Gerald Holweg and Wolfgang Pribyl. *Design and development of a mixed signal prototyping system to achieve very high data rates for contactless applications*, e&i Journal (Elektrotechnik & Informationstechnik), Analog & Mixed Signal-Schaltungen und -Systeme, 4/2008
- Markus Auer, Edmund Ehrlich, Albert Missoni, Walter Kargl, Gerald Holweg and Wolfgang Pribyl. *Analoge Eingangsstufe mit ADC-basierendem Demodulator für HF-Transponder zur Verarbeitung hoher Datenraten*, e&i Journal (Elektrotechnik & Informationstechnik), Analog & Mixed Signal-Schaltkreise, 11/2009
- Markus Auer, Edmund Ehrlich, Albert Missoni, Walter Kargl and Wolfgang Pribyl. *Design und Entwicklung eines Mixed Signal Prototyping System für RFID Applikationen mit Datenraten größer 848kbit/s*, Austrochip 2009, 17th Austrian Workshop on Microelectronics, Graz, Austria

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Invention Disclosures and Patent Applications

- Walter Kargl, Edmund Ehrlich and Matthias Emsenhuber. *Contactless Data Reception*. United States Patent Application Publication, 2010. Pub. No.: US 2010/0243737 A1.
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- Walter Kargl and Edmund Ehrlich. *Demodulator and Method for Demodulating a Modulated Carrier Signal*. Invention Disclosure, 2010. Reference No.: IO100401PUS.
- Walter Kargl and Edmund Ehrlich. *Demodulator and Method for Demodulating a Carrier Signal*. Invention Disclosure, 2010. Reference No.: IO100402PUS.

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- Matthias Emsenhuber. Development of an analog frontend for an RFID reader for high datarate. Diploma thesis, Graz, University of Technology, Institute of Electronics, 2008
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