System Evaluation and Development of an Evaluation Reader for 13.56 MHz RFID Systems Providing Very High Data Rates up to 13.56 Mbit/s

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We can't solve problems by using the same kind of thinking we used when we created them.

[Albert Einstein]

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Abstract

This thesis deals with the increase of the available data rates of 13.56 MHz proximity coupling radio frequency identification (RFID) devices. Applications like passports have to deal with increasing amounts of data stored on the device by reducing the transaction time at read points, such as gates at the airport. Those devices are passive and have to be powered by the emitted H-field of the reader which is also used to transmit data. Due to the physical settings of the RFID system the transmit channel is bandwidth limited which has to be taken into account when increasing the data rate from 848 kbit/s to a maximum of 13.56 Mbit/s. Increasing the data rate by a factor of up to 16 requires the analysis of the currently used as well as new modulation schemes. The introduction of a new modulation scheme will also result in hardware modifications on the system to enable a stable communication.

This thesis is separated into 10 chapters starting with a general discussion of RFID systems. After the introduction, the specific components of the system, which are reader and transponder, are defined and mathematically described. This description is applied to a simulation model of an exemplary RFID system. The simulation model is used to analyze the interaction of system parameters such as, coupling factor or current consumption.

The characterization results of the model define the frame work of very high data rates for both communication directions. To achieve very high data rates the focus has to be set on two points. On the one hand the provided bandwidth of the hardware has to be increased and on the other hand a new modulation scheme has to be found which is more bandwidth efficient.

The communication direction from reader to transponder currently uses amplitude shift keying (ASK). To guarantee a stable communication and transmit sufficient power to the transponder alternative modulations like multi level ASK or phase shift keying (PSK) are discussed. All selected modulation schemes are evaluated in terms of bandwidth requirement and energy transmission to find the most suitable one. For the PSK modulation scheme it will be shown that the modulation of a segment guarantees the power transmission and fulfills spectral requirements.

The data transmission from transponder to reader is a passive communication. Due to the limited energy available on the transponder it is done by so called load modulation. For passive load modulation the transponder changes its impedance by switching a modulation resistor in dependency of the data. Utilizing this modulation scheme, different alphabets of patterns are defined which guarantee the supply of the transponder during the modulation. These alphabets of patterns are introduced and compared in different perspectives such as power spectral density or energy stability.

From those theoretical cognitions a hardware specification is derived, which was used to implement an evaluation reader. This evaluation reader receive path is based on the concept of software defined radio and the reader transmitter is able to transmit all new specified data rates as well as data rates of the existing standard. This product-like demonstration was already presented several times with great success to allow a direct comparison in reality with the actual standardized data rates and the investigated novel transmission scheme.

Due to a very flexible structure of the hardware, the evaluation reader can be used to test other standards as well, which enables a much wider field of applications.

Kurzfassung

Die vorliegende Doktorarbeit beschäftigt sich mit der Datenratenerhöhung passiver 13,56 MHz RFID Systeme. Anwendungen wie der elektronische Reisepass, müssen mit immer größer werdenden Datenmengen im Speicher fertig werden, während die Kommunikationszeit verkürzt werden soll. Diese Systeme sind meist passiv ausgelegt und beziehen ihre Energie aus dem emittierten H-Feld, welches auch zur Datenübertragung genutzt wird. Durch die physikalischen Gegebenheiten von RFID Systemen ist die Bandbreite des Übertragungskanals begrenzt, was bei der Erhöhung der Datenrate von aktuell 848 kbit/s auf bis zu 13.56 Mbit/s berücksichtigt werden muss. Diese Erhöhung der Datenrate um den Faktor 16 verlangt neue Modulationsarten sowie eine Anpassung der Hardware um eine stabile Kommunikation zu gewährleisten.
Die Arbeit ist in 10 Kapitel aufgeteilt, beginnend mit einer generellen Einführung in RFID Systeme. Die einzelnen Teile des RFID Systems, wie der Reader oder Transponder, werden vorgestellt und mathematisch beschrieben. Mithilfe dieser mathematischen Beschreibung wurde ein Simulationsmodell generiert. Dieses Modell wird genutzt um Interaktionen zwischen Parametern, wie den Koppelfaktor oder die Stromaufnahme, zu simulieren.
Die Simulationsergebnisse definieren die Rahmenbedingungen zur Einführung sehr hoher Datenraten für beide Kommunikationsrichtungen. Um die Erhöhung der Datenraten zu erreichen muss der Fokus auf zwei Hauptpunkte gelegt werden: Zum einen muss die Bandbreite der Hardware vergrößert werden, zum anderen muss eine Modulationsart gefunden werden, die sehr bandbreiteneffizient arbeitet.
Für die Kommunikation vom Reader zur Karte wird aktuell Amplitudenmodulation (ASK) verwendet. Um eine stabile Kommunikation zu gewährleisten und genügend Energie zu übertragen, werden alternative Modulationsschemen überlegt, wie mehrstufige ASK oder Phasenmodulation (PSK). Die ausgewählten Modulationsarten werden bezüglich ihres Bandbreitenbedarfs und der Energieübertragungseigenschaften bewertet um die geeignetste Modulationsart zu finden.
Die Datenübertragung vom Transponder zum Reader erfolgt durch die sogenannte Lastmodulation. Dabei ändert der Transponder seine Impedanz durch Schalten eines Modulationswiderstandes in Abhängigkeit der zu übertagenden Daten. Basierend auf dieser speziellen Übertragungsart werden Voraussetzungen für ein Symbolalphabet definiert, die genügend Energie während der Modulation garantieren.
Anforderungen an die Hardware werden von diesen theoretischen Überlegungen abgeleitet, welche zur Entwicklung eines Demo-Readers führen. Dieser Reader basiert auf dem Konzept des Software Defined Radios und ist in der Lage alle neu definierten Datenraten, sowie die Datenformate aktuell definierter Standards zu senden. Dieser produktnahe Demonstrator ist bereits mehrfach erfolgreich bei live Vorführungen eingesetzt worden.
Durch den flexiblen Aufbau der Hardware kann der Reader für Tests anderer Standards herangezogen werden, was den Einsatzbereich bedeutend erweitert.

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1. Introduction

A few years ago, very few people knew what **R**adio **F**requency **ID**entification, or **RFID** [1] for short, is about. RFID involves the identification of individuals, animals, tools or any products, with the help of radio waves. In the recent years, more and more RFID solutions have appeared and people are now familiar with this term. What does it mean? What is it about? Is it dangerous? Today, nearly everyone knows what RFID means, or at least already had contact with this technology. Just think of buying a pair of trousers or some perfume, where a tag is fixed on the product, which will trigger an alarm in case the item is illegally removed. Those are very simple RFID applications, called EAS (Electronic Article Surveillance) [2]. More critical applications are tickets for the public transportation, passports and the health insurance card [3].
In everyday life we have contact with RFID solutions. But to get an idea of the RFID system itself, the historic development can not be neglected, and so the first chapter will sum up the main inventions which led to today's RFID systems.

1.1. Historical Development

RFID systems have a very long history. The roots can be found in 1935, when Alexander Watson-Watt invented the radar [4]. He showed that it is possible to locate physical objects with the help of radio waves. Based on the finding that objects reflect radio waves, he was able to locate them at large distances. Depending on the geometry and the material, the so called echo is different, and so it is possible to distinguish between different objects. This technology was improved and led to one of the most important inventions of World War II, when countries started to detect planes and ships at very large distance with this principle. This was a huge benefit for the military, but they had the problem of distinguishing between own and enemy planes. The Germans found out that the signal which is reflected to the base station changed if the pilots rolled their planes. With this very crude method, the radar crew could identify friendly planes. That way the Germans used the first passive RFID solution to identify planes in a passive way, just by changing the reflection [5].
The British army improved this solution by adding passive transponders on their planes, which reflected the radar waves. Those transponders were tuned to the home radar frequency and so the planes appeared much brighter on the screen than enemy planes. This system was called IFF (Identification Friend or Foe) [6].
The first RFID related publication was in 1948 by Stockman. He described a communication system with radio frequency in his paper [7], where he replaced the transmitter with a modulated reflector.
In the 1960s the interest on RFID grew continuously. The first RFID transponder was patented by Richardson in 1963. His transponder was able to extract the energy of the field and to rectify it to power any on board electronics. The next patent was in 1967 by Vinding, who invented a

simple and cheap transponder, which communicated with a host by loading the antenna circuit. In 1975, effective ways for backscatter modulation were found. And in the late 1960s, the first EAS systems were developed which led to the breakthrough into commercial areas in the 1980s and 1990s. The interest and the applications grew continuously and different commercial areas used RFID components [6].
With the introduction of RFID systems into everyday life, many new applications appeared. The first commercial usage was EAS in the 1980s. In the beginning of this technology the focus was only on identifying if an object was present or not, via the transmission of simple serial numbers, but it has evolved to active communication today. The increase of commercial usage led to the need for different standards. A standardized communication increases the robustness in the data exchanges and guarantees that the communication of systems with the same frequency will not influence each other. Most international standards were managed by the International Standardization Organization (ISO) and International Electrotechnical Commission (IEC). An overview of different RFID standards and their typical applications will be summarized in Section 1.4.
The usage of RFID systems in commercial areas grew continuously in the last ten years. Nowadays RFID tags can be found in all areas of life. Examples are the EAS systems in shops, smart cards for tickets for the public transport, animal tracking, and logistic applications. There are few restrictions with this technique, and with this large growth, the requirements for RFID applications changed as well. Depending on the application, different data rates are needed. EAS systems require limited data to be transmitted, thus low data rates are sufficient. Fare collection transmits more data which leads to higher data rates. This enables a fast transaction time and therefore a low waiting time at the ticket counter.
The base data rate is 106 kbit/s. With the increasing amount of data, which has to be transmitted, the need of a higher data rate is inescapable, which prompted the introduction of data rates up to 848 kbit/s. For most applications these higher data rates were sufficient to keep the transaction time low. With the introduction of ePassports a large field of research was opened again. The first version of the ePassport stored the personal data as well as a picture on the chip, which was used for verification at the boarders and airports. With the enlargement of the passport through the tracking of fingerprints, the transmitted data increased again.
The health card [3, 8] is another example. At the moment, there is only personal data stored on the card, but there are ideas to enhance the storage and to save further data, such as pictures, reports or allergies on the card. If this should be done, the memory size, as well as the transmission rate has to be increased. With the desire to keep the transaction time low, and to increase the amount of data the transmission rate has to be increased significantly, while a stable communication has to be guaranteed.
In the following section the general idea and function of RFID systems will be introduced. Different standards will then be listed and the requirements for Very High Data (VHD) rates are presented.

1.2. Overview of RFID Systems

There are a huge number of different RFID systems available on the market. Even if the systems differ in many aspects, the basic principle of RFID systems is always the same and depicted in Figure 1.1. Depending on the application and the frequency, the systems have different require-

ments and specifications, but the basic structure stays similar.
An application is attached to a reader, which interacts with the transponder over the air interface. The reader emits an electromagnetic field with a specified frequency and field strength. This field is used for data transmission from the reader to the card, to extract the clock, and also to power the transponder. There is a difference between passive and active transponders. Active transponders often have a sensor attached to observe parameters in their surrounding, and are supplied by a battery. In this case the carrier field is only used for the communication and the clock extraction. The clock extraction is needed to derive an on board clock domain, and to ensure frequency synchronicity between the reader and the transponder.
If a passive transponder is used, the transponder does not have a battery and has to be supplied by the field. Therefore the transponder has a certain quality factor to boost the received energy.
The system is based on the master slave principle, and so the transponder has to wait until the master (reader) sends the commands and the transponder reacts. Depending on the antenna and the energy, the range of the system is defined. The transponder itself can vary a lot. For simple applications, the transponder just sends its identification (ID) without any encoding. For more critical applications the communication is encoded and so the risk of unauthorized listening is reduced.
This chapter will give an overview of different applications, a more detailed description of the components can be found in Chapter 3.

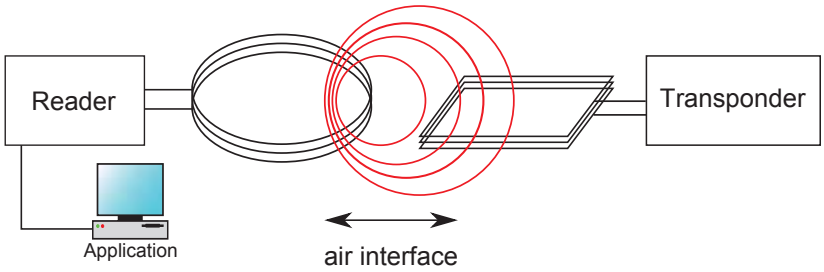


Figure 1.1.: Principle of an RFID Application

1.3. Possible Applications

The range of possible applications covers a wide area and is only summarized here.
Public transport
In some big cities, such as London, Moscow, Warsaw, and many cities in China, RFID transponders are used for tickets in the public transport system. In 2008 more than 3 billion transponders for transportation where circulating [9]. For the public transport in Dhaka it is proposed to use RFID tickets as well, and to potentially place an RFID tag on the bus to display information for the passengers on screens [10].
Car access immobilizer
This category combines everything which is related to cars, such as keyless entry, tire pressure sensor and immobilizer. The requirement for those products is a very robust design often operating with different frequencies, from low frequency (LF) to ultra high frequencies (UHF), and as well active or passive [9].

Animal tracking
Animal tracking describes the identification and tracking of animals from their birth to slaughter. The advantages are that only healthy animals come to slaughter and the animals can be tracked, and so it is harder to steal them. The largest benefit is for the individual treatment of the animals with medicine and food and should be a seal of quality [11]. Furthermore, animal tracking is also used to identify valuable breeding animals.

Pharmacy market
The benefits of RFID tags on medicinal products are tracking as well as protection from counterfeiting. All products have an ID, and with the help of a database it is possible to control the product at all points, from the production to the use. With the unique ID, it is possible to define the actual placement of a product, to allow tracking of the whole life cycle of the product and to guaranteeing the right storage of the product [9]. If a sensor, for example for temperature, is attached to the RFID tag, it is also possible to monitor the cold chain during transportation.

Fashion
Fashion is the ideal environment for RFID tags. The shop entrance areas are clearly defined and so they are ideal for gate antennas. Since the percentage of the tag costs, compared to the product costs, is very low, the tag can be used for identification, EAS and counterfeit protection. Furthermore, the requirements for the tags are very low, since the lifetime is limited with the fast change of fashion trends [9].

Access control
In many companies RFID transponders are used for access control as well as time recording. With an individual ID it is possible to allow individual access to security relevant areas and equipment.

Libraries
In many libraries RFID tags are used to check in and out books and control the inventory without taking the books out of the shelf.

Healthcare
Many applications can be found in the area of healthcare. From access control and personal tracking of employees, to the product insurance and counterfeit detection. One part is patient identification [12], to ensure the right identification of the patient with RFID based wristbands. The health card is another big area of RFID used in the health care segment. Personal data as well as relevant patient data are stored on the card to allow emergency teams to identify patients and get relevant data [8]. Furthermore, an idea is to store radiographs on the healthcard as well.

eGovernment
The main focus of this work will be settled in the area of eGovernment to increase the speed of passport reading. Since an increasing number of countries claim for higher security, the International Civil Aviation Organization (ICAO) decided to make the ISO14443 a worldwide standard for ePassports [13].

Near field communication
Near field communication, NFC for short, is used to communicate over short distances, for example between two mobile phones, if they have an NFC interface, or load information from smart posters [14] on the phone. The introduction of NFC allows for more applications than pure RFID due to the fact that the user is able to be an active partner in the communication. For example, it is possible to pay in shops by confirming the transaction. Furthermore, the NFC device can be used for public transport, having the ticket stored on a phone, car parking, and many other applications mentioned before [15].

These are some of the possible applications, and every day new ideas are proposed which use RFID. Different applications have different requirements, and so an uncountable number of different antennas, sizes, field strengths, transponder voltages and so on are on the market. To be able to control all those inventions, standards and regulations have to be written and controlled, to prevent huge RFID disorder.

1.4. Relevant RFID Standards

Different standards are used to define the communication for different applications. A standard defines the working frequency, field strength, antenna size, kind of modulation, protocol and other relevant parameters. The applications can be separated with the help of the used carrier frequency f_c in low frequency (LF up to 135 kHz), high frequency (HF 13.56 MHz), ultra high frequency (UHF 860-960 MHz) and microwave (2.45 GHz). The focus of this thesis is the HF range. For the communication at 13.56 MHz different standards exist beside each other. Some of them complement each other, or can be seen in different frequency ranges, but then an additional ending is added, such as ISO/IEC 18000-x. The ending -2 stands for the LF standard, -3 for HF, -6 for UHF and -4 for microwave. Further standards, which also deal with the same frequency range are for example ISO/IEC 15693 [16], ISO/IEC 14443 [17] and ISO/IEC 18092 [18].
The most important standard for eGovernment is the ISO/IEC 14443 concerning the RFID passport, since ICAO decided [19] to make the ISO/IEC 14443 the base standard for passport applications. The standard is separated into different parts. Part 1 [20] contains the physical characteristics, such as antenna size, and is linked to other standards, which enhance the specification, such as ISO/IEC 10373-6 [21]. Part 2 [17] is the physical layer, which defines the physical part of the communication, such as timing, signal shapes and field strength. This part will be the basis for this thesis and is described in more detail after the overview of this standard. Part 3 [22] deals with the communication, how a frame looks like, the timing and the anti collision, while Part 4 [23] describes the transmission protocol itself.

1.4.1. ISO/IEC 14443 Part 2

Part 2 contains the physical parameters of the standard. Historically two different communication methods existed in parallel due to disagreements over the implementation of a single scheme. The problem was that two companies already had products on the market, with differing implementations, which led to a separation into Type A and Type B. For the communication from the reader (in the standard it is called PCD, which stands for Proximity Coupling Device) to transponder (or PICC what is the short form for Proximity Integrated Circuit Card or subject) two different modulation types are specified. Both types are based on ASK. Type A is a modified Miller code with 100 % ASK. This means that a symbol is represented by a certain pause time within the bit time. Depending where the pause is located, either a ”0” or ”1” is transmitted. Furthermore, a zero followed by a ”1” has no pause. The envelope of the signal is shown in Figure 1.2. Type B is a 10 % ASK with Non Return to Zero (NRZ) coding. Therefore the amplitude level is reduced by 10 % if a zero should be transmitted.

It can be seen, that Type B is rather simple. The problem with this coding is that the transponder has a limiter structure, which reduces the amplitude differences. To make sure that the signal is transmitted with a certain quality, the borders as well as the settling time of the signal and minimum and maximum reduction are defined very accurately in the standard.

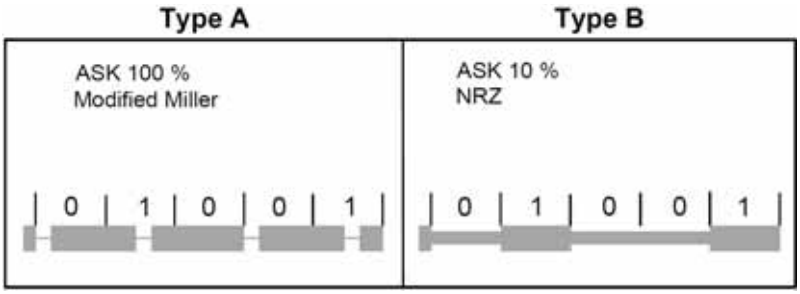


Figure 1.2.: Overview of base data rates for the communication PCD to PICC [17]

Type A encodes data with three possible symbols, depending on the last transmitted one. A “1” is represented by a pause in the second half of the bit time, while a “0” can either be a sequence without any pause if the “0” comes after a “1”, or has a pause at the beginning of the bit time if the “0” follows another “0”. To guarantee that the communication is stable, the signal shaping has to stay between certain borders, which defines the time when the signal has to reach a certain level (90 % or 5 %) and how much overshoot is allowed. This is valid for Type A as well as Type B for the basis data rate of 106 kbit/s.

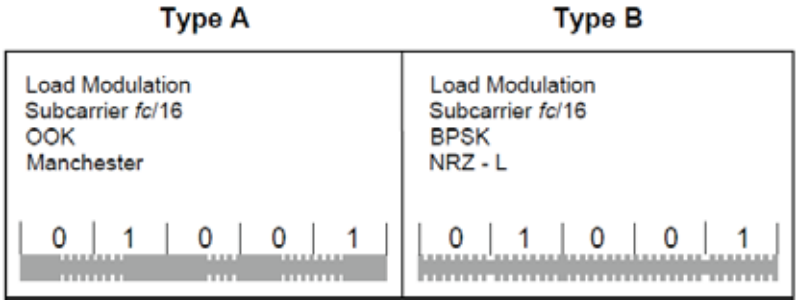


Figure 1.3.: Overview of basis data rates for the communication PICC to PCD [17]

The communication from PICC to PCD is done by load modulation. That means that the transponder changes its impedance according to the data with the help of a load modulator. The load modulator can either be a transistor, or a switch with a resistor which changes the impedance. This changes cause a change of the quality factor, thus it influences the field which can be detected by the reader. The principle of load modulation will be explained in more detail in Section 3.2.
For the communication from PICC to PCD, Type A uses a Manchester coded On-Off-Keying (OOK). This means that either the first half of a bit is modulated with a subcarrier of $f_c/16$ (847.5 kHz), which stands for a “1”, or the modulation is in the second half, which represents a “0”. This is only valid for the basis data rate of 106 kbit/s shown in Figure 1.3.
Type B is called a Binary Phase Shift Keying (BPSK) with a NRZ-L , where the bits are represented by a load modulator signal with $f_c/16$, and either the bit starts with the load modulator

turned on, which results in a logical “1”, or starts with no modulation which represents the “0”. That way a phase shift of the modulator signal of 180 degrees is achieved, which is used for the term BPSK.
For both communication directions higher data rates up to 848 kbit/s are defined. The coding stays the same in case of the communication from reader to card, with the difference that the symbol duration is reduced. By reducing the symbol duration, the bandwidth requirement is increased, and so the quality factor has a bigger impact on the signal. To be able to generate the signals, the envelope definition of the signals is changed, as can be seen in [17].
For the communication from PICC to PCD, the coding of Type B is enhanced to achieve 848 kbit/s. The symbol time is decreased and so fewer subcarrier periods are within the symbol duration. For the data rate of 848 kbit/s a single subcarrier period represents a symbol.

1.4.2. ISO/IEC 10373

The ISO/IEC standard 10373-6 describes the test methods for the standard ISO/IEC 14443. In this standard all measurements, requirements for the measurement equipment, and boundary conditions are listed. It is clearly defined how the transponders are tested in terms of electromagnetic discharge (ESD), at which location the test has to be carried out, and how the different antennas used for measurements are shaped. The ISO antenna radiates the field in a loop antenna with a diameter of 150 mm and two turns. One turn is connected to the source, while the second turn is open, used for electrical compensation. The anti Helmholtz coils are placed above and below the transmit antenna at a distance of 37.5 mm and are single loop antennas shaped rectangular with a dimension of 70 times 100 mm and round edges with a radius of 10 mm. Furthermore, all relevant circuits are described and the required electronic elements are listed. Annex A of this standard describes all relevant parts in more detail. In all experimental results presented in this thesis, the ISO PCD1 antenna is used as reference. This antenna has a matching circuit which tunes the antenna to a quality factor of 35. The ICO PCD2 antenna is also defined, and distinguishes only the components of the matching network and has a quality factor of 8, but will not be used in this thesis for measurements. According to the standard, the PCD1 antenna is used to characterize systems with a data rate of 106 kbit/s, while the PCD2 antenna is used to characterize data rates from 212 up to 848 kbit/s. Since most reader products have a high quality factor, all experiments will be performed with the PCD1 antenna, as long as it is not marked additionally.

1.5. Relevant RFID Regulations

Standards are product related, while regulations are valid generally in a certain area, in this case in the European Union (EU). Two different concepts have to be separated. On the one hand, regulations define the levels and parameters, on the other hand, test methods describe how those parameters are defined and measured. The most important regulation with respect to RFID is ERC/REC 70-03 [24], where the radiation limits, what energy the reader is allowed to radiate, and the spectral mask, at which frequency the reader is allowed to radiate a certain field strength, are defined. The test methods, for these parameters are defined in ETSI EN 300 300-1

which can be found in [25]. With both documents [24] and [25], all required parameters can be defined and measured. Figure 1.4 shows the spectral mask [24, 25]. The spectral mask defines the allowed emission at a specific carrier frequency. It can be seen that the allowed emission at the carrier frequency is +60 dBµA/m for 13.56 MHz systems. For the range of $f_c \pm 150$ kHz a

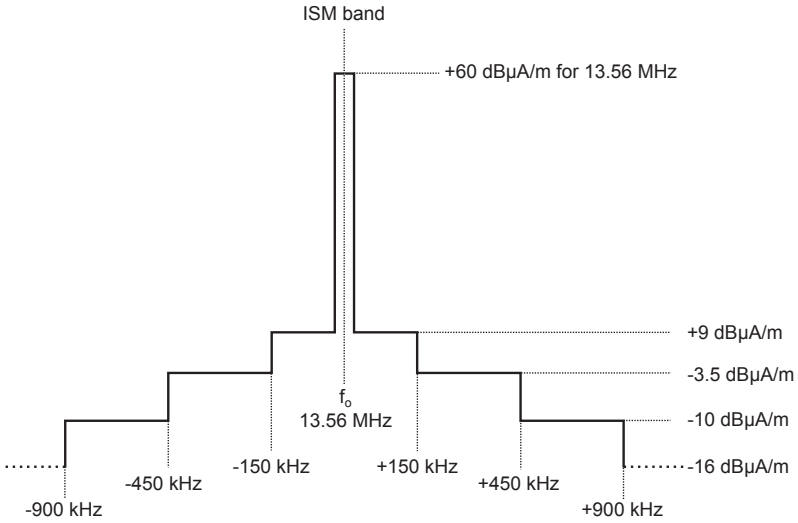


Figure 1.4.: Spectral mask for short range devices [25]

limit of +9 dBµA/m is defined, and it can be seen, that the allowed emissions are reduced with increasing bandwidth. At the moment, only the reader has to fulfill the spectral mask as an active device. The transponder as passive device does not have concerns regarding the spectral mask, since it is not an active transmitter. It is under discussion at the moment whether to enhance the measurements of the reader with an attached transponder, since the emissions change due to detuning and other influences. It might be possible that the reader does not fulfill the mask as soon as a transponder is moved inside the generated field of the reader.
For the development of very high data rates this mask is a limitation. Due to the higher transmission rate, the spectral components of the signal increases. Therefore, it is a goal for the development of a very high data rate communication system not to violate this spectral mask definition. Different findings will be presented in Section 5.1.

1.6. Future Trends

It is impossible to say how the future of RFID, smartcard or NFC will look. The problem is that there are many changes ongoing, and so the only trend which can be seen is that all kinds of RFID solutions are gaining more and more influence over everyday life, and they are getting more popular on the market. Starting at the health card, every Austrian owns, going to ePassports, and ending at access control of companies, sport areas or transportation, everybody gets in contact with this technology. Many things make life easier, for example the access control based on RFID. It is easier to allow certain people access to confidential areas, just by enabling access within a computer program. Another big advantage is the flexibility of RFID systems. If a key-card gets

lost or stolen, the only thing which has to be done is to erase the ID in the system, and the key is useless. Using physical keys, the whole locking system has to be changed and the keys of other persons as well.
Not only is the identification purpose a big market, with the introduction of NFC, a communication based on the RFID technology is possible and so the pure identification is shifted to more communication. With the use as an interface, the need of higher data rates is inescapable in order to be competitive with other interfaces, such as Bluetooth, with actual enhanced data rate of 2.1 Mbit/s (Bluetooth 2.1 + Enhanced Data Rate) [26].
A huge market can be reached if the transponders are used on products and replace the Barcode. Nowadays most products have Barcodes to be read, when they are delivered to the market, as well as when the customer pays at the checkout. The disadvantage is, if the label is dirty, creased or partly covered, the barcode cannot be read. The benefit of RFID is that no line of sight has to be guaranteed to read the code, which allows placing the transponder within the package, where it is protected from outer influences. Many products can be read at once if the tags support anti collision methods. Furthermore the orientation of the product is not critical, and additional information could be added, such as the expiration date. Even if there are many benefits, there is one mayor drawback: the cost. A transponder costs around 10 times more than a simple barcode sticker [27], and so it will be hard to replace it, unless further functionalities are needed. One way would be to store the expiration date, to guarantee the customer does not pay for products which are out of date, or attach sensors, to ensure the cold chain. Besides all the benefits and drawbacks, the infrastructure for barcodes is well established, and so it is hard to replace it, since it will take a lot of time as well as money.
To get an idea of possible RFID applications, it is enough to „Google“ it and some interesting topics are listed. Just as example, a disco in Rotterdam, the „Baja Beach Club“ who implants some volunteers an RFID chip in their upper arms [28]. Those chips contain all personal data, which are needed for payment. Those people can use an own gate at the entrance, where the transponders are read. Moreover they can pay for their drinks with the chip, and charge their bank account directly. With the transponder those guests do not need any hard cash. At the same time some people like the idea, other are strictly against it. This trend shows the possibilities of RFID technology, and also the power for further applications, which might have the potential to divide the society.

1.7. Benefit of Enhanced Data Rates and Goals of the Doctoral Thesis

Independent of the application, this doctoral thesis shows the feasibility of enhanced data rates for RFID systems. The actual standardized data rates up to 848 kbit/s are enough for basic applications. For more advanced applications it is important to increase the data rate to reduce the transmission time. While more data will be stored on ePassports, health cards, and similar products, it is necessary to keep the transaction time low. Especially at airports, an increase of the transmission time would result in long waiting times. New applications based on mobile phones require higher data rates as well to reduce the transaction time. It should soon be possible to download traffic information and subway plans to a mobile phone using RFID based technology.

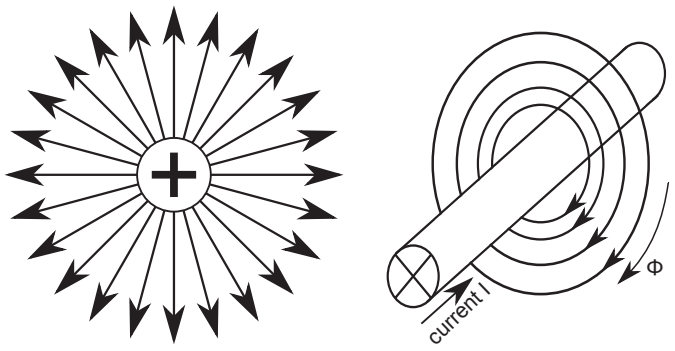
For these applications it is especially important to keep the transaction time low because it will increase the Quality of Experience [29] of users.
This work on the one hand focuses on the system simulation to show the influence of different parameters on the whole system, and on the other hand on the development of an evaluation reader to test the findings. The problem is that all parts interact with each other, and so a change of a single parameter can lead to a complete different behavior. To understand the relation between different parameters on the system, a detailed system simulation should be performed to outline different effects. Based on those findings the system should be understood and different requirements will be defined. Based on specified requirements an evaluation reader is implemented, which finally allows the testing of high data rates.

2. Physical Background

This chapter explains the physical background of RFID systems. RFID systems combine different parameters, such as the magnetic field or coupling factor. Some of them are independent on each other, others depend on another parameter that they are inextricably linked to each other, and chancing one parameter means to influence the other as well. To give the inexperienced reader an idea of the different parameters used in the thesis, the main parameters will be explained and established.

2.1. Magnetic Field

Each current carrying conductor generates an electric field, depicted in Figure 2.1(a), which is normal to its surface. At the same time, an electric field that is normal to the conductor, generates a magnetic field, which forms concentric circles around the conductor. The magnetic field is shown in Figure 2.1(b). In many proximity coupling RFID systems, the transponder is battery



(a) electric field (b) magnetic field

Figure 2.1.: Electric and magnetic field of a single conductor (modified from [30])

free and so energy has to be transferred over the air interface. Therefore, energy is transmitted by the magnetic field generated by the reader. The parameter, which is used to define the energy is the magnetic field strength H, which is defined as [30]:

$$\Theta = \int \vec{H} d\vec{s}, \tag{2.1}$$

where Θ is the magnetomotive force and $\vec{s}$ the integration path. If the integration is along a magnetic field line, which is a circle as long as there are no disturbances in the area around, the

path can be replaced by $2\pi r$. According to [30], the magnetomotive force Θ can be replaced by the current I through the conductor which leads to:

$$H = \frac{I}{2\pi r}, \tag{2.2}$$

where r stands for the radius, corresponding to the distance from the conductor.
In 13.56 MHz RFID applications, the reader antennas are formed as loop antennas with one or more windings. The change of the shape, and the fact that the conductor is bent, leads to a different shaping of the magnetic field. The single field lines of the conductor overlay each other and generate specific characteristics. Figure 2.2 shows the field of a coil or a general loop antenna. With this change of the field lines, it is necessary to expand Equation 2.2 to:

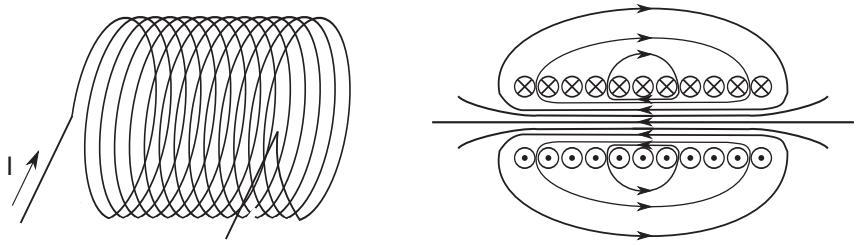


Figure 2.2.: Magnetic field of a loop antenna (modified from [30])

$$H = \frac{I\,N\,r^2}{2\sqrt{(r^2+x^2)^3}}, \tag{2.3}$$

where N is the number of loops, r the radius of the antenna and x the distance from the origin along the rotation axis.
For the reader manufacturers, circular antennas are often hard to handle since many reader housings are of rectangular shape. Therefore it is much easier to implement a rectangular antenna in the housing instead of a circular one. To calculate the field strength of a rectangular antenna, the formula has to be extended again to:

$$H = \frac{I\,N\,a\,b}{4\pi\sqrt{\left(\frac{a}{2}\right)^2+\left(\frac{b}{2}\right)^2+x^2}}\left(\frac{1}{\left(\frac{a}{2}\right)^2+x^2}+\frac{1}{\left(\frac{b}{2}\right)^2+x^2}\right) \tag{2.4}$$

Here a and b are the length and width of the antenna, respectively.

2.2. Inductance

As described before, each conductor generates a magnetic field if a current is flowing. The relation between the magnetic flux linkage Ψ and the current I through a loop of the area A can be expressed by the inductance L. Figure 2.3 shows the setting, and Equation 2.5 the calculation of the inductance.

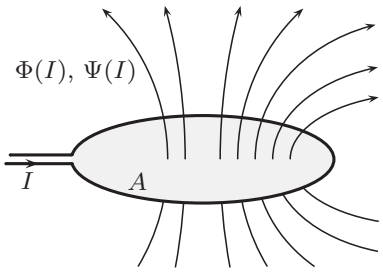


Figure 2.3.: Magnetic field of a loop antenna [31]

$$L = \frac{\Psi}{I} \tag{2.5}$$

In a conductor, each winding has the same current, which leads to the same magnetic flux Φ. That way the magnetic field flux linkage can be replaced by the number of windings N and the magnetic flux through a single conductor, so Ψ can be replaced by $\Psi = N\,\Phi$. Furthermore the magnetic flux Φ can be represented, according to [32], by:

$$\Phi = \int_A \vec{B}\; d\vec{A}, \tag{2.6}$$

where $\vec{B}$ is the magnetic flux density and $\vec{A}$ the area of the coil. Inserting those expressions to Equation 2.5 leads to

$$L = \frac{N}{I} \int_A \vec{B}\; d\vec{A}. \tag{2.7}$$

According to [32] the integral can be separated into the integral over the circumference as well as area of the coil, which leads to:

$$L = \frac{N}{I} \int_0^{2\pi r} \left[\int_R^{2r-R} \frac{\mu_0 N I}{2\pi a}\; da \right]\; dc, \tag{2.8}$$

where r is the radius of the coil, and R the radius of the conductor itself. Solving the integrals results in Equation 2.9, which expresses the inductance with geometric parameters only.

$$L = \mu_0\; N^2\; r\; ln\left(\frac{2r-R}{R}\right) \tag{2.9}$$

2.3. Mutual Inductance

The mutual inductance M describes the effect which can be observed when a second coil moves in the vicinity of a primary current carrying coil. Figure 2.4 depicts the setting and shows all parameters. The first coil L_1, enclosing the area A_1, generates a magnetic field caused by the current I_1. Parts of the magnetic field pass through the second coil L_2 and cause a field flux linkage Ψ_{21}. The relation between them is defined as mutual inductance M_{21}, where the index $_{21}$ means that a flux through L_2 is caused by a current through L_1.
M_{21} is defined as [33]

$$M_{21} = \frac{\Psi_{21}(I_1)}{I_1} = \frac{\int_{A2} B_2(I_1)\, dA}{I_1} \tag{2.10}$$

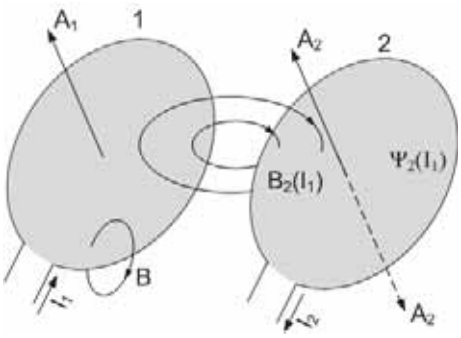


Figure 2.4.: Illustration of the mutual inductance of two coils (modified from [33])

As a result of the induced voltage from L_1 in L_2, L_2 also generates a field which induces a voltage in L_1. Therefore the mutual inductance for M_{12} is

$$M_{12} = \frac{\Psi_{12}(I_2)}{I_2}, \tag{2.11}$$

according to the inversion theorem it can be said that

$$M_{12} = \left.\frac{\Psi_{12}(I_2)}{I_2}\right|_{I_1=0} = \left.\frac{\Psi_{21}(I_1)}{I_1}\right|_{I_2=0} = M_{21} = M. \tag{2.12}$$

To get a formula with the geometric parameters, assuming two circular antennas, it is possible to insert Equation 2.6 to 2.10 and solve the integral over the area of coil 2. That way the formula is transformed to

$$M_{21} = \frac{B_2\left(I_1\right) N_2 r_2^2}{I_1}. \tag{2.13}$$

Furthermore, according to [30] B can be represented by the field strength and the permeability μ. That means $B = \mu H$ and H can be replaced by Equation 2.3, thus leading to the general formula for the mutual inductance of circular coils

$$M_{21} = \frac{\mu N_1 r_1^2 N_2 r_2^2 \pi}{2\sqrt{\left(r_1^2 + x^2\right)^3}}. \tag{2.14}$$

For the other direction M_{12} the indices of coil 1 and coil 2 have to be exchanged.

2.4. Coupling Factor

In general, the mutual inductance is a function of physical dimensions and the position of the antennas. A simplification of mutual inductance is to describe the interaction between two coils as the coupling factor. Therefore, antennas with different sizes will show lower coupling (e.g. ISO reader coupled to ID1 or NFC devices), whereas similar antennas (e.g. NFC coupled to NFC) will have a larger coupling factor. The coupling factor is defined with the help of mutual inductance and the inductivities of the coils as defined in [30]:

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{2.15}$$

One of two extremes is no coupling $(k = 0)$, so the coils are completely decoupled. This can be observed first, by having very large distances between the coils, second by one or both coils are shielded, or last when they are orthogonal to each other. The other extreme is the complete coupling $(k = 1)$. This is reached when both coils have the same flux, which can be achieved by the same geometric settings and close distance, or with the help of an iron core.
The coupling factor can have values between 0 and 1 and is often expressed in percent. In standard proximity coupling devices, for example the Pegoda Reader [34] coupled to an ID1 transponder, the coupling is up to 30 %. In NFC applications, where both antennas have nearly the same size, the coupling factor can go up to more than 70 %. The influence of the coupling factor on the system will be discussed in detail in Chapter 4.

2.5. Law of Induction

As described in Section 2.1, each current carrying conductor generates an electric and magnetic field. At the same time, if a loop is close to a magnetic or electric field, a voltage is induced. The condition is that the magnetic field is changing, which can be achieved by a moving magnet, or an alternating field. In RFID applications the reader produces an alternating field which can be used to power the transponder with the induced voltage. The induced voltage is defined as:

$$u_i = \oint \vec{E}_i \, d\vec{s} = -\frac{d}{dt} \left(\int_{A(t)} \vec{B}(t) \, d\vec{A} \right), \tag{2.16}$$

where $\vec{E}_i$ is the induced electrical field strength, caused by the electric eddy current field.

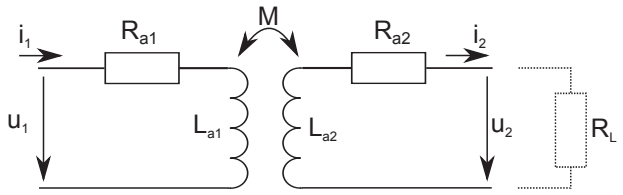


Figure 2.5.: Equivalent circuit of the transformer (modified from [33])

The coupling system and the induction can also be seen with the help of the equivalent circuit of a transformer, as depicted in Figure 2.5. Since the antennas are separated in their inductance and inner resistance, the indices are changed to express the separation of the pure antenna and the equivalent circuit. The current through L_{a1} induces a voltage in L_{a2}, while the current through L_{a2} influences the voltage in L_{a1}. In Equation 2.17 the transformer equation is given according to [33]:

$$u_2 = M \frac{di_1}{dt} - L_{a2} \frac{di_2}{dt} - i_2 R_{a2} \tag{2.17}$$

Since the field is generated by a sine wave, Equation 2.17 can be expressed by the complex amplitude according to [35] to:

$$\underline{U}_2 = j\omega M \underline{I}_1 - j\omega L_{a2} \underline{I}_2 - R_{a2} \underline{I}_2 \tag{2.18}$$

Here $\omega = 2\pi f$. The degree of freedom can be reduced by the current $\underline{I}_2$. Thus $\underline{U}_2$ depends only on $\underline{I}_1$, the primary source of induction. Therefore $\underline{I}_2$ is replaced by $\underline{U}_2/R_L$.

$$\underline{U}_2 = \frac{j\omega M \underline{I}_1}{1 + \frac{j\omega L_{a2} + R_{a2}}{R_L}}. \tag{2.19}$$

With this equation the voltage induced in a second coil can be calculated depending primarily on the elements of the second coil plus mutual inductance and the current. To harvest more energy on the transponder, and to reduce the required input energy at the reader at the same output field strength, a resonance circuit is added. A resonance circuit enables a more efficient operation and is explained in the next chapter.

2.6. Resonance Circuit

The coil itself has a resonance frequency according to the inductance, resistance and the parasitic capacitor. The equivalent circuit of an antenna can be seen in Figure 2.6, where the antenna is represented by its inductivity L_{a2}, its inner resistance R_{a2} and its parasitic capacitance C_{a2}. The resonance frequency can be calculated as:

$$f = \frac{1}{2\pi\sqrt{L_{a2}C_{a2}}} \tag{2.20}$$

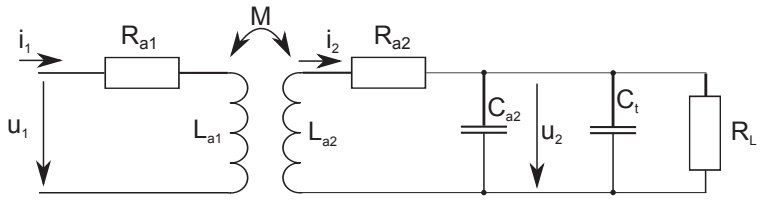


Figure 2.6.: Equivalent circuit of the transformer with resonance circuit (modified from [35])

To harvest more energy, an additional capacitor is added to create a resonance circuit at a certain frequency. Using the resonance circuit, the energy is boosted and more energy is available at the transponder. To calculate the additionally needed capacitor C_t, Equation 2.20 can be rewritten and the required capacitor can be calculated as:

$$C_t = \frac{1}{(2\pi f)^2 L_{a2}} - C_{a2} \tag{2.21}$$

This enhancement leads to a benefit of the voltage at the second coil. Figure 2.7 shows the voltage at the load R_L of the second coil both with the resonance circuit and without it. The trend of the voltage is linear in case of the coil. With the resonance circuit, a peak at a certain frequency can be seen. The peak represents the tuning frequency, and can be defined with the help of the tuning capacitor C_t. The voltage $\underline{U}_2$, depicted in Figure 2.7 without resonance circuit

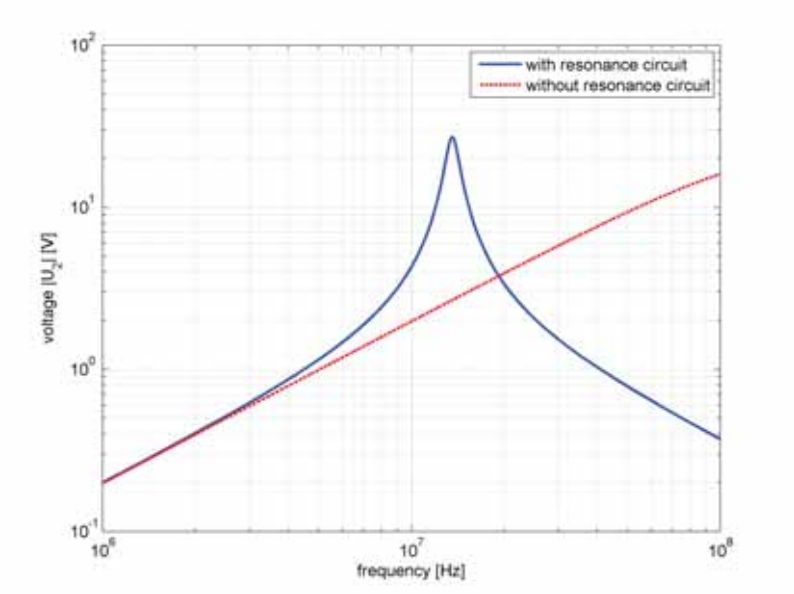


Figure 2.7.: Voltage at the load with and without resonance circuit

is calculated with the help of Equation 2.19, while the voltage with the resonance circuit can be calculated by [35]

$$\underline{U}_2 = \frac{j\omega\, k\, \underline{I}_1 \sqrt{L_1 L_2}}{1 + (j\omega L_{a2} + R_{a2}) \left(\frac{1}{R_L} + j\omega\,(C_{a2} + C_t)\right)}. \tag{2.22}$$

Figure 2.7 shows the voltage at the transponder coil in dependency of the carrier frequency. Comparing the two curves it can be seen that the coil without resonance circuit has a linear voltage dependency over the frequency, while the resonance circuit causes a peak in the voltage at the resonance frequency. This principle can be used to increase the voltage transmission at a certain frequency, which is tuned to the carrier frequency.

2.7. Quality Factor and Bandwidth

To be able to define the power efficiency, or how much the voltage or current is boosted in a resonance circuit, the quality factor Q is introduced. There are many different definitions for the quality factor. It can be defined by the energy stored divided by the energy dissipated per cycle times 2π as [36]:

$$Q = 2\pi \frac{\text{Energy stored}}{\text{Energy dissipated per cycle}} \tag{2.23}$$

Furthermore, it can also be defined by the resonance frequency f_r and the 3 dB bandwidth B_{3dB} such as:

$$Q = \frac{f_r}{B_{3dB}} \tag{2.24}$$

or with the help of the components in the resonance circuit. There it has to be distinguished, whether the resonance circuit consists of a parallel or a serial resonator. In case of a serial resonator, the quality factor can be calculated with the serial resistor R_{ser}, the inductance L and the resonance frequency f_r [37]:

$$Q = \frac{2\,\pi\,f_r\,L}{R_{ser}} \tag{2.25}$$

For a parallel resonance circuit the formula changes to the parallel resistor R_p:

$$Q = \frac{R_p}{2\,\pi\,f_r\,L} \tag{2.26}$$

It expresses the boost of the voltage or current in a circuit and makes a system more energy efficient. The parallel resonator maximizes the voltage, while a serial resonator maximizes the current in the circuit. The quality factor depends on the inductance of the coil and the resistor, and can be seen in Equation 2.25 and 2.26. That means with an additional resistor, the quality factor can be influenced, as it is done in the ISO test setup described in [38].
At the same time, the quality factor is an indicator of the energy efficiency, and it can also be used to define the bandwidth as shown in Equation 2.24. The quality factor is directly linked to the bandwidth, and by transforming Equation 2.24 to Equation 2.27, the bandwidth limitation can be defined:

$$B_{3dB} = \frac{f_r}{Q} \tag{2.27}$$

Figure 2.8 depicts the relation between the quality factor Q_1 and Q_2, and the bandwidth B_1 and B_2 of two resonators. Equation 2.27 shows that Q and B are indirect proportional. The quality

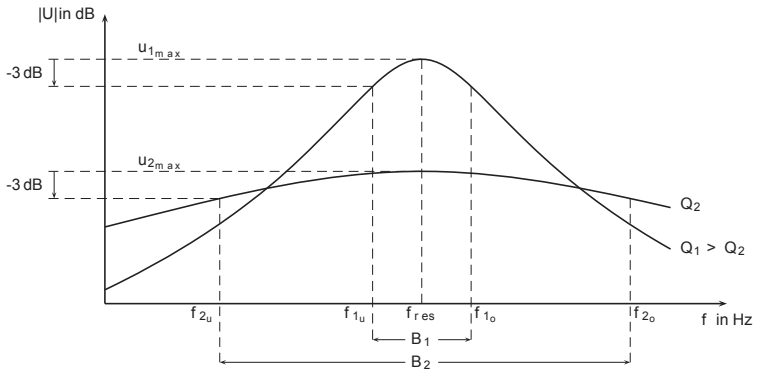


Figure 2.8.: Comparison between 2 different quality factors taken from [31]

factor Q_1 is much higher than Q_2, which results in a higher field strength, assuming a constant input power. At the same time the energy efficiency is improved the bandwidth is reduced. This is shown in Figure 2.8, where the quality factor Q_1 is higher than Q_2, represented by a higher amplitude on the y-axis. By mapping the related bandwidth to the curves on the x axis, it is shown that the bandwidth B_1 corresponding to Q_1 is smaller than the bandwidth B_2 for a lower quality factor. This shows that the bandwidth and the quality factor are indirect proportional and either a high bandwidth or a high quality factor can be achieved.
Increasing the data rate by reducing the symbol time increases the required bandwidth, which leads to a lower quality factor to ensure the required bandwidth. This on the other side makes

the system more energy consuming, and the power efficiency is reduced. To keep the quality factor high an alternative modulation has to be found, not to increase the required bandwidth. Therefore, different modulation schemes will be evaluated and compared to find the best suitable modulation for the given system.

3. Basic Structure of 13.56 MHz RFID Systems

Depending on the application described in the previous chapter, RFID systems have different requirements. These requirements are fulfilled by different hardware structures, but from top level view the system stays the same in all kinds of application. It consists of a reader device, a transponder and an air interface in between. In the following chapter these three parts will be described and the equivalent network of each part will be calculated. The chapter is separated in three sections, where first the reader is described. After that the transponder will be presented and in the end the interaction of both will be outlined by the air interface.

3.1. Reader

On the one hand the reader has the function of providing the energy which is needed to power the transponder, as most transponders are battery less and are supplied by the field. On the other hand it also sends data to the transponder and receives the answers. For the energy transmission the shape of the antenna, the input voltage and the matching network are relevant parameters. Depending on the application, the reader has different sizes, which also ends in different antenna sizes and shapes. To describe the reader in a mathematical way a certain system has to be defined. To keep the transparency of this thesis the ISO test setup is taken as reference which is defined in [38].
Figure 3.1 shows the schematic of the reader. It consists of a source, a matching network and an antenna. The matching network on the one hand matches the input of the network to the output of the source (in most cases 50 Ohm, due to the fact that much of the laboratory equipment has an output of 50 Ohm). The second task is to form a resonance circuit with the antenna to be more energy efficient. To do all calculations the electrical parameters of the antenna have to be extracted first, which will be explained in Subsection 3.1.1.

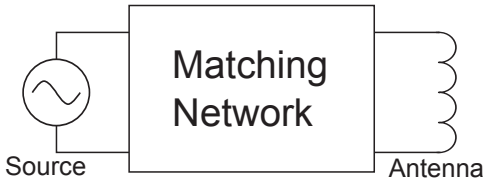


Figure 3.1.: Block diagram of the ISO reader

3.1.1. Reader Antenna Characterization

Due to the fact that there are many different reader antennas available, nearly all competitors use different antennas, number of windings, sizes, shapes, and quality factors, it is hard to compare systems with each other. In Figure 3.2 some examples of different reader antennas are shown. The shape of the antenna is influenced by the application, needed energy and available space.

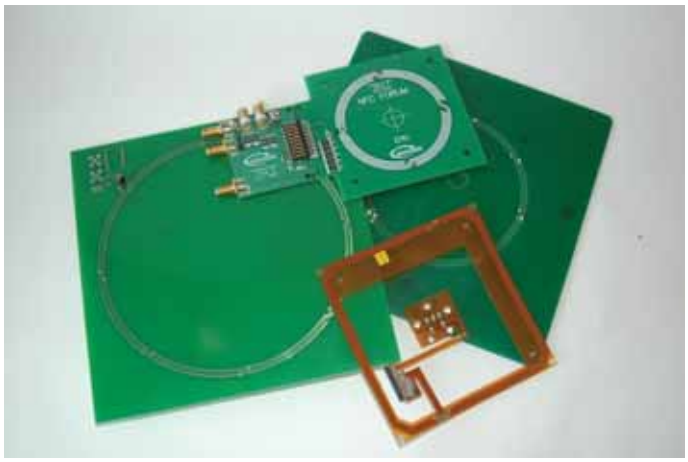


Figure 3.2.: Different possible reader antennas

With the shape of the antenna the field can be influenced and so the read range of the reader is varied. Due to the fact that there are many different reader antennas, the ISO setup is used as reference reader model. This has the advantages that all competitors have access to the same antenna and same parameters and so it is possible for everyone to prove the results. Another advantage is that the ISO setup is used to characterize transponders and so a huge number of measurement results are available which can be used to verify the system and model.
Typical antennas are for example a square antenna with 2 windings with a dimension of 10 times 10 cm. For eGovernment applications the antenna has to be larger, not to influence the optical scan. The dimension is approximately 18 times 15 cm to guarantee that the passport can be scanned without any disturbing wires. Those two antennas show a huge difference, and will influence the system in other ways. For the basic findings the ISO antenna will be taken as reference to show the feasibility and to reduce the measurement and simulation effort. The ISO test setup is described in [38]. In this standard the layout of the printed circuit board (PCB) is shown and important physical parameters, such as the material of the PCB and the thickness of the copper layer, are given. With those parameters it is possible to produce the antenna, but due to manufacturing tolerance the electrical parameters of the antennas vary a little. The antenna used in this thesis is modified, due to the reason that a receive path is necessary to use the antenna as reader, therefore an additional connection was implemented which allows to measure the signal at the dumping resistors.
In the latest amendment of the standard two different matching topologies are available, for the base data rate of 106 kbit/s and the higher data rates from 212 up to 848 kbit/s. Since the goal is to reach data rates up to 6.78 Mbit/s, the second topology with the lower quality factor could be used. In this case some problems, which will occur with the higher quality factor, will not be addressed, but for research purpose the goal with the topology for lower data rates is more

challenging, which will be described later. Furthermore readers in real applications use a higher quality factor and so the lower data rate antenna is closer to a real system.
The electrical parameters of the antenna can be defined by measurements or calculations. First the inductance of the antenna will be calculated from the geometrical parameters, before the antenna is characterized by measurements.

Antenna Calculation

The inductance can be calculated with Equation 2.9, which is described in Section 2.2.
Since the conductor of the ISO antenna is not a circle as described in the formula, the radius of the conductor has to be replaced by

$$R = \frac{w + t}{2}, \tag{3.1}$$

where w is the width of the conductor and t the thickness. With the parameters shown in Table 3.1 and Equation 2.9 the inductance of the antenna is calculated and leads to $L = 500\ nH$.

R [mm]	w [mm]	t [µm]	N
72.25	1.8	35	1

Table 3.1.: Parameters for the inductance calculation

As described in [39] there are different ways to calculate the inductance of an antenna. The problem is that the antenna calculation is not very accurate and different approaches lead to different results. In this calculation the result is $L = 500\,\text{nH}$. Other approaches, which are described in [39], lead to a variation of the results from $L = 143\,\text{nH}$ up to $L = 500\,\text{nH}$, using the same input parameters. To be sure that the assumed inductance matches with the reality, additional measurements will be done to define the inductance of the used antenna. Furthermore, other relevant parameters, such as the parasitic capacitor and the resistance will be measured as well.

Antenna Measurement

There are several ways to measure the inductance of the antenna. The easiest way would be to use the Inductance-Capacitance-Resistance (LCR) meter. For that purpose the antenna is connected to the input of the measurement device and the inductance is defined. Furthermore, the serial as well as parallel resistance can be measured, as well as the capacitor of the antenna. Due to the fact that the antenna has production uncertainties, several antennas were measured and the results were averaged.
Another way is to measure the parameters with the help of a network analyzer and the Smith chart. The inductance and resistance at 1 MHz are measured and the results are displayed in Table 3.2.

Going further in the Smith chart, the resonance frequency of the antenna and the parallel resistance can be defined.

L_{AR}	480 nH
R_{DC}	140 mΩ

Table 3.2.: Antenna measurement results at 1 MHz

f_{res}	45 MHz
R_p	9.5 kΩ

Table 3.3.: Antenna measurement results at resonance frequency

With the values of the measurement the electrical parameters of the antenna can be calculated. The capacitor can be calculated with the help of the resonance frequency and the inductance by

$$C \cong \frac{1}{\omega^2 L}. \tag{3.2}$$

The parallel resistance at the carrier frequency can be calculated with the help of the factor described in Equation 3.3. The factor represents the skin effect of the antenna conductors at the carrier frequency of 13.56 MHz:

$$K = \sqrt{\frac{f_{res}}{f_{carrier}}} \tag{3.3}$$

With the help of this factor the resistance at the carrier frequency can be calculated as

$$R_{P,fc} = K\, R_{P,res}. \tag{3.4}$$

Converting the parallel resistor to a serial resistor with the help of the quality factor leads to

$$R_S = \frac{(\omega L)^2}{R_P}. \tag{3.5}$$

Adding the resistance at 1 MHz leads to the equivalent resistance of the antenna $R_{AR} = R_S + R_{DC}$. The quality factor of the antenna without any network can be calculated by

$$Q_A = \frac{(\omega L)^2}{R_{AR}}. \tag{3.6}$$

With the help of the calculations above the antenna can be described electrically. The values are given in Table 3.4, and will be kept constant during the whole thesis.

L_{AR}	480 nH
C_{AR}	26 pF
R_{AR}	0.237 Ω
$R_{P,AR}$	17.306 kΩ
Q_{Ant}	172.8

Table 3.4.: Antenna parameters

3.1.2. Matching Network

The matching network of the reader has two main functionalities. On the one hand, it forms the resonance circuit with the antenna and on the other hand it matches the input of the matching network to the connection. In this specific case the matching should be 50 Ohm due to the fact, that the amplifier has an output resistance of 50 Ohm and the used cables are also matched to 50 Ohm.
If the network is matched perfectly it has an impedance of 50 Ohm real and no imaginary part. To achieve the matching, a network of capacitors and resistors is used. The topology of the matching network can be seen in Figure 3.3.

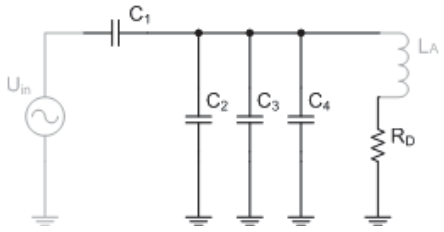


Figure 3.3.: Matching network of the reader

The capacitors C_2, C_3 and C_4 form the resonance circuit with the antenna and together with C_1 they form the matching network to get 50 Ohm real at the input of the network. With the resistor R_D the quality factor can be reduced. This resistor is called the quality factor reducing resistor, or dumping resistor. The external resistor can be calculated by Equation 3.7 with the help of the values from Table 3.4:

$$R_D = \frac{\omega\, L}{Q_{wanted}} - R_{AR} \tag{3.7}$$

The matching network can be calculated by Equation 3.8 and 3.9. Here it has to be said that those formulas are approximations which fit good in reality but checking those values in expanded calculations will show that there is an error left:

$$C_1 = \frac{1}{\omega \cdot \sqrt{R_{IN} \cdot R_{P,total}}} \tag{3.8}$$

$$C_4 = \frac{1}{\omega^2 \cdot L_{AR}} - C_1 - C_{AR} - C_2 - C_3 \tag{3.9}$$

It would be possible to expand these formulas to get a more exact result, but the effort in production would be too high and due to tolerances of the various parts the values cannot be achieved that accurate as they can be calculated. With the help of Equations 3.7, 3.8 and 3.9 and the parameters of the ISO setup (defined in [17]) the required matching components are calculated and the results are listed in Table 3.5.

With the help of these calculations, the matching network, as well as the reader antenna can be described electrically. With those parameters it is possible to calculate the transfer function and the current through the antenna, which is the relevant parameter for the field strength.

$C_{1,standard}$	47 pF
$C_{1,calculated}$	44 pF
C_2	180 pF
C_3	33 pF
C_4	1 pF
R_D	0.94 Ω

Table 3.5.: Matching network parameters

3.1.3. Mathematical Reader Description

The matching network consists of one serial capacitor and three parallel capacitors (in the calculation, those three capacitors can be summed to one single capacitor, but according to the ISO standard, they are separated to achieve the wanted value). This network is connected to the ISO antenna and five dumping resistors. Here it is necessary to use parallel resistors due to the high current through the resistors. At these dumping resistors, the receive path of the reader is connected. The advantage is that the signal is the same as on the other connector of the antenna, with a lower amplitude, which makes an additional voltage divider dispensable.

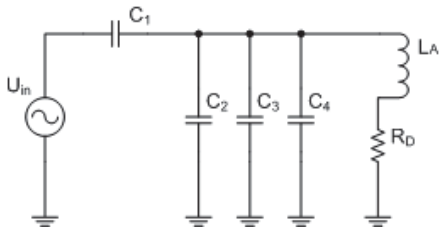


Figure 3.4.: Schematic of the ISO reader

The antenna itself can be replaced in the calculation by its equivalent circuit, which consists of a parallel capacitor C_{AR} over the inductance L_{AR} and the conductor resistance R_{AR}. The full equivalent network can be seen in Figure 3.5.
The amplifier used in this network is a voltage amplifier with an output impedance of 50 Ohm.
Simplifying the reader to the network shown in Figure 3.6, the formula gets complicated, with all variables shown before.

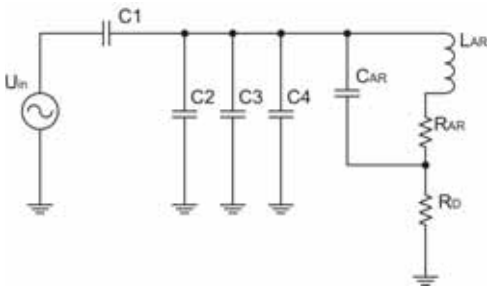


Figure 3.5.: Equivalent network

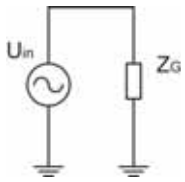


Figure 3.6.: Simplified network of the reader

$$Z_G = \frac{1}{i\,\omega\,C_1} + \frac{1}{i\,\omega\,(C_2 + C_3 + C_4) + \frac{1}{R_D + \frac{1}{i\,\omega\,C_{AR} + \frac{1}{i\,\omega\,L_{AR} + R_{AR}}}}} \tag{3.10}$$

If the network is matched perfectly Z_G has 50 Ohm real and no imaginary part. This can be calculated on the one hand, on the other hand it can be proved by a network analyzer and the Smith chart.
With the help of the equivalent circuit all currents and voltages in the reader can be calculated. The most interesting part of the reader is the current through the antenna and the voltage at the dumping resistor. The current defines the field strength emitted in the air around the antenna. The voltage drop over the dumping resistor is used to demodulate the signal received from the transponder.
With the help of Equation 3.10 the current consumption of the reader can be calculated, and with this current, the voltage and current in each point of the reader can be evaluated. Furthermore, the equation can be used to calculate the transfer function and show the behavior over frequency. A detailed analysis of the reader is done in Section 4.3.

3.2. Transponder

The transponder consists of various parts as depicted in Figure 3.7. The antenna represents the interface to the environment and is used to power the integrated circuit (IC) and transmit data. The antenna is connected to a matching circuit, which forms the resonance circuit on the transponder to increase the energy efficiency, like on the reader. The voltage from the resonator is connected

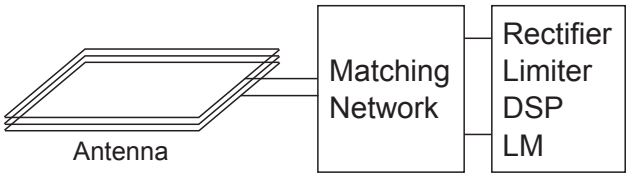


Figure 3.7.: Schematic of a transponder (DSP: digital signal processing, LM: load modulator)

to a rectifier, which generates a DC voltage which is needed to power the IC. A limiter guarantees that the voltage does not exceed a certain value, which could harm the IC, and it regulates the voltage to a certain level. The voltage is defined by the process, which is used to produce the IC. A smaller process needs a lower voltage, not to destroy the inner structure. Depending on the

application, product, standard and so on, the demodulation is either done digitally or analog. The last part of the transponder is the load modulator. It can consist of a switch and a resistor, or a transistor. The task of the load modulator is to change the impedance of the transponder, which results in a change of the quality factor, seen on the reader. The various parts of the transponder will be explained in more detail in the following part.

3.2.1. Transponder Antenna Characterization

Transponder antennas have different shapes and sizes depending on the application. The actual antenna size for proximity cards is defined in [20]. This is the format, which is known from credit cards, health cards and many other cards. The total size of the card itself is defined in [40]. The card has a size of 85.5 x 54 mm. Depending on the card, different constraints are made, for special structures, such as magnetic stripe, or contact-type interface. The antenna itself has to be within a certain range, which is defined by two rectangles, as depicted in Figure 3.8. Since

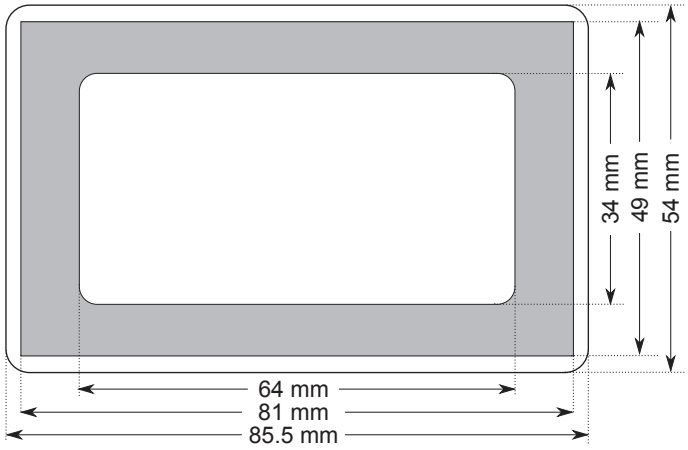


Figure 3.8.: Definition of the ID-1 antenna

the trend goes to smaller antennas, standardization discussions are ongoing at the moment. The antenna sizes should be made much smaller, as can be seen in the amendment for the standardization in [41]. In this thesis the reference for the measurements, as well as simulation will be the ID-1 antenna. As there are many different ID-1 antennas, the reference antenna in this thesis will be the reference PICC antenna defined in [38]. The reason is that all antennas, although they pass the same tests, have different parameters depending on the manufacturing process. In Figure 3.9 different transponder antennas are shown. All are in the same ID-1 class, but it can be seen that they vary. The main differences will be seen in the next two subchapters, where those antennas will be analyzed and measured.

Figure 3.9.: Picture of different ID-1 antennas

Antenna Analysis

The inductance of a rectangular antenna is calculated generally as follows [42].

$$
\begin{aligned}
L &= \frac{\mu_0}{\pi}\left(x_1 + x_2 + x_3 + x4\right) \cdot N^{\alpha} \qquad (3.11)\\
x_1 &= a \cdot ln\left(\frac{2 \cdot a \cdot b}{d \cdot \left(a + \sqrt{a^2 + b^2}\right)}\right)\\
x_2 &= b \cdot ln\left(\frac{2 \cdot a \cdot b}{d \cdot \left(b + \sqrt{a^2 + b^2}\right)}\right)\\
x_3 &= 2 \cdot \left(a + b - \sqrt{a^2 + b^2}\right)\\
x_4 &= \frac{a+b}{4}\\
d &= \frac{2 \cdot (t + w)}{\pi}\\
\alpha &= 1.8
\end{aligned}
$$

As described in [39], different ways can be used to calculate the coefficients a and b. The result varies, depending if the arithmetic, geometric or other ways to calculate the average for a and b are used. Furthermore it can be seen in [39], that α is not a fixed value, and has to be adjusted depending on the shape of the antenna, the gap between the conductors and the width of them. To get more accurate results, several antennas of the same type are measured and the results are averaged to obtain a typical value for each antenna.

Antenna Measurement

The measurement procedure, as well as the calculation, was already explained at the reader antenna measurement. Therefore here only the results are listed. Different antennas where used to show the variance between the electrical parameters of the same antenna type, but different production processes. In Figure 3.9 different production processes can be seen, as well as different types of ID-1 antennas, which vary in the width of the conductors as well as the gap between them. According to the material, width and thickness of the conductor, the electrical parameters vary, and so the characteristic of the antenna changes. In Table 3.6 different production processes as well as antenna types are characterized, and it can be seen, that the values vary in a quite large range, although they are all based on the same standard.

	ref. PICC	**etched**	**wired**	**printed**	**galvanic**
turns	4	4	5	5	6
outer dimension [mm]	7.20 x 4.20	7.50 x 4.60	8.00 x 4.90	8.00 x 4.80	7.60 x 4.40
inner dimension [mm]	6.45 x 3.45	7.15 x 4.25	7.40 x 4.30	6.80 x 3.60	6.40 x 3.20
fres [MHz]	44.66	45.80	40.85	37.87	27.30
L [µH]	2.31	3.15	4.88	3.33	4.27
C [pF]	5.50	3.83	3.26	5.31	7.93
R [Ω]	0.85	4.57	8.24	17.29	7.34

Table 3.6.: Electrical parameters of different ID-1 antennas

3.2.2. Analog Front End

The analog front end of the transponder can be seen in Figure 3.10. The antenna is connected to the matching network, which forms the resonance circuit, like on the reader. That way the

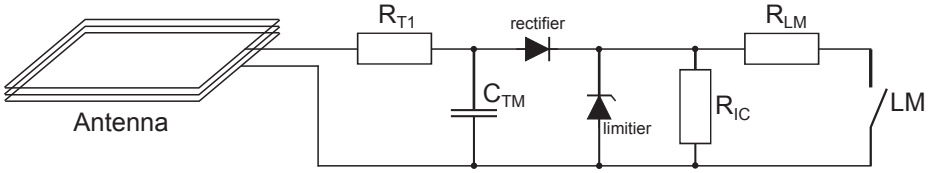


Figure 3.10.: Schematic of a transponder

energy efficiency of the transponder is increased. The best performance, in terms of energy, would be achieved by tuning the resonance circuit to the carrier frequency of 13.56 MHz. Since this would result in other problems, the resonance frequency is tuned by the capacitor C_{TM} to a value between 14 and 18 MHz. This is necessary to reduce the detuning of the reader, mainly if more transponders are in the field at the same time. The detuning effect will be explained in Chapter 4. The resonance frequency can be calculated by

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{L_A\, C_{TM}}}. \tag{3.12}$$

The resistor R_{T1} represents the losses of the conductor.
The IC itself needs a DC supply voltage, and so the signal of the resonance circuit is rectified. The rectifier is here depicted as single diode. In reality the rectifier is more complicated and built of several transistors to get a good performance. Since the main focus is on the reader, it is enough to represent the rectifier in the model with a diode. For further analysis this diode is replaced by a full wave rectifier in the model to get a close to nature performance, in the figures this rectifier is only displayed as diode.
The limiter structure is represented as single Zener diode, which limits the DC voltage to a certain level. In the IC itself, the limiter is much more complicated and has the function to protect the IC from too high voltages and regulate the voltage to a certain level. This is achieved by a structure, which regulates a transistor in a way to change its resistance to achieve the wanted voltage. If the energy at the transponder is low, the transistor has a very high resistance, not to limit the voltage. As soon as the transponder comes to the range, where the voltage is too high, the resistance is reduced to stabilize the voltage to a certain level. The voltage level of the IC is dependent of the process, which is used to fabricate the IC.
The resistor R_{IC} represents the current consumption of the transponder. In the model it is a good approximation to use a resistor instead of the IC to save simulation time. The current consumption is given by

$$I_{IC} = \frac{U_{limiter}}{R_{IC}}. \tag{3.13}$$

I_{IC} is the current consumption of the IC, $U_{limiter}$ the limiter voltage of the IC and R_{IC} the value of the resistor which represents the IC. The last part in Figure 3.10 represents the load modulator. In the IC itself it is another transistor, but in this model the transistor is replaced by a switch and a resistor. With the help of the load modulator the transponder transmits the data to the reader by changing its impedance. This modulates the quality factor of the transponder by different load levels. The easiest way to emulate this behavior is with a switch and resistor as it can be seen in the Figure. With the help of the resistor the magnitude of the modulation can be defined. The strongest feedback can be achieved with a very low resistor, which short circuits the transponder. The only remaining resistances are the conductor resistance and the voltage drop over the rectifier. The presented transponder is based on the reference PICC, which is used to test readers.

3.2.3. Mathematical Transponder Description

To describe the transponder mathematically, two different settings have to be separated. The first version is, when the load modulator is open, and so the resistor R_{LM} is not connected to the circuit. The second case is during the modulation, where R_{LM} is in parallel to the resistor which represents the current consumption of the IC. Furthermore, the limiter is represented as resistor in the calculation model, since the current flow through the transistor, which limits the voltage at the IC, can be achieved by varying the resistance. The rectifier can be seen as constant voltage drop to simplify the calculation. Figure 3.11 shows the equivalent network of the transponder, using the same antenna equivalent as in the reader. The parameters of the antenna are listed in Table 3.6 in the first column (reference PICC). Since there is no need at the moment to characterize the transponder as single component, the calculation will be done in the next chapter, where the whole system will be verified.

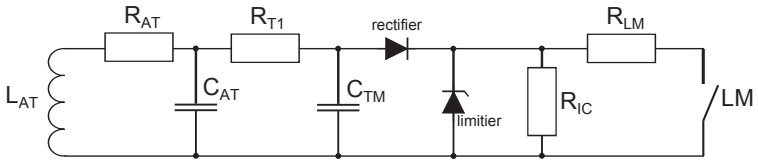


Figure 3.11.: Equivalent network of a transponder

3.3. Channel

The definition of the channel differs in most books. According to [43] the channel is defined as:
*„**Channel** A medium or medium -associated allocation, such as carrier frequency, for electronic communication.“* [43]
According to Sklar:
*„**Channel** The propagation medium or electronic path connecting the transmitter and receiver is called channel. In general, ...in case of radio-frequency links, waveguides, the atmosphere, or empty space.“* [44]
Even if the definition differs a little, the glue is the same in both definitions. In RF systems, the channel is everything, which is between the transmitter and the receiver. Due to the architecture RFID systems operate in the near field, and so they have different behavior than classical RF systems. Effects like atmospheric attenuation, Doppler Effect and multi path propagation can be neglected in general in RFID systems, unless the system is located in a real harmful environment. The problem in systems which operate in their near field, is that they influence each other, and a so called detuning can be observed, which will be explained in Chapter 4.
Due to the influence and detuning, the air interface cannot be observed as isolated part, and the system has to be described as one whole system. This leads to the definition of the mutual inductance.

3.3.1. Mutual Inductance and Coupling Factor

The mutual inductance, described in Section 2.3, or the coupling factor described in Section 2.4 is a single term, which describes the relation between two coils, which are close to each other. That way the coupling factor is the missing part to combine the reader and the transponder to a

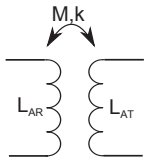


Figure 3.12.: Mutual inductance or coupling factor

single system, which influence each other. To understand all effects, which are caused by the coupling, the whole system has to be taken into account. A detailed analysis of the coupling factor can be found in [39].

3.3.2. Mathematical Description

As mentioned before the mutual inductance or coupling factor is based on the geometry of the antennas, as well as their position to each other. As illustrated in [39] there are several possible ways to calculate the coupling factor with a certain degree of accuracy and complexity. Those formulas always assume either circular or rectangular antennas, but never a combination of both. In the system which should be evaluated, the antenna shapes are different. The reader antenna is a circle one, while the transponder antenna is rectangular, as defined in [38].
Therefore the coupling from a circle to a rectangular antenna has to be approximated. To calculate the coupling factor with higher accuracy, the calculation is performed twice. First the rectangular antenna is transformed into an area equivalent round antenna according to:

$$r^2\pi = a \cdot b \rightarrow b = a \tag{3.14}$$

That way the coupling factor can be calculated with the formula for circle antennas [39]:

$$k = \mu_0 \frac{r_1\, r_2\, N_1\, N_2}{4\,\pi\sqrt{L_1 L_2}} \int_0^{2\pi} \frac{\cos(\varphi_1 - \varphi_2)}{\sqrt{x^2 + y^2 + z^2}} \mathrm{d}\varphi_1\, \mathrm{d}\varphi_2 \tag{3.15}$$

$$\begin{aligned} x &= x_1 + r_1\, \cos\varphi_1 - x_2 - r_2\, \cos\varphi_2 \\ y &= y_1 + r_1\, \sin\varphi_1 - y_2 - r_2\, \sin\varphi_2 \\ z &= z_1 - z_2 \end{aligned}$$

The used parameters in Equation 3.15 are defined in Figure 3.13. The parameters x, y and z

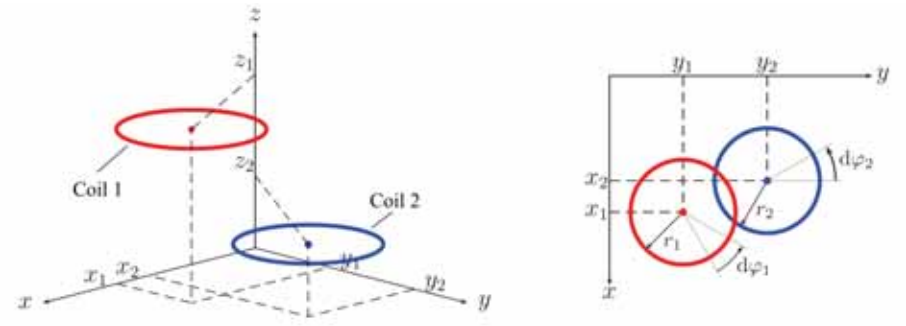


Figure 3.13.: Arrangement of two circular antennas [39]

are the coordinates of the origin of each antenna in the volume. r represents the radius, while φ is the angle between the plane of the antenna and the ground.
In the next step the round antenna is transformed in an area equivalent rectangular antenna with Equation 3.14 to calculate the coupling factor with the help of the formula for the rectangular

antenna:

$$
\begin{aligned}
k =& \mu_0 \frac{N_1 N_2}{4\pi\sqrt{L_1 L_2}} \int_{-\frac{a}{2}}^{\frac{a}{2}} \int_{-\frac{c}{2}}^{\frac{c}{2}} \frac{1}{\sqrt{(x-\chi_1+\chi_2)^2+\left(y-\frac{b}{2}+\frac{d}{2}\right)^2+z^2}} \cdots \\
&\cdots - \frac{1}{\sqrt{(x-\chi_1+\chi_2)^2+\left(y-\frac{b}{2}-\frac{d}{2}\right)^2+z^2}} - \frac{1}{\sqrt{(x-\chi_1+\chi_2)^2+\left(y+\frac{b}{2}+\frac{d}{2}\right)^2+z^2}} \cdots \\
&\cdots + \frac{1}{\sqrt{(x-\chi_1+\chi_2)^2+\left(y+\frac{b}{2}-\frac{d}{2}\right)^2+z^2}} \mathrm{d}\chi_1 \, \mathrm{d}\chi_2 \cdots \\
&\cdots + \mu_0 \frac{N_1 N_2}{4\pi} \int_{-\frac{b}{2}}^{\frac{b}{2}} \int_{-\frac{d}{2}}^{\frac{d}{2}} \frac{1}{\sqrt{\left(x-\frac{a}{2}+\frac{c}{2}\right)^2+(y-\upsilon_1+\upsilon_2)^2+z^2}} \cdots \\
&\cdots - \frac{1}{\sqrt{\left(x-\frac{a}{2}-\frac{c}{2}\right)^2+(y-\upsilon_1+\upsilon_2)^2+z^2}} - \frac{1}{\sqrt{\left(x+\frac{a}{2}+\frac{c}{2}\right)^2+(y-\upsilon_1+\upsilon_2)^2+z^2}} \cdots \\
&\cdots + \frac{1}{\sqrt{\left(x+\frac{a}{2}-\frac{c}{2}\right)^2+(y-\upsilon_1+\upsilon_2)^2+z^2}} \mathrm{d}\upsilon_1 \, \mathrm{d}\upsilon_2
\end{aligned}
\tag{3.16}
$$

The used parameters are the same like in the figure before, where the radius is replaced by the length of each side a and b for the first antenna and c and d for the second one.
To reduce the error of each calculation, which is caused by the shape transformation, the average of both results is calculated and used as reference.
The shown formulas are rather complicated, but can be simplified if the antennas are located coaxial (which means $\varphi_1 = \varphi_2 = 0$, $x_1 = x_2$ and $y_1 = y_2$) . Due to higher flexibility in future, the simplifications are neglected to keep the highest degree of freedom. In the following system calculations, the coupling factor is added as single parameter, according to the position of the antennas.

3.4. Mathematical System Description

In this chapter all findings from the last chapters are combined to describe the whole RFID system in one equation. To calculate the whole system the equivalent network of the air interface will be used, according to Figure 3.14. All parts are as described in the previous Chapters. The only change is a simplification of the transponder, since the main focus is on the reader side. In the figure it can be seen, that the rectifier is removed, since it will cause a constant voltage drop, which is caused by the threshold voltage of the diodes. Instead of taking this voltage drop into account in the calculation, the limiter voltage will be increased by the voltage drop, to take the effect of the rectifier into account as well. Furthermore, the limiter is replaced by a variable resistor $R_{limiter}$, which is a good approximation of the real limiter. Depending on the induced voltage, the resistor is reduced till the required voltage is achieved.

$$
Z_G = \frac{1}{i\,\omega\,C_1} + \frac{1}{i\,\omega\,(C_2+C_3+C_4) + \frac{1}{R_D + \frac{1}{i\,\omega\,C_{AR} + \frac{1}{i\,\omega\,L_{AR}+R_{AR}+Z_{Transponder}}}}}
\tag{3.17}
$$

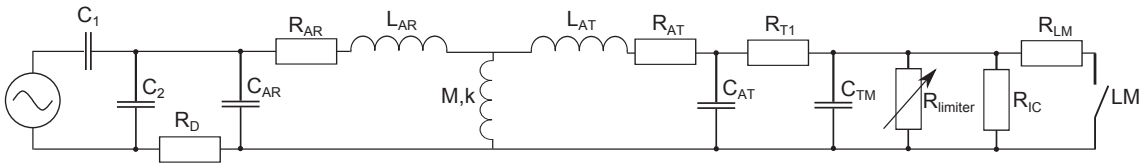


Figure 3.14.: Equivalent network of the RFID system

To describe the system the impedance of the whole structure is calculated. Equation 3.17 is the same like Equation 3.10, which represents the reader, with an additional term in the last fracture. The term $Z_{Transponder}$ represents the impedance, which is caused by the coupling and the transponder:

$$Z_{Transponder} = \frac{1}{\frac{1}{i\,\omega\,M} + \frac{1}{R_{AT}+i\,\omega\,L_{AT}+\frac{1}{i\,\omega\,C_{AT}+\frac{1}{R_{T1}+i\,\omega\,C_{TM}+\frac{1}{\frac{1}{R_{LM}}+\frac{1}{R_{IC}}+\frac{1}{R_{limiter}}}}}}} \tag{3.18}$$

The first term in the numerator of Equation 3.18 of the large fraction is dependent of the mutual inductance M. If the transponder is removed from the field, the mutual inductance M goes to 0. That way the numerator of the first term is 0, and so the fraction goes to infinity. If the numerator of a fraction is infinite, the whole fraction is 0, which means that $Z_{Transponder} = 0$ and the transponder does not have any influence on the reader.
Increasing the coupling, which means that the distance between the reader and the transponder is reduced, Equation 3.18 is gaining more influence on the whole impedance and the influence on the reader can be described.
The next chapter will deal with different simulations to gain insights in the numerous effects which have to be handled in RFID systems.

4. System Analysis and Effects on 13.56 MHz RFID Systems

This chapter describes the influences of parameters, such as the current consumption at the transponder or the resonance frequency, on the whole system. Therefore a Matlab model is generated based on the mathematical description of the previous chapter. With this model different effects, for example the change of the quality factor, or the resonance frequency, can be analyzed. Those cognitions lead to a better understanding of the system, and effects can be forecasted and counteractions can be performed. As already mentioned there are an uncountable number of variations within RFID systems, therefore the hardware of the ISO/IEC 10373 test setup is taken, to describe the effects which are caused by different settings and parameters of the system.

4.1. Realization in MATLAB

The system described in Section 3.4 is implemented in Matlab to give an idea how the system behaves.
The system is implemented as depicted in Figure 4.1. The rectifier, which is used to provide the DC voltage, can be seen as full wave rectifier with 4 diodes. In the model the full wave rectifier is replaced to simplify the simulation. Each diode has a threshold voltage $V_{th,d}$ of 0.7 V. To consider the threshold voltage as well, the limiter voltage V_{lim} has to be increased according

$$V_{lim,tot} = V_{lim} + 2\,V_{th,d} \tag{4.1}$$

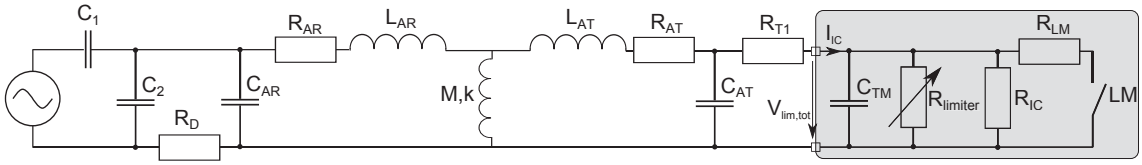


Figure 4.1.: Equivalent network of the RFID system

The limiter structure of the IC is also replaced by an approximation. In the transponder IC itself a control circuit, which changes the conductance of a transistor, guarantees a stable supply voltage. In the Matlab model the limiter is replaced by a variable resistor which is controlled by a loop. The resistor $R_{limiter}$ changes the resistance according to

$$R_{limiter} = \frac{V_{lim,tot}}{I_{IC}} \tag{4.2}$$

till the wanted limiter voltage is achieved. It also assures that the required current I_{IC} is available at the IC. Before the limiter is active the resistance of the limiter also has to be defined to model the current consumption of the IC. Therefore the resistance is set to the operating point, where the limiter voltage would be achieved. The value of the limiter resistor will be seen in the simulation later on.
To decrease the complexity of the simulation handling, and to provide a tool, which can be used by everyone for further simulations, a graphical user interface (GUI) was created. The GUI can be seen in Figure 4.2. The path of the location, where the simulation data are stored, has to be added and the program reads all available data and displays them in the GUI. To calculate a certain setting or parameter, for example a variation of the limiter voltage, the according checkboxes have to be marked and the calculation can be started by pressing the evaluation button.

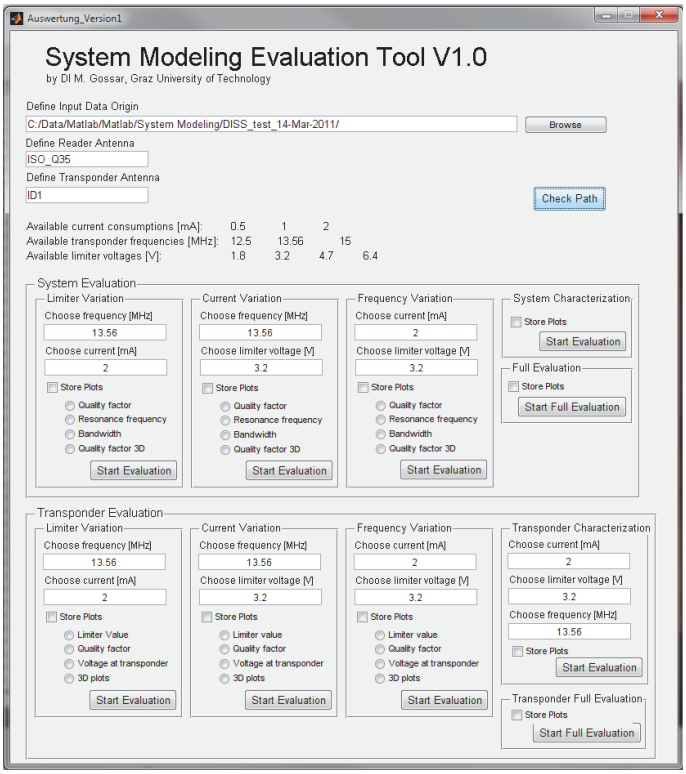


Figure 4.2.: Graphical user interface in Matlab

4.2. Transponder Behavior and Model Description

Since the whole system is very complex, and changes on one part will influence the whole system, the system is separated into two parts. In the first part only the transponder will be characterized to see the influences of different parameters on the transponder. Some parameters will be changed, and the influences will be outlined. The next part will also include the reader and show the influences of the transponder on the system.

4.2.1. Tunable Parameters on the Transponder

On transponder side there are several tunable parameters which can be divided in electrical as well as geometrical parameters.
The geometrical parameters are the antenna size, the position in the system, the distance between the antennas and the material of the conducting path itself as well as the substrate.
To make the system not too complex, the antenna size and material are fixed. The material would change the antenna resistance as well as the capacitor and inductance, as shown in Subsection 3.2.1. Taking into account all those parameters would make the model too complicated, therefore the hardware is fixed, as defined in [38]. The position of the transponder antenna is also fixed, and will only be simulated coaxially. That means the transponder antenna is placed in the center of the reader antenna, and both antennas are always parallel to each other, and the only variation is the distance which influences the coupling factor. There would be the possibility to change the angle between the reader and the transponder antenna, as well as the position in the volume. Those possibilities are neglected, not to increase the complexity. A change of those parameters would result in additional tunable parameters which are only visible in the coupling factor. For the simulations only a distance variation is performed to change the geometric settings.
The electrical parameters are the limiter voltage, the current consumption and the resonance frequency.
The listed electrical parameters will be changed during the simulation. It should be shown which influence different parameters have on the transponder as well as on the whole system.
To start with a low degree of freedom the first observation only varies the distance, to get a basic understanding of the transponder. Later, different parameters, such as limiter value, quality factor e.g. change as well.

4.2.2. Transponder Characterization

In the first simulation, only the distance will be varied. The simulation settings of the reader can be seen in Table 4.1, which are the settings described in [38].

parameter	**value**
reader antenna	ISO Q35
field strength	1.5 A/m
distance	0...25 cm

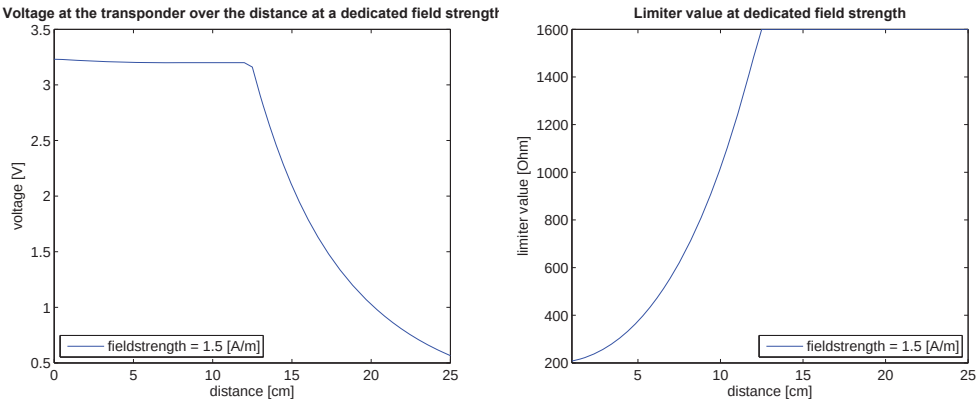
Table 4.1.: Reader parameter

The transponder uses the ID1 antenna of the reference PICC, whose parameters are listed in Table 4.2.
In Figure 4.3(a) the voltage at the transponder can be seen in dependency of the distance between the reader and the transponder. At large distance the voltage which is induced in the transponder is very low but is increasing, when the distance is reduced. Further, it can be seen that the transponder reaches its limiter voltage at around 12 cm. That means in this point the limiter starts working and reduces the resistance of the limiter resistor. The value of the limiter

parameter	value
L_{AT}	2.34 µH
C_{AT}	5.28 pF
R_{AT}	0.65 Ω
f_{res}	13.56 MHz
V_{lim}	1.8 V ($V_{lim,tot}$=3.2 V)
I_{IC}	2 mA

Table 4.2.: Transponder parameter

resistor can be seen in Figure 4.3(b). The plot shows that the value of the limiter resistor is the same as long as the required voltage is not achieved.



(a) Voltage (b) Limiter value

Figure 4.3.: Simulation results at the transponder at a field strength of 1.5 A/m

The resistance for the case no limiter is working is calculated with the limiter voltage and the defined current consumption. As soon as the limiter voltage is reached the limiter reduces its value to stabilize the voltage to the desired level. By reducing the resistance more power is damped by the limiter according to

$$P_{lim} = \frac{U_{lim}^2}{R_{lim}}. \tag{4.3}$$

The reduction of the limiter resistance has an impact on the quality factor of the transponder, which can be seen in Figure 4.4.
The shown plots describe the relation between the voltage, limiter resistance and quality factor. At large distance the voltage induced at the transponder is very low and the limiter is not working. The same time the quality factor is high to boost the energy at the transponder. As soon as the limiter voltage is reached, the voltage at the transponder is stabilized, and the limiter resistance and simultaneously the quality factor are reduced.

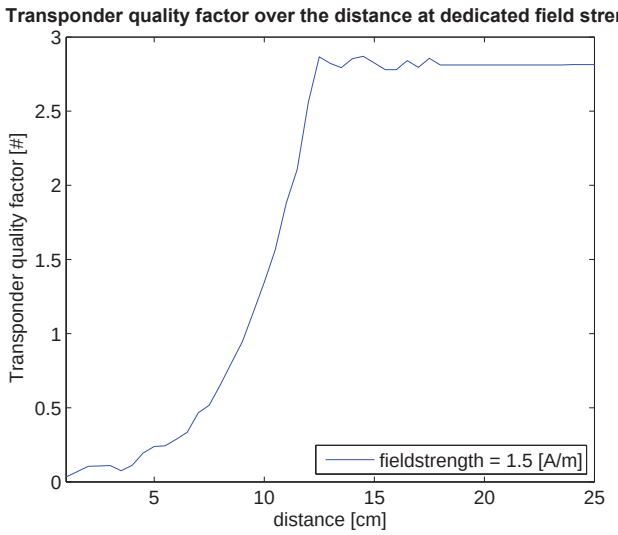


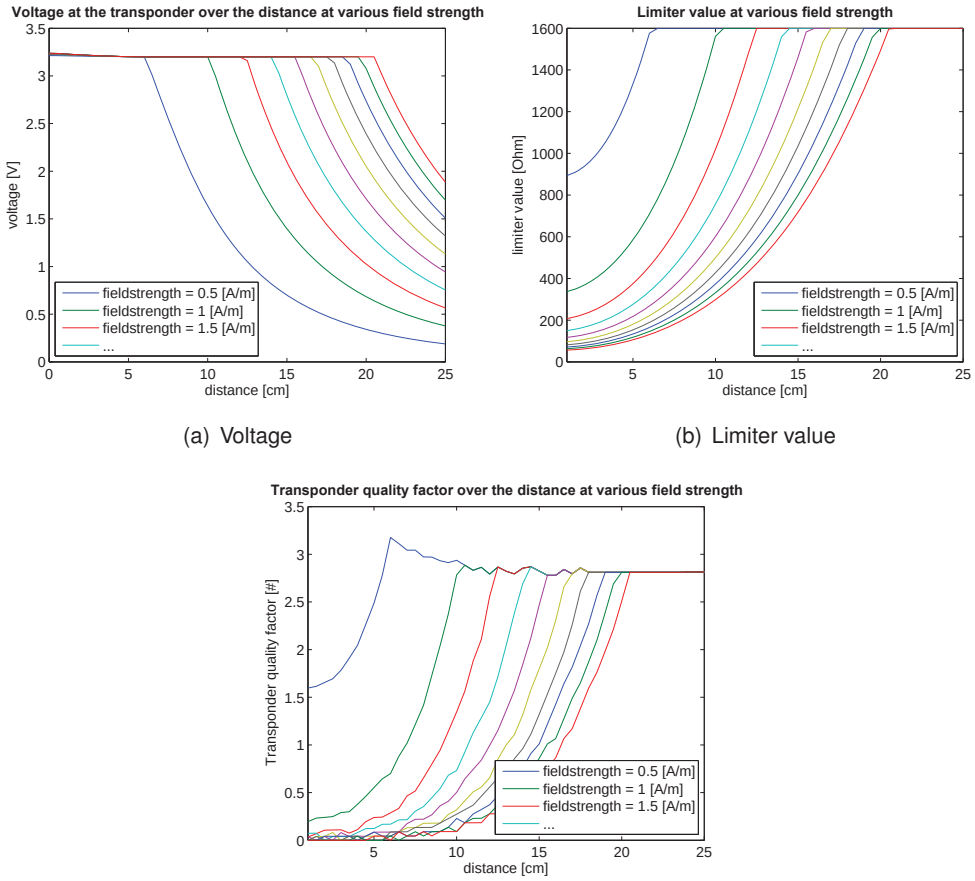
Figure 4.4.: Quality factor of the transponder at a field strength of 1.5 A/m

4.2.3. Transponder Characterization at Different Field Strengths

Now the simulations are enhanced by a field strength variation. In the last chapter, the transponder was only analyzed at one dedicated field strength of 1.5 A/m. Here the field strength will be increased from 0.5 up to 5 A/m. The other settings of the simulations stay the same.
A higher field strength results in a higher available energy at the same distance. This means if a certain energy is required to power the transponder, it can be reached at higher distance. This can also be seen in Figure 4.5(a), where the voltage at the transponder is plotted. It can be seen that the required voltage is achieved at higher distance, if the field strength is increased. Each curve represents the voltage at the transponder at one particular field strength level, starting at 0.5 A/m in steps of 0.5 A/m.
Simultaneously the voltage is achieved earlier, and the limiter also starts to work earlier to stabilize the voltage not to destroy the transponder IC. In Figure 4.5(b) the value of the limiter resistor is plotted which shows the same trend. A higher field strength implies a higher range where the desired voltage of the transponder is achieved.
The reduction of the limiter resistor results in a reduction of the quality factor as well, as plotted in Figure 4.5(c).

4.2.4. Transponder Characterization with Limiter Voltage Variation

The following simulation results are again conducted at a dedicated field strength of 1.5 A/m. In this simulation the limiter voltage V_{lim} will be varied.
Figure 4.6(a) shows the voltage at the transponder in dependency of the distance. It can be seen, that the voltage rises till the limiter voltage is achieved, and the limiter starts working. The value of the limiter can be seen in Figure 4.6(b). Figure 4.6(c) finalizes the plots and shows the quality factor of the transponder in dependency of the distance. All plots show that the limiter voltage is achieved at nearly the same distance of around 12.5 cm. This would mean that the

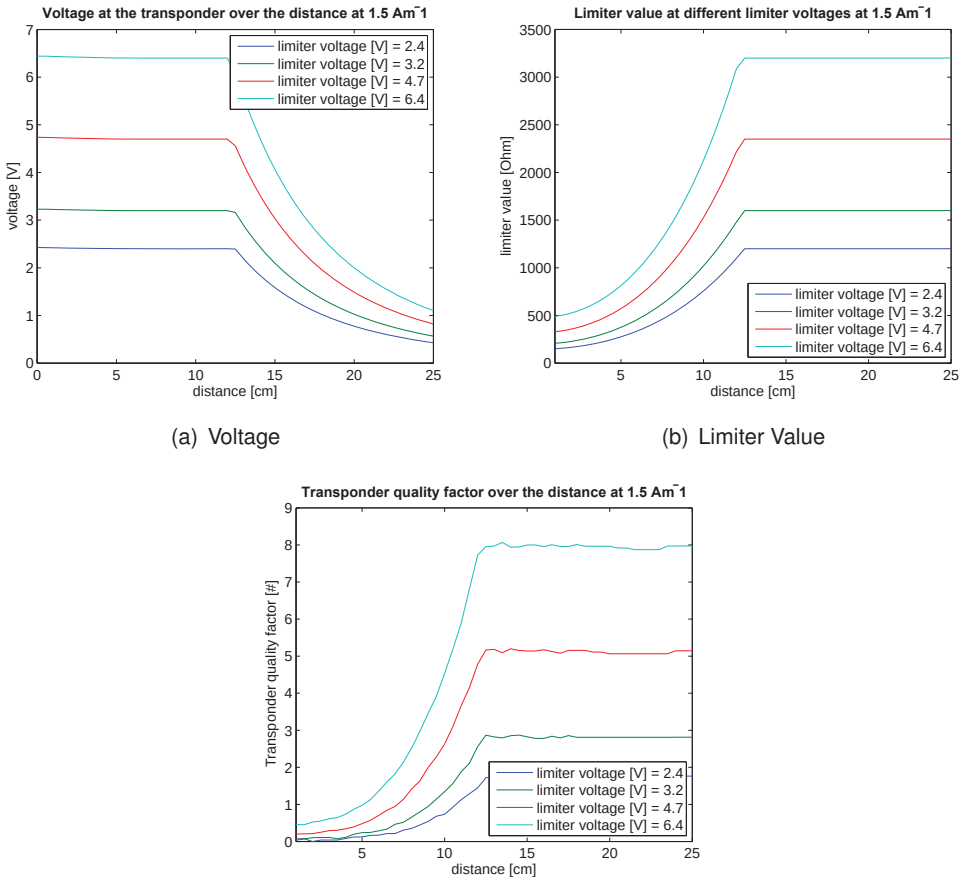


(a) Voltage

(b) Limiter value

(c) Quality factor

Figure 4.5.: Simulation results at the transponder at different field strengths



(a) Voltage

(b) Limiter Value

(c) Quality factor

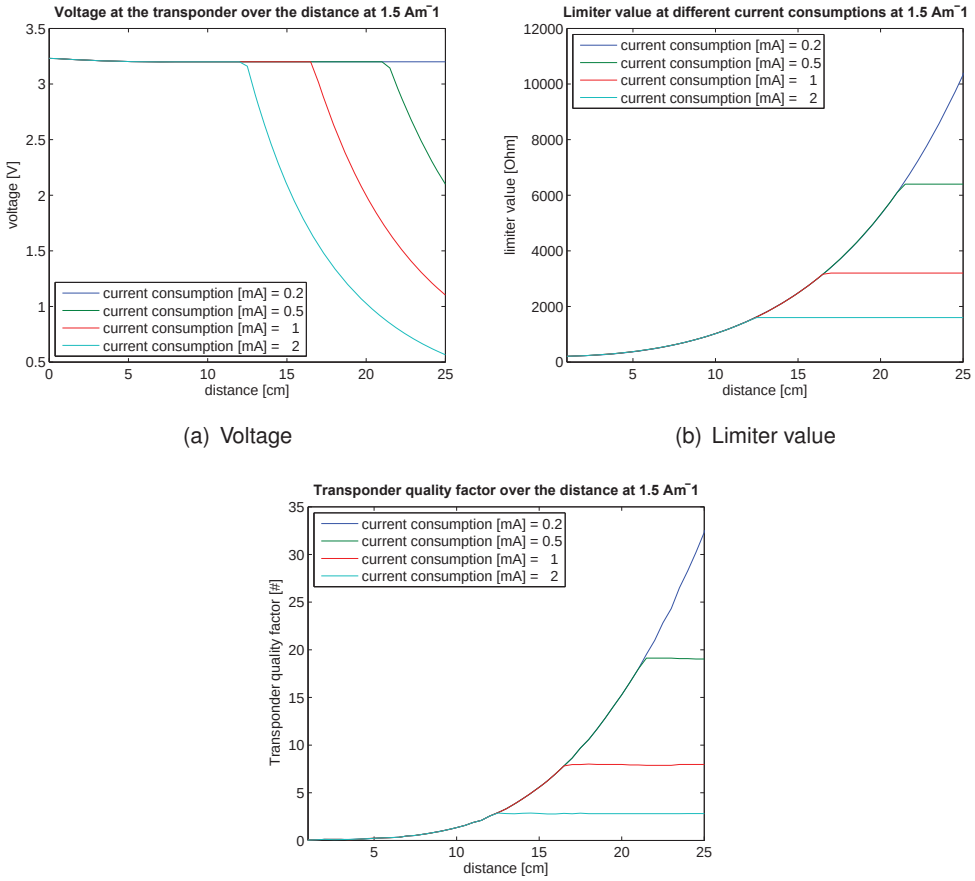
Figure 4.6.: Simulation results at the transponder at different limiter voltages

limiter voltage has no impact on the reachable distance, and can be neglected. This is only partly true, due to the way, how the operating point is defined. By setting the limiter value as well as the current consumption to a specific value, the resistance is calculated, which represents the IC when the limiter is not working. As seen in Figure 4.6(b) each limiter voltage results in another resistance at high distance. The problem is that ICs outside their operating area have no defined resistance. This makes it hard to define a resistance which represents the IC without functionality. Due to the fact that the required voltage and the desired current result in an operating point, this approximation is taken as reference.
Concluding it can be said that the limiter voltage has no impact on the range, where the transponder is powered.

4.2.5. Transponder Characterization with Different Current Consumption

In the last section the limiter value has been varied, which is set again to 3.2 V now. This simulation focuses on the current consumption of the transponder, which will be varied from 200 µA

up to 2 mA. In Figure 4.7(a) the voltage at the transponder can be seen, and it is shown that the limiter voltage is achieved earlier if the current consumption is reduced. According to the same formula for the operating point, the limiter value is calculated with the set voltage and the defined current consumption. This means that the limiter value is increased up to 16 kΩ, which means a very low load, compared with 1.6 kΩ at 2 mA current consumption. The limiter would even be working for a distance of 25 cm with the low current consumption.



(a) Voltage

(b) Limiter value

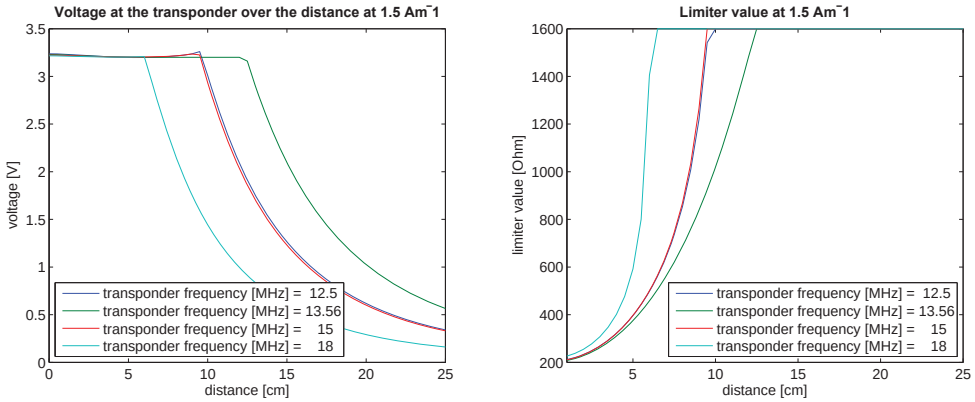
(c) Quality factor

Figure 4.7.: Simulation results at the transponder at different current consumptions

Furthermore, it can be seen that the quality factor is increased dramatically by decreasing the current consumption. By increasing the parallel resistance, the quality factor is increased as well, which results in a higher range due to the fact that a high quality factor is able to harvest more energy.

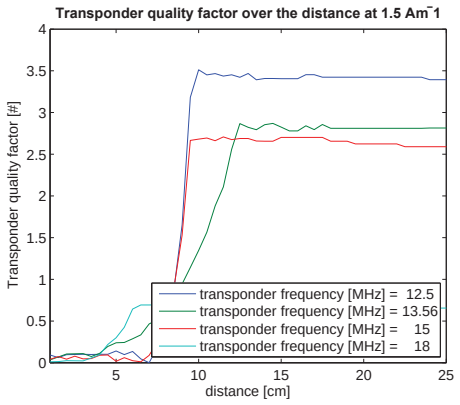
4.2.6. Transponder Characterization with Resonance Frequency Variation

The third and last variation at the transponder will be the resonance frequency. By shifting the resonance frequency of the transponder, the influence on the reader can be changed, as well as the energy range, where the transponder is powered. The current consumption is set to 2 mA and the limiter voltage to 3.2 V again, and the resonance frequency is varied from 12.5 MHz up to 18 MHz. The best performance is achieved by setting the resonance frequency to the carrier frequency of 13.56 MHz. The problem in this case is that the same resonance frequency causes higher influences, and if there is more than one transponder in the field, the resonance frequencies are shifted and it can happen that no card is powered any more. A detailed analysis of this effect can be found in [31].



(a) Voltage

(b) Limiter value



(c) Quality factor

Figure 4.8.: Simulation results at the transponder at different resonance frequencies

Figure 4.8(a) shows the voltage at the transponder. It can be seen that the limiter starts its work at highest distance, if the resonance frequency is set to the carrier frequency. Defining a resonance frequency above or below the carrier frequency decreases the distance, where the limiter is working, resulting in a lower range, where the transponder is powered. The same

behavior can be seen in the limiter value in Figure 4.8(b) and the quality factor of the transponder in Figure 4.8(c).
This makes it clear that the same resonance frequency will lead to the highest distance, but also the highest influence on the reader, as will be shown in the next part.

4.2.7. Transponder Characterization Conclusion

The transponder characterization shows that there are different parameters which have influence on the behavior of the transponder. It is shown in the simulations that from transponder point of view, the best in terms of achievable distance is a high field strength, which has to be provided by the reader. Furthermore the achievable distance can be increased by a low current consumption and a resonance frequency which is very close to the carrier frequency.
Nevertheless only one parameter is tunable, and the other parameters are fixed with the process and the requirements of the IC. The limiter voltage is fixed by the process, which is used to produce the IC. Using the CMOS14 process, which is used within the VHD project for the test IC, the limiter voltage is set to 1.8 V. A higher voltage would harm the transistors of the digital part, and so the voltage has to be limited. The current consumption is defined by the amount of signal processing, and other parts of the IC, such as crypto unit or clock frequency.
The parameter which can be defined is the resonance frequency of the transponder. To achieve the highest distance, the best would be to set the resonance frequency of the transponder to the carrier frequency. On the other hand, using a resonance frequency which is farther away to the carrier frequency reduces the influence on the reader, as will be shown in the next part and is analyzed in detail in [31].

4.3. System Simulation

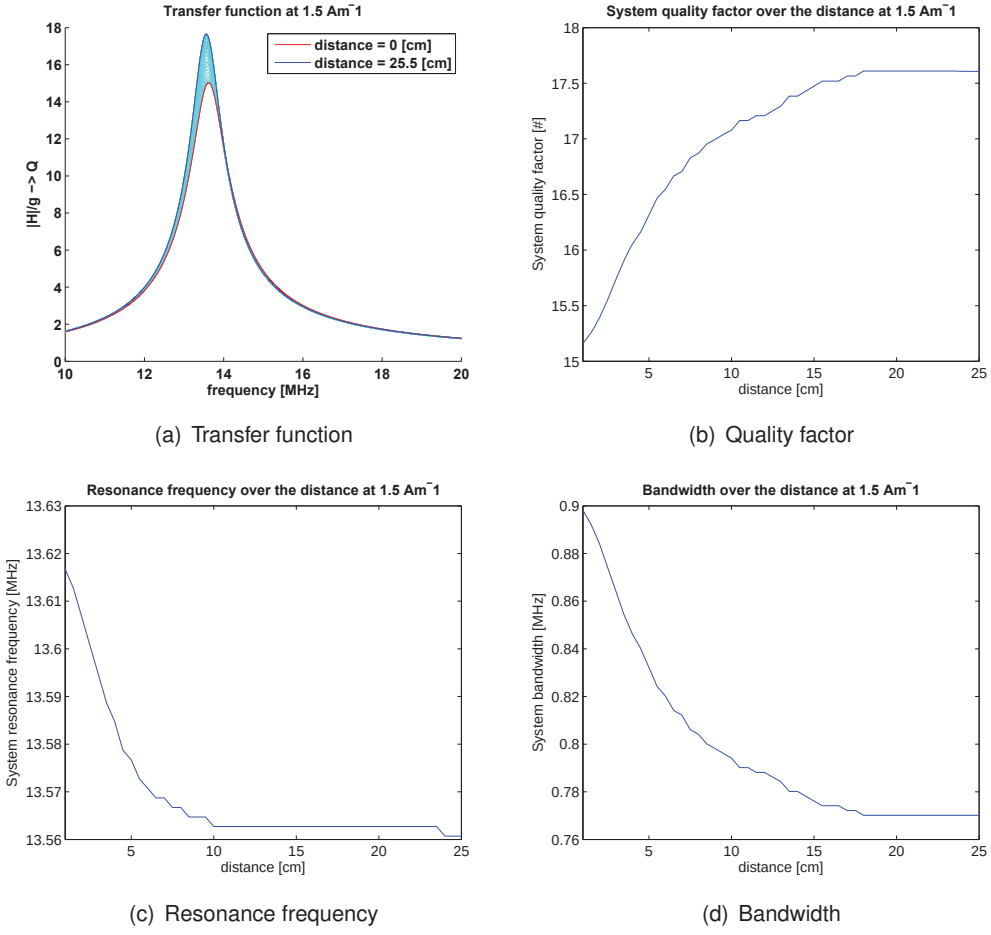
Up to this point the focus of this chapter was on the transponder side, and the effects on the system were neglected. In this part the focus is on the whole system, and the effects of different parameters will be shown. Defining the system, and not the reader, has the reason that the reader is the dominating part in the system according to this setup. Since the interest is not only on the reader, but on the whole system, the characterization will be done for the whole system.

4.3.1. Model Parameters

The model parameters are chosen like defined in Chapter 3, which means that the reader is represented by the ISO setup, with the difference that only the ISO antenna is used, without the other antennas defined in [38].
The transponder settings are like in the first part of this chapter, and depending on the parameter which should be analyzed they will be varied.

4.3.2. Distance Variation

Like in the transponder characterization the reader will also be first analyzed just by changing the distance between the reader and the transponder. As shown in 4.2.2, the transponder changes its limiter and according to that the quality factor in dependency of the distance. The same time the transponder comes closer, it changes its influence on the reader, which leads to a change of the transfer function, as depicted in Figure 4.9(a). The blue line, which is the outermost line of the transfer function, represents the transfer function of the reader when the card is at very high distance, which means it has little influence on the reader. The red line is at a very low distance, and all lines in between, drawn in cyan, represent a dedicated distance, but should only show, how the transfer function changes.



(a) Transfer function

(b) Quality factor

(c) Resonance frequency

(d) Bandwidth

Figure 4.9.: Simulation results of the whole system

It can be seen that the quality factor, which is drawn on the y-axis, is decreasing, if the transponder comes close to the reader. To make it clearer, the quality factor is printed over the distance in Figure 4.9(b). Starting at a quality factor of approximately 17.5, it is reduced to around 15.2 at very low distance. The same time the quality factor changes it can be seen that the zenith of the red curve is shifted to the right in Figure 4.9(a), which means that the resonance frequency of the

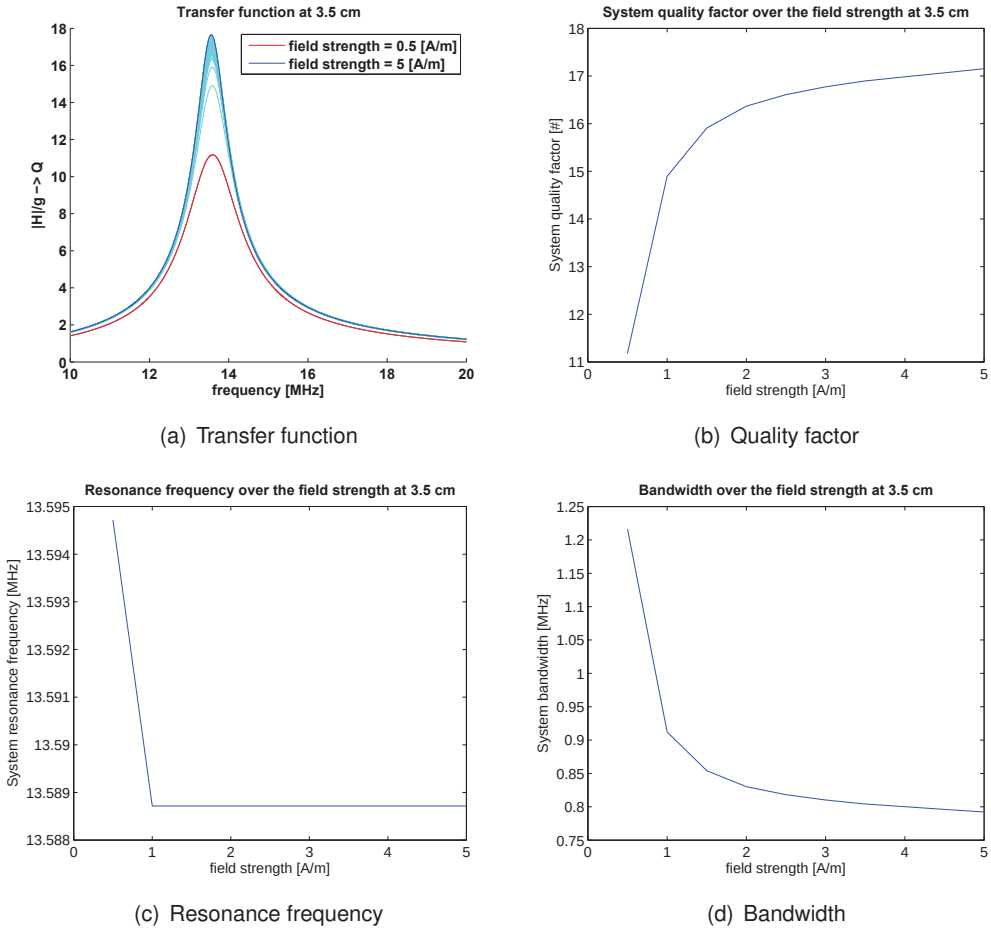
reader has changed. The change of the resonance frequency is depicted in Figure 4.9(c). It is shown that the resonance frequency is increasing, if the transponder comes close to the reader. The same time all those parameters change, the bandwidth of the system changes as well as depicted in Figure 4.9(d). A change of the bandwidth, which goes along with the quality factor and the resonance frequency, means that the channel changes and the signals are influenced in a different way. For the signal processing on the transponder, as well as reader side, it has to be taken into account that the channel changes during the operation. A change of the channel results in different influences on the signal, which are caused by the channel.

4.3.3. Field Strength Variation

In this simulation the distance between the transponder and the reader stays constant at 3.5 cm, and the field strength is varied from 0.5 A/m to 5 A/m. Figure 4.10(a) shows again the transfer function of the system over the frequency. The blue line represents the transfer function at high field strength, and it can be seen that the quality factor is at 17.5 like expected. Decreasing the field strength also decreases the quality factor, according to the detuning caused by the transponder, till it ends in the red line with a quality factor slightly above 11. The reduction of the quality factor is also shown in Figure 4.10(b) in dependency of the field strength. Figure 4.10(c) depicts the resonance frequency of the system and it can be seen that it stays constant over the whole range except for the low field strength of 0.5 A/m, where the frequency is shifted to higher values. The shift of the resonance frequency of 29 kHz is caused by the detuning of the transponder. Since the transponder stays at the same distance, it does not change over the field strength, except for the low field strength values, because the quality factor of the transponder is increased, to gain enough energy, which results in a higher detuning. The detuning is stronger, if the quality factor of the transponder is higher.
In dependency of the quality factor and the resonance frequency, the bandwidth is also influenced as can be seen in Figure 4.10(d). If the field strength is reduced the bandwidth is increased due to the lower quality factor. It is shown that the bandwidth is around 800 kHz at 5 A/m and is increased to 1.2 MHz at 0.5 A/m, the same time the quality factor is reduced from 17.2 to around 11. All plots show that a lower field strength has more influence on the system due to the higher detuning caused by the higher quality factor of the transponder. To make the system more stable and to increase the range where the transponder is powered, a higher field strength is recommended.

4.3.4. Distance and Field Strength Variation

In the last two sections the influence of either the distance between the transponder and the reader, or the influence of different field strengths were analyzed. To get a more understandable view of the system, this section combines the findings. Figure 4.11 shows a three dimensional plot, where the distance as well as the field strength is varied. On the z-axis the quality factor is depicted to show the change of the quality factor, which represents all other influences as the bandwidth and resonance frequency. The worst case can be seen at at low distance of the transponder and a low field strength. In this case the quality factor is reduced to around 8, which would change the channel significantly, compared to a quality factor at higher distance of 17.5.



(a) Transfer function

(b) Quality factor

(c) Resonance frequency

(d) Bandwidth

Figure 4.10.: Simulation results of the whole system

To get a more stable system it would help to increase the field strength from 0.5 A/m to 1 A/m, which would increase the quality factor by 18 % at low distances. The same time the distance can influence the system as well. If the transponder is not able to touch the reader antenna, and the lowest possible distance is increased from 0 to 5 mm, this would results in a quality factor improvement of 16.4 %.
Concluding it can be said that the worst scenario for the stability is a low field strength combined with a low distance between reader and transponder.

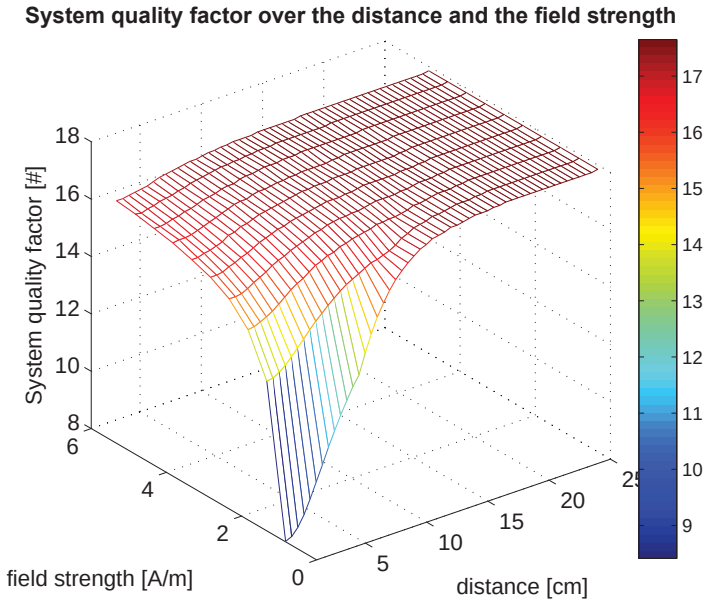


Figure 4.11.: Quality factor at distance and field strength variation

4.3.5. Influence of the Transponder Limiter Voltage

As described in Subsection 4.2.4 the limiter voltage of the transponder is dependent of the process, which is used to manufacture the IC itself. Due to different transponder voltages the influence of the transponder on the reader and the whole system is changed. Figure 4.12 shows a similar plot like in the section before, with the additional different limiter voltages on the transponder. It can be clearly seen that the influence on the system is lower, if the limiter voltage is lower. This is caused by the quality factor of the transponder. All other parameters are the same in all simulations, but due to the lower limiter voltage, the transponder achieves its voltage earlier. As soon as the voltage is achieved, the quality factor of the transponder is reduced, and the influence on the reader is reduced as well. The opposite behavior can be seen in the case with the high limiter voltage of 6.4 V, which results in 5 V at the transponder after the rectifier. The limiter voltage is achieved later, and the quality factor of the transponder is higher. Due to this high quality factor of the transponder, the detuning is much higher, which results in a stronger change of the quality factor.
Concluding it can be said that a lower limiter voltage at the transponder has less impact on the

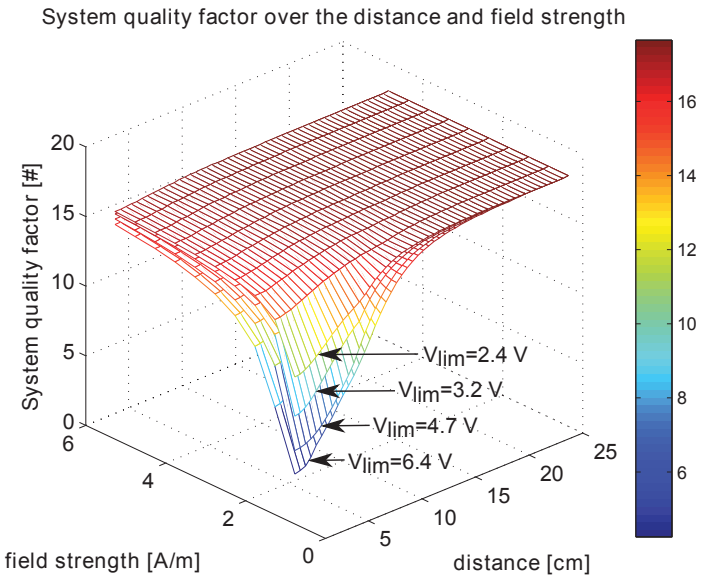


Figure 4.12.: Quality factor at distance and field strength variation

system, due to the lower transponder quality factor, depicted in Figure 4.6(c).

4.3.6. Influence of the Transponder Current Consumption

In this section the current consumption of the transponder is changed. Due to the simulation settings, as described in Subsection 4.2.5 the influence on the quality factor of the transponder is very low, which also results in a very low influence on the quality factor of the system. Figure 4.13 shows the quality factor of the system, and the only difference can be seen at low field strength and a distance between approximately 10 and 25 cm. This means that the influence, according to the simulation, and the way, how the current consumption is modeled, has very low impact on the system.

4.3.7. Influence of the Transponder Resonance Frequency

In this section the transponder resonance frequency is varied, and to make it easier to see the changes, the quality factor is only plotted for one dedicated field strength value. Figure 4.14 shows that the largest impact is caused by a transponder with the same resonance frequency as the reader. Two antennas with the same resonance frequency have the largest impact on each other, which results in the largest detuning and change of the quality factor. Increasing or decreasing the resonance frequency for the approximately same frequency to 12.5 MHz and 15 MHz result in nearly the same influence on the system as shown in the Figure in blue and red. If the difference between the resonance frequencies is increased, the influence on the system is decreased, which is shown in cyan.
Concluding it can be said that the biggest influence can be caused by the same resonance

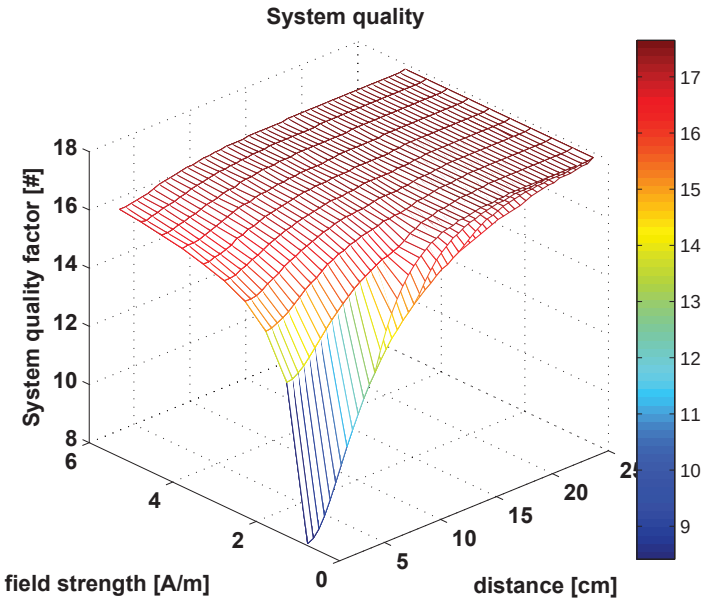


Figure 4.13.: Quality factor at distance and field strength variation

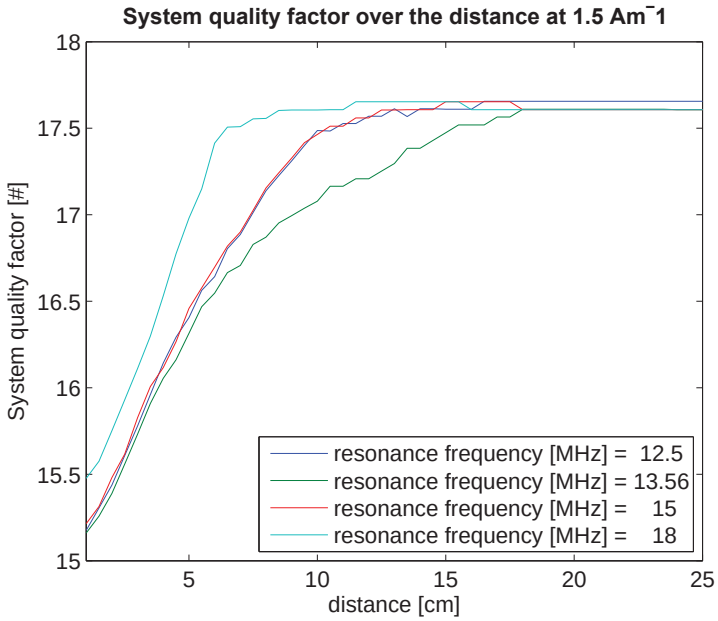


Figure 4.14.: Quality factor at distance variation

frequency, but also leads to the highest range as shown in Figure 4.8(a). A resonance frequency which is farther away from the carrier frequency has less influence, but also reduces the available energy which results in a smaller range, where the transponder is powered.

4.4. Conclusion of the System Modeling

This chapter has shown the influences of different parameters on the transponder as well as the system. Several possible parameters have been changed and the effects were analyzed. From three different parameters on the transponder, the limiter voltage, energy consumption and resonance frequency, only the resonance frequency can be defined freely. The limiter voltage is linked to the process, which is used to produce the IC. This means by defining the physical process, the limiter voltage is defined as well. The current consumption is defined by the functionality of the transponder. Simple transponders which only send their ID need less power than other ones which have complex signal processing as well as a crypto unit on board. Design aims can be defined, but the current consumption is mainly linked to the functionality and the required number of functional blocks on the IC.
The reader has the possibility to define the field strength, which is limited by different regulations and requirements of the application.
It is shown that a higher field strength leads to a more stable system. This is caused by the fact that the limiter resistor on the transponder is active, reducing the quality factor of the transponder. A reduced quality factor on the transponder has two kinds of impact. The first one is that a lower quality factor has less influence in forms of detuning, shifting the resonance frequency of the reader, which results in a stable resonance frequency of the resonance and matching circuits. Second a reduced quality factor results in a wider bandwidth, which has less influence on the signal in forms of inter symbol interference (ISI). Beside those effects a higher field strength results in a higher range, where the transponder is powered.
A lower limiter voltage on the transponder causes the same results as mentioned above, due to the reduction of the quality factor on the transponder.
A lower current consumption leads to a higher powering range, but has little effect on the system at all.
The resonance frequency has impact on the powering as well as the detuning of the system. If the resonance frequency is close to the carrier frequency, the range, where the transponder is powered, is larger, but the detuning influence on the reader is also stronger. A higher resonance frequency means a lower range, but less detuning effects on the system, which is very important for applications where more than one transponder is in the field.
In the end it has to be noticed, that this simulations are mainly thought to show the behavior of the system. Only the powering range is taken into account without any simulation of data. Due to effects of the load modulator, it can happen that the communication is not possible in the whole range, where the transponder is powered.
Table 4.3 summarizes the results from the simulations. In the first column the parameter which is varied is shown. The second column shows the effect on the transponder in terms of powering range. A higher powering range is a better result than a low one. The third column indicates the influence on the reader. A lower change in the quality factor stands for a more stable system which is more desirable.

parameter	Energy range	△ Q System
field strength	3.2 V, 2 mA, 13.56 MHz	
0.5 A/m	6.0 cm	50.3 %
1.0 A/m	12.0 cm	13.9 %
5.0 A/m	20.5 cm	4.1 %
limiter voltage	2 mA, 13.56 MHz, 1.5 A/m	
1.2 V	12.5 cm	5.3 %
3.2 V	12.4 cm	15.2 %
5.0 V	12.25 cm	22.8 %
current consumption	3.2 V, 13.56 MHz, 1.5 A/m	
0.2 mA	25.0 cm	13.9 %
0.5 mA	21.0 cm	13.9 %
1.0 mA	16.5 cm	13.9 %
2.0 mA	12.5 cm	13.9 %
resonance frequency	3.2 V, 2 mA, 1.5 A/m	
12.00 MHz	10.0 cm	13.8 %
13.56 MHz	12.5 cm	13.9 %
15.00 MHz	9.5 cm	13.6 %
18.00 MHz	6.5 cm	12.3 %

Table 4.3.: Parameter comparison

5. Signal Comparison and Special Requirements for VHD

The previous chapters have defined the system in a proper way and lead to the conclusion that a coding scheme would be beneficial, requiring a low bandwidth. As described in [17] and Subsection 1.4.1 different coding schemes are possible for the communication from reader to card, as well as from card to reader. To achieve the wanted data rate of 6.78 Mbit/s, either the current modulation schemes can be extended, or a new modulation scheme can be introduced. In this chapter different approaches are introduced and compared with each other. The content of this chapter is based on [45].

5.1. Communication Reader to Card

To increase the data rate different ways are possible. The simplest way would be to increase the data rate according to the current standard by using ASK. Beside ASK there are also other modulation schemes feasible.
First different modulation schemes will be evaluated theoretically and afterwards measurements will be performed to prove the findings. The required bandwidth and the energy transmission behavior are important parameters which will be compared. Due to the limited bandwidth of the channel, and to reduce ISI, the modulation schemes should have a narrow bandwidth, to guarantee a transmission at low distortion, and furthermore enough energy has to be transmitted to power the transponder. To perform measurements in an objective way, the ISO test assembly as defined in [21] will be used.
According to [44] three different main modulations are possible. ASK, phase shift keying (PSK) and frequency shift keying (FSK). ASK is used in all current systems, and is defined in different standards. The modulated signal is defined as:

$$y_{ASK}(t) = A(t) \cdot cos(\omega t + \varphi), \tag{5.1}$$

where $A(t)$ is the modulated amplitude, $\omega = 2\pi f_c$ is the carrier frequency in radians, t is the time index and φ any phase shift to a reference. This means that the relevant information is in the amplitude, and with the help of different amplitude levels, the information is transmitted.
The second possibility is PSK, where the amplitude is constant and the carrier phase is modulated according to the encoded information as:

$$y_{PSK}(t) = A \cdot cos(\omega t + \varphi(t)), \tag{5.2}$$

here, $\varphi(t)$ is the modulated parameter.
The third main possibility is to change the frequency in dependency of the information, which

should be transmitted. A frequency change results in:

$$y_{FSK}(t) = A \cdot cos(\omega(t)t + \varphi), \tag{5.3}$$

where , $\omega(t)$ is the modulated parameter, which changes the frequency.
To complete the list of different modulation schemes, different forms of combinations, such as ASK/PSK (APK) or quadrature amplitude modulation (QAM) [44] are possible, but due to the higher complexity in the generation as well as demodulation, those modulation schemes will not be used. Independent of the modulation principle, the reader has to transmit sufficient power to allow Smartcard chip operation. Therefore FSK will not be used as well, due to the fact that both resonance circuits are tuned to a certain frequency to transmit enough energy. By changing the frequency, less energy will be transmitted, which leads to problems in powering the transponder.

5.1.1. Amplitude Shift Keying

For current standardized data rates, two different types have to be distinguished, as described in Subsection 1.4.1 and [17]. Independent of the used type, the increase of the data rate is reached by reducing the symbol time.
The on-off keying of Type A codes the symbols by using a certain pause time either in the beginning or middle of the symbol. The pause has a duration between 2-3 µs at the base data rate of 106 kbit/s, which corresponds to a duty cycle of around 33 %. At base data rate, where the symbol lasts for 128 carrier periods, this means a pause time of 40 carrier periods, since a carrier period equals $1/f_c$ s. Increasing the data rate to 848 kbit/s, and keeping the same duty cycle the pause would be reduced to 0.37 µs, which is equal to 5 carrier periods of pause within a symbol duration of 16 carrier periods. Increasing the bit rate to 6.78 Mbit/s, one symbol would last for 2 carrier periods and a duty cycle of 33 % would mean less than a carrier period for the pause time. According to this duty cycle and short symbol time, it will be difficult to detect data.
The next problem is the quality factor of the system, which is used to make the system more energy efficient. If the quality factor is higher, the bandwidth is decreasing and those short changes will be filtered, which makes it very complicated and maybe impossible to detect data and transmit enough energy. Therefore an extension of Type A will not be possible to reach the target data rate.
The coding of Type B differs completely and the amplitude change lasts for the whole symbol duration. That way the amplitude changes in dependency of the data and will last for the whole period. In addition the reduction of 10 % is easier to realize than the short and deeper changes in Type A.
However continuing the trend in decreasing the symbol duration to increase the data rate results in an increase of modulation bandwidth as shown in Figure 5.1. The required spectral bandwidth for a data rate of 1.67 Mbit/s is 3.39 MHz even in the ideal case. Increasing the bit rate up to 6.78 Mbit/s will lead to a bandwidth of 13.56 MHz.
This high bandwidth demand and the limited bandwidth of the system, which is defined by the quality factor, introduces a lot of ISI, which has to be filtered on the transponder. A possibility to reduce the ISI would be to reduce the quality factor, but this will lead to a very inefficient system in terms of energy. Actually only two different amplitude states are used in the communication. Another way to increase the data rate would be to define several amplitude levels within a symbol. In the current standard only two different levels are defined, which results in an information

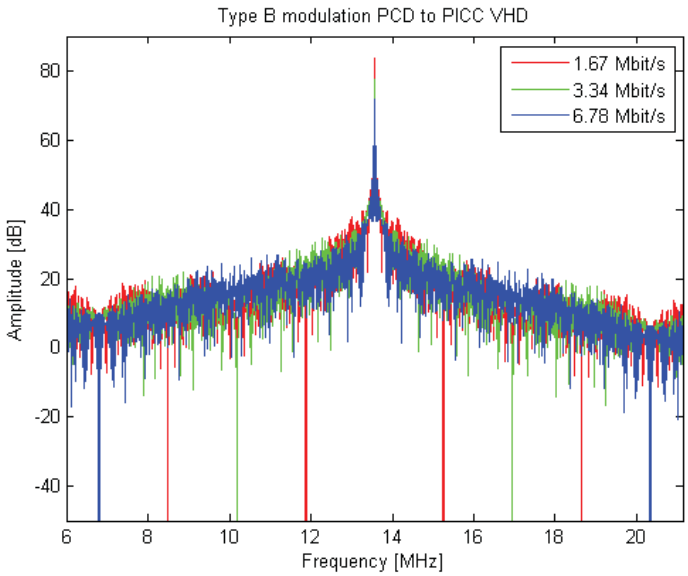


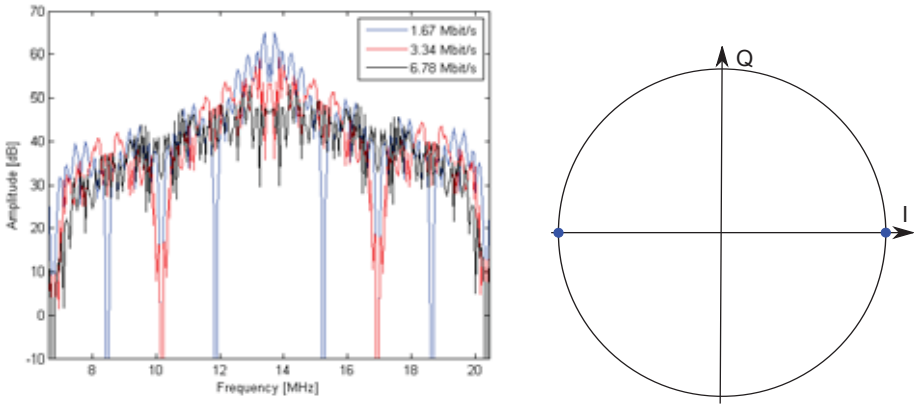
Figure 5.1.: Frequency spectrum of Type B method at VHDR

of only one bit within one symbol. Defining more amplitude levels would allow to transmit more bits within one symbol, which results in a higher data rate without increasing the bandwidth.
The problem of this innovation will be that any state-of-the-art Smartcard has an integrated voltage limiter. This limiter is used to regulate the internal supply voltage of the card, e.g. for the power domain of the digital part. That way the regulation of the voltage will compensate the modulated amplitude levels in dependency of the distance and field strength, which will lead to a compensation of the different amplitude levels. This compensation will lead to a negative impact on the correct level detection, which means that multi level ASK will not be a good solution to increase the data rate.
In case that the increase of the data rate should be realized with ASK, it is obvious that the best solution would be to use Type B. Type A would result in pause times less than a carrier period, which will not be realizable, and a multi level ASK will be distorted by the on board limiter on the transponder. Since the best choice for ASK would be Type B, this modulation scheme will be used for measurements.

5.1.2. Phase Shift Keying

Although all products and standards at the moment are based on ASK, PSK modulation could be used in RFID systems as well. Furthermore PSK has some advantages in RFID systems, since the phase information is less distorted by the transponder and the on board limiter structure than the amplitude. This allows to use more than 2 phase states to encode data, which enables more than 1 bit per symbol for transmission. The advantage of more bits per symbol is that the data rate can be increased without increasing the required bandwidth the same time. Figure 5.2(a) shows the spectrum of a PSK modulated signal at different data rates. To achieve the wanted data rate, the symbol duration has to be reduced as well as in the ASK. Figure 5.2(a) shows

the spectrum of the 2 PSK at different data rates. Like in ASK, it can be seen that the required bandwidth is increasing, by increasing the data rate. The problem in this case is the same like at



(a) Spectrum (b) Constellation

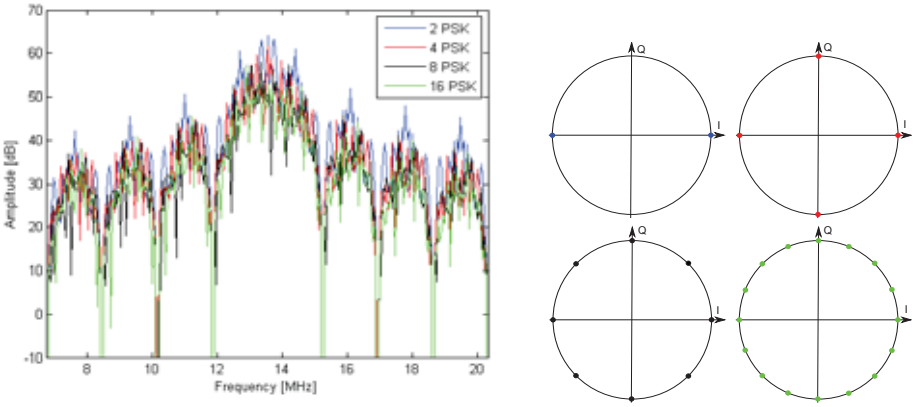
Figure 5.2.: 2 PSK at data rates up to 6.78 Mbit/s

ASK. The required bandwidth is increased by increasing the data rate, which will lead to ISI. The advantage in the PSK modulation is that the bandwidth restriction can be avoided by using more phase states, instead of reducing the symbol time.
Table 5.1 lists different options which are possible to achieve the wanted data rate of 6.78 Mbit/s. One way would be to reduce the symbol time and keep the same PSK order (along one column) as shown above. The better choice is to keep the symbol duration constant and increase the order of PSK (stay in a row). Both ways achieve the target bit rate at different ways.

symbol time	2 PSK	4-PSK	8-PSK	16-PSK
8/fc	1.67	3.34	5.09	6.78
4/fc	3.34	6.78		
2/fc	6.78			

Table 5.1.: Selected VHD data rates using PSK modulation

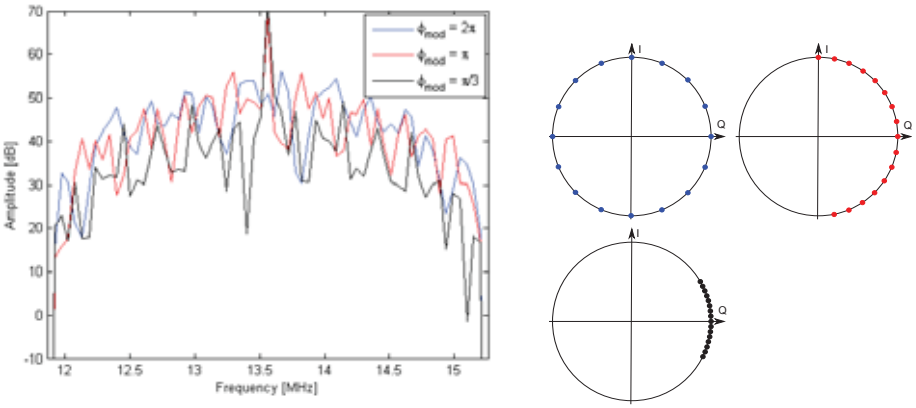
Figure 5.3(a) shows the increase of the data rate by keeping the symbol duration constant, but increasing the order of PSK instead (moving along a row in Table 5.1). This leads to an increase of the data rate, at the same bandwidth, as shown in the Figure. By increasing the order of PSK, the required bandwidth is lower compared to ASK or 2 PSK with only one bit per symbol at the same bit rate. The same time the number of constellation points in Figure 5.3(b) is increased up to 16 points at the 16 PSK. This also means that the distance between the possible points is decreasing, which will lead to a higher required signal to noise ratio (SNR) to detect the signal.
By comparing Figure 5.1 and Figure 5.3(a) it can be seen that there is not a peak at the carrier frequency f_c in the PSK spectrum. The problem is that this peak is needed to transmit sufficient energy to the transponder. Without this peak the radiated power has to be increased to achieve the required energy, which will lead to violations of the spectral mask. Another way to transmit enough energy is to reduce the interval of possible modulation angles of the phase mod-



(a) Spectrum (b) Constellation

Figure 5.3.: Different PSK orders at data rates up to 6.78 Mbit/s

ulation. This means that the symbols are not mapped to the whole circle any more but rather to a segment, which is shown in Figure 5.4(b). A reduction of the modulation angle interval will lead to changes in the spectrum, which leads to a peak at f_c, which is shown for the 16 PSK at 6.78 Mbit/s, for three different modulation angles in Figure 5.4(a).



(a) Spectrum (b) Constellation

Figure 5.4.: 16 PSK at phase modulation angles at 6.78 Mbit/s

Figure 5.4(a) shows that the carrier is not present for a modulation angle of 2π, but as soon as the modulation angle is reduced, the carrier gets a dominant part in the spectrum. This peak at the carrier frequency is used to transmit the required power to the transponder, without violating the spectral mask. Using an angle smaller than 2π the energy transmission of the PSK can be guaranteed, which will also be shown in the measurements later. The drawback of this scenario is that the SNR has to be increased again, since the constellation points are very close together, and effects like phase noise could cause communication errors.

5.1.3. Comparing ASK and PSK

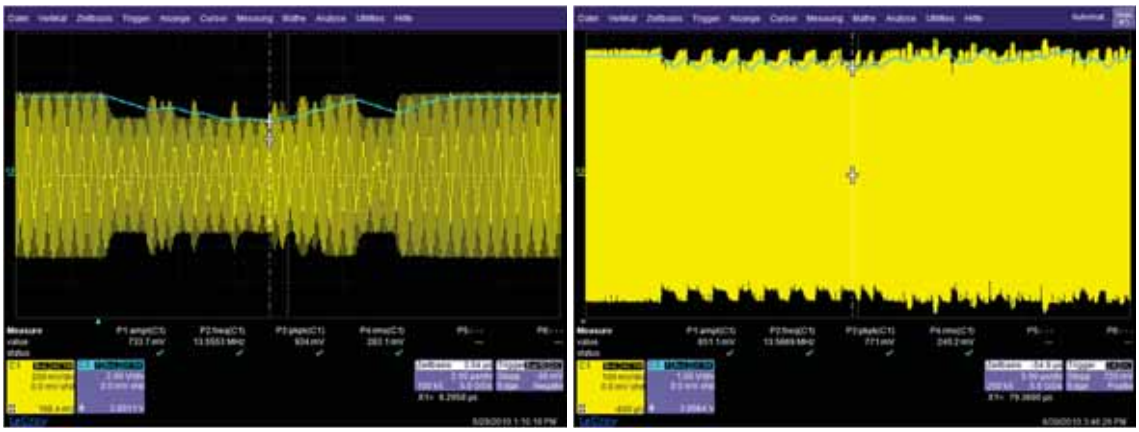
The previous sections show that both modulation schemes will be possible, either ASK or PSK. To compare them with each other, one parameter can be the required bandwidth. It is possible to transmit the data at lower bandwidth as well, but this will lead to ISI, which will cause errors in the communication [44]. The bandwidth comparison in Table 5.2 shows that the bandwidth of the 2 PSK is increasing at higher data rate. The same trend can be seen for ASK, while the required bandwidth for higher order PSK stays the same. The number before the bandwidth in the M-PSK case indicates the order of PSK. According to Table 5.2, a higher order PSK has a lower bandwidth than ASK or 2 PSK at the same data rate.

datarate	ASK	2 PSK	M-PSK
3.34 Mbit/s	6.78 MHz	6.78 MHz	4: 3.39 MHz
5.09 Mbit/s	-	-	8: 3.39 MHz
6.78 Mbit/s	13.56 MHz	13.56 MHz	16: 3.39 MHz

Table 5.2.: Required bandwidth of different modulation schemes

5.1.4. Energy Transmission Measurements

Since all findings so far are only theoretical, a measurement should show the performance in terms of energy transmission in real environment. Therefore energy transmission measurements are performed on the ISO test bench with a low quality factor. A lower quality factor makes the system more energy inefficient, but increases the available bandwidth, which decreases the ISI due to the lower time constant which allows fast signal changes. Furthermore, only the H-field strength is measured, and so it does not matter how much energy is needed to drive this field strength, since this parameter is not taken into account.
As transponder the reference PICC is used, which is described in [21], and the energy transmission is measured on the transponder. The resonance frequency of the card is tuned to 15.5 MHz and the load of the card is fixed to 3 kΩ. The reference card does not have a limiter, therefore a resistor is used to simulate a certain current consumption. The setup is the same for ASK and PSK modulation. The test condition of the measurement guarantees that the voltage at the card is $\geq$ 3 VDC during the whole communication.
The measurement will be performed at 6.78 Mbit/s. Screenshots of the measurement are depicted in Figure 5.5 (a) and (b). Both figures show the H-field of the air interface, as well as the DC voltage on the transponder after the rectifier. The H-field is represented by channel C1, in yellow, which is defined in the lower left corner. The voltage of the transponder is plotted in blue at channel C3. The ASK modulation can be found in Figure 5.5(a) and shows the Type B Request for a data rate of 6.78 Mbit/s. It can be seen that the voltage level of the transponder is decreasing during the modulation, and afterwards rises again. This is an indication that the energy supply is not that good during the communication as when the field is unmodulated. Figure 5.5(b) shows the same measurement with a 16 PSK modulation. Again it can be observed that the voltage level is decreasing during the communication but not that strong as in the ASK case. It also has to be noticed, that the scaling in both pictures is not the same. The PSK has a smaller scaling,



(a) ASK (request B) (b) PSK (start of frame)

Figure 5.5.: Voltage measurements for the reader to card communication

which means that the same change of the amplitude would be seen twice as large as in the ASK case.

modulation	**required field** [A/m]	**voltage drop** [%]
ASK	1.027	32
PSK	0.79	10

Table 5.3.: Measurement results for ASK and PSK at 6.78 Mbit/s

Comparing both voltage levels shows a significant lower voltage decrease for PSK modulation. The measurement results are summarized in Table 5.3. It can be observed that the required field strength for the ASK modulation is 23 % higher than for PSK modulation, assuming that the voltage level at the card has to stay ≥ 3 VDC. Furthermore the voltage drop is 3 times smaller for PSK modulation than for ASK. This trend shows that the PSK modulation has a better performance than the ASK modulation in terms of required field strength as well as voltage stability.

5.1.5. Conclusion

To conclude the findings for the communication from reader to card, it has to be said, that it is obvious that PSK is more suitable than ASK, due to several reasons. It has been shown that the bandwidth requirement for higher order PSK is lower than for 2 PSK or ASK. The advantage is that higher order modulation is possible, due to the fact that the transponder and the limiter structure on the transponder have less influence on PSK than on ASK. A multi level ASK will not be possible due to the limiter structure on the transponder. The required H-field is lower in case of PSK than ASK and the voltage stability is also better than in the ASK case.
The only drawback of this scenario is that both, the transmitter as well as the receiver, need

further adaptations. The reader has to have the possibility to transmit PSK signals, which is not that hard to implement, but the transponder has to demodulate PSK modulated signals which requires a completely new design of the receiver at the transponder, compared to current products. Furthermore, to stay backwards compatible, both receivers have to be implemented to demodulate ASK as well as PSK, which makes the concept more complicated. Nevertheless, the measurements show that PSK has some major advantages.

5.1.6. ISO Proposal

Based on the findings from this chapter, an ISO proposal was written, which proposes the enhancement of the current ISO 14443 standard to very high data rates up to 6.78 Mbit/s. The complete proposal can be found in Appendix A. Here only the proposal for 6.78 Mbit/s is listed. A change from ASK to PSK is proposed and also channel coding is introduced, which is expressed in Figure 5.6.

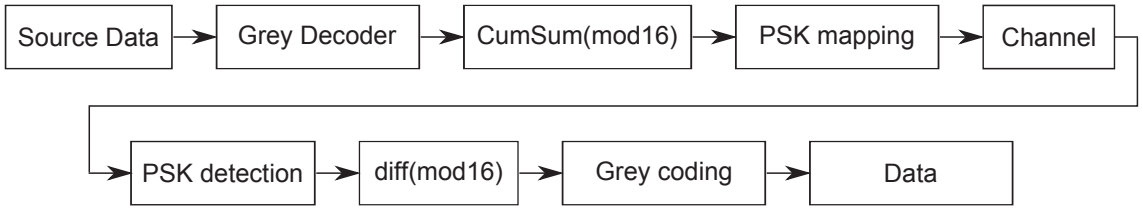


Figure 5.6.: Proposed signal path for transmission reader to card [46]

The source data are grey decoded. This means that the source data are decoded, assuming they are grey coded. This has the advantage that the transponder can encode the grey data, which is less power consuming than the decoding. It does not matter if the data are first coded and then decoded, or the other way round. This simple change of the coder and decoder leads to a reduction of processing power on the transponder. The data are now transformed by

$$out(n) = (out(n-1) + in(n))\text{mod16} \tag{5.4}$$

where $out(n-1)$ is the last output symbol of the coder, $in(n)$ the current symbol which should be transmitted and $out(n)$ the current output, that will be transmitted. This means that only the difference between the current and the last symbol is transmitted. This symbol (cumsum out) is now mapped to the correct constellation point according to Table 5.4 and transmitted.
On the transponder side the symbols are first detected, the difference is calculated to obtain the actual symbol and the grey coder is used to get the original data.
Furthermore, a preamble is defined to calculate filter coefficients on the transponder, which will be explained in 7.3.1. The submitted ISO proposal can be found in Appendix A.

5.2. Communication Card to Reader

For the communication from card to reader other requirements are valid than for the communication from reader to card. The transponder is powered by the field of the reader, and so it has

Phase state	Cumsum out 16 PSK
$\phi_0 + 32°$	0000
$\phi_0 + 28°$	0001
$\phi_0 + 24°$	0010
$\phi_0 + 20°$	0011
$\phi_0 + 16°$	0100
$\phi_0 + 12°$	0101
$\phi_0 + 8°$	0110
$\phi_0 + 4°$	0111
ϕ_0	1000
$\phi_0 - 4°$	1001
$\phi_0 - 8°$	1010
$\phi_0 - 12°$	1011
$\phi_0 - 16°$	1100
$\phi_0 - 20°$	1101
$\phi_0 - 24°$	1110
$\phi_0 - 28°$	1111

Table 5.4.: PSK mapping for 16 PSK

too less energy to transmit its data active. The communication from card to reader is passive, and is performed by changing the impedance of the card. These changes influence the reader field, which allows the reader to receive data from the card. The problem of this modulation is that only two states are available, either the circuit is loaded or not. Furthermore the load of the field depends on the coupling factor, the distance, the required voltage on the transponder and many more effects.
The following chapter will compare different possibilities to transmit data from the card to the reader, which have to fulfill different requirements.

5.2.1. Requirements for the Modulation from Card to Reader

The load modulator consists of a transistor which changes its conductance in dependency of the data. The problem of the design is that during the modulation, where the load modulator is turned on, the transponder is not able to harvest any energy from the field. This means that the transponder has to be powered by an internal capacitor during the modulation. In general there are two possibilities. Either the capacitor is large enough to guarantee the power supply during the whole communication from card to reader, meaning for a whole frame, or the duty cycle of the signal is smaller or equal 50 %. To make the capacitor that large that the transponder is able to transmit a whole frame without additional power would result in a very large capacitor, which requires a large area, resulting in higher costs.
Furthermore, the bandwidth of the signal has to be as small as possible due to the limited bandwidth of the channel, and the pattern should be as easy as possible, since the energy for signal processing is limited.
Taking into account the current ISO 14443 standard, the modulation pattern are the same for data rates from 212 kbit/s up to 848 kbit/s. At a base data rate of 106 kbit/s two different modulation

pattern are available. Type B is only using a so called BPSK. Here it has to be mentioned that the term subcarrier frequency does not mean a subcarrier in the classical sense. Within the RFID community, working with the ISO 14443 and related standards the term subcarrier as well as PSK modulation has another meaning which has been adopted over the years. The subcarrier frequency describes the frequency, used to switch the load modulator within a symbol. As already depicted in Subsection 1.4.1, Type B controls the load modulator with a certain frequency, which is called the subcarrier frequency. Furthermore the term PSK refers to the way, how a bit is represented. Till now there was no PSK modulation in the classical sense in RFID systems, therefore there was no confusion, using PSK in another way. In this thesis the PSK modulation for the communication from reader to card is introduced, meaning the classical PSK modulation. Using the term PSK modulation for the communication direction from card to reader means the way how a bit is represented. Either the modulation starts with a high or low state of the load modulator. In the definition of this standard this can be seen as PSK, since the modulated bit is inverted, or shifted by 180 degrees. In Type B this means that it can be distinguished which symbol is transmitted by detecting if the symbol starts with a high or low state. Type A has either a modulation of the symbol in the first or the second half and the receiver is searching for the subcarrier.
Due to the well established term PSK for the way how the bit is represented for the load modulation, this term is used here as well.
Higher data rates from 212 kbit/s to 848 kbit/s only use Type B modulation. This means that the symbol is modulated by the subcarrier frequency, but the symbol time is reduced. Starting with 16 subcarrier periods in a symbol at 106 kbit/s, 8 for 212 kbit/s and ending with 1 subcarrier period within a symbol. That way this modulation scheme cannot be increased any further, except for increasing the subcarrier frequency. The next subchapter will compare different approaches to each other and evaluate them.

5.2.2. Possible Modulation Patterns

An increase of the data rate can be achieved by reducing the symbol time, which results in an increase of the subcarrier frequency. This is shown in Table 5.5. Extending the data rate the same way as in Type B, the subcarrier frequency is increased to half of the carrier frequency. Assuming 2 PSK would mean that one carrier period is modulated and the other one unmodulated. The resulting pattern is shown in Figure 5.7(a). The low symbol duration will result in a very high

subcarrier frequency [MHz]	**2 PSK** [Mbit/s]	**4 PSK** [Mbit/s]	**8 PSK** [Mbit/s]
fc/16	0.848	1.695	2.543
fc/8	1.695	3.39	5.085
fc/4	3.39	6.78	10.170
fc/2	6.78		

Table 5.5.: Possible modulation patterns

bandwidth again. That way the required bandwidth would be 27.12 MHz at 6.78 Mbit/s. To reduce the bandwidth 4 PSK could be used instead of 2 PSK. Here again the term PSK is used due to

the long history of this term in this community. 4 PSK can be explained by a high and low state of the same length, which is shifted by 90 degrees for each new symbol. The advantage of this way is that the bandwidth is halved, and there are at least always two carrier periods with the same state, which makes it easier to detect the signal. The patterns which are used are depicted in Figure 5.7(b).
A higher order PSK is also possible in theory, but would also make the demodulation more complicated, due to the higher amount of possible states, which have to be separated. An advantage from 2 PSK to 4 PSK can be seen, but a decrease in performance going to 8 PSK (Figure 5.7(c)) occurs.

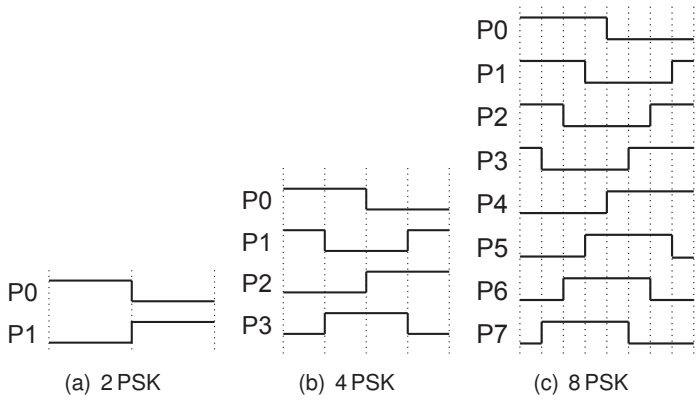


Figure 5.7.: Modulation patterns

Another proposal from another company introduces several patterns which are not coded in the classical style as shown in Figure 5.7. They propose to use the same symbol length at all different data rates, but increase the number of possible patterns to increase the data rate. The problem of this scheme is that the duty cycle of 50 % cannot be guaranteed any more. The patterns are shown in Figure 5.8. It can be seen that the first 4 patterns are the same like in Figure 5.7, but

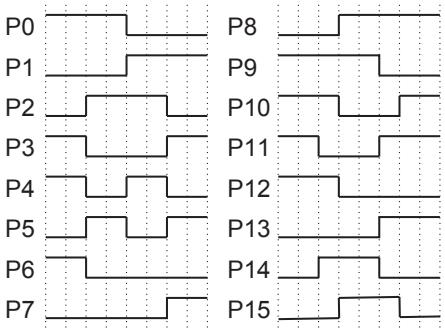


Figure 5.8.: Alternative patterns

to reach 6.78 Mbit/s the number of patterns has to be increased to 16. With 8 patterns plotted in Figure 5.7(c) only 5.085 Mbit/s can be reached. This means to achieve the required data rate, 16 patterns are needed, but the symbol duration is kept constant with 8 carrier periods. The following section will compare the proposed patterns in terms of bandwidth and other parameters.

5.2.3. Signal Comparison

In the following section the different modulation schemes presented in Subsection 5.2.2 will be compared with each other. For that purpose different parameters are taken into account at a data rate of 6.78 Mbit/s. For the comparison it has to be mentioned that for 8 PSK, the data rate differs from 2 and 4 PSK. Due to the number of 8 patterns and the related 3 bits per symbol which are transmitted, the achievable data rate with 8 PSK is 5.085 Mbit/s instead of 6.78 Mbit/s. This means that the data rate, which is used to compare the 8 PSK with the other modulation schemes is lower. This also means that at the same performance the other signals shall be preferred, due to the higher data rate.

Number of Bits

The order of the PSK m defines the number of patterns which are used to transmit data. The number of bits n transmitted with the PSK can be calculated with Equation 5.5.

$$n = \log_2(m) \tag{5.5}$$

The alternative patterns can be seen as code with 16 states, which transmit 4 bits, due to the fact that not all possible patterns are used. 8 PSK means 3 bit per symbol, 4 PSK results in 2 bit and 2 PSK in 1 bit per symbol.

Duty Cycle

The first parameter which will be mentioned is the duty cycle. To power the transponder the load modulator control signal has to have a duty cycle of 50 % or lower. The patterns in Figure 5.7 have a fixed duty cycle of 50 %, while the patterns of Figure 5.8 have a duty cycle of up to 62.6 %, which will lead to problems in the energy supply of the transponder.

Hamming Distance

One important aspect is the minimum Hamming distance (d_{min}) [44]. The Hamming distance defines the number of positions which are different between two code words of the same length. It can also be expressed as the number of bits, which have to be changed to generate one code word from another one. If the Hamming distance is larger, the code is more robust in terms of error stability, since a wrong bit does not lead to a detection error. For example a code consists of 3 symbols, and each symbol has 3 bits:

$$x = 001$$
$$y = 011$$
$$z = 110$$

To generate y out of x one bit has to be changed which results in a Hamming distance of 1. To generate z out of x or y two bits have to be changed which results in a Hamming distance of 2. The most interesting distance is the smallest possible Hamming distance, since d_{min} is the

weakest part in the code and a measure of the code robustness. If the Hamming distance is 1, a wrong detection of a single bit can lead to another valid codeword, which would result in a transmission error. If the Hamming distance is 2, a single error would result in a wrong code word, which can be detected. Therefore it is better to increase the Hamming distance if possible. Calculating the Hamming distance for the patterns shown in Figure 5.7 and Figure 5.8 will lead to a Hamming distance of 2 for all patterns in Figure 5.7 (2, 4 and 8 PSK). Comparing the code in Figure 5.8 will lead to a Hamming distance of 1, which is caused for example by the comparison of pattern P0 with P8, P1 with P9 and P2 with P14 and so on.
Even if the code is not used in the sense of hamming coded signals in general it is a measurement of the robustness of a code. If there are more differences within two code words it is easier to detect the right symbol. This means that the modulation patterns from Figure 5.7 should be preferred due to the higher Hamming distance.

Bandwidth Requirement and Root Mean Square Error

To compare the bandwidth of the signals for a random bit sequence, a Matlab model was created, which provides a bit stream with the different modulation patterns.

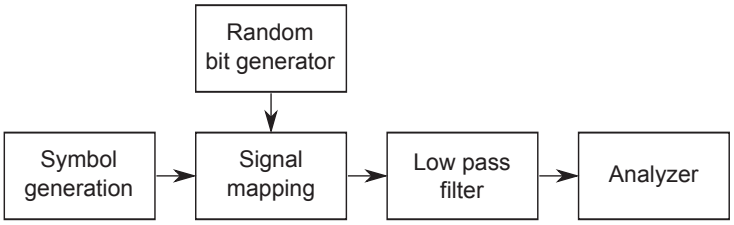


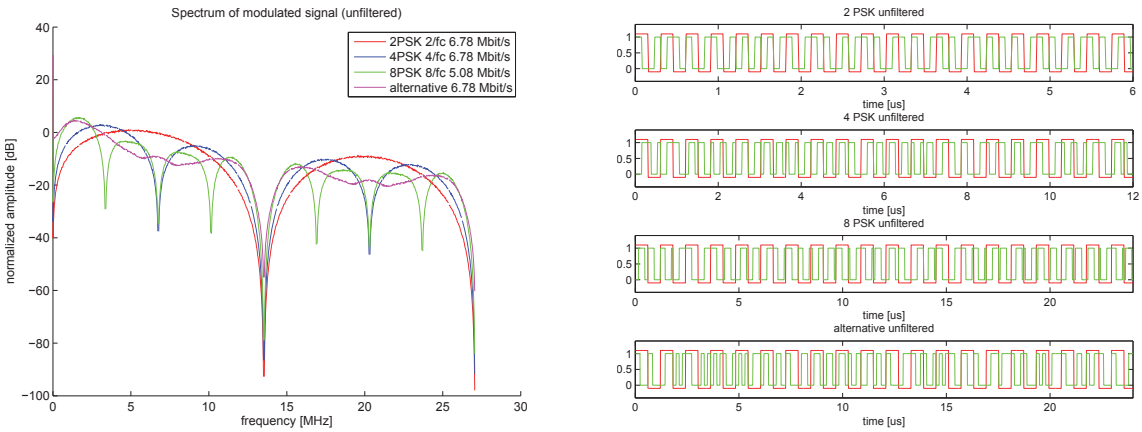
Figure 5.9.: Matlab simulation chain

The structure of the simulation is depicted in Figure 5.9. The first block ”Symbol generation” provides a mapping table where the shape of the patterns is defined as depicted before. In the block ”Signal mapping” the randomly generated bits are mapped to the patterns according to the mapping table. To simulate the bandwidth restrictions a low pass filter limits the bandwidth with a high order low pass filter to get sharp edges. The low pass filter is used to simulate the bandwidth restriction of the channel. Instead of converting the signal in the pass band by mixing with the carrier frequency, the simulation is done in the base band by filtering with a low pass filter, resulting in the same effects according to [47]. In the last block the signal is analyzed to get the spectrum of the different signals, to compare the required bandwidth. Furthermore the originally sent and the received signals are compared to calculate the root mean square error (RMSE) which indicates the difference between the two signals. If the signals are the same the RMSE is 0, a higher number indicates differences between the signals, but has no indication if they are phase shifted, inverted or distorted in any other way. The RMSE is calculated by

$$RMSE = \frac{1}{N} \cdot \sum_{n=0}^{N} \sqrt{\left(S_{(RX)_n} - S_{(TX)_n}\right)^2} \tag{5.6}$$

Figure 5.10 shows the spectrum of the different patterns with random data as described above. It can be seen that the first zero for 2 PSK is at 13.56 MHz, while the first zero of 4 PSK is already

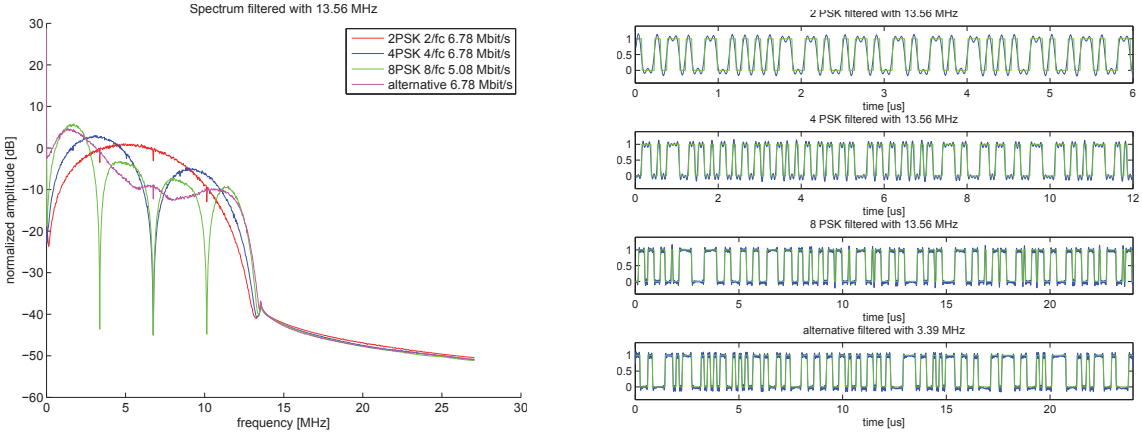
at 6.78 MHz. Increasing the order of PSK to 8 PSK the required bandwidth is only 3.39 MHz. The spectrum of the alternative pattern looks very different from the others due to the fact that the duty cycle is not constant. The zero is at 13.56 MHz, but there are ditches earlier as well. To see the modulation signal, Figure 5.10(b) shows the signal in green, and additionally a red signal which indicates a new symbol. There it can be seen that the 2 PSK only consists of the two patterns described before and the higher order PSK and alternative accordingly more.



(a) Spectrum (b) Time domain signal

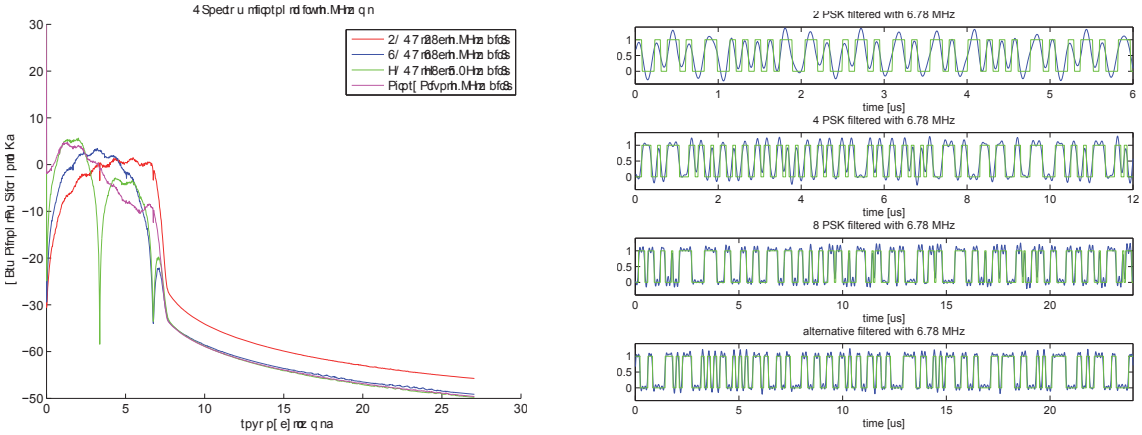
Figure 5.10.: Possible modulation patterns

Figure 5.11(a) shows the same plots as before, but with the bandwidth limited signal. The signal is sent through a low pass filter which cuts all frequencies higher than 13.56 MHz very sharply. The according signals in the time domain can be seen in Figure 5.11(b). It can be observed that all signals are very close to the transmitted one. Here the green signals are the transmitted signals, and the blue ones are after the bandwidth restriction at the low pass filter.



(a) Spectrum (b) Signal

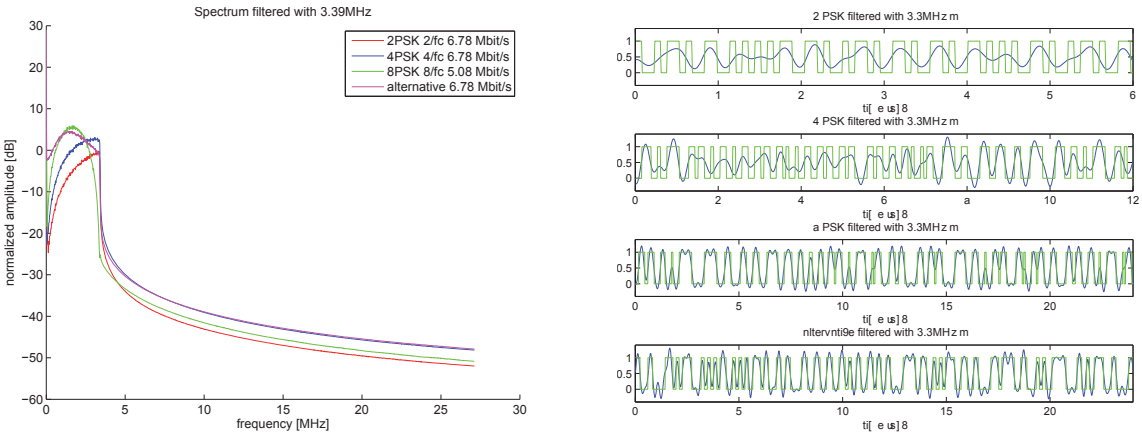
Figure 5.11.: Possible modulation patterns filtered at 13.56 MHz



(a) Spectrum (b) Time domain signal

Figure 5.12.: Possible modulation patterns filtered at 6.78 MHz

The same can be seen in Figure 5.12 again with a bandwidth limitation of 6.78 MHz. This means that half of the spectrum of the 2 PSK is already filtered, while the spectrum till the first zero pole of the 4 PSK is transmitted. It can be seen in the time domain, that the signal at 2 PSK differs more from the original (green) one, than the other, although there is already a big gap at the 4 PSK as well.
Going further and limitting the bandwidth at 3.39 MHz in Figure 5.13 it can be seen that the signals differ a lot from the previous ones. The short changes in the 2 PSK are smoothened due to the limited bandwidth. The same can be seen in the 4 PSK. Here the advantage is that each signal has at least one part where 2 carrier periods stay at the same state, which allows the signal to follow its pattern. The 8 PSK with the lower bandwidth requirement follows its original signal quite good and the alternative patterns seems to perform very good at the limited bandwidth.



(a) Spectrum (b) Time domain signal

Figure 5.13.: Possible modulation patterns filtered at 3.39 MHz

To give a more objective statement, the RMSE of each signal at the different bandwidth limitations is calculated and listed in Table 5.6. They are also plotted in Figure 5.14 to visualize the results. As also seen in the Figures above the 2 PSK has the biggest difference between the sent and the received signal due to the high bandwidth requirement. Increasing the order of PSK decreases the required bandwidth and the RMSE is also decreased. The best performance will respect to RMSE can be achieved with the alternative pattern, even though the RMSE it is only slightly below the one of 8 PSK. The problems in this modulation are the different duty cycle and the 16 possible patterns.

Bandwidth	2PSK	4PSK	8PSK	alternative
filtered at 13.56 MHz	0.2027	0.1684	0.1293	0.1262
filtered at 6.78 MHz	0.2817	0.2312	0.1744	0.1647
filtered at 3.39 MHz	0.4580	0.3708	0.2427	0.2327

Table 5.6.: Results of RMSE for different modulation schemes and bandwidth limitations

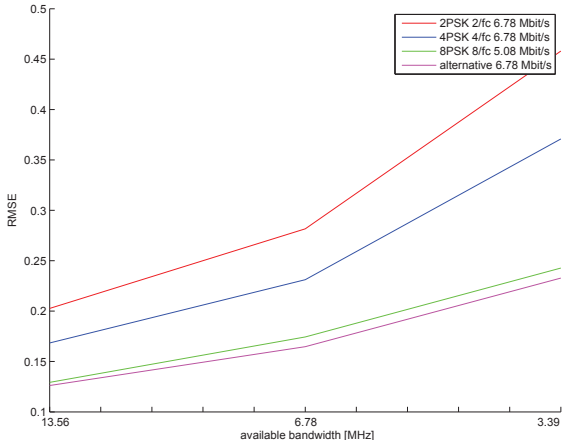
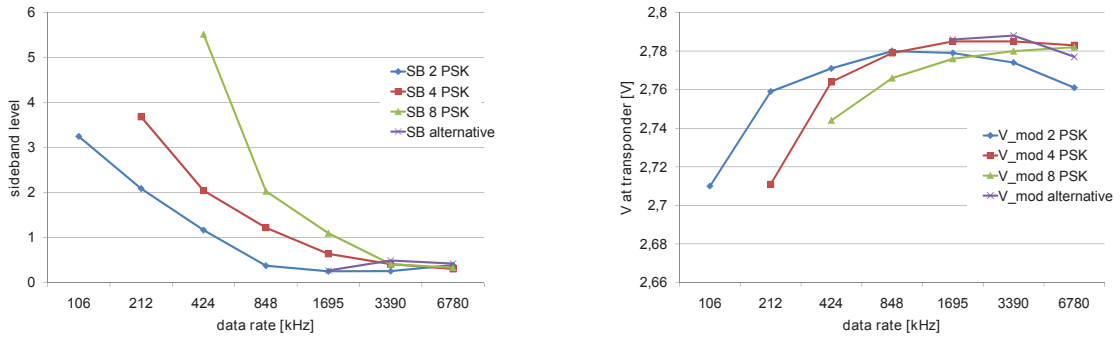


Figure 5.14.: RMSE of the different modulation patterns at limited bandwidth

5.2.4. Signal Measurement

To compare the signals with each other in real environment a measurement was performed on the ISO test assembly with a reference PICC. The reference PICC was tuned to 13.56 MHz and the limiter was set to 3 V. The measurement was performed at a field strength of 1.5 A/m. To generate all relevant load modulator signals the Tabor Arbitrary Waveform Generator WX2182 was used. The patterns were generated with the help of the same script as depicted in Figure 5.9, and stored as .csv file, which can be transformed in the required format for the waveform generator with the included software of the generator.
The data were sampled on the oscilloscope and post processed in Matlab. Here it has to be said that the scaling is not ISO conform, due to the fact that the signal was not measured on the anti Helmholtz coils, but on the RX pin of the setup, to evaluate other parameters as well. To compare

the results, data rates starting from 106 kbit/s were also measured.
Two different parameters are measured and compared. The first one is the side band level. The side band level indicates the difference between the level of the carrier and the side band at the related subcarrier frequency. To ensure a stable communication special side band levels are defined in the standard. The second parameter which is measured is the supply voltage at the transponder.
Analyzing the 2 PSK curve in Figure 5.15(a), it can be seen that the side band levels of the lowest data rate is the highest in this curve. This can be explained with the quality factor, since the signal has enough time to settle and reaches its steady state. Increasing the data rate, the required bandwidth is increasing and the time constant of the antenna is too large and the signal cannot reach its steady state, which results in a lower side band level. Increasing the data rate means decreasing the side band level. The same trend can be seen for the 4 PSK as well as the 8 PSK. Here it has to be mentioned again that the data rate for 8 PSK is lower than for the other curves. The side band levels for the alternative proposal are rather constant.
In Figure 5.15(b) it can be seen that the minimum voltage of the 2 PSK at the transponder is increasing during the communication, when the data rate is increased from 106 kbit/s to 848 kbit/s, and it is the highest voltage compared to the others. From 1.696 Mbit/s to 6.78 Mbit/s the voltage decreases for 2 PSK, but increases for 4 PSK as well as 8 PSK. The alternative patterns are rather constant again.



(a) Side band levels

(b) Supply voltage

Figure 5.15.: Comparison of the different modulation patterns

5.2.5. Conclusion

Since there are many different parameters, this section should conclude all findings to decide, which pattern should be used in the ISO Standard proposal.
The alternative patterns are more complicated to generate than the pure PSK modulation patterns, furthermore the Hamming distance is only 1, while the other patterns have a minimum Hamming distance of 2. The RMSE is the best in case of bandwidth restriction, but due to the higher duty cycle the pattern does not fulfill the requirements and will not be proposed.
The classical patterns shown in Figure 5.7 are all having the same minimum Hamming distance of 2 and a duty cycle of 50 %. The RMSE error shows that the best would be 8 PSK, due to the

lowest required bandwidth, followed by 4 PSK and the worst performance can be found in the 2 PSK. Taking into account the side band level measurement again the same ranking as before can be seen, due to the time constant, but the difference is very small at the required data rates of 1.695 Mbit/s to 6.78 Mbit/s. Observing the voltage at the transponder, 2 PSK is the best choice for the base data rate and also for higher data rates from 212 kbit/s to 848 kbit/s, while the voltage drops again for very high data rates, here 4 PSK performs best.
Summing all findings, the proposal for the ISO Standard will be 4 PSK, since the complexity is lower than for 8 PSK.

5.2.6. ISO Proposal

The ISO proposal for the communication from card to reader is based on the findings above and proposes 4 PSK. Again only the data rate of 6.78 Mbit/s is described, and all other data rates can be found in Appendix A.
The symbols are shaped as depicted in Figure 5.16.The only difference between Figure 5.7(b)and Figure 5.16 is the arrangement of the patterns and the naming. In the standard the patterns are called symbols. Each symbol of the 4 PSK has a certain binary information content which is mapped to the symbols in Table 5.7.
Again a preamble is defined to synchronize the communication. A more detailed explanation can be found in the Appendix.

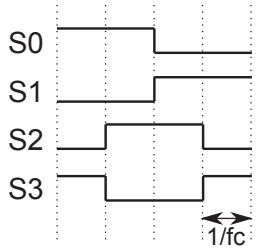


Figure 5.16.: Load modulation symbols

Information content	Symbols
00	S0
11	S1
10	S2
01	S3

Table 5.7.: Symbols and information content [46]

6. Possible Reader Concepts

In this chapter different reader concepts are introduced and compared to each other. The reader has to cover the basic requirements as to provide a field to power the transponder, transmit and receive data. Based on the findings of the previous chapters the different concepts are compared and the most promising concept will be implemented in a reader prototype. For the comparison the chapter is separated into two parts, where the first one focuses on the transmit path of the reader and the second one deals with the receive path.

6.1. Transmit Path of the Reader

To implement the transmit path of the reader several existing designs were analyzed to get an idea of how current systems generate their field and perform the amplitude modulation. Most current reader ICs generate the output field by switching a transistor stage to the supply voltage or to ground. The generated rectangular wave at the nodes TX1 and TX2 in Figure 6.1 have to be transformed to a sine wave with the help of a filter. Using an electromagnetic compatibility (EMC) filter, higher harmonics of the carrier are suppressed leading to a sine wave. The same time the voltage output is transformed into a current source by the EMC filter, since the current is the required dimension to drive the antenna current which is responsible for the field. A typical circuit is shown in Figure 6.1. On the left side the output structure of the IC can be seen which

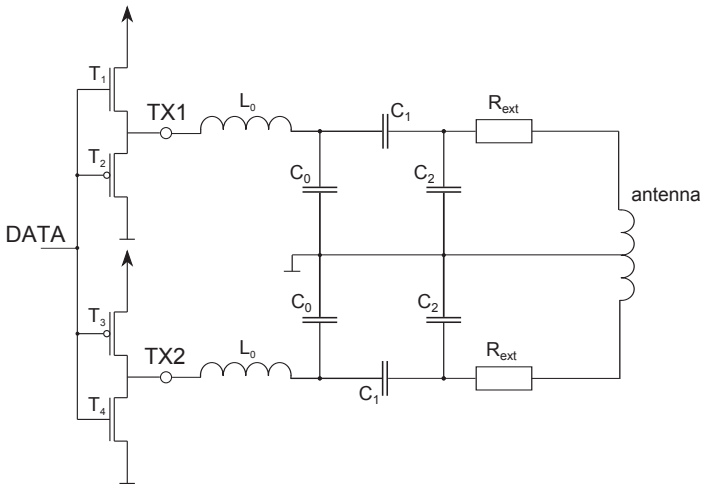
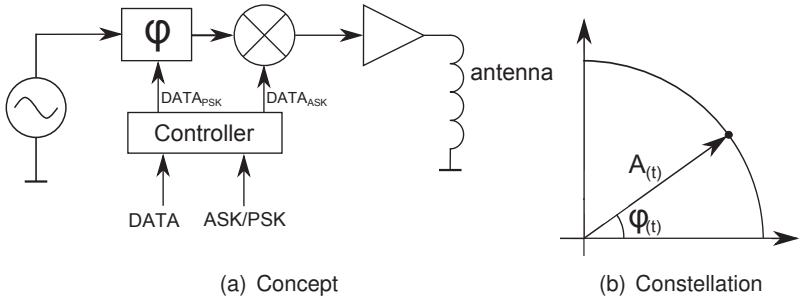


Figure 6.1.: Possible output and matching structure

consists of two transistors for each path, which either connect the output to the supply voltage

(T1, T3) or to ground (T2, T4). The differential output is realized by the same structure twice, where the second output is controlled by the inverted signal of the first one.
The EMC filter consists of a coil (L_0) and a capacitor (C_0) as shown in the Figure. The cut off frequency of the filter is calculated to allow the carrier and the upper side band of the modulation to pass the filter, while higher harmonics are suppressed. In case of the base data rate of [17], this would mean $f_{\text{cutoff}} = 13.67\,\text{MHz}$. For the highest data rate of 848 kbit/s it would result in $f_{\text{cutoff}} = 14.41\,\text{MHz}$. The problem of this setup is that the output is bandwidth limited, since the rectangular wave has to be filtered and transformed into a sine wave. Increasing the bandwidth to allow data transmission at higher data rate would not result in a sine wave any more, since too many harmonics will pass the filter.
The matching network is the same as presented in Subsection 3.1.2, but it is conducted differentially, which means that the matching circuit in fact is doubled.
The bandwidth limitation leads to the need of a new structure, which allows a good signal shaping as well as a high bandwidth to transmit at very high data rates.
Another idea is to realize the phase changes with the help of different delay lines. A sine source provides a carrier at 13.56 MHz and with the help of different delay lines the phase changes are realized. The problem of this setup is that most delay lines are designed for digital signals, and the rectangular wave has to be transformed to a sine wave afterwards. That way the problems will be the same as in the considerations above. Another problem is to find a delay line with the required accuracy and speed to change the delay. To realize a phase change of 4 degrees, a delay of 819.4 ps would be required. To generate the constellation diagram shown in Subsection 5.1.6 a delay line is needed which is able to set the delay from 0 to 12.29 ns in 819.4 ps steps. Furthermore, the changes have to be fast enough to switch the signal as fast as possible to settle within a symbol period and a higher Q factor. Additionally, the change from one delay to another has to be performed continuously not to detect a wrong phase change as symbol.
To control the delay line a controller is needed which provides the control signal for the delay line in dependency of the input data. The drawback of this realization is that no amplitude modulation can be performed, which means that an additional multiplier or attenuator has to be added allowing to reduce the amplitude by 10 % (Type B) or to turn it off for a certain time (Type A). A possible realization of this concept is depicted in Figure 6.2(a).



(a) Concept (b) Constellation

Figure 6.2.: Possible reader structure with a delay line and a multiplier

The output signal of the reader depicted in Figure 6.2(a) is described by

$$S_{TX}(t) = G \cdot A(t) \cdot \sin\left(\omega_c t + \varphi(t)\right) \tag{6.1}$$

Here G is the gain of the amplifier, $A(t)$ the amplitude modulation and $\varphi(t)$ the phase delay.
With this realization the reader is able to provide all required signals, PSK as well as ASK at different data rates, assuming a delay line with the required specification is used.
Another way would be to use an IQ modulator which multiplies the Inphase and Quadraturphase with the sine and cosine like depicted in Figure 6.3(a). For that purpose the data has to be separated in an I and Q part, which are needed as input of the modulator. This separation can be done by a controller, which is clocked at symbol rate, and provides a new I and Q value for each symbol. The advantage of this concept is that it is able to realize amplitude as well as phase modulation by changing the values of I and Q. The variable delay line, which is needed to perform the phase modulation in the last concept is replaced by a fixed delay line, which shifts the input signal by $\pi/2$. This fixed delay line can be realized at higher accuracy than the flexible one and does not have to be changed.

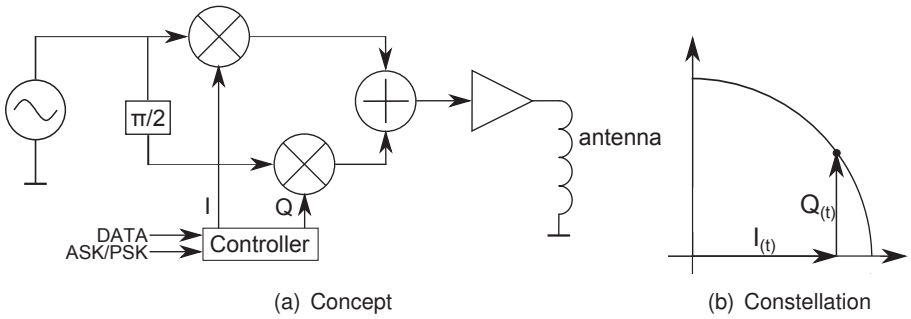


Figure 6.3.: IQ modulation concept

The output is defined by Equation 6.2.

$$S_{TX\_IQ}(t) = G \cdot \left[I(t) \cdot \sin(\omega_c t) + Q(t) \cdot \sin\left(\omega_c t + \frac{\pi}{2}\right) \right] \tag{6.2}$$

Beside the signal generation an amplifier is needed, which provides enough power to reach the required field strength. The dimensioning of the amplifier and the whole setup is described in Chapter 7.

6.2. Receive Path of the Reader

The receiver has to extract a very small amplitude variation from a large carrier amplitude with an accuracy which is high enough to demodulate the signal. Two main different concepts are possible as depicted in Figure 6.4. It is possible to use one antenna for both, signal transmission and reception, or to separate them into a transmit antenna and a receive antenna. Both topologies have different advantages as well as disadvantages.
Using the one antenna topology different concepts are possible again, as depicted in the same Figure, which will be explained later.

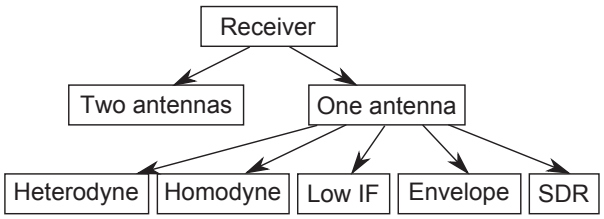


Figure 6.4.: Possible receive structures

6.3. Two Antenna Structures

The two antenna structure has some benefits and simplifications compared to the one antenna structure. The big advantage is that each antenna can be optimized for its special purpose, and no tradeoff has to be made between the requirements of the transmit and the receive antenna. The transmit antenna should have a higher quality factor to make the system more energy efficient, the same time the time constant should be adapted that the transmitted signal can be send without introducing too much ISI. The tradeoff between the bandwidth and the quality factor has already been discussed.
Using another antenna for the receive path, which is the more complicated one in RFID technologies, since the information has to be extracted from a large carrier, makes it easier to detect the data. The first advantage is that the receive signal does not have to be decoupled by a network from the transmit path to get the desired voltage level. Since the receive path has much more relaxed requirements on the energy efficiency, the quality factor can be kept low to have a higher bandwidth, which reduces ISI.
What has to be taken into account is the coupling factor between the different antennas. The coupling factor should be high between the transponder and the receive antenna, but the same time as low as possible between the receive and transmit antenna. If the receive and transmit antenna have a high coupling factor, the influence of the transmit antenna is high on the receive antenna, so that nearly the same signal can be seen on both antennas at different amplitude. This can be achieved by a loop close to the transmit antenna as shown in Figure 6.6(b). This effect causes strict requirements on the antenna design to allow a good performance.
Going one step further the receive antenna can be shaped differentially. The advantage of a differentially shaped antenna is that the carrier can be reduced or even canceled as depicted in Figure 6.5.
As can be seen in the left picture, the two antennas are in the same field, which leads to the same induced voltage, if the antennas have the same size and location in the field. This means that $u_1 = u_2$. By connecting them differentially as in the right picture, the potentials are canceled and no voltage u should be seen at the output. This means, if there is no modulation, u should be zero. There is always a little mismatching due to inaccuracy in the antenna shaping and location, but this can be tuned by a resistor to reach the minimum at the output. The same principle is used in the anti Helmholtz setup of the ISO test assembly described in [38].
The advantage of this design is that the antenna can be designed with a very low quality factor to keep the influence of the bandwidth low. The problem of this design is that the antenna has a so called blind spot. If the transponder is placed in the middle of the two coils, as depicted in

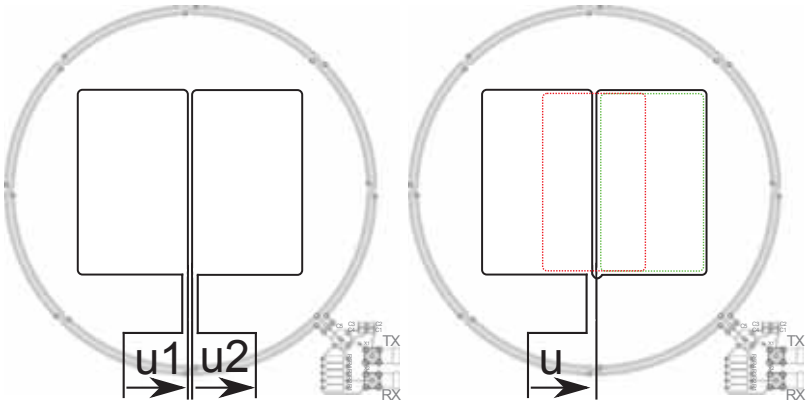
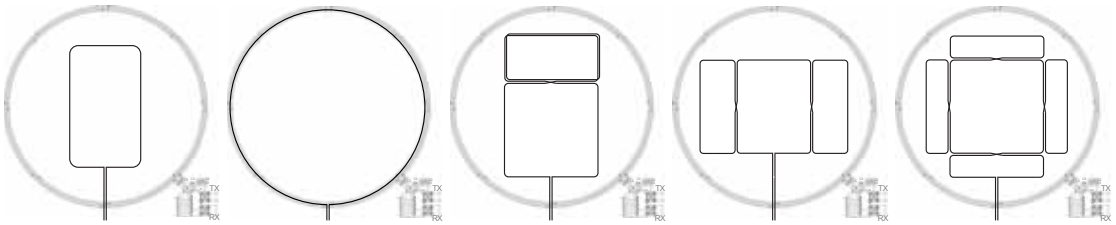


Figure 6.5.: Principle of differential antennas

the right picture in red, the influence of the transponder on the field influences the induced voltage in both loops the same way and so the changes are also canceled and no communication can be detected. If the transponder is located like shown in green, the modulation is maximized and the response can be seen clearly. To avoid or make it hard to find blind spots the antenna shaping can be changed. Figure 6.6(c) to Figure 6.6(e) show different antenna shapes which can be used, and which all have a little blind spot if ID-1 transponders are used. The ideas for the shapes are taken from [48].



(a) Sense coil (b) Antenna 1 (c) Antenna 2 (d) Antenna 3 (e) Antenna 4

Figure 6.6.: Possible receive antennas

The parameters of the antennas depicted in Figure 6.6 are listed in Table 6.1. All antennas are placed directly on the transmit antenna except for the sense coil, which is located 37.5 mm below the transmit antenna as defined in [38].

	Sense coil	**Antenna 1**	**Antenna 2**	**Antenna 3**	**Antenna 4**
concept	loop	loop	differential	differential	differential
f_{res} [MHz]	77.60	48.46	32.20	37.25	31.64
L [nH]	208	531	1070	848	1137
C [ρF]	20.22	20.31	22.69	21.53	22.25
R [mΩ]	165.8	162.3	343.9	318.7	446.6

Table 6.1.: Antenna parameters

Figure 6.6(b) represents a single loop which is close to the transmit antenna. Due to the close distance to the transmit antenna and the caused high coupling factor the antenna experiences nearly the same signal as the transmit antenna at a different voltage level. In Figure 6.6(c) a differential antenna is shown, which has a bigger loop, and 2 loops each half of the area of the big one. That way the antenna has the same field in each loop and the output is reduced. If the transponder is placed in the larger loop, or in the smaller loop the field is canceled while the responce can be detected. If the transponder is placed such that both loops influence them the same way, the response is canceled as well and the transponder is placed in the blind spot. Figure 6.6(d) has a bigger loop in the middle and on each side a smaller one, with half of the area. It is nearly the same as the last antenna, with the difference that the loops are not placed at the top of each other, which reduces the blind spot. Figure 6.6(e) increases the complexity and the antenna consists of a larger area and 4 times a smaller area which are together the same as the larger one. That way the field is canceled again and it is nearly impossible to find a blind spot with an ID-1 transponder.
To compare those antennas the ISO test assembly is used with the reference PICC, and the differential antennas are placed on top of the transmit antenna. The relative voltage difference between the unmodulated V_{unmod} and modulated V_{mod} case is plotted in Figure 6.7 normalized with half of the peak to peak value V_{pp} of the unmodulated carrier as defined by

$$\Delta = \frac{2 \cdot (V_{unmod} - V_{mod})}{V_{pp}} \tag{6.3}$$

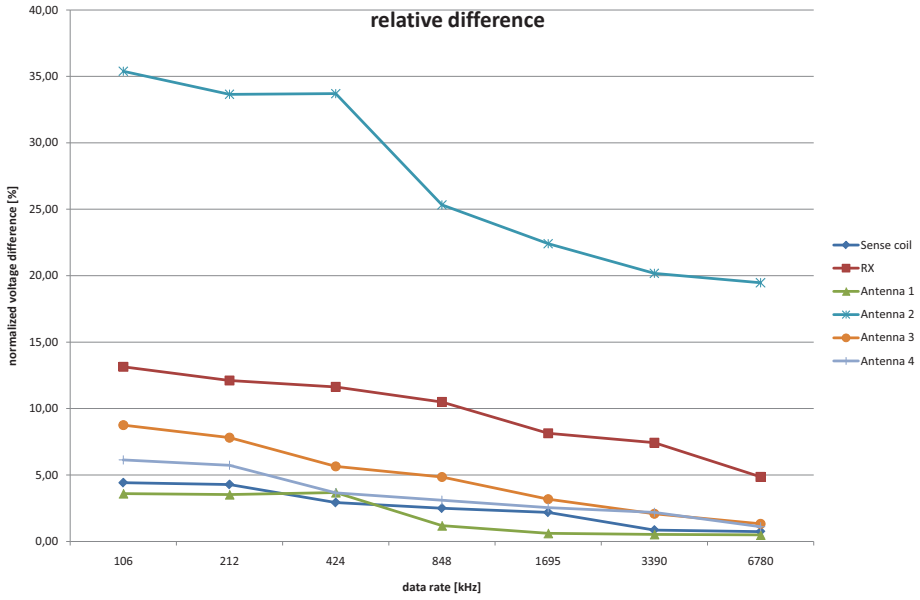


Figure 6.7.: Voltage difference of different receive antennas

In the measurement the differential antennas are placed directly on the transmit antenna, which makes the coupling between the transmit antenna and the differential antenna high. It can be seen that the RX pin of the ISO antenna has a good performance. There is only one differential antenna concept which is much better than the RX pin and all other antenna concepts are performing worse.

There is a simple way to improve the performance of the differential antenna, if the antenna is located at higher distance to the transmit antenna. For example if the differential antenna is 1.5 cm distant from the transmit antenna the signal is much better. Due to reasons of the housing of the reader the realization is complicated, since the housing has to be made larger. Furthermore, the antennas are only hand made with a copper wire, which has limited accuracy.
If the antennas shown in Figure 6.6 would be tuned to the size of the transponder, the performance would also be increased in one point, but if the transponder is located in a different way, the performance will decrease significantly.
Furthermore the problem of the two antenna concept is that another antenna has to be tuned to the input of the reader IC and the antenna has to be implemented in the housing. Therefore it is harder for the reader development to design a reader, since the effort of two antennas in the housing is higher than for only one antenna. Based on this it would be a disadvantage compared to competitors if they only need one antenna for both. Moreover, a second antenna leads to problems in certain applications, for example at eGovernment, where the reader antenna is placed around an optical scan area. This means the differential antenna has to be outside the optical field, not to influence the scan which is needed to generate the key to read the data on the IC.
Concluding this experimental excursion, it was shown that there is a way with differential antennas to increase the received signal by suppressing the carrier. The antenna design is not that easy since an optimum between the carrier suppression and volume, where the transponder can be placed, has to be found, avoiding blind spots. Although the effort of the signal processing is reduced, the complexity is shifted from the signal processing to the antenna design. A demonstration in the lab has shown that it is possible to increase the data rate up to 27.12 Mbit/s with differential antennas. The problem is that the antenna has to be distant from the transmit antenna and very close to the transponder. Furthermore, the volume where the transponder is operating is limited due to the antenna design. There was an additional strong desire from management that only one antenna is used, which implicates that the differential antenna concept is mentioned as excursion but will not be part of further findings.

6.4. One Antenna Structures

Beside the two antenna structures as described above, the more common design is with a single antenna for both, transmission and reception. Many concepts which will be mentioned in the next part are based on general telecommunication purpose, which means that not all of them are useable for RFID applications, but the following part should separate the possible concepts and lead to further investigations of only two concepts, which can be compared with each other.
In all concepts it is assumed that the receive signal is extracted from the transmit antenna over the dumping resistors as described in Subsection 3.1.1.

6.4.1. Heterodyne Receiver

The heterodyne receiver has its origin in satellite communication. The idea behind this concept is to be able to choose different channels, which have different carrier frequencies, by tuning a local oscillator. The structure can be seen in Figure 6.8. The signal from the antenna is amplified and mixed to an intermediate frequency (IF). The frequency of the tunable local oscillator (LO)

is defined such that the carrier frequency is mixed to the IF band. The bandpass filter (BPF) removes all unwanted frequencies and the signal is amplified again, before it is mixed to the baseband by an IQ demodulator. The mixed signal is low pass filtered (LPF) to reduce the doupled IF, before it is sampled and digitized.
The advantage of this concept is the tunable first LO. By changing the frequency the desired signal is mixed to a defined IF. A constant IF means that all filters can be implemented without tunable components, since they do not need to vary the frequency. The down conversion by two steps also has some advantages, since the filters can be implemented more accurate at lower frequency and distortions can be filtered more effectively.
However, all those advantages are not relevant for the wanted application. The frequency is set to 13.56 MHz and there is no other band which can be chosen. Therefore there is no need to change an IF. The frequency is not that high that there is any benefit of a two step conversion. In this case the disadvantages are dominating, since the complexity is very high. Furthermore, the design has many RF nodes, and more power for the extra filters and amplifiers is needed [49].

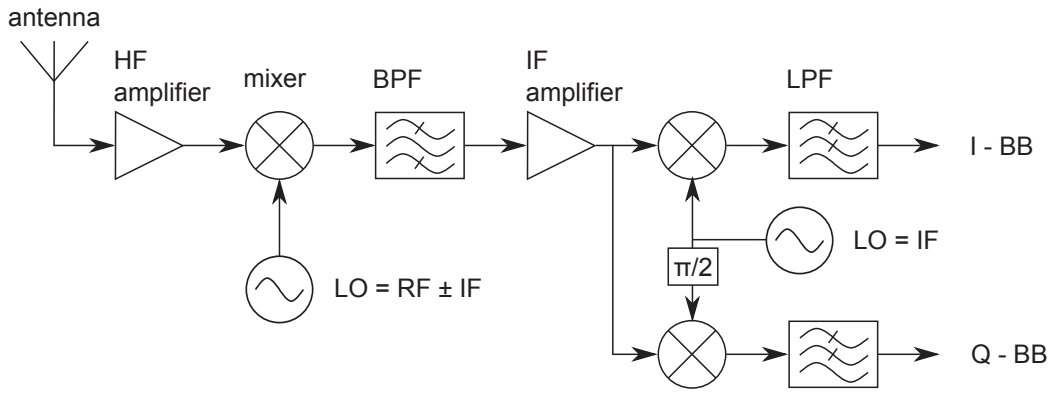


Figure 6.8.: Heterodyne receiver schematic

Concluding it can be said that the concept is good for very high frequencies and if there are several bands which should be chosen, but for the defined requirements the receiver is too complex. That means that for further considerations this concept will not be taken into account.

6.4.2. Homodyne Receiver

The homodyne receiver is also called direct conversion or zero-IF receiver. Different from the heterodyne receiver, there is no IF, and the signal is mixed to the baseband without any intermediate steps. The principle can be seen in Figure 6.9. The signal from the antenna is amplified by a low noise amplifier (LNA) and connected to an IQ demodulator, whose local oscillator is running at the carrier frequency.
The advantage of this concept is that there are few RF nodes and the integration is easier. The output is at baseband and can be sampled by two analog to digital converters (ADC) for further signal processing.
The drawback is that signal leakage paths can occur, and the signal from the local oscillator can pass the mixer to the antenna and re-enter the mixer stage. That way a DC offset is generated which can harm the signal. Furthermore IQ mismatch can lead to SNR degradation.

Concluding it can be said that this concept is easier to implement than the heterodyne concept. With the few RF nodes it is not that power consuming as comparable concepts and the concept is already used in present ICs. Therefore this concept will be evaluated in further steps. The main difference from present ICs will be that the limited bandwidth has to be enhanced to be able to receive VHD rates.

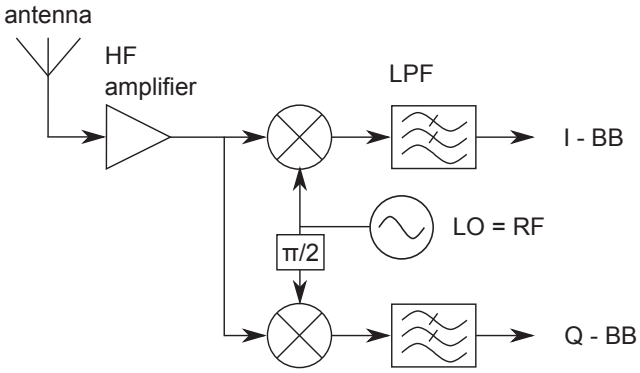


Figure 6.9.: Homodyne receiver schematic

6.4.3. Low Intermediate Frequency Receiver

The low IF receiver is a combination of the heterodyne as well as homodyne receiver as seen in Figure 6.10. The received signal is amplified and connected to an IQ demodulator. The LO has a frequency such that the carrier is not mixed into the baseband, but to an IF. The signal at IF is sampled and a complex signal processing is performed to generate the base band signal.
The advantage of this structure is that the complexity in the analog domain is reduced, and the spectral information is not lost. Furthermore, since the signal is not converted to baseband, there is no flicker noise as well as no DC offset.
The drawback of this concept is that there is a higher sensitivity of IQ mismatch than in the homodyne concept and the signal processing is more complex.

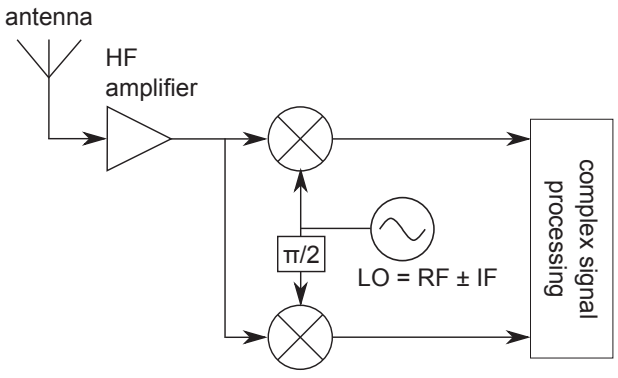


Figure 6.10.: Low IF receiver structure

It can be said that this concept has more advantages than the heterodyne receive structure but for the needed application it is not the best choice, since the signal processing at any IF is more complex than in the baseband. The carrier frequency is quite low compared with other telecommunication systems which means that mixing to an IF has no benefit at all. This concept will not be taken into account for further findings.

6.4.4. RF Envelope Detection

The RF envelope detection recovers the envelope of the signals as the name describes. This detector can be implemented easily with very low effort. The problem is that the detector is only able to detect amplitude modulation and so it has to be guaranteed that all the information is in the amplitude and not in the phase. A very simple concept of the envelope detector is depicted in Figure 6.11. The problem is to dimension the low pass filter, which extracts the envelope. The carrier has to be suppressed and the envelope should not be distorted. If the bandwidth of the transmitted data is close to the carrier frequency, very sharp and accurate filters are needed to achieve the required performance. In the wanted setup the carrier frequency is only twice the signal frequency, which leads to a very tough and complicated filter to get a satisfying performance. For lower data rates this concept works fine, if the amplitude modulation is deep enough. For the desired setup the envelope detector in its simple form will not work, due to the fact that the signal is distorted and the signal will not reach its steady state during the communication. Therefore this concept will not be evaluated.

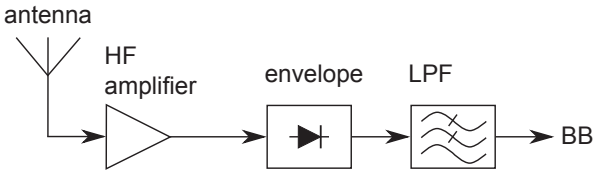


Figure 6.11.: Envelope detection

6.4.5. Software Defined Radio

Figure 6.12 shows the principle of a Software Defined Radio (SDR). An SDR has an antenna, which is connected to an amplifier and an ADC. This means that the received signal is just amplified and converted to the digital domain. The signal processing, such as down sampling or mixing, is done in the digital domain. The advantage of this concept is that the receiver structure is only defined by software and can be changed very easily and fast [50].
It is hard to distinguish where SDR ends and other receiver structures begin, since there are also concepts which have an IQ demodulator before the ADC. To avoid misunderstandings, in this thesis SDR defines the sampling of the received signal right after the amplifier without any signal processing before the ADC.
Due to the very flexible integration of the receiver as well as the transmitter, the focus of the thesis will be on this concept. Beside the concept of the SDR, the concept of the homodyne receiver will also be taken into account for comparisons.

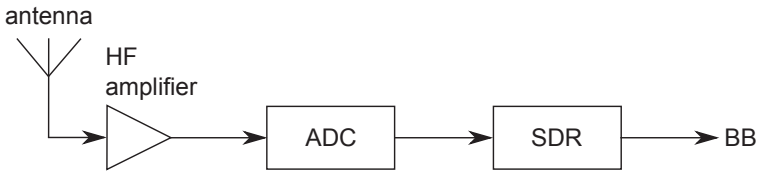


Figure 6.12.: Software Defined Radio

6.4.6. Conclusion

This section has shown different receiver concepts which can be used for a possible RFID receiver implementation. Each concept has its benefits, but not all of them are beneficial for the use in RFID systems. Table 6.2 lists some aspects of the different concepts to compare them with each other. As listed in Table 6.2 two concepts will be taken into account for further investigations.

	Heterodyne	**Homodyne**	**Low IF**	**Envelope**	**SDR**
RF nodes	many	~	~	few	~
costs	high	~	~	low	~
analog complexity	high	~	~	low	low
digital complexity	low	low	high	high	high
advantage	not relevant	few RF nodes	no DC	easy	flexible
disadvantage	power	DC	IF	DR too high	ADC res.
integration	complicated	possible	possible	easy	possible
further considerations	no	yes	no	no	yes

Table 6.2.: Conclusion receiver concepts

Selected on the requirements for the RFID system the concept of SDR and homodyne receiver fit most perfect to the requirements. Due to the wanted flexibility of the evaluation reader, the SDR has advantages in terms of flexibility as well as costs. With only one accurate ADC the signal is sampled and the signal processing can be performed on board. Especially for the wanted evaluation reader, the concept is the most promising one, since all different signals can be sampled and the signal processing is done in software. This concept can also be used for other measurements as well, due to the highly flexible integration. For the way of working this means that the prototype will be implemented based on the concept of SDR, described in Chapter 7.
In a second step an additional IQ demodulator will be added in front of the ADC to mix the signal to the baseband before it is sampled, which reduces the requirements for the ADC. The implementation of the IQ demodulator is described in Section 9.2.

7. Implementation of a Prototype

In the last chapter different concepts which can be implemented in a prototype and evaluation reader have been investigated. According to the comparison in the last chapter the evaluation platform will be based on the concept of SDR. This concept enables a wide area of applications and a very flexible setup, allowing to compare all modulation schemes described in Chapter 5. Beside the flexibility and the coverage of all different data rates, the setup was designed to allow a simple handling. Before the implementation will be described a short summary of the requirements will be given.

7.1. Requirements

The requirements for the evaluation reader contain a wide spectrum. It should be possible to transmit and receive all signals which are specified in the ISO 14443 proposal, described in Subsection 5.1.6 and 5.2.6 as well as in Appendix A. Furthermore, it should also be possible to transmit all signals standardized in [17].

Symbol duration	ASK Type A/B	2 PSK	4 PSK	8 PSK	16 PSK
128/fc	106	-	-	-	-
64/fc	212	-	-	-	-
32/fc	424	-	-	-	-
16/fc	848	-	1695	2542	3390
8/fc	1695	1695	3390	5090	6780
4/fc	3390	3390	6780	10170	13560
2/fc	6780	6780	13560	20340	27012

Table 7.1.: Required signals for transmission PCD to PICC in [kbit/s] [51]

Since the evaluation reader should also be used as measurement equipment and to compare different proposals with each other, it has to support all data rates and modulation schemes listed in Table 7.1. As mentioned in Section 5.1 the modulation angle has to be reduced to power the transponder and utilize the whole available spectrum. This means the evaluation reader has to support a modulation angle of 2π, π, $\pi/2$ and $\pi/3$ to find the ideal modulation angle for the transmission and show the differences.
Furthermore the transmit amplifier has to provide a field strength range from 0.5 A/m up to 7.5 A/m.
The receive path of the evaluation reader should be as simple as possible to reduce possible error sources which are caused by wrong user defined settings. It also should be possible to receive any types of signals, different modulation patterns as well as data rates to show the full

reader functionality. To communicate with different transponders, which have different modulation strength, the sensitivity of the evaluation reader should be as high as possible.
Additionally, the evaluation reader should provide an LM control signal to perform bit error rate BER measurements as standalone device. This LM signal is used to control the load modulator on a reference PICC or any other transponder with a control input for the load modulator. For the stand alone BER measurement the LM control signal is connected to a reference PICC or any other IC, which has an LM control input, and the received data is evaluated at the reader.

7.2. Concept of the Evaluation Reader

Driven from the requirements in the last section a concept is created, which fulfills all requirements and is depicted in Figure 7.1. To keep the highest degree of freedom, the evaluation reader is based on a field programmable gate array (FPGA). That way it is possible to create all relevant signals on the FPGA, and to perform the signal processing on board as well. With the FPGA as base for the reader, it is possible to change the order of PSK, modulation angle and other parameters easily and no changes on the hardware have to be done, which makes it easier to handle.
The interface between the digital domain of the FPGA and the analog environment is realized by a digital to analog converter (DAC) in the transmit direction and an ADC in the receive path.
An analog board will filter the signal at the DAC and amplify it to transmit it over the air interface and achieve the required field strength.

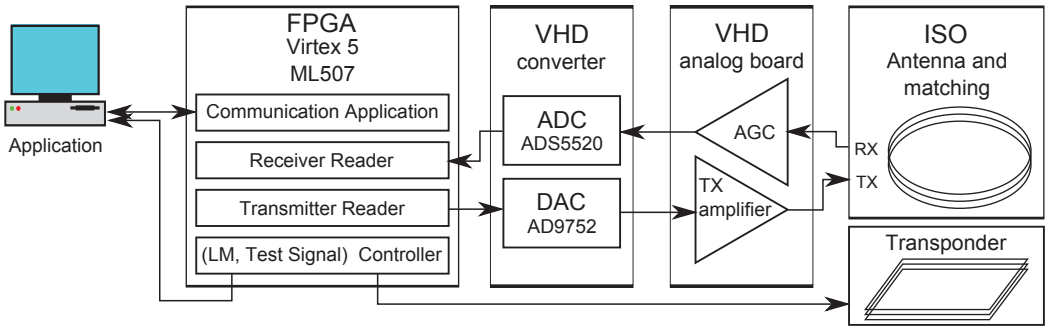


Figure 7.1.: Block diagram of the evaluation reader

To use the optimal range of the ADC and not to destroy it at higher field strength, an automatic gain control (AGC) is used to regulate the input voltage automatically to the optimum. That way the user only has to control the field strength, and does not have to take care about the receive path and the signal strength at the ADC. Furthermore, the voltage drop due to detuning if a transponder is in the field is also compensated by the AGC.
The FPGA also provides an output for the LM control on a reference PICC or any other IC which provides an LM control input. Since this signal is only a high low signal, it can be connected to any input and output (IO) pin of the FPGA and does not require a DAC.
To send commands to the FPGA a controller is added which allows the communication between

a host PC and the FPGA. That way it is possible to control the PSK order, modulation angle and define data, which should be sent over the air interface, and at the same time it is possible to transmit the receive data of the ADC to a host PC. Based on this communication the signal processing can be performed on the PC, for example in Matlab, which makes it easier to develop a receiver concept. The final receiver signal processing is also implemented on the FPGA such that the processed bit stream can be send to the PC for further analysis or any application.
The basis of this evaluation reader was developed together with colleagues within the project and is described in [52]. The original concept is similar although many components changed and were modified to improve and enhance the performance. That way the signal processing complexity increased significantly and the analog performance increased as well.

7.3. Implementation of the Evaluation Reader

The VHD evaluation reader consists of 4 main parts which are depicted in Figure 7.2. Based on the requirements and the concept it was tried to keep the highest degree of freedom and not to be limited with the resources. Only commercially available components were used, such as the Virtex 5 Evaluation Board ML507, which forms the base of the evaluation reader. The ML507 is

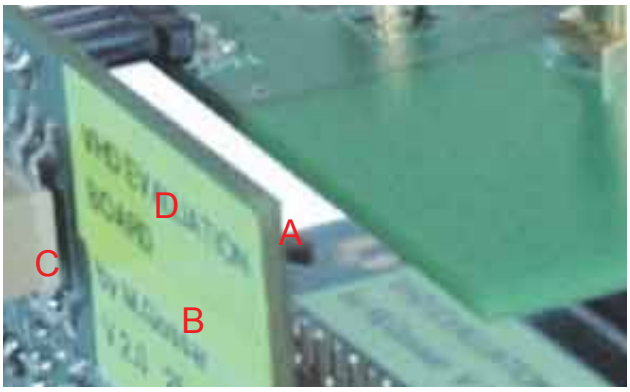


Figure 7.2.: VHD evaluation reader

marked in the Figure with A. To connect the converter, marked with C, an adapter B is needed to combine the IO pins of the FPGA to a socket. D indicates the analog part of the VHD evaluation reader and hosts the transmit amplifier, as well as AGC and the power supply unit for the setup.
The following section will go into more detail of each element, organized in the different parts of the evaluation reader.

7.3.1. Digital Unit - FPGA

The ML507 board was chosen because of its availability and flexibility and the number of different connections with respect to a demonstration. It is possible to connect a keyboard or mouse as user interface, or add a monitor to have a standalone demonstrator. For that the required software has to be written, which runs at the embedded soft core processor of the FPGA.

The evaluation board provides different clock domains which are needed for different communication interfaces. Several DIP switches can be used to load different programs or change settings, and pushbuttons and an liquid crystal display (LCD) allow to navigate through different programs on the FPGA. Different light emitting diods (LED) indicate the state of the FPGA and can be used as indicators for certain functions or initialization. Different interfaces such as universal serial bus USB, RS232, Ethernet and IO pins allow the interaction with different peripheries and the analog environment [53].

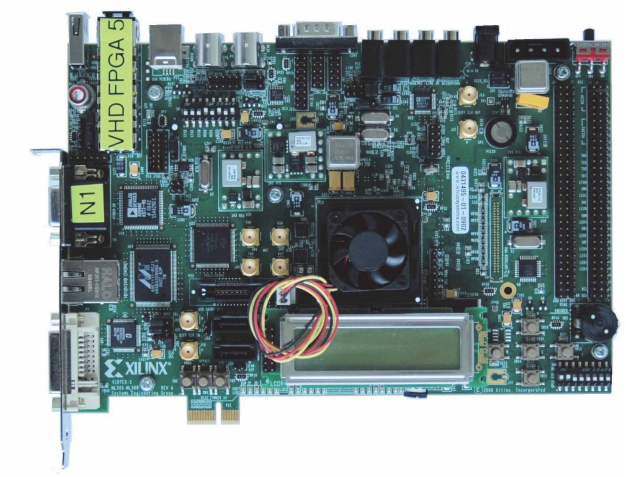


Figure 7.3.: FPGA board ML507

Figure 7.3 shows the ML507 board. In the middle, covered by the fan, the FPGA is placed. The fan is additionally mounted to prolong the lifetime of the FPGA and cool it, if the whole signal processing is used. As little side remark, a fan controller is implemented to reduce the speed of the fan if the FPGA is cool enough to reduce the noise of the setup.
There are different ways to program the FPGA. The joint test action group (JTAG) interface can be used to program the FPGA directly, or send the file to any on board random access memory (RAM), where the FPGA loads it from. That way the program is also available if the power supply of the ML507 board is interrupted. Additionally, the program can be placed on the compact flash card, which is placed on the bottom of the board, allowing to program the FPGA without a programmer from Xilinx. The use of the compact flash card also has the advantage that different programs can be stored and with the help of the navigation buttons different programs can be loaded.
The RJ45 or Ethernet connection is used to communicate with the FPGA from a PC. In the first version the RS232 connection was used, but due to the higher amount of data which is transferred in the actual version, the RS232 was too slow. With this interface different commands are sent to the FPGA to control it. That way it is possible to change from transmit to receive mode, change the PSK order and many other parameters. Furthermore, files can be transferred from the PC to the FPGA, which are encoded and transmitted over the air interface to the transponder. The same time the received data from the ADC can be sent to the PC to perform the signal processing on the PC, for example in Matlab, or get the received and processed bit stream, which was sent from the transponder.
The different clock domains of the FPGA are also important for the setup. The 100 MHz phase

locked loop (PLL), which is a default IC from production is replaced by an 108.48 MHz crystal oscillator in the evaluation reader. The board allows a maximum locking frequency of 550 MHz, but in this setup the clock is based on 8 times the carrier frequency. That way it is possible to define a sine wave by 8 samples per carrier period. The crystal is located in the right top corner of the FPGA between the power connector and the power switch. Additionally, other clock domains are needed for different interfaces, such as the Ethernet connection. It is not possible to clock the Ethernet interface also with the 108.48 MHz, since the interface on the computer will not be able to work on this frequency. Therefore an additional interface had to be implemented between the two clock domains, which mainly consists of a circular buffer.
The communication with the analog domain is done by 32 single ended signal connectors on the right side of the board. They are used to connect the transmit path to the DAC and the receive path to the ADC. Furthermore the LM control signal and additional signals, which are useful to trigger measurement devices, are provided over those connectors. Additionally two power domains are available next to the IO pins. It is possible to extract 5 V and 3.3 V from the ML507 board to power the converters.
The 16 pairs of differential IO pins are used for debugging the FPGA design and to control certain points within the signal processing chain.

FPGA Program Transmit Path

The FPGA implementation consists mainly of 4 blocks as seen in Figure 7.1. The communication interface of the FPGA is used to control the FPGA, and to exchange data between the FPGA and the PC. The ML507 board provides an Ethernet controller which is used for this interface. Due to the different clock domains a circular buffer is used to decouple the different domains.
The controller for the LM interface is implemented in a very simple way. To perform BER measurements random data are required. Therefore a random number generator generates a bit stream and the FPGA uses this bit stream as payload data. The preamble and the training sequence, defined in Appendix A, is followed by random data. To have the opportunity to debug the design it is also possible to send the same frame all time. To compare the different symbol shapings, which are described in Section 5.2, it is possible to change between the defined settings. This LM controller is only used for BER measurements during the development stage. In the demonstration the transponder is sending own data frames, which are received and processed on the reader side.
The transmit path consists of different stages to fulfill the ISO requirements. User defined data have to be processed as described in Appendix A and are mapped to the DAC as depicted in Figure 7.4. The evaluation reader uses the concept of SDR, which means that the whole signal processing, such as mixing, is done on the FPGA, and the signal which is transmitted over the air interface is sent to a DAC to be converted to the analog domain. In the following section the functionality of the shown blocks will be described.

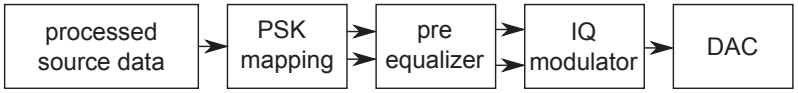


Figure 7.4.: Block diagram of the TX FPGA design

Processed Source Data The user defined source data are stored in a RAM on the FPGA. The Ethernet connection is used to transmit different data frames from the host PC to the FPGA. The possible frame lengths which are supported are 512, 1024 and 2048 kbyte. The FPGA transforms the stored data into a data frame as defined in Appendix A with the preamble and the training sequence, which is needed on the receiver side to detect the frame and calculate filter parameters. This frame is processed as described with the Grey decoder and cumulative sum to fulfill the requirements. Additional information can be found in Appendix A.

PSK mapping The PSK mapping block performs the mapping from the bit stream to the related symbols. In dependency of the order of PSK the mapping converts the related number of bits to a symbol in the related constellation diagram as defined in Appendix A. In case of 2 PSK each bit in the data stream is mapped to one symbol in the constellation diagram. Using the 16 PSK 4 bits define a symbol. In dependency of the symbol duration, the mapping provides a new I and Q value for each symbol. Each I and Q sample is expressed by 10 bits, which allows a high accuracy. The mapping is implemented with the help of different look up tables (LUT) for each PSK order.

Pre Equalizer The pre equalizer pre-EQ is an optional block, which is not defined in the committee draft of the standard. In the standard there is only a definition of the signal at the air interface. The standard does not define how it should be achieved and each company can chose a way. One way to achieve a clean signal, with less ISI, is to reduce the quality factor. This approach is very simple and straight forward, but has the drawback that the energy efficiency is reduced, due to the higher required power to achieve the same field strength.
An innovation of this project was the introduction of a pre equalizer. First experiments with a passive analog pre equalizer did not lead to the wanted results and so the pre equalizer was shifted into the digital domain. The first approach in the digital domain was with a single tap pre equalizer, working on the symbol rate [54]. Figure 7.5 shows the transmitted signal a(t) in the base band by the reader in red. The received signal at the transponder without pre equalization r(t) is plotted in green. Using a single tap pre equalizer at the reader leads to the signal r(t) PreEq. It can be seen that the signal with the pre equalizer reaches the same angle as the transmitted

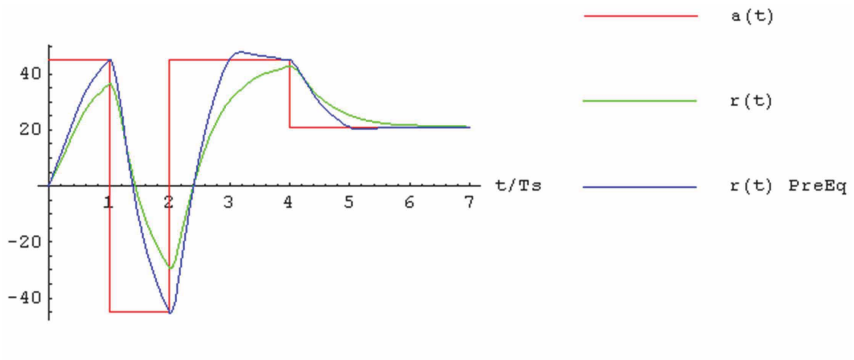


Figure 7.5.: Signal at base band with and without a single tap pre equalizer

signal at the bit edge. The problem of this approach is the overshoot if two same symbols are

behind each other. To avoid this overshoots an additional tap is introduced in the pre equalizer leading to the behavior in Figure 7.6. By comparing the signals with pre equalizer of Figure 7.5

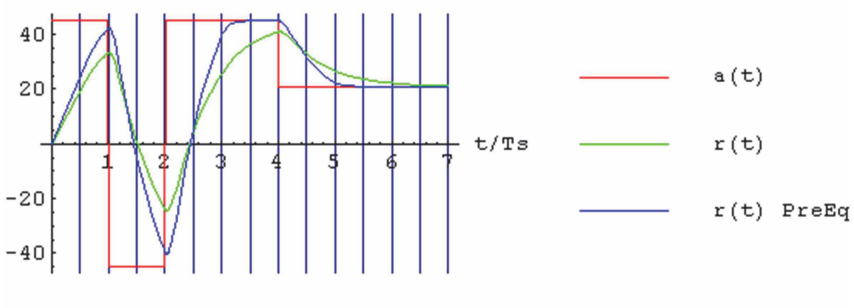


Figure 7.6.: Signal at base band with and without a two tap pre equalizer

and Figure 7.6 it can be seen that the single tap pre equalizer reaches the same angle as the transmitted one, while the two tap approach does not reach the same angle, but also does not have an overshoot if two symbols are equal behind each other.
To overcome this problem the pre equalizer is implemented as two tap pre equalizer [55], working at twice the symbol rate. This means that the signal is calculated twice in a symbol and the results are mixed to the pass band by an IQ modulator. Figure 7.7 shows the received signal at the transponder with this pre equalizer and it is seen that the angle is reached within the second half of the symbol and two same symbols after each other do not causes overshoots. Figure 7.8(a)

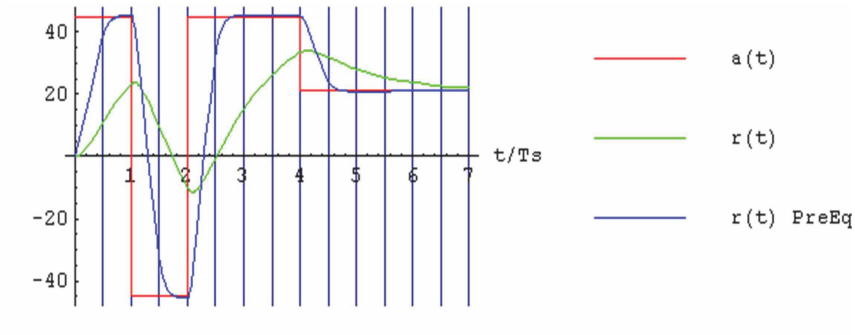
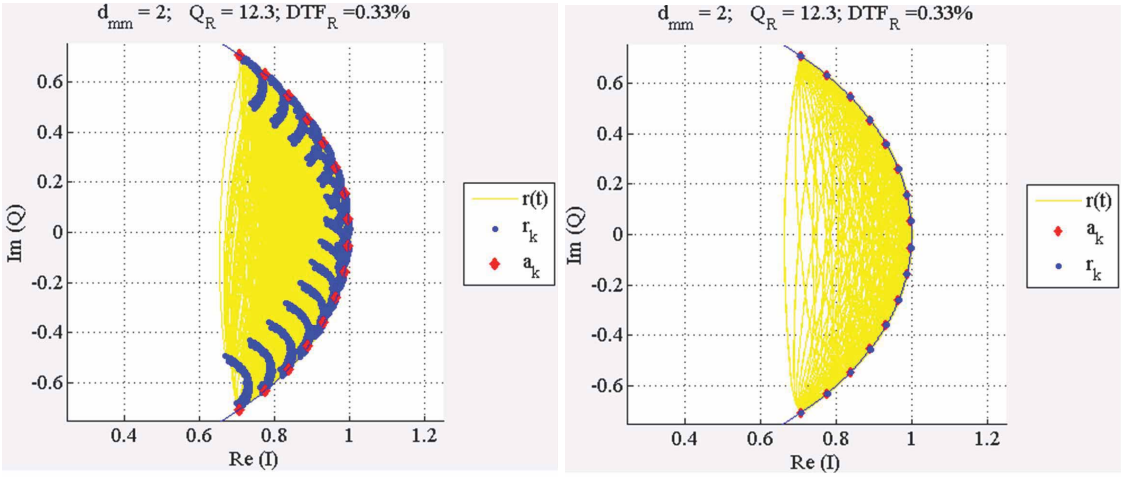


Figure 7.7.: Signal with and without a two tap pre equalizer working on twice the symbol rate

shows the signal at the air interface without pre-EQ. The red dots represent the ideal constellation diagram, while the blue points indicate the symbol in reality. These clouds around the ideal signal are caused by the quality factor of the system. It can be seen that those clouds overlap each other, which makes it difficult for the transponder to detect the correct signal. To detect the right signal would result in a complex signal processing and filtering on the transponder side, where the energy is limited. With the pre equalizer on the reader side the complex signal processing is shifted to the reader, where more energy is available. More details about the implementation of the pre equalizer on the FPGA can be found in [56] and [55].



(a) without pre-EQ (b) with pre-EQ

Figure 7.8.: 16 PSK at the air interface [55]

IQ Modulator The IQ modulator is implemented with two multipliers and an adder, the same way as depicted in Figure 6.3(a). The I value is multiplied with the sine, while the Q value is multiplied with the cosine before they are added. Since the clock frequency of the FPGA is 8 times the carrier frequency, each period is expressed by 8 samples. The samples of each period are the same, which allows to store them into a LUT, and a counter cyclically reads the values and multiplies them with the result of the pre equalizer. Since the Q value has to be multiplied by a cosine and the I with a sine, the same LUT can be used with an offset of 2, which results in a phase shift of $\pi/2$. That way the mixer can be implemented at low complexity without any CORDIC algorithm. While the inputs I and Q have a bit width of 10 bits, the output has 12 bits. Each multiplication results in a higher number of bits, and with a round operation the value is represented by 12 bits, which can be directly connected to the DAC.
In this schematic the implementation of the ASK is not shown, since it is not focus of the new development. To be backwards compatible it is possible to transmit ASK signals of Type A and B. Therefore an additional path is implemented, which replaces the PSK mapping and performs an ASK mapping instead, to use the pre-EQ as well as the same modulator. That way it is also possible to define the modulation depth by changing the entries in the LUT.

FPGA Program Receive Path

For the implementation of the receive path a detailed signal analysis was performed in advance. Based on two simulation models the requirements for the receive path where derived. The first model was the already presented simulation model in Chapter 4. Beside this model a switch state space model [57] was implemented to have the possibility to adapt the signal processing on this specific need for this communication. Both models are valid for the receive path, focusing on different topics. The described model in Chapter 4 is used for analog simulation to simulate

the signal levels in dependency of different settings. The state space model, mainly generated by the signal processing group in Klagenfurt, focuses on one specific setup and simulates the signal received on the reader with all distortions and influences like ISI. This model will only be mentioned in a few words, since the main work was done by colleagues within this project. Further information can be found in [57] or [58].
The receive path can be seen as two different time discrete linear systems, which are changed in dependency of the position of the load modulator switch. The two different systems and the switch are shown in Figure 7.9. The input u_k is the sine wave generated by the reader, while the

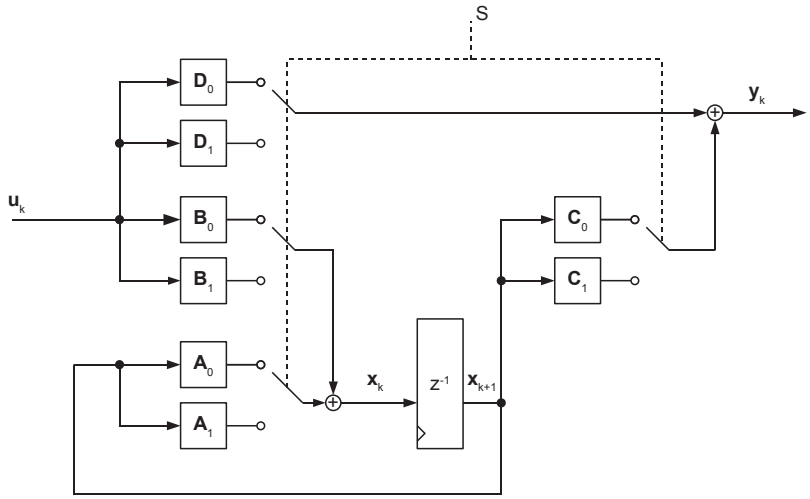


Figure 7.9.: Equivalent network of the RFID system [58]

signal y_k is the received signal on the receive path of the antenna. Depending on the position of the load modulator switch the parameters of either the opened switch (A_0, B_0, C_0, D_0) or the closed switch (A_1, B_1, C_1, D_1) are taken. The received signal y_k is calculated by

$$x_{k+1} = A_s x_k + B_s u_k \tag{7.1}$$

$$y_k = C_s x_k + D_s u_k \tag{7.2}$$

The state vectors are derived from the analog model, and in dependency of the used time steps k the accuracy of the model can be defined. The received signal is a similar representation of the received signal at the antenna and can be used to adapt the signal processing to this specific setup.
For the integration in the setup the interface to the analog domain is an ADC with 12 bits, which results in an internal bit width of 12 bits. In the FPGA there is the possibility to directly send the data which are sampled at the ADC, to the PC, to perform the signal processing on the PC, for example in Matlab. This has the advantage that different concepts can be implemented very fast and easily without being limited by timing restrictions or to program the algorithm in VHDL.
For a real reader implementation it is more interesting to have the signal processing on the FPGA and only send the processed data stream to the PC. Therefore the signal processing block is implemented on the receiver side of the FPGA as depicted in Figure 7.10.

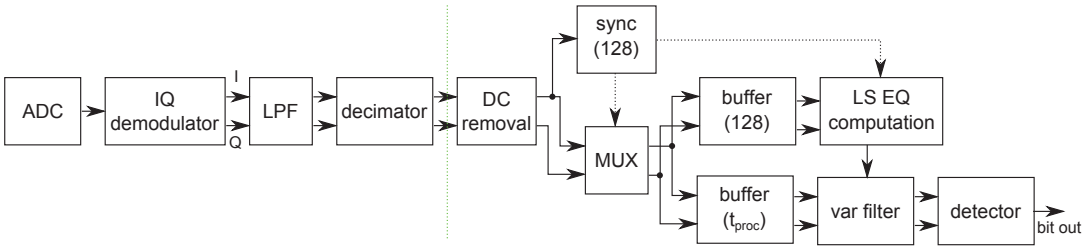


Figure 7.10.: Block diagram of the RX FPGA design

IQ Demodulator The IQ demodulator performs a demodulation to get the I and Q samples from the received signal. This is done by separating the signal. One path is mixed with the sine, and the second with the cosine of the carrier. That way the received signal is separated in an I and Q path, which represents the signal in the constellation diagram.

LPF The low pass filter removes the higher frequent parts, which are caused by the mixer. By mixing the signal the received signal is converted to the base band, but an additional spectral component at twice the carrier frequency is present in the signal. To remove this component the signal is filtered with a cut off frequency of 7 MHz.

Decimator Till this point the sampling rate of the signal processing is in the highest clock domain of 108.48 MHz. To reduce the complexity in the calculation the received data is decimated such that each symbol is only represented by two sampling points. This means that dependent of the data rate the down conversion has another factor, but the rest of the signal processing is clocked with the doubled data rate.

DC removal Due to the mixing and sampling an offset may occur. To reduce the required bit width to represent the symbols accurately enough the DC offset is removed by calculating the mean of the signal and subtracting it. That way the required bit width is reduced to represent the symbols.

sync The synchronization is done by a detector which observes the signal and tries to find the sync sequence which is defined in the ISO standard. The sync detection is based on an autocorrelation function.

MUX, buffer and LS EQ computation The multiplexer (MUX) is used to define, where the signal is routed. As long as the sync frame is not detected, the signal is buffered in a circular buffer with a length of 128 bits. This has to be done, since the bits, followed by the sync sequence, contain the training sequence which is needed to calculate the filter coefficients for the variable filter. As soon as the sync sequence is detected, the received signal is routed to another buffer, which stores the data while the filter coefficients for a variable filter are calculated. Therefore the reader calculates the linear equalizer vector, leading to the smallest error between the received

signal and the known training sequence. This least square equalizer (LS EQ) vector is used to filter the received signal [58] and [59].

var filter The variable filter gets its coefficients from the LS EQ computation block. That way the filter is matched to the channel, which distorts the signal, and the best performance can be achieved. The filter has a length of 3 taps, which is quite short, but if the size of the filter is increased, the computation of the coefficients needs more time and the buffer has to be increased. The size is a tradeoff between accuracy and costs.

detector Finally in the signal processing chain the detector decides which bit was sent. Due to the signal processing the signal is a time discrete amplitude continuous signal. To get a digital signal out of the detector the continuous amplitude has to be transformed in a discrete amplitude which has a defined high or low state. This step is performed in the detector.

7.3.2. Adapter

To keep the connections between the IO pins and the converters as short as possible an adapter is needed, which combines the relevant signals to a socket, which can be used to connect the converter board to the FPGA adapter. The IO pins of the ML507 are realized as male headers, which are combined at the adapter with the help of female headers. Those connections have a good connectivity as long as they are not connected and disconnected too frequently. All together there are more than 100 pins which are connected, which result in a high force to connect and disconnect the adapter.
The required signals are combined to a Harting socket, which allows to connect the adapter in a vertical position, and the connection can be plugged and unplugged easily and fast. Furthermore, the Harting socket is designed for more connection and disconnection cycles without loss of connectivity. The advantage of this short connection and the vertical mounting is that the digital part is separated from the analog domain with the highest possible distance. The digital wires, which are clocked at 108.48 MHz, are kept short to reduce the influence on the analog domain. The first version contained too long wires which had influence on the signal shaping as well as the whole analog performance due to unwanted emissions in the ground plane. The Harting socket provides the connections for the ADC, the DAC, the clock signals and the power supply of 5 V and 3.3 V.
Finally, the 16 pairs of differential IOs from the ML507 board are connected to a pin connector on the top of the adapter. Those pins are easy accessible and can be probed by the digital input of the oscilloscope. These pins are needed for debugging the FPGA design to allow probing different signals within the FPGA. To probe them they only have to be connected to the output pins by software, which can be done easily.

7.3.3. Converter

The converter is located on the vertical part of the platform and is used to convert signals from the analog domain into the digital domain and vice versa.

The converter is based on [52], with some improvements in the circuit as well as changes in the layout, mainly to improve the performance and increase the analog sensitivity.
On the left side of Figure 7.11 the ADC is located. The conversion is done by the ADS5520 from Texas Instruments and has a resolution of 12 bit [60], which perfectly fits in the reader concept. The differential input range of 2.3 V_{pp} allows a voltage resolution of around 562 μV exploiting the full range. This high accuracy makes the reader very sensitive, and the analog receiving performance is mainly limited by the analog part, which is used to process the signal before it is sampled.
The maximum sampling rate of the IC allows 125 Msps. This sampling rate is not used in this setup, since there is no clock domain on the FPGA providing this frequency. Furthermore, it is easier for the signal processing to have a clock frequency, which is an integer multiple of the carrier frequency. Therefore the ADC is clocked with the clock reference from the FPGA at 108.48 MHz, resulting in 8 samples per period.
Another benefit of this ADC is that it requires a single supply voltage of 3.3 V. With the low power consumption of 578 mW it is possible to power the ADC by the FPGA, which prevents an additional power supply.

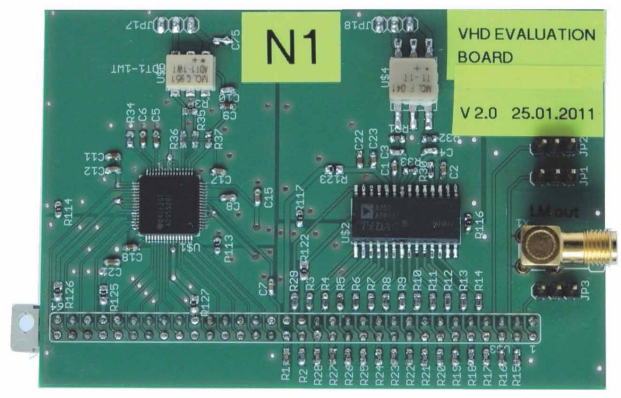


Figure 7.11.: VHD converter board

The ADC requires a differential input, which means that a transformer is needed to transform the single ended signal to a differential one. Another benefit of the transformer is that the signal is galvanically decoupled from the analog board. That way there is no ground connection between the analog part and the converter, which ensures a more stable ground on each part.
The DAC is an AD9752 from Analog Devices and is placed in the middle part of the converter. Due to the concept of SDR the signal is generated on the FPGA and is only converted to the analog domain by the DAC. To allow a high analog precision of the amplitude and phase modulated signal, the DAC needs a high resolution to convert the signal accurately. With a resolution of 12 bit and a sampling frequency of 108.48 MHz, although the highest possible sampling frequency is 125 Msps [61], this DAC fits ideally in the concept. The required voltage supply of 3.3 V and 5 V are both provided by the FPGA, which allows to use the DAC without additional external voltage supply.
The output of the DAC is differentially and drives up to 20 mA output current. To use the signal at a single ended connection it has to be transformed by a transformer. This transformation enables

an unloaded output voltage up to 800 mV. Again the transformer decouples the signal such that there is no connection between the ground of the analog part and the converter.
On the right side of the converter additional outputs can be found such as the LM control signal which is provided at the SMA connector as well as the male header. Furthermore, two more digital signals are provided which can be used to trigger external measurement devices or indicate a new period or a certain state of the program.
In the first version the converter had a common and single ground plane over the whole PCB. This has introduced many distortions in the analog signal which decreased the SNR of the sampled signal as well as the output of the DAC. To reduce the influences of the digital signal on the analog signal the layout was modified to improve the performance by introducing several different ground planes.
Due to the high frequency of the digital signals and fast changes of the state they introduce a distortion in the ground plane. Especially for the analog part of the ADC it is important to guarantee a stable ground, since all amplitude changes can be interpreted as load modulation from the transponder, if they are strong enough. To keep the ground as stable as possible 4 separate ground domains where introduced. The digital part of the ADC as well as the DAC have an own ground plane which are connected at the Harting socket to the ground of the ML507 board. The digital control signals for the LM and additional digital signals are combined at the ground plane of the DAC.
Furthermore the analog domains of the ADC and the DAC have their own ground plane, which are connected at two points with the related digital plane. This can be seen in the layout in Appendix B. With the help of those steps the influence of the digital signals on the analog ground can be minimized.
As mentioned before the ground plane of the converters are separated from the ground of the analog part completely by the transformer. The secondary side of the DAC transformer and the primary side of the ADC transformer are connected to the ground of the analog PCB, while the secondary respectively primary side is referred to the ground of the related converter. That way the ground planes are galvanically decoupled from each other, which guarantees a more stable ground, and no ground loop between the voltage supply of the FPGA and the analog part can be generated.
Finally, as few signals as possible were routed on the bottom ground plane of the converter. Due to the continuous ground plane, and the placement of most components on the averted side of the FPGA and analog PCB, it is used as electrical shield to minimize distortions on the amplifier and on the ML507 board.

7.3.4. Evaluation Board

The analog PCB is separated in several functional blocks which are needed for the full reader functionality. The PCB is depicted in Figure 7.12. On the left side the connectors to the converter board can be seen, where the signal from the DAC as well as the signal to the ADC is connected. The PCB is separated into 4 parts, which all have separate ground planes to reduce interactions, which can be seen in the Figure. On the bottom side of Figure 7.12 the transmit amplifier is located with the filters to smoothen the signal. Above, on the left hand side, the AGC circuit is located, which regulates the input signal to the desired level. The power supply unit of the PCB is located on the right side next to the AGC. On the right boarder of the PCB the power supply

unit for the FPGA can be seen, which is used in demonstration setups to reduce the number of external voltage sources.

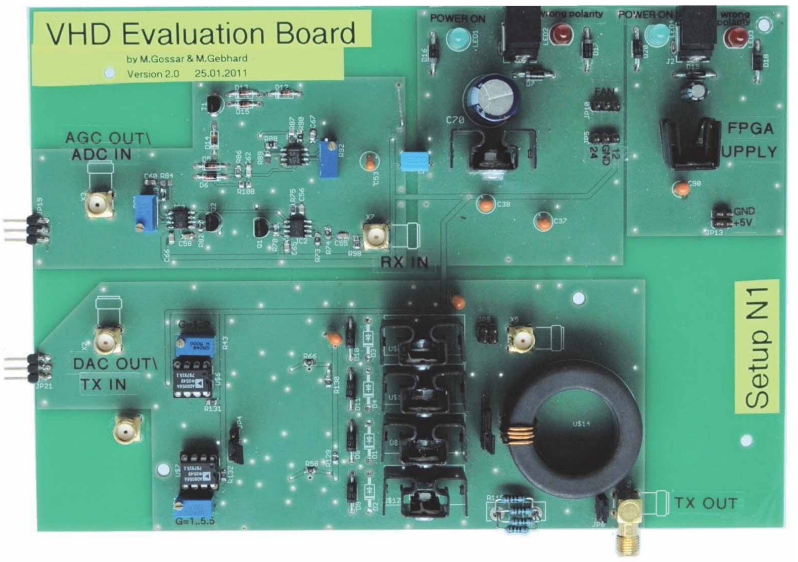


Figure 7.12.: VHD evaluation board

Transmit Amplifier

The transmit amplifier has to amplify the signal to the desired field strength and filter the higher harmonics, which are mainly caused by the clock frequency of the DAC.
To dimension the amplifier, the required output power has to be taken into account. The setup should achieve a field strength H of 7.5 A/m at a distance x of 37.5 mm according to [17]. The used antenna in this setup is standardized in [38], with a quality factor Q of 35, a radius r of 7.5 cm and one turn $N = 1$. As described in Subsection 3.1.1 the antenna has an inductance L of 480 nH.
According to Biot-Savart (Equation 7.3), the current I in the antenna conductor has to be 1.57 A, assuming the parameters above.

$$I = \frac{H\sqrt{r^2 + x^2}^3}{N\,r^2} \tag{7.3}$$

The required output power P_0 of the amplifier is calculated based on the required current and the antenna parameters with Equation 7.4.

$$P_0 = \frac{2\pi f_c L I^2}{N^2 Q}, \tag{7.4}$$

The input of the antenna is matched to $R = 50\,\Omega$, which means that the required voltage U_{rms} can be calculated as

$$U_{rms} = \sqrt{R\,P_0^2}. \tag{7.5}$$

Calculating the required peak to peak voltage of the output by

$$U_{pp} = \frac{U_{rms}}{\sqrt{2}}, \tag{7.6}$$

results in an output voltage of 67 Vpp in the unloaded case, to achieve the required field strength.To achieve this output voltage, the amplifier would require a supply voltage of more than ± 35 V in case of differential supply or an input voltage of 70 V, if the amplifier is single supplied. In laboratory environment it is more practical to use a single supply to reduce wires and the requirements of the power source. Most commercial power adaptors have an output voltage of 3.3, 4.5, 5, 6, 9, 12, 18 or 24 V, sometimes 48 V. Some also provide higher output voltage, but they are more expensive than with lower output voltage and due to the lower demand, they are harder to find off the rack. Furthermore, the power amplifier can be powered with ± 15 V, or in the single supply mode with 30 V. Therefore an power adaptor with 24 V is the requirement to keep it commercially available and reduce costs.
To achieve a higher output voltage, the amplifier is realized as four quadrant amplifier with two paths. Each path amplifies the signal, one non inverted and the other one inverted, and the signals are combined at the output stage again like depicted in the block diagram of the transmit amplifier in Figure 7.13. The signal from the DAC is connected to the first amplifier which has

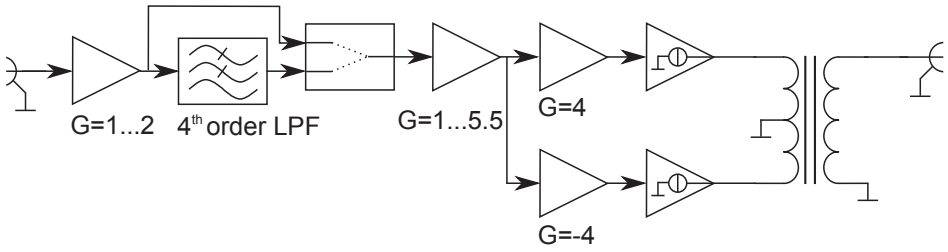


Figure 7.13.: Transmit amplifier block diagram

a variable gain between 1 and 2. This amplifier is mainly used to amplify the signal before it is filtered and not to load the output of the transformer, respectively the output of the DAC. The amplifier has a single supply voltage of 12 V, and to use it as full wave amplifier, an offset of 6 V has to be added to the signal. Therefore the signal is decoupled from the transformer by a capacitor and the offset is added. The circuit can be found in Appendix B.
The amplified signal is connected to two serial multi feedback low pass filters of 4th order, with a cut off frequency of 27.24 MHz, which is more than twice the carrier frequency. Before the signal is connected to the high voltage amplifier an additional non inverting amplifier is used with a variable gain factor between 1 and 5.5 to adjust the output voltage.
There is also the possibility to bypass the low pass filter for different applications. Either it can be bypassed if all harmonics should be transmitted, or if a higher bandwidth is required. Or if the amplifier is used to amplify a signal, which is already filtered like from a signal generator.
The described components are all powered by 12 V which limits the output voltage. The implementation of the filter and the amplifiers is done by broadband operation amplifiers from Analog Devices. The AD8056 has a bandwidth of 300 MHz at a gain factor of 1 [62], which is ideal for this application.
The used high voltage amplifiers have a fixed gain, meaning that the variation of the output voltage and according to that, the field strength is defined by the amplifiers realized with the AD8056

chips. To avoid clipping of the signal, the input of the high voltage amplifiers should not exceed 5.5 V. With the implemented gain factors and the maximum output voltage of 800 mV of the DAC, it is possible to amplify the signal up to 8.8 V. A higher voltage than the 5.5 V would not destroy any elements, but the signal will clip which results in unwanted higher harmonics and distort the signal. Nevertheless the gain factor was chosen to amplify the signal from other sources as well, or if the DAC is not used in the full range, if a lower resolution should be simulated. Furthermore, it is possible to increase the supply voltage to 30 V, which is the maximum for the high voltage amplifiers, and then a higher input voltage would be needed. Due to the design of the supply unit this will not be a problem, since the 12 V are generated on board, as will be explained later.
At this point the signal is separated into two paths as shown in Figure 7.13. The signal is once amplified by the factor of 4, and the second path is amplified by a gain of -4. That way two paths are generated, which are inverted to each other. By combining them after the amplification the doubled output voltage can be achieved. The amplifiers are realized by THS3091 high voltage, low distortion current feedback operational amplifiers. They are supplied by 24 V and have a bandwidth of around 200 MHz at a gain of 4 [63].
High voltage amplifiers have the tendency to start oscillating, which makes it necessary to keep the voltage supply as stable and clean as possible, and the feedback loop as short as possible, not the get any distortions in the feedback loop. Figure 7.14 shows the circuit of the non inverting amplifier. The input signal is DC decoupled from the first amplifier stage by the capacitor C1. This has to be done because of the 6 V offset of the first part, based on the supply voltage of 12 V. This amplifier has a supply voltage of 24 V and to amplify both half waves the offset has to be set to half of the supply voltage, which is done by the voltage divider R3 and R4. Additionally, to keep the offset voltage clean, the input voltage of the divider is decoupled by an additional resistor R2 and stabilized by two capacitors C4 and C5. The same is done for the power supply of the amplifier by the resistor R1 and the capacitors C2 and C3. That way the influence of the amplifier on the supply voltage is minimized.

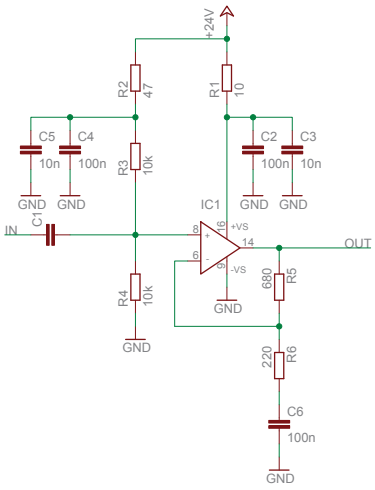


Figure 7.14.: High voltage amplifier circuit

The feedback loop is realized by the resistors R5 and R6 and the capacitor C6. This capacitor is required since the amplifier is not based on ground at the input, instead it is referred to an offset

of 12 V. With the help of this capacitor a virtual level of 12 V is generated, and it does not require and additional voltage divider.
The circuit and the layout can be found in Appendix B. For the design of the amplifier it was tried to keep the required area as small as possible, to reduce influences from outside, such as coupling from other devices, and to keep a closed ground plane on the other layer, to shield the whole circuit. Furthermore, it was necessary to keep the feedback loop as short as possible not to get any distortions or oscillations. The first two versions of the amplifier had the problem that they started oscillating at a certain amplitude. This problem was solved by reducing the length of the feedback loop and move it to the second layer. An additional problem was caused by the amplifier itself. The IC has a power plate on the bottom, which has to be connected to ground for cooling purposes. Due to the many components around the amplifier, the ground plane had a lot of interruptions which reduced the cooling capability. To increase it again, a via had to be added to have a better heat dissipation, which did not allow the shortest connection of the feedback loop. A compromise with a little increased length and a via solved the problem.
Each high voltage amplifier allows to drive an output current of 350 mA. Not to overload them and reduce the heat at the IC, an additional current amplifier was added to boost the output current. The most promising amplifier concept for this prototype is the AB amplifier described in [64] and [65].
Realizing the current amplifier with two transistors, one NPN and a PNP transistor, allows to amplify the output current. The used transistors are the BD139 and BD140, which have a maximum input voltage of 80 V and an output current of 1.5 A [66]. With the circuit shown in Appendix B, the current is amplified and the ICs are relieved.
To combine the differential signal to a single ended signal, a broadband ferrite balun FT140-61 [67] is used. The output of each path is connected to a single turn on the balun, while the secondary side has two windings to increase the output voltage.

Receive Path

The input signal from the antenna can vary between 1 V and 5 V depending on the field strength which is set by the transmit amplifier. To reduce the complexity in handling the evaluation reader, an AGC circuit is used to guarantee the maximum input range of the ADC and to protect it from overload. For the design of the AGC, different aspects have to be taken into account. On the one side the AGC has to be fast enough to follow changes, caused by detuning the antenna, if a transponder is located in the field or the amplification of the transmit amplifier is changed, and on the other side it has to be slow enough not to cancel the load modulation of the transponder.
The block diagram of the AGC is shown in Figure 7.15. A voltage follower is used, not to load the RX pin of the antenna and make the system more stable. This voltage follower is in front of two amplifiers with a variable gain, which form the AGC. Finally an additional variable amplifier, which can be tuned by hand, is used to set the output level to any desired level. Since the AGC itself has a limited input and output range, the additional amplifier is used to set the output to any level, if another voltage is required. In this case the ADC has an input voltage of maximum 2.3 V, which can be tuned by this amplifier, since the AGC is set to 2 V. To set the output voltage to 2 V at an input voltage from 1 V to 5 V, the AGC has to have a gain from 0.4 to 2. As seen in Figure 7.15, the AGC is implemented with two identical inverting amplifiers, which requires to split the gain factor for each amplifier. To achieve a total amplification from 0.4 to 2, the square root is taken

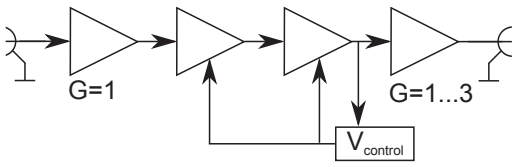


Figure 7.15.: AGC block diagram

and each amplifier has to have a gain factor from 0.63 to 1.41.
To realize a variable amplifier a JFET is used which is used as variable resistor in the feedback loop. That way it is possible to change the gain factor by changing the voltage at the JFET which changes its resistance. Simulations have shown that the resistance R_{DS} between drain and source changes from 300 Ω to 700 Ω at a voltage between gate and source V_{GS} of -1 V to -2 V. Since everything in the AGC is related to an offset of 6 V the control voltage $V_{control}$ has to vary from 4 V to 5 V. The bias point of each amplifier is defined such that the gain g is 1 at a resistance of the JFET of $R_{DS} = 500\,\Omega$. Defining $R_2 = 500\,\Omega$, R_1 has to be $250\,\Omega$, according to

$$R_1 = \frac{1}{g} \cdot \frac{R_2 \cdot R_{DS}}{R_2 + R_{DS}}. \tag{7.7}$$

Another problem is that the JFET does not have a linear resistance R_{DS}, which can be easily linearized by an additional 100 Ω resistance between gate and drain.
The control voltage for the JFETs are generated with the help of the output signal. As can be seen in the schematic in Appendix B, the output is rectified, and with the help of a variable rectifier the control voltage can be defined. To tune the control voltage to the desired level the gain factor has to be tuned to 1 if a sine wave of 2 V_{pp} is connected at the input. After this tuning step the AGC works automatically for the desired input range.
One problem appears in this design. If the circuit is turned on, the capacitor in the control loop is discharged and has to be charged such that the control loop is functional. The problem of this design is that this means that the input of the AGC is amplified with the maximum gain till the control loop is settled. According to the design the AGC always regulates the output from the maximum to the desired level. This could harm the input of the AGC, which makes a compensation necessary.
The easiest way is to pre-charge the capacitor which is responsible for the control voltage. If this capacitor is pre-charged the gain factor will be low, and as soon as the pre-charge voltage is removed, the control loop starts to work. Therefore an additional circuit is implemented which connects the capacitor to the positive supply voltage when it is turned on, and as soon as a certain level is reached the voltage is disconnected, not to distort the regulation.

Supply Unit PCB

The whole analog board is supplied by a single 24 V source. The high voltage amplifiers require an input voltage of 24 V, while the AGC and the AD8056 need 12 V. To reduce the number of external power supplies an on board voltage regulator is used to generate the 12 V. Both supply voltages are stabilized by capacitors to reduce any high frequent distortions on the supply voltage. The 12 V domain is generated by an LT7812 which provides 1.5 A [68].

To make the board more user friendly a reverse polarity protection is added, which indicates the wrong polarity by a red LED.
Additionally two connectors are added, which provide 12 V and 24 V to power external devices, such as a fan, if the reader is embedded in a housing.
There is no voltage regulator for the 24 V domain on the PCB to have the possibility to increase the supply voltage up to 30 V for testing. All elements, which are connected to the 24 V domain can also be powered by 30 V, which can be used to increase the output power if needed.

Supply Unit ML507 Board

The same way the power supply for the PCB is generated on board there is an additionally power supply unit implemented for the case the FPGA board should also be powered without an additional power supply. This could be used for demonstration purpose to reduce the number of connections to the environment. The unit is built similarly to the supply unit for the PCB with a voltage regulator and reverse polarity indication.

8. Performance Characterization

This chapter summarizes the performance characterization of the implemented evaluation reader, described in Chapter 7. In the first part of this chapter the analog performance of the individual blocks are characterized, such as output power, output current and bandwidth. The second part characterizes the evaluation reader in its function as reader for demonstration. Therefore the signal quality at the air interface is evaluated and the full demonstration setup, including the transponder, is shown.

8.1. Analog Components

For the characterization of the evaluation reader, the analog blocks are measured isolated from each other to gather the required information. This means that the analog blocks are separated and measured individually depending on the characteristic parameters of the individual blocks.
Some elements are just tested during the soldering process, such as the connector board, where only the connections from one board to another are realized. The performance characterization of the ADC and DAC are not described in detail. For the test of both different ramp signals are either generated by the FPGA and sampled by an oscilloscope, or a signal generator provided test tones which are sampled by the FPGA and compared in Matlab.
The characterization of the program on the FPGA is done during the test of the whole demonstration setup, if all commands lead to the expected results.

8.1.1. Transmit Amplifier

As already described, the transmit amplifier has to filter and amplify the signal to ensure the correct data transmission over the air interface. Relevant parameters are the output power, current and voltage amplification, the provided bandwidth and frequency characterization as well as the noise figure of the amplifier.

Output Power

One important parameter of the amplifier is the output power and the range, where the output power can be varied. To measure the output power directly a shunt resistance is connected to the output of the amplifier and the voltage is measured. The output power can be calculated according to

$$P = \frac{\left(\frac{V_{pp}}{2\sqrt{2}}\right)^2}{R}. \tag{8.1}$$

The shunt resistance has a value $R = 50\,\Omega$. According to Equation 8.1 the output power range is from 30 mW to 828 mW. This results in a maximum field strength of 3.2 A/m at the ISO setup. This achievable field strength is enough for a demonstration reader to show the reader functionality as well as to perform different measurements. The output power is also enough to compare the evaluation reader to commercially available readers, due to the fact that most of them provide an output field between 1 and 2.5 A/m. Based on that the reader can be used as demonstrator with product like behavior. The lack of output power is caused by the output matching to 50 Ohm, which is realized by a serial resistance, as well as the reduction of the supply voltage. As the calculations have shown the required input voltage would be higher, but due to the easier availability of a 24 V voltage source, a little decrease of power will be accepted. Nevertheless, it is too less to fulfill the requirements to perform full ISO compliant measurements, where the reader has to provide a field strength up to 7.5 A/m. Therefore there will be additional improvements on the output power, which will be described in Chapter 9.

Current Amplification

Another parameter is the current amplification over the whole chain. To measure the current amplification the input current is compared with the output current according to

$$I_{gain} = \frac{I_{out}}{I_{in}}. \tag{8.2}$$

The input current is measured with the help of a resistance, where the voltage drop is measured and the current can be calculated. The output current is measured the same way as before, with the help of a shunt resistance.

I_{in}	0.412 mA
I_{out}	364 mA
I_{gain}	883

Table 8.1.: Current characteristic

Table 8.1 summarizes the measured values. The current amplification over the whole chain is good, but too low to achieve the target of 7.5 A/m.

Voltage Amplification

The output voltage range can be changed from $V_{out\_min} = 7.25\,\text{V}$ to $V_{out\_max} = 37.1\,\text{V}$ if the output is unloaded. Using a $50\,\Omega$ load at the output the range is limited to $V_{out\_max} = 18.2\,\text{V}$.

Bandwidth

The bandwidth of the setup is a very important parameter, since the main focus of the analog development was on a large bandwidth to transmit the signals at very high bandwidth if required. The low pass filter in the beginning of the amplifier chain limits the bandwidth, but it can be

disconnected to allow the whole bandwidth range. Figure 8.1 shows the bandwidth of the full setup at different gain factors when the output is loaded. For the measurement the amplifier is disconnected from the ADC and connected to a network analyzer sweeping the frequency from 300 kHz to 60 MHz. As seen in the figure, the lower cut of frequency is around 1.8 MHz. This

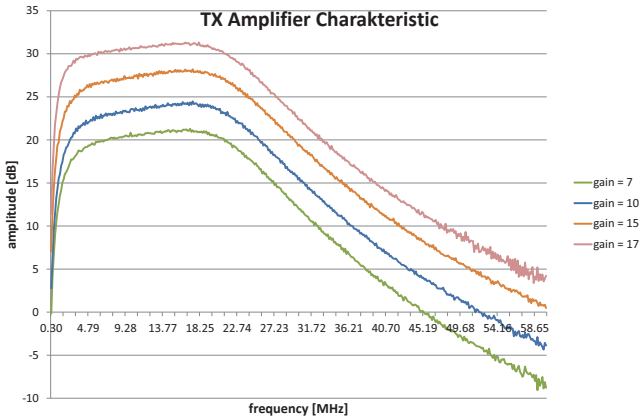


Figure 8.1.: Transmit amplifier characteristic

lower cut off frequency is caused by the balun which is used to combine the two paths in the amplifier. The carrier is at 13.56 MHz, therefore the lower cut of frequency does not influence the signal, since no DC offset is required. The upper cut of frequency is above 24 MHz. As

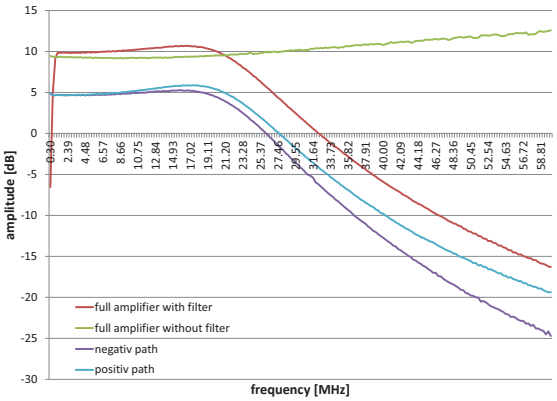


Figure 8.2.: Transmit amplifier characteristic

mentioned before there is also the way to disconnect the input filter to use the whole bandwidth. Figure 8.2 shows again the output signal of the amplifier without ADC and measured with the network analyzer. The red curve shows the bandwidth of the amplifier with input filter and balun, resulting in a lower and upper cut off frequency. If the input filter is disconnected it can be seen that the characteristic increases slightly over the whole range up to 60 MHz, but for the findings within this project the whole range will not be used, therefore this slight increase does not cause any problems. Furthermore there is the way to use each path on its own. If the balun is disconnected, each path, the negative as well as the positive, is connected to a separate

output. The characteristic of both with the input filter can be seen in the same figure as well. The separated output can be used to drive differential antennas without any limitations.

Signal Quality

The noise figure of the amplifier is very good and is above the expectations. To compare the amplifier with other amplifiers the noise figure NF is calculated according to

$$NF = SNR_{in,dB} - SNR_{out,dB}. \tag{8.3}$$

The noise figure of the amplifier is 6 dB, which is very satisfying and competitive with commercially available amplifiers.

8.1.2. Receive Path

The AGC has different parameters which are important for the correct functionality. The main parameter at the AGC is the output voltage range related to the input voltage range. To define the behavior of the AGC, the dynamic range (DRange) of the input and the output is defined. Equation 8.4 indicates the relation from the lowest to the highest voltage, and defines the DRange of the input and the output separately.

$$DRange = \frac{V_{max}}{V_{min}} \tag{8.4}$$

For the measurement the AGC was connected to a frequency generator which provides a signal at carrier frequency and a voltage sweep. Figure 8.3 shows the output voltage as function of the input voltage. It is shown that the output voltage has a linear gain for an input range from 1 Vpp to 6 Vpp. The output voltage increases from 1.8 Vpp to 2.5 Vpp. According to Equation 8.4, this means the output has a DRange of $DRange_{out} = 1.39$, compared to $DRange_{in} = 6$ of the input. The noise figure of the AGC is calculated with Equation 8.3 and results in $NF_{AGC} = 2$ dB.

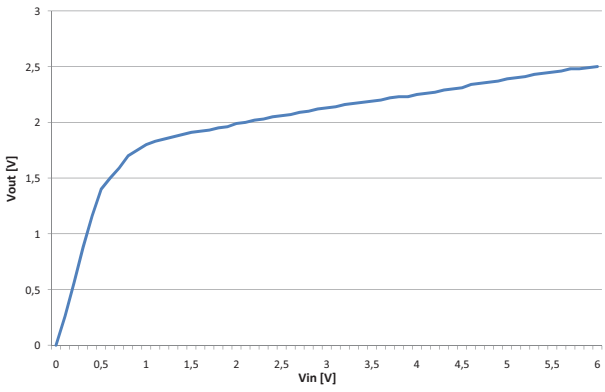


Figure 8.3.: AGC output characteristic

The required time is $\tau = 10\,\mu s$ to follow any amplitude changes at the input. According to that it

is fast enough to follow any changes in the amplitude, caused by detuning of the transponder or if the output power is changed, but slow enough not to distort any received signal at the input.

8.1.3. Supply Unit

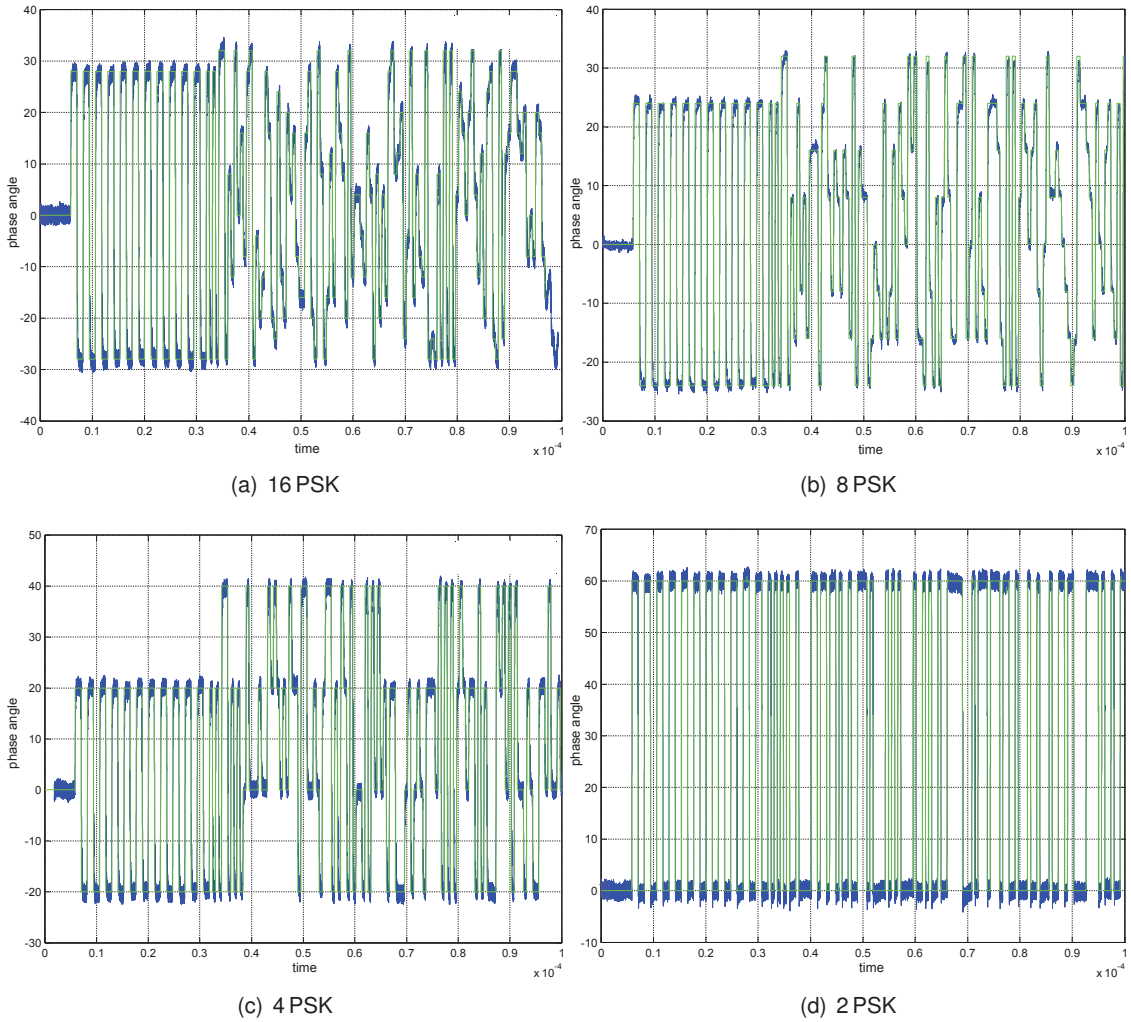
The supply unit does not require any special specifications, since the only functionality is to provide the supply voltage for the whole board. The input voltage of 24 V is divided into an additional 12 V power domain to supply the filter, amplifier and AGC. The used IC provides 1.5 A, which is not needed and so there are not any limitations as well.

8.2. System Performance

To test the whole performance of the system the full setup is connected and the different communication directions and modulation schemes are tested. The reader antenna is placed in the ISO setup to fulfill all requirements for a full ISO compliant test. The signal is sampled at the air interface with the help of the sense coil, which is also used to define the field strength. To evaluate the signal at the air interface, parts of the ISO measurement setup for VHD is used, which is also developed within this project [69]. Only the required elements were used and combined in a stand alone measurement setup to evaluate the reader, without time and processing overhead. With this setup it is possible to define different parameters and if the ISO requirements are fulfilled, the reader passes the test. Different PSK orders as well as data rates are tested to show the whole functional range and flexibility of the reader.
Figure 8.4 shows different PSK orders at a symbol duration of $f_c/8$, which result in different data rates, listed in Table 7.1. A difference between the ideal phase states of the signal, plotted in green, and the sampled and decimated signal, plotted in blue, can be seen. This difference is caused by the limited bandwidth of the antenna and the matching circuit.
The frames, which are plotted, contain the start of frame (SOF) sequence, which is defined in Appendix A.3. The SOF consists of a calibration sequence, a synchronization sequence and a training sequence, which is used to estimate different parameters for the signal processing on the transponder side. Depending on the PSK order, different modulation angles can be noticed.
Although there is a little difference between the ideal and real signal, the reader passes all different signal tests.
Another parameter which is measured is the error vector magnitude (EVM). The definition of the EVM is shown in Figure 8.5 and indicates how accurate the signals are, and how much distortion is added to the signal. Therefore the distance between the ideal and the real signal is calculated according to

$$EVM = \frac{\sqrt{\frac{1}{N}\sum_{J=1}^{N}\left[\left(I_J - \widetilde{I}_J\right)\left(Q_J + \widetilde{Q}_J\right)\right]}}{|\vec{v}_{max}|}. \tag{8.5}$$

I_J is the I part of the received signal, while $\widetilde{I}_J$ is the part of the ideal signal. The same is defined for the Q part of the symbol. If all received signals are added and normalized, the EVM is calculated and indicates the accuracy of the symbols. If the available bandwidth is reduced by



(a) 16 PSK (b) 8 PSK

(c) 4 PSK (d) 2 PSK

Figure 8.4.: Phase of different PSK orders measured at the air interface

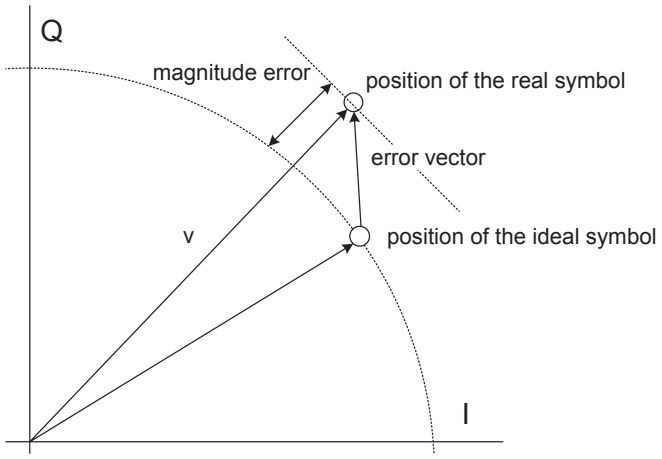


Figure 8.5.: EVM definition

using an antenna with an higher quality factor, the EVM increases. To transmit data within the ISO specifications, the pre equalizer has to be enabled, to allow to fulfill the requirements. Figure 8.6 shows the EVM with and without pre equalizer and an antenna with a quality factor of 35. It is shown that the pre equalizer reduces the EVM significantly, and the specifications defined in Appendix A are fulfilled. The curves for the EVM with the pre equalizer show a minimum between 5 and 6 cm. This is due to the fact that the filter coefficients of the pre equalizers are optimized to a distance of 5.5 cm. Optimizing the filter coefficients for lower distance would decrease the EVM at lower distance, but also increase it at higher distance. An optimization to 5.5 cm is a good trade off for the communication. From reader point of view the use of a pre equalizer is more energy efficient than a reduction of the quality factor and increasing the output power, which would lead to the same result. Further details can be found in [55] and [56].

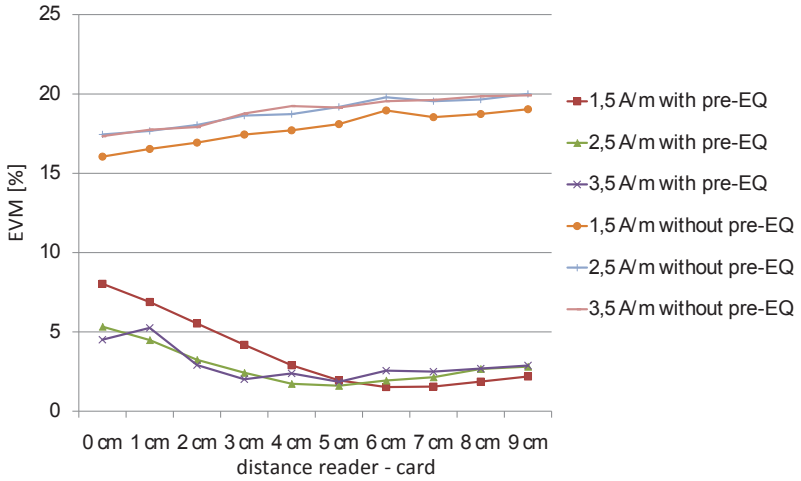


Figure 8.6.: EVM comparison at different field strengths

The output signal of the reader completely fulfills the specification and so the evaluation reader is

tested together with an analog front end IC for VHD, which is also developed in the same project. The IC is only a test IC which is able to demodulate the PSK signal, and outputs a digital signal, representing the phase stage of the received symbols. With the help of an FPGA the data are filtered and processed before they are compared with the reference signal to calculate the BER and the frame errors. Due to the Hamming coding a certain number of bit errors can be corrected within a frame, but if there are too many bit errors, the whole frame is corrupted and has to be retransmitted.
On the right side of Figure 8.7 the evaluation reader can be seen beside the first PC, which controls the reader functionality. In the middle the air interface with the reader antenna is located with the transponder on top of it. The flat cable of the transponder transmits the digital signal to the second FPGA, where the received signal is processed and the BER is calculated. The bit stream is sent to the second PC, where the BER is calculated.

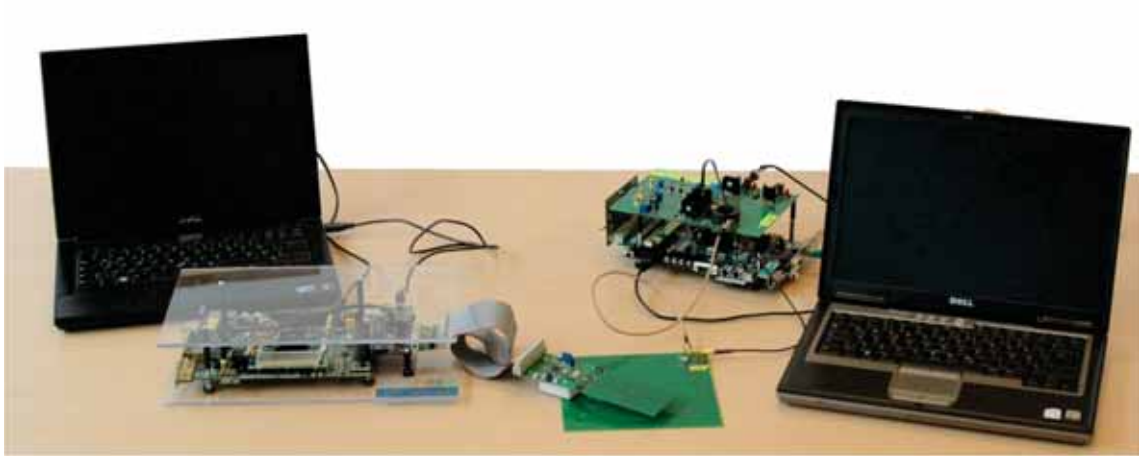
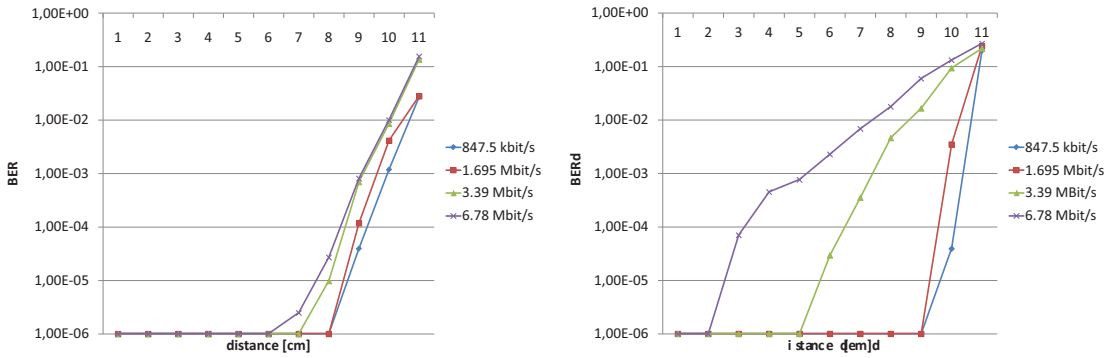


Figure 8.7.: Full VHD demonstration setup

Due to the fact that the focus of this work is on the reader side, it is only mentioned that it is possible to transmit data from the reader to the transponder, with the setup shown in the figure up to a distance of 13 cm, at a field strength of 2 A/m. The first bit errors occur at a distance of 8 cm, but with the Hamming code and the error correction it is possible to correct the bit errors that no frame is corrupted and the communication is possible without retransmitting single frames. The first frame errors occur at a distance of 13 cm.
For the evaluation reader the receive path is important as well to show the full reader functionality. Unfortunately the VHD transponder does not support the load modulation due to the fact that the focus was on the receive path of the transponder, and there were not any constraints to send data as well. Therefore the BER measurement for the communication direction from transponder to reader is done with the reference PICC. The new generation of the VHD transponder will also provide an LM to support the communication in both directions.
The evaluation reader is connected to the antenna and is providing the field, which is needed to power the transponder, as well as to allow the load modulation. The receive signal is connected over the dumping resistors, as described in Subsection 3.1.3, to the receive structure of the evaluation reader.

Figure 8.8 shows the BER for different quality factors and data rates over the distance. The



(a) Q8 (b) Q35

Figure 8.8.: BER of the communication PICC to PCD

floor of the measurement was defined to be at a BER of 10e-7. The field strength was set to 2.5 A/m without transponder in the field. Due to detuning the field strength decreases once the transponder is located in the field, which can be observed at commercial readers as well. The limiter voltage of the transponder was set to 3 V for all measurements and the resonance frequency to 15.5 MHz. To calculate the BER 100000 frames, each consisting of 1024 symbols, are transmitted. Figure 8.8(a) shows the BER with an antenna with a quality factor of 8. It can be seen that for short distances up to 6 cm no error occurred. Increasing the distance the BER is increasing as well. It is shown that the BER increases earlier at higher data rates. Increasing the data rate means to reduce the symbol duration, which results in a higher bandwidth requirements, and the ISI is increased. A range of 6 cm without errors is seen as a good result for the demonstration setup.
Increasing the quality factor to 35 also means to reduce the available bandwidth. This means that the communication channel bandwidth is reduced, introducing more ISI on the signal, which results in more errors at the detection. In Figure 8.8(b) it is shown that the first errors already occur at low distance, especially for higher data rates. Even if the transponder has the same parameters as before, the BER increases due to the higher quality factor of the reader. At a data rate of 6.78 Mbit/s the first errors occur already at 2 cm, while the communication with 3.39 Mbit/s is stable till 5 cm. This trend also shows the importance to allow fall back solutions. If the BER is increased up to a certain level, the system has the possibility to reduce the transmission data rate to allow a more stable communication.

8.3. Conclusion

The characterization of the evaluation reader has confirmed the full functionality. It was shown that the reader is able to transmit the required signals within the defined specifications, and the development of the pre equalizer enables the use of a higher quality factor. The reader is able to transmit different PSK orders, different data rates and subcarrier frequencies, even outside the specification. Furthermore it is possible to transmit ASK signals at 106 kbit/s up to 848 kbit/s to allow the communication with current transponders.

The analog performance of all elements is satisfying, except for the output power of the transmit amplifier. The achievable field strength of 3.2 A/m is high enough for demonstration purposes, since most commercially available readers provide less than this, but to perform full ISO compliant measurements, which was an additional idea for this reader, the output power has to be increased. The increase of the output power is described in Chapter 9.
The receiver of the evaluation reader is very flexible and is not limited to any special signal shape. With the implemented LS EQ the channel can be filtered in dependency of the specific distortions caused by different transponders. The concept of SDR allows a high degree of freedom and the performance is very good and can be used as base for further developments.

9. Evaluation of Reader Modifications

This chapter outlines the possibility to improve the output power of the current evaluation reader. By modifying the output impedance circuit the output power can be increased up to 1 W. Another possibility is to increase the supply voltage to 30 V, resulting in an increase of the output power. Beside the improvement of the output power the implemented IQ demodulator will be introduced by a few words.

9.1. Increase of the Output Power

The aim is to achieve an output power to be able to drive 7.5 A/m at the ISO antenna. The first versions of the amplifier achieved a fraction of that and the developed and characterized evaluation reader is able to drive 828 mW, resulting in a field strength of 3.2 A/m. The voltage amplification is at its borders with a supply voltage of 24 V. The problem is that the loaded output voltage is decreasing from 37.1 V to 18.2 V. To increase the output power, the current amplifier stage is modified to drive a higher output current. Therefore the input stage of the current amplifier is modified to increase the input current. This also results in a higher load of the high voltage amplifier. According to that change, the unloaded output voltage is still at 38 V, but the loaded output achieves an output voltage of 20 V, resulting in an output power of 1 W. With this output power, it is possible to drive an field strength of 3.62 A/m, which is more, but still below the ISO requirements.
Furthermore the output impedance is adapted more accurately to 50 Ω using an additional capacitor and a lower resistance to guarantee an output impedance of 50 Ω real and 0 Ω imaginary. The changes are already updated in the schematics.
Another way to improve the output power of this setup is by increasing the voltage. For that only the supply voltage has to be increased, since the 12 V devices have an on board voltage regulator and the high voltage amplifier and the transistors can be supplied up to 30 V. This voltage increase also increases the output power slightly.

Version	supply voltage	$V_{out,unloaded}$	$V_{out,50\,\Omega}$	P_{out}	field strength
evaluation reader	24 V	37.1 V	18.2 V	828 mW	3.20 A/m
improved version	24 V	38.0 V	20.0 V	1 W	3.62 A/m
improved version	30 V	48.2 V	23.9 V	1.43 W	4.30 A/m

Table 9.1.: Output of the amplifier at different settings

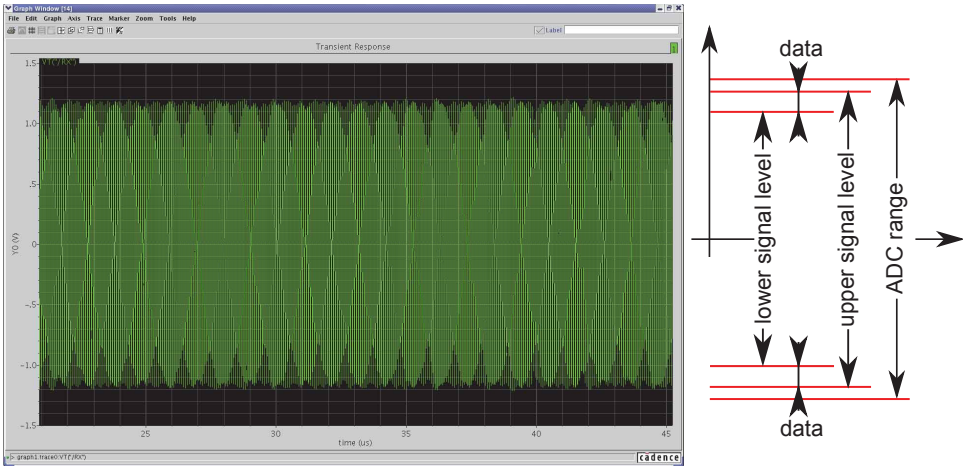
It is shown in Table 9.1 that the output power is increased by an adaption of the current amplifier stage, as well as a more accurate matching at the output. Additionally an increase of the supply voltage increases the output power, resulting in 4.3 A/m. This is still below the ISO requirement,

but more than 1 A/m improvement compared to the original version.
Another change in the layout is an additional connector to connect the reader to a commercially available amplifier, which is specified in the ISO standard. To use the signal processing of the evaluation reader and send the signals to the amplifier it has first be filtered before it is amplified, since the commercially available amplifier has a very wide bandwidth and would amplify the higher harmonics, resulting in steps in the carrier field. To use the LPF, an additional output is created which can be connected if required. An additional attenuator reduces the voltage level, since otherwise the minimum field strength of 1.5 A/m would not be achieved, due to the high amplification factor of the commercially available amplifier. Using this amplifier allows to drive a higher field strength as well as to reach the field strength with a low Q antenna.
Compared to the first versions of the amplifier and reader the output is matched to 50 Ω. The first versions did not have this matching to generate a higher field strength. The output matching to 50 Ω reduces the output power, but this has to be done to evaluate the reader correctly. If the output is not matched to 50 Ω, the matching circuit has a different quality factor as well as frequency behavior. It would be possible to adapt the matching network to the output of the reader, to get a defined quality factor as well as frequency behavior, but then the connection between the output stage and the antenna has to be short. If the connection should be realized by a wire, matched to 50 Ω, it would result in errors. This changed behavior improves the BER for the communication from card to reader, since the quality factor is lower, and the time constant decreases. This results in a higher bandwidth, and the signal produced by the transponder is much cleaner than at a higher quality factor. This reduces the complexity of the signal processing and the BER will improve.
On the other hand a mismatch between the antenna and the output impedance will decrease the BER from PCD to PICC, since the pre equalizer is set to the wrong channel and therefore the signal will be distorted.
To have a lab scaled prototype, the output matching requires a matching to 50 Ω, although it means a lower output power.
The actual evaluation reader concept, presented in this thesis has a very good BER performance. Compared to the beginning of the project the BER is reduced significantly, which is achieved by an improve in the digital as well as analog part. The analog part has a stable behavior, achieved by ground plane separation, and additional elements such as the AGC guarantee an optimized usage of the used components, since the ADC range is fully used. Furthermore, the digital signal processing is adapted to the specific needs of this setup. A well defined definition of a preamble allows to calculate filter parameters to adapt the signal processing continuously.

9.2. IQ Demodulator Concept and Prototype

As mentioned in Chapter 6 another concept beside the SDR, which is used for the current evaluation reader, would be the IQ demodulation in front of the ADC. The change of this concept is minor, since the principle stays the same, but the IQ conversion of the signal is done in the analog domain instead of in the digital domain.
For the signal processing on the FPGA the concept stays the same with the difference that instead of one signal from the ADC, two signals are provided which are already IQ demodulated. This means the block diagram of Figure 7.10 is equal with the difference that the I and Q signal

after the IQ demodulator block is provided by the ADCs.
Comparing the ADR concept with the analog IQ demodulator it can be seen that the received signal has a very low amplitude variation. As described in Subsection 5.2.4 and Section 6.3, the amplitude variation of the load modulation is very small, also depicted in a plot of a simulation in Cadence in Figure 9.1(a). This is caused by the limited bandwidth of the system. To demodulate



(a) Time domain (b) ADC distribution

Figure 9.1.: Received signal

the received signal, the whole signal has to be sampled, resulting in the sampling of a large carrier without any information and little data on top of it. Figure 9.1(b) shows the distribution of the signal levels. The ADC has a maximum input range of 2.3 Vpp resulting in a voltage resolution of 562 µV. The AGC regulates the input voltage of the ADC to 2.2 Vpp to enable a little margin, to protect the ADC from overvoltage.
With an 100 % range of 2.3 V of the ADC, an amplitude of 2.2 V uses 94.7 % of the ADC range. With a modulation of 13 % this results in 87.2 %, or above 2 Vpp, where only carrier, without any information is sampled. Sampling the received signal without any analog signal processing or mixing means that more than 87 % of the signal is just carrier without any information.
This leads to high requirements for the ADC, since the resolution of this little margin where the data are located have to be sampled with an accuracy which is high enough to distinguish the amplitude levels and detect the load modulation.
To reduce the requirements for the ADC the down conversion can be shifted to the analog domain. For this project an additional IQ demodulator is implemented with discrete elements in the analog domain. It consists of two separate mixers as is depicted in Figure 9.2. The received signal from the antenna is connected to a variable amplifier to adapt the level to the desired input level of the mixers. The reference signal for the mixer signal is extracted from the TX amplifier of the reader. Since the received signal requires a certain time, which results in a phase delay, a variable phase shifter is implemented to tune the reference to be phase synchronous to the received signal. An additional phase shifter performs the phase shift of $\pi/2$ for the second mixer. The output of each mixer is filtered by a multi feedback LPF of 4-th order with a cut off frequency of 6.7 MHz. And finally a capacitor removes the DC offset before the signal is sampled by 2 ADCs.

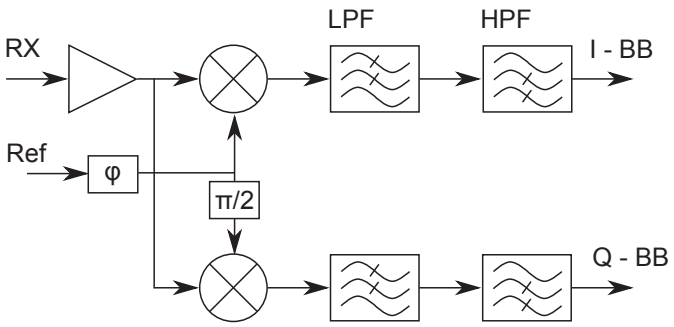


Figure 9.2.: Concept of the analog IQ demodulator

Figure 9.3 shows the output of the simulation in cadence. It can be seen that the amplitude range has changed and the signal has to be amplified if the same ADC should be used. Due to the conversion into the baseband and the reduction of the spectral frequency at the doubled carrier, the signal is much cleaner. The load modulation can be seen, but there is still a frequency component at 27.12 MHz left on the signal, caused by the lower order LPF. The baseband signal can now be sampled by two ADCs with lower requirements to achieve the same performance.

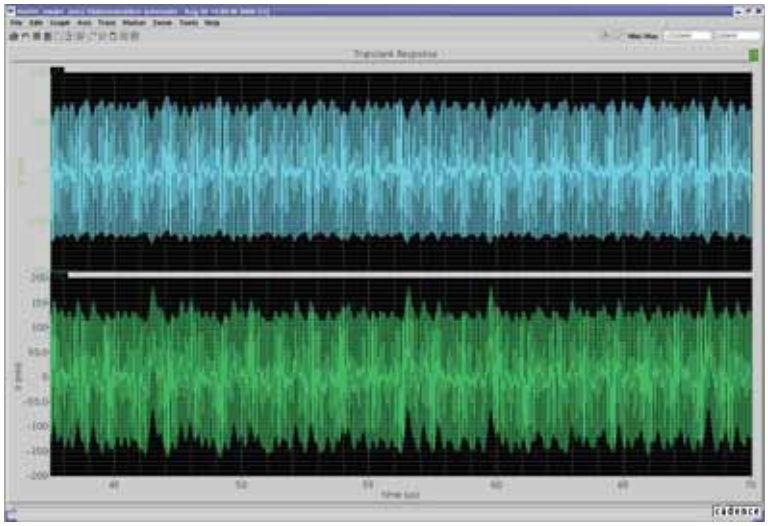


Figure 9.3.: I and Q signals after filtering

Those simulations show the ability and the benefit of an analog IQ demodulator. For test purpose an analog IQ demodulator was designed and produced to show the functionality.
The evaluation of the analog IQ demodulator shows a higher noise level than the SDR implementation. This higher noise level is caused by the large area of the IQ demodulator and the high field strength in close distance of the demodulator. Analog measurements show the principle functionality of the mixers and the signal levels.
The whole characterization of this setup will be done as follow up project. The analog component is provided with an additional ADC and the IQ demodulator. The missing link is the implementation of the second signal path from the ADC to the signal processing which is planed to be done in the next project.

10. Conclusion and Outlook

This chapter starts with a summary on the increase of data rates of 13.56 MHz proximity coupling RFID devices. Additionally the summary lists the results and contributions of this thesis. Although this thesis presents a fully functional system, there are possibilities for further research which will be addressed in the last section.

10.1. Summary and Contributions

The thesis has focused on the increase of the data rate from actual 848 kbit/s to a maximum of 13.56 Mbit/s for proximity coupling RFID systems. Current systems have been analyzed and a simulation model has been developed. The simulation model has been utilized to derive requirements for the increased data rates.
The first chapter gives a general introduction on RFID systems and an overview of applications using RFID technology. Furthermore, the related standards and regulation are presented. In the second chapter the basic parameters are introduced.
A mathematical description of an exemplary reader has been defined in Chapter 3 and has been used as reference system throughout this thesis. This has been done by modeling the loop antenna with their equivalent circuits. The interaction between two antennas has been represented by their coupling factor. Based on this mathematical description a simulation model has been developed to simulate various effects of the system. This model has been delivered to NXP where it is used to evaluate current products as well as new developments. Effects on the system and influences of different parameters, such as current consumption or resonance frequency of the transponder can be isolated analyzed. This model shows for example the energy range of the transponder for a field strength, taking into account the parameters of the transponder. Exemplarily the simulations have shown the relation between the limiter voltage on the transponder, the energy range and the detuning. Increasing the limiter voltage on the transponder has very little impact on the energy range, while the detuning of the system is increased significantly. Therefore a system with lower limiter voltage is preferable to ensure a more stable communication. More effects are described in Chapter 4. This model allows to show the relation between different parameters and their influences on the system.
Chapter 5 investigates different modulation schemes for RFID systems incorporating the cognitions of the system modeling. Firstly, modulation schemes for the communication direction from reader to transponder have been discussed, followed by the modulation schemes from transponder to reader. For the communication from reader to transponder the actual standard currently defines ASK. The analysis has shown that an increase of the data rate using ASK is possible in principle but has considerable drawbacks regarding bandwidth requirements. Using PSK modulation instead relaxes the bandwidth requirements. However, due to limitations in energy transmission, PSK over the whole constellation circle is not possible. Therefore, the proposed

PSK modulation uses only a certain segment of the constellation circle which allows to transmit enough energy and does not violate the specified spectral mask. Furthermore, measurements have confirmed simulation results that a reader using PSK modulation can be operated at lower field strength, transmitting the same amount of energy to a transponder compared to ASK. On top the power transfer to a transponder is more stable over time during PSK modulation.
For the communication from transponder to reader the principle of load modulation is still used, due to energy restrictions. To increase the data rate in this communication direction different modulation patterns have been investigated. The modulation patterns have been analyzed in terms of bandwidth requirements and communication stability. It has been shown that an alphabet of four patterns results in the most stable performance in terms of power spectral density and communication robustness.
Finally, the development results discussed from Chapter 3 to Chapter 5 have been proposed as ISO/IEC 14443 amendment to the ISO standardization community. The draft documents can be found in Appendix A. Moreover, the proposals contain a protocol structure for both communication directions to ensure a stable communication and defined activation of the higher data rates [23].
Due to the fact that neither the new defined PSK modulation, nor the defined modulation pattern for the load modulation can be transmitted, respectively, received by current reader products, a evaluation reader has been developed. Therefore various possible reader structures have been compared. For the implementation of the reader two paths have been analyzed separately. The receive path and the transmit path. For the receive path two main concepts can be used. On the one hand a single antenna structure, on the other hand a two antenna structure. The benefit of a two antenna structure is the separation of a transmit antenna from the receive antenna. Therefore each antenna can be optimized to its specific functionality. The transmit antenna is used to provide the carrier field and transmit the data from the reader to the transponder, while a receive antenna with a low quality factor is used to receive the information from the transponder. Optionally the receive antenna can be shaped differentially, resulting in an improved reception performance. A special shaped differential antenna can cancel out the carrier field. Thus, only the secondary field of the transponder containing the data is received. This approach is described in Chapter 6.
The focus in this thesis has been set to a single antenna solution where the concept of SDR is the most suitable one for the usage as evaluation reader. The signal at the antenna is regulated by an AGC before it is sampled by an ADC and the signal processing is performed on the FPGA. The transmit path has been implemented based on the concept of SDR. The signal is generated on the FPGA and converted to the analog domain by a DAC. Based on the requirements of the previous chapters the implementation of the evaluation reader with its hardware is described in Chapter 7.
Chapter 8 presents the characterization of the evaluation reader. All analog parts have been characterized and described in this chapter. It has been shown that the evaluation reader has full reader functionality fulfilling all requirements. It is possible with the developed reader to cover all standardized data rates from 106 kbit/s to 848 kbit/s ASK modulated and new proposed data rates up to 13.56 Mbit/s PSK modulated. Additionally, the reader also provides the higher data rates up to 13.56 Mbit/s ASK modulated to compare it with competitor's proposals and deal with different protocol structures.
As positive side effect, the flexible structure of the setup also enables the use for other standards and protocols as well. Therefore the setup can be used for example for tests of the NFC standard

[18], or other standards such as [16] or [70]. This multi usability allows an inexpensive test setup for first communication and characterization tests.
Beside the development of the SDR approach an analog IQ demodulator has been implemented. Therefore the received signal is demodulated in the analog domain by two mixers and the demodulated signal is sampled by two ADCs. This approach has the advantage that the requirements for the ADCs decrease, since the carrier is removed and base band signals are directly sampled. In the SDR concept a single ADC has to sample the carrier with the data. The drawback of this analog IQ demodulator is the limited filter order in the analog domain and the additional noise introduced by the higher area requirement. Nevertheless both setups are functional, but the SDR concept is used for the demonstrator.
Finally, this setup enables the full reader functionality for usage in product-like demonstration. This demonstration setup has already been used in live-demonstrations presenting the communication up to 13.56 Mbit/s.

10.2. Research Summary

The following section summarizes the achievements of this doctoral thesis with respect to scientific research. To enhance the actual highest data rates of 848 kbit/s to the wanted very high data rates of 13.56 MHz, various aspects had to be taken into account. With the increase of the data rate the bandwidth requirement is increased as well, which would not be possible with the current topology of the reader, due to its very limited bandwidth. Therefore the system is analyzed and different coding schemes are evaluated to find the most suitable coding scheme for the communication.
At the beginning of the research work current reader products were analyzed. This was done to get an understanding of the RFID system itself, and compare different reader topologies to each other. The advantages as well as disadvantages of each product are listed, and the various elements are evaluated, if they are reusable for the new requirements. Unfortunately none of those products could be adapted, due to the high required bandwidth for the transmission at very high data rates.
Due to the fact that a new reader has to be implemented, simulation models where created to define a list of requirements for the new reader. As reference for the reader and card model the ISO setup was defined as general usable reader device. Based on this system an accurate simulation model was created in Matlab, simulating different parameters and influences on the system. Based on those simulations it could be clearly shown, that actual products do not have the capability to transmit or receive very high data rates, which lead to the development of a novel evaluation reader for very high data rates, enabling the transmission as well as reception of the new signals.
The same model was used to simulate various influences of the system, if a transponder is lowered to the reader. These simulations have shown the relation of different parameters of the transponder, such as the resonance frequency or current consumption, on the system. Chapter 4 gives a detailed analysis of those influences on the system. The first time all parameters of the transponder can be changed and the influences of those changes can be simulated to enable the optimization of the transponder as well as reader setup. The understanding of those phenomena such as detuning allows to optimize the signal processing and adapt the algorithms

to the needs of this product.
Furthermore the model was used to define framework conditions for the development of very high bit rate communication systems, such as maximum allowed quality factor. If the quality factor is increased, the energy efficiency of the reader is increased, resulting in a limited bandwidth, introducing more ISI to the signal. Furthermore the operating range could be defined at a certain field strength and power consumption of the transponder.
Moreover, due to the strict regulation concerning the spectral mask (described in Section 1.5), a modulation scheme had to be found, which enables the communication at very high bit rate. Furthermore, it had to be ensured that enough power is transmitted to the transponder without violating the spectral mask. This is achieved by a phase modulated signal with a modulation angle of 60 degrees, described in Section 5.1. The use of PSK instead of ASK modulation is new in 13.56 MHz RFID systems, and required a new transceiver structure on the reader side, as well as a new receiver concept on the transponder side.
For the communication from transponder to reader the concept of load modulation is still the same as in current products, but an alternative modulation pattern was used to guarantee a stable communication. All analysis have shown that 4 PSK has spectral advantages compared to the actually used 2 PSK and detection advantages compared to higher order PSK. The simulation as well as measurements have shown that 4 PSK has the best performance in terms of stability and power transmission.
The new findings, which are defined in this doctoral thesis have led to the ISO proposal in Appendix A, which are presented at the ISO standardization meeting in 2010.
The evaluation of different reader structures in Chapter 6 has shown that two concepts are most promising. The analysis has shown that current transmitter structures cannot be used, due to the limited bandwidth at the output. The current output structure consists of two transistors, where the output is either connected to the positive supply voltage or to ground. This rectangular wave is shaped to a sine wave by an EMC filter. This filter forms the signal to a sine wave, but due to the very limited bandwidth it cannot be used for the transmission of PSK signals. Therefore a new output structure had to be found. Instead of those switching transistors an ADC is used. The ADC allows the generation of a waveform close to a sine wave, which is filtered by external components. The benefit of this approach is that the filter only has to remove the higher harmonics generated by the sampling frequency of the ADC, and does not have to shape the sine out of a rectangular wave. With the implemented hardware the clock frequency is 8 times the carrier frequency, and to generate a smooth sine wave a low pass filter of 4th order is used with a cut off frequency of 27.24 MHz instead of 13.56 MHz in case of the switching transistors. This high bandwidth enables the transmission of PSK signals without distortion.
The achievement of this step is to show the possibility to generate a sine wave at high accuracy with the required bandwidth. The integration to a reader IC will be the next step but this approach has shown that it is possible to generate a sine wave with commercially available elements. The hardware implementation has lead to design rules to guarantee a stable amplification, which is realized by more specific ground planes and different supply voltages to decouple the various stages.
The developed evaluation reader allows the verification of the newly defined PSK communication in RFID systems. The hardware can be used as reader for VHD and also allows the backwards compatibility to lower data rates down to the base data rate of 106 kbit/s. This shows that the developed reader is able to deal with actual data rates, Type A and B, as well as very high data rates. The evaluation reader is used for demonstration and verification purpose.

Furthermore, the implementation of the pre equalizer for the transmit signal to reduce the influence of the matching and resonance circuit of the reader antenna is new in this application field. With the help of the pre equalizer it is possible to use high quality factor antennas even for the communication at very high data rate as shown in Subsection 7.3.1. This allows a more energy efficient usage of the reader and deal with different types of reader, antennas by changing the filter coefficients.
Summarizing the achievements a multi useable full functional evaluation reader was developed which enables testing new approaches very fast and easily due to the high flexibility in the setup. The evaluation reader can be used to verify different existing standards such as [16], [18] or [70], and enables the test of new defined concept with a carrier frequency of 13.56 MHz.

10.3. Outlook

This thesis has shown the feasibility of data rates up to 13.56 Mbit/s in RFID systems working at 13.56 MHz. The implemented evaluation reader has full reader functionality and can be used for live-shows for product like demonstration. The implemented reader is fully characterized and the functionality is guaranteed.
Beside the implemented evaluation reader, based on the concept of SDR, an IQ demodulator was implemented as add on additionally. The hardware of this analog IQ demodulator is already tested and the functionality is proved, but for full system integration the digital part on the FPGA is missing. This implementation of the digital part, the system evaluation and the comparison to the SDR will be done in a follow up project. The hardware is handed over to NXP for the final implementation and characterization.
The output power of the evaluation reader is high enough for the usage as demonstration reader and for basic evaluations, which was the scope of this thesis. The reader setup allows using single ended antennas as defined in the ISO standard, and additionally differential antennas, used in many reader products. During this thesis the idea came up to use this setup for full ISO characterization but for that the output power of the amplifier has to be increased. There are already plans for follow up projects increasing the output power.

Author's Puplications

Magazine Paper

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List of Abbreviations

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
APK	Amplitude Phase Keying
ASK	Amplitude Shift Keying
BPF	Band Pass Filter
BPSK	Binary Phase Shift Keying
BER	Bit Error Rate
CAL	Calibration Sequence
DAC	Digital to Analog Converter
DR	Data Rate
DSP	Digital Signal Processing
EAS	Electronic Article Surveillance
EMC	Electromagnetic Compatibility Filter
EOF	End of Frame
ESD	Electromagnetic Discharge
EU	European Union
EVM	Error Vector Magnitude
ETU	Elementary Time Unit
FPGA	Field Programmable Gate Array
FSK	Frequency shift keying
GUI	Graphical User Interface
HF	High Frequency
IC	Integrated Circuit
ICAO	International Civil Aviation Organization
ID	Identification
IEC	International Electrotechnical Commission
IF	Intermediate Frequency

IFF	Identification Friend or Foe
IO	Input and Output
ISI	Intersymbol Interference
ISO	International Standardization Organization
JFET	Junction gate Field Effect Transistor
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LCR	Inductance Capacitance Resistance
LED	Light Emitting Diode
LF	Low Frequency
LM	Load Modulator
LNA	Low Noise Amplifier
LO	Local Oscilator
LPF	Low Pass Filter
LS EQ	Least Square Equalizer
LUT	Look Up Table
MUX	Multiplexer
NFC	Near Field Communication
NRZ	Non Return to Zero
NRZ-L	Non Return to Zero, L stands for level
OOK	On-Off Keying
PCB	Printed Circuit Board
PCD	Proximity Coupling Device
PICC	Proximity Integrated Circuit Card
PLL	Phase Locked Loop
pre-EQ	pre equalizer
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
RAM	Random Access Memory
RFID	Radio Frequency Identification
RMSE	Root Mean Square Error
SDR	Software Defined Radio

SNR	Signal to Noise Ratio
SOF	Start of Frame
SYNC	Synchronisation Sequence
TSC	Trainings Sequence
UHF	Ultra High Frequency
USB	Universal Serial Bus
VHD	Very High Data

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A. Appendix ISO Proposal

This Appendix contains the most important findings and proposals for the ISO amendment, which was presented at the ISO standardisation meeting in Takamatsu 2010. Most parts were accepted in the Committee Draft, which is also available on the website of the Standardization Organization, but due to the fact that it is a Committee Draft, it is only visible for owners who have access. All findings and proposals from NXP and this project group are summarized in this Appendix, which is mainly the proposal itself, which can be found in [46]. Beside the propsals, which are already shown in Chapter 5, the relevant innovations of this proposal are combined in a few pages. This amendment was thought as enhancement of the actual ISO14443 and therefore there are only extensions, instead of a full standard. This means that the existing standard stays the same, and only the parts for the very high data rates are added. All accepted amendments would be added in the current standard and would be published as soon as it is accepted. Due to strong counteractions from outer companies, only parts of this amendment are accepted. The idea to change from ASK to PSK for data rates higher than 848 kbit/s was denied and so it is only possible to use PSK above 6.78 Mbit/s currently. The proposal deals mainly with the enhancement of the data rates from 848 kbit/s to 13.56 Mbit/s, but due to the rejection, in the actual standard only data rates above 6.78 Mbit/s are defined with PSK. The current draft and committee version is also available at the standardization website with authentication. Due to the limitations in the current draft version, the actual development focus is on the data rate above 6.78 Mbit/s, which is also possible with the current evaluation reader setup.

A.1. PSK Modulation from PCD to PICC

For the modulation from reader to card different modulation schemes are possible. The focus of this work is on an elementary time unit (ETU) of 8/fc. Nevertheless the other time units should be defined as well, and the reader should be able to provide the data. Table A.1 lists all different PSK orders and subcarrier frequencies and the related data rates.

A.1.1. PSK Signal Parameters for the Modulation

To ensure the interoperability of this system, the generated symbols at the air interface have to be defined. Therefore two main parameters can be used to define the constellation diagram. Figure A.1 shows the constellation diagram of the 4 PSK, which is defined by M, the order of PSK and Φ_{Seg}, the portion of the circle used for the modulation. It is defined as the angle of the outermost symbols in the constellation diagram.

The symbol interval Φ_{SI} is defined by the order of PSK M and the angle of the constellation diagram as:

Phase N Unitary Φ_{Seg}	2 PSK $2 = 2^1$ Φ_{Seg} = 60°	4 PSK $2 = 2^2$ Φ_{Seg} = 60°	8 PSK $8 = 2^3$ Φ_{Seg} = 56°	16 PSK $16 = 2^4$ Φ_{Seg} = 60°
1 ETU ≅ 16/fc		4PSK16: fc/8 (~1.695 Mbit/s)	8PSK16 fc/(16/3) (~2.54 Mbit/s)	16PSK16: fc/4 (~3.39 Mbit/s)
1 ETU ≅ 8/fc	2PSK8: fc/8 (~1.695 Mbit/s)	4PSK8: fc/4 (~3.39 Mbit/s)	8PSK8: fc/(8/3) (~5.09 Mbit/s)	16PSK8: fc/2 (~6.78 Mbit/s)
1 ETU ≅ 4/fc	2PSK4: fc/4 (~3.39 Mbit/s)	4PSK4: fc/2 (~6.78 Mbit/s)	8PSK4: fc/(4/3) (~10.179 Mbit/s)	16PSK4: fc (~13.56 Mbit/s)
1 ETU ≅ 2/fc	2PSK2: fc/2 (~6.78 Mbit/s)	4PSK2: fc (~13.56 Mbit/s)		

Table A.1.: Different PSK modes

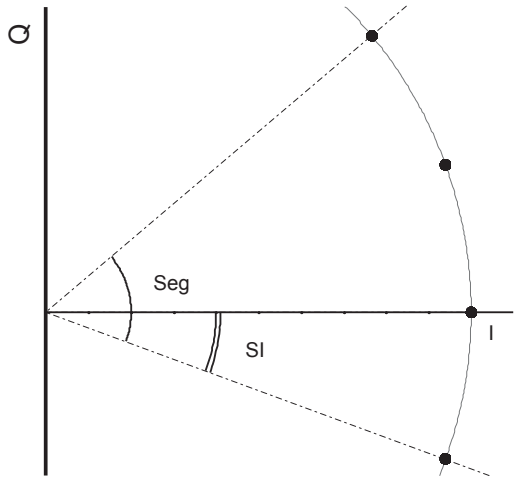


Figure A.1.: PSK modulation parameter illustration

$$\Phi_{SI} = \frac{\Phi_{Seg}}{M-1}$$

The reader has to provide a field with the constellation angle, specified in Table A.2.

The same time the PICC has to allow a certain uncertainty of the signal and the IQ constellation for the reception is defined in Table A.3.

A.1.2. ISI Parameters

The antenna matching and resonance circuit lead to a bandwidth limitation, which introduces ISI, resulting in clouds around the origin constellation point. This is shown in Subsection 7.3.1, where the pre equalizer is introduced. To define a maximum allowed ISI, the clouds have to be defined,

PSK order M	Parameter	Min	Max
2,4,16	Φ_{Seg}	58	62
8	Φ_{Seg}	54	58

Table A.2.: PCD transmission: IQ segment parameters for all PSK modes

PSK order M	Parameter	Min	Max
2,4,16	Φ_{Seg}	56	64
8	Φ_{Seg}	52	60

Table A.3.: PICC reseption: IQ segment parameters for all PSK modes

which is done with the parameters ISI_m and ISI_d. ISI_m is the ISI magnitude, normalized to the symbol interval Φ_{SI} and ISI_d the ISI rotation. Instead of observing ISI_m directly, the distance between the two outermost points of an ISI cloud L can be measured and the corresponding ISI_m can be calculated as:

$$ISI_m = \frac{\arcsin(\frac{L}{R})}{\Phi_{SI}}$$

where R is the amplitude of the original constellation points, depicted in Figure A.2.

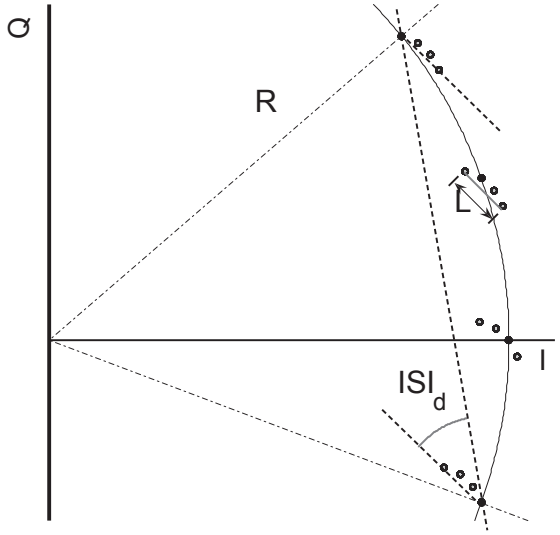


Figure A.2.: ISI parameter illustration

The ISI magnitude ISI_m generated by the PCD shall be as specified in Table A.4. The parameter $ISI_{d,lim}$ is used in the condition field.

Furthermore the PICC shall be able to receive an amount of ISI as specified in Table A.5

Parameter	PSK order M	Condition	Min	Max
ISI_m	2	-	0	0.5
ISI_m	4, 8, 16	abs(ISI_d) $> ISI_{d,lim}$	0	0.5
ISI_m	4, 8, 16	abs(ISI_d) $\leq ISI_{d,lim}$	0	1.8
$ISI_{d,lim}$	2	-	N/A	N/A
$ISI_{d,lim}$	4, 8, 16	-	20°	20°

Table A.4.: PCD transmission: ISI parameters

Parameter	PSK order M	Condition	Min	Max
ISI_m	2	-	0	0.52
ISI_m	4, 8, 16	abs(ISI_d) $> ISI_{d,lim}$	0	0.52
ISI_m	4, 8, 16	abs(ISI_d) $\leq ISI_{d,lim}$	0	1.9
$ISI_{d,lim}$	2	-	N/A	N/A
$ISI_{d,lim}$	4, 8, 16	-	21°	21°

Table A.5.: PICC reception: ISI parameters

A.1.3. Phase Noise

Any physical signal will in practice be contaminated by noise. In the case of a PSK modulated signal, it is the noise in the phase component of the signal (also known as the phase noise) that could affect reliable data recovery and should therefore be within limits. Similar to ISI, such phase noise would be visible in a constellation diagram as clouds around the wanted constellation points. It is possible to distinguish the two due to the fact that ISI can be modeled by a linear filter response of the transmitted signal, whereas noise, of course, cannot.
The amount of noise added to the PSK signal (on top of the ISI) is defined by PN_{RMS}, which is the root-mean-square phase component of the noise, present in the PSK signal, normalized to a symbol interval Φ_{SI}. Normalizing to the symbol interval means that the measured RMS phase noise is expressed in degrees and this number has to be divided by the symbol interval Φ_{SI} (also expressed in degrees) to yield PN_{RMS}. The amount of phase noise by which the PCD signal is contaminated is specified in Table A.6

Parameter	Min	Max
PN_{RMS}	0	0.030

Table A.6.: PCD transmission: Phase noise parameters for all PSK rates

The PICC on the other side has to be able to receive an amount of noise as specified in Table A.7

A.2. Bit Representation and Coding

The signal processing chain of the source data, which are transmitted to the receiver is shown in Figure A.3. The data is transmitted in symbols, and each bit rate has its individual symbol

Parameter	Min	Max
PN_{RMS}	0	0.032

Table A.7.: PICC reception: Phase noise parameters for all PSK rates

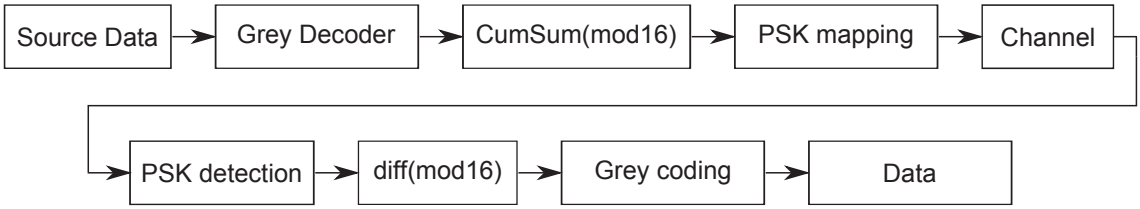


Figure A.3.: Signal processing chain for VHD rates

alphabet. This is caused by the number of bits, which are combined in a symbol. For 2 PSK the binary information is encoded in 2 symbols allowing an information content of 1 bit per symbol. Using 4 PSK allows an information content of 2 bits per symbol, 8 PSK allows 3 bits and 16 PSK allows 4 bits per symbol.
The following part will define the information chain for each PSK order.

A.2.1. Bit Representing and Coding for 2 PSK

According to Figure A.3, the first step is the Gray decoding of the source data. The mapping can be seen in Table A.8. The second step forms the cumulative sum of the data according to:

Source data	Gray decoder out
0	0
1	1

Table A.8.: Source data to Gray decoding for 2 PSK

$$out(n) = (out(n-1) + in(n))\text{mod2}$$

Afterwards the output is mapped to the PSK symbol as described in Table A.9

On the transponder side the symbols are mapped to the binary information according to Table A.9. Afterwards the differential of the symbols are calculated according to:

$$out(n) = (in(n) - in(n-1))\text{mod2}$$

The final step restores the source data by the Gray decoding according to Table A.10

A.2.2. Bit Representing and Coding for 4 PSK

According to Figure A.3, the first step is the Gray decoding of the source data. The mapping can be seen in Table A.11. The second step forms the cumulative sum of the data according to:

Phase state	Cumsum out 2 PSK
$\phi_0 + 60°$	0
ϕ_0	1

Table A.9.: PSK mapping for 2 PSK

Diff out	Data replica
0	0
1	1

Table A.10.: Data replica by Gray decoding for 2 PSK

$$out(n) = (out(n-1) + in(n))\text{mod4}$$

Afterwards the output is mapped to the PSK symbol as described in Table A.12

On the transponder side the symbols are mapped to the binary information according to Table A.12. Afterwards the differential of the symbols are calculated according to:

$$out(n) = (in(n) - in(n-1))\text{mod4}$$

The final step restores the source data by the Gray decoding according to Table A.13

A.2.3. Bit Representing and Coding for 8 PSK

According to Figure A.3, the first step is the Gray decoding of the source data. The mapping can be seen in Table A.14. The second step forms the cumulative sum of the data according to:

$$out(n) = (out(n-1) + in(n))\text{mod8}$$

Afterwards the output is mapped to the PSK symbol as described in Table A.15

On the transponder side the symbols are mapped to the binary information according to Table A.15. Afterwards the differential of the symbols are calculated according to:

$$out(n) = (in(n) - in(n-1))\text{mod8}$$

The final step restores the source data by the Gray decoding according to Table A.16

A.2.4. Bit Representing and Coding for 16 PSK

According to Figure A.3, the first step is the Gray decoding of the source data. The mapping can be seen in Table A.17. The second step forms the cumulative sum of the data according to:

$$out(n) = (out(n-1) + in(n))\text{mod16}$$

Afterwards the output is mapped to the PSK symbol as described in Table A.18

Source data	Gray decoder out
00	00
01	01
10	11
11	10

Table A.11.: Source data to Gray decoding for 4 PSK

Phase state	Cumsum out 4 PSK
$\phi_0 + 40°$	00
$\phi_0 + 20°$	01
ϕ_0	11
$\phi_0 - 20°$	10

Table A.12.: PSK mapping for 4 PSK

On the transponder side the symbols are mapped to the binary information according to Table A.18. Afterwards the differential of the symbols are calculated according to:

$$out(n) = (in(n) - in(n-1))\text{mod16}$$

The final step restores the source data by the Gray decoding according to Table A.19

A.3. Start of Frame

For very high bit rates, the standard frame contains a start of frame (SOF) field and an end of frame (EOF) field.
The SOF consists of the calibration sequence (CAL), which is 44 elementary time units (ETU) long, followed by the synchronization sequence (SYNC) lasting for 4 ETU, and a training sequence (TSC) with 92 ETU terminates the SOF.

The constitution of the calibration sequence and the synchronization sequence is generic, the same principle is applied to all VHD PSK modes.
The calibration sequence consists of 2 symbols of the IQ segment, depending on the PSK order. A portion of 2 equal symbols is alternating with a portion of 2 other equal symbols. This sequence

Diff out	Data replica
00	00
01	01
10	11
11	10

Table A.13.: Data replica by Gray decoding for 4 PSK

Source data	Gray decoder out
000	000
001	001
010	011
011	010
100	111
101	110
110	100
111	101

Table A.14.: Source data to Gray decoding for 8 PSK

Phase state	Cumsum out 8 PSK
$\phi_0 + 32°$	000
$\phi_0 + 24°$	001
$\phi_0 + 16°$	010
$\phi_0 + 8°$	011
ϕ_0	100
$\phi_0 - 8°$	101
$\phi_0 - 16°$	110
$\phi_0 - 24°$	111

Table A.15.: PSK mapping for 8 PSK

Diff out	Data replica
000	000
001	001
010	011
011	010
100	110
101	111
110	101
111	100

Table A.16.: Data replica by Gray decoding for 8 PSK

Source data	Gray decoder out
0000	0000
0001	0001
0010	0011
0011	0010
0100	0111
0101	0110
0110	0100
0111	0101
1000	1111
1001	1110
1010	1100
1011	1101
1100	1000
1101	1001
1110	1011
1111	1010

Table A.17.: Source data to Gray decoding for 16 PSK

Phase state	Cumsum out 8 PSK
$\phi_0 + 32°$	0000
$\phi_0 + 28°$	0001
$\phi_0 + 24°$	0010
$\phi_0 + 20°$	0011
$\phi_0 + 16°$	0100
$\phi_0 + 12°$	0101
$\phi_0 + 8°$	0110
$\phi_0 + 4°$	0111
ϕ_0	1000
$\phi_0 - 4°$	1001
$\phi_0 - 8°$	1010
$\phi_0 - 12°$	1011
$\phi_0 - 16°$	1100
$\phi_0 - 20°$	1101
$\phi_0 - 24°$	1110
$\phi_0 - 28°$	1111

Table A.18.: PSK mapping for 16 PSK

Diff out	Data replica
0000	0000
0001	0001
0010	0011
0011	0010
0100	0110
0101	0111
0110	0101
0111	0100
1000	1100
1001	1101
1010	1111
1011	1110
1100	1010
1101	1011
1110	1001
1111	1000

Table A.19.: Data replica by Gray decoding for 16 PSK

CAL	SYNC	TSC
44 ETU	4 ETU	92 ETU

Figure A.4.: SOF definition

is transmitted 11 times, resulting in 44 ETU in total.
For 2 PSK the sequence starts with 2 symbols of 60° followed by 2 symbols of 0°.
For 4 PSK the sequence starts with 2 symbols of 20° followed by 2 symbols of - 20°.
For 8 PSK the sequence starts with 2 symbols of 24° followed by 2 symbols of - 24°.
For 16 PSK the sequence starts with 2 symbols of 28° followed by 2 symbols of - 28°.
The synchronization sequence consists of the same 2 symbols as the calibration sequence. The sequence starts with the symbol of the positive phase. One symbol alternating with the other symbol is transmitted 2 times, which results in 4 ETU in total.
The training sequence is specific for each PSK order separately. For the first frame which is transmitted, the TSC consists of 92 ETU, for all following frames the TSC consists of 28 ETU. The idea of two different frames is to initialize the system with a longer TSC, since all parameters have to be estimated. For the following frames the first parameters will be used and updated with the second TSC to save communication time. The concept of the TSC is a pseudo-random sequence, a definition for every data rate is listed in Tables A.20 to A.23.

ETU No	phase state	ETU No	phase state	ETU No	phase state	ETU No	phase state
1	60	24	0	47	60	70	60
2	0	25	0	48	0	71	60
3	60	26	60	49	60	72	0
4	0	27	60	50	0	73	60
5	0	28	60	51	0	74	60
6	60	29	0	52	60	75	0
7	0	30	60	53	0	76	0
8	0	31	0	54	0	77	60
9	0	32	0	55	60	78	0
10	0	33	0	56	60	79	0
11	60	34	0	57	60	80	0
12	60	35	60	58	60	81	60
13	0	36	0	59	60	82	0
14	60	37	60	60	0	83	0
15	60	38	0	61	0	84	60
16	0	39	60	62	0	85	0
17	60	40	0	63	60	86	0
18	60	41	0	64	0	87	0
19	0	42	0	65	60	88	60
20	60	43	0	66	60	89	0
21	0	44	60	67	60	90	0
22	0	45	0	68	0	91	60
23	60	46	0	69	60	92	60

Table A.20.: Phase states of the TSC for the first frame of 2 PSK

ETU No	phase state	ETU No	phase state	ETU No	phase state	ETU No	phase state
1	40	24	20	47	-20	70	20
2	40	25	20	48	40	71	0
3	-20	26	-20	49	-20	72	40
4	20	27	40	50	40	73	-20
5	-20	28	40	51	0	74	40
6	20	29	0	52	40	75	-20
7	-20	30	0	53	0	76	40
8	0	31	20	54	20	77	-20
9	40	32	0	55	-20	78	20
10	0	33	-20	56	20	79	40
11	0	34	20	57	20	80	20
12	0	35	40	58	-20	81	0
13	20	36	40	59	-20	82	20
14	0	37	-20	60	-20	83	20
15	0	38	20	61	0	84	-20
16	40	39	-20	62	20	85	40
17	20	40	40	63	-20	86	-20
18	40	41	20	64	0	87	20
19	20	42	-20	65	20	88	-20
20	0	43	40	66	0	89	-20
21	20	44	-20	67	-20	90	-20
22	0	45	0	68	20	91	40
23	40	46	0	69	20	92	20

Table A.21.: Phase states of the TSC for the first frame of 4 PSK

ETU No	phase state	ETU No	phase state	ETU No	phase state	ETU No	phase state
1	32	24	32	47	-24	70	24
2	32	25	-24	48	32	71	16
3	-24	26	16	49	-8	72	-16
4	8	27	8	50	-24	73	-24
5	-16	28	8	51	8	74	32
6	24	29	-24	52	-24	75	-24
7	-8	30	-16	53	8	76	32
8	8	31	0	54	32	77	-24
9	-16	32	-8	55	8	78	8
10	16	33	-16	56	-16	79	24
11	16	34	24	57	-16	80	16
12	16	35	-16	58	24	81	0
13	-24	36	-8	59	24	82	16
14	24	37	16	60	32	83	24
15	32	38	-16	61	-16	84	-8
16	8	39	24	62	0	85	-24
17	-8	40	8	63	32	86	0
18	16	41	0	64	-16	87	32
19	8	42	32	65	8	88	8
20	-8	43	16	66	-8	89	8
21	16	44	32	67	-16	90	16
22	8	45	-16	68	24	91	8
23	-16	46	-16	69	24	92	0

Table A.22.: Phase states of the TSC for the first frame of 8 PSK

ETU No	phase state	ETU No	phase state	ETU No	phase state	ETU No	phase state
1	32	24	4	47	-4	70	-24
2	32	25	16	48	-12	71	-28
3	-28	26	-8	49	16	72	8
4	8	27	-16	50	4	73	-28
5	-12	28	-16	51	-28	74	32
6	32	29	16	52	8	75	-28
7	0	30	28	53	-20	76	32
8	16	31	-20	54	4	77	-28
9	-8	32	-28	55	-16	78	4
10	28	33	32	56	28	79	24
11	32	34	8	57	32	80	16
12	-28	35	-28	58	8	81	0
13	-4	36	-16	59	12	82	20
14	-20	37	12	60	20	83	32
15	-12	38	-16	61	-24	84	4
16	28	39	28	62	-4	85	-12
17	16	40	16	63	32	86	12
18	-20	41	8	64	-16	87	-20
19	-24	42	-20	65	8	88	24
20	24	43	32	66	-8	89	28
21	-12	44	-12	67	-12	90	-24
22	-20	45	4	68	32	91	-28
23	20	46	4	69	-28	92	32

Table A.23.: Phase states of the TSC for the first frame of 16 PSK

A.4. Load Modulation from PICC to PCD

For the communication from PICC to PCD a new way of load modulation should be used. Instead of using the BPSK modulation defined in [17], 4 different symbols should be used for this communication direction.

A.4.1. Bit Representation and Coding for Bit Rates of fc/8, fc/4 and fc/2, fc

For data rates of fc/8, fc/4, fc/2 and fc the coding is based on symbols of the information content of 2 bits. This is referred as 4 PSK. The symbols are defined in time domain shown in Figure A.5.

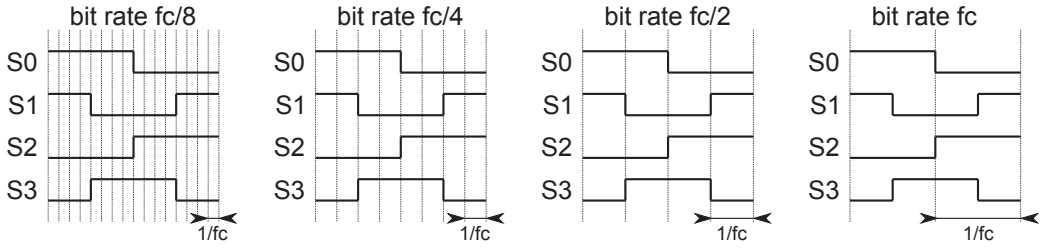


Figure A.5.: Symbols definition for 4 PSK

The symbols are defined as follows: - S0 uses load modulation in the duration of the first half ETU and no load modulation during the second half ETU.
- S1 uses no load modulation in the duration of the first half ETU and load modulation during the second half ETU.
- S2 uses no load modulation in the duration of the first quarter ETU, load modulation in the duration of the second and third quarter ETU, and no load modulation in the duration of the last quarter ETU.
- S3 uses load modulation in the duration of the first quarter bit, no load modulation in the duration of the second and third quarter bit, and load modulation in the duration of the last quarter ETU.
The information content of the symbols is given in Table A.24.

Information content	Symbols
00	S0
11	S1
10	S2
01	S3

Table A.24.: Information content for the 4 PSK

A.4.2. SOF Definition

For very high data rates, the standard frame contains a SOF field and an EOF. The SOF consists of 40 ETU, subdivided in the synchronization sequence (8 ETU) and the training sequence (32

ETU). The synchronization sequence has the content of HHLLHLHL, where state H represents load modulation during one ETU, and state L represents no load modulation during one ETU. The concept of the training sequence is a pseudo-random signal, the content is defined in Table A.25.

ETU No	Symbol	ETU No	Symbol	ETU No	Symbol	ETU No	Symbol
1	S0	9	S2	17	S3	25	S0
2	S2	10	S3	18	S2	26	S0
3	S1	11	S1	19	S0	27	S1
4	S2	12	S2	20	S2	28	S2
5	S1	13	S3	21	S0	29	S3
6	S3	14	S3	22	S3	30	S2
7	S3	15	S0	23	S0	31	S0
8	S1	16	S1	24	S1	32	S3

Table A.25.: Training sequence for PICC to PCD

The EOF is defined as no load modulation of 2 ETU.

B. Appendix Analog Parts

This Appendix contains the layout as well as the schematics of the user defined elements of the evaluation reader. That way the findings are replicable and the results can be proved.

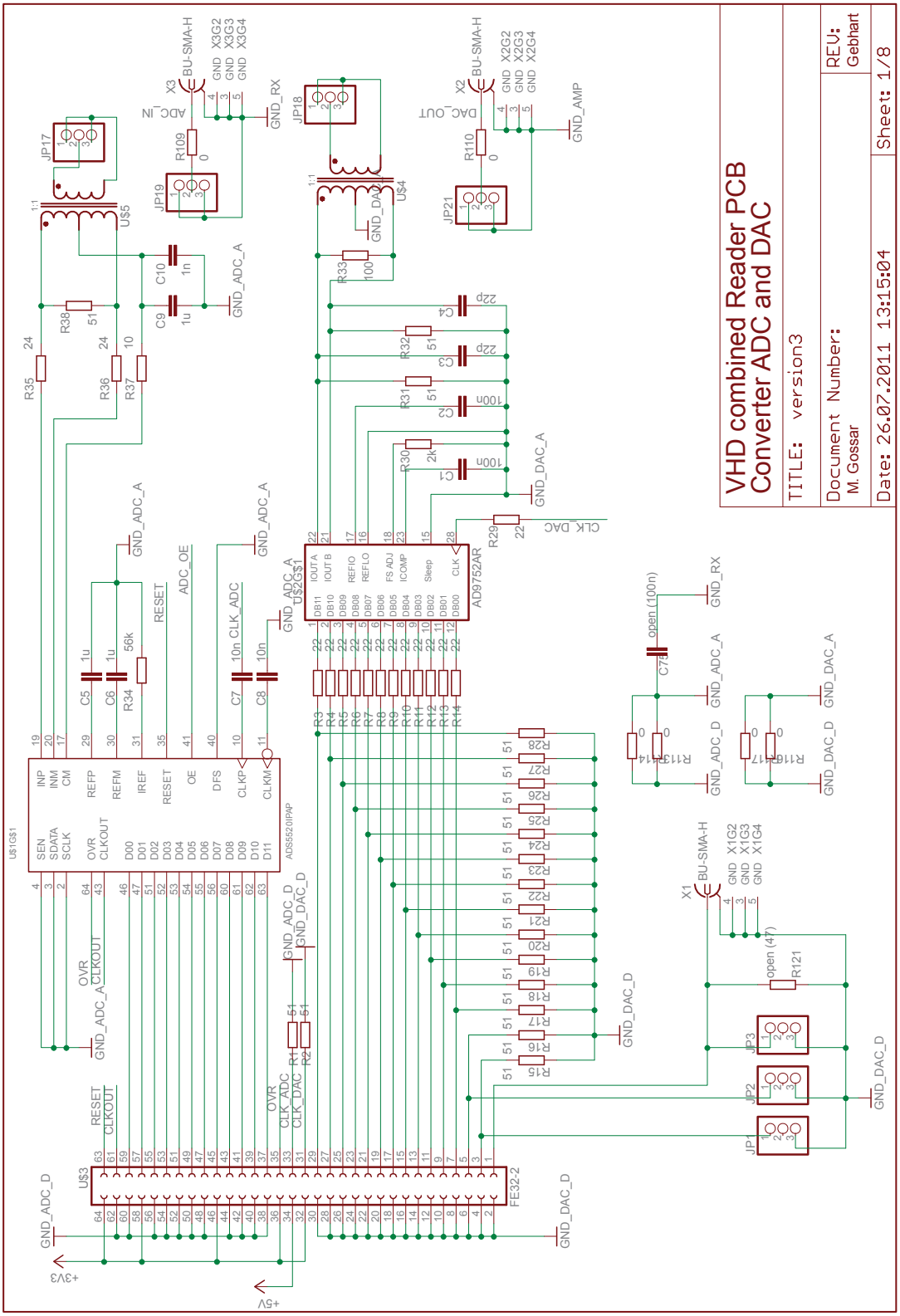


Figure B.1.: Converter

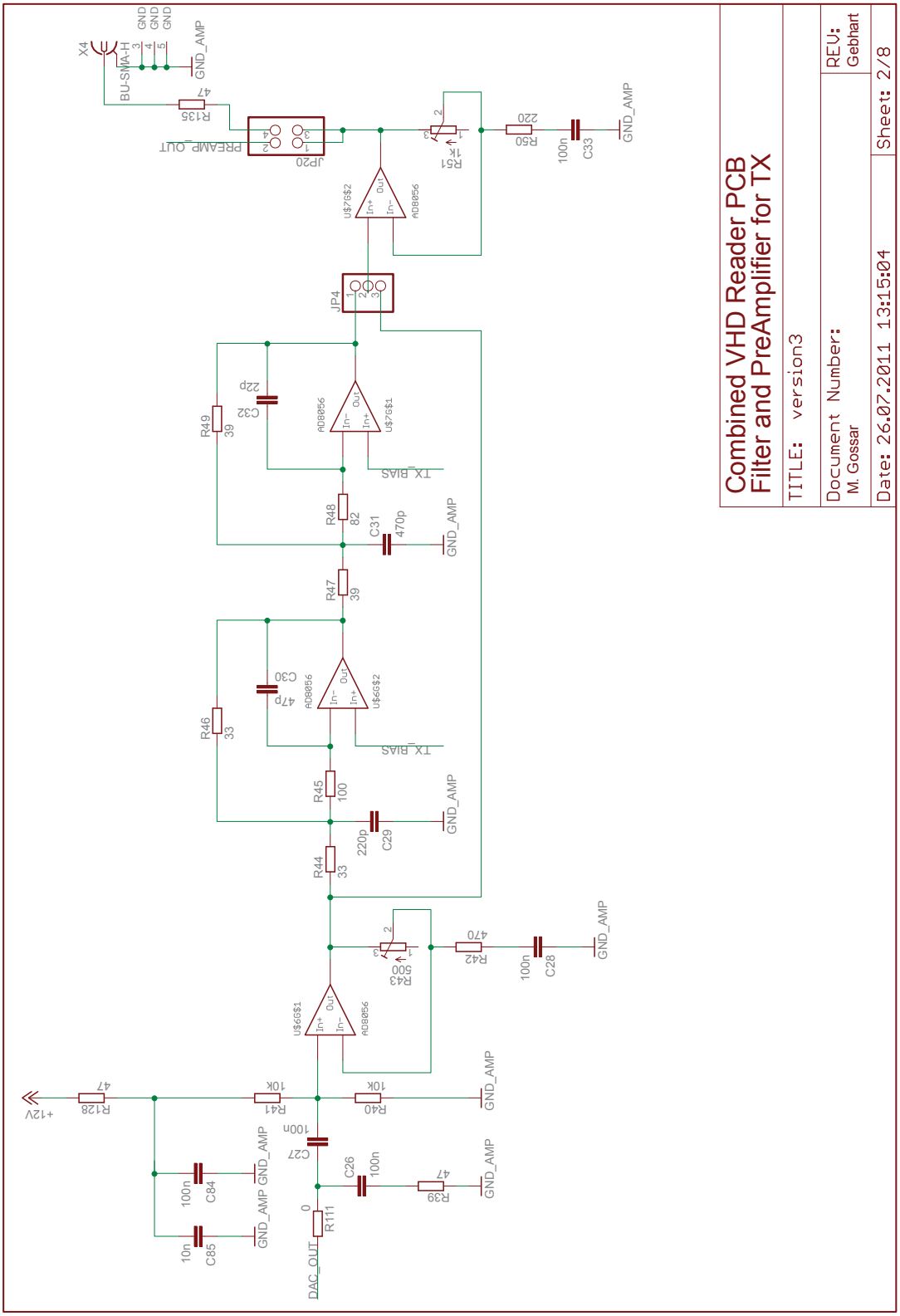


Figure B.2.: LPF and amplifier 12 V

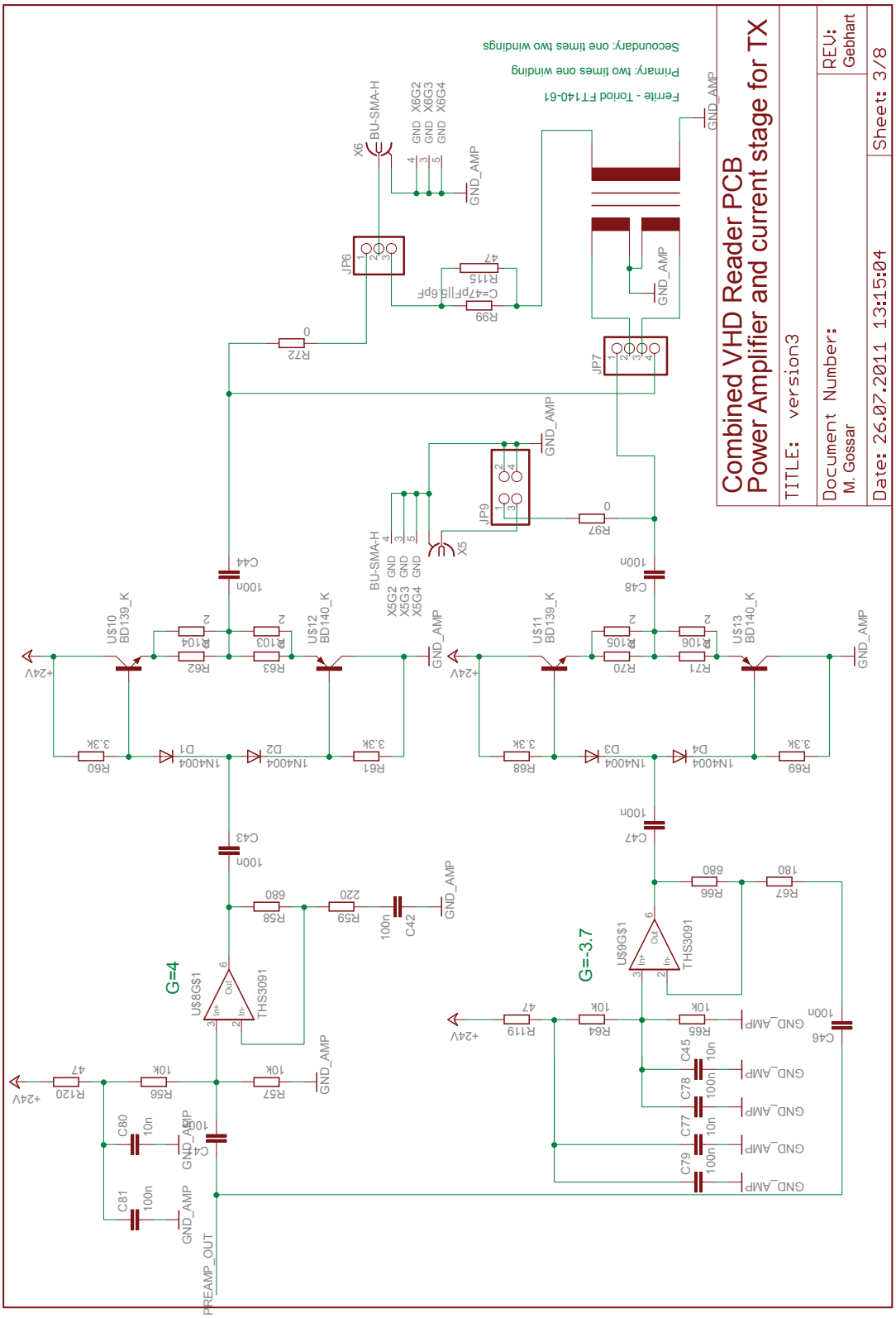


Figure B.3.: Power amplifier 24 V

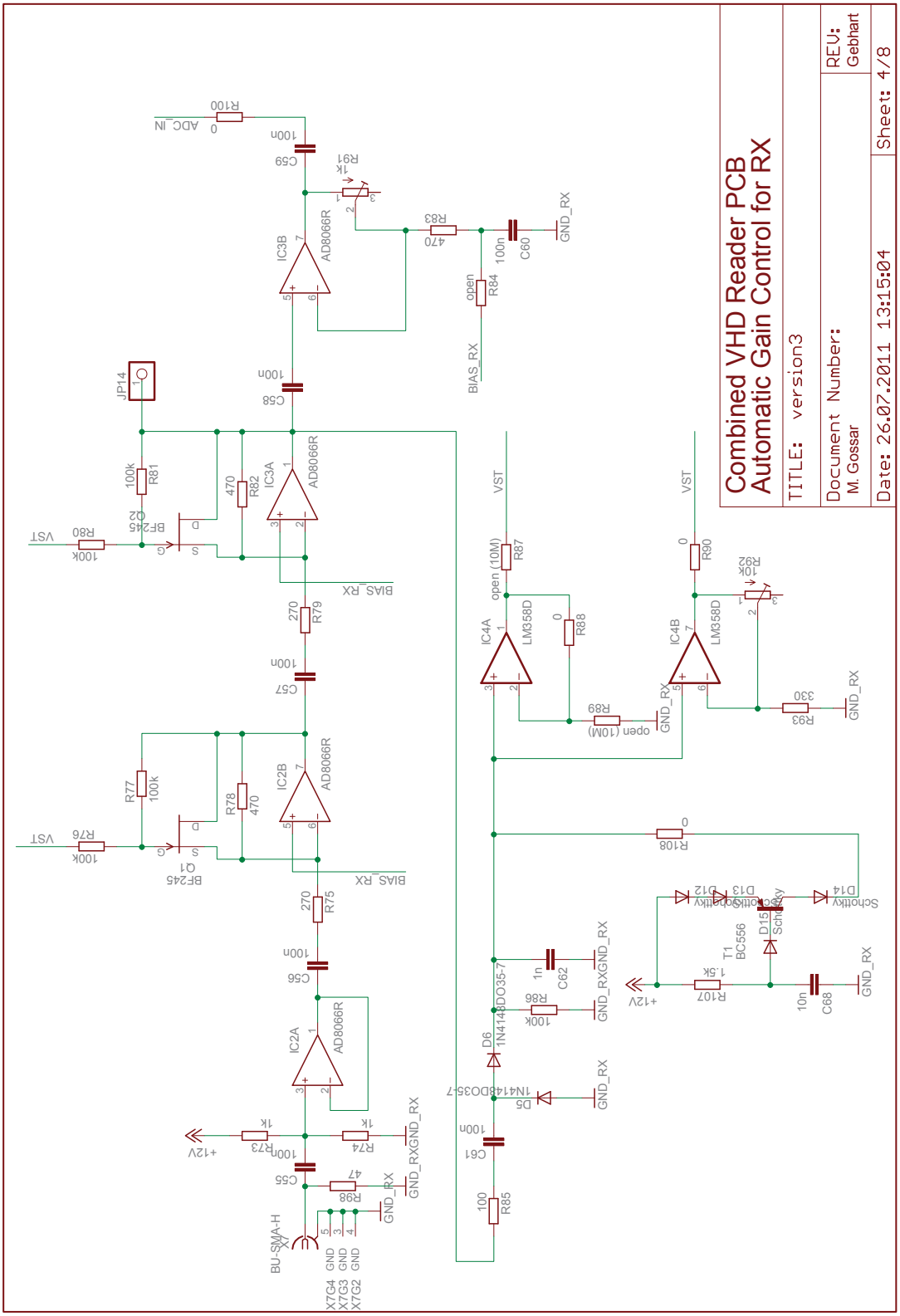


Figure B.4.: Automatic gain control circuit

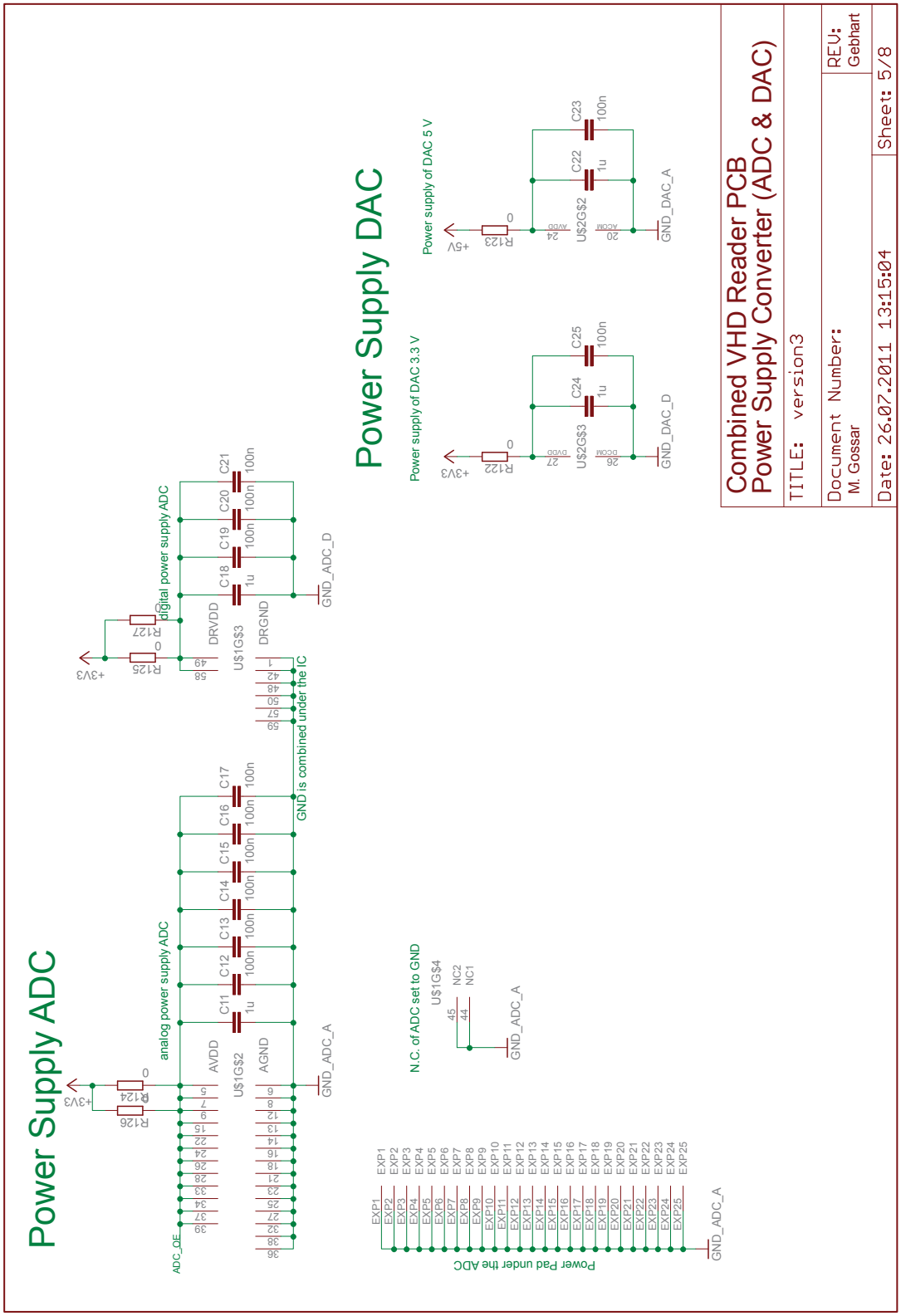


Figure B.5.: Power supply part 1

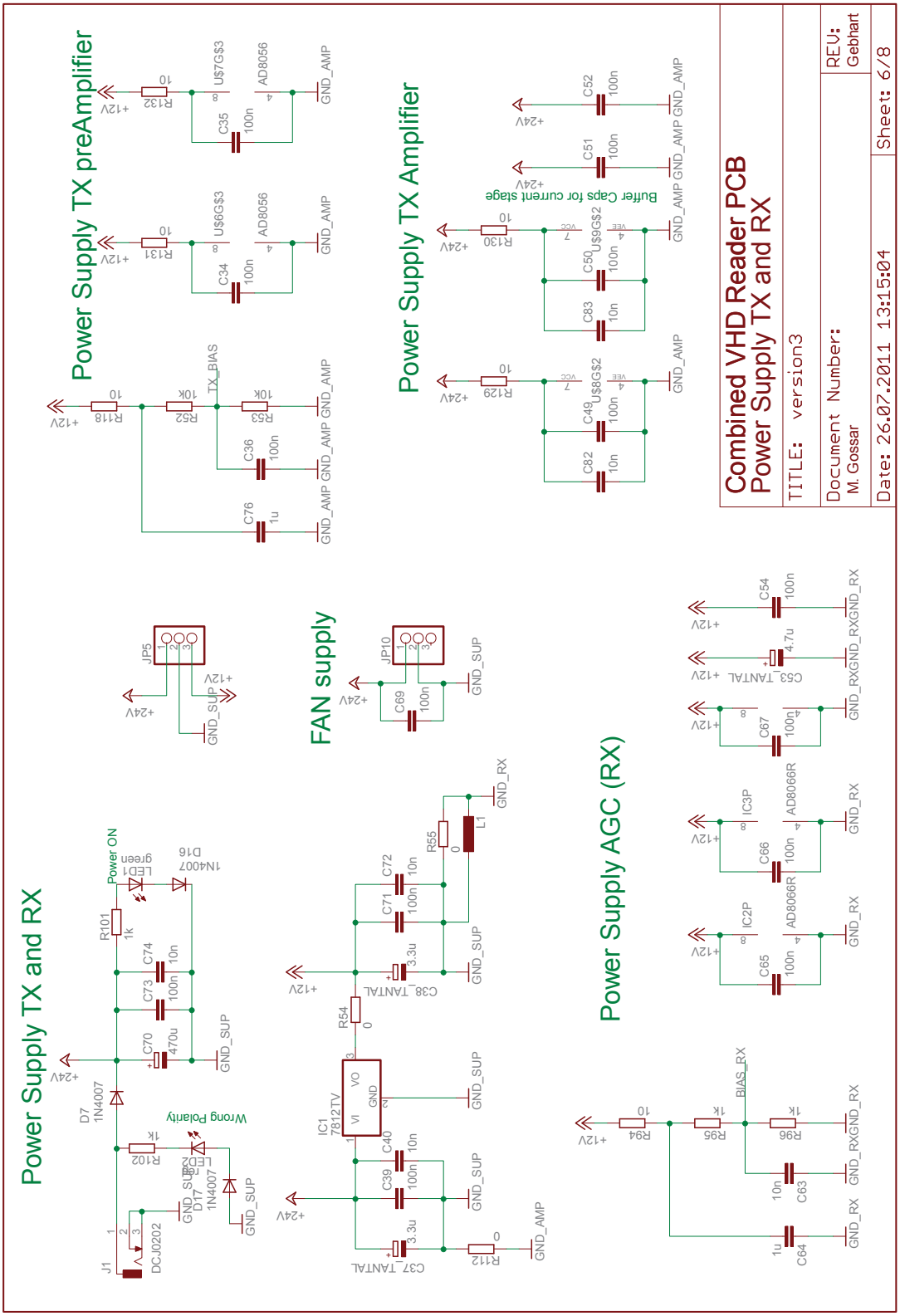


Figure B.6.: Power supply part 2

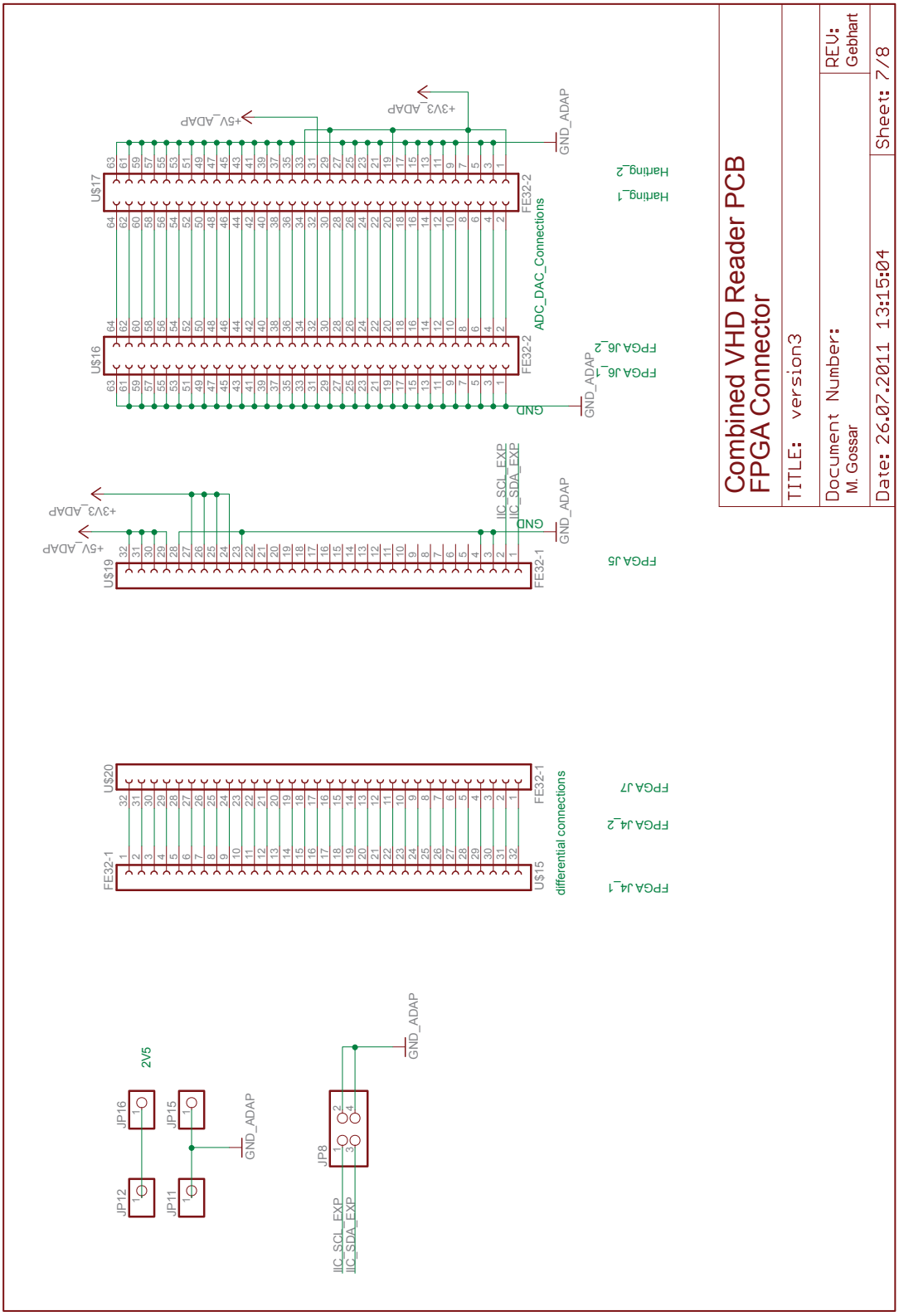


Figure B.7.: Adapter

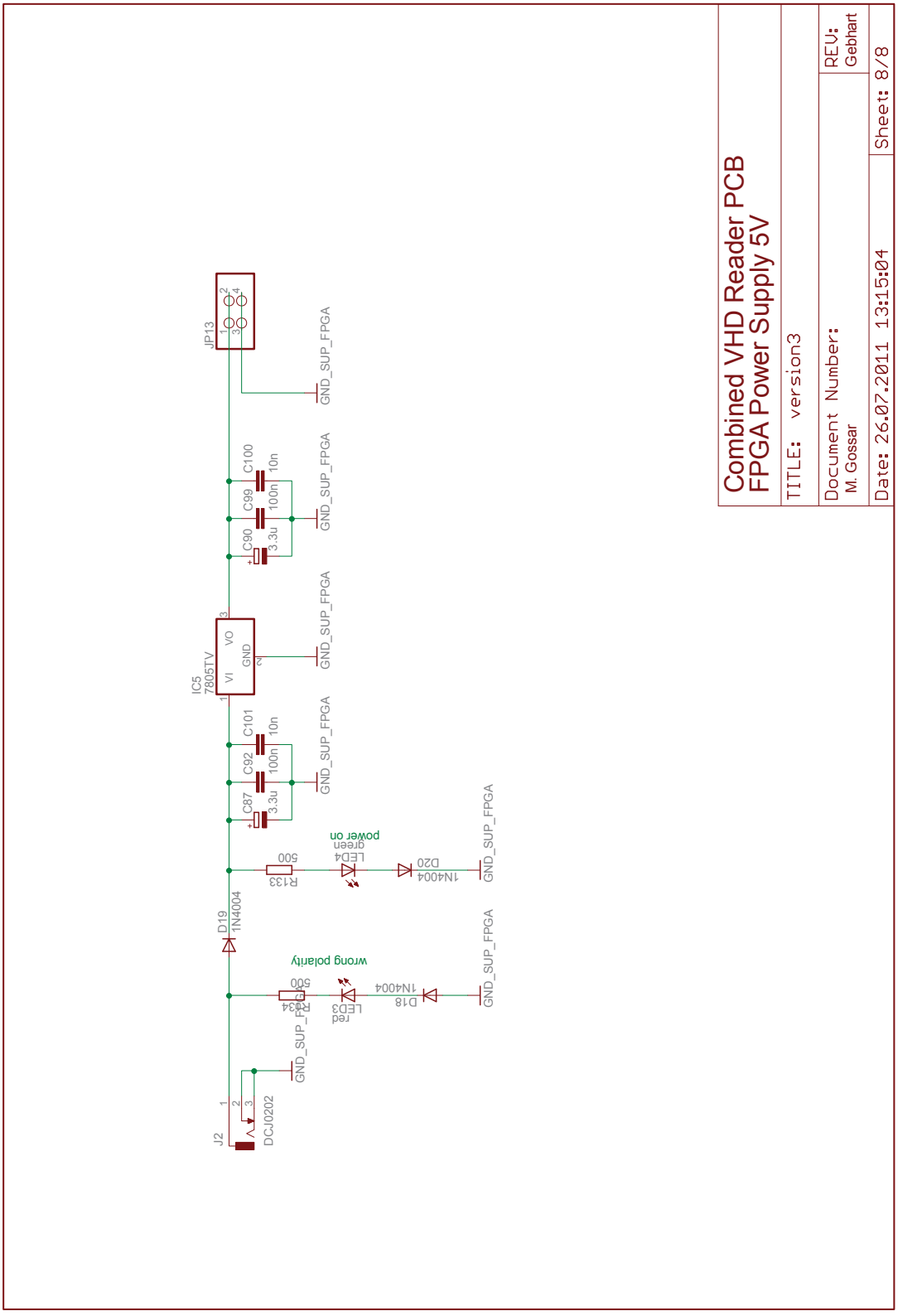
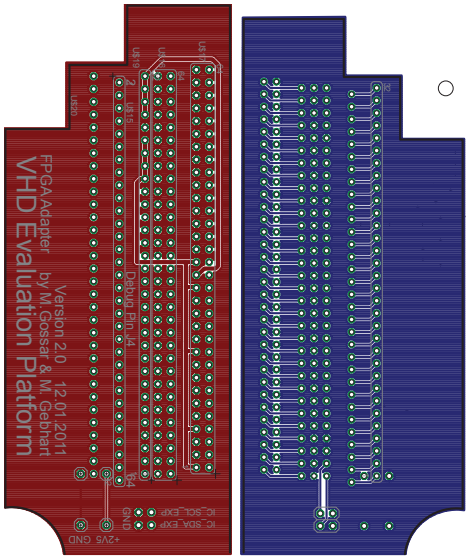
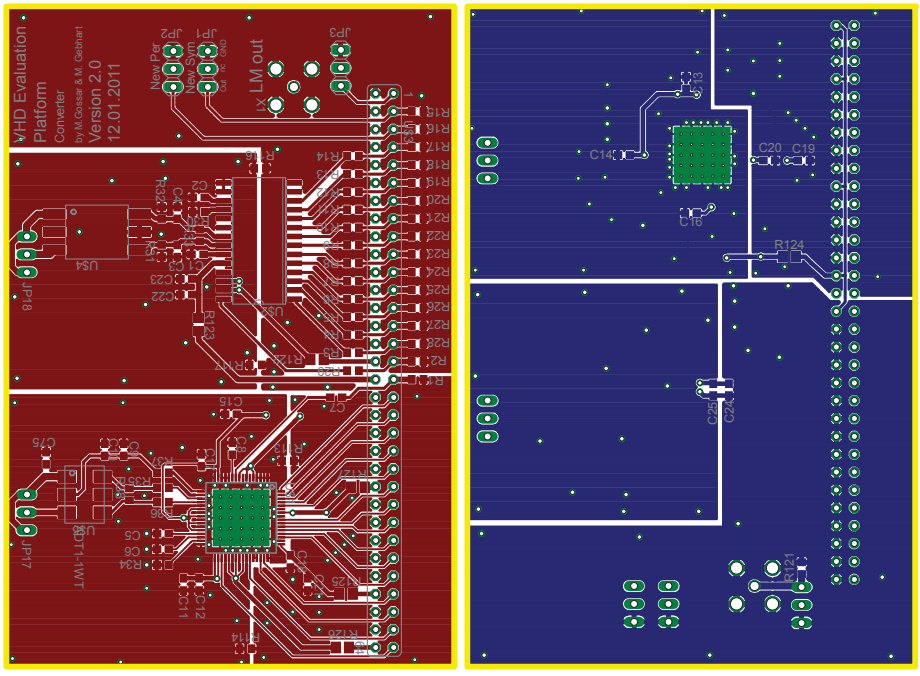


Figure B.8.: Power supply unit for the FPGA with voltage regulator



(a) Top (b) Bottom

Figure B.9.: Adapter layout



(a) Top (b) Bottom

Figure B.10.: Converter layout

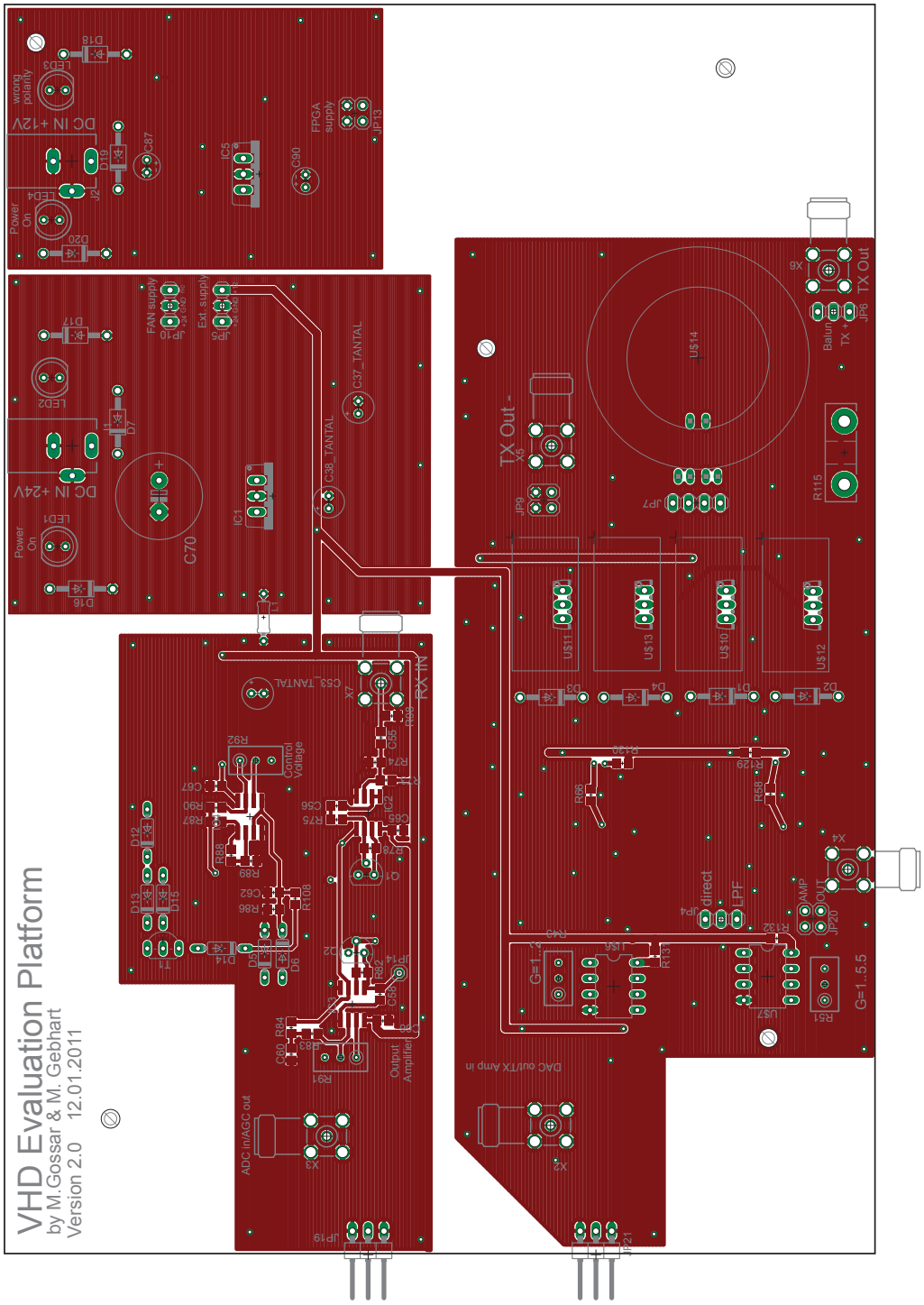


Figure B.11.: Analog PCB top layout

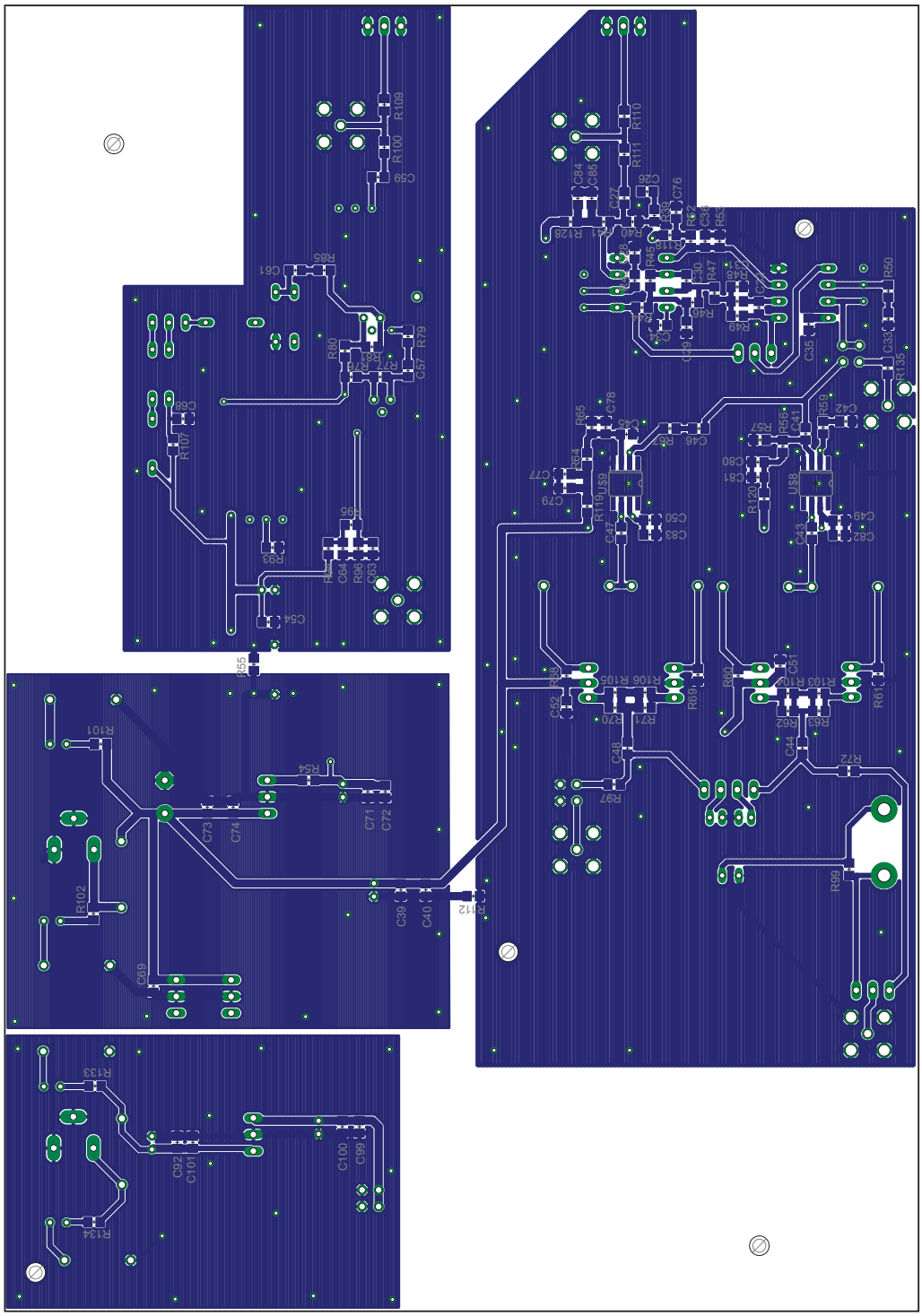


Figure B.12.: Analog PCB bottom layout