High Frequency Inductor Based DC-DC Buck Converter in 65 nm Low Power CMOS Technology

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Abstract

The goal of this thesis was to develop a high frequency inductor based DC-DC buck converter that can be used to replace linear voltage regulators in huge portable systems, like in chips for mobile phones. If DC-DC converters replaced most of the linear voltage regulators, the chips would achieve much higher overall power conversion efficiencies from the batteries to the loads. This would increase the active usage times of the devices and it would also reduce the re-charging cycles of the batteries.
In order to make the converter competitive to linear voltage regulators, three important constraints have to be fulfilled: First, the converter should be able to handle light loads down to some milliamperes with a high power conversion efficiency; second, only small passive components should be used for the input and output filter of the converter and third, the occupied chip area of the converter design should be in the range of a linear voltage regulator.
The outcome of this thesis is a completely new developed high frequency inductor based DC-DC buck converter where several innovative concepts were used:

1. Stacked transistors are used instead of drain extended transistors for the power switches;

2. Robust high speed voltage level shifters with short propagation delays were developed for controlling the switching time instants of the power switches;

3. A very fast low power body diode conduction sensor which is able to measure body diode conduction durations down to some hundred picoseconds was developed;

4. An automatic and robust dead time optimization concept for optimizing the switching time instants of the power switches during normal converter operation was developed.

A test chip of the design was fabricated in a 65 nm low power CMOS technology and the performance of the design was verified in the laboratory.

Kurzfassung

Ziel der Dissertation war es einen hochfrequenten DC-DC Buck Konverter mit LC Ausgangsfilter zu entwickeln, welcher dann in großen integrierten Systemen für tragbare Anwendungen wie beispielsweise in Mobiltelefonen als linearer Spannungsregler-Ersatz zum Einsatz kommen soll. Wenn es möglich wäre die meisten linearen Spannungsregler durch DC-DC Konverter zu ersetzen, dann könnten viel höhere Systemwirkungsgrade erreicht werden. Somit würde die Energie im Akku der Geräte länger ausreichen und die Zeitspannen der Ladezyklen würden erhöht werden.
Um Vorteile gegenüber dem Einsatz von linearen Spannungsreglern zu haben soll der Konverter folgende drei Eigenschaften aufweisen: Erstens, der Konverter soll auch bei niedrigen Laststrombereichen von einigen milli-Ampere einen hohen Konverterwirkungsgrad erreichen, zweitens, es dürfen nur kleine passive Bauteile für das passive Eingangs- und Ausgangsfilter des Konverters verwendet werden und drittens, die verbrauchte Chip Fläche soll im Bereich von linearen Spannungsregler liegen.
Das Ergebnis dieser Dissertation ist ein komplett neu entwickelter Hochfrequenz DC-DC Buck Konverter mit LC Ausgangsfilter bei dem viele innovative Konzepte eingesetzt wurden:

1. Die Konverterausgangsstufe wurde anstatt mit üblichen Hochvolttransitoren mit “gestackten” Transistoren aufgebaut.

2. Es wurden robuste und sehr schnelle Pegelwandler mit kurzen Verzögerungszeiten für die genaue Steuerung der Schaltzeitpunkte der Ausgangstransistoren entwickelt.

3. Ein schneller “body diode conduction” Detektor zum Messen der Stromflussdauer durch die parasitäre “body diode” der Ausgangstransistoren wurde entwickelt. Der Detektor erkennt bereits Stromflusszeiten von einigen hundert Pikosekunden.

4. Ein automatisches und robustes Konzept zur Totzeitoptimierung der Leistungstransitoren in der Ausgangsstufe, welches auch während des normalen Konverterbetriebes funktioniert, wurde eintwickelt.

Es wurde ein Testchip in einer 65 nm low power CMOS Technologie hergestellt und dann im Labor vermessen.

Acknowledgment

I would like to thank Dr. Florian Michl, the head of the DES IP AMS department at Infineon Technologies Austria AG in Villach, and all the colleagues in the “Power Management Systems” team who have helped me in the realization of my dissertation.
I would especially like to thank Christoph Sandner, who was my adviser and mentor at Infineon. Christoph Sandner gave me a lot of freedom during my PhD work and he pushed me a lot to try new concepts and ideas. He supported me in the scientific field but he was also a mentor on the human side. Furthermore, he was the initiator of the collaboration between Infineon and the Graz University of Technology which enabled me to do my dissertation at Infineon in Villach.
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1 List of Abbreviations

AC	Alternating current
ADC	Analogue to digital converter
BDCS	Body diode conduction sensor
CMOS	Complementary metal oxide semiconductor
DAC	Digital to analogue converter
DC	Direct current
DCR	Direct current resistance
DVS	Dynamic voltage scaling
DeMOS	Drain extended MOS
DPWM	Digital pulse width modulator
DSP	Digital signal processing
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ESL	Equivalent series inductance
ESR	Equivalent series resistance
FET	Field-effect transistor
FSL	Fast switching limit
FSM	Finite state machine
IB DC-DC	Inductor based DC-DC converter
IC	Integrated circuit
IO	Input-output
IU	Upper peak current threshold
LCO	Limit cycle oscillation
LDO	Low dropout linear voltage regulator
LSB	Least significant bit
LVSH	High-side level shifter
LVSL	Low-side level shifter
Mbps	Megabit per second
MOS	Metal oxide semiconductor
MP3	MPEG-1 Audio Layer 3
NMOS	N-channel MOS transistor
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PFM	Pulse frequency modulation
PI	Proportional-integral

PMOS	P-channel MOS transistor
PMU	Power management unit
PSiP	Power system-in-package
PSoC	Power system-on-chip
PVT	Process, voltage and temperature
PWM	Pulse width modulation
PWM-CCM	Pulse width modulation - continuous conduction mode
PWM-DCM	Pulse width modulation - discontinuous conduction mode
RF	Radio frequency
RMS	Root Mean Square
SC DC-DC	Switched capacitor DC-DC converter
Si	Silicon
SiP	System-in-package
SMPS	Switched mode power supply
SoC	System-on-chip
SRAM	Static random-access memory
SSL	Slow switching limit
VDD	Common drain voltage (positive supply voltage)
VLSI	Very large scale integration
VSS	Common source voltage (negative supply voltage)
ZCS	Zero current switching
ZVS	Zero voltage switching

2 Introduction

The first chapter of this thesis gives a brief overview of the topics that are handled in this work. Furthermore it gives an impression of the problems and challenges in the research area “energy management” which is one of the most miscellaneous and challenging topics in modern chip design.

2.1 Motivation

It can be seen from new products that electronic systems have to provide more and more functionality and that their complexity increases continuously. Especially the electronic market for mobile phones can be seen as a prime example which shows this trend very well: Fig. 1 illustrates the increase of the overall system performance of mobile phones over time. Today, some vendors already sell products that fulfil the IMT-Advanced (International Mobile Telecommunications Advanced) requirements. This is the so-called “fourth generation standard” (4G) for mobile telecommunication. For instance, the broadband wireless standard defines data rates of 100Mbps downlink speed and 50Mbps uplink speed. This allows features like real time television, fast music and video downloads but it also gives the opportunity for fast data exchange with other peripheral devices like digital cameras, MP3 players and desktop computers.
Beside the provided technical features one of the most important selling points of portable devices is their “energy management” performance. Information concerning the “talk-time” and the “standby-time” is typically printed directly on the offers of the devices. So customers can directly compare these values with values from other vendors. Of course, the wish from customer’s side is clear: Customers would like to have both, extended active usage times of the devices without recharging the battery but also more and more implemented features. Since the implemented features are typically power hungry the gap between the overall system performance of the devices and battery performance will increase (see Fig. 1).
In order to overcome the challenge with the limited power budget in mobile devices new solutions have to be found. Two different research fields deal with this topic: The first one is called “energy management” and the second one is called “power management”. Often, both notations are used in the same context since both fields have to deal with similar overall problems and challenges. But it has to be mentioned that each field concentrates on a different

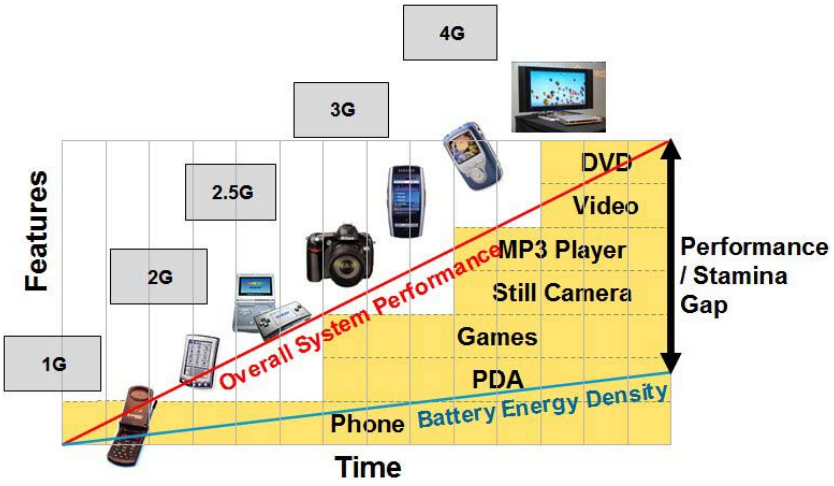


Figure 1: Increasing functionality in mobile phones [11]

focus:

The goal of energy management is to extend the active usage time of the devices from system's point of view. A well known example which is often used for digital circuits is dynamic voltage scaling for reducing the power consumption and adaptive body biasing for reducing leakage power [39]. Only the system knows when digital circuits or processors need performance and when they can switch to a low performance mode with low power consumption.

Another example is to switch off all blocks that are currently not needed for a certain operation. If a block is required, it is switched on again, which means that all the blocks are only in active mode if their functionality is required. Again, only the system knows if blocks have to operate or if they can be switched to an inactive low power mode.

In contradiction to energy management, power management has the goal to extend the active usage time of the mobile devices from one battery recharge cycle to the next from block level point of view. It includes selection of the type of the voltage converter, for instance the usage of switched mode power supplies instead of linear voltage regulators that typically gives an improvement in power conversion efficiency and it also includes the usage of low power design techniques and block level optimization.

Finally it has to be mentioned that if switched mode power supplies in a system are almost never active, linear voltage regulators might be the better option in terms of energy management, since they typically can be designed with much lower quiescent current. Therefore, a better power management performance does not automatically result in a better energy management

performance.

2.2 Energy management in mobile phones nowadays

Typical building blocks in mobile phones are the micro controller with integrated SRAM, the RF receiver and transmitter, signal processing units for the baseband, audio processing, back light drivers for the display and SIM card interfaces [26], [12]. Since such systems are extremely complex, well-elaborated system level power distribution concepts from the power sources to the system loads are one key to success.
The power management unit (PMU) controls the power distribution from battery to the different building blocks (loads). Fig. 2 shows an example of a possible power distribution concept in a portable device: On the left side there is the battery that provides the energy for the system operation and on the other side there is the system with the different loads. The loads are the power consumers that can be on chip but also outside of the chip. So in general, the PMU consists of several different voltage converters and a controller that controls the different voltage converters in order to control the energy flow from the battery to the loads.
Often, different power domains with different voltage levels are defined. This allows separating the power supply concept for different building blocks which make the designs more robust – but it can also help to reduce power consumption of the blocks since each block can be supplied with the optimum supply voltage (also dynamic voltage scaling can be used [39]).
Let's now have a brief look at the different blocks in Fig. 2, which are responsible for the overall system power conversion performance.

2.2.1 Batteries

The batteries provide the power for the system. Nowadays, typically lithium-ion (Li-Ion) batteries are used which have high capacity per weight, low leakage and almost no memory effects [55]. Although there is a continuous improvement every year, the battery performance is doubling only every ten years [7]. In comparison to batteries, the device level performance of microprocessors doubles every 18 months which further increases the gap between the "Overall System Performance" and the "Battery Energy Density" [11], [7] like it already has been depicted in Fig. 1.
Additional circuitry for battery protection is required in order to guarantee

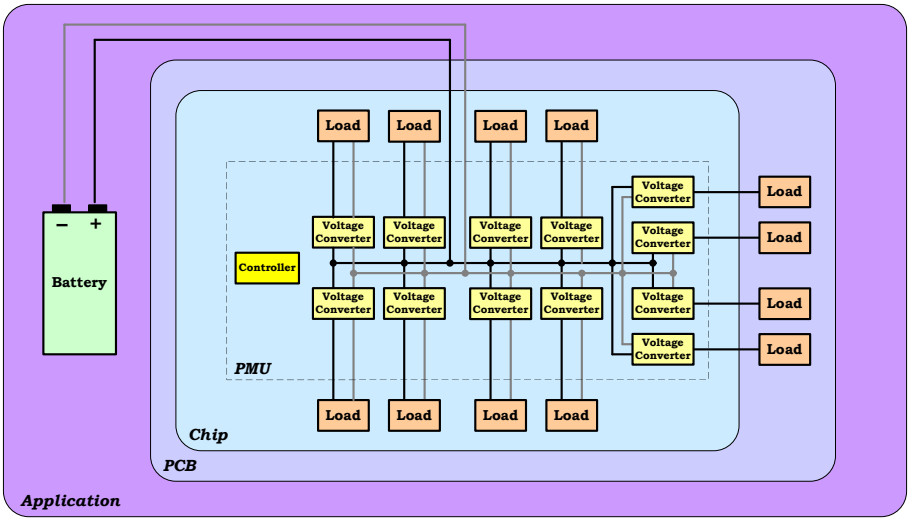


Figure 2: Power management in large systems. The main contributors are the battery, the power traces, the power management unit (PMU) with the voltage converter, and of course the different loads.

safe operation during charge and discharge phase. Typically, the protection circuit is placed into the battery pack [51]. Monitored parameters used in the protection circuits are [21]: battery voltage[1], current flow[2] and battery temperature [3].

2.2.2 Loads

Typical power consumers (loads) in cellular phones are displays, DSP, card interfaces, the power amplifier, the RF part and the keyboard driver [44]. Typically, the loads are connected to different power supply domains since they often have completely different requirements on the supply voltage. The PMU have to be designed to fulfil these requirements of the loads in order to guarantee safe operation[4].

[1]This allows preventing over-charging (over voltage detection) and over-discharging (under voltage detection), which reduces cycle life. Moreover, over-charging can overheat the battery, which can destroy the battery [51].

[2]This allows protecting the battery for overload and short circuit scenarios.

[3]The typical temperature range suitable for charging Li-Ion batteries is 0 °C to 45 °C. Charging outside of these limits can cause a mechanical breakdown or even an explosion of the battery [63].

[4]Required start-up times, highest possible load current, largest output voltage ripple, load regulation, line regulation, noise and so on.

2.2.3 Power Traces

Power traces are the connections between the battery, the PMU and the loads. The traces[5] have to be dimensioned strong enough in order to be able to carry the current without overheating. Furthermore, layout of the power traces has to be done very carefully in order to avoid large cross coupling effects and EMI problems [43]; but well done power routing also increases the system reliability and the power conversion efficiency of the PMU[6] [14].

2.2.4 Used chip technology

There is the clear trend to implement more and more functionality in the digital domain. Therefore, low power digital block design plays an important role. The energy consumption of a digital block is generally given by

$$E_{avg} = \int \left(\alpha_{0\to1} \cdot C_L \cdot V_{dd}^2 \cdot f_{clk} + I_{sc} \cdot V_{dd} + I_{leakage} \cdot V_{dd}\right) dt \quad . \qquad (1)$$

Eq. 1 is composed of three main terms: the first term describes the dynamic energy consumption due to switching events, the second part is the energy consumption due to short circuits during switching and the last part describes the energy consumption due to transistor leakage. Eq. 1 shows again that all terms are related to the supply voltage V_{dd}, so one effective way to reduce energy consumption in digital circuits is simply to lower the supply voltage [39]. Since the newest technology nodes are typically supplied with lower supply voltages than older nodes, the usage of the newest technology in a design reduces the energy consumption of digital circuits effectively.
For analogue circuits the usage of the newest technologies does not necessarily give a better energy performance – power dissipation tends to become worse for analogue circuits in deep sub-micron [3]. In [1] it is shown that the power consumption of an implemented CMOS voltage follower (with optimum biasing and dimensioning for a given specification) decreases down to about 0.35 um – 0.25 um technologies and starts to increase again for smaller technologies.
A possible way to optimize both, the energy performance of both digital parts and the analogue parts is to use a System-in-Package (SiP) approach. There the digital circuits can be implemented in the newest low power deep submicron technology and “older” processes can be used for the analogue blocks.

[5] It includes the power traces on the PCB, the bonding wires, the on-chip power routing.
[6] Low parasitic inductances limit IR-drops and high frequency ringing on the power traces.

Finally, both chips are put together into one chip package and are interconnected with each other. The trade-offs between a single chip solution (also called SoC System-on-Chip) and SiP are discussed in [27], [31].
Since mobile handsets typically are most of the time in standby mode, leakage power consumption is another very important constraint. Although the supply voltage decreases with newer technologies, power consumption due to leakage currents increases. In [25] it is shown, that static power dissipation can be even higher than dynamic power dissipation for deep sub-micron technologies.

2.2.5 PMU

The PMU has to control the energy flow from the power source (battery) to the different power consumers (loads). It consists of voltage converters for supplying the different loads and a controller, which controls the power status of the voltage converters. For instance if a certain load is disabled, the voltage converter can be switched to power down mode. The voltage converter is switched on again if the load restarts. Modern PMUs support several different power modes[7].

2.2.6 Voltage converters

Voltage converters generate stable output voltages with semi-static values[8] from the high and unstable battery voltage, which are used for the different loads as supply voltage. The voltage converters should fulfil the following requirements: 1) high power conversion efficiencies under all load conditions; 2) protection features like under voltage lock out, over voltage protection, soft start and so on; 3) smart features like multi-mode operation with automatic handover, fully configurable output voltages, regulation loops and so on; and 4) they should be cheap, should have a low pin count and should not need a lot of external passive devices or even any external passive devices.
Three different voltage converter types are typically used in PMUs:

1. Linear voltage regulators
2. Switched capacitor DC-DC converters (SC DC-DCs)

[7] Some commonly used modes: active mode, idle mode, sleep mode, standby mode, power down mode,...

[8] Often the output voltages are programmable – so it can also be changed during operation e. g. in order to provide adaptive voltage scaling.

3. Inductor based DC-DC converters (IB DC-DCs)

Each of them has advantages and disadvantages, so it is not possible to say that a certain type is the best one for all applications. In principle, the different types can be separated into two classes: First, the class of linear voltage regulators and second, the class of switched mode power supplies (SMPS).
Typically, linear voltage regulators achieve worse power conversion efficiencies than SMPS. Of course this is not necessarily true e. g. if the regulated output voltage is close to the input voltage of the regulator, or if the provided output power is very low, but in most of the cases it is valid. On the other hand SMPS are more expensive, since more passive components are required and typically they are more complicated to design.
Nowadays most the of "voltage converters" in Fig. 2 are realized by means of linear voltage regulators. Linear voltage regulators can be designed very compact and typically they only need one external buffer capacitor – so they are also cheap. Therefore, linear voltage regulators are often the preferred solution, especially if the supplied loads are inactive most of the time and if the power consumption of the loads is below some hundred milliwatts. In this case the worse power conversion efficiencies of linear voltage regulators are often tolerated.
But with the development of monolithic passives with large values and high quality factors in the recent years new opportunities appear for PMU designers: Now it becomes possible to integrate complete PMUs fully on chip (monolithic approach) or at least in one chip package (SiP approach). This allows exchanging more and more linear voltage regulators with SMPS. For SC DC-DC this was already possible in the past since they only require large capacitors for their operation. For IB DC-DC converters the perspective was worse since it is/was extremely challenging to design on-chip inductors with large inductance value and high quality factor with today's technologies.
But the clear vision for the future is to replace all the linear voltage regulators by high efficient SMPS, which strongly increases the power conversion efficiency of large integrated systems and which can close the gap between the overall system performance and battery performance as it was depicted in Fig. 1 on page 2.

2.3 Scope of this work and contributions

The scope of this work was to develop an integrated, area optimized high efficient inductor based DC-DC converter that can be used as linear voltage regulator replacement in large integrated systems. Beside switched capacitor DC-DC converters the designed converter should be used to improve the overall power conversion performance of the PMUs which should allow to continue increasing the complexity of the chips and to implement additional features without lowering the active usage times of the devices.
The outcome of this work is an inductor based DC-DC converter test chip that comprises several new circuit concepts and topologies. Detailed information about the implemented converter can be found in section 5 on page 65 with the title “IB DC-DC converter for portable applications”. A summary of the own publications is listed in section 8 on page 109 “Own Publications”.
Furthermore, several invention disclosures have been submitted to the patent department during this work. The invention disclosures not only deal with IB DC-DC converters but also with other topics like SC DC-DCs. A list of the own invention disclosures can be found in chapter 9 on page 111 “Invention Disclosures”.

2.4 Thesis overview

The thesis is organized as follows:
Chapter 3 gives an overview of the three voltage converter types mainly used in PMUs in modern chip designs. Discussed are the basic operating principles of the converters and the important performance parameters and limitations.
Chapter 4 gives then a more detailed overview of the major building blocks of IB DC-DC buck converters. Special focus will be on the discussion of the main loss contributors that are relevant for the power conversion efficiency of the converter. Furthermore, different controller strategies are explained and a small signal model of the used peak current controller topology is developed in this chapter.
Chapter 5 then shows detailed information about the implemented IB DC-DC buck converter. The chapter starts with the explanation of the top-level structure of the whole converter. Afterwards, the most important building blocks are discussed on the circuit level.
Chapter 6 shows measurement results of both fabricated test chips. In the first test chip a new developed body diode conduction sensor for optimizing

switching time instants of the power switches was placed beside an existing converter output stage. The test chip has shown that the new sensor is functional and that it can be used for integrated power stages to measure if body diode conduction will occur or not.
The second test chip contains the complete IB DC-DC buck converter design that has been completely newly designed during this work. Shown are the most important measurement results, e. g. the achieved power conversion efficiencies for different operating modes and the performance of the automatic dead time optimization algorithm. At the end of this chapter a performance summary of the second test chip is given.
Finally chapter 7 will give a summary of the work and a short outlook.

3 Voltage converters

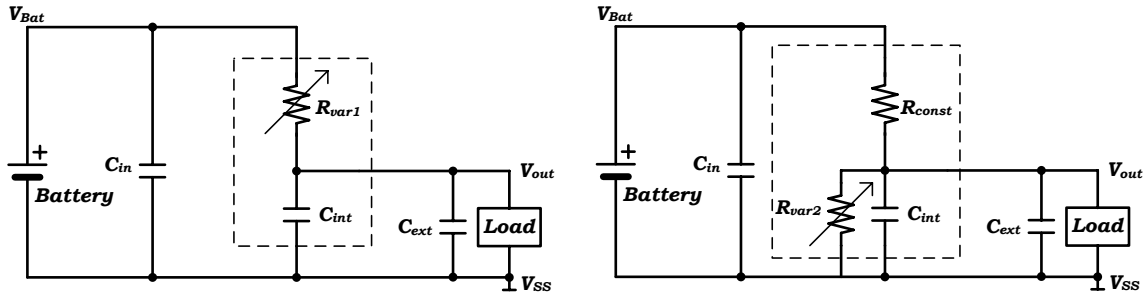
This chapter gives a rough overview about the three different voltage converter types used in PMUs. In modern PMUs all three types are used in parallel.
In principle the different voltage converter types can be classified into two groups: The first group are the linear voltage regulators. With linear voltage regulators, only voltage-to-voltage down conversion is possible. A special class of linear voltage regulators is low drop out regulators (LDOs). These are regulators that allow having the regulated output voltage close to the input voltage.
The second class of voltage converters in PMUs is the switched mode power supplies (SMPS). With SMPS both voltage-to-voltage down[9] and voltage-to-voltage up[10] conversion are possible. In SMPS the energy is transferred step by step from the input node to the output node that typically allows converting voltages with much higher power conversion efficiency.
Both linear voltage regulators and SMPS have advantages and disadvantages that will be discussed in this section.

3.1 Linear Voltage Regulators

Linear voltage regulators are used to adapt the supply voltages for the loads. Some reasons can be keeping the node voltages of transistors within the safe operating area; increasing the efficiency of a digital system due to the lower supply voltage; or isolating noise between the supply voltages [23].
Fig. 3 shows the two different linear voltage regulator types: The first type is called “series regulator” and is depicted in Fig. 3a. The idea is to regulate the output voltage V_{out} by adjusting the series resistance R_{var1}. R_{var1} is implemented as a transistor. This transistor is often denoted as “pass device” or “pass transistor” and can either be a PMOS or an NMOS device in CMOS technology.
The highest possible power conversion efficiency of a series regulator is given by the input and output voltage ratio:

$$\eta_{series\_max} = \frac{V_{out}}{V_{Bat}} \quad . \tag{2}$$

[9] also called step down converter or buck converter
[10] also called step up converter or boost converter



(a) Series regulator (b) Shunt regulator

Figure 3: Principle schematic and function of a linear voltage regulator

Fig. 3b shows a so-called "shunt regulator". There, a controlled resistance R_{var2} is connected in parallel to the load. The idea is that R_{var2} takes over the energy if the load does not need it. R_{var2} can be implemented with PMOS or NMOS devices, but also other devices like Zener diodes can be used. Advantage of a shunt regulator is that it provides a constant current flow from the battery additionally to the constant output voltage V_{out}. But a big disadvantage of this regulator type is that it typically has a very bad power conversion efficiency that is given by:

$$\eta_{shunt\_max} = \frac{V_{out}}{V_{Bat}} \frac{I_{out}}{I_{Bat}} \quad . \tag{3}$$

Only under very special conditions (for instance for regulators for ultra light loads) it could be beneficial to use a shunt regulator instead of a series regulator. But for most of the designs, series regulators are better due to the better power conversion performance.

3.1.1 Important performance parameters of linear voltage regulators

In the next section important performance parameters of linear voltage regulators will be briefly discussed. This topology will be considered since only series regulators are used most of the time.

Output voltage headroom

The output voltage headroom specifies the allowed output voltage range of the converter where it fulfils the given specification. If the specified output voltage of the regulator is always much lower than the applied supply voltage, then the regulator works as a "classical" linear voltage regulator. In this

case, either NMOS or PMOS transistors can be used for the pass device. If the specified output voltage of the regulator can be close to the applied input voltage, the regulator is called low drop-out regulator (LDO). If NMOS devices are used as pass device, the gate voltage of the pass device has to be pulled above the applied supply voltage. A second supply voltage [23] or also an internal charge pump [5], [6] can generate the gate driver voltage for the pass device. Subsequently, charge pumps in LDOs can cause noise on the regulated output voltage and can also cause EMC issues [61].

Load regulation

Load regulation is one of the most important parameters for linear voltage regulators. It is given in percentage and specifies the amount of voltage drop on the regulator output during a specified load jump. Since there is the trend to reduce the capacitance values of the blocking capacitors C_{int} and C_{ext} or rather to remove C_{ext} completely[11] the regulation loop of the regulator has to become very fast. Fast regulation loops are easier to design if NMOS devices are used for the pass device instead of PMOS transistors, since NMOS devices have inherently low output impedance due to the source follower structure [19]. Linear voltage regulators with PMOS pass device tend to be slower since the dominant pole is at quite low frequencies and therefore the regulation loop has lower bandwidth [6].

Area consumption

Area consumption should always be as small as possible since it is directly related to costs. If only the electrical performance of the transistors is considered, then linear voltage regulators with NMOS pass devices usually consume smaller area [23]. For LDOs without charge pump, a PMOS pass device could be better in terms of area consumption, since it can turn on with large overdrive voltage [19].

Current efficiency

Efficiency is one of the most important parameters in PMUs. Typically, if people talk about efficiency, they mean power conversion efficiency. For linear voltage regulators the theoretical efficiency is inherently given by $\eta_{max} = V_{out}/V_{Bat} \cdot 100\,\%$. A more meaningful comparison parameter for linear voltage regulators seems to be the current efficiency. It is defined as $\eta_{current} = I_{out}/(I_{Bat} + I_q) \cdot 100\,\%$. The current efficiency shows how much auxiliary

[11] called “capacitor-free” or “capacitor-less” linear voltage regulator [23]

current I_q is consumed by the voltage regulator itself. This is particularly important for systems where battery power is restricted.

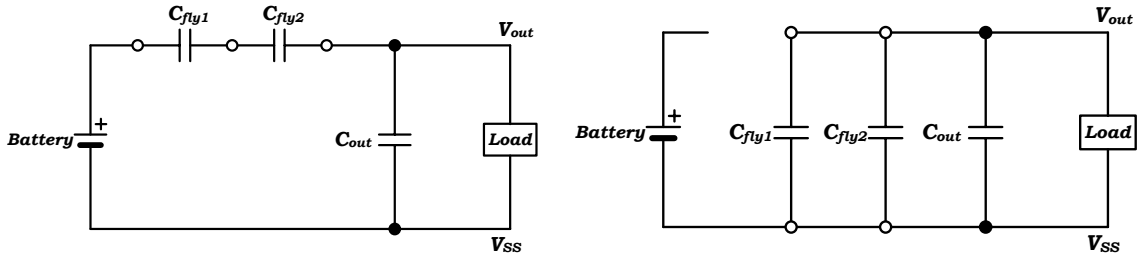
3.1.2 The trend to capacitor-less linear voltage regulators

Capacitor-less[12] linear voltage regulators play a big role in SoC designs since they can be designed very compact and cost efficient. In order to achieve a comparable load regulation to non capacitor-free regulators the bandwidth of a capacitor-less regulator has to be much higher, since there is only a small integrated capacitor C_{int} that buffers the output voltage.
Nevertheless, the energy during load jumps has to be provided from somewhere – since C_{ext} doesn't exist any more, the energy comes from C_{int} and due to the high regulator bandwidth also from C_{in}. Therefore, C_{in} has to be placed as close as possible to the supply pins of the regulator in order to reduce wiring parasitics and to ensure high regulation speeds.

3.2 Switched Mode Power Supplies

Switched Mode Power Supplies (SMPS) are very popular voltage regulators since they provide very high power conversion efficiencies. A lot of different SMPS topologies have been developed [50]. The different types are designed to either step-down[13] the input voltage or to step up the input voltage[14] or to do both: step-up and step-down the input voltage[15]. Furthermore, different topologies are used for different power classes. The different SMPS topologies can provide power from a few milliwatts up to more than several megawatts [50].
SMPS in mobile phones typically have to provide output power below 1 W. In this thesis the focus will be on topologies that will provide this low power class with very high power conversion efficiency.
In principle, the SMPS can be classified in two different categories: First, there are SMPS that operate without any power inductor – they only use capacitors for the power conversion. This class of SMPS is called "Switched Capacitor DC-DC Converter" (SC DC-DC).

[12] Capacitor-less means the regulators can operate without any external buffer capacitor C_{ext} on the output (see Fig. 3a). Integrated buffer capacitors C_{int} are not considered by this denotation.
[13] called buck converter or step-down converter
[14] called boost converter or step-up converter
[15] buck-boost converter



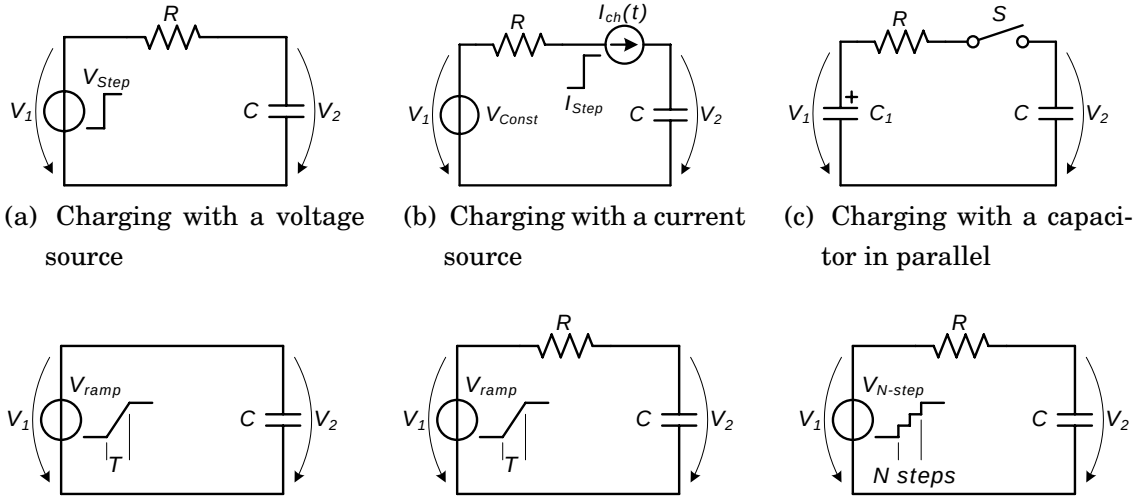
(a) Phase 1 (b) Phase 2

Figure 4: SC DC-DC step-down converter

The second class of SMPS is called “Inductor Based DC-DC Converter” (IB DC-DC). IB DC-DC needs inductors and capacitors for operation. In terms of full on chip integration, this is a disadvantage as the integration of the large power inductors with high quality factors is a challenging task with today’s technologies.
SC DC-DC and IB DC-DC will be discussed a bit more in detail in the next section.

3.2.1 Switched Capacitor DC-DC Converter (SC DC-DC)

The idea of SC DC-DC is to transport the energy coming from a battery to a load only by means of capacitors. They can be used either to step-down, step-up or also to step-down and step-up DC voltages. The basic principle of such a converter is illustrated in Fig. 4. It is an example of an SC DC-DC step-down converter where the output voltage of the converter is ideally one third of the input voltage in steady state.
Energy transportation is done in two phases. In the first phase (see Fig. 4a) the so-called flying capacitors C_{fly1} and C_{fly2} are connected in series between the battery node and the output capacitor C_{out}. This forms a capacitive voltage divider where C_{out} will be charged if V_{out} is smaller than one third of the battery voltage. In the second phase (see Fig. 4a) the configuration of the flying capacitors C_{fly1} and C_{fly2} is changed – now they are connected in parallel to C_{out}. Again if V_{out} in phase 1 is smaller than one third of the battery voltage, then the voltage across C_{fly1} and C_{fly2} is higher than V_{out} and therefore charge flows from C_{fly1} and C_{fly2} to C_{out}. This means that V_{out} is charged in phase 2 as well as in phase 1.



(a) Charging with a voltage source

(b) Charging with a current source

(c) Charging with a capacitor in parallel

(d) Charging with a voltage ramp

(e) Charging with a voltage ramp with a resistance

(f) Charging with a voltage source in N steps

Figure 5: Charging of a capacitor C by means of different sources

3.2.1.1 Charging Capacitors - Physical Limitation

In order to understand the limitations of SC DC-DC it is important to understand their basic functionality. As written before energy transportation from the input to the output of the converter is done only by switched capacitors. Therefore it is beneficial to study the theoretical possible energy conversion efficiency that we could get if different source voltages will charge a single capacitor C. Fig. 5 shows six different ways to charge a single capacitor.
In Fig. 5a a capacitor C is charged by means of a unity step V_{Step}. Let's assume that the capacitor C is pre-charged to the voltage V_2 at time instant zero and that C will be charged from V_2 to V_1. The provided energy from the voltage source V_{Step} is then

$$\Delta W_{Step} = V_1 \cdot \Delta Q \tag{4}$$

and the additional energy stored in the capacitor is

$$\Delta W_C = \frac{1}{2} C V_1^2 - \frac{1}{2} C V_2^2 \quad . \tag{5}$$

Combining Eq. 4 and 5 gives the energy conversion efficiency if a capacitor C is charged with a voltage step:

$$\eta_V = \frac{\Delta W_C}{\Delta W_{Step}} = \frac{1}{2} \frac{V_1 + V_2}{V_1} = \frac{1}{2} \left(1 + \frac{V_2}{V_1} \right) = \frac{1}{2} \left(1 + u_r \right) \tag{6}$$

with

$$u_r = \frac{V_2}{V_1} \in [0,1] \quad . \tag{7}$$

From Eq. 6 it can be seen that in ideal case the energy conversion efficiency only depends on the voltage ratio of V_1 and V_2 – the value of the series resistor R doesn't contribute to the power conversion efficiency. Furthermore it can be seen that the smaller the voltage difference $V_1 - V_2$ the higher the conversion efficiency. If $V_2 = 0$ as it is the case in digital circuits, we get the well-known conversion efficiency of $\eta_V = 1/2$ [48]. If V_2 is close to V_1, efficiencies up to almost 100 % are possible. This awareness is of particular importance for SC DC-DC designs.

Let's have a look at the next scenario depicted in 5b. There, a capacitor C is charged by an initial voltage V_2 up to V_1 by means of a current source I_{ch}. For this scenario we get the same power conversion efficiency as above:

$$\eta_I = \frac{\Delta W_C}{\Delta W_{Const}} = \frac{1}{2}\frac{V_1 + V_2}{V_1} = \frac{1}{2}(1 + u_r) \quad \text{with} \quad u_r = \frac{V_2}{V_1} \in [0,1] \quad . \tag{8}$$

Important thing about Eq. 8 is that the power conversion efficiency is independent of the current waveform provided by I_{ch} and again it is independent of the series resistance R.

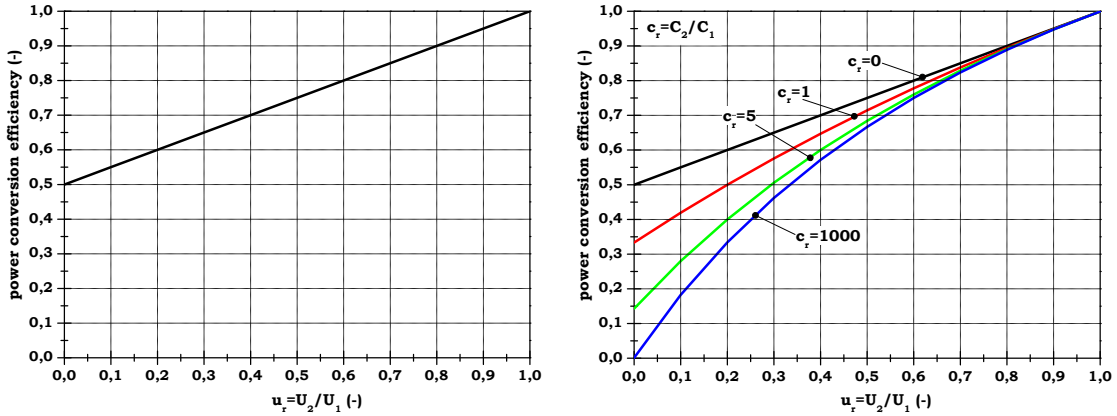
In the next scenario depicted in Fig. 5c it should be checked how the power conversion efficiency behaves in a case where a capacitor C_1 charges a second capacitor C. In this case, the power conversion efficiency is

$$\eta_C = c_r \frac{1 + 2 \cdot c_r \cdot u_r - u_r^2 - 2 \cdot c_r \cdot u_r^2}{2 \cdot c_r + c_r^2 - 2 \cdot c_r \cdot u_r - c_r^2 \cdot u_r^2} \tag{9}$$

where

$$c_r = \frac{C}{C_1} \in [0,\infty] \quad \text{and} \quad u_r = \frac{V_2}{V_1} \in [0,1) \quad . \tag{10}$$

Fig. 6 shows the different power conversion efficiencies for different voltage ratios u_r and different capacitor ratios c_r. The plot shows that the conversion efficiencies strongly depend on the voltage ratios u_r and of course it can be seen that the higher the voltage difference $V_1 - V_2$ (before closing the switch S) the lower the power conversion efficiency. Furthermore it can be seen from plot 6b that the conversion efficiency also depends on the capacitor ratio c_r. The impact is higher for higher u_r that means that conversion efficiency will



(a) η_V and η_I (b) η_C

Figure 6: Power conversion efficiencies η with respect to different u_r and c_r ratios

become lower if capacitor C is large in relation to C_1. But especially if the voltage difference $V_1 - V_2$ is small, the conversion efficiency dependency on the capacitor ratio c_r is quite small as well.
Let's have a look at the next scenario where a capacitor is charged by means of a voltage ramp V_{ramp} as it is depicted in Fig. 5d. If the applied voltage ramp is

$$v_1(t) = \frac{V_{Bat}}{T} \cdot t \tag{11}$$

then the current through the capacitor is

$$i_C(t) = C \cdot \frac{\mathrm{d}v_1(t)}{\mathrm{d}t} = \frac{V_{Bat}}{T} \quad . \tag{12}$$

From Eq. 11 and 12 the required energy for charging C can be calculated:

$$\Delta E_{ramp} = \int_{t=0}^{T} v_1(t) \cdot i_C(t)\, \mathrm{d}t = \frac{C \cdot V_{Bat}^2}{2} \quad . \tag{13}$$

Since the stored energy in the capacitor C is $\Delta E_C = \frac{C \cdot V^2}{2}$ the energy conversion efficiency is

$$\eta_{ramp} = \frac{\Delta E_C}{\Delta E_{ramp}} = 100\,\% \quad . \tag{14}$$

It can be seen that the energy conversion efficiency η_{ramp} is independent of the rise time T of the voltage source V_{ramp} – the conversion efficiency is always 100 %. This is because the voltage source V_{ramp} and capacitor C don't see any voltage difference during charging.

Fig. 5e shows a more realistic scenario where a resistor R is included in the schematic that represents the series resistance of the whole current path. In this case the required energy which comes from V_{ramp} depends on both, the rise time T of the ramp and the series resistance R in the current path:

$$\begin{aligned} \Delta E_{ramp1} = \frac{C \cdot V_{Bat}^2}{2} + \frac{R \cdot V_{Bat}^2 \cdot C^2}{T} + \\ \frac{e^{-\frac{T}{C \cdot R}} R^2 \cdot V_{Bat}^2 \cdot C^3}{T^2} - \frac{R^2 \cdot V_{Bat}^2 \cdot C^3}{T^2} \end{aligned} \tag{15}$$

If we insert the limits for T and R we get

$$\lim_{T \to 0} \Delta E_{ramp1} = C \cdot V_{Bat}^2 \quad \forall\, R > 0, C > 0 \tag{16}$$

$$\lim_{R \to 0} \Delta E_{ramp1} = \frac{C \cdot V_{Bat}^2}{2} \quad \forall\, T > 0, C > 0 \tag{17}$$

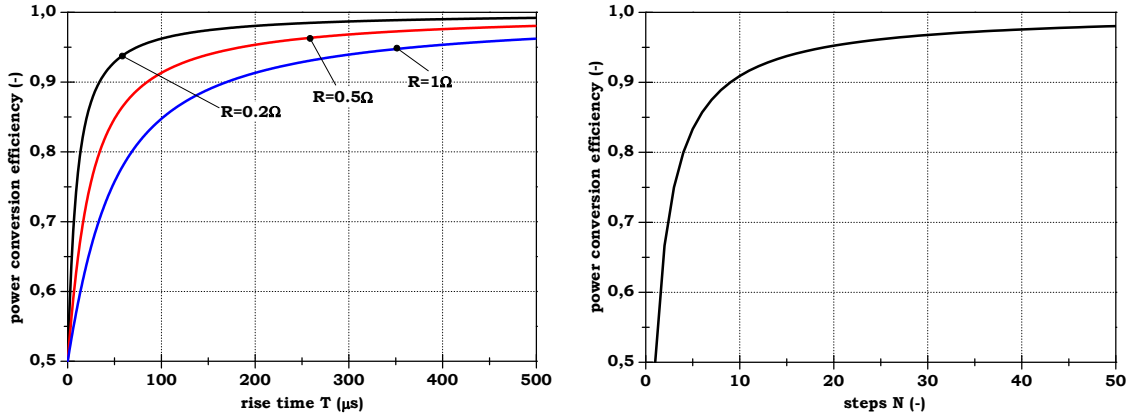
The results are as expected – a very short rise time equates to a unit step of the voltage source and therefore half of the energy provided by the voltage source is burned in the series resistor. If R is very small, then there is the case considered in Eq. 13 where a voltage ramp charges a capacitor without any series resistance.

Fig. 7a shows the power conversion efficiencies eta_R for different voltage rise times T and different series resistances R. If a capacitor is charged with voltage ramps with longer rise times T, the power conversion efficiencies are higher. Furthermore it can be seen that R also has an influence now on the conversion efficiency eta_R. The lower R is the higher eta_R becomes.

From the previous investigations it can be summarized now that there are two possible strategies to charge a single capacitor without large losses: The first strategy is to charge capacitors with voltage sources close to the initial voltage of the capacitor. The second strategy is to charge with linear voltage ramps. Since voltage sources, which generates such ramps don't exist the strategy has to be reconsidered.

Fig. 5f shows a possible workaround were N superimposed voltage sources approximated an ideal voltage ramp. This means that the capacitor C will be charged to the desired value V_1 in N steps where the voltage steps have the height of V_{Bat}/N. Furthermore it should be assumed that each charging step takes ΔT and that $\Delta T \gg R \cdot C$. Then the energy in the capacitor after N steps is

$$\Delta E_{Ca} = \frac{1}{2} \Delta Q \left(\frac{V_1}{N} \cdot n + \frac{V_1}{N} \cdot (n-1) \right) \tag{18}$$



(a) Charging a capacitor by means of a voltage ramp with different rise times T and with different resistances R

(b) Charging a capacitor by means of voltage steps

Figure 7: Energy conversion efficiencies η for charging a capacitor $C = 10\,\mu\text{F}$ to $V_{bat} = 1.2\,\text{V}$

and the energy provided by the voltage source is

$$\Delta E_{Bata} = \Delta Q \left(\frac{V_1}{N} \cdot n \right) \quad . \tag{19}$$

This gives a power conversion efficiency of charging a capacitor C in N voltage steps of

$$\eta_N = \frac{\Delta E_{Ca}}{\Delta E_{Bata}} = \frac{N}{N+1} \quad . \tag{20}$$

Fig. 7b shows the power conversion efficiencies η_N for different voltage steps N. If $N = 1$, which is the typical case in digital circuits, $\eta_N = 50\,\%$. However, if $N \to \infty$ then the conversion efficiency becomes $\eta_N = 100\,\%$, which is the same result as if the capacitor is charged with an ideal voltage ramp.

Summary

From the previous analysis we can conclude that:

1. The power conversion efficiency of capacitors strongly depends on the voltage ratio u_r between the voltage source and initial capacitor voltage. Conversion efficiency is high if the voltage ratio $u_r = 1$.

2. The power conversion efficiency does not depend on the current waveforms that charge the capacitor. We get the same power conversion efficiency, regardless whether large or small current sources are used to

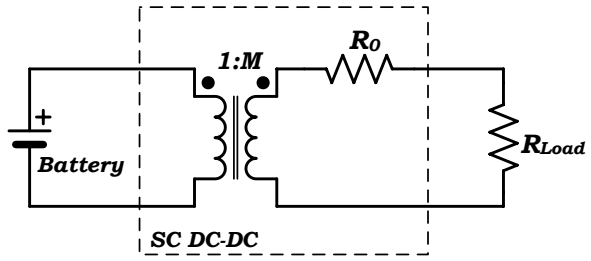


Figure 8: DC model of a SC DC-DC converter

charge a capacitor. This also means that power conversion efficiency does not depend on the value of the on on-resistance of a switch S or on the wire resistances of the power routing (if the source doesn't have a ramp shape).

3. The achieved power conversion efficiencies shown in Fig. 6 are a fundamental limit. Even if ideal components are used, the conversion efficiencies cannot exceed these limits.

3.2.1.2 SC DC-DC model

Fig. 8 shows a DC model of a SC DC-DC [37]. The model is composed of an ideal DC transformer with the turns ratio $1 : M$ and an output resistance R_0. If R_{Load} is disconnected, the converter operates in open loop configuration and the output voltage is

$$V_{out(openloop)} = \frac{V_{Bat}}{M} \quad . \tag{21}$$

3.2.1.3 Converter Efficiency

Maybe the most important parameter of SC DC-DCs is the achieved power conversion efficiency. Of course it should be as high as possible – in ideal case 100 % – in order to allow long battery life times but there is also a physical upper boundary of the efficiency that is valid for all SC DC-DC converters [37]

$$\eta_{SCDC-DC} = \frac{V_{out}}{V_{Bat}} \frac{1}{M} \tag{22}$$

where M is the open loop conversion ratio of the converter (gain factor) without any load[16]:

$$M = \frac{m}{n} = \frac{V_{out}}{V_{Bat}} \quad \text{with} \quad m, n \in \mathbb{N} \quad \text{and} \quad R_{Load} = \infty \ . \tag{23}$$

It can be seen from Eq. 22 that the conversion efficiency $\eta_{SCDC-DC}$ directly depends on the ratio of the battery voltage and the converter output voltage. If $M = 1$, then an SC DC-DC achieves similar conversion efficiencies as linear voltage regulators. For appropriate voltage ratios very high converter efficiencies can be achieved – again theoretical 100 % are possible. If were not the case, the only possibility to increase the converter efficiency would be to choose a suited gain factor M. Fig. 9 shows the theoretical converter efficiencies for different battery voltages and fixed output voltage of $V_{Out} = 1.2\,\mathrm{V}$ and by using different gain factors M. For each battery voltage the usage of a certain gain factor gives optimum power conversion efficiency. If the input voltage varies in a wide range, a lot of different gain factors often have to be implemented in order to keep the power conversion efficiencies high. The technique that automatically changes the configuration of the flying caps or in other words the technique that automatically adjusts the gain of the converter depending on the input-output voltage ratio is called "gain hopping" [32].

The energy conversion efficiency calculated from Eq. 22 comprises only the inherently arising losses due to charging and discharging the capacitors[17]. Typically, this loss contributor is the biggest one but of course, there are additional ones that also have to be considered:

1. Parasitic capacitances on the terminals of the flying capacitors: They have to be charged and discharged every switching cycle that reduces the converter efficiency. Especially for fully integrated capacitors in CMOS technology the parasitic bottom plate capacitance C_{BP} can be quite high in proportion to intrinsic capacitance C. For instance for poly-Nwell capacitors C_{BP} can be 5 %–10 % of C [49].

2. Gate drive losses of the switches: Switches are used to reconfigure the capacitor network in order to transport the energy from the input to the output of the converter. Driving the gates of the switches gives switching losses, which again reduces the conversion efficiency of the converter.

[16] M is equivalent to the turns ratio M defined in the SC DC-DC model in 3.2.1.2.

[17] The loss type can be called "conduction losses" since the power is dissipated on the series resistance of the capacitor R_{ESR} and the on-resistance of the switch R_{on} [4].

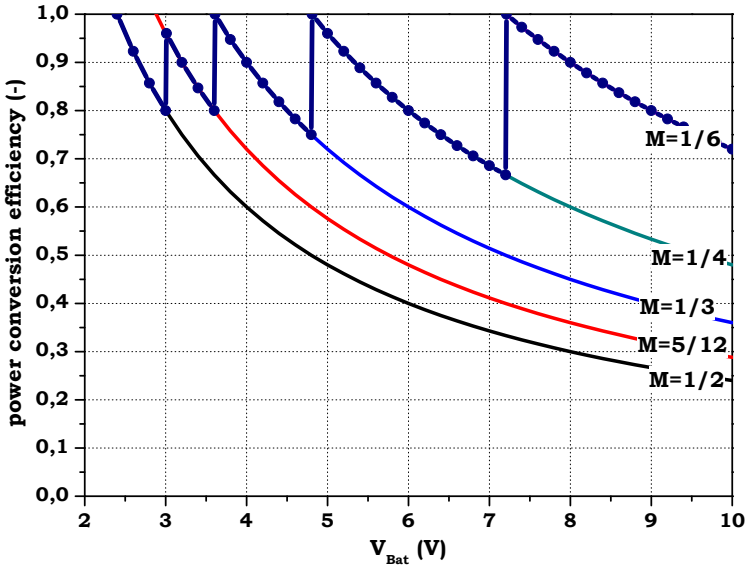


Figure 9: Theoretical achievable SC DC-DC converter efficiencies with different gain factors M for different battery voltages V_{Bat} and fixed output voltage of $V_{out} = 1.2\,\mathrm{V}$

3. Controller: It is used to regulate the converter output voltage to the desired value. The power consumption of the controller also has to be considered.

The loss contribution of a fully integrated SC DC-DC converter in 45 nm CMOS technology reported in [49] with a final efficiency of 68.5 % is for instance: 14.8 % conduction losses, 8.8 % bottom plate losses, 7.2 % switching losses and 0.7 % control and other losses.

3.2.1.4 Controller strategies for SC DC-DC

The controller regulates the output voltage V_{out} of the converter to the desired voltage. From the SC DC-DC model in Fig. 8 it can be seen that in principle there are two possible approaches which can be used to regulate the output voltage: The first opportunity is to change the gain factor M. With this method only coarse output voltage regulation is possible since there is only a limited amount of different gain factors. The second opportunity is to change the output resistance R_0 of the converter. Changing the on-resistance of the switches used in the capacitor network in order to reconfigure the the capacitor connections can do this or it can also be done by changing the switching frequency of the converter.

A very common controller strategy for SC DC-DCs is pulse frequency modulation (PFM). The idea of this mode is to switch the flying capacitors only if energy is needed at the converter output. The rest of the time, there is no switching activity. A voltage comparator can be used to monitor the converter output voltage V_{out}. If V_{out} goes below a certain threshold voltage, the converter starts to switch again which transports energy from the input to the output.
Beside PFM, also fixed frequency control strategies can be used. A very common fixed frequency control mode is pulse width modulation (PWM). There the on-phases of the switches are varied depending on the duty cycle of the actuating variable of the controller. Another method is to change the on-resistance of the converter by segmenting the switches. It is often used if digital controller implementations are used.

3.2.1.5 Output resistance

The output resistance R_0 of the converter (see Fig. 8) gives information about the output power capability of the converter at a certain output voltage. The output impedance can be constructed with two different asymptotic limits, the so called fast and slow switching limits (FSL and SSL) [52]. If a converter operates in SSL, the time constant τ_N of the switching network is much smaller than the switching period T_S ($\tau_N \ll T_S$). This means that the charge redistribution in the capacitor network will always be finished during every switching cycle. In this case R_0 is proportional to [37]

$$R_0 = R_{SSL} \sim \frac{1}{C \cdot f_{sw}} \quad . \tag{24}$$

On the other hand there is the situation where τ_N is much larger than the switching period T_S ($\tau_N \gg T_S$). In this case the charge redistribution will not be finished during every switching cycle and therefore, the output impedance will become almost independent of the switching frequency of the converter. Under this circumstance the output impedance of the converter is only proportional to the on-resistances of the switches in the capacitor network [52]:

$$R_0 = R_{FSL} \sim R_{on\_switches} \quad . \tag{25}$$

Fig. 10 shows the output impedance R_0 of the SC DC-DC converter with $M = 1/3$ depicted in Fig. 4 for different switching frequencies. It is assumed that

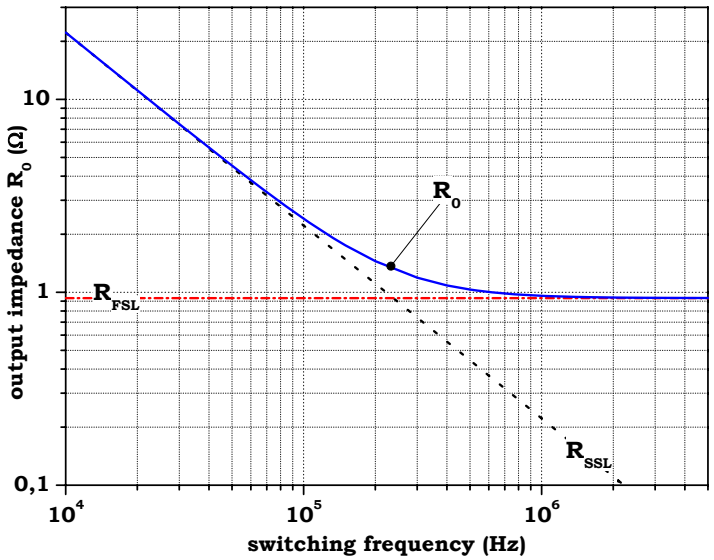


Figure 10: Output impedance of a SC DC-DC converter with $M = 1/3$

1 μF flying capacitors are used and that seven switches with an on-resistance of 600 mΩ are used for reconfiguring the switching network.
Depicted are the two asymptotic limits R_{FSL} and R_{SSL} and the complete output impedance R_0. It can be seen that R_{SSL} becomes equal to R_{FSL} at a frequency of about 200 kHz. At this frequency R_0 starts to become independent of the switching frequency and R_0 converges to R_{FSL} that is about 930 mΩ in this case.
With the knowledge of R_{FSL} the highest possible output current that can be provided by the converter can be estimated. If V_{Bat_min} is the lowest allowed battery voltage and V_{Out_min} is the lowest allowed output voltage of the converter, then the highest possible output current can be calculated with

$$I_{Out\_max} = (V_{Bat\_min} \cdot M - V_{Out\_min}) \frac{1}{R_{FSL}} \quad . \tag{26}$$

3.2.2 Inductor Based DC-DC Converter (IB DC-DC)

Inductor based DC-DC converters (IB DC-DC) are popular due to their high power conversion efficiency over a wide input-output voltage ratio. They are designed to provide output power from several mega watts down to some milliwatts [60], [20], [56].
In PMUs for mobile applications, the converters are typically designed for an output power up to some watts. One of the most important converter types

is the step-down or buck converter since it is necessary to convert the battery voltage down to the desired voltage levels used in the chip.
The basic topology of SMPS shall be explained by means of a DC-DC buck converter that is shown in Fig. 11. The converter can be divided into four parts:

1. Input filter: The input filter is a very critical part in an IB DC-DC converter design since it has to block the fast and large transient current spikes which are inherently generated by the converter during normal operation. It is important that the input filter is placed very close to the converter in order to avoid large parasitic inductances on the power rails. This ensures that the voltage drops over these inductances will be limited.

2. Controller: The controller senses the output voltage V_{out} of the converter and controls the on- and off-times of the power switches M_P and M_N in a way that the output voltage V_{out} gets the desired value. Analogue and also digital controllers with different controller schemes can be implemented. Different control schemes are used to improve the converter efficiency and the load regulation performance for different kinds of loads and for different operating conditions.

3. Power Stage: The power stage routes the energy from the input to the output of the converter. Typically, large power switches are used in the power stage in order to reduce conduction losses and therefore also self-heating. Gate drivers control the power switches. Since they have to be fast, power efficient and accurate, their design can be quite challenging.

4. Output Filter: IB DC-DCs use LC-type output filters. The task of the output filter is to smooth the large voltage ripple on the switching node SW of the converter. Furthermore, the output filter is used to limit the current slopes in the power switches and in the power traces.

Main advantage of IB DC-DC converters is their high power conversion efficiency. The theoretically achievable power conversion efficiency is 100 %, also for different input voltages and for different load currents. Of course in practice the theoretically possible efficiency can never be achieved since the operation is always lossy. But at least converter efficiencies close to 100 % are possible today.

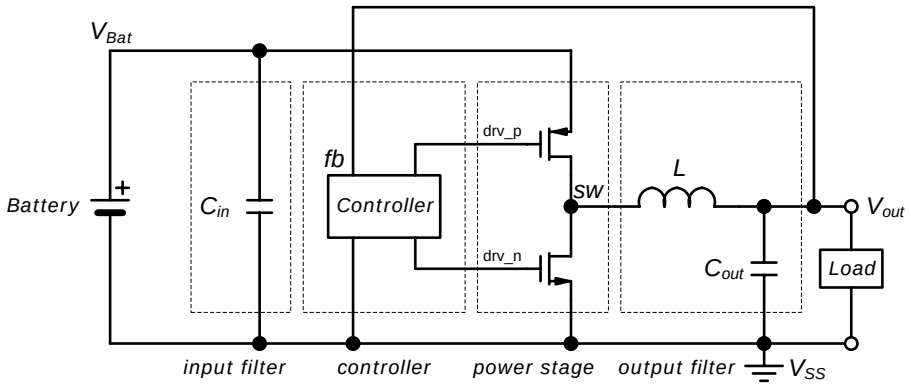


Figure 11: Principle topology of a DC-DC buck converter

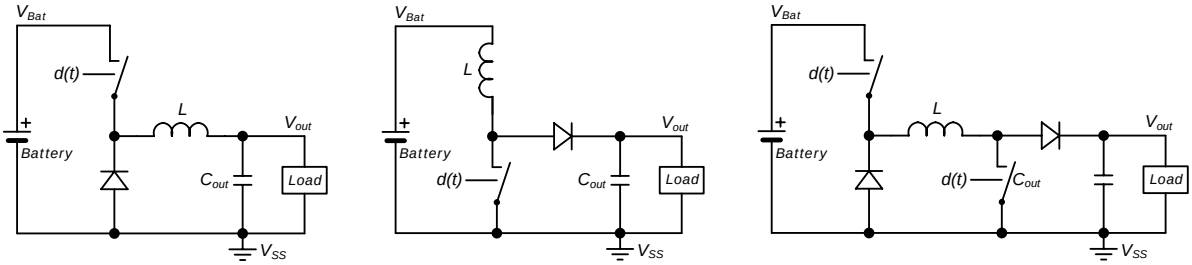
IB DC-DC converters can be used to convert a certain converter input voltage to a lower, higher or also a lower and higher output voltage. In the next section the different topologies shall be discussed briefly.

3.2.2.1 The three main topologies: Buck, Boost and Buck-Boost converters

The three basic topologies buck, boost and buck-boost converters are depicted in Fig. 12. Again it should be mentioned that all topologies use LC-type output filters.

Fig. 12a shows the principle topology of an IB DC-DC buck converter that converts an input voltage to an output voltage that is lower than the input voltage. A controller regulates the duty cycle of the switch depending on the output voltage deviation of the converter. A diode provides a defined current path for the case where the switch is off. The efficiency of the converter can be improved by replacing the diode by a MOS power switch. Such converters are then called “synchronous rectifier” and they typically achieve higher efficiency values due to the lower conduction losses on the low side power path of the converter. A disadvantage of the synchronous rectifiers is that the switching time instants of the power switches have to be controlled very accurately as shoot through current and long body diode conduction durations have to be avoided.

Fig. 12b shows the basic principle of an IB DC-DC boost converter that converts a certain input voltage to a higher output voltage. The topology is quite similar to the IB DC-DC buck converter – only the components are re-arranged. Again a controller regulates the on and off times of the power



(a) DC-DC buck converter (b) DC-DC boost converter (c) DC-DC buck-boost converter

Figure 12: Three basic IB DC-DC converter topologies used in PMUs

switch. Also here a MOS power switch can exchange the diode in order to improve the converter efficiency.

Fig. 12c shows an IB DC-DC buck-boost converter. This topology allows converting a given input voltage either to a lower (buck operation) or to a higher output voltage (boost operation). It only depends on the duty cycle d if the converter operates as buck or boost converter. A disadvantage of the IB DC-DC buck-boost converter is that it achieves lower efficiency values in buck mode than a "real" buck converter. In boost mode lower efficiency values than a "real" boost converter can be achieved, since in sum there is one more switch in the power path that generates losses.

Table 2 shows a summary of important relations of the three different IB DC-DC converter types shown in Fig. 12. The equations are simplified, so no parasitics are considered.

Table 2: Important converter equations in continuous conduction mode

	Buck	Boost	Buck-Boost
duty cycle $\boldsymbol{D}$	$\frac{V_{out}}{V_{Bat}}$	$1 - \frac{V_{Bat}}{V_{out}}$	$\frac{V_{out}}{V_{Bat}+V_{out}}$
coil current ripple $\boldsymbol{\Delta I_L}$	$\frac{1}{f_s}\frac{V_{out}}{V_{Bat}}\frac{V_{Bat}-V_{out}}{L}$	$\frac{1}{f_s}(1 - \frac{V_{Bat}}{V_{out}})\frac{V_{Bat}}{L}$	$\frac{1}{f_s}\frac{V_{out}}{V_{Bat}+V_{out}}\frac{V_{Bat}}{L}$
output voltage ripple $\boldsymbol{\Delta V_{out}}$	$\frac{V_{out}}{8 \cdot L \cdot C \cdot f_s^2}(1-\frac{V_{out}}{V_{Bat}})$	$\frac{I_{out}}{2 \cdot C \cdot f_s}(1 - \frac{V_{Bat}}{V_{out}})$	

3.2.2.2 Fully integrated SMPS

Customers always prefer the simplest possible solution for a certain applica-

tion. They would like to get a one-chip solution where the complete system with all the blocks and passive components is integrated in a single chip. This eases their PCB designs and furthermore it saves PCB area and therefore costs.
The situation for IC manufactures looks different: Since a lot of functionality has to be handled within a single chip the systems become huge and very complex. This complicates the complete design flow since complex and costly simulation tools are necessary to guarantee the functionality of the system.
"Power on chip" is a very popular research field that has the target to integrate a complete PMU fully beside a VLSI system on the chip. The challenge there is that the PMU has to handle the high battery voltages, large supply noise, large IR drops on the power rails and high self-heating due to high power dissipation on the chip.
One of the biggest challenges is the integration of high quality passive components suited for power conversion like capacitors and power inductors. Fig. 13 shows an overview of the performance of existing on chip inductors suited for power conversion. Depicted are the inductance densities versus the peak quality factors of different inductors presented in the recent years. You can see that quite impressive inductance densities have already been achieved – values of more than $1000\,nH/mm^2$ have been reported. Also inductors with very high quality factors have been reported. Power inductors with peak quality factors of more than 20 can be seen in the figure.
For highly efficient power conversion in IB DC-DC converters inductors with both high inductance densities and high quality factors[18] are required. This lowers the required switching frequency of the converter to feasible values and therefore limits the switching losses. And high quality factors are required in order to limit the converter losses due to the losses in the power inductor.

3.2.2.3 Level of Integration

SMPS can be built up in different levels of integration. Fig. 14 shows seven different levels of integration. First level in Fig. 14a shows an SMPS with external inductors, capacitors and power switches. Only the controller and the protection circuits are integrated in silicon. Such a design is often used for

[18]The quality factor of inductors is defined as ratio between the imaginary part and the real part of the impedance: $Q = \frac{2\pi f L}{Re}$.

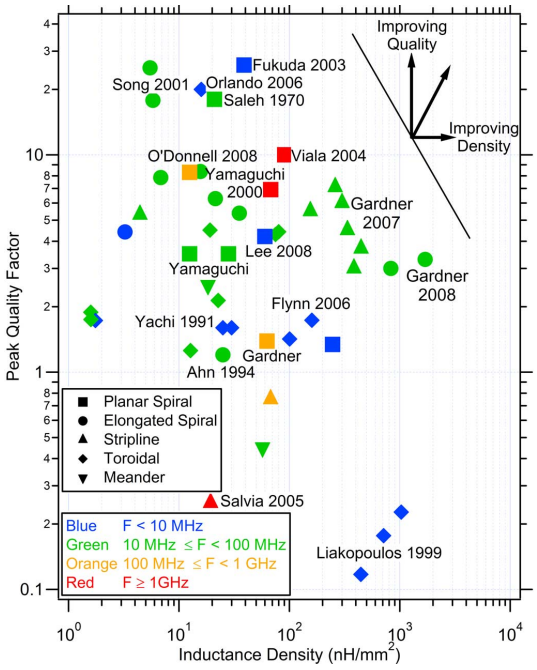


Figure 13: Inductance density versus peak quality factor of integrated inductors on Si-substrate [16]

converters with high output power since it allows you to use discrete power switches with high current drive and voltage capability. For instance, an example is the DC-DC buck converter TLE6389 from Infineon with input voltages up to 60 V and output currents of up to 2.3 A.

Fig. 14b shows a solution where the power switches are integrated in silicon. Because of the integration it is possible to control the power switches in a more accurate way since the parasitics of the switches can be minimized. Therefore, higher switching frequencies are possible which allows reducing the sizes of the components of passive input and output filters of the converter. Furthermore, integrated current sensing techniques can be implemented. A disadvantage of course is that now the whole power has to flow through the chip, which requires a well-done on-chip power routing. Also self-heating has to be considered since the power flow now goes through the chip. An example of such an approach is the DC-DC buck converter TLF50281EL from Infineon where integrated power switches are used.

The next level of integration depicted in Fig. 14c shows a co-packaged SMPS where single passive components are put into the package side-by-side with the active die. In general people talk of Power System in Package (PSiP) in this case. The integration of the power inductor into the package is depicted.

All other passive components are placed outside of the chip-package again. In many discussions it was found that the main driver of this approach is the fact that customers don't like to engage in power inductors and power magnetics. There doesn't seem to be a technical reason for preferring the integration of power inductors instead of the capacitors in a package. An example of this level of integration is the buck converter EP5348UI from Enpirion where the power inductor is placed into the package.
The next level of integration depicted in Fig. 14d shows the placement of the chip die and the complete output filter of an IB DC-DC converter side-by-side in one package. An advantage of this approach is that parasitics on the power traces are minimized further and PCB area can be saved.
The next level of integration is the integration of all components required for the SMPS operation into the chip package. This can be done side-by-side as depicted in Fig. 14e or stacked as depicted in Fig. 14f. The advantage of the full integration is that customers don't have to think about the circuit any more and furthermore all the power paths are minimized which allows a higher power conversion efficiency with higher converter switching frequency at the same time. Examples of such integration are the buck converter LM2825 from National Semiconductor and the buck converter TPS82677 from TI.
Last level of integration is shown in Fig. 14g. There, all the passive components required for the SMPS are integrated on chip in silicon. This allows very compact routing of the power traces and therefore opens the opportunity for the implementation of very high frequency DC-DC converter designs since parasitics generally are minimized. This approach is often called Power System on Chip (PSoC). Nevertheless, the basis of this approach is the availability of high quality on chip power inductors and capacitors with large values. Only then are high power conversion efficiencies are possible with such approaches. Since the integration of such high performance passive components is not possible with today's technologies, no commercially traded power converters exist in this sector.
But at least you can see that there are a lot of research activities on this topic and of course a lot of publications about PSoC solutions are already available. A nice overview of existing solutions is given in [57].

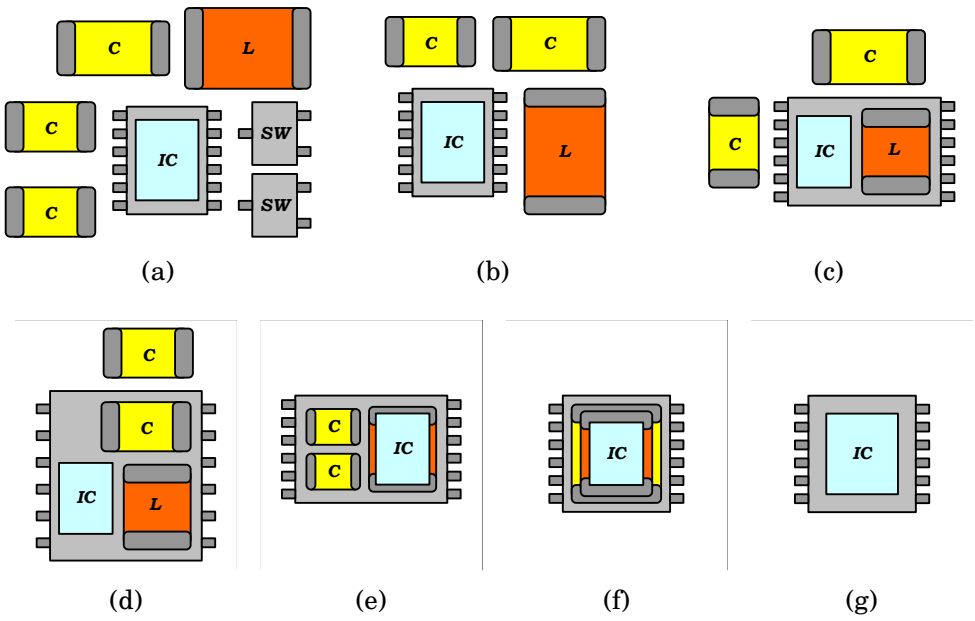


Figure 14: Level of integration for SMPS

3.3 Summary

Three different types of voltage converters are used in power management units of large systems. The first type is linear voltage regulators which can lower a given input voltage to a certain output voltage. Common linear voltage regulators only need buffer capacitors on the regulator output. There is a trend to “capless” linear voltage regulators that require no external buffer capacitors. Capless voltage regulators are one of the cheapest solutions but they suffer in terms of power conversion efficiency.

The second type of voltage converters are switched capacitor DC-DC converters. The energy conversion efficiency of these converters mainly depends on the voltage ratio of the input and the output voltage. “Gain Hopping” is a method to optimize the converter efficiency for different input/output voltage ratios. The different gain hopping modes are implemented by means of capacitor networks. The power conversion efficiency is typically much higher than for linear voltage regulators.

The last type of voltage converters is inductor based DC-DC converters. The characteristic of this type of converter is that power inductors are used in the output filter. The advantage of this converter type is that highest possible power conversion efficiencies can be achieved – also for different input/output voltage ratios and for different load currents. Main drawback of this converter

type is that power magnetics is used in the output filter. This makes the application more expensive and furthermore this is the main handicap of full integration.
Table 3 shows a summary of important characteristics of SC DC-DC and IB DC-DC converters, and linear voltage regulators. Only typical scenarios are compared.

Table 3: Comparison of different power management blocks

	Linear regulator	SC DC-DC	IB DC-DC
Efficiency	lowest[a]	high[b]	highest
Complexity	simple	harder	most difficult
Cost	cheap[c]	expensive[d]	expensive[e]
Integration level	SiP/monolithic	SiP/monolithic	SiP/monolithic[f]
Dynamic response	fastest	slow	fast
Output ripple	very low	moderate	moderate

[a] Efficiency of a linear regulator is given by $\eta = V_{out}/V_{in}$. Therefore, conversion efficiency is typically low. But if the regulated output voltage is close to the input voltage, the conversion efficiency could be high as well, even higher than for SMPS.

[b] Efficiency of an SC DC-DC is given by $\eta = V_{out}/(G \cdot V_{in})$. In case of well-suited converter input-output voltage ratios, efficiencies close to 100 % can be achieved.

[c] Typically, only one discrete input and one output capacitor is required. In case of capless linear voltage regulators, no output capacitor is required any more. Due to simple topology the design costs are low.

[d] The higher the amount of gain modes the higher the amount of required single capacitors. For very low output power converters these capacitors can be integrated monolithically on chip that reduces PCB area and it also reduces the pin count. But of course the occupied chip area will increase due to the capacitors and the power switches in the switching network.

[e] Main cost contributor in IB DC-DC converter designs is the power inductor required in the output filter. Another cost adder is the design costs due to the high system complexity.

[f] Several fully monolithically integrated IB DC-DC converters have been published in the recent years. The bottleneck of these designs are always the small inductance values and losses of the power inductors. Therefore, fully integrated IB DC-DC converters achieve much lower efficiency values than converters with external output filter.

4 Components of IB DC-DC converters

Several different blocks are critical for the performance of IB DC-DC converters. First, there are the passive components like resistors, capacitors and inductors. Resistors can be used in the power path for measuring the current flow, capacitors are used at the converter input as blocking capacitors and at the converter output to lower the voltage ripple, and inductors are used to limit the current slopes in the power paths and also to reduce the voltage ripple on the converter output. Second, there is the power stage that controls the power paths. The power stage mainly consists of the power switches and the gate divers. Third, there is the controller that controls the power switches. In principle, a controller strategy that allows high power conversion efficiencies over a wide load range should be used and furthermore the controller should be able to regulate the output voltage to the desired value independently of the load and line changes. In this chapter the performance relevant properties of the different blocks in IB DC-DC converters will be discussed.

4.1 Passive Components

The different properties of power inductors and capacitors will be described briefly in the following section.

4.1.1 Power inductors

One major characteristic of IB DC-DC converters is that power inductors are required for the converter operation. The power inductors are used in the output filter in order to limit the current in the power paths and to smooth the voltage ripple of the converter output. Since the whole output power of the converter is flowing over the power inductors, a careful selection thereof is important in order to guarantee high converter performance over the whole specified load range.
In order to achieve highest possible converter performance you have to use power inductors with a small form factor, low electrical losses, and stable inductance values over the specified load current.
Two different types of power inductors are used in low power IB DC-DC converter designs:
The first type is the *wire-wound power inductor*. Wire-wound power inductors consist of a ferromagnetic core with a winding coil around the core. In order

to keep the magnetic flux within the coil that reduces AC losses and EMI problems, the whole power inductor is often shrouded in magnetic resign. Such coils are called “shielded” power inductors in contrast to “un-shielded” power inductors, where the magnetic flux also goes outside the coil.
The second power inductor type is the *multilayer power inductor*. This type is quite new on the market and is not offered by all power inductor vendors up to now. Main advantage of this inductor type is that large inductance values are possible with very small package sizes. Therefore, multilayer power inductors are typically preferred in applications for mobile devices where the form factor is one of the most critical parameters.

4.1.1.1 Losses in power inductors

Lossy power inductors reduce the converter efficiency. Furthermore the losses can heat the inductors to forbidden high values that can degenerate the magnetic performance subsequently. Table 4 shows a summary of the different loss contributors in power inductors. In principal, two different types of loss contributors can be distinguished: First, there are the winding losses which mainly occur due to the series resistances of the winding wires of the coils and second, there are the core losses which arise mainly from the remagnetising the ferromagnetic material in the coils.
Table 4 shows formulas that can be used for the estimationa of the losses in the power inductors. In general it can be seen that most of the losses are directly related to the operating frequency f. This means that the losses of the converter strongly increase due to the power inductors if the operating frequency is increased[19]. You also can see that the core losses depend on the amount of the ripple of the magnetic flux density ΔB. This means that the coil losses will increase strongly if the power inductors operate with higher current ripples. Last but not least it can be seen that the DC resistance of the windings generate DC losses that become disproportionately high for higher power inductor currents.

4.1.1.2 Characterization of power inductors

Power inductors are offered by a lot of different manufacturers. Therefore, a defined characterisation process in the laboratory is required which allows a

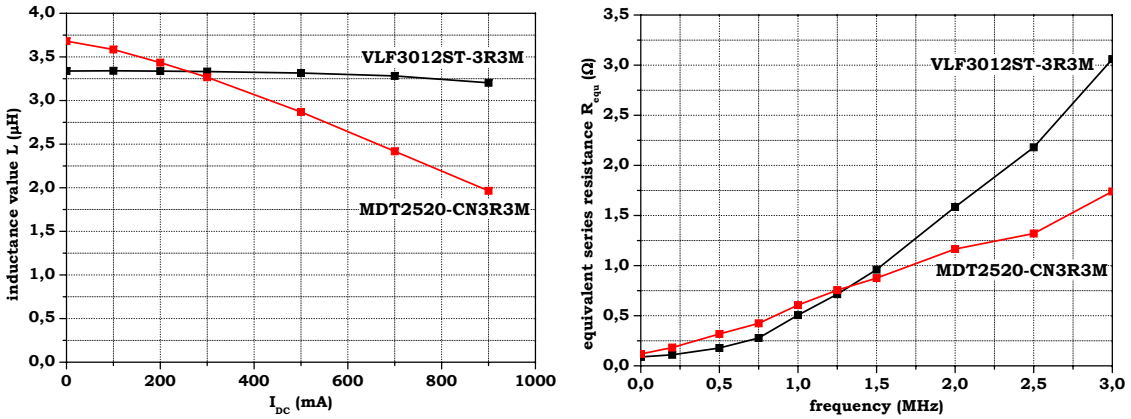
[19]Frequency of the remagetising the ferromagnetic material in the coil.

Table 4: Losses in power inductors and their behaviour

	loss type	behaviour
winding losses	DC copper losses	$P_C \propto I_{rms}^2 \cdot R_{DC}$
	skin effect	$P_S \propto k_S \cdot \sqrt{f}$
	proximity effect	winding shape, f
core losses	hysteresis losses	$P_H \propto k_H \cdot \Delta B \cdot f$
	eddy current losses	$P_E \propto k_E \cdot \Delta B^2 \cdot f$
	gap losses	core shape

pre-selection of suited power inductors for a respective application.
The following characterisation procedure is proposed:
Equivalent circuit diagram for the measurements is a resistor-inductor series connection (R-L). The elements R-L in the circuit diagram are measured at different frequencies and for different DC currents through the power inductors. As measurement device a Wayne Kerr Precision Magnetic Analyser 3260B is used to get an equivalent of R-L circuit diagram. In order to also get comparable results for different inductance values of the power inductor, the same AC current ripple magnitude has to be used for all measurements. Since the measurement device only allows adjusting the AC voltage ripple magnitude, a translation into an equivalent current ripple is required (adjusted voltage ripple on the measurement device depends on the inductance value of the power inductor).
It has to be mentioned that with the used measurement device it is not possible to find the absolute losses that would occur during normal DC-DC converter operation, but since all power inductors are characterised with the same AC current ripple, the relative losses among the different power inductors are comparable.
Fig. 15 shows, as an example, measurement results for two different power inductors. The first inductor VLF3012ST-3R3 is from the company TDK[20] and is a wire-wound type. The second inductor MDT2520-CN3R3M is from the company Toko[21] and is a multilayer power inductor. Both inductors have a spec-

[20] www.tdk.com
[21] www.toko.com



(a) DC bias dependency (b) Equivalent series resistance

Figure 15: Measured power inductor performance

ified nominal inductance value of 3.3 μH. The package size of the MDT2520-CN3R3 is 2.5 mm x 2.0 mm x 1.2 mm and for the VLF3012ST-3R3, which is a bit larger, it is 3.0 mm x 2.8 mm x 1.2 mm.

Fig. 15a shows the comparison of both inductors in terms of DC bias dependency. You can see that the inductance of the VLF3012ST-3R3 is quite stable for the depicted DC current range. In comparison, the inductance value falls for the MDT2520-CN3R3 significantly at higher DC currents. In IB DC-DC converter designs such behaviour has to be considered since a drop of the inductance value can cause stability problems of the controller of the converter. Another drawback is that a reduced inductance value would causes an increase of the peak-to-peak currents in the power paths of the IB DC-DC converters that reduces the converter efficiency and the lifetime of the converter.

Fig. 15b shows the measured equivalent series resistance $\boldsymbol{R_{equ}}$ of both power inductors for different operating frequencies. Since all loss contributors are combined in one value $\boldsymbol{R_{equ}}$[22] it really shows the loss performance of the whole coil and therefore it is a quite nice value for the coil comparison. For instance Fig. 15b shows that the MDT2520-CN3R3 has a much lower $\boldsymbol{R_{equ}}$ at higher frequencies than the VLF3012ST-3R3. Therefore, if switching frequency of the IB DC-DC converter were high, the usage of the MDT2520-CN3R3 would be the better choice since inductor losses would then be lower.

[22]The different loss contributors can be found in Table 4.

4.1.2 Capacitors

Capacitors are used as voltage smoothing capacitors at the output filter and as blocking capacitors at the input filter of the converter. In both cases the capacitors should have equivalent series resistances ($\boldsymbol{ESR}$) and equivalent series inductances ($\boldsymbol{ESL}$) as low as possible. This avoids large voltage drops on the input node of the converter in case of fast transient current waveforms and large voltage drops on the output of the converter in case of load jumps. Especially high frequency DC-DC converters are designed with very short current commutation times, which means that the current waveforms in the power traces have very steep slopes. Therefore, capacitors with low $\boldsymbol{ESL}$ values are mandatory.

Fig. 16a shows a simple and often used model of a capacitor. If a given current $i(t)$ is applied to the capacitor, then the voltage across the capacitor $u(t)$ is given by:

$$u(t) = \boldsymbol{ESR} \cdot i(t) + \boldsymbol{ESL} \cdot \frac{\mathrm{d}i(t)}{\mathrm{d}t} + \frac{1}{C} \int i(t)\mathrm{d}t \quad . \tag{27}$$

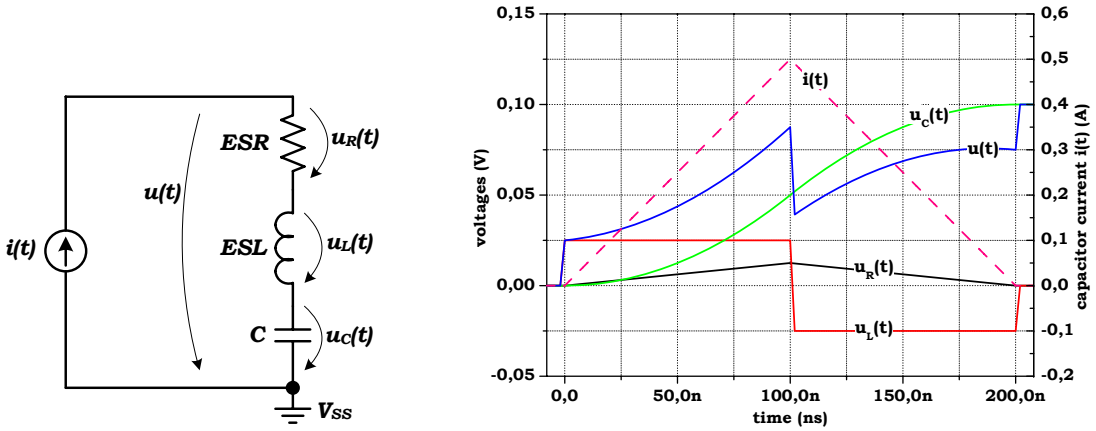
Fig. 16b shows the calculated voltage $u(t)$ across the capacitor if Eq. 27 is used – also shown are the different voltage drops on each parasitic element.

If it is assumed that a current ramp $i(t)$ is applied to the capacitor and if $C = 500\,\mathrm{nF}$, $\boldsymbol{ESR} = 25\,\mathrm{m\Omega}$ and $\boldsymbol{ESL} = 5\,\mathrm{nH}$, then it can be seen that the voltage drops u_R and u_L across the parasitic elements become quite large. Especially for very steep current ramps – which typically happens in IB DC-DC converters as it already has been mentioned before – the situation becomes critical.

Another important issue of capacitors is the dependency of the capacitance value on the bias point of the capacitor. For instance if a capacitor with a specified nominal capacitance value of $C_{nom} = 22\,\mu\mathrm{F}$ is used in an application the effective capacitance C_{eff} value which will be present in an certain application is often much lower than the specified nominal value C_{nom}.

Four effects reduce C_{nom}: First, there is the DC bias voltage dependency which means that the capacitance value becomes lower if a DC bias voltage is applied across the capacitor. This is almost always the case since the capacitors are used as output or buffer capacitors in the converters. Fig. 17a shows measurement results of the DC bias dependency of a ceramic capacitor from the company muRata[23]. You can see that the capacitance value drops more than 15 % if a DC bias voltage of 3 V is applied.

[23] www.murata.com



(a) Simple circuit diagram of a capacitor with parasitics

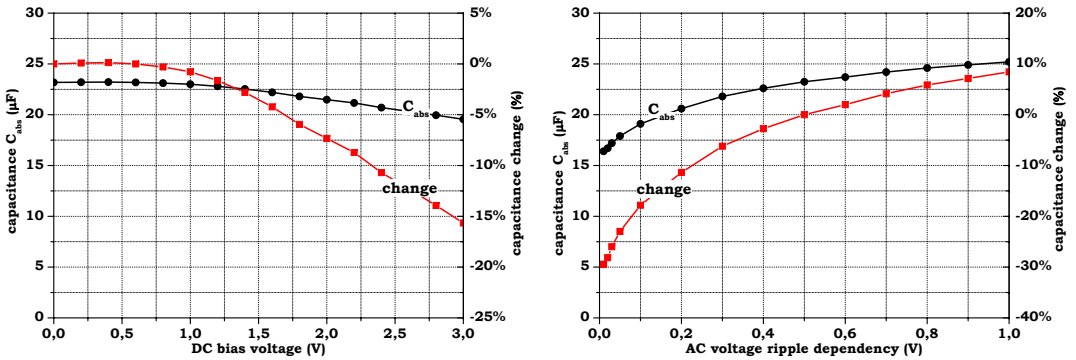
(b) Calculated voltage drops

Figure 16: Behaviour of a capacitor if a current ramp $i(t)$ is applied (Assumption: $C = 500\,\text{nF}$, $ESR = 25\,\text{m}\Omega$, $ESL = 5\,\text{nH}$)

Second, there is an AC ripple voltage dependency of the capacitance value. Fig. 17b shows that the capacitance value decreases for smaller AC ripple voltages. For the same capacitor from the company muRata as mentioned above it can be seen that the measured capacitance value C_{eff} is about 30 % lower than it is for C_{nom} if only a very small voltage ripple is applied. This is almost always the case in practice also, since only small input and output voltage ripples are typically allowed in applications.
Third, the temperature also affects the capacitance value. Ceramic capacitors have typically highest capacitance values around room temperature. For lower and higher temperatures the capacitance values drop.
The fourth effect that cause variations of C_{nom} is the normal process variations and ageing. The specified tolerances can be found in datasheets – typically they are in the range of $\pm 20\,\%$.
If all four effects are present in an application, C_{eff} of the used capacitor can be much lower than the specified nominal capacitance value C_{nom}.

4.2 Power switches

Power switches are used to control the power flow from the input to the output of the converters. Fig. 18 shows the two power paths with the current waveforms in an IB DC-DC buck converter operating in PWM-CCM. In phase



(a) DC bias dependency (Analyser: HP4192A+HP16047E)

(b) AC voltage ripple dependency (Analyser: Wayne Kerr 3260B)

Figure 17: Capacitance values of the capacitor GRM31CR61A226ME19 from the company muRata in different operating points. Nominal capacitance value C_{nom}: 22 μF.

1 (see Fig. 18a) the upper power switch M_P is switched on, therefore energy flows from the battery V_{Bat} over M_P through the power inductor L to the output of the converter. During this phase the current through the power switch M_P increases linearly (see Fig. 18c). In phase 2 M_P is switched off and the low side power switch M_N is switched on. The power path now goes through M_N as it can be seen in Fig. 18b and also from the current waveform in Fig 18c.

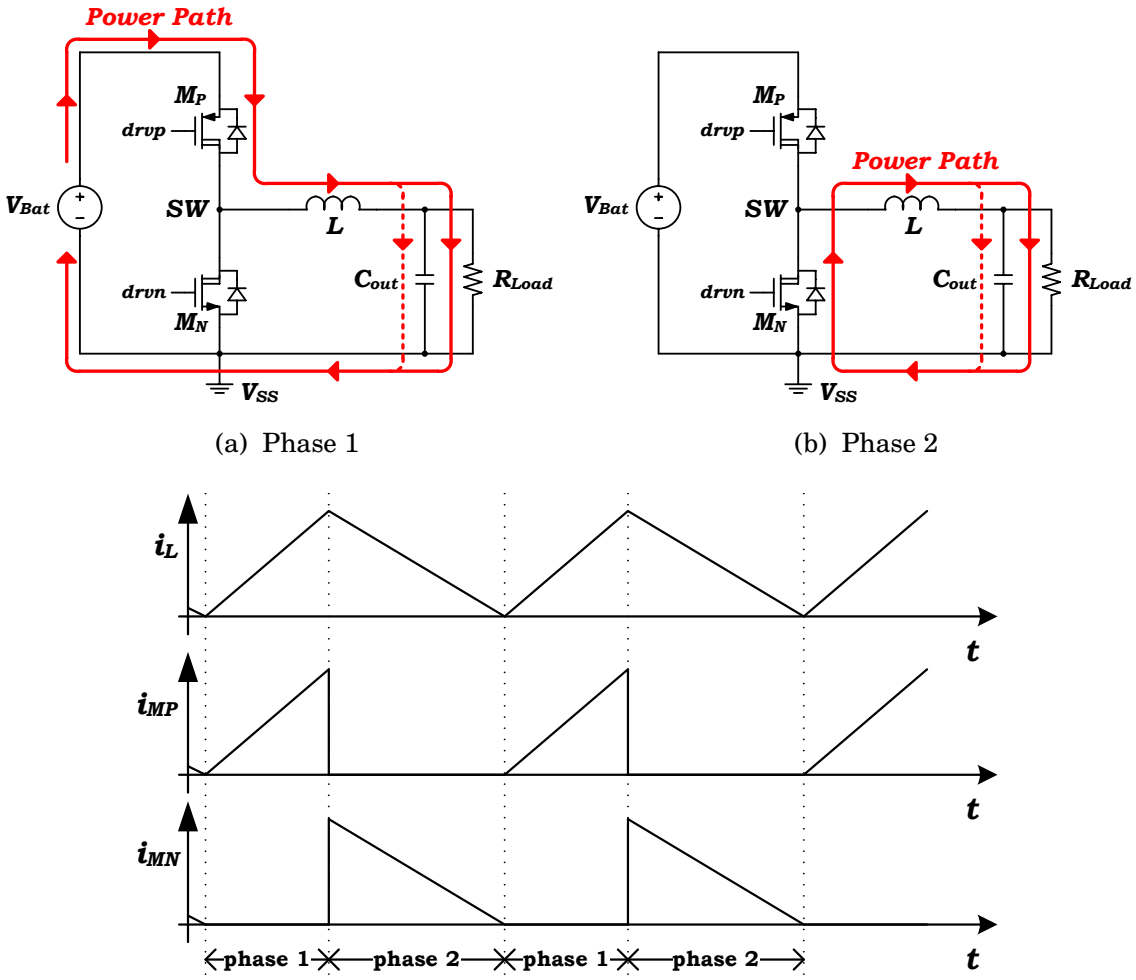
So it can be summarized that for a certain time exactly one power switch will draw the whole output current of the converter and that the power path is defined by the switch setting. Since the power switches always draw the full converter output current and since the power switches are responsible for the power path commutation, they are typically the largest loss contributor in IB DC-DC converters [14].

Three different loss types can be distinguished which should be discussed briefly.

Conduction losses

Conduction losses occur due to the finite on-resistance R_{on} of the power switches during their on-phase. The conduction losses can be estimated by using the following equation

$$P_{cond} = \frac{1}{t_{off} - t_{on}} \int_{t=t_{on}}^{t_{off}} I_{DS}^2(t) \cdot R_{on}(t)\, \mathrm{d}t \tag{28}$$



(a) Phase 1

(b) Phase 2

(c) Current waveforms through the power inductor and the power switches

Figure 18: Power paths in an IB DC-DC buck converter operating in PWM-CCM

where $R_{on}(t)$ is the time depended on-resistance of the power switch and $I_{DS}(t)$ is the current through the switch. For simple calculations $R_{on}(t)$ is often set to a constant value but for real power switches this of course is not a very accurate approach because it takes quite some time to completely switch on and off the power switches and thus R_{on} changes over time.
From Eq. 28 it can be recognized that in PWM-CCM the conduction losses are independent from the switching frequency of the converter since the ratio between the on and off times of the power switches during one switching period always remains the same for different switching frequencies.[24]

Gate drive losses

Gate drive losses occur due to charging and discharging the gates of the power switches. Since large switches have to be used in the output stage, also the parasitic gate capacitances are quite large. Therefore, strong gate drivers are required in order to be able to switch the power switches in a fast manner. Since the gate drivers are not lossless as well, their losses also have to be considered for the overall converter efficiency estimation.
Basically the gate drive losses of power switches can be calculated by

$$P_{gate} = Q_g \cdot V_{drv} \cdot f_{sw} \tag{29}$$

where Q_g is the required charge that charges the gate of the power switch to the desired gate source voltage V_{drv} and f_{sw} is the switching rate of the switch.
Especially if power switches with high gate-drain capacitors are used, the Miller effect can limit the switching speed of the devices drastically. In Fig. 19 the output stage of an IB DC-DC buck converter where the parasitic capacitances on the low side power switch M_N is shown. It can be seen that if the high side power switch M_P is switched off, M_N is connected in a common source configuration (see Fig. 19a). In this case Miller effect is present and the gate drain capacitor C_{GD} can be rearranged in an equivalent gate-source and drain-source capacitance as it is depicted in Fig. 19b. The equivalent gate-source capacitance is then given by $C_{GS} + C_{GD} \cdot (1 + |A|)$ which is of course typically much higher than the simple gate-source capacitance C_{GS} of the power switch (A is the small signal voltage gain of the output stage).
It is well known and also stated in Eq. 29 that gate drive losses in IB DC-DC converters increase with higher switching frequencies. For high frequency

[24] This of course is only valid in case of an ideal IB DC-DC converter without any losses.

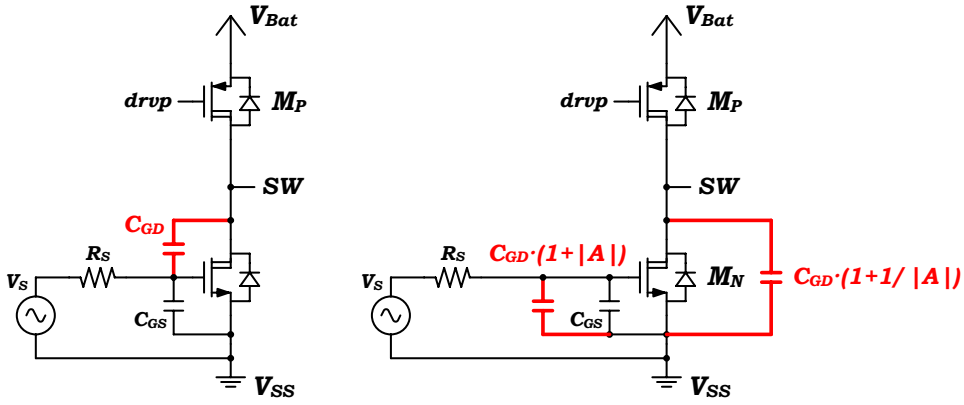


Figure 19: Miller effect on the power switches of an IB DC-DC buck converter

converters the gate drive losses are one of the major loss contributors in the converter.

Transition losses

Transition losses occur during commutation of the different current paths. There, losses arise because a current flows through the switch although a high transistor drain-source voltage V_{DS} is present at the same time. If we assume that the voltage and current waveforms are piecewise linear, the transition losses can be estimated by [13]:

$$P_{tr} = \frac{1}{2} V_{Bat} \cdot I_L \cdot t_d \frac{1}{f_{sw}} \quad . \tag{30}$$

There, V_{Bat} is the applied battery voltage, I_L the current through the power inductor at the transition, t_d the commutation time duration and f_{sw} is the switching frequency of the converter.

Different techniques are used to reduce transition losses. Very common techniques are zero-voltage switching (ZVS) and zero-current switching (ZCS). Often this techniques are called “soft switching” techniques[25] [64]. If these techniques cannot be implemented because of the used converter topology, then the only way to reduce the transition losses is to reduce the commutation time t_d.

Transition losses become critical in high frequency DC-DC converters because P_{tr} also depends on f_{sw}

[25] People talk about “hard switching” if ZVS and ZCS are not implemented.

dV/dt immunity

High dV/dt immunity guarantees that large and fast drain-source voltage changes at the power switches are not able to switch on the power switches due to the capacitive gate coupling. If the dV/dt immunity is low, then fast transients on the drain node of a power switch can raise the gate source voltage of the switch for a short time that means that the switch will be on for a short time [62]. If this happened in an output stage of an IB DC-DC converter, cross current would flow through the power switches that would reduce the converter efficiency immediately. Furthermore EMI problems can arise since large current spikes will occur at the converter input node.

Dimensioning the power switches

It is not possible to find power switch dimensions that are the optimum for all converter conditions. Typically, power conversion efficiency should be optimized – there the optimum power switch sizes depend on the performance of the switches itself[26] but it also depends on the operating mode of the converter[27]. Since the optimized power switch sizes depend on so many factors, an output stage can only be typically optimized for one converter condition. In order to achieve also almost optimized efficiency values for other operating conditions of the converter, the technique "output stage scaling" can be implemented [59]. There, segmented power switches are implemented which can be switched on and off independently or, in other words, the size of the power switches can be changed during the converter operation.

4.3 Switching time instants of the power switches

As discussed in section 4.2 power switches control the energy flow from the input to the output of the converter. They are switched on and off in a way that the output of the converter has the desired converter output voltage. In order to achieve high power conversion efficiency all the series resistances in the power paths have to be minimized. Therefore, power inductors and capacitors with lowest possible $\boldsymbol{ESR}$ should be used and power switches should have low on-resistances. Typically, on-resistances of on-chip power switches are in the range of some 100 mΩ. In DC-DC converters that use discrete power switches, the on-resistance of such switches can be much lower, of course.

[26] gate drive, transition and conduction losses

[27] input voltage, output voltage and switching frequency of the converter, PWM-DCM, PWM-CCM, load current, used power inductor

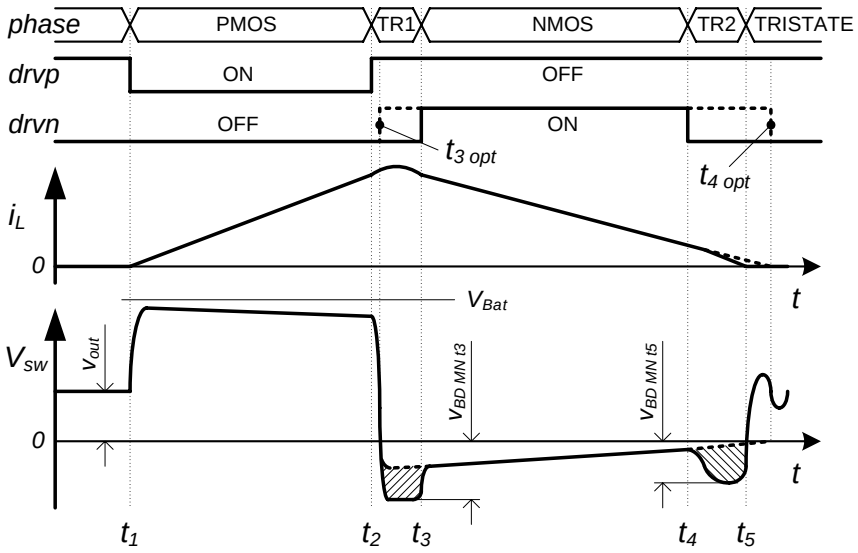


Figure 20: Typical signal waveforms of an IB DC-DC buck converter that operates in PWM-DCM [34].

One of the most critical tasks is now the commutation of the power paths. Fig. 20 shows typical signal waveforms of an IB DC-DC buck converter operating in PWM-DCM. Shown is the voltage waveform at the switching node V_{SW}, the current i_L through the power inductor and the control signals for the high side power switch $drvp$ and low side power switch $drvn$. In PWM-DCM there are the three main phases (PMOS, NMOS and TRISTATE phase) and two transition phases (TR1 and TR2 phase). In PMOS phase only the high side power switch is switched on, therefore V_{SW} goes up to almost the battery voltage V_{Bat}. In this phase the current i_L through the power inductor increases linearly. In NMOS phase only the low side power switch is switched on. That is why V_{SW} goes below the ground potential. And finally there is the TRISTATE phase where both power switches are switched off. In this phase, no current flows through the power inductor and therefore the voltage V_{SW} is equal to the output voltage V_{out} of the converter.
The two critical phases are now the two transition phases TR1 and TR2 where commutation between the main phases is done. At TR1 the converter switches from PMOS to NMOS phase. If the low side power switch is switched on too late, as it is depicted in Fig. 20, the current will flow for a short time through the parasitic body diode[28] of the power switches. This results in a

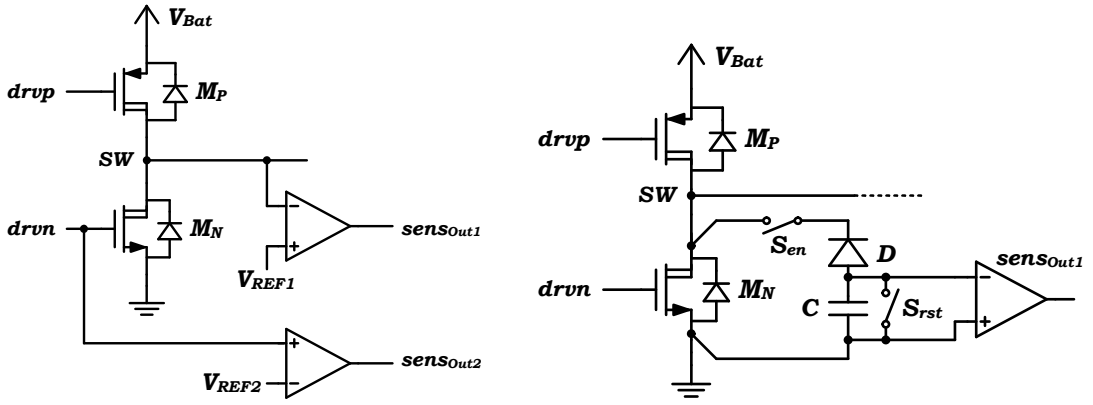
[28]The parasitic body diode is inherently present at the power switches if CMOS technology is used.

large voltage drop V_{BDMNt3} for a short time on the low side power switch that increases the conduction losses and therefore it reduces the converter efficiency.
Of course it also has to be guaranteed that the low side power switch is not switched on before the high side power switch is switched off. If this occurred, both low ohmic power switches are switched on at the same time which results in a large cross current flow. Let us assume that the applied battery voltage of the DC-DC converter is 5 V, the on-resistance of the high side power switch is 500 mΩ and the on-resistance of the low side power switch is 300 mΩ. Then 6.25 A will flow through the power switches from battery to ground if both switches are fully switched on at the same time. Since such a high current is not considered in the design of the converter, bond wires, metal connections and transistors can be destroyed. Another problem is that such high current peaks also reduce the EMC performance of the chip since blocking capacitors are typically not dimensioned for such high current spikes.
It can be seen from Fig. 20 that exactly one time instant for TR1 exists where commutation should be done: If it is done exactly at time instant t_{3opt}, no cross current will flow through the power switches and also no body diode conduction will occur. Therefore, conduction losses will be a minimum at this transition phase.
The same observation can be made during TR2 where the commutation between NMOS and TRISTATE phase is done: If the low side power switch is switched off exactly at the time instant t_{4opt} where the current i_L through the power inductor becomes zero, no body diode conduction will occur and therefore conduction losses will be a minimum.

How to find the optimum switching time instants of the power switches

In [34], [36], [15], [40] it has been shown that the converter efficiency drops immediately even if body diode conduction duration is a few nanoseconds. Furthermore, the situation becomes worse if the switching frequency of the converter is increased since the occurrence rate of body diode conduction directly scales with the switching frequency of the converter[29]. That is why the optimization of the switching time instants is mandatory especially in high frequency DC-DC converter designs. But optimization is not that easy, as

[29]Body diode conduction losses are conduction losses because they result from an ohmic voltage drop in the power path but they are also switching losses as they are directly proportional to the switching frequency of the converter.



(a) Typical approach for optimizing body diode conduction duration: using voltage comparators at the switching node and at the gate of the low side power switch.

(b) Proposed body diode conduction sensor for dead time optimization

Figure 21: Dead time optimization techniques

there are several challenges to solve. First, switching large power devices on and off within a nanosecond range is not easy since large gate capacitors have to be charged and discharged. It requires very strong gate drivers that can be controlled very accurately. Second, there are several different delays in the switching chain: Typically there are the delays of the logic gates in the digital controller that controls the power stage and there are the delays of the level-shifters and of the gate drivers. Third, the delays mentioned before are not constant over PVT so they can change a lot from sample to sample which makes it impossible to trim them. And fourth, the optimum switching time instants also depend on the applied input voltage, the output voltage and the load current of the converter.

A typical way to optimize the body diode conduction duration in a DC-DC buck converter is to sense the voltage on the switching node and the gate voltage of the low side power switch with a comparator, as shown in Fig. 21a. If the comparator on the switching node detects zero voltage crossing, the low side switch can be switched on. The second comparator, which is connected to the gate of the low side switch, is used to pre-charge the gate to the threshold voltage of the switch at the same time in order to reduce the remaining switch-on time delay. It has been shown that by using these optimization techniques quite good results can be achieved [38], [58].

But not all issues can be solved with this approach. There are always the

delays of the voltage comparators that vary over PVT. Also, very fast comparators have to be used in order to be able to reduce the remaining body diode conduction duration to values below 1 ns, for instance. Fast comparators are power hungry so we may ask if a maximum efficiency improvement of the converter can be achieved by using such a technique.
A method that overcomes these problems was developed during this PhD work. The key idea is to connect a negative peak voltage detector in parallel to the low side power switch (see Fig. 21b). The peak voltage detector consists of a diode D, a capacitor C and switches S_{en} and S_{rst} for controlling the sensor. Let us assume now that the capacitor C is completely discharged and that S_{en} is closed and S_{rst} is open. If body diode conduction will occurs during transition, current will flow through the parasitic body diode of M_N. In this case the voltage on the switching node SW will be much lower than the ground potential. Therefore, the diode D becomes conductive and the capacitor C will be charged. Now the nice thing is that the information, if body diode conduction has occurred or not, is stored in C. If there is no body diode conduction, the voltage across C is zero; if there is body diode conduction, C is charged and therefore the voltage across C is not zero. Once the information is stored in C the evaluation can be done with a slow medium accurate low power comparator that will not de-gradate the overall efficiency of the converter.
Three different operating modes are implemented in the sensor: In `reset mode` the capacitor C will be discharged which prepares the sensor for the next measurement cycle ($S_{en} = 0$ and $S_{rst} = 1$). In `sense mode` the sensor is ready to measure body diode conduction ($S_{en} = 1$ and $S_{rst} = 0$) and in `hold mode` the sensor is disconnected from the output stage and the information, which is stored in C, remains unchanged. In `hold mode` the evaluation of the stored information can be done with a voltage comparator. Since the information in C also remains unchanged over several switching cycles, a very slow low power comparator can be used to detect if body diode conduction has occurred or not.

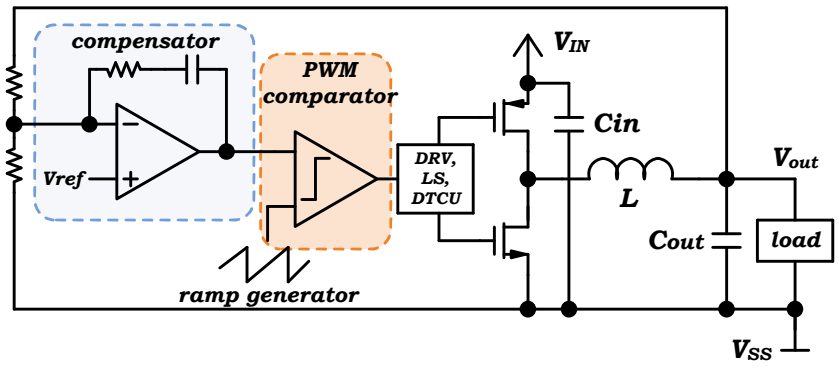
4.4 Controller

In general the controller keeps the output voltage of the converter as constant as possible for different applied input voltages, over PVT, for different loads and of course during the specified load jumps. A lot of different controller

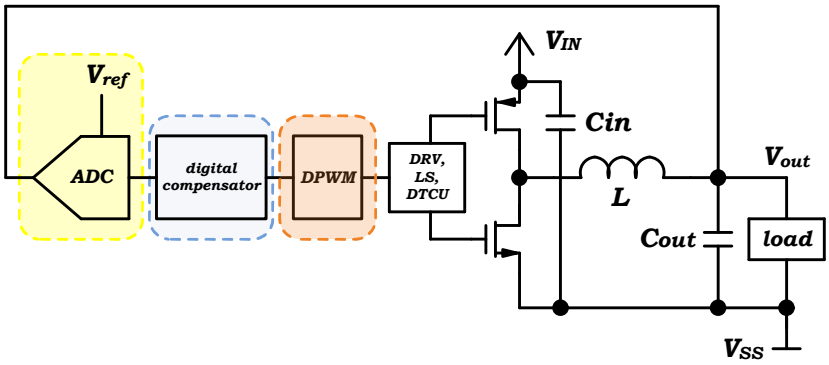
types have been published in literature. They are optimized for different converter types (e. g. buck, boost, flyback converter), for low or high power modes, for high power conversion efficiencies, for fast line and load regulation and so on. It is often not so trivial to find a controller, which is able to fulfil all of the specified targets. Also, it is not possible to find a controller that is the best choice for all different applications and that gives optimized results under all converter conditions. All of the controllers have advantages and disadvantages – now the challenging task is to find the most reasonable controller structure for a certain application out of the whole controller pool.
Although SMPS always change their steady state during operation the topologies can be modelled in small signal representations that allow making controller optimization and stability proof with well-known methods like Bode-Plots. In this section some basic aspects of controller design will be discussed briefly. The "Peak Current Control" method is discussed in a bit more detail as this control method is used in the designed IB DC-DC converter described in section 5 on page 65.

4.4.1 Digital vs. analogue controller

A very hot topic which popped up is the question if power conversion should be done with a digitally or an analogue controlled converter. Of course both controller types have the same goal: to provide high power conversion efficiency and to keep the output voltage as constant as possible during load jumps. But there are also fundamental differences that should be discussed briefly.
Fig. 22 shows the principle differences between digitally and analogue controlled DC-DC buck converters. In case of the analogue controller (see Fig. 22a) a continuous time compensator compares the scaled output voltage of the converter with a reference voltage V_{ref}. This error signal of the compensator is then used in a PWM block to generate the control signals for the power switches. Picture 22b shows the digital controlled counterpart: Since the controller operates in the digital domain an ADC converts the output voltage of the converter into a digital representation. From the output of the ADC a digital compensator calculates the digital actuating variable for the digital pulse width modulator (DPWM) that again generates the control signals for the power stage.
The main difference between the analogue and digital controller from the perspective of control theory is that in digitally controlled DC-DC converters there are discretization elements within the control loop. At the input



(a) analogue



(b) digital

Figure 22: Analogue versus digitally controlled IB DC-DC buck converter

there is an ADC that converts the output voltage of the converter to discrete digital values with a certain sampling frequency. This means that there is a discretization in time as well as in amplitude domain. Then the digital compensator calculates the digital actuating variable for the DAC with a constant frequency that is typically called DPWM in DC-DC converters. Since analogue controllers continuously operate without any discetization they generally show a better transient performance than digital controllers [47]. Analogue controllers can immediately react to input changes – so there is no sampling delay. Typically analogue controllers are able to control the output voltage of the converter with a much finer resolution since there is no discretization in the amplitude domain as it is in digital controllers.
Although analogue controllers have a lot of advantages and although they are well engineered there is the clear trend to go to digitally controlled DC-DC converters. The main advantage of the digital world is the flexibility: Designs can be easily ported to different technologies, they are absolutely stable over PVT and in the digital world a lot of features can be implemented with digital design tools in quite a convenient way. Implemented features are often digital calibration algorithms for reference circuits, monitor functions, frequency spreading operations, dynamic voltage scaling, digital dead time optimization, automatic adjustments of controller parameters in order to always have the optimized control loop for different operating modes (PWM-CCM, PWM-DCM, PFM, Feed-Forward compensation) and so on. Especially in very large integrated systems with complex PMUs, digitally controlled power conversion opens the opportunity to do very smart on-chip energy management. There, the different SMPS and linear voltage regulators can be switched into different modes depending on the loads and the conditions of the system.

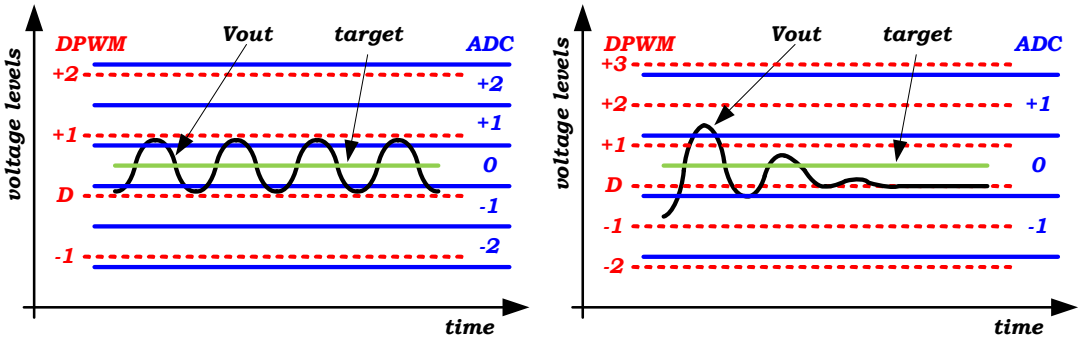
Limit Cycle Oscillation (LCO)
People are often afraid of limit cycle oscillation (LCO) – therefore it is a topic often discussed during concept and design phase. LCO is the output voltage oscillation in steady state due to the hysteresis in the digital loop (see Fig. 23a). LCO only occurs in digitally controlled systems. If an application has relaxed output voltage ripple constraints LCO can sometimes be accepted, since the amplitude of the oscillation is typically not very high. If LCO cannot be accepted, it can be avoided by using the following techniques.
The first method to avoid LCO is to increase the DPWM resolution so that it is higher than the ADC resolution [46]. This means that the following conditions have to be fulfilled: $\Delta V_{Out\_DPWM} < \Delta V_{ADC}$ with $\Delta V_{Out\_DPWM} = V_{IN} \cdot \Delta D$.

If the previous equation is satisfied, it is guaranteed that DPWM value always exists which generates an output voltage of the converter that is within the zero error bin of the ADC (see Fig. 23b). Therefore it is always possible for the output voltage to settle to a stable steady state voltage level (which corresponds to one DPWM value D) that is within the zero error bin of the ADC.
Especially for high frequency DC-DC converters, the implementation of low power high resolution DPWMs might be impractical. For instance, a counter based DPWM with 7bit resolution that should be used for an 80 MHz DC-DC converter would need a system clock of $2^n \cdot fs = 2^7 \cdot 80\,MHz \approx 10\,GHz$ which, of course, is not feasible. So it would be better to use other DPWM topologies like a delay line based DPWM or a hybrid DPWM that is a combination of a counter based DPWM for the coarse resolution and a delay line based DPWM for the fine resolution.
Another technique that can be used to increase the DPWM resolution and therefore to make it also suitable for high frequency DC-DC converters is to apply dithering [46] or $\Sigma\Delta-$modulation [30]. This is a very smart technique but is has to be considered that with this technique you cannot achieve the same small output voltage ripple of the converter than with "real" high resolution DPWMs.
Another technique to avoid LCO without increasing the DPWM resolution is to shift the target value of the output voltage exactly to a comparator's threshold in the ADC[30] [28]. This can be done simply by always adding 0.5 LSB to the output of the ADC. With this approach the output voltage always toggles between the comparator's thresholds around the zero error bin in steady state operation, as it is depicted in Fig. 23c. In order to achieve high static accuracy only this comparator in the ADC has to be designed with low offset.

4.4.2 Peak current controller for PWM-DCM operation

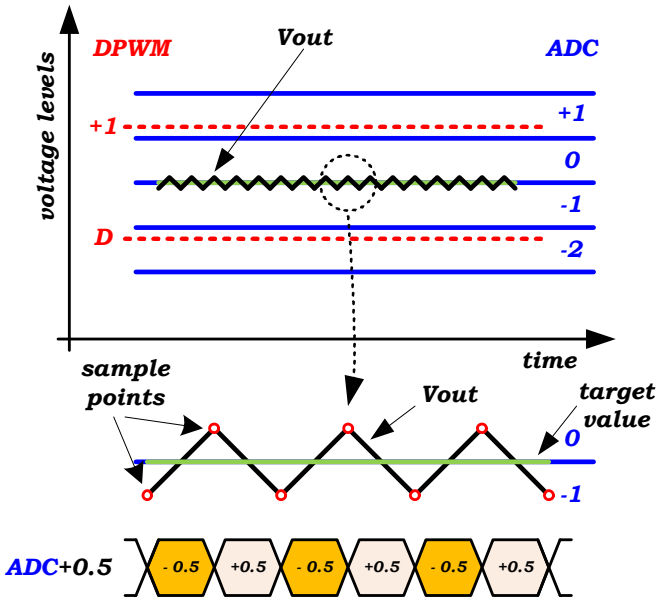
Since a peak current controller is used in the implemented IB DC-DC buck converter shown in section 5, this controller type will be discussed a bit more in detail.
For high light load power conversion efficiencies, two different controller strategies are common. The first one is the so-called Pulse Frequency Modulation (PFM) strategy: Charge packages with fixed energy are sent to the output of the converter with variable switching frequency. The resulting

[30]This technique uses a flash ADC to sample the converter output voltage.



(a) Limit cycle oscillation

(b) No limit cycle oscillation if $\Delta V_{Out\_DPWM} < \Delta V_{ADC}$



(c) No limit cycle oscillation by adding half of an LSB to the ADC output

Figure 23: Limit cycle oscillation in digitally controlled SMPS

switching frequency depends on the applied load current of the converter – if there is almost no load, the converter will switch with a very low frequency. Therefore, the switching losses will be low. If the load increases, the switching frequency will also increase. One problem of the PFM mode is that the switching frequency is never fixed and always changes depending on the load current. Therefore, the EMI performance of the SMPS is unpredictable and therefore PFM cannot be used in many designs.
Another controller strategy that provides high light load efficiency but also operates with synchronous switching frequency is the Pulse Width Modulation – Discontinuous Conduction Mode (PWM-DCM). In this thesis the focus will be on such a peak current controller for an IB DC-DC buck converter that operates in PWM-DCM since it is the controller type used in the designed converter shown in section 5 on page 65.
The basic idea behind this controller strategy is to send variable charge packages with a fixed switching frequency from the input to the output of the converter. Fig. 24 shows the current waveform I_L through the power inductor of these energy packages. It can be seen that the current waveforms are triangular and that they always start and end with zero current. The area within one triangle is the charge Q_{Pulse}, which is transferred from the input to the output of the converter during one switching cycle. The higher the load current of the converter is the higher the charge Q_{Pulse} is in one pulse. Q_{Pulse} can be controlled by changing Δt_1 which means that it can be controlled by varying the duty ratio of a squared wave signal (classical duty cycle control) or it can be controlled by the peak current threshold IU (peak current control).
In order to understand the behaviour and the limitations of the control method used, the dependency of the load of the IB DC-DC buck converter I_{Load} against the peak current value IU should be calculated.
The charge of one current pulse Q_{Pulse} is given by[31]

$$Q_{Pulse} = \frac{IU \cdot (\Delta t_1 + \Delta t_2)}{2} \tag{31}$$

where

$$\Delta t_1 = IU \cdot \frac{V_{in} - V_{out}}{L} \quad \text{and} \quad \Delta t_2 = IU \cdot \frac{V_{out}}{L} \ . \tag{32}$$

If this Q_{Pulse} occurs fsw-times during a time period $T_{Periode}$, the delivered

[31] All the calculations are without parasitics e. g. DCR of the power inductor, ESR of the capacitors, on-resistances of the power switches and so on.

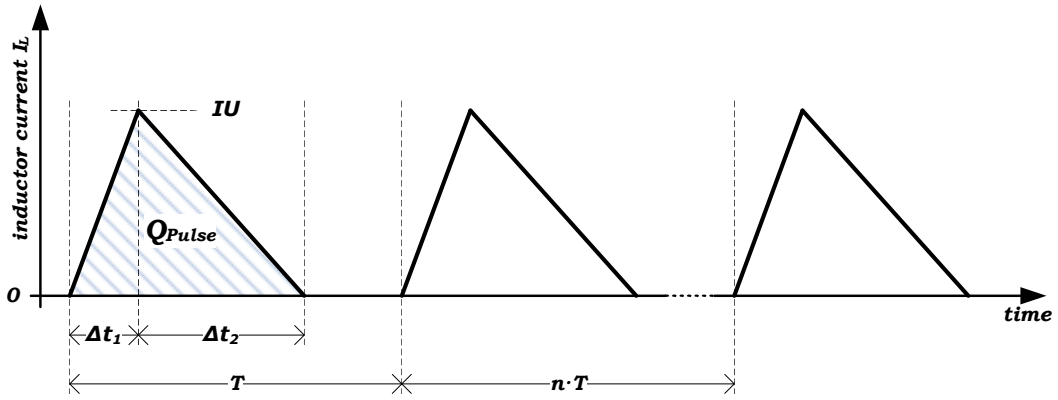


Figure 24: Current waveform of the coil current I_L in PWM-DCM

charge to the output can be calculated by combining Eq. 31 and Eq. 32:

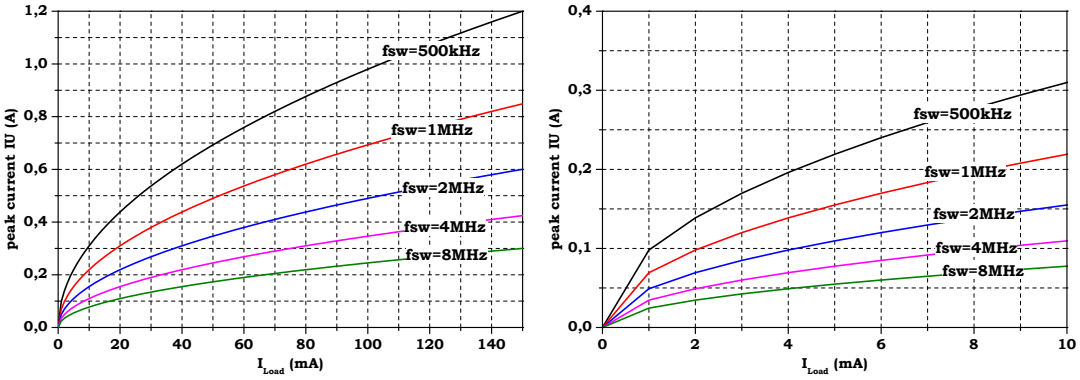
$$Q_{out} = I_{Load} \cdot T_{Periode} = IU^2 \cdot \left(\frac{1}{2 \cdot \frac{V_{in}-V_{out}}{L}} + \frac{1}{2 \cdot \frac{V_{out}}{L}} \right) \cdot fsw \cdot T_{Periode} \quad . \tag{33}$$

You get the required peak current IU for an IB DC-DC buck converter, which switches with a switching frequency fsw and should deliver a load current I_{Load} by rearranging Eq. 33 as follows:

$$IU = \sqrt{\frac{I_{Load}}{\left(\frac{1}{2 \cdot \frac{V_{in}-V_{out}}{L}} + \frac{1}{2 \cdot \frac{V_{out}}{L}} \right) \cdot fsw}} \quad . \tag{34}$$

Fig. 25 shows the graphical outputs of Eq. 34 where you can see the peak currents IU versus the load currents I_{Load} for different switching frequencies fsw. It should be noticed that in PWM-DCM the provided load current I_{Load} depends not only on the used peak current IU but also on the chosen switching frequency fsw. So there are two degrees of freedom in the design that allows controlling the output voltage of the converter[32]. For a chosen switching frequency $fsw = 500\,\text{kHz}$ and a load current of $I_{Load} = 150\,\text{mA}$ the required peak current IU would be 1.2 A. As this is a very large value for such a small output current, such a configuration is not practicable in a

[32]Here it is assumed that the input voltage V_{in}, the output voltage V_{out} and the inductance value L of the power inductor are all fixed values in a design.



(a) Full load current range (b) Zoom-in to very light loads

Figure 25: Peak current IU versus load current I_{Load} for an IB DC-DC buck converter in PWM-DCM and for different switching frequencies fsw

design. It is better to use a higher switching frequency e. g. $fsw = 8\,\text{MHz}$. In this case IU would be about 300 mA that is more reasonable.
We can conclude that if the converter should provide a wide load current range, it would be beneficial to adjust the switching frequency of the converter depending on the load. This guarantees that the peak current value IU never exceeds very high values which reduces the converter efficiency due to high RMS-values of the current waveforms and which might not be able to handle by the passives, by the power switches and by the power traces.

4.4.3 Stability analysis for a DC-DC buck converter operating in PWM-DCM

Stability analysis of DC-DC converters is typically done with analytical models. This allows using high-level tools like Matlab for analysing the plant with the implemented controller in open loop configuration. Control theory can be used to draw Bode-Plots that allows to printing the open loop transfer function of the design in a convenient graphical way. An equivalent circuit diagram in the s-domain of a peak current controlled IB DC-DC buck converter is shown in Fig. 26. It consists of the plant ($Plant(s)$) which is a small signal model of the converter operating in PWM-DCM; a current sense block ($current\_sens(s)$) which represents the transfer function of the high side power switch current sensing block; a voltage to current converter ($U\ to\ I(s)$) which converts the actuating variable from the controller into a current and

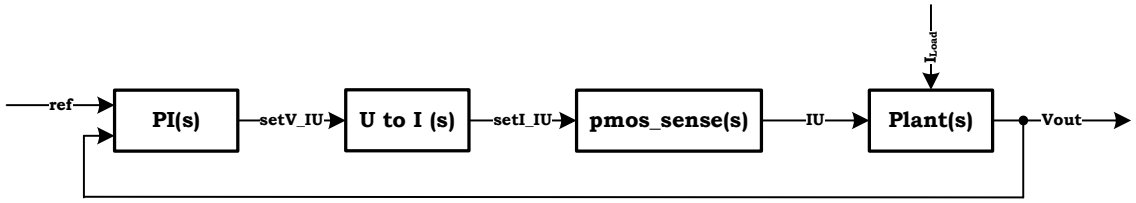


Figure 26: Equivalent circuit diagram of the peak current controller in the s-domain

finally the controller ($PI(s)$) which compares the output voltage of the converter with a reference voltage and sets the actuating variable $setV\_IU$, depending on the deviation of both voltages.
Nevertheless it has to be mentioned that analytical stability analysis can never replace transient large signal stability simulations with load steps since it is almost never possible to model several non-linear effects in the analytical described control loop. This means that after the optimization of a certain compensator in a small signal representation the stability of the design also has to be proved with transient simulations.

The Plant

The most complicated model of the whole converter is the plant because in PWM-DCM there are three different phases that have to be merged in order to get one model (see different phases in Fig. 20 on page 46). In the first phase, the high side power switch is switched on, in the second phase the high side power switch is switched off and the low side power switch is switched on, and in the third phase both switches are switched off.
A well-known approach for modelling converters is to use state space averaging [41]. There, the state space equations are linearised around the steady state operating points of the converter using small signal approximation – the description of the plant has then the following form that is well known in control theory:

$$\dot{x} = A \cdot x + b \cdot u \qquad y = c \cdot x + d \cdot u \tag{35}$$

or with the used state vectors

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} b_{11} & b_{12} \\ b_{21} & b_{22} \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ IU \end{bmatrix} \tag{36}$$

$$v_{out} = \begin{bmatrix} c_1 & c_2 \end{bmatrix} \cdot \begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} + \begin{bmatrix} d_1 & d_2 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ IU \end{bmatrix} \tag{37}$$

The corrected full-order model in [22] will be used as a starting point for the plant model of the IB DC-DC buck converter operating in PWM-DCM. The nice thing about this model is that it is also accurate for higher frequencies, e. g. above one-tenth of the switching frequency, and it also includes the most important parasitics in the power stage like the ESR of the output capacitor, the DCR of the power inductor and so on.
The corrected full order model for a DC-DC buck converter operating in PWM-DCM is given by [22]:

$$\dot{i_L} = \frac{d_1 \cdot v_{in}}{L} - \frac{2 \cdot i_L \cdot v_C \cdot r_b}{d_1 \cdot T_s \left(v_{in} - i_L \cdot \acute{r_a} - v_C \cdot r_b\right)} - \frac{i_L \cdot r_a}{L} \tag{38}$$

$$\dot{v_C} = \frac{i_L \cdot r_b}{C} - \frac{v_C \cdot r_b}{R \cdot C} \tag{39}$$

Since peak current control is used in the design the duty cycle d_1 in Eq. 38 has to be replaced by the peak current IU. By rearranging the equations in paper [22] the duty cycle d_1 can be expressed as

$$d_1 = \frac{IU \cdot L}{T_s} \frac{1}{v_{in} - i_L \cdot \acute{r_a} - v_C \cdot r_b} \ . \tag{40}$$

Substituting Eq. 40 into Eq. 38 gives the final corrected full-order model for the converter, where IU replaces the duty cycle d_1:

$$\dot{i_L} = \frac{v_{in} \cdot IU}{T_s \left(v_{in} - i_L \cdot \acute{r_a} - v_C \cdot r_b\right)} - \frac{2 \cdot i_L \cdot v_C \cdot r_b}{IU \cdot L} - \frac{i_L \cdot r_a}{L} \tag{41}$$

$$\dot{v_C} = \frac{i_L \cdot r_b}{C} - \frac{v_C \cdot r_b}{R \cdot C} \tag{42}$$

where $R = V_{out}/i_L$, $r_b = R/\left(R + r_C\right)$, $\acute{r_a} = r_L + r_S + r_C \cdot r_b$ and $r_a = d_1 \cdot r_S + r_L + r_C \cdot r_b$.
The model of Eq. 41 can now be used to calculate the small signal representation of the plant by calculating the total differential:

$$\dot{i_L} + \Delta i_L = \frac{\partial \dot{i_L}}{\partial i_L} \cdot \hat{i_L} + \frac{\partial \dot{i_L}}{\partial v_C} \cdot \hat{v_C} + \frac{\partial \dot{i_L}}{\partial v_{in}} \cdot \hat{v_{in}} + \frac{\partial \dot{i_L}}{\partial IU} \cdot \hat{IU} \tag{43}$$

$$\dot{v_C} + \Delta v_C = \frac{\partial \dot{v_C}}{\partial i_L} \cdot \hat{i_L} + \frac{\partial \dot{v_C}}{\partial v_C} \cdot \hat{v_C} + \frac{\partial \dot{v_C}}{\partial v_{in}} \cdot \hat{v_{in}} + \frac{\partial \dot{v_C}}{\partial IU} \cdot \hat{IU} \tag{44}$$

This way we can get the coefficients of the model in Eq. 36. The coefficients for the small signal representation of the plant of an IB DC-DC buck converter operating PWM-DCM with peak current control are then given by

$$a_{11} = \frac{-v_{in} \cdot IU \cdot (-T_s \cdot r_a')}{\left[T_s \cdot (v_{in} - i_L \cdot r_a' - v_C \cdot r_b)\right]^2} - \frac{2 \cdot v_C \cdot r_b}{IU \cdot L} - \frac{r_a}{L} \tag{45}$$

$$a_{12} = \frac{-v_{in} \cdot IU \cdot (-T_s \cdot r_b)}{\left[T_s \cdot (v_{in} - i_L \cdot r_a' - v_C \cdot r_b)\right]^2} - \frac{2 \cdot i_L \cdot r_b}{IU \cdot L} \tag{46}$$

$$a_{21} = \frac{r_b}{C} \tag{47}$$

$$a_{22} = \frac{-r_b}{R \cdot C} \tag{48}$$

$$b_{11} = \frac{IU - v_{in} \cdot IU \cdot T_s}{\left[T_s \cdot (v_{in} - i_L \cdot r_a' - v_C \cdot r_b)\right]^2} \tag{49}$$

$$b_{12} = \frac{v_{in}}{T_s \cdot (v_{in} - i_L \cdot r_a' - v_C \cdot r_b)} - \frac{-2 \cdot i_L \cdot v_c \cdot r_b \cdot L}{(IU \cdot L)^2} \tag{50}$$

$$b_{21} = 0,\ b_{22} = 0 \tag{51}$$

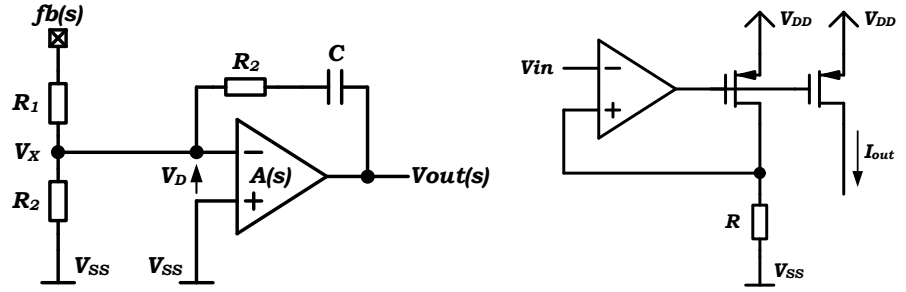
$$c_0 = 0,\ c_1 = 1,\ d_0 = 0,\ d_1 = 0 \tag{52}$$

From the state space model of the plant the transfer function $Plant(s)$ can be calculated by using the following relation found in textbooks:

$$Plant(s) = c\,(sE - A)^{-1}\,b + d\ . \tag{53}$$

Proportional-Integral (PI) controller and voltage to current converter

Fig. 27a shows a PI controller that can be used as a controller in the peak current controlled IB DC-DC buck converter operating in PWM-DCM. On the input a voltage divider is used to scale down the feedback voltage fb of the converter to a voltage V_X. This voltage can be handled with the transistors used in the core voltage domain of the converter. An operational amplifier with an RC-feedback network performs the PI behaviour of the controller.



(a) PI controller with voltage divider at the input

(b) Voltage to current converter

Figure 27: Topology of PI controller and voltage to current converter

From Kirchhoff's first law we get

$$\frac{V_{fb} + V_D}{R_1} + \frac{V_D}{R_0} + \frac{V_{out} + V_D}{R_2 + \frac{1}{s \cdot C}} = 0 \quad . \tag{54}$$

If we use a simplified transfer function $A_D(s)$ for the operational amplifier with only one pole at the frequency ω_g

$$A_D(s) = \frac{A_0}{\frac{s}{\omega_g} + 1} \tag{55}$$

and if the voltage difference V_D between the positive and negative input pin of the operational amplifier is

$$V_D = \frac{V_{out}}{A_0} \tag{56}$$

where A_0 is the open loop gain and ω_g is the bandwidth of the amplifier, the transfer function of the PI-controller including the voltage divider on the input is

$$PI\,(s) = \frac{V_{out}(s)}{fb(s)} = \frac{A_D(s)}{R_1} \cdot \frac{1}{-\frac{1}{R_0} - \frac{1}{R_1} - \frac{A_D(s)+1}{R_2 + \frac{1}{s \cdot C}}} \quad . \tag{57}$$

The transfer function typically has one pole at a low frequency (due to the limited gain of the operational amplifier), a pole at a high frequency (due to the limit gain bandwidth of the operational amplifier) and a zero between the two poles (given by the RC-feedback network of the operational amplifier).

Let's have a look now at the transfer function of the voltage-to-current converter. If the bandwidth of the operational amplifier for the voltage-to-current converter in Fig. 27b is much higher than the bandwidth of the PI controller, a simplified transfer function with constant gain can be used. The amplifier regulates the voltage across the resistor R to the voltage value V_{in}. Therefore the current through this resistor is $I = V_{in}/R$. If both PMOS transistors have equal sizes[33], the simplified transfer function of the voltage-to-current converter is

$$UtoI\,(s) = \frac{I_{out}}{V_{in}} = \frac{1}{R} \quad . \tag{58}$$

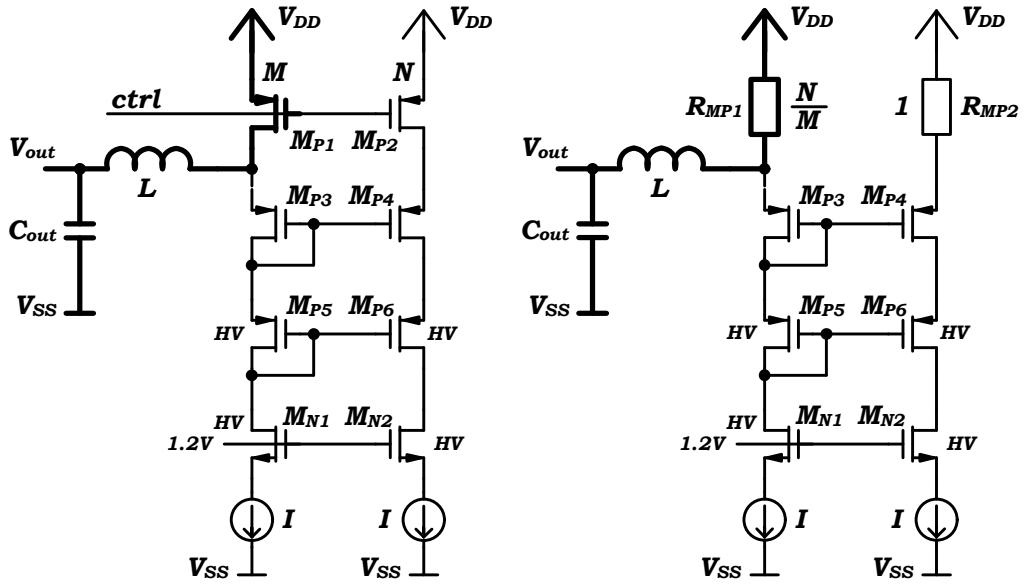
High side power switch current sense

For peak current control it is required to measure the peak currents flowing in the power paths. The easiest way is to put a small sense-resistor into the power path. This allows measuring the current flow via the voltage drop on the sense-resistor by using voltage comparators. The biggest disadvantage of this method is the high power dissipation in the sense-resistor, which reduces the overall power conversion efficiency of the converter. So it is preferable to use other sensing techniques with very low power dissipation also for heavy loads. A nice summary of existing current sense techniques used in IB DC-DC buck converter designs can be found in [45]. Especially for integrated power switches it is a common sense technique to use a small sense-FET that is connected in parallel to the power switch [45], [9], [8], [42]. The current flow through the power switch can be evaluated from the difference of the on-resistance of both switches during the on-phase.

Fig. 28a shows the used topology for sensing the current flow through the high side power switch M_{P1} during the on-phase. There, M_{P1} is the M-times placed unity power switch and M_{P2} is the N-times placed sense-FET. If the switches M_{P1} and M_{P2} are switched on, they are low ohmic and therefore they are in the triode region that can simply be represented as resistors in steady state operation (see Fig. 28b). Since only scaled unity transistors are used, the resistance of R_{MP1} is smaller by the factor N/M.

The voltage drops across R_{MP1} and R_{MP2} can be calculated by using the

[33] This means that a $1:1$ current mirror is used



(a) Current sensing with sense-FET

(b) Current sensing with sense-FET – switches are exchanged by resistors during the on-phase.

Figure 28: Current sensing of high side switch used for the peak current control

Kirchhoff's laws

$$V_{RMP1} = \frac{N}{M} \cdot (I_L + I) \quad \text{and} \quad V_{RMP1} = 1 \cdot I \tag{59}$$

where I_L is the current through the power inductor and I is a small current that is used to bias the sense circuit.
R_{MP3} and R_{MP4} perform a common gate amplifier, which senses the drain voltages of R_{MP1} and R_{MP2}. The circuit detects the point where both drain voltages are equal. The resulting simplified transfer function of the high side power switch sense circuit is then given by

$$pmos\_sense\,(s) = \frac{I_L}{I} = \frac{M - N}{N} \quad . \tag{60}$$

The complete open loop transfer function

The complete open loop transfer function of the DC-DC buck converter operating in PWM-DCM now can be calculated by multiplying all the single transfer

functions developed in this section:

$$\boldsymbol{G}(s)_{ol} = \boldsymbol{PI}(s) \cdot \boldsymbol{UtoI}(s) \cdot \boldsymbol{pmos\_sense}(s) \cdot \boldsymbol{Plant}(s) \tag{61}$$

5 IB DC-DC buck converter for portable applications

The IB DC-DC buck converter which has been designed during this PhD work will be discussed in this chapter. The implemented converter can be used as a replacement for linear voltage regulators in large integrated circuits. For instance, there are reports that a non-DC-DC power supply concept would increase the average battery current of about 17 % for a GSM baseband-radio with a fully integrated PMU [18]. If only one DC-DC converter is used in the PMU, about 17 % of battery current can be saved.
Since a lot of different voltage domains are required in such huge systems the PMUs typically consist of several voltage converters. Especially in ultra-low-cost phones the majority of the voltage converters are of linear type for cost saving reasons [17], [18]. Therefore, the power conversion efficiency can be improved a lot if most of the linear voltage regulators are replaced by high efficient SMPS.
The first target of this thesis was to develop a suitable concept for an IB DC-DC that can be used as a replacement for linear voltage regulators. The second target of the thesis was to implement the developed concept in a 65 nm low power CMOS technology.
In order to be competitive to linear voltage regulators, the IB DC-DC converter should achieve much higher power conversion efficiencies over the full load range; the occupied chip area should be in the same order as it is for linear voltage regulators and components with small form factors should be used for the input and output filter.
Additional requirements that are given by the application are the fixed 1.2 V output voltage of the converter and the opportunity to connect the converter directly to Li-Ion batteries. Since most of the linear voltage regulators, which the designed buck converter should replace, are designed for light load currents, the converter should achieve high power conversion efficiencies especially at light load.

5.1 The converter concept – the top level

This section will give a brief overview of the implemented blocks of the IB DC-DC buck converter.
The converter uses an analogue peak current controller with synchronous

switching frequency. Automatic frequency hopping with fixed frequency values is implemented in order to provide high power conversion efficiencies over a wide load range. Furthermore the converter supports a pulse skipping mode which allows loads down to 0 mA. The used analogue peak current controller concept for PWM-DCM operation has been discussed in detail in section 4.4.2 on page 53.
In order to get optimized switching time instants of the power switches an automatic body diode conduction duration optimization concept was developed for the converter. The implemented concept has been discussed in section 4.3 on page 45.
A digital interface is used in order to adjust internal converter settings e. g. to enable or disable complete building blocks, to change the output voltage and to enable or disable certain control algorithms. The master digital state machine does the overall control of the blocks.
Fig. 29 now shows the simplified top-level topology of the converter. The different building blocks implemented in the design are shown in a hierarchical manner in Fig. 30. Two blocks shown with dashed border lines were taken from existing designs: The first one is a reference block (**`reference_block`**) which generates programmable reference currents and reference voltages and the second one is the digital interface (**`fcsi`**) which is used to communicate with the chip and to program the chip.
Basically, the converter can be divided into four main parts. These parts should be explained in a bit more detail.

dcdc_ana:
The first part is the **`dcdc_ana`** block (shown in green in Fig. 29) – it consists of the output stage of the converter with the high side and low side power switch; the driver for the power switches (**`dcdc_ana_driver`**) and the level shifters (**`LVSH`** and **`LVSL`**) which are used to convert the signals coming from the digital controller build in the core voltage domain to the power domain. Furthermore, a bias block **`bias`** is implemented to generate the driver voltages of the stacked power switches. Additionally a snubber circuit **`snubber`** is implemented for damping high frequent voltage ringing on the switching node. Otherwise, large ringing on the switching node will occur if the power stage is switched to tristate (this is always the case in PWM-DCM, see section 4.4.2 on page 53). The frequency of the voltage ringing is determined by the series LC tank composed of the parasitic capacitor on the switching node

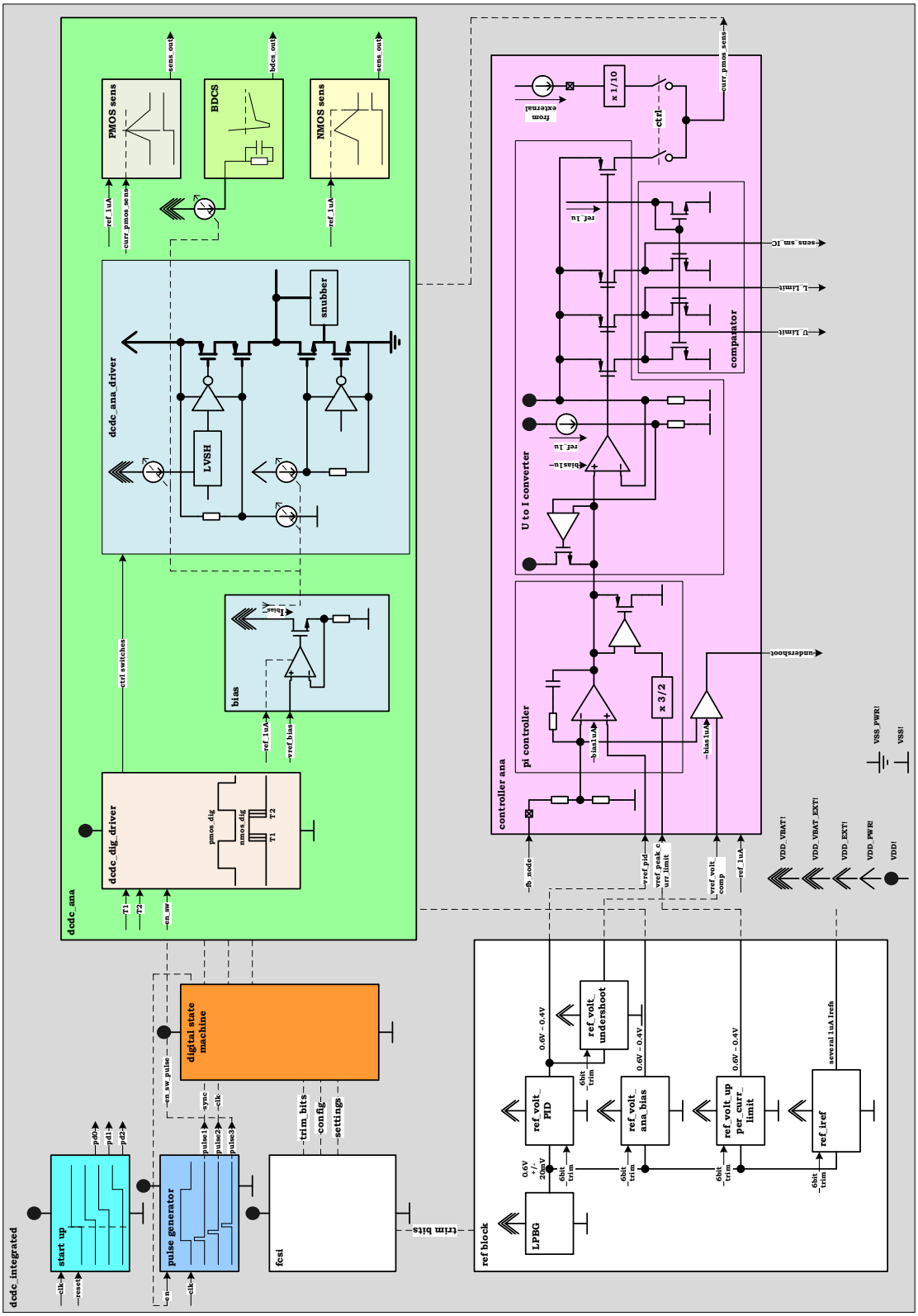


Figure 29: Simplified top-level schematic

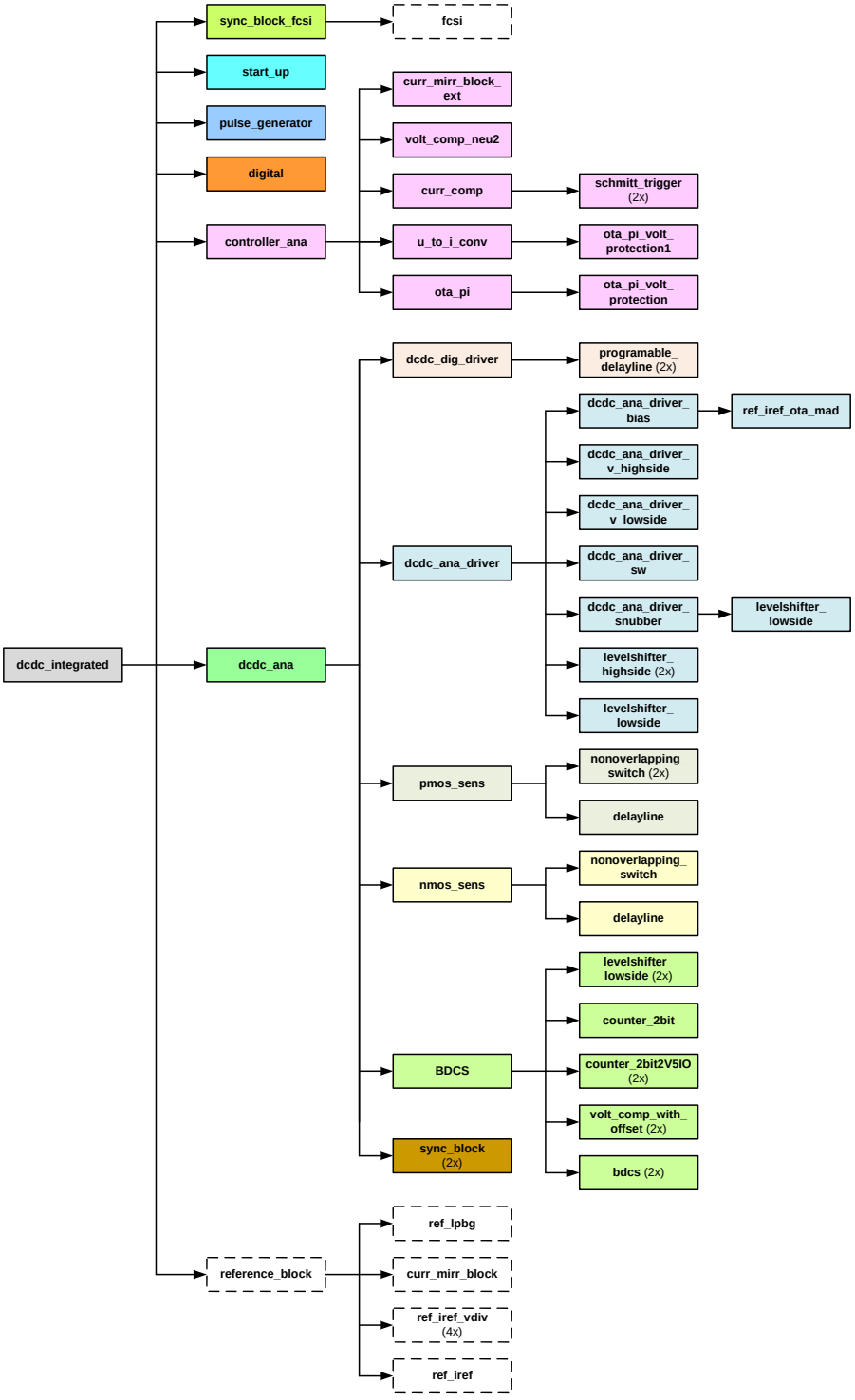


Figure 30: Hierarchical structure of the blocks

and the power inductor of the output filter.
Also implemented are current sensing blocks that measure the current through the high side (**PMOS sens**) and low side (**NMOS sens**) power switch. The current information of the high side power switch is used for controlling the converter (peak current controller). Furthermore, it is used to implement an over current protection functionality.
The current information of the low side power switch is used for detecting the zero current crossing point of the power inductor current. After zero current is detected, the converter switches to tristate.
Another important block in the **dcdc_ana** part is the body diode conduction sensor (**BDCS**). The sensor is used to measure the body diode conduction duration during the commutation phases of the power stage. The information of the $BDCS$ is used in the finite state machine to optimize the switching time instants of the power switches during normal converter operation (see section 4.3 on page 45).
Finally, a full custom analogue state machine (**dcdc_dig_driver**) generates the digital switching sequences of the power switches. Furthermore, the block generates the programmable dead times of the power stage of the converter with asynchronous down counters connected to a 2 GHz ring oscillator. More details about this block can be found in my publication [36].

controller ana:
The second part is the controller (**controller ana**). A peak current control concept with PI controller (**pi controller**) is used for the control strategy. The PI controller is connected to a resistive voltage divider which scales down the 1.2 V output voltage (feedback voltage)of the converter to 0.5 V that can be handled internally in a more convenient way. The output of the PI controller is connected to a voltage to current converter (**U to I converter**) – the generated output current is then the actuating variable of the regulation loop: It controls the peak current through the power inductor of the output filter.
Since the output current of the voltage to current converter is a direct replica of the peak current through the power inductor, this current can also be used to implement over current protection functionality.
Last but not least the current is also used for the implementation of the automatic frequency-hopping concept. The current is used to detect different peak current thresholds through the power inductor. This allows adjusting the switching frequency of the converter depending on the load values of the

converter. If there is a low load current, the switching frequency of the converter will be reduced. If the load current is high, the switching frequency will be increased which subsequently decreases the peak current through the power inductor (see more details in section 4.4.2 on page 53). The different current thresholds are measured with the current comparators **comparator**. Also included in the controller block is a voltage comparator that is used for under-voltage detection of output voltage of the converter (emergency feature). An under-voltage scenario could occur if heavy load jumps are applied to the converter. The information of the under-voltage comparator output is used in the digital state machine to change the controller parameters immediately (e. g. the switching frequency of the converter will be increased).
Finally, also a bypass mode is implemented in the controller which allows setting the actuating variable of the converter to a certain value by an external reference current. This mode can be used to debug the controller behaviour and to check the thresholds of the high side current sense block.

ref block and fcsi:
The reference block **ref block** generates all reference voltages and reference currents that are required for the analogue blocks. All reference voltages and currents are programmable, so they can be adjusted by programming internal values of the finite state machine. This allows changing a lot of different converter settings like the target output voltage of the converter (**ref_volt_PID**) or the under-voltage detection threshold.
A digital interface **fcsi** is used for the chip communication.

digital:
A digital state machine is used to control the overall behaviour of the converter. The state machine enables digital blocks, it automatically changes the switching frequency depending on the load (frequency hopping), it evaluates the results from the body diode conduction sensor and it changes the digital settings for switching time instants of the power switches. Furthermore, it is used to multiplex debug signals to the debug pins.
Short pulses generated by a pulse generator block (**pulse generator**) clock the digital state machine. The pulse generator takes the external clk signal and generates three short pulses with short delays out of the external clock signal: The first pulse is used for the synchronization of the analogue blocks with the digital state machine. This should avoid metastability at the input

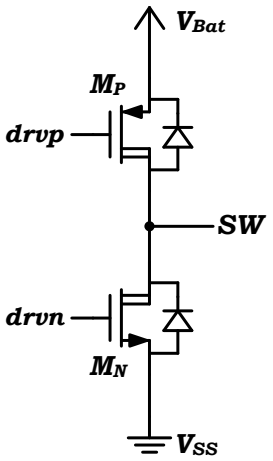
signals of the digital state machine connected to analogue signals. The first pulse clocks two in series connected master-slave flipflops, whereas the first flipflop is sensitive to the rising edge and the second flipflop is sensitive to the falling edge of the first pulse.
The second pulse is the clock input signal for the finite stage machine and the third pulse is used to start a switching cycle of the converter. The nice thing about this these implementation is that three steps are done within one clock cycle of the external clock: synchronisation, finite state machine execution and starting a switching cycle of the converter. Therefore, an external clock with the same low clock frequency as the converter switching frequency can be used.
Finally a start-up block (**`start up`**) is implemented which guarantees safe start-up behaviour of the chip.
In the next section the most important blocks will be discussed a bit in more detail.

5.2 Output stage

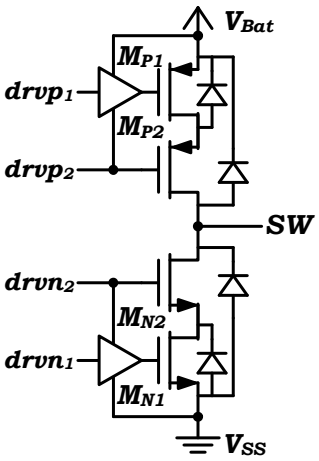
The output stage consists of the power switches that control the power flow from the input to the output of the converter. In our case the output stage has to withstand a voltage of up to 5 V since it is directly connected to the battery. Therefore also the used power switches have to withstand such a high drain-source voltage. In the used 65 nm CMOS process, thin oxide DeMOS[34] transistors are available which are able to withstand 5 V drain-source voltage inherently. So the natural approach to build the output stage is to use p-DeMOS devices for the high side power switch and n-DeMOS devices for the low side power switches as it is depicted in Fig. 31a.
Another approach which can be used to get 5 V capability of the output stage is to use stacked power switches as it is depicted in Fig. 31b [2], [54], [24]. There, the low side power switch is composed of two 2.5 V IO-NMOS[35] devices and the high side switch is composed of two 2.5 V IO-PMOS devices. By a proper setting of the bias voltages $drvp_2$ and $drvn_2$ it can be guaranteed that the drain source voltages of all of the transistors never exceed the allowed

[34] Drain-Extended lateral MOS transistor with $V_{DSmax} = 5\,\mathrm{V}$ and $V_{GSmax} = 1.2\,\mathrm{V}$

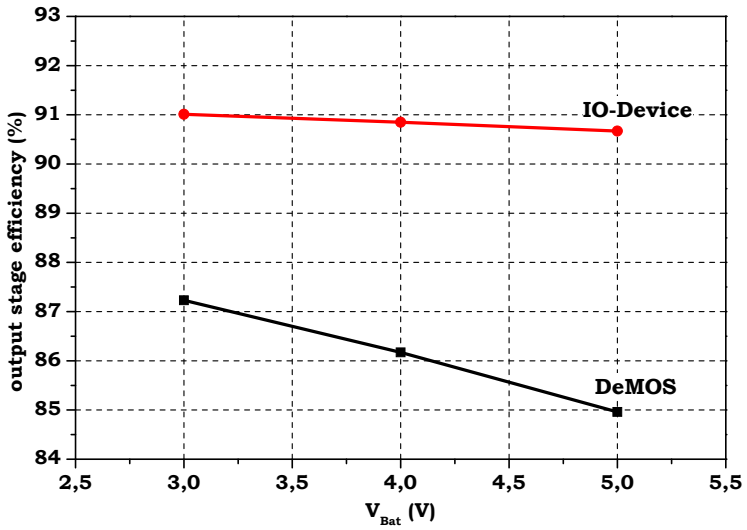
[35] IO devices: Thick gate MOS devices that are available for three different drain source voltage classes: $V_{DSmax} = 1.8\,\mathrm{V}$, $V_{DSmax} = 2.5\,\mathrm{V}$ or $V_{DSmax} = 3.3\,\mathrm{V}$ and $V_{GSmax} = 4.2\,\mathrm{V}$



(a) Power stage with 5 V DeMOS devices



(b) Power stage with stacked 2.5 V IO devices



(c) Power conversion efficiencies for both power stage topologies of Fig. 31a and Fig. 31b used for an IB DC-DC buck converter

Figure 31: Power stage topologies and power conversion efficiencies for IB DC-DC buck converters with input voltages of up to 5 V

2.5 V drain-source voltage[36]. To switch the power switches on and off only the transistors M_{P1} and M_{N1} have to be switched on and off – M_{P2} and M_{N2} can be biased with constant voltages $drvp_2$ and $drvn_2$.
In my paper "Output stage topologies of DC-DC buck converters operating up to 5 V supply voltage in 65 nm CMOS" [35], you can see that a stacked transistor approach, as it is depicted in Fig. 31b, shows a better performance in terms of power conversion efficiency than the conventional approach with the DeMOS power switches for the used technology. Fig. 31c shows simulation results of the power conversion efficiency of both output stage topologies depicted in Fig. 31a and Fig. 31b for different battery voltages V_{Bat}. The output stage was used for an IB DC-DC buck converter operating with a switching frequency of 5 MHz. The output voltage of the converter was 1.2 V and the output current was set to 100 mA; for the output filter a 2 μH power inductor and a 10 μF capacitor where used. In order to get comparable simulation setups both output stages are designed to have the same DC on-resistances for the high side and low side power switch, respectively.
The simulation results in Fig. 31c show that the power conversion efficiency is 4 % better at a battery voltage of 3 V if stacked IO-devices are used in the power stage instead of the conventional DeMOS devices. The main reason for the worse performance of the DeMOS devices is because of the large gate-drain capacitor that is present because of the drift region of the devices. Since this gate-drain capacitor is further increased by the Miller-effect (see chapter 4.2 on page 43), switching on and off the DeMOS devices in a fast, power efficient and accurate way is difficult. However the IO devices are symmetric devices without drift region, therefore only the small gate-drain overlap capacitors are present which allow to switch these devices in a more power efficient way.
It also has to be mentioned that in existing publications the bias voltage nodes $drvp_2$ and $drvn_2$ are typically connected together [24]. Of course this has the advantage that only one bias voltage generation circuit and one buffer capacitor is needed but we have shown that this results in a strong input voltage dependency of the converter efficiency since the over drive voltage of the power switches change with respect to the battery voltage.
In the paper [35] the most important loss contributors of the power switches

[36] Of course this is only valid in steady state operation – the voltage can exceed the allowed voltage for a short time in case of voltage ringing on the power traces due to parasitic inductances in the loops

are also discussed. Simple simulation setups are shown to evaluate the amount of the different loss contributors. This allows to comparing different devices in terms of their switching performance. From these results you can select the best-suited device for an output stage in a given technology.

5.3 Gate drivers for the power switches

In order to achieve a high power conversion efficiency of the converter the power switches have to be switched very fast and accurately for lowest transition losses during current commutation and for minimized body diode conduction durations respectively. Strong gate drivers do the switching of the power switches.
The gate driver block is completely controlled by digital signals coming from the 1.2 V core power domain. This allows you to do all the trimming activities and the optimization of the switching time instants of the power switches in the digital state machine.
One of the most important issues in the gate driver design is reliability. The gate drivers have to be designed in such a way that it never happens that both power switches are switched on at the same time. If this occurred, a disallowed large crosscurrent would directly flow from one battery terminal to the battery ground terminal. Second, the gate drivers have to work very reliably in the rough environment. Due to parasitic inductances in the power traces large voltage ringing can occur at the power switches – for instance in the designed IB DC-DC converter test chip we got ringing up to $\pm$ 1.5 V with a frequency of about hundred megahertz. Therefore, the gate driver block has to be of such robust design that it always operates in the correct way. Third, the gate driver block has to generate the bias voltages for the stacked power switches. Since a stacked transistor approach is used to limit the voltage drops on each transistor the right bias voltages have to be generated during normal converter operation, but they also have to be generated in power down mode because the converter typically is also connected to the battery voltage during power down.
Fig. 32 now shows the simplified schematic of the implemented gate driver circuit that also includes the bias voltage generation of the stacked power switches. M_{P1-2} is the stacked high side power switch and M_{N1-2} is the stacked low side power switch. Since identical gate driver topologies are used for the high and low side power switch, the functionality of the gate driver

block is discussed by means of the part of the gate driver responsible for the low side power switch.
Let's assume that the generated bias voltage $drvn_2$ of the stacked transistor M_{N2} is 2.8 V, the applied battery voltage V_{Bat} is 4 V[37] and that $drvn_1$ is switched to V_{SS_PWR} which means that the low side power switch is switched off. If the high side power switch is switched on, the switching node SW will be approximately V_{Bat}, because there is a very low ohmic path from SW to V_{Bat}. In this case M_{N2} shields M_{N1} against a drain-source voltage that is too high. M_{N1} has on the drain node only the bias voltage $drvn_2 = 2.8$ V minus the threshold voltage of M_{N2} which is about 400 mV on the drain node. This gives us the drain-source voltages of M_{N2} and M_{N1} that is 1.6 V and 2.4 V, respectively. Of course if the low side power switch is switched off, both drain-source voltages of the transistors are below the allowed 2.5 V, since the SW will be approximately V_{SS_PWR}.
The low side power switch will be switched on by driving the gate of M_{N1} up to the bias voltage $drvn_2$. This is done by means of tapered buffers[38] that are controlled by the low-side level shifter $LVSL$. This level shifter shifts the digital control signal n_{dig} coming from the controller in the core power domain (1.2 V digital domain) to the power domain $drvn_2$ and V_{SS_PWR} of the output stage. The tapered buffers are connected to $drvn_2$. This means that both transistors M_{N1} and M_{N2} of the low-side power switch have the same overdrive voltage during the on state.
It should also be mentioned that the drain voltage of M_{N1} can never exceed the bias voltage $drvn_2$ minus V_{th_MN2} during off state if the same transistor types with the same transistor sizes are used for M_{N1} and M_{N2} since both bulks of the transistors are connected to V_{SS_PWR}. The sub-threshold leakage of M_{N2} is always lower than it is for M_{N1} due to the back gate effect that it is guaranteed in this case.
Next, the bias voltage generation for the stacked transistor M_{N2} will be explained. It should be mentioned that the tapered buffers are directly connected to this bias voltage at node $drvn_2$ so the whole energy, which is required to charge the gate of the power switch M_{N1}, comes from the bias voltage domain. In the implemented design the domain has to provide a peak

[37] This is a typical value for Li-Ion battery.
[38] Tapered buffers are a series connection of inverter stages with increasing driver capability. This allows you to drive large capacitive loads like a gate of a power switch in a very fast way [29], [10].

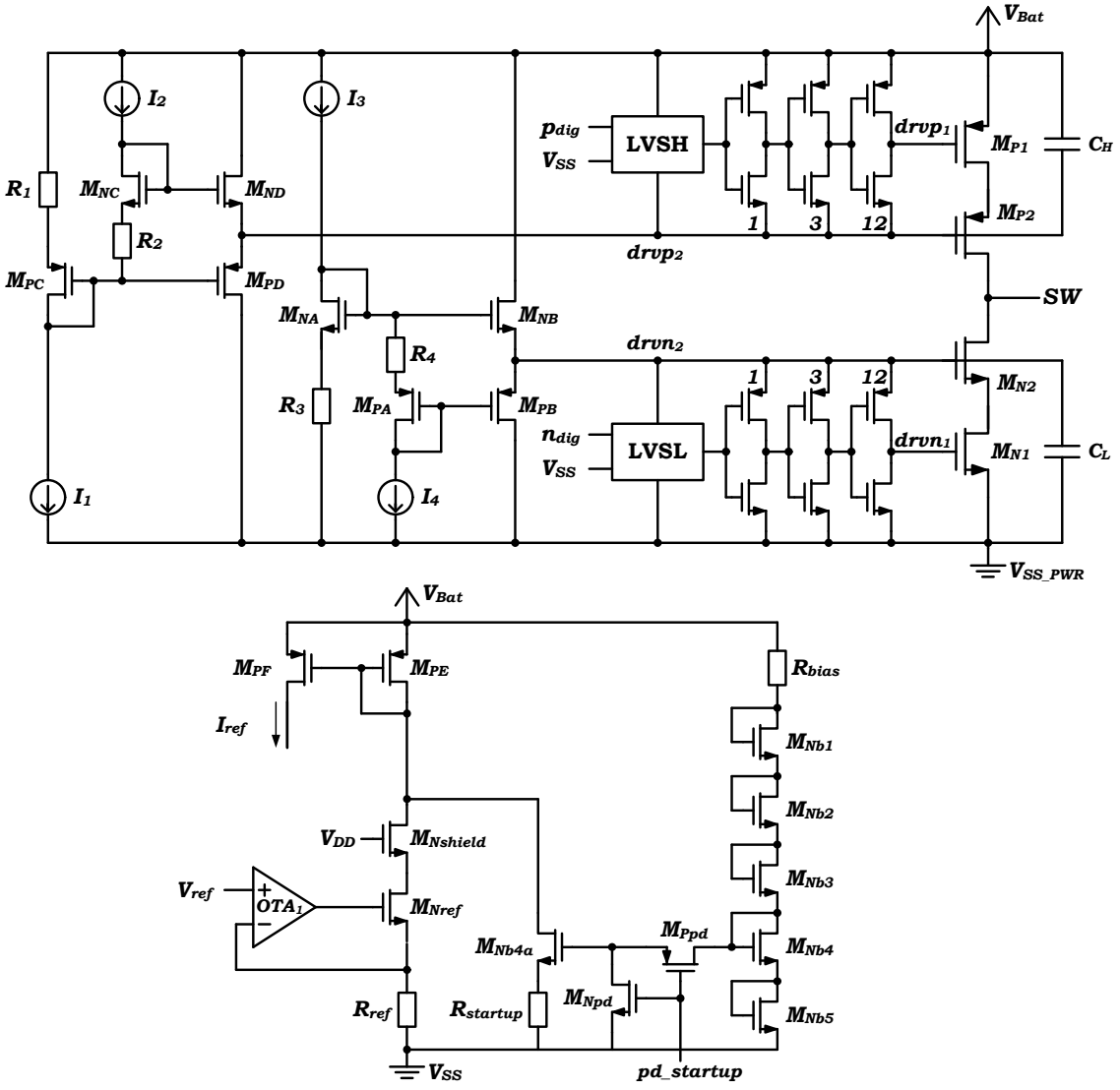


Figure 32: Simplified schematic of the gate driver with bias voltage generation for the stacked power switches

current of about 15 mA with a duration of 2 ns.
Another important requirement of the bias voltage driver is that it has to have strong source and sink capability. Due to the large gate drain capacitance of M_{N2} noise will be coupled from the very "noisy" switching node SW to the node $drvn_2$.
Therefore, complementary connected source followers M_{NB} and M_{PB} are used which provide low ohmic source and sink capability for node $drvn_2$ (see Fig. 32). If M_{NB} and M_{NA} match, the voltage at node $drvn_2$ is mainly the voltage across resistor R_3. The p-type source follower M_{PB} is biased with the same method: The resistor R_4 is used to set the sensitivity of the source followers. The higher the voltage drop across resistor R_4 is, the larger the cross current through M_{NB} and M_{PB} is and therefore the lower the resistance on node $drvn_2$ in steady state. The small signal resistance at node $drvn_2$ is approximately given by $1/gm_{MNB} \parallel 1/gm_{MPB}$.
Of course, during transients only M_{NB} or M_{PB} will be conductive. If M_{N1} is switched on, the voltage at node $drvn_2$ goes down and therefore M_{NB} becomes conductive and now provides a strong current path from V_{Bat} to the net $drvn_2$. M_{NB} is conductive exactly as long as node $drvn_2$ is below the target voltage. For the other direction it works in the same way: if the voltage at node $drvn_2$ becomes too high, M_{PB} becomes conductive and discharges the node $drvn_2$ again to the target voltage level.
In parallel to the bias generation circuitry a MOS capacitor C_L is placed to buffer net $drvn_2$ additionally. This significantly reduces the current peaks in the power domain during the driver activity.
The lower schematic in Fig. 32 shows the bias current generation of the gate driver. The currents are generated with an OTA (OTA_1) connected to a source follower M_{Nref}: The OTA regulates the gate voltage of M_{Nref} in such a way that the voltage across the resistor R_{ref} is exactly the reference voltage V_{ref}. Therefore, the current through the resistor R_{ref} is given by V_{ref}/R_{ref} and if M_{PE} and M_{PF} have the same transistor size, also I_{ref} is equal to the current through this resistor.
The important point is now that R_{ref} should be matched with all resistors in the gate driver block. If this is the case, V_{ref}, the resistor ratios and the current mirror ratios primarily define the voltages $drvn_2$ and $drvp_2$ – so it is possible to set the bias voltages in the output stage quite accurately.
Fig. 32 also shows an auxiliary circuitry which provides a current I_{ref} during start-up of the chip and in power down mode (in this case no reference voltage

V_{ref} is available). This is required since the stacked transistors in the output stage always have to be biased with proper values in order to guarantee that the drain source voltage on each transistor never exceeds the voltage limits.

5.4 Level shifters (LVSH, LVSL)

Level shifters are the interface between the power domain (domain where the battery is connected) and the core power domain (digital 1.2 V domain). They are required because of the different voltage levels of the domains but also because of large potential shifts between the voltage domains during the switching activity of the converter. In the designed IB DC-DC buck converter potential shifts up to $\pm$ 1 V are possible due to parasitic inductances in the power traces. This means that if the level shifter should shift a signal from the core power domain ($VDD = 1.2\,\mathrm{V}$, $VSS = 0\,\mathrm{V}$) to the power domain ($drvn_2 = 2.8\,\mathrm{V}$, $V_{SS\_PWR} = 0\,\mathrm{V}$) the level shifter also has to operate for voltages of $drvn_2 = 3.8\,\mathrm{V}$, $V_{SS\_PWR} = 1\,\mathrm{V}$ and $drvn_2 = 1.8\,\mathrm{V}$, $V_{SS\_PWR} = -1\,\mathrm{V}$. So you can see that the level shifters have to be very robust and voltage tolerant in design.
Two different level shifters have been implemented in this work: the $LVSH$ which is used for controlling the high side power switch and the $LVSL$ which is used for controlling the low side power switch and auxiliary blocks like the snubber circuit and the body diode conduction sensor. Both level shifter blocks have been depicted in Fig. 32 in the previous section.
In principle, the level shifters have to fulfil the following requirements: They should have short propagation delays in order to control the power switches in an accurate way; they should have low power consumption since the overall converter efficiency should be kept high and finally they should be very robust. Robust means that they should be robust against voltage ringing at the power traces and they always have to provide the right output information depending on the input control signals. This of course is obvious since the outputs of the level shifters are directly connected to the gates of the power switches.
In the paper “Fast and robust level shifters in 65 nm CMOS” [33] I have presented two very robust level shifter designs with very low propagation delays of below 1 ns over PVT. A highlight of the presented level shifters is that they provide very short propagation delays without the usage of capacitive coupling capacitors between the power domains, like it is done for instance in

other designs [53]. Of course, with capacitive coupling between the power domains, extremely short signal propagation delays from the input to the output of the level shifters can be achieved but the drawback of such an approach is that this will also create a strong noise coupling path between the power domains because of the coupling capacitors. And in worst case, this noise could be large enough to flip the level shifter output that could destroy the converter due to large cross current in the output stage.

5.5 Current sensing through the high side power switch

Since peak current control is used in the designed converter the peak current in the power path has to be measured. A circuitry that operates without lossy sense resistors is depicted in Fig. 33: A small sense transistor M_{P2} is connected in parallel to the high side power switch M_{P1}[39]. Both transistors M_{P1} and M_{P2} are of the same type and are controlled by the same input signal $ctrl$. The ratio between M_{P1} and M_{P2} is M/N. If the high side power switch M_{P1} and the sense transistor M_{P2} are switched on, they operate in the linear region, and therefore they can be seen as simple resistors. The current sensing block detects the peak current I_L through the power transistor M_{P1} – the calculation of the trigger point has been discussed in section 4.4.3 Eq. 60 on page 63:

$$I_L = IU \cdot \frac{M - N}{N} \quad . \tag{62}$$

As already mentioned in section 4.4.3, the trigger point of the current sensing circuit is exactly at the condition where the voltage drop across M_{P1} exceeds the voltage drop across M_{P2}. A common gate amplifier M_{P3-4} senses the voltage drops. The common gate amplifier is built with core devices that have the best matching factors in the used technology. This allows a detecting of even small voltage differences very accurately.
The output of the common gate amplifier is a current that is compared with the current through the current source M_{NC}. If the current through M_{P4} is higher than the current through M_{NC}, the high ohmic current comparator output $comp_1$ goes up. This node is connected to common drain amplifier M_{Ncomp} that further increases the gain of the amplification. In a last amplification stage the voltage at node $comp_2$ is amplified by an inverter stage. The

[39] In order to keep the circuit diagram simple, the stacked high side power switch is depicted as single transistor M_{P1}.

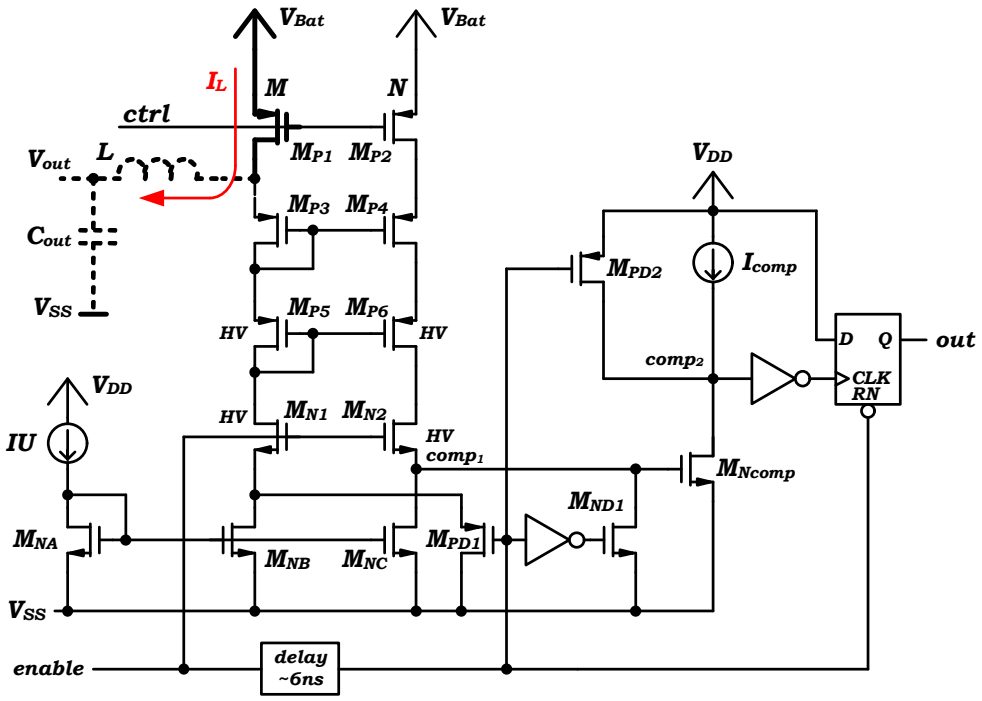


Figure 33: Simplified schematic of the current sense block for the high side switch

inverter output is connected to the clk-input of a master-slave flipflop. At a rising edge of the converter output signal the output of the flipflop becomes a logic one which indicates that the peak current through the high side power switch exceeds a certain value which was set by the input current IU (IU is the actuating variable of the controller).

High voltage transistors M_{P5-6} are used to protect the core devices M_{P3-4} against drain-source voltages that are too high and high voltage transistors M_{N1-2} are for the protection of the current mirror transistors M_{NB-C} which are also built with core devices.

Last but not least it should be mentioned that the circuitry only has to be enabled if the high side power switch is switched on. In all other conditions the complete circuitry can be switched to power down in order to reduce the power consumption and therefore the losses of the converter. In order to avoid wrong output values of the block a fixed delay time of about 6 ns is used to blank each “noisy” start up phase of the circuit. After the 6 ns all internal comparator nodes and the flipflop are released. It has been verified by simulation that all nodes have been settled accurately enough within this short delay time.

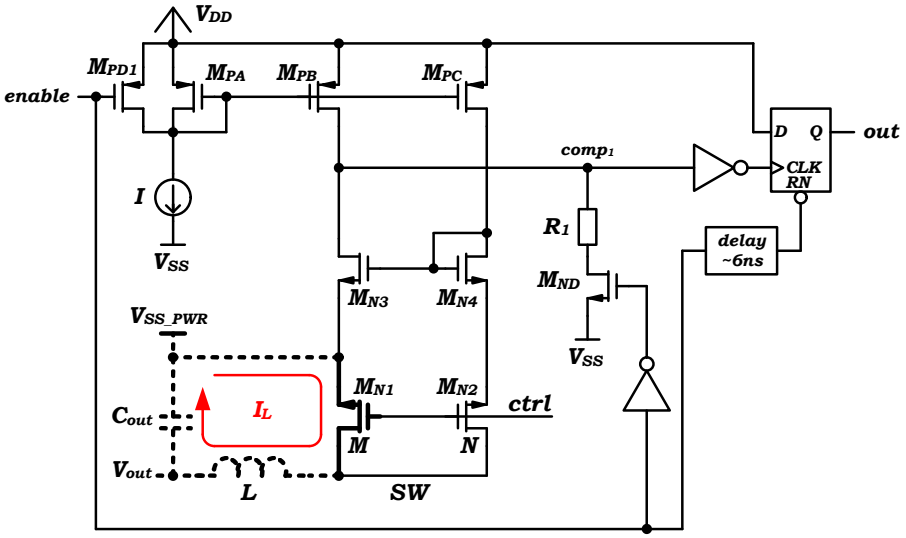


Figure 34: Simplified schematic of the current sense block for the low side switch

5.6 Current sensing through the low side power switch

In PWM-DCM the low side power switch should be switched off at the instant the inductor current I_L becomes zero. Therefore, a current comparator is required in the design which senses the zero crossing point of I_L. In practice it makes more sense to detect a current value which is slightly higher than zero – for instance 50 mA – than to try to detect the zero crossing point exactly. This is because of the fact, that it takes time for the controller to switch off the low side power switch. Therefore, all delays in the signal path have to be counted up – the sum of the delays determines the current of the power inductor which should be detected.

Again, a sense transistor topology, like the one depicted in Fig. 34, is used for measuring the current through the power switch. The used principle is the same as in the high side current sensing block explained in section 5.5: A small sense transistor M_{N2} is connected in parallel to the low side power switch M_{N1}. Both transistors are of the same type and are controlled by the same signal $ctrl$. The ratio between M_{N1} and M_{N2} is again M/N. If the low side power switch M_{N1} is switched on, it operates in the linear region. The same is valid for the sense transistor M_{N2}. Therefore, the equilibrium, or the trigger point of the current sense block is exactly when the drain-source voltage drops of both transistors M_{N1} and M_{N2} are equal. This is exactly the

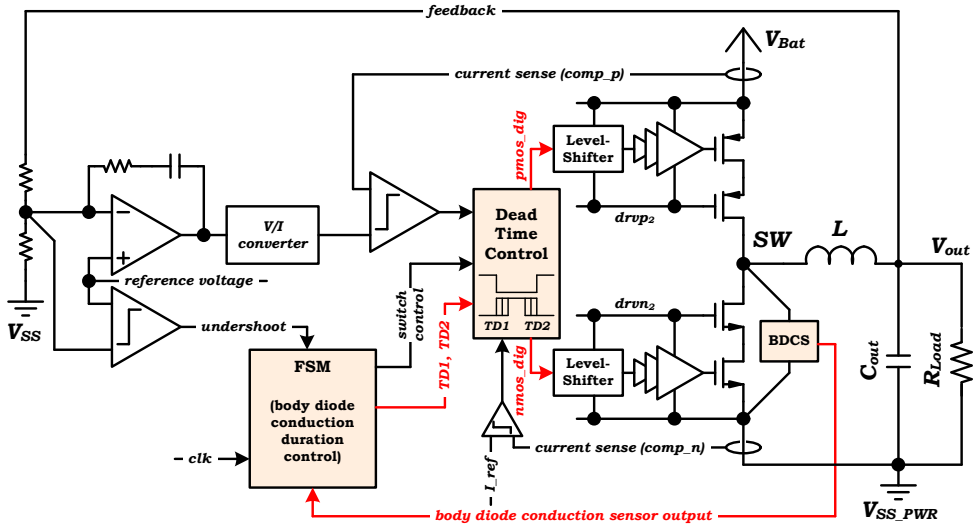
case when the power inductor current I_L becomes

$$I_L = I \cdot \frac{M - N}{N} \quad . \tag{63}$$

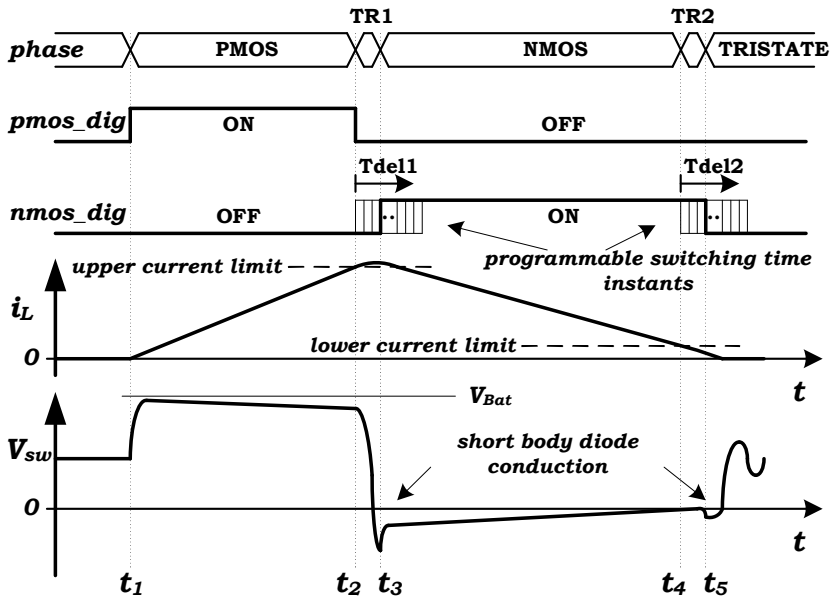
In Fig. 34 it can be seen that a delay block of about 6 ns is used to blank the measurement after start-up or after power down. This avoids wrong output signals of the current sense block due to circuit settling issues and during transients.

5.7 Automatic dead time control in the output stage

A powerful implementation of an automatic dead time control in the output stage that operates during normal converter operation is important since the implemented converter operates at very high switching frequencies. In the used concept no fast and power hungry voltage comparators are needed. On the contrary, the body diode conduction durations during the commutation phases of the power switches is measured. This means that the body diode conduction durations observe if the switching time instants of the power switches are already optimized or if they have to be adjusted (see section 4.3 on page 45).
The automatic dead time optimization concept is shown in Fig. 35a. The optimization process works in three steps:
First, there is a body diode conduction sensor (BDCS) that detects if body diode conduction occurred in the current switching cycle or not. The sensor is connected in parallel to the low side power switch and has a digital output – a logic “1” means that the BDCS measured a certain amount of body diode conduction duration and a logic “0” means that no conduction was measured. In order to be able to detect body diode conduction durations below 1 ns, disturbances (ringing, coupling) in the connection lines must be avoided. Therefore, the sensor uses sense lines that are directly connected to the power switch.
The optimization of each commutation phase in the power stage requires a separate BDCS. Therefore, two sensors are needed for a converter which operates in PWM-DCM: A first sensor, which measures the body diode conduction duration during the commutation phase where the high side power switch is switched off and the low side power switch is switched on and a second sensor, which measures during the commutation phase where the low side power switch is switched off and the converter enters the tristate phase.



(a) Block level schematic of the automatic dead time optimization concept



(b) Voltage and current waveforms at the output stage with control signals

Figure 35: Automatic dead time optimization concept for IB DC-DC buck converter with integrated power switches

More information of the used BDCS can be found in my paper: “A sensor concept for minimizing body diode conduction losses in DC/DC converters” [34].
Second, there is a finite state machine (FSM) that takes the output information of the BDCS and adjusts the digital dead time values (TD1 and TD2) according to the sensor outputs. If body diode conductions were measured in the previous switching cycle, the dead times are too long, therefore the FSM reduces the digital dead time values.
The third block in the automatic dead time control chain is the analogue dead time control block which takes the digital dead time values from the FSM and which generates the analogue control signals for the power switches with the corresponding dead times.
Fig. 35b shows how the dead time control concept is now working: You see the voltage waveform of the switching node V_{SW}, the current waveform of the power inductor current i_L and the digital control signals for the power switches $pmos\_dig$ and $nmos\_dig$. If the high side current sense block described in section 5.5 on page 79 detects the upper current limit of the power inductor i_L, the high side power switch is switched off ($pmos\_dig : 1 \rightarrow 0$).
At the same time a programmable counter based delay line starts to run, which delays the turn-on event of the low side power switch by the delay time $Tdel1$. As mentioned before, this delay is set by the FSM which has adjusted the value according to the previous BDCS outputs: $Tdel1$ will be increased if no body diode conduction duration is detected by the BDCS and it will be decreased if the BDCS has detected body diode conduction duration.
If the low side power switch is switched on after the delay $Tdel1$ at time instant t_3, almost no body diode conduction can be observed at V_{sw} – this means that the commutation has already been optimized.
The same principle is used for the switching-off event of the low side power switch. There, the target is to detect exactly the zero current transition in the inductor current i_L. After the lower current limit is detected by the low side current sense block described in section 5.6 on page 81 (at time instant t_4) a programmable delay line propagates the switching-off event of the low side power switch depending on the value set by the FSM. If the low side power switch is switched off exactly after the delay $Tdel2$ at time instant t_5, almost no body diode conduction occurs which means that t_5 is the optimized switching time instant to switch it off.
In order to be able to optimize the switching-off event of the low side power

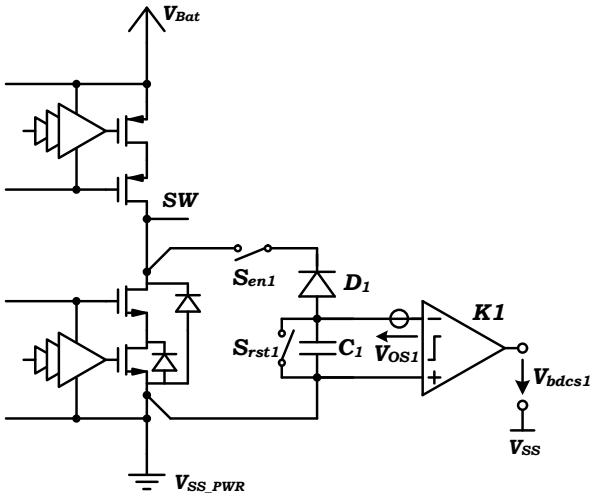


Figure 36: Body diode conduction sensor

switch it has to be guaranteed that the detected inductor current $i_L$at time instant t_4 is always positive. If this is not the case, an automatic trimming is not possible any more since the lowest possible delay $Tdel2 = 0$ already gives a current threshold below “zero”.
The overall automatic dead time optimization concept was presented in my paper: “Automatic dead time optimization in a high frequency DC-DC buck converter in 65 nm CMOS” [36].
Finally it should be mentioned that the developed automatic dead time concept is not limited to buck converters – it can also be used for other converter types.

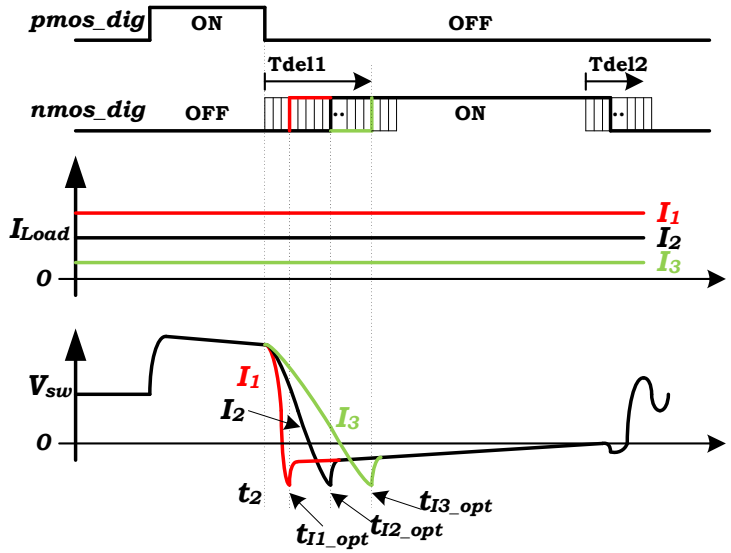
5.7.1 Body diode conduction sensor – BDCS

As already explained in the previous section, the BDCS measures if there is body diode conduction or not. Fig. 36 shows in a bit more detail how the sensor is constructed: The sensor is connected with sense wires in parallel to the low side switch in order to measure if a large negative drain-source voltage occurs. This would be the case if current flows through the parasitic body diode of the power switch. In case of a positive voltage on the switching node SW the diode D_1 protects the capacitor C_1 from being charged up – in case of negative voltage on the SW, D_1 will become conductive and C_1 will be charged up. The switches S_{en1} and S_{rst1} are for setting the different operating modes of the sensor (see also section 4.3 on page 45 and [34]).
For controlling the switches S_{en1} and S_{rst1} level shifters are used which shift

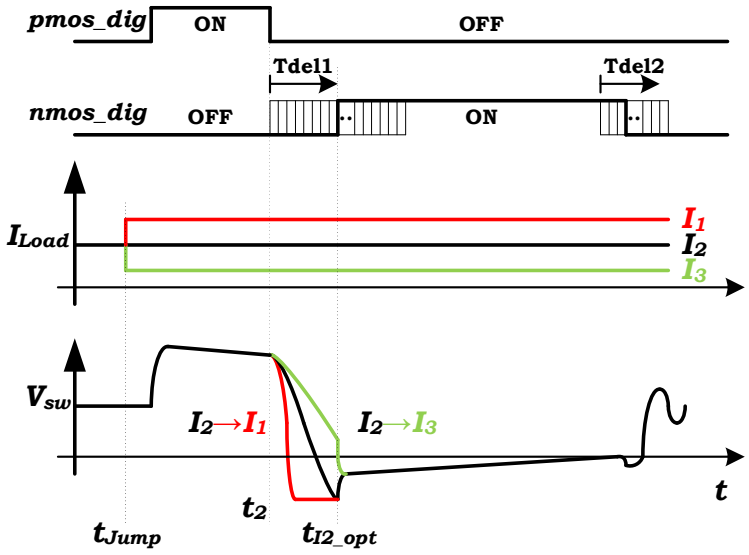
the control signals from the 1.2 V core power domain to the 5 V power domain (see section 5.4 on page 78). Another level shifter is required to shift the result from the BDCS back to the core domain. This level shifter is integrated in the comparator $K1$ that evaluates the voltage across the capacitor C_1. The output V_{bdcs1} of $K1$ is then used to adjust the dead times of the power switches.
Although the developed concept is very simple a lot of design effort has to be spent to manage the large voltage ringing in the power domain. It has to be especially guaranteed that C_1 will not be charged during transients because of voltage ringing and cross coupling effects.

5.7.2 Behaviour of the optimization algorithm during load changes

The dead time optimization concept uses the approach that the BDCS first checks if body diode conduction occurs or not. Afterwards, the FSM adjusts the dead times of the power switches depending on the results of the BDCS outputs. Since the optimization is done stepwise the used concept needs a certain time to find the optimized switching time instants. In case of process and temperature variations this is not a problem since such variations have slow time constants. The same is true for input voltage variations: Since the converter is connected to a Li-Ion battery also the changes of the input voltage also have a slow time constant.
But this is not true for load jumps. Since it is very common that loads connected to the converter change their load currents very fast the dead time optimization algorithm is not always able to provide the optimized dead time values because the algorithm rather takes some time to find the optimized values again. Especially if heavy load jumps with high occurrence rates are applied to the converter, the optimization concept could be too slow to always find the optimized dead time values. If this were the case, the efficiency improvement of the automatic dead time optimization concept could be small.
Next, you should see how the dead time concept behaves during positive and negative load jumps. Fig. 37a shows the optimized switching time instants for transition phase 1 for different load currents I_1, I_2 and I_3, where $I_1 > I_2 > I_3$. You can see that the higher the load current is, the faster the voltage ramps at the switching node and the shorter the optimized delay values $Tdel1$ are. This is because of the parasitic capacitance at the switching node which is discharged by the inductor current i_L. If i_L is high, the parasitic capacitance at the switching node will be discharged fast, but if i_L is low, it takes more time to discharge it. That is why there are three different



(a) Optimized switching time instants for different load currents I_1, I_2 and I_3 in steady state



(b) Body diode conduction after a load jump

Figure 37: Behaviour of the automatic body diode conduction optimization algorithm in case of load jumps

optimized switching-on time instants t_{I1_opt}, t_{I2_opt} and t_{I3_opt} of the low side power switch for three different load currents I_1, I_2 and I_3.
Fig. 37b now shows what happens during load jumps: First, let us assume that there is a positive load jump from I_2 to I_1 at the time instant t_{Jump}. Since the dead time optimization algorithm cannot react instantaneously or in advance, the low side power switch is switched on at time instant t_{I2_opt} which is the optimized value for the current I_2. Since $I_1 > I_2$ the switching node of the converter will be discharged faster. Since the low side power switch is switched on at t_{I2_opt} – which is too late now – body diode conduction will occur. Now, the BDCS will detect body diode conduction duration and the FSM will counteract. But anyhow, the switching time instants of the power switches will not be optimized for several switching cycles after the load jump, since it takes time to re-converge again.
The same can be observed in case of a negative load jump from I_2 to I_3 where $I_2 > I_3$. In this case the current which discharges the switching node becomes smaller therefore, the low side power switch will already be switched on before the voltage on the switching node crosses the zero voltage cross point. From Fig. 37b it can be seen that no body diode conduction will occur after such a load step but you can be see that the low side power switch is switched on too early. This means that the low side power switch will actively discharge the switching node. Again, the dead time optimization concept needs some switching cycles to again find the optimum switching time instants of the power switches.
So it can be summarized that the effectiveness of the developed dead time optimization concept strongly depends on the occurrence rate of the load jumps.

5.8 Controller stability

This section shows the stability analysis of the peak current controller for one operating condition of the converter. For the stability proof the analytical small signal model developed in section 4.4 on page 49 is used.
First, all transfer functions of the blocks within the controller loop have to be calculated. Afterwards, the whole open loop transfer function of the controller loop can be calculated by using different controller types with different properties, e. g. open loop gain, gain bandwidth, and so on. Since the optimization is done analytically also the plant properties can be varied very easily: The output filter size of the converter can be changed; different load currents can

be used for the analysis; the stability can be checked for different input and output voltages of the converter and so on. Finally, the controller which fits best into the application and which shows the best overall performance is then chosen.

Now, the stability proof of one operating point of the designed IB DC-DC buck converter operating in PWM-DCM with peak current control is shown. The given parameters which are used in the example for the transfer function of the plant are: $L = 350\,\mathrm{nH}$, $C = 400\,\mathrm{nF}$, $R_S = 500\,\mathrm{m\Omega}$, $R_L = 130\,\mathrm{m\Omega}$, $R_C = 25\,\mathrm{m\Omega}$, $V_{out} = V_C = 1.2\,\mathrm{V}$, $V_{in} = 5\,\mathrm{V}$, $I_L = 20\,\mathrm{mA}$, $fsw = 4\,\mathrm{MHz}$. By using Eq. 53 on page 60 the transfer function of the plant can be calculated. It is

$$Plant\,(s) = \frac{4.3 \cdot 10^{13}}{s^2 + 6.1 \cdot 10^7 \cdot s + 3 \cdot 10^{12}} \quad . \tag{64}$$

The transfer function of the PI controller can be calculated by using Eq. 57 on page 61. If $R_0 = 80\,\mathrm{k\Omega}$, $R_1 = 112\,\mathrm{k\Omega}$, $R_2 = 750\,\mathrm{k\Omega}$, $C = 4\,\mathrm{pF}$, $\omega_g = 2 \cdot \pi \cdot 25\,\mathrm{kHz}$ and $A_0 = 1000$ the transfer function $PI(s)$ is given by

$$PI\,(s) = \frac{3.8 \cdot 10^7 \cdot s + 1.3 \cdot 10^{13}}{0.6 \cdot s^2 + 5.9 \cdot 10^6 \cdot s + 3.0 \cdot 10^{10}} \quad . \tag{65}$$

The transfer function of the voltage to current converter can be calculated with Eq. 58 on page 62, if $R = 90\,\mathrm{k\Omega}$, then it is

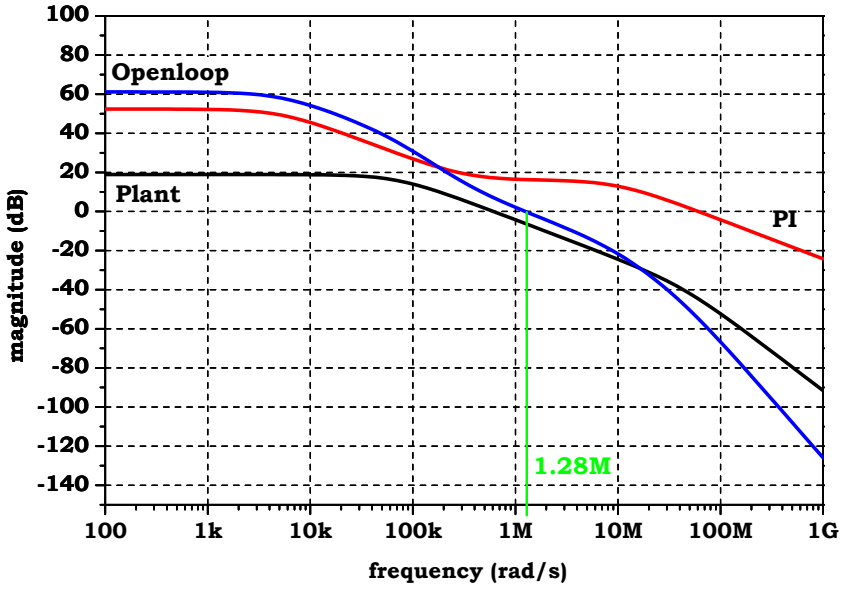
$$UtoI\,(s) = \frac{1}{90 \cdot 10^3} \quad . \tag{66}$$

Last but not least, the transfer function of the high side power switch current sensing block has to be calculated by using Eq. 60 on page 63. If $M = 1400$,$N = 1/4$ and $k = 5$, the transfer function is given by

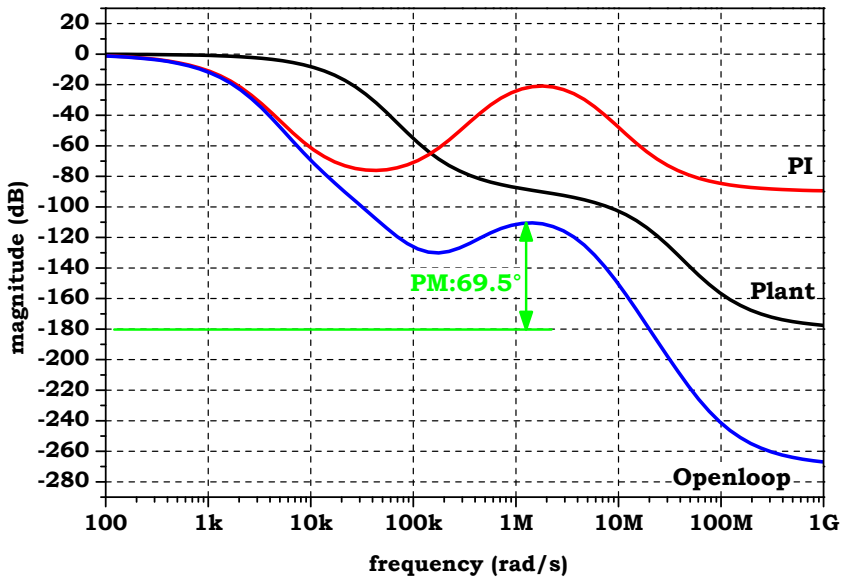
$$pmos\_sense\,(s) = 27995 \quad . \tag{67}$$

Now, the open loop transfer function can be calculated by multiplying all single transfer functions as it is shown in Eq. 61 on page 64. In the used example the final open loop transfer function is

$$G\,(s)_{ol} = \frac{2.8e25 \cdot s + 9.3e30}{5.5e4 \cdot s^4 + 2.9e12 \cdot s^3 + 2.3e19 s^2 + 1.7e24 \cdot s + 8.1e27} \quad .$$



(a) magnitude



(b) phase

Figure 38: Bode plot of the open loop transfer function of Eq. 68

(68)

The bode plots of the open loop transfer functions $G(s)_{ol}$ (Eq. 68), the PI controller (Eq. 57 on page 61) and of the plant (Eq. 53 on page 60) are shown in Fig. 38. The cross over frequency is at about 1.28 MHz, the phase margin is 69.5 ° which shows that the controller is perfectly stable.
Also it should be mentioned that the phase of the open loop transfer function raises at a frequency of about 200 kHz due to the "zero" of the implemented PI controller.

5.9 Digital state machine

The digital state machine (FSM) is used to control the the overall functionality of the chip. The FSM was developed in the digital design flow – VHDL was used to code the functionality, then the code was synthesized and finally an automatic place and route tool was used to generate the digital layout of the FSM. Features implemented in the FSM are:

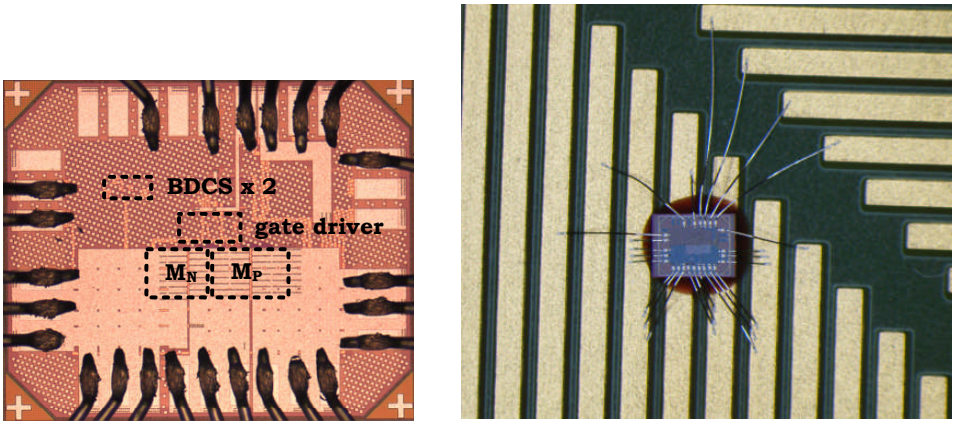
- automatic frequency hopping
- emergency functionality to handle large voltage undershoots of the converter output voltage during heavy load jumps
- automatic pulse skipping mode to provide high power conversion efficiencies at very light loads
- manual programmable power down functionality for each block in order to measure the current consumption of each block
- automatic dead time optimization concept and manual programmable dead times
- different test modes e. g. lock frequency hopping and force a certain switching frequency of the converter
- digital debug features of important signals e. g. the BDCS outputs

6 Test chips and measurement results

This section shows the measurement results of both fabricated test chips during this work. In the first test chip the body diode conduction sensor shown in Fig. 36 on page 85 was tested. In the second test chip the whole designed IB DC-DC buck converter was implemented.

6.1 First test chip: body diode conduction sensor

The target of the first test chip was to evaluate the performance of the proposed body diode conduction sensor concept. The main question was if the sensor is also able to give reasonable results in a real power stage of a DC-DC buck converter with a harsh environment. Especially large voltage ringing at the power traces will occurs due to the parasitic power inductances in the power paths.
In the test chip, two body diode conduction sensors were placed beside the low side power switch in an existing power stage of an IB DC-DC buck converter: The first sensor was for measuring the body diode conduction duration during transition phase 1 and the second one was for measuring the body diode conduction duration during transition phase 2 (see the transition phases $TR1$ and $TR2$ in Fig. 4.3 on page 45). In order to have more possibilities to evaluate the performance of the sensors in the laboratory, linear voltage amplifiers with an amplification factor of five were placed at the sensor outputs instead of voltage comparators. This allows you to measure the absolute output voltage of the sensor for different body diode conduction durations.
Fig. 39a shows a die photograph of the test chip including the converter output stage with the power switches M_P and M_N, the gate drivers of the output stage and the two body diode conduction sensors. The die was not put into a package but it was directly bonded on a PCB as shown in Fig. 39b.
Fig. 40 shows measurement results of the first test chip: In Fig. 40a the voltage waveform of the switching node of the converter is shown – it can be seen that the converter operates in PWM-DCM and that there is body diode conduction during transition phase 1 where the current commutation from the high side to the low side power switch is done. Furthermore it can be seen that there is also body diode conduction during transition phase 2 where the low side power switch is switched off and the converter enters the tristate phase.
Fig.40b shows the amplified sensor output that detects body diode conduction



(a) Die photo (b) Die bonded directly on a PCB

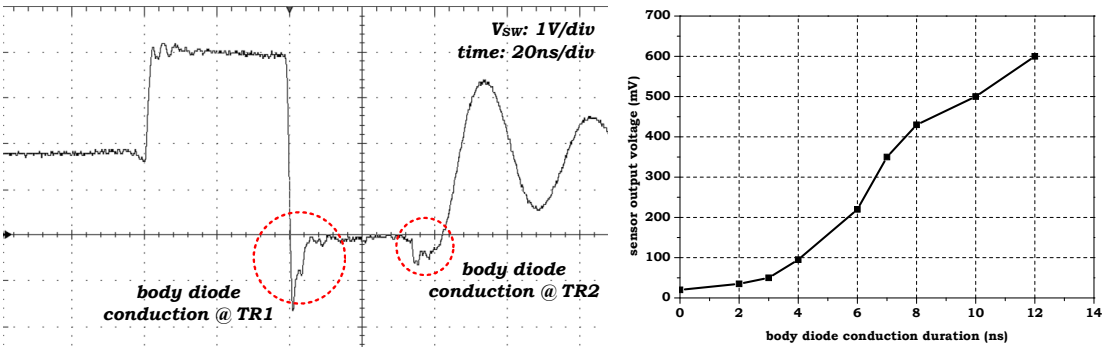
Figure 39: First test chip with body diode conduction sensors [34]

during phase 2. It can be seen that the sensor behaves as expected: The longer the body diode conduction duration is the higher the voltage across the capacitor in the BDCS and therefore the higher the voltage at the output of the linear amplifier.

It has to be mentioned that the inductor current at transition phase 2 ideally should become "zero" before the low side power switch is switched off. If it is switched off a bit too early where the inductor current is slightly positive. Only this remaining small current will flow through the parasitic body diode. Therefore, the forward voltage of the body diode will be small which is the reason why the sensor is only able to detect body diode conduction durations down to about 4 ns for transition phase 2.

Fig. 40a shows body diode conduction also during transition phase 1 – the duration is about 4 ns. Due to a design problem in the fabricated test chip it was not possible to also adjust the dead times for transition phase 1. Therefore no measurement results of the relation between the sensor output and the corresponding body diode conduction duration times are available. Due to the fixed dead times the sensor output was always about 470 mV.

The test chip has shown that the body diode conduction sensor works very well for transition phase 1 that fits to the simulation results. The results were presented in my paper [34].



(a) Voltage waveform of the switching node

(b) Body diode conduction sensor output

Figure 40: First test chip with body diode conduction sensor [34]

6.2 Second test chip: whole IB DC-DC buck converter

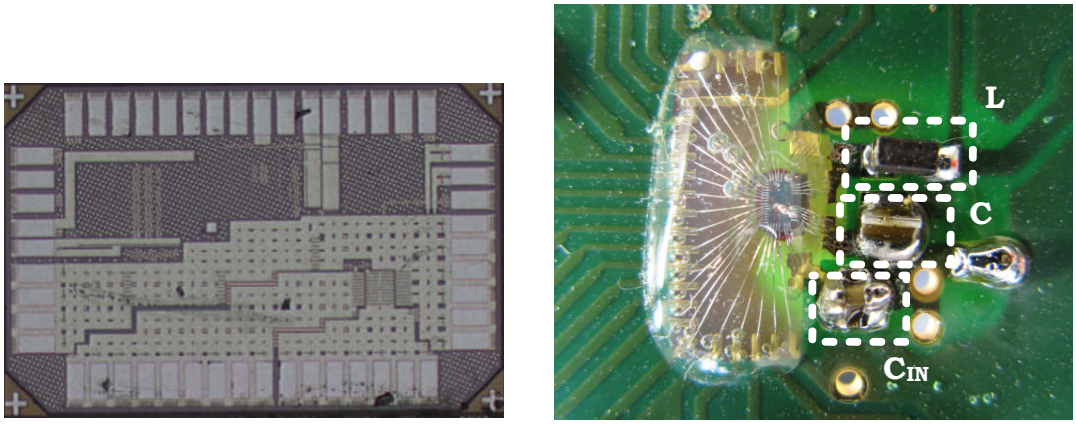
In the second test chip the whole IB DC-DC buck converter shown in chapter 5 on page 65 was implemented. The design includes several innovative concepts like an automatic dead time optimization concept, high speed level shifters and a stacked power switch approach which allows you to apply high input voltages up to 5 V to the converter.

Fig. 41a shows a die photograph of the fabricated chip. The whole converter only occupies 0.088 mm^2 in area. Again the die directly was bonded onto a PCB like it is depicted in Fig. 41b: There, the silicon was placed side by side with the passive components of the output and input filter. With this approach the power traces can be kept short. Therefore, the parasitic inductances in the power traces are smaller, which would emulate a chip package co-design approach.

6.2.1 The power conversion efficiency

The most important converter parameter is probably the power conversion efficiency. Fig. 42 shows the power conversion efficiencies of the converter for a lot of different operating points.

Fig. 42a shows measurement results for different load currents. It can be seen that the achieved converter peak efficiency is around 74 % at a load current of 40 mA, a switching frequency of 4 MHz and a battery voltage of 3 V. You can also see that the power conversion efficiency is high for very light loads I_{Load}: At $I_{Load} = 10\,\text{mA}$ the achieved power conversion efficiency is almost 73 %,



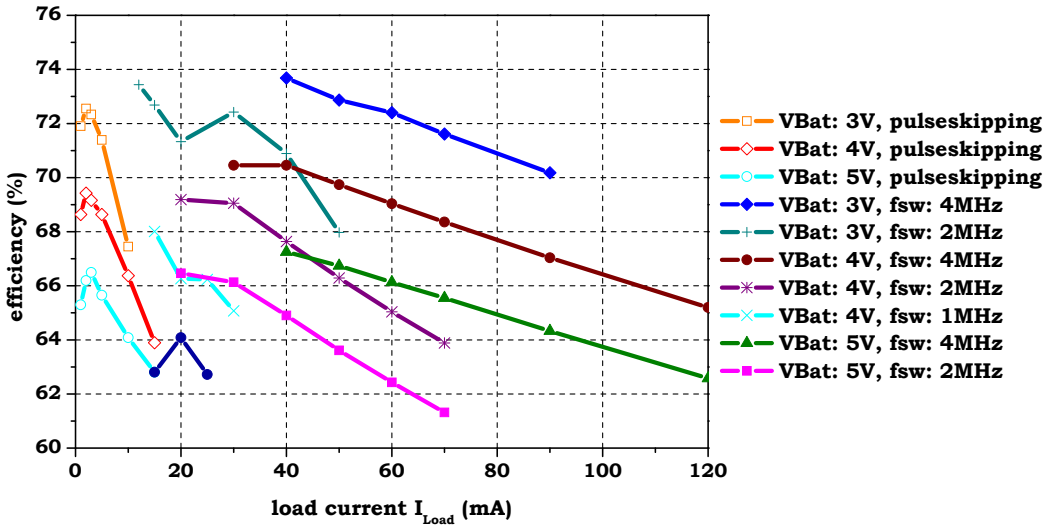
(a) Die photo (b) Die bonded directly on a PCB

Figure 41: Second test chip of the whole IB DC-DC buck converter [36]

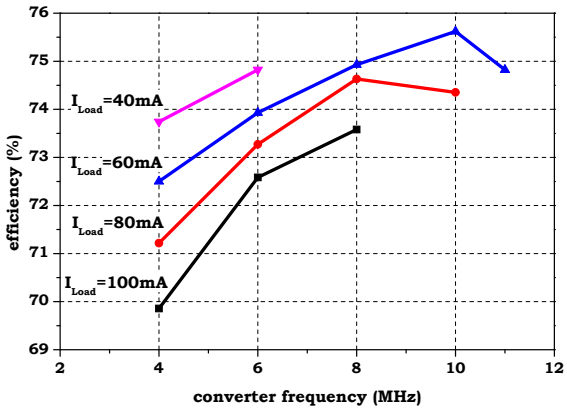
which is almost the peak efficiency value.
The power conversion efficiency goes down if the input voltage of the converter is increased. In this case the transition losses of the high side power switch become higher. Additionally the losses increase due to charging and discharging the parasitic capacitor on the switching node. The measurement results show that the power conversion efficiency of the converter is about 6 % lower for a battery voltage of 5 V than it is for a battery voltage of 3 V.
Fig. 42b and 42c show efficiency measurement results for different switching frequencies. The efficiency of the converter increases if higher switching frequencies are used. This shows that the major loss contributors of the converter are the conduction losses of the power switches since the peak current of the current pulses decreases with a higher switching frequency if a constant load current is applied to the converter (see also Fig. 25 on page 57). At a certain switching frequency of the converter the efficiency starts to decrease again – at this point the switching losses of the power stage become the major loss contributor and conduction losses will not dominate any more.

6.2.2 Transient behaviour and frequency hopping

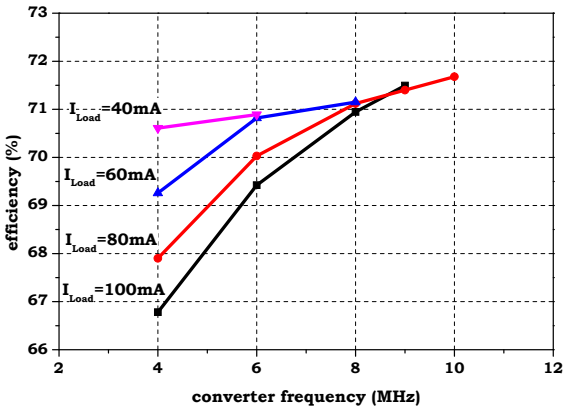
This section shows measurement results during load jumps. Fig. 43a shows the regulation behaviour of the converter if a load jump is applied during pulse skipping mode: The upper waveform is the load current I_Load, the waveform in the middle is the output voltage V_{out} of the converter and the lower waveform shows the voltage on the switching node. First, a very light



(a) Converter efficiency versus the load current I_{Load}



(b) Converter efficiency versus switching frequency for $V_{Bat} = 3V$



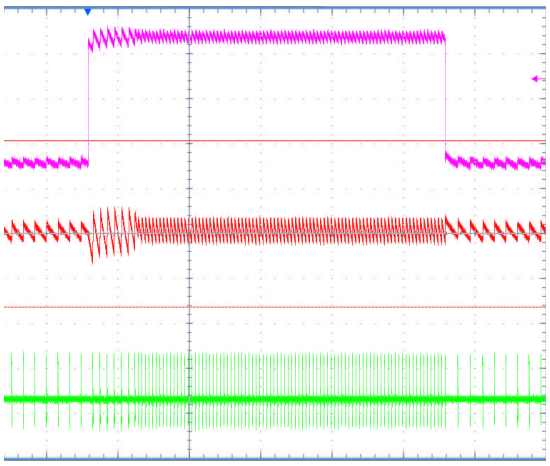
(c) Converter efficiency versus switching frequency for $V_{Bat} = 4V$

Figure 42: Efficiency measurements at different operating points for a converter output voltage of $V_{out} = 1.2V$

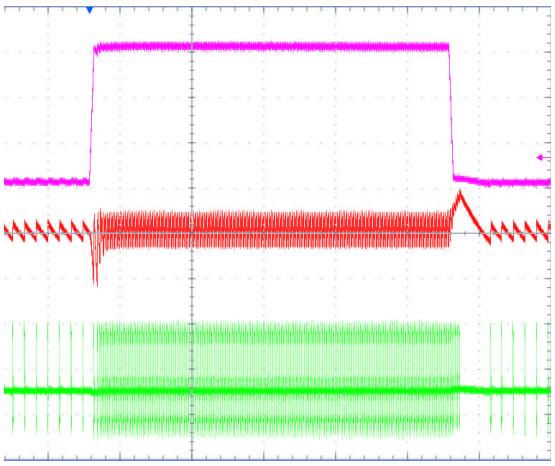
load current of 3 mA is applied to the converter. For this light load the converter operates in pulse skipping mode – therefore, the switching frequency of the converter is only about 250 kHz. After a small load jump of 14 mA the converter leaves the pulse skipping mode and moves to a constant switching frequency of 500 kHz. In order to now provide the load of 17 mA at a switching frequency of 500 KHz, the peak current becomes high. Therefore, the output voltage ripple also becomes higher. Due to the higher RMS value of the current pulses in the power paths the converter efficiency goes down. In this case, the converter automatically changes the switching frequency to 1 MHz which reduces again the peak current through the power inductor and therefore the voltage ripple on the converter output. Now the power conversion efficiency of the converter will increase since the peak current value and the RMS value of the current in the power paths become smaller as a consequence.
For the load jump back to $I_{Load} = 3\,\mathrm{mA}$ it is exactly the opposite: The converter goes back into pulse skipping mode in order to handle these very light loads with a high power conversion efficiency.
Fig. 43b shows a 60 mA load jump, starting again from a constant load of 3 mA. This situation is quite a bad situation for the converter since a high load jump occurs while the converter is in pulse skipping mode where the switching frequency is low. Due to the low switching frequency the converter can react too late – therefore, the resulting voltage undershoot on the converter output will be high which triggers an under-voltage comparator (the comparator threshold is 90 mV below the steady state output voltage of the converter). If the under-voltage comparator is triggered, the converter immediately goes to a switching frequency of 4 MHz. In this mode the converter can handle much higher loads. The voltage undershoot on the converter output for such a load jump is about 100 mV, as it can be seen in Fig. 43b.
For a load jump back to $I_{Load} = 3\,\mathrm{mA}$ again it is the opposite: The converter goes back into pulse skipping mode in order to provide the very light load. The voltage overshoot on the converter output is about 90 mV.
The waveform in the middle of Fig. 43c shows the steady state output voltage ripple of the converter operating at $V_{Bat} = 4\,\mathrm{V}$, $I_{Load} = 50\,\mathrm{mA}$ and $fsw = 4\,\mathrm{MHz}$. It can be seen that the converter output voltage ripple is about 30 mV.

6.2.3 Automatic dead time optimization concept

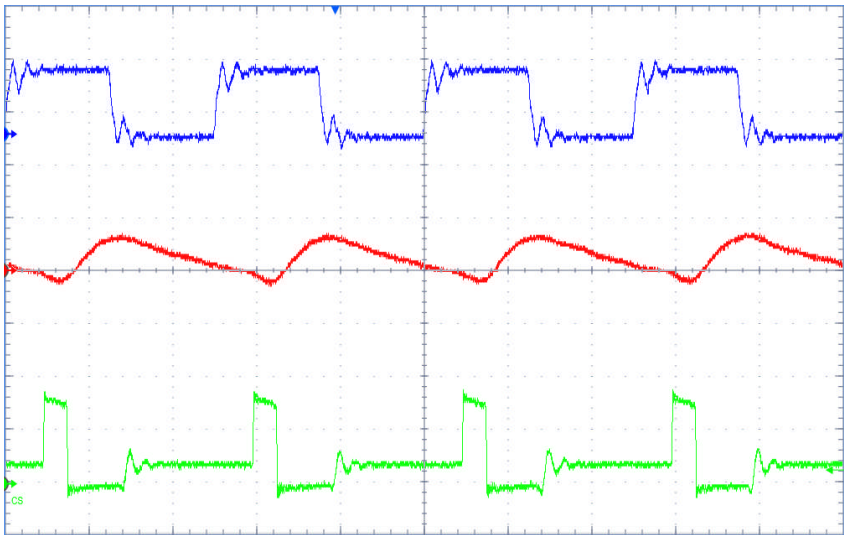
The automatic dead time optimization concept (see more information in section 5.7 on page 82) was one of the most important outcomes of this work. The



(a) Load step from $3\,mA$ to $17\,mA$ (upper curve: load current $5\,mA/div$; middle curve: output voltage $90\,mV/div$; lower curve: sw node $3\,V/div$; time: $20\,\mu s/div$)

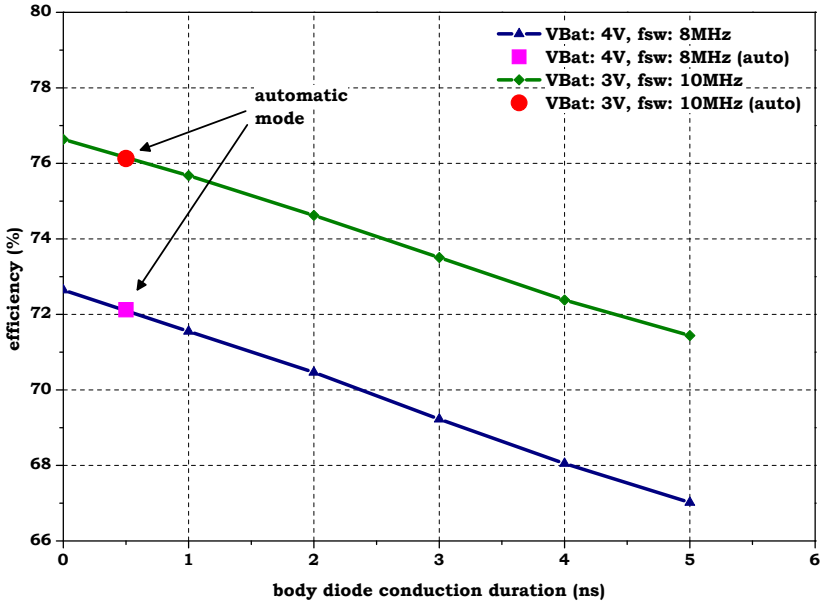


(b) Load step from $3\,mA$ to $63\,mA$ (upper curve: load current $20\,mA/div$; middle curve: output voltage $90\,mV/div$; lower curve: sw node $2\,V/div$; time: $20\,\mu s/div$)

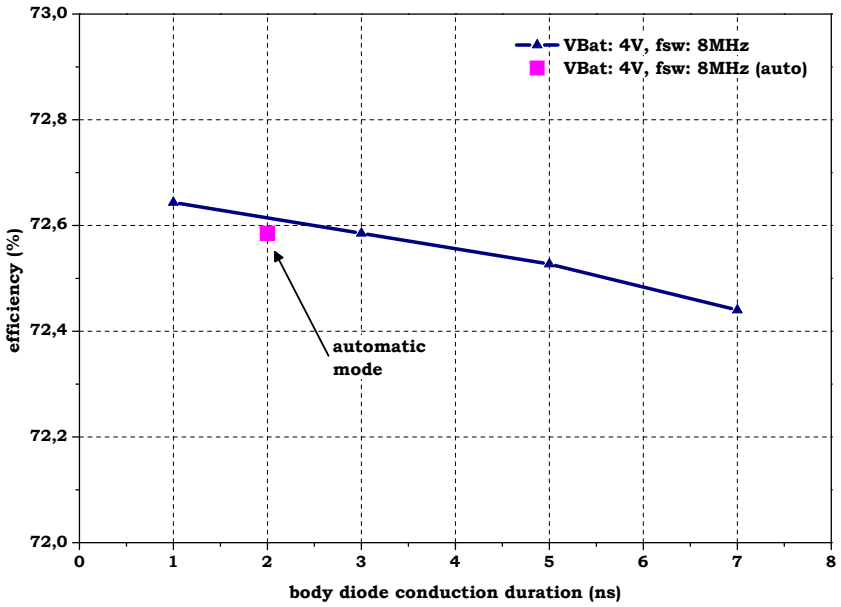


(c) Output voltage ripple at $V_{Bat} = 4\,V$ and $I_{Load} = 50\,mA$ (upper curve: clk; middle curve: output voltage $30\,mV/div$; lower curve: sw node $3\,V/div$; time: $100\,ns/div$)

Figure 43: Converter behaviour during load jumps and output voltage ripple



(a) Transition phase 1



(b) Transition phase 2

Figure 44: Converter efficiency for different body diode conduction durations for $V_{out} = 1.2V$ and $I_{Load} = 60mA$ [36]

gate drivers for the power switches of the output stage were implemented in such a way that it is possible to adjust manually the dead times of the output stage of the converter. This gives the opportunity of measuring the power conversion efficiency of the converter for different dead time durations.
Fig. 44a shows measurement results of the converter efficiency for different body diode conduction durations at transition phase 1. It can clearly be seen that the power conversion efficiency immediately goes down if the dead times are increased by only 1 ns. Without any body diode conduction the converter is able to achieve a power conversion efficiency of almost 77 %. If the duration is increased to 5 ns, which could be a typical value for a design without an implemented dead time optimization concept, the converter efficiency goes down to about 72 %. The situation becomes even worse if the load current and the switching frequency of the converter are increased.
The red data point in Fig. 44a shows the achieved power conversion efficiency with enabled automatic dead time optimization. It can be seen that by using this concept almost the same converter efficiency can be achieved as with perfect manually trimmed dead times. So it is guaranteed that the converter always switches with optimized dead time values over PVT.
The same measurements were done for transition phase 2. You can see here that almost the same power conversion efficiency of the converter can be achieved as with perfect manually trimmed dead times if the automatic dead time optimization algorithm is enabled. Of course the efficiency benefit is much lower for transition phase 2 than for transition phase 1 since the current through the power inductor is already almost zero at this phase. However, it can be seen that the concept also works very well for transition phase 2.

6.2.4 Summary table – performance

Table 5: Performance table of the IB DC-DC

Property	**Value**	**Results and comments**
Input voltage V_{in}	2.5 V to 5 V	Stacked IO devices were used for the power switches to withstand the high input voltages in the used 65 nm CMOS technology (see section 5.2 on page 71)
Nominal output voltage V_{out}	1.2 V	
Output voltage ripple V_{out_pp}	below 100 mV	V_{out_pp} strongly depends on the peak current IU and therefore on the switching frequency of the converter (see section 4.4.2 on page 53). Automatic frequency hopping was implemented to limit $V_{out\_pp} <$ 100 mV (see measurement results in Fig. 43 on page 99)
Load current I_{Load}	0 mA to 120 mA	Automatic frequency hopping was implemented to optimize the power conversion efficiency of the converter over the complete load current range (see section 4.4.2 on page 53). A pulse skipping mode is implemented to allow load currents down to zero.

Continued on next page

Table 5 – *Continued from previous page – converter performance*

Property	**Value**	**Results and comments**
Power inductor L	350 nH	A very small wire-wound power inductor is used at the output filter of the converter. For the chip verification the power inductor **BRC1608TR35M** from the company "Taiyo Yuden" with $L = 350\,\text{nH}$ and $Rdc = 0.080\,\Omega$ was used. More information about power inductors can be found in section 4.1.1 on page 35.
Output capacitor C_{out}	470 nF	The ceramic capacitor **EWK107BJ474MV-T** with very low ESL from the company "Taiyo Yuden" was used at the output filter of the converter. Additional information about capacitors can be found in section 4.1.2 on page 39.
Input capacitor C_{in}	470 nF	For C_{in} the same capacitor type was used as for C_{out}.

Continued on next page

Table 5 – *Continued from previous page – converter performance*

Property	**Value**	**Results and comments**
Switching frequency fsw	0 Hz to 10 MHz	In normal mode the fsw of the converter is synchronous. The highest possible fsw is set by an external clock. The converter automatically changes the fsw according to the applied load current in fixed frequency steps. If the external clock is 8 MHz, then fsw can be 8 MHz, 4 MHz, 2 MHz and 1 MHz (automatic frequency hopping). In order to provide very light loads pulse skipping mode was also implemented. More information about the used controller is in section 4.4.2 on page 53.
Converter efficiency η	Peak efficiency up to 76 %	The measured power conversion efficiency of the converter is above 70 % for loads from 1 mA to 90 mA (see measurement results in Fig. 42a on page 97). The measured peak efficiency of the converter is 76 % (see Fig. 44a on page 100).
Chip area	0.088 mm^2	Since the design is targeted as a linear voltage regulator replacement, the area consumption of the design was very critical. The outcome is a converter design which only occupies 0.088 mm^2 (area is comparable to linear voltage converter designs).

Continued on next page

Table 5 – *Continued from previous page – converter performance*

Property	**Value**	**Results and comments**
Technology	65 nm CMOS	Low power CMOS technology with 5 V transistor option

6.2.5 Summary table – properties

Table 6: Property table of the IB DC-DC

Property	**Results and comments**
Controller	An analogue peak current controller with frequency hopping and pulse skipping mode is implemented. More information about the controller can be found in section 4.4.2 on page 53.
Dead time optimization	For both transition phases automatic dead time control is implemented which operates during normal converter operation. If the optimization algorithm is enabled, the remaining dead times for transition phase 1 and transition phase 2 are about 500 ps and 2 ns, respectively (see measurement results in Fig. 44 on page 100). More information about the automatic dead time concept is in section 5.7 on page 82.
High speed level shifters	Two robust, high-speed level shifters with propagation delays below 1 ns over PVT were developed. The level shifters are the interface between the power domain and the core voltage domain. More information about the level shifters is in section 5.4 on page 78.

7 Research summary and outlook

The outcome of this PhD work is a fully functional test chip of a high frequency IB DC-DC buck converter design in 65 nm CMOS technology. The converter should be used as a linear voltage replacement in chips for mobile applications.

Several innovative concepts and circuits have been used in the converter design and have been proved on silicon in the laboratory:

The power stage of the converter does not use conventional 5 V DeMOS devices available in the used technology – instead, stacked 2.5 V IO-devices were used for the power switches in order to be high voltage capable. This work has shown that with a stacked transistor approach higher power conversion efficiencies of the converter are possible. The results were presented in [35].

Another important topic covered during this work was the automatic optimization of the switching time instants of the power switches in the power stage of the converter. Up to now no fast and low power solutions were available in literature.

The goal was to find new concepts in order to minimize body diode conduction durations in the power stage as much as possible. In this work, a robust body diode conduction sensor was developed which is able to detect body diode conduction durations below 1 ns. This sensor opens the opportunity to optimize the dead times of the converter during normal converter operation whereas the whole optimization concept consumes only about 15 μA. Furthermore, it allows a designing of very high frequency converters which operate with automatically optimized switching time instants of the power switches. The developed concept can improve the overall power conversion efficiency of the converter significantly. The results of the body diode conduction sensor have been presented in [34] and the whole dead time optimization concept used in the designed IB DC-DC buck converter was presented in [36].

Since the remaining dead times in the power stage are below 1 ns the gate drivers for the power switches have to be controlled in a very accurate sequence. In order to allow such small dead times two robust high-speed level shifters with very short propagation delays have been developed during this work. The level shifters are the interface between the power domain of the output stage and the core voltage domain. For both level shifters, the propagation delays are below 1 ns over PVT. Furthermore, the level shifters are very voltage tolerant and very robust in design against high frequency volt-

age ringing. The results of the level shifters have been presented in [33].
All concepts and designs are silicon proven. They are used in the designed IB DC-DC buck converter that operates in PWM-DCM – the converter uses a peak current control with automatic frequency hopping and pulse skipping mode.
Another important feature of the implemented converter is that the whole design only occupies $0.088\,\mathrm{mm}^2$ of the chip's area. Only such a small design allows being competitive against linear voltage regulator designs.
Additionally several invention disclosures have been filed during this work. The invention disclosures deal with topics regarding IB DC-DC converters and SC DC-DC converters. A full list of submitted invention disclosures can be found in section 9 on page 111.
A list of my own publications can be found in section 8.
Although the PhD study has taken more than three years there are still questions remaining open. For instance it can be seen that the implemented design has the potential to also provide high power conversion efficiencies at much higher switching frequencies than currently used. Higher switching frequencies would allow reducing the size of the passive components in the input and output filter further.
Another very interesting question is if the automatic dead time concept also works in large discrete power stages designed for load currents up to 100 A. It would also be very interesting to investigate the question if the concept works in PWM-CCM and PFM operation.

8 Own Publications

[C1] **G. Maderbacher**, T. Jackum, W. Pribyl, and C. Sandner. A sensor concept for minimizing body diode conduction losses in DC/DC converters. In *ESSCIRC, 2010 Proceedings of the*, pages 442–445, 2010.

[C2] T. Jackum, **G. Maderbacher**, W. Pribyl, and R. Riederer. Fast capacitor free linear voltage regulator in a 65 nm CMOS technology for supplying digital processor. In *Austrochip*, October 2010.

[C3] T. Jackum, **G. Maderbacher**, W. Pribyl, and R. Riederer. A digitally controlled linear voltage regulator in a 65 nm CMOS process. In *ICECS, 2010 Proceeding of the*, pages 982–985, 2010.

[C4] Thomas Jackum, **Gerhard Maderbacher**, Wolfgang Pribyl, and Roman Riederer. Fast transient response capacitor-free linear voltage regulator in 65 nm CMOS. In *Circuits and Systems (ISCAS), 2011 IEEE International Symposium on*, pages 905 –908, may 2011.

[C5] **G. Maderbacher**, T. Jackum, W. Pribyl, and C. Sandner. Output stage topologies of DC-DC buck converters operating up to 5 V supply voltage in 65 nm CMOS. In *Ph.D. Research in Microelectronics and Electronics (PRIME), 2011 7th Conference on*, pages 105–108, 2011.

[C6] **G. Maderbacher**, T. Jackum, W. Pribyl, S. Michaelis, D. Michaelis, and C. Sandner. Fast and robust level shifters in 65 nm CMOS. In *ESSCIRC (ESSCIRC), 2011 Proceedings of the*, pages 195–198, 2011.

[C7] **G. Maderbacher**, T. Jackum, W. Pribyl, M. Wassermann, A. Petschar, and C. Sandner. Automatic dead time optimization in a high frequency DC-DC buck converter in 65 nm CMOS. In *ESSCIRC (ESSCIRC), 2011 Proceedings of the*, pages 487–490, 2011.

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[C9] T. Jackum, F. Praemassing, **G. Maderbacher**, and W. Pribyl. Capacitorless LVR for a 32-bit automotive microcontroller SoC in 65 nm CMOS. In *ESSCIRC, 2012 Proceedings of the*, pages 329–331, 2012.

[C10] T. Jackum, **G. Maderbacher**, R. Riederer, and W. Pribyl. Output current limitation in a digitally controlled low dropout linear voltage regulator. In *Austrochip*, October 2012.

9 Invention Disclosures

[ID1] **G. Maderbacher**. Body diode conduction sensor. Invention Disclosure, 2009

[ID2] **G. Maderbacher**, and C. Sandner. Body diode conduction sensor. Invention Disclosure, 2009

[ID3] **G. Maderbacher**, C. Sandner, and C. Ahrens. SiP for Switched Mode Circuits. Invention Disclosure, 2010

[ID4] **G. Maderbacher**, S. Marsilli, and W. Hoellinger. Digital Controller for Switched Capacitor DCDC with selectable switching frequency. Invention Disclosure, 2011

[ID5] **G. Maderbacher**, S. Marsilli, and W. Hoellinger. Switched Capacitor DCDC converter Plant implementation digitally programmable. Invention Disclosure, 2011

[ID6] **G. Maderbacher**, S. Marsilli, and W. Hoellinger. Digital Slope Control for Switched Capacitor DCDC converter. Invention Disclosure, 2011

[ID7] **G. Maderbacher**, and C. Sandner. Frequenz-Hopping bei DC-DC convertern fuer erhoehte EMV-Anforderungen. Invention Disclosure, 2011

[ID8] **G. Maderbacher**, and C. Sandner. Totzeit-Optimierung bei DC-DC Konvertern Invention Disclosure, 2011

[ID9] **G. Maderbacher**, and T. Jackum. EMV Verbesserung bei DC-DCs durch verlustfreies Glaetten der Strom- und Spannungsverlaeufe Invention Disclosure, 2011

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