Fully Integrated Low Power and Low Drop DC/DC Converters

Dipl.-Ing. Stefan Gruber

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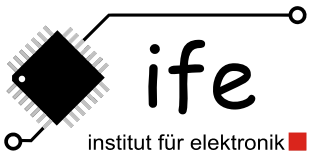

Institute of Electronics

Supervisor: _____

Univ.-Prof. Dipl.-Ing. Dr.techn. Wolfgang Pribyl

Co-Supervisor: _____

Prof. Dr.-Ing. Yiannos Manoli

Graz, November 2011

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Abstract

Wireless Sensor Nodes (WSNs) are an emerging technology with a wide range of applications. Different types are presented in literature or sold by companies. The principle is always similar: A self-sustained sensor is deployed to provide or route information to a different location. One major issue is the availability of energy to supply the WSN. This conflicts with the claim of extending the functionalities of sensor nodes, as demanded by the market. To accomplish this requirement, chip designers have to reduce the current consumption of the individual blocks of the sensor node and increase the efficiency of the power management.

Three different chapters discuss unique regulator architectures and a power management unit. These implementations address a variety of requirements demanded by the different power sources and operational units used for WSNs. This thesis presents implementation details and general considerations on the design of voltage regulators dedicated to WSNs having load currents in the microampere range. State-of-the-art circuits are analyzed for their adaptability to ultra-low power implementations. Whenever traditional approaches cannot be used, new circuit concepts are presented. In addition to details on circuit level, novel system design concepts are also introduced.

As an application example, a rich-featured WSN dedicated to, but not exclusively designed for, an in-tire Tire Pressure Monitoring System (TPMS) is presented. After an introduction of the various building blocks, the power management of this sensor node is discussed. Special attention is given to the voltage regulators required to provide the necessary supply voltages for the Integrated Circuit (IC). As WSNs operate in a harsh environment, the power management has to perform reliably. Whereas this usually conflicts with reducing the current consumption, this thesis presents novel circuits which operate in the automotive environment ($-40\,°C$ to $125\,°C$) and still require only a few nanoamperes.

In addition to a highly efficient DC/DC conversion, fast dynamic response times of the regulators are also required. To follow this requirement, a novel voltage regulator is presented. A Switched Capacitor (SC) regulator is combined with a linear regulator. The SC regulator provides the highly efficient DC/DC conversion, while the fast dynamic response is achieved by the linear regulator. Both regulators operate in parallel, but the linear regulator is disabled by default. It only operates if a fast dynamic response is required. The current consumption of the building blocks is below 150 nA to keep the efficiency high. To achieve this low current consumption, bias currents down to 1 nA are used. The efficiency of this regulator is up to 20 % higher than the one a conventional linear regulator provides.

Some power sources used for WSNs generate voltage levels too low to supply the IC. This thesis presents two different boost converters which utilize the SC approach. One generates a constant output voltage whereas the other one enters a periodic operation to reduce the current consumption during low input voltages. The input voltage has to be at least 0.52 V even if the output voltage is 1.2 V.

All discussed circuits have been fabricated in an Infineon 0.13 µm low-cost CMOS process. The obtained measurement results support the theory and the simulation results presented in this thesis.

Kurzfassung

Wireless Sensor Nodes (WSNs) erfuhren in den letzten Jahren eine große Verbreitung. Eine große Anzahl verschiedener Sensorknoten wurden in einschlägiger Literatur publiziert und von Firmen zum Kauf angeboten. Das Prinzip ist immer ähnlich: Ein autarker Sensorknoten wird platziert, um Information zu sammeln und zu verteilen. Da keine Energieversorgung über Stromleitungen möglich ist, müssen diese Sensoren mit möglichst wenig Energie auskommen. Der Markt fordert aber immer mehr Funktionen des Sensorknotens. Deshalb muss der Stromverbrauch der integrierten Schaltung reduziert werden. Der Entwickler kann dazu die Effizienz der Spannungsregler des Leistungsmanagements erhöhen und den Stromverbrauch der individuellen Schaltungsblöcke reduzieren.

In drei verschiedenen Kapiteln werden verschiedene Spannungsregler vorgestellt. Diese Spannungsregler werden den verschiedenen Anforderungen, welche sich durch die unterschiedlichen Energiequellen für WSNs ergeben, gerecht. Bei der Implementierung der Schaltungen liegt das Augenmerk auf der Reduktion des Stromverbrauchs. Dazu werden Schaltungen, die dem neuesten Stand der Technik entsprechen, analysiert. Es wird untersucht wie sich diese Strukturen für den Betrieb am Sensorknoten eignen. Zusätzlich werden gänzlich neue Schaltungskonzepte vorgestellt, die immer dann Anwendung finden, wenn traditionelle Schaltungen nicht mehr die gewünschten Eigenschaften erzielen.

Als Anwendungsbeispiel wird ein Sensorknoten für *Tire Pressure Monitoring Systems (TPMSs)* mit den notwendigen Schaltungsblöcken vorgestellt. Der Fokus liegt dabei auf den unterschiedlichen Spannungsreglern, die für das Leistungsmanagement benötigt werden. Da Sensorkonten oft in einer rauen Umgebung arbeiten, benötigen sie zuverlässige Schaltungen. Dies steht oft im Widerspruch zur Reduktion des Stromverbrauches. In dieser Arbeit werden Schaltungen vorgestellt, die in der Automotive-Umgebung ($-40\,°C$ bis $125\,°C$) zuverlässig arbeiten und trotzdem nur wenige Nanoampere benötigen.

Die Spannungsregler müssen nicht nur eine effiziente Spannungsumsetzung ermöglichen, sondern sie müssen auch ein schnelles Regelverhalten zeigen. In dieser Arbeit wird eine neuartige Kombination aus einem *Switched Capacitor (SC)* Regler und einem Linearregler präsentiert, welche beide Anforderungen erfüllt. Während des Normalbetriebs ist der Linearregler ausgeschaltet. Kann der SC Regler die benötigte Leistung nicht zur Verfügung stellen, beginnt der Linearregler automatisch zu arbeiten. Der Gesamtstromverbrauch des Reglers liegt unter 150 nA. Dazu werden Biasströme in der Größe von 1 nA verwendet. Die Effizienz des Reglers ist bis zu 20 % höher als jene eines konventionellen Linearreglers.

Manche Energiequellen die für die WSNs verwendet werden, liefern eine niedrigere Spannung als zur Versorgung des Sensorknotens notwendig ist. Um die Eingangsspannung entsprechend hochzusetzen, werden SC Schaltungen verwendet. Es werden zwei verschiedene Konzepte vorgestellt. Während ein Regler eine konstante Ausgangsspannung liefert, arbeitet der andere periodisch, um bei kleinen Eingangsspannungen die Stromaufnahme zu reduzieren. Bei einer Ausgangsspannung von 1.2 V kann die Eingangsspannung so bis auf 0.52 V reduziert werden.

Alle vorgestellten Schaltungen wurden in einem Infineon 0.13 µm CMOS Prozess gefertigt und anschließend vermessen.

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Stefan Gruber

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Acronyms

ABS	Anti-lock Braking System
AC	Alternating Current
AC/DC	Alternating Current to Direct Current
ADC	Analog to Digital Converter
ADI	Analog to Digital Interface
BAW	Bulk Acoustic Wave
CAD	Computer-Aided Design
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital to Analog Converter
DC	Direct Current
DC/DC	Direct Current to Direct Current
EMI	Electromagnetic Interference
EPC	Electronic Product Code™
ESC	Electronic Stability Control
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transformation
FIB	Focused Ion Beam
FOM	Figure of Merit
GFT	General Feedback Theorem
HF	High Frequency
IC	Integrated Circuit
IQ	In-phase/Quadrature
LTI	Linear and Time-Invariant
MEMS	Micro-Electromechanical System
MIM	Metal-Insulator-Metal
MOS	Metal Oxide Semiconductor
NMOS	n-channel MOSFET
NTC	Negative Temperature Coefficient
OTA	Operational Transconductance Amplifier
PMOS	p-channel MOSFET

PMU	Power Management Unit
PSRR	Power Supply Ripple Rejection
PTAT	Proportional to Absolute Temperature
PTC	Positive Temperature Coefficient
RF	Radio Frequency
RFID	Radio Frequency Identification
SC	Switched Capacitor
SCM	Self-cascode MOSFET
SOC	System on Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
SR	Slew Rate
STI	Shallow Trench Isolation
TPMS	Tire Pressure Monitoring System
UGF	Unity Gain Frequency
(U)HF	(Ultra) High Frequency
UHF	Ultra High Frequency
WSN	Wireless Sensor Node

Chapter 1

Introduction

> The beginning of knowledge is the discovery of something we do not understand.
>
> *(Frank Herbert)*

1.1 The Need for Ultra-low Power Power Management (Motivation and Problem Statement)

As proposed by M. Niedermayer in [58]: To be competitive and to reach a large market potential, the development costs of Wireless Sensor Nodes (WSNs) need to be cost-efficient. These costs are mainly formed by the manufacturing costs and by the Integrated Circuit (IC) costs. IC costs can be minimized by feature size reduction and increasing the yield in production. Manufacturing costs are decreased by simplification of the assembly and by reducing the off-chip devices. Developing fully integrated Systems on Chips (SOCs) seems to be the future approach. If the power consumption of the IC is minimized, it is even possible to integrate the battery, which is used to supply the node [78]. WSNs down to a few cubic millimeters using 3D stacking technology are already available [14]. From science's point of view the topic of fully integrated WSNs is quite challenging. This field offers a lot of open research fields and open tasks.

As discussed in [3], WSNs are classified by different applications. These applications have different requirements concerning the design and the implementation of the sensor. They have in common that they suffer from limited energy. This limitation requires new techniques in the power management. On the one hand the power consumption of the power management itself has to be reduced and on the other hand the power or the energy gathered from the power supply needs to be distributed in an efficient manner.

The reduction of the current consumption of the power management leads to more noise, less bandwidth and thus to worse load and line regulation capabilities of the regulators used for the power management. This work presents techniques on how to cope with these effects and provides design solutions. To manage the limited current budget, new design concepts are found as well as traditional methodologies are adapted to suit the new requirements.

This thesis refers several times to *ultra-low power* designs and approaches. In literature ultra-low power is defined differently. Unless noted otherwise, in this thesis ultra-low power is referred

to as an overall power dissipation of a functional block (for instance a temperature sensor or a digital control circuit) of 10 µW and below. Individual building blocks, like reference cells, oscillators, or voltage level detectors usually have a power dissipation of 50 nW and below. Tail currents* down to one nanoampere are used.

The first chapter introduces the topic of ultra-low power regulator design. Well known design concepts are analyzed for their suitability to fully integrated WSNs. Problems arising when the power consumption is reduced are discussed. Design challenges as well as simulation and measurement methodologies are presented.

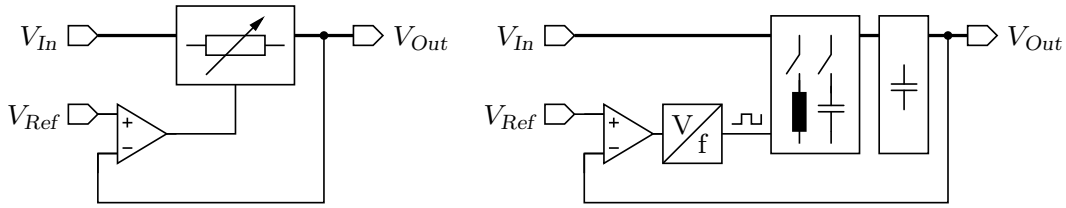
The main part of the thesis discusses implementation details of regulators used in ultra-low power designs. These regulators provide a stable supply voltage for circuits having current consumptions from several microampere to several milliampere. The power supplies, which are used to supply WSNs, are very different in their characteristics. So voltage regulators capable of voltage sources with an output voltage up to 3.3 V and sources having an output down to 0.5 V are discussed. Additionally, the presented regulators face input voltage transient speeds considered to be slow as well as fast transients. Clearly, these requirements need different regulator implementations. The main part is divided into three parts:

Chapter 2 – Power Management for an Ultra-low Power Wireless Sensor Node
This chapter presents the power management which has been implemented for a WSN dedicated to in-tire Tire Pressure Monitoring Systems (TPMSs). The design of the chip is done in a way which allows the IC to operate in different application scenarios as well. The sensor can be supplied by three different power sources and consists of four power sinks from the power management's point of view. Besides detailed analysis of the behavior of the power management, four different voltage regulators are presented in detail. The chapter gives insight into design issues and implementation details and concludes with measurement results. Comparisons to state-of-the-art implementations are also given.

Chapter 3 – A Robust and Fault Tolerant Switched Capacitor Regulator
The power management presented in Chapter 2 provides no efficient conversion of the input voltage of the WSN. This chapter introduces a Switched Capacitor (SC) voltage regulator. The conversion efficiency of the power management is improved and thus the lifetime of the WSN. As fully customized implementations are not preferable, the regulator supports many different power sources used for WSNs with a supply voltage range of 1.35 V to 3.3 V. The nominal load current is 1 µA and the output voltage is 0.8 V. The regulator adapts itself to higher load current demands. For this regulator innovative analog blocks are designed and compared to recent publications. The measurement results of the regulator presented at the end of this chapter are comparable to recently published similar works.

Chapter 4 – Voltage Regulators for Low Input Voltages
Some power supplies used for WSNs provide a nominal voltage below the voltage required to power the IC. This chapter presents two solutions to solve this issue: Whereas one approach is a straightforward implementation, the other one tries to minimize the current

* A tail current is the current which exists at the source of a transistor.



(a) Linear regulator (b) Switched regulator

Figure 1.1: Basic linear and switching regulator circuits [74]

	Linear Regulator	Switched Capacitor	Switched Inductor
Efficiency	Lowest	Low	Highest
Cost	Lowest	Low	Highest
Dynamic response	Fastest	Slowest	Fast
Load current	Low to High	Low	High
Fully integrated	Yes	Yes	No*

*A few fully integrated solutions are published (i.e. [89, 91]).

Table 1.1: Comparison of different DC/DC converter topologies [28]

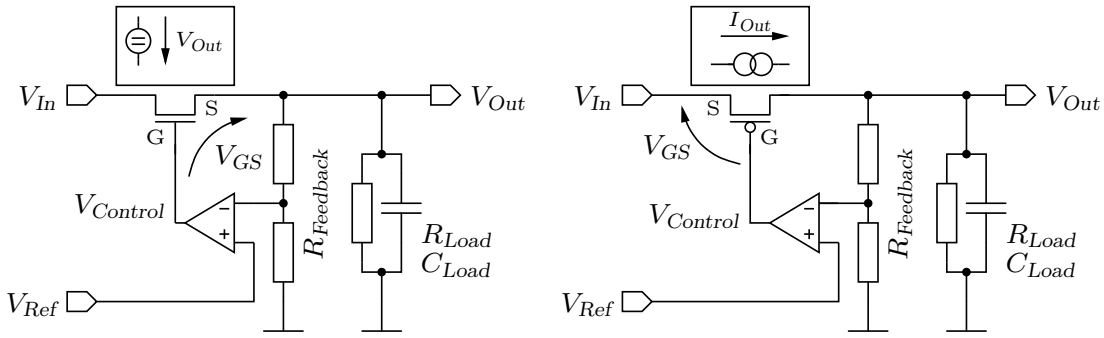
requirements on low input voltages. The minimization is achieved by a periodic operation of the regulator.

1.2 Introduction to Linear and Switched Regulators

Gabriel Alfonso Rincón-Mora defines voltage regulators in his book *Analog IC Design with Low-Dropout Regulators* [74]:

> A regulator generates and regulates accurate and stable output voltages that are impervious to variations in the input supply, loading environment, and various operating conditions. Unlike references, regulators supply substantial DC currents. Regulators also protect and filter ICs from exposure to voltages exceeding junction-breakdown levels.

Voltage regulators are classified as: (1) linear and (2) switched regulators. Linear regulators make use of a resistive device in series (pass device) as shown in Figure 1.1a. The resistance is adjusted to set the desired output voltage. In CMOS technology an NMOS or a PMOS transistor is used as pass device. Switched regulators make use of an energy storage device like inductors or capacitors as illustrated in Figure 1.1b. A switch enables or disables the current flow through this device. Switching regulators first convert DC into AC and afterwards back to DC. At the output a filter is required.



(a) NMOS regulator (b) PMOS regulator

Figure 1.2: Block diagram of the NMOS and the PMOS regulator

Each type of regulator has specific advantages and disadvantages. A comparison of these parameters is shown in Table 1.1. This thesis has the focus on fully integrated ultra-low power solutions. So, only linear and SC regulators are presented.

The next paragraphs revise the basic theory of fully integrated regulators. The presentation is done differently compared to actual literature. Design issues arising from to the need of low currents are discussed. General solutions and design considerations for DC/DC converters in the ultra-low power domain are presented.

1.2.1 Linear Regulators in CMOS Technology

Linear regulators used for ICs in CMOS technology have a wide range of applications. Especially whenever a stable and low noise supply voltage is required, linear regulators are in favor. Depending on the pass device type, two regulator categories are distinguished: (1) PMOS regulators, and (2) NMOS regulators.

NMOS Regulators

Figure 1.2a shows the block diagram of an NMOS regulator. To achieve an output voltage (V_{Out}) mostly independent of external influences, an error amplifier is used which adjusts the gate of the pass device ($V_{Control}$). The advantage of this implementation is the low output impedance of the NMOS transistor. Usually, stabilization of the feedback is easy and the output is rather insensitive to input voltage variations. These advantages make this architecture preferable for low power implementations, since the error amplifier can be very simple. Despite these advantages the architecture has a major drawback. The gate voltage ($V_{Control}$) of the pass device needs to be at least one threshold voltage higher than the output voltage of the regulator. If the input voltage of the regulator is lower than $V_{Out} + V_{Th}$, the required gate voltage is not available. Thus an input voltage multiplication circuit is necessary to generate $V_{Control}$. Usually, a charge pump is used for this multiplication. Depending on the regulator

requirements the charge pump can either supply the error amplifier [29, 94] or the gate of the pass device [11, 25, 26, 37].

PMOS Regulators

The block diagram of the PMOS regulator shown in Figure 1.2b is similar to the NMOS block diagram in Figure 1.2a. Here the pass device is formed by a PMOS transistor. The PMOS device has a high output impedance and operates as current source. Clearly, stabilization and regulating the pass device is more sophisticated than for the NMOS type. So PMOS regulators are not the ideal solution for lower power implementations. As $V_{Control}$ is always smaller than the input voltage, this architecture is advantageous if the input and the output voltage of the regulator are in the same region.

Low-dropout Recovery Problem

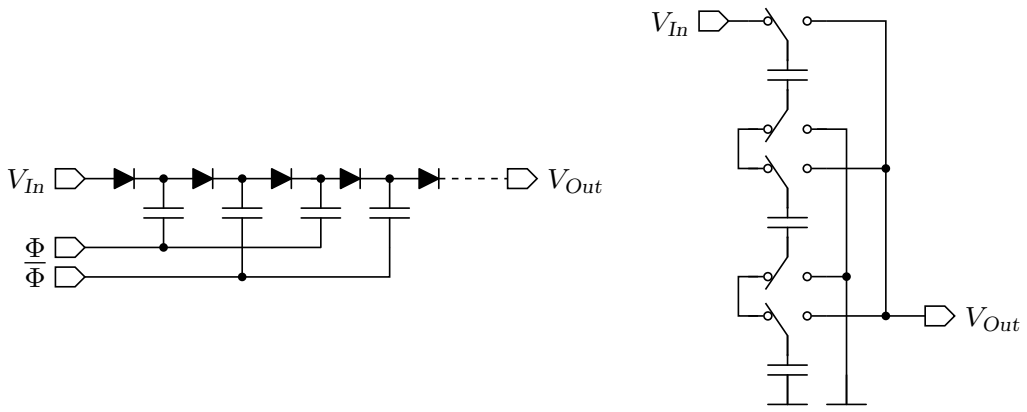
Linear regulators, as shown in Figure 1.2, suffer from the so-called low-dropout recovery problem. PMOS and NMOS regulators are affected similarly. For the PMOS type, the gate of the pass device is at a very low level when the regulator is in low-dropout mode. If the input voltage is rising fast, the gate voltage of the pass device must also rise fast. Otherwise, overshoots on the output voltage occur. Especially for ultra-low power implementations this is a serious problem as the high current required for a fast rising gate voltage is not available. The most effective solution (besides a large off-chip capacitor) is to ensure that the gate voltage of the pass device is always higher than a certain limit. For the NMOS regulator, it is necessary to keep the gate voltage below a certain limit.

Regulation of the Output Voltage

The presented architectures make use of an error amplifier to adjust the gate potential of the pass device for different input, output, and environmental conditions. If the output voltage of the regulator must not be very accurate, the feedback can be omitted. In this case it is for instance possible to supply the gate of the pass device with a reference voltage. This reference voltage can be dependent on various parameters like temperature or load current to achieve a more or less independent output voltage of the regulator.

1.2.2 SC Regulators in CMOS Technology

SC regulators provide a power efficient DC/DC conversion. According to [45], SC regulators can be categorized into three different types: (1) step-down (or buck) converters, (2) step-up (or boost) converters, and (3) step-down-step-up (or buck-boost) converters. The most famous implementation of step-up converters are charge pumps, like the Dickson charge pump presented in [17] and shown in Figure 1.3a. Step-down converters usually alternatingly switch capacitors in series or parallel. Figure 1.3b shows a step-down converter which divides the



(a) Step-up Converter (Dickson charge pump) (b) Step-down converter

Figure 1.3: Basic SC regulator architectures

input voltage by three. To achieve a highly efficient voltage conversion, a certain capacitor size or oscillator frequency is necessary. Otherwise, the necessary charge cannot be provided by the SC circuit.

If on-chip capacitors are used, the efficiency is lower than by using off-chip devices [56]. One reason is that on-chip capacitors are limited to several hundred picofarad in their size, while off-chip capacitors can have a size of several microfarad. Using off-chip capacitors allows conversion efficiencies higher than 90 % [42, 95]. For on-chip implementations, the achieved efficiency strongly depends on the load current. If the load is in the milliwatt range, the efficiency is about 50 % to 80 % [9, 43, 62]. For low power circuits delivering load currents in microampere range the efficiency is about 70 % [5, 6, 34, 39, 67, 92]. If the load current is reduced to below one microampere, the efficiency drops below 60 % [92]. To achieve the optimum efficiency, the charge transferring capacitors and the clock frequency need to be optimized. For SC regulators in the microwatt range and below, the current consumption of the oscillator is one of the limiting factors in the achievable efficiency.

1.3 Challenges in the Analog Design of Ultra-low Power Circuits

Reducing the current consumption of a circuit results in less speed and more noise. These parameters fundamentally depend on the current and cannot be influenced beyond a certain value unless the power is increased. Besides the decrease of the speed and the increase of the noise other challenges arise if the current consumption in analog circuits is decreased to a few nanoamperes. The most critical problems designers have to be aware of are discussed in this section.

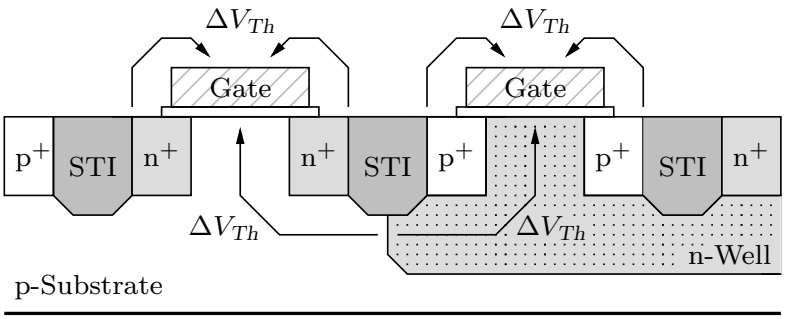


Figure 1.4: Cross section of the CMOS process showing the STI stress and well proximity effect

1.3.1 Parasitic Capacitors

For ultra-low power circuits, capacitive loads become a serious issue. Loading a capacitor of only 100 fF with a current of 10 nA to 1 V already requires 10 µs. So capacitive loads need to be avoided. The lower the current consumption gets the more important the layout becomes. Parasitic capacitors generated by wires routed in parallel can slow down a circuit significantly. Modern Computer-Aided Design (CAD) tools allow the extraction of the layout of an IC to obtain parasitic capacitors generated due to the layout. As the layout is generated very late in the design process, the designer already has to estimate the parasitic capacitors in the schematic based view. Experience is essential for this estimation process.

1.3.2 Weak Inversion

In ultra-low power designs tail currents of 10 nA down to 1 nA or even below that value are typical values. Usually, this current is too small to operate a transistor in the strong inversion region. A typical current mirror in an ultra-low power design operates in weak inversion, unless the length of the transistor is increased to an unreasonably large value. According to [88], the drain current of a transistor in weak inversion can be estimated using (1.3.1). I_{DO} is the specific current of a transistor, W/L are its dimensions, V_{GS} is the gate-source voltage, V_{Th} is the threshold voltage, n is the slope factor, and V_T is the thermal voltage.

$$I_D = I_{D0} \cdot W/L \cdot \mathrm{e}^{\frac{V_{GS}-V_{Th}}{n \cdot V_T}} \tag{1.3.1}$$

(1.3.1) shows that the drain current grows exponentially as a function of the threshold voltage of the transistor. So matching becomes very important to keep differences in threshold voltage small. In the layout Shallow Trench Isolation (STI) stress and the well proximity effect influence the threshold voltage of a transistor [18]. Both effects are illustrated in Figure 1.4. As the influence is unknown before the layout is available, these effects require post-layout simulation. To minimize these influences, common centroid and similar layout matching techniques are unavoidable [76].

Not only the threshold voltage has a high impact on the drain current, but also the gate-source voltage is important. Due to the low current, analog circuits have high ohmic nodes

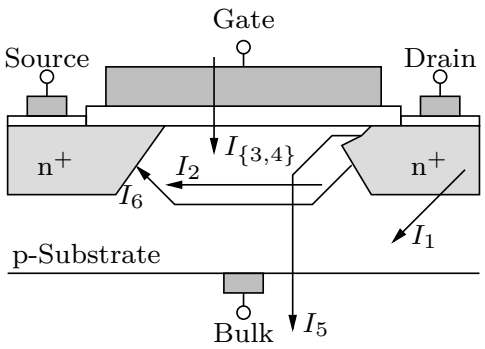


Figure 1.5: Leakage currents mechanisms of deep submicron transistors according to [75]

in the gigaohm region. These nodes are very sensitive to crosstalk. So distortions have to be avoided.

Of course, source degeneration reduces the sensitivity of the current mirror. (1.3.2) shows the transconductance of the degenerated transistor. If R_{Source} is increased, transconductance and thus the sensitivity decreases. As this technique requires a large ohmic resistor which increases the chip size and the complexity of the layout, it is often not feasible.

$$\widetilde{g}_m = \frac{g_m}{1 + R_{Source} \cdot (g_m + g_{mbs} + g_{ds})} \tag{1.3.2}$$

1.3.3 Leakage Currents

The performance of MOS transistors suffers from leakage currents. According to [75] the most significant leakage mechanisms are (refer also to Figure 1.5):

- pn-junction reverse-bias current (I_1): Currents which leak through reverse biased pn-junctions.
- Subthreshold leakage (I_2): If the gate-source voltage of the transistor is smaller than the threshold, it operates in the subthreshold region. The current which occurs is caused by six different phenomena (weak inversion effect, drain induced barrier lowering, body effect, narrow width effect, effect of channel length, and temperature) [55].
- Tunneling into and through gate oxide (I_3): The thin gate oxide leads to a high electromagnetic field, which results in tunneling electronics from or into the substrate.
- Injection of hot carriers from substrate to gate oxide (I_4): Due to the high electric field near the gate oxide, electrons gain enough energy to cross the interface barrier into the oxide layer.
- Gate-induced drain leakage (I_5): If the transistor is in accumulation mode and the negative gate bias is large (large voltage difference between gate and drain), the drain region under the gate can be depleted or even inverted. Caused by different effects

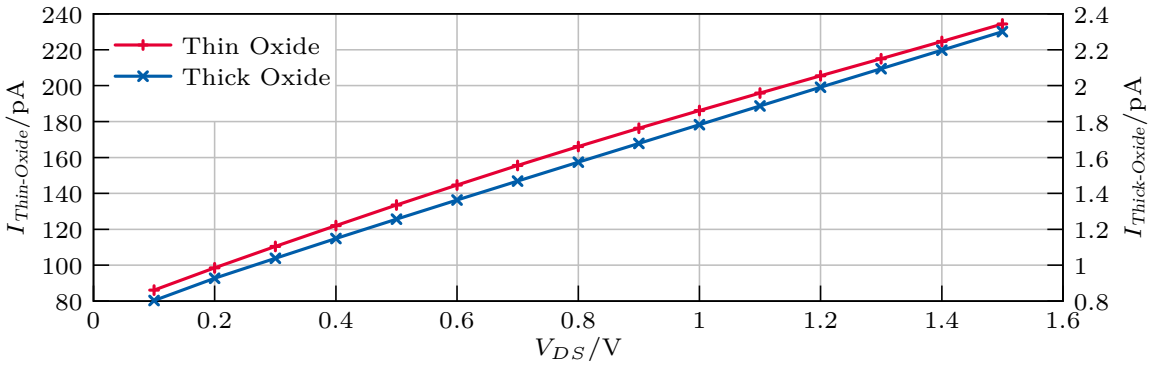


Figure 1.6: Comparison of the leakage current of a thick oxide and a thin oxide NMOS transistor at 27 °C and $V_{GS} = 0\,\mathrm{V}$

(e.g. avalanche multiplication and band-to-band tunneling) minority carriers are emitted underneath the gate and drawn into the substrate.

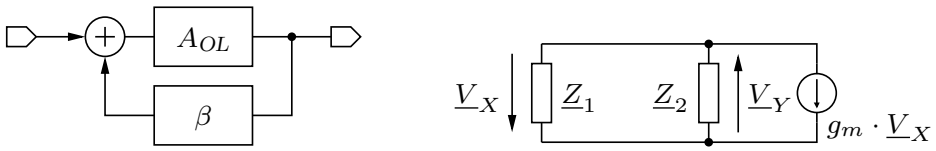
- Punchthrough (I_6): In short channel devices the depletion regions of drain and source are close to each other. At a high drain source voltage the two depletion region merge. Punchthrough has taken place. In this state, majority carriers in the source enter the substrate. Some of them are collected by the drain [55].

If the design is not done carefully, the leakage current of one transistor can be in the region of its tail current. Leakage currents can most effectively minimized by reducing the voltage drop across the transistor terminals. Using thick oxide transistors also allows for significant reduction of the gate leakage. The threshold voltage of the transistor has a major impact on the drain leakage current. Figure 1.6 shows the difference between the leakage current into the drain region of a thick oxide with having a large threshold voltage and a thin oxide NMOS transistor having a low threshold voltage in the technology used in this thesis. Concerning leakage the thick oxide device is clearly preferable. As the thick oxide transistor has also disadvantages (e.g. lower mobility or larger minimum length), this type cannot always be used.

1.4 Simulation and Measurement Methodology

This chapter summarizes the most challenging problems in the measurement and simulation of ultra-low power circuits, in particular linear voltage regulators. Simulation as well as measurement methodologies are discussed.

Linear regulators are considered as Linear and Time-Invariant (LTI) feedback systems, if they are treated as small-signal models. So, stability of the closed loop needs to be ensured. Various methods to verify stability exist. Here the mathematical approach of one method is presented.



(a) Block diagram of a feedback system

(b) Norton equivalent

Figure 1.7: Feedback system with its Norton equivalent

High ohmic nodes on the IC make it sensitive to crosstalk. This fact has to be considered in measurement. Both measurement and simulation results are affected by the limited current accuracy of the measurement and the simulation setup.

1.4.1 Stability Analysis

Most types of voltage regulators have a built-in negative feedback loop. The loop is required to measure and compare the output voltage of the regulator with a reference voltage. As in any negative feedback system, stability analysis is essential. Depending on the application, different methods to verify the stability of linear systems have been developed (Routh Hurwiz Criterion, Nyquist Criterion, Bode Plot Method, Lyapunov's method, and so on). Not all methods are applicable to ultra-low power designs. This section summarizes the method used for stability analysis in this thesis.

Based on the work published by H. Bode in [8], the transfer function of negative feedback amplifiers is given by (1.4.1).

$$A_{FB}(\jmath\omega) = \frac{A_{OL}(\jmath\omega)}{1 + \beta(\jmath\omega) \cdot A_{OL}(\jmath\omega)} = \frac{A_{OL}(\jmath\omega)}{1 + L(\jmath\omega)} \tag{1.4.1}$$

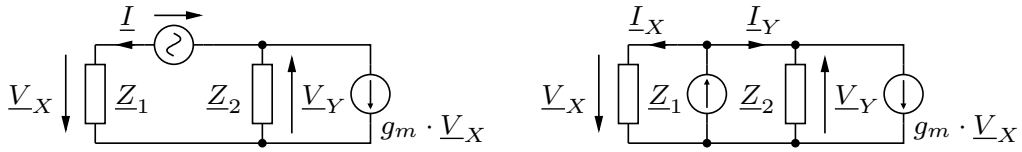
$A_{FB}(\jmath\omega)$ is the gain of the amplifier with feedback, $\beta(\jmath\omega)$ is the feedback factor, and $A_{OL}(\jmath\omega)$ is the gain of the open-loop amplifier. Necessary for stability is that the *phase margin* defined by (1.4.2) of the loop gain at unity gain ($|L(\jmath\omega_{UG})| = 1$) is greater than 0°. The phase margin for linear regulators or buffers is usually designed to be about 60°.

$$PM = \angle L(\jmath\omega_{UG}) - 180° \tag{1.4.2}$$

To determine the loop gain by measurement or by simulation, different methods are used. Here, the *Double-Injection Technique* published by R. D. Middlebrook in [51] is presented. A negative feedback loop as shown in Figure 1.7a can be transformed into a *Norton equivalent* depicted in Figure 1.7b or *Thévenin equivalent*. The loop gain of the equivalent circuit can be calculated using (1.4.3).

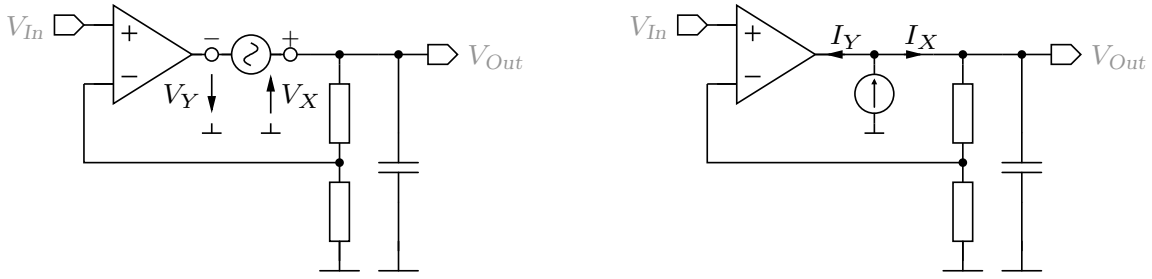
$$L(\jmath\omega) = g_m \cdot \frac{\underline{Z}_1 \cdot \underline{Z}_2}{\underline{Z}_1 + \underline{Z}_2} \tag{1.4.3}$$

The complex impedances $\underline{Z}_1$ and $\underline{Z}_2$ are unknown. To obtain these values and thus the loop gain, the feedback is broken at an injection point. At this point two injections (Figure 1.8) are



(a) Voltage injection (b) Current injection

Figure 1.8: Middlebrook's Double-Injection Technique



(a) Voltage injection (b) Current injection

Figure 1.9: Double-Injection in an OTA feedback loop

done. The resulting transfer functions at this point are calculated or measured. The transfer function using a voltage source as shown in Figure 1.8a can be calculated using (1.4.4a). The transfer function using a current source as shown in Figure 1.8b can be calculated using (1.4.4b). The results in (1.4.4a-b) are combined and plugged in (1.4.3) to get the overall loop gain in (1.4.5). This result is then analyzed in terms of phase margin.

$$T_V(j\omega) = \frac{\underline{V}_Y}{\underline{V}_X} = \frac{\underline{Z}_2}{\underline{Z}_1} + g_m \cdot \underline{Z}_2 \tag{1.4.4a}$$

$$T_I(j\omega) = \frac{\underline{I}_Y}{\underline{I}_X} = \frac{\underline{Z}_1}{\underline{Z}_2} + g_m \cdot \underline{Z}_1 \tag{1.4.4b}$$

$$L(j\omega) = \frac{T_V(j\omega) \cdot T_I(j\omega) - 1}{T_V(j\omega) + T_I(j\omega) + 2} \tag{1.4.5}$$

The described method only works accurately if the signal flow in the loop is unilateral. Reverse transmissions are generated for instance by coupling effects from the drain to the gate of a transistor. A method which accounts for reverse gain effect is proposed by M. Tian in [80]. Also, R. D. Middlebrook developed a more general method, the General Feedback Theorem (GFT), which allows complete analysis of feedback circuits [52]. As reverse transmissions usually occur at frequencies much higher than the Unity Gain Frequency (UGF), they are negligible in stability analysis. The resulting loop gain is independent of the location of the injection point in the loop as long as the direction and the orientation of the current and voltage probes with respect to the loop is ensured.

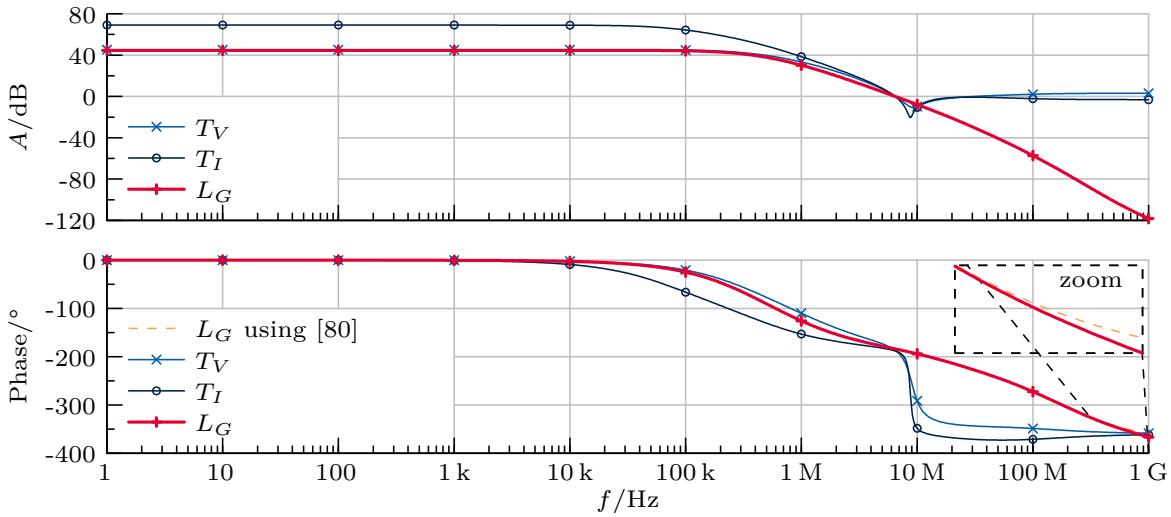


Figure 1.10: Bode plot showing the different transfer functions of an OTA in negative loop

For illustration an Operational Transconductance Amplifier (OTA) used in a closed negative feedback is analyzed. For the OTA a real model of an implemented amplifier is used. As shown in Figure 1.9, the feedback is broken and current and voltage injections are done. The respective transfer functions T_V and T_I at the injection point are plotted in Figure 1.10. The overall transfer function L_G is calculated using (1.4.5). For comparison the result of the method proposed by [80], which accounts for reverse feedback effects, is also shown.

Modern simulation tools provide the Double-Injection Technique. The user has to specify the injection point and the tool automatically runs two simulations – current injection and voltage injection. With the results of both simulations the loop gain is calculated.

1.4.2 High Ohmic Nodes

The gate of an MOS transistor is high ohmic. So CMOS circuits are sensitive to crosstalk at the input. For circuits having only a few nanoamperes tail current, the output is also high ohmic. The resistance of the channel of a transistor having a drain current of 1 nA is in the gigaohm region. So ultra-low power circuits have a lot of Electromagnetic Interference (EMI) sensitive nodes. This sensitivity requires caution when measuring the IC in the lab. On-chip buffers and decoupling networks are required to get accurate measurement results.

1.4.3 Current Accuracy

As discussed in Chapter 1.4.2, measuring ultra-low power circuits requires decoupling networks because of the high sensitivity to crosstalk. Therefore, off-chip capacitors are used for the measurement setup. As evaluated by measurement, these decoupling capacitors have leakage

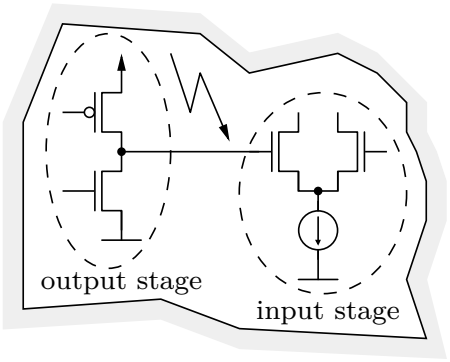


Figure 1.11: EMI sensitive nodes in ultra-low power designs

currents in the range of a few nanoamperes. Of course, these currents need to be determined by a preliminary measurement of the decoupling network.

Not only the measurements need to be verified, but the simulation results also need special attention. When simulating ultra-low power circuits, the simulator's default settings need to be revised. Simulation Program with Integrated Circuit Emphasis (SPICE) simulators usually terminate open nodes automatically with resistors to ensure convergence. Additionally, a resistor is added across nonlinear components [38]. It is necessary to ensure that these resistors have a sufficiently large value, especially when using post-layout extracted circuits. When simulating SC circuits, large current peaks appear during the switching period. These peaks are several decades larger than the average current of the circuit. To get an accurate current profile, the parameters of the simulator setting the accuracy need to be tightened.

1.5 Performance Parameters of Linear Regulators

Voltage regulators are characterized by different performance parameters and key figures. As such a regulator is a complicated system operating in different modes and conditions, a large number of parameters are required to describe the performance. Depending on the field of application, different specifications are decisive. This chapter summarizes the most important parameters including their definitions used for ultra-low power linear regulators. The focus is on power consumption and related parameters, whereas regulation accuracy or similar specifications have minor attention. Figures which affect CMOS circuits in general, like active area size, are not discussed.

Operation Regions

The operating regions define the possible input voltage range of the regulator with respect to the output voltage. It is common to distinguish between three different operation regions:

1. Linear operation,

2. Low-dropout operation, and

3. Below low-dropout operation.

The different operating modes are determined by the operating region of the pass device. As long as the input voltage is high enough to operate the pass device in the saturation region, the regulator is in linear operation. As soon as the input voltage drops to a level in which the pass device operates in the linear region, low-dropout operation is entered. This region is also referred to as low-gain mode, as the loop gain of the regulator is lowered [74]. Especially for NMOS type regulators, achieving low-dropout operation requires some effort. If the input voltage of the regulator drops below the output voltage, it is below low-dropout operation. Linear regulators require an additional switched regulator to operate in below low-dropout operation.

(Energy)efficiency and Power Consumption

For low power implementations, the power and the energy consumption of the regulator is essential. One design goal is always to optimize the current consumption of the regulator itself. Energy consumption is important for periodically operated circuits.

The performance of a DC/DC conversion is defined by the conversion efficiency. It is defined by the power delivered to the load of the regulator divided by the power taken by the regulator from the power source (1.5.1). The theoretical limit of the efficiency is calculated using (1.5.2a). For linear regulators, the limit is the ratio of the output voltage to the input voltage. For the sake of completeness, the equation for the maximum achievable efficiency for SC regulators is shown in 1.5.2b. The maximum depends on the input voltage and the output voltage ripple (ΔV_{Out}).

$$\eta = \frac{P_{Out}}{P_{In}} \cdot 100\,\% = \frac{V_{Out} \cdot I_{Out}}{V_{In} \cdot I_{In}} \cdot 100\,\% \tag{1.5.1}$$

$$\eta_{Linear} \leq \frac{V_{Out}}{V_{In}} \cdot 100\,\% \tag{1.5.2a}$$

$$\eta_{SC} \leq \frac{1}{1 + \dfrac{\Delta V_{Out}}{V_{In}}} \tag{1.5.2b}$$

For some implementations, the energy efficiency is also an important parameter. Here the energy consumption ratio is used (1.5.3).

$$\eta_E = \frac{E_{Out}}{E_{In}} \cdot 100\,\% = \frac{\displaystyle\int_{t_1}^{t_2} P_{Out}(t)\,dt}{\displaystyle\int_{t_1}^{t_2} P_{In}(t)\,dt} \cdot 100\,\% \tag{1.5.3}$$

As long as no boundary conditions are listed, the power and the energy efficiency are at nominal conditions.

Transient Characteristics

In the time domain the transient response time of the regulator is important. Various cases are distinguished:

- Startup settling time: Time from enabling the regulator until the output voltage is stable
- Load pulse settling time: Time from load pulse occurrence until the output voltage is stable again
- Maximum input Slew Rate (SR): Fastest input voltage transient (rising or falling) which does not affect the output voltage noticeable.

These parameters can be summarized by the so-called line and load regulation capabilities of the regulator.

Small Signal Parameters

Small signal parameters describe the regulator performance in its operating point. In addition to typical amplifier parameters like bandwidth or gain, Power Supply Ripple Rejection (PSRR) (not to be confused with Power Supply Rejection Ratio which is also abbreviated using PSRR [74]) and the output resistance are used.

PSRR describes how the output voltage changes on input voltage ripples. The value usually depends on the frequency of the input voltage.

$$\mathrm{PSRR} = \frac{\partial V_{In}}{\partial V_{Out}} \tag{1.5.4}$$

The output resistance describes how the output voltage changes if the load current is changed.

$$r_{Out} = \frac{\partial V_{\mathrm{Out}}}{\partial I_{\mathrm{Load}}} \tag{1.5.5}$$

Stabilization method

In analog chip design a major design goal is to keep everything on-chip or at least in-package. For stabilization purposes, sometimes large capacitors are required which cannot be fully integrated. So the method of stabilization becomes crucial. An important performance criterion is whether the stabilization is done internally or externally, and if externally, which type of off-chip capacitors can be used. In literature the terms “capacitor-less” [40] or “capacitor-free” [35] compensation techniques are used. These terms refers to stabilization techniques using no off-chip capacitors. On-chip capacitors are still in use.

Chapter 2

Power Management for an Ultra-low Power Wireless Sensor Node

> It is amazing what you can accomplish
> if you do not care who gets the credit.
>
> *(Harry S. Truman)*

2.1 Tire Pressure Monitoring Systems

The following chapter is mainly taken from [30, 31] (own publications). ■

This chapter presents a Wireless Sensor Node (WSN) dedicated to Tire Pressure Monitoring Systems (TPMSs). The purpose of a TPMS is to acquire the pressure in the tire of a car or a truck. An alarm is triggered if the pressure in one or more tires is too low. In the United States of America TPMSs are already mandatory for new cars. The European Commission has also announced that it will make TPMSs mandatory for all new cars by 2012 [21]. TPMSs improve safety and reduce CO_2 emissions caused by increased fuel consumption due to under-inflation [21].

By now two different systems can be distinguished [10]: (1) Indirect systems do not require dedicated sensors. Parameters extracted from the Anti-lock Braking System (ABS) and the Electronic Stability Control (ESC) are used to estimate the pressure in the tires. The main advantage of this approach is that it is inexpensive and easy to implement. The required calibration is of course a major drawback. (2) Direct systems use dedicated sensors in the tires to measure the pressure directly. The data is transmitted using an active transmitter. Direct systems are more expensive than indirect systems. However, providing additional features makes them advantageous compared to indirect systems.

After an introduction to the WSN in Chapter 2.2, Chapter 2.3 gives insight into the power management of the sensor node. The various power supplies and the operating modes of the Integrated Circuit (IC) are explained. Chapters 2.3.2 through 2.3.5 introduce the voltage regulators supplying the different blocks on the IC. Section 2.4 concludes Chapter 2.

This work has been partly funded by the Austrian Research Promotion Agency (FFG) within the project *iTire*.

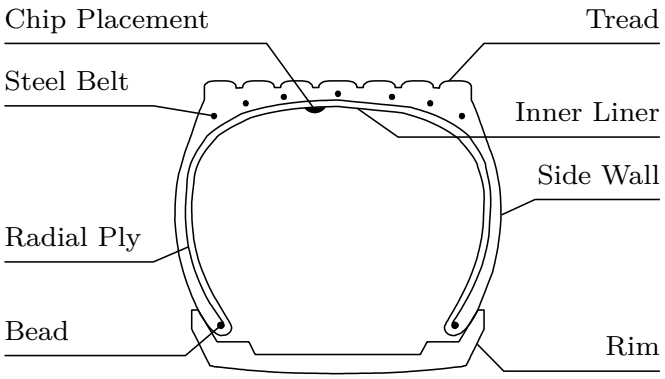


Figure 2.1: Simplified scheme of a tire showing the estimated chip placement position

2.2 Wireless Sensor Node

The WSN presented in this chapter is designed within a collaboration of Graz University of Technology and Infineon Technologies Austria AG and is published in [30] (own publication). Follow up publications of the system or details on some blocks of the WSN are [27, 29, 31, 69–73]. My contribution to this work is the design of the on-chip voltage regulators and assisting in designing the power management and the top-level. Additionally, I provided some of the measurement setups, as published in [32], and measurement results. ■

The WSN presented in this chapter is dedicated to but not exclusively designed for a direct TPMS. Although the main purpose of the WSN is temperature and pressure monitoring in a tire, it can also be used in different applications like healthcare monitoring.

According to [24]:

> State-of-the-art direct TPMSs are WSNs mounted on the rim. Attaching the node on the inner liner of a tire allows sensing of additional technical parameters, such as road condition, tire wearout, temperature, tire friction, side slip, wheel speed and vehicle load. They may be used for improved tracking and engine control, feedback to the power train and car-to-car communication purposes.

Following this statement, an IC for a direct TPMS which is suitable for mounting on the inner liner of the tire has been implemented.

2.2.1 System Overview

The basic functionality of the presented IC is a batteryless sensor mounted on the inner liner of the tire. Figure 2.1 shows the simplified cross section of a tire including the mounting position of the IC.

In order to increase the attractiveness of the IC for tire manufacturers and consumers it is equipped with Radio Frequency Identification (RFID) technology, which allows simple warehouse and supply chain management. Additionally, tire type identification is possible in

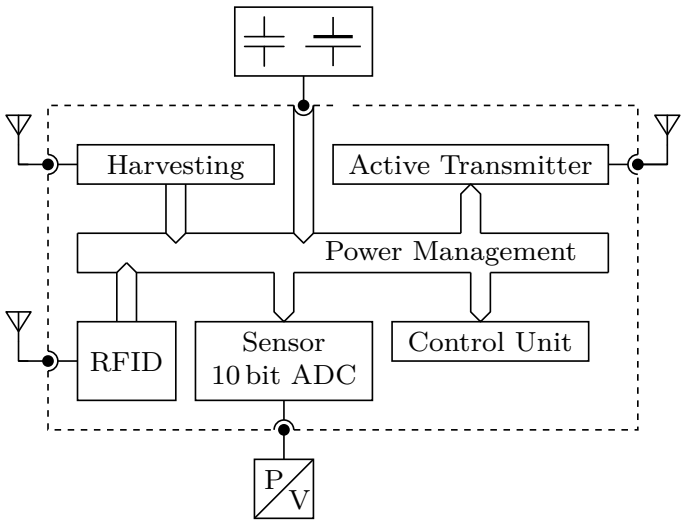


Figure 2.2: Block diagram of the WSN

the car. Providing tire parameters like tread pattern or rubber type can improve ABS and ESC performance. The RFID front-end, presented in [54], is working in the frequency range from 1 MHz to 2.45 GHz. The Electronic Product Code™ (EPC) protocols for HF and UHF are supported.

Figure 2.2 illustrates the block diagram of the WSN. The IC can be divided into six different blocks:

- Power source (energy harvesting)
- RFID
- Control unit
- Sensor and Analog to Digital Converter (ADC)
- Active transmitter
- Power management

Discussing all these blocks in detail is beyond the scope of this thesis. The focus is on managing the power on the IC. Therefore, details of the power management and the voltage regulators are discussed. For a better understanding, the operating modes of the WSN and the building blocks are briefly presented.

Power Sources

WSNs are most commonly powered by a battery [3]. Due to limitations in weight and size of the sensor if it is mounted on the inner liner of a tire, using a battery is not the best solution. So other solutions had to be found.

Power Source	Voltage range	Transient speed
RFID UHF	1.2 V to 1.6 V	fast (100 kV/s)
RFID HF	1.2 V to 3.3 V	
RF Harvesting	1.2 V to 3.3 V	slow (1 kV/s)
Battery	1.2 V to 3.3 V	very slow

Table 2.1: Summary of the different power sources used for the WSN

Depending on the application, the chip can be powered by three different power sources: (1) If the IC is used for TPMSs, an electromagnetic energy harvesting system is employed. The energy gained by this system is stored in an off-chip buffer capacitor. (2) In the case of using RFID, the power is gained by the RFID interface. (3) The off-chip capacitor of the harvesting interface can simply be replaced by a battery. Generally, any DC source can be used to replace one of the buffer capacitors. The DC/DC charge pump in the harvesting unit generates the required voltage level for low voltage inputs. Measurements using a small photovoltaic cell to power the IC showed satisfactory results.

The analog front-end used as energy harvesting interface has first been presented in [72]. The front-end is composed by two stages. The first stage is formed by a rectifier which converts the RF input into DC voltage. The converted energy is stored in a buffer capacitor. The second stage is a DC/DC charge pump. Using a charge pump the voltage in the buffer capacitor is transformed to higher levels. An additional buffer capacitor is used to store the output energy of the second stage. If the voltage level at this buffer capacitor is high enough, the sensor is activated. The measured input sensitivity is −19.7 dBm.

If the sensor node is powered by the RFID field, the analog front-end of the RFID interface transforms the RF energy to DC energy. This interface is first presented in [54] and an improved version in [69]. It is operable in a frequency range from 1 MHz to 2.45 GHz. This enables supporting different frequency standards commonly used for RFID. In comparison to the harvesting interface the required input power is higher if the chip is powered by the RF field of the RFID reader. This is because the analog front-end of the RFID interface has modulation and demodulation capabilities. Additionally, the load current is about 10 µA, whereas in the harvesting case the load current is only 200 nA. The measured input sensitivity of the RFID interfaces are −12.5 dBm and −10.3 dBm respectively.

The second buffer capacitor of the harvesting interface can be replaced by a battery. In this case the sensor node is operating in polling mode, because the voltage level is always high enough to enable the sensor node. The sensor data is then cyclically transmitted to the base station using the active transmitter. It is also possible to replace the first buffer capacitor with a DC source. This is useful for low voltage sources, as the input voltage is amplified using the charge pump of the harvesting interface.

Table 2.1 summarizes the different power sources used for the WSN. The typical voltage ranges and expected transients on the output voltage of the power source are also listed.

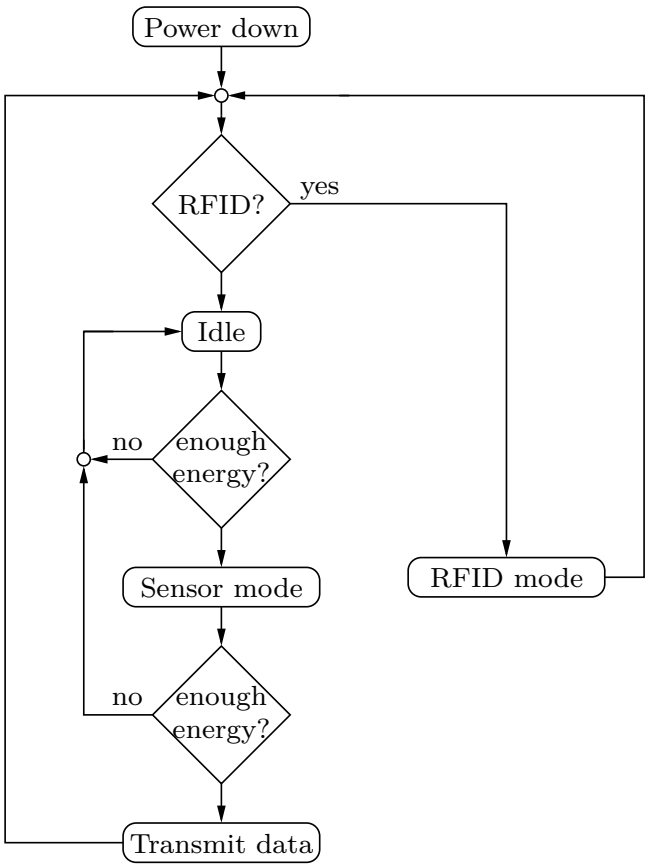


Figure 2.3: Flow chart of the state machine used for controlling the sensor

Control Unit

To control the different analog blocks on the IC, a state machine is implemented. Traditionally, such digital control units are implemented in synchronous logic. The behavior is described in a hardware description language, which is synthesized. Afterwards the layout is generated by powerful tools. For this sensor node a different approach is chosen. Driven by the strict power requirements, the state machine is implemented in asynchronous logic. The advantage of this approach is that there are no currents generated by clock signals. Especially if only a few transitions are required compared to the clock frequency, this method saves power. The drawback is that formal verification of this approach is difficult [57].

The inputs of the state machine are logic signals generated by level detectors. These level detectors monitor the input voltage of the sensor node. Depending on these voltage levels, different states are entered. Additionally, the output voltage levels of the different voltage regulators used for the power supply are monitored. If one of these voltage levels is too low, the operating mode is changed. If RFID mode is not considered, four different states are distinguished. The flow chart of the state machine is depicted in Figure 2.3.

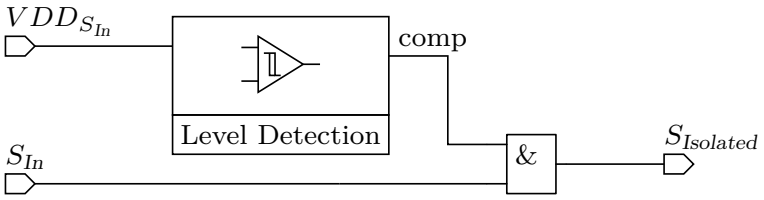


Figure 2.4: Isolation logic to isolate undefined digital signals

For low input power, the chip is turned off. Only the energy harvesting unit operates and transfers energy into the buffer capacitor. If the energy in the buffer capacitor is high enough, the sensor is started. After acquiring the temperature data, it is stored in the on-chip memory. From now on the IC waits until the energy is high enough for an active transmission of the data. If for any reason the voltage at one of the voltage regulators of the power supply is too low, the chip is reset and the operation starts from the beginning. Otherwise, the data is transmitted.

If the IC is in RFID mode, the digital control unit of the RFID block takes over the control. The communication follows EPC (U)HF standards. By using memory write and read functions, different blocks of the sensor node are controlled. Thus it is also possible to operate the on-chip sensor with the RFID interface.

To reduce leakage currents, unused blocks are turned off completely. Thus in power-down state undefined signals are generated by these blocks. Additionally, during startup signals may be wrong. To solve this problem, an isolation logic is implemented between the control unit and the sensor node. The isolation logic monitors the supply voltage of the blocks, which may provide wrong or undefined signals. The output signals are only forwarded to the control logic if the supply is high enough.

Figure 2.4 shows the principle of the isolation logic. A comparator monitors the supply voltage ($VDD_{S_{In}}$). The result of this comparison is gated using an AND gate with the signal S_{In}. As long as the signal *comp* is at low level, the AND gate will not draw any current regardless of the value of S_{In} and the output will stay at low level. If different voltage supply levels are in use, level shifters are additionally required. Every signal on the IC routed to the control unit is isolated using the presented circuit.

Sensor and Analog to Digital Converter

To measure the temperature, an on-chip temperature sensor is implemented. It compares a temperature dependent to a temperature independent voltage. To generate these voltages, a low power bias cell is implemented.

The bias cell operates according to the principle of a Switched Capacitor (SC) bandgap reference. This principle is first published in [63]. The measured current consumption of the bias cell is 500 nA and the area consumption is a third compared to conventional designs.

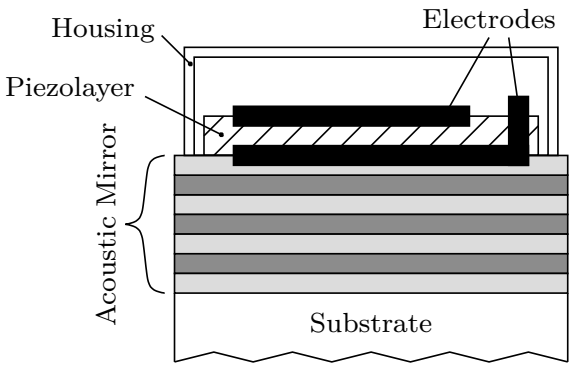


Figure 2.5: Cross section of a BAW resonator as reported in [65]

For sensing the pressure, an off-chip Micro-Electromechanical System (MEMS) device is necessary. On the WSN an analog input is available which can be connected to this device. The ADC converts the input signal of the pressure sensor into a digital representative. By this technique different off-chip devices can be used.

To obtain a digital value of the temperature and the pressure, a 10 bit successive approximation ADC is implemented. The Digital to Analog Converter (DAC) is formed by a charge redistribution architecture using a split capacitor array. The comparator operates according to the principle of the time-domain comparator published in [1]. By using a clock frequency of 1 MHz, 36 kSamples/s are achieved. The current consumption in this case is only 4 µA. This current is mostly consumed by the buffers used to drive the DAC.

Active Transmitter

The sensor data can be transmitted using an active transmitter. Similarly to the battery, an off-chip crystal may not be used for the active transmitter. Instead, a Bulk Acoustic Wave (BAW) resonator is used as frequency reference. Figure 2.5 shows the cross section of a BAW resonator. Referring to [7], the functionality of a BAW can be described as follows:

> The basic BAW resonators consist of a thin-film layer of piezoelectric material sandwiched between two metal thin-film electrodes. The voltage or the electrical field between the two electrodes excites an acoustic wave. The wave bounces back from the top and bottom surfaces of the two electrodes, and an acoustic cavity is formed between the top surface of the upper electrode and the bottom surface of the lower electrode. The frequency at which the resonance occurs is determined by the thickness of the piezolayer and the thickness and mass of the electrodes.

Compared to a crystal, the BAW resonator is more robust against mechanical stress. Additionally, the startup time of oscillators using a BAW resonator is in the range of only a few microseconds, whereas crystal based oscillators need several milliseconds [23]. Thus, the energy consumption can be improved significantly.

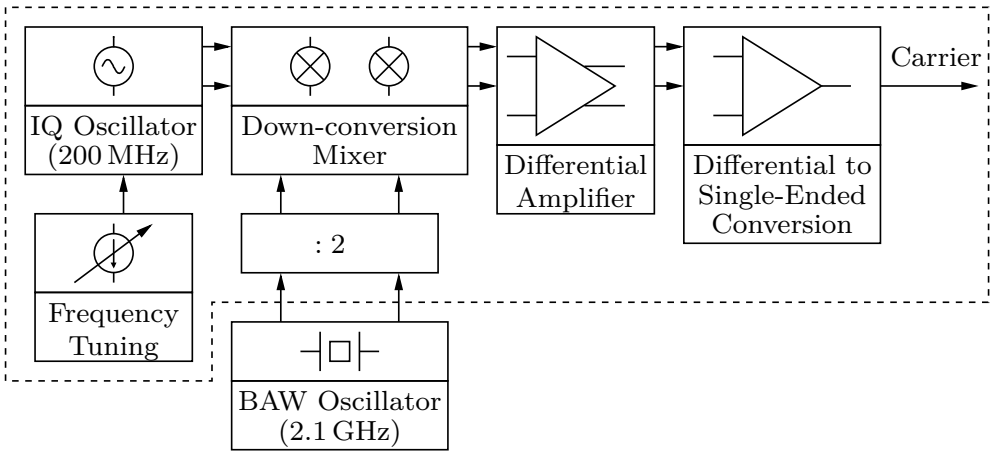


Figure 2.6: Block diagram of the carrier generation for the active transmitter

The main drawback of the BAW resonators is the temperature dependency of the reference frequency of about $-19\,\mathrm{ppm/K}$ [2]. Thus, such resonators need temperature compensation. For the presented chip, the correction is done by mixing the reference frequency with a temperature dependent oscillator. The architecture of the carrier generation using the BAW resonator is shown in Figure 2.6. The current of the IQ oscillator is adjusted depending on the temperature. This frequency is mixed with half of the frequency of the BAW resonator. The result is amplified and afterwards converted to a single-ended signal. By shifting the frequency of the IQ oscillator to different values, different transmission bands can be selected.

The generated carrier is fed into the power amplifier block, where on-off keying takes place. Four different power levels are supported: $-6.4\,\mathrm{dBm}$, $-1.5\,\mathrm{dBm}$, $4.0\,\mathrm{dBm}$, and $5.4\,\mathrm{dBm}$. Thus, the power ranges of state-of-the-art TPMS modules are covered. The data is Manchester encoded and four different data rates are supported: $250\,\mathrm{kbit/s}$, $125\,\mathrm{kbit/s}$, $62.5\,\mathrm{kbit/s}$, and $31.25\,\mathrm{kbit/s}$.

Communication Scenarios

The implemented sensor node allows different application scenarios. Depending on the power supply and the communication method, a different operating mode is selected. Figure 2.7 gives an overview on the different possible communication scenarios. The symbol holding the exclamation mark, which is the symbol used for TPMS failures, indicates the sensor. The sensor node can be operated as RFID tag (*RFID supply chain management*). In this case it is also possible to use the on-chip sensor. For transmitting the data either passive backscattering (*Passive RFID sensor*) or active transmission (*RFID sensor with active transmitter*) can be used. If the chip is supplied by a battery, it behaves like a general purpose wireless sensor node. The data is transmitted cyclically using the active transmitter (*Active sensor in polling mode*). Instead of the battery the harvesting interface can be used. In this case the chip is supplied by an RF field (*Fully passive sensor functionality*). If the energy harvested is high enough, the sensor data is transmitted using the active transmitter.

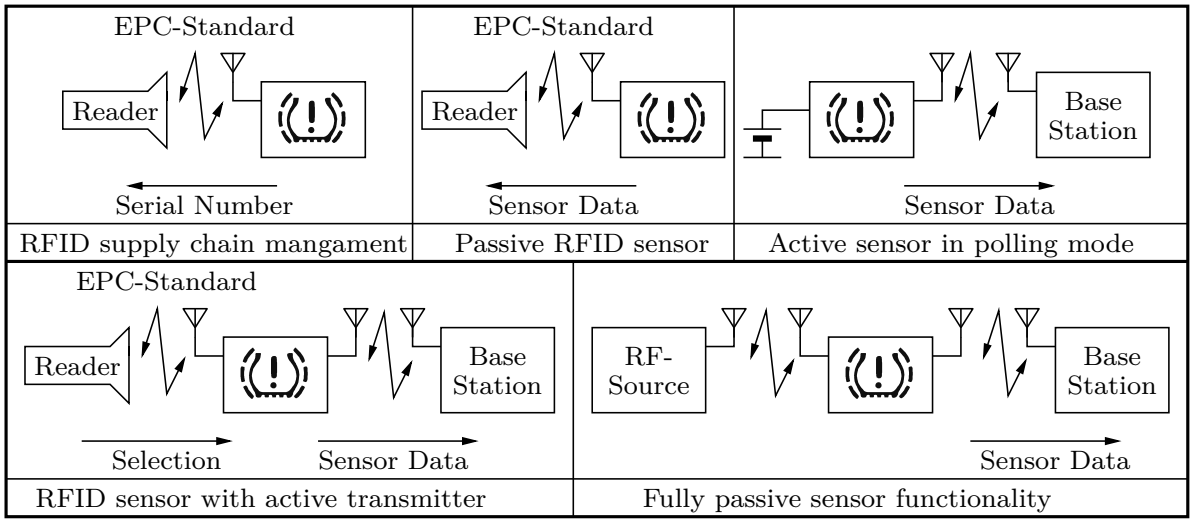


Figure 2.7: Communication scenarios possible with the presented wireless sensor node

2.3 Power Management of the Wireless Sensor Node

Depending on the application, the sensor node is powered by different power sources. These sources have different characteristics in terms of voltage level, transient speed, and internal resistance. The task of the power management is to route the power on the IC and to provide the necessary supply voltage at the right time for distinguished blocks. Also, overvoltage protection is necessary, since the input voltage of some power sources is beyond the breakdown voltage of some MOS transistor types. This chapter presents how the power management is achieved on this IC.

The circuits presented in this chapter operate in an automotive environment. Thus one challenge was to ensure a robust operation in the temperature range of $-40\,°C$ to $125\,°C$. Also, all corners of the CMOS process are considered.

2.3.1 System Overview

Figure 2.8 shows the block diagram of the IC from the power management's point of view. Three power sources are distinguished:

- Harvesting unit,
- RFID transponder, and
- Battery.

If the WSN is used for TPMS or RFID, either the harvesting unit or the RFID interface is used to supply the chip. The harvesting unit uses an off-chip buffer capacitor. This capacitor can be

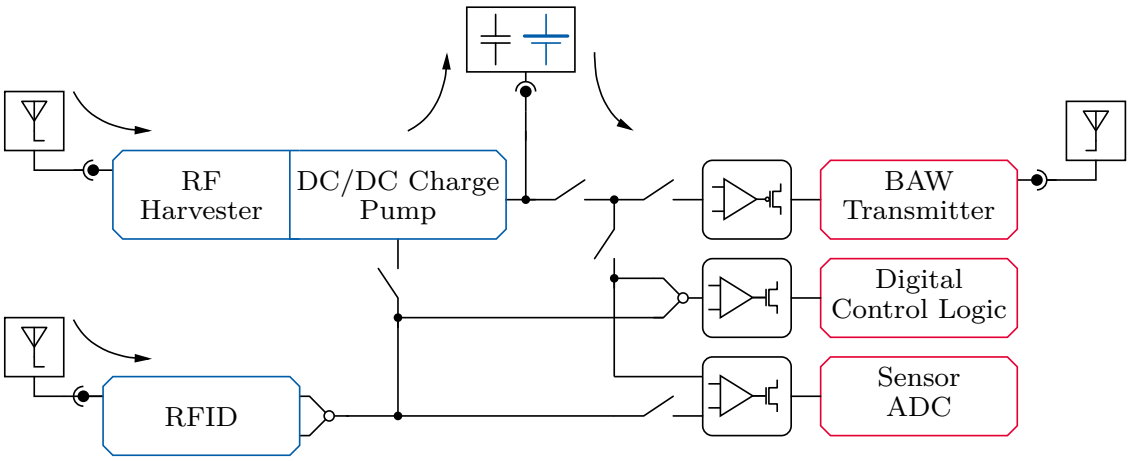


Figure 2.8: Block diagram of the WSN from the power management's point of view

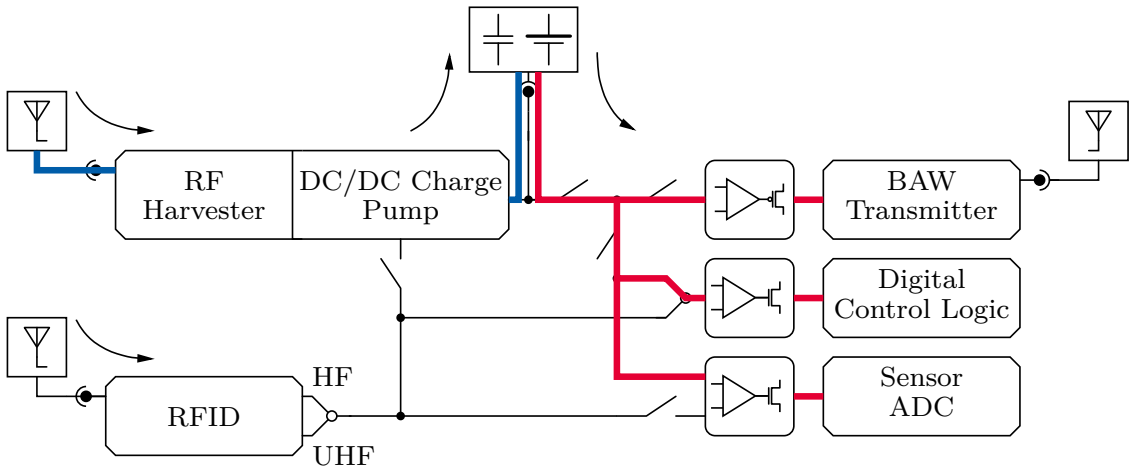
replaced by a battery. In this case the IC is operating like a general purpose sensor node in polling mode*. The power generated by one of these sources is consumed by the:

- Control unit,
- Sensor and the ADC, and the
- RF unit.

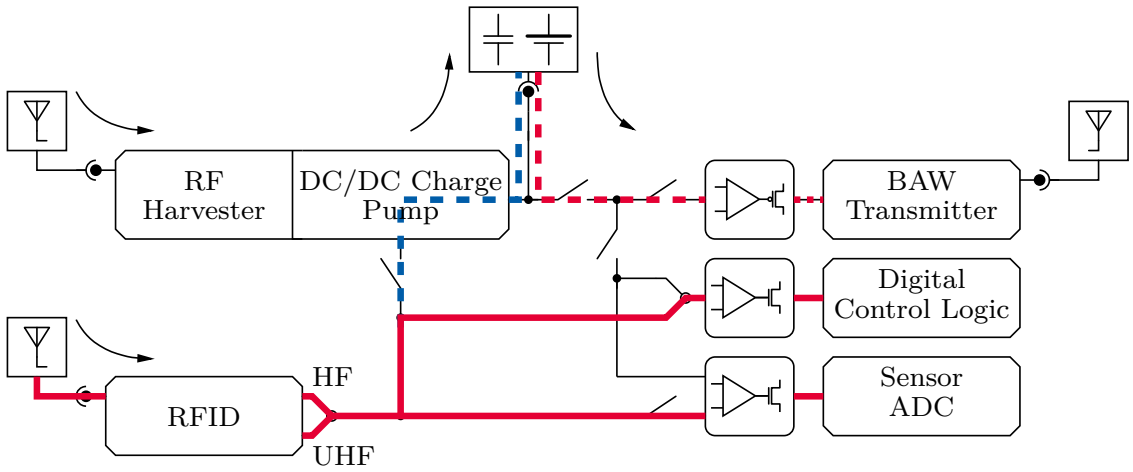
Figure 2.9 gives an overview on the different power flows on the chip. In harvesting mode, as shown in Figure 2.9a, the harvesting interface first converts the AC signal at the antenna input into a DC voltage. A DC/DC charge pump is then used to transfer energy into the off-chip buffer capacitor. If the voltage level at this buffer capacitor exceeds a certain limit, the control unit of the IC is enabled. The control unit now enables or disables the different functional blocks depending on the available energy in the buffer capacitor. By replacing the buffer capacitor with a battery, the WSN operates in polling mode. If the RFID field is used for powering, the AC/DC converter in the RFID unit converts the RF energy into DC voltage as shown in Figure 2.9b. This supply is used to operate the control unit and the on-chip sensor. The power available in RFID mode is usually too low to operate the active transmitter. If the power gained by the RFID interface is more than required to operate the control unit and the on-chip sensor, the DC/DC charge pump transfers the excess energy into the off-chip buffer capacitor. This allows using the active transmitter when the WSN is supplied by the RFID interface. Whenever the available energy in the capacitor is high enough and an active data transmission is required, the transmitter unit is enabled.

Four on-chip voltage regulators are required to generate the required voltage levels. An NMOS regulator supplies the on-chip temperature sensor along with the ADC. Another NMOS regulator is required for the control unit. For the active transmitter, two PMOS regulators are necessary. One supplies the carrier generation unit and the other one the power amplifier. These four regulators are presented in the following sections in detail.

* In polling mode the sensor data is transmitted periodically.



(a) Power flow if the WSN is supplied by the harvesting unit or the battery



(b) Power flow if the WSN is supplied by the RFID unit

Figure 2.9: Power routing on the WSN

2.3.2 Regulator for the On-Chip Temperature Sensor along with the Analog to Digital Converter

The following chapter is mainly taken from [29] (own publications). ■

The voltage regulator presented in this chapter supplies the on-chip temperature sensor along with the ADC. The sensor as well as the ADC are ultra-low power implementations. The temperature sensor has a current consumption of 500 nA and the ADC about 4 µA. Both require a supply voltage of 1.2 V. To achieve accurate results, a stable supply voltage is required. The lower the current consumption of the sensor along with the ADC is, the higher the Power Supply Ripple Rejection (PSRR) of the regulator needs to be, as it gets more sensitive to supply variations.

As discussed in Chapter 1.2.1, NMOS regulators having a low output impedance are preferable

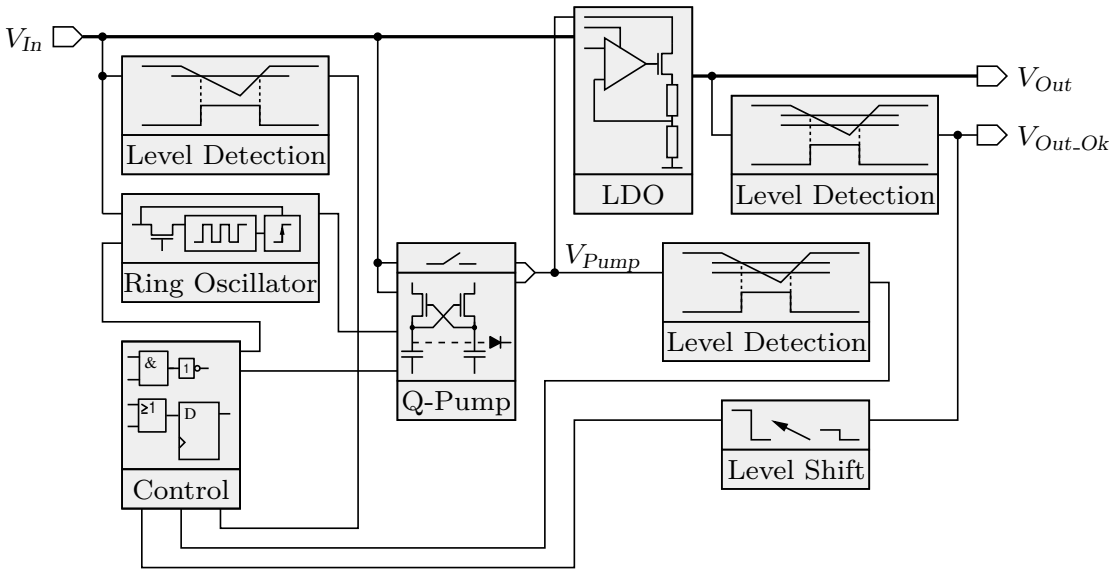


Figure 2.10: Simplified block diagram of the regulator used for the on-chip temperature sensor along with the ADC

if a high PSRR is required. Therefore an NMOS architecture as shown in Figure 2.10 is implemented. To enable low-dropout operation, the error amplifier is supplied by a charge pump. A voltage level detector at the input enables the charge pump block if necessary. If the charge pump block is enabled, an additional voltage sensor enables or disables the oscillator for the charge pump. The output of the regulator is monitored by a voltage sensor. This sensor states if the output of the regulator is high enough to allow accurate operation of the temperature sensor. A simple control logic switches between the different operating modes of the regulator.

The following sections discuss the different blocks of this regulator. The transient behavior and the control unit are presented as well. A conclusion summarizes the performance parameters of the regulator and compares them to actual publications.

Error Amplifier

The purpose of the error amplifier is to adjust the gate voltage of the pass device. Some of the important overall parameters of the regulator, like bandwidth or current consumption, are determined by the type of the error amplifier.

The reference voltage available on the IC is 500 mV. This low voltage requires a PMOS input of the differential pair. If the regulator is in low-dropout operation, it is preferable if the output of the error amplifier is able to reach the positive supply. To meet this constraint, a push-pull output stage is used. Figure 2.11 shows the resulting architecture. It comprises a differential pair of PMOS transistors and a push-pull stage. Using the low ohmic output of the differential pair leads to a one stage amplifier. Equations (2.3.1a-b) can be used for a

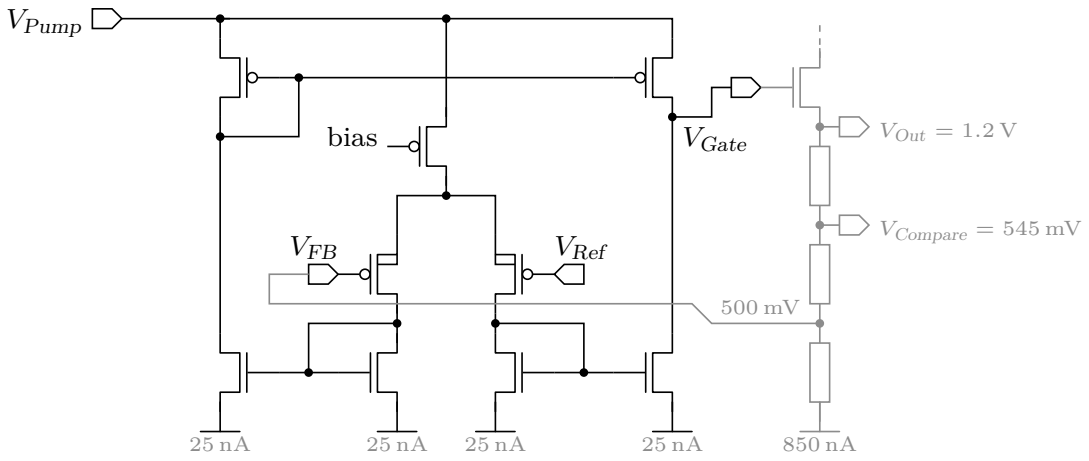


Figure 2.11: Architecture of the error amplifier

quick estimation of the small signal parameters of the amplifier. $A(\jmath\omega)$ is the complex voltage gain, g_m is the transconductance of the input transistor, and $\left\{R_{Out} \left\| \frac{1}{\jmath\omega \cdot C_{Out}} \right.\right\}$ is the output impedance formed by the capacitive load (C_{Out}) in parallel to the output resistance of the push-pull stage.

$$A_V(\jmath\omega) = g_m \cdot \left(R_{Out} \left\| \frac{1}{\jmath\omega \cdot C_{Out}} \right. \right) \tag{2.3.1a}$$

$$\text{UGF} = \frac{g_m}{2\pi C_{Out}} \tag{2.3.1b}$$

A major part of the overall current consumption is determined by the voltage divider used in the feedback loop. In CMOS technology either polysilicon resistors or MOS diodes can be used for the divider. Resistors allow arbitrary ratios. MOS diodes only offer integer multiples of the reference voltage. Additionally, the temperature coefficient of MOS transistors is larger than the temperature coefficient of polysilicon resistors. The area consumption at the same current consumption of MOS diodes is much smaller compared to polysilicon resistors. For this regulator only resistors are possible, as the output voltage (1.2 V) is not an integer multiple of the reference voltage (500 mV). With an area consumption of 42 µm × 92 µm a resistance of 2.4 MΩ is achieved. The current consumption of the voltage divider is 850 nA in the nominal case.

Output Voltage Sensor

The regulator provides a status signal (V_{Out_Ok}) which states if the output voltage is high enough. To generate this signal, the reference voltage is compared to the divided output voltage of the regulator. This division is also done by the voltage divider used for the error amplifier.

For the comparison, a voltage comparator with built-in hysteresis presented in [4] is used. The architecture of the comparator is depicted in Figure 2.12. According to [4], the hysteresis

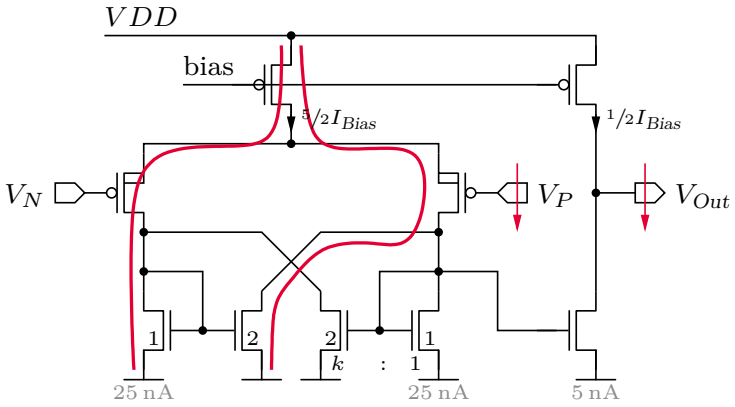


Figure 2.12: Comparator with built-in hysteresis

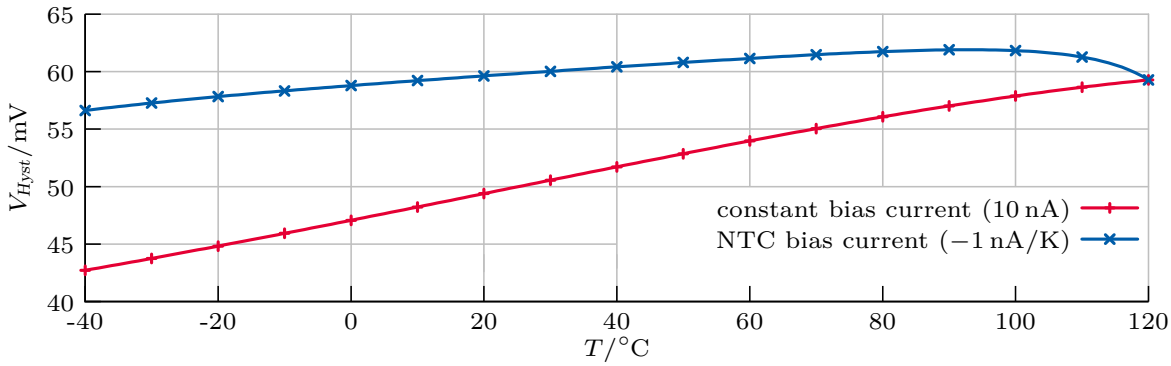


Figure 2.13: Simulation of the hysteresis voltage of the window comparator

voltage can be calculated with (2.3.2). Differentiating (2.3.2) with respect to the temperature T leads to (2.3.3). β is the product of the transistor geometries, the mobility and the specific oxide capacitance of the input transistor. BEX is the temperature exponent of the mobility parameter. Thus the hysteresis voltage is increasing if the temperature or the bias current is increased. To reduce the temperature effect in the hysteresis voltage, a bias current having a Negative Temperature Coefficient (NTC) should be used. Simulation results as shown in Figure 2.13 prove the proposed equations. As a bias current having an NTC is not available, the design is done accordingly to ensure a sufficiently large hysteresis at low temperatures. At 27 °C the hysteresis is: $V_{On} = 1.155\,\mathrm{V}$ and $V_{Off} = 1.055\,\mathrm{V}$.

$$V_{Hyst} = \sqrt{\frac{2 \cdot I_{Bias}}{(1+k) \cdot \beta}} \cdot \left(1 - \sqrt{k}\right) \tag{2.3.2}$$

$$V_{Hyst}\,(T) = f\left\{\sqrt{\frac{1}{T^{\mathrm{BEX}}}}\right\} \qquad \mathrm{BEX} \approx -1.5 \tag{2.3.3}$$

Due to capacitive coupling effects, the status signal V_{Out_Ok} may change to high state for a short time when enabling the regulator. To suppress this pulse, the output of the comparator is gated

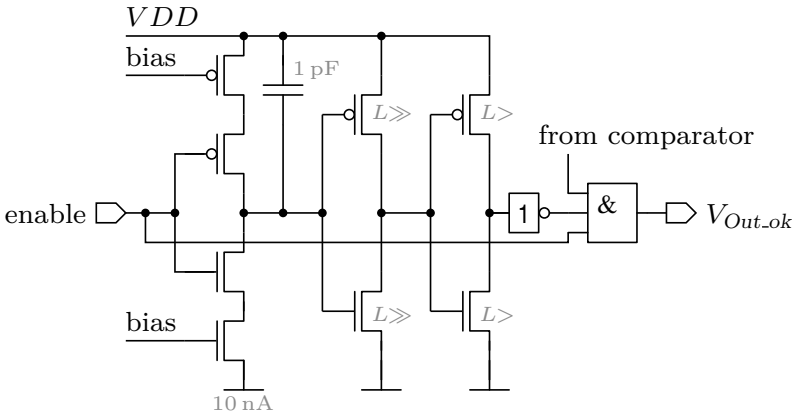


Figure 2.14: Delay element

with a delayed version of the *enable* signal using an AND gate. The circuit which generates the signal V_{Out_Ok} is shown in Figure 2.14. A capacitor is charged by a current starved inverter. This charging process takes approximately 50 µs. To limit the current consumption of the following stages, inverters having transistors with a long channel length are used.

Charge Pump and Bypass

The charge pump supplies the error amplifier and thus indirectly the gate of the pass device. It is only required for low input voltages. The most important design constraint is to get a sufficiently high supply voltage for the error amplifier when the input voltage is at its minimum level of 1.2 V.

The proposed voltage doubler in [22] fulfills the requirement for a fast and highly efficient voltage generation of the supply voltage for the error amplifier. Figure 2.15 shows the circuit. The cross-coupled NMOS transistors act as charge pump. The output voltage is ideally twice the input voltage. The PMOS transistors between the output of the charge pump (V_{Pump}) and the cross-coupled NMOS transistors rectify this pulsed voltage. Two additional PMOS transistors in parallel generate the supply voltage for the n-well. As the load current on V_{Bulk} is lower than on V_{Out}, V_{Bulk} will always be higher than V_{Out}.

[22] only discusses how to maximize the conversion efficiency. Here the voltage doubler is optimized for: (1) a high conversion efficiency (η), (2) a low output voltage ripple (ΔV_{Out}), and (3) a sufficiently high output voltage (V_{Out}). Due to layout constraints, the Metal-Insulator-Metal (MIM) capacitors have a fixed value of 1 pF and the four PMOS transistors should have the same geometry. The clock frequency has a fixed value of 200 kHz. The load current is about 150 nA. Table 2.2 gives an overview on how the transistors have to be sized. It is important to keep bold written constraints, whereas the influence of the other constraints on the optimization process is small. Increasing the output capacitor decreases the voltage ripple but also increases the startup time.

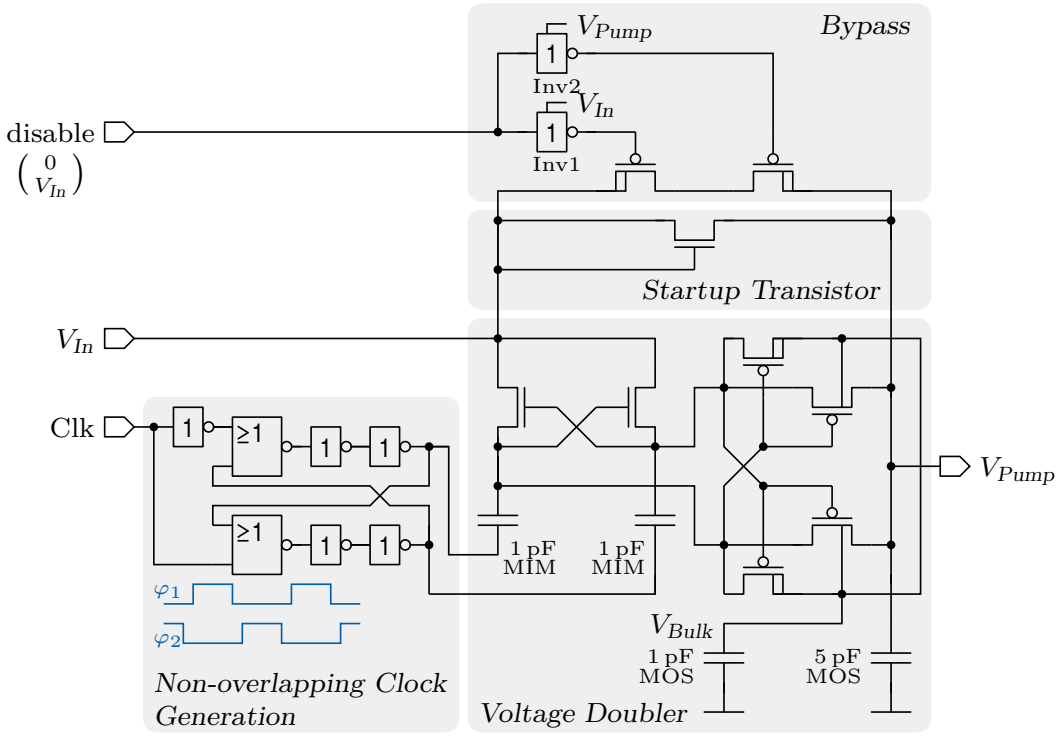


Figure 2.15: Voltage doubler proposed in [22]

	width of NMOS	width of PMOS	length of NMOS*	length of PMOS
η	**small**	**small**	small	medium
ΔV_{Out}	large	**small**	small	**large**
V_{Out}	small	**small**	small	small

*very low influence

Table 2.2: Design recommendations for the voltage doubler

To reduce the startup time of the voltage doubler, an NMOS transistor is connected parallel to the charge pump. Figure 2.15 shows that this startup transistor is in diode configuration. As long as the output voltage of the voltage doubler is smaller than the input voltage minus a gate-source voltage, this transistor is conductive.

If the clock is turned off, no electrical connection from the input to the output is available. In this case the error amplifier is not supplied by any voltage. So, a bypass in parallel to the charge pump is implemented. A PMOS switch conducts if the charge pump is turned off. Due to the different voltage levels, the bypass, also shown in Figure 2.15, is sophisticated. The use of two PMOS transistors ensures that the bulks of the transistors are always at the highest potential. Each input of the inverters either has to be at ground, at supply level, or higher. Otherwise, unwanted currents will flow through the inverters. The *disable* signal is either at zero or at V_{In} level. In the case of *disable* being at V_{In}, the PMOS transistor in the inverter

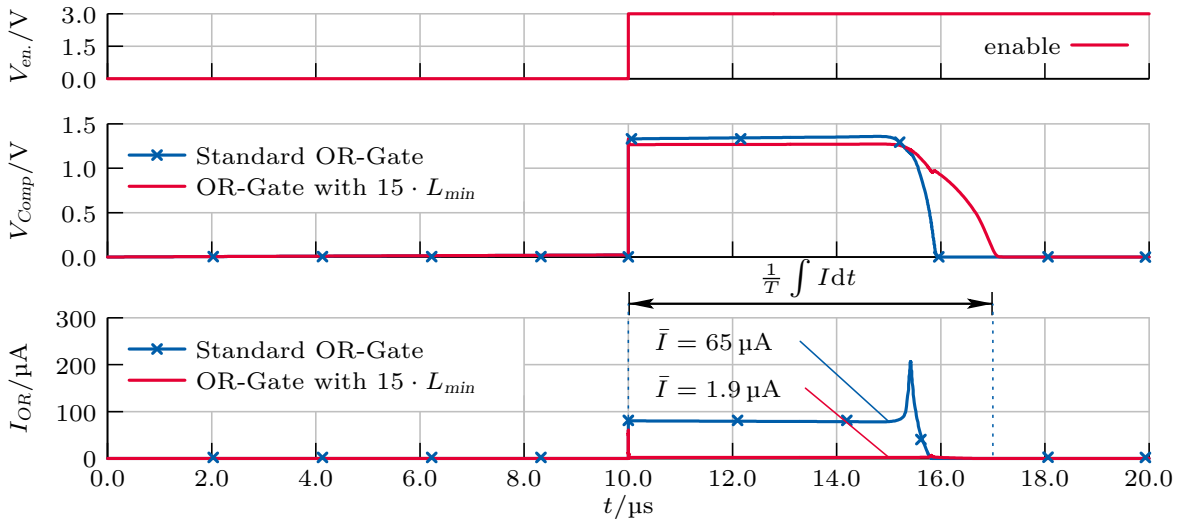


Figure 2.16: Comparison of the current consumption of the charge pump voltage sensor by using different transistor lengths during startup

Inv1 is turned off and the output is zero. As *disable* is not high if V_{Pump} is higher than V_{In} (the charge pump operates in that case), the PMOS in the inverter *Inv2* is also turned off and the output is zero. If disable is zero, the NMOS transistors in both inverters are turned off anyway, and so are the PMOS transistors in the switch.

The voltage doubler is clocked by a non-overlapping clock. Figure 2.15 shows a circuit which generates these clock signals. It is published in [81]. The advantage of this method, compared to others using only delay elements, is the use of feedback which ensures non-overlapping pulses. The inverters generate the time delay during the phase change of the outputs. If no inverters are used, the clock transitions are separated by just one delay time of the NOR gate. Using two inverters, as in this design, a separation time of a multiple of three gate delay times is generated. If four inverters are used, a separation time of a multiple of five gate delay times is achieved and so on.

The efficiency of the voltage doubler at $V_{In} = 1.2\,\mathrm{V}$ and $I_{Load} = 150\,\mathrm{nA}$ is $\eta = 76.2\,\%$. In this case an output voltage of $V_{Out} = 2.0\,\mathrm{V}$ and an output voltage ripple of $\Delta V_{Out} = 24.9\,\mathrm{mV}$ is achieved. A startup time (0 % to 90 % of V_{Out}) of approximately 80 µs is required.

Charge Pump Voltage Sensor

In the operating mode in which the charge pump is enabled, the output voltage of the pump is monitored. The output voltage of the charge pump has to stay around 2 V. Thus a comparator with a built-in hysteresis is used for monitoring. The low threshold is at 1.9 V and the high threshold is at 2.1 V. The comparator is similar to the one depicted in Figure 2.12. To increase the Slew Rate (SR) of the output voltage, the current source in the output stage is replaced by a switch.

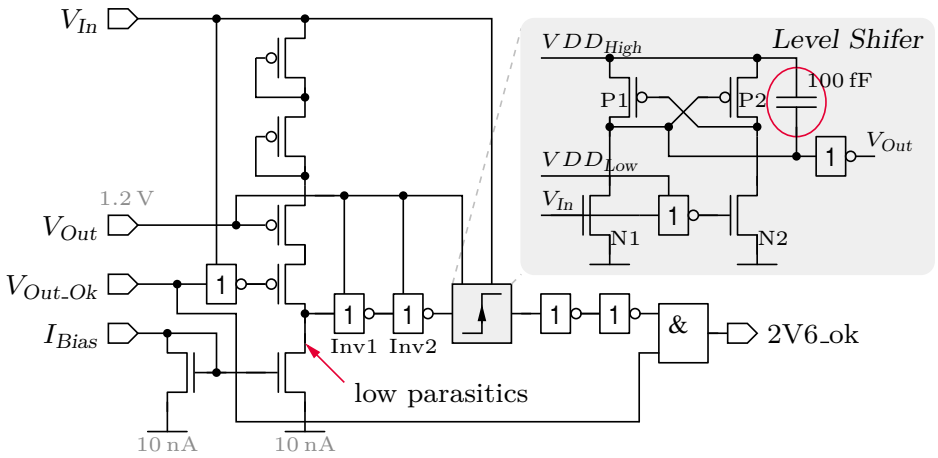


Figure 2.17: Input voltage detector

When the regulator is enabled, the output of the comparator generates a weak high pulse because of capacitive coupling effects (similar to the output voltage detector). This signal is routed to a digital gate, which draws a lot of current during this phase. Thus the lengths of the transistors in this gate are increased to limit this current pulse. A comparison of the current consumption during the startup phase for different transistor lengths is shown in Figure 2.16. The upper chart shows the *enable* pulse and the mid chart the output of the comparator. Since the OR gate with the larger transistors has a high input capacitance, the output of the comparator stays longer in the high state. The bottom chart compares the current consumption. Clearly, the average current during the startup phase is reduced severely. Due to the larger length of the transistors in the gate, the output SR of the OR gate is reduced. The impact of this reduction on the current consumption of the following gate is negligible.

The reference voltage used for the comparator is 500 mV. This requires a division of the output voltage of the charge pump by four. The division is achieved by using four diode-connected PMOS transistors in a row. The current consumption of the divider exhibits a quadratic growth as a function of the input voltage. The voltage divider draws a current of 490.5 nA at 3.3 V. Thus it is a good idea to turn off the voltage divider whenever the bypass is active, as it is not required in this case. This is presented in Chapter 4.3.

Input Voltage Detector

The charge pump is disabled (and the bypass activated) for input voltages higher than 2.6 V. Hence the input voltage needs to be measured. The straightforward approach is to divide the input voltage using a voltage divider and compare the result to a reference voltage. Especially for high input voltages, this method suffers from the high current consumption of the voltage divider. Thus a different approach, shown in Figure 2.17, is chosen.

The output voltage of the regulator (V_{Out}) is used as reference voltage. As soon as the input voltage is higher than this reference voltage plus three gate-source voltages, the NMOS current

source pulls the input of the first inverter to V_{In}. Only for input voltages lower than this sum is the NMOS current source able to hold this node at ground level. As soon as the inverter's input is high, the output (*2V6_Ok*) of the circuit changes to high state. Due to the different supply voltages of the inverters, a voltage level shifter is required additionally. If the regulator is in startup mode, the signal V_{Out_Ok} is zero and the output of the detector is forced to zero.

The advantage of this method is the low current consumption. When the input voltage is higher than 2.6 V, the current consumption of the detector is 10 nA. For lower input voltages or when V_{Out_Ok} is zero, the static current consumption is zero.

The drawback is the large variation of the detection level over temperature or process variations. The lowest detection level of 2.1 V occurs when the threshold voltage of the transistors is at a minimum, which appears at 125 °C and the *fast process* corner. The highest detection level is at 3.1 V. It occurs when the threshold voltages are at their maximum. Obviously, this is at −40 °C and the *slow process* corner. Even if this variation seems large, the detector always operates properly, as the detection level is defined high enough. After all, if the detector turns off the charge pump even if it would be required, the output voltage of the regulator will drop. Thus the reference voltage of the detector also drops and the charge pump will be enabled again.

For this level detector some issues had to solved. These are presented in the following section.

Design Issues

The output of the PMOS ladder may have a slow transient. The parasitic capacitances of the wire between this output and the inverter *Inv1* have to be kept low so as not to slow down this transient unnecessarily. The current consumption of this inverter during an input voltage transition has to be examined. By increasing the length of the transistors in the inverter or by using a current starved inverter, the current pulse can be limited to a certain value. In this design a standard inverter provides sufficient results.

The output of the inverter *Inv2* is at 1.2 V. So a level shifter has to convert this voltage to the voltage level of the input. The level shifter is also shown in Figure 2.17. During startup the lower supply voltage (VDD_{Low}) is not available. Thus the inverter supplied by this voltage provides an undefined potential at its output. In this case the level shifter may draw an undefined high current. To prevent this current, usually level shifters are disabled as long as the lower supply voltage is not available. Here such an enable signal cannot be generated. The SR of the input voltage of the regulator is always faster than 400 MV/s. This fact is exploited to use capacitive coupling effects to get the level shifter into a valid operation region during startup. A sandwich capacitor[‡] having 100 fF pulls the gate of the PMOS transistor P2 to VDD_{High} level. As this transistor becomes non-conducting, no undefined currents can flow.

[‡] Capacitor composed by the different metal layers in a CMOS process

If the input (V_{In}) and the lower supply voltage of the level shifter (VDD_{Low}) rise equally, the NMOS transistor N1 conducts as soon as the input voltage is higher than a threshold voltage. The gate of the PMOS transistor P1 is most likely at zero at startup. So this transistor is conductive with a very low on-resistance. This means that both transistors (N1 and P1) are conductive and uncontrolled current flows from the high supply voltage to ground. As long as the NMOS transistor N1 is not able to pull its drain potential to ground, the current will flow. When the on-resistance of the NMOS transistor N1 is decreased by the rising input voltage, the gate of the PMOS transistor P2 is drawn to ground and it becomes conductive. As soon as this transistor conducts, the gate voltage of the PMOS transistor P1 is drawn towards the supply and the transistor becomes non-conductive. The current can be limited by a large channel length of the PMOS transistors and a large channel width of the NMOS transistors. If it is ensured that the input voltage of the level shifter is zero during startup, this problem does not occur at all.

The comparator makes no use of a hysteresis in the detection level. Thus the output may oscillate if the input of the detector is at the detection threshold. Generating a hysteresis requires a circuit with additional current demands, which are saved here by omitting it. In Chapter 4.3 this problem is partly solved by using a clocked comparator.

Ring oscillator

The charge pump used to supply the error amplifier requires an oscillator having a frequency of about 200 kHz. The focus of the design is to be economical with the current consumption. The absolute frequency and a small jitter are not important.

A three-stage current starved inverter architecture satisfies the needs well. Figure 2.18 shows the schematic of the oscillator. The frequency is determined by the bias current and the buffer capacitors. Of course, the frequency is also affected by the supply voltage, the temperature, the process, and many other parameters. To reduce the current consumption of the output buffer, one stage is built without a capacitor. As the SR at this stage is the fastest, the output of this stage is routed to the output buffer.

The oscillator has two control signals *disable* and *enable_clock*. The first one disables the oscillator while the latter just enables the output. If the charge pump is turned off, the oscillator should also be stopped. Turning the oscillator on takes some time, which is a problem if fast transients occur at the input. So only the output buffer is turned off and the oscillator keeps running.

The output of the oscillator needs to be at the voltage level of the input voltage of the regulator. This can be up to 3.3 V. The transistors used for the oscillator have a breakdown voltage of 1.5 V and are destroyed at higher input voltages. Thus the supply voltage of the oscillator has to be limited. The limitation circuit is also shown in Figure 2.18. An NMOS transistor controls the supply voltage of the oscillator. The gate voltage of this transistor cannot exceed the sum of five gate-source voltages of diode-connected PMOS transistors. For low input voltages, the gate of the NMOS transistor is at V_{In} level, because the PMOS transistors are not conductive. If the input voltage is rising, the PMOS transistors conduct and limit the gate voltage of the

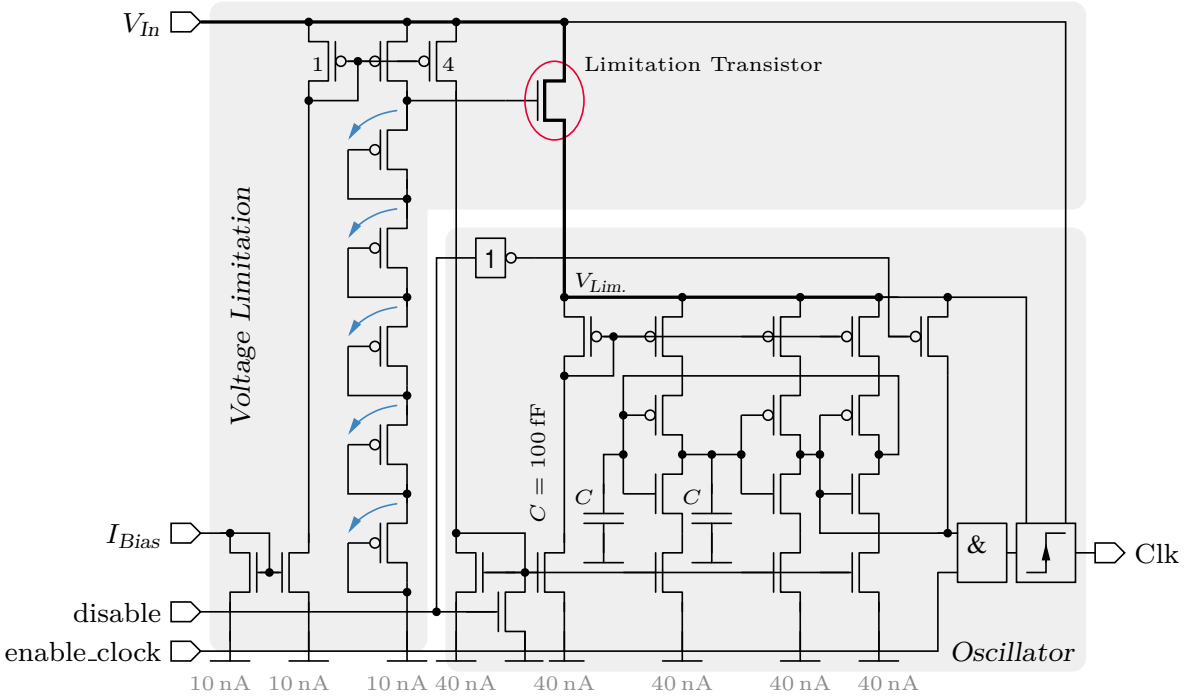


Figure 2.18: Ring oscillator with supply voltage limitation

NMOS transistor. At the output of the ring oscillator a voltage level shifter restores the output voltage level of the clock.

Another advantage of limiting the supply voltage of the oscillator is that the current consumption, especially for high input voltages, is reduced. Figure 2.19 shows the current consumption of the oscillator on different input voltage levels. The current consumption of the whole oscillator (I_{Osc}) and the current consumption of the level shifter (I_{LS}) are shown separately. The middle chart shows the frequency and the upper chart the regulated supply voltage of the oscillator. At an input voltage level higher than 2.6 V the output of the oscillator is disabled. Thus the output frequency and the current consumption of the level shifter become zero. In this case the current consumption of the oscillator is approximately 300 nA. The dashed lines show the theoretical current consumption of the oscillator if the output is not disabled at input voltages higher than 2.6 V. In the case in which the charge pump block is enabled, the charge pump voltage sensor enables or disables the output of the oscillator as required. The dotted line in the bottom chart shows the current consumption of the oscillator if the output buffer is disabled. Thus, the actual current consumption in the input range of 1.2 V to 2.6 V is between the solid and the dotted line.

Stability Analysis

To examine the stability of the regulator, the double injection method discussed in Chapter 1.4.1 is used. Figure 2.20 shows the injection point and Figure 2.21 the resulting bode plot of the

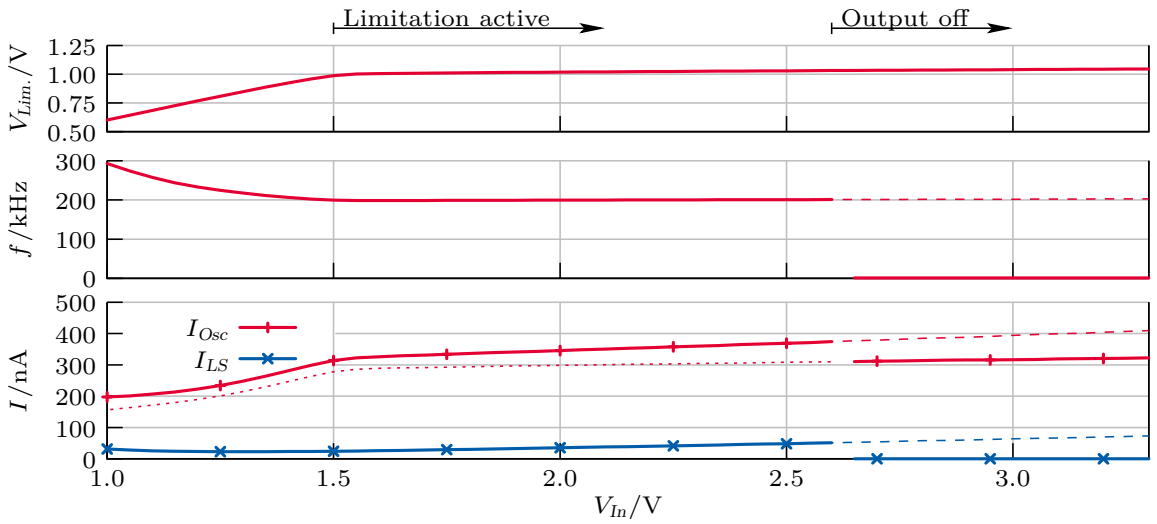


Figure 2.19: Current consumption and frequency of the ring oscillator on different input voltage levels

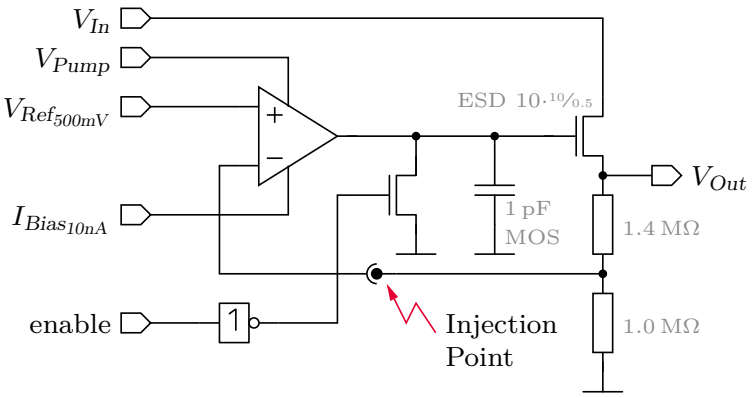


Figure 2.20: Core of the regulator showing the injection point

loop gain. The plot shows a phase margin of 84° in case of nominal load and 62° in case the load is disconnected.

To ensure stability, the poles and zeros of the system need to be identified. The dominant pole (f_{p_1}) is formed by the output impedance of the error amplifier and the capacitive load of the amplifier. Using (2.3.4a) shows that the absolute pole frequency is $f_{p_1} = 195\,\text{Hz}$. C_{Pass} is the capacitance of the pass device and C_{Comp} the capacitance of the compensation capacitor. The first non-dominant pole (f_{p_2}) is formed by the load of the regulator and the pass device. (2.3.4b) gives an estimation of this frequency. Post-layout simulation yields an absolute pole frequency of the non-dominant pole of $f_{p_2} = 290\,\text{kHz}$. The absolute value of the non-dominant pole frequency is decreasing if the load current is decreased or the load capacitance is increased. If no load is connected, the absolute pole frequency drops to 54 kHz. The phase margin in this

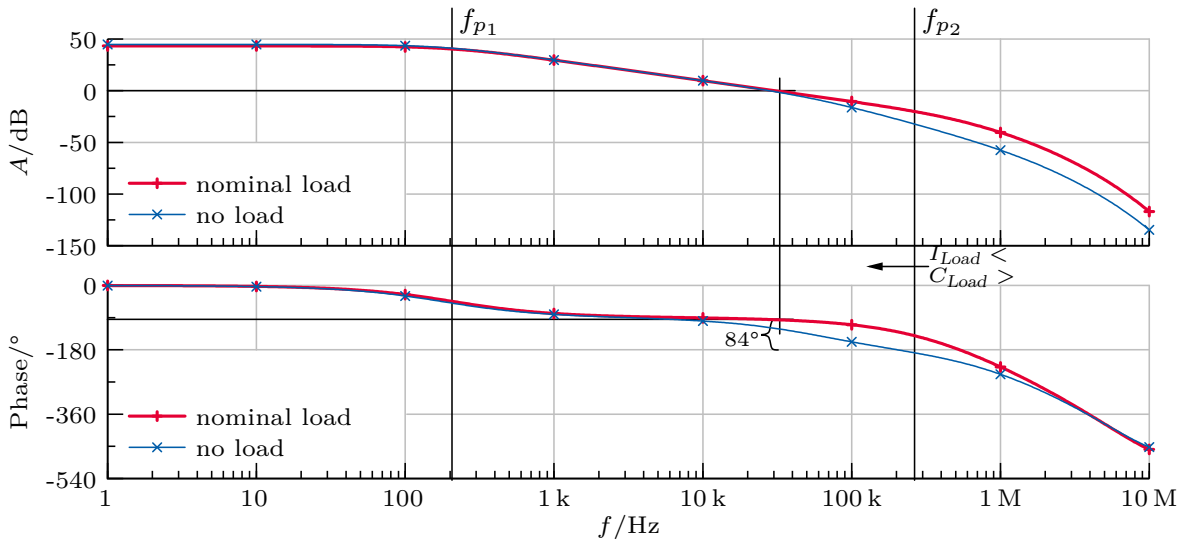


Figure 2.21: Loop gain of the regulator

case is 62°.

$$|f_{p_1}| = \frac{1}{2\pi \cdot (C_{Pass} + C_{Comp}) \cdot R_{Out_{OTA}}} = \frac{1}{2\pi \cdot (C_{Pass} + C_{Comp}) \cdot \left(\frac{1}{g_{ds_N} + g_{ds_P}}\right)_{OTA}} \tag{2.3.4a}$$

$$|f_{p_2}| = \frac{1}{2\pi \cdot C_{Load} \cdot \left[R_{Feedback} || R_{Load} || \left(\frac{1}{g_m + g_{mbs}}\right)_{pass\ device}\right]} \tag{2.3.4b}$$

For the overall frequency response, the feedback network needs to be analyzed. The feedback network contains polysilicon resistors connected in series. The area consumption of these resistors, having a resistance of 2.4 MΩ, is approximately 40 µm × 90 µm. Thus the parasitics to substrate have to be taken into account. Also, the individual resistor fingers are placed closely, which causes parasitic capacitances between them. These parasitic capacitances influence the transfer function significantly. An analytic expression for the overall transfer function is hard to find. Generally speaking, parasitics to substrate generate poles and parasitics between fingers generate zeros. Post-layout simulation shows that multiple poles and zeros appear beyond 1 MHz causing a fast degeneration of the phase.

In addition to the mentioned poles and zeros, the error amplifier itself also generates poles and zeros in the transfer function. Here the NMOS current mirror (refer to Figure 2.11) at the output generates a pole-zero doublet. The absolute pole frequency is at approximately 13 MHz and the absolute zero frequency is at 87 MHz. As the absolute values of these frequencies are far beyond the Unity Gain Frequency (UGF), their influence is negligible.

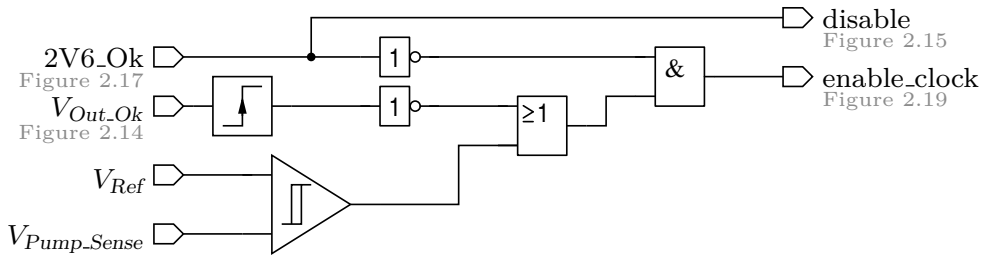


Figure 2.22: Control logic of the regulator

Transient Behavior and Control

Three operating modes of the regulator are distinguished:

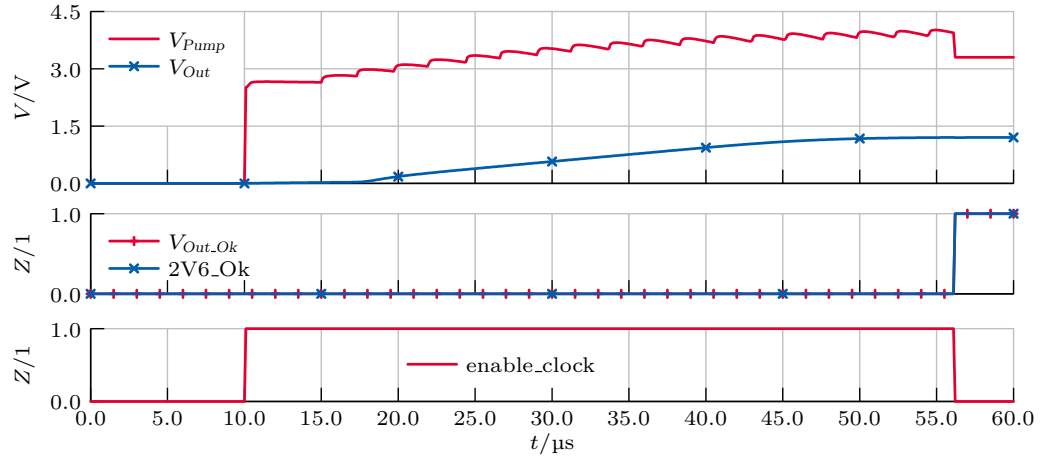
Startup: The regulator is enabled and it starts to operate. Startup is complete when the output voltage sensor sets V_{Out_Ok} to high state.

Low-dropout mode: The input voltage of the regulator is below 2.6 V causing the charge pump to be enabled.

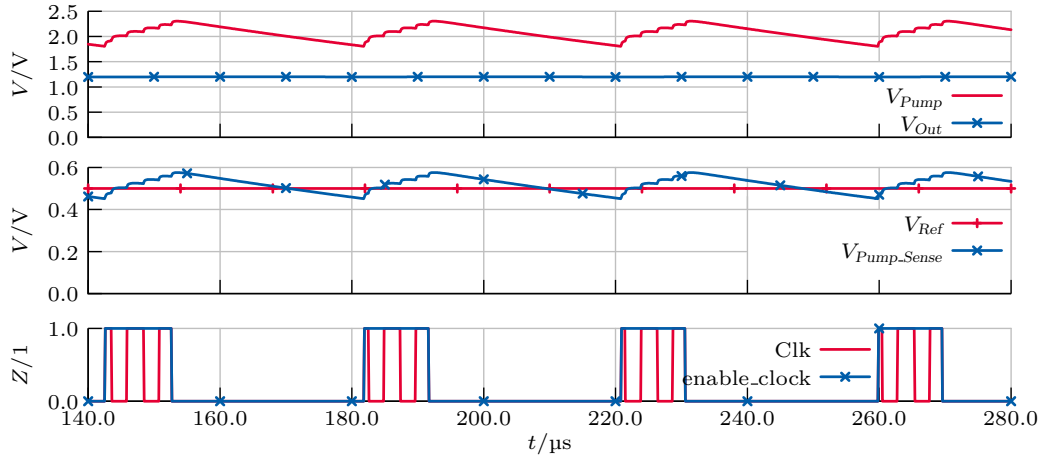
Regular operation: The input voltage of the regulator is high enough to disable the charge pump.

For a better overview, Figure 2.22 shows the simplified control logic of the regulator. The outputs and inputs have references to the corresponding circuits where they are in use. The logic is supplied by the input voltage of the regulator. Thus a level shifter for the V_{Out_Ok} signal is required.

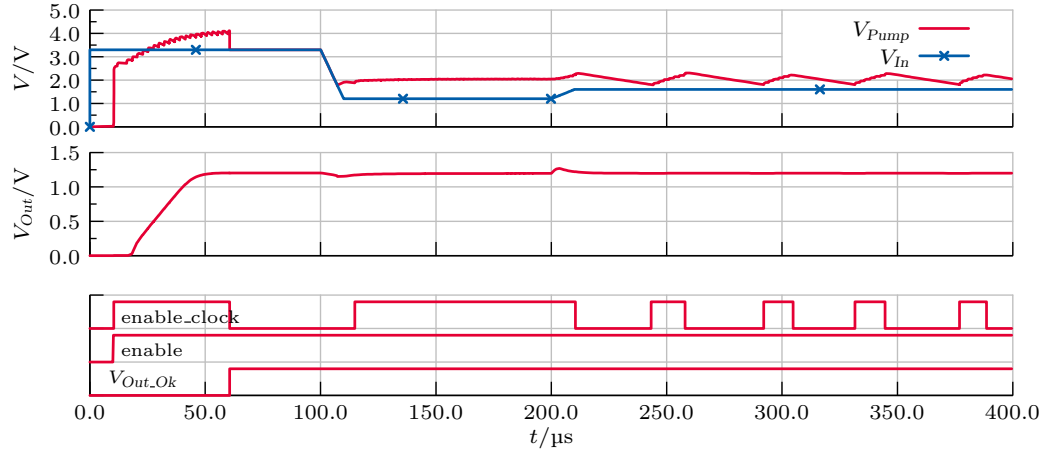
If the regulator is disabled, a power switch in series to the regulator is non-conductive. As long as the regulator is disabled, all internal nodes are tristate. Control signals routed to different blocks are isolated using the circuit presented in Chapter 2.2.1 in Figure 2.4. The regulator starts to operate when the power switch is closed by the signal *enable* changing to high state. Both *2V6_Ok* and V_{Out_Ok} are in low state and the charge pump starts to operate, as *enable_clock* is set to high state. Because of the voltage difference between V_{Pump} and V_{In}, the NMOS diode in the bypass of the charge pump, which acts as startup transistor, conducts. Figure 2.23a shows the transient behavior of the most important signals during startup. The upper chart shows the output voltage of the charge pump and the output voltage of the regulator. At 10 µs the regulator is enabled and switched to an input voltage of 3.3 V. The startup transistor forces the charge pump output to rise fairly fast to 2.6 V. The bottom chart shows the *enable_clock* signal which enables or disables the charge pump. During startup this signal is forced to high state. The oscillator requires approximately 5 µs to start. Thus the output voltage of the charge pump starts to rise at 15 µs. The error amplifier starts to operate and adjusts the output voltage of the regulator to the required voltage. At 56 µs the output voltage of the regulator is at its desired level, V_{Out_Ok} changes to high state, and startup is complete. As the input voltage is higher than 2.6 V, the signal *2V6_Ok* changes to zero. The regulator is now in regular operating mode.



(a) Transient behavior at startup at an input voltage of 3.3 V

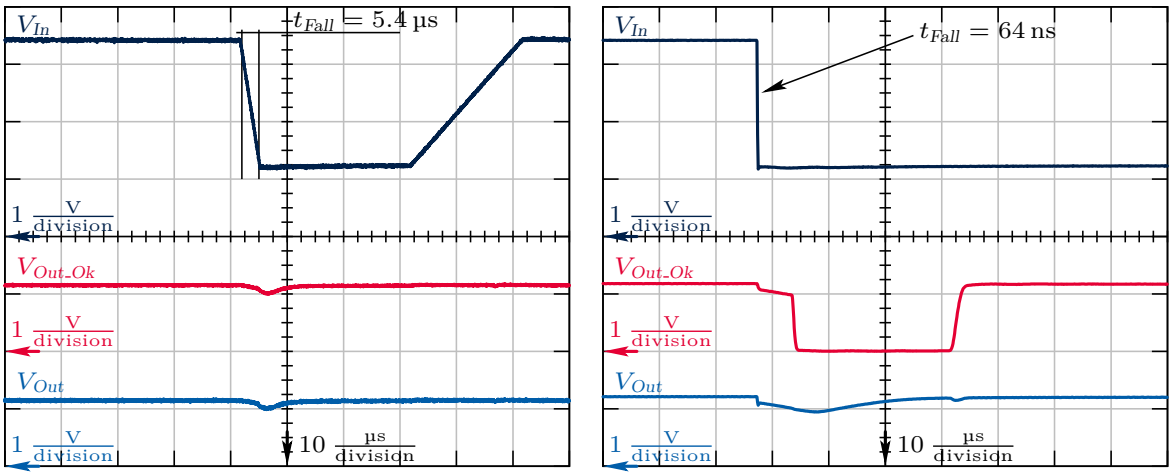


(b) Transient behavior at low-dropout mode at an input voltage of 1.7 V



(c) Transient analysis showing all possible operating modes

Figure 2.23: Detailed transient analysis of the operating modes of the regulator



(a) Maximum SR on the input voltage without affecting the V_{Out_Ok} signal

(b) SR of the input voltage is too fast to be handled by the regulator

Figure 2.24: Measurement of the regulator's behavior during different input voltage slew rates

If the input voltage of the regulator is lower than 2.6 V, it operates in low-dropout mode. Figure 2.23b shows the most important signals of the regulator when it is operating in this mode. Here the input voltage is 1.7 V. Thus *2V6_Ok* is zero and the charge pump is enabled. The upper chart shows the output voltage of the regulator and the output voltage of the charge pump. Whenever the output of the charge pump drops below 1.9 V, the output of the clock is enabled and the charge pump operates. In the bottom chart the clock (*Clk*) and the enable signal of the clock (*enable_clock*) are shown. Three clock pulses are required to achieve a sufficiently high output voltage of the charge pump and to disable the oscillator again. The middle chart shows the reference voltage and the sense signal generated by dividing the output of the charge pump.

Figure 2.23c summarizes the transient behavior of the regulator in all possible operating modes. As long as V_{Out_Ok} is zero, the regulator is in startup mode. As soon as this signal changes to high state, regular operation is entered as *enable_clock* is zero. At 100 µs the input voltage drops to 1.2 V. Thus low-dropout mode needs to be enabled and *enable_clock* changes to high state. At 200 µs the input voltage is rising to 1.6 V. The regulator still operates in low-dropout mode but the charge pump is periodically enabled and disabled. The signal *enable_clock* is alternatingly in high and low state.

Measurement Results

The regulator is implemented as a stand-alone version as well. For verification, this test chip is measured. The most important parameters are the line regulation capabilities and the current consumption. Also, the clock throughput to the output voltage needs to be evaluated.

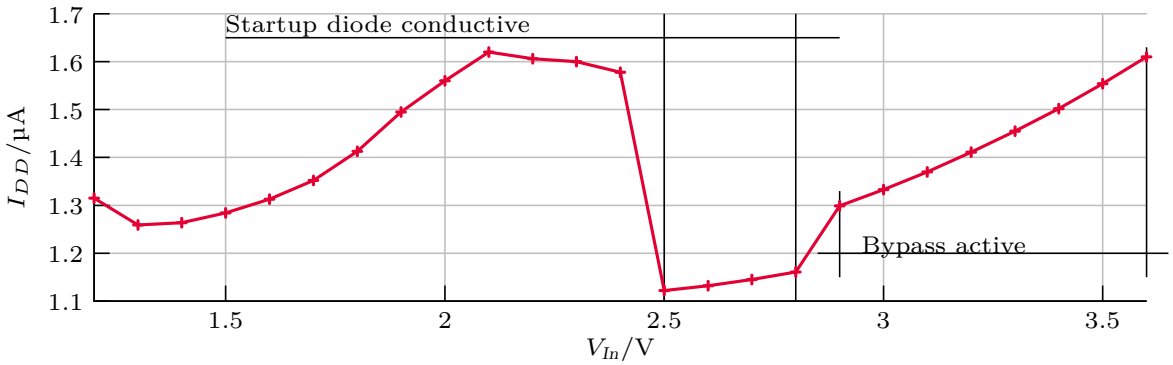


Figure 2.25: Measured current consumption of the regulator

Figure 2.24 shows the measured transient behavior of the regulator. The curves are obtained using an oscilloscope. Figure 2.24a shows the measurement of the maximum allowed input voltage drop speed without causing V_{Out_Ok} to change into zero state. The maximum SR of the input voltage is 398 kV/s. If the SR is higher than this value, V_{Out_Ok} changes to zero because the output voltage of the regulator drops below the specification. Figure 2.24b shows detailed measurement results at an input voltage SR higher than 398 kV. After the output voltage is recovered V_{Out_Ok} changes to high state again. Rising transitions on the input voltage do not noticeably affect the output voltage. The highest SR which could be generated in the laboratory has an SR of 31 MV/s. Using this SR for an input voltage transition from 1.2 V to 3.3 V causes a voltage ripple on the output voltage of approximately 200 mV.

One major performance parameter of the regulator is the current consumption. The measurement result of the current consumption without any load is shown in Figure 2.25. In the input voltage interval from 1.2 V to 2.4 V the current consumption increases because the level shifter implemented inside the ring oscillator requires more current. At 2.5 V the NMOS diode in parallel to the bypass is conductive. Thus V_{Pump} is higher than 2 V and the level shifter in the oscillator is turned off. At 2.8 V the bypass is active and V_{Pump} equals V_{In}. The current consumption is increasing at this level because the voltage divider used for the charge pump control draws more current. Clearly, a major improvement is to turn off the voltage divider if the bypass is active, as it is not needed anyway. This is presented in Chapter 4.

For SC networks, clock feedthrough is typically an issue. The clock frequency of the charge pump may occur at the output voltage of the regulator. Measurements showed that for this implementation clock feedthrough is not an issue. Figure 2.26 shows the measured Fast Fourier Transformation (FFT) of the output voltage of the regulator referred to 50 Ω. No spurious tone at the oscillator frequency, which is about 200 kHz, can be seen. The spurs at an integer multiple of 23 kHz are caused by the periodic enabling and disabling of the charge pump. Depending on the input voltage, these frequencies are shifted. When the charge pump is permanently enabled or disabled the spurs vanish.

Performance parameters which are commonly used to compare different regulators are presented in the next section.

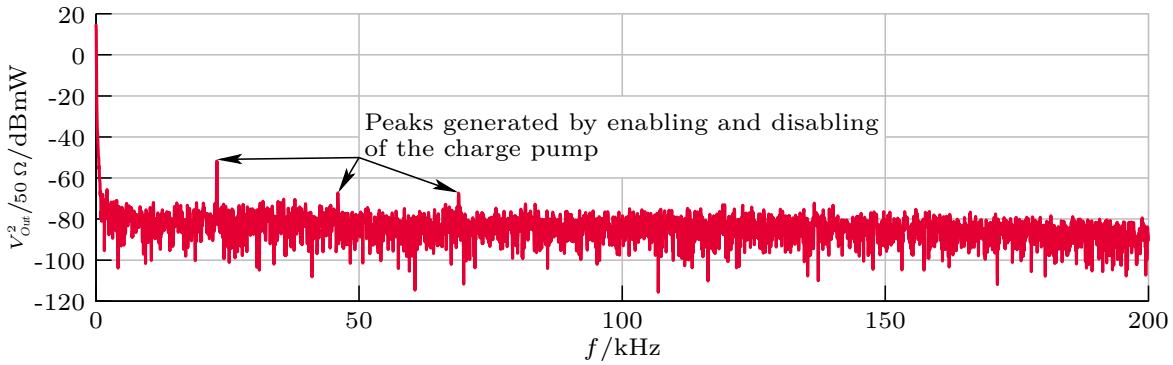


Figure 2.26: Measured FFT of the output voltage referred to 50 Ω

Comparison and Conclusion

Table 2.3 on page 49 summarizes the most important parameters of the regulator. These values are compared to a similar published work. The lower current consumption of the work in [16] results in a longer startup time and in a longer load pulse settling time. The comparison points out that there is always a trade-off between current consumption and speed. The focus of the referenced work is clearly on reducing the current consumption, whereas this work also considers the transient behavior.

This chapter presented a voltage regulator dedicated to an on-chip temperature sensor along with an ADC. As the load current is only a few microampere, the current consumption of the regulator is set to approximately 1 µA. The input voltage may have fast transients up to 398 kV/s and the input voltage range is from 1.2 V to 3.3 V.

2.3.3 Regulator for the Digital Control Unit

This chapter presents the voltage regulator which provides the supply voltage for the control unit of the WSN. As described in Chapter 2.2.1, this unit consists of an asynchronous state machine. Additionally, the regulator supplies a clock similar to the one presented in [54] with a frequency of 2.16 MHz and a polling oscillator having a frequency of approximately 1.3 kHz. The required output voltage is 1 V. The load current is estimated as 2 µA.

The regulator's input voltage characteristics are similar to the characteristics of the regulator used for the on-chip temperature sensor as presented in Chapter 2.3.2. Figure 2.8 shows the three possible power sources: (1) the RFID interface in HF or in UHF mode, (2) the harvesting interface, or (3) the battery. An on-chip voltage sensor monitors the voltage generated by one of these sources. Whenever the voltage exceeds 1 V, the regulator is enabled.

As the regulator supplies the main control logic, it has to operate reliably. Fast transients generated by one of the possible power supplies of the WSN must not affect the output voltage of the regulator in a way that leads to a malfunction of the control unit. The regulator has requirements similar to those of the regulator used for the temperature sensor

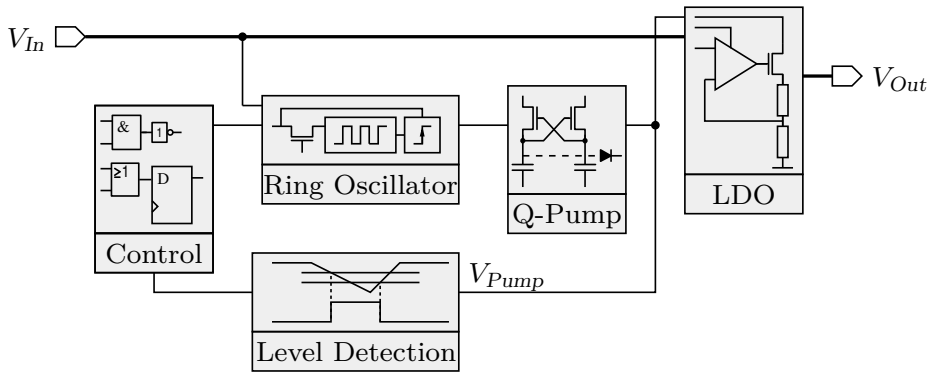


Figure 2.27: Simplified block diagram of the regulator used for the digital control unit

presented in Chapter 2.3.2. However, if the regulator for the temperature sensor fails, the signal V_{Out_Ok} resets the sensor and the operation starts from the beginning. The regulator presented here must not fail, as it will reset the whole WSN, which is of course an unwanted behavior.

Figure 2.27 shows the simplified block diagram of the regulator. The architecture is similar to the architecture presented in Figure 2.10. To handle the stricter requirements concerning current consumption and fault tolerance, the architecture for this regulator is simplified. In contrast to the regulator for the temperature sensor, the input voltage sensor, the output voltage sensor, and the bypass of the charge pump are removed. Thus this regulator provides no information about the validity of the output voltage. Also, the "regular operating mode" is not available. Instead, the regulator always operates in low-dropout mode.

As this regulator is very similar to the regulator for the temperature sensor, this chapter describes only the differences and improvements. At the end measurement results are presented and compared to the results of the regulator designed to supply the temperature sensor and to recent publications.

Regulator Core

Figure 2.28 shows the core of the regulator: the error amplifier, the pass device, and the feedback network. Additionally, the power-down circuit for the pass device is shown. Compared to regulator for the temperature sensor along with the ADC, shown in Figure 2.20, the width of the pass device is smaller and the feedback network is implemented differently.

As already discussed in Chapter 2.3.2, it is advantageous to make use of MOS diodes for the voltage divider in the feedback loop. The resistance per area is larger for MOS diodes compared to polysilicon resistors. The area consumption, without using dummy structures for matching reasons, is 15 µm × 24 µm. By extensive dummy resistor usage, an area of 45 µm × 19 µm is finally occupied by the MOS diodes. At room temperature the current consumption of the divider is 31 nA. The area consumption of an equivalent polysilicon resistor without dummy structures would be 90 µm × 840 µm. The dominant effect of the temperature behavior of an

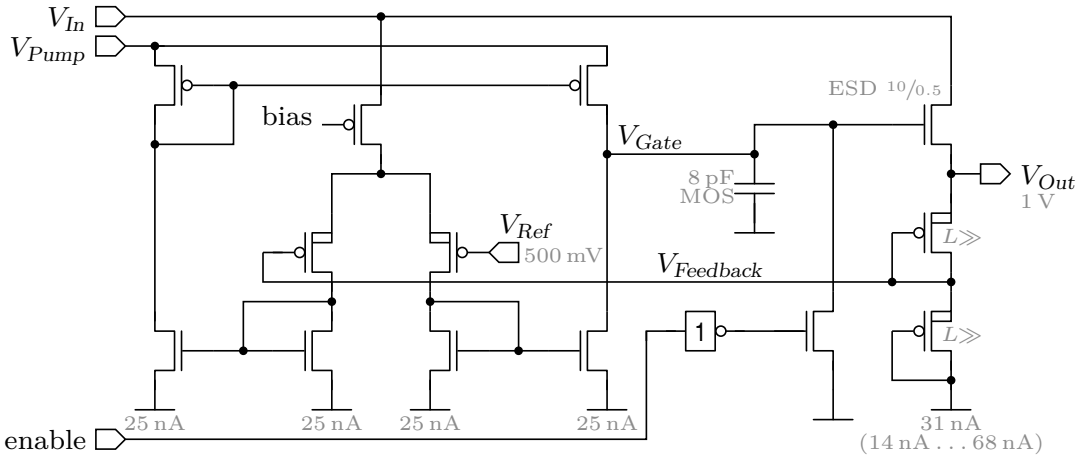


Figure 2.28: Core of the regulator

MOS transistor is the decreasing threshold voltage if the temperature is increased. Thus the resistance of an MOS diode is decreasing if the temperature is increased. In the temperature range of −40 °C to 125 °C the current in the divider ranges from 14 nA to 68 nA. Considering the process corners the current range is increased from 7.5 nA to 120 nA.

Charge Pump and Charge Pump Control

To enable low-dropout operation, a charge pump supplies the error amplifier. As discussed, for energy saving reasons the charge pump used for the regulator supplying the on-chip temperature sensor is disabled at high input voltages. Also, an NMOS diode parallel to the charge pump improves the startup time. If either the switch or the startup diode is conductive, spikes on the input voltage are passed on to the error amplifier. Due to the limited PSRR of the error amplifier, these spikes are passed on to the output of the regulator. Thus the startup diode and the switch are removed in this implementation.

The charge pump is enabled as soon as V_{Pump} drops below 2 V, regardless of the input voltage of the regulator. To measure the output voltage of the charge pump, it is divided using four PMOS diodes and compared to the reference voltage. The comparator is equivalent to the one shown in Figure 2.12, except that a different output stage is used. For power saving reasons, the oscillator is turned off when the charge pump is disabled.

The lower the input voltage is, the more charge pump cycles are required to achieve the necessary supply voltage for the error amplifier. In other words, if the input voltage is dropping, the operating mode of the charge pump has to be changed from a few cycles to always on. The limiting factor of the fastest input voltage drop the regulator can handle is the turn-on time of the oscillator. Thus it is advantageous if the supply voltage of the error amplifier gets a boost on fast input voltage drops because as a result the turn-on time can be longer. This boost is achieved by a simple trick: Figure 2.29 shows the current flow and voltage transitions in the charge pump during an input voltage drop. With ϕ_2 being at ground level, the output of

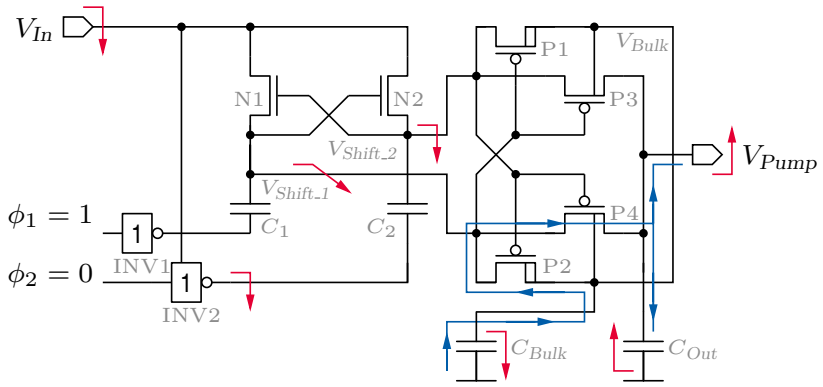


Figure 2.29: Illustration of the push on the output voltage of the charge pump during an input voltage drop

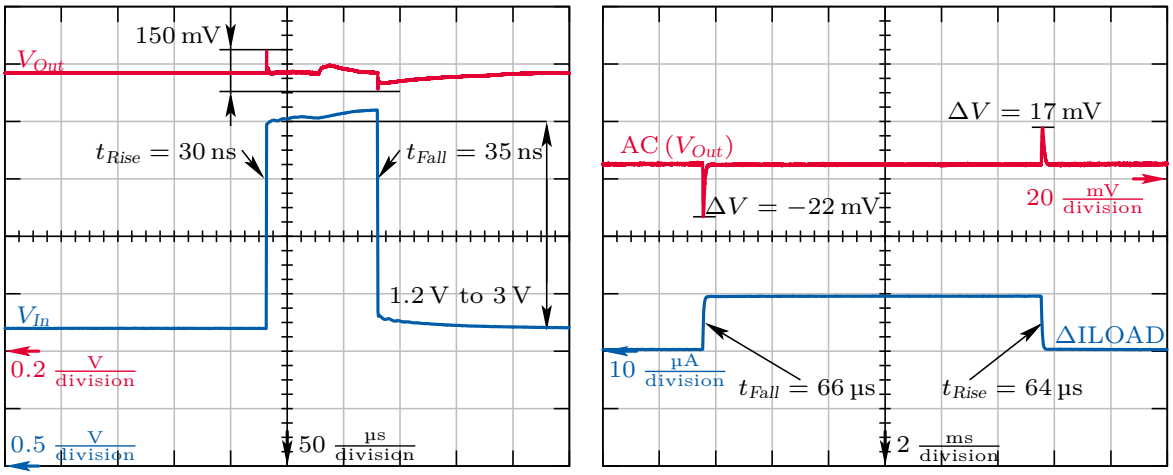
the inverter INV2 is at V_{In} level. When the input voltage drops, the output of this inverter drops equally. Thus V_{Shift_2} also drops fast, causing N1 to get non-conductive. N1 and C_1 form a lowpass filter. Thus V_{Shift_1} is decreasing slowly. Due to V_{Shift_2} being low, P2 and P4 get conductive, connecting C_{Bulk} and C_{Out}. As V_{Bulk} is always higher than V_{Out}, a current from C_{Bulk} charges C_{Out} until both capacitors have the same potential. That means that the output voltage of the charge pump is boosted if the input voltage drops fast.

Stability Analysis

To verify the stability of the regulator, the loop gain is evaluated using the double injection method. For the nominal load, a phase margin of 82° is achieved. By decreasing the load current, the phase margin is also decreased. If no load is present, the phase margin is 65°.

(2.3.5a-c) are used to calculate the corresponding pole and zero frequencies. The dominant pole is formed by the output impedance of the error amplifier and the capacitive load at this node. The load of the regulator combined with the pass device and the resistance of the feedback network generates the non-dominant pole. If the load is disconnected, the dominant resistive part in the equation for the pole frequency is determined by the current flowing in the feedback divider. Thus, at low temperatures and a slow process the absolute frequency of the pole is at a minimum. In addition to these two poles, a pole-zero doublet is generated by the PMOS voltage divider in the feedback loop. The diode between the output voltage of the regulator and $V_{Feedback}$ generates a zero and the diode between $V_{Feedback}$ and ground generates a pole (refer to Figure 2.28).

$$|f_{p_1}| = \frac{1}{2\pi \cdot (C_{Pass} + C_{Comp}) \cdot R_{Out_{OTA}}} = \frac{1}{2\pi \cdot (C_{Pass} + C_{Comp}) \cdot \left(\frac{1}{g_{ds_N} + g_{ds_P}}\right)_{OTA}} \quad (2.3.5a)$$



(a) Input voltage pulse

(b) Load current pulse

Figure 2.30: Measurement of the regulator's behavior on different input voltage and load current transients

$$|f_{p_2}| = \frac{1}{2\pi \cdot C_{Load} \cdot \left[R_{Feedback} || R_{Load} || \left(\frac{1}{g_m + g_{mbs}} \right)_{pass\ device} \right]} \tag{2.3.5b}$$

$$|f_{p_3}| = \frac{g_{m_{Diode_1}}}{2\pi \cdot C_{Diode_1}}, \qquad f_z = -\frac{g_{m_{Diode_2}}}{2\pi \cdot C_{Diode_2}} \tag{2.3.5c}$$

Measurement and Simulation Results

A standalone version of the regulator is not available. Thus only a few measurement results are available. Parameters not accessible by measurement are obtained by simulation. As discussed in the introduction, robustness in terms of transient regulation characteristics is essential.

Figure 2.30 shows the measured transient behavior of the output voltage of the regulator on input voltage and load current pulses. A voltage pulse source is used to obtain the results in Figure 2.30a. The input voltage of the WSN is pulsed within 1.2 V and 3 V. The rise and fall times are 30 ns and 35 ns respectively. The on-chip reference cell cannot handle these pulses. Thus, for this measurement the reference voltage is stabilized off-chip. This is not possible for the reference current. Hence, the influence caused by pulses on the reference current is unknown. The measured output voltage shows a peak to peak ripple of 150 mV.

In Figure 2.30b, an off-chip current source generates pulses between 0 µA and 10 µA. The current is measured using a series resistance of 100 kΩ between the voltage source and the power supply pin of the WSN. The voltage drop over this resistance is measured with an oscilloscope. As the WSN is fully functional during this measurement, the off-chip current is added to the

	Regulator for the control unit*,¶	Regulator for the temperature sensor*,¶	[16] by G. De Vita*
Output Voltage	1.0 V	1.2 V	605 mV
Input Voltage Range	3.6 V to 1.0 V	3.6 V to 1.2 V	1.5 V to 6.3 V
Quiescent current	580 nA to 1.05 µA	1.12 µA to 1.62 µA	34 nA
Line sensitivity	12 mV/V	2.6 mV/V	0.8 mV/V
DC output resistance	46 Ω	21 Ω	100 Ω
Load pulse settling time ($0 \rightarrow 4$ µA; 7 %)	190 ns	120 ns (0.3 % of V_{Out})	480 µs
Start-up settling time ($0 \rightarrow 3$ V / $0 \rightarrow 1.2$ V)	200 µs / 241 µs	45 µs / 70 µs	1.5 ms / n.r.
Maximum load current	300 µA	800 µA	5 µA
Maximum input slew rate ($3.3 \rightarrow 1.2$ V)	> 50 MV/s	398 kV/s	not reported
PSRR at DC ($V_{In} = 3.3$)	−85.6 dB	−51.8 dB	−58.5 dB
PSRR at DC ($V_{In} = 1.3$)	−79.3 dB	−71.6 dB	
Chip area	0.015 mm^2	0.02 mm^2	0.025 mm^2

*measured ¶simulated

Table 2.3: Performance summary of the regulator used for the on-chip temperature sensor and of the regulator dedicated to the control unit

nominal load. The fastest achievable rise and fall times of the measurement device are 66 µs and 64 µs respectively. This leads to voltage ripples of 22 mV and 17 mV.

Performance parameters which are commonly used to compare different regulators are presented in the next section.

Comparison and Conclusion

This chapter presented a voltage regulator dedicated to the control unit of the WSN. The implementation is similar to the regulator presented in Chapter 2.3.2. The requirements concerning the load regulation capabilities and the current consumption are stricter. The output voltage is 1 V and the nominal load current is 2 µA.

Table 2.3 summarizes the performance parameters of the regulator. The results are compared to the regulator presented in Chapter 2.3.2 and to a similar published work. The table indicates an improvement in all parameters except the startup time. Thus better line regulation capabilities are gained at the expense of a longer startup time.

Compared to the regulator implemented for the temperature sensor, the PSRR is improved significantly, especially for high input voltages. The reason is that the supply voltage of the error amplifier is decoupled from input voltage by the charge pump. As neither a startup diode

nor a bypass of the charge pump is implemented, the isolation is also active for higher input voltages.

2.3.4 Regulator for the Carrier Generation Unit

This chapter presents the voltage regulator which provides the supply voltage for the carrier generation unit. The carrier generation unit mixes the output of an IQ oscillator with a BAW oscillator. For testing purposes, a ring oscillator can be selected instead of the BAW oscillator. The supply voltage is 1.5 V. The current consumption is estimated with 5 mA.

The load current of this regulator is much higher than the typical values in this thesis. It will be shown that it is possible to design a regulator requiring only a few microampere which provides sufficient regulation capabilities for this load. Not considering the current consumption of the voltage divider in the feedback loop, the regulator requires approximately 15 µA. Usually off-chip capacitors are required to stabilize the control loop. Here such a capacitor is not required.

Regulator Architecture

As a result of the large load current, the NMOS architecture with a charge pump to supply the error amplifier as presented in Chapter 2.3.2 and Chapter 2.3.3 is not possible here. The error amplifier has a current consumption of about 10 µA. This requires a powerful charge pump and is therefore not the best solution. Also, the switching noise generated by the charge pump may translate into phase noise of the oscillator. Here a PMOS pass device configured as a current source is better suited.

The fact that no off-chip components are allowed has to be considered from the beginning of the design. The pole frequency generated by the load of the regulator is estimated using (2.3.6).

$$|f_p| \approx \frac{1}{2\pi \cdot C_{Load} \cdot R_{Load}} \approx 5\,\text{MHz} \tag{2.3.6}$$

To ensure stability, the pole frequency of this pole and the next (non-)dominant pole need to be spread over decades. For good load and line regulation capabilities, the dominant pole should be formed by the load and the non-dominant pole by the error amplifier. This would require a pole frequency in a typical system inside the error amplifier of at least 5 GHz. Clearly, the current consumption of the error amplifier to achieve this high bandwidth is not affordable. Thus compensation is done inside the error amplifier at the expense of line and load regulation capabilities.

Figure 2.31 shows the simplified block diagram of the regulator on transistor level. The architecture can be divided into three blocks: (1) startup control, (2) error amplifier, and (3) output stage.

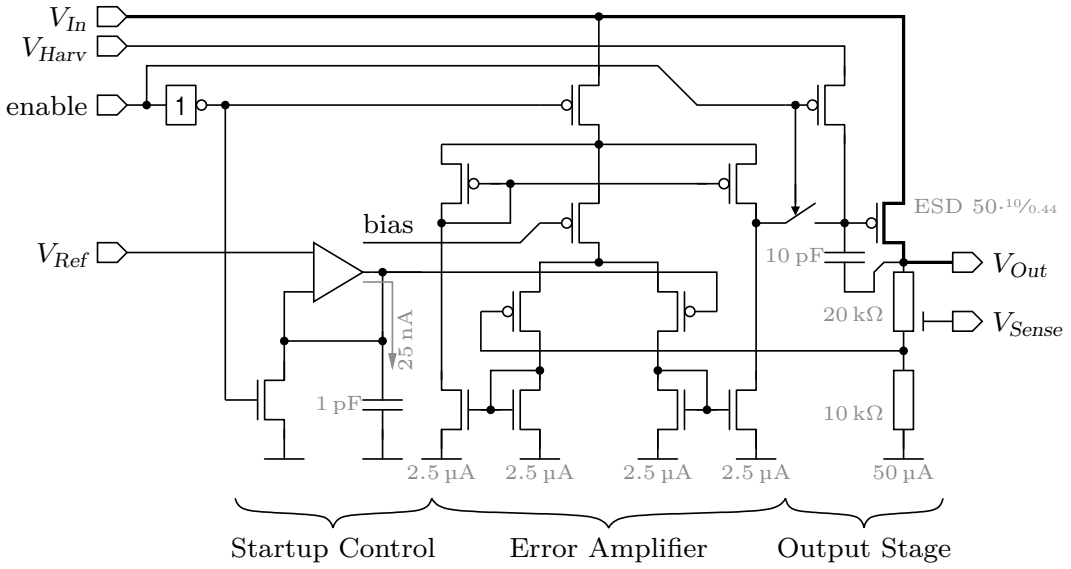


Figure 2.31: Simplified architecture of the regulator supplying the carrier generation unit

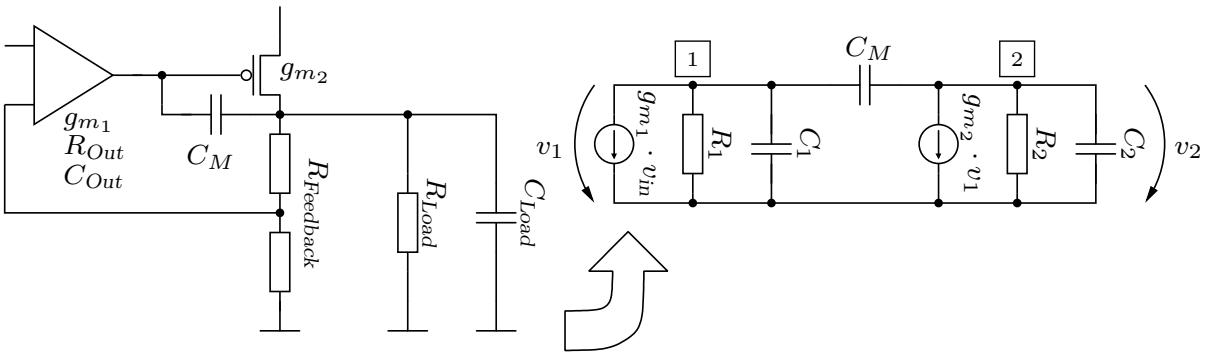


Figure 2.32: Equivalent circuit of a two-stage amplifier

Stability Analysis

Figure 2.32 shows the equivalent circuit of the regulator, which is in general a two- stage amplifier. For the nodes 1 and 2, the node equations in the frequency domain are:

$$\boxed{1}: \quad -g_{m_1} \cdot v_{in} - \frac{v_1}{R_1} - sC_1 v_1 - sC_M (v_1 - v_2) = 0$$

$$\boxed{2}: \quad sC_M (v_2 - v_1) + g_{m_2} \cdot v_1 + \frac{v_2}{R_2} + sC_2 v_2 = 0$$

These two equations can be solved to obtain v_1 and v_2. If v_2 is divided by v_{in}, the open loop transfer function of the system is derived:

$$A(s) = \frac{g_{m_1} g_{m_2} R_1 R_2 \left(1 - s\frac{C_M}{g_{m_2}}\right)}{1 + s \cdot \lambda_1 + s^2 \cdot \lambda_2} \tag{2.3.7}$$

$$\lambda_1 = R_1 (C_1 + C_M) + R_2 (C_2 + C_M) + R_1 R_2 g_{m_2} C_M$$
$$\lambda_2 = R_1 R_2 (C_1 C_2 + C_1 C_M + C_2 C_M)$$

To obtain the poles, the zeros of the denominator of the open loop transfer function in (2.3.7) with respect to s are calculated. The zeros in the open loop transfer function are the zeros of the numerator with respect to s. Solving these equations is not trivial. That is why the so-called "Miller Approximation" is used to estimate the poles and zeros [53]. Even though C. A. Makris states in [46] that the errors by these approximations are not negligible, it is used here because it gives a rough estimation of the poles.

The transfer function of a second order linear system without any zeros is:

$$H(s) = \frac{1}{1 + as + bs^2} = \frac{1}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)}$$

If the poles are sufficiently widespread, the function can be approximated:

$$H(s) \approx \frac{1}{(1 + as)\left(1 + \frac{b}{a}s\right)}$$

In this case the pole frequencies are:

$$p_1 \approx -\frac{1}{a} \qquad p_2 \approx -\frac{a}{b}$$

Thus the poles of the open loop transfer function are:

$$p_1 = -\frac{1}{R_1 (C_1 + C_M) + R_2 (C_2 + C_M) + R_1 R_2 g_{m_2} C_M} \approx -\frac{1}{R_1 R_2 g_{m_2} C_M} \tag{2.3.8a}$$

$$p_2 = -\frac{R_1 R_2 g_{m_2} C_M}{R_1 R_2 (C_1 C_2 + C_1 C_M + C_2 C_M)} = -\frac{g_{m_2} C_M}{C_1 C_2 + C_1 C_M + C_2 C_M} \tag{2.3.8b}$$

The zero is obtained by setting the numerator of (2.3.7) equal to zero and solving the equation with respect to s.

$$z = \frac{g_{m_2}}{C_M} \tag{2.3.9}$$

The circuit has also been simulated using the double injection method. The results obtained by this method support (2.3.8a-b) and (2.3.9).

As for the regulator presented in Chapter 2.3.2, a pole-zero doublet is generated by the current mirror inside the error amplifier (refer to Figure 2.31). The pole frequency is slightly higher than the frequency of p_2 in (2.3.8b). Thus the phase is decreasing rapidly beyond this frequency. That means that the compensation capacitor C_M has to be sufficiently large to ensure stability. Choosing 10 pF results in a phase margin of 89°. This value seems large. As during the design phase the capacitive load of the BAW oscillator was unknown, the phase margin is designed to have enough margin.

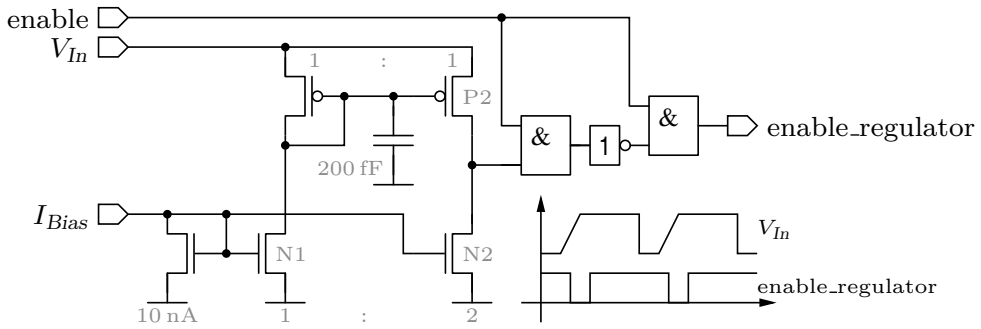


Figure 2.33: Input transient monitor

Startup Control

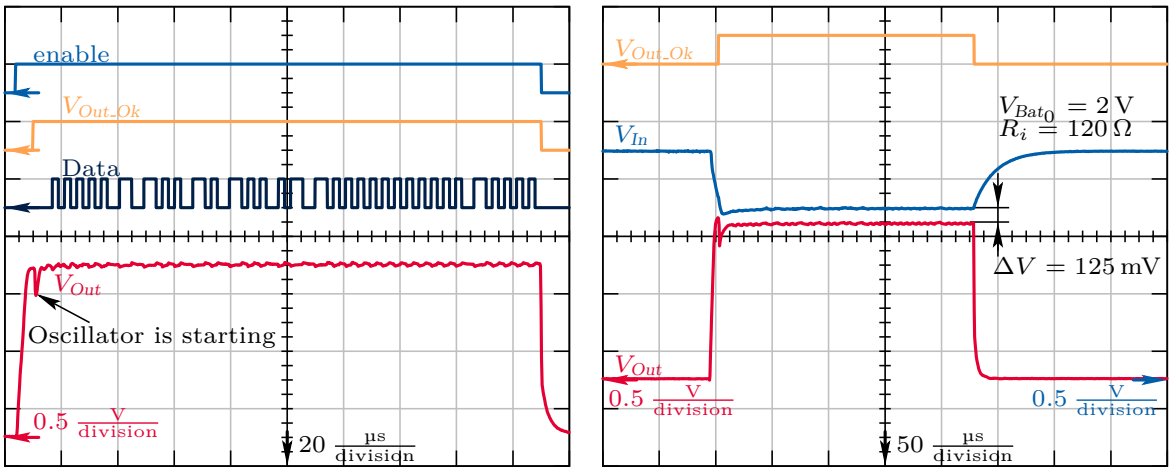
The frequency compensation of the regulator is done using a capacitor between the drain and the gate of the pass device. Thus the "Miller Effect" increases the equivalent input capacitor. The drawback of this method is that line and load regulation capabilities become worse. As no fast transient either at the load or the line side is expected, these parameters are not crucial.

When the regulator is enabled, V_{In} rises fast. Thus precautionary measures are taken to prevent an overshoot of the output voltage. The power management of the WSN switches V_{In} to V_{Harv} when the regulator is enabled. Thus V_{Harv} is always available before V_{In}. As indicated in Figure 2.31, during the phase when the regulator is disabled, the gate of the pass device is pulled to V_{Harv}. So it is ensured that the pass device is non-conductive at the time of enabling the regulator. To make sure no current is drawn from the sensitive supply V_{Harv}, a switch is inserted between the output of the error amplifier and the pull-up. In addition to this pull-up, the reference voltage is fed into a lowpass filter. The output of this filter rises slowly during startup. Thus at the beginning the regulator is forced to regulate its output voltage towards zero. The bias current of the error amplifier is generated by a constant-gm cell. This cell is disabled until the enable signal changes to high state. So the bias current of the error amplifier is also increased slowly. The measurement results discussed later on prove a smooth startup.

Input Transient Monitor

During the design phase it was not ensured that fast rising transients on the input voltage are impossible. As overshoots on the output voltage have to be prevented at any costs, an input voltage monitor is implemented. This monitor switches the pass device off if fast rising transients on the input voltage occur.

Figure 2.33 shows the circuit for the input voltage monitoring. It operates between the enable signal which is used to enable the regulator and the enable signal which actually enables the regulator's output. During normal operation, meaning a stable input voltage, N2 pulls the input of the AND gate to ground, as it is designed to draw twice the current of P2. If the input



(a) Operation cycle of one data transmission

(b) WSN supplied with a battery

Figure 2.34: Measurement results of the regulator used for the carrier generation unit

voltage is rising fast, the gate-source voltage of P2 is increased as the gate is held to ground by the capacitor. Thus the current generated by P2 gets higher than the current drawn by N2 and the input of the AND gate rises causing *enable_regulator* changing to zero. As soon as the potential of the capacitor is restored by N1, the output of the monitor changes to high state again. To monitor dropping input voltages, a similar architecture is possible. In this case the capacitor is connected between V_{In} and the gate of the PMOS current mirror. The width of $P2$ has to be doubled and the width of N2 needs to be halved. This circuit does not improve the line regulation capabilities. It only protects the load of the regulator against too high voltage peaks.

Measurement Results

A standalone version of the regulator is not available. Thus, only a few measurement results are done. Parameters not accessible by measurement are obtained by simulation.

The startup behavior of the regulator is of great interest, as in this phase the regulator undergoes a fast input voltage transient. Figure 2.34a shows one operation cycle of the data transmission. The curve of V_{Out} proves a smooth startup without any overshoot. After the startup is completed, the output voltage sensor of the regulator sets V_{Out_Ok} high and the on-chip oscillator starts. The current pulse of the carrier generation unit when the oscillator starts causes a voltage drop of V_{Out} of approximately 200 mV. As no BAW device was available during measurement, the results show the behavior of the regulator using the on-chip ring oscillator. The output voltage of the regulator shows a ripple of approximately 30 mV. These pulses are generated by a buffer inside the carrier generation unit which generates current peaks up to 3.5 mA. This buffer should be supplied by the regulator used for the power amplifier. A misunderstanding during the top-level design led to this mistake.

	this work	[44] by K. N. Leung	[33] by P. Hazucha	[41] by S. K. Lau	[48] by T. Y. Man
Tech.	0.12 µm	0.6 µm	0.09 µm	0.35 µm	0.35 µm
V_{In}	1.5 V	1.5 V	1.2 V	1.2 V	1.0 V
V_{DO}	0.125 V	0.2 V	0.3 V	0.2 V	0.1 V
I_{Load_Max}	20 mA	100 mA	100 mA	100 mA	100 mA
I_Q	0.065 mA	0.38 mA	6 mA	0.1 mA	0.0012 mA
T_R	3.4 µs	2 µs	0.00054 µs	50 µs	2.8 µs
Active area	0.016 mm^2	0.31 mm^2	0.09 mm^2	0.12 mm^2	0.09 mm^2
FOM	11.8 ns	0.76 ns	0.032 ns	50 ns	0.067 ns
FOM2	0.176 ns mm^2	0.24 ns mm^2	0.003 ns mm^2	6 ns mm^2	0.006 ns mm^2

Table 2.4: Performance comparison of the regulator used for the carrier generation unit to recent published similar work

One application scenario of the WSN is to operate it as a general purpose sensor node having an active transmitter. In this case the node is supplied by a battery. During the lifetime of the battery the open-circuit voltage decreases to 2 V and the internal resistance increases to 100 Ω [19]. Clearly, the critical operation point is at the end of the lifetime of the battery. Figure 2.34b shows the measurement of the regulator at this operation point. Using a voltage source having an open-circuit voltage of 2 V and a series resistor of 120 Ω emulates an empty battery. As a result of the current of the carrier generation unit, the input voltage of the regulator drops to 1.5 V. The voltage drop over the pass device is 125 mV. Thus the resulting output voltage is 1.38 V. This is the minimum allowed limit of the output voltage. That is why V_{Out_Ok} still signals that the output of the regulator is high enough.

Comparison and Conclusion

This section briefly discussed the voltage regulator implemented for the carrier generation unit. No off-chip components are required. Compensation is achieved by a Miller Capacitor inside the error amplifier. Thus, the dominant pole is not at the load side as usual. Clearly, this limits the load and line regulation capabilities, but allows a low power implementation. As no fast transient either at the input or the line side appears, load and line regulation capabilities are not crucial. A startup control handles the fast rising input voltage when the regulator is enabled. Additionally, a circuit monitoring input voltage transients was presented.

Table 2.5 summarizes the most important performance parameters of the regulator. T. Y. Man introduces in [48] a Figure of Merit (FOM) to compare such regulators. (2.3.10a) shows the equation for this FOM. T_R is the recovery time of the regulator after a load current pulse, I_Q is the quiescent current and I_{Load_Max} is the maximum load current. Clearly, to achieve good results adaptive biasing is required. Considering the fact that adaptive biasing is not used here, the achieved FOM = 11.8 µs is comparable to FOM = 0.067 µs presented in [48]. A more representative FOM takes the area consumption into account. (2.3.10b) presents this FOM.

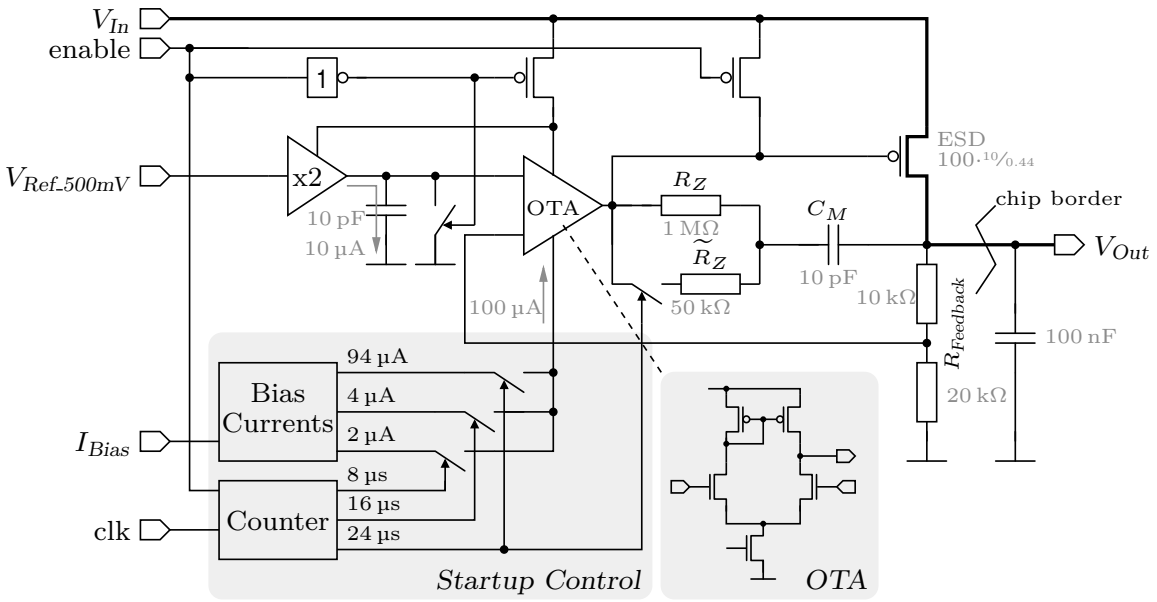


Figure 2.35: Simplified architecture of the regulator supplying the power amplifier

T. Y. Man presents in [48] a comparison of different regulator architectures. These results are shown in Table 2.4 and compared to the results of this regulator.

$$\text{FOM} = \frac{T_R \cdot I_Q}{I_{Load\_Max}} \tag{2.3.10a}$$

$$\text{FOM2} = \frac{T_R \cdot I_Q}{I_{Load\_Max}} \cdot (\text{Active area}) \tag{2.3.10b}$$

2.3.5 Regulator for the Power Amplifier

This chapter presents the regulator which provides a stable supply voltage for the power amplifier. The power amplifier is of Class E and makes use of an off-chip inductor connected between the output of the power amplifier and the voltage regulator. The power amplifier supports different power levels. For the nominal power level, the current consumption of the amplifier is 2 mA at a nominal supply voltage of 1.5 V.

Although the regulator is slightly off-topic as it is no ultra-low power design and it makes use of an off-chip capacitor, it is discussed briefly for the sake of completeness.

Regulator Architecture

As the inductor used for the power amplifier requires a pin, this pin is also exploited to use an off-chip capacitor for the regulator. The architecture of the regulator is shown in Figure 2.35. The pass device is a PMOS transistor. A startup control improves the startup time and prevents

overshoots. The dominant pole is formed by the load and the large off-chip capacitor. Thus the internal poles have to be at high frequencies. So a fast differential pair is used as error amplifier. For the NMOS input of the differential pair, the reference voltage has to be scaled to 1 V using a buffer.

Stability Analysis

As discussed in the introduction of this regulator, the dominant pole is formed by the load. By using (2.3.11a) the absolute value of the pole frequency is estimated between 82 Hz in the no-load case and 12 kHz at a load current of 10 mA. Without a compensation capacitor the non-dominant pole, formed by the pass device and the output resistance of the error amplifier, is between 5.5 MHz and 275 kHz in the same load current range. These results are obtained using (2.3.11b). One good solution to stabilize the regulator is to use a nulling resistor in series to the Miller Capacitor. The frequency of the zero is placed in order to compensate for the first non-dominant pole. A third pole, calculated by (2.3.11d), is generated by the current mirror inside the error amplifier. The pole frequency is at 250 MHz which is far beyond the UGF.

$$|f_{p_{Load}}| = \frac{\frac{1}{R_{Load}} + g_{ds_{Pass}} + \frac{1}{R_{Feedback}}}{2\pi \cdot C_{Load}} \quad (2.3.11a)$$

$$|f_{p_{Pass}}| = \frac{1}{2\pi \cdot C_{Pass} \cdot R_{Out_{OTA}}} \quad (2.3.11b)$$

$$f_z = \frac{1}{2\pi \cdot C_M \cdot \left(\frac{1}{g_{m_{Pass}}} - R_Z\right)} \quad (2.3.11c)$$

$$|f_{p_{Mirror}}| = \frac{g_{m_{Mirror}}}{2\pi \cdot C_{Node}} \quad (2.3.11d)$$

Startup Control

As indicated in Figure 2.35, the regulator makes use of a startup control. When the regulator is enabled, no load is present. If the output capacitor is loaded too fast, the output voltage becomes too high. This voltage level remains for a long time if no load is present. Thus the gate potential of the pass device is decreased slowly to prevent this current by: (1) increasing the bias current step by step, (2) slowly increasing the reference voltage, and (3) switching of the nulling resistor.

Increasing the bias current step by step has the effect that the current available to discharge the gate of the pass device is low. By increasing the reference slowly, the error amplifier tends to regulate the output of the regulator towards zero. By switching the nulling resistor, the zero frequency is shifted towards lower frequencies and the regulator becomes slow from the small-signal's point of view as the phase margin is increased. The most influential and thus the most effective method is increasing the reference voltage slowly. Of course, this method requires a buffer, which results in an increase of the current consumption of the regulator. The other two methods require additional area on the die, but no additional current.

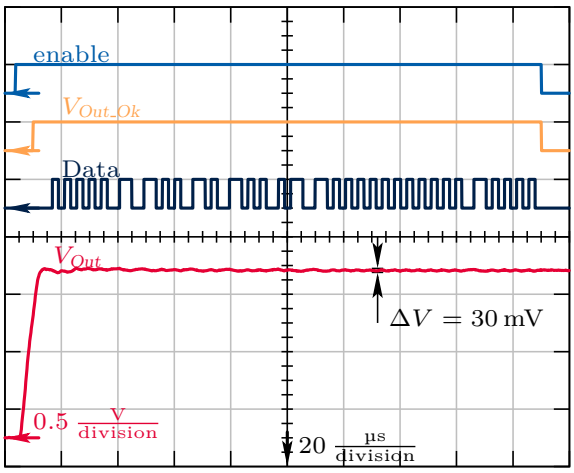


Figure 2.36: Transient output of the regulator

Results and Conclusion

The briefly discussed regulator is measured to verify the functionality. Measurements are only available in the environment of the WSN as no separate test chip is fabricated. For the proof of functionality, the measured transient output of the regulator is shown in Figure 2.36. The measured voltage ripples related to the data pulses are 30 mV. Compared to simulation, where the ripple is evaluated with a value of 3 mV, this value seems large. The reason is that the power amplifier is not operating in Class E mode, because an appropriate matching network was not available. In the unmatched case, the power amplifier draws current peaks whereas in Class E operation the current drawn from the regulator is much more smooth.

The most important performance parameters are listed in Table 2.5. As no test chip is available, these values are obtained by a post-layout simulation.

2.4 Conclusion

Chapter 2 presented a WSN dedicated to but not exclusively designed for in-tire TPMSs. After a short introduction to the possible applications, the power management was introduced. The focus of this chapter was on how the different voltage regulators used to generate the required supply voltage on the IC are designed.

Two ultra-low power regulators using an NMOS pass device and two regulators using a PMOS pass device were presented. The NMOS regulators have a current consumption of about 1 µA. With this low current a trade-off between power awareness and robustness in terms of line and load regulation is found. The results of the NMOS regulators are compared to actual publications. This comparison emphasizes that a reduction of the current consumption leads to worse regulation capabilities. Also, the energy consumption of the system is potentially increased by a longer startup time. The PMOS regulators are quite different in their architecture.

	Regulator for the carrier generation unit	Regulator for the power amplifier
Output voltage	1.5 V	1.5 V
Nominal load	4 mA	2 mA
Input voltage range	1.5 V to 3.3 V	1.5 V to 3.3 V
Quiescent current	65 µA	200 µA
Line sensitivity	6.3 mV/V	1.8 mV/V
DC output resistance	355 mΩ	2 Ω
Load pulse settling time ($0 \rightarrow 4$ mA; 3 %)	2.1 µs	drop not below 3 %
Load pulse settling time (4 mA $\rightarrow$ 0; 3 %)	2.0 µs	drop not below 3 %
Load pulse settling time ($0 \rightarrow$ max. load 3 %)	3.4 µs	drop not below 3 %
Start-up settling time ($0 \rightarrow 3.3$ V)	12 µs	23 µs
Maximum load current	20 mA	30 mA
Maximum input slew rate ($3.3 \rightarrow 1.5$ V)	400 kV/s	n.r.
PSRR at DC ($V_{In} = 3.3$)	−51 dB	−63 dB
Chip area	0.016 mm^2	0.036 mm^2
Off-chip capacitor	none	100 nF

Table 2.5: Performance summary of the regulator used for the carrier generation unit and the regulator for power amplifier

One requires no off-chip capacitor and the compensation is done inside the error amplifier. The other one makes use of an off-chip capacitor to stabilize the feedback network. Generally, an internal compensation makes it hard to get short response times of the regulator on line or load variations. Literature proposes adaptive biasing in this case to get a good trade-off between current consumption and short response times. Here adaptive biasing is not used because a design constraint was to keep the circuits simple. Nevertheless, the results are comparable to actual publications.

This chapter proves that it is possible to implement voltage regulators providing good regulation capabilities requiring only a few microampere in a 0.13 µm CMOS process. The circuits operate reliably in the temperature range of −40 °C to 125 °C and in all CMOS process corners[§].

[§] When processing variations are combined with environmental variations, we define design or process corners [90].

Chapter 3

A Robust and Fault Tolerant Switched Capacitor Regulator

> Things should be made as simple as possible, but not simpler.
>
> *(Albert Einstein)*

3.1 Introduction

The following chapter is mainly taken from [28] (own publications). ■

Wireless Sensor Nodes (WSNs) have a wide range of applications [3]. One famous scenario is distributing a large number of nodes over some area. An example regarding this utilization of WSNs was the Smart Dust project [36]. One design goal of this project was to miniaturize the sensor node down to $1\,\mathrm{mm}^3$. Another famous recently published scenario is an intraocular pressure monitor [13] (preliminary work [14, 78]). Here the node size is limited to $1.5\,\mathrm{mm}^3$. These two examples have in common shrinking the WSN down to very small values. A major limiting factor in the shrinking process is the energy density of the power supply, which is usually a battery. The energy stored in a battery or capacitor is:

$$E = \frac{C}{2} \cdot V^2 \tag{3.1.1}$$

C is the capacitance and V is the voltage across the terminals. Thus it is preferable to use high voltage levels to increase the amount of stored energy. The average dynamic power consumption of a digital Integrated Circuit (IC) is:

$$\overline{P}_{Dyn} \propto C \cdot V^2 \cdot f_{Clk} \tag{3.1.2}$$

C is the equivalent load capacitance, f_{Clk} is the clock frequency, and V the supply voltage. Clearly, to minimize the power consumption the supply voltage should be reduced. Reducing the supply voltage for the IC is in contradiction to increasing the voltage on the energy storage device. Efficient DC/DC converters solve this problem.

If a linear regulator does this voltage level conversion, the maximum achievable conversion efficiency is very low because of the large voltage drop on the pass device (refer to (1.5.2a)). Additionally, so as not to unnecessarily increase the volume of the WSN a fully integrated

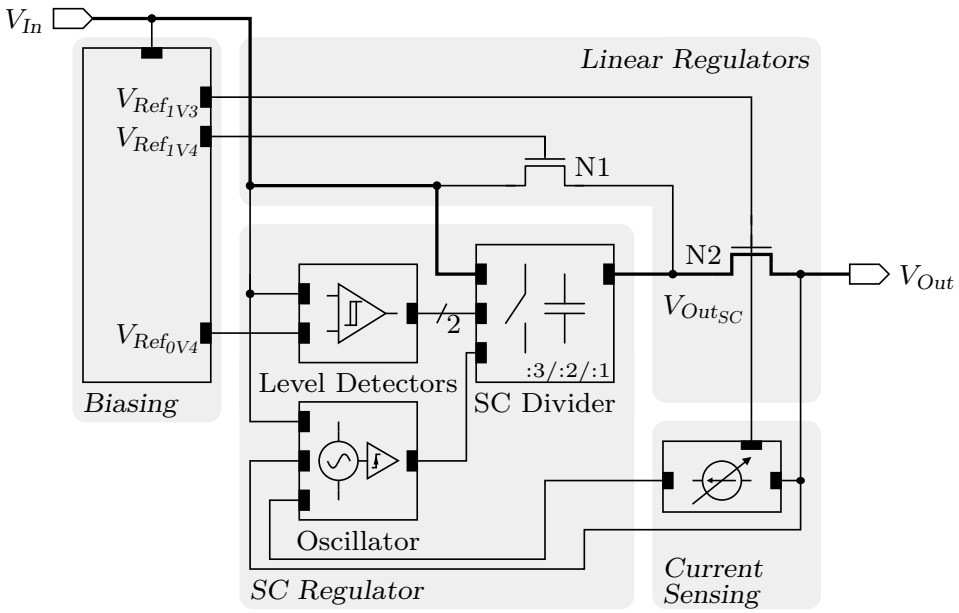


Figure 3.1: Simplified block diagram of the hybrid DC/DC converter

voltage conversion is preferable. Summing up, to enable tiny self-sustained WSNs a fully integrated and highly efficient DC/DC conversion is required. This conclusion is supported by Y. Manoli in [47]. Referring to Table 1.1 on page 3, Switched Capacitor (SC) regulators are best suitable to fulfill these requirements.

As discussed in Chapter 1.2 and summarized in Table 1.1, SC regulators have a slow dynamic response. Thus these types of regulators cannot be used when fast transients at either the load or the line side are expected. This limits the selection of possible power sources for the WSN. Linear regulators provide a fast dynamic response. Thus if an SC regulator and a linear regulator are combined in a smart way, both problems can be solved. The SC regulator provides a highly efficient conversion of the voltage, while the linear regulator only operates on fast transients. This chapter presents a regulator which achieves both, a high conversion efficiency and a fast dynamic response. After a short introduction to this hybrid regulator, the individual building blocks are presented. The chapter concludes with measurement results and a comparison to recent publications.

3.2 A Hybrid DC/DC Converter

The introduction of this chapter proposes to combine a linear and an SC regulator to gain the advantages of both. Such a combination is shown in Figure 3.1. The regulator itself is composed of two nested stages: An SC regulator is embedded within a two-stage linear regulator. While the SC regulator provides a highly efficient pre-scaling of the input voltage, the linear regulator in parallel ensures a fast transient response. At the output of the SC regulator a linear regulator ensures a stable output voltage.

A related architecture is proposed by H. Martinez in [49]. H. Martinez combines a switched inductor regulator and a linear regulator in a similar way. In addition to improving the dynamic response by this linear-assisted topology, the output voltage ripple of the switched regulator is reduced. In the design presented here, the output voltage ripple is not of much interest, even if the ripple generated by the SC regulator is reduced by the two-stage linear regulator.

Depending on the voltage level, the SC regulator divides the input voltage by three or by two. For low input voltages, the divider is turned off. As the output of the SC regulator depends on the input voltage, N2 is used to set the output voltage to a constant value of 0.8 V. The response time of the SC divider is slow compared to a linear regulator. This drawback is solved using an additional linear regulator in parallel (N1). This regulator only operates on fast load or line variations. During normal operation the SC regulator provides a highly efficient conversion of the input voltage while during fast transients the linear regulator provides good regulation capabilities. If the output of the SC regulator is too low to achieve the required output voltage of the regulator, N1 conducts and provides the required load current.

To keep the efficiency high for increasing load currents, either the size of the capacitors or the oscillator frequency must be increased. Otherwise, the necessary charge cannot be provided by the SC regulator. Of course, adapting the capacitor size depending on the load current shows a better conversion efficiency, but increasing the oscillator frequency is more efficient in terms of area consumption. For this implementation the method of increasing the frequency is chosen. To achieve this frequency variation, the load current is measured and a small part of it is used to bias the oscillator.

The nominal output voltage is 0.8 V and the nominal load current is 1 µA. For this implementation the gate voltage of the pass devices is held constant. Of course, the combination of an SC regulator with a linear regulator, as presented here, can also be used with a regulated pass device.

The regulator requires various circuits operating in the ultra-low power domain. These blocks are the biasing block, an oscillator, and level detectors. They are discussed in the following sections. For each of these blocks, measurement results conclude the corresponding section. Additionally, transient analysis of the regulator is presented.

3.2.1 Switched Capacitor Divider

The core of the hybrid regulator is composed by an SC regulator. This circuit, depicted in Figure 3.2, achieves the highly efficient conversion of the input voltage. The input voltage is divided by the SC regulator by alternatingly switching capacitors in series or parallel. If three capacitors are connected in series and afterwards in parallel, the voltage level is divided by three. Using two capacitors leads to a halved input voltage.

If the signal *div_by3* is at V_{In} level, the circuit divides by three, and by two if *div_by3* is set to ground level. If the clock signals (Φ_1 and Φ_2) are set to ground level, the divider is turned off. The capacitors are realized as MOS capacitors with a capacity of 25 pF each.

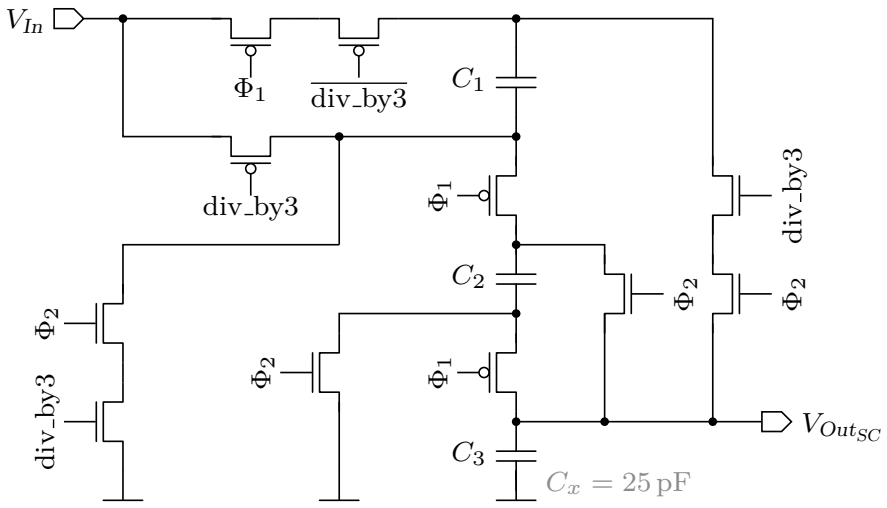
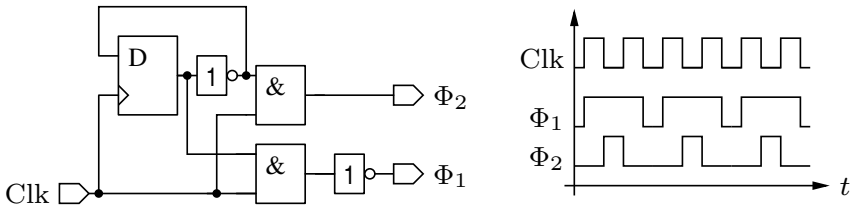


Figure 3.2: SC regulator



(a) Circuit (b) Clock pulses

Figure 3.3: Non-overlapping clock generation

To control the switches in the SC divider, digital gates are required. For instance the clock signal Φ_2 and the signal *div_by3* must be conjugated. To save power, digital gates are omitted. An AND gate consumes approximately 20 nA at 200 kHz at a supply voltage of 3 V. This current is saved by using two transistors in series instead of using the AND gate. Similarly, other logic functions are realized.

Generally, a non-overlapping clock is required to drive the SC regulator. Early implementations make use of the non-overlapping clock generator shown in Figure 3.3a. It turned out that the non-overlapping clock pulses shown in Figure 3.3b are an ineffective approach. During Φ_1 being high and Φ_2 being low, C_3 would be the only source supplying the load. This would require a large buffer capacitor to achieve a high conversion efficiency. Reducing the duration of this gap in the clock signals requires a more advanced clock generation circuit. As this means an increase of the current consumption of the regulator, an overlapping clock is used instead. Short clock transition times keep the effects caused by the overlapping negligible. Simulations showed that these losses are below 1.0 %.

Figure 3.4 shows the transient behavior of the SC divider when using an overlapping and a non-overlapping clock. In the non-overlapping case three states are distinguished: (1) all

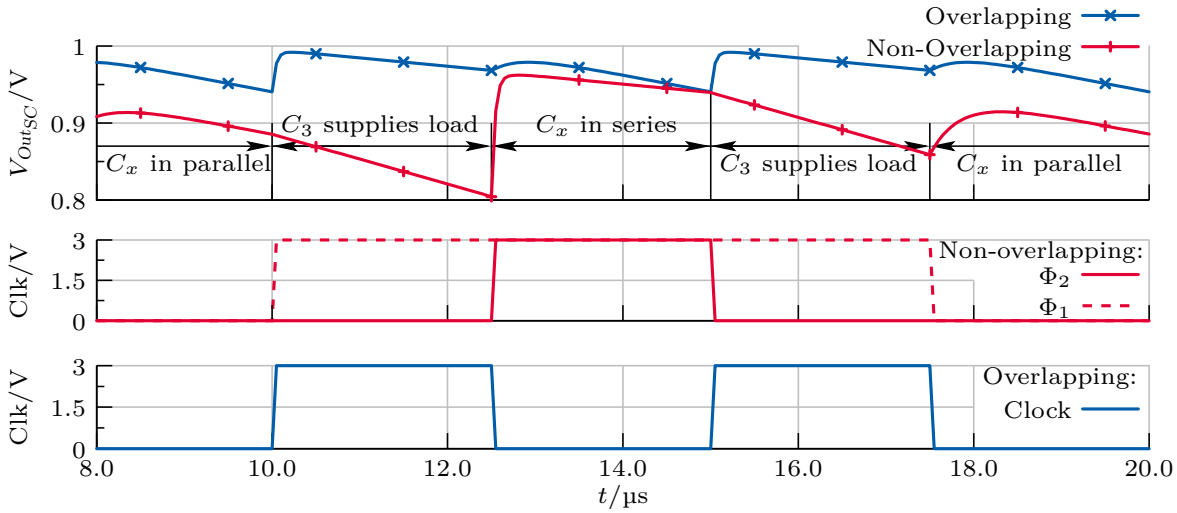


Figure 3.4: Comparison of the output of the SC divider using a non-overlapping and an overlapping clock

capacitors are in parallel (C_x in parallel), (2) only the output capacitor supplies the load, and (3) all capacitors are in series (C_x in series). When overlapping clock signals are used, the second state does not occur. Here the capacitors are alternatingly connected in series and in parallel without any dead time. This results in less voltage ripple and a slightly higher output voltage.

Due to the low current in ultra-low power designs, the on-resistance of the transistors used as switches can be neglected. Here the capacitance between the gate and the channel is crucial. The higher this capacitance is the more current is needed to drive the switch. Additionally, charge injection from the switch into the SC network reduces the efficiency. The reason is that the voltage ripple (ΔV_{Out}) is increased. According to (1.5.2b), the higher the voltage ripple is, the lower the efficiency is.

To keep the are consumption small, the flying capacitors are formed by MOS capacitors. The capacitance of MOS capacitors is strongly non-linear depending on the voltage across the terminals. If the gate-source voltage is in the region of the threshold voltage or below, the capacitance is decreasing because the conductive channel beneath the gate is not formed. Thus the voltage divider requires a sufficiently high voltage difference across the capacitors. The hybrid regulator is designed to provide a nominal output voltage of 0.8 V. So the gate-source voltage of the capacitors is at least 0.8 V, which is high enough to form the required channel. As the load current is in the microampere range, the Equivalent Series Resistance (ESR) of the capacitor is negligible. In Chapter 3.2.6 it will be discussed that the parasitic capacitor of the n-well to the substrate reduces the efficiency significantly.

3.2.2 Bias Block

A voltage regulator requires a reference voltage level which predetermines the output voltage of the regulator. The reference has a significant influence on the overall performance parameters of the regulator. Here the current consumption of the regulator is of major concern. Thus an ultra-low power reference cell is implemented.

The regulator requires different reference voltages (refer to Figure 3.1). So the output of the reference cell is scaled to the required values. In addition to the voltage reference a bias current is generated. It is used to bias the different circuits operating for the hybrid regulator. The nominal bias current is as low as 1 nA to minimize the current consumption of the regulator. The reference cell has a current consumption below 20 nA. Both the reference cell and the scaling are discussed in this section.

Current and Voltage Reference

Bandgap references as discussed in literature like [68] are commonly used in CMOS circuits. The operating principle is to add a voltage with a Negative Temperature Coefficient (NTC) to a voltage with a Positive Temperature Coefficient (PTC). The voltage with an NTC is generated over a pn-junction (in CMOS this is usually a lateral pnp transistor). The temperature coefficient of this pn-junction is approximately $-2\,\mathrm{mV/K}$. As a current having a PTC can easily be generated in CMOS technology, the voltage with a positive temperature coefficient is obtained from a resistor which is biased by this current.

To reduce the current consumption of the bandgap reference and the nominal value of the reference current, the resistor has to be increased to values larger $1\,\mathrm{M\Omega}$. This leads to a huge area consumption on silicon, when high-resistive polysilicon resistors are not available in the CMOS process. Especially for low cost processes, like the one used in this thesis, such resistors are not available. So different solutions have to be found. One approach is to exploit the different operating regions of MOS transistors to obtain a voltage independent of the temperature [60, 79, 82–87]. The advantage of this approach is that the area consumption can be decreased compared to standard bandgap references. A major drawback is that the statistical variance and the temperature variation of the reference voltage is usually worse.

Figure 3.5 shows the circuit of the implemented bias cell. It is the combination of two publications: The PTAT generator proposed by F. Serra-Graells in [79] generates a reference current which is translated into a reference voltage using the active load presented by G. D. Vita in [87]. Both blocks are connected via a feedback path.

The PTAT generator is a modified version of the commonly known “Delta-Vth-Bias” circuit. Figure 3.6a shows this circuit. If the NMOS transistors operate in weak operation, the reference current can be calculated using (3.2.1a). The voltage drop over the resistor is described by (3.2.1b). n is the slope factor as in (1.3.1), N is the ratio of the NMOS transistors, and V_T the thermal voltage. Looking at (3.2.1b) shows that the voltage only depends on fundamental

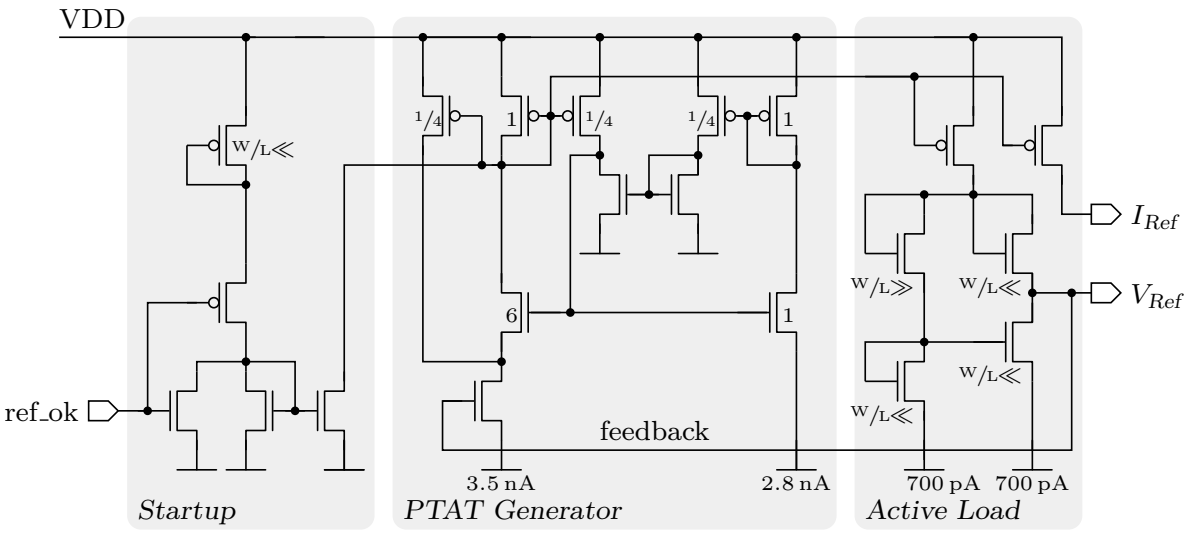
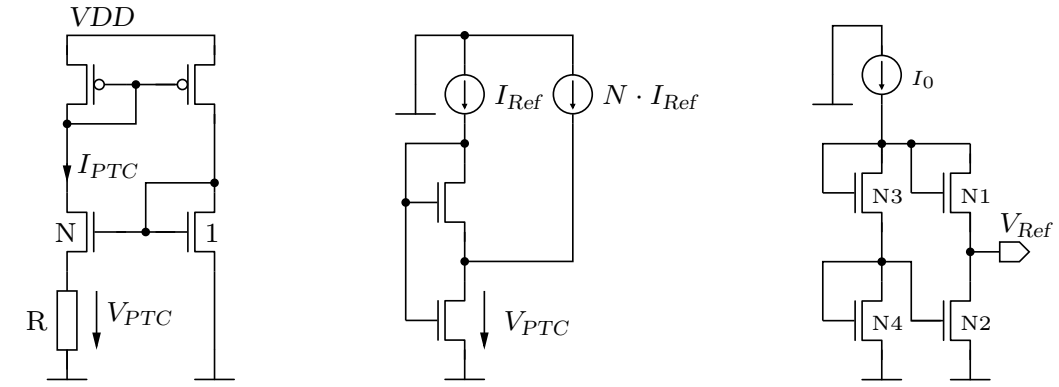


Figure 3.5: Bias cell



(a) Delta-Vth-Bias circuit

(b) Self-cascode MOSFET (SCM) [12]

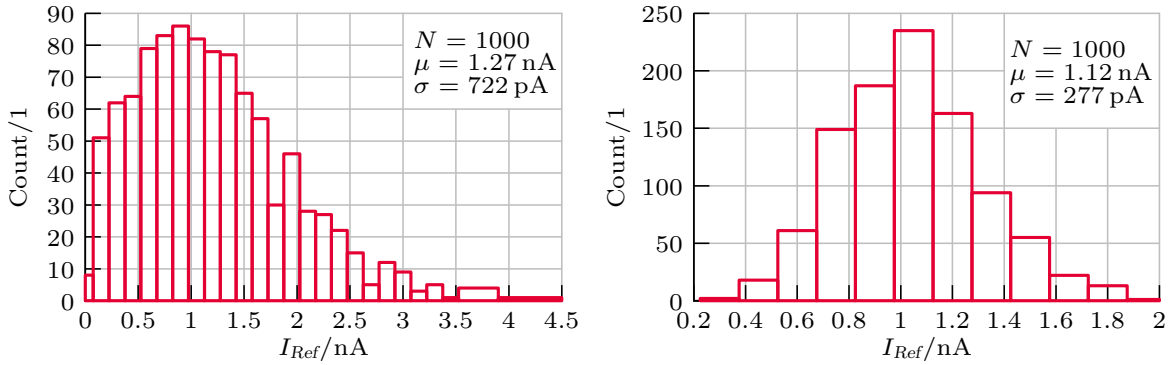
(c) Active load as proposed in [87]

Figure 3.6: Building blocks of the bias cell

constants and, most importantly, not on the resistor. That is why F. Serra-Graells denotes this voltage "reference voltage" in [79]. As a result of V_T it has a PTC.

$$I_{PTC} = {}^1\!/\!_R \cdot n \cdot V_T \cdot \ln(N) \qquad (3.2.1a) \qquad V_{PTC} = n \cdot V_T \cdot \ln(N) \qquad (3.2.1b)$$

There are various methods to implement the resistor in CMOS technology. Most common is using polysilicon resistors. As they require a large area on silicon other methods have to be found in ultra-low power design. In [79] the so-called Self-cascode MOSFET (SCM) [12] is used. Figure 3.6b shows this circuit. The upper transistor operates in the saturation region, while the lower transistor operates in the triode region. C. C. Enz already proposed in [20] in 1996 to use this circuit for Proportional to Absolute Temperature (PTAT) voltage references. Using the SCM instead of a polysilicon resistor increases the variance of the reference current



(a) SCM instead of polysilicon resistor

(b) SCM enhanced by feedback loop

Figure 3.7: Distribution of the reference current

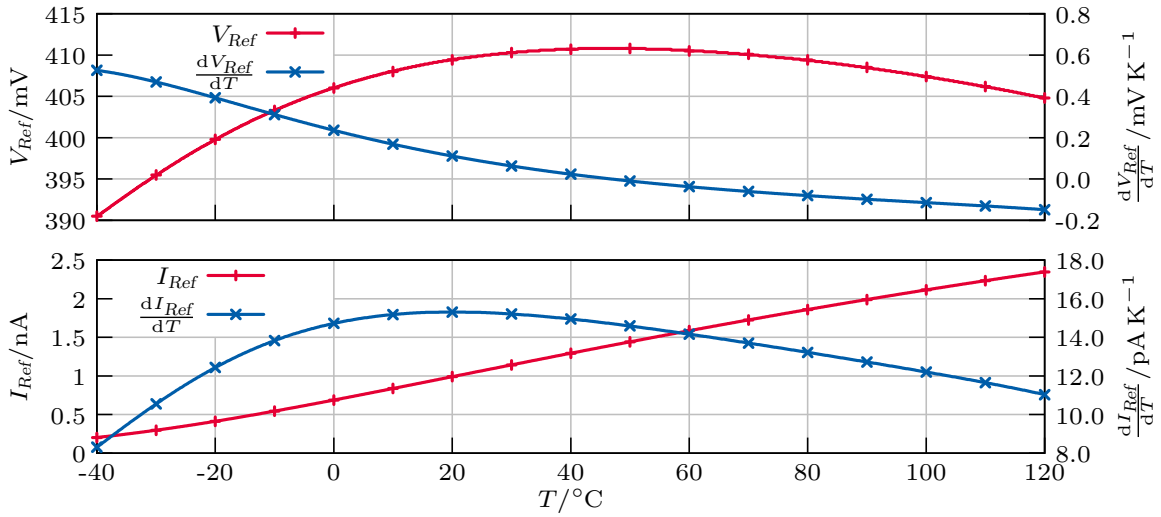


Figure 3.8: Temperature behavior of the reference voltage and the reference current

in the statistic distribution. A feedback loop from the active load to the PTAT generator, as shown in Figure 3.5, prevents the increase of the variance partially. The difference in the distribution of the reference current when using the SCM in comparison to the feedback is shown in Figure 3.7.

Figure 3.8 shows the dependency of the reference voltage and the reference current on the temperature. Considering the fact that the overall current consumption at a reasonable active area is only 15.9 nA, the results are quite good. For a better illustration, the derivatives of the reference voltage and the reference current are also shown.

Table 3.1 summarizes the simulated performance parameters of the reference cell. The values are compared to recent publications.

	this work	[87] by G. D. Vita	[93] P. Yuan
Reference Cell			
Technology	0.13 µm CMOS	0.35 µm CMOS	0.18 µm CMOS
Supply range	0.8 V - 3.3 V	1.5 V - 4.3 V	1 V - 2.5 V
I_{DD}	15.9 nA at 3.3 V	110 nA at 4.3 V	46 nA at 1 V
Active area	0.07 mm^2	0.015 mm^2	0.0036 mm^2
Reference Voltage			
Nominal Value	409 mV	891.1 mV	548 mV
$\sigma(\Delta V_{Ref}/V_{Ref})$	4.15 %	n.r.	n.r.
TC	530 µV/K	10.7 µV/K	16.44 µV/K
Line sensitivity	1 mV/V	19.78 mV/V	0.677 mV/V
PSRR (DC)	−59 dB	−59 dB	$<$ −54 dB
PSRR (10 MHz)	−51 dB	−52 dB	n.r.
Reference Current			
Nominal Value	1.12 nA	n.r.	n.r.
$\sigma(\Delta V_{Ref}/V_{Ref})$	24.8 %	n.r.	n.r.
Line sensitivity	27 pA/V	n.r.	n.r.

Table 3.1: Performance comparison of the reference cell to recent publications

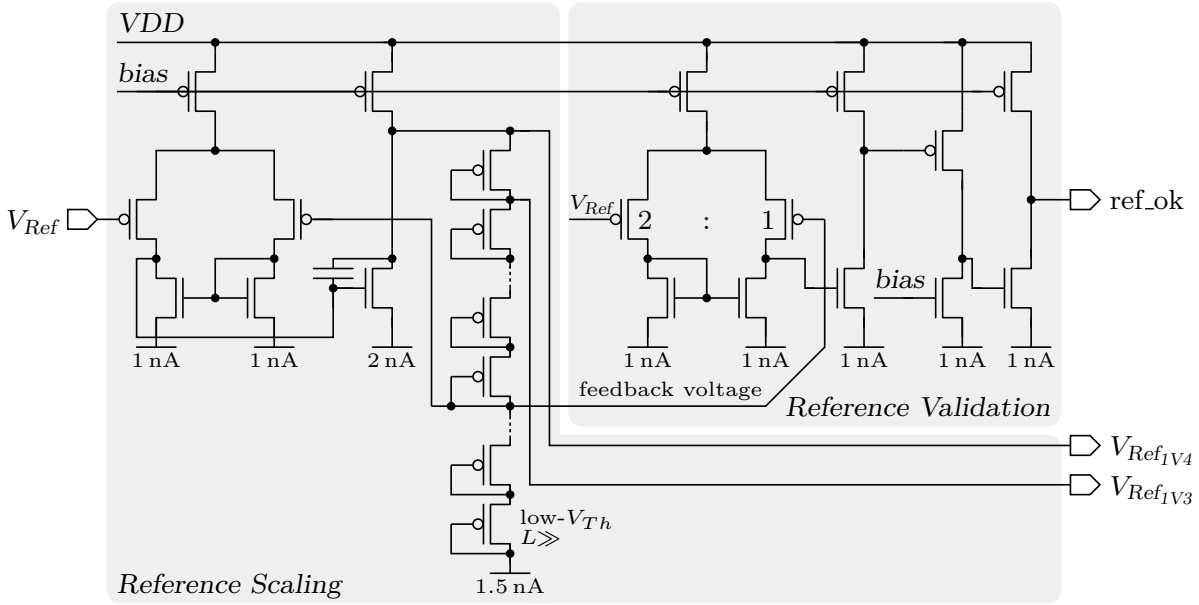


Figure 3.9: Scaling of the reference voltage

Voltage Reference Scaling

The linear regulator requires two reference voltages: 1.4 V and 1.3 V. As the reference cell generates 400 mV, scaling is required. Figure 3.9 shows the circuit used to scale the reference voltage to the required levels. It is composed of two blocks: the scaling of the reference voltage and the validation of the scaling result.

The reference voltage generated by the reference cell is fed into a buffer. The buffer utilizes a voltage divider composed of PMOS diodes. By choosing low threshold devices, it is possible to tap reference voltages with a distance of 100 mV. To determine if the output of the scaling unit is valid, the voltage level in the feedback path is compared to the reference voltage. The comparison is done by a comparator having a defined offset voltage.

The buffer, which scales the reference voltage, is supplied by the input voltage of the hybrid regulator. Due to the very low current consumption of the buffer, it has a bad Power Supply Ripple Rejection (PSRR). This limits the achievable overall PSRR. The overall current consumption is below 15 nA.

3.2.3 Oscillator

The SC divider requires an oscillator having a frequency of a few hundred kilohertz. The design constraint is to achieve this frequency with a minimal amount of power. Two different oscillator architectures are investigated for their suitability. The first architecture is a current-conveyor relaxation oscillator based on [64], and the second one is a current starved ring oscillator.

The oscillator is supplied by the output voltage of the hybrid regulator to exploit the efficient voltage conversion. The SC divider requires a clock having an amplitude equal to the input voltage level. A voltage level shifter generates the required voltage level of the clock. This is the most efficient way in terms of current consumption of the clock generation.

As discussed in the introduction in Chapter 3.2, the oscillation frequency is adapted to load current. How this is done is also discussed in section.

Current conveyor relaxation oscillator

J. Popovic proposes in [64] a current conveyor relaxation oscillator based on the current conveyor shown in [59]. In this paper oscillators having clock frequencies in the megahertz range requiring several microampere are presented. Here the bias current of the oscillator is reduced and the transistors are sized accordingly to reduce the frequency to several 100 kHz and the current consumption to below 100 nA respectively.

Figure 3.10 shows the circuit of the oscillator. Assuming *node1* and *node2* are at high potential, transistor P1 and the current mirror *mirror1* are turned off. N1 and the current mirror *mirror2* are conductive. Thus the node *node2* is pulled to ground. The current mirror *mirror3* also

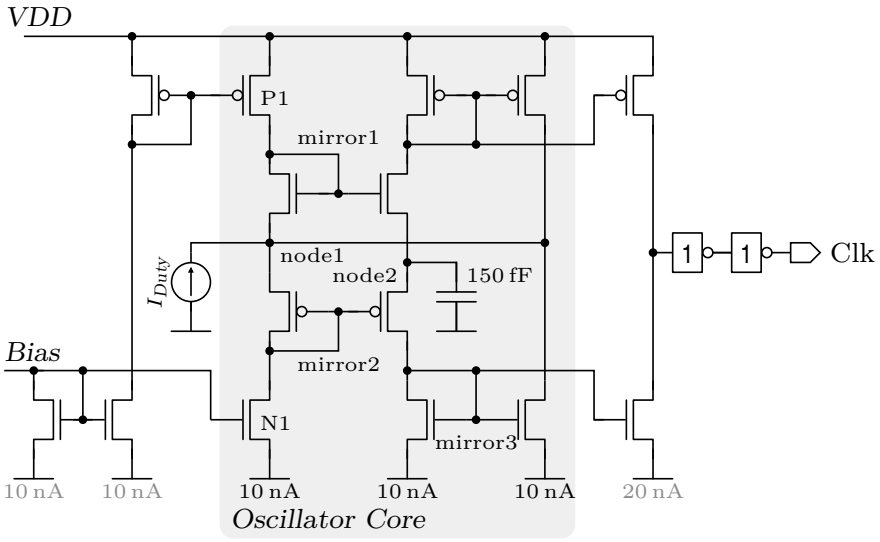


Figure 3.10: Current-conveyor relaxation oscillator proposed in [64]

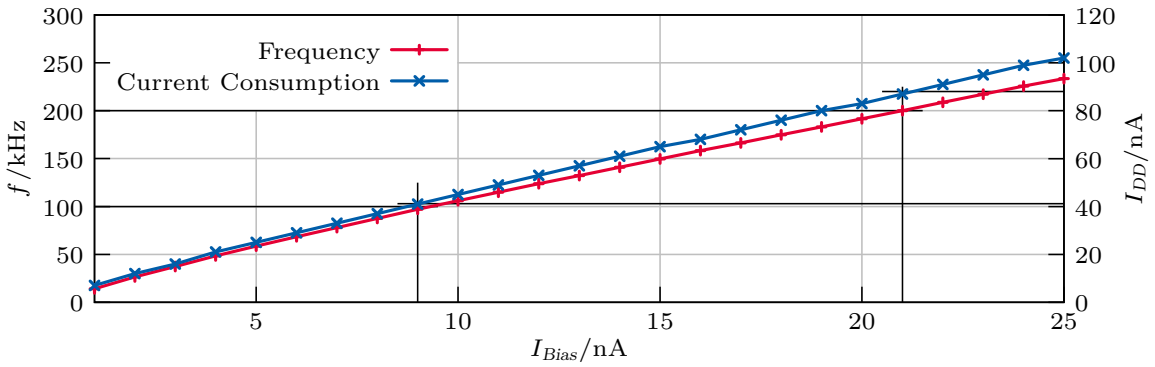


Figure 3.11: Frequency and current consumption of the current-conveyor oscillator at different bias currents at 1 V

pulls *node1* to ground. Concurrently, the transistor P1 and the current *mirror1* get conductive and the nodes *node1* and *node2* are pulled to *VDD* again.

J. Popovic proposes to use an ohmic resistor at node *node1* to adjust the duty cycle. For the ultra-low power implementation, a resistor of several gigaohms would be required. Here, using a current source or sink at *node1* is the better approach if the duty cycle should be adjusted.

The minimal supply voltage level of the oscillator is the sum of two gate-source voltages and two saturation voltages. Measurements showed that at −40 °C at least 1.2 V are required. The output voltage of the hybrid regulator is only 0.8 V. As it is intended to supply the oscillator by this voltage, it cannot be used unless a separate supply generation is implemented. Besides the promising measurement results presented in the following, the oscillator is not utilized to drive the SC divider for this reason.

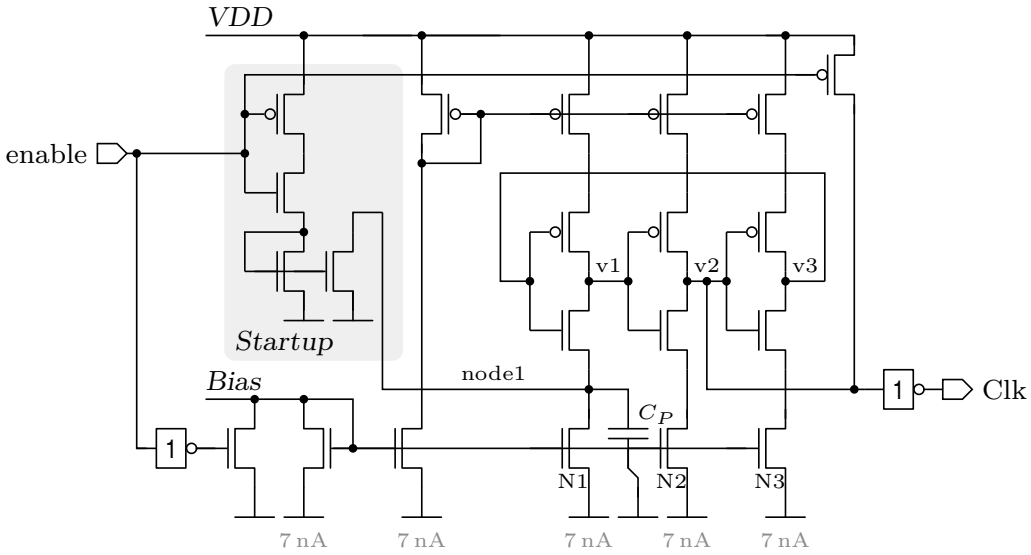


Figure 3.12: Three-stage current starved ring oscillator

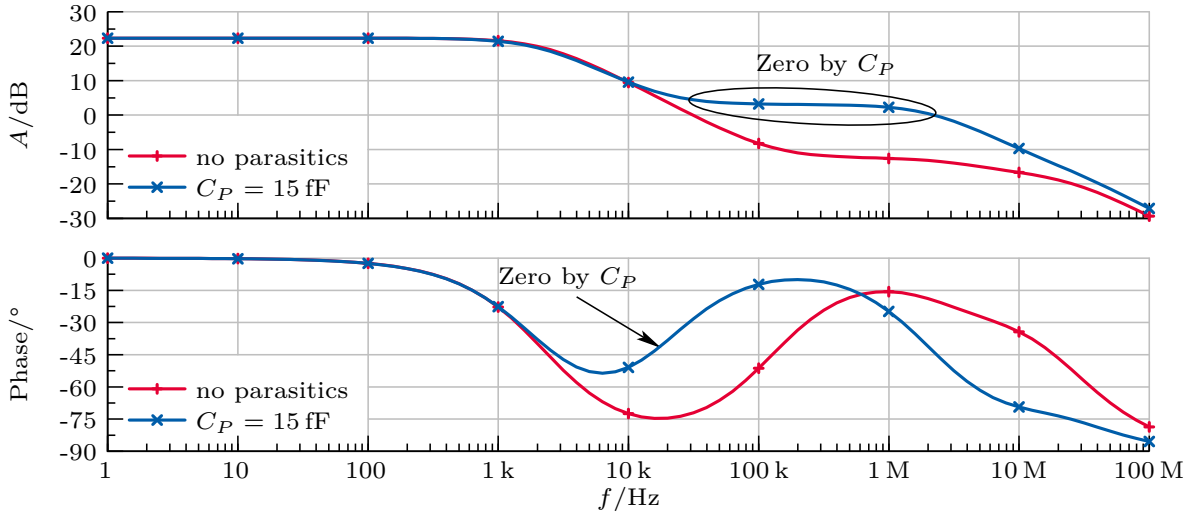
A standalone test chip of the oscillator has been fabricated and measured. Figure 3.11 shows the dependency of the frequency and the current consumption on the bias current at a supply voltage of 1 V. An output frequency of 100 kHz is achieved at a bias current of 9 nA. In this case the current consumption of the oscillator is 41 nA. Using a bias current of 21 nA results in a frequency of 200 kHz and a current consumption of 87 nA.

Current Starved Ring Oscillator

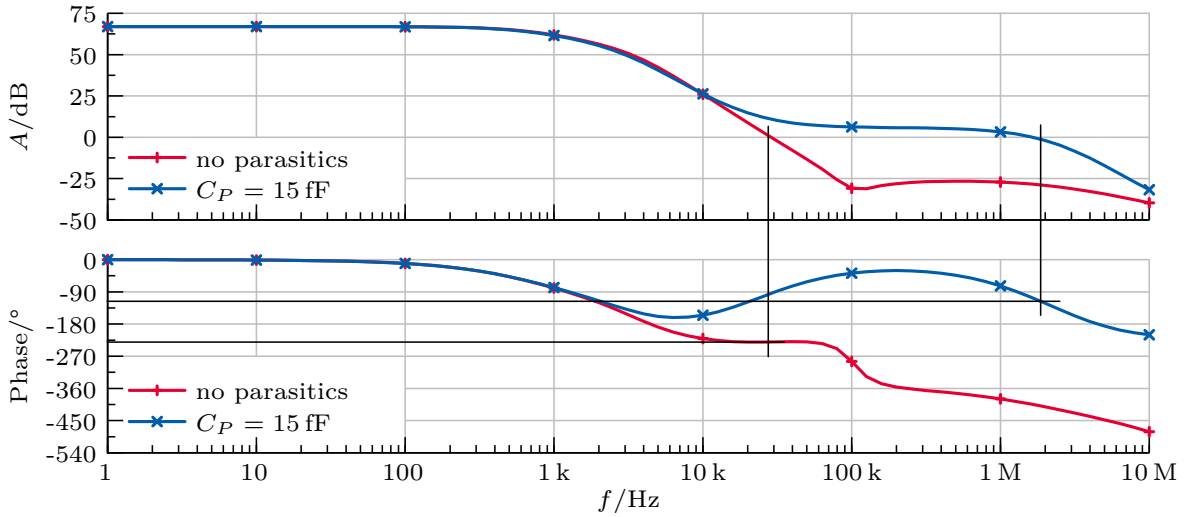
The second investigated architecture is a three-stage current starved ring oscillator. Figure 3.12 shows the circuit. Usually delay elements formed by capacitors and resistors are used to adjust the frequency of the oscillator. Here the current consumption of the oscillator is of most concern, while the absolute frequency is not so important. Thus no resistors or capacitors are used. Omitting these devices leads to startup problems, or in general prevents the oscillator from oscillating. The reason for that are discussed in the following.

Oscillator Startup

Ring oscillators are generally considered to oscillate if the number of stages is odd, as the gain and the phase shift are usually sufficiently high. When omitting the delay elements, the parasitic capacitor at *node1* may prevent the oscillator from starting. Analyzing the startup from the transient's analysis point of view describes this issue well. If the regulator is disabled, *v1* is forced to *VDD* (not shown in the schematic). When the oscillator is enabled, N1 has to drain the parasitic capacitor C_P before *v1* can be pulled to ground. If the current is too small or the capacitor is too large, the capacitor is not drained fast enough and the oscillator stops



(a) Loop gain of the single stage current starved inverter



(b) Loop gain of the three-stage oscillator

Figure 3.13: Loop gain analysis of current starved inverters

oscillating. The startup circuit, also shown in Figure 3.12, drains this capacitor on an enable pulse. The described behavior has been verified by measurement.

By the help of small signal analysis this behavior is also confirmed by simulation. One approach is to do a loop gain analysis. A single stage containing all parasitics of that stage is simulated. Figure 3.13a shows the result. Two cases are distinguished: The red curve shows the transfer function of the inverter without the parasitic capacitor and the blue curve shows the transfer function including the parasitic. Apparently, the parasitic capacitor generates a zero in the transfer function at 20 kHz. This zero affects the overall transfer function of the three-stage oscillator in such a way that the phase at the transit frequency is larger than $-180°$ as shown

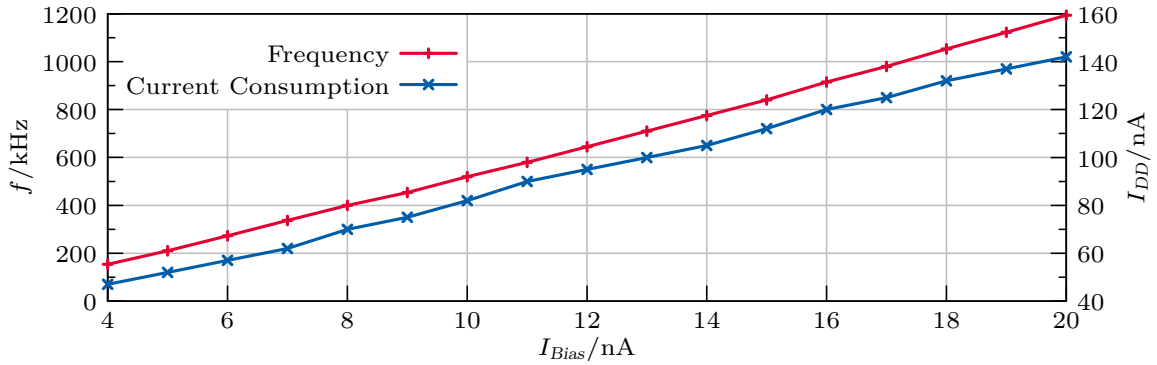


Figure 3.14: Frequency and current consumption of the three-stage current starved oscillator at different bias currents at 0.8 V

by the overall transfer function in Figure 3.13b. Oscillation is only possible if sufficient gain is available at a phase shift of −180°.

Measurement Results

A standalone test chip of the oscillator has been fabricated and measured. Figure 3.14 shows the dependency of the frequency and the current consumption on the bias current at a supply voltage of 0.8 V. The measurement includes the current consumption of the inverter in the level shifter used to shift the clock to input voltage level. The level shifter is not part of the oscillator itself but as the Slew Rate (SR) of the oscillator's output influences the current consumption of this inverter, it has to be considered in the overall consumption. The inverter consumes approximately 35 % at high frequencies and 45 % at low frequencies of the overall current consumption.

Biasing of the Oscillator

Considering only the losses of the oscillator and the linear regulator, (3.2.2a) is used to calculate the efficiency of the regulator. Also, the losses of the SC regulator itself are neglected. If the bias current of the oscillator is linearly dependent on the load current, as shown in (3.2.2b), the efficiency of the regulator becomes independent of the load current. Of course, the result in (3.2.2c) is only a first order approximation.

$$\eta = \frac{V_{Out} \cdot I_{Load} - V_{Out} \cdot I_{Osc}}{V_{Out_{SC}} \cdot I_{Load}} \tag{3.2.2a}$$

$$I_{Osc} = k \cdot I_{Load} \tag{3.2.2b}$$

$$\eta = \frac{V_{Out} \cdot (1-k)}{V_{Out_{SC}}} \tag{3.2.2c}$$

Measurements showed that this approximation fits well in a load current range from 1 µA to 5 µA. At higher load currents other losses become dominant.

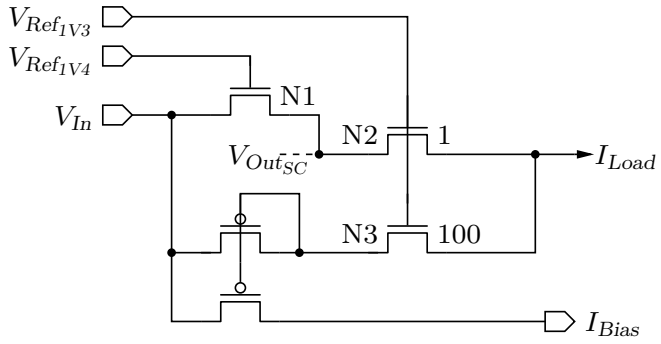


Figure 3.15: Circuit to derive the bias current for the oscillator

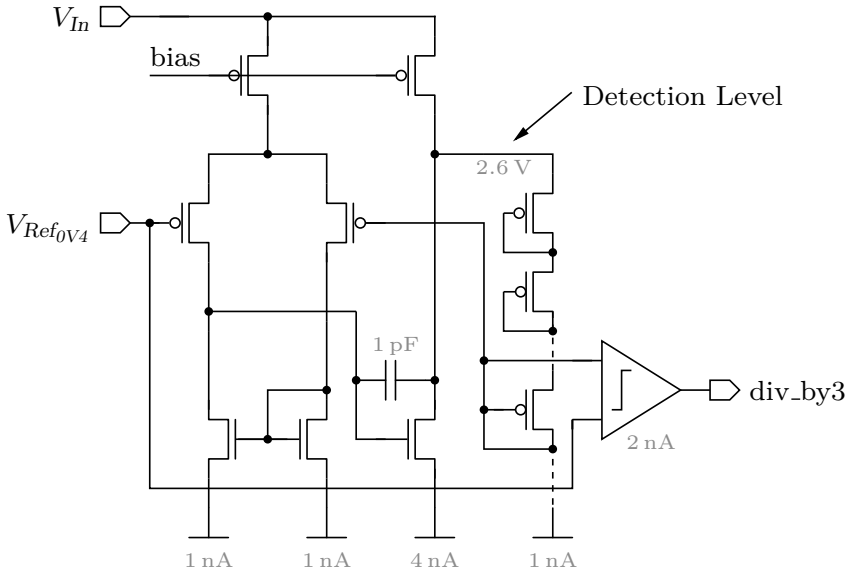


Figure 3.16: Concept of the level detector

To achieve the necessary frequency variation, the load current is measured and a small part of this result is used to bias the oscillator. The circuit used to measure the load current and to generate the bias current for the oscillator is shown in Figure 3.15. The transistors N1 and N2 are the same transistors as in Figure 3.1. For an appropriate operation of the current mirror (N2:N3), N2 must operate in saturation. By biasing N1 100 mV higher than N2, saturation is ensured.

If the load current undergoes a fast transient without adjusting the frequency fast enough, N1 will conduct. This leads to reduced efficiency, but the output voltage of the regulator is still constant. As soon as the oscillator frequency has been increased by the increased bias current, the efficiency rises again.

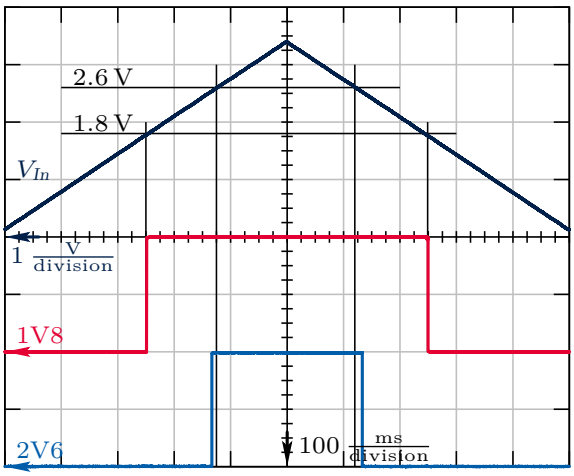


Figure 3.17: Measurement results of the level detectors

3.2.4 Level Detectors

The input voltage of the regulator is measured to select the appropriate operating mode of the SC voltage divider. State-of-the-art voltage level detectors like the architecture presented in [15] divide the input voltage and compare the result with a reference voltage. Dividing the input voltage is inefficient in terms of current and area consumption. Therefore a different approach, depicted in Figure 3.16, is chosen. Using a feedback configuration, the reference voltage is scaled to the needed detection level. As long as the supply voltage of the buffer in the feedback configuration, which is the voltage to be sensed, is higher than the detection level, the reference voltage equals the voltage in the feedback loop. If the voltage in the feedback loop drifts below the reference voltage, the detection limit is crossed and detected by a comparator.

To determine the operating modes of the regulator, two level detectors are implemented. One is used to enable or disable the SC regulator. The threshold level is 1.8 V. The second detector has a threshold level of 2.6 V and is used to set the division ratio to two or to three. The tail currents in the level detectors are only 1 nA. The current consumption of a detectors is below 10 nA. This low current consumption improves the overall efficiency of the regulator. Of course, this low current translates into a slow decision process of several hundred microseconds of the comparators. During this decision phase, the SC regulator may operate in the wrong operating mode. As the linear regulator in parallel will operate in this case, the output voltage of the regulator will not be influenced.

Figure 3.17 shows the measured transient behavior of both level detectors. The input voltage rises from 0.2 V to 3.3 V in 500 ms and afterwards it drops to 0.2 V again. The output of both level detectors is plotted. The detector for 1.8 V shows the expected result. The threshold level of the 2.6 V-detector is at approximately 2.55 V. The difference is caused by a systematic offset inside the comparator.

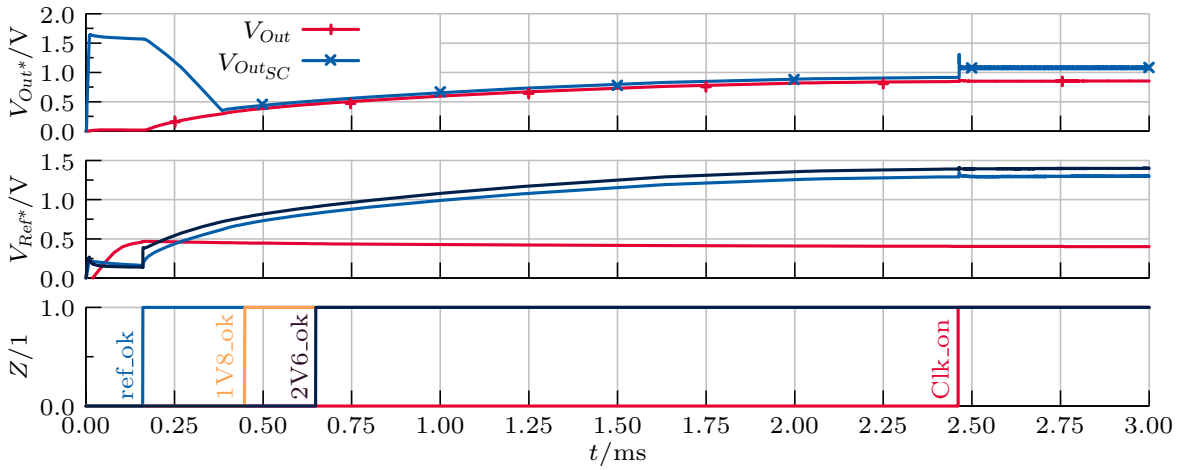


Figure 3.18: Startup of the hybrid regulator at an input voltage of 3.3 V

3.2.5 Transient Analysis

Various operating modes of the hybrid regulator are distinguished. Depending on the input voltage level the modes are changed, i.e. the appropriate division ratio of the SC divider is selected. For input voltages higher than 2.6 V, the divider divides by three. If the input voltage is between 1.8 V and 2.6 V, it is halved by the SC divider. For input voltages lower than 1.8 V, the divider is turned off. This section gives insight on the regulator's behavior on input voltage level changes and how startup is achieved.

Startup

When the regulator is enabled, that means if it is supplied by at least 1.35 V, it starts to operate. Figure 3.18 summarizes the most important signals during this phase. The upper chart shows the output voltage of the regulator and the output voltage of the SC divider. In the mid chart the reference voltages 400 mV, 1.3 V, and 1.4 V are depicted. At the bottom the various control signals are shown. From 0 µs to 10 µs the input voltage rises from 0 V to 3.3 V. The regulator starts to operate. The bias cell is the block which starts to operate first. The reference rises to 400 mV. When the startup of the reference cell is completed, the signal *ref_ok* changes to high state. The reference voltages 1.3 V and 1.4 V rise slowly. Concurrently, the output voltage of the regulator rises. As the oscillator is not yet enabled, only the linear regulator operates. Approximately 300 µs after the rising edge of *ref_ok*, *1V6_ok* changes to high state. 200 µs later *2V6_ok* also becomes high. The SC divider is configured to divide by three. As the oscillator is still not enabled, the SC divider is off. The reference scaling takes the most amount of time to start. After 2.4 ms the reference voltages 1.3 V and 1.4 V are available at their desired levels. The oscillator is not started until this point in time, as it makes no sense to operate the SC divider before these reference voltages are available. *Clk_on* changes to high. The operating SC divider causes $V_{Out_{SC}}$ to rise. Additionally, the noise generated by the switching can be seen on that voltage.

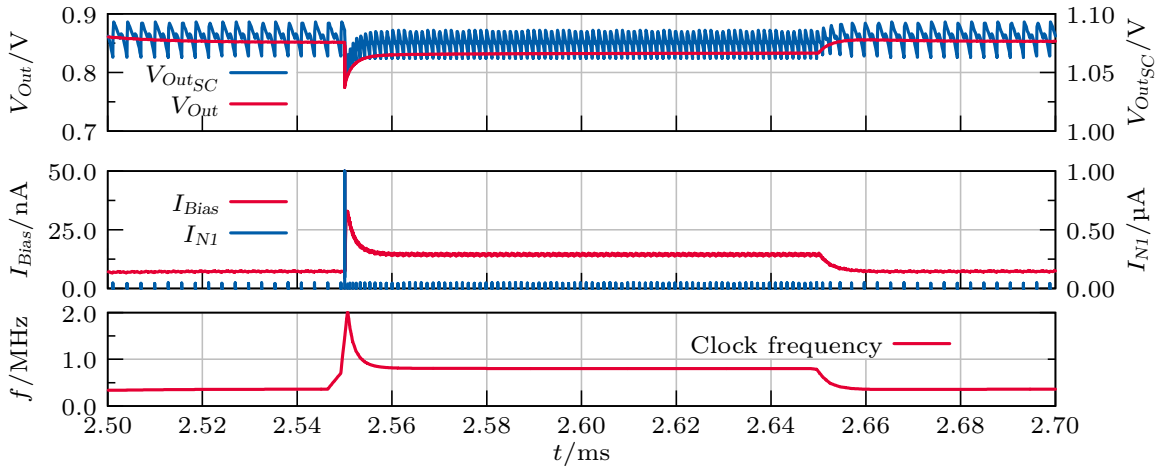


Figure 3.19: Behavior of the hybrid regulator on load variations

The oscillator is supplied by the output voltage of the regulator. Therefore, the SC divider can only operate if the regulator already provides a sufficiently high output voltage. During the phase where the oscillator is not operating because of a too low output voltage, the linear regulator in parallel provides the required output power. As soon as the oscillator starts to operate, the SC divider takes over and the linear regulator in parallel is turned off automatically. The startup follows the bootstrap concept.

Load variations

As discussed in the introduction of this thesis in Chapter 1.2, SC regulators have a slow dynamic response compared to linear regulators. The hybrid regulator, presented in this chapter, makes use of a linear regulator in parallel to the SC regulator to overcome this problem. This short section discusses the interaction of the linear and the SC regulator on load variations.

Figure 3.19 shows the necessary signals to describe the behavior of the regulator on load variations. The regulator is simulated with a nominal load current of 1 µA. At 2.55 ms the load current is doubled and, additionally, a load capacitance of 10 pF is added. Both the additional load current and this capacitor are removed again at 2.65 ms. The upper chart shows the output of the hybrid regulator and the output of the SC divider. The middle chart depicts the bias current of the oscillator and the current flowing through the linear regulator in parallel (N1). At the bottom the frequency of the oscillator clocking the SC divider is shown. To load the capacitor which is added at 2.55 ms, a very large current (theoretical infinity) is required. The SC divider cannot provide this current. Thus the output voltage of this block drops very fast. As a result of this voltage drop, the linear regulator in parallel conducts. This regulator provides the current pulse which is required to load the capacitor. The current is only limited by the channel resistance of N1 and N2 (refer to Figure 3.1). As soon as $V_{Out_{SC}}$ is high enough, N1 disables autonomously. Not only the load capacitance is increased, but also the load current

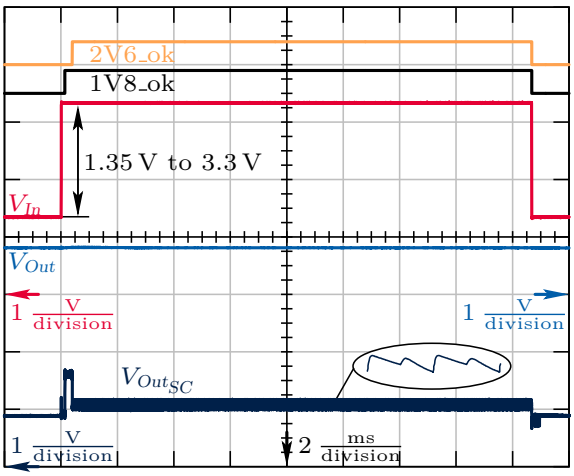


Figure 3.20: Measured behavior of the regulator during input voltage transitions

is doubled. The higher load current requires an increase of the oscillator frequency. Thus the bias current of the oscillator is increased from 7 nA to 14 nA, which results in a doubled clock frequency. The additional load is removed at 2.65 ms, causing the bias current to drop to 7 nA again.

Changing of the operating mode

If the input voltage of the regulator changes, the operating mode of the regulator has to be adapted, i.e. the division ratio of the SC divider has to be changed. Figure 3.20 shows the measured behavior of the regulator on input voltage transients. For the first 2 ms, the input voltage is 1.35 V. The SC divider is disabled. At 2 ms the input voltage rises to 3.3 V. The SC divider now has to divide by three. Since the outputs of the level detectors require some time to change, it takes some time to reconfigure the SC divider. 50 µs after the rising edge of the input voltage *1V8_ok* changes to high state, and the SC divider divides by two. $V_{Out_{SC}}$ is half of the input voltage during this phase. 150 µs later *2V6_ok* also becomes high and $V_{Out_{SC}}$ is now a third of the input voltage. Even if the SC divider operates in the wrong mode for 200 µs, the output voltage of the regulator is not affected. The measurement proves that the output voltage of the regulator is always constant, independently of the input voltage level.

3.2.6 Measurement Results and Comparison

This chapter discusses the measurement results of the hybrid regulator and compares them to recent publications. The results of the individual blocks are presented in the according sections. Here only the overall performance is analyzed.

A key parameter for this kind of regulator is the efficiency on different input voltages and load currents. To optimize the efficiency, some modifications on the fabricated IC took place. First,

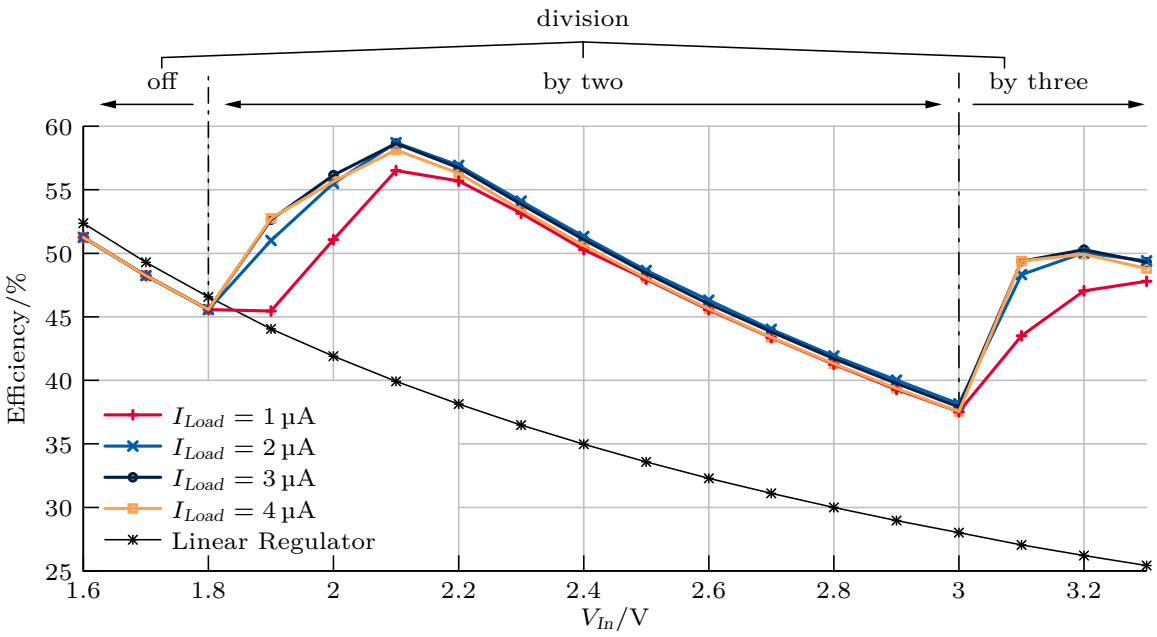


Figure 3.21: Measured efficiency of the regulator using different load currents in comparison to a linear regulator at $V_{Out} = 0.8\,V$

the non-overlapping clock generation is disabled by the Focused Ion Beam (FIB) technique. Second, the threshold level of the second level detector is shifted to 3 V by using a slightly higher reference voltage for this block.

Figure 3.21 shows the measured efficiency for input voltages from 1.6 V to 3.3 V using load currents in the range of 1 µA to 4 µA. The measurement of the efficiency includes all discussed blocks. At 1.8 V and 3.0 V the operating mode of the voltage divider is changed. The dashed line represents the simulated efficiency of a conventional linear regulator. The difference in the efficiency below 1.8 V is caused by the current consumption of the level detectors. The most significant facts of the implemented regulator are summarized in Table 3.2. The performance parameters are compared to recently published representative similar works: [92] by M. Wieckowski and [67] by Y. K. Ramadass.

Post-layout simulations showed efficiency values up to 15 % higher than the measurement results when the SC regulator divides by three. The difference is caused by a parasitic capacitor. The flying capacitor is formed by a PMOS transistor. The n-well of this transistor and the p-substrate form a diode having a junction capacitor. This capacitor increases the output voltage ripple of the SC divider significantly and thus the efficiency decreases. As this parasitic diode is not modeled in the design environment, simulation results do not follow measurement results. When the SC regulator divides by two, this parasitic has no influence, as it is in parallel to the input voltage. During the division by three, the parasitic capacitor is periodically charged and discharged. This decreases the efficiency significantly. To increase the efficiency of the regulator, especially when it divides by three, other capacitor types have to be used.

	this work	[92] by M. Wieckowski	[67] by Y. K. Ramadass
CMOS Technology	0.13 µm	0.13 µm	0.18 µm
Active area	0.051 mm^2	0.262 mm^2	0.57 mm^2
Flying capacitors	3×25 pF MOS	4×200 pF MIM	2.4 nF MOS
Input voltage range¶	1.35 V to 3.3 V	2.5 V to 3.6 V	> 1.8 V
Output voltage	0.8 V	444 mV	0.3 V to 1.1 V
Nominal load	1 µA	285 nA	5 µW to 1 mW
η at nominal load¶	37 % to 56 %	56 % (Max.)	> 70 %§
PSRR*@1 kHz	−44 dB	not reported	not reported
¶measured	*post-layout simulated		§w/o oscillator

Table 3.2: Performance summary of the hybrid regulator compared to recent publications

3.3 Conclusion

This chapter presented an innovative SC regulator for ultra-low power wireless sensor nodes. The architecture supports a wide range of power supplies. Using the SC network allows a highly efficient DC/DC conversion. As SC regulators usually do not provide good line and load regulation capabilities, the SC circuit is surrounded by a linear regulator which operates on fast line or load transients. The implementation is simple and robust. To support different load conditions, the load current is measured and the frequency of the SC regulator is adapted accordingly. The efficiency of this regulator is up to 20 % higher than the one a conventional linear regulator provides. As the linear regulator enables autonomously, the dynamic performance parameters of the regulator are not affected by the SC regulator.

The nominal load current for the regulator is only 1 µA. So as not to decrease the efficiency of the regulator, the current consumption of the building blocks must be very low. By introducing novel design concepts, the current consumption of the regulator is reduced to below 150 nA. For the bias cell, different circuits published in literature are combined. A new concept for input voltage level detection has been implemented. This architecture has a lower current consumption than state-of-the-art detectors.

For this implementation the gate voltage of the pass devices is constant. The combination of an SC regulator with a linear regulator, as presented here, can also be used with a regulated pass device. The same efficiency improvement is expected in that case.

Chapter 4

Voltage Regulators for Low Input Voltages

> A creative man is motivated by the desire to achieve, not by the desire to beat others.
>
> *(Ayn Rand)*

4.1 Introduction

Chapter 2 and Chapter 3 presented voltage regulators and a Power Management Unit (PMU) for Wireless Sensor Nodes (WSNs). The presented implementations support a wide range of power sources. The voltage provided by the power source is lowered by linear regulators to enable supplying the WSN. So far the voltage level of the power source has had to be higher than the voltage level required to supply the WSN. This chapter presents solutions to enable power sources which also generate voltage levels below the required supply voltage. The presented DC/DC converters fall into the category of buck-boost converters as the input voltage can be below or above the input voltage level.

This chapter presents two different architectures. For input voltages higher than 1.2 V, they operate similarly. If the input voltage is below 1.2 V, the architectures behave differently. The DC/DC converter presented in Chapter 4.2 provides a continuous output while the converter discussed in Chapter 4.3 operates periodically.

4.2 Regulator for Permanent Supply Requirements

This chapter presents a voltage regulator with an input voltage range of 0.6 V to 3.3 V at a constant output voltage of 1.2 V. The linear regulator presented in Chapter 2.3.2 has proved to be successful. It operates at an input voltage range from 1.2 V to 3.3 V. By using an additional Switched Capacitor (SC) regulator, the input voltage range is increased to 0.6 V to 3.3 V. The SC regulator ensures that the input voltage of the linear regulator is at least 1.2 V. For efficiency reasons, the SC regulator is only enabled at input voltage levels below 1.2 V.

Figure 4.1 shows the block diagram of this regulator. It is composed of two parts: (1) the input voltage adjustment, and (2) the linear regulator. The linear regulator is presented in

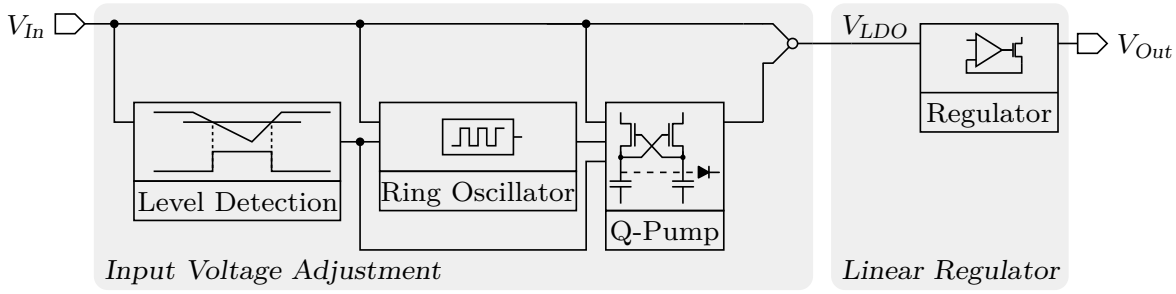


Figure 4.1: Architecture of the regulator for permanent supply requirements

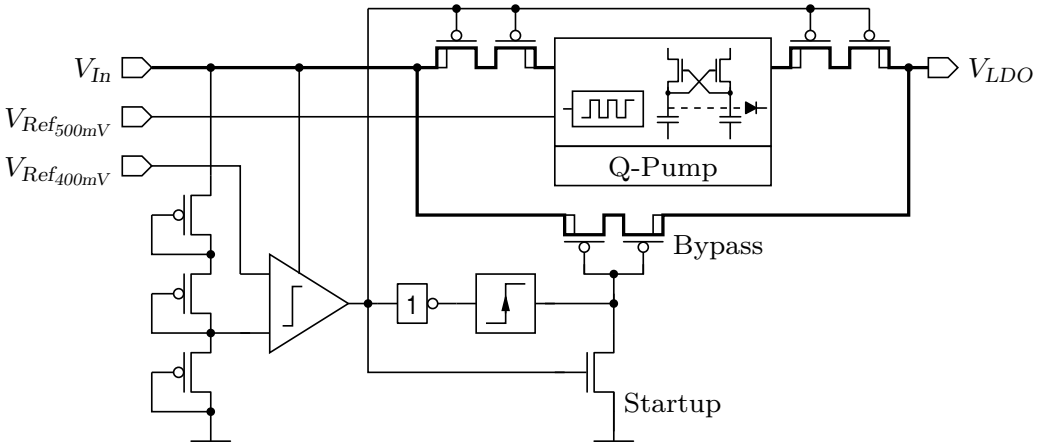


Figure 4.2: Architecture of the input voltage adjustment

Chapter 2.3.2. This chapter only discusses the input voltage adjustment. The different building blocks of this circuit are presented. A short summary including measurement results finalizes this chapter.

4.2.1 Input Voltage Adjustment

Figure 4.2 shows the simplified circuit of the input voltage adjustment. The core is formed by a charge pump. If the input voltage (V_{In}) is smaller than 1.2 V, the PMOS power switches in series to the charge pump are closed. The charge pump starts to operate and it generates the required input voltage for the linear regulator (V_{LDO}).

Input voltage sensor

To sense the input voltage, a voltage sensor, as proposed in [15], is implemented. The input voltage is divided by a voltage divider composed of PMOS diodes. As discussed earlier, the area consumption of MOS diodes is smaller in comparison to resistors. In the worst case, the voltage drop over the divider is 3.3 V. The transistors in the divider have to be sized

sufficiently large to limit the current consumption. Here the current consumption at 3.3 V is 490 nA.

If the input voltage is higher than 1.2 V, the bypass switch of the charge pump is enabled and the supply of the charge pump is disabled. To prevent bulk currents in the switches, two PMOS transistors are connected in series. The control voltage of the bypass switch has to be at V_{LDO} level. This requires a voltage level shifter, which shifts the output of the comparator to V_{LDO}. At startup the voltage level of V_{LDO} is undefined. That means that the output of the level shifter is also undefined. To ensure startup, the output of the level shifter is pulled down to ground as long as the bypass is conductive.

Charge Pump and Oscillator

M. Liu states in his book that a voltage doubler as proposed in [22] is best suited for low input voltages and high current demands [45]. So this circuit, which is also shown in Figure 2.15 on page 32, is used. The design considerations in Table 2.2 on the same page are still valid. The maximum output voltage of the charge pump is the doubled input voltage. So the input voltage of the regulator has to be at least 0.6 V. The charge pump is designed to deliver a maximum load current of 5 µA. The flying capacitors have a capacitance of 10 pF each.

The charge pump requires a clock frequency of 2.5 MHz to be able to deliver the required load current. The higher the input voltage is, the lower the frequency can be. The requirement to decrease the output frequency if the input voltage increases is achieved by using a current starved ring oscillator. Thus a three-stage ring oscillator, as shown in Figure 2.18, is used. The oscillator is supplied by the input voltage of the regulator. So the frequency will drop if the input voltage rises.

The output of the charge pump is monitored by a voltage level detector. Whenever the output exceeds 1.5 V, the charge pump is disabled. If the voltage drops below this threshold, the charge pump is enabled again.

4.2.2 Measurement Results

This section discusses the measurement results of the regulator. The current consumption at different input voltages as well as the transient behavior of the regulator is presented.

Figure 4.3 shows the measured current consumption of the regulator at a load current of 5 µA. Below an input voltage of 0.7 V, the output of the regulator does not achieve the required level of 1.2 V. In the input voltage from 0.7 V to 0.9 V, the current consumption is highest. Here, the charge pump is enabled permanently. The overall efficiency of the regulator is in this case approximately 50 %. For input voltages higher than 0.9 V, the charge pump for the input voltage adjustment is operating periodically. Thus, the current demand of the regulator drops. At input voltages higher than 1.2 V, the input voltage sensor disables the voltage adjustment. Thus, the current consumption drops significantly. If the load current is subtracted,

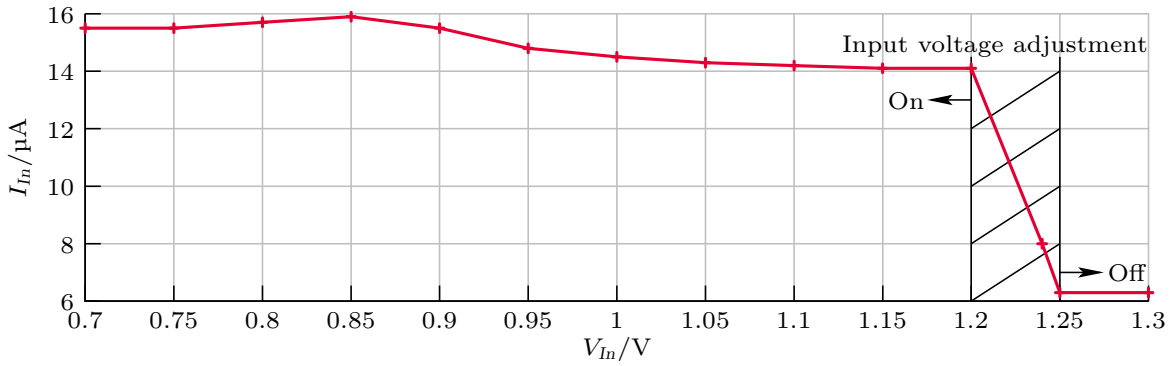
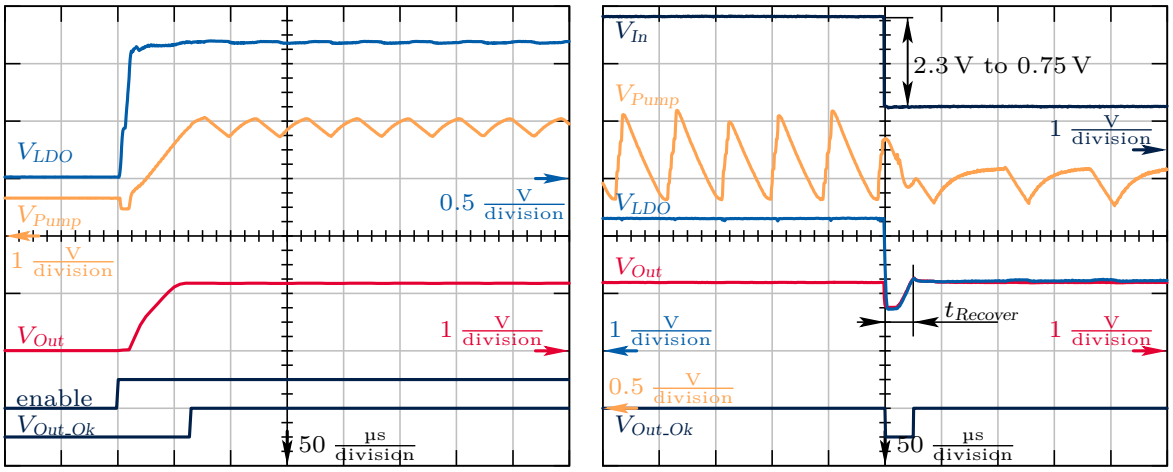


Figure 4.3: Measured current consumption at I_{Load}=5 µA



(a) Startup at $V_{In} = 0.7$ V

(b) Input voltage drop

Figure 4.4: Measurement results of the regulator

the input current is 1.3 µA. This is the current consumption of the linear regulator (compare to Figure 2.25).

Figure 4.4 summarizes the transient behavior of the regulator. The behavior at startup as well as during input voltage drops is shown. The following paragraphs describe the different operating modes.

If the regulator is enabled at an input voltage lower than 1.2 V, the charge pump has to generate an input voltage for the linear regulator (V_{LDO}) of at least 1.2 V. The transient signals in this case are shown in Figure 4.4a. At 100 µs the regulator is enabled. The input voltage adjustment starts immediately. V_{LDO} rises fast to 1.3 V. As the linear regulator is an NMOS type, an additional charge pump is required to generate the supply voltage for the error amplifier. Chapter 2.3.2 elaborates this in detail. The output of this charge pump is V_{Pump}. As soon as V_{Pump} is high enough, the output voltage of the regulator (V_{Out}) gets 1.2 V. 60 µs after the enable pulse, the output voltage detector sets V_{Out_Ok} high. Even if the input voltage is only

0.7 V, the output of the regulator is still 1.2 V.

If the input voltage of the regulator drops from high levels to levels below 1.2 V, the input voltage adjustment has to start operating. As the charge pump requires some time to be fully operational, the output voltage of the regulator will drop during this phase. Figure 4.4b summarizes the most important signals during an input voltage drop from 2.3 V to 0.75 V. In the time interval from 0 µs to 50 µs, the input voltage adjustment is disabled, as it is not required. The input voltage of the regulator (V_{In}) equals the input voltage of the linear regulator (V_{LDO}). At 50 µs the input voltage drops to 0.75 V. V_{LDO} also drops, causing V_{Out} to drop, and consequently V_{Out_Ok} changes to zero. After a time delay ($t_{Recover}$), which is in this case approximately 25 µs, V_{LDO} rises. This indicates that the input voltage adjustment is now operating appropriately. V_{Out} is able to rise to 1.2 V again. For the regulator described in Chapter 2.3.2, the output voltage drop during input voltage transients was caused by the output voltage drop of the charge pump required for the NMOS regulator. Figure 4.4b shows that in this case V_{Pump} is always sufficiently high.

4.2.3 Conclusion

Chapter 4.2 presented a voltage regulator capable of an input voltage range of 0.6 V to 3.3 V. The output voltage is 1.2 V. To achieve an output voltage which is higher than the input voltage, the regulator presented in Chapter 2.3.2 is enhanced by a so-called input voltage adjustment. This block comprises a charge pump and a level detector. Whenever the input voltage of the regulator is lower than 1.2 V, the charge pump is enabled. The maximum load current of the regulator is 5 µA.

The lower the input voltage gets, the higher the input current is. If the input voltage is doubled, the current consumption is twice as high, to satisfy the law of conservation of energy. At a load current of 5 µA, the input current is 15 µA. The difference of 5 µA is caused by the current consumption of the regulator itself and by losses inside the charge pump.

4.3 Regulator for Slot-Based Operation

Chapter 4.2 presented a voltage regulator which allows input voltages lower than the output voltage. A charge pump amplifies the input voltage. When the charge pump operates, the current demand of the regulator rises significantly. The lower the input voltage is, the higher the current consumption becomes. For some power supplies, like batteries, this is an unwanted behavior. Implementations like [50] solve this problem by dynamic load control. This technique matches the input impedance of the charge pump to the power supply. This chapter presents a different solution which allows a rather constant current consumption of the regulator independently of the value of the input voltage. The concept is similar to the harvesting concept presented in [72] and the concept of a slot-based operation shown in [37]. Both papers propose a periodic operation of the power management. For input voltages higher than 1.2 V, the regulator behaves similarly to the regulator in Chapter 4.2. When the input voltage is lower, it operates differently. The regulator enters a periodic operation. First an (on-chip) capacitor is

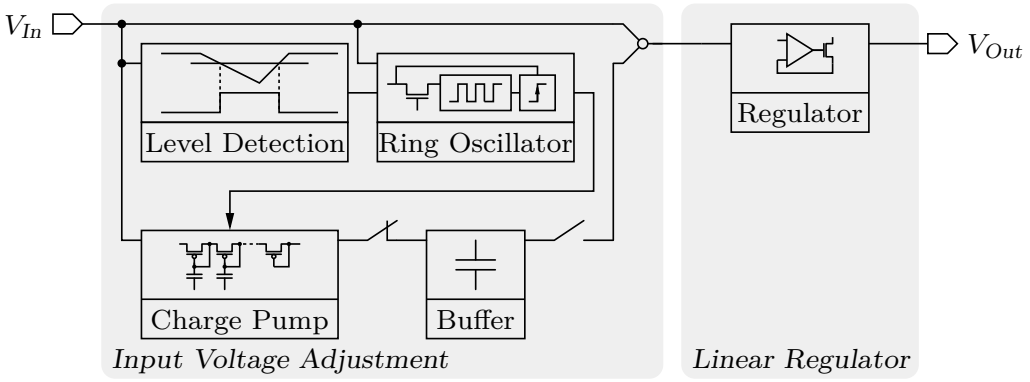


Figure 4.5: Architecture of the regulator for slot-based operation

charged by a charge pump and the load is disconnected. As soon as enough energy is stored in the capacitor, the charge pump is disabled and the load is enabled.

Figure 4.5 shows the simplified architecture of the regulator. An input voltage level detector monitors the input voltage. If the voltage is higher than 1.2 V, it is routed directly to the linear regulator. Otherwise, the charge pump is enabled and the buffer capacitor is charged.

The concept seems rather simple, but implementing this kind of regulator is not trivial. A sophisticated control unit is needed to manage the different supplies required inside the regulator. Figure 4.6 gives a more detailed insight into the architecture. The regulator is formed by three different blocks:

1. The *Clock Generation* provides the necessary clock signals. Besides the two charge pumps operating inside the regulator, various other blocks also require clock signals. The different level detectors controlling the operating modes reuse concepts which are presented in this thesis. They are enhanced by clocked comparators. The clock required for these comparators is generated by this block. The control unit of the regulator also requires a clock signal which is generated by this block.

2. When the input voltage is lower than 1.2 V, the regulator enters the periodic or pumping mode. In this case the *Input Voltage Adjustment* generates the input voltage for the linear regulator. Otherwise, the input voltage of the regulator is routed directly to the linear regulator. The *Control Unit* is also located in this block.

3. The *Linear Regulator* generates a stable output voltage of 1.2 V. The pass device is formed by an NMOS transistor. Thus a charge pump for low input voltages is required. The signal V_{Out_Ok} states if the output of the regulator is in its desired range.

The next sections discuss the different blocks of the regulator in detail. At the end of this chapter transient analysis and measurement results clarify the functionality of this voltage regulator. A short conclusion summarizes and concludes this chapter.

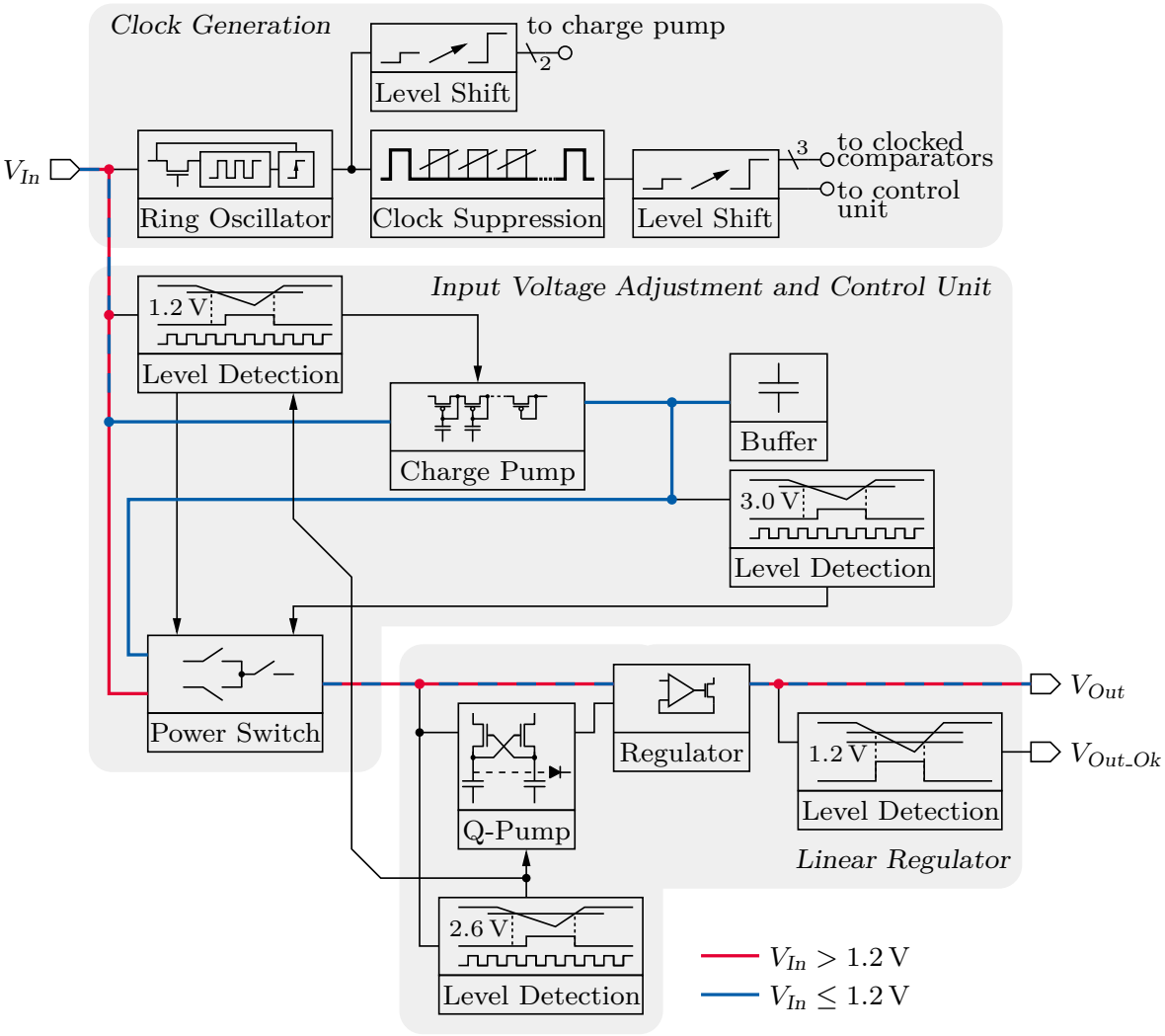


Figure 4.6: Detailed architecture of the regulator for slot-based operation

4.3.1 Clock Generation

The purpose of the clock generation is to provide the required clock signal. For power saving reasons, only one oscillator is used. All clock signals are derived from this oscillator.

The oscillator is a three-stage current starved oscillator with supply voltage limitation. Figure 2.18 on page 37 shows the circuit. So far this architecture has been used to drive charge pumps. Here, this oscillator also clocks digital circuits.

Whereas glitches do not pose a problem for charge pumps, they have to be prevented in digital circuits. As the used architecture tends to generate glitches, they need to be prevented. How this is done is presented in the following.

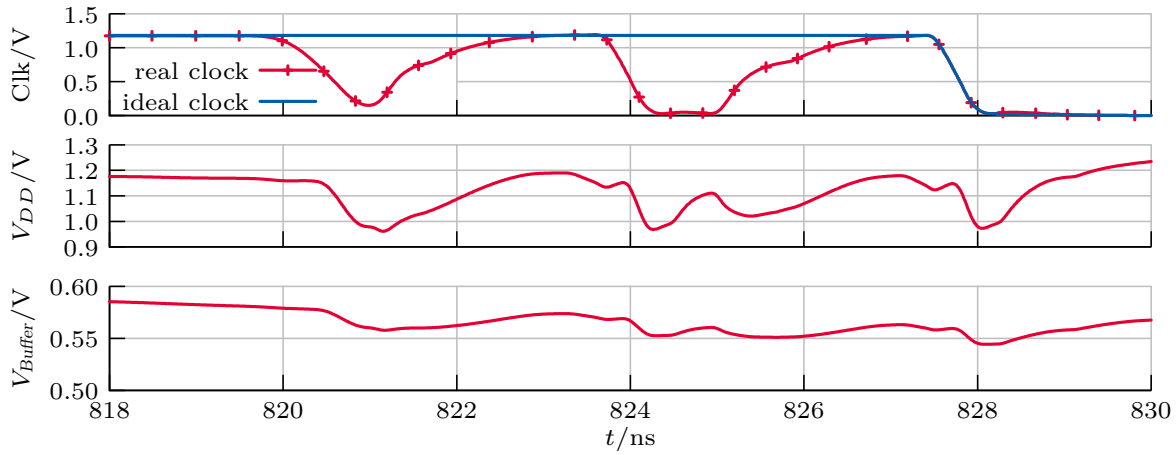


Figure 4.7: Glitches generated by the oscillator

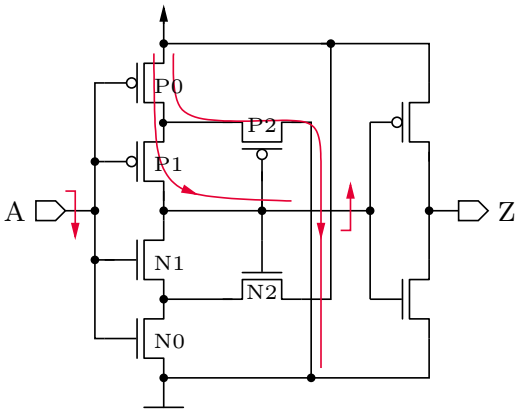
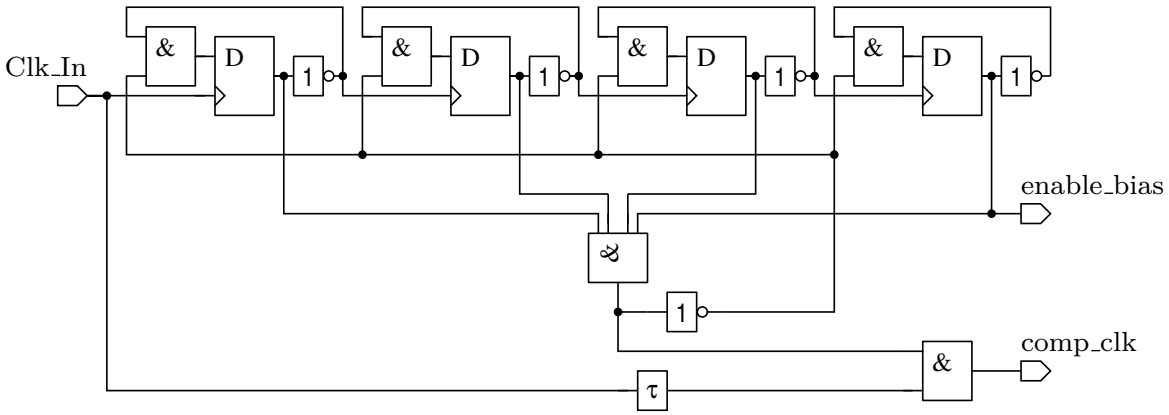


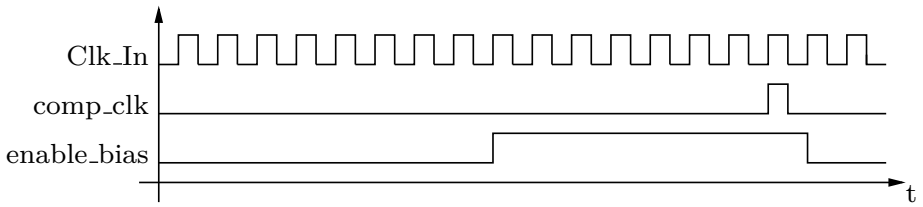
Figure 4.8: Schmitt trigger

In the phase when the output of the oscillator alters from high to low or vice versa, the current consumption is at a maximum. As a result of the output resistance of the power supply of the oscillator, the supply voltage drops during this phase. Due to the lowered supply voltage, the threshold level of the output buffer is shifted. This translates into a toggling output. Figure 4.7 shows this behavior. The upper chart compares the output of the oscillator with the ideal clock signal. In middle chart the supply voltage of the oscillator is shown. The bottom chart shows the input of the output buffer. Between 818 ns and 830 ns the input of the output buffer (V_{Buffer}) is near the threshold of the buffer. Thus the current demand of this buffer increases significantly, causing V_{DD} to drop which in turn shifts the threshold of the buffer. As a consequence, the output of the buffer toggles.

One solution to eliminate the glitches is to implement a Schmitt trigger between the ring oscillator's output and the first buffer. Figure 4.8 shows the CMOS implementation of a Schmitt trigger. The hysteresis is generated by the cross-coupling of the transistors N2 and P2. If the input is dropping, P2 reduces the current through P1, which is required for an output change.



(a) Circuit



(b) Clock signals

Figure 4.9: Circuit of the clock suppression and the generated clock signals

As soon as the input voltage is low enough that the current flowing through P1 is larger than the current flowing through P2, the output of the Schmitt trigger changes its state. As the input is inverted by the Schmitt trigger, an additional inverter is required.

Duty Cycle Adjustment

The clocked comparators used for the level detectors require a clock signal. They make use of a latch which stores the output of a comparator on a rising clock edge. The frequency of the clock has to be much lower than the frequency used for the charge pump. Also, a large duty cycle is required. Figure 4.9 shows the circuit which modifies the clock frequency as required. It suppresses 15 clock pulses, and every 16th pulse is let through. The bias current of the level detectors is disabled as long as the clock is zero, as they do not operate anyway. As the comparators require a startup time, the biasing is enabled before the clock of the latch changes to high. The signal *enable_bias* enables or disables the biasing of the comparators.

The supply voltage of the oscillator is lower than the input voltage of the regulator. So the different clock signals are shifted to the required voltage levels by voltage level shifters.

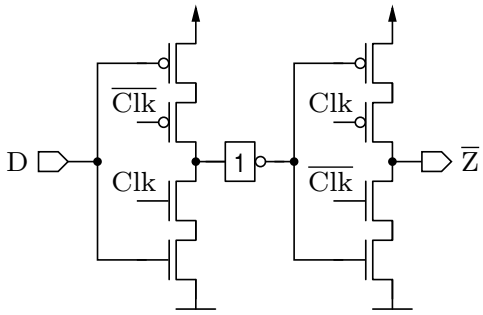


Figure 4.10: Gated D latch

4.3.2 Input Voltage Adjustment and Control Unit

This section presents the various blocks which are required to generate the input voltage of the linear regulator. An input voltage sensor monitors the input voltage of the regulator and enables or disables the pumping operation. In pumping operation, a charge pump transfers energy from the input to the buffer capacitor.

Controlling the different blocks is sophisticated. This chapter also gives insight into the control unit. For better understanding, the description of the control is simplified. Only the basic operational principle is presented.

Input Voltage Sensor

The input voltage sensor monitors the input voltage of the regulator. Whenever it is below 1.2 V, it enables the pumping mode of the regulator. The voltage sensor divides the input voltage and compares this result to a reference voltage. At high input voltages the voltage divider consumes a lot of current. Thus it is disabled on high input voltages. Whenever the output of the voltage detector for 2.6 V* is high, this divider is disabled. During the phase when the buffer capacitor supplies the regulator, it is also disabled.

The output of the comparator has a slow Slew Rate (SR), as the bias current is only 10 nA. During transitions of this output the digital gate driven by this signal draws a lot of current. This problem is solved by a gated D latch which is connected to the output of the comparator. Figure 4.10 shows the circuit. As long as the *Clk* signal is zero, the gate draws no current regardless the voltage level at *D*. Whenever *Clk* changes to high state, the state of *D* is stored. The clock signal *comp_clk* in Figure 4.9 is used as *Clk* signal. As this signal has a large duty cycle, the latch is enabled only for a short time interval. During this time interval, the output of the comparator is stored in the latch. In the remaining time interval, the output of the comparator can change its state without affecting the output of the latch. The worst case is that the output of the comparator changes its state, while *Clk* is high. This will cause a high

* This detector is required for the charge pump supplying the error amplifier of the regulator (compare with Chapter 2.3.2).

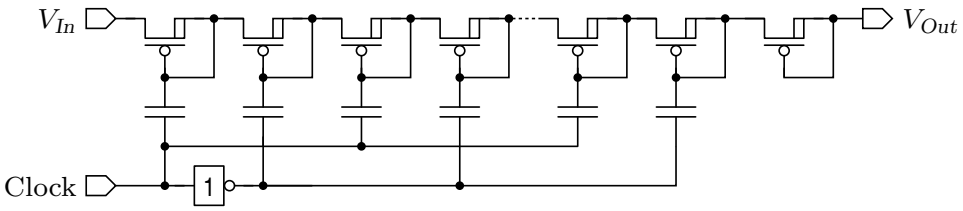


Figure 4.11: Dickson charge pump in CMOS technology

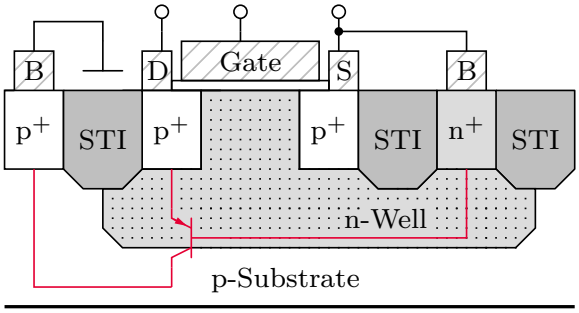


Figure 4.12: Cross section of a PMOS transistor showing the parasitic pnp transistor

current pulse. This current pulse will appear for a short time only anyway, because of the short *Clk* pulse.

Dickson Charge Pump

During pumping operation of the regulator, a ten-stage Dickson charge pump amplifies the input voltage. The charge transferred by this charge pump is stored in the buffer capacitor. The Dickson charge pump is extensively discussed in literature, like [45]. Figure 4.11 shows an implementation method in CMOS technology.

In CMOS technology the diodes can either be formed by NMOS or PMOS transistors. In literature NMOS transistors are common. In a single well p-substrate process, the drawback of using NMOS transistors is that the body effect increases the threshold voltage of the diodes and thus limits the output voltage of the charge pump. To overcome this problem, PMOS diodes are used here. The bulk of the PMOS transistor is connected to the corresponding output of each stage. It is important to know that during the pumping operation the bulk-source diode (drain and source alternate) may get conductive for a short time. Figure 4.12 shows that the bulk-source diode is part of the parasitic pnp transistor. The influence of the pnp transistor is well known from the latchup effect [61] or power loss effects in switches [66]. Due to the low current in this design, the voltage drop over the channel is low. This means that the forward voltage of the bulk diode is also very small. So latchup is not an issue. The designer has to be aware that the bulk current is amplified by β of the pnp transistor and drawn from the drain. This generates losses. The parasitic bipolar transistor is usually not considered by the MOS model.

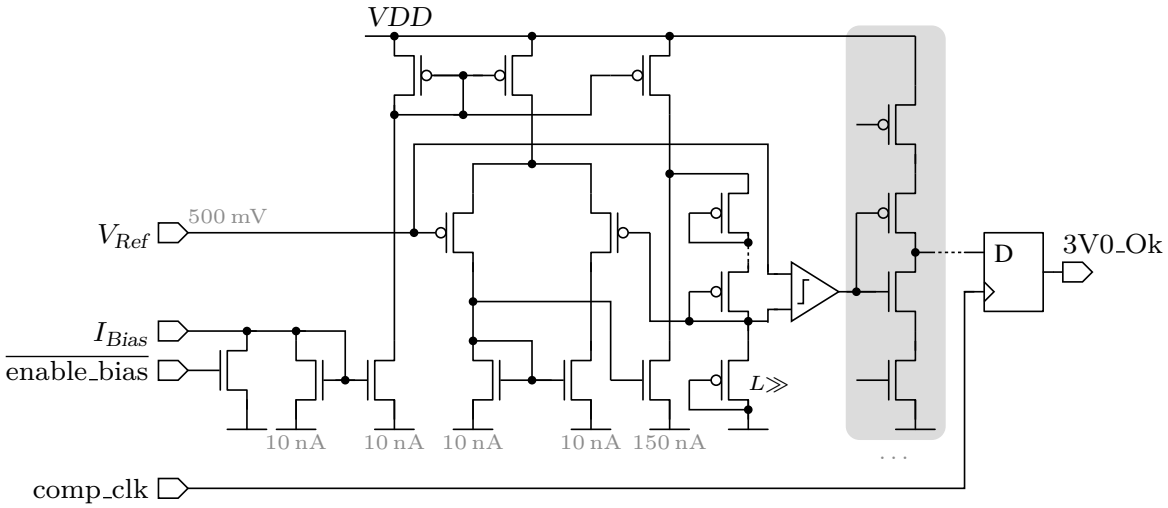


Figure 4.13: 3.0V detector

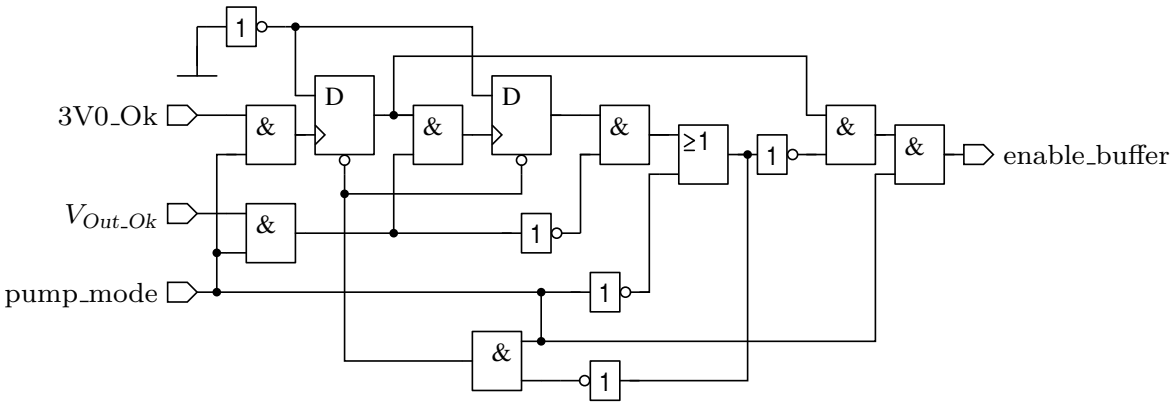
Charge Pump Monitor

A voltage sensor monitors the voltage level at the buffer capacitor. As the detection level is considered high, the concept discussed in Chapter 3.2.4 and shown in Figure 3.16 on page 75 is used. Again it is enhanced by a gated D latch. To further decrease the power consumption, the biasing is only enabled periodically by the signal *enable_bias* generated by the clock generation (refer to Figure 4.9). Figure 4.13 shows the simplified schematic. Whenever $\overline{enable\_bias}$ is in high state, the bias current is redirected to ground and the current consumption of the detector is reduced. The output of the comparator is routed to a multi-stage current starved inverter chain. The bias current of each stage is increased to get a higher SR at the output. The output of the final inverter is connected to the gated D latch. The latch stores this value whenever the *comp_clk* is high.

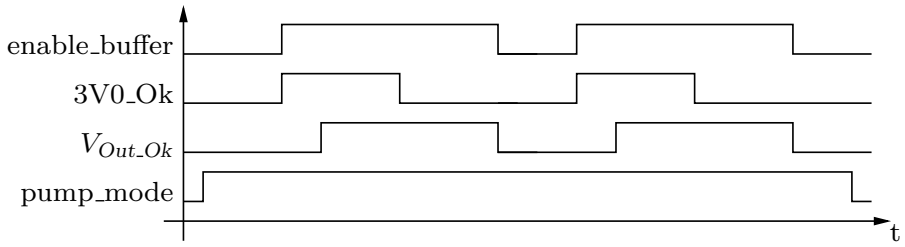
Control Unit

The control unit controls the power flow inside the regulator. Thus it controls the power switches during pumping operation and the Dickson charge pump. Basically four different signals are processed: (1) *pump_mode* is in high state if the regulator is in pumping operation, (2) V_{Out_Ok} is in high state if the output voltage of the regulator is high enough, (3) *3V0_Ok* switches to high state if the buffer capacitor is charged to 3 V or higher, and (4) *enable_buffer* is used to enable to buffer capacitor in pumping operation.

In pumping operation, the regulator enters a periodic operation. As the input voltage is lower than 1.2 V, the Dickson charge pump is enabled. It transfers charge into the buffer capacitor. As soon as the 3.0V detector detects 3 V across the buffer capacitor, the regulator is enabled. The output voltage becomes 1.2 V and V_{Out_Ok} changes to high state. During the operating phase of the regulator, the Dickson charge pump is disabled. The voltage level at the buffer capacitor



(a) Control unit



(b) Signals

Figure 4.14: Control unit and signals

drops. As soon as it is too low to generate an output voltage of 1.2 V, the signal V_{Out_Ok} changes to zero. Hence, the regulator is disabled and the Dickson charge pump is enabled. As soon as the buffer capacitor is charged to 3 V, the regulator is enabled again. Figure 4.14a shows the control unit generating the signal *enable_buffer*. If *enable_buffer* is high, the linear regulator is enabled and the Dickson charge pump is disabled. Figure 4.14b summarizes the most important control signals processed by the control unit.

Power Switch

If the regulator is in regular operation, the linear regulator is supplied by the input voltage of the regulator. Otherwise, the buffer capacitor supplies the linear regulator. Figure 4.15 shows the switch which selects either the input voltage or the buffer to supply the linear regulator. The control signals are at V_{In} level. To successfully turn the PMOS transistor off, level shifters are required. The switch also generates the signal *LDO_enabled*. This signal states whether the linear regulator is supplied, and is mainly used to enable and disable the various level shifters required to control the linear regulator.

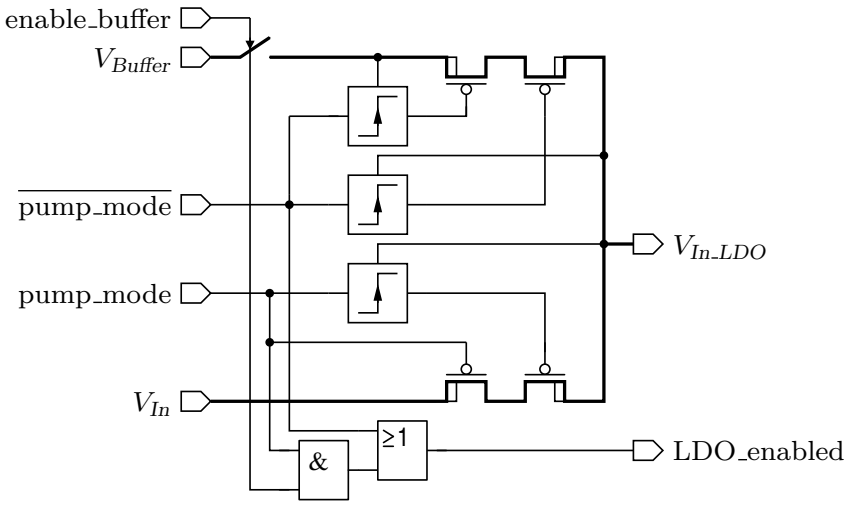


Figure 4.15: Power switch

4.3.3 Linear Regulator

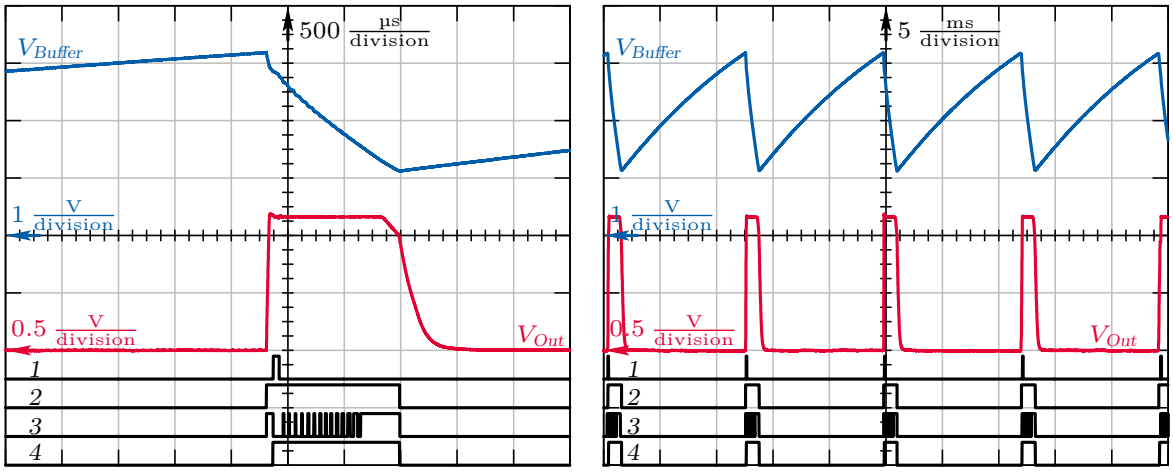
The linear regulator has to generate the required output voltage of 1.2 V. The linear regulator presented in Chapter 2.3.2 satisfies the needs well. Thus this architecture is also employed here. To decrease the current consumption some improvements were necessary:

- As already proposed in Chapter 2.3.2, the voltage divider for the charge pump is disabled whenever the bypass is active. Also, the input voltage sensor, which enables or disables the bypass, is enhanced by a clocked D latch. The input of the latch is connected to the parasitic sensitive node (refer to Figure 2.17 on page 34).

- As discussed in Chapter 2.3.2, the charge pump voltage sensor generates a weak high pulse during startup. This pulse causes a current peak. So far this current has been reduced by increasing the length of the following digital gate. Here, the pulse is isolated by an AND gate. The second input of the AND gate is connected to the output voltage sensor. This signal is at ground level during startup and can be used to suppress the pulse generated by the charge pump voltage sensor. Using the AND gate reduces the current consumption at startup, but does not reduce the current pulses during output transitions of the level detector. Here, a current starved logic or at least gates with larger lengths of the transistors are required.

4.3.4 Measurement Results

This section discusses the measurement results of the regulator. The current consumption on different input voltages as well as the transient behavior of the regulator is presented.



(a) One operation cycle

(b) Periodic output of the regulator

1 . . . *2V6_Ok*
2 . . . *enable_buffer*
3 . . . *enable_clock*
4 . . . V_{Out_Ok}

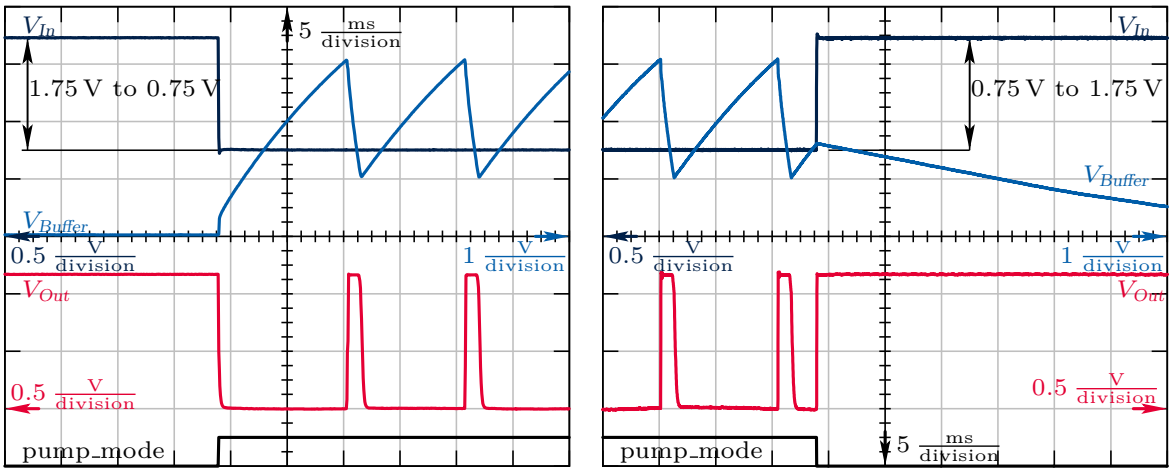
Figure 4.16: Measured behavior of the regulator in pumping operation

Figure 4.16 summarizes the regulator's behavior when it operates in pumping operation. Figure 4.16a shows an operation cycle in detail and Figure 4.16b illustrates the periodic output behavior of the regulator.

Figure 4.16a shows one operation cycle. The buffer capacitor is charged to approximately 3.3 V. At this level the regulator is enabled by *enable_buffer* changing to high state. The output of the regulator (V_{Out}) rises to 1.2 V and V_{Out_Ok} changes to high state. As the input voltage of the linear regulator, which is in this case V_{Buffer}, is higher than 2.6 V, *2V6_ok* is set high. The signal *enable_clock* indicates an operation of the charge pump for the error amplifier inside the linear regulator (compare to Chapter 2.3.2). The lower V_{Buffer} gets, the longer the charge pump has to operate. As soon as the voltage level at the buffer capacitor is too low to get 1.2 V at the output of the regulator, V_{Out_Ok} changes to zero and the linear regulator is disabled.

As shown in Figure 4.16b, the regulator generates a periodic output voltage when the input voltage is lower than 1.2 V. The Dickson charge pump periodically charges the buffer capacitor. During the charging process, the voltage across the buffer capacitor (V_{Buffer}) rises. As soon as this voltage level is higher than 3.0 V, the regulator is enabled by the signal *enable_buffer* changing to high. At the same time the Dickson charge pump is disabled. The output of the regulator rises to 1.2 V. As a result of the load current and the current demand of the regulator itself, V_{Buffer} drops. If this voltage is below 1.2 V, the output voltage of the regulator also starts to drop. Thus the signal V_{Out_Ok} changes to zero. The linear regulator is disabled and the Dickson charge pump is enabled. The buffer capacitor is charged again.

The regulator's behavior on input voltage transitions from levels below 1.2 V and to levels above



(a) Regular operation to pumping operation

(b) Pumping operation to regular operation

Figure 4.17: Measured behavior of the regulator during operating mode changes

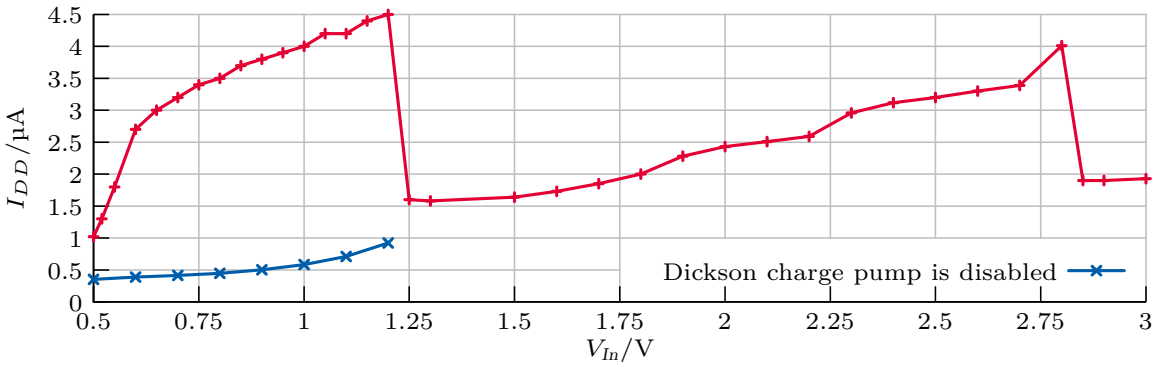


Figure 4.18: Measured current consumption of the regulator

1.2 V is worth to examine. Figure 4.17 summarizes the measured behavior of the regulator in this case. In Figure 4.17a the input voltage of the regulator drops from 1.75 V to 0.75 V causing the regulator to change its mode from normal operation to pumping operation. Thus the output voltage changes from a constant value to a periodic output. In Figure 4.17b the input voltage shows a rising edge. Here the mode of the regulator is changed from pumping operation to regular operation. Thus the output voltage changes from a periodic behavior to a constant value.

Figure 4.18 shows the measured current consumption of the regulator. For input voltages below 1.2 V, two cases are distinguished: The lower curve shows the current consumption of the regulator when the Dickson charge pump is disabled. The upper curve represents the current consumption when the Dickson charge pump operates and the buffer capacitor is charged. Compared to the regulator presented in Chapter 4.2, the current consumption of the regulator is rather constant (compare to Figure 4.3). As discussed in the introduction, this is advantageous

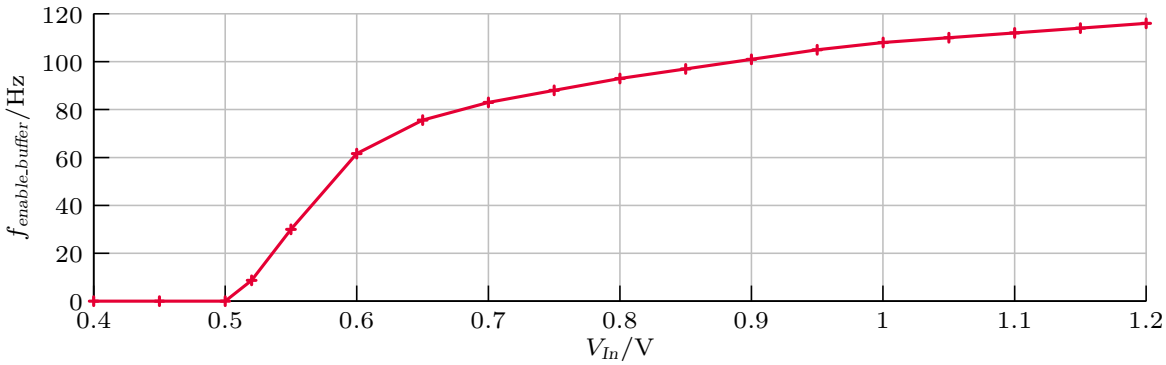


Figure 4.19: Measured frequency of the enable signal of the buffer

for power sources where the internal resistance increases with decreasing output voltages, like batteries.

Whenever the voltage in the buffer capacitor is sufficiently high to enable the regulator the *enable_buffer* changes to high. During *enable_buffer* being low, the buffer capacitor is charged. The lower the input voltage is, the longer it takes to charge the buffer. Figure 4.19 shows the frequency of the signal *enable_buffer* on different input voltages. The buffer capacitor has a capacity of 900 pF is in this case. The load on the buffer capacitor is the linear regulator without any additional load current. Figure 4.19 shows also that the measured minimum input voltage of the regulator is 0.52 V. The Dickson charge pump operates already at input voltages of 0.4 V but the voltage at the buffer capacitor does not reach 3 V and thus the regulator will not be enabled.

4.3.5 Conclusion

Chapter 4.3 presented a voltage regulator with an input voltage range of 0.52 V to 3.3 V. The output voltage is 1.2 V. When the input voltage is below 1.2 V, the regulator enters a periodic operation. First, a buffer capacitor is charged to 3 V by a Dickson charge pump. As soon as the voltage at the buffer capacitor reaches this threshold, the Dickson charge pump is disabled and the linear regulator is enabled. The regulator generates an output voltage of 1.2 V as long as the energy in the buffer capacitor is high enough. As soon as the output voltage of the regulator drops below 1.2 V, the linear regulator is disabled and the Dickson charge pump is enabled again.

The level detectors required for the regulator reuse different concepts presented in this thesis. To reduce the current consumption and to improve reliability, they are enhanced by clocked comparators. For power saving reasons, redundant level detectors are disabled whenever possible. Since a lot of blocks are periodically enabled and disabled, and there are different operating modes required a careful design of the control unit is required.

It has been shown that current starved ring oscillators generate glitches which pose a problem for digital circuits. By using a Schmitt trigger, they are prevented.

Compared to the regulator presented in Chapter 4.2, which has a similar input voltage range, the current consumption of this regulator is rather constant. This solves the problem of the large current demand at low input voltages. Of course, this solution is only usable when the output voltage of the regulator can be periodic. As WSNs typically operate according to a slot-based operation mode, this type of regulator is best suitable.

4.4 Conclusion

This chapter presented two regulators which also operate on input voltages lower than the output voltage. Both regulators are an improvement of the linear regulator presented in Chapter 2.3.2. The output voltage is still 1.2 V. The input voltage range of the linear regulator was from 1.2 V to 3.3 V. Here it is increased to 0.52 V to 3.3 V.

Two different concepts were investigated: (1) A charge pump between the input of the linear regulator and the regulator ensures that the voltage level at the input of the linear regulator is at least 1.2 V. For input voltages higher than 1.2 V, the charge pump is disabled. To satisfy the law of conservation of energy, the input current of the regulator needs to be a multiple of the load current in case the charge pump is active. Thus the lower the input voltage, the higher the current consumption of the regulator is. As long as the power supply is able to provide this current, this approach is sufficient. (2) The second implementation follows the harvesting concept presented in [72]. Whenever the input voltage of the regulator is below 1.2 V, a Dickson charge pump charges a buffer capacitor. During this phase, the output of the regulator is disabled. As soon as enough energy is stored in the buffer capacitor, the Dickson charge pump is disabled and the load of the regulator is enabled. When the buffer capacitor is empty, the Dickson charge pump is enabled again. This leads to periodic output voltage of the regulator. The advantage of this approach is that the current consumption of the regulator is much lower at low input voltages compared to the first approach.

The implementations of both architectures were not optimized in their efficiency and current consumption. The main idea was to prove and compare both concepts. While the first one is simple and straight forward, the second one requires a sophisticated control unit. The measurement results of both regulators are promising and encourage further improvement of these types of regulators.

Because of the low power consumption and the fact that no off-chip devices are required, both regulators are best suited to WSNs. Also, the dynamic response is fast, as the linear regulators have a low output impedance. Additionally, the linear regulators are decoupled from the input by the charge pump at low input voltages. This translates into a higher Power Supply Ripple Rejection (PSRR) compared to implementation where the linear regulator is directly supplied by the input voltage.

Chapter 5

Conclusion and Research Summary

> Am schenern macht's des Bácherl, es lauft allweil tala, aber's Herz, vo wos aussárinnt s'Herz des laßt's da.
>
> *(Franz Stelzhamer)*

In this thesis the topic of *Fully Integrated Low Power and Low Drop DC/DC Converters* was discussed in three different chapters, addressing different requirements in the regulator design. This chapter summarizes the most important findings on the regulator design. Also, general considerations on implementing ultra-low power DC/DC converters are presented.

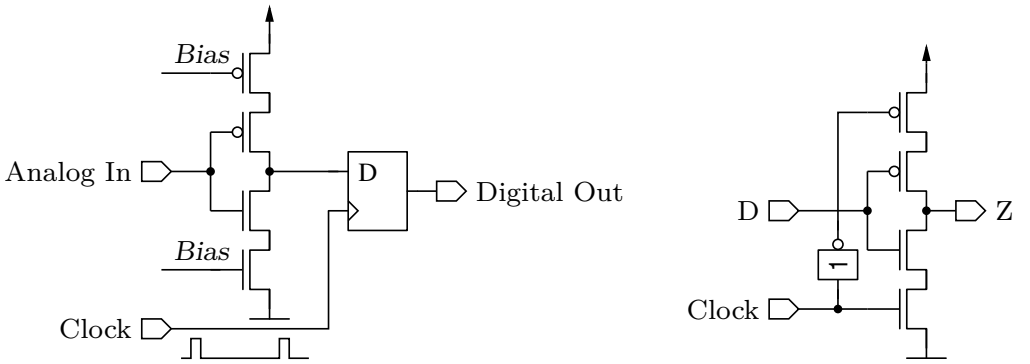
5.1 General Considerations in Ultra-low Power DC/DC Converter Design

Chapter 1.1 states that for the Wireless Sensor Node (WSN) of the future a highly efficient power management is required. Integrated batteries and innovative energy harvesting devices can then be used to supply the node, which reduces the volume and enables new applications. The regulator and power management implementations presented in this thesis show that it is possible to design highly efficient, fully integrated and robust solutions. No off-chip components are required for the ultra-low power circuits.

This thesis proved that circuits having bias currents down to 1 nA works well in a 0.13 µm CMOS technology. The area consumption of the circuits on silicon is still reasonable. This required finding new design concepts and revising traditional approaches. During the design of the presented circuits, similar problems addressing ultra-low power designs came up. This chapter summarizes these problems and presents solutions.

5.1.1 Analog to Digital Interface

CMOS technology has the advantage of zero static current (neglecting leakage currents) in the digital domain. Logic gates draw current only during input or output transitions. Thus it is preferable to process data in the digital domain. The inputs for the digital control logic are generated by analog circuits. For an appropriate operation of the digital logic, the output of



(a) ADI by gated D latch and current starved logic

(b) Transmission gate "inside" the inverter [77]

Figure 5.1: Clocked ADI

the analog circuits needs to be preprocessed by the Analog to Digital Interface (ADI) before they are fed into digital gates.

Three different tasks of the ADI are distinguished: (1) The Slew Rate (SR) of the signal needs to be sufficiently high to reduce the current consumption of the digital gate during input transitions. (2) If the analog circuit is disabled, its output voltage is undefined. As floating inputs need to be prevented, the ADI has to isolate such signals from the digital gates. (3) During startup of analog circuits, the output may generate spikes. These spikes need also be isolated.

How theses tasks are accomplished is discussed in the following section.

Slew Rate

CMOS gates make use of complimentary transistors connected in series. In the static case, only one transistor conducts. During transitions, both transistors conduct and current flows from the supply to ground. The lower the SR of the input signal of the gate, the higher the current consumption gets. The current is only limited by the channel resistance of the transistors. So as not to unnecessarily decrease the SR, parasitic capacitors have to be avoided.

The simplest approach to limit the current consumption is to increase the channel resistance by increasing the transistor lengths. If the length is increased, not only the current consumption decreases, but also the output SR of this gate. Thus the current consumption of the following gate increases. As the input capacitance is increased by the larger gate length the current consumption of the previous gate rises too. So, multiple gates have to be cascaded. There is an optimum number of gates. Finding this optimum is a complex task. Moreover the optimum depends on a many parameters and can only be found for one operating point.

A more advanced approach is to use a current starved logic. Here, the maximum current is limited by current sources and sinks. Again, cascading is required.

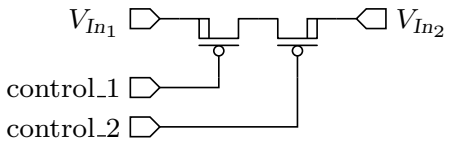


Figure 5.2: Power switch

The best solution found in this thesis is to use a gated D latch in combination with a current starved logic. Figure 5.1a shows this concept. If the clock is at ground level, the voltage level at the signal *Analog In* does not affect the current consumption. If clock is in its high state and *Analog In* is at ground or supply level, no static current is drawn by the latch. The worst case scenario is that *Analog In* changes its state during *Clock* being high. By choosing a large duty cycle of the clock signal, this is very unlikely. Additionally, the current starved logic ensures a minimum SR at the input of the latch. As this approach requires a clock signal, it is only useful if a clock signal at a reasonable frequency is available. This concept is first applied for the level detectors in Chapter 4.3.

According to [77], different methods exist to implement a D latch. To prevent the current during transitions on the input as described above, the implementation variant using an inverter with a transmission gate "inside" is required. Figure 5.1b shows the schematic of an inverter with a transmission gate "inside". As long as the signal *Clock* is in low state, the output Z is high ohmic regardless of the state of the signal D. This block is the first stage of the latch.

Isolation Logic and Startup

Especially for low power designs, unused blocks are disabled whenever they are not required. Circuits without supply generate undefined outputs which have to be isolated from the digital control unit. The simplest approach is to use an AND gate. One input is the output of the analog block and the other is an enable signal. Whenever enable is zero, the output of the gate is at ground level regardless of the state of the other input. Usually, the enable signal is also used to enable the analog block itself. As the circuit requires some startup time, it is possible that wrong outputs are generated during the first period. Chapter 2.3 presented an isolation logic which also solves this problem. Figure 2.4 on page 22 shows the simplified circuit. The isolation logic monitors the supply voltage of the analog block, which is in startup state. As soon as the supply crosses a certain threshold, the outputs are enabled.

5.1.2 Power Switch

To disable unused blocks and to limit leakage currents, power switches are required. If two voltage sources should be combined, two major issues have to be considered: First, bulk currents need to be prevented. Second, the control voltage of the switch has to be at an appropriate level. In this thesis two PMOS transistors are connected in series as shown in Figure 5.2. As either V_{In_1} or V_{In_2} can be at a higher voltage level, two transistors are required to prevent bulk

currents. At least one of the two control signals must be able to reach the highest occurring voltage level or higher to be able to turn off the switch.

5.1.3 Voltage Level Shifters

The different regulator architectures presented in this thesis make use of different internal supply voltages for individual blocks. Thus voltage level shifters are required to control these blocks. As explained in detail in Chapter 2.3.2, conventional level shifters in CMOS technology may lead to problems if the lower supply is not available. Thus the design of the concept must be done carefully, to ensure an appropriate operation of the level shifters.

5.1.4 Voltage Level Detectors

The voltage regulators presented in this thesis have different operating modes, which are selected by voltage level detectors. The state-of-the-art approach, as presented in [15], requires a voltage divider. This architecture suffers from the current consumption of this voltage divider. To overcome this problem, this thesis presented a new approach: A reference voltage is scaled to the required detection level by a buffer. This buffer is supplied by the voltage which is monitored. Of course, the scaling is only possible if the supply voltage is higher than the detection level. By evaluating if the scaling was successful, the detector decides if the input voltage is higher than the detection level.

5.1.5 Current Starved Ring Oscillator

Special attention is given to the current starved ring oscillator. This well known and commonly used circuit showed startup problems at bias currents lower than 10 nA. A parasitic capacitor prevented the oscillator from oscillating. The low bias current is not able to drain this capacitor in an appropriate time interval. Thus a startup circuit is required, which drains this capacitor. Measurements showed that the oscillator can be stopped if spikes are injected into the supply voltage of the oscillator. The reason is that the parasitic capacitor introduces a zero in the small signal transfer function of the oscillator. Due to this zero, the “Barkhausen’s Criteria” is not fulfilled, which is a necessary condition for oscillators.

5.1.6 Bias Cell

Analog circuits usually require a reference cell which generates a reference voltage and a bias current. Bandgap references are a quite common implementation. This type of reference cell requires an ohmic resistor. In ultra-low power designs this resistor would have several megaohms, which consumes a large area on silicon. Thus other concepts have to be found. In this thesis a reference cell which exploits the different operating regions of the MOS transistor is presented. For this circuit no resistor is required. Thus the area consumption becomes reasonable. The drawback of this implementation is the large statistical variation of the reference voltage and

the reference current compared to the traditional bandgap circuits. Also, the variation of the reference voltage on temperature changes is larger.

5.2 Implemented DC/DC Converters

Chapter 2 presented a WSN dedicated to Tire Pressure Monitoring Systems (TPMSs). A fully customized Power Management Unit (PMU) was presented. Four different voltage regulators provide the necessary supply voltages for the different blocks. Two of them – the regulator for the on-chip temperature sensor along with an Analog to Digital Converter (ADC) and the digital control unit – are considered as ultra-low power implementations. The input conditions (input voltage range and input voltage transients) require robust architectures. Using an NMOS architecture, as shown in Figure 1.2a, is found to be the best approach. The low output impedance of the pass device allows a more relaxed regulation circuitry, e.g. phase compensation to ensure stability of the feedback loop is more simpler. For low-dropout operation, a charge pump is required to supply the gate of the pass device. In literature two different methods are presented: (1) The charge pump supplies the error amplifier of the regulator, or (2) a series capacitor is connected between the output of the error amplifier and the gate of the pass device. This coupling capacitor is charged to a constant voltage by a charge pump. Here, the first method was used. The current consumption of this implementation is higher, but it provides a better Power Supply Ripple Rejection (PSRR) as the error amplifier's supply is isolated from the input of the regulator by the charge pump.

To prolong the life time of the WSN, the efficiency of the DC/DC conversion needs to be improved. Linear regulators, as presented in Chapter 2, have a very low efficiency. Chapter 3 presented a solution for a more efficient DC/DC conversion using Switched Capacitor (SC) techniques. To improve the dynamic response of the SC regulator, a linear regulator operates in parallel. This linear regulator operates only during fast input voltage or load current transients. Thus, the regulator provides both: a highly efficient DC/DC conversion and a fast dynamic response. In addition to the unavoidable losses in the SC regulator, the current consumption of the building blocks limits the achievable efficiency. Therefore, a major design constraint of the various building blocks presented in this chapter was to reduce the current consumption. A new concept to implement level detectors was presented. Also, different oscillator architectures and their suitability for ultra-low power implementations were discussed. For the reference cell, no ohmic resistor or bipolar transistor was used.

Chapter 4 improved the linear regulator presented in Chapter 2 by increasing the input voltage range. Using a charge pump enabled output voltages which are higher than the input voltage. The chapter presented two different techniques. The first makes use of a charge pump between the linear regulator and the input. This charge pump doubles the input voltage, if it is smaller than the desired output voltage of the regulator. Thus it ensures a sufficiently high supply voltage for the linear regulator. Especially at low input voltages, the current consumption of this regulator is increasing. To overcome this problem, a second architecture was presented. Here also a charge pump is used to amplify the input voltage. To reduce the current consumption during low input voltages, the linear regulator is disabled in case the

charge pump is enabled. The charge pump transfers energy from the input to a buffer capacitor. As soon as enough energy is stored in the buffer capacitor, the linear regulator is enabled and supplied by this energy. Of course, the output of the regulator now has a periodic behavior. As WSNs typically operate according to a slot-based operation mode, this type of regulator is best suitable.

The achievable speed of analog circuits depends on the bias current. For this reason, ultra-low power circuits are slow. Especially for voltage regulators, this is a serious issue, as the transient characteristics (refer to Chapter 1.5) get worse. This thesis proved that with smart system design ultra-low power voltage regulators still provide good regulation capabilities. The presented voltage regulators are a first step to developing the WSN of the future – a tiny and self-sustained sensor which operates reliably with a long lifetime in a harsh environment.

Appendix A

Test chip Layouts

Each circuit presented in this thesis has been fabricated in an Infineon 0.13 µm CMOS process. This chapter gives an overview of the layouts of the various test chips containing these circuits. The Integrated Circuits (ICs) are named according to the respective chapter names.

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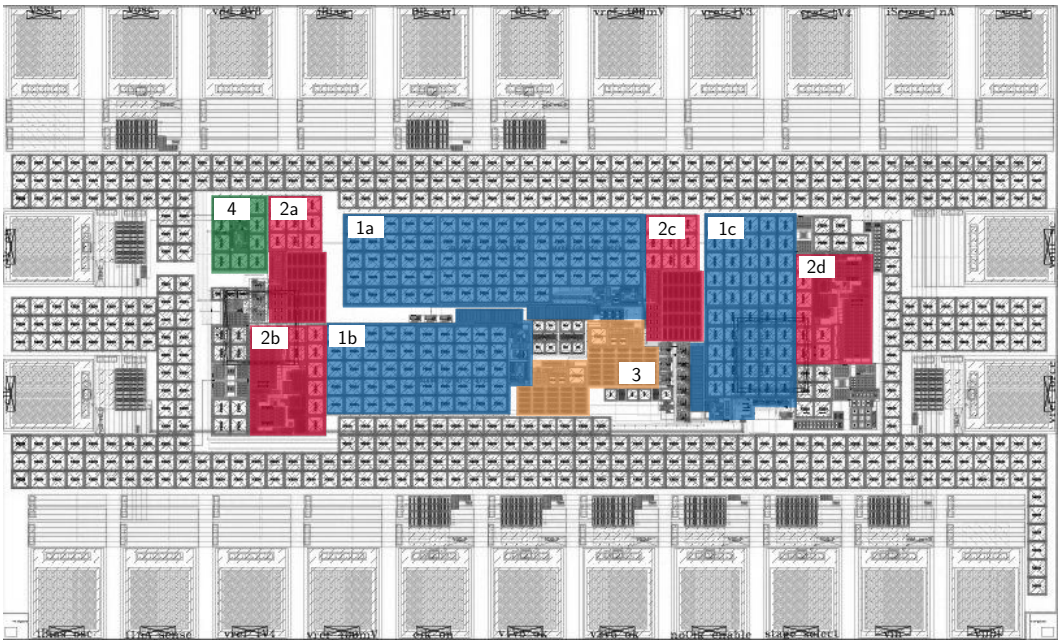
A.1 Power Management for an Ultra-low Power Wireless Sensor Node

Figure A.1: Test chip TO1209

1	. . . . .	Regulator for the On-Chip Temperature Sensor along with the Analog to Digital Converter
2	. . . . .	Regulator for the Digital Control Unit
3	. . . . .	Regulator for the Carrier Generation Unit
4	. . . . .	Regulator for the Power Amplifier

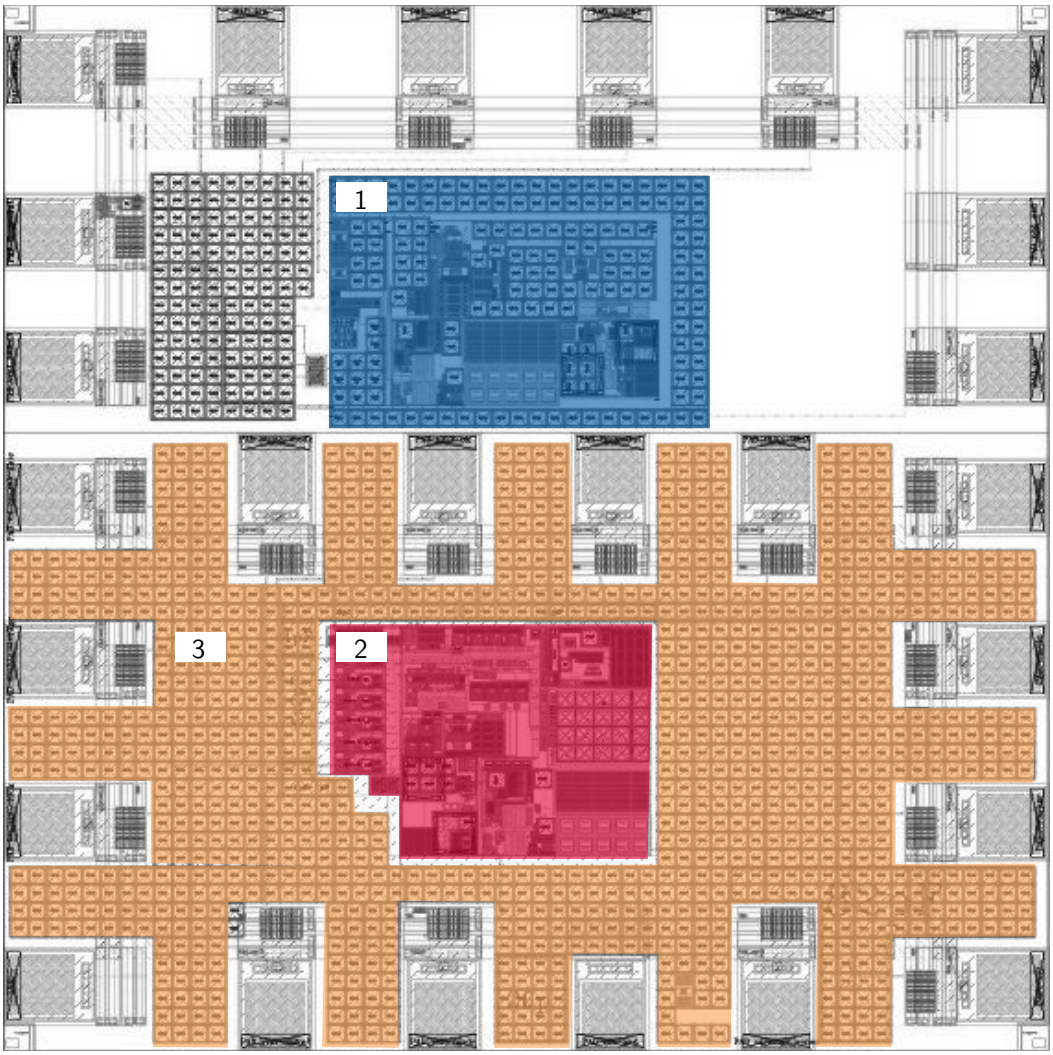
A.2 A Robust and Fault Tolerant Switched Capacitor Regulator



1	.....	**Hybrid regulators**
1a	.....	3-stage regulator
1b	.....	3-stage regulator without oscillator
1c	.....	2-stage regulator
2	.....	**Bias cells**
2a	.....	Reference scaling (standalone version)
2b	.....	Reference cell (standalone version)
2c	.....	Reference scaling (for regulators)
2d	.....	Reference cell (for regulators)
3	.....	**Level detectors**
4	.....	**Current starved ring oscillator**

Figure A.2: Test chip TO0709

A.3 Voltage Regulators for Low Input Voltages



1 . . . . . Regulator for Permanent Supply Requirements
2 . . . . . Regulator for Slot-Based Operation
3 . . . . . 850 pF on-chip buffer

Figure A.3: Test chip TO1210

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