Simon Josef Außerlechner

Proton Induced Doping and Space Charge Layer Formation in Organic Thin-Film Transistors

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Ao.Univ.-Prof. Dipl.-Ing. Dr.techn. Egbert Zojer

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To Mom and Dad.

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Abstract

In the present thesis several methods to change the characteristics of organic thin-film transistors (OTFT) are discussed.

First surface proton transfer doping is established as a relevant process for shifting the threshold voltage. Modifying the gate/dielectric-semiconductor interface of OTFTs with covalently bonded trichlorosilane molecules including an acidic functionality results in the formation of a negatively charged acid residue layer coexisting with proton doped pentacene molecules. This results in a shift of the threshold voltage to more positive values in the p-channel pentacene based OTFTs. The validity of this mechanism is confirmed by several experiments and simulations.

An alternative realization of a negative space charge layer that changes the threshold voltage is with electrons that are trapped at the gate/dielectric-semiconductor interface. In the current work, these electrons originate from dissociated excitons, where the latter are formed by UV illumination. Investigations of details regarding the trapping and detrapping process are provided paving the way for a simple and versatile organic memory device.

Besides their role as dopants, protons may play another crucial role in OTFTs, as they have been held responsible for bias-stress effects. To further clarify their role for that parasitic process, we have studied bias stress in basic conditions realized by exposing the device to ammonia gas.

Moreover, protons can be used for bulk doping of organic semiconductors. Also this process results in a shift of the threshold voltage to more positive values in p-channel devices. It can, for example, be achieved by exposing a pentacene transistor to hydrochloric acid vapor. HCl-induced doping, however, does not occur when using 6,13-bis(triisopropylsilylethynyl)pentacene (Tips-pentacene) as active layer material, due to the side chains, which protect the molecule against protonation. In the last section of this thesis it is discussed that this different behaviour of the two semiconductor materials can be used to realize a pH-sensitive switch, when combining a pentacene and a TIPS-pentacene transistor to form a depletion-load inverter.

Kurzfassung

In der vorliegenden Arbeit werden verschiedene Methoden diskutiert, welche es ermöglichen die Schwellspannung in organischen Dünnfilmtransistoren (OTFTs) zu verschieben.

Mit Hilfe von dünnen, saure Funktionalitäten beinhaltenden Zwischenschichten konnte Protonentransferdotierung beobachtet werden. Die dabei eingesetzten Trichlorsilanmoleküle sind an der Grenzfläche zwischen Dielektrikum und Halbleiter kovalent gebunden. Die durch die Protonierung der Moleküle gebildete negativ geladene Schicht aus Säureresten führt zu einer Verschiebung der Schwellspannung zu positiven Werten in den verwendeten p-Kanal OTFTs. Der Mechanismus wurde sowohl mit verschiedenen experimentellen Methoden untersucht als auch durch Simulationen bestätigt.

Eine alternative Realisierungsmöglichkeit von negativ geladenen Raumladungen stellen Elektronen dar, welche an der Grenzfläche zwischen dem Dielektrikum und dem Halbleiter eingefangen (getrapped) werden. In der vorliegenden Arbeit wurden diese Elektronen durch Dissoziation von mit UV-Licht erzeugten Exzitonen erzeugt. Dazu wurden Untersuchungen hinsichtlich "Trapp-" und "Enttrapp-Vorgängen" durchgeführt, wodurch die Realisierung eines Speicherbausteines möglich scheint.

Protonen werden neben ihrer Möglichkeit organische Halbleiter zu dotieren auch für den sogenannten Bias-Stress Effekt verantwortlich gemacht. Um dies zu überprüfen wurden Versuche mit Ammoniak Gas durchgeführt.

Darüber hinaus lassen sich organische Halbleiter nicht nur an der Grenzfläche zum Dielektrikum sondern auch in ihrem gesamten Volumen dotieren. Dies führt ebenfalls zu einer Verschiebung der Einsatzspannung zu positiven Werten in p-Kanal Transistoren. Die Volumendotierung kann im organischen Halbleitermaterial Pentacen durch Salzsäure-Exposition erzielt werden. Dies ist bei Verwendung des Halbleiters 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-Pentacen) nicht beobachtbar. Ursächlich hierfür sind die Seitenketten, welche eine Dotierung durch Protonen verhindern. Der genannte Unterschied der Halbleitermaterialien bezüglich Volumendotierung ermöglichte die Realisierung eines pH-sensitiven Schalters. Dies wurde durch die Ver-

schaltung eines Pentacen basierenden und eines TIPS-Pentacen basierenden Transistors zu einem sogenannten Depletion-Load Invertierer demonstriert.

Contents

Chapter 1

Introduction

Organic electronics combines the well established theories, powerful simulation methods and high-end experimentally methods of solid state physics with the huge variability of organic chemistry. Therefore, organic electronics opens a large field of applications. For example, high quality solid state lighting especially using organic light emitting diodes (OLEDs) [1] and high efficient organic photo voltaic (OPVs) [2] should be possible. Another field of application for organic semiconductors are organic thin-film transistors (OTFTs) [3]. They are used for example as driver devices in commercially OLED displays, which results in rollable displays. Additionally, they are used as sensors [4] to build up more complex circuits like inverters [5] or radio-frequency identification (RFID) transponders [6].

Moreover, organic electronics is also a highly attractive area for fundamental research. There are still unsolved fundamental problems, for example concerning metal/organic-semiconductor interfaces, charge transport in organic materials and organic superconductivity [7].

In part I of the present thesis several fundamental aspects are discussed: In chapter 2 metal-oxide-semiconductor field-effect transistors (MOS-FETs) are compared to organic thin-film transistors (OTFTs) concerning the definition of relevant quantities like the threshold voltage (V_{th}), and charge transport through the device. Additionally, in this chapter several methods are described which are used to extract device parameter from device characteristics. In the chapter 3 basics concerning inverters are briefly focusing on the so called depletion-load inverter as this device will be used later in the thesis. Chapter 4 gives an overview about prominent organic semiconductors and, finally, in chapter 5 the fabrication steps of so called self-assembled monolayers (SAMs) are discussed.

In part II the results are summarized. In chapter 6 surface proton transfer doping is established as a process relevant for OTFTs containing acidic

interfacial layers. Due to covalently bonded molecules containing acidic functionalities at the gate-dielectric/semiconductor interface it is possible to shift the V_{th} of pentacene based OTFT to high positive values. This is not observable in 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) based devices. Additionally, this V_{th} can be compensated with the help of ammonia gas. In chapter 7 a memory is realized, that is based on a simple pentacene OTFT with SiO_x as dielectric layer. The programming and erasing step was done by UV light illumination and simultaneously applying positive voltage and negative voltage, respectively, between gate and source. In these devices charges trapped at the interface result in positive threshold voltages and the threshold voltage can be shifted back to the initional state by the erasing step. Chapter 8 dedicated the still unsolved reason of the so called bias-stress effect where we tested, whether ammonia exposure can be used to eliminate bias stress caused by protons. Finally in 9 a pH-sensitive switch was realized by a so called depletion-load inverter. This was achieved by combining a pH-sensitive (pentacene) and a pH-insensitive (TIPS-pentacene) transistor. In such a combination the inverter characteristics is enabled/disable by exposure to an acid or base. In this way, one can switch between a high level voltage state and a low level voltage state at the output for a high level input voltage at the input.

Part I

Fundamentals

Chapter 2

Basics of field-effect transistors

There exist two classes of field-effect transistors (FETs), namely metal-oxide-semiconductor (MOS) FETs and organic thin-film transistors (OTFTs), which are relevant for the present thesis. For a better understanding of their working principle, first the so called MOS capacitor is explained, followed by a detailed description of MOS-FETs and OTFTs. The used references for MOS capacitor and MOS-FET are [8], [9] and [10].

2.1 MOS capacitor

A MOS capacitor consists of a metallic gate electrode (M) on an oxidic dielectric (O), which acts as insulation to the semiconducting substrate (S). To contact the substrate, which is also called bulk, there is another metallic electrode, the bulk electrode. Usually it is grounded and all voltages are defined with respect to this grounded bulk potential. Depending on the voltage applied between gate and bulk (V_{GB}), one can distinguish three different bias cases referred to as accumulation, depletion and inversion (Fig. 2.1). The following considerations are given for a MOS capacitor comprising p-type (p-doped) semiconducting substrates.

2.1.1 Accumulation

Applying a negative V_{GB} leads to electron attraction in the gate electrode and hole attraction in the substrate. Therefore, a hole conducting layer forms in the semiconductor (Fig. 2.1 $(a), (b_1)$ and (c_1)). It is called p-type channel and is realized by holes, which are the majority carriers in p-type semiconductors. Increasing V_{GB} from low negative values to higher negative values leads, finally, to the flat band condition.

2.1.2 Flat band condition

The flat band condition is realized, when V_{GB} equals the flat band voltage (V_{FB}). This is the case, when no net charge is present on both sides of the dielectric layer. Charge is connected with electrostatic potential via Poisson equation. So no charge results in no band bending, which means that the bands are flat. V_{FB} can also be defined as difference between the gate work function (ϕ_g) and the semiconductor work function (ϕ_{sc}).

$$V_{FB} = \phi_g - \phi_{sc} \tag{2.1}$$

One can distinguish between three cases:

- In the simplest, but unrealistic case, ϕ_g equals ϕ_{sc}. Therefore, flat band condition is achieved at zero bias. ($V_{FB} = 0\,\mathrm{V}$)
- When $\phi_g > \phi_{sc}$, then $V_{FB} > 0\,\mathrm{V}$ (Fig. 2.1 (d_1)). Therefore, the zero bias situation is fulfilled in accumulation (Fig. 2.1 (b_1)).
- $\phi_g < \phi_{sc}$ results in $V_{FB} < 0\,\mathrm{V}$ (Fig. 2.1 (b_2)) and, therefore, zero bias situation is achieved in depletion. (Fig. 2.1 (d_2)).

2.1.3 Depletion

By applying V_{GB} larger than V_{FB} positive charges are attracted at the gate electrode. On the opposite site of the MOS capacitor the same amount of negative charges are formed by negatively charged acceptors (Fig. 2.1 (c_2), (d_2) and (e)).

2.1.4 Threshold voltage and inversion

Increasing V_{GB} finally results in attracting electrons to the dielectric-semiconductor interface. At this voltage, weak inversion starts. Further increase of V_{GB} results in forming an electron channel. This is the starting point of strong inversion and the voltage at this point is called threshold voltage (V_{th}). Electrons are the minority carriers in p-type semiconductor, but in this case they form the channel (Fig. 2.1 (f) and (g)).

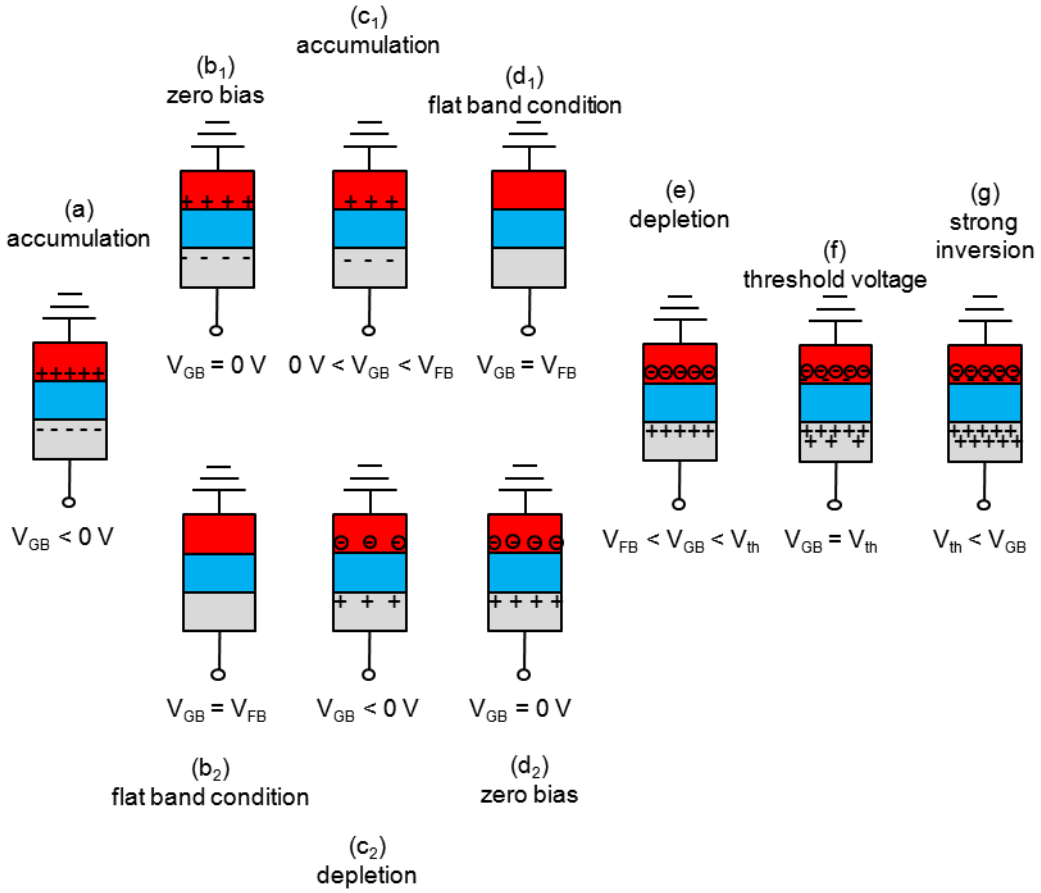

Figure 2.1: Different bias cases of a MOS capacitor, consisting of a metallic gate (grey), oxidic insulation layer (cyan) and a p-doped semiconductor (red). The symbols + and - represent holes and electrons, respectively, and $\ominus$ represent negative charged atomic cores. Figures $(b_1), (c_1)$ and (d_1) show the situation if $\phi_g > \phi_{sc}$ and Figures $(b_2), (c_2)$ and (d_2) are representative for $\phi_g < \phi_{sc}$.

2.2 MOS-FET

A MOS-FET is a voltage controlled resistor. It consists of a MOS capacitor and two additional electrodes, namely source and drain (see Fig. 2.2). Usually source and bulk electrodes are electrically connected and grounded. So from now on we write V_{GS} instead of V_{GB}. By applying V_{GS} one can vary the resistance between source and drain. In an n-channel (p-channel) or n-type (p-type) MOS-FET the channel is formed by the minority charge carriers electrons (holes) in a p-doped (n-doped) semiconducting substrate. To be

consistent with the considerations about MOS capacitor, we again choose a p-type substrate. In this case, source and drain are realized by n-doped islands in the p-doped substrate. The semiconducting islands are connected to metallic wires for biasing. Therefore, one has to dope the islands in a sufficient highly way, resulting in an ohmic contact, instead of a Schottky contact.

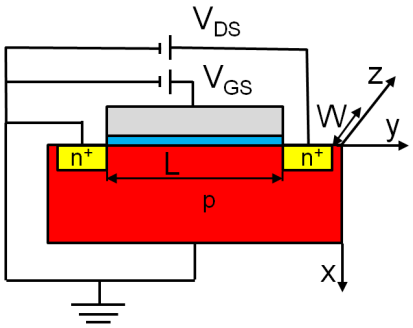

Figure 2.2: Schematic structure of a biased n-channel MOS-FET, consisting of gate (gray), oxide (blue), p-doped bulk (red) and heavily n-doped source and drain (yellow). The source is the grounded left electrode and the drain is on the right. L is called channel length and W is the channel width. It is the second relevant geometric value for the channel between source and drain.

2.2.1 Threshold voltage of MOS-FETs

If one choose $V_{GS} < V_{th}$ the region between source and drain close to the dielectric-semiconductor interface is in depletion. Therefore an applied voltage between source and drain (V_{DS}) do not lead to a current (I_{DS}) between them. Because, whatever the polarity of the applied V_{DS} is, one of the pn-junctions, forming by the source and drain electrodes and the semiconductor bulk, is reverse biased and therefore closed.

Choosing $V_{GS} \geq V_{th}$ results in n-channel formation between source and drain. Therefore, applying V_{DS} lead to a current between source and drain, but also influences the channel potential. It is uniform in the y-direction without applying V_{DS} and decrease approximately linear from source in the direction of the drain when applying $V_{DS} < V_{GS} - V_{th}$. If one choose V_{DS} equal to $V_{GS} - V_{th}$, the channel is pinched of at the drain electrode. This so called pinch-off point moves in the direction of $-y$ by applying $V_{DS} > V_{GS} - V_{th}$. A second important parameter of MOS-FETs is the so called charge carrier mobility (μ).

2.2.2 Phenomenologically view on charge carrier mobility

The classic definition of μ connects the drift-velocity ($\vec{v_D}$) of a charge carrier with the applied electric field ($\vec{E}$).

$$\vec{v_D} = \mu \vec{E} \tag{2.2}$$

In the case of an anisotropic material, μ is a second rank tensor. For sake of simplicity, we presuppose an isotropic transport medium. In this case it is simply a scalar.

μ is also connected to the electric conductivity (σ) by

$$\sigma = e(\mu_e n + \mu_h p), \tag{2.3}$$

where n and p are the electron and hole volume densities, respectively, e is the elementary charge, μ_e is the electron and μ_h is the hole mobility. Together with the ohm's law,

$$\vec{j} = \sigma \vec{E}, \tag{2.4}$$

one gets the following equation for the current density ($\vec{j}$) .

$$\vec{j} = e(\mu_e n + \mu_h p)\vec{E} \tag{2.5}$$

As one can see from Equation 2.5, $\vec{j}$ for a given $\vec{E}$ depends, on the one hand, on the charge carrier volume densities n and p and, on the other hand, on the material dependent values μ_e and μ_h.

To compare different transistors, in the following a classification and characterization methods are discussed.

2.2.3 Device classification and characterization

Depletion and enhancement mode

To classify MOSFETs, two different modes were defined, depending on the electronic behavior without gate-source bias. A MOS-FET is called a depletion mode or normally-on device, if a channel between source and drain is formed, even without applying V_{GS}. When applying a non-zero V_{GS} is necessary to get a channel, it is called enhancement mode or normally-off device.

Transfer and output characteristics

Transfer and output characteristics are two complementary curves to describe the electronic behavior of MOS-FETs. Measuring the drain current (I_D) as function of V_{GS} and setting V_{DS} as parameter results in the so called transfer characteristic (Fig. 2.3). I_D is equal to I_{DS} in the case of no leakage. To get the output characteristic one has to set V_{GS} as parameter and measure I_D as function of V_{DS} (Fig. 2.4). To describe them theoretically, it is quite usual to differ three regions.

Cut-off, linear and saturation region

In the cut-off region ($U_{GS} < U_{th}$) the transistor is switched off and, therefore,

$$I_{DS} = 0A. \tag{2.6}$$

For the linear or also called ohmic region ($V_{DS} < V_{GS} - V_{th}$ and $U_{GS} \geq U_{Th}$) the following equation in MOS-FET theory is derived,

$$I_{DS} = \mu c_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right), \tag{2.7}$$

and in the saturation region ($V_{DS} > V_{GS} - V_{th}$ and $U_{GS} \geq U_{Th}$) the current is described by:

$$I_{DS} = \mu c_{ox} \frac{W}{2L} (V_{GS} - V_{th})^2. \tag{2.8}$$

c_{ox} is the capacitance per unit area of the gate-dielectric, W is the channel width and L is the channel length. Equation 2.6, Equation 2.7 and Equation 2.8 and the corresponding inequalities are derived for n-channel devices with V_{GS} independently μ. They are also valid in the p-channel case, when one exchanges the left and the right side in all inequalities. Additionally, one has to multiply I_{DS} by -1. This takes into account, that holes instead of electrons are the charge carriers.

Fig. 2.3 and Fig. 2.4 show a transfer curve family and a set of output curves, respectively, of an n-channel, enhancement mode MOS-FET.

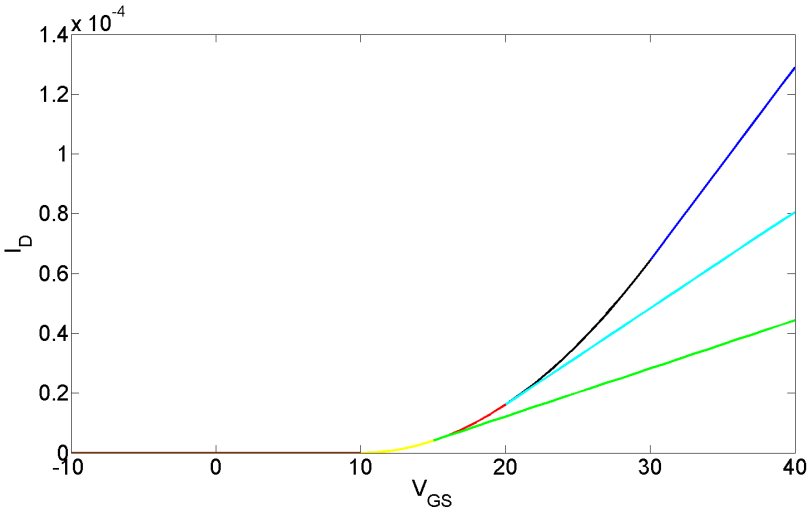

Figure 2.3: Cut-off region (brown), saturation region (yellow, red and black) and linear region (green, cyan and blue) of three different transfer curves. V_{th} is set to 10 V and V_{DS} is set to 5 V for the brown-yellow-green, to 10 V for the brown-yellow-red-cyan and to 20 V for the brown-yellow-red-black-blue transfer characteristic.

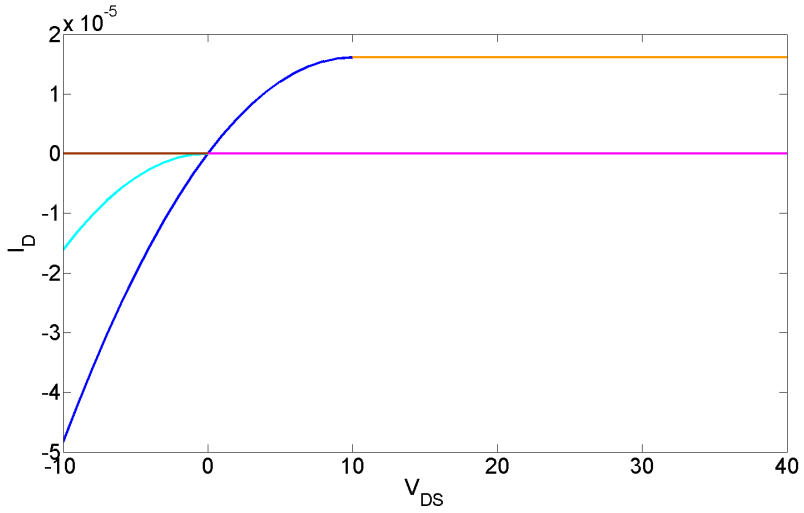

Figure 2.4: Cut-off region (brown), linear region (cyan and blue) and saturation region (pink and orange) of three different output characteristics. V_{th} is set to 10 V and V_{GS} is set to 5 V for the brown-pink, to 10 V for the cyan-pink and to 20 V for the blue-orange output curve.

As one can see in Fig. 2.3 and Fig. 2.4, I_{DS} in the linear region is a straight line in the transfer characteristic. In this region the channel potential between source and drain drops linearly. Saturation behavior is seen in the saturation region of the output characteristics, which means that I_{DS} is independent of the applied V_{DS}, because the channel is pinched of.

2.3 Organic thin-film transistor and comparison to MOS-FET

An OTFT is also a voltage controlled resistor. It has only three electrodes, namely the metallic source and drain electrodes (yellow in Fig. 2.5), and the gate electrode (green in Fig. 2.5) with an isolation layer (blue in Fig. 2.5); there is no bulk electrode. The semiconducting material, in which the channel is formed, is an organic material (red in Fig. 2.5). Another difference is the necessity of bulk doping in MOS-FETs, while OTFTs also work without doping of the organic layer. Fig. 2.5 shows the four possible OTFT structures.

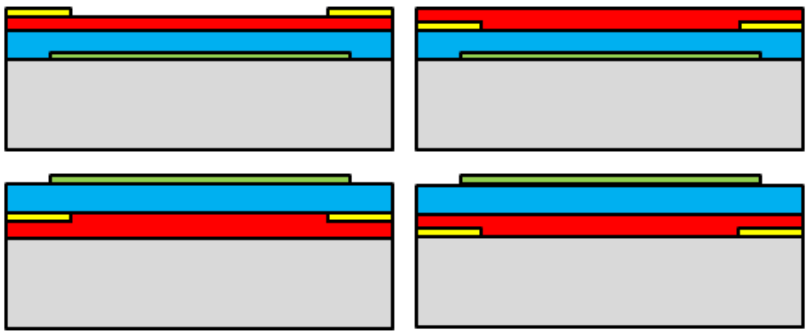

Figure 2.5: In the top-line on the left there are a top contact/bottom gate OTFT and on the right a bottom contact/bottom gate device shown. In the bottom line a top contact/top gate OTFT are shown (left) and a bottom contact/top gate device (right).

In our case, the gate electrode is made of doped silicon and the insulation layer is SiO_x. Together they form the substrate. In this setup, no additional substrate (gray in Fig. 2.5) is necessary. One can distinguish between devices in which the charges carriers are injected directly into the channel and devices in which the charge carriers have to drift through a region of low conductivity, before they arrive at the channel.

As discussed for MOS-FETs, usually source is grounded and all voltages are defined with respect to this potential. One can again distinguish between n-channel and p-channel OTFTs, normally-on and normally-off devices and one can again distinguish between cut-off, linear and saturation region.

To control the resistance between source and drain one has to apply V_{GS}. In OTFTs the channel between source and drain is formed in accumulation, in contrast to MOS-FETs, where this is the case in inversion. As described before, the channel in a p-doped (n-doped) semiconductor bulk of an MOS-FET is formed by electrons (holes). In contrast to that the channel of OTFTs is formed by holes (electrons) in p-doped (n-doped) organic materials. Therefore, the given V_{th}-definition for MOS-FETs as starting point of strong inversion, is not applicable to OTFTs.

2.3.1 Threshold voltage of OTFTs

For the sake of simplicity, first an undoped organic layer is supposed. In this case the organic semiconductor is an insulator without applying V_{GS}. To make it conductive, which means to come into accumulation, one has to apply $V_{GS} \leq V_{FB}$ in a p-channel device and $V_{GS} \geq V_{FB}$ in an n-channel OTFT. Therefore, an adequate definition of V_{th} in OTFTs is [11, 12],

$$V_{th} = V_{FB}, \tag{2.9}$$

because V_{FB} separates accumulation from depletion.

Applying $|V_{GS}| \geq |V_{FB}|$ leads to charge carrier injection from the source and drain electrode into the organic layer, if one chooses the material combination of the metallic electrodes and organic semiconductor in a suitable way. One can distinguish between two cases:

- efficient electron injection: If $(\phi_m + \Delta - E_i) < (\phi_m + \Delta - E_a)$, then electron injection dominates over hole injection.
- efficient hole injection: $(\phi_m + \Delta - E_a) < (\phi_m + \Delta - E_i)$ results in more efficient hole injection than electron injection.

ϕ_m is the work function of the metal, E_i the ionization energy of the organic material, E_a is the electron affinity of the organic material and $+\Delta$ is the interface dipole.

Another important factor is an adequate choice of the dielectric material. For example, SiO_x is an electron trapping material [13]. Therefore, to get a n-channel device it is not sufficient to get the electrons into the semiconductor, but one also needs to avoid trapping by the dielectric.

For the sake of generality, in the following a p-channel OTFT, including a p-doped organic semiconductor is chosen. In this case Equation 2.9 is no longer valid. As described in Refs. [11, 14, 12, 15] and when using the definition of the capacitance per unit area of a plate capacitor,

$$c_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{d_{ox}}, \tag{2.10}$$

one gets the following equation for V_{th} of an OTFT including a p-doped semiconductor:

$$V_{th} = V_{FB} + \frac{eN_A d_{sc}}{c_{ox}}. \tag{2.11}$$

ε_0 is the dielectric constant of vacuum, ε_{ox} the dielectric constant of the dielectric, which is in our case SiO_x, d_{ox} the thickness of the oxide, N_A the volume density of acceptors and d_{sc} the thickness of the semiconducting layer.

Moreover, this V_{th}-definition takes space charges (modeled by σ_{if}) and dipoles (modeled with $d_{dip}\sigma_{dip}$) at the dielectric-semiconductor interface, into account. This is realized by an extended definition of the flat band voltage,

$$V_{FB} = \phi_g - \phi_{sc} + \frac{d_{ox}\sigma_{if}}{\varepsilon_0 \varepsilon_{ox}} + \frac{d_{dip}\sigma_{dip}}{\varepsilon_0 \varepsilon_{dip}}, \tag{2.12}$$

where d_{dip} is the dipole length and ε_{dip} is the dielectric constant of the dipoles.

A quite usual, but parasitic effect on V_{th}, which is a huge problem in OTFTs, is the so called bias-stress effect.

2.3.2 Bias-stress effect

It results in an shift of V_{th} in the direction of the applied V_{GS} during device operation. Usually, it is described by a stretched exponential model [16]:

$$\Delta V_{th}(t) = V_0 \left\{ 1 - exp\left[-\left(\frac{t}{\tau} \right)^{\beta} \right] \right\}. \tag{2.13}$$

$\Delta V_{th}(t)$ is the shift of V_{th} at time t, V_0 is V_{th} at the beginning of the gate-source bias-stress, t is the stress time and τ and β are fit parameters. Without applying a gate bias, the OTFT recovers.

The microscopic reason for the bias-stress effect is still under discussion. Mostly it is attributed to charge carriers trapped in deep traps located in the gate-dielectric, in the organic semiconductor, or at the interface between them [17]. There exists also an alternative hypothesis to explain bias-stress effect, namely by proton migration in the dielectric [18, 19, 20]. In this

model, an electrolysis reaction of water, which is adsorbed at the dielectric-semiconductor interface, is proposed as proton source. These protons migrate into the SiO_x substrate and shielded the applied V_{GS}. As described in [20], the stretched exponential model is still valid.

2.3.3 Charge transport through a organic thin-film transistor

As pointed out above, by apply $|V_{GS}| \geq |V_{th}|$ a channel between source and drain is formed and when applying V_{DS} charges can flow. In contrast to MOSFETs, I_{DS} has two possible limitations, namely the resistance of organic semiconductor itself and the contact resistances of the source- and drain-semiconductor junctions. In the case of a dominant bulk resistance, the current is called bulk or space-charge limited and in the case of dominant contact resistances the current is called injection limited [21, 22, 23].

Bulk limited transport

Bulk limited current takes place, if the source- and drain semiconductor junctions are ohmic contacts. An ohmic contact is defined as a contact, which has a much larger density of free charge carriers at the metal-semiconductor junction and in its directly surroundings than this is the case in the semiconductor bulk [21]. This means, that the contact supports the semiconductor with high enough amount of charges. In other words, an ohmic contact has a negligible contact resistance in comparison to the total resistance of the semiconductor device [8]. Therefore, to describe the charge transport through the path consisting of the source-semiconductor junction, the channel in the active organic material and the semiconductor-drain junction, in short called source-drain path, the important value for bulk limited currents is the charge carrier mobility of the organic semiconductor material.

Ideal crystals show perfect lattice periodic translation symmetry resulting in delocalized Bloch-states [24]. The charge transport is governed by such crystal-electrons [24]. In this case, the main limitation of transport are scattering events of crystal-electrons by phonons [23].

Charge transport in organic materials is quite different from that in inorganic semiconductors. To describe transport in these kind of materials many different models have been elaborated, which are reviewed in [23] in an excellent way. As a first example, an organic material, without chemical or physical defects is assumed. In this case the transport behavior is governed by the interplay of electron-electron and electron-phonon coupling [23]. In

contrast to inorganic solids, in organic materials the electron-phonon coupling is usually higher, resulting in the formation of a quasi particle called polaron, leading to dynamic disorder [23]. One prominent model to describe polaron transport is based on Marcus theory [25], where sometimes one talks in this case about hopping transport [23]. Due to the fact that defects cannot neglected in most organic materials instead of the so called polaronic charge transport models static disorder models are presented here [23].

Static disorder results in the formation of spatially localized states, called Anderson localization (chapter 1 of [22] and [25]), and so called extended states, which are still delocalized ([23] and chapter 1, 2 and 6 of [22]). They are separated from each other by the mobility edge. In general mobility edges of electrons and holes are different and define the mobility gap like the band gap in crystalline materials. The mobility edge of electrons (holes) in disordered materials is the analogue to conduction (valence) band edge of ordered materials (chapter 1 of [22]). Depending on the kind of states, which are relevant for charge transport, one can split up the static disorder models in two classes.

- Extended state transport: In this case charge carrier transport is governed by the extended states, but charge carriers could also be trapped in localized states, called traps. After some time they are thermally activated to the extended states. As we can see, both extended and localized states, are involved in charge transport. This idea was originally developed for inorganic amorphous materials (for example [26]) and is now used as multiple trapping and thermal release (MTR) model even for micro crystalline organic materials [27]. Within this model, one can derive μ as,

$$\mu = \mu_0 \frac{n_c}{n_t} exp\left[-\frac{E_c - E}{k_B T}\right], \tag{2.14}$$

  where μ_0 is the mobility of the bottom extended states, n_c is the volume density of extended states near the band edge, n_t is the volume density of localized or trap states, E_c is the mobility edge, E is the constant energy of trap states, k_B the Boltzmann constant and T the temperature.

- Hopping transport: Such models are typically used to describe amorphous materials. In this models no delocalized states are involved in transport, like it was the case in the MTR model. The transport is governed by hopping between localized states. One prominent representative of hopping transport is the variable range hopping (VRH)

model by Vissenberg and Matters [28]. In their model the hopping process is a thermally activated tunneling process [28]. Therefore, the transition rates are described by the Miller-Abrahams formalism [29]. The tunneling transition probability for an electron which tunnels from state i to state j with lower energy than the energy of state i is given by:

$$\nu_{ij} = \nu_0 exp\left(-\frac{2r_{ij}}{\alpha}\right). \tag{2.15}$$

Additionally, one can derive the transition probability for tunneling from state i to a higher energy state j by:

$$\nu_{ij} = \nu_0 exp\left(-\frac{2r_{ij}}{\alpha}\right) exp\left(-\frac{E_j - E_i + |E_j - E_i|}{2k_B T}\right). \tag{2.16}$$

ν_0 is a preexponential factor, r_{ij} is the distance between state i and state j. The localization length α describes the exponential decay of the localized wave functions of the localized states, E_i is the energy of the initial state and E_j is the energy of the final state. The equations are valid in the case of an occupied state i and an unoccupied state j.

In this model an exponential density of states (DOS) in the form of

$$D(E) = \frac{n_t}{k_B T_0} exp\left(\frac{E}{k_B T_0}\right), \tag{2.17}$$

is often used [28]. With the help of percolation theory the following proportionality for μ in an OTFT, containing an amorphous organic semiconductors has been derived:

$$\mu \propto exp\left(-\frac{E_a}{k_B T}\right), \tag{2.18}$$

where E_a is the so called activation energy [28].

Increasing negative V_{GS} leads to a decrease of E_a and, therefore, to an increase of μ. In other words, μ depend on V_{GS}.

Moreover μ increases with increasing T, because in this case transport is phonon or thermally activated [28]. This is in contrast to μ of perfect crystalline materials, where phonons are the main limiting factor of charge transport, due to scattering.

Mobility degradation

In contrast to the above described situation, where μ increases with increasing $|V_{GS}|$, also the opposite behavior is observed for high $|V_{GS} - V_{th}|$

in OTFTs. This behavior is also known in the field of MOSFETs and there is attributed to a lower μ of the semiconducting material close to the gate/dielectric-semiconductor interface due to charged centers, surface phonons and surface roughness [30]. Mobility degeneration is also observed in OTFTs. A sufficiently high gate-source bias results in charge transport predominantly close to the gate/dielectric-semiconductor interface, where μ is lower, for example due to a higher amount of traps at the interface than in the bulk of the organic layer [31]. Therefore the overall μ decreases.

Injection limited transport

As mentioned above, the second main transport limitation in OTFTs is charge carrier injection. In case the source-semiconductor and drain-semiconductor contacts are non-ohmic contacts the contact resistance dominates in comparison to the resistance of the channel. To describe the voltage dependent charge carrier injection and ejection, it is quite usual to do this with Richardson-Schottky thermionic emission and Fowler-Nordheim field emission [21].

2.4 Parameter extraction

2.4.1 Transfer curve methods

To get V_{th} and μ from transfer characteristics several different methods exist. All these methods have first been developed for analyzing MOS-FET characteristics [32], which can be described by Equation 2.6, Equation 2.7 and Equation 2.8. These equations are based on V_{GS} independent μ and negligible R_c. As described before, μ in OTFTs depends on V_{GS} and R_c is non-negligible. Additionally, V_{th} in MOS-FET is defined differently than in OTFTs. Nevertheless, it is quite common to use these classic extraction methods also for OTFTs [33].

Extrapolation in the saturation region method

The extrapolation in the saturation region (ESR) method [32] uses the saturation region of the transfer characteristics. Plotting $\sqrt{I_D}$ as function of V_{GS} and extrapolate this function linearly (in the direction of the V_{GS}-axis) at its maximum slope, one get V_{th} as intercept of the V_{GS}-axis. Additionally one can derive μ from the slope of the extrapolation function.

Extrapolation in the linear region method

This method (ELR) [32, 33] uses the linear region of a transfer curve ($I_D(V_{GS})$). Extrapolating $I_D(V_{GS})$ at its maximum first derivative to the V_{GS}-axis results in an V_{GS}-axis intercept. By adding $V_{DS}/2$ to the V_{GS}-axis intercept one get V_{th} and from the slope of the extrapolation function one can derive μ.

Second derivative method

The SD method [32, 33] defines V_{th} as V_{GS} at which the transfer curve has highest curvature. By this method one can only determine V_{th}, but not μ.

Second derivative logarithmic method

The second derivative logarithmic (SDL) method [32, 33] uses the logarithmic transfer curve ($log\,[I_D(V_{GS})]$) and defines V_{th} as the V_{GS} with highest curvature of $log\,[I_D(V_{GS})]$. This voltage is often referred to as turn-on voltage (V_{on}). As it was the case for SD method, one can not determine μ with SDL method.

2.4.2 Transmission line method

The transmission line method or transfer line method (TLM), was first used to get the contact resistance in the field of inorganic thin-film transistors (for example [34, 35]) and later it was introduced also for analyzing OTFT measurements [36, 37]. Additionally, with TLM one can extract μ and V_{th} [35].

The method is based on the following expressions,

$$R_{on} = \left[\left(\frac{\partial I_D}{\partial V_{DS}} \right) \Bigg|_{V_{DS} \to 0}^{V_{GS}} \right]^{-1} = R_{ch} + R_i + R_e \tag{2.19}$$

where R_{on} is the total resistance for a current I_D through an OTFT at negligible V_{DS}, that is the sum of the channel resistance R_{ch}, the parasitic injection contact resistance (R_i) and parasitic ejection contact resistance (R_e) [34]. As it is not possible to determine R_i and R_e separately with TLM, one defines the sum of R_i and R_e as the contact resistance (R_c):

$$R_c = R_i + R_e. \tag{2.20}$$

For R_{ch} in Ref. [34, 35, 36, 37] the following equation is given in a heuristic way,

$$R_{ch}(L) = \frac{1}{c_{ox}\mu W(V_{GS} - V_{th})} L, \tag{2.21}$$

for the device being in the linear regime and for $V_{DS} \to 0$ and for a given V_{GS}. Equation 2.19, Equation 2.20 and Equation 2.21, lead to:

$$R_{on}(L) = \left[\left(\frac{\partial I_D}{\partial V_{DS}} \right) \Big|_{V_{DS} \to 0}^{V_{GS}} \right]^{-1} = \frac{1}{c_{ox} \mu W (V_{GS} - V_{th})} L + R_c. \tag{2.22}$$

As one can see from Equation 2.22 [34], R_{on} scales linearly with L for a given V_{GS}.

Therefore, to determine R_c for a given V_{GS}, one has to measure output characteristics and differentiate I_D with respect to V_{DS} numerically. The value,

$$\left[\left(\frac{\partial I_D}{\partial V_{DS}} \right) \Big|_{V_{DS}=0}^{V_{GS}} \right]^{-1}, \tag{2.23}$$

is $R_{on}(L)$ for the specific V_{GS}. One has to repeat this procedure on OTFTs with different L for the same V_{GS}. Linear fitting of the plotted (R_{on}, L) data points gives R_c, for the chosen V_{GS}, as the intercept of the fitting function and the $R_{on}(L)$-axis. By taking R_{on} at $V_{DS} = 0\,\mathrm{V}$, one gets R_c for a zero voltage applied on the contact, which is in agreement with the definition of R_c, given for example in [8]. Usually one multiplies Equation 2.22 with W,

$$R_{on}(L) * W = R_{onn}(L) = \left[\left(\frac{\partial I_D}{\partial V_{DS}} \right) \Big|_{V_{DS} \to 0}^{V_{GS}} \right]^{-1} = \frac{1}{c_{ox} \mu (V_{GS} - V_{th})} L + R_{cn}, \tag{2.24}$$

which results in the width normalized R_c ($R_{cn} = R_c * W$) as intercept of the fitting function and the width normalized $R_{on}(L)$-axis ($R_{onn}(L)$-axis).

Moreover, with the help of the TLM one can derive μ and V_{th} [35]. $R_{onn}(L)$ is a linear function in L for a specific V_{GS} as parameter (Equation 2.24) with slope (k):

$$k = \frac{1}{c_{ox} \mu (V_{GS} - V_{th})}. \tag{2.25}$$

One can do the above fitting procedure for several different V_{GS}, resulting finally in as many different k values. By plotting the $(\frac{1}{k}, V_{GS})$ data points and fitting them linearly one can derive μ from the slope of the fit function and V_{th} from the axis intercept using the following equation.

$$f(V_{GS}) = \frac{1}{k} = c_{ox} \mu (V_{GS} - V_{th}) \tag{2.26}$$

Chapter 3

Inverter - basic overview and one example

3.1 Basics inverter overview

Field-effect transistors are devices often used in electronics. With the help of field-effect transistors, one can for example realize different gates, which are the basic components in digital electronics. The most simple one is the so called NOT gate. It has only one input and one output. A logical 1 (0) at the input is converted to a logical 0 (1) at the output. This functionality can be realized electronically by an inverter.

One can distinguish between bipolar and unipolar inverters. Complementary metal oxide semiconductor (CMOS) inverters uses n-channel and p-channel devices and, therefore, they are part of the bipolar inverter family. One example for an unipolar inverter, which use either n-channel or p-channel devices, is the so called transistor-transistor logic (TTL) inverter. It is realized by two transistors, the load transistor and the switch or driver transistor (The information for this section is taken from Ref. [8] and Ref. [38]).

3.2 Depletion-load inverter

In the so called depletion-load configuration of a TTL inverter (see Fig. 3.1), the load transistor is a depletion mode (normally-on) device and the driver transistor is an enhancement mode (normally-off) transistor. At the load transistor always a gate-source voltage (V_{GSl}) of 0 V is applied, because gate and source of the load transistor are short-circuited. Nevertheless, due to the normally-on operation of the load transistor, the source-drain path is

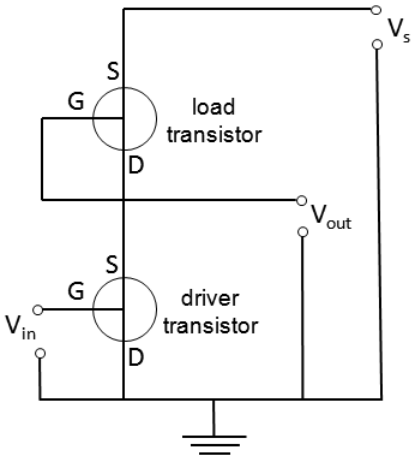

Figure 3.1: Schematic structure of a depletion-load inverter, wherein V_{in} is the input voltage, V_{out} is the output voltage, V_s is the supply voltage. S symbolizes source, D drain and G gate.

conductive. In short, the load transistor always is open. The gate-source voltage of the driver transistor (V_{GSd}) is also the input voltage (V_{in}) of the inverter. One can distinguish two cases, depending on the value of V_{in} in comparison to the threshold voltage of the driver transistor (V_{thd}). Applying $V_{in} < V_{thd}$ for a n-channel device and $V_{in} > V_{thd}$ for a p-channel device at the input, results in a driver transistor which is in the cut-off region. In other words, the driver transistor is closed. In the other case, a sufficiently high voltage is applied at the input, which means $V_{in} \geq V_{thd}$ in the case of n-channel transistor and $V_{in} \leq V_{thd}$ in a p-channel device. This results in an open device. To analyze the case of an open driver transistor an equivalent circuit of the inverter is presented in the following.

3.2.1 Equivalent circuit

As one can see in Fig. 3.1 the load and the driver transistor are electrically connected. The source-drain pathes of the two transistors represent non-ohmic resistors with a resistance of R_{sdl} for the load and a resistance R_{sdd} for the driver transistor, which are connected in series. The equivalent circuit (see Fig. 3.2) of this series network represent a voltage divider on which the supply voltage (V_s) is applied, where V_s has to be positive for n-channel devices and negative for p-channel devices.

Therefore, the whole electrical behavior of the depletion-load inverter can be understood in terms of a simple voltage divider. One can characterize

the inverter by source and measure the V_{in} and measure the resulting V_{out}, which results in the so called inverter characteristics ($V_{out}(V_{in})$). A low level V_{in} should result in high level V_{out} and vice versa, to realize the NOT gate functionality. Moreover, the range of V_{in}, where V_{out} changes the voltage level, should be as small as possible.

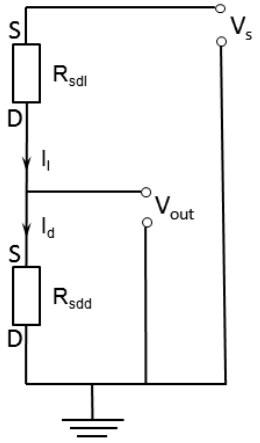

Figure 3.2: Equivalent circuit of the source-drain pathes of the load and the driver transistor, connected electrically in series. R_{sdl} is the resistance of the source-drain path of the load transistor, R_{sdd} is the resistance of the source-drain path of the driver transistor, V_s is the supply voltage, V_{out} is the voltage drop over R_{sdd}, I_l is source-drain current of the load transistor and I_d is the source-drain current of the driver transistor.

To get a better idea of the influences on the shape of $V_{out}(V_{in})$ the so called load-line method can be used.

3.2.2 Load-line method

In Fig. 3.3 an output characteristic family of the driver transistor is shown. Additionally, shown is one output characteristic of the load transistor, where V_{GSl} is set to zero volts, because source and gate of the load transistor are short-circuited. As one can see in Fig. 3.3 on the abscissa V_{out} is shown, which is the drain-source voltage (V_{DS}) of the driver transistor, but not V_{DS} of the load transistor. In fact, V_{DS} of the load transistor is $V_S - V_{out}$. Therefore, to illustrate the output characteristic of the load transistor ($I(V_S - V_{out})$) in the $I_D(V_{out})$ diagram of Fig. 3.3 in a correct way, one has to mirror the curve at the ordinate and afterwards one has to shift the $V_{DS} = 0\,\mathrm{V}$ point of the output curve by V_s in the direction of the abscissa as this is shown in Fig. 3.3.

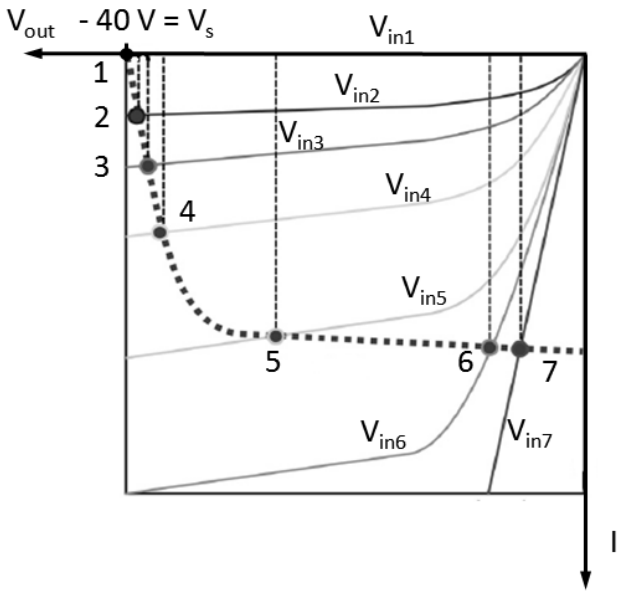

Figure 3.3: Load-line construction for a depletion load inverter. The solid lines show an output curve family of a driver transistor for different inverter input voltages V_{in}, where V_{in1} is larger than the threshold voltage of the driver transistor (V_{thd}) and the other V_{in} decreases with the index number. The dashed line shows an output characteristic of a load transistor, where V_{GSl} is set to zero (taken from Ref. [38] and modified).

Due to electrically connection of load and driver transistors, in this series network I_l and I_d (see Fig. 3.2) have to be the same (I), which is fulfilled at the crossing points of the curves in Fig. 3.3. Each crossing point shown in Fig. 3.3 defines one point of $V_{out}(V_{in})$. Beginning with high values of V_{in} results in low values of V_{out}. As one can see in Fig. 3.3, in this inverter characteristic region the load is in the linear region and the driver in cut-off region (crossing points 1 in Fig. 3.3). Due to decreasing V_{in}, the driver is in saturation (crossing points 2 in Fig. 3.3) and the load in linear region. Decreasing the value of V_{in} more and more results in a somewhat higher V_{out} (crossing points 3 and 4 in Fig. 3.3). At a certain point (crossing point 5 in Fig. 3.3), both transistors are in saturation. From now on, a huge change of V_{out} occurs by a minimal change of V_{in}. In the case of ideally saturated devices, this would result in a step function in the inverter characteristics. Therefore, to have a very low V_{in} range, in which V_{out} switches from high to low level, one has to use devices with well saturation behavior. Another decrease of V_{in} results in higher V_{out}. In this inverter region, the load transistor is in the saturation region and the driver transistor is in the linear region (crossing point 6 and 7 in Fig. 3.3).

As described above, to get proper inverter functionality one has to make sure, that it is possible for both devices to be in the necessarily regions, for example that it is possible for both devices to be in saturation region simultaneously. This is achieved by the adjustment of several inverter parameters to each other, which are V_{thl}, V_{thd}, V_s, R_{sdl} and R_{sdd}, where R_{sdl} is adjustable by the charge carrier mobility (μ), the channel length (L), the channel width (W) and the gate-dielectric capacitance per unit area (c_{ox}) of the load transistor. R_{sdd} one can adjust with the help of the corresponding parameters of the driver transistor and the values of V_{in}. (some aspects of this section are taken from Ref. [38])

Chapter 4

Organic Semiconductors

In the present work the prominent small molecules pentacene and 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) are used. For sake of completeness, additionally to the mentioned small molecules, also the prototype semiconducting polymer, in especially Poly(3-hexylthiophene) (P3HT), is discussed.

4.1 Pentacene

Pentacene is an oligoacene, which consists of 5 benzene rings. They are fused together linearly as shown in Fig. 4.1, resulting in a planar molecule with a π-conjugated system. The intramolecular charge transport is governed by the π electrons and, therefore, a good overlap of π-orbitals of different molecules is needed for good intermolecular charge transport [39].

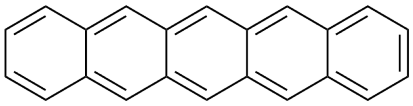

Figure 4.1: Chemical structure of Pentacene.

4.2 6,13-bis(triisopropylsilylethynyl)pentacene

TIPS-pentacene is a derivative of pentacene. Due to the side chain substituents, TIPS-pentacene is soluble and more stable [40].

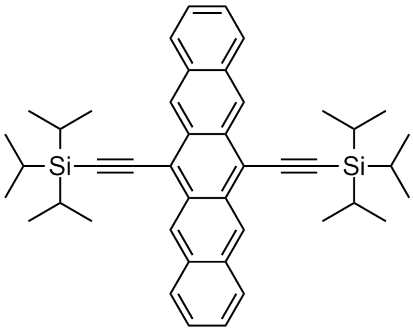

Figure 4.2: Chemical structure of 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene)

4.3 Poly(3-hexylthiophene)

P3HT consists of the monomer thiophene, which is substituted by a hexyl chain (C_6H_{13}) (see Fig. 4.3), resulting in a structure which is called 3-hexyl-thiophene.

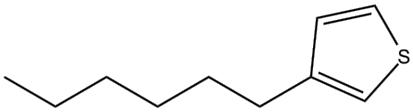

Figure 4.3: Chemical structure of 3-hexyl-thiophene.

One can connect the momonomers to polymers in different ways. The so called head-to-tail-head-to-tail (HT) arrangement, results in best electronic behavior [41] (Fig. 4.4). HT-P3HT is also called Poly(3-hexylthio- phene-2,5-diyl). Thereby, an important parameter is the so called regio-regularity. The HT regularity, or simple the regio-regularity measures in percent how many couplings of the polymer are HT one [41]. Usually HT-P3HT or Poly(3-hexylthio-phene-2,5-diyl) is called regioregular P3HT (rr-P3HT).

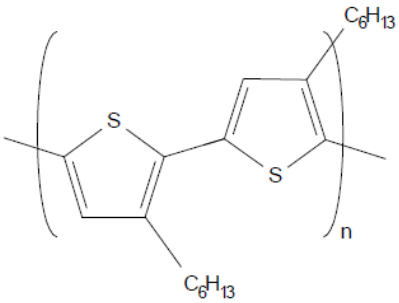

Figure 4.4: Chemical structure of head-to-tail-head-to-tail regioregular poly(3-hexylthiophene) (rr-P3HT).

Chapter 5

Self-assembled monolayers

'Self-assembled monolayers (SAMs) are highly ordered two-dimensional structures that form spontaneously on a variety of surfaces '[42]. There exist two important classical SAM classes, namely thiols on gold surfaces and organosilanes on silicon oxide (SiO_x) surfaces. Moreover, there exist a third important SAM class, called phosphonates [43]. In all cases, the molecules which form the SAM, consist of a surface and a head group [44]. Another name for the surface group is functional group, because it functionalizes the SAM molecule in a desired way. The head group is responsible for covalent bonding of the molecules to the substrate and, therefore, it is also called docking group. Between the functional and the docking group there is the so called molecular backbone.

In the following, the focus is on the growth process of SAMs which have trichlorosilane as docking group and which grow on SiO_x surfaces. This growth process is influenced by many different parameters, for example the kind of solvent used [45], the water content of the solvent [45], the temperature during SAM formation [46, 47, 48], and the substrate pretreatment [49]. For the latter, dry etching by oxygen plasma is a quite commonly used process [42, 44]. The oxygen plasma cleans the substrate and hydroxylates the SiO_x substrate surface, which means that there is a high amount of silanole (Si-OH) groups on the surface [44]. These groups are highly hydrophilic and, therefore, water (H_2O) is adsorbed leading to an hydrated surface. In our case the water originated from an ultrasonic bath in H_2O, which was done immediately after the plasma etching step. The involved steps during trichlorosilane SAM formation on SiO_x substrate surfaces are [44] (see Fig. 5.1):

Physisorption

The SAM molecules are physisorbed at the hydrated surface. It is important to start the SAM production immediately after the activation process. Additionally, adding the SAM molecules to the solution containing the substrates should be the last step to avoid polymerization of the SAM molecules.

Hydrolysis

The adsorbed H_2O molecules hydrolyze the SAM docking group into trihydroxysilane (-Si(OH_3)). Another reaction product is hydrochloric acid.

Covalent grafting to the substrate

The -Si(OH_3) groups starts to bonds covalently to hydroxyl groups (-OH) on the surface. Thereby also H_2O is formed.

In plane reticulation

The last step is the crosslinking to neighbor molecules. In an ideal case one silanol of the docking group bonds to one Si-OH group of the surface and the other two Si-OH groups bonds to neighbor SAM molecules. Typically, however, not every molecule even bond to the substrate. In this case the molecule bonds to the other molecules with all of the three bonding possibilities, results in thicker layers, than a monolayer.

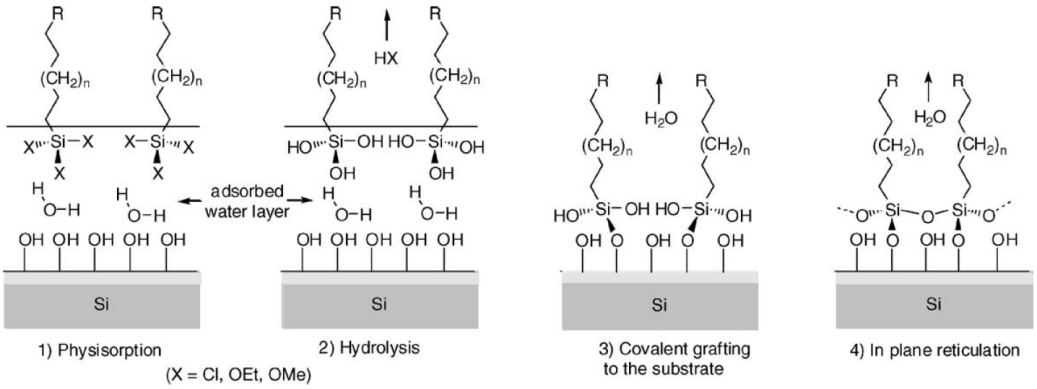

Figure 5.1: Involved steps for trichlorosilane SAM formation with alkyl chain ($(CH)_{2n}$) as molecular backbone, taken with permission from [44]. In the present case X is chlorine (Cl), resulting in trichlorosilane as docking group. As functional group R several different one were used.

Part II

Results

Chapter 6

Surface Proton Transfer Doping

6.1 Preamble

This chapter is published in physica status solidi (a), Volume 209, Issue 1, pages 181–192, January 2012, DOI: 10.1002/pssa.201127595 by Simon J. Ausserlechner, Manfred Gruber, Reinhold Hetzel, Heinz-Georg Flesch, Lukas Ladinig, Lucas Hauser, Anja Haase, Michael Buchner, Roland Resel, Ferdinand Schürrer, Barbara Stadlober, Gregor Trimmel, Karin Zojer and Egbert Zojer

My part of this work involves OTFT production without pentacene evaporation, contact angle measurements and hydrochloric acid exposure together with Lucas Hauser, Karl Fischer Titration together with Lucas Ladinig, ammonia exposure and the most of the electronic electronic measurements. Manfred Gruber, Michael Buchner, Karin Zojer and Ferdinand Schürrer are responsible for two-dimensional drift-diffusion based simulations. Reinhold Hetzl produced the 6,13-bis(triisopropylsilylethynyl)pentacene (Tips- pentacene) based devices and measured some of them. Additionally he is responsible for the $\Theta/2\Theta$ measurements together with Roland Resel. Heinz-Georg Flesch and Roland Resel are responsible for the x-ray reflectivity measurements. Anja Haase and Barbara Stadlober are responsible for atomic force microscopy and pentacene evaporation. Gregor Trimmel give input to the chemical structure of surface proton transfer doping. And Finally Egbert Zojer is responsible for quantum-mechanical simulations and is the major source of ideas concerning this paper.

6.2 Abstract

A number of studies show that chemical modification of the semiconductor-dielectric interface can be used to control the threshold voltage (V_{th}) of organic thin film transistors (OTFTs). A promising chemical functionality to achieve that are acidic groups, which - at the semiconductor-dielectric interface - have been used to realize chemically responsive OTFTs and easy to fabricate inverter structures. Especially for pentacene-based OTFTs, the underlying chemical and physical mechanisms behind the acid-induced V_{th} shifts are not yet fully understood. Their clarification is the topic of the present paper.

To distinguish between space-charge and dipole-induced effects, we study the impact of the thickness of the gate oxide on the device characteristics achieving maximum V_{th} shifts around 100 V. To elucidate the role of the acid, we compare the doping of pentacene by acidic interfacial layers with the impact of hydrochloric acid vapour and investigate the consequences of exposing devices to ammonia. Complementary experiments using 6,13-bis(triisopropylsilylethynyl)pentacene as active layer hint towards the central (6 and 13) carbon atoms being subject to the electrophilic attack by the acidic protons. They also prove that the observed V_{th} shifts in pentacene devices are indeed a consequence of the interaction between the acidic groups and the active material. The experimental device characterization is supported by drift-diffusion based device modelling, by quantum chemically simulations, as well as by contact angle, atomic force microscopy and x-ray reflectivity. The combination of the obtained results leads us to suggest proton transfer doping at the semiconductor-dielectric interface as the process responsible for the observed shift of V_{th}.

6.3 Introduction

The crucial role played by the semiconductor-dielectric interface has been demonstrated by a number of studies during the past few years [50, 51]. It, for example, influences charge-carrier trapping [13] and thin film growth [52]. This, in turn, determines device parameters like the carrier mobility (μ) [53, 54, 55] and the threshold voltage (V_{th}). From an application-oriented point of view, the control of V_{th} is necessary to realize low voltage operation organic electronics [56, 57], or to fabricate depletion-load inverters using only a single-type of semiconductor material [58, 5]. Beyond that, understanding processes affecting V_{th} is also of fundamental interest for understanding the operation mechanism of OTFTs.

The methods developed over the years to tune V_{th} via interface modifications include: UV [58], UV-ozone [59, 60], or oxygen plasma [60] treatment of the surface of the dielectric, changing the dielectric capacitance [61], inserting dipole-polarized [62] or polarizable layers [63, 64], or storing charges at the dielectric-semiconductor interface [65]. Of particular relevance for the present study is the use of functional self-assembled monolayers (SAMs) [66, 67, 68, 69, 70]. Their insertion between the gate dielectric and the organic semiconductor layer has been shown to give rise to V_{th} shifts of several ten volts. A number of underlying mechanisms for the shifts have been suggested. One is the formation of dipole layers when using polar SAMs that shift the potential of the semiconductor-dielectric interface [66, 67, 68, 70], where the charge carrier transport takes place [31]. The experimentally observed V_{th} shifts did, however, not necessarily match the expectations based on the 'dipole' model [66, 69]. Moreover, it was argued on the basis of a comparison between device characteristics and secondary electron emission spectroscopy experimentscite[55] that realistic molecular dipole moments would lead to V_{th} shifts of only a few volts. This notion has been supported by drift-diffusion based simulations [14].

Thus, a charge transfer between the organic semiconductor and the SAM has been suggested as an alternative explanation [66, 69]. This process is reminiscent of 'electronic' surface transfer doping [71, 72, 73, 74, 75], where the underlying chemical process is a redox reaction between the semiconductor and the SAM [71]. The model is based on the assumption that semiconductor-dielectric interfacial space charges can shift the flat band voltage (V_{fb}) and, therefore, V_{th}. This can be derived analytically [11, 12] or by numerical, drift-diffusion based simulations [14, 15, 76, 77] and has also been measured in OTFTs [65].

An analogous model has been proposed for OTFTs containing acidic SAMs using regioregular poly(3-hexyl-thiophene) (rr-P3HT) as the active layer. In such devices, the 'normally on' (depletion mode) operation of the devices has been explained by proton transfer from the acid to the polythiophene [78]. Such acid-base reactions are well-known in polymers [79] or oligomers [80]. Their impact on the device characteristics can be understood in the following way (for the sake of simplicity assuming a negligibly small voltage drop between source and drain in the explanation): When applying no voltage between gate and source (V_{GS}), the proton transfer induces mobile (vide infra) holes in the channel in analogy to the doping of the chemically related poly(3,4-ethylenedioxythiophene) (PEDOT) by protons of the acidic poly(styrenesulfonate) (PSS) [81]. The charge of these holes exactly compensates the (immobile) negative space charge layer originating from the acid residues. Applying a negative V_{GS} then results in the accumulation of more

holes, while a positive V_{GS} is needed to deplete the channel. One can view the situation also purely 'electrostatically': If the space-charge layer due to the acid residues was not compensated by holes, it would induce opposite charges in the gate electrode. This would result in a potential drop over the dielectric in analogy to the situation in a plate capacitor putting the channel at a significantly different potential than the gate. This gives rise to carrier accumulation in the channel [14] equivalent to what would happen, if a voltage equal to the potential drop over the gate dielectric had been applied to the gate in the absence of any space charges.

Such acidic interfacial layers hold high promise for tuning the functionality of organic electronic devices. They allow the fabrication of chemo-responsive OTFTs detecting the presence of bases like ammonia that compensate the acid doping [78, 82]. They can also be used for a controlled chemical tuning of V_{th} over more than 80 V in rr-P3HT based OTFTs containing acidic SAM [83]. Beyond that, some of us have recently used photo-acid polymers as interface modification layers to control the growth of organic layers [52] and to photo chemically tune V_{th} [5]. The latter paves the way for the straightforward photolithographic production of inverters and potentially also more complex electronic circuits. Beyond that, protons at the semiconductor-dielectric interface have been found to play a decisive role for the bias-stress in OTFTs [18, 20] and it has been suggested that their production upon bonding of silanes to SiO_x also impacts the device characteristics [84].

In several of the above examples, pentacene has been used as the active material. In contrast to the situation for P3HT, where the interaction with the acid can be viewed in analogy to doping in PEDOT/PSS (vide supra), for pentacene it is much less clear, what the actual processes are that result in threshold voltage shifts due to the presence of an acid at the interface between the dielectric and the semiconductor. Clarifying that is of distinct relevance and, therefore, the topic of the present paper. In particular, we will provide evidence (i) that the main origin of the acid-induced V_{th} shift is the formation of a space-charge layer at the interface, (ii) that the V_{th} shift is the result of an acid base reaction, (iii) that the pentacene molecules are involved in that reaction, (iv) that it is the central carbon atoms of the pentacene molecules (i.e., those at the 6 and 13 positions) that are subject to protonation and (v) that the protonation results in the formation of free holes. This is achieved by combining a number of experimental investigations on different types of OTFTs with drift-diffusion based device modelling and quantum-mechanical simulations.

6.4 Results and discussion

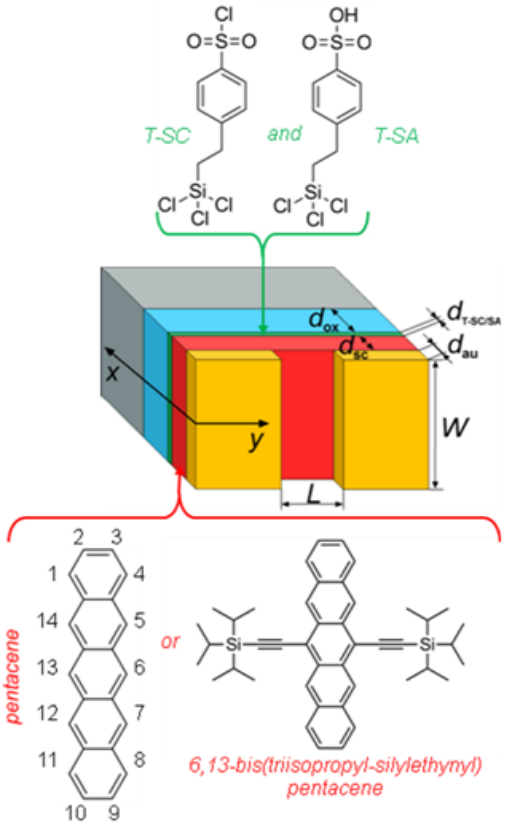

Figure 6.1: Schematic structure of the investigated top-contact bottom-gate device structure, with channel lengths of $L = 50\,\mu m$ or $L = 25\,\mu m$ and a channel width of $W = 7\,\text{mm}$. The orientation of the axes is such that a direct comparison with Fig. 6.5 showing the potential landscape is possible. The source and drain contacts are made of gold (Au) with a thickness of $d_{au} = 50\,\text{nm}$. The active layer material is either pentacene or 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) with a layer thickness of $d_{sc} = 35\,\text{nm}$ or $d_{sc} = 56\,\text{nm}$, respectively. The positions at which pentacene can be protonated are numbered to ease discussions later in the manuscript. The semiconductor-dielectric interface layer is a blend of the two functional trichlorosilanes, T-SC and T-SA, and its thickness is in the range of 1 nm ($d_{T-SC/SA}$). Thermally grown silicon oxides with thicknesses of $d_{\text{ox}} = 102.2\,\text{nm}$, $d_{\text{ox}} = 147.5\,\text{nm}$, $d_{\text{ox}} = 152.0\,\text{nm}$ and $d_{\text{ox}} = 245.0\,\text{nm}$ are used as the dielectric.

The schematic structure of the investigated devices is shown in Fig. 6.1.

We used pentacene and 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) as the active layer. The OTFTs were fabricated on doped silicon substrates with a SiO_x dielectric that has been modified using a blend of two functionalized trichlorosilanes namely 4-(2-(trichlorosilyl)ethyl)benzene-1-sulfonyl chloride (T-SC) and its sulfonic acid derivate 4-(2-(trichlorosilyl)-ethyl)benzenesulfonic acid (T-SA).

6.4.1 Varying the thickness of the oxide layer

To separate the effects of dipole and space-charge layers, we followed a suggestion from Ref. [14], where it has been shown that, when dipolar layers are responsible for the V_{th} shift, it should be independent of the capacitance per unit area (c_{ox}) of the gate dielectric. When caused by a space charge layer, V_{th} should, however, scale linearly with the inverse of c_{ox}. This can be simply understood when viewing gate electrode, dielectric, and channel as a plate capacitor (vide supra). For a given space charge, the potential drop in that capacitor and, thus (for a given gate potential) the potential of the channel is linearly proportional to the oxide thickness, d_{ox}. Therefore, we fabricated transistors with gate oxides of varying thickness.

Exemplary transfer characteristics of (Si|SiO_x|T-SC/SA|pentacene|Au) OTFTs on oxides with nominal thicknesses d_{ox-n} of 100 nm, 150 nm, and 250 nm are shown as solid squares in the three panels of Fig. 6.2.

In all devices, high, positive V_{th} are observed, which increase with d_{ox}. Prior to further analysing these data, the layer structures of the device shall be characterized in more detail. As a first step, the relevant layer thicknesses, d_{ox} and $d_{T-SC/SA}$ are determined by x-ray reflectivity (XRR) measurements. To obtain satisfactory agreement between measurements and fits (see Supporting Information 6.8), the T-SC/SA layers had to be modelled as a double layer structure, i.e. as consisting of two layers with different electron density. The obtained layer thicknesses (d), the surface root mean square (rms) roughness values (σ), and the refractive index decrements (δ) are summarized in Tab. 6.1.

The measured d_{ox} values deviate only slightly from the numbers provided by the wafer suppliers (i.e. d_{ox-n}). The $d_{T-SC/SA}$ values on the three substrates are virtually identical and in the range of what is expected for a monolayer, whose thickness has been calculated to be 0.96 nm [82]. This is insofar important as the wafers have been obtained from two different sources. We attribute the similar SAM growth to the substrate pretreatment (cf. Experimental section 8.4) and the carefully controlled growth conditions.

Also the contact angles of diodomethane (Θ_d) and deionized water (Θ_w) as well as the derived surface free energies per unit area (E_s) of the T-

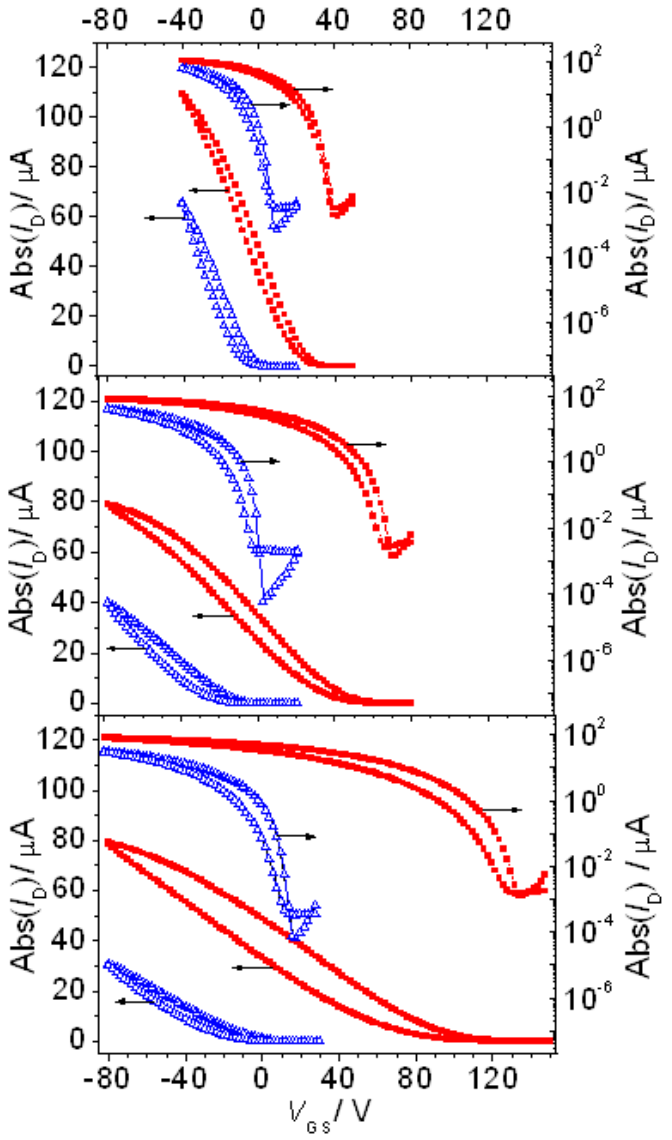

Figure 6.2: Exemplary transfer characteristics of pentacene based devices including a T-SC/SA semiconductor-dielectric interface layer with nominal (actual) oxide thicknesses of d_{ox-n} = 100 nm (d_{ox} = 102.2 nm), d_{ox-n} = 150 nm (d_{ox} = 147.5 nm), and d_{ox-n} = 250 nm (d_{ox} = 245.0 nm). Solid squares correspond to devices before and open triangles to devices after exposure to a flow of pure NH_3 gas. The source-drain voltage (V_{DS}) was set to -2 V. The increased hysteresis in the bottom plot is primarily a consequence of the extended measurement range. Further data are found in the Supporting Information 6.8.

Table 6.1: left: Thickness (d), root mean square roughness (σ) and refractive index decrement (δ) of the fitted 3-layer structure for the three different oxide thicknesses (d_{ox}); The net-thickness of the T-SC/SA layer, $d_{T-SC/SA}$, is given by the sum of $d_{T-SC/SA-1}$ and $d_{T-SC/SA-2}$. right: average water contact angles Θ_w, diiodomethane contact angles Θ_d, and surface free energies per unit area E_s . Average values obtained for two measurement series on separately prepared layers are reported (the full data set is contained in the Supporting Information 6.8).

d_{ox}	σ_{ox}	δ_{ox}	$d_{T-SC/SA-1}$ $d_{T-SC/SA-2}$	$\sigma_{T-SC/SA-1}$ $\sigma_{T-SC/SA-2}$	$\delta_{T-SC/SA-1}$ $\delta_{T-SC/SA-2}$	$d_{T-SC/SA}$	Θ_d	Θ_w	E_s
$[nm]$	$[nm]$	$[10^{-6}]$	$[nm]$	$[nm]$	$[10^{-6}]$	$[nm]$	$[°]$	$[°]$	$[\frac{mJ}{m^2}]$
102.2	0.46	73.0	0.7 0.3	0.10 0.24	36 46	1.0	35.5	62.0	52.6
147.5	0.43	73.0	0.7 0.3	0.10 0.24	36 46	1.0	36.4	65.9	50.3
245.0	0.48	73.0	0.7 0.4	0.10 0.25	36 46	1.1	37.3	66.2	49.9

SC/SA layers are in the same range for the three samples (see Tab. 6.1). Es is apparently largest for $d_{ox} = 102.2\,\text{nm}$, but the variations between the two measurement series (cf. Supporting Information) are in the same range as the differences between the substrates.

As far as pentacene growth on the T-SC/SA layers is concerned, we find similar 'over-all' morphologies on all substrates with the typical dentritic pentacene grain shape. The average grain size of the pentacene crystallites are, however, largest on the $d_{ox} = 102.2\,\text{nm}$ substrate, which has the largest E_s, as can be seen in the exemplary pictures in Fig. 6.3 (*cf.* Ref. [85, 86, 87]).

Having characterized the layers, we now turn to a more detailed evaluation of the transfer characteristics shown in Fig. 6.2. The obtained average values for the turn-on (V_{on}) and the threshold voltages, the calculated mobilities (μ), and the on-to-off ratios (I_{on}/I_{off}) are summarized in the top part of Tab. 6.2. These values have been extracted from the off-to-on sweeps at a drain-source voltage (V_{DS}) of $-2\,\text{V}$. A certain complication arises from the fact that there are a number of methods for determining V_{th} that do not necessarily yield equivalent values [33]. Therefore, we included the results obtained using the extrapolation in the linear region (ELR) [33], the second derivative method (SD) [33], and the logarithmic second derivative method (SDL) [33]. The

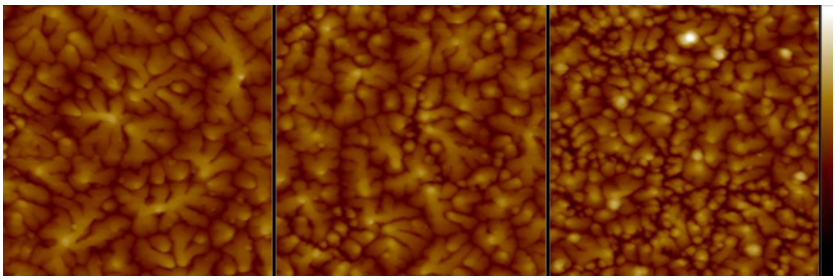

Figure 6.3: AFM images showing 5 μm x 5 μm sections of 35 nm thick pentacene layers grown on T-SC/SA covered SiO_x dielectrics with $d_{ox} = 102.2$ nm (left), 147.5 nm (center) and 245.0 nm (right).

corresponding threshold voltages are denoted as V_{ELR} and V_{SD} while V_{SDL} is associated with the turn-on voltage, as it corresponds to the point of highest curvature in the logarithmic plots of the transfer characteristics.

Table 6.2: Device parameters of (Si|SiO_x|T-SC/SA|pentacene|Au) transistors as function of different oxide thicknesses (d_{ox}) before (top part) and after NH_3 exposure (bottom part, *cf*, discussion in section 2.3). Threshold/onset voltages derived with different methods, V_{ELR}, V_{SD}, and V_{SDL} (details see main text), mobilities (μ) , and on-to-off ratios (I_{on}/I_{off}) are reported. I_{off} is defined as the drain current when the gate voltage equals V_{on} and I_{on} is the current for V_{GS} equaling $V_{on} - 40$ V. All values are average values over three different devices. A more detailed compilation of the measurement results can be found in the Supporting Information 6.8.

d_{ox} $[nm]$	c_{ox} $\left[\frac{nF}{cm^2}\right]$	V_{ELR} $[V]$	V_{SD} $[V]$	V_{SDL} $[V]$	μ $[\frac{cm^2}{Vs}]$	I_{on}/I_{off} $[10^3]$
102.2	34.8	20	25	38	0.24	30
147.5	23.0	39	44	65	0.12	20
245.0	14.1	90	98	136	0.13	2
d_{ox} $[nm]$	c_{ox} $\left[\frac{nF}{cm^2}\right]$	$V_{ELR-NH3}$ $[V]$	V_{SD-NH3} $[V]$	$V_{SDL-NH3}$ $[V]$	μ_{NH3} $[\frac{cm^2}{Vs}]$	$(I_{on}/I_{off})_{NH3}$ $[10^3]$
102.2	34.8	−5	1	8	0.22	60
147.5	23.0	−16	−9	3	0.11	90
245.0	14.1	−9	−3	20	0.12	40

In Ref. [33] the SD method, where V_{th} is associated with the maximum of the second derivative of I_D with respect to V_G, has been suggested for

extracting V_{th}. In a few of our devices, we, however, observe a relatively constant curvature of the transfer characteristics over a relatively wide voltage range in spite of the only very small applied V_{DS} of $-2\,\mathrm{V}$. We also often suffer from a relatively poor signal to noise ratio when calculating the numerical second derivative. In contrast, the ELR method can be readily applied and appears reasonable considering the relatively wide voltage range over which I_D depends linearly on V_{GS} (see Fig. 6.2). Also the reported μ values have been calculated for that region.

The devices with $d_{ox} = 147.5$ and $d_{ox} = 245.0\,\mathrm{nm}$ show similar μ. The latter nearly doubles for $d_{ox} = 102.2\,\mathrm{nm}$ consistent with the large size of the pentacene crystals (see Fig. 6.3) [52, 86, 88, 89]. As shown in Fig. 6.4, all extracted voltages increase close to linearly with d_{ox} and thus also with $1/c_{ox}$ [90]. From what has been discussed above, this indicates that the formation of a space-charge layer is the primary cause for the V_{th} shift. Interestingly, however, for all fitted lines we obtain an intercept with the V_{th}-axis at negative voltages of -32 V (ELR), -30 V (SD) and -35 V (SDL). The magnitude of this 'voltage offset' is clearly larger than the estimated standard deviation for the intercept of about 5 V extracted for the three fit functions. The fit to the V_{on} (equalling V_{SDL}) is, naturally, 'compromised' by the sub-threshold swing and the values of V_{ELR} and V_{SD} suffer from the ambiguity of the threshold-voltage determination. Nevertheless, this non-zero axis intercept suggests that part of the d_{ox}-dependent V_{th} shift arising from the space-charge layer is, as a secondary effect, compensated by a dipole layer.

This offset is significantly larger than what one would expect from the difference in work functions of the gate electrode and the semiconductor material. A certain contribution also comes from the intrinsic molecular dipoles of the T-SC/SA molecules that have been calculated to be a few Debye resulting in potential shifts of a few volts [78]. The bond-dipole due to the binding of the silanes to the dielectric surface should additionally somewhat influence the situation. All these effects can, however, not fully explain the magnitude of the dipole-induced shift. Possible origins of the necessary 'extra' dipole could be trapped protons that did not react with the pentacene (vide infra), or also trapped holes. Note that it follows from basic electrostatics that positive charges trapped above the negatively charged acid residues should not be considered as a space charge layer with a d_{ox}-dependent impact. As long as their density is smaller than that of the negatively charged acid residues they rather form a charged double layer (i.e. a dipole layer) with part of the negative charges from the acid residues. This makes their impact independent of d_{ox}.

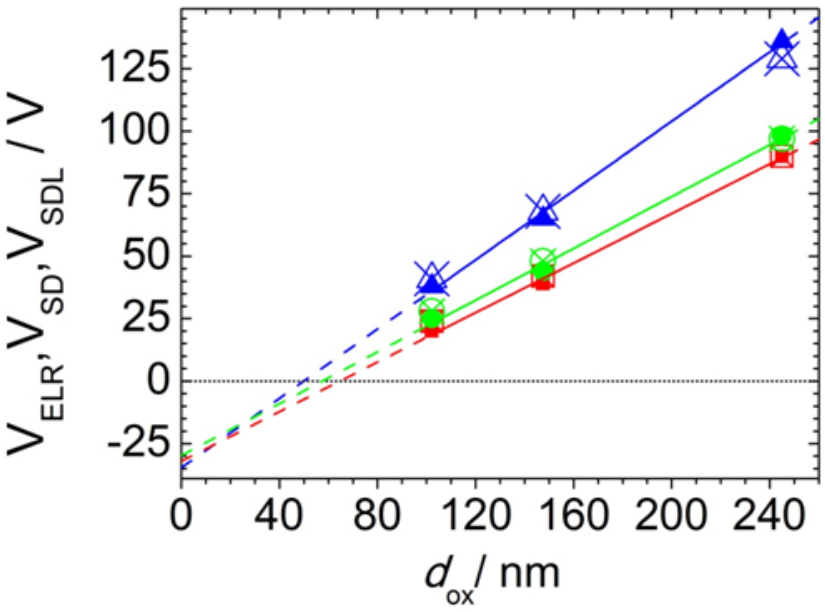

Figure 6.4: Dependence of V_{ELR} (solid squares), V_{SD} (solid circles) and V_{SDL} (solid triangles) on d_{ox} for devices with three different d_{ox}. The plotted solid symbols correspond to the average experimental values, the solid lines are linear fits and the open symbols have been extracted from the results of drift-diffusion based modelling. They have been obtained by applying the same procedures used for analysing the experimental data (see main text) also to the simulated transfer characteristics.

6.4.2 Results of drift-diffusion based device simulations

The above described situation is fully consistent with the results of drift-diffusion based simulations. Assuming an uncompensated negatively charged interfacial space charge layer with an areal space-charge density of -1.5 x $10^{17}\,\mathrm{em}^{-2}$ and a dipole layer with a dipole density corresponding to a potential jump of $-31\,\mathrm{V}$, the experimental trend for V_{th} can be fully reproduced (see open symbols in Fig. 6.4). The above space charge density corresponds to about 12 % of the acid groups being deprotonated assuming a molecular density at the interface of 1.3 * $10^{18}\,\mathrm{m}^{-2}$ (i.e., 1/3 of the molecular packing density of the SAM obtained when assuming a $25\,\mathrm{Å}^2$ footprint in this way accounting for the T-SC/T-SA ratio in the used sample)

To fully reproduce the measured transfer characteristics, a relatively complex model including different types of traps (to reproduce the sub-threshold swing and the hysteresis) as well as a mobility depending on d_{ox} to account for the different experimentally observed film morphologies needs to be em-

ployed. The results from these simulations have been used for the data in Fig. 6.4 and are contained in the Supporting Information 6.8. To understand the fundamental processes responsible for the V_{th} shifts, it is, however, advisable to discuss the situation within a simplified model, disregarding traps and assuming a constant mobility in all devices. The resulting potential distributions in the device at $V_{DS} = -2\,\mathrm{V}$ for the three d_{ox} values are shown in Fig. 6.5 (a).

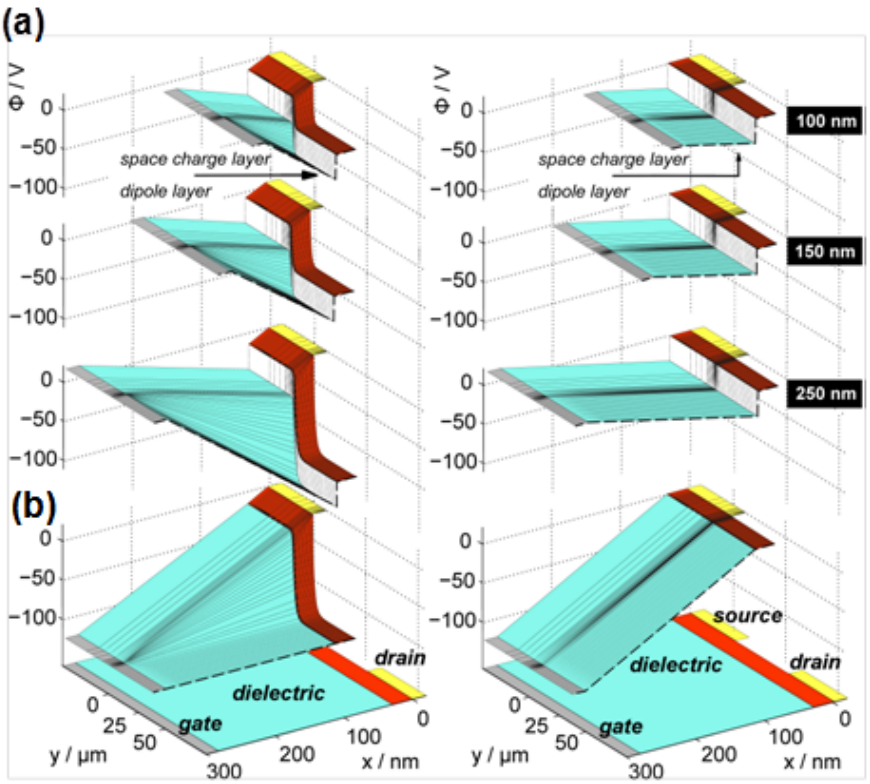

Figure 6.5: (a) Simulated potential distributions for devices with a fixed negative space charge layer and a fixed dipole layer at the semiconductor-dielectric interface for oxide layer thicknesses $d_{ox} = 100\,\mathrm{nm}$, 150 nm, 250 nm. Shown is the situation in the absence of mobile charges (left column) and for the steady state (right column) in the linear regime ($V_{DS} = -2\,\mathrm{V}$). The gate biases V_{GS} are chosen to induce the same total amount of accumulated charges in the steady state ($I_{DS} = 81\ \mu\mathrm{A}$) for all oxide thicknesses, ($V_{GS} = -12.5\,\mathrm{V}$, $-3.3\,\mathrm{V}$, and $15.3\,\mathrm{V}$). To prevent obscuring important details, we omit showing the potential in the "drain-region" of the device; the position of the corresponding cut in the profiles is indicated by a broken line.

The left panels depict the situation immediately after applying the volt-

ages, while the right panels show the steady-state situation. The gate bias V_{GS} is chosen such (i) that all devices operate in the linear regime and (ii) that the same total steady-state current (here arbitrarily set to $I_{DS} = 81\,\mu\text{A}$) is achieved for all oxide thicknesses. This corresponds to $V_{GS} = -12.5\,\text{V}$, $-3.3\,\text{V}$, and $15.3\,\text{V}$, for $d_{ox} = 100\,\text{nm}$, $150\,\text{nm}$, and $250\,\text{nm}$, respectively. Discussing a situation with $I_{DS} = \text{const}$ represents a more general situation than merely discussing the onset regimes. The latter, however, can be easily recovered by setting $I_{DS} = 0\,\text{A}$. Note that for $I_{DS} \neq 0$, the differences in the associated V_{GS} do not directly correspond to the offsets in V_{th}, as in the transfer characteristics also the slope of the $I_{DS}(V_{GS})$ curves is proportional to the capacitance of the dielectric (i.e., inversely proportional to d_{ox}).

To illustrate the impact of the space charge and dipole layers on the potential distribution, we first discuss the situation for the instant the external voltage is applied (i.e., before mobile charges are injected). In that case, gate, drain, and source electrodes are set to a fixed potential and no mobile charges are in the device. Without space charges or dipoles at the interface (see Fig. 6.5 (b)), the potential in the pentacene volume that is not covered by source or drain electrodes ($0 < y < 50\ \mu\text{m}$) assumes the value of the gate potential. This is a consequence of the huge aspect ratio of the considered transistors (channel length of $50\,\mu\text{m}$ vs. an overall thickness of the active region and dielectric between $135\,\text{nm}$ and $285\,\text{nm}$).[14] Further, the potential drops linearly from the source/drain electrodes to the gate electrode ($y \leq 0, 50\,\mu\text{m} \leq y$) with different slopes in the semiconductor and the dielectric as dictated by their dielectric constants.

The situation in the channel region not covered by the source- and drain electrodes is significantly modified in the presence of the interfacial space charges and dipole layers. Due to the space charge layer, there is an additional voltage drop across the dielectric layer (Fig. 6.5 (a), left panels). The corresponding electric field in the oxide layer is the same for all oxide thicknesses as a consequence of comparing situations with equivalent drain currents in the steady-state (vide supra). The extent of the potential drop increases linearly with d_{ox}, reminiscent of the situation in a plate capacitor. The potential step at the interface due to presence of the dipole layer partly counteracts the potential drop over the oxide. Since the height of this step is, however, solely determined by the dipole density, it is independent of d_{ox}.

Underneath the source and drain electrodes, a different situation is encountered: Here, the total potential difference is given by V_{GS} and VGD, respectively. As a consequence, there is a potential drop over the pentacene layer (unlike in the channel region far from source and drain described in the previous paragraph). For the three situations depicted in Fig. 6.5 (a), this potential drop is independent of d_{ox}. This follows from the requirement that

for the steady state all drain currents are identical. The same requirement explains why also the field in the oxide does not depend on d_{ox}. This then results in the observed d_{ox} dependent potential drop over the oxide that is offset by the potential discontinuity due to the dipole layer.

For reaching the steady state (Fig. 6.5 (a), right panels), charges are injected from the source electrode and accumulate in the channel region. As a consequence, in the regions underneath the contacts the potential in the pentacene layer is fixed to the source and drain potentials. I.e., there is neither a field in the x- nor in the y-directions. Also in the part of the device not covered by the electrodes, the field in the x-direction vanishes, but there is a steady potential drop in the y-direction as a consequence of the applied V_{DS} (as the latter is chosen to be only $-2\,\mathrm{V}$ here, this potential drop is, however, not well resolved in Fig. 6.5). Because we compare the situation of identical I_{DS}, the accumulated hole density at the semiconductor/dielectric interface is the same for all d_{ox}, which also renders the field in the oxide identical.

6.4.3 Dedoping by ammonia and bulk doping using hydrochloric acid

To determine, whether the V_{th} shift is a consequence of an acid-base reaction, we performed two test experiments: First, we exposed the devices containing the T-SC/SA layers to a base as the latter should neutralize the acid; for that purpose we chose NH_3 gas and exposed the devices for 30 min to ensure that an equilibrium situation is established (details see Experimental section 8.4 and Supporting Information 6.8). This exposure results in a substantial shift of V_{th} to less positive values with the total shift being essentially proportional to d_{ox} (see Fig. 6.2). As a result, the V_{th} values of all devices after NH_3 exposure become similar. In analogy to what has been described in [78, 82] for P3HT based devices, this shift can be explained by a neutralization of the acidic groups of the T-SA molecules by NH_3 resulting in the formation of the electronically inactive ammonium 4-(2-(trichlorosilyl)ethyl)benzenesulfonate as shown for pristine T-SC/SA layers by various spectroscopic techniques [82]. Interestingly, the I_{off} are in the same range before and after NH_3 exposure [91].

In a second test experiment, we exposed (Si|SiO_x|pentacene|Au) devices, i.e., devices not containing a T-SC/SA interfacial layer, to HCl gas. The resulting device characteristics are shown in Fig. 6.6.

Very much like in the devices containing an acidic interfacial layer, exposure of 'conventional' (Si|SiOx|pentacene|Au) transistors to HCl vapor results in highly positive V_{th} and V_{on}. This shift to positive V_{th} is stable over days

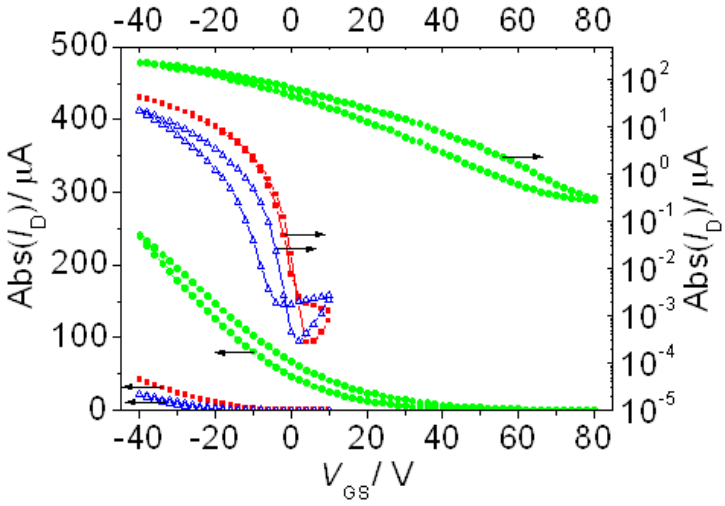

Figure 6.6: Transfer characteristics of an exemplary (Si|SiO_x|pentacene|Au) device with $d_{ox} = 152.0\,\text{nm}$ (solid squares), after exposure to HCl vapour (solid circles) and after subsequent exposure to NH_3 (open triangles). V_{DS} is set to $-2\,\text{V}$. Further data are found in the Supporting Information 6.8.

when keeping the devices in an Ar-glove box, which indicates a strong chemical interaction between pentacene and the HCl molecules, because otherwise HCl would gradually diffuse out of the device. The fact that again V_{on} can be shifted back to around zero upon exposure of the device to NH_3 gas (see open triangles in Fig. 6.6) shows that also here we are dealing with acid-base reactions. This is consistent with the notion that bulk doping of the active layer material shifts V_{th} as derived on the basis of analytic equations [11, 12, 15] and by drift-diffusion based simulations [14, 76, 77].

Thus, we propose a protonation of some of the pentacene molecules in the active layer upon interaction with a strong enough acid (HCl vapour or the T-SC/SA interface layer). Protonation of pentacene molecules in the gas phase has, indeed, been suggested by quantum chemical simulations [92, 93] and by several different experimentally measurements, namely by Fourier transform ion cyclotron resonance mass spectrometry [92], IR and IR multiple-photon dissociation spectroscopy [94]. The experiments presented here are a strong indication that analogous reactions occur also in the solid state.

Interestingly, the exposure to HCl vapour in several of the investigated devices resulted in a deterioration of the I_{on}/I_{off} ratio as a consequence of a significant increase of I_{off}. This is in clear contrast to the insertion of the T-SC/SA layer as shown in Fig. 6.2. It should, however, be mentioned that the measured values of I_{off} upon exposure to HCl display a significant

device-to-device variation as shown in the Supporting Information 6.8.

A possible explanation for the increased I_{off} in Fig. 6.6 is that exposure to HCl vapor induces proton-transfer doping throughout the whole film, while it is reasonable to assume that the use of an interfacial layer (like T-SC/SA) primarily affects the region close to the semiconductor-dielectric interface. In literature [95] it has indeed been suggested that bulk doping results in an increased off current. This, is, however, cast into doubt by Refs. [76, 77], where it is argued that such an increase of I_{off} is a consequence of traps, while bulk doping without trap creation (albeit at a much lower concentration than in [89]) only results in a shift of V_{th}.

6.4.4 Acid-base reactions in TIPS-pentacene based devices

To clarify, which part of the pentacene molecule is actually affected by the protons of the acid, it is useful to consider the proton affinity (PA) of the various carbon positions. Calculations in Ref. [92, 93] indicate that the two carbon atoms of the central ring in pentacene have the highest PA. Our quantum-chemical simulations at the B3LYP/6-31G(d,p) level indeed confirm that the protonation of pentacene at the central 6 position is energetically favoured by 0.87 eV (resp. 0.74 eV and 0.15 eV) over a protonation at the 3 (resp. 4 and 5) positions (the numbering of the carbon atoms in the pentacene backbone is included in Fig. 6.1).

To test experimentally, whether this is the case also in the solid state, we performed comparative studies using a suitably modified pentacene derivative as the active semiconductor material: In TIPS-pentacene (chemical structure see Fig. 6.1), the central two carbon atoms of pentacene are substituted by triisopropyl(prop-1-yn-1-yl)silane, which can be expected to very significantly modify their proton affinity. Indeed, already when fully optimizing the structure of a protonated TIPS-pentacene molecule (corresponding to the gas phase), the energetic 'advantage' of the 6 over the 3 position is reduced to 0.48 eV (0.37 eV for the 4 position; protonation at the 5 position is, in fact, energetically favoured here by 0.25 eV). Moreover, primarily due to a change in hybridisation of the protonated carbon atom, the structure of the molecule is heavily distorted as shown in the Supporting Information 6.8. Such a distortion will not happen in the solid state, especially in a highly crystalline [40], densely packed layer. Thus, we also calculated the total energy of a protonated TIPS-pentacene molecule, in which the central part of the backbone was forced to remain planar. In this case, protonation at the central carbon atom becomes energetically more costly by 0.37 eV (resp.,

0.48 eV and 1.10 eV) than protonation at the 3 (resp. 4 and 5) positions. These data shows that due to the substitution protonation at the central carbon atoms can be excluded in a TIPS-pentacene film.

Thus, if the above described high positive V_{th} upon insertion of a T-SC/SA layer or exposure to HCl vapor were, indeed, the consequence of a protonation of the central pentacene carbon atoms, they should not occur when using TIPS-pentacene as the active material. This is exactly what we observe in the corresponding test experiments, where neither the inclusion of a T-SC/SA layer nor the exposure to HCl vapor gives rise to any shift in V_{th} (for transfer characteristics see the Supporting Information 6.8). This can be considered as convincing evidence that (i) the acid-induced V_{th} shifts in pentacene-based devices are a consequence of a chemical reaction between the acid and the active material and not, e.g., due to an interaction with silanole surface groups or related species; and that (ii) the position of protonation in pentacene is at the central carbon atom.

6.4.5 The suggested mechanism for surface proton transfer doping in pentacene based OTFTs

The above results lead us to suggest the mechanism depicted in Fig. 6.7 for surface proton transfer doping in pentacene based OTFTs: A fraction of the pentacene molecules close to the interface with the T-SC/SA layer are protonated. This fraction remains relatively small, as can be inferred from the drift-diffusion based modelling (vide supra). Such a situation is consistent with the protonation being an endothermal process rendering the reaction entropy-driven. The positive charge on the pentacene molecule originating from the proton transfer is then transferred to a neighbouring molecule. This is necessary to explain the experiments, as otherwise one would be dealing with trapped rather than mobile holes as a result of the proton-transfer doping process.

It is also consistent with our quantum-chemical simulations, as the charge transfer to a non-protonated pentacene results in an energy gain of 0.60 eV. This value is obtained from the comparison of the B3LYP/6-31G(d,p) calculated ionization potentials of pentacene and the pentacene-6-ylium with an additional proton at the central position (for chemically structure see Fig. 6.7) and assumes equivalent screening in both systems. The reason for the increased ionization potential of the molecule bearing the extra proton is the disrupted conjugation by the central sp^3 hybridized carbon atom. As a consequence, pentacene-6-ylium molecules will no longer participate in the hole transport at the interface, but they will also not act as traps. Thus, the

carrier mobility should not be reduced by the protonation of a small fraction of the pentacene molecules, which is again consistent with the experiments. Considering the increased reactivity of pentacene-6-ylium molecules in situation (c) of Fig. 6.7 due to their radical character, it cannot be excluded that these molecules are actually subject to a second protonation process, but we have no clear evidence for this to actually happen.

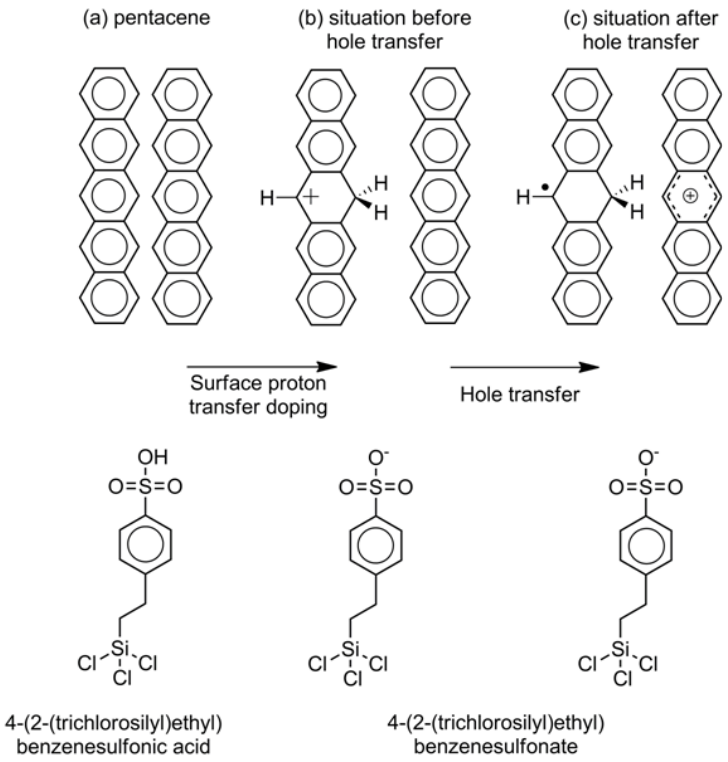

Figure 6.7: Suggested mechanism for surface proton transfer doping of pentacene by the protons of the sulfonic acid functionalities of the T-SA molecules. (a) shows the situation before doping. (b) shows a protonated pentacene molecule (pentacene-6-ylium); the resulted disruption of the conjugation results in the positive charge being transferred to a neighbouring molecule, forming a free hole (c).

6.4.6 Establishing equilibrium and the role of ambient light

Finally, it should be noted that the high positive V_{th} values induced by a T-SC/SA layer and depicted in Fig. 6.2 develop only gradually. I.e., for devices

stored in the glove-box in light (i.e., without any intentional darkening), it takes several days until a stable situation is reached that also does not change under the measurement conditions described below. In contrast, the equilibrium is established instantaneously, when performing the doping experiments using HCl vapour. This can be attributed to the abundance of HCl molecules when exposing the devices to HCl vapour. Interestingly, we saw immediate doping also when using two types of polymeric interfacial layers that consist of photo acids [5]. We attribute this to the fact that in these experiments, to form the acids, we illuminate the samples by UV-light and it is known for several organic systems that their acidity is much higher, when the molecules are in the excited state [96, 97, 98, 99].

In fact, also for doping with a T-SC/SA interfacial layer, the exposure to light impacts the steady-state situation. When storing a device in darkness for a month right after fabrication, the achieved positive V_{th} were clearly smaller than in a control device stored under ambient light. When the latter device is then kept in darkness for several days, its V_{th} shifts back to the value measured for the device never exposed to ambient light. This could be a consequence of a shift in the chemical equilibrium of the reactions depicted in Fig. 6.7 upon illumination.

On the other hand, a 'darkness-induced' shift of V_{th} to more negative values is reminiscent of the experiments by Jing et al., who observed (albeit for P3HT based devices on bare SiO_x, i.e., without any interface modifications) threshold voltages as low as -60 V when storing their devices in the dark [100], which can be attributed to charge-carrier trapping. In that spirit, it cannot be excluded that the less positive values of V_{th} for T-SC/SA containing pentacene devices stored in the dark are due to a partial cancellation of the doping effect by charge carrier trapping rather than a result of a shifted chemical equilibrium. To definitely answer such questions, extensive tests of the impact of light (of different wavelength) on various types of transistors containing different interface modifications and active layer materials will be necessary. This goes clearly beyond the scope of the present paper.

6.5 Conclusions

Combining a number of experiments with drift-diffusion based device modelling and quantum-chemical calculations, we study the mechanism responsible for the high positive threshold voltages observed in pentacene based OTFTs, where the active layer is in contact with an acid. This is of relevance as, for example, devices containing acidic layers have a high potential for realizing chemically responsive devices [101] and allow for an efficient

photochemical production of depletion-load inverters [5]. The focus of the present study lies on pentacene transistors containing acidic monolayers covalently bonded to the gate dielectric. The theoretical and experimental investigation of the dependence of the monolayer-induced threshold-voltage shift on the thickness of the gate dielectric reveals that it is due to the formation of an interfacial space-charge layer partially compensated by the formation of a dipole layer. The fact that a similar effect can be realized by HCl exposure of devices not containing an acidic layer and the finding that the V_{th} shift can be eliminated by exposing the devices to a base (in our case NH_3) show that the observed doping is the consequence of an acid/base reaction. Interestingly, none of the above effects is observed when replacing pentacene by TIPS-pentacene. This, on the one hand, proves that it is the interaction between the acid and the active material that is responsible for the V_{th} shift and, on the other hand, points to the central two carbon atoms of pentacene being subject to the electrophilic attack by the protons. It also implies that whether or not a certain semiconductor is prone to protonation (and, thus, useful for the above mentioned applications), subtly depends on the proton affinity of the available docking sites. These data together with results of quantum-chemical simulations finally allow suggesting the chemical and electronic mechanism sketched in Fig. 6.7 for surface proton transfer doping in pentacene based OTFTs.

6.6 Experimental

As especially the growth of the T-SC/SA layers is impacted severely by the very details of the fabrication process (especially by minute changes of the water concentration during film growth), we considered it appropriate to provide a very detailed description of the applied methodologies. Due to space limitations, they are, however, largely contained in the Supporting Information 6.8.

Device fabrication: As substrates (serving also as gate electrodes), we used doped silicon wafers with thermally grown oxides with thicknesses $d_{ox} = 102.2\,\text{nm}$, $d_{ox} = 147.5\,\text{nm}$, $d_{ox} = 152.0\,\text{nm}$, and $d_{ox} = 245.0\,\text{nm}$ pre-cut into 2 cm x 2 cm pieces supplied by Siegert Consulting and Silchem. The oxide surfaces of the substrates were cleaned and activated by an oxygen plasma etching process and subsequently sonicated for 2 min in deionized water. This rendered the oxide surfaces of all samples highly hydrophilic lowering the contact angle of H_2O to below 10°, the limit of our contact-angle measurement set-up. This is important as the resulting high concentration of -OH groups on the waver surface is beneficial for the docking of silanes [44].

As a next step, T-SC/SA layers were grown on the majority of the wafers as described below. The active layer material pentacene was deposited under high-vacuum conditions typically some days after growing the T-SC/SA layer. The first 5 nm were deposited at a rate of 0.02 Å/s and the following 30 nm at a rate of 0.1 Å /s, as measured with a quartz microbalance. During pentacene-growth, the substrates were held at a temperature of 65 °C. Alternatively, TIPS-pentacene films were deposited from a 1 t % solution in toluene by spin coating in air with the substrate heated to 60 °C using an IR lamp (spin parameters set to: 2000 rpm for 18s and 4000 rpm for 20 s). The ca. 50 nm thick gold source and drain electrodes were produced at a pressure in the range of 10^{-6} mbar in a home-built evaporation set-up operated inside an Ar glove-box. Four transistors were fabricated on each substrate.

Growth of the T-SC/SA layer: After the plasma etching process and the water sonication, the substrates were further cleaned in several steps (cf. Supporting Information 6.8) and put into 10 ml highly dry toluene (water content of about 7 ppm measured with Karl Fischer Titration) inside an Ar glove-box. To that we added 10 μl of the commercial T-SC/SA solution from ABCR, which is a 50 vol % mixture of T-SC/SA molecules and toluene and let the layer grow for 16 h. After this time, the substrates were sonicated and rinsed in fresh toluene. Finally, they were annealed for 30 min at about 100 °C at a pressure of about 0.6 mbar.

The *XRR data* were recorded on a Bruker D8 Discover diffractometer using CuK_α-radiation and analyzed using WinGixa [102], which is an implementation of Parratt' s recursive algorithm [103]. It includes interface, σ_{ox}, and surface roughness, $d_{T-SC/SA}$, according to the approach of Nevot and Croce [104]. *Contact angles* were measured with a Kruess DSA 100 drop shape analysis system using deionized water and diiodomethane as test liquids. Based on the method by Owens Wendt [105] the surface free energy per unit area E_s of the T-SC/SA layers were calculated automatically. *AFM pictures* were measured with a Veeco Dimension DI3000 in tapping mode with standard silicon tips.

To *expose the devices to NH_3 gas*, we put our devices in a homemade measurement cell and flooded the cell with NH_3 gas for either 30 min (data in Fig. 6.2) or 1 min (data in Fig. 6.6). After the NH_3 exposure, we flooded the cell with argon gas until we could not detect ammonia at the gas outlet of the measurement cell. For HCl-vapor exposure, we put the ready-made devices over a beaker filled with fuming hydrochloric acid for 1 min. *Hazard warning! NH_3 is highly toxic and HCl vapor is very acidic; thus, experiments should always be performed in a fume hood using appropriate gloves and protective glasses!*

Source meter measurements: To measure the electronic characteristics of

the transistors, we used a Keithley 2636A dual source-meter controlled with a home-made software. We started the transfer sweeps at positive gate bias, reduced V_{GS} in steps of $-2\,\mathrm{V}$ (setting the delay time to 0.1 s). The reported device parameters were always determined for the sweep from positive to negative V_{GS}. All measurements were performed under ambient light inside a glove box.

Drift-diffusion based modeling: The numerical model to describe device characteristics is a two-dimensional drift-diffusion approach as described in Ref. [14] with special boundary conditions at the source and drain electrodes. Charge carrier injection occurs via thermionic emission and tunnelling through a potential barrier (given by the image charge model) in the Wenzel-Kramers-Brillouin approximation and is corrected by an interface recombination current [106]. The corresponding system of equations with appropriate boundary conditions is solved self-consistently on a non-regular two-dimensional grid [14][25] using an implicit time integration. A hole injection barrier of 0.47 eV [107] and dielectric constants of $\epsilon = 3.4$ (pentacene) and $\epsilon = 3.9$ (SiO_x) are assumed. To model interfacial charge and dipole layers areal charge distributions with fixed densities were used. To further account for the shapes of the I-V curves obtained in the experiments also two types of traps need to be considered: (i) The occurrence of a hysteresis is simulated by including bulk traps, whose occupation is determined self-consistently for each time step. (ii) To account for the shape of the transfer-characteristics in the sub-threshold region, additional interface traps with significantly shorter time constants are incorporated. Considerably more details on these simulations are contained in the Supporting Information 6.8.

Quantum-mechanical modelling The quantum-mechanical calculations were performed using Gaussian03 [108] applying the B3LYP [109] hybrid functional and a 6-31G(d,p) basis set. Total energies were extracted from the last step in the geometry optimizations. Note that we encountered serious convergence problems, when optimizing the geometry of planarized TIPS-pentacene protonated at one of the central C-atoms. The way we circumvented these problems is described in the Supporting Information 6.8.

6.7 Acknowledgements

We thank A. Fian for growing the pentacene films of the transistors exposed to HCl vapour, H. Brandner for reproducing the findings of Ref. [100], and Christian Slugovc as well as Thomas Grießer for stimulating discussions. Financial support by the Austrian Science Fund (FWF) (P 19959-N20) is acknowledged. Supporting Information is available online from Wiley Inter-

Science or from the authors.

6.8 Supporting information

As especially the growth of the T-SC/SA layers is impacted severely by the very details of the fabrication process (especially by minute changes of the water concentration during film growth), we considered it appropriate to provide a relatively detailed description of the applied methodologies.

Device fabrication

(this is a significantly extended version of the description in the main manuscript) As substrates (serving also as gate electrodes), we used doped silicon wafers with thermally grown oxides with thicknesses $d_{ox} = 102.2\,\text{nm}$, $d_{ox} = 147.5\,\text{nm}$, $d_{ox} = 152.0\,\text{nm}$, and $d_{ox} = 245.0\,\text{nm}$ pre-cut into 2 cm x 2 cm pieces. Which of the oxides has been used in a certain experiment is specified in the figure captions in the main text.

The waver with $d_{ox} = 102.2\,\text{nm}$ was boron doped (company: Silchem) and supplied with a plastic coating on the oxide for protection. To remove this plastic coating, we cleaned them in an ultrasonic bath in ultra-pure water for 2 min, cleaned it with a cleaning liquid (Photonic Cleaning Technology, type: First Contact) that was first brushed onto the waver and then left to dry for ca. 15 minutes. The resulting film was then removed by ultrasonic treatment in ultra-pure water produced with a cleaning system (company: Millipore, type: Simplicity 185; and the resulting specific resistance was in the range of MΩcm) for 2 min. Finally we dried the substrates with carbon dioxide gas. The other wavers were phosphorus doped (company: Siegert Consulting) and were delivered without any coating on the oxide.

As a next step, all substrates were cleaned in a CO_2 gas stream and, finally, the oxide surfaces of the substrates were cleaned and activated by an oxygen plasma etching process using a commercial set-up (company: diener electronic, type: Femto). First the plasma etching chamber was evacuated with a scroll pump (company: Varian, type: SH110) to a pressure of 0.2 mbar. In this context it should be mentioned that the use of an oil-free pump (like a scroll pump) is advantageous, as in XPS experiments performed to study the composition of the wafer surface after the plasma etching step, we found fluorine on the SiO_x surface when using a rotary vane pump most likely due to decomposed pump oil. Subsequently, the chamber was flooded with oxygen (company: Air Liquide, type: Alphagaz oxygen) setting the flow-meter to a value of 90 at an (over) pressure of 2.5 bar. Before starting the plasma

etching process, we then waited until the pressure inside the chamber silized at 0.3 mbar. The frequency of the high frequency generator was 40 kHz and we performed the plasma etching at a power of 100 W for 30 s. After the plasma etching process and the water sonication, the substrates were again cleaned with CO_2 gas.

Afterwards, we put them into cleaned glass containers (for a detailed description of the cleaning procedure see below) filled with ultra-pure water, did an ultrasonic treatment for 2 min and left them inside the bottles for about 25 min. This rendered the oxide surfaces of all samples highly hydrophilic lowering the contact angle of H_2O to below 10 °, the limit of our contact-angle measurement set-up (vide infra). This is insofar important as (i) before the plasma etching the contact angles of the different wafer batches differed considerably and (ii) the resulting high concentration of -OH groups on the waver surface is beneficial for the docking of silanes when growing the functional monolayers.

Meanwhile, other glass containers (which we had been held at 80 °C least over night) to be used for T-SC/SA layer growth were transferred into the glove box while still being hot. Note: We observed increased thicknesses of the T-SC/SA layers when transferring cooled down glass containers, presumably due to the adsorbed water at the inner walls of the containers, as minute amounts of water significantly impact the layer growth. Inside the glove box (H_2O and O_2 concentration < 1 ppm), each of the substrates was put into a separate glass containers that was filled with 10 ml highly dry toluene (water content of about 7 ppm measured with Karl Fischer Titration). To that we added 10 μl of the T-SC/SA solution, which is a 50 vol % mixture of T-SC/SA molecules and toluene (company: ABCR, product number: AB129108) and let the layer grow for 16 h. After this time, we put the substrates into glass containers with 6 ml fresh highly dry toluene, sealed the containers, transferred them out of the box, sonicated them for 2 min, and rinsed them with fresh toluene (company: Sigma-Aldrich, product number: 34866). This toluene had a water content of about 29 ppm measured with Karl Fischer Titration. Then we dried the samples using CO_2 gas and annealed them for 30 min at about 100 °C at a pressure of about 0.6 mbar. Between the annealing process and pentacene evaporation as well as between pentacene evaporation and gold deposition the substrates were in air and exposed to light for several hours.

The active layer material pentacene (company: tokyo chemical industry, product number: P0030) was vacuum deposited under high-vacuum conditions (base-pressure in the range of 10^{-6} mbar typically some days after growing the T-SC/SA layer. The first 5 nm were deposited at a rate of 0.02 Å/s and the following 30 nm at a rate of 0.1 Å /s, as measured with a

quartz microbalance. During pentacene-growth, the substrates were held at a temperature of 60 °C. Alternatively, TIPS-pentacene films were deposited from a 1 wt % solution of TIPS-pentacene (company: Sigma-Aldrich, product number: 716006-1G) in toluene (company: Sigma-Aldrich, product number: 34866). The films were fabricated by spin coating (company: Chemat Technology, type: KW-4A) in air with the substrate heated to 60 °C using an IR lamp (spin parameters set to: 2000 rpm for 18 s and 4000 rpm for 20 s). The 50 nm thick (measured with a quartz microbalance) gold (company: Oegussa, quality: fine gold plate) source and drain electrodes were produced at a pressure in the range of 10^{-6} mbar in a home-built evaporation set-up operated inside an Ar glove-box. For technical reasons, the manometer had to be located outside the glove box, i.e., close to the turbomolecular pump. Four transistors were fabricated on each substrate.

Cleaning process for glass containers used to grow T-SC/SA layers

(as mentioned above, the 'state' of the glass bottles has a distinct influence on the growth of the T-SC/SA layer)We always cleaned 19 glass containers (company: Bartelt, product number: 9.072 303) with 32 ml Hellmanex (company: Hellma, product number: 9-307-010-507) in 1.6 l deionized water with an ultrasonic bath for 25 min. Then we emptied the bucket containing the glasses, refilled it with deionized water, emptied every single glass container, cleaned the bucket with deionized water, put the glass containers back into the bucket and filled it with deionized water until the glass containers were covered with water. Now we did the ultrasonic treatment for 7 min and repeated the whole process two times, but without the bucket cleaning step. As a final cleaning step, every glass bottle was rinsed with ultra-pure water and stored in an oven at 80 °C at least overnight. The ultra-pure water was produced with a cleaning system (company: Millipore, type: Simplicity 185) and the resulting specific resistance was in the range of MΩcm.

Details on the chosen measurement procedure

Before measuring the device characteristics, the pentacene layer around the source and drain areas of the four devices located on each substrate is mechanically removed. This reduces the apparent gate current by up to two orders of magnitude in our common gate devices. To measure the electronic characteristics of the transistors, we used a Keithley 2636A dual source-meter controlled with a home-made software. We started the transfer sweeps at positive gate bias, reduced V_{GS} in steps of -2 V, setting the delay time, which is the time between applying V_{GS} and the measurement of I_D, to 0.1 s. It

should, however, be noted that this is not in all cases the actual time between two measurement, because the integration time for every measurement point is set automatically by Keithley firmware to obtain a sufficient signal to noise ratio. Therefore, at very small currents, significantly increased measurement times were applied. V_{GS} was decreased until we reached the most negative reported gate bias (set to a value that did depend on V_{th}). Then V_{GS} was again increased to the highest positive value reported in the figures. The given device parameters were always determined for the sweep from positive to negative V_{GS}. V_{DS} was $-2\,\mathrm{V}$ for the data reported in Fig. 6.8 and Fig. 6.10, and -60 V for the data in Fig. 6.11. The very low V_{SD} in the first case was chosen to maximize the linear region for data extraction, while in the TIPS-pentacene devices we applied a larger V_{DS} to avoid too small currents. All measurements were performed under ambient light inside a glove box.

Additional data for oxide thickness depended transfer curves

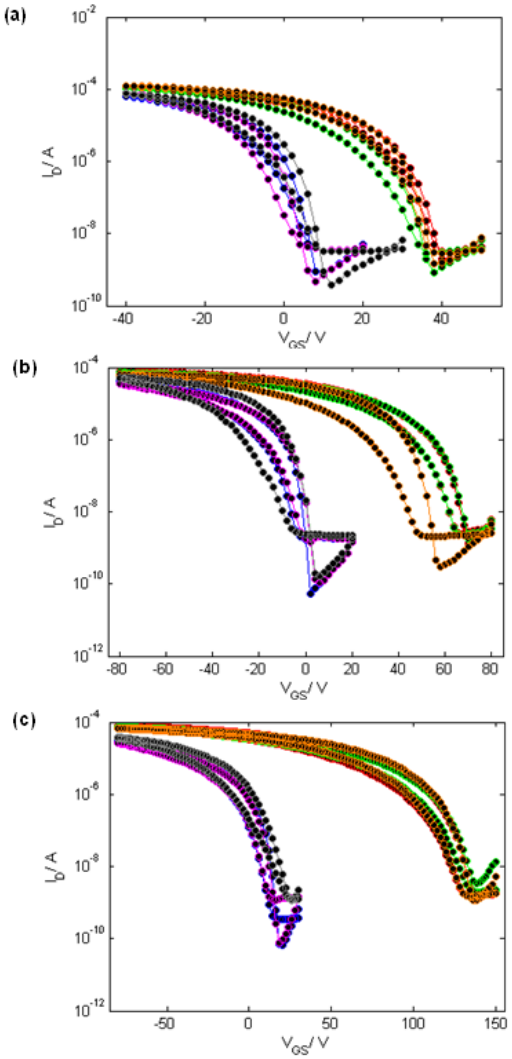

Figure 6.8: Additional transfer characteristics of pentacene based devices including a T-SC/SA semiconductor-dielectric interface layer with nominal (actual) oxide thicknesses of $d_{ox} - n = 100\,\text{nm}$ ($d_{ox} = 102.2\,\text{nm}$), $d_{ox} - n = 150\,\text{nm}$ ($d_{ox} = 147.5\,\text{nm}$), and $d_{ox} - n = 250\,\text{nm}$ ($d_{ox} = 245.0\,\text{nm}$). High positive V_{th} correspond to devices before and low V_{th} to devices after exposure to a flow of pure NH_3 gas. The source-drain voltage (V_{DS}) was set to -2 V. The increased hysteresis in the bottom plot is primarily a consequence of the extended measurement range

Table 6.3: Additional device parameters of (Si|SiOx|T-SC/SA|pentacene|Au) transistors as a function of the oxide thicknesses (d_{ox}) before (top table) and after NH_3 exposure (bottom table). Threshold/onset voltages have been derived with different methods and are denoted as, V_{ELR}, V_{SD}, and V_{SDL} (details see main paper), mobilities (μ), and on-to-off ratios (I_{on}/I_{off}) are reported. I_{off} is defined as the drain current when the gate voltage equals V_{on} and I_{on} is the current for V_{GS} equaling $V_{on} - 40\,\mathrm{V}$. The last line for each oxide thickness gives the average values.

d_{ox}	c_{ox}	V_{ELR-1} V_{ELR-2} V_{ELR-3}	V_{SD-1} V_{SD-2} V_{SD-3}	V_{SDL-1} V_{SDL-2} V_{SDL-3}	μ_1 μ_2 μ_3	$(I_{on}/I_{off})_1$ $(I_{on}/I_{off})_2$ $(I_{on}/I_{off})_3$
		V_{ELR}	V_{SD}	V_{SDL}	μ	I_{on}/I_{off}
$[nm]$	$[\frac{nF}{cm^2}]$	$[V]$	$[V]$	$[V]$	$[\frac{cm^2}{Vs}]$	$[10^3]$
102.2	34.8	22	29	40	0.22	20
		16	19	36	0.24	30
		22	27	38	0.25	40
		20	25	38	0.24	30
147.5	23.0	40	46	70	0.13	6
		42	46	70	0.11	5
		36	39	56	0.13	50
		39	44	65	0.12	20
245.0	14.1	88	96	136	0.14	2
		85	94	136	0.13	0.8
		96	103	136	0.13	3
		90	98	136	0.13	2

d_{ox}	c_{ox}	$V_{ELR-NH3-1}$ $V_{ELR-NH3-2}$ $V_{ELR-NH3-3}$	$V_{SD-NH3-1}$ $V_{SD-NH3-2}$ $V_{SD-NH3-3}$	$V_{SDL-NH3-1}$ $V_{SDL-NH3-2}$ $V_{SDL-NH3-3}$	μ_{NH3-1} μ_{NH3-2} μ_{NH3-3}	$(I_{on}/I_{off})_{NH3-1}$ $(I_{on}/I_{off})_{NH3-2}$ $(I_{on}/I_{off})_{NH3-3}$
		$V_{ELR-NH3}$	V_{SD-NH3}	$V_{SDL-NH3}$	μ	I_{on}/I_{off}
$[nm]$	$[\frac{nF}{cm^2}]$	$[V]$	$[V]$	$[V]$	$[\frac{cm^2}{Vs}]$	$[10^3]$
102.2	34.8	-5	0	8	0.20	40
		-7	-1	6	0.25	70
		-3	2	10	0.21	70
		-5	1	8	0.22	60
147.5	23.0	-17	-11	2	0.10	90
		-14	-9	4	0.08	100
		-17	-7	4	0.14	80
		-16	-9	3	0.11	90
245.0	14.1	-8	0	18	0.12	70
		-11	-1	18	0.10	40
		-8	-4	24	0.14	5
		-9	-3	20	0.12	40

Details on the x-ray reflectivity measurement

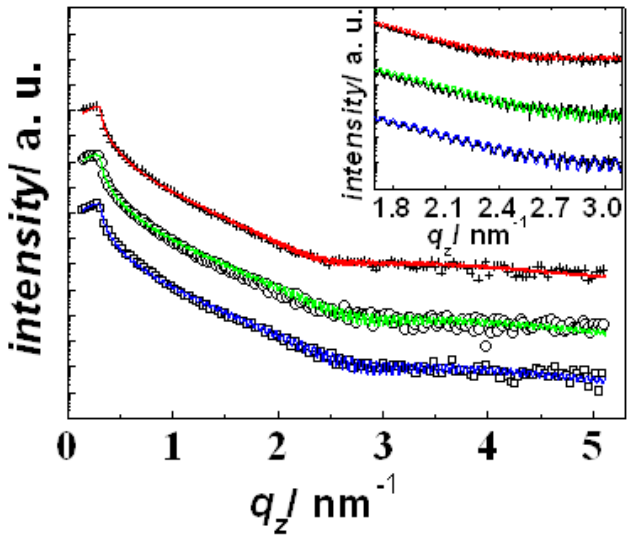

Figure 6.9: Specular x-ray reflectivity measurements for three samples with different d_{ox} (data points: squares: $d_{ox} = 102.2\,\mathrm{nm}$, circles: $d_{ox} = 147.5\,\mathrm{nm}$, +: $d_{ox} = 245.0\,\mathrm{nm}$; and corresponding fit curves). The inset shows a zoom into a smaller q_z range displaying the interference fringes due to the SiO_x layer (curves shifted for clarity).

The x-ray reflectivity measurements were performed on a Bruker diffractometer (type: D8 Discover) using CuK_α-radiation from a sealed tube. For the primary and secondary side optics and the receiving slit a sequence of 0.05 mm, 0.1 mm and 0.1 mm was used. On the secondary side, an automatic absorber is mounted. To analyze the data, we fitted them using WinGixa [102], which is an implementation of Parratt's recursive algorithm [103] including interface, σ_{ox}, and surface root mean square roughness, $\sigma_{T-SC/SA}$, according to the approach of Nevot and Croce [104]. The kink around $2.5\,\mathrm{nm}^{-1}$ originates from the interference within the T-SC/SA layer, while the fast oscillating fringes (see inset of Fig. 6.9) are a consequence of interference within the SiO_x layer. To obtain satisfactory agreement between measurements and fits (see Experimental section 8.4), the T-SC/SA layers had to be modeled as a double layer structure, i.e. as consisting of two layers with different electron density. The corresponding thicknesses are denoted as $d_{T-SC/SA-1}$ and $d_{T-SC/SA-2}$. Thus, in total a three-layer structure has been used as a model to fit the experimental data.

Contact angle measurements

The contact angles were measured with a drop shape analysis system (company: Kruess GmbH, type: DSA 100) using deionized water and diiodomethane (company: Sigma-Aldrich, product number: 158429) as test liquids (drop volume $3\,\mu$l). Based on the method by Owens Wendt [105], the surface free energy per unit area E_s of the T-SC/SA layers were calculated automatically. The contact angles were obtained by means of the sessile drop method and were measured within 2 seconds.

Table 6.4: Diiodomethane Θ_d and water Θ_w contact angles for two independent series for T-SC/SA layers grown on substrates with three different oxide layer thickness d_{ox} and the out of that calculated surface free energy E_s. The values are the standard deviations to the corresponding values derived from five independent measurements.

d_{ox}	Θ_{d1} Θ_{d2}	σ_{d1} σ_{d2}	Θ_{w1} Θ_{w2}	σ_{d1} σ_{d2}	E_{s1} E_{s2}	σ_{d1} σ_{d2}
	Θ_d	σ_d	Θ_w	σ_d	E_s	σ_d
$[nm]$	[°]	[°]	[°]	[°]	$[\frac{mJ}{m^2}]$	$[\frac{mJ}{m^2}]$
102.2	36.1	1.0	66.2	0.6	50.2	0.3
	34.8	0.7	57.7	1.1	55.0	0.3
	35.5		62.0		52.6	
147.5	37.2	1.1	68.6	0.8	48.7	0.3
	35.6	0.3	63.1	0.9	51.9	0.1
	36.4		65.9		50.3	
245.0	36.5	0.8	70.2	0.2	48.2	0.2
	35.6	0.7	62.1	1.5	51.6	0.3
	36.4		66.2		49.9	

NH_3 gas exposure (experimental procedure)

We put our devices in a homemade measurement cell and flooded the cell with NH_3 gas (company: Linde Gas, product number: UN1005), for either 30 min (data in Fig. 6.8) or 1 min (data in Fig. 6.10).The NH_3 pressure was 1.5 bar and the volume flow was approximately $8\,\mathrm{lh}^{-1}$. After the NH_3 exposure, we flooded the cell with argon gas (company: Air Liquide, type: ALPHAGAZ ARGON 1) until we could not detect ammonia at the gas outlet of the measurement cell. *Hazard warning! NH_3 is highly toxic, thus experiments should always be performed in a fume hood using appropriate gloves and protective glasses!*

HCl vapor exposure (experimental procedure)

We put the ready-made devices over a beaker filled with fuming hydrochloric acid (company: Sigma-Adrich, product number: 30721) for 1 min. Hazard warning! HCl vapor is very acidic thus experiments should always be performed in a fume hood using appropriate gloves and protective glasses!

Additional characteristics for the exposure of (Si|SiO_x|pentacene|Au) devices first to hydrochloric acid vapor (HCl) and afterwards to ammonia gas (NH_3)

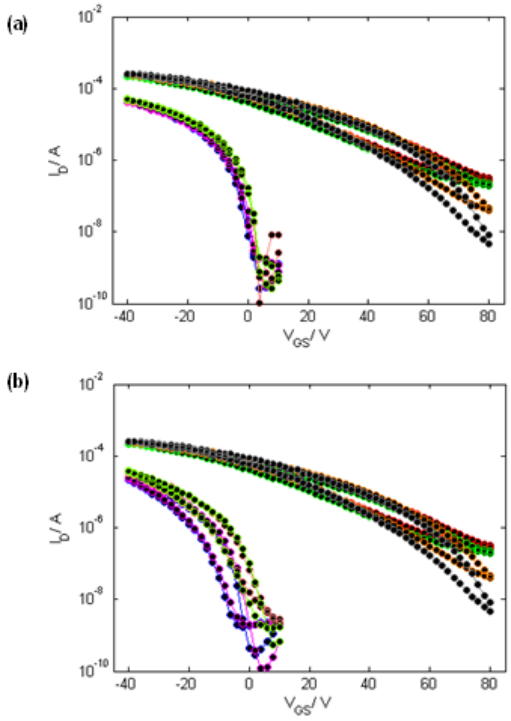

Figure 6.10: (a) Transfer characteristics of different devices before (low V_{th}) and after exposure to HCl vapor (high V_{th}); (b) transfer characteristics of the same devices after HCl exposure (high V_{th}) and after subsequently NH_3 (low V_{th}) exposure in the bottom (Fig. 6.6 (b)).

Additional data on TIPS-pentacene devices exposed to HCl vapor or containing T-SC/SA layers

TIPS-pentacene devices containing a T-SC/SA layer at the interface between the organic semiconductor and the SiO_x dielectric, as well as 'conventional'

TIPS-pentacene devices exposed to HCl vapor show clearly negative V_{th} and V_{on} in contrast to pentacene based devices (see Fig. 6.8 and Fig. 6.10).

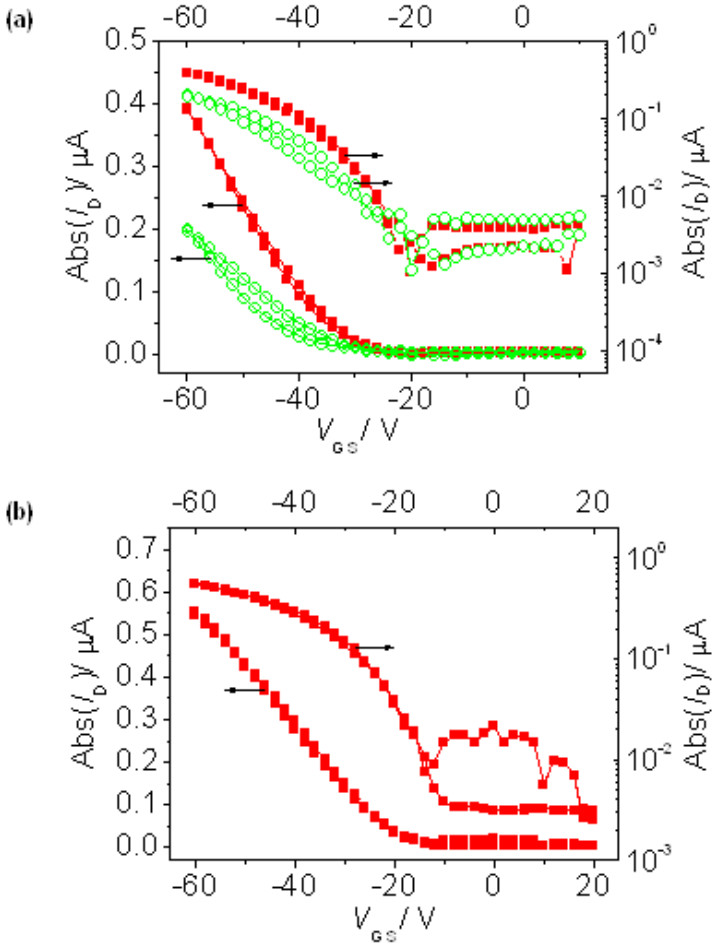

Figure 6.11: (a) Transfer characteristic of a (Si|SiO_x|TIPS-pentacene|T-SC/SA|Au) device with $d_{ox} = 152\,\text{nm}$ before (solid squares) and after exposure to HCl vapor (open circles). (b) Transfer characteristic of a (Si|SiO_x|T-SC/SA|TIPS-pentacene|Au) devices with $d_{ox} = 152\,\text{nm}$. V_{DS} is set to $-60\,\text{V}$.

In this context, it should be mentioned that the investigated TIPS-pentacene films are preferentially aligned in the (001) and (011) orientation as can be inferred from the thin-film x-ray diffraction data shown in Fig. 6.12. This means that the molecular backbones lie essentially parallel to the substrate surface ((001) orientation) or are somewhat inclined (011 orientation), which is clearly different from the preferential orientation of pentacene on SiO_x, where the molecules typically stand (close to) upright [110]. This can cause

differences in the diffusion of gasses like HCl through the active layer. Considering, however, (i) that no acid doping is observed also for acidic SAMs directly in the channel region, (ii) that the active regions are very thin, which should allow HCl to diffuse right to the channel independent of crystallite orientation and (iii) that there should be a massive impact on the transistor characteristics also if only the regions of the OSC layer close to the surface were doped and thus made conducting, it appears safe to conclude that TIPS-pentacene is not prone to acid doping (at least not when using HCl or T-SC/SA as the reagents)

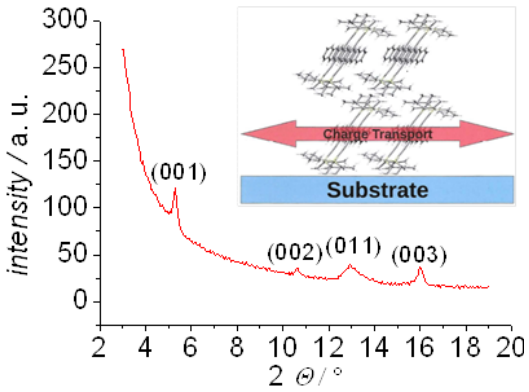

Figure 6.12: $\Theta/2 * \Theta$) scan of a pentacene layer spin-coated from toluene with the substrate held at 60 °C. The inset (courtesy of Armin Moser) shows the schematic structure for the (001) orientation.

Quantum-mechanical simulations

The quantum-mechanical calculations were performed using Gaussian03 [108] applying the B3LYP [109] hybrid functional and a 6-31G(d,p) basis set. Total energies were extracted from the last step in the geometry optimizations. Note that we encountered serious convergence problems, when optimizing the geometry of planarized TIPS-pentacene protonated at one of the central C-atoms. To circumvent these problems, we first performed a geometry optimization with loose convergence criteria (which did converge), then increased the convergence criteria to the standard values and reduced the step-size in the optimization process. Even this procedure yielded only partially converged geometries (i.e., not all of the geometry convergence criteria could be met). This problem prevailed when changing the optimizer to the Newton algorithm. As the differences between all obtained total energies (fully converged with loose convergence criteria, and partially converged with standard criteria) were smaller than 1 meV, they were eventually accepted as the

appropriate values for planarized TIPS-pentacene protonated at one of the central C-atoms. GaussView 2.1 [111] was used to plot the molecular structure in Fig. 6.13.

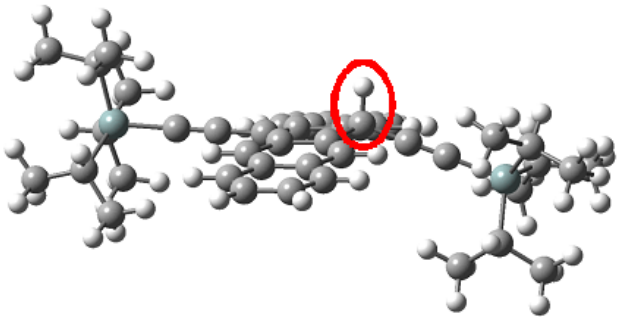

Figure 6.13: (a) B3LYP/6-31G(d,p) optimized gas-phase geometry of TIPS-pentacene protonated at the central position

Calculations of the reaction enthalpies of proton transfer between T-SC/SA or HCL and pentacene Calculations on isolated protonated/deprotonated pentacene, HCL, and TSA molecules yield energy differences between 4.0 eV and 4.7 eV (not correcting for basis-set superposition errors). These energies, however, severely overestimate the actual situation, as they do not consider the Coulomb attraction between the proton and the acid residue and also neglect medium polarization effects, which additionally significantly stabilize the charge-separated situation. Describing the actual situation in the bulk is, however, clearly beyond the scope of the present manuscript and is severely complicated by the unknown details of the interface structure and by DFT's tendency to overestimating charge delocalization.

Methodology for drift-diffusion based simulations

(this is a significantly extended version of the description in the main manuscript)

The numerical model to describe device characteristics is a two-dimensional drift-diffusion approach as described in Ref. [14] with special boundary conditions at the source and drain electrodes. Charge carrier injection occurs via thermionic emission and tunneling through a potential barrier (given by the image charge model) in WKB approximation and is corrected by an interface recombination current [106]. The corresponding system of equations containing the Poisson equation, the drift-diffusion current density equation, and the continuity equation with appropriate boundary conditions is solved self-consistently on a non-regular two-dimensional grid [14] using an implicit time integration.

During the simulation, the device geometry, the hole injection barrier of 0.47 eV from gold into pentacene [107], and the dielectric constants of pentacene ($\epsilon = 3.4$) and SiO_2 ($\epsilon = 3.9$) are kept fixed. To describe the different onset voltages at different device thicknesses, a fixed negative interface charge distribution with a density of 1.5 x 10^{17} em^{-2} and an interface dipole layer with a density resulting in a potential shift of 31 V were placed at the pentacene-SiO_x interface. The latter were realized by placing two oppositely charged space charge layers with an areal charge density of 2.0 x 10^{19} em^{-2} at a distance of 3 Å.

To further account for the shape of the I-V curves obtained in the experiments two types of traps are considered: (i) The occurrence of a hysteresis (cf. Fig. 6.13) is simulated by including bulk traps. The density $p_{trap}(x, y)$ of trapped holes is self-consistently determined for each time step using the rate equation $dp_{trap}(x, y)/dt = 1/\tau'_{trap} p(x, y) - 1/\tau'_{detrap} p_{trap}(x, y)$, where p(x,y) denotes the hole density and τ'_{trap} and τ'_{detrap} are the trapping and detrapping time constants, respectively. The latter are of the order of seconds; the used numerical values are listed in Table 6.5. For the bulk traps we assume that the available number of trapping sites far exceeds the number of trapped carriers for the considered time scales (i.e., it does not need to be considered explicitly) (ii) To properly account for the shape of the transfer-characteristics in the sub-threshold region (cf. Fig. 6.13), additional interface traps are incorporated [76]. To prevent a possible influence on the hysteresis, they are treated as being always in the steady state, which is a reasonable assumption as long as the associated time constants are clearly shorter than the acquisition times for each measurement point. A simulation including a single trap level is not sufficient to capture the shape of the transfer characteristic at gate voltages close to the threshold-voltage (see next section). This deficiency can be mended by assuming a trap distribution rather than a single trap level. The actual density of trapped carriers p_t is self-consistently determined depending on the mobile carrier density at the interface and the width of the trap distribution. For the sake of simplicity, the trap distribution is assumed to be rectangular shaped, to have a width $\sigma = 0.1$ eV, and to be shifted by $A = 0.1$ eV with respect to the hole transport level E_{HOMO}. I.e., the trap density can be written as $D_t(E) = p_{t0}/\sigma\Theta(E - (E_{HOMO} + A))\Theta(E_{HOMO} + A + \sigma - E)$ with $\Theta(E')$ denoting the Heaviside function and p_{t0} the total number of traps. To describe the density of trapped carriers, p_t, we solve the following differential equation: $dp_t(x, y)/dt = 1/\tau_{trap}(p_{t0} - p_t)/p_{t0} p(x, y) - 1/\tau_{detrap} p_t(x, y)$, where the term $(p_{t0} - p_t)/p_{t0}$ is introduced to provide an upper limit of the total number of trapped carriers; in the steady state one only needs to know the ratio $\tau_{detrap}/\tau trap$. For the above described rectangular density of states, the

latter becomes: $\tau_{detrap}/\tau_{trap} = exp[(\sigma(1 - p_t/p_{t0}) + A)q/k_BT]$, where k_B is the Boltzmann constant, and $T = 298\,\mathrm{K}$ the temperature. The above two equations are solved self-consistently.

Table 6.5: Parameters used to simulate the transfer characteristics for all oxide thicknesses d_{ox}. Mobility, μ; acquisition time per data point, t; trapping time constant, t_{trap}, and detrapping time constant, t_{detrap}, of the long-lived bulk traps; density of the short-lived interface traps, p_{t0}. The values of the hole mobility and the density of interface traps of the 100 nm device differ somewhat from the corresponding value in thicker devices. The differently pretreated substrate in the 100 nm device presumably has interface properties that deviate from the 150 nm and 250 nm devices and, thus, alter interface-determined quantities such as mobility and interface trap density. The deviation between the intrinsic mobility used here and the effective mobility extracted from the experiments will be discussed in section 'Detailed discussion of the impact of traps on the device characteristics'.

d_{ox} $[nm]$	μ $[\frac{cm^2}{Vs}]$	t $[s]$	p_{t0} $[\frac{1}{m^2}]$	τ_{trap} $[s]$	τ_{detrap} $[s]$
100	0.34	0.1	$3.2 * 10^{16}$	11	4
150	0.21	0.1	$4.3 * 10^{16}$	11	4
250	0.23	0.1	$4.3 * 10^{16}$	11	4

Comparison between measured and calculated transfer characteristics

The simulated curves are in an excellent agreement with the measured ones (cf., Fig. 6.14), in particular, considering that only a few degrees of freedom have been taken to account in the simulations. Reasons for the residual mismatch between theory and experiment could possibly be (i) more sophisticated trap-distributions, (ii) the varying data acquisition time of the Keithley source meter at low device currents (vide supra, resulting in an overestimation of the hysteresis at small currents), and (iii) mobility degradation that affects the high current region. The latter gives rise to an overestimation of IDS for large negative V_{GS}, which could either be accounted for by a V_{GS}-dependent mobility or assuming a mobility that decreases close to the interface [31], where charge carriers are more strongly accumulated at large negative V_{GS}.

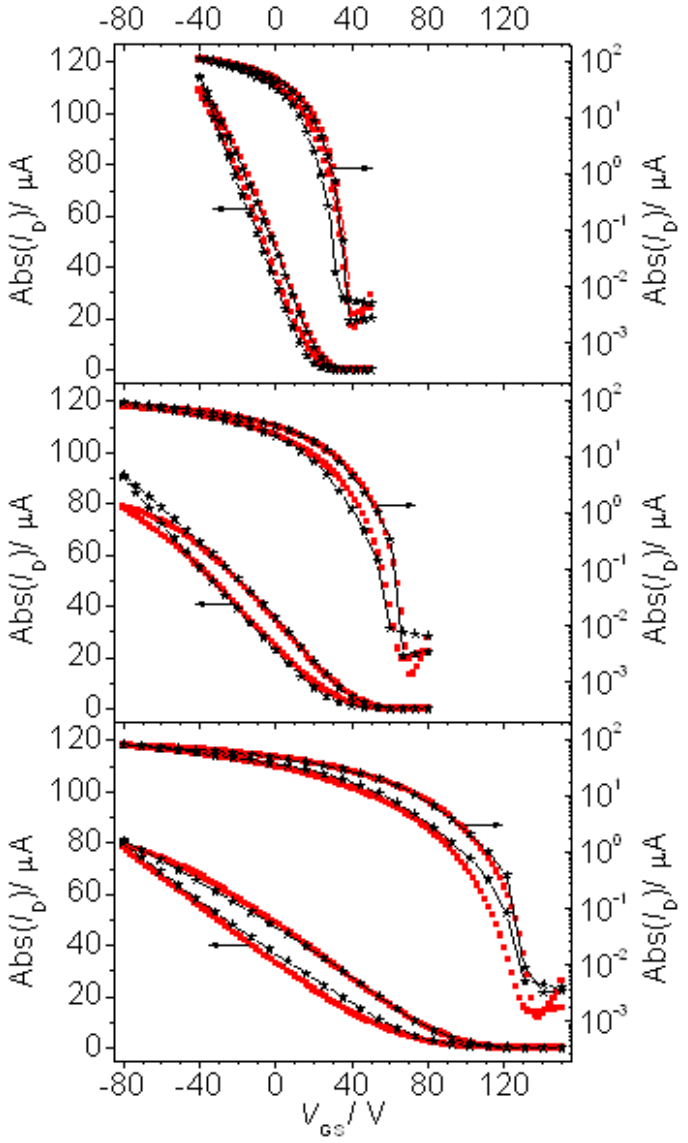

Figure 6.14: . Comparison between simulated (black stars) and measured (red squares) transfer characteristics (from top to bottom: $d_{ox-n} = 100\,\text{nm}$, $d_{ox-n} = 150\,\text{nm}$ and $d_{ox-n} = 250\,\text{nm}$).

Detailed discussion of the impact of traps on the device characteristics

While the general observation of a gate-oxide thickness dependent V_{th} can be consistently modeled by the space charge and dipole densities as discussed extensively in the main manuscript, the detailed shapes of the transfer

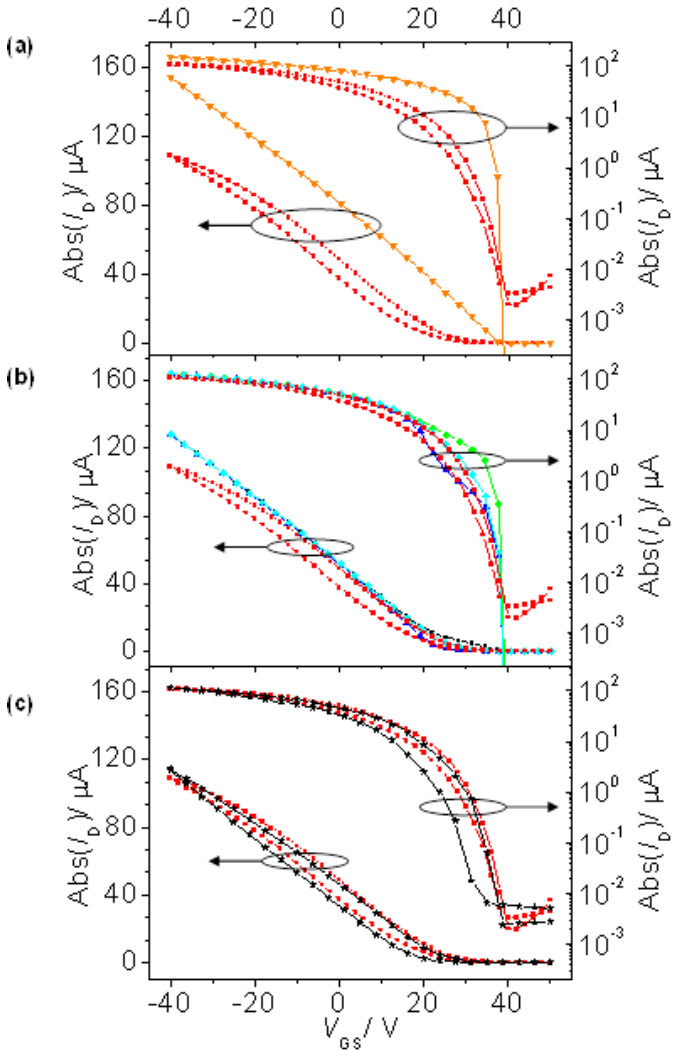

Figure 6.15: Linear (left) and semi-logarithmic (right) plot of simulated transfer curves for the $d_{ox} = 100\,\text{nm}$ device assuming fixed intrinsic mobilities and interface charge layers upon increasing the number of considered effects. The experimental curves are shown as red solid squares for comparison. (a) considering no further effects; (b) comparison between interface trap distributions: a single interface trap level at 0.1 (green solid circles) and 0.2 eV (blue solid triangles) above the transport level and a constant interface trap density between 0.1 eV and 0.2 eV above the hole transport level (cyan solid diamond). (c) 'final' model including the rectangular interface trap density from b) and bulk traps as described in section 12 black solid stars()

characteristics are not reproduced in a 'straightforward' calculation assuming a fixed carrier mobility and disregarding traps. This becomes obvious from a comparison between Fig. 6.14 and Fig. 6.15 (a). To further illustrate that, Fig. 6.7 shows the evolution of the transfer-characteristics upon including an increasing amount of effects. As discussed in the main text, the switch-on voltage is quantitatively captured by the charge distributions at the dielectric-pentacene interface.

Including various types of traps, the full characteristics can, however, be recovered even regarding the hysteresis and a suitable off-current. Which details of the characteristics are affected by which physical effect can be seen in Fig. 6.15, where we successively increase the complexity of the applied model. Fig. 6.15 (a) compares the experimental transfer characteristics with the one obtained in the simulations assuming a constant mobility of $\mu = 0.34\,\mathrm{cm}^2/(\mathrm{Vs})$. The latter is somewhat larger than that extracted from the experimental data. It can be regarded as an 'intrinsic' mobility that is determined by the transport properties of pentacene and by shallow traps that are filled/emptied at time-scales much faster than those relevant for the experiment. It is necessary to start with such a large value of μ, as the 'effective' mobility will be reduced when introducing traps in the following steps. A satisfactory agreement between theory and experiment is also not achieved, when using the experimentally determined effective mobility.

The correct description of the shape of the curves (in particular the subthreshold swing) requires the incorporation of interface traps [107]. It is important to note here the quality of agreement needs to be assessed both from the linear as well as from the semi-logarithmic plot. As illustrated in Fig. 6.15 (b), the inclusion of a single level of short-lived traps causes the desired reduced slope of the I-V curve in the sub threshold region (circles and triangles). Upon inspecting the curves in the logarithmic plot (corresponding right panel) it , however, becomes evident that a single trap level is even qualitatively not sufficient to reproduce the measurements due to a marked kink, e.g., at $V_{GS} = 30\,\mathrm{V}$ for a 0.1 eV trap. Rather, as shown as diamonds in Fig. 6.15 (b), a distribution of traps can reproduce the shape satisfactorily, since the resulting 'superposition' of trap levels smears out the kinks associated with a single trapping energy. Finally, the incorporation of additional, long-lived traps gives rise to a hysteresis (Fig. 6.15 c). Regarding the origin of residual deviations between theory and experiment see the discussion at the end of section 'Comparison between measured and calculated transfer characteristics'.

Chapter 7

Organic thin-film transistor based memory

7.1 Introduction

Space charges at the semiconductor-dielectric interface have a huge impact on the threshold voltage (V_{th}) [14]. One possibility to realize such space charges is by covalent bonding of so called self-assembled monolayers including an acidic functional group at the semiconductor-dielectric interface, as shown in chapter 6. Due to proton transfer between the functional group and pentacene, holes and a negative charged acid residue layer are generated simultaneously, which results in a shift of V_{th} to high positive values in p-channel organic thin-film transistors (OTFTs). This chemically induced V_{th} shift can be compensated with the base ammonia (NH_3).

Another possibility to realize such negative charged space charges is by electrons, which are trapped at the semiconductor-dielectric interface. This can be realized by injecting or generating electrons in the organic semiconductor material and ensuring that these electrons are trapped at the semiconductor-dielectric interface. Realizing that is the topic of the present chapter. As the used devices were p-channel OTFTs, the electrons were not injected from the gold source and drain electrodes, due to high electron injection barrier between gold and pentacene. Instead, in the pentacene layer excitons were generated with the help of ultraviolet (UV) light. In case excitons dissociate, they can act as "electron source". Such electrons can then be attracted to the semiconductor-dielectric interface by applying a positive voltage between gate and source (V_{GS}). Due to the choice of silicon oxide (SiO_x) as dielectric material, the attracted electrons can be expected to get trapped [13]. This then should result in a shift of V_{th} to more positive

values in the used p-channel OTFTs. The trapped electrons could then be detrapped by light illumination and by simultaneously applying a negative V_{GS}. This should then shift V_{th} back to lower values.

In principle this setup, consisting of a simple pentacene based OTFT with SiO_x as dielectric material, represents a nonvolatile memory, where the two memory states logical 0 and logical 1 realized, on the one hand, by the low V_{th} state and, on the other hand, by the high V_{th} state of the OTFT.

7.2 Results and discussion

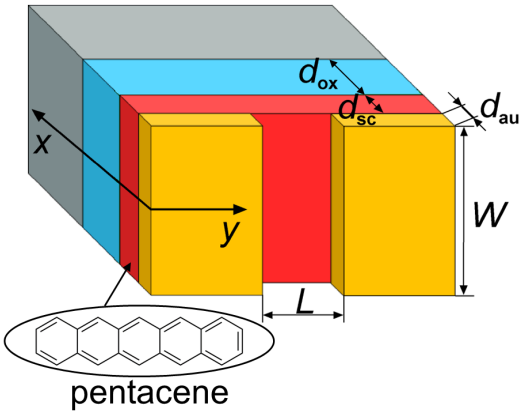

Figure 7.1: Configuration of top-contact bottom-gate transistors, where the gate electrode is made of doped silicon, the dielectric is thermally grown silicon oxide, the active layer material is pentacene and source and drain electrodes are made of gold. The channel length (L) is 25 μm, the channel width (W) is 7 mm, the oxide thickness d_{ox} is 150 nm, the thickness of the organic semiconductor (d_{sc}) is 50 nm and the thicknesses of the source and drain electrodes (d_{au}) are 50 nm, where the latter two values were measured with a quartz micro balance.

The devices were based on pentacene as active layer material and SiO_x as dielectric layer. Moreover, source and drain electrodes were made of Au (see Fig. 7.1). The used devices were common gate, which means that always four devices were produced on one substrate and, thus, four devices used one common gate.

As mentioned above, to realize the two memory states, excitons in the pentacene film are necessary as electron source. Therefore, to be sure that the available UV light source is appropriate, in a first step it was tried to reproduce some observations concerning OTFT characteristics, which were

attributed to excitons. In Ref. [112] it is described that the V_{th} of OTFTs measured during UV light illumination is shifted to more positive values. Additionally, the authors observed for an increased hysteresis for "double sweep" transfer curve measurements in comparison to measurements performed in darkness. Moreover, the V_{th}-shift is lower after switching off the UV light and measuring in darkness, it is nevertheless still visible.

7.2.1 Influence of ultraviolet light illumination on the device characteristics

Measurements during ultravilot illumination

Fig. 7.2 and Fig. 7.3 clearly show, that we could reproduce the following findings of Ref. [112], namely a shift of V_{th} (see Tab. 7.1) to more positive values and an increased hysteresis for measurements, which were performed during UV illumination (for details concerning UV illumination see Experimental section). Therefore, we are sure, that the used light source and the used intensity are appropriate.

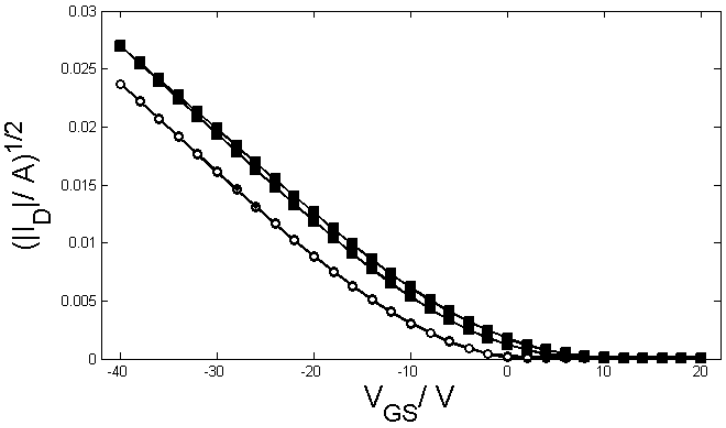

Figure 7.2: Square root of the absolute value of the drain current (I_D) as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. The open circles corresponds to a measurement in darkness and the closed squares corresponds to a measurement under ultraviolet illumination.

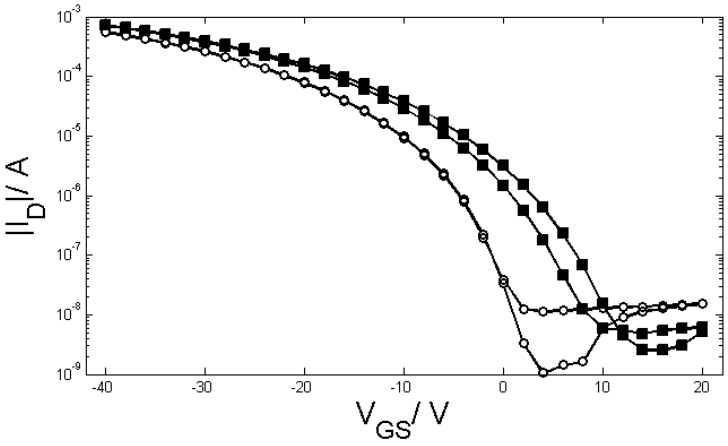

Figure 7.3: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. The open circles corresponds to a measurement in darkness and the closed squares corresponds to a measurement under ultraviolet illumination.

Moreover, V_{th} shifted more and more by repeating the measurement during UV illumination, as can be seen in Fig. 7.4 and Fig. 7.5. The charge carrier mobility (μ) was hardly influenced by UV light and the on-to-off ratios (I_{on}/I_{off}) were all in the same range (see Tab. 7.1).

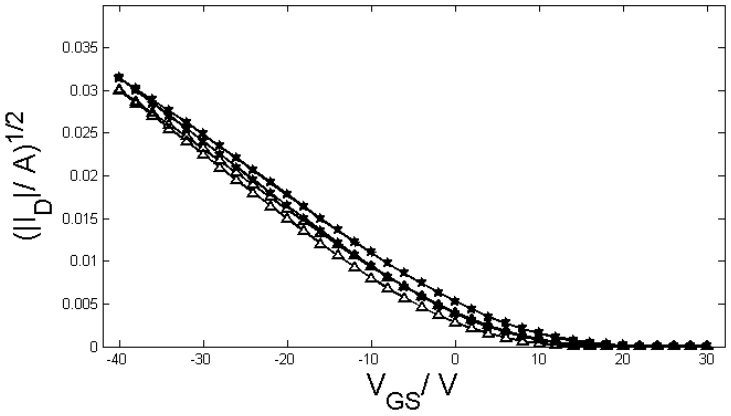

Figure 7.4: Square root of the absolute value of the drain current (I_D) as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage V_{DS} of -20 V. The open triangles corresponds to the second measurement under ultraviolet (UV) illumination and the closed stars corresponds to the third measurement under UV light.

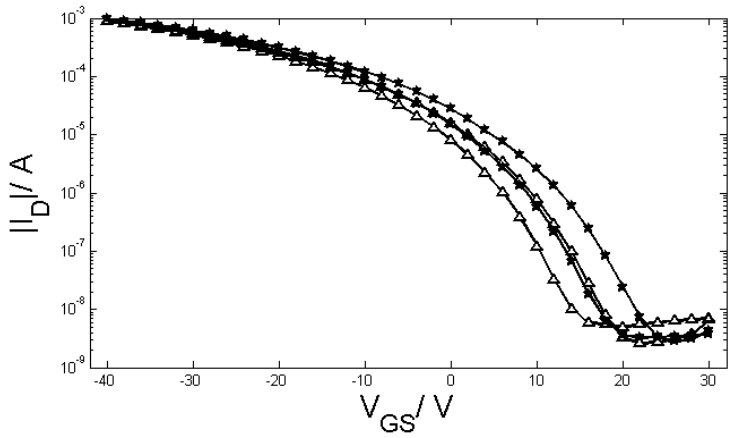

Figure 7.5: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage V_{DS} of -20 V. The open triangles corresponds to the second measurement under ultraviolet (UV) illumination and the closed stars corresponds to the third measurement under UV light.

Table 7.1: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}), mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) and the on-to-off ratios I_{on}/I_{off} are shown. I_{off} is defined as the drain current when the gate voltage equals V_{SDL} and I_{on} is the current for V_{GS} equaling $V_{on} - 30$ V. The values indicated with different symbols (S) were extracted of the corresponding curves in Fig. 7.2, Fig. 7.3, Fig. 7.4 and Fig. 7.5. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

S [1]	V_{ESR} [V]	V_{SDL} [V]	μ [$\frac{cm^2}{Vs}$]	I_{on}/I_{off} [10^3]
circle	-8	4	0.17	100
square	-2	12	0.15	50
triangle	4	20	0.14	30
star	7	24	0.13	30

Measurements after ultravilot illumination

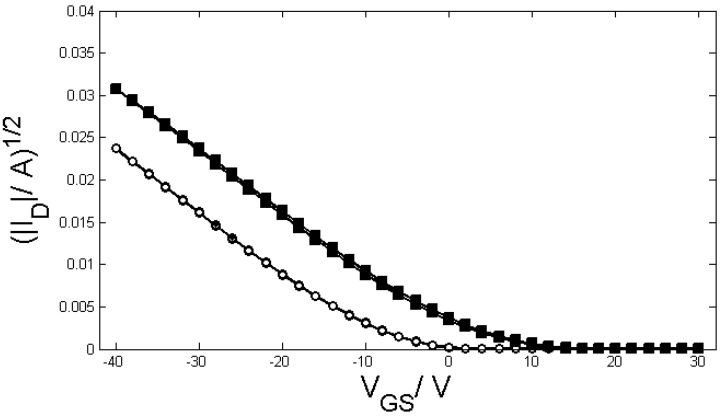

Figure 7.6: Square root of the absolute value of the drain current (I_D) as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage V_{DS} of -20 V. The curve indicated with open circles is the initial curve and the closed square curve is measured after switch of the ultraviolet (UV) light source.

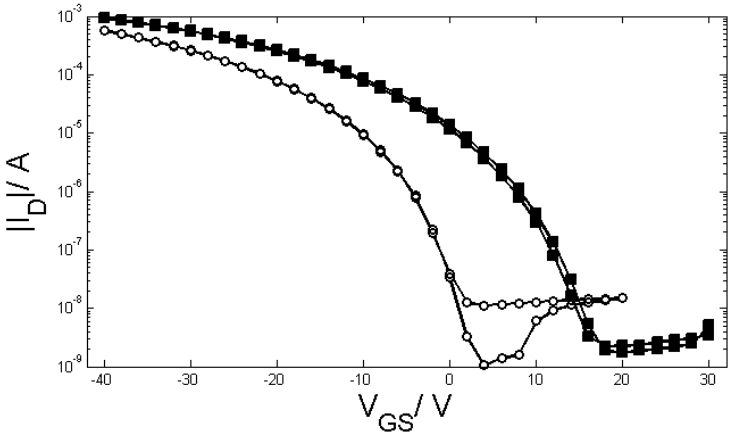

Figure 7.7: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage V_{DS} of -20 V. The curve indicated with open circles is the initional curve and the closed square curve is measured after switch of the ultraviolet (UV) light source.

Table 7.2: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}), mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) and the on-to-off ratios I_{on}/I_{off} are shown. I_{off} is defined as the drain current when the gate voltage equals V_{SDL} and I_{on} is the current for V_{GS} equaling $V_{on} - 30$ V. The values indicated with different symbols (S) were extracted of the corresponding curves in Fig. 7.6 and Fig. 7.7. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

S [1]	V_{ESR} [V]	V_{SDL} [V]	μ [$\frac{cm^2}{Vs}$]	I_{on}/I_{off} [10^3]
circle	-8	4	0.17	100
square	3	18	0.16	60

Measuring the same device afterwards in darkness, lead to a decrease of the hysteresis (see closed squares in Fig. 7.6 and Fig. 7.7), but in comparison to the initial measurement (open circles in Fig. 7.6 and Fig. 7.7), a clear V_{th}-shift was observed, which is in agreement with Ref. [112].

One can conclude, that the programming step of the memory from low level memory state (low V_{th}) to high level memory state (high V_{th}) could be realized as confirmed by measured transfer curves during illumination of the devices with UV light. In a next step, it was tried to erase the memory, which means shift the high level V_{th} back to low level V_{th}. Our first try was to do this with the help of an electric field.

7.2.2 Influence of a electric field on the device characteristics

As one can see from Fig. 7.3 the measurement before and after applying V_{GS} of -40 V for 1 min are nearly identical, which is reflected also in the extracted parameters (see Tab. 7.3). That is, shifting V_{th} back solely by applying an electric field does not work. This is, however, necessary to realize the low level memory state, i. e., to erase the memory.

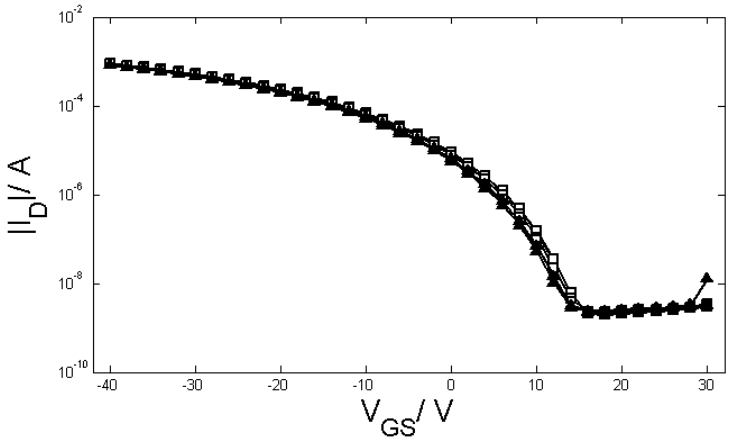

Figure 7.8: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. Between the measurement indicated with open squares and the measurement indicated with closed triangles, a V_{GS} of -40 V was applied for 1 min.

Table 7.3: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}), mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) and the on-to-off ratios I_{on}/I_{off} are shown. I_{off} is defined as the drain current when the gate voltage equals V_{SDL} and I_{on} is the current for V_{GS} equaling $V_{on} - 30$ V. The values indicated with different symbols (S) were extracted of the corresponding curves in Fig. 7.3. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

S [1]	V_{ESR} [V]	V_{SDL} [V]	μ [$\frac{cm^2}{Vs}$]	I_{on}/I_{off} [10^3]
square	1	16	0.16	60
triangle	0	14	0.16	60

Therefore, it was tried to detrap the trapped electrons by infrared (IR) light illumination.

7.2.3 Influence of infrared light illumination on the device characteristics

This frequency range was chosen, on the one hand, to prevent creation of excitons by absorption in pentacene, and, on the other hand, to support the electrons with sufficient energy to be detrapped. In a first approach the two mentioned conditions, concerning IR light source were tested. Therefore, transfer measurements done under IR light illumination were compared to measurements performed in darkness. This was done to check the results of Ref. [112], where several effects were attributed to exciton formation due to UV light. It is expected that we can not observe any of these effects in the case of IR light illumination.

Measurements during infrared illumination

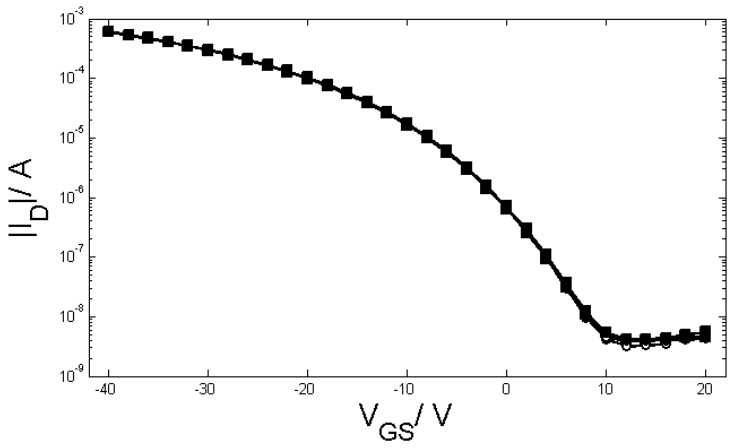

Figure 7.9: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. The measurement indicated with open circles was done in darkness and the measurement indicated with closed squares was done under infrared illumination.

Table 7.4: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}), mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) and the on-to-off ratios I_{on}/I_{off} are shown. I_{off} is defined as the drain current when the gate voltage equals V_{SDL} and I_{on} is the current for V_{GS} equaling $V_{on} - 30$ V. The values indicated with different symbols (S) were extracted of the corresponding curves in Fig. 7.3. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

S [1]	V_{ESR} $[V]$	V_{SDL} $[V]$	μ $[\frac{cm^2}{Vs}]$	I_{on}/I_{off} $[10^3]$
circle	-6	10	0.16	30
square	-6	10	0.16	30

The above described experiments reveal that it is impossible to distinguish the two measurements (see Fig. 7.9), where one was done in darkness and the other one under IR illumination. This is also reflected in identical extracted device parameters (see Tab. 7.4). This means that the used IR lamp fulfills the "non-excitation" condition, i. e. there is no increased hysteresis and no shift of V_{th} to positive values. In a next step it was tried to detrap electrons in devices, which includes trapped electrons due to UV illumination and simultaneously voltage apply, by IR illumination. Therefore, we first illuminated the devices with IR light without applying a voltage on the device during illumination and measure them afterwards in darkness.

Measurements after infrared illumination

As one can see, the try to erase the memory, in especially to shift V_{th} back to lower values, due to IR illumination induced detrapping was not successful (see Tab. 7.5). There is no difference between the curves before and after IR illumination observable (see Fig. 7.10).

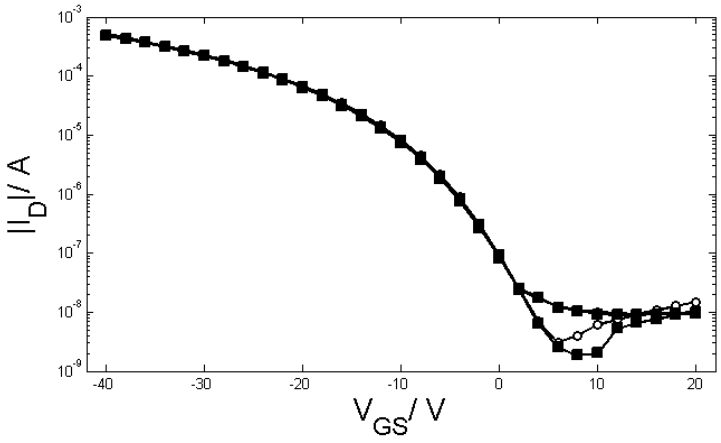

Figure 7.10: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. The measurement indicated with open circles is the initional measurement done in darkness and the measurement indicated with closed squares was even done in darkness, after infrared illumination for some minutes.

Table 7.5: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}), mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) and the on-to-off ratios I_{on}/I_{off} are shown. I_{off} is defined as the drain current when the gate voltage equals V_{SDL} and I_{on} is the current for V_{GS} equaling $V_{on} - 30$ V. The values indicated with different symbols (S) were extracted of the corresponding curves in Fig. 7.3. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

S [1]	V_{ESR} [V]	V_{SDL} [V]	μ [$\frac{cm^2}{Vs}$]	I_{on}/I_{off} [10^3]
circle	-9	6	0.16	30
square	-9	6	0.15	60

We can not exclude, that the IR photons indeed detrap the electrons, but due to low diffusion velocity and/or high trapping rate, the detrapped electrons were trapped anew. Therefore, the following test experiment was done.

Measurements after infrared illumination combined with applying a voltage

During IR illumination a negative V_{GS} was applied. If the IR light source does not detrapp the electrons, then the applying of V_{GS} during IR light illumination should not be able to detrapp the electrons. In the case of detrapping the electrons due to IR light, the detrapped electrons drift due to negative V_{GS} away from the dielectric-semiconductor interface, where the traps are located, and the electrons can flow out the device. Therefore, a shift of V_{th} to low values can be expected.

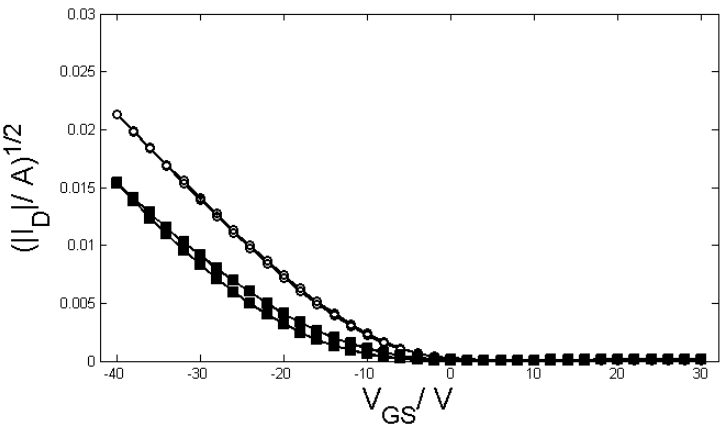

Figure 7.11: Square root of the absolute value of the drain current (I_D) as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. The measurement indicated with open circles is the initional measurement done in darkness and the measurement indicated with closed squares was even done in darkness, after infrared illumination for 2 min and simultaneously apply a gate-source voltage (V_{GS} of -80 V.

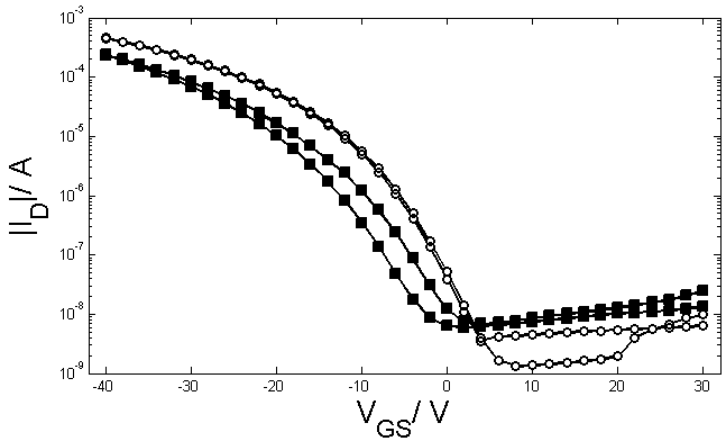

Figure 7.12: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. The measurement indicated with open circles is the initional measurement done in darkness and the measurement indicated with closed squares was even done in darkness, after infrared illumination for 2 min and simultaneously apply a gate-source voltage (V_{GS} of -80 V.

Table 7.6: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}), mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) and the on-to-off ratios I_{on}/I_{off} are shown. I_{off} is defined as the drain current when the gate voltage equals V_{SDL} and I_{on} is the current for V_{GS} equaling $V_{on} - 30$ V. The values indicated with different symbols (S) were extracted of the corresponding curves in Fig. 7.3. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

S [1]	V_{ESR} [V]	V_{SDL} [V]	μ [$\frac{cm^2}{Vs}$]	I_{on}/I_{off} [10^3]
circle	-10	6	0.16	80
square	-16	0	0.12	10

As one can see from Fig. 7.11 and Fig. 7.11 one can shift V_{th} back to lower values with the help of applying a negative V_{GS} during IR illumination. This has the following quite important consequence in terms of an application. As mentioned above, the used devices are common gate, which means that always four devices are build on one substrate. To erase less than all four

memories, one can illuminate all memories with IR light and only those ones are erased to which a negative V_{GS} is applied.

Inspired by the finding of the possibility to detrap electrons we tried to modify also the programming step of the memory.

7.2.4 Memory programming and erase step

Measurement after ultraviolet illumination

First we check, whether only illumination of a device with UV light is sufficient to trap electrons or whether additionally a positive V_{GS} is necessary.

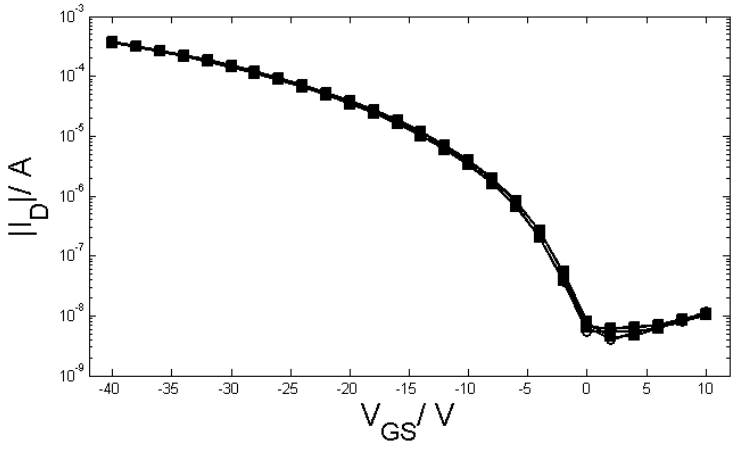

Figure 7.13: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. The measurement indicated with open circles is the initional measurement done in darkness and the measurement indicated with closed squares was even done in darkness, after ultraviolet illumination for 1 min.

Table 7.7: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}), mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) and the on-to-off ratios I_{on}/I_{off} are shown. I_{off} is defined as the drain current when the gate voltage equals V_{SDL} and I_{on} is the current for V_{GS} equaling $V_{on} - 30$ V. The values indicated with different symbols (S) were extracted of the corresponding curves in Fig. 7.3. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

S [1]	V_{ESR} [V]	V_{SDL} [V]	μ [$\frac{cm^2}{Vs}$]	I_{on}/I_{off} [10^3]
circle	-11	0	0.13	20
square	-11	0	0.13	20

The data in Tab. 7.7 show that illumination of the OTFT with UV light do not change the device characteristic (see Fig. 7.13 and Tab. 7.7). Therefore, in the next control eyperiment during UV illumination, a positive V_{GS} was applied, to attracted electrons to the gate-dielectric interface where they are trapped.

Measurement after ultraviolet illumination with combined positive voltage apply

Table 7.8: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}), mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) and the on-to-off ratios I_{on}/I_{off} are shown. I_{off} is defined as the drain current when the gate voltage equals V_{SDL} and I_{on} is the current for V_{GS} equaling $V_{on} - 30$ V. The values indicated with different symbols (S) were extracted of the corresponding curves in Fig. 7.3. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

S [1]	V_{ESR} [V]	V_{SDL} [V]	μ [$\frac{cm^2}{Vs}$]	I_{on}/I_{off} [10^3]
circle	-3	14	0.09	20
square	4	22	0.08	10

As one can see the different way to program the memory was successful.

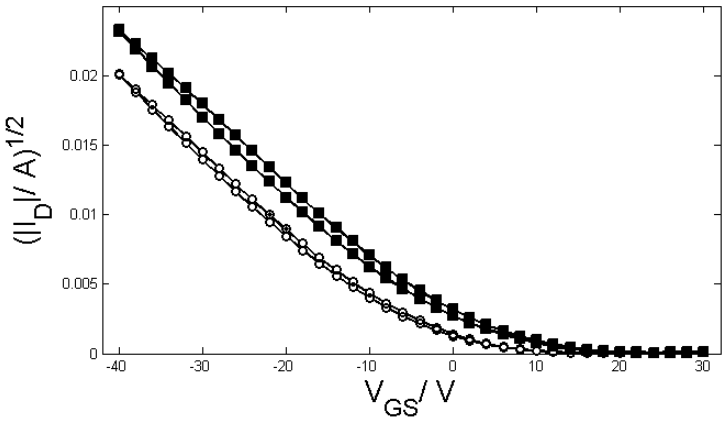

Figure 7.14: Square root of the absolute value of the drain current (I_D) as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. The measurement indicated with open circles is the initional measurement done in darkness and the measurement indicated with closed squares was even done in darkness, after ultraviolet illumination for 1 min and simultaneously apply a gate-source voltage (V_{GS}) of 40 V.

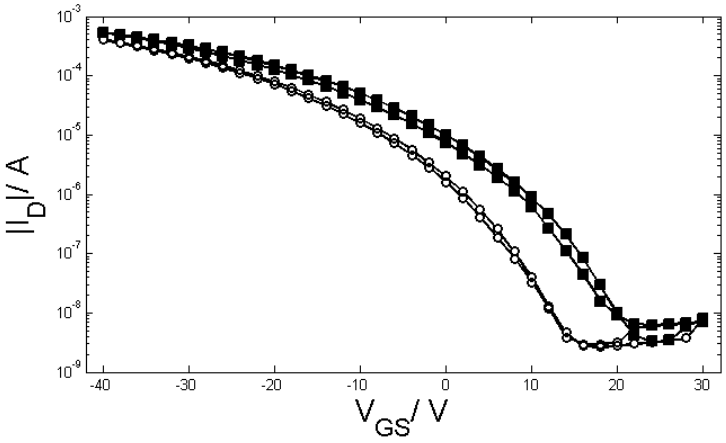

Figure 7.15: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. The measurement indicated with open circles is the initional measurement done in darkness and the measurement indicated with closed squares was even done in darkness, after infrared illumination for 1 min and simultaneously apply a gate-source voltage (V_{GS}) of 40 V.

V_{th} was shifted to higher values due to a positive applied V_{GS} and simultaneously illumination with UV light.

Another consequence of the observation that trapping of electrons originates from UV excited excitons only when they are trapped attracted to the dielectric-semiconductor interface due to negative V_{GS} is the following: In principle even the erase process should be successful by using UV light source instead of the IR light source. On the one hand the UV light has enough energy to detrap electrons and on the other hand even though UV light creates electrons, due to dissociation of UV excited excitons, a positive V_{GS} prevents their trapping just as described above for the IR-detrapped electrons.

Therefore, we tried to detrapp the trapped electrons also with UV light while applying a negative V_{GS} during illumination.

Measurement after ultraviolet illumination with combined negative voltage apply

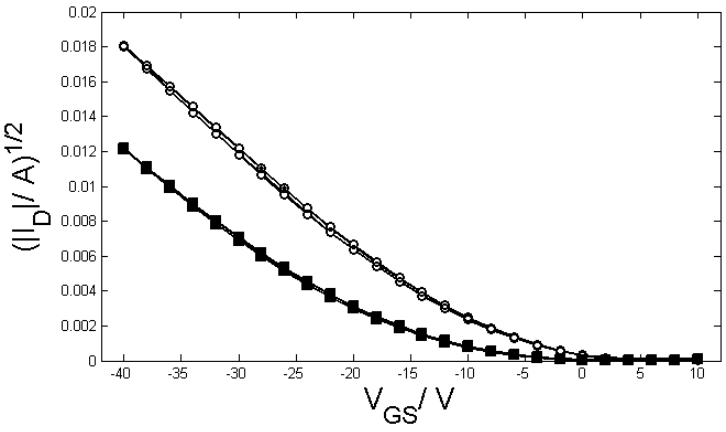

Figure 7.16: Square root of the absolute value of the drain current (I_D) as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. The measurement indicated with open circles is the initional measurement done in darkness and the measurement indicated with closed squares was even done in darkness, after ultraviolet illumination for 1 min and apply V_{GS} of -80 V simultaneously.

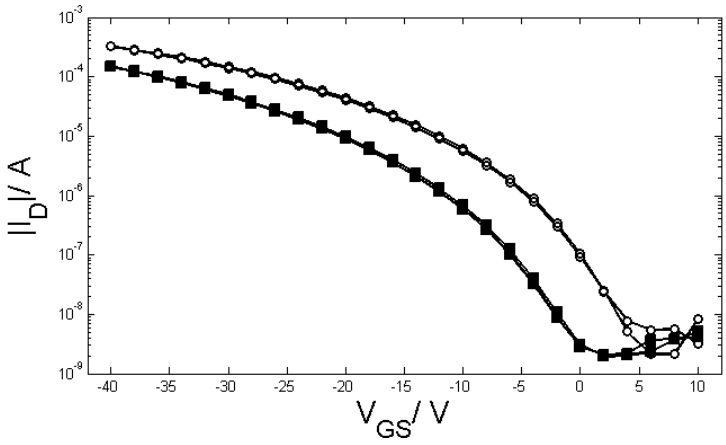

Figure 7.17: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}), measured with a drain-source voltage (V_{DS}) of -20 V. The measurement indicated with open circles is the initional measurement done in darkness and the measurement indicated with closed squares was even done in darkness, after ultraviolet illumination for 1 min and apply V_{GS} of -80 V simultaneously.

Table 7.9: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}), mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) and the on-to-off ratios I_{on}/I_{off} are shown. I_{off} is defined as the drain current when the gate voltage equals V_{SDL} and I_{on} is the current for V_{GS} equaling $V_{on} - 30$ V. The values indicated with different symbols (S) were extracted of the corresponding curves in Fig. 7.3. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

S [1]	V_{ESR} [V]	V_{SDL} [V]	μ [$\frac{cm^2}{Vs}$]	I_{on}/I_{off} [10^3]
circle	-9	8	0.10	7
square	-16	0	0.08	20

Fig. 7.16 and Fig. 7.17 shows that this modified erasing step works well.

It was possible to shift V_{th} to lower values (Tab. 7.9) and to shift V_{th}n to higher values with only one light source, i. e. a UV light source.

7.3 Conclusions

We could show, that it is possible to realize a binary memory on a simple pentacene based OTFT including SiO_x as dielectric. Nowadays SiO_x is no more used as dielectric material, because of its electron trapping properties. In this case exactly this behavior is important. We propose exciton creation due to UV light in the pentacene layer. By applying negative V_{GS} the electrons, originating from the excitons, are trapped at the semiconductor-dielectric interface. This trapped charges are the reason for the V_{th}-shift to positive values. By illumination with light again, one allows the trapped electrons to detrap and by simultaneously applying positive V_{GS} one achieve, that they are removed from the device. Additionally, we could show that one light source is sufficient for programming as well as erasing step of the memory. Moreover, our test experiment show that the programming and erasing step is selective addressable by apply V_{GS}, where their is no need for a mask to shield the UV light.

7.4 Acknowledgment

We thank Manfred Gruber from the Institute of Theoretical and Computational Physics of Graz University of Technology for fruitful discussions.

7.5 Experimental

7.5.1 Device fabrication

The device production was done in the same way as described in chapter 6, but without the ultrasonic bath step, because we do not need a high amount of OH-groups for self-assembled monolayer growth (see chapter 6).

7.5.2 Light illumination

Infrared illumination

An IR light source (company: Phillips, type: HP3616) was used. The cross section of the IR emission of the lamp has a diameter of 12 cm. Note, that we do not use the whole lighting area, because the cross

Ultraviolet illumination

A ultraviolet light source (company: EFOS, type: Novacure) was used, where we chosen the geometry of the setup and the output intensity of the light source in such a manner that the intensity at the devices was in the range of $10\,\mathrm{mW/m^2}$.

Chapter 8

Bias-stress effects caused by protons

8.1 Introduction

As pointed out in chapter 6 acids and bases have a huge impact on the device performance and here especially on the threshold voltage (V_{th}). With the help of acids, V_{th} is shifted to more positive values in p-channel devices, where this acid induced V_{th} shift can be compensated with a base. In this surface proton transfer doping process, protons play a crucial role. Additionally, protons are responsible for bias stress effect, as has been proposed in [18, 19, 20]. The protons, relevant there originate from an electrolysis reaction between water, which is adsorbed at the semiconductor-dielectric interface, and holes, which are present in the channel during device operation. Due to diffusion they migrate into the SiO_x layer and shield the gate electric field, which leads to bias-stress [18, 19, 20].

To further investigate the role of proton for bias-stress, we, therefore, in a first step reduced the amount of water molecules at the semiconductor-dielectric interface, which was achieved by heating the substrates during pentacene evaporation. Subsequently, several experiments with ammonia (NH_3) were performed. It was expected that NH_3 as a base would react with the protons, in full analogy to the acid-base reactions of chapter 6. This should then result in reduction or actually switching-off of the parasitic proton-induced bias-stress.

8.2 Results and discussion

The used device structure is shown in Fig. 8.1. Due to the end of a project in cooperation with Joanneum Research, where the pentacene layers investigated in the previous chapters had been produced, the vacuum evaporation was done by myself in our vacuum evaporation setup. This setup does not have a shutter and, therefore, the resulting layer thicknesses varied from batch to batch and was in the range of some 10 nm. Nevertheless, the devices showed excellent performance, in particular low hysteresis even without passivation of the SiO_x and quite high mobilities in the range of 0.1 $cm^2/(Vs)$.

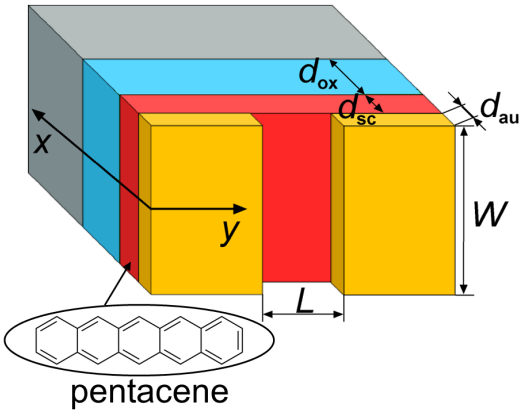

Figure 8.1: Schematic device structure of the used top-contact bottom-gate transistors, with channel length of of $L = 25\,\mu m$ and a channel width of $W = 7$ mm. The source and drain electrodes are 50 nm thick and made of gold (Au). As organic semiconductor pentacene was used, in the thickness range of some 10 nm. The substrate was doped silicon, with a 150 nm thick thermally grown SiO_x.

8.2.1 Impact of substrate heating on device performance

To investigate the influence of water adsorbed at the semiconductor-dielectric interface on the bias-stress effect two different production processes were tested. In one process the substrates first were heated up to 120 °C to reduce the amount of adsorbed water molecules and afterwards the substrates were cooled down to 60 °C was reached (for more details see Experimental section 8.4). At this temperature (T_{ve}) pentacene was vacuum evaporated. $T_{ve} =$ 60 °C, was chosen to get well ordered molecular pentacene crystallites in thin-film-phase [113]. In the other process pentacene was deposited at room temperature without heating the substrates before the evaporation step.

Impact of substrate heating on characteristic device parameters

Heating of the substrates during pentacene evaporation and before the evaporation process has no significant influence on the threshold voltage extracted in the linear region (V_{ELR}) and the logarithmic second derivative threshold voltage (V_{SDL}) (for extraction methods, see chapter 2). V_{ELR} and V_{SDL}, for devices whose pentacene film were grown at 60 °C, were in the same range as V_{ELR} and V_{SDL} for devices grown at room temperature, respectively (see Tab. 8.1). In contrast to that, the charge carrier mobility (μ) extracted in the linear region (for extraction method, see chapter 2) show a huge dependence on T_{ve}. As one can see, μ is higher in the case of heated the substrates during pentacene deposition. One reason for this behavior could be better ordered molecular pentacene crystals at elevated substrate temperatures, as reported in [113]. Another possible explanation is a reduced H_20 induced trap density, that should also result in higher μ [114]. The latter is also held responsible for the reduced hysteresis and the higher on-to-off ratio (I_{on}/I_{off}) in the case of heated substrates (see Fig 8.3) [114].

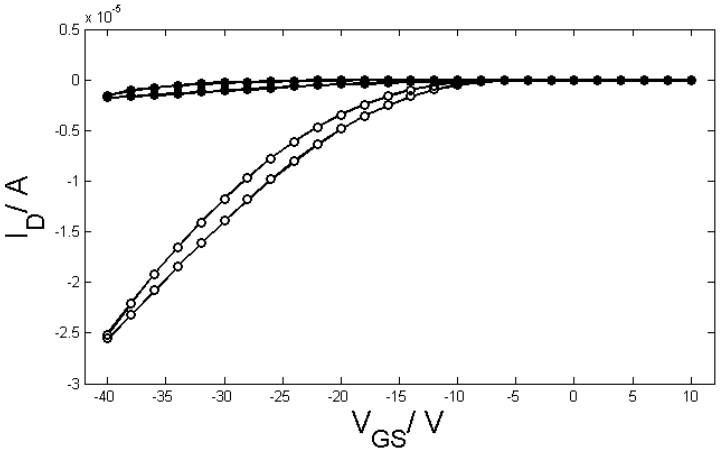

Figure 8.2: Drain current (I_D) as function of gate-source voltage (V_{GS}) for devices grow at 60 °C (open symbols) and grown at room temperature (closed symbols). The drain-source voltage (V_{DS}) was set to -2 V.

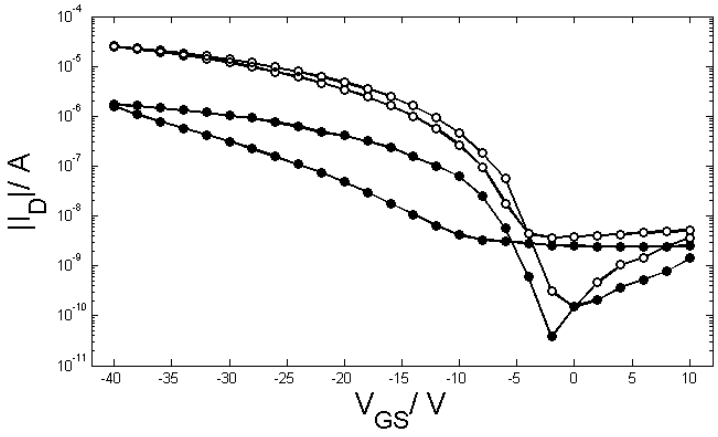

Figure 8.3: Absolute value of drain current (I_D) plotted on a logarithmic scale as function of (V_{GS}) for devices grown at 60 °C (open symbols) and grown at room temperature (closed symbols), where drain-source voltage (V_{DS}) was set to -2 V.

Table 8.1: Threshold voltages extracted from the linear region (V_{ELR}), logarithmic second derivative threshold voltages (V_{SDL}) (for extraction methods see chapter 2), mobilities extracted from the linear region (μ) and on-to-off ratios (I_{on}/I_{off}) for two different temperatures (T_{ve}), where T_{ve} is the substrate temperature during pentacene vacuum evaporation. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

T_{ve} $[°C]$	V_{ELR} $[V]$	V_{SDL} $[V]$	μ $[\frac{cm^2}{Vs}]$	I_{on}/I_{off} $[10^3]$
25	-18	0	0.09	20
60	-15	-2	0.01	5

Impact of substrate heating on bias-stress effect

Additionally, devices which were heated up to 120 °C before and heated at 60 °C during pentacene evaporation show significantly lower bias-stress, than those grown at room temperature. This can be see in Fig. 8.4. The higher initial I_D (I_{D0}) in Fig. 8.4 of the "heated" device in comparison to the "unheated" one, is due to its higher μ of the heated OTFTs. To compare the bias-stress measurements, the bias-stress curves are normalized to I_{D0} (see Fig. 8.5). The reduced stress behavior in the case of heat the substrates, can

be attributed to a lower H_2O induced trap density, which results in a lower amount of protons, originating from an electrolysis reaction of holes and H_2O molecules [18, 19, 20].

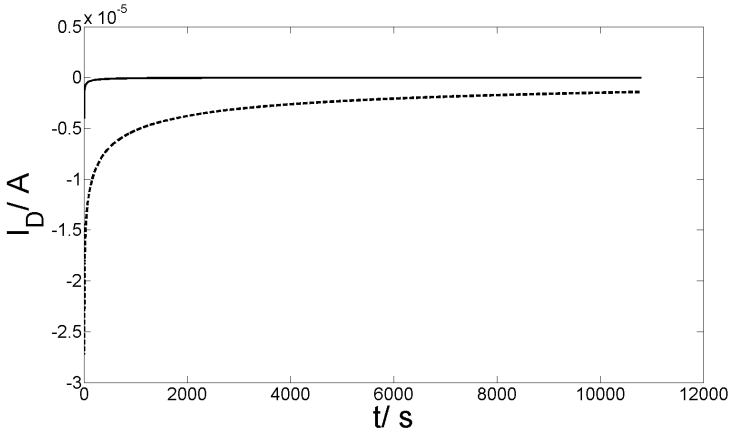

Figure 8.4: Drain current (I_D) versus time (t) for devices grown at 60 °C (broken line) and at room temperature (solid line). The drain-source voltage (V_{DS}) was set to -2 V and the gate-source voltage (V_{GS}) was set to -30 V.

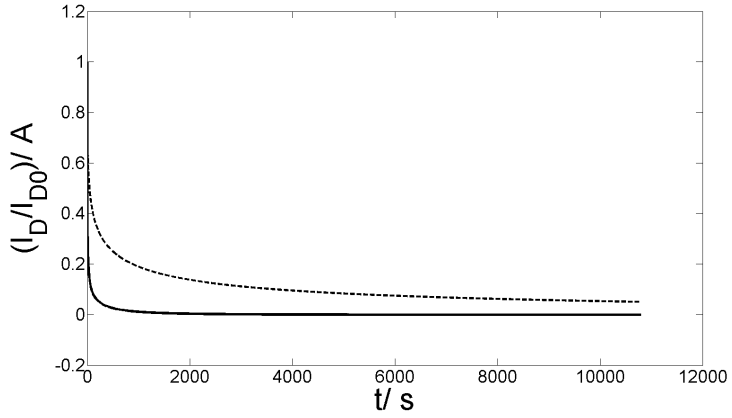

Figure 8.5: Drain current (I_D) normalized to initial drain current (I_{D0}), (I_D/I_{D0}), as function of time (t), for devices grown at 60 °C (broken line) and at room temperature (solid line). The drain-source voltage (V_{DS}) was set to -2 V and the gate-source voltage (V_{GS}) was set to -30 V.

8.2.2 Impact of exposure to ammonia on the device performance

To distinguish between the two mentioned reasons for bias-stress, which are either protons or traps, the devices were exposed to ammonia gas (NH_3) during devices operation. The motivation for doing that, was to try to reduce the stress by neutralizing the protons originating from the hydrolysis reaction of H_2O with holes with the strong base NH_3 before the protons migrate into the SiO_x dielectric. In this context it should be mentioned that in such experiments it also cannot be excluded that NH_3 also affects H_2O induced trap states that might be present at the interface. Therefore, bias-stress measurements of devices, which were exposed with NH_3 during biasing should be compared to measurements on devices, which were unbiased during NH_3 exposure.

As explained above, devices which were heated up to 120 °C before pentacene evaporation and were held at 60 °C during evaporation show significant lower bias-stress effect as devices grown at room temperature. Therefore, to have a high difference between the initial bias-stress behavior, and the bias-stress behavior of NH_3 exposed devices, in the following unheated devices were used.

Investigations on the impact of ammonia on characteristic device parameters

To characterize the devices, transfer curves were measured. As one can see in Fig. 8.6 (open circles), it was not possible to measure reliable transfer characteristics during NH_3 exposure. This is attributed to a NH_3 gas induced conductive path between source and gate electrodes, due to temporally doping of the device holder, made of poly(methyl methacrylate) (PMMA). Several weeks before the present measurements had been done even during NH_3 exposure reliable measurements had been done by Lukas Lading. But over time the PMMA sample holder gets cloudy, which indicates a chemically reaction of the PMMA and NH_3. This explanation is also supported by the high gate current (I_G) for measurements during NH_3 exposure, where this high I_G is reduced over time (see Fig 8.8).

About 0.5 h after NH_3 exposure, it was possible to measure a transfer characteristic, which displayed a very large hysteresis (closed squares Fig. 8.6 and Fig. 8.7). About 4.5 h after NH_3 exposure the hysteresis was smaller (closed triangles in Fig. 8.6 and Fig. 8.7) and μ was higher (see Tab. 8.2).

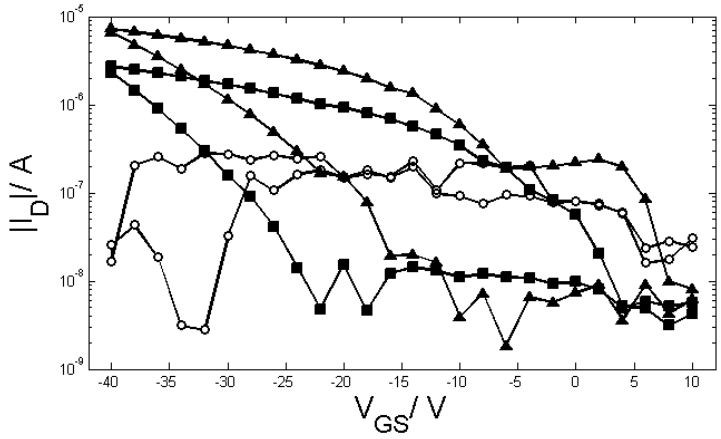

Figure 8.6: Absolute value of drain current (I_D) plotted on a logarithmic scale as a function of gate-source voltage (V_{GS}) during ammonia (NH_3) exposure (open circles), about 0.5 h after NH_3 exposure (closed squares) and about 4.5 h (closed triangles) after NH_3 exposure. The drain-source voltage V_{DS} was -2 V.

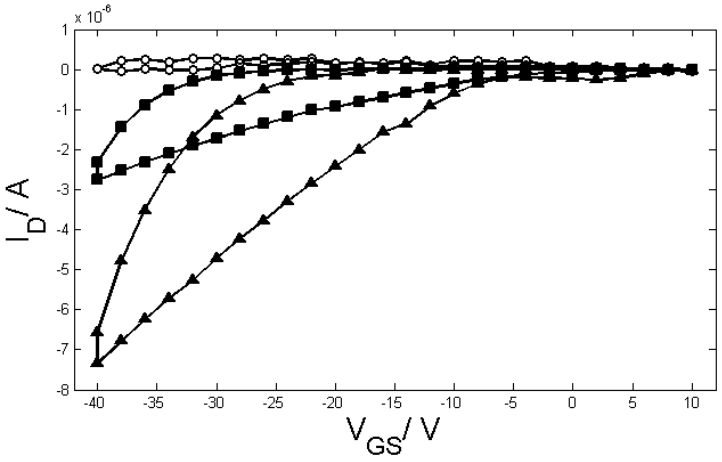

Figure 8.7: Drain current (I_D) as function of gate-source voltage (VGS) measured during (open circles) ammonia (NH_3) exposure, about 0.5 h after (closed squares) and about 4.5 h (closed triangles) after NH_3 exposure. The drain-source voltage V_{DS} was -2 V.

Table 8.2: Threshold voltages extracted from the linear region (V_{ELR}), logarithmic second derivative threshold voltages (V_{SDL}) (for extraction methods see chapter 2), mobilities extracted from the linear region (μ) and on-to-off ratios (I_{on}/I_{off}) for devices measured about 0.5 h after and about 4.5 h after exposure. This time is called Δt in the table. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

Δt $[h]$	V_{ELR} $[V]$	V_{SDL} $[V]$	μ $[\frac{cm^2}{Vs}]$	I_{on}/I_{off} $[10^3]$
0.5	-15	4	0.009	0
4.5	-13	8	0.022	0

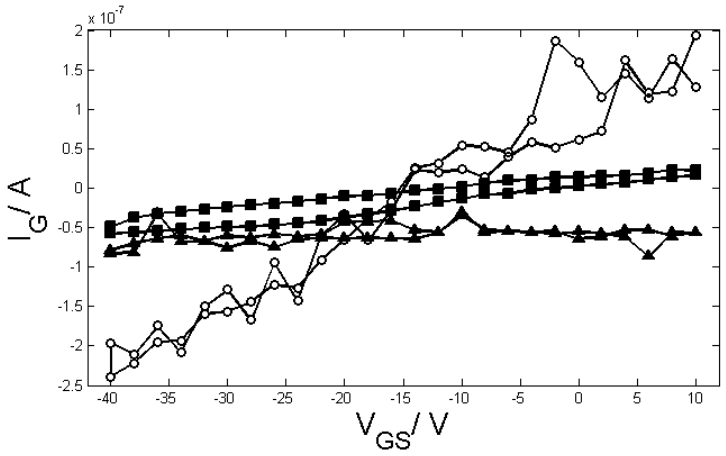

Figure 8.8: Gate current (I_G) as function of gate-source voltage (V_{GS}) during ammonia (NH_3) exposure (open circles), about 0.5 h after NH_3 exposure (solid squares) and about 4.5 h after NH_3 exposure (solid triangles). The drain-source voltage V_{DS} was -2 V. Note that I_G without NH_3 exposure are in the range of 10^{-8} A.

Due to these experimental problems during NH_3 exposure, we had to resort to a study of devices exposed NH_3 without employing any bias. As one can see from Fig. 8.9 and Fig. 8.10 there is however no significant difference in bias-stress behavior between OTFTs, which were exposed to NH_3 and such devices, which were not.

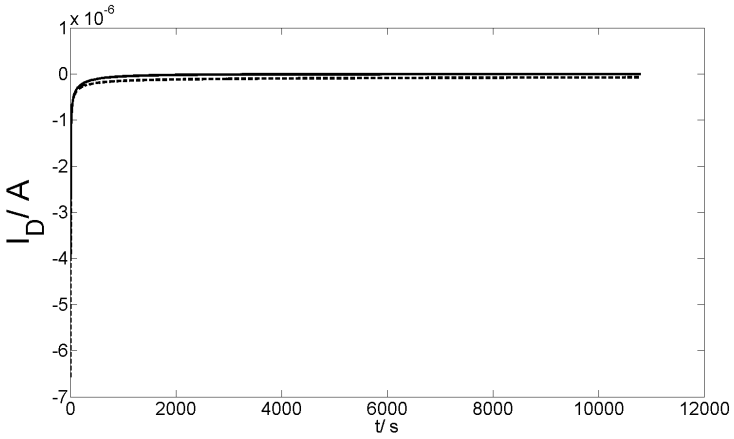

Figure 8.9: Drain current (I_D) as function of time (t), for devices grown at room temperature. The dashed line corresponds to a ammonia (NH_3) exposed device and the solid line corresponds to an unexposed device, where the drain-source voltage (V_{DS}) was set to -2 V and the gate-source voltage (V_{GS}) was set to -30 V.

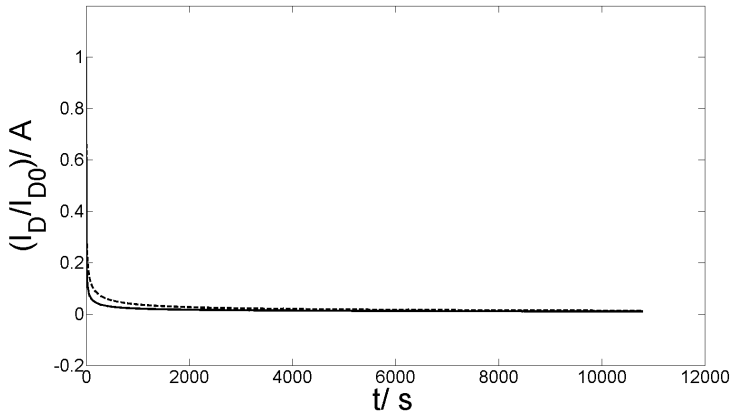

Figure 8.10: Drain current (I_D) normalized to initial drain current (I_{D0}), (I_D/I_{D0}), as function of time (t), for devices grown at room temperature. The dashed line corresponds to a ammonia (NH_3) exposed device and the solid line corresponds to an unexposed device. The drain-source voltage (V_{DS}) was set to -2 V and the gate-source voltage (V_{GS}) was set to -30 V.

8.3 Conclusion

Heating of the substrates during pentacene vacuum evaporation, impacts the OTFT behavior in several important device properties. The mobility and the on-to-off ratio are higher and the hysteresis is lower, when heating

up the substrates to 120 °C before pentacene evaporation and then holding the substrate temperature at 60 °C during pentacene deposition compared to pentacene devices grown at room temperature. Additionally, the bias-stress is lowered, which we attributed to a lower amount of water molecules adsorbed at the semiconductor-dielectric interface. Unfortunately we failed in the actual goal of the present project, which was identifying the actual mechanism responsible for bias-stress (H_2O induced traps versus proton migration) due to problems with our set-up. We, however, found, that exposure of the devices to NH_3 prior to bias-stress experiment has no effect.

8.4 Experimental

In the following the production steps of the OTFTs used in this chapter are listed in more detail.

8.4.1 Device fabrication

- cleaning the substrates in a flow box by carbon dioxide (CO_2);
- activation and cleaning of the substrates by plasma etching process (company: diener electronic, type: Femto):
  - evacuation of the plasma etching chamber to 0.2 mbar;
  - flooding the champer with oxygen (company: Air Liquide, type: Alphagaz oxygen), where the flow-meter was set to a value of 90% at an over pressure of 2.5 bar;
  - waiting until the pressure in the chamber stabilized at 0.3 mbar;
  - starting plasma etching process with a power of 100 W for 30 s;
- cleaning the substrates again in a flow box by CO_2;
- pentacene vacuum evaporation:
  - heating up the substrates in a home made vacuum evaporation setup, up to about 120 °C and holding the substrates at this temperature for 1 h;
  - cooling down to 60 °C is reached;
  - evaporating pentacene (company: Aldrich, product number: P1802-5G) at 60 °C at a pressure in the range of 10^{-6} mbar; the time to evaporated the layers was in the range of some 10 s;

- cooling down to room temperature;

- producing gold electrodes:
  - the gold (company: Oegussa, quality: fine gold plate) evaporation was done at room temperature at a pressure in the range of 10^{-6} mbar;
  - the thickness was about 50 nm, measured with quartz micro balance;
  - the time needed to deposited 50 nm, were some seconds;

8.4.2 Ammonia exposure

- during measurements
  - The devices were flooded with NH_3 (company: Linde Gas, product number: UN1005) during the electronic measurements at a pressure of 1.5 bar (see Fig. 8.6 (open circles)).
  - Afterwards the measurement cell was flooded with argon gas (company: Air Liquide, type: ALPHAGAZ ARGON 1) until it was not possible to detect NH_3 at the outlet of the exposure cell.

- before measurements
  - The devices were flooded with NH_3 for about 5 min at a pressure of 1.5 bar.
  - Afterwards the devices were flooded with argon gas, until it was not possible to detect NH_3 at the outlet of the exposure cell (see Fig. 8.9 and Fig. 8.10 dashed lines).

Chapter 9

pH-sensitive switch based on an organic inverter

9.1 Introduction

In chapter 6 it was described, that pentacene and 6,13-bis(triisopropylsilyl ethynyl)pentacene (Tips-pentacene) have significantly different properties concerning doping and dedoping with an acid and a base, respectively. In fact, bulk doping with hydrochloric acid (HCl) is possible in the case of pentacene, where it results in a shift of the threshold voltage (V_{th}) to more positive values in the case of a p-channel device. Additionally, it is possible to dedope such bulk doped pentacene based devices with the base ammonia (NH_3), which leads to a shift of V_{th} back to lower values. In contrast to that, such V_{th}-shifts were not observed in the case of Tips-pentacene. This different sensitivity of pentacene and TIPS-pentacene to HCl and NH_3 was used to build a pH-sensitive switch. This means that the device is in high voltage level after HCl exposure and in low voltage level after NH_3 exposure, respectively. It was realized by a depletion-load inverter, consisting of one pentacene based organic thin-film transistor (OTFT) and one TIPS-pentacene based device.

9.2 Results and discussion

The used OTFTs are shown schematically in Fig. 9.1. Fig. 9.2 depict a depletion load-inverter as black-box with schematic electrical wiring. At the inverter input the input voltage (V_{in}) is applied, which leads to a specific voltage on the inverter output (V_{out}). As power supply, one applies the supply voltage (V_s). The transistor which includes pentacene as active layer

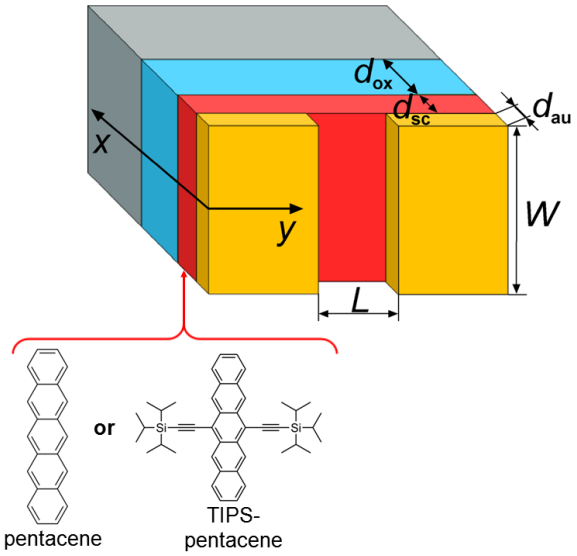

Figure 9.1: Schematic device structure of the used top-contact bottom-gate transistors, with a channel length of of $L = 25\,\mu m$ and a channel width of $W = 7\,\text{mm}$. The electrodes, source and drain, were 50 nm thick (d_{au}) and made of gold (Au). As organic semiconductor either pentacene or 6,13-bis(triisopropylsilylethynyl)pentacene (Tips-pentacene) was used, with a thickness (d_{sc}) of some 10 nm. As substrate doped silicon with a 150 nm thick (d_{ox}) thermally grown SiO_x was used.

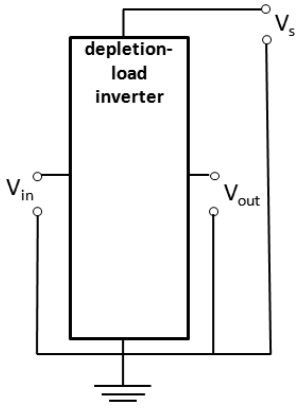

Figure 9.2: Wiring of a depletion-load inverter. V_{in} is the input voltage, V_{out} the output voltage and V_s is the supply voltage of the inverter.

material acts as load transistor and the TIPS-pentacene device is used as driver transistor. For details concerning depletion-load inverters see chapter 3.

9.2.1 Initial situation

First, transfer curve measurements of the pentacene based device and the TIPS-pentacene based device were performed. These are shown as Fig. 9.3 and Fig. 9.4.

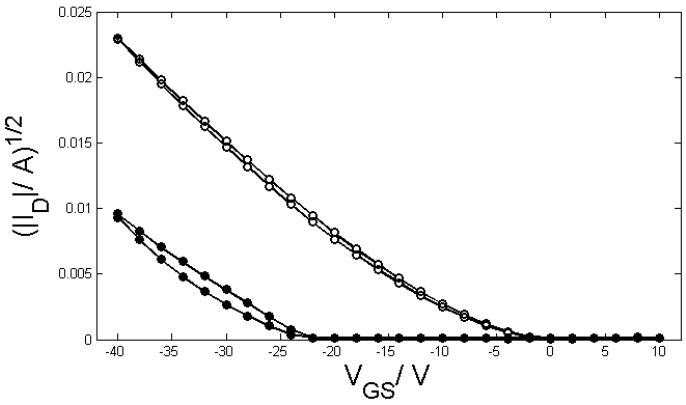

Figure 9.3: Square root of the absolute value of the drain current (I_D) as function of the gate-source voltage (V_{GS}) for a pentacene based device (open symbols) and for a 6,13-bis(triisopropylsilylethynyl)pentacene (Tips-pentacene) based device (closed symbols), measured with a drain-source voltage of $V_{DS} = -40\,\mathrm{V}$.

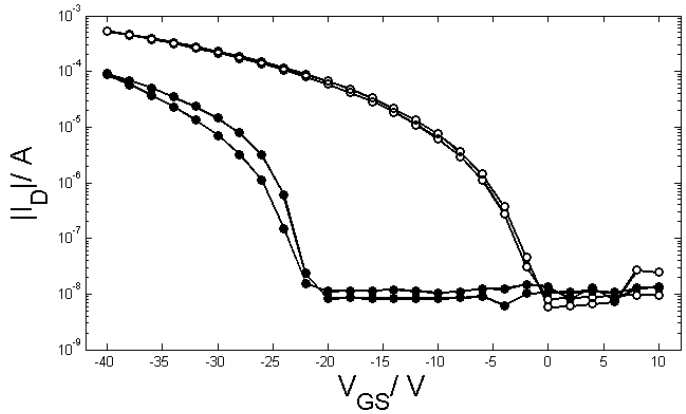

Figure 9.4: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}) for a pentacene based device (open symbols) and for a 6,13-bis(triisopropylsilylethynyl)pentacene (Tips-pentacene) based device (closed symbols), measured with a drain-source voltage of $V_{DS} = -40\,\mathrm{V}$.

Table 9.1: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}) and mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) for the pentacene (P) or TIPS-pentacene (TP) OTFTs shown in Fig. 9.3 and Fig. 9.4. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

M [1]	V_{ESR} $[V]$	V_{SDL} $[V]$	μ $[\frac{cm^2}{Vs}]$
P	-11	0	0.20
TP	-25	-22	0.13

As one can see from the extracted V_{th} values in Tab. 9.1, both devices are normally-off, for both V_{th} extraction methods. Therefore, as pointed out in chapter 3, a depletion load-inverter consisting these two devices should not show inverter functionality. This behavior is indeed reflected measuring inverter characteristics ($V_{in}(V_{out})$), which means sweeping V_{in} and measuring V_{out}.

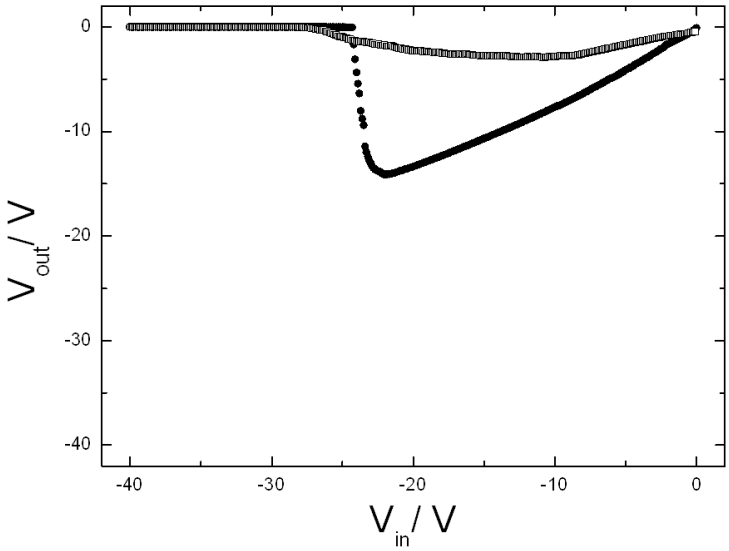

Figure 9.5: Inverter characteristic ($V_{in}(V_{out})$) of a inverter consisting of a normally-off load transistor and a normally-off driver transistor.

The crucial result of this $V_{in}(V_{out})$ characteristic of Fig. 9.5 concerning switch functionality is that a high level V_{in} (0 V) results in a high level V_{out} (0 V). To get a proper inverter functionality, the load transistor of the depletion-load transistor has to become a normally-on device. Therefore, in a next step, both devices were exposed to HCl gas, where a V_{th}-shift is expected for the pentacene device and an uninfluenced V_{th} is expected for the TIPS-pentacene devices.

9.2.2 Situation after hydrochloric acid exposure

As one can see from Tab. 9.2, the exposure to HCl for 10 s results in a significantly shift of V_{SDL} and V_{ESR} is hardly influenced in the case of pentacene devices. To clarify this behavior we show the initial curve (open symbols in Fig. 9.4) and the curve after HCl exposure (closed symbols in Fig. 9.9) together in one figure (see Fig. 9.7). It clearly show that due to HCl exposure a shoulder is growing, which indeed hardly influence V_{ESR} (see Fig. 9.6) and influences V_{SDL} significantly.

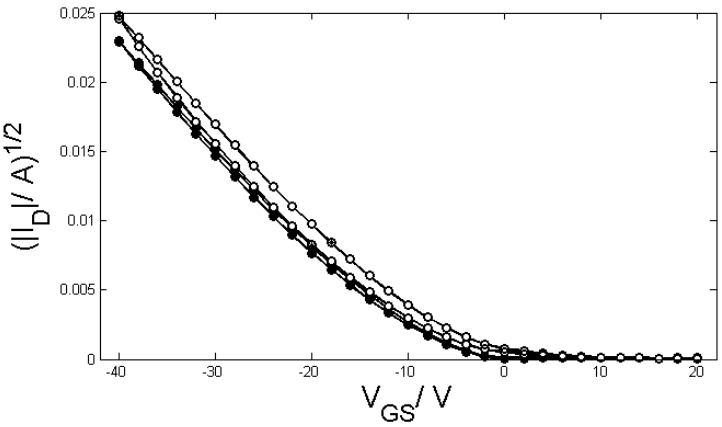

Figure 9.6: Square root of the absolute value of the drain current (I_D) as function of the gate-source voltage (V_{GS}) for a pentacene based device (open symbols) and for a 6,13-bis(triisopropylsilylethynyl)pentacene (Tips-pentacene) based device (closed symbols), measured with a drain-source voltage of $V_{DS} = -40$ V.

Moreover, when using the ESR method, a negative value for V_{th} is obtained which suggests that the device is a normally-off device. If one uses the SDL method, V_{th} is positive and, therefore, the OTFT is a normally-on device. We used the SDL method to decide between normally-on and normally-off, because as will be seen in the following (Fig. 9.12), the $V_{out}(V_{in})$

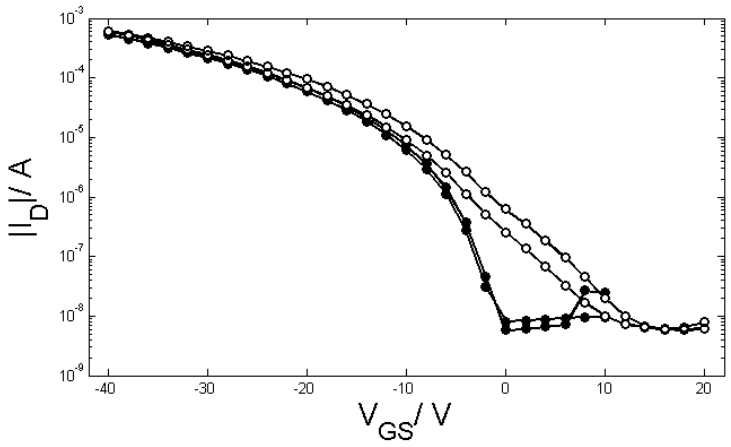

Figure 9.7: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}) for a pentacene based device (open symbols) and for a 6,13-bis(triisopropylsilylethynyl)pentacene (Tips-pentacene) based device (closed symbols), measured with a drain-source voltage of $V_{DS} = -40\,\mathrm{V}$.

characteristics showed proper inverter functionality and for depletion-load inverters this is only possible in the case of a normally-on load transistor. This choice of the V_{th}-extraction method is also supported by Fig. 9.9, where one can see a drain current I_D which is three orders of magnitude higher than the off-current, at a voltage of -9 V. The value corresponding to V_{th} when using ESR method.

Table 9.2: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}) and mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) for the pentacene (P) or TIPS-pentacene (TP) OTFTs shown in Fig. 9.3 and Fig. 9.4. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

M [1]	V_{ESR} $[V]$	V_{SDL} $[V]$	μ $[\frac{cm^2}{Vs}]$
P	-9	12	0.19
TP	-19	0	0.13

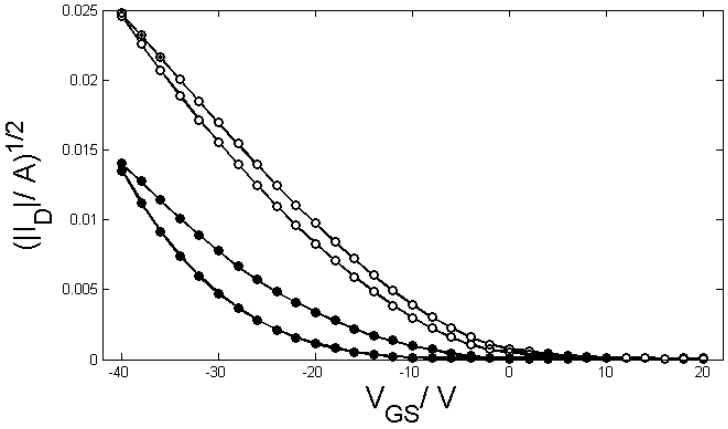

Figure 9.8: Square root of the absolute value of the drain current (I_D) as function of the gate-source voltage (V_{GS}) for a pentacene based device (open symbols) and for a 6,13-bis(triisopropylsilylethynyl)pentacene (Tips-pentacene) based device (closed symbols) after exposed the devices to hydrochloric acid (HCl) for 10 s. The measurements were performed with drain-source bias of $V_{DS} = -40$ V.

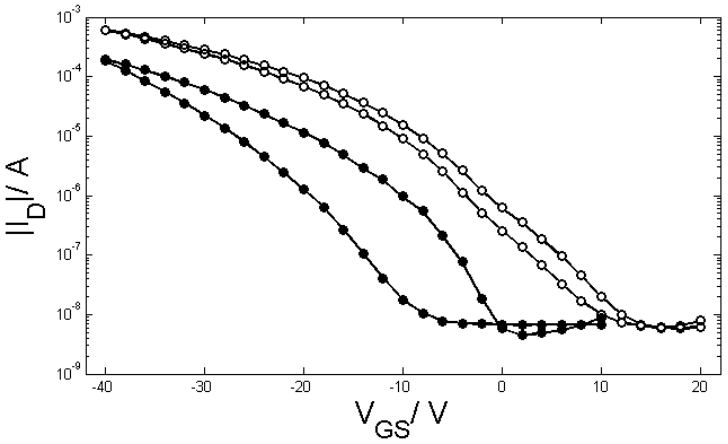

Figure 9.9: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}) for a pentacene based device (open symbols) and for a 6,13-bis(triisopropylsilylethynyl)pentacene (Tips-pentacene) based device (closed symbols) after exposed the devices to hydrochloric acid (HCl) for 10 s. The measurements were performed with drain-source bias of $V_{DS} = -40$ V.

An unexpected observation is that the TIPS-pentacene device also showed a shift of V_{th} in the direction of higher values, but they are still normally-off

devices for both extraction methods. This is at variance with the results of chapter 6. A possible explanation could be the different timescales of the experiments. While we here measured the devices right after HCl exposure (done in our lab), in chapter 6 the devices were measured between 30 minutes and a few hours after the exposure (done at the chemistry department). An alternative explanation could be a difference in the used HCl due to lab change. (for more details see Experimental section)

This assessment is indeed supported by the data shown in Fig. 9.10 and Fig. 9.11.

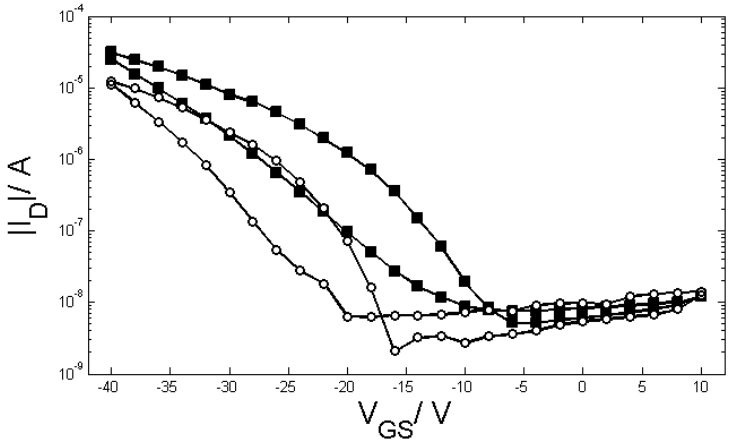

Figure 9.10: Absolute value of the drain current (I_d) plotted on a logarithmic scale as function of gate-source voltage (V_{GS}) for an unexposed device (open circle) and after 10 s exposure of the device to hydrochloric acid (HCl), measured some minutes after the exposure (closed squares). The drain-source voltage (V_{DS}) was set to $V_{DS} = -40\,\mathrm{V}$.

As one can see from the values in Tab. 9.3 extracted from the curves in Fig. 9.10 and Fig. 9.11, HCl do not influences V_{ESR} also in the case of TIPS-pentacene. As pointed out above, the important value to decide between normally-on on normally-off is V_{SDL}. This value is shifted to higher values by HCl, but this V_{th}-shift disappears with time.

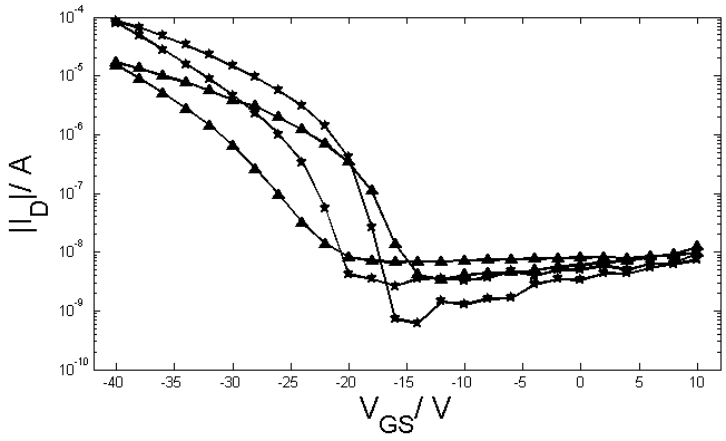

Figure 9.11: Absolute value of the drain current (I_d) plotted on a logarithmic scale as function of gate-source voltage (V_{GS}) of the same device, which was characterized in Fig. 9.10. Due to picture always double-sweep measurements which leads to hysteresis, two figures were performed to have a clear view concerning the measurement curves. The measurement indicated with closed triangles was performed after about 2 h after HCl exposure and the measurement indicated with closed stars was done 3 days after HCl exposure. The drain-source voltage (V_{DS} was set to $V_{DS} = -40\,\mathrm{V}$.

Table 9.3: Depending on the material (M), which was either pentacene (P) or TIPS-pentacene (TP), threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}) and mobilities extracted (μ) extracted from the saturation region were shown (for extraction methods see chapter 2). All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

N [1]	V_{ESR} [V]	V_{SDL} [V]
1	-23	-16
2	-21	-6
3	-23	-14
4	-24	-16

An inverter characteristics measurement for the HCl exposed pentacene and TIPS-pentacene transistors results in inverter functionality with quite large hysteresis in the inverter $V_{in}(V_{out}$ (Fig. 9.12). We attributed this to the increased hysteresis of the "double-sweep" transfer curve measurements. An

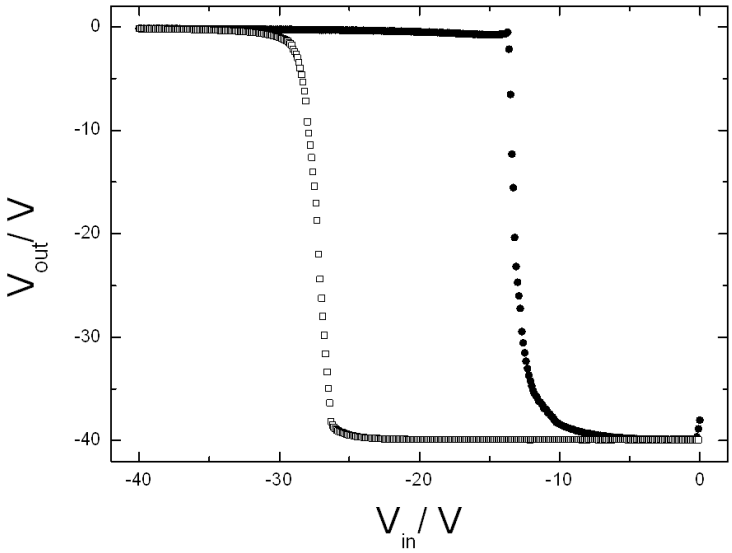

Figure 9.12: Inverter characteristic ($V_{in}(V_{out})$) of a inverter consisting of a normally-on load transistor and a normally-off driver transistor. This situation is realized by connecting HCl exposed devices.

additionally reason is the quite high bias-stress effect of the TIPS-pentacene devices. Nevertheless, a proper inverter functionally is observable, which means that a high level V_{in} (0 V) results in low level V_{out} (-40 V) and vice versa. In especially, in contrast to the situation depicted in Fig. 9.5, after HCl exposure a high level V_{in} (O V) results in a low level V_{out} (-40 V).

To get again a similar situation as the initial one, which means a high level V_{in} results in a V_{out} which is at high level too, the transistors were exposed to NH_3.

9.2.3 Situation after ammonia exposure

As one can see from the values in Tab. 9.4, where the extracted values are based on the curves of Fig. 9.13 and Fig. 9.14, V_{ESR} and V_{SDL} are shifted back to negative values, which means that the TIPS-pentacene based device as well as the pentacene based OTFT is again a normally-off device. Moreover, as shown in Fig. 9.15 exposure to NH_3 again results to a $V_{in}(V_{out})$ characteristics as the one contained in Fig.9.5 before gas exposure. Concerning switch functionality high level V_{in} again results in a high level V_{out}.

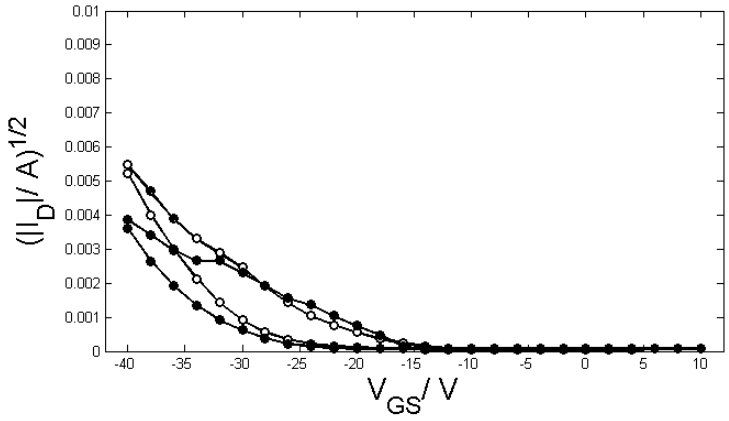

Figure 9.13: Square root of the absolute value of the drain current (I_D) as function of the gate-source voltage (V_{GS}) for a pentacene based device (open symbols) and for a 6,13-bis(triisopropylsilylethynyl)pentacene (Tips-pentacene) based device (closed symbols) after ammonia (NH_3) exposure for 1 min. The measurements were performed with drain-source bias of $V_{DS} = -40$ V.

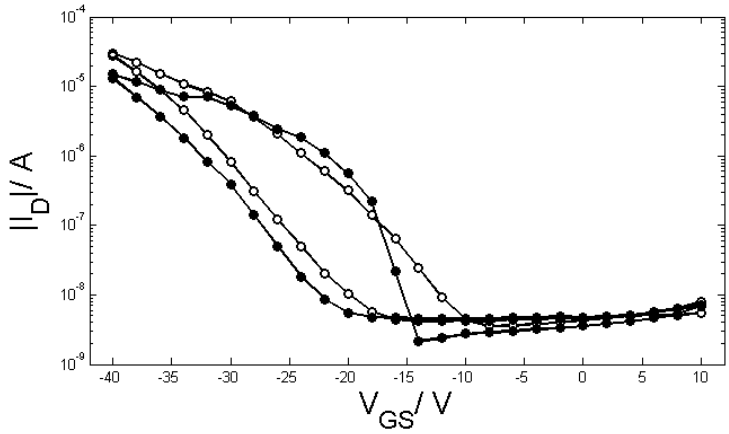

Figure 9.14: Absolute value of the drain current (I_D) plotted on a logarithmic scale as function of the gate-source voltage (V_{GS}) for a pentacene based device (open symbols) and for a 6,13-bis(triisopropylsilylethynyl)pentacene (Tips-pentacene) based device (closed symbols) after ammonia (NH_3) exposure for 1 min.. The measurements were performed with drain-source bias of $V_{DS} = -40$ V.

Table 9.4: Threshold voltages extracted from the saturation region (V_{ESR}), logarithmic second derivative threshold voltages (V_{SDL}) and mobilities extracted from the saturation region (μ) (for extraction methods see chapter 2) for the pentacene (P) or TIPS-pentacene (TP) OTFTs shown in Fig. 9.3 and Fig. 9.4. All values are extracted from the downward sweep (measured first and characterized by a higher current at a given voltage).

M [1]	V_{ESR} $[V]$	V_{SDL} $[V]$	μ $[\frac{cm^2}{Vs}]$
P	-26	-10	0.05
TP	-23	-14	0.02

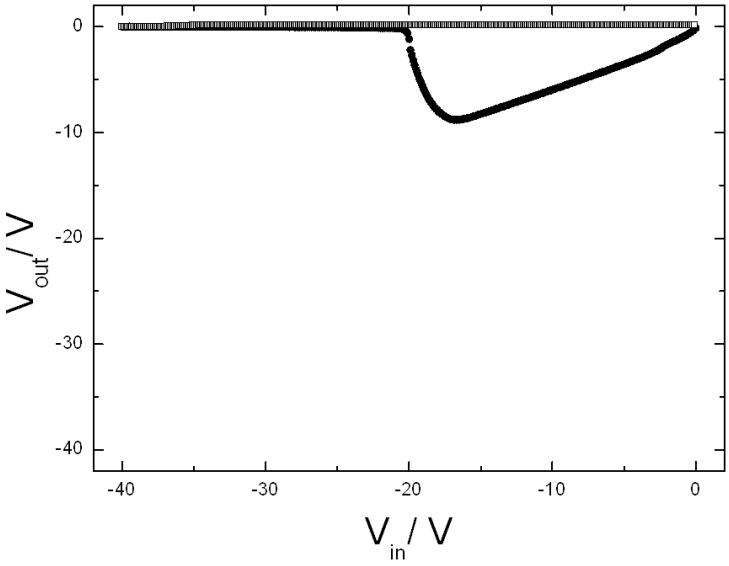

Figure 9.15: Inverter characteristic ($V_{in}(V_{out})$) of a inverter consisting of a normally-off load transistor and a normally-off driver transistor.

9.3 Conclusion

We could realize a pH-sensitive switch, based on an organic depletion-load inverter. Starting from an initional situation, where a high level input results in a high level output signal, proper inverter characteristics is realized through exposure to HCl. This is compensated by NH_3. In other words, the output signal flips from high level state to low level state due to acid exposure and from low level state to high level state due to base exposure.

9.4 Acknowledgments

We thank Thomas Rothländer and Barbara Stadlober from Joanneum Research in Weiz to provide their expertise and their measuring setup concerning inverters.

9.5 Experimental

9.5.1 Device fabrication

Pentacene and TIPS-pentacene devices were made like described in chapter 8.

9.5.2 Hydrochloric acid exposure

The ready made devices were held over beaker filled with fuming hydrochloric acid (company: Sigma-Aldrich, product number: 84422) for 10 s in contrast to chapter 6, where we used a different HCL (company: Sigma-Aldrich, product number: 30721).

9.5.3 Ammonia exposure

- The devices were flooded with NH_3 (company: Linde Gas, product number: UN1005) for about 1 min at a pressure of 1.5 bar with a volume flow of about 8 l/h.
- Afterwards the devices were flooded with argon gas (company: Air Liquide, type: ALPHAGAZ ARGON 1), until it was not possible to detect NH_3 at the outlet of the exposure cell.

9.5.4 Electronic characterization

Transfer characteristics

Transfer curve measurements were performed by our dual source-meter (company: Keithley, type: 2636A) controlled with a home-made software.

Inverter characteristics

They were done with parameter analyzer (company: mb technologies GmbH, type: only one type without special name available) and the associated software.

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series. Considering, however, that $d_{T-SC/SA}$ amounts to less than 1% of the overall thickness of all dielectrics and that its dielectric constant is roughly one third of that of SiO_x its influence can be safely neglected.

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