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# Development of an Ultra-Low Voltage Digital Cell Library to Reduce the Startup Voltage of Thermoelectric Harvesting Systems in Body Area Networks

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## Abstract

Wireless sensor nodes have gained increasing interest in recent years as they enable flexible networks for control and monitoring in the field of industrial and home automation systems. Another field of application is medical diagnostics where in- and on-body sensor nodes can be used for continuous monitoring of vital parameters of patients with chronic diseases in their home environment which reduces the amount of in-hospital medical checkups. Those such devices are typically very small and consist of a measurement unit, a processor, a wireless communication unit and a local power supply. A frequently addressed problem in the field of sensor nodes is their limited operation time due to the limited energy storage capability which causes unwanted maintenance effort.

The scope of this thesis is the development of a fully integrated thermoelectric energy harvesting circuit for on-skin sensors in body area networks and covers the complete development flow. This thesis begins with the development of a thermoelectric equivalent circuit diagram to allow power output optimization. This follows investigations into the characteristics of the human body as a heat source. As thermoelectric energy sources on the human body are known to provide a low output voltage, the next part deals with the development of an ultra-low voltage digital cell library which allows operation in the deep sub-threshold region at 90 mV to 1.2 V and functionality over a wide temperature range. Due to their characteristics, on-skin sensors can be directly operated from the voltage provided by the thermoelectric generator and this then enables the system to self-start. The third topic to be discussed is the power conversion stage which has to be self-sustaining. Consequently, an analytical model of a self-sustaining charge pump was then developed, to calculate the optimum number of stages to achieve high power conversion efficiency. Finally, the implementation of the complete system on silicon is described in detail. It starts to become functional at an input voltage of 90 mV and generates a nominal output voltage of 1.2 V from a voltage of 140 mV provided by the thermoelectric generator. After the startup the output voltage remains steady down to 110 mV at the input node.

In this thesis three test chips were carried out using an Infineon 130 nm low-cost CMOS process. All implementations were done without using any special process options, e.g. low-$V_{TH}$ transistors.

# Kurzfassung

Drahtlose Sensorknoten erfahren zunehmendes Interesse in den letzten Jahren da sie flexible Netzwerke zur Überwachung und Steuerung im Bereich von Industrie und Heimautomatisierungssystemen ermöglichen. Ein weiteres Anwendungsgebiet ist die medizinische Diagnostik durch Sensoren im Körper und auf der Haut, welche zur Langzeitüberwachung von Patienten mit chronischen Erkrankungen im häuslichen Umfeld verwendet werden können und die Anzahl der Kontrolluntersuchungen in Krankenhäusern reduzieren. Diese Sensorsysteme sind üblicherweise sehr klein und bestehen aus einer Messeinheit, einem Prozessor, einer drahtlosen Kommunikationsschnittstelle und einer lokalen Energieversorgung. Ein häufig auftretendes Problem von Sensorknoten ist die limitierte Betriebsdauer aufgrund des begrenzten Energiespeichers, was den Wartungsaufwand erhöht.

Diese Dissertation beschäftigt sich mit der Entwicklung einer vollständig integrierten thermoelektrischen harvesting Schaltung für Sensoren auf der Haut in Körpernetzwerken und deckt sämtliche Bereiche der Entwicklung ab. Zu Beginn erfolgen Untersuchungen zu Eigenschaften des menschlichen Körpers als Wärmequelle, um ein thermoelektrisches Ersatzschaltbild zur Optimierung der Ausgangsleistung zu entwickeln. Thermoelektrische Energiequellen am menschlichen Körper sind bekannt für ihre geringe Ausgangsspannung. Daher beschäftigt sich diese Arbeit im nächsten Schritt mit der Entwicklung einer digitalen Schaltungsbibliothek für einen Versorgungsspannungsbereich im tiefen sub-threshold Bereich, startend ab 90 mV bis 1.2 V und einer Funktionalität über einen weiten Temperaturbereich. Aufgrund ihrer Eigenschaften kann die Logik direkt mit der Ausgangsspannung des Thermogenerators betrieben werden. Dies ermöglicht ein selbststartendes System. Das dritte Thema zur Diskussion behandelt die selbsterhaltende Spannungswandlungsstufe. Dazu wird zuerst ein analytisches Model der selbsterhaltenden Ladungspumpe entwickelt, um die optimale Anzahl der Stufen für maximale Wandlungseffizienz zu berechnen. Anschließend wird die Implementierung des Systems auf Silizium im Detail beschrieben. Es beginnt ab einer Eingangsspannung von 90 mV zu arbeiten und erzeugt eine nominale Ausgangsspannung von 1.2 V ab einer vom thermo-elekrischen Generator erzeugten Spannung von 140 mV. Nach erfolgtem Start wird die nominale Ausgangsspannung bis zu einer Eingangsspannung von 110 mV gehalten.

In der Disseration werden drei Testchips vorgestellt, welche in einem Standard Infineon 130 nm CMOS Prozess implementiert wurden. Dabei wurde auf speziellen Prozessoptionen, wie z.B. Low-$V_{TH}$ Transistoren, verzichtet.

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# Chapter 1

# Introduction

## 1.1 Motivation

The Internet-of-Things and Machine-to-Machine communication are terms that are frequently used nowadays when talking about future developments in home automation and human assistance systems. The idea is to equip physical objects we use in our daily life with embedded computing systems to achieve a greater value. Wireless Sensor Networks are part of this technology and consist of distributed sensor nodes that monitor physical or environmental conditions. In medical applications, Wireless Senor Networks are typically called Body Area Networks and enable the continuous monitoring of vital parameters of patients with chronic diseases, even in domestic surroundings. These nodes typically consist of a local power source, a sensor and a processing unit as well as an RF-interface. A frequently addressed issue in Wireless Sensor Networks is the power supply which is typically realized by using finite energy sources which leads to a high maintenance effort. A solution to this problem is energy harvesting or scavenging which is the approach of deriving electric power locally from different environmental sources (e.g. solar power, thermal energy, electromagnetic energy, kinetic energy, ...) and enables battery-less operation. A recently published summary of characteristics and research achievements can be found in Proceedings of IEEE (Issue 11, Nov. 2014). Energy harvesting systems suffer from a generic approach and finding a suitable source requires careful investigation into the corresponding application scenario. A detailed investigation of feasible harvesting sources found on the human body is carried out in [26] and a brief summary of the characteristic is given in Table 1.1. Photovoltaics can rarely be used, as 90 % of the skin is typically covered by clothing. Clothes are no barrier for RF-signals but their energy density rapidly decreases with increasing distance from the transmitter. So, to provide sufficient power to an on-skin sensor a powerful RF source needs to be installed not too far away. Kinetic harvesters represent an unpredictable source with irregular power output which relies on people's mobility. The only stable energy source of a human being is the body temperature which is typically about 10 °C higher than the ambient air. It is therefore the aim of this thesis to develop a fully integrated thermoelectric energy harvesting interface with self-starting capabilities. The thesis presents the full scope of the development, starting from the physical background of the harvesting principle right through to the complete system integration on silicon.

| | Characteristics | Suitability in Body Area Networks |
|---|---|---|
| Optical Energy | + high efficiency outside<br>+ good scalability<br>+ flexible organic cells<br>o moderate efficiency inside<br>- no power generation overnight | + usable in “intelligent clothes”<br>o limited applicability in on-skin sensors (≈ 90 % of the skin is typically covered)<br>- not for implanted devices |
| RF Energy | + simple and cheap realization<br>- power output 100-1000 times lower than alternative sources<br>- bad reputation of ”electric smog” | + wireless power transmission through skin barrier to power implants |
| Kinetic Energy | + simple design<br>+ low costs of macroscopic devices<br>o unsteady source<br>- bad scalability (MEMS technology necessary) | + implantable |
| Thermal Energy | + body heat is a constant source<br>o high costs of thermal electric generators<br>o power conversion challenging due to low output voltage | + usable for on-skin sensors<br>- unusable for implanted sensors |

Table 1.1: Comparison of different harvesting sources in Body Area Networks.

## 1.2 Organization of the Thesis

Chapter 1 deals with the basics regarding thermoelectric energy harvesting in Body Area Networks. The characteristics of a thermoelectric generator are discussed through investigation of the thermal and electrical properties of the device. As the power conversion efficiency highly depends on the thermal resistances of the entire system in an application scenario a literature study is performed to provide the corresponding data for the human body. Finally a simple model combining the thermal and electrical is developed which allows estimation of the power conversion efficiency in dependency on the parasitic thermal resistances of the complete harvesting system.

The development of digital logic gates so that they are functional in the deep sub-threshold region is presented in Chapter 2. It starts with investigations into the behavior of MOS transistors in this operation region. Then, a leakage compensation technique is introduced which allows a significant reduction in the minimum supply voltage of CMOS gates without requiring special process options or post-fabrication steps. The principle is used to develop an ultra-low voltage digital cell library which contains inverter, NAND- and NOR-gates as well

as flip-flops. The functionality of interconnected gates is demonstrated with measurements of basic digital circuits over a wide temperature range.

In Chapter 3 an analytical model of fully integrated charge pumps for ultra-low voltage inputs is derived. It considers the impact of stray capacitances as well as the control effort which is caused by the self-sustaining operation. Expressions for voltage gain, efficiency and optimum number of stages are derived which allows optimization during the design flow.

Chapter 4 combines the achievements of the previous chapters by presenting the design of a fully integrated thermoelectric energy harvesting system with self-starting capabilities. The ultra-low voltage digital logic cells enable an autonomous start in the deep sub-threshold region. By using the analytical model of chapter 3 the entire system is implemented in a chip area and power efficient way which is proven by measurements of multiple samples.

Finally, Chapter 5 summarizes the achievements of the thesis and provides a conceptual system design for a smart booster antenna skin patch based on thermoelectric energy harvesting for continuous data logging of conventional implanted passive sensor grains.

## 1.3 Thermoelectric Energy Harvesting

The thermoelectric effect, or Seebeck effect was first discovered by Thomas Johann Seebeck in 1821 and describes the direct conversion of a temperature gradient induced heat flow into electric power. Interconnecting two dissimilar materials and forcing their interconnects to be different temperatures results in a diffusion current from the hot to the cold side (and vice versa) in order to reach energy equilibrium. Due to the higher speed of hot charge carriers compared to cold ones an electric field and therefore a measurable voltage is developed. Its value depends on material properties expressed by the Seebeck coefficient ($\alpha^*$) and decreases with charge carrier concentration. In metals it is typically less than $30\,\mu V/K$ and in semiconductors a few $100\,\mu V/K$ [10]. To compare different materials a figure of merit ($Z$) was employed in 1949 by A.F. Ioffe [70], taking into account electrical ($\sigma$) and thermal ($\lambda$) conductivity of thermocouples (1.3.1). Consequently a well performing thermoelement provides a low thermal conductivity to increase the temperature gradient across the device, a high electrical conductance to reduce the Joule heating losses and a high Seebeck coefficient.

$$Z = \alpha^2 \frac{\sigma}{\lambda} \tag{1.3.1}$$

Isolators typically provide the lowest thermal conductivity combined with a very high electrical resistivity, making them inapplicable in thermocouples. Metals on the other hand are excellent electrical and heat conductors, which again leads to a low $Z$. A trade-off is semiconductor material which provides a low thermal and in case of proper doping a relatively high electrical conductivity in addition to an attractive $\alpha$. Therefore the latter is widely used in thermoelectric power generation. Since all parameters of $Z$ are in fact temperature dependent, different operation temperature regions require certain materials. At room temperature bismuth telluride

* $\alpha$ is defined by the differential Seebeck coefficient of two materials in a thermocouple

($Bi_2Te_3$) is the state-of-the-art thermoelectric material outside laboratories providing a $Z$ of $0.003\,\mathrm{K}^{-1}$ [61]. In order to improve $Z$ scientists are focusing on the development of new materials and low-dimensional structures (e.g. nanowires). It is expected by J.H. Goldsmid that $Z$ will be improved by a factor of 4 in the near future and up to a factor of 20 in the long term [18].

An important aspect in thermoelectric power generation is the optimum conversion efficiency ($\eta_{max}$) of a thermoelectric device which is generally determined by the electrical power output at a certain thermal input. It can be shown that for small gradients, where temperature independency can be assumed, $\eta_{max}$ is given by (1.3.2) [64]. The first expression in (1.3.2) is the Carnot factor ($\eta_c$), well known from thermodynamics to describe the fundamental limit of ideal heat engines. It depends on the difference in temperature of the hot side ($T_H$) and the cold side ($T_C$) divided by $T_H$. The second expression is called reduced efficiency ($\eta_r$) and considers the device properties multiplied by the average temperature $\overline{T} = (T_H - T_C)/2$.

$$\eta_{max} = \eta_c \cdot \eta_r = \frac{T_H - T_C}{T_H} \cdot \frac{\sqrt{1 + Z\overline{T}} - 1}{\sqrt{1 + Z\overline{T}} + \frac{T_C}{T_H}} \tag{1.3.2}$$

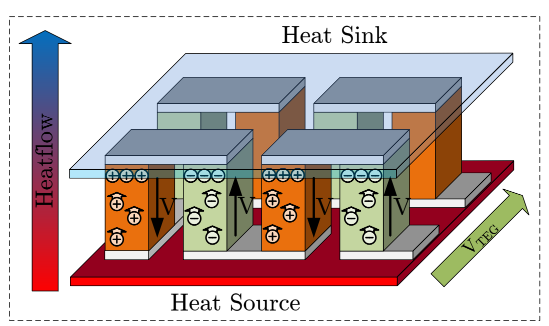
In order to get a rough estimation of the achievable efficiency using on-body applications, values are inserted in the above formula. Assuming a body temperature of $T_H$=310 K in an ambient environment of $T_C$=300 K results in a Carnot factor of about 0.032. Taking into account $Z$ of $Bi_2Te_3$ further reduces this result to 0.0056. In other words, just about 0.56 % of the delivered thermal power is converted to electrical power. It has to be noted that this calculation neglects additional parasitic parameters e.g. thermal resistances of the heat source and sink.

### 1.3.1 System Architecture of a Thermoelectric Generator

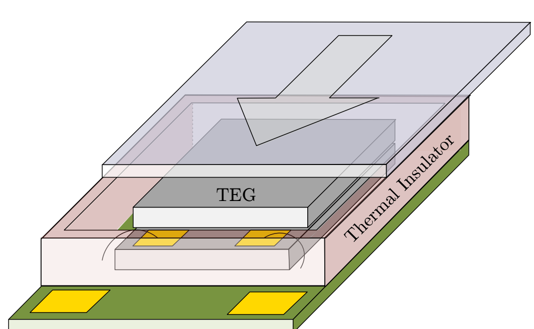
A simplified schematic of a thermoelectric generator (TEG) is shown in Figure 1.1a. The structure is similar to a Peltier heat pump, used in small refrigerators. It is built of an array of thermocouples arranged vertically in between a non conducting heat absorber and rejection ceramic plate. As a result the elements of the device are connected thermally in parallel and electrically in series. In semiconductor thermoelectric materials the majority carriers drift to the cold side. Therefore doping influences the sign of the Seebeck coefficient. By alternating n- and p-type elements the voltage contribution of all pillars add up while the entire temperature gradient is applied to each element. As shown in (1.3.3) the open circuit output voltage ($V_{TEG_{open}}$) of a thermoelectric generator depends on the number of pillars ($N$), $\alpha$ and the temperature gradient across the device ($\Delta T_{TEG} = T_H - T_C$).

$$V_{TEG_{open}} = N\alpha\Delta T_{TEG} \tag{1.3.3}$$

In principle any voltage per kelvin ratio is feasible by choosing a proper $N$, but each thermocouple adds electrical resistance while providing an additional heat path which effects the overall device performance. This trade-off will be discussed later in this thesis.




(a) Schematic of a thermoelectric generator




(b) Model of a packaged device

Figure 1.1: Internal structure of a thermoelectric generator, typically provided in a package.

| | MPG-D751 |
|---|---|
| Dimension | 4.248 mm × 3.364 mm |
| Thickness | 1.090 mm |
| Number of Pillars | 540 |
| Thermal Resistance @ 85 °C | 12.5 K/W |
| Electrical Resistance @ 23 °C | 300 Ω |
| Output Voltage | 140 mV/K |

Table 1.2: Characteristic data of the MPG-D751 thermoelectric generator [49].

Manufacturers of commercially available thermoelectric generators are using hundreds of thermocouples in order to reach a reasonable output voltage. Additionally a package is required to protect the generators from mechanical stress. It is typically the same sandwich architecture of two heat conducting plates, separated by thermally isolating sidewalls (Figure 1.1b). In this thesis a commercially available thin film thermoelectric generator from Micropelt GmbH is used. The device MPG-D751 is originally designed for wireless sensor nodes in industrial applications and provides a relatively high output voltage per Kelvin ratio. Due to its small physical size it is a suitable candidate to power on-skin sensor nodes of Body Area Networks. Table 1.2 shows the characteristics taken from the data sheet [49].

### 1.3.2 Thermoelectric Equivalent Circuit Diagram and Power Optimization

A thermoelectric generator converts thermal energy into electrical power. Therefore its model has to consider the thermal and electrical properties in order to optimize the device in both directions. V. Leonov did a lot of research in this area by investigating thermoelectric generators in Body Area Networks [38–40, 43]. He stated the importance of matching the thermal resistance of a device to the environment by design. Derived from his work an equivalent circuit diagram, respecting the thermal and electrical relationship, is given in Figure 1.2.

The device can be represented by a temperature dependent voltage source having an internal

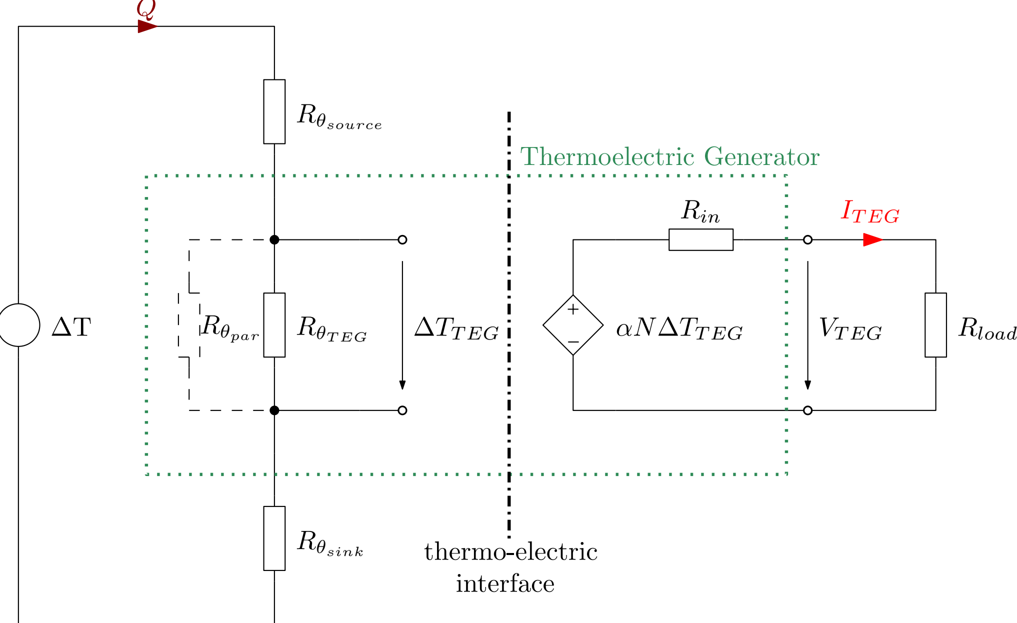



Figure 1.2: Equivalent circuit diagram of a thermoelectric generator.

series resistance ($R_{in}$) which increases with the number of thermocouples. Applying a load ($R_{load}$) results in a current ($I_{TEG}$) and an output voltage, defined by the ratio of the resistive divider (1.3.4).

$$V_{TEG} = V_{TEG_{open}} \frac{R_{load}}{R_{load} + R_{in}} \tag{1.3.4}$$

In the thermal domain, a difference in temperature ($\Delta T$) is generated by a heat source (e.g. human metabolism) and initializes a heat transfer $Q$ to the sink (e.g. ambient air). Similarly to Ohm's law the height of $Q$ is defined by the ratio of the gradient and the thermal resistance of the heat path. In this simplified model the latter is represented by three thermal resistors. While $R_{\theta_{source}}$ includes the body-to-TEG resistance (human tissue, skin, ...), $R_{\theta_{sink}}$ is mainly given by the junction resistance to the ambient air. The third one ($R_{\theta_{TEG}}$) is introduced by the device itself and decreases with the number of thermocouples. $R_{\theta_{par}}$ represents the parasitic heat path from the bottom to the top plate defined by the thermal conductance of the air and the thermally isolating sidewalls of the package. In macro-scale devices $R_{\theta_{par}}$ is typically much higher compared to $R_{\theta_{TEG}}$. In Figure 1.2 it is therefore just added for the sake of completeness and will be neglected in further investigations.

As it can be seen from the equivalent circuit diagram in Figure 1.2, a difference in temperature alone is not sufficient to generate electric power. It requires a heat flow from the source to the sink causing a temperature gradient across the device (1.3.5). Due to the thermal resistances of source and sink the effective temperature gradient applied to the thermoelectric generator is less than provided by the heat source. This is especially an issue in Body Area Networks where

$R_{\theta_{sink}}$ and $R_{\theta_{source}}$ are typically much larger than $R_{\theta_{TEG}}$. As a result a low output voltage must be addressed in such an application.

$$\Delta T_{TEG} = Q\, R_{\theta_{TEG}} = \frac{\Delta T}{R_{\theta_{TEG}} + R_{\theta_{sink}} + R_{\theta_{source}}} R_{\theta_{TEG}} \tag{1.3.5}$$

To calculate the power generated by a thermoelectric generator, (1.3.5) is substituted into (1.3.3) and the latter into (1.3.4) in order to get the output voltage under load conditions. Using $V_{TEG}$ the delivered power is given by (1.3.6).

$$P_{load} = \frac{{V_{TEG}}^2}{R_{load}} = N^2 \alpha^2 \Delta T^2 \frac{{R_{\theta_{TEG}}}^2}{(R_{\theta_{TEG}} + R_{\theta_{sink}} + R_{\theta_{source}})^2} \frac{R_{load}}{(R_{in} + R_{load})^2} \tag{1.3.6}$$

Due to the fact that in (1.3.6) the parameters $N$, $\alpha$, $R_{\theta_{TEG}}$ and $R_{in}$ are device specific, there are only a few opportunities left for optimization. According to the maximum power theorem, one way is to align the load to the inner resistance of the device [5]. Another option is to minimize the parasitic thermal resistances $R_{\theta_{source}}$ and $R_{\theta_{sink}}$. In industrial applications this is achieved by mounting the thermoelectric generator close to the heat source and applying a large radiator. This approach is only suitable to a limited extent in Body Area Networks as the thermal resistance of the source is defined by the human body and a large radiator is inapplicable due to size restrictions.

To demonstrate the effect of parasitic thermal resistances, the power delivered by a single MPG-D751 to a matched load is shown in Figure 1.3. For calculation purposes, device specific parameters are taken from Table 1.2 and inserted in equation (1.3.6). $P_{load}$ is plotted as a function of the normalized thermal resistance of the ambiance with respect to $R_{\theta_{TEG}}$. In the figure each curve represents another difference in temperature seen from the source to the sink. Since in industrial applications the parasitic thermal resistances are typically low, an output power in the milliwatt range is feasible. Unlike Body Area Networks where due to the high ratio less than 100 µW can be expected. Considering the thermal path during the design phase of a sensor node is therefore of great importance.

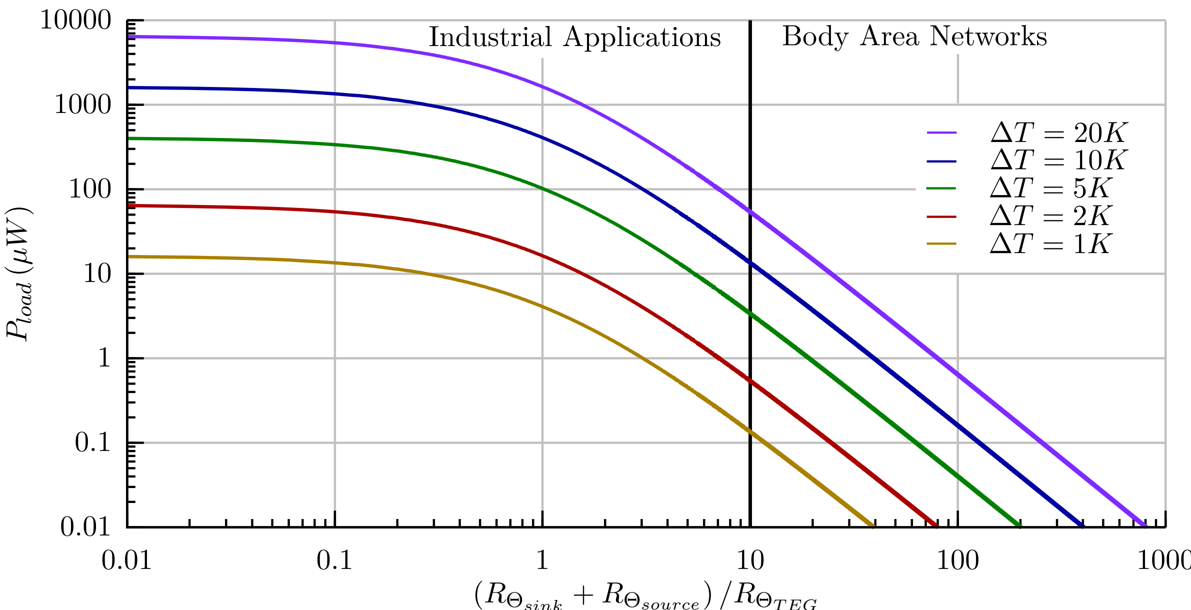



Figure 1.3: Estimated power delivered to an electrically matched load by a thermoelectric generator at different temperature differences.

## 1.4 Thermal Resistance of the Human Body

The human body continuously generates heat from metabolic processes and mainly dissipates it by convection and radiation through the skin to the environment. In order to keep the core temperature at about 310 K, blood circulation distributes excess thermal energy to peripheral regions using a network of blood vessels. Temperature regulation is achieved by changing the flow rate through vascular constriction and dilatation. As a result the thermal resistance of the human body is variable and depends on body mass, environmental conditions and the activity level. Location plays another important role. Muscles and body fat insulate the blood vessels from the ambient temperature and increase the thermal resistance in certain regions. This was confirmed by measurements performed in [41, 42] where the typical thermal resistance is given at different places on the human body. Arms, legs and the lower trunk are highly resistive while, for example, the forehead, inner wrist and chest provide a value five to ten times lower. Therefore those locations are more suitable for energy harvesting. The results are summarized in Figure 1.4.

From medical literature the basal metabolic rate is known to be about 2.9 kW h per day for a sitting human of 75 kg. Assuming a body surface of 2 $m^2$ results therefore in a mean heatflow of 6 $mW/cm^2$. In order to concentrate the heatflow in a certain area, a lower resistive path to the environment can be established by applying a radiator. As shown in [38], the body resistance significantly reduces with the heatflow. This might be caused by a compensation activity of the body. Directing thermal energy away from the body reduces the temperature locally. To counteract, the diameter of the blood vessels enlarges in this area to provide a

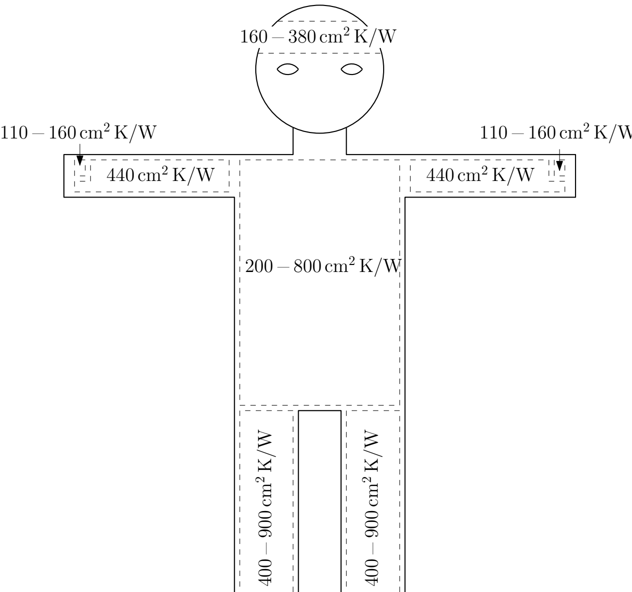



Figure 1.4: Typical values of the thermal resistance on the human body as published in [41, 42].

higher amount of energy. Therefore applying a radiator not just influences the surface to the ambient temperature, but causes some kind of positive feedback which helps to increase the power output of a thermoelectric generator. However increasing the heatflow beyond a certain level results in an uncomfortable sensation of coldness. According to [38], it should therefore be limited to $15 - 25\,\mathrm{mW/cm^2}$.

# Chapter 2

# Development of an Ultra-Low Voltage Digital Logic Cell Library

*The following chapter is mainly taken from [27], [28], [29] and [30] (own publications).* ■

## 2.1 Minimum Supply Voltage of Digital Logic Cells

The complexity of electronic circuits is steadily increasing and with it the number of transistors in electronic circuits is also constantly increasing too. Efficiency enhancement is therefore of great importance in order to minimize power consumption, especially in portable systems with limited power budget. The conventional method of reducing the switching losses by lowering the supply voltage affects the drive strength and therefore the propagation delay. As a consequence the time required to finish an operation is extended. Leakage energy is proportional to the time required for a certain operation. Therefore the losses due to leakage increase with a lower supply voltage. These two effects counter each other and therefore an optimum supply voltage level can be found. Several publications discuss this minimum energy point for optimized digital circuits design [63, 71, 73]. Dependent on the process technology, it is in general close to the threshold voltage. In some applications, such as thermoelectric energy harvesting, the power source provides even lower voltages in the order of 100 mV. Therefore voltage conversion has to be preceded when using conventional logic gates. At least for start-up, some components of the DC/DC converter still need to be functional in the deep sub-threshold region for wake-up and generation of a clock signal (Figure 2.1).

When compared to strong-inversion operation the electrical properties of transistor devices significantly change below the threshold voltage, resulting in a couple of challenges that have to be considered [16].

- **Speed:** The propagation delay of logic cells is determined by the slope of the switching edge which is a function of the output current divided by the load capacitance. The latter includes the input capacitance of the following stage and parasitic capacitances of connection wires. The former shrinks exponentially with the supply voltage, used to control the gate. This leads to an extended delay which limits the maximum operation frequency to the kHz region in deep sub-threshold operation.

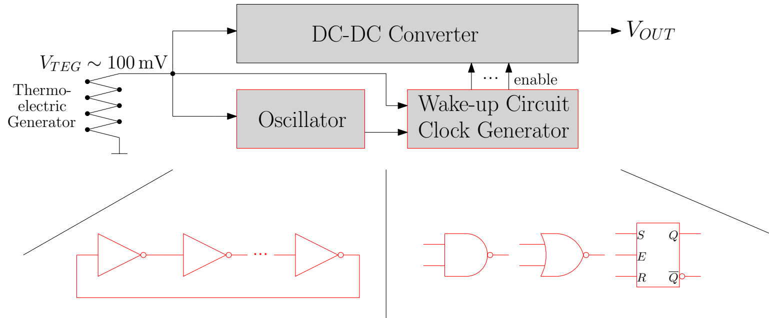



Figure 2.1: Use case for sub-threshold logic reducing the start-up voltage of a DC-DC converter. The minimum supply of the clock generator defines the start-up voltage of the circuit [30].

- **Gain:** Lowering the supply voltage to below $3-4$ times the thermal voltage ($V_t = kT/q$) causes degradation of the on/off current ratio due to $V_{DS}$ roll-off. As a result the gain and the voltage swing is greatly reduced.

- **Temperature:** The behavior of a MOS transistor on a rising temperature is affected by two counteracting properties, a decreasing threshold voltage and mobility degradation. While the former causes a higher current, the latter reduces it. The overall behavior is therefore determined by the dominating effect which depends on the operation region. In strong-inversion the mobility degradation predominates and reduces the speed of a circuit. In weak-inversion the exponential dependency on the threshold voltage overtakes and allows higher operation frequencies.

- **Process:** The exponentially decreasing on/off current ratio of transistors in push-pull gates, affected by process variations, leads to a serious reliability issue with sub-threshold circuits [9]. Considering an inverter in a worst case scenario of a strong PMOS and a weak NMOS (or vice versa), the leakage current of the strong device may remain higher than the current capability of the weak one. As a result the weak device is not able to change the state of the output node which causes a logic failure. Additionally, layout techniques for good matching have to be applied to ultra-low voltage logic gates, as the threshold voltage is influenced by well proximity effects and Shallow Trench Isolation (STI) stress [13].

Several techniques have been introduced to lower the minimum voltage level of digital cells. By proper transistor sizing and circuit topology optimization a 180 mV FFT-processor was realized in [72], using standard CMOS transistors. Another approach is to shift the sub-threshold region to lower values by applying forward body biasing to the devices. Different topologies of dynamic or static body biasing were introduced in [65] and [52]. Those techniques typically require triple-well technologies and suffer from additional circuitry effort, due to biasing generation or limitation circuits to prevent the forward-biased PN junction diode from conducting. Nevertheless a successful demonstration of an 8 bit microprocessor operating at

160 mV was shown in [20]. Post-fabrication process steps, such as charge injection into the gate oxide, significantly reduce the threshold voltage of transistors. Therefore a minimum $V_{DD}$ of 95 mV was achieved accepting an exponentially growing leakage current and higher fabrication costs [8]. A different digital circuit family, based on logic operations in the current domain, is source-coupled logic and was introduced for sub-threshold operation in [68]. In comparison to CMOS logic this approach uses source-coupled differential pairs connected to a highly resistive load. The switching network consists only of NMOS transistors which decreases the process variation sensitivity. Nevertheless as a differential input stage consists of a series connection of three transistors, the supply voltage reduction is limited.

### 2.1.1 Sub-threshold Conduction of MOS Transistors

The threshold voltage ($V_{TH}$) is defined by the gate-source voltage ($V_{GS}$) required to build up an inverted channel from the source to the drain of a MOS transistor. Below $V_{TH}$ this conducting channel does not exist. Charge carrier movement is therefore caused by diffusion instead of a drift current. As a result the characteristics change significantly. While in super-threshold operation the drain-source current ($I_{DS}$) increases quadratically with $V_{GS}$, it shows an exponential dependency in the sub-threshold region. According to [73], the expression of $I_{DS}$ is given by (2.1.1). $W/L$ represents the geometry, $m$ the sub-threshold slope factor and $V_t$ the thermal voltage $kT/q$. The factor $\eta$ models the Drain-Induced Barrier Lowering (DIBL), which is the major second-order effect occurring in that region. $I_0$ defines the saturation current of a transistor and considers process dependent parameters such as mobility ($\mu_0$) and oxide capacitance ($C_{ox}$) (2.1.2). In the following equations the process dependent parameters are printed in bold letters.

$$I_{DS} = \boldsymbol{I_0} \frac{W}{L} \mathrm{e}^{\left(\frac{V_{GS} - \boldsymbol{V_{TH}} - \eta V_{DS}}{m V_t}\right)} \left(1 - \mathrm{e}^{-\frac{V_{DS}}{V_t}}\right) \tag{2.1.1}$$

$$I_0 = \boldsymbol{\mu_0} \, \boldsymbol{C_{ox}} \, (m-1) \, V_t^2 \tag{2.1.2}$$

The sub-threshold current of a MOS device is much more sensitive to process variation compared to super-threshold operation. By investigation of equation (2.1.1), two process dependent parameters are identified. $I_0$ and $V_{TH}$, where in particular the latter is critical due to its exponential impact on $I_{DS}$. Strictly speaking, the sub-threshold slope factor also shows a weak process dependency, which is neglected here for simplicity.

### 2.1.2 MOS Transistor as Leakage Current Source

The leakage current ($I_{leak}$) of a MOS transistor is defined by the drain-source current at $V_{GS} = 0\,\mathrm{V}$. Therefore interconnecting gate and source results in a leakage current source. As

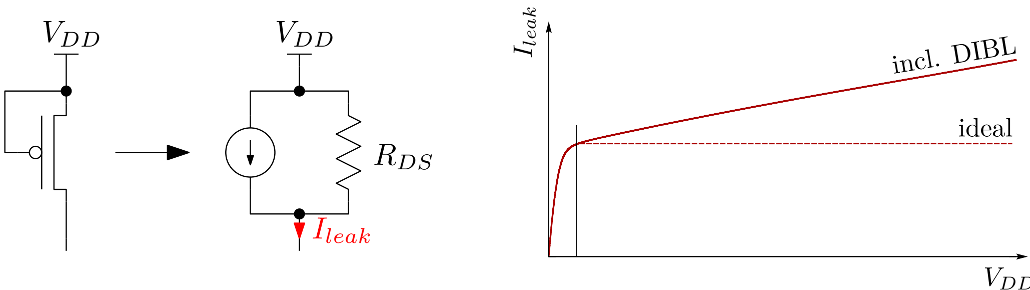



Figure 2.2: Schematic diagram of the output characteristic of a leakage current source.

shown in Figure 2.2, such a device nearly provides a constant output current with a weak dependence on $V_{DD}$ due to Drain-Induced Barrier Lowering. In a first order approximation it is therefore modeled by a current source with a resistor in parallel. In order to get the output current of a leakage current source, (2.1.1) can be rewritten as shown in (2.1.3).

$$I_{leak} = \boldsymbol{I_0} \frac{W}{L} \mathrm{e}^{\left(\frac{-\boldsymbol{V_{TH}} - \eta V_{DS}}{m V_t}\right)} \left(1 - \mathrm{e}^{-\frac{V_{DS}}{V_t}}\right) \tag{2.1.3}$$

The leakage current itself strongly depends on process and temperature variations, but due to correlation effects it can be used as a high-resistive load for a digital logic gate. This issue is discussed in more detail in Chapter 2.2.

### 2.1.3 Short-Channel Effect

Another parameter affecting $V_{TH}$ is the gate length of a device due to short-channel effects. As is known from the literature, short transistors suffer from a reduced threshold voltage caused by charge sharing (CS) at the overlapping space-charge region of drain and source junctions [60]. Therefore in current process technologies, the effective doping level is increased by applying halo implants. As a result the threshold voltage rises again which is commonly known as reverse short-channel effect (RSCE) [60]. In Figure 2.3, the dependency of the threshold voltage on the gate length was simulated for an N- and P-MOS device, assuming a constant width. As can be seen, for the Infineon 130 nm process technology, RSCE causes the highest $V_{TH}$ for minimum gate length. Therefore the sub-threshold design methodology of digital logic cells is different to super-threshold operation. Instead of increasing the current capability by changing the width, it is more effective to increase the gate length of a device. This is true for short-channel devices where RSCE has an effect on $V_{TH}$.

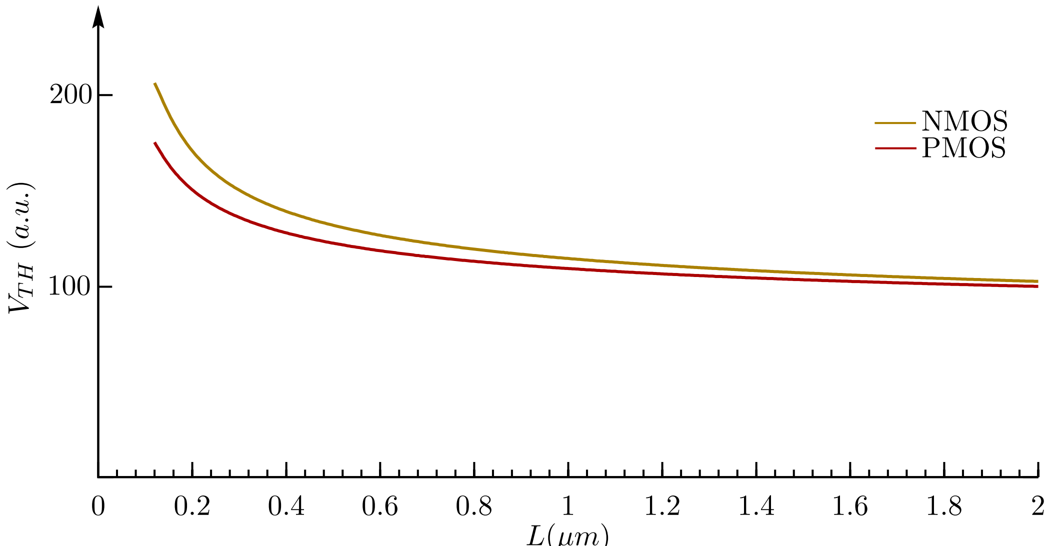



Figure 2.3: Dependency of the threshold voltage on the gate length of a transistor.

### 2.1.4 Transistor Sizing for Maximum Operation Frequency

To change the state of the output node of an inverter, a driving transistor has to charge or discharge the input capacitance of the following logic gate which consists at least of one NMOS and PMOS pair. As a result the circuit's maximum operation frequency is determined by the slew rate, which is given by current divided by capacitance. Enlargement of the transistor width for higher frequencies increases current capability and gate capacitance and therefore affects nominator and denominator of the slew rate in the same direction. Conventional digital logic cells use minimum channel length and set the current capability by the width in order to keep the gate capacitance low. As discussed in the previous chapter, in the deep sub-threshold region the length is an additional (nonlinear) parameter used to increase $I_{DS}$ in the process technology used. Finding the optimum gate length for a minimum propagation delay is therefore the next step in the optimization process.

To verify the impact of the gate length on the slew rate a parametric sweep simulation was performed by applying a gate voltage of 100 mV to an NMOS and a PMOS transistor of similar width for different device lengths. The drain-source current as well as the gate capacitance of the two transistors were monitored and set in relation to plot the slew rate for different values of $L$. The resulting curves in Figure 2.4 show some interesting properties in comparison to strong inversion operation. Starting at minimum length the PMOS transistor shows a higher current capability compared to its counterpart up to a length of 600 nm. The reason can be found in the lower rise of the threshold voltage due to RSCE of the PMOS transistor (review Figure 2.3). Above, the lower mobility dominates and the PMOS becomes the weaker device. At the intersection point, which is close to the maximum slew rate, both transistors have similar strength. Therefore a gate length of 600 nm was chosen for the gates of the ultra-low voltage digital cell library.

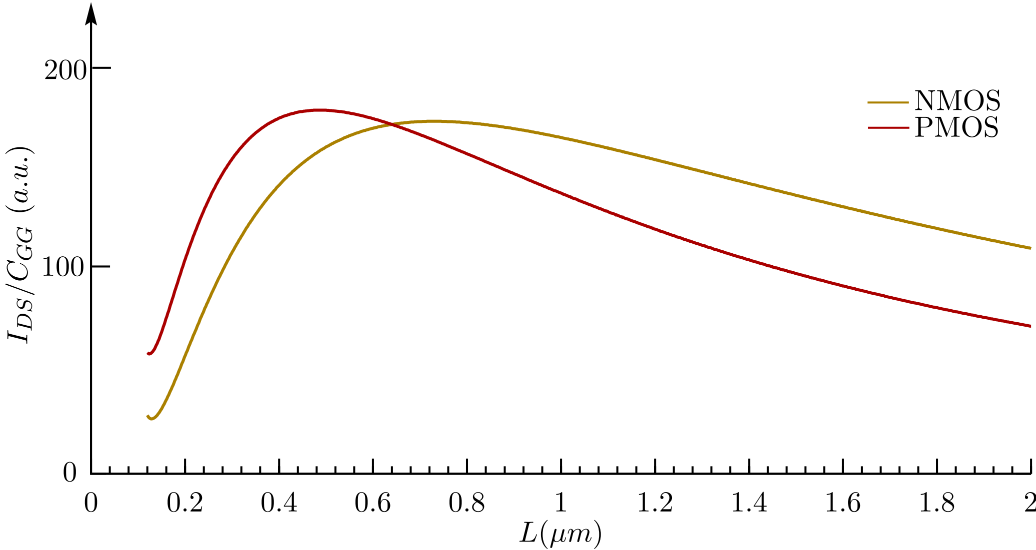



Figure 2.4: Dependency of the slew rate of the gate length of a transistor.

## 2.2 Reducing Process-dependent Variations in the Deep Sub-threshold Region

The aim of this chapter is to discuss the issue, which is related to process variation, of reducing the supply voltage of a CMOS inverter to the deep sub-threshold region of less than 100 mV. Therefore, the equivalent circuit diagram of the gate is analyzed at the transition point of $V_{IN} = V_{DD}/2$, which is the switching threshold of the idealized digital circuitry. Then, in the following chapters, the topology is adapted by introducing N- and P-type inverters. This results in the creation of a CMOS inverter with reduced sensitivity to process variations for ultra-low voltage operation.

### 2.2.1 Standard CMOS Inverter

A standard CMOS inverter is shown in Figure 2.5 and consists of an interconnected NMOS and PMOS pair, implementing logical negation. It can be modeled by two complementary current sources operating in a push-pull configuration. The output voltage is determined by the current capability of the stronger transistor which is controlled by the gate-source voltage.

$$I_{MN} = \mathrm{e}^{\left(\frac{V_{IN}}{mV_t}\right)} \cdot \boldsymbol{I_{leak_N}} \tag{2.2.1}$$

$$I_{MP} = \mathrm{e}^{\left(\frac{V_{DD}-V_{IN}}{mV_t}\right)} \cdot \boldsymbol{I_{leak_P}} \tag{2.2.2}$$

$$\boldsymbol{V_{SW}} = \frac{1}{2}\left(V_{DD} + mV_t \ln \frac{\boldsymbol{I_{leak_N}}}{\boldsymbol{I_{leak_P}}}\right) \tag{2.2.3}$$

For the purpose of this discussion the behavior a logical low at the input node is assumed. While the PMOS is fully turned on, the NMOS transistor is just leaking. Its drain-source current is therefore given by (2.1.3). As a result the output node is pulled up to a logical high. Raising the input voltage increases the current capability of the NMOS by amplification of $I_{leak}$ with an exponential factor (2.2.1). The opposite behavior is observed for the PMOS which becomes weaker due to $V_{GS}$ reduction (2.2.2). As soon as the input voltage exceeds the switching threshold ($V_{IN} = V_{DD}/2$), the NMOS transistor sinks more current than the PMOS can deliver, therefore the drain-source voltage drops to a low level. At the transition point, both current sources are of similar strength resulting in an output voltage of $V_{OUT} = V_{DD}/2$, due to the finite drain-source resistances.

Process related variations influence the leakage currents and therefore the switching threshold ($V_{SW}$) of the inverter. In order to discuss this issue the transition point is investigated by setting up the current balance equation ($I_{MP} = I_{MN}$) at the output node. Solving $V_{IN}$ results in the ideal switching threshold of $V_{DD}/2$ which is shifted by an error term, depending on the leakage currents ratio given by (2.2.3). This expression shows that the switching level $V_{SW}$ has a logarithmic dependency on the saturation currents $I_{0_N}$ and $I_{0_P}$ and changes linearly with the transistors threshold voltage ($V_{TH_N}$, $V_{TH_P}$). As the parameters of both devices vary in an uncorrelated way, a large deviation in the switching threshold can be expected. To verify the impact of process related variations on the switching threshold of the standard CMOS inverter in Figure 2.5, the voltage transfer curve was simulated by performing a Monte Carlo simulation at a supply voltage of 80 mV. The corresponding output characteristic is illustrated in Figure 2.6 and shows a six-sigma deviation of ±55.6 mV. This confirms the assumption that conventional CMOS logic cells are unusable in the deep sub-threshold region.

### 2.2.2 N-type Inverter

As shown in the previous chapter the deviation of the switching threshold causes serious issues in conventional CMOS logic cells in ultra-low voltage domains, due to uncorrelated process parameter dependencies of NMOS and PMOS transistors. A solution to this problem is to replace the active PMOS by a leakage current source of its opposite type as illustrated in Figure 2.7. The leakage current source consists of a certain amount of NMOS devices, as used for the active part. This is because in order to provide a logical high, the load needs to be

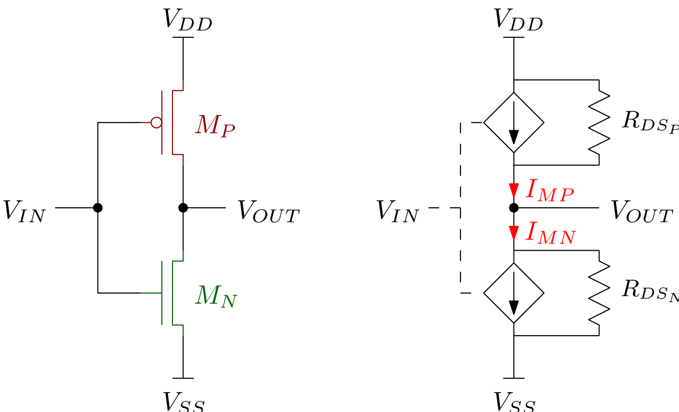



Figure 2.5: Standard CMOS inverter and its simplified equivalent circuit diagram [30].

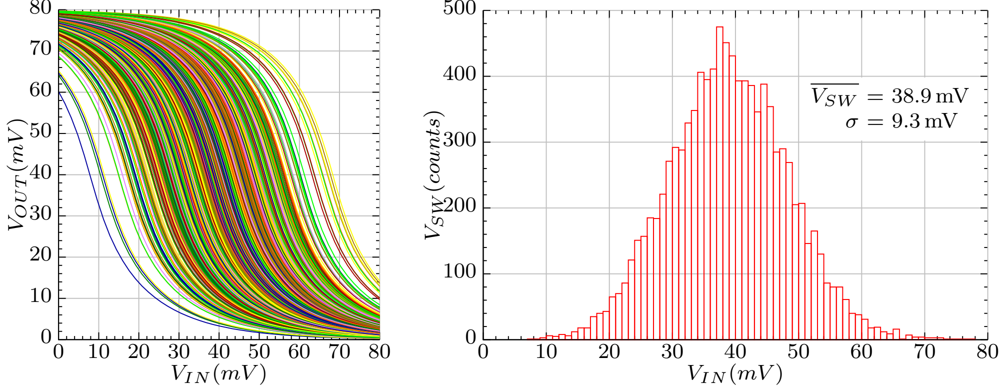



Figure 2.6: Simulated voltage transfer curve of a standard CMOS inverter at a supply voltage of 80 mV applying 10000 Monte Carlo runs.

able to pull-up the output node. The advantages of such a configuration are correlated process parameters of the active device and the load.

$$I_{MN1} = \mathrm{e}^{\left(\frac{V_{IN}}{mV_t}\right)} \cdot \boldsymbol{I_{leak_N}} \tag{2.2.4}$$

$$I_{MN2} = n \cdot \boldsymbol{I_{leak_N}} \tag{2.2.5}$$

$$V_{SW} = mV_t \cdot \ln(n) \tag{2.2.6}$$

In order to discuss the behavior of the n-type inverter of Figure 2.7, the switching threshold is again calculated by setting up the current balance equation at the output node. The current capability of $M_{N1}$ is known from the previous chapter and given by (2.2.4), while the load ($M_{N2}$) provides $n$ times the leakage current of the active device. Unlike the standard CMOS inverter, $I_{leak}$ drops out of the current balance equation resulting in a process- and supply

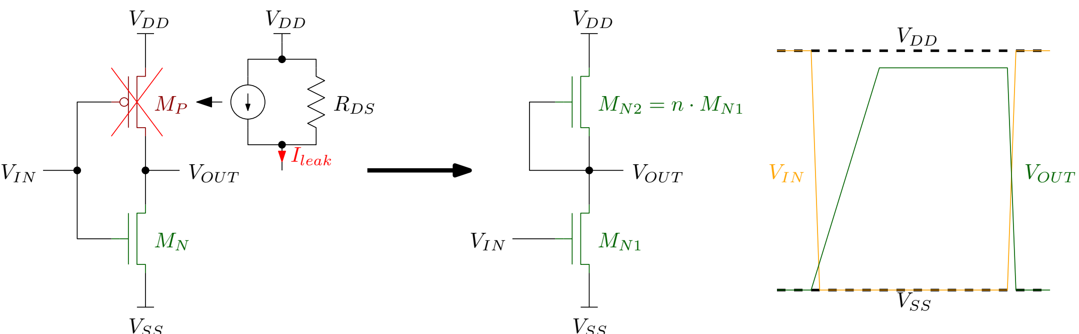



Figure 2.7: N-type inverter. Using a single transistor type reduces the influence of process dependencies due to correlation effects.

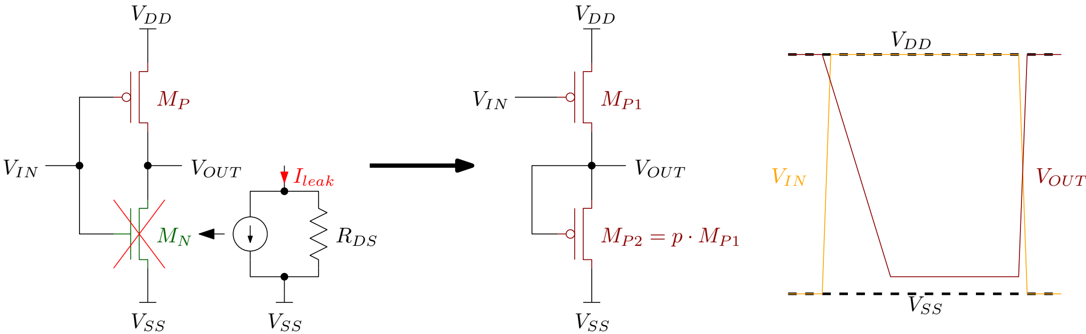



Figure 2.8: P-Type Inverter. Using a single transistor type reduces the influence of process dependencies due to correlation effects.

independent switching threshold. $V_{SW}$ is adjustable to the number of devices used for the leakage source (2.2.6). The cost of the process independence is a slow rising edge as it is just the leakage current charging the load capacitance. Additionally the voltage swing is reduced due to a lower logical high state.

### 2.2.3 P-type Inverter

The same approach can be applied by replacing the NMOS by a certain amount ($p$) of PMOS leakage current sources to get a P-type inverter (Figure 2.8). The corresponding current equations are given in (2.2.7) and (2.2.8) again resulting in a process independent switching threshold when setting up the current balance equation at the output node (2.2.9). In contrast to the N-type inverter, the switching threshold $V_{SW}$ is referred to $V_{DD}$. When studying the shape of the output voltage in Figure 2.8, it shows a weak falling edge due to the leakage current discharging the load capacitance. Additionally the voltage swing is reduced due to a higher logical low state.

$$I_{MP1} = \mathrm{e}^{\left(\frac{V_{DD}-V_{IN}}{mV_t}\right)} \cdot \boldsymbol{I_{leak_P}} \tag{2.2.7}$$

$$I_{MP2} = p \cdot \boldsymbol{I_{leak_P}} \tag{2.2.8}$$

$$V_{SW} = V_{DD} - mV_t \cdot \ln(p) \tag{2.2.9}$$

In summary both inverter topologies that were introduced enable a reduction of the supply voltage. This is due to their process variation immunity produced by using just a single transistor type. As their switching threshold refers to different reference points, mixing up both topologies is not feasible without level shifting. In addition $V_{SW}$ of N- and P-type are complementary affected by the thermal voltage. A significant drawback, compared to CMOS inverters, is the asymmetric slew rate of the switching edge caused by the weak load device. Solving this issue while maintaining process variation immunity is discussed in the following section.

### 2.2.4 Proposed CMOS Inverter

To overcome the drawbacks of N- and P-type inverters, both devices are connected in parallel as shown in Figure 2.9. The idea is to benefit from an active push-pull configuration similar to CMOS technology while removing the influence of process variations on the switching threshold. To analyze the behavior of the proposed gate, the current balance equation is again set up at the transition point using the current expressions from (2.2.4), (2.2.5), (2.2.7) and (2.2.8). At the switching threshold, current equilibrium occurs, which can be expressed as shown in equation (2.2.10). It includes the process dependent leakage currents of NMOS and PMOS transistors. Although those parameters are multiplied by a process independent factor in brackets defining the strength of the influence.

$$\boldsymbol{I_{leak_N}} \cdot \left(n - \mathrm{e}^{\left(\frac{V_{IN}}{mV_t}\right)}\right) = \boldsymbol{I_{leak_P}} \cdot \left(p - \mathrm{e}^{\left(\frac{V_{DD}-V_{IN}}{mV_t}\right)}\right) \tag{2.2.10}$$

$$n_{opt} = p_{opt} = \mathrm{e}^{\frac{V_{DD}}{2mV_t}} \tag{2.2.11}$$

For a given supply voltage $n$, $p$ can be chosen in a way such that this factor becomes zero. In that case the variation of $V_{TH_N}$, $V_{TH_P}$, $I_{0_N}$ and $I_{0_P}$ no longer affects the switching threshold. The corresponding equation is given in (2.2.11). When assuming a supply voltage of 80 mV, room temperature and a sub-threshold slope factor of 1.2 , the calculated optimum number of devices for leakage compensation is $n = p \approx 4$. The influence of the leakage compensation on $V_{SW}$ was verified by performing a Monte Carlo simulation of the proposed CMOS inverter using the calculated optimum compensation factor of 4. The geometry and simulation conditions

that were chosen similar to the standard inverter in Chapter 2.2.1. Figure 2.9 illustrates the corresponding schematic.

The resulting voltage transfer curve, shown in Figure 2.10, demonstrates the beneficial effect of leakage compensation on process variation immunity to the gate by reducing the six-sigma deviation from original value of ±55.6 mV to ±8.4 mV. This corresponds to an enhancement of 85 % due to the proposed compensation technique. Operation in the deep sub-threshold is therefore feasible. It has to be noted that this compensation network not only suppresses the influence of process variations at a certain supply voltage but also reduces them for higher voltages. Additionally, operation of the logic gate is not just limited to the sub-threshold region as the network loses its influence in strong inversion. The trade-off is a layout area overhead resulting in a larger input capacitance, a lower gain due to the reduced output resistance and a reduction of the voltage swing. These issues will be discussed in more detail in the following chapter.

At this point a general rule to apply the technique to other logic cells is defined. Firstly introduced in [31], the instruction of compensation specifies how to modify standard logic cells in order to become ultra-low voltage-ready:

> **For each active path from $V_{DD}$ to $V_{OUT}$/$V_{OUT}$ to $V_{SS}$ add a certain number of leakage-transistors ($V_{GS}$=0 V) of the same kind and geometry from $V_{OUT}$ to $V_{SS}$/$V_{DD}$.**

For example the inverter consists of one active PMOS device connected between $V_{DD}$ and $V_{OUT}$. Therefore a certain number of similar PMOS devices are added from $V_{OUT}$ to $V_{SS}$. By applying the same procedure to the active NMOS (connected between $V_{OUT}$ and $V_{SS}$), a certain amount of similar NMOS transistors are added from $V_{DD}$ to $V_{OUT}$.

### 2.2.5 Area, Speed and Power Analysis of the Proposed CMOS Inverter

Process variation immunity gained applying a compensation network is achieved at the cost of area overhead and increased power dissipation. Each of the compensation devices adds the gate capacitance and the leakage current of one transistor unit. Compared to the layout of a standard inverter ($A_0$), the area demand of the proposed inverter ($A_n$) grows linearly with the number of compensation devices ($n, p$) (2.2.12). As a result, the load capacitance of the gate increases by the same amount and so does the power dissipation. In equation (2.2.13), $P_0$ corresponds to the standard CMOS inverter and $P_n$ considers the compensation network. Additionally the slew rate is affected by the larger capacitance to be charged and discharged which reduces the maximum operation frequency.

$$A_n = A_0 \left(1 + n\right) \tag{2.2.12}$$

$$P_n = P_0 \left(1 + n\right) \tag{2.2.13}$$

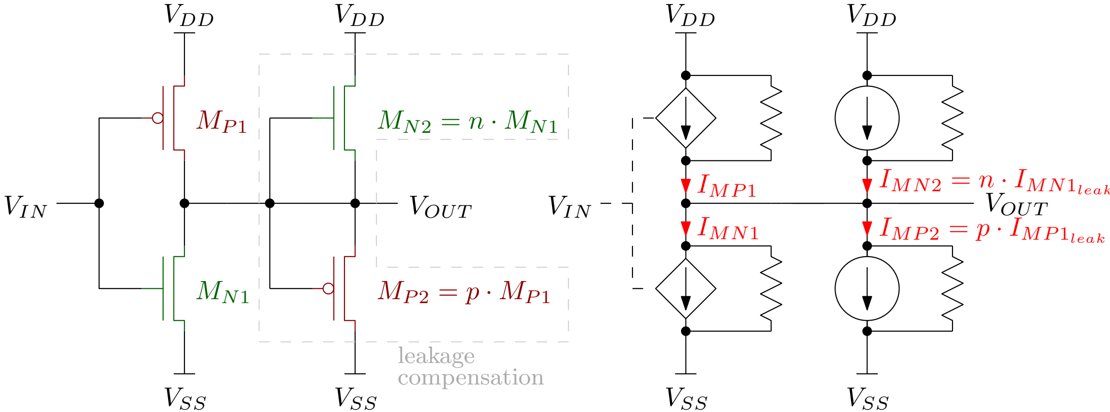



Figure 2.9: Proposed CMOS inverter and its simplified equivalent circuit diagram [30].

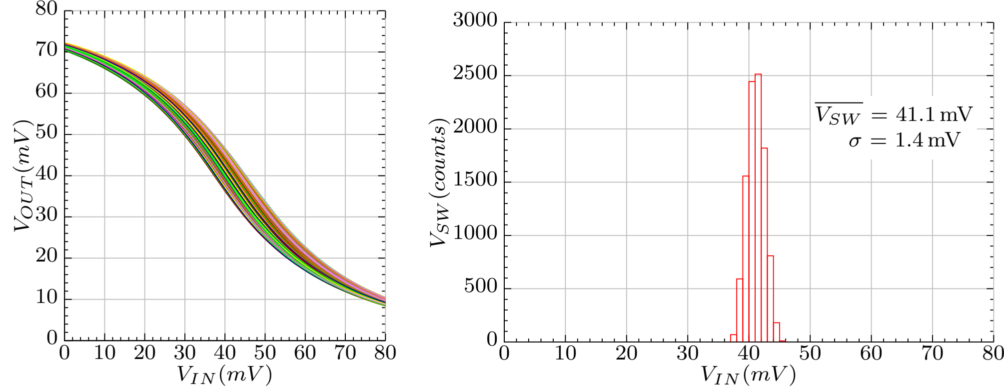



Figure 2.10: Monte-Carlo simulation of the output characteristic of the proposed CMOS inverter using 10000 runs.

It can be seen from the previous analysis that the number of transistors in the compensation network significantly influences the performance of the logic gate. Selection of $n$,$p$ is therefore a trade-off between process related variation and layout area, affecting power dissipation and maximum operation frequency. At a supply voltage of 80 mV the switching threshold is shown in Figure 2.10 to shift by ±10 %. For proper functionality of digital logic cells a larger variation of $V_{SW}$ is still acceptable. From simulations a compensation factor of $n = p = 2$ has shown to be a good compromise and is therefore used for the development of the sub-threshold digital cell library. Finally it has to be noted that the number of leakage devices affects the output resistance and therefore the gain of a stage at a certain supply voltage level. Therefore more complex logic cells (NAND and NOR) require a minimum operation voltage of 90 mV to be functional.

## 2.3 Cell Library

This section deals with the design, layout and evaluation of an ultra-low voltage digital cell library with a supply voltage range starting from 90 mV to 1.2 V. It is achieved without any special process options, such as Low-$V_T$ devices, or post-fabrication process steps and exclusively uses regular transistors provided by the Infineon 130 nm design kit. Starting with the simple inverter the previously developed compensation technique is applied to NAND and NOR gates to realize more complex logical operations. Subsequently these basic logic cells are combined into flip-flops which are the fundamental building blocks of digital cores.

For verification, the Static Noise Margin (SNM) analysis is applied in the design phase. Firstly introduced by C. F. Hill in [22], this approach is a conventional method of evaluating the stability of digital logic cells. Therefore an infinite chain of gates is assumed in a worst-case situation (e.g. minimum signal amplitude). In practice this chain is formed by two cross-coupled inverting gates where each output node is connected to the other's input. This architecture leads to a bistable latching circuitry storing an initialized value. Static Noise Margin is defined by the error voltage to be added to both inputs in order to change the state of this structure. It is found by plotting the voltage transfer curve (VTC) of the first element against the inverse VTC of the second, commonly know as butterfly plot. By finding the largest inscribed square between both curves, SNM can be estimated in a graphical way. A detailed explanation and mathematical analysis of Static Noise Margin can be found in [46]. In order to use SNM in a circuit simulator, a simulation method based on the graphical technique taken from [62] is applied in this thesis. Process and mismatch variations are considered by applying Monte Carlo analysis on the parasitic extracted model of the developed logic gates. The layout of each cell is made by hand with focus on reduction of systematic process errors by using common centroid layout and dummy cells. Additionally the distance to the well border is increased to weaken well proximity effects. As a result the current layout is not optimized for minimum area requirements. In order to enable a modular arrangement, the height of the logic cells is chosen to be similar for across all kinds of inverter-, NAND-, NOR- gates. Therefore, simplified cascading of logic gates is feasible.

A test chip was fabricated to evaluate the functionality of the presented logic gates. It contains the invented basic logic cells (inverter, NAND, NOR and D-FF) and digital circuits (ring-oscillator, full-adder, shift register and a counter). The current chapter focuses on the system architecture of single gates including basic measurements under ultra-low voltage conditions at room temperature. For detailed analysis of the maximum operation frequency and power dissipation with respect to supply voltage and temperature variation refer to Chapter 2.4.

### 2.3.1 Inverter

The simplest gate of a digital cell library is the inverter. It is therefore the first element to be discussed. Inverters are commonly used for signal negation and amplification in a buffer configuration. Typical standard libraries provide a set of inverters of several current capabilities to support a wide range of load conditions. This requirement is met by introducing four inverter

| | INV1 | INV2 | INV3 | INV4 |
|---|---|---|---|---|
| $W_{M_{P1}}$ | 0.9 µm | 1.5 µm | 3 µm | 6 µm |
| $L_{M_{P1}}$ | 0.6 µm | 0.6 µm | 0.6 µm | 0.6 µm |
| $W_{M_{N1}}$ | 0.68 µm | 1.42 µm | 2.84 µm | 5.68 µm |
| $L_{M_{N1}}$ | 0.6 µm | 0.6 µm | 0.6 µm | 0.6 µm |
| $n, p$ | 2 | 2 | 2 | 2 |
| Layout | 7.5 µm × 5.35 µm | 8.25 µm × 5.35 µm | 11.5 µm × 5.35 µm | 17.45 µm × 5.35 µm |
| $\overline{SNM}$ | 5.07 mV | 5.54 mV | 5.93 mV | 6.11 mV |
| $\sigma_{SNM}$ | 1.91 mV | 1.31 mV | 1.04 mV | 0.88 mV |

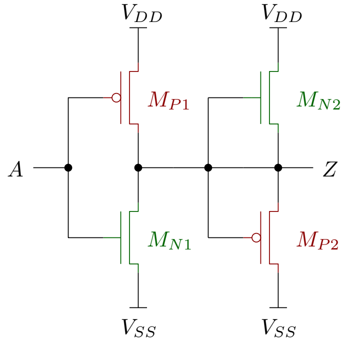
Table 2.1: Geometry of the inverters of the ultra-low voltage digital cell library.

gates. Their driving strength is indicated by numbers where incrementing is equivalent to approximately doubling the transistor width. The compensation network consists of two devices respectively. A summary of the transistor's geometry and other characteristics can be found in Table 2.1. As the principle architecture is similar in all cases, the weakest device is considered in more detail in the following section.

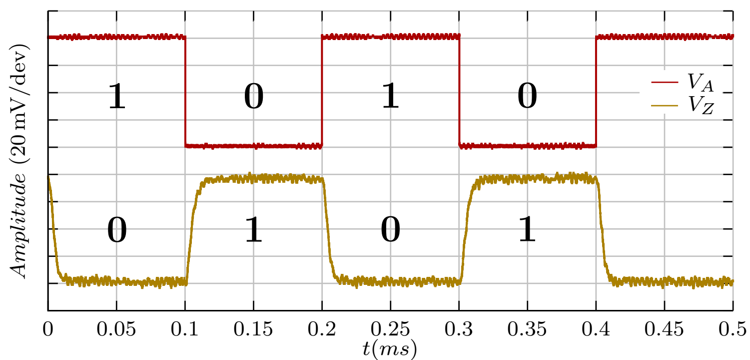
The system architecture and functionality of the proposed inverter with the corresponding schematic, shown in Figure 2.11a, have already been discussed in Chapter 2.2.4. Therefore the layout is considered next. As it can be seen in Figure 2.11c, common centroid layout is applied by arranging the compensation network around the active transistors. Encapsulation by dummy cells on the left and right side takes care of equivalent ambient conditions to compensate for systematic errors due to proximity effects. Contacts to substrate and n-well represent the top and bottom boundary. Due to the uniform height, the following gate can be attached directly to the contacts to build a digital circuit. The layout area of the weakest inverter ($INV1$) is given by 7.5 µm × 5.35 µm and scales linearly with the driving strength.

For evaluation, Static Noise Margin was simulated at a supply voltage of 80 mV, using the model including the extracted parasitics of the layout cell. Therefore process, mismatch and layout related second order effects are considered. Referring to the corresponding results in Table 2.1, the standard deviation ($\sigma_{SNM}$) decreases with growing transistor size due to reduced matching issues. While in simulation the weakest inverter provides a yield of 99.5 %, INV4 is even suitable in a six-sigma design. To prove the functionality, Figure 2.11b shows the measurement transient behavior of the proposed inverter in operation at a supply voltage of 80 mV. The input port is stimulated by a 5 kHz rectangular signal from a signal generator. As expected, the output signal represents the inverted input.

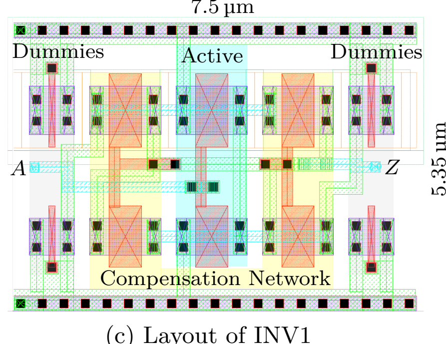
The set of inverters that were introduced allow processing of a single signal. Functionality of the current digital cell library is therefore limited to a few applications. For example an oscillator, which is typically required in all digital circuits. The next step is therefore to enable comparison of two or more signals by developing ultra-low voltage NAND- and NOR- gates.



(a) Schematic of INV1




(b) Measured input and output signals at $V_{DD}$=80 mV. The gate is stimulated with 5 kHz from a signal generator




(c) Layout of INV1

Figure 2.11: Schematic, measurement and layout of the proposed inverter $INV1$.

### 2.3.2 NAND-Gate

A NAND gate is a fundamental logic cell processing two input signals into a single output node. Its functionality is characterized by producing a logic high at the output unless both inputs are pulled-up to $V_{DD}$. Referring to Figure 2.12a, the conventional CMOS architecture consists of two NMOS devices ($M_{N1}$ and $M_{N2}$) in series and two PMOS transistors ($M_{P1}$ and $M_{P2}$) in parallel. Process variation immunity is achieved by extending the conventional design according to the instruction of compensation on Page 21 by a compensation network. Similar to the inverter, a compensation factor n=p=2 is used for the proposed NAND gate. Each of the active PMOS devices is compensated by two PMOS leakage current sources ($M_{P3}$ and $M_{P4}$), connected from $V_{OUT}$ to $V_{SS}$. On the other hand, one NMOS-path is available from the output to ground which is compensated by one NMOS leakage path ($M_{N3}$ and $M_{N4}$) from $V_{DD}$ to $V_{OUT}$*. Considering the output node, the proposed NAND gate suffers from a lower output resistance in comparison to the inverter, due to the larger number of transistors in parallel. As a result, the gain and therefore the voltage swing is reduced. To counteract this phenomenon a buffer is added to recover the signal amplitude. A detailed list of data describing the architecture is given in Table 2.2.

* In principle a single leakage current source would be sufficient but to achieve symmetry two devices are used.

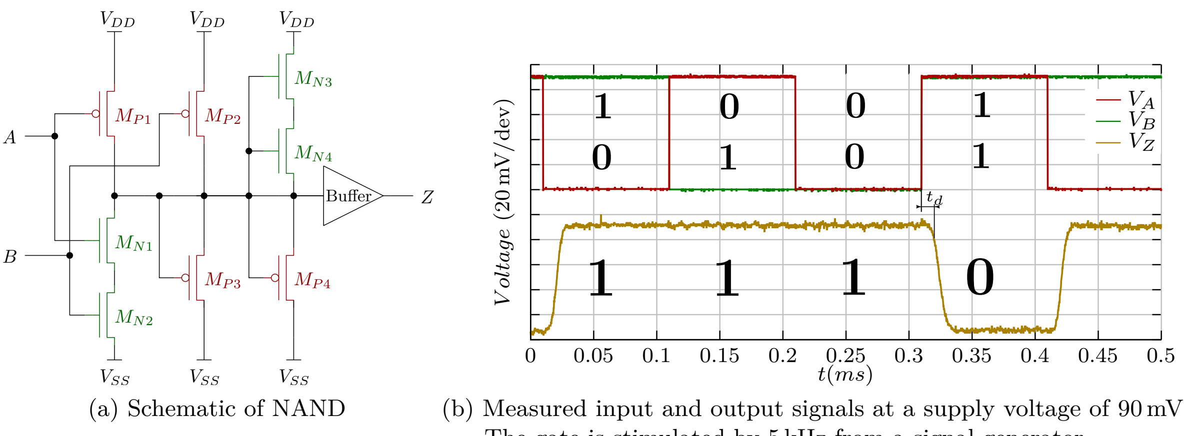
| | NAND1 | NOR1 |
|---|---|---|
| $W_{M_{P1,2}}$ | 0.6 µm | 1.6 µm |
| $L_{M_{P1,2}}$ | 0.6 µm | 0.6 µm |
| $W_{M_{N1,2}}$ | 1 µm | 0.68 µm |
| $L_{M_{N1,2}}$ | 0.6 µm | 0.6 µm |
| n,p | 2 | 2 |
| Layout | 21.9 µm × 5.35 µm | 21.9 µm × 5.35 µm |
| $\overline{SNM}$ | 18.1 mV | 18.4 mV |
| $\sigma_{SNM}$ | 3.4 mV | 3.3 mV |
| $\overline{SNM}$ *combined* | 17.9 mV | |
| $\sigma_{SNM}$ *combined* | 3.9 mV | |

Table 2.2: Geometry of the NAND and NOR cell data base.

The layout, depicted in Figure 2.12c, is again optimized for reduced systematic errors by encapsulating the active transistors with the compensation network in a common centroid arrangement. The buffer consists of two inverters and is included in the cell. Dummy structures at the left and right outer edge complete the structure. With a dimension of 21.9 µm × 5.35 µm the cell can easily be attached to other gates of the ultra-low voltage digital cell library.

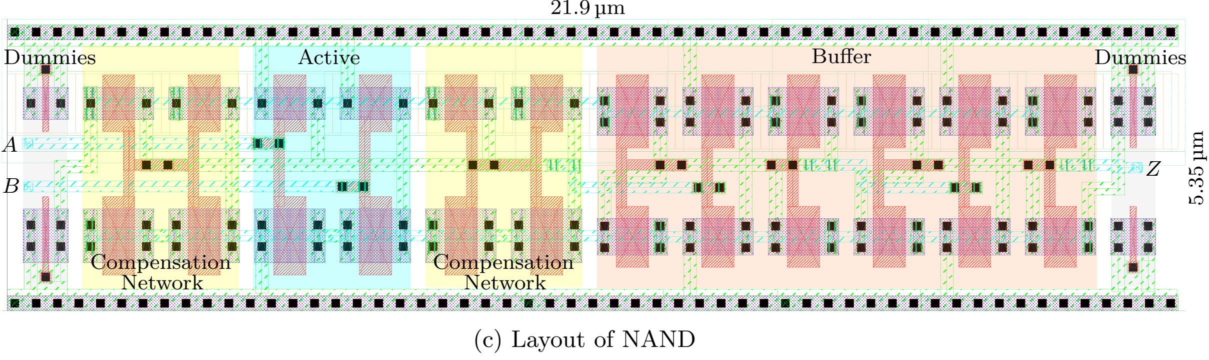
Verification during the design phase is achieved by performing a Monte Carlo simulation of Static Noise Margin. Due to the lower gain, the supply voltage is increased to 90 mV. Systematic and random errors due to process, layout and mismatch are considered by investigating the parasitic extracted model of the NAND gate. As already mentioned, SNM needs to be analyzed in a worst-case situation in terms of signal amplitude. Therefore the input state providing the lowest loop-gain of the cross-coupled structure needs to be investigated. Compared to the inverter, the NAND has two inputs, enabling four possible states, where three of them produce a logic high at the output. The weakest logic high amplitude occurs for the input state of lowest gain and is found by inspection of the conventional NAND schematic. In case of a low-signal on both inputs, two transistors in parallel ($2 \cdot gm$) pull-up the output node against the load of two series connected devices ($2 \cdot R_{DS_{OFF}}$). This is in contrast to complementary input signals, where one PMOS ($1 \cdot gm$) is working against the off-resistance of a single transistor ($R_{DS_{ON}} + R_{DS_{OFF}} \approx R_{DS_{OFF}}$). Therefore the latter provides less gain and is used for Static Noise Margin analysis. The corresponding SNM, listed in Table 2.2, is given by 18.1 mV with a standard deviation of 3.4 mV.

Finally the proposed logic cell was measured in operation at the given supply voltage with the corresponding oscilloscope snapshot in Figure 2.12b. As expected the output signal remains in high state until both inputs are pulled-up to $V_{DD}$. The output signal appears delayed by $t_d \approx 50$ µs in the plot which corresponds to an operation frequency in the kHz range.




(a) Schematic of NAND

(b) Measured input and output signals at a supply voltage of 90 mV. The gate is stimulated by 5 kHz from a signal generator.




(c) Layout of NAND

Figure 2.12: Schematic, layout and proof of operation of the proposed NAND gate.

### 2.3.3 NOR-Gate

A NOR gate is the second fundamental logic cell processing two input signals to a single output node. Together with the NAND, each logic operation can be performed by proper interconnection of the two. Its functionality is characterized by producing a logic low state at the output unless both inputs are pulled-down to $V_{SS}$. Referring to Figure 2.13a, the conventional CMOS architecture consists of two NMOS devices ($M_{N1}$ and $M_{N2}$) in parallel and two PMOS transistors ($M_{P1}$ and $M_{P2}$) in series. Process variation immunity is achieved by extending the conventional design according to the instruction of compensation on Page 21 by a compensation network, using n=p=2. Each of the active NMOS devices is compensated by two NMOS leakage current sources ($M_{N3}$ and $M_{N4}$) connected from $V_{DD}$ to $V_{OUT}$. The single PMOS-path from the output to ground is compensated by one PMOS leakage path ($M_{P3}$ and $M_{P4}$) from $V_{OUT}$ to $V_{SS}$. Similar to the NAND gate, the output resistance is reduced due to the larger number of transistors in parallel. A buffer is therefore added to recover the signal amplitude. A detailed list of data describing the architecture is given in Table 2.2.

The layout, depicted in Figure 2.13c, is again optimized for reduced systematic errors by encapsulating the active transistors with the compensation network in a common centroid arrangement.

A buffer consisting of two inverters is included in the cell. Dummy structures at the left and right outer edge complete the structure. With a dimension of 21.9 µm × 5.35 µm the cell can easily be attached to other gates of the ultra-low voltage digital cell library.

Verification during the design phase is achieved by performing a Monte Carlo simulation of Static Noise Margin at a supply voltage of 90 mV. Systematic and random errors due to process, layout and mismatch are considered by investigating the parasitic extracted model of the NOR gate. In order to investigate the worst-case scenario of lowest loop-gain, both inputs are fed by complementary signals ($V_A$=low, $V_B$=high) to get the weakest logic low state. The corresponding SNM, listed in Table 2.2, is given by 18.4 mV with a standard deviation of 3.3 mV.

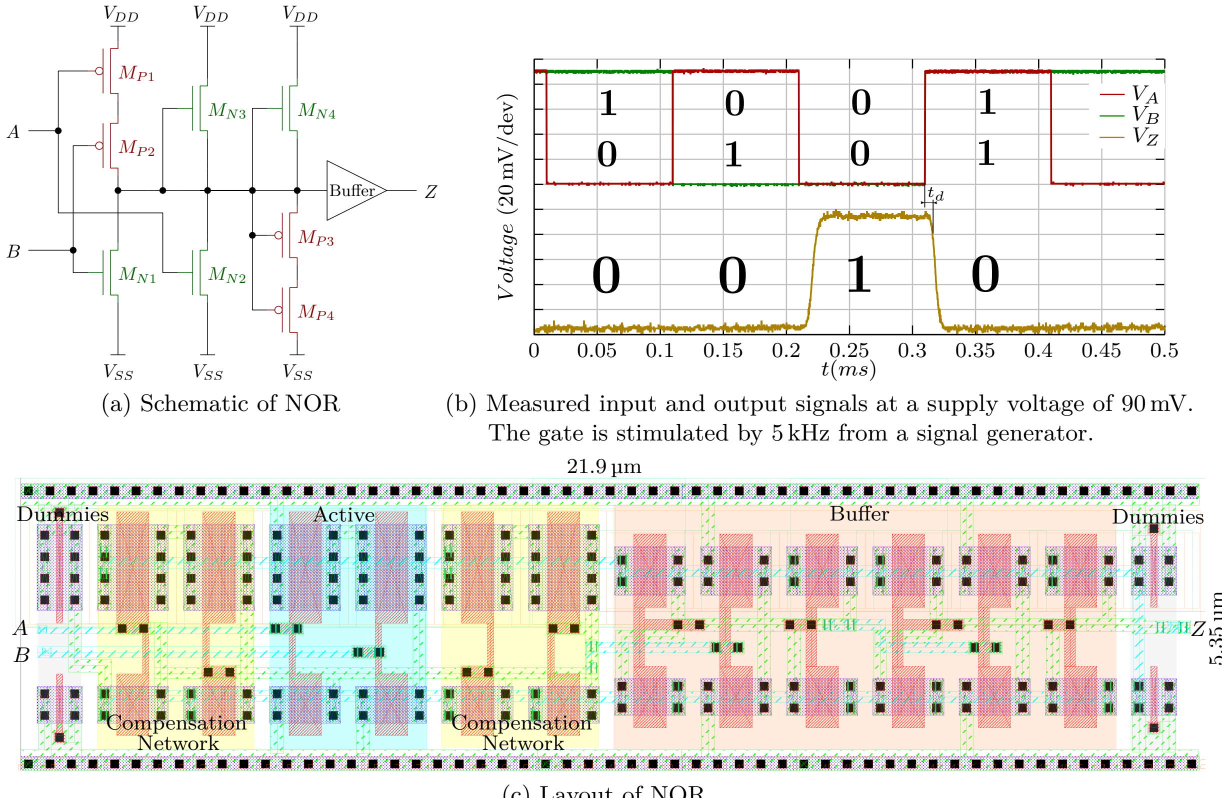
To prove the functionality the proposed logic cell was measured in operation at the given supply voltage with the corresponding oscilloscope snapshot in Figure 2.13b. As expected, the output signal remains in low state until both inputs are pulled-down to $V_{SS}$. Additionally a delay ($t_d$) in the order of 50 µs is shown in the plot.

The previous Static Noise Margin analysis doesn't consider an interconnection of NAND and NOR gates which typically occurs in digital circuits. Therefore a cross-coupled NAND and NOR structure with complementary input states is analyzed in order to obtain the combined SNM of the ultra-low voltage digital cell library at the minimum supply voltage for save operation. As shown in Table 2.2, the corresponding Static Noise Margin is given by 17.9 mV with a standard deviation of 3.9 mV. The fundamental logic cells are therefore expected to operate from 90 mV to 1.2 V.

### 2.3.4 Flip-Flop

In this section an edge-triggered ultra-low voltage D-flip-flop (DC_FF) is introduced which is operational at a supply voltage level of 90 mV. Flip-flops are basic elements of sequential logic circuits. In contrast to combinational logic circuits, their output state depends on the input state and, due to feedback loops, on the previous output conditions of the gate. The scope of digital circuits is therefore extended by a storage option which is of great importance in the realization of digital computation. Sequential logic cells are typically triggered by a clock signal to synchronize processing operations.

It is known from the literature that different CMOS logic families have pros and cons in terms of complexity, area overhead and power consumption [76]. Frequently used implementations are Clocked CMOS ($C^2$MOS) and Pass Transistor (PT) logic as they are area and power efficient. Their disadvantages are stacked transistor architectures which lead to decreased operational margin and complexity. In the deep sub-threshold region the prior objective is stability and functionality under ultra-low voltage conditions. For this reason, a cascaded structure is given preference over the previously mentioned cascoded ones, previously mentioned, even at the cost of area overhead. Therefore static CMOS logic cells by modular interconnection of NAND and NOR gates are used to design sequential logic gates of the ultra-low voltage digital cell library. System architecture and layout are discussed and a proof of operation is shown.




(a) Schematic of NOR

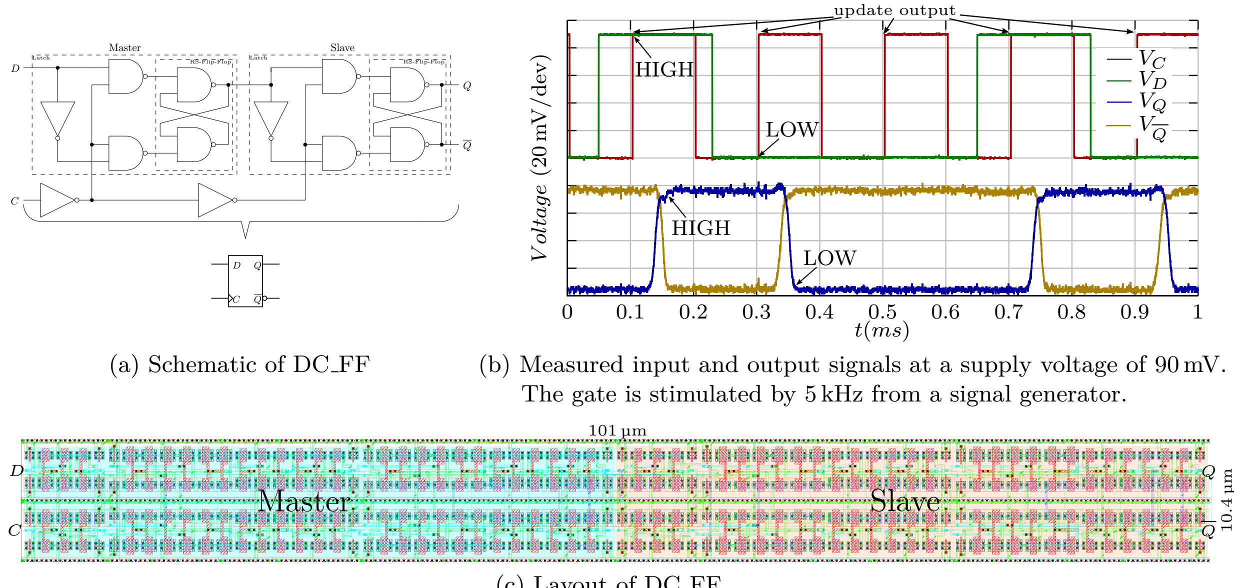
(b) Measured input and output signals at a supply voltage of 90 mV. The gate is stimulated by 5 kHz from a signal generator.

(c) Layout of NOR

Figure 2.13: Schematic, layout and proof of operation of the proposed NOR gate.

The principle architecture of the proposed D-flip-flop is shown in Figure 2.14a. It is realized by two gated latches in a master-slave arrangement. During the low state of the clock signal, the $D$ input is sensed by the master. At the rising edge of $C$ the current state is internally stored and handed over to the slave which releases the value on the output. This is shown in Figure 2.14b. The $D$ input is sampled at the rising edge of the 5 kHz clock signal and handed over to the output $Q$. Between two clock cycles the flip-flop keeps the value of $Q$ (and respectively its inverse $\overline{Q}$) independent of signal changes at the input $D$. The resulting output represents the input signal, synchronized to the clock. The corresponding layout can be reviewed in Figure 2.14b and shows a required layout area of 101 µm × 10.4 µm.

The development of fundamental logic cells was discussed in the previous chapters by providing several examples, representative for the ultra-low voltage digital cell library. The system architecture, layout considerations, as well as a functional proof of the process variation compensation scheme was presented by showing measurement results at a supply voltage of 90 mV. With this background, other logic operations (e.g. AND, OR, XOR, RS-FF, ...) can be realized by the reader in a similar way. Therefore the explanation of basic cells is concluded at this point in order to continue with detailed analysis of the behavior of basic digital circuits under temperature and supply voltage aspects in the following chapter.




(a) Schematic of DC_FF

(b) Measured input and output signals at a supply voltage of 90 mV. The gate is stimulated by 5 kHz from a signal generator.

(c) Layout of DC_FF

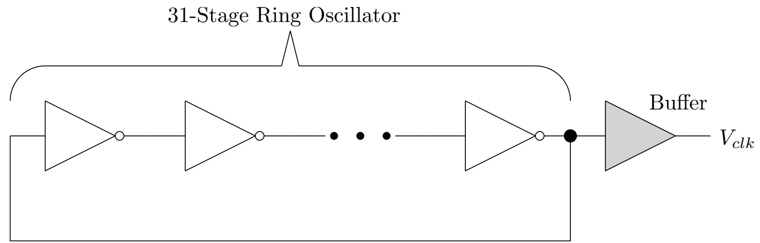
Figure 2.14: Schematic, layout and proof of operation of the proposed D-flip-flop.

## 2.4 Sub-threshold Digital Circuits

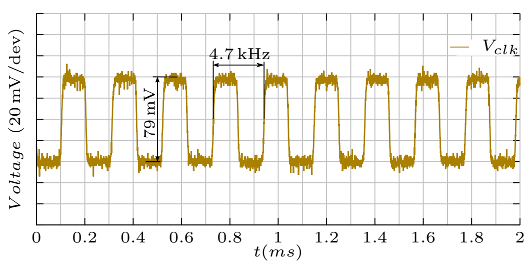
In this chapter, the gates of the ultra-low voltage digital cell library are combined to demonstrate the behavior of functional building blocks under ultra-low voltage conditions. Therefore a sub-threshold ring oscillator, a full-adder, a 4 bit shift-register and a 3 bit counter are presented. A set of $N = 10$ samples are evaluated to analyze the individual dependencies of propagation delay and power consumption on temperature and supply voltage variations. Additionally, the minimum $V_{DD}$ of each circuit is verified. A key figure is the operational temperature range of sub-threshold circuits which is typically limited. The available samples are tested across a temperature range from −20 °C to 120 °C. The investigated supply voltage ranges of 80 mV to 250 mV.

### 2.4.1 Ring Oscillator

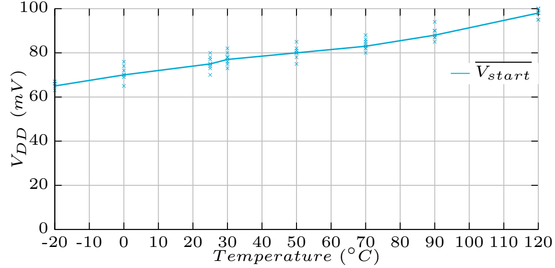
The first digital circuit based on multiple gates of the cell library to be discussed is the well-known ring oscillator. It consists of an odd number of inverters where the output of the last element is fed back into the first. This results in an unstable condition of a 180° phase shift and therefore an oscillation. The ring oscillator is self-starting and requires no reference voltage but provides a frequency that is not well defined, determined by the propagation delay ($t_D$) of the ring line. As $t_D$, besides the supply voltage, depends on process related parameters, ring oscillators are frequently used to benchmark process technologies. It is therefore the first circuitry to demonstrate the functionality in the deep sub-threshold region.



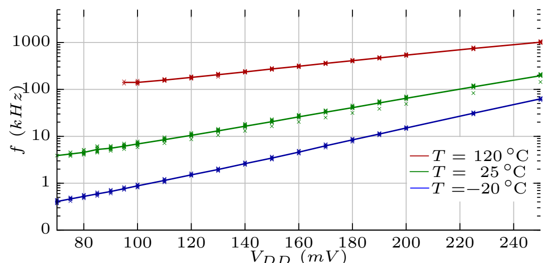

(a) Schematic of the 31-stage ring oscillator using ultra-low voltage inverters.



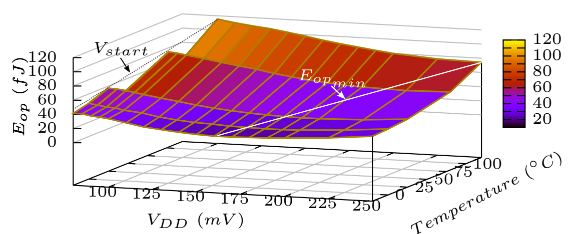

(b) Output signal of the 31-stage ring oscillator at a supply voltage of 90 mV ($T = 25\,°C$).




(c) Start-up voltage of the ring oscillator with respect to temperature.




(d) Oscillation frequency with respect to supply voltage at different temperatures.




(e) Energy per operation of the ultra-low voltage ring oscilltor.

Figure 2.15: Schematic and measurement data based on $N = 10$ samples of the 31-stage ring oscillator. A temperature range from $-20\,°C$ to $120\,°C$ is investigated at a supply voltage range from 80 mV to 250 mV. The average value and variation of individual test chips is plotted in the figures.

For evaluation, a 31-stage ring oscillator was manufactured on a test chip with the corresponding schematic in Figure 2.15a. In order to prevent distortion of the clock frequency through parasitic load capacitances of package and probe, a buffer is added between the circuit and the output pin. Figure 2.15b shows the transient output signal at a supply voltage of 90 mV at room temperature. The frequency ($f$) is given by 4.7 kHz which results in a propagation delay of 3.5 µs per stage using equation (2.4.1) with $m$ representing the number of stages. Additionally, the voltage swing is reduced by 12 % due to the lower gain by the compensation network.

$$t_D = \frac{1}{2mf} \tag{2.4.1}$$

In order to find the start-up voltage, $V_{DD}$ is successively increased while monitoring the output signal of each test chip across the full temperature range. As presented in Figure 2.15c, the mean start-up voltage is found to be 75 mV at $T$ = 25 °C and increases with temperature by a coefficient of 236 µV/°C. This rise is caused by the growing leakage current that reduces the output resistance and therefore the gain of each stage. In Figure 2.15c the variation of the start-up voltage of each individual test chip is shown in addition to the average value.

Theoretically, the sub-threshold drain-source current of a transistor increases exponentially with $V_{GS}$. As the propagation delay is inversely proportional to $I_{DS}$, the frequency is expected to grow in a similar way with the supply voltage. This behavior is observed in Figure 2.15d by monitoring $f$ with respect to $V_{DD}$. Starting from 4 kHz at 80 mV, the frequency increases exponentially to 200 kHz at 250 mV, assuming $T$ = 25 °C. The same applies for the temperature behavior. Considering $V_{DD}$ =100 mV, the frequency is given by 900 Hz at −20 °C, but increases to 140 kHz when heating the test chips to 120 °C. Figure 2.15d defines therefore the absolute maximum frequencies achievable with the ultra-low voltage digital cell library in the deep sub-threshold region for given temperature and supply voltage specifications.

Finally the power consumption is taken into account by investigating energy per operation ($E_{op}$) of the 31-stage ring oscillator over the full temperature and supply voltage range. $E_{op}$ is a commonly used efficiency indicator in digital circuits. It describes the energy demand of a single logical operation and considers dynamic (switching) and static (leakage) losses. Assuming invariant environmental conditions it is calculated by dividing the average power by the frequency (2.4.2).

$$E_{op} = \frac{V_{DD} \cdot I_{DD}}{f} \tag{2.4.2}$$

The corresponding measurement data is plotted in Figure 2.15e and is primarily discussed regarding a constant temperature. As mentioned in the introductory section of this chapter, dynamic losses are dominant at higher voltages while the leakage energy takes over at low voltages with an optimum operation point ($E_{op_{min}}$) in between. This assumption is in agreement with the measurement results. It can be explained by the following consideration. Lowering the supply voltages reduces the dynamic losses by decreasing the current capability of the gates. This leads to an extended propagation delay and therefore affects the frequency in the same direction. For the free running ring oscillator, the dynamic energy per clock cycle is therefore only slightly improved by a lower $V_{DD}$. The opposite behavior is observed for the static losses. The leakage current is, in general, independent of the supply voltage, when neglecting Drain-Induced Barrier Lowering. Therefore the same leakage current flows for the exponentially increased propagation time leading to a growing static energy demand per cycle. As a conclusion, decreasing $V_{DD}$ reduces the amount of dynamic losses at the cost of higher leakage energy per cycle. Assuming room temperature, the optimum $E_{op}$ is found to be 29 fJ/op at 190 mV and grows in both directions to 61 fJ/op at 75 mV and to 35 fJ/op at 250 mV, respectively.

Considering the temperature behavior, the static losses are strongly affected by the exponential impact on the leakage current which is shown by a stronger influence at low supply voltages. Across the 140 °C temperature range, the energy per operation increases by a factor of 4 at 80 mV and doubles at 250 mV. A temperature dependency is observed for the optimum $E_{op}$ which is shifted towards higher values. To conclude, higher temperatures lead to less performance at a certain $V_{DD}$ but increase the maximum operation frequency.

So far, only a single input cell type has been evaluated which illustrates the best-case in terms of Static Noise Margin. The measurement results obtained therefore represents the upper limit of operation frequency and the lowest start-up voltage. The next step is to design a full-adder by interconnecting NAND and NOR gates to demonstrate processing of multiple input signals in the deep sub-threshold region.

### 2.4.2 Full Adder

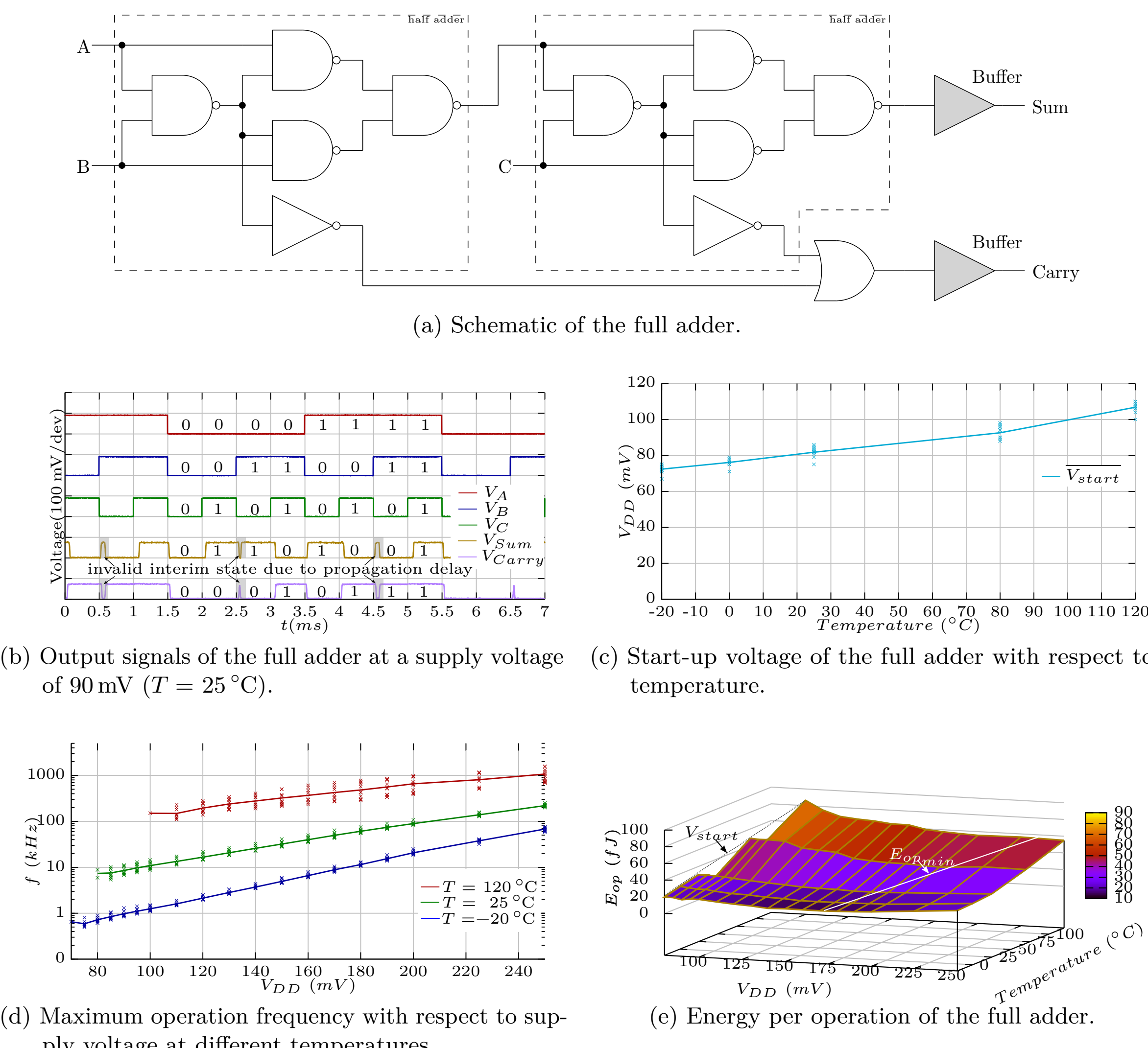
A full adder is a digital circuit used, for example, in arithmetic logic units to sum up 3 binary values and return a 2 bit result. The first output represents the calculation results while the second indicates an overflow of the current digits range, commonly known as a carry bit. Each digit of number to be added requires its own full adder in order to consider both terms and the carry bit of the less significant digit.

The system architecture is shown in Figure 2.16a and is based on static logic cells taken from the ultra-low voltage digital cell library. It consists of two cascaded half adders built of NAND gates. Additionally an OR gate is used to evaluate the carry bits. Unaffected monitoring of the output signal is achieved by adding unity gain buffers.

In Figure 2.16b the transient behavior of the implemented full adder at a supply voltage of 90 mV is shown. The circuit is stimulated by a 3 bit signal, counting from 0 to 7 to apply all possible input states. Verification is done by considering a few example codes. Adding up $0 + 0 + 1$ results in an 0 1 output code, where the former represents the carry and the latter the sum bit. The addends $1 + 0 + 1 = 1\ 0$ generate an overflow of the digits range, indicated by the carry bit, while the sum bit remains 0. The greatest result appears at $1 + 1 + 1$ with both outputs to be 1. Changing the $B$- and $C$- input state in a complementary way leads to invalid interim states due to the different propagation delay by cascaded arrangement. It is therefore recommended to cache the result using D flip-flops and pass it to the following stage with the next clock cycle. Nevertheless, proper operation under ultra-low voltage conditions is confirmed by measurements shown in Figure 2.16b.

As shown in Figure 2.16c, the mean minimum start-up voltage at room temperature is given by 80 mV and grows linearly by a coefficient of 250 µV/°C. Compared to the ring oscillator it is about 5 mV higher due to the use of NAND and NOR gates.

An exponential increase is observed for the dependencies of the maximum frequency on temperature and supply voltage. It therefore varies by order of magnitude within the range of interest. Assuming a supply voltage of 100 mV, the maximum frequency changes from 1 kHz




(a) Schematic of the full adder.

(b) Output signals of the full adder at a supply voltage of 90 mV ($T$ = 25 °C).

(c) Start-up voltage of the full adder with respect to temperature.

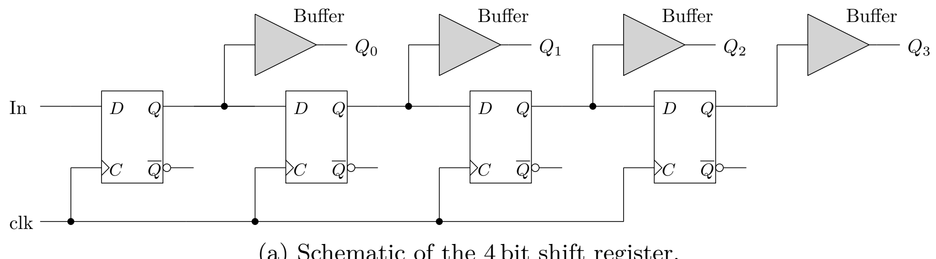
(d) Maximum operation frequency with respect to supply voltage at different temperatures.

(e) Energy per operation of the full adder.

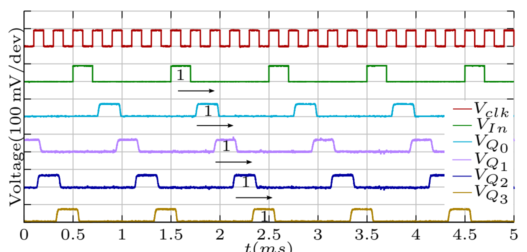
Figure 2.16: Schematic and measurement data based on $N = 10$ samples of the full adder. A temperature range of −20 °C to 120 °C is investigated at a supply voltage range of 80 mV to 250 mV. The average value and variation of individual test chips is plotted in the figures.

at −20 °C to 105 kHz at 120 °C. The entire measurement results can be reviewed in Figure 2.16d.

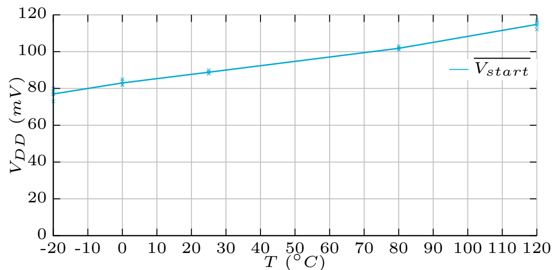
The performance parameter $E_{op}$ is plotted in Figure 2.16e. Similar to the ring oscillator, it is strongly affected by the temperature due to increasing leakage currents. Assuming $V_{DD}$=100 mV it increases across the full temperature range by a factor of 4. In contrast to a weaker dependency on the supply voltage by a factor of 1.5 at $T$ =25 °C. $V_{DD_{opt}}$ grows from 175 mV at −20 °C to 225 mV at 120 °C. Assuming room temperature, the minimum energy per operation is given by 21 fJ/op at 190 mV.



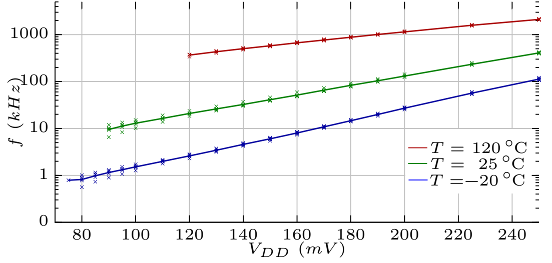

(a) Schematic of the 4 bit shift register.



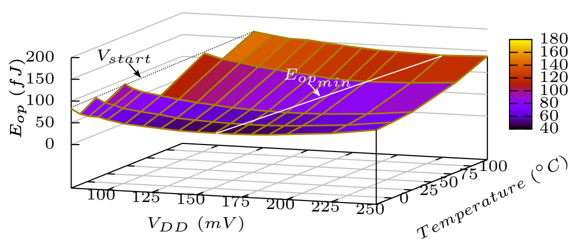

(b) Output signals of the 4 bit shift register at a supply voltage of 90 mV ($T = 25$ °C).




(c) Start-up voltage of the 4 bit shift register with respect to temperature.




(d) Maximum operation frequency with respect to supply voltage at different temperatures.




(e) Energy per operation of the 4 bit shift register.

Figure 2.17: Schematic and measurement data based on $N = 10$ samples of the 4 bit shift register. A temperature range from −20 °C to 120 °C is investigated at a supply voltage range from 80 mV to 250 mV. The average value and variation of individual test chips is plotted in the figures.

As shown in this section, the processing of mathematic operations using the ultra-low voltage digital cell library is made feasible by taking into account invalid interim states due to the extended propagation delay. To overcome this issue, sequential logic is recommended to hold the dissemination of the signal until a valid state is reached. An exemplary circuit using flip-flops is therefore discussed next.

### 2.4.3 4 bit Shift Register

This section is about demonstration and verification of a 4 bit shift register under ultra-low voltage conditions. In digital computation, shift registers are commonly used as a data

queue for serial to parallel conversion (or vice-versa) and consist of cascaded D flip-flops sharing the same clock signal. Their functionality can be explained as follows. The data present at the input ($In$) is shifted with each rising edge of the clock signal ($clk$), stage by stage according to a first in, first out principle through the array of gates. As a result, it appears delayed by $n$ clock cycles at the last stage's output with $n$ representing the number of stages.

For evaluation, the internal nodes of the shift register are lead through buffers to the pins, to separate them from the measurement equipment. The corresponding schematic is shown in Figure 2.17a. In Figure 2.17b an oscilloscope snapshot is presented, proving the functionality of the circuit at a supply voltage of 90 mV. The data input and clock signal are provided by a signal generator using an operation frequency of 5 kHz. As expected, the input signal is shifted by one stage with each rising edge.

Finding the minimum start-up voltage across the full temperature range is the next step in the evaluation process. Therefore, the internal nodes of the test chips are observed for bit-errors whilst successively decreasing the supply voltage at different temperatures. The data input and clock signal are again provided by a signal generator at a frequency of 100 Hz in order to exclude the propagation delay as an error source. The graph in Figure 2.17c shows a mean start-up voltage of 78 mV at −20 °C that linearly increases by a temperature coefficient of 271 µV/°C to 114 mV at 120 °C. At room temperature it is given by 90 mV. This is in agreement with the analysis of the basic logic cells in Chapter 2.3.

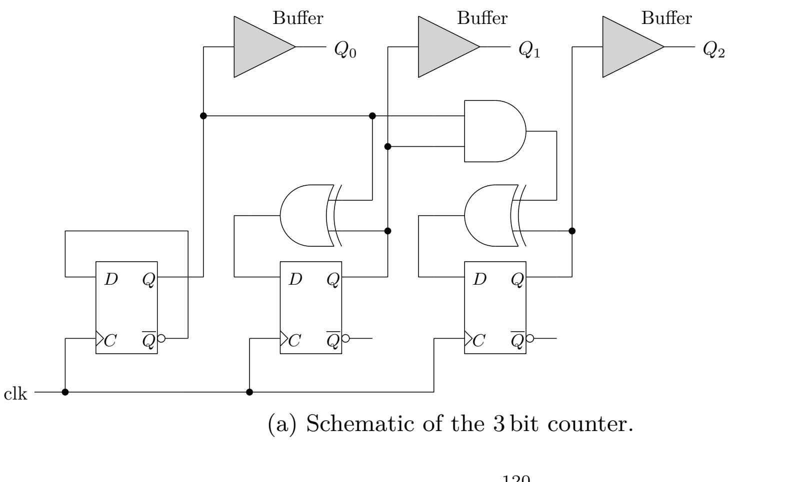
The maximum operation frequency over the supply voltage range is shown in Figure 2.17d. Starting from the low kHz-range, it increases exponentially with $V_{DD}$ and the temperature. To operate this circuit e.g. at 10 kHz across the full temperature range, a supply voltage of at least 160 mV needs to be provided.

Efficiency analysis is depicted in Figure 2.17e. The dependency of the optimum energy per operation point of the temperature is analogical to the previously discussed circuits. It increases from 44 fJ/op at 170 mV to 134 fJ/op at 225 mV across the full temperature range. Assuming room temperature, $E_{op_{min}}$ is given by 62 fJ/op at a supply voltage of 180 mV for the 4 bit shift register.

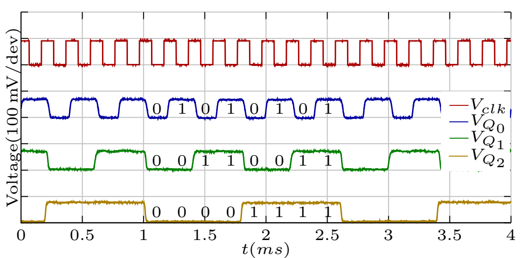
The currently discussed circuit consists exclusively of a chain of D flip-flops of the ultra-low voltage digital cell library with input signals taken from a signal generator. The last example shown is a 3 bit counter which extends the architecture of the shift register by combinational logic gates to define a desired sequence of the ouput signal.

### 2.4.4 3 bit Counter

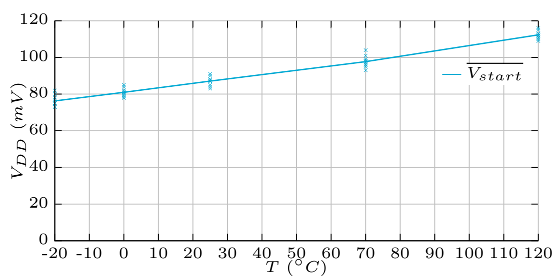
The aim of this section is the realization of a binary 3 bit counter by interconnection of flip-flops and combinational logic of the proposed ultra-low voltage digital cell library. Compared to the shift register, the data is generated internally by proper feedback loops and only the clock signal is provided by an external source. This circuit is therefore a good candidate for validating the functionality under ultra-low voltage conditions across the full temperature range.



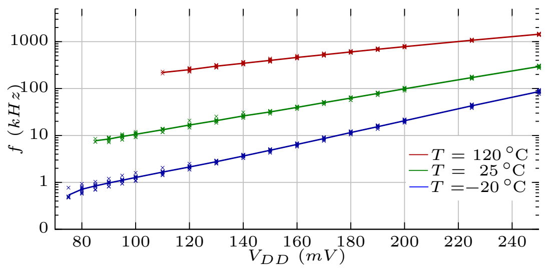

(a) Schematic of the 3 bit counter.



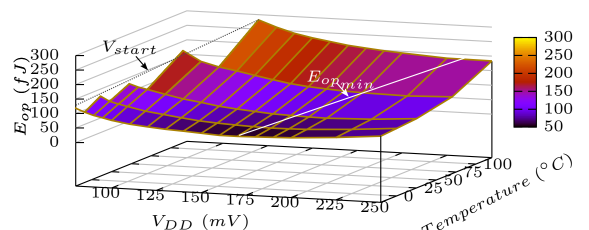

(b) Output signals of the 3 bit counter at a supply voltage of 90 mV ($T = 25\,°C$).




(c) Start-up voltage of the 3 bit counter with respect to temperature.




(d) Maximum operation frequency with respect to supply voltage at different temperatures.




(e) Energy per operation of the 3 bit counter.

Figure 2.18: Schematic and measurement data based on $N = 10$ samples of the 3 bit counter. A temperature range from −20 °C to 120 °C is investigated at a supply voltage range of 80 mV to 250 mV. The average value and variation of individual test chips is plotted in the figures.

In Figure 2.18a, the schematic of the 3 bit counter is shown. The binary digits are stored by three D flip-flops which are controlled by an external clock signal. Intermediary AND and EXOR gates ensure the desired number sequence. Unaffected monitoring of the internal nodes is achieved by adding unity gain buffers.

Operation at a supply voltage of 90 mV at 5 kHz is presented in Figure 2.18b. As shown, the count is incremented by one with each clock cycle. Due to the sequential processing no invalid

interim states occur. The measurement is done at room temperature.

To evaluate the minimum start-up voltage, the test chips are tempered accordingly and observed for bit-errors while successively decreasing the supply voltage at different temperatures. The corresponding measurement results are given in Figure 2.18c. From −20 °C to 120 °C, $V_{DD_{min}}$ grows linearly from 76 mV to 114 mV due to the decreasing gain. Similarly to the shift register, a temperature coefficient of 271 µV/°C is calculated from the data.

The maximum operation frequency over the supply voltage range is shown in Figure 2.18d. Starting from the low kHz-range, it increases exponentially with $V_{DD}$ and the temperature. Compared to the previously discussed shift register, operation of this circuit at 10 kHz across the full temperature range requires a supply voltage of at least 180 mV.

Analyzing energy per operation results in an $E_{op_{min}}$ of 51 fJ/op at 170 mV and 183 fJ/op at 230 mV considering −20 °C to 120 °C. For comparison, by operation at minimum supply voltage, energy per operation is increased to 116 fJ/op and 282 fJ/op.

## 2.5 Conclusion

Chapter 2 presented the development of an ultra-low voltage digital cell library providing an operational supply voltage range of 90 mV to 1.2 V. The results were achieved by using the Infineon 130 nm process technology, without any special process options such as Low-$V_T$ devices, or post-fabrication process steps.

Requirements and properties of circuits in the deep sub-threshold region were discussed first. In the second step, a standard CMOS inverter was analyzed in a low voltage domain which identified the uncorrelated process variation which was to be blamed for the malfunction. Successive modification of the architecture led to a new approach, improving the process variation sensitivity by 85 % at 80 mV. As a result, the minimum supply voltage is significantly reduced. Referring to Page 21, an instruction of compensation was defined and the modification of standard static logic gates in order for them to become ultra-low voltage-ready was explained. Additionally, layout considerations were discussed. The approach was used to design basic combinational and sequential logic gates.

Investigation of the functionality was performed using the gates to build basic digital logic circuits and the behavior across a temperature range of −20 °C to 120 °C at different supply voltages was analyzed. A summary of measurement data is given in Table 2.3. While higher temperatures lead to an increased supply voltage level requirement, the frequency range of proper operation grows by several orders of magnitude. By comparing the data, global limitation values are derived to be 77 mV at −20 °C, 89 mV at 25 °C and 115 mV at 120 °C. The optimum supply voltage for best efficiency is in the order of 170 mV at −20 °C, 190 mV at 25 °C and 250 mV at 120 °C.

The previous analysis confirms the strong influence of temperature and supply voltage on the performance of digital circuits operated in the deep sub-threshold region. A possible solution to this issue is to implement adaptive voltage or frequency domains. Therefore

| Ring oscillator | | | |
|---|---|---|---|
| Temperature | −20 °C | 25 °C | 120 °C |
| $V_{DD_{min}}$ | 65 mV | 75 mV | 98 mV |
| $V_{DD_{opt}}$ | 160 mV | 190 mV | 250 mV |
| $E_{op}$@$V_{DD_{min}}$ | 38 fJ | 61 fJ | 115 fJ |
| $E_{op}$@$V_{DD_{opt}}$ | 20 fJ | 30 fJ | 74 fJ |
| $E_{op}$@250 mV | 32 fJ | 36 fJ | 74 fJ |
| $f_{max}$@$V_{DD_{min}}$ | 0.37 kHz | 4.2 kHz | 140.7 kHz |
| $f_{max}$@$V_{DD_{opt}}$ | 4.6 kHz | 51.6 kHz | 1015 kHz |
| $f_{max}$@250 mV | 63 kHz | 196 kHz | 1015 kHz |

(a) Characteristic values of the 31-state ring oscillator.

| Full adder | | | |
|---|---|---|---|
| Temperature | −20 °C | 25 °C | 120 °C |
| $V_{DD_{min}}$ | 70 mV | 82 mV | 107 mV |
| $V_{DD_{opt}}$ | 140 mV | 160 mV | 200 mV |
| $E_{op}$@$V_{DD_{min}}$ | 20 fJ | 30 fJ | 86 fJ |
| $E_{op}$@$V_{DD_{opt}}$ | 13 fJ | 21 fJ | 56 fJ |
| $E_{op}$@250 mV | 22 fJ | 26 fJ | 58 fJ |
| $f_{max}$@$V_{DD_{min}}$ | 0.65 kHz | 8.8 kHz | 170 kHz |
| $f_{max}$@$V_{DD_{opt}}$ | 4.2 kHz | 45.2 kHz | 900 kHz |
| $f_{max}$@250 mV | 61 kHz | 217 kHz | 1412 kHz |

(b) Characteristic values of the full adder.

| Shift register | | | |
|---|---|---|---|
| Temperature | −20 °C | 25 °C | 120 °C |
| $V_{DD_{min}}$ | 77 mV | 89 mV | 115 mV |
| $V_{DD_{opt}}$ | 170 mV | 190 mV | 225 mV |
| $E_{op}$@$V_{DD_{min}}$ | 83 fJ | 108 fJ | 166 fJ |
| $E_{op}$@$V_{DD_{opt}}$ | 44 fJ | 63 fJ | 134 fJ |
| $E_{op}$@250 mV | 71 fJ | 79 fJ | 138 fJ |
| $f_{max}$@$V_{DD_{min}}$ | 0.79 kHz | 9.5 kHz | 367 kHz |
| $f_{max}$@$V_{DD_{opt}}$ | 11 kHz | 114 kHz | 1582 kHz |
| $f_{max}$@250 mV | 113 kHz | 408 kHz | 2111 kHz |

(c) Characteristic values of the 4 bit shift register.

| Counter | | | |
|---|---|---|---|
| Temperature | −20 °C | 25 °C | 120 °C |
| $V_{DD_{min}}$ | 76 mV | 89 mV | 114 mV |
| $V_{DD_{opt}}$ | 170 mV | 200 mV | 250 mV |
| $E_{op}$@$V_{DD_{min}}$ | 116 fJ | 156 fJ | 280 fJ |
| $E_{op}$@$V_{DD_{opt}}$ | 51 fJ | 74 fJ | 183 fJ |
| $E_{op}$@250 mV | 78 fJ | 89 fJ | 183 fJ |
| $f_{max}$@$V_{DD_{min}}$ | 0.49 kHz | 7.8 kHz | 252 kHz |
| $f_{max}$@$V_{DD_{opt}}$ | 8.5 kHz | 97.6 kHz | 1427 kHz |
| $f_{max}$@250 mV | 83 kHz | 285 kHz | 1427 kHz |

(d) Characteristic values of the 3 bit counter.

Table 2.3: Overview of the characteristics of the ultra-low voltage digital circuits.

a PTAT voltage reference with a similar temperature coefficient can be used to regulate $V_{DD}$ according to the temperature. On the other hand, as the clock frequency of a ring oscillator is affected analogically to the digital core by the environmental conditions, it is well suited to use as an automatic adapting clock reference. The corresponding draft is provided in Figure 2.19.

In Table 2.4 the proposed logic cells are compared to published representative similar works:[72] by A. Wang, [20] by S. Hanson and [20] by P.-H. Chen [8].

Based on the achievements described in this chapter a digital control unit, directly powered from a thermoelectric generator, can be developed in order to reduce the start-up voltage of a thermoelectric energy harvester.

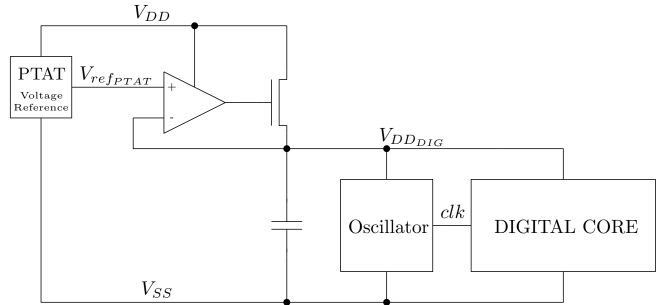



Figure 2.19: Power management unit of an ultra-low voltage digital core using a self-adapting supply voltage and frequency approach.

| Reference | [72] | [20] | [8] | **Own work [30]** |
|---|---|---|---|---|
| Published in | JSSC | JSSC | ISSCC | **ISCAS** |
| Year | 2005 | 2008 | 2011 | **2013** |
| CMOS Process | 180 nm | 130 nm | 65 nm | **130 nm** |
| Minimum Supply Voltage | 180 mV | 160 mV | 95 mV | **80 mV** |
| Post-fabrication | no | no | yes | **no** |
| Additional Circuitry Effort | no | yes | no | **no** |
| Special Process options | no | yes | no | **no** |

Table 2.4: Performance comparison of ultra-low voltage digital logic cells.

# Chapter 3

# Linear Charge Pumps for Ultra-Low Voltage Inputs

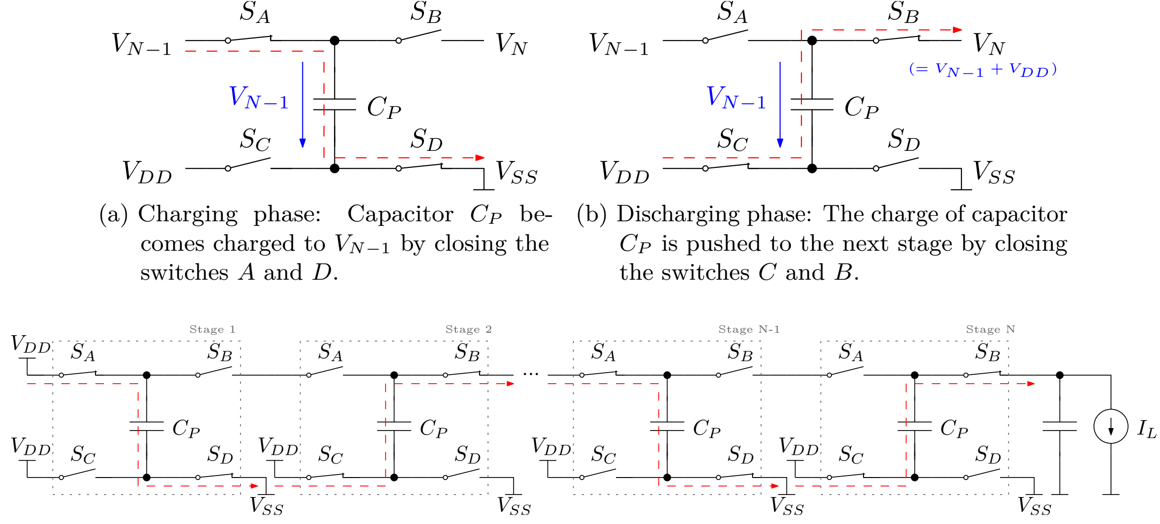
## 3.1 Introduction to Charge Pumps

A charge pump is a voltage converter that uses only capacitors and switches to step-up or step–down the supply voltage. Both components are available in semiconductor process technologies and their characteristics improve with technology scaling. Therefore a charge pump enables a fully integrated voltage converter solution. Instead of a continuous energy flow, switched capacitor power supplies deliver portions of charge with each cycle, leading to a load dependent ripple of the output voltage. This noise can be reduced through the use of a large output capacitor, a high clock frequency and multi-phase techniques.

The pumping stages generally have a simple design but to achieve high efficiency additional effort is required in the clock signal generator to overcome threshold voltage limitations and backwards conduction at the switches. The efficiency is mainly dictated by the switching control losses and the stray capacitances and is typically in the order of 60 % at higher conversion ratios in recent technologies [12, 44, 56, 57]. When using off-chip capacitors, up to 90 % efficiency is feasible [67, 74].

The principle architecture of a charge pump stage is shown in Figure 3.1. It consists of four switches ($S_{A...D}$) and a pumping capacitor ($C_P$), transferring charge from the input to the output by proper controlling of the switches. The operation can be divided into a charging and a discharging phase. During the charging phase the switches $S_A$ and $S_D$ are closed while $S_B$ and $S_C$ remain open (Figure 3.1a). As a result $C_P$ becomes charged to the voltage level provided at the upper input node ($V_{N-1}$). During the second phase, $S_A$ and $S_D$ are opened and the capacitor becomes interconnected between the lower input node ($V_{DD}$) and the output node ($V_N$) through $S_B$ and $S_C$ (Figure 3.1b). The voltage seen at $V_N$ is now given by the sum of $V_{N-1}$ and $V_{DD}$. Assuming $V_{DD}$ at both inputs results in a maximum output voltage of $2 \times V_{DD}$. Higher voltage conversion ratios are achieved by cascading inversely controlled stages with each stage increasing the open circuit output voltage linearly by $V_{DD}$. This topology is therefore known as linear charge pump.

In order to realize very high voltage conversion ratios, by reducing the number of stages used, nonlinear topologies were developed by proper interconnection of the pumping capacitors.




(a) Charging phase: Capacitor $C_P$ becomes charged to $V_{N-1}$ by closing the switches $A$ and $D$.

(b) Discharging phase: The charge of capacitor $C_P$ is pushed to the next stage by closing the switches $C$ and $B$.

(c) By cascading of inversly controlled stages the multiplication factor is adjusted. The open circuit output voltage is given by $(N + 1) \times V_{DD}$.

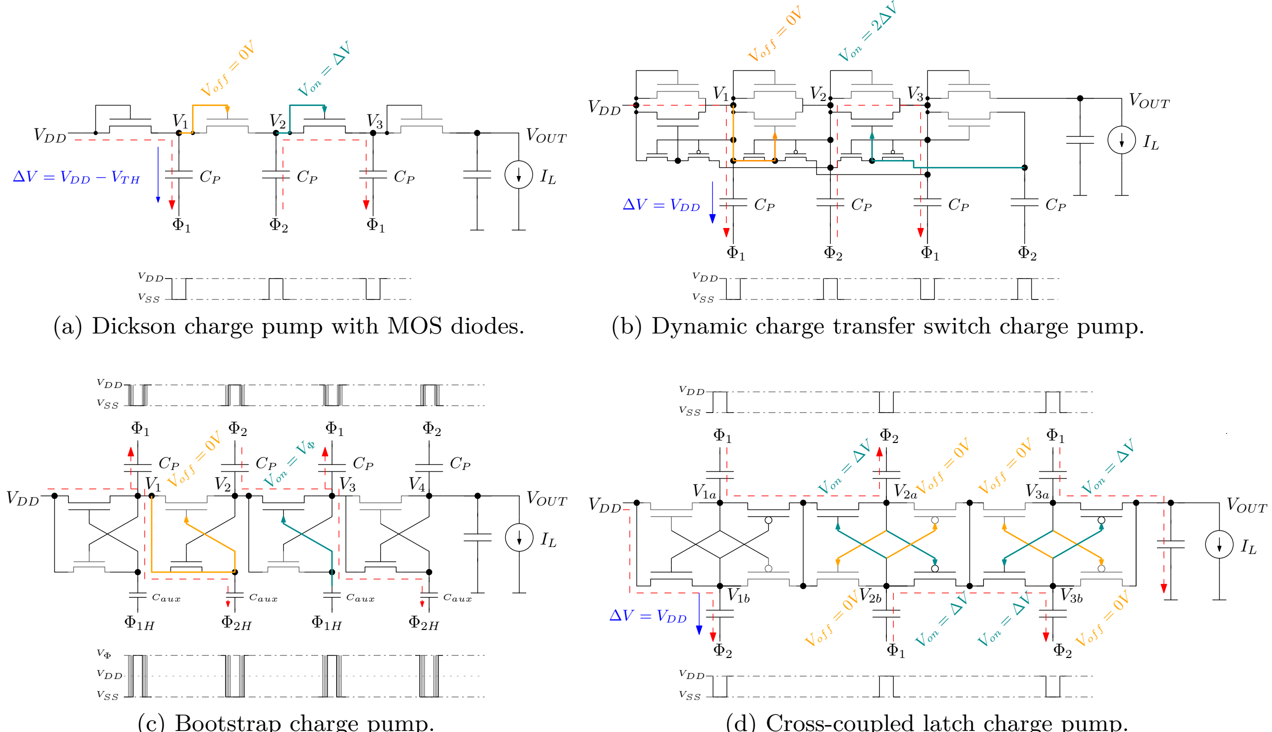
Figure 3.1: Schematic of an N-stage linear charge pump using active switches to control the current flow.

Examples are the Fibonacci charge pump [69] and exponential charge pump [6], growing like a Fibonacci sequence or exponentially with the number of stages. In [35], W.-H. Ki analyzed the on-chip performance of those circuits in comparison to linear charge pumps by taking into account the stray capacitances. He found the linear topology to be the best performing solution in fully integrated circuits. Linear charge pump characteristics are therefore discussed in more detail in the following section.

## 3.2 Gate Control Strategies under Low Voltage Conditions

Linear charge pumps are characterized by the way that the input voltage ($V_{DD}$) is always applied to the negative electrode of the pumping capacitor during the discharging phase. Therefore the parasitic stray capacitance of the bottom plate, which is typically large due to the small distance to the substrate, is fed by the input and doesn't subtract electric charge from the pumping capacitor itself. As a result, it does not influence the voltage gain of the circuit. The issue of stray capacitances is addressed in more detail later in this chapter. For the overview of charge pump topologies stray capacitances are neglected for simplicity in order to focus on gate control strategies under low voltage conditions.

In 1976 J. Dickson introduced a commonly used structure (shown in Figure 3.2a), using MOS transistors in a diode configuration to provide unidirectional charge flow [11]. The main advantage is a reduced control effort due to unnecessary active switching operations. Applying a two-phase clock is therefore sufficient for proper operation. As the voltage gain of each stage is reduced by the voltage drop of the MOS transistors threshold voltage, this circuit is of limited




(a) Dickson charge pump with MOS diodes.

(b) Dynamic charge transfer switch charge pump.

(c) Bootstrap charge pump.

(d) Cross-coupled latch charge pump.

Figure 3.2: Conventional charge pump control strategy for low voltage operation.

use under low voltage conditions. In fact, the minimum supply voltage must be greater than $V_{TH}$ of the last stage for proper functionality of the Dickson charge pump. This is due to the body effect, increasing the gate voltage necessary to establish a channel with growing source potential.

In order to overcome the voltage limitation of the Dickson topology, charge pumps based on charge transfer switches were introduced, using the higher potential of subsequent stages in order to sufficiently overdrive the switches. The first implementation with static backward control was presented in [79], showing issues with reversed current conduction [78]. Further improvements were achieved by dynamic backward control [77], which is depicted in Figure 3.2b. Considering the charging phase, the main switching transistor is in an off-state as the gate is connected to the inner node of the previous stage. During the discharging phase it is overdriven by twice the input voltage, which is derived from a subsequent stage. Due to the charge transfer switch technique, the minimum input voltage is reduced to $V_{TH}/2$ without increasing the control effort. Nevertheless, the last stage is still realized by a MOS diode affecting the overall voltage gain.

A further reduction of the minimum input voltage can be achieved by adding a bootstrapping circuit for each stage consisting of an additional MOS transistor and a capacitor [3, 37]. At the charging phase the gate of the power transistor is connected to the previous voltage node by the auxiliary MOS device, preventing reversed current conduction. At the discharging phase, the

bootstrapping capacitor enables a sufficient overdrive of the switch by the auxiliary clock signals $\Phi_{1H}$ and $\Phi_{2H}$. A proper gate voltage can be derived, for example, from the output node of the charge pump. Therefore, this circuit doesn't suffer from an input voltage limitation but requires a four-phase clock signal provided at different voltage amplitudes.

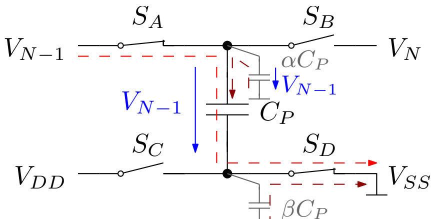
Another interesting solution is the Nakagome charge pump, first introduced in [51] and continuously adapted e.g. in [15, 17, 50]. This solution uses cross-coupled NMOS and PMOS switches realizing two pumping stages in parallel with one being operated in the charging phase while the second delivers charge to the subsequent stage. The effective frequency is therefore doubled, resulting in a reduced ripple of the output voltage. The charge transfer characteristic is shown in Figure 3.2d. As NMOS and PMOS devices behave inversely on a rising gate voltage, only one device is conducting at each clock phase. Nevertheless, using a simple 2-phase clock scheme results in backwards conduction during the switching operation as both devices are controlled simultaneously by one signal which is comparable to the cross current occurring in digital gates. To guarantee unidirectional charge flow, the individual control of each switch (through the use a non-overlapping clock signal) is mandatory; which in turn increases the complexity of the clock generator. The disadvantages are an increased on resistance due to the necessary series connection of both transistor types and a reduced overdrive voltage of the power switches caused by the discharging of the pumping capacitor. The minimum input voltage is again limited to $V_{TH}$.

The previously discussed switched capacitor voltage converter topologies can be realized by using PMOS transistors as power switches to overcome the body effect issue. In this case care has to be taken with the n-well potential in order to prevent a latch-up caused by the parasitic pn-junction of the PMOS device [58]. In the following section a steady-state analysis of the linear charge pump under ultra-low voltage conditions is performed. The aim is to discuss the output voltage and conversion efficiency under consideration of stray capacitances and the load current.

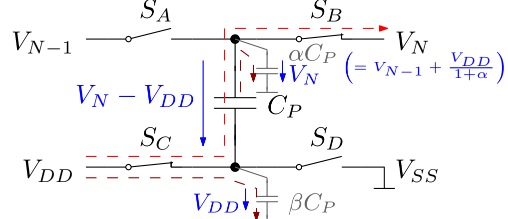
## 3.3 Impact of On-Chip Stray Capacitances

The efficiency and voltage gain of an integrated charge pump are highly affected by parasitic capacitances which are significant due to the small distances involved with on-chip implementations. As those parasitic devices influence the performance of the circuit, by taking part in the charge transfer process, they need to be considered in the design phase. Therefore the model of the pumping capacitor is typically extended by additional capacitors connected to ground, both for the top- ($C_\alpha$) and the bottom- ($C_\beta$) plate. The capacitance of $C_P$ depends on the process technology and grows with the area used for implementation. Similar behavior is observed for the parasitic capacitances. Their values can therefore be specified by proportionality factors $C_\alpha = \alpha\ C_P$ and $C_\beta = \beta\ C_P$.

In Figure 3.3, the adapted schematic of a pumping stage from Figure 3.1, including the parasitic devices, is depicted. Investigation of the circuit for each of the two clock phases lead to a modified steady-state charge transfer behavior. During the charging phase (Figure 3.3a), the energy stored in the parasitic bottom capacitor is dissipated to ground. The top capacitance




(a) Charging phase: The energy stored in $C_\beta$ is discharged to ground and is therefore dissipated while $C_\alpha$ redistributes charge to the pumping capacitor.




(b) Discharging phase: $C_\beta$ is charged by the input voltage ($V_{DD}$) while $C_\alpha$ subtracts charge from the pumping capacitor which affects the voltage gain.

Figure 3.3: Charge transfer phases of a linear charge pump including the effect of parasitic capacitances.

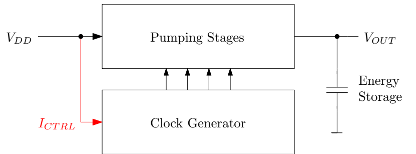
$C_\alpha$ redistributes charge back to the pumping capacitor as the top-plates potential decreases from $V_N$ to $V_{N-1}$. At the discharging phase (Figure 3.3b), $C_\beta$ becomes recharged from the input voltage ($V_{DD}$) while the charge of $C_P$ is distributed to the subsequent stage and partly to the parasitic top capacitance $C_\alpha$. This reduces the voltage gain of a pumping stage by $1/(1+\alpha)$ compared to the idealized circuit. In order to optimize the voltage gain, the parasitic top capacitance needs to be minimized. This can be achieved by increasing $C_P$ at a certain area by using smaller technologies or implementing vertically oriented structures. The bottom plate capacitor on the other hand is charged by $V_{DD}$ and therefore doesn't drain any charge from the pumping capacitor. As a result, $C_\beta$ doesn't influence the voltage gain but has an impact on the efficiency of the DC/DC converter.

## 3.4 Modeling of Self-Sustaining Linear Charge Pumps

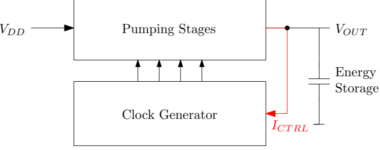
The analytical description is required to estimate the performance and optimize the design of a DC/DC converter. The charge balance law is a powerful tool used to analyze the steady state behavior of switched capacitor circuits. It was introduced by W.-H. Ki in [34] and was later used in [35] to derive the charge transfer characteristic for different charge pump topologies.

In a conventional design approach for capacitive DC/DC converters the logic circuitry for clock generation and switch control is powered from the input node which limits the minimum $V_{DD}$ to the threshold voltage (Figure 3.4a). When implementing ultra-low voltage charge pumps this limitation can be circumvented by using the output node to supply the control logic. Such a circuit has to deliver its own control power and is therefore required to be self-sustaining (Figure 3.4b). In this configuration, sufficient overdrive of the switches is guaranteed to be independent of the input voltage at the cost of a base load current ($I_{CTRL}$).

Detailed investigation of conventional linear charge pumps has already been performed in literature by W.-H. Ki in [34, 35] and G. Palumbo in [54, 55, 57]. These papers provide analytical description of conventional linear charge pumps and present guidelines to optimize




(a) Conventional charge pump. The control logic is powered from the input node.




(b) Self-sustaining charge pump. The output node provides power to the control logic.

Figure 3.4: Comparison of power supply concepts for the control logic.

the design in terms of voltage gain and conversion efficiency. However, base load current at the output node was omitted in the formulas presented. Therefore, the expressions provided are not valid for self-sustaining charge pumps and need to be expanded. In the following section the steady-state behavior of self-sustaining charge pumps is investigated in detail and expressions for voltage gain and efficiency are derived.

### 3.4.1 Voltage gain

In [35], the charge balance approach was used to derive a general expression of the steady-state output voltage ($V_{OUT}$) of a linear charge pump under consideration of parasitic capacitances ($C_\alpha$ and $C_\beta$) and the load current ($I_L$). The corresponding equation is given in (3.4.1) with $N$ denoting the number of stages and $f$ the clock frequency. Additional stages increase $V_{OUT}$ while parasitics and the load current counteract.

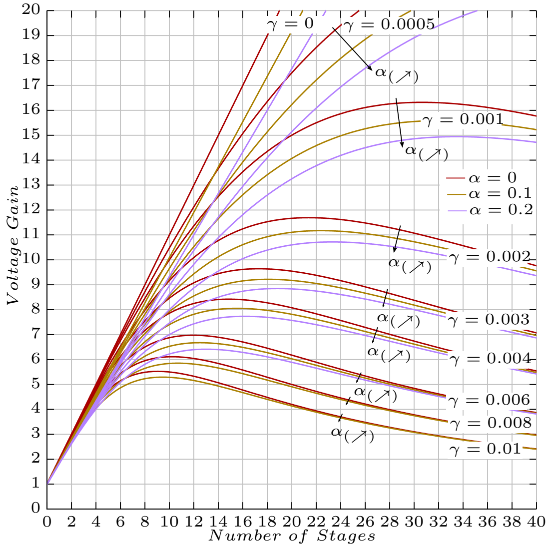
$$V_{OUT} = V_{DD} \cdot \left(1 + \frac{N}{1+\alpha}\right) - \frac{I_L}{f \cdot C_P} \cdot \left(\frac{N}{1+\alpha}\right) \tag{3.4.1}$$

The load current $I_L$ contains the output current $I_{OUT}$ and the control effort current $I_{CTRL}$ as shown in (3.4.2). The latter considers the charge required within each clock cycle to drive the switches of the pumping stages and therefore increase with $N$. As the control effort at a certain frequency grows proportionally with $C_P$, for example due to larger switches, it can be specified by a control effort proportionality factor $\gamma$. The complete expression of $I_{CTRL}$ is given in (3.4.3).

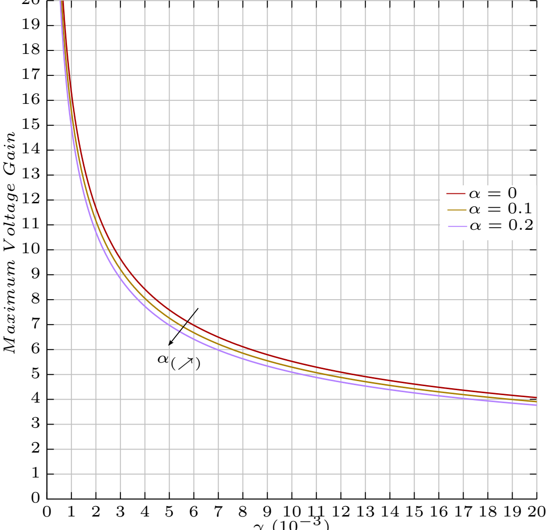
$$I_L = I_{OUT} + I_{CTRL} \tag{3.4.2}$$

$$I_{CTRL} = \gamma \cdot N \cdot V_{OUT} \cdot C_P \cdot f \tag{3.4.3}$$

The impact of $I_{CTRL}$ on the output voltage is calculated by substituting (3.4.3) and (3.4.2) in equation (3.4.1). Rearranging to $V_{OUT}$ results in an extended expression for the output voltage of self-sustaining charge pumps as shown in (3.4.4). Compared to (3.4.1), the control effort




(a) Voltage gain in dependency of the number of stages for different control effort factors ($\gamma$). In addition the impact of the parasitic top-plate capacitance is plotted.




(b) Maximum achievable voltage gain in dependency of the control effort factor ($\gamma$), which becomes further reduced by the parasitic top-plate capacitance.

Figure 3.5: Calculated voltage gain versus the number of stages considering the impact of parasitic capacitances and control effort losses.

factor $\gamma$ extends the denominator of the equation and shows a quadratical dependency on the number of stages.

$$V_{OUT} = V_{DD} \cdot \left( \frac{1 + \alpha + N}{1 + \alpha + \gamma N^2} \right) - \frac{I_{OUT}}{f \cdot C_P} \cdot \left( \frac{N}{1 + \alpha + \gamma N^2} \right) \tag{3.4.4}$$

$$G_0 = \frac{V_{OUT_0}}{V_{DD}} = \frac{1 + \alpha + N}{1 + \alpha + \gamma N^2} \tag{3.4.5}$$

Due to the duty-cycled operation in energy harvesting applications, the DC/DC converter delivers power to an energy storage device which is typically disconnected from the load (e.g. sensor, transmitter,...). The output current is therefore negligible in the discussion of the open-circuit voltage gain ($G_0$), which represents the maximum achievable voltage gain under consideration of parasitic losses. In (3.4.5), the expression $G_0$ is given with the corresponding plot in Figure 3.5a versus the number of stages for different values of $\gamma$ and $\alpha$. Due to the quadratic dependency, the control effort factor $\gamma$ significantly influences the voltage gain with growing $N$. In fact, the characteristic curve shows a maximum for a certain number of stages and degenerates again for higher values of $N$. A less significant reduction is determined by the parasitic top-plate capacitance which also influences the voltage gain. In comparison to the conventional charge pump, an arbitrary gain is not possible by cascading.

Deriving relationship (3.4.5) for $N$ and setting it to zero results in the equation for an optimum number of stages which can then be used to calculate the maximum achievable voltage gain for a certain control effort factor. The corresponding plot is shown in Figure 3.5b. Using the characteristic curves of Figure 3.5 allows a first estimation of the requirements and limitation regarding achievable voltage gain for self-sustaining charge pumps. If a voltage gain of 11 is desired and assuming $\alpha = 0.1$ results in an optimum $N$ of 22 and a control effort factor that may not exceed $2 \cdot 10^{-3}$. Higher voltage gains require even lower values of $\gamma$ and therefore significantly increase the design complexity of the control logic in order to reduce $I_{CTRL}$ accordingly.

### 3.4.2 Efficiency

In power converting systems the efficiency indicates the amount of power that is lost during the voltage conversion process. It is typically defined by the ratio of the output power ($P_{OUT}$) compared to the input power ($P_{IN}$). Assuming steady-state those values are given by the product of the average current and the voltage at the corresponding nodes (3.4.6). The output voltage is already known from the previous section. Therefore the expressions of $I_{OUT}$ and $I_{IN}$ need to be derived.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \cdot I_{OUT}}{V_{DD} \cdot I_{IN}} \tag{3.4.6}$$

The output current is already included in (3.4.4) and is therefore evaluated by solving the equation for $I_{OUT}$. The resulting expression is shown in (3.4.7) with $G$ representing the effective voltage gain ($G = V_{OUT}/V_{DD}$). Since a charge pump delivers portions of charge, a meaningful approach is to describe the contributing terms using charge per clock cycle. The resulting output current depends therefore on charge transferred within each clock cycle of a lossless charge pump ($\Delta Q_{ideal}$) minus the charge lost due to the parasitic top-plate ($\Delta Q_{\alpha}$) and the charge taken by the control logic ($\Delta Q_{\gamma}$). While $\Delta Q_{\alpha}$ only shows a weak influence, the control effort losses significantly reduce $I_{OUT}$ with growing $G$ and $N$.

$$I_{OUT} = \frac{\Delta Q_{ideal} - \Delta Q_{\alpha} - \Delta Q_{\gamma}}{T} = f \cdot C_P \cdot V_{DD} \cdot \left(1 - \frac{G-1}{N} \cdot (1+\alpha) - G \cdot N \cdot \gamma\right) \tag{3.4.7}$$

After the output current has been determined, the input current is investigated. Three main contributors can be found:

- **Input current related to the load condition ($I_{L_{IN}}$)**: $I_{L_{IN}}$ considers the amount of charge ($\Delta Q$) transferred within each clock cycle from stage to stage providing the output current by assuming an ideal charge pump behavior without energy losses. It is taken from the power supply at each input node ($N + 1$) of the circuit. The control effort factor $\gamma$ is already considered by the expression for $I_L$ (3.4.8).

$$I_{L_{in}} = (N+1) \cdot \frac{\Delta Q_L}{T} = (N+1) \cdot I_L \tag{3.4.8}$$

- **Input current related to the parasitic top-plate capacitance ($I_{C_\alpha}$)**: Since $C_\alpha$ is connected in parallel to $C_P$ some charge ($\Delta Q_\alpha$) is temporarily stored in the parasitic capacitor during the charging phase which causes energy losses. It can be calculated by using (3.4.1) to investigate the voltage drop at the output in dependency on $\alpha$ by subtracting $V_{OUT}$ in an ideal case ($\alpha = 0$) from the real case (3.4.9).

$$I_{C_\alpha} = \frac{\Delta Q_\alpha}{T} = \frac{C_P}{T} \cdot \left( V_{OUT_{|\alpha=0|}} - V_{OUT} \right) = N \cdot \frac{\alpha}{1+\alpha} \cdot (f \cdot C_P \cdot V_{DD} - I_L) \tag{3.4.9}$$

- **Input current related to the parasitic bottom-plate capacitance($I_{C_\beta}$)**: $C_\beta$ is completely charged and discharged between $V_{DD}$ and $V_{SS}$ which applies to all stages. Therefore the input current caused by the corresponding amount of charge dissipated within each clock cycle is given by (3.4.10).

$$I_{C_\beta} = \frac{\Delta Q_\beta}{T} = N \cdot \beta \cdot C_P \cdot f \cdot V_{DD} \tag{3.4.10}$$

The total current consumption ($I_{IN}$) in steady state is given by summation of the contributors (3.4.8), (3.4.9) and (3.4.10). Using (3.4.2) and (3.4.7) simplifies the expression to equation (3.4.11) which represents $I_{IN}$ dependent on the number of stages and the voltage gain.

$$I_{IN} = f \cdot C_P \cdot V_{DD} \cdot \left( 2 + N \cdot (1+\beta) - \frac{G-1}{N} \cdot (1+\alpha) - G \right) \tag{3.4.11}$$

Substituting the current equations (3.4.7) and (3.4.11) into (3.4.6) leads to a general expression for the efficiency ($\eta$) of the self-sustaining charge pump shown in (3.4.12). It is worth noting that the efficiency depends neither on the frequency nor the pumping capacitor but is only defined by the technology parameters ($\alpha$ and $\beta$), the number of stages and the effective voltage gain.

$$\eta = G \cdot \frac{1 - \frac{G-1}{N} \cdot (1+\alpha) - G \cdot N \cdot \gamma}{2 + N \cdot (1+\beta) - \frac{G-1}{N} \cdot (1+\alpha) - G} \tag{3.4.12}$$

### 3.4.3 Optimum Number of Stages

To calculate the number of stages for maximum efficiency in dependency of the voltage gain, (3.4.6) is derived with respect to $N$ and the result is set to zero. The corresponding equation is given in (3.4.13) in a simplified manner by omitting dispensable terms without introducing a significant error.

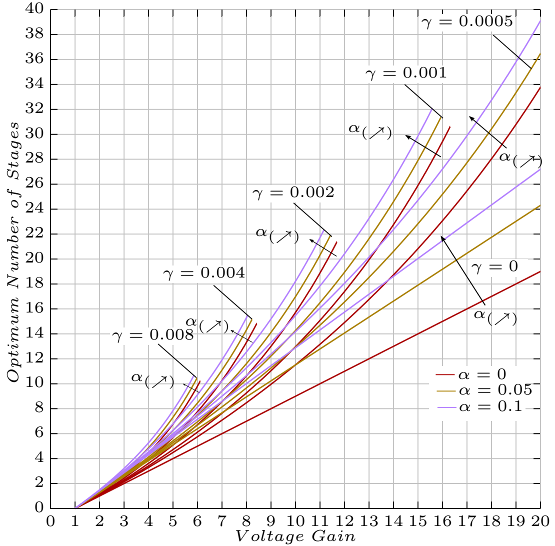
$$N_{opt} \approx (G-1) \cdot \frac{1+\alpha+\beta+G\cdot\gamma+\sqrt{\alpha+\beta+G^2\cdot\gamma\cdot(1+\alpha)}}{1+\beta-G\cdot\gamma\cdot(G-2)} \tag{3.4.13}$$

Using this relationship, the optimum number of stages ($N_{opt}$) can be plotted versus $G$ for different technology parameters. In Figure 3.6a, the optimum number of stages considering different values of $\alpha$ and $\gamma$ while neglecting the bottom-plate capacitance ($\beta = 0$) is shown. In contrast to Figure 3.6c where a similar plot by assuming $\alpha = 0$ for different values of $\beta$ and $\gamma$ is depicted. The end points of the curves represents $\eta$ =0 % which corresponds to the voltage gain limitation derived in Chapter 3.4.1. From the figures, a weak dependency on the efficiency of technology related parasitic parameters ($\alpha$ and $\beta$) in modern process technologies can be observed. On the other hand the control effort factor significantly influences the result. For example, assuming $\alpha = \beta = 0$ and a required voltage gain of 10 leads to 16 stages for $\gamma = 0.002$ by inspection of the characteristic curves. Halving the control effort factor saves three stages while the desired voltage gain is not feasible assuming $\gamma = 0.004$.

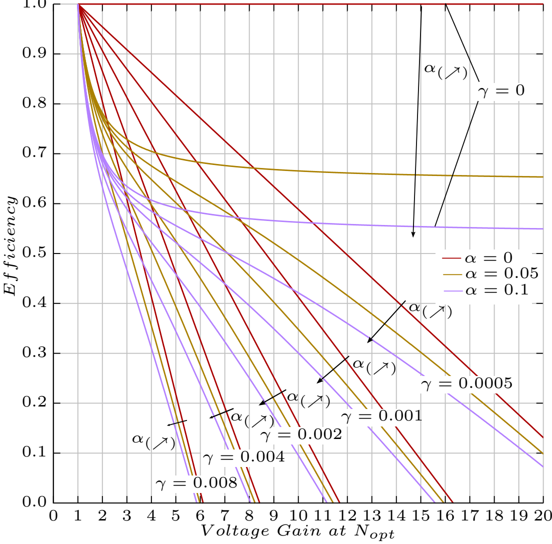
By considering a design using the optimum number of stages, calculation of the maximum efficiency is feasible by inserting the expression of optimum number of stages into (3.4.6). The resulting characteristic curves are plotted in Figure 3.6b and Figure 3.6d versus the voltage gain for the same parameter setting used in the previous section. The efficiency of conventional on-chip implementations ($\gamma = 0$) tends asymptotically to a constant value in the order of 60 % with growing values of G which agrees with the assumption in the beginning of the chapter. However, in self-sustaining charge pumps ($\gamma > 0$) it decreases successively with larger voltage gains. Taking the previous example and assuming $\gamma = 0.002$, the maximum efficiency is given by approximately 15 % but increases up to 40 % at $\gamma = 0.001$.

## 3.5 Conclusion

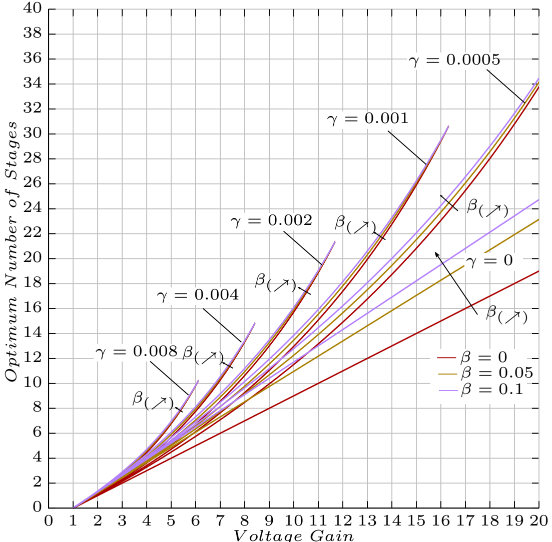
In Chapter 3, the theoretical background of linear charge pumps for ultra-low voltage domains was prepared. Therefore the principle architecture of low voltage charge pumps from the literature was discussed, focusing on gate control strategies to maintain operation under low voltage conditions. During this investigation bootstrapping turned out to enable a supply independent overdrive of the switches which prevents from an input voltage limitation. Cross-coupled switches are another interesting solution used to improve the output current without increasing the control complexity. Based on the achievements, a hybrid system of both topologies will be developed in the following chapter in order to develop an ultra-low voltage charge pump for thermoelectric energy harvesting operational in the deep sub-threshold region.



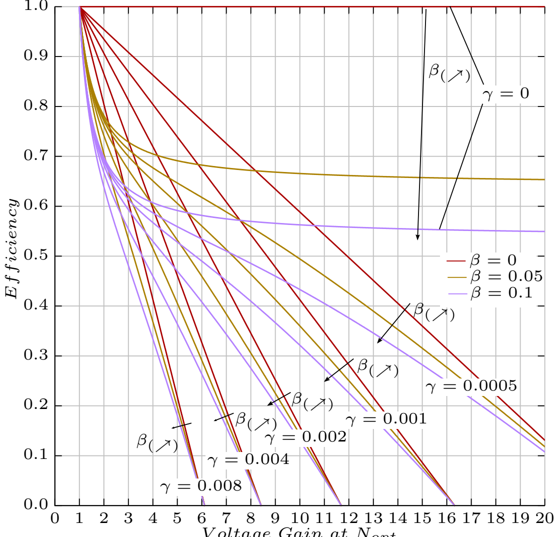

(a) Optimum number of stages to achieve maximum efficiency in dependency on the voltage gain. In addition the impact of the control effort and the parasitic top-plate capacitance is considered.




(b) Maximum efficiency in dependency on the voltage gain using optimum number of stages including the effect of of the control effort and the parasitic top-plate capacitance.




(c) Optimum number of stages to achieve maximum efficiency in dependency on the voltage gain. In addition the impact of the control effort and the parasitic bottom-plate capacitance is considered.




(d) Maximum efficiency in dependency on the voltage gain using optimum number of stages including the effect of the control effort and the parasitic bottom-plate capacitance.

Figure 3.6: Calculated efficiency versus the number of stages considering the impact of parasitic capacitances and control effort losses.

The second part of the chapter deals with the development of an analytical steady state model of the self-sustaining charge pump. It provides characteristic curves of voltage gain and efficiency in comparison to process- and control-related parasitic effects in order to estimate the performance of self-sustaining DC/DC converters. In addition, the optimum number of stages required to achieve maximum efficiency was calculated therefore enabling an optimized design flow.

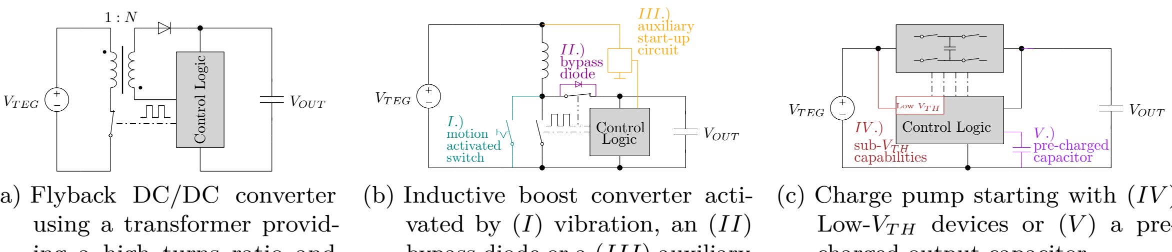
# Chapter 4

# Design of a Fully Integrated Thermoelectric Energy Harvester with Sub-threshold Start-up Capability

## 4.1 Introduction

In Chapter 1.3, the characteristics of a thermoelectric generator in Body Area Networks was found to provide a DC voltage in the order of 100-200 mV. The basis of any thermoelectric energy harvester is therefore an ultra-low voltage DC/DC converter for up-conversion of the input to a "usable" supply voltage level in a certain process technology. The key challenges of such a system are the high conversion ratio and the start-up procedure, as in the initial state there is no higher voltage available than provided by the thermoelectric generator. To overcome these issues three circuit topologies and several start-up mechanisms can be found in literature. An overview is depicted in Figure 4.1:

- **Flyback converter**: A flyback converter (Figure 4.1a) consists of a transformer with the primary side connected to the source while the secondary side is followed by a rectifying diode and an output capacitor. In order to operate the transformer, DC to AC conversion of the input signal needs to be performed by adding a switch to the primary loop. The control logic which is powered from the output node has to provide the corresponding clock signal. The conversion ratio is defined by the turns ratio of the transformer and therefore easily enables high voltage gains. By using a depletion-mode transistor the current on the primary side immediately starts to flow when connecting the source to the circuit. This causes an initial voltage induction on the secondary side which is sufficient to start the control logic circuit. Flyback converters therefore achieve the lowest start-up voltage (e.g. 20 mV in [47] or 40 mV in [23]) and the highest voltage gain at the cost of bulky external components. The efficiency shows a maximum at low input voltages but decreases with rising $V_{TEG}$ due to the fixed turns ratio of the transformer. In terms of efficiency, the inductive boost converter improves its behavior as the input voltage increases. Therefore in [23], flyback and inductive boost operation are combined in a single circuit.
- **Inductive boost converter**: The conventional boost converter connects a coil alternately to ground and the output capacitor in order to charge the latter to higher voltage




(a) Flyback DC/DC converter using a transformer providing a high turns ratio and a depletion-mode transistor switch.

(b) Inductive boost converter activated by ($I$) vibration, an ($II$) bypass diode or a ($III$) auxiliary start-up circuit.

(c) Charge pump starting with ($IV$) Low-$V_{TH}$ devices or ($V$) a pre-charged output capacitor.

Figure 4.1: Circuit topologies of thermoelectric energy harvesting systems considering different start-up strategies.

levels (Figure 4.1b). Again, the control logic is powered from the initially discharged output node which requires a start-up mechanism. In [59], a motion activated switch is used to initialize the kick-off at $V_{TEG} = 35\,\text{mV}$. Therefore mechanical forces are required which might not occur in a certain environment. Another approach is to use a bypass diode to pre-charge the output or directly take the power from the input which leads typically to a start-up voltage greater than 330 mV ([1, 25]). A frequently applied solution is an auxiliary start-up circuit typically realized by a small charge pump to pre-charge the output as shown in [21, 45]. This solution suffers from similar start-up voltage limitations. Reducing the threshold voltage with post-processing hot carrier injection [8] or using Low-$V_{TH}$ transistors [75] enable a successful kick-off in the range of $50-80\,\text{mV}$. Compared to the flyback converter, the inductive boost converter is smaller in size as it typically uses a single external coil and provides a higher efficiency over a wide range of input voltages.

- **Charge pump**: The capacitive DC/DC converter (Figure 4.1c) is independent of external devices and is therefore an interesting solution in energy harvesting applications. Nevertheless, the start-up procedure is even more complicated as an increased amount of control signals are required to turn the switches on an off accordingly. Therefore 250 mV are achieved in [19, 33]. Reducing $V_{TH}$ using forward body biasing [7, 36] enables a lower start-up at $150-180\,\text{mV}$ in standard process technologies. Without the need of external components, charge pumps are the most compact solution, but their power transfer efficiency is typically lower (especially for high conversion ratios) in comparison to the topologies previously presented.

The aim of this chapter is the design of a thermoelectric energy harvester with self-starting capabilities using Infineon 130 nm process technology. In order to realize a fully integrated solution a capacitive DC/DC topology is chosen. A successful start-up below 150 mV is targeted by using the ultra-low voltage digital cell library. In operation, a variation of the input voltage between 130 mV and 300 mV is expected. The nominal output voltage is 1.2 V which results in a conversion ratio of 4-10. The specification of the thermoelectric energy harvester is given in Table 4.1.

| | |
|---|---|
| Start-up Voltage | <150 mV |
| Input Voltage | 130 – 300 mV |
| Output Voltage | 1.2 V |
| Voltage Gain | 8-10 |
| Start-up Mechanism | self-starting |
| External Components | no |

Table 4.1: Specification of the thermoelectric energy harvester.

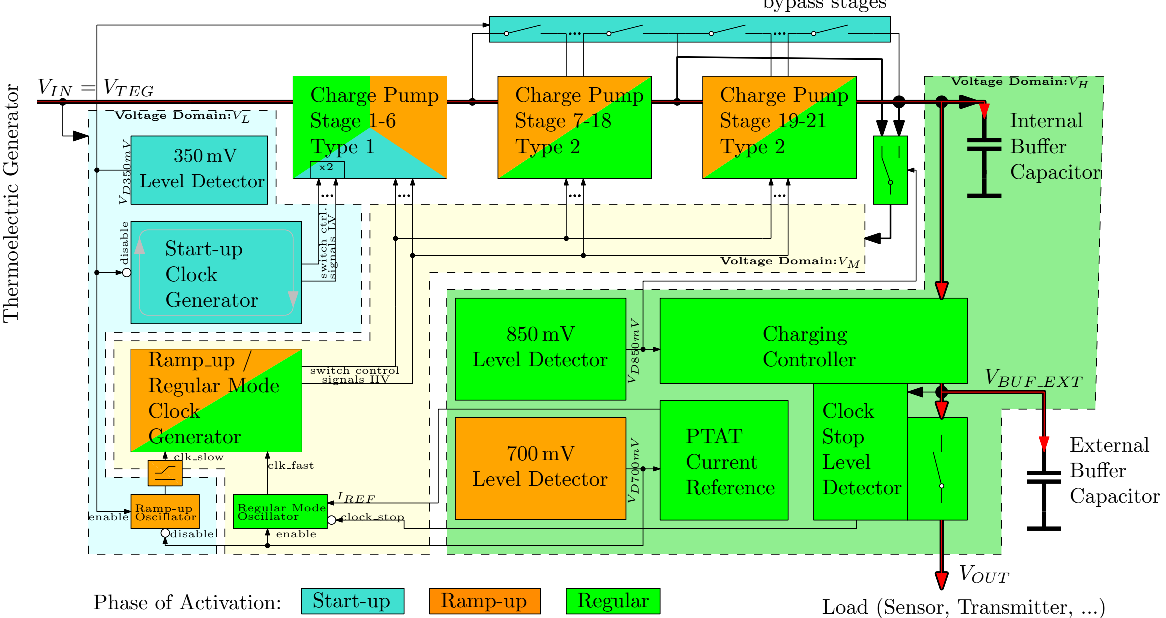



Figure 4.2: System architecture of the fully integrated thermoelectric energy harvester.

## 4.2 System Architecture

In this section a general overview of the proposed thermoelectric energy harvester topology is given on a functional basis. A capacitive DC/DC converter is used to realize a fully integrated solution. The system architecture is depicted in Figure 4.2. To achieve the desired voltage conversion ratio, 21 pump stages are added together. From this quantity, only 6 are used during the start-up phase while the others are initially bypassed. This is to reduce the capacitive load of the start-up clock generator in order to lift the voltage level at the internal buffer capacitor node out of the sub-threshold region. Afterwards, the chain of pump stages is extended by cascading all 21 stages. Two types of pump stages are used. Type 1 (Chapter 4.4.1) contains voltage doublers and switches suitable for sub- and super-threshold operation while type 2 (Chapter 4.4.2) is only usable in super-threshold operation but is smaller in layout area.

When applying a voltage to the input node, the circuit has to run through three operation

modes. These are subdivided into start-up, ramp-up and regular mode, until it delivers power to the load. During the modes, the power supply of the sub-circuits is successively changed from the input node to the output node of the pump stages in order to obtain a self-sustaining system. As not all sub-circuits are active in each mode, the background color of the building blocks in Figure 4.2 indicate the corresponding affiliation. The respective mode is determined by the voltage level at the internal buffer capacitor ($V_H$) and sets different requirements of the participating sub-circuits.

Several sub-circuits are used to control the DC/DC converter accordingly. For functionality and efficiency reasons they are powered from three different supply voltage domains. The low supply voltage domain, $V_L$, is directly connected to the input of the harvesting circuit and is indicated in the figure by a light-cyan background bounded with dashed lines. The corresponding building blocks require sub-threshold operation capabilities and are typically active during the start-up phase. The medium supply voltage domain, $V_M$, is derived from the internal buffer capacitor during the ramp-up phase and from an intermediate node of the pump stages in regular mode operation. It reduces the power losses for generation of the control signals used to drive the switches. In the figure, a light-yellow color represents the corresponding voltage domain. Finally, the high supply voltage domain, $V_H$, indicated by a light-green background, is derived directly from the output node of the last pump stage.

For start-up, a free-running sub-threshold clock signal generator (Chapter 4.5.1) based on logic gates of the ultra-low voltage digital cell library is used. It is completely powered from the low voltage domain and uses clock doublers to drive the switches of the type 1 pump stages accordingly while the type 2 stages are bypassed. The frequency is typically low and undefined as it depends highly on the input voltage ($V_{IN}$), process parameters and temperature.

At a voltage level of $V_H = 350\,\text{mV}$ at the internal buffer capacitor, the free-running start-up clock signal generator is stopped by the 350 mV level detector (Chapter 4.7.1) in order to initialize the ramp-up phase. Therefore the ramp-up oscillator (Chapter 4.6.1) and the regular mode clock generator (Chapter 4.5.2) are enabled. Both circuits are powered from different voltage domains using a level shifter in between. The former is part of the low voltage domain while the latter is connected to $V_M$. As a result, the power losses during the ramp-up phase are limited to the clock signal generator while the oscillator doesn't put an additional load on the internal buffer capacitor. Compared to the start-up mode, the clock signal of the ramp-up oscillator is 10 times faster which is feasible as the regular mode clock generator drives the switches at a reasonable supply voltage of $V_H > 350\,\text{mV}$. In addition the number of active pump stages is increased to 21 by deactivating the bypass switches. This allows a higher voltage conversion ratio and increases the output current charging the internal buffer capacitor.

At $V_H > 700\,\text{mV}$, the 700 mV level detector (Chapter 4.7.2) initializes the regular operation mode by disabling the ramp-up oscillator and enabling the regular mode oscillator (Chapter 4.6.2). The latter is basically a relaxation oscillator using a PTAT current reference to generate a well-defined clock frequency of about 700 kHz. Now both the oscillator and the clock signal generator put a load on the internal buffer capacitor. By reaching a voltage level of 850 mV (Chapter 4.7.2), the medium supply voltage domain is decoupled from the internal buffer capacitor and connected

| Mode | Voltage Range | Supply concept | Load current | Frequency | Frequency stability | Switch control voltage |
|---|---|---|---|---|---|---|
| **Start-up** | $< 350\,\mathrm{mV}$ | $V_{IN}$: Free-running Clock Generator (x2 x2 x2 x2) | no | low | bad | $2 \cdot V_{IN}$ |
| **Ramp-up** | $350\,\mathrm{mV}$-$700\,\mathrm{mV}$ | $V_{IN}$: Ramp-up Oscillator; $V_M$: High Voltage Clock Generator | moderate | medium | moderate | $V_M = V_H$ |
| **Regular** | $> 700\,\mathrm{mV}$ | $V_M$: Current Reference, Regular Mode Oscillator, High Voltage Clock Generator | full | high | good | $V_M$ |

Table 4.2: Characteristics of the three operation modes of the thermoelectric energy harvester.

to an intermediate node of the pump stages. As a result, the power losses due to the regular mode clock generator are reduced which increases the efficiency and conversion ratio of the overall circuit. In addition the charge controller is enabled. The characteristics of the three operation modes are summarized in Table 4.2.

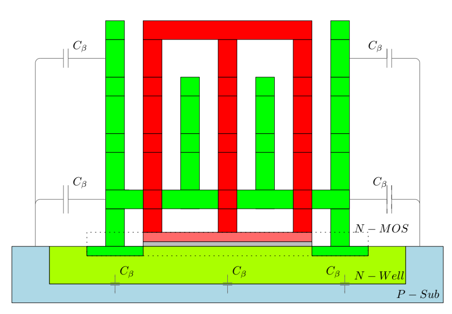
After finishing the start-up and ramp-up operation the internal buffer capacitor is pre-charged and the control unit can be completely powered from the output node in the regulator mode operation. At this point in time, charge can be transfered to the load of the harvesting circuit which will be explained next.

Charge is transfered from the input ($V_{IN}$) through the pump stages to an internal buffer capacitor ($V_H$). As it provides power to most of the sub-circuits in regular mode operation, the voltage level $V_H$ has to remain above a certain value to maintain functionality. Therefore the charging controller monitors the node and controls the charge transfer from the internal to the external buffer capacitor ($V_{BUF\ EXT}$) in a way that prevents the latter from discharging the former. The external buffer capacitor is connected to the output node ($V_{OUT}$) using a switch that is controlled by the clock stop level detector. In addition, this circuit disables the oscillator at the nominal output voltage.

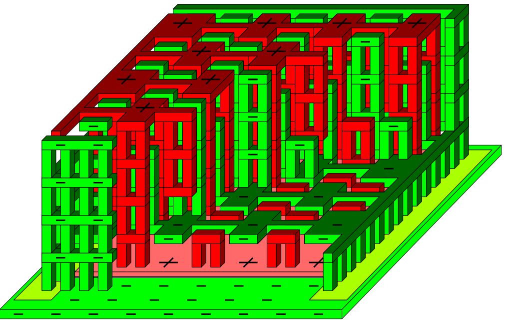
In the following chapters 4.3 to 4.8, the architecture and functionality of the sub-circuits including simulations and measurement results are discussed in detail. Finally, measured results of voltage gain, output current and efficiency based on 10 test chips containing the harvesting system are presented in Chapter 4.9.

## 4.3 On-chip Capacitor

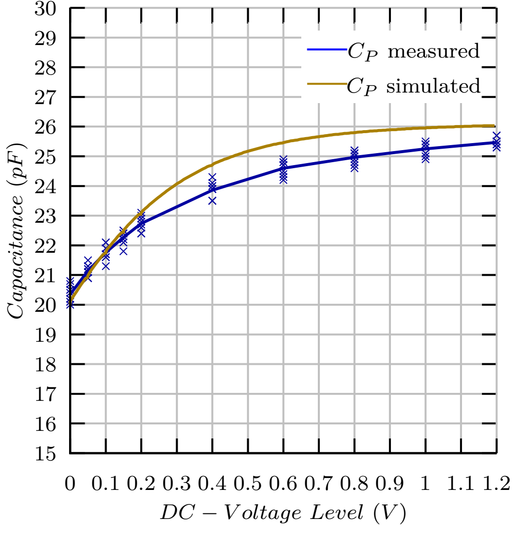
Process technologies provide several opportunities to realize on-chip capacitors which improve their quality with advanced technologies. Starting from the bottom, the MOSFET provides the highest capacitance per area at the cost of nonlinearity, a process parameter dependent $C$ and a small distance to the substrate. Instead of transistors, metal layers can be used in different shapes to realize horizontal or lateral structures [2]. Their capacitance is limited by the minimum distance between the layers given by the design rules of the corresponding process




(a) Cross section of the on-chip capacitor: A vertically oriented comb-structure is stacked over an n-capacitor (NMOS embedded in an n-well).



(b) 3D model of the pumping capacitor: The positive electrode is completely enclosed by the negative electrode. Therefore, a parasitic top-plate capacitance has no influence.




(c) Simulated and measured capacitance of the proposed pumping capacitor at different DC-voltage levels. The plot shows the voltage dependency of the MOS capacitor.

(d) Simulated and measured proportionality factor of the parasitic top- and bottom plate capacitances. Due to the encapsulated design the former is close to zero while the latter is typically lower than 14 %.

Figure 4.3: Cross section, 3D model and characterization of the on-chip capacitor.

technology. With each layer the distance to substrate increases and therefore the effect of the parasitic capacitance loses influence. The accuracy is typically higher compared to the MOS capacitor due to better controllability of processing metal layers.

Due to small distances, on-chip capacitors suffer from parasitic capacitances from both terminals to substrate which have a huge impact on the performance of a charge pump. The capacitance can be increased by scaling but with it the parasitics grow proportionally. Therefore a well performing on-chip capacitor for charge pumps needs to provide a high capacitance per area and low parasitics to substrate, this is particularly important for the top-plate that directly

influences the voltage gain as discovered in Chapter 3.3.

In order to combine a volumetric capacity with low parasitic top-plate capacitance a new architecture is designed which completely encapsulates the top-plate with the bottom plate of the on-chip capacitor. The corresponding 3D-model is shown in Figure 4.3b with the positive (top-plate) electrode in red and the negative (bottom-plate) colored in green. It consists of a dual-gate MOS capacitor that is composed of an NMOS transistor located in an N-well to reduce the depletion region at low voltages. Compared to the standard NMOS, the dual gate device provides reduced gate capacitance but is more resistive to high voltages and less affected by gate leakage currents. The well and the drain/source contacts are part of the negative electrode and represent the lower boundary of the structure while the gate belongs to the positive terminal. On top of the transistor gate the fringe capacitance of a vertically oriented comb-structure with alternating electrodes at minimum distances is used. The vertical structure is given preference as the process technology that is used allows lower lateral distances compared to vertical ones. The fringe capacitor is encapsulated by a "wall" which is connected to the negative electrode. For a better understanding, the cross-section of the proposed architecture is depicted in Figure 4.3a.

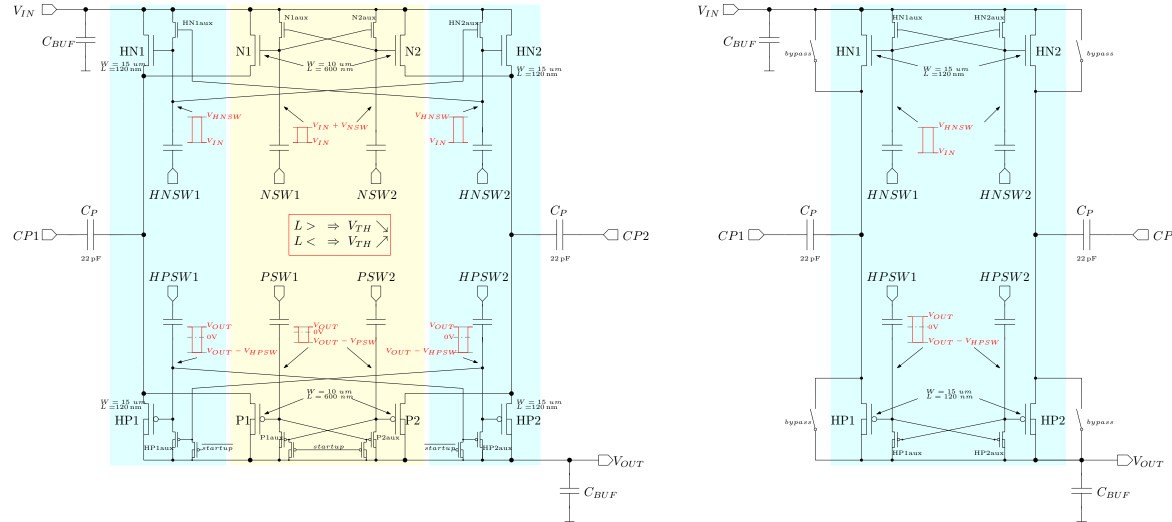
The on-chip capacitor requires a layout area of 60 µm x 68 µm and provides a capacitance of 20 to 25 pF which corresponds to 6.12 fF/µm$^2$. The values are obtained by simulation of the extracted model of the structure and measurements. In comparison, the extracted model shows some inaccuracy compared to the measurement results. As shown in Figure 4.3c the contribution of the MOS capacitance leads to a voltage dependency which reduces the effective $C$ by 20 % at low voltages.

In addition, the parasitic parameters are investigated by simulation and measurements which are illustrated in Figure 4.3d. As expected, the parasitic top-plate capacitance has no influence due to the encapsulation of the corresponding electrode. Therefore the voltage gain factor of an idealized charge pump is feasible. The parasitic bottom-plate capacitance is in the order of 10 to 15 % of the pump capacitor, leading to a lower efficiency of the circuit.

## 4.4 Charge Pump Stage

In this chapter the pump stages architecture is presented. Based on the investigations in Chapter 3.2, a cross-coupled latch charge pump stage using capacitively injected control signals is developed. It extends the Nakagome approach [51] by an auxiliary charge pump and bootstrapped switches. Due to the capacitively coupled control signals, the bottom voltage level of each switch is aligned to the corresponding DC-potential of the stage, while the switches overdrive is defined by the amplitude of the control signals.

As driving the switches from the voltage level of the harvesting circuits input node is not sufficient in the ultra-low voltage domain, the clock signals are typically derived from the output side. Nevertheless, at least for start-up, operation from the input node is mandatory in order to pre-charge the output capacitor to a certain voltage level. This leads to two operational modes with different requirements on the pump stage. During the start-up operation, the voltage level




(a) Hybrid stage type 1 contains a current path for the start-up mode and one for regular operation. $C_P$ is used in both cases.

(b) Stage type 2 is bypassed during the start-up mode and becomes functional in regular operation.

Figure 4.4: Cross-coupled latch charge pump stage using capacitively coupled control signals.

of the control signals is in the sub-threshold region leading to a weak driver strength. In order to transfer charge under such conditions at a reasonable frequency, the threshold voltage of the transistors needs to be reduced by increasing the gate-length of the sub-$V_{TH}$ switches. This is counterproductive in the regular operation mode where the power is taken from the output node in order to achieve a large gate overdrive and operate the circuit at a high frequency. In this case the gate-length should be minimized to reduce the on-resistance as well as the gate capacitance of the switches to lower the control effort load current. A detailed investigation of the architecture of the two types is provided in the following subsections.

### 4.4.1 Type 1

The hybrid charge pump stage type 1 is shown in Figure 4.4a. It combines two latch charge pumps with auxiliary voltage doublers controlled at a phase shift of 180° to realize unidirectional charge flow. Each of the cross-coupled switches is implemented twice in order to align its characteristics to the current operational mode. During the start-up (*yellow background*), the control signals are provided to $NSW1$, $NSW2$, $PSW1$ and $PSW2$, driving the transistor pairs $N1$ and $N2$ as well es $P1$ and $P2$ across the bootstrapping capacitors. The devices with a larger gate-length provide a lower $V_{TH}$ and are therefore more suitable to be driven in the sub-threshold region, powered from the input node of the harvesting circuit. In regular operation mode (*cyan background*) the power switches $HN1$, $HN2$, $HP1$ and $HP2$ take over the charge transfer by using the control signals $HNSW1$, $HNSW2$, $HPSW1$ and $HPSW2$ which are derived from the output node. Due to the large amplitude of the clock signal, minimum gate-length is used to minimize the on-resistance and the gate capacitance. The

pump capacitor $C_P$ typically requires a large layout area and is therefore used in both operation modes.

The function of the auxiliary charge pump is explained based on the cross-coupled NMOS pair ($N1$ and $N2$). The clock signals $NSW1$ and $NSW2$ are non-overlapping. Assuming a high-state at the former and a low-state at the latter results in a gate voltage at transistor $N1$ of $V_{G,N1} = V_{IN} + V_{NSW1}$. It therefore enables charge transfer to the stages pump capacitor. The same voltage level occurs at the gate of auxiliary transistor $N2aux$ and interconnects the gate of $N2$ with the input node of the stage. Power switch $N2$ and the auxiliary transistor $N1aux$ are in an off-state preventing backwards conduction to the input. As the node $V_{G,N1}$ is unloaded, except for a small leakage current caused by $N2aux$, it remains nearly constant for the entire clock period. Changing to the opposite state is done in two steps. Firstly, the clock signal $NSW1$ drops to a low-state turning off all switches. Afterwards, $V_{NSW2}$ rises and with it the gate voltage of $N2$ to $V_{G,N2} = V_{IN} + V_{NSW2}$. Now, the power switch $N2$ conducts and $N1aux$ aligns the gate potential of $N1$ to $V_{IN}$.

A similar behavior using inverted clock signals is used for the cross-coupled PMOS switches. In that case the clock signals $PSW1$ and $PSW2$ overlap and gate voltage of $P1$ and $P2$ is aligned to $V_{OUT}$. The clock signal turns on the power switches alternately by pull-down their gate potential to $V_{G,P1,2} = V_{OUT} - V_{PSW1,2}$ which may reach voltage levels below $V_{SS}$.

### 4.4.2 Type 2

The type 2 charge pump stage, shown in Figure 4.4b, is of similar architecture compared to type 1 but waives the start-up switches. During that phase the switches are bypassed by transmission gates and connect the pump capacitors directly to the output node. Therefore the pump capacitors of stages 6-21 are temporarily connected in parallel to the internal buffer capacitor, which is an important aspect for the preparation of the regular operation mode. In general, the inner node voltages of a charge pump require several clock cycles to ramp-up until a current is delivered to the output capacitor. Applied to self-sustaining charge pumps, the regular operation mode would put a load on the output but does not deliver charge to the output node in the beginning. This behavior causes a voltage drop at the output which might be sufficient to fall back in the start-up mode and interrupt the procedure. By pre-charging, the pump stages are able to immediately deliver a current when switching to the regular operation mode. The clock signals are derived from the output node which enables a large overdrive voltage at the switches and significantly reduces the charge transfer time between the stages. As a result the frequency may be increased to the MHz region.

## 4.5 Clock Signal Generation

In the previous chapter, the system architecture of the pump stage was introduced. In order to charge the output capacitor, a clock signal drives the switches accordingly is necessary. The start-up voltage of the harvesting circuit is therefore limited by the minimum operation voltage of the oscillator. A simple and frequently used approach to generate a clock is a ring oscillator

as it is self-starting and does not require any voltage or current references which makes it suitable for low-voltage operation. The oscillator clocks a digital logic circuit to generate a proper control sequence to guarantee unidirectional charge flow. Its gate delay needs to be sufficient to allow the signal to run through the logic cells before it initializes the next state. In the current design two clock generators are implemented. A free-running start-up clock generator using gates of the ultra-low voltage digital cell library powered from the input voltage level of the harvesting circuit. Instead of an extra ring oscillator, the signal generator contains an inner feedback loop that uses a state controller to monitor the pass-through time of the gates and adapt the frequency accordingly. Additionally, clock doublers increase the voltage level of the sub-$V_{TH}$ control signal used to drive the switches. The start-up clock generator pre-charges the output capacitor to a certain voltage level that enables the ramp-up/regular mode clock generator.

Considering the control sequence of a cross-coupled latch charge pump, the two current paths are driven at a phase shift of 180°. As a result one pump capacitor is always in the charging phase while the second delivers charge to the subsequent stage. In order to prevent backward conduction, a break-before-make approach is used to drive the switches. That is, in between two transfer states all switches involved are temporarily turned off. Additionally, the voltage level of the pump capacitors bottom plate is raised to its final value before switching on the PMOS transistors in the charge delivering phase. The switching states of a complete control sequence is illustrated in Figure 4.5.

### 4.5.1 Free-Running Start-up Clock Generator

The schematic of the free-running start-up clock generator is shown in Figure 4.6. As already mentioned, ultra-low voltage digital logic cells are used to be functional at a supply voltage in the order of 100 mV. In operation, the initial state is defined by the state controller and the signal runs through the combinational logic cells by changing the states of the switches until it reaches the control signals of the PMOS transistors. At this point in time the charge transfer takes place. The feedback loop is closed by a delay element, implemented to guarantee complete charge transfer, until the state controller inverts its output signal and reinitializes a new iteration. The delay time of the element depends on the supply voltage and therefore correlates with the charge transfer time of the pump stage. In the figure, the signal path through the gates is illustrated in *red* for phase A ($STATE = 1$) and *blue* for phase B ($STATE = 0$). The corresponding simulation result for a supply voltage of $V_{DD}$ =100 mV is depicted in Figure 4.7. Signal $V_{STATE}$ represents the output of the state controller. Each of the control signals is boosted by a clock doubler to $\sim 2\ V_{DD}$ which requires a few cycles to become effective. The bottom plate of the pump capacitors is directly connected to $CP1$ and $CP2$ and requires a strong driver to push the charge from stage to stage. A detailed investigation into the voltage doubler and the driver circuit is presented in the following subsequent sections.

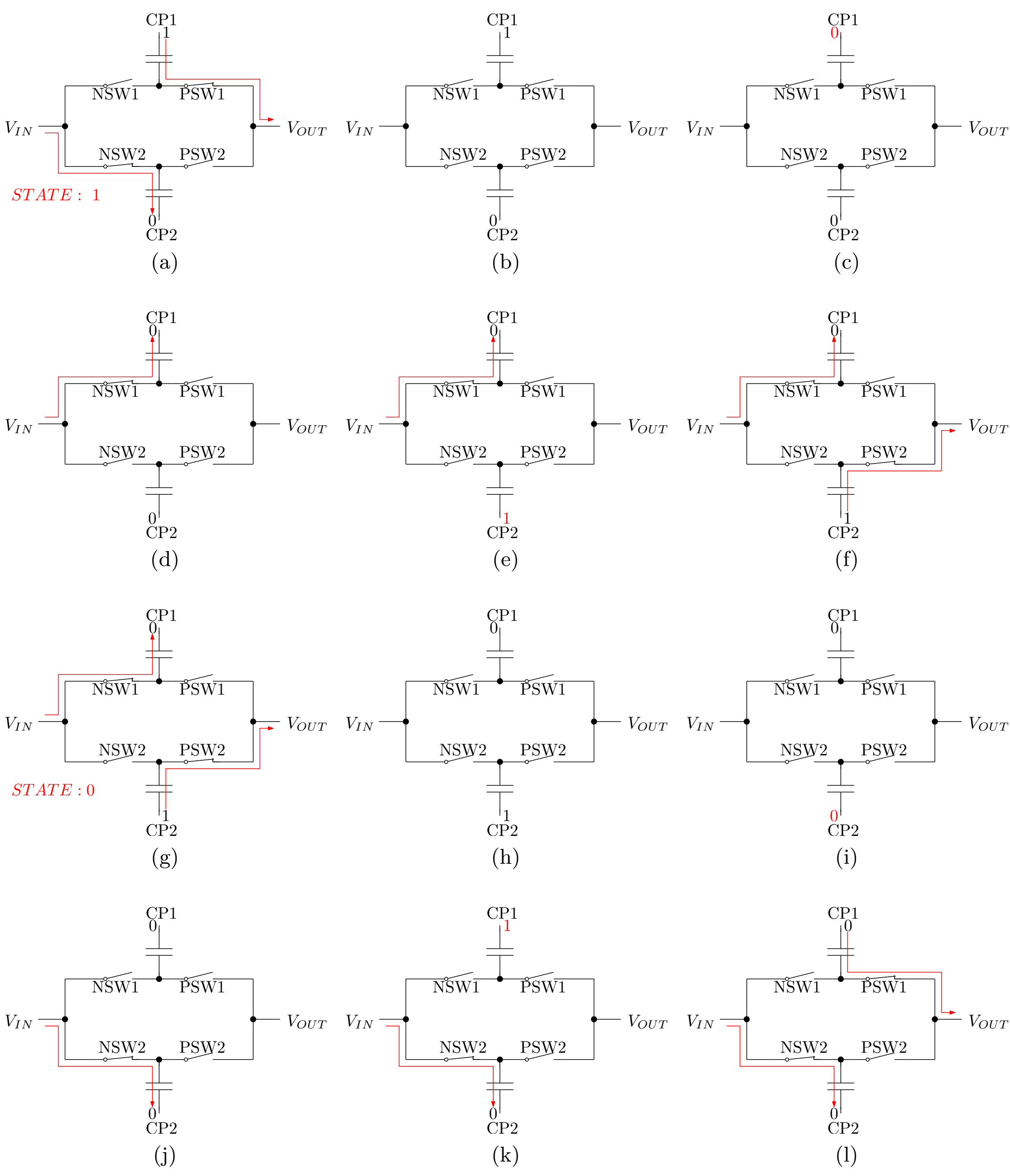



Figure 4.5: Break-before-make control scheme of the cross-coupled charge pump using the signals generated by the LV clock generator in Figure 4.7.

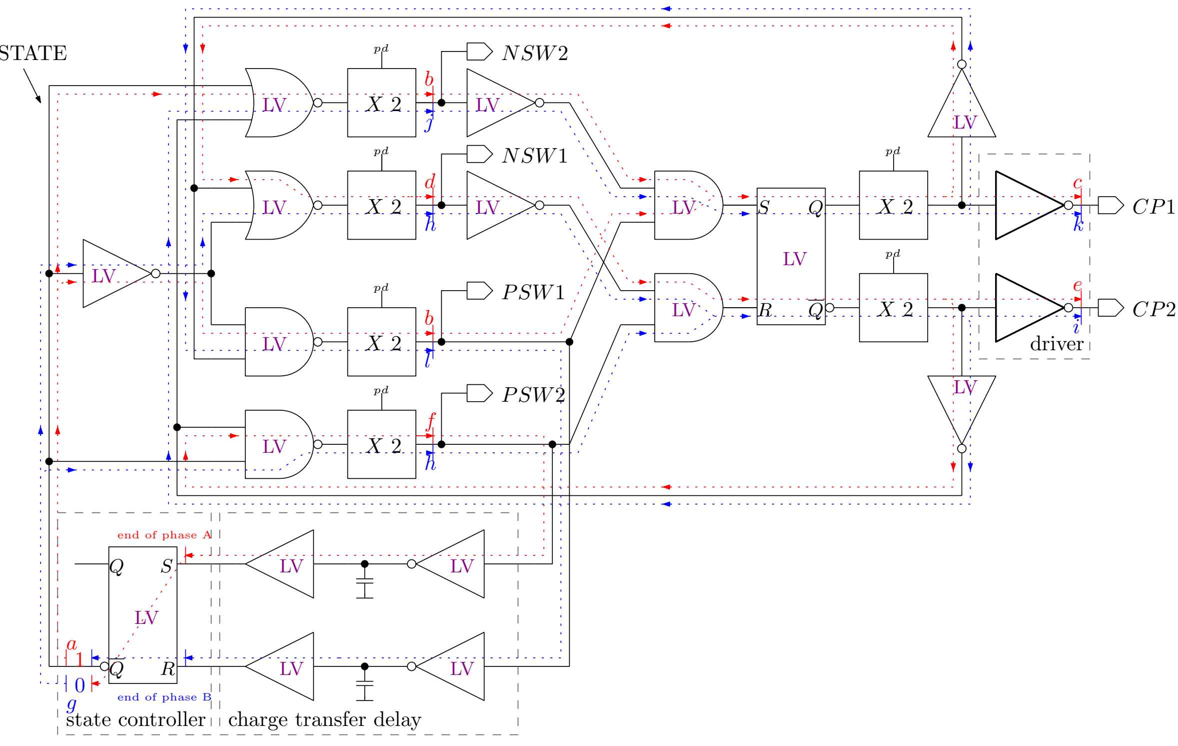



Figure 4.6: Free-running low voltage clock generator using cells from the ultra-low voltage digital cell library.

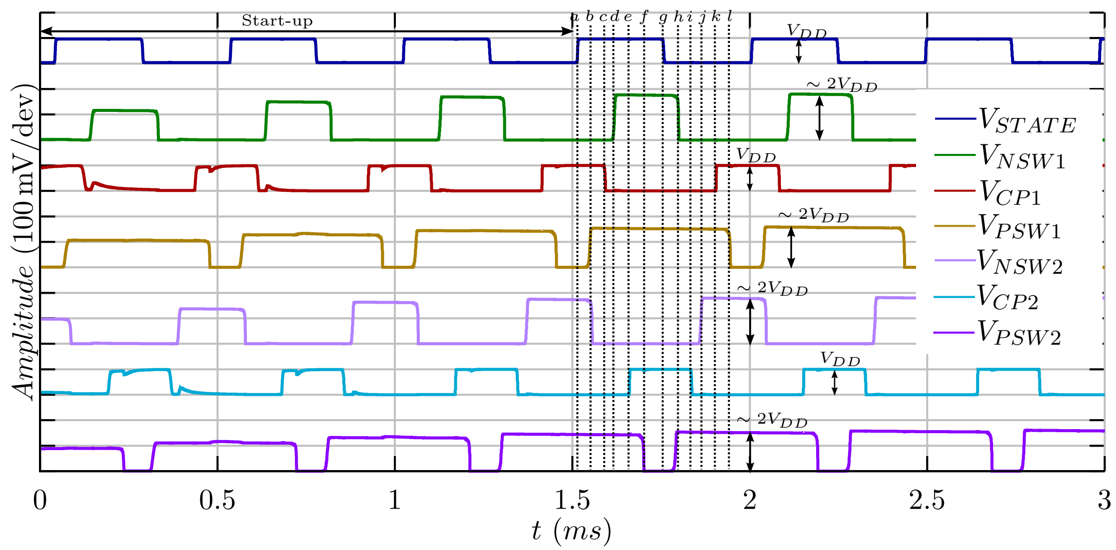



Figure 4.7: Simulated transient behavior of the low voltage clock generator to control the switches at a supply voltage of 100 mV.

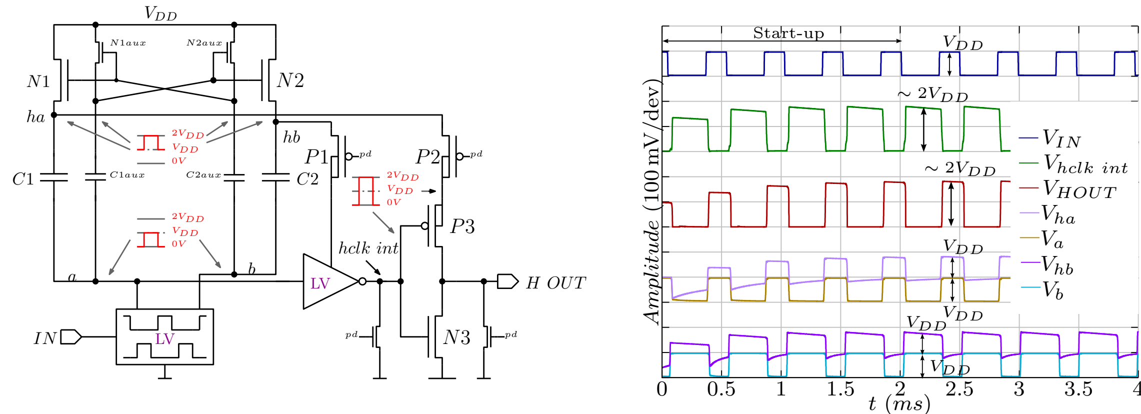
### Voltage Doubler

The pump stage switches are implemented using regular transistors with a threshold voltage 2-3 times higher than the input voltage of the harvesting circuit. While the logic gates of the clock generator are functional under ultra-low voltage conditions, driving the switches at a gate voltage in the order of 100 mV leads to insufficient weak charge transfer behavior. To overcome this limitation, voltage doublers are used in the signal chain to increase the effective gate voltage at the switches. The architecture and simulation results are depicted in Figure 4.8. Referring to Figure 4.8a, a structure similar to the pump stage containing a cross-coupled NMOS pair and an auxiliary voltage doubler is used. The input signal generates a non-overlapping clock at the internal nodes $a$ and $b$ as well as $ha$ and $hb$ across the bootstrapping capacitors. While the former toggles between 0 V and $V_{DD}$ the latter alternates between $V_{DD}$ and 2 $V_{DD}$. The internal nodes $ha$ and $hb$ supply the inverters of the output driver used to double the signal amplitude.

Operation at $V_{DD}$=100 mV is shown in Figure 4.8b. The circuit requires a few start-up clock cycles to provide the boosted voltage levels and become functional. Assuming a rising edge at signal $IN$ leads to a high-state at nodes $a$ and $ha$ as well as a low-state at $b$ and $hb$. The LV-inverter therefore sees $V_{DD}$ at the input and the supply pin and weakly ($V_{GS} = V_{DD}$) pulls-down $hclk\ int$ representing the input of the second inverter gate. As the latter is supplied from $ha$, the PMOS transistor $P3$ is more strongly driven at a gate voltage 2 $V_{DD}$ while $N3$ is in off-state. The output signal ($HOUT$) follows the input with twice the amplitude. The falling edge at the input pin inverts all internal states. Signals $a = V_{SS}$, $ha = V_{DD}$, $b = V_{DD}$ and $hb = 2\ V_{DD}$. The LV-inverter pulls-up $hclk\ int = 2\ V_{DD}$ which turns-off $P3$ and drives $N3$ at a gate voltage of 2 $V_{DD}$. As a result, output $HOUT$ follows to a logic low state. Compared to the LV-inverter, both states of the second stage are controlled at twice the supply voltage which is reasonable for driving large capacitive loads. In power down mode the inverters are disconnected by the PMOS switches $P1$ and $P2$ and the output is pulled-down to $V_{SS}$, independent of the input state.

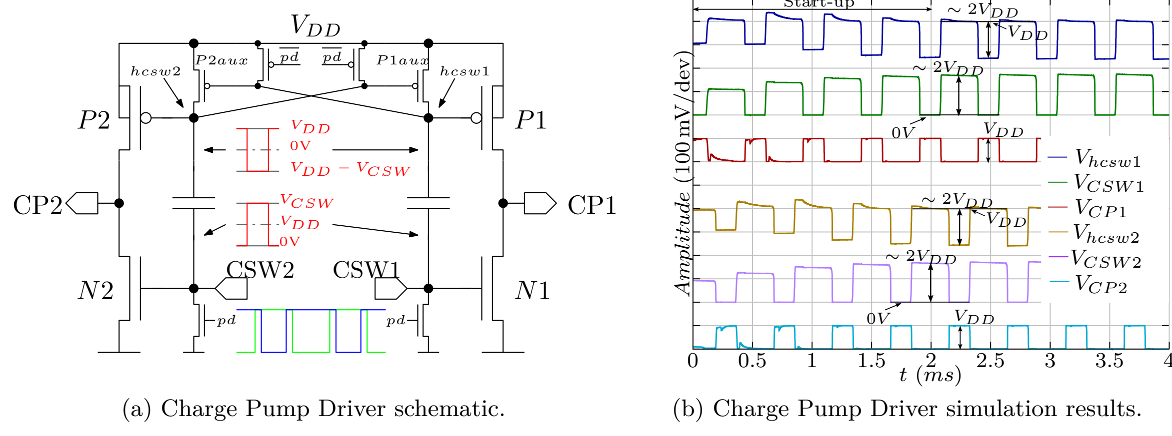
### Charge Pump Driver

In order to transfer charge from stage to stage, the bottom plate of the pump capacitor is pushed to $V_{DD}$ by the charge pump driver circuit. Its output is therefore heavily loaded and requires a certain driver strength. Conventionally, a driver is realized by cascading inverter gates of growing current capability. This approach is not feasible for ultra-low voltage inputs due to the following reason. Considering an inverter, the gate voltage of the NMOS is referred to $V_{SS}$ while the PMOS is related to the supply line (e.g. $V_{DD}$). Applying a boosted clock signal, for example provided from a voltage doubler, turns on the NMOS sufficiently but does not improve the gate overdrive of the PMOS transistor as it would need a negative gate voltage. As a result the PMOS remains weak in driving strength, independent of the signal amplitude provided by the clock. To overcome this issue a negative voltage doubler is implemented by using cross-coupled PMOS transistors capacitively driven at an overlapping clock signal (as shown in Figure 4.9a). Assuming a high-state at $CSW1$ and a low-state at $CSW2$ turns-on




(a) Schematic of the clock doubler circuit.
(b) Simulation results for a supply voltage of 100 mV.

Figure 4.8: Clock doubler schematic and simulation result at a supply voltage of 100 mV to sufficiently drive the charge pump switches in the sub-threshold region for start-up.




(a) Charge Pump Driver schematic.
(b) Charge Pump Driver simulation results.

Figure 4.9: Charge Pump Driver

$N1$. Node $hcsw1$ is connected to $V_{DD}$ by the auxiliary transistor $P1aux$ and $CP1$ drops to ground. As a result $P2aux$ is in off-state and $hcsw2$ remains at $V_{GS,P2} = V_{DD} - V_{CSW}$ due to the unloaded condition. The low-state of $CSW2$ turns off transistor $N2$ and $CP2$ rises to $V_{DD}$. This architecture applies a similar gate overdrive for the NMOS and PMOS transistors of the proposed charge pump driver. In power down mode all output transistors are off leading to a tri-state of the circuit.

### 4.5.2 Ramp-up/Regular Mode Clock Generator

While the main focus of the start-up clock generator is operation at the lowest voltage levels, the regular mode circuit has to offer low power losses in order to achieve high voltage gain and

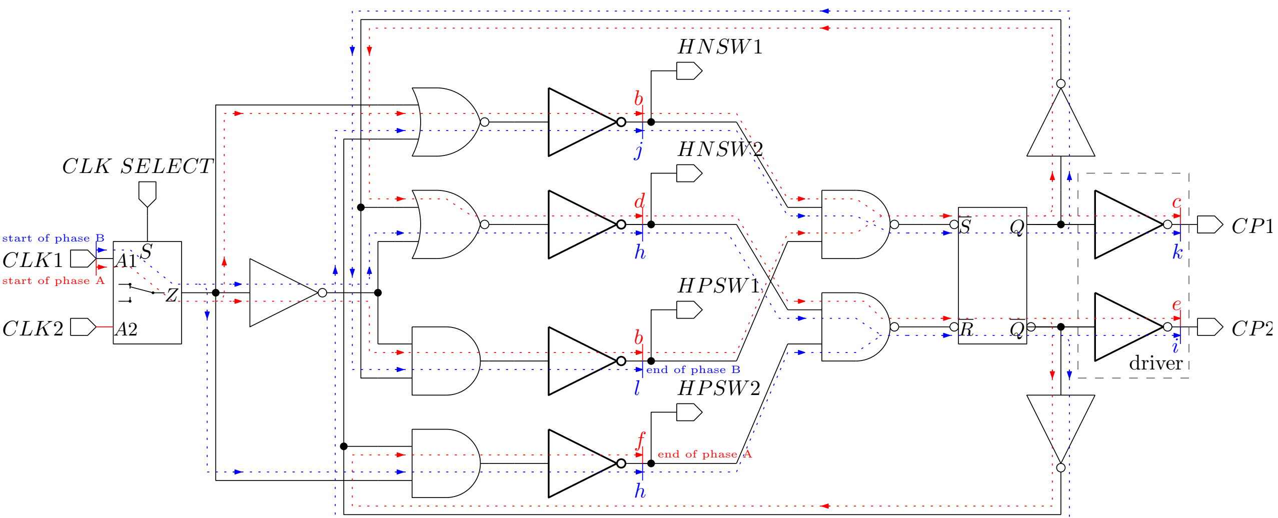



Figure 4.10: Schematic and signal path through the ramp-up/regular mode clock generator based on standard logic cells.

efficiency. The ramp-up/regular mode clock generator is activated when the output capacitors voltage level exceeds the sub-threshold region ($V_H > 350\,\mathrm{mV}$) and reliable operation of standard logic cells is feasible. Its architecture is based on a similar topology to the start-up circuit but uses the logic gates of the standard digital library provided by the Infineon design kit instead of ultra-low voltage gates. The advantage is a smaller gate capacitance due to the optimized layout area and the non-existence of compensation devices. As standard logic cells are not functional in the sub-threshold region they are powered from the output node of the harvesting circuit. An overview of the schematic and the signal path through the design is shown in Figure 4.10. Instead of a feed-back loop, two selectable clock signals provided by different oscillators define the operation frequency. One is used during the ramp-up phase ($350\,\mathrm{mV} < V_H < 700\,\mathrm{mV}$) and is generated by a sub-threshold ring oscillator which will be discussed in Chapter 4.6.1. The second input is connected to a relaxation oscillator providing a well defined clock frequency which is functional in regular operation mode ($V_H > 700\,\mathrm{mV}$). A closer investigation of the circuit is provided in Chapter 4.6.2. Simulation results of the ramp-up/regular mode clock generator at a supply voltage of 500 mV are shown in Figure 4.11. In order to make the gate delays visible a frequency of 5 MHz was chosen in this example. In operation it is typically about 700 kHz. All gates are minimum size except for the drivers of the control signals. The pump capacitor driver is of similar architecture to Figure 4.5.1 but uses smaller device sizes of transistors and capacitors for efficiency reasons.

The regular mode oscillator and the clock generator drive the switches of the pump stages and are therefore the main contributors to the base load current ($I_{CTRL}$) of a self-sustaining charge pump, as previously discussed in Chapter 3. In order to estimate the achievable voltage gain of the harvesting circuit, the control effort factor $\gamma$ needs to be found by investigating the power demand of the control logic. A digital circuit requires a certain amount of charge to change the states of its internal nodes within each clock cycle. Its power demand can therefore be

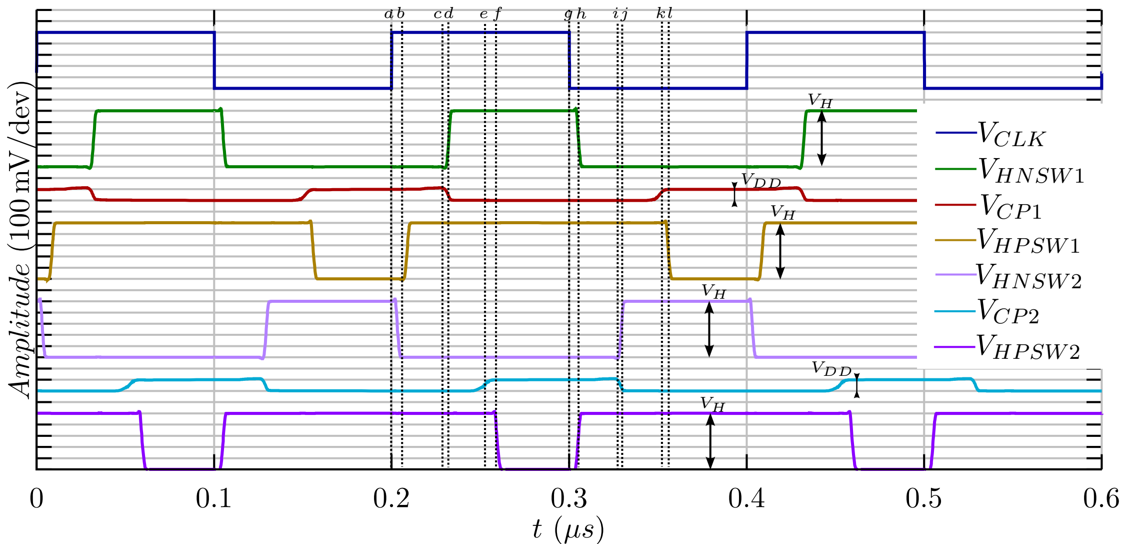



Figure 4.11: Simulated transient behavior of the ramp_up/regular mode clock generator at a supply voltage of 500 mV.

represented by a capacitor having an equivalent capacitance ($C_{eq}$) that has to be repetitively charged and discharged within each clock cycle. The value of $C_{eq}$ can be determined by stand-alone simulation of the parasitic extracted oscillator and clock generator with the control signals connected to the pump stages to monitor the corresponding supply currents at a certain frequency and voltage condition. Using relationship (4.5.1) enables calculation of the equivalent capacitance by rearranging it to (4.5.2). A summary at different supply voltage levels of the medium voltage domain ($V_M$) is presented in Table 4.3. In the table, the purely digital clock generator and the stage show a voltage independent equivalent capacitance while the oscillator's power demand significantly increases for a high voltage level of $V_M$. This is caused by the limited slew rate of the comparator's output signal which extends the transition time required to change the state at higher supply voltages and causes cross-current losses at the latter inverter stage. As the oscillator is typically operated at lower voltages it does not affect the performance of the circuit. It has to be noted that the equivalent capacitance of the oscillator ($C_{eq,Osc}$) and the clock generator ($C_{eq,Clkgen}$) occur only once while the capacitance of the stage ($C_{eq,Stage}$) increases proportionally with the number of stages (4.5.3).

$$Q = C \cdot V = I \cdot T \tag{4.5.1}$$

$$C_{eq} = \frac{I}{f \cdot V_M} \tag{4.5.2}$$

$$I_{CTRL} = f \cdot V_M \cdot (C_{eq,Osc} + C_{eq,Clkgen} + N \cdot C_{eq,Stg}) \tag{4.5.3}$$

| $V_M$ | 600 mV | 800 mV | 1 V | 1.2 V |
|---|---|---|---|---|
| $C_{eq,Osc}$ | 551 fF | 440 fF | 725 fF | 1.62 pF |
| $C_{eq,Clkgen}$ | 850 fF | 880 fF | 904 fF | 928 fF |
| $C_{eq,Stage}$ | 126 fF | 124 fF | 124 fF | 122 fF |
| $\sum C_{eq@N=21}$ | 4.05 pF | 3.91 pF | 4.23 pF | 5.12 pF |
| $\gamma$ | **0.0022** | **0.0028** | **0.0038** | **0.0055** |
| $G0_{max}$ | **11.2** | **9.8** | **8.2** | **6.4** |

Table 4.3: Simulated equivalent load capacitance of the oscillator, clock generator and pump stage switches to estimate the control effort factor. The parasitic extracted circuit is used.

$$\gamma = \frac{V_M}{V_H} \cdot \left( \frac{C_{eq,Osc} + C_{eq,Clkgen}}{N \cdot C_P} + \frac{C_{eq,Stg}}{C_P} \right) \tag{4.5.4}$$

The general expression of the base load current ($I_{CTRL}$) of a self-sustaining charge pump expressed by the control effort factor $\gamma$ is given by (3.4.3) and was earlier defined in Chapter 3.4.1. Equating (3.4.3) and (4.5.3) results in (4.5.4) which shows a dependency of $\gamma$ on the supply voltage level of the control logic and its equivalent capacitances. In order to increase the voltage gain, the control effort needs to be decreased which can be achieved by design optimizations (e.g. low number of gates in the control logic, reduced gate capacitance of the switches,...) and reduction of the supply voltage level $V_M$. In Table 4.3, the absolute values of $\gamma$ for different supply voltage levels are shown. Applying these values to characteristic curve Figure 3.5b gives the maximum voltage gain of the unloaded circuit which ís also added to the table. These values represent an idealized gain as some other analog components (e.g. current reference, voltage level detectors,...), that are powered from the output node, are not considered in this calculation. In order to reach a voltage gain of $G_0 = 10$, the medium supply voltage domain should be lower than 800 mV. Nevertheless, as $V_M$ affects the charge transfer time it should not be reduced below 600 mV in order to guarantee complete charge transfer of the pump stages at the operation frequency.

The clock signal generators presented in this chapter provide a control sequence to drive the switches of the charge pump accordingly and prevent losses due to reversed current conduction. In addition, the amplitude of the control signals is defined by a fraction of the output voltage which enables sufficient charge transfer at a reasonable frequency. The clock signal itself is generated locally by a feedback loop in the case of the start-up clock generator but has to be provided by oscillators in the case of the ramp-up and regular mode operation mode. These circuits are discussed in the following chapter.

## 4.6 Oscillators

As already mentioned, two types of oscillators are used to drive the regular mode clock generator. The sub-threshold ring oscillator is activated during the ramp-up phase at an output voltage of between 350 mV and 700 mV. It is completely powered by the input node of the harvesting circuit and is therefore designed to operate at a supply voltage level as low as 100 mV. A local voltage regulator limits its frequency to a few tens of kHz, independent of $V_{TEG}$. When the output voltage exceeds 700 mV the start-up procedure is completed by activating the current reference circuit and the relaxation oscillator. Both circuits take their power from the output node and generate a well defined frequency of 700 kHz for the regular mode operation. In the following sub-sections both architectures are investigated in detail by discussing the architecture and presenting simulation results for the parasitic extracted circuits.

### 4.6.1 Ramp-up Oscillator

The architecture of the ramp-up oscillator is shown in Figure 4.12. Its clock signal is generated by a 5-stage ring oscillator using gates of the ultra-low voltage digital cell library. As the frequency of a ring-oscillator highly depends on the supply voltage, a linear voltage regulator and a local reference voltage ($V_{REF}$) is added to define a certain supply voltage level ($V_{DD,OSC}$) in operation and limits the frequency to a few tens of kHz. It is powered from the input node and therefore requires sub-threshold capabilities.

The circuit generates a local reference voltage by stacking 22 N-type leakage current sources ($N1$) on top of an NMOS-diode ($N2$) of the same geometry. This architecture is similar to the N-type inverter discussed in Chapter 2.2.2, but with a feedback loop created by interconnecting the output to the input. As a result, a PTAT reference voltage independent of process variations is generated. It is self-starting and does not require any external current reference. The provided reference voltage level is defined by expression (4.6.1) and results in $V_{REF} \approx 105\,\text{mV}$ when applying $n = 22$ and assuming $m = 1.3$ in the current design approach. As the reference voltage shows a logarithmic dependency on $n$, a linear growth of $V_{REF}$ requires an exponentially increasing area demand of the leakage current sources. In order to reach a higher nominal value for $V_{DD,OSC}$, a systematic offset is implemented by design of the linear voltage regulator. It consists of a differential pair $N3$ and $N4$ with a current mirror load ($P1$ and $P2$). Transistor $P3$ controls the output current accordingly to reach the desired voltage level at the gate of $N4$ and $N5$. The current mirror ratio ($cmr$) at the differential pair forces a three times higher current through transistor $N4$ compared to $N3$. The systematic offset ($\Delta V$) is therefore provided by the additional gate voltage required at $N4$ to drive the bias current. The corresponding expression is given in (4.6.2) and results in a systematic offset of $\Delta V \approx 40\,\text{mV}$. The supply voltage of the ring oscillator is the sum of both expressions and shown in (4.6.3). Expression $V_{DD,OSC}$ is therefore a process variation independent PTAT voltage of about 145 mV.

$$V_{REF} = mV_t \cdot \ln(n) \tag{4.6.1}$$

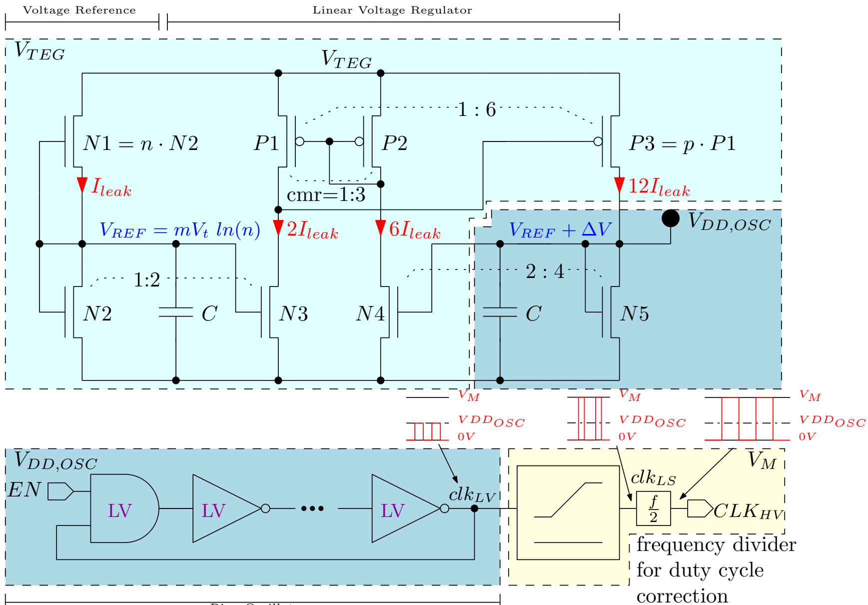



Figure 4.12: Ramp-up oscillator consisting of a local voltage reference, a voltage regulator and a ring oscillator. The circuit is functional in the deep sub-threshold region and is therefore mainly powered from the input of the harvesting circuit.

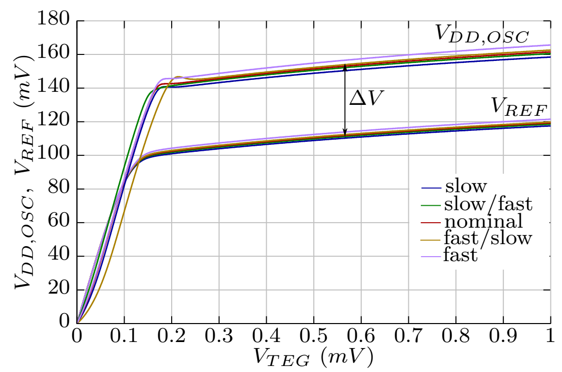
$$\Delta V = mV_t \cdot \ln(cmr) \tag{4.6.2}$$

$$V_{DD,OSC} = mV_t \cdot (\ln(n) + \ln(cmr)) \tag{4.6.3}$$

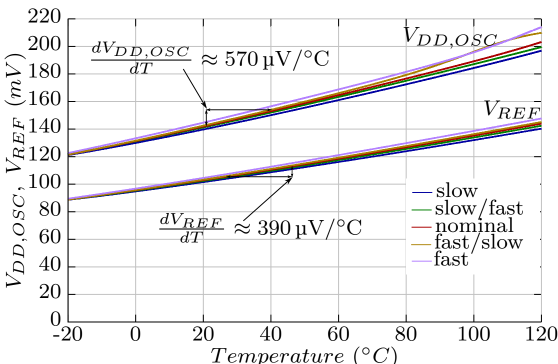
For verification of the reference and the regulator, the input voltage of the harvesting circuit ($V_{TEG}$) is swept and the corresponding voltage of different process corners is shown in Figure 4.13a. Starting from the bottom, both voltages follow $V_{TEG}$ until they reach their nominal values independent of the process corner in good agreement with the calculation. In Figure 4.13b the temperature dependency of $V_{REF}$ and $V_{DD,OSC}$ is depicted. This dependency is acceptable in this application due to the correlation with the maximum frequency of the clock signal generator's logic gates.

The linear voltage regulator supplies the 5-stage ring oscillator at a relatively constant voltage level in order to generate a frequency of several kHz. As the regular mode clock generator is part of the medium supply voltage domain, a level shifter is required to align the amplitude of the clock. During the ramp-up procedure $V_M$ increases from 350 mV to 700 mV which requires a level shifter capable of sub-threshold input signals and high-ratio voltage level adaptation. Its architecture is discussed in the following subsection. A frequency divider implemented with a D flip-flop corrects the duty-cycle to a ratio of 50 %.

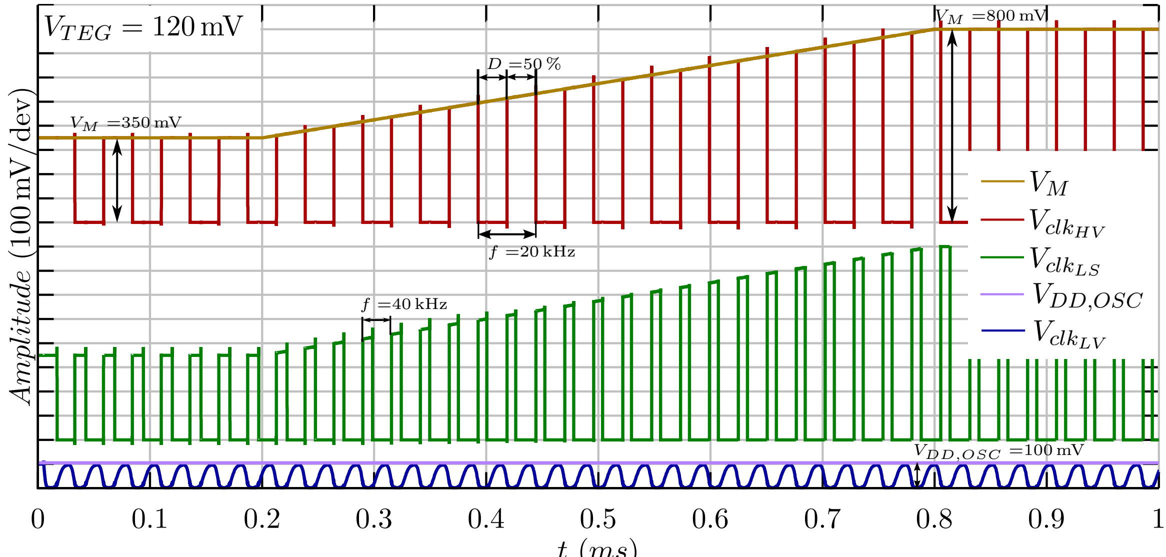
Considering the power demand perspective, the ramp-up oscillator is functional in the deep sub-threshold region and is therefore powered by the input of the harvesting circuit. Only the




(a) Corner simulation of the reference voltage ($V_{REF}$) which is dependent on the input voltage sweep ($V_{TEG}$). By introducing a systematic offset ($\Delta V$) the supply voltage of the oscillator ($V_{DD,OSC}$) is defined.



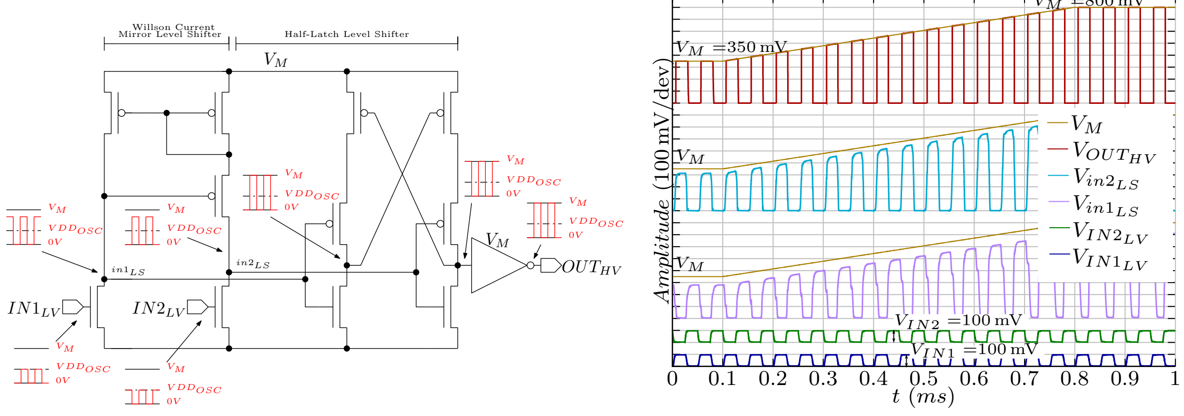

(b) $V_{REF}$ and $V_{DD,OSC}$ have a positive temperature coefficient which is acceptable in this application due to the correlation with the maximum frequency of the clock signal generator's gates.




(c) Transient simulation of the parasitic extracted ramp-up oscillator at an input voltage of $V_{TEG}$ =120 mV. The generated clock signal is level shifted from $V_{DD,OSC}$ to the medium voltage level domain which rises from 350 mV to 800 mV during the start-up procedure.

Figure 4.13: Simulated behavior of the voltage regulator and the ramp-up oscillator operated in the deep sub-threshold region.

level shifter and the latter D flip-flop puts a load on the output node. This constellation helps to maintain a successful ramp-up even at low input voltages.




(a) Schematic of the sub-threshold level shifter.

(b) Simulation of level shifting operation from 100 mV up to 800 mV.

Figure 4.14: Schematic and simulation results of the sub-threshold level shifter in operation during the ramp-up procedure.

### Sub-threshold Level Shifter

The requirements on the level shifter are reliable operation at sub-threshold input voltages in the order of 100 mV and a level shifting ratio between 3 and 8. Its architecture is shown in Figure 4.14a and consists of two stages. The input stage is based on the wilson current mirror approach introduced in [48], transforming the sub-threshold signal close to the potential of the medium supply voltage domain ($V_M$). It is followed by a conventional latch type level shifter to reach the desired output amplitude. As the circuit tends to shift the duty cycle in different process corners, a frequency divider is added for recovering of the clock signal. Simulation results of the sub-threshold level shifter are provided in Figure 4.14b. It shows the internal nodes in operation for a 100 mV signal applied to inputs $IN1_{LV}$ and $IN2_{LV}$ during a complete ramp-up scenario of $V_M$ from 350 mV to 800 mV*. The output signals of the first stage ($V_{in_{LS1}}$ and $V_{in_{LS2}}$) show weak edges and insufficient amplitude. Therefore the second stage is attached to provide a rail-to-rail output signal ($V_{OUT_{HV}}$). The presented interface circuit converts the clock signal of the ring oscillator to the medium supply voltage domain and efficiently clocks the regular mode clock signal generator during the ramp-up procedure.

## 4.6.2 Regular Mode Oscillator

In order to operate the harvester at a well controlled clock frequency in regular mode operation, a low-power relaxation oscillator is started when the output voltage reaches 700 mV. The implemented architecture was introduced by H. Enzinger in [14] and generates a temperature compensated clock frequency of 700 kHz.

* just for demonstration purposes of the level shifter. In general the ramp-up procedure is finished at $V_H$ =700 mV

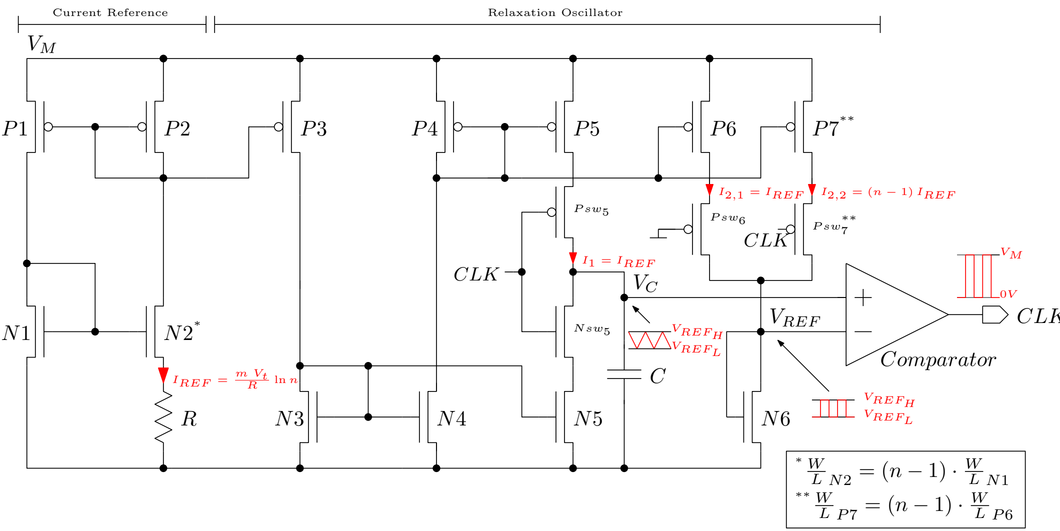
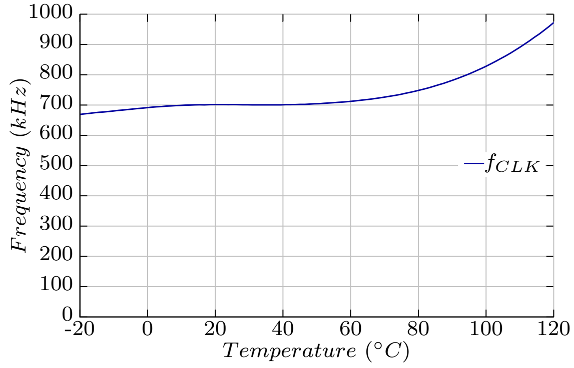
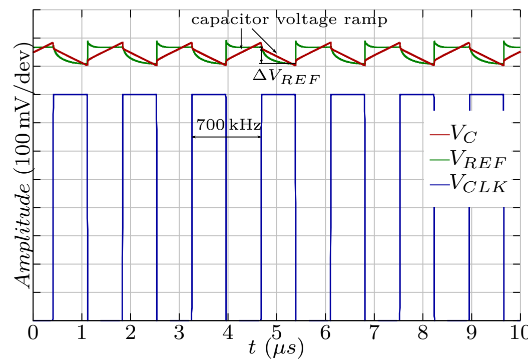



Figure 4.15: Schematic of the regular mode relaxation oscillator containing a local current reference.




(a) Simulated frequency which is dependent on the temperature. The oscillator shows a good compensation behavior in the typical operation temperature range.




(b) The capacitor is repetitively charged and discharged between two threshold voltages. A comparator senses $V_C$ and $V_{REF}$ and controls the state by forming a feedback loop.

Figure 4.16: Simulated behavior of the regular mode oscillator at a supply voltage of 800 mV.

The corresponding schematic is shown in Figure 4.15 and consists of a local current reference and a relaxation oscillator. The former is well known from the literature to generate a reference current ($I_{REF}$) that is positive to absolute temperature (PTAT). When assuming weak inversion operation, $I_{REF}$ is defined by the device count ratio of the bottom current mirror ($N1$ and $N2$), the resistor $R$ and the thermal voltage ($V_t$) as given in (4.6.4). The relaxation oscillator uses the PTAT current to repetitively charge and discharge a capacitor between two adaptive threshold voltages ($V_{REF,L}$ and $V_{REF,H}$). Both reference voltages are derived by applying two different current densities of ratio $1 : n$ to an NMOS diode in weak inversion. While the absolute values of $V_{REF,L}$ and $V_{REF,H}$ depend on process parameters, their difference is given

by expression (4.6.5) which shows a similar dependency on the temperature than the expression of the reference current (4.6.4), when neglecting the influence of the resistor. As proposed in [14], temperature independence is achieved if the relative temperature coefficients of $I_{REF}$ and $\Delta V_{REF}$ are the same (4.6.6).

$$I_{REF} = \frac{mV_t}{R} \cdot \ln(n) \tag{4.6.4}$$

$$\Delta V_{REF} = mV_t \cdot \ln(n) \tag{4.6.5}$$

$$\frac{\partial I_{REF}/\partial T}{I_{REF}} = \frac{\partial \Delta V_{REF}/\partial T}{V_{REF}} = \frac{1}{T} \tag{4.6.6}$$

Simulation results shown in Figure 4.16a confirm the temperature independence of the oscillator up to a temperature of 80 °C, which is a sufficient temperature range for the harvesting circuit. In Figure 4.16b the transient behavior is shown. The capacitor is repetitively charged and discharged between an alternating reference voltage. A comparator senses $V_C$ and $V_{REF}$ and controls the state by forming a feedback loop. The output of the comparator represents the clock signal that is fed to the regular mode clock generator. In the plot $V_C$, $V_{REF}$ and $V_{CLK}$ are shown to oscillate at a frequency of $f_{CLK}$ =700 kHz.

In the last two sections, three different clock generation schemes for start-up, ramp-up and regular operation mode were described. As the respective operation mode is defined by the voltage level of the internal buffer capacitor $V_H$, it has to be monitored in the absence of a stable reference voltage and at restricted power consumption. The architecture of the voltage level detectors will now be discussed.

## 4.7 Voltage Level Detection

In a conventional design approach the voltage level is detected using a comparator and a bandgap reference voltage. These circuits provide a well defined switching threshold but require a certain supply voltage level and power demand which is in general not available during the start- and ramp-up phase of the thermoelectric energy harvester. Therefore alternative low-power topologies to detect the voltage level at the output of the pump stages are presented in the following sub-sections.

### 4.7.1 350 mV Detector

The first voltage level to be detected is about $V_H = 350\,\text{mV}$ and denotes the transition from the start-up mode to the ramp-up mode. In its initial state, the internal buffer capacitor at the output of the pumping stages is completely discharged ($V_H = 0\,\text{V}$). When applying a sufficient voltage level in the order of $V_{IN} = 100\,\text{mV}$ at the input, the harvesting circuit is activated in

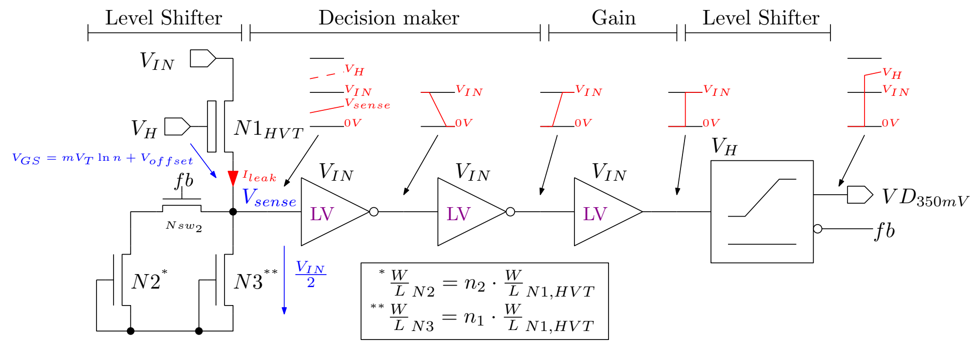
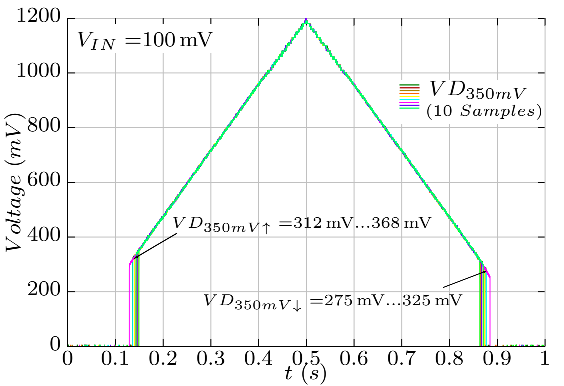
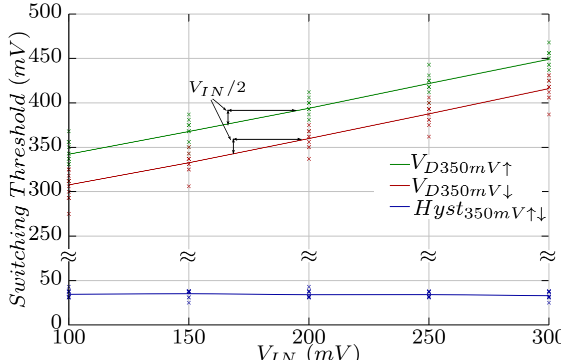



Figure 4.17: Schematic of the 350 mV detector.




(a) Measurement of the switching threshold of the 350 mV level detector. $V_H$ is raised in a triangle shape provided by a waveform generator from 0 V to 1.2 V and back to 0 V in 1 s.




(b) Dependency of the switching threshold on the input voltage ($V_{IN}$). The hysteresis remains constant while the rising and the falling edge increase linearly by $V_{IN}/2$.

Figure 4.18: Measurement of the switching threshold of 10 test samples of the 350 mV level detector.

the start-up mode. That is, the free-running clock generator drives the pump stages at a low frequency resulting in a low output current delivered to the internal buffer capacitor. As the output current in this mode is typically in the nA-range, an important aspect for a successful start-up is to prevent any load on the internal buffer capacitor. This requirement is fulfilled by designing a voltage detector that is powered from the input while sensing the voltage at the output of the pump stages.

The corresponding schematic is shown in Figure 4.17. In order to operate the circuit from the input node, the voltage level of $V_H$ is shifted by the input stage using a source follower. It consists of transistor $N_1$ and the leakage current sources $N_2$ and $N_3$. The latter defines a leakage current ($I_{leak}$) and forces a certain $V_{GS}$ at transistor $N_1$. By calculating the gate source voltage for current equilibrium, $V_{sense}$ is shown to be independent of process variations and follows $V_H$, lowered by $V_{GS} = mV_t \cdot \ln n$, with $n$ representing the device count ratio between the current sources and transistor $N_1$. This is valid when assuming similar device types for all transistors of the source follower. Due to the logarithmic dependency on the ratio $n$, it

is difficult to shift the voltage level by several 100 mV with this topology. Therefore $N_1$ is represented by a thick oxide (HVT) NMOS transistor. These devices are characterized by an increased gate oxide thickness which leads to a higher threshold voltage in comparison to the regular NMOS transistor. As regular and thick oxide NMOS transistors are in principle similar devices, they are similarly affected by process induced errors. As a result the threshold voltage of both transistors shift by nearly the same absolute value in different process corners and their difference remains constant. In a simplified view, transistor $N1_{HVT}$ can therefore be seen as a regular transistor having a threshold voltage that is increased by a process variation independent offset voltage $V_{offset} \approx 220\,\text{mV}$ (4.7.1). The effective gate source voltage of the source follower using a thick oxide NMOS transistor is calculated in (4.7.2).

$$V_{TH,NHVT} = V_{TH,NREG} + V_{offset} \tag{4.7.1}$$

$$V_{GS,N1_{HVT}} = mV_t \cdot \ln(n) + V_{offset} \tag{4.7.2}$$

The decision maker is implemented by an inverter of the ultra-low voltage digital cell library which is powered from $V_{IN}$. As known from Chapter 2.2.4, the process variation compensation technique enables an accurate switching threshold of $V_{SW} = V_{IN}/2$ for the inverter gate. It is followed by gain buffers to strengthen the switching edge. At the end of the signal chain a sub-threshold level shifter aligns the signal amplitude to the high supply voltage domain. In order to realize a hysteresis, the device count ratio of the source follower is changed by a feedback ($fb$) signal which represents the inverted output signal of the level detector ($VD_{350mV}$).

For $VD_{350mV} = 0\,\text{V}$, both current paths through $N_2$ and $N_3$ are active. The rising edge of $VD_{350mV}$ is therefore defined by (4.7.3). At this point in time the device count ratio is reduced from $n = n_1 + n_2 = 15$ to $n_2 = 5$ and lowers the switching threshold of the falling edge of $VD_{350mV}$ to (4.7.4). The resulting hysteresis can be found by subtracting (4.7.4) from (4.7.3) and is shown in (4.7.5). It is not affected by $V_{IN}$.

$$VD_{350mV\uparrow} = mV_t \cdot \ln(n_1 + n_2) + V_{offset} + \frac{V_{IN}}{2} \tag{4.7.3}$$

$$VD_{350mV\downarrow} = mV_t \cdot \ln(n_2) + V_{offset} + \frac{V_{IN}}{2} \tag{4.7.4}$$

$$Hyst_{350mV\uparrow\downarrow} = mV_t \cdot \ln\left(1 + \frac{n_1}{n_2}\right) \tag{4.7.5}$$

In Figure 4.18a, measurement results based on 10 test samples are presented. The stimulus is provided by a waveform generator using a slow triangle signal with a cycle duration of 1 s. It represents rising and falling voltage levels of $V_H$ at the internal buffer capacitor. As shown in the figure, the rising edge varies from 312 mV to 368 mV and the falling edge from 275 mV

to 325 mV which is of sufficient accuracy for this purpose. The measurement procedure is repeated for different input voltages ranging from 100 mV to 300 mV with the corresponding result shown in Figure 4.18b. As predicted by the equations, the switching thresholds increase linearly with the input voltage while the hysteresis remains constant at a value of 35 mV on average.

Considering the power demand of the voltage detector, there is no static current to be taken from the monitored node as it is connected to a gate, while the power consuming source follower, decision maker and gain stages are powered directly from $V_{IN}$. It is only the level shifter that consumes a small amount of power during the switching operation. The proposed circuit allows voltage detection in the sub-threshold region without putting a load on the buffer capacitor and therefore enables the harvester to pull itself out of the deep sub-threshold region during the start-up procedure.

### 4.7.2 700 mV and 850 mV Detector

The transition from the ramp-up mode to the regular mode is indicated by another low-power voltage level detector topology. It is implemented twice and generates an enable signal at the voltage levels $V_H = 700\,\text{mV}$ and $V_H = 850\,\text{mV}$. The former activates the regular mode oscillator and the latter the charging controller, transferring charge from the internal to the external buffer capacitor. In comparison to the previously presented solution it is directly connected to the internal buffer capacitor and uses a locally generated reference voltage to define the switching threshold. In addition, the proposed topology provides temperature compensation capability for detection of the voltage level $V_H = 850\,\text{mV}$.

The corresponding schematic is shown in Figure 4.19. As already mentioned, the circuit is connected to the internal buffer capacitor through the power-down switch $P_{sw_1}$ which is controlled by the 350 mV voltage level detector. During the critical start-up mode, it is therefore disconnected from the source to avoid power consumption. In this phase, the output signals $VD_{700mV}$ and $VD_{850mV}$ are forced to a low-state by $N_{sw_1}$. The first stage of the voltage detector consists of three diode-connected PMOS transistors forming a voltage divider, operated in weak-inversion, stacked on top of a PNP transistor. The base-emitter voltage ($V_{BE}$) is known from the literature to depend mainly on physical constants and temperature conditions. It is therefore only marginally affected by process parameters and increases logarithmically with the current through the device. At a given temperature it can be assumed to provide a constant voltage drop. Due to the low current in the nA-range a base-emitter voltage of $V_{BE} \approx 540\,\text{mV}$ is determined by simulation. Using this simplified approach leads to a voltage drop at transistor $P_1$ given by expression (4.7.6) which represents the input voltage of the second stage ($V_{sense} = V_{GS_{P_4,P_7}}$). Transistors $P_4$ and $P_7$ are loaded by the leakage current sink $P_6$. When neglecting the cascode transistors $P_5$ and $P_8$, this structure is already known from Chapter 2.2.3 to be a P-type inverter gate. The switching threshold of the P-type inverter only depends on the temperature and the device count ratio and was originally derived in (2.2.9). Using (4.7.6) as input voltage of (2.2.9) gives the switching threshold of the voltage level detector shown in (4.7.7). It depends on the sum of two terms. The absolute value of $V_{SW}$ is process independent and defined by the device count ratio between the active devices and

the leakage current sink. The rising edge of $V_{sw}$ is detected by a current-starved inverter using a positive feedback loop for slew-rate enhancement to increase the gain of the decision stage [66].

$$V_{sense} = \frac{V_H - V_{BE}}{3} \tag{4.7.6}$$

$$V_{sw} = 3mV_t \cdot \ln(p) + V_{BE} \tag{4.7.7}$$

Considering the temperature behavior, $V_{BE}$ is well known to be complementary to absolute temperature (CTAT). Its temperature coefficient is determined by simulation to be about $-1.3\,\mathrm{mV/K}$. The switching threshold of a P-type inverter, on the other hand, shows PTAT behavior with a temperature coefficient depending on the device count ratio $p$. At a certain $p$, both temperature coefficients compensate each other, leading to a temperature independent switching threshold at $V_H = 850\,\mathrm{mV}$.

$$VD_{700,850mV\uparrow} = 3mV_t \cdot \ln(p_1) + V_{BE} \tag{4.7.8}$$

$$VD_{700,850mV\downarrow} = 3mV_t \cdot \ln(p_1||p_2) + V_{BE} \tag{4.7.9}$$

$$Hyst_{700,850mV\uparrow\downarrow} = 3mV_t \cdot \ln\left(1 + \frac{p_1}{p_2}\right) \tag{4.7.10}$$

To realize a hysteresis the device count ratio is adjusted by a feedback signal $fb$. In the initial state the device count ratio $p_1$ is given by $P_6$ to $P_4$ while the current path through $P_7$ is disabled. The corresponding switching threshold is therefore given by (4.7.8). With the rising edge of $VD_{700,850mV}$, transistor $P_7$ is connected in parallel to $P_4$. The device count ratio changes to $p_1||p_2$. In this implementation $p_1 = p_2$. As a result the current ratio is halved leading to a reduced switching threshold for the falling edge (4.7.9). The 850 mV voltage level detector is designed with a device count ratio of $p_{1,850mV} = 25$ while the 700 mV uses $p_{1,700mV} = 6$. Calculating the difference of (4.7.8) and (4.7.9) leads to the hysteresis as shown in expression (4.7.10).

In Figure 4.20, measurement results from both voltage level detectors based on 10 test samples are presented. The stimulus is provided by a waveform generator using a slow triangle signal with a cycle duration of 1 s. It represents rising and falling voltage levels of $V_H$ at the internal buffer capacitor. As shown in figure 4.20a, the rising edge of the 700 mV voltage level detector varies from 675 mV to 732 mV and the falling edge from 618 mV to 648 mV with a corresponding hysteresis of ≈60 mV. In Figure 4.20b, the measurement is repeated across the temperature range starting from −20 °C to 120 °C. The switching threshold of the voltage level detector shows a negative temperature coefficient in the order of −500 µV/°C on average for the rising edge and −800 µV/°C for the falling edge when considering the typical operation temperature range between 0 °C and 80 °C.

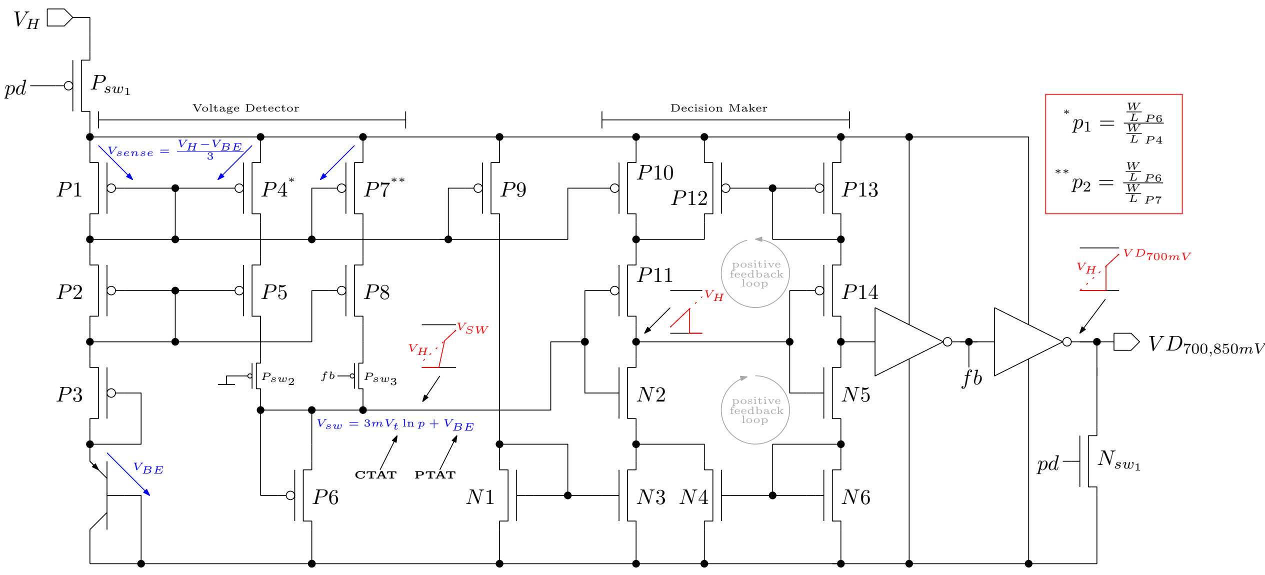


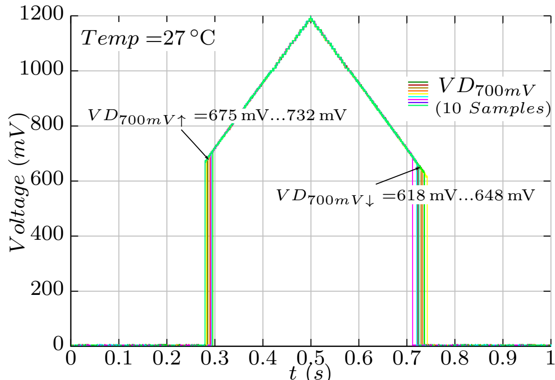

Figure 4.19: Schematic of the 700 mV and 850 mV detector topology. The corresponding switching threshold is set by the device count ratios $p_1 = \frac{W/L_{P6}}{W/L_{P4}}$ and $p_1||p_2 = \frac{W/L_{P6}}{W/L_{P4}+W/L_{P7}}$.

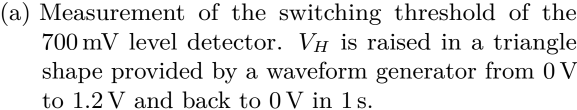
Referring to Figure 4.20c, the same measurement procedure is applied to the 850 mV voltage level detector with the rising edge varying between 806 mV and 887 mV and the falling edge between 737 mV and 818 mV. A hysteresis of ≈70 mV is implemented. The temperature behavior is shown in Figure 4.20d. In simulation, temperature independence is predicted at a switching threshold of 850 mV. As shown in the plot, the circuit is overcompensated leading to the small positive temperature coefficient in the order of 280 µV/°C for the rising edge and 157 µV/°C for the falling edge.

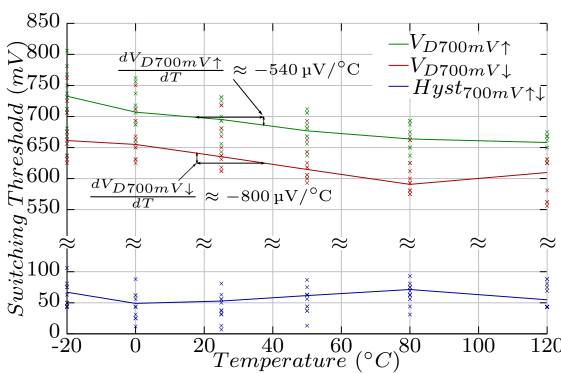
In this chapter, voltage level detectors controlling the states of the start-up procedures are presented. Starting from $V_H = 0$ V to $V_H = 850$ mV different operation modes are active to achieve a successful ramp-up of the thermoelectric harvester circuit. With the rising edge of the 850 mV level detector the charging controller is enabled which transfers charge in a controlled way from the internal buffer capacitor to the external one. It is discussed in detail in the following chapter.

## 4.8 Charging Controller

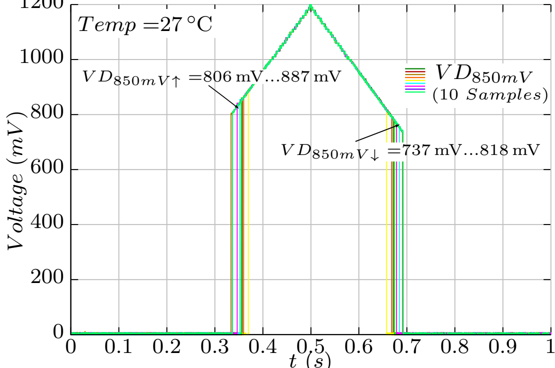
The proposed energy harvesting circuit uses a two-stage charge storage concept at the output node of the pump stages. In order to ensure a successful start-up, the former has to provide a negligible leakage current and is therefore implemented on-chip by using the capacitor architecture discussed in Chapter 4.3. This fully integrated solution avoids leaking ESD-structures typically required when connecting the circuit to external components. The capacitance of the internal buffer capacitor is about 100 pF which is sufficient for providing a stable power supply to the control logic in operation. As the thermoelectric energy harvester is self-sustaining,



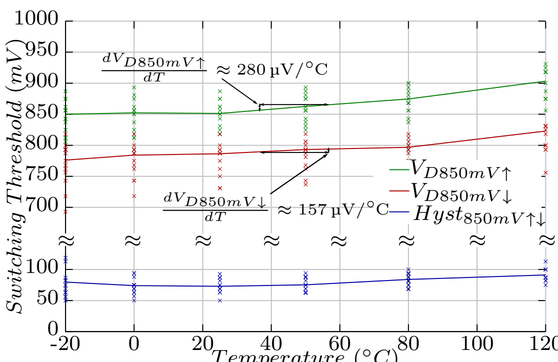


(a) Measurement of the switching threshold of the 700 mV level detector. $V_H$ is raised in a triangle shape provided by a waveform generator from 0 V to 1.2 V and back to 0 V in 1 s.




(b) Measurement of the switching threshold of the 700 mV level detector across the temperature range from −20 °C to 120 °C.




(c) Measurement of the switching threshold of the 850 mV level detector. $V_H$ is raised in a triangle shape provided by a waveform generator from 0 V to 1.2 V and back to 0 V in 1 s.




(d) Measurement of the switching threshold of the 850 mV level detector across the temperature range from −20 °C to 120 °C.

Figure 4.20: Measurement of the switching threshold of 10 test samples of the 700 mV and 850 mV level detector.

the voltage level at the internal buffer capacitor always has to stay above 850 mV to maintain functionality. Considering the subsequent power consuming load (e.g. sensors, transmitter,...), a second energy storage of larger capacitance (µF to mF) is required to allow a complete measurement and transmission cycle of a sensor system. Between the internal and the external buffer capacitor a charge controller is necessary to prevent the latter from completely discharging the former. It operates like a charge overflow by monitoring $V_H$ and transferring just the charge that rises the voltage level at the internal buffer capacitor above a certain voltage threshold.

In Figure 4.21, the architecture of the controller circuit is shown. Charge is transfered from the internal node ($V_H$) to the external node ($V_{BUF\ EXT}$) through transistors $P_5$ and $P_{10}$. While the former operates as a voltage controlled current source, the latter represents a switch to

realize a direct connection between both nodes. It is activated after pre-charging the external buffer capacitor to the voltage level $V_H$ which is monitored by the sense transistor $P_6$. The threshold voltage for activating the current source is defined by a temperature compensated reference voltage ($V_{REF}$). It is generated locally by stacking a bipolar transistor and a PTAT voltage source based on three diode connected PMOS transistors ($P_{2-4}$) and a leakage current source ($P_1$). The temperature compensation mechanism has already been discussed in Chapter 4.7.2 and is therefore not considered in this chapter.

To investigate the functionality of the charge controller an initial state of a completely discharged external buffer capacitor is assumed whilst the voltage $V_H$ rises due to the current delivered by the pump stages. Below the threshold voltage defined by $V_{REF}$, current source $P_1$ is in off-state and the source potentials of transistors $P_2$ to $P_4$ follow $V_H$ directly. As a result $P_5$, $P_6$ and therefore $P_{10}$ are disabled. When the rising voltage at the internal buffer capacitor passes $V_{REF}$, the source potential of $P_2$ remains on a constant voltage level while $P_1$ takes the additional voltage drop and limits the current in the reference branch to $I_{leak}$. As the voltage across the current source also represents the overdrive of $P_5$, a current ($I_{pre-charge}$) starts to transfer excess charge from the internal to the external buffer capacitor. During the pre-charging phase, $V_{BUF\ EXT}$ slowly increases. The sense transistor $P_6$ remains in off-state until the voltage of the external buffer capacitor reaches $V_{REF}$. At this point in time, $V_{sense}$ changes its state and turns-off $P_9$ while the current mirror $N_2$ and $N_4$ pulls-down the gate of $P_{10}$ and establishes a low-ohmic connection between $V_H$ and $V_{BUF\ EXT}$. The voltage level detector connected to $V_{BUF\ EXT}$ initializes a clock stop at 1.2 V which represents the maximum voltage rating of the process technology. The corresponding simulation results are presented in Figure 4.22.

A voltage sweep starting from $V_H = 0\,\text{V}$ to 1.2 V at the internal buffer capacitor is performed in Figure 4.22a to investigate the characteristics of $V_{REF}$ and $V_{BUF\ EXT}$ under consideration of all process corners. As expected, the reference voltage first follows the input and stabilizes at about 850 mV. Therefore no charge transfer occurs between the internal and the external buffer capacitor until $V_H$ reaches a sufficient voltage level. Above, the charge controller establishes a connection between $V_H$ and $V_{BUF\ EXT}$ to align voltage levels at both nodes. Due to the process variation sensitivity of the leakage current source, the voltage drop across the bipolar transistor ($V_{BE}$) in the reference branch and within $V_{REF}$ varies in the range of +/- 40 mV, which is of sufficient accuracy for this purpose.

The dependency of $V_{REF}$ on the temperature is depicted in Figure 4.22b by investigating the behavior across the full temperature range of $-20\,°\text{C}$ to $120\,°\text{C}$ in all process corners. A voltage drift of $<10\,\text{mV}$ is shown for example in the nominal case as an example. In other corners the voltage level is shifted by an offset due to the $V_{BE}$ variation. Nevertheless, the results prove the possibility of generating a stable and relatively accurate reference voltage over a wide temperature range using a very simple architecture requiring no additional circuit overhead (current reference, start-up mechanism,...). The accuracy can be further improved by considering trimming steps.

Finally, the transient simulation of the charging controller in operation is shown in Figure 4.22c using the test bench depicted in the upper-left corner of the figure. A current source represents the pump stages and charges the internal buffer capacitor by delivering a current of 1 µA. Due

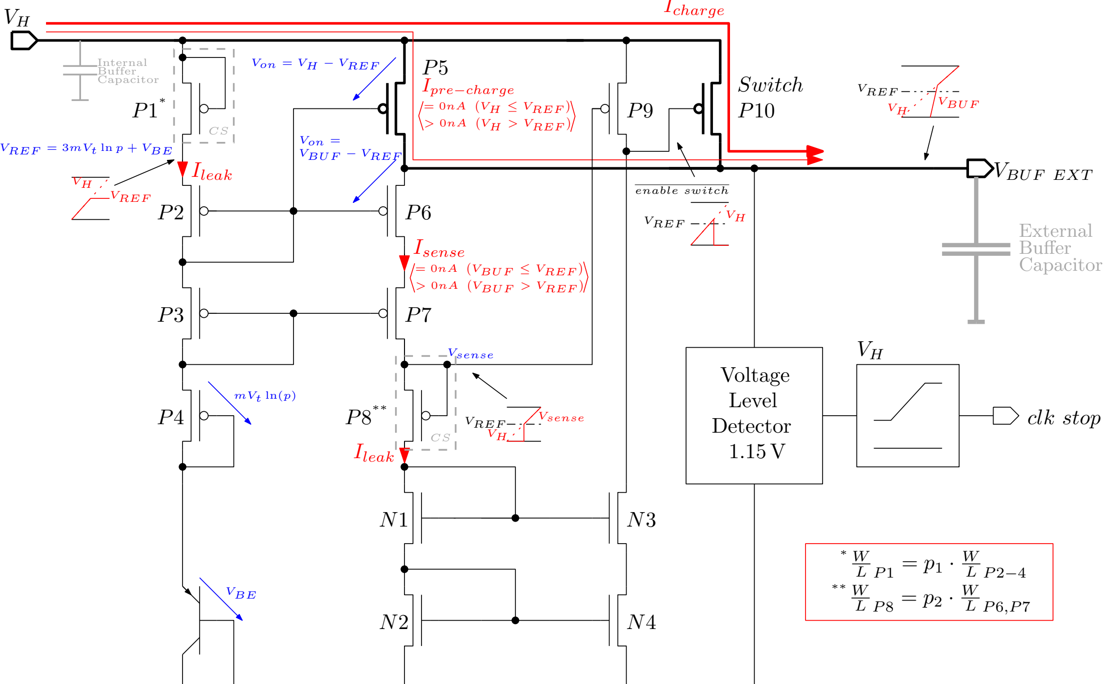


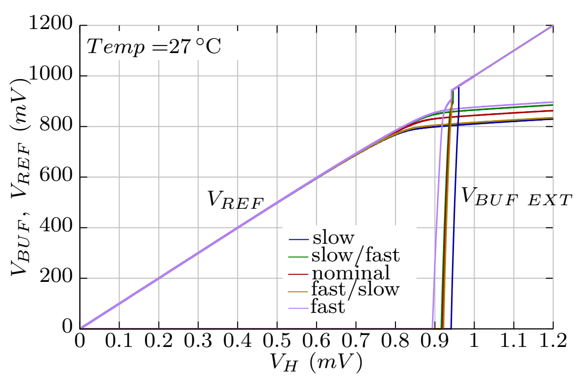

Figure 4.21: Schematic of the charge controller.

to the low capacitance, $V_H$ and $V_{REF}$ rises quickly in the beginning. When $V_H$ reaches 850 mV, the reference voltage settles while $V_H$ further increases to approximately 1 V. The voltage difference represents the overdrive of transistor $P_5$ required to drive $I_{pre-charge}$. In the test bench a 10 nF capacitor is used as an external buffer capacitor. It is slowly charged during the pre-charge phase. At $V_{BUF\ EXT} = 900$ mV the switch $P_{10}$ is closed to establish a low-ohmic connection. Reaching the maximum voltage level is indicated by the clock stop ($clk_{stop}$) signal generated by a voltage level detector that is attached to $V_{BUF\ EXT}$. It interrupts the charging operation in order to protect the circuit from over-voltage.

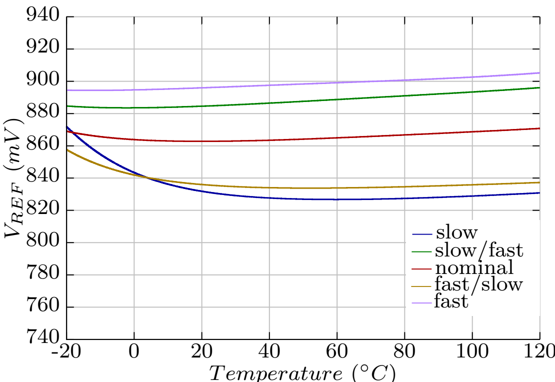
### 4.8.1 Clock Stop Level Detector

The clock stop level detector is based on a similar architecture to the level detectors introduced in Figure 4.7.2 and monitors the voltage level at the external buffer capacitor ($V_{BUF\ EXT}$). Its switching threshold is set by design to 1.2 V and includes a small hysteresis in the order of 50 mV. The output signal disables the oscillator for $V_{BUF_EXT}$ reaching the maximum voltage rating of the used process technology.

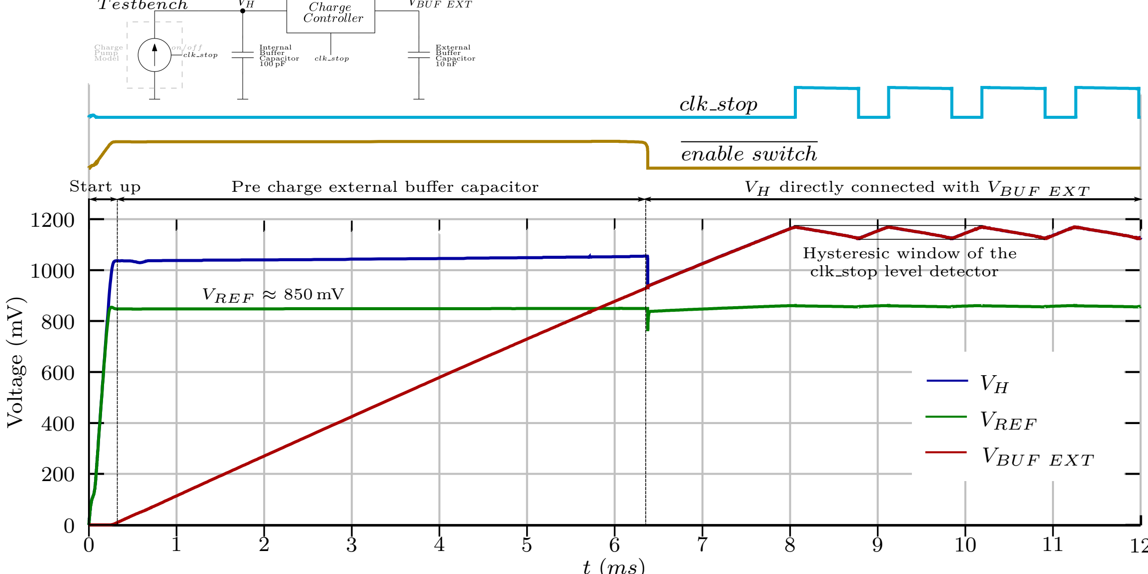
In Figure 4.23, measurement results based on 10 test samples are presented. The stimulus is provided by a waveform generator using a slow triangle signal with a cycle duration of 1 s. It represents rising and falling voltage levels of $V_{BUF_EXT}$ at the external buffer capacitor. As shown in figure 4.23a, the rising edge of the clock stop voltage detector varies from 1.22 V to 1.25 V and the falling edge from 1.2 V to 1.17 V. In Figure 4.23b the measurement is repeated




(a) Corner simulation of the voltage sweep ($V_H$). The reference voltage settles at about 850 mV and activates the charging controller.

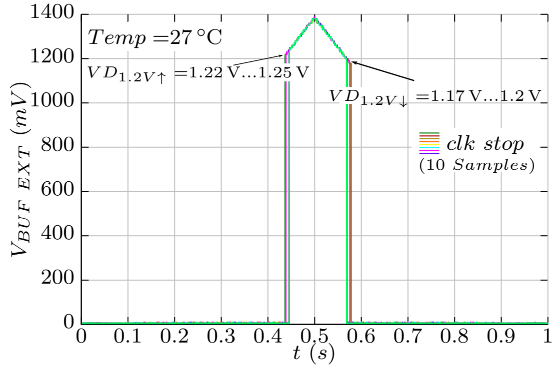



(b) Corner simulation of the local generated reference voltage ($V_{REF}$) across the full temperature range of −20 °C to 120 °C.

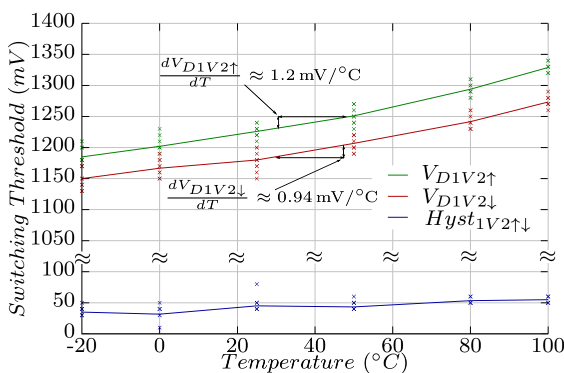



(c) Transient simulation of the charging controller in operation including the corresponding test bench. At sufficient voltage level of node $V_H$, the external buffer capacitor becomes pre_charged until $V_{BUF\ EXT}$ reaches $V_{REF}$. At this point in time the internal and the external capacitors are directly connected by a switch to enable low-ohmic charge transfer. The charge pump is disabled at 1.15 V in order to protect the circuit from over-voltage.

Figure 4.22: Simulation results of the charging controller. Process variations and temperature behavior are considered in addition to the transient behavior.




(a) Measurement of the switching threshold of the clock stop level detector. $V_{BUF\ EXT}$ is raised in a triangle shape provided by a waveform generator from 0 V to 1.5 V and back to 0 V in 1 s.




(b) Measurement of the switching threshold of the clock stop level detector across the temperature range of −20 °C to 100 °C.

Figure 4.23: Measurement of the on-/off switching threshold for 10 test samples of the clock stop level detector.

across the temperature range starting from −20 °C to 100 °C. The switching threshold of the clock stop level detector shows a positive temperature coefficient in the order of 1.2 mV/°C on average for the rising edge and 0.94 mV/°C for the falling edge when considering the typical operation temperature range between 0 °C and 80 °C.

In this chapter a charging controller was presented to coordinate the current flow from the internal to the external energy storage. In addition an over-voltage protection is included, stopping the oscillator at a nominal voltage of 1.2 V. It is realized by a very simple design that does not require any additional reference circuits or start-up mechanism to be functional in all process corners as well as a wide temperature range.

## 4.9 Evaluation and Measurement

After investigating each sub-circuit with detailed measurements, results of the proposed energy harvesting system are presented in this chapter. These are based on 10 test chips manufactured using a 130 nm process technology provided by Infineon.

### 4.9.1 Start-Up and Voltage Gain

In this subsection a DC sweep is performed by changing the input voltage stepwise while monitoring the output voltage and the internal voltage domains $V_H$ and $V_M$. The measurement procedure is performed whilst incrementing the input voltage in Figure 4.24a and decrementing it in Figure 4.24b.

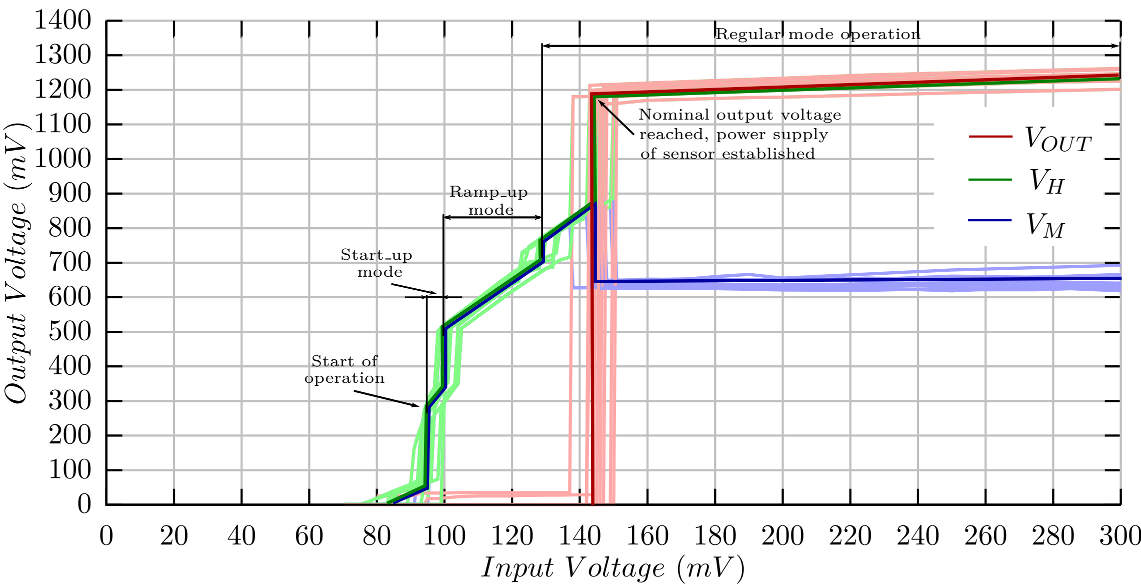
As shown in Figure 4.24a, the circuit is self-starting in the start-up mode at $V_{IN} = 90\,\text{mV}$ and charges the internal voltage nodes to about 300 mV by using 5 pump stages. The output voltage remains at 0 V in this phase as it is disconnected from the internal node until $V_H$ reaches a sufficient voltage level. At $V_{IN} = 100\,\text{mV}$ the 350 mV level detector activates the ramp-up mode which is characterized by changing the number of pump stages to 21 and increasing the clock frequency. As a result the voltage level at $V_H$ and $V_M$ surges to 500 mV and linearly grows with the rising input voltage. The regular mode operation is activated by the 700 mV level detector at about $V_{IN}$ =130 mV. At this point in time, the frequency is further increased to its nominal value of $f$ =700 kHz which raises the internal voltage domains to about 800 mV. The voltage gain is once again rapidly increased at $V_{IN}$ =145 mV by separating the medium from the high voltage domain and connecting the former to an intermediate voltage node of the pump stages which significantly reduces the power demand of the clock signal generator. Due to the sufficient voltage level at $V_H$, the charge controller charges the external buffer capacitor and activates the switch to power the load. In order to limit the output voltage for higher input voltages, the clock stop level detector disables the oscillator at the nominal output voltage of about 1.2 V.

In Figure 4.24b the behavior of the harvesting circuit on a decreasing input voltage is depicted. Starting from $V_{IN} = 300\,\text{mV}$, the output voltage remains steady at its nominal value due to the discontinuous operation by the en- and disabling of the oscillator which occurs until an input voltage of 135 mV is applied. At this point, the circuit provides the nominal voltage at the output node without running it in a duty-cycle mode. For lower values the voltage gain of the harvesting circuit is insufficient which causes a steady decrease in the monitored voltages in the figure. The sensor load is disconnected from the harvester at $V_{IN} = 110\,\text{mV}$ which represents the minimum input voltage for a system which is already started. Nevertheless, the harvesting circuit remains in operation until $V_{IN}$ reaches 90 mV, introducing the shut down of the system.

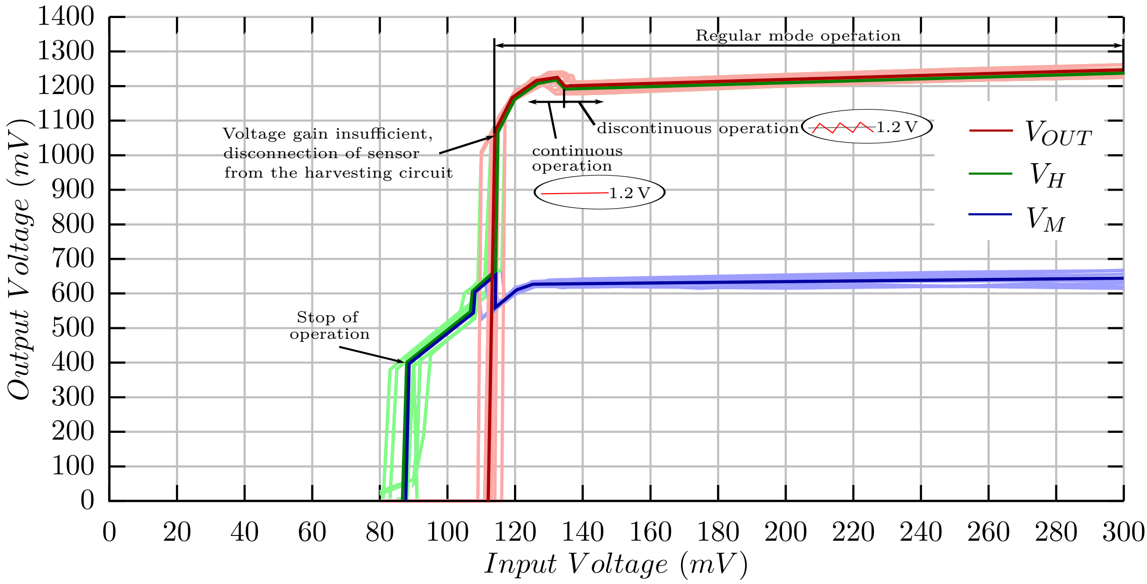
In this subsection the output voltage was measured for an unloaded condition. The circuit starts to operate at about $V_{IN} = 90\,\text{mV}$ and provides a sufficient voltage gain to reach the nominal output voltage at $V_{IN} = 145\,\text{mV}$. Once started, the input voltage may be reduced to $V_{IN} = 110\,\text{mV}$. The influence of a load on the output voltage is the next area to be investigated.

### 4.9.2 Output Current

In this subsection, the output node of the harvesting circuit is loaded at a defined current by connecting a source meter in parallel to the external buffer capacitor. In fact, this does not represent a typical operation scenario as the load is typically disconnected from the charge pump during the harvesting mode. Nevertheless for complex sensor nodes highly capacitive energy storage mechanism (e.g. super-capacitors,...) are used which suffer from a not negligible leakage current. The measurements presented in Figure 4.25 show the current capability of the circuit for several input voltage conditions between $V_{IN} = 130\,\text{mV}$ and $V_{IN} = 300\,\text{mV}$.




(a) Voltage level of the internal high ($V_H$) and medium voltage ($V_M$) domain and the output voltage ($V_{OUT}$) for a stepwise increase of the input voltage.




(b) Voltage level of the internal high ($V_H$) and medium voltage ($V_M$) domain and the output voltage ($V_{OUT}$) for a stepwise decrease of the input voltage.

Figure 4.24: Measurement of the output voltage in dependency of the input voltage based on 10 test samples.

The measurement setup is depicted in Figure 4.25a. As already mentioned, the source meter sinks a defined current at $V_{BUF\ EXT}$ while monitoring the corresponding node. In addition the internal high voltage ($V_H$) domain is monitored through a test pin. At the pin, an analog buffer is used as an interface element to prevent the voltmeter from influencing the internal node. Internally, nodes $V_H$ and $V_{BUF\ EXT}$ are interconnected through the charge controller which limits the current transfer to the external node in order to maintain a sufficient supply voltage level for the control logic.

Referring to Figure 4.25b, for an input voltage of $V_{IN} = 130\,\text{mV}$, $V_H$ and $V_{BUF\ EXT}$ are directly interconnected by the charge controller and remain stable at the nominal voltage level until the output current reaches $I_{OUT} = 200\,\text{nA}$. Higher load conditions successively decrease the voltages at the monitored nodes. The maximum current is limited to $I_{OUT} = 420\,\text{nA}$ by the charge controller that disconnects the load when the internal voltage reaches its lower threshold.

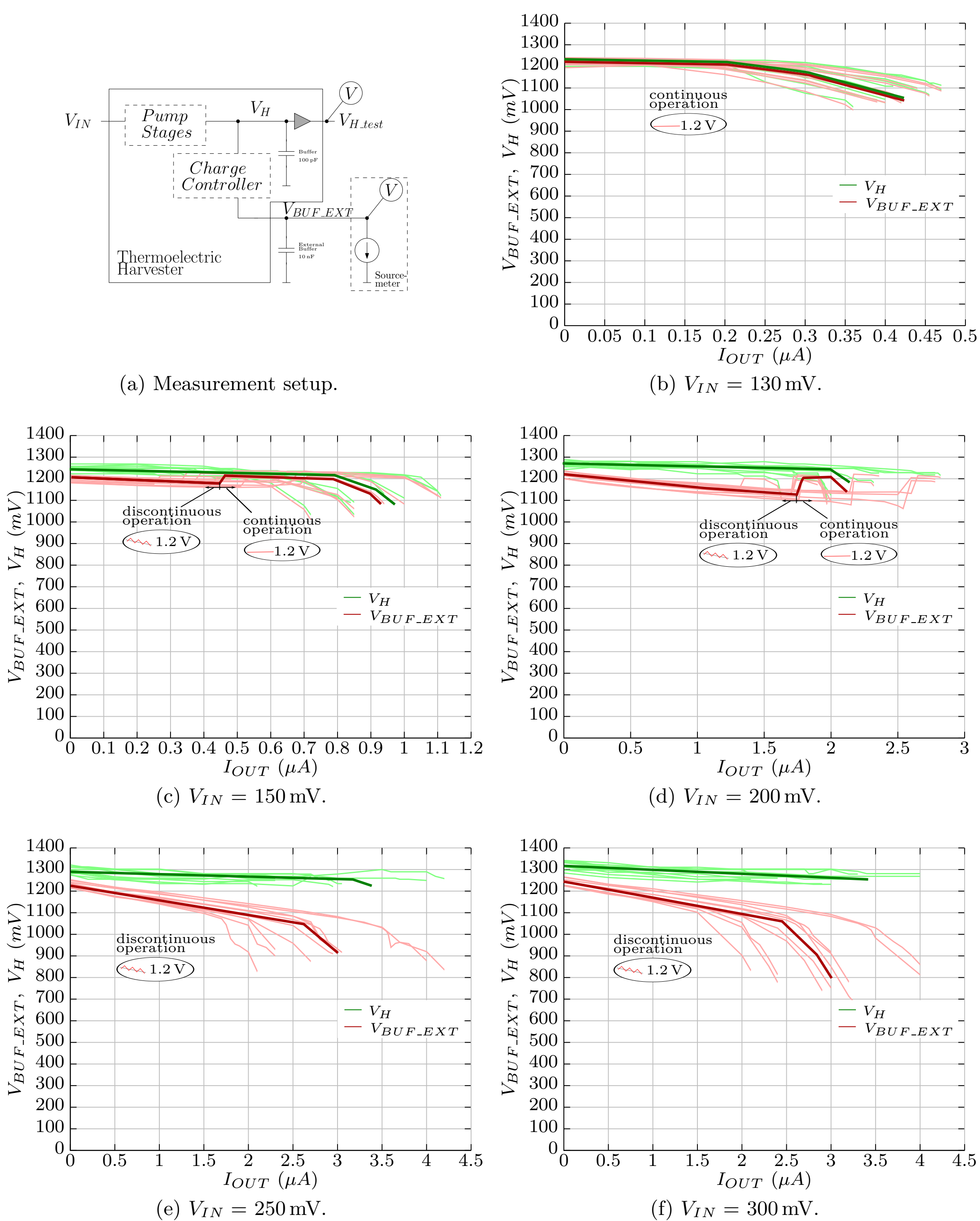
In Figure 4.25c, the measurement is repeated for an input voltage of $V_{IN} = 150\,\text{mV}$ which leads to an increased charge transfer per clock cycle. As a result, the output voltage remains stable until the output current reaches $I_{OUT} = 800\,\text{nA}$. Whilst for the previously discussed input voltage condition the circuit is always operated in continuous operation, the mode is changed to a duty-cycled mode for lower loads at $V_{IN} = 150\,\text{mV}$. In the discontinuous mode the oscillator is frequently disabled as $V_H$ reaches the maximum voltage level. As a result a ripple occurs at $V_{BUF\ EXT}$ which is indicated by a reduced voltage level at the external buffer capacitor due to the averaging effect of the voltmeter. The maximum load condition is reached for $I_{OUT} = 920\,\text{nA}$.

At $V_{IN} = 200\,\text{mV}$, the switch from the discontinuous mode to continuous mode occurs at about $1.7\,\mu\text{A}$. The corresponding plot is shown in Figure 4.25d. A maximum load of $I_{OUT} = 2.2\,\mu\text{A}$ is feasible.

Applying an input voltage of $V_{IN} = 250\,\text{mV}$ further increases the current capability of the circuit which is shown in Figure 4.25e. Due to the growing ripple, the average voltage at the external buffer capacitor successively decreases with the load current. The maximum current is given by $I_{OUT} = 3\,\mu\text{A}$.

Finally, Figure 4.25f shows the affect of a load current on the output voltage for an input voltage of $V_{IN} = 300\,\text{mV}$. The maximum output current is similarly to the $250\,\text{mV}$ measurement at $I_{OUT} = 3\,\mu\text{A}$ which represents the maximum current provided by the charge controller to the external buffer capacitor.

In this subsection the affect of a load current (e.g. leakage of the energy storage) on the voltage nodes $V_H$ and $V_{BUF\ EXT}$ was discussed. In addition, the figures allow estimation of the power provided by the circuit to an energy storage device for different input voltage conditions. It extends from $P_{OUT} = 400\,\text{nW}$ at $V_{IN} = 130\,\text{mV}$ to $P_{OUT} = 2.7\,\mu\text{W}$ at $V_{IN} > 250\,\text{mV}$. Investigation of the system efficiency for voltage conversion is discussed in the following subsection.




(a) Measurement setup. (b) $V_{IN} = 130\,\text{mV}$.

(c) $V_{IN} = 150\,\text{mV}$. (d) $V_{IN} = 200\,\text{mV}$.

(e) $V_{IN} = 250\,\text{mV}$. (f) $V_{IN} = 300\,\text{mV}$.

Figure 4.25: Measurement of the voltage at the external buffer capacitor ($V_{BUF\ EXT}$) and the internal high voltage domain ($V_H$) for different input voltages in dependency of the output current. The characteristics are based on 10 test samples.

### 4.9.3 Efficiency

The efficiency is defined by the power delivered to a load in comparison to the power taken by the system at the input node. As discussed in Chapter 3.4.2, in self-sustaining systems, it significantly depends on the control effort factor ($\gamma$) which was estimated by simulation in Table 4.3 for the corresponding system. From the table, the efficiency is expected to remain lower than 15 % for the harvesting circuit. Referring to Figure 4.26a, the output power ($P_{OUT}$) of the harvesting circuit is measured by loading $V_{BAT_EXT}$ with a defined current using a source meter in parallel to the external buffer capacitor. At the input node a precise ampere meter and a volt meter are used to obtain the corresponding input power ($P_{IN}$). The measurements, presented in Figure 4.26, show the system efficiency of the circuit for several input voltage conditions between $V_{IN} = 130\,\text{mV}$ and $V_{IN} = 300\,\text{mV}$.

For an input voltage of $V_{IN} = 130\,\text{mV}$, the circuit runs in continuous operation for all load currents. As shown in Figure 4.26b, the efficiency starts from zero and increases nearly linear with the output current to a maximum of about 7 % at $I_{OUT} = 420\,\text{nA}$. This is due to the fact that the control logic requires a constant amount of charge delivered within each clock cycle by the pump stages to maintain the system's functionally. This base load current is principally independent of the output current. As a result, a linearly growing $P_{OUT}$ leads to a linear improvement in efficiency.

Figure 4.26c shows the affect of a change in operation on the efficiency for different load conditions for an input voltage of $V_{IN} = 150\,\text{mV}$. For lower currents, the circuit runs in discontinuous operation and changes to continuous operation for a higher load. The change occurs at $I_{OUT} = 420\,\text{nA}$ which is indicated in the figure by a drop in efficiency of about 1 %. These characteristics can be explained as follows. In discontinuous mode the oscillator is frequently turned off which reduces the overall power demand of the control logic. When switching to continuous operation the higher control effort leads to the sudden drop in efficiency. Afterwards, the characteristic grows again linearly with the output power. The maximum efficiency is given by 10.5 % at 820 nA. In comparison to the continuous operation, the efficiency can be improved for low output currents by about 2 % by using discontinuous operation.

In Figure 4.26d, the efficiency characteristics at an input voltage of $V_{IN} = 200\,\text{mV}$ is shown. Up to an output current of $I_{OUT} = 1.7\,\mu\text{A}$ the circuit runs in discontinuous operation which improves the efficiency by more than 50 % at 500 nA in comparison to continuous operation. The peak efficiency of 13 % is achieved at about $I_{OUT} = 2\,\mu\text{A}$.

The plot of the efficiency at $V_{IN} = 250\,\text{mV}$ in Figure 4.26e shows the characteristics of discontinuous mode over the complete load current range. The efficiency saturates close to 12 % and decreases again for higher load currents. The reason can be found in the limitation of the power transfer from the internal to the external buffer capacitor due to the charge controller which results in a voltage drop that reduces the system efficiency.

Finally, the efficiency plot at an input voltage of $V_{IN} = 300\,\text{mV}$ is depicted in Figure 4.26f. The peak efficiency of 10.5 % is measured at $I_{OUT} = 2\,\mu\text{A}$ and decreases again for higher load currents.

In this sub-section the efficiency of the harvesting system was investigated for different load currents and several input voltage conditions. The measurements show a peak efficiency of 13 % which is in good correlation with the theoretical investigations in Chapter 3.4 and estimations by simulation in Chapter 4.5.2.

## 4.10 Conclusion

In Chapter 4 the design of a fully integrated thermoelectric energy harvesting circuit was presented starting with an introduction of transformer based, inductive and capacitive converter topologies including their characteristics. It was followed by the definition of the system architecture and its functional description during the start-up, ramp-up and regular mode operation. Afterwards, the sub-circuits were discussed in detail.

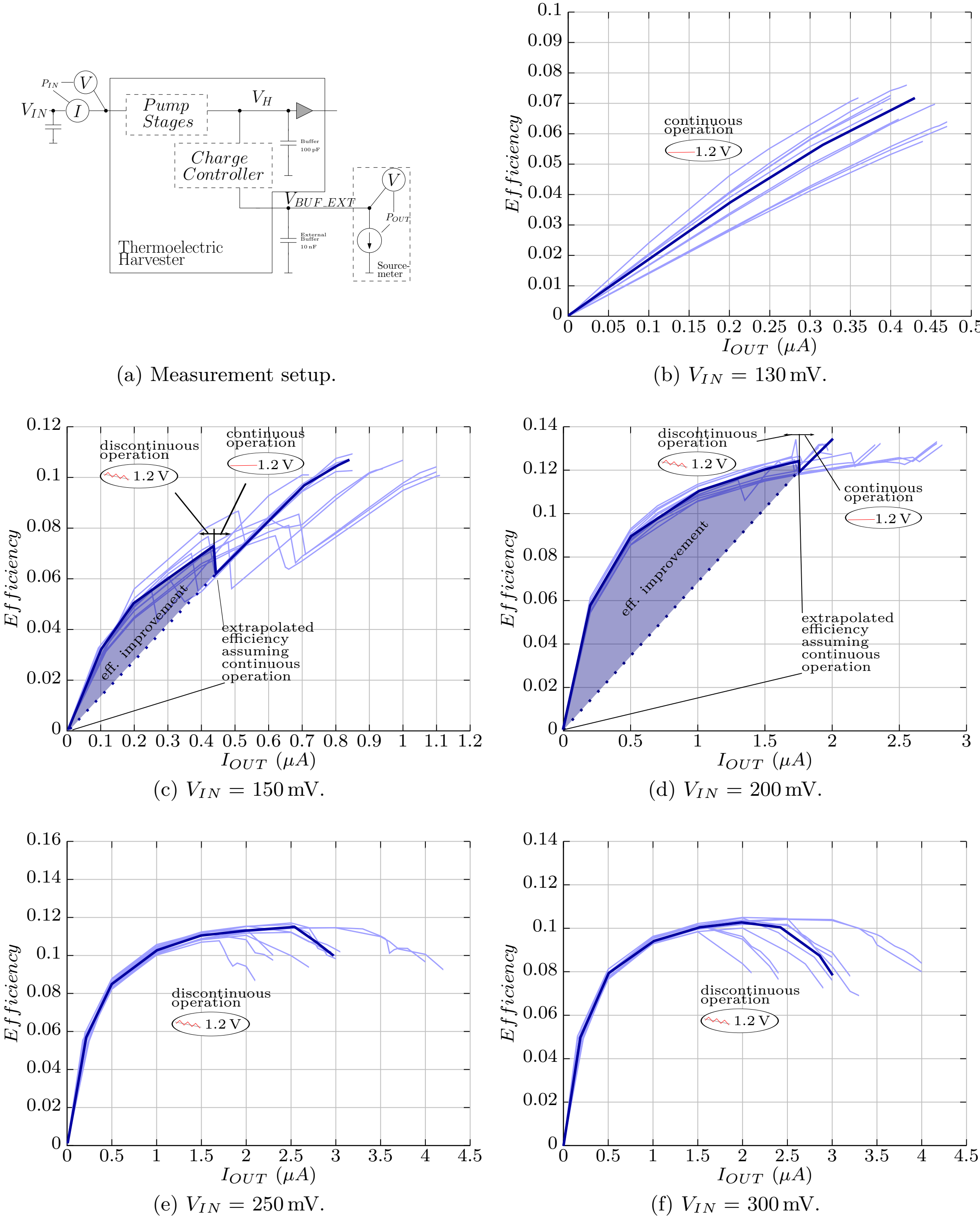
In order to increase the voltage gain an encapsulated on-chip capacitor with a negligible top-plate capacitance was presented. Using this device the pump stages for sub-threshold and super-threshold operation were designed. By using a bootstrapping technique an overdrive of the switches independent of the input voltage is feasible. To start the circuit at ultra-low voltage conditions a free-running clock signal generator based on logic gates of the ultra-low voltage digital cell library and clock doublers was implemented. In order to sufficiently transfer charge from stage to stage a charge pump driver for ultra-low voltage inputs was developed.

The clock signals were generated by two kinds of oscillators. A sub-threshold oscillator directly powered by the input was used during the ramp-up mode while a low-power relaxation oscillator provided a stable frequency in regular mode operation mode. In order to en-/disable the corresponding operation modes, level detectors that used a locally generated reference voltage to define the corresponding switching thresholds were used.

As in self-sustaining circuits, the control logic is powered from the internal buffer capacitor and a discharge below a certain voltage level has to be prevented. This is ensured by the charge controller limiting the charge transfer from the internal to the external energy storage of the corresponding circuit.

The final section dealt with measurement results based on 10 samples of the thermoelectric energy harvesting circuit. The start-up voltage and conversion ratio was investigated first. The start of operation was found to occur at an input voltage of $V_{IN} = 90\,\text{mV}$ providing an insufficient voltage level at the output node. The nominal value as reached at $V_{IN} = 145\,\text{mV}$ and could be reduced during operation to $V_{IN} = 110\,\text{mV}$. The voltage gain measurement was followed by the output current characteristics and the efficiency of the complete system. It reached from $P_{OUT} = 400\,\text{nW}$ at $V_{IN} = 130\,\text{mV}$ to $P_{OUT} = 2.7\,\mu\text{W}$ at $V_{IN} > 250\,\text{mV}$ at a peak efficiency of 13 %.

In Table 4.4, a list of transformer based and inductive thermoelectric energy harvester circuits are presented from recent works: [23] by J.-P. Im, [4] by E. Carlson and [8] by P.-H. Chen. The authors reached very good efficiencies and low input voltage in operation but suffered from deficient external devices such as a coil or a bulky transformer. Only [21] by H. Hernandez showed




(a) Measurement setup.

(b) $V_{IN} = 130\,\text{mV}$.

(c) $V_{IN} = 150\,\text{mV}$.

(d) $V_{IN} = 200\,\text{mV}$.

(e) $V_{IN} = 250\,\text{mV}$.

(f) $V_{IN} = 300\,\text{mV}$.

Figure 4.26: Measurement of the efficiency at the external buffer capacitor ($V_{BUF_EXT}$) for different input voltages in dependency of the output current. The characteristics are based on 10 test samples.

a fully integrated inductive boost converter for thermoelectric energy harvesting applications but without providing measurement results from silicon. This list is continued in Table 4.5 by focusing on capacitive examples, enabling a fully integrated solution. The results of [19] by R. Grezaud, [24] by W. Jung and [36] by J. Kim are compared to the thermoelectric energy harvesting circuit proposed in Chapter 4.

| Reference | [23] | [4] | [8] | [21] |
|---|---|---|---|---|
| Published in | JSSC | JSSC | ISSCC | LASCAS |
| Year | 2012 | 2010 | 2011 | 2013 |
| CMOS Process | 130 nm | 130 nm | 65 nm | 180 nm |
| Type | flyback/inductive | inductive | inductive | inductive |
| Ext. Components | yes | yes | yes | no |
| Start Mechanism | self-starting | ext. voltage | aux. ch. p. | aux. ch. p. |
| Startup Volt. | 40 mV | 600 mV | 80 mV | 300 mV |
| Min. Input Volt. | 40 mV | 20 mV | 80 mV | 300 mV |
| Output Volt. | 2 V | 1 V | 1.3 V | 1.1 V |
| Stages | 1 | 1 | 1 | 1 |
| Peak Efficiency | 61 % ($V_{IN} = 300\ mV$) | 75 % ($V_{IN} = 100\ mV$) | 60 % ($V_{IN} = 80\ mV$) | 45 % ($V_{IN} = 300\ mV$) |
| Note | external transformer required | external voltage required to start | post-process $V_{TH}$ tuning by hot carrier injection | results are based on simulation |

Table 4.4: Performance comparison of transformer based and inductive thermoelectric energy harvesters.

| Reference | [19] | [24] | [36] | **This Work** |
|---|---|---|---|---|
| Published in | NEWCAS | ISSCC | ISSCC | |
| Year | 2013 | 2014 | 2014 | **2015** |
| CMOS Process | 180 nm | 180 nm | 130 nm | **130 nm** |
| Type | capacitive | capacitive | capacitive | **capacitive** |
| Ext. Components | no | no | no | **no** |
| Start Mechanism | self-starting | self-starting | self-starting | **self-starting** |
| Startup Volt. | 250 mV | 140 mV | 150 mV | **145 mV** |
| Min. Input Volt. | 360 mV | 350 mV | 180 mV | **110 mV** |
| Output Volt. | 1.2 V | 2.2 V-5.2 V | 0.62 V | **1.2 V** |
| Stages | 3 | 4 | 3 | **21** |
| Peak Efficiency | 70 % ($V_{OPEN} = 900\ mV$) | 50 % ($V_{IN} = 450\ mV$) | 34 % ($V_{IN} = 180\ mV$) | **13 %** ($V_{IN} = 200\ mV$) |
| Note | - | low $V_{TH}$ devices | switched body biasing | - |

Table 4.5: Performance comparison of capacitive thermoelectric energy harvesters.

# Chapter 5

# Research Summary and Outlook

In this thesis, the issue of harvesting electric power from body heat was discussed over the entire spectrum in four chapters by addressing the physics of thermoelectric generators, operation of digital logic cells in the deep sub-threshold region, linear charge pumps for ultra-low voltage inputs and the development of the complete thermoelectric energy harvesting system to be used in Body Area Networks. This chapter summarizes the work and presents the main achievements in the respective sections. Finally, a first demonstration system of an on-skin sensor containing the thermoelectric harvester and a temperature sensor on a single die is shown. An outlook on future work in this field of research will also be given.

## 5.1 Summary of Achievements

Starting with the system architecture of state-of-the-art thermoelectric generators and their characteristics in different environments, an equivalent circuit diagram combining the thermal and electrical properties of a thermoelectric harvesting system was developed in Chapter 1. The model allows power output estimation and optimization based on the thermal and electrical parameters of commercially available thermoelectric generators and the ambiance. While the former is typically provided in the device manufacturers data sheet the latter depends on the application scenario. The focus in this thesis was an on skin patch for Body Area Networks. Therefore the characteristics of the human body were investigated by performing a literature study.

Knowing the challenges of thermoelectric energy harvesting in low-temperature gradient environments, Chapter 2 addressed the development of ultra-low voltage digital logic cells to be operated directly from a thermoelectric generator in the deep sub-threshold region starting from $V_{DD} = 90\,\text{mV}$. This corresponds to a difference in temperature of $< 1\,°\text{C}$ across the used thermoelectric generator. The result was achieved by introducing a leakage compensation technique reducing the impact of process variation dependencies, on the switching threshold of CMOS gates in the sub-threshold region, by 85 % without the need for special process options or post-fabrication steps. The approach was used to design basic combinational and sequential logic gates resulting in an ultra-low voltage digital cell library which is operational at a supply voltage range between 90 mV and 1.2 V at room temperature and 120 mV to 1.2 V at a temperature of 120 °C. The functionality of the logic gates in the composite was verified by the design and manufacturing of basic logic circuits (full adder, counter and shift register) and

measurements over a temperature range from −20 °C to 120 °C. The research results in this chapter led to patent applications in several nations [27], [28] and [29].

In Chapter 3, gate control strategies of charge pumps under low voltage conditions were investigated in order to find a suitable topology for fully integrated thermoelectric energy harvesters. From this, a cross-coupled charge pump using bootstrapped control signal injection was found to be a suitable topology to realize a self-sustaining charge pump for ultra-low voltage inputs. Analytical steady-state models of conventional charge pumps are already present in the literature. As in this case the DC/DC converter needed to be self-sustaining, the second part of the chapter dealt with the development of an analytical steady state model for self-sustaining operation. The resulting characteristic curves of voltage gain and efficiency in dependency of process- and control related parasitic effects allowed optimization of the number of stages to achieve a certain voltage gain and efficiency which enables an optimized design flow.

Chapter 4 combined the results of the previous chapters by addressing the design of a fully integrated thermoelectric energy harvesting system to be used in Body Area Networks. The following list highlights the main achievements during the design phase:

- A high-density on-chip capacitor based on a vertically oriented comb-structure stacked on top of a MOS capacitor which was designed as a pump capacitor. It provides a capacitance of 6.12 pF/µm$^2$ and a negligible parasitic top-plate capacitance as the top-plate electrode is completely encapsulated by the bottom plate. As a result the voltage gain factor of an idealized charge pump is feasible with this structure.
- By using the ultra-low voltage digital cell library, a free-running sub-threshold clock generator to control the switches of the pump stages was developed. This allowed an operation to start at an input voltage as low as $V_{IN} = 90\,\text{mV}$. Instead of an extra oscillator, the signal generator contains an inner feedback loop that uses a state controller to adapt the frequency according to the charge-transfer time of the pump stages in the sub-threshold region.
- The switches of the pump stages consist of regular transistors with a threshold voltage 2-3 times the input voltage level. In order to improve the charge transfer behavior during start-up, a sub-threshold clock doubler circuit, which drove the gates of the switches at twice the signal amplitude provided at the input was designed.
- A novel charge pump driver providing similar current capability for the rising and falling edge was developed by implementing a negative voltage doubler to control the PMOS devices independently of the input voltage level.
- Charge pump stages for sub- and super-threshold operation through use of bootstrapped control signal injection enable charge transfer in all operation modes.
- A voltage level detector sensing the voltage level at the output node of the charge pump without putting a load on it. The signal is shifted to lower values and compared to the input voltage level. The circuit is operational over a wide voltage and temperature range without requiring a start-up mechanism.

- A temperature compensated voltage level detector using a locally generated reference voltage was designed based on a leakage current source stacked on top of a bipolar diode. The circuit is operational over a wide voltage and temperature range without requiring any start-up mechanism.
- A charging controller based on charge-overflow monitoring was developed to connect a highly capacitive energy storage device to the low capacitive internal buffer without disturbing the operation of the self-sustaining circuit.

The system was manufactured and evaluated through the measurement of 10 samples. Start of operation at an input voltage of $V_{IN} = 90\,\text{mV}$ was achieved. At $V_{IN} = 145\,\text{mV}$, the nominal output voltage of $V_{OUT} = 1.2\,\text{V}$ is reached which remains constant down to input voltages of 110 mV in operation. The voltage gain measurement was followed by the output current characteristics and the efficiency of the complete system. The circuit delivers a maximum output power between $P_{OUT} = 400\,\text{nW}$ at $V_{IN} = 130\,\text{mV}$ and $P_{OUT} = 2.7\,\mu\text{W}$ at $V_{IN} > 250\,\text{mV}$ and achieves a peak efficiency of 13 %. It is therefore well-suited to power a sensor in Body Area Networks.

## 5.2 Concepts of System Design

*The following chapter is mainly taken from [32].* ■

The work in this thesis focused on the design of a thermoelectric energy harvesting interface to power an on-skin sensor node in Body Area Networks. It therefore presents a solution for maintaining a power supply but does not cover the development of a complete sensor node which would require, in addition, a sensor and a transceiver unit. Nevertheless, a few thoughts and solutions to arising challenges in system design are presented in the following sub-sections. The corresponding patent application is available in [32].

### 5.2.1 Continuous Data Logging of Conventional Implanted Passive Sensor Grains Using a Smart Booster Antenna Skin Patch

In this sub-section an application scenario to power an implanted passive sensor grain using a smart booster antenna skin patch with thermoelectric energy harvesting capability is presented.

Implants are typically powered by finite local energy sources (e.g. batteries) which limits their lifetime and requires repetitive replacement. Another solution are passive sensors powered by inductive coupling from an external source. As implants are typically small in size and human tissue is known to absorb RF signals, the maximum distance for power transmission to such a passive sensor grain is limited to the mm-range. It can be significantly increased by using an interface plaster containing a booster antenna. Such a device is able to collect the magnetic field from a large area by using a pick-up antenna and concentrates the field energy in a small coupling coil located straight over the implant. As a result the reading distance increases significantly [53].

One issue of passive sensor systems is that they are not functional without an external reader device and therefore not suitable for continuous data logging in, for example, the domestic environment. A solution to this problem is to extend the interface plaster with a thermoelectric harvesting unit which uses the temperature gradient between skin and environment to accumulate electric power in an energy storage device. At regular time intervals the locally generated power is used to inductively couple electric power from the plaster to the (passive) implanted device via the small coupling antenna. For the implant, the plaster emulates a reader device and triggers a measurement cycle. The result of each measurement is stored in the non-volatile internal memory. This enables continuous data logging of conventional implanted passive sensor grains. Power intensive calibration and read-out of measurement results is accomplished by again applying an external field using an NFC-reader device (e.g. smartphone).

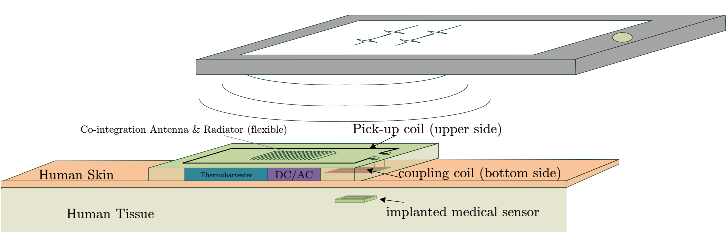
The sketch of the application scenario is depicted in Figure 5.1a and the cross section of the plaster in Figure 5.1b. A small sensor grain is implanted and therefore enclosed by human tissue. On the skin the smart interface plaster is mounted by aligning the coupling coil above the implant. The patch includes the harvesting unit and interconnects the coupling coil located at the bottom to the pick-up antenna on the upper side of the interface plaster. It consists of several windings enclosing nearly the complete surface of the patch. The RF-field provided by the reader is collected by the pick-up coil and guided through the device and inductively induced to the medical implant by the coupling coil. The harvesting unit consists of a thermoelectric generator, the harvester interface and energy storage. In addition a DC/AC converter is implemented in order to emulate the reader's field to provide self-sustaining operation. Two operation modes are available.

- **Mode A** is activated by providing an external field using a reader device. This allows data communication and calibration of the implanted device within an extended range using the booster antenna of the interface plaster. In addition, instantaneous measurements and data read-out is possible. In this mode the harvesting interface is disconnected from the coupling coil.
- **Mode B** represents operation without applying an external field. The harvesting unit continuously accumulates energy in an energy storage cell and is connected to the coupling antenna. Duty cycled activation of the DC/AC converter transmits power to the implanted sensor via the coupling coil and emulates a reader device. As a result the passive sensor wakes up to execute a measurement cycle and store the result internally in the non-volatile memory.

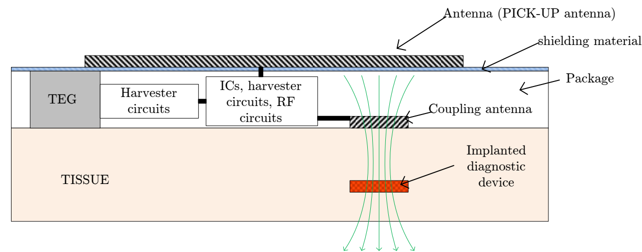
In this sub-section the system architecture was briefly discussed. The following part addresses the issue of integrating an antenna on a flexible heat sink.

### 5.2.2 Co-integration of Antenna and Heat Sink on a Flexible Substrate

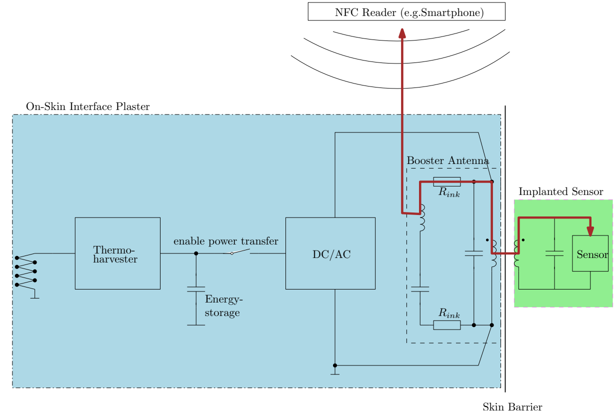
A wireless sensor plaster suffers from limitations to its thickness and requires a flexible architecture in order to align it to the skin. As a result a huge heat sink, which is typically



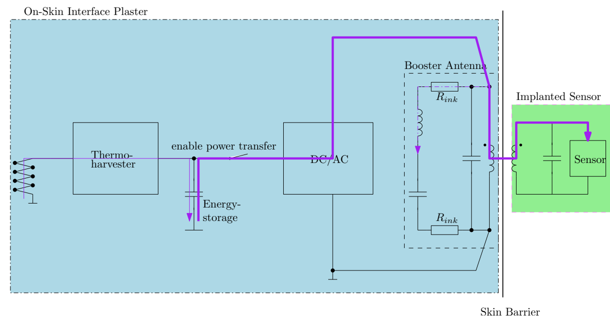

(a) Sketch of the interface plaster during read-out of data.




(b) Cross section of the plaster. The pick-up antenna is located on the top-side while the coupling coil is located close to the skin. The harvesting unit is integrated in the patch.




(c) MODE A: Power transmission and data communication with extended range using the booster antenna of the interface plaster.




(d) MODE B: Continuous power generation by the energy harvesting circuit and duty cycled activation of the DC/AC unit to trigger a measurement operation.

Figure 5.1: Continuous Data Logging of conventional implanted passive sensor grains using a smart booster antenna skin patch. System architecture and description of operation.

used in industrial application, is not feasible in Body Area Networks. Instead, the heat energy is distributed over the total surface of the patch using a thermally high conductive material (e.g. metal). A cross section of a sensor plaster with the corresponding heat flow is shown in Figure 5.2a. The bottom plate collects heat from the skin which is transfered through the thermoelectric generator to the top surface for heat distribution and radiation.

A complication is the implementation of the antenna as the metal surface would disturb the data communication. It can be solved using an electrical insulator as the heat sink material or reduction of the surface area to create a space for the antenna. Both approaches lead to a weak performance of the heat sink.

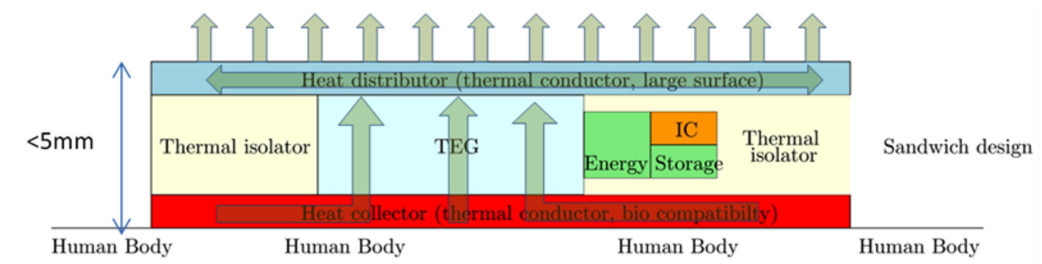
To overcome these issues a new heat sink architecture is proposed in this section. It enables co-integration of heat sink and antenna capability without compromise though use of a three-layer architecture. Each layer is described in the following list (Figure 5.2b):

- **Metal Layer:** In order to decrease the interface resistance from the heat sink to the environment, its surface needs to be maximized. As bulky cooling fins are not feasible in Body Area Networks the surface of the top plate of the sensor plaster is typically used. Therefore a thermally low-resistive material is required to distribute the heat from the small package of the thermoelectric generator to the top-plate of the patch. This can be achieved by using a flexible copper foil of 10 µm thickness.
- **Ferrite Layer:** The flexible ferrite foil has a thickness of 100 µm and shields the magnetic field lines from the metal layer by guiding them directly underneath the antenna layer through the ferrite material. As a result the field lines are not disturbed by the metal layer. Ferrite is known to be an electrical insulator but conducts heat relatively well. In this architecture, the minimal thickness and the rougher surface leads to an improved heat transfer to the environment.
- **Antenna Layer:** Due to the high electrical resistance of ferrite, the antenna can be directly applied using inkjet printing of conductive silver.

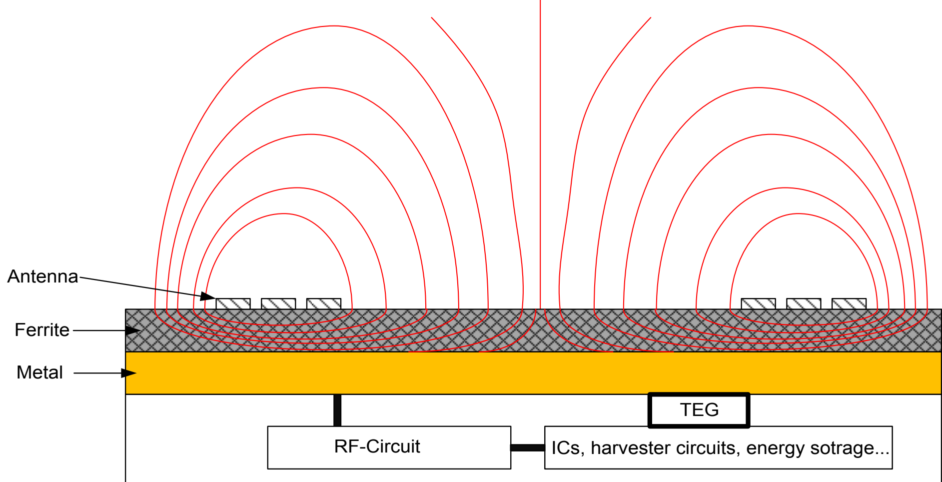
The approach leads to a good heat distribution by the metal layer, a thin and flexible RF field insulation by the ferrite layer and a reduced thermal interface resistance to the environment due to increased surface. It is usable up to a frequency of 13.56 MHz (NFC). A picture from the lab during manufacturing is shown in Figure 5.2c. The pick-up coil is located on the outer rim and encloses an area of printed cooling fins to further enlarge the surface interface to the environment.

## 5.3 Future Work

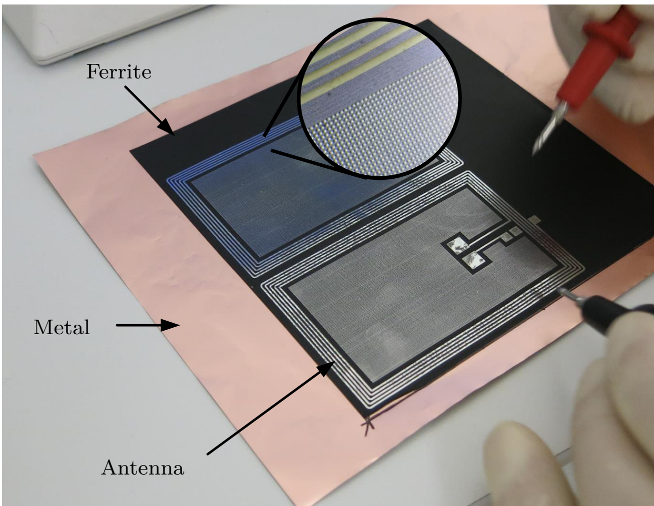
In this thesis, the design of a fully integrated thermoelectric energy harvesting circuit was presented. Nevertheless, a sensor node requires, in addition to the power source, a sensing circuit and a data transmitter. Whilst a low power temperature sensor is already available at Infineon and therefore implemented on silicon in Figure A.3, the transmitter needs to be developed by another PhD candidate.




(a) Thermal heat path through the sensor plaster. The bottom plate collects heat from the skin which is transfered via the thermoelectric generator to the top plate for heat distribution and radiation to the environment.




(b) Course of magnetic field lines. They are guided through the ferrite layer and are therefore not influenced by the metal layer underneath.




(c) Picture from a prototype of the proposed archtitecture.

Figure 5.2: Co-integration of antenna and heat sink on a flexible substrate using a three-layer architecture.

In addition the idea of continuous data logging of conventional implanted passive sensor grains using a smart booster antenna skin patch needs to be further investigated and manufactured.

# Appendix A

# Test Chip Layouts

Each circuit presented in this thesis has been fabricated in an Infineon 0.13 µm CMOS process. This chapter gives an overview of the layouts of the various test chips containing these circuits. The IC are named according to the respective chapter names.

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## A.1 Development of an Ultra-Low Voltage Digital Logic Cell Library

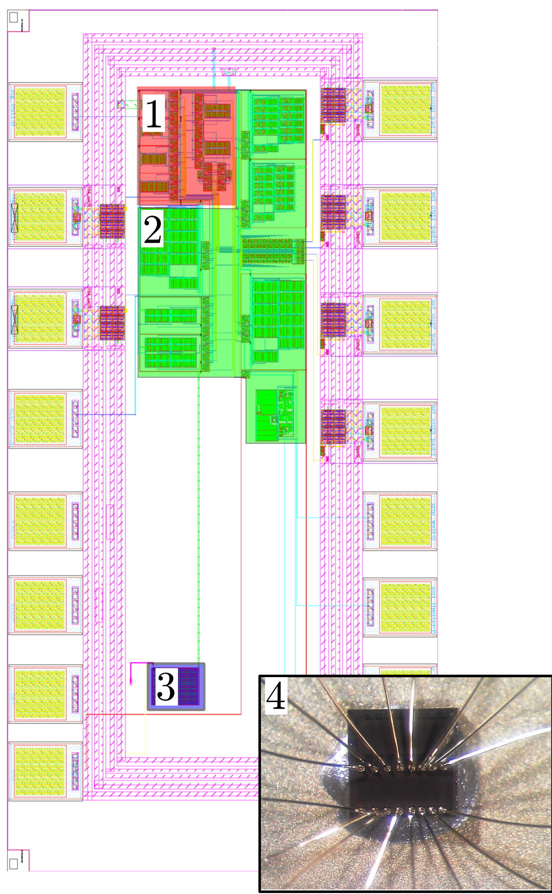


Figure A.1: Test Chip ultra-low voltage digital logic cells.

| | |
|---|---|
| 1 . . . . . . . . . . . . . . . . . . . . . . . . . . . | Basic logic gates (inverter, NAND, NOR,...) |
| 2 . . . . . . . . . . . . . . . . . . . . . . . . . . . | Basic digital logic circuits (full-adder, counter,...) |
| 3 . . . . . . . . . . . . . . . . . . . . . . . . . . . | High density on chip capacitor |
| 4 . . . . . . . . . . . . . . . . . . . . . . . . . . . | Test chip photo |

## A.2 Design of a Fully Integrated Thermoelectric Energy Harvester with Sub-threshold Start-up Capability (Version 1)

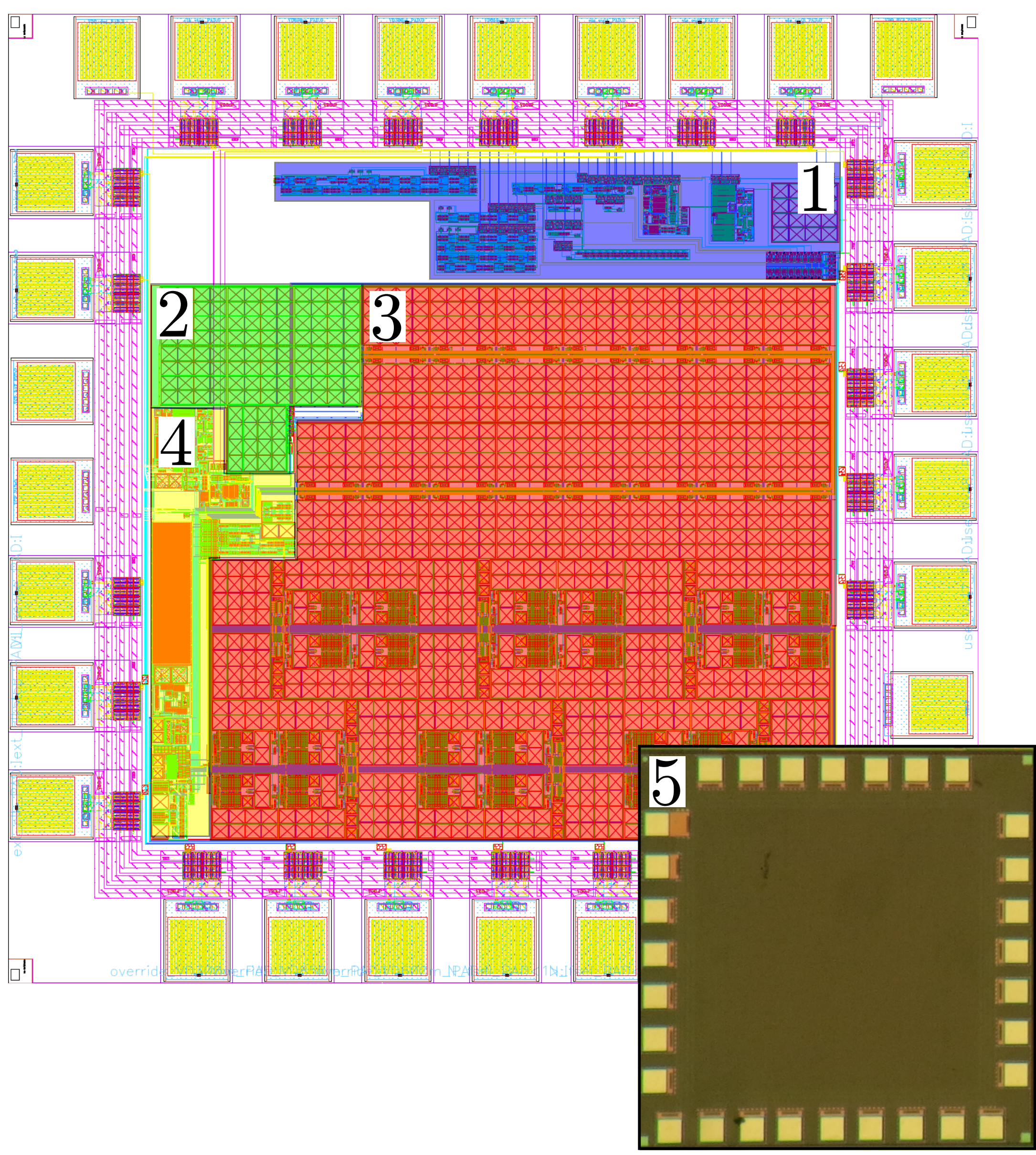


Figure A.2: Version 1 of the thermoelectric energy harvesting test chip.

1 . . . . . . . . . . . . . . . . . . . . . . . . . . . . Sub-threshold test structures
2 . . . . . . . . . . . . . . . . . . . . . . . . . . . . Internal buffer capacitor array
3 . . . . . . . . . . . . . . . . . . . . . . . . . . . . Pump stages
4 . . . . . . . . . . . . . . . . . . . . . . . . . . . . Control unit
5 . . . . . . . . . . . . . . . . . . . . . . . . . . . . Test chip photo

## A.3 Design of a Fully Integrated Thermoelectric Energy Harvester with Sub-threshold Start-up Capability (Version 2) Including a Low-power Temperature Sensor

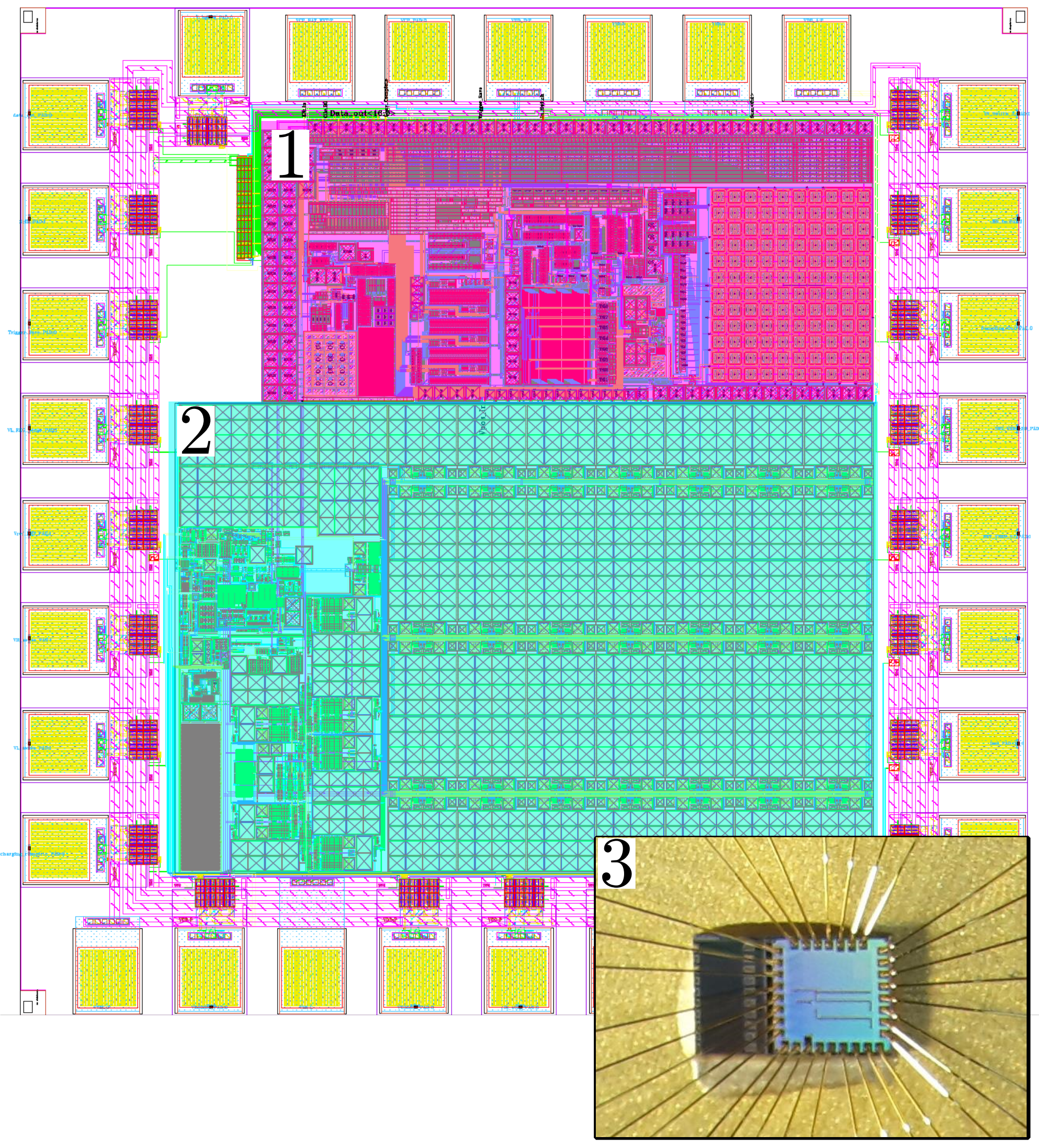


Figure A.3: Monolithic implementation of Version 2 of the thermoelectric energy harvesting interface and a low power temperature sensor.

| | |
|---|---|
| 1 . . . . . . . . . . . . . . . . . . . . . . . . . . . | Low-power temperature sensor provided by Infineon |
| 2 . . . . . . . . . . . . . . . . . . . . . . . . . . . | Layout optimized version 2 of the thermoelectric harvesting interface |
| 3 . . . . . . . . . . . . . . . . . . . . . . . . . . . | Test chip photo |

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