Alternative Concepts for Linear Voltage Regulators in Deep Sub-Micron Technologies

Thomas Rene Jackum

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Dipl.-Ing.(FH) Thomas Rene Jackum

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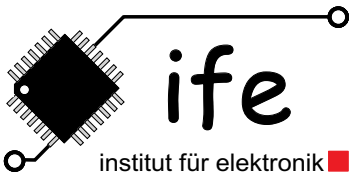

Institute of Electronics

1st Supervisor: .....
Univ.-Prof. Dipl.-Ing. Dr. techn.
Wolfgang Pribyl, MBA

2nd Supervisor: .....
Univ.-Prof. Dipl.-Ing. Dipl.-Phys. Dr. rer. nat.
Doris Schmitt-Landsiedel

Graz, October 2013

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Abstract

Linear voltage regulators have been widely used circuits in electronics and micro electronics for decades. They are used to supply the following circuits with a constant voltage and thereby keep disturbances at the main supply away from the sensitive circuits. Due to the evolution of integrated CMOS technologies, new challenges and opportunities come up continuously. In this thesis new concepts for linear voltage regulators have been investigated which became possible in deep sub micron technologies. Three different concepts are presented in this thesis. All of them have been implemented and verified on silicon in a 65nm CMOS technology. The first concept presented is a linear voltage regulator that is fully digitally controlled. Due to the deep sub micron process the digital error amplifier has low area consumption and also a reasonably small current consumption that can compete with analog implementations. The second concept presented is a fast transient response output capacitor-less linear voltage regulator for load currents in the 100mA range. Such a linear voltage regulator doesn't need an external load capacitor opposed to a conventional linear voltage regulator for such a load current range. In the used 65nm CMOS process, an internal load capacitor with reasonably small area consumption can be implemented. Due to the fast error amplifier the needed load capacitance value can be kept small while still ensuring low output voltage deviation during fast transient disturbances. The third concept presented is a further improved output capacitor-less linear voltage regulator. This linear voltage regulator can handle load current jumps that are ten times faster compared to the previous version. To reduce the area consumption an optimized non-standard ESD protection for the pass device and the load has been developed. Implementation details and measurement results are presented for each of the three concepts.

Kurzfassung

Linearspannungsregler werden seit Jahrzehnten in der Elektronik und Mikroelektronik eingesetzt. Sie versorgen die nachfolgenden Schaltungen mit einer konstanten Spannung. Dadurch werden die nachfolgenden, oft empfindlichen Schaltungen vor Störungen auf der Versorgungsleitung abgeschirmt. Durch die kontinuierliche Weiterentwicklung von CMOS Fertigungsprozessen entstehen auch laufend neue Herausforderungen und Möglichkeiten. In dieser Dissertation wurden neue Konzepte für Linearspannungsregler untersucht, welche durch Fertigungsprozesse mit Strukturgrößen deutlich unter dem Mikrometerbereich ermöglicht wurden. Drei verschiedene Konzepte werden hier vorgestellt. Dabei wurden alle in einem 65nm CMOS Prozess implementiert und auf Silizium verifiziert. Das erste Konzept ist ein digital geregelter Linearspannungsregler. Durch den 65nm Prozess verbraucht der digitale Regler wenig Fläche und gleichzeitig wenig Strom, vergleichbar mit voll analogen Implementierungen. Das zweite Konzept ist ein Linearspannungsregler ohne externe Stützkapazität am Ausgang. Dieser Regler wurde für schnelle transiente Störungen und Lastströme im 100mA Bereich ausgelegt. Konventionelle Linearspannungsregler für diesen Strombereich benötigen externe Stützkapazitäten. Durch den 65nm CMOS Prozess stehen einerseits flächeneffiziente chipinterne Kapazitäten zur Verfügung und andererseits sorgt ein schneller Regler für geringe Spannungsabweichungen, wenn Störungen auf das System einwirken. Das dritte Konzept ist ein weiter verbesserter Linearspannungsregler ohne externe Stützkapazität. Dieser Regler kann im Vergleich zum Vorgänger zehnmal schnellere Störungen ausregeln. Um den Flächenbedarf zu optimieren wurde ein spezieller ESD Schutzmechanismus für diesen Regler entwickelt. Die Implementierungsdetails und Messergebnisse aller drei Konzepte werden präsentiert.

Acknowledgments

I would like to thank Infineon Technologies Austria AG for giving me the possibility to do my research at their facilities. Representatively, I would like to thank Dr. Florian Michl the head of the DES IP AMS department in the Development Center Villach for the chance to work in this department. Due to this chance I've been able to have fruitful discussions with several experts working on analog integrated circuit design in this department. Additionally, I've been enabled to tape out three dedicated test chips on different linear voltage regulators. I would also like to thank my mentor at Infineon Dipl.-Ing. Roman Riederer who supported me in getting started with the topic linear voltage regulators. He often supported me with advice and valuable discussions.

Furthermore, I would like to thank my supervisor Prof. Wolfgang Pribyl. He offered me the possibility to start my research in such an interesting field that led to this dissertation. Additionally, I would like to appreciate my colleague Dipl.-Ing. Gerhard Maderbacher with whom I've had intensive and fruitful discussions, not only limited to the scope of my thesis.

My special thanks I want to address to my parents who supported me during my whole studies.

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List of Abbreviations

AC	Alternating current
ADC	Analog to digital converter
BJT	Bipolar junction transistor
CCM	Continuous conduction mode
CDM	Charged device model
CMOS	Complementary MOS
DAC	Digital to analog converter
DC	Direct current
DEMOS	Drain extended MOS
DPI	Direct power injection
DSP	Digital signal processor
DVS	Dynamic voltage scaling
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EOS	Electrical over stress
ESD	Electrostatic discharge
ESR	Equivalent series resistance
HBM	Human body model
HDL	Hardware description language
IC	Integrated circuit
I/O	Input/output
JFET	Junction field effect transistor
LDO	Low dropout linear voltage regulator
LHP	Left half plane
LSB	Least significant bit
LVR	Linear voltage regulator

MOS	Metal oxide semiconductor
NMOS	N-channel MOS transistor
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PD	Proportional and derivative
PDA	Personal digital assistant
PID	Proportional, integrative and derivative
PLL	Phase locked loop
PMOS	P-channel MOS transistor
PSR	Power supply rejection
PSRR	Power supply rejection ratio
PVT	Process, voltage and temperature
RHP	Right half plane
SAR	Successive approximation register
SC	Switched capacitor
SiP	System in package
SMPS	Switched mode power supply
SoC	System on chip
UGF	Unity gain frequency
VDD	Common drain voltage (positive supply voltage)
VHDL	Very high speed integrated circuit hardware description language
VSS	Common source voltage (negative supply voltage)

1 Introduction

In this thesis alternative concepts for linear voltage regulators are discussed. Three different concepts have been investigated deeply and implemented on a chip. Since linear voltage regulators are major components in power management systems a short overview on the field power management will be given.

1.1 Power Management

What is power management? An explanation of how power management is interpreted in this thesis follows:

Today's systems on chip (SoC) consist of several different building blocks depending on the application of the SoC. Depending on the function of each building block they often don't need to operate at the same time. Each building block consumes a different amount of current. Furthermore, some building blocks may need to be connected to a different supply voltage. E.g. a microcontroller may operate at 1.2V in its core while its I/O (input/output) pins operate at 2.5V and an embedded analog to digital converter (ADC) needs to be supplied with 5V. From the supply point of view the easiest solution would be to build all blocks in the same voltage domain and supply all the blocks as long as the system is turned on. But this wouldn't be the optimal solution from the power dissipation point of view. This is especially a problem in systems where the thermal budget is critical (e.g. systems with high power dissipation in a small form factor) and in systems where the supply energy is very limited (e.g. battery supplied systems). The aim of power management is now to supply each building block with the necessary voltage during the time the building block is active and allow consuming the right amount of current from this supply. Supplying the subsystem only as long as it needs to operate saves idle power. Supplying the subsystem with the minimum voltage it requires to operate properly saves active power while it is on. And designing the power supply only for the maximum current

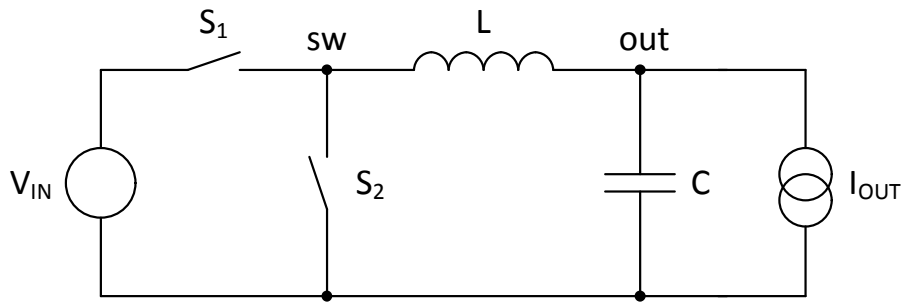

Figure 1.1: Basic topology of an inductor based DC-DC buck converter

the subsystem could need reduces the power consumed by the voltage regulator itself.

For DC-DC voltage conversion (i.e. DC voltage in and DC voltage out) there are basically three different schemes available. These are the inductor based DC-DC converter, the switched capacitor DC-DC converter and the linear voltage regulator. The inductor based DC-DC converter and the switched capacitor DC-DC converter are often called switched mode power supplies (SMPS) since they need to switch an energy storing element (either inductor or capacitor) in their circuit. On the other hand a linear voltage regulator is typically a continuous time circuit. Each of the three converter schemes has its advantages and disadvantages that subsequently decide which converter is used in which application. The basic properties of each converter type will be discussed briefly in the following.

1.1.1 Inductor Based DC-DC Converter

As its name indicates, the energy conversion of the inductor based DC-DC converter is realized by means of an inductor. The most commonly known type of inductor based DC-DC converter is the basic buck converter shown in Figure 1.1. The buck converter can only generate an output voltage that is lower than the input voltage, but also boost converters exist, which generate an output voltage higher than the input voltage. The theoretical maximum efficiency of this converter is 100% and it is independent of the ratio between input voltage and output voltage. This means all the energy consumed at the input of the converter is transferred losslessly to the output. Real converters that are commercially available often achieve efficiency values larger than 90% over a wide operating range e.g. [1].

The working principle shall be explained in the continuous conduction mode (CCM).

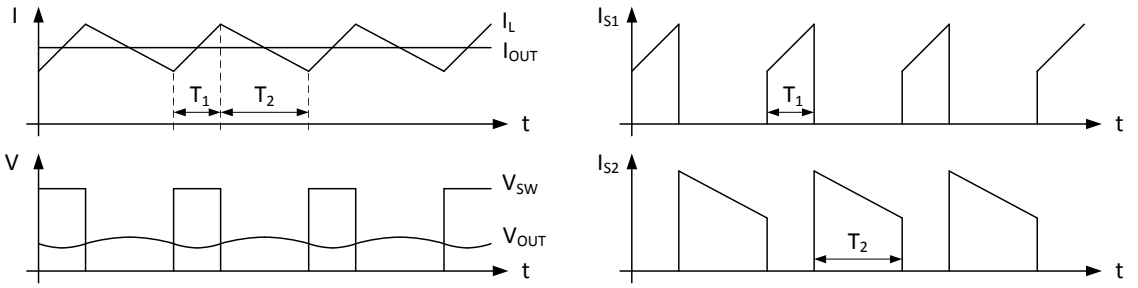

Figure 1.2: Voltages and currents in the inductor based DC-DC buck converter

In this mode there is always a current flowing through the inductor. Because the inductor is connected in series to the load the DC load current needs to flow through this inductor. The voltage conversion from the input to the output needs a superimposed nearly triangular AC current through the inductor. In a first phase during T_1 the switch S_1 in Figure 1.1 is closed while the switch S_2 is open. As can be seen in the diagram in Figure 1.2, the inductor current rises according to $i_L = L \cdot \int_{t0}^{t1} (v_{IN} - v_{OUT}) \cdot dt$. This leads to $\Delta I_L = L \cdot (V_{IN} - V_{OUT}) \cdot T_1$ because V_{IN} is constant and V_{OUT} can be approximated as constant. V_{OUT} must be nearly constant since by definition it is the aim of the DC-DC converter to produce a constant output voltage. In the second phase during T_2 the switch S_1 is now open but S_2 is closed instead. The inductor current falls and in steady state it reaches again the same value as at the beginning of the first phase. From this follows $\Delta I_L = L \cdot V_{OUT} \cdot T_2$. By equating the two presented formulas for the inductor current ripple the well known formula for the voltage conversion ratio can be found:

$$\frac{V_{OUT}}{V_{IN}} = \frac{T_1}{T_1 + T_2} \tag{1.1}$$

A somehow more intuitive explanation of the voltage conversion can be found by looking at the voltage at the switching node *sw* between the two switches S_1 and S_2. This waveform V_{SW} is depicted in Figure 1.2 and it has a rectangular shape. Interpreting the inductor L and the capacitor C as an ideal low pass filter makes the output voltage V_{OUT} just the average of the switching node voltage V_{SW}.

The main advantage of the inductor based DC-DC converter is its high achievable efficiency over a wide input voltage range. The major disadvantage on the other hand is the relatively high cost for the passive components. Especially the inductor is a significant cost factor. Additionally, often the large size of the inductor is not desirable. A detailed discussion on inductor based DC-DC converters of several types can be found e.g. in [2].

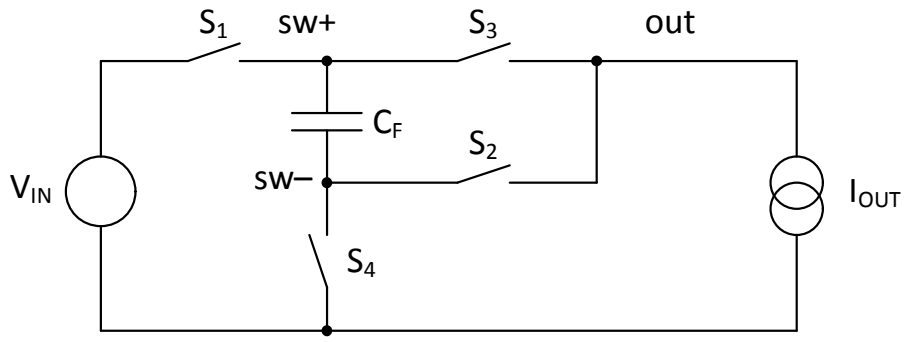

Figure 1.3: Example basic SC DC-DC 2:1 converter

1.1.2 Switched Capacitor DC-DC Converter

Opposed to the inductor based DC-DC converter in the switched capacitor (SC) DC-DC converter, the energy for the voltage conversion isn't transferred over an inductor but rather over one or more capacitors. In each switching cycle a certain charge is transferred over a capacitor from the input to the output, depending on the voltages and the capacitance value of the used capacitors. Therefore, SC DC-DC converters are often referred to as charge pumps. Similar to the inductor based DC-DC converter also these converters may generate an output voltage higher or lower than the input voltage. In Figure 1.3 a simplified example topology of a 2:1 step down SC DC-DC converter is shown. Again, the theoretical efficiency can be up to 100%. Unfortunately, the SC DC-DC converter has one significant constraint more to achieve the 100% even in theory. This constraint is the ideal voltage conversion ratio of input voltage to output voltage. The maximum conversion efficiency is given by:

$$\eta_{MAX} = \frac{V_{OUT}}{V_{IN} \cdot n} \tag{1.2}$$

where V_{OUT} is the output voltage, V_{IN} is the input voltage and n is the ideal voltage conversion ratio of the SC DC-DC converter [3]. The ideal voltage conversion ratio is determined by the topology. For the example given in Figure 1.3 it is 0.5. A detailed description of the SC DC-DC converter in Figure 1.3 is given in [4].

Assuming ideal switching, Figure 1.4 shows the voltages and currents in the SC DC-DC converter of Figure 1.3. Switches S_1 and S_2 are closed in the first half period of a clock cycle and switches S_3 and S_4 are closed during the second half period. During the first phase, when S_1 and S_2 are closed, the capacitor C_F gets charged, causing its voltage V_{CF} to rise while it gets discharged during the second phase, when S_3 and S_4 are closed.

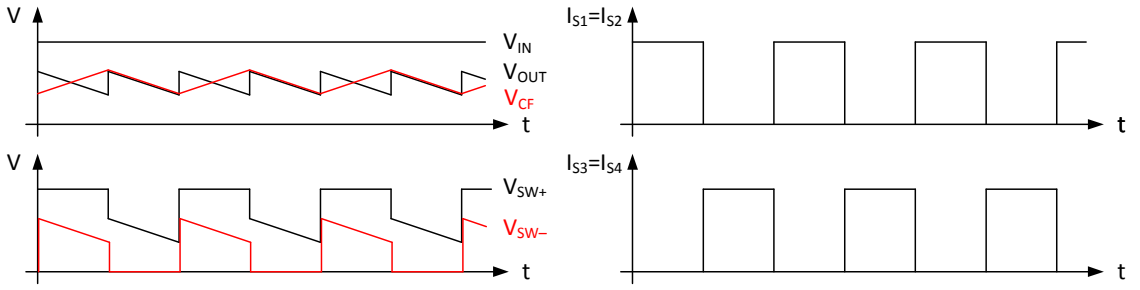

Figure 1.4: Voltages and currents in the SC DC-DC converter

One advantage of SC DC-DC converters is that for low load currents they can be fully integrated with reasonable area consumption in integrated circuits. State of the art fully integrated SC DC-DC converters can reach peak efficiencies of more than 80% for load currents in the 200mA range [5]. Commercially available SC DC-DC converters with external capacitors having a high efficiency of more than 80% can be easily found e.g. [6]. A detailed discussion on SC DC-DC converters can be found e.g. in [7].

1.1.3 Linear Voltage Regulator

Linear voltage regulators (LVRs) are widely used components in power management circuits. The main advantage of LVRs is their relative simple structure compared to the switching mode power supplies (SMPS) discussed before. A single transistor as pass device and an error amplifier is basically enough. There is no need for a clock or additional switches. There are several possibilities to distinguish between different linear voltage regulator topologies. Three criterions shall be mentioned here: firstly, the location of the pass device i.e. in series or parallel to the load. The large majority of the linear voltage regulators are series regulators. In this topology a pass device is in series to the load and it can be interpreted as a resistive voltage divider with the load in respect of the supply voltage as illustrated in Figure 1.5a.

The pass device can be any type of transistor like a bipolar junction transistor (BJT), junction field effect transistor (JFET) or MOS transistor. An error amplifier regulates the voltage drop over the pass device in order to keep the output voltage constant. The maximum achievable efficiency of such a series regulator is only defined by the voltage ratio of input and output.

$$\eta_{MAX} = \frac{V_{OUT}}{V_{IN}} \tag{1.3}$$

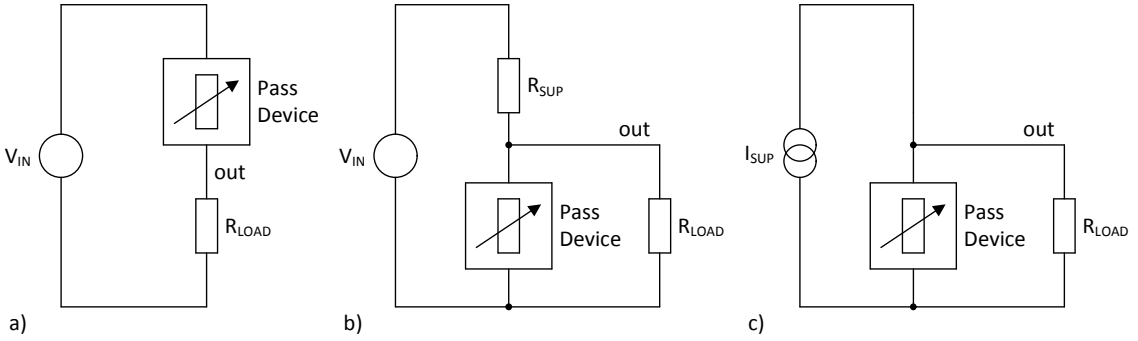

Figure 1.5: LVR topologies: a) series regulator; b) and c) shunt regulator

Of course the energy efficiency of the linear voltage regulator is degraded by its own power consumption leading to

$$\eta = \frac{V_{OUT} \cdot I_L}{V_{IN} \cdot (I_L + I_Q)} \tag{1.4}$$

where I_L is the load current and I_Q the current consumed by the regulator. Therefore, the current efficiency has been introduced that can be optimized by design

$$\eta_I = \frac{I_L}{I_L + I_Q}. \tag{1.5}$$

Linear voltage regulators where the pass device is parallel to the load are referred to as shunt regulators. Figures 1.5b and 1.5c show such an example. They are by far not as often used as series regulators but they shall be mentioned here for the sake of completeness. Analog to the voltage divider behavior of the series regulator, the shunt regulator behaves as a current divider between the load and the pass device. They are especially useful when the supply is a current source or has high impedance. The output voltage is kept constant by controlling the current through and therefore the voltage drop over the supply resistor R_{SUP}. In the following only the series regulator will be discussed further.

The second criterion is the polarity of the pass device i.e. NMOS Figure 1.6a or PMOS Figure 1.6b in a CMOS circuit. This property is critical for the error amplifier since a NMOS pass device acts as a source follower with gain slightly less than 0dB and non inverting behavior. On the other hand a PMOS pass device can have significant gain and has 180° phase shift from the gate to the regulator output.

The third criterion is not as sharply defined as the previous two. It is the so called low dropout capability. The dropout voltage is the voltage drop over the pass device at which the output voltage can't be sustained when decreasing the input voltage further [8]. The dropout voltage is typically measured at the maximum load current when the

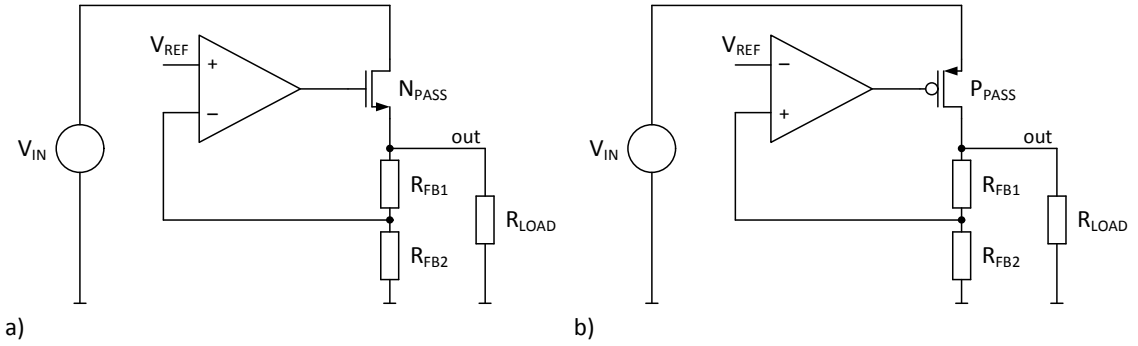

Figure 1.6: LVR topologies: a) NMOS regulator; b) PMOS regulator

output voltage has dropped by a certain percentage (e.g. 10%) of its nominal value due to decreasing the input voltage. When the dropout voltage of a linear voltage regulator is low then it is called a low dropout linear voltage regulator or shortly LDO. The problem is the definition of "low". One possible definition of low dropout is that the dropout voltage is lower than the threshold voltage of a MOS. From that definition follows, that a NMOS pass device can't be used in an LDO as long as no auxiliary voltage is available (e.g. due to a charge pump). Low dropout capability is an important property in various applications since only LDOs can achieve high power efficiency as indicated by Equation 1.3. One of the main disadvantages of the linear voltage regulator is that its efficiency is limited by the input to output voltage ratio. This is often not only a limitation in terms of available power but more related to the dissipated heat. Opposed to the SMPS only step down operation is possible i.e. the output voltage can only be smaller than the input voltage.

1.1.4 Project PUMA

The acronym PUMA stands for "Power Management Solutions for Next Generation Mobile Applications". Detailed information can be found in the project report [9]. A short summary of the report follows: PUMA was a project carried out as a cooperation between Infineon Technologies Austria AG and the Institute of Electronics of the Graz University of Technology. It was partially funded by the FIT-IT program of the Austrian federal ministry for transport, innovation and technology (German: Bundesministerium für Verkehr, Innovation und Technologie – BMVIT). The project started in April 2008 and ended in December 2010. The aim of PUMA was the development of highly efficient on-chip power management solutions and the reduction of system costs by reducing the size or even eliminating the need for external components in a system. The main targeted sys-

tems in PUMA were handheld devices like mobile phones or personal digital assistants (PDA). The increasing features in such systems like internet access, music playing, game playing etc. for next generation devices gives challenges in maintaining or even prolonging the battery lifetime compared to existing battery powered devices. Additionally, the physical form factor of such devices should not increase but rather decrease. To address these challenges the main focus within PUMA was put on:

- Highly efficient DC-DC converters for SoC solutions
- Accurate modeling of the converter circuits including external components
- Fully integrated DC-DC converter
- Output capacitor-less linear voltage regulator
- Switched capacitor DC-DC converter

The contribution to PUMA described in the thesis obviously belongs to the item "Output capacitor-less linear voltage regulator".

1.1.5 Project HIPA3

The project "Highly Integrated Power Architectures for Automotive Applications" is abbreviated as HIPA3. Opposed to PUMA, HIPA3 was not publicly funded. Again it was a cooperation between Infineon Technologies Austria AG and the Institute of Electronics of the Graz University of Technology. This project started in January 2011 and ended in August 2012. As the project name indicates, it focuses on power management in automotive applications. The focus of HIPA3 on automotive applications compared to PUMA which focused on battery powered applications is also related to the carve out of the wireless business line of Infineon in 2010. Nevertheless, the main targets of both PUMA and HIPA3 are basically the same: highly efficient and highly integrated power management solutions. One of the main challenges is the design of robust circuits in the automotive environment. The two focus topics in HIPA3 are:

- Fast transient response capacitor-less linear voltage regulator
- System in Package (SiP) integration of passives for automotive DC-DC converters

The contribution to HIPA3 described in the thesis obviously belongs to the item "Fast transient response capacitor-less linear voltage regulator".

1.2 Scope of this Work

The scope of this work has been mainly defined by the requirements of the projects PUMA (section 1.1.4) and HIPA3 (section 1.1.5). In both projects there are workpackages dedicated to LVRs. For PUMA the LVRs need to deliver a nominal load current of 150mA. For HIPA3 the nominal load current is 200mA. All regulators are designed in a 65nm CMOS technology. The aim of this work is to investigate non standard LVR concepts. The focus is put on two topics. Firstly, a digital control loop for an LVR and secondly, an LVR without external output capacitor. As an initial step, existing solutions were analyzed. Then LVRs for the use cases defined in PUMA and HIPA3 were designed using a new concept. Finally, the LVRs were produced as test chips and characterized in the laboratory. The design, the results and the comparison with previously published works are discussed in chapter 2 (Research Results) of this thesis.

1.2.1 Why a Digitally Controlled Linear Voltage Regulator?

First of all it has to be clarified how the term "digital controller" or "digital compensator" is used in the context of this work. In this work it will be defined like in [10, chapter 1.1]. This means that the digital controller is fed with a sampled signal represented by a finite number of digits generated by an analog to digital converter (ADC). Similarly, the digital signal computed by the controller is then converted by a digital to analog converter (DAC) back into the analog domain.

Such digital circuits are typically built with synchronously clocked logic. Beside synchronous digital logic also asynchronous digital logic exists. The focus is put on synchronous logic due to its wide distribution in industry. Subsequently, tools for synthesis and automated place and route for synchronous digital logic are also widely available. Sometimes circuits using only logic gates like CMOS inverters are called digital circuits even though these logic gates are operated as analog amplifiers [11]. In this work the term digital controller is used for a compensator built with synchronously clocked digital logic.

Conventional linear voltage regulators are fully analog and therefore, they are a continuous time system. Using a digital compensator in an LVR can lead to a variety of benefits. A digital compensator can be designed by means of hardware description languages (HDL) like VHDL or Verilog. This allows easier implementation of complex linear or nonlinear control laws. The layout of the compensator can be automatically generated

within a digital design flow. Also a portation of the compensator to a different technology is easily possible since it is HDL code. Additionally, the compensator is not susceptible to temperature, supply voltage or process variations. Logic gates can replace large internal compensation capacitors used in analog compensators. This can decrease die area consumption. Also, programmable compensator coefficients are possible. One scenario could be to sell a regulator with a standard configuration that safely operates with limited performance but a wide load capacitor range. The customer can then decide for a certain capacitor and load optimized coefficients for the use case. A further possibility is to change the output voltage by changing directly the reference in the digital domain. Such changing of the output voltage during normal operation is often used in DC-DC converters supplying microcontrollers and is referred to as dynamic voltage scaling (DVS) [12].

Of course there are also challenges when implementing a digitally controlled LVR. Since the output voltage of the LVR is of course an analog signal there is the need for an ADC to feed the output voltage information to the digital compensator. To bring back the result of the compensator to the analog domain a DAC is necessary. These two components ADC and DAC increase the complexity of the LVR significantly. This is especially true when the LVR must have a fast response to disturbances. Traditionally, LVRs have a much faster response time compared to SMPS where digital controllers have been investigated and used for decades [13]. As a rule of thumb the sampling frequency of the ADC should be at least a factor of ten faster than the unity gain frequency (UGF) of the regulator [14, p. 525], [15, p. 326]. E.g. a regulator with a UGF of 1MHz should have a sampling rate of about 10MHz. Not only the complexity, but also the quiescent current of the LVR will be affected by ADC and DAC. In contrary to the digital compensator the ADC and DAC are not easily portable to other technologies.

1.2.2 Why a Capacitor-Less Linear Voltage Regulator?

Again, it must be clarified what capacitor-less means. Often the terms capacitor-free or cap-less are used instead of capacitor-less. In the context of this work capacitor-less means that there is no external output capacitor for an LVR. Of course there will always be a capacitance at the output of an LVR just like at any circuit node. This capacitance can be placed by intention or it could be parasitic. For LVRs supplying load currents in the range of 100mA, typical on-chip capacitances range from 10pF (parasitic) to 10nF. On-chip capacitances in the range of 10nF and higher are already quite area consuming

and therefore not economical with today's CMOS technologies. Capacitor-less LVRs are especially interesting for SoCs where no parasitics due to bonding, printed circuit board (PCB) or external capacitor are present. On the one hand in such SoCs, LVRs with very fast response times can be achieved. On the other hand the overall system costs can be reduced due to omitting the pin to the external capacitor and also the external capacitor itself. These advantages must not be outweighed by a higher quiescent current and area consumption.

Due to the lack of a large output capacitor one of the challenges for the designer of such a capacitor-less LVR is to guarantee that the current through the pass device can be changed fast enough to supply loads with steep load current slopes while keeping the output voltage in a certain tolerance band. Also the power supply rejection ratio (PSRR) is affected by the lack of a large output capacitor. In capacitor-less LVRs the error amplifier must control the PSRR actively over a wide frequency range.

1.3 Performance Characteristics

A summary about the performance characteristics used to compare linear voltage regulators in this work has been published in [16].

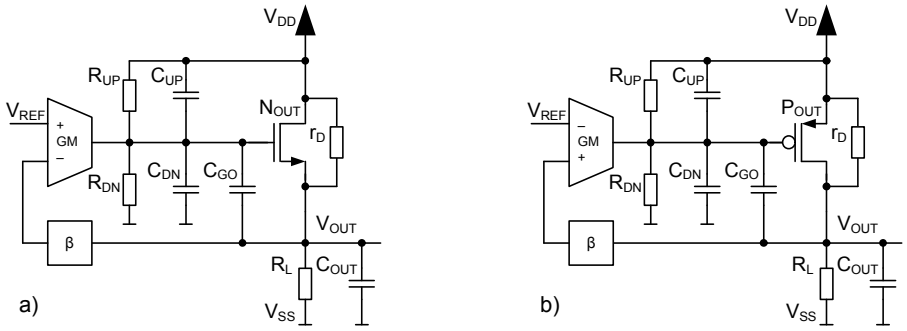

Figure 1.7: Basic structure of an LVR. a) NMOS pass device. b) PMOS pass device.

1.3.1 Stability

Of course a stable system is a prerequisite for any regulator. This subsection discusses which compensation schemes can be used to guarantee a stable regulator. Following, based on the simple LVR models in Figure 1.7, there are equations for basic performance characteristics derived in Table 1.1. The models are based on a single stage operational transconductance amplifier (OTA), a pass device N_{OUT} or P_{OUT}, an output capacitor C_{OUT}, a feedback divider with the divider ratio β and a load resistor R_L. The elements R_{UP}, C_{UP} and R_{DN}, C_{DN} represent the output impedance of the OTA with respect to VDD and VSS, respectively. R_D is the drain source resistance of the pass device and C_{GO} is the capacitance between the gate node of the pass device and the output of the LVR. The auxiliary variables R_{OTA} and C_{OTA} in Table 1.1 are the parallel connection of R_{UP}, C_{UP} and R_{DN}, C_{DN}, respectively, and R_{OUT} is the parallel connection of R_L and R_D.

For ensuring stability of the basic structures in Figure 1.7, five different topologies are meaningful. For building a stable system one of the four capacitors depicted is made large by intention. The remaining three capacitors are considered to be parasitic. For the NMOS regulator there are the two possibilities of generating the dominant pole with either the output capacitor (indicated by the symbol $C_{OUT} >>$ in Table 1.1) or with the load capacitor of the OTA (indicated by the symbol $C_{OTA} >>$ in Table 1.1). The same two possibilities exist for the PMOS regulator plus the Miller compensation by design-

Table 1.1: Equations for performance characteristics

		PMOS		NMOS	
Open Loop Gain	A_{DC} [dB]	$gm \cdot GM \cdot \beta \cdot R_{OUT} \cdot R_{OTA}$	(1a)	$GM \cdot \beta \cdot R_{OTA}$	(1b)
	ω_Z [rad/s]	$\frac{gm}{C_{GO}}\ (LHP)$	(2a)	$\frac{gm}{C_{GO}}\ (RHP)$	(2b)
	$UGF\ (C_{OUT} \gg)$ [rad/s]	$\frac{gm \cdot GM \cdot \beta \cdot R_{OTA}}{C_{OUT}}$			(3)
	$\omega_{ND}\ (C_{OUT} \gg)$ [rad/s]	$\frac{1}{(C_{OTA} + C_{GO}) \cdot R_{OTA}}$			(4)
	$UGF\ (C_{OTA} \gg)$ [rad/s]	$\frac{gm \cdot GM \cdot \beta \cdot R_{OUT}}{C_{OTA}}$	(5a)	$\frac{GM \cdot \beta}{C_{OTA}}$	(5b)
	$\omega_{ND}\ (C_{OTA} \gg)$ [rad/s]	$\frac{1}{C_{OUT} \cdot R_{OUT}}$	(6a)	$\frac{gm}{C_{OUT}}$	(6b)
	$UGF\ (C_{GO} \gg)$ [rad/s]	$\frac{GM \cdot \beta}{C_{GO}}$	(7)	–	
	$\omega_{ND}\ (C_{GO} \gg)$ [rad/s]	$\frac{gm}{C_{OUT}}$	(8)	–	
Z_{OUT}	Z_{OUT-DC} [Ω]	$\frac{1}{gm \cdot GM \cdot \beta \cdot R_{OTA}}$			(9)
	$Z_{OUT-MAX}\ (C_{OUT} \gg)$ [Ω]	Z_{OUT-DC}			(10)
	$\omega_{ZOUT-MAX}\ (C_{OUT} \gg)$ [rad/s]	$DC \ldots UGF$			(11)
	$Z_{OUT-MAX}\ (C_{OTA} \gg)$ [Ω]	R_{OUT}	(12a)	$\frac{1}{gm}\ //\ R_{OUT}$	(12b)
	$\omega_{ZOUT-MAX}\ (C_{OTA} \gg)$ [rad/s]	$UGF \ldots \omega_{ND}$			(13)
	$Z_{OUT-MAX}\ (C_{GO} \gg)$ [Ω]	$\frac{1}{gm}\ //\ R_{OUT}$	(14)	–	
	$\omega_{ZOUT-MAX}\ (C_{GO} \gg)$ [rad/s]	$UGF \ldots\ \omega_{ND}$	(15)	–	
PSRR	PSRR-DC [dB]	$gm \cdot GM \cdot \beta \cdot r_D \cdot R_{OTA}$			(16)
	PSRR-HF [dB]	$\frac{C_{GO} \cdot (C_{UP} + C_{DN} + C_{OUT}) + C_{OUT} \cdot (C_{UP} + C_{DN})}{C_{GO} \cdot C_{UP}}$			(17)
	PSRR zero	UGF			(18)
	dominant PSRR pole [rad/s]	$\frac{1}{R_{OTA} \cdot (gm \cdot r_D \cdot (C_{GO}+C_{DN}) + C_{UP})}$	(19a)	$\frac{1}{R_{OTA} \cdot (C_{GO}+C_{DN} + gm \cdot r_D \cdot C_{UP})}$	(19b)
	$PSRR_{MIN}\ (C_{OUT} \ll)$	$\frac{r_D + R_L}{r_D} \cdot \frac{C_{UP} + C_{DN} + gm \cdot r_D \cdot C_{GO}}{C_{UP} + gm \cdot r_D \cdot (C_{DN} + C_{GO})}$	(20a)	$gm \cdot r_D \cdot \frac{C_{UP} + C_{DN}}{gm \cdot r_D \cdot C_{UP} + C_{DN} + C_{GO}}$	(20b)

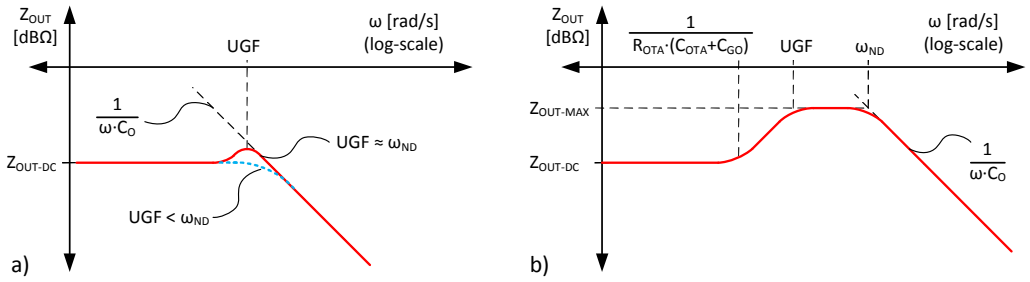

Figure 1.8: LVR output impedance: a) Dominant output pole b) Dominant internal pole

ing C_{GO} large (indicated by the symbol $C_{GO} >>$ in Table 1.1). This work focuses on LVRs with maximum load currents of more than 100mA. For such LVRs a typical output capacitor range is between 100nF and 100μF when generating the dominant pole at the output. If such an external output capacitor is replaced by an on-chip one, then the output capacitance will be restricted to a much smaller value. On-chip output capacitances are typically well below 10nF due the high cost of the die area occupied by this capacitance. Due to the much smaller on-chip output capacitance the pole at the output will move several decades to higher frequencies. The parasitic pole at the gate of the pass device can't move in the same range with reasonable current consumption. Therefore, for such output capacitor-less LVRs the pole at the gate of the pass device is made dominant.

1.3.2 Load Regulation

The load regulation of a voltage regulator describes how strong a change of the load current influences the output voltage. Ideally, a change of the load doesn't influence the output voltage at all. The load regulation can be subdivided into three different categories. Firstly, into static load regulation that describes how strong a DC load current change influences the output voltage. Secondly, into AC load regulation that is a small signal quantity and it reflects the frequency response of the output voltage on the load current. The AC load regulation is the small signal output impedance of the voltage regulator. Thirdly, there is the transient load response that represents the large signal time domain response of the regulator output voltage to a change of the load current. As can be seen from Equation (9) in Table 1.1 the low frequency output impedance or AC load regulation is inversely proportional to the voltage gain of the error amplifier and the transconductance of the pass device. Also the feedback divider ratio influences the output impedance. Figure 1.8 shows a qualitative frequency response of the output impedance of an LVR. On

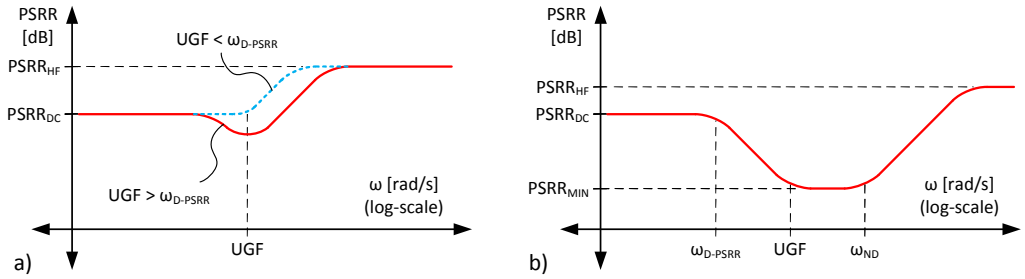

Figure 1.9: PSRR of an LVR. a) Dominant output pole. b) Dominant internal pole

the left hand side there is a plot for the LVR topologies with the dominant pole generated with the output capacitor and on the right hand side there is a plot for the LVR topologies with the dominant pole generated by the internal capacitances C_{OTA} or C_{GO}. The characteristic figures in this diagram can be found in Table 1.1 for all above mentioned LVR types. One observation that can be made in Figure 1.8 is that the LVR with dominant internal pole has an output impedance maximum in the range between the UGF and the non-dominant pole (output pole). Here the LVR with dominant output pole has a lower output impedance.

1.3.3 Line Response

The line regulation of a voltage regulator describes how strong a change of the supply voltage influences the output voltage. Ideally, a change of the supply voltage doesn't influence the output voltage at all. Also the line regulation can be subdivided into three categories. Firstly, into static line regulation that describes how a DC supply change influences the output voltage. Secondly, into AC line regulation that is a small signal quantity and it reflects the frequency response of the output voltage on the supply voltage. Often the power supply rejection (PSR) or alternatively power supply rejection ratio (PSRR) in datasheets refer to this AC line regulation. Thirdly, there is the transient line response, that describes the large signal time domain response of the regulator output voltage to a change of the supply voltage.

In [17] it has been shown that the differential to single ended conversion in the error amplifier of an LVR has a large impact on the PSRR. As a conclusion the active current mirror that performs the differential to single ended conversion should be of the same type as the pass device. This boundary condition was considered for the calculations in this chapter. From Equation (16) in Table 1.1 it can be seen that the low frequency PSRR is the

product of the intrinsic gain of the pass device, the voltage gain of the error amplifier and the feedback divider ratio. A qualitative frequency response of the PSRR is depicted in Figure 1.9. On the left hand side there is a plot for the LVR topologies with the dominant pole generated with the output capacitor and on the right hand side there is a plot for the LVR topologies with the dominant pole generated by the internal capacitances C_{OTA} or C_{GO}. The characteristic figures in this diagram can be found in Table 1.1 for all above mentioned LVR types. One observation that can be made in Figure 1.9 is that the LVR with dominant internal pole has a PSRR minimum in the range between the UGF and the non-dominant pole (output pole). Here the LVR with dominant output pole has a higher PSRR. Similar to the load regulation section also, the LVR with dominant output pole shows a more beneficial behavior here.

1.3.4 Costs

The cost contributors of an LVR can be separated into internal and external costs. External costs contain the costs of an external input capacitor, external output capacitor and indirect costs due to printed circuit board (PCB) complexity and PCB routing. Internal costs contain the costs for the silicon area occupied but also costs for the package due to used pins. By utilizing an output capacitor-less LVR, especially external costs for LVRs in a SoC can be minimized. In such a capacitor-less design not only the external capacitor can be saved but also the needed pin count, PCB area and PCB routing complexity can be reduced. From this point of view the capacitor-less LVR is more beneficial than the LVR with external capacitor.

Also the testability and the test time of an LVR need to be considered. The test time can contribute significantly to the overall costs. Therefore, easy and fast testing must be ensured. A long test time could be necessary e.g. if an LVR is only marginally stable with the parasitic elements of the tester because then the output voltage could take a long time to settle.

1.4 Related Work

This section deals with published work related to the topics discussed in this thesis. The related work is considered up to the time when the results discussed in this thesis were published for the first time in a paper. Here, existing concepts will be discussed, omitting detailed performance figures. The exact numbers will be compared in the relevant section later in chapter 2 of this thesis.

1.4.1 Digitally Controlled Linear Voltage Regulators

The results of the digitally controlled linear voltage regulator developed in this work were published in 2010 [18]. Not much related work was found until 2010. Only a few publications claim to have implemented a digitally controlled linear voltage regulator.

In 2005 there is a digitally controlled dynamic bias circuit in [19]. That actually means that the bias current of the analog error amplifier is set to two different current levels depending on the load current. A similar approach is used in [20] where knowledge about the system's current demand is used to adjust the bias current in order to optimize the quiescent current of the LDO.

In 2007 there is a digital control for a linear voltage regulator proposed in [21]. This linear voltage regulator has a push-pull output. It has a PMOS pass device between the supply and the output on the high side and an NMOS pass device between the output and ground on the low side. The pass devices are split into 16 parallel devices. Each gate of the split devices is connected to a cascade of CMOS inverters used as buffers. This section consisting of pass devices and inverter buffers is declared as DAC and supplies the load current to the output. This DAC is connected to an ADC and receives a 16 level thermometer code. The ADC consists of a resistor ladder with 16 comparators connected to the tabbing points of the ladder. The resistor ladder in the ADC is supplied by an error amplifier built up with CMOS inverters. Even though the error amplifier utilizes CMOS inverters it is still an analog error amplifier since these CMOS inverters are biased to operate at their trip point. Compared to the target of this thesis the linear voltage regulator in [21] has still an analog error amplifier and the digital part of the regulator is asynchronous. Since the digital part in [21] consists only of ADC and DAC it cannot of course be designed by means of a hardware description language (HDL) and automated place and route tools.

The most relevant work for this topic was presented at [22] in 2008. Unfortunately, not many details about the performance of the regulator are available. This regulator was implemented in a 130nm CMOS process and utilizes full digital control. That means it has an ADC, a digital compensator and a DAC. An 8 bit successive approximation register (SAR) ADC with 1.54MHz sampling frequency does analog to digital conversion of the output voltage. A digital PID controller running at 20MHz steers a 5 bit DAC. The pass device in this concept is an NMOS regulator.

Also [23] proposed an LDO with digitally controlled loop in 2008. This design utilizes two equivalent oscillators. A frequency difference between the two oscillators is generated by a voltage difference between the reference voltage and the output voltage of the LDO. A phase-frequency detector generates a control signal for a charge pump followed by a loop filter. The output of the loop filter is the gate voltage of the pass device. This is more or less the same concept as in a basic charge pump phase locked loop (PLL) [24, p. 556]. Therefore, this isn't considered to be a classical digital circuit either.

Another publication in 2008 that claimed to have an LDO with digital error amplifier is [11]. The error amplifier is based on CMOS inverters followed by an OTA as differential to single ended converter. But all inverters are biased in an operating point to act as analog amplifier. This means the design is still fully analog.

1.4.2 Capacitor-Less Linear Voltage Regulators

The results of the first capacitor-less linear voltage regulator developed within this thesis have been published in 2010 [18] and in 2011 [25]. The results of the second one have been published in 2012 [26]. Unlike the previous section about the digitally controlled linear voltage regulator there has already been much research done on capacitor-less regulators. Therefore, only a small portion of the available publications can be discussed here. Many publications head towards a solution with ultra low quiescent current and leaving transient behavior as a secondary requirement. Here, mainly fast transient response regulators will be discussed since this is the main aim of the regulators in this thesis.

The fastest capacitor-less linear voltage regulator found in literature has been published as early as 2005 [27]. This PMOS regulator has been built in a 90nm CMOS technology and is supplied with 1.2V to generate 0.9V. One of the key elements in this circuit is to use so called voltage positioning. This means to generate ideally an output impedance of the regulator including load capacitor that behaves as an ohmic resistance. Therefore,

the regulator pole needs to be matched to the zero generated by the load capacitor and its equivalent series resistor (ESR). Additionally, the ESR needs to equal the DC output impedance of the regulator. As a consequence the DC load regulation is compromised by the load capacitor size and the regulator bandwidth if the mentioned resistive behavior of the overall system wants to be achieved. The results proposed show very fast transient load response with a test load jump of 0mA to 100mA within 100ps. However, this fast transient behavior is paid with a high quiescent current of 6mA for a 100mA regulator.

One example of a low quiescent current capacitor-less linear voltage regulator was published in 2006 [28]. This regulator is designed for a maximum load current of 240mA while consuming only 3μA in no load condition. It uses a load current feedback loop to adaptively bias the error amplifier. The regulator is implemented in a 0.35μm technology and it has been tested with a moderately fast load jump of 1mA to 150mA within approximately 1.5μs.

An interesting concept named single transistor control LDO has been published in 2008 [29]. Excluding the PMOS pass device, there is only one active transistor in the feedback loop. Although this 0.35μm LDO hasn't got ultra fast transient response, its idea is quite nice. The test load jump for this circuit is 0mA to 50mA within approximately 300ns. Unfortunately, this concept works only for a limited supply voltage range. The voltage difference between supply and output voltage mustn't exceed a certain load dependent maximum.

In 2010 [30] proposes an add-on to a well known PMOS LDO topology. In the proposed topology a replica biasing concept is used to generate a process and temperature dependent auxiliary reference voltage derived from a constant reference voltage. It is implemented in a 0.35μm CMOS technology. The biasing circuit is enhanced with a high pass filter connected to the output to detect fast output voltage deviations. If the output voltage changes quickly due to a large load current jump, then the bias current is increased in order to increase the slew rate at the gate of the pass device. The idea is to have low bias current in steady state and increase the bias during output voltage disturbances. One disadvantage of this topology is that the bias current is due to the high pass filter also dependent on power supply noise. The test load has a moderately fast slope with a jump from 1mA to 100mA in 1μs.

Another publication in 2010 proposes a slew rate enhancement technique [31]. The key idea is to use an additional capacitively coupled feedback path that is off in steady

state. A fast undershoot of the output voltage triggers this capacitvely coupled feedback path and quickly discharges the gate of the PMOS pass device. Therefore, the slew rate is much higher compared to the steady state error amplifier. This linear voltage regulator is implemented in a 0.35μm CMOS technology. The design shows a low quiescent current of 20μA and it is tested with fast load current jumps of 0mA to 100mA in 100ns.

Later in 2010 a further improvement of the basic topology utilized in [30] has been proposed in [32]. An additional gain stage improves the static load and line regulation and additionally relaxes the slew rate problem for discharging the gate of the PMOS pass device. Therefore, the output voltage spike detection that increases the bias current is only necessary in one direction, which is for charging the gate of the PMOS pass device. Subsequently, no extra sensitivity of the bias current to the supply is added opposed to [30]. This LDO is implemented in a 90nm CMOS technology limiting the supply voltage to 1.2V. Even though the LDO consumes a very low quiescent current of 8μA it can react to fast load jumps like 3mA to 100mA in 100ns. One disadvantage of this LDO is that a minimum load current in the range of 1mA to 3mA is necessary to guarantee stability.

A modified version of the LVR in [31] has been published in 2011 in [33]. It uses the same basic topology but reduces the internal capacitances needed for stability. Again it is implemented in a 0.35μm CMOS technology and it is tested with a load current jump from 0mA to 100mA in 250ns.

In 2012 a differential common gate amplifier based linear voltage regulator with dynamic biasing has been proposed in [34]. The proposed error amplifier allows a push/pull behavior where the charge and discharge current of the PMOS pass device is not limited by the biasing current. Therefore, the slew rate at the gate of the pass device is improved. This design allows a low quiescent current of 7μA. It is implemented in a 0.35μm CMOS technology and tested with a load current jump from 50μA to 100mA in 500ns.

2 Research Results

2.1 Digitally Controlled Linear Voltage Regulator

A summary of the digitally controlled linear voltage regulator (LVR) presented in this section has been published in [18] and received the Best Student Paper Award of the IEEE International Conference on Electronics, Circuits and Systems. In [35] the current limitation has been discussed.

2.1.1 Design Targets

In this section the feasibility of a digitally controlled LVR will be shown. Unlike conventional LVRs this LVR has a digital compensator instead of an analog error amplifier like an operational amplifier or operational transconductance amplifier. Here the term digital means discrete in time and discrete in value. Furthermore, a synchronous digital design is produced. This allows the use of standard semi custom design flow tools like a hardware description language and automated place and route tools. Because the output voltage is an analog quantity also an analog to digital converter (ADC) and a digital to analog converter (DAC) are needed in the control loop. The LVR is implemented in a 65nm digital CMOS process. Due to the deep sub-micron process the digital compensator can be kept small in area. The LVR is assumed to be part of a Li-ion battery powered mobile phone system on chip (SoC) and shall generate an output voltage of 2.87V for external circuits. Because the battery voltage can go below 3V low dropout capability is essential in this application. I.e. the LVR is a low dropout LVR (LDO). The LDO is designed for a nominal load of 150mA with an external buffer capacitor of 470nF. Also an algorithm for output current limitation is included in the digital compensator. The core voltage for the 65nm transistors is 1.2V. Therefore, a 1.2V domain is necessary to supply the digital core of the LDO. The 1.2V LVR is not part of the digital LDO but it is assumed to exist on the SoC.

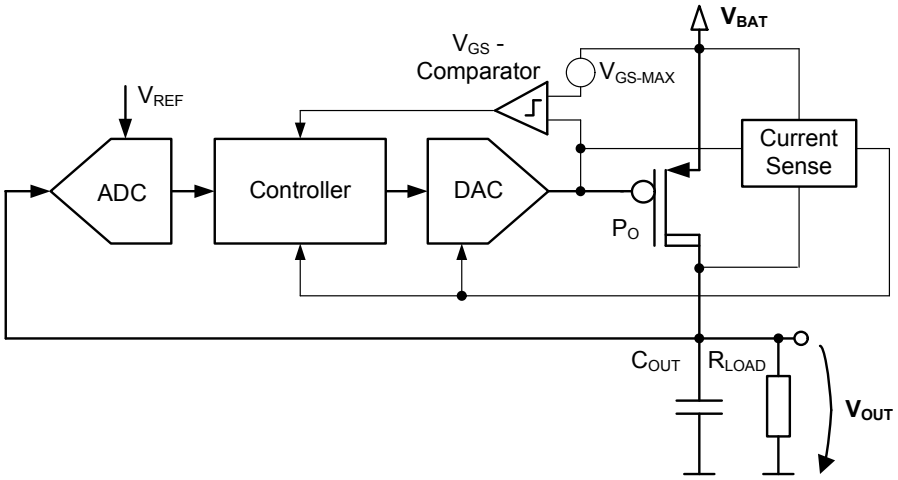

Figure 2.1: Functional block diagram of the digitally controlled LDO

2.1.2 Circuit Description

A block diagram of the digitally controlled LDO is depicted in Figure 2.1. It consists of six major parts: the PMOS pass device P_O, the current sensing circuit, the ADC, the DAC the digital controller and the gate-source over voltage comparator. These components will be discussed in more detail after a short system description.

The ADC senses the output voltage and converts it into a digital signal. The digital controller is fed with this digital output voltage information and calculates the digital actuating signal. The DAC converts the digital actuating signal into a current that charges the gate of the pass device P_O. This in turn changes the gate source voltage of the pass device and subsequently its drain current. The new drain current corrects the output voltage on the load resistor R_{LOAD} and the load capacitor C_{OUT}. The effective clock frequency of the controller, the ADC and DAC is 8MHz. This clock frequency is derived from a 104MHz master clock. Several phase shifted 8MHz clocks are derived for synchronization purposes. The dependency of the derived synchronization signals on the main clock can be seen in Figure 2.8. Not only the output voltage is converted into the digital domain. Also the output current is measured and converted into the digital domain. The current level is used to determine the operating point of the pass device. This information is used to adopt the regulator coefficients in the digital controller in order to keep the transfer function, especially the unity gain frequency of the system in a certain range. An auxiliary regulator that is not part of the design generates V_{CORE}, the 1.2V core domain for supplying the controller. Also a band gap reference that is not part of this work is placed

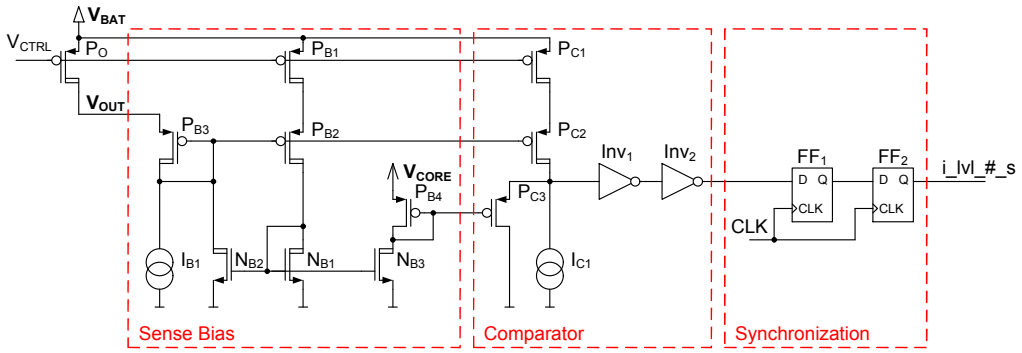

Figure 2.2: Schematic of the current sensing circuit

on the test chip. For debugging purposes the internal reference voltage and bias currents can be alternatively forced externally. A digital interface is also part of the test chip for debugging the digital controller.

Current sensing circuit

A detailed schematic of the utilized current sensing circuit and the current comparator can be seen in Figure 2.2. P_O is the pass device of the LDO and P_{B1} and P_{C1} are replica devices of the pass device. Because these transistors are operated at the battery supply voltage that can be up to 5V these are drain extension MOS (DEMOS) transistors. Transistors P_{B2} and P_{C2} are cascoding devices to ensure that the drain source voltage of the replica devices is the same as for the pass device. This allows considering the finite output resistance of the pass device in the output current. The transistor P_{B3} senses the output voltage of the LDO to generate the gate voltage for the cascodes P_{B2} and P_{C2}. The current through P_{B3} tracks the output current due to the current mirror built by N_{B1} and N_{B2}. This is necessary because otherwise the gate source voltage of P_{B3} would be constant. But the gate source voltage of the cascodes P_{B2} and P_{C2} depend on the actual current through the replica devices P_{B1} and P_{C1}, respectively and subsequently on the output current. Finally, the drain source voltage of the replica devices P_{B1} and P_{C1} would not track the drain source voltage of the pass device if the current through P_{B3} would be constant. The current comparator block in Figure 2.2 consists of the replica of the pass device P_{C1}, the cascode of the replica device P_{C2}, the current source I_{C1} that defines the comparator threshold, the two inverters Inv_1 and Inv_2 acting as amplifier and the voltage clamp P_{C3}. As long as the current through P_{C1} is less than the threshold current of I_{C1} the output of the comparator stage will be logic low. If the current through P_{C1} approaches the threshold current, then

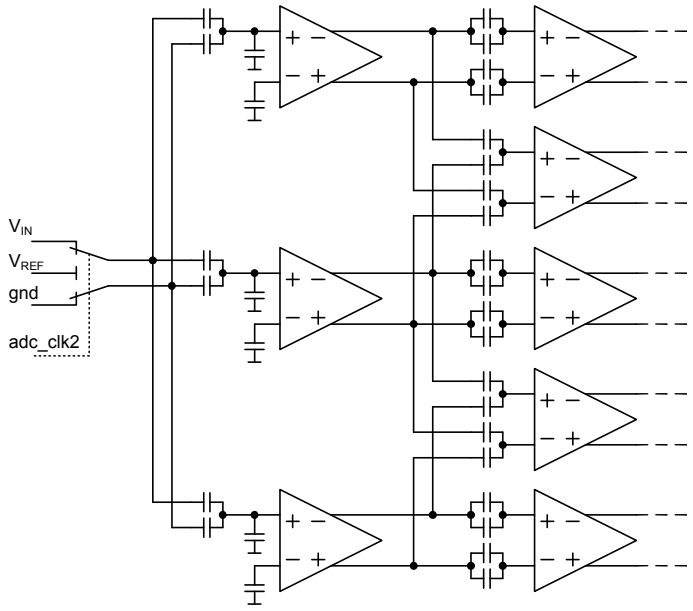

Figure 2.3: Schematic of the first two ADC stages

the node voltage at the drain of P_{C2} will rise until the output of the comparator will go to logic high. If the current through P_{C1} rises further, then the node voltage at the drain of P_{C2} would approach the supply voltage V_{BAT}. Therefore, the clamping transistor P_{C3} limits this node voltage to the core supply voltage of 1.2V.

ADC

The ADC utilized in the proposed digitally controlled LDO is a capacitive interpolation flash ADC. The architecture of the chosen ADC is described in [36]. Figure 2.3 shows a simplified diagram of the ADC. The ADC design has also been taken from an existing project. In the present work only the input voltage range, the quantization steps and the conversion rate have been modified.

The ADC is designed to consume low power i.e. less than 100μA. To keep the power consumption low a digital resolution of only 4 bit was chosen. For having still a high voltage resolution two methods have been applied. Firstly, the voltage window around the center voltage of the ADC is set to $\pm$ 57mV which is less than the allowed output voltage deviation of the LDO. The voltage window is designed so small because there is no need to convert a voltage signal into the digital domain that must not be present during normal operation. And secondly, a nonlinear quantization scheme is used. That means the quantization steps near the set point of the output voltage are small and the

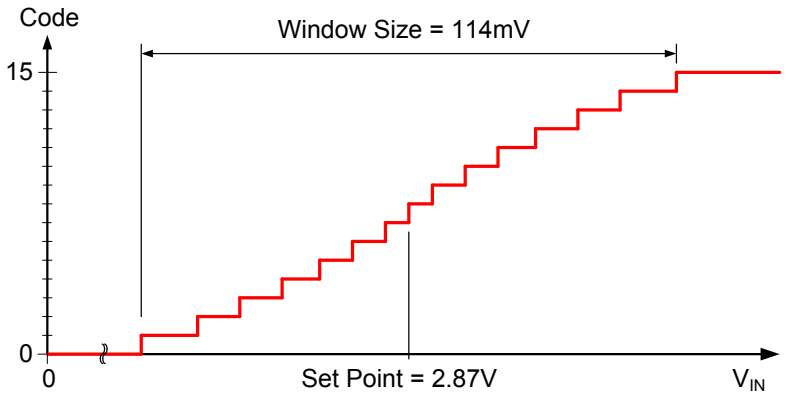

Figure 2.4: Transfer curve of the 4 bit ADC including 0.5 LSB offset

quantization steps at the border of the voltage conversion window are large. The idea behind this is the following: If the output voltage of the LDO is at its set point, small deviations from the output voltage should be recognized to keep the output voltage ripple low. If the output voltage of the LDO is already farther away from its set point, then the exact value of the deviation is not so important as long as the voltage regulation works and brings the output voltage back to its set point. This results in a slightly "S"-shaped transfer curve of the ADC as depicted in Figure 2.4. Furthermore, a constant of 0.5 least significant bits (LSB) is added to the ADC output. This prevents a zero-error output signal between two conversion levels and always forces an error signal of at least 0.5 LSB. Therefore, in steady state the output voltage will toggle around the set point and the ripple at the output voltage can be less than one LSB [37]. The 4 bit value of the measured voltage signal is interpolated inside the digital controller to a 7 bit signed integer value. This interpolation does also a conversion of the ADC's regressive nonlinear quantization scheme ("S"-shaped transfer curve) to a progressive nonlinear transfer curve. This makes the regulator more aggressive for high deviations of the output voltage from its set point.

DAC

In the digitally controlled LDO there is a 10 bit DAC implemented. It is a simple binary weighted charge pump DAC and its schematic is depicted in Figure 2.5. The two LSBs are realized by stacking four and two unit transistors, respectively. The remaining seven bits are realized by putting multiple unit transistors in parallel. This gives a current mirror bank with current paths that provide powers of two times the bias current. I.e. $I_O = I_B \cdot 2^n$ with $n = -2...6$. This current mirror bank is implemented with PMOS

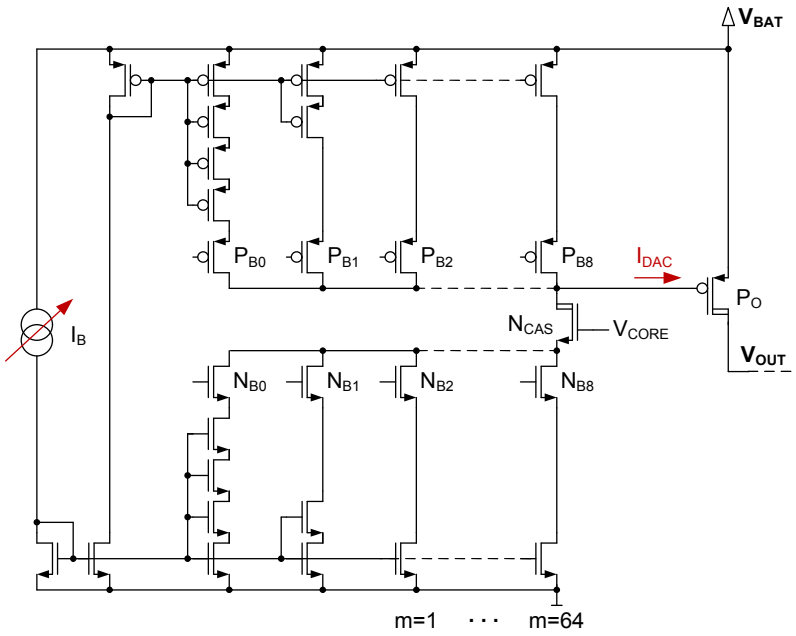

Figure 2.5: Schematic of the DAC

transistors for a positive output current and with NMOS transistors for a negative output current of the DAC. The tenth bit controls the sign of the output current. The control transistors P_{B0} thru P_{B8} connect the paths of the correspondingly weighted positive currents to the output of the DAC, and the control transistors N_{B0} thru N_{B8} connect the paths of the correspondingly weighted negative currents to the output of the DAC. All these transistors are core transistors with a rated supply voltage of 1.2V. The output of the DAC is connected to the gate of the pass device P_O. The gate source voltage of P_O is also rated for the core voltage of 1.2V, therefore the transistors of the PMOS current mirror bank in the DAC can be connected directly to the output of the DAC. The gate source voltage comparator indicated in Figure 2.1 allows the digital controller to guarantee that a maximum gate source voltage of the pass device (and subsequently a maximum drain source voltage for the PMOS current mirror bank in the DAC) is not exceeded. Therefore, the output voltage of the DAC referred to ground will always be higher than the rated core voltage. This high DAC output voltage requires the shielding transistor N_{CAS} that protects the transistors in the NMOS current mirror bank. The DAC has an integrating behavior in the control loop because the output of the DAC has a current source characteristic and the load of the DAC is the gate capacitance of the pass device P_O. An important feature of the DAC is that its gain can be adjusted asynchronously. This is realized by adjusting the bias current as indicated in Figure 2.5. Therefore, the gain of the control loop can

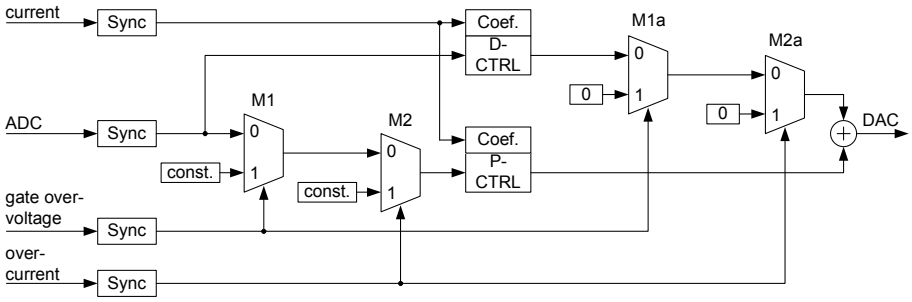

Figure 2.6: Control path of the controller

be changed significantly faster than in one clock cycle of the digital controller. A similar gain adaption technique is used in [19]. To keep the DAC design simple, the gain can only be changed in a small range. The ratio of the maximum gain to the minimum gain equals $\Delta k_{\text{DAC\_MAX}} = \frac{k_{\text{DAC\_4}}}{k_{\text{DAC\_0}}} = \Delta k_1 \cdot \Delta k_2 \cdot \Delta k_3 \cdot \Delta k_4 = 5$. Each of the four output current comparator thresholds increases the DAC gain by approximately the same amount i.e.

$$\Delta k \stackrel{!}{=} \sqrt[4]{\prod_{i=1}^{4} \Delta k_i} = \sqrt[4]{5} \approx 1.5 \tag{2.1}$$

Controller

Due to the synchronous design of the digital controller standard tools for a digital design flow can be used. The controller is implemented in VHDL. The main part of the overall digital controller is the digital error amplifier. The digital error amplifier is a proportional derivative (PD) controller and not a standard proportional integrative derivative (PID) controller like in [22]. A quasi integrating behavior is still present in the control loop due to the high ohmic current output of the DAC connected to the gate capacitance of the pass device P_O. Equation 2.2 defines the control law of the implemented PD controller:

$$G_{\text{PD}}(z) = \frac{(k_{\text{P}} + k_{\text{D}}) \cdot z - k_{\text{D}}}{z} \tag{2.2}$$

where k_P stands for the coefficient of the proportional part and k_D stands for the coefficient of the derivative part of the controller. There is an individual set of coefficients for each of the five output current regions of the LDO. All coefficients are 6 bit signed integer values. Together with the multiplication with the 7 bit signed integer error signal and the summation of the proportional and derivative part this gives a 13 bit signed integer as an internal actuating variable. This internal actuating variable is limited to a 10 bit value to

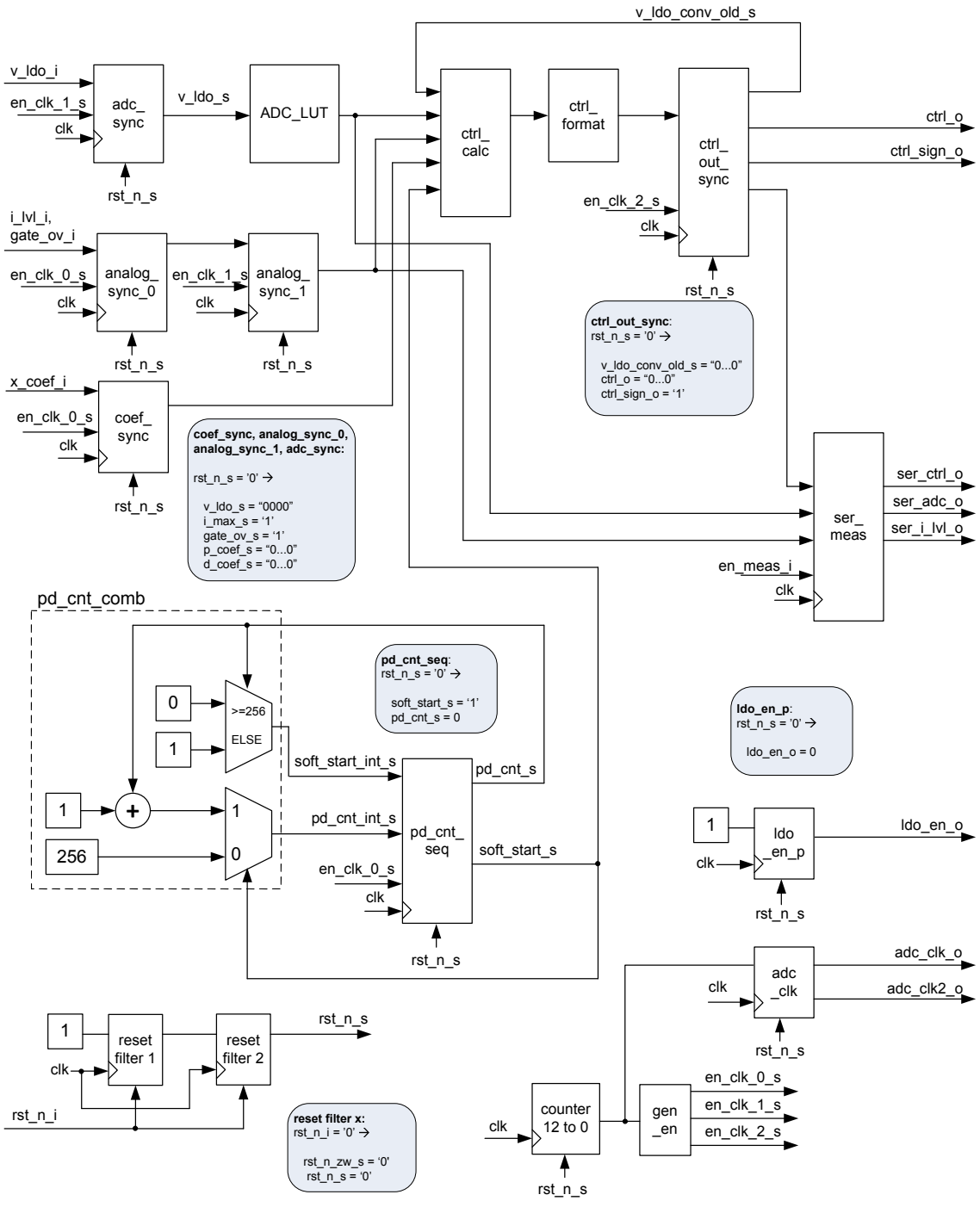

Figure 2.7: Detailed diagram of the digital controller

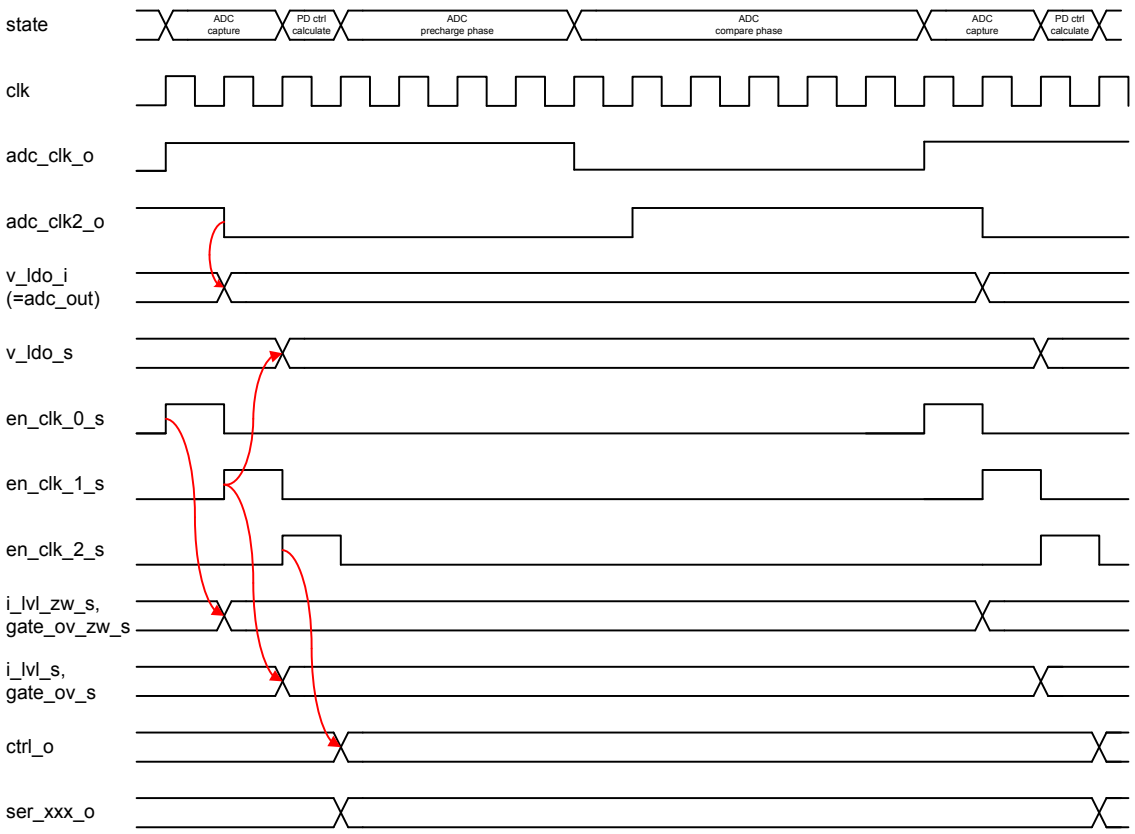

Figure 2.8: Timing diagram of the digital controller

drive the DAC. Figure 2.6 shows a simplified diagram of the digital controller. The PD controller is split into separate P-part and D-part due to the way how the voltage control loop is opened during over current and gate over voltage mode.

The full diagram of the digital controller including its auxiliary functions is depicted in Figure 2.7. All blocks without "clk" input contain combinational logic only. It can be seen that all input signals are synchronized before used in any digital function. Only the signal "rst_n_i" can trigger the reset asynchronously but it is released synchronously through the reset filters 1 and 2. After the synchronous reset has been released the analog part of the LDO is enabled with the signal "ldo_en_o". The soft start functionality, which is explained later in more detail, uses a counter that starts after a reset has been released and keeps the soft start signal "soft_start_s" high for a predefined amount of time. The master clock of the digital controller is 104MHz, but all operations are performed at a rate of 8MHz. The master clock is used to derive the 8MHz control signals "en_clk_x_s" and the ADC clocks "adc_clk_o" and "adc_clk2_o". The timing diagram of the digital controller is depicted in Figure 2.8 and shows the sequence of the internal signals. The

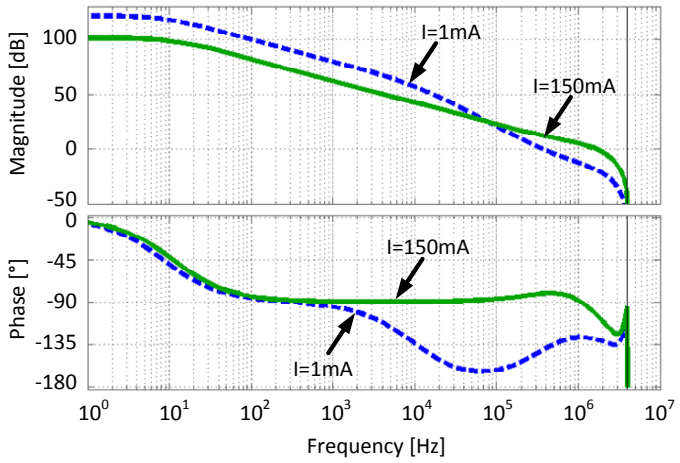

Figure 2.9: Bode diagram of the digital LDO for 1mA and 150mA load current

digital actuating variable is split into a 9 bit unsigned integer signal "ctrl_o" and the sign of the actuating variable "ctrl_sign_o". Finally, for debugging purposes the values of the digital actuating variable, the ADC output and the output current level can be transmitted on a serial output pin by setting the signal "en_meas_i" to high.

A model for the digitally controlled LDO was implemented in MATLAB. In this model the analog part i.e. the pass device and the load is described by continuous time equations while the digital part i.e. ADC, DAC and controller is described by discrete time equations. As mentioned above, there is a dedicated set of compensator parameters for each of the five output current operating ranges. The current comparator levels are set to 15mA, 33mA, 64mA and 117mA. A Bode diagram for a low load of 1mA and the full load of 150mA is depicted in Figure 2.9. For 1mA load current the phase margin is 40° and for 150mA load current the phase margin is 77°. The vertical line at 4MHz in the Bode diagram shows the Nyquist frequency of the sampled system.

Digital Current Limitation

Figure 2.6 shows the signal paths in the digital controller. In normal operation the signals "gate over-voltage" and "over-current" are low and the output of the DAC that drives the pass device P_O is determined by the digitized LDO output voltage provided by the ADC. However, if the output current limit is exceeded the signal "over-current" goes to high and the LDO goes into current limitation mode. In this mode the LDO behaves like a current source and the output voltage will break down. The blocks in the voltage control path labeled P-CTRL and D-CTRL will try to increase the output voltage again. But as

can be seen from Figure 2.6 the over-current signal disconnects the output of the voltage controller from the output of the overall controller through the multiplexers M2 and M2a. As explained before, the voltage controller is a PD controller. That means there is no integrative behavior in the voltage controller. This simplifies the design of the current limitation feature. If there was an integrative part in the voltage controller, the integrator output could run away, while the voltage control loop is opened in current limitation mode. In that case other counter measures would be necessary to avoid a large voltage overshoot after the transition from current limitation mode back to normal operation mode.

In the LDO there are five current threshold levels recognized. These current signals are converted into the digital domain by means of five current comparators. To reduce the probability of metastabilities in the digital circuit the comparator signals need to be synchronized. In the proposed LDO there are two synchronization stages utilized. The timing diagram in Figure 2.8 illustrates the synchronization scheme. The asynchronous output of the comparator is read by the first synchronization stage to the signal bus i_lvl_zw_s and in the second synchronization stage to the signal bus i_lvl_s, where the signal buses i_lvl_zw_s and i_lvl_s are thermometer coded and have a width of five bits. To reduce the delay caused by the synchronization, the synchronization stages are clocked with two phase shifted clocks. That means the effective delay for the current level signals is only two 104MHz clock cycles instead of two 8MHz clock cycles. Finally, the output of the controller is available three 104MHz clock ticks after the asynchronous signals have been sampled.

The working principle of the current limitation is quite simple but very effective. In case the current limit is exceeded the control signal "over-current" in Figure 2.6 (that corresponds to the fifth current comparator output) goes to high. Therefore, the output of the overall controller that drives the DAC is overwritten with a constant value that decreases the output current. The constant output of the controller is kept as long as the "over-current" signal is high. After the "over-current" signal goes to low the voltage controller takes over control and the LDO is in normal operation again. Due to the delay present in both the analog comparator and the digital controller, there will be a current ripple around the target value of the maximum output current.

Soft Start Mode

Also a soft start mode is implemented in the digitally controlled LDO. This soft start mode has two effects. Firstly, it limits the inrush current of the LDO. This is especially important in large systems with several LDOs. When such a large system is started up the load current of all subsystems is summed up at the main supply. Then either all subsystems need to start up consecutively or each subsystem has to have a current limitation. Secondly, there would be an output voltage overshoot at a start up with no load similar to a negative load current jump from maximum load to zero. Also, the soft start mode is simple in its implementation but effective. In the soft start mode the current limitation explained in the previous subsection is realized not with the highest level current comparator but with a lower level. If the soft start functionality is enabled, then a timer is started after enabling the LDO. After the timer overflow the original and higher current limit is activated. This means the current limit is simply reduced for a predefined amount of time after enabling the LDO. In the proposed LDO the current limit is set to 68mA for 32μs in the soft start mode.

Gate Source Over Voltage Comparator

The gate source over voltage comparator senses the gate source voltage of the pass device P_O and compares it with the maximum allowed gate source voltage of 1.2V. During normal operation this wouldn't be necessary and also the current limitation feature handles an overload condition at the output. But if the supply voltage of the digitally controlled LDO is too low (i.e. the LDO runs into dropout), the output voltage will not reach its set point and the controller would increase the gate source voltage of P_O over a destructive level. This can happen because P_O isn't a symmetric high voltage transistor but a DEMOS transistor that can only handle a high voltage across the drain and any other terminal but not across the gate and the source. In case the gate source voltage is too high, the controller stops normal operation and the voltage control loop is opened. Similar like in the over current mode a constant value that decreases the gate source voltage is applied to the DAC input by the digital controller. How the normal signal flow in the digital controller is interrupted by the "gate over voltage" signal can be seen again in Figure 2.6.

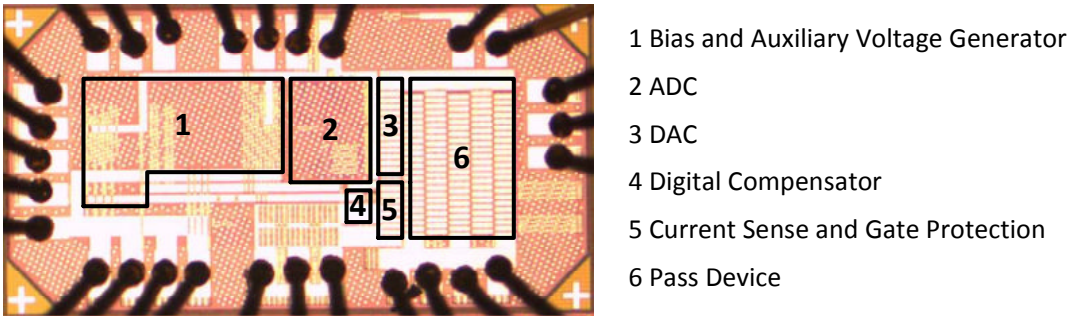

Figure 2.10: Die photograph of the digitally controlled LDO

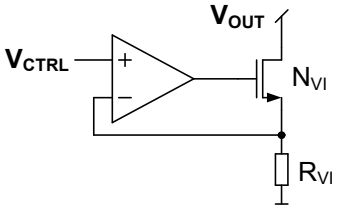

Figure 2.11: Load current sink

2.1.3 Measurement Results

A test chip of the digitally controlled LDO has been manufactured in a 65nm digital CMOS process. A photograph of the test chip die is depicted in Figure 2.10. The regulator consisting of pass device, digital controller, ADC, DAC, current sensing circuit and gate source over voltage comparator consumes 0.152mm^2. All measurements were done at nominal conditions, i. e. supply voltage V_{BAT}=4V, C_{OUT}=470nF and room temperature. For loading the LDO actively an external controllable current sink was used and for loading the LDO passively at the start up measurements standard resistors were used. A simplified schematic of the load current sink is depicted in Figure 2.11. The current depicted in the oscilloscope screen shots is always measured directly at the load. That means this current also includes the current provided by the buffer capacitor C_{OUT}.

An oscilloscope screen shot with a transient load response for the digitally controlled LDO can be seen in Figure 2.12. In this picture a load current jump from 1mA to 150mA and back to 1mA with a rise time and fall time of 1μs can be seen. The voltage undershoot is 53mV while the overshoot is 48mV. The unloaded DC output voltage is 2.85V that is 20mV or 0.7% below the nominal value of 2.87V. The measured power supply rejection ratio (PSRR) of the digitally controlled LDO can be seen in Figure 2.13. The PSRR of the unloaded LDO stays above 30dB in the whole measurement range up to 1MHz.

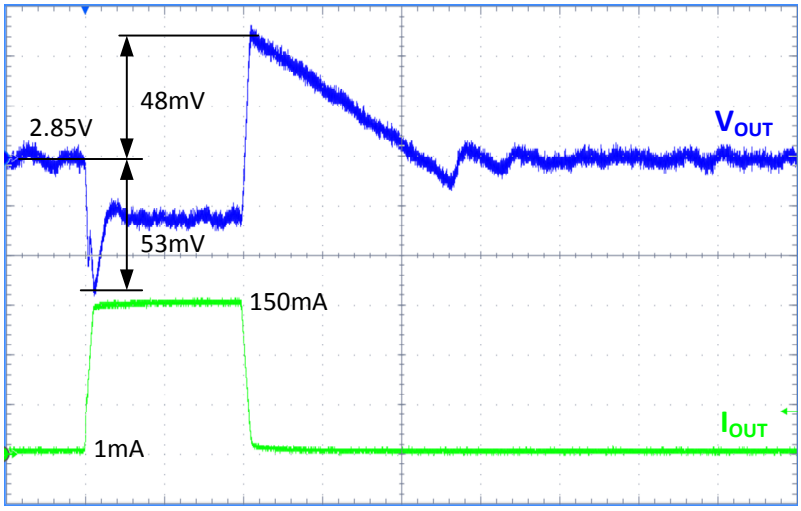

Figure 2.12: Transient load response; V_{OUT}: 20mV/div; I_{OUT}: 50mA/div; t: 10μs/div

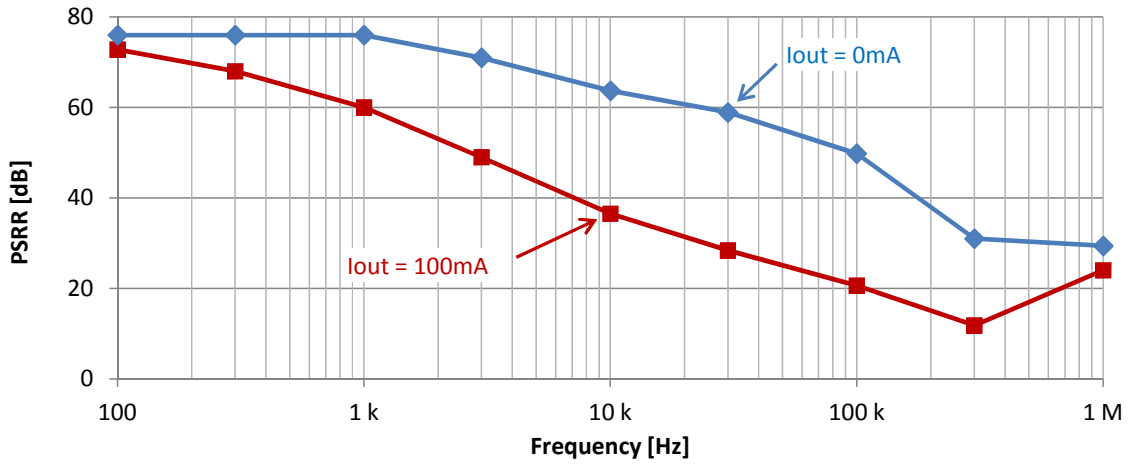

Figure 2.13: Measured PSRR of the digitally controlled LDO

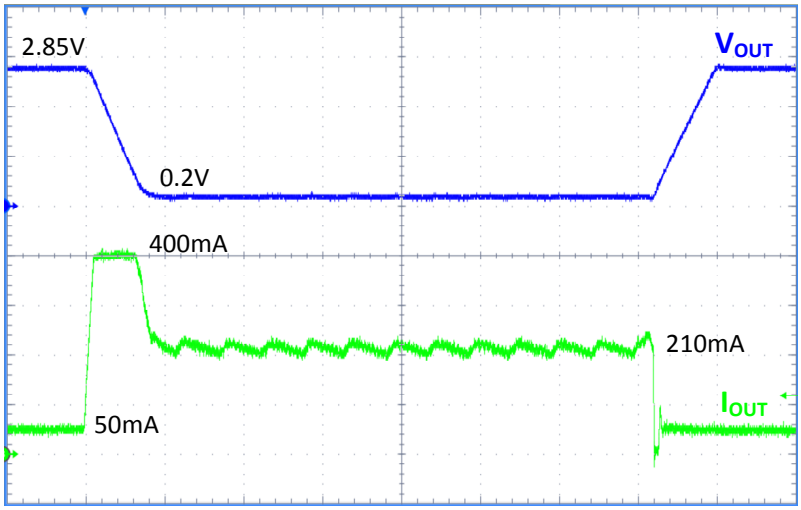

Figure 2.14: Over current response; V_{OUT}: 1V/div; I_{OUT}: 100mA/div; t: 10μs/div

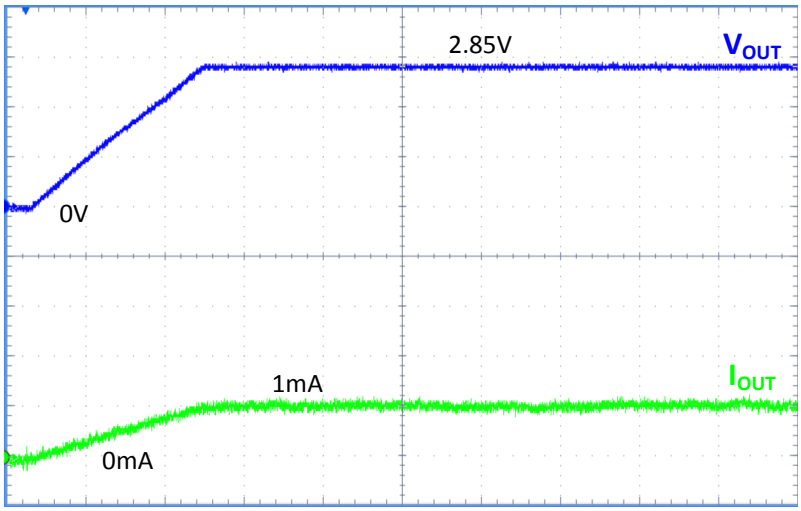

Figure 2.15: Start up with a load of 2700Ω; V_{OUT}: 1V/div; I_{OUT}: 1mA/div; t: 10μs/div

When loaded with 100mA the PSRR of the LDO reaches a minimum of 12dB at 300kHz. Figure 2.14 shows an oscilloscope screen shot of a transient overload event. The voltage controlled current source draws initially 50mA from the LDO output and jumps then to a target load current of 400mA. Because the output current of the LDO is limited to ∼210mA, the output capacitor is discharged with 400mA – 210mA = 190mA until the output voltage breaks down to 0.2V. Then the supply voltage for the external current sink is too low and it can't draw more current than supplied by the LDO. After the target value of the load current sink is set to 50mA again, the output capacitor is charged with 210mA – 50mA = 160mA and the output voltage rises again until it reaches its set point value of 2.85V. The normal start up with a high ohmic load is depicted in Figure 2.15. In this

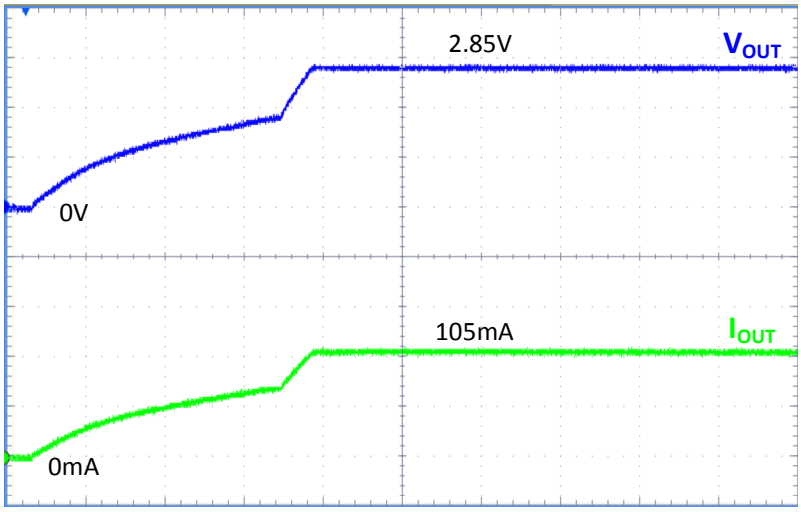

Figure 2.16: Start up with a load of 27Ω; V_{OUT}: 1V/div; I_{OUT}: 50mA/div; t: 10μs/div

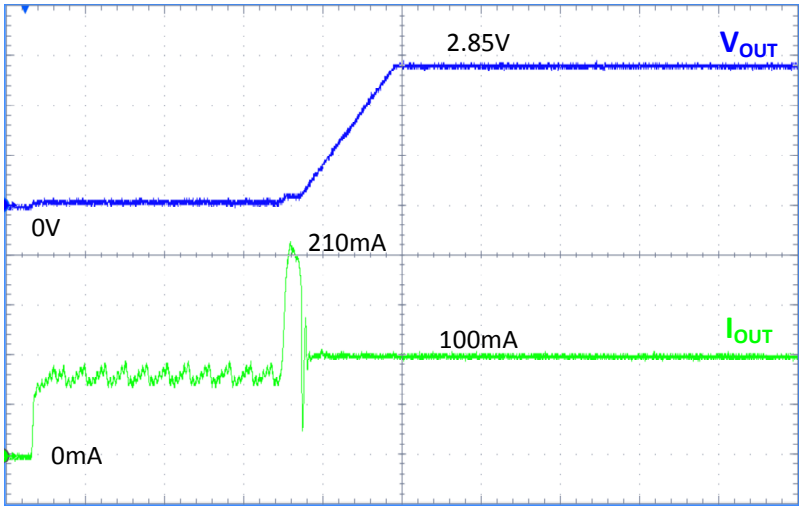

Figure 2.17: Start up with current sink load. V_{OUT}: 1V/div; I_{OUT}: 50mA/div; t: 10μs/div

case the load is a 2700Ω resistor and almost the whole output current of the LDO which is limited to ∼70mA during start up is used to charge the output capacitor. In Figure 2.16 a start up with a low ohmic load is shown. In this case the load is a 27Ω resistor and the set point of the LDO output voltage can't be reached with the start up current limit because

$$V_{\text{LOAD-MAX}} = I_{\text{START-UP}} \cdot R_{\text{LOAD}} \approx 70mA \cdot 27\Omega = 1.89V < 2.85V. \tag{2.3}$$

After 32μs the normal current limitation of ∼210mA is enabled again and the set point of 2.85V for the LDO output voltage can be reached. Finally, in Figure 2.17 at the same time the LDO is enabled, also the current sink is enabled with a target current that is above the start up current limit. The target value of the load current sink is set 100mA. As long as

Table 2.1: Summary of the static properties of the digitally controlled LDO

Process	65nm digital CMOS
Active area for regulator	0.152mm^2
Supply voltage	2.93V - 5.5V
Output voltage	2.85V
Load current	0mA - 200mA
Static load regulation	17μV/mA
Static line regulation	158μV/V
Current consumption	188μA

the start up current limitation of ∼70mA is active, the output voltage stays at almost 0V. Only after the LDO releases its normal current limit after 32μs the output capacitor can be charged with 210mA – 100mA = 110mA and the set point of the LDO output voltage can be reached. The short peak current after 32μs is caused by the finite speed of the control loop in the load current sink. As long as the output voltage is close to 0V, the load current sink isn't working in its specified operating range but it rather behaves as low ohmic resistor. During the short time the load current sink needs to settle to its target load value the high current limit of the LDO limits the load current to 210mA.

A summary of the static performance properties of the digitally controlled LDO can be found in Table 2.1.

2.1.4 Comparison with State of the Art

Few research works have been published in this field. Publications [11, 19, 21–23] claim to have implemented a digitally controlled linear voltage regulator. In [19] the control loop is still analog, only the bias current can be set dynamically to discrete values. In [11] the error amplifier is called digital, because only CMOS inverters are used. But actually these inverters are used as analog amplifiers. The LDO's error amplifier in [23] consists of two parallel current controlled oscillators, a phase detector and a charge pump, similar to a phase locked loop. The resulting system is discrete in time, but since the error signal is the phase difference of the oscillators, the error signal still is continuous in value. The system in [21] is quantized but still is continuous in time. In contrast, the work in this thesis focuses on the evaluation of a synchronously clocked digitally controlled LDO. The linear voltage regulator presented in the talk [22] also uses a synchronous design, but since it uses an NMOS output, it hasn't got low drop out capability. Measurement results for comparison are not available from [22]. Because no digitally controlled LDOs

Table 2.2: Comparison of the digitally controlled LDO with analog LDOs

Publication	[38]	[39]	This work
Year	2006	2006	2010
Process	0.35μm CMOS	130nm CMOS	65nm CMOS
V_{IN} [V]	2 - 5.5	3 - 4.5	2.93 - 5.5
V_{OUT} [V]	1.8	2.8	2.85
$I_{OUT\text{-}MAX}$ [mA]	200	150	200
I_Q [μA]	20	122	188
C_{LOAD} [μF]	1	1	0.47
Area [mm^2]	0.264	0.166	0.152
ΔV_{OUT} [mV]	54	15.8	53
$\Delta I/\Delta t$ [mA/μs]	0-200/0.1	0-150/2.5	1-150/1

are available for comparison, state of the art analog LDOs with similar specifications are used for a comparison in Table 2.2. The LDO in [38] has a worse transient load response, especially when the undershoot is normalized to the nominal output voltage. However, the load jump in [38] is more aggressive than the one in this work. Both LDOs in [38, 39] have a higher dropout voltage and consume more active area. From this comparison it can be clearly seen that a digitally controlled LDO can compete with state of the art analog LDOs and can additionally make use of the advantage of its digital implementation.

2.2 Capacitor-Less Linear Voltage Regulator

The circuit description of the linear voltage regulator (LVR) presented in this section has been published in [40]. A summary including measurement results of the regulator presented in this section has been published in [25].

2.2.1 Design Targets

In this section an output capacitor-less LVR is presented. The LVR is designed to supply a digital signal processor (DSP) where a nominal load current of 150mA is assumed. Furthermore, a current limitation is included to limit the maximum output current to 210mA. A load capacitance for the LVR of 150pF is assumed. The target system is a Li-ion battery powered mobile phone system on chip (SoC). Therefore, the main supply voltage can vary between 2.5V to 5V. Also an intermediate voltage domain with nominal 1.8V is available which a switched mode DC-DC converter generates. This intermediate voltage varies only between 1.65V and 1.95V because it is already regulated. The target process for this SoC is a digital 65nm CMOS process. The core supply voltage for the thin oxide transistors of 1.2V shall be generated by the presented LVR. In this process also 5V drain extended MOS (DEMOS) transistors are available. Additionally to the thin oxide transistors and the DEMOS transistors also thick oxide transistors for a nominal voltage of 1.8V are available. The main objective of this LVR is to supply fast load current transients of more than 100mA/100ns without deviating more than 10% from the nominal output voltage. Also a high DC accuracy of the output voltage is required which requests a high DC gain and low offset of the error amplifier.

2.2.2 Circuit Description

Because low dropout is not necessary in the system described, the LVR presented in this section takes advantage of the NMOS source follower topology. This means the pass device is an NMOS transistor. Furthermore, because a 1.8V domain is available, the pass device is supplied from this domain and the pass device is a 1.8V thick oxide transistor. Additionally, to have sufficient gate overdrive for the pass device, the battery supplies the error amplifier that drives the gate of the NMOS pass device directly. The LVR consists mainly of four different blocks as can be seen in Figure 2.18. These blocks are:

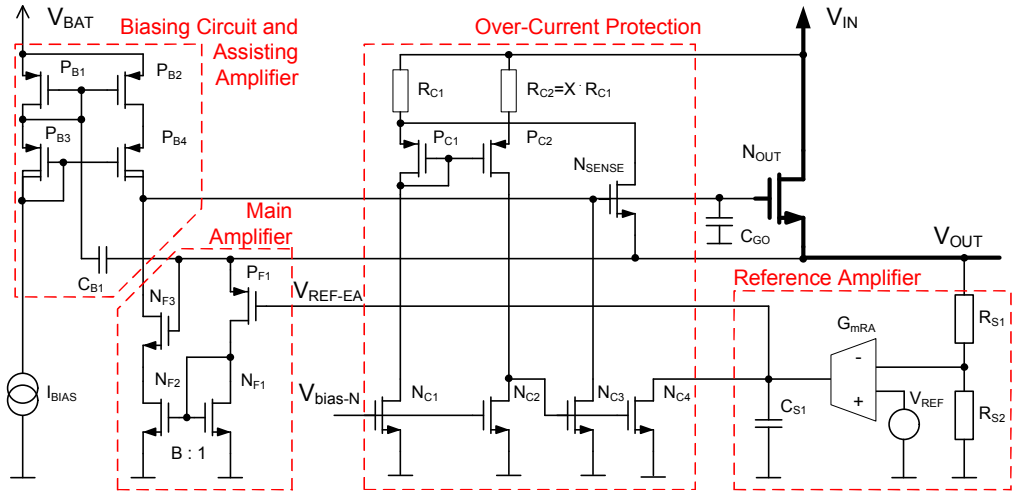

Figure 2.18: Schematic of the capacitor-less LVR

- Main amplifier
- Reference amplifier
- Biasing circuit acting as assisting amplifier
- Over current protection

A detailed description of the components follows later in this section. The main amplifier is a simple structure that allows fast transient response. The reference amplifier adjusts the reference voltage $V_{REF\text{-}EA}$ for the main amplifier to improve the DC accuracy of the LVR. To further improve the transient load response without increasing the DC current consumption the biasing circuit is extended to work as an additional error amplifier for high frequencies. An over current protection circuit is implemented to limit the maximum output current. And of course a pass device is also present in the LVR.

Main amplifier

A common gate error amplifier topology is utilized in the presented LVR. A similar circuit was used in [41] for a PMOS LVR to assist their main error amplifier. Due to the PMOS pass device an additional inverting stage is necessary. The proposed voltage regulator is based on an NMOS source follower output. This structure has an inherent regulating behavior due to the voltage sensitive source node of the pass device at the output. A disadvantage of this structure is that the supply voltage needs to be significantly higher than the output voltage; at least by the value of the maximum gate source voltage of the

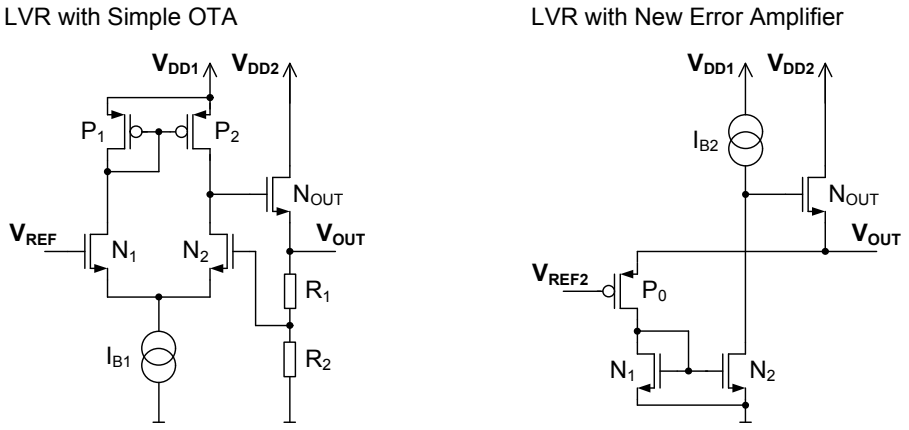

Figure 2.19: Simplified structure of the capacitor-less LVR

pass device for driving an output current of 210mA plus the saturation voltage of the bias circuit. In our case the supply voltage should be some 1V above the output voltage. Therefore the 1.8V supply V_{IN} is not capable of driving the main amplifier for generating 1.2V on the regulator output. To take advantage of the NMOS structure anyway, the main amplifier is biased directly from the battery supply that has a minimum voltage of 2.5V. The main amplifier consists basically of the four transistors P_{F1}, N_{F1}, N_{F2}, N_{F3} and the bias current source P_{B2}-P_{B4} as can be seen in Figure 2.18. P_{F1} acts as a common gate amplifier for sensing the output voltage and as a common source amplifier for the reference input. The drain current of P_{F1} is amplified by the current mirror N_{F1}-N_{F2} by the factor B=5 and drives the gate of the pass device N_{OUT}. The transistor N_{F3} acts as a cascode and increases the output resistance of the main amplifier. Additionally, N_{F3} shields N_{F2} from the voltage at the gate of the pass device to avoid voltage stress on N_{F2}. This structure driving N_{OUT} forms an operational transconductance amplifier (OTA) with one low impedance input and one high impedance input. The main amplifier can achieve a higher current efficiency while having the same transconductance compared to a conventional differential pair based OTA. A comparison of a simplified version of an LVR with a conventional OTA and the here used OTA is depicted in Figure 2.19. When assuming the input transistors are biased in sub threshold, the transconductance for the main amplifier is

$$Gm_{\mathrm{MA}} = B \cdot gm_{\mathrm{PF1}} = B \cdot \frac{I_{\mathrm{B}}}{n \cdot V_{\mathrm{T}}} \tag{2.4}$$

where B is the mirror ratio of N_{F1} to N_{F2}, I_B is the bias current through transistor P_{F1}, n is the substrate factor of the MOS devices and V_T is the temperature voltage. The

transconductance of the conventional OTA can be calculated as

$$Gm_{\mathrm{OTA}} = \frac{gm_1 + gm_2}{2} = \frac{1}{2} \cdot \frac{I_{\mathrm{B}}}{n \cdot V_{\mathrm{T}}} \tag{2.5}$$

A measure of how much bias current is needed to generate a certain transconductance in an OTA is the ratio of the transconductance to the total current consumption. Here this is referred to as current efficiency but it mustn't be confused with the current efficiency of an LVR that is defined in Equation 1.5 as ratio of the load current to the total current consumption. The ratio of the current efficiencies of the two OTA topologies is

$$\frac{\frac{Gm_{\mathrm{MA}}}{I_{\mathrm{TOTAL}}}}{\frac{Gm_{\mathrm{OTA}}}{I_{\mathrm{TOTAL}}}} = \frac{B \cdot \frac{I_{\mathrm{B}}}{n \cdot V_{\mathrm{T}}}}{(1+B) \cdot I_{\mathrm{B}}} \cdot \frac{I_{\mathrm{B}}}{\frac{1}{2} \cdot \frac{I_{\mathrm{B}}}{n \cdot V_{\mathrm{T}}}} = 2 \cdot \frac{B}{1+B} \tag{2.6}$$

This means that the OTA used as the main amplifier has a transconductance that is theoretically up to a factor of two higher than in a conventional OTA consuming the same current. Additionally, the feedback divider used in the LVR with the conventional OTA shown on the left in Figure 2.19 further decreases the effective transconductance by the voltage divider ratio. This, on the other hand means additional effort to generate the local reference voltage when using no feedback divider.

Reference amplifier

The reference amplifier is a slow error amplifier with high DC gain and low statistical offset. Its purpose is to generate the above mentioned local reference voltage $V_{\mathrm{REF\text{-}EA}}$ for the main amplifier. Two basic concepts for generating $V_{\mathrm{REF\text{-}EA}}$ were considered. On the one hand replica biasing and on the other hand a surrounding slow control loop. Both concepts are illustrated in Figure 2.20.

The advantage of the replica based generation of the local reference voltage $V_{\mathrm{REF\text{-}EA}}$ as depicted in Figure 2.20a is that the reference amplifier has no influence on the stability of the control loop closed by the main amplifier. The nested loop concept in 2.20b has the advantage, that the DC loop gain of the resulting system is increased by the DC gain of the reference amplifier. Additionally, due to the lack of the replica transistor no offset due to the mismatch of the input transistor P_{F1} of the main amplifier to its replica can occur and no current through this replica device is necessary. Therefore, the nested loop concept has been employed in this LVR. To neglect the influence of the reference amplifier on the overall stability, this reference amplifier is significantly slower than the main amplifier. A detailed discussion follows in the stability analysis section. Because the output of the

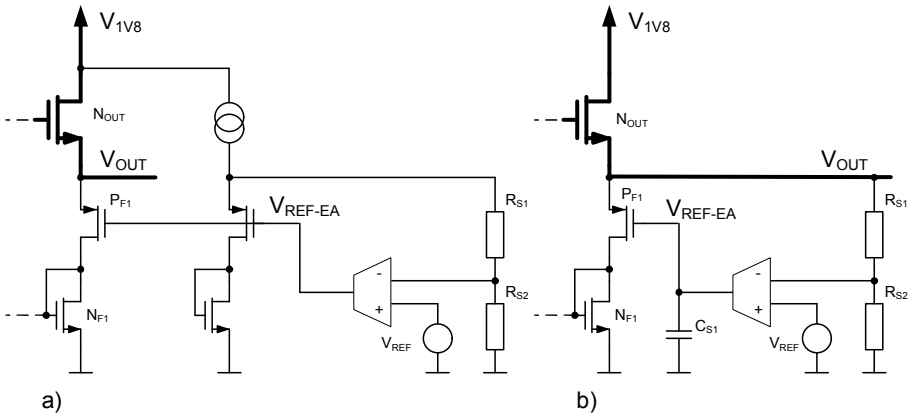

Figure 2.20: Generating the local reference voltage $V_{REF\text{-}EA}$

reference amplifier is connected to the reference input of the main amplifier, the feedback path closed over the reference amplifier also contains the transconductance of the main amplifier. The effective transadmittance of the reference amplifier is

$$Ym_{\mathrm{RA}} = Gm_{\mathrm{MA}} \cdot FB \cdot \frac{Gm_{\mathrm{RA}} \cdot r_{\mathrm{RA}}}{1 + s \cdot r_{\mathrm{RA}} \cdot C_{\mathrm{S1}}} \tag{2.7}$$

This is the transfer function from the voltage V_{OUT} to the drain current through P_{F1} in Figures 2.18 and 2.20b. Where FB is the feedback divider ratio of R_{S1} and R_{S2}, Gm_{RA} is the transconductance of the reference amplifier, r_{RA} is the output resistance of the reference amplifier and C_{S1} is the capacitor connected to the output of the reference amplifier.

Biasing circuit acting as assisting amplifier

The biasing block for the output of the main error amplifier is used as an additional amplifier. This amplifier is realized by connecting the capacitance C_{B1} between the LVR output and the gate of the transistor P_{B2} that delivers the bias current in the output path of the main amplifier. Because the biasing block is used as an amplifier, there is no additional current consumption. A similar approach is used in [30]. Opposed to the solution shown here the LVR in [30] uses a PMOS pass device. Therefore, in [30] an additional inverting stage is needed for modifying the bias current. The input of the assisting amplifier has a high pass characteristic due to the series connection of the capacitor C_{B1}. The effective transadmittance of the assisting amplifier can be expressed as:

$$Ym_{\mathrm{AA}} = gm_{\mathrm{PB2}} \cdot \frac{C_{\mathrm{B1}}}{C_{\mathrm{B1}} + C_{\mathrm{GS\text{-}PB}}} \cdot \frac{s \cdot \frac{C_{\mathrm{B1}} + C_{\mathrm{GS\text{-}PB}}}{gm_{\mathrm{PB1}}}}{1 + s \cdot \frac{C_{\mathrm{B1}} + C_{\mathrm{GS\text{-}PB}}}{gm_{\mathrm{PB1}}}} \tag{2.8}$$

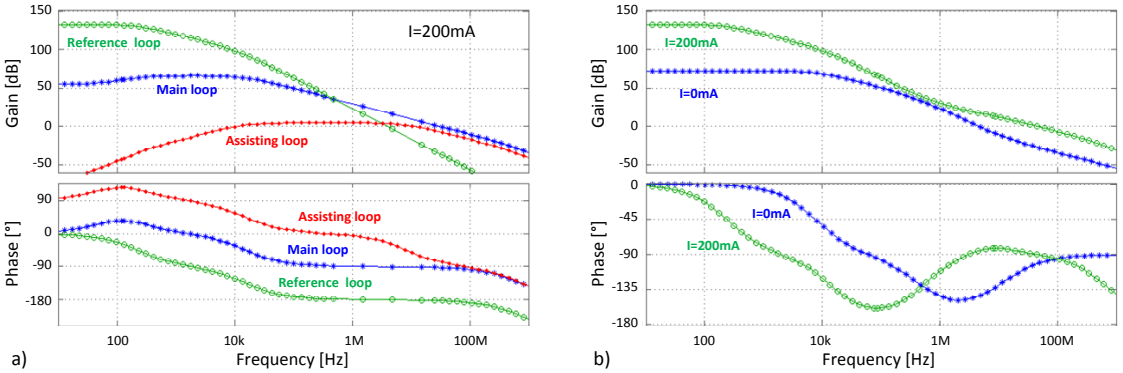

Figure 2.21: Bode diagram of the LVR; a) contribution of loops b) overall loop

where gm_{PB1} is the transconductance of the biasing transistor P_{B1}, gm_{PB2} is the transconductance of the biasing transistor P_{B2} and C_{GS_PB} is the sum of the gate source capacitance of the biasing transistors P_{B1} and P_{B2}. Because the transconductance of the main amplifier is only slightly higher than the transconductance of the assisting amplifier and both amplifiers are connected to the same compensation capacitance C_{GO}, the slope of the assisting amplifier in the Bode diagram approaches the slope of the main amplifier near the unity gain frequency (UGF). When summing up the transfer functions of the parallel control loops closed by the main amplifier and the assisting amplifier, this generates a pole-zero doublet near the UGF that increases slightly the overall UGF and it also improves the phase margin. An illustration of how the different loops closed over the three amplifiers contribute to the overall transfer function is given in Figure 2.21.

The disadvantage of the assisting amplifier is that the power supply rejection ratio (PSRR) is compromised. That is also true for the concept used in [30] with the PMOS pass device. Due to the capacitor C_{B1} at high frequencies there is a low ohmic path from V_{BAT} to V_{OUT} over the biasing transistor P_{B1} that is connected in MOS diode configuration. This introduces two problems. Firstly, the direct coupling path just mentioned degrades the PSRR. Secondly, the current flowing through P_{B1} also flows amplified by the current mirror ratio of B_B=14 through P_{B2} directly into the gate node of the pass device. The second coupling path degrades the PSRR more significantly.

Stability analysis

For the stability analysis the regulation loop of the LVR is opened between the output of the main error amplifier and the gate of the pass device. The LVR has three different

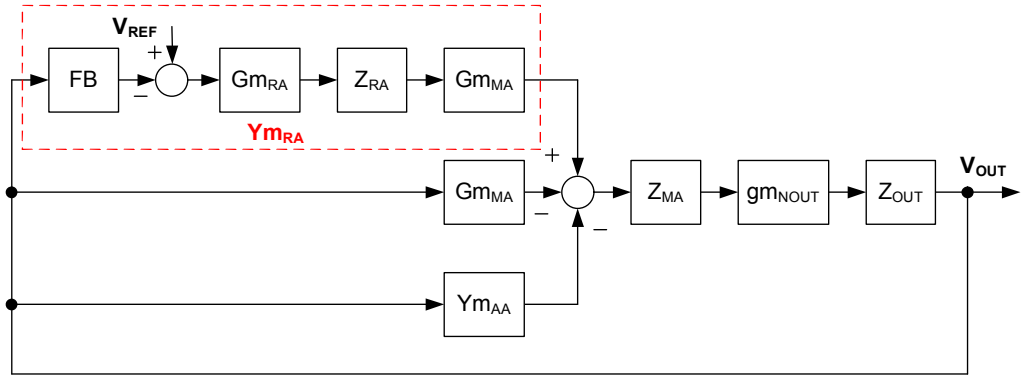

Figure 2.22: Control engineering block diagram of the LVR

feedback paths. The first feedback path is closed over the main amplifier and the pass device. The second feedback path is closed over the resistive feedback divider, the reference amplifier, the main amplifier and the pass device. And the third feedback path is closed over the capacitor C_{B1}, the biasing block and the pass device. Due to the three parallel feedback paths there are two pole-zero doublets generated. In [42] two parallel amplifiers are used to get high DC gain and a high UGF by generating a pole-zero doublet. In [43] it has been discussed how a pole-zero doublet changes the settling behavior of a system. It was found that the change in settling time due to a pole-zero doublet is relevant for sub 1% error bands. For the LVR described here this sub 1% error settling behavior is of minor interest. To illustrate the parallel structure a control engineering diagram is depicted in Figure 2.22. Figure 2.21a shows the contribution of each path for the full load case I=200mA. In Figure 2.22 Z_{RA}, Z_{MA} and Z_{OUT} represent the output impedances of the reference amplifier, the main amplifier and the LVR, respectively.

The open loop transfer function A_{OL} of the LVR according to Figure 2.22, when the loop is opened at the gate of the pass device, is

$$A_{\mathrm{OL}} = (Gm_{\mathrm{MA}} + Ym_{\mathrm{RA}} + Ym_{\mathrm{AA}}) \cdot Z_{\mathrm{MA}} \cdot gm_{\mathrm{NOUT}} \cdot Z_{\mathrm{OUT}} \tag{2.9}$$

This leads to the normalized open loop transfer function

$$A_{\mathrm{OL}} = \frac{gm_{\mathrm{NOUT}} \cdot B \cdot gm_{\mathrm{PF1}} \cdot r_{\mathrm{G}} \cdot FB \cdot Gm_{\mathrm{RA}} \cdot r_{\mathrm{RA}}}{gm_{\mathrm{NOUT}} + gm_{\mathrm{PF1}} \cdot FB \cdot Gm_{\mathrm{RA}} \cdot r_{\mathrm{RA}}} \cdot \frac{\left(1 + \frac{s}{\omega_{\mathrm{Z1}}}\right) \cdot \left(1 + \frac{s}{\omega_{\mathrm{Z2}}}\right) \cdot \left(1 + \frac{s}{\omega_{\mathrm{Z3}}}\right)}{\left(1 + \frac{s}{\omega_{\mathrm{P1}}}\right) \cdot \left(1 + \frac{s}{\omega_{\mathrm{P2}}}\right) \cdot \left(1 + \frac{s}{\omega_{\mathrm{P3}}}\right) \cdot \left(1 + \frac{s}{\omega_{\mathrm{P4}}}\right)} \tag{2.10}$$

where gm_{NOUT} is the transconductance of the pass device, B is the mirror ratio of the transistors N_{F1} and N_{F2}, r_G is the output resistance of the main amplifier, and FB is the

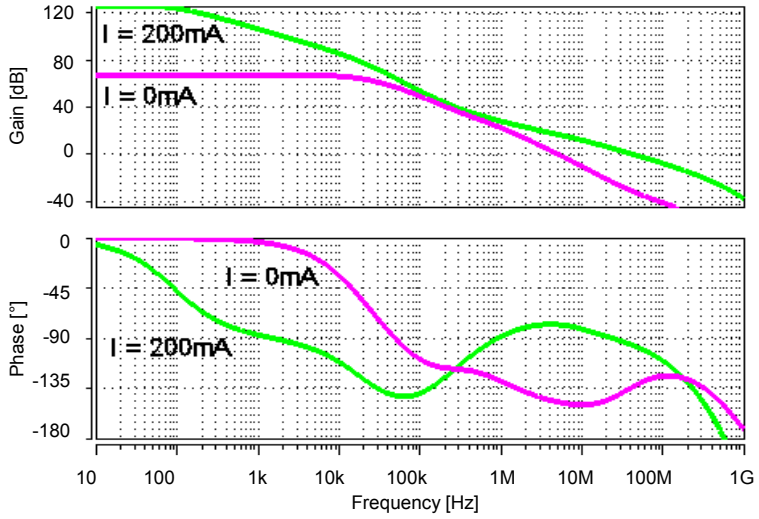

Figure 2.23: Open loop gain of the LVR

feedback divider ratio of R_{S1} and R_{S2}, Gm_{RA} is the transconductance of the reference amplifier, r_{RA} is the output resistance of the reference amplifier and ω_{Px} and ω_{Zx} are the most relevant poles and zeros. The output resistance of the main amplifier can be calculated as

$$r_G = (r_{DS\text{-}NF2} \cdot gm_{NF3} \cdot r_{DS\text{-}NF3}) \,//\, (r_{DS\text{-}PB2} \cdot gm_{PB4} \cdot r_{DS\text{-}PB4}) \tag{2.11}$$

The dominant pole ω_{P1} is generated by the reference amplifier and its load capacitance

$$\omega_{P1} = \frac{Gm_{RA}}{C_{S1}} \cdot FB \cdot \frac{gm_{PF1}}{gm_{NOUT}} \tag{2.12}$$

This pole is followed by the zero ω_{Z1} generated due to the parallel paths of the reference amplifier and the main amplifier.

$$\omega_{Z1} = \frac{Gm_{RA}}{C_{S1}} \cdot FB \tag{2.13}$$

The second pole ω_{P2} is the dominant pole for the main amplifier and it is generated by the output resistance of the main amplifier r_G and the compensation capacitor C_{GO}.

$$\omega_{P2} = \frac{1}{C_{S1} \cdot r_G} \tag{2.14}$$

The zero ω_{Z2} is generated due to the parallel structure of the main amplifier and the assisting amplifier in the biasing block. Here this ω_{Z2} is ahead of the pole ω_{P3} that is the counterpart of the pole-zero doublet generated due to the parallel structure of the main

amplifier and the assisting amplifier. This doublet is placed near the UGF to improve the phase margin of the system:

$$\omega_{Z2} = \frac{gm_{PB1}}{C_{S1} + C_{GS\text{-}B}} \cdot \frac{B \cdot gm_{PF1}}{B \cdot gm_{PF1} + gm_{PB2}} \tag{2.15}$$

$$\omega_{P3} = \frac{gm_{PB1}}{C_{S1} + C_{GS\text{-}B}} \tag{2.16}$$

where gm_{PB1} is the transconductance of the input transistor of the biasing current mirror, gm_{PB2} is the transconductance of the output transistor of the biasing current mirror and $C_{GS\text{-}B}$ is the sum of gate source capacitance of the biasing transistors P_{B1} and P_{B2}.

The output pole ω_{P4} of the LVR generated by the load capacitor C_{OUT} and the transconductance gm_{NOUT} of the pass device is placed above the UGF. The output pole frequency is decreased by the capacitive voltage divider ratio of the compensation capacitor C_{GO} to the gate source capacitance of the pass device $C_{GS\text{-}NOUT}$. Therefore, C_{GO} should be larger than $C_{GS\text{-}NOUT}$ to push ω_{P4} to higher frequencies.

$$\omega_{P4} = \frac{gm_{NOUT}}{C_{OUT}} \cdot \frac{C_{GO}}{C_{GO} + C_{GS\text{-}NOUT}} \tag{2.17}$$

The zero ω_{Z3} due to the finite gate source capacitance $C_{GS\text{-}NOUT}$ is also beyond the UGF.

$$\omega_{Z3} = \frac{gm_{NOUT}}{C_{GS\text{-}NOUT}} \tag{2.18}$$

Figure 2.23 shows the simulated Bode diagram of the open loop gain for the LVR. The output resistance of the LVR can be calculated as

$$r_{OUT} = \frac{1}{gm_{NOUT} + gm_{PF1} \cdot FB \cdot Gm_{RA} \cdot r_{RA}} \tag{2.19}$$

Over current protection

To protect the LVR and the load, a current limiting circuit is included in the LVR. The LVR should work in normal operation up to 200mA. The over current protection clamps the output voltage gradually, starting at 210mA load current. The circuit for the over current protection is shown in Figure 2.24. It basically comprises the transistors N_{C1} to N_{C4}, N_{SENSE}, P_{C1}, P_{C2} and the resistors R_{C1} and R_{C2}. The transistor N_{SENSE} is a replica of the pass device N_{OUT} with the ratio $B_{N\text{-}SENSE}$ = 1:100. Due to having the same gate source voltage, a defined fraction of the output current is delivered over N_{SENSE}. The drain of N_{SENSE} is connected to the resistor R_{C1}. Therefore, when neglecting the small constant bias current over N_{C1} and P_{C1}, the drain current of N_{SENSE} generates a voltage drop over

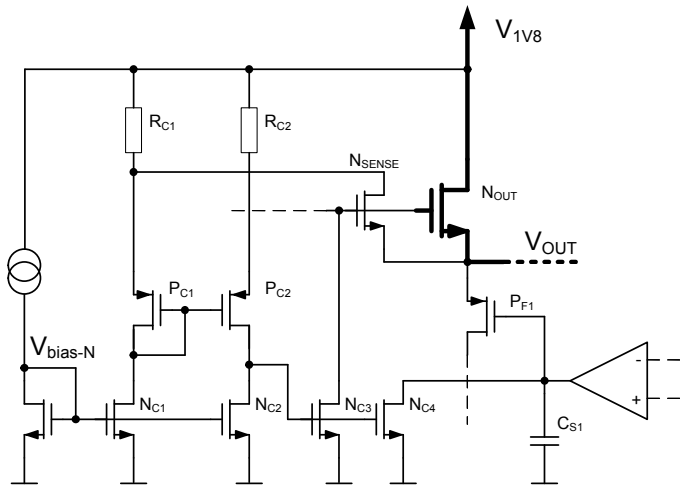

Figure 2.24: Current limiter section of the LVR

R_{C1} that is proportional to the output current. Because P_{C1} is in MOS diode connection and the gates of P_{C1} and P_{C2} are connected together, the transistor P_{C2} acts as a source follower on the resistor R_{C2}. As long as P_{C1} and P_{C2} are biased in sub threshold, the voltage across R_{C2} can be approximated as

$$V_{\text{RC2}} = V_{\text{RC1}} - V_{\text{GS-PC1}} + V_{\text{GS-PC2}} \approx V_{\text{RC1}} \tag{2.20}$$

Subsequently, the current through R_{C2} can be calculated as

$$I_{\text{RC2}} = \frac{V_{\text{RC2}}}{R_{\text{C2}}} \approx \frac{V_{\text{RC1}}}{R_{\text{C2}}} \tag{2.21}$$

Because the voltage across R_{C1} is generated by a fraction of the output current, also the current through R_{C2} can be expressed as a fraction of the output current. Equation 2.22 is valid as long as the current source transistor N_{C2} is not in saturation, i.e. the current through R_{C2} and P_{C2} is smaller than the current through N_{C2} in saturation.

$$I_{\text{RC2}} \approx \frac{R_{\text{C1}}}{R_{\text{C2}}} \cdot B_{\text{N-SENSE}} \cdot I_{\text{OUT}} \tag{2.22}$$

As soon as the current I_{RC2} exceeds the reference current through N_{C2}, the voltage at the drain of N_{C2} rises and turns on the transistor N_{C3}. N_{C3} in turn discharges the gate of the pass device and therefore limits the output current delivered by N_{OUT}. Additionally, the transistor N_{C4} limits the voltage at the output of the reference amplifier. This is necessary, because otherwise the reference voltage $V_{REF\text{-}EA}$ would run away due to the reduced output voltage. This structure allows a high current efficiency because the sense current through N_{SENSE} is not dissipated to ground but used as part of the output current. There is only a

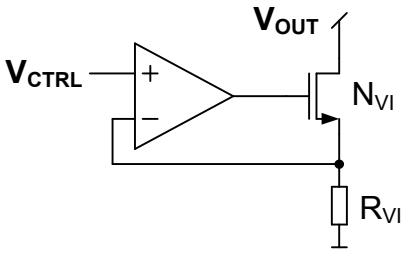

Figure 2.25: Voltage controlled current source

fixed current consumption of 1μA for biasing P_{C1} and a maximum of another 1μA through N_{C2} when the current limit is reached.

Current consumption

The simulated overall current consumption of the capacitor-less LVR is approximately 133μA in total. The output stage of the main amplifier is supplied with 96μA by a current mirror from the battery supply V_{BAT} and 7μA are used in the input of the current mirror. The input stage of the main amplifier draws 20μA from the LVR output that is subsequently supplied by the intermediate voltage domain V_{IN}. Also, V_{IN} supplies the reference amplifier with 5μA. The voltage divider composed of R_{S1} and R_{S2} draws another 5μA via V_{OUT} from the intermediate supply V_{IN}. This means the quiescent current from V_{BAT} is 103μA and the quiescent current from V_{IN} is 30μA for a nominal simulation.

2.2.3 On-Chip Voltage Controlled Current Source

To be able to characterize the LVR, a test load has been placed on the same test chip. This test load is a voltage controlled current source where an externally applied voltage V_{CTRL} generates a defined load current through an integrated resistor R_{VI}.

The voltage controlled current source is used to generate defined load current slopes of up to 150mA/100ns for the LVR. Figure 2.25 shows the schematic of the voltage controlled current source. The amplifier is supplied by a dedicated pad to separate the current consumption of the test load from the current consumed by the LVR itself. The drain of N_{VI} is the output of the voltage controlled current source and it is connected to the output node of the LVR V_{OUT}.

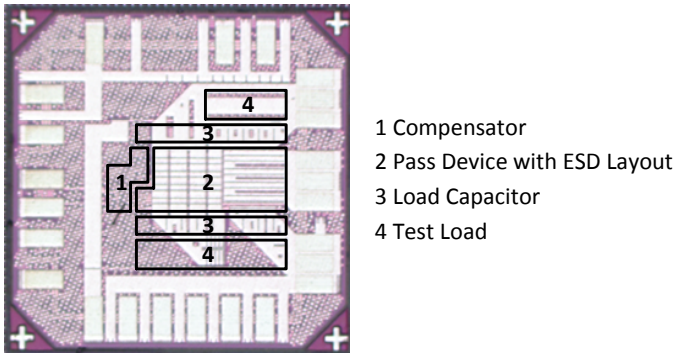

Figure 2.26: Die photo of the unbonded LVR test chip

2.2.4 Measurement Results

The test chip for the capacitor-less LVR has been fabricated in a 65nm digital CMOS process. A photograph of the unbonded die can be seen in Figure 2.26. The test chip has a size of 1mm by 1mm. The total active area without pads is 0.135mm^2. The regulator consumes 0.04mm^2. There is also an electro static discharge (ESD) protection for the pass device, which is necessary for handling the chip with the external pin for the LVR output voltage. In an SoC where only an internal load is present and no external pin is necessary, this ESD protection of 0.055mm^2 would also not be needed in full size. And the 150pF integrated load capacitor consumes another 0.04mm^2. All measurements were performed at room temperature with a nominal battery voltage of 3.6V at V_{BAT} and 1.8V at the intermediate voltage V_{IN}. The output voltage of the LVR test chip is 1.200V with an external 600mV reference voltage. The offset of the LVR is less than 1% for six sigma. This figure was not measured but simulated with 1200 Monte Carlo runs taking local and global variations into account. The focus of the LVR is on transient load response. This transient load response was measured with the integrated voltage controlled current source. Therefore, very fast perturbations emulating on-chip loads are possible. Figure 2.27 shows a load current jump from 1mA to 150mA with a rise time of 100ns. This fast load current jump caused a voltage undershoot of 90mV which is well within the desired 10% limit of the nominal output voltage.

Figure 2.28 shows the transient response to an over load event. The load is a combination of a constant load and a dynamic load. The constant load is an external discrete 10Ω resistor and the dynamic load is the integrated voltage controlled current source. The current source jumps again from 1mA to 150mA with a rise time of 100ns. As can be seen from the oscilloscope screenshot, the output voltage breaks down after a short over

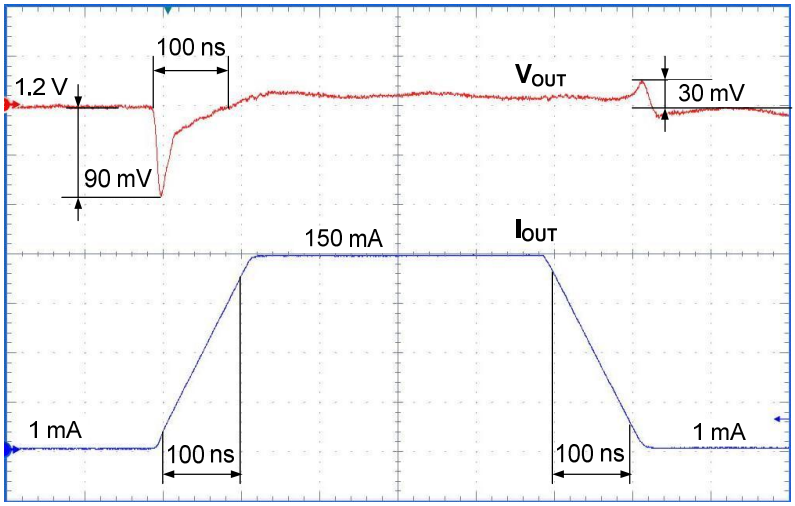

Figure 2.27: Transient load response; V_{OUT}: 50mV/div, I_{OUT}: 37.5mA/div, t: 100ns/div

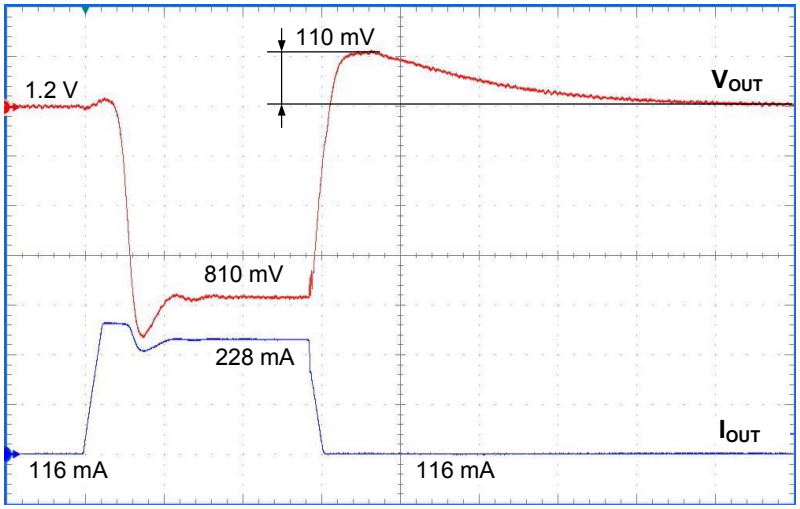

Figure 2.28: Over current response; V_{OUT}: 100mV/div, I_{OUT}: 50mA/div, t: 500ns/div

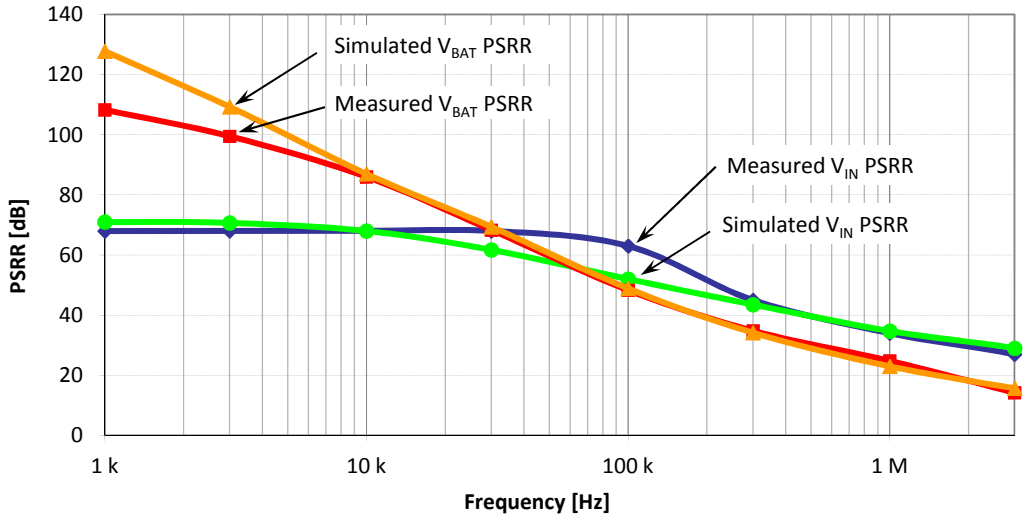

Figure 2.29: Measured and simulated PSRR of the LVR at I_{OUT}=120mA

Table 2.3: Summary of the static properties of the LVR

Process	65nm digital CMOS
Active area for regulator	0.04mm^2
Area for ESD protection	0.055mm^2
Area for 150pF load capacitor	0.04mm^2
Battery supply voltage	2.5V - 5V
Intermediate supply voltage	1.65V - 1.95V
Output voltage	1.2V
Load current	0mA - 200mA
Static load regulation	78μV/mA
Static line regulation battery supply	8μV/V
Static line regulation intermediate supply	433μV/V
Current consumption battery supply	96μA
Current consumption intermediate supply	36μA

current. In this case the output voltage is reduced to 810mV to limit the output current to 228mA. After the voltage controlled current source goes back to 1mA also the output voltage recovers with a short overshoot.

The results of the PSRR measurement are illustrated in Figure 2.29. Because there are two separated supply pins V_{BAT} and V_{IN}, there are also two PSRR curves plotted. Both curves show good agreement with the simulated PSRR results. Above 80dB the PSRR measurements are not very reliable because the measured voltages were already at the boarder of the resolution of the measurement equipment. A summary of the measured static properties of the LVR can be found in Table 2.3.

Table 2.4: Comparison of the capacitor-less LVR with state of the art

Publication	[44]	[30]	[29]	[28]	This work
Year	2008	2010	2008	2006	2010
Process	0.35μm CMOS	0.35μm CMOS	0.35μm CMOS	0.35μm CMOS	65nm CMOS
V_{IN} [V]	2-3	1.4	1.2-1.5	2-3.6V	2.5-5 & 1.65-1.95
V_{OUT} [V]	1.8	1.2	1	1.8	1.2
$I_{OUT-MAX}$ [mA]	100	100	50	240	200
I_Q [μA]	27	43	95	3	132
C_{LOAD} [pF]	- [1]	- [1]	20 [1]	- [1]	150
Area [mm^2]	0.26	0.16	0.045	0.11	0.08
ΔV_{OUT} [mV]	1000	70	160	50	90
$\Delta I/\Delta t$ [mA/μs]	1-100/0.5	1-100/1	0-50/0.3	1-150/1.5	1-150/0.125

2.2.5 Comparison with State of the Art

In this section the results of the presented capacitor-less LVR are compared with other published capacitor-less LVRs with similar values for the maximum load current and output voltage. Table 2.4 gives an overview of the key properties of the published LVRs. The load current slope of [28–30] lies in the range of 100mA/μs to 170mA/μs (50mA/300ns). The capacitor-less LVR in this work is tested with a load current slope of 1200mA/μs (150mA/125ns) that is faster by a factor of more than seven. Except from [44], which has been tested with a load current slope of 100mA/500ns and has an undershoot of more than 50%, all regulators in Table 2.4 have an undershoot in the range of 3% to 16% of the nominal output voltage. As direct comparison the LVR in this work has an output voltage undershoot of only 16mV or less than 2% of the nominal output voltage when loaded with a current slope of 120mA/μs (1mA-150mA/1.25μs). The advantage of regulation speed of the presented LVR has to be paid with a higher current consumption than the other LVRs in the direct comparison.

2.2.6 Improvements

The current limitation in the presented LVR is not robust. It works fine for short over current pulses. But if the over load is applied for a long period the local reference voltage V_{REF-EA} runs away. This can be explained by the mismatch of the clamping currents through the transistors N_{C3} and N_{C4} in the current limiter block. One possible solution could be to not connect the clamping transistor N_{C4} to the output of the reference amplifier

[1] No dedicated capacitor used. In [29] 20pF are estimated for the measuring probe.

but rather to clamp the input of the reference amplifier. That could be disconnecting the non-inverting input of the reference amplifier from the reference voltage V_{REF} and clamp this input to ground. Therefore both can be achieved, a fast clamping of the gate voltage of the pass device N_{OUT} and avoiding the runaway of the local reference voltage $V_{REF\text{-}EA}$.

2.3 Improved Capacitor-Less Linear Voltage Regulator

A summary of the linear voltage regulator (LVR) presented in this chapter has been published in [26].

2.3.1 Design Targets

In this section a second version of an output capacitor-less LVR is presented. This LVR has been developed to further improve the transient performance of the LVR presented in the previous section. The idea is to use this LVR to supply a high performance microcontroller without using an external buffer capacitor. As a target application a microcontroller from Infineon's future automotive product palette called AURIX was chosen. This 32-bit microcontroller runs with a clock of up to 200MHz and has a size of almost 3 million NAND gate equivalents. It is implemented in a 65nm digital CMOS process with flash memory.

In such huge digital blocks like microcontrollers, so called filler cells are used. These are small cells that have the same height as digital standard cells in the layout but their only function is to act as a small buffer capacitor for the digital supply voltage. These filler cells are also used when a big external buffer capacitor for the digital supply voltage is present. The capacitor formed by the filler cells is distributed over the whole digital core and it is effective up to the Gigahertz range where the external capacitor is already ineffective due to bonding parasitics and routing parasitics. In the case of the here mentioned AURIX implementation the total load capacitance of the core including the filler cells is about 5nF. Although 5nF is already quite a large capacitance for on-chip integration, this is the load and not an additional dedicated capacitance. Therefore the term output capacitor-less is used for the described LVR. Typical capacitance values for published output capacitor-less LVRs are in the range of 100pF [27, 31–34].

The LVR has to generate an output voltage of 1.3V and has to deliver a maximum output current of 200mA. The input voltage is nominal either 5V or 3.3V both with a variation of up to $\pm 10\%$. This means a total input voltage range of 2.97V to 5.5V. Fast load changes of the microcontroller (e.g. from sleep mode into normal mode) result in a fast change in the load current. Therefore, the LVR has to supply load transients of up to 100mA/20ns without resulting in a voltage undershoot or overshoot of more than 100mV.

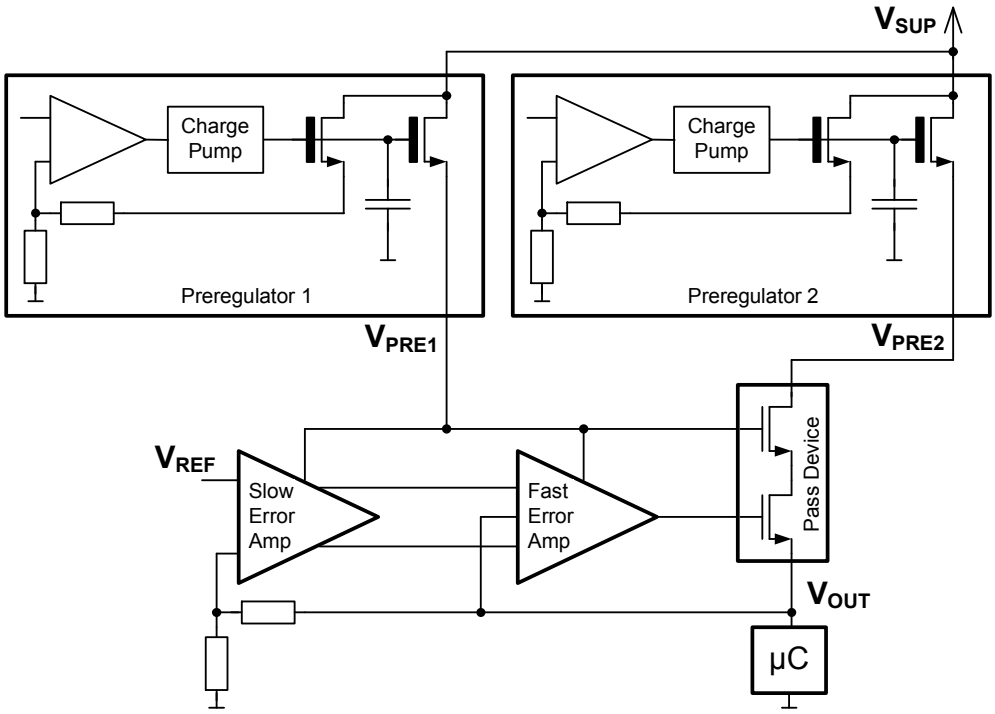

Figure 2.30: System overview

The static accuracy of the LVR must be within ± 30mV. The target range for the junction temperature is -40°C to 170°C.

2.3.2 Circuit Description

To be able to generate the core voltage of 1.3V for the microcontroller from a supply voltage of up to 5.5V the circuit for the LVR has to be built with transistors that can be operated at that voltage. Such medium voltage transistors are available in the used 65nm CMOS process with flash memory. But these medium voltage transistors have a much worse performance compared to the thin oxide core transistors that can only be operated at 1.3V.

As a consequence the LVR was divided into an inaccurate preregulator for the 5V supply and a fast and accurate main regulator for delivering the 1.3V core voltage, whereas the preregulator is built with medium voltage transistors and the main regulator is built with thin oxide core transistors. The main regulator is subdivided again into a fast error amplifier for fast transient response, a slow error amplifier for high DC accuracy and a pass device. In Figure 2.30 the five main blocks of the proposed LVR are depicted.

These blocks are:

- Preregulator 1
- Preregulator 2
- Fast error amplifier
- Slow error amplifier
- Core pass device

A detailed description follows after a short description in this section. Both preregulators are identical in topology but different in driving strength. Preregulator 1 supplies the core transistor error amplifiers and preregulator 2 supplies the full output current of up to 200mA to the core pass device. The fast error amplifier is the heart of the LVR and it allows fast transient response. The slow error amplifier has a high DC gain to allow high DC accuracy of the LVR. The core pass device consists of two stacked minimum length thin oxide transistors and a sensing transistor to determine the output current. Finally, the microcontroller represents the load including the output capacitance for the LVR.

Preregulators 1 and 2

Both preregulators have an identical topology. They only differ in their output current driving capability. Due to the worse small signal performance and transient performance of the medium voltage transistors compared to the core transistors available in the used 65nm CMOS process with flash memory, these medium voltage transistors are not used exclusively in this LVR. Instead a stacked regulator approach is used. The preregulator doesn't regulate the intermediate voltage directly (i.e. the output of the preregulator). It is a replica biased source follower and therefore, only the gate voltage of this medium voltage NMOS pass devices is controlled. This has the advantage that the control loop in the preregulator doesn't need to be fast. Otherwise the error amplifier in the preregulator would consume a multiple of the quiescent current of the fast core error amplifier. The drawback of this solution however, is that the intermediate voltage varies strongly depending on the load current. Because of the low gain factor of the medium voltage transistor the width of this transistor has to be increased to a very large value in order to keep the intermediate voltage in a certain range. For preregulator 1 this means the dimensions W/L are 2.5mm/800nm to maintain a voltage between 2.1V and 2.6V and for

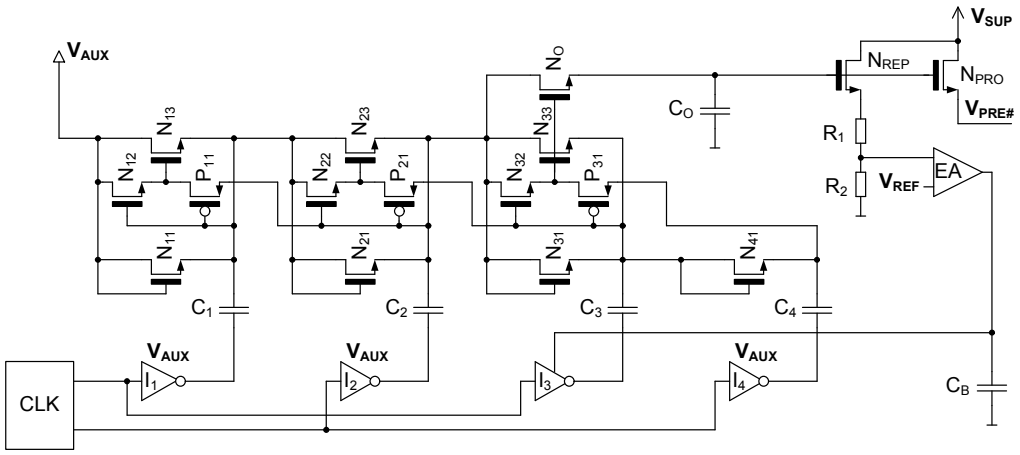

Figure 2.31: Schematic of one preregulator including the charge pump

preregulator 2 the dimensions W/L are 20mm/800nm to maintain a voltage between 1.7V and 3V over all process, voltage and temperature (PVT) corners and the whole current range. To minimize the high dropout voltage of this preregulator a charge pump has also been implemented to drive the gate of the preregulator pass device. A schematic of the preregulator including the charge pump is depicted in Figure 2.31. To maximize the efficiency of the charge pump a topology with active switches parallel to diode connected transistors between the single pumping stages according to [45] has been implemented. The charge pump has no DC load beside the gate leakage of the pass device that is negligible. Due to the big dimensions of the pass device in the preregulator two subsequent problems arise. Firstly, the power supply rejection ratio (PSRR) deteriorates because of the drain gate capacitance of the preregulator pass device. This capacitance gives a coupling path of the power supply noise directly to the gate of the source follower connected pass device. Secondly, the transient load response of the preregulator is deteriorated by the large gate source capacitance. Since the output impedance of the charge pump that drives the gate of the pass device is quite high, a sudden change in the intermediate voltage couples to the gate of the pass device and changes the gate voltage. Both effects mentioned can be relaxed in putting a large capacitor that buffers the gate voltage against the ground potential. This capacitor has to be at least in the same order of magnitude as the parasitic capacitances mentioned before. In the case of preregulator 1 a capacitance of 10pF is used while for preregulator 2 a 20pF capacitance is used.

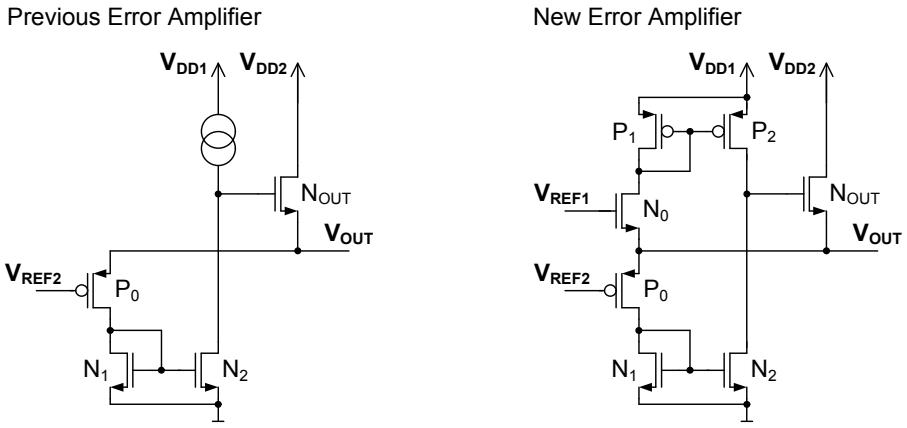

Figure 2.32: Simplified structure of the improved capacitor-less LDO

Fast error amplifier

The core of the LVR described in this section is the fast error amplifier and it is based on the LVR described in the previous section 2.2. The new error amplifier is created by complementary expanding the previous error amplifier from a PMOS input P_0 to a PMOS plus NMOS input stage P_0 and N_0 as illustrated in Figure 2.32. Therefore, the new error amplifier has a class AB output instead of only having a class A output like the basic configuration of the error amplifier in the previous section. The disadvantage however, is that the bias current in the output stage of the new error amplifier has to be defined with more effort compared to the class A output stage. This bias current is defined by the bias current in the input stage formed by transistors P_0 and N_0 and the both current mirrors formed by N_1-N_2 and P_1-P_2, respectively. Furthermore, the reference voltages V_{REF1} and V_{REF2} and the properties of the input transistors P_0 and N_0 define the bias current in the input stage. One possibility to define the bias currents in the input and output stage of the error amplifier is to generate the reference voltages V_{REF1} and V_{REF2} with diode connected replicas of P_0 and N_0 biased with a constant current like P_{R0} and N_{R0} in Figure 2.33. That means that the bias current in the output stage is dependent on the bias current through the diode connected replica transistors and the matching of N_{R0} to N_0 and P_1 to P_2. The same is true for the complementary part comprising P_{R0}, P_0, N_1 and N_2. Unfortunately, good matching requires large transistor dimensions whereas high speed for the regulator requires small dimensions to keep the parasitics low. Therefore, a compromise between bias current matching and regulator speed has to be found. The fast error amplifier is an operational transconductance amplifier (OTA) that has a higher current efficiency for

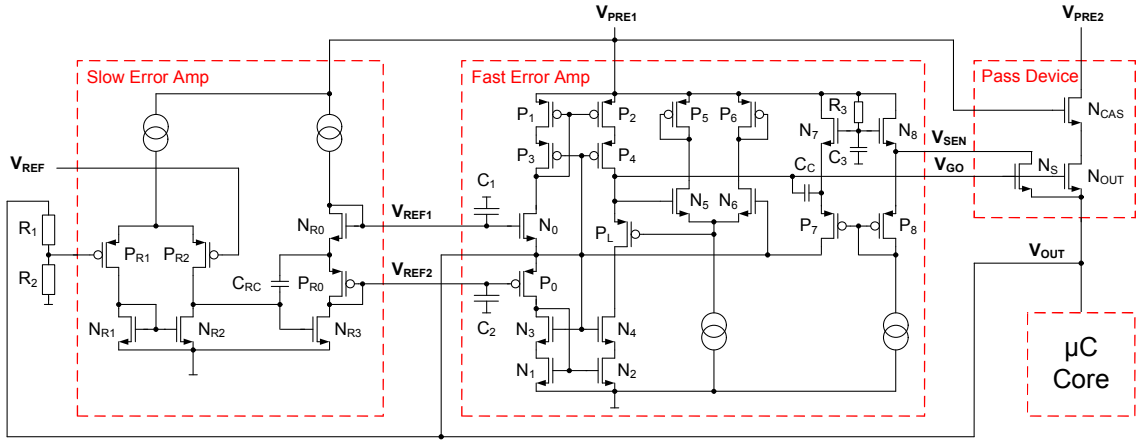

Figure 2.33: Schematic of the core transistor circuit of the capacitor-less LVR

achieving the same transconductance compared to a conventional differential pair based OTA. When assuming the input transistors are biased in sub threshold the transconductance for the fast error amplifier is

$$Gm_{\mathrm{FEA}} = B \cdot (gm_{\mathrm{N0}} + gm_{\mathrm{P0}}) = B \cdot 2 \cdot \frac{I_{\mathrm{B}}}{n \cdot V_{\mathrm{T}}} \tag{2.23}$$

where B is the mirror ratio of N_1 to N_2 (P_1 to P_2), I_B is the bias current through transistors N_0 and P_0, n is the substrate factor of the MOS devices and V_T is the temperature voltage. For the conventional OTA can be calculated

$$Gm_{\mathrm{OTA}} = \frac{gm_1 + gm_2}{2} = \frac{1}{2} \cdot \frac{I_{\mathrm{B}}}{n \cdot V_{\mathrm{T}}} \tag{2.24}$$

The ratios of the current efficiencies is

$$\frac{\frac{Gm_{\mathrm{FEA}}}{I_{\mathrm{TOTAL}}}}{\frac{Gm_{\mathrm{OTA}}}{I_{\mathrm{TOTAL}}}} = \frac{B \cdot 2 \cdot \frac{I_{\mathrm{B}}}{n \cdot V_{\mathrm{T}}}}{(1+B) \cdot I_{\mathrm{B}}} \cdot \frac{I_{\mathrm{B}}}{\frac{1}{2} \cdot \frac{I_{\mathrm{B}}}{n \cdot V_{\mathrm{T}}}} = 4 \cdot \frac{B}{1+B} \tag{2.25}$$

That means with the same total current consumption with the fast error amplifier a higher transconductance can be achieved compared to the conventional OTA by a factor of theoretically up to 4, depending on the mirror ratio B. Figure 2.33 shows all parts of the core transistor circuit of the LVR where the "Fast Error Amplifier" is highlighted and labeled among the other blocks. Here the basic error amplifier on the right hand side of Figure 2.32 is expanded to extend the supply voltage range, to improve the large signal behavior and to guarantee small signal stability. The supply voltage of the error amplifiers V_{PRE1} can be up to 2.6V that is the double of the rated voltage of the core transistors in the used 65nm CMOS process. Basically, the output voltage of the error amplifier V_{GO}

can also vary between 0V and V_{PRE1}. Therefore, to not stress the transistors N_2 and P_2 in the output stage of the fast error amplifier, the cascode transistors N_4 and P_4 have been introduced. Additionally, the cascode transistors N_3 and P_3 have been introduced to increase the systematic current matching of the current mirrors consisting of N_1-N_2 and P_1-P_2, respectively. With 2.6V at V_{GO} the transistor N_4 would be stressed between drain and source because its source potential would be one gate source voltage below the output voltage of 1.3V. Due to the replica biased source follower structure of the preregulators the intermediate voltage V_{PRE1} reduces gradually with the load current. This happens because a part of the output current of the LVR is delivered over the preregulator 1 and the current sensing transistor N_S. When the output current is at its maximum, also the gate voltage of the pass device V_{GO} is at its maximum value that is nearly V_{PRE1}. But at that moment V_{PRE1} is significantly below 2.6V and no transistor in the fast error amplifier will be stressed. On the other hand the PMOS transistor P_4 would be stressed in zero load condition. This is prohibited by the limiting transistor P_L. The transistor P_L limits the minimum output voltage of the error amplifier V_{GO} to approximately the output voltage of the LVR V_{OUT}. The maximum voltage chooser comprising the transistors N_5, N_6, P_5 and P_6 controls the gate of the transistor P_L. In normal operation (i. e. the output current of the LVR is not zero) the output voltage of the error amplifier V_{GO} is at least on threshold voltage above the output voltage of the LVR V_{OUT}. As a consequence, most of the bias current in the maximum voltage chooser flows through N_5 and N_6 is nearly pinched off. Now P_L is operated in the linear region as a switch because the gate source voltage of P_L is identical to the gate source voltage of N_5. The transistor N_5 is designed to have a sufficiently high gate source voltage in normal operation. On the other hand, if the output voltage of the error amplifier V_{GO} begins to move towards voltages below the output voltage of the LVR V_{OUT}, the bias current of the maximum voltage chooser gradually moves from N_5 to N_6. Subsequently, this reduces the gate source voltage of N_5 and pinches off P_L. This voltage limiting feature not only protects the transistor P_4. It especially improves the large signal performance of the LVR after a load current jump from a high value to zero. Without the limiting circuit described, the output voltage of the error amplifier V_{GO} could approach 0V. If the load current then jumped from zero again to a high value while V_{GO} is still at 0V, then a large undershoot at the output of the LVR V_{OUT} would occur.

For frequency compensation the dominant pole of the fast error amplifier is placed at

the output node of fast error amplifier. Therefore, a capacitor C_C is connected to the node V_{GO}. Additionally, the transistors N_7 and P_7 in combination with the capacitor C_C generate a zero in the transfer function. This zero is designed to track the output pole of the LVR. Tracking the output pole can be achieved by forcing the current of N_7 and P_7 to be proportional to the output current. To fulfill this requirement the sensing transistor N_S supplies a fraction of the output current which is defined by the ratio B_{SEN} of N_{OUT} to N_S. This fraction of the output current also flows through the diode connected transistor N_8 generating an according voltage drop over N_8. Already at moderate output current levels the current through N_8 is dominated by the sensed current through N_S and the bias current can be neglected. Therefore, the voltage at node V_{SEN} is defined by the output current. The diode connected transistor P_8 is biased in the sub threshold region and defines the gate voltage of transistor P_7 to be approximately one threshold voltage below V_{SEN}. The voltage drop between their gates defines the current through N_7 and P_7. This voltage is equivalent to the sum of the gate source voltages of N_7 and P_7:

$$V_{\text{G-N7}} - V_{\text{G-P7}} = V_{\text{GS-N7}} - V_{\text{GS-P7}} = V_{\text{GS-N8}} - V_{\text{GS-P8}} \tag{2.26}$$

where $V_{GS\text{-}N8}$ is defined by the load current and $V_{GS\text{-}P8}$ is one threshold voltage.

$$V_{\text{GS-N8}} = V_{\text{TH-N}} + \sqrt{\frac{2 \cdot I_{\text{D-N8}} \cdot L_{\text{N8}}}{K'_{\text{N}} \cdot W_{\text{N8}}}} \tag{2.27}$$

$$V_{\text{GS-P8}} \approx V_{\text{TH-P}} \tag{2.28}$$

with

$$I_{\text{D-N8}} = I_{\text{D-NS}} + I_{\text{BIAS}} \approx I_{\text{D-NS}} = \frac{I_{\text{OUT}}}{B_{\text{SEN}}} \tag{2.29}$$

follows

$$I_{\text{D-N7}} \approx \frac{I_{\text{OUT}}}{k_{\text{I-Z}}} \tag{2.30}$$

with

$$k_{\text{I-Z}} = B_{\text{SEN}} \cdot \left(\frac{K'_{\text{N}}}{K'_{\text{P}}} \cdot \frac{W_{\text{N8}} \cdot L_{\text{P7}}}{L_{\text{N8}} \cdot W_{\text{P7}}} + \frac{W_{\text{N8}} \cdot L_{\text{N7}}}{L_{\text{N8}} \cdot W_{\text{N7}}} + 2 \cdot \frac{W_{\text{N8}}}{L_{\text{N8}}} \cdot \sqrt{\frac{K'_{\text{N}}}{K'_{\text{P}}} \cdot \frac{L_{\text{N7}} \cdot L_{\text{P7}}}{W_{\text{N7}} \cdot W_{\text{P7}}}} \right) \tag{2.31}$$

The small signal resistance r_Z generated in series to C_C is defined by the transconductances of transistors N_7 and P_7.

$$r_{\text{Z}} = \frac{1}{gm_{\text{N7}} + gm_{\text{P7}}} \approx \sqrt{\frac{k_{\text{I-Z}}}{2 \cdot I_{\text{OUT}}}} \cdot \frac{1}{\sqrt{K'_{\text{N}} \cdot \frac{W_{\text{N7}}}{L_{\text{N7}}}} + \sqrt{K'_{\text{P}} \cdot \frac{W_{\text{P7}}}{L_{\text{P7}}}}} \tag{2.32}$$

The open loop output resistance $r_{\text{ROUT-OL}}$ is dominated by the transconductance of the pass device N_{OUT}. As will be shown in the stability analysis in subsection 2.3.2 the pole at the output of the LVR is mainly defined by $r_{\text{ROUT-OL}}$ and the load capacitor C_{OUT}. The approximate frequency of the pole at the output is

$$\omega_{\text{P-OUT}} \approx \frac{1}{r_{\text{ROUT-OL}} \cdot C_{\text{OUT}}} \approx \frac{gm_{\text{NOUT}}}{C_{\text{OUT}}} = \frac{\sqrt{2 \cdot I_{\text{OUT}} \cdot K'_{\text{N}} \cdot \frac{W_{\text{NOUT}}}{L_{\text{NOUT}}}}}{C_{\text{OUT}}} \tag{2.33}$$

The zero $\omega_{\text{Z-T}}$ generated by the described circuit is

$$\omega_{\text{Z-T}} = \frac{1}{r_{\text{Z}} \cdot C_{\text{C}}} \approx \frac{\sqrt{2 \cdot I_{\text{OUT}}} \cdot \left(\sqrt{K'_{\text{N}} \cdot \frac{W_{\text{N7}}}{L_{\text{N7}}}} + \sqrt{K'_{\text{P}} \cdot \frac{W_{\text{P7}}}{L_{\text{P7}}}} \right)}{\sqrt{k_{\text{I-Z}}} \cdot C_{\text{C}}} \tag{2.34}$$

The ratio k_{PZ} between $\omega_{\text{Z-T}}$ and $\omega_{\text{P-OUT}}$ is a design parameter dependent constant and pole zero cancellation can be achieved by setting k_{PZ} to unity

$$k_{\text{PZ}} = \frac{\omega_{\text{Z-T}}}{\omega_{\text{P-OUT}}} = \frac{\sqrt{K'_{\text{N}} \cdot \frac{W_{\text{N7}}}{L_{\text{N7}}}} + \sqrt{K'_{\text{P}} \cdot \frac{W_{\text{P7}}}{L_{\text{P7}}}}}{\sqrt{k_{\text{I-Z}} \cdot K'_{\text{N}} \cdot \frac{W_{\text{NOUT}}}{L_{\text{NOUT}}}}} \cdot \frac{C_{\text{OUT}}}{C_{\text{C}}} \stackrel{!}{=} 1 \tag{2.35}$$

As explained, the current through N_7 and P_7 increases with the load current. To increase the current efficiency of the LVR the drain of P_7 is connected to the output. This means the current used to generate the load dependent resistor is not wasted but actively contributes to the output current. Unfortunately, the diode connected transistor N_7 generates at high frequencies a low ohmic connection over the compensation capacitor C_C directly to the gate of the pass device N_{OUT} (i.e. a low ohmic path between nodes V_{PRE1} and V_{GO}). This would compromise the PSRR of the LVR. Therefore, the gates of the transistors N_7 and N_8 are decoupled from the supply with a low pass filter composed of R_3 and C_3.

Slow error amplifier

The aim of the slow error amplifier is to adjust the two reference voltages V_{REF1} and V_{REF2} for the fast error amplifier. As its name indicates it has only a low bandwidth but it has high DC gain in the order of 60dB and low statistic offset. Therefore, a high DC accuracy for the output voltage of the LVR of below $\pm 1.5\%$ for ± 6 sigma can be achieved. The slow error amplifier is also built with thin oxide core transistors and is supplied by the preregulator 1. It has a similar topology like a two stage Miller compensated operational amplifier. The slow error amplifier not only defines the output voltage of the LVR but also defines the bias current in the input stage of the fast error amplifier. Therefore, the two

diode connected transistors N_{R0} and P_{R0} that are matched to the input transistors of the fast error amplifier N_0 and P_0 with a mirror ratio of 4 define the reference voltages V_{REF1} and V_{REF2}. This means the bias current in the input stage of the fast error amplifier is 4 times the bias current in the second stage of the slow error amplifier. The compensation capacitor C_{RC} has a value of 9pF. It is connected between the input of the second stage of the slow error amplifier and the center tap of the diode connected transistor stack consisting of N_{R0} and P_{R0}. It is essential to connect the capacitor to the center tap because the voltage of this node is the target value for the output voltage of the LVR. Transient noise like generated when switching between normal mode and low power mode can shift this target voltage to a wrong value. Due to the low speed of the slow error amplifier it would take a long time to recover the target voltage. The two capacitors C_1 and C_2 act as buffer capacitors for the reference voltages.

Core pass device

The block "Pass Device" in Figure 2.33 includes the actual pass device N_{OUT} but also the output current sensing transistor N_S and the cascoding transistor N_{CAS}. Controlling the gate of the pass device N_{OUT} with the error amplifier regulates the output voltage of the LVR. N_{CAS} limits the voltage drop across the drain source connections of N_{OUT}. This is necessary because the voltage on the preregulator output V_{PRE2} can reach up to 3V and result in a voltage drop of more than the rated voltage of 1.3V across N_{OUT}. Both, N_{OUT} and N_{CAS} have W/L dimensions of 4000μm/60nm. The width of the sensing transistor N_S is smaller by a factor of $B_{SEN} = 100$. Because it has the same gate source voltage as the pass device N_{OUT}, the current through N_S is proportional to the output current. This output current information is used in the fast error amplifier to generate the load dependent zero as shown before.

Stability analysis

The LVR has two parallel feedback paths. One feedback path is closed over the resistive feedback divider, the slow error amplifier, the fast error amplifier and the pass device. This loop allows high DC accuracy for the LVR output voltage. The second feedback path is closed only over the fast error amplifier and the pass device. This second loop ensures fast reaction to disturbances and fast settling of the LVR output voltage. Due to the parallel feedback structure of the error amplifiers a zero is generated in the transfer

function. The idea of combining a slow high gain amplifier with a low gain high speed amplifier has been proposed in [42]. The transfer function of the open loop A_{OL}, when opening the control loop at the gate of the pass device is

$$A_{\text{OL}} = \frac{A_{\text{SEA}} \cdot FB \cdot B \cdot gm_{\text{NOUT}} \cdot gm_0 \cdot r_{\text{DS2}} \cdot gm_4 \cdot r_{\text{DS4}}}{gm_{\text{NOUT}} + 2 \cdot A_{\text{SEA}} \cdot FB \cdot gm_0} \cdot \frac{\left(1 + \frac{s}{\omega_{\text{Z1}}}\right) \cdot \left(1 + \frac{s}{\omega_{\text{Z2}}}\right)}{\left(1 + \frac{s}{\omega_{\text{P1}}}\right) \cdot \left(1 + \frac{s}{\omega_{\text{P2}}}\right) \cdot \left(1 + \frac{s}{\omega_{\text{P3}}}\right)} \tag{2.36}$$

In this equation A_{SEA} is the voltage gain of the slow error amplifier, FB is the feedback divider ratio, B is the current mirror factor of the transistors N_1-N_2 (P_1-P_2). The transistors N_0 to N_4 are designed to have ideally the same electrical properties as P_0 to P_4. Therefore, gm_0 is the transconductance of N_0 and P_0, r_{DS2} is the drain source resistance of N_2 and P_2 and $gm_4 \cdot r_{DS4}$ is the gain due to the cascode transistors N_4 and P_4. For high load currents near the maximum of 200mA the voltage between the supply V_{PRE1} and the gate of the pass device decreases and the transistor P_4 won't act as a cascode anymore. The corner frequencies ω_{P1}, ω_{P2} and ω_{P3} are the three most relevant poles and ω_{Z1} and ω_{Z2} are the relevant zeros in the LVR system. The first zero is generated due to the parallel feedback structure

$$\omega_{\text{Z1}} = \frac{FB \cdot gm_{\text{PR1}}}{C_{\text{RC}}} \tag{2.37}$$

The second zero is generated in the fast error amplifier as discussed in section 2.3.2

$$\omega_{\text{Z2}} = \frac{gm_{\text{N7}} + gm_{\text{P7}}}{C_{\text{C}}} \tag{2.38}$$

The zero generated by the gate source capacitance of the pass device has been neglected since it lies significantly above the unity gain frequency (UGF) of the LVR.

The dominant pole of the control loop is

$$\omega_{\text{P1}} = \frac{gm_{\text{NOUT}} + 2 \cdot A_{\text{SEA}} \cdot FB \cdot gm_0}{C_{\text{OUT}} + C_{\text{RC}} \cdot A_{\text{SEA}} \cdot \frac{gm_{\text{NOUT}}}{gm_{\text{PR1}}}} \tag{2.39}$$

and for very high currents it approaches the low frequency pole determined by the Miller compensation in the slow error amplifier. This pole is followed by the zero generated due to the parallel feedback structure. C_{OUT} describes the sum of the distributed decoupling capacitance. The second pole

$$\omega_{\text{P2}} = \frac{1}{\left(\frac{r_{\text{DS2}} \cdot gm_4 \cdot r_{\text{DS4}}}{2} + \frac{1}{gm_{\text{N7}} + gm_{\text{P7}}}\right) \cdot C_{\text{C}}} \tag{2.40}$$

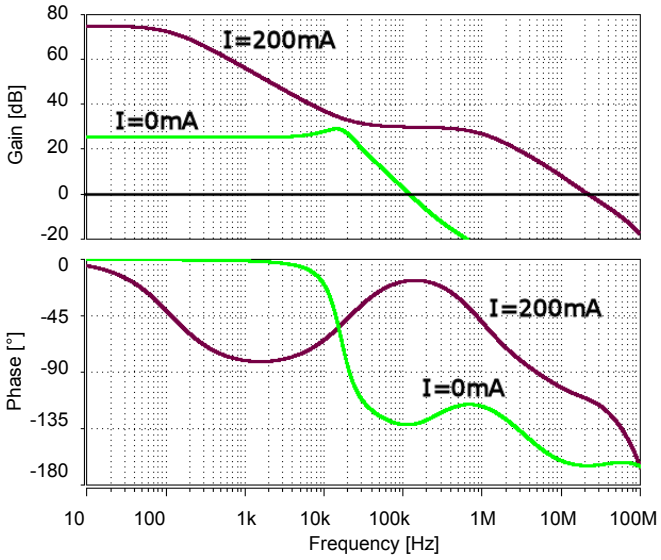

Figure 2.34: LVR open loop gain. The loop is opened at the gate of the pass device.

is mainly defined by the compensation capacitor in the fast error amplifier and the output resistance of the fast error amplifier. For very high currents the second pole is pushed to higher frequencies, since the transistor P_4 loses voltage headroom, therefore it isn't operated in saturation anymore and the gain $gm_4 \cdot r_{DS4}$ vanishes. Finally, the third pole

$$\omega_{P3} = \frac{gm_{NOUT}}{C_{OUT}} + \frac{gm_{PR1}}{C_{RC} \cdot A_{SEA}} \tag{2.41}$$

is strongly load dependent. To guarantee stability, the load dependent zero in Equation 2.38 that is generated with the compensation capacitor C_C tracks the third pole. As already mentioned the current through N_7 and P_7 is proportional to the load current. This allows the zero to track the third pole. For low load currents the poles and zeros approach each other. Simulation results for the loop gain analysis of the proposed LVR can be found in Figure 2.34. The low frequency small signal output resistance of the proposed LVR can be calculated as

$$r_{OUT} = \frac{1}{A_{SEA} \cdot FB \cdot B \cdot gm_{NOUT} \cdot gm_0 \cdot r_{DS2} \cdot gm_4 \cdot r_{DS4}} \tag{2.42}$$

Current consumption

From nominal simulations the shares are 150μA for the fast error amplifier, 6.5μA for the slow error amplifier, 2μA for the resistive voltage divider, 6.5μA for the preregulators without charge pump, 2μA for the load dependent compensation and the pass device gate

voltage limitation and 1μA result in from electro static discharge (ESD) protection circuit leakage. Overall the simulated nominal current consumption is 168μA plus the frequency dependent current of the charge pumps in the preregulators. Both charge pumps together consume approximately 3μA at 2MHz.

Low power mode

For switching between normal mode and low power mode the current mirror ratio between N_1-N_2 (and also P_1-P_2) can be selected. In normal mode the current mirror ratio is 5.5, while in low power mode the ratio is 1. Therefore, the current consumption of the fast error amplifier can be reduced by a factor of 3.25. Furthermore, the ratio of the input transistor of the fast error amplifier N_0 (P_0) to its replica in the slow error amplifier N_{R0} (P_{R0}) is switched at the same time from 4 to 2. This in turn reduces the current consumption of the fast error amplifier by another factor of 2. In total, this reduces the mode dependent current consumption of the fast error amplifier by a factor of 6.5. The mode dependent current consumption of the fast error amplifier is 150μA in normal mode and 23μA in low power mode. The rest of the LVR adds a constant current of 18μA to this mode dependent current. That results in a total current consumption of 168μA and 41μA, respectively.

2.3.3 On-Chip Test Loads

To be able to characterize the LVR, test loads have been placed on the same test chip. These test loads are a voltage controlled current source and a switched capacitive load.

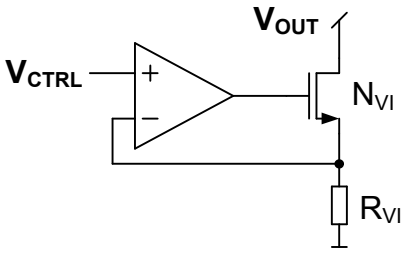

Figure 2.35: Voltage controlled current source

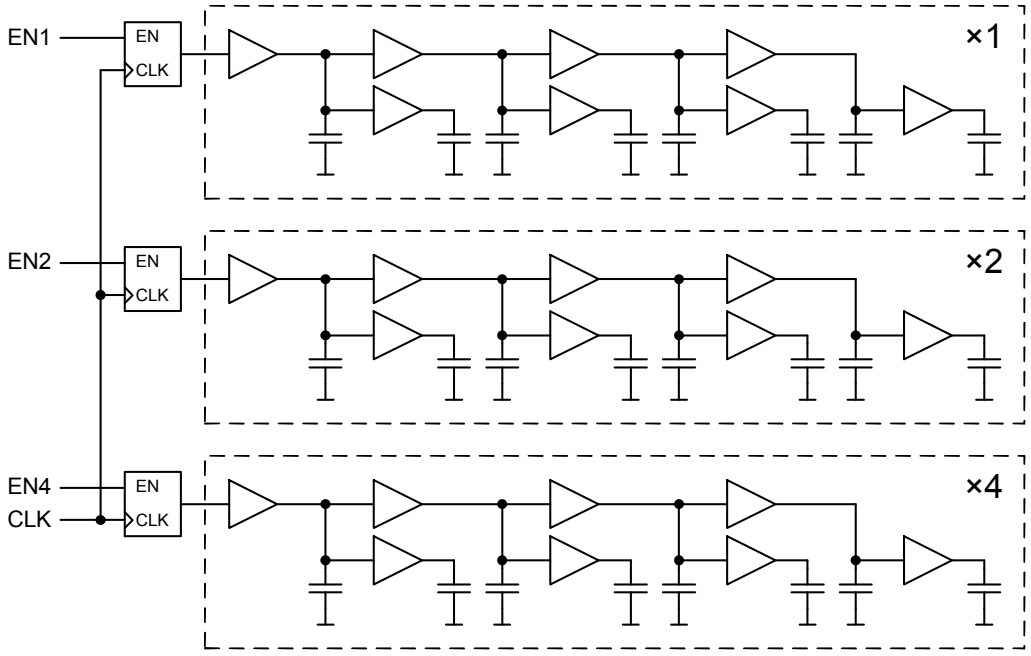

Figure 2.36: Controllable clocked capacitive load

Voltage controlled current source

The voltage controlled current source is used to generate defined load current slopes of up to 100mA/10ns for the LVR. Figure 2.35 shows the schematic of the voltage controlled current source. The amplifier is supplied by a dedicated pad to separate the current consumption of the test loads from the current consumed by the LVR itself. The drain of N_{VI} is the output of the voltage controlled current source and it is connected to the output node of the LVR V_{OUT}.

Clocked capacitive load

The clocked capacitive load is used to emulate the switching activity of a large digital block e.g. a microcontroller. The basic block of the clocked load can be seen in the dashed box in Figure 2.36. In total up to seven of these blocks can be activated dynamically in a binary weighted manner. One basic block consists of a four stage delay line with clock buffers and a total capacitance of 9pF. This means the maximum switched capacitance in the clocked capacitive load is 63pF. The clock buffers in this block are supplied by the output of the LVR to generate the load current.

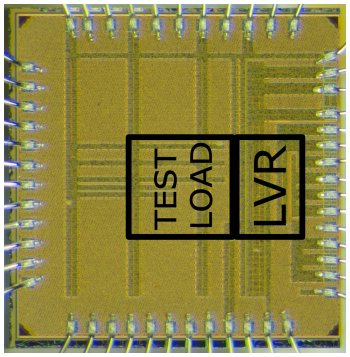

Figure 2.37: Die photo of the LVR test chip

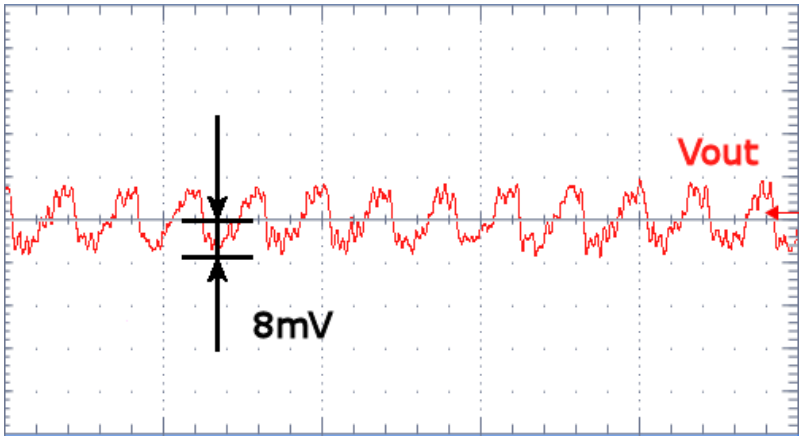

Figure 2.38: Transient load response with switching load. V_{OUT}: 10mV/div; t: 50ns/div

2.3.4 Measurement Results

The LVR has been fabricated on a 65nm digital CMOS process with flash memory. Because of the flash add-on also 5V capable transistors are available. A die photo of the LVR is depicted in Figure 2.37. The reference voltage for the LVR and the reference bias currents were supplied externally to the chip. A lumped 4.4nF poly-poly capacitor was placed on the test chip to emulate the distributed capacitive load of a microcontroller. The overall area of the test chip is 4mm^2 from which 0.21mm^2 are occupied by the LVR. The preregulator with ESD protection occupies about 60% of the LVR area. All measurements were performed at room temperature with a 100nF capacitor at the 5V supply pin of the LVR test chip and no external capacitor at the output. The transient load responses were generated with the on-chip test structures described before. Figure 2.38 shows the output voltage ripple generated by the switching activity of the clocked capacitive load. The DC voltage is 1.3V while the voltage undershoot is 8mV with the full load capacitance of 63pF switching at a frequency of 50MHz. The transient load response for a load current

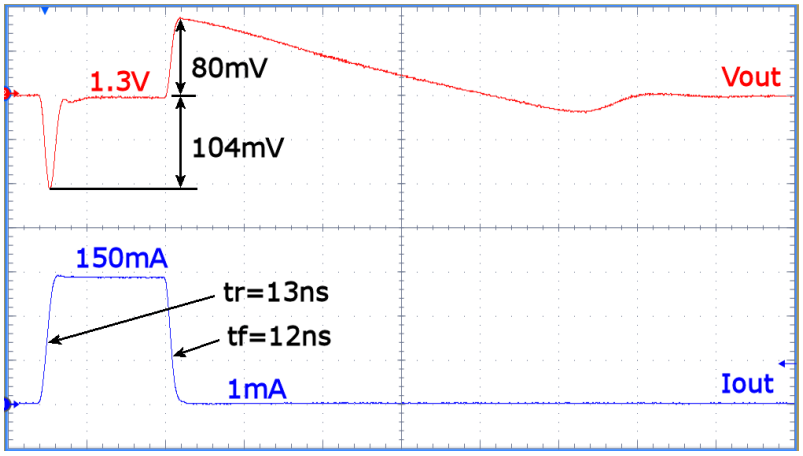

Figure 2.39: Transient load response; V_{OUT}: 50mV/div; I_{OUT}: ∼52mA/div; t: 100ns/div

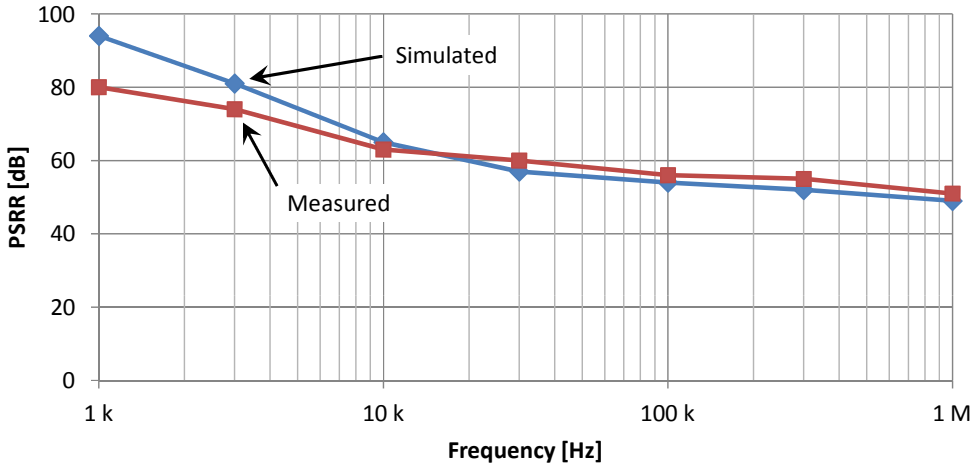

Figure 2.40: Measured and simulated PSRR of the LVR at I_{OUT}=100mA

jump from 1mA to 150mA with a rise time (10% - 90%) of 13ns is depicted in Figure 2.39. At the rising edge of the load current the voltage undershoot at the regulator output is only 104mV. The set point of the output voltage of 1.3V is reached again after approximately 60ns. For the falling edge of the load current the overshoot is even smaller with a value of 80mV. These fast load current slopes are generated with the on-chip voltage controlled current source. The result of the power supply rejection ration (PSRR) measurement is depicted in Figure 2.40. The PSRR was measured over a frequency range from 1kHz up to 1MHz and it stays above 50dB over the whole range. At 200mA load the minimum supply voltage for maintaining the output voltage at 1.3V is 2.07V i.e. the dropout voltage is 770mV. The overall current consumption was measured to be 176μA in total. From which 1μA is consumed by the charge pumps clocked at 10kHz. This

Table 2.5: Summary of the static properties of the improved capacitor-less LVR

Process	65nm digital flash CMOS
Active area for regulator	0.21mm^2
Supply voltage	2.07V - 5.5V
Output voltage	1.3V
Load current	0mA - 200mA
Static load regulation	17μV/mA
Static line regulation	435μV/V
Current consumption	176μA

Table 2.6: Comparison of the improved capacitor-less LVR with state of the art

Publication	[27]	[34]	[33]	[32]	[31]	This work
Year	2005	2012	2011	2010	2010	2012
Process	90nm CMOS	0.35μm CMOS	0.35μm CMOS	90nm CMOS	0.35μm CMOS	65nm CMOS
V_{IN} [V]	1.2	2.5-4	2.4-3.3	1.2	1.8-4.5	2.07-5.5
V_{OUT} [V]	0.9	2.35	2.2	1	1.6	1.3
$I_{OUT\text{-}MAX}$ [mA]	100	100	100	100	100	200
I_Q [μA]	6000	7	29.6	8	20	176
C_{LOAD} [pF]	600	100	100	50	100	4400
Area [mm^2]	0.008	0.064	0.103	0.019	0.145	0.21
ΔV_{OUT} [mV]	90	236	62	114	97	104
$\Delta I/\Delta t$ [mA/ns]	0-100/0.1	0.05-100/500	0-100/250	3-100/100	0-100/100	1-150/16

means the measured value of the quiescent current is 7μA higher than the nominal simulated value. The current consumption in low power mode was measured to be 42μA. A summary of the static performance properties of the capacitor-less LVR test chip can be found in Table 2.5.

2.3.5 Comparison with State of the Art

Most state of the art capacitor-less LVRs with a comparable output current range are designed for load current jumps from low load to full load within 1μs to 100ns [31–34]. This results in a maximum load current slope of 100mA/1μs up to 100mA/100ns. For such a full load jump the output voltage deviation is in the order of 10% of the nominal output voltage. Table 2.6 gives a detailed comparison. There is one exception in this table. The LVR in [27] can handle a full load current jump within only 100ps. But this regulator consumes 6mA quiescent current. The typical current consumption for the other regulators in the table is in the range of 7μA to 30μA.

The advantage of the LVR presented in this work is that it can handle much faster load

current slopes than [31–34]. For an output voltage deviation of 8% of the nominal output voltage the presented LVR can handle a load jump from 1mA to 150mA within 16ns. This is a load current slope of almost 100mA/10ns while consuming 176μA. Only [27] can handle load jumps that are fast but at a 40 times higher quiescent current. Furthermore, the presented LVR can also withstand input voltages of up to 5.5V. Some fast LVRs take advantage of thin oxide core transistors at the cost of limiting the maximum input voltage [27, 32]. On the other hand the here presented LVR has a significant dropout voltage of 770mV.

2.4 Smart ESD Protection for the Linear Voltage Regulator

The electro static discharge (ESD) protection discussed in this section was developed for the linear voltage regulator (LVR) presented in section 2.3 but of course it is not limited to this topology. It is intended to protect both, the pass device itself and the intermediate node between the slow preregulator and the fast main regulator. This ESD protection has been documented 2012 in [46].

2.4.1 Technical Problem

Typically linear voltage regulators connect the external supply of a system on chip (SoC) with internally generated supplies of a lower voltage. Of course there has to be an adequate ESD clamp on chip at the external supply node that protects all devices on this node. Because at the internally generated supply, devices of a lower voltage class than the external supply are typically used, an additional adequate ESD protection is needed at the internal node. In such a case the devices on both supply nodes are protected from electrical over stress (EOS). But if the pass device comes into a conductive state due to coupling over parasitics like the gate drain capacitance due to the fast transients during the ESD event, then part of or even almost the whole ESD current could flow over the pass device. As described in [47, chapter 6.4] this coupling to the gate of a MOS transistor can decrease its breakdown voltage during the ESD event. Due to inhomogeneous current distribution over the width of the pass device a hot spot can occur and destroy the pass device. Therefore, it must be guaranteed that during an ESD event the current through the pass device of the LVR can't exceed a destructive level. Two well known solutions exist for protecting the pass device and the circuitry connected to the internal supply:

a) One solution is to use silicide blocked layout for the pass device. This makes it self-protecting, a specified minimal total width of the pass device and a maximum finger width presumed. The pass device can then carry the whole ESD current because the additional drain resistance of the non silicided MOS transistor forces the current to be distributed uniformly over the total width [47]. At the output of the linear voltage regulator a full size ESD protection of the respective voltage class is needed. This ESD protection is needed to ensure a voltage clamping below the destruction level of the connected circuitry in case of an ESD event, if the complete ESD current is forced through the pass device to the output. This is the standard solution and it can be used for both types of linear voltage regulators where the output is an external pin or only an internal node.

b) Another significantly more area efficient solution exists. But it is only allowed in case the output of the linear voltage regulator has no connection to an external pin. A keep-off circuit needs to be included to switch off the pass device during an ESD event. For example an RC-element can be used to detect an ESD pulse on the supply and force the pass device to be non-conducting. This allows the current through the LVR pass device to be limited. In turn the pass device doesn't need to have silicide blocked layout. Due to the current limitation, the ESD protection at the output of the linear voltage regulator can be much smaller and still protect the circuitry in the lower voltage domain.

For the target application, none of the two described existing solutions is applicable. The circuitry connected to the output of the preregulator contains core devices, while the voltage level at the preregulator output is above core supply level and does not allow the use of a standard ESD clamp for core devices. For this node an ESD protection using devices of a higher voltage level is needed. At the same time it must be ensured that a very low clamping voltage during an ESD event is not exceeded to ensure the protection of the very sensitive core devices. This is possible by limiting the current through the pass device during an ESD event using an RC-triggered keep-off circuit as described in b).

The problem with this solution is that noise on the power supply could trigger the keep-off circuit in normal operation. Such power supply noise can be ringing caused by switching mode power supplies or DPI (direct power injection)-stress applied during tests in automotive systems. If such noise triggers the keep-off circuit, then the performance

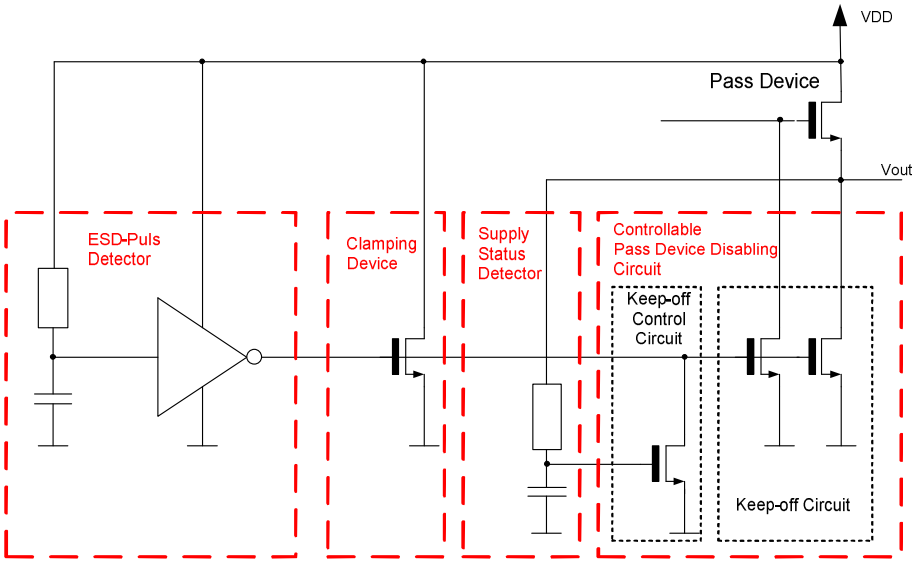

Figure 2.41: Concept of the smart ESD protection

of the linear voltage regulator will be degraded. It can even happen that the regulator is switched off completely during normal operation. That of course would stop the product from working.

2.4.2 Implementation

This solution proposes to use a smart keep-off circuit to control the pass device. This smart keep-off circuit can be disabled during normal operation. This combination allows in general the implementation of the very area efficient solution as described in subsection 2.4.1 b), even in case noise on the supply is present. The idea behind this is following: ESD events can occur during handling, manufacturing or assembly of integrated circuits (IC). During these steps the devices are always unpowered. But when the IC is in operation it is generally already mounted on a printed circuit board (PCB) in a system. There system level ESD protection is generally present which typically does not rely on the on-chip ESD protection. The smart keep-off circuit detects the system status of the IC (i.e. supplied or unsupplied) and disables the keep-off circuit in case the chip is in a safe power-up status to avoid malfunction during operation. An implementation example of such a smart ESD protection can be seen in Figure 2.41. The design target is to make the test chip for the improved capacitor-less LVR robust against ESD pulses according to the human body model (HBM) [48] up to 2kV (class 2). Also ESD robustness according to the charged device model (CDM) [49] up to 1kV (class III) will be tested. This means

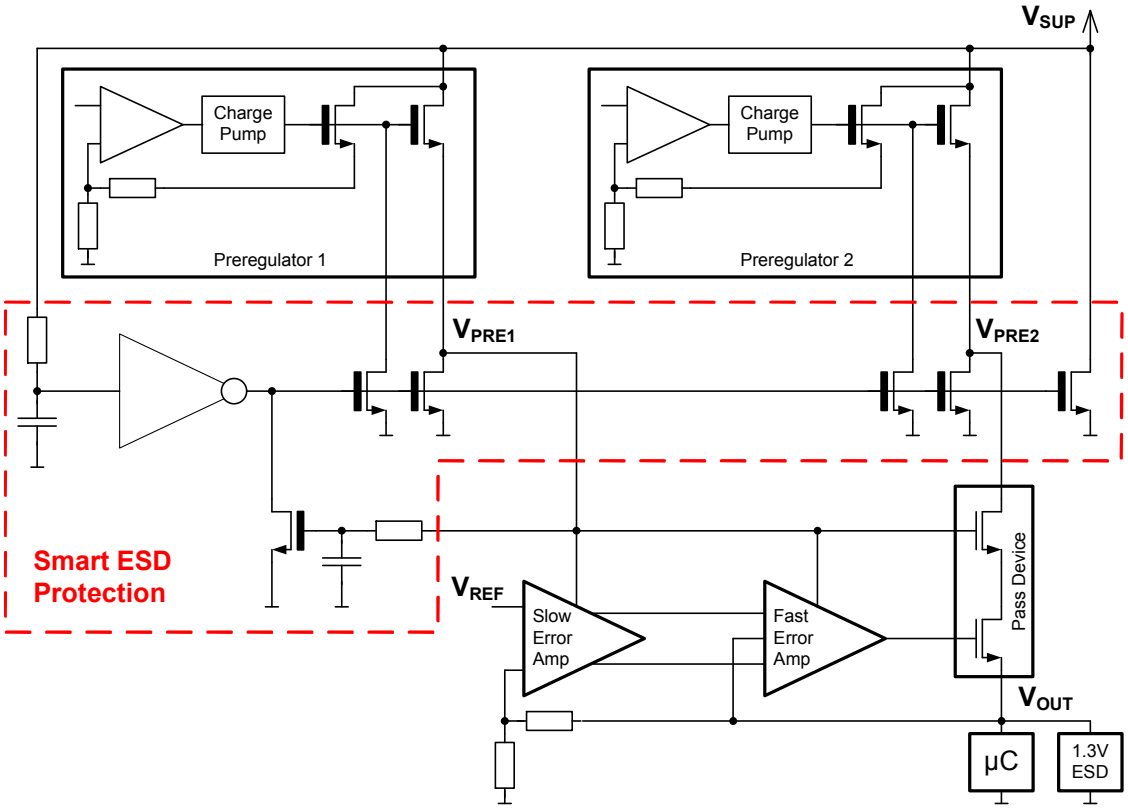

Figure 2.42: Smart ESD protection inside the LVR

that not only the discussed ESD protection has to be included. It only protects the pass device over its drain-source connection and the output of the preregulator. Of course also the supply pins with external connection have to be protected for their respective voltage class. These are the main supply V_{SUP} with a 5V-class ESD clamp and the output of the fast regulator V_{OUT} with a 1.3V-class ESD clamp. For these pins standard ESD clamps from a library have been used. An overview schematic of the capacitor-less LVR incorporating the described smart ESD protection is given in Figure 2.42.

2.4.3 Functional Verification

The concept of the discussed smart ESD protection has been implemented in a 65nm digital CMOS process with flash memory as part of the improved capacitor-less linear voltage regulator in section 2.3. For verifying the functionality of the proposed ESD protection 16 samples of the linear voltage regulator test chip have been verified for their voltage regulation functionality and their current consumption. All samples have been labeled and afterwards each sample has been exposed to defined ESD stress. To find out

Table 2.7: Summary of the ESD results of the improved capacitor-less LVR

Sample no.	ESD test type	Stress voltage	Comment	Status
1	CDM	250V		pass
2	CDM	250V		pass
3	CDM	500V		pass
4	CDM	500V		pass
5	CDM	750V		pass
6	CDM	750V		pass
7	CDM	1kV		pass
8	CDM	1kV		pass
9	HBM	1kV		pass
10	HBM	1kV		pass
11	HBM	1.5kV		pass
12	HBM	1.5kV		pass
13	HBM	2kV	not tested	x
14	HBM	2kV		pass
15	HBM	2.5kV		fail
16	HBM	2.5kV		fail

the limit of the ESD protection eight groups of ESD stress scenarios were tested with two samples in each group. ESD stress according to the charged device model (CDM) from 250V to 1kV and ESD stress according to the human body model (HBM) with voltages from 1kV to 2.5kV was tested.

Table 2.7 shows the result of the ESD tests. As can be seen all samples tested with the CDM up to the maximum tested voltage of 1kV passed the ESD test. That means no difference in the quiescent current and the output voltage of the LVR was observed after the ESD stress. The samples no. 9 thru 12 which were stressed with up to 1.5kV in the HBM also passed the test. So did sample no. 14 with 2kV HBM. Unfortunately, sample no. 13 could not be tested, since it was destroyed mechanically during shipment to the ESD lab. The only two test cases where ESD stress measurably damaged the circuit were the two 2.5kV HBM samples. The damage was identified due to an increased current consumption of the circuit after the ESD stress. The current consumption was increased by several 100μA compared to the first measurement.

At least all tested samples up to the designed ESD robustness of 2kV HBM passed the test. As a proof of concept this is acceptable. For a safe proof of course tests with more samples need to be done.

3 Conclusion

3.1 Further Work

3.1.1 Digitally Controlled Linear Voltage Regulator

The implementation of the digitally controlled low dropout linear voltage regulator (LDO) presented in section 2.1 showed the desired results. Further work on this topic could address advanced non-linear control techniques that can be implemented in a digital controller. Due to such advanced control algorithms the regulator performance could be further improved on the one hand. On the other hand the sampling frequency and subsequently the quiescent current of the system could be decreased while maintaining the same regulator performance. In switched mode power supplies (SMPS) non-linear control techniques like sliding-mode control are already in the focus of academia e.g. in [50]. Additionally, improvements in the current efficiency of the digitally controlled LDO could be researched due to optimized analog to digital converter (ADC) and digital to analog converter (DAC) topologies for that specific use case. Also sophisticated low power modes that involve not only the clocking frequency but also a reconfigurable ADC and DAC structures are highly desirable. Another topic that has not been covered within this thesis is the electromagnetic interference (EMI) produced by the digitally controlled LDO.

3.1.2 Capacitor-Less Linear Voltage Regulator

Two output capacitor-less linear voltage regulator (LVR) structures have been investigated in an evolutionary approach by designing the second LVR in section 2.3 based on an extension of the first LVR in section 2.2. The final results of the improved capacitor-less LVR showed excellent dynamic performance. One of the main disadvantages of both capacitor-less LVRs is the absence of the low dropout capability. Using a PMOS pass device is the classical solution for achieving the low dropout capability. Since the error

amplifier utilized has an inverting behavior from the feedback input to the output at the gate of the pass device, no PMOS pass device can be used here. One possibility to include the desired low dropout capability would be generating a DC shift between the output of the error amplifier and the gate of the pass device by means of a precharged capacitor as reported in [51]. Such an implementation doesn't need a charge pump that needs to supply the full bias current of the error amplifier but only a very low current for keeping the voltage constant across the shifting capacitor. Combining the fast response of the error amplifier in section 2.3 with the low dropout capability would be highly desirable.

3.2 Conclusion

In this thesis alternative concepts for linear voltage regulators have been investigated. These concepts were enabled by the utilization of a deep sub-micron 65nm CMOS process. In older process technologies utilizing significantly larger feature sizes they would have not been efficient in terms of area consumption or quiescent current. On the first test chip presented in section 2.1 there has been a fully digitally controlled LDO implemented. At the time when designing this LDO no publication of such a digitally controlled LDO was found except one talk without paper. Implementing a digital control loop for a typically small circuit like an LDO would have been quite area consuming and therefore costly in e.g. an old 1μm CMOS process. The measurements on the test chip of the digitally controlled LDO have shown good performance comparable to state of the art analog LDOs. Additional to achieving this performance, specific advantages of the digital implementation can be exploited. Among these is easy portability of the controller between technologies due to HDL based design. Also non-linear signal manipulations can be implemented easily. An output capacitor-less LVR has been designed for the second test chip as described in section 2.2. A 150pF on-chip load capacitor has been placed which is reasonably small in the used 65nm CMOS process. With the introduced error amplifier fast transient disturbances can be suppressed. Measurements on this test chip showed fast load response, high DC accuracy and high stability. The third test chip has been used to verify the design of the improved version of a capacitor-less LVR in section 2.3. In the field application the LVR will only see the load capacitance of a microcontroller core that can be quite high. For the target application this load capacitance is in the range of 5nF. Due to the flash memory add-on of the used 65nm CMOS process for this test chip also a high input voltage of up to 5.5V can be tolerated. Measurement results have shown excellent performance. Compared with state of the art capacitor-less LVRs the presented LVR is among the fastest. For this LVR also an optimized ESD protection has been developed and tested according to standardized ESD stress. HBM robustness up to 2kV and CDM robustness up to 1kV has been achieved with the test chip.

Own Publications

[E1] G. Maderbacher, **T. Jackum**, W. Pribyl, and C. Sandner, "A sensor concept for minimizing body diode conduction losses in DC/DC converters," in *European Solid State Circuit Conference (ESSCIRC)*, September 2010, pp. 442–445.

[E2] **T. Jackum**, G. Maderbacher, W. Pribyl, and R. Riederer, "Fast capacitor free linear voltage regulator in a 65 nm CMOS technology for supplying digital processors," in *Austrochip*, October 2010, pp. 1–5.

[E3] **T. Jackum**, G. Maderbacher, W. Pribyl, and R. Riederer, "A digitally controlled linear voltage regulator in a 65nm CMOS process," in *International Conference on Electronics, Circuits and Systems (ICECS)*, December 2010, pp. 982–985.

[E4] **T. Jackum**, G. Maderbacher, W. Pribyl, and R. Riederer, "Fast transient response capacitor-free linear voltage regulator in 65nm CMOS," in *International Symposium on Circuits and Systems (ISCAS)*, May 2011, pp. 905–908.

[E5] G. Maderbacher, **T. Jackum**, W. Pribyl, and C. Sandner, "Output stage topologies of DC-DC buck converters operating up to 5 V supply voltage in 65 nm CMOS," in *Conference Ph.D. Research in Microelectronics and Electronics (PRIME)*, July 2011, pp. 105–108.

[E6] G. Maderbacher, **T. Jackum**, W. Pribyl, S. Michaelis, D. Michaelis, and C. Sandner, "Fast and robust level shifters in 65 nm CMOS," in *European Solid State Circuit Conference (ESSCIRC)*, September 2011, pp. 195–198.

[E7] G. Maderbacher, **T. Jackum**, W. Pribyl, M. Wassermann, A. Petschar, and C. Sandner, "Automatic dead time optimization in a high frequency DC-DC buck converter in 65 nm CMOS," in *European Solid State Circuit Conference (ESSCIRC)*, September 2011, pp. 487–490.

[E8] P. Faragó, **T. Jackum**, C. Böhm, and M. Hofer, "Illustration of automatic digital synthesis for Camellia-128 cipher algorithm," *Acta Technica Napocensis - Electronics and Telecommunications*, vol. 53, no. 1, pp. 21–24, March 2012.

[E9] **T. Jackum**, G. Maderbacher, and W. Pribyl, "Considerations for replacing conventional LVRs with output capacitor free LVRs," in *Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, June 2012, pp. 83–86.

[E10] **T. Jackum**, F. Praemassing, G. Maderbacher, R. Riederer, and W. Pribyl, "Capacitor-less LVR for a 32-bit automotive microcontroller SoC in 65nm CMOS," in *European Solid State Circuit Conference (ESSCIRC)*, September 2012, pp. 329–332.

[E11] **T. Jackum**, G. Maderbacher, R. Riederer, and W. Pribyl, "Output current limitation in a digitally controlled low dropout linear voltage regulator," in *Austrochip*, October 2012, pp. 71–75.

Invention Disclosures

[ID1] T. Santa, **T. Jackum**, and C. Lindholm, “A synchronous control loop speed-up triggered by an asynchronous event,” December 2009, Invention Disclosure.

[ID2] E. Thaler, T. Santa, and **T. Jackum**, “Settling time reduction of linear voltage regulators,” October 2010, Invention Disclosure.

[ID3] G. Maderbacher and **T. Jackum**, “EMI improvement for DC-DCs by lossless smoothing of current and voltage waveforms (original: EMV Verbesserung bei DC-DCs durch verlustfreies Glätten der Strom- und Spannungsverläufe),” April 2011, Invention Disclosure.

[ID4] **T. Jackum**, F. Praemassing, A. Missoni, E. Bach, and S. Berger, “Capless linear voltage regulator,” July 2011, Invention Disclosure.

[ID5] **T. Jackum**, F. Praemassing, A. Missoni, E. Bach, and S. Berger, “Digitally assisted linear voltage regulator,” July 2011, Invention Disclosure.

[ID6] **T. Jackum**, D. Alvarez, C. Kupfer, and F. Praemassing, “Smart ESD protection of LDOs which prevents functional fail during operation,” February 2012, Invention Disclosure.

[ID7] **T. Jackum**, N. Da Dalt, and A. Cristofoli, “LDO with output voltage adjustable lower or higher than the reference voltage,” January 2013, Invention Disclosure.

Bibliography

[1] "MAX8884Y/MAX8884Z: 700mA DC-DC step-down converters with dual 300mA LDO in 2mm x 2mm CSP," Maxim Integrated Products, Datasheet, 2010.

[2] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York: Kluwer Academic Publishers, 2001.

[3] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Transactions Power Electronics*, vol. 23, no. 2, pp. 841–851, March 2008.

[4] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, September 2011.

[5] H.-P. Le, M. Seeman, S. R. Sanders, V. Sathe, S. Naffziger, and E. Alon, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm2 at 81% efficiency," in *International Solid State Circuit Conference (ISSCC)*, February 2010, pp. 210–211.

[6] "MAX1730: 50ma regulated step-down charge pump for 1.8v or 1.9v logic," Maxim Integrated Products, Datasheet, 2000.

[7] M. D. Seeman, "A design methodology for switched-capacitor DC-DC converters," Ph.D. dissertation, Electrical Engineering and Computer Sciences, University of California at Berkeley, May 2009.

[8] B. S. Lee, "Technical review of low dropout voltage regulator operation and performance," Texas Instruments, Application report, August 1999.

[9] "PUMA Final Report," Infineon Technologies Austria AG and Graz University of Technology, Research Report, 2011.

[10] G. F. Franklin, J. D. Powell, and M. L. Workman, *Digital Control of Dynamic Systems*, 3rd ed. California: Addison Wesley Longman Inc., 1998.

[11] Y.-S. Hwang, M.-S. Lin, B.-H. Hwang, and J.-J. Chen, "A 0.35um CMOS sub-1V low-quiescent-current low-dropout regulator," in *Asian Solid-State Circuits Conference (APPCAS)*, November 2008, pp. 153–156.

[12] R. Min, T. Furrer, and A. Chandrakasan, "Dynamic voltage scaling techniques for distributed microsensor networks," in *IEEE Computer Society Workshop on VLSI*, April 2000, pp. 43–46.

[13] N. R. Miller, "A digitally controlled switching regulator," in *IEEE PESC*, June 1977, pp. 142–147.

[14] C.-T. Chen, *Analog & Digital Control System Design*. Orlando: Saunders College Publishing, 1993.

[15] B. C. Kuo, *Digital Control Systems*, 2nd ed. New York: Oxford University Press, 1992.

[16] T. Jackum, G. Maderbacher, and W. Pribyl, "Considerations for replacing conventional LVRs with output capacitor free LVRs," in *Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, June 2012, pp. 83–86.

[17] V. Gupta, G. A. Rincon-Mora, and P. Raha, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," in *International SOC Conference (SOCC)*, September 2004, pp. 311–315.

[18] T. Jackum, G. Maderbacher, W. Pribyl, and R. Riederer, "A digitally controlled linear voltage regulator in a 65nm CMOS process," in *International Conference on Electronics, Circuits and Systems (ICECS)*, December 2010, pp. 982–985.

[19] S.-H. Lu, W.-J. Huang, and S.-I. Liu, "A fast settling low dropout linear regulator with single miller compensation capacitor," in *Asian Solid-State Circuits Conference (ASSCC)*, November 2005, pp. 153–156.

[20] M. Lüders, B. Eversmann, J. Gerber, K. Huber, R. Kuhn, D. Schmitt-Landsiedel, and R. Brederlow, "A fully-integrated system power aware LDO for energy harvesting applications," in *Symposium on VLSI Circuits (VLSIC)*, June 2011, pp. 244–245.

[21] P. Hazucha, S. T. Moon, G. Schrom, F. Paillet, D. Gardner, S. Rajapandian, and T. Karnik, "High voltage tolerant linear regulator with fast digital control for biasing of integrated DC-DC converters," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 66–73, January 2007.

[22] F. Praemassing, F. Schmidt, and J. Schaefer, "A digitalized embedded linear voltage regulator for providing the power supply for 8-, 16- and 32-bit microcontrollers," September 2008, talk at Kleinheubacher Tagung.

[23] J.-J. Chen, M.-S. Lin, H.-C. Lin, and Y.-S. Hwang, "Sub-1V capacitor-free low-power-consumption LDO with digital controlled loop," in *Asia Pacific Conference on Circuits and Systems (APCCAS)*, November 2008, pp. 526–529.

[24] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw Hill, 2001.

[25] T. Jackum, G. Maderbacher, W. Pribyl, and R. Riederer, "Fast transient response capacitor-free linear voltage regulator in 65nm CMOS," in *International Symposium on Circuits and Systems (ISCAS)*, May 2011, pp. 905–908.

[26] T. Jackum, F. Praemassing, G. Maderbacher, R. Riederer, and W. Pribyl, "Capacitor-less LVR for a 32-bit automotive microcontroller SoC in 65nm CMOS," in *European Solid State Circuit Conference (ESSCIRC)*, September 2012, pp. 329–332.

[27] P. Hazucha, T. Karnik, B. Bloechel, C. Parsons, D. Finan, and S. Borkaret, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 933–940, April 2005.

[28] Y. Lam, W. Ki, and C. Tsui, "Adaptively-biased capacitor-less CMOS low dropout regulator with direct current feedback," in *Asia and South Pacific Conference on Design Automation (ASP-DAC)*, January 2006, pp. 104–105.

[29] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok, and M. Chan, "Development of single-transistor-control LDO based on flipped voltage follower for SoC," *IEEE Transactions on Circuits and Systems I*, vol. 55, no. 5, pp. 1392–1401, June 2008.

[30] P. Or and K. Leung, "An output-capacitorless low-dropout regulator with direct voltage-spike detection," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 458–466, February 2010.

[31] E. Ho and P. Mok, "A capacitor-less CMOS active feedback low-dropout regulator with slew-rate Enhancement for portable on-chip application," *IEEE Transactions on Circuits and Systems II*, vol. 57, no. 2, pp. 80–84, February 2010.

[32] J. Guo and K. Leung, "A 6uW chip-area-efficient output-capacitorless LDO in 90-nm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1896–1905, September 2010.

[33] E. Ho and P. Mok, "Design optimization of an output capacitor-less low dropout regulator with compensation capacitance reduction and slew-rate enhancement technique," in *International Symposium on Circuits and Systems (ISCAS)*, May 2011, pp. 53–56.

[34] X. Ming, Q. Li, Z. Zhou, and B. Zhang, "An ultrafast adaptively biased capacitorless LDO with dynamic charging control," *IEEE Transactions on Circuits and Systems II*, vol. 59, no. 1, pp. 40–44, January 2012.

[35] T. Jackum, G. Maderbacher, R. Riederer, and W. Pribyl, "Output current limitation in a digitally controlled low dropout linear voltage regulator," in *Austrochip*, October 2012, pp. 71–75.

[36] C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kuttner, "A 6-bit 1.2-GS/s low-power flash-ADC in 0.13um digital CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 7, pp. 1499–1505, July 2005.

[37] F. Kuttner, H. Habibovic, T. Hartig, M. Fulde, G. Babin, A. Santner, P. Bogner, C. Kropf, H. Riesslegger, and U. Hodel, "A digitally controlled DC-DC converter for SoC in 28nm CMOS," in *International Solid State Circuit Conference (ISSCC)*, February 2011, pp. 384–385.

[38] M. Al-Shyoukh, R. A. Perez, and H. Lee, "A Transient-enhanced 20uA-quiescent 200mA-load low-dropout regulator with buffer impedance attenuation," in *Custom Integrated Circuits Conference (CICC)*, Sptember 2006, pp. 615–618.

[39] K. Wong and D. Evans, "A 150mA low noise, high PSRR low-dropout linear regulator in 0.13um technology for RF SoC Applications," in *European Solid State Circuit Conference (ESSCIRC)*, September 2006, pp. 532–535.

[40] T. Jackum, G. Maderbacher, W. Pribyl, and R. Riederer, "Fast capacitor free linear voltage regulator in a 65 nm CMOS technology for supplying digital processors," in *Austrochip*, October 2010, pp. 1–5.

[41] A. H. Rodrigues-Neves, "A capacitor-less low dropout voltage regulator for small analog cores," Master thesis, Technical University of Lisbon, Lisbon, October 2007.

[42] M. Kayal, F. Vaucher, and P. Deval, "New error amplifier topology for low dropout voltage regulators using compound OTA-OPAMP," in *European Solid State Circuit Conference (ESSCIRC)*, September 2006, pp. 536–539.

[43] B. Kamath, R. Meyer, and P. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 9, no. 6, pp. 347–352, December 1974.

[44] W. Leung, T. Man, W. Chan, and M. Chan, "A high precision, output-capacitor-free low-dropout regulator for system-on-chip design," in *International Symposium on Circuits and Systems (ISCAS)*, May 2008, pp. 2242–2245.

[45] J.-T. Wu and K.-L. Chang, "MOS charge pumps for low-voltage operation," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 592–597, 1998.

[46] T. Jackum, D. Alvarez, C. Kupfer, and F. Praemassing, "Smart ESD protection of LDOs which prevents functional fail during operation," 2012, Invention Disclosure.

[47] A. Ameraseker and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd ed. West Sussex: John Wiley & Sons, 2002.

[48] *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, JEDEC Solid State Technology Association Std. JESD22-A114, Rev. E, January 2007.

[49] *Field-Induced Charged-Device Model Test Method for Electrostatic- Discharge-Withstand Thresholds of Microelectronic Components*, JEDEC Solid State Technology Association Std. JESD22-C101, Rev. E, December 2009.

[50] M. Agostinelli, R. Priewasser, S. Marsili, and M. Huemer, "Non-linear control for energy efficient DC-DC converters supporting DCM operation," in *International Midwest Symposium on Circuits and Systems (MWSCAS)*, August, 2010, pp. 1153–1156.

[51] D. Camacho, P. Gui, and P. Moreira, “Fully on-chip switched capacitor NMOS low dropout voltage regulator,” *Springer Journal of Analog Integrated Circuits and Signal Processing*, vol. 65, no. 1, pp. 141–149, October 2010.