Low Power Wireless Receiver Frontends for Sensor Network Applications

Dipl.-Ing. Markus Dielacher

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Graz University of Technology

institut für elektronik

Institute of Electronics

Supervisor: .....
Univ.-Prof. Dipl.-Ing. Dr. techn. Wolfgang Pribyl

Co-Supervisor: .....
Prof. Dr. ir. Willy Sansen
(Katholieke Universiteit, Leuven, Belgium)

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Kurzfassung

Immer mehr Anwendungen, von der Kontrolle von Körperfunktionen und diversen Umweltparametern bis hin zu Funktionen im Automobil- und Flugzeugsektor basieren heutzutage auf Sensornetzwerken. Aufgrund dieses breiten Spektrums von Anwendungen können auch die Anforderungen an solche Netzwerke sehr unterschiedlich sein, je nachdem ob es sich um reine Komfortfunktionen handelt, oder um sicherheitskritische Anwendungen. Die Lebensdauer, und damit verbunden die Leistungsaufnahme, sind mitunter die größten Hürden in der Entwicklung von Sensorknoten, die an unzugänglichen Orten installiert werden, wo ein Austausch von Batterien schwierig oder unmöglich ist. In sternförmigen Netzwerken, in denen die einzelnen Sensorknoten lediglich Informationen senden, ohne Nachrichten zu empfangen, ist diese Problematik ein wenig entspannter. Die Sender sind die meiste Zeit in einem inaktiven Stromsparmodus, aus dem sie nur von Zeit zu Zeit erwachen, um eine Messung durchzuführen und die ermittelten Daten an einen zentralen Knoten zu senden. Dieser zentrale Knoten ist der einzige, der permanent aktiv auf eine Übertragung wartet und kann mithilfe einer leistungsstarken Energiequelle betrieben werden. Ganz anders sieht es in wirklich autonomen Sensornetzwerken aus. In solchen Netzen kann jeder Knoten Daten empfangen und an seine Nachbarn weiterübermitteln, bis sie schließlich an ihrem Bestimmungsort angelangt sind. Diese Arbeit beschreibt einen miniaturisieren Sensorknoten für Anwendungen im Automobilbereich, wobei der Schwerpunkt der Arbeit auf den Empfängerschaltungen liegt. Sowohl der Sender, als auch der Empfänger beruhen auf der Verwendung von sogenannten BAW Resonatoren zur Erzeugung einer Referenzfrequenz. Diese sind kleiner und robuster als herkömmliche Quarzkristalle. Dies ist wichtig, da die Überwachung des Reifendrucks als exemplarische Anwendung ausgewählt wurde. Im Gegensatz zu herkömmlichen Modulen zur Reifendruckkontrolle, die auf der Felge montiert sind, werden die in dieser Arbeit vorgestellen Sensorknoten direkt an der Lauffläche befestigt, wo sie enormen Beschleunigungen standhalten müssen. Daher sind auch die Abmessungen auf 1 cm^3 limitiert, um Gradienten in den einwirkenden Kräften aufgrund von Verformungen zu vermeiden. In dieser Arbeit wird die Architektur der Sensorknoten vorgestellt. Eine geeignete Empfängerarchitektur wird entwickelt, und ein rauscharmer Verstärker mit filternden Eigenschaften wird gezeigt. Diese Filterung erfolgt wieder mit BAW Resonatoren. Um eine ausreichend niedrige Leistungsaufnahme zu erzielen genügt es nicht, die einzelnen Schaltungen zu optimieren, auch die Kommunikatinonsprotokolle und Ablaufsteuerung müssen speziell für die Anwendung angepasst werden. In dieser Arbeit wird gezeigt wie mit der verwendeten BAW basierten Architektur die niedrigste Leistungsaufnahme erzielt werden kann. Schlussendlich werden einige Technologien vorgestellt, die verwendet werden um einen dreidimensionalen miniaturisieren Aufbau zu ermöglichen.

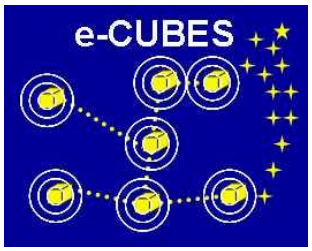
Abstract

Today sensor networks are emerging in various fields, from fitness and health monitoring, environmental monitoring to automotive and aeronautic applications. Due to the broad range of applications, also the requirements may differ significantly, from safety-critical to pure comfort features. Lifetime and therefore power consumption are among the most important obstacles to overcome in order to establish sensor networks in hostile places where batteries cannot be replaced. This issue is a bit relaxed when star-topology networks are used where the individual nodes only transmit data according to a certain schedule and can be switched off most of the time. In those networks there is only one central node which is connected to a high capacity power supply and listening for incoming messages. In truly autonomous sensor networks however, each sensor node contains a receiver and a transmitter, such that it can receive messages and pass them on to other neighboring nodes. This work describes a miniaturized sensor node for automotive applications, focusing on the receiver architecture and circuits. The transmitter as well as the receiver in the developed sensor node use bulk acoustic wave (BAW) resonators instead of quartz crystals to generate the reference frequency and in the receiver those resonators are also used for filtering. The advantage of using BAW resonators instead of crystals is that they are more robust and smaller in size. This is important because as a first target application, tire pressure monitoring has been chosen. In contrast to conventional modules which are mounted on the rim, the developed sensor nodes are meant to be attached to the inner liner of the tire where they have to withstand extremely high accelerations. That is why also the size of the sensor nodes has been limited to 1 cm^3 in order to avoid force gradients due to device deformation. In this work the architecture of the sensor node is presented. A suitable architecture for the receiver frontend is developed and a low noise amplifier (LNA) with filtering capabilities is described. The filtering in the LNA is accomplished by integrating BAW resonators into the circuit. Measurement results are provided to enable comparison with state of the art solutions. In order to achieve a power consumption that is low enough for wireless sensor networks, not only the circuits have to be optimized, but also the communication protocols and the scheduling have to be tailored for the application. In this work it is shown how the benefits of the presented BAW based architecture can be exploited to achieve the lowest possible power consumption. Finally some technologies for 3D-integration are explained and it is shown how to achieve a sensor node that is smaller than 1 cm^3 including the power supply.

Acknowledgements

This work has been carried out at Infineon Technologies Austria, Design Center Graz, within the research project e-Cubes, funded by the EU. I would like to thank my supervisors Prof. Wolfgang Pribyl and Prof. Willy Sansen. Special thanks go to Thomas Lentsch who provided the opportunity to carry out this research work within the professional environment of the department of Sense and Control at Infineon. The project has been coordinated by Thomas Herndl and Werner Weber who provided the playground for this research work, to try out new concepts and ideas, and who were always helpful in solving problems of any kind. To finally end up with a working demonstrator has only been possible because of the excellent teamwork of my colleagues and friends Josef Prainsack, Rainer Matischek, Martin Flatscher, and Hartwig Unterassinger who always provided a friendly and pleasant working atmosphere. And of course I would like to thank all other colleagues from the departments of SC and CRE at Infineon who were always helpful in discussing problems and finding solutions without naming all of them.

Markus Dielacher
Graz, May 2011



Contents

Nomenclature

µController	Microcontroller
ABS	Anti-lock Braking System
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
ASIC	Application Specific Integrated Circuit
B	Bandwidth
BAW	Bulk Acoustic Wave
BER	Bit Error Rate
BVD	Butterworth-Van-Dyke
CHOSeN	Cooperative Hybrid Objects Sensor Networks
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
F	Noise Factor
FOM	Figure of Merit
FSK	Frequency Shift Keying
IF	Intermediate Frequency
IIP3	Input Referred Third Order Intersept Point
ISM	Industrial, Scientific, and Medical
LDS	Laser Direct Structuring
LF	Low Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
MBVD	Modified Butterworth-Van-Dyke
MEMS	Micro-Electro-Mechanical System

MID	Molded Interconnect Device
NCO	Numerically Controlled Oscillator
NF	Noise Figure
OIP3	Output Referred Third Order Intersept Point
P1dB	1 dB Compression Point
PCB	Printed Circuit Board
PDC	Park Distance Control
PLL	Phase Locked Loop
PPF	Polyphase Filter
Q	Quality Factor
RAM	Random Access Memory
RKE	Remote Keyless Entry
ROM	Read Only Memory
RSSI	Received Signal Strength Indicator
RTC	Real Time Clock
SiP	System in Package
SMD	Surface Mounted Device
SMR	Solidly Mounted Resonator
SNR	Signal to Noise Ratio
SoC	System on Chip
SPI	Serial Peripheral Bus
TPMS	Tire Pressure Monitoring System
VCO	Voltage Controlled Oscillator
WSN	Wireless Sensor Network

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1. Introduction

This work describes the architecture of a wireless sensor node for tire pressure monitoring with focus on the analog frontend and the low noise amplifier (LNA) of the employed receiver.

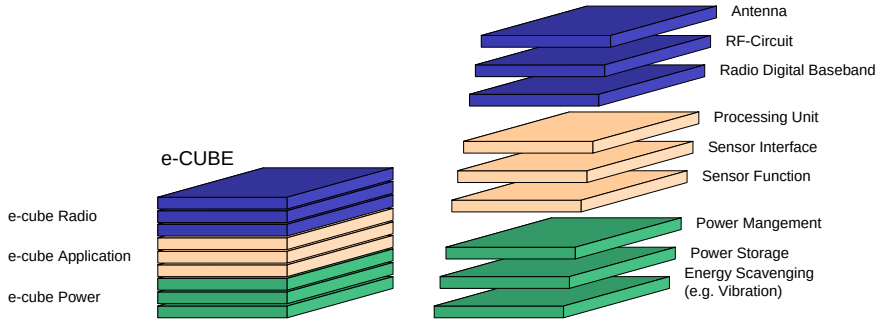


Figure 1.1.: Miniaturization of a sensor node. Source: [101]

Parts of this work have been published in journals, books, and conference proceedings. These publications are referenced in the text as [1] - [16].

1.1. The e-Cubes Project

The work has been carried out within the framework of the EU-funded FP6-project e-Cubes. The objectives of this project are to advance the micro-system technologies to allow for the cost effective realization of highly miniaturized, truly autonomous systems for ambient intelligence [101]. In other words the project targets at the development of wireless sensor networks (WSN). A WSN is defined as a number of devices communicating with each other and at least some of these devices sense some physical quantity in their environment. Common examples for these physical quantities are temperature, humidity, pressure, acceleration, sound, light, infrared, magnetic fields, radiation, location, chemical compositions and mechanical stress [98].

In order to achieve miniaturization of the sensor nodes, the different functional units of the node are meant to be organized in a vertical stack as shown in Figure 1.1. Three demonstration scenarios are targeted within the e-Cubes project: Health and Fitness, Aeronautics and Space, and Automotive applications. The automotive demonstrator which is focused in this work has been developed by Infineon Technologies Austria together with several academic and industrial partners.

1.1.1. Wireless Sensor Networks in Cars

The number of electronic devices in today's cars is increasing steadily. Not only upper class cars, but also medium and small sized vehicles are affected by this trend. Most of these devices are connected via cables, however there is an increasing demand for wireless applications [105, 107, 108, 109]. One reason for this increase is that the large number of cables inside the car accounts for additional weight and fuel consumption. Today's cars contain more than 4 kilometers of wiring [106]. Although single wires for every device or application have already been replaced by sophisticated bus systems like the CAN bus, Byteflight or FlexRay, wireless sensor networks could increase the flexibility of a car's electronic system considerably. Another reason for using wireless links is, that in certain places it is simply not possible to attach cabled devices or sensors. For example in rotating structures wireless devices are much more convenient than cabled ones. In the future, wireless sensor networks will not only be used inside vehicles, but car to car communication and car to infrastructure communication will become more and more interesting [94].

Tire pressure monitoring has been chosen as target application for the e-Cubes automotive demonstrator, because it is a typical example for a wireless sensor network which is already available in vehicles today. This sensor network is built up in a typical star topology. Wireless sensor nodes inside the tires transmit their data to a central unit which is located somewhere in the car and connected to the car battery. This sensor network can be extended by a number of additional devices, for example the electronic car key for remote keyless entry (RKE), which is also already a very common wireless automotive application today. In the future, also other sensing devices like park distance control (PDC), radar, light sensors or temperature sensors for the air condition could be included in this network and transmit their data through a wireless channel. The star-topology which is used today could be replaced by ad-hoc multihop networks, however this imposes severe constraints on the power consumption of the wireless sensor nodes because this new architecture requires sensor nodes with receivers which are continuously listening into the channel. Different network topologies are shown in Figure 1.2.

The first network in Figure 1.2 (a) shows a typical star topology network for tire pressure monitoring. There is only one receiving sensor node, located in the dashboard and powered by the car battery. The sensor nodes inside the tires only include transmitters. The power consumption of the central node in the dashboard is not that critical, although it also has to stay below a certain limit, so as not to drain the car battery, even if the car is parked for several weeks. The power consumption of the nodes inside the tires on the other hand has to be extremely low, because their batteries cannot be replaced or recharged and they have to work for up to ten years [22].

The second network in Figure 1.2 (b) is a multihop network, where each sensor node contains a receiver and a transmitter. The measured data are passed from node to node to their destination via several hops. The advantage of this approach is, that the network can organize itself and it can be rerouted if a node is busy. With this approach, it is also possible to scale down the output power of the transmitters because the data can take several hops and do not have to be transmitted across the whole car in worst case. To enable such a network, a sophisticated power management is required in each sensor node.

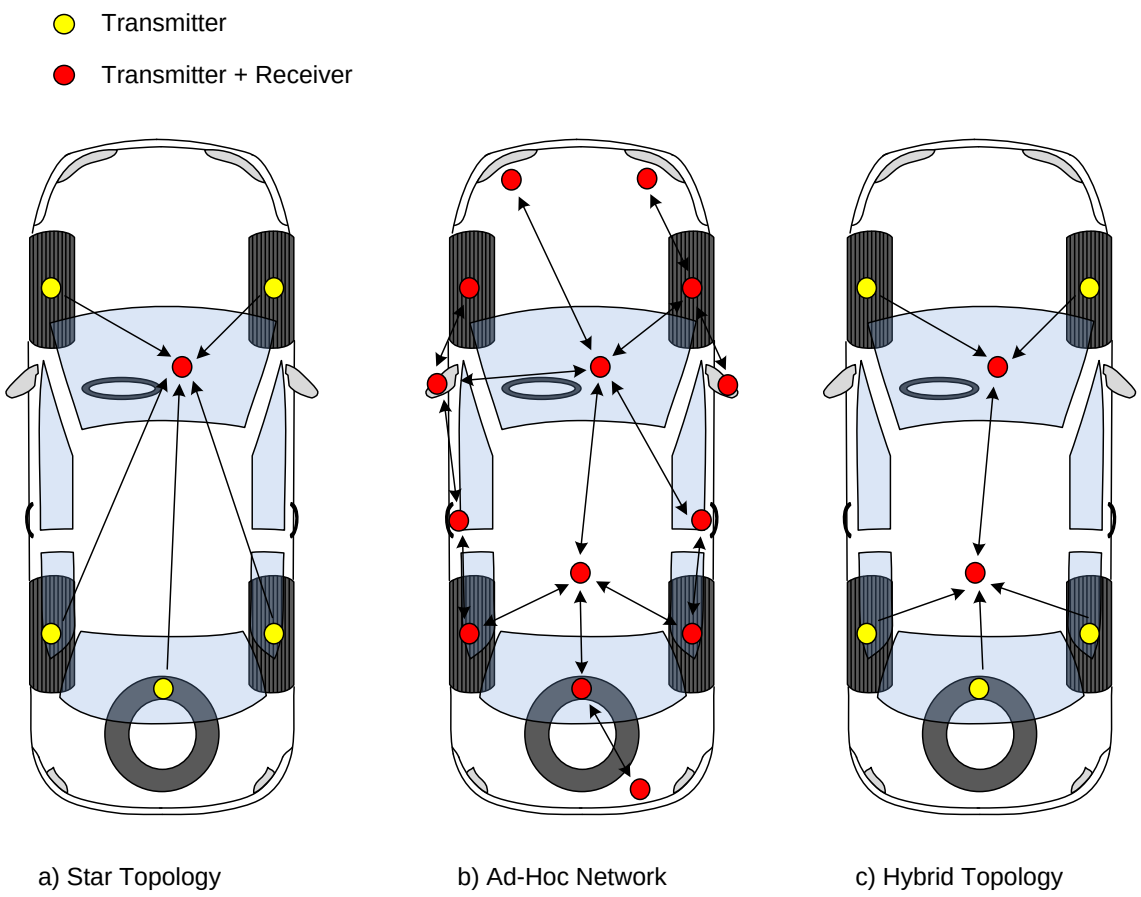


Figure 1.2.: Topologies for Wireless Sensor Networks

The third network in Figure 1.2 (c) is a heterogeneous network. It consists of sensor nodes which only contain transmitters as well as sensor nodes with full functionality, also containing receivers. So the functionality and power consumption of each node can be scaled individually.

1.1.2. Application - TPMS

State of the art Tire Pressure Monitoring Systems (TPMS) are modules which measure the pressure and acceleration inside the tire and transmit the data to a central unit in the car. These modules are mounted on the rim of the wheel using the valve as antenna [28]. There are TPMS modules available which also include a low frequency (LF) receiver with very low power consumption. Due to the low power consumption the LF receiver can be always on and act as a wakeup receiver. A transmitter unit in the car can then activate the TPMS modules by sending an LF signal. Other TPMS modules do not contain the LF receiver, they wake up from standby and perform their measurements according to a fixed schedule. Figure 1.3 shows a state of the art TPMS module. Another way of monitoring the tire pressure is to evaluate the data coming from the anti-lock braking system (ABS).

Figure 1.3.: TPMS module

Under-inflated tires will result in a higher rotation speed of the according tire, and this can be detected by the ABS. This indirect TPMS however is inferior to the direct pressure measurement in terms of accuracy and it only detects pressure loss of a tire relative to the other tires.

1.2. The eCubes Automotive Demonstrator

This work describes a miniaturized sensor node for TPMS. In contrast to state-of-the-art TPMS the presented sensor nodes are designed for being mounted on the inner liner of the tire instead of the rim. This special mounting location allows sensing of additional data like side-slip, wheel speed, tire wearout, road condition, tire friction, and vehicle load. These data can be used for improved tracking and engine control, feedback to the power train, car-to-car communication purposes and safety features [1]. Also the developed sensor nodes include receivers in order to enable other network topologies than the standard star-topology.

1.2.1. Constraints

Mounting a TPMS on the inner liner of a tire instead of the rim imposes severe constraints on the design. The required temperature range is from -40 °C to +125 °C. The acceleration caused by the circular movement of the tire can reach values higher than 1,000 g [28]. This value does not include the acceleration caused by vibrations or the impacts when the TPMS module hits the road surface. Including also these effects, acceleration peaks of 4,000 - 5,000 g must be taken into account [22]. Because of these high forces, the volume of the modules has to be below 1 cm^3 in order to avoid force gradients due to device deformation. The weight is limited to five grams including package and power supply. Not only because of the additional weight, power supply is a critical issue. Once the system is installed inside the tire, the power supply has to last for ten years. Batteries providing the required capacity and at the same time being small enough are not available today.

New developments try to include energy harvesting devices into the module instead of batteries. A very promising approach is to use the vibrations inside a vehicle's tires to generate electrical energy. The power which can be delivered by vibrational energy harvesters with the desired dimensions is only in the range of up to 10 µW [25, 24, 22]. So the power consumption of the TPMS modules has to be extremely low.

1.3. Conclusion

This chapter introduces the background of the thesis. The target is to develop a miniaturized sensor node for automotive wireless sensor networks. The application is described and the most important constraints are derived based on existing sensor nodes for TPMS. However the targeted sensor nodes clearly exceed state-of-the-art by:

- being mounted on the inner liner of a tire instead of the rim in order to gain additional information,
- reducing the size to below 1 cm^3,
- being powered by energy harvesting devices delivering only a few µW of power, and by
- including a receiver and in this way enabling new network topologies.

2. Sensor Node Architecture

This chapter describes the architecture of the developed sensor nodes. More detailed descriptions can be found in [1] and [5]. The automotive demonstrator is a sensor node consisting of

- a microcontroller ASIC (µController),
- a sensor for pressure and acceleration, based on a micro-electro-mechanical system (MEMS)
- a bulk acoustic wave (BAW) based transceiver,
- and a power supply module.

A block diagram of the system is given in Figure 2.1.

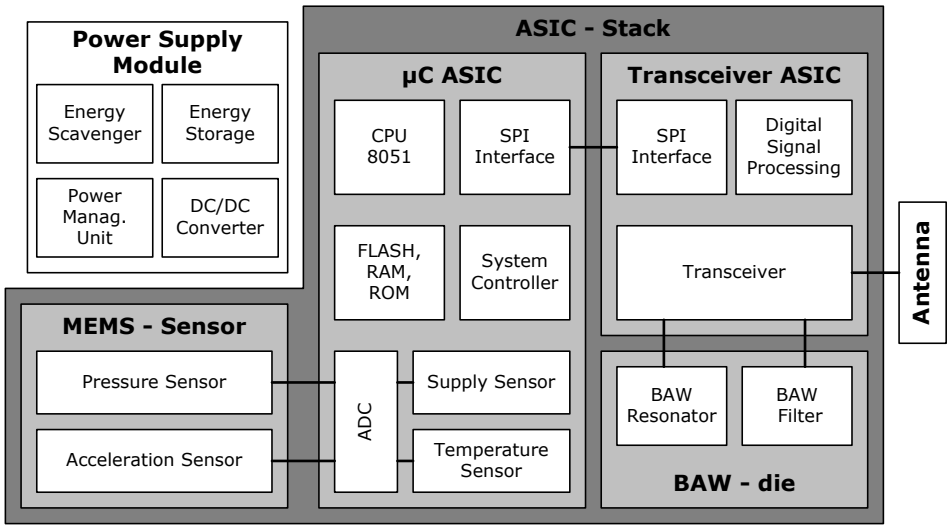


Figure 2.1.: Sensor Node

The µController is fabricated in a 0.25 µm CMOS process. It is based on an 8051 CPU and contains an interface for the pressure and acceleration sensor, an analog to digital converter (ADC) and several types of memory (RAM, ROM, FLASH). The µController can be programmed via an I²C interface and communicate with the transceiver via a serial peripheral bus interface (SPI). The µController ASIC is qualified for automotive applications, thus it supports the required temperature range from -40 °C to +125 °C.

The sensor die is a bulk micromachined MEMS device which contains sensors for pressure and acceleration. It consists of a glass-silicon-glass triple stack. One of the glass layers contains a cavity which is sealed by the active silicon layer. The silicon

layer contains a membrane which is located above the cavity. So the pressure inside this sealed chamber is used as a reference for the pressure measurements. The glass layer on the other side of the stack contains a pressure inlet which leads to the other side of the membrane.

The transceiver, which is the main topic of this work, is fabricated in a 0.13 µm CMOS process. In contrast to conventional transceivers, it does not use a quartz crystal as frequency reference, but it uses BAW resonators to generate the carrier signal in transmit mode and the local oscillator (LO) signal in receive mode. Using BAW resonators offers a number of advantages compared to conventional crystal based systems. The crystal itself is very bulky and shock sensitive. When mounted on the inner liner of a tire, there is a high risk that the crystal is damaged due to the high acceleration. And also for the power consumption, the use of a BAW instead of a crystal is very beneficial. The BAW based oscillators directly oscillate at the carrier frequency of 2.1 GHz or 2.45 Ghz. They do not require another voltage controlled oscillator (VCO) and a phase locked loop (PLL) which drastically reduces the turn on time of the transceiver. The turn on time is an important factor for applications such as sensor networks. If the data payload is very small, the turn-on time can become the dominating factor for power consumption. This will be explained in detail in Chapter 12. The crystal- and PLL-less approach is described in [6].

2.1. Demonstrator Generations

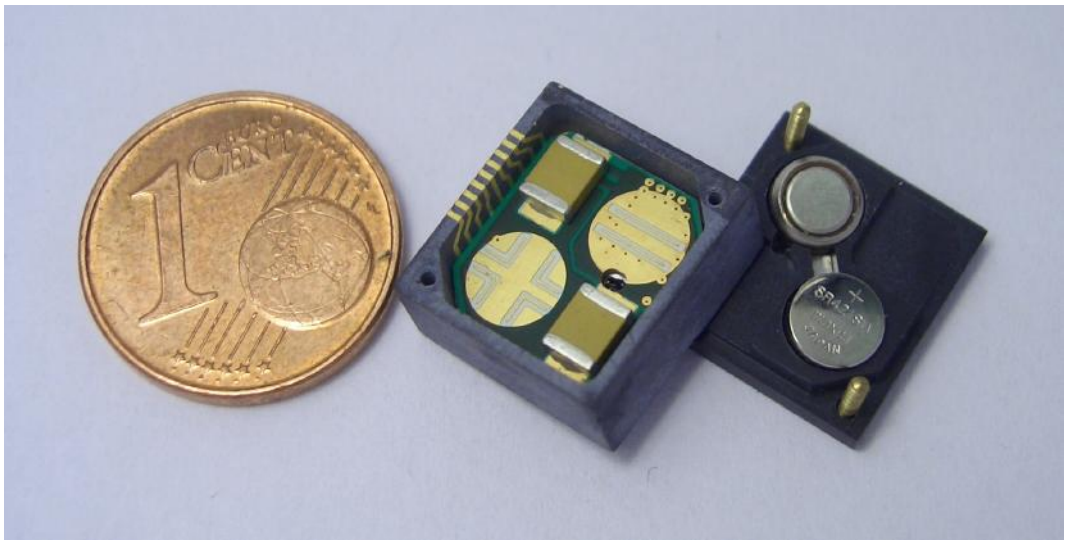


Figure 2.2.: 3D Package

The automotive demonstrator has been developed in three stages with three generations of Demonstrators.

- D1: The first demonstrator is a functional proof of concept, with the system's components mounted onto a large printed circuit board (PCB). This PCB offers a number of debugging possibilities.

- D2: The second demonstrator already targets at the miniaturization of the system, but the components are still arranged in a lateral way. A three dimensional package containing also the batteries is used to achieve the small system size. Figure 2.2 shows the small size module.
- D3: the third and last demonstrator uses 3D vertical chip stacking technologies to further reduce the volume. These technologies will be briefly described in Chapter 13.

2.2. Conclusion

In this chapter the architecture of the sensor nodes is introduced. The most important components are described and the steps toward miniaturization are explained. With the presented architecture a completely autonomous sensor node with multi-hop capabilities can be achieved.

3. The eCubes Transceiver

This chapter explains the architecture of the transceiver which has been developed for the eCubes sensor nodes.

3.1. Architecture

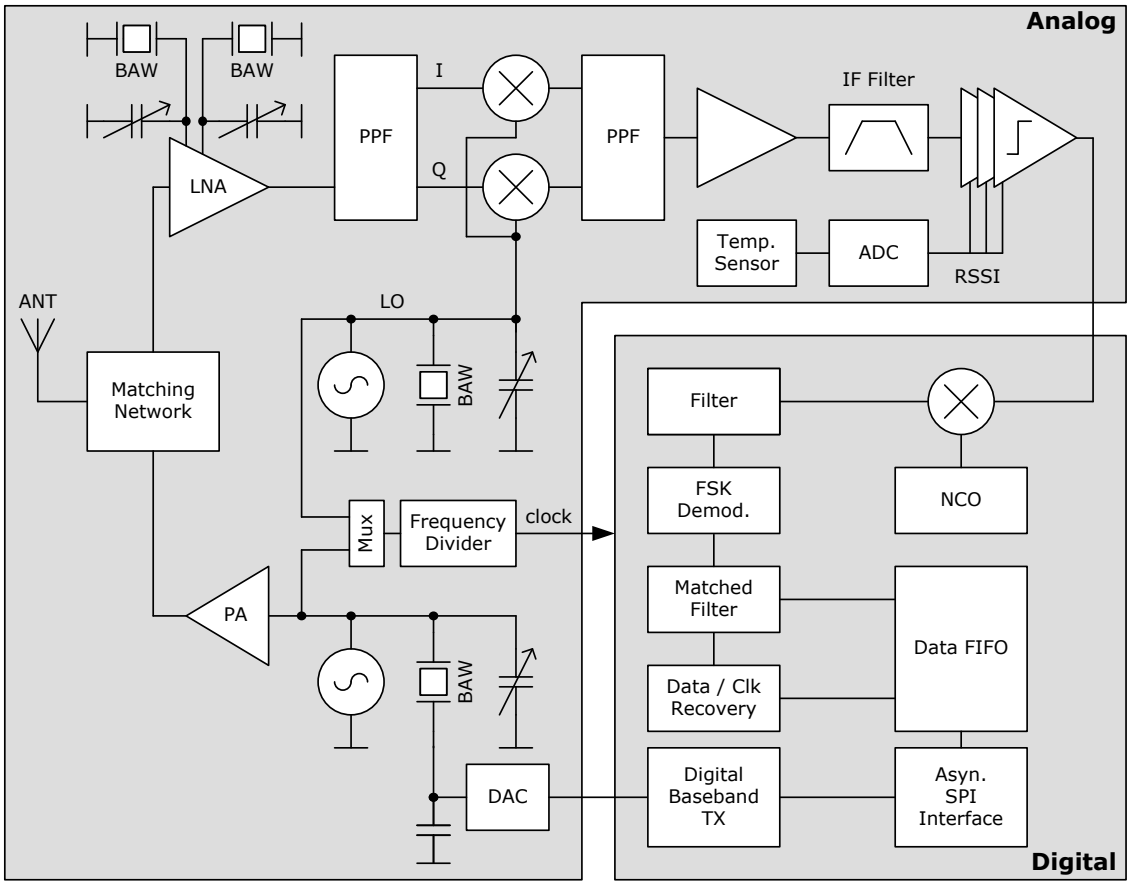


Figure 3.1.: The ecubes transceiver

In Figure 3.1 the schematic of the BAW based transceiver is shown. It contains two fully integrated BAW oscillators, one is used for generating the modulated carrier in transmit mode and the other provides the LO signal in receive mode. The two oscillators have a frequency offset, accomplished with different BAW resonators, for realizing a heterodyne receiver with a low IF of 10.7 MHz. The transceiver has been evaluated with two different BAW devices. In the first version the resonant frequency of the BAW is around 2.1 GHz

and in the second version it is around 2.45 GHz. The oscillators are tunable over a certain frequency range to enable temperature compensation, process compensation, and to perform modulation in the transmit path. In the 2.4 GHz ISM (industrial, scientific, and medical) band the tuning range of the BAW oscillators will not be sufficient to cover all channels, but due to the low costs and due to the fact that the BAW devices can easily be integrated, a bank of BAW resonators with slightly different resonant frequencies can be used to solve this problem. As the presented transceiver is only a proof of concept, it is not necessary to cover the whole band, and only single resonators are used. The oscillators have a very short turn on time and this fact in combination with the small data packet of the sensor node results in a very narrow active time slot and therefore the system is very energy efficient. The short turn-on time is feasible because the reference frequency is already at RF. The BAW based oscillator together with the transmitter architecture is not part of this work, but is described in detail in [5].

The core of this work is the receiver frontend of the sensor node. In order to be able to specify the requirements for the frontend and to choose an appropriate architecture, it is necessary to investigate the environment where it is meant to be installed and to consider any other constraints which are imposed by the system.

3.2. Channel Properties

The transmission range of a transmitter - receiver system can be derived from the output power of the transmitter, the input sensitivity of the receiver, and the path loss.

Path loss in free space can be calculated according to Friis's transmission formula [80]:

$$L = 10 \cdot \log \left(\frac{4\pi d}{\lambda} \right)^2 - G_{\mathrm{Tx}} - G_{\mathrm{Rx}}, \tag{3.1}$$

where d is the distance in meters, and λ is the wavelength of the transmitted signal. G_{Tx} and G_{Rx} are the antenna gains of the transmitter and the receiver respectively. The antenna gain is defined as the ratio of the power transmitted in a certain direction relative to the power transmitted by an ideal isotropic antenna. Figure 3.2 shows the free space path loss for different frequencies, assuming an antenna gain of 0 dB for both the transmitter and the receiver antenna. For a sensor node, an isotropic antenna is the best solution, because the mounting location and orientation is not known.

Indoor path loss cannot be expressed by such a generic equation as free space path loss because indoors a lot of effects like echo and multipath fading have to be considered. For sensor networks inside a car, the quality of the communication channel strongly depends on the location of the sensor nodes and also the movement and surroundings of the car itself. Channel measurement results inside a car have been reported in [84]. The results in [84] show that the path loss in two different scenarios does not exceed 76.8 dB in the 2.4 GHz frequency band. The reported values represent the mean path loss over the bandwidth from 2.36 GHz to 2.5 GHz which is important to notice because fading can be very strong at single frequencies within this band and negligible in others. Many considerations for communication requirements in wireless sensor networks as presented in [113] cannot be used for automotive sensor networks because they assume short range

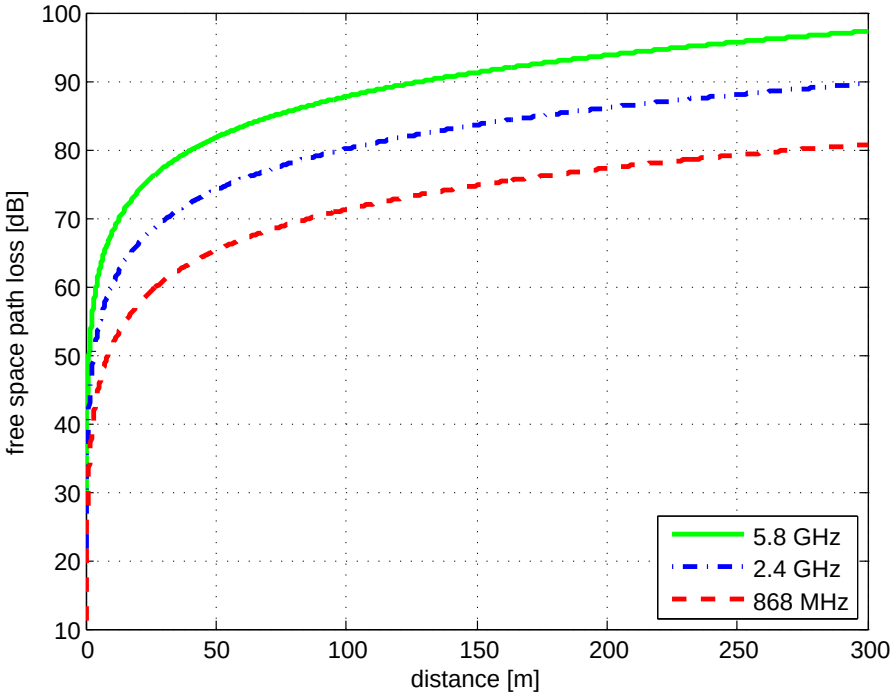


Figure 3.2.: Free space path loss for different frequency bands

(10 m) communication at free line of sight. This assumption leads to sensitivity requirements which are not sufficient for automotive scenarios.

The sensitivity of a receiver defines the minimum signal level which can be detected with a signal-to-noise ratio (SNR) that is acceptable for the demodulator. It can be derived from the bandwidth (B), the required SNR and the noise figure (NF) of the frontend [99].

$$P_{\text{in.min}} = -174\frac{\text{dBm}}{\text{Hz}} + NF + 10\log B + SNR_{\text{min}} \tag{3.2}$$

The required SNR depends on the chosen modulation scheme, the data rate, the available bandwidth and the desired bit error rate (BER).

3.3. Receiver Specifications and Link Budget

As the transceiver is part of the sensor node, the general requirements concerning temperature range, power consumption, mechanical robustness, and size listed in Section 1.2.1 are all valid also for the transceiver. The most relevant specifications and requirements which only concern the receiver and not the whole system are given below:

- Power Consumption: As for the whole system, power consumption is one of the most important constraints for the receiver frontend. However, there is always a trade-off with performance. It is not useful sacrificing too much performance just to achieve an ultra low power consumption, because it might turn out that power may be saved more efficiently with fast and reliable transmission of signals and with

Sensor Node	
Size	$<$ 1 cm³
Weight	$<$ 5 grams
Lifetime	10 years
Temperature range	-40°C to +125°C
Max. acceleration	1,000 g
Avg. power consumption	$<$ 10 µW
Receiver	
Data rate	$<$ 100 kbit/s
Modulation	FSK
Power consumption	$<$ 8 mA
Demodulator SNR	10.8 dB
Sensitivity (at BER = 10^{-3})	-92.8 dBm
Noise figure	26.4 dB

Table 3.1.: Specifications for the sensor node and for the receiver

sophisticated protocols and sleep modes when the system is not active. Those aspects will be covered in Chapter 12. As a good compromise, the total current consumption of the receiver including LO generation, voltage regulators, and all other peripheral blocks has been specified not to exceed 8 mA.

- Data Rate: As the data payloads which have to be transmitted and received by the sensor nodes are very small, data rates of up to 100 kbit/s are sufficient for the application. In Chapter 12 it will be shown that for very small data packets, the start-up time of the system can be dominating in terms of power consumption. The employed modulation scheme is incoherent frequency shift keying (FSK). For this modulation scheme the required $\frac{E_b}{N_0}$ at a BER of 10^{-3} is about 10.8 dB [78]. With the assumed data rate of 100 kbit/s and a system bandwidth of about 300 kHz which is determined by the channel filter, the required SNR can be calculated as 6.2 dB. The BER of 10^{-3} is sufficient because of the small data payloads. To add some redundancy, packets can be sent repeatedly.

- Sensitivity: The required sensitivity for the receiver can be estimated taking the wireless channel inside the car into account. Taking the value of 76.8 dB from [84] and assuming an antenna loss of -5 dB at both the transmitter and the receiver, the total path loss calculates to 86.8 dB. With a transmitter output power of 0 dBm, the given path loss, and the required SNR, the desired sensitivity can be calculated as -92.8 dBm.

- Noise Figure: With the desired sensitivity, the maximum allowable noise figure of the receiver frontend can be calculated. The noise floor is -174 dBm/Hz multiplied with the bandwidth of 300 kHz, resulting in -119.2 dBm. By subtracting the sensitivity from the noise floor, the maximum allowed noise figure of 26.4 dB can be obtained.

Table 3.1 summarizes all requirements for the sensor node in general and for the receiver frontend in particular.

3.4. Conclusion

In this chapter, the architecture of the employed transceiver has been introduced. The required performance has been evaluated according to the expected channel properties. As the transceiver is not operating in free space, channel properties reported in literature have been taken as a reference. Although the requirements regarding data rate and sensitivity might seem relaxed compared to applications like UMTS or wireless LAN, the requirements are very challenging considering the low power consumption.

4. The eCubes Receiver Frontend

This chapter describes the receiver architecture which has been chosen for the eCubes transceiver. It has been published in [2].

4.1. eCubes Receiver Frontend Architecture

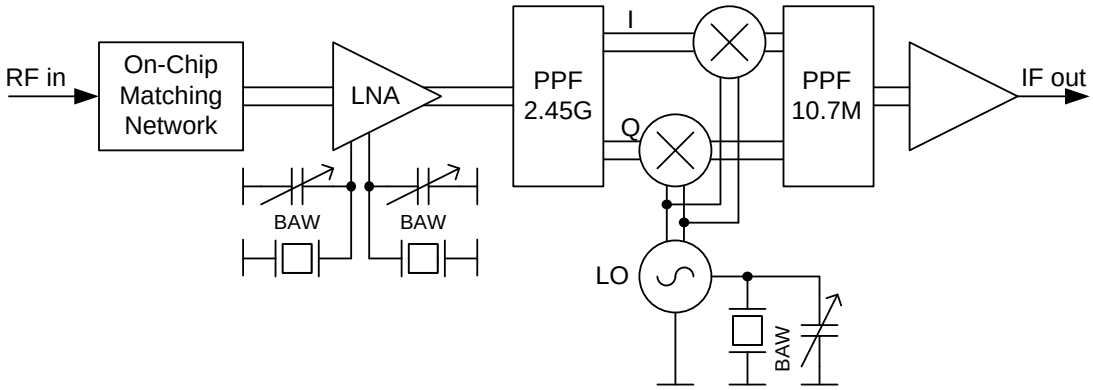


Figure 4.1.: The ecubes receiver frontend

The receiver architecture which has been chosen for the eCubes sensor nodes is based on the Hartley image reject architecture. Additionally, it uses the narrow bandwidth of single BAW resonators to suppress the image before downconversion. A block diagram of the eCubes receiver frontend is shown in Figure 4.1. The choice for this architecture has been made for several reasons:

- As miniaturization of the system is a very important constraint for the system, a combined matching network for the receiver and the transmitter has been designed which does not require any external components. A detailed description of the circuit is given in Chapter 6. The matching network exploits the fact that the capacitive input of the LNA can be brought into resonance with an on-chip inductor and so an additional voltage gain can be achieved.
- The system uses a BAW based oscillator to generate the LO signal for downconversion. This BAW based oscillator does not provide quadrature phases and it directly oscillates at the frequency of interest. In PLL based systems, the VCO often oscillates at a multiple of the desired frequency such that I- and Q- phases can be obtained easily from an integer frequency division. Designing an oscillator with quadrature outputs would be possible but at the cost of a prohibitively high

current consumption. That is why a homodyne receiver frontend has not been implemented, as it requires exact I- and Q- signals. Another drawback of homodyne receivers is, that flicker noise and DC offsets due to second order nonlinearities may distort the downconverted signal.

- The intermediate frequency has been chosen to be 10.7 MHz. With this IF it is possible to perfectly use the BAW resonators in the receive path for image rejection, because it is about half the difference between the series and the parallel resonance of the resonators. The resonators are described in Chapter 5 and their integration into the LNA is explained in detail in Chapter 7. Another advantage of this frequency is that cheap ceramic IF filters are available.

- In order to achieve an even higher image suppression than with the BAW resonators alone, an image reject architecture has been implemented but unlike the typical Hartley architecture [99] where the I- and Q- phases are provided by the LO, the quadrature phases in this receiver frontend are generated in the signal path by a polyphase network. This polyphase network is designed for quite a large bandwidth, because resonators with different resonant frequencies between 2.1 and 2.45 GHz have been assembled. Over this large bandwidth, amplitude errors in the quadrature phases might occur, which has been the reason for not using the homodyne frontend. In an image reject architecture however it is just the image rejection that might suffer from such a problem. The signal path itself is not affected by amplitude errors because the contributions of the desired signal sum up at the output of the frontend. This behavior is shown in Equations 4.1 - 4.6.

Figure 4.2 shows a simplified representation of the frontend concept. The on-chip matching network, containing also the RX/TX switch feeds the incoming RF signal to the differential LNA. The LNA is followed by a polyphase network which generates the quadrature phases required for the I- Q-mixers. After downconversion, another polyphase network is used for image cancellation. In this simplified representation, the polyphase networks are included as 90° shifts in the I-path. In reality, the polyphase networks cause shifts of 45° with opposite signs in the I- as well as in the Q-path.

Assuming that $\omega_{\mathrm{S}} < \omega_{\mathrm{LO}}$, and $\omega_{\mathrm{IM}} > \omega_{\mathrm{LO}}$, then the contribution of the desired signal in node A can be calculated as

$$\begin{aligned} y_{\mathrm{A_S}}(t) &= \frac{1}{2}[\cos((\omega_{\mathrm{S}} - \omega_{\mathrm{LO}})t - 90°)] \\ &= \frac{1}{2}[\cos(-\omega_{\mathrm{IF}}t - 90°)] \\ &= \frac{1}{2}[\cos(\omega_{\mathrm{IF}}t + 90°)]. \end{aligned} \tag{4.1}$$

The contribution of the image can be calculated in the same way as

$$\begin{aligned} y_{\mathrm{A_{IM}}}(t) &= \frac{1}{2}[\cos((\omega_{\mathrm{IM}} - \omega_{\mathrm{LO}})t - 90°)] \\ &= \frac{1}{2}[\cos(\omega_{\mathrm{IF}}t - 90°)]. \end{aligned} \tag{4.2}$$

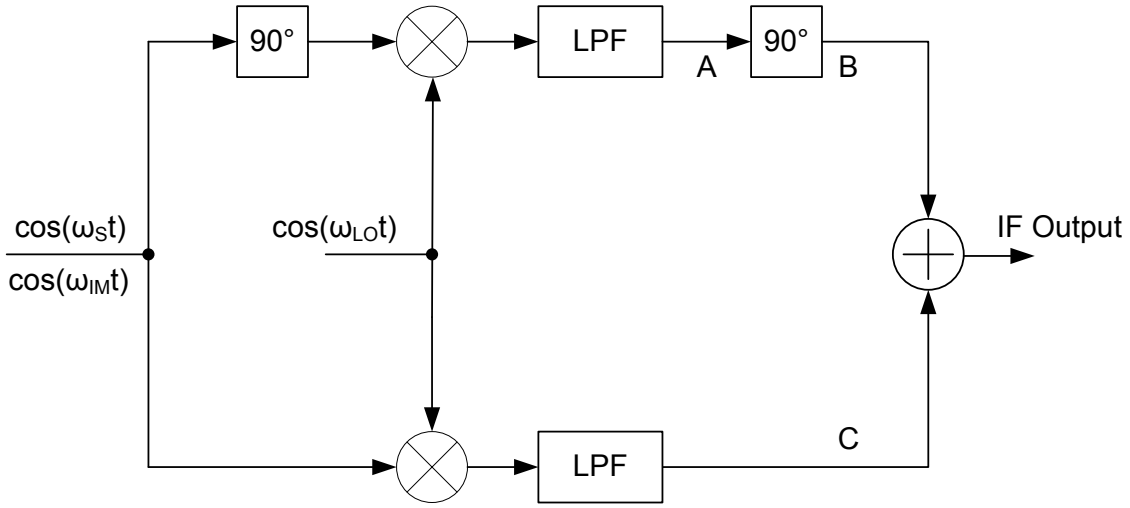


Figure 4.2.: Image reject architecture containing two polyphase networks

After another 90° shift, the contribution of the desired signal to the signal in node B becomes

$$y_{\mathrm{B_S}}(t) = \frac{1}{2}[\cos(\omega_{\mathrm{IF}}t)]. \tag{4.3}$$

And the image becomes

$$\begin{aligned} y_{\mathrm{B_{IM}}}(t) &= \frac{1}{2}[\cos(\omega_{\mathrm{IF}}t - 180°)] \\ &= -\frac{1}{2}[\cos(\omega_{\mathrm{IF}}t)]. \end{aligned} \tag{4.4}$$

Node C carries the downconverted signals without any additional phase shift:

$$y_{\mathrm{C_S}}(t) = \frac{1}{2}[\cos(\omega_{\mathrm{IF}}t)], \tag{4.5}$$

and

$$y_{\mathrm{C_{IM}}}(t) = \frac{1}{2}[\cos(\omega_{\mathrm{IF}}t)]. \tag{4.6}$$

At the output, the contributions of the desired signals sum up, whereas the contributions of the image signals are opposite-phased and cancel out. Which of the two sidebands is canceled by the image reject architecture and which is passed through can be changed easily by inverting the polarity of either the I- or the Q- path. In a fully differential design this can be done by simply crossing the two branches of the differential signal.

4.2. Analog to Digital Conversion and Digital Processing

After downconversion and image rejection, the signal is fed to an off-chip IF-filter where the channel is selected. Afterwards the analog to digital conversion is performed by

means of a limiter. A limiter is a multi stage amplifier with a very high gain, in the case of this design more than 80 dB. The limiter used in this work has been designed by [73]. It clips the signal at the upper and lower supply voltages and produces a rectangular output signal. So the amplitude information is removed but the result is a binary signal and the need for an automatic gain control (AGC) is eliminated, which reduces the complexity of the system. The binary output signal of the limiter is sampled and further processing is done in the digital domain. Besides the binary output signal, the limiter also provides a received signal strength indicator (RSSI). This RSSI signal can be fed into an on-chip ADC and converted to a 10-bit digital value. So it can be used as a wake-up criterion for the system or to fine-tune the BAW based oscillators, the filters in the LNA or the matching network. In the digital domain the sampled output signal of the limiter is mixed into complex baseband by using a numerically controlled oscillator (NCO) which allows tuning the frequency in very fine steps. The digital clock can be derived from any of the two BAW based oscillators. After additional digital filtering and demodulation the signal is passed to the matched filter. By means of the clock and data recovery unit the output of the matched filter is sampled and the received payload is stored in a data FIFO where is can be accessed via the SPI [1].

4.3. Conclusion

A receiver architecture specially suitable for the BAW based approach is introduced in this Chapter. On the one hand it deals with the drawback of a BAW based oscillator providing only in-phase and no quadrature signals by using a polyphase filter in the signal path to generate the quadrature phases. On the other hand, it benefits from the narrow bandwidth of single BAW resonators to achieve an extraordinary image suppression. Calculations show how the chosen architecture is able to reject the image frequency while downconverting the desired signal.

5. RF Filters

As pointed out in the previous chapters, the presented transceiver makes extensive use of BAW resonators. That is why this chapter explains in detail the working principle of such resonators. Bulk acoustic wave (BAW) and surface acoustic wave (SAW) have become the dominating technologies in RF filter design. In terms of performance, size, and cost they are superior to other RF filter technologies [97, 100]. This chapter explains the working principle of the two technologies and provides a comparison between them.

5.1. Working Principle

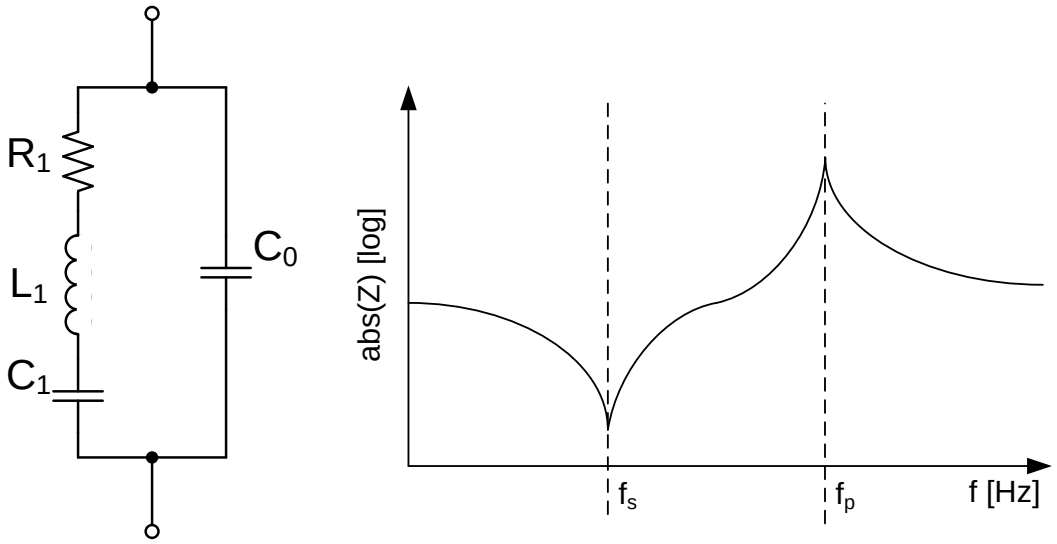
SAW and BAW resonators are Micro-Electro-Mechanical Systems (MEMS). In a MEMS device, electrical energy is converted to mechanical energy and vice versa. In a SAW or BAW resonator acoustic waves are generated and transformed back to electrical signals by means of transducers and piezoelectric materials. The quality factor (Q) of BAW and SAW devices is very high compared to other technologies, because the applied acoustic materials have very low propagation loss. Another advantage of these devices is, that they are very small. The propagation speed of an acoustic wave is four to five orders of magnitude less than the speed of the electromagnetic wave. This means that also the wavelength is much smaller and indeed the first applications for BAW and SAW devices was to use them as delay lines [100].

5.2. Equivalent Circuit

Basically a piezoelectric resonator behaves like a RLC-resonant circuit. A very simple equivalent circuit is sketched in Figure 5.1a. Figure 5.1b shows the impedance of the resonant circuit. Two frequencies, the series resonant frequency f_s, set by L_1 and C_1, and the parallel resonant frequency f_p, defined by C_0 in series with L_1 and C_1 [77], can be determined. f_s is defined as the frequency of maximum conductance and f_p is defined as the frequency of maximum resistance [86]. The model in Figure 5.1a is called the Butterworth-Van-Dyke model (BVD) [100]. C_0 is the static or plate capacitance. It determines the impedance of the device in the regions far away from f_s and f_p. R_1, C_1, and L_1 represent the motional resistance (acoustic loss), capacitance, and inductance respectively [100].

5.3. Filter Topologies

Both BAW and SAW filter devices always consist of more than just one single resonator. Due to the high Q of a single resonator (in the range of 1,000 - 2,000), its bandwidth is



(a) Equivalent circuit (b) Impedance

Figure 5.1.: Primitive model of a piezoelectric resonator

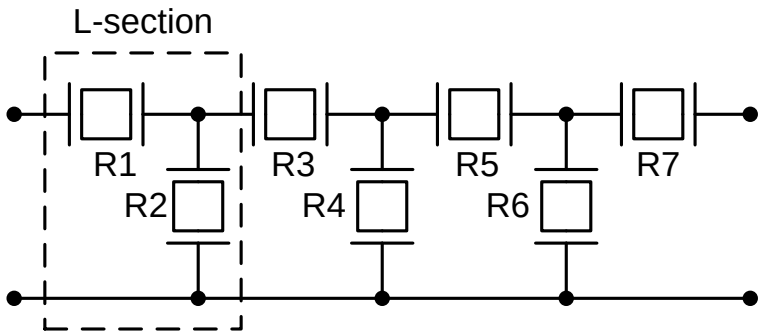


Figure 5.2.: Filter device consisting of several resonators connected in a ladder structure

very narrow, and a number of resonators with different center frequencies are used to achieve a certain desired bandwidth. Usually, these resonators are connected in a ladder structure, as shown in Figure 5.2.

BAW and SAW resonators have two resonant frequencies, a series resonant frequency f_s where the impedance is very low, and a parallel resonant f_p where the impedance is very high. Each L-section of the ladder structure consists of a resonator in series and a resonator in parallel with slightly different resonant frequencies. The series resonant frequency of the series resonator R1 is used to preserve desired signals while the parallel resonant frequency rejects undesired signals. The resonator R2 in the parallel path works the other way round. The series resonant frequency rejects undesired signals while the parallel resonant frequency preserves the desired components of the input spectrum. This behavior is shown in Figure 5.3.

Another filter topology which is less common than the ladder topology is the lattice topology. Its drawback is, that it can only be used for differential signals, whereas the

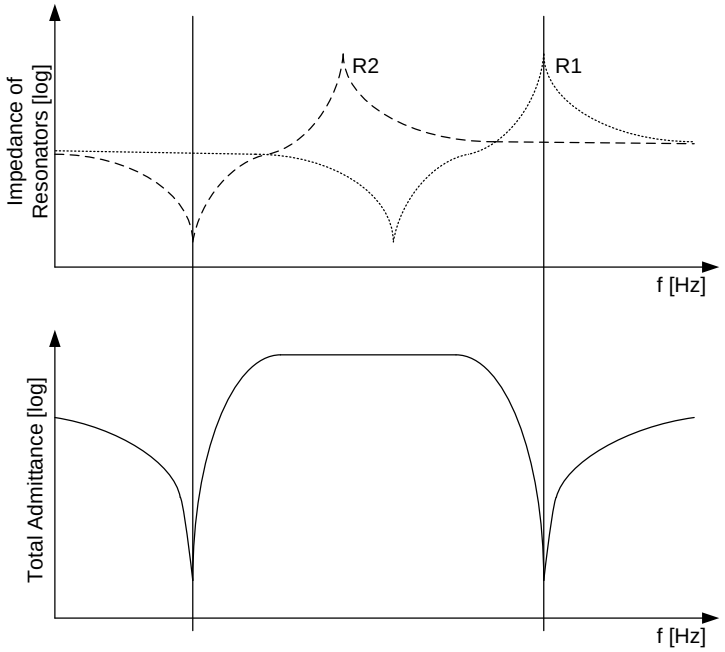


Figure 5.3.: Frequency response of one L-section

ladder topology performs better for single ended inputs, which is more common. The lattice topology is shown in Figure 5.4.

5.4. SAW

As its name indicates, a surface acoustic wave is a wave travelling along the surface of a structure. The basic structure of a SAW resonator is shown in Figure 5.5.

The substrate of a SAW resonator consists of a piezoelectric material. On top of it, it contains a pair of interleaving combs called interdigital transducer (IDT) between two grating reflectors. When the IDT is excited with an alternating voltage, a wave is launched along the substrate. The two grating reflectors form an acoustic cavity which is many wavelengths long. For a certain wavelength λ, a standing wave can be generated between the two reflectors. The resonant frequency is determined mainly by the pitch of the IDT. The IDT and the grating reflectors are typically made of thin-film metal, in most cases aluminum.

5.5. BAW

The difference between SAW and BAW resonators is that in BAW resonators the acoustic waves are launched into the bulk of the device instead of travelling along the surface. Basically a BAW resonator consists of a thin-film layer of piezoelectric material between two thin-film metal electrodes. When the piezoelectric layer is excited by a voltage or an

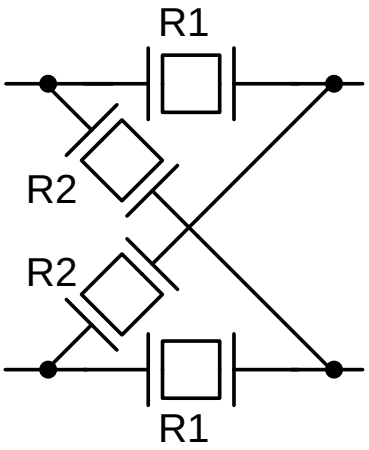


Figure 5.4.: Lattice Filter Topology

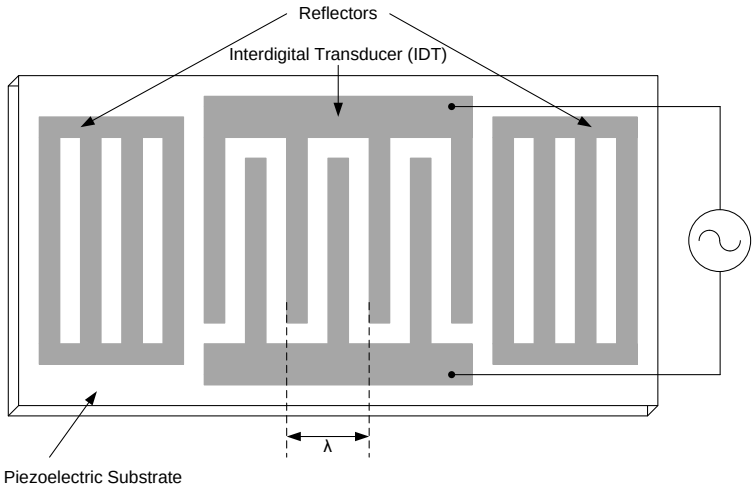


Figure 5.5.: Structure of a SAW Resonator

electric field between the two electrodes, an acoustic wave is generated. The resonance frequency is determined by the thickness of the piezoelectric layer and the thickness and mass of the electrodes. At the resonance frequency, there is exactly one half of the acoustic wavelength between the top and the bottom of this stack. The propagation speed of the acoustic wave is four to five orders of magnitude less than the speed of the electromagnetic wave. Therefore the acoustic wavelength is also much shorter than that of the electromagnetic wave.

Acoustic waves with the desired frequency are trapped within the resonator. In order to prevent acoustic waves with other wavelength from propagating any further into the substrate, they have to be reflected. There exist two types of BAW resonators, with different means of reflecting the waves at the bottom electrode. The first ones are the free-standing bulk acoustic resonators (FBAR) and the second ones are the solidly mounted resonators (SMR). FBARs are based on a cavity underneath the resonator, and SMRs

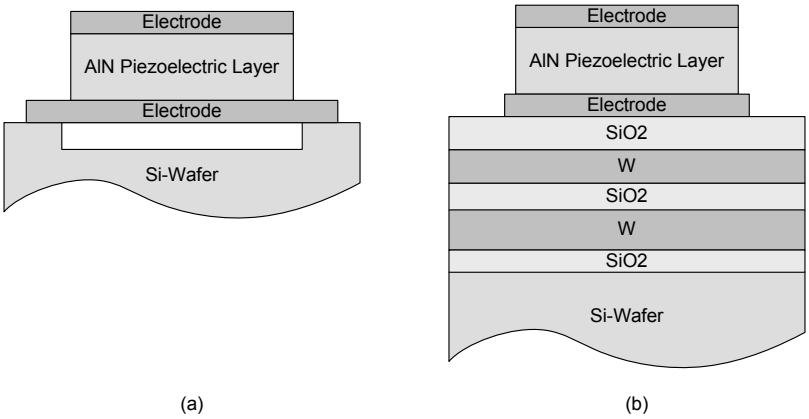


Figure 5.6.: FBAR (a) and SMR (b) Technologies

use a Bragg reflector underneath the bottom electrode to reflect the waves. A Bragg reflector consists of alternating high and low impedance $\lambda/4$ thin-film layers. The two different topologies are sketched in Figure 5.6. Large ratios of high to low impedance materials are required to reflect the acoustic energy over a wide bandwidth, for example Tungsten (W) and Silicon-Dioxide (SiO2) with a ratio of 7:1.

5.6. Key Features of Piezoelectric Resonators

This section describes the key features used for characterizing piezoelectric resonators.

Piezoelectric effective coupling coefficient The effective coupling coefficient k^2_{eff} is defined as the ratio of the stored mechanical energy to the electrical energy [112]. It can be expressed according to Equation 5.1 [87].

$$k^2_{\mathrm{eff}} = \frac{\pi^2}{4} \cdot \frac{f_{\mathrm{s}}}{f_{\mathrm{p}}} \cdot \frac{f_{\mathrm{p}} - f_{\mathrm{s}}}{f_{\mathrm{p}}} \tag{5.1}$$

The effective coupling coefficient determines the bandwidth of a filter device as in Figure 5.2 [85]. The best reported value is 6.9% [100]. There are two reasons why a high k^2_{eff} is desirable. On the one hand, a higher k^2_{eff} improves the insertion loss of a filter, and on the other hand it can be traded off for Q [97].

Bandwidth The bandwidth (B) of a resonator is defined as $B = (f_{\mathrm{p}} - f_{\mathrm{s}})/f_{\mathrm{p}}$. Here the best reported value is 2.8% [100].

Quality Factor One of the most significant parameters describing a filter is its quality factor. Not only filters can be described by this parameter but all kinds of resonant circuits,

not limited to electric circuits. The most generic definition of Q is that it describes for a sinusoidal excitation of a system with frequency ω how much energy is lost per cycle.

$$\begin{aligned} Q &= \omega \frac{\text{energy stored}}{\text{average power dissipated}} \\ &= 2\pi \frac{\text{energy stored}}{\text{energy dissipated per cycle}} \end{aligned} \tag{5.2}$$

A more comprehensive definition of Q for a filter is the center frequency (f_c) divided by the 3-dB bandwidth [88]. Regarding BAW resonators, the Q values of series and parallel resonance do not necessarily have to be equal.

$$Q_\mathrm{p} = \frac{f_\mathrm{p}}{\Delta f_\mathrm{3dB}}, \text{regarding the impedance } Z \text{ of the resonator,} \tag{5.3}$$

and

$$Q_\mathrm{s} = \frac{f_\mathrm{s}}{\Delta f_\mathrm{3dB}}, \text{regarding the admittance } Y = \frac{1}{Z} \text{ of the resonator.} \tag{5.4}$$

Q_s mainly depends on the ohmic loss of the electrodes, while Q_p is determined mostly by the acoustic loss in the resonator. Q is a dimensionless parameter.

For each of the two resonant frequencies in Figure 5.1b the quality factors can be calculated with the equations above, but a more accurate method of obtaining Q_s and Q_p is to use the phase derivative.

$$Q_\mathrm{s,p} = \frac{f}{2} \left| \frac{\mathrm{d}\phi}{\mathrm{d}f} \right|_{f=f_\mathrm{s} \text{ or } f_\mathrm{p}} \tag{5.5}$$

In a ladder filter, the values of Q_s and Q_p determine the insertion loss and the selectivity.

Impedance Z_C The impedance Z_C is defined as the impedance of the plate capacitance C_0 at $(f_\mathrm{s} + f_\mathrm{p})/2$. Typical values are in the range between 50 Ω and 100 Ω.

5.7. Comparison between SAW and BAW Technology

Although the two technologies are very similar, BAW resonators have shown to be superior to SAW in some aspects.

- Especially above 2 GHz BAW resonators have higher Q values than SAW resonators. Due to this filters with lower insertion loss and better selectivity are available [100].
- The required BAW chip size is smaller than SAW (Factor of 2 for 1.8 GHz filters [32]).
- BAW resonators have a lower temperature drift of only up to -20 ppm/℃ compared to -45 ppm/℃ of SAW. This makes the design easier and less guardband is required for filters [100].

- BAW can operate up to higher frequencies than SAW [100].
- SAW filters require a hermetically sealed package, whereas BAW resonators only need a cavity [32].
- BAW technology is compatible with any wafer processing such as silicon or gallium arsenide [100]. So it is possible to integrate BAW resonators directly on radio ASICS and even above active die area. This is not the case with SAW resonators [31, 30, 29]. On the other hand, SAW resonators require only two layers of photo masks, compared to up to ten layers for BAW [100].

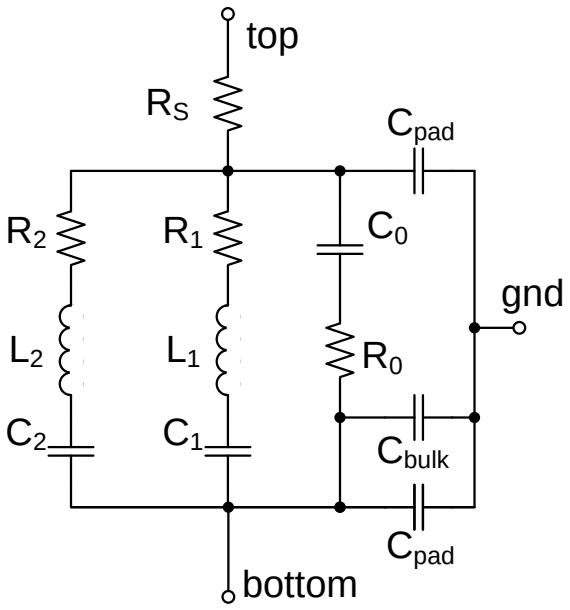
The decision whether to integrate BAW resonators directly above active area or as separate dies has to be made separately for every application. On the one hand, chip cost will increase if the small size resonators are processed on top of it and the total yield will decrease. On the other hand, assembly cost and packaging can be significantly cheaper for a SoC than for a SiP. Regarding miniaturization, a SoC will be hard to beat. According to [32], filters above active area are rather unlikely to become mainstream in the near future although it would be beneficial for certain applications. The feasibility has already been proven [31, 30, 29].

5.8. Resonators in the eCubes Transceiver

For the eCubes transceiver BAW resonators of SMR type have been used. Although above-IC resonators would have been very beneficial in this case, only separate dies have been available. A model of the employed resonators is shown in Figure 5.7. Adding R_{S} and R_0 to the BVD model results in the commonly used modified Butterworth-Van-Dyke model (MBVD). In order to get the component values, a resonator can be measured using a network analyzer and the model can be fitted to the measured s-parameters by means of a least mean squares algorithm as described in [77]. The model used for the e-Cubes resonators is shown in Figure 5.7. In addition to the MBVD model it contains parasitic capacitances C_{pad} representing the bond pads and another capacitor C_{bulk} which is required because the bottom electrode has a higher capacitance against ground than the top electrode. So the device is not symmetrical which will be important for the LNA design in Chapter 7. R_2, L_2, and C_2 represent the first harmonic of the resonator.

As commercially available filters always consist of a number of resonators, connected in a certain way, and encapsulated under a cavity it is not possible to contact single resonators out of such a device as it is required for the eCubes transceiver. However, on every BAW wafer there are test structures available distributed over the whole wafer, which are used for process calibration. Those test structures contain single resonators which can be contacted individually during the processing of a wafer. For the eCubes transceiver resonators from those test structures have been used and no dedicated mask set has been manufactured for eCubes BAWs. Nevertheless, two different types of resonators have been used in the eCubes transceiver:

- The first type of resonators has been taken from a wafer carrying filters for mobile



Component	Value
R_s	1.59 Ω
C_0	1.13 pF
R_0	18 mΩ
R_1	1.2 Ω
L_1	90 nH
C_1	50 fF
R_2	8 Ω
L_2	365 nH
C_2	4.7 fF
C_{pad}	42 fF
C_{bulk}	407 fF

Figure 5.7.: Model used for BAW resonators and component values of the 2.4 GHz device

phones with a resonant frequency of about 2.1 GHz. The model extraction for those resonators has been done by [71], using values measured in the lab.

- The second type of resonators has been designed for the eCubes transceiver. The mask set itself has not been modified, but an additional process step has been introduced. In order to mechanically compensate for the temperature drift of the resonators, an additional layer with an inverse temperature coefficient to that of the piezoelectric material has been introduced [76, 75]. Additionally the thickness of the resonators has been modified to shift the resonant frequency from 2.1 GHz to 2.45 GHz. The parameters for the model of those resonators have been estimated and provided by the designer of the resonators. So the model is less accurate than that for the 2.1 GHz resonators.

5.9. Temperature Compensation

In order to compensate for the temperature drift of the resonators, the oscillators include a bank of binary weighted capacitors to tune the frequency [71]. Copies of this bank of capacitors are switched in parallel to the filtering BAWs in the LNA. The oscillator itself is not part of this work, but as it determines the performance of the receiver, some results are shown below. The oscillator together with the transmitter architecture of the e-Cubes transceiver is described in [71].

Figure 5.8 shows the measured temperature drift of an uncompensated 2.1 GHz resonator together with a linear trendline. The temperature drift has a slope of -19 ppm/°C and can be compensated electrically by switching capacitors in parallel. Due to a non-linear behavior of the tuning network, the required digital codeword has to be calculated

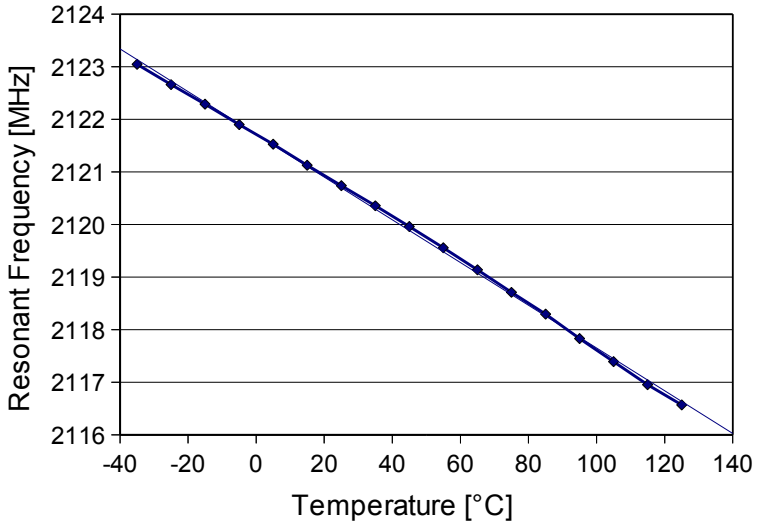


Figure 5.8.: Measured temperature drift of a 2.1 GHz resonator

using a second order polynomial, but the resulting temperature drift can be shown to be within ±40 ppm/°C over the whole temperature range [7]. Another way of tuning the resonance frequency is to apply a DC voltage across a resonator. The DC voltage changes the stiffness of the piezoelectric material and so the frequency is shifted. This effect is very linear and in the transmit path of the transceiver it is exploited for modulation. It cannot be used for process and temperature compensation however, because the tuning range is limited to 40 kHz/V [5]. The accurate compensation of the temperature drift is directly related to the performance of the receiver because a drift of only a few hundreds of kHz completely shifts the received signal out of the bandwidth of the IF filter. In [8, 10, 9] the temperature drift due to self-heating of the demonstrator during transmission is explored.

Figure 5.9 shows the temperature drift of two 2.4 GHz resonators. These samples have been mechanically temperature compensated as described in [76, 75]. The overall drift is indeed much smaller than that of the 2.1 GHz resonator, but unfortunately it differs very much from lot to lot and from wafer to wafer. So the remaining required codeword for the electrical compensation cannot be calculated by simply using a second order polynomial. For the 2.1 GHz version, only the coefficients of the polynomial have to be adapted for every resonator. In the 2.45 GHz version not only the coefficients but the whole equation differs from sample to sample. So the benefit of the mechanical temperature compensation is questionable because in the end it increases the system complexity instead of reducing it. It has to be mentioned however, that those samples have only been taken from test-wafers. Sample A in Figure 5.9 looks very promising, indicating that the mechanical temperature compensation might be a good solution.

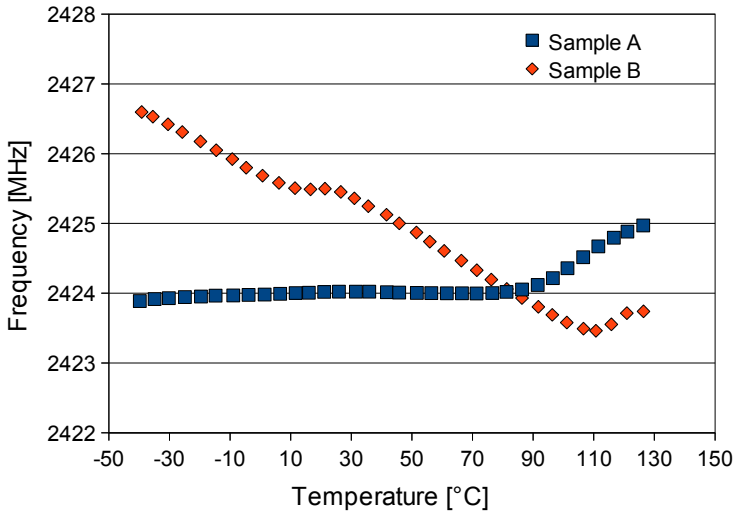


Figure 5.9.: Measured temperature drift of two 2.4 GHz resonators

5.10. Conclusion

This chapter explains the operating principle of BAW and SAW resonators. The differences are described and the advantages as well as the drawbacks of each technology are highlighted. It is shown how the BAW is modeled for circuit simulations and the temperature drift is explored. Finally the behavior of mechanically temperature compensated BAW resonators is evaluated.

6. Input Matching

This chapter describes the meaning of matching the impedance of the antenna to the input of the LNA. Different architectures are examined and finally a suitable topology for the e-Cubes transceiver is chosen.

6.1. Matching

Most RF circuits are matched to a certain impedance. This means that the antenna impedance equals the input impedance of the receiver and the output impedance of the transmitter. A very common value is $50\,\Omega$. In this way, the maximum power can be delivered from the antenna to the receiver and from the transmitter to the antenna. In most receiver frontends, the LNA is the first active block in the receiver chain, which follows right after the antenna or an external band select filter. In the case of an external filter, the input impedance is even more important because the transfer characteristics of many filters are sensitive to the termination [88]. In order to match the LNA to the antenna, a resistive input impedance is required. Different techniques are known to transform the input impedance to a desired value.

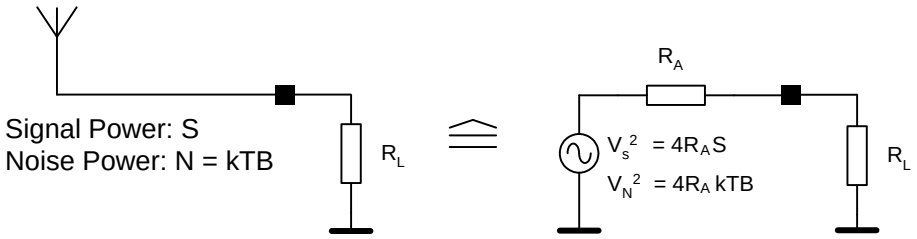


Figure 6.1.: Equivalent Circuit of an Antenna

Figure 6.1 shows the equivalent circuit of an antenna connected to a load resistor. The antenna is modeled as a voltage source in series with a noiseless resistor. The signal power delivered from the antenna to the load is denoted as S, and N is the noise power which can be calculated as $N = \mathrm{k}TB$. The signal voltage V_S can thus be expressed as

$$V_\mathrm{S} = \sqrt{4R_\mathrm{A}S}, \tag{6.1}$$

and the noise voltage is

$$V_\mathrm{N} = \sqrt{4R_\mathrm{A}\mathrm{k}TB}. \tag{6.2}$$

The signal power P_L which is delivered to the load can be calculated as

$$P_\mathrm{L} = V_\mathrm{S}^2 \frac{R_\mathrm{L}}{(R_\mathrm{A} + R_\mathrm{L})^2}. \tag{6.3}$$

As explained in [99] the Noise Factor F can be expressed as

$$F = \frac{\text{total output noise power}}{\text{output noise power due to input source}}.$$

By making $R_{\mathrm{A}} = R$ and $R_{\mathrm{L}} = \alpha R$, and assuming that the load resistor adds noise to the signal itself, the above expression evaluates to:

$$\begin{aligned} F &= \frac{4\mathrm{k}TB\left[\frac{\alpha}{(1+\alpha)^2} + \frac{1}{(1+\alpha)^2}\right]}{4\mathrm{k}TB\frac{\alpha}{(1+\alpha)^2}} \\ &= \frac{1+\alpha}{\alpha} \end{aligned} \tag{6.4}$$

Equation 6.4 shows that when the load is matched to the antenna ($\alpha = 1$), $F = 2$ and the NF is 3 dB respectively.

Figure 6.2 shows the noise figure (a), the ratio of the total power to the power delivered to the load (b), and the voltage across the load resistor (c) for different values of α.

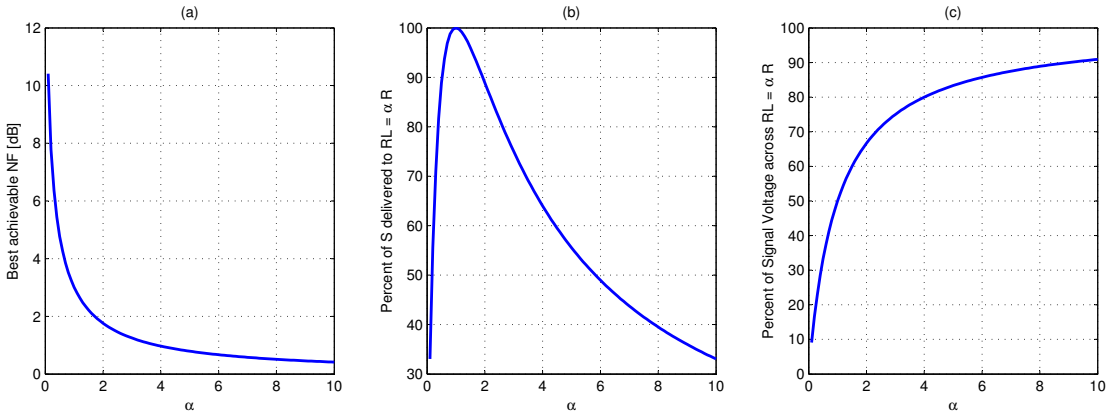


Figure 6.2.: Matching Aspects

A very obvious way to achieve a resistive input impedance of a certain value is to add a shunt resistor with the desired value in front of the input transistor. As shown in Figure 6.4 however, this approach imposes a lower limit of 3 dB on the noise figure. So this is not a very good idea.

6.1.1. Resistive Feedback

Figure 6.3 shows an LNA using resistive feedback to achieve a certain input impedance. As shown in [88], the real part of its input impedance can be expressed as:

$$R_{\mathrm{in}} = \frac{R_{\mathrm{F}}}{1 + \frac{R_{\mathrm{L}}}{R_{\mathrm{S}}}} \tag{6.5}$$

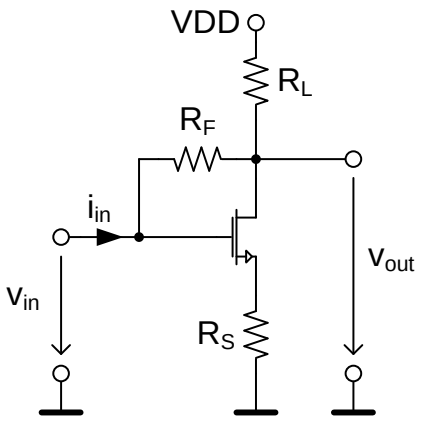


Figure 6.3.: Matching with resistive feedback

Although the resistive feedback also contributes to the overall noise, the performance of such a circuit is better than with a simple shunt resistor [88]. Due to its broadband input matching capabilities, this circuit is often used for wideband LNAs as for example in [69], [26] or [68].

6.1.2. Common Gate

Another easy way to achieve a resistive input of a certain value is to implement an LNA in a common gate configuration with an input impedance of $Z_{\mathrm{in}} = \frac{1}{g_{\mathrm{m}}}$ as shown in Figure 6.4. In terms of noise figure however, also this topology does not lead to an optimum, because there is still a noisy resistor in the signal path, although in this case, it is not a device, but it is the channel resistance of the transistor.

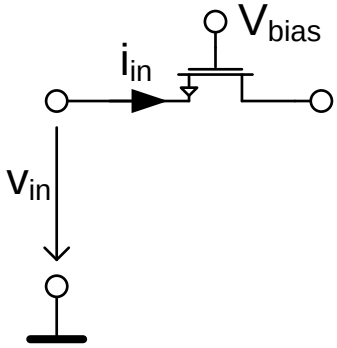


Figure 6.4.: Common Gate Amplifier

6.1.3. Inductive Source Degeneration

Typically LNAs make use of common source amplifier input stages. The input of a common source amplifier is purely capacitive as it is only defined by the gate-source capacitance C_{GS}. A very common approach of generating a resistive component in the input impedance is to apply inductive source degeneration. This technique uses a series inductor L_{S} following the source of the input transistor, as shown in Figure 6.5. In contrast to the resistive feedback approach, inductive source degeneration is specially suitable for narrowband LNAs.

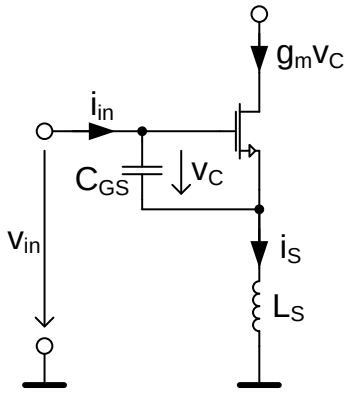


Figure 6.5.: Inductive Source Degeneration

With $v_{\mathrm{C}} = \frac{i_{\mathrm{in}}}{\mathrm{j}\omega C_{\mathrm{GS}}}$ and $i_{\mathrm{S}} = i_{\mathrm{in}} + g_{\mathrm{m}} v_{\mathrm{C}}$, the input impedance Z_{in} can be calculated as:

$$\begin{aligned} Z_{\mathrm{in}} &= \frac{v_{\mathrm{in}}}{i_{\mathrm{in}}} \\ &= \frac{v_{\mathrm{C}} + \mathrm{j}\omega L_{\mathrm{S}} \cdot i_{\mathrm{S}}}{i_{\mathrm{in}}} \\ &= \frac{\frac{i_{\mathrm{in}}}{\mathrm{j}\omega C_{\mathrm{GS}}} + \mathrm{j}\omega L_{\mathrm{S}} \cdot \left(i_{\mathrm{in}} + g_{\mathrm{m}} \frac{i_{\mathrm{in}}}{\mathrm{j}\omega C_{\mathrm{GS}}} \right)}{i_{\mathrm{in}}} \\ &= \frac{1}{\mathrm{j}\omega C_{\mathrm{GS}}} + \mathrm{j}\omega L_{\mathrm{S}} \cdot \left(1 + \frac{g_{\mathrm{m}}}{\mathrm{j}\omega C_{\mathrm{GS}}} \right) \\ &= \frac{g_{\mathrm{m}} L_{\mathrm{S}}}{C_{\mathrm{GS}}} \cdot \mathrm{j} \left(\omega L_{\mathrm{S}} - \frac{1}{\omega C_{\mathrm{GS}}} \right) \end{aligned} \tag{6.6}$$

L_{S} can be used to tune the real part of the input impedance to a desired value. As the resistive term is generated by a pure reactance however, it does not introduce any noise to the circuit, so it does not degrade the noise figure. With another series inductor L_{G} ahead of the gate of the transistor as shown in Figure 6.6, the reactance can be tuned to zero. Equation 6.7 shows the input impedance of an inductively degenerated common source LNA with a series inductor L_{G}.

$$
\begin{aligned}
Z_{\mathrm{in}} &= \frac{g_{\mathrm{m}} L_{\mathrm{S}}}{C_{\mathrm{GS}}} \cdot \mathrm{j}\left(\omega L_{\mathrm{S}} - \frac{1}{\omega C_{\mathrm{GS}}}\right) + \mathrm{j}\omega L_{\mathrm{G}} \\
&= \frac{g_{\mathrm{m}} L_{\mathrm{S}}}{C_{\mathrm{GS}}} \cdot \mathrm{j}\left(\omega L_{\mathrm{G}} + \omega L_{\mathrm{S}} - \frac{1}{\omega C_{\mathrm{GS}}}\right)
\end{aligned} \tag{6.7}
$$

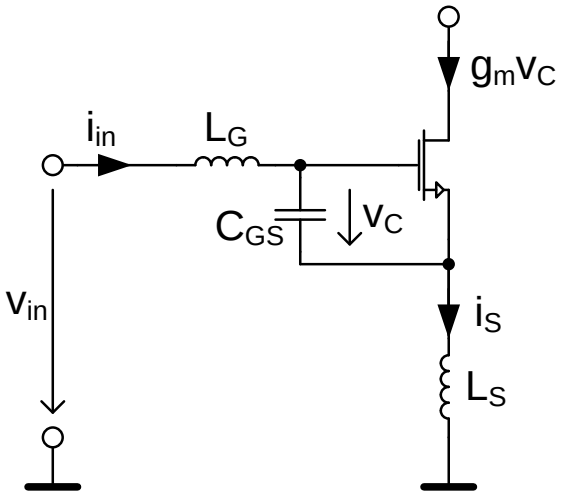


Figure 6.6.: Inductive Source Degeneration with Additional Series Inductor

6.2. Resonant Circuit

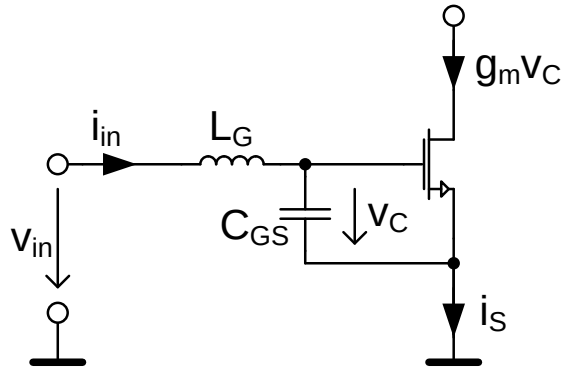


Figure 6.7.: Resonant Circuit with LNA and inductor

As already pointed out, the input of a common source amplifier is purely capacitive in its nature, and one might wonder, if it is even necessary to deliver the maximum power from the antenna to the LNA. What a common source amplifier requires at its input is a high voltage and not necessarily the maximum power. A method to increase the voltage at

the input of the LNA considerably is to build a resonant circuit for the desired frequency, as shown schematically in Figure 6.7 [95]. With the series inductor L_G in front of the capacitive LNA input represented by C_{GS} the circuit can be brought into resonance, and the input impedance is determined by the parasitic resistance of the inductor and the transistor. This very small parasitic series resistance can be transformed mathematically to a very large parallel resistance where the input power is not absorbed but reflected while the voltage at the LNA input is very high. Critical about this approach is however, that if there are any discontinuities in the wave resistance between the antenna and the LNA, the reflected power is reflected again leading to distortions in the original signal.

6.3. Implemented eCubes Matching Network

The proposed concept of the matching network as presented in [3, 5] matches the antenna to the losses of the on-chip resonant circuit in order to achieve the highest possible voltage amplification and to prevent reflections between the LNA and the antenna.

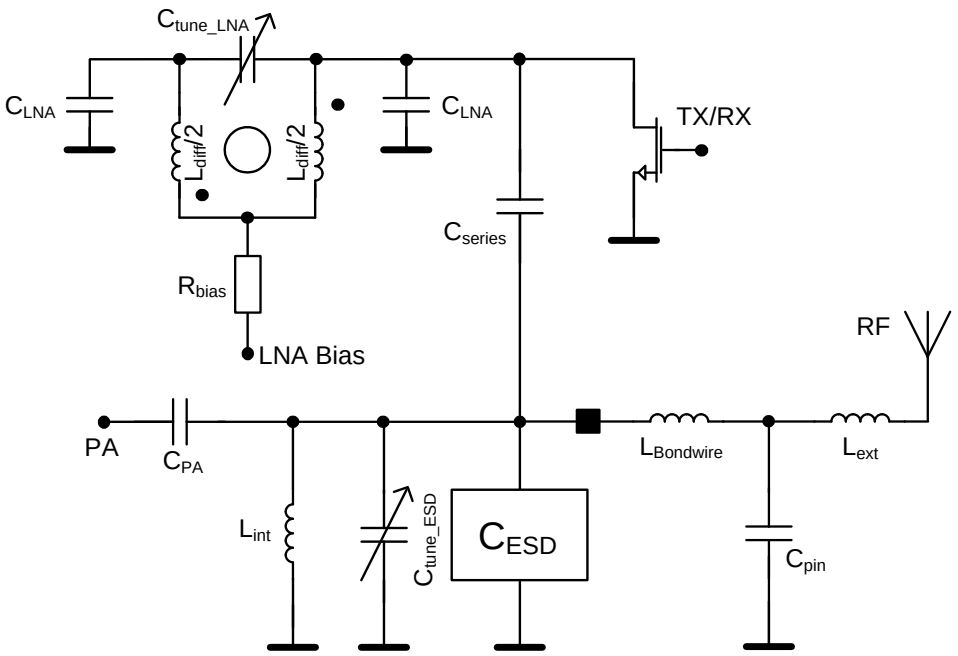


Figure 6.8.: Implemented on-chip matching network

Figure 6.8 shows the implementation of the matching network. A differential inductor L_{diff} generates a resonant circuit in combination with the capacitive input of the differential LNA, represented by two capacitors C_{LNA}. It also provides a single-ended to differential conversion and allows to feed the bias voltage to the input transistors. A bank of varactors, represented by C_{tune_LNA}, is used to tune the resonant frequency. The losses of the resonant circuit are dominated by the parasitic resistance of the inductor L_{diff} which is in the range of a few Ω. As L_{diff} is an on-chip inductor in standard CMOS without a special RF process extension, its Q factor is only around 6. The series resistance of the resonant

Component	Value
C_{LNA}	105 [fF]
C_{tune_LNA}	500 - 1500 [fF]
L_{diff}	6.8 [nH]
R_{bias}	8 [kΩ]
C_{series}	500 [fF]
C_{PA}	4 [pF]
C_{tune_ESD}	500 - 1500 [fF]
C_{pin}	200 [fF]
L_{int}	6.8 [nH]
$L_{Bondwire}$	2 [nH]
L_{ext}	2.5 [nH]

Table 6.1.: Component values of the passive devices used in the matching network

circuit can be converted to an equivalent parallel resistance of 630 Ω, which has to be matched to the 50 Ω required for the antenna. This resistance of 630 Ω is first transformed to 100 Ω by making use of a capacitive voltage divider consisting mainly of C_{series} and C_{ESD}. As C_{ESD} is very large, another on-chip inductor L_{int} is used to compensate a part of it. C_{tune_ESD} is a bank of switched capacitors and can be used to fine-tune the circuits process variations. The remaining resistance of 100 Ω is then transformed to 50 Ω by making use of the inductive bond-wire and an external inductor L_{ext} which can be integrated into the antenna. C_{PA} is the coupling capacitor of the transmit power amplifier. In transmit mode, when the transistor acting as TX/RX switch is on, the upper part of the matching network is pulled to ground. C_{series} is then parallel to C_{ESD} and L_{int}. With a different setting of C_{tune_ESD}, the network can be brought into resonance in transmit mode. Table 6.1 contains the components values of all relevant devices in the matching network.

Figure 6.9 shows the achievable input impedance in receive mode, depending on the tuning codewords and Figure 6.10 shows the achieved gain and noise figure at the LNA input when matched to 50 Ω.

As shown in Figure 6.10, the matching network alone accounts for a considerable noise figure. This is caused mainly by the lossy on-chip inductors. The performance would be much better if off-chip passives were used or at least a CMOS process with better RF performance.

6.4. Conclusion

This chapter explains the concept of input matching. Different matching network topologies are shown and a novel architecture for a combined matching network for the receiver and the transmitter is developed. This new architecture requires no off-chip passives and it includes also the RX/TX switch.

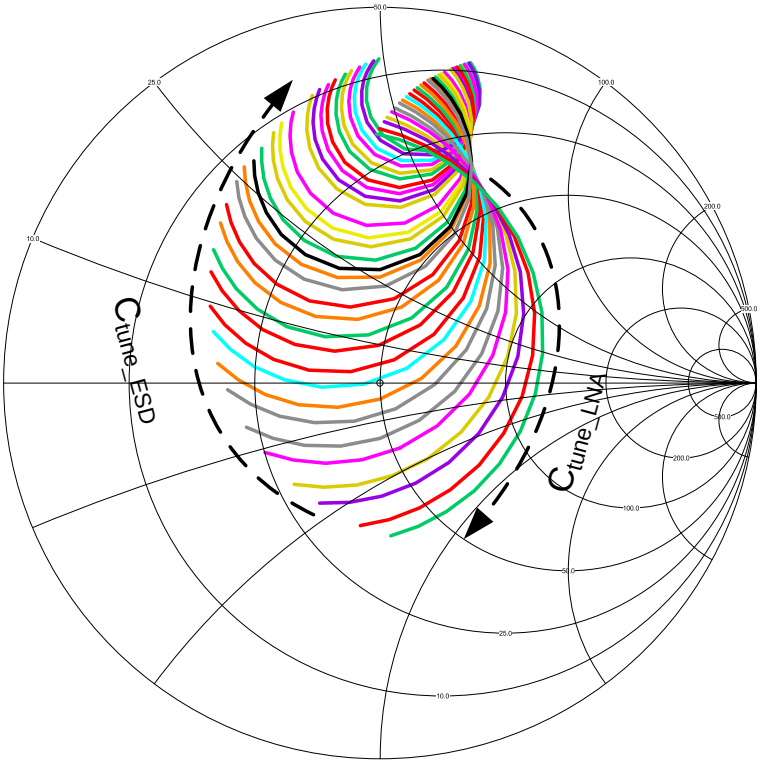


Figure 6.9.: Simulated input impedance, depending on tuning capacitors

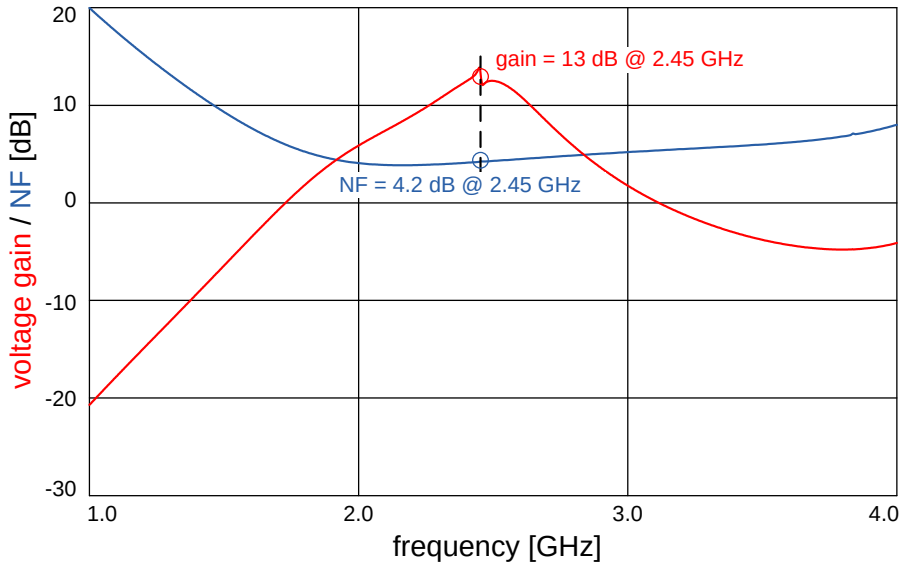


Figure 6.10.: Simulated voltage gain and noise figure of the matching network

7. Low Noise Amplifier (LNA)

This chapter describes in detail the architecture of the applied LNA. The performance of the LNA has a strong impact on the performance of the whole receiver frontend. Its task is to provide gain while adding as little noise as possible to the amplified signal. A low noise amplifier providing high gain relaxes the noise requirements of the following stages, because their noise factor can be divided by the gain of the LNA as shown in Equation 7.1 for a system containing three stages each having gain G and noise factor F as shown in Figure 7.1. F represents the noise figure in linear scale, often referred to as Noise Factor.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} \tag{7.1}$$

[96]

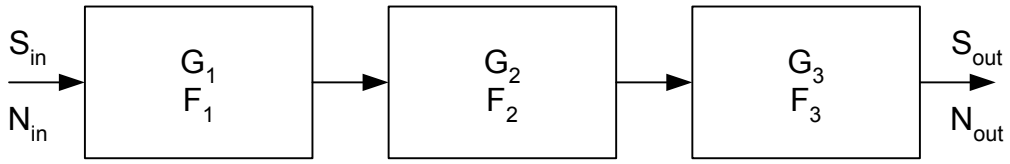


Figure 7.1.: Noise figure of cascaded stages

7.1. LNA Circuit

As the whole eCubes receiver frontend is fully differential, also the implemented LNA is a differential circuit.

The schematic of the proposed LNA as it has been presented in [3] is shown in Figure 7.2. The input stage is a differential common source stage with cascode transistors. The load of the amplifier consists of an active inductor stage with impedance

$$Z = \frac{1}{g_\mathrm{m}} \frac{1 + \mathrm{j}\omega RC}{1 + \frac{\mathrm{j}\omega C}{g_\mathrm{m}}}. \tag{7.2}$$

A source follower is used as output stage in order to drive the following on-chip polyphase network. The feedback path in the source follower output stage is used to improve the output impedance and linearity.

Connected inside the cascode, the LNA contains the two BAW resonators for filtering together with the tuning capacitors. The low impedance nodes inside the cascode have

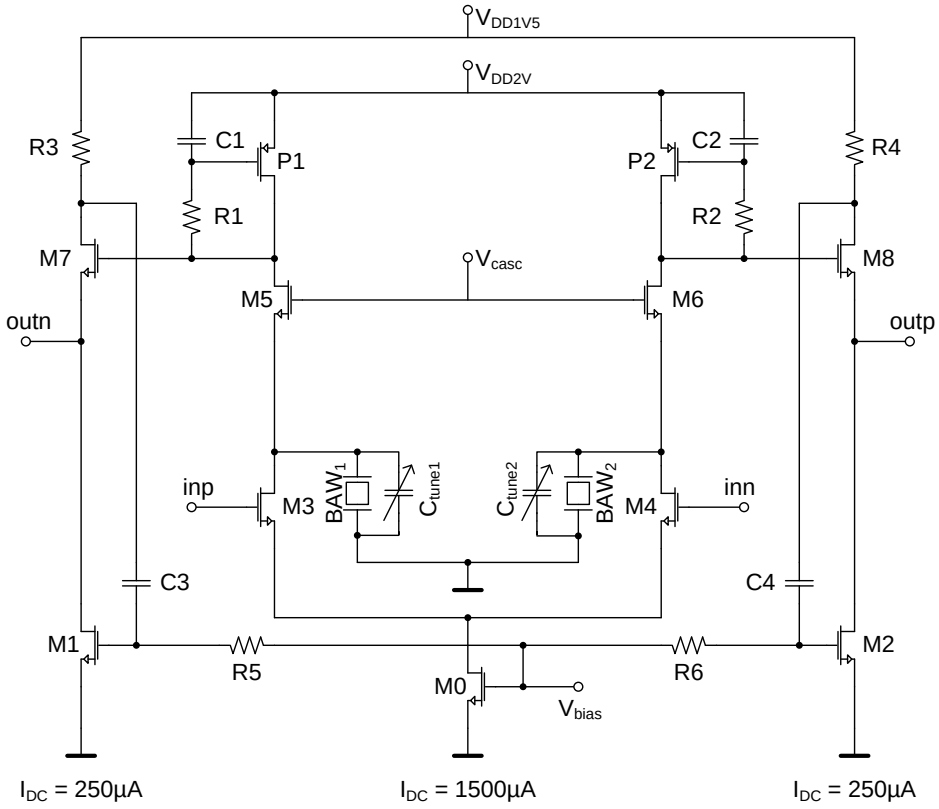


Figure 7.2.: LNA Circuit

been chosen for inserting the BAWs because the impedance of a BAW resonator is only in the range of 2 kΩ, even at its parallel resonance frequency where the impedance is a maximum. When all tuning capacitors are switched in parallel, the impedance even drops to about 500 Ω. As the BAWs are connected via wire-bonds, ESD protection circuits are required which are not shown in the schematic. These ESD protection circuits represent a very large parasitic capacitance which cannot be switched off. For the selectivity of the BAW filters, it would be better to insert them into high impedance nodes, for example in parallel to the load. The drawback in this case would be that the gain of the LNA would drop significantly with 500 Ω in parallel to the high impedance active inductor stage. The applied BAW resonators are not symmetrical. As the bottom electrode is much closer to the substrate than the top electrode, it has a higher capacitance against ground as described in Chapter 5. Due to that, two resonators are used, one in each branch of the differential amplifier, instead of only one between the two branches.

Figure 7.3 shows the simulated voltage gain of the LNA excluding the matching network. One can see that the frequency difference between the series and the parallel resonance is 28 MHz when no tuning capacitors are switched in parallel. By placing the local oscillator between the series and the parallel resonance frequency such that the desired signal is exactly at the parallel resonant frequency and the image is exactly at the series resonant frequency, an image rejection of up to 24 dB can be achieved. As the BAW resonators have a temperature drift of -19 ppm/°C, a part of the tuning range has to

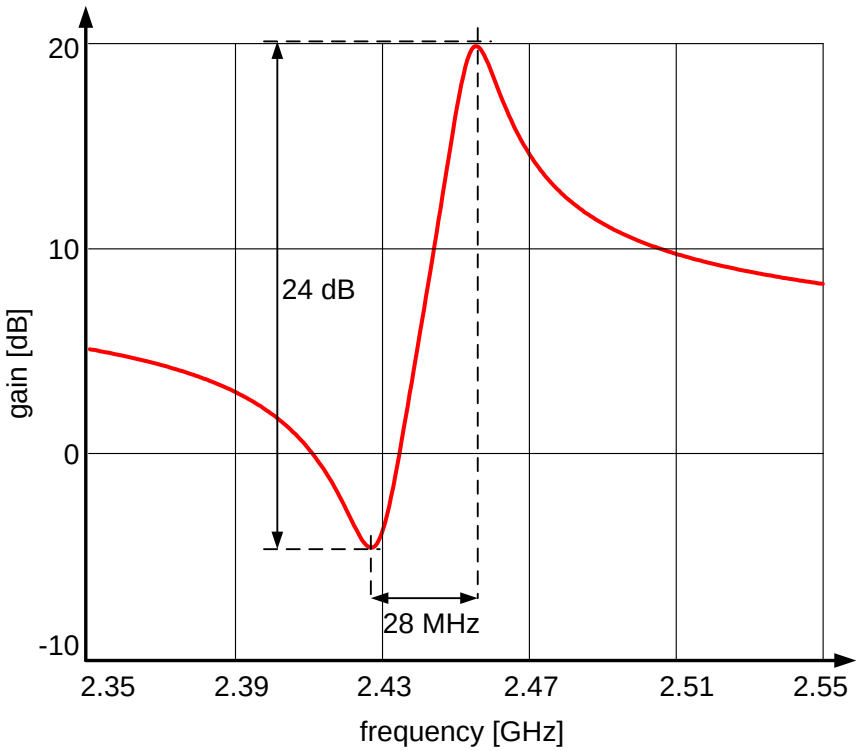


Figure 7.3.: Voltage gain and image rejection of LNA including BAWs

be spent in order to compensate for temperature variations. This reduces the difference between the series and the parallel resonance to about 23 MHz. In the presented architecture an IF of 10.7 MHz has been chosen because of the availability of ceramic filters for this frequency. So it is possible to place the image very close to the series resonance. Tables 7.2 and 7.1 show all component values of the devices used in the LNA.

Resistor	R [Ω]	Capacitor	C [fF]
R1	5,000	C1	30
R2	5,000	C2	30
R3	1,000	C3	700
R4	1,000	C4	700
R5	8,000	Δ C_{tune1}	1,000
R6	8,000	Δ C_{tune1}	1,000

Table 7.1.: Component values of the passive devices used in the LNA

Transistor	W [µm]	L [µm]	I_{DS} [µA]	g_m [mS]
M0	600	0.36	1,500	28.5
M1	100	0.36	250	4.8
M2	100	0.36	250	4.8
M3	80	0.12	750	11.8
M4	80	0.12	750	11.8
M5	15	0.12	750	6.1
M6	15	0.12	750	6.1
M7	15	0.12	250	3.4
M8	15	0.12	250	3.4
P1	5	0.12	750	1.7
P2	5	0.12	750	1.7

Table 7.2.: Dimensions of the transistors used in the LNA

7.2. Active Inductor

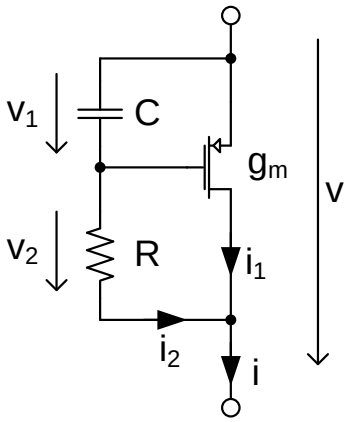
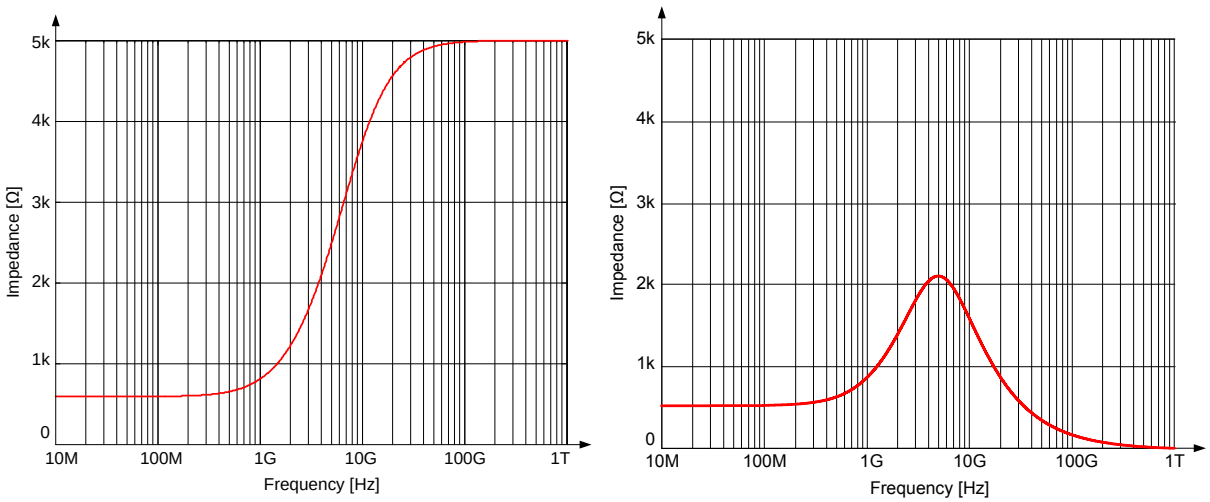


Figure 7.4.: Active inductor

Figure 7.4 shows the load the LNA. From Equation 7.2 one can see that for very low frequencies the load impedance $Z = \frac{1}{g_\mathrm{m}}$ because resistor R connects gate and drain of the transistor. For very high frequencies the capacitor C short-circuits source and gate of the transistor, leading to $Z = R$. For the range in between, where $\frac{1}{RC} \ll \omega \ll \frac{g_\mathrm{m}}{C}$, the impedance $Z \sim \frac{\mathrm{j}\omega RC}{g_\mathrm{m}}$, which is an inductive behavior as the impedance increases with frequency. This intuitive examination of the circuit can be confirmed by deriving the impedance of the active inductor stage as shown in Equation 7.3.



(a) Calculated Impedance of active inductor

(b) Simulated Impedance with nonideal devices

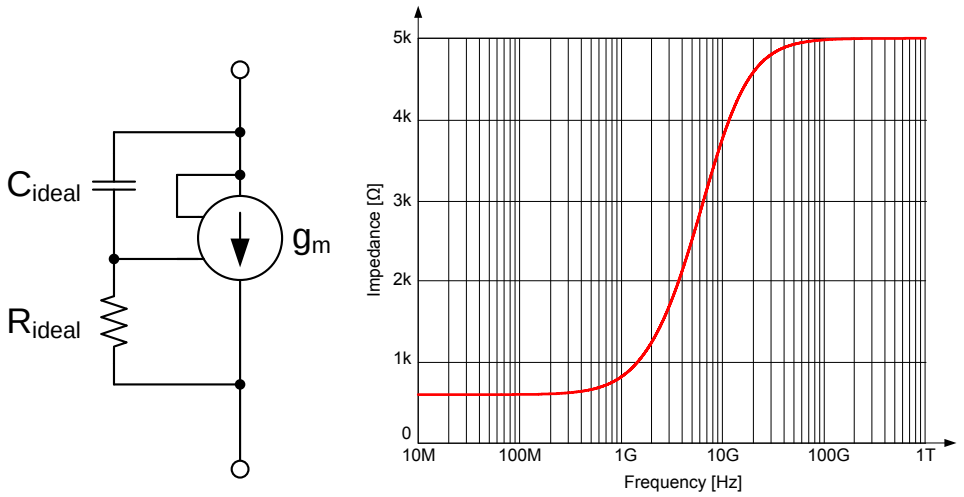
Figure 7.5.: Calculated and simulated impedance

$$
\begin{aligned}
v_1 &= \frac{i_2}{\mathrm{j}\omega C} \\
v_2 &= i_2 R \\
i_1 &= g_\mathrm{m} v_1 = g_\mathrm{m} \frac{i_2}{\mathrm{j}\omega C} \\
Z &= \frac{v}{i} = \frac{v_1 + v_2}{i_1 + i_2} = \frac{\frac{i_2}{\mathrm{j}\omega C} + i_2 R}{g_\mathrm{m} \frac{i_2}{\mathrm{j}\omega C} + i_2} \\
&= \frac{i_2(\frac{1}{\mathrm{j}\omega C} + R)}{i_2(\frac{g_\mathrm{m}}{\mathrm{j}\omega C} + 1)} = \frac{1 + \mathrm{j}\omega RC}{g_\mathrm{m} + \mathrm{j}\omega C} \\
Z &= \frac{1}{g_\mathrm{m}} \cdot \frac{1 + \mathrm{j}\omega RC}{1 + \frac{\mathrm{j}\omega C}{g_\mathrm{m}}}
\end{aligned}
\tag{7.3}
$$

Figure 7.5a shows the calculated impedance of the inductor stage over frequency. Circuit simulations however show a different behavior of the load stage than expected from the intuitive approach and from Equation 7.3. The simulated value of the load impedance is shown in Figure 7.5b. One can see, that for low frequencies, the assumptions are correct, but for higher frequencies, they are not. Instead of the high-pass behavior which has been calculated and which is shown in Figure 7.5a, the simulated impedance in Figure 7.5b shows the band-pass behavior of a resonant circuit.

By replacing R and C in Figure 7.4 with ideal devices, and the MOS transistor with an ideal voltage controlled current source, as shown in Figure 7.6a, it can be shown that the assumptions in 7.3 are correct, and the band-pass behavior is caused by parasitics. Figure 7.6b shows the simulated impedance of the active inductor consisting of ideal

devices from Figure 7.6a.

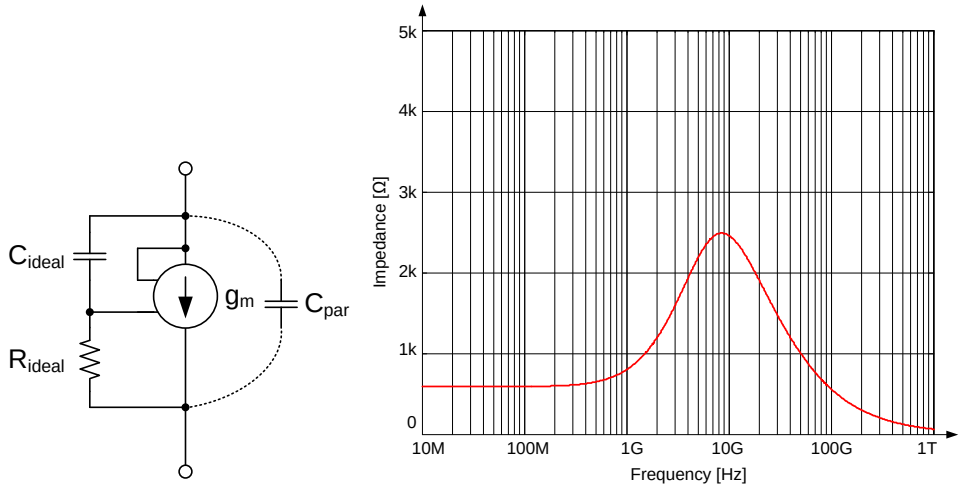


(a) Ideal devices

(b) Voltage controlled current source and ideal R and C

Figure 7.6.: Simulated impedance with ideal devices

By including a small parasitic capacitor C_{par} of only 2.5 fF as shown in Figure 7.7a in the calculation, the calculated impedance shown in Figure 7.7b drops to the non-ideal simulated values.



(a) Active inductor with parasitic Capacitor

(b) Calculated impedance with parasitic capacitor

Figure 7.7.: Calculated impedance with parasitic capacitor in parallel to ideal devices

Basically the same inductive behavior can be achieved with an NMOS device instead of the PMOS device shown in Figure 7.4. The NMOS topology is described in [95]. In this case the capacitor and resistor have to be swapped of course. The impedance can

then be calculated in exactly the same way, but in the given technology, there is only a common p-substrate for all NMOS transistors, and there are no separate p-wells. So if an NMOS were used in the applied topology instead of the PMOS its body-effect would have a strong impact on the behavior. That is why the PMOS topology has been chosen.

7.3. Source Follower with Feedback

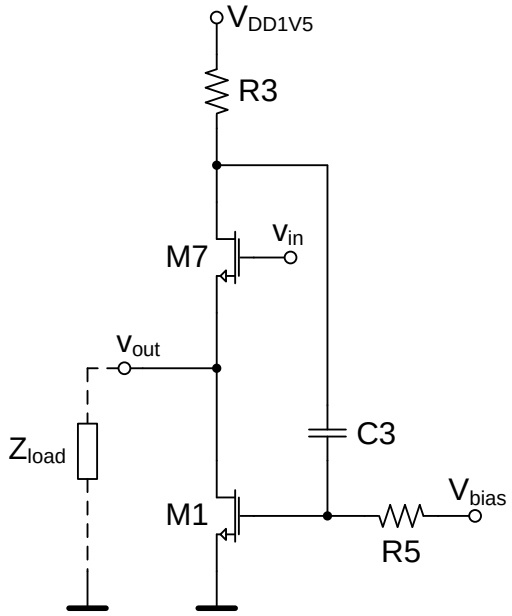


Figure 7.8.: Source Follower Output Stage with Feedback

Figure 7.8 shows the source follower output stage of the LNA. In contrast to a typical source follower, the presented output stage contains a feedback path. This feedback path is used to reduce the output impedance and to increase the linearity of the stage. Assuming that no load is connected and $Z = \infty$, then the feedback has no effect at all. The current through the transistors is defined by V_{bias} and a change in the input signal v_{in} only results in a shift of v_{out}, by changing the drain-source voltage of the input transistor $M7$. An additional voltage drop across resistor $R3$ does not occur. With a load impedance connected however, when $Z \neq \infty$, an AC-current flows into the load. This AC current is not defined by the current source transistor $M1$. It causes a voltage drop across $R3$ which is fed back to the current source $M1$ via $C3$ where the current is then increased or reduced respectively. Resistor $R5$ is sufficiently large to decouple V_{bias} from the AC-signal at the gate of $M1$. By controlling the current in the current source transistor $M1$, the output voltage v_{out} does not change, but the output impedance is lowered and linearity is improved.

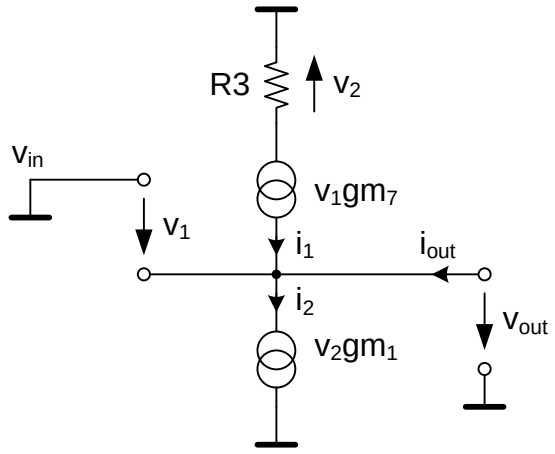


Figure 7.9.: Source Follower small signal analysis

From the small signal equivalent circuit shown in Figure 7.9, the output impedance neglecting parasitics can be calculated as shown in Equation 7.4

$$\begin{aligned} Z_{\mathrm{out}} &= \frac{v_{\mathrm{out}}}{i_{\mathrm{out}}} \\ v_{\mathrm{out}} &= -v_1 \\ i_{\mathrm{out}} &= i_2 - i_1 \\ &= v_2 \cdot g_{\mathrm{m}_1} - v_1 \cdot g_{\mathrm{m}_7} \\ &= -v_1 \cdot g_{\mathrm{m}_7} \cdot g_{\mathrm{m}_1} \cdot R - v_1 \cdot g_{\mathrm{m}_7} \\ Z_{\mathrm{out}} &= \frac{-v_1}{-v_1 \cdot g_{\mathrm{m}_7} \cdot g_{\mathrm{m}_1} \cdot R - v_1 \cdot g_{\mathrm{m}_7}} \\ &= \frac{1}{g_{\mathrm{m}_7} \cdot (g_{\mathrm{m}_1} \cdot R + 1)} \end{aligned} \tag{7.4}$$

7.4. Simulation Results

Figure 7.10 shows the voltage gain and the NF of the LNA together with the matching network for two different settings of the BAW tuning capacitors. If the BAWs are not tuned at all (except for parasitic capacitances which cannot be switched off) the voltage gain is 31.5 dB at a NF of 4.6 dB. When all tuning capacitors are switched on, the gain drops to 28.3 dB at a NF of 5.4 dB.

In order to compare the presented LNA to other reported implementations, a figure of merit (FOM) is required. Most reported LNAs are designed with their output matched to 50 Ω. Commonly used FOMs therefore include the power gain of the LNA instead of the voltage gain. So in order to compare the presented LNA to others, Figure 7.11 shows the simulated power gain. For this simulation, the output of the LNA is connected differentially to a 400 Ω load, which matches the output impedance of the source follower stage. The simulation setup is shown in Figure 7.12.

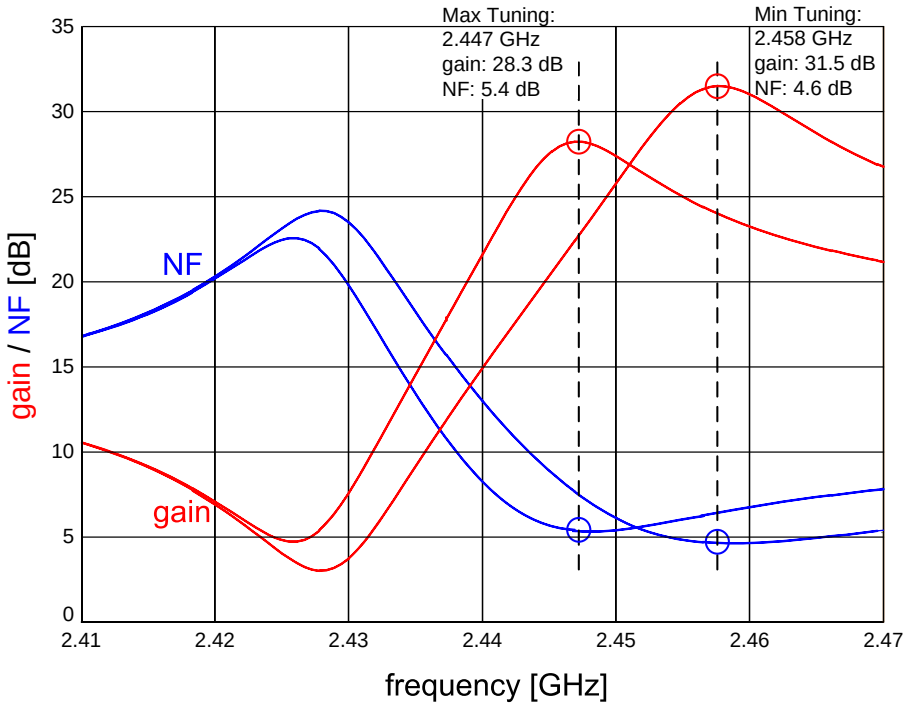


Figure 7.10.: Simulated gain and NF with different tuning words

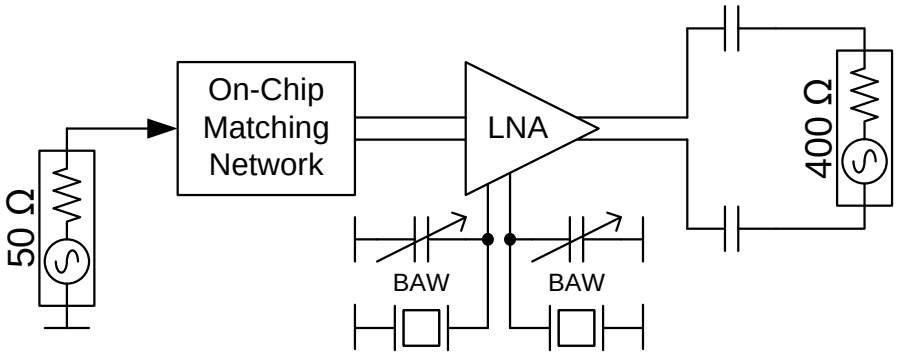


Figure 7.12.: Simulation setup for LNA power gain

Connecting a low ohmic load to the output of course reduces the voltage gain. The highest voltage gain is achieved with open outputs. The gain in Figure 7.10 is achieved when the LNA is connected to its real load, the polyphase network followed by the mixer. Figure 7.13 once again shows the simulated voltage gain under the three conditions open, matched load, and high ohmic real load. As expected, the difference between the open outputs and the matched outputs is 6 dB.

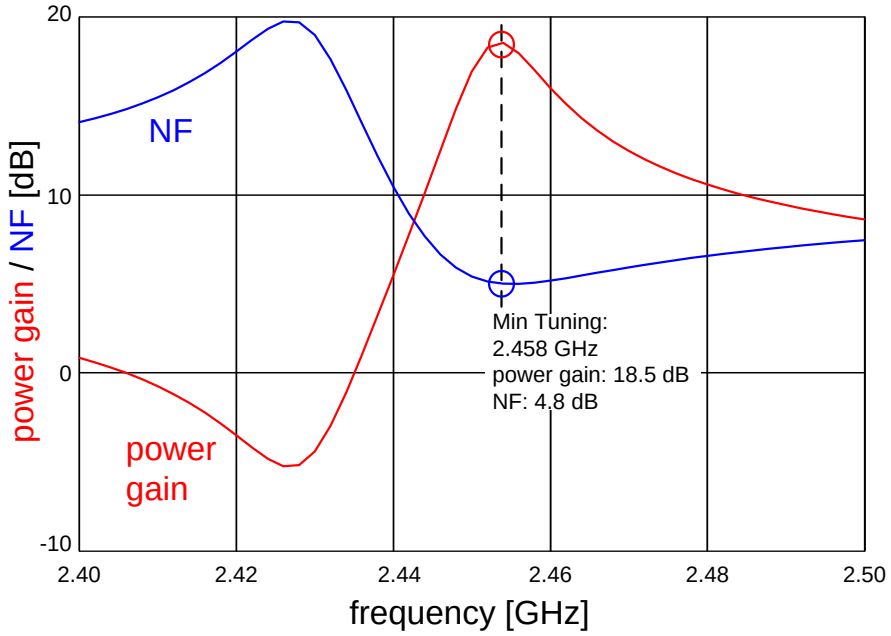


Figure 7.11.: Power gain of the LNA

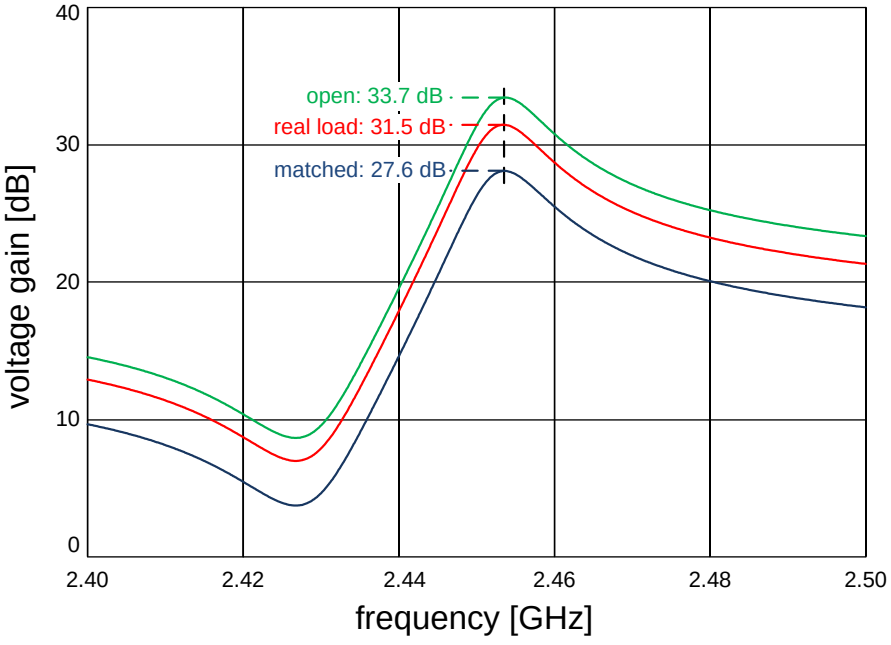


Figure 7.13.: Simulated voltage gain with different loads

Figure 7.14 shows the simulated P1dB of the LNA when connected to the matched 400 Ω load.

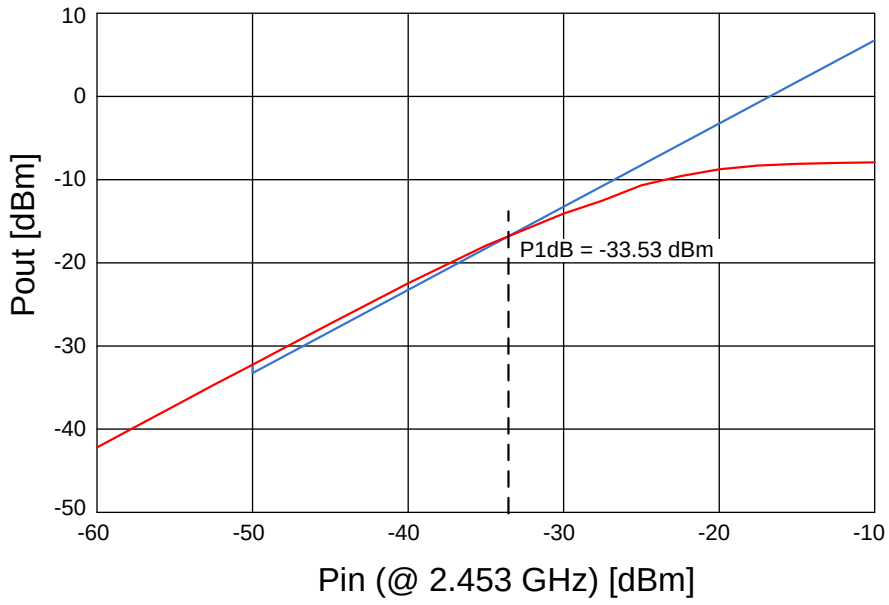


Figure 7.14.: Simulated P1dB of matched LNA

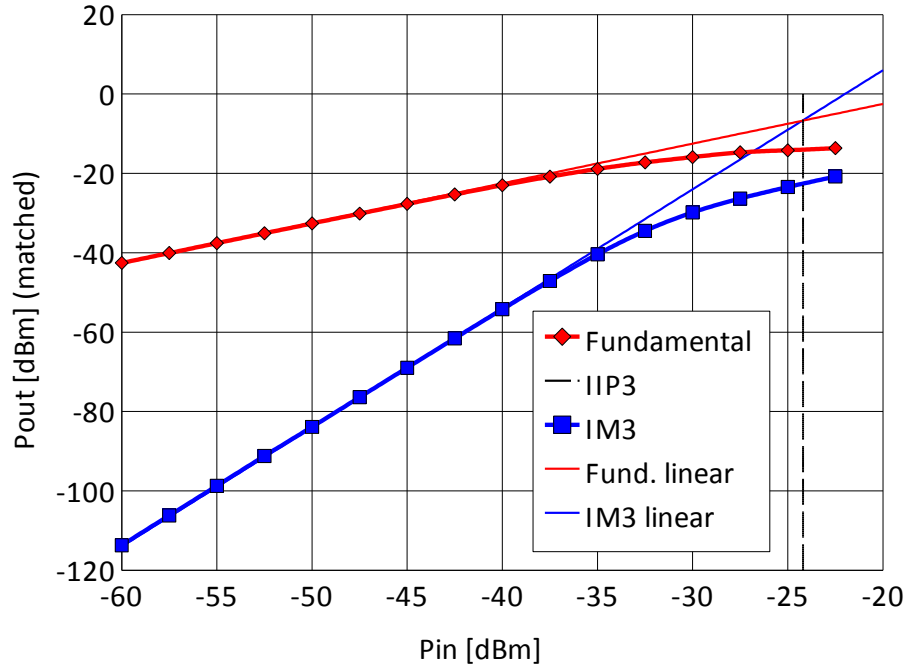


Figure 7.15.: Simulated IIP3 of matched LNA

Figure 7.15 shows that the simulated IIP3 of the output matched LNA is -24 dB. These results are in good agreement with the rule of thumb that the difference between the P1dB and the IIP3 should be about 9.6 dB. The expected difference between IIP3 and P1dB can be given exactly, because both figures are defined by the same polynomial. In the

definition of the FoMs for linearity (IIP3, P1dB), it is assumed that the nonlinear behavior of a circuit can be approximated by a third order polynomial as shown in Equation 7.5 [99].

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{7.5}$$

With a single tone input, the P1dB can be calculated as

$$A_{1-\mathrm{dB}} = \sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|}, \tag{7.6}$$

and by applying two tones, the IIP3 can be calculated as

$$A_{\mathrm{IP3}} = 2\sqrt{\frac{\alpha_1}{3\alpha_3}}, \tag{7.7}$$

where $A_{1-\mathrm{dB}}$ and A_{IP3} are the amplitudes of the input signals.

The coefficients of the polynomial in Equation 7.5 can be derived from both, the P1dB and the IIP3. If these results are not the same, it means that either there is a measurement error, or the simple third order polynomial is not sufficient to describe the system. In this case it might be necessary to increase the order of the polynomial or to take the frequency response of the system into account [70].

7.5. Figure of Merit

As mentioned before, in order to compare the performance of the LNA to other implementations, a FoM is required, which includes all relevant performance indicators. These performance indicators are:

- P_{DC}: Power consumption in mW. Most systems are constrained in power consumption. If unlimited power is available, basically any desired performance can be achieved. That is why power consumption is a very important factor in the FoM because all other parameters are a trade-off with power consumption. This can be easily illustrated by simply connecting two LNAs in parallel and assuming that input matching can be maintained. If one LNA outputs a signal voltage V_{S}, then the output signal of two LNAs will be $2 \cdot V_{\mathrm{S}}$. The signal voltages can be added, because they are correlated. The output noise voltage V_{N} on the other hand will only be increased by the square root of two $\sqrt{2} \cdot V_{\mathrm{N}}$, because the noise voltages of the two LNAs are not correlated. So the noise power is increased by a factor of two while signal power is increased by a factor of four. This means that the SNR is doubled at the cost of a doubled power consumption and of course area [19].

- G: Gain. Comparing the gains of different LNAs is not always straight forward. Discrete LNAs are always matched to a certain input impedance and a certain output impedance. This is also true for LNAs used in integrated receiver frontends with off-chip image reject filters. The output impedance of those LNAs is 50 Ω in most cases, equal to the input impedance. Driving such loads requires output

buffers which consume current and do not improve the performance of the LNAs. For those discrete LNAs power gain is a very important performance indicator. On the other hand, LNAs applied in fully integrated receiver frontends do not have to drive large loads, and they are not matched to a certain output impedance. In this case voltage gain is the more interesting performance parameter. But of course it is not fair to compare the voltage gain of an LNA which is matched to a low-ohmic load with an LNA that is connected to a high ohmic load. So in order to allow for a fair comparison, power gain has to be included in the FoM. For this reason it has been simulated and shown in Figure 7.11 for the presented LNA although it is not relevant for the application. In literature, a very common mistake is mixing up voltage and power gain. Only if the input and output of an amplifier are matched and the input and output impedances are equal, then voltage and power gain are the same, as shown in Equation 7.8

$$\begin{aligned} \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}}|_{\mathrm{dB}} &= 10\log\frac{\frac{v_{\mathrm{out}}^2}{R_{\mathrm{out}}}}{\frac{v_{\mathrm{in}}^2}{R_{\mathrm{in}}}} \\ &= 20\log\frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} + 10\log\frac{R_{\mathrm{in}}}{R_{\mathrm{out}}} \end{aligned} \tag{7.8}$$

- NF: Noise figure is maybe the most important performance indicator of an LNA, because a low noise figure is what an LNA is made for. It has to provide some gain in order to relax the noise requirements of the following stages. Most of the noise generated in an LNA is typically contributed by the input transistor. As shown above, this parameter can be exchanged for current consumption.

- IIP3: The linearity of an LNA is of high importance in applications and frequency bands, where strong interfering signals are present. The IIP3 of a MOSFET is proportional to $\frac{I_{DS}}{g_m}$ [67]. So there is again a linear relation to power consumption.

- f: The frequency of operation is also linearly related to power consumption. The required gain-bandwidth product for an amplifier can be translated into a required gm, and the gm in turn depends on the current through a transistor [95].

In [67], a FOM is defined which includes all the parameters given above:

$$FoM = \frac{G \cdot IIP3 \cdot f}{P_{\mathrm{DC}} \cdot (F-1)} \tag{7.9}$$

The gain included in Equation 7.9 refers to voltage gain with open output which is not stated in [67] but clear from the text and drawings. Additionally, the parameters included in the FoM have been related to technology dependent device parameters in order to predict the performance of future technologies. The fact that this approximation can be made indicates that a FoM will always stay within certain boundaries where the technology limits the performance.

In later literature different variations of this FoM can be found. In [69], two FoMs are defined as:

$$FoM_1 = 10\log\frac{f\ [\text{GHz}]\cdot G\ [\text{lin}]}{P_{\text{DC}}\ [\text{mW}]\cdot(F\ [\text{lin}]-1)} \tag{7.10}$$

$$FoM_2 = 10\log\frac{f\ [\text{GHz}]\cdot G\ [\text{lin}]\cdot IIP3\ [\text{mW}]}{P_{\text{DC}}\ [\text{mW}]\cdot(F\ [\text{lin}]-1)} \tag{7.11}$$

whereas in [68], basically the same FoMs are used, but they are calculated taking a log20 instead of log10.

The biggest problem when tables of FoMs are presented is, that it is unclear in many cases whether the term G [lin] refers to $10^{\frac{G|_{\text{P,dB}}}{10}}$ or $10^{\frac{G|_{\text{V,dB}}}{20}}$.

Another FoM is introduced in [48] which is calculated as

$$FoM_3 = 10\log\left(100\cdot\left(\frac{G\ [\text{lin}]\cdot f^2\ [\text{GHz}]}{(F\ [\text{lin}]-1)\cdot P_{\text{DC}}\ [\text{mW}]}\right)\left(\frac{OIP3\ [\text{mW}]}{P_{\text{DC}}\ [\text{mW}]}\right)\right) \tag{7.12}$$

In this FoM, the NF and the nonlinearity are not as heavily weighted as the other parameters, because all parameters are squared except for those two. By taking $OIP3 = G\cdot IIP3$, one can see that also the gain is squared which is not immediately obvious from Equation 7.12.

7.5.1. Comparison and Interpretation of the Results

Table 7.3 lists a number of reported LNAs and their calculated FoMs. The LNA presented in this work is one of those with lowest power consumptions. The biggest weakness is obviously its nonlinearity. That is why the value of FOM_2 is extremely low. However, regarding the application and the architecture of the complete receiver frontend, nonlinearity is not that important. Basically, nonlinearities in a receiver frontend are troublesome for two reasons:

- The first reason is clipping. Higher modulation schemes rely on phase and amplitude information. That is why a clipping signal results in the loss of information. This is not the case in the presented receiver. Here only FSK is used and the received signal is clipped in the limiter at the end of the receiver chain anyway.

- The second and more important reason is the rejection of neighboring interferers. Strong neighboring signals may drive the LNA into saturation and block the desired signal. Another very important effect is that due to third order nonlinearities, two neighboring signals can produce intermodulation products which lie directly on top of the desired signal. In fact this is exactly what the IIP3 describes. A very detailed description of the effects of nonlinearity is given in [99]. In the presented LNA, the situation is relaxed because the filtering behavior of the BAWs with their narrow bandwidth rejects most of the interfering signals before they can block or disturb the desired channel. That is why FOM_2 including the nonlinearity is less relevant for this design. In the presented simulation of the IIP3, the two input frequencies

Ref	Author	f [GHz]	Gain [dB]	NF [dB]	IIP3 [dBm]	P1dB [dBm]	P_{DC} [mW]	Tech. [µm]	Year	FOM1	FOM2
[3]	This work	2.4	18.5	4.8	-24	-33.5	4	0.13	2009	13.2	-10
[33]	Borrem.	3.4	16.8	2.2	-11.5		7.3	0.13	2007	15.3	3.8
[54]	Li	5.8	9.4	2.5	7.6		3.42	0.18	2005	12.8	20.4
[53]	Walling	5.4	20	3	-22		2.7	0.18	2007	23	1
[52]	Linten	5.5	13.3	2.9	-3	-11.5	9.7	0.09	2005	11.1	8
[51]	Linten	5.5	11.2	3.2	-8.6	-17.5	2.1	0.09	2004	15	6.4
[50]	Fan	2.2	8.4	1.92	-2.55		16.2	0.35	2008	2.3	-0.3
[48]	Chandr.	2.4	12.1	2.77	2.4		4.5	0.15	2002	9.9	12.3
[49]	Han	5.2	16.5	1.11	-11.5	-19.9	12.4	0.18	2005	18.1	6.6
[47]	Hsiao	2.4	15	3.2	-1.1	-13	9.8	0.18	2003	8.5	7.4
[45]	Point	2.4	14.7	2.88	-0.5		?[1]	0.25	2002	-	-
[44]	Leroux	1.23	20	0.8	-11		9	0.25	2002	18.3	7.3
[43]	Liu	2.4	21.6	1.7	-9.5[2]	-19.1	6	0.18	2008	20.8	11.3
[46]	Huang	2.4	19.9	2.5	2	-12	14.7	0.35	2001	13.1	15.1
[35]	Aspemyr	5.8	12.5	1.7	4		16.8	0.09	2006	11.1	15.1
[34]	Ho	2.4	13	5	-9	-18	2.8	0.09	2006	9	0
[69]	Joo	2.4	28.3	2.0	-22.4	-35	4.8	0.13	2009	27.6	5.2

[1] I_{DC} = 11.4 mA, VDD not given
[2] Not given, assuming P1dB + 9.6 dB

Table 7.3.: Comparison with reported LNAs

have been chosen with an offset of only 400 kHz such that both tones lie within the bandwidth of the filtering BAWs and the result is not falsified.

As shown in Figures 7.16 and 7.17 where FOM_1 is plotted against $IIP3$ and P_{DC}, the performance of the LNA in terms of FOM_1 is in the mid range of reported designs. Considering the constraints which have been imposed on the design of this LNA, this value is not bad:

- As the sensor node might be operated by using a very weak energy source like for example an energy harvester, a fully differential circuit topology is used for the complete receiver frontend in order to provide a better power supply rejection. Most of the other reported LNAs are single ended however and in order to achieve the same noise performance as a single ended solution a differential circuit requires more current [35].
- The matching network including also the RX/TX switch is completely implemented on-chip. In the applied process, the inductors have rather low quality factors which results in a NF of 4.2 dB already at the output of the matching network. With off-chip passive components this number could be significantly better. On the other hand, this process has been chosen, because it is qualified for automotive applications.
- The presented LNA provides a very narrow bandwidth at a high center frequency. If other reported implementations had to provide this bandwidth with external filters,

their insertion loss would certainly affect the FoM.

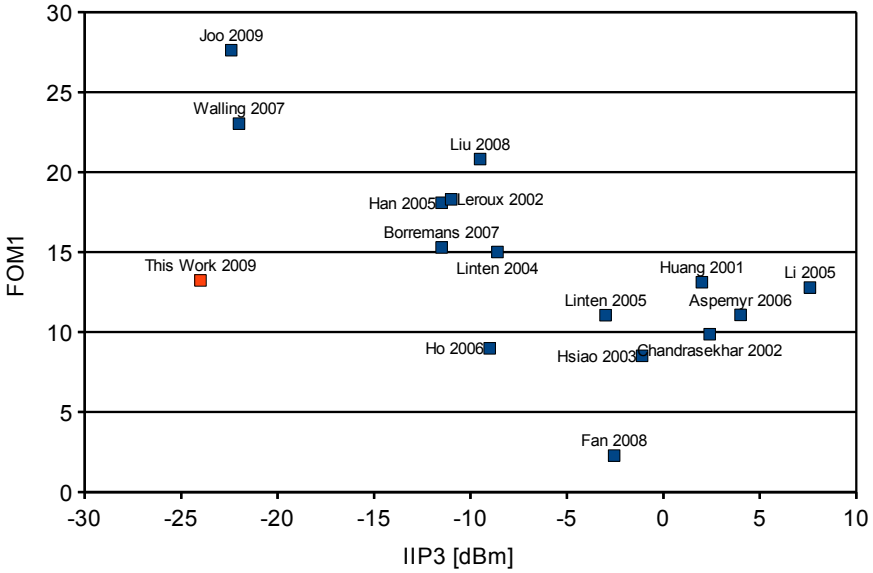


Figure 7.16.: LNA FOM1 plotted versus IIP3

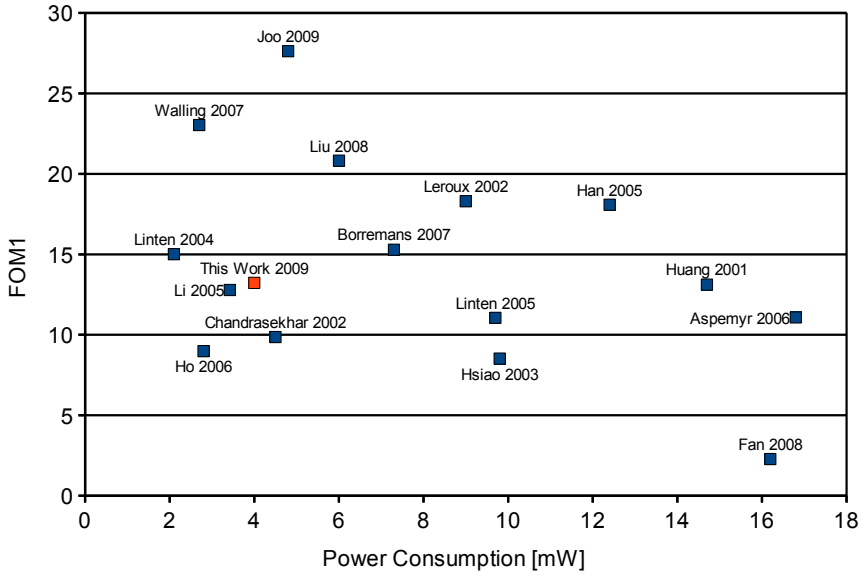


Figure 7.17.: LNA FOM1 plotted versus power consumption

Parameter	Value
Technology	0.13 µm CMOS
Frequency	2.4 [GHz]
Power Consumption	4 [mW]
Power Gain	18.5 [dB]
Voltage Gain (open)	33.7 [dB]
Voltage Gain (matched)	27.6 [dB]
Noise Figure (matched)	4.8 [dB]
IIP3 (matched)	-24 [dBm]
P1dB (matched)	-33.5 [dBm]
Image Rejection (max)	24 [dB]

Table 7.4.: Summary of LNA results

7.6. Comparison with a Similar Reported Topology

Another LNA, reported in [103] uses a similar approach of wire-bonding BAW resonators into the circuit. This LNA however applies the BAWs in front of the input transistors to use them for input matching and it does not aim at achieving a narrow bandwidth. That is why a lattice filter topology is used. The reported matching still requires an external balun for single ended to differential conversion and it only matches the receiver, so there is no RX/TX switch included. Reported measurement results are difficult to compare with the LNA in this work, because no values are given for the LNA alone, only the signal after downconversion to an IF of 100 MHz is given without including the power consumption of all circuit components. So although a comparison in performance cannot be made, the reference is given at this point, because the design approach is very similar to the one presented in this work.

7.7. Conclusion

In this chapter, a novel LNA architecture is presented which integrates BAW resonators into the circuit to provide a very narrow bandwidth, which is tunable over a frequency range of 11 MHz. The narrow bandwidth of the parallel resonance in combination with the close spacing of the series resonance relaxes the linearity requirements and enables a high image rejection in the LNA. All subunits of the circuit are examined in detail and simulation results are presented. The power consumption is among the lowest reported ones and the performance is remarkable, considering that no off-chip passive components are used (except for the BAW resonators of course). A thorough investigation for a meaningful FoM is made, and the chosen FoM is compared to other reported designs. Table 7.4 summarizes the relevant performance parameters of the LNA.

8. Polyphase Networks (PPF)

This chapter explains the use of polyphase networks, also called polyphase filters (PPF). The contents of this chapter have partly been published in [2].

8.1. Polyphase Networks

Polyphase networks are required in many receiver architectures. Basically they are used for two purposes: For generating quadrature phases of any signal and for image rejection. A single-stage polyphase network generates a 90° phase shift at the output for any input frequency, but only for a certain input frequency, the amplitudes of the I- and Q- signal at the output are equal. Only if the amplitudes are equal the image can be cancelled. In order to provide matching I- and Q- phases for a larger bandwidth, a polyphase network consisting of several stages with different cut-off frequencies can be used. The RC-time constants have to be chosen such that their geometric mean is the desired center frequency [88]. The drawback is that each stage attenuates the desired signal. Figure 8.1 shows two-stage polyphase networks in two different configurations as they are used in the presented receiver frontend (with different RC products). With the inputs $Q_{in}+$ and $Q_{in}-$ connected to AC-ground (a), it can be used to generate quadrature phases from the differential input signal $I_{in}+$ - $I_{in}-$ around 2.45 GHz. And with the outputs connected (b), it is used to cancel the image at 10.7 MHz.

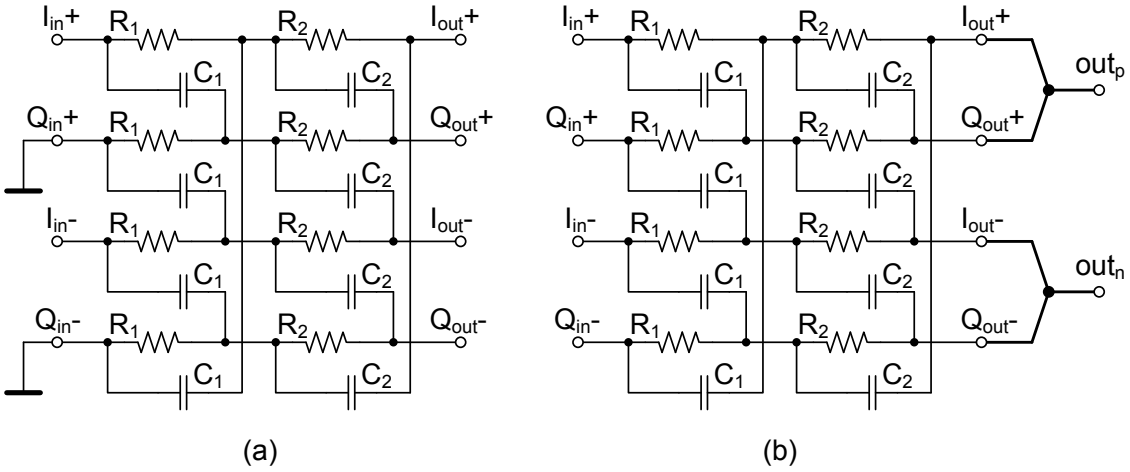


Figure 8.1.: Polyphase Network Configurations

Parameter	Value
R_1	480 Ω
C_1	150 fF
f_1	2.21 GHz
R_2	1,900 Ω
C_2	30 fF
f_2	2.79 GHz
f_c	2.48 GHz

Table 8.1.: Component values of the 2.45 GHz PPF as shown in Figure 8.1a

8.2. Dimensioning of a Polyphase Network

In order to cover a certain bandwidth, it is required to use a multi-stage polyphase network, but also to cover process variations which arise between different lots [72] a certain excess margin in the bandwidth has to be considered. As a rule of thumb it can be assumed that each stage provides a reasonably constant gain (within about 0.2 dB) over a 10% bandwidth. So a two stage network will be sufficient to cover a bandwidth of about ±20% [88]. The attenuation in every stage depends on its load. If a stage is followed by an identical stage, then the signal is attenuated by 3 dB. Generally speaking, the lower the load impedance, the higher the loss. That is why another rule of thumb is to progressively increase the impedance from stage to stage. The value of the resistors is increased steadily and the pole frequencies are tuned with the capacitor values. The input impedance of a polyphase filter strongly depends on the input frequency. If the polyphase network is not resistively loaded but capacitively as for example with a differential amplifier or an active mixer, then the input impedance at DC is infinite. At the pole frequency of the first stage, it falls down to $R||(1/\mathrm{j}\omega C)$ and at even higher frequencies it consists of the load capacitance to ground in series with the filter capacitors [72].

The polyphase network in the eCubes receiver frontend, generating the quadrature phases at 2.45 GHz has been designed using the rules of thumb given above. The poles of the two stages have been placed about 10% above and below the desired frequency with the geometric mean at about 2.45 GHz. For the versions assembled with 2.1 GHz resonators a resulting I- Q- imbalance has been taken into account, so the image rejection of those samples is lower. The component values of the 2.45 GHz PPF as shown in Figure 8.1a is given in Table 8.1.

Figure 8.2 shows a Monte Carlo simulation of the amplitude error covering process and mismatch in 1000 runs. The mean error is not centered around zero as there is a systematic error introduced by the placing of the two corner frequencies.

8.3. Conclusion

In this chapter a short overview of polyphase networks and their applications is given. Some general rules for the dimensioning are explained and the design of the 2.45 GHz PPF is given in detail. Monte Carlo simulations show that the amplitude error stays within about ±0.2 dB, although a systematic offset is introduced.

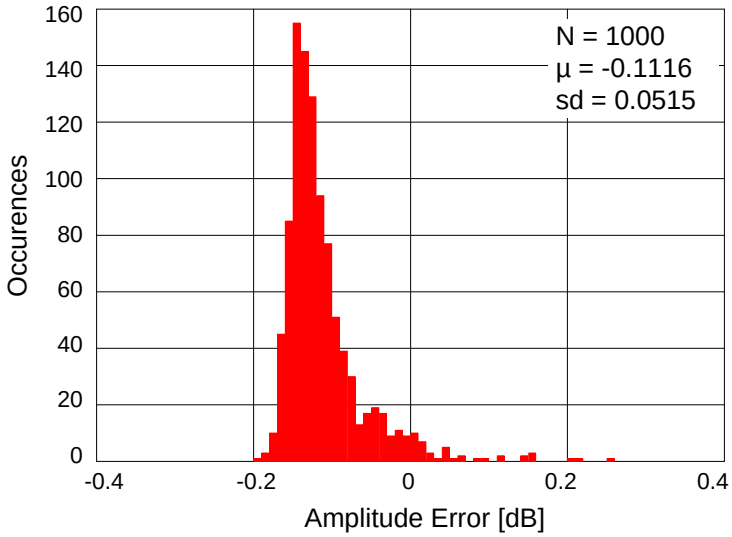


Figure 8.2.: Amplitude Error

9. Mixer and IF path

This chapter describes the mixer and IF path of the eCubes receiver. The IF path of the presented receiver has been reused from an existing receiver for sub-GHz ISM bands [66]. The mixer has been slightly modified to support the higher input frequencies. The individual circuits of the IF path are not part of this work, only their selection and integration into the frontend of the e-Cubes transceiver. That is why only a short overview is given and simulation results together with the RF-parts are provided in order to compare them with measured values in Chapter 10.

9.1. Mixer

The employed mixers are active Gilbert type mixers. A very generic schematic of a Gilbert mixer is shown in Figure 9.1.

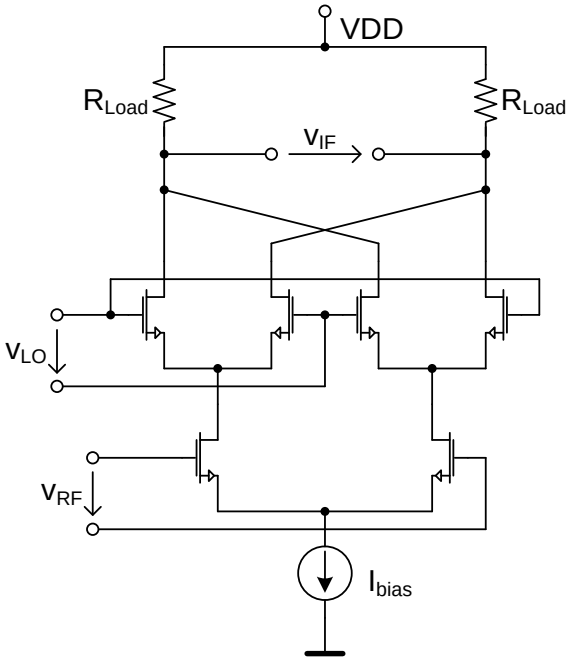


Figure 9.1.: Gilbert mixer

The basic working principle of such a mixer is that it converts the RF voltage to a current in the lower stage which is then multiplied with the LO signal in the current domain. The

advantage of an active mixer compared to a passive one is that it is able to provide gain. Passive mixers on the other hand show better linearity.

9.2. IF Path

Figure 9.2 shows the IF path of the receiver from the mixers to the digital section of the receiver. The mixers are followed by the second PPF operating at the IF frequency of 10.7 MHz where the image is rejected. The signal is then fed into an output buffer with an output impedance of 330 Ω to match the off-chip IF filter. After filtering, the signal is fed to the limiter. There it is converted to a rectangular signal by means of amplification and clipping. This rectangular signal is then fed into the digital section where it is sampled and again downconverted by digitally multiplying it with a numerically controlled oscillator (NCO) signal. After some additional digital filtering it is demodulated (see Figure 3.1). Besides the rectangular signal, the limiter provides an RSSI which can be converted to a digital 10 bit value on-chip or fed to an output pin as an analog voltage. The RSSI is a signal that is proportional to the logarithm of the input signal level [74].

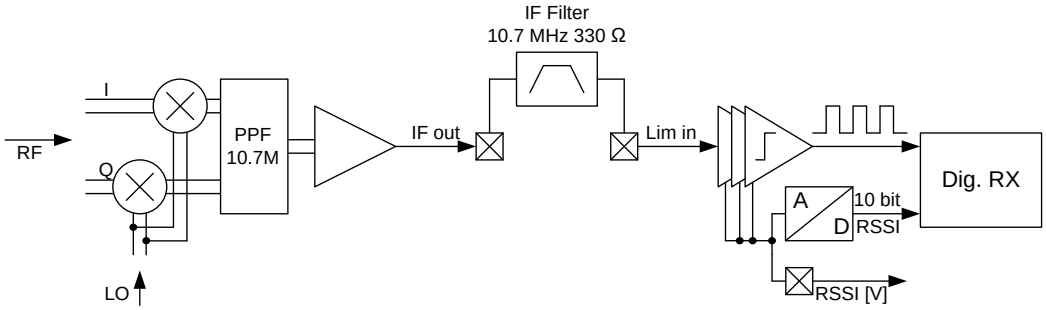


Figure 9.2.: IF path

Figure 9.3 shows the simulated power gain and noise figure of the complete eCubes receiver, from the RF input to the IF output which goes into the IF filter. The simulation results are gained from post-layout extracted circuits. The output impedance of the IF path at 10.7 MHz is 330 Ω. In simulation, as well as in the measurements in Chapter 10, the output is matched to 50 Ω by means of a passive LC circuit.

The simulated power gain is 26.6 dB at a NF of 13.41 dB. The total image rejection, including the effect of the image reject architecture and the BAWs in the LNA is 54.9 dB.

9.3. Conclusion

In this chapter, a brief overview of the IF-path in the presented receiver is given. The basic architecture of an active Gilbert type mixer is explained and simulation results including the complete receiver from the RF input down to the IF output are given.

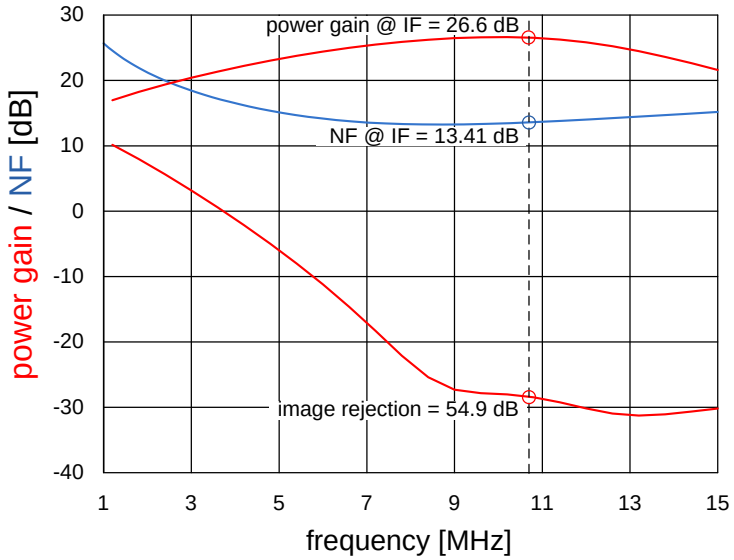


Figure 9.3.: Simulated power gain and noise figure of complete receiver frontend

10. Measurements

This chapter presents some simulation and measurement results of the receiver frontend. Before explaining the measurement results, some simulations are shown which point out the challenges of the measurements. Figure 10.1 shows several different simulated frontend gains. Different nonidealities which affect the frontend gain or image rejection are considered.

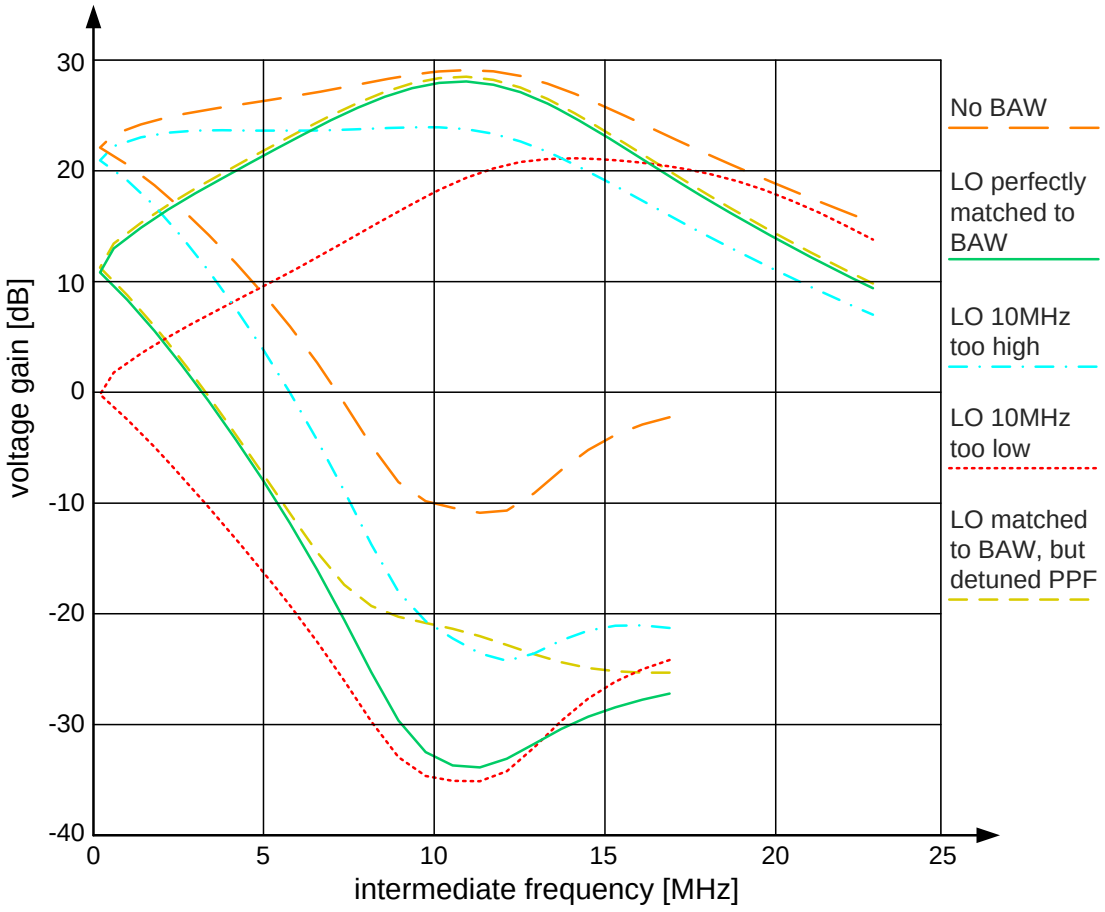


Figure 10.1.: Effect of different mismatches on RX gain

The simulation shows the downconverted signal together with its image frequency. As the intermediate frequency approaches zero, the left half of the signal is mirrored around, and only positive frequencies are available. So for every output frequency, two signal values are shown. One is the desired signal, the other one represents the image.

The orange line shows a simulation when no BAW is inserted into the LNA. This behavior can only be shown in simulation, because the capacitive tuning network and the pad structures including ESD protection circuits are integrated on chip. Simply cutting the bond-wires is not sufficient because in this case the large capacitance of the tuning network and pad structures remains in the LNA. The simulated image rejection is about 40 dB. When BAW filters are inserted into the LNA, and the simulated LO is perfectly placed 10.7 MHz below the BAWs resonant frequency, then the insertion loss of the BAW filters is only in the range of 1-2 dB but an additional image rejection of about 22 dB can be simulated. Unfortunately the LO and the BAW filters do not always match so perfectly, as explained in the next section. The blue line shows what happens to the downconverted signal when the LO frequency is 10 MHz higher than desired (or the resonant frequency of the BAW filters is 10 MHz lower than desired). The resulting downconverted signal shows a significantly lower gain, and the image is not suppressed by the same amount as before. When the LO is 10 MHz too low, the gain is deteriorated even more, but at least the image is rejected. The last effect which is shown in the plot is what happens when the poles of the polyphase filter generating the quadrature phases are shifted. One can see, that this has almost no impact on the desired signal, as explained in Chapter 4, but the image is no longer rejected by the same amount.

10.1. Matching of LO and Filtering BAWs

The first problem arises when assembling the demonstrator PCB. Each PCB carries three BAW dies, each containing eight resonators. A picture showing the transceiver together with the BAW dies is shown in Figure 10.2

Above the transceiver, a BAW die is bonded carrying the resonator for the TX oscillator. In the upper left corner, one can see the BAW die which contains the resonator for generating the LO signal. Its resonance frequency should be exactly 10.7 MHz below the TX BAW. From the third BAW die, two resonators are wire-bonded to the LNA. Their resonance frequency should be the same as that of the TX-BAW. Only with this distribution a transmitted signal, generated by a TX BAW can be passed through the filtering BAWs and downconverted to the correct IF. Unfortunately, the resonators on the available 2.4 GHz BAW wafers show a wide spread of resonance frequencies and the situation is even worse when taking resonators from different wafers. Figure 10.3 shows the distribution of the resonant frequency on four different 2.4 GHz BAW wafers. One can see that only a few transmitter - receiver combinations are possible and the respective resonators have to be picked by hand. This wide spread of frequencies is due to the fact that the 2.4 GHz wafers are only test-wafers. The 2.1 GHz resonators on the other hand have been taken from productive filter-wafers, which have been trimmed to the correct frequency. The deviation from the desired frequency is much smaller for those resonators. In fact, it is too small, such that it is not possible to achieve the desired IF of 10.7 MHz. Also shown in Figure 10.2 is the location of the LNA on the transceiver ASIC. The chosen location is a compromise between being located close to the antenna pad on the one hand and close to the filter BAW pads on the other hand. Placing the antenna pad closer to the filter BAW pads is not possible because the matching network also requires some space and the TX oscillator with the power amplifier also has to be taken into account. The two inductors

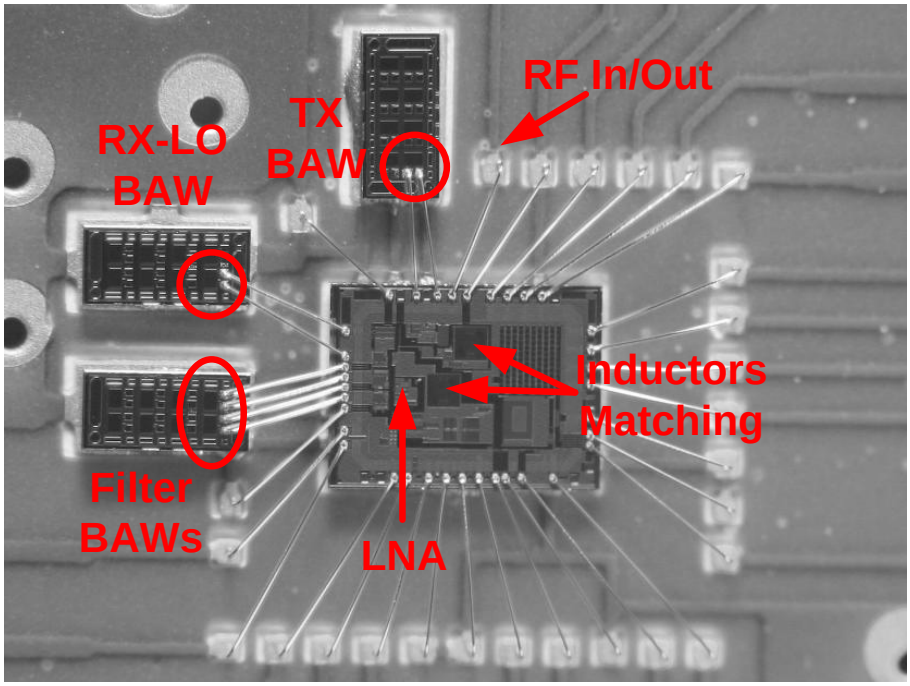


Figure 10.2.: Chip photo of transceiver and BAW dies

from the matching network which account for a significant part of the silicon area can be seen very easily.

10.2. Measurement Setup

Figure 10.4 shows the measurement setup. A signal generator is connected directly to the input of the transceiver. This can be done, because the impedance of the signal generator is 50 Ω, which is also the input impedance of the receiver, provided by the on-chip matching network.

Measurements are quite complicated because there are only very few outputs. The RF signals at the output of the LNA or the polyphase network are not fed to output pins in order to avoid parasitic capacitances introduced by additional pins in the RF-path. The only signal which can be measured is the downconverted signal at the IF. The applied off-chip ceramic filters have an input and output impedance of 330 Ω. That is why this is also the output impedance of the output buffer. In order to connect the transceiver to measurement equipment like a spectrum analyzer, another matching network is required to match the 330 Ω output to the 50 Ω input of the lab equipment. A very convenient way to measure the output signal is to use the on-chip limiter. On the one hand, one can see the binary output signal by using a simple oscilloscope. On the other hand one can measure the RSSI as an analog voltage at a test-pin, or use the on-chip ADC to output the RSSI as a digital 10 bit value.

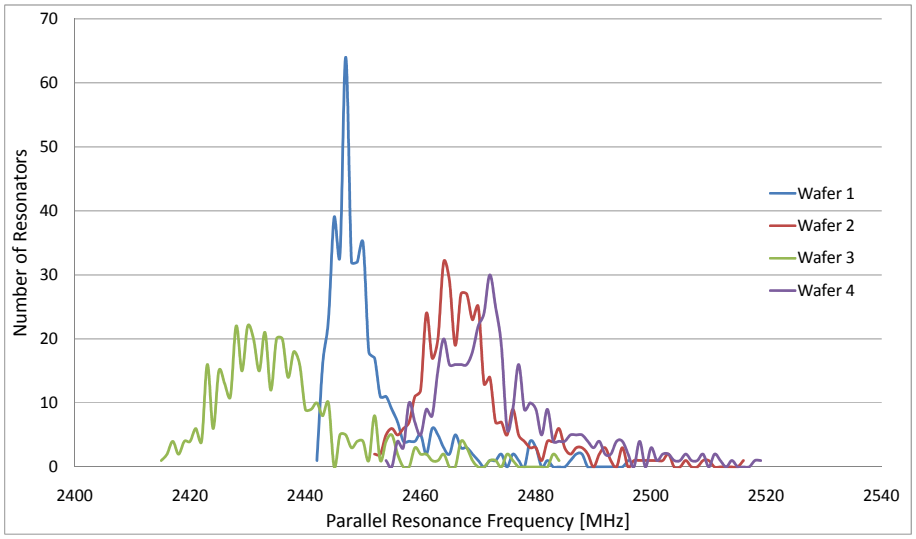


Figure 10.3.: Distribution of resonance frequency on four wafers

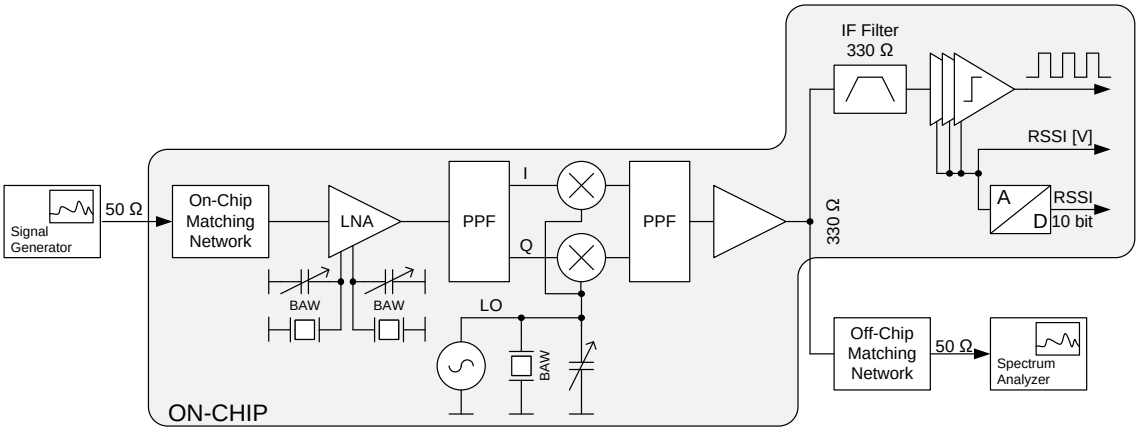


Figure 10.4.: Measurement Setup

10.3. Measurable Input Frequencies

As the LO signal is generated by an internal BAW based oscillator, the possible input frequencies which can be downconverted are limited to a very narrow band which is divided into two parts. Starting from an initial frequency, the LO can be shifted downward by about 15 MHz by means of the tuning capacitors. The receiver frontend can switch between high-side and low side injection of the LO signal, so the observable frequency range is twice the tuning range of the LO. Figure 10.5 shows the measurable frequencies. The hole in the observable band arises because the tuning range of the LO is smaller than twice the IF.

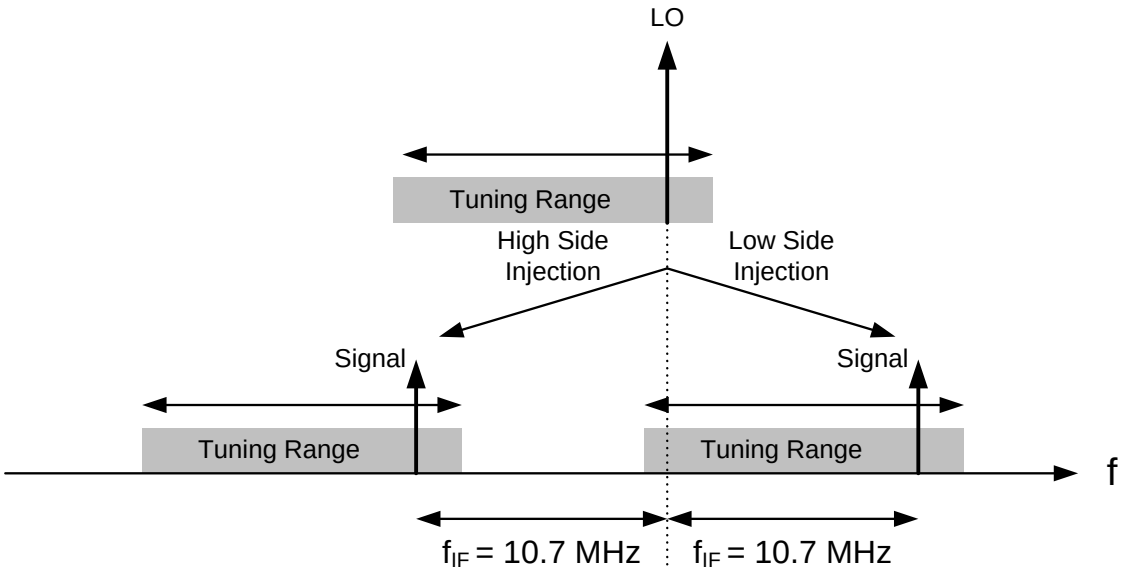


Figure 10.5.: Measurable Input Frequencies

10.4. Gain, Image Rejection and Noise Figure

As it is not possible to simply sweep the input frequency and plot the gain of the LNA, the measurement requires to sweep the codeword which tunes the LO frequency and set the input frequency accordingly in order to get a corresponding output value at the IF. First the LO tuning codeword is set to zero, resulting in the highest possible LO frequency, and the image reject architecture is set to receive the upper sideband. Then an input signal is fed into the receiver, which is 10.7 MHz above the LO frequency and the IF output is measured. In the next step the image reject architecture is set to receive the lower sideband. The input frequency is reduced by 21.4 MHz, which is twice the IF, and the output is measured again. This process is repeated for different tuning codewords of the LO and for different tuning codewords of the filtering BAW resonators in the LNA. As a result, the plots in Figure 10.6 are obtained. All values in the graphs have been measured at 10.7 MHz and plotted against the input frequency. On the y-axis, the graphs show the 10 bit RSSI value from the limiting amplifier. From the measured values, the filtering characteristic of the BAWs can be reconstructed. Figure 10.6 contains the measurement results for three different filter-tuning codewords, 0 (=min), 255, and 511 (=max). Besides the measured values, the figure also contains trendlines for all filter-tuning codewords. The plots in Figure 10.6 always contain two measurement values for the same LO frequency, one in the left half, and the other in the right half of the plots. In both groups, one can see that for the lower frequencies the measured RSSI values drop off from the trendline. As the same effect can be observed in both groups, it is assumed to be caused by the LO signal. When the oscillator is tuned with too many capacitors in parallel to the BAW the amplitude of the LO signal drops and the conversion gain of the mixer is reduced [3].

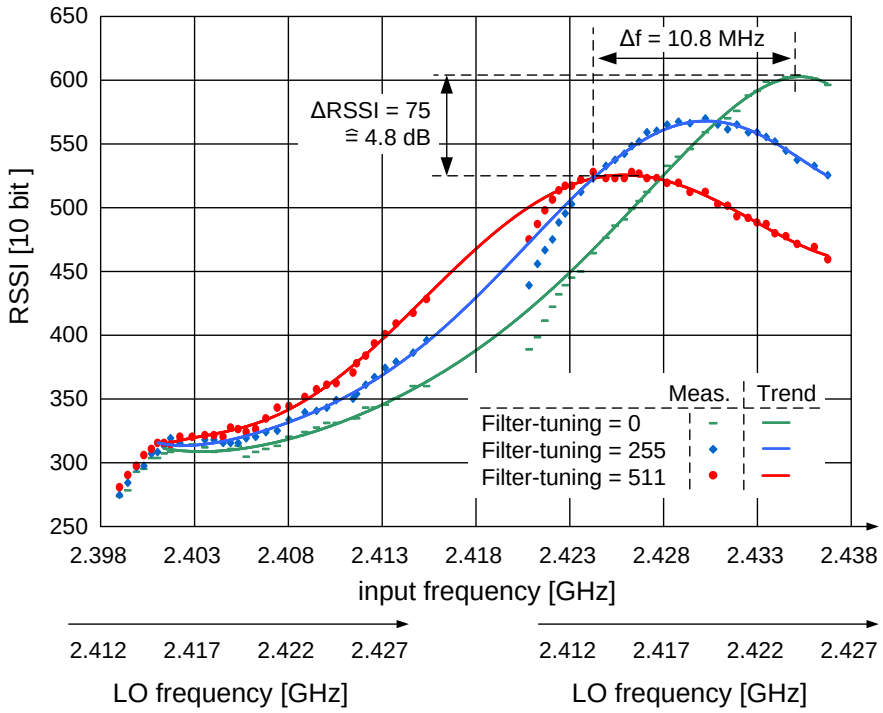


Figure 10.6.: Measured output RSSI for different filter tuning values

The measured power gain of the complete receiver frontend is shown in Figure 10.7. The maximum measured power gain is about 18 dB which is lower than expected from simulation. The gain is measured at the IF, but plotted against the input frequency. The frontend allows switching between high side injection which means that the LO should be located above the desired signal and low side injection with a LO lower than the desired signal. In the case of low side injection, the BAW resonators reject the image frequency, and with high side injection they reject the desired signal. By switching between these two modes, the total image rejection of the frontend can be split up into its two components, the first one caused by the BAW resonators and the second one, caused by the image reject architecture. The measurement shows that the image rejection caused by the BAW resonators is only 12 dB instead of 18 dB shown in the simulation. The reason for this degradation might be that the impedance of the applied resonators is lower than the values used in the BAW models for simulation, and that the parasitic capacitances are larger than anticipated. The image rejection caused by the image reject architecture is 29 dB at the frequency of interest [2]. The reason why there is no hole in the middle of the measurement plot as in Figure 10.6 is that the measurement values have not all been shifted to 10.7 MHz but also obtained at other IF frequencies. This means that not all of the measured frequencies could also be processed by the digital part of the receiver.

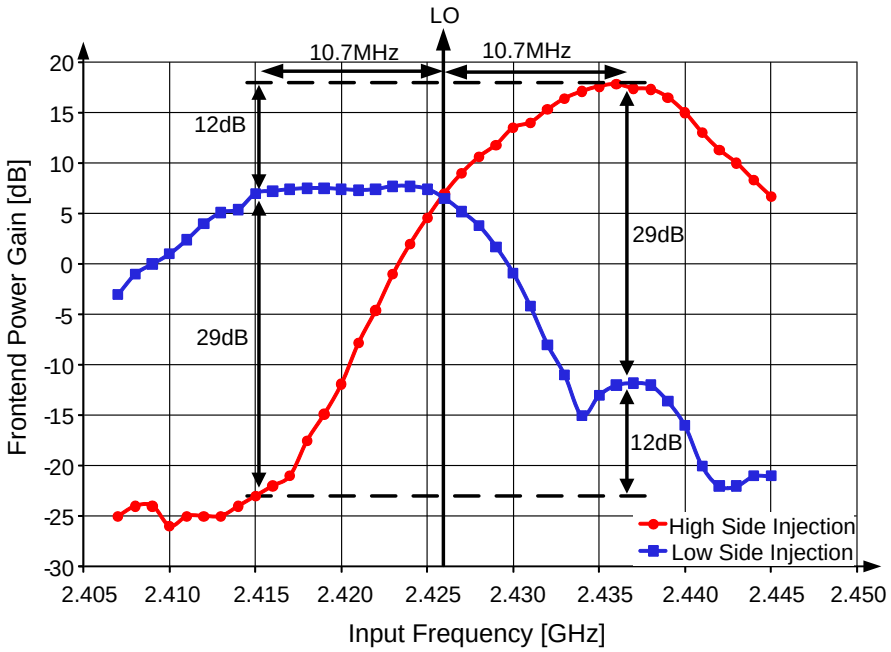


Figure 10.7.: Measured image rejection with high side and low side injection

Figure 10.8 once again shows the measured power gain together with the NF of the whole receiver frontend. As the gain is 7.5 dB lower than expected, the NF is degraded accordingly.

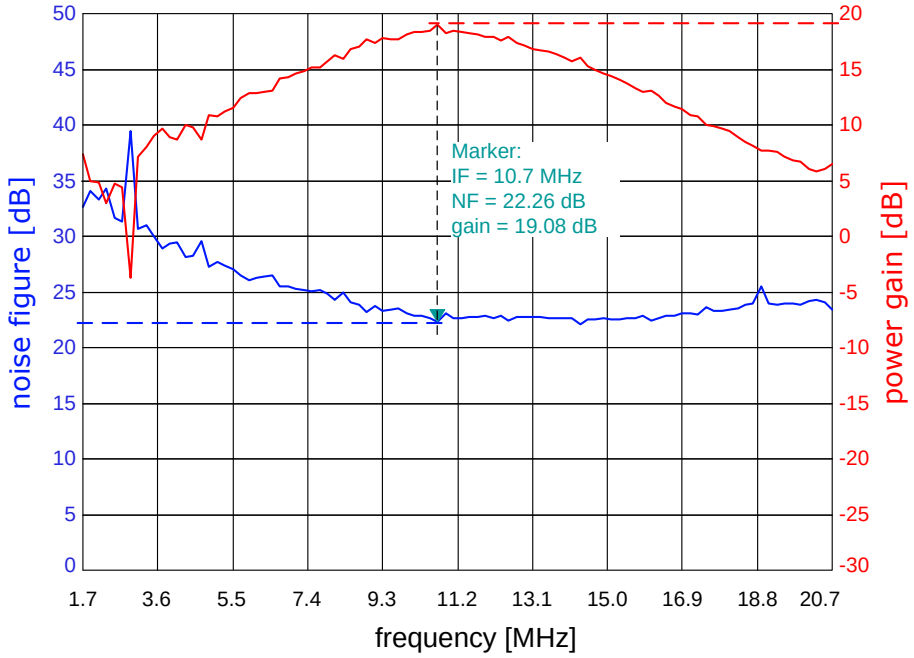


Figure 10.8.: Measured power gain and NF

10.5. Nonlinearity

Figures 10.9 and 10.10 show the 1 dB compression point (P1dB) and the input referred third order intermodulation product (IIP3) measured at the IF. The IIP3 has been measured with two tones at an offset of 400 kHz.

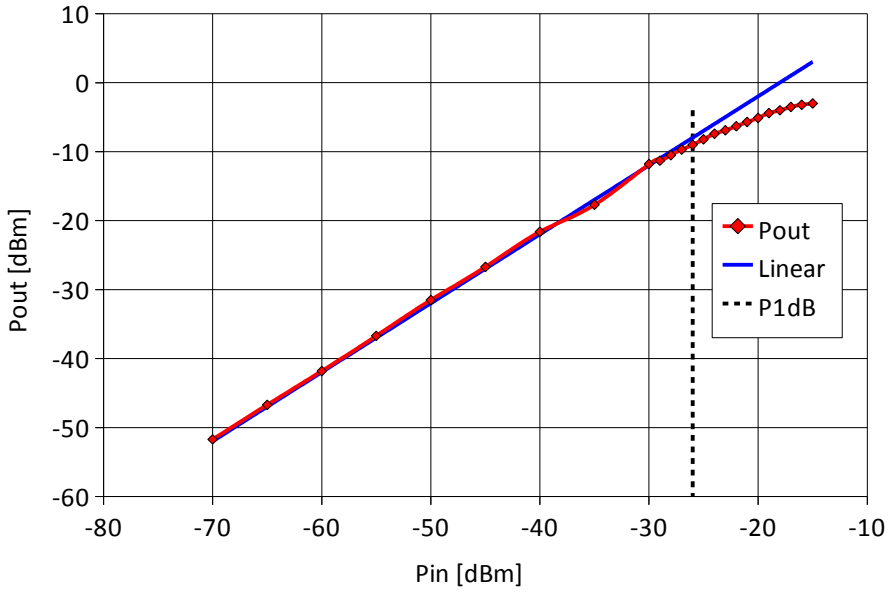


Figure 10.9.: Measured P1dB

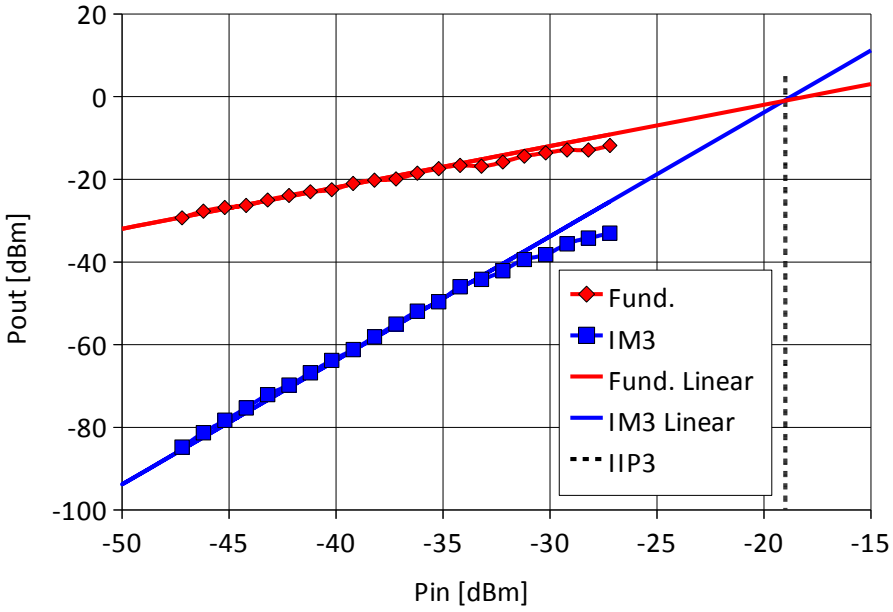


Figure 10.10.: Measured IIP3

The obtained P1dB is -26 dBm, and the IIP3 is -19 dBm.

10.6. Limiter Sensitivity

Figure 10.11 shows the RSSI of the limiter plotted versus the input power. One can see that down to about -100 dBm a signal can be detected by the limiter.

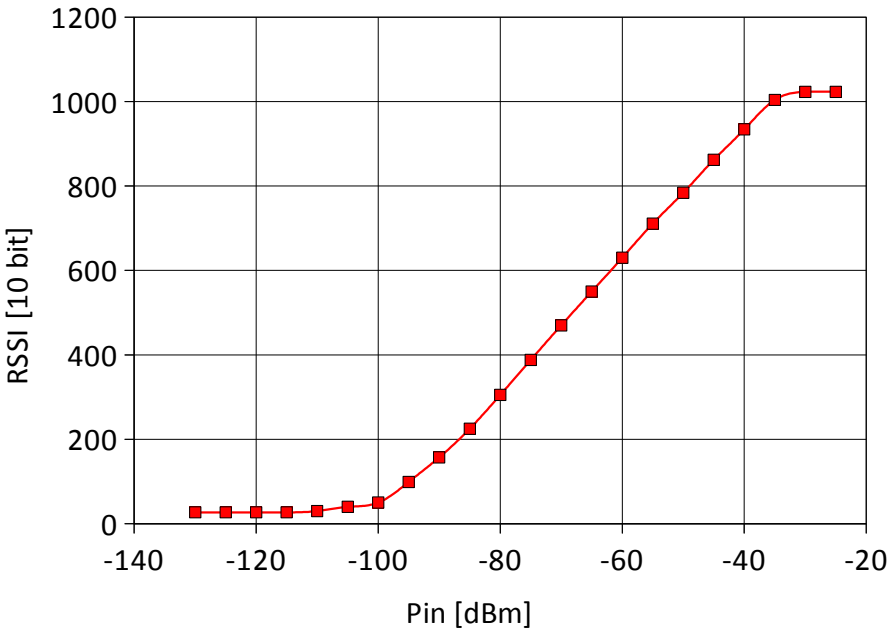


Figure 10.11.: Measured RSSI versus Pin

10.7. Bit Error Rate

Figure 10.12 shows the measured BER of the receiver including the limiter and the digital signal processing. One can see that a sensitivity around -90 dBm can be achieved. For higher input powers, the BER curve flattens instead of falling off with a steep slope. This behavior is caused by the clock and data recovery unit in the digital signal processing chain, which processes only a very short run-in sequence in order to cause as little communication overhead as possible. The measurement shows that the required BER as specified in Chapter 3 is almost achieved, although the measured gain is significantly lower than expected from simulations.

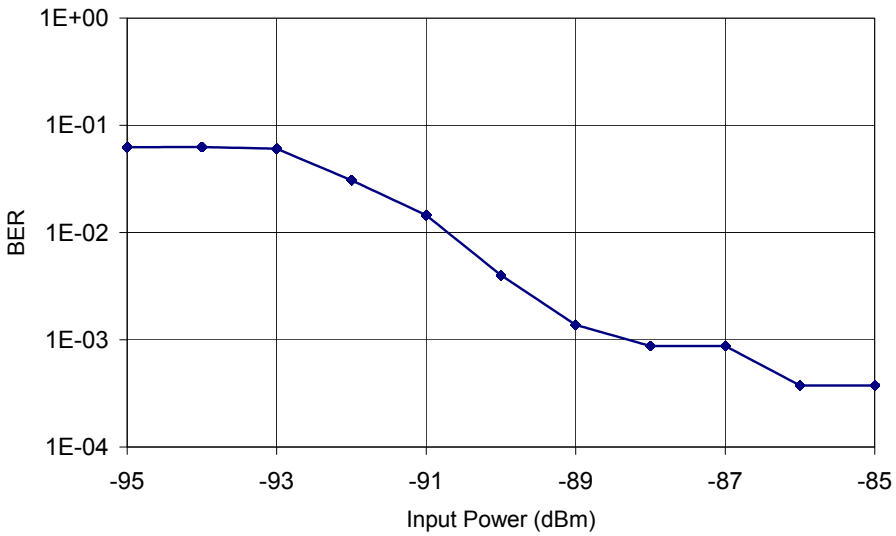


Figure 10.12.: Measured BER

10.8. Interpretation of the Results and Comparison with State of the Art

From the measurement results presented in this chapter, one can see that unfortunately the simulated performance of the receiver cannot be achieved on silicon. The power gain is 7.5 dB less than simulated and the NF is 8.6 dB worse than anticipated. As the NF degrades along with the gain, this indicates that the problem occurs in one of the very first stages. Most likely matching network and LNA both contribute to this degradation. A very likely cause for this degradation is that the losses in the matching network are higher than expected. If the first stage provides less gain, then the noise of the following stages contributes much more to the total NF as shown in Equation 7.1. Also the linearity has improved which indicates that the LNA is driven by a much weaker signal than in the simulation. The reduced image rejection of the BAWs indicates that their impedance is lower than expected. This suspicion is hardened by the drop-off in the tails of the RSSI-curves in Figure 10.6. It seems that the oscillator fails to maintain oscillation in these regions, which indicates that the impedance of the resonator might be too low. The degraded gain and NF of course affects the sensitivity of the receiver, which is nevertheless still close to the value of -92.8 dBm as specified in Chapter 3.

Table 10.1 shows a comparison with other reported receiver frontends. Only few of the reported designs include the LO and voltage regulators, that is why the power consumption of these implementations is significantly higher than some others. Regarding this work, it has to be mentioned that the power consumption seems quite high, because the overall supply voltage is 3 V. On chip, this voltage is regulated down to lower values with linear voltage regulators, which is very inefficient of course. In fact, only very few circuits really require the 3 V supply. The LNA for example draws 2 mA from a 2 V supply. So its power consumption is basically 4 mW but in this overall figure it accounts for 6 mW. The same is true for the oscillator which is supplied by 1.5 V. That is why the

Name	Ref.	IF [MHz]	f_c [GHz]	NF [dB]	G [dB]	IIP3 [dBm]	P_{DC} [mW]	I_{DC} [mA]	LO incl.	Techn. [µm]
This Work		10.7	2.4	22[1] 13.4[2]	19.1[1] 26.6[2]	-19	24	8	Yes	0.13
Hafez	[65]	0.0	2.4	8.5	60		7.2[3]	6	No	0.13
Kim	[64]	4.0	2.4	13.0		-4.5	9.0	5.0[4]	No	0.18
Kwon	[63]	480.0	2.4	6.5	32.0	-9.0	8.8	4.9[4]	No	0.18
Kwon	[62]	480.0	2.4	9.6	34.0	-29.0	8.0	6.7[4]	No	0.18
Seo	[61]	0.0	0.9	9.5	88.0	-10.0	25.0	14	Yes	0.18
Song	[60]	10.0	2.4	10.2	30.5		0.5[3]	0.5	No	0.18
Yoo	[59]	10.0	2.4	4.8	30.5	-18.0	11.3	4.5[4]	No	0.25
Kluge	[58]	2.0	2.4	5.7		-16.0	26.5[3]	14.7	Yes	0.18
Arasu	[57]	0.0	2.4	8.1	23.0	-15.0	4.8	2.7[4]	No	0.18
Chen	[56]	10.0	2.4	4.9	35.0	-10.0	93.0[3]	31	Yes	0.25
Jaervinen	[55]	0.0	2.4	28.0	47.0	-21.	3.4	2.75	No	0.13

[1] measured
[2] simulated
[3] calculated from VDD and I_{DC}
[4] calculated from VDD and P_{DC}

Table 10.1.: Comparison with reported receivers

current consumption is also included in the table, and it is the more relevant parameter for comparison.

Figure 10.13 shows a comparison of the presented receiver with the other fully integrated solutions containing also the LO from Table 10.1. The comparison includes NF, frequency, and current consumption. Gain is not included because once the signal is downconverted, gain can be achieved at the IF without considerably increasing the overall power consumption. One can see that the presented receiver is the one with the lowest current consumption of those including the LO which has been the main focus in the design. The simulated NF is at a reasonable value, while the measurement unfortunately shows a significant degradation as explained above.

10.9. Conclusion

This chapter provides all relevant measurement results for the transceiver. The measurement setup is explained in detail and the importance of proper selection and assembly of corresponding BAW resonators is highlighted. The measurements are compared to simulation and the deviations are explained. Finally, a comparison to other reported receiver frontends is provided. Table 10.2 summarizes the relevant performance parameters of the receiver.

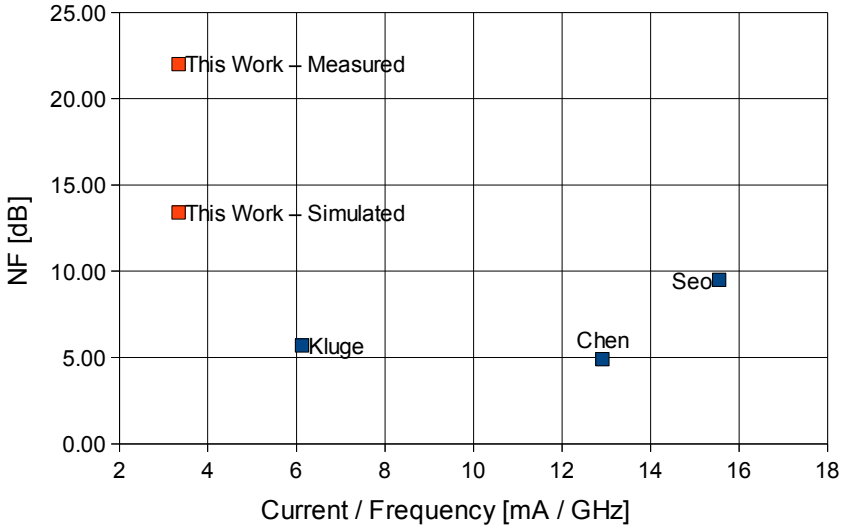


Figure 10.13.: Comparison of fully integrated solutions

Parameter	Value
Technology	0.13 µm CMOS
Frequency	2.4 [GHz]
Power Consumption	24 [mW]
Current Consumption	8 [mA]
Power Gain	19.1[1] [dB]
	26.6[2] [dB]
Noise Figure	22.26[1] [dB]
	13.41[2] [dB]
IIP3	-19 [dBm]
P1dB	-26 [dBm]
Image Rejection (max)	41[1] [dB]
	54.9[2] [dB]
Sensitivity (at BER 10^{-3}, 50 kbit)	-88 [dBm]

[1] measured
[2] simulated

Table 10.2.: Summary of receiver performance

11. Power Supply of the eCubes Sensor Node

This chapter covers the power supply unit of the sensor node. As shown in Chapter 2, the transceiver is not the only active component in a sensor node. There is also a µController which performs the required measurements by controlling the sensors and converting the measurement data to digital values. The µController is also in charge of scheduling and timing of events.

The power supply of the sensor node consists of two small batteries which can also be replaced by an energy harvesting device. As the total size of the sensor node is a major constraint, the power supply topic is very challenging. The total size of a sensor node is limited to 1 cm^3. The batteries alone which are used in conventional TPMS sensor nodes have a volume which is higher than that. Three parameters have to be considered when choosing a battery for a wireless sensor node:

- Supply voltage
- Maximum current which can be delivered
- Capacity

When designing a sensor node for automotive applications, a fourth parameter has to be considered, which is the temperature range. Typical batteries only work in a considerably smaller temperature range than from -40℃ to +125℃. In order to keep the size of the demonstrator as small as possible, batteries have been chosen which do not fulfill all requirements but still the demonstrator can be considered as a proof of concept. Batteries providing all required electrical characteristics as well as the small geometries are not available on the market today. Due to the constraints concerning the size, the power supply has been optimized for transmitting sensor nodes only. The power supply relies on the fact that the sensor nodes are switched off most of the time, and only from time to time they are activated to perform measurements and transmit data to a base station which is always on and powered by the car battery. This concept of duty cycling will be explained in detail in the following Chapter and it will be shown how it can be exploited also for the receiving sensor node.

The batteries which have been chosen are Silver Oxide coin cells of type SR416SW with a capacity of 8 mAh. As the output voltage of those batteries is only 1.55 V, two batteries connected in series are used to provide the required supply voltage. Also the required peak current cannot be delivered by the chosen batteries. In order to account for that, the batteries are buffered with large capacitors. Figure 11.1 shows a schematic of the battery based power supply.

In order to dimension the capacitors, the required charge for one measurement and transmission event has to be estimated. Figure 11.2 shows the measured current profile

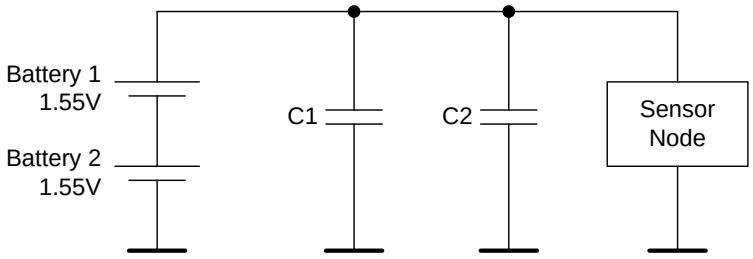


Figure 11.1.: Battery based power supply of the sensor nodes

for one event. It mainly consists of three sections. The first one is the measurement of pressure, acceleration and temperature. In the second section, the measured data are conditioned for transmission and the transceiver is configured, based on the measured temperature. The last section is the transmission itself which requires the highest current.

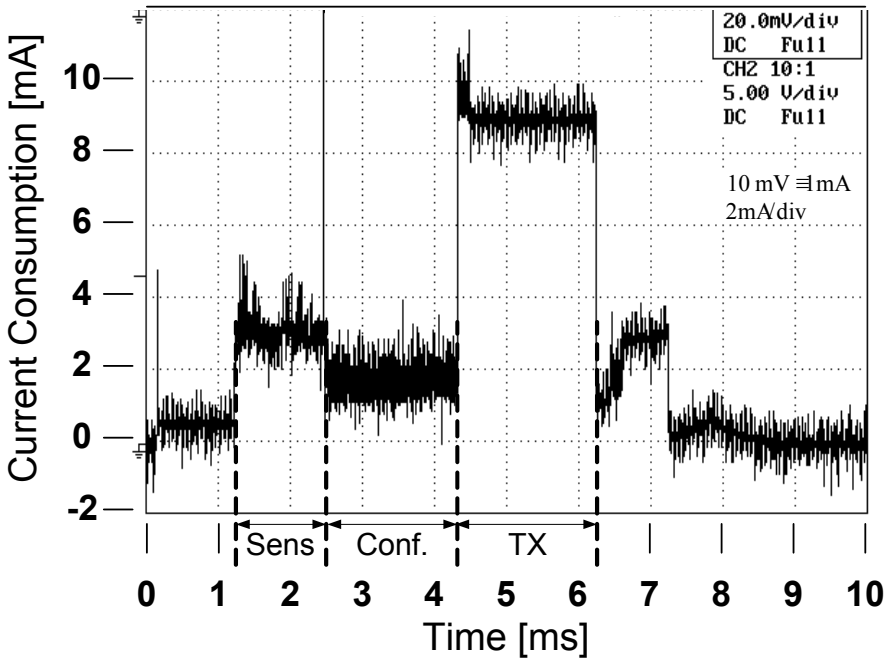


Figure 11.2.: Current profile for one event

For the dimensioning of the capacitors an average current consumption $i = 5\ \mathrm{mA}$ for the duration $t = 10\ \mathrm{ms}$ has been assumed, which is very pessimistic compared to the measured values in Figure 11.2. The required charge Q can be calculated as:

$$Q = \int_0^T i(t)\mathrm{d}t \approx i \cdot \Delta t = 5\,\mathrm{mA} \cdot 10\,\mathrm{ms} = 50\,\mu\mathrm{C} \tag{11.1}$$

To get the required size of the capacitors, the maximum allowed voltage drop has to be taken into account. The maximum voltage is 3.1 V because each of the two batteries provides 1.55 V when they are full. The minimum voltage for the system to operate is

2.9 V, so the voltage drop $\Delta V = 3.1 - 2.9 = 200\,\mathrm{mV}$ and

$$C = \frac{Q}{\Delta V} = \frac{50\,\mu\mathrm{C}}{200\,\mathrm{mV}} = 250\,\mu\mathrm{F} \tag{11.2}$$

As the estimations made for the calculation are worse than the measurements, the required capacitors would be a bit smaller, but the range is correct. In order to store the charge for at least two events, two capacitors with a size of 220 µF each are used. For the total current consumption also the standby current has to be taken into account. Assuming one event every 10 seconds, the estimated average active current is only 5 µA. The standby current is mainly caused by the µController where a real time clock is running and by the leakage current of the capacitors. The overall standby current is estimated to be around 3 µA, so it is in the same region as the active current.

11.1. Energy Harvesting

Another version of the eCubes power supply is based on energy harvesting. A MEMS based electrostatic energy harvester which converts vibrational energy into electrical energy has been developed at Vestfold University College [23]. At 50 km/h it should be able to deliver about 10 µW of power [22]. A PCB carrying the harvester is shown in Figure 11.3.

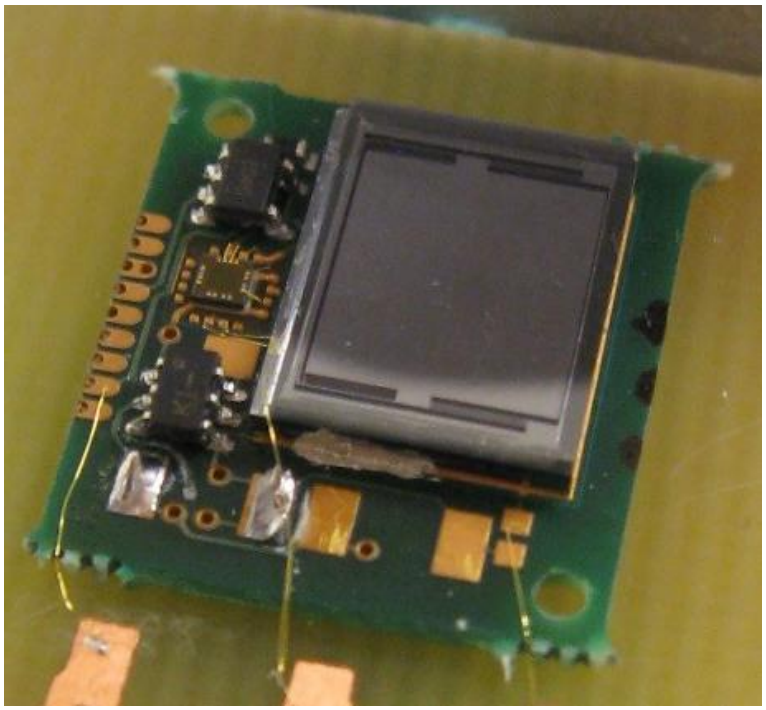


Figure 11.3.: Energy harvester PCB (Source: Vestfold)

The small PCB is carrying the energy harvester which is connected to a rectifier followed by an energy conversion ASIC which has been developed by TU Vienna [79]. The

harvested energy is then stored in buffer capacitors until enough charge is available to trigger an event at the sensor node. The energy harvester basically consists of a moving mass, which is mounted with springs above an electret. When the mass vibrates, an AC current is generated. As the mass is very small, is has to be sealed in an evacuated cavity in order to be able to move. Unfortunately, there has been a problem with the vacuum in the produced samples of the harvester. That is why measurements could only be performed in an evacuated chamber mounted on a shaker. These measurements have also been performed by Vestfold University College, and the results have been used to build up a test environment for the eCubes sensor nodes as shown in Figure 11.4. In this test environment, the harvester itself is replaced by an AC voltage source with a large resistor in series which limits the current delivered to the conversion ASIC. Instead of the AC source, also a DC voltage source with current limitation can be used to prove the feasibility of the energy harvesting power supply. The conversion ASIC stores the energy in a large buffer capacitor and when the voltage across this capacitor exceeds a certain limit, it activates the sensor node. When the measurement and transmission are completed, the sensor node signals the conversion ASIC to shut off the supply again, in oder to always keep a certain amount of charge in the buffer capacitor. The software running on the µController for this test setup is described in detail in [18].

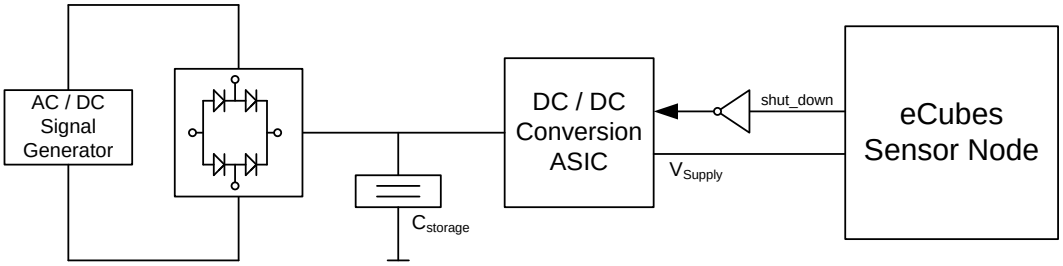


Figure 11.4.: Test setup for harvester based supply

11.2. Conclusion

In this chapter, the power supply of the sensor node is described. Measurements show that the average active current is below 5 mA and the peak current does not exceed 10 mA. The standby current is around 3 µA. By applying an appropriate duty cycle, which is fitting to an application where only the transmitter is used, the average active current is in the same range (5 µA). It is shown how two small sized coin cell batteries in combination with buffer capacitors can be used to supply the sensor node under these conditions. Finally a setup is described, where the sensor node is supplied by a vibrational MEMS based energy harvester.

12. Receivers in Multi Hop Sensor Networks

In this chapter, the power supply concept for transmitting sensor nodes is extended to fully equipped sensor nodes also containing receivers. The contents of this chapter have been published in [4]. The power saving is achieved by exploiting the short start-up time of the BAW based oscillator which can have a high impact on the overall power consumption in certain cases as shown in [111]. The effect of start-up time on transmitter power consumption in wireless sensor networks is examined in [27].

12.1. Wireless Sensor Networks

Power can be saved by switching the sensor nodes off when no data transmission or other activity is ongoing. This is no problem for sensor nodes which are only transmitting data and do not act as receivers. In this way, star topology networks can be built with a base station which is always on and listening into the channel if there is any incoming transmission from a remote sensor node. Such topologies can be used for example in vehicles where the base station can be powered by the car battery. The duty cycle d of the transmitting sensor nodes can be expressed as the active time t_{act} divided by the total time t_{tot}

$$d = \frac{t_{\mathrm{act}}}{t_{\mathrm{tot}}} = \frac{t_{\mathrm{act}}}{t_{\mathrm{act}} + t_{\mathrm{slp}}} \tag{12.1}$$

In this way, the power consumption can be reduced to any desired value just by making the sleep time t_{slp} long enough in relation to the active time t_{act}. The standby-current in sleep mode is the lower limit and whether the required t_{slp} is tolerable or not depends on the application of interest. By introducing a duty cycle in the transmitting nodes, it is only possible to build star-topology networks however. In order to build ad-hoc multi-hop networks it is necessary to reduce the power consumption of receiving sensor nodes as well, such that they can monitor the communication channel without draining the battery.

In [93] three types of rendez-vous schemes are presented:

- Purely synchronous. All nodes are synchronized in time and specific time slots are agreed for communication. The drawbacks of this scheme are that it is hard to accomplish in a fully ad-hoc network and that it causes a high communication overhead which may result in an increased power consumption.
- Purely asynchronous. In this rendez-vous scheme, each sensor node is equipped with a dedicated wake-up receiver. This wake-up receiver is designed for extremely low power consumption such that it can be always on and monitor the communication channel. The wake-up receiver cannot be used for the main communication

however. It supports only very low data rates and reported designs suffer from a rather low sensitivity compared to communication receivers. The sensitivity of wake-up receivers typically lies in a range from -50 dBm [91, 89] to -72 dBm [92] at a power consumption between 50 µW [92] and 65 µW [90]. The sensitivity can be increased by sending a longer preamble and thus achieve a certain coding gain, but these measures increase the power required by the transmitter to send the longer preamble. Another way of increasing the range of the wake-up signal is to increase the output power of the transmitter for a short wake-up pulse. Whether such an approach is feasible depends on the application and where more power is available, at the receiver or at the transmitter.

- Pseudo-asynchronous. Sensor nodes establish communication links on demand. [93] presents two different approaches, one where the communication is triggered by the transmitter, and another one, where the communication is triggered by the receiver. This rendez-vous scheme is based on duty-cycled transmitters as well as receivers. It is shown in [93] that this rendez-vous scheme can outperform the purely asynchronous approach.

The scheme presented in this chapter is a combination of the purely asynchronous and the pseudo-asynchronous approach. Like in the pseudo-asynchronous scheme, the receiver is operated in a duty-cycled mode of operation. Unlike the protocols in [93] however, where the receiver and transmitter negotiate a time for transmission the presented architecture does not rely on bidirectional communication for forwarding or receiving a data packet. Instead the main receiver is duty-cycled with a very high repetition rate such that it acts as a wake-up receiver. This is possible because the eCubes transceiver is based on BAW resonators instead of a crystal. Compared to conventional crystal based oscillators, the start-up time of a BAW based oscillator can be much shorter as shown in Figure 12.3.

12.1.1. Calculating the Duty Cycle

In order to reduce the average power consumption, a duty cycle d has to be introduced. The active time t_{act} consists of the start-up time t_{start} of the receiver and the actual reception time t_{rx}. The total time t_{tot} of one cycle consists of t_{start}, t_{rx}, and the sleep time t_{slp}.

$$d = \frac{t_{\mathrm{act}}}{t_{\mathrm{tot}}} = \frac{t_{\mathrm{start}} + t_{\mathrm{rx}}}{t_{\mathrm{start}} + t_{\mathrm{rx}} + t_{\mathrm{slp}}} \tag{12.2}$$

The average power consumption P_{avg} can be calculated as

$$P_{\mathrm{avg}} = \frac{P_{\mathrm{slp}} t_{\mathrm{slp}} + P_{\mathrm{start}} t_{\mathrm{start}} + P_{\mathrm{rx}} t_{\mathrm{rx}}}{t_{\mathrm{slp}} + t_{\mathrm{start}} + t_{\mathrm{rx}}} \tag{12.3}$$

If the average power P_{avg} is limited by the source, the duty cycle has to be chosen accordingly. Assuming that P_{slp}, P_{start}, and P_{rx} have been optimized as much as possible, there is only one remaining variable, which is the sleep time. The sleep time which is

required for a certain P_{avg} can be calculated as

$$t_{\mathrm{slp}} = t_{\mathrm{start}}\left(\frac{P_{\mathrm{start}} - P_{\mathrm{avg}}}{P_{\mathrm{avg}} - P_{\mathrm{slp}}}\right) + t_{\mathrm{rx}}\left(\frac{P_{\mathrm{rx}} - P_{\mathrm{avg}}}{P_{\mathrm{avg}} - P_{\mathrm{slp}}}\right). \tag{12.4}$$

The resulting duty cycle can be expressed as

$$d = \frac{(t_{\mathrm{start}} + t_{\mathrm{rx}}) \cdot (P_{\mathrm{avg}} - P_{\mathrm{slp}})}{t_{\mathrm{start}}(P_{\mathrm{start}} - P_{\mathrm{slp}}) + t_{\mathrm{rx}}(P_{\mathrm{rx}} - P_{\mathrm{slp}})}. \tag{12.5}$$

Once the required duty cycle is known, t_{act} has to be kept as short as possible in order to allow for a high repetition rate. Figure 12.1 presents two different modes of operation. Both of them have the same duty cycle of $d = 1/4$, but the repetition rate of the second one is much higher. In this way the power consumption of the transmitter can be reduced because the required preamble length t_{pre} which the transmitter has to send is exactly one period of the receivers duty cycle t_{tot}.

$$t_{\mathrm{pre}} = t_{\mathrm{slp}} + t_{\mathrm{act}} = t_{\mathrm{tot}} \tag{12.6}$$

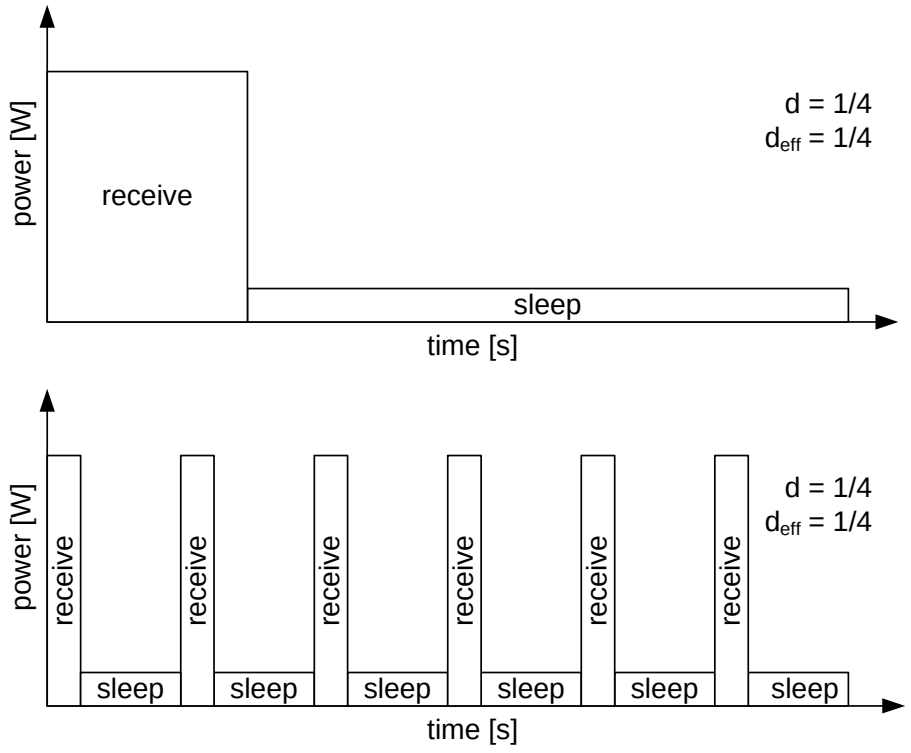


Figure 12.1.: Duty cycle with different repetition rates

As shown in Equation 12.4, the required sleep time depends on t_{start} and t_{rx}. While t_{rx} scales with the number of bytes to be received and the data rate, t_{start} is fixed and in order to achieve the highest possible repetition rate, it has to be ensured, that the first term is only a fraction of the second one. Otherwise the start-up time dominates the active time as shown in Figure 12.2. In this case, the duty cycle $d = 1/4$ as in Figure 12.1, but the

effective duty cycle $d_{\mathrm{eff}} = 1/24$. For the transmitter, this means that the preamble has to be six times longer. Of course the situation is a bit more relaxed and t_{sleep} can be shorter if $P_{\mathrm{start}} < P_{\mathrm{rx}}$.

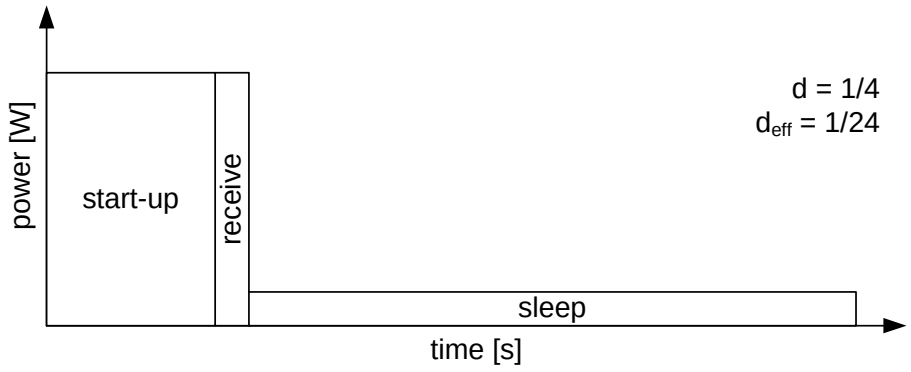


Figure 12.2.: Duty cycle dominated by start-up

12.1.2. Lower Limit of the Start-Up Time

Virtually every high performance receiver requires a very precise frequency reference to generate a LO signal, which is then used to downconvert a received signal to lower frequency bands. A good overview of relevant receiver architectures can be found in [99]. The start-up time of this high precision oscillator limits the start-up time of a receiver. The most common frequency reference is a quartz crystal. Quartz crystals are available up to frequencies of around 40 MHz and with quality (Q) factors around 10^4 up to 10^5. As a rule of thumb, the start-up time of an oscillator is proportional to the product of its Q and the period of its center frequency f_{c} [42]. A more detailed derivation of the minimum startup time of a crystal oscillator can be found in [95], where the time until the oscillator has reached quiescent operation is shown to be about 1,200 cycles. For a 10 MHz quartz, this means 120 µs. By using a resonator with a higher resonant frequency, the start-up time of the receiver can be reduced significantly. The BAW based oscillators used in the eCubes transceiver directly oscillate at the carrier frequency of 2.1 GHz or 2.4 Ghz respectively. In contrast to this, typical quartz based systems use a voltage controlled oscillator (VCO) which derives its frequency accuracy from the quartz in a phase locked loop (PLL). The PLL also requires a certain time until it has locked and this time of course has to be added to the start-up time of the oscillator. The Q value of the used BAW resonators is around 1,000. Figure 12.3 shows the measured start-up time of the oscillator. From the moment when the enable signal goes to high, it takes about 1.5 µs until the system is stable. This measurement has been performed with the oscillator in the transmit path because it can easily be measured at the antenna-pin. The measured start-up time is very short compared to commercially available crystal based systems like [40] (0.5 ms) or [41] (2 ms).

With the presented architecture, it is possible to use the main receiver as wake-up receiver by applying a duty-cycled mode of operation with a high repetition rate.

The wake-up criterion should be evaluated in two stages.

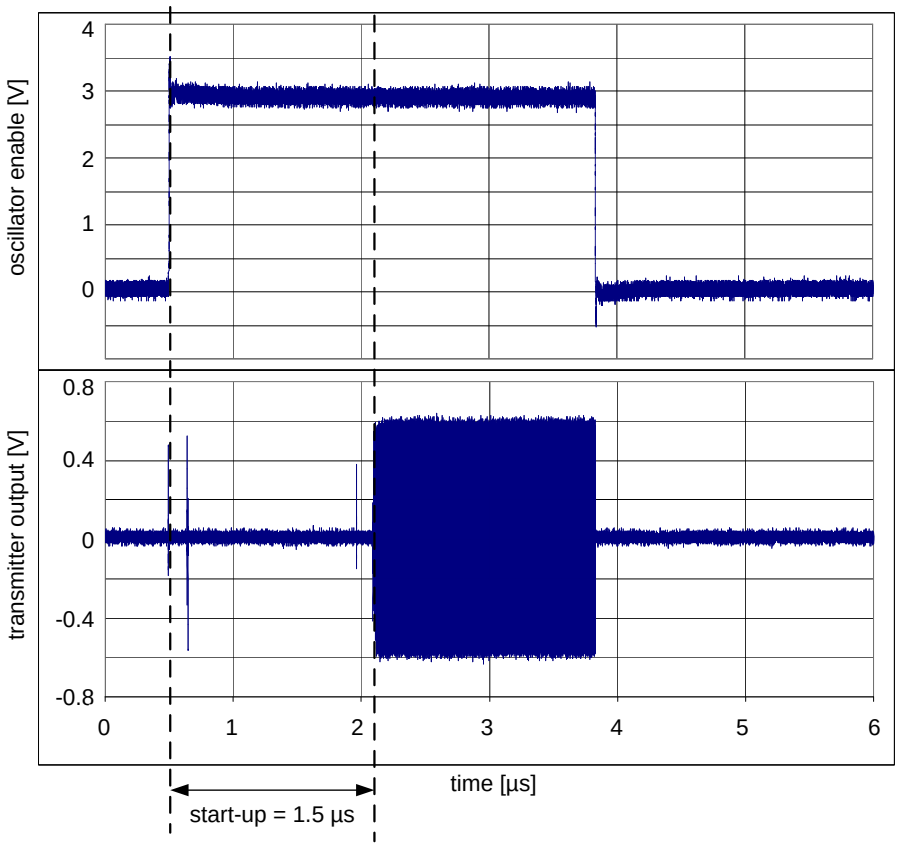


Figure 12.3.: Start-Up Measurement

1. The RSSI value can be evaluated very quickly. If it is above a certain threshold, a carrier is present. If this is not the case, then the receiver can go back into sleep mode immediately. The sensitivity of this first stage can be configured by choosing the threshold accordingly.

2. If a carrier has been detected, the receiver remains active and polls for a run-in sequence. The sensitivity of this second stage depends on the data-rate of the transmitted signal, and is a trade-off with power consumption. With a lower datarate, the sensitivity of the receiver increases, but on the other hand, a lower datarate means that both the receiver and the transmitter have to be active for a longer period, which increases the power consumption (or decreases the repetition rate).

12.2. Optimization of the Overall Power Consumption

In order to compare the BAW based approach to a conventional crystal based system, the power consumption of the system, including the receiver and the transmitter is evaluated. Table 12.1 contains values for the given parameters. The values concerning the power consumption of the BAW based transmitter have been published in [7]. In order to allow for a fair comparison, a crystal based receiver is assumed which has the same values

Receiver	
P_{start}	3 [mW]
t_{start}	0.5 [µs] (BAW)
	120 [µs] - 2 [ms] (Quartz)
P_{rx}	24 [mW]
t_{rx}	30 [µs]
P_{slp}	3 [µW]
Transmitter	
P_{tx}	18 [mW]
P_{slp}	3 [µW]

Table 12.1.: Transmitter and receiver parameters

for P_{start}, P_{rx}, t_{rx} and P_{slp} as the BAW based receiver. Only t_{start} is different, and varied from 120 µs as calculated in [95], to 0.5 ms and 2 ms as reported in [40] and [41]. As mentioned in Chapter 10 the power consumption of the BAW based system might be misleading, as most blocks are supplied by linear voltage regulators which dissipate a lot of power because the chip-supply is 3 V while most of the circuits require supply voltages of 2 V or 1.5 V. However, for comparison with crystal based systems this is not important as long as the same assumptions are made for all systems. With a lower supply voltage all power consumptions scale down by the same factor.

Figure 12.4 shows the system's power consumption assuming one wake-up event per second, plotted versus the repetition rate of the receiver. With a higher repetition rate, the power consumption of the transmitter decreases while the power consumption of the receiver increases. The power consumption of the receiver increases because for a given active time as defined by t_{start} and t_{rx} in Table 12.1, only t_{slp} can be scaled to achieve a certain repetition rate. Thus the duty cycle of the receiver is changed, and a higher repetition rate means a higher power consumption. For the transmitter, the higher repetition rate means that the preamble can be shorter and the power consumption decreases. When the two power consumptions are added in order to evaluate the system's power consumption, an optimum can be found.

For very low repetition rates, the overall power consumption is dominated by the transmitter, while the receiver dominates the power consumption for higher repetition rates. The optimum of the overall power consumption can be found where the two power consumptions are equal. So the power consumption of the receiver as well as of the transmitter is half the system power consumption shown in the graphs. One can observe, that for the crystal based system, the power consumption increases much faster with a higher repetition rate than the power consumption of the BAW based system. This effect is caused by t_{start} which becomes the dominating factor compared to t_{rx} and t_{slp}.

12.3. Required Extension to the Presented Transceiver

Not yet implemented in the BAW based transceiver is the low power real time clock (RTC) with the purpose of triggering the duty cycle. The real time clock of the sensor node is provided by the µController. For low power duty-cycling of the receiver however this is not

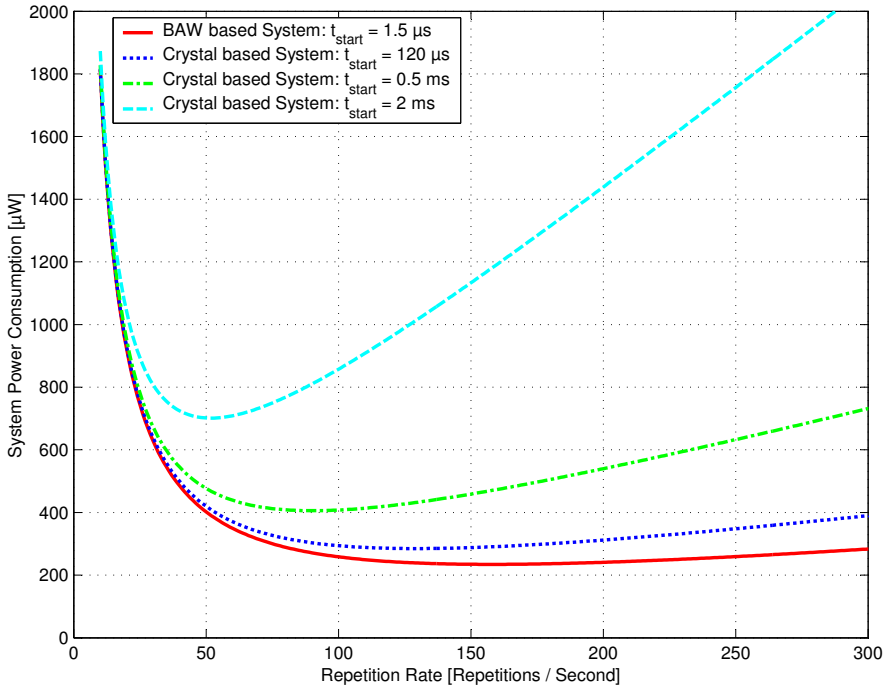


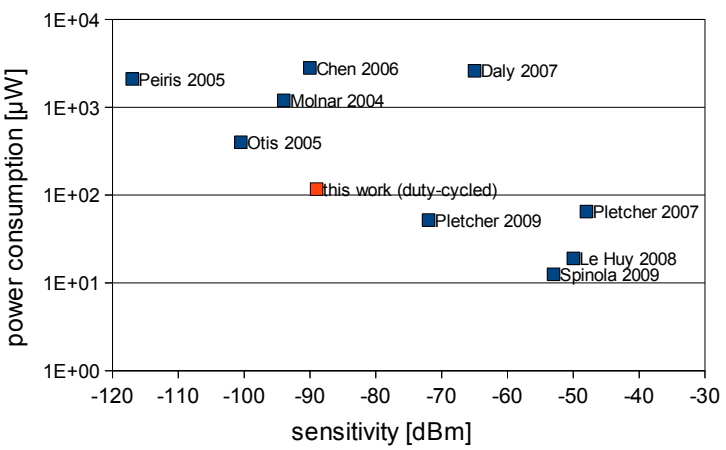
Figure 12.4.: System power consumption vs repetition rate

sufficient, because the communication between the µController and the transceiver and the configuration of the transceiver produces a high overhead.

12.4. Power Management Unit

A power management unit (PMU) suitable for wireless sensor networks has been developed in another EC funded project called CHOSeN (Cooperative Hybrid Objects Sensor Networks) [102]. The transceiver developed in the CHOSeN Project is not based on BAWs but on a conventional crystal oscillator, but it includes a very innovative power management which divides the transceiver into four different power domains. An overview is given in Figure 12.6.

A description of the PMU with focus on the RTC has been published in [13]. Each of the power domains can be switched off separately when it is not required. In this way it is possible to implement very energy efficient power down and deep sleep states. The supply voltage of the ASIC is 3.3 V, however some of the building blocks require a supply of 1.5 V. For this purpose a number of voltage regulators are integrated on chip and activated when the corresponding power domains are active. In *Power Down*, only the asynchronous wake-up unit is active. This block is able to detect external events and wakes up the transceiver. Additionally the attachment of a battery is detected as an event which activates the transceiver. Besides the *Power Down* state, the transceiver supports four different *Deep Sleep* states in which the power consumption is also only the range of a few µW as shown in Table 12.2. In *Deep Sleep*, not only the asynchronous wake-up



References	
Peiris 2005	[38]
Chen 2006	[56]
Molnar 2004	[37]
Daly 2007	[39]
Otis 2005	[110]
Pletcher 2007	[92]
Pletcher 2009	[90]
Le Huy 2008	[36]
Spinola 2009	[89]

Figure 12.5.: Comparison with implementations of wake-up receivers

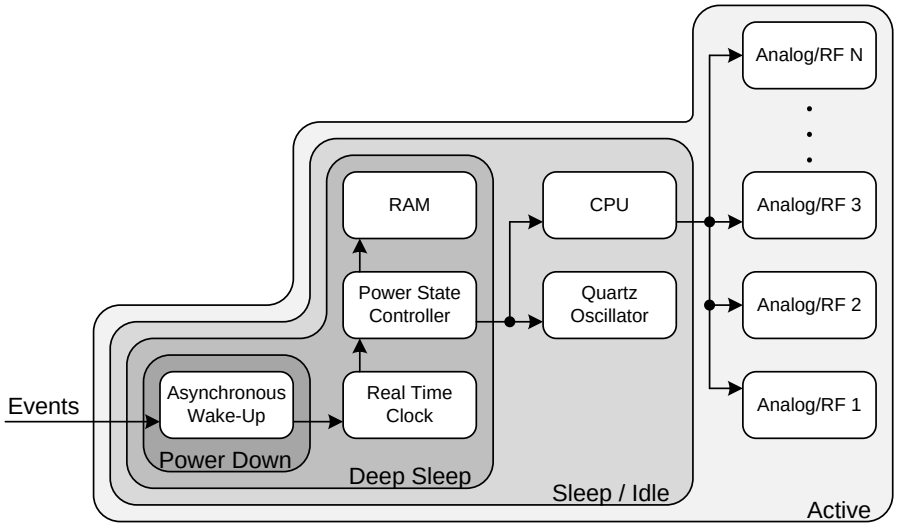


Figure 12.6.: Power Domains

unit, but also a power state controller (PSC) is active. The PSC is a small state machine, which can wake up the main state machine of the transceiver after a defined *Deep Sleep* time. In *Sleep* mode, the main state machine keeps control over the system, and only the RF parts are switched off. Of course the power consumption in *Sleep* is much higher than in *Deep Sleep* mode. The PSC is clocked by a low power RTC, which has been developed by [17]. Besides the RTC also the RAM of the transceiver is in the same power domain as the PSC. In this way the state of the transceiver is retained in *Deep Sleep*. Thus, the transceiver can resume its operation after *Deep Sleep* mode. RTC and RAM can be switched on and off separately, resulting in four different *Deep Sleep* states which are shown in Table 12.2.

From a functional point of view, *Deep Sleep 4* is equivalent to *Power Down*, however the power consumption is different. In *Deep Sleep 4* a low power bandgap reference and a low power voltage regulator are active, which are deactivated in *Power Down*. Besides

State	RTC	RAM	Power Consumption
Deep Sleep 1	on	on	< 5.3 µW
Deep Sleep 2	on	off	< 4.6 µW
Deep Sleep 3	off	on	< 2.8 µW
Deep Sleep 4	off	off	< 2.5 µW
Power Down	off	off	< 0.8 µW

Table 12.2.: Deep sleep states

that, the wakeup from *Deep Sleep 4* is considerably faster than from *Power Down*.

12.5. Conclusion

In this chapter, it is shown that it is possible to use high performance communication receivers as wake-up receivers. By using appropriate duty cycles the power consumption can be reduced such that it can be compared to dedicated wake-up receivers. The presented approach offers two important advantages:

1. The only additional circuitry which is required is a low power real time clock.
2. The sensitivity of the receiver is not impaired, when it is used as a duty cycled wake-up receiver. So the presented approach is capable of outperforming dedicated wake-up receivers which suffer from a very low sensitivity. In a sensor network it does not make sense when the sensitivity of the main receiver is higher than that of the wake-up receiver.

Furthermore it has been shown that the start-up time of the LO has a major impact on the achievable repetition rate of the duty cycle. A high repetition rate is required to allow for a short preamble in the transmitted signal. In this way the power consumption of the transmitter and the whole communication system can be optimized. That is why the presented BAW based system with its short start-up time is superior to conventional crystal based transceivers.

13. 3D Integration

This chapter gives an overview of the assembly and miniaturization of the sensor nodes. The development has been carried out in three stages.

13.1. D1 - Functional Demonstrator

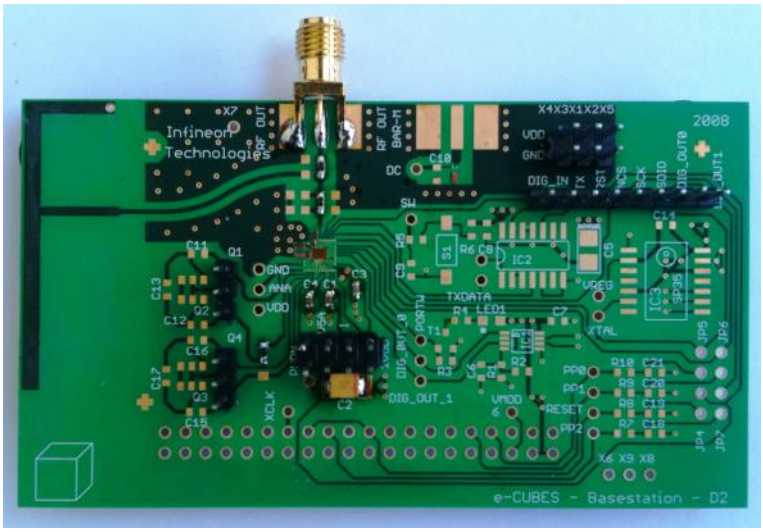


Figure 13.1.: D1 board

Figure 13.1 shows the first eCubes automotive demonstrator. It is meant to be a functional proof of concept.

13.2. D2 - MID Version no Stack

The second demonstrator is already very small-sized. In order to allow for the smallest possible size, the demonstrator is available in different versions.

- One of the versions does not include an IF filter, and no BAW resonators for the RX path are available. So the demonstrator is only a transmitter. The on-board µController measures the pressure and sends the data to another node.
- The second version of the D2 demonstrator contains a fully equipped receiver, but the sensor is not available. So it can be used as a relay node. The µController polls the receiver and forwards the data to the base station or another node. This type of sensor node is shown in Figure 13.2.

- The third version of the demonstrator contains only a fully equipped transceiver without the µController. It represents the base station and can be used in combination with a PC or laptop to visualize the transactions between the sensor nodes.

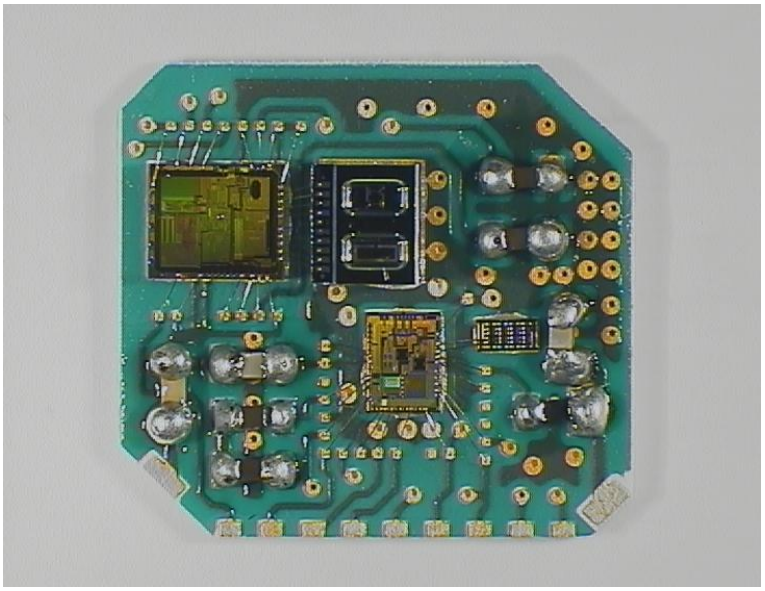


Figure 13.2.: D2 Demonstrator - Version 1

Each version of the D2 demonstrator consists of a small PCB carrying all required components. The ASICs are connected to the PCB using wire-bonds. On the backside of the PCB, there are either contact areas for small sized batteries or SMD IF filters. The PCB is then mounted into a three dimensional package called molded interconnect device (MID). An MID is an injection molded plastic part which can be selectively metalized. The body of the MID consists of a modified polymer, which can be activated by a laser beam. When the MID is then put into a chemical bath, the activated areas are metalized with a thin film of gold. This process is called the laser direct structuring (LDS) method. Figure 13.4 shows an empty MID with its lid. The lid also holds two screws which are used to close the MID and it contains a metal spring which contacts two coin cell batteries on top.

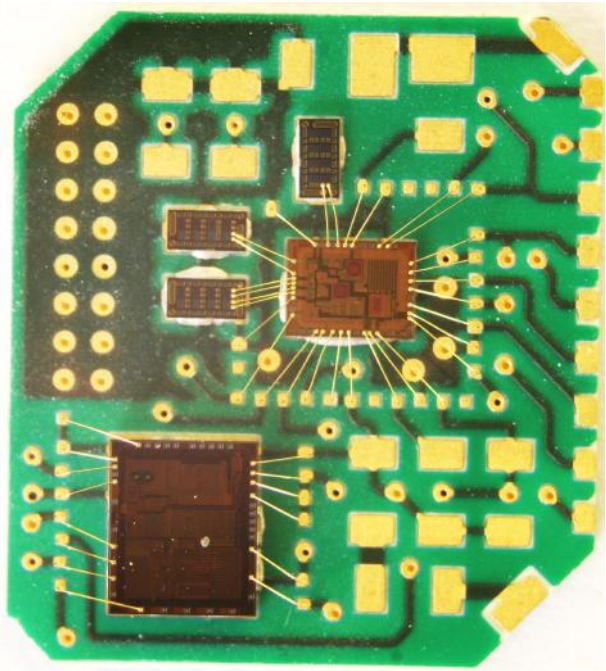


Figure 13.3.: D2 Demonstrator - Version 2

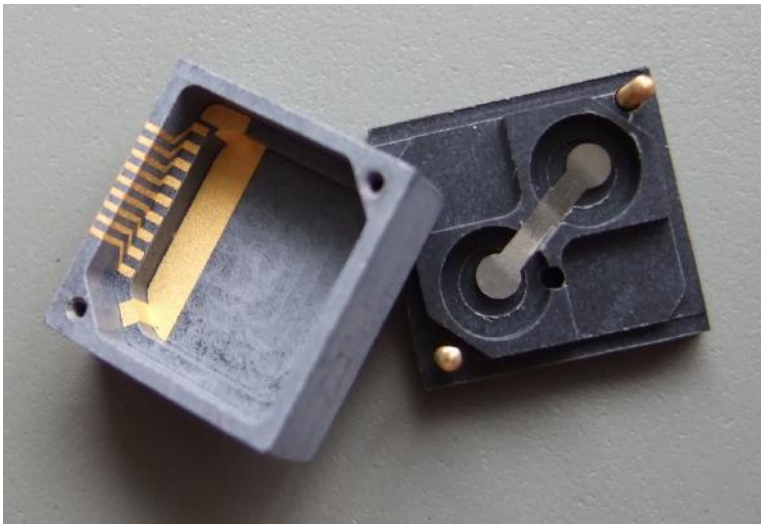


Figure 13.4.: Empty MID with Lid

Inside the MID, one can see a projection in the lower half. The PCB is placed on the edge of this projection, with the ASICs facing downward, such that the bond-wires are protected within the cavity underneath. Backfilling the MID is not possible, because the BAW resonators need the air gap for the mechanical oscillation. Commercially available BAW filters are encapsulated under a cavity, so they can be packaged easily. Only the test structures used for the e-Cubes demonstrators do not have this cavity. The metalization inside the MID serves two purposes. First, it is used to contact the PCB and the

ASICs from the outside. For this purpose, the metal lines starting on the projection and running to the outside along the walls of the MID can be used. The PCB is placed inside, such that a row of contact areas matches the metalization on the edge. And second, the metalization is used to build an antenna. The large metal area along the bottom of the MID serves as a loop antenna, whose dimensions are designed for frequencies around 2 GHz. Depending on the assembled BAW dies the resonant frequency of the antenna can be fine-tuned with SMD capacitors to be either 2.1 GHz or 2.4 GHz. The MID has been provided by project partners from Infineon in Regensburg, Germany, and the antenna has been designed by the University of Uppsala, Sweden. Figure 13.5 shows an MID where the original lid has been replaced with a PCB carrying an energy harvester. The PCB is the one which has already been shown in Figure 11.3. The metalization at the edge of the harvester PCB has been designed such that it contacts the metal lines at the edge of the MID. On the backside of the harvester PCB there are pads for soldering additional buffer capacitors.

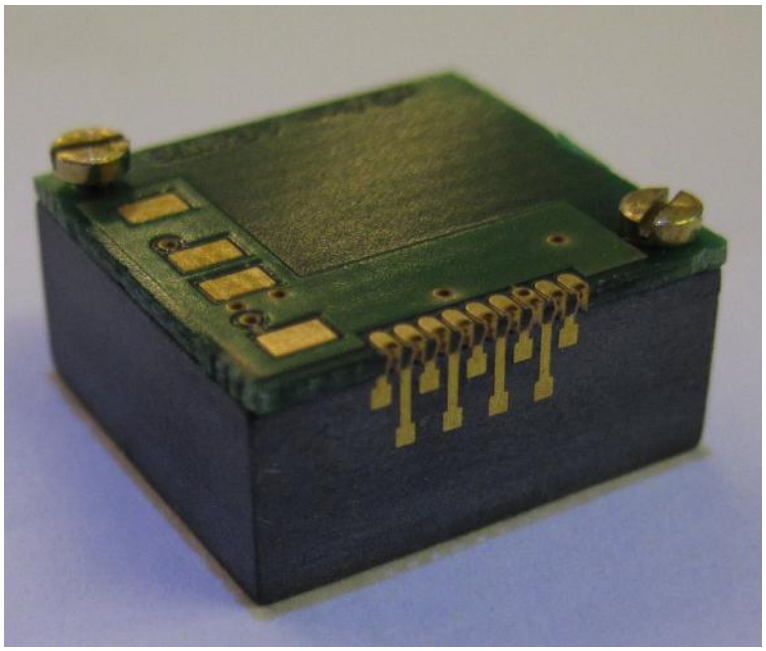


Figure 13.5.: MID with energy harvester pcb as lid

13.3. D3 - Stacked Versions

Two different 3D integration technologies have been used to build very compact sensor nodes. A very comprehensive overview of existing technologies for 3D integration of circuits can be found in [104]. In the e-Cubes project, one demonstrator has been developed using through silicon vias (TSV), and another one has been developed using the ultra thin chip stacking (UTCS) technology. By stacking the separate dies and building interconnections between them, the number of additional wire-bonds can be reduced to a minimum. The whole ASIC stacks are then bonded onto a small PCB which only carries

very few external components. As the topic of 3D-stacking is beyond the scope of this work, only a brief summary is given in this chapter.

13.3.1. TSV Stack

In the TSV version of the 3D stack, interconnects between the sensor and the µController, the transceiver and the µController, and the µController to the outside world are routed through the transceiver. For this purpose, the transceiver contains areas of 3 x 10 µm² which are reserved for the TSVs. Through these areas, holes are etched down to a depth of 60µm on wafer level. These holes are then filled with tungsten and the transceiver wafer is thinned from the backside to a total thickness of about 60µm such that the tungsten filled vias can be contacted on the backside of the transceiver. After thinning, metal redistribution layers are processed on the top and on the bottom side of the wafer. The TSVs for the eCubes automotive demonstrator have been processed by Fraunhofer IZM Munich. All process steps are explained in detail in [14].

Figure 13.6 shows the structure of the TSV stack. The bottom layer is the µController, on top of which one can see a metal redistribution layer. µBumps are used to contact the metal redistribution layer on the bottom side of the transceiver, which is placed on top of the µController. This two-layer stack is filled with a backfiller to provide a higher robustness and stability. The top metal redistribution layer of the transceiver is connected to the sensor and the BAW die via stud-bumps. Stud bumps are metal balls which are used for flip-chipping in a process which is similar to thermosonic wire-bonding whereas µ-Bumps are smaller and the process is more similar to soldering. Underneath the BAW die it is not possible to apply a backfiller, because the resonators require an open cavity.

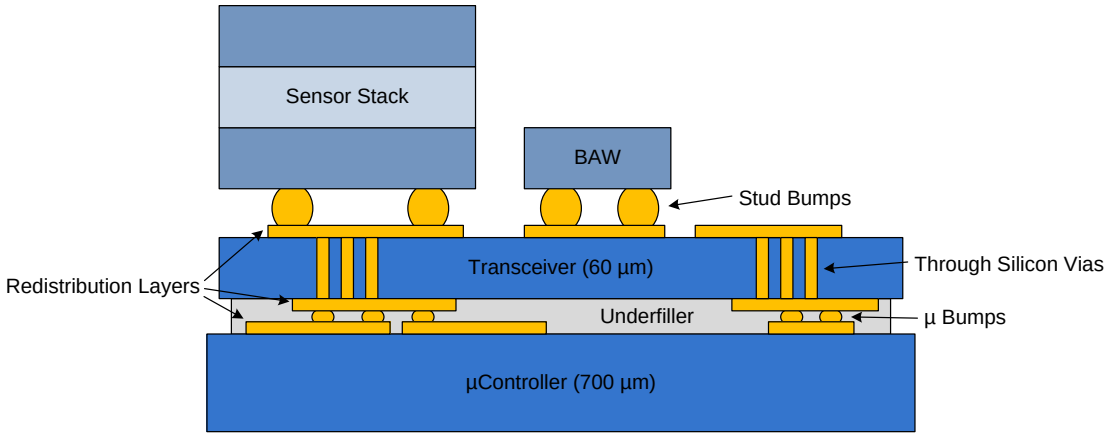


Figure 13.6.: TSV process

Figure 13.7 shows the TSV stack mounted onto the PCB which is then glued into the MID. Figure 13.8 shows the TSV stack in a transparent model of the MID. The transparent MID is not functional, as no metalization is available there.

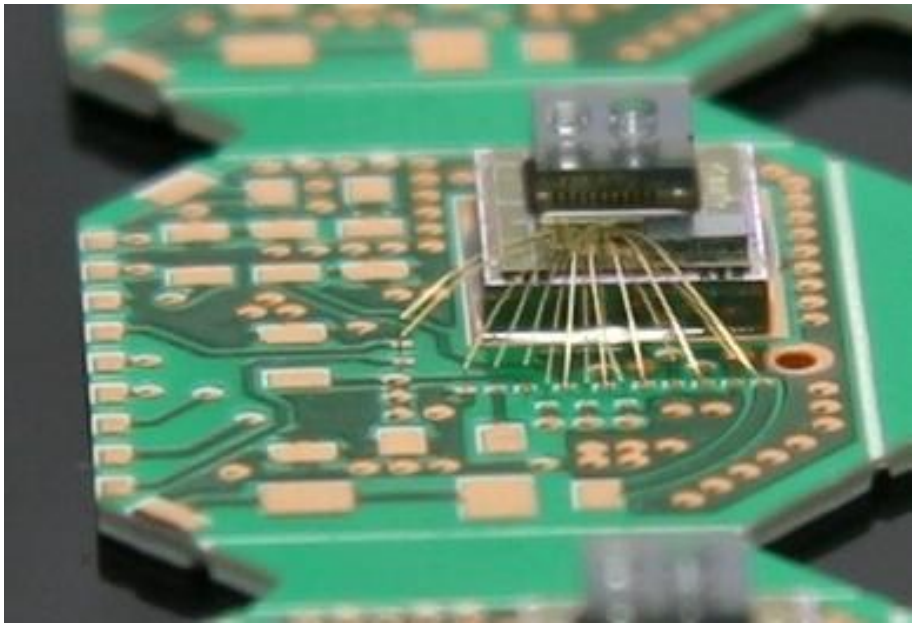


Figure 13.7.: TSV stack

13.3.2. UTCS Stack

In contrast to the TSV process, the UTCS technology does not rely on through silicon vias. With the UTCS technology, all components of the stack are thinned and mounted onto a carrier substrate. Figure 13.9 shows a simplified representation of the structure of the UTCS stack.

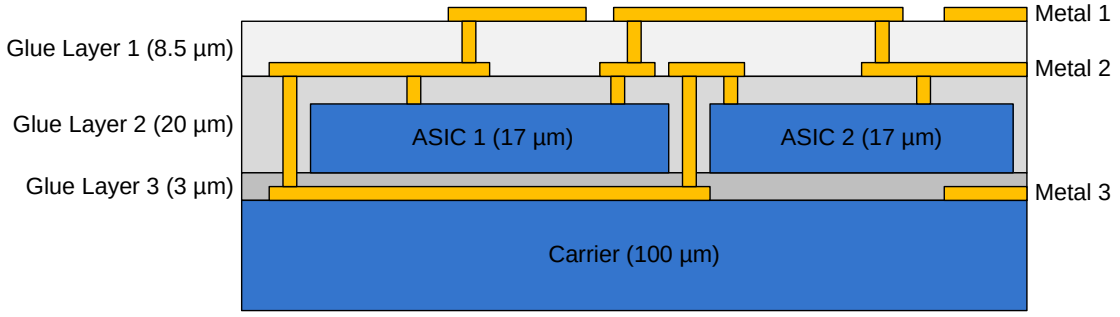


Figure 13.9.: UTCS process

The lowest layer of the stack is an interposer wafer, which is thinned to 100 µm. On top of the interposer follows the first metal redistribution layer which is then covered by a glue layer with a thickness of 3 µm. This first glue layer carries the µController and the transceiver which are thinned to a thickness of 17 µm. The active ASICs are embedded in the second glue layer, on top of which lies the second metal redistribution layer. Finally the stack contains one more glue layer and also a third metal layer. The third metal layer is used for wire bonding and for flip chipping the BAW and the sensor die. The process has been carried out by IMEC in Leuven, Belgium, and is described in detail in [81], [82]

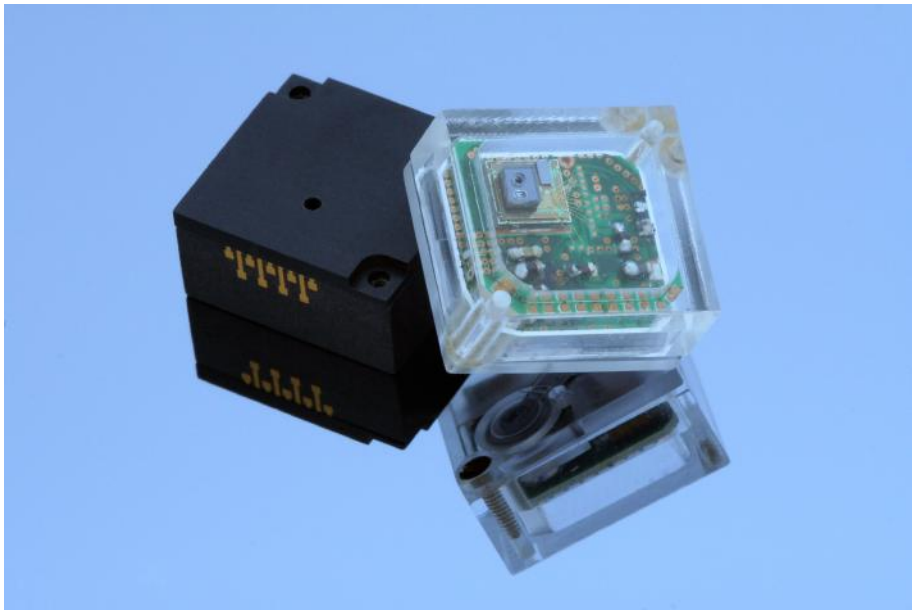


Figure 13.8.: Transparent MID, Source: SINTEF

and [83].

The UTCS stack itself has been designed in two versions. In the smaller version of the stack, the pads for flip-chipping the sensor and the BAW die are located directly above the µController and the transceiver respectively. This version of the stack is shown in Figure 13.10.

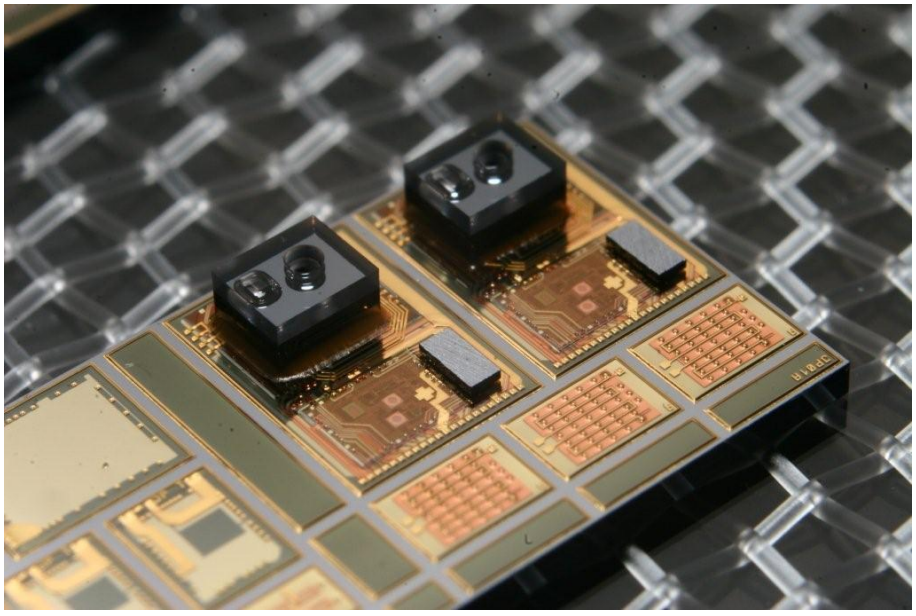


Figure 13.10.: TCI stack

In order to make sure that the µController and the transceiver are not damaged due to

stamping forces during the flip-chipping process, another version of the stack has been designed where the sensor and the BAW are not located directly above the ASICs, but beside them as shown in Figure 13.11. The stack in Figure 13.11 is only a test structure. It does not contain the µController ASIC, instead there is a large empty area. The square metal areas in the lower right corner of the stack are meant for soldering SMD capacitors on top of the stack. These capacitors are required for fine-tuning the MID-antenna and for the on-chip voltage regulators. If not soldered on top of the stack, these SMDs have to be mounted onto the PCB carrying the stack, as in all other versions of the demonstrator.

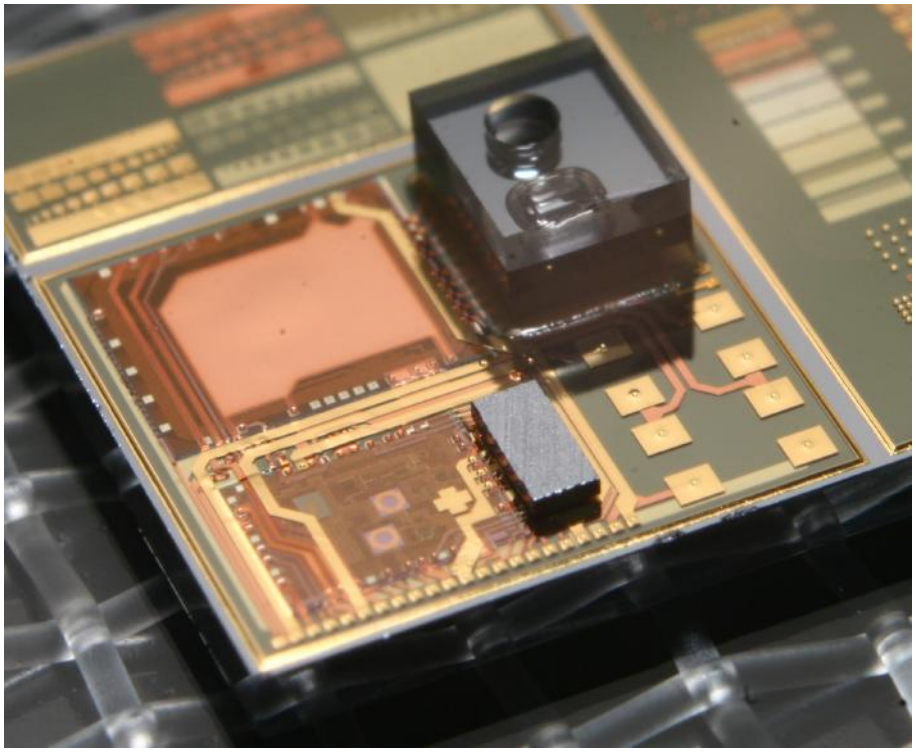


Figure 13.11.: UTCS Stack with pads for SMDs

13.4. Conclusion

This chapter gives an overview of the activities which have been carried out in close cooperation with project partners from within Infineon and from universities and other industrial partners to achieve a miniaturization of the presented sensor nodes to below 1 cm^3. The evolution of the sensor node is described and the technologies which have been applied are explained.

14. Research Summary

To conclude this thesis, a short summary of the work is given in this chapter. The main aspects and novelties covered in the work are highlighted and an overview of published papers is given.

14.1. Summary

The context of this thesis is a miniaturized sensor node for automotive applications. This work covers several aspects of receivers in wireless sensor networks, with a special focus on automotive requirements.

- The requirements for sensor networks in general and automotive sensor networks in particular have been explained. These requirements are:
  - The volume of the sensor node has to be below 1 cm^3.
  - The total weight must not exceed 5 grams.
  - A lifetime of 10 years is required.
  - The allowed temperature range is from -40°C to +125°C.
  - The sensor node has to withstand forces of thousands of g.
  - The total average power consumption must not exceed 10 µW.
- An appropriate receiver architecture has been defined, implemented and tested, according to the specifications derived from the requirements. The key facts of the developed frontend include:
  - The whole system is based on BAW resonators which are used as frequency reference and for filtering.
  - The receiver is an image-reject architecture which generates its I- and Q-phases from the RF input signal by applying a polyphase filter.
  - Further image rejection is achieved by selecting an IF of 10.7 MHz which allows to exploit the parallel and the series resonance frequencies of the applied BAWs.
  - The peak current consumption of the receiver does not exceed 8 mA including all sub-components from voltage regulators to the local oscillator.
- BAW technology has explained and its suitability for receivers in wireless sensor networks has been evaluated.
  - Comparison with SAW technology has been given.

  - The problem of temperature drift has been explained as solutions have been shown.
  - The BVD-model which is typically used for circuit simulations has been explained.
- RF circuits for the chosen receiver frontend have been developed and tested.
  - An LNA has been designed which directly includes BAW resonators for narrowband filtering at RF.
  - The LNA only consumes 2 mA from a 2 V supply.
  - A matching network topology has been designed which is implemented completely on-chip without any off-chip passive components.
  - The power gain of the LNA is 18.5 dB at a NF of 4.8 dB.
- The impact of startup time on total power consumption has been evaluated and it has been shown that with the developed architecture significant improvements with respect to conventional architectures can be achieved.
  - Due to the fast start-up of the BAW based oscillator, which is 100 - 1000 times shorter than that of a crystal based oscillator, a duty cycle with an extremely high repetition rate can be applied.
  - By making use of this fast duty-cycling, the need for an external wake-up receiver can be avoided at an even higher performance.
  - The described approach presents an optimum because it balances power consumption between receiver and transmitter,
  - and it avoids the problem that dedicated wake-up receivers have much lower sensitivities than the main communication receivers they should activate.
  - The dissipated power when balanced with the transmitter is only 117 µW.
- An outlook on different techniques for 3D-stacking of ASICs and for miniaturization of sensor nodes has been given.
  - The suitability of MID-type packages for sensor nodes has been evaluated and an MID has been designed with a volume below 1 cm^3 which holds all required components of the sensor node including batteries.
  - Also the antenna has been metalized into the structure of the MID.
  - A 3D-integrated ASIC stack using TSVs has been manufactured, to further reduce the volume and the number of wire-bonds of the sensor node.
  - A second version of the ASIC stack has been manufactured using the UTCS technology.

14.2. Novelties in the Presented Work

The core of this work is a receiver frontend which is tailored to the needs of wireless sensor networks for automotive applications. A receiver architecture has been developed

which makes use of BAW resonators for reference frequency generation and for filtering. The intermediate frequency of the receiver frontend has been chosen in a way such that the transfer function of single resonators is optimally exploited to cancel the image frequency. For this purpose a low noise amplifier incorporating these resonators has been designed and integrated into the frontend. Also in terms of power consumption investigations have been carried out, how the developed frontend can ideally be operated. It has been shown that by making use of excessive duty cycling which is possible due to the short start-up time of the system, the average power consumption of the receiver can be low enough to compete with dedicated wake-up receivers. As a result, this work constitutes a significant contribution to the design of a network of miniaturized sensor nodes. Other aspects of the design of such nodes such as for example vertical stacking of dies are also described in the text.

14.3. Summary of Published Works

In the course of the project, a number of international conference and journal papers as well as book chapters have been published. A summary of all published works is given below.

Published as Main Author Within the works published as main author, all main aspects and novelties of this thesis are covered.

- [1]: *A Robust Wireless Sensor Node for in-Tire-Pressure Monitoring*
  This work gives an overview of the sensor node and its application. It covers the architecture including all components and their assembly. The most important circuits are described and also relevant communication protocols are mentioned.
- [2]: *Image Rejection with a BAW Resonator and an Image Reject Architecture*
  This publication goes into detail regarding the developed receiver architecture. The concept of image rejection is explained and it is shown how the benefits of the BAW based transceiver topology can be exploited to achieve the highest possible performance.
- [3]: *A Low Noise Amplifier with On-Chip Matching Network and Integrated Bulk Acoustic Wave Resonators for High Image Rejection*
  In this publication the LNA together with the matching network is described in detail. It is highlighted that the matching network does not require any off-chip passive components and still provides input impedance match for the LNA, output match for the Power Amplifier and also the RX/TX switch is implemented on chip. The novel architecture of the LNA, directly including BAW resonators for narrowband filtering at RF is explained in detail.
- [4]: *A BAW based Transceiver used as Wake-Up Receiver*
  This publication summarizes the features and benefits explained in the works described above and shows how the architecture can be optimally exploited to achieve a fully functional sensor node providing bi-directional communication while achieving extremely low power consumption. The low power consumption is achieved by

duty-cycling with a very high repetition rate which is enabled by the BAW based approach.

Published as Co-Author Some of the works published as co-author are very closely related to the design of the receiver in the context of the wireless sensor node, others are more process related or deal with higher levels of abstraction in the sensor network.

- [6]: *A bulk acoustic wave(BAW)-based sensor node for automotive wireless sensor networks*
  This work describes the PLL-less approach of replacing the crystal based oscillator with a BAW based solution.

- [7]: *A robust wireless sensor node for in-tire-pressure monitoring*
  [5]: *A bulk acoustic wave (BAW) based transceiver for an in-tire-pressure monitoring sensor node*
  These papers also describe the transceiver in the context of the overall architecture of the sensor node. A detailed description of the oscillator circuit is given and the temperature compensation is shown in detail.

- [14]: *Miniaturised sensor node for tire pressure monitoring (e-CUBES)*
  This publication contains a detailed description of the 3D-integrated ASIC-stack using TSV technology. All process steps including thinning of the wafers, generation of the vias, and stacking of the different ASICs are explained in detail.

- [8]: *Design issues of BAW employment in 3D integrated sensor nodes*
  [9]: *Miniaturization of a wireless sensor node by means of 3d interconnects*
  [11]: *Miniaturization of a wireless senor node by means of 3d interconnects: An invited talk*
  [10]: *Design issues of BAW employment in 3d integrated sensor nodes*
  These works describe aspects which have to be considered during the design of the 3D-ASIC-stack and problems that arise. The topics described include temperature gradients due to self heating and the resulting temperature drift of the BAW based oscillator and the suitability of TSVs for RF signals.

- [12]: *Optimized protocol processing for a low-power wireless senor node*
  In this work, a protocol processing unit optimized for low power MAC protocols is presented.

- [15]: *A power management unit for ultra-low power wireless sensor networks*
  [16]: *Asynchronous logic application in a power management unit for low power sensor nodes*
  [13]: *A 100 kHz voltage controlled oscillator embedded in a power management unit for ultra low power sensor nodes*
  These works describe the architecture of the power management unit which is required for the duty-cycling approach presented in [4]. A detailed description of the PMU-architecture is given in [15] while [13] and [16] concentrate on the real time clock and event-detection respectively.

A. Own Publications

Publications

[1] **M. Dielacher**, M. Flatscher, T. Herndl, T. Lentsch, R. Matischek, J. Prainsack, and W. Weber, “A Robust Wireless Sensor Node for in-Tire-Pressure Monitoring,” *MEMS-based Circuits and Systems for Wireless Communication (accepted for publication)*, Springer, 2012.

[2] **M. Dielacher**, M. Flatscher, J. Prainsack, R. Matischek, T. Herndl, and W. Pribyl, “Image rejection in a receiver frontend by means of BAW resonators and an image-reject architecture,” *e & i Elektrotechnik und Informationstechnik*, vol. 126, no. 11, pp. 408–414, November 2009. [Online]. Available: http://www.springerlink.com/content/07n7277m82716710/

[3] **M. Dielacher**, M. Flatscher, and W. Pribyl, “A low noise amplifier with on-chip matching network and integrated bulk Acoustic Wave resonators for high image rejection,” in *Research in Microelectronics and Electronics, 2009. PRIME 2009. Ph.D.*, July 2009, pp. 172–175.

[4] **M. Dielacher**, J. Prainsack, M. Flatscher, R. Matischek, T. Herndl, and W. Pribyl, “A BAW based Transceiver used as Wake-Up Receiver,” in *Workshop on ultra low power wireless sensor networks*, February 2010.

[5] M. Flatscher, **M. Dielacher**, T. Herndl, T. Lentsch, R. Matischek, J. Prainsack, W. Pribyl, H. Theuss, and W. Weber, “A Bulk Acoustic Wave (BAW) Based Transceiver for an In-Tire-Pressure Monitoring Sensor Node,” *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 1, pp. 167–177, Jan. 2010.

[6] M. Flatscher, **M. Dielacher**, J. Prainsack, R. Matischek, T. Herndl, T. Lentsch, and W. Pribyl, “A bulk acoustic wave(BAW)-based sensor node for automotive wireless sensor networks,” *e & i Elektrotechnik und Informationstechnik*, vol. 125, no. 4, pp. 143–146, April 2008. [Online]. Available: http://www.springerlink.com/content/a58293j8259t5t72/

[7] M. Flatscher, **M. Dielacher**, T. Herndl, T. Lentsch, R. Matischek, J. Prainsack, W. Pribyl, H. Theuss, and W. Weber, “A robust wireless sensor node for in-tire-pressure monitoring,” *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, pp. 286–287,287a, Feb. 2009.

[8] J. Prainsack, **M. Dielacher**, M. Flatscher, T. Herndl, R. Matischek, J. Stolle, and W. Weber, “Design issues of BAW employment in 3D integrated sensor nodes,” in *Design, Test, Integration & Packaging of MEMS/MOEMS, 2009. MEMS/MOEMS ’09. Symposium on*, April 2009, pp. 81–85.

[9] J. Prainsack, J. Stolle, J. Weber, **M. Dielacher**, M. Flatscher, T. Herndl, R. Matischek, P. Ramm, and W. Weber, “Miniaturization of a Wireless Sensor Node by Means of 3D Interconnects,” *ECS Transactions*, vol. 25, 2010.

[10] J. Prainsack, **M. Dielacher**, M. Flatscher, T. Herndl, R. Matischek, J. Stolle, and W. Weber, “Design issues of BAW employment in 3D integrated sensor nodes,” *Microsystem Technologies*. [Online]. Available: http://www.springerlink.com/content/911r082471425665/

[11] J. Prainsack, **M. Dielacher**, M. Flatscher, T. Herndl, R. Matischek, P. Ramm, J. Stolle, J. Weber, and W. Weber, “Miniaturization of a Wireless Sensor Node by Means of 3D Interconnects: An Invited Talk,” *ECS Meeting Abstracts*, vol. 902, no. 26, pp. 2172–2172, 2009. [Online]. Available: http://link.aip.org/link/?ECA/902/2172/1

[12] R. Matischek, **M. Dielacher**, M. Flatscher, T. Herndl, and J. Prainsack, “Optimized Protocol Processing for a Low-Power Wireless Senor Node,” in *Workshop on ultra low power wireless sensor networks*, February 2010.

[13] P. Unterkircher, **M. Dielacher**, and M. Auer, “A 100 kHz Voltage Controlled Oscillator Embedded in a Power Management Unit for Ultra Low Power Sensor Nodes,” in *Austrochip*, October 2010.

[14] K. Schjølberg-Henriksen, M. M. V. Taklo, N. Lietaer, J. Prainsack, **M. Dielacher**, M. Klein, J. Wolf, J. Weber, P. Ramm, and T. Seppänen, “Miniaturised Sensor Node for Tire Pressure Monitoring (e-CUBES),” in *Advanced Microsystems for Automotive Applications 2009*, ser. VDI-Buch. Springer Berlin Heidelberg, 2009, pp. 313–331. [Online]. Available: http://www.springerlink.com/content/g8136nq26430m267/

[15] H. Unterassinger, **M. Dielacher**, M. Flatscher, S. Gruber, G. Kowalczyk, J. Prainsack, T. Herndl, J. Schweighofer, and W. Pribyl, “A Power Management Unit for Ultra-Low Power Wireless Sensor Networks,” 2011, submitted to AFRICON 2011.

[16] G. Kowalczyk, **M. Dielacher**, M. Flatscher, J. Prainsack, H. Unterassinger, J. Schweighofer, and S. Gruber, “Asynchronous Logic Application in a Power Management Unit for Ultra Low Power Sensor Nodes,” 2011, submitted to AFRICON 2011.

Supervised Master's and Bachelor's Theses

[17] P. Unterkircher, "A 100 khz voltage controlled oscillator embedded in a power management unit for ultra low power sensor nodes," Master's thesis, TU Graz, 2010.

[18] F. Vollmaier, "Development of a demonstrator for tire pressure monitoring," Bachelor's thesis, TU Graz, 2011, unpublished.

Patent Applications

[19] T. Herndl, M. Dielacher, M. Flatscher, and M. Greschitz, "System including receiver frontends," Patent Application 20 100 233 983, September 16, 2010.

[20] J. Prainsack, M. Dielacher, M. Flatscher, and R. Matischek, "Medium access control in industrial and automotive wireless with combined wired and wireless sensor networks," Patent Application 20 090 310 571, December 17, 2009.

[21] J. Prainsack, M. Dielacher, M. Flatscher, and R. Matischek, "Generating a phase value for a complex signal," Patent Application 20 090 237 155, September 24, 2009.

B. Bibliography

[22] M. Loehndorf, T. Kvisteroy, E. Westby, and E. Halvorsen, "Evaluation of Energy Harvesting Concepts for Tire Pressure Monitoring Systems," in *Technical Digest, PowerMEMS 2007*, 2007, pp. 331–334.

[23] E. Halvorsen, E. Westby, S. Husa, A. Vogl, N. Ostbo, V. Leonov, T. Sterken, and T. Kvisteroy, "An electrostatic energy harvester with electret bias," in *Solid-State Sensors, Actuators and Microsystems Conference, 2009. TRANSDUCERS 2009. International*, 2009, pp. 1381 –1384.

[24] J. Park, D. Lee, J. Park, Y. Chang, and Y. Lee, "High performance piezoelectric MEMS energy harvester based on D33 mode of PZT thin film on buffer-layer with PBTIO3 inter-layer," in *Solid-State Sensors, Actuators and Microsystems Conference, 2009. TRANSDUCERS 2009. International*, 2009, pp. 517 –520.

[25] J. Liu, H. Fang, Z. Xu, X. Mao, X. Shen, D. Chen, H. Liao, and B. Cai, "A MEMS-based piezoelectric power generator array for vibration energy harvesting," *Microelectronics Journal*, vol. 39, p. 802–806, 2008.

[26] X. Wang, W. Aichholzer, and J. Sturm, "A 0.1-4GHz resistive feedback LNA with feedforward noise and distortion cancellation," in *ESSCIRC, 2010 Proceedings of the*, 2010, pp. 406 –409.

[27] A. Wang, S. Cho, C. Sodini, and A. Chandrakasan, "Energy efficient modulation and MAC for asymmetric RF microsensor systems," in *Low Power Electronics and Design, International Symposium on, 2001.*, 2001.

[28] M. Fischer, *Tire Pressure Monitoring: Design and functionality of direct measuring systems*. Verl. Moderne Industrie, 2003.

[29] J. Carpentier, A. Cathelin, C. Tilhac, P. Garcia, P. Persechini, P. Conti, P. Ancey, G. Bouche, G. Caruyer, D. Belot, C. Arnaud, C. Billard, G. Parat, J. David, P. Vincent, M. Dubois, and C. Enz, "A SiGe:C BiCMOS WCDMA zero-IF RF front-end using an above-IC BAW filter," Feb. 2005, pp. 394–395 Vol. 1.

[30] M.-A. Dubois, J.-F. Carpentier, P. Vincent, C. Billard, G. Parat, C. Muller, P. Ancey, and P. Conti, "Monolithic above-IC resonator technology for integrated architectures in mobile and wireless communication," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 1, pp. 7–16, Jan. 2006.

[31] S. Razafimandimby, C. Tilhac, A. Cathelin, A. Kaiser, and D. Belot, "An Electronically Tunable Bandpass BAW-Filter for a Zero-IF WCDMA Receiver," Sept. 2006, pp. 142–145.

[32] R. Aigner, “RF-MEMS filters manufactured on silicon: key facts about bulk-acoustic-wave technology,” in *Silicon Monolithic Integrated Circuits in RF Systems, 2003. Digest of Papers. 2003 Topical Meeting on*, 2003, pp. 157 – 161.

[33] J. Borremans, P. Wambacq, G. Van der Plas, Y. Rolain, and M. Kuijk, “A Bondpad-Size Narrowband LNA for Digital CMOS,” in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE*, 2007, pp. 677 –680.

[34] D. Ho and S. Mirabbasi, “Low-Voltage Low-Power Low-Noise Amplifier for Wireless Sensor Networks,” May 2006, pp. 1494–1497.

[35] L. Aspemyr, H. Sjoland, H. Jacobsson, M. Bao, and G. Carchon, “A 5.8 GHz 1.7 dB NF fully integrated differential low noise amplifier in CMOS,” in *Microwave Conference, 2006. APMC 2006. Asia-Pacific*, 2006, pp. 309 –312.

[36] P. Le-Huy and S. Roy, “Low-Power 2.4 GHz Wake-Up Radio for Wireless Sensor Networks,” Oct. 2008, pp. 13–18.

[37] A. Molnar, B. Lu, S. Lanzisera, B. Cook, and K. Pister, “An ultra-low power 900 MHz RF transceiver for wireless sensor networks,” in *Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004*, 2004, pp. 401 – 404.

[38] V. Peiris, C. Arm, S. Bories, S. Cserveny, F. Giroud, P. Graber, S. Gyger, E. Le Roux, T. Melly, M. Moser, O. Nys, F. Pengg, P.-D. Pfister, N. Raemy, A. Ribordy, P.-F. Ruedi, D. Ruffieux, L. Sumanen, S. Todeschin, and P. Volet, “A 1 V 433/868 MHz 25 kb/s-FSK 2 kb/s-OOK RF transceiver SoC in standard digital 0.18 µm CMOS,” in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, 2005, pp. 258 –259 Vol. 1.

[39] D. Daly and A. Chandrakasan, “An Energy-Efficient OOK Transceiver for Wireless Sensor Networks,” *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 5, pp. 1003 –1011, May 2007.

[40] *TDA5250 D2 ASK/FSK 868MHz Wireless Transceiver*, Data sheet 2007 ed., Infineon Technologies AG, 2007.

[41] *CC1000 Single Chip Very Low Power RF Transceiver*, Data sheet 2008 ed., Texas Instruments, 2008.

[42] B. Neubig and W. Briese, *Das große Quarzkochbuch*. Franzis Verlag GmbH, February 2000.

[43] H. Liu and Q. He, “2.4 GHz CMOS LNA for Wireless LAN Application,” in *Millimeter Waves, 2008. GSMM 2008. Global Symposium on*, 2008, pp. 220 –222.

[44] P. Leroux, J. Janssens, and M. Steyaert, “A 0.8-dB NF ESD-Protected 9-mW CMOS LNA operating at 1.23 GHz [for GPS receiver],” *Solid-State Circuits, IEEE Journal of*, vol. 37, no. 6, pp. 760 –765, Jun. 2002.

[45] R. Point, M. Mendes, and W. Foley, “A differential 2.4 GHz switched-gain CMOS LNA for 802.11b and Bluetooth,” in *Radio and Wireless Conference, 2002. RAWCON 2002. IEEE*, 2002.

[46] J. Huang, R.-M. Weng, C.-C. Chang, K. Hsu, and K.-Y. Lin, “A 2 V 2.4 GHz fully integrated CMOS LNA,” in *Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on*, vol. 4, May 2001, pp. 466 –469 vol. 4.

[47] C.-L. Hsiao, R.-M. Weng, and K.-Y. Lin, “A 1V fully differential CMOS LNA for 2.4 GHz application,” in *Circuits and Systems, 2003. ISCAS ’03. Proceedings of the 2003 International Symposium on*, vol. 1, May 2003, pp. I–245 – I–248 vol.1.

[48] V. Chandrasekhar, C. Hung, Y. Ho, and K. Mayaram, “A packaged 2.4 GHz LNA in a 0.15 µm CMOS process with 2kV HBM ESD protection,” in *Solid-State Circuits Conference, 2002. ESSCIRC 2002. Proceedings of the 28th European*, 2002, pp. 347 –350.

[49] K. Han, J. Gil, S.-S. Song, J. Han, H. Shin, C.-K. Kim, and K. Lee, “Complete high-frequency thermal noise modeling of short-channel MOSFETs and design of 5.2-GHz low noise amplifier,” *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 3, pp. 726 – 735, 2005.

[50] X. Fan, H. Zhang, and E. Sanchez-Sinencio, “A Noise Reduction and Linearity Improvement Technique for a Differential Cascode LNA,” *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 3, pp. 588 –599, 2008.

[51] D. Linten, L. Aspemyr, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Thijs, R. Garcia, H. Jacobsson, P. Wambacq, S. Donnay, and S. Decoutere, “Low-power 5 GHz LNA and VCO in 90 nm RF CMOS,” in *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*, 2004, pp. 372 – 375.

[52] D. Linten, S. Thijs, M. Natarajan, P. Wambacq, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Donnay, and S. Decoutere, “A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS,” *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 7, pp. 1434 – 1442, 2005.

[53] J. Walling, S. Shekhar, and D. Allstot, “A gm-Boosted Current-Reuse LNA in 0.18 µm CMOS,” in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE*, 2007, pp. 613 –616.

[54] X. Li, S. Shekhar, and D. Allstot, “Gm-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18- µm CMOS,” *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 12, pp. 2609 – 2619, 2005.

[55] J. Jarvinen, J. Kaukovuori, J. Ryynanen, J. Jussila, K. Kivekas, M. Honkanen, and K. Halonen, “2.4-GHz receiver for sensor applications,” *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 7, pp. 1426 – 1433, 2005.

[56] C.-P. Chen, H.-S. Kao, C.-C. Su, and S. Li, “A 2.4-GHz Low-Power Single-Chip Tunable CMOS Low-IF ISM Receiver,” in *Solid-State and Integrated Circuit Technology, 2006. ICSICT ’06. 8th International Conference on*, 2006, pp. 1496 –1498.

[57] M. Annamalai Arasu, H. Kok Fong Ong, Y. B. Choi, and W. G. Yeoh, “A 2.4-GHz CMOS RF front-end for wireless sensor network applications,” in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2006 IEEE*, 2006, p. 4 pp.

[58] W. Kluge, F. Poegel, H. Roller, M. Lange, T. Ferchland, L. Dathe, and D. Eggert, “A Fully Integrated 2.4-GHz IEEE 802.15.4-Compliant Transceiver for ZigBee Applications,” *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 12, pp. 2767 –2775, 2006.

[59] S.-S. Yoo and H.-J. Yoo, “A Low Power Current-reused CMOS RF Front-end with Stacked LNA and Mixer,” in *Silicon Monolithic Integrated Circuits in RF Systems, 2007 Topical Meeting on*, 2007, pp. 103 –106.

[60] T. Song, H.-S. Oh, E. Yoon, and S. Hong, “A Low-Power 2.4-GHz Current-Reused Receiver Front-End and Frequency Source for Wireless Sensor Network,” *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 5, pp. 1012 –1022, May 2007.

[61] H.-M. Seo, Y. Moon, Y.-K. Park, D. Kim, D.-S. Kim, Y.-S. Lee, K.-H. Won, S.-D. Kim, and P. Choi, “A Low Power Fully CMOS Integrated RF Transceiver IC for Wireless Sensor Networks,” *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 15, no. 2, pp. 227 –231, 2007.

[62] I. Kwon, S. Song, and J. Ko, “A 1.2-V 8-mW 2.4-GHz CMOS RF Receiver IC for Low Power WPAN,” in *Sarnoff Symposium, 2006 IEEE*, 2006, pp. 1 –4.

[63] I. Kwon and K. Lee, “A low power highly linear 2.4 GHz CMOS receiver front-end using current amplifier,” in *Solid-State Circuits Conference, 2004. ESSCIRC 2004. Proceeding of the 30th European*, 2004, pp. 431 – 434.

[64] S. Kim, I. Nam, T. Kim, K. Kang, and K. Lee, “A single-chip 2.4GHz low-power CMOS receiver and transmitter for WPAN applications,” in *Radio and Wireless Conference, 2003. RAWCON ’03. Proceedings*, 2003, pp. 163 – 166.

[65] A. Hafez, M. Dessouky, and H. Ragai, “Design of a low-power ZigBee receiver front-end for wireless sensors,” in *Microelectronics, 2007. ICM 2007. Internatonal Conference on*, 2007, pp. 183 –186.

[66] *TDA5230 TDA5231 Universal Low Power ASK/FSK Single Conversion Multi-Channel Image-Reject Receiver with Digital Baseband Processing*, Data sheet 2007 ed., Infineon Technologies AG, June 2007.

[67] R. Brederlow, W. Weber, J. Sauerer, S. Donnay, P. Wambacq, and M. Vertregt, “A mixed-signal design roadmap,” *Design Test of Computers, IEEE*, vol. 18, no. 6, pp. 34 –46, 2001.

[68] J. Borremans, P. Wambacq, C. Soens, Y. Rolain, and M. Kuijk, “Low-Area Active-Feedback Low-Noise Amplifier Design in Scaled Digital CMOS,” *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 11, pp. 2422 –2433, 2008.

[69] S. Joo, T.-Y. Choi, and B. Jung, “A 2.4-GHz Resistive Feedback LNA in 0.13- µm CMOS,” *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 11, pp. 3019 –3029, 2009.

[70] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*. Kluwer Academic Publisher, 1998, iSBN 0-7923-8186-6.

[71] M. Flatscher, “A bulk acoustic wave based ultra low-power transmitter,” Ph.D. dissertation, TU Graz, 2011, unpublished.

[72] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, “CMOS mixers and polyphase filters for large image rejection,” *Solid-State Circuits, IEEE Journal of*, vol. 36, no. 6, pp. 873 –887, Jun. 2001.

[73] M. Mark, “Analysis and Optimization of a Limiting Amplifier / RSSI in a 0.13 µm CMOS Technology,” Master’s thesis, TU Graz, 2004.

[74] M. Mark, F. Darrer, and G. Dorner, “Electrical/Physical Co-Design in Case of a Robust 3.3 V, 10.7 MHz Limiting Amplifier with RSSI-Generation in a 0.13 µm Standard CMOS Process,” in *Euro DesignCon 2004*. IEC, October 2004.

[75] M. Allah, J. Kaitila, R. Thalhammer, W. Weber, and D. Schmitt-Landsiedel, “Temperature compensated solidly mounted bulk acoustic wave resonators with optimum piezoelectric coupling coefficient,” in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1 –4.

[76] M. Allah, J. Kaitila, R. Thalhammer, W. Weber, and D. Schmitt-Landsiedel, “Temperature compensated solidly mounted resonators with thin SiO2 layers,” in *Ultrasonics Symposium (IUS), 2009 IEEE International*, 2009, pp. 859 –862.

[77] I. Larson, J.D., P. Bradley, S. Wartenberg, and R. Ruby, “Modified Butterworth-Van Dyke circuit for FBAR resonators and automated measurement system,” in *Ultrasonics Symposium, 2000 IEEE*, vol. 1, Oct. 2000, pp. 863 –868 vol.1.

[78] J. Zyren and A. Petrick, “Tutorial on Basic Link Budget Analysis,” *Intersil Application Note 9804*, June 1998.

[79] T. Herndl, J. Jongsma, F. Darrer, T. Kvisterøy, C. Hambeck, S. Mahlknecht, E. Westby, S. Husa, E. Halvorsen, A. Vogl, and N. Østbø, “An Energy Harvesting System for In-tire TPMS,” International Workshop on Power Supply On Chip, Cork, Ireland, Sep 2008.

[80] H. Friis, “A Note on a Simple Transmission Formula,” *Proceedings of the IRE*, vol. 34, no. 5, pp. 254 – 256, May 1946.

[81] P. Muller, F. Iker, P. Soussan, E. Beyne, G. Carchon, and W. De Raedt, “Chip ultra-thinning and embedding technology for autonomous sensors array applications,” May 2009, pp. 1437 –1439.

[82] F. Iker, D. Tezcan, R. Teixeira, P. Soussan, P. De Moor, E. Beyne, and K. Baert, “3D Embedding and Interconnection of Ultra Thin ($<$20 µm) Silicon Dies,” dec. 2007, pp. 222 –226.

[83] F. Iker, P. Soussan, E. Beyne, and K. Baert, “Technology platform for 3-D stacking of thinned embedded dies,” may. 2008, pp. 8 –11.

[84] R. D’Errico, L. Rudant, and J. Keignart, “Channel characterization for intra-vehicle WSNs in the ISM bands,” apr. 2010, pp. 1 –5.

[85] K. Lakin, G. Kline, and K. McCarron, “High-Q microwave acoustic resonators and filters,” *Microwave Theory and Techniques, IEEE Transactions on*, vol. 41, no. 12, pp. 2139 –2146, dec 1993.

[86] “IEEE Standard on Piezoelectricity,” *ANSI/IEEE Std 176-1987*, pp. 0–1, 1988.

[87] R. Naik, J. Lutsky, R. Reif, and C. Sodini, “Electromechanical coupling constant extraction of thin-film piezoelectric materials using a bulk acoustic wave resonator,” *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on*, vol. 45, no. 1, pp. 257 –263, jan 1998.

[88] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits, Second Edition*. Cambridge University Press, 2003.

[89] M. Durante and S. Mahlknecht, “An Ultra Low Power Wakeup Receiver for Wireless Sensor Nodes,” in *Sensor Technologies and Applications, 2009. SENSORCOMM ’09. Third International Conference on*, June 2009, pp. 167–170.

[90] N. Pletcher, S. Gambini, and J. Rabaey, “A 2GHz 52 µW Wake-Up Receiver with -72dBm Sensitivity Using Uncertain-IF Architecture,” in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, Feb. 2008, pp. 524–633.

[91] S. von der Mark and G. Boeck, “Ultra low power wakeup detector for sensor networks,” in *Microwave and Optoelectronics Conference, 2007. IMOC 2007. SBMO/IEEE MTT-S International*, 29 2007-Nov. 1 2007, pp. 865–868.

[92] N. Pletcher, S. Gambini, and J. Rabaey, “A 65 µW, 1.9 GHz RF to digital baseband wakeup receiver for wireless sensor nodes,” in *Custom Integrated Circuits Conference, 2007. CICC ’07. IEEE*, Sept. 2007, pp. 539–542.

[93] E.-Y. Lin, J. Rabaey, and A. Wolisz, “Power-efficient rendez-vous schemes for dense wireless sensor networks,” in *Communications, 2004 IEEE International Conference on*, vol. 7, June 2004, pp. 3769–3776 Vol.7.

[94] P. Papadimitratos, A. La Fortelle, K. Evenssen, R. Brignolo, and S. Cosenza, “Vehicular communication systems: enabling technologies, applications, and future outlook on intelligent transportation,” *Communications Magazine, IEEE*, vol. 47, no. 11, pp. 84–95, November 2009.

[95] W. M. Sansen, *Analog Design Essentials (The Springer International Series in Engineering and Computer Science)*. Springer, 2006.

[96] J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*. 685 Canton Street, Norwood, MA 02062: Artech House, 2003, iSBN 1-58053-502-x.

[97] R. Ruby, "Review and Comparison of Bulk Acoustic Wave FBAR, SMR Technology," in *Ultrasonics Symposium, 2007. IEEE*, Oct. 2007, pp. 1029–1040.

[98] M. Kuorilehto, M. Kohvakka, J. Suhonen, P. Hämäläinen, M. Hännikäinen, and T. D. Hamalainen, *Ultra-Low Energy Wireless Sensor Networks in Practice: Theory, Realization and Deployment*. Wiley, 2008.

[99] B. Razavi, *RF Microelectronics (Prentice Hall Communications Engineering and Emerging Technologies Series)*. Prentice Hall PTR, 1997.

[100] F. Bi and B. Barber, "Bulk Acoustic Wave RF Technology," *IEEE microwave magazine*, vol. 9, no. 5, pp. 65–80, Oct. 2008.

[101] "http://www.ecubes.org."

[102] "http://www.chosen.eu."

[103] J. Chabloz, C. Muller, F. Pengg, A. Pezous, C. Enz, and M.-A. Dubois, "A Low-Power 2.4GHz CMOS Receiver Front-End Using BAW Resonators," *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, pp. 1244–1253, Feb. 2006.

[104] *3D Integration: Technology and Applications*. Wiley-VCH, 2008.

[105] H.-M. Tsai, W. Viriyasitavat, O. Tonguz, C. Saraydar, T. Talty, and A. Macdonald, "Feasibility of In-car Wireless Sensor Networks: A Statistical Evaluation," in *Sensor, Mesh and Ad Hoc Communications and Networks, 2007. SECON '07. 4th Annual IEEE Communications Society Conference on*, June 2007, pp. 101–111.

[106] G. Leen and D. Heffernan, "Expanding automotive electronic systems," *Computer*, vol. 35, no. 1, pp. 88–93, Jan 2002.

[107] G. Leen, D. Heffernan, and A. Dunne, "Digital networks in the automotive vehicle," *Computing & Control Engineering Journal*, vol. 10, no. 6, pp. 257–266, Dec 1999.

[108] G. Leen and D. Heffernan, "Vehicles without wires," *Computing & Control Engineering Journal*, vol. 12, no. 5, pp. 205–211, Oct 2001.

[109] M. Ahmed, C. Saraydar, T. ElBatt, J. Yin, T. Talty, and M. Ames, "Intra-vehicular Wireless Networks," in *Globecom Workshops, 2007 IEEE*, Nov. 2007, pp. 1–9.

[110] B. Otis, Y. Chee, and J. Rabaey, "A 400 μW-RX, 1.6mW-TX super-regenerative transceiver for wireless sensor networks," Feb. 2005, pp. 396–606 Vol. 1.

[111] D. Murali and N. Ida, "A sampling method for reduction of power in battery operated receivers," May 2008, pp. 47–50.

[112] C. Enz, J. Chabloz, J. Baborowski, C. Muller, and D. Ruffieux, “Building Blocks for an Ultra Low-Power MEMS-based Radio,” Dec. 2007, pp. 158–167.

[113] J. Ayers, K. Mayaram, and T. Fiez, “Tradeoffs in the Design of CMOS Receivers for Low Power Wireless Sensor Networks,” May 2007, pp. 1345–1348.