Design and Development of a HF-RFID Transponder to Achieve Very High Data Rates for Contactless Applications

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Graz, May 2011

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Kurzfassung

Die Dissertation ist in 9 Kapitel unterteilt. Nach einer Darstellung der Motivation für die Arbeit beschäftigt sich das zweite Kapitel mit der RFID Standardisierung und bereitet die theoretischen Fakten und Grundlagen hinsichtlich der Übertragung hoher Datenraten auf.
Die nächsten zwei Kapitel behandeln den Entwurf der analogen Eingangsstufe und diskutieren die theoretischen Grundlagen hinsichtlich der Übertragung hoher Datenraten in passiven Transponder Anwendungen.
Folgend werden unterschiedliche analoge Demodulatoren für die analoge Eingangsstufe vorgestellt und verglichen. In den weiteren Kapiteln wird auf das Layout und die Messergebnisse der Testchips eingegangen. Zum Schluss werden eine Zusammenfassung der entscheidenden Punkte der Dissertation und ein Ausblick weiterer Arbeiten im Hinblick auf hohe Datenraten dargelegt. Der Anhang beinhaltet Hintergrund- und ergänzende Informationen zum Inhalt der vorliegenden Arbeit.
Den Kern der Arbeit (Kapitel 5) bietet ein effizientes Demodulatorkonzept für die Übertragung hoher Datenraten für passive RFID Transponder basierend auf einer Trägerfrequenz von 13.56 MHz. Hierbei stellt die Demodulationsschaltung einer der wichtigsten analogen Komponenten der Transpondereingangsstufe dar. Der Datenstrom des emittierten elektromagnetischen Feldes des Lesegerätes wird durch den Demodulator extrahiert. Der Datenaustausch und die Energieversorgung finden über das gesendete elektromagnetische Feld des Lesegerätes statt.
Der Hauptfokus der entwickelten neuen analogen Eingangsstufe und der Demodulatorschaltung liegt bei einer Flächenreduktion und einer geringeren Leistungsaufnahme sowie einer gleichzeitigen Erhöhung der Detektionsrate, um hohe Übertragungsraten zu erreichen. Des Weiteren werden einige Demodulatorkonzepte miteinander verglichen. Der Schwerpunkt beruht auf der Entwicklung einer Demodulationsschaltung und den analogen Komponenten der Eingangsstufe. Zusätzlich werden einige vorliegende *trade-offs* aufgezeigt. Um die Stabilität des Systems besser untersuchen und gewährleisten zu können, wurde ein mathematisches und simulationstechnisches Modell des Demodulators eingeführt.
Ferner zeigen Simulations- und Messergebnisse, dass der integrierte Test Chip bei einer Datenrate von 13.56 Mbit/s kleinste Phasenänderungen von bis zu $\pm 3^\circ$ erkennt. Anhand der Messergebnisse kann man sehen, dass es durchaus möglich ist, einen Phasendemodulator für sehr hohe Datenraten und hoher Phasengenauigkeit zu entwickeln und gleichzeitig einen sehr geringen Stromverbrauch zu erzielen.
Im Zuge der Arbeit wurden drei *tapeouts* durchgeführt und Teststrukturen gefertigt. Die entwickelten Testchips beinhalten jeweils eine analoge Eingangsstufe und einen Demodulator und basieren auf einem 120 nm bzw. 90 nm Flash CMOS Prozess der Firma Infineon.

Abstract

The thesis has been organized in nine chapters. The first one starts with an introduction to high data rates in RFID systems. The objectives of this chapter are the RFID standardization and the theoretical aspects concerning high data transmission.
The next two chapters deal with the design of the analog front end and discuss the theoretical aspects of high data rates in passive transponder applications.
Chapter 5 compares several analog demodulators used in the analog front end. The following chapters include the layout and measurement results of the test chips.
The final chapter, offering a summary and an outlook, contains the most important achievements of the thesis and recommendation for further work related to high data rates.
Finally, the appendixes include background information and supplementary material.
The core of the thesis (chapter 5) deals with an efficient demodulator concept which allows high data rates for passive RFID transponders operating at a carrier frequency of 13.56 MHz. The demodulator is one of the major analog components of the transponder front end. It extracts the data stream from the emitted electromagnetic field of the reader. Passive transponders draw their energy from the electromagnetic field generated by the reader.
The goal of the proposed analog front end and the demodulator circuit are the reduction of area and power consumption and at the same time an increased detection rate allowing high data throughput. Several demodulator concepts are compared and the emphasis is placed on the design of the demodulator circuitry and the analog front end environment. Additionally, some trade-offs are pointed out. To enable the careful investigation of the stability of the system, a mathematical and simulation model of the demodulator concept was introduced.
Furthermore, measurement and simulation results show that the test chip is able to recognize very small phase changes down to $\pm 3^{\circ}$ at a bit rate of 13.56 Mbit/s. The measurement results demonstrated that is practicable to fabricate low power and at the same time high speed, high precision phase demodulators.
In the course of the work three tape-outs have been carried out. Each designed test chip includes an analog front end and a demodulator circuit which was processed by Infineon Technologies Austria AG in a 120 nm process respectively 90 nm Flash CMOS process.

Acknowledgements

The presented work was part of the ReadRF project, which has been partly funded by the Austrian Research Promotion Agency. So I would like to express my gratitude to the agency for the opportunity for this work.

On university side I would like to thank my supervisor Univ.-Prof. Dipl.-Ing. Dr.techn. Wolfgang Pribyl for his advice and project support.

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Special thanks to my colleagues Dipl.-Ing. Dr.techn. Albert Missoni for the analog expert support, Dipl.-Ing. Walter Kargl for the brainstorming and expert support and Georg Stadlober, as well as Peter Amreich for the layout.

I am also extremely thankful for the encouragement of my parents, Helmut and Gisela.

And last but not least, I am also especially grateful to my friend Dipl.-Ing. Dana Belovičová for her encouragement and the proofreading.

Markus Auer
Graz, May 2011

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Nomenclature

AC	Alternating Current
ADC	Analog to Digital Converter
AFE	Analog Front End
AMI	Alternate Mark Inversion
ADPLL	Analog/Digital Phase-Locked Loop
APLL	Analog Phase-Locked Loop
ASK	Amplitude Shift Keying
AWG	Arbitrary Waveform Generator
BW	Bandwidth
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
CLCC	Ceramic Leadless Chip Carrier
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
DAC	Digital to Analog Converter
EAS	Electronic Article Surveillance
EMC	Electromagnetic Compatibility
EN	European Norm
ERC	European Radiocommunications Committee
ESD	Electrostatic Discharge
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FFG	Österreichische Forschungsförderungsgesellschaft
FFT	Fast Fourier Transformation

FIB Focused Ion Beam

FPGA Field Programmable Gate Array

FSK Frequency Shift Keying

HF High Frequency

IC Integrated Circuit

ICO Current Controlled Oscillator

ICAO International Civil Aviation Organization

IEC International Electrotechnical Organization

ISM Industrial Scientific Medical (Band)

ISO International Standard Organization

JTAG Joint Test Action Group

JTC Joint Technical Comittee

M-ASK Multilevel Amplitude Shift Keying

M-PSK Multilevel Phase Shift Keying

MOS Metal Oxide Semiconductor

NMOS n-type Metal-Oxide Semiconductor

NRZ Non Return To Zero

NVM Non Volatile Memory

OTA Operational Transconductance Amplifier

PCB Printed Circuit Board

PJM Phase Jitter Modulation

PLL Phase-Locked Loop

PMOS p-type Metal-Oxide Semiconductor

PTAT Proportional to Absolute Temperature

PSK Phase Shift Keying

PFD Phase Frequency Detector

Q Quality Factor

QPSK Quadrature Phase Shift Keying

ReadRF Contact-less Reader Technology for Logistic and Data-Management Challanges

REC Recommendation

RFID Radio Frequency Identification

RMS Root Mean Square

RS232 Recommended Standard 232

RX Receive

RZ Return To Zero

SNR Signal to Noise Ratio

TAG RFID Transponder (chip and antenna)

TX Transmit

Transponder Transmitter and Responder

USB Universal Serial Bus

VCO Voltage Controlled Oscillator

VCVS Voltage Controlled Voltage Source

VHBR Very High Bit Rate

VHDR Very High Data Rate

WG8 Working Group 8

WP Work Package

1 Motivation

The amount of data being transferred between reader and transponder is increasing continuously. Media files like pictures, audios and even videos are exchanged via contact-less links between stations and devices.

General solutions are based on the standard ISO/IEC 14443 [38] for near field applications at a carrier frequency of 13.56 MHz. The maximum communication speed in common passive transponder systems for proximity applications is 848 kilobits per seconds and is typically done at ASK having 10 % modulation index. Due to bandwidth limitations in existing systems, it is not an easy task to increase the data transmission frequency of 848 kHz, which is approximately 1.2 microseconds per bit. The thesis at hand deals with the realization and integration of the transponder and in particular with the demodulator concept for the analog front end. Therefore, it was necessary to redesign the whole transponder to achieve bit-rates higher than 848 kbit/s.

Additionally, ongoing standardization activities at ISO/IEC 14443 are pointed out, with the aim of standardizing significantly enhanced data rates. Therefore high data- and detection rates are seen to be optimal for new RFID applications, such as e-government applications.

This work has been partly funded by the Austrian Research Promotion Agency with the aim of developing an RFID demodulator for high bit-rates. It was a co-operation project between the Graz University of Technology and Infineon Technologies Austria, Development Center Graz. The “ReadRF” project is divided into three distinct parts: the reader system, the transponder and the transmission channel. In the course of this, the reader system was considered by DI Edmund Ehrlich and the transmission channel by DI Walter Kargl from Infineon Technologies.

2 Introduction

2.1 Radio Frequency Identification and Applications

2.1.1 Standardization (ISO/IEC 14443, 18000-3)

There are different methods to increase data rates in a contactless reader-transponder system. Working Group 8(WG8)[1] developed three ISO proposals for high data rates in contactless chip-cards. Due to bandwidth limitations in existing systems, it is not possible to increase the data transmission frequency of 848 kHz, which is approximately $1.2\,\mu s$/bit.
One way to increase the data rate between the reader and the transponder significantly is a multi-level modulation technique using phase modulation or amplitude modulation. Another way lies in bit time reduction. However, conventional methods do not detect multiple phase angles and most methods require a period of downtime for the detection circuit to recalibrate before demodulating the next incoming data. The following sections will explain the three WG8 proposals in detail.

2.1.2 Multi Level Phase Modulation

Phase modulation is a method of modulating data signals to represent information as variations in the instantaneous phase of a carrier wave. In the Philips proposal about "very high bitrates up to 27.12 MBit/sec" a possibility to reach high data rates using phase modulation is shown for ISO/IEC standard 14443 Type A. One benefit of the phase modulation technique is the constant power transfer from the reader to the transponder. Table 2.1 shows different phase shifts depending on symbol time. A higher number of phase states and a reduction in symbol time increase the data rate. But the values above 27.12 MBit/sec are very academic (see table 2.1).

Equation 2.1 shows the logarithmic relationship between bit rate and symbol order. However, with a high symbol order the data rate does not increase as fast as with low symbol orders. In other words, due to the logarithmic curve the data rate is not increasing significantly.

$$bitrate = \frac{log_2 M}{T} \tag{2.1}$$

2.1.3 Bit Time Reduction

In this proposal amplitude modulation with smaller bit times is used ($\leq$8 periods/bit as specified in standard ISO/IEC 14443). Due to a minimization of bit time, higher data rates are possible. But the reduction of bit time combined with a high quality factor of the antenna system results in a difficult demodulation process. A comparison between data rate and bit time is given in table 2.2.

[1] Working Group within the subcommittee ISO/IEC JTC1/SC17 "Identification Cards"

Table 2.1: Multi level phase modulation. A comparison between the number of phase states used, the minimum phase difference and the bit rates achieved in theory. If the number of possible phase states increases and the minimum phase difference decreases, the bit rate will increase. Thereby bit rates above 27.12 Mbit/s are possible only in theory, because the SNR is limited by the noise influence and the maximum allowable field strength.

	Minimum Phase Difference [°]							
	180	**90**	**45**	**22.5**	**11.25**	**5.63**	**2.8**	**1.4**
	Number of Phase States [-]							
Periods/Bit	**2**	**4**	**8**	**16**	**32**	**64**	**128**	**256**
[-]	**Corresponding Bit Rate [kbit/s]**							
128	**106**	**212**	**318**	**424**	**530**	**636**	**742**	**848**
64	**212**	**424**	**636**	**848**	**1060**	**1272**	**1484**	**1696**
32	**424**	**848**	**1272**	**1696**	**2120**	**2544**	**2968**	**3392**
16	**848**	**1696**	**2544**	**3392**	**4240**	**5088**	**5936**	**6784**
8	**1695**	**3390**	**5085**	**6780**	**8475**	**10170**	**11865**	**13560**
4	**3390**	**6780**	**10170**	**13560**	**16950**	**20340**	**23730**	**27120**
2	**6780**	**13560**	**20340**	**27120**	**33900**	**40680**	**47460**	**54240**
1	**13560**	**27120**	**40680**	**54240**	**67800**	**81360**	**94920**	**108480**

Table 2.2: Relationship between bit time and bit rate. Another way to increase the bit rate significantly is the bit time reduction. If the bit time decreases the resulting bit rate increases. With this simple scheme bit rates up to 13.56 Mbit/s are possible.

Bit-Time	**Periods/Bit**	**Bit-Rate**
$[\mu s]$	[-]	[kbit/s]
9.440	**128**	**106**
4.720	**64**	**212**
2.360	**32**	**424**
1.180	**16**	**848**
0.590	**8**	**1695**
0.295	**4**	**3390**
0.147	**2**	**6780**
0.074	**1**	**13560**

2.1.4 Multi Level Amplitude Modulation

This proposal suggests to use more levels for the amplitude modulation instead of 2 level amplitude shift keying. The number of amplitude levels defines the degree of modulation. With multilevel ASK high data rates are also obtainable. But multilevel amplitude modulation is very sensitive concerning signal distortion. To illustrate the multi-level amplitude modulation a M-ASK modulated signal with the corresponding modulation index is shown in figure 2.1. Multilevel ASK also seems very critical in respect to load changes due to higher sensitivity between the amplitude levels. Another disadvantage is the deeper modulation index which causes a bigger energetic disadvantage for higher resonance frequencies.
A comparison between data rate, the number of amplitude levels and bit time is given in table 2.3.

Table 2.3: Multi level amplitude modulation. A multi level amplitude modulated signal divides the signal amplitude in equidistant amplitude levels. With this principle higher bit rates are possible. The disadvantage of this method is the influence of the amplitude fluctuations on the signal quality (higher bit error rate).

	Periods/Bit [-]							
Number of AM-Levels	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
[-]	**Corresponding Bit Rate [kbit/s]**							
1	**106**	**212**	**424**	**848**	**1696**	**3392**	**6784**	**13560**
2	**212**	**424**	**848**	**1696**	**3392**	**6784**	**13560**	**27120**
3	**318**	**636**	**1272**	**2544**	**5088**	**10176**	**20352**	**40704**
4	**424**	**848**	**1696**	**3392**	**6784**	**13560**	**27120**	**54240**

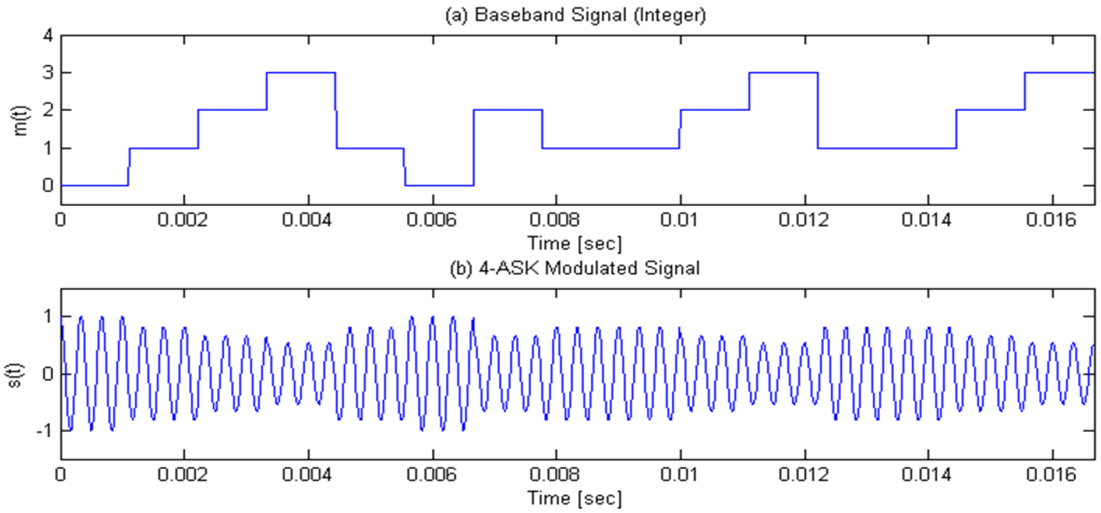


Figure 2.1: 4-ASK. An amplitude modulated signal with four amplitude subdivisions seems to be reasonable concerning detectability. There are four different amplitude values of the signal over time. Here, the baseband signal defines the modulation index at a specific point in time.

The mathematical definition of an amplitude modulated and M-ASK signal is given in Equation 2.2 and 2.3

$$s(t) = A_i \cdot \cos(2\pi f_c t), \;\; 0 \leq t \leq T \tag{2.2}$$

$$A_i = A \cdot \frac{(1 - i \cdot m)}{(1 + i \cdot m)} for\ i = 0, 1, 2, ...M - 1\ und\ M \geq 4 \tag{2.3}$$

s(t): M-ASK of the carrier
A_i: amplitude value
m: modulation index
f_c: carrier frequency
T: symbol time
M: number of amplitude levels

2.1.5 Applications

There are many RFID applications which work at the carrier frequency of 13.56 MHz with maximum distances of 10 cm between the reader and the transponder. The data transfer from the reader to the transponder is based on the modulation of the carrier, whereas in opposite direction, the load modulation is used to transfer the data from the transponder to the reader. If a lot of data has to be transferred high data rates lower the transmission time.
As well, high data rates allow an exchange of large amounts of data stored on contactless smart cards with the reader device. The achieved data rates in the proposed system are ten times faster than current solutions specified in the standard ISO/IEC 14443 [38]. These new technologies extend the area of applications, such as improved e-passport applications. The electronic passport or biometric passport stores personal data and biometric information, such as the images of the fingerprint, the face and the iris. The way data have to be stored are defined by the International Civil Aviation Organization (ICAO) [34].

2.2 System Components

Figure 2.2 shows the overall demonstration system including the reader FPGA, the reader antenna, the transponder PCB and the transponder antenna. The printed circuit board includes the integrated chip and the transponder FPGA for the emulation of the transponder digital part. With this test setup all the measurements were taken.

A detailed schematic of the transponder board layout for the test-chip I is given in figure 2.3 and for the test-chip II in figure 2.4. It includes the test and control pins, the chip socket (CLCC68), passive components and the transponder antenna. Here the transponder antenna has the typical check card size (format ID-1 [37]) with 4 windings to allow compatibility with standardized products.

2.2.1 Reader

A functional view of the entire system is given in Figure 2.5 [1]. It was developed and realized in hardware to form a demonstration system. The system was divided into three distinct parts,

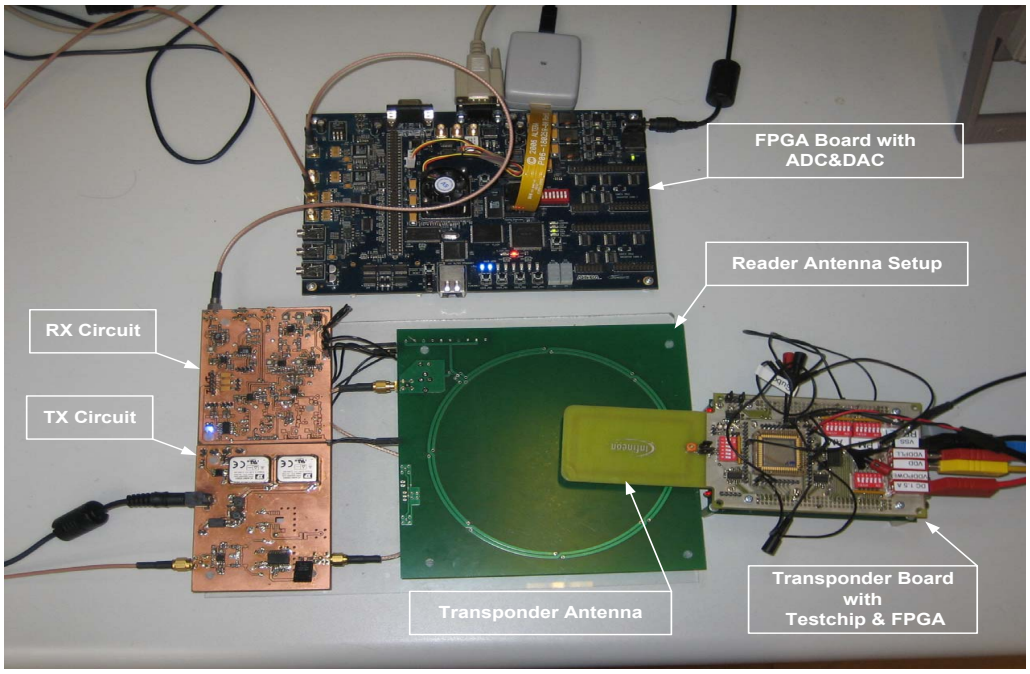


Figure 2.2: Complete RFID system. The reader FPGA is connected with the receive (RX) and transmit (TX) circuit including the reader resonance circuit. With the connection to the reader antenna the complete reader system is defined. The reader FPGA board is controlled by a PC with an ADC and DAC over RS232 interface. A USB/JTAG interface has been used to program the FPGA. To receive and process the emitted data a transponder board has been used. The transponder board includes the analog front end chip connected to the transponder antenna and a FPGA that provides the control signals for the test chip.

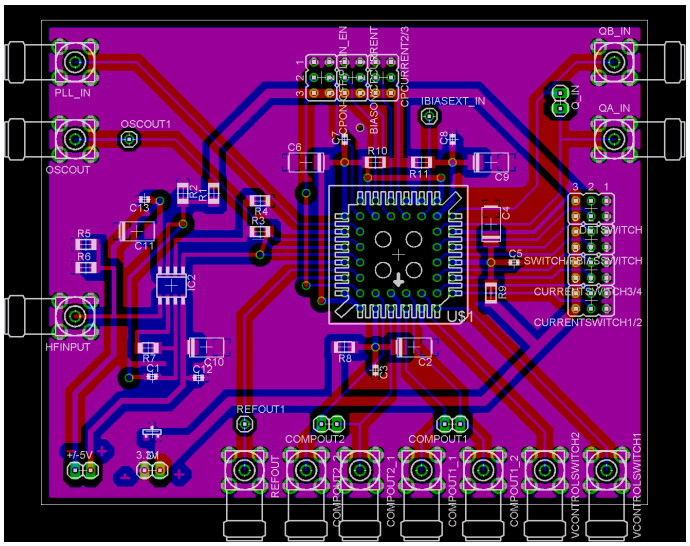


Figure 2.3: PCB layout for testchip I. PCB layout of the test board for the verification of the AFE and demodulator circuits placed on test chip I.

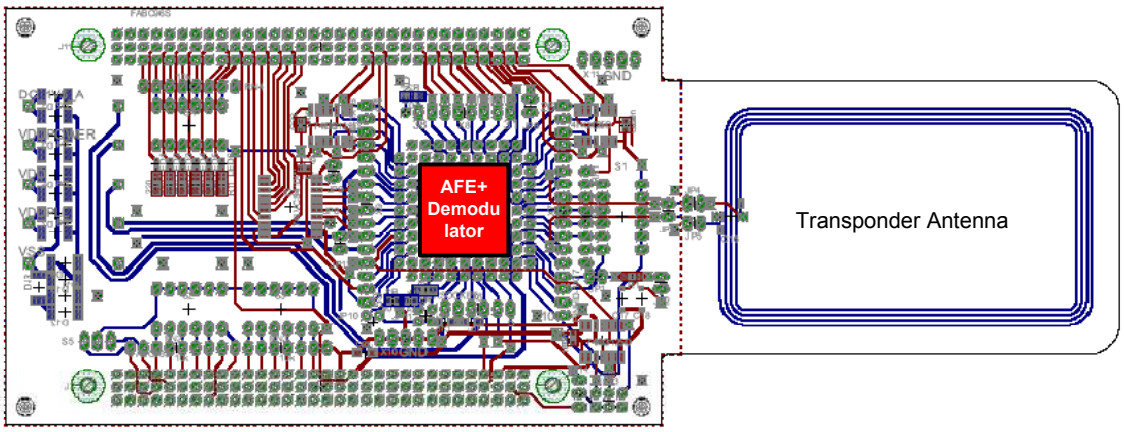


Figure 2.4: PCB layout for testchip II. To test the functionalities of the second test chip an improved test board has been created. This test board includes the possibility to dock to the transponder FPGA board, which provides the digital signals for test chip II.

the reader, the receive/transmit circuit and the passive transponder. The reader is based on a FPGA prototyping system with ADC and DAC for higher flexibility to test different modulation and coding types. The modulated reader signal is amplified by a power amplifier and is filtered by an electromagnetic compatibility filter (EMC filter). Due to inductive coupling the electromagnetic field induces a voltage in transponder antenna L2, which supplies the analog and digital part of the transponder [25].

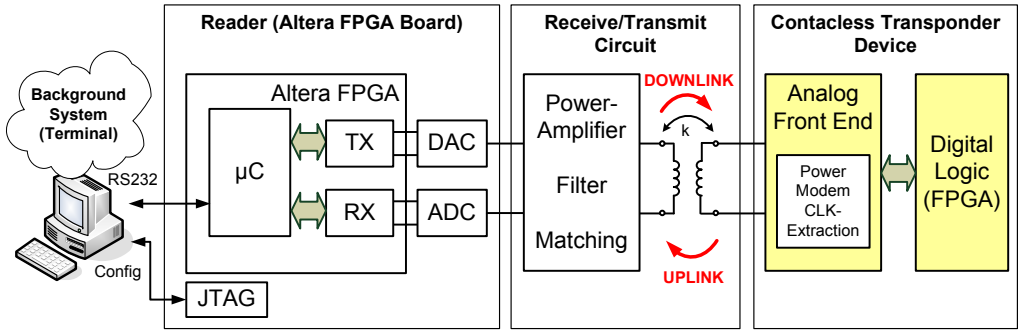


Figure 2.5: Block diagram of the complete RFID System. There are several components which are necessary to get a complete RFID system. The reader FPGA is controlled by the terminal program from the background system via RS 232 interface. For signal generation and preparation a DAC, a power amplifier, an EMC filter and a resonance circuit are used. The displayed coupling factor k represents the coupling between the reader and transponder antenna. This factor depends on the inductances of the antennas and the distance between both antennas. To complete the RFID system a transponder including the analog front end and digital part was designed and integrated into a test chip.

With the carrier energy the contactless transponder system is powered, and the data communication between reader and contactless transponder (Downlink/Uplink) device is achieved by modulation/demodulation of the carrier. Downlink denotes the communication direction from the reader to the contactless transponder device. The communication in the reverse direction is

called uplink.

2.2.2 Transponder

The transponder consists of three main blocks, the transponder antenna, the analog front end and the digital part (2.5). Here the analog front end of the transponder includes a tuning capacitor, rectifier, shunt system, modulator, clock recovery unit, voltage reference circuit, voltage regulator and phase demodulator. Most of the circuits mentioned are optimized for high bit rates. As a result the digital part interacts with the analog front end and provides the control signals. Furthermore, the clock signal is generated by the clock extraction unit for the digital block. Both areas, the analog front end and the digital part, are clocked by the recovered clock from the clock extraction unit.

2.2.3 Air Interface

2.2.3.1 Simulation Setup of the Transmission Channel

To simulate the air interface in an adequate realistic way, a simulation model for the equivalent circuit of the air interface has been used, shown in Figure 2.6.

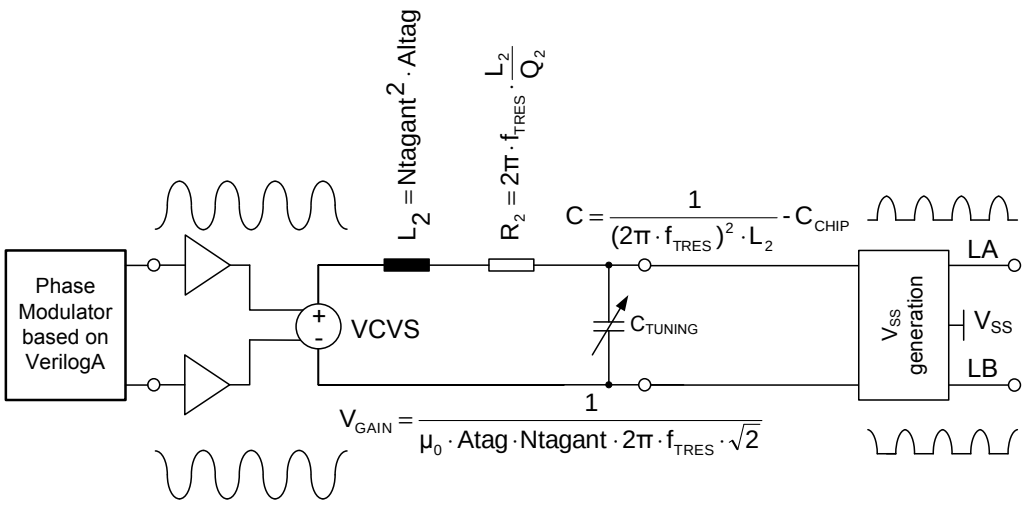


Figure 2.6: Simulation model of the air interface. In order to get adequate simulation results a simulation model for the air interface was designed. For a high flexibility to test different modulation and coding types the modulated signals were programmed in Verilog A. To allow adjustable field strengths a gain factor has been introduced. The output of this simulation model are modulated half waves which can be used for the verification of the analog front end and demodulator circuits.

The phase modulated signal is described in a VerilogA-Model, which is adjusted in amplitude by an ideal amplifier stage. The difference of both input signals is achieved via a $VCVS$ (Voltage Controlled Voltage Source). The parallel resonance circuit includes an inductance L_2, a resistor R_2, a chip capacitor C_{CHIP} and a tuning capacitor C_{TUNING}.
The quality factor depends on the resistors of the reader coil and the wire resistance. Thereby, the quality factor can be adjusted by Q_2. The V_{SS}-Generation block allocates the reference potential

V_{SS}. The displayed half waves are gained from the incoming signals by two simple crossed NMOS-switches. For a detailed consideration of the air interface and the resonance circuits on both, the reader- and transponder side, a simulation model including mutual coupling effects was introduced. In this context the primary and secondary side are marked by index 1 and 2.

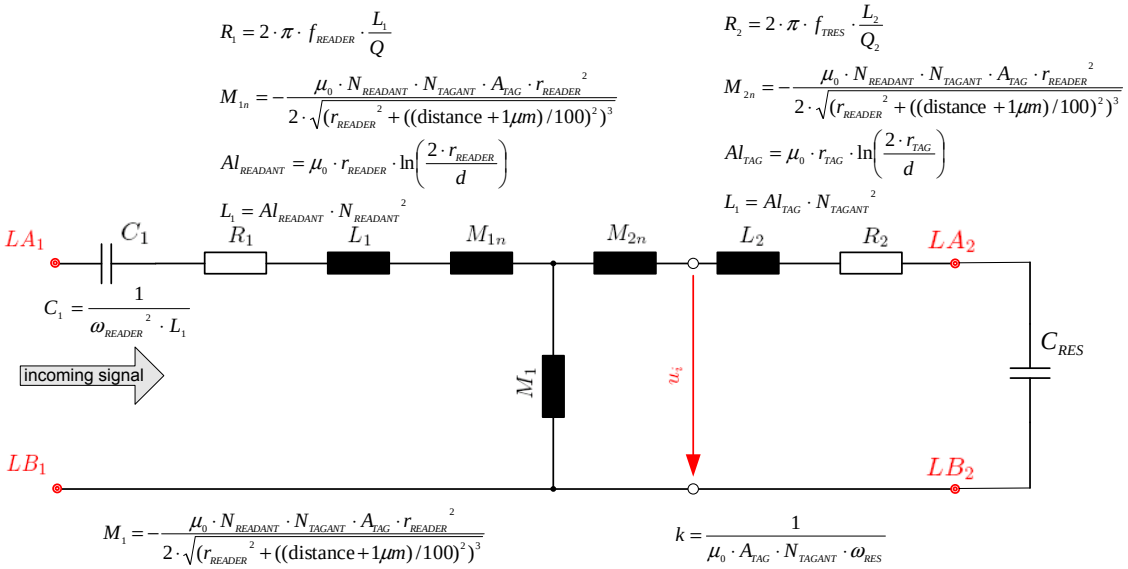


Figure 2.7: Transmission channel. For detailed air interface considerations the T equivalent circuit diagram is useful. It includes both sides, the reader and the transponder resonance circuit. With this equivalent circuit diagram it is possible to consider the mutual coupling effects. The simulation results of the model are also very similar to the measurement results of the real air interface.

μ_0 Magnetic Constant

x Distance between Reader and Transponder

r_{READER} Radius of Reader Antenna

f_{READER} Reader-Antenna Resonance Frequency

f_{TRES} Transponder-Antenna Resonance Frequency

r_{TAG} Radius of Transponder Antenna

N_1 Number of Coil-Windings of Reader Antenna

N_2 Number of Coil-Windings of Transponder Antenna

R_1 Resistor on the reader side

R_2 Resistor on the transponder side

M_{12} Mutual Inductance

A_{TAG} Area of Transponder Antenna

Al_{TAG} Geometric Factor of the Transponder Antenna Inductance

$Al_{READANT}$ Geometric Factor of the Reader Antenna Inductance

d Diameter of the wire

Q Quality Factor of the Reader Resonance Circuit

Q_2 Quality Factor of the Transponder Resonance Circuit

If the resonance circuit is tuned at the carrier frequency the quality factor can be determined by formula 2.4.

$$Q = \frac{2 \cdot \pi \cdot f_{READER} \cdot L_1}{R_1} \tag{2.4}$$

Furthermore, the mutual inductance M_{12} can be determined by formula 2.5 [25].

$$M_{12} = \frac{\mu_0 \cdot N_1 \cdot N_2 \cdot A_{TAG} \cdot R_1^2}{2 \cdot \sqrt{(r_{READER}^2 + ((distance + 1\mu m)/100)^2)^3}} \tag{2.5}$$

if $A_2 \leq A_1$.
The resonance capacitance C_1 is determined by $C_1 = \frac{1}{\omega_{READER}^2 \cdot L_1}$.
The coupling factor is given by formula 2.6 [25].

$$k = \frac{1}{\mu_0 \cdot A_{TAG} \cdot N_{TAGANT} \cdot \omega_{RES}} \tag{2.6}$$

With the simulation model in Figure 2.7 the mutual coupling effects in both directions, from transponder to reader and from reader to transponder, can be taken into account.
Figure 2.8 shows the simulation model of the phase modulated signal and the resonance circuits of transponder and reader device. To test different modulation and coding types a “VerilogA”-Model has been written.
The reader resonance circuit includes the wire resistance R_1, capacitor C_1 and inductance L_1. The parallel resonance circuit on the transponder side includes the inductance L_2, wire resistance R_2 and capacitor C_2. The resonance frequency f_{RES} and the quality factor of the reader and transponder resonance circuits are influenced by the wire and inductance resistance. This means, the smaller the resistance, the higher the quality factor for given values of L and C (See Equation 2.4).

The reader and transponder resonance circuit components are calculated by equations 2.7, 2.8, 2.9 and 2.10. Resonance frequencies f_{RES}, f_{RES2} and inductances L_1, L_2 are typically constant values. Additionally it can be seen that the quality factors Q and Q_2 depend on the capacitor values C_1 and C_2 at resonance frequency.

$$Q = \frac{2 \cdot \pi \cdot f_{RES} \cdot L_1}{R_1} \tag{2.7}$$

$$C_1 = \frac{1}{(2 \cdot \pi \cdot f_{RES})^2 \cdot L_1} \tag{2.8}$$

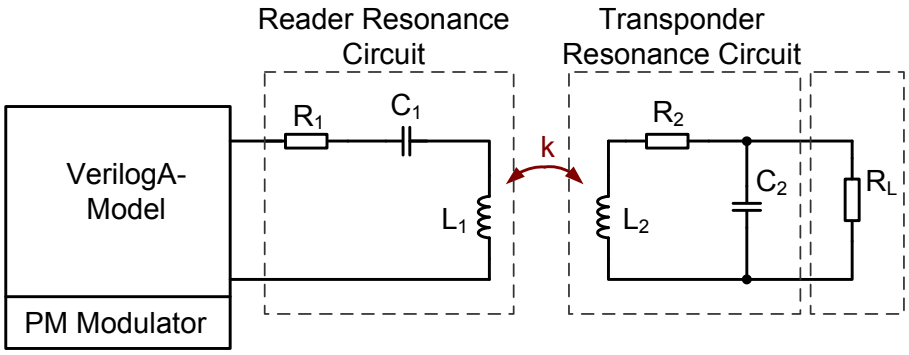


Figure 2.8: Simplified resonance circuit on the reader and the transponder-side. Generally, the air interface is divided into two sections, the reader and transponder resonance circuit. In this project the proposed system includes a series resonance circuit at the reader-side and a parallel resonance circuit at the transponder-side. Furthermore, the load impedance is split into a load capacitor and resistor. Here, the load capacitor corresponds to the input capacitance of the analog front end.

$$Q_2 = \frac{2 \cdot \pi \cdot f_{RES2} \cdot L_2}{R_2} \tag{2.9}$$

$$C_2 = \frac{1}{(2 \cdot \pi \cdot f_{RES2})^2 \cdot L_2} \tag{2.10}$$

2.2.3.2 Test Environment

The standards ETSI and FCC define the maximum field emission generated by the PCD antenna. Thereby the spectrum mask is specified by EN 300330 for RFID and EAS applications. The maximum emission permitted is $42\,dB\mu A/m = 0.126\,mA/m$ ($60\,dB\mu A/m = 1\,mA/m$ in Europe) for a carrier frequency of 13.56 MHz ($\pm\,7\,kHz$) [24].
The type and speed of data modulation define the spectrum characteristic around the carrier. If the emitted power of the reader antenna is increased the amplitude of the whole spectrum will increase. During this scenario the amplitude difference between the carrier and the side-bands remains constant. RFID readers generate and radiate an electromagnetic field. Therefore it is important that other radio services are not badly affected by this electromagnetic field. Due to this circumstance an emitted maximum HF field is specified in the standard. The emission limitation is defined in the ETSI EN 300330 [36] regulations (Figure 2.9) and the technical report ERC/REC 70-03.

In order to fulfill the emission regulation the suitable modulation and coding types have to be chosen carefully. For example, if the pulse width of the baseband data increases, the sideband amplitudes evenly decrease.
The magnetic field characteristic over reader-transponder distance can be seen in figure 2.10.

The H-field is divided into two areas, the near and the far-field. In this context the equations 2.11 and 2.12 represent the near-field approximation formula and the logarithmic version for the H-Field. In this context, the H-Field depends on the antenna current $Iantenna$, the number of windings N, the reader antenna radius r_{READER} and the distance from reader to transponder

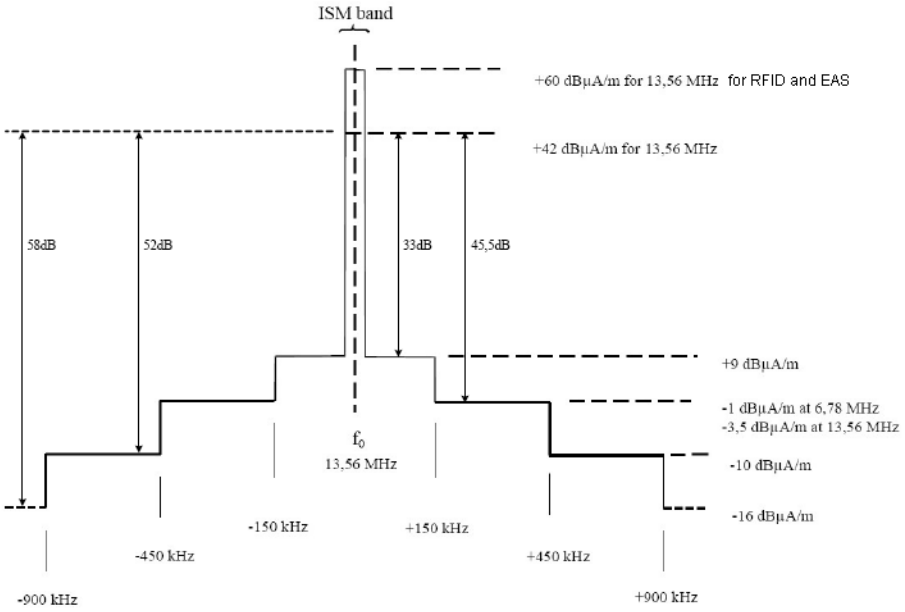


Figure 2.9: ETSI EN 300330 regulation. The maximum emission field strength is specified in the ETSI EN 300330. This standard defines a curve with a chimney characteristic, where the maximum field strengths have to be below this curve.

$distance$. It can be noticed that the decay of field strength is approximately $60\,dB$ per decade in the near field of the reader coil and flattens out to $20\,dB$ per decade in the far field.
ISO 14443 defines the magnetic field strength at 10 m distance from the reader antenna. In accordance with the standard the minimum field strength is 1.5 A/m and the maximum field strength lies at 7.5 A/m.

$$Happr(distance) = \frac{Iantenna \cdot N \cdot r_{READER}^2}{2 \cdot \sqrt{(r_{READER}^2 + distance^2)^3}} \tag{2.11}$$

$$HapprdB(distance) = 20 \cdot \log\left(\frac{Happr(distance)}{10^{-6}}\right) \tag{2.12}$$

To determine the maximum possible current through the reader antenna (d = 0 cm) Ampere's law has been used.

$$\begin{aligned} H_{d=3.521m} &= H_{d=10m} + 20 \cdot (\log(10) - \log(3.521)) && (2.13)\\ &= 60\,dB\mu A/m + 9.067\,dB\mu A/m && (2.14)\\ &= 69.067\,dB\mu A/m && (2.15) \end{aligned}$$

$$\begin{aligned} N \cdot I &= \frac{2 \cdot H_{d=3.521m} \cdot (\sqrt{(r_{READER}^2 + d^2)}^3)}{r_{READER}^2} && (2.16)\\ &= 44.11\,A && (2.17) \end{aligned}$$

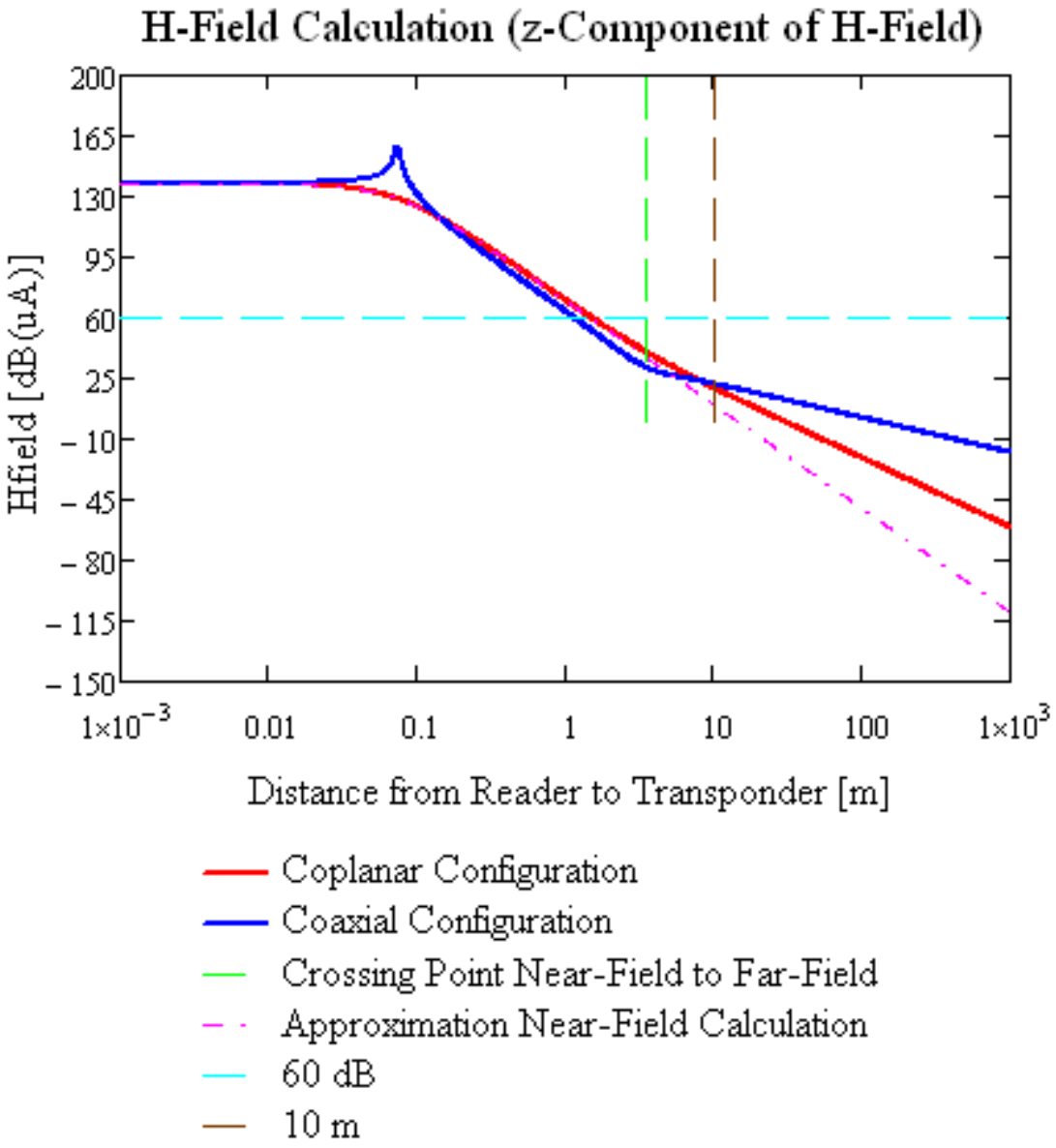


Figure 2.10: Magnetic field characteristic. The orientation of the reader antenna to the transponder antenna is very important concerning field strength considerations. Two configurations are considered, the coaxial and coplanar configuration. Coaxial means that the centers of both antenna conductors are on the same line, normal to the conductor path plane. In coplanar case, the reader and transponder antenna are in the same plane. In the near field the coplanar configuration and in the far field the coaxial configuration is dominating. Another important point is the crossing point of near field and far field, which is marked by a green dashed line.

To determine the maximum field strength at the reader antenna formula 2.18 has been used. A typical antenna radius of 0.075 m has been chosen. Based on this equation, it can be said that the maximum field strength decreases if the antenna radius also decreases. As a consequence of reducing the antenna radius the spectrum limitation matter is no longer a problem.

$$H_{d=0} = \frac{N \cdot I}{2 \cdot r_{READER}} = \frac{44.11\,A}{2 \cdot 0.075\,m} \tag{2.18}$$

$$= 294.07\,A/m \rightarrow 169.37\,dB\mu A/m \tag{2.19}$$

Based on the Biot-Savart law the magnetic field equations 2.21, 2.22, 2.23 and 2.24 are deduced for a more accurate calculation of the magnetic field.
To calculate the crossing point for near-field to far-field formula 2.20 is used. Additionally, a 10 m marker is shown in figure 2.10, which marks the definition point of the international standard.

$$x = \frac{3 \cdot 10^8}{fres \cdot 2\pi} \tag{2.20}$$

The equation 2.21 [28] represents the vector from the circle antenna center to the magnetic vector point. Thereby, xr, yr, zr define the coordinates of the magnetic vector xs, ys, zs the coordinates of the coordinate origin and β the propagation constant.

$$rsr(xr,\, yr,\, zr, \varphi) = \sqrt{(xs + a \cdot \cos(\varphi) - xr)^2 + (ys + a \cdot \sin(\varphi) - yr)^2 + (zs - zr)^2} \tag{2.21}$$

$$\beta = \frac{\lambda}{2\pi} = \frac{2\pi \cdot fres}{3 \cdot 10^8} = 0.284 \tag{2.22}$$

$$prj(xr,\, yr,\, zr) = a + (xs - xr) \cdot \cos(\phi) + (ys - yr) \cdot \sin(\phi) \tag{2.23}$$

$$Hz(xr,\, yr,\, zr) = \frac{Iantenna \cdot a \cdot \left| \int_0^{2\pi} \frac{e^{-i \cdot \beta \cdot rsr(xr,\, yr,\, zr, \varphi)}}{rsr(xr, yr, zr, \varphi)^2} \cdot i \cdot \beta + \frac{1}{rsr(xr, yr, zr, \varphi)} \cdot prj(xr,\, yr,\, zr)\, d\phi \right|}{4 \cdot \pi} \tag{2.24}$$

The magnetic field is specified in $\left[\frac{dB}{\mu A}\right]$ by the international standard EN 300330. To convert the results of equation 2.24 into the standardized unit the equation 2.25 is used.

$$HzdB(xr,\, yr,\, zr) = 20 \cdot \log\left(\frac{Hz(xr,\, yr,\, zr)}{10^{-6}}\right) \tag{2.25}$$

In order to determine the magnetic field strength at the reader antenna HzdB (0, 0, 0.001) has to be calculated. With the described equations above the magnetic field strength can be calculated at different distances from the reader antenna.

For maximum field strength calculation figure 2.11 has been used. Thus the field characteristics are shown of the far and near field and the transition region between these two field regions. To simulate the worst-case scenario the near field calculation is based on the coplanar configuration and the far field calculation is based on the coaxial configuration. The maximum field strength allowed is $60\,dB\mu A$ at a distance of 10 m [25]. From this point onwards the field strength at the reader antenna is determined. In the underlying example two antenna forms were tested, a circular and a rectangular antenna with the same antenna area. The difference between the two field strength curves is not significant.

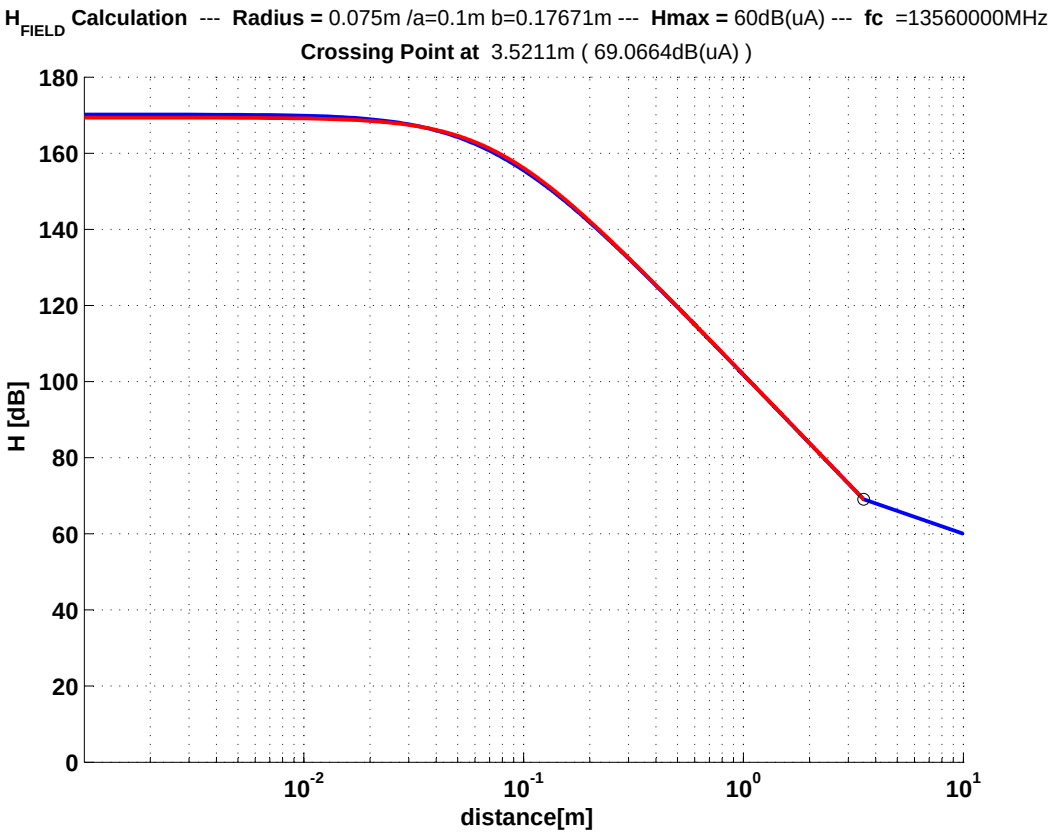


Figure 2.11: Maximum allowed field strength. To determine the maximum allowable field strength at the reader antenna the field strength at 10 m is calculated backwards to the reader antenna.

The underlying test setup is shown in figure 2.12. It consists of the background system (personal computer with terminal program), the measurement setup, the reader FPGA and the transponder PCB with the analog front end chip. In the background, four measurement signals of the phase demodulator can be seen on the screen. The first signal shows the transmitted data and the second and third measurement signals represent the extracted data signal of phase detector 1 and phase detector 2. And the last trace shows the phase deviation of the phase modulated input signal over time. The measurement results and the test setup are described in more in detail in chapter 5. Furthermore, to test the maximum operation range the ISO measurement tower has been used for the test setup [35]. The maximum operating range of the test chip at a bit rate of 13.56 Mbit/s is about 4 cm.

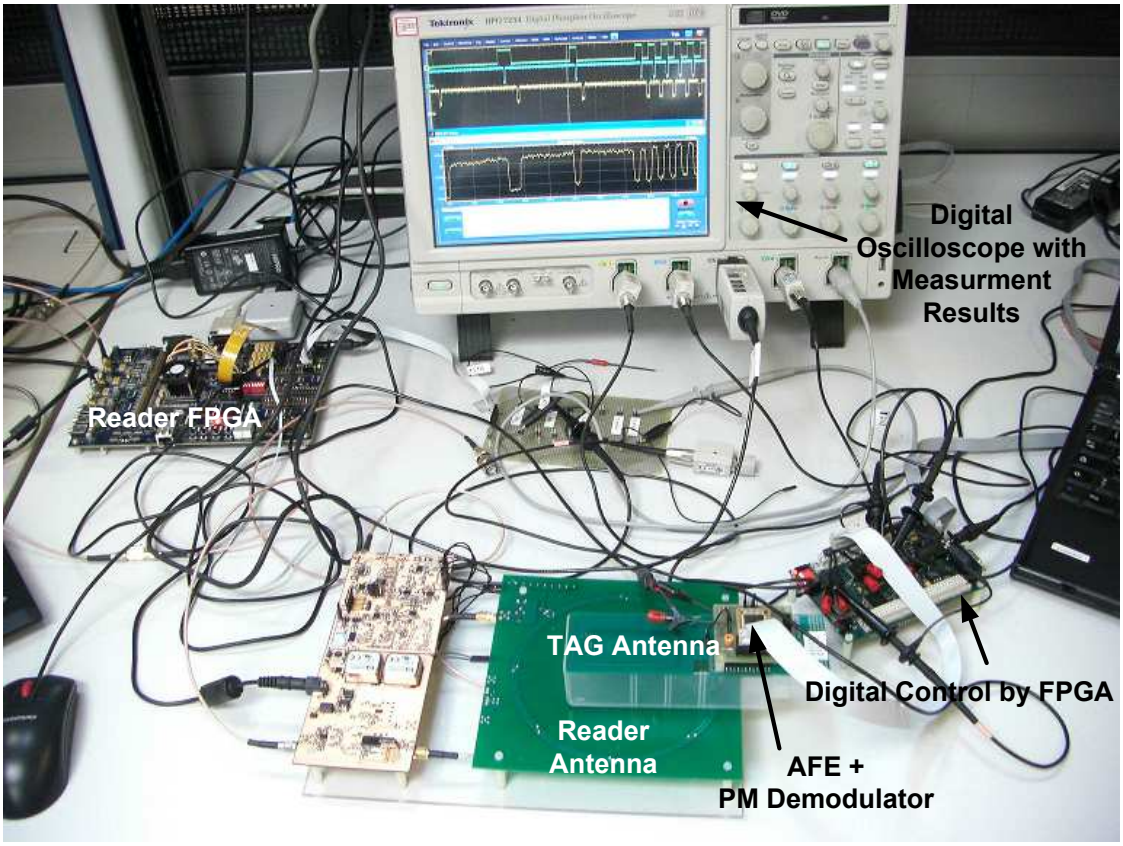


Figure 2.12: Test setup. For chip verification a compact test setup is important to test the functionality of the analog front end and the digital part. All the designed components are optimized in terms of high bit rates.

2.3 Summary

The introduction gives a short overview of the standardization activities and the field of RFID applications. In addition, different modulation types are discussed. A block diagram is presented, which shows the main RFID system components: the reader, the transponder and the transmission channel. A simulation model of the air interface is also shown and discussed in detail.

3 Data Rate - Important Issues

3.1 Modulation Methods for High Data Rates

Three different modulation methods and the combination of these methods are described for passive transponder applications:

- Amplitude Modulation (AM, ASK)
- Phase Modulation (PM, PSK, PJM)
- Frequency Modulation (FM, FSK)

3.1.1 Amplitude Modulation (AM, ASK)

In case of amplitude modulation the data transfer is made via amplitude variations of the carrier signal. The main benefit of amplitude modulation is the low complexity of the modulator and demodulator circuits. Two types of amplitude modulation are possible. First, the amplitude modulation with a $8\% - 14\%$ [38] modulation index[1]. Second, the ASK modulation with a modulation index of $100\,\%$. A general formula of the ASK modulation is given in equation 3.1.

$$s(t) = A \cdot m(t) \cdot \cos(2\pi f_c t) \tag{3.1}$$

The character A specifies the amplitude of the carrier signal and f_c stands for the carrier frequency. The baseband data stream is represented by the bit sequence $m(t)$. For the ASK modulation this sequence consists of binary 0 or 1.
Amplitude shift keying with a modulation index of $100\,\%$ has the great disadvantage of gaps in energy transfer (field gaps).
For high data rates it is necessary to send the data stream with a high modulation index (modulation index up to 16%). A high modulation index implies the benefit that the demodulation is much easier on the transponder-side.
In case of multilevel amplitude modulation the carrier is divided into a number of voltage levels. When considering the average power, the FSK performance is the same as for ASK. But when we look at the peak power at FSK, this modulation type has a 3 dB advantage compared to ASK. The problems with ASK-RFID systems are caused inter alia by the dynamic and the quality factor. The dynamic occurs if the user moves the transponder. By moving the transponder the amplitude and the modulation index vary depending on the distance between the reader and the transponder. This movement causes a significantly change in amplitude of the magnetic field that reaches the transponder coil. That in turn influences the modulated amplitude shift which in turn increases the detection complexity. For this reason, the AC shunt (limiter) of the transponder

[1] The modulation index m is defined as $\frac{A-B}{A+B}$ where A and B are the peak and minimum signal amplitude respectively. The value of the index may be expressed as a percentage.

is needed to limit the supply voltage to a defined voltage value. But the limiter causes another problem for the amplitude demodulation process. The limitation of the HF input signal partly eliminates the modulated amplitude shifts. Due to these problems the phase modulation was chosen for data communication from reader to transponder for high data rates.
This fact has to be also taken into account in developing the amplitude demodulator and it also increase the complexity of the circuit design. Due to the quality factor of the antenna resonance circuit there is a settling process caused by an amplitude change. This settling behavior is a big problem for the demodulation. Another problem is caused by the voltage limiter, which limits the voltage at the input and distorts the incoming signal of the amplitude demodulator.

3.1.2 Phase Modulation (PM, PSK, PJM)

There are three types of well-known phase modulation, namely the analog phase modulation, the phase shift keying and the phase jitter modulation technique. In the proposed system a phase jitter modulation technique [55, 56, 78, 60] is used for data transmission from reader to transponder. The concept proposed here uses only a small area in the constellation diagram for phase changes. The maximum value of the phase jump follows from the fact that there are reader field emission limitations which are defined in the international standard. Additional information on this issue and $\Delta\varphi$ limitation is available in the paper “Design and development of a mixed signal prototyping system to achieve very high data rates for contactless applications” [1].
One common way to illustrate the modulation techniques is the constellation diagram. To give an example, some phase states are shown in the constellation diagram in figure 3.1. In this example maximum phase changes of ± 15 degrees are assumed. The minimum distance from one phase state to a neighboring phase state is 5 degrees. It might be possible, of course, to reduce the distance, but by doing this, the SNR has to be increased significantly.

In table 3.1 the relationship between the phase jump value and the corresponding time shift and frequency deviation value is shown. These values are based on a carrier frequency of 13.56 MHz.

Table 3.1: Phase jump value compared with the corresponding time shift Δt and the frequency shift Δf

phase jump [°]	Δt **[ps]**	Δf **[kHz]**
1	**205**	**37.7**
2	**410**	**75.3**
3	**615**	**113.0**
4	**819**	**150.7**
5	**1024**	**188.3**
...	**...**	**...**
15	**3073**	**565.0**

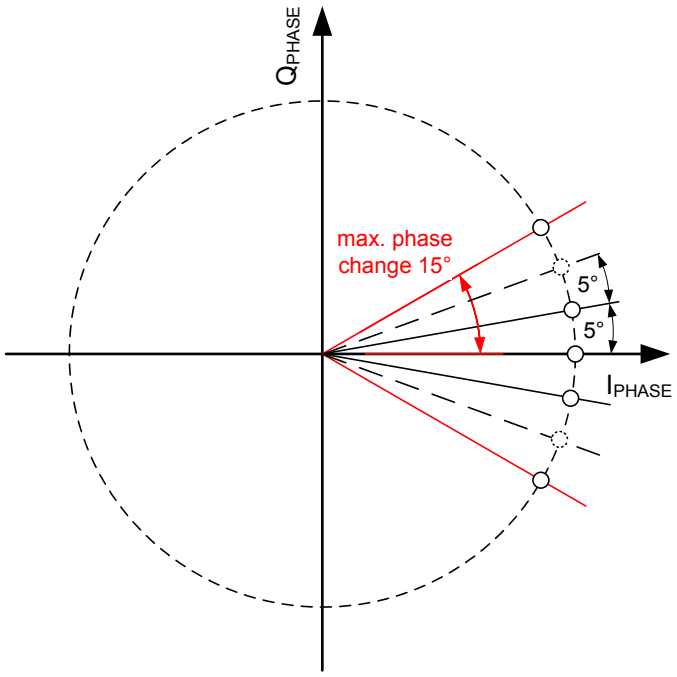


Figure 3.1: Constellation diagram - phase jitter modulation. With the phase jitter modulation method the phase deviations of the modulated signal are relatively small. Due to this fact, it is possible to have a larger number of phase states without causing a violation of the emission regulation.

In Figure 3.2 a phase modulated bit with phase changes from one to 40 degrees is given. The phase deviation over time for each phase modulated bit is shown in this figure. If the phase jump value increases the phase change requires more time to settle to the final value.

In figure 3.3 the phase settling behavior are simulated depending on the quality factor and the crossing point with different phase resolutions are illustrated. The rise and fall phase characteristic can be described by equations 3.2 and 3.2 (f_c=carrier frequency, Φ=phase jump value).

$$\varphi_{RISE} = \Phi - \Phi \cdot e^{-t \cdot \frac{f_c \cdot \pi}{Q}} \tag{3.2}$$

$$\varphi_{FALL} = \Phi \cdot e^{-t \cdot \frac{f_c \cdot \pi}{Q}} \tag{3.3}$$

With the help of the equations 3.2 and 3.3 the number of periods per_{FALL} can be determined until a defined phase value φ_1 is reached (equation 3.4).

$$per_{FALL} = \frac{-\ln\left(\frac{\varphi_1}{\Phi}\right) \cdot Q}{\pi} \tag{3.4}$$

Another important relationship exists between the quality factor of the reader resonance circuit and the required settling periods after a phase change. A linear behavior between the quality factor and the required periods for settling can be noticed in Figure 3.4.
The settling time of a $30°$ phase jump is determined for a phase detector resolution of $20°$, $22.5°$, $25°$ and $27.5°$.

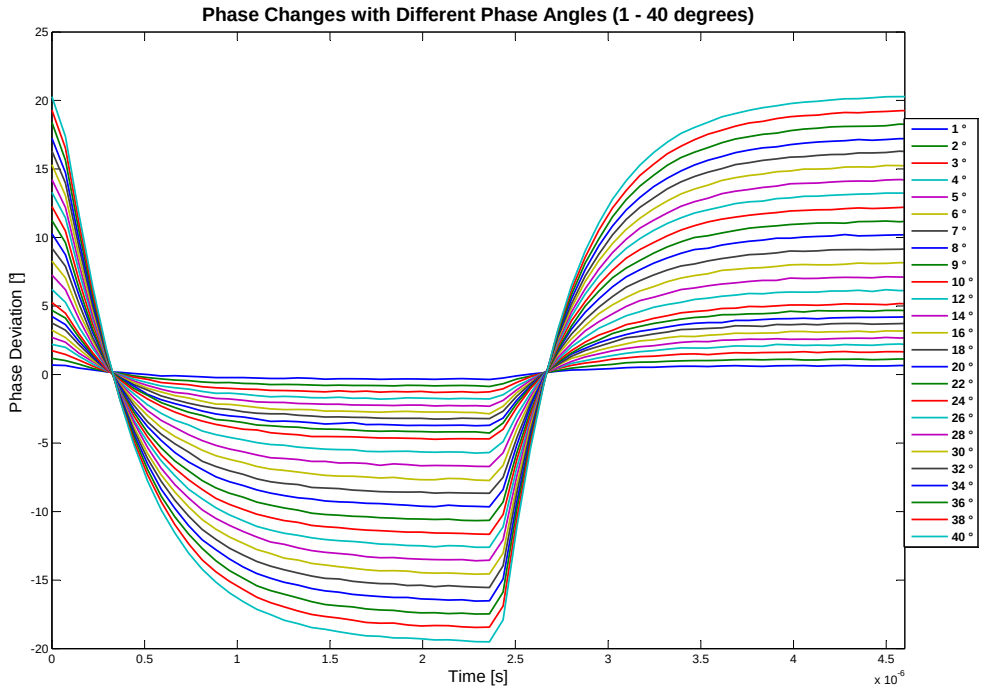


Figure 3.2: Phase changes with different phase angles for 1 - 40 degrees (measurement results). The length of the transient phase transition depends on the quality factor of the reader resonance circuit and the value of the phase change. If the phase change value increases, the settling time becomes larger. The settling time also becomes larger if the quality factor is increased.

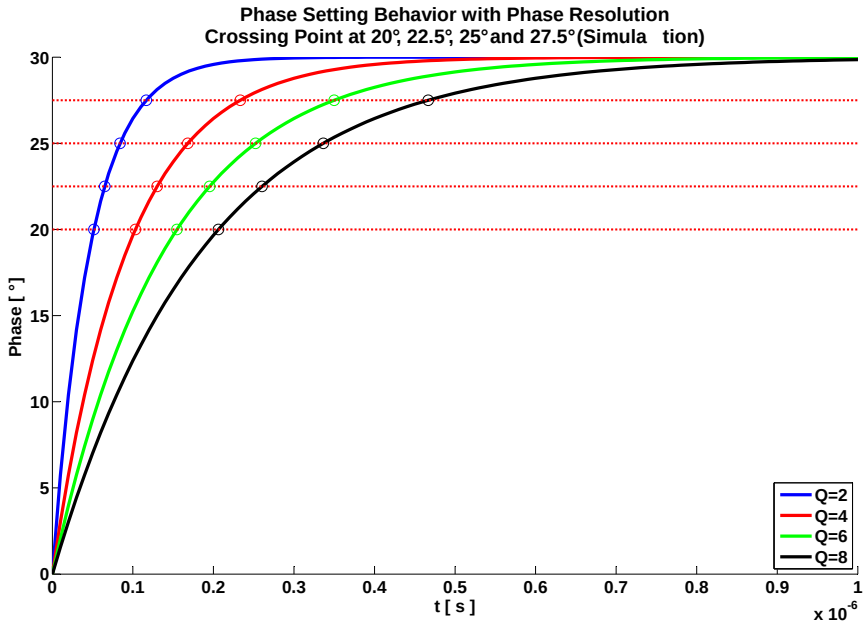


Figure 3.3: Phase settling behavior. After a phase jump of 30 degrees the number of periods for phase settling increases in a linear way if the quality factor is increased in a linear way.

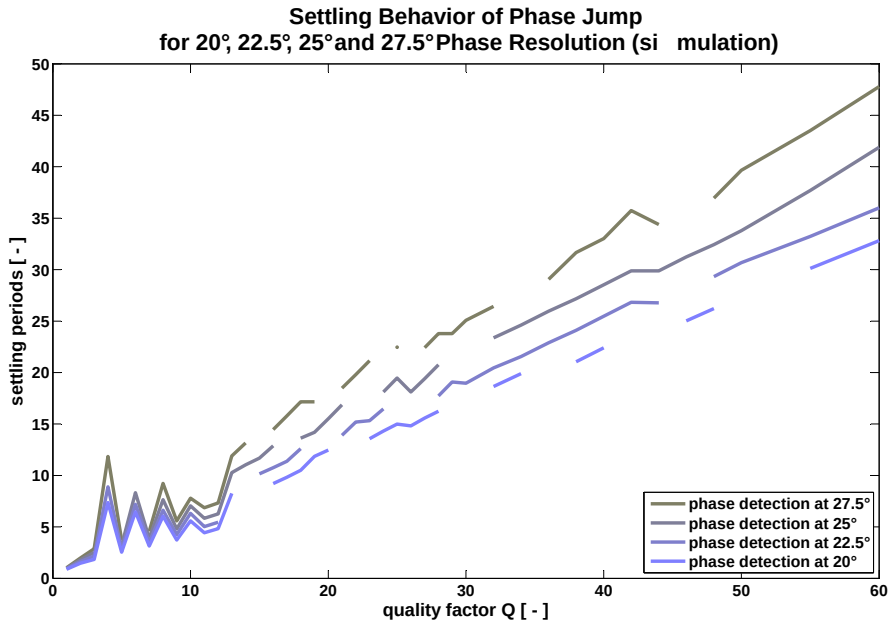


Figure 3.4: Settling behavior of a $30°$ phase jump for $20°$, $22.5°$, $25°$ and $27.5°$ phase detection level. If the quality factor of the reader resonance circuit increases in a linear way the number of periods for phase settling also increases.

Relationship between an ideal input signal and a phase modulated input signal distorted by a resonance circuit

One simulated phase modulated input stream is given in figure 3.5. The figure shows the phase deviation of an ideal phase modulated input signal and three curves, which show the settling behavior due to a resonance circuit with a quality factor of two.
The three curves show the period, frequency and phase deviation of the phase modulated signal. In this example phase deviations of about 22.5 and 45 degrees are used.

This method of data modulation is also an angle modulation as FSK, except for the fact that only one frequency is used, and the shift between 1's and 0's is accomplished by shifting the phase of the clock by 180 degrees. Two common types of PSK are:

- phase change at any '0', or
- phase change at any data change $(0 \rightarrow 1\, or\, 1 \rightarrow 0)$.

PSK provides fairly good noise immunity, a moderately simple design, and a faster data rate than FSK. In terms of bit error rate, PSK has an advantage over FSK and ASK with equal signal amplitudes levels and has a higher power transmission efficiency via the inductive link. But the carrier recovery effort is higher and requires more chip area.

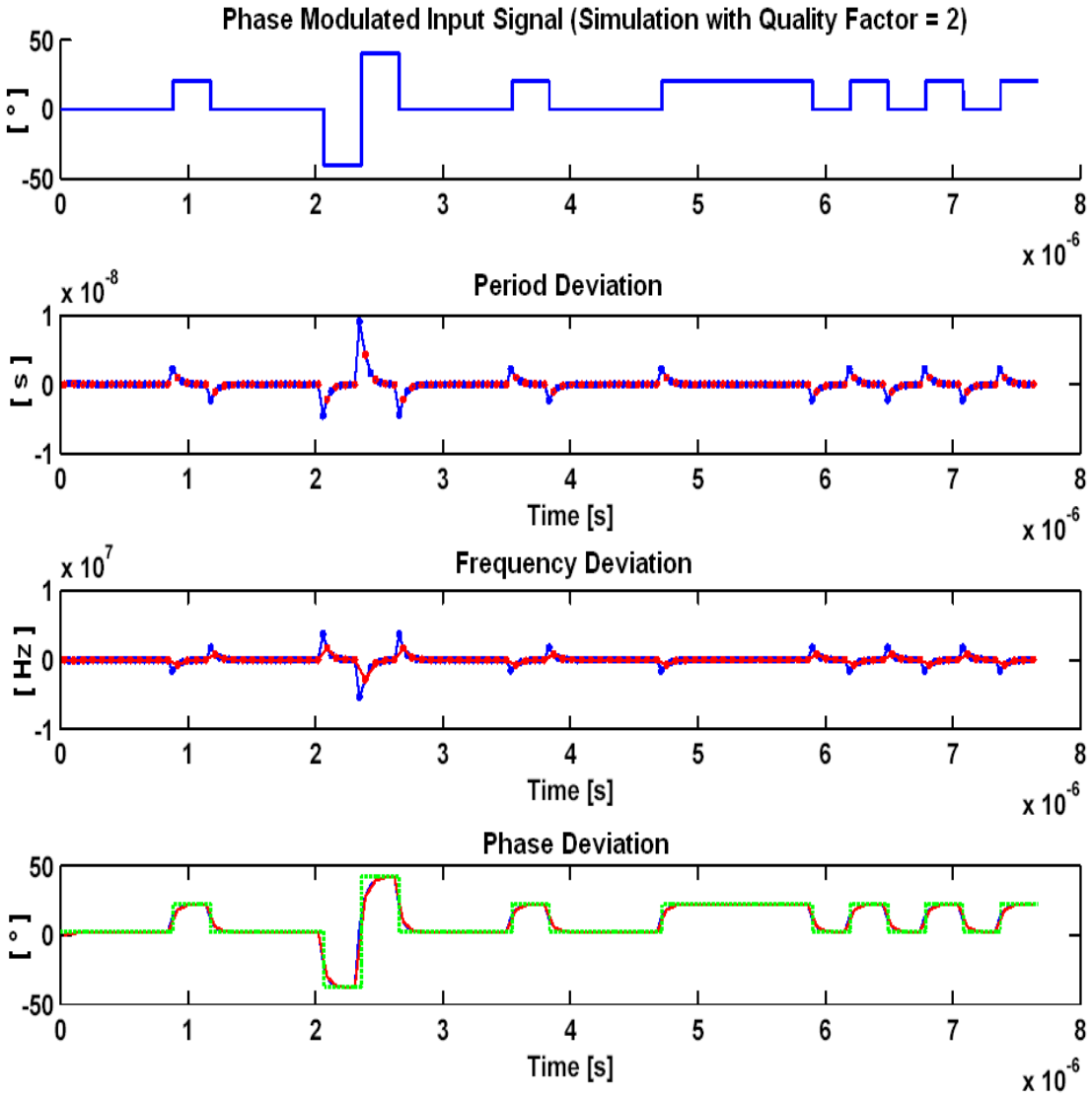


Figure 3.5: Simulated phase modulated input signal. Drawing the phase/frequency deviation of a phase modulated signal is one way to illustrate the phase information of a phase modulated signal. By regarding the phase/frequency deviation view the phase/frequency settling can be easily illustrated. Another interesting view is the period deviation, which expresses implicitly how long it takes to get the final phase value. For instance, a phase change of one degree equals a phase deviation of $205\,ps$ in time scale and $37.7\,kHz$ in frequency.

3.1.3 Frequency Modulation (FM, FSK)

Frequency modulation is the third possible modulation method to send the data stream from reader to transponder. Frequency shift keying (FSK) operates with two different frequencies. The distance between these two frequencies has to be as low as possible due to spectrum regulation (± 7 kHz). It is not easy to send and demodulate an FSK modulated signal with this limitation. Another disadvantage of FSK compared to PSK is the poor bandwidth efficiency. If the transmission bandwidth decreases the maximum amount of transferred power is lowered. FSK is mainly used in communication systems where the focus is put on reducing signal fading.

3.1.4 Combination of Different Modulation Methods

For a further bit rate increase a combination of these modulation types and a simultaneous bit time reduction are the next meaningful steps. The combination of the modulation types allows bit rates above 13.56 Mbit/s. But there is a trade-off between higher modulation orders and the bit error rate. Besides it is a fact, that the existing SNR defines the meaningful order of modulation. A detailed discussion of these topics can be found in chapter 5.

3.2 Coding Types

It is well known in signal theory that there are several coding types available for different applications, such as the unipolar NRZ code, the bipolar NRZ code, the unipolar RZ code, the bipolar RZ code, the AMI code, the Manchester code, differential Manchester code, Miller code and Modified Miller code [25, 38, 39]. When choosing the most suitable coding type there are three important points that have to be taken into account, namely the signal spectrum, the susceptibility to interference (transmission errors) and power supply interruptions.
In our project the focus of our attention was on the unipolar NRZ-Code for the downlink, because this coding type is the simplest one and requires less bandwidth than others. Less bandwidth results from the fact that the pulse width is low and a $0 \rightarrow 1$ change occurs only after a bit time. Additionally, a higher bit rate can be achieved with a low bandwidth. The drawbacks of the NRZ-Code are the existing DC-part and the fact that there is no clock regeneration possible after long periods of ones and zeros at amplitude modulation. However, the drawback of long periods of ones and zeros can be compensated by using the phase modulation technique. With the help of the phase modulation technique a constant amplitude can be reached.

3.3 Quality of the Transmitted Data (Q-Factor - Reader Antenna Resonance Circuit)

If a good quality of the transferred data shall be achieved, the quality factor of the reader resonance circuit plays an important role. In other words, the quality factor has to be low enough to guarantee that the phase jump achieves its final value. If the final value is not achieved ISI (intersymbol interference) results. Due to ISI the data extraction is much more difficult. Figure 3.6 shows the distortion of a phase change of the transmitted data bit on the reader side. The rise and fall behavior of the phase of the transmitted bit looks like a charge and discharge curve of the capacitor. It can be observed that a low quality factor of the reader resonance circuit leads

to low rise and fall times of the phase change.
Table 3.2 shows the relationship between the quality factor for a specific baud rate, the required minimum bandwidth and the bit time etu (elementary time unit). The minimum required quality factor can be calculated by $Q_{MIN} \approx \frac{13.56\,MHz}{2 \cdot baudrate}$.

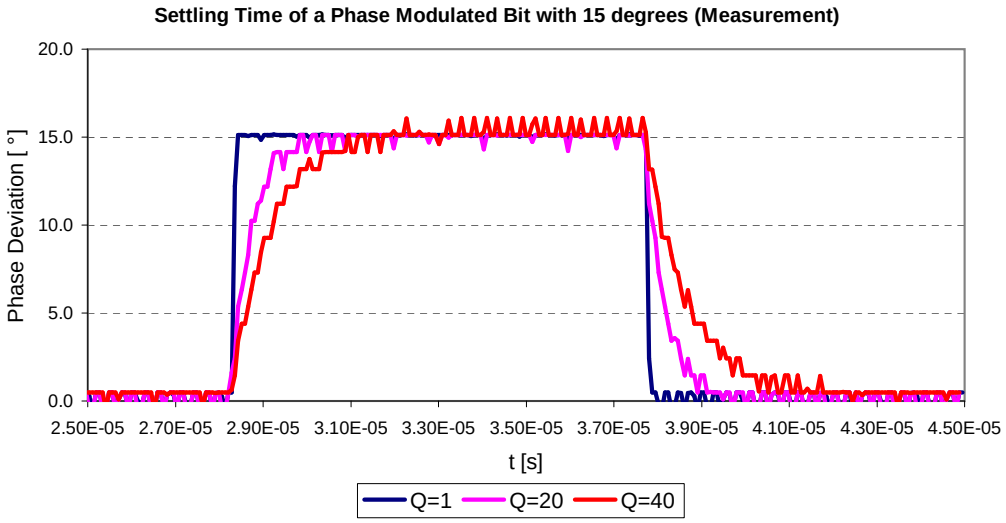


Figure 3.6: Sent data depending on different quality factors. As already mentioned the settling time of a phase modulated bit or bit stream depends on the quality factor of the reader resonance circuit. A low quality factor of one allows a low settling time, but requires a high bandwidth. On the other hand a quality factor of 40 requires much less bandwidth.

Table 3.2: Minimum quality factor.

Minimum Quality Factor			
etu	**data rate [kbit/s]**	BW_{MIN} **[Hz]**	Q_{MIN} **[Hz]**
128/fc	**106**	**212**	**64**
64/fc	**212**	**424**	**32**
32/fc	**424**	**848**	**16**
16/fc	**848**	**1700**	**8**
8/fc	**1700**	**3400**	**4**
4/fc	**3400**	**6800**	**2**
2/fc	**6800**	**13560**	**1**

3.4 Transponder Resonance Frequency Influence on the Reader (Q-Factor - Transponder Antenna Resonance Circuit)

In order to avoid distorting the quality of the incoming data on the transponder side, there should be the least possible influence of the transponder on the reader. In this context the magnetic moment of the transponder antenna $M = N \cdot A_{ANTENNA} \cdot I_{ANTENNA}$ [28] must be kept low. In this equation there are two tunable parameters - current through antenna $I_{ANTENNA}$ and number of antenna windings N. Low current through the antenna can be achieved by limiting the input voltage via the AC-Shunt. The number of windings is the second parameter which has to be kept small. On the other hand high energy transfer requires a high quality factor of the resonance circuit. The quality factor of the transponder Q_2 is given in equations 3.5 [28] and 3.6, where R_{SUM} represents the transponder total resistance and f_0 the center frequency. Q is defined as the ratio of energy stored to energy dissipated or as the ratio of the operation center frequency to the $3\,dB$ bandwidth [25, 44].

$$Q_2(N) = \frac{R_{SUM}(N)}{\omega \cdot L_2(N)} \tag{3.5}$$

$$Q = \frac{f_0}{\Delta f_{3dB}} \tag{3.6}$$

To maximize the quality factor Q there are three possible ways: reduce the resístance, increase the reactance or both. Figure 3.7 shows the quality factor and the number of windings of the transponder antenna.

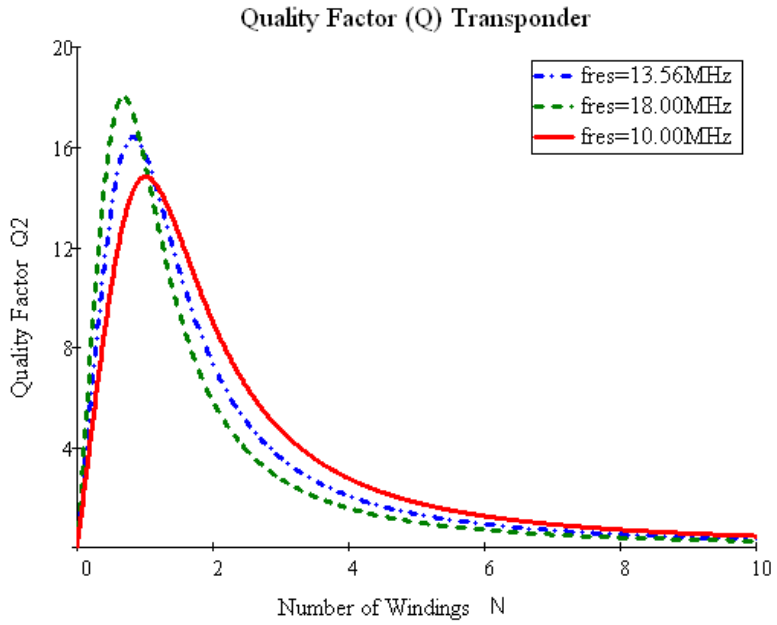


Figure 3.7: Quality factor vs. number of windings. The optimal number of windings depends on the current quality factor of the transponder resonance circuit and the resonance frequency used.

To achieve a good trade-off between high data quality and high energy transfer a quality factor of the resonance circuit of 4 has been chosen.

3.5 Bit Time Reduction

An efficient method to increase the bit rate from reader to transponder significantly is bit time reduction. Bit rates of $\frac{fc}{128}$ (106 kbit/s), $\frac{fc}{64}$ (212 kbit/s), $\frac{fc}{32}$ (424 kbit/s), $\frac{fc}{16}$ (848 kbit/s) are defined in the standard ISO/IEC 14443-2. The standardized bit stream is transferred by the use of ASK modulation with a modulation index between 8 and 14 percent.
But the bit time reduction method also can be applied to the phase modulation technique. The general relation between the bit time and bit rate is shown in table 2.2. In the proposed phase modulation principle up to one period/bit are used, which equals a data rate of about 13.56 Mbit/s. In the opposite direction, from transponder to reader, load modulation with a sub-carrier of 6.78 MHz has been used to achieve a data rate of 6.78 Mbit/s, which also equals to a bit time reduction to one period of the subcarrier per bit.
It is essential for higher transmission rates to tune the transponder resonance frequency at carrier frequency while the input voltage is limited to a low input voltage level by the AC-Shunt. Due to the tuned antenna system the quality factor reaches a high value. The high quality factor and the limited input voltage cause a high current flow through the AC-Shunt.

3.6 Summary

Chapter 3 *Data Rate - Important Issues* gives a comparison between the modulation types and shows the possibility to combine different modulation methods. Furthermore, the quality of the transmitted data is discussed and the influence of the transponder resonance frequency to the reader-side is considered. The coding types which are used for the standard and the proposed system are also discussed. One way to increase the bit rate significantly is the bit time reduction method, which is also presented here. It has the advantage that it is relatively simple and can be implemented easily. But the disadvantage is that a high quality factor of the reader antenna resonance circuit causes intersymbol interference at low bit times. This fact results in a difficult extraction of the data.

4 Analog Front-End Design

4.1 System Overview (Components, Block Diagram)

The core of the thesis is the transponder with the analog front end. Figure 4.1 shows the block diagram of the contactless transponder device. The transponder contains an analog front end (AFE) and a digital part including an antenna and a matching circuit, a clock recovery, AC shunt, a full wave rectifier, a modulator/demodulator and circuits to provide a constant supply voltage (voltage regulator). The AFE is coupled to a transponder antenna by the connectors LA and LB. Transponder antenna and tuning capacitance C_{TUNE} build a resonant circuit, which extracts the energy from the electromagnetic field. The clock recovery circuit extracts the 13.56 MHz carrier clock from the incoming high frequency field. This recovered clock is used by the digital part and the demodulator.

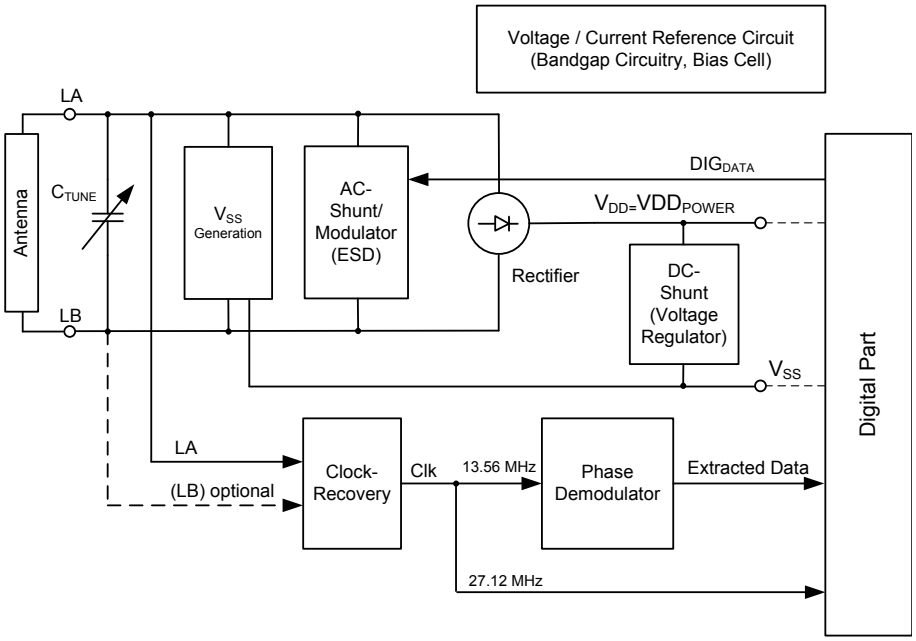
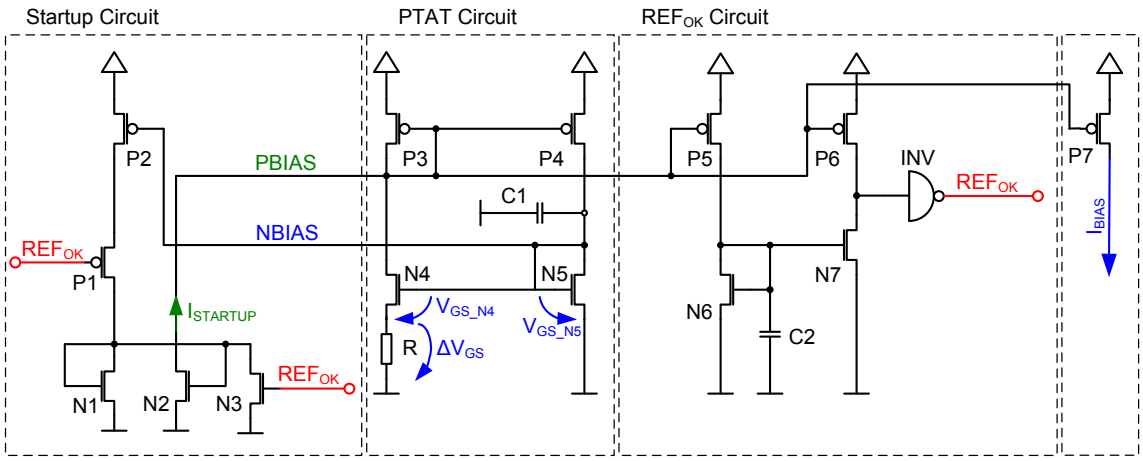


Figure 4.1: Block diagram of analog front end. The analog front end consists of the analog and digital part. Thus the analog part supplies the digital part and interacts with it.

There are several types of rectifiers which can be used on the transponder-side. Two of those types are the half wave rectifier and the full wave bridge rectifier. In the current transponder system a rectifier is used with a gate-voltage control. The induced voltage is used as input voltage of the rectifier. All modules are supplied by the DC output voltage of the rectifier.
The functionality of AC shunt [17] equals a protection structure and limits the current through the rectifier and the modulator. Additionally, it has to be guaranteed that the AC shunt does its

job properly at field strengths between 1.5 A/m and 7.5 A/m. These values are specified in the standard ISO/IEC 14443.
With the DC shunt the voltage supply of the digital logic is regulated to a constant value. Furthermore the DC shunt controls the AC shunt. When it shunts more than the defined upper limit it ramps up the AC shunt. If the current through DC shunt reaches the defined bottom limit it ramps down the AC shunt.
The uplink is realized by a load modulation of the carrier, the magnetic field is attenuated by the contactless transponder device depending on the digital signal DIG_{DATA}. Therefore the impedance of the resonant circuit is modified by the modulator. The effect of load modulation can be seen in the electromagnetic field and can be detected by the reader.

In addition, a PTAT reference circuit [5, 66] provides a constant voltage reference to control the power regulation and bias currents/voltages for the chip (figure 4.2). In contrast to the conventional bandgap circuit [18] the power consumption of the PTAT circuit is much lower. The bias cell consists of the startup, the PTAT and the REF_{OK} circuit. The startup circuit is only activated if the REF_{OK} signal is set to $zero$.



N1, N2= 1µm/3µm
N3= 1µm/0.4µm
N4= 16µm/4µm
N5= 4µm/4µm
N6= 0.2µm/5µm
N7= 3µm/0.4µm

P1= 1µm/0.4µm
P2= 1µm/8µm
P3= 5µm/7µm
P4, P5= 5µm/7µm
P6, P7= 1µm/7µm

C1= 3pF
C2= 4pF
R= 100kΩ

$I_{BIAS} \cong$ 600nA

Figure 4.2: Bias cell. It is important to have a constant current source where the power supply fluctuations don't affect the output current. Therefore a bias cell is needed. In the proposed analog front end the PTAT cell is used for the circuits which do not have high demands on the current constancy. For all other circuits which need a constant current a bandgap circuit has been introduced.

Reference current I_{BIAS} of the PTAT cell in Figure 4.2 is determined by equation 4.1.

$$I_{BIAS} = \frac{\Delta V_{GS}}{R} = V_{GS\_N4} - V_{GS\_N5} \tag{4.1}$$

Both transistors N_4 and N_5 operate in a weak inversion region to get a linear relationship between the output current and ΔV_{GS}. This circuit operates with a low supply voltage. Additionally,

a high swing cascode is introduced to increase the power supply rejection ratio. The simulation of the signals $NBIAS$, $PBIAS$, REF_{OK}, V_{DD}, I_{BIAS} and $I_{STARTUP}$ for current reference circuit is shown in Figure 4.3. The supply voltage V_{DD} ramps up to 1.5 V. At the same time, the voltages $NBIAS$ and $PBIAS$ settle to a desired value and current flows from transistor P5 and P6 to the n-channel transistors N6 and N7. If the gate-source voltage of transistor N6 reaches the threshold voltage of transistor N7 the node voltage at REF_{OK} goes up. The REF_{OK} turns the startup circuit off and the bias circuit is not charged anymore by the startup current $I_{STARTUP}$.

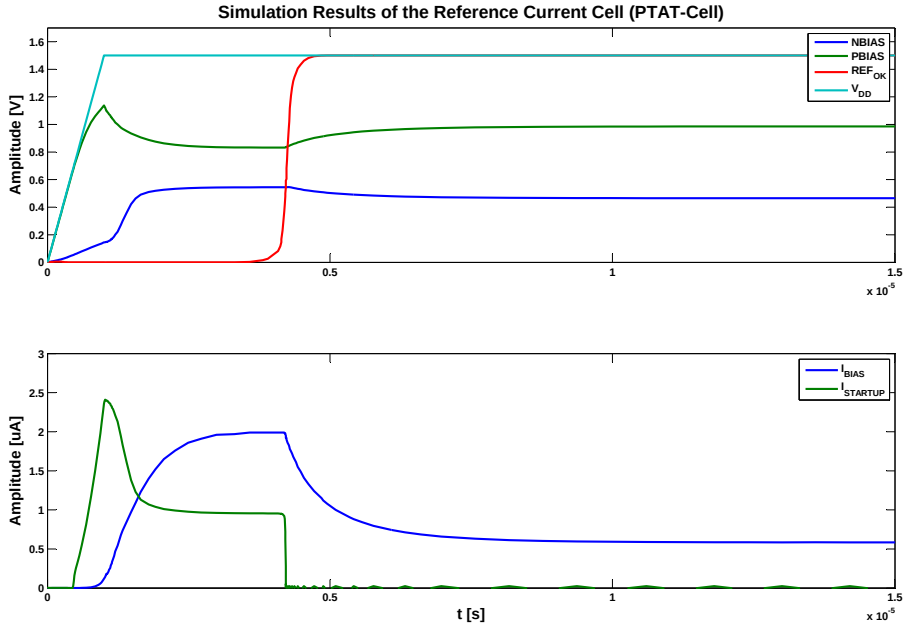


Figure 4.3: Simulation results of the current reference circuit show the most interesting signals of the PTAT cell the bias voltages, the reference-ok signal, the startup current and the output current. This means the startup current is important to initialize the reference circuit and to adjust the operating voltages.

For further distribution and adjustment of the current the circuit in figure 4.4 has been used. The reference voltage V_{REF} is used to define the reference current at the output node I_{OUT}. Here the current value can be adjusted with the switches $S_1 \cdots S_4$.

For the downlink the reader sends a phase modulated carrier signal which can be detected by the phase demodulator of the contactless transponder. Common demodulator circuits (envelope detectors) are based on an amplitude modulated signal. In the case of the envelope detector, the demodulator needs to be carefully designed for a large dynamic detection range due to the possible movement of the transponder in the field of reader. The phase demodulator does not have this dynamic dependency.
A phase-locked loop (PLL) is used to recover the 13.56 MHz system clock. The 13.56 MHz clock signal is used by the phase demodulator and the digital part. The main advantage of phase modulation compared to an amplitude modulation is the quasi constant energy transfer from reader to transponder. Only a small voltage drop occurs in the carrier signal during the phase modulation. The disadvantage of a phase-modulated carrier signal is the complexity of the clock extraction, but if the focus is on high bit rates this drawback has to be neglected.

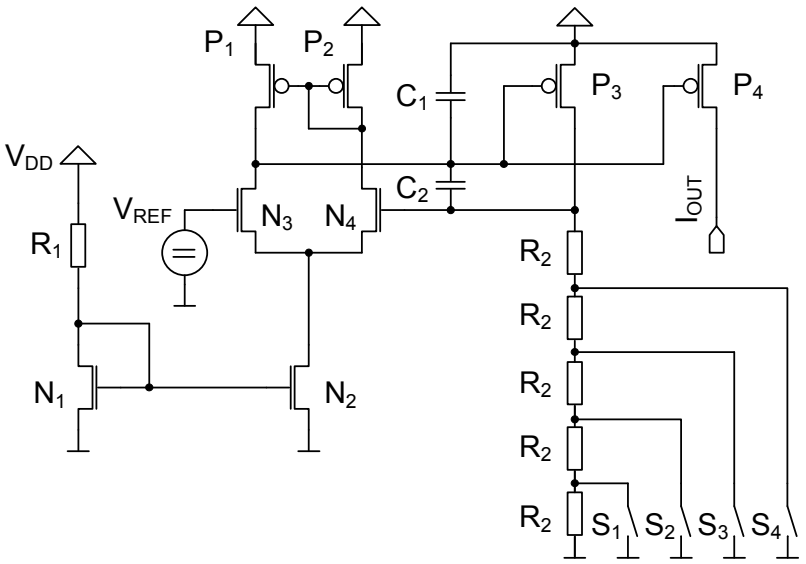


Figure 4.4: Current bank for current distribution. The currents of the bias cell have to be distributed for the analog circuits of the analog front end.

4.2 System and Circuit Design for Very High Bit Rates

The block diagram of the analog front end proposed in Figure 4.5 shows the essential modules of the analog front end. The proposed analog front end operates with a limited small input voltage below 3.5 V compared to traditional solutions which uses voltages above 5 V. A benefit of this small operation voltage is the small coupling influence from transponder to reader-side. Due to this, the settling time of the transponder input signal is only a function of the quality factor of the reader antenna resonance circuit. As a consequence the phase modulated input bits have a smaller settling time and can be detected more easily by the phase demodulator. But the disadvantage of such low input voltage is a weak load modulation from transponder to reader. The weak load modulation complicates the data detection at the reader-side, but this drawback can be solved by inverse load modulation technique.
Especially at the input structure of the analog front end, several thick oxide transistors are needed. The typical threshold voltages of an NMOS and a PMOS thick oxide transistor are $-0.65\,V$ respectively $-0.70\,V$. Thin oxide transistors ("low voltage transistors") are used in the rest of the analog front end.
The analog front end includes an alternating current shunt (AC_{SHUNT}) controlled by the voltage source $V_{GATESHUNT}$, rectifier and voltage regulator with a direct current shunt (DC_{SHUNT}). At the input of the analog front end, the AC_{SHUNT} limits the incoming high induced voltage to a desired voltage value $V_{GATESHUNT}$ + V_{GS}. This limited voltage is rectified by the rectifier and passed to the voltage regulator circuit which produces a stable 1.5 V DC voltage independent of the voltage at node LA/LB (varies with the electromagnetic field strength = position of the transponder with respect to reader antenna). The rectifier consists of two PMOS transistors driven by the current controlled voltage source V_{GATE} and the capacitor C_{RECT}, which smoothes the incoming high frequency voltage. The smoothing capacitor C_{RECT} must be high enough to lower the ripple voltage at VDD_{POWER} node. Instead of NMOS diodes two voltage controlled PMOS transistors have been chosen to reduce the voltage drop from input to rectifier

output [6].
The voltage regulator includes a DC_{SHUNT}, a capacitor C_{STAB}, resistors R_1 and R_2 and a voltage comparator with band gap reference voltage V_{REF}. The voltage comparator compares the input voltage of a voltage divider with a band gap reference voltage V_{REF}. If the voltage node V_{DIV} is higher than the voltage V_{REF}, the output voltage of the comparator $DCSHUNT_{CTRL}$ gets low turning DC_{SHUNT} on. Thereby the node VDD_{POWER} gets discharged. If the node voltage V_{DIV} falls below V_{REF}, the voltage comparator outputs "1" and the DC_{SHUNT} are switched off. In other words, the voltage at node VDD_{POWER} is adjusted by the voltage regulator, depending on the division factor of the voltage divider and the band gap reference voltage. The input signal frequency of the phase demodulator is extracted from the incoming high frequency field by a clock extraction unit. To separate the phase modulated data from the 13.56 MHz carrier an accurate reference clock independent of any phase deviation is needed.

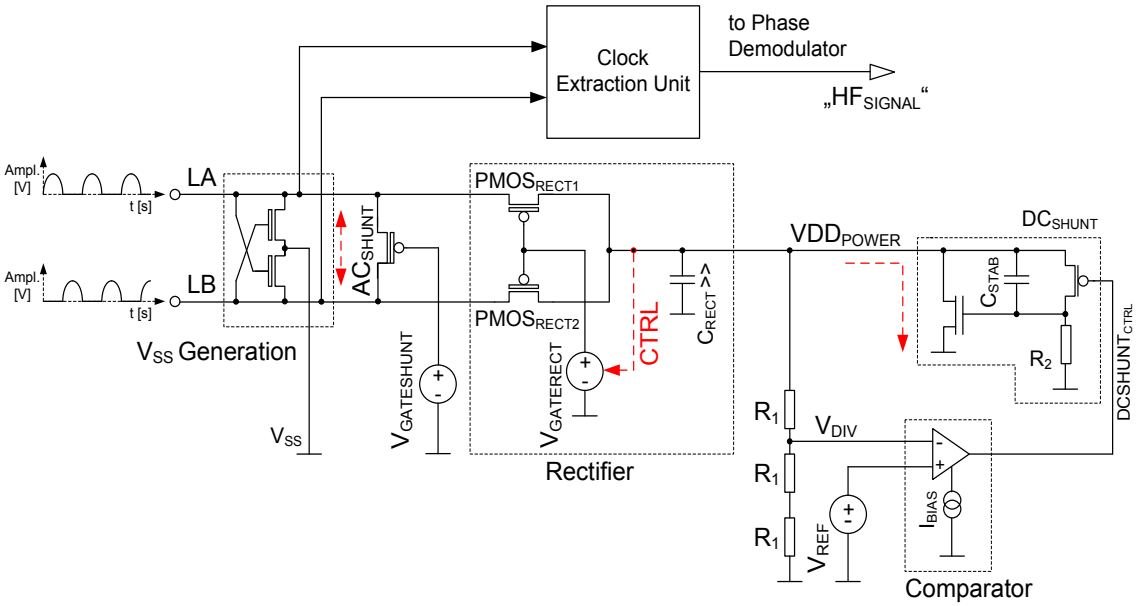


Figure 4.5: Modified analog front end architecture. A common analog front end operates with bit rates up to 848 kbit/s. But the proposed analog front end operates with bit rates which are much higher.

4.3 Load Modulation for High Bit Rates

Tag to reader communication is achieved through variation of the tag impedance. By varying its impedance, the tag varies the current through its loop, which alters the magnetic field. The load modulation technique has been used for data transfer from transponder to reader for several years [25, 85]. Therefore standardized sub carrier frequencies fs of 106 kHz, 212 kHz, 424 kHz and 848 kHz are used.
Possible ways to implement the load modulation technique are the the Manchester-Code with sub-carrier and the binary phase shift keying (BPSK) principle [38]. The standard ISO/IEC 14443 describes two types of the bi-directional data transfer, type A and type B:

Type A: The signaling utilizes 100% amplitude modulation of the RF field for communication from the reader to the card with Modified Miller encoded data. The RF field is turned off for short periods of time when the reader is transmitting. The integrated circuit must store enough energy on internal capacitors to continue functioning while the RF field is momentarily off during field modulation. In opposite direction, on-off keying modulation of an 848 kHz subcarrier with Manchester encoded data is used from transponder to reader.

Type B: BPSK modulation of an 848 kHz subcarrier with NRZ (non-return-to-zero) encoded data. The RF field is continuously on for type B communications. The load modulation principle is based on switching on/off a load at the transponder-side, which results in voltage variations at the reader antenna. This process results in an ASK modulation of the carrier.

The spectrum of the load modulation can be easily interpreted. Two spectral lines are created at a distance of $\pm fs$ around the carrier frequency fc. The spectral lines are shown in 4.6. In the two sidebands the data is transmitted, depending on the modulation of the subcarrier with the baseband coded data stream.

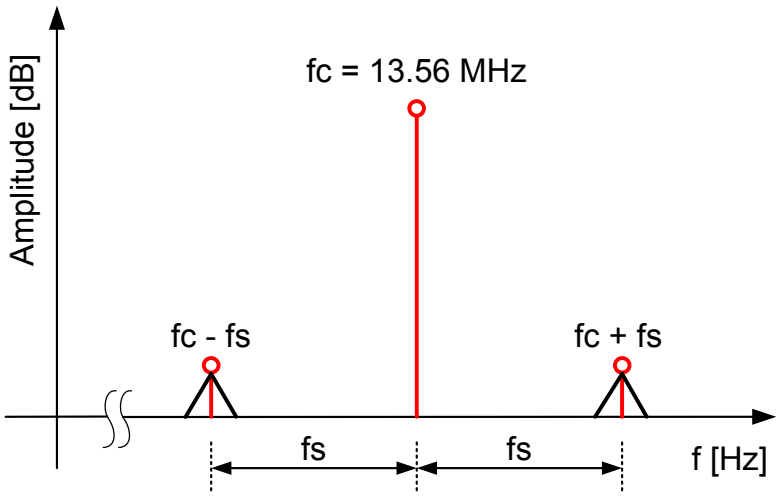


Figure 4.6: Spectrum of the load modulation signal. When we consider the load modulation the load modulation spectrum is of high importance. One main parameter is the distance between the amplitude of the carrier and the sidebands.

Due to the fact that the transponder is a passive device - transmitting significantly less power than the reader antenna - the limitation through the spectral mask is no longer relevant.

Figure 4.7 shows the standardized principle of the load modulation technique [25]. In this example a sub-carrier of 848 kHz is multiplied by a bit stream of "1 0 1 1 0 1 0 0 1 0". The multiplication result is a modulated sub-carrier. In order to shift the data to a higher frequency value the product is multiplied with the carrier frequency by 13.56 MHz.

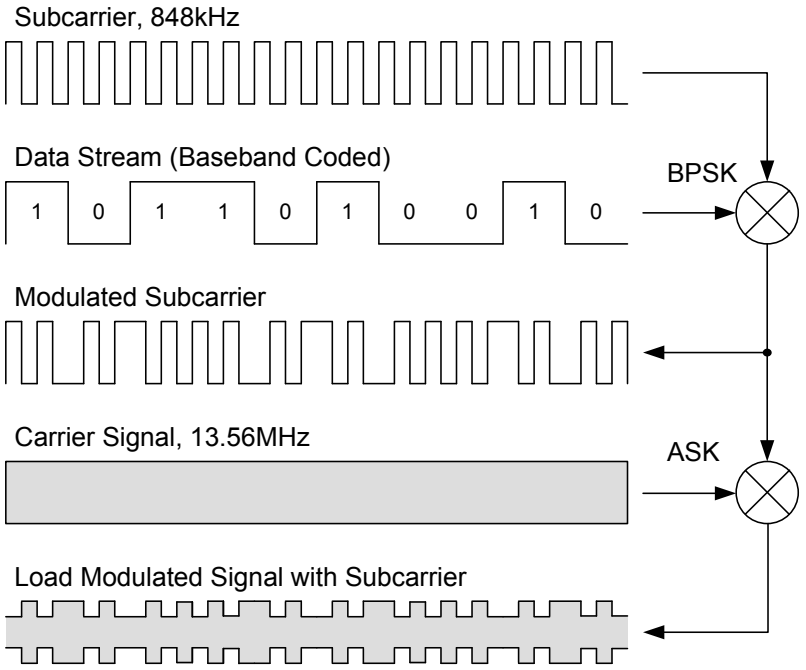


Figure 4.7: Principle of load modulation. The well known principle of load modulation is shown in this figure. In order to increase the bit rate a higher sub-carrier frequency has been chosen. In the proposed system the sub-carrier frequency can be adjusted between 106 kbit/s and 6.78 Mbit/s.

In the proposed system the load equals the AC-shunt/modulation transistor [42], whereby the transistor is placed parallel to the transponder antenna. The advantage of using the same transistor for limiting the input voltage and load modulation is the reduced chip area. The modulation index has to be low enough to guarantee the power supply of the transponder chip and high enough for a detectable signal. In the proposed implementation, a minimum terminal peak voltage between LA and V_{SS} of $2.2\,V$ has been defined. Standardization efforts are currently under way for this issue. Additionally the width of the transistor must be high enough for good voltage clamp property. Because of the eventuality of ESD-pulses an ESD-safe layout of the transistor is necessary and important.

If the "on/off switching" is controlled by the digital data, the data can be transferred from the transponder to the reader.

To increase the bit rate for the uplink a higher sub carrier frequency has been chosen: increased sub carrier frequencies fs of 1.695 MHz, 3.39 MHz and 6.78 MHz are used in order to achieve bit rates of 1.695 Mbit/s, 3.39 Mbit/s and 6.78 Mbit/s (table 4.1). This is a simple method to increase the bit rate significantly without increasing the design complexity. But the disadvantage is that extraction of the bit-stream is not easy due to the low voltage drops (few mV) of the load-modulated

signal.

Table 4.1: Load modulation for high data rates.

subcarrier frequency	subcarrier periods		
	1	2	3
$\frac{fc}{8}$	**1.695 Mbit/s**	—	—
$\frac{fc}{4}$	**3.390 Mbit/s**	**1.695 Mbit/s**	—
$\frac{fc}{2}$	**6.780 Mbit/s**	**3.390 Mbit/s**	**1.695 Mbit/s**

Measurement results (Figure 4.8) of the third test chip show a bi-directional data transmission with a download bit rate of 13.56 Mbit/s and an upload bit rate of 6.78 Mbit/s. The TxD signal stands for the transmitted data, the RxD signal for the received data and the HF_{SIGNAL} for the high frequency signal at input L_A.

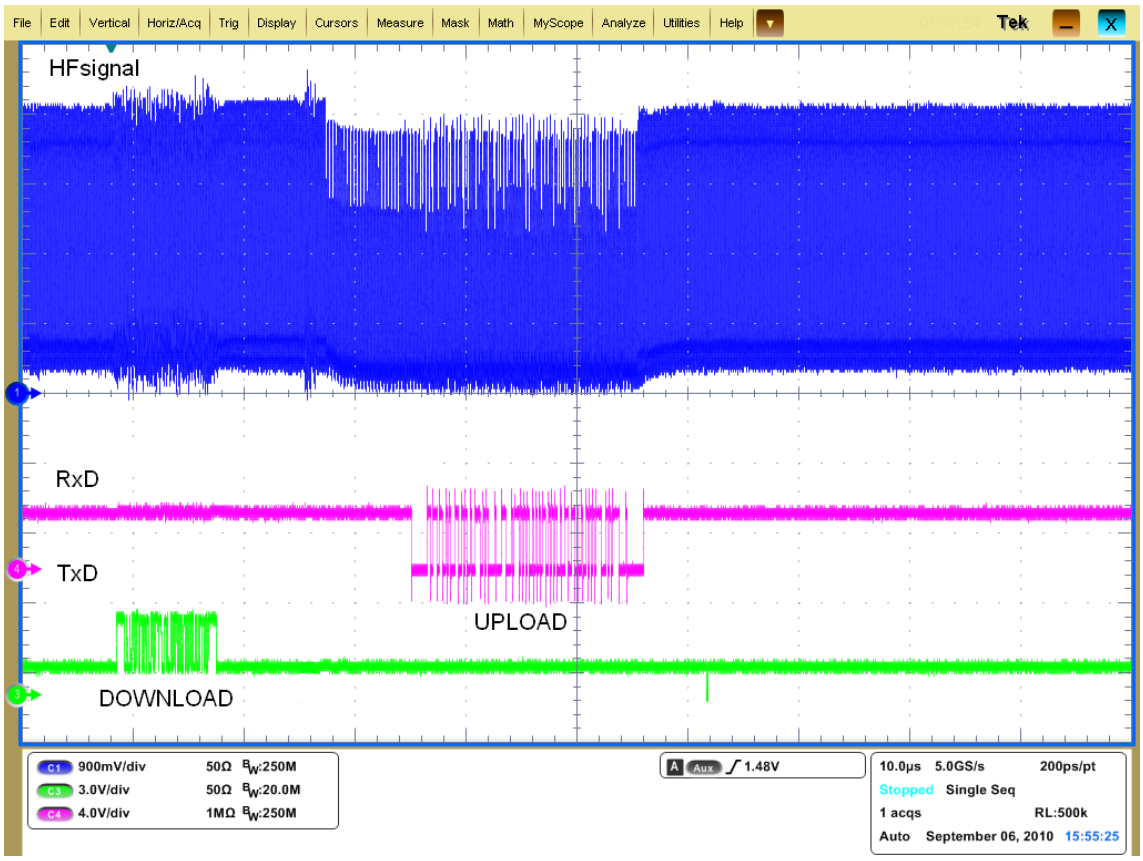


Figure 4.8: Data transmission: 13.56 Mbit/s for download and 6.78 Mbit/s for upload

4.4 Verification

To limit the input voltage to $V_{GATE} + V_{GS}$ at specified field strengths of 1.5 A/m-7.5 A/m, the described shunt system in chapter 4.2 (figure 4.5) has been used. To generate a defined supply voltage of 1.5 V for the transponder chip a voltage regulator has been implemented. The aim of the shunt system is to limit the input voltage as much as possible in order to reach an undistorted data modulation and to simultaneously ensure a stable supply voltage. To find the lowest possible input voltage the functionality of the voltage regulator circuit has been examined. The AC-shunt gate voltage $V_{GATESHUNT}$ (figure 4.5) has been set up to 4 V by the AC-shunt control unit. Figure 4.9 shows the limited input voltages at different input field strengths and the corresponding output supply voltage V_{DD} generated by the linear voltage regulator. A vertical dashed line marks the point when the supply voltage reaches 1.5 V. It can be seen that the minimal limited input voltage uses about 2 V.

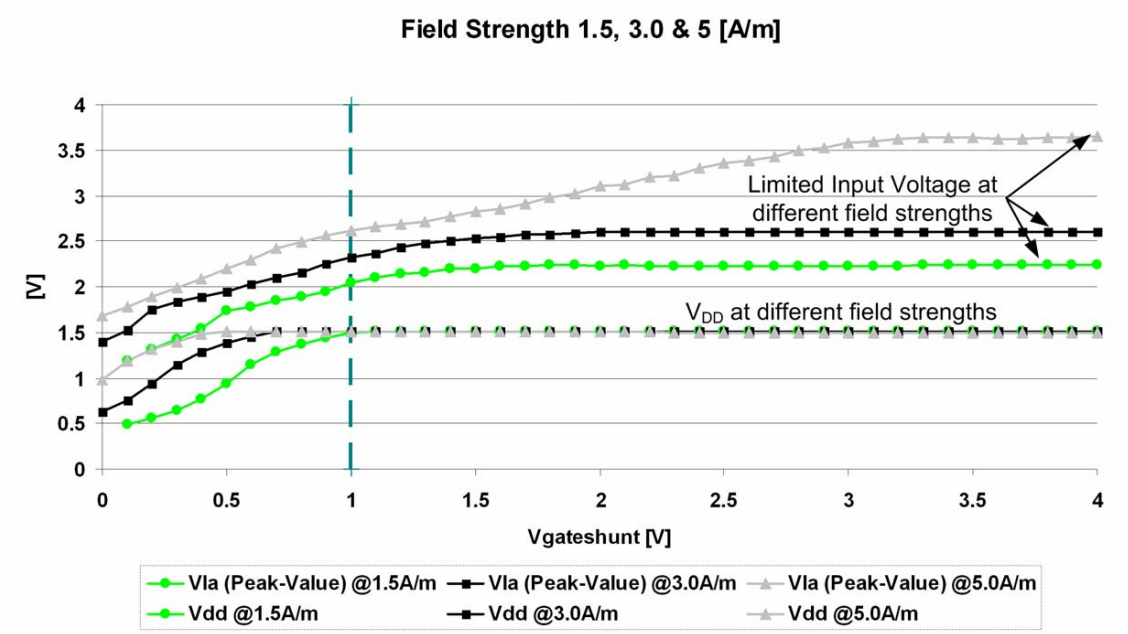


Figure 4.9: Measurement results of the analog front end.

4.5 Summary

Chapter 4 *Analog Front-End Design* deals with the complete system including reader, air interface and transponder and the design knowhow to implement a very high bit rate system. Furthermore, the proposed load modulation technique is discussed with the aim to increase the bit rate from transponder to reader. Finally, measurement results of the second test chip are shown. This test chip shows that it is possible to integrate a compact analog front end with a demodulator for high bit rates.

5 Analog Demodulators

5.1 Discussion of Existing Phase Demodulator Concepts

Phase modulation is a method of modulating wireless data signals to represent information as variations in the instantaneous phase of carrier wave [11]. Conventionally, phase modulation has not been widely used since it requires more complex receiving hardware and since ambiguity problems have often arisen when determining whether, for example, the signal has changed phase by $+180^{\circ}$ or -180°. Instead, existing wireless communication systems often employ amplitude-shift keying (ASK), which is a modulation method that represents digital data as variations in the amplitude of a carrier wave. Generally, the maximum communication speed in those systems based on 13.56 MHz carrier frequency is approximately 848 kbit/s and is typically done at ASK having 10 % modulation index.

5.1.1 Delay Line Concept

A block diagram of the delay line concept is shown in Figure 5.1 [51, 39]. It uses a delay line to store the phase information of the 13.56 MHz clock as it was N periods ago (time shift). A phase comparator (phase frequency detector = PFD) is used to compare the actual phase with the stored one in order to demodulate the phase modulated data [55]. A digital calibration is necessary to get the delay line very close to an N clock period delay. While receiving data the delay line is held in lock, this means the phase of the incoming signal is very close to the phase of the delayed clock by means of a delay locked loop. The PFD only sees a phase difference during the time it takes the phase change to propagate through the delay line. The output pulses of the PFD at node QA and QB control a current charge pump depending on the input phase deviations of both PFD inputs. Incoming data bits are extracted by comparison of the outputs of a low pass filter with time constant τ_1 and a capacitor block with time constant τ_2 by a phase detector unit (figure 5.1).

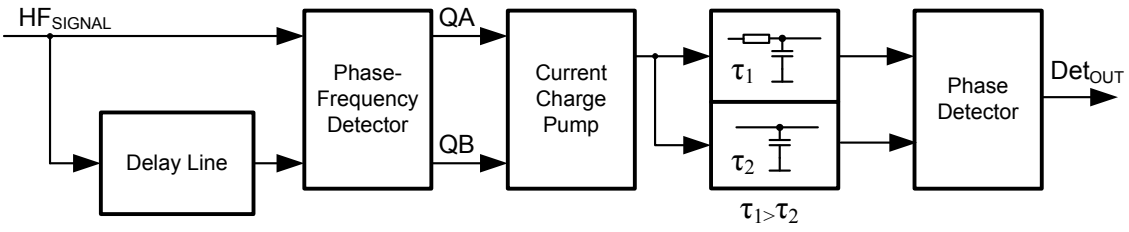


Figure 5.1: Delay line principle. The delay line is the main component of this demodulator type. It is based on the same principle as the coincidence demodulator [55].

The first and major drawback of this concept is a high power and chip area consumption. Another disadvantage is that a digital auto calibration for a delay line is needed, because of tem-

perature drift and process variations. Additionally, it is difficult to differentiate between different phase states of a multi-level phase modulated signal.

5.1.2 I/Q Demodulator

The block diagram in figure 5.2 shows another concept of phase demodulation at the transponder -side. This principle is based on an In-Phase/Quadrature-Phase demodulator [64], where the incoming carrier signal (HF_{SIGNAL}) is multiplied by a sine and cosine signal respectively. For example, a Gilbert cell [65] can be used as a multiplier. In typical applications a local oscillator or a phase locked loop generates the sine wave (reference clock). The cosine wave is derived from the sine signal by a 90 degree phase shifter. In case of a passive transponder it is difficult to generate an accurate reference clock which is independent of the phase modulated data signal at the input, because it is not economically or even not feasible at all to put external components on the smart labels, such as external oscillators or PLLs.
The incoming signal is multiplied by the sine/cosine and is filtered by a lowpass filter to suppress the high frequency components, which are a result of the multiplication. Output signals of both lowpass filters are evaluated by a threshold decision with a comparator circuit.
Two main advantages of the I/Q demodulator are low current consumption and a reduced chip area. In addition there is no need for a digital calibration. Instead an analog calibration with a phase locked loop is used. Drawbacks are the phase jitter of the local oscillator or phase-locked loop and a limited phase shift accuracy of the 90° shifter.

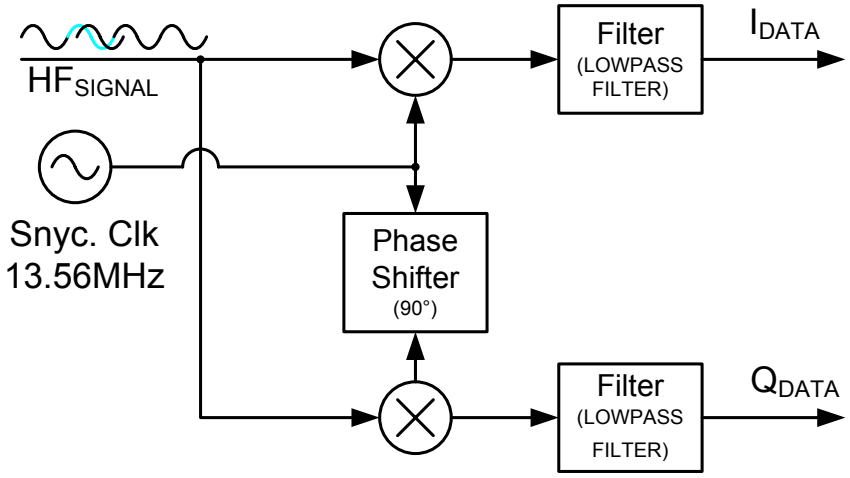


Figure 5.2: IQ demodulation block diagram. IQ demodulation is a common type of phase demodulation. It owns its popularity to the simplicity and the possibility to output the baseband data directly.

In this context two demodulation principles are possible, the coherent demodulation and the non-coherent demodulation technique.
Coherent demodulation means that the carrier signal must be gained from the incoming electromagnetic field. In phase modulation case, this concept relies on a recovered clock signal with a high quality. On the other hand the non-coherent demodulation technique makes it possible to extract the data from an incoming signal with reduced quality with low SNR. A typical non-coherent demodulation method is the envelope detector for amplitude and frequency demodulators.
Generally, the phase modulated input signal is described with the formula

$A(t) \cdot cos(2 \cdot \pi \cdot f \cdot t + \varphi(t))$ whereas $\varphi(t)$ represents a phase change in the incoming PM signal (figure 5.3).
Then the phase modulated input signal is multiplied by an extracted 13.56 MHz sine signal or by a reference signal of a local oscillator which is represented by the equation $cos(2 \cdot \pi \cdot f \cdot t)$ or the 90° shifted one $cos(2 \cdot \pi \cdot f \cdot t + \frac{\pi}{2})$.
The multiplication result contains two product terms, the high frequency component ($\frac{1}{2} \cdot A(t) \cdot cos(4 \cdot \pi \cdot f \cdot t + \varphi(t)$ or $\frac{1}{2} \cdot A(t) \cdot cos(4 \cdot \pi \cdot f \cdot t + \varphi(t) + \frac{\pi}{2})$) and the baseband term ($\frac{1}{2} \cdot A(t) \cdot cos(\varphi(t)$ or $\frac{1}{2} \cdot A(t) \cdot cos(\varphi(t) + \frac{\pi}{2})$). The high frequency term is canceled by a high-order low pass filter. Furthermore, the filtered multiplication results are shown in figure 5.3 on the right side.

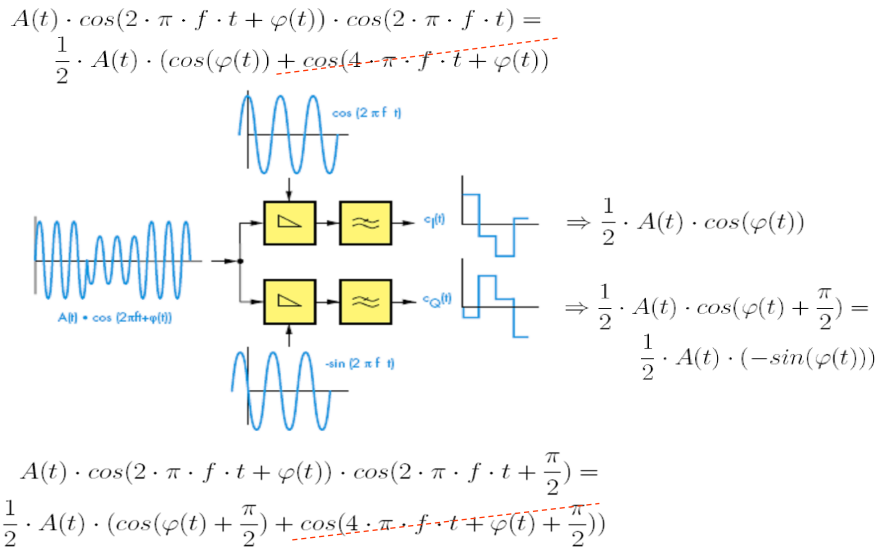


Figure 5.3: IQ demodulation principle

The principle of coherent demodulation is simple, but the method is difficult to implement as the clock has to be gained from the phase modulated signal. In case of a phase-modulated signal the clock extraction can be done by a phase locked loop. The disadvantage of the I/Q demodulator is a doubling of the hardware effort, because an additional multiplier, filter and level shifter is needed.
Due to the mentioned disadvantages of the delay-line concept and the well known I/Q demodulator, novel demodulator concepts and circuits for high bit rates had to be designed and integrated. In the following three proposed demodulators are discussed in the following chapters:

- Amplitude demodulator for bit rates up to 3.4 Mbit/s: chapter 5.2
- 2-state phase detector for bit rates up to 13.56 Mbit/s: chapter 5.3
- Multi-level phase detector with ADC for bit rates above 13.56 Mbit/s: chapter 5.4

It will be shown that it is possible to extract amplitude-modulated bit streams with bit rates above 3.4 Mbit/s by a novel amplitude demodulator. But for bit rates up to 27.12 Mbit/s the phase modulation technique is the better choice. Therefore, two novel phase demodulation techniques have been introduced.

5.2 Proposed Amplitude Demodulator for Very High Bit Rates

Common amplitude demodulators are envelope detectors (figure 5.4). The demodulation circuitry consists of a peak detector and a high pass to eliminate the constant component.

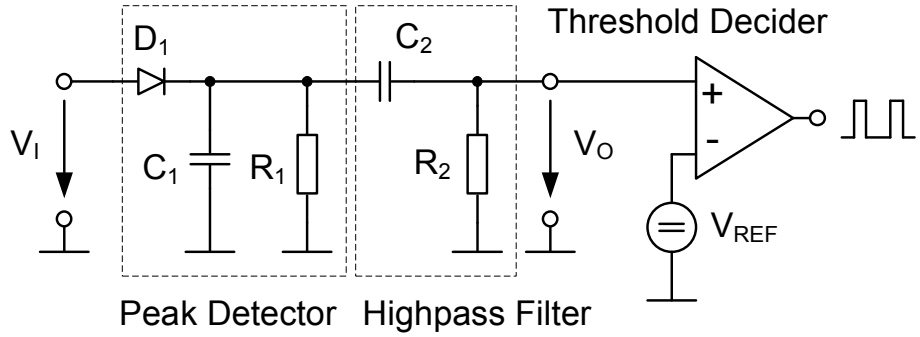


Figure 5.4: Common amplitude envelope detector. For the demodulation of an amplitude modulated signal the envelope detector is the simplest way. The peak detector consists of three components, a diode, a capacitor and a resistor. If the resistor and capacitor are correctly chosen, the circuit outputs the peak envelope of the input signal. After that the baseband component is filtered out.

The capacitor in the circuit stores charge on the rising edge, and releases it slowly through the resistor when the signal falls. If the resistor and capacitor are correctly chosen, the output of this circuit will approximate a voltage-shifted version of the original (baseband) signal. A simple filter can then be applied to filter out the DC component. This non-coherent amplitude demodulation scheme is very simple to implement, but it is not useful for high data rates, because the carrier frequency has to be significantly higher than the maximum frequency of the data signal[80].

Simulation results show an amplitude modulated signal and the corresponding envelope signal of the peak detector in figure 5.5.

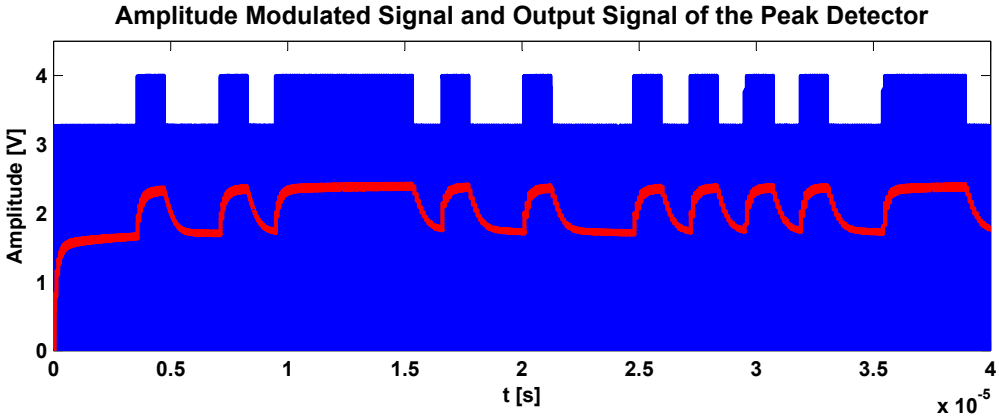


Figure 5.5: Amplitude modulated signal and envelope information. Due to the diode a voltage drop occurs between the input signal V_I and the peak detector output. The final evaluation will be done by a threshold decider. As a result the envelope detector outputs the data stream (baseband data).

Furthermore the envelope signal is evaluated by a 'threshold decider'. The output signal of the threshold decider is the extracted baseband data.

5.2.1 Analog Front End with Amplitude Demodulator

As already mentioned, the envelope detector circuitry are not useful for recognition of high data rates. Therefore a novel amplitude demodulator [2] (Auer et al.,2009) is further discussed for bit rates up to 3.4 Mbit/s.
The block diagram in figure 5.6 shows the important modules of the transponder. In the following the demodulator is described in detail.

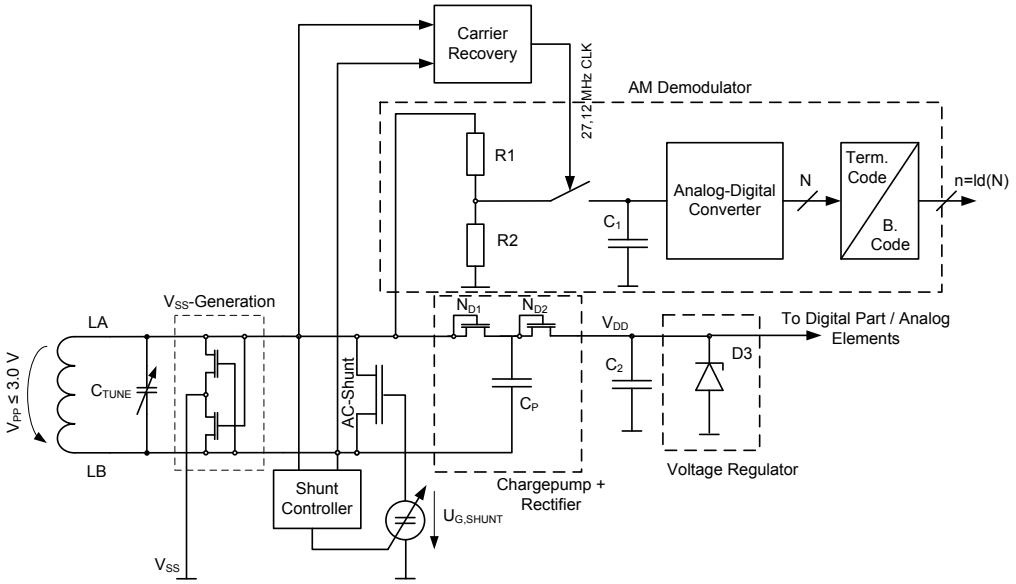


Figure 5.6: Analog front end with amplitude demodulator for high bit rates. A better way to extract the baseband data is an ADC structure in contrast to the envelope detector. The binary output word of the ADC can be digitally processed to get the baseband data.

The proposed analog front end consists of the analog front end and an ADC amplitude demodulator. In contrast to typical implementation methods the input voltage V_{PP} is limited to a value of less than or equal $3\,V$. As a result of the limited input voltage a low quality factor follows. Due to a low quality factor the result is a bigger bandwidth and a low settling time of the amplitude modulated signal. This implies that the amplitude modulated input signal with a smaller bit time can be detected more easily. But the disadvantage of the voltage limitation is a weak load modulation. To counteract this problem the inverse load modulation technique [41] can be used. A second way to circumvent this drawback is to increase the voltage level of the input voltage by means of a charge pump circuit. To get an efficient charge pump functionality both input nodes, LA and LB, are used. If a charge pump circuitry with a big output capacitor is used no rectifier is required in the analog front end design. The charge pump output voltage is set to a defined value by the line regulator. Due to this the output voltage of the charge pump is independent of the dynamic field strength.
The amplitude demodulator includes the carrier recovery unit, the integrated sample and hold circuit, the analog to digital converter and the decoder. The sample frequency of the demodulator

is 27.12 MHz, which is generated by the clock recovery unit. To generate a 27.12 MHz clock the negative and positive half waves of the incoming signal are used. Before the ADC is fed by the input signal, the voltage amplitude of the input signal is lowered by the voltage divider between nodes LA and V_{SS}. This voltage is sampled with the 27.12 MHz clock from the clock extraction circuit. Thereby the optimal sample point has been adjusted by a variation of the capacitor in the carrier recovery unit.
The ADC compares the input voltage with 16 reference voltages. These reference voltages are defined $\pm\Delta V$ around the peak value of the input signal. Due to this definition the detection of overshoots and undershoots is also possible. In the proposed concept a low power ADC was integrated to minimize the voltage drop of the supply voltage. The 16 output signals of the ADC are encoded to a 4 bit binary word by a thermometer to binary decoder. For further digital processing the 4 bit binary word feeds the digital part of the analog frond end.

5.2.2 Amplitude Demodulator Verification

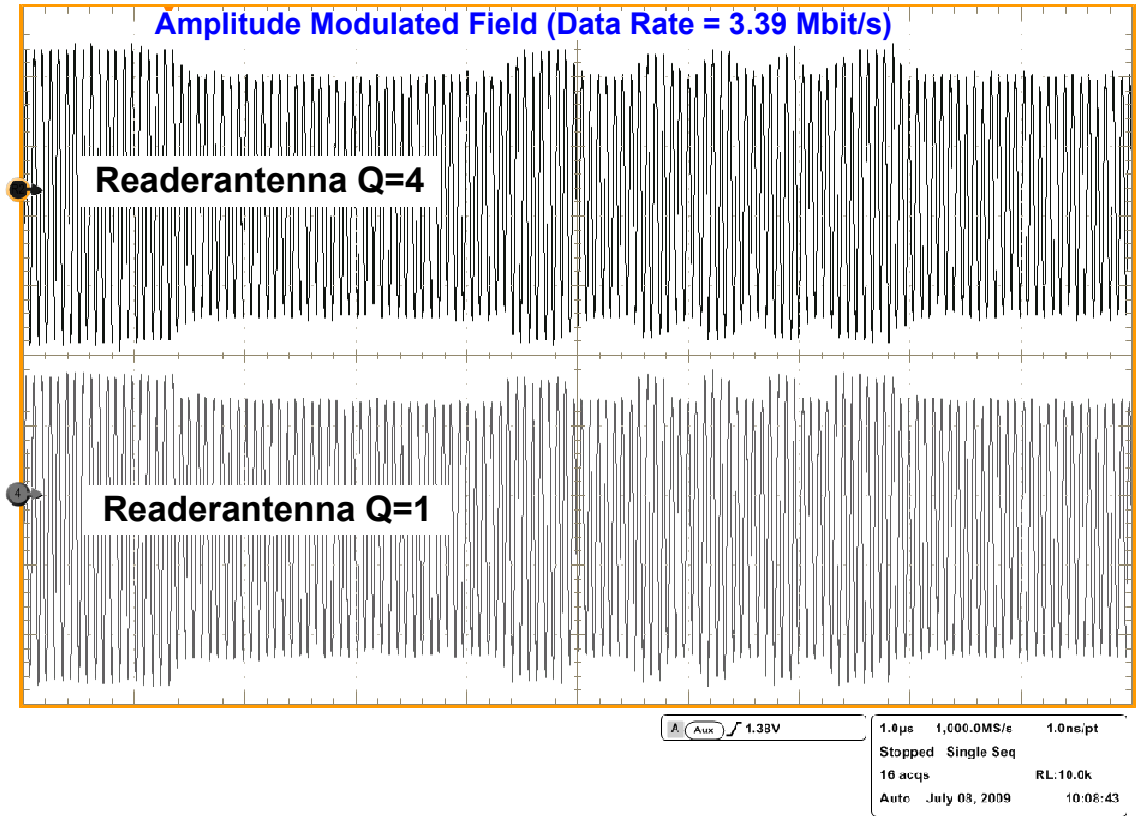


Figure 5.7: Amplitude modulated field with different quality factors. Here, an amplitude modulated signal is shown with two different quality factors. Thereby, the edge transitions are much steeper if the quality factor is low and the baseband data can be extracted more easily.

Figure 5.7 shows measurement results of an amplitude modulated signal, which is modulated by a data rate of 3.4 Mbit/s at a carrier frequency of 13.56 Mbit/s.
The bandwidth limitation and thus the limitation of the maximum data rate is determined by the quality factor of the reader resonance circuit. Due to a high quality factor of the reader resonance circuit there exists a better energy transfer from reader to transponder. On the other hand the transmission bandwidth decreases with higher quality factors. With a high quality factor the settling time of the emitted amplitude modulated field signal increases and the extraction of the modulated data is much easier. The relationship between the quality factor and the bandwidth is given in 5.1.

$$Q = \frac{f_{RES}}{B} = \frac{2 \cdot \pi \cdot f_{RES} \cdot L_{COIL}}{R_S} \tag{5.1}$$

Q ...Quality Factor

f_{RES} ...Resonance Frequency

L_{COIL} ...Inductance of Reader Antenna

R_S ...Series Resistance of Reader Antenna

B ...Bandwidth

To achieve a good power transfer from reader to transponder a high quality factor Q of the reader resonance circuit is required. At the same time a low quality factor of the resonance circuit is needed to increase the transmission bandwidth for high data rates. Figure 5.7 shows an amplitude modulated signal with different antenna configurations on the reader-side. Reader antenna 1 has a quality factor of 4 and reader antenna 2 of 2. The bit rate of both AM signals is 3.39 Mbit/s (4 periods/bit).
The baseband data of the modulated signal is more difficult to extract in case of antenna configuration 1 compared to antenna configuration 2 with a lower quality factor and without signal distortion. A good solution is the use of an ADC amplitude demodulator to extract the data. With this kind of amplitude demodulators more than two output levels are possible. Furthermore the ADC variant enables the possibility for digital post processing. However, one problem is that amplitude fluctuations have a great influence on the quality of the data extraction. Consequently the amplitude fluctuation, the noise and jitter influence contribute to the practicable maximum ADC resolution. Simulation results have been shown that the 4-bit ADC is a good compromise between a low power design and a maximum amplitude resolution.
The integrated analog front end with the amplitude demodulator for high bit rates and the corresponding measurement results are shown in figures 5.6 and 5.8.
Measurement results of the amplitude modulated input signal are shown in figure 5.8 compared to the binary output word of the ADC. In the upper trace the bit changes of the input signal are shown whereas in the trace below the corresponding ADC output can be seen. In this case a bit rate of 3.39 Mbit/s is transferred, which is equivalent to a bit time of 295 ns (4 periods/bit). After the demodulation process the data is transferred to the digital part. The digital part receives the analog to digital converted signal and makes a threshold decision to get the extracted bit sequence. This bit sequence is equivalent to the incoming amplitude modulated data.

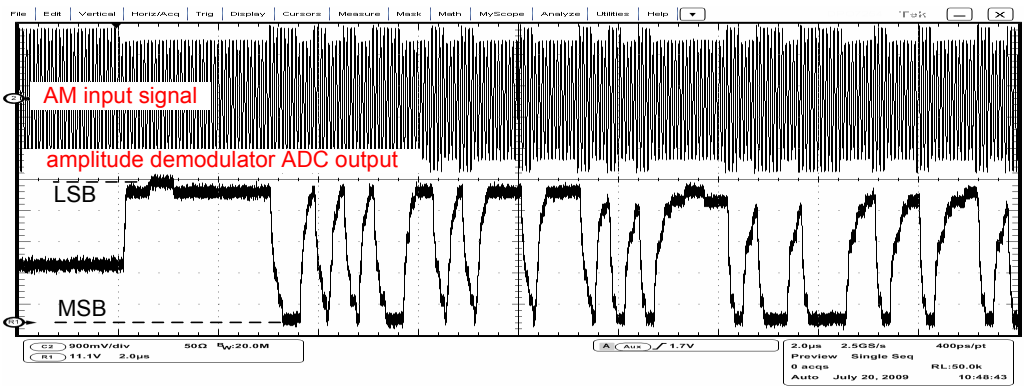


Figure 5.8: Measurement results of the analog front end with amplitude demodulator for high bit rates. The Figure above shows an amplitude modulated signal and the output values of the ADC. The ADC output value corresponds to the voltage variations of the amplitude modulated signal.

The measurement results of the test chip show that it is possible to gain the data from an amplitude modulated signal with high bit rates. Here a bit rate of 3.34 Mbit/s is detected by the amplitude demodulator, but by means of digital post processing higher bit rates up to 13.56 Mbit/s

are possible with the same demodulator principle. But multi level amplitude demodulation is not so easy due to unwanted amplitude fluctuations, caused by the supply voltage fluctuations and the distorted AM input signal. To avoid the amplitude dependency, phase modulated signals are used in the following (chapter 5.3). These phase modulated signals show a relative stable amplitude over time with low modulation index.

5.3 Proposed 2-State Phase Demodulator for Very High Bit Rates

In chapter 5.2.1 a proposed amplitude demodulator has been presented for bit rates up to 3.4 Mbit/s. To achieve a further increase of the bit rates from reader to transponder a novel phase demodulator [4] is introduced. An improved implementation method of a demodulator circuit for high bit rates is the phase demodulator. A novel clock recovery principle has been introduced to get a constant reference clock for data extraction. The clock generation principle, the phase demodulator circuitry and the verification of the phase demodulator are topics of further discussions.

5.3.1 Clock Generation Principle

In typical passive transponder architectures the reference clock is extracted from the incoming amplitude modulated field (13.56 MHz) with the aid of a clock recovery unit.
The proposed transponder architecture, however, is based on a phase modulated signal from reader to transponder. To get the phase modulated signal it is important to have an accurate reference clock with constant phase and frequency behavior. This means that the clock must be stable having a constant period independent of phase shifts in the phase modulated signal. The challenge is to extract a constant clock from the incoming phase modulated field. To achieve an independent reference clock a reference bit was added at the beginning of each transmitted data frame. Figure 5.9 shows an example of the proposed phase modulated bit stream. Each data frame consists of L phase modulated data bits $BIT_1 ... BIT_L$ and one reference bit REF. The first occurring reference bit can be recognized with the help of a training sequence. Reference bits are used to stabilize the demodulator circuitry. The main advantage of this method is the resulting constant reference clock, which is independent of phase deviations from the input signal.

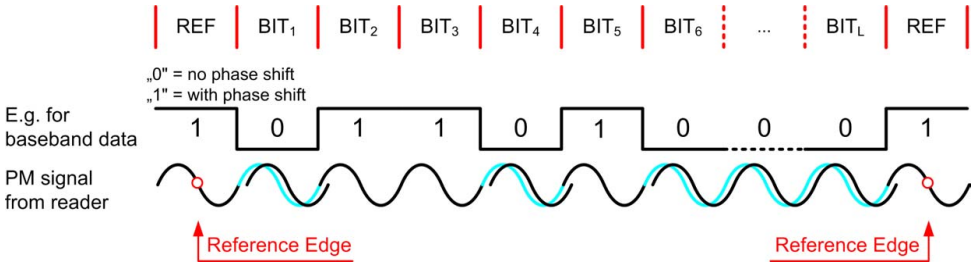


Figure 5.9: Introduced bit frame. This figure shows the extracted baseband data and the suggested phase modulated signal. A typical bit stream in the proposed demodulator system consists of 8 data bits and one reference bit for synchronization.

5.3.2 Phase Demodulator

Figure 5.10 shows a detailed block diagram of the phase demodulator. The phase demodulator includes a phase locked loop (PLL) and two phase detectors. The PLL consists of two $\frac{1}{N}$ counters, a phase-frequency detector, a current charge pump, an RC filter, a current controlled oscillator and $\frac{1}{M}$ divider. The phase locked loop generates the reference clock $OscOut$ for the phase detector. Phase detectors serve to recover the phase jump in the incoming signal. Phase detectors sample the incoming phase information with half of the bit frequency and outputs the binary word at $CompPD1$ and $CompPD2$. In the proposed design two phase detectors are used in a two state mechanism, which allows a better time resolution of the sampled data.

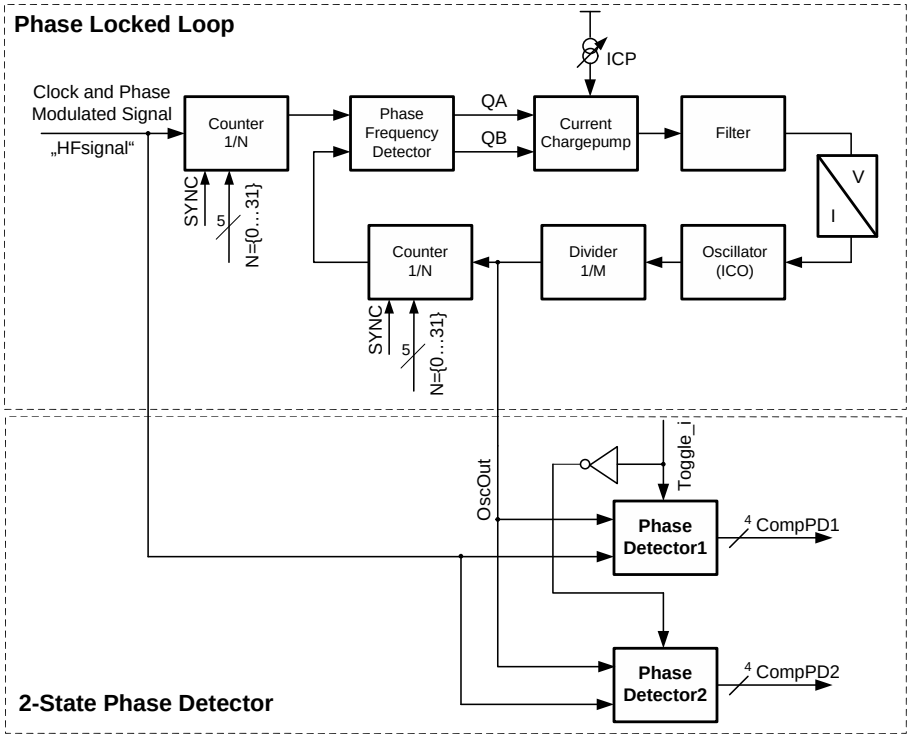


Figure 5.10: Phase demodulator with two phase detectors. As already explained, the phase locked loop is important to generate a constant 13.56 MHz clock for the phase detectors. The input signal of both phase detectors are the incoming phase modulated signal HF_{SIGNAL} and the phase locked loop output clock $OscOUT$.

The phase deviation over time for the input and output signal of the phase locked loop are shown in Figure 5.11. In this case, the phase-locked loop generates the clock without any synchronization processes and counters. Additionally, the PLL parameters are tuned to get a fast settling characteristic. The output phase of the phase locked loop follows the phase curve of the incoming signal. With this approach a detection of a 2-state phase modulated signal is possible without problems. As part of this chapter, new ways are adopted to improve the phase demodulator for multi-level phase detection.

The phase-locked loop generates the system clock out of the incoming phase modulated field signal. This clock has the same frequency as the carrier. The phase locked loop includes two adjustable counters, an adjustable current charge pump, a phase frequency detector, a filter, a

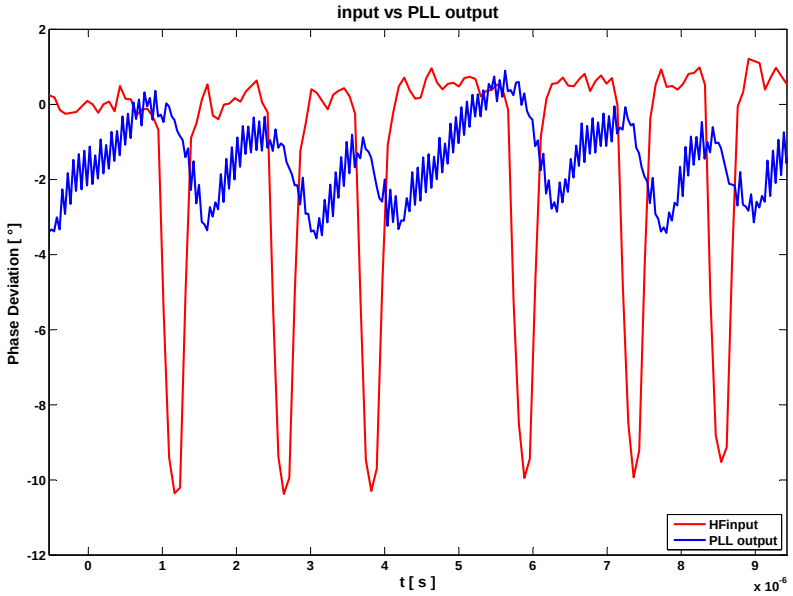


Figure 5.11: Measurement results of the phase deviation of nodes HF_{INPUT} and $OSCout$ without any synchronization mechanism. It can be seen that the PLL output clock $OSCout$ follows the incoming signal HF_{SIGNAL}.

voltage to current stage, current-controlled oscillator and the $\frac{1}{M}$ divider. The input frequency of the signal HF_{SIGNAL} is divided by a factor of N with the help of the counter circuit. Due to the divided input clock the phase locked loop triggers at each reference bit. Thereby the counter must be synchronized with a synchronization bit (Input $SYNC$). Here, the distance between the synchronization bits can be adjusted by the counter value N.
The adjustable counter is shown in figure 5.12.

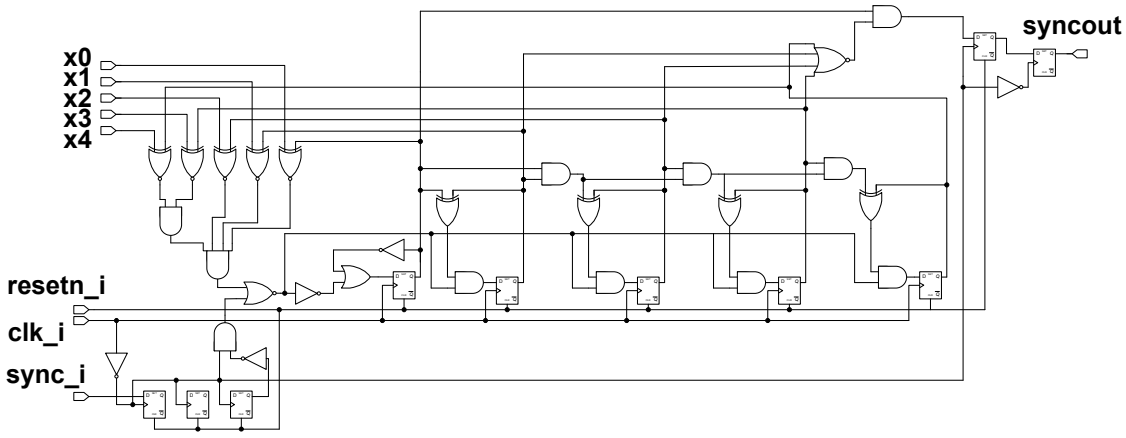


Figure 5.12: Synchronized adjustable counter. For a correct phase-locked loop synchronization two adjustable counters are used. The inputs include the clock input clk_i, the synchronization input $sync_i$, the reset input $resetn_i$, the input pins $x < 0 : 4 >$ and the output node $syncout$.

The counter input is called clk_i and the output $syncout$. The division factor of the counter can be adjusted between 1 and 32 by the input pins $x0$ to $x4$. This division factor depends on the

incoming bit rate and is set due to a training sequence. After the synchronization pin $sync\_i$ is set to one the division value N is put back to one. Because of this principle the phase-locked loop does not see any phase deviations caused by the phase-modulated input signal HF_{SIGNAL}. Between the synchronization pulses a phase error occurs as a result of floating effects and phase jitter. On the basis of this fact and of measurement results, the maximum period of the PLL trigger signal is limited by a factor of 32 periods $(2.36\,\mu s)$. Above this counter value the accumulated phase jitter causes too many detection errors.
The phase-frequency detector determines the difference between the phases of the two input signals. Furthermore, the output signals of the phase frequency detectors control the current charge pump. The phase deviation between the phase frequency detector input signals represents the phase error generated by the phase locked loop. The phase error is proportional to the output voltage of the charge pump circuit $(-2 \cdot \pi < \Theta e < 2 \cdot \pi)$. A loop filter smoothes the high-frequency components of the current charge pump output for the current controlled oscillator. The current controlled oscillator output depends on the current output of the $\frac{V}{I}$ converter. The relationship between the voltage at filter node and the measured but divided output frequency of the $108\,MHz$ oscillator for different chips can be seen in Figure 5.13. In order to reduce the oscillator jitter the oscillator frequency has been multiplied by an factor M. The gain of the oscillator is about $270\,MHz/V$ and the circuit is optimized to achieve a low power consumption. This high gain factor has been chosen to minimize the settling time at the training sequence. The oscillator output frequency is divided by factor M (Figure 5.10) and is then comparable with the input signal HF_{SIGNAL}.

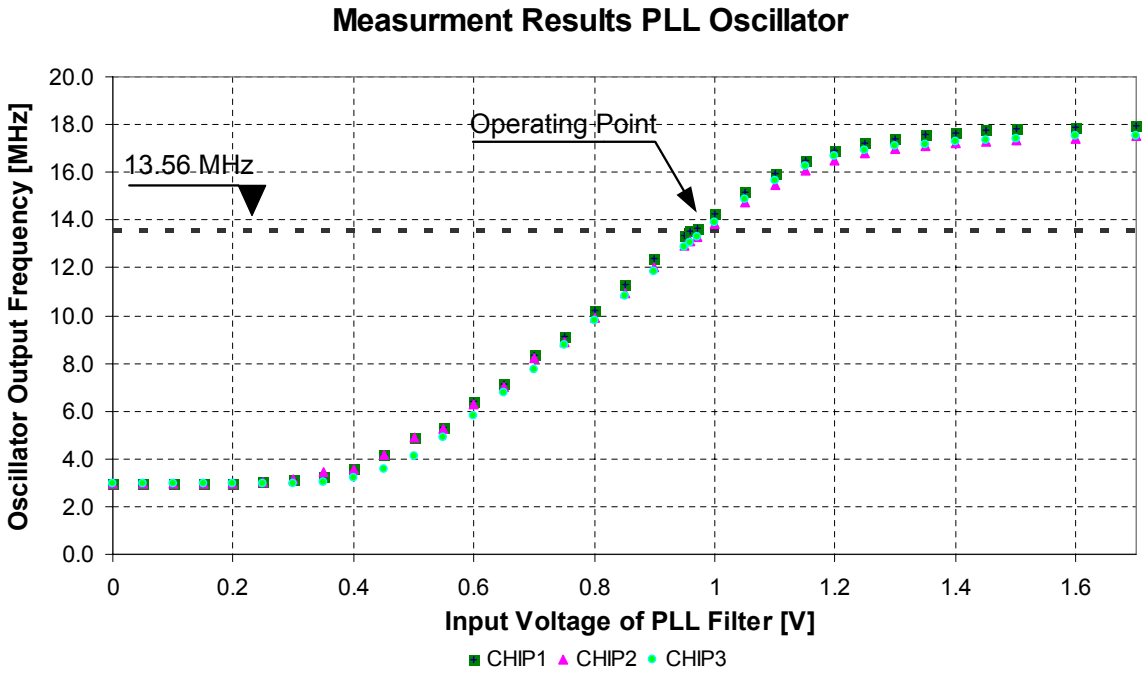


Figure 5.13: Divided output frequency of the voltage controlled oscillator depending on the input voltage. So the oscillator frequency is a multiple of $13.56\,MHz$ $(M \cdot 13.56\,MHz)$.

The loop is locked when the frequency of Osc_{OUT} is equal to the frequency of the input signal HF_{SIGNAL} and when both signals are in phase.

A simple ring oscillator [22] includes three inverter stages. In Figure 5.14 the current controlled oscillator is driven by a current source I_{DC}.

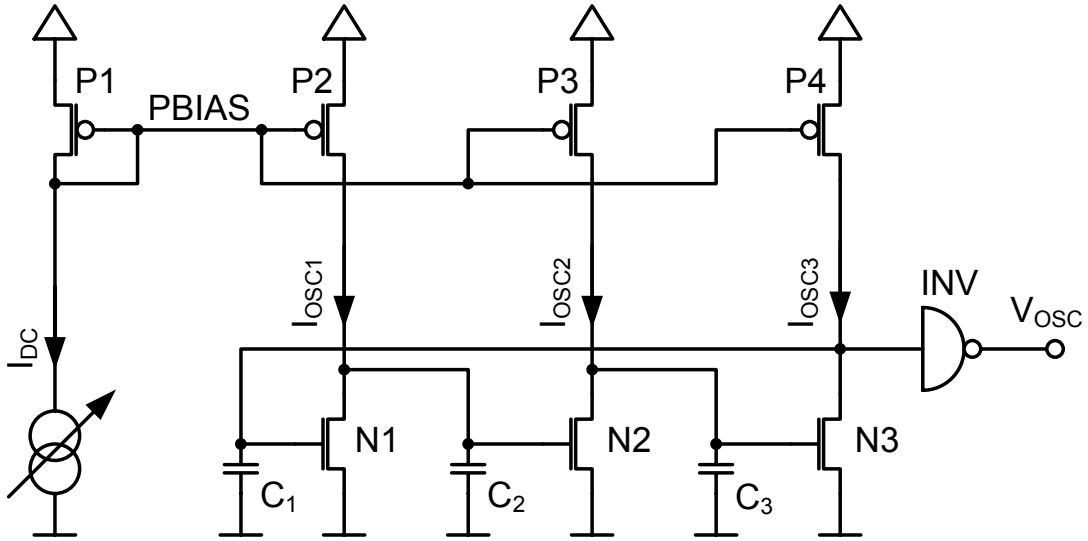


Figure 5.14: Ring oscillator. A well known oscillator type is the ring oscillator which is used in the proposed system.

In case of a low-frequency and low-power oscillator, the inverter stages are weak (big transistor length) and the number of stages is high. The currents I_{OSC1}, I_{OSC2}, I_{OSC3} and the capacitors C_1, C_2, C_3 and the parasitic capacitors of NMOS transistors $N1$, $N2$ and $N3$ define the free-running output oscillator frequency.
Another way to implement a ring oscillator is the current starved oscillator [22, 26]. The current starved oscillator is sourced by the current sources I_{OSC1}, I_{OSC2} and I_{OSC3} from NMOS and PMOS transistors, the current mirrors and the three inverter stages with capacitors C_1, C_2, C_3. By using a current sink and current source, the oscillator is decoupled from the power supply. Here the current sources I_{OSC1}, I_{OSC2} and I_{OSC3} can be adjusted by the current source I_{DC}. Furthermore to get an adequate output signal an output buffer is used. The disadvantages of this type of oscillator compared to the ring oscillator is that the power and area consumption are higher.

Figure 5.16 shows the comparison of the gain curves of the two oscillator structures, the ring oscillator and the current starved oscillator. Typical values of the gain factor are above $210\,MHz/V$ in the proposed design at the operating voltage range. The high value is needed in order to achieve a fast settling time at the start of frame sequence.

A further interesting way to visualize the oscillator jitter is the phase jitter histogram. Jitter is usually specified in $\pm$pico seconds. Jitter measurements can be classified into three categories: cycle-to-cycle jitter, period jitter, and long-term jitter. All jitter measurements are at a specified operating voltage, usually 1.5 V. In the following, the cycle-to-cycle jitter and the long-term jitter are generally used for the measurements. For long-term jitter measurement the TIE (Time Interval Error) function is used to illustrate the jitter performance of the system. TIE is a measure of $\varphi(t)$ that compares the jitter clock to an ideal clock source operating on the long-term average frequency of the signal. In effect, TIE is the discrete time domain representation of phase noise expressed in pico-seconds. TIE is measured by subtracting the time of crossing through the

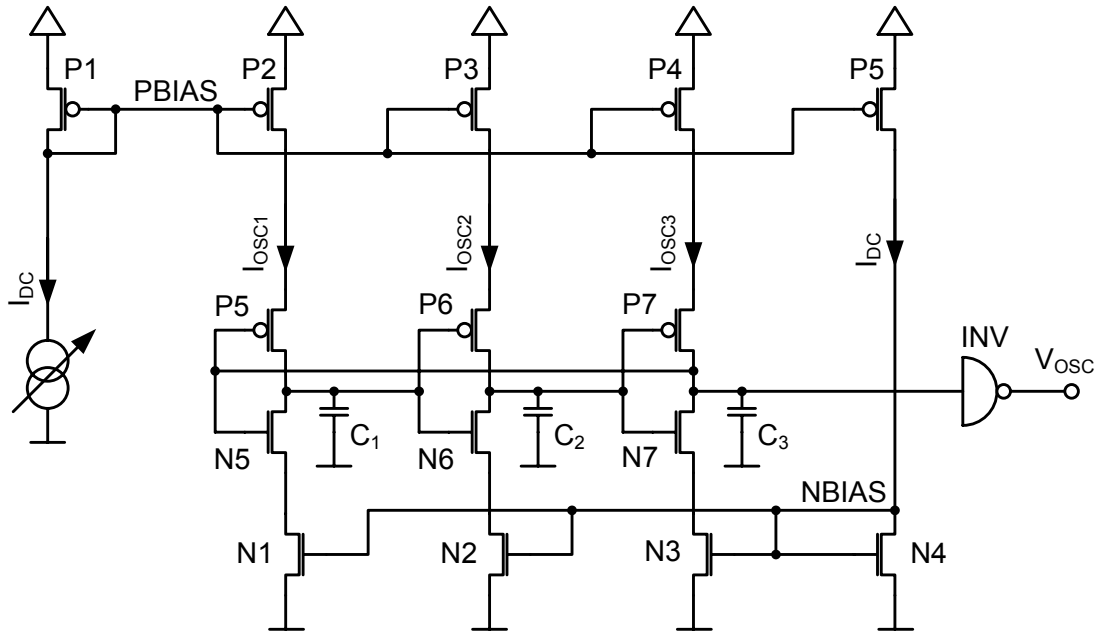


Figure 5.15: The current starved oscillator is an improved ring oscillator.

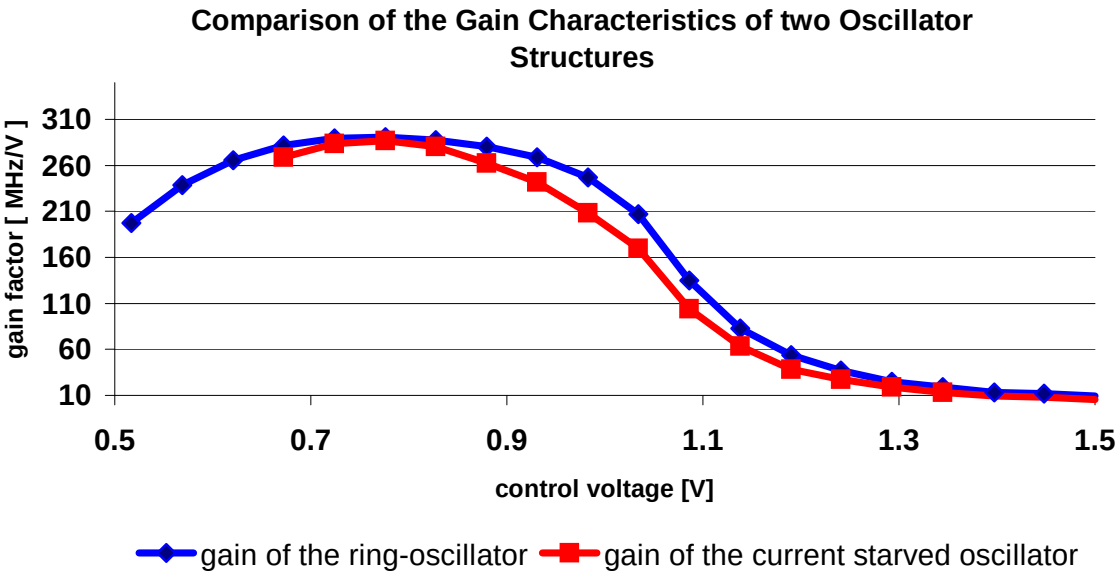


Figure 5.16: Comparison of gain curves of two oscillator structures. To compare both oscillator types the gain curves depending on the control voltage are shown.

reference level by the clock from ideal crossing location. The measurements were done by the digital storage oscilloscope (Tektronic DPO 7254) with a sample frequency of 2.5 GHz (40 GS/s, phase resolution=25 ps). The phase jitter histogram and the determined sample-standard deviation of the output phase jitter of the PLL are shown in Figure 5.17. Jitter can be quantified using the standard deviation of this distribution (RMS). The measurement in figure 5.17 is based on 1000 periods.

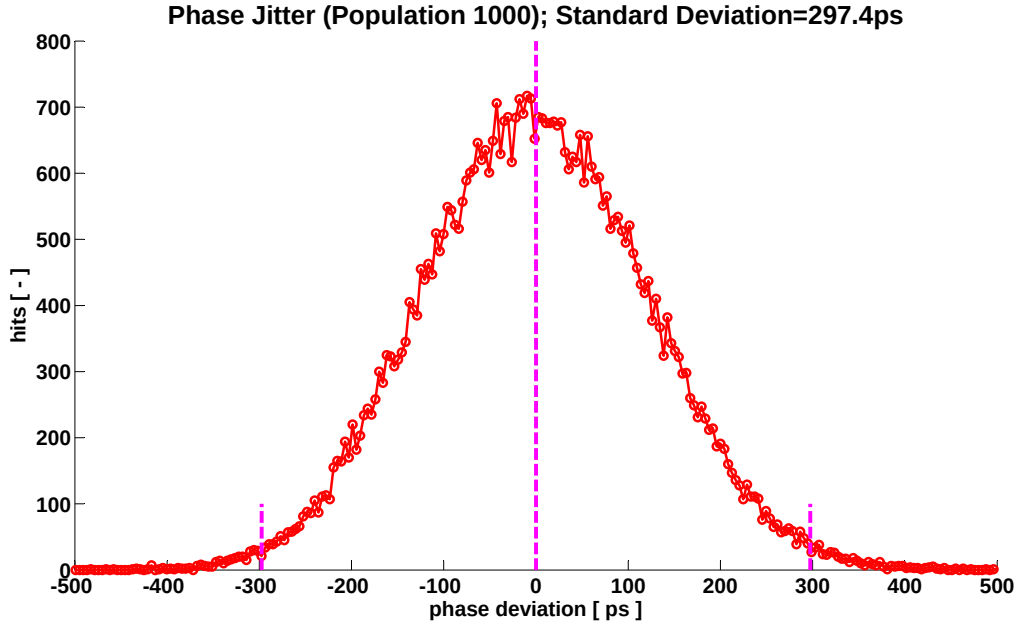


Figure 5.17: Measurement result - jitter of the current controlled oscillator. For performance analysis the phase jitter of the current controlled oscillator is measured. Furthermore the standard deviation is determined.

Another phase-jitter diagram is shown in figure 5.18. According to measurements the phase locked loop toggles between two states, the control loop is opened and closed. In this example the ”hold time” varies between $0.5\,us$ and $16\,us$. As can be seen in figure 5.18 the phase jitter is increasing with increasing hold time, because a frequency deviation occurs when the control loop is in hold mode. In the test chip I the hold mode is initiated by an analog non-synchronized signal.

For a defined hold mode the sync signal is synchronized with the PLL clock in the second test chip. Figure 5.19 shows the measured phase jitter performance of this case. As expected, lower jitter values can be achieved.

As already mentioned, the hold mode causes a phase and frequency drift, which is shown in figure 5.20.

The blue signal shows the measured frequency drop over time and the white one the average of the blue curve. First the PLL is locked. In the second step the PLL is switched to the hold mode.

The oscillation frequency of a ring oscillator can be calculated by equation 5.2. Here the number of inverter stages of the oscillator has no effect on the noise behavior at the same power consumption. The time delay can be adjusted by the capacitors between the inverter stages of the

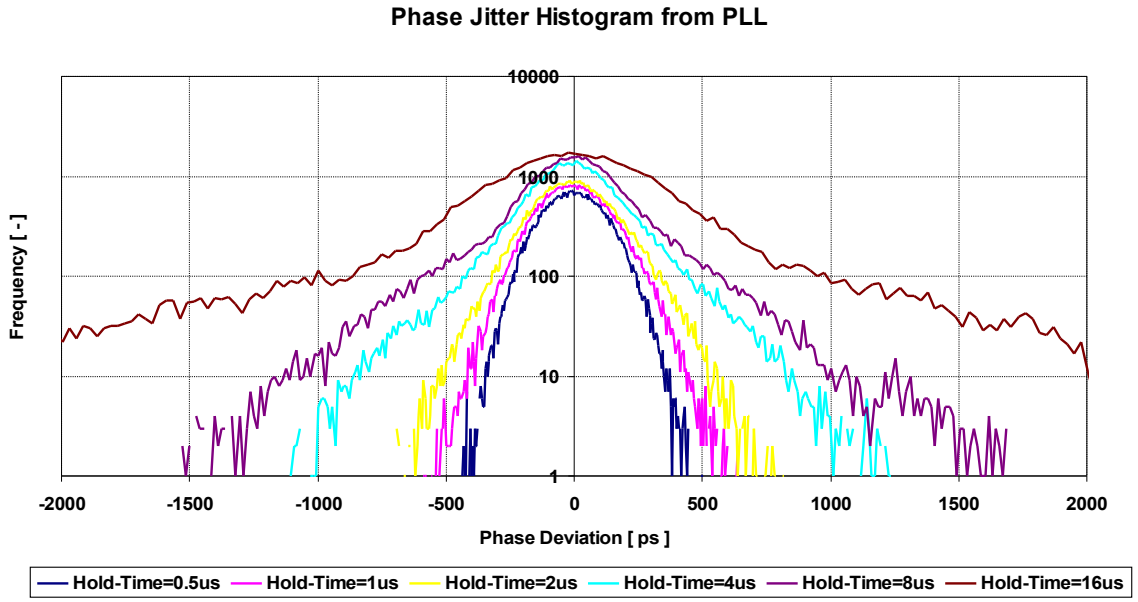


Figure 5.18: Phase jitter behavior of test chip I. The phase locked loop toggles between the states open and closed to verify the phase jitter behavior in this operating condition. In this histogram toggle frequencies of 31.25 kHz, 62.5 kHz, 125 kHz, 250 kHz, 500 kHz and 1 MHz are used.

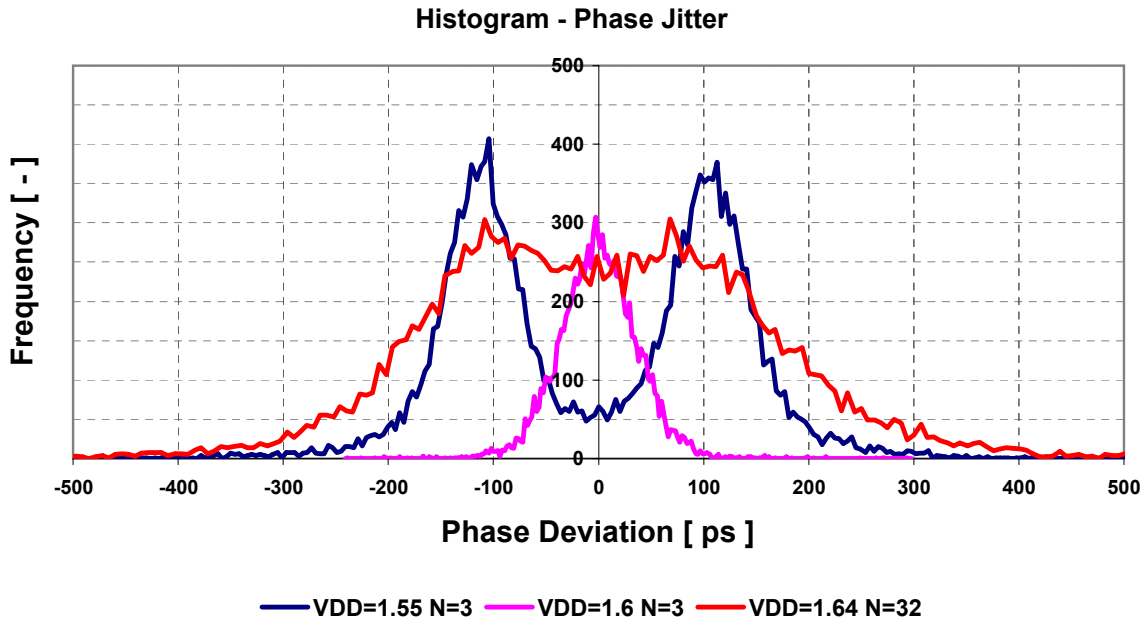


Figure 5.19: Phase jitter behavior of test chip II. To show the stability and the phase jitter characteristic of the test chip II different supply voltages and counter values are tested.

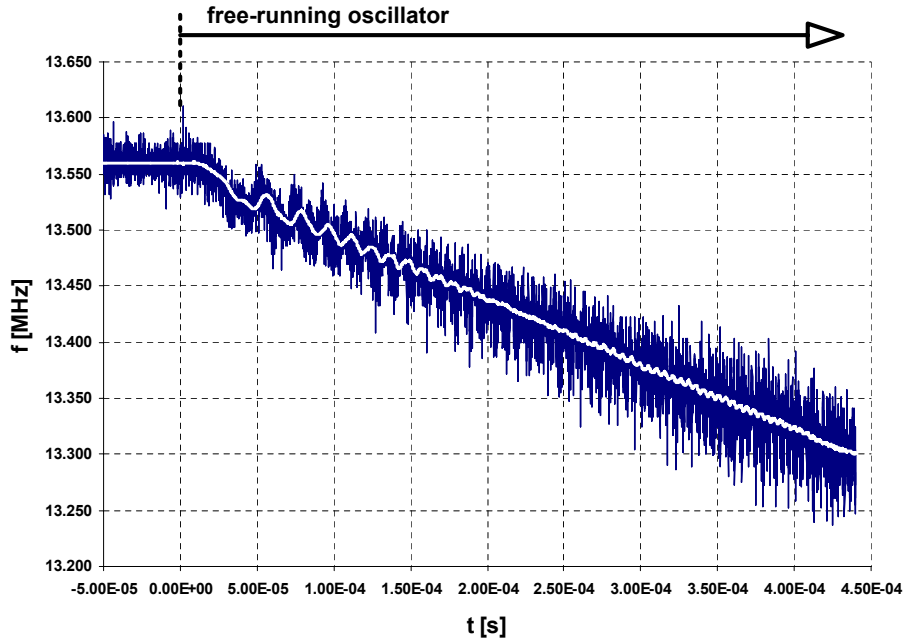


Figure 5.20: Frequency drift during hold mode. If the loop is not closed the PLL acts as a free running oscillator circuit with a frequency drift over time.

oscillator. To minimize the area consumption small capacitor values are chosen, so the parasitic capacitors of the transistors get a more important role.

$$f_{OSC} = \frac{1}{2 \cdot M \cdot T_d} \tag{5.2}$$

f_{OSC} Oscillation frequency

M Number of stages

T_d Time delay of a single inverter stage

The relationship between the current, the capacitor, the number of stages and the output frequency of the oscillator is:

current value $I_{DC} \uparrow$	**output frequency** $f_{OSC} \uparrow$
capacitor value $C_1 \ldots C_M \uparrow$	**output frequency** $f_{OSC} \downarrow$
number of stages $M \uparrow$	**output frequency** $f_{OSC} \downarrow$

5.3.3 Phase-Locked Loop Noise Spectra

Another important aspect is the noise behavior of the PLL [53, 31], whereby components of the PLL have a small but massive influence as far as noise is concerned.

Figure 5.21 shows a typical phase noise spectrum. At low frequencies the flicker-noise is dominating. For medium offset frequencies white-noise behavior becomes evident up to the point where the constant amplifier noise floor is the dominating one.
The most important noise sources of the phase-locked loop are the reference clock, the charge pump, the loop filter and the current-controlled oscillator [52]. The divider stage introduces a negligible noise in the feedback system.
There are three practicable types of oscillators, the ring oscillator, the relaxations oscillator and the LC oscillator. As the chip area minimization plays an important role, a low area consumption is desired. Due to the fact that the RC oscillators are usually much more compact than LC oscillators and as the relaxations oscillators have in principle no particular advantages at high frequencies compared to ring oscillators the ring oscillator was chosen for the proposed phase demodulator circuit. However the ring oscillators are also much noisier and consume more power than their counterparts. In case of the 13.56 MHz HF-field and low distances between the reader and transponder currents up to 20 mA are available for the analog front end (i.e. for the demodulator and the phase-locked loop).
The noise transfer functions of the charge pump, the reference and the divider stage have a low pass characteristic, the loop filter has a band pass characteristic and the voltage controlled oscillator a high pass behavior [16, 15]. To suppress the noise of the charge pump, the loop filter, the reference and divider stage, the PLL bandwidth should be as low as possible on the one hand and to minimize the ICO noise the PLL bandwidth should be as high as possible on the other hand. It is important that the PLL bandwidth is chosen very carefully to guarantee a phase margin greater than 45 degrees and a settling time of a few periods (≤ 8 periods).
The PLL is mainly affected by the noise of the reference signal (input signal) and the voltage/current controlled oscillator.

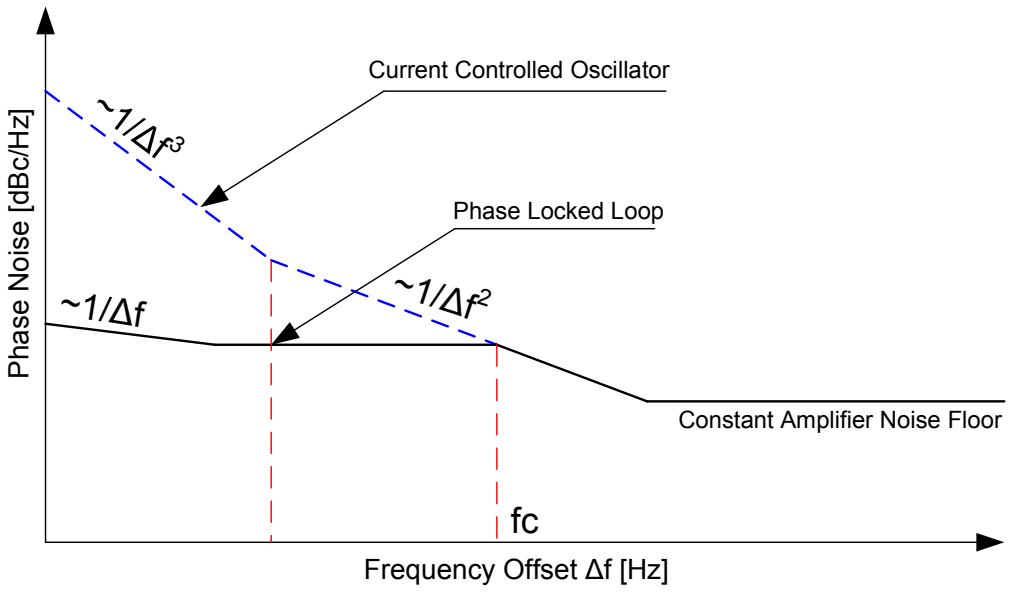


Figure 5.21: Noise spectra of the voltage-controlled oscillator and phase-locked loop

The classical design trade-off in PLL design is lock time vs. spurs. If you design the PLL for a narrow loop bandwidth, the spur levels look much better, but the lock time is degraded. If the loop

bandwidth increases, the lock time can be improved at the cost of the spur levels. In terms of phase noise, the only reason why the loop bandwidth is optimized for the demodulation process is the noise reduction of the ICO. It is important to have a low noise level for the demodulation process.

Power Spectral Density

The $L(f)$ plot gives the sideband noise distribution in the form of a power spectral density function in units of dBc. The total noise power of the sidebands can be determined by integrating the $L(f)$ function over the interesting band (equation 5.3). Furthermore, the RMS jitter is determined by equation 5.4. From this, the RMS Jitter can be calculated with the equations 5.3-5.5.

$$N = Noise\,Power = \int_{f1}^{f2} L(f)\,df \tag{5.3}$$

$$RMSPhaseJitter\,(radians) = \sqrt{10^{\frac{N}{10}} \cdot 2} \tag{5.4}$$

$$RMSJitter\,(sec) = \frac{Jitter\,(radians)}{2\pi \cdot fosc} \tag{5.5}$$

5.3.4 Phase Locked Loop Stability Consideration

An important aspect is the stability of the phase locked loop. It has to be guaranteed that the phase locked loop is stable in all possible conditions which are specified. To consider the stability of the phase locked loop a mathematical representation of the analog components of the phase locked loop was taken into account and a stability model for spice programs (shown in figure 5.22) was introduced.

Table 5.1 contains the dimensioning values of the stability model.

Table 5.1: Dimensioning of the spice model for stability consideration.

dimensioning values	
device	**size**
$C1$	$24\,pF$
$C2$	$2\,pF$
$R1$	$25\,k\Omega$
R_u2i	$10\,k\Omega$
V_5	$800\,mV$
$N0$	$600\,fF$

5.3.4.1 Stability - Spice Simulation Model

The simulation model includes the current charge pump (CP), a 2nd order filter (Filter2nO), a voltage to current converter (V-I), the current controlled oscillator (ICO) and a simplified current

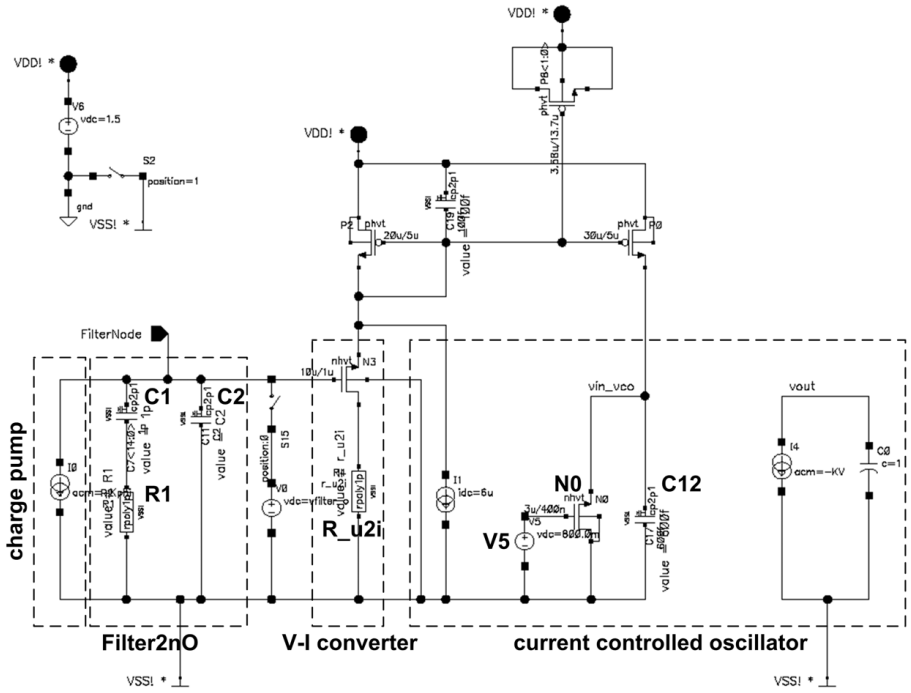


Figure 5.22: Simulation model for stability consideration [4] (Auer et al.,2010). A Spice model of the PLL was introduced to consider the loop stability including the parasitic capacitors.

mirror. The charge pump is emulated with an ideal current source, the 2nd order filter with two poly-poly capacitors C1, C2 and a resistor R1, the V-I converter with an n-channel transistor and a resistor R_u2i, the current controlled oscillator with a NMOS transistor N0, a capacitor C12 and operating voltage V5. The main advantage of such a simulation model is the inclusion of parasitic capacitors of passive and active devices.

The results of the simulation model in Figure 5.22 are shown in Figure 5.23. These simulation results show almost the same characteristics as the Matlab simulation results, which have been described before. They show the amplitude and frequency characteristics of the open loop system with a phase margin (PM) of 52 degrees, which means that the system stability is assured.

5.3.4.2 Stability - Mathematical Model

A mathematical model has been used for stability consideration to validate the spice model and for further stability discussions. Figure 5.24 shows the theoretical aspects of the enhanced PLL concept. I_P is the charge pump current and G_{LPF} defines the transfer function of the filter structure that was used. The current controlled oscillator (ICO) has an integrated behavior, which is described by the transfer characteristic $\frac{K_{ICO}}{s}$. The important aspects in respect of the stability of the phase locked loop are the transfer function of the filter structure, the PFD/CP gain and the ICO gain factor. In this context the AC model was designed and simulated in Matlab R2700b (Sisotool). The stability can be discussed by using the root-locus diagram, the bode diagram, the step response, and a combination of these possibilities of visualizing and analyzing. The root locus technique shows the closed-loop pole trajectories in the complex plane when k (gain factor) varies. Additionally, a bode magnitude plot and a bode phase plot can be used to show

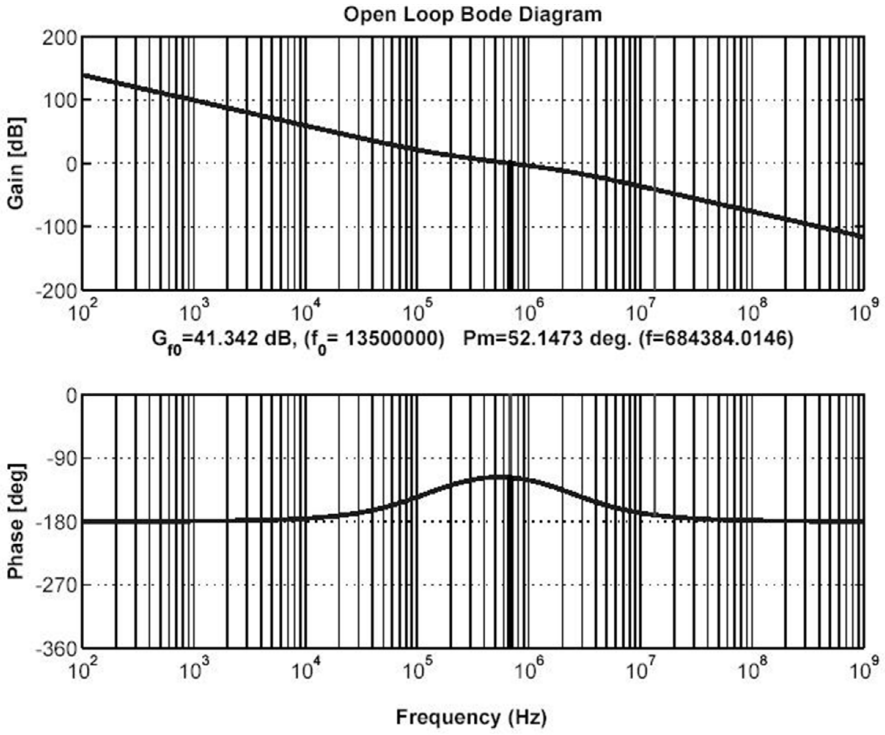


Figure 5.23: Bode diagram simulated in Cadence based on the circuit in figure 5.22.

the transfer function and frequency response. A system is stable if all its poles are in the left half of the s-plane for the continuous system.

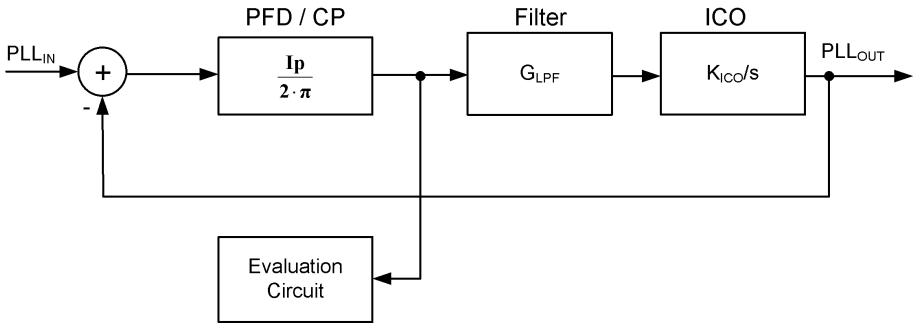


Figure 5.24: Mathematical model of the PLL. For theoretical considerations of stability a mathematical model with the essential PLL components has been introduced.

A simplified block diagram of the mathematical model is given in figure 5.25. The figure includes three sub-blocks C,G and H:

C Chargepump and phase frequency detector

G Lowpass filter and current controlled oscillator

H Frequency divider

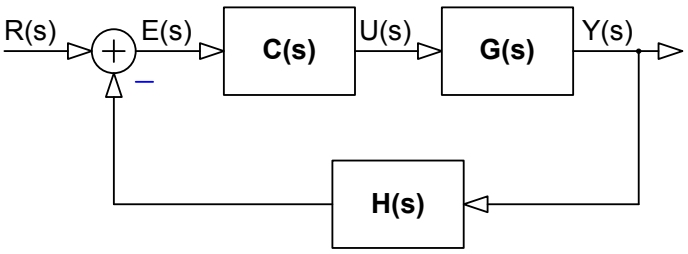


Figure 5.25: Block diagram for stability analysis. Edge block stands for a combination of PLL components. The mathematical representation of the output y to the input r are given in the equations 5.6, 5.7 and 5.8.

The formula derivation of the closed loop system 5.12 can be seen in equations 5.6-5.8.

$$Y(s) = G(s) \cdot U(s) \tag{5.6}$$
$$U(s) = C(s) \cdot E(s) \tag{5.7}$$
$$E(s) = R(s) - H(s) \cdot Y(s) \tag{5.8}$$

$R(t)$ stands for an incoming modulated rectangle signal, $e(t)$ for the PFD input signal and $y(t)$ for the phase locked loop output signal. Furthermore, the equations 5.6-5.8 can be enhanced with equations 5.9-5.10. The equations include the passive filter devices C_1, C_2 and R, where capacitor C_1 and resistor R are in series and capacitor C_2 is parallel to this series connection.

$$C(s) = \frac{I_P}{2 \cdot \pi} \left[\frac{A}{rad}\right] \tag{5.9}$$
$$G(s) = \frac{s \cdot (C_1 \cdot R) + 1}{s^2 \cdot (C_1 \cdot C_2 \cdot R) + s \cdot (C_1 + C_2)} \cdot \frac{K_{ICO}}{s} \tag{5.10}$$
$$H(s) = \frac{1}{N} \tag{5.11}$$

This second order filter is preferable for a fully integrated loop filter, because the bottom plates of C_1 and C_2 are both grounded. Due to this filter arrangement a possible substrate noise coupling via the capacitor C_2 into the filter output node has been completely eliminated. Thus the tuning voltage is less affected by the substrate noise and the noise influence of the oscillator decreases.
The charge pump and the phase frequency detector can be described by equation 5.9. Equations 5.10 and 5.11 stand for the mathematical representation of the passive filter, the current controlled oscillator and the frequency divider block. Different filter structures were taken into account, and as the result a second order filter structure was chosen. The zero of the transfer function 5.10 is at $-\frac{1}{R \cdot C_1}$ and the poles are at $zero$ and $-\frac{C_1+C_2}{R \cdot C_1 \cdot C_2}$. An additional pole exists at $zero$ due to the current-controlled oscillator transfer function. The centre of the circle is at $-\frac{1}{R \cdot C_1}$, and the radius equals $\frac{1}{R \cdot C_1}$. Capacitor C_2 suppresses high frequency components due to a current switching of the charge pump mechanism.

Finally, the closed loop system can be described by equation 5.12:

$$T_{CLOSED} = \frac{Y(S)}{R(S)} = \frac{G(s) \cdot C(s)}{1 + H(s) \cdot G(s) \cdot (C(s)} \tag{5.12}$$

$$= \frac{I_P \cdot K_{ICO} \cdot N \cdot (C_1 \cdot R \cdot s + 1)}{I_P \cdot K_{ICO} + C_1 \cdot I_P \cdot K_{ICO} \cdot R \cdot s + (2\pi \cdot C_1 \cdot N + 2\pi \cdot C_2 \cdot N) \cdot s^2 + 2\pi \cdot C_1 \cdot C_2 \cdot N \cdot R \cdot s^3} \tag{5.13}$$

For further stability consideration the bode diagram 5.26 and the root locus has been taken into account. To avoid instability of the phase locked loop the filter components are automatically adapted.

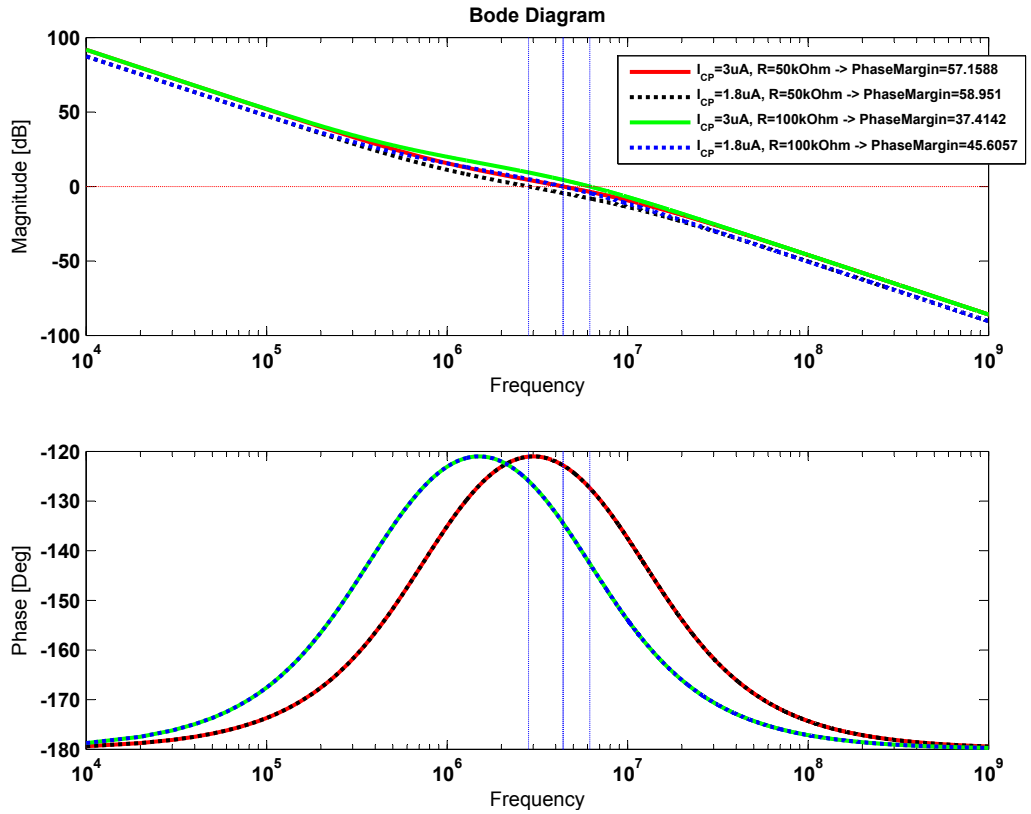


Figure 5.26: Bode diagram of the PLL, simulated in Matlab. The counter value can be defined with 5 input bits (maximum division factor = 32). Thus, the phase locked loop can become unstable for certain division factors. As a workaround, the loop components can be changed simultaneously to increase the phase margin. In this regard, the current through the current charge pump, the gain factor of the oscillator and the loop filter components are optimized.

The root locus of the proposed design is shown in figure 5.27. The root locus characterizes a curve of the pole location of a transfer function when the gain K varies. With this method it can be verified when the poles are in the left hand plane of the root locus, which indicates a stable behavior.

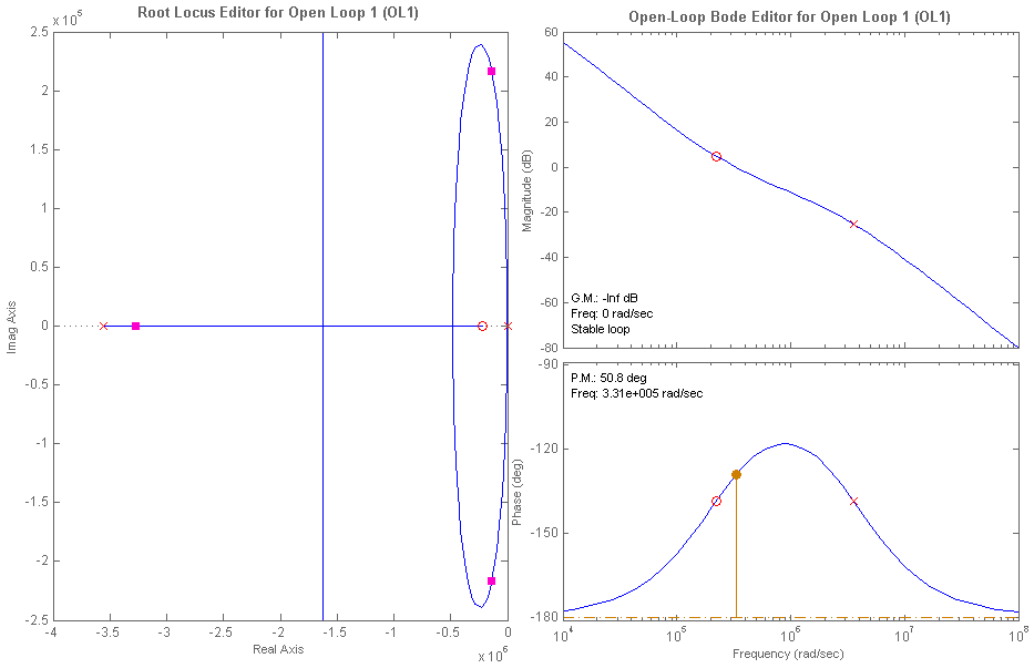


Figure 5.27: Root locus and bode diagram for the open loop to verify the stability of the PLL.

5.3.4.3 Transimpedance

There will be also some stray resistance at the phase locked loop filter node. This stray resistance results from the leakage of the components, the substrate leakage and the finite current-source output impedance of the charge pump circuit. The leakage current mostly depends on the voltage level at the V/I converter and the impedance of the current sources, which can change dynamically, depending on its on/off state. In the proposed demodulation architecture the transimpedance plays an important role, because the hold-mode that was introduced. In hold mode operation the leakage current must be kept as low as possible. To minimize the substrate leakage an n-channel transistor with an active well has been used.
This leads to another important point of discussion, the consideration of spurious effects on the filter node. The filter node is influenced by the leakage current of the loop filter components and the mismatch of the current sources of the charge-pump.
There are several types of leakage current in the proposed system, such as the capacitor C_1 itself, the input transistor of the voltage to current converter and the current charge pump output. The mismatch in the charge-pump results in different types of devices for the current sources. The N-type current source sinks the current from the output node to the ground and the P-type current source sources current from the supply to the filter node. As a result of mismatch effects and different types of transistors both current sources do not generate exactly the same current value.

5.3.4.4 Phase Margin - Phase Locked Loop

For the design of the loop parameters the open loop bandwidth fc and the phase margin Φm play an important role for the phase demodulator. The open loop bandwidth or 0 dB cross-over frequency is defined in equation 5.14 and the phase margin in equation 5.15.

$$|G(j2\pi fc)| = 1 \tag{5.14}$$

$$\Phi m = arg(G(j2\pi fc)) + \pi \tag{5.15}$$

It has to be guaranteed that the phase demodulator is stable in all specified operation points. The stability depends on the loop filter components, the gain factors from the current controlled oscillator, and the current charge pump. Several typical parameters have been varied (figure 5.28) to test the stability behaviour of the phase demodulator.

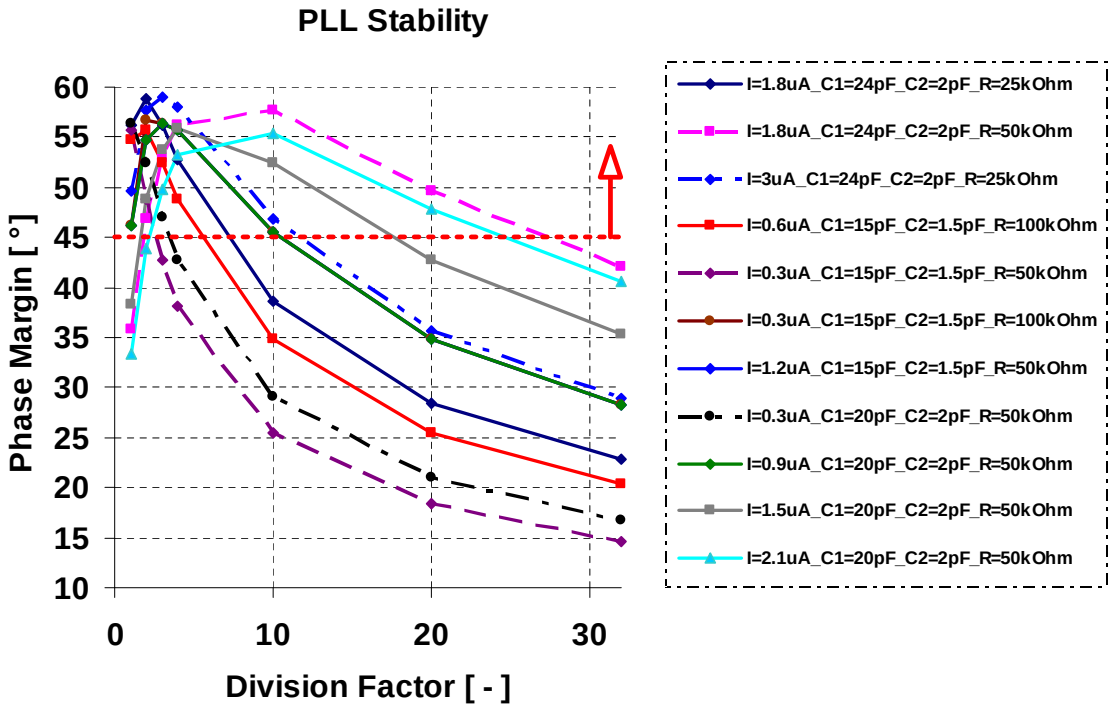


Figure 5.28: Stability overview. Component sweep and corresponding phase margin. As already mentioned in figure 5.26 the loop components can be varied to maximize the phase margin at different counter settings. Here the charge pump current I, the capacitor values C_1 and C_2 and the resistor R are changing.

The diagram shows the phase margin over the division factor at different component settings. It can be seen that the phase margin decreases over the division factor N of the divider. This means that the PLL gets unstable with a higher division factor N. It has to be guaranteed that the phase margin is greater than 45 degrees to be resistant against the effect of process variations. Consequently, the phase of the transfer function can be calculated by equation 5.19.

$$\tau_2 = R_1 C_1 \tag{5.16}$$

$$\tau_3 = R_1 \frac{C_1 C_2}{C_1 + C_2} \tag{5.17}$$

$$\Phi(j\omega) = -\pi + \arg(1 + j\omega\tau_2) - \arg(1 + j\omega\tau_3) \tag{5.18}$$

$$= -\pi + \arctan \omega\tau_2 - \arctan \omega\tau_3 \tag{5.19}$$

Furthermore, the position of the frequency of maximum phase advance is calculated by equation 5.20.

$$\omega_{max} = \sqrt{\frac{1}{\tau_2 \tau_3}} \tag{5.20}$$

So the value of the maximum phase advance can be determined by equation 5.21, depending on the filter parameters that can be calculated as a function of τ_2 and τ_3.

$$\Phi_{max} = \arctan \frac{\tau_2 - \tau_3}{2\sqrt{\tau_2 \tau_3}} \tag{5.21}$$

If ω_c is dimensioned to be equal to ω_{max}, then the phase margin Φ_m equals the value of Φ_{max} given in equation 5.21.

Thus the PLL open-loop bandwidth can be determined by equation 5.22. Moreover, the open-loop bandwidth depends on the current of the current charge pump circuit I_{CP}, the gain factor of the oscillator K_{ICO}, the divider factor N and the filter components R_1, C_1 and C_2.

$$\omega_c = \frac{I_{CP} K_{ICO}}{N} \cdot R_1 \cdot \frac{C_1}{C_1 + C_2} \tag{5.22}$$

5.3.5 Transient Response

Besides of stability the step response of the phase-locked loop module (figure 5.29) is another important factor.

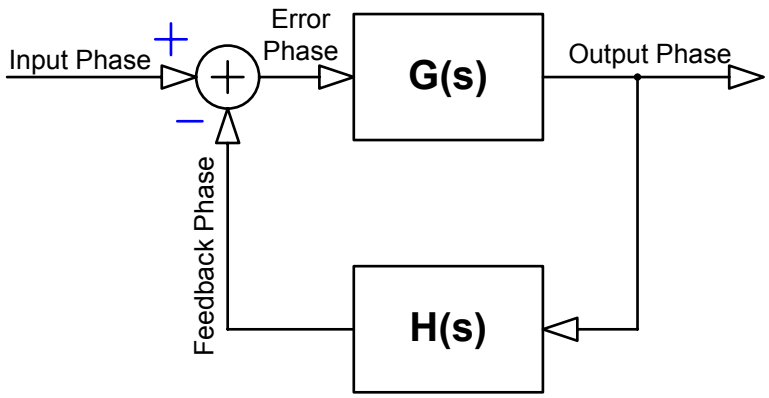


Figure 5.29: Closed loop system. A simplified model of the phase loop is given. It reflects the flow of the phase information.

Several step responses for different settings are shown in Figure 5.30.

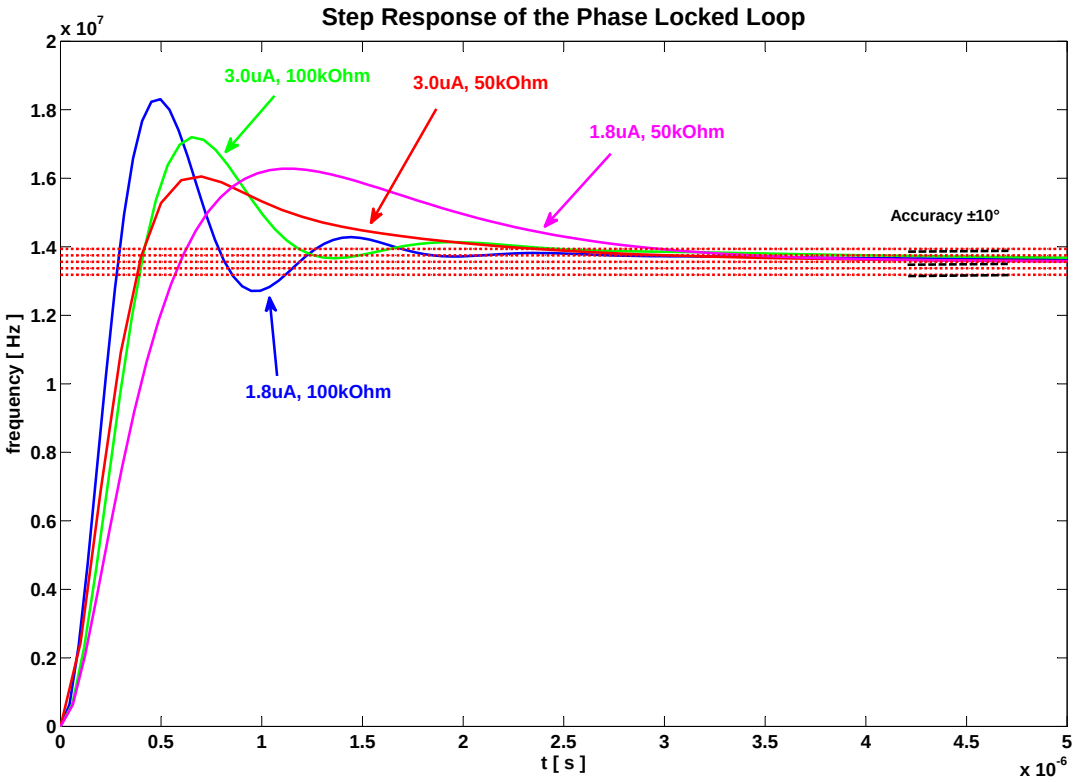


Figure 5.30: Simulated step response. Based on the step response the settling behavior and stability of the PLL can be discussed. It can be seen that different loop parameters result in different settling behaviors.

Because of the initial phase jump it is important to keep the settling time of the phase locked loop as small as possible. But there are several trade-offs between the settling behavior, the phase-locked loop stability and the power consumption. It is not possible to increase the current through the charge pump or choose another value for the loop filter components without a change in stability. In figure 5.31 the settling behaviour of the PLL at different current values of the current charge pump is shown. The measurement results show the transient response of the PLL at charge pump currents ICP of $75\,nA$, $675\,nA$, $1.275\,\mu A$ and $1.875\,\mu A$. It can be seen that if the charge pump current increases, the settling time becomes smaller.

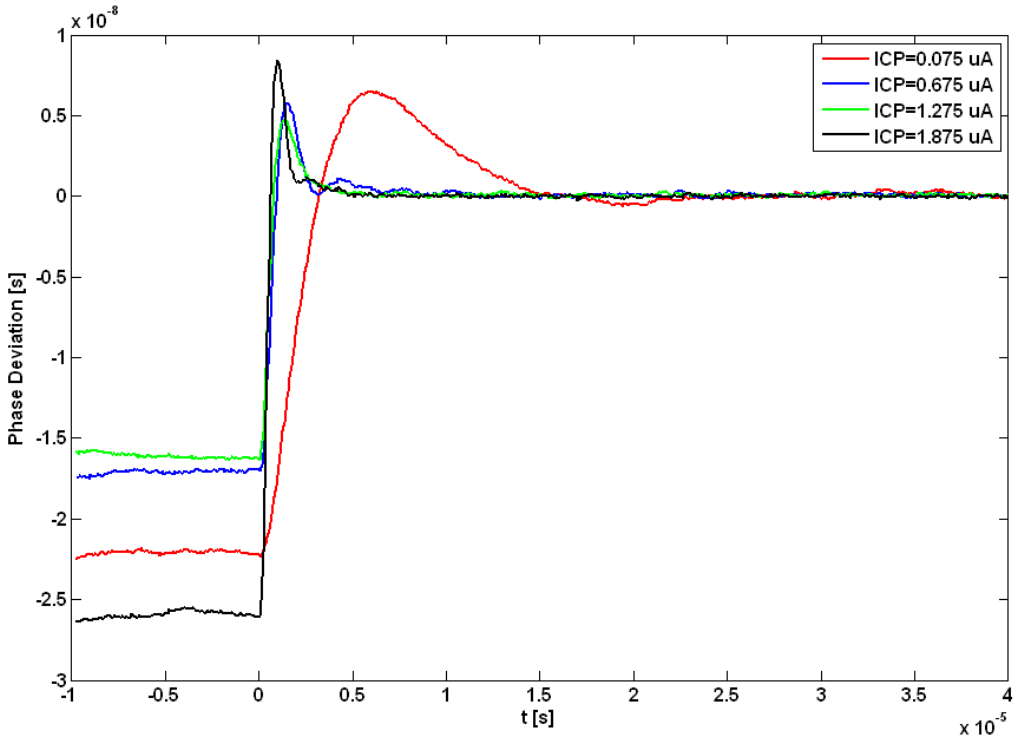


Figure 5.31: Step response (measurement). Step response at different current values of the PLL charge pump (measurement). If the current increases, the settling time decreases.

5.3.6 2-State Phase Detector

In the following, the 2-state phase detector of the proposed phase demodulator is discussed in detail. The basic idea of the 2-state phase detector is that the phase modulated input signal is compared by two phase detectors in an alternate operating mode. The main advantage of this system is that it allows higher detection rates than common phase detectors.
The phase deviation due to the phase modulated signal between signal $\mathrm{HF_{SIGNAL}}$ and $\mathrm{Osc_{OUT}}$ (see the overall block diagram in figure 5.10) is detected by the phase detectors. The phase detector implementation which is shown in Figure 5.32 contains a phase-frequency detector, a current charge pump, a voltage divider with resistors $\mathrm{R_1}$, $\mathrm{R_2}$ and bias current $\mathrm{I_{REF}}$, a switch $\mathrm{S_1}$, a window comparator with an operational amplifier, resistors R, an adjustable bias current and comparators.

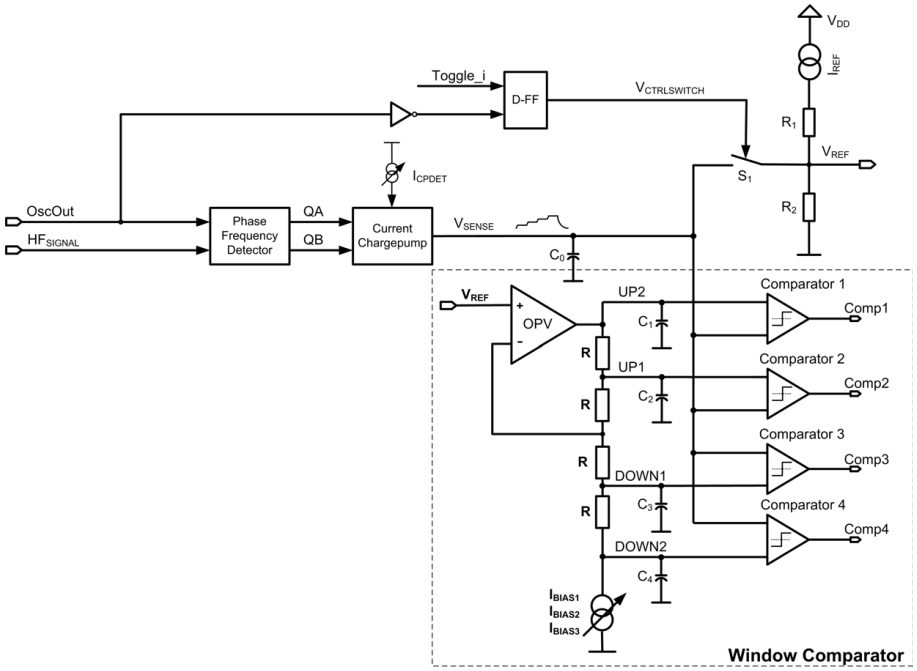


Figure 5.32: 2-state phase detector circuitry. For data recognition a 2-state phase detector circuit has been implemented with a window comparator stage. The circuit is able to detect positive and negative phase jumps.

A phase-frequency detector (PFD) compares the reference input with the feedback of the phase-locked loop until the PLL is locked. If there is no phase modulation at the input, the $\mathrm{HF_{SIGNAL}}$ and the $\mathrm{Osc_{OUT}}$ have the same frequency and are in phase. If a phase change occurs at the input $\mathrm{HF_{SIGNAL}}$, the frequency and phase of the clock signal $\mathrm{Osc_{OUT}}$ remain still constant during the data frame.
The sensitivity of the phase-locked loop can be adjusted by a current $\mathrm{I_{CP}}$ through the current charge pump. The current charge pump sources or sinks an amount of current into the capacitor $C0$ depending on the clock inputs QA and QB (Switch $\mathrm{S_1}$ is closed). If QA and QB have the same synchronized sequence, the current charge pump sinks and sources the same amount of current into the capacitor $C0$, so that the voltage at node $\mathrm{V_{SENSE}}$ stays constant. At first the voltage at node $\mathrm{V_{SENSE}}$ is held at voltage $\mathrm{V_{REF}}$ by the voltage divider (resistors $\mathrm{R_1}$ and $\mathrm{R_2}$).

$\mathrm{V_{REF}}$ is used to generate several voltage levels above and below the reference voltage. The voltage window is generated by an operational amplifier and a current source $\mathrm{I_{BIAS}}$. Equation 5.23 shows the dependency between the voltage variation at node $\mathrm{V_{SENSE}}$ and the input phase difference. Here, the parameter Kd represents the gain factor of the current charge pump.

$$\Delta V = Kd \cdot (\varphi i - \varphi a) \tag{5.23}$$

If a phase change occurs at input $\mathrm{HF_{SIGNAL}}$, the phase deviation can be seen at node $\mathrm{V_{SENSE}}$ as a voltage deviation as a result of the loading mechanism of the current charge pump.
If the voltage at $\mathrm{V_{SENSE}}$ exceeds the threshold voltages of the window comparator at node UP1 (comparator 1) or UP2 (comparator 2), it outputs a ONE and a positive phase jump has been detected. On the contrary, if the voltage at node $\mathrm{V_{SENSE}}$ falls below the voltage at DOWN1 or DOWN2 of the window comparator, the comparator 3 or comparator 4 outputs an ONE and a negative phase jump has been detected.
The current flowing through the current charge pump and the capacitor $C0$ are the most interesting design parameters for the phase detector. The sensitivity of the phase detection is increased by a higher current from the current charge pump, a lower capacitor value and a lower current through the voltage divider stage. $C0 \cdot \Delta \mathrm{U_{VSENSE}} = \mathrm{I_{CPDET}} \cdot \Delta t$ shows the relationship between the charge pump current $\mathrm{I_{CPDET}}$, the voltage deviation at node $\mathrm{U_{VSENSE}}$ and the capacitor $C0$. For small phase changes switch $\mathrm{S_1}$ can be opened by the digital input signal $\mathrm{V_{CTRLSWITCH}}$ during a phase change. At the end of this phase change switch $\mathrm{S_1}$ is closed by the digital input, and the voltage at node $\mathrm{V_{SENSE}}$ settles again to the reference voltage $\mathrm{V_{REF}}$. The start of such a detector operation can be initiated by a phase calibration process with an input pattern. This calibration process includes a configuration of the voltage window size and the charge pump current depending on the actual noise at node $\mathrm{V_{SENSE}}$. To increase the detection speed two phase detectors which are controlled by a digital signal $\mathrm{V_{CTRLSWITCH1}}$ and an inverted signal $\mathrm{V_{CTRLSWITCH2}}$ sent by the transponder FPGA were implemented. Due to the alternate operating mode of the two phase detector circuits the time constant at node $\mathrm{V_{SENSE}}$ is canceled. Thanks to this cancellation it is also possible to extract bit streams with bit rates of up to 13.56 Mbit/s.

The reference voltage V_{REF}, the sense voltage V_{SENSE} and the UP/DOWN reference voltages V_{UP} and V_{DOWN} of the phase detector in Figure 5.32 are shown in figure 5.33.

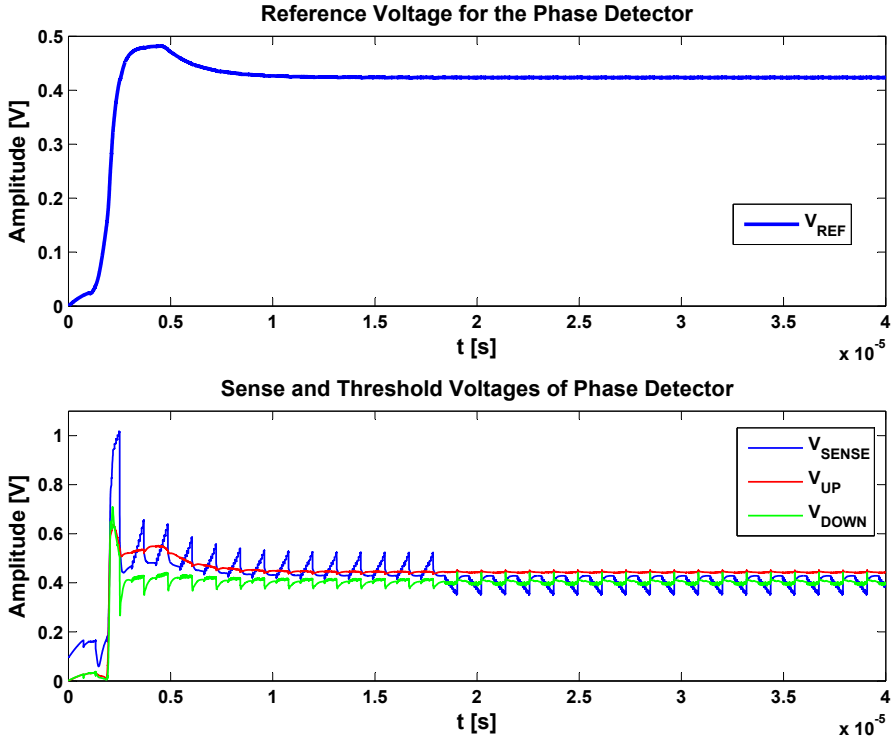


Figure 5.33: Signals of a phase detector. The signals of the phase detector during data transmission and the corresponding reference voltage are shown. If the voltage V_{SENSE} exceeds the threshold voltage V_{UP} or V_{DOWN}, a phase change has been detected.

The reference voltage V_{REF} of the bias cell settles in a few micro seconds to a desired bias voltage. Voltages V_{UP} and V_{DOWN} are generated from the reference voltage V_{REF}. If the sense signal crosses one of the two reference signals, the comparator output is high.

The FPGA test-board emulates the digital part of the transponder chip. It receives the PLL output signal which serves the reference clock and the eight phase demodulator output signals - four outputs of each of the two phase detectors. All FPGA measurements were done by SignalTap®[8] Software.

The reader transmits the phase modulated bit stream (Figure 5.34b) which is evaluated by the phase demodulator. In this measurement the phase jumps are set to 5 degrees.

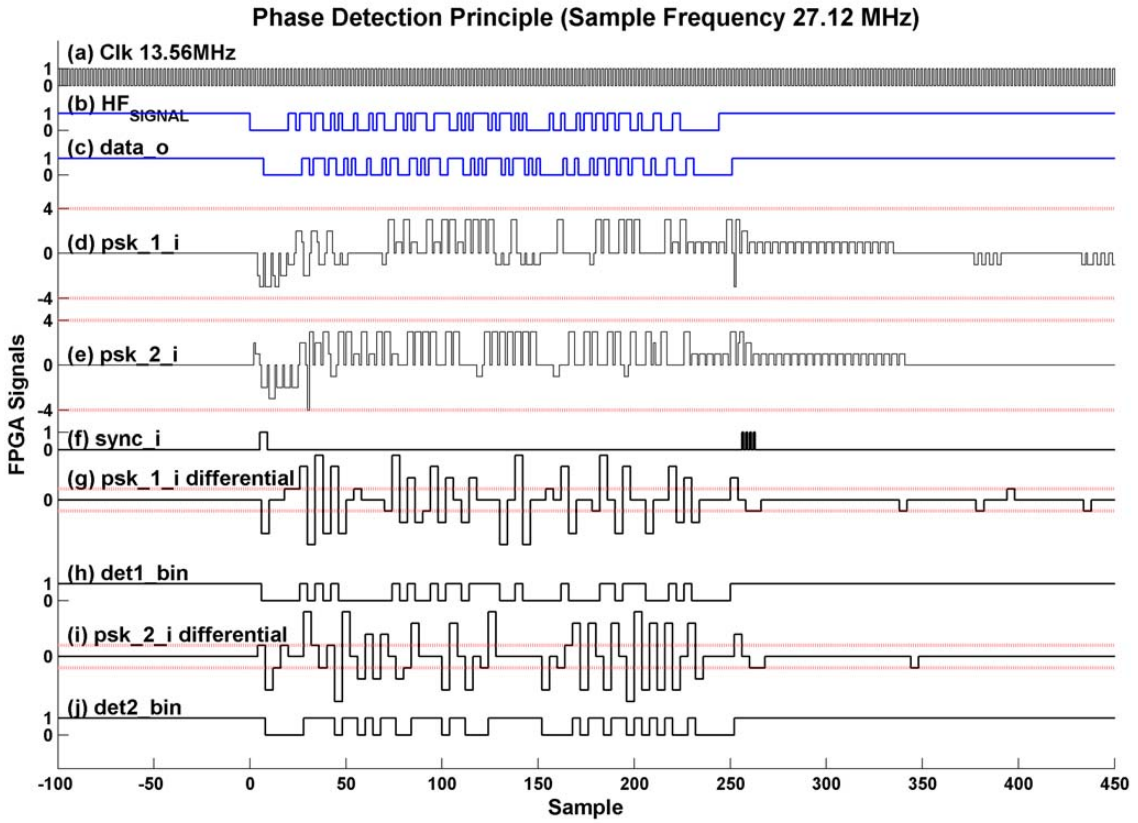


Figure 5.34: Phase detection principle for 13.56 MBit/s. Signal processing flow which is necessary to extract the baseband data from the phase modulated input signal.

A phase change of 5 degrees equals 1.25 ns in time scale at a carrier frequency of 13.56 MHz. The ADC outputs of both phase detectors are shown in Figures 5.34 d-e.
Furthermore, the comparator outputs were sampled with the PLL output frequency of 27.12 MHz. The signals $psk\_1\_i\,differential$ and $psk\_2\_i\,differential$ (Figures 5.34g and 5.34i) are the derivatives of signals psk_1_i and psk_2_i.
The derivatives are compared with a threshold of ± 1 and the results are displayed in figures 5.34h and 5.34j ($det1\_bin$, $det2\_bin$).
The final result $data\_o$ is shown in figure 5.34c. It is computed with the help of the signals $det1\_bin$ and $det2\_bin$. The figure shows the detected data stream that equals the sent one (see figure 5.34b). The measurement results show that the phase demodulator is able to detect phase changes equal and greater than 5 degrees with a data rate up to 13.56 Mbit/s. A bit rate of 13.56 Mbit/s reduces the bit time to 74 ns, which equals one period/bit at a carrier frequency of 13.56 MHz.

Figures 5.35a-5.35g show the constant 13.56 MHz reference clock Osc_{OUT}, the incoming phase-modulated signal HF_{SIGNAL} with the reference bit REF, the $V_{CTRLSWITCH}$ and the V_{SENSE} of both phase detectors as well as the phase locked loop synchronization signal $Sync$.

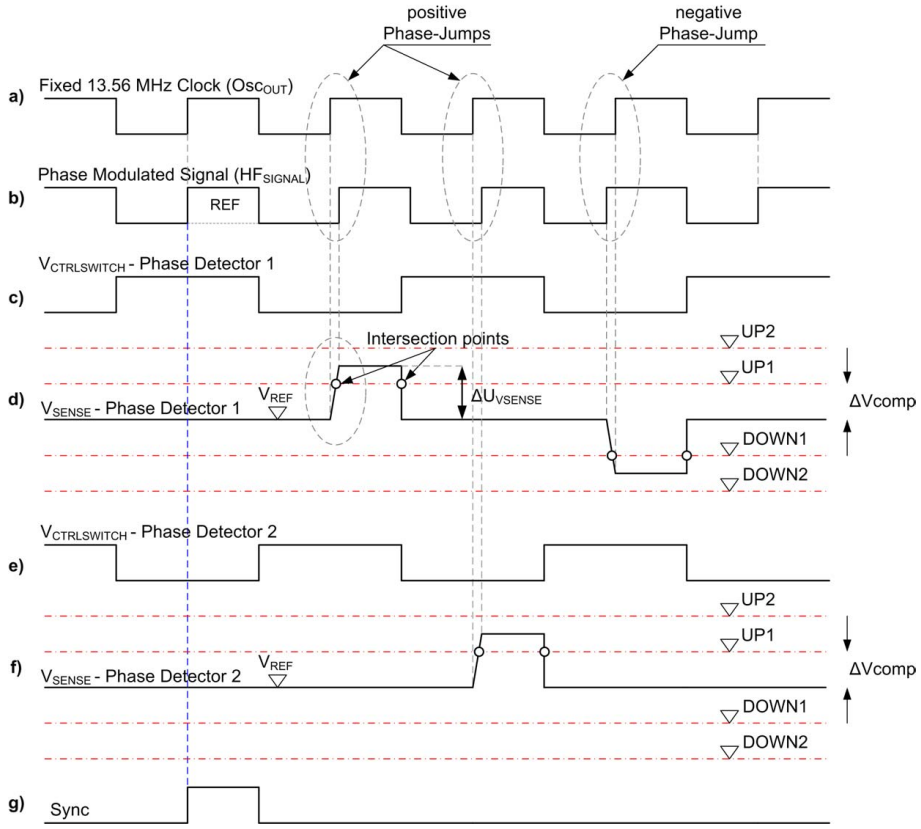


Figure 5.35: Phase detector principle. In order to explain the phase detector principle the important and interesting signals are shown in detail.

A stable reference clock, which is independent of the incoming phase-modulated signal, is generated by the phase-locked loop. The counter divisor N is set to $N = 32$ in figure 5.35. $V_{CTRLSWITCH}$ is used to connect and disconnect the node voltage V_{SENSE} from the reference voltage. Switch $S1$ toggles with the half bit frequency to get a maximum voltage deviation at the capacitor Cap (node voltage V_{SENSE} of both phase detectors in figures 5.35d and 5.35f). The voltage deviation is compared to several reference voltages at a voltage distance of ΔV_{COMP}. In closed mode the voltage at node V_{SENSE} is set to V_{REF} (operating point). To ensure that the reference clock of the phase-locked loop is stable during a phase change, the synchronization of the PLL is of particular importance. The rising edges of the synchronization clock are used as the reference points of the incoming data frame. Additionally, the counter must be configured to the frame length of the incoming signal. This means the phase locked loop is N periods in the hold mode, which causes a phase drift. In order to reach a phase drift minimization the maximum frame length was set to 32 carrier periods.

5.3.7 Evaluation Circuitry

In the chapter 5.3.6 the 2-state phase detector was explained in detail. In order to expand the 2-state phase detector to a multi-level phase detection circuit the circuit in figure 5.36 is discussed. It shows the most obvious way to implement a multi phase-level detection circuit on the basis of previous discussions.

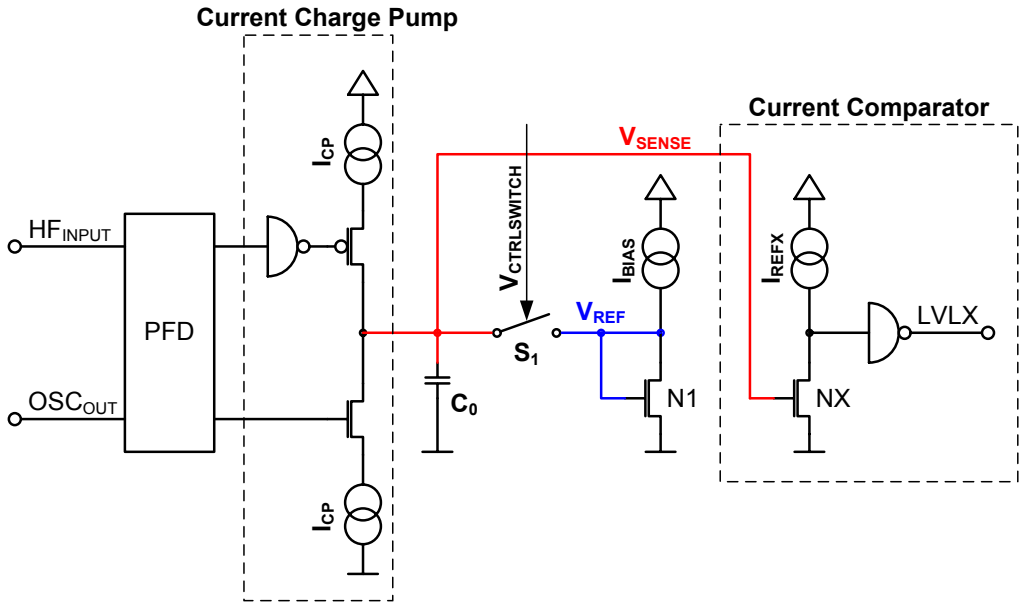


Figure 5.36: Evaluation circuitry. The evaluation circuit represents one stage of the analog to digital converter that was used. Some of those stages are connected in parallel to form a multi phase level detection circuit.

The circuit uses the incoming signals HF_{INPUT} and OSC_{OUT} from the phase locked loop to convert the phase information plus the phase error into a binary word. To extract the data, a phase-frequency detector, a charge pump circuit, a hold mechanism and a current comparator are implemented. The current charge pump and a capacitor C_0 are used to convert the phase information into the voltage domain. Additionally, with the implementation of a hold mechanism the voltage at node V_{SENSE} can be increased. A current comparator makes the threshold decision. An array of this current comparators is integrated to get a high detector resolution. The number of current comparators is limited by the comparator offset and the phase error of the PLL. One drawback of this phase detector is the quadratic dependency between the phase information and the output signal $LVLX$ due to the transistor NX. An improved multi phase level detection circuit with X chargepump stages is shown in figure 5.37. The PFD outputs pulses depending on the input signals HF_{INPUT} and OSC_{OUT}. The short output pulses control the charge pump array. Each charge pump stage has its own bias current value. The bias currents ($I_{CPP1} = I_{CPN1} \ldots I_{ICPPX} = I_{CPNX}$) are weighted in a linear way. Due to this method the current phase detector does not allow a linear relationship between the phase deviation of the incoming signal and the detected output pulses of the phase frequency detector. Thus, this phase detector is only suitable for the detection of a few phase states. In the next chapter, another method is presented which allows a better relationship between the phase deviation at the input and the ADC output value.

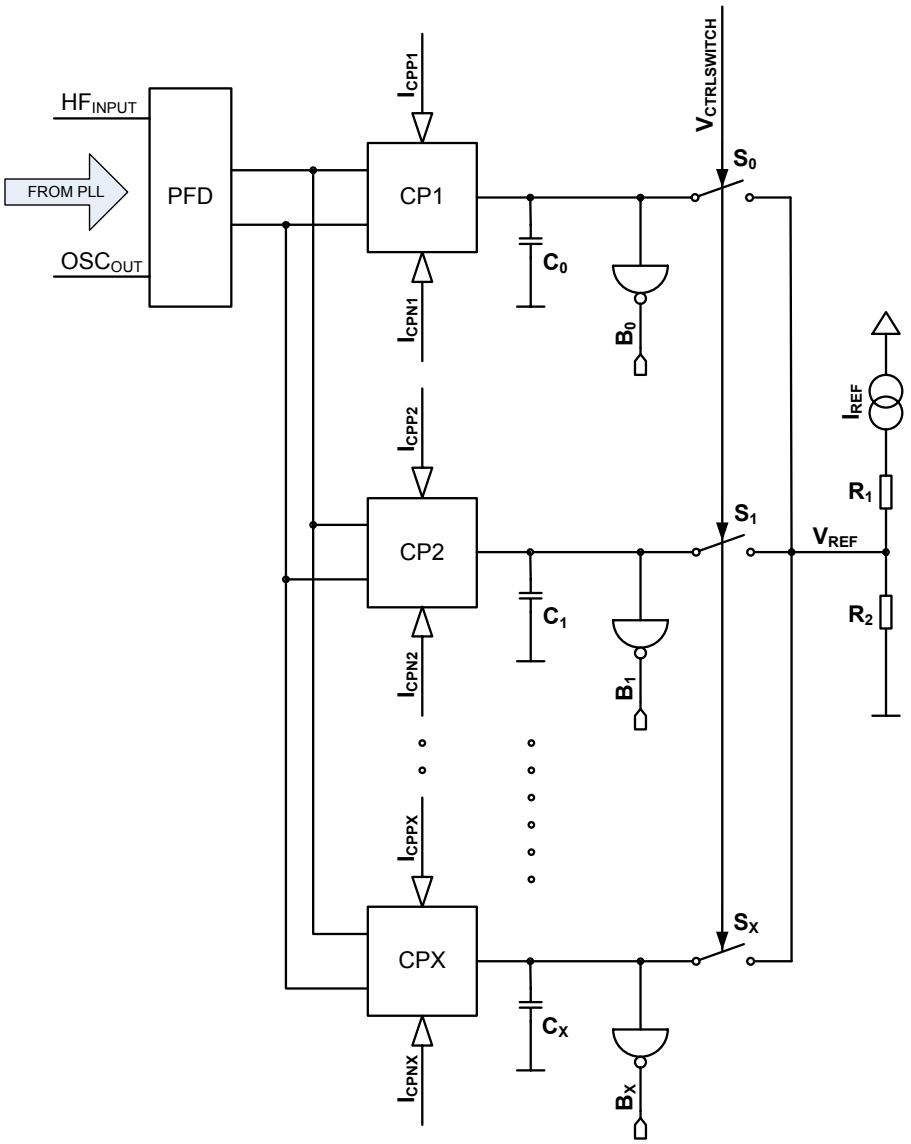


Figure 5.37: Multi level phase detection circuit. A further possible way to implement a phase detection circuit for multi level phase detection is a charge pump array in parallel connection. Each current charge pump has its own current sources to sink and source an amount of current into the respective capacitor $C_0 \cdots C_X$. The current values are weighted with the function $\frac{1}{x}$ to achieve a linear dependency between the phase information and the output voltage. Additionally, a voltage divider with resistors R_1 and R_2 defines the operation voltage V_{REF}. This voltage is the starting point for the detection cycle.

5.4 Proposed Multilevel Phase Detection Circuitry

In the previous chapter 5.3 a proposed phase demodulator has been discussed for bit rates up to 13.56 Mbit/s. This proposed phase demodulator is based on a two-state phase jitter modulation [55]. In order to increase the bit rates above 13.56 Mbit/s a multi-level phase jitter modulation is presented in this chapter. To demodulate the M-PSK input signal a phase detector circuit with an ADC is needed.
Figure 5.38 shows the block diagram of the phase detector including the phase frequency detector, the pulse generator, the ADC and the thermometer to binary decoder.

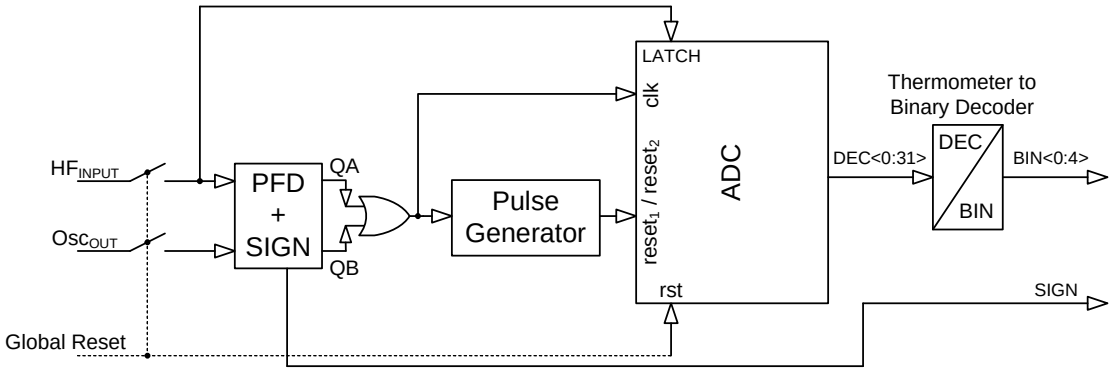


Figure 5.38: Block diagram of the phase detector with an 5-bit ADC (part of test chip III). The phase detector is one of the essential parts of the phase demodulator. It allows a phase detection of $\pm 5 \; - \; 90\, degrees$.

Three different ways were simulated to implement the reference signals for the phase detector. All three methods are functional but they are more or less suitable for the underlying low power ADC which is described here.
The *first method* is shown in figure 5.39. The ADC is based on an $N-1$ capacitor array, thereby the capacitor values increase linearly. The current source has the same value for all ADC stages. During the reset pulse the reset switch is closed and the capacitors are discharged. If the switch is opened the current source charges the capacitors. So the buffer stage outputs a '1' until the voltage value at the capacitors falls below the threshold value. The ADC in this form generates pulses with different lengths at nodes $digout_0 \ldots digout_{N-1}$. These values are compared with the negative edges of the phase modulated clock signal at the phase demodulator input. As a result the phase demodulator outputs a binary word which corresponds to the phase deviation of the PM input signal.

The *second circuit* to generate the reference signals for the phase detector ADC is shown in figure 5.40. Type II works with $N-1$ current sources of different current values. In this method the values of the capacitors are the same, but the current sources ($I_{REF0}, I_{REF1}, I_{REF(N-1)}$) increases accordingly with the function $\frac{1}{t}$.
In the case of ADC type II the same procedure is used as for ADC type I. So each capacitor node is discharged with the reset pulse. The resulting reference pulses are compared by the negative edge of the phase modulated input clock.

The *third method* is shown in figure 5.41. In this method several threshold voltages are generated by an operational amplifier, a voltage divider and an adjustable current source (I_{BIAS1}, I_{BIAS2}, I_{BIAS3}) with the help of the reference voltage V_{REF}.

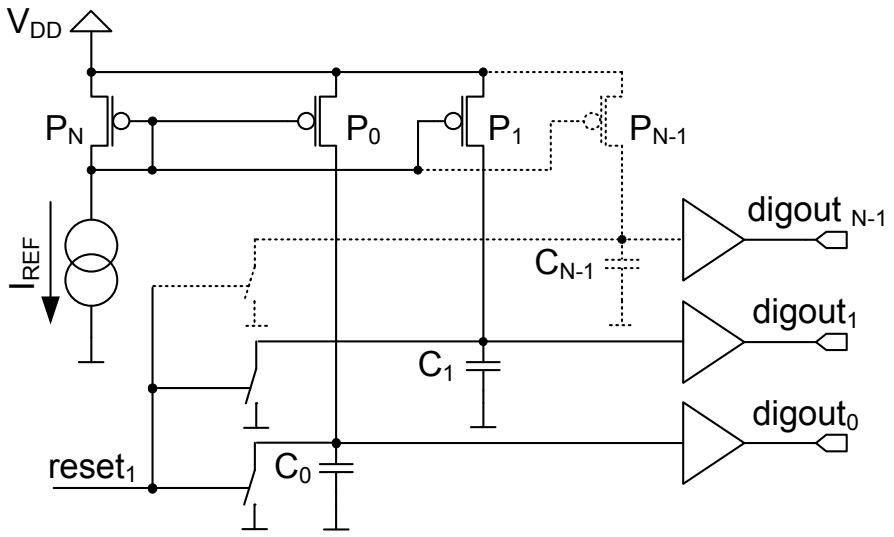


Figure 5.39: Reference signal generation for the ADC. First way to generate the voltage thresholds for the ADC.

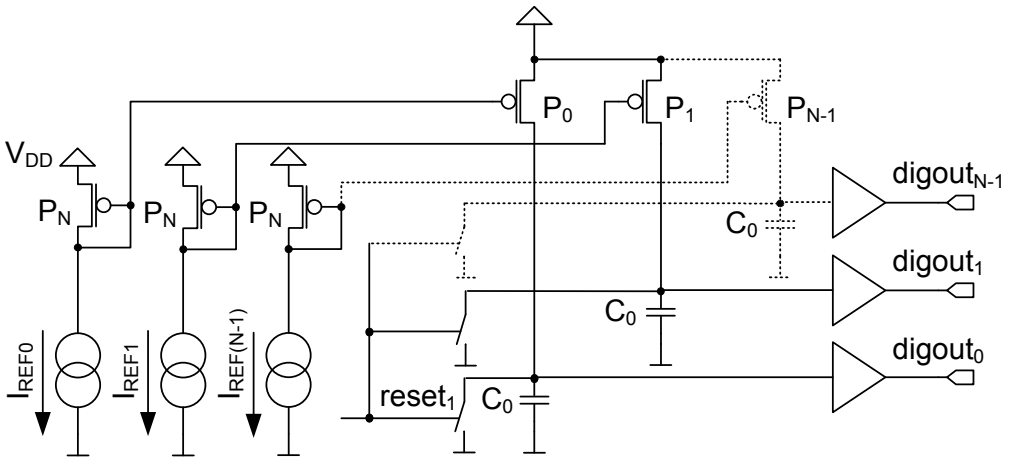


Figure 5.40: Second way to generate the reference signal for the ADC.

The generated threshold voltages are compared with the voltage at node V_{SENSE}. As already mentioned, the voltage at node V_{SENSE} is created by the phase frequency detector and the current charge pump circuit of the phase detector circuit. The principle of this third variant has been implemented in test chip I and test chip II.

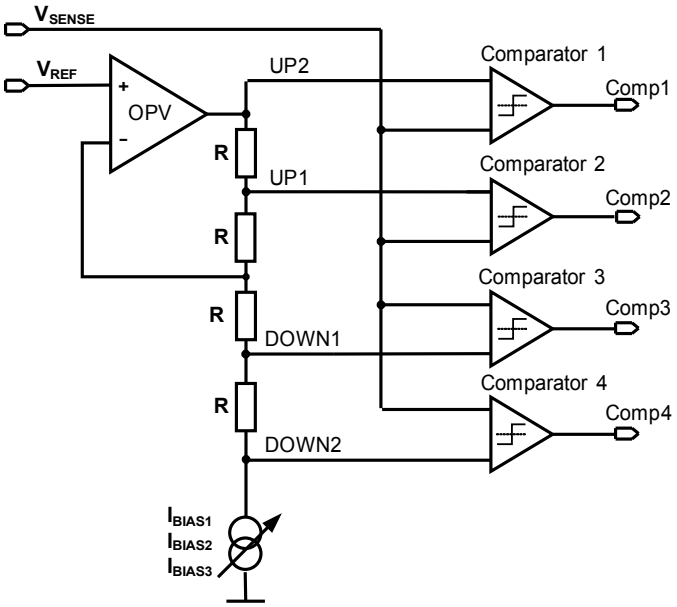


Figure 5.41: Window comparator. Another method to generate the reference signals for the phase detector ADC.

It is important that the ADC complexity is kept small to achieve a low power consumption of the whole phase demodulator. In contrast to the second variant the first variant has the advantage that the phase deviation at the input is proportional to the ADC binary output word. In variant two the values of the current sources have to be increased by a $\frac{1}{x}$ function to get a linear relationship between the phase deviation at the input signal and the output value of the ADC. It is not an easy task to get a $\frac{1}{x}$ distribution of the current sources with a well matching current mirror.
In variant three the power consumption is higher than in both other cases, because the complexity of the voltage reference generation is much higher. The distances between the generated voltage levels must be the same to get a linear dependency between the phase detector input and ADC output.
The first variant in figure 5.39 is implemented in test chip III. Here, an important aspect is that the reset pulse length is high enough to guarantee that the analog voltages at the capacitor nodes are completely discharged. The layout of the capacitor array is also essential with regard to good relative matching behaviour.
For a better control of the parasitic capacitors, a shielding has been introduced into the layout. Therefore, metal wires have been integrated between the capacitors. Additionally, the potential of the metal lines are set to a defined value to avoid floating effects.
For evaluation if the phase difference between the inputs HF_{SIGNAL} and $Oscout$ a phase frequency detector is needed. Additionally, it is important to distinguish between a positive and a negative phase jump. Therefore, a phase frequency detector with sign generation has been introduced. Figure 5.42 shows the phase frequency detector implementation with two edge-triggered,

resetable D flip-flops. Their D input is tied to a logic 1. The inputs of interest, HF_{INPUT} and Osc_{OUT}, serve as the clocks of the flip-flops. If $QA = QB = 0$ and HF_{INPUT} rises, QA rises too. If this is followed by a rise at Osc_{OUT}, QB goes high and the AND gate resets both flip-flops. The difference between the pulses at QA and QB still represents the input phase or frequency difference. Each flip-flop can be built with two edge-triggered cross-coupled RS latches. The PFD has a linear phase detection range of $\pm 2\,\pi$ radians. It is duty cycle insensitive. The delay in the reset path is used to eliminate the dead zone (undetectable phase difference range). In order to generate the sign bit both input signals HF_{INPUT} and Osc_{OUT} are compared by a D-Flip Flop.

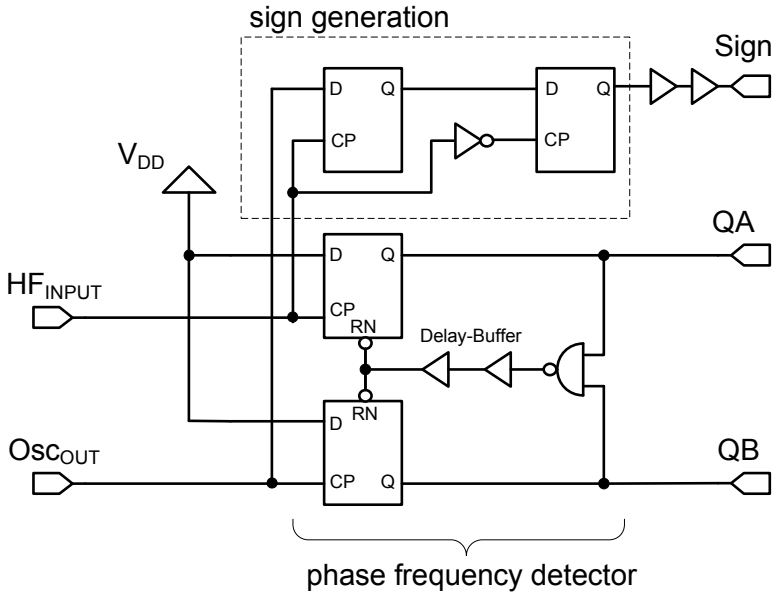


Figure 5.42: Phase frequency detector with sign generation (PFD+SIGN). In order to differentiate between positive and negative phase jumps a sign generation has been introduced.

Some signals are shown in figure 5.43 to demonstrate the functionality of the phase detector ADC. The resolution of the ADC is 5 bit for the positive phase jumps and 5 bit for the negative phase jumps. To adjust the ADC sensitivity a 3 bit $RISEI$ signal has been introduced. So it is possible to change the phase resolution of the phase detector ADC. The simulation results in figure 5.43 show some important signals of the phase detector ADC, the phase deviation of the phase modulated input signal, the sensitivity adjustment (signal $risei$), the positive/negative phase jump decision signal (signal $sign$) and the output of the phase detector ADC (signal ADC_OUT).

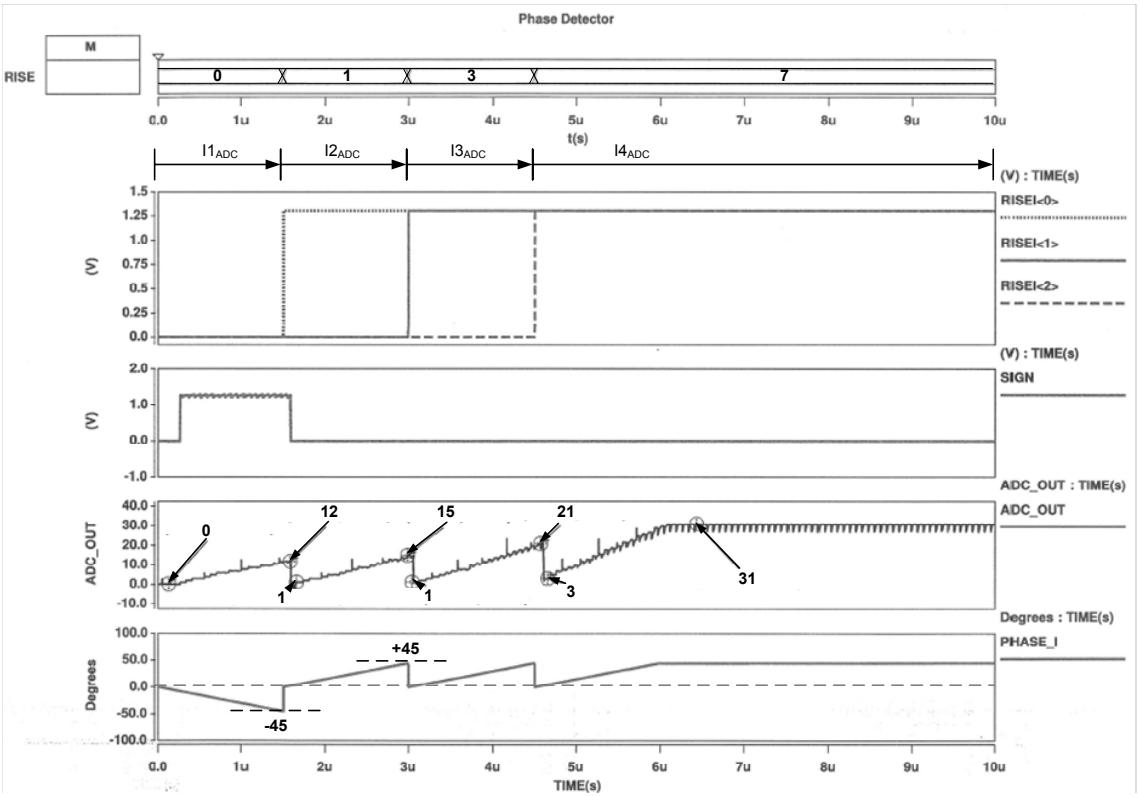


Figure 5.43: Simulation results of the phase detector ADC. The ADC is tested with the phase deviation of a phase modulated input signal (shown in the last picture). ADC_OUT represents the corresponding ADC output value. Additionally the generated sign signal and the phase detector adjustments are shown.

In Figure 5.43 the ADC sensitivity increases in time and the corresponding ADC output values are shown below. The ADC value also increases with increased sensitivity over time. For a higher sensitivity of the ADC the currents through the ADC stages are increased. Thereby current $I4_{ADC} > I3_{ADC} > I2_{ADC} > I1_{ADC}$.
If a negative phase jump occurs at the input the signal $sign$ is 1, otherwise the signal is 0 at positive phase jumps. The example described shows the phase deviation of the phase modulated input signal with a ramp characteristic. The ADC output is proportional to the phase deviation of the phase modulated input signal. As already mentioned, the ADC has a resolution of about 5 bits for positive and negative phase changes. A specified area of the constellation diagram will be divided into equidistant parts.

In order to show the possibility for sensitivity adjustment of the phase detector unit the constellation diagrams are shown in figures 5.44 and 5.45. The phase range of figure 5.44 is about 45 degrees and 90 degrees at the second constellation diagram. Due to the ADC resolution the phase differences are 1.41 degrees and 2.81 degrees, respectively.

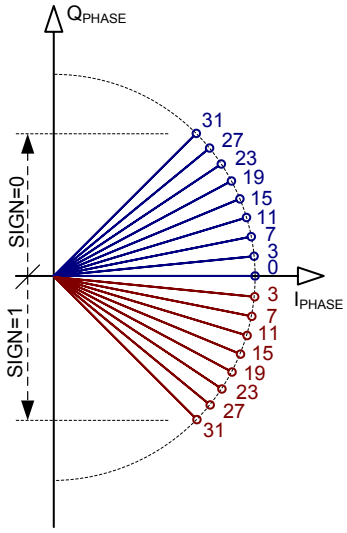


Figure 5.44: Constellation Diagram (Phase Range = ± 45 degrees) for fine resolution of the ADC.

The maximum detectable phase change can be adjusted by a current through the analog digital converter from the phase detector. Due to the adjustable current value it is possible to detect large phase jumps as well as small phase changes.

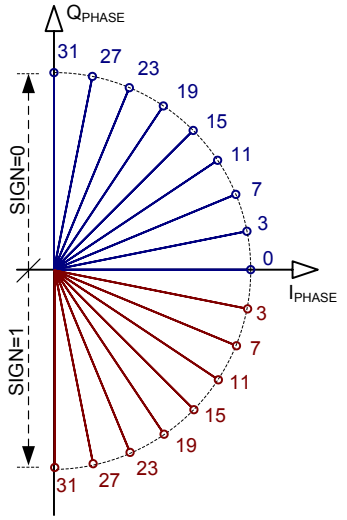


Figure 5.45: Constellation Diagram (Phase Range = ± 90 degrees) for coarse resolution of the ADC.

5.4.1 Phase Detector ADC

In the previous chapter the functionality of three different ADC types have been discussed. Two of these types are integrated in the test chips. Here, the multi-level phase detector with the first ADC type is considered in detail. Figure 5.46 shows the circuit of the phase detector ADC for the multi-level phase detection mechanism. The circuit includes a current source, $N-1$ ADC stages with an $N-1$ capacitor array, D-FFs, a synchronization block and a thermometer to binary decoder.

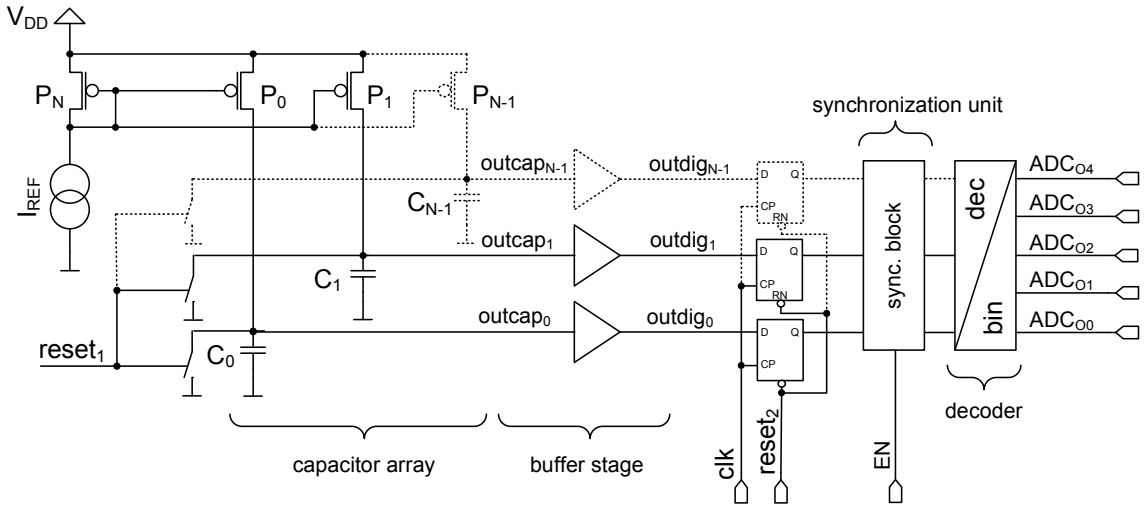


Figure 5.46: Phase detector ADC. The phase detector ADC can be represented by dividing the circuit into the important blocks, such as the capacitor array, the buffer stage, the synchronization unit and the decoder stage.

Thereby the capacitor value grows linearly with the index of the ADC stages. All PMOS transistors have the same size (have the same $\frac{w}{l}$ relationship). In order to digitize the analog signals at node $outcap_{0\ldots N-1}$ buffers have been implemented. To compare the phase modulated input signals with signals $outdig_{0\ldots N-1}$ D-FFs have been chosen. The synchronization block synchronizes the output signals from the D-FFs at the negative edges of signal HF_{SIGNAL}. With the aid of the thermometer decoder the 32 synchronized digital signals are encoded to a 5 bit binary word. The decoder has been designed with several multiplexers to avoid glitches. The functionality of the ADC is based on the flash A/D converter principle. Each converter stage includes a current reference, a capacitor, a reset-switch, a buffer and a D-FlipFlop.

Furthermore, the thermometer to binary decoder is shown in figure 5.47 in detail. Here, the circuit is composed by several multiplexers and buffers. An advantage of the multiplexer-based decoder is its more regular structure than compared with other structures. It is also possible to balance the delay between the paths by introduction of buffers in the decoder.

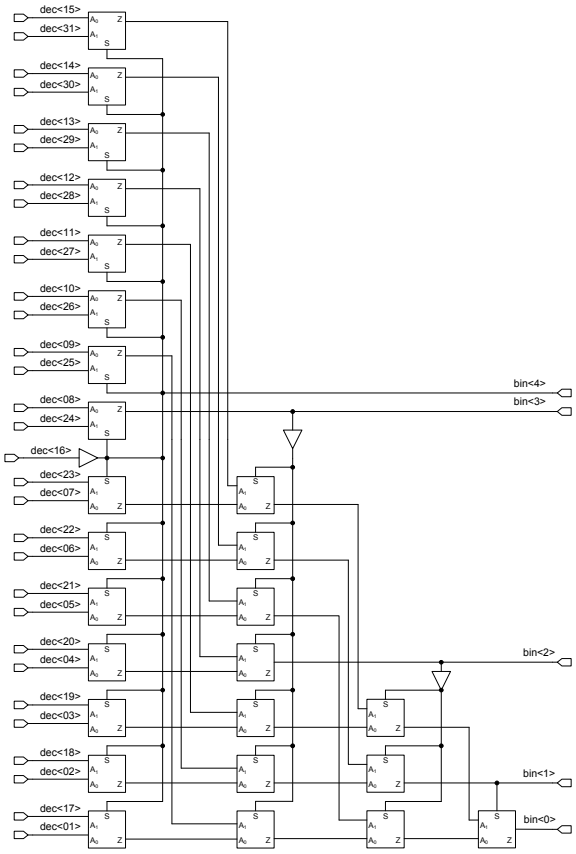


Figure 5.47: Thermometer to binary decoder. The input signals $dec\langle 01\rangle \cdots dec\langle 31\rangle$ from the voltage threshold decisions are encoded by the thermometer to binary decoder to a 5-bit word.

The simulation result is shown in figure 5.48.

Several signals such as the PLL output signal Osc_{OUT}, the phase modulated input signal HF_{INPUT}, the output signal of the phase frequency detector, the two reset signals $reset_1$ and $reset_2$, the analog signal outcap and the digitalized signal $outdig$ are shown in the simulation result. Both input signals, Osc_{OUT} and HF_{INPUT}, are compared by the PFD from the phase detector. The reset signals set the analog signals outcap to zero and reset the D-FFs. Furthermore, the digitalized output signal $outdig$ is compared with the PFD output signal PFD_{OUT}. With the help of this concept the phase detector can divide the constellation diagram into 32 phase zones.

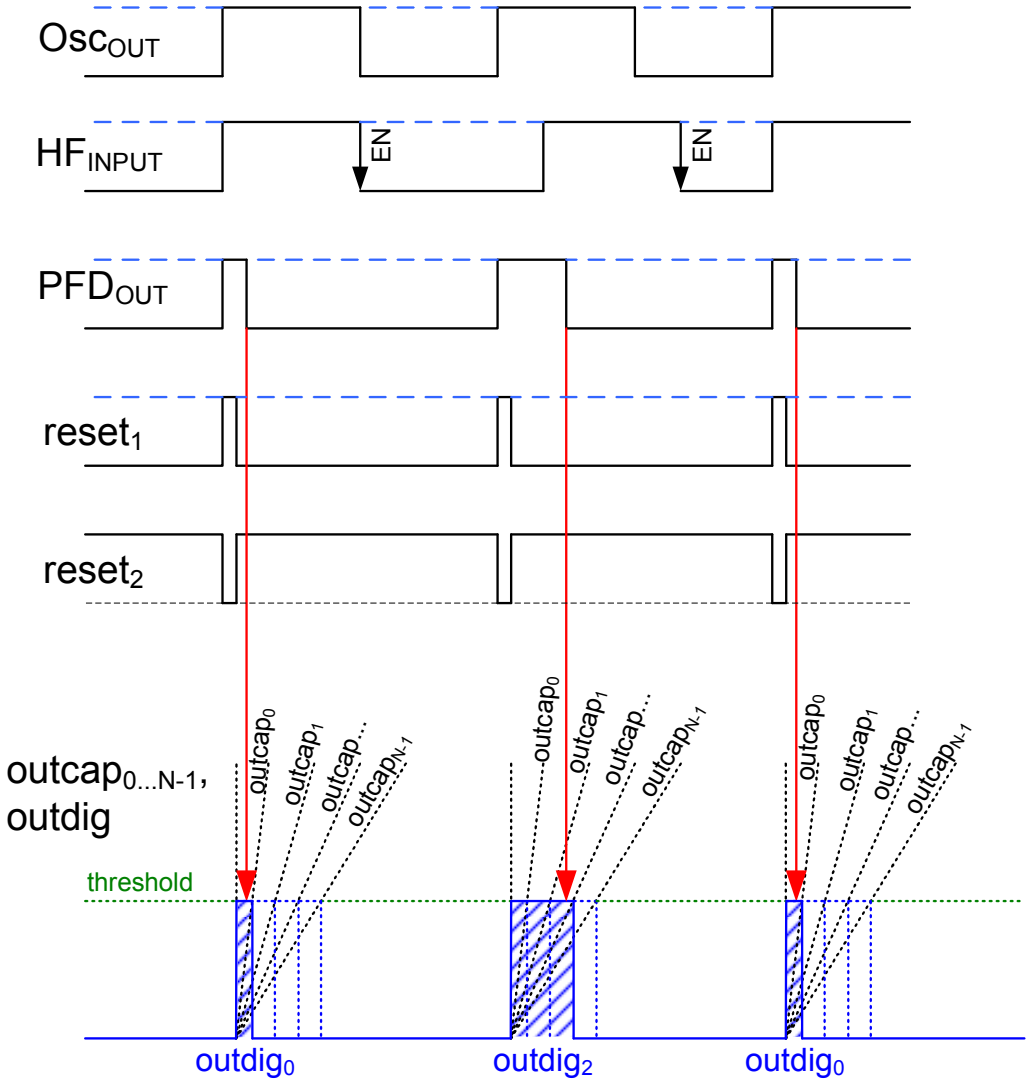


Figure 5.48: Simulation signals - Phase detector ADC. Several signals are necessary to provide the functionality of the phase detector. Two typical input signals Osc_{OUT} and HF_{INPUT} are shown above. The phase frequency detector output PFD_{OUT} and both reset signals of the ADC $reset_1$ and $reset_2$ are also shown. At the bottom of the figure the integrated voltage curves at the capacitors $C_0 \cdots C_{N-1}$ are indicated. With the integrated voltage curves and the buffer stages pulse references are generated for the phase detection mechanism.

To generate positive edge-triggered reset pulses the circuit in figure 5.49 has been used. In the underlying circuit the reset length can be changed by the number of delay buffers. It is important that the reset pulse has to be long enough to fully discharge the capacitor array. In this design 4 delay buffers have been chosen leading to a reset pulse width of typical $2\,ns$.

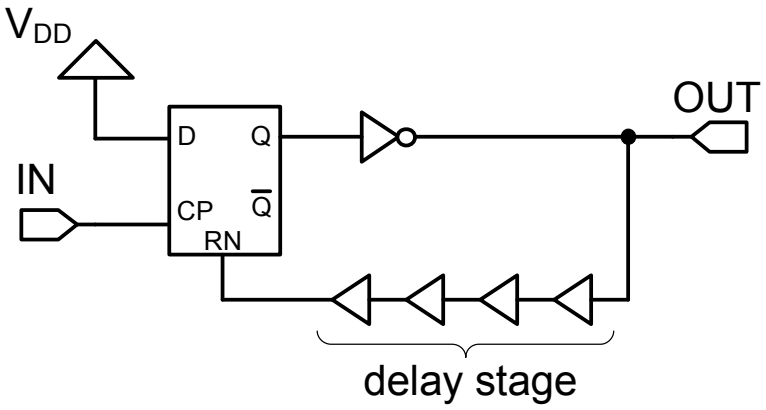


Figure 5.49: Reset pulse generation. In order to generate a reset pulse for the phase detector a loop with D-FF and a delay stage have been used.

5.4.2 Simulation Results of the Digital Part for Multi-Level Phase Demodulation

To complete the proposed multi-level phase demodulator a digital part is needed. One of the main tasks of the digital part is to generate signals to control the analog components of the phase demodulator circuitry. The important signals of the digital unit are shown in figure 5.50. The first signals show the ADC output BIN, the overflow bit $OVERFLOW$ and the sign signal $SIGNUM_O$.

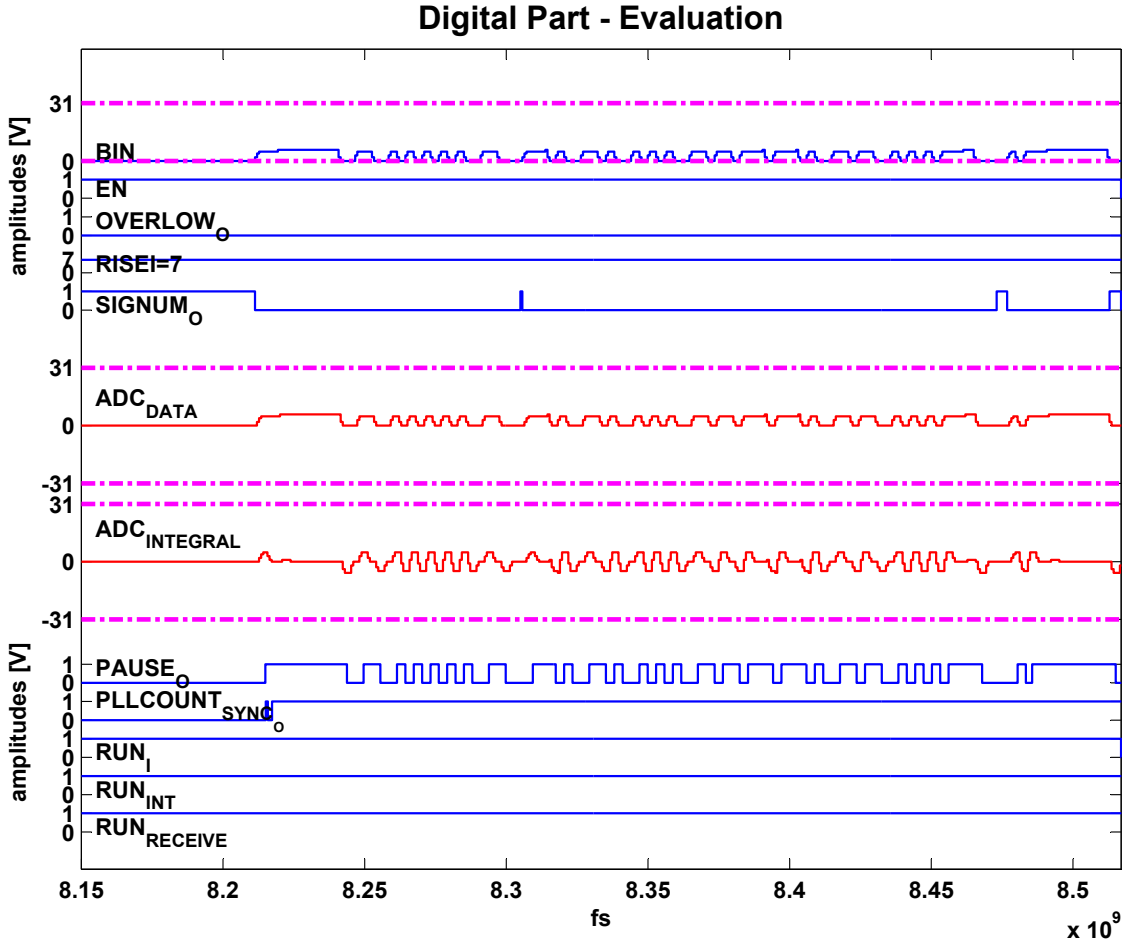


Figure 5.50: Simulation results - digital part (1/2).
In this case a phase modulated signal with 2 phase states has been transmitted. The transponder FPGA receives the ADC output values (ADC_{DATA}) and $(SIGNUM_O)$ and transmits the control signals $(PLLCOUNT_{SYNC_O}, EN)$ and $(RISEI)$ for the demodulator and load modulation circuit $(PAUSE_O)$.

Furthermore, the control signals from the digital part, such as the enable signal EN, the current control signal for the ADC $RISEI$, the digitalized ADC output ADC_{DATA}, the integrated ADC output $ADC_{INTEGRAL}$, the extracted bit stream $PAUSE$ and the synchronization signal of the PLL $PLLCOUNT_{SYNC_O}$ are also shown.
With the help of the control signal $RISEI$ and the synchronization signal $PLLCOUNT_{SYNC_O}$ the binary output word of the ADC ADC_{DATA} is created. Both signals, ADC_{DATA} and $SIGNUM_O$, are combined to get the digitalized phase deviation. The pause signal represents

the bit information, which is extracted from the ADC output value.
In the current example the data of a phase modulated signal with two phase states is extracted, whereby the data is transferred by a transmission rate of one period/bit. This is equivalent to a transfer rate of 13.56 Mbit/s.

To further increase the transmission rate up to 27.12 Mbit/s a phase modulated signal with more than two phase states has been used. Figure 5.51 also shows the digital signals from the digital block for the analog components.

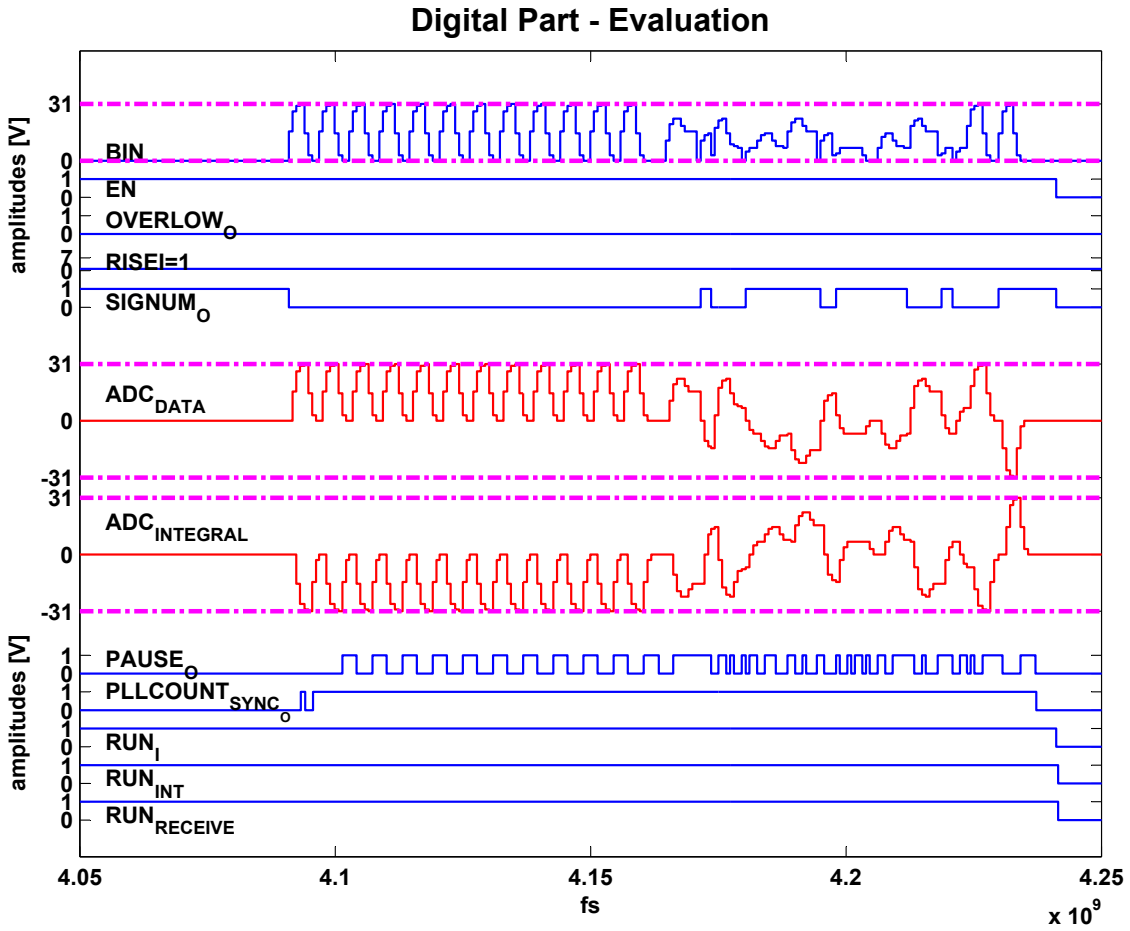


Figure 5.51: Simulation results - digital part (2/2). In this case, a phase modulated signal with 16 phase states has been transmitted. The ADC output ADC_{DATA} is encoded into the bit stream $PAUSE_O$.

The simulation shows the functionality and the I/O signals of the digital part without the influence of the analog circuits. This means that the incoming signals of the digital part are simulated without any phase and frequency jitter influence. Due the noise and jitter influence of the phase demodulator and the analog components the distinction between one phase state and another phase state is more difficult than in the simulated ideal case. The simulation in figure 5.51 is based on a phase modulated signal with 16 phase states at a bit time of $73.75\,ns$, which is not practicable in a real environment. For this reason, in the proposed phase demodulator concept a phase modulated signal with 4 phase states has been chosen.

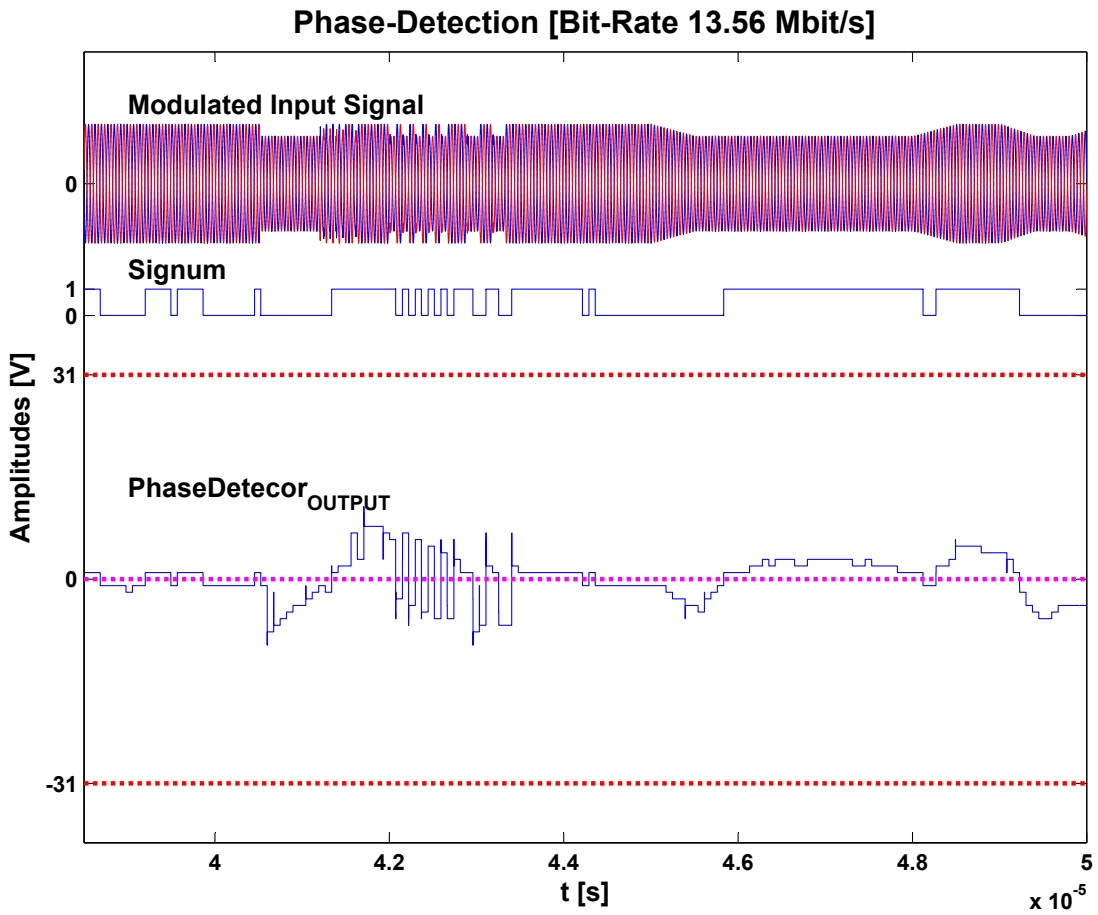


Figure 5.52: Simulated analog signals of the phase detector. This figure shows an phase-modulated signal, the corresponding sign output signal and the ADC output of the phase detector without any synchronization of the PLL. The maximum value of the ADC lies at ± 31, which is marked with a dashed red line.

For a separation of the phase states a run-in pattern (learn pattern) is necessary. At first a reference carrier has to be transmitted. The reference carrier is used to calibrate the digital part. With the help of the learn-in pattern the phase states are defined for the digital post processing.

The analog signals of the phase detector, such as the modulated input signal, the phase detector output $PhaseDetector_{OUTPUT}$ and the sign signal $Signum$ are shown in figure 5.52. To visualize the phase modulated signal in a better way the PM signal has been converted into a corresponding amplitude modulated signal.

To decode the bit stream from the ADC output values a digital post-processing is necessary. For digital post-processing of the ADC output signal two methods have been tested and integrated in the digital part. In the first method the ADC output is compared by fixed threshold values. This method has the advantage of a low complexity. In the second method the ADC output is differentiated and the results are also compared by fixed threshold values. Maximum threshold value of ± 31 is drawn as a red dashed line. The advantage of the second method is that the PLL stability does not affect the evaluation process.

5.5 Layout of Test Chip I, Test Chip II and Test Chip III

As already mentioned, in the course of the thesis three tape-outs were processed.

- Test chip I was integrated in a 120 nm process,
- Test chip II was integrated in a 90 nm process and
- Test chip III was integrated in a 90 nm process

5.5.1 Layout - Test chip I

Figure 5.53 shows the layout of the complete phase demodulator system. The implementation includes the PAD frame, the blocking capacitors between V_{DD} and V_{SS} and the phase-locked loop with phase detector for data rates up to 1.695 Mbit/s. The demodulator requires an silicon area of about $0.07\,mm^2$ (120 nm Flash CMOS process).

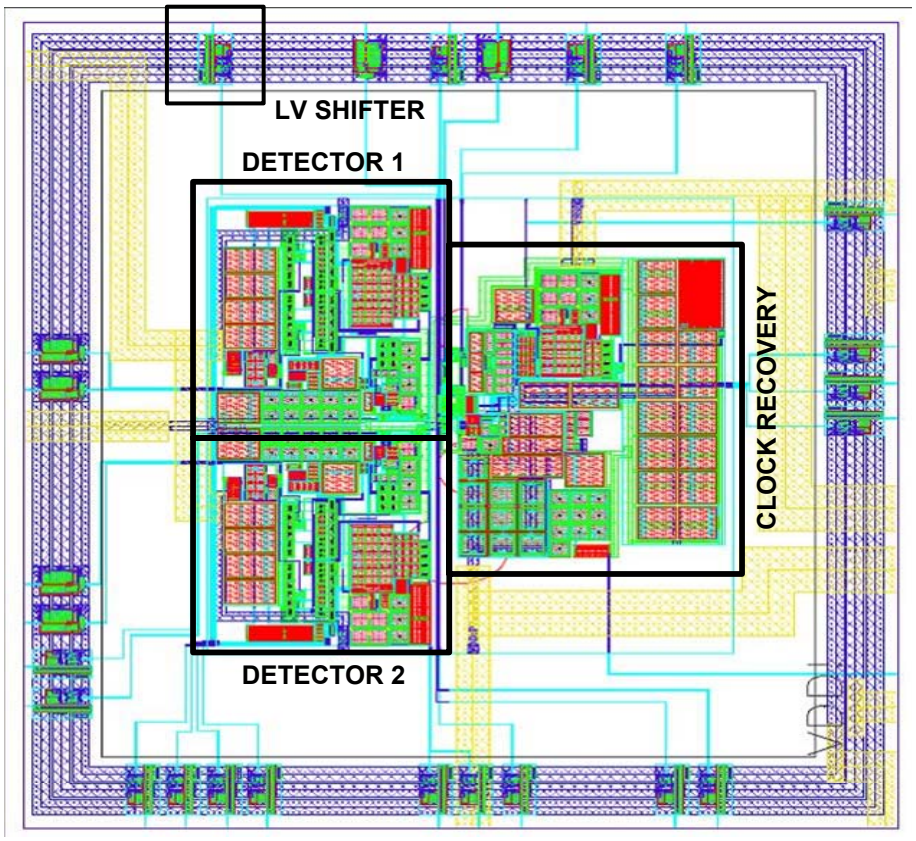


Figure 5.53: Layout phase demodulator I. The first test chip was fabricated in a 120 nm Flash CMOS process. It includes the demodulator circuit with the two-state phase detector circuit.

5.5.2 Layout - Test chip II

The layout in figure 5.54 shows a test structure of the complete transponder analog front end with an advanced phase demodulator for data rates up to 13.56 Mbit/s. The outer frame consists of

test pads with ESD structures for chip verification. Within the frame there are blocking capacitors, a rectifier, a voltage regulator and a bias cell on left side, a phase-locked loop and a phase detector on the right hand side and underneath there is the shunt system.
Furthermore, the demodulator was put as far away as possible from the shunt transistor (heat source). The transponder chip was fabricated in a 90 nm Flash CMOS process working with a supply voltage of $1.4\,V$. The average power consumption of the phase demodulator is 0.56 mW. The demodulator circuit begins to operate when the field strength exceeds a value of about $0.4\,A/m \triangleq 20 \cdot \log(400000\,\mu A/m = 112\,dB\mu A/m)$. In order to this, the minimum field strength at different bit rates is limited by the analog front end rather than the phase demodulator circuitry.

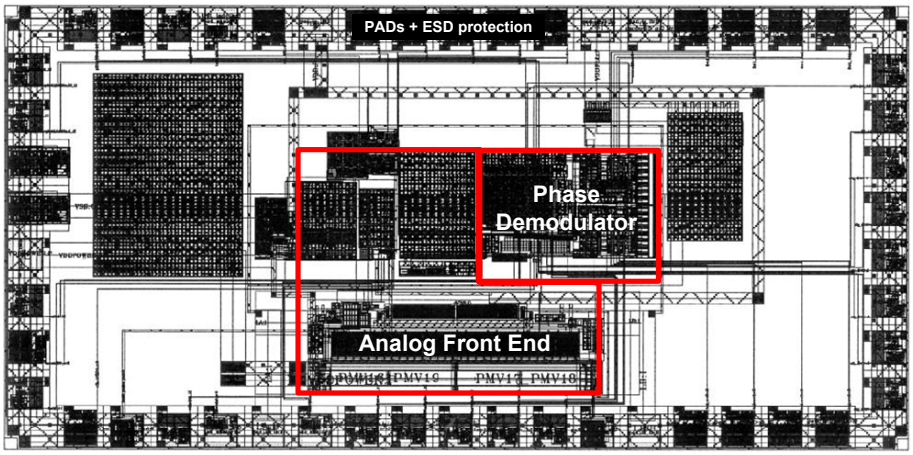


Figure 5.54: Layout phase demodulator II. The aim is a "stand-alone" transponder system for high bit rates. Therefore an analog front end was designed to allow a verification of the phase demodulator with an AFE. Several changes have been made in contrast to typical AFEs. For this design a 90 nm Flash CMOS process has been used.

5.5.3 Layout - Test chip III

The layout of the next generation of the analog front end and the phase demodulator is shown in figure 5.55. It shows the 5-bit phase detector ADC and the phase-locked loop of the improved phase-demodulator concept. Both circuits are controlled by the digital part.

The area consumption is about $0.029\,mm^2$ of the phase detector cell and $0.034\,mm^2$ of the phase-locked loop. Table 5.2 shows a summary of area consumption of the three test chips. The first one has been implemented on a 120 nm CMOS process and the second and third one are based on a 90 nm Flash CMOS process.

Several measurements have shown that the leakage current in the 90 nm process is much higher than in the 120 nm process. Due to the higher leakage current, the phase drift in hold mode is much higher than in a 120 nm process. As a result the hold time of the phase-locked loop has to be significantly lower to achieve the same phase detection performance.
In the first two test chips there is no digital part included. Therefore the digital signals were emulated by an FPGA board.
The first test chip contained a phase demodulator circuit for bit rates up to 1.695 Mbit/s without an analog front end component.
The second test chip was processed with a complete analog front with an increased detection

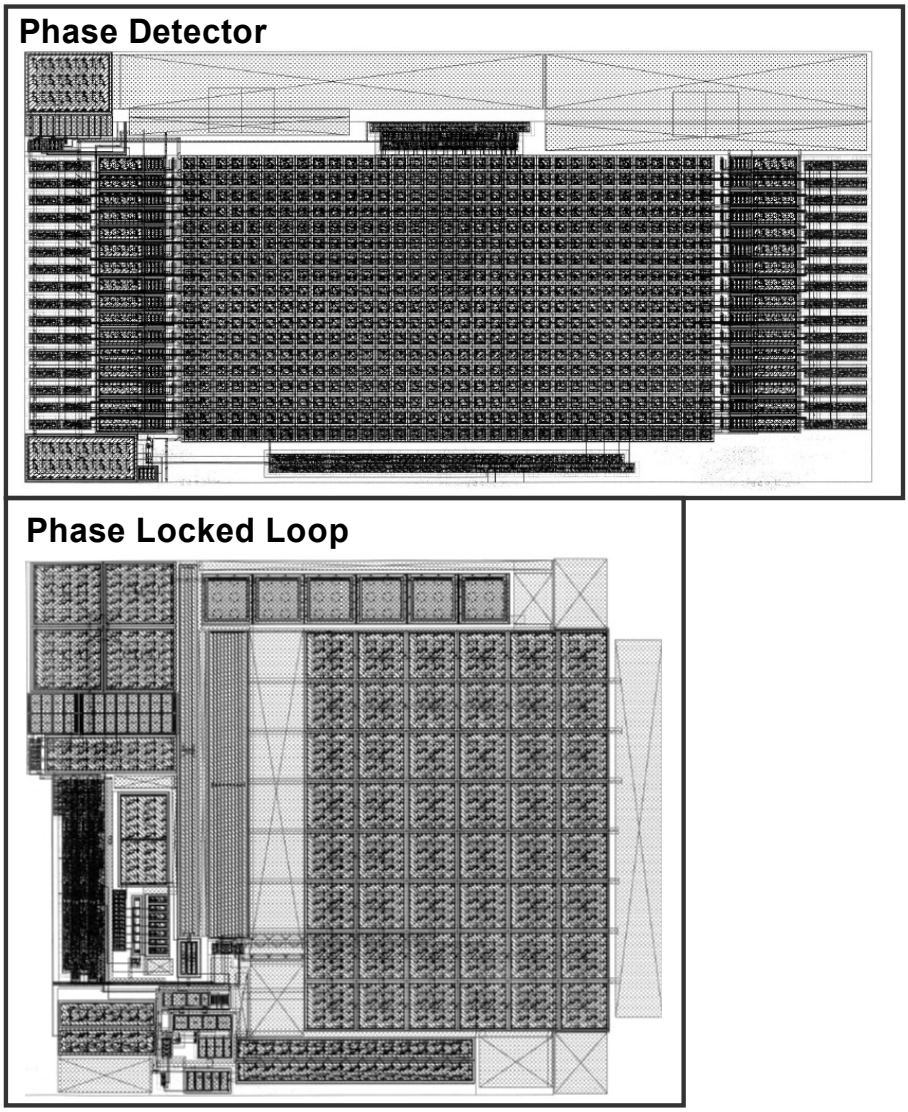


Figure 5.55: Layout of the phase demodulator III. One particular component is still missing in test chip II, the digital part of the standalone transponder system. For this reason a digital part with an improved phase detector has been integrated into a third test chip.

Table 5.2: Area consumption - different test chips. For a good overview the area consumption of the different test chips are set in relation. The third test chip needs much less area than the other test chips, but requires more power.

Test Chip	Area Consumption Phase Detector	Area Consumption PLL	Area Consumption Phase Demodulator	Power Consumption Σ
I	$0.040mm^2$	$0.030mm^2$	$0.070mm^2$	$0.30\,mW$**@1.5 V**
II	$0.050mm^2$	$0.048mm^2$	$0.098mm^2$	$0.56\,mW$**@1.5 V**
III	$0.029mm^2$	$0.034mm^2$	$0.063mm^2$	$0.61\,mW$**@1.35 V**

rate up to 13.56 Mbit/s.
The third test chip includes an integrated digital part. Due to this the test-chip can be seen as a ”stand-alone” system. This test chip consists of a phase demodulator with a 5-bit ADC, a 5-bit amplitude demodulator and an analog front end with a digital part for high bit rates up 13.56 Mbit/s.
Table 5.3 illustrates the minimum field strength for stable RxD and TxD communication between reader and transponder (test chip III). It can be seen that the demodulator circuit begins to operate when the field strength exceeds a value of $0.8\,A/m \triangleq 20 \cdot \log(800000\,\mu A/m = 118\,dB\mu A/m)$. The operating distance and minimum field strength at different bit rates are limited by the analog front end functionality. Table 5.3 shows similar minimum field strengths, because the power consumption of the phase demodulator is constant over different bit rates.

Table 5.3: Minimum field strength of test chip III (measurement).

Minimum Field Strength	
Bit Rate [kbit/s]	**Hmin [A/m]**
106	**0.818**
212	**0.818**
424	**0.818**
848	**0.830**
1700	**0.818**
3400	**0.830**
6800	**0.841**
13560	**0.852**

5.6 Verification

5.6.1 Test Chip I

Figure 5.56 illustrates a detected data stream. At first, the transmitted phase modulated signal from the reader is shown .

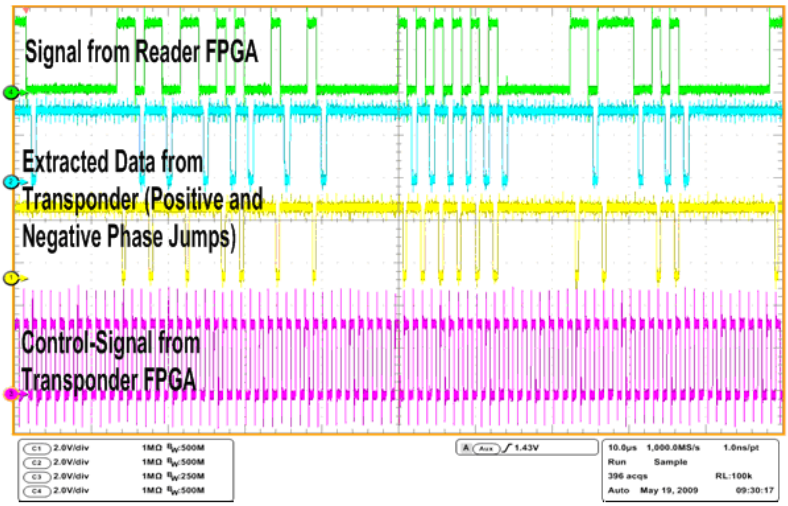


Figure 5.56: Measurement results of test chip I. Bit rates of 848 kbit/s have been tested.

The next two signals corresponds to the positive and negative phase jumps, which are extracted by the integrated phase demodulator. At least, the control signal of the transponder FPGA is shown, which toggles between the hold mode state on and off. During the hold mode the voltage deviation which equals the phase deviation is accumulated (figure 5.57).

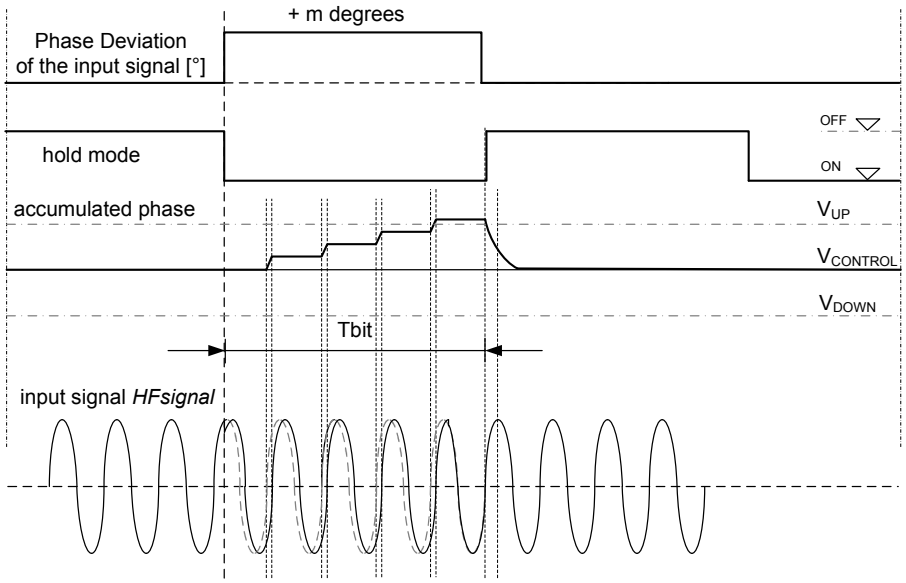


Figure 5.57: Phase demodulator principle - test chip I

If the accumulated voltage $V_{CONTROL}$ exceeds the upper threshold voltage V_{UP} or the lower threshold voltage V_{DOWN} the phase demodulator detects a positive respectively a negative phase jump. The phase demodulator is able to summarize the voltage deviations of four periods. In order to this, a data extraction is possible with a bit rate up to 1696 kbit/s. In contrast to test chip II and test chip III, test chip I is supplied by an external voltage source.
By minimization of the accumulation periods the detection of higher bit rates are possible. But the disadvantages are that the current consumption is not constant over time and the complexity of the phase detector is high. As a consequence of the results achieved from test chip I, additional steps have been taken to improve the phase demodulator performance for test chip II and test chip III, as discussed in chapter 5.3.

5.6.2 Test Chip II

Figure 5.58 shows the phase deviation of the modulated signal and the output voltage of the phase detector ADC.

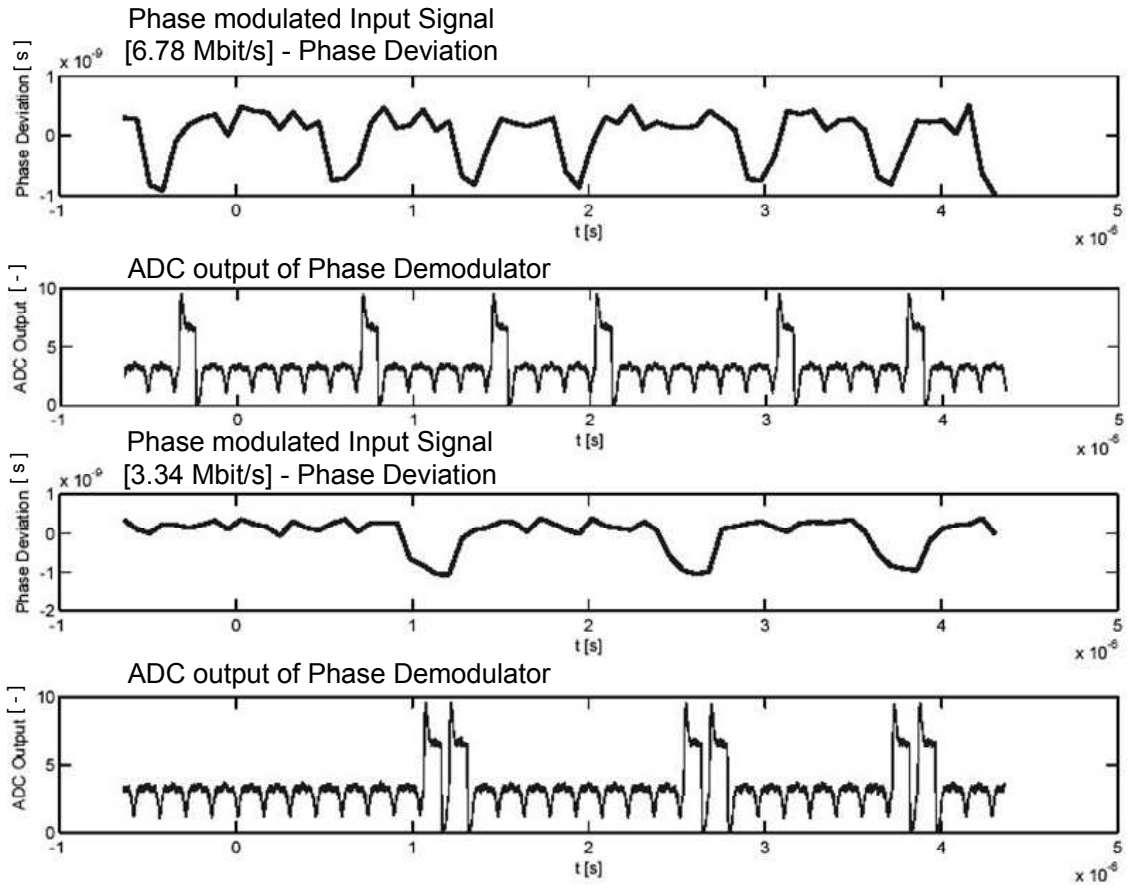


Figure 5.58: Measurement results of test chip II. Bit rates of 3.34 Mbit/s and 6.78 Mbit/s have been tested. The data stream based on an NRZ coded phase modulated signal.

As expected, the phase detector ADC output voltage increases if a phase change occurs. In the measurement the modulated data were transmitted with a data rate of 3.34 Mbit/s and 6.78 Mbit/s at a carrier frequency of 13.56 MHz. The ADC output is proportional to the phase deviation of the input. In the proposed system two 2-bit ADCs are used - one to recognize positive, the second one to recognize negative phase changes. The resolution of the ADC determines the amount of possible phase states which can be recognized. The upper graph shows a phase modulated carrier signal (13.56 MHz) with phase changes of -5 degrees (displayed in nanoseconds) at a bit rate of 6.78 Mbit/s. The second graph shows the output of one of the two phase detectors (ADC output). If a phase shift occurs, the output voltage (sum of all 4 comparator output voltages) increases - reaching a value corresponding to the value of the phase change. In this case, a phase change of 5 degrees corresponds to an ADC-code of 6. The two graphs below show the same signals as the ones above by using half of the bit rate of the upper signals - 3.34 Mbit/s.

Figure 5.59 shows measurement results of the phase detector for bit rates of 13.56 Mbit/s (testchip II).

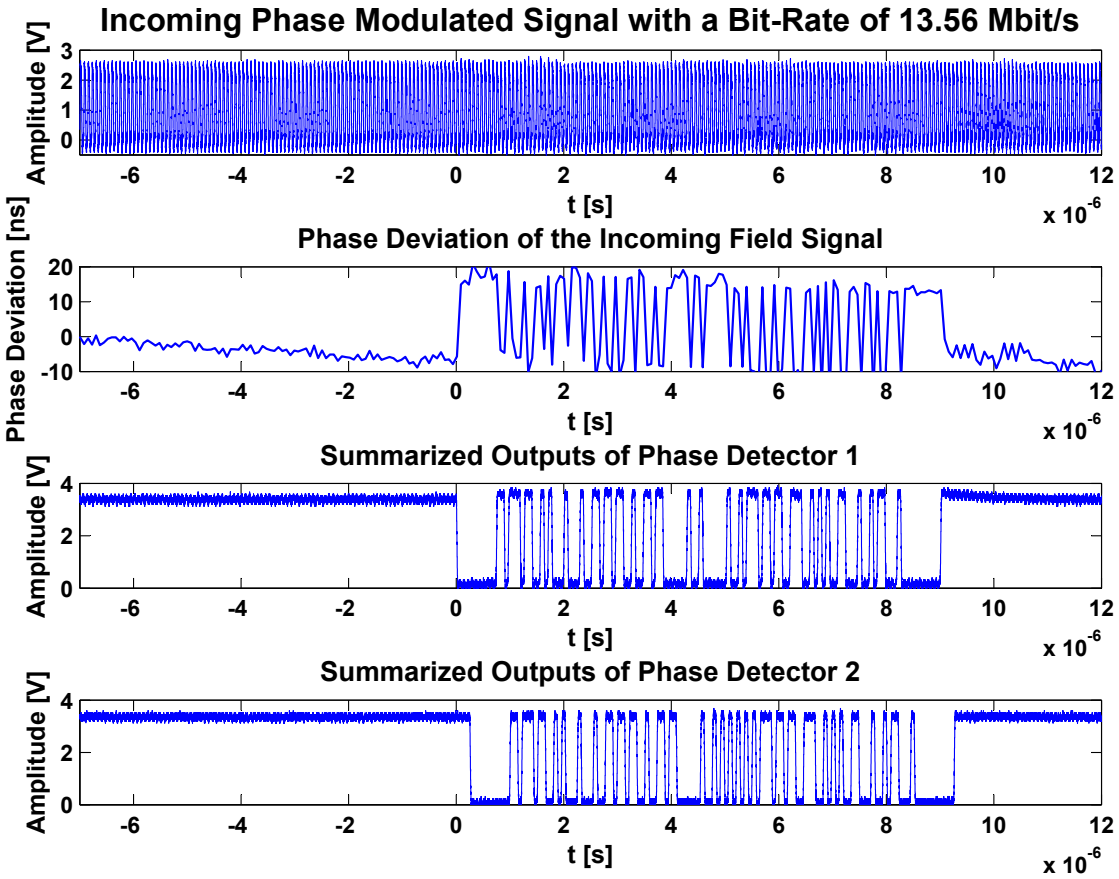


Figure 5.59: Measurement results: Extraction of the baseband with a bit rate of 13.56 Mbit/s.

The phase-modulated input, the phase deviation of the incoming signal, and the output signals of both phase detectors are displayed. In this case the incoming input signal is phase modulated with 10 degrees. The phase detector provides two bits for positive phase jumps and two bits for negative phase changes. The distance between the generated voltages, also called window voltages, can be adjusted by a bias current to test different ADC phase resolutions.
The digital parts of test chip I and test chip II are based on a frequency of 27.12 Mhz (2 samples/period).

5.6.3 Test Chip III

In the third tape-out a modified phase demodulator has been integrated into the analog front end. The measurement results of this phase demodulator are shown in figure 5.60.

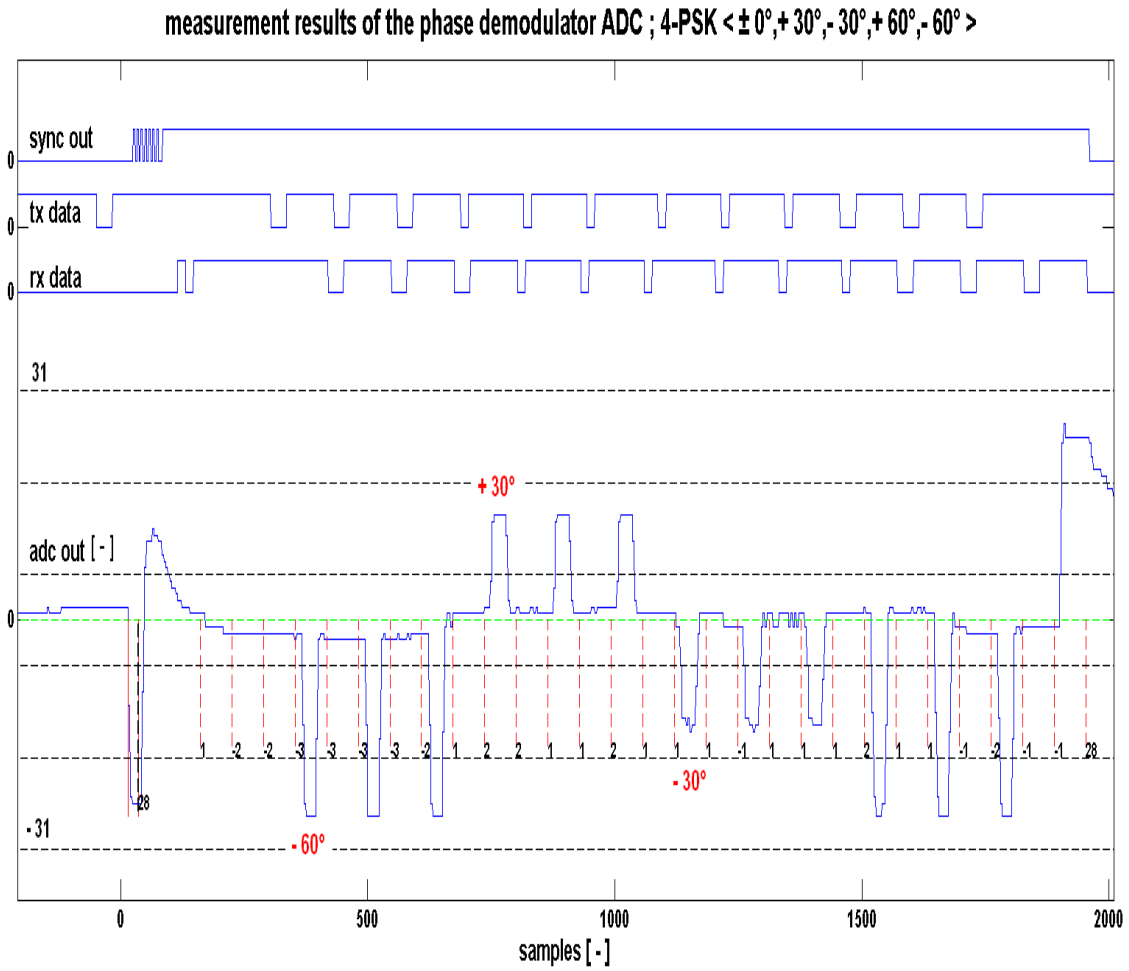


Figure 5.60: Output signal of the phase detector ADC of test chip III and the digital post-processed signal (measurement). This figure shows the transmitted signal $tx\ data$, the extracted pause signal of the transponder phase demodulator $rx\ data$, the synchronization signal $sync\,out$ and the ADC output signal $adc\,out$.

In this measurement a phase modulated signal with four phase states has been transmitted. The four phase jump values are $+30°$, $-30°$, $+60°$ and $-60°$.

Therefore the PLL parameters and the digital part are optimized for bit rates of 13.56 Mbit/s. The PLL counter value is set to 20, the threshold value to seven and the differential length to 1. It can be noticed that it is possible to differentiate between 4 phase states. Here, the digital part of test chip III operates with a sample frequency of 27.12 MHz (4 samples/period).

In order to assess the PLL accuracy a phase-deviation histogram has been measured. Figure 5.61 shows the phase-deviation characteristic at a counter value of $1, 16$ and 31. Additionally, the moving average of these characteristics are shown.

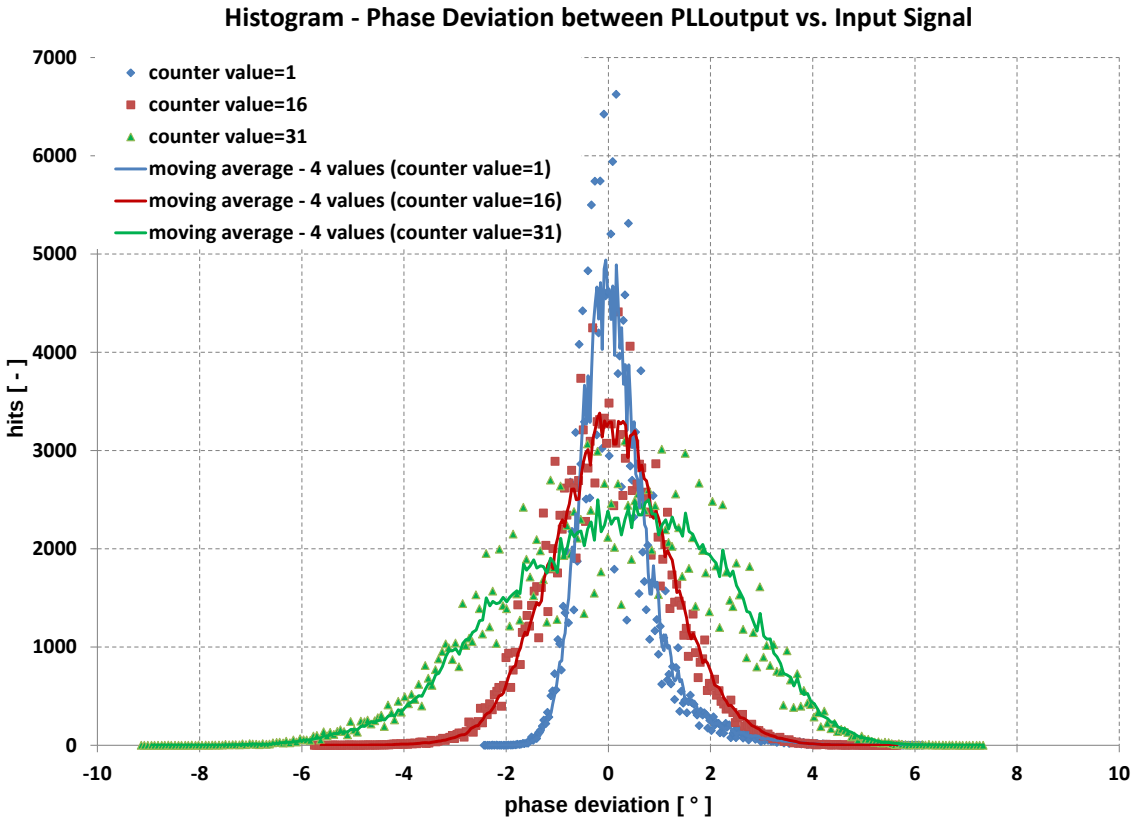


Figure 5.61: Histogram - phase deviation of the PLL (test chip III) at different counter values.

The standard deviation of the illustrated characteristics:

Table 5.4: Sample standard deviation (RMS - 1σ).

counter value	s
1	$2.5°$
16	$3.3°$
31	$4.8°$

Table 5.4 shows the dependency between the RMS - 1σ value and the counter value N. These results represent the minimum phase deviation, which can be detected by the phase demodulator circuit. It can be read out that the phase deviation increase with the counter value.

The underlying estimator for σ is an adjusted version, the sample standard deviation, denoted by s and defined in equation 5.24, where $x_1 ... x_n$ are the observed values of the sample items and $\overline{x}$ is the mean value.

$$s = \sqrt{\frac{1}{n-1} \Sigma_{i=1}^{n} \left(x_i - \overline{x}\right)^2} \tag{5.24}$$

5.7 Summary

Chapter 5 *Analog Demodulators* comprises different types of demodulators with the main focus on the amplitude demodulator and phase demodulator.
In addition, the key component of the phase demodulator the “2-state phase detector” is explained in detail. To guarantee the stability of the phase demodulator two stability models have been introduced. Another important point is the noise behavior of the demodulator circuit. The noise behavior of the PLL indirectly defines the maximum phase resolution of the demodulator circuit. In order to show the settling behavior of the PLL to a phase jump simulation and measurement results are shown.
Furthermore, the possibilities of an implementation of multi-level phase detection are discussed. Several ADC structures are compared to get a profound estimation of the complexity. Finally, the test chip layouts of the three tape-outs which were processed in the course of the thesis are shown. The simulation results of the analog front end and the demodulator circuits are well confirmed by measurements.

6 Research Summary

In the dissertation on hand the transmission of high data rates for passive RFID transponder applications has been investigated.
One of the essential research achievements are transmitted data rates from 106 kbit/s to 13.56 Mbit/s in both directions, from reader to transponder and from transponder to reader. Today, the maximum available data rate is 848 kbit/s, which is not enough for future applications. One example of these new applications would be an electronic passport, which would hold a larger amount of information to be transferred. These new applications would require a higher data transmission rate. To achieve higher data rates a feasibility study was done and as a result of this study new concepts and techniques were designed.
The bidirectional data transfer is made over an air interface. At the same time, the electromagnetic field induces a voltage into the transponder antenna and supplies the analog and digital components of the passive transponder device with energy. To describe the air interface a spice model was introduced to cover mutual coupling effects in both directions and to make it possible to simulate the data transmission in a realistic way.
A number of important points have been considered, such as the limitations due to spectrum regulation, the modulation/coding principle and the quality factor or bandwidth of the resonance circuits. The characteristic of the near-field and far-field zones and the means of energy coupling in each of these regions have also been explained.
In order to lower the magnetic moment to the reader the AC-shunt has been introduced to limit the input voltage to a desired low voltage value. This approach results in a less distorted transmission signal.
In the current work a phase jitter modulation technique has been used to fulfill the spectrum regulation for the data transmission from reader to transponder. Phase jitter modulation uses only a small part of the complex plane for the phase states. In contrast to the amplitude modulation method, the phase modulation is not affected by dynamic problems. With the phase modulation method bit rates up to 13.56 Mbit/s (2 phase states) and 27.12 Mbit/s (4 phase states) have been transmitted. The introduced phase demodulator is able to extract a data stream with a bit rate up to 13.56 Mbit/s. There are also 27.12 Mbit/s detectable, but only under laboratory conditions. Both the phase demodulator and the digital part use the output clock signal of a clock recovery unit with a low input threshold voltage which is described in the appendix. The phase demodulator and the clock recovery circuit operate up to a very low supply voltage of 0.9 V. Due to this low operation voltage, the circuits also work at a high ripple voltage of 10 % of the nominal system operating voltage.
In the course of the project three test chips were designed and fabricated. Three new architectures and designs were developed in order to achieve high data rates for RFID applications. The integrated test chips have been implemented in 120 nm and 90 nm Flash CMOS process. Measurements of 90 nm test chip confirm previous simulation and design results for data rates of 13.56 Mbit/s. The findings of this study, will have important implications for future applications.
Within the framework of the thesis a novel phase detector circuit (“Circuit for demodulating

a phase modulated signal", French Patent Application Number.: 10 02186, 2009) has been invented. The core of the invention is a 2-state phase detector principle. It is based on a phase to voltage conversion. The circuit summarizes the input phase deviations of the phase modulated bit. If the accumulated value reaches a defined value a phase change is detected by a comparator circuit. Additionally, the phase detector circuit is based on a two state mechanism. The two states are separated in two phase detector circuits. If phase detector 1 operates in state 1 phase detector 2 works in state 2 and vice versa.

- **state 1: voltage initialization/calibration phase**
  phase 1 is used to initialize the measurement at a defined voltage level. The current charge pump is disconnected during this time.
- **state 2: measurement of phase deviation**
  measurement of the input phase deviation is done in phase 2. The charge pump is connected to the measurement unit while the initialization circuit is disconnected. The phase angle is linearly converted to a voltage without signal distortion.

A detailed description of the 2-state phase detector is given in chapter 5.3.6.
Furthermore, a novel rectifier circuit has been invented ("Circuit and method for rectifying and regulating voltages", Patent Application, United States Appl. No.:11/948,037, April 2009). This rectifier circuit allows a lower output-voltage ripple and a lower voltage drop between the input and the output node.
It is recommended that further research be undertaken in the following areas:

- Increasing symbol order of multilevel modulation techniques for higher data rates than 27.12 Mbit/s.
- A reduction of the energy demand.
- A further increase of the phase resolution of the phase demodulator ($< \pm 3^\circ \widehat{=} \pm 615\,ps$).
- The analog PLL can be replaced by an analog/digital phase-locked loop. In this case, the analog filter is replaced by a digital filter, the V/I converter by an ADC, the current controlled oscillator (ICO) by a digital controlled oscillator (DCO) and the phase frequency detector by a time to digital converter (TDC). This modification has a potential for improvement concerning a better hold-mode behavior (open-loop stability).
- Further research might explore the possibility of using different frequencies for data and energy transmission.

Analog/Digital Phase Locked Loop

As already mentioned, the analog phase locked loop (APLL) can be replaced by an analog/digital phase locked loop (ADPLL). The drawback of the APLL is the time-limited hold-mode (open loop). In figure 6.1 the simulated ADPLL is shown, which includes the PFD, the 10-bit counter, the high-frequency oscillator, the control unit, the 10-bit digital to analog converter, the current controlled oscillator (ICO), the 2^{nd} order filter and the 1/N divider stage. The combination of the 10-bit counter and the high-frequency oscillator can be interpreted as a time to digital converter (TDC). It converts the PFD output pulses into a digital equivalent. Analogous to the APLL the ADPLL is locked when the frequencies of the inputs of the PFD are equal and when the inputs are in phase.

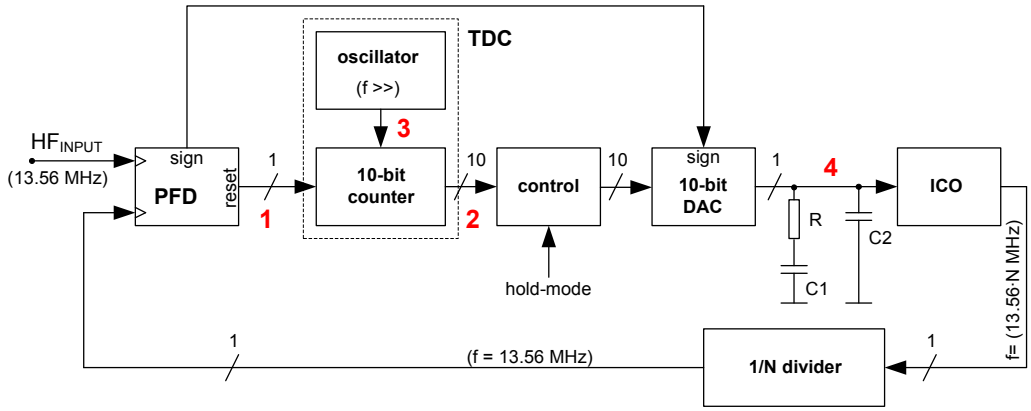


Figure 6.1: Digial Phase Locked Loop

Figure 6.2 shows the functional principle of the ADPLL. If a phase deviation (figure 6.2a) occurs the 10-bit counter starts to count the pulses (figure 6.2c) of the high-frequency oscillator (figure 6.2b). Then the final counter value is converted to a corresponding current value which sources the second-order filter (figure 6.2d). Due to the resulting voltage value at the filter node the ICO outputs a clock signal.

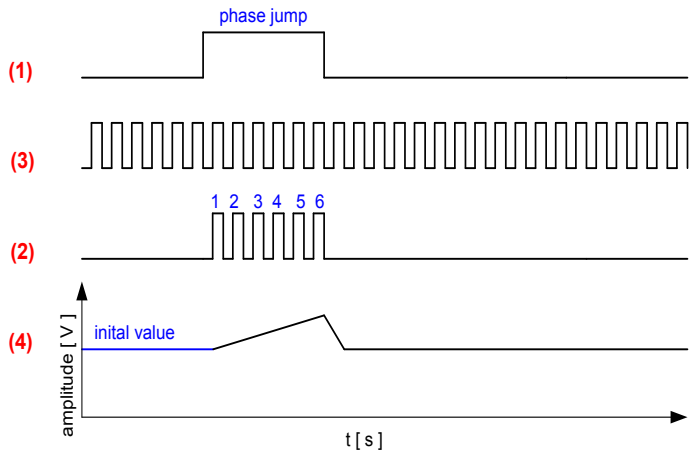


Figure 6.2: ADPLL principle

The benefit of the ADPLL is that the 10-bit counter value can be stored by a digital part when the PLL inputs have the same frequency and they are in phase. If the 10-bit value is stored the loop will be opened by the control unit. At the same time, the PLL input clock signal is compared with the ”stored” PLL output clock signal by a phase detector. Here, the phase detector extracts the phase jumps of the incoming signal.

Comparison of several proposals for VHBR RFID systems

There are some documents which deals with the field of high bit rates in RFID applications. But most of the described systems are based on an external power supply, an external clock signal and/or discrete circuit components.
But the proposed system operates with a extracted power supply and clock from the incoming high-frequency field and is integrated on a test chip.

Selected works:

“High Speed RFID/NFC at the Frequency of 13.56 MHz” [49]:

In the paper ”High Speed RFID/NFC at the Frequency of 13.56 MHz” an implementation of a lab scaled prototype with a transmission rate of 6.78 Mbit/s from transponder to reader (uplink) is demonstrated and discussed. It should be pointed out that is also possible to achieve high bit rates from transponder to reader. But there is no suggested solution given to realize high bit rates from reader to transponder. Furthermore the prototype is only based on a discrete circuit, not an integrated version on a test chip.

“Demonstrator für hochratige RFID- und NFC-Systeme”[69]:

This diploma thesis deals with the development of a ”demonstrator” platform that demonstrates the data transmission with a data rate up to 6.78 Mbps from transponder to reader. The demodulator is based on a FPGA prototyping system with discrete devices as well as the previous paper.

“Fully Asynchronous Contactless Systems, Providing High Data Rates, Low Power and Dynamic Adaptation” [20]:

This paper shows an implementation of a demodulator concept with an asynchronous event-based communication (Cyclic Asynchronous Code (CAC) with 4 phase states). Here, bit rates up to 1.02 Mbit/s are possible from transponder to reader. But the achieved bit rates are still eight times lower than in the proposed demodulator concept in this thesis.

“Wireless Interface dedicated to improve Power Transfer Efficiency and bi-directional Data Communication of implantable Electronic Devices”[33]:

This paper presents an integrated BPSK demodulator for bit rates up to 1.12 Mbit/s.

“Contactless Demonstration Reader Frontend for Very High RX Data Rates”[57]:

This paper presents a prototype that is able to receive data frames at bit rates up to 3.4 Mbit/s. The prototype is based on a discrete I/Q demodulator circuitry of the reader (transmission direction - transponder to reader) and is not integrated on a test chip. This is realized with an analog front-end (demodulator) and a digital back-end (decoder). The load modulated carrier signal is first demodulated by the analog demodulator. After that, the digital decoder, implemented on an FPGA, demodulates the subcarrier and decodes the data.

“Contactless Demonstration Reader Decoder Optimization for Receiving Very High Bit Rates”[46]:

The paper discusses a smartcard demonstration reader that is capable to receive data rates as high as 3.39 Mbit/s. The aim of this work was to optimize the decoder’s performance, it is also not integrated on a test chip (transmission direction from transponder to reader). The reader consists of an analog front-end (demodulator, filter, 8-bit ADC) and a digital backend (digital decoder).
A summary of the previous papers are given in table 6.1. It can be seen that the achieved bit rates in the compared documents are much lower than in the proposed system in the thesis at hand. There are several papers, which operate outside the frequency band of 13.56 MHz, but these frequency bands are not discussed in this thesis.

Table 6.1: Different demodulators/analog front end for high bit rates:

document type	author/commitee	maximum bit rate reader→transponder	maximum bit rate transponder→reader	CMOS-process	VDD
conference contribution [49]	C. Patauner, H. Witschnig, D. Rinner, A. Maier, E. Merlin, E. Leitgeb	n/a[a]	6.78 Mbit/s	n/a	n/a
diploma thesis [69]	Michael Roland	n/a	6.78 Mbit/s	n/a	n/a
conference contribution [20]	D. Caucheteux, Edith Beigné, E. Crochon, M. Renaudin	1.02 Mbit/s[b]	n/a	130 nm	1.2 V
dissertation [33]	Yamu Hu	1.12 Mbit/s	n/a	180 nm	1.8 V
diploma thesis [57]	Philip Oberstaller	n/a	3.4 Mbit/s	n/a	n/a
diploma thesis [46]	Daniel Kusternigg	n/a	3.4 Mbit/s	n/a	n/a
ISO/IEC 14443-2 FDAM 2 [38]	ISO/IEC JTC 1	848 kbit/s	848 kbit/s	n/a	n/a
ISO/IEC 18000-3 [39]	ISO/IEC JTC 1	424 kbit/s	8·106 kbit/s (8 channels)	220 nm	1.5 V
thesis at hand	Markus Auer	13.56 Mbit/s	6.78 Mbit/s	90 nm	1.35 V

[a] 6.78 Mbit/s, but with introduced external clock and without integrated solution
[b] for biomedical applications

7 Outlook

Outlook

In the course of time the demand for higher bit rates will continue to grow. This also includes the field of RFID applications. The ISO/IEC 14443 offers communication data rates from 106 kbit/s up to 848 kbit/s. The test results of the proposed demodulator circuitries show that it is possible to integrate a low power analog front end with higher bit rate recognition.
Different methods are being tested, for instance an AFE with an AM demodulator and an AFE with a PM demodulator. It has been shown that the data from a PM signal can be extracted up to a bit rate of 13.56 Mbit/s. Furthermore, the demodulator circuits are downward compatible and also support standardized bit rates of 106 kbit/s, 212 kbit/s, 424 kbit/s and 848 kbit/s.
It is current a trend for high bit rates in RFID applications. There are a lot of standardization activities with respect to high data rates under way. Research is in progress for high data rates in order to force a revision of the standard ISO/IEC 14443. The findings of the underlying project provide the capability to directly influence the recent activities of standardization.

8 Project Schedule

The project was divided into the following four work-packages:

- WP1: Requirements specification
- WP2: Feasibility studies
- WP3: Prototype system realization
- WP4: Project management

Furthermore, two diploma-theses and one project-thesis have been completed, within the VHBR project of ReadRF:

- Matthias Pichler: ”Implementation of a digital demodulator to process high data rates in contactless applications (13.56 MHz)” (Diploma-Thesis, completed 5/2009)
- Matthias Emsenhuber: ”Development of an analog front-end for an RFID reader for high datarate” (Diploma-Thesis, completed 9/2008)
- Matthias Pichler: ”Verification of a contactless transponder ICs” (Project-Thesis, completed 6/2008)

Project ReadRF (long title: Reader Technology for logistic challenges with contactless identification devices) was started by March 1^{ST}, 2007. For the prototyping system technologically critical modules have been integrated into test chips, while the digital part was realized as FPGA. Bi-weekly meetings were held to consider the current project status and to discuss further steps and work.
Every 3 to 4 months detailed presentations were held to define the project status. The project phases were written down in two documents.
The first project phase *WP1: Requirement Specifications* were merged into a common *ReadRF-Hardware-Requirement-Report* and the second part *Very High Baud Rate (VHBR) Theory and Options* was summarized in the *ReadRF-Modulation-Demodulation-Report*.
Thereby the feasibility study includes the reader feasibility system and the transponder feasibility system. As a result the Milestone 1 (Requirement) was finished.
First silicon samples were finished in July 2008 and the Milestone 2 (Feasibility System) could be finalized. After the finalization of the first test chip an FIB (Focused Ion Beam) call was done to optimize the test chip.
The aim of work package three WP3 (Prototype System Realization) was the further increase of the baud rate. The design was processed in a second shared reticle run in May 2009 and was improved by a metal change in September 2009.
For further improvement of the analog front end and the demodulator circuits a third test chip was fabricated in May 2010. This test chip is able to detect bit rates up to 13.56 Mbit/s and has the capability to recognize data with a bit rate above 13.56 Mbit/s.

9 Appendix

9.1 Fundamental Equations and Relationships

Equations 9.1 and 9.2 show the general way to calculate the quality factor [25]. The quality factor depends on the resonance frequency f_{RES} and the bandwidth BW, which means that the quality factor is inversely proportional to the bandwidth. It can be inferred from this equations that the bandwidth has to be big enough for high speed data communication.

$$Q = \frac{f_{RES}}{BW} \tag{9.1}$$

$$Q = \frac{2 \cdot \pi \cdot f_{RES} \cdot L_{COIL}}{R_S} = \frac{R_P}{2 \cdot \pi \cdot f_{RES} \cdot L_{COIL}} \tag{9.2}$$

Table 9.1 shows the comparison of different modulation types. The minimum bandwidth represents the minimum required transmission bandwidth when R is the bit rate. It can be seen that the BPSK and QPSK have the same bit error performance. The formula below stands for unipolar modulation types.

$$erfc(x) = \frac{2}{\sqrt{\pi}} \cdot \int_x^\infty e^{-u^2}\, du \tag{9.3}$$

Table 9.1: Comparison of digital modulation methods. Two different system parameters are analyzed more closely in the course of the feasibility study, namely the minimum required bandwidth and the bit error rate for coherent and non-coherent demodulation methods.

Type	Minimum Bandwidth (BW)	Error Performance	
		Coherent	**Noncoherent**
ASK	R_{MAX}	$\frac{1}{2}\, erfc\sqrt{\frac{E_b}{2\,N_0}}$	$\frac{1}{2}\exp^{-\frac{1}{2}E_b/N_0}$
BPSK	R_{MAX}	$\frac{1}{2}\, erfc\sqrt{\frac{E_b}{N_0}}$	**None**
FSK	$2\Delta f + R_{MAX}$	$\frac{1}{2}\, erfc\sqrt{\frac{E_b}{2\,N_0}}$	$\frac{1}{2}\exp^{-\frac{1}{2}E_b/N_0}$
QPSK	$\frac{R_{MAX}}{2}$	$\frac{1}{2}\, erfc\sqrt{\frac{E_b}{N_0}}$	**None**

E_b = energy per bit

N_0 = noise power spectral density

M = symbol order

R_{MAX} = maximum bit rate

r = roll-off factor

R_S = series resistance

R_P = parallel resistance

L_{COIL} = coil inductance

The relationship between the transmission bandwidth $BW\,[Hz]$, the maximum data rate $R_{MAX}\,[Bit/s]$, the roll-off factor r and the symbol order M is given in equation 9.4.

$$BW = \frac{R \cdot (1+r)}{2 \cdot log_2(M)} \tag{9.4}$$

Above all, the maximum data rate R is limited by the channel capacity.

9.2 Phase Deviation - Amplitude Equivalent

In paper [1] (Auer et al., 2008) a novel phase demodulation technique was discussed and three different phase demodulation concepts were compared. But an analysis and comparison of an amplitude and a phase input modulated signal at transponder side is missing.
To extract data bits emitted by the reader, a clock extraction unit and a demodulator circuit are necessary. Therefore the clock extraction circuit has to be highly independent as possible of any V_{DD} variation. In the following a threshold decision with a simple sinusoidal signal is discussed in detail.
Figure 9.1 shows a half-wave of an analog front end input signal with two different amplitude levels. The threshold value was chosen to be 50% of the maximum amplitude peak value. The intersection line crosses with the input signals. Intersection points depend on the amplitude level of the input signal and the threshold value of the clock extraction unit.

Deltax represents the time variation of the two input half-waves. The time variation Deltax [in nanoseconds ns and degree °] over the amplitude variation of the inner signal [in V and %] is shown in figure 9.2. Due to the amplitude level-phase shift (deltax) relationship, a dependency can be noticed between the phase modulation and the amplitude modulation technique.

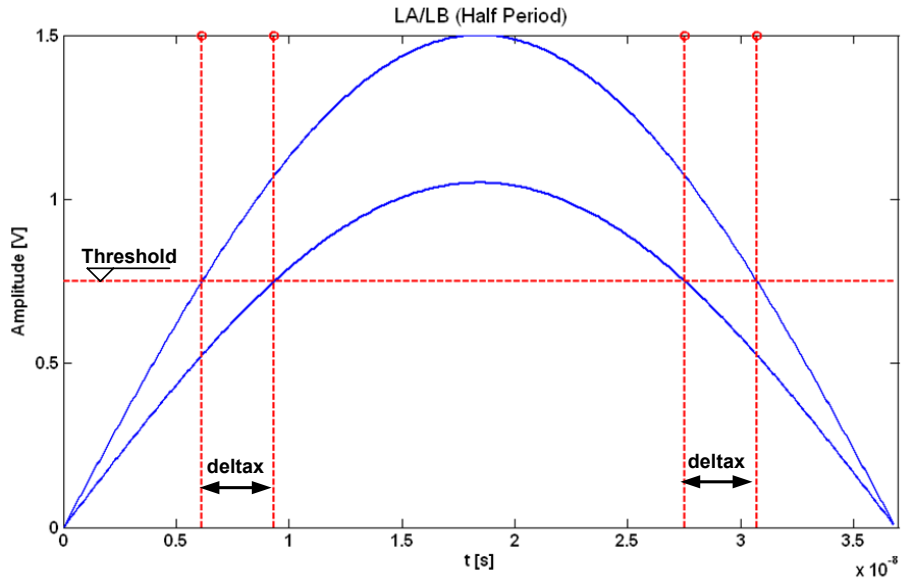


Figure 9.1: Different Amplitude Levels (Threshold 50%). The clock extraction unit should have a small threshold voltage input value to minimize the dependency on amplitude fluctuations.

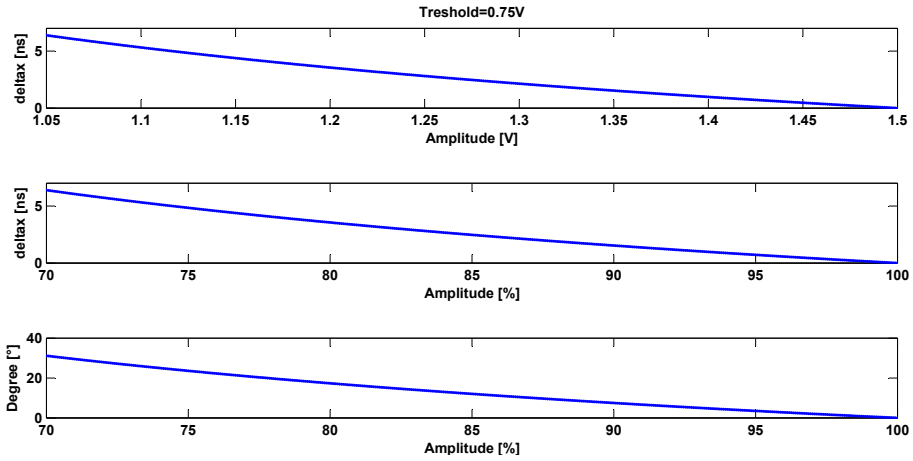


Figure 9.2: Different amplitude levels (threshold value = 50% of the maximum amplitude). The relationship between an amplitude change and the output pulse width (phase deviation) is shown.

9.3 Clock Extraction Circuit

In order to work against the dependency between the phase and amplitude deviation a modified clock extraction unit has been introduced. There are two circuits possible to extract the clock from the incoming phase modulated signal, a circuit based on a simple inverter structure or a differential amplifier. An inverter structure leads to the dependency between amplitude variations and the phase information of the phase modulated input signal as described before. A simple differential amplifier suppresses this phenomenon, because the threshold level is much lower than in the case of an inverter circuit. One method to implement such a clock extraction unit is shown in figure 9.3. The clock extraction circuit consists of the comparator with PMOS transistors $P_1 \ldots P_4$ and NMOS transistors $N_1 \ldots N_4$, the current source I_{REF} and the output driver with PMOS transistors $P_7 \ldots P_{10}$ and NMOS transistors N_5, N_6. At the gates of PMOS transistor P_1 and P_2 there are the input signals CLK_{IN1} and CLK_{IN2}. So the input signals are derived from the half-wave signals at nodes LA and LB. The output drivers are sourced by the reference current to reduce the supply-voltage dependency.

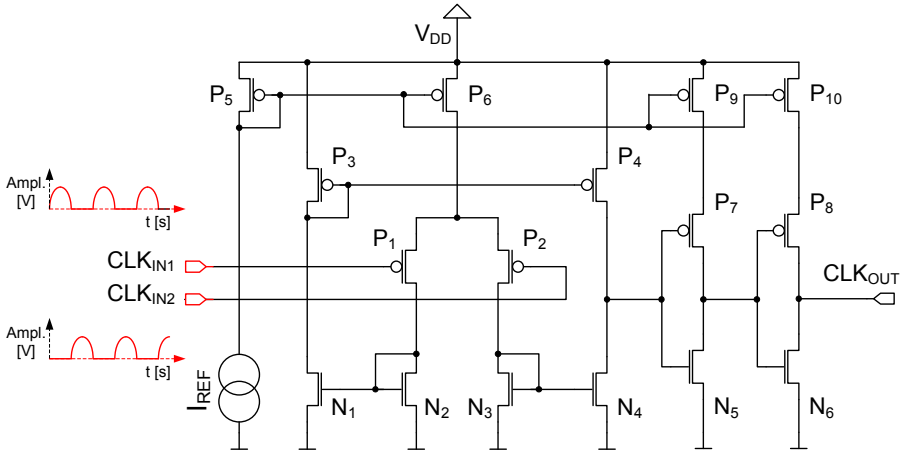


Figure 9.3: Clock extraction unit. For the clock extraction a clock recovery unit with less dependency between amplitude fluctuations at the input and associated output phase variations is necessary. In this case the threshold value has been decreased by the usage of a comparator stage. Moreover, the output inverters are sourced by a constant current source.

With the help of the clock recovery circuit a 13.56 MHz clock signal can be extracted from the incoming high-frequency input signal. It is also possible to generate a 27.12 MHz clock signal with two clock recovery units. In this case the first and second clock recovery unit have exchanged inputs. Both outputs of the clock recovery units are connected to the inputs of an OR-gate. This OR-gate outputs the 27.12 MHz clock signal. This clock is required by the digital part.

9.4 ADC-Output Linearity

As already mentioned, a low power ADC has been designed and implemented on a test chip. For multilevel phase detection the phase demodulator ADC has to be linear over different phase jump values. To illustrate this, figure 9.4 shows the measured ADC output value at different phase jump values. The ADC is discussed in chapter 5.4.1. It consists of a capacitor array, which is sourced by a current mirror array.

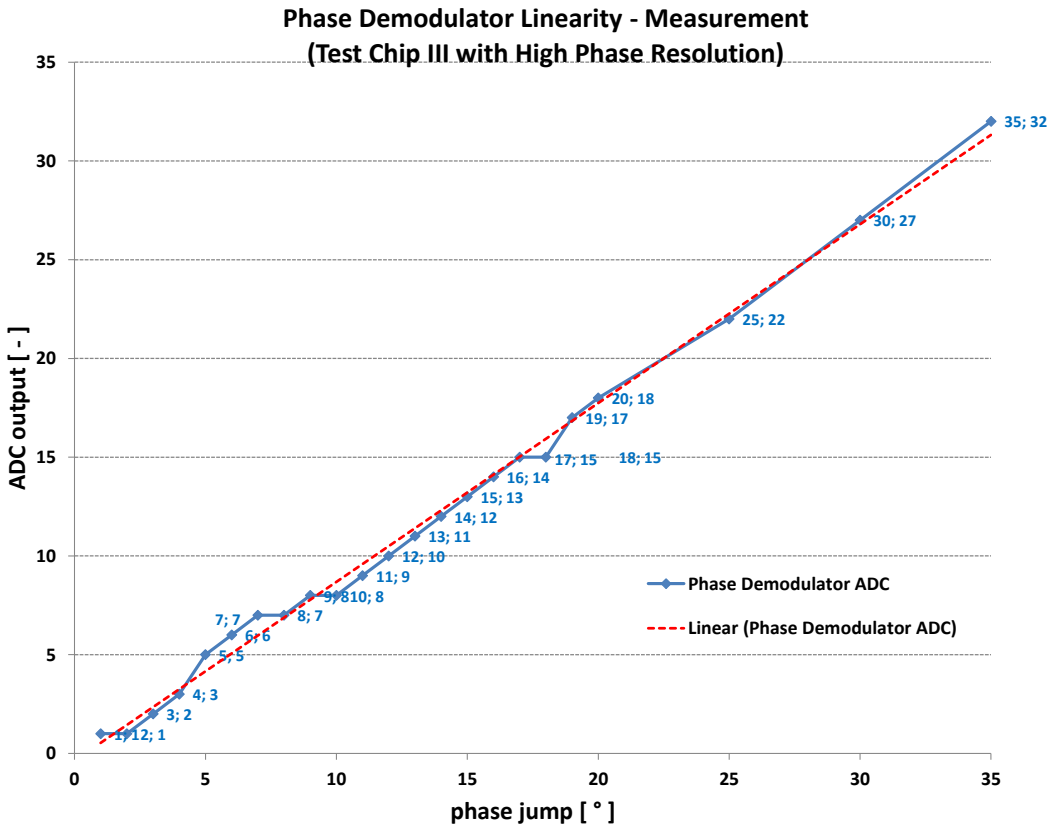


Figure 9.4: ADC output characteristic.

Due to the non-ideal matching of the current mirrors and the process variation of the capacitor array the ADC linearity deviates from the ideal line (dashed red line). Additional linearity error is caused by measurement inaccuracies. But the phase resolution of the phase demodulator is ± 3 degrees which mean that the phase demodulator accuracy is high enough.

Schematics

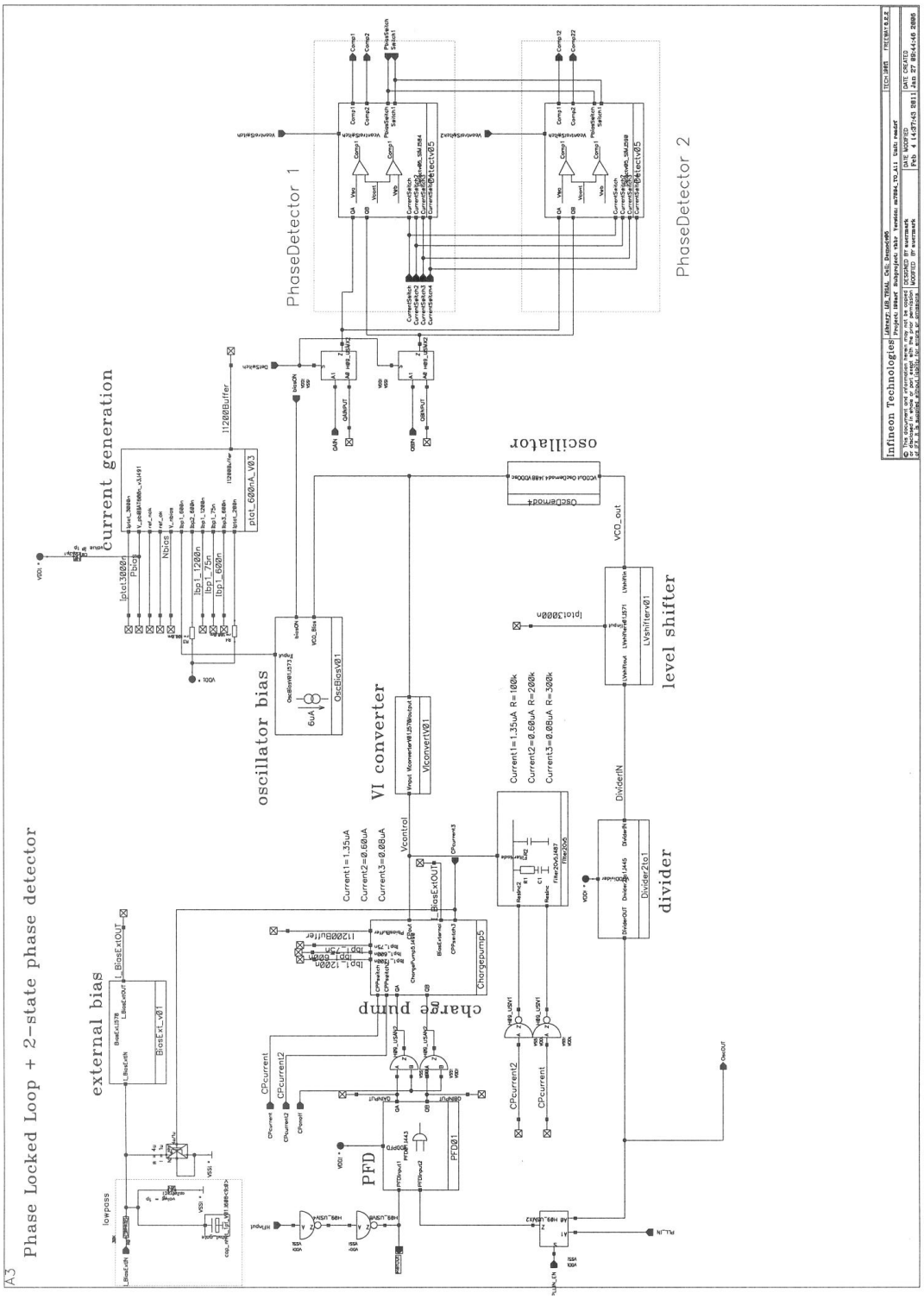


Figure 9.5: Test chip I: phase demodulator

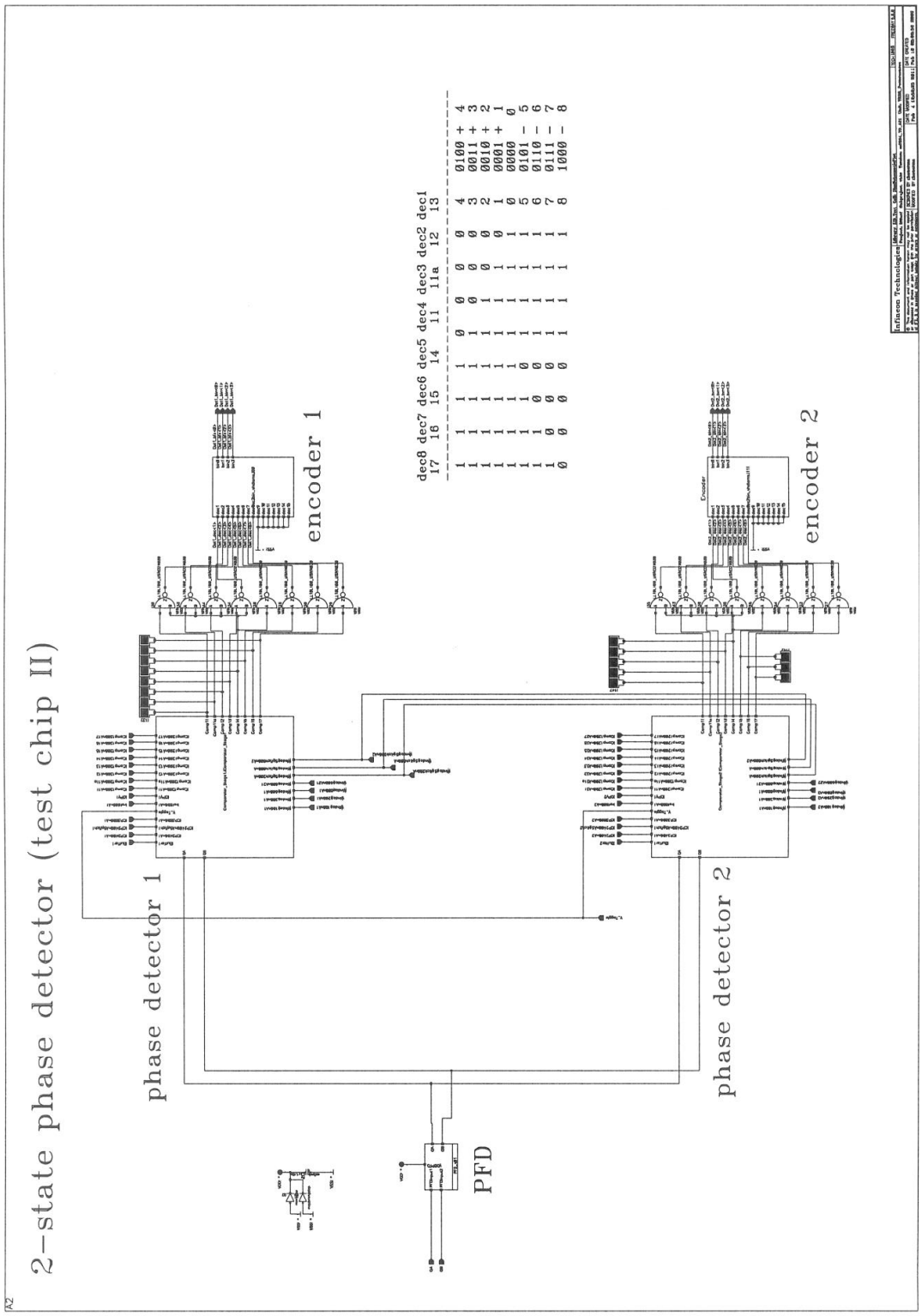


Figure 9.6: Test chip II: 2-state phase detector

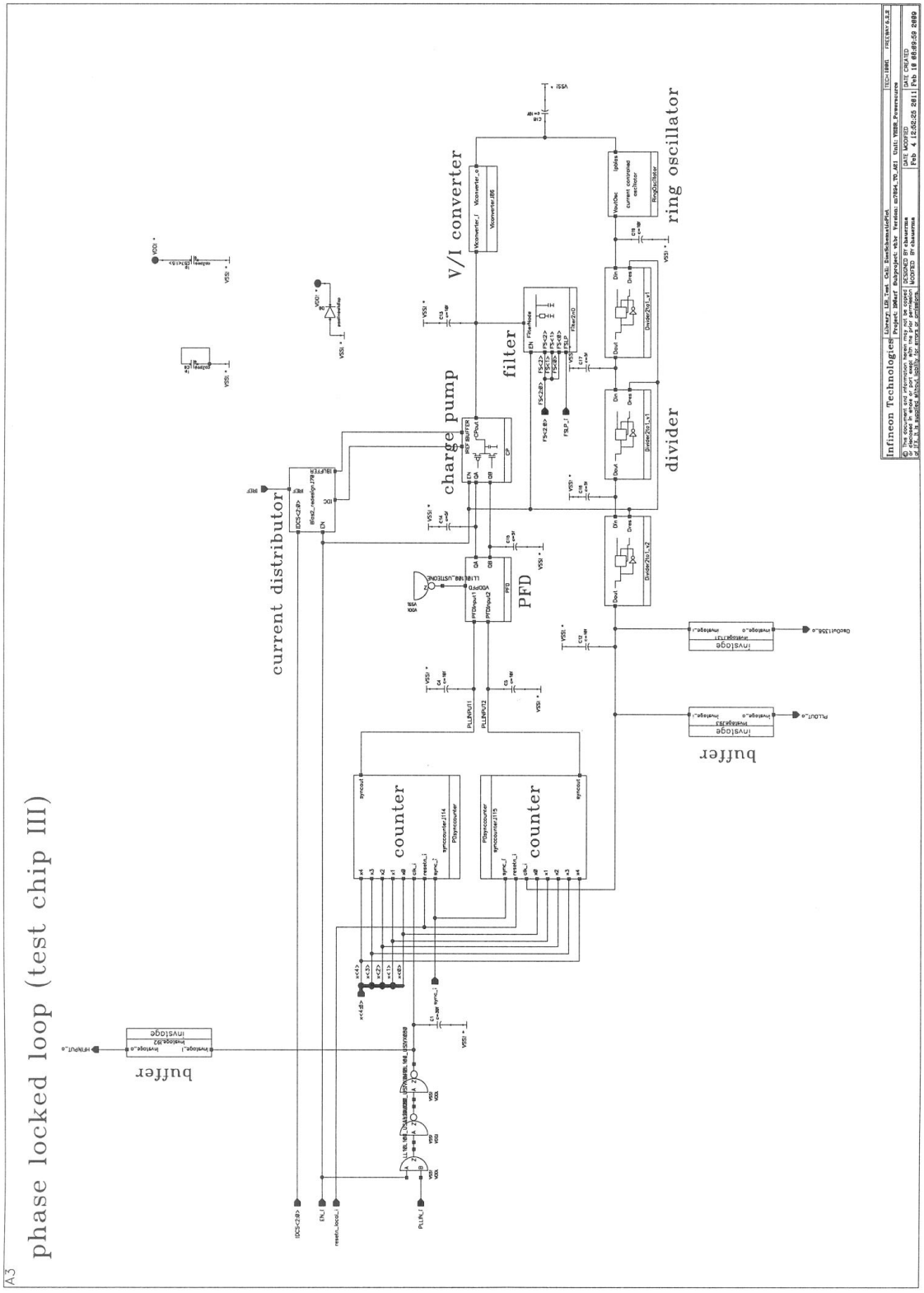


Figure 9.7: Test chip III: phase-locked loop

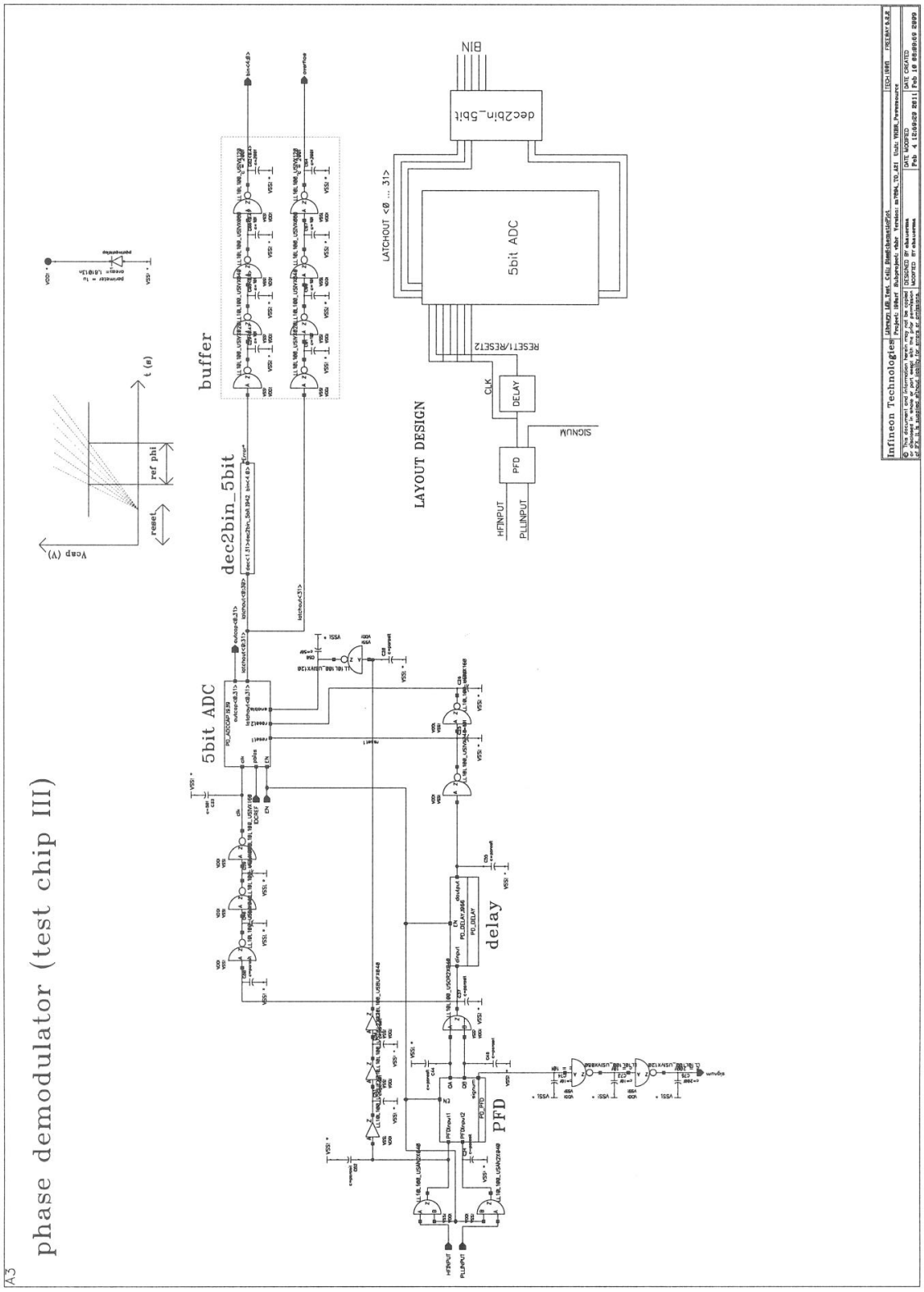


Figure 9.8: Test chip III: phase detector (1/2)

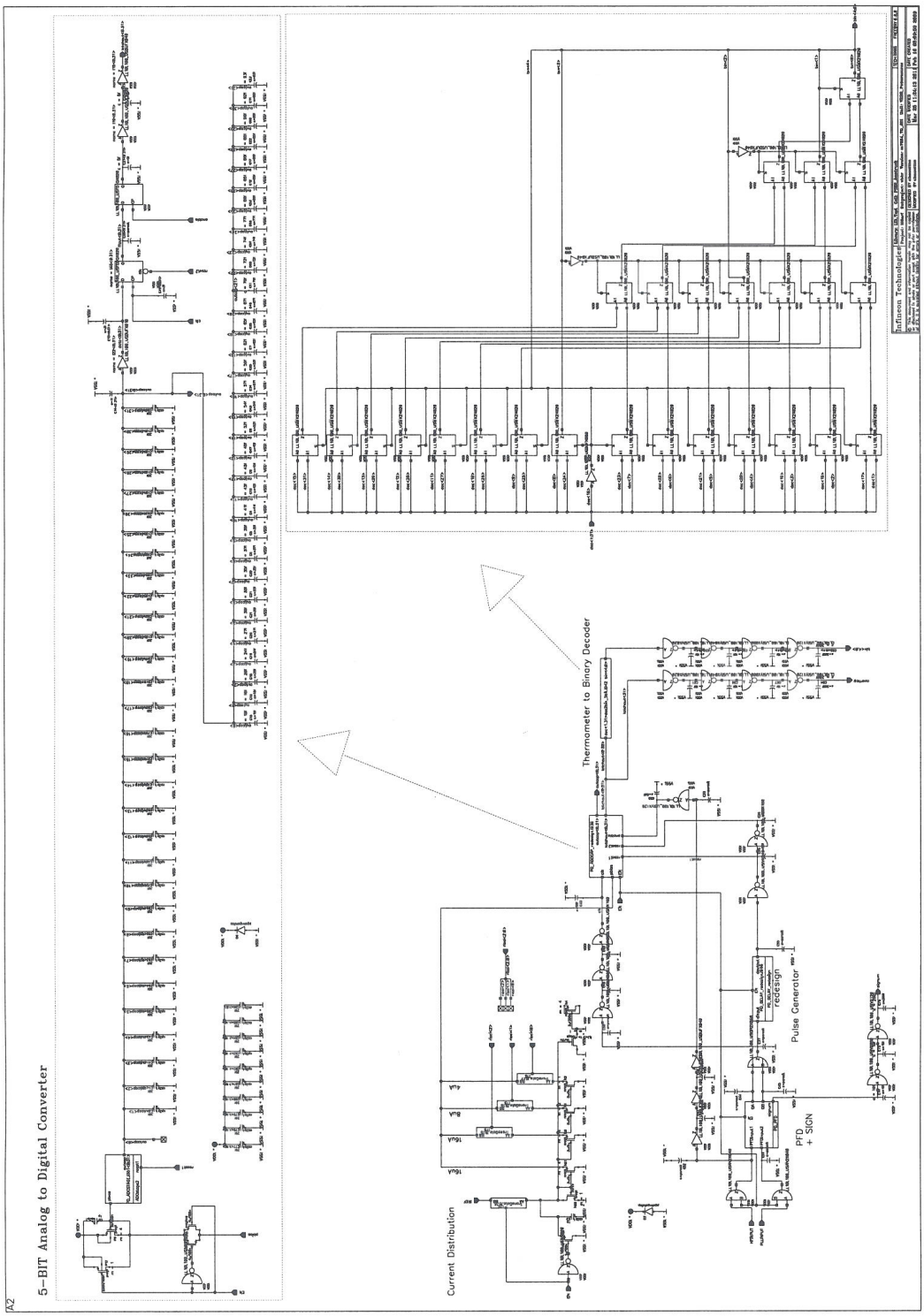


Figure 9.9: Test chip III: phase detector (2/2)

Own Publications

Paper

- Markus Auer, Edmund Ehrlich, Albert Missoni, Walter Kargl, Gerald Holweg and Wolfgang Pribyl. *Design and development of a mixed signal prototyping system to achieve very high data rates for contactless applications*. Wien, New York: Springer, e&i March 2008
- Markus Auer, Edmund Ehrlich, Albert Missoni, Walter Kargl, Gerald Holweg and Wolfgang Pribyl. *Analoge Eingangsstufe mit ADC-basierendem Demodulator für HF-Transponder zur Verarbeitung hoher Datenraten*. Wien, New York: Springer, e&i August 2009
- Markus Auer, Edmund Ehrlich, Wolgang Pribyl, Albert Missoni and Walter Kargl., *Design und Entwicklung eines Mixed Signal Prototyping Systems für RFID Applikationen mit Datenraten grösser 848 kbit/s*. Workshop on Microelectronics, Austrochip 2009, October 2009
- Markus Auer, Albert Missoni and Walter Kargl. *HF RFID Transponder with Phase Demodulator for Very High Bit-Rates up to 13.56 Mbit/s*. RFID conference, IEEE RFID 2010, April 2010

Invention Disclosures and Patent Applications

- Christian Klapf, Markus Auer and Guenther Hofer, *Circuit and method for rectifying and regulating voltages.* Patent Application, United States Application Number.:7 738 272 B2, June 2010
- Walter Kargl, Markus Auer and Albert Missoni, *Circuit for demodulating a phase modulated signal.* French Patent Application Number.: 10 02186,
  United States Appl. No.:US 2010/0303173 A1, December 2010

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[7] Walter Kargl, Markus Auer and Albert Missoni. *Circuit for demodulating a phase modulated signal.* French Patent Application Number.: 10 02186, US Patent Application Number.: US2010/0303173 A1, December 2010

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