Design of an Analog Interface for Frequency Band Comprehensive RFID Systems

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Graz, Juni 2010

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Kurzfassung

In passiven RFID Applikationen haben sich drei Frequenzbänder - LF, HF und UHF - durchgesetzt. Welches Band eingesetzt wird, hängt von den Bedürfnissen der Applikation, von den lokalen Regulatorien, der etablierten Infrastruktur oder zum Beispiel von den Herstellungskosten ab. Ziel dieses Projektes war es, einen RFID Chip mit angepasster Antenne zu entwickeln, der gemeinsam als Tag sowohl in einem standardisierten HF als auch in einem UHF Frequenzband mit entsprechenden Readern kommunizieren kann. Ebenso wird die durch den Reader generierte bzw. abgestrahlte Energie für die Versorgung des Chips herangezogen. Nach Auswahl des entsprechenden Frequenzbandes arbeitet der CTS Chip gleich wie ein handelsüblicher HF oder UHF RFID IC der nur auf einer Trägerfrequenz selektiv ist und auf diese optimiert wurde.

Der Schwerpunkt dieser Dissertation lag auf dem Entwurf und Entwicklung eines integrierten Schaltkreises, bestehend aus diversen Analogschaltung die für den Betrieb von mehrfach Frequenz selektiven RFID Chip notwendige sind und deren Verifizierung samt meßtechnischer Erfassung. Im Rahmen der Dissertation wurden neue Gleichrichter, Oszillatoren und Module für die kontaktlose Kommunikation vorgestellt. Der Chip wurde als Testchip in einer Infineon 120nm CMOS Technologie gefertigt.

Das Ergebnis dieser Arbeit sind drei neue Schaltungsarchitekturen für passive RFID ICs, die sowohl im HF als auch im UHF Band selektiv sind. Die Leistungsfähigkeit der Schaltungen wird in drei Kapiteln beschrieben und mit Simulationen bzw. Messungen untermauert. Es handelt sich bei dieser Arbeit um den weltweit ersten EPCglobal Transponder, der sowohl den HF als den UHF Standard unterstützt. Mittels eines Demonstrators (bestehend aus HF und UHF Reader, CTS Antenne und CTS Chip) kann die Leistungsfähigkeit verdeutlicht werden.

Abstract

In passive RFID applications three frequency bands predominate worldwide - the LF, HF and the UHF band. Which of these bands is finally chosen depends on the application, on the local regulations, on the established infrastructure or on the costs. The aim of this thesis was to develop an analog front-end together with a digital control unit which can work together with a multi frequency selective antenna. This bundle should be able to communicate in standardized HF or UHF frequency bands with corresponding readers. The generated and radiated field of the reader antenna will be used to power the chip. After selection of the corresponding frequency band, the CTS chip behaves equivalent to a single frequency chip which is selective only in one carrier frequency.

The focus of this thesis is the development and the design of an integrated circuit for this purpose. This circuit consists of a chip - antenna interface and an integrated analog unit which is necessary for a multi frequency selective RFID chip. New rectifier architectures, local oscillator concepts and modules for the contactless communication are presented in this thesis. The test chip has been manufactured in a low cost 120nm Infineon CMOS process.

The results of this project are three new design architectures for low power RFID applications. The performance of the introduced circuits are presented in three chapters of this thesis and are confirmed by simulations and measurement results. This work presents the very first EPCglobal chip which supports both the HF and UHF standard. A fully functional demonstrator (composed of HF and UHF reader, CTS antenna and CTS chip) represents the capability of the CTS transponder.

Acknowledgements

During this project I was working part-time at Infineon Technologies Design Center Graz as a system engineer and analog designer responsible for analog front-ends which are used in contactless Smart Cards. It was a pleasure for me to meet many people who I would like to thank in the following:

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Special thanks to my colleague Dipl.-Ing. Günter Hofer from Infineon Technologies for the introduction into the field UHF RFID engineering and especially for the great layout support.

Thanks also to my colleague Dr.techn. Dipl.-Ing. Christian Klapf for many discussions and his helping hand before tape-out.

I would also like to thank Dipl.-Ing. Johann Heyszl for providing an efficiently working digital EPC state machine , for the good cooperation and the well implemented EPCglobal codec.

Without a compact antenna the best chip could not be presented in a performance demonstration. For the well working antenna I would like to thank Dr.techn. Dipl.-Ing. Lukas Mayer.

Finally, I would like to thank FIT-IT and Infineon Technologies for funding the CTS project.

Albert Missoni
Graz, June 2010

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Nomenclature

AC	Alternating Current
AFE	Analog Front End
AM	Amplitude Modulation
ASK	Amplitude Shift Keying
CCO	Current Controlled Oscillator
CL	ContactLess
CMOS	Complementary Metal Oxide Semiconductor
CTAT	Complementary To Absolute Temperature
CTS	Comprehensive Transponder Systems
DC	Direct Current
DUT	Device Under Test
EAS	Electronic Article Surveillance
EEPROM	Electrically Erasable Programmable Read Only Memory
ENOB	Effective Number Of Bits
EPC	Electronic Product Code
FIT-IT	Forschung, Innovation, Technologie - Informationstechnologie
GDS	Global Data Synchronization
HF	High Frequency
IC	Integrated Circuit
ICO	Current Controlled Oscillator
ID	Identification Number
ISM	Industrial Scientific and Medical
ISO	International Standards Organization
LF	Low Frequency

LO Local Oscillator

MIM capacitor Metal Isolator Metal - capacitor

MIT Massachusetts Institute of Technology

NVM Non Volatile Memory

OTA Operational Transconductance Amplifier

PCB Printed Circuit Board

PPM Parts Per Million

PTAT Proportional To Absolute Temperature

RF Radio Frequency

RFID Radio Frequency IDentification

RxD Receive Data

SCR Silicon Controlled Rectifier

TO Tape-out

TxD Transmit Data

UHF Ultra High Frequency

VCO Voltage Controlled Oscillator

1 Motivation - The CTS Project

Several ISM frequency bands are defined for RFID applications and so far three of them - LF, HF and UHF - have been established worldwide. To profit from frequency band synergies, a new chip for transport and identification will be developed during the CTS (Comprehensive Transponder Systems) project.

1.1 The CTS - Comprehensive Transponder Systems Project

As LF transponders are not used in transport applications because of higher transponder costs, size and low read distance, the CTS chip does not focus on this band. The next higher RFID frequency band is the popular HF 13.56MHz ISM band, which is approved worldwide with similar power levels; therefore it is the most universal frequency band. Tag operation distance is well defined to approximately half a meter with small reader antennas. In the UHF frequency band around 900MHz we have country specific frequency slots with different power levels. Already close to the micro wave band the popular 2.45GHz slot is also available for RFID applications. All UHF 900MHz low power tags are designed for far field operation and can reach a distance of about 5 meter. Electrical far field radar reflections are typical for higher frequencies where the wave is already solved from the antenna. The low damping factor in the far field causes a maximum tag operational distances of 10 meter [LKL06]. Compared to HF, this 20 times higher distance could also be a disadvantage when privacy or other reasons for a reliable low distance operation are desired. Shielding or multiple reader systems with distance estimation are necessary for a traceable reduced operation distance. Both methods to reduce the UHF operation distance are very expensive compared to the new CTS proposal. Material sensitivity of radiated waves could also be a reason to go either for a UHF- or for a HF - RFID system [BMU09]. In table 1.1 some differences and affinities of the three most frequently used RFID bands are shown. It illustrates the specific benefits of each frequency band.

The aim of the frequency band comprehensive project is to combine a multiple selective antenna, a single port analog frontend and a digital control unit to one chip. The CTS demonstrator which consists of an antenna and an attached IC shows the benefits of a frequency band comprehensive transponder system.
To be cost-competitive, the CTS chip area of the analog and of the digital module are similar to single band products. Most of the chip modules are able to support the 13.56MHz HF band as well as the 900MHz UHF frequency band. Some minor modules are single frequency selective only. If both frequencies are applied simultaneously, the chip can choose which band will be the preferred one. Typically, the IC will prefer the HF band, because the transponder has to be very close to the reader antenna; therefore, the possibility of an intended HF communication is very high.
Moreover, the CTS antenna costs and performance should be comparable to commercial HF coil

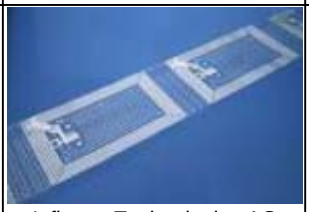
Frequency band	LF	HF	UHF
Frequency range	125/134kHz	13.56MHz	860 - 960MHz
Typical operating distance	10cm	50cm	5m
Tag costs	high	medium	low
Skin depth of water	8m	2m	4cm
Typical Tag design	 Sokymat ®	 Infineon Technologies AG	 Alien ®

Table 1.1: Most common frequency bands and characteristics

antennas. Finally, from the overall transponder cost point of view, the CTS chip can be compared to a typical HF tag and delivers the UHF functionality as an important additional feature.

The intent of this work was to design an analog front end for passive RFID with two antenna pads (single port) which can operate either in the HF or UHF frequency band. Power generation and communication units have to fulfill air interface requirements according to the chosen EPC-global specifications. A low cost 120nm CMOS Infineon process with EEPROM option was used without special RF transistors or Schottky diodes. Within the scope of the technology limitations, the chip performance was measured and compared to single frequency ICs. According to the chip input impedance, an impedance matching comprehensive transponder antenna was developed together with the Vienna University of Technology - Institute of Communications.

The chip was developed at Infineon Technologies Design Center Graz in cooperation with the Institute of Electronics at Graz University of Technology. The project was funded by the Austrian research funding agency FFG with the program FIT-IT and Infineon Technologies Austria AG.

This thesis comprises the development and design of the analog front end for the CTS chip. In the course of the project four new CMOS low power design concepts were developed and presented at international conferences [MKP+08] [MKH07] [KMP+08] [MHP10]. These design concepts are described in the following chapters of this thesis:

Chapter 4 - Power Generation Units
After a short introduction in Chapter 2 the power generation module, which is necessary for a good power performance, will be discussed and the new CTS power supply design architecture will be introduced. The final power path design is a compromise between the power generation performance for both frequency bands and a robust RxD and TxD communication. Also impedance matching between the analog front end of the IC and the selective CTS antenna will be mentioned. Several alternative rectifier concepts then will be reviewed. Finally, power path performance measurement results and the chip layout of this module will be illustrated in this chapter.

Chapter 5 - Clock Generation Units
Beside the HF clock recovery module, which derives the clock signal directly from the alternating coil voltage, a low-power local oscillator at about 2MHz is necessary. In this section, a new low-voltage and low-power relaxation oscillator will be presented and will be compared with conventional UHF RFID oscillator designs. Measurement results of several design studies and the module layout will conclude this chapter.

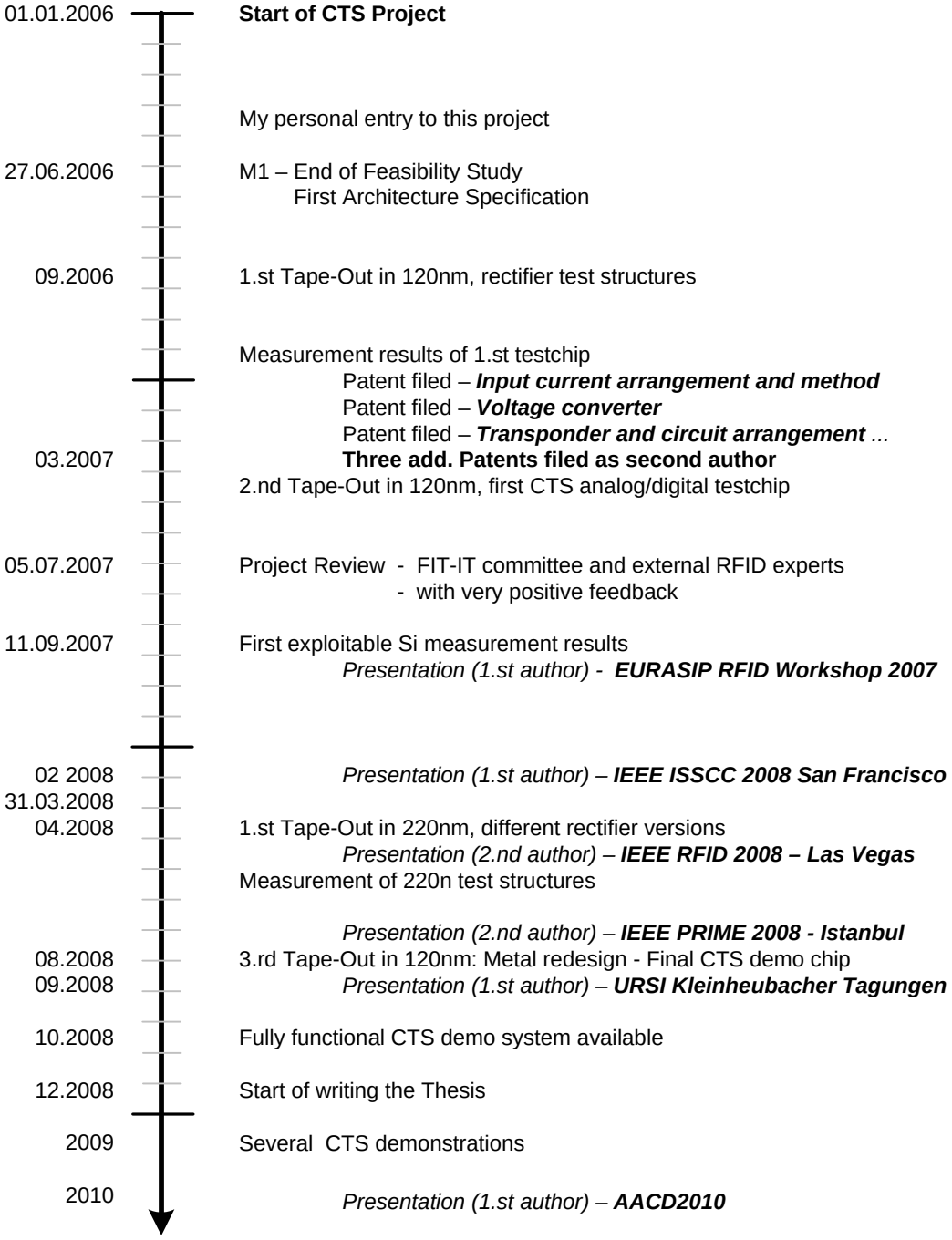
Chapter 6 - Contactless Communication Units
A new UHF RxD DC bias generation scheme and a new HF/UHF TxD unit applicable for both frequency bands will be introduced in this chapter. Due to this load modulator and backscatter concept not only the power transistor area but also the parasitic capacitance are reduced significantly compared to common modulator implementations.

Chapter 7 - Secondary Units and top cell
In this chapter, bias current and reference voltage generation will be shown. Next, minor modules like a power-down reset unit or the impact of the frequency band selector will be presented. Last, in the CADANCE top cell schematic all previously mentioned CTS modules will be shown interconnected.

Chapter 8 - Research Summary and Outlook
In the concluding chapter, the research and evaluation section of this thesis will be provided.. The extended research summary will mention all innovative highlights of this work and will refer to publications and submitted invention disclosures. Finally, an outlook with some ideas for future improvements will be listed.

1.2 Project progress

The time line shows the progress and achievements of the CTS project. The nominal duration of a FIT-IT funded project usually amounts to two years. As the last tape-out was delayed by half a year till summer 2008, the duration of the CTS project was extended by 3 additional months to the end of March 2008.



2 Introduction to passive RFID

RFID can be a major technology enabler or a simple supplement. RFID is already used in different quantity in payment, identification, supply chains, packaging, sensor network and many other applications. RFID is launched in the LF frequency band or even in the microwave band (SHF).

The bandwidth of these segments grows with inventive market requirements and with the corresponding technical RFID solution in response. A general passive RFID introduction will not be given in this thesis. Detailed information about the broad field of passive RFID can be found in literature [Fin06] [FKFS02] [Bak07] [Ker06] and [CH07].

EPCglobal AUTO-ID labs have defined UHF as the preferred RFID band and the latest EPCglobal Class-1 Generation-2 specification. Meanwhile, labs also have been working together with companies to establish an EPC standard for the 13.56MHz HF band, which will finally be similar to existing standards. The availability of similar standards for two frequency bands favors EPCglobal to be used in the CTS chip. A short general historical survey about the origin of the EPC standard and about the current efforts to establish RFID as one important EPC medium will be given in the following:

2.1 EPC Standard linked with Passive RFID

Using the Electronic Product Code (EPC) it is possible to identify every object with an ubiquitous and globally singular code. Attached to a worldwide network and compatible software infrastructure - to the Global Data Synchronization (GDS) - it should be possible to define the appearance of each object in the database or to get information from each EPC tagged object [Eng02]. In 1999, the first AUTO-ID Lab Center was established at the MIT in Chicago. In the following years several centers were set up all over the world. Soon a RFID supply chain management flow was established and finally standardized. AUTO-ID lab recommends the 900MHz UHF band as target frequency band because of its increased read distance and additional high data-rate compared to former established RFID standards. Only a well defined small memory size is necessary to store the EPC number [War06]. All these restrictions will result in a small and cheap EPCglobal compliant chip. In UHF, the antenna can be designed within one metal layer which is also cheaper compared to lower frequency coils.

EPC air interface standards Class 0 and Class 1 were defined in the early AUTO-ID Lab formation phase. As these two additional standards are not compliant and not optimized for EPC requirements, the new Class1 - Generation 2 standard was ratified 2006 by the Internal Organization for Standardization as ISO 18000-6C [Bak07] [Ker06] [EPC07a]. In 2005, Wal-Mart in the USA and Metro in Europe already started to use tagged pallets and transport cases in the commercial logistics flow.

A pre-released EPC specification - the ”HF Version 2 Draft Version 0.3” [EPC07b] - was published in 2007, is very similar to the UHF EPC specification and it also shows affinity to the HF vicinity standard. An official HF Generation 2 tag protocol standard is still not available and will be published soon at $www.epcglobalinc.org$. We started the CTS project with the very first Version 0.0 and modified our latest CTS product according to Version 0.3.

Why use RFID alongside bar-code or other printed optical coding concepts which are unrivaled in price? Some benefits of an EPC RFID supported logistics chain could be:

- Increased speed of supply chain cycles - all items are recognized quickly worldwide by an unique code
- It is not necessary to search for the barcode on the product any more
- Additional electronic information can be stored directly on this item
- EAS anti-theft protection combined with smart-shelf technology alerts the staff earlier [Sys03]
- The chip can be locked with a key and a kill command. No information is passed over to unknown individuals.

Obviously, there are also concerns about data privacy and data security or production cost disadvantages when RFID is used instead of printed paper labels. However, to balance the pros and cons of using RFID for an application is the task of the systems integrator after all.

2.2 CTS transponder - An application example

Let me take transport and logistics to explain and show the benefits of using a multi frequency RFID tag. Figure 2.2 shows products which are manufactured in a factory, stored and finally carried on transport vehicles to local outlets or international key account customers. On several items, a CTS transponder is attached. The question is when to use either the HF or the UHF band for communication. The customer could decide to use one of the two frequency bands for best performance. One feasible fragmentation for a transport application is shown in figure 2.1. When individual items are programmed, operation distance should be short and reliable because only this target unit in front of the reader antenna should be programmed and prepared. For this application, it is appropriate to use short-range HF RFID. For capturing the according IDs of items in a region around the reader antenna, a far distance application like RFID UHF is necessary. This hierarchy view is transformed into the transport flow shown in figure 2.2. In this example, the customer would like to get the products packaged in a cardboard box. 6 items of type 1 and 3 items of type 2 should be placed into each box. To be able to track each item stored in the container already during the production phase, each product is signed with its unique ID (identification number) with the help of an HF reader. The type of product is also stored in the tag memory. When the box is carried into the factory store, a final scan with a UHF reader could read all items at once and check each box for completeness. A central computer records all incoming and outgoing products and guarantees an accurate manufactory store data base. On each pallet a CTS tag can be accessed by an HF reader. This HF reader is mounted on a fork-lift truck to

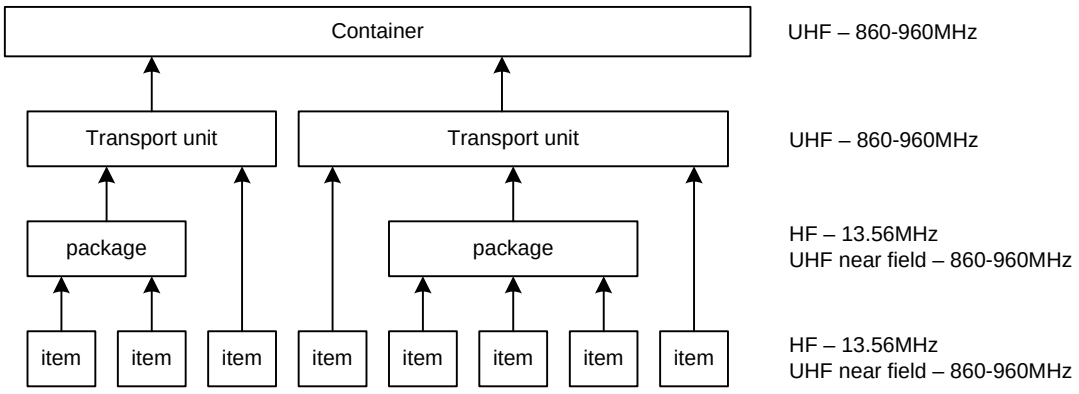


Figure 2.1: HF and UHF RFID systems in transportation

check if the driver has taken the right pallet. Finally, outside on the container skin one CTS chip packaged in a special outdoor label could store the content of the container.

2.3 EPC Global Regulations

Why did we choose EPC HF and UHF as air interface standard?

Digital:
In a CTS related diploma thesis by Johann Heyszl [Hey07] a detailed comparison of how to merge different RFID standards into one homogeneous digital interface was performed. The result was a clear preference for a combination of the EPCglobal version 2 standards (UHF Gen2 and HF version 0) because both use the EPCglobal UHF Gen2 logic layer. Digital encoder and decoder are very similar and the number of gates overhead is small. Also a control logic for analog modules was implemented in the digital unit.

Analog:
For the analog power generation unit, the big frequency step of a factor of 64 between HF and UHF frequency bands was more significant than the question of the chosen protocol standard. Only two RF pads and a high reuse of transistors are the essential goals of the CTS project in order to minimize the area overhead. As regards the TxD communication unit architecture and the voltage limiter, the separation between the two frequency bands was done with a small transistor overhead. For the RxD path two separated demodulators were designed for HF and UHF. As these module areas are small, the disadvantage in the total chip area is negligible.

2.3.1 EPC standards

As already mentioned, the following air interface protocol standards are used during the CTS project:

- EPCglobal HF Version 2, Draft Version 0.3 [EPC07b] (pre-release)

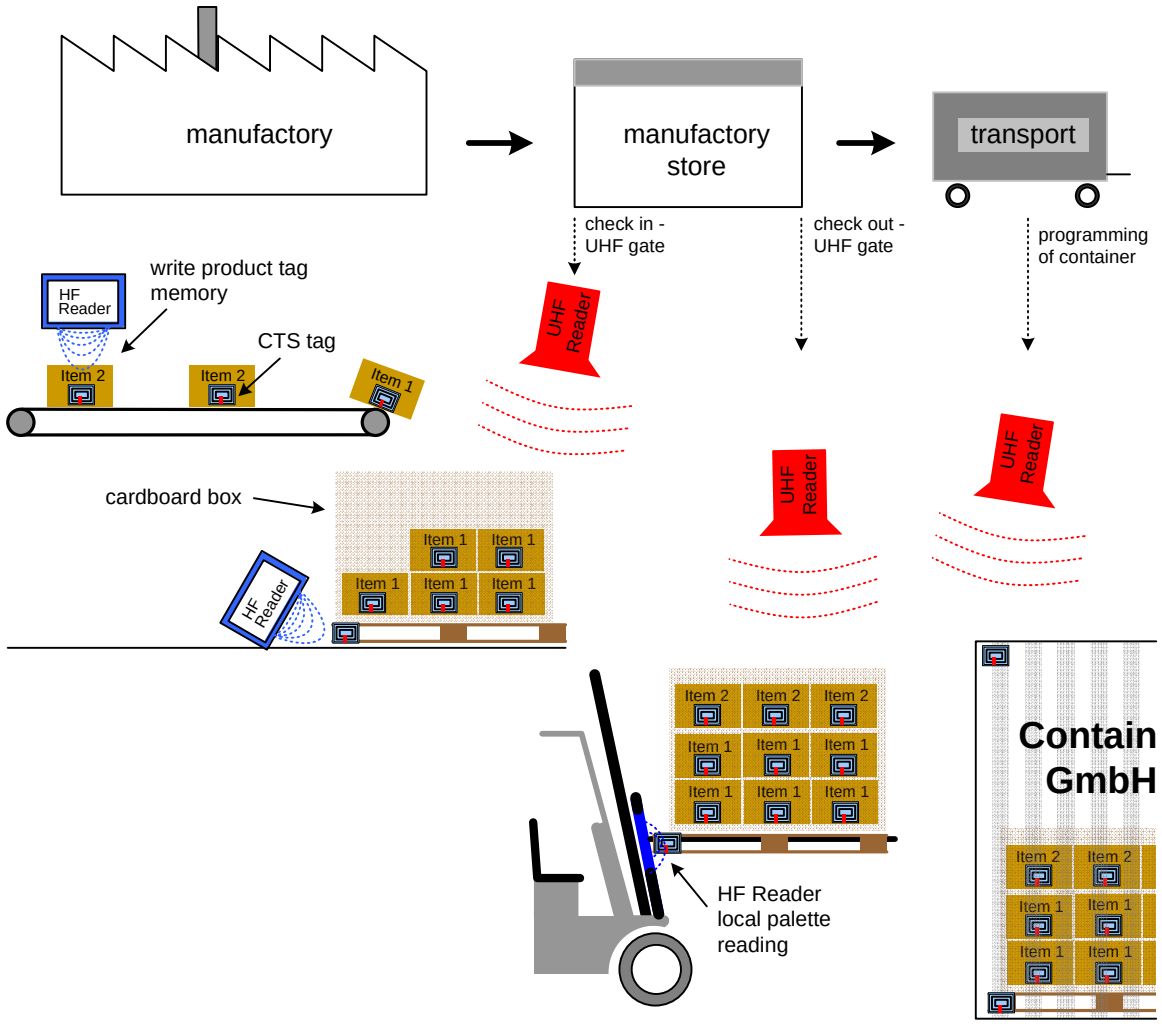


Figure 2.2: CTS tags are fixed on label products, pallets and container

- EPCglobal UHF Class 1 Generation 2 [EPC07a]

The final HF Generation 2 tag protocol standard is still pending. In each of the following chapters there are some EPCglobal standard numbers listed which are necessary to specify the features of the local oscillator, modulator and demodulators. There is no introduction or summary of the EPCglobal standards in this thesis but it can be downloaded from the EPCglobal homepage - www.epcglobalinc.org

2.4 Air interface parameters

The wavelength λ for a given frequency f can be written as [Fin06]:

$$\lambda = \frac{c}{f} \tag{2.1}$$

$c \approx 300.000 km/s$ is the velocity of light. The wavelength for UHF (868MHz) is about 34cm and for HF (13.56MHz) about 22.1m.

Damping factor:
In general, the magnetic or electric field damping in free space can be separated into two regions: The near-field region with a damping factor of -60dB/dec and the far-field region with a damping factor of -20dB/dec. In between, an intermediate zone - the Fresnel zone - smoothens the intersection between far and near field. In HF after a constant magnetic field strength region, the field drops by $1/r^3$. This is equivalent to -60dB/dec. For small HF antennas, the near field region ends at a distance r away from the antenna:

$$r = \frac{\lambda}{2 \cdot \Pi} \tag{2.2}$$

´ For HF conditions, this border is at about 3,5 m. At farther distances, the magnetic field strength decreases less rapidly and finally reaches a slope of -20dB/dec in the far field. Is the transponder in this far-field region, the residual field strength is far below the chip sensitivity [Kla09] [Fin06]. Thus, a passive HF RFID transponder will only operate properly in the near-field region.

For 868MHz UHF, the calculated near-field border is at about 5,4 cm. When the transponder is moved away from the reader antenna, it passes an intermediate zone, the radiating near field or $Fresnel\ region$. Equation 2.3 describes the end of the intermediate zone.

$$r > \frac{2 \cdot D^2}{\lambda} \tag{2.3}$$

D is the largest dimension of the reader antenna [m]. Farther away from the reader antenna the far field starts [Hol07] [Sto07]. This far-field region is also the normal operation distance for a UHF transponder. The damping is only -20dB/dec and guarantees operation distances up to 10 meters. Precondition is a low-power consumption of the chip and a reader which operates at its maximum allowed power level as shown in figure 4.2.

2.4.1 Power Matching

Maximum power from the source to the load is transfered when power matching is fulfilled. The source impedance has to be conjugate-complex compared to the load impedance.

$$Z_{source} = Z^*_{load} \tag{2.4}$$

Especially in the UHF RFID band, a careful impedance matching is necessary for optimum performance. Radiation resistance and resistive conductor losses on the antenna system have to match with the non-linear chip input resistance. The resulting antenna inductance has to be matched with the non-linear chip input capacitance.
Another term for the impedance matching is the reflection coefficient value ρ or the S-parameter S11 value.

$$S_{11} = \frac{Z_{load} - Z^*_{source}}{Z_{load} - Z_{source}} \tag{2.5}$$

$$S_{11} = \sqrt{\frac{P_{reflected}}{P_{incoming}}} \tag{2.6}$$

In equation 2.6, the transferred power to the load is marked as $P_{incoming}$ and the hopefully small reflected power amount at the input of the load is called $P_{reflected}$.
In real UHF RFID applications, the right matching will only be possible at a dedicated incoming power level close to the minimum power required to start the chip. Reason for this is the non-linear capacitance of the input stage which is formed by the semiconductor rectifier and the power generation circuits. Moreover, the chip resistance is non-linear and will therefore also cause a reduction of the performance of the tag. With a serial chip resistor value of 15Ω and even lower, the compatibility to the common 50Ω system is not valid anymore. This increases the measurement efforts when the antenna or chip has to be characterized.

2.4.2 Quality Factor - Q

Beside the resonance frequency f_{res}, the quality factor Q is the second characteristic number which describes a parallel or serial LRC resonance circuit [CR64]. Finally, after some simplifications the antenna to IC interface is similar to a parallel resonator as shown in figure 2.3. A very

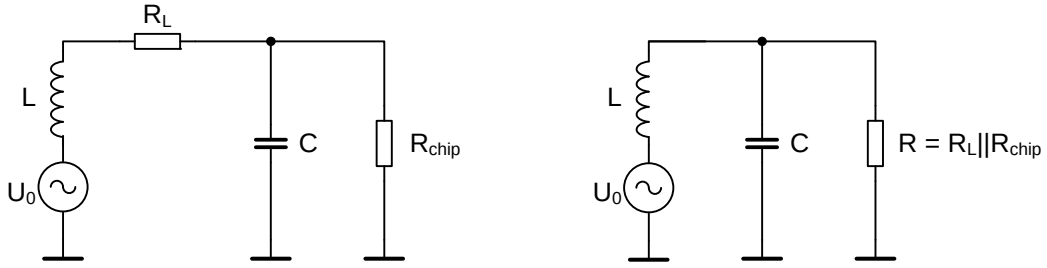


Figure 2.3: Parallel RLC tank circuit

general description of the quality factor on power levels is presented in equation 2.7.

$$Q = \omega \cdot \frac{energy\ stored}{average\ power\ dissipated} \quad [\text{Lee04}] \tag{2.7}$$

Energy stored in a capacitor is handed over to an inductance once a period and is stored there for half a period. A part of this energy is dissipated during each cycle in the resistor R. This alternating current has to be considered when the on-chip metal wire width is calculated in order to avoid electro-migration problems when the current density gets too high. As the peak energy stored in the capacitor is the same as in the inductor, only one energy reservoir is considered in the following equations:

$$E_{blind} = \frac{C \cdot U^2}{2} = \frac{C \cdot (I_{pk}R)^2}{2} \tag{2.8}$$

$$P_{dissipated} = \frac{I_{pk}^2 \cdot R}{2} \tag{2.9}$$

Taking both formulas in relation, the maximum peak current I_{pk} can be extracted and only the component values of the LRC tank are in the final equation.

$$Q = \omega_0 \cdot \frac{E_{blind}}{P_{absorbed}} = \frac{R}{\sqrt{L/C}} = \frac{R}{\omega_0 \cdot L} = \omega_0 \cdot C \cdot R \tag{2.10}$$

This equation is valid for all frequencies and, therefore, valid for all passive RFID frequency bands.
Finally, the bandwidth of the resonance circuit is considered:

$$BW = \frac{\omega}{Q} \tag{2.11}$$

One definition of the bandwidth of a resonant circuit is shown in equation 2.11. The bandwidth B is inversely proportional to the quality factor Q. Higher data rates during communication cause a larger frequency gap between sideband and carrier. Damping of these sidebands is avoided when the Q factor is reduced. From the technical point of view, the reduction of the Q factor is not a problem, but with the smaller voltage multiplication the maximum operation distance will be reduced too. As already mentioned, all equations are valid only for sinusoidal signal wave forms. As passive RFID is supplied with big amplitude wave forms and the attached components like switches, diodes or transistor regulators are not linear, it is obvious that the weak input signal is not a sinusoidal wave form anymore and this reduces the accuracy of previously mentioned equations.

2.5 Air Interface Circuits

HF or UHF air interface circuits are similar to resonance circuits. Antenna and chip are represented with only two components. In figure 2.4 the source symbol represents the induced coil voltage or the received power delivered from the attached antenna. The mathematical conversion from magnetic field strength to an induced voltage and vice versa can be taken from [Fin06]. This simple air interface could be extended with parasitic or non-linear components to get a model

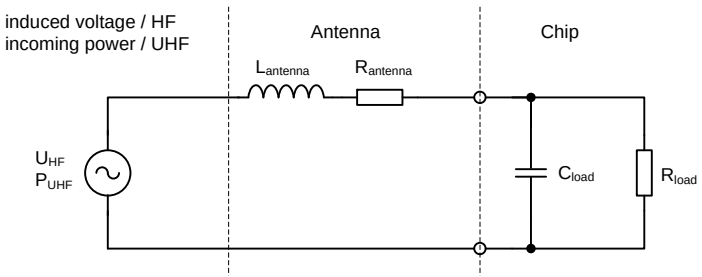


Figure 2.4: Equivalent tag electrical circuit

that is closer to the real application. Difficult to estimate are 3 dimensional resistive Si-substrate losses [KN99] and also DC voltage dependent junction-capacitors form active diffusions to the substrate. Special software tools used for spiral on-chip inductors will help to get an estimation of these substrate losses.

2.6 How to combine different frequency bands?

As the number of chip pads on the CTS chip is limited to two and the form factor of the antenna is limited to a credit card format, the separation of both frequency bands with two analog interfaces for two antennas is not possible. One antenna which is selective at both frequency bands is attached to both balanced chip interface pads. Only one analog chip interface - especially one rectifier - is necessary to be compliant with the CTS interface definition. The challenge with taking only one antenna is getting two separated high quality factors - one at the HF and one at the UHF frequency band.

3 Infineon Si process information

Next, a brief description of the used Infineon 120nm process will be given. All values are typical and do not include process variations (fast/slow) or temperature aspects.

3.1 MOS transistors - electrical parameters

Thin oxide transistors are used for digital and analog modules. They withstand a permanent power supply voltage of 1.5V (considering the short RFID product lifetime). The process option NVM memory (EEPROM) also delivers transistors with an increased oxide thickness - so called thick oxide transistors. These transistors can withstand a permanent voltage stress of 7V.

transistor type	V_{th_typ}	L_{min}	R_{poly-}/square
Thin oxide N/PMOS	350mV	120nm	5Ω
Thick oxide N/PMOS	600mV	1000nm	200Ω

To be compliant with commercial HF RFID products, a coil voltage of 4V is necessary. Only the thick oxide transistor withstands the electrical field and have to be used close to the HF-coil/UHF-antenna.

However, thick oxide transistors have disadvantages at high frequencies:

The specific resistor of the thick oxide gate-poly is 40 times higher than that of the thin oxide transistor. It causes a delay in transistor switching and a reduction in the overall quality factor Q of the IC.
According to formula 3.1, maximum speed is reduced inversely proportionally to L^2. Moreover, at each power level applied to the antenna, the overdrive voltage $V_{GS} - V_T$ is always smaller than thin oxide transistors [San08].

$$f_T = \frac{g_m}{2\pi C_{GS}} = \frac{3\mu}{4\pi L^2}(V_{GS} - V_T) \tag{3.1}$$

$$f_T \approx= \frac{v_{sat}}{2\pi L} \tag{3.2}$$

When one observes the disadvantages of thick oxide transistors, it becomes quite clear that in the long run, a performance loss in UHF operation will be the consequence compared to thin oxide transistors or Schottky diodes.

3.2 MOS transistors - Symbols

Especially at the interface antenna to chip, several thick oxide transistors are used. For a better distinction of transistors used in the following schematics, the symbols can be seen in figure 3.1 and 3.2. The typical threshold voltage of a NMOS thick oxide transistor is $\approx 0.65V$. The comple-

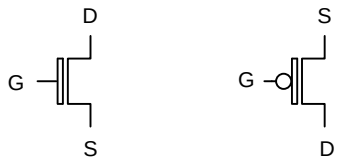


Figure 3.1: Symbol of thick oxide NMOS transistor (left) and PMOS transistor (right)

mentary PMOS transistor has a slightly higher threshold voltage of $\approx -0.70V$. The gate length of N/PMOS transistors is limited to a minimum of 1µm.

Thin gate oxide transistors are also called "'low voltage"' transistors and are used in analog and digital designs. The oxide withstands a permanent stress level of 1.5V. The typical threshold

Figure 3.2: Symbol of thin oxide NMOS and PMOS transistor

voltage for a NMOS or PMOS thin oxide transistor is $\approx \pm 0.4V$. Minimum gate length is 120nm. Because of the drastically improved performance of thin oxide transistors compared to thick oxide ones, each application of a high-Vth transistor is carefully considered during the design phase of the project. Naturally, these transistors are inserted only when absolutely necessary.

3.3 Passive components

Integrated passive components like resistors and capacitors change their values according to the applied voltage, silicon temperature and process parameter variations [Bak07].

Capacitors
Because of the second poly gate (the floating gate) in the EEPROM process technology, linear poly to poly capacitors are available. Their capacitance is independent of the applied voltage on either of the two poly plates. The area capacitance with $\approx 2fF/\mu m^2$ is clearly smaller than a thin oxide transistor capacitance but it withstands up to 15V constant voltage stress. Therefore, it can also be used as resonance capacitor at the coil input pads. The parasitic capacitor from the lower poly plate down to the lossy substrate is $\approx 8\%$ of the nominal poly to poly capacitance. Especially in RF applications these parasitic losses may increase the equivalent serial resistance of the chip which will finally result in a reduced power performance in the UHF frequency band [BVR$^+$09], [KF03]. A MIM capacitor with a much lower parasitic capacitance against the substrate is not available in this technology process. Metal to metal capacitors without special isolation are feasible but as there are no dedicated Infineon simulation models available for them, they are not used in the following designs.

Resistors
To minimize the resistor area, the analog design has been carried out with only a small number of poly resistors. Wherever possible, resistors have been replaced in the CTS design by transistors. A specific sheet resistance of $\approx 300\Omega/square$ and a voltage independent resistor value are the crucial factors for using a poly resistor. Temperature dependency can be compensated when n-poly and p-poly resistors are combined in the right ratio together to one resistor with temperature stable resistor value.

4 Power Generation Units

Coupling between reader and transponder relies on magnetic field (inductive coupling), electric field (capacitive coupling) or radiation field (electromagnetic coupling) [Pur08]. Inductive and capacitive coupling are usually near-field powering methods with an operation distance which is proportional to the reader antenna size. At UHF frequencies, the far-field coupling is applicable and is a guarantor for a big operating distance over several meters.

4.1 Passive RFID power generation

Any RFID ISM band reader generates a magnetic or electric field into the near-field region and radiates an electromagnetic wave into the far field. The CTS transponder power generation unit receives and converts the incoming power into a stable internal DC power supply. In figure 4.1, only one antenna is gathering energy form the field and transfers the power to the attached rectifier. New CTS design concepts for the AC/DC and DC/DC converter are necessary to fulfill the selective circumstances of each frequency band. These concepts are described in the following. The most crucial characteristic of the CTS AC/DC converter is its high efficiency in each of the

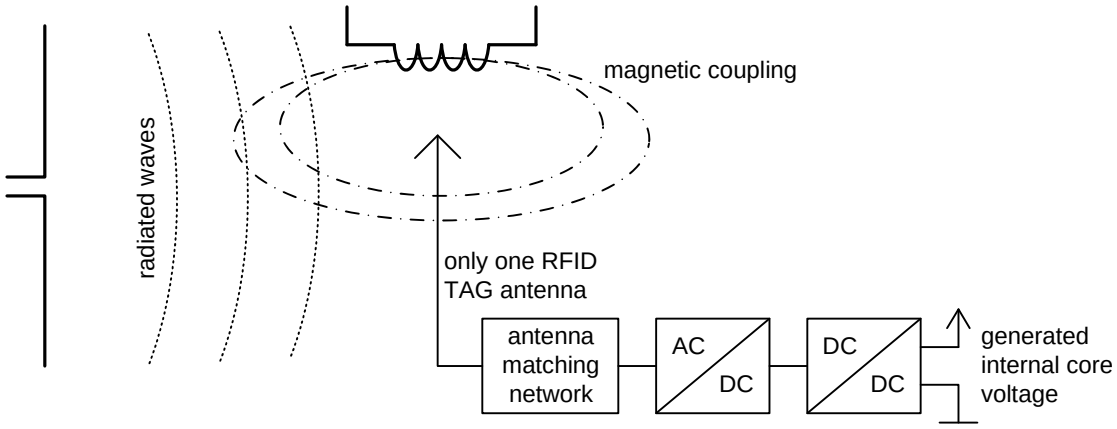


Figure 4.1: Power generation modules - An architectural overview

two frequency bands. The diction ”highly efficient” comprises the following key aspects:

- best chip impedance to antenna impedance matching in the HF and especially in the UHF band
- the right voltage potential at the antenna-chip interface

- high rectifier and DC/DC converter efficiency
- damping of internal chip noise to avoid wrong backscatter information to the reader

In the HF near-field operation, the amplitude of the rectifier rises to 4Vpeak already at a weak field strength. The low drop rectifier generates an output voltage of about 3.6V, which is much too high to be used as internal power supply voltage. For a voltage level reduction the first DC/DC converter is necessary. In the far-field, the voltage at the rectifier input rises more slowly compared to HF. To get a stable internal power supply voltage, an up-converter has to be used. This is the second DC/DC converter.
The contactless power and data performance, silicon chip area and the developed chip technology complexity have to be competitive with typical HF/UHF band products, which are already established in the market. For example, no on-chip energy reservoir capacitor for energy harvesting is allowed to increase the UHF operating range. A drawback of these cost-saving measures, however, is the reduced chip sensitivity in the UHF mode.

4.2 Available power in different RFID frequency bands

Power levels at the corresponding ISM frequency bands are shown in figure 4.2. Reasons to choose and to invest into the right frequency band are:

- local RF regulations and limitations in each country
- already used reader infrastructure
- necessary operation distance of the transponder
- maximum data rate
- transponder costs

The intent of the CTS power generation unit is to be able to handle every applied RFID frequency form the LF band up to the 2.45GHz UHF band. The power generation unit also has to handle the wide dynamic range of incoming power levels delivered to the rectifier. Frequency selection with the help of a tunable on-chip matching circuit is not supported. This kind of matching would increase the chip area significantly and would reduce the quality factor Q of the transponder circuit especially at lower frequencies. Impedance matching is performed by special measures in the antenna design an not by the chip input structure.

To get a cost competitive transponder for transport and identification, the CTS chip - antenna prototype supports the EPCglobal HF and UHF standard. The power generation design concept would be able to handle also the LF and 2.45GHz ISM band, but for proper operation first, an additional capacitance and second, a more powerful transistor for the rectifier would be necessary. Some key parameters will help to specify and describe the CTS power unit.

- Rectifier frequency range = 100kHz . . . 2.45GHz
- $V_{coil\ max\ HF} = 5V_{peak}$

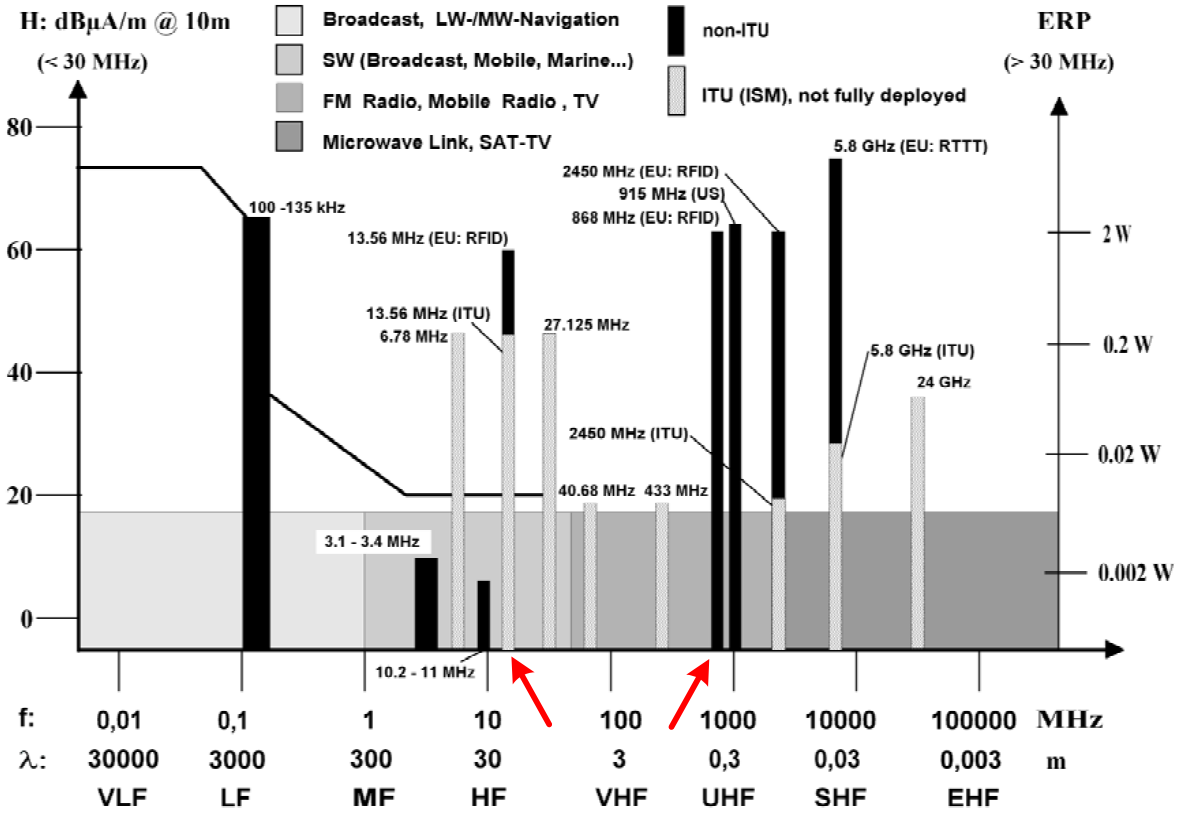


Figure 4.2: RFID frequencies and corresponding maximum power levels [Fin06]

- $V_{antenna\ min\ UHF} = 0.8V_{peak}$
- Power path efficiency HF $>$ 80%
- Power path efficiency UHF $>$ 15%
- I_{load} at VDD = 10µA ... 20µA
- some Si technology restrictions

Frequency range

125kHz or 134kHz carrier frequencies are applied to the rectifier when the LF (low frequency) band is chosen. Energy could be derived by use of this CTS rectifier and communication done via the HF demodulator and load modulator. In this mode, additional internal energy reservoir capacitors and external resonance capacitors are necessary. From the digital point of view the CTS chip has to support the typical LF coding like ISO11785 or ISO14223. From the application point of view, the analog and digital area overhead for a LF band system cannot be supported. A reliable reduced operation distance is already given in the HF band. During the feasibility study the CTS team decided to optimize the chip architecture for the HF and UHF frequency band.
In the upper UHF band, close to the MWF (micro wave frequency) band, the popular 2.45GHz band is approved for RFID but it is used rarely for passive RFID applications. The biggest benefit

of using this band is the smaller antenna size compared to a 900MHz antenna. The maximum operation distance is reduced to about 1m, which is much less than in the UHF band. Moreover, for this MWF frequency band, we did not see the determined advantage of being implemented in the CTS chip.

Antenna voltage limits
An antenna voltage dynamic range from 0.8V up to 5V peak is necessary to be compliant to corresponding HF and UHF regulations and performance requirements. This high carrier peak voltage of 5V at the coil is necessary, because HF load modulation requires a certain voltage peak potential dynamic of about $3V_{peak}$ [ISO08] [ISO06] during the switching. The peak voltage value during the load modulation phase is limited to about 500mV or even close to zero when an on-chip PLL is used. To fulfill the ISO sideband requirements, the peak voltage in the normal phase (during non-modulation phase) has to be above $4V_{peak}$ or when the inverse load modulation concept is used, the peak voltage during the load modulation has to reach the aspired $4V_{peak}$. [Kla09] [Ber03].
The lower voltage limit of $0.8V_{peak}$ in the UHF band is not a number which is defined in the EPC specification; it is simply a CTS rectifier performance limitation. The lower the antenna voltage can be without losing rectifier or charge pump efficiency, the better the maximal operation distance of the tag will finally be. By use of Schottky diodes instead of thick oxide MOS transistors the level of 0.8V could be reduced even to $V_{AC\_coil1/2} = 0.5V_{peak}$ and the efficiency would increase up to 35% [KF03].

Power path efficiency
During the design phase the digital current consumption was not exactly known. An overall load current bandwidth from 5µA up to 15µA for the digital modules was estimated. The rectifier has to deliver this current in all frequency bands with an arguable power efficiency of 80% in HF operation and 15% in the UHF band.

Technology restrictions
In the coarse CTS power path specification, the last item regards the Infineon technology limitation. Schottky diodes are powerful in every sense and perfect for RF charge pumps: are characterized by a small forward voltage and an exponential U/I sensitivity. So far they have been used in all commercial high performance UHF RFID front ends. The diode area with the corresponding junction capacitance is small compared to MOS transistors.
In a modern CMOS process, thin oxide MOS transistors have a threshold voltage V_{th} of about 400mV. Even special zero threshold transistors with a high leakage current will never reach the performance of Schottky diodes. To handle the voltage range at the antenna to chip interface, special high voltage devices with increased oxide thickness are used in the analog front end. This type of transistor is characterized by a threshold voltage of about 600mV. The minimum channel length is increased from 120nm to 1µm and the drain/source p/n diffusion areas are significantly increased compared to thin oxide transistors.

4.3 Balanced and unbalanced rectifier structures

In RF systems we have to distinguish between balanced (symmetrical) and unbalanced (asymmetrical or single ended) systems. For permanent operation or for system tests, balanced or unbalanced RFID antennas are connected to balanced or unbalanced RFID chip frontends. When these two systems are linked together, special measures are necessary. The same problem will occur when unbalanced measurement equipment is connected to balanced chip interfaces. In

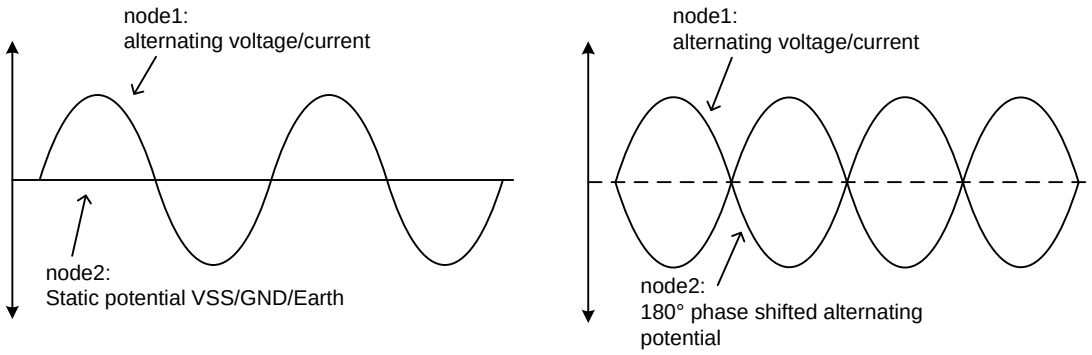


Figure 4.3: Is there an unbalanced signal applied, we only have one ”hot” node - in balanced configuration two

figure 4.3, the balanced and unbalanced types of control signals are shown. In the contactless air interface, a sinusoidal waveform is delivered in all frequency bands from the reader antenna in the form of an electromagnetic field. Half- and full-wave rectifiers in combination with a storage capacitor are the common architecture to convert sinusoidal input voltages into a DC output potential. Typically, the full-wave concept is more efficient, because the negative half-wave is mirrored to a positive half-wave and the corresponding charge frequency is doubled. This full-wave performance advantage is clearly valid at low frequencies like 13.56Mhz and at moderate or high current consumption of the chip when several mA are consumed by the internal load. At frequencies located in the UHF band and at low or moderate current consumption, integrated AC - coupling capacitors can be used as level shifter which allow a DC level shift and an increased rectifier efficiency. Figure 4.4 shows the antenna to chip interface of an unbalanced AC/DC con-

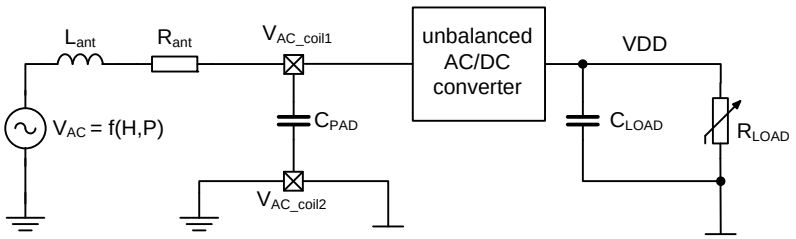


Figure 4.4: A typical UHF RFID antenna - chip interface

verter. Typically UHF RFID products especially use this approach for 2 or 3 stage charge pumps

[See05] [SHCW06] [KF03] and [GBC$^+$04]. In the unbalanced AC/DC converter, DC-blocking capacitors in front of the rectifier shift the sinusoidal voltage to an individually higher potential. The corresponding peak-to-peak voltage at the passive capacitor plate is about 10% or even 20% lower than the peak-to-peak voltage at the active antenna plate which is directley connected to the transponder antenna.
One advantage of an unbalanced input stage is the connection of one antenna branch to the internal chip VSS via one pad. From the chip's perspective, the VSS pad will notice no dynamic voltage oscillation and all parasitic capacitive or parasitic inductive influences can be neglected at this node. This parasitic simplification is a very big benefit for the floorplan and layout of unbalanced chips. The distance between the RF and VSS pad can be increased on the chip as far as necessary. A minimum antenna-pad distance for proper backend assembly is necessary and usually is longer than $500\mu m$. A limited number of 100 squares are necessary to transport the big alternating current during HF high-field strength operation (electromigration) and to get a high Q-factor in weak field-strength conditions (low resistive input structure). UHF rectifier and charge pumps are typically concentrated very closely around the RF pad to achieve best performance. The VSS pad is connected well to the local chip substrate. A balanced input structure is

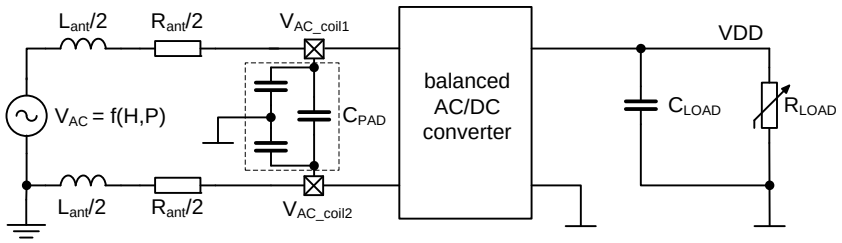


Figure 4.5: A typical HF RFID antenna - chip interface which is also used for the CTS chip

shown in figure 4.5. Two cross-coupled switches (see figure 4.11) define the chip VSS potential and, therefore, also the two coil potentials $V_{AC\_coil1/2}$. Because of these switches, the potential at $V_{AC\_coil1/2}$ is always above -200mV compared to the internal power supply potential VSS. Thus, coupling capacitors are not necessary any more to avoid negative voltages and triggered PN junctions. This architecture is perfect for LF and HF bands, but it has some drawbacks for higher frequencies. With some innovations, this concept of a balanced input structure will be used in the CTS project.
Another balanced rectifier structure is the so-called Greinacher cell, which delivers a positive and a negative power supply potential. An isolated silicon process (e.g. SOI) is necessary to benefit from such an input structure [ASI09] and [CDDJ07].

4.4 Proposed CTS power architecture

Before starting with the detailed rectifier implementation on transistor level, the architecture of the CTS power supply unit will be presented and compared with typical passive RFID implementations. Generating a local IC power supply is the target of the CTS power architecture. This defines a local VSS and a positive voltage potential big enough to operate the on-chip digital state machine reliable. On the left of figure 4.6, a HF rectifier with an attached DC/DC converter

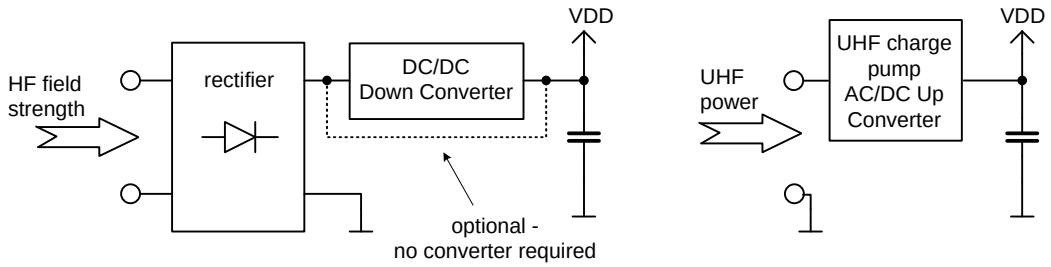


Figure 4.6: Typical power generation in the HF and UHF frequency bands

is shown. The detailed schematic implementation of the rectifier is presented in the next sections. As already mentioned, HF load modulation sideband requirements result in an increased coil voltage, which simply is too big for a rectification without DC/DC down converter when a sub quarter-micron gate oxide transistor technology is used. In this case, the DC/DC down converter implemented as linear serial regulator is necessary for a stable and reliable VDD potential of about 1.4V.
Commercial UHF frequency band products are done with an unbalanced input structure. This charge pump operates with 868MHz or 915MHz and tries to increase the small antenna voltage at weak incoming power conditions to reach a usual core VDD power supply potential. This charge pump also takes over the rectification of the incoming RF amplitude. A big antenna voltage of several volt is not necessary for UHF. The HF step down converter, therefore, is not necessary either. One reason for the relaxed dynamic is the increased backscatter sensitivity of a UHF reader [NR06a]. Is the voltage amplitude bigger than specified in the previous table, the excessive power will be converted into temperature by a local shunt which is located parallel to the antenna.

A combination of HF and UHF power architecture is the basis of the CTS concept in figure 4.7. A special low-drop voltage rectifier which can work down to a coil peak voltage of 0.7V is the common interface for both frequency bands. The simple voltage rectifier with a dynamic peak

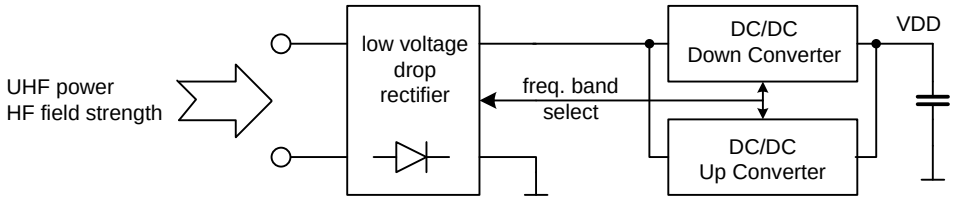


Figure 4.7: Proposed CTS architecture to handle HF and UHF bands

voltage range from 4.5V down to 0.55V would vary too much to be used as a core power supply voltage. The afterwards attached DC/DC up/down converter will do the task of ”regulating” VDD to the right voltage value. Down-conversion is done with a linear voltage regulator which is characterized by a good PSRR. For up-conversion, the local oscillator delivers a low-frequency

clock of about 2MHz to a highly efficient one stage charge pump. With the help of these two core modules, a stable local VDD power supply voltage value of 1.5V is guaranteed in all frequency bands.

4.4.1 HF rectifier

Why not integrate an unbalanced HF rectifier? High coil voltages at the chip interface are necessary to power the IC and to fulfill requirements which are defined in the ISO15693 or ISO14443. An alternating voltage oscillating symmetrically around VSS is chosen as the input voltage. Because of a constant impedance represented by a resistor, the coil voltage $U_{resistor}$ in figure 4.8 is proportional to the magnetic field strength. In a self-isolation CMOS process without triple well

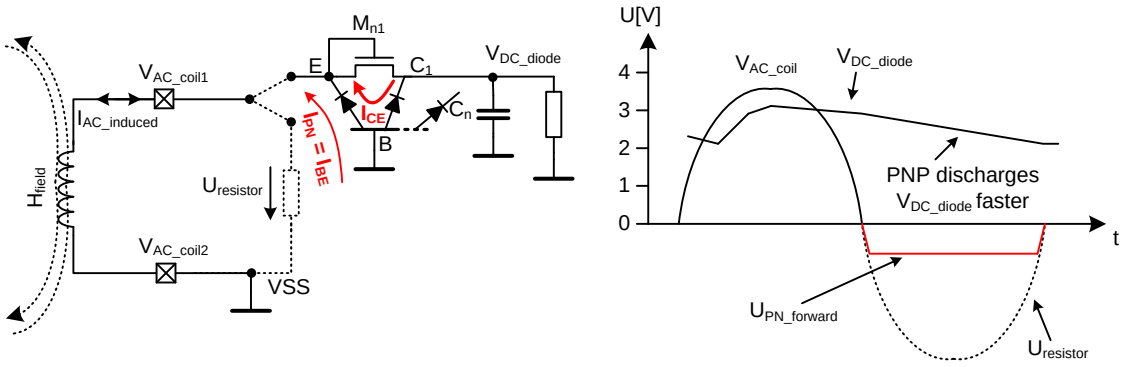


Figure 4.8: First, a resistor only and then, additionally a rectifier is connected to an inductance

option, a more negative voltage than -600mV triggers a PN-diode in forward operating mode. A junction diode from substrate to this node operates in forward direction and a big current clamps the voltage accurate defined around -0.7V versus VSS. Not only the clamping of the voltage is the problem here; the parasitic bipolar transistor in figure 4.8 is also triggered by this conductive PN-diode. It represents the base-emitter diode of a bipolar transistor. If this diode conducts, the collector node can be any PN diode which operates in backward direction and the current is limited only by the substrate resistance and special technology measures. If a sensitive node is affected by this NPN transistor, malfunction of a module in the analog front end at high-field strength can be the consequence.

An AC-coupling capacitor in front of each PN diode provides a DC voltage shift at node V_{AC_coil1}, but the additional parasitics rapidly increase the overall input capacitance between the two antenna nodes. If a poly-poly capacitor is chosen, an additional capacitance to substrate of 10% of the nominal value is the consequence and pushes the resonance capacitance value at the rectifier input far above the typical value of 15pF. Additional capacitance results from metal wiring capacitances to connect the big AC-coupling capacitor area.
Especially in the UHF frequency band, a bigger input capacitance causes a linear reduction of the rectifier input voltage. The antenna voltage generated by the incoming electromagnetic wave is amplified by a smaller voltage multiplication factor [Dob07]. Typical values for UHF only TAG input capacitance are 0.2pF - 0.5pF. The input resonance capacitance of the CTS chip is about

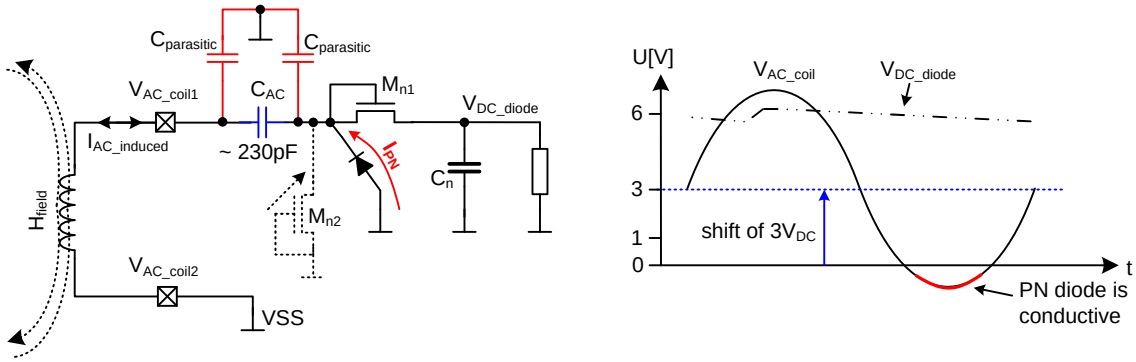


Figure 4.9: Simple rectifier with additional big AC-coupling capacitor

600fF. Figure 4.10 and equation 4.1 show the influence of the chip capacitors on the input voltage

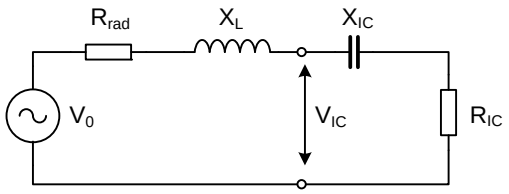


Figure 4.10: Simplified antenna to chip interface

V_{IC}. Precondition of the equation is a perfect power matching and a significantly smaller serial resistor R_{IC} compared to X_{IC} and X_L.

$$\frac{V_{IC}}{V_0} = \frac{R_{IC} + X_{IC}}{2 \cdot R_{IC}} \approx \frac{X_{IC}}{2 \cdot R_{IC}} \tag{4.1}$$

To avoid negative voltages at the input of the IC, figure 4.11 shows two cross-coupled NMOS transistors defining the VSS potential in both designs. On the left side of figure 4.11, a standard HF rectifier is shown with two diodes to power the resistive load and to supply an energy reservoir capacitor. Both are attached to a single node V_{DC}. A voltage requirement of about $5V_{peak}$ at the coil requires NMOS diodes with an increased voltage robustness which typically results in an increased threshold voltage. Additionally, the bulk of each transistor has to be connected to VSS to prevent backward current from the internal voltage reservoir back to the coil. This bulk connection causes an increased threshold voltage V_{th} of transistor M_{n3} and M_{n4} because of back-gate modulation [AH02].

$$i_{DS} = \frac{\mu_0 C_{OX} W}{L} \left[(v_{GS} - V_{th}) - \frac{v_{DS}}{2} \right] v_{DS}(1 + \lambda \cdot v_{DS}) \tag{4.2}$$

λ is the channel length modulation parameter $[volt^{-1}]$
μ_0 is the surface mobility of the channel of a MOS transistor
C_{OX} the capacitance per unit area

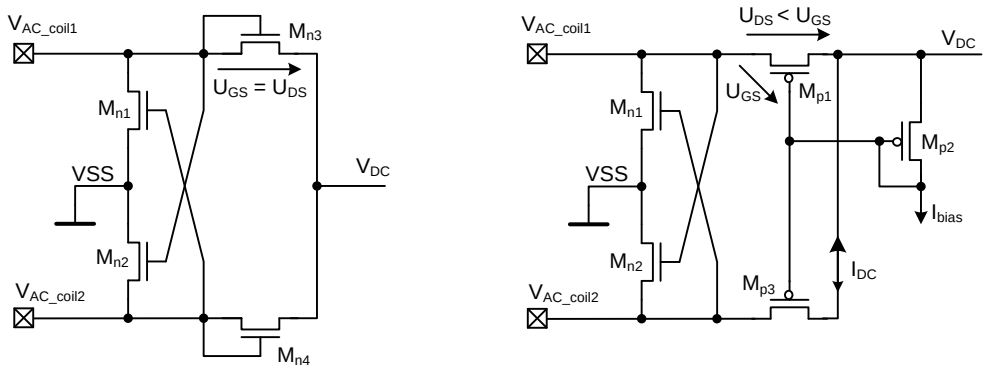


Figure 4.11: HF rectifier structures with two NMOS diodes and PMOS mirror transistors

W/L are the transistor dimensions
In a modern process it can be assumed that $\lambda \approx 0.12$. This is valid for thin oxide transistors with a transistor length which is 5 times bigger than the minimum transistor length.

Figure 4.12 shows the impact of two cross-coupled NMOS transistors on the coil voltage. At the

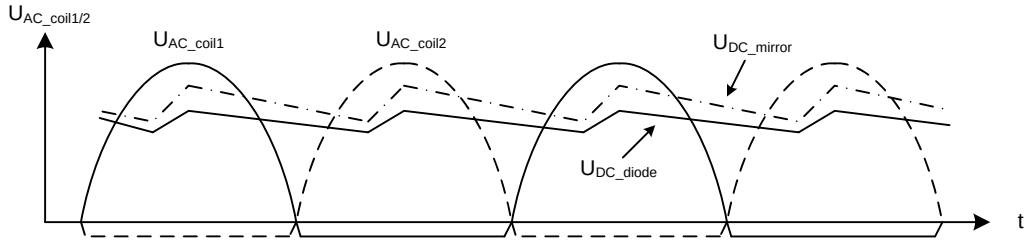


Figure 4.12: Coil voltage of both HF rectifier versions

rectifier, a pulsed waveform of 27.12MHz is generated. The two powerful cross-coupled NMOS transistors guarantee that the most negative voltage of the transistor drain does not exceed a potential of -600mV. In this case, no reverse current through any PN diode will occur.
With the help of the current mirror concept shown in figure 4.11 the voltage drop of the rectifier is reduced compared to the usual NMOS diode architecture [UY06]. A drawback of this rectifier concept is a moderate backward current from the internal power reservoir to the coil. Because of the reuse of these PMOS transistors in the UHF mode this rectifier architecture has been chosen for the CTS testchip. PMOS transistor M_{P2} generates a bias voltage for the big power transistors M_{P1} and M_{P3}. Transistor width and length of the two diodes M_{P1} and M_{P3} have to be chosen with respect to the load current and the maximum voltage drop V_{DS}. 200mV of drain to source voltage drop is acceptable for load currents below 100µA. The bias current through the transistor M_{P2} is about 20nA. For the CTS project, a modified PMOS transistor gate control circuit with active AC bias voltage coupling is necessary. This circuit is shown in figure 4.24.

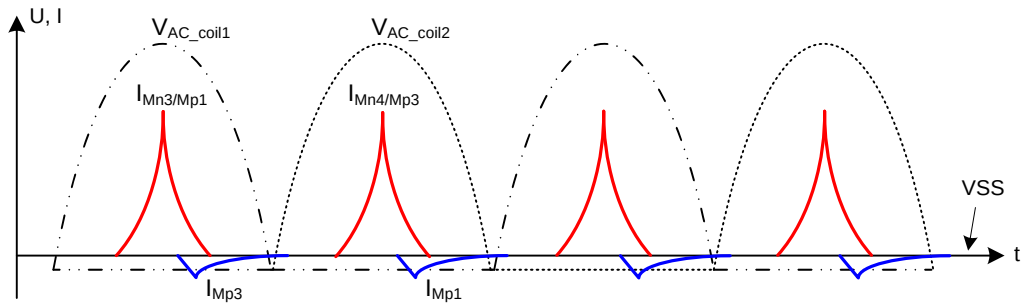


Figure 4.13: Simple rectifier with additional big AC-coupling capacitor

4.4.2 UHF rectifier

UHF guarantees a maximum passive RFID operation distance because in the far-field, the transponder already is a few cm away from the reader antenna. The incoming power at the rectifier falls below 100µW at distances of several meters. The coil peak voltage at the IC input falls below $0.6V_{peak}$ but the chip can still be powered by the contactless field. If, additionally, even a voltage drop of a Schottky diode of about 150mV has to be subtracted, 450mV V_{DC} will be the rectified DC voltage, which is too low for operating an analog or digital CMOS circuitry. If in the input stage a voltage doubler is used instead of a simple rectifier, the corresponding DC voltage can reach 2 x 450mV = 900mV, which is sufficient to operate a modern digital technology. A possible implementation of a two stage charge pump is shown in figure 4.14. If Schottky diodes are not available, CMOS transistors with minimum gate lengths could be chosen and still reach a good UHF performance. Small transistor or diode dimensions are important because each PN device area causes a junction capacitance to substrate.However, without further knowledge of the technology process applied and without any well fitted simulation tools and parameters, the substrate resistance is hard to predict, which reduces the transponder quality factor Q [BVR+09]. As already shown in figure 4.13, AC-coupling is necessary for this unbalanced charge pump for

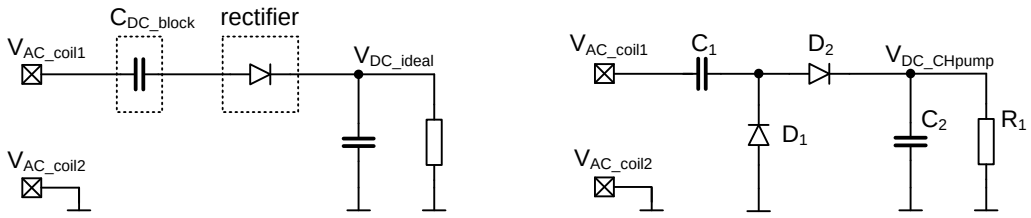


Figure 4.14: UHF rectifier principle and typical implementation

UHF frequencies which is also feasible with an internal capacitor. In C1 in figure 4.14 on the right side, C1 represents the AC-coupler device and C2 the energy reservoir for the single stage charge pump. Antenna node V_{AC_coil2} is connected directly to VSS and because of capacitor C_1 node V_{AC_coil1} can oscillate symmetrically compared to VSS. In the CTS project, this type of charge pump or rectifier is not used, as not enough power can be coupled in the HF band over the capacitor C_1.

A step closer to the CTS architecture is the rectifier concept as shown in figure 4.15, with symmetrical full wave rectifier and UHF charge pump [FB06]. Especially the initiation of a balanced rectifier, which is not common in UHF passive RFID, is the conspicuous link to the new CTS power concept. This voltage is already the base level of the final power supply voltage. As a simple amplitude rectification does not deliver a sufficient voltage potential, a 3-stage differential charge pump is added, which is powered by the UHF antenna signals. A disadvantage of this architecture is the performance limitation when MOS transistors are used. In general, the abdication of Schottky diodes reduces the power performance by approximately 3dBm - 5dBm compared to CMOS transistors of sub-quarter-micron channel length with a typical threshold voltage V_{th} of 300mV - 500mV. The reason why this concept was not taken for the CTS chip is the

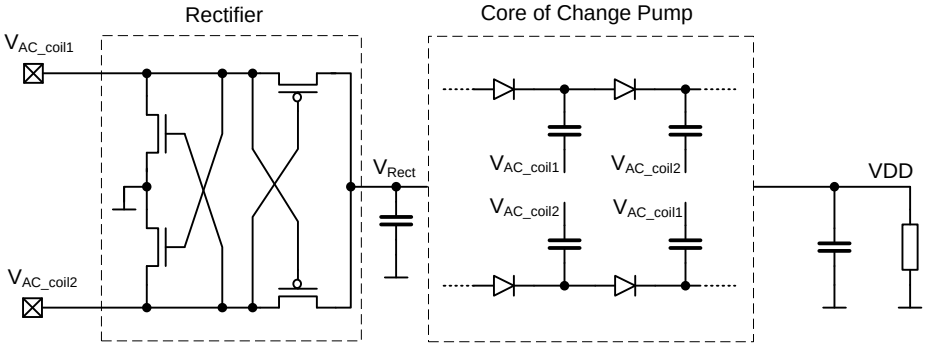


Figure 4.15: UHF rectification and additional UHF charge pump [FB06]

additional charge pump which is directly attached to the antenna pads. Charge transfer from the antenna to VDD is approximately proportional to the frequency when parasitics are neglected. If this concept is used in the HF band, too, the pump capacitors have to be increased by a factor of about 20 (same I_{VDD} load current but increased antenna/coil voltage by a factor of 4). The

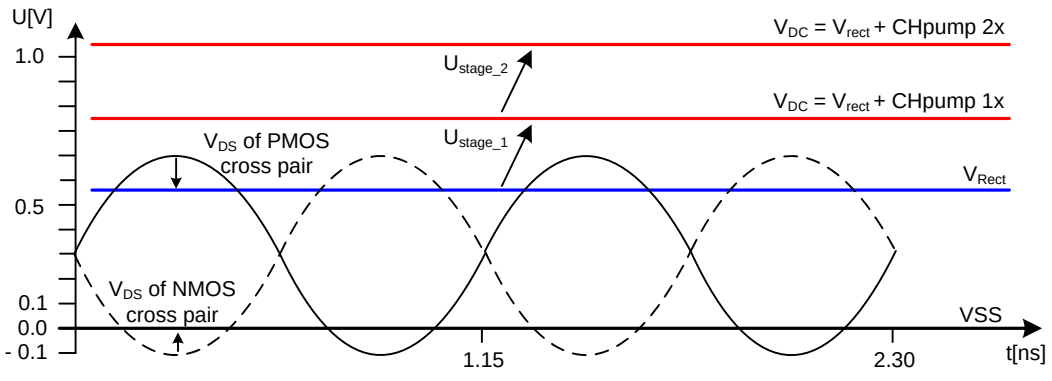


Figure 4.16: UHF rectification and additional UHF charge pump

transient timing in figure 4.16 shows the benefit of the rectifier with the additional DC offset generated by the rectifier and on top the added potential of each charge pump stage. The higher the

number of stages is in the charge pump, the lower the add on voltage of each additional pump stage will be. The reason for this is that the antenna input voltage will drop because of the bigger resonance capacitor and the reduced power efficiency.

4.5 Frequency selection

Broadband antenna designs are shown especially in the UHF RFID segment. The purpose of designing a broadband antenna is to deliver a high quality factor over the worldwide UHF frequencies with only one antenna [CWE06] [CCP05] [Dea09]. For dual band RFID antennas, some band selection versions are available [LNC07]. However, there has not been any publication dedicated to RFID yet in which the selection of several RFID bands on chip design level is described.
High-voltage swing in the HF frequency band as well as low voltage levels at low UHF power levels both require a universal rectifier which can handle both requirements. Low cost-passive RFID chips typically have only two pads for the power generation and for communication. The CTS chip also has to handle both frequencies with two pads only.
A pragmatic approach would be to place local passive components like capacitors and inductors close to the external antenna so that only corresponding frequency bands are blocked or handed over to the right modules in the analog front end. If this is possible, two well-known rectifier architectures - a HF and a UHF rectifier - can be connected together with these passive components in parallel. In figure 4.17, both inductors $L_{UHFblock}$ separate the two cross-coupled

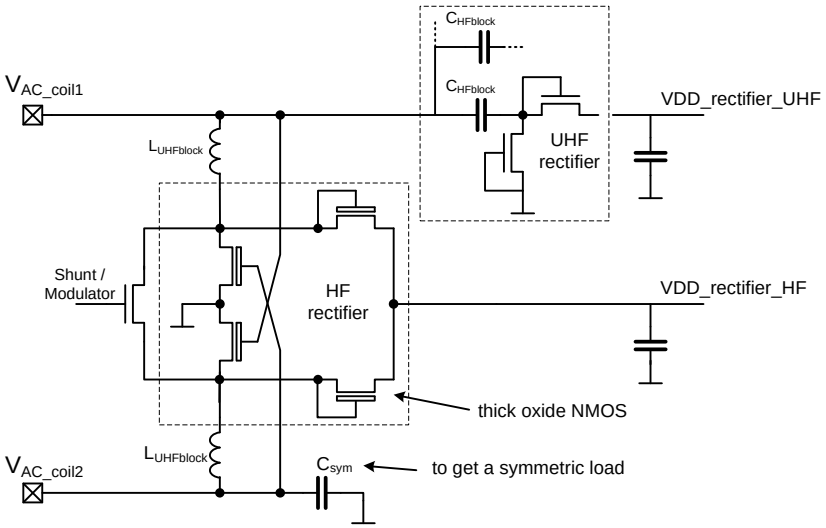


Figure 4.17: Proposal for power generation with ideal passive components

rectifier transistors which are necessary to define the local VSS when HF power is applied. Let us assume that UHF could be blocked sufficiently by two inductors with an impedance of $10k\Omega$ each. At a frequency of 868MHz an inductance of 1,8µH is necessary. According to Lee [Lee04],

the addiction between radius and inductance can be written as:

$$L = \mu_0 n^2 r \approx 1.2 \cdot 10^{-6} n^2 r \tag{4.3}$$

The question if 1,8µH could be easily implemented on silicon will be answered in the following. A simple equivalent circuit [YRL96] is shown in figure 4.18 for one inductor or even more precisely for one inductor segment. As the inductor should not be visible in the HF frequency band, the serial resistance R_s should be below 10Ω, which is equivalent to 100 squares when one single metal layer is used. In UHF and microwave frequency bands an additional serial resistance - R_{eddy} - appears. A heavily doped substrate of $20m\Omega$ per cm is able to transport currents induced by lower inductor metal wires. With distributed capacitors between the wires and substrate, these substrate currents will a Q-factor reduction of the antenna-chip interface. With the help of a 3D solver like FastHenry®, the inductance and serial resistance for an integrated inductor shape can be calculated. To do this, a good knowledge of Si process technology parameters and especially of the metal-stack is necessary. Taking liberal parameter numbers with $n = 10$ and $r = 300\mu m$,

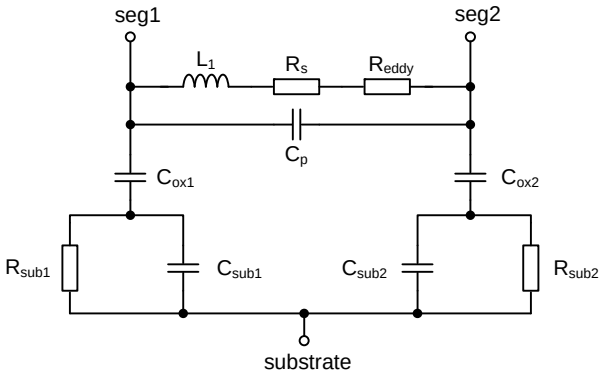


Figure 4.18: Equivalent circuit for one segment of an on-chip inductor

quite a small inductance of $36nH$ is the approximate estimation according to the equation. This value is far away from the target inductance of $1,8\mu H$, which is necessary for a good frequency separation. Furthermore, parasitic capacitors down to substrate, a high resistance because of missing low-ohmic metal layers and finally, the big area to reach the target inductance - all this is reason enough not to use passive on-chip decoupling devices for frequency separation.

4.6 CTS power architecture - An overview

In order to keep the analog power interface frequency band universal and small in area, only one power branch with mainly 4 transistors is used in the CTS rectifier. With slight modifications, this rectifier version is able to transport enough energy to the chip in any frequency band, still with - competitive performance values. As the antenna voltage in UHF and microwave frequencies get small, a charge pump driven by the internal oscillator is attached to this rectifier. Parallel to the CTS project, this new power supply concept was developed and shown by Bergeret from Ecole Polytech. Univ. de Marseille [BGP07]. The basic building blocks of the CTS power path are shown in figure 4.19. They consist of a rectifier, a low frequency DC/DC charge pump and a voltage control module. [YKMT09] and [FGB+08] also investigated into the separation of rectifier,

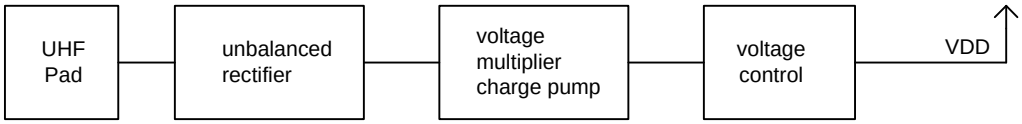


Figure 4.19: Power generation concept valid for CTS and Bergeret [BGP07]

low drop charge pump and low drop regulator. In the CTS analog front-end not only rectifier and charge pump concepts are introduced, but also secondary charge pumps and a down DC/DC converter. To get the best energy performance, a frequency-band detect module further adapts and adjusts the control circuit of these power transistors in the rectifier of the CTS power unit. Antenna aspects of a multiple selective antenna are included in the rectifier design. The architec-

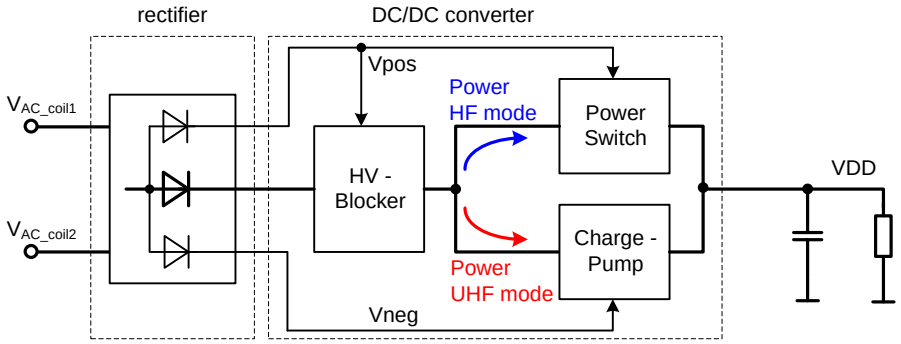


Figure 4.20: Power architecture of the CTS chip

ture in figure 4.20 shows the CTS rectifier with one main power and two secondary power paths. Behind the high voltage (HV) blocker, once a DC/DC up-converter and once a power switch is used to hand over energy to the power supply node VDD [Mis07].

A more detailed schematic of the CTS power path architecture including transistors and energy reservoir capacitors is shown in figure 4.21. In the rectifier path, the main amount of power from the alternating RF to DC is drawn by four rectifier transistors which were mentioned before - 2 PMOS and 2 NMOS transistors. Cross-coupled NMOS transistors Mn1 and Mn2 on the very

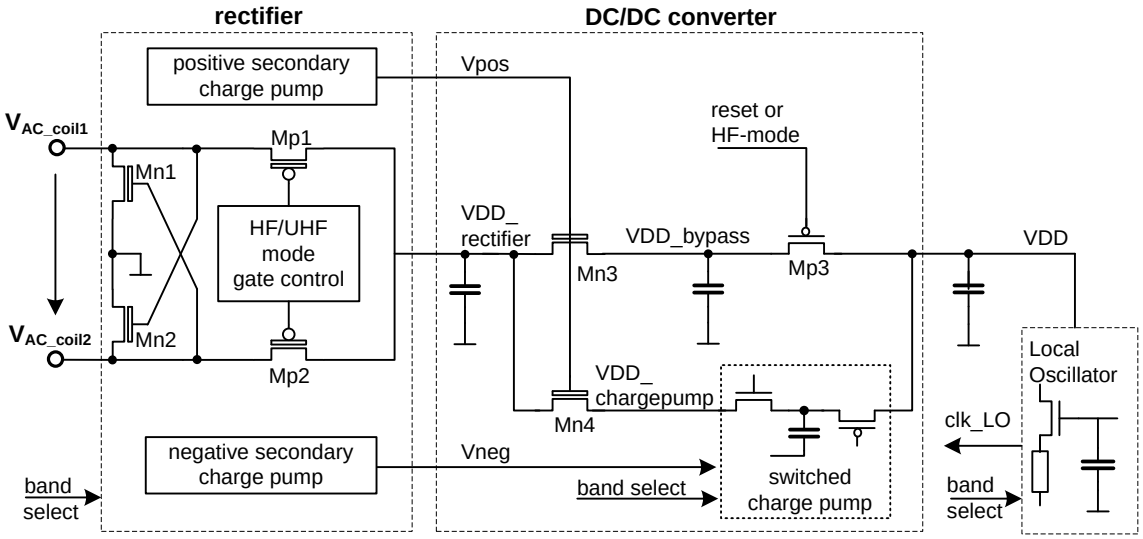


Figure 4.21: More detailed power architecture of the CTS chip

left side are active in all frequency bands. These two transistors are responsible for a balanced rectifier input structure. The two PMOS transistors are the two ”diodes” and with the help of them the rectifier is fully balanced. PMOS transistor gates are controlled individually in UHF mode and have the same DC potential in HF mode. In the rectifier two charge pumps - a positive and a negative voltage doubler - once deliver voltage potentials to the serial regulator and to the internal charge pump.

HF power path mode

In figure 4.22, some internal power path potentials are drafted for the HF application mode. In

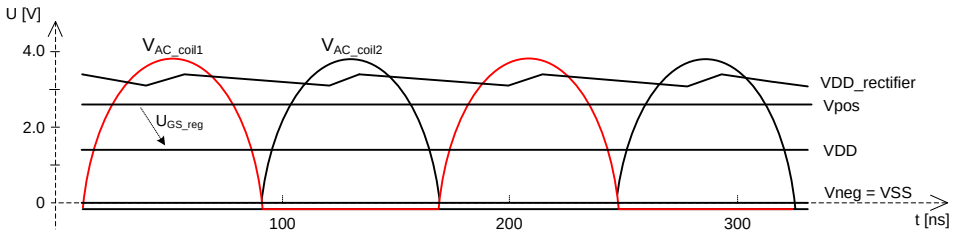


Figure 4.22: Some power relevant voltages in HF mode

this operating mode, PMOS rectifier diodes convert 4V AC_{peak} voltage applied at the coil pads to a DC_{mean} value of about 3.5V. This $VDD\_rectifier$ potential pulses at 27.12MHz and shows an alternating amplitude of several hundred mV. Serial regulator transistor Mn3 reduces this high potential of 3.5V down to about 1.45V. As VDD is the core power supply for analog and digital modules, a tight voltage tolerance and a good PSRR of the serial regulator is required. $Vpos$ is the secondary high side charge pump and controls the gate of the serial regulator. $Vneg$ is not necessary in the HF band operation. The negative secondary charge pump does not generate a negative potential in HF mode and, therefore, $Vneg$ is shorted to VSS.

UHF power path mode
If 848MHz or a higher frequency is applied to the chip, the rectifier gates are controlled by a phase shift of 180°, and both secondary charge pumps $Vpos$ and $Vneg$ are required and therefore activated. In figure 4.23, only one antenna pad voltage V_{AC_coil1} is shown. The positive AC_{peak} voltage level of 1V is a typical potential at a moderate incoming power level of -5dBm and lower. The transistors in the rectifier convert the 868MHz AC peak potential to a DC potential reduced by about 150mV which is then available at node $VDD\_rectifier$. The same

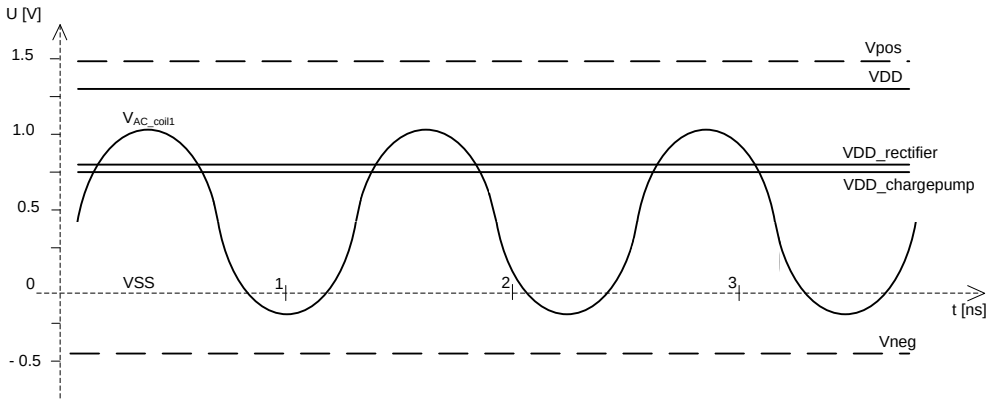


Figure 4.23: Some power relevant voltages in UHF mode

serial regulator device which is also used in the HF operation mode is necessary to shield voltages above 1.5V. Behind the serial regulator only low voltage transistors with thin oxide are used any more. This serial regulator reduces the DC voltage once again by 50mV and generates a $VDD\_chargepump$ potential of 750mV. This potential is now clearly too low and the attached voltage doubler has to increase it. As a current of 10µA up to 20µA will be consumed by the load at node VDD, the efficiency of the charge pump is very important. An additional negative voltage of about -400mV will obviously increase the efficiency when voltages below 800mV are available at node $VDD\_chargepump$.

Startup-phase
During the startup-phase when RF power is applied to the chip, a bypass mode in the DC/DC converter is active. If the chip is in reset mode, the chip cannot provide the power path with any frequency band information. Both, rectifier and DC/DC converter will start in ”uniform” operation mode, where the power can be delivered in weak HF field-strength and low UHF power to the internal power supply VDD. This uniform power unit configuration is called bypass. None of the power voltage levels is regulated to its well-defined final value but these values are precise enough to start the chip reliably.

4.6.1 CTS Rectifier and secondary charge pumps

Since a balanced rectifier structure with cross-coupled NMOS transistors for the generation of VSS is used for the CTS rectifier concept, the impact of these transistors on the overall junction area and on the leakage current between the two antenna pads has to be considered especially

in UHF operation mode. This is the reason for a new shunt concept, where the shunt current does not pass the cross-coupled transistors anymore and their transistor width and junction area can be reduced significantly. Especially in the HF mode we have to consider shunt currents up to 50mA DC or more than 100mA alternating current between the resonator elements. In figure

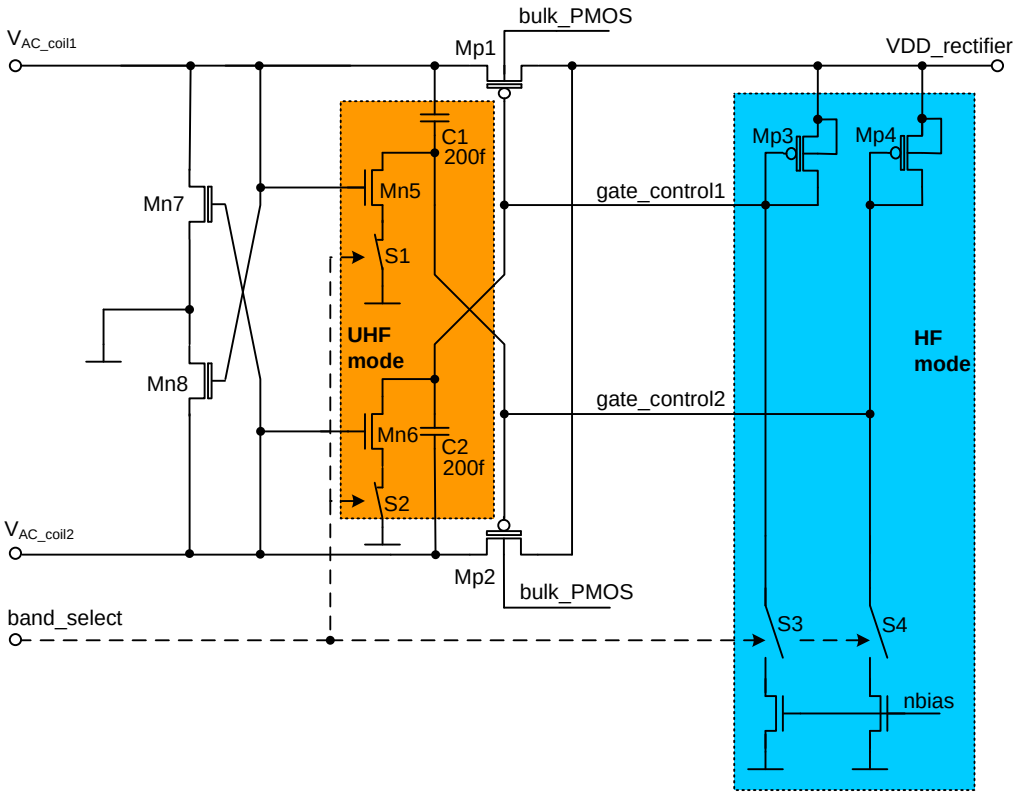


Figure 4.24: Core module of the CTS rectifier

4.24 the 2 cross-coupled NMOS and the 2 PMOS diodes are not colored. Such transistors are not activated or deactivated frequency selective.

Negative charge pump

If the $band\_select$ signal which is delivered by the clock recovery unit detects the UHF frequency at the antenna pads, the orange colored negative charge pump starts, because the signal $band\_select$ in this case is HIGH. Transistor Mn5 and Mn6 define the VSS potential for the two capacitors C1 and C2 during the positive voltage peak of $VAC\_coil1/2$. After the positive voltage peak has occurred at VAC_coil1, the bottom plate of C1 is attached to the VSS potential via S1 and a small current peak occurs through transistor Mn5. A falling potential at the antenna node VAC_coil1 pushes the potential of node $gate\_control2$ to a lower potential than VSS, as shown in figure 4.25. Because of parasitic capacitors and resistive losses in the switches, the negative peak voltage does not reach the same dynamic as the antenna voltage. If a voltage swing of $1V_{peak}$ is applied at the antenna nodes, the dynamic is reducesd to about $-500mV_{peak}$. If the voltage is below -650mV, several PN diodes start to conduct and a reverse current from VSS to the negative charge pump occurs. Thus, the power path efficiency is reduced moderately. But

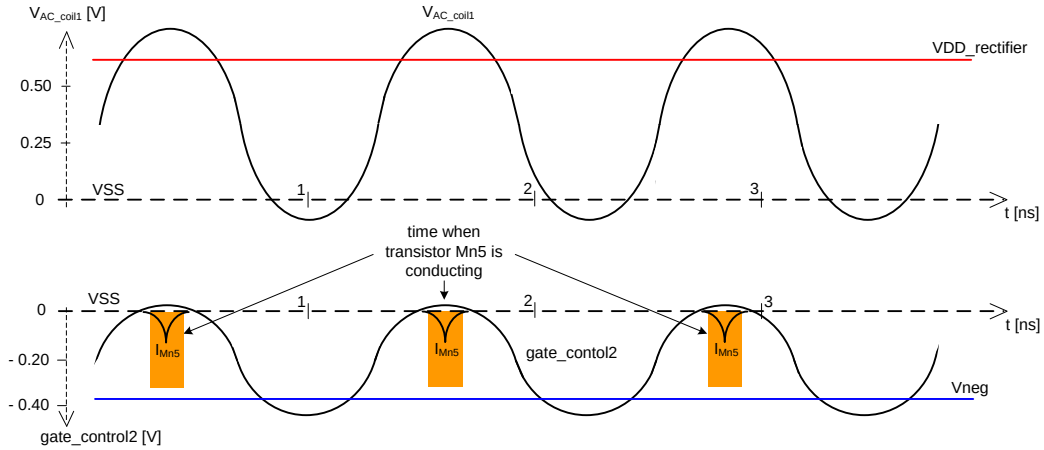


Figure 4.25: Gate control in UHF mode and generation of the negative secondary voltage Vneg

these PN diodes are the voltage limiter in high RF power conditions that are close to the reader, when the antenna voltage reaches a peak voltage of 2V. Not only the PMOS diodes are controlled by this negative voltage, but also a DC power supply $Vneg$ is generated. In figure 4.26 two low voltage NMOS transistors with a constant VSS gate potential combine the 180° phase shifted negative AC signals to one DC signal. With a threshold voltage of about 400mV, Mn1 and Mn2 are high ohmic resistors with a V_{DS} voltage drop of about 50mV. As the two transistors operate

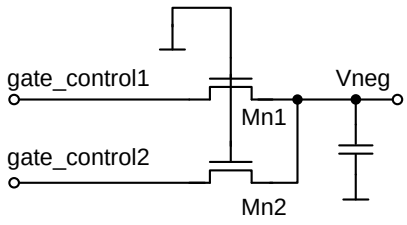


Figure 4.26: Negative charge pump

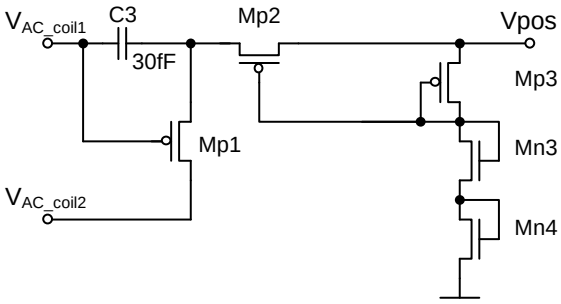


Figure 4.27: Positive charge pump

close to their threshold voltages, no reverse current occurs when the input voltage only drops by a small amount. A reverse current between the two AC nodes also reduces the voltage swing for the PMOS gates, which reduces the efficiency of the power rectifier. The impact on power losses in the negative power supply generation unit is smaller in weak power conditions compared to the benefits of a good working DC/DC power charge pump. Measurements have shown, that the improvement is +2.5dBm when a negative secondary voltage charge pump is used. For the measurements setup with and without negative pump the same VDD power supply voltage level of 1V and the same VDD load current of 10µA were taken.

Positive charge pump

A positive charge pump is necessary to control the serial regulator in the DC/DC converter. Similarly to the negative charge pump, one transistor and capacitor doubles the antenna peak voltage. Once C3 is shorted by Mp1 to the positive peak voltage of V_{AC_coil2}. Half a period later the inner plate of capacitor C3 is pushed to twice the antenna peak voltage of node V_{AC_coil1}. In serial between the weak charge pump (represented by C3 and Mp1) and the sloppy Zener diode structure (represented by transistors Mp3, Mn3 and Mn4) transistor Mp2 is used as diode and weak serial resistor. An additional capacitor in parallel to the Zener structure guarantees a constant potential during RxD and TxD phase, if the incoming power or field-strength varies a lot.

In the HF operation mode, $Vpos$ is about 2.1V so that the internal power supply voltage is regulated down to about 1.5V. As $Vpos$ is stabilized well with a capacitor of 5pF and the serial regulator structure is a source follower, the PSRR is good and the power consumption of the regulator small. A value of 30fF for capacitor C3 seems to be too low for a proper 13.56MHz charge pump operation but some tenth of nA are enough to define the gate voltage $Vpos$ to a level above 2.0V. The charge pump output $Vpos$ is loaded by a thick oxide transistor with negligible leakage current. In figure 4.28, some internal rectifier and serial regulator nodes against different

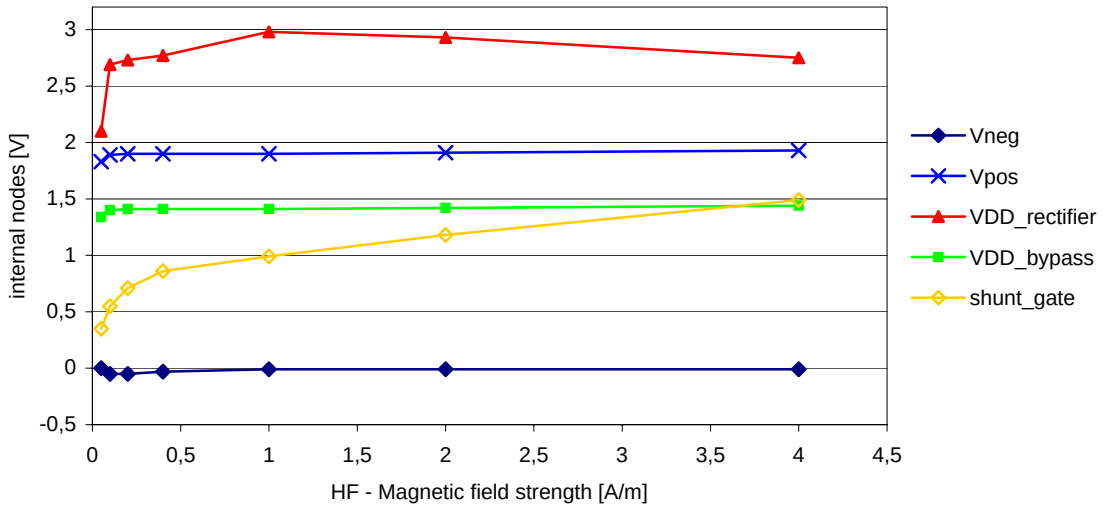


Figure 4.28: HF magnetic field strength sweep and bearing of some internal power path nodes

field-strength levels are plotted. The gate voltage of the shunt transistor which is located in the TxD unit is also shown in graph 4.28. This shunt voltage shows at which field strength level the nominal coil voltage is reached. If there is a magnetic field applied, the voltage limiter is already turned on slightly at 50mA/m, which is close to the lowest field-strength where the chip starts to work. If the field strength is higher than 50mA/m, the charge pump reaches its nominal value with the help of the weak serial transistor Mp2 and additional diode clamping. Node potential $Vpos$ is almost independent of field strength above 50mA/m. As the serial regulator is a NMOS source follower, the output VDD_bypass is as constant as $Vpos$. In summary, it can be said that the secondary charge pump clamped by a diode structure to its operational value works well in HF

mode for an overall power consumption which is smaller than 500nA.

In the UHF frequency band the serial regulator functionality is not required anymore but it still blocks the high voltage of $Vrect$ during the HF operation or during the start-up phase. $Vpos$ has to be pushed to a high potential to operate the serial regulator as a very low ohmic switch. In figure 4.29, the performance of this "switched" transistor Mn4 of figure 4.21 is illustrated. The maximum V_{DS_MN4} voltage loss is smaller than 50mV in the interesting chip current load range. Even at a very big power level of +20dBm, the rectifier and external shunt are able to limit the DC voltage to a low-voltage level where no serial regulator is necessary to protect the sensitive thin oxide transistors at VDD. Even at a low antenna voltage of about $0.7V_{peak}$ the positive charge

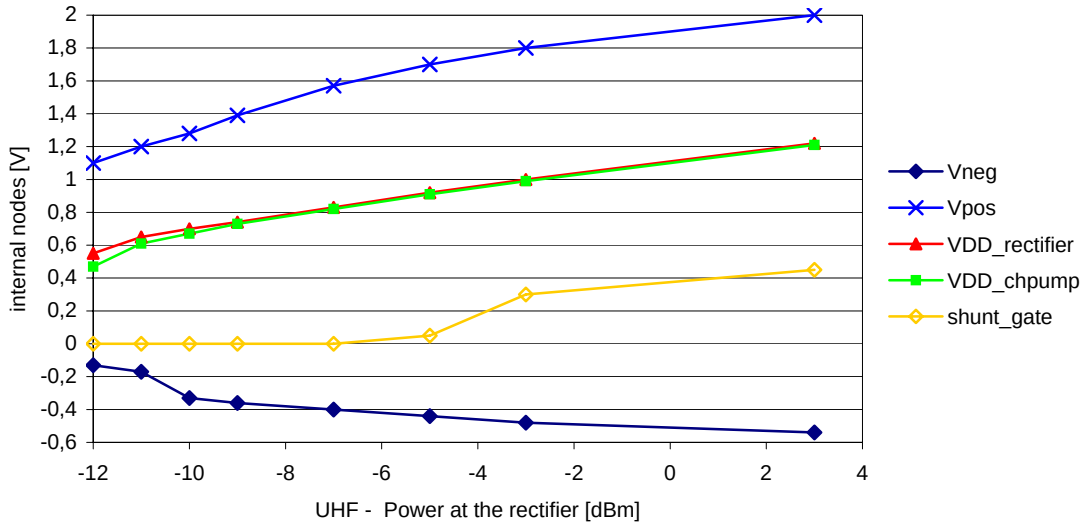


Figure 4.29: UHF power sweep at the rectifier and the impact on power path nodes

pump is strong enough to push Vpos to about $2 \cdot V_{AC\_coil1/2} - 300mV$. In a compensation for the reduced voltage level in the UHF operation mode, a frequency 80 times higher than HF increases the positive charge pump output power significantly. The positive charge pump design phase is a balancing act between different voltage levels, carrier-frequencies and only a moderate power waste in the pump stage. The charging capacitor value is the parameter with the biggest influence. A capacitor of about 30fF is sufficient to charge $Vpos$ in the UHF mode and with the help of a coil voltage that is bigger than 2V, this capacitor value is also sufficient for the HF operation mode. The bigger the charge pump capacitor C3 and the stronger Mp3, the more energy is lost in UHF mode for a pumped voltage which is not even necessary in this very power-sensitive frequency band. The other secondary charge pump $Vneg$ in UHF is also active and provides voltage down to -500mV. Both charge pumps show a sloppy output voltage characteristic against the applied UHF power, as shown in figure 4.29.

4.6.2 Bulk Potential Generation

This module is one of the crucial modules in the CTS project. Parasitic PN diodes are often included in simulation models but parasitic lateral bipolar transistors usually are not. Indeed, only

by means of the final transistor layout, an estimation of the current amplification is possible and an extraction of parasitic bipolar transistors can be done. Two parasitic bipolar transistors at the

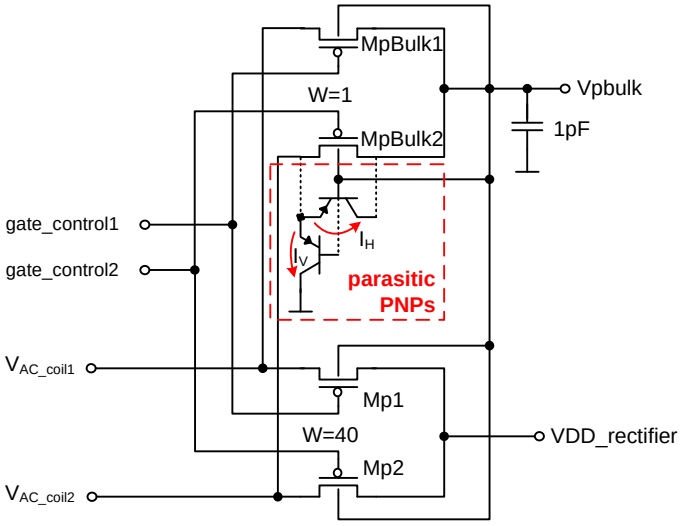


Figure 4.30: Concept for generating the highest DC voltage from the AC antenna voltage

PMOS transistor MpBulk2 are drawn in figure 4.30. MpBulk1/2 are weak transistors compared to Mp1/2 which are 40 times wider (all have the same transistor length). All transistors get the same source and gate potential. The bulk generation operates similar to the main rectifier path. A big difference is the very weak load current of few nA at the bulk node compared with the approximated 25µA which the rectifier has to provide.

Two transient phases are essential for the bulk generation:

Constant field strength
During the tag's lifetime a stable peak voltage level often exists at the antenna to chip interface. In this case, the voltage-drop from source to drain of the two PMOS transistors MpBulk1/2 has to be less than 450mV. If this is fulfilled in all process and temperature corners, no parasitic bipolar will be triggered because no parasitic PN junction is opened in forward direction.

Fast rising field-strength
A greater challenge for the bulk voltage generation is the very dynamic antenna voltage level change when the voltage at the antenna rises rapidly. In this case, the 1pF capacitor and the additional big transistor-well capacitance has to be charged. During this phase a V_{DS} voltage drop of transistor MpBulk1/2 is increased but it may not to exceed 550mV under nominal conditions. When a bipolar structure starts to conduct during this transient phase, the forward diode (emitter-base) supports the charge of the bulk-node. The disadvantage of the forward diode is that the corresponding current amplification of the vertical transistor may conduct the parasitic current Iv shown in figure 4.30 to VSS. As this could happen e.g. after every field gap, this potential parasitic Iv current could increase the average chip current consumption explicitly. Even a permanent malfunction is possible.

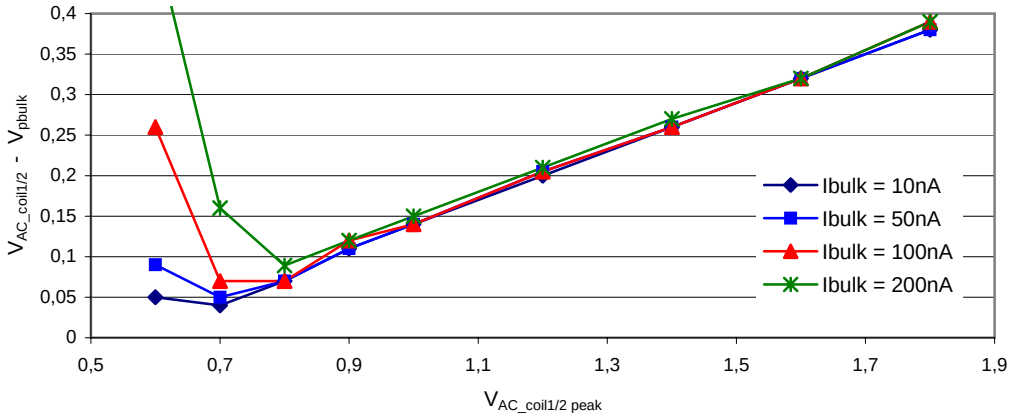


Figure 4.31: Difference between coil-peak and Vpbulk-DC voltage

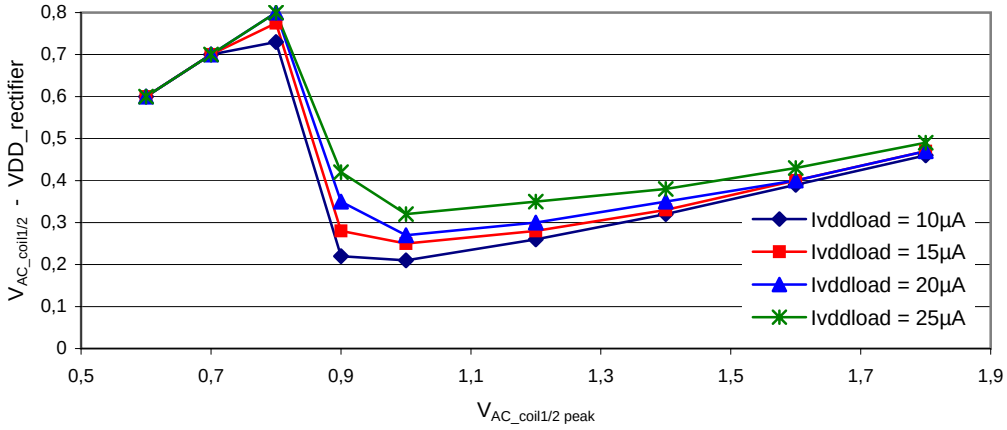


Figure 4.32: Difference between coil-peak and Vrectifier-DC voltage

4.6.3 DC/DC charge pump for UHF operation

A power supply voltage VDD of 1V is sufficient for surviving RxD and TxD energy losses. The rectifier output voltage $VDD\_rectifier$ can vary in UHF mode from 550mV up to 1.4V (see figure 4.29). To close this gap, a voltage doubler with a good voltage boosting factor will be introduced in this chapter. Moreover, designs with two capacitor stages were simulated, but the efficiency and the minimum operation power level of a single stage charge pump was never reached.

In the CTS DC/DC charge pump a switched PMOS and a NMOS are used for power transfer from node $VDD\_chargepump$ to the internal power supply VDD. In figure 4.33 an additional secondary charge pump can be seen which controls the main power charge pump. NMOS transistor Mn1 is used as low side switch, because with VSS potential at the gate this type of transistor can be switched off fast and well defined. If a PMOS would be used instead of the NMOS at its gate, a voltage level close to the pumped peak voltage would be necessary to prevent backward current from C1 to node $VDD\_chargepump$. CMOS inverter Inv2 switches the bottom plate of

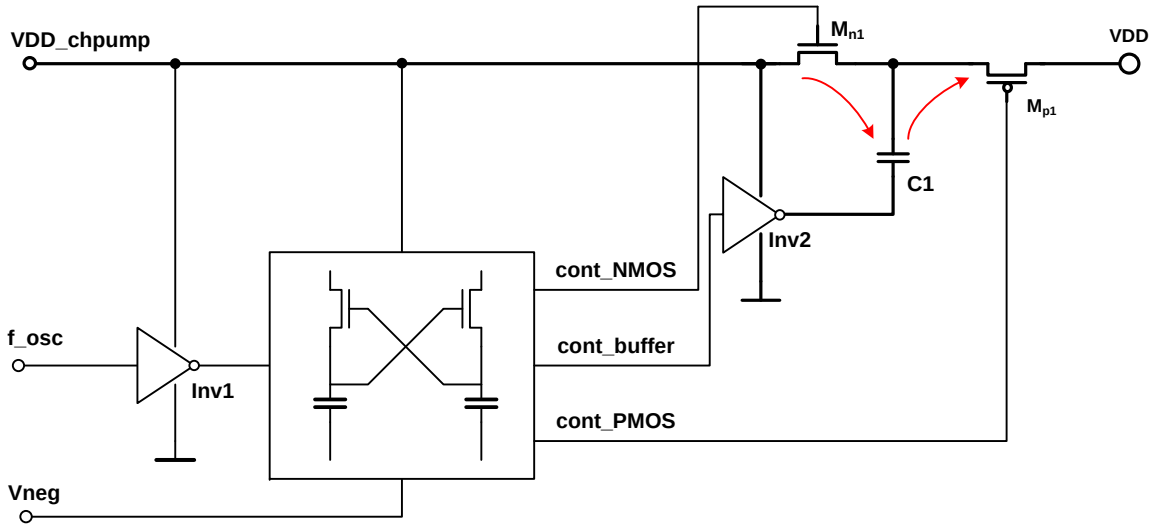


Figure 4.33: Architecture of the CTS single stage charge pump

the poly-poly capacitor C1 between VSS and $VDD\_rectifier$ potential and doubles the voltage at the top plate (if all parasitics are neglected). With the $Vneg$ potential at the gate of power transistor Mn1, PMOS transistor Mp1 is switched on very well and charge is transported to the VDD energy reservoir capacitor.
Only one clock signal (instead of two or even four non-overlapping clock signals) is necessary to operate this charge pump without reverse currents and with high over-all power efficiency. Time delays in control paths and the use of NMOS and PMOS transistors in the right position of the power path design reduce the risk that some amount of charge might take the way back to the source. For a non-overlapping clock unit several logic gates are necessary which waste power and finally decrease the power efficiency.
Furthermore, the additional power consumption in the negative secondary voltage $Vneg$ should be considered carefully. As the impedance of this weak negative charge pump is high, the voltage may approximate the VSS potential more and more, especially when the power consumption is bigger than 500nW. Therefore, only a few selected transistors which are used to control ”power” transistors are attached to this sensitive node. In graph 4.34 the influence of 4 different $Vneg$ voltage potentials on the efficiency of the voltage doubler is shown. Especially at weak power conditions below -5dBm and at a load current of 20µA, the rectifier DC level $VDD\_rectifier$ is below 0.75V. The lowest $VDD\_rectifier$ voltage level at which the charge pump still runs sufficiently is 0.65V, which results in a $VDD\_chargepump$ potential of 0.55V. These voltage levels are equivalent to -9.5dBm incoming power at the rectifier. In graph 4.35 $Vneg$ was measured with a running DC/DC charge pump, which corresponds to an average load current of about 40nA at the output of the negative secondary charge pump. As the graph has a ”weak” characteristic, both the dimension especially of the capacitor especially and the switch of the negative pump at the antenna input have to be sized carefully. $Vneg$ is also a good indicator for the negative voltage pulse levels at the gates of transistor Mp1 and Mp2 which are shown in figure 4.24.

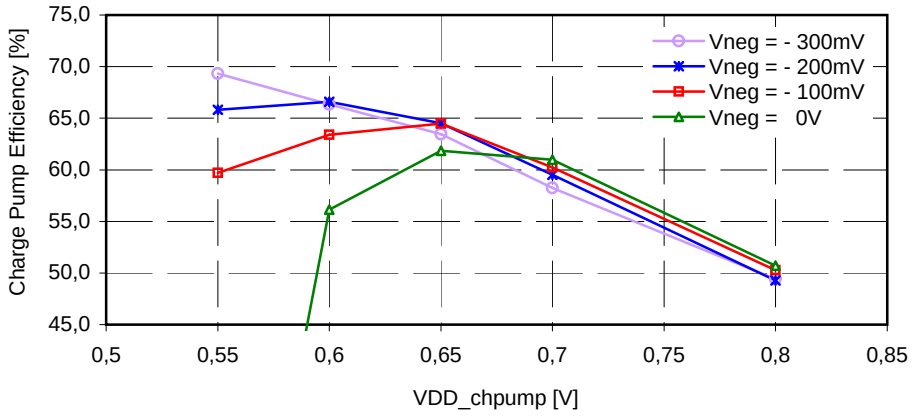


Figure 4.34: Measured power transfer efficiency versus Vneg voltage level

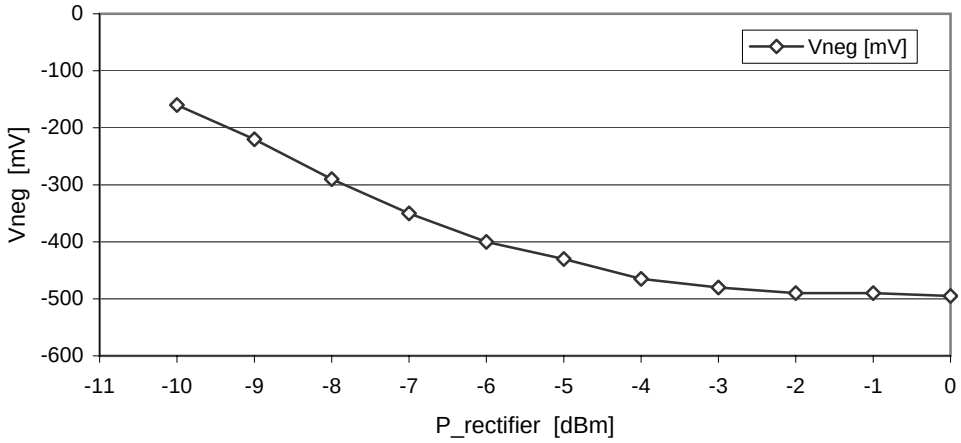


Figure 4.35: Measured negative charge pump Vneg versus incoming rectifier power

A detailed CTS DC/DC charge pump schematic is shown in figure 4.36. All transistors are thin oxide devices and are protected via a serial regulator against high rectifier DC output voltages of up to 4V in the HF frequency band operation. Node VDD_chpump is the rectified and regulated voltage which delivers power to charge the capacitor C1 with the frequency f_osc. As the VDD_chpump voltage level can drop down to 0.5V during a charge cycle, a PMOS transistor with the VSS potential at its gate is an insufficient conductor. With the negative charge pump a potential of -0.4V can applied which results in a better conductive PMOS transistor Mp1.
During the second phase, when charge is transported via the second transistor to the internal power supply, a PMOS transistor would need a bigger voltage than VDD_chpump to stay non conductive. These measures - once a negative and once a positive control voltage - result in a NMOS as first power transistor in the charge pump.
A very efficient low power secondary charge pump delivers the doubled control voltage for this MNOS Mn1. A kind of level shifter defined by transistor Mn3 and C2 controls the power switch Mn1. This level shifter also uses the negative voltage $Vneg$. The control voltage at node

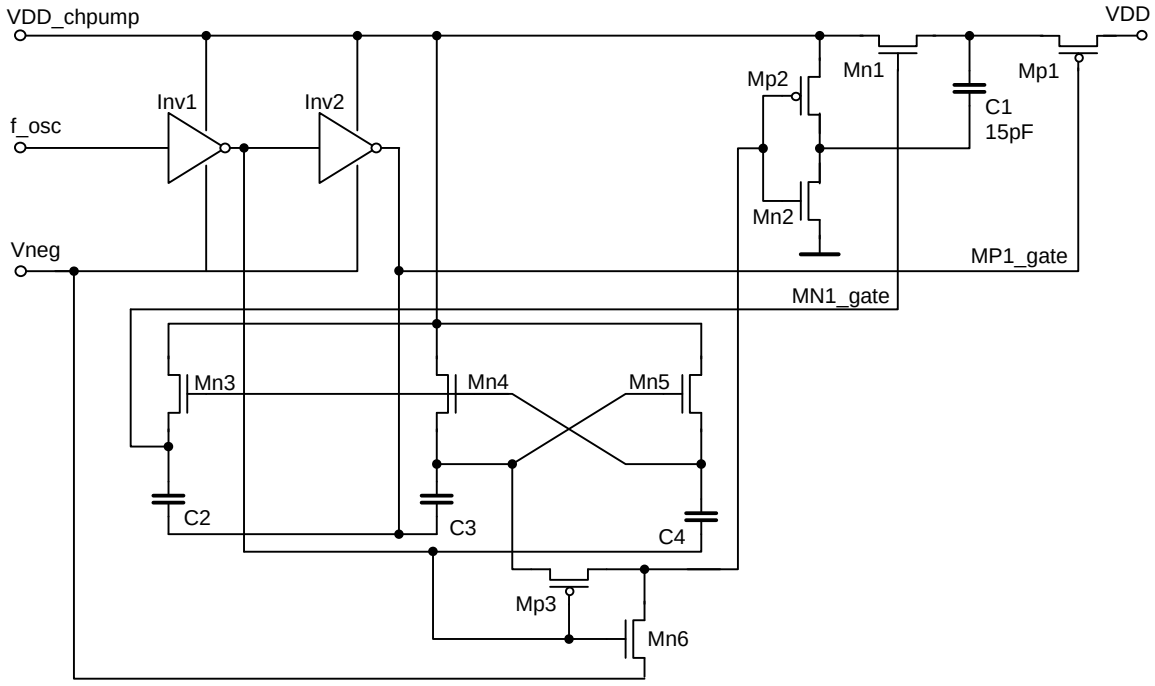


Figure 4.36: Schematic of the CTS charge pump

$Mn1\_gate$ reaches the VDD_chpump level more than two times. In figure 4.37, the control gate reaches a voltage level of 1.4V while the power source delivers 0.6V only. A U_{GS} voltage of 1.2V down to 0.8V is enough to get a well conductive transistor Mn1 for charging capacitor C1 within 250ns. A leakage current during the first phase from the internal power supply to capacitor C1 caused by MP1 would increase the charging speed of this node and decrease the efficiency of the pump only moderately.
A PMOS Mp1 is used during the second phase when the collected charge during the first phase has to be transferred to the internal power supply VDD. With the help of $Vneg$, transistor Mp2 pushes the bottom plate of C1 fast to the VDD_chpump potential and charge is transfered to the internal power source until the top plate potential is dropped down to VDD potential. The size of transfer transistors Mp1 and Mn1 are designed to fulfill a 100% charge transfer during 200ns in each phase with an additional 20% margin. The small additional amount of energy necessary to control the transfer transistor can be neglected compared to the efficiency losses of the DC/DC charge pump when no negative voltage is applied. Figure 4.37 shows the transient DC/DC converter start-up phase when VDD is pumped up by a factor of 1.4 - 1.8 times VDD_chpump. It is important that the first charge transfer switch Mn1 is clearly switched on and especially in the next phase clearly switched off. With a combination of NMOS and PMOS transistors, no charge pump typical non-overlapping clock scheme is necessary to lower the power consumption because only one clock f_osc, which is derived from the internal oscillator, is used.
A compact low power level shifter and once again only a few transistors at $Vneg$ guarantee a good DC/DC converter efficiency. Parasitic capacitance to substrate of the used poly - poly transistor reduces the efficiency compared to an ideal capacitor by a factor of 8%. The power charge pump efficiency versus the input voltage level is shown in figure 4.38. For this simulation the load

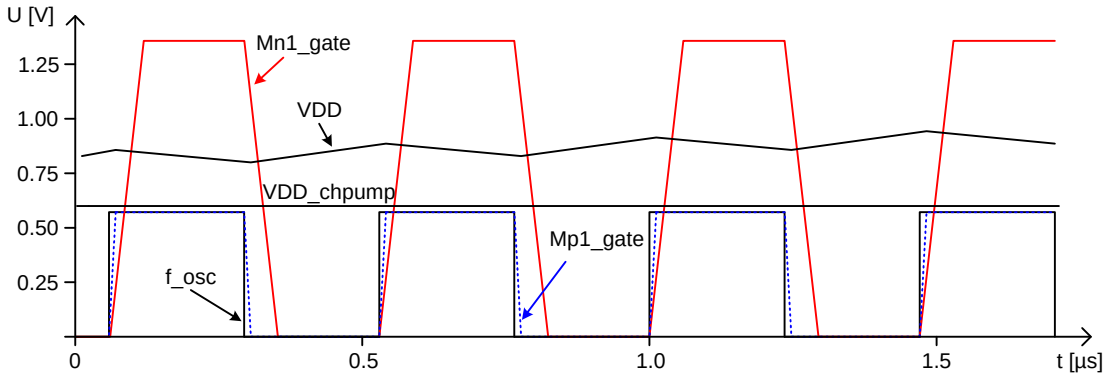


Figure 4.37: Some transient nodes of the DC/DC converter during charging of VDD_internal

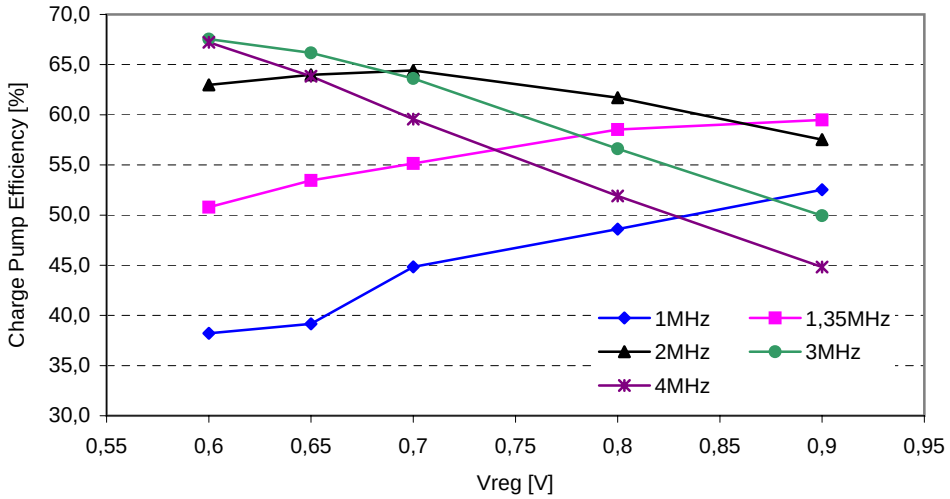


Figure 4.38: Charge pump efficiency versus local oscillator frequency at constant load (Vreg = VDD_chpump)

current was assumed to be constant at about $10\mu A$. The clock frequency of the local oscillator was varied from 1MHz up to 3MHz. The optimum frequency for the CTS chip is slightly below 2MHz (1.92MHz). At lower frequencies, the boosting capacitor C1 is too weak and the internal voltage will not reach its nominal value any-more. When the oscillator frequency is increased to 3MHz and more, the transferred power is higher than the consumed load power and the internal voltage limiter will waste the additional power.
In figure 4.39, another simulation parameter - the internal load current - was changed. The oscillator frequency, however, was constant at 2MHz in this graph. The current consumption was changed stepwise and the internal generated voltage VDD was measured. With this setting the best performance can be achieved with a load of $10\mu A$. Is the load smaller, the wasted power in the internal limiter increases with the input voltage. At higher load currents the charge pump is not able to deliver the necessary amount of charge to the output, especially not with small input voltages applied to the input of the charge pump.

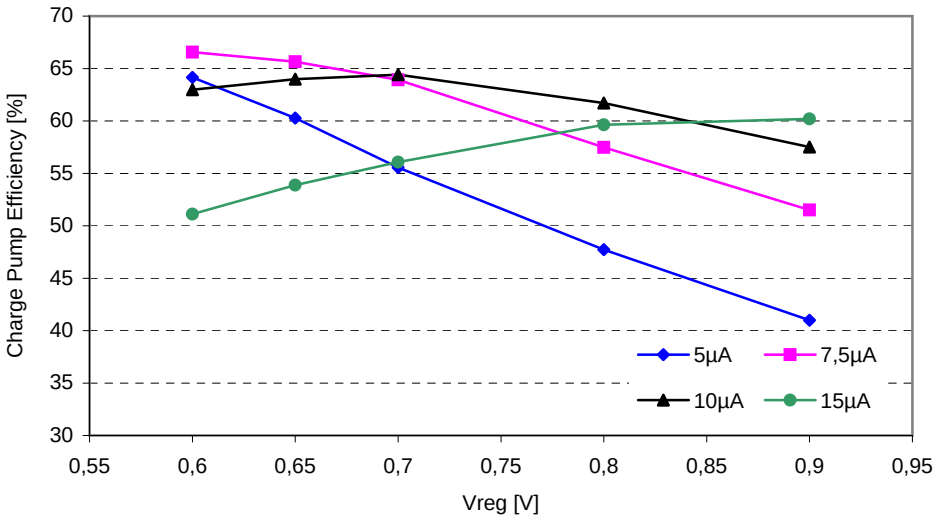


Figure 4.39: Charge pump efficiency versus different constant load current at constant oscillator frequency (Vreg = VDD_chpump)

The charge pump efficiency is designed to reach the optimum of 65% with a load current of about $10\mu A$ and an internal oscillator frequency of 2MHz. The minimum operation voltage is 0.6V.

4.6.4 Serial NMOS voltage regulator

A passive serial regulator is used to reduce a rectified voltage level of 4V down to 1.5V. By Using a buck converter (with an external inductor) for a highly efficient down conversion or a down converter with switched capacitors it costs additional silicon area or even an external element and only increases the contactless performance in the HF frequency band mode. As this band is used as near-field communication medium and UHF for far distances anyway, an increased communication distance of approximately 10% is not necessary or even against some application use cases. Two linear serial regulator concepts are shown in figure 4.40. Considering the

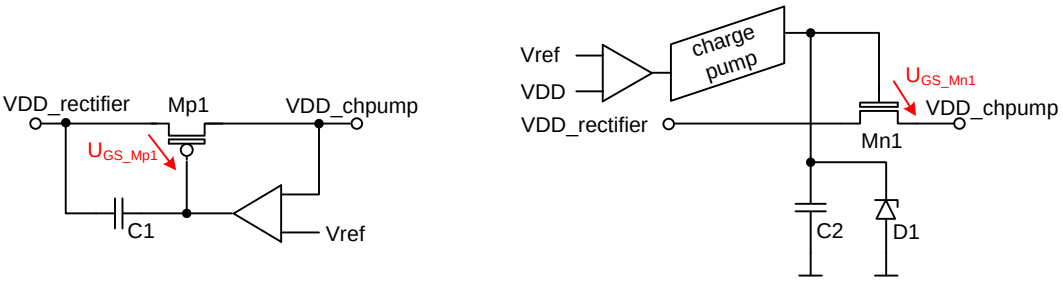


Figure 4.40: PMOS or NMOS transistor used as power regulator

regulation, point of view it would be easier to control a PMOS serial regulator because the reg-

ulator's power supply of the regulator could be the unregulated input voltage $VDD\_rectifier$ and VDD_chpump. As the rectifier, however, delivers in weak field situations especially a very dynamic $VDD\_rectifier$ potential, the regulator should have a PSRR bigger than 26dB. Small signal analysis response for NMOS and PMOS serial regulator are illustrated in figure 4.41. Stimulation and load testbench are similar for both versions. Only the PMOS transistor width is twice as much as that of compared to the NMOS width. For both regulator versions, a current con-

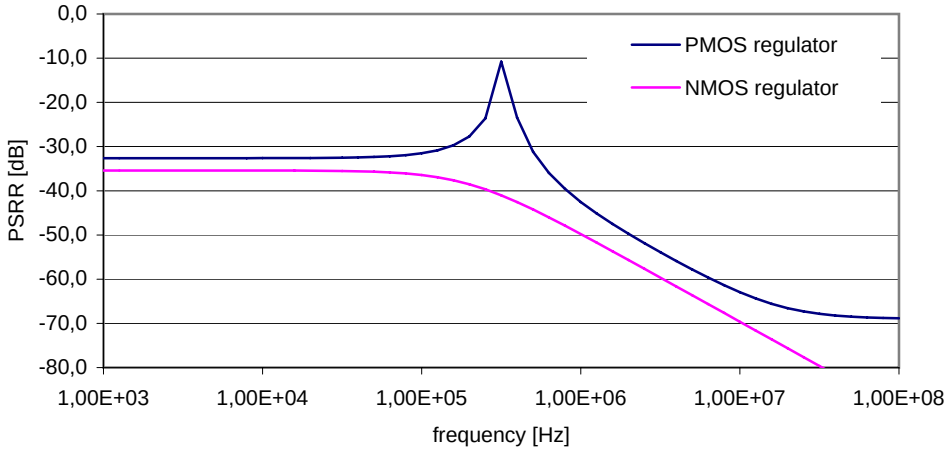


Figure 4.41: PSRR Comparison of NMOS and PMOS serial regulator with same testbench and similar transistor geometry

sumption of about 1µA is used for the regulation circuit and the overall regulator sizes are also similar. Especially during the load modulation phase with at a sub carrier frequency at of about 100kBit, the PSRR of the PMOS gets much worse compared to the NMOS. When the regulator current is increased, the PMOS performance will gets better, but a current consumption bigger than 1µA is not acceptable for a simple regulation system any more.
Why is a good PSRR so important for passive RFID transponder units during the RxD phase? When the field-strength decreases during RxD, the capacitor attached to $VDD\_rectifier$ and the sink current dominate the steepness of the falling slope. A typical value is 0.2V/µs. This moderate slope value is not reached at the rising edge anymore, because the field- strength rises fast and the rectifier hands over this speed to the node $VDD\_rectifier$. A rising slope speed of 10V/µs challenges the regulation speed of a PMOS. So during the RxD phase we have to take a value for the falling edge that is in the low frequency region shown on the left side in graph 4.41. Using an NMOS serial regulator, a constant and stable voltage source at the regulator gate is sufficient to get a PSRR value higher than 20dB. The disadvantage of this regulator concept is the need for a higher control voltage level. This level can either be supported by the input voltage or after the startup phase by the output voltage. This high voltage level is generated by a weak charge pump. In the CTS project, a very weak voltage doubler, as shown in figure 4.27, is used with a sloppy shunt for defining the gate potential of the serial regulator. As the power serial regulator has to be used, this results in an additional voltage drop over the serial transistor in the UHF frequency band. In UHF, it is also necessary to protect thin oxide transistors in the DC/DC charge pump with a good PSRR.

In figure 4.42 the detailed schematic of the positive charge pump is shown. The power con-

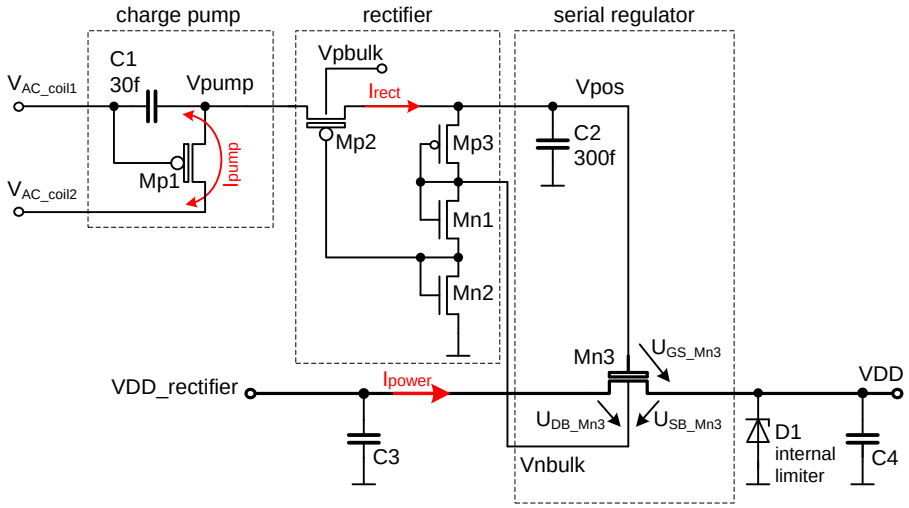


Figure 4.42: Detailed schematic of the serial regulator

sumption of this control circuit for the serial regulator is $\leq 500nW$ at low incoming UHF power and $\leq 100nW$ at small HF field-strength. If the incoming power is increased in the UHF band, the antenna voltage also increases and the efficiency decreases because the commuting current between the two antenna nodes and via C1/Mp1 increases. But there is no drawback of this increased current in the charge pump, because in this case, the available power at the antenna is far above the minimum power limit of the chip and excessive power has to be exhausted somewhere on the chip anyway.

In figure 4.43 simulation results of a UHF power sweep and a HF field-strength sweep are shown. In both bands the positive charge pump pushes node $Vpos$ to 2.5V in UHF and 2V in HF operation mode. During the UHF operation mode the serial regulator control voltage U_{GS_Mn3} is higher than in HF mode because the active power charge pump is located behind the regulator and the regulator operates as switch. An average charge pump efficiency of 60% and a similar current consumption in HF and UHF cause higher current through the serial regulator transistor Mn3. Under a specification conform operation, the typical coil voltage $V_{AC\_coil1/2}$ reaches from 3V up to 4.5V in HF mode and from 0.8V up to 2Vin the UHF mode. In figure 4.43, no external voltage limiter is used; thus a coil voltage of 5.2V is possible in the HF mode.

The conclusion drawn from figure 4.43 is that the voltage dynamic at the internal power supply VDD is reduced by a factor of 10 compared to the output voltage $VDD\_rectifier$ which is delivered by the rectifier. The chip area for the charge pump and shunt regulation overhead is dominated by capacitor C2 and transistor Mn3.

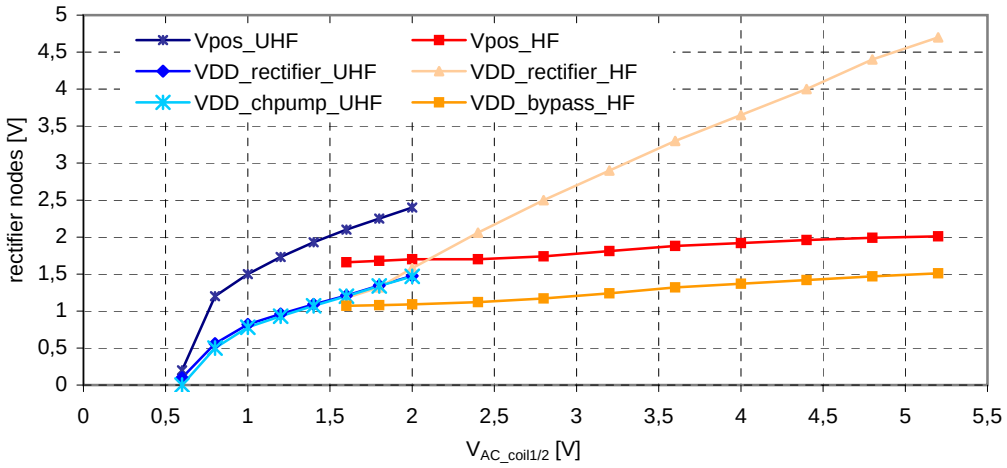


Figure 4.43: Serial regulator nodes measured at different Coil or Antenna voltages

4.7 Alternative rectifier concepts for multi band applications

During this thesis some alternative power generation concepts were designed, simulated, layouted and measured. All following rectifier concepts are applicable to multi-frequency RFID transponders. Some of the following rectifier architectures are partially similar to the CTS rectifier concept. These rectifiers were fabricated in a 220nm Infineon CMOS technology process with EEPROM option. Thin oxide transistors with a 220nm gate length behave similarly to the faster 120nm process. The maximum gate-to-bulk voltage for thin oxide transistors is raised from 1.5V to 2.5V. Thick oxide devices have the same characteristic in both technologies and are used in the CTS chip.

The measurement setup to test the rectifier performance is shown in figure 4.44. The measurement setup includes the network analyzer, a matching network, the rectifier and a constant load. Rectifier structures shown in figure 4.45 are the alternative design concept for the CTS

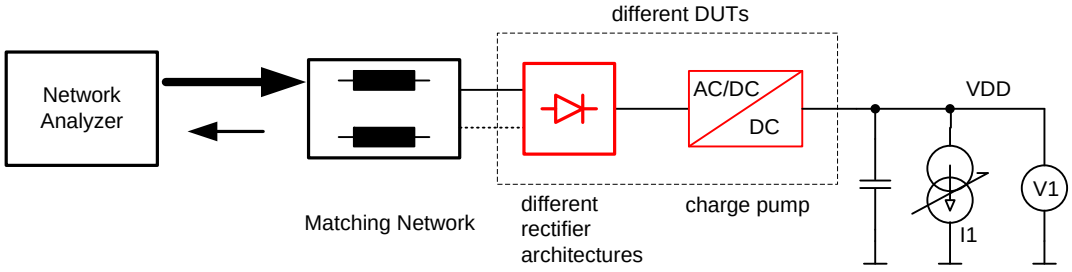


Figure 4.44: Some rectifier architectures are measured and finally compared

chip. On the left side, a cross-coupled NMOS and PMOS pair rectifier version shows a very good power performance. When at this rectifier the coil voltage is increased over one PMOS threshold voltage, a circular current takes place between the two coil pads over the common DC node of the rectifier. The rotating current is especially bad during the HF load modulation period, because

the coil voltage is clamped during this time and the modulation index is too small. Because of its good UHF performance, however, this architecture is still interesting and is going to serve as benchmark. The second rectifier concept is illustrated on the right side of figure 4.45 and it

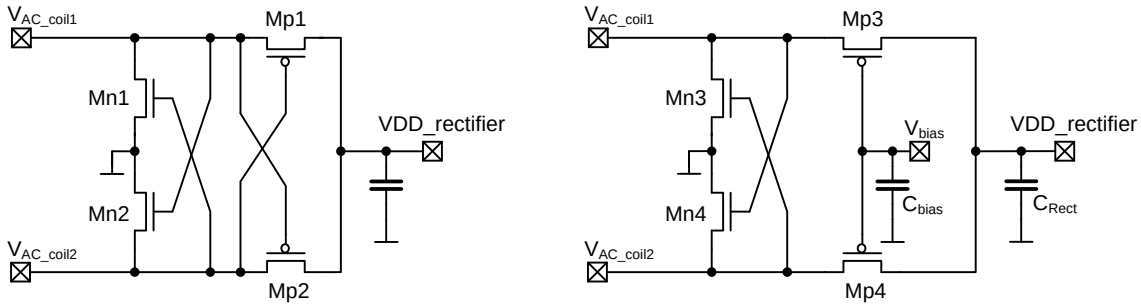


Figure 4.45: A cross-coupled and a constant bias voltage controlled rectifier

is very similar to the CTS architecture. This rectifier, nevertheless, is designed with thin oxide devices. For the frequency mode switching no design overhead is implemented which reduces the parasitic capacitance compared to the CTS architecture. The gate control voltage V_{bias} can be adjusted externally. A higher coil voltage with low circular currents can be archived when the external gate potential V_{bias} is increased to about 2V. V_{AC_coil} reaches a positive peak voltage of 3V.
The last rectifier version was built with Schottky diodes shown in figure 4.46. Such a diode can be

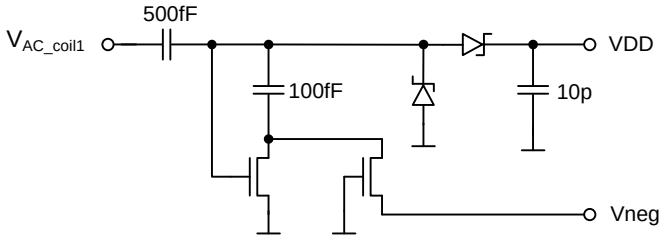


Figure 4.46: Unbalanced Schottky diode rectifier with generation of negative secondary potential

manufactured with a standard CMOS process but it is not qualified for the used Infineon process and, therefore, it cannot be used productively. This voltage charge pump is a common architecture for UHF [KF03] [Bak07], but cannot be used for HF. The cross-coupled NMOS pair, which is necessary to avoid negative coil voltages during HF, is missing in this concept. This Schottky diode rectifier was implemented and measured because of its good UHF performance.

4.8 Measurement results of different rectifier architectures

All rectifier structures were manufactured in silicon and tested with a network analyzer under UHF conditions. Thick oxide MOS transistors were used for the CTS interface between the antenna and rectifier. To be able to compare the platform in 220nm, one cross-coupled design with thick

oxide transistors was implemented, too. For good matching conditions, the resonance frequency for these chips was adjusted to about 900MHz. The frequency adjustment was done with external components in the matching circuit.

Cross-coupled rectifier

The cross-coupled PMOS version has the advantage that all 4 transistors start to conduct reliably little above their threshold voltage V_{th}. When low voltage transistors are used, the rectifier starts to conduct at an antenna peak voltage of about 600mV. When the power at the rectifier input increases, the voltage also rises but the circular current from one antenna node to the other will also increase, too. The disadvantage of the cross-coupled transistor pair concept is the limitation of the antenna voltage - especially in weak HF field-strength conditions.

Constant bias rectifier

The second rectifier version with bias voltage control can also be used for higher antenna voltages. The bias voltage has to be tuned to one threshold below the maximum peak antenna voltage the rectifier is conductive during the voltage peak and the circular current is small. This is the reason why a similar type of rectifier architecture is used in the CTS chip. In the 220nm technology $V_{AC\_coil1/2}$ can reach a voltage level of 3.5V without damaging thin oxide transistors. Both architectures show a good performance with thin oxide transistors. With an internal power supply voltage below 1V, the performance of these two MOS architectures is even slightly better than that of the Schottky diode charge pump. When thick oxide MOS transistors are used, the

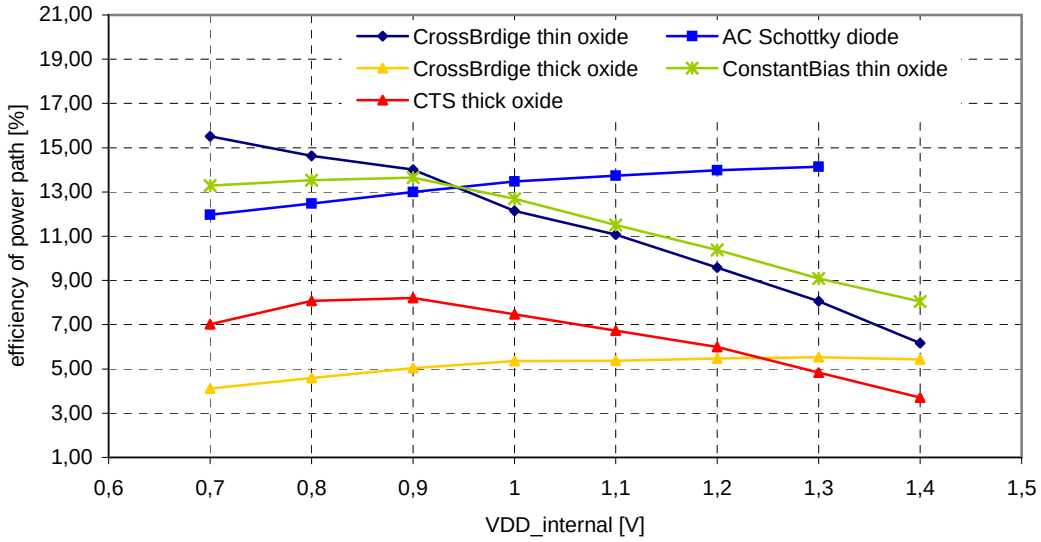


Figure 4.47: Comparison of different rectifier architectures and the impact on the overall power path efficiency

efficiency of the cross-coupled rectifier - referred as $CrossBrdige$ in figure 4.47 - decreases rapidly from 15.5% down to 4% at 0.7V $VDD\_internal$. To conclude, we see that the constant bias rectifier which is built with thin oxide transistors could improve the energy performance of the thick oxide CTS rectifier by a factor of two.

Measurement setup
For UHF power measurement with a network analyzer impedance matching is a pre-condition for reliable measurement results. If no matching structure is switched in front of the DUT (Device under Test), the reflected power is similar to the delivered chip power and the S11 factor is close to 1. The small delta to S11=1 is much too small to get a high confidence level for the measured value.
Impedance tuning with an external impedance tuner or matching with external components is necessary [MS08b] [GRH$^+$09]. Since a balanced rectifier structure was implemented in this project, a careful DC decoupling is necessary. In figure 4.48, the favored measurement method is shown.

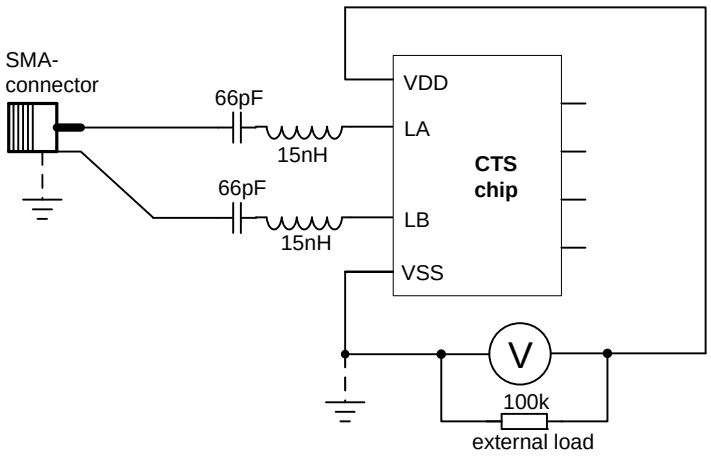
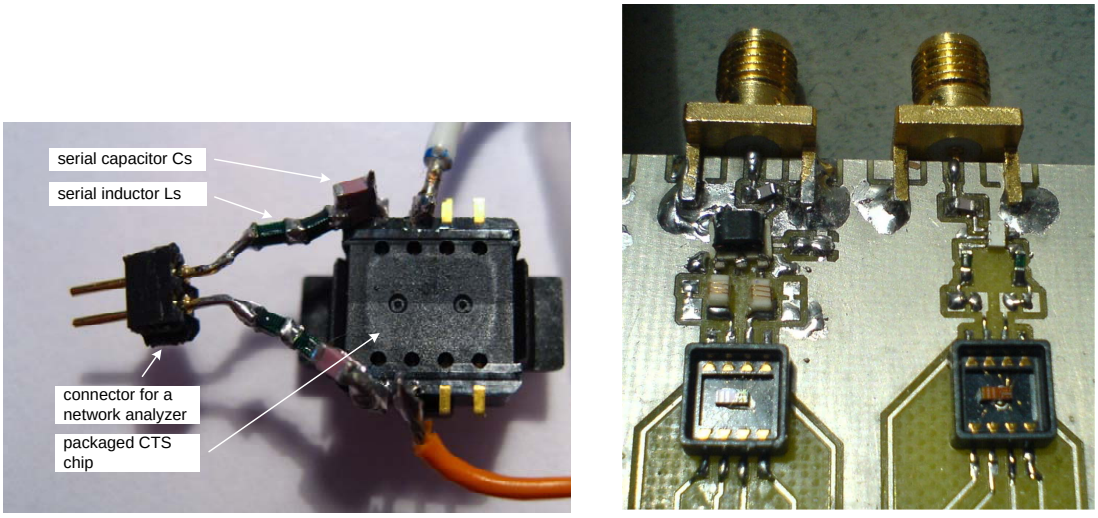


Figure 4.48: Circuitry for incoming power measuring versus generated DC voltage

A very compact circuitry is shown in figure 4.49(a). No lossy carrier material is in front of the bonded CTS chip because all external components are soldered without the help of a printed circuit board. The counter part of the shown plug is a modified SMA connector which can be screwed directly to the network analyzer as an interface. With inductance and carrier frequency tuning the chip capacitor impedance can be compensated and the measured S11 reaches a minimum (of about 0.1). If the resonance frequency is close to the 868MHZ UHF center frequency, the S11 value can be measured and will be precise. Then, the absorbed rectifier power can be calculated (see chapter 3.5.1).
Electrically the same circuit is shown in figure 4.49(b). In addition, baluns were used to decouple the chip from the network analyzer. The PCB has the benefit of a robust substrate but additional board parasitics will cost performance in the region of a few tenth of dBm.

4.9 Layout

In the CTS analog front end, the power generation occupies most of the chip area. Especially the energy reservoir capacitors on the serial regulator and rectifier are responsible for the biggest amount of silicon area. Capacitors and the drain/source area of the serial regulator is respon-



(a) Loose soldered matching network

(b) PCB based matching network

Figure 4.49: Optional caption for list of figures

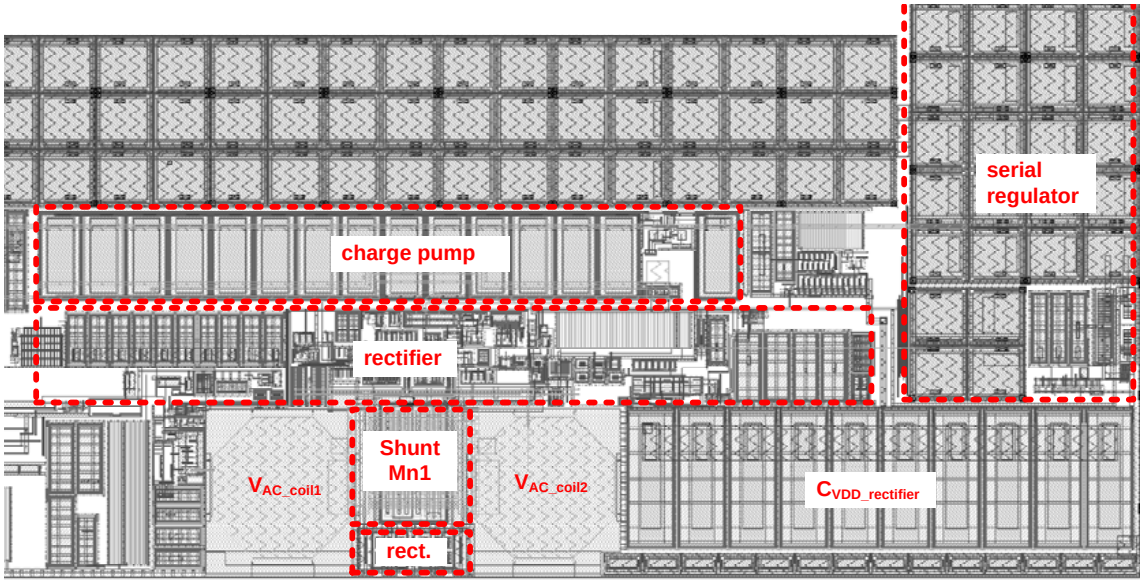


Figure 4.50: Modules necessary for the power generation of the CTS chip

sible for an area of $\approx 0.052mm^2$. The power charge pump with $\approx 0.09mm^2$ is similar in size compared to the rectifier module area and is also dominated by poly-poly capacitors.
Shunt or voltage limiter transistor Mn1 is not part of the power generation unit. It is described in chapter "Contactless communication units". The reason why this transistor is located in between the two pads is that all transistors attached to the RF pads $V_{AC_coil1/2}$ have to be as close as possible around the RF pads in order to reduce substrate losses or intensive coupling to surrounding metal lines.

5 Clock Generation Units

Which type of oscillator has to be used mainly depends on the timing requirements and on the chosen air interface protocol. In synchronous interfaces with precise timing requirements, it is necessary to use quartz oscillators with an absolute frequency error of a few ppm. Such local oscillator systems are too expensive for low cost RFID systems and are not necessary for the coding or for the observance of a frequency mask. A typical UHF RFID clock source is a local low power oscillator built with about 15 - 30 transistors.

5.1 Requirements for the clock generation units

Typical requirements for an oscillator are the center frequency, the long and short time accuracy of the delivered clock signal, the power consumption, the delay at the start-up or the minimum power supply voltage. Typically, in RFID chip systems the digital state machine power consumption is the biggest power consumer. As the power waste is proportional to the clock frequency, the state machine architecture is designed in a way that each digital sub-module is controlled with its optimal (lowest) frequency. In the CTS chip two different clock sources are used; namely a local oscillator for the UHF EPC Gen2 coding and a 13.56MHz clock recovery for the HF EPC. An architecture without dedicated local oscillator can also be chosen [KCPS08]. However, in this application a time dependent module is integrated which supports the relevant timings for the chip.

5.2 HF Clock Recovery

By means of a clock recovery it is possible to extract the 13.56MHz clock from the coil voltage reliably. Next, low power HF clock recovery and the CTS band detect unit are combined in one module.
The following two clock recovery concepts are typically used for low power passive RFID:

- Inverter (Asymmetric-Inverter)
- Source follower

Both designs will be described later in this thesis. Some basic electrical requirements for this CTS clock recovery module are:

- $V_{COILmin} = 500mV_{peak}$
- $V_{COILmax} = 4V_{peak}$
- $Pload_{typ} = 500nW$

- $VDD = 550mV \ldots 1.8V$
- $I_{bias} = 100nA \pm 30\%$

No frequency divider and no powerful clock driver is included in the 500nW power requirement. In order to get the information of the right frequency band during the power-startup as early as possible, the minimum VDD level has to be at about 550mV. The clock recovery schematic is shown in figure 5.1. NMOS transistor M_{n1} is connected as source follower and once converts

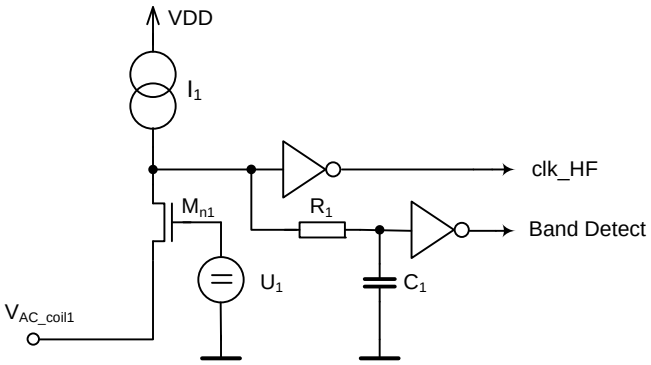


Figure 5.1: Block architecture of clock recovery and band detect

the AC coil voltage into an oscillating voltage with VDD level or into a slowly changing DC voltage (band detection functionality).

Clock extraction is the common method at 13.56MHz (which is generated by the reader's magnetic flux) to guarantee a stable system frequency for the operation time. During RxD and TxD the risk of clock losses is high but the chip performance can benefit from it. If the coil voltage $V_{AC\_coil1/2}$ is smaller than one threshold of the MOS transistor Mn1 during RxD (e.g. 100% ASK), the clock recovery will fail. During this period there can be no power delivered via the rectifier to the chip load either. This behaviour is good for the maximum power performance. The digital load is switched off by stopping the clock for the digital modules. It is necessary to include the possibility of such clock losses during contactless communication in the digital decoder concept to be able to deal with.

Transistor M_{n1} is connected to the current source transistor Mp1 which acts as a current comparator. The voltage-decision level at the source of Mn1 is at about 400mV. As the antenna voltage drops periodically with a duty cycle of about 50%, the HF Clock output clk_HF toggles at 13.56MHz according to the coil voltage.

5.2.1 Frequency Band Detect Module

A carrier frequency in UHF mode of 860MHz is too high for a low power clock recovery similar to the HF one. If a frequency is higher than about 100MHz applied to the clock recovery input structure, the current source Mp1 is too weak, saturates up to a static value and causes no additional current. With the information of this saturated input-structure, the clock recovery delivers a stable logic HIGH level at node $BandDetect$ in UHF (starting from the 400MHz band). Because of that information some analog modules are tuned (e.g. rectifier) or they are selected/deselected (HF

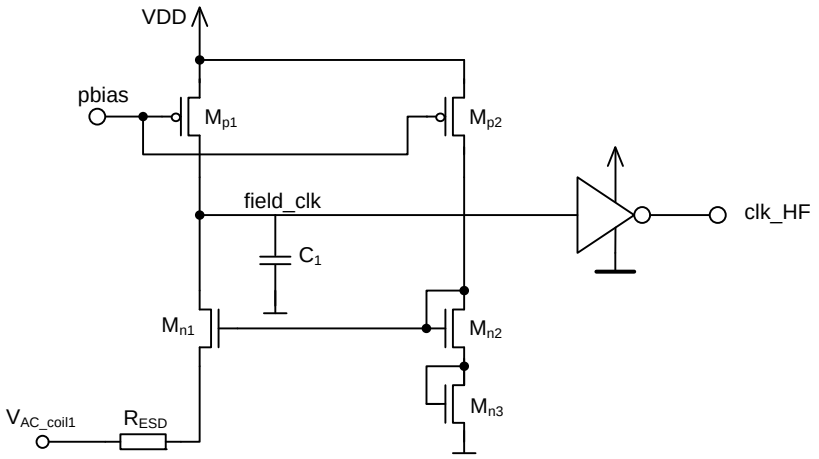


Figure 5.2: HF clock recovery

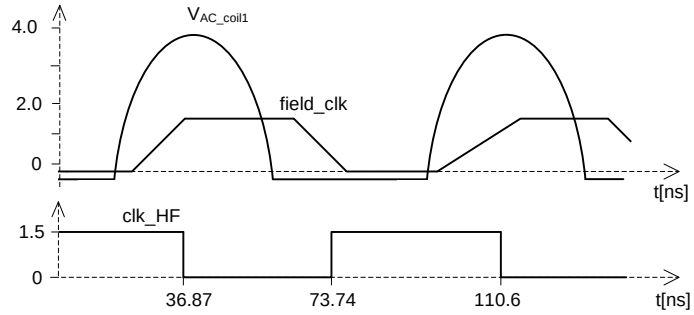


Figure 5.3: Timing - HF clock recovery

or UHF demodulator) to increase the data and power performance.
In the HF band, transistor M_{n1} is nearly very ns conductive for a short time and discharges node $field\_clk$ regularly close to VSS potential. $C1$ with 20fF and a weak current from current source transistor Mp1 of 500nA results in a stable DC voltage during the UHF operation. One NMOS threshold of M_{n4} is the trigger-point for the current comparator M_{n4} / M_{p4}, which is responsible for the conversion of node $field_clk$ into a digital logic state.

5.3 UHF Local Oscillator Concepts

UHF RFID protocols consider the fact, that no quartz-precise or quartz-constant frequency is necessary on the chip. The diploma thesis by Johann Heyszl [Hey07] (part of the CTS project) and the leading UHF tag manufacturer Impinj [Imp05] showed that the minimum local oscillator frequency is 1.92MHz to support all data rates which are specified in the EPC UHF Gen 2 standard [CSHW07]. If the oscillator center frequency is chosen to be higher, the power consumption increases linearly, too. But no advantage for contactless communication robustness can be gained from the higher oscillator frequency. A rough current consumption estimation of the digital CTS unit results in $5\mu A/MHz$. When only a handshake acknowledge or a serial num-

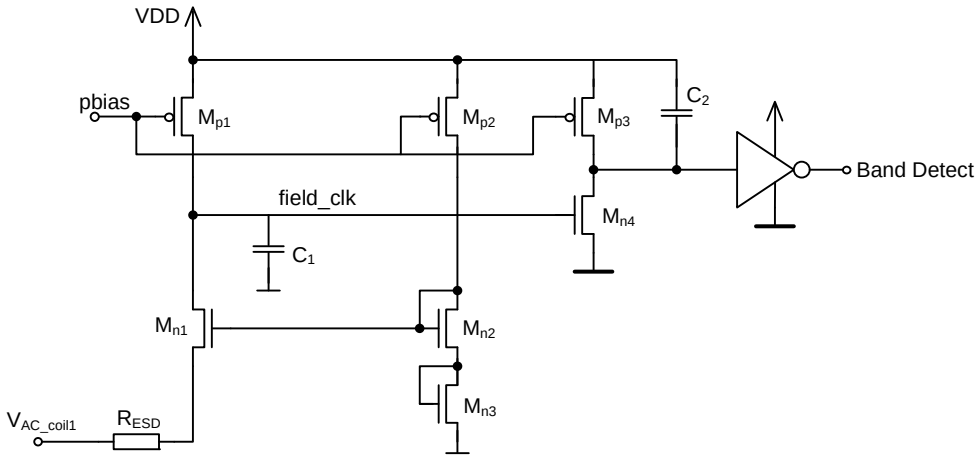


Figure 5.4: Frequency band detection unit

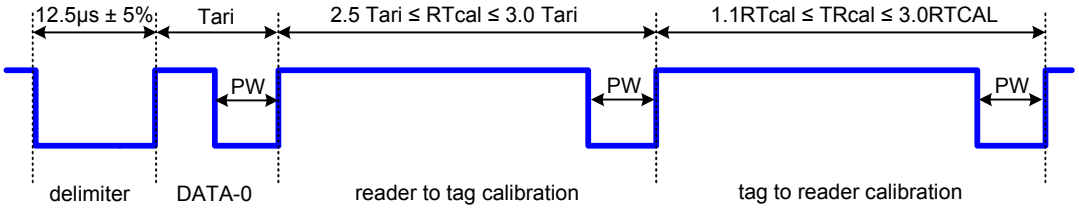


Figure 5.5: Reader to tag preamble is part of the EPC specification [EPC07a]

ber has to be transfered between reader and tag, the lowest specified data rate can be chosen for this event. In this case, the internal oscillator frequency can be reduced adaptively to some hundred kHz. For the CTS power path architecture a clock reduction is not feasible. The DC/DC charge pump power strength is proportional to the clock frequency. An oscillator frequency that is too low would end in a power-down reset.
The following electrical parameters specify the internal oscillator according to EPC Class-1 Generation-2 UHF version 1.2.0 and according to the necessity of getting a low power, low voltage CTS clock source:

- $fosc_{min} = 1.92MHz$
- $\Delta fosc_{extendTemp} = \pm 4\%$
- $\Delta fosc_{duringTxD} = \pm 2.5\%$
- $Pload_{typ} = 600nW$
- $VDD = 600mV \ldots 1.6V$
- $I_{bias} = 100nA \pm 30\%$

A simple beta-multiplier circuit is used as bias current reference [Bak07] with a typical technology and temperature variation of $\pm 30\%$. The very fast startup and the small power consumption are

the reasons to use this unprecise current reference. This implies that the oscillator cannot rely on a precise current.

5.3.1 Oscillator Frequency Drift

As the oscillator is used for the DC/DC charge pump and digital state machine, the term jitter is more often used in the following section than the term ”phase noise” which is often used in analog RF aspects where spectral purity is required. In signal analysis applications a low noise floor is essential for a good data transfer performance. Clock Jitter in a sampled system (ADC) can be converted quite easily into a corresponding phase noise and has an impact for example on the resulting ENOBs, for example. In RFID there has been no need for accurate signal analysis so far. 100% or even 10% ASK in an absolute amplitude change from few hundred mV up to few volt does not need a precise and power hungry RxD unit. In RFID (up to now) it has not been necessary to care about noise floor in the region of a few mV generated by an unstable clock. Neither specific signal analysis nor sampling is necessary. Nevertheless, if short term jitter in such simple systems causes an increased data error rate even at low power oscillators up to a few ns, the problem typically is located in an unfavorable state machine implementation and not in an oscillator weakness. In passive RFID, the clock jitter only has an impact when the synchronization between analog and digital domain has to be precise. There are two different types of jitter:

- Cycle to Cycle Jitter (short term jitter)
  A relative clock perturbation during each successive period is defined as cycle-to-cycle jitter. This jitter definition is well defined and can be easily measured with a with a modern oscilloscope in the time domain.

  $$J_{CC} = T_{n+1} - T_n \tag{5.1}$$

  When many periods are measured, a statistical preparation of equation 5.1 typically shows a Gaussian frequency distribution. In the EPC timing guidelines only accumulated periods of min. 20 periods or more are specified (e.g. the TAG response time T_1).

- long term frequency drift (accumulated jitter)
  A challenge for the long term frequency stability of a local oscillator are accurate protocol timing constraints. In EPC Gen2 UHF at the beginning of each RxD calibration phase, bits RTcal and TRcal are indicate the bit-length and the backscatter data rate. For these timing requirements which consist of over hundreds of clock cycles, long term requirements for an oscillator are important. It is not only the noise-related jitter but also the power supply rejection (influence from VDD), the influence of the bias current and even a temperature change during the period of interest. A passive RFID TAG will never have a stable power supply especially not during the RxD and TxD phase. These critical sections will prove the robustness of the oscillator concept.

5.3.2 Oscillator architectures

Several low-power local oscillator architectures are presented in literature but their electrical performance according low-power RFID requirements is typically not elaborated. Therefore, several

local oscillator architectures are presented and finally compared with the newly proposed CTS oscillator.

Which electrical parameter could vary during a typical contactless operation?
Obviously, internal electrical parameters like power supply voltage and bias current can change dynamically and are the most critical parameters. Some hundred mV of voltage change in 1µs could occur. A special serial regulator with an attached reservoir capacitor would be necessary but it would increase power consumption and especially silicon area dramatically. Silicon temperature would change more slowly over seconds compared to the internal voltage but it could be a temperature step-up during active mode of about 60℃ in strong magnetic field-strength when the reader is switched on. Nevertheless, the most critical communication section takes up to probably some ms and results in a constant oscillator frequency during RxD and TxD. So the focus lies on finding an architecture with good PSRR (against voltage and current) which causes a low jitter [PP03] and a reduced frequency dependency versus power supply voltage changes [McN94] [JK04]. **CMOS inverter ring oscillator**

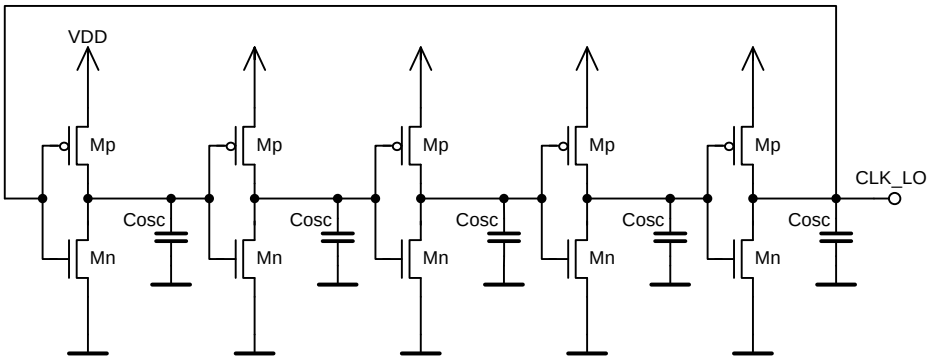


Figure 5.6: Ring oscillator with weak inverter-stages

The nominal ring oscillator frequency can be specified as:

$$f_{osc} = \frac{1}{n \cdot (t_{PHL} + t_{PLH})} = \frac{1}{n \cdot 0.7 \cdot (R_{Mn} + R_{Mp}) \cdot C_{tot}} \tag{5.2}$$

with

$$C_{tot} = C_{outMp} + C_{outMn} + \frac{3}{2} \cdot (C_{inMp} + C_{inMn}) \tag{5.3}$$

t_{PHL} and t_{PLH} are the intrinsic delays of an CMOS inverter [Bak07]. It is the time delay of an ideal rail to rail input-edge transition until the response appears at the output of the inverter. At the output of each stage a node voltage of VDD/2 has to be reached to motivate the toggling of the following inverter stage. The power consumption can be separated into dynamic inverter cross current through NMOS and PMOS and charge transfer current to integrate oxide and junction capacitor potentials.

$$P_{dyn} = n \cdot \frac{1}{t2 - t1} \int_{t1}^{t2} u(t) \cdot i(t)\, dt \tag{5.4}$$

$$P_{charge} = \frac{n}{2} \cdot f_{osc} \cdot VDD^2 \cdot C_{tot} \tag{5.5}$$

During one period the dynamic current occurs twice, charge transfer from VDD to VSS only once (from the source to the sink). The two time boundaries t_1 and t_2 represent the start and stop inverter crossing current time. An assumption from [PP03] specifies the dynamic power portion with about 15% of the total power consumption. In case of a low-frequency and low-power oscillator, the inverter-stages are weak (big transistor length) and the number of stages is small (n=5,7,..). Because of slowly switching inverter stages, the dynamic power may get more dominant. Then, the oscillator frequency with inverter stages may be too high and additional capacitors at each stage may increase P_{charge} again.

RC oscillator

All following oscillator architectures have a better PSRR than the previously explained ring oscillator. The RC oscillator inverter core shown in figure 5.7 is similar to the ring oscillator. Once again, a resistor ($r_{DS} + R_1$) charges a capacitor ($C_{OX} + C_1$). To reduce the dominance of the

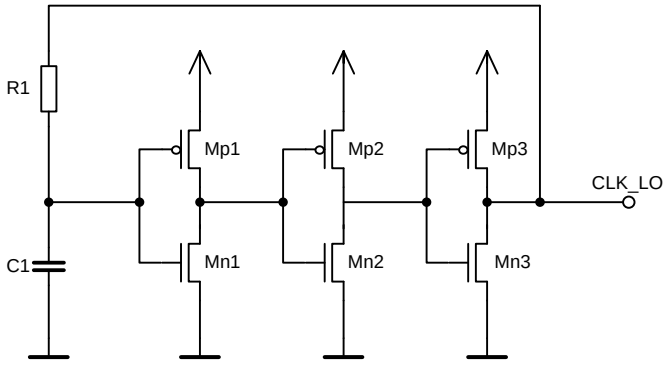


Figure 5.7: RC-time defined oscillator with inverter as amplifier

power supply potential, the resistor R_1 should be significantly higher than the transistor dynamic output resistor $R_1 > r_{DS}$ of transistor Mp3. The same approach is valid for the capacitor. An increased length in the inverter stages is not necessary anymore to reduce the frequency.

CCO - Current Controlled Oscillator

By using a current sink or current source, the oscillator is somehow decoupled from the power supply. Each of the following architectures include current sources and capacitors which are charged by these currents.

$$\Delta U = \frac{I \cdot \Delta t}{C} = \frac{\Delta Q}{C} \tag{5.6}$$

If the sensitivity and the intrinsic receiver delay (comparator or next inverter stage) is known, the period time Δt can be determined. Obviously, equation 5.6 is simplified and does not consider channel length modulation or nonlinear transistor input capacitance. In figure 5.8 and 5.9, the amplifier stages are inverters and differential amplifiers. The differential signal approach of each differential stage also reduces the impact on short term jitter. Figure 5.8 shows the most commonly used local oscillator architecture in passive RFID chips. With two current sources connected to an inverter, the oscillation frequency is independent from VDD but it is linearly proportional to the bias current. Parasitic capacitors at the sources of the inverters deliver additional charge in parallel with the current source and are an additional problem. Typically, the transient

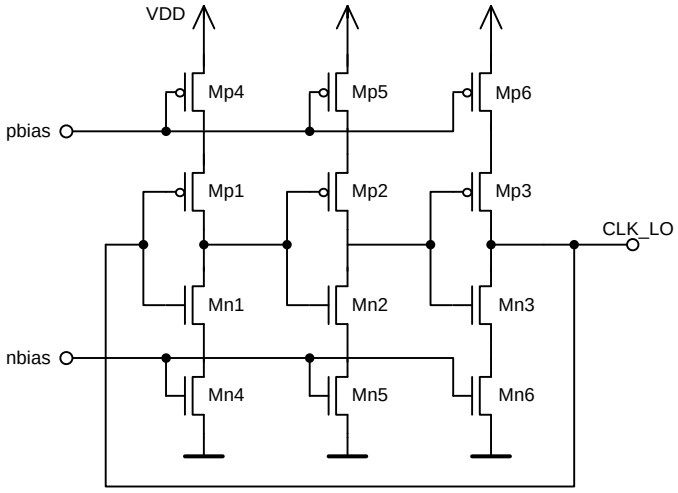


Figure 5.8: Current Controlled Oscillator (CCO)

switching operation points of balanced inverters are around the VDD/2 voltage level. The conversion from the ”analog” oscillator core signal to a digital signal, however, is critical. With this converter it is once again easy to get a VDD dependency into the oscillator frequency. An alternative architecture is an inverter in serial to only one current sink. A PMOS is typically used as current source to be resistive against VDD noise. In this case, a simple transistor current-comparator could be a reliable converter into the digital domain. Nevertheless, the problem with the additional charge and the proportional bias current dependency still exists.

Differential stage oscillator

Differential stages are often used as precise LC-oscillators, cross-coupled switches or as analog inverters. Each single amplifier stage oscillates with a small sinusoidal amplitude around the DC

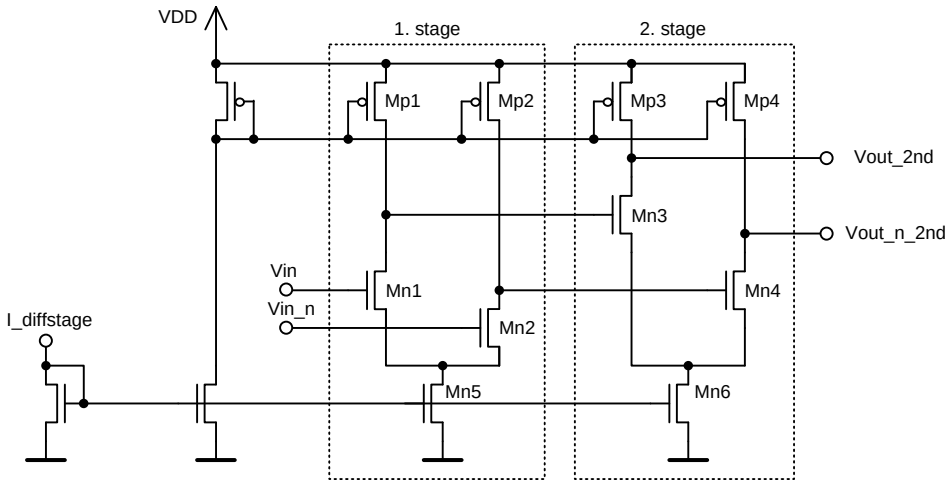


Figure 5.9: Two units of an oscillator with differential stages

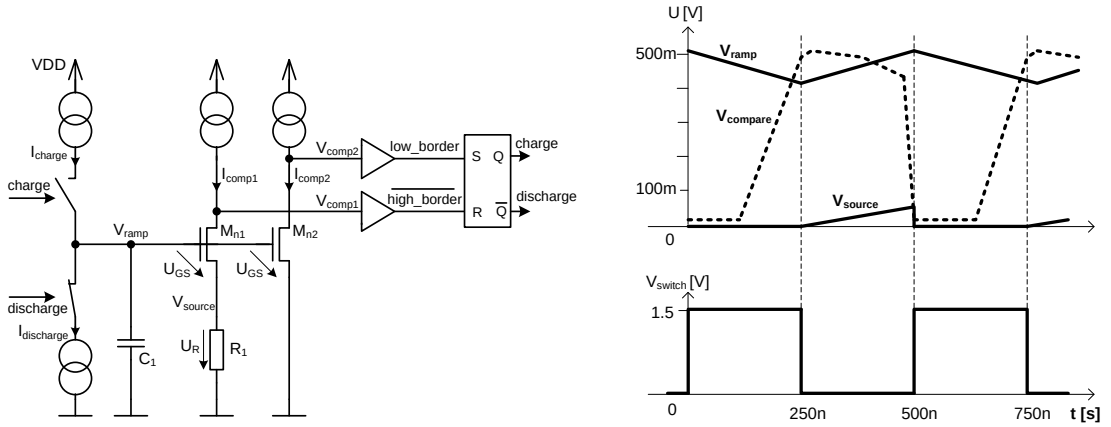
operation point. In figure 5.9 two differential stages are shown. The influence of parasitic capacitors is negligible.
A disadvantage of this structure is the increased voltage headroom for proper operation:

$$V_{VDDmin} = V_{DSMp} + V_{GS_Mn} + V_{DSMn} \tag{5.7}$$

In equation 5.7 both drain-to-source voltages should not fall below $2 \cdot 250mV$ to guarantee well saturated current mirrors. All other current mirror architectures only need one saturation voltage and this is a significant advantage to be used as low voltage CTS local oscillator.

5.3.3 CTS Relaxation Oscillator

The linear relation between bias current and the oscillator frequency as well as the partially bad PSRR of the previous architectures have been reason enough to start with the CTS oscillator design. Figure 5.10(a) shows the architecture of the relaxation oscillator. One switched current source/sink path charges/discharges a capacitor at node V_{ramp} alternately. According to the gate potential of transistor M_{n1} the source potential V_{source} will follow the triangular wave shape amplitude V_{ramp}. Current I_{R1} through the linear poly resistor R_1 will also increase with a triangular shape. In combination with the constant current I_{comp1}, this source follower represents a current comparator. In this stage the conversion into the digital domain already takes place. In the simplified schematic of figure 5.10(a) two current comparators are shown, one for the detection of the upper current limit and one for the detection of the lower current limit. Finally only two constant current paths and a weak inverter are necessary for the core of this oscillator architecture. In



(a) CTS oscillator architecture

(b) Simplified Timing of major nodes

Figure 5.10: Optional caption for list of figures

figure 5.10(b) the triangular V_{ramp} voltage starts at about 550mV. In this case the current sink is activated, the voltage Vramp drops and the current through transistor M_{n2} drops, too. As soon as the threshold voltage of transistor M_{n2} is reached, I_{comp2} will be quickly bigger and the voltage Vcomp2 toggles. Then, the input stage also toggles and the current source is switched on. Now the charge at C_1 ramps up until the current through R_1 is bigger than I_{comp1}. In this case, the potential at this current comparator $V_{compare}$ drops closely to VSS and the output state potential $high\_boarder$ will indicate that the upper boarder is reached. Finally the input stage toggles

again and the requirements for an oscillation are achieved.
To reduce power consumption, the functionality of two current comparator units can be summarized in one path. By shorting the resistor R_1 at the right time, the non-resistive current path I_{comp2} can be emulated with a switch in parallel to R1.

Figure 5.11 shows the CTS oscillator implemented on transistor level with only one current comparator path. Transistor M_{n4} represents the switch which is responsible for the reduction to one

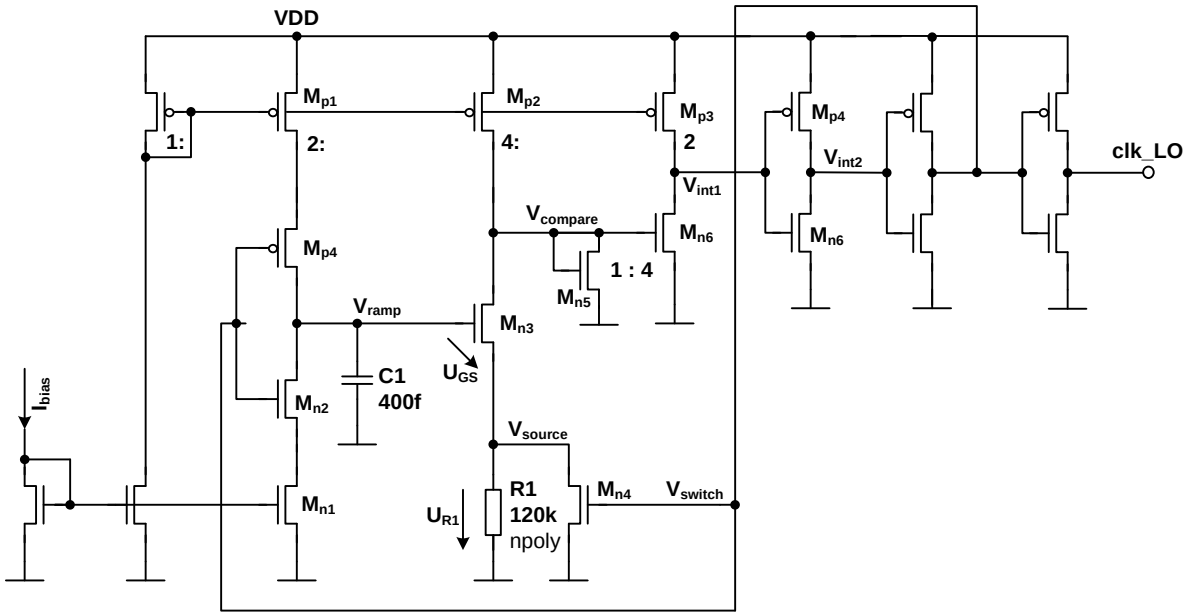


Figure 5.11: New CTS relaxation oscillator

signal path. In the low ohmic condition of switch M_{n4}, the NMOS current sink M_{n1} is active and the gate voltage of M_{n3} is reduced close to the threshold voltage. Current comparator M_{n6} and M_{p3} toggle and the switch gate potential $Vswitch$ changes to LOW potential. Switch M_{n4} does not conduct any more and the upper switching limit is defined when the currents through resistor R1 and transistor Mp2 are equal.

$$I_{R1} = \frac{U_{R1}}{R_1} = I_{Mp2} \tag{5.8}$$

$$\Delta V_{ramp} = \frac{I_{Mp1/Mn1} \cdot t}{C_1} \tag{5.9}$$

$$t = \frac{I_{Mp1/Mn1} n R_1 C_1}{I_{Mp1/Mn1}} = n R_1 C_1 = \frac{T}{2} \tag{5.10}$$

Equation 5.10 shows the oscillator period T independence towards power supply voltage and bias current variations. Current mirror ratio of M_{p1} and M_{p2} is considered with the factor n. If an accurate frequency is necessary, capacitors in parallel to C_1 could adjust the center frequency during the product test.

5.3.4 Performance comparison of different oscillator architectures

After the architecture introduction it is time to compare some electrical performance parameters. Power supply voltage and bias current variations are the two parameters with the best transient dynamics during the RxD and TxD phase. Both quantities fall by about 30% during field energy gaps and increase by 10% because of regulator ringing after the end of field gaps (step response). Compared to VDD and bias current variations, the temperature varies rather slowly. Therfore, the temperature can be neglected in the calibration phase before contactless communication. Nevertheless, in the temperature corner with the lowest oscillator frequency, the minimum frequency has to be higher than 1.92MHz. A curve with a steep change in temperature to frequency characteristic would cause a much higher oscillator frequency in the other temperature corner, which would also cause a proportionally increased power consumption.

VDD power supply variation

Figure 5.12 shows the frequency dependency compared to power supply changes. The worst

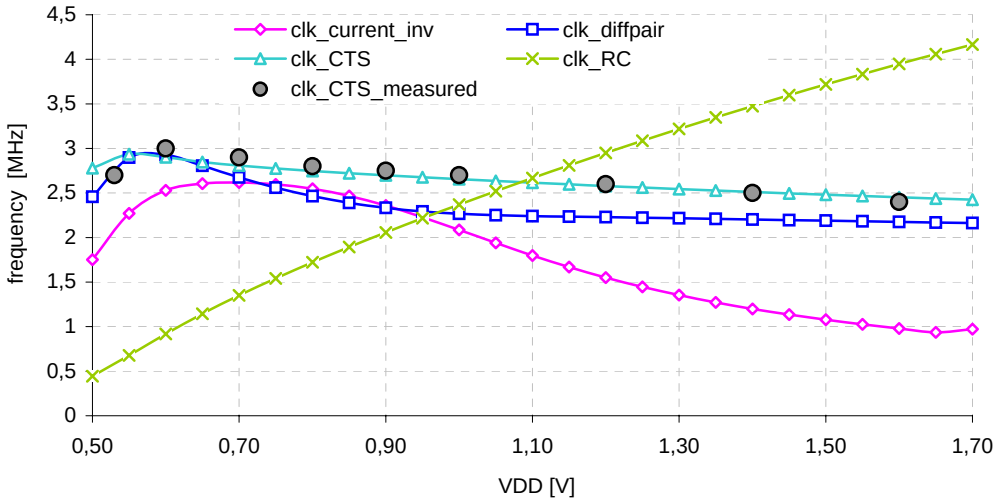


Figure 5.12: Power supply variation

PSRR performance is shown by the RC oscillator (clk_RC). Under low voltage conditions the dynamic output resistor r_{DS} can reach the resistor value of R1 in the RC-unit. A more powerful output driver stage would reduce the gradient of the actual characteristic to a more linear curve, but it still would not satisfy the requirements. An inverter with an attached current source/sink $(clk\_current\_inv)$, by contrast, shows a smoother trend.
Best PSRR results shows the differential pair $(clk\_diffpair)$ and the CTS oscillator (clk_CTS). With some measures it certainly will be possible to improve the performance of the differential pair until the CTS oscillator performance is reached. The slightly falling slope of the CTS oscillator at power supply voltages higher than 0.6V results from the second stage M_{n7} and M_{p4} in the current comparator. Transistor channel length modulation increases the current through the current comparator path of M_{p3} current sources but it cannot compensate the increased VDD/2 level of the following inverter stage. A solution to this problem could be a steeper slope

by increasing the M_{p3} source current but this would also increase parasitic capacitances and module power consumption of this oscillator. Below 0.6V power supply voltage the voltage headroom in all current sourced paths is too low. None of them is saturated well and the according charge time of parasitic capacitors gets more dominant. CTS architecture measurement results $(clk\_CTS\_measured)$ fit well compared to simulation results performed with parasitic back-annotated spice netlists.

Bias current variation

Power supply variation also changes the bias current moderately too. By using a beta multiplier circuit [Bak07], a bias generator architecture with good PSRR is already chosen. Because of the still finite PSSR and a U/I bias current characteristic dependency, the generated current changes during the operation. The correlation between oscillator frequency and bias current for various architectures is shown in figure 5.13. Only the CTS oscillator has no linear characteristic of a

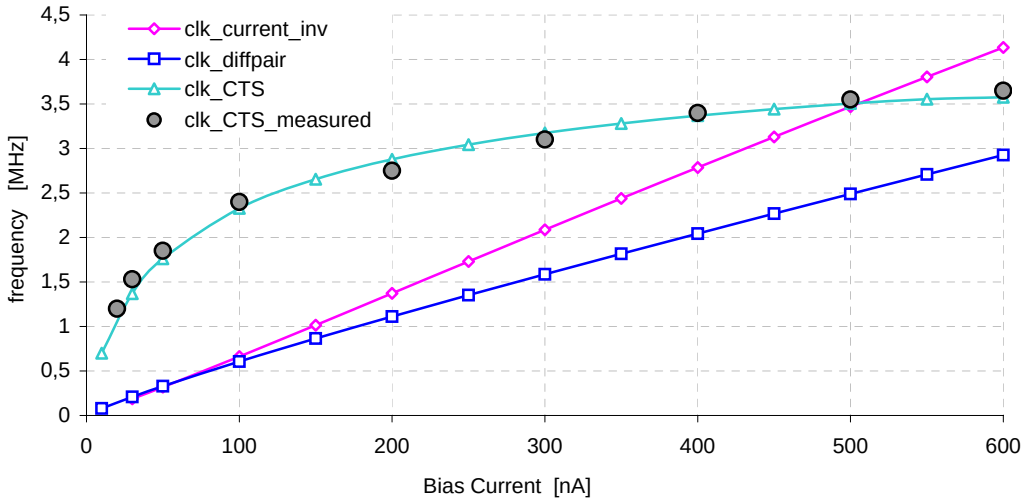


Figure 5.13: Bias current sweep

typical ”current charge a capacitor” behavior. Currents below 100nA lead to a rapid frequency reduction triggered by parasitic capacitors in the CTS current comparator path. For the product a bias current of 110nA was chosen. A bigger transistor current shows a smaller bias current dependency but the overall power consumption of the CTS oscillator would get higher.

Temperature variation

In graph 5.14 the temperature behavior over a wide range is presented. The typical consumer electronic temperature range reaches from 0°C to 70°C. The poly resistor temperature dependency has the greatest influence on frequency in the CTS architecture. In plot 5.14, the curve characteristic $clk\_CTS\_R\_poly$ shows the temperature dependency implemented with a poly resistor. Two poly resistors with different doping dose are used in graph $clk\_CTS\_R\_compens$ to compensate the temperature response of the resistor value. To verify the temperature compensation an ideal resistor without any temperature coefficient was used in graph clk_out_RC. It shows the same curve steepness compared to the two poly version but with an offset because of the missing parasitic capacitance to substrate. To get a plain frequency curve, several additional

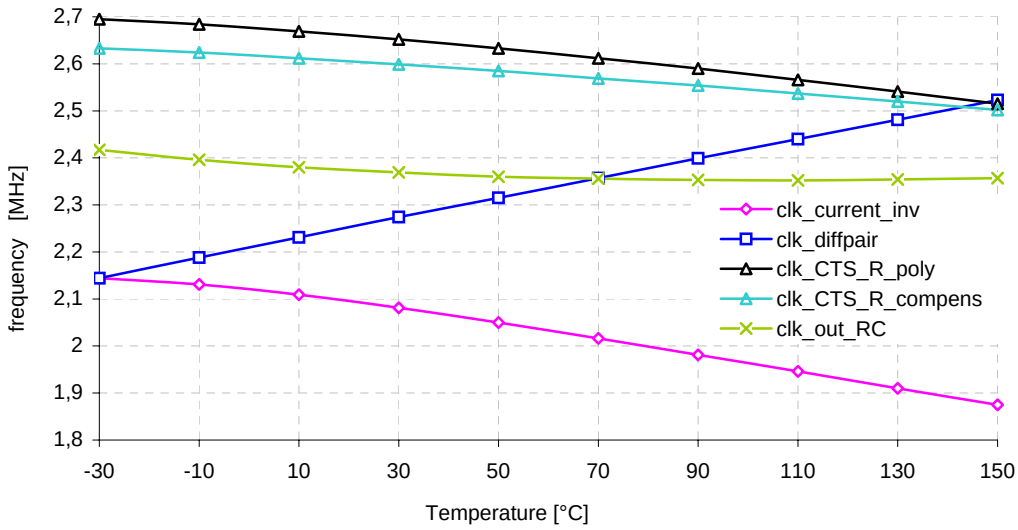


Figure 5.14: Temperature sweep

measures would be necessary which depends on technology related parameters. As technical parameters vary a lot over the production cycle, all design measures - including the matching of different doped resistors - are not effective to guarantee a tight frequency tolerance. All simulation setups were done with ideal temperature independent current and voltage sources.

5.3.5 Power Supply Rejection

In this section, two structures, namely - the ring oscillator of figure 5.6 and the CTS relaxation oscillator concept, will be compared regarding their robustness against power supply variation. From EPC global specification we get an allowed local oscillator frequency drift during the very dynamic backscatter phase of ±2.5% frequency variation which is the most challenging specified number. During the backscatter phase the DC power supply voltage variation can be 30% or 500mV when a modern process is used. This modulates the frequency of a ring oscillator almost linearly and it causes a frequency error equivalent of 30%.

Because capacitor C_{osc} is big compared to transistor capacitance C_{out_Mp}, the small signal behavioral model of the ring oscillator shown in figure 5.16 is equivalent to a first order low-pass filter. Figure 5.15 represents a simplified output stage, the following input stage and the frequency determinative charge reservoir capacitor Cosc which is responsible for reducing the center frequency. In addition to the reservoir capacitance the dynamic output resistor r_{DS} of the NMOS and PMOS inverter transistors gets a lower value when the power supply voltage VDD rises.

The CTS oscillator AC small-signal circuit is shown in figure 5.16. In comparison to the ring oscillator, it has highly resistive r_{DS} current sources. At low frequency conditions the parallel transistor capacitors impedance is low and the sensitive node 'CTS oscillator' is not affected by power supply variation and small signal noise. In the layout floorplan parasitics between VDD and this sensitive node should also be avoided and determined for simulation. Figure 5.17 shows the two

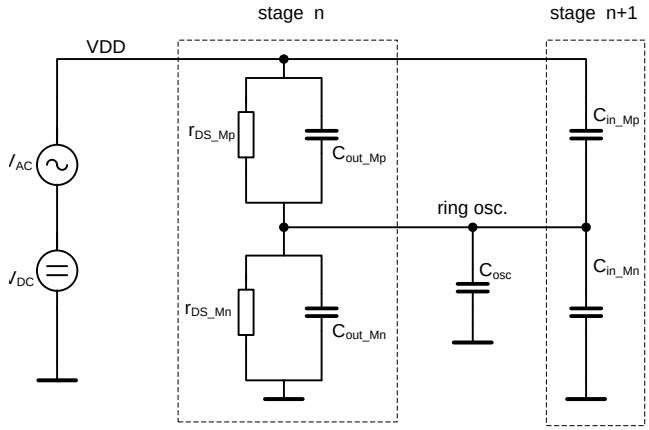


Figure 5.15: AC circuit of one ring oscillator stage

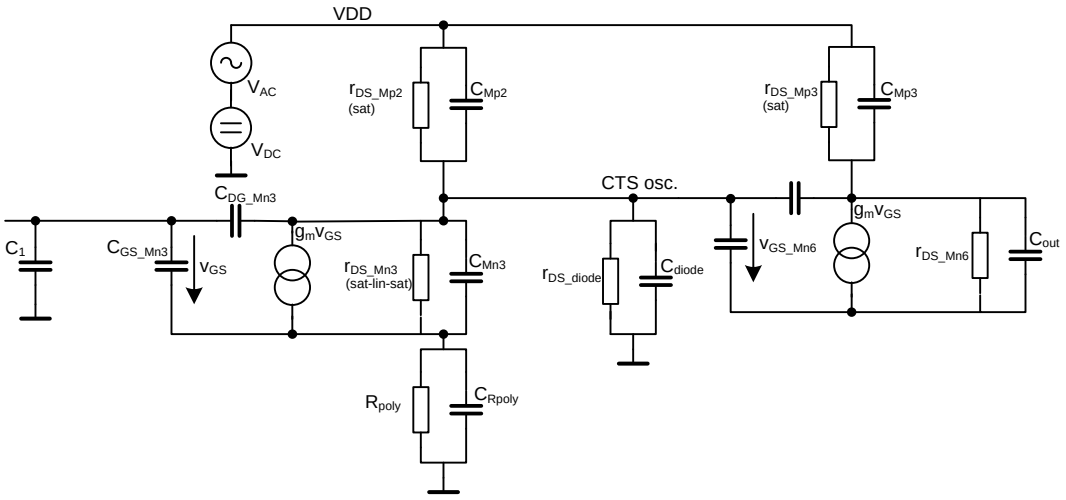


Figure 5.16: AC circuit CTS oscillator core

before presented AC small signal cores simulated with typical transistor dimension.

Taking the RFID typical big power supply voltage changes at low frequency conditions into account, the favorite is clearly the CTS oscillator architecture, even if the ring oscillator architecture archives better results regarding high frequency noise $(> 1MHz)$. As low frequency power supply voltage changes of several hundred mV are typical for RFID chips but high frequency noise is limited to some mV, the ring oscillator will not be taken.

Clock source selection
According to the information from the frequency band detect unit, one of the two clock sources is selected (local oscillator or clock recovery). Immediately after chip start-up, the band select signal switches to the right signal. It could happen that a glitch occurs at the signal clk_chip

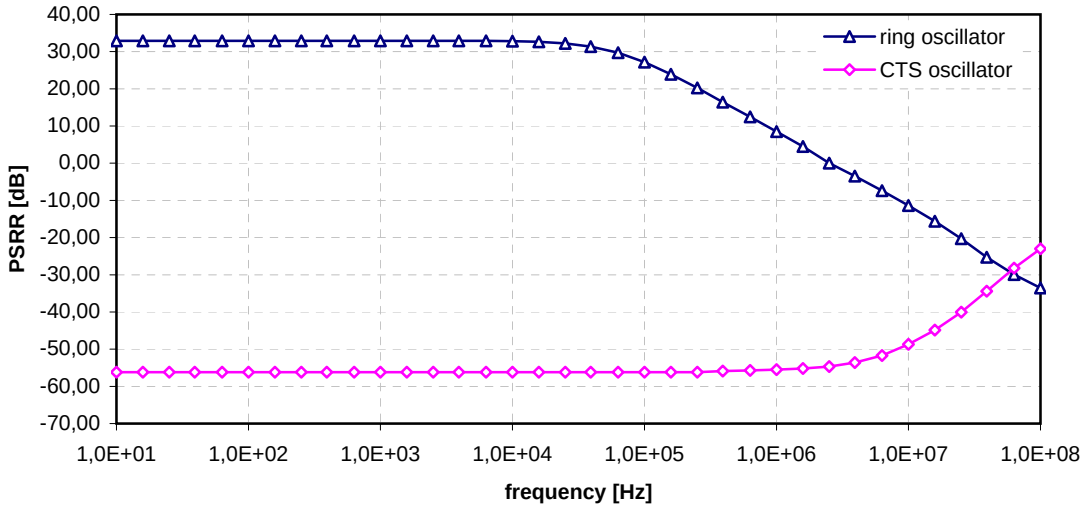


Figure 5.17: PSRR Comparison between ring and CTS oscillator

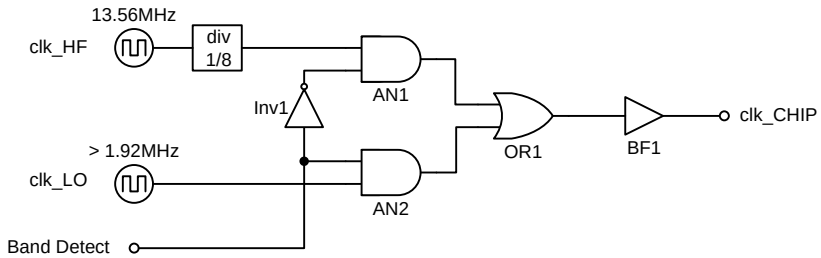


Figure 5.18: Generation of two clock sources the master clock of the chip

because of asynchronous switching, which could disturb the digital state machine. To avoid this, the reset signal is always released a few μs after the band switching at the very early start-up. If during UHF operation the HF field-strength gets stronger the frequency band detection unit possibly toggles its state. The CTS chip then will restarts and afterwards operates in the HF operation mode.

5.4 Layout of the local oscillator

The two passive components R1 and C1 which are responsible for the definition of the oscillator-period, are the biggest components in the CTS oscillator module. The PMOS transistors switched

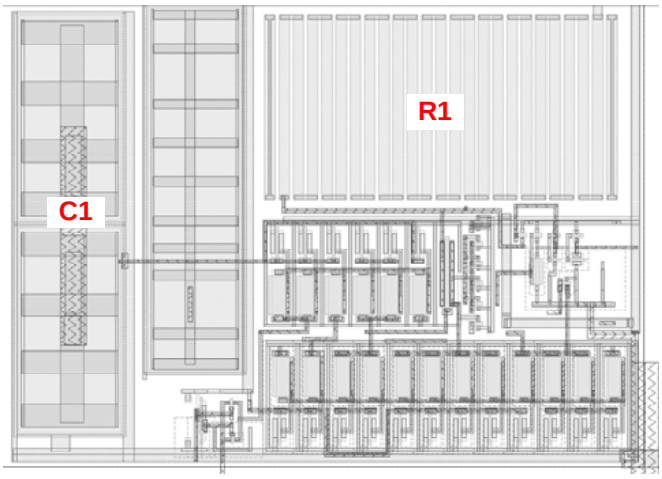


Figure 5.19: Layout of the CTS oscillator

as current mirror transistors dominate the active region. The total area of this module is about $0.002m^2$.

6 Contactless Communication Units

The communication between reader and transponder is based on transponder impedance manipulation (TxD) or on field-strength or emitted power variation (ASK - RxD). After a short introduction into communication relevant EPC specifications, new TxD and RxD design architectures will be presented in this chapter.

6.1 Waveform Requirements for HF and UHF

- Downlink - RxD
  Communication from the reader to the transponder is called downlink or RxD (from tag's view). Modulation type is ASK with different modulation levels (modulation index) specified. Pulse interval encoding is used in both frequency bands. In figure 6.1, a coding scheme

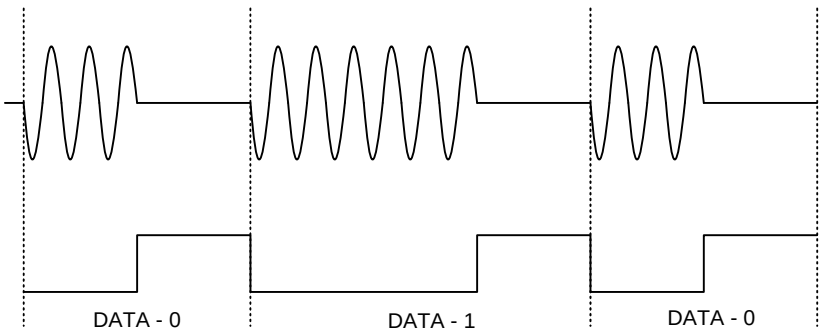


Figure 6.1: Pulse interval coding and ASK with 18% down to 100% modulation depth are used for RxD

with a much too low carrier frequency is shown compared to the information length of one bit. In this figure, the tag gets the data information from the reader with a big dynamic in form of a carrier ON/OFF information (electric or magnetic field changes). That is good, because a RxD module in the chip with low complexity consumes 500nW or even less. In the latest EPCglobal HF standard [EPC07b] the field modulation index varies from 10% to 30%. If a UHF field is applied [EPC07a], the information is forwarded via a modulation depth reaching from 80% down to 100%. Because of the big signal dynamic and the clear information, only few transistors are necessary for the UHF demodulator design. A few more transistors - one integrator and two comparators - are necessary for a HF ASK demodulator. The gap-time can vary from 2µs up to 13.1µs. Anywhow, a precondition for a stable and error-free communication for both demodulators is a "linear" voltage limiter. The voltage swing at the chip input terminals should be proportional to the magnetic field-strength or proportional to the incoming power variations when electro-magnetic waves are

	HF Gen2	UHF Gen2
Physical bearing	Load Modulation	Backscatter
Subcarrier modulation	Manchester/Miller-Modulation	Miller
Data coding	Manchester/FM0/Miller-Modulation	FM0/Miller Modulation
Communication link	Half-duplex (synch.)	Half-duplex(asynch.)

Table 6.1: EPC specification for TxD

received.
At the beginning of the RxD communication phase a preamble defines the duration of one bit. With this information the reader defines the bitrate and the chip measures the number of clock cycles which are required for one bit with the help of the internal oscillator shown in figure 5.5. This pulse-width measuring by the demodulator should be accurate and reliable during the whole RxD cycle.

- Uplink - TxD
  Load modulation or backscatter modulation is performed when data is transfered form the tag to the reader. In the TxD phase more different coding methods are defined for both RFID frequency bands. To get an overview of the communication methods, table 7.1 shows some crucial issues for both EPCglobal Gen2 specifications. The uplink frequency is selected during the $QueryCommand$ and reaches from 53kBit/s up to 848kBit/s.
  In spite of these differences, in table 7.1 the electrical design of the TxD power module is the same for both frequency bands but the regulation circuit for this power module varies. During the backscatter phase the modulator transistor switches the reflection coefficient from a nominal load condition to a resistive short - in the ideal case a total reflection is the result. Close to the reader the nominal chip impedance is close to a short anyway and causes only a slight change in the reflection coefficient. According to the small power loss in the free space when the distance is short, a small change in the reflexion coefficient causes a signal dynamic in the reader receiver unit which is big enough to be detected. 2- and 3-bit sequences FM0 / Miller coded are shown in figure 6.2. In the CTS project the shunt and modulator power transistor are combined in the same device. No synchronization between the two modules is necessary in the configuration any more, but a fast and precise regulation of this power transistor is demanded, especially in HF mode.

- Voltage limiter - Shunt
  Both communication modules and the voltage limiter (shunt) have to be aligned for a reliable contactless operation. During the RxD phase the shunt impedance has to behave like a constant linear resistor. The regulation loop should be frozen in a state before the contactless reception starts. As the chip does not know when the first or next command from the reader will appear, this ”stop before start of RxD” will never work. The workaround is to reduce the regulation speed - the speed of changing the antenna voltage - of the shunt loop down to a very low speed compared to normal operation. Then the voltage limiter is not able anymore to react fast enough to field-changes. This is good when the magnetic/electric field drops but it is bad when the field intensity rises fast. The answer for the CTS project lies in a simple speed adaptive regulation loop for the shunt.

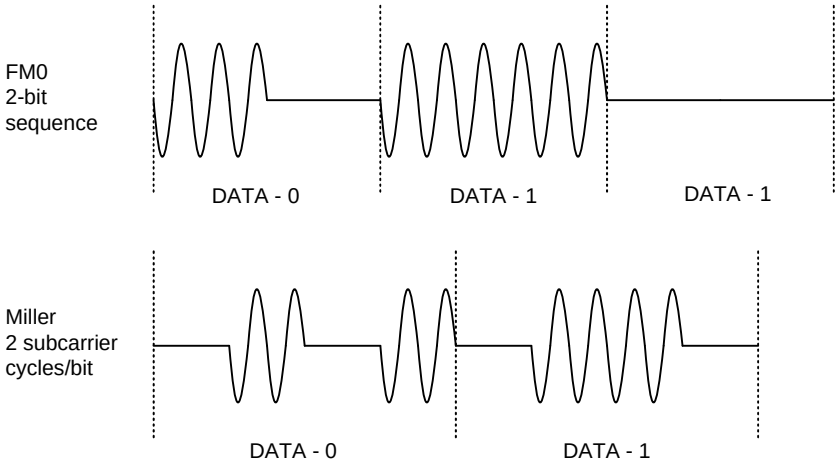


Figure 6.2: Uplink - Two examples of operation

During the TxD phase the generated envelope voltage wave-shape preferably should be rectangular. With a rectangular waveform the resulting sideband gets maximized [Kla09] when a constant modulation depth and different modulation waveforms are compared. In the order to ensure having a very steep rising edge after load modulation, a very fast shunt regulation loop is necessary. Finally, the CTS shunt regulator concept is a compromise between power consumption and the risk of an unstable loop.

For determining the envelope waveform during RxD and TxD, not only the voltage limiter behavior is relevant, but also the bearing of the air interface. Transponder resonance frequency, antenna to chip impedance matching, geometrical data of the coil/antenna, magnetic/electric field-strength and the carrier envelope reader signal tolerance are some additional facts a RFID chip developer has to care about.
In general, during the design phase a matrix of possible influences among different modules or of the air interface has to be defined and especially executed during the pre-silicon verification before tape-out.

6.2 Voltage Limiter

A constant resistor as voltage limiter would reduce the maximum distance or the minimum field-strength for operation extremely. The limiter resistance has to be designed for the maximum field strength or maximum power applied to the chip during the HF or UHF phase. In this high power condition the peak voltage should be smaller than the (short time) technology limit for transistors used in the analog front end in the interface region. The final communication and power range of this tag with constant resistor value will be only 20% or even less of a passive RFID chip interface compared with an intelligent shunt design.

A typical shunt implementation is shown in figure 6.4 for UHF and HF applications. Cross-coupled NMOS transistors for defining the VSS potential are usually a for HF rectifier design. With this structure, no AC coupling with capacitors is necessary and the voltage drop via the

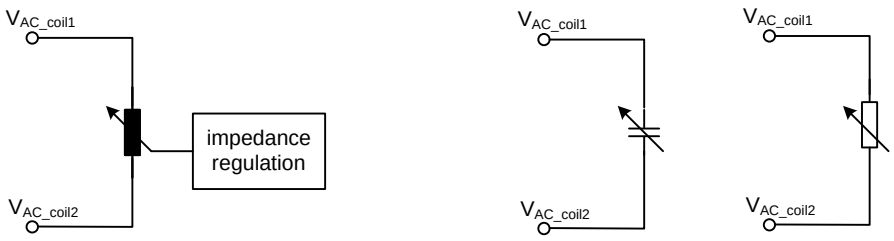


Figure 6.3: Impedance control by a regulation loop. Could be either capacitive detuning or resistive load change

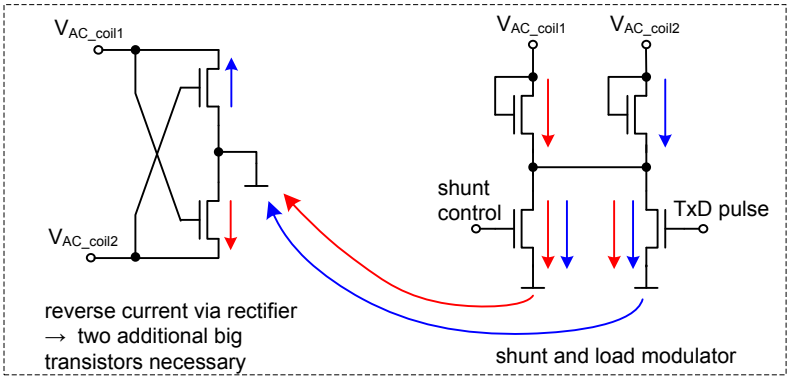


Figure 6.4: A common shunt/load-modulator structure of a HF TAG

NMOS transistors is small. But if the shunt is located ”behind” these transistors, the current from VSS to the coil/antenna terminals increases by a factor bigger than 200 and the width of them will increases, too. As these transistors in the rectifier are also very important for ESD protection, the minimum finger width has a certain limit anyway. This also causes a minimum width when only a small current has to be transported via these transistors and it reduces the tremendous factor 200 down to about 10 times the transistor width which is necessary for a correct electrical operation. Gate voltage node $shunt\_control$ regulates the current through the shunt transistor in function of the coil voltage $V_{\text{AC\_coil1/2}}$. During TxD the current through the shunt transistor and additionally the modulator current is directed back to the coil pads via VSS and the NMOS rectifier transistors. In the CTS project small junction areas are necessary for a good UHF performance and going to provoke a new voltage limiter concept.

Unbalanced rectifier structures are common for UHF front end designs. Only one ”hot” node instead of two signal nodes are used. Several concepts to implement a shunt for UHF are shown in figure 6.5.

- Capacitive detuning
  With a nominal chip input capacitance of 300fF up to 1pF for typical UHF devices, a capacitive tuning circuit could be realized with small additional parallel capacitors. A varactor could be used as regulated capacitor to control the antenna voltage [KF03]. If this concept

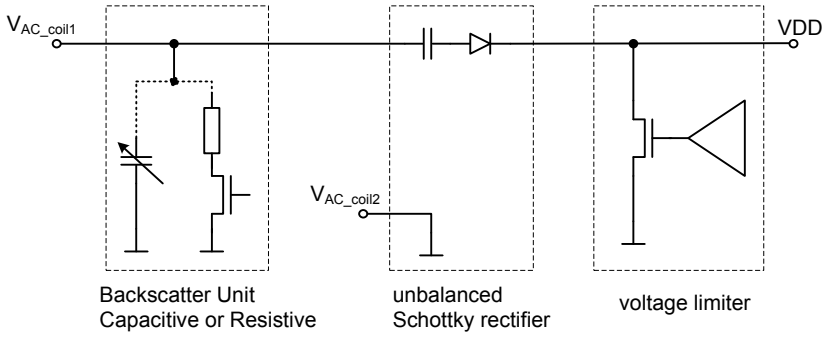


Figure 6.5: In UHF the shunt is situated behind the rectifier/charge pump. The TxD module is typically located in front of the rectifier

should also be implemented for a HF RFID chip, the capacitance would be 100pF which is much too big for a UHF chip. The varactor capacitor is much bigger in silicon-area than an active resistive shunt and, therefore, will never be used in commercial products.

- Resistive load
  This would be the typical design concept for a HF voltage limiter, but it is also used for UHF chips. When in the input structure no AC coupling capacitor is used and the Schottky diodes are connected straight to the antenna, a power shunt transistor can be used at the internal VDD node [PHD07] [Zhu04] [ZJC05]. In this case, no additional junction capacitance is generated at the sensitive RF input. Such an approach guarantees a good UHF power performance.
  As already shown in figure 6.4, also a parallel path to VDD could sink the current. Additional area and junction capacitance are the drawbacks of this architecture but VDD power supply disturbance can be easily avoided.

- No protection
  To increase the antenna voltage peak voltage, a RF charge pump is often used in UHF transponders. Usually, AC coupling capacitors are used to transport charge from the antenna pads to the internal charge pump nodes. These capacitors can resist a big voltage difference of e.g. 20V when the isolator is thick enough. Metal-Metal capacitors are scalable according to the prospective antenna peak voltage and they have low capacitive parasitics to the chip substrate. No voltage limiter at the RF pad - not even at high electric field conditions - is required [**?**]. But on the RF input there is still an ESD protection and a module for backscatter necessary. Anyway, this concept is not feasible for HF and, therefore, it is not useful for the CTS chip.

6.3 CTS Voltage Limiter

To fulfill HF and UHF requirements and to still get a good power performance compared to single frequency products, the shunt configuration in figure 6.6 is used for the CTS chip. An NMOS transistor with permanent alternating source/drain terminals and a well regulated DC voltage at

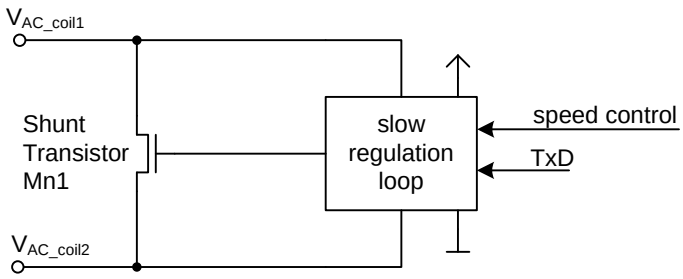


Figure 6.6: CTS chip voltage limiter with one shunt transistor directly between the antenna terminals and a slow regulation loop

the gate node represents the power path of the shunt [Mag89] [Fin06] and [Liu05]. This CTS voltage limiter configuration fulfills all desired features:

- minimized active area: only one transistor between the two coil/antenna terminals
- speed is adjustable: fast/slow/hold regulation speed modes are possible
- constant load behavior (constant shunt impedance)
- shunt transistor can be upgraded for TxD operation
- no AC coupling necessary

Transistor Mn1 is the shunt transistor of the voltage limiter which controls the Q-factor of the resonance circuit by varying its output resistance r_{DS}. The shunt transistor dimension depends on several parameters like maximum gate voltage $U_{GS\_Mn1\_max}$, transponder coil inductance or resonance circuit tuning (the frequency tuning can be done with C_{f_tune}). In figure 6.7, magnetic and

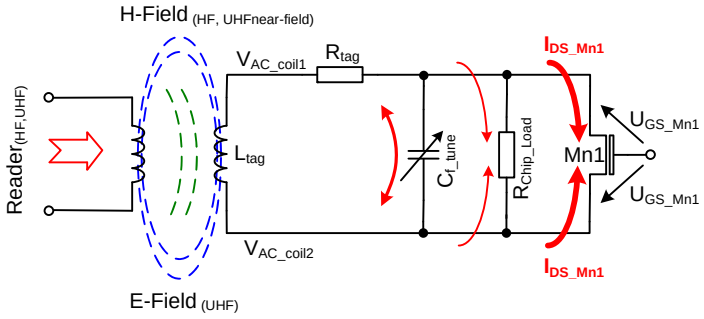


Figure 6.7: Some parameters to determine the shunt transistor dimension

electric coupling is shown. R_{tag} concentrates the resistive parts of a coil/antenna in one resistor. C_{f_tune} is the summarized capacitance of the coil/antenna. Before a shunt current assumption can be started, some contactless communication dominant limitations are summarized in the following table:

Parameter	Value	Dimension
H_{field_max}	10	A/m
L_{TAG_min}	5	µH
R_{TAG_min}	3	Ω
f_{res}	14.5	MHz
$R_{VDDload\_min}$	10	kΩ
$U_{GS\_Mn1\_max}$	3.5	V
$U_{DS\_Mn1\_max}$	5	V

Are 5V V_{DS} really necessary?
For HF load modulation a minimum voltage delta is necessary to deliver enough information to the reader receiver unit - especially at far operation distances. During the feasibility study of the CTS project, the decision was made to support up to $5V_{peak}$ at the coil interface. Transistors with a thick-oxide of 20nm and with an increased drain to source transistor channel length need a bigger transistor area (width) as compensation which generally results in a very poor transistor RF performance. In contrast to HF, a UHF reader usually has a more sensitive RxD unit in order to receive backscatter information from the TAG. Modern UHF reader sensitivity reaches down to -80dBm [NR06a] and shows a dynamic range of about 120dBc.

Current through the shunt transistor
A voltage limiter at the coil/antenna interface is necessary to influence the quality factor of the resonance circuit by drawing a high current through the shunt transistor. Especially in HF, but also in the powerful UHF near-field region, currents of several tenths of mA are possible. As the power consumption of power optimized RFID chips is smaller than 100µA even during power-hungry operations like EEPROM programming, the excessive power has to be transformed into temperature by a device somehow. The following equations will help to get an idea of the current through the limiter structure. Several air interface simplifications result in a handsome formula for both frequency bands.
As we have seen, in RFID a parallel RLC tank can represent the coil or antenna to chip interface. The quality factor Q_P of a RLC network can be represented by:

$$Q_P = \frac{R_{chip}}{\omega_0 \cdot L_{antenna}} = \omega_0 \cdot C_{chip} \cdot R_{chip} \tag{6.1}$$

To reduce the complexity, the numbers of parallel resistors merge into one linear resistor R_{chip}.

$$R_{chip} = R_{shunt} + R_{analog} + R_{digital} + R_{parasitics} \tag{6.2}$$

$$R_{chip} \approx R_{shunt} \tag{6.3}$$

Voltage limiter current I_{shunt} is still valid for the HF and for the UHF frequency bands:

$$I_{shunt} = \frac{U_{IC}}{R_{shunt}} = \frac{U_0 \cdot Q_P}{R_{shunt}} \tag{6.4}$$

Because of the induced voltage U_0, a separation of HF and UHF bands is necessary. In HF the magnetic field and in UHF an electro-magnetic wave generates a voltage in the antenna.

$$U_{0\,HF} = \omega \cdot \mu_0 \cdot A \cdot N \cdot H \tag{6.5}$$

$$U_{0\,UHF} = l_0 \cdot E \tag{6.6}$$

$$I_{shunt\,HF} = \frac{U_{0\,HF} \cdot Q_P}{R_{shunt}} = \frac{U_{0\,HF} \cdot R_{shunt}}{\omega L \cdot R_{shunt}} = \frac{\mu_0 \cdot A \cdot N \cdot H}{L} \tag{6.7}$$

$$I_{shunt\,UHF} = \frac{U_{0\,UHF} \cdot Q_P}{R_{shunt}} = \frac{U_{0\,UHF} \cdot R_{shunt}}{\omega L \cdot R_{shunt}} = \frac{l_0 \cdot E}{\omega L} \tag{6.8}$$

A calculation example should show the prospective current through the shunt in HF mode. The tag inductor could be calculated with [Fin06]

$$L = N^2 \cdot \mu_0 \cdot R \cdot ln\frac{2 \cdot R}{d} \tag{6.9}$$

Varying the number of windings N in equation 6.9, the inductance L changes with the power of two. If the outer dimension is limited, the enclosed area gets smaller with each additional winding and the formula gets more complex. A credit card format is chosen as outer boundary limitation for the coil antenna. The transponder inductance was calculated with the Coil Calculator, which was developed by Infineon and TU Hannover [Kla09] [LGE$^+$07] [LGEL06]. The result was a non-quadratic dependency between N and L.

$$N = 6,\ L = 3.8\mu H,\ C_{TAG\_coil} = 3.7pF,\ A = 0.003m^2 \tag{6.10}$$

$$I_{shunt\,HF\,N\_6} = \frac{4 \cdot \pi \cdot 10^{-7} \cdot 3^{-3} \cdot 6 \cdot 10}{3.8 \cdot 10^{-6}} = 60mA \tag{6.11}$$

$$I_{shunt\,HF\,N\_1} = \frac{4 \cdot \pi \cdot 10^{-7} \cdot 3^{-3} \cdot 1 \cdot 10}{3.8 \cdot 10^{-6}} = 157mA \tag{6.12}$$

The variation of the number of turns N is only one of the parameters that influence the current in the voltage limiter. Concerning also a good UHF performance, the area of the shunt transistor should be as small as possible. In the CTS project a current of 50mA is the absolute upper maximum and is one of the most critical design limitations in the shunt design. This current limitation can still be compared with commercial HF only devices.
A CTS voltage limiter block diagram with the shunt transistor Mn1 is shown in figure 6.8. The module $Shunt\ Regulator\ Unit$ controls the gate of Mn1 addicted to potential $V_{AC\_coil1/2}$. Regulator performance can be adjusted according to the frequency band and the contactless communication state. To adjust the regulation speed capacitor, C1 can be switched to node $shunt\_gate$, which results in a very slow regulation loop. During the TxD phase C1 controls the $shunt\_gate$ potential via AC coupling at the lower potential plate. Reference voltage unit $Vref\ generation$ is powered directly by rectifier diodes from the RF field. This self-starting of the reference voltage and reference bias reduces the state complexity during the startup phase when a contactless field is applied.

Figure 6.9 shows the shunt regulation unit on transistor level in detail. No differential amplifier or even a more complex operational amplifiers is used as regulator module. There is only one transistor Mp3, which is responsible for the current-balancing of node $shunt\_gate$. Let us assume the gate potential of transistor Mp3 is constant and the source potential which is attached to two diodes Mn3 and Mn4 rises because the field-strength also rises. Current I_{DS_Mp3} will also

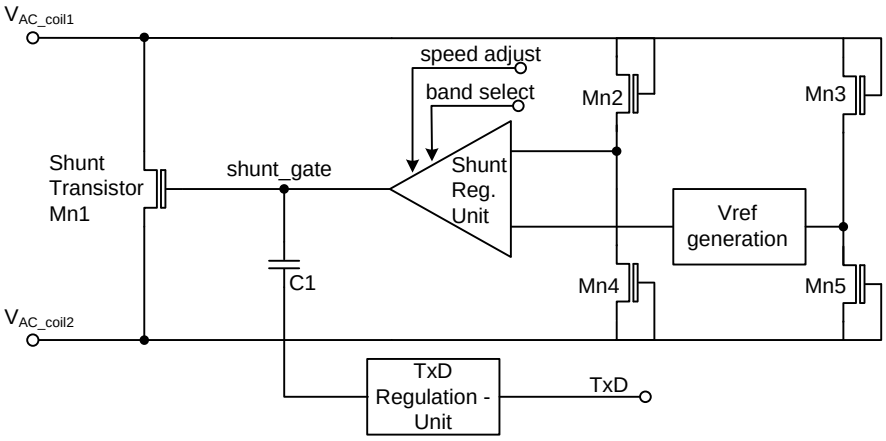


Figure 6.8: More detailed voltage limiter concept with integrated TxD unit

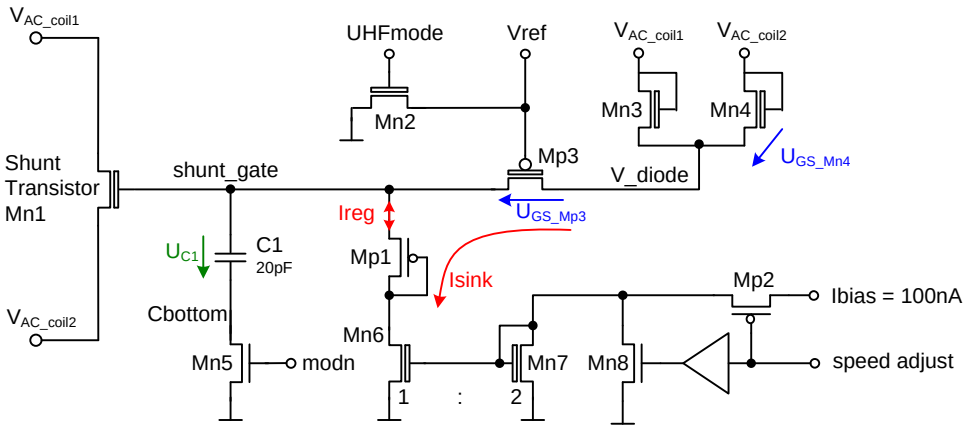


Figure 6.9: Detailed shunt regulation loop

increase according to the g_m of Mp3. A current sink in the drain of Mp3 sinks the current via a diode Mp1 to VSS. When more current is sourced from Mp3, capacitor C1 and the parallel parasitic capacitance are charged and the potential on node $shunt\_gate$ rises. During the charging phase in equation 6.15, the current peak through Mp3 equals the average sink current defined by the current skin transistor Mn6.

$$I_{DS\_Mp3} = \frac{KP\_pt}{2} \cdot \frac{W}{L} \cdot (U_{GS\_Mp3} - U_{THpt})^2 \tag{6.13}$$

$$U_{shunt\_gate} = \frac{\Delta Q_{Mp3}}{C1 + C_{parasitics}} = \tag{6.14}$$

$$= \frac{1}{C1 + C_{parasitics}} \cdot \int_{t_{start}}^{t_{stop}} I_{DS\_Mp3}\, dt \tag{6.15}$$

If the peak voltage potential of nodes $V_{AC\_coil1/2}$ is lower than the stable regulation condition of equation 6.16, node $shunt\_gate$ will be discharged, shunt transistor Mn1 will conduct less current

and the coil voltage will rise at the coil nodes again.

$$V_{AC\_coil1/2\ peak} = Vref + UGS\_Mp3 + max(UGS\_Mn3, UGS\_Mn4) \tag{6.16}$$

Discharging of node shunt_gate consumes a much longer time than charging via Mp3. This type of regulation cannot be compared with symmetrical small signal changes nor can the phase margin be simulated with conventional AC simulations techniques.
A discharge stop for the gate voltage composes diode Mp1 in front of current sink transistor Mn6. This should prevent overshoots at coil nodes $V_{AC\_coil1/2}$ when the field strength rises fast and the shunt has to work again.

Mn1 is a thick oxide transistor with a threshold voltage of about 720mV. Mp1 is a low voltage oxide transistor with about V_{th}=390mV. The lowest possible $shunt\_gate$ potential is little above 390mV and the shunt transistor Mn1 already conducts when additional 205mV are applied at the $shunt\_gate$ node. Equation 6.19 summarizes the voltage drops over the according transistors.

$$\Delta U shunt\_gate = V_{th\_Mn1} - V_{th\_Mp1} - U_{DS\_Mn6} - V_{DS\_rectifier} = \tag{6.17}$$

$$= 720mV - 390mV - 5mV - 120mV \tag{6.18}$$

$$= 205mV \tag{6.19}$$

A disadvantage of this concept is the fact that two different transistor types are used. Parameters of both transistors can vary in opposite directions depending on the global process technology tolerance. Monte Carlo simulations have shown, that 205mV are enough to reliably get Mn1 out of the conductive state. A leakage current in the region of 100pA is usual for a MOS transistor with a big channel width at room temperature.

Shunt speed control
A regulation speed adjustment can be done with node $speed\_adjust$. Normal shunt operation (fast speed mode) is guaranteed with $speed\_adjust$ = LOW. In this mode, the bias current is sunk via transfer transistor Mp2 to diode Mn7. Mirror transistor Mn7 is adjusted to sink the nominal current of 50nA and together with the regulator transistor Mp3 it defines the DC point of node $shunt\_gate$. When the digital state machine expects a HF/UHF RxD gap, node $speed\_adjust$ is set to HIGH. No current can pass through transistor Mp2 and the gate voltage of Mn7 is equal to VSS. Transistor Mn6 does not conduct anymore and no path draws current from node $shunt\_gate$. As the antenna/coil voltage is lower in these contactless operation states, no current charges capacitor C1 and the voltage potential is frozen.

Shunt HF versus UHF mode
In normal shunt operation, only the reference voltage differs between the two modes. Is the HF mode selected, node $Vref$ is pushed to 2.3V_{peak}. In UHF operation mode $Vref$ is connected via Mn2 to VSS. According equation 6.16 and 6.21, the maximum antenna voltage amounts to 4.05V_{peak} in HF operation mode and 1.75V_{peak} in UHF.

$$V_{AC\_coil1/2\ HFpeak} = 2,3V + 800mV + 950mV = 4,05V \tag{6.20}$$

$$V_{AC\_coil1/2\ UHFpeak} = 0V + 800mV + 950mV = 1,75V \tag{6.21}$$

Shunt during the RxD mode
After start-up the digital state machine enters into a permanent listening mode. Analog RxD

modules are turned on and the digital state machine waits for the first gap in the antenna peak voltage. In this state, the shunt has to control the $V_{AC\_coil1/2}$ peak potential and reacts fast when a field strength overshoot occurs. When the opposite state is applied, this means a field strength reduction in form of a gap occurs, the shunt follows at a very moderate regulation speed. The impedance of the shunt transistor Mn1 only changes only a little during the state of entering a field reduction. Coil voltage $V_{AC\_coil1/2}$ changes directly proportionally to the reduced field strength. In the HF operation mode the gap depth of the ASK modulation is defined as modulation index in UHF as modulation depth.

$$m_{index\ HF} = \frac{A-B}{A+B} \cdot 100\% \tag{6.22}$$

$$m_{depth\ UHF} = \frac{A-B}{A} \cdot 100\% \tag{6.23}$$

Where A is the average field-strength in the not modulated state and B the (average) value during the field modulation gap. According to [EPC07b] and [EPC07a] in HF mode the absolute modulation depth is much lower than in UHF and therefore more critical. In figure 6.10, the modulation index variation of the HF operation versus the magnetic field-strength is shown. In general, the RxD module unit - the HF demodulator - detects a gap with the length of a Tari = 8µs signal and it stops the shunt (with a constant $shunt\_gate$ potential). When the demodulator detects a gap, the shunt is switched into the hold mode and the gate voltage of Mn1 is conserved and stays constant. The resulting modulation index shows in weak and strong field strength condi-

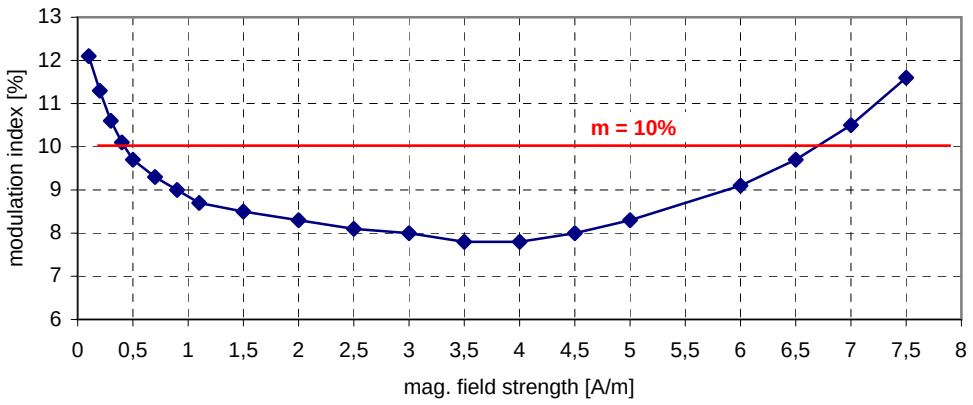


Figure 6.10: A modulation index applied of m=10% is compressed by the CTS shunt down to 8% voltage change at the coil

tions a modulation index amplification and in between (at moderate field strength) it shows an index compression below 8% instead of 10%. Because of this index reduction, the demodulator is trimmed to more sensitivity in order to detect smaller coil voltage variations than expected by calculating the modulation index. Modulation index variation is proportional to r_{DS} variation of the shunt transistor Mn1. Some parameters which influene the modulation index are taken into account in a first order impact function 6.24 and in a second order impact function, as shown in

equation 6.25.

$$r_{DS\ Mn1\ 1st} = f\left(RxD\_delay,\ waveform\right) \tag{6.24}$$

$$r_{DS\ Mn1\ 2nd} = f\left(triode/sat.,\ C_{DG} + C_{V_{AC\_coil1/2}},\ carrier\ distortion,\ TAG\ coil\right) \tag{6.25}$$

Most of these parameters are defined by the coil inductance shape and material, by reader parameters and tolerances or they are simply the result of this shunt design concept. During the design phase a big number of influencing variables has to be considered and worst case parameter sets have to be defined to speed up the pre-silicon verification phase.

Shunt during TxD
In the CTS project the shunt is also used as TxD module for load modulation or backscatter. In both frequency bands the impedance of Mn1 will be reduced by increasing the gate node potential $shunt\_gate$. When a load modulation is performed, the shunt is switched into hold mode by pulling node $speed\_adjust$ to HIGH. At the end of a TxD phase the same amount of charge is subtracted from the gate and reaches the nominal voltage potential it had before modulation. In the short non-modulation phases during TxD the shunt regulation is active and keeps the coil/antenna voltage constant.

Shunt during start-up
After more than 1ms of no-field, a magnetic or electric field bigger that is stronger than the minimum field strength is applied to the TAG once again, whereupon the voltage limiter has to cope with a safe chip start-up. Wide dynamic ranges in the field ramping speed and also a big dynamic in the final absolute value of the field strength have to be handled without a stable VDD supply voltage and stable bias current. Voltage clamping has to be very fast to be safe from voltage overshoots when the field is applied ”digital” fast. Because of two dominant resonance circuits in the RFID system, limited bandwidth reduces the speed during the field-strength ramping. For a HF system, 3 periods of about 220ns is the minimum delay for the field to ramp up and to reach its final value. Figure 6.11 shows a typical start-up with the decision after 2.6µs to switch into HF mode. During the beginning in the first 2.6µs, $Vref$ is pulled down like in UHF mode to VSS and a very low $V_{AC\_coil1/2}$ voltage appears at the coil pads. In 2.6µs the rectifier delivers power to VDD, the band detect module selects HF mode and the bias current starts to sink a current. One threshold of a thick oxide transistor is the constant voltage difference between node source and gate for the regulator transistor Mp3.

$$\begin{aligned} &V\_diode_{average} - Vref = V_{GS\ Mp3} = 800mV \\ &V_{AC\_coil1/2\ peak} = V\_diode_{peak} + max(UGS\_Mn3, UGS\_Mn4) \\ &= 3.0V + 0.95V = 3.95V_{peak} \end{aligned}$$

In this case, the maximum overshoot amplitude at the two coil pads is about 500mV. 20µs after the start-up settles $Vref$ and therefore also the coil voltage when the magnetic field strength is stronger than 1A/m. At lower field strength conditions the transient tuning time takes up to 50µs. In very weak magnetic field-strength situations below 30mA/m, the charging phase especially of VDD takes longer again and the chip starts, but it is not able to finish any contactless communication anymore.
A high charge current transfered via Mp3 to capacitor C1 guarantees the very good overshoot

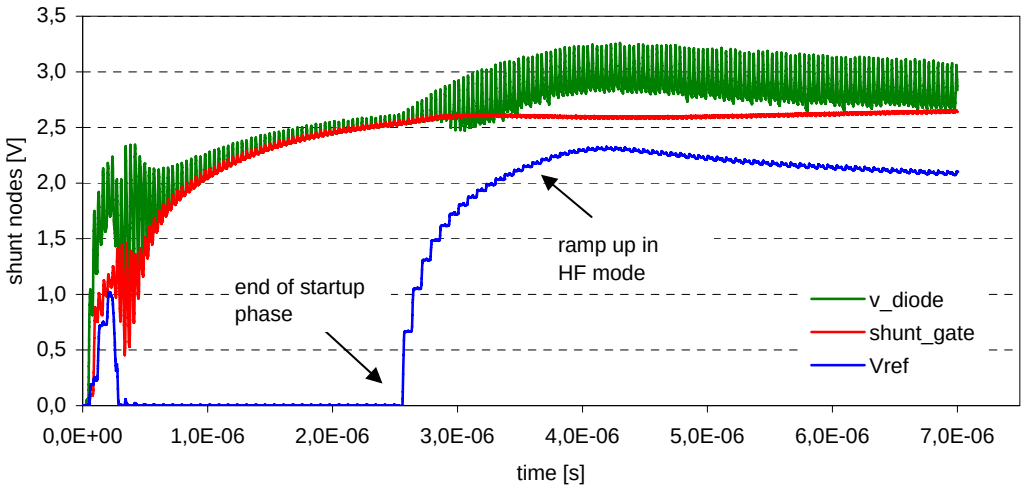


Figure 6.11: A maximum field-strength of 10mA/m HF mode startup phase

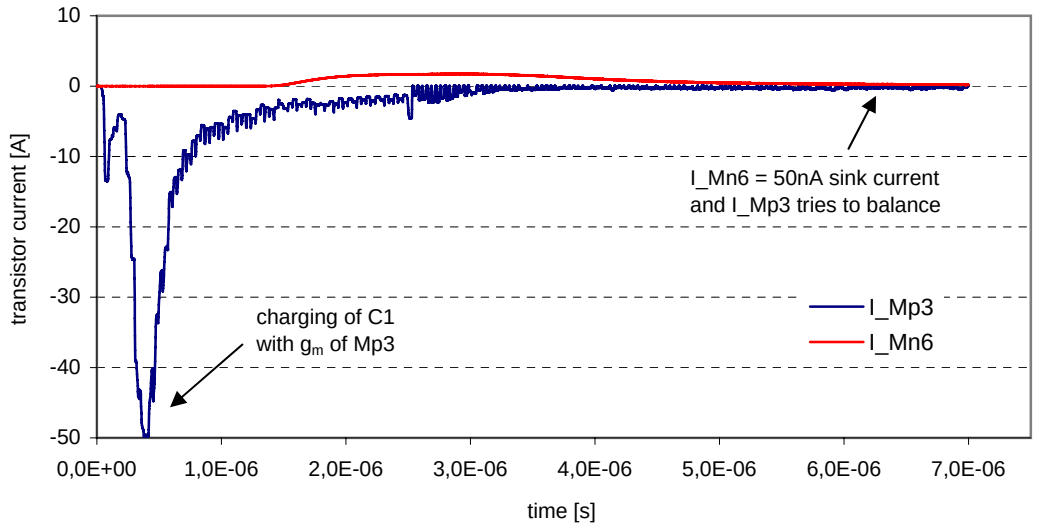


Figure 6.12: Charging current I_{Mp3} and balanced current in normal shunt mode

protection in this high field situation. The numerically averaged peak current I_Mp3 of 50µA in graph 6.12 shows the very asymmetric speed of this regulation concept. Big current spikes of up to 100µA are derived directly from the coil when an overshoot of a few hundred mV at node $V_{AC\_coil1/2}$ occurs. Thus, no power from an internal power reservoir is taken for the fast and power-hungry regulation concept.

Small signal analysis

The shunt regulation loop involves the NMOS shunt transistor, the air interface and the shunt reg-

ulation unit. As the regulation speed of the CTS regulator is unsymmetrical and rectifier diodes are also included in the loop, a small signal analysis cannot give the right frequency response. The AC analysis at least is to give us an approximation of the poles and zeros:

$$f_{dominantPole} \approx \frac{1}{2 \cdot \pi \cdot (C1 + C_{Mn1} + C_{parasitic}) \cdot (r_{0\ Mp3} || r_{Isink})} \tag{6.26}$$

$$f_{2.ndPole} \approx \frac{1}{2 \cdot \pi \cdot (C_{V\_diode} \cdot r_{diode})} \tag{6.27}$$

$$f_{zero} \approx \frac{1}{2 \cdot \pi \cdot r_{DS\ Mn6} \cdot C1} \tag{6.28}$$

$$r_{diode} = \frac{r_{DS\ Mn3}}{2}$$

The dominant pole is shown in equation 6.26. The low frequency response is formed primarily by the regulator transistor Mp3 and the capacitors $C1 + C_{\text{GS\_shunt}}$. As the early-voltage of a thick oxide transistor is high and the added capacitors are about 25pF, the -3dB reduced magnitude is at 350Hz (dominant cut-off frequency). This pole is also responsible for the very slow regulation speed in the stable operation point - in the current equilibrium of equation 6.29.

$$I_{Mp3} \approx I_{Mn6} = 50nA \tag{6.29}$$

An additional advantage of the big capacitor C1 compared to transistor capacitance $C_{\text{DG Mn1}}$ is the small capacitive voltage divider. During RxD operation mode, the shunt regulation loop is frozen - no charge is sourced into the node $shunt\_gate$ nor sunk from it. When the field-strength is reduced by the reader, $V_{\text{AC\_coil1/2 peak}}$ voltage also gets smaller and capacitive coupling to the shunt reduces its potential. This causes a reduced voltage potential at the shunt gate and, therefore, an increased dynamical resistor value r_{DS}. Coil voltage will not drop as low as the field-strength has already dropped. A reduced field gap modulation depth is the consequence and the result can be seen in figure 6.10.
C1 forms a zero with the serial transistor Mn5,as written in equation 6.28. Its negative phase shift of finally -90° increases the phase margin confidence level of the regulation loop. Both field-strength conditions show a phase margin bigger than 90° and we can expect to get a very stable regulation system. Without the zero the second pole written in equation 6.27 would not effect the loop stability, as a phase margin bigger than 80° would still ensures a very stable regulation loop. With the two diodes Mn3 and Mn4, transistor Mp3 and parasitic capacitors at node v_diode form a low pass filter at a very high cut-off frequency. The disadvantage of using no dedicated capacitor behind the rectifier is an increased 27.12MHz noise at this node and the field-strength dependent coil voltage. The CTS shunt close-loop frequency-response is shown in figure 6.13. The graph $weak$ in figure 6.13 corresponds to a field strength of 0.5A/m and $strong$ to 5A/m. Many transient simulations at different air interface conditions are additionally performed and analyzed to ascertain the regulation loop stability.

Shunt and rectifier as ESD protector

Without dedicated protection, an ESD pulse will cause a damaged chip. Passive RFID chips have only two pads which have to be protected against an over-voltage stress. SCRs and PN diodes are usually used to conduct the ESD energy burst to VSS or to another external power supply [DM99]. When shunt transistors or rectifier transistors with big transistor widths for normal RFID operation are necessary anyway, they can also be used exclusively for ESD protection. Current

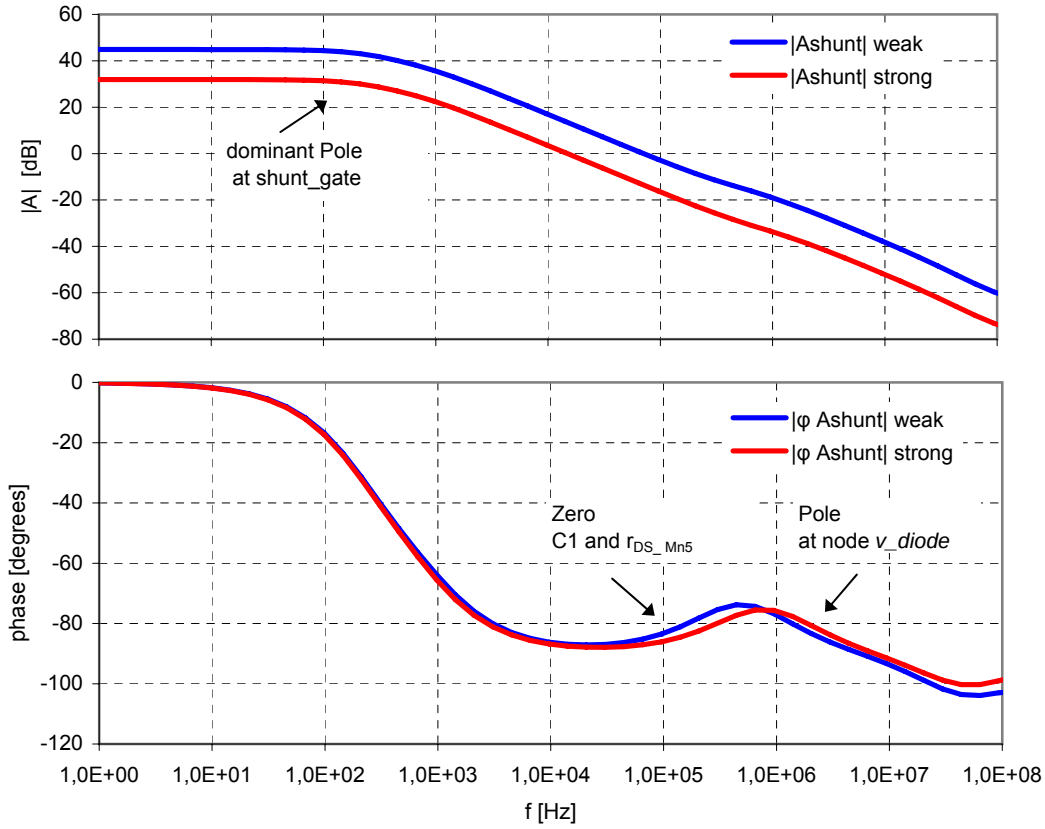


Figure 6.13: AC small signal simulation in conditions equivalent to weak an strong field-strength

distribution over the whole transistor width can be enhanced by increasing the contact to gate-edge distance and therefore also the transistor area. Avalanche breakdown from the n-diffusion

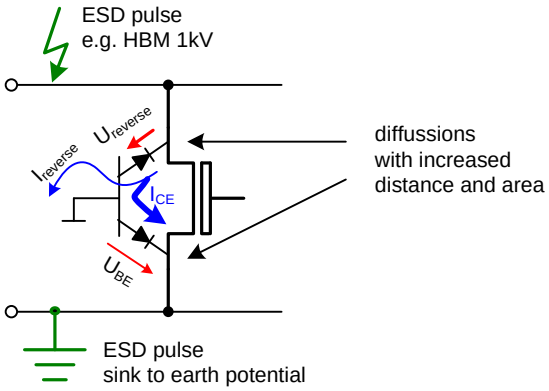


Figure 6.14: Activation of parasitic bipolar transistor during ESD stress

to substrate boosts up the voltage potential locally around the affected MOS transistor and a

forward PN diode from substrate to the second n-diffusion starts to conduct. This basis-emitter current is amplified by the geometrical $Beta$ of the corresponding MOS transistor and an NPN bipolar transistor sinks a big collector (drain) current to the emitter (source) [LS94]. This "triggered" bipolar transistor reduces the $V_{AC\_coil1/2}$ voltage drop from avalanche potential (e.g. 12V) down below normal HF mode operation voltage.

Vref generation unit

A sloppy $Vref$ value generation is done with a current-to-voltage conversation, as shown in figure 6.15. A precise coil voltage level is not necessary. A more accurate regulation system is necessary for the internal VDD voltage generation. The serial regulator which controls the VDD value, gets a more accurate reference with an absolute error of $\pm 22\%$. Four transistor threshold voltages with little overdrive define the shunt regulator gate voltage. Monte Carlo simulations and temperature/technology parameter variations show a spread of $\pm 30\%$. This tolerance and an additional safety margin of 10% define the operation point for the shunt regulator. Current source

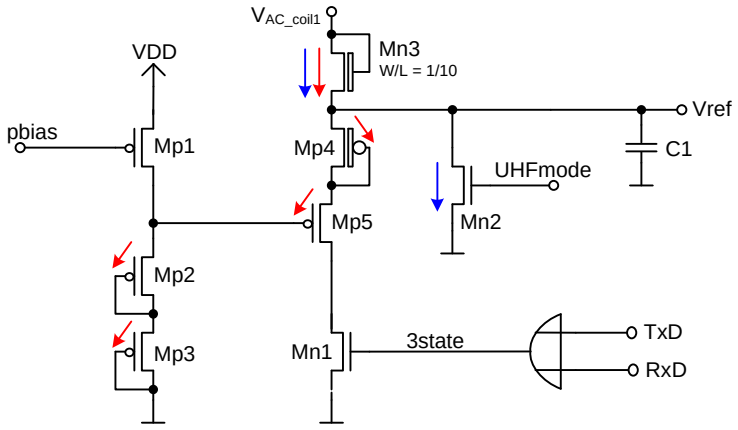


Figure 6.15: Gate voltage generation for the PMOS Regulator

Mp1 in figure 6.15 generates an intermediate voltage of about 0.9V with two thin oxide transistors. Additional 0.6V of thin oxide transistor Mp5 and 0.9V of thick oxide transistor Mp4 define Vref with a value of 2.3V. One NMOS transistor represents a rectifier diode with a big channel length. This is the active pull-up transistor of the reference circuit. Vref voltage level dependency of the input peak coil voltage $V_{AC\_coil1/2}$ is shown in graph 6.16. In the active region of the shunt limiter above 3.5V the clamping mechanism of the four transistors is evident.
The reason for the unusual design concept of this reference generator is the need for a very fast start-up when high field-strength is applied. The regulator transistor Mp3 gate potential lasts at VSS potential but the source rises rapidly. Next, a big amount of current is transferred to node $shunt\_gate$ and the shunt transistor conducts very well. This results in a voltage clamp at very low coil voltage level, in an IC power starvation and, consequently, in a transponder malfunction. When the coil voltage rises, the potential reduced by one threshold voltage and immediately forwarded to $Vref$ by diode Mn3. Clamping of the reference potential enters when $Vref$ reaches four threshold voltages. PMOS Mp5 will strictly discharge the excessive current of diode Mn3 to VSS.

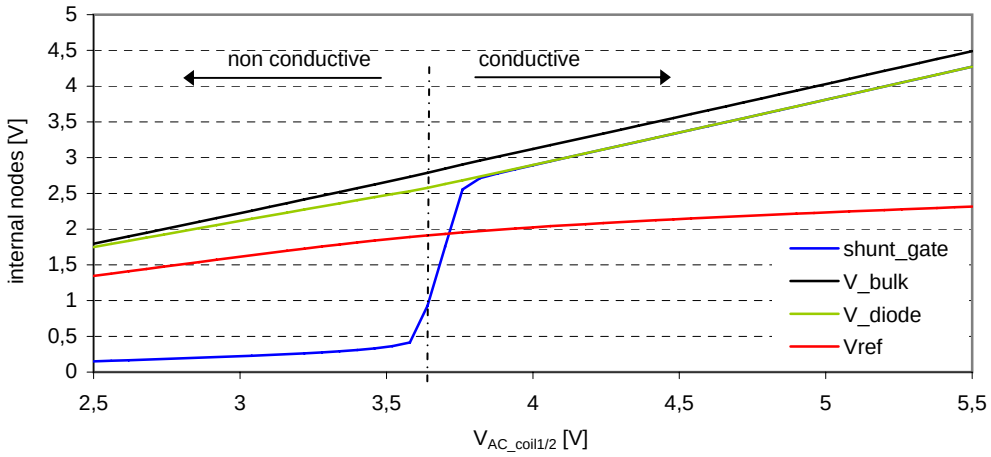


Figure 6.16: Vref variation during active shunt area of only 380mV

6.4 TxD - Transponder to Reader communication

Changing the chip impedance at input nodes $V_{AC\_coil1/2}$ is the base for TxD communication in both frequency bands. Either resistive [LZYX06] or capacitive changes [PYN+02] are feasible for a passive RFID transponder system. In the CTS project, primarily the differential shunt resistance changes and in the second order the nonlinear chip input capacitance is manipulated (the capacitance changes). Finally, we will get always a mixture of amplitude and phase modulation in both frequency bands.

6.4.1 HF Load Modulation

Some differences between HF and UHF were already shown in table 7.1. In addition to the parameters listed there, an obvious HF TxD relevant requirement is to interact synchronous with the reader (to the 13.56MHz carrier) during the modulation phases. The easiest way to stay synchronous is to guarantee enough carrier amplitude during load modulation pulses so that the clock recovery can still work. Conventional designs have two MOS diodes in serial to a modulator transistor or a more advanced modulation unit [Phi05]. These diodes ensure a defined minimum peak voltage level at $V_{AC\_coil1/2}$ during the load modulation. Typically, the coil voltage will never drop with its peak value below a MOS transistor diode threshold.

$$\begin{aligned} U_{GS\_Mn1\ peak} &= U_{GS\_Mn2\ peak} = U_{GS\_Mn\_diode} \\ U_{TxD} &= U_{GS\_Mn\_diode} + U_{DS\_Mn3\ peak} \\ &= f(H_{field}, gm_{Mn\_1,2,3}, TAG\ parameter) \end{aligned} \tag{6.30}$$

The thick oxide switch Mn3 should be turned on during the load modulation pulse with a voltage level close to the coil voltage to reduced voltage drop U_{DS_Mn3}. The lowest voltage drop will always occur at the lowest field strength where the transponder is able to work. This design concept is simple and robust.

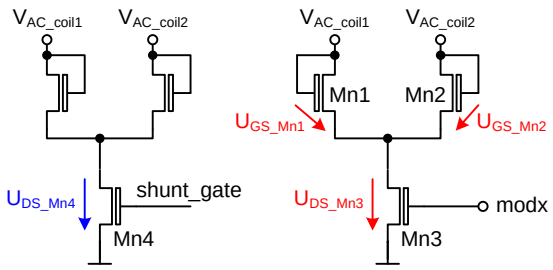


Figure 6.17: A typical schematic for commercial products with separate shunt and TxD path, each equipped with a rectifier

When such a challenging concept with combined shunt and TxD modulator with only one transistor has to be implemented, special attention to the regulation loop should be obtained. Usually the sensitive shunt regulation is separated from the TxD switch. To fulfill the CTS requirements a sensitive shunt and sensitive TxD regulation for the HF band is necessary. In the UHF band it is not necessary to care about a minimum peak voltage during TxD because the chip is driven by an internal oscillator anyway.

TxD regulation scheme
Directly before the load modulation starts, only the shunt regulation unit is active and current equilibrium between source current from regulator transistor I_{Mp3} and current sink I_{Mn6} is reached (see equation 6.9). During this process, the modulation path is off and transistor Mn6 in figure 6.18 conducts well.

6.4.2 CTS TxD Unit

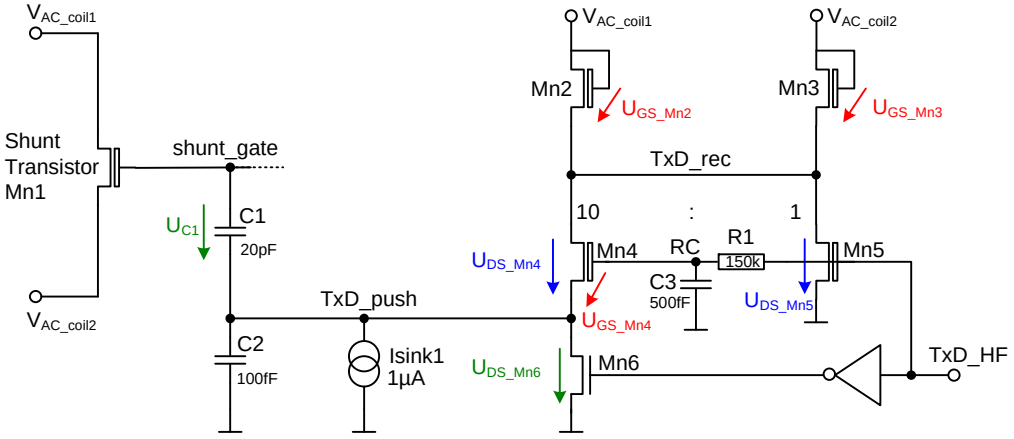


Figure 6.18: TxD Unit for HF load modulation

When TxD starts the uplink with a transponder to reader data transfer, the modulator unit is switched on before the beginning of the first load modulation frame. Before the HF modulation

phase starts, the interface signal TxD_HF is LOW and inverter output Mn6 HIGH. This pulls node TxD_push and so the bottom plate of C1 down to VSS potential. Load modulation starts with changing the potential of node TxD_HF from LOW to HIGH potential.
Some crucial internal TxD signals are shown in figure 6.19. During the modulation phase, the fast

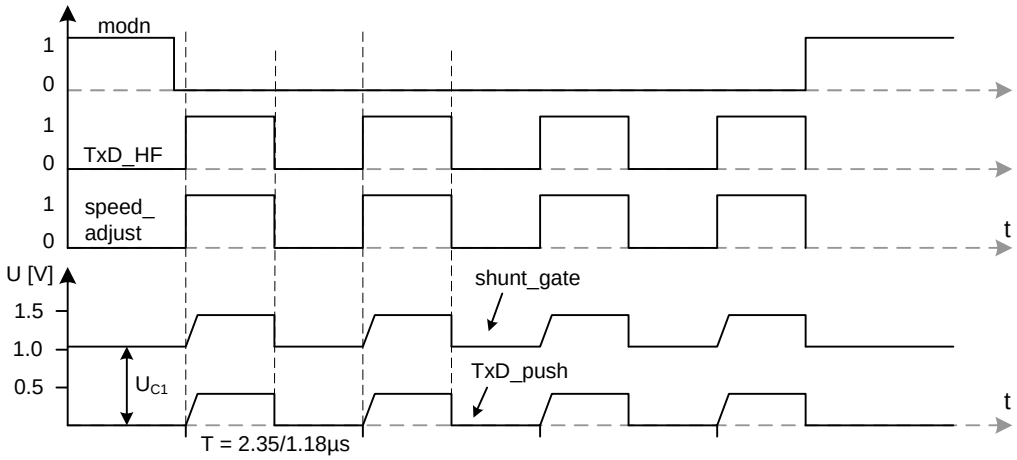


Figure 6.19: Control signals of the shunt/modulator for EPC-HF Gen2 at 53kbit/s load modulation and moderate field-strength

regulation loop of the TxD module starts to reduce the coil voltage form 4V to about 700mV$_{peak}$. This should be done in between one or two carrier periods ($t \approx 150ns$). Fast regulation loops tend to over- or in this case, to undershoot because the phase margin of such regulation loops are usually too small. 500mV is the absolute minimum for a proper CTS 13.56MHz clock recovery function. The weak pull down transistor Mn5 (about 10 times smaller than Mn4) immediately starts to conduct when node TxD_HF rises to HIGH potential. Mn5 then sinks a certain current via the two MOS diodes Mn2 and Mn3 to VSS. Compared to the gm of the shunt/modulator transistor Mn1, Mn4 is 120 times weaker but it still sinks a current of 15µA up to 38µA (depending on VDD). Mn5 makes sure that the capacitive is removed charge below the two diodes at node TxD_rec and that already a weak constant load is pulled at the coil nodes. Low pass filter R1 and C3 delays the rising edge of signal TxD_HF by $\tau = 75ns$ and provides the gate potential for regulator transistor Mn4. The gate to source voltage U$_{GS\ Mn4}$ is the input signal for the big regulator transistor Mn1 and is responsible for the fast clamping of the coil voltage level. In this regulation loop, transistor current starvation is controlled via U$_{DS\ Mn4}$, which is the regulation mechanism. In figure 6.20, the source of transistor Mn4 is represented by TxD_push and the drain is represented by the very fast falling voltage TxD_rec. One τ after the rising edge of signal TxD_HF the gate of transistor Mn4 reaches 800mV and starts to source charge into node TxD_push which will be pulled up.

$$V_{AC\_coil1/2\ peak} = U_{GS\_Mn2\ peak} + U_{DS\_Mn4\ peak} + \Delta U_{TxD\_push} \quad (6.31)$$

$$\Delta I_{DS} = g_m \cdot \Delta U_{GS\_Mn1} \quad (6.32)$$

As the linear poly-poly capacitor C1 with a value of 20pF is big compared to the parasitic capacitance at the tristate node $shunt\_gate$, the voltage level dynamic from the lower poly plate

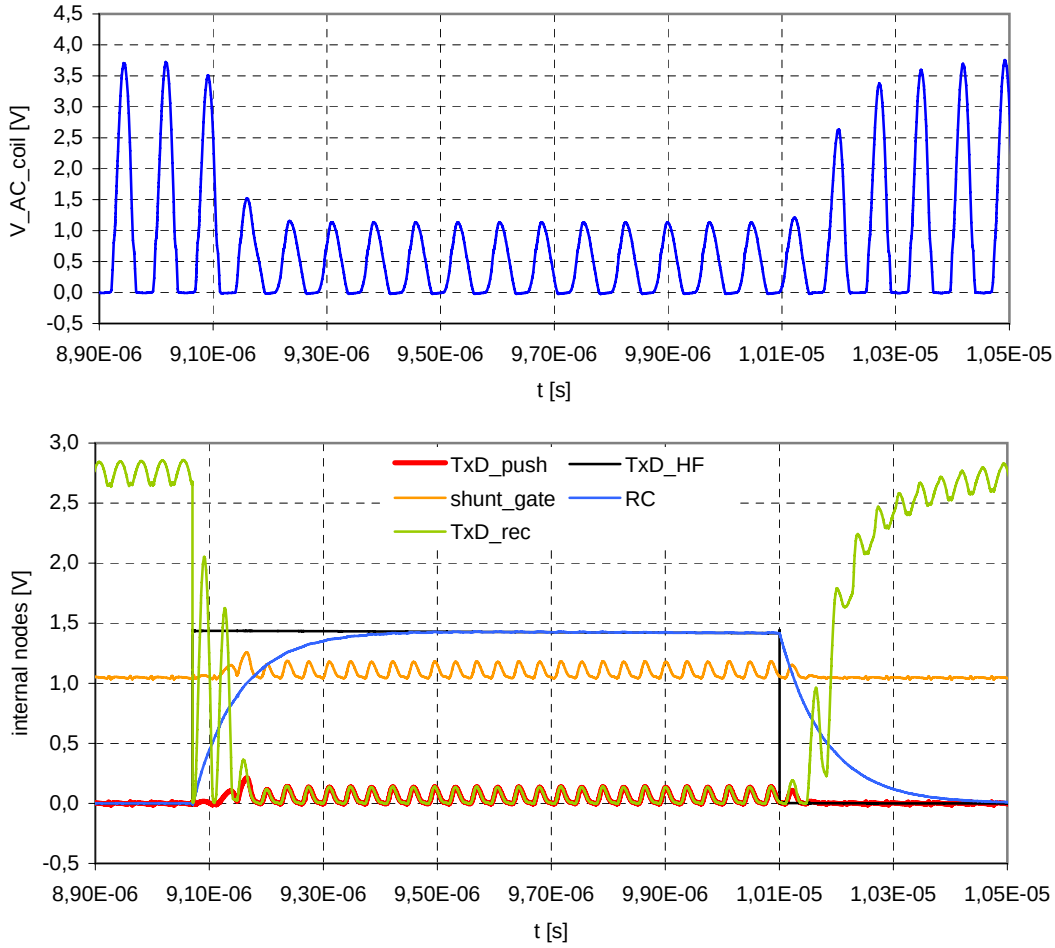


Figure 6.20: HF load modulation at 1.5A/m

TxD_push is coupled reliable to the upper poly-plate. If due to parasitic capacitive dividers (extracted from back annotated layout extraction) the upper poly plate does not follow the lower plate any more. In this case during the load modulation phase node TxD_push will find its stable regulation point at a slightly higher potential. According to formula 6.31, an increased potential at node TxD_push increases the coil voltage $V_{AC\_coil1/2}$ and therefore, a reduced modulation depth is caused. Because of a high gm for the shunt/modulator transistor Mn1, a slightly increased $shunt\_gate$ voltage is enough to divide the coil voltage peak level. Additionally, during the modulation phase the cross-coupled NMOS pair in the rectifier is weaker. This causes a more negative $V_{AC\_coil1/2}$ potential which increases the regulator potential $U_{GS\ Mn1}$. In graph 6.21, the speed of this regulation can be seen in the very transient signal TxD_push and $shunt\_gate$ signal response at the beginning of the load modulation. High current is necessary for this regulation speed and it is derived from the dropping field. Finally the consumed power is a small part of the total load current.
An increased regulation speed typically entails the risk of an unstable loop. As in nominal shunt regulation situations, the dominant pole is still the gate capacitance of Mn1 with secondary par-

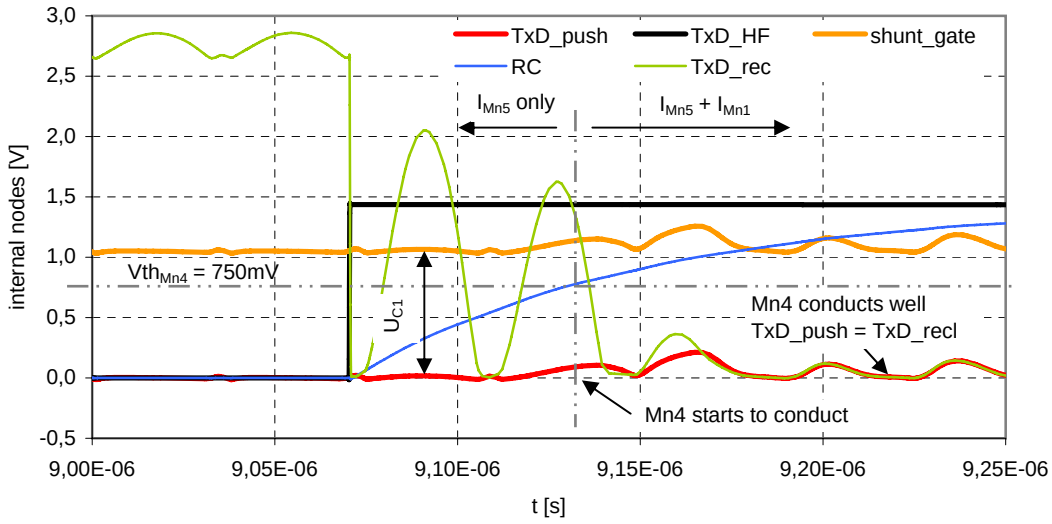


Figure 6.21: Zoomed start phase of HF load modulation

asitic capacitors at this node. A secondary non-dominant pole is located at node TxD_rec. Mn5 sinks a big current and supports a fast charge transfer from this critical node to VSS.

6.4.3 UHF backscatter

In the UHF frequency band either ASK or PSK backscatter modulation is feasible. Both architectures could be implemented in a small chip silicon area. Shunt regulation works similarly as in the HF mode but TxD backscatter is implemented in a power-optimized matter.
Assuming a specification conform to TxD operation at all data rates and equivalent layout-area for both modulation types, following system parameters should provide a fundamental appreciation for ASK versus PSK backscatter modulation. Backscattered power density changes from the transponder to the reader can be calculated via radar equations shown in [HPV+09], [NR06b], [Sko01], [Fin06], [FKFS02] and [AV03]. The following equations are valid for perfect matching and free space conditions:

$$P_{tag\_received} = A_{e\_tag} \cdot S \tag{6.33}$$

$P_{tag\_received}$ is the power collected by the tag antenna, A_{e_tag} the effective area of the tag antenna and S is the power density.

$$A_{e\_tag} = \frac{G_{tag} \cdot \lambda^2}{4\pi} \tag{6.34}$$

G_{TAG} is the tag antenna gain.

$$P_{reader\_in} = P_{backscatter} \cdot G_{tag} \cdot G_{reader} \frac{\lambda_0^2}{(4\pi \cdot r)^2} \tag{6.35}$$

As backscatter information, the reader gets a sideband power P_{reader_in} reflected back to the reader antenna. $P_{backscatter}$ can also be expressed with the help of the radar cross section ΔRCS.

$$P_{backscatter} = S \cdot \Delta RCS \tag{6.36}$$

Modulation type	Backscatter power	Power disposable for the IC
perfect Matching ⇔ OPEN	$0.50 \cdot P_{avail}$	$0.50 \cdot P_{avail}$
perfect Matching ⇔ SHORT	$0.50 \cdot P_{avail}$	$0.50 \cdot P_{avail}$
resistive ASK	$0.22 \cdot P_{avail}$	$0.55 \cdot P_{avail}$
resistive PSK	$0.32 \cdot P_{avail}$	$0.80 \cdot P_{avail}$

Table 6.2: Different modulation types and power loading

With the radar cross section definition, the influence of impedance changes at the chip input can be visualized.

$$\Delta RCS = \frac{\Delta Z_{IC} \cdot \lambda_0^2 \cdot G_{tag}^2}{4\pi \cdot R_{IC}} \tag{6.37}$$

Z_{IC} is a complex vector and includes resistive variations and the capacitive amount of the chip input impedance. As in the HF band, sideband information in the reader does not only depend only on mechanical parameters (effective area, gain of antennas) and electrical parameters (shape of the waveform, quality of the short/open/detuning).
The reflected power to the reader and the power still available for the IC during the backscatter phase are further performance criteria. A PSK backscatter scheme can be chosen in the UHF mode and would be an opportunity to supply the IC also during the backscatter phase. Table 6.2 gives a short overview of the amount of reflected power and of the power consumed by the IC [Dob07]. Again, these values are only valid for perfect impedance matching and perfect power switching conditions. We clearly see the advantage of PSK phase shift keying modulation. It delivers a good backscattered power efficiency and forwards the biggest power amount to the chip. Also [CDDJ07] and [KF03] show the advantage of PSK.

Is it really necessary to optimize the ratio of reflected to delivered chip power?
The reader sensitivity is the maximum delta between the emitted power by the reader antenna and the received backscatter power information. It is defined in dBc. According to paper [NR06a], a sensitivity of about 120dBc is enough to overcome maximum tag power performance distance by a factor of 6. As the power performance of the CTS chip is about 6dB worse than that of single band UHF chips, the receiver channel of the reader never limits the maximum operation distance. This fact is the basis for the final decision about which concept to use for the CTS backscatter modulation. With a reuse of most of the already implemented HF band transistors and only some additional transistors and passive components for the UHF backscatter unit, the silicon overhead is small and below $10\mu m^2$. Every additional parasitic junction or parasitic oxide capacitive will reduce the UHF power performance. Thus, ASK was chosen as backscatter method with small modifications at one performance uncritical DC node. The schematic is shown in figure 6.22. Similar to the HF load modulation concept, during UHF backscatter node TxD_push potential will be increased. No precise regulation is necessary. As a local oscillator and no clock recovery delivers the internal clock, no minimum peak voltage potential at $V_{AC\_coil1/2}$ is necessary anymore and fast and precise regulation is not used either. The thin oxide transistor Mp1 is conductive during the modulation phase and it increases the potential at node TxD_push very fast. C1 hands over this potential to the node $shunt\_gate$ and Mn1 reduces its dynamic output resistance. $V_{AC\_coil1/2}$ peak voltage depends on the incoming power and as it will be in weak field-strength conditions $(< -6dBm)$ below 100mV during the backscatter phase,it will be close to an ideal

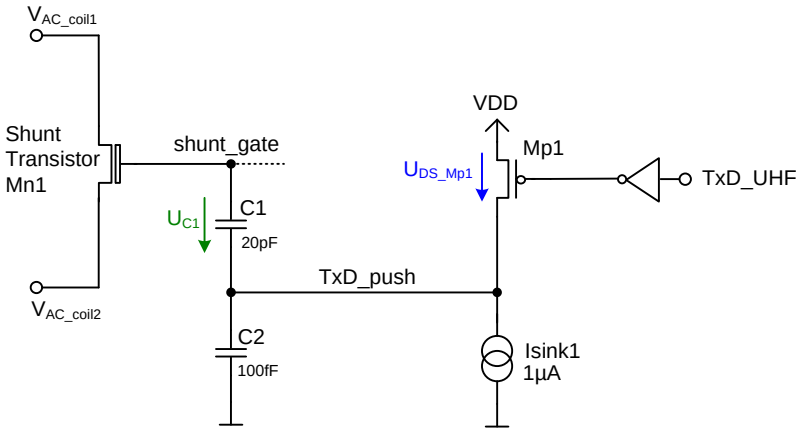


Figure 6.22: TxD Unit for UHF backscatter

short-circuit.

6.5 RxD - Reader to Transponder communication

In almost all specifications for RFID air interface protocols ASK is used. Only PJM ISO/IEC18000-3 Mode 2 uses phase jitter modulation for the RxD path. The disadvantage of PSK on-chip demodulator units is their higher module power consumption compared to ASK RFID peak detection demodulators. EPCglobal prescribes for both frequency bands ASK for RxD with similar gap lengths and field modulation depths. It would be obvious to use one demodulator for both frequency bands, however, less modulation information in HF and different DC operation points require a flexible demodulator input stage. Since the area of the UHF demodulator module overhead is small and each can be switched off, the decision was made to use two optimized demodulator units for the CTS project. Figure 6.23 shows two separated analog demodulator units

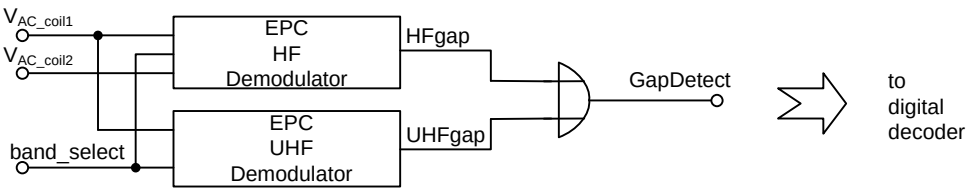


Figure 6.23: Two specialized analog demodulators are used in the CTS project

with one common output $GapDetect$ which is handed over to the digital decoder. Concurrent operation of both demodulators will not occur because only one decoder will always be selected according to the signal $band\_select$ which is generated in the clock recovery module.

6.5.1 HF ASK demodulator

The basic design concept is derived from a patent [Mis04] and was introduced for high data rate applications with a highly dynamic modulation index. In the HF EPC specification, the data rate is low compared to 848kBit/s used in proximity applications, but the advantages of this design concept prevail compared to the simple single intersection detectors [Fin06]. Power consumption of this demodulator is less than 500nW.

Building blocks of the demodulator architecture can be seen in figure 6.24. A rectifier converts the

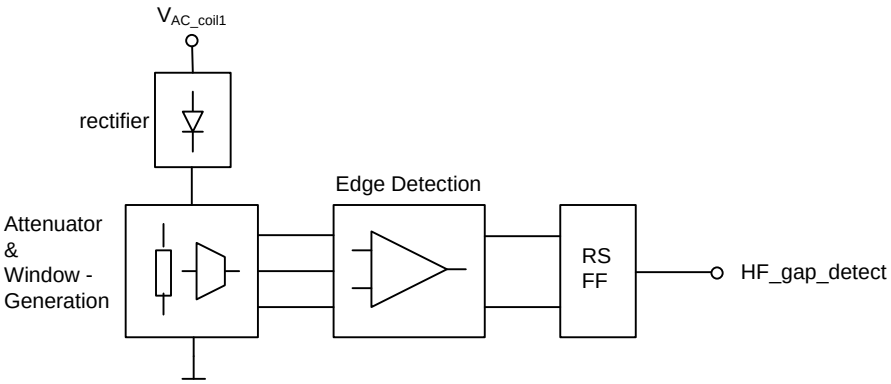


Figure 6.24: CTS HF demodulator block schematic

coil voltage $V_{AC\_coil1/2}$ with thick oxide transistors into a DC voltage with superposed 27.12MHz noise. The noise is filtered in the following block and 3 signals with equal voltage intervals generate the so called ”window”. An integrator then reduces the speed of the central signal. A window comparator detects the two intersection points and generates the signal HF_gap_detect which is delivered to the digital decoder.
The rectifier NMOS diodes are already part of the attenuator which is shown in figure 6.25. To

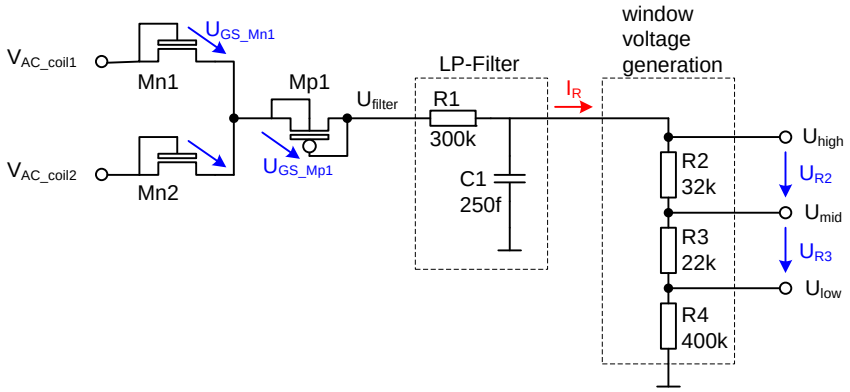


Figure 6.25: Attenuator, low-pass filter and window voltage generation

conserve the modulation depth information, one additional diode Mp1 is used instead of a resistive divider with a bigger divider ratio. Resistor R1 is part of the low pass filter to reduce noise and is already part of the voltage divider. In between the second big resistor value R4 of 400k there are two smaller resistors for the window generation. $22k\Omega$ and $32k\Omega$ will never generate equal voltages drops. They compensate the systematic offset of the attached integrator. Obviously, an integrator with a systematic offset smaller than 1mV could be designed but it would draw more current and, especially, would take up more area. With the help of the Monte Carlo analyses, node $Umid$ is placed in between U_{high} and U_{low}. The current I_R through the resistors defines the voltage drop and, therefore, the voltage window size as well as the cut off frequency of the low-pass filter.

$$\begin{aligned} U_{filter\ peak} &= V_{AC\_coil1/2\ peak} - U_{GS\_Mn1/2\ peak} - U_{GS\_Mp1\ peak} \\ &= 4.5V - 1.4V - 1V = 2.1V_{peak} \end{aligned} \tag{6.38}$$

The small signal AC analysis response of the input structure is shown in figure 6.26. Derived from simulation results, the peak voltage at node U_{filter} can be converted to an average voltage which is the base level of the following current calculation.

$$U_{filter\ average} \approx 0.8 \cdot U_{filter\ peak} = 1.68V \tag{6.39}$$

The factor 0.8 is derived from transient simulations and is valid for the voltage band from 2.5V_{peak} up to 5V_{peak}.

$$I_R = \frac{U_{filter\ average}}{R_1 + R_2 + R_3 + R_4} \approx 2.3\mu A \tag{6.40}$$

This current is quite high even for the HF band, but it delivers a good transient field-change response at all three window signals, even with the additional capacitive loaded detectors. The two unsymmetric window voltages which compensate the integrator offset are:

$$U_{R2} = R2 \cdot I_R = 74mV$$
$$U_{R3} = R3 \cdot I_R = 51mV$$

In graph 6.26, the AC response of the attenuator is shown with transistor-gate and parasitic capacitance. Node $Vdiode$ is loaded with the parasitic capacitor formed by the poly of transistor-gate Mn1, Mn2 and Mp1 to the substrate. The non-dominant pole cutoff frequency is at about 36MHz. In the schematic, following nodes are located behind the low pass filter R1 - C1 and they represent the 3 demodulator window signals. The sharpest dip in the frequency response effects the node with the lowest voltage potential U_{low}. At this node beside the dominate pole R1-C1 there are already some additional R-C bundles active. At 27.12MHz the attenuator reduces the voltage noise by a value of 29dB.

Instead of an additional resistor the voltage divider includes the diode Mp1, which helps to increase the modulation index at the attenuated output nodes. In figure 6.27 node U_{mid} was chosen to show the modulation index of this node compared with the modulation index generated by the ideal field. The advantage of an increased field gap modulation is a reduced demodulator sensitivity, which correlates well with design complexity and also with power consumption. EPCglobal specification defines an index from 10% down to 30%. In this region the attenuator

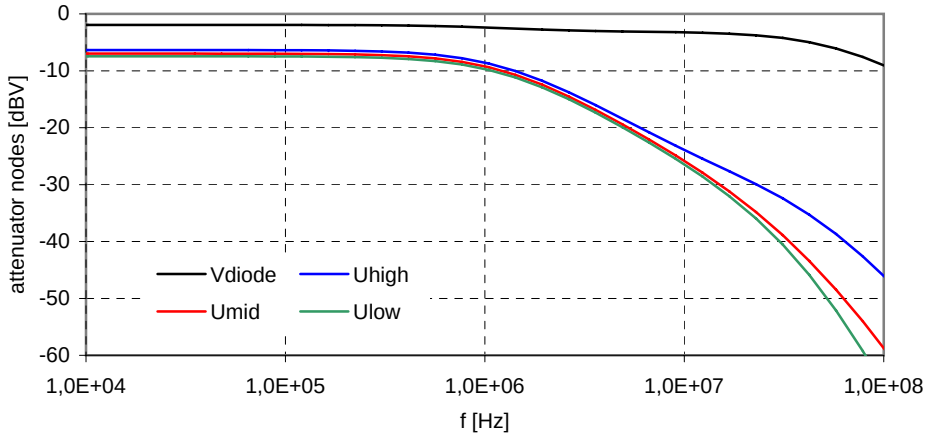


Figure 6.26: Small signal AC analysis of the input attenuator

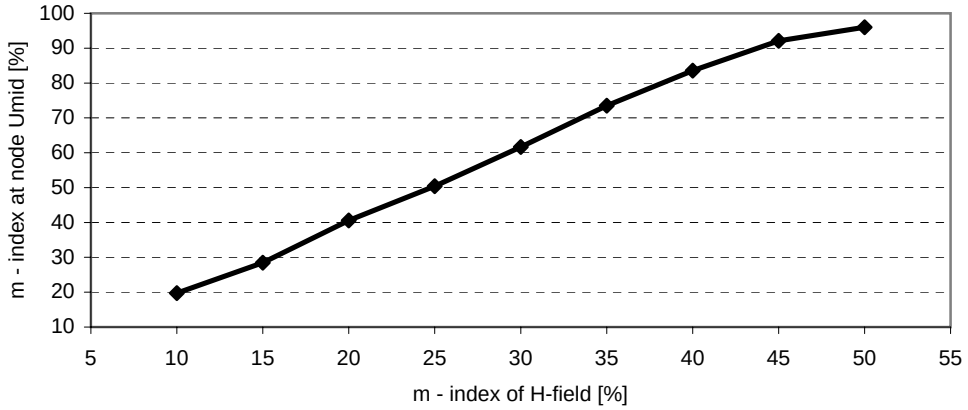


Figure 6.27: The modulation index - m is almost doubled at node U_{mid}

generates an increased index by a factor of 2. If the modulation index gets very deep, the voltage divider saturates and the positive effect of an increased modulation index shrinks, still, the demodulator gets a signal information of already close to 100% during the deep modulaion.

HF demodulator block module

Two signals from the attenuator U_{high} and U_{low} and one centered signal U_{mid_int}, which is similar to U_{mid}, are weighted by two comparators. With an attached RS flip-flop the detected edge is stored. The demodulator output $HFgap$ is buffered and routed to the digital state machine. In the EPC HF regulations, the gap duration of a field-strength modulated signal is defined by an absolute maximum value of 4.5µs. Based on simulation results shown in graph 6.29, a nominal U_{mid} value of 600mV is assumed. A value of 10% is the weakest field modulation index specified. The not ideal external voltage limiter impedance characterisitc reduces this value. Since the shunt causes a 20% index reduction and also a 10% margin because of additional delays in the

attenuator, the following worst-case EPC specification for the CTS HF demodulator is the result:

$$\begin{aligned} U_{high\ no\ modulation} &\approx 600mV \\ m_{field\ min.\ EPC\ index} &= 10\% \\ equivalent\ atten.\ mod\_index &\approx 14.5\% \\ equivalent\ atten.\ mod\_level &\approx 0.75 \\ safety\ margin &= 20\% \\ \Delta U_{high} &= (U_{high\ nom} - U_{high\ nom} \cdot 0.75) \cdot 0.8 = 168mV \\ \frac{U_{high\ EPCspec}}{\mu s} &= \frac{168mV}{4.5\mu s \cdot 1.1} = 33.6mV/\mu s \end{aligned}$$

This slew rate number for the falling/rising slope is only valid in between 10% - 90% of the final modulation depth waveform amplitude. To detect the weakest steepness of the field-strength variation, node U_{mid_int} has to be slower than node U_{mid} during rising and falling edges.

$$\begin{aligned} \frac{U_{mid\_int\ slow}}{\mu s} &= \frac{I_{bias}\ slowOTA}{C_{OTA}} = \frac{37.5nA}{4pF} = 9.3mV/\mu s \\ \frac{U_{mid\_int\ fast}}{\mu s} &= \frac{I_{bias}\ fastOTA}{C_{OTA}} = \frac{400nA}{4pF} = 100mV/\mu s \end{aligned}$$

A worst-case factor of 3.5 between the attenuator signal steepness ($33.6mV/mus$) and the output of the integrator in the slowest operation condition ($9.3mV/\mu s$) is enough to detect all EPC HF specified edges. The reason for taking a big safety factor between both signals are delays in

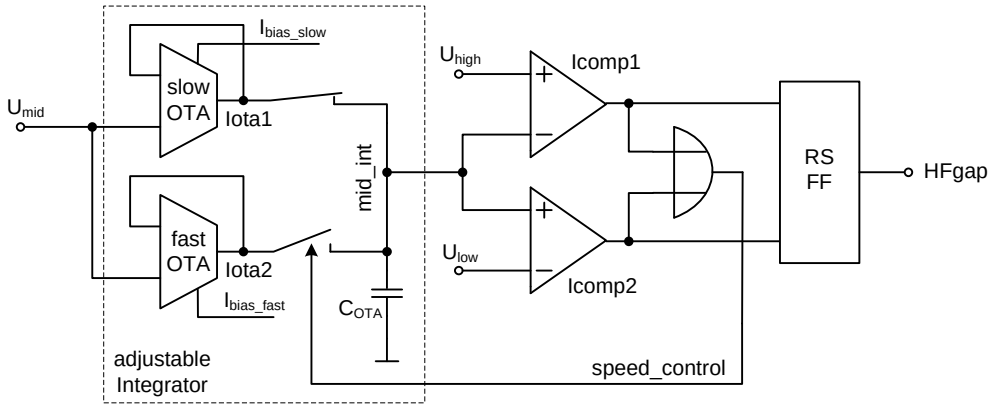


Figure 6.28: Edge detector with adjustable integrator and 1 bit ADC

the edge detection and an offset voltage difference which reduces the depth once more.
In figure 6.28, the demodulator with a logic gate triggered by the RS Flip-Flop increases the speed of the OTA at each detected crossing of either U_{mid_int} with U_{high} or U_{mid_int} with U_{low}. The speed switching is done with an additional current that is delivered by a second faster OTA with an increased performance. When the very fast node U_{mid_int} is back again in between the two outer signals ($Uhigh$ and $Ulow$), the speed is reduced and only the slow OTA is attached

once again.

A simulation of two modulation gaps in moderate field-strength is shown in graph 6.29. On the very left side of the graph we can see a non-modulated phase. There the impact of the asymmetric attenuator can be seen in the non-equidistant voltage range. With the systematic offset of

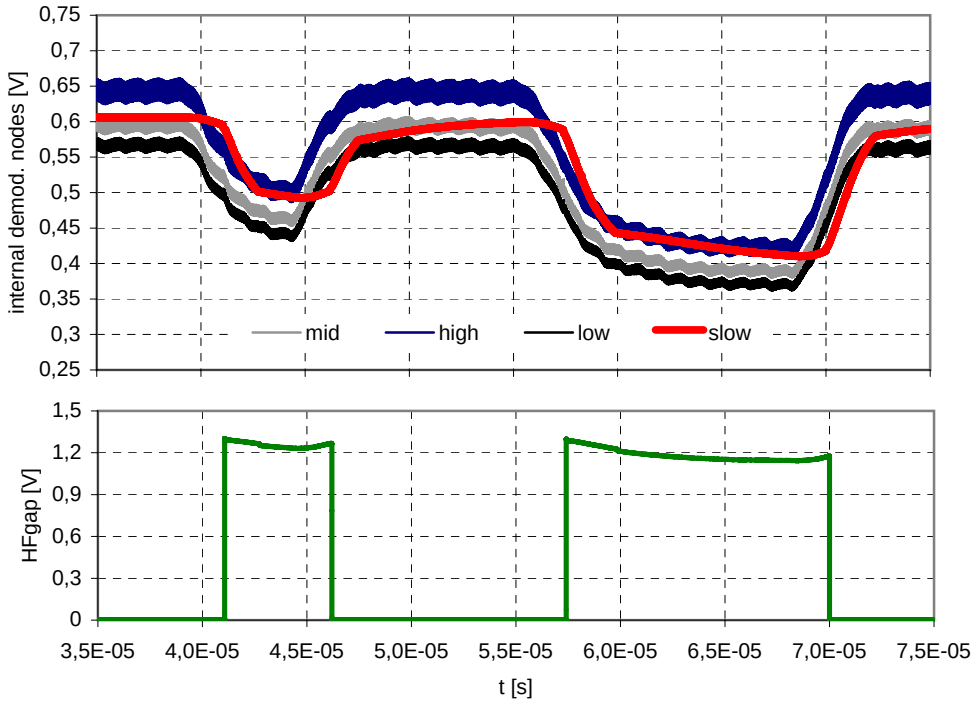


Figure 6.29: Signals at the comparators and the resulting gap-detecting signal after the RS-FF

the attached integrator node, U_{mid_int} then is finally centered in between the two outer signals U_{high} and U_{low}. According to the transfer function of graph 6.26, these two signals are delayed compared to the coil voltage envelope but they are still fast enough. Comparator Icomp1 detects the crossing of U_{high} and U_{mid_int} and switches the OTA into the "'fast"' operation mode. U_{mid_int} follows at a speed 10 times higher than in normal mode and passes the high signal once again. If the gap bottom is reached at about 42µs, the crossing of U_{mid_int} and U_{high} is over and with a small delay, the OTA is switched back into slow mode again. At the rising edge the sequence is repeated when U_{mid_int} crosses U_{low}. The OTA changes from slow to fast until the nominal U_{mid_int} level is reached once again. This demodulator concept is robust and handles a big dynamic in modulation index and bit rate.

Figure 6.30 shows the OTA, which is used for both speed versions (slow and fast speed). This is a usual architecture with a PMOS differential pair [AH02] which, unlike an NMOS input structure, also works well during very deep modulation gap. Apart from the regulation loop stability, the reason to choose this design was to get a current sink/source with a good PSRR. No Miller capacitor is necessary for the loop stabilization. Low OTA bias currents of 37.5nA and 400nA are derived by Mp3 once in slow and once in fast mode. Sub threshold operation for the input

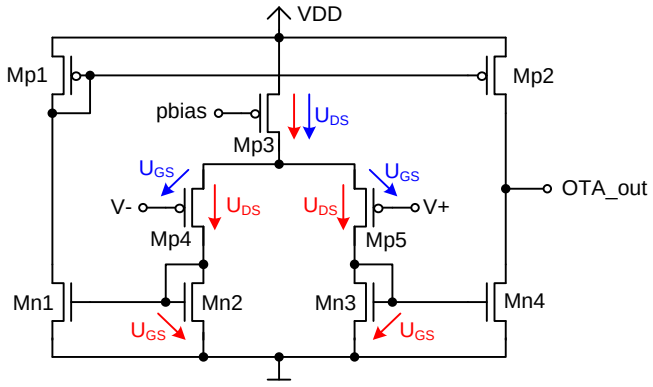


Figure 6.30: OTA used in the edge detector for slow and fast integrator path

structure cannot be avoided and will cause an additional random offset. Transistor channel length modulation [Bak07] is the reason for the systematic offset and is generated by transistor Mp2 and Mn4. To avoid this effect, either the gate length could be increased or a cascode structure could be included.
The two comparators in figure 6.31 are used to detect the crossing points which are shown in figure 6.29. The comparator design consists of a two-stage operational amplifier without frequency compensation and of two inverters with different driver strength capability. PMOS transistors are

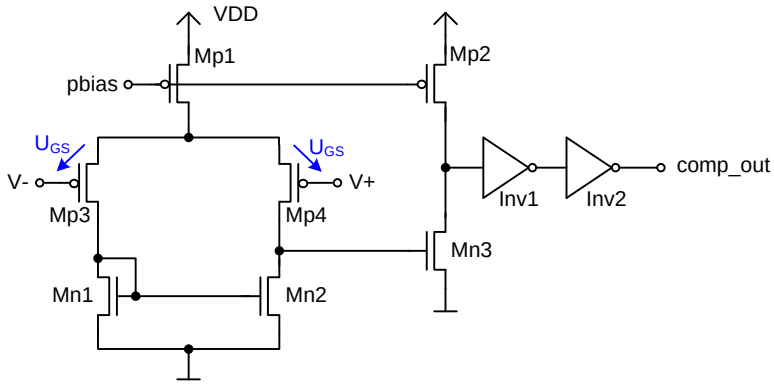


Figure 6.31: Comparators used to detect either a rising or a falling coil voltage

also taken for the differential input pair because the voltage range is already tuned for them. A worst case corner delay of 270ns - 450ns and an average current consumption of about 200nA are crucial issues of the comparator. An increased comparator speed is not necessary because the delay occurs at the falling and at the rising edge and, therefore, the timing error can be neglected. The result is a constant and correct gap length which is delivered to the digital state machine.

6.5.2 UHF ASK Demodulator

In contrast to the high peak voltage potential at the coil during HF operation, no attenuator is necessary to generate an information signal for the UHF demodulator. Another crucial difference is the minimum modulation depth of 80%. In HF an equivalent minimum modulation depth of about 18% is defined.
Especially the relaxed sensitivity does not demand a ”complex” core used for the HF demodulator any more and the attenuator is useless for UHF. In literature, many architectures of decoupling units have been introduced and, obviously, have been optimized regarding their shunt and rectifier concept [KF03] [Fin06] [NYY07]. A new demodulator concept is introduced which consumes less current than the HF RxD module and is optimized for EPC UHF. In figure 6.32, the architecture

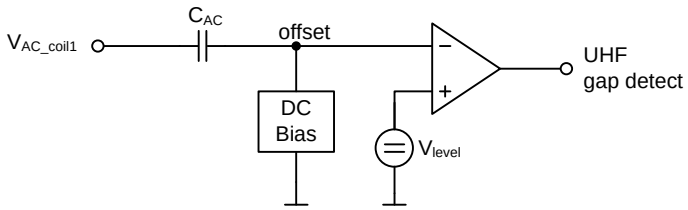


Figure 6.32: Low power ASK demodulator concept for the UHF frequency band

of the demodulator is shown. Capacitive AC coupling and the generation of a constant DC bias voltage are the basic units of the CTS demodulator. C_{AC} is used to couple the antenna peak voltage information (with a value range of 0.7V - 1.5V) to the internal node $offset$. There, a constant DC potential is added and, together with a peak voltage limiter, this arranges a stable signal which is converted to a digital state by a comparator. In HF mode, node $offset$ is protected against over-voltage and power loss is negligible. The transistor-level schematic of the UHF RxD unit is shown in figure 6.33.

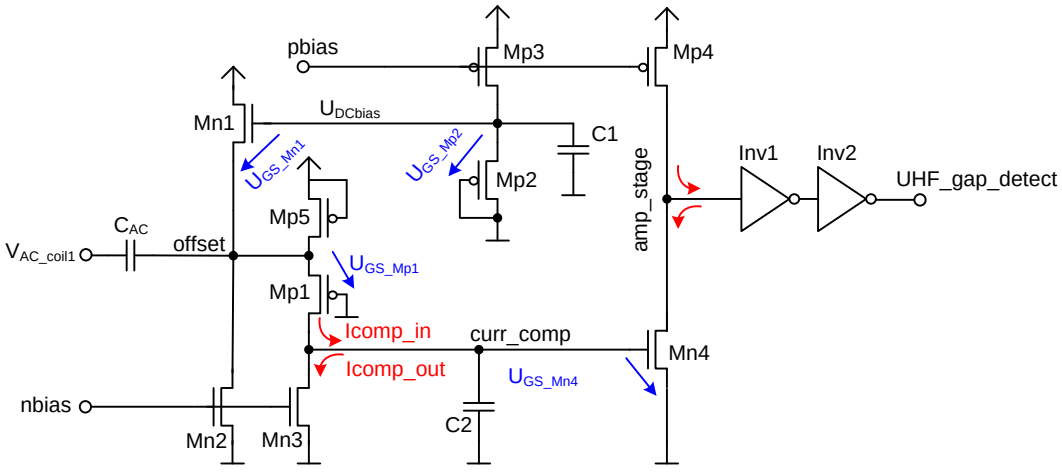


Figure 6.33: CTS UHF demodulator

- DC bias generation
  As already mentioned, the DC point recovery is necessary after capacitive coupling. Mn1 is a source follower and is able to deliver much current into node $offset$ when U_{GS_Mn1} is bigger than 520mV. In this case, current from the internal power supply is handed over to the source of Mn1 and the voltage will not drop to a lower potential anymore.

$$\begin{aligned} U_{offset\_min} &\approx U_{Vth\_Mp2} - U_{Vth\_Mn1} - V_{overdrive} \\ &\approx 750mV - 520mV - 100mV = 130mV \end{aligned} \tag{6.41}$$

  The gate potential of the source follower is defined by the current biased PMOS transistor Mp2, which is switched as a diode in forward direction. Mp2 and Mp1 have the same geometry and, therefore, technology variations and temperature drifts are compensated in the threshold voltages. This will finally purge two absolute voltage errors and surrender in a more robust design. A source follower reduces the voltage headroom by one threshold and it also provides a maximum peak voltage limitation at the oscillating node $offset$.

$$U_{offset\_max} \approx VDD + U_{GS\_Mp5} \approx 1.2V + 500mV = 1.7V \tag{6.42}$$

  Clamping of positive voltages will not occur because a value of 100fF for capacitor C_{AC} already represents a capacitive voltage divider with parasitic capacitors at node $offset$. The amplitude of this coupled node is about 35% less than $V_{AC\_coil1/2}$ in normal operation. A DC sweep of node $offset$ is shown in graph 6.34. The static switching points of the current comparator node $curr\_comp$ and the output of the RxD unit are also shown in figure 6.34.

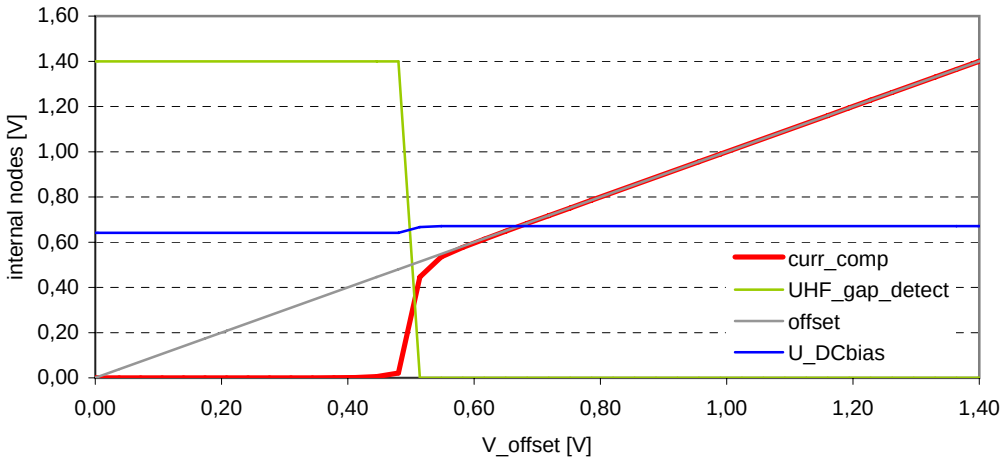


Figure 6.34: DC sweep of node $offset$ and current comparator reply

If the node potential $offset$ drops below 520mV, the current through Mp1 gets smaller than I_{Mn3} and finally, the output shows LOW at node UHF_gap_detect.

- No gap occurs - normal operation
  Mp1 senses the potential at its source and amplifies small voltage changes into big amplitudes in the current domain according to transistor gm_{Mp1}. Mp1 is also the current source

of current mirror node $curr\_comp$ with Mn3 as constant current sink. If the voltage at node $offset$ is bigger than one thin oxide transistor threshold voltage + overdrive voltage, Mp1 conducts well and $curr\_comp$ is pulled up. This causes a well conductive transistor Mn4. This is already the comparator input stage and part of the first amplifier stage. The second stage of the comparator with node amp_stage is a weak but symmetric inverter and toggles at $VDD/2$ potential. The second inverter $Inv2$ amplifies the signal and finally forces a LOW at the output signal UHF_gap_detect.
Low pass Mn3//Mp1 and C2 reduces the noise at node $curr\_comp$ and helps to separate contactless data from air interface noise and power supply noise. As in HF operation, the absolute delay of detecting the rising or the falling edge could cause analog detuning of the front-end or a failure in the digital decoder. Thus, mixed-signal simulations are recommended to guarantee a robust analog - digital interface.

- Gap occurs
  When the electrical field is reduced by the reader, the antenna voltage $V_{AC\_coil1/2}$ is also reduced linearly. As the modulation depth is always bigger than 80%, the potential at node $offset$ should also get smaller by the same factor. However, the peak potential of node $offest$ is smaller than the threshold voltage of Mp1, so after a short delay the current comparator node drops to LOW. This is a well-defined input signal for the comparator Mn4/Mp4 and the output signal UHF_gap_detect gets HIGH.

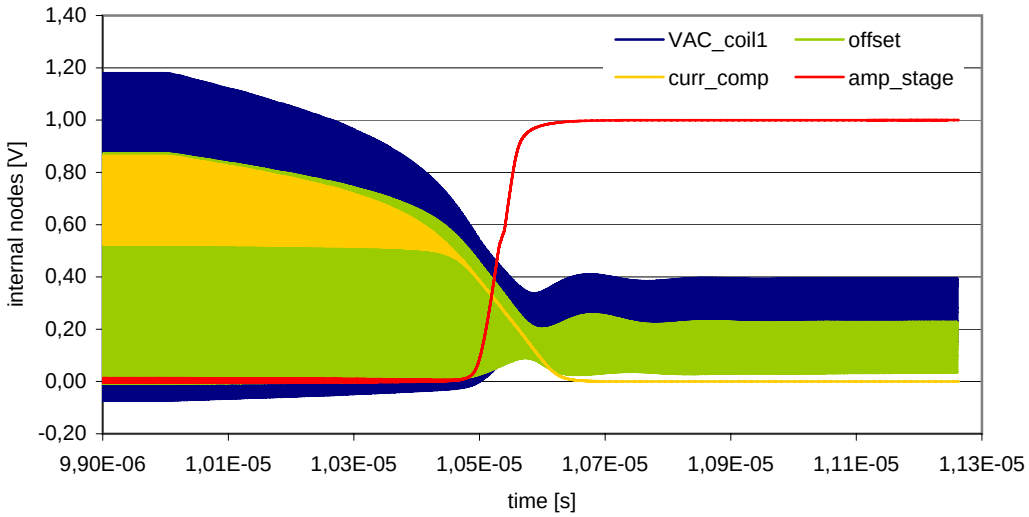


Figure 6.35: Start of an UHF gap in moderate field strength conditions

The demodulator average current consumption is about 500nA; the minimum VDD power supply voltage lies at about 0.85V.

6.6 Measurement Results and Layout

With the help of several test pads, individual module signals are routed to the chip boarder. There, level shifter structures with strong buffers are implemented to deliver sharp signal edges even at a load capacitor of 10pF, which is typical for an oscilloscope probe.

RxD - HF

In figure 6.36, an ASK signal with a field-strength modulation index of 8% is shown. The measured modulation depth is even lower because of a non ideal external voltage limiter regulation behavior. Nevertheless, the sensitive detection method with its two comparators is able to recognize even this signal with a typical delay of 1.5µs. The effective modulation depth at the two coil

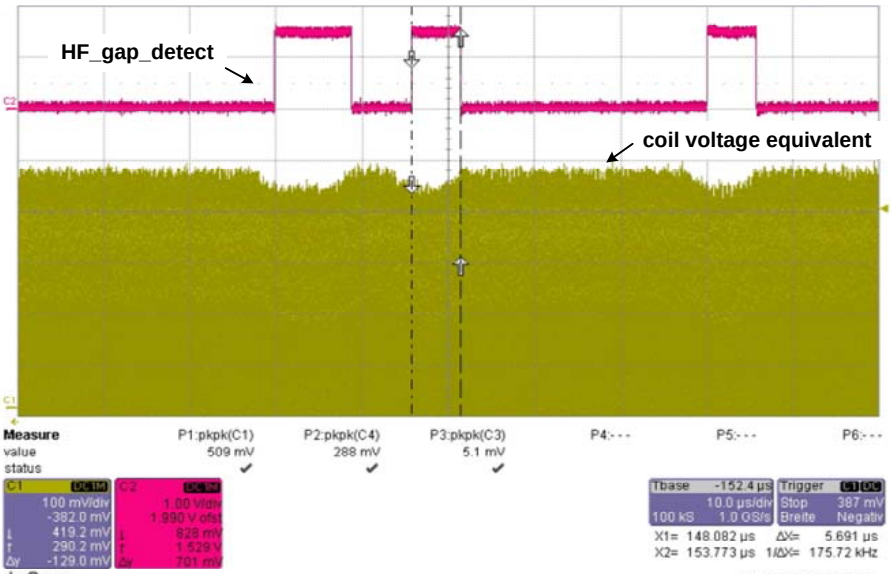


Figure 6.36: 10% modulation index response of the HF demodulator

pads - which is also the information source for the HF demodulator - can vary with the type of coil, absolute field-strength or demodulator speed. Naturally, the more clearly the gap is embossed, the easier it is to detect the information.

100% ASK gaps can also be handled with this type of decoder. In comparison with the UHF demodulator, increased power consumption is the major drawback to be accepted for a higher sensitivity and flexibility of this demodulator architecture. Sometimes - e.g. in EPC UHF mode or ISO14443 Type A - this sensitivity is not desired because of the considerable deep field strength modulation (down to 100%).

RxD - UHF

In figure 6.37, a start-up of internal VDD can be seen when the power is applied to the rectifier in the middle of this picture. At the bottom of figure 6.37, a zoom region shows the UHF demod-

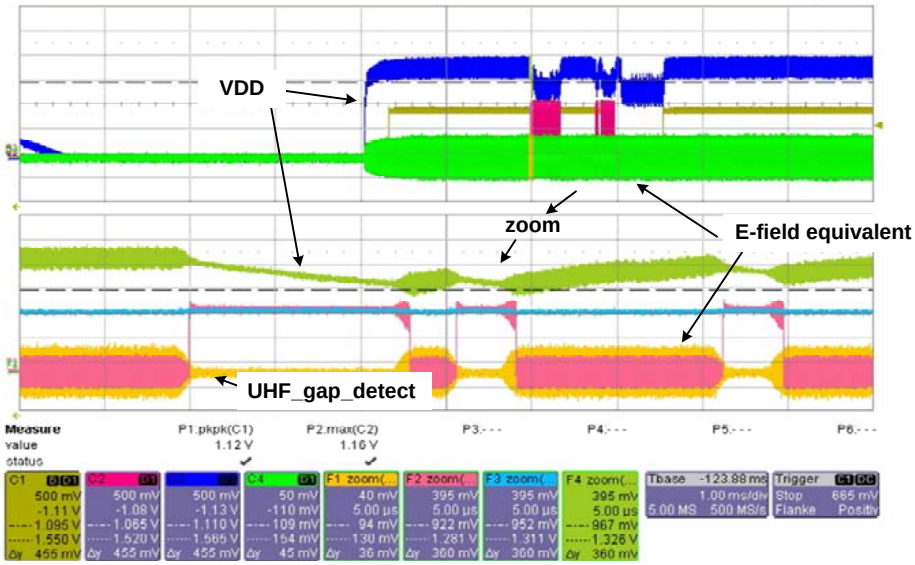


Figure 6.37: Response of the UHF demodulator on field strength variations

ulator gap response. When the UHF power declines, the detector rises the signal gap_detect in between 1µs to its active HIGH state.

RxD - layout

The confusing alignment of HF and UHF demodulator branches has historical relevance derived from the 1.st tape-out. Some design modifications were necessary for the 2.nd tape-out but the layout floorplan was not changed any more. Also the distributed UHF demodulator layout is the result of a redesign. Total area of both detectors: $\approx 0.017mm^2$

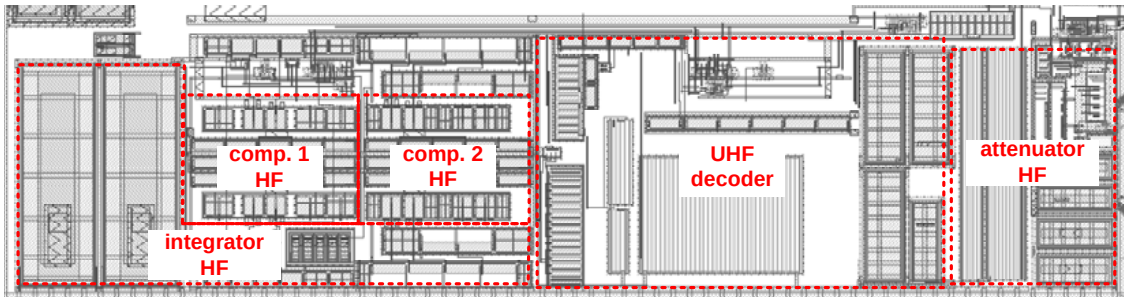


Figure 6.38: HF and UHF decoder layout - the lowest two metals are routed

TxD - HF

HF load modulation sequence is shown in figure 6.39. This measurement was recorded at weak field-strength conditions. In the lower half of the picture two zoomed load modulation pulses are shown. With the fast regulation loop, coil voltage declines to a certain peak voltage still big enough to have an operative HF clock recovery. Rising edges of these pulses are slower than

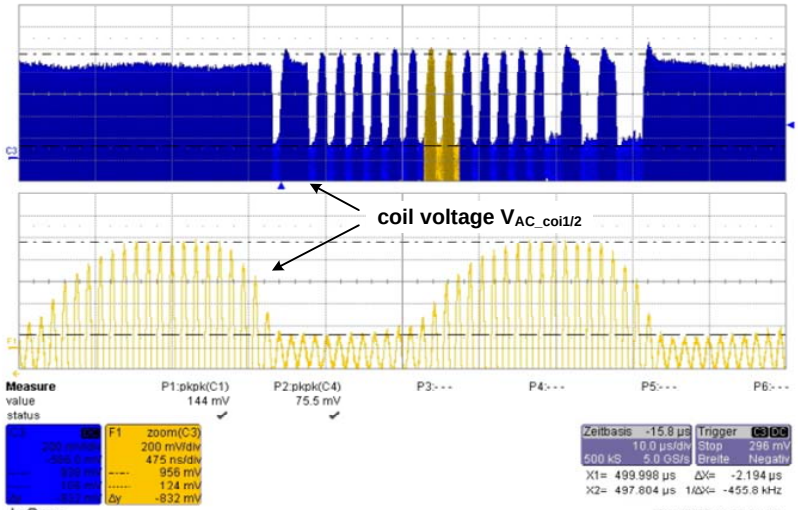


Figure 6.39: Load modulation response of the coil voltage $V_{AC\_coil1/2}$

the slope of falling edges. A reduced bandwidth caused by an increased quality factor Q is one of the reasons for the smoother rising slope. Another reason is the additional amount of charge that is delivered from the coil to the internal power reservoirs via the rectifier.

After each load modulation, small overshoot spikes are triggered by the shunt regulator. During the rising edge the shunt regulation loop reduces the load current through the shunt transistor which is located between the RF pads. This load current reduction has to be compensated after the final coil voltage has been reached by the shunt once again. As the low power regulation loop is not fast enough, an overshoot occurs, as seen in graph 6.39.

TxD - UHF

A method of testing the UHF back-scattering of the chip is to short circuit the local oscillator with the back scatter unit. As both modules and their input/output signals are accessible from external (via a plastic package), the corresponding pins are shorted and the result can be seen in figure 6.40. This is also a method of to measure the oscillator frequency galvanic decoupled. In this case, the local oscillator frequency is $\approx 1.7MHz$. With this configuration, the minimum

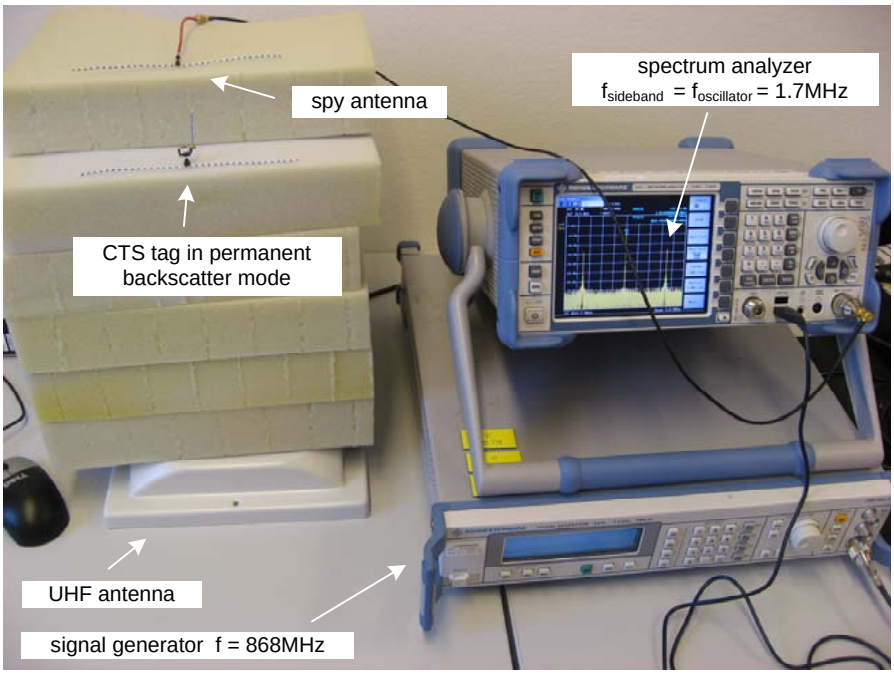


Figure 6.40: One way to measure the internal oscillator frequency is to operate the TxD backscatter unit straight with the LO

electrical field-strength or the maximum operation range can be easily verified. This configuration is also used to check the performance of different antennas.

Application

In picture 6.41, the CTS transponder (on the right side of the picture) is between the HF and UHF reader antenna. This setup is the actual CTS demonstrator setup. At each antenna a local laptop shows the communication status and communication performance between the reader and the transponder. In this application configuration, the UHF field is strong and the HF reader far away (3.5m) from the tag. The tag clearly chooses the UHF field as communication medium and only the communication rate counter number at the UHF laptop increases.

Figure 6.41: HF reader antenna (left side) and UHF reader antenna (in the background). In between the CTS transponder

7 Secondary Units and AFE Top

7.1 Bias current generation

Bias current generation and voltage reference circuitry are attached to the internal power supply VDD. On the CTS chip no electrical circuit requires a precise absolute current or a precise voltage value. Because of this relaxed requirement a beta-multiplier [Bak07] will generate the reference current value instead of a more precise bandgap reference circuit. An analog startup circuit

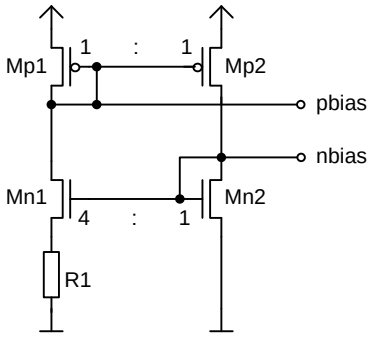


Figure 7.1: Standard beta-multiplier circuit for good power supply rejection

attached to the beta-multiplier increases both bias currents during startup. This helps to settle stable operation points of various modules after the startup. The bias current also supplies the power on reset module which is released after a short delay.

7.2 Voltage reference

Two stacked MOS diodes and the current coming from the beta-multiplier current source are used as ”reference” voltage $Vref$. Voltage level stability can be forced when the CTAT behavior of the MOS transistor threshold voltage is compensated by a PTAT current [Bak07]. The effort for such a compensation scheme can help to reduce the spread but, after all, $Vref$ will never have the quality of a bandgap regulated circuit. The stochastic parameter spread during the production phase shows the weakness of this concept.

condition	Vref value
slow-speed, -20℃	930mV
fast-speed, 110℃	785mV

Table 7.1: Simulation results for $Vref$ at its worst case temperature and technology split corners

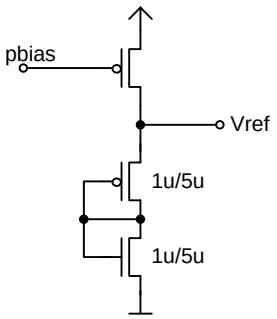


Figure 7.2: Reference voltage generation

7.3 Power up/down reset module

A reliable function is the most important feature of a power-on reset circuit. It has to start correctly without any knowledge about the absolute reference current or voltage values. As the beta multiplier will start with its startup circuit it will provide about 50nA after 200ns delay. The beta-multiplier starts working already at 550mV but the thick oxide transistor Mn1 with a threshold voltage of 850mV will not conduct. Then, node U_{ini} is pulled up via the 50nA current source close

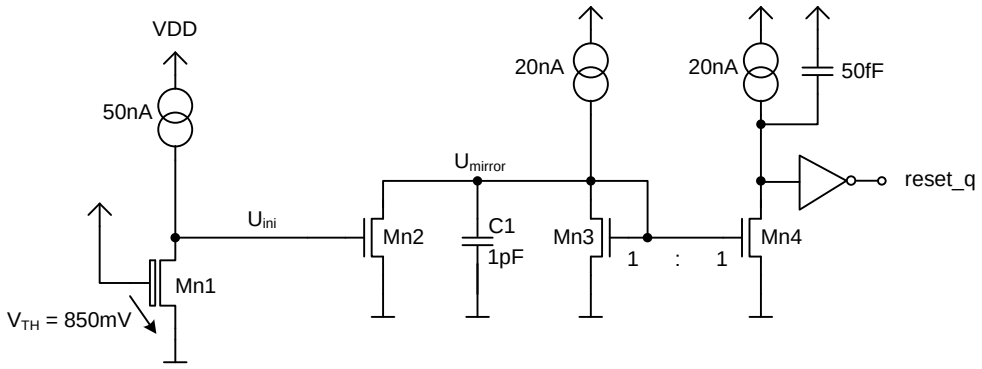


Figure 7.3: Power Up/Down reset with unidirectional lagging

to VDD potential. Thin oxide transistor Mn2 conducts well and no current is mirrored to Mn4. 20nA current charges the 50fF capacitor C2 and the input capacitance of inverter Inv1. Next, the output $reset\_q$ switches to LOW. When VDD exceeds the threshold voltage of Mn1 of about 850mV, node U_{ini} is pulled down by Mn1 and Mn2 does not conduct any current anymore. C1 is charged slowly by 20nA. This span of time should guarantee that all units which are controlled by the reset signal have enough time to settle. The charging phase is stopped by diode Mn3 and mirror Mn3. Then, Mn4 starts to sink current in front of the inverter. 40nA pulled by the active mirror transistor Mn4 and a permanent source current of 20nA finally result in a 20nA sink current which discharges C2 and the input of the inverter Inv1. The reset signal $reset\_q$ toggles

to its not active state - to HIGH when the level at the inverter input is smaller than VDD/2. If the core power supply voltage VDD drops down below 850mV. Mn1 gets high ohmic and Mn2 will discharge C1 quickly. Then the current mirror sinks no current any more, C2 gets charged with 20nA and signal $reset\_q$ toggles much faster from HIGH to LOW back again and all modules are in their reset mode.

7.4 Measurement results

Start-up of the internal oscillator in UHF operation
During start-up it is necessary for the local oscillator to start when the bias generator delivers enough bias current. If the chip is operated at the lower UHF power limit of -10dBm, the chip starts in the power bypass mode and VDD rises. In this bypass mode, enough power and volt-

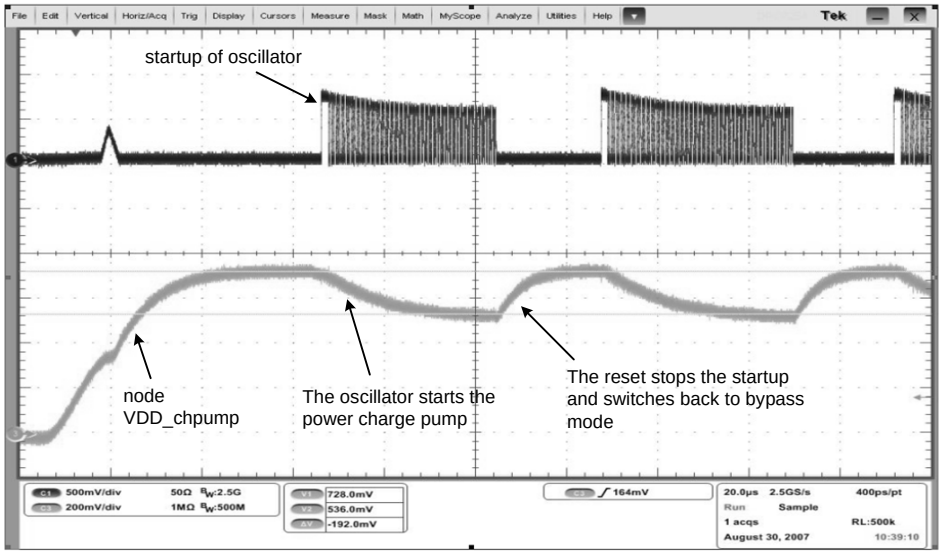


Figure 7.4: Impact of the power down reset on the local oscillator in weak UHF field

age is available for a proper oscillator operation. In figure 7.4, the oscillator starts to operate after a delay and current is transported from VDD_chpump to the internal VDD via the internal charge pump. In this case, the external and the internal power supply drop and the power down reset level is reached. In the reset state the chip is once again in a startup condition and the serial regulator is switched into bypass mode. The local oscillator is stopped, the total power consumption declines and the power supply voltage VDD_chpump rises again.

Star-tup UHF
In figure 7.5, the UHF reader starts to deliver power to the chip. The internal power supply nodes $VDD\_rectifier$ and VDD rise during the first phase of the bypass mode. After the release of the reset signal, the DC/DC charge pump starts to work and pushes VDD to 1V. As in this case the delivered UHF power is close to the minimum power limit of -8.5dBm, the $VDD\_rectifier$ power supply level is only 700mV.

Startup HF
When the HF field is applied to the chip, once again the start-up is active in the first phase as shown in figure 7.6. After the start-up phase, the serial regulator releases node $VDD\_rectifier$ to a higher potential of about 2.4V.

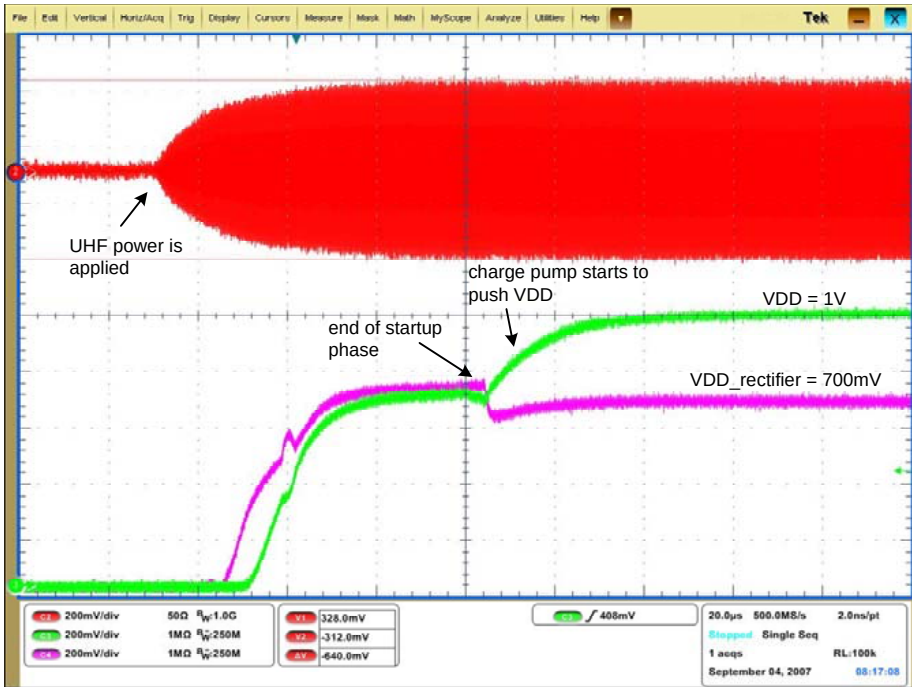


Figure 7.5: Start-up when minimum UHF power is applied to the tag antenna

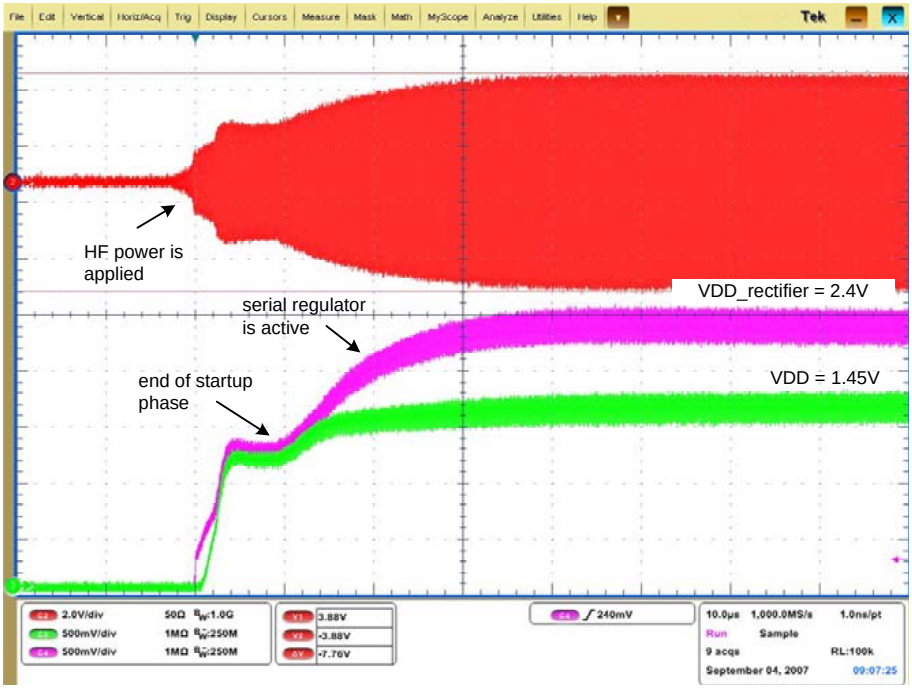


Figure 7.6: HF field of 1A/m is applied to the tag antenna

7.5 Top schematic

The analog top schematic in figure 7.7 shows the top hierarchy of the CTS front end. All units described in the previous chapters are shown again in this CTS top view. Bias current generation unit $BIAS\_Iptat\_vth\_V01$ is a shared module which was also used in other CTS projects [Kla09]. The HF clock prescaler and test pads with their corresponding level shifters are miss-

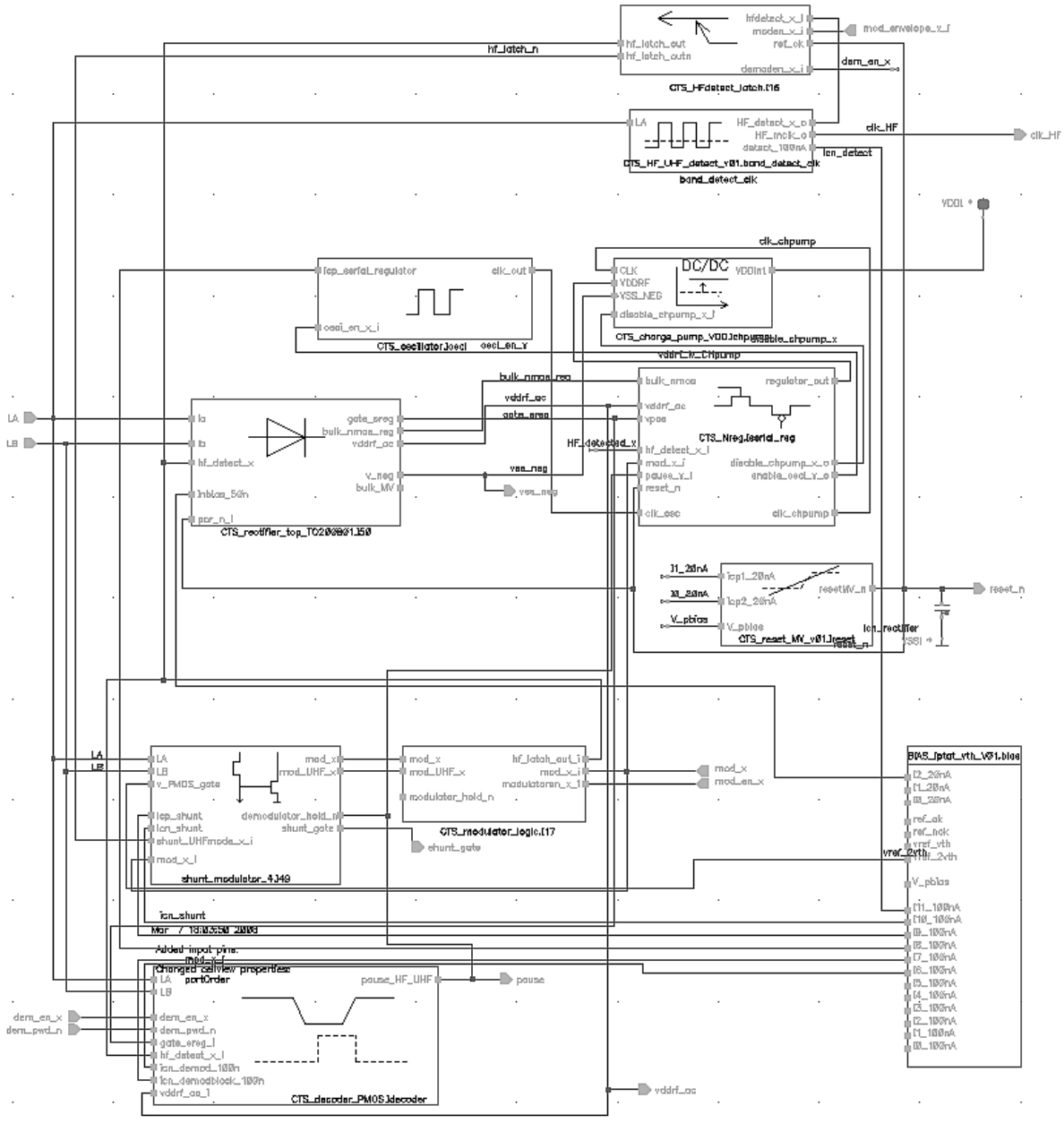


Figure 7.7: CADENCE CTS top schematic view

ing in this chip top view. In this schematic, coil/antenna pads are named LA and LB which corresponds to $V_{AC\_coil1/2}$ used in this thesis.

8 Research Summary and Outlook

An analog front end for a multiple frequency selective RFID transponder was designed and verified. The latest EPCglobal HF and UHF standards were chosen as air interface protocols. The chip was manufactured in a low cost 120nm CMOS Infineon EEPROM technology process. A measured minimum field-strength of 35mA/m is a very competitive HF performance value compared to commercial HF single frequency transponders. For a proper UHF operation, a minimum measured power level of -8.5dBm is necessary at the two plastic package antenna terminals where the chip is bonded. It was shown that the UHF performance could be improved to -12dBm when using thin oxide transistors instead of thick ones. The presented and implemented RxD units support all data rates which are specified in the EPCglobal documents. One transistor at the antenna/coil interface operates as shunt, load modulator and backscatter element, which reduces the chip size provides sufficient HF sideband voltages and big backscatter signals.

Since September 2008 functional CTS demonstrator, vested with an HF and UHF selective antenna, together with the presented CTS chip have proven advantage of a dual frequency selective transponder used in an RFID application.

8.1 Conclusions

This is the first EPCglobal chip which supports contactless operation in both the HF and UHF frequency bands. In the course of the thesis, the following three new architectures and designs were developed in order to achieve a well working multi frequency RFID analog front end. The developed designs are protected by 4 patents and were presented at 5 international meetings and several local workshops.

- **Power generation unit**
  An uncommon balanced rectifier architecture was chosen for the CTS antenna to chip interface. This type of rectifier is typical for HF systems but not usual for UHF chips. Only a few rectifier transistors and some secondary MOS diodes are attached to the RF signal. In a typical UHF product, the voltage charge pump is directly attached to the UHF antenna terminals. In the CTS project, the charge pump is powered by the rectified DC voltage and controlled by the local oscillator. The pump shows an efficiency of 65% at 600mV power supply voltage which is far above that of a typical UHF charge pump. The low power oscillator generates a clock frequency of 2MHz at a power supply voltage of 550mV. This good performance with is close to the transistor threshold voltage can only be archived with the help of a secondary negative charge pump which is delivered by the CTS rectifier. This circuit arrangement is described in Chapter 3.6 and in the US patent ”Voltage Converter” [Mis07]. This type of power interface can be used for RFID applications from LF up to

2.45GHz.

To reduce parasitic junction capacitors at higher frequencies to the resistive loaded substrate, another invention disclosure was written. The idea was, to have only one NMOS transistor which performs as voltage limiter (shunt), as load modulator and as backscatter device [KHK+08]. During the disclosure phase, an overlap of a new invention from the company NXP was detected [BBS06] [Kla09].

- **Local oscillator**
  In general, UHF RFID chips use an internal local oscillator as clock source. Low power and low voltage oscillators with good power supply rejection are required. After extensive research on previously published clock generator architectures, a new relaxation oscillator architecture was introduced [MKP+08]. The frequency is in the first oder independent of bias current and power supply voltage variations and it is dominated by passive R and C components. Used as current controlled oscillator in a PLL, the oscillator was published in [KMP+08] and compared with several other oscillator architectures.

- **Contactless communication units**
  TxD
  As only one shunt transistor is used and a modulation via big parallel MOS diodes is unreasonable, the load modulation modules needs a precise and fast regulation unit. This new architecture drives the power amount for the fast regulation unit directly from the contactless field. The modulation depth is reached during one clock cycle and no undershoot occurs. This design concept was presented at two technical meetings [MKP+08] [MKH07].

  RxD
  For the reader to transponder RxD communication, two power consumption and operation point optimized demodulator units are implemented. Especially the UHF demodulator shows a novel architecture for recognizing EPC conform modulation signals. An invention disclosure was written about selecting the right decoder or about the adjustment of modules according to the detected frequency band [MHK+08].
  In the CTS project, a shunt current related demodulator is also used. A new module to reduce the dynamic in the current was developed and introduced in the thesis of Christian Klapf [Kla09]. For this work an invention disclosure [MK07] was written.

In figure 8.1, the chip layout is fragmented into the digital state machine and analog modules. The total area of the analog front end is $\approx 0.155mm^2$. Some of the test pads are bonded to an 8 pin package. Finally, the package is soldered onto one of the CTS antennas which were developed during the project phase. The displayed antenna shows the favored CTS antenna which was developed and delivered by Lukas Mayer from Vienna University of Technology and is part of the actual CTS demonstrator [MS08a] [May09]. Other multi-band antennas are presented by [ITLS09] and [HPV+09].

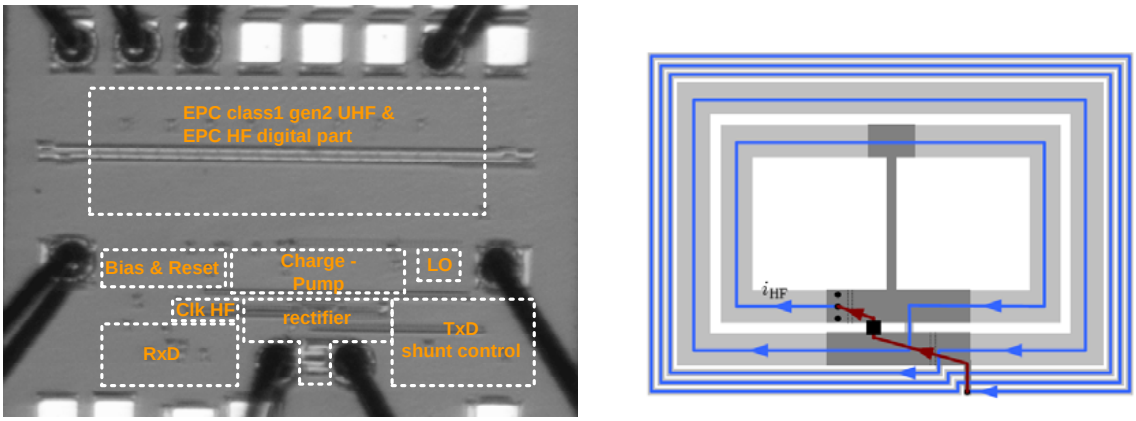


Figure 8.1: Bonded CTS chip with modules and CTS antenna with chip and HF current flow

8.2 Outlook

The 220nm testchip with different rectifier architectures has shown its potential when the presented CTS concept would be built with thin oxide transistors. The measured value of -8.5dBm for the CTS prototype turns out to be the biggest difference between current test chip measurements results and the aspired minimum power value of -12dBm. Moreover, at 8% the rectifier efficiency is smaller than the specified minimum value of 15%. To reach the power limit of a typical single chip sensitivity of -12dBm ... -15dBm, thin oxide MOS transistors are necessary (or even Schottky diodes). With the Infineon 220nm technology process and thin oxide rectifier test structures it was shown, that a sensitivity of -13dBm could be reached with the CTS equivalent power unit design.

Early 2008 a FIT-IT founded follow-up project $I - Tire$ was started. Several concept ideas from the CTS chip were reused in this new project. As the minimum power requirements were even tougher, the rectifier was constructed with thin oxide transistors and an additional energy harvester circuitry.

A Appendix

A testboard was manufactured to get a stable and reliable measurement set-up for the CTS testchip. Several baluns were tested to transform the unbalanced signal delivered by an external network analyzer to a balanced waveform. Schematic A.1 shows three different baluns right behind the SMA conductors. However, none of the integrated balun solutions achieved finally the

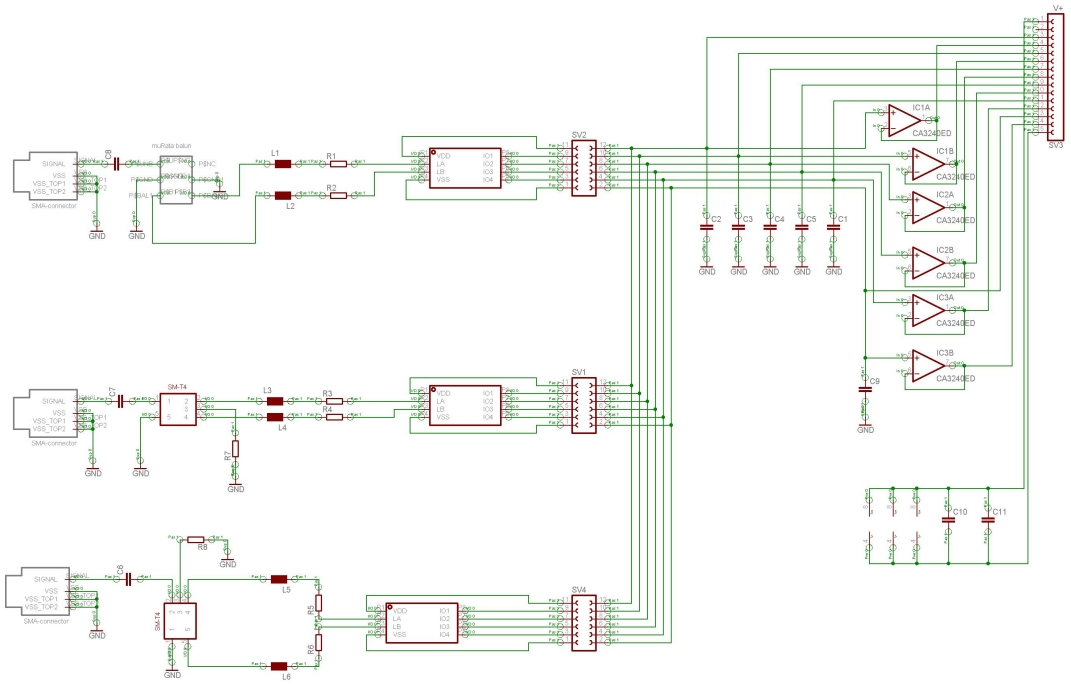


Figure A.1: CTS Testboard schematic

performance of a simple discrete matching circuit, as shown in figure 4.48.

The testboard was manufactured at the Institute of Electronics in Graz on a standard FR4 substrate. A photo of the sampled board can be seen in figure 4.49(b).

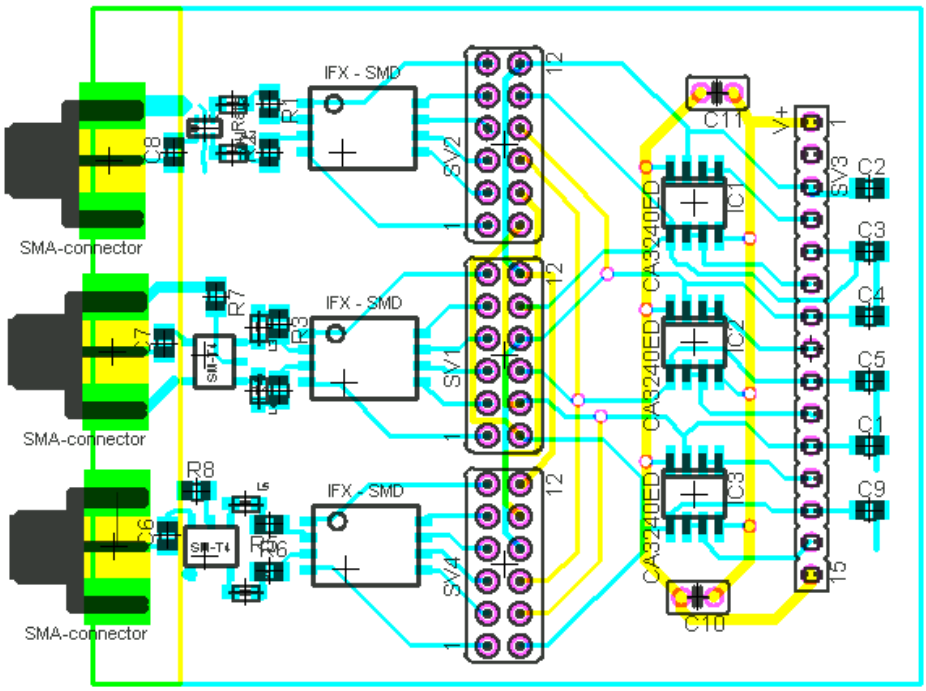


Figure A.2: CTS Testboard layout

Own Publications

Published papers and research articles

- Albert Missoni, Guenter Hofer and Wolfgang Pribyl. *A Frequency Band Comprehensive RFID TAG.* AACD 2010 - Workshop on Advances in Analogue Circuit Design, Graz, 2010.
- Albert Missoni, Christian Klapf, Wolfgang Pribyl, Guenter Hofer and Gerald Holweg. *A Triple-Band Passive RFID Tag.* ISSCC 2008, Session 15.2, San Francisco, USA, 2008.
- Albert Missoni, Christian Klapf, Wolfgang Pribyl, Guenter Hofer and Gerald Holweg. *A Multi Band RFID Tag.* C.7 Hardwareaspekte der Signalverarbeitung in RF Schaltungen, U.R.S.I Kleinheubacher Tagung 2008.
- Albert Missoni, Christian Klapf and Gerald Holweg. *Dual frequency comprehensive transponder with inverse load modulation.* EURASIP Workshop on RFID Technology RFID 2007, Vienna, Austria, 2007.
- Albert Missoni and Christian Klapf. *Transponderschaltungen fuer moderne RFID Systeme (RFID Transponderchips).* Forschungsjournal WS 06/07, 2007. Graz University of Technology.
- Christian Klapf, Albert Missoni, Wolfgang Pribyl, Guenter Hofer, Gerald Holweg, and Walter Kargl. *Improvements in Operational Distance in passive HF RFID Transponder Systems.* IEEE RFID 2008, Las Vegas, USA, 2008.
- Christian Klapf, Albert Missoni, Wolfgang Pribyl, Guenter Hofer and Gerald Holweg. *Analyses and Design of Low Power Clock Generators for RFID TAGs.* IEEE PRIME 2008, Istanbul, Turkey, 2008.
- Christian Klapf, Albert Missoni, Wolfgang Pribyl, Gerald Holweg and Guenter Hofer. *Inverse load modulation circuit concept for passive RFID transponder.* e&i Special Issue on RFID 12/2007.

Invention Disclosures and Patent Applications

- Albert Missoni, Gerald Holweg, Christian Klapf, Walter Kargl and Guenter Hofer. *Transponder circuit arrangement and method for operating a demodulator.* PATENT Application, April 17, 2007 (DE). German Patent Appl. No.: 10 2007 018 097.9, United States Appl. No.: 12/104,477, Pub. No.: US 2008/0258874 A1.
- Albert Missoni. *Voltage converter* PATENT Application, February 28, 2007 (DE). German Patent Appl. No.: 10 2007 009 838.5, United States Appl. No.: 11/687,816, Pub. No.: US 2008/0205105 A1.
- Albert Missoni and Christian Klapf. *Input current controller arrangement and method.* PATENT Application, February 8, 2007 (DE). German Patent Appl. No.: 10 2007 006 347.6, United States Appl. No.: 11/685,100, Pub. No.: US 2008/0192518 A1.
- Christian Klapf, Albert Missoni and Guenter Hofer. *Shunt regulation circuit.* Invention Disclosure, 2007. Reference No.: 2007E50085 AT.
- Christian Klapf, Albert Missoni and Guenter Hofer. *Transponder device and method for providing a supply voltage.* PATENT Application, April 13, 2007 (DE). German Patent Appl. No.: 10 2007 017 534.7, United States Appl. No.: 11/748,879, Pub. No.: US 2008/0252418 A1.
- Christian Klapf, Guenter Hofer, Walter Kargl, Albert Missoni and Gerald Holweg. *Apparatus and method for providing a supply voltage and a load modulation in a transponder.* PATENT Application, January 31, 2007 (DE). German Patent Appl. No.: 10 2007 004 843.4, United States Appl. No: 11/674,897, Pub. No.: US 2008/0180224 A1.

Supervised Diploma Thesis

- Lukas Perktold. *Design of a test configuration to verify a comprehensive transponder system* Project Thesis, Graz, University of Technology, Institute of Electronics, 2007.

Related Diploma Thesis

- Johann Heyszl. *System Research and RTL Design of a combined passive HF / UHF RFID Tag* Master Thesis, Graz, University of Technology, Institute of Electronics, 2007.

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