A Bulk Acoustic Wave based Ultra Low-Power Transmitter

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Kurzfassung

Platziert man das Sensormodul eines Reifendruckmesssystems (Tire Pressure Monitoring System - TPMS) auf der Innenseite der Lauffläche des Reifens, lassen sich zusätzliche wichtige technische Parameter messen. In dieser Arbeit wird ein neuartiger Sender für ein solches System vorgestellt. Die Herausforderungen sind groß: Das maximale Gewicht und Volumen des Sensors sind begrenzt, eine lange Lebensdauer der Stromversorgung muss erreicht werden und hohe Robustheit ist erforderlich um extremen Beschleunigungen standzuhalten. Durch die Verwendung eines Bulk Acoustic Wave (BAW) Resonators entfällt die Notwendigkeit eines großen stoßempfindlichen Quarzes und eines Phasenregelkreises (Phase Locked Loop - PLL). Dies macht das System robuster, reduziert die Anlaufzeit und verringert die Leistungsaufnahme. Der entwickelte Sender ist Teil eines 3D Chip-Stapels und daher wurden Problemstellungen durch die Verwendung von 3D-Integrationstechnik berücksichtigt. Neue analoge Schaltungen für die wichtigsten Schaltungsblöcke wurden entwickelt: ein BAW-Oszillator, asynchrone Teiler und ein Leistungsverstärker (Power Amplifier - PA) mit Anpassnetzwerk. Diese Schaltungen können in praktischen Implementierungen von Sendern verwendet werden und können helfen, die Performance zu verbessern und die Stromaufnahme zu verringern.

Ein zweistufiger BAW Oszillator, der sich die Parallelresonanzfrequenz zu Nutze macht, wird als Frequenzreferenz verwendet. Der vorgestellte Oszillator kann mit Hilfe von digital zuschaltbaren Kondensatoren verstimmt werden, um eine Temperatur- und Prozesskompensierung durchführen zu können. Die verbleibende Frequenzabweichung nach Ausführen des Kompensierungsalgorithmuses ist kleiner als ±150ppm. Der BAW kann auch mit einer variablen Gleichspannung, die für eine Modulation benutzt wird, verstimmt werden.

Neue Arten von asynchronen Teilern werden vorgestellt. Zum Beispiel ein asynchroner Frequenzteiler mit einem Teilerfaktor von 1,5, der für die Isolierung von BAW Oszillator und Leistungsverstärker (PA) verwendet werden kann. Durch die Teilung des Referenzsignals durch 1,5 treten Oberwellen des Ausgangssignals und die des Referenzssignals nicht bei der gleichen Frequenz auf.

Weiters wird ein neues integriertes Anpassnetzwerk vorgestellt. Die fast rein reaktive Eingangsimpedanz des rauscharmen Verstärkers (low noise amplifier - LNA) ist Teil eines Schwingkreises, der an die Antenne angepasst wird um die maximale Amplitude der Schwingung zu erhalten. Die höchste Spannungsverstärkung erhält man durch Anpassung der Antenne an die Verluste des Anpassnetzwerkes. Der Vorteil dieses Ansatzes liegt darin, dass dieser Schwingkreis im Sendebetrieb leicht an den Leistungsverstärker (PA) angeschlossen werden kann. Eine neuartige Schaltung zur Steuerung eines Klasse E Leistungsverstärkers (PA) wird vorgestellt. Das Tastverhältnis des Eingangsignals eines Klasse E Leistungsverstäkers (PA) hat einen starken Einfluss auf die Effizienz. Die vorgestellte Schaltung kann beliebige Tastverhältnisse erzeugen und verringert dadurch den Stromverbrauch.

Abstract

Attaching the sensor node of a Tire Pressure Monitoring System (TPMS) on the inner liner of a tire allows the sensing of important additional technical parameters. In this work, a novel transmitter for such a system is presented. The challenges are high: The maximum weight and volume of the sensor are limited, a long power supply lifetime must be achieved, and high robustness against extreme levels of acceleration is required. By exploiting a Bulk Acoustic Wave (BAW) resonator, the use of a bulky and shock-sensitive crystal and a Phase Locked Loop (PLL) can be avoided. This makes the system more robust, radically reduces the start-up time, and decreases power consumption. The proposed transmitter is part of a 3D chip stack and hence design issues when using 3D integration techniques were considered. New analog circuitry for the main building blocks was developed: a BAW oscillator, asynchronous dividers, and a Power Amplifier (PA) with a matching network. These circuits can be applied in practical implementations of transmitters and can help to improve performance and to decrease the current consumption.

A two-stage BAW oscillator which makes use of the parallel resonance frequency is used as frequency reference. The proposed oscillator is tunable to enable temperature and process compensation by means of digitally controlled capacitors parallel to the BAW resonator. The remaining frequency deviation after applying the compensation algorithm is lower than ±150ppm. The BAW can also be tuned with variable DC biasing, which is used for modulation.

New types of asynchronous dividers are presented. For example, an asynchronous frequency divider with a division ratio of 1.5 can be used to achieve isolation between the BAW oscillator and the PA. By dividing the reference signal by a factor of 1.5, the harmonics of the output signal and the harmonics of the oscillation signal do not occur at the same frequency.

Further, a new on-chip matching network is proposed. The almost purely reactive input impedance of the low noise amplifier (LNA) is part of a resonance circuit, which is matched to the antenna to obtain maximum amplitude of oscillation. The highest voltage amplification is obtained by matching the antenna to the losses of this network. The advantage of this approach is that this resonance circuit can easily be connected to the PA in the case of transmit mode. A novel circuit for the control of a class E PA is shown too. The duty cycle of a class E PA input signal has a large impact on efficiency. The proposed circuitry can provide arbitrary duty cycles and this reduces power consumption.

Acknowledgements

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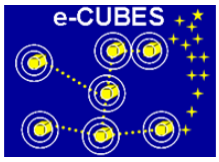


Contents

Nomenclature

µC	Microcontroller
ADC	Analog to Digital Converter
AlN	Aluminium-Nitride
ASIC	Application-Specific Integrated Circuit
ASK	Amplitude Shift Keying
BAW	Bulk Acoustic Wave
BER	Bit Error Rate
BVD	Butterworth-Van-Dyke
BW	Bandwidth
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CPFSK	Continuous Phase Frequency Shift Keying
CPU	Central Processing Unit
CU	Central Unit
DAC	Digital to Analog Converter
DCO	Digitally Controlled Oscillator
DMD	Dual Modulus Divider
DMP	Dual Modulus Prescaler
DR	Data Rate
E-TSPC	Enhanced True Single Phase Clocked
ESD	Electro-Static Discharge
FBAR	Freestanding Film Bulk Acoustic Wave Resonator
FIFO	First In, First Out
FM	Frequency Modulation
FoM	Figure-of-Merit
FSK	Frequency Shift Keying
FTR	Frequency Tuning Range

GFSK Gaussian Frequency Shift Keying

GMSK Gaussian Minimum Shift Keying

HBM Human Body Model

IC Integrated Circuit

ISM Industrial, Scientific, and Medical

LDS Laser Direct Structuring

LNA Low Noise Amplifier

LO Local Oscillator

M-ary FSK Multi-Frequency Shift Keying

MAC Medium Access Control

MBVD Modified Butterworth-Van-Dyke

MEMS Micro Electro-Mechanical System

MID Molded Interconnect Device

MMD Multi Modulus Divider

MMP Multi Modulus Prescaler

MUX Multiplexer

NCO Numerically Controlled Oscillator

NF Noise Figure

NIC Negative Impedance Converter

NOB Number of Bits

PA Power Amplifier

PCB Printed Circuit Board

PDE Partial Differential Equation

PLL Phase Locked Loop

PPF Polyphase Filter

PTAT Proportional to the Absolute Temperature

PVT Process-Voltage-Temperature

Q Quality Factor

RAM Random Access Memory

RF Radio Frequency

RIE Reactive Ion Etching

RKE Remote Keyless Entry

ROM	Read Only Memory
RSSI	Received Signal Strength Indicator
RX	Receiver
SAW	Surface Acoustic Wave
SBB	Stud Ball Bumping
SCL	Source-Coupled Logic
SEM	Scanning Electron Microscope
SFR	Special Function Register
SiP	System in Package
SMR	Solidly Mounted Resonator
SoC	System on Chip
SPI	Serial Peripheral Interface
TDC	Time-to-Digital Converter
TPMS	Tire Pressure Monitoring System
TSPC	True Single Phase Clocked
TSV	Through Silicon Via
TX	Transmitter
UTCS	Ultrathin Chip Stacking
VCO	Voltage Controlled Oscillator

1 Introduction and Background

1.1 The e-Cubes Project

The following chapter was mainly taken from [1, 2, 8, 14] (own publications). My contribution to this work comprises all building blocks belonging to the transmitter or to the BAW oscillator.

The objectives of the e-Cubes project are to advance micro-system technologies to allow cost-efficient realization of highly miniaturized, truly autonomous systems for ambient intelligence [16]. So the project addresses highly integrated systems, namely so-called independent sensor node applications. Characteristic properties of such nodes are sensor functionality, wireless communication capability (with each other or with a base station), and independence from external power supply. In the project three different applications have been examined: health and fitness, aeronautics and space, and automotive applications. This work is the result of the investigations into the transmitter used in the automotive demonstrator. The project setup of the automotive demonstrator is shown in Figure 1.1.

The target application of the automotive demonstrator is a tire pressure monitoring system (TPMS). State-of-the-art TPMS modules are wireless sensor nodes mounted on the rim (see Figure 1.2). Besides a sensor for pressure, the e-Cubes demonstrator also contains sensors for acceleration, temperature, and supply voltage. A typical

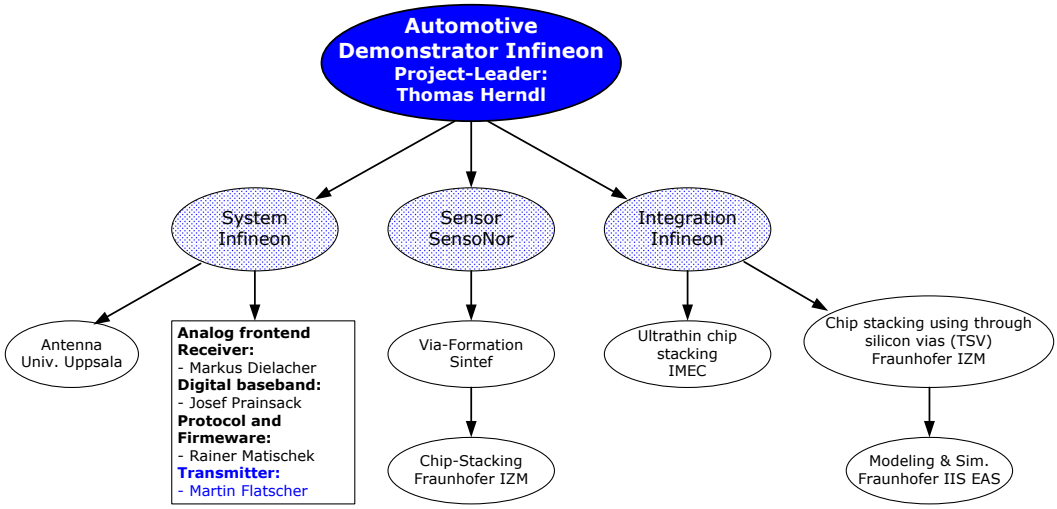


Figure 1.1: Project setup of the automotive e-Cubes demonstrator.

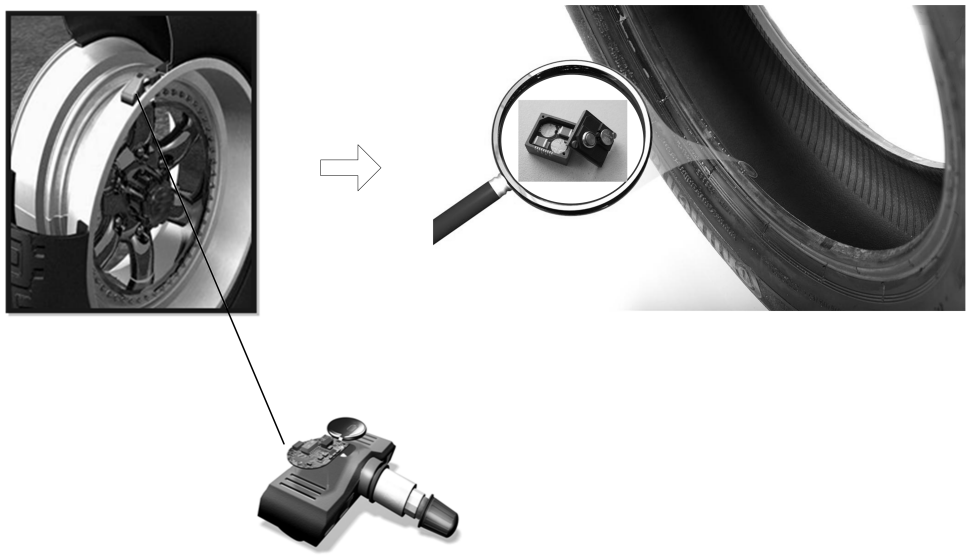


Figure 1.2: State-of-the-art tire pressure monitoring system (TPMS) mounted on the rim (left) and future tire mounted TPMS (right).

output signal of the acceleration sensor during two rotations of the tire can be found in Figure 1.3. As long as the module is moving around, a more-or-less constant negative acceleration can be measured. When the module enters the region where the tire tread has contact to the road, a spike occurs followed by an increased acceleration signal indicating the standstill of the module. When the module starts moving again, a second spike appears. From this acceleration profile the contact area of the tire can be calculated. Considering the known pressure and temperature of the air in the tire, the contact area can be used to approximate the vehicle load. Attaching the sensor node on the inner liner of a tire allows sensing of further important technical parameters, such as road condition, tire wearout, temperature, tire friction, side slip, and wheel speed. These may be used for improved tracking and engine control, feedback to the power train and car-to-car communication purposes.

Those new features come at a price: the maximum weight of the sensor is limited to 5 grams including package, power supply, and antenna. The node size is limited to about 1 cm³ to avoid high force-gradients due to device-deformation. Since the battery can only be changed with difficulty, a long power supply lifetime must be achieved. And, finally, robustness is required against extreme levels of acceleration. The static acceleration can be calculated using equation 1.1 [17]. $r_{\mathrm{wheelunit}}$ depends on the mounting location. For a tire dimension of 235/45 R17, acceleration reaches 2200g (g = 9.81 m/s²) when driving at 300 km/h. In addition, the acceleration coming from the road surface has to be considered.

$$a = r_{\mathrm{wheelunit}} \cdot \frac{v^2}{r_{\mathrm{tire}}^2} \tag{1.1}$$

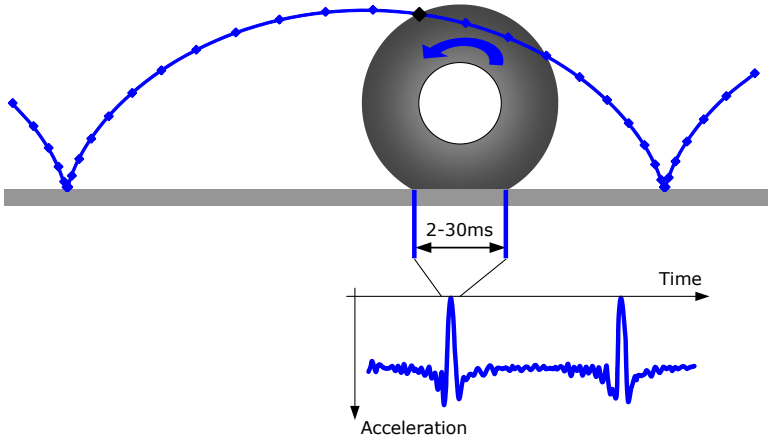


Figure 1.3: Acceleration profile of the tire mounted TPMS.

In such applications an individual identifier code and additional data payload are transmitted to a common receiver (RX) in the central unit (CU). Optionally the data transmission is repeated in order to increase the probability that the message is not disturbed by interference or other radio noise. To reduce the power consumption of the entire wireless network, the communication protocols have to be optimized for low-power operation because they have to operate self-sufficiently for several years.

Furthermore the power consumption of the wireless receiver system also needs to be minimized, since the receiver may be active for a long time. Therefore it has to be ensured that the receiver does not drain the battery. An efficient way to reduce the overall power consumption of the wireless communication system without decreasing the reception quality is to use duty cycling of the radio units. The basic principle is similar to the common "Low Power Listening" protocol [60]: The radio reception is activated for a short time followed by a longer period where the radio is in a power down mode and reception is disabled. During the reception period the advanced systems are first listening for a carrier; only in case of a detected signal do they keep listening for a specific header or preamble. The drawback of this duty cycled receiver protocol is that the acyclic transmitting sensor nodes have to send a longer preamble (increased overhead) to bridge the power down time gap of the receiver. Consequently the following trade-off has to be considered: on the one hand the power consumption of the receiver unit is reduced; on the other hand, the longer preamble comes along with increased power consumption for each transmission.

Energy saving by duty cycling with conventional low power radios is rather limited, since they are typically based on quartz crystal oscillators. The main limiting aspect is the start-up time of the crystal oscillator and the PLL which is typically in the range of ms [39, 38]. Using data rates of typical low-power wireless sensor networks (20 - 50 kbit/s [41]) the actual time for carrier sensing (or receiving a short preamble) is about 0.3 - 0.6 ms [41], thus the quartz crystal start-up time can become dominating. More details on duty cycling can be found in [10, 13].

In order to overcome these limitations, the presented sensor node utilizes a MEMS (micro electro-mechanical system) based radio architecture which allows for a significantly faster start-up of the oscillator. The radio uses a bulk acoustic wave (BAW) based oscillator, which achieves a start-up time of about 2 µs. This improves the overall power consumption [69] and is especially beneficial for duty cycled wireless sensor networks applying idle listening: A shorter start-up time can be used for a higher repetition rate with a constant duty cycle at the receiver. In this case a shorter preamble is required, which especially reduces the overhead and power consumption of the transmitting nodes. Another advantage of this configuration will be important for future wireless sensor applications: The shorter start-up time and shorter cycle time of the receiver allows for a significantly decreased message delay independent of the used MAC protocol, so it can be used for more time-critical wireless applications.

1.2 The 3D Integrated Sensor Node

The following chapter was mainly taken from [1, 2, 8, 14] (own publications). My contribution to this work comprises all building blocks belonging to the transmitter or to the BAW oscillator.

In Figure 1.4 a block diagram of the proposed wireless sensor node is shown, which consists of four different dies: a sensor, a microcontroller, a transceiver, and a BAW die. The sensor die is a bulk micromachined MEMS device containing sensors for pressure and acceleration. The sensor interface together with an ADC for converting the sensor data is integrated on the microcontroller die. Besides that, the microcontroller contains RAM, ROM, and a FLASH memory. It also provides additional sensors for measuring the temperature and the battery voltage. The communication with the transceiver ASIC is established via a serial peripheral interface (SPI). The BAW die includes four separate resonators, two of them are connected to two different oscillators and the other two resonators are used as filters in the receiver.

3D integration technologies have become a major topic in the semiconductor assembly industry, which are applied to result in a very compact system-in-package (SiP): The microcontroller, the transceiver, the sensor, and the BAW die are arranged in two different versions of 3D chip stacks using either through silicon vias (TSV) [26, 27, 28, 29, 30] or the ultrathin chip stacking (UTCS) method [31, 32]. The UTCS method has been used for the health demonstrator of the e-Cubes project; for the automotive application it was only a backup solution and was not the focus of the investigations. A picture of the 3D chip stack using UTCS is illustrated in Figure 1.5. This integration reduces the required connections to external components to a minimum and only very few additional wire-bonds are required. As shown in [74] the BAW technology is compatible with a standard integrated circuit (IC) process. Therefore it is possible to integrate BAW resonators above an IC. An example of the integration of BAW filters on top of a receiver front end is given in [73]. But SiP can

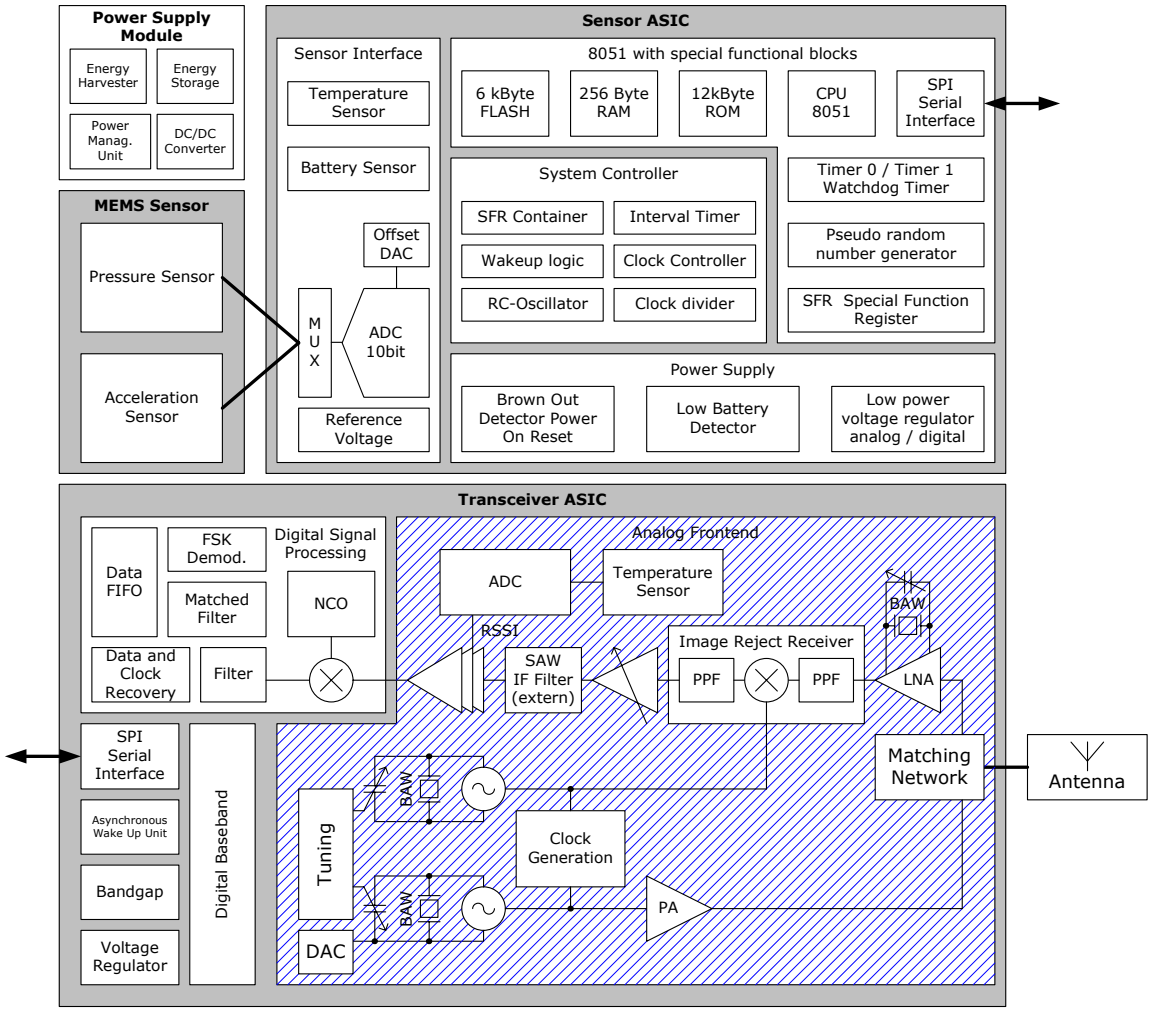


Figure 1.4: Block diagram of the sensor node.

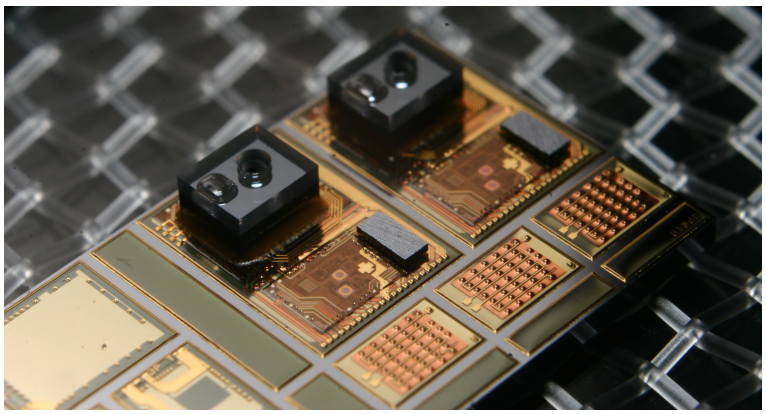


Figure 1.5: 3D chip stack using the ultrathin chip stacking (UTCS) method [31, 32].

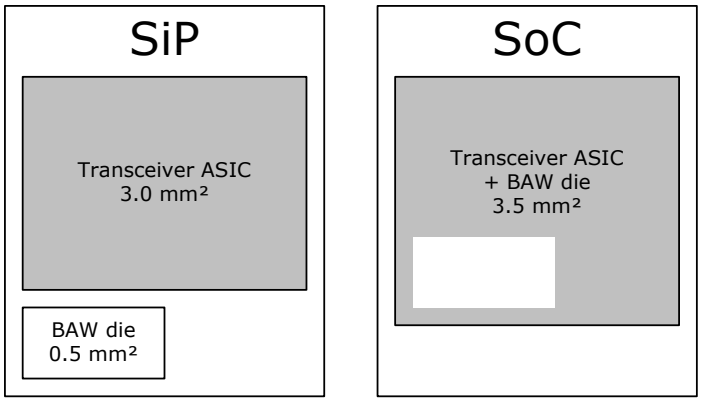


Figure 1.6: Comparison of system-in-package (SiP) and system-on-chip (SoC).

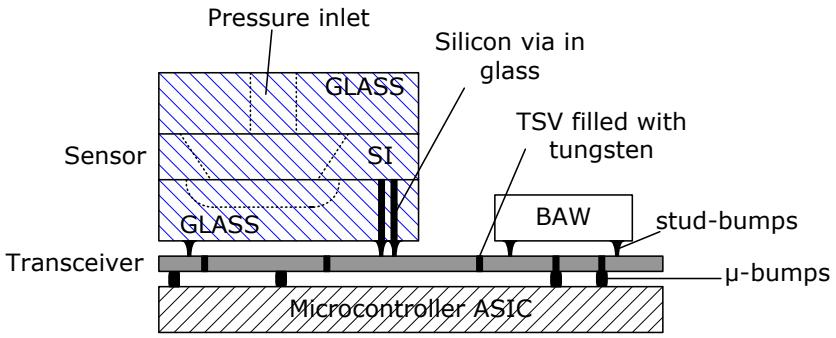


Figure 1.7: Sketch of the 3D ASIC stack using through silicon vias (TSV).

be advantageous in terms of price compared to a system-on-chip (SoC) implementation as shown in the example in Figure 1.6. A transceiver die with a size of 3 mm² and a BAW resonator die with a size of 0.5 mm² are combined to a SiP (Figure 1.6 left) and to a SoC (Figure 1.6 right). In chapter 4.5 on page 81 it will be shown that the yield of the BAW resonators is limited due to the requirement of a precise frequency. Assuming a yield of 80% and 10 required masks for the BAW resonator die and a yield of 95% and 25 masks for the transceiver ASIC a cost factor can be calculated as follows:

$$\begin{aligned} \text{cost factor} &= \frac{\text{number of masks} \cdot \text{area}}{\text{yield}} \\ \text{cost factor SiP} &= \frac{10 \cdot 0.5}{0.8} + \frac{25 \cdot 3}{0.95} = 6 + 79 = 85 \\ \text{cost factor SoC} &= \frac{35 \cdot 3.5}{0.8 \cdot 0.95} = 161 \end{aligned} \tag{1.2}$$

This approximation does not include the packing and bonding process, but shows a significant difference in the die costs of SiP and SoC. Even if the BAW resonator could be integrated on top of the transceiver ASIC, such that the total size would not be increased by the BAW size, a SoC implementation would not be competitive.

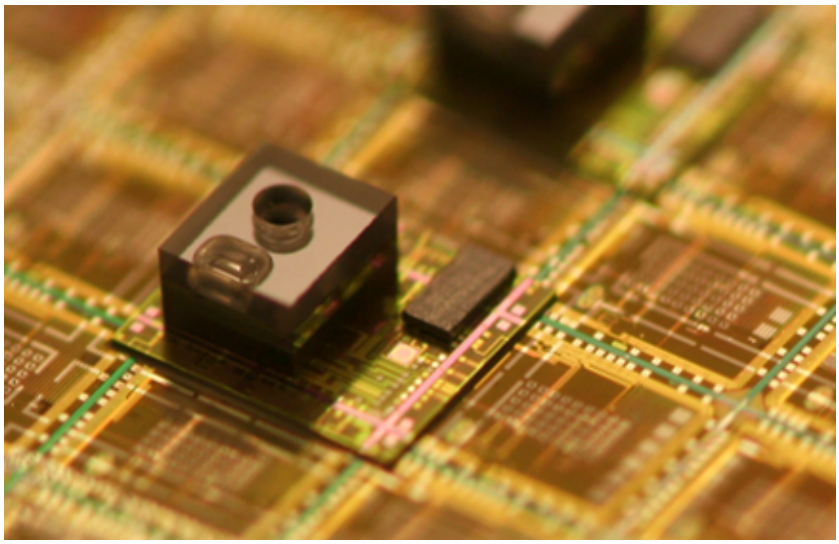


Figure 1.8: Photo of the 3D ASIC stack using through silicon vias (TSV) on wafer level (Source: SINTEF, Norway, [23]).

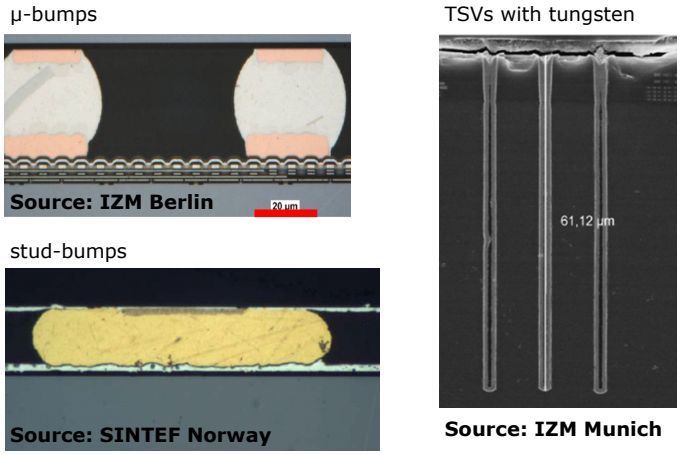


Figure 1.9: Photo of the µ-bumps, stud-bumps, and TSVs used as interconnects.

A sketch of the 3D integrated stack with silicon vias in glass in the sensor die and TSVs in the transceiver ASIC is shown in Figure 1.7. The MEMS based sensor and a BAW die, both flip-chipped, are stacked on top of the RF transceiver using gold stud ball bumping (Au SBB) [23, 24, 25]. The transceiver die is thinned to 50 µm and is connected to the microcontroller ASIC with a combination of TSVs and µ-bumps. A photo of the stack on wafer level, which shows the RF transceiver together with the MEMS sensor and BAW die on top, mounted on the microcontroller, is shown in Figure 1.8. Photos of the µ-bumps, stud-bumps, and TSVs are illustrated in Figure 1.9.

The AlSiCu redistribution layers on the topside and backside of the transceiver die are shown in Figure 1.10. The TSV array structure can be easily recognized next to the original bonding pads of the transceiver, but also within the pad ring at preferred

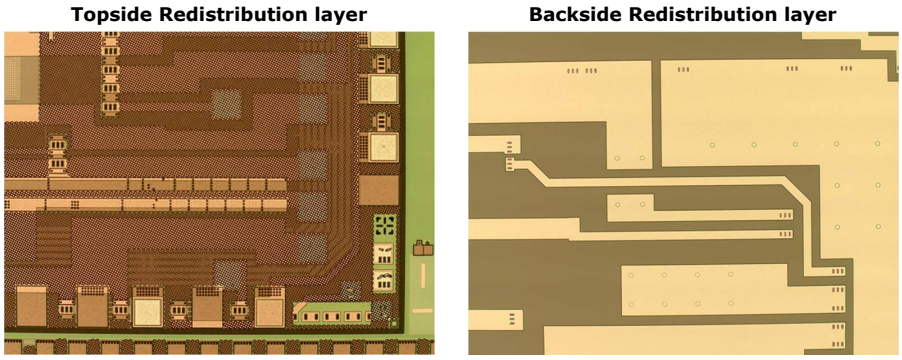


Figure 1.10: AlSiCu redistribution layer on the topside and on the backside of the transceiver.

locations. The redistribution has been realized in order to connect the TSVs to the original pads of the transceiver and to define new pads for attaching the pressure sensor and BAW devices by means of Au stud-bumps. Additionally a small number of pads for wire bonding have been defined, for instance the RF connection to the antenna.

Subsequently the metalized TSVs have been opened from the backside making use of different wafer-thinning technologies like grinding, spin-etching, chemical mechanical polishing (CMP) and maskless reactive ion etching (RIE). An additional AlSiCu redistribution layer and appropriate ground planes, as shown in Figure 1.10, have been realized on the backside applying a sputtering process. These planes provide shielding between sensitive blocks of the transceiver and the microcontroller ASIC. Additionally the supplies are connected in a star topology, preventing the ground currents from impacting each other. In total three ground planes are implemented, in order to separate analog, digital and RF sections. Furthermore TSV structures can be placed close to sensitive circuits anywhere all over the transceiver, which decreases the impedance to ground, and therefore the impact of noise and ripples caused by neighboring circuits is reduced. More details on miniaturization by means of 3D interconnects can be found in [8].

The whole ASIC stack is bonded onto a printed circuit board (PCB - see Figure 1.11) using chip-on-board technologies and standard soldering processes. Beside the ASIC stack, the PCB only contains a few external capacitors for the voltage regulators and some capacitors to bring the loop antenna, which is integrated into the package, to resonance. The values of these capacitors have to be adapted according to the operating frequency of the transceiver, which can be around 2.1 GHz or around 2.45 GHz depending on the assembled BAW devices.

The outer shape of the final demonstrator housing is a 3D substrate in MID (molded interconnect device) technology shown in Figure 1.12. An MID is a 3D plastic part which - after molding or milling - undergoes a selective surface metalization process

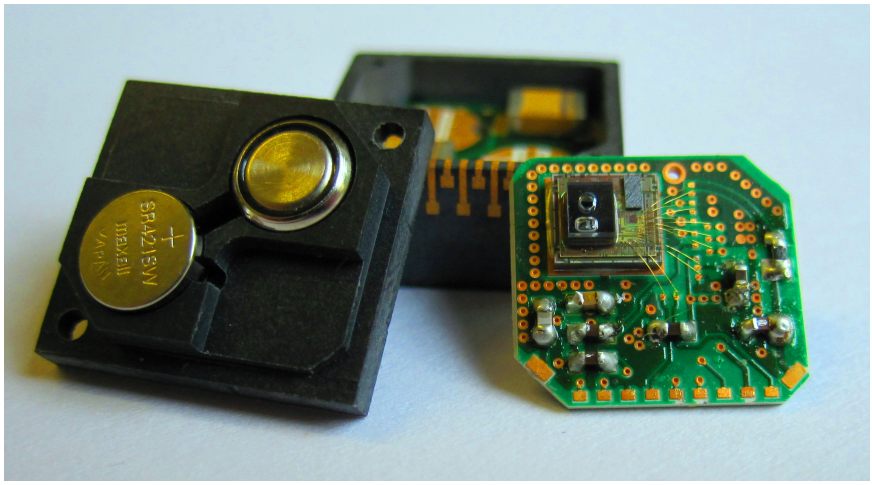


Figure 1.11: 3D ASIC stack mounted onto a PCB.

in order to create conductor lines as well as solderable and/or bondable pad surfaces. This is done by taking advantage of the laser direct structuring method (LDS): The surface of the plastic part is selectively activated by a laser beam making it susceptible for subsequent electroless CuNiAu-plating. The conducting line on the bottom of the MID cavity actually serves as loop antenna - one of the great benefits of using MID technology in the current sensor node application (see Figure 1.12). After assembling the PCB, which carries the ASIC stack, the PCB itself is electrically connected to the MID using a conductive adhesive.

In a first version a power supply module is used, which contains two small coin cells (CR416SW, 8 mAh) together with two capacitors. The capacitors are required because the batteries are not able to provide the required peak current. For this reason the batteries slowly charge the capacitors, which are then capable of delivering the peak current. These two capacitors are mounted onto the other side of the PCB, while the lid holds the two batteries. Connecting the batteries with a stamped metal spring makes up for unavoidable dimensional height tolerances. In addition, the lid does not need to undergo a complicated metalization process but can be manufactured as a simple plastic part. The whole sensor node is shown in Figure 1.13.

In a second version the lid of MID is replaced by an additional PCB carrying another power supply module. This power supply module consists of an energy scavenger, which converts vibrations into electrical energy, and a power management ASIC. Similar to the battery-driven version the energy is stored in large capacitors. The mounting location on the inner liner of the tire is beneficial for the energy scavenger because there is much more vibration energy available in that position than on the rim, where state-of-the-art TPMS are attached. The active microcontroller ASIC, fabricated in a 0.24 µm CMOS process, consumes less than 3 mA during data conditioning, event triggering, evaluation of the temperature compensation algorithm, and protocol stack handling. Only during measurement of pressure and acceleration can the

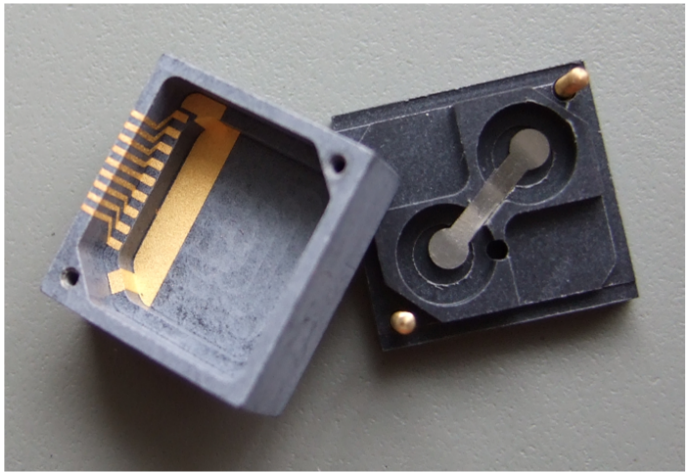


Figure 1.12: Molded Interconnect Device (MID) with circuit tracks on the surface.

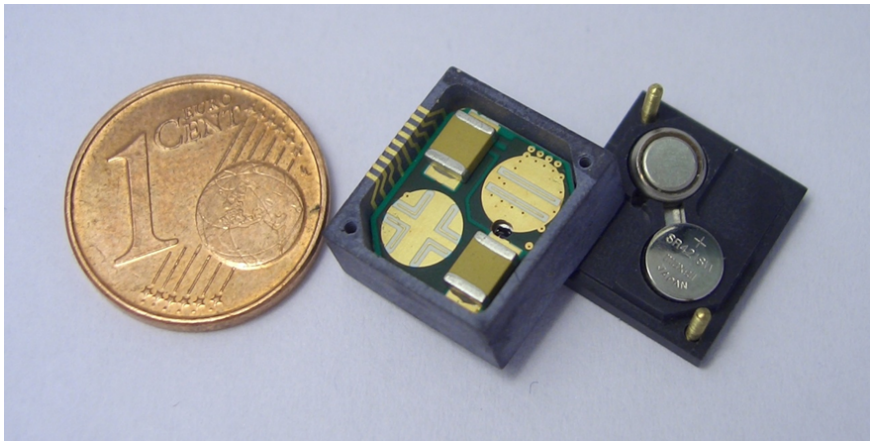


Figure 1.13: 3D integrated sensor node showing PCB assembled into metalized package and lid containing batteries.

current consumption rise up to 5 mA. Characterization has proven that the microcontroller as well as the transceiver ASIC can be operated in a temperature range from -40°C to 125°C. The transceiver ASIC has been fabricated using a 0.13 µm standard CMOS process. Its current consumption is 6 mA in transmit mode with a transmit output power of 1 dBm and 8 mA in receive mode with a sensitivity of -90 dBm (at a bit error rate of 10^{-2}) or -88 dBm (at a bit error rate of 10^{-3}) at a data rate of 50 kbit/s. The start-up time of the transceiver is shorter than 2 µs.

The duration of one complete reporting event is 7 ms, the total required charge is about 30 µC (current profile see Figure 1.14). Even when considering the worst case - one reporting event every 10 s (only required during alert, when the tire pressure is critical) - this contributes only 3 µA to the overall current. This contribution is even lower during normal, non-alerting operation with reporting periods of 30 s to 2 min. To obtain the overall current consumption, the power down current, mainly caused

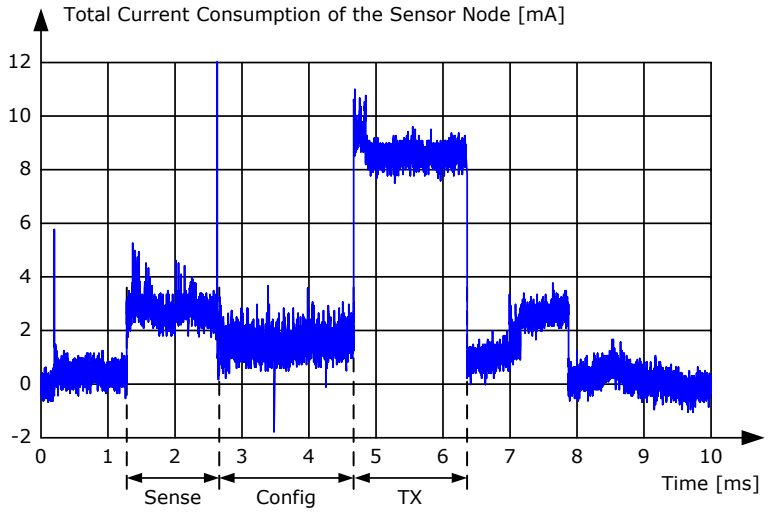


Figure 1.14: Current profile for one event, measured with a 10 Ω shunt resistor.

by the RC-oscillator in the system's wake-up unit (1 µA) and leakage of the employed monolithic ceramic buffer capacitor, has to be taken into account. The total current consumption is in the range of what the anticipated very low-weight, vibration-based MEMS scavenging system is able to deliver to attain full self-sufficiency of the wireless TPMS node. The key figures are summarized in Table 1.1.

1.3 The BAW-based Transceiver

The following chapter was mainly taken from [1, 2, 8, 14] (own publications). My contribution to this work comprises all building blocks belonging to the transmitter and to the BAW oscillator.

In Figure 1.15 the block diagram of the BAW based transceiver is presented, which uses BAW resonators with a size of only 0.02 mm² as frequency reference. By using BAW resonators the employment of a bulky and shock-sensitive quartz crystal and a PLL can be avoided. As already mentioned, this makes the system more robust and radically reduces the start-up time. The operating frequency of the transceiver is about 2.11 GHz or about 2.45 GHz depending on the assembled BAW device.

The chosen receiver structure is an image-reject architecture. An internal matching network, also containing the RX/TX-switch, feeds the incoming radio signal into a differential low noise amplifier (LNA), which also includes two BAW resonators for filtering purposes. The employed resonators are mirror-type BAWs, also known as solidly mounted resonators (SMR) [64]. Typically, the parasitic capacitances of the electrodes of such BAWs are not equal, since the bottom electrodes have a higher capacitance against ground due to their proximity to the substrate. It is therefore advantageous to use two BAWs, one in each branch of the differential LNA [7]. Since

Weight	<5g
Volume (12 x 13 x 6.4 mm³)	<1 cm³
Technology	
Transceiver	CMOS, 0.13 µm
Microcontroller	CMOS, 0.24 µm
Supply Voltage	
Microcontroller	2 - 3.6 V
Transceiver:	
in receive mode:	2.9 - 3.6 V
in transmit mode:	2 - 3.6 V
(all internal transmitter building blocks operate at 1.5 V)	
Current Consumption	
Microcontroller	3 - 5 mA
Transceiver:	
in receive mode (FSK, -90 dBm, 50 kbit/s):	8 mA
in transmit mode (FSK, 1 dBm):	6 mA
Oscillator core + biasing	900 µA
Power amplifier (1 dBm, 2.1 GHz)	3.5 mA
Overall peak current	<10 mA

Table 1.1: Key figures of the proposed sensor node.

the attenuation near the series resonance frequency of the BAW is very high, low side injection of the local oscillator (LO) signal leads to a high additional suppression of the image frequency, allowing for a low intermediate frequency (IF) of 10.7 MHz. Typically, the I- and Q-phases required for the image reject mixers are generated by the local oscillator. The applied BAW oscillator, however, does not provide quadrature phases because a quadrature oscillator would have a higher current consumption. This is why the I- and Q- phases are generated in the signal path by the polyphase filter (PPF) which follows the LNA. Because of the intermediate frequency of 10.7 MHz, the LO signal required for the mixers has a certain frequency offset with respect to the transmit frequency. Therefore a second oscillator has to be integrated, which is connected to a BAW resonator with a slightly different resonance frequency. After mixing, the IF signal is filtered and fed to a limiting amplifier with a gain of more than 80 dB. The limiting amplifier eliminates the need for an automatic gain control and delivers a binary signal. Additionally, the limiting amplifier delivers an RSSI (received signal strength indicator) signal, which is converted to a digital codeword by a 10bit ADC. The RSSI signal can be used as wake-up criterion as well as for fine tuning of the LO frequency, the BAW filters, and the matching network. In the digital domain, the binary output of the limiting amplifier is directly mixed into complex baseband by using a numerically controlled oscillator (NCO), which allows tuning of the frequency

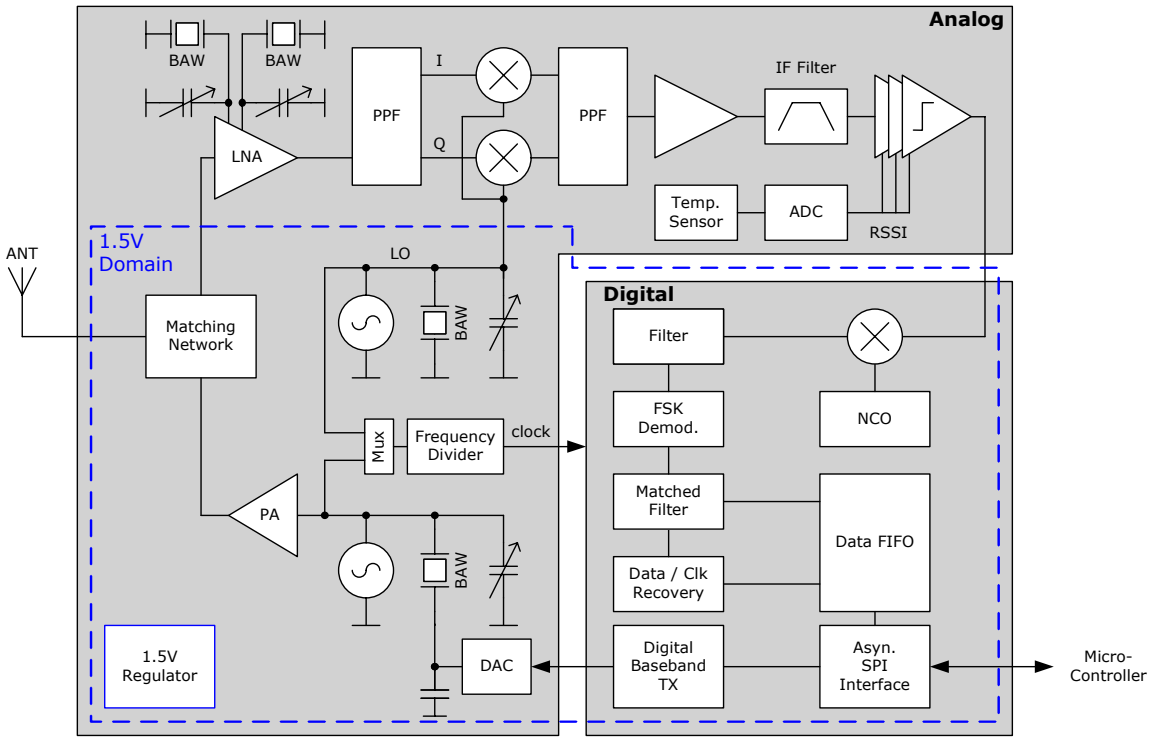


Figure 1.15: Block diagram of the transceiver.

in very fine frequency steps. The digital clock is derived from one of the two BAW oscillators. After additional digital filtering and demodulation, the signal is passed to the matched filter. By means of the clock and data recovery unit, the output of the matched filter is sampled and the received payload is stored in a FIFO memory, where the microcontroller can access the data via the SPI. In order to have access to the FIFO and to allow configuration of the transceiver while the oscillators are turned off, the SPI is implemented asynchronously.

The modulated carrier signal for the transmitter is generated by a free-running BAW oscillator in the same way as the LO signal for the receiver. To overcome temperature drift effects of the resonance frequency, the temperature is measured and compensated by means of digitally controlled capacitors in parallel to the resonator. In addition to the capacitor bank, the BAW can be tuned with a variable DC biasing. More details on tuning can be found in chapter 4.5 on page 81. The modulated carrier is fed to a power amplifier after pre-amplifying. In transmit mode the power amplifier allows transmission of a signal with a power of about 1 dBm into a 50 Ω load.

1.4 Design Issues when using 3D Integration Techniques

The following chapter was taken from [8, 9, 14] (own publications). My contribution to the work was to provide information about the RF application and to support the

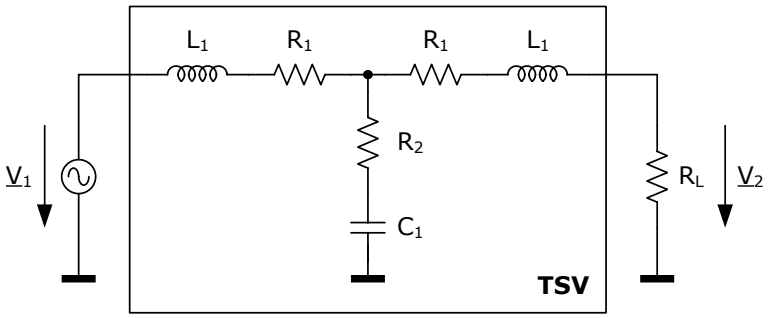


Figure 1.16: Symmetric equivalent network of TSV.

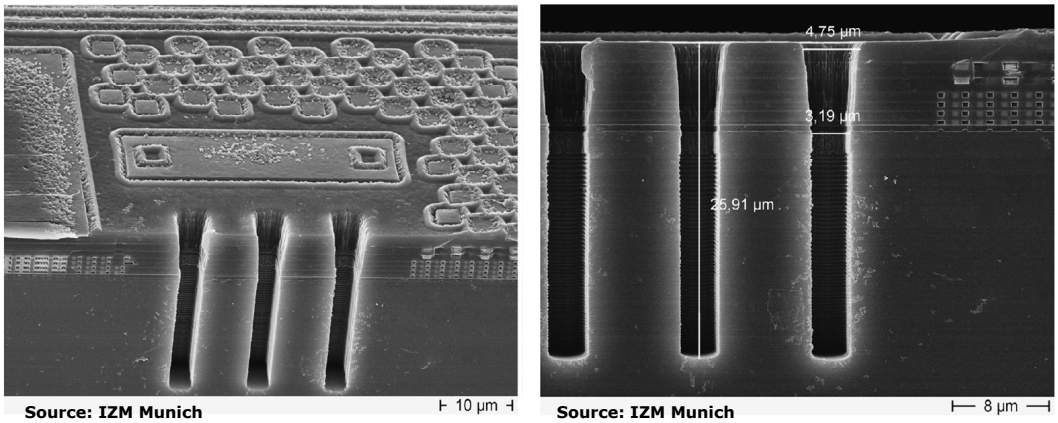


Figure 1.17: Scanning electron microscope (SEM) photo of the TSV.

analytical calculation of the efficiency out of the S-parameters and I provided a proposal of a round via structure. The simulations and interpretation were accomplished by project partners.

In [8, 9, 14], design issues when using 3D integration techniques are investigated. The most important issue in a 3D stack is the interconnection of the different dies. For this reason in [8, 9, 14] analyses and simulations of different TSVs structures have been performed. The output of the FEM simulations are scattering (S) parameter matrices describing the RF performance of the TSVs. With the help of [35] the S-parameter matrix $\underline{\mathbf{S}}$ can be transformed to the impedance parameter matrix $\underline{\mathbf{Z}}$:

$$\underline{\mathbf{Z}} = \mathbf{Z}_0^{\frac{1}{2}}(\mathbf{E} - \underline{\mathbf{S}})^{-1}(\mathbf{E} + \underline{\mathbf{S}})\mathbf{Z}_0^{\frac{1}{2}} \tag{1.3}$$

A possible equivalent circuit of the TSV is shown in Figure 1.16. From the $\underline{\mathbf{Z}}$-matrix, the values of the components for one frequency can be calculated. The efficiency η of a TSV is defined as the output power P_o divided by the total electrical power P_i and

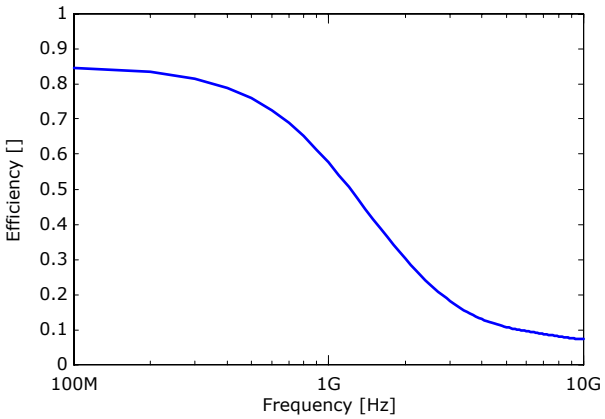


Figure 1.18: Efficiency for default TSV, half wafer thickness, double conductance of substrate, double oxide thickness, and 50 Ω load impedance.

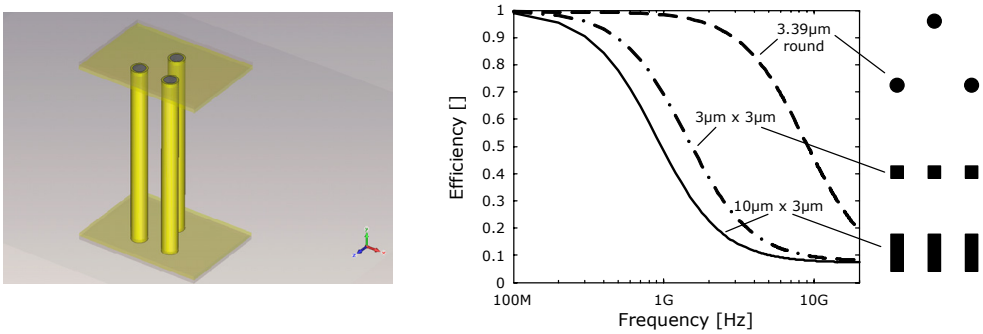


Figure 1.19: Microwave studio (from CST AG) 3D simulation model of round TSV and efficiency of different TSV structues.

can be determined using equation 1.4:

$$\begin{aligned} \eta &= P_\mathrm{o}/P_\mathrm{i} \\ P_\mathrm{o} &= \Re\{\underline{V}_2\underline{I}_2^*\} = \Re\{R_\mathrm{L}\underline{I}_2\underline{I}_2^*\} = R_\mathrm{L}|\underline{I}_2|^2 \\ P_\mathrm{i} &= |\underline{I}_1|^2\Re\left\{\underline{Z}_{11} - \frac{\underline{Z}_{12}^2}{\underline{Z}_{11}+R_\mathrm{L}}\right\} \\ \eta &= \frac{R_\mathrm{L}\left|\frac{\underline{Z}_{12}}{\underline{Z}_{11}+R_\mathrm{L}}\right|^2}{\Re\left\{\underline{Z}_{11} - \frac{\underline{Z}_{12}^2}{\underline{Z}_{11}+R_\mathrm{L}}\right\}} \end{aligned} \tag{1.4}$$

In the proposed transmitter, rectangular TSV are used. A scanning electron microscope (SEM) photo of the TSV after etching is shown in Figure 1.17. Chapter 4, page 59, explains why the oscillator makes use of the parallel resonance of the BAW. The resistance at parallel resonance is in the range of a few kΩs. Hence the resistor R_1 contributes only a minor part of the overall losses. But this is not the case for R_2, which represents losses due to the resistance of the substrate. From Figure 1.18 it can be seen that, at 2.1 GHz, 68% of the energy is lost in the substrate

Table 1.2: Comparison of component values of the TSV equivalent circuit.

TSV structure	R_1	L_1	R_2	C_1
10 x 3 µm^2 rectangular	0.015 Ω	38 pH	156 Ω	300 fF
3 x 3 µm^2 square	0.01 Ω	29 pH	166 Ω	190 fF
round, diameter: 3.39 µm, area: 9 µm^2	5.4 Ω	0.2 pH	75 Ω	44 fF

when connected to 2 kΩ. Hence in the proposed transmitter the BAW is flip-chipped directly onto the transceiver, as shown in Figure 1.7, without using TSVs. Simulations [8, 9, 14] showed that the losses into the substrate can be optimized by reducing the parasitic capacitance C_1, for example by utilization of a thicker oxide for isolation or by reducing the thickness of the wafer. Another possibility is to optimize the conductivity of the substrate.

Another approach is to use another TSV topology: In Figure 1.19 the simulation model of three round TSVs is presented, each with an area of 9 µm² (diameter of 3.39 µm), and placed at the corners of an equilateral triangle. This topology has the lowest possible surface area with the same cross section as the rectangular ones. The parallel connection of multiple TSVs reduces the total resistance and inductance [33].

On the right side of Figure 1.19 the simulations of the efficiency of the proposed round via is compared to vertical interconnections consisting of a 1 by 3 rectangular TSV array. In the first case the shape of the TSV is a 3 x 3 µm^2 square, and in the second case a 10 x 3 µm^2 rectangle. Table 1.2 provides the corresponding component values of the TSV equivalent circuit given in Figure 1.16. The round TSVs show the best performance.

1.5 Conclusion

State-of-the-art Tire Pressure Monitoring Systems (TPMS) are wireless sensor nodes mounted on the rim. Attaching the node on the inner liner of a tire allows the sensing of important technical parameters and enables the storage of additional information. By exploiting BAW resonators, the use of a bulky and shock-sensitive quartz crystal and a PLL can be avoided. This makes the system more robust and radically reduces the start-up time from a few ms, as in state-of-the-art quartz crystal oscillator based systems, to 2 µs.

It was shown that a system-in-package (SiP) can be advantageous in terms of price compared to a system-on-chip (SoC) implementation, although the BAW technology is compatible with a standard integrated circuit (IC) process and it is possible to integrate BAW resonators above an IC [74]. The reason for this is the relatively low yield (80%) of the BAW resonators caused by the process variation of the resonance frequency. More details on this can be found in chapter 4.5 on page 81. Since the BAW

resonator is very small, the costs of the stand-alone resonator are negligible. But if the resonator is integrated on top of the relatively large and expensive transceiver ASIC, the overall yield is dramatically reduced.

Therefore a 3D chip stack was developed by project partners to provide best compactness, lowest volume, and maximum robustness. Design issues when using this integration technique were considered. It was shown that an optimized structure, where three round TSVs are placed at the corners of an equal-sided triangle can significantly reduce losses into the substrate. This structure has the lowest possible surface area to the substrate and hence TSV technology could be also applied for RF interconnections.

2 Transmitter Concept

2.1 The Power-Bandwidth Trade-Off

In the following chapter the required features of the transmitter - like modulation scheme (and therefore the required bandwidth BW of the receiver), maximum data rate, transmit power S_{T}, start-up time, and current consumption are specified. The design goal of a transmitter is to keep the required energy per bit low. This can be done by finding the optimum transmit power and the optimum data rate. A higher data rate allows a short active time of transmission, but would require a higher bandwidth or a more complex modulation scheme and hence a higher complexity of the transmitter. On the other hand a higher bandwidth implies more received noise in the receiver and this reduces the signal-to-noise ratio at the receiver. Or in other words the sensitivity of the receiver is getting worse. To compensate this effect the transmit power must be increased to allow the same communication distance between transmitter and receiver. This problem is known as power-bandwidth trade-off [22]. These basic relations are expounded by the Shannon-Hartley theorem.

This theorem can be obtained from the following considerations. In Figure 2.1 an input signal is sampled with the sampling frequency f_{s}. Subsequently it is quantized by means of an ADC with N bits. Hence the amplitude range A is divided into $n = 2^N$ equal parts. Assuming that the input signal is uniformly distributed, all levels are equally present over time. After quantization the signal power P_{S} can be calculated

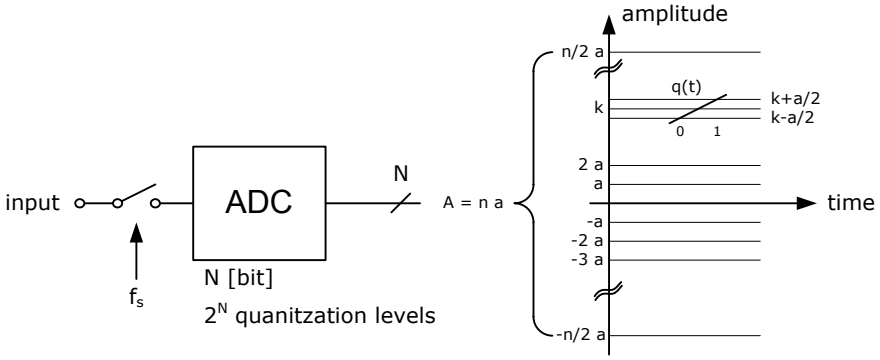


Figure 2.1: Time and amplitude discrete system.

with:

$$P_{\mathrm{S}} = \frac{1}{n}\sum\left(2\left(\frac{a}{2}\right)^2 + 2\left(\frac{3a}{2}\right)^2 + 2\left(\frac{5a}{2}\right)^2 + \cdots + 2\left(\frac{(n-1)a}{2}\right)^2\right) = \frac{a^2}{12}(n^2-1) \tag{2.1}$$

Since the input signal is uniformly distributed, the quantization noise is too. Thus the quantization noise power P_{Q} can be calculated by squaring and integration of a linear ramp $q(t) = -\frac{a}{2} + a \cdot t$ (see Figure 2.1). The ramp starts at $t = 0\,\mathrm{s}$ and leaves the quantization level at $t = 1\,\mathrm{s}$. Hence P_{Q} is:

$$P_{\mathrm{Q}} = \int_0^1 \left(-\frac{a}{2} + a \cdot t\right)^2 = \frac{a^2}{12} \tag{2.2}$$

If one knows the signal and noise power it is easy to calculate the signal-to-noise ratio.

$$\frac{P_{\mathrm{S}}}{P_{\mathrm{Q}}} = \frac{S}{N} = n^2 - 1 \quad \rightarrow \quad \log_2\left(\frac{S}{N} + 1\right) = 2\log_2 n \tag{2.3}$$

After sampling and quantization the data rate C at the output of the ADC is $f_{\mathrm{s}} \cdot N$. The Nyquist sampling theorem states that the input signal with the bandwidth BW, has to be sampled at least with $f_{\mathrm{s}} = 2BW$. The channel capacity can be calculated as follows:

$$\begin{aligned} C &= f_{\mathrm{s}} \cdot N = 2 \cdot BW \cdot N = 2 \cdot BW \cdot \log_2 n \\ C &= BW \log_2\left(\frac{S}{N} + 1\right) \end{aligned} \tag{2.4}$$

Equation 2.4 is known as Shannon-Hartley theorem. The Shannon-Hartley theorem [18, 22] describes the available channel capacity C in $[\mathrm{bit/s}]$ of a communication link perturbed by additive white Gaussian noise as a function of the required bandwidth BW and of the required signal-to-noise ratio $S_{\mathrm{R}}/N_{\mathrm{R}}$ at the receiver. Although the Shannon-Hartly law provides only a theoretical limit, which cannot be reached in a practical implementation, basic relations can be obtained from it.

To find the optimum transmit power a simple model of the communication link including transmitter and receiver is introduced (see Figure 2.2). The overall noise figure NF_{tot} can be calculated by dividing the signal-to-noise ratio $\frac{S_{\mathrm{T}}}{N_{\mathrm{T}}}$ at the transmitter and the signal-to-noise ratio at the receiver $\frac{S_{\mathrm{R}}}{N_{\mathrm{R}}}$. NF_{tot} includes the path-losses as well as other non-idealities, such as noise introduced by the receiver front end. In the proposed model the receiver and the transmitter are operating at standard noise temperature $T_0 = 290\,\mathrm{K}$. If the maximum overall noise figure is assumed to be known, the signal-to-noise ratio at the receiver can be determined as shown in equation 2.5.

$$NF_{\mathrm{tot}} = \frac{S_{\mathrm{T}}/N_{\mathrm{T}}}{S_{\mathrm{R}}/N_{\mathrm{R}}} \quad \rightarrow \quad \frac{S_{\mathrm{R}}}{N_{\mathrm{R}}} = \frac{S_{\mathrm{T}}}{N_{\mathrm{T}} \cdot NF_{\mathrm{tot}}} = \frac{S_{\mathrm{T}}}{\mathrm{k} \cdot T \cdot BW \cdot NF_{\mathrm{tot}}} \tag{2.5}$$

By using the equations 2.4 and 2.5 the available channel capacity can be calculated.

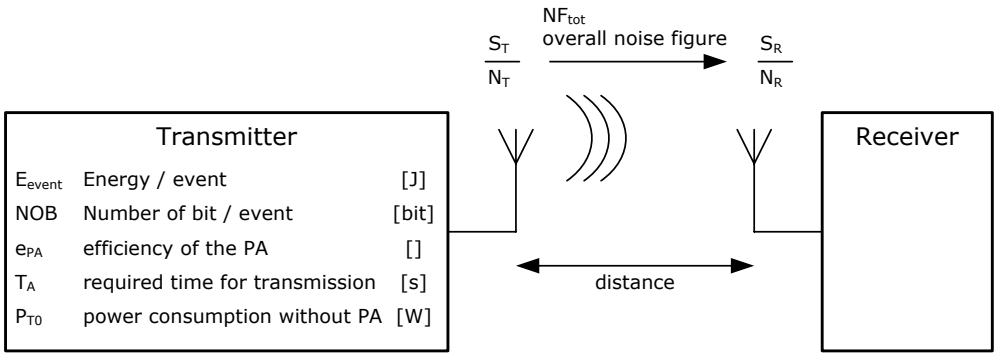


Figure 2.2: Simplified model of the communication.

Assuming a certain number of bits per event (NOB) the active time T_A needed for a transmission can be found using equation 2.6.

$$\begin{aligned} T_\mathrm{A} &= \frac{NOB}{C} \\ C &= BW \log_2\left(\frac{S_\mathrm{R}}{\mathrm{k}\cdot T\cdot BW}+1\right) = BW\log_2\left(\frac{S_\mathrm{T}}{\mathrm{k}\cdot T\cdot BW\cdot NF_\mathrm{tot}}+1\right) \end{aligned} \tag{2.6}$$

The total amount of energy E_event, which is consumed during one event, is the active time T_A multiplied with the power consumption of the transmitter. The transmitter's power consumption is composed of the transmitted power corrected by the efficiency e_PA of the power amplifier (PA) and the power consumption of the remaining transmitter P_T0. Additionally the energy E_startup has to be added to take the energy required during the start-up into account. Using equation 2.6 yields in:

$$E_\mathrm{event} = T_\mathrm{A}\cdot\left(P_\mathrm{T0}+\frac{S_\mathrm{T}}{e_\mathrm{PA}}\right) = \frac{NOB}{BW\log_2\left(\frac{S_\mathrm{T}}{\mathrm{k}\cdot T\cdot BW\cdot NF_\mathrm{tot}}+1\right)}\cdot\left(P_\mathrm{T0}+\frac{S_\mathrm{T}}{e_\mathrm{PA}}\right)+E_\mathrm{startup} \tag{2.7}$$

In this way it is possible to plot the energy consumed during one event against the transmitted signal power. The result is illustrated in Figure 2.3 for an overall noise figure $NF_\mathrm{tot} = 90\,\mathrm{dB}$ and in Figure 2.4 for $NF_\mathrm{tot} = 60\,\mathrm{dB}$. For the two plots some assumptions have been made: The number of bits per event is assumed to be 1000, the power consumption P_T0 is 3 mW (this is equal to a current consumption of 2 mA at a supply voltage of 1.5 V), and the efficiency of the PA is 30%. This fits the features of the proposed transmitter. The start-up energy E_startup is disregarded due to the short start-up time of oscillator, which is about 2 µs. In Figure 2.3 the planned operating point of the transceiver system is marked. The outcome of equation 2.7 is the fact that an optimum of the transmitted signal power can be found: A high signal power would cause a high current consumption of the power amplifier. On the other hand, a very low signal power induces a lower signal-to-noise ratio at the receiver and thus the receiver can only process lower data rates and this is equivalent to a longer transmit time, which increases the energy required at

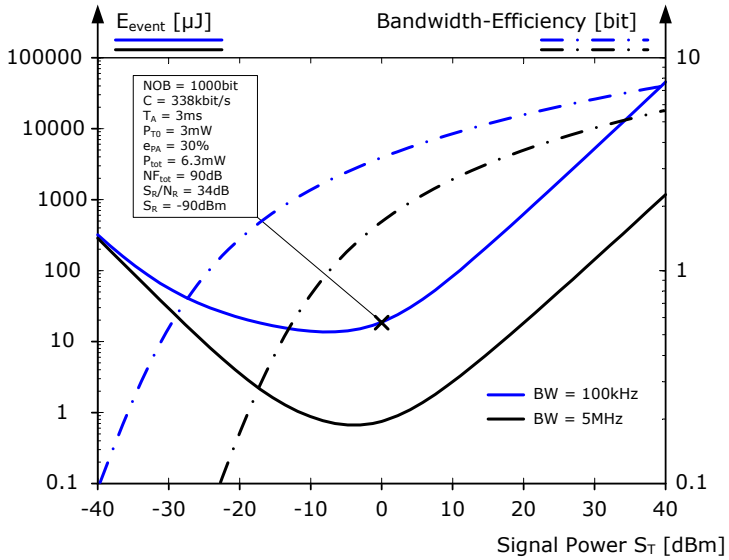


Figure 2.3: Simplified power-bandwidth trade-off ($NF_{\mathrm{tot}} = 90\,\mathrm{dB}$).

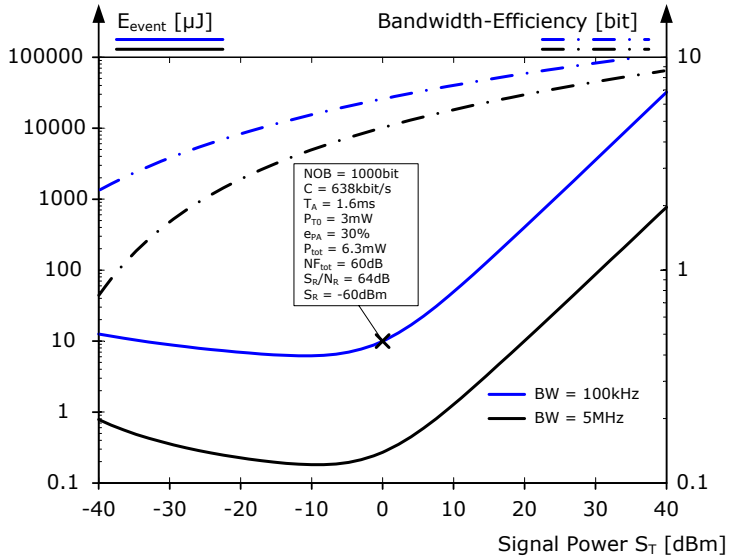


Figure 2.4: Simplified power-bandwidth trade-off ($NF_{\mathrm{tot}} = 60\,\mathrm{dB}$).

the transmitter. Besides that, a higher available bandwidth can help to reduce the power consumption of the transmitter. The bandwidth and the losses (here taken into account by the overall noise figure NF_{tot}) are the two parameters describing the quality of the communication link.

It is important to note that the channel capacity C close to the minimum is 338 kbit/s for an overall noise figure of 90 dB, whereas the bandwidth is only 100 kHz. In the proposed transmitter continuous phase frequency shift keying (CPFSK) or ASK is used for modulation. Although the bandwidth of a CPFSK modulated carrier is

theoretically not limited, according to [36] the occupied bandwidth BW_{FM}, where most of the energy is concentrated, can be approximated with the Carson rule. For a modulation index $m > 1$ the bandwidth can be derived as a function of the frequency deviation Δf and of the data rate DR:

$$\begin{aligned} m &= \Delta f \cdot T_{\mathrm{s}} = \frac{\Delta f}{\mathrm{DR}} \\ BW_{\mathrm{FM}} &= 2(\Delta f + DR) = 2(m+1)DR \end{aligned} \tag{2.8}$$

Unfortunately, it is not possible to transmit 338 kbit/s in a 100 kHz channel with CPFSK. To accomplish such a data rate, a higher modulation scheme has to be used. This would require more complex hardware, such as a linear power amplifier, mixers, and so on. Therefore the model of the receiver is enhanced. In Table 2.1 the sensitivity values found in the data sheet [37] of an FSK receiver for different data rates are given. The occupied bandwidth in the table is calculated with equation 2.8. The used bandwidth at IF is taken from the data sheet. The noise floor is determined using the IF bandwidth and the relation $\mathrm{k} \cdot T \cdot BW$. For the first model the required signal-to-noise ratio (see equation 2.9) for correct demodulation at the receiver is found by rewriting equation 2.4, by replacing the channel capacity C with the data rate DR, and by adding a noise figure NF_{RX} to take all non-ideal properties of the receiver front end and demodulator into account. The noise figure is chosen in such a way that the sensitivity value given in the first row in the table is exactly fitted.

$$\frac{S_{\mathrm{R}}}{N_{\mathrm{R}}} = \left(2^{DR/BW_{\mathrm{FM}}} - 1\right) \cdot NF_{\mathrm{RX}} \tag{2.9}$$

An alternative way (model 2) to calculate the sensitivity is to use the $\frac{E_{\mathrm{b}}}{N_0} = 11\,\mathrm{dB}$, which is taken from a bit error probability curve (at a bit error rate of 10^{-3}) found in [22]. In this way it is possible to determine the signal-to-noise ratio as shown in equation 2.10. Here again the noise figure is added to take the non-idealities of the receiver into account.

$$\frac{S_{\mathrm{R}}}{N_{\mathrm{R}}} = \frac{E_{\mathrm{b}}}{N_0} \frac{DR}{BW_{\mathrm{FM}}} \cdot NF_{\mathrm{RX}} \tag{2.10}$$

The first model is used to extrapolate the sensitivity for higher data rates. The IF bandwidth is assumed to be equal to the occupied bandwidth. The result is illustrated in Figure 2.5. The sensitivity increases linearly with increasing data rate. If the path-loss is known, the required transmit power can be calculated easily. Assuming unobstructed free space with no multipath propagation (free line of sight), the Friis transmission equation [19] can be used to estimate the distance R between transmitter and receiver. The Friis formula is given in equation 2.11, where G_{R} and G_{T} denote the gain of the receive antenna and of the transmit antenna respectively and L denotes the path loss.

$$L = \frac{S_{\mathrm{R}}}{S_{\mathrm{T}}} = \frac{G_{\mathrm{R}} \cdot G_{\mathrm{T}} \cdot \lambda^2}{(4\pi R)^2} \tag{2.11}$$

Data Rate DR [kbit/s]	Frequency Defiviation Δf [kHz]	occupied Bandwidth [kHz]	used IF Bandwidth [kHz]	Sensitivity (Datasheet) [dBm]	Noise floor [dBm]	S_R/N_R (Model 1) [dB]	Sensitivity (Model 1) [dBm]	Deviation (Model 1) [dBm]	S_R/N_R (Model 2) [dB]	Sensitivity (Model 2) [dBm]	Deviation (Model 2) [dBm]
2	10	24	50	-119	-126.8	7.84	-119.0	0.0	7.81	-119.0	0.0
10	14	48	50	-114	-126.8	12.01	-114.8	0.8	11.79	-115.1	1.1
10	50	120	125	-112	-122.9	7.84	-115.0	3.0	7.81	-115.1	3.1
50	50	200	300	-105	-119.0	12.87	-106.2	1.2	12.58	-106.5	1.5
2	10	24	300	-110	-119.0	7.84	-111.2	1.2	7.81	-111.3	1.3
10	14	48	300	-106	-119.0	12.01	-107.0	1.0	11.79	-107.3	1.3
10	50	120	300	-110	-119.0	7.84	-111.2	1.2	7.81	-111.3	1.3

Table 2.1: Comparison of the sensitivity of a receiver (TDA5240, Infineon [37]) with different models for different data rates.

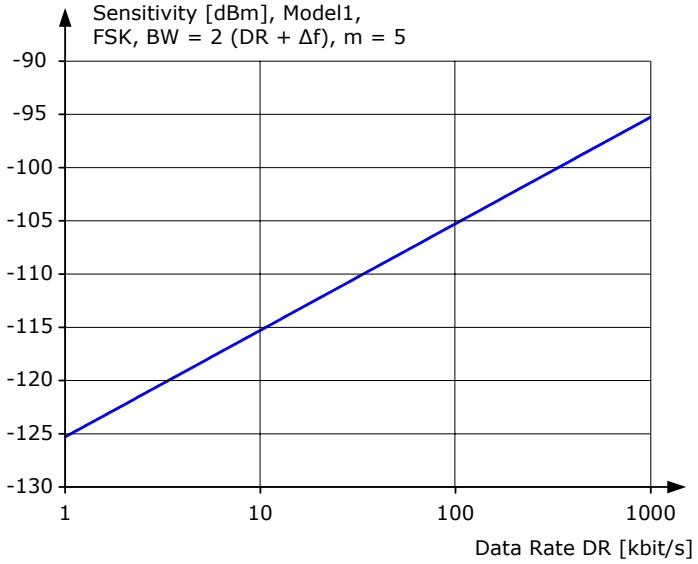


Figure 2.5: Sensitivity of the modelled receiver versus data rate.

With an antenna loss of 5 dB for each antenna, the overall noise figure NF_{tot} of 90 dB implies a ratio of received power to transmitted power $\frac{S_{\mathrm{R}}}{S_{\mathrm{T}}}$ of -80 dB. Under the assumption that the antennas radiate isotropically, the antenna gains are equal to 0 dB and thus the distance R in free space can be calculated as about 100 m for a 2.4 GHz ($\lambda = 0.12\,\mathrm{m}$) transmission frequency.

In the following considerations a more conservative scenario is assumed for the communication from the tires to the base station in the car. The path-loss exponent is increased from 2 to 4. To account for multipath and polarization effects 20 dB attenuation are added. Further two times 10 dB are supposed to be caused by the radiation efficiency of the antennas. The result is 108 dB path-loss for a 5 m communication distance. By adding the path-losses and the sensitivity, the required signal power S_{T} can be calculated as a function of the data rate. By using the introduced model in equation 2.7 the energy for one event E_{event} can be determined. The relationship between signal power, energy for one event, and data rate can be found in Figure 2.6.

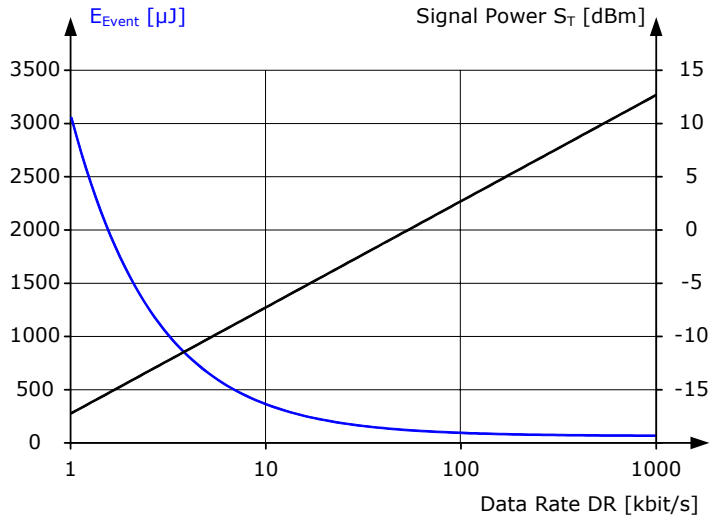


Figure 2.6: Required energy per event and the transmitted signal power versus data rate.

Thus the transmitter's power consumption can be significantly reduced by increasing the data rate. Increasing the data rate implies a higher bandwidth for an FSK transmitter and therefore the signal power has to be increased in the same way to keep the communication distance constant. Due to the higher data rate, the active time is reduced and so the power amplifier needs the same amount of energy independently of the data rate. But the portion of the remaining transmitter P_{T0} (the overhead) is reduced due to the short active time and hence the energy for one event converges to its ideal value with increasing data rate as seen in Figure 2.6. Also the model of the FSK transmitter shows a good compromise at a relatively low transmission power S_{T} of 0 dB.

The power-bandwidth trade-off can be summarized as follows. An increase in the data rate can be achieved in two different ways:

- The first possibility is to increase the data rate while keeping the bandwidth constant. A higher signal power at the transmitter increases the signal-to-noise ratio at the receiver and therefore the channel capacity is increased as known from the Shannon-Hartley theorem. A clear optimum for signal power and data rate at a certain bandwidth can be found. Or, in other words, DR/BW is at its optimum. DR/BW is a measure how efficiently the bandwidth (bandwidth-efficiency) is occupied. A higher bandwidth, which corresponds to an improved communication link, helps to reduce the required energy as shown in Figure 2.3. For a low bandwidth (bandwidth limited systems) the optimum DR/BW is quite high and this corresponds to a complex modulation technique like GMSK or M-ary signaling. For high available bandwidth the optimum DR/BW is smaller, resulting in a low complexity modulation scheme like FSK or for even higher bandwidths in frequency spreading. For high available bandwidths, the optimum power is lower

(power limited systems). Obviously this is preferred for a low power transmitter, if the required bandwidth is available.

- An increase in the data rate can also be achieved by simultaneously increasing the bandwidth. This corresponds to a constant bandwidth efficiency or constant DR/BW. In this situation the signal power has to be increased in the same way as the data rate increases. But due to the higher data rate the active time decreases and the power amplifier consumes the same amount of energy. However, the overhead in the transmitter decreases too, because of the short active time; hence the overall energy per event is improved for high data rates at the drawback of a high peak current caused by the high transmitted signal power.

For a very high bandwidth BW the Shannon-Hartley theorem given in equation 2.6 can be simplified as shown in equation 2.12. This equation is also known as the Shannon limit.

$$\begin{aligned}
&\lim_{x\to 0}(1+x)^{1/x} = \mathrm{e} \quad \rightarrow \quad x = \frac{S_\mathrm{R}}{\mathrm{k}\cdot T\cdot BW}\\
&C = BW\log_2\left(\frac{S_\mathrm{R}}{\mathrm{k}\cdot T\cdot BW}+1\right) = BW\,x\log_2\left(1+x\right)^{1/x} \quad \rightarrow\\
&\lim_{BW\to\infty} C = \lim_{BW\to\infty} BW\frac{S_\mathrm{R}}{\mathrm{k}\cdot T\cdot BW}\log_2(\mathrm{e}) = \frac{S_\mathrm{R}}{\mathrm{k}\cdot T}\log_2\mathrm{e} = \frac{S_\mathrm{T}\cdot L}{\mathrm{k}\cdot T}\log_2\mathrm{e}
\end{aligned} \tag{2.12}$$

For a large bandwidth, channel capacity C is directly proportional to signal power at the receiver and therefore also to signal power S_T radiated by the transmitter times the path loss L. This result is very similar to the given FSK example and indicates to the theoretical limit.

The outcome of the previous considerations is that the current consumption of state-of-the-art TPMS sensor nodes (4-10 kbit/s) can be improved by increasing the data rate. To keep the complexity of the transmitter low, a simple FSK modulation scheme is used. For a certain modulation technique, increasing the data rate makes sense, till the energy for one event is close to its ideal value. Then the overhead, mainly caused by the BAW oscillator, is negligible. For the BAW-based transmitter this is the case for a data rate in the range of 100 kbit/s and a signal power in the range of 0 dBm.

2.2 Transmitter Architectures

The task of a transmitter is to perform modulation, up-conversion, and power amplification [21]. In the proposed transmitter, modulation and up-conversion are combined in one step, as illustrated in Figure 2.7, the simplest block diagram of a transmitter. This kind of transmitter is ideally suited for simple modulation schemes, like continuous phase frequency shift keying (CPFSK) or amplitude shift keying (ASK). To

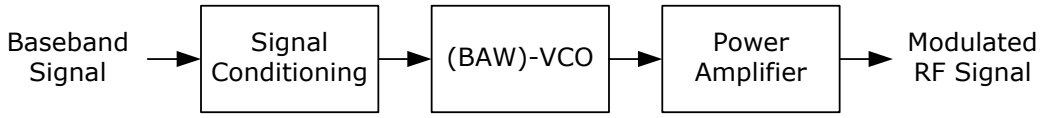


Figure 2.7: Simplest architecture of a transmitter [21].

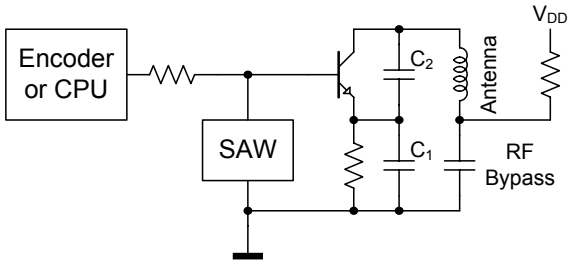


Figure 2.8: Simple implementation of a transmitter with discrete components [43].

overcome temperature and process variations of the BAW oscillator, the baseband signal has to be processed by the signal conditioning block. Additionally the bandwidth of the transmitted signal can be reduced by means of digital filtering of the baseband signal. For instance in a GFSK application a Gaussian filter can be used to avoid any abrupt frequency deviation or a Blackman filter can be used in case of ASK modulation. No pulse shaping has been implemented in the proposed prototype, but could be implemented with little effort in the digital domain. The advantage of this architecture is the low power consumption due to the low complexity. In the proposed implementation the signal conditioning block is very simple and its power consumption is negligible. An additional task of the signal condition block is to overcome temperature drift effects of the resonance frequency, therefore the temperature is measured and compensated by means of digitally controlled capacitors in parallel to the resonator.

Indeed such simple transmitters using resonators have been in widespread use for unlicensed application. Applications such as automotive keyless entry, door and gate openers, wireless alarm sensors, medical alert pendants, bar code readers, wireless remote control, security, and data transmission areas [43] employ them. An example of a transmitter using a surface acoustic wave (SAW) resonator and discrete components is drawn in Figure 2.8. The main disadvantage of this architecture is its fairly unstable frequency source. On the other end of the spectrum of complexity there is a transmitter based on the all-digital frequency synthesizer illustrated in Figure 2.9, which has been presented in [45]. The task of the PLL is to transform the precise and stable frequency of quartz crystal to RF. The required building blocks are the digitally controlled oscillator (DCO), a time-to-digital converter (TDC), loop filter, a gain normalization block, and a reference and oscillator phase accumulator. All

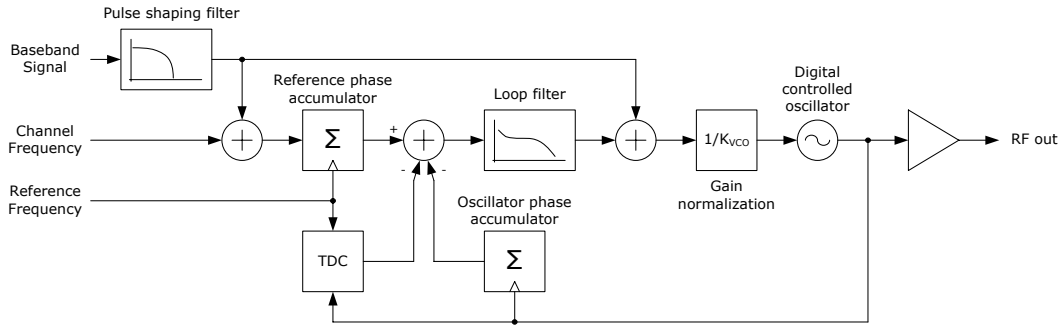


Figure 2.9: Transmitter based on the all-digital frequency synthesizer [45].

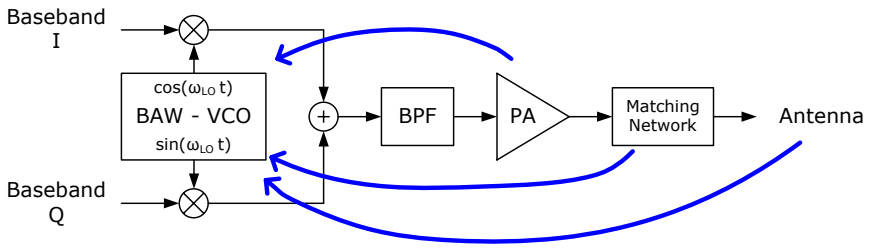


Figure 2.10: Direct (up)-conversion transmitter [21].

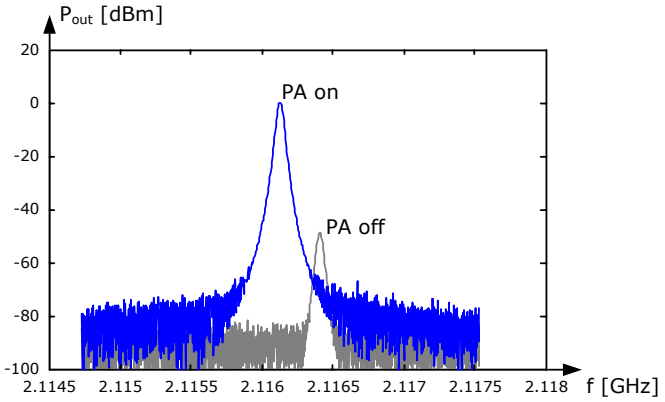


Figure 2.11: Measurement of BAW Oscillator pulling.

blocks except the DCO are implemented in the digital domain. Two-point modulation allows proper wide-band modulation of the carrier. A calibration step in which the gain normalization is carried out makes the transmitter independent of process-voltage-temperature (PVT) variations. Additionally the frequency reference drift can be compensated if the temperature can be measured and the channel frequency is set according to a characteristic curve of the frequency drift.

Another drawback of a simple up-conversion transmitter like the one in Figure 2.10 is oscillator pulling [21]. Feedback from the power amplifier back to the oscillator can cause an unintended frequency shift. Of course, there can be different ways of

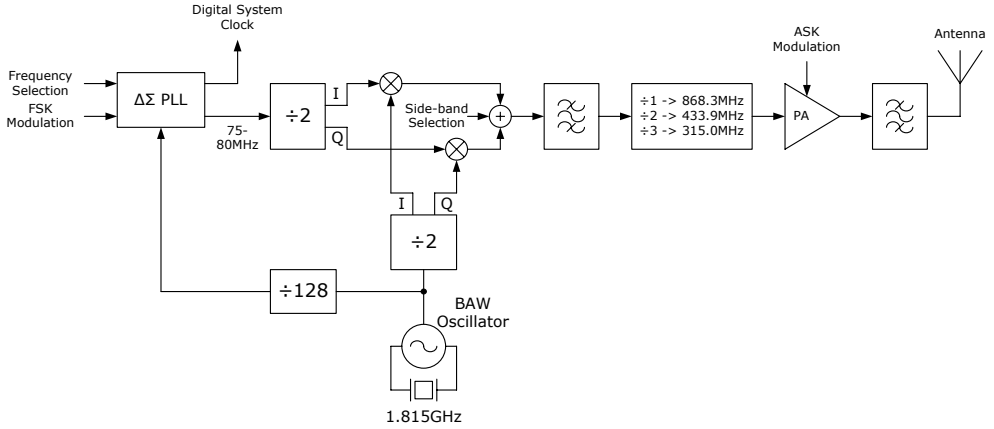


Figure 2.12: Increased oscillator stability by using a $\Delta\Sigma$-PLL [12].

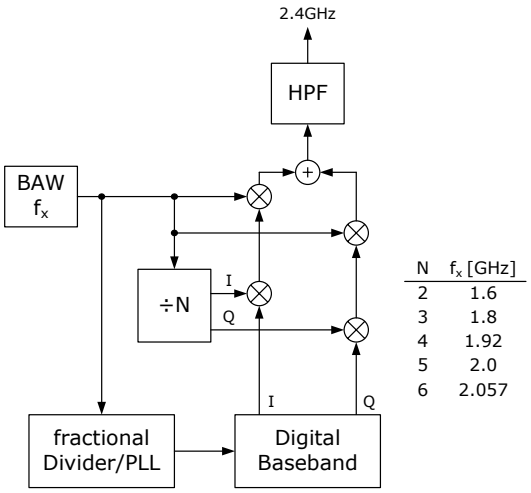


Figure 2.13: Possible implementation of a two-step transmitter.

coupling, which can also vary with time if the environment changes. For example, the coupling between antenna and oscillator can be influenced by simply holding one's hands close above the sensor node. This significantly changes the resonance frequency of the proposed transmitter. The measured oscillator frequency with the power amplifier turned on and turned off is shown in Figure 2.11. The measurable frequency shift is about 300 kHz, which corresponds to 140 ppm!

To overcome these limitations, different solutions can be implemented. Pulling is avoided if the oscillator's frequency is sufficiently lower or higher than the output frequency. This can be achieved for instance by using a PLL as shown in Figure 2.12 [12]. Another way is a two-step transmitter as illustrated in Figure 2.13. Both solutions have an increased complexity and therefore a significantly higher power consumption.

Another way to provide isolation between power amplifier and oscillator is the usage of a divider with a divider ration of 1.5 (see Figure 2.14). After division by 1.5

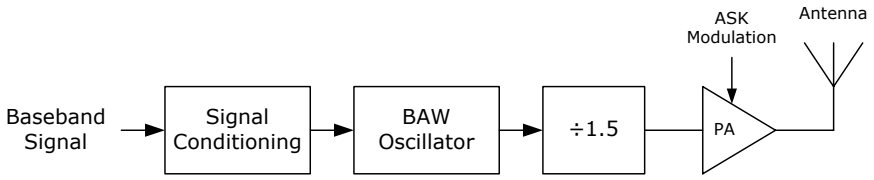


Figure 2.14: Providing an offset between output and reference frequency achieved by a division of 1.5.

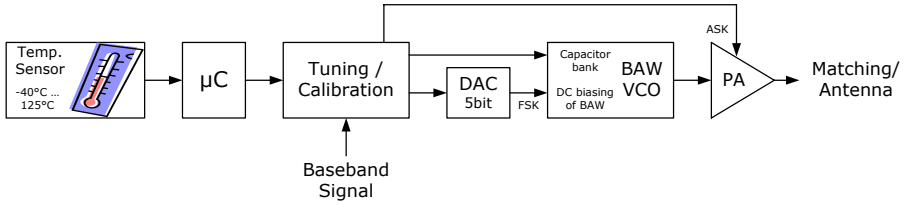


Figure 2.15: Increased oscillator stability achieved by temperature compensation.

the output frequency and all integer multiples cannot disturb the oscillation. An offset between output and reference frequency would be mandatory for a practical implementation. This is the motivation for the asynchronous divider proposed in chapter 5.7 on page 109.

The simplified block diagram of the implemented transmitter is shown in Figure 2.15. A temperature sensor provides a measure for the current temperature on the chip. A microcontroller can calculate the appropriate tuning word by using a characteristic curve of the temperature drift of the BAW resonator. This curve is determined by a calibration step. For details on BAW tuning see chapter 4.5 on page 81. A more detailed block digram of the transceiver is illustrated in Figure 2.16.

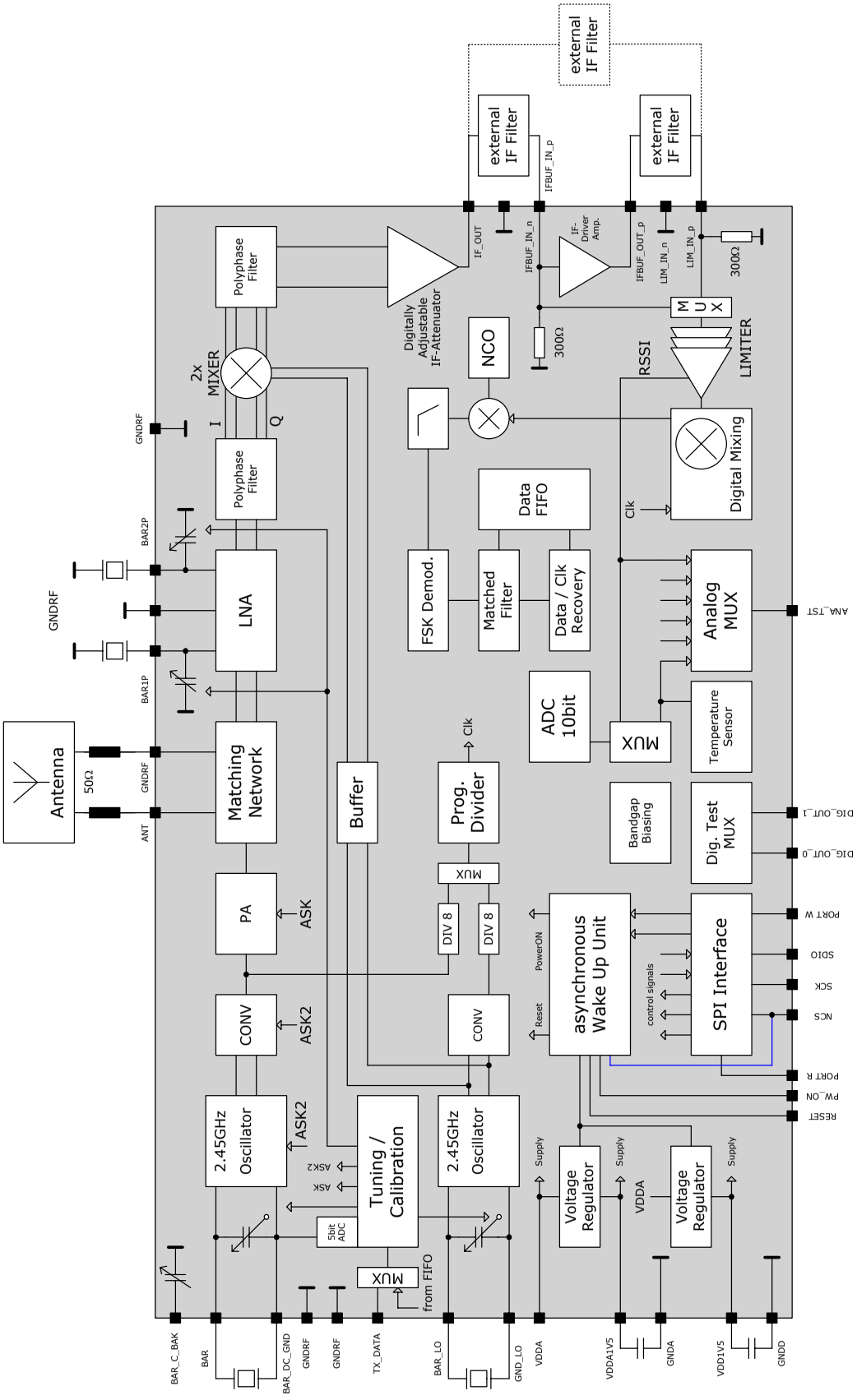


Figure 2.16: Detailed block diagram of the e-Cubes transceiver.

Reference	IC Technology	Application	Datarate [kBit/s]	fc [GHz]	Supply Voltage [V]	Current Consum. [mA]	Power Consum. [mW]	Temp. Range [°C]	Transmitted Power [mW]	Transmitted Power [dBm]	Efficiency [%]	Energy per Bit [nJ/bit]	FoM_{WSN} [dB]	FoM2 [nJ/bit/mW]
[This Work]	**CMOS 0.13µm**	**WSN (eCubes) - *FSK Mode***	**100**	**2.45[1]**	**1.5**	**4.7**	**7.1**	**-40...125**	**1.48**	**1.7**	**21**	**71**	**87.1**	**48**
[Otis05]	CMOS 0.13µm	WSN (PicoRadio)	5	1.9	0.9-1.3	-	1.47[4]	-	0.38	-4.2	26	294	86.9	774
[Leung07]	CMOS 0.18µm	WLAN IEEE 802.11a	56000	5.35	1	-	53	-	1	0	2	0.95	80.0	0.95
[Kluge06]	CMOS 0.18µm	ZigBee IEEE 802.15.4	250[2]	2.4	1.8	15.7	28	-	2.00	3.0	7	113	82.3	57
[Staszewski04]	CMOS 0.13µm	Bluetooth	1000[2]	2.4	1.5	28	42	-	1.78	2.5	4	42	80.1	24
[Staszewski05]	CMOS 90nm	GSM/EDGE	500[2]	0.824	1.2	42	50	-	3.98	6	8	101	78.1	25
[Yuan09]	CMOS 0.18µm	UWB	40000	3.1-4.5	1.8	9.9	18	-	0.05	-13	0	36	70.2	711
[Infineon09]	-	RKE, Metering, Remote Control, ...	50	0.315-0.915	1.9-3.6	16	48	-40...85	10	10	21	960	82.8	96
[Raja08]	CMOS 0.35µm	WSN/WBAN	10000	0.433	1	1.2[4]	1.2[4]	-	0.0537	-13	4	0.120	72.9	2.23
[Cook06]	CMOS 0.13µm	WSN	300-500	2.34	0.4	-	1.12	-	0.32	-4.9	29	2.24	88.3	7.0
[Daly07]	CMOS 0.18µm	WSN	1000	0.9165	1.4	-	9.1	-	0.60	-2.2	7	9.1	77.8	15
[Chee05]	CMOS 0.13µm	WSN	50	1.9	0.28	-	3.2[4]	-	1	0	31	64	87.7	64
[Chee06]	CMOS 0.13µm	WSN	330	1.9	0.65	-	2.7[4]	-	1.2	0.8	44	8	89.3	7

[1] Oscillator was also tested with 2.1GHz BAW resonator, values are given for 2.45GHz BAW.
[2] These values are assumed.
[3] The BAW-Oscillator is always running, only the PA is switched on and off.
[4] Values are given for a clean carrier. The power consumption is reduced by half when OOK (50%) is used, but also the transmitted power (therefore no impact on the FoM).

[Otis05] = [89]	[Leung07] = [98]	[Kluge06] = [99]
[Staszewski04] = [100]	[Staszewski05] = [101] or [102]	[Yuan09] = [103]
[Infineon09] = [40]	[Raja08] = [104]	[Cook06] = [105]
[Daly07] = [106]	[Chee05] = [107]	[Chee06] = [108]

Table 2.2: Comparison of this work with other high performance transmitters including Figure-of-Merit (FoM).

2.3 The BAW Oscillator in Receive Mode

The task of the BAW oscillator is to provide the required signals not only for the transmitter but also for the receiver. Because of the intermediate frequency of 10.7 MHz, the LO signal required for the mixers has a frequency offset with respect to the transmit frequency. Therefore a second BAW oscillator is integrated, which is connected to a BAW resonator with a slightly different resonance frequency as already mentioned in chapter 1 on page 17.

2.4 Figure-of-Merit (FoM) and Comparison with State-of-the-Art

A Figure-of-Merit often used for transmitters is the energy E_{bit} consumed during transmission of one bit. In Table 2.2 a performance comparison is given and Figure 2.17 shows the power consumption versus the available data rate for high performance transmitters. Since the energy per bit E_{bit} is the power consumption divided by the data rate, each point in the figure can be assigned to a certain energy per bit value. Different E_{bit}-values are indicated with black lines. This FoM can be interpreted as energy efficiency. It cannot be used to compare different architectures: this would be unfair, since the transmitted power is not considered. Therefore in [104] a FoM including the transmitted power is introduced. This FoM can be calculated with the

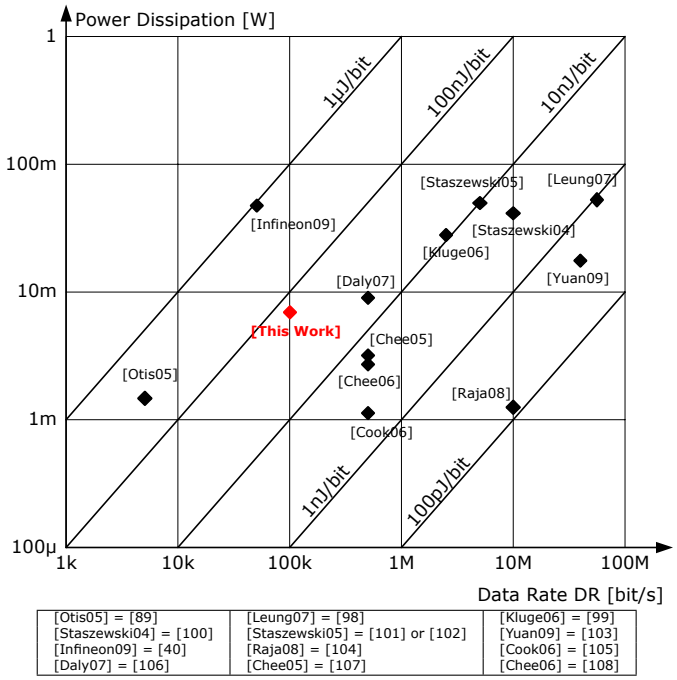


Figure 2.17: Power dissipation versus data rate for different transmitters.

following equation:

$$FoM = \frac{E_{\mathrm{bit}}}{S_{\mathrm{T}}} = \frac{P_{\mathrm{T}}}{DR \cdot S_{\mathrm{T}}} \tag{2.13}$$

However, this improved FoM does not include many important aspects of transmitters. The most important is the challenge faced by the receiver to receive the transmitted signal. If the bandwidth-efficiency DR/BW and the E_{b}/N_0 needed for correct reception are given, the required signal power S_{R} at the receiver is proportional to the data rate as it can be seen from equation 2.9 or from equation 2.10. This relation is also plotted in Figure 2.5 on page 40. On that condition the ratio $k = S_{\mathrm{T}}/DR$ is a measure of how much effort the reception requires. Another very important aspect is the frequency of the carrier. It is assumed that power consumption is proportional to this. Therefore a new FoM is introduced:

$$FoM_{\mathrm{WSN}} = 10\log\left(\frac{f_{\mathrm{T}} \cdot E_{\mathrm{bit}}}{k}\right) = 10\log\left(\frac{f_{\mathrm{T}} \cdot P_{\mathrm{T}}}{S_{\mathrm{T}}}\right) \tag{2.14}$$

It is important to note that this FoM is independent of the data rate. Indeed, if the complexity of the transmitter is low, the data rate can be increased without any effort as is the case in the topology used. Chapter 4.5 shows that the transmitter can cope with very high data rates. For example, the demodulated output of the transmitter for a data rate of 2 Mbit/s is shown in Figure 4.41 on page 91. But the receiver is not able to receive this signal. The data rate can be increased and hence the energy per bit decreases, but obviously the challenges for the receiver are increasing too

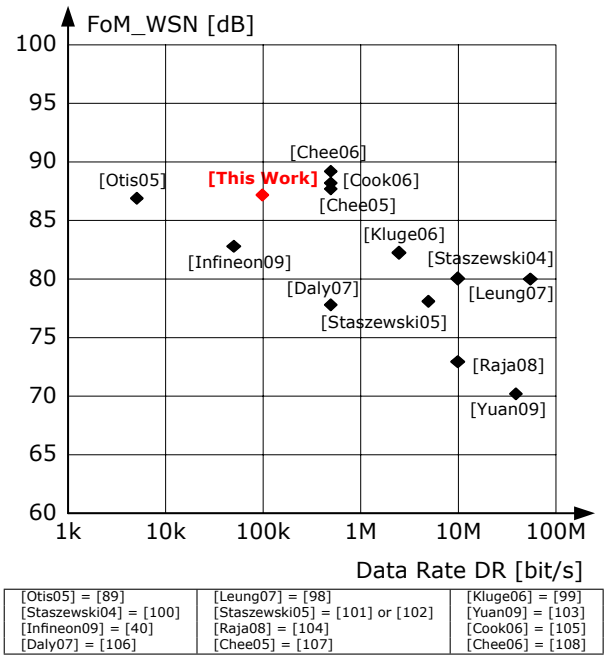


Figure 2.18: Figure-of-Merit (FoM) of different transmitters versus dissipated power.

(this means that k decreases). To compensate this effect, the transmit power has to be increased and consequently the advantage gained by increasing the data rate is nullified. That is why this kind of FoM is well suited for the low complexity transmitters often used in wireless sensor networks (WSN). As already mentioned, systems with higher bandwidth-efficiency require more complex hardware, such as linear power amplifiers and mixers. Of course, this has an impact on the power consumption and therefore this FoM is not recommended for such systems. A graphical representation of the FoM given in equation 2.14 versus the data rate can be found in Figure 2.18.

There are still some properties of transmitters that are not included in the FoM, such as phase noise, frequency accuracy, temperature range, power supply rejection ratio, bandwidth-efficiency, and so on. One can see that the proposed transmitter is comparable to other high performance transmitters. It is possible that the proposed transmitter lags a little bit behind because the power consumption of all required blocks such as bandgap, voltage regulators, and digital control unit are included. the high temperature range up to 125°C also probably has a certain impact. For the current consumption given in Table 2.2 the dividers are turned off. However a differential to single-ended converter, which is able to drive the power amplifier and the dividers, is included in the power consumption. Additionally, if a separate transmitter and receiver matching with external components is used (as is the case, for example, in [107] (=[Chee05]), the current consumption is lower compared to an integrated solution.

Low complexity transmitters clearly have the best FoM because there is no need for

linear circuitry and they also do not require additional blocks like PLLs and mixers. However the bandwidth-efficiency is not good, due to the low complexity modulations scheme of ASK and FSK. Frequency accuracy is another issue which is often overlooked.

2.5 Conclusion

In the this chapter it was shown that an optimum transmitted signal power can be found. As a first step, the bandwidth was kept constant. Then a higher signal power at the transmitter increases the signal-to-noise ratio at the receiver and therefore the channel capacity is increased, as known from the Shannon-Hartley theorem. A clear optimum for signal power and data rate at a certain bandwidth can be found. Or, in other words, an ideal DR/BW can be determined. For a low bandwidth (bandwidth limited systems) the optimum DR/BW is quite high and this corresponds to a complex modulation technique such as GMSK or M-ary signaling. For high available bandwidth the optimum DR/BW is smaller, resulting in a low complexity modulation scheme like FSK and for even higher bandwidths in frequency spreading. For high available bandwidths, the optimum energy required for one event is lower (power limited systems). Clearly this is preferable for the proposed low power transmitter, since the required bandwidth is available.

In the second step it was assumed that the bandwidth is not a limiting factor. Then an increase of the data rate can also be achieved by simultaneously increasing the bandwidth. This corresponds to a constant bandwidth efficiency or constant DR/BW. In this situation, the signal power has to be increased correspondingly as the data rate increases. However, due to the higher data rate the active time decreases and the power amplifier consumes the same amount of energy. Nonetheless, the overhead in the transmitter also decreases, because of the short active time; hence the overall energy per event is improved for high data rates with the drawback of a high peak current caused by the high transmitted signal power. The theoretical limit, known as Shannon limit (see equation 2.12), of such systems was derived. The required energy per transmission decreases with increasing data rate.

As a result it was shown that for the proposed transmitter implementation a data rate in the range of 100 kBit/s is sufficient. A further increase would not save much more power (see Figure 2.6). Using the Shannon theorem it was shown that the operating point of the transmitter is not far from its optimum. In this operating point, the transmit power is in the range of 0 dBm and the DR/BW indicates that this is the limit where a low complexity modulation can be used instead of complex modulation. Of course, the amount of transferred bits and the required distance between transmitter and receiver have a deep impact on this operating point.

Furthermore, it was shown that the implementation of this novel transmitter is competitive with other high performance transmitters.

3 The BAW Device

Basically a BAW resonator consists of a piezoelectric thin film between two electrodes. The used piezoelectric material is typically aluminium-nitride (AlN). Like a quartz crystal or a surface acoustic wave (SAW) resonator, the BAW uses the piezoelectric effect to generate a resonance. Unlike the SAW, where the acoustic wave propagates along the surface, the acoustic waves in a BAW are launched into the bulk of the device [63]. Therefore it has to be ensured that the energy is not absorbed by the carrier substrate. For this reason, acoustic decoupling from substrate is required. To overcome this problem, there are basically three main approaches (shown in Figure 3.1) that can be adopted.

The first approach (Figure 3.1-left) makes use of a bulk micromachining process (backside etching) to create a cavity below the resonator. The second approach (Figure 3.1-middle) makes use of a surface micromachining process to generate a membrane keeping the resonator away from the substrate. These two types of BAW resonators are often called membrane types [64], freestanding or (thin) film bulk acoustic wave resonators (FBAR) [63, 67]. In the third approach (Figure 3.1-right), an acoustic mirror is fabricated, which reflects the waves so that they cannot propagate any further into the substrate. A more detailed cross-section of this type is shown in Figure 3.2 [66]. The resonators employed in the proposed transmitter are mirror-type BAWs, also known as solidly mounted resonators (SMR) [64, 63, 67]. The advantage of the freestanding BAW resonators compared to the SMR technology is that this kind of resonator seems to have the potential of higher quality factors (Q) due to less substrate losses. The advantages of the SMR resonators are high mechanical robustness, good heat dissipation, and lower temperature coefficients [66]. Typically, the parasitic capacitances of the electrodes of such BAWs are not equal, since the bottom electrodes have a higher capacitance against substrate due to their

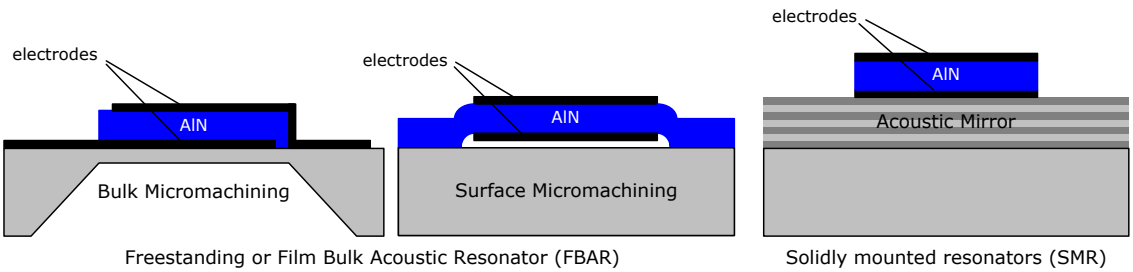


Figure 3.1: Different types of BAW resonators.

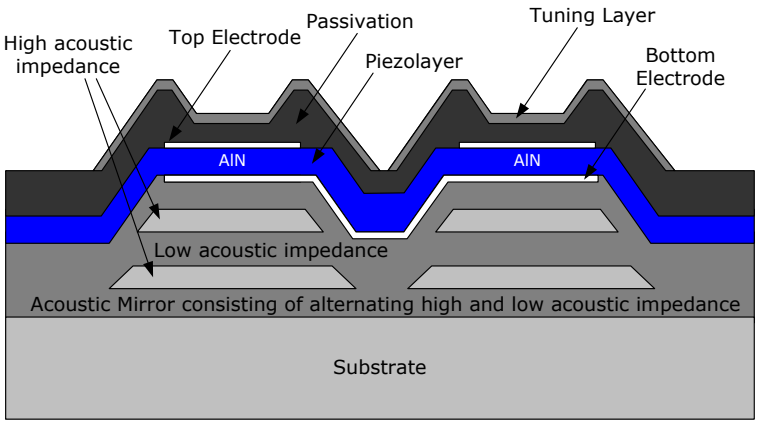


Figure 3.2: Solidly mounted resonators with acoustic mirror [66].

proximity. Therefore it can be advantageous to use two BAWs in a differential circuit, as it is in the LNA, or to use one single-ended BAW resonator.

The resonance frequency of the resonator is determined by the thickness of the piezolayer and the mass of the electrodes and of the passivation. So a tuning layer on top of the resonator (see Figure 3.2) can be used to compensate process variations and fine tune the resonance frequency of the resonator during production. Due to the lower acoustic wave speed compared to the speed of an electromagnetic wave, the wavelength is much shorter and so the BAW resonator can be very small. The thickness of the BAW is only $\lambda/2$, while the acoustic cavity in a SAW, where the interdigital transducer (IDT) is interacting with the acoustic wave over several wavelengths, is much larger. Therefore in a SAW the losses, such as diffraction loss and also mode conversion loss, are higher and the quality factor is lower, although the crystal-grown lithium tantalate typically used for SAWs has a better coupling factor than the piezolayer material in BAWs [68].

The benefits offered by a BAW device include [68]: extremely high mechanical robustness, higher quality factor (Q) than SAW devices, very small chip-size, lower temperature coefficients than SAW (but higher than state-of-the-art quartz crystals), higher ESD robustness than SAW, higher power-handling capability, and frequency limits far above 5 GHz. Additionally, the BAW resonators can be monolithically integrated (but this can be more expensive as already shown in equation 1.2 on page 22), flip-chipped, or wire bonded to the transceiver die in order to avoid external components and therefore reduce cost and size.

Another benefit is that the BAW device can be easily modelled. The equivalent circuit is shown in Figure 3.3. This circuit is the so-called modified Butterworth-Van Dyke (MBVD) model proposed in [70]. The difference from standard five element BVD model, also used for state-of-the-art quartz crystals, is a resistor R_0, which covers the acoustic losses, added in series with the plate capacitance C_0. R_a, L_a, and C_a are the motional resistance, inductance, and capacitance and R_s is used to take the

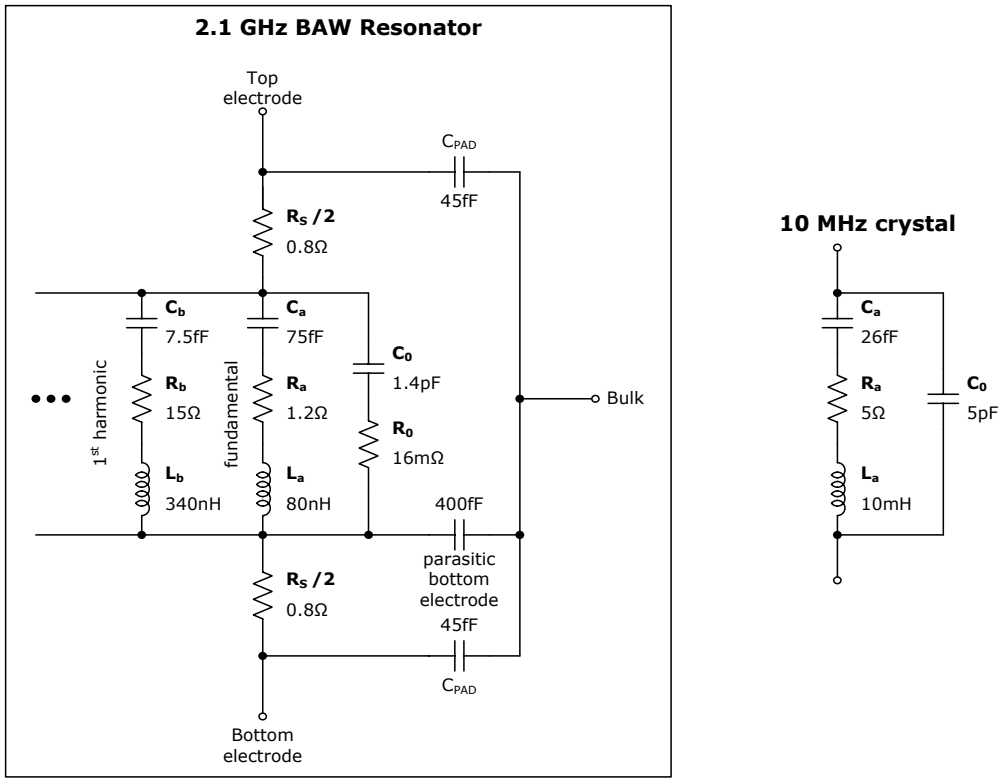


Figure 3.3: Equivalent circuit of a BAW including bulk parasitics and the first harmonic and equivalent circuit of a 10 MHz crystal (taken from [55]).

ohmic losses of the electrode into account [68]. It is important to note that parasitic capacitors against substrate are also included in the equivalent circuit. In chapter 4 oscillators utilizing BAW resonators will be compared with ones which make use of crystals. Therefore the equivalent circuit of a crystal [55] is also given in Figure 3.3.

The used model was approximated by applying a least square estimation. The least square method fits the model to the measurement data by minimizing the sum of the squared residuals. The choice of these residuals is essential to guarantee a match of the absolute value of the impedance as well as to match the phase angle equally. It is also very important that the residual is weighted in such a way that deviations at very low values (series resonance) and at very high values (parallel resonance) of the impedance are considered similarly. For this reason, the residual was defined as deviation of the reflection coefficient of the prediction from the measurement. This is equal to the geometric distance in the Smith Chart, which is illustrated in Figure 3.4. Additionally, a weight function $W(f_n)$ was introduced to ensure that the model fits the measurement data in the frequency range of interest. The sum of the squared

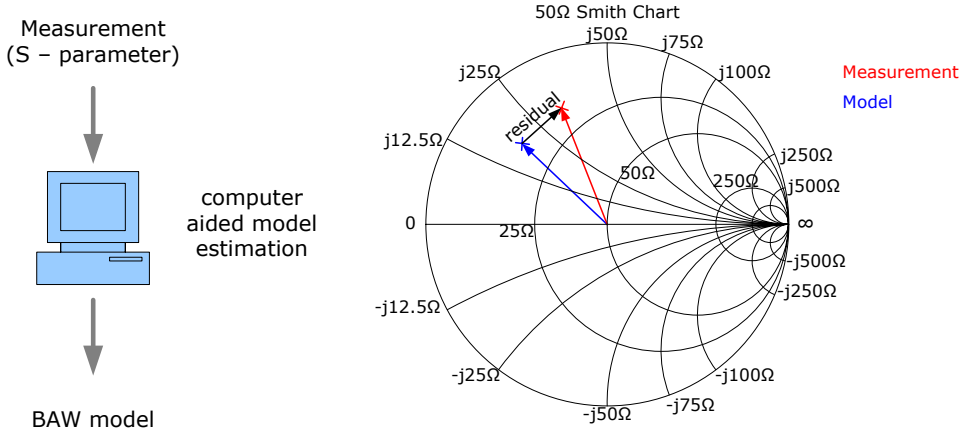


Figure 3.4: Basic principle of the computer-aided model estimation of the BAW resonator.

residuals SlS was calculated as follows:

$$SlS = \sum_{n=1}^{N} W(f_n) \cdot \cdot \left[\left(\Re\{\underline{S}_{11_{\text{model}}}(f_n)\} - \Re\{\underline{S}_{11_{\text{meas}}}(f_n)\} \right)^2 + \left(\Im\{\underline{S}_{11_{\text{model}}}(f_n)\} - \Im\{\underline{S}_{11_{\text{meas}}}(f_n)\} \right)^2 \right] \tag{3.1}$$

The result of the computer-aided model estimation is shown in Figure 3.5 for the impedance and in Figure 3.7 for the reflection coefficient. The model fits the measurement data very well and covers also two harmonics. In Figure 3.6 we can see the impedance in the region of interest. The series resonance frequency is smaller than the parallel resonance frequency. In between, the resonator behaves like an inductor (phase shift of +90°) and for frequencies smaller than the series frequency or higher than the parallel resonance frequency the resonator acts as a capacitor (phase shift of -90°). A further comparison between the measurement and the simulation of the model is shown in the Smith Chart in Figure 3.8.

Thanks to the consistency between the model and the measurements, the key figures of the resonator can be ascertained from the model much more easily than by doing direct measurements.

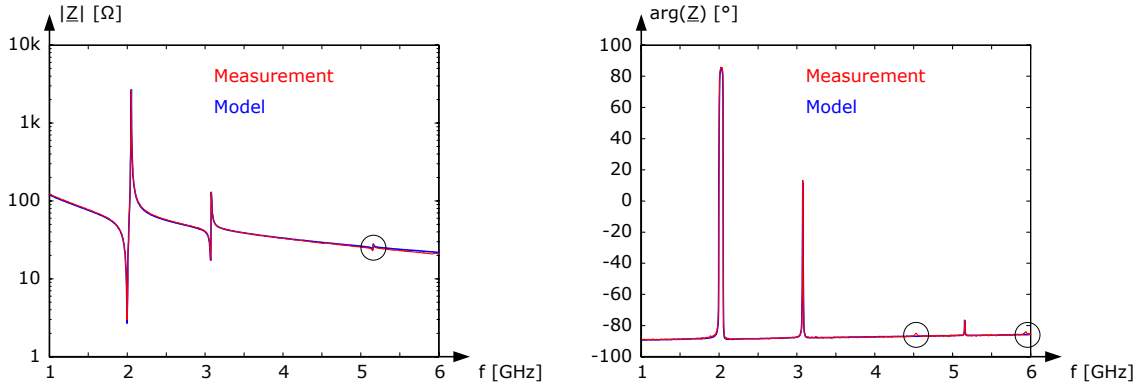


Figure 3.5: Measured impedance of the BAW resonator (2.1 GHz) and simulated impedance of the BAW model.

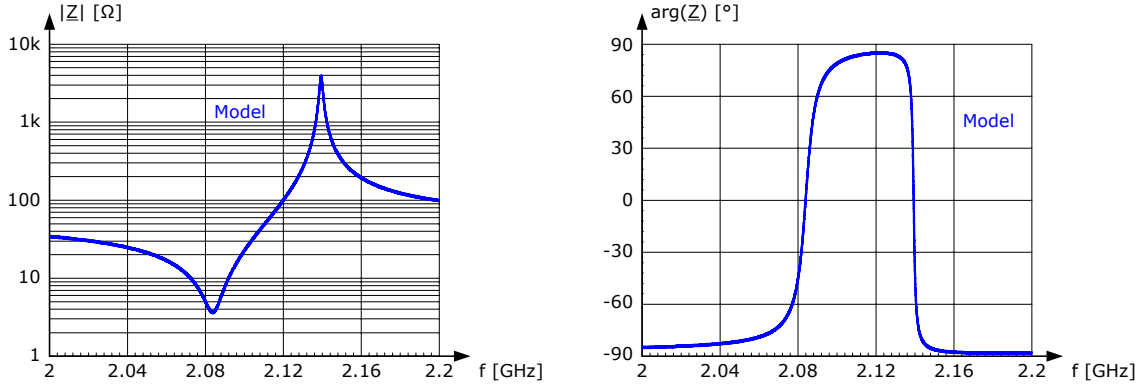


Figure 3.6: Simulated impedance of the BAW model (zoomed in).

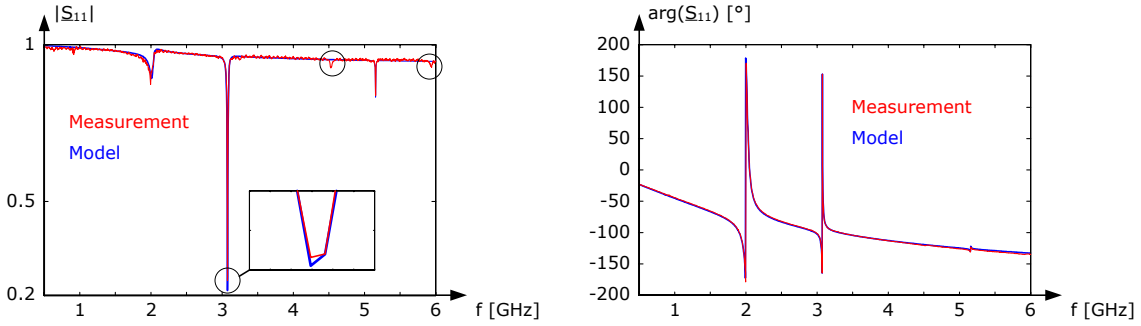


Figure 3.7: Measured S-parameter (reflection coefficient) of the BAW resonator (2.1 GHz) and simulated S-parameter of the BAW model.

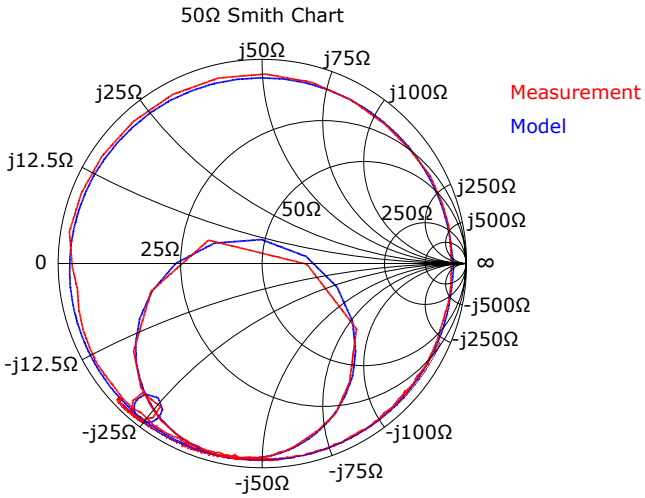


Figure 3.8: Smith Chart of the measured S-parameter (reflection coefficient) of the BAW resonator (2.1 GHz) and simulated S-parameter of the BAW model.

The most important parameters of a SMR resonator are [68]:

- Q_s: Quality factor at series resonance frequency f_s
- Q_p: Quality factor at parallel resonance frequency f_p
- Z_{C_0}: Absolute value of the impedance of C_0 at $(f_\mathrm{p}+f_\mathrm{s})/2$ (e.g. 60 Ω or 100 Ω)
- Z_min: Impedance at the series resonance frequency f_s
- Z_max: Impedance at the parallel resonance frequency f_p
- C_0: Plate capacitance
- BW_BAW: Relative bandwidth determined by $BW_\mathrm{BAW} = (f_\mathrm{p}-f_\mathrm{s})/f_\mathrm{p}$
- k^2_eff: Effective piezoelectric coupling factor; determines energy exchange between electrical and mechanical domain: $k^2_\mathrm{eff} = \frac{\pi^2}{4}\frac{f_\mathrm{s}}{f_\mathrm{p}}\frac{f_\mathrm{p}-f_\mathrm{s}}{f_\mathrm{p}} \approx 2.4 \cdot BW$

The quality factor Q_s and Q_p can be different due to the impact of the different losses. The ohmic losses of the electrodes, which are modelled with R_s, have a higher impact on the quality factor at the series resonance frequency, whereas the resistor R_0 in series to the plate capacitance C_0 mainly affects the quality factor at the parallel resonance frequency.

4 The BAW Oscillator

4.1 Oscillation Theory

An oscillator is basically based on a positive feedback from the output of an amplifier back to its input (see Figure 4.1) [55]. The transfer function of this system is described by equation 4.1.

$$\underline{H}(\mathrm{j}\omega) = \frac{\underline{A}(\mathrm{j}\omega)}{1 - \underline{A}(\mathrm{j}\omega)\underline{B}(\mathrm{j}\omega)} \tag{4.1}$$

If Barkhausen's criterion [61] is fulfilled, no input is needed to generate a sinusoidal output signal. Barkhausen's criterion is a necessary condition for oscillation, but it is not sufficient. The criterion can easily be applied to the model of a one-port oscillator, but more detailed information can be gained from the Nyquist stability criterion, which will be used later for the one-port model. The one-port model of an oscillator consists of a negative impedance converter (NIC) and a load, which represents the resonator. The feedback model and the one-port model are illustrated in Figure 4.1. The NIC is represented by the transfer function $\underline{A}(\mathrm{j}\omega)$, whereas the resonator is modelled with $\underline{B}(\mathrm{j}\omega)$. Assuming that the current $\underline{i}$ at the resonator is the input of the NIC and the voltage $\underline{v}$ is the output of the NIC yields:

$$\begin{aligned} \underline{A}(\mathrm{j}\omega) &= \frac{\underline{v}}{\underline{i}} = \underline{Z}_{\mathrm{NIC}}(\mathrm{j}\omega) \\ \underline{B}(\mathrm{j}\omega) &= \frac{\underline{i}}{\underline{v}} = -\frac{1}{\underline{Z}_{\mathrm{Res}}(\mathrm{j}\omega)} \end{aligned} \tag{4.2}$$

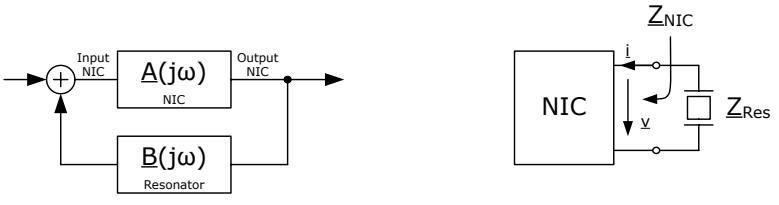


Figure 4.1: The feedback amplifier model and the one-port model of an oscillator.

If these equations are plugged into Barkhausen's criterion the following equations are obtained:

$$\begin{aligned} |\underline{A}(\mathrm{j}\omega)\underline{B}(\mathrm{j}\omega)| = 1 \quad &\rightarrow \quad |\underline{Z}_{\mathrm{NIC}}(\mathrm{j}\omega)| = |\underline{Z}_{\mathrm{Res}}(\mathrm{j}\omega)| \\ \varphi_A + \varphi_B = 0^\circ \quad &\rightarrow \quad \varphi_{\mathrm{NIC}} + 180^\circ - \varphi_{\mathrm{Res}} = 0 \\ &\rightarrow \quad \varphi_{\mathrm{NIC}} = \varphi_{\mathrm{Res}} - 180^\circ \end{aligned} \tag{4.3}$$

From these equations it can be seen that the real part of the sum of the impedances and the imaginary part of the sum of the impedances have to be zero, or that:

$$\Re\{\underline{Z}_{\mathrm{NIC}}(\mathrm{j}\omega)\} = -\Re\{\underline{Z}_{\mathrm{Res}}(\mathrm{j}\omega)\} \quad \text{and} \quad \Im\{\underline{Z}_{\mathrm{NIC}}(\mathrm{j}\omega)\} = -\Im\{\underline{Z}_{\mathrm{Res}}(\mathrm{j}\omega)\} \tag{4.4}$$

As a consequence the real part of the impedance of the NIC must be negative, if the real part of the impedance of the resonator is positive. On the other hand the resonator has to operate in its inductive region if the output impedance of the NIC is capacitive or the other way round. To guarantee proper start-up of the oscillation, in any practical implementation of an oscillator the loop gain is typically higher than one ($|\underline{A}(\mathrm{j}\omega)\underline{B}(\mathrm{j}\omega)| \geq 1$). As a result of equations 4.2 to 4.4, the absolute value of the impedance $|\underline{Z}_{\mathrm{NIC}}(\mathrm{j}\omega)|$ has to be higher than the absolute value of the impedance $|\underline{Z}_{\mathrm{Res}}(\mathrm{j}\omega)|$. But this is only true if the current $\underline{i}$ is the input of the NIC. Assuming voltage $\underline{v}$ as input of the NIC, the role of $\underline{Z}_{\mathrm{NIC}}(\mathrm{j}\omega)$ and $\underline{Z}_{\mathrm{Res}}(\mathrm{j}\omega)$ are interchanged. Both cases are shown in equation 4.5:

$$\begin{aligned} \text{If} \quad \underline{A}(\mathrm{j}\omega) = \frac{\underline{i}}{\underline{v}} = \frac{1}{\underline{Z}_{\mathrm{NIC}}(\mathrm{j}\omega)} \quad &\text{and} \quad \underline{B}(\mathrm{j}\omega) = \frac{\underline{v}}{\underline{i}} = -\underline{Z}_{\mathrm{Res}}(\mathrm{j}\omega) \quad \rightarrow \\ |\underline{A}(\mathrm{j}\omega)\underline{B}(\mathrm{j}\omega)| \geq 1 \quad &\rightarrow \quad |\underline{Z}_{\mathrm{Res}}(\mathrm{j}\omega)| \geq |\underline{Z}_{\mathrm{NIC}}(\mathrm{j}\omega)| \\ \text{If} \quad \underline{A}(\mathrm{j}\omega) = \frac{\underline{v}}{\underline{i}} = \underline{Z}_{\mathrm{NIC}}(\mathrm{j}\omega) \quad &\text{and} \quad \underline{B}(\mathrm{j}\omega) = \frac{\underline{i}}{\underline{v}} = -\frac{1}{\underline{Z}_{\mathrm{Res}}(\mathrm{j}\omega)} \quad \rightarrow \\ |\underline{A}(\mathrm{j}\omega)\underline{B}(\mathrm{j}\omega)| \geq 1 \quad &\rightarrow \quad |\underline{Z}_{\mathrm{NIC}}(\mathrm{j}\omega)| \geq |\underline{Z}_{\mathrm{Res}}(\mathrm{j}\omega)| \end{aligned} \tag{4.5}$$

Depending on the definition of input and output of the NIC, two different conditions for oscillation are obtained. It seems as if there exist two different types of NICs. These two basic types are shown in Figure 4.2.

In the first example (see Figure 4.2 top) the input of the NIC is a voltage. This voltage is amplified by a factor of two. The voltage across the resistor, which is connected between the output of the amplifier and its positive input, is therefore equal to the input voltage $\underline{v}$. This causes a current $\underline{i}$ flowing out of the port and hence the input resistance is negative. If the port of the NIC is shorted, the voltage at the input of the amplifier is zero. If a resistor with a resistance smaller than R is connected to the port, a voltage $\underline{v}$ at the input of the amplifier will cause a current $\underline{i}$, which is too small to generate the same voltage across the load. Therefore at the steady state operating point no current is flowing and all voltages are zero. This type of oscillator is stable if the port is shorted or even if a load smaller than R, is

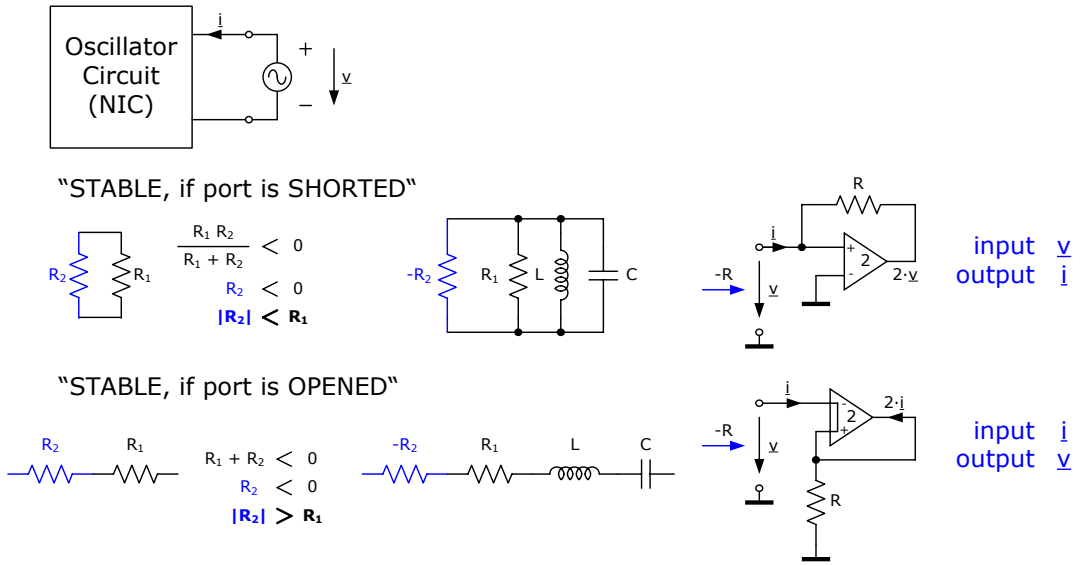


Figure 4.2: Two types of negative impedance converters (NIC).

connected to the port. The resistance of the load must be higher than R at the desired frequency to ensure oscillation. Therefore, typically a parallel resonance circuit is used to bring this NIC type into oscillation. A resistor with a negative resistance $-R_2$ in parallel to a parallel resonance circuit can compensate the losses R_1 of the LC tank. To achieve an overall negative resistance, the absolute value $|-R_2|$ has to be larger than R_1 (see Figure 4.2 top).

The second example (see Figure 4.2 bottom) is the exact opposite of the first one. In this example, the current I of the load is sensed and the amplifier provides twice as much current, but in the opposite direction. Because of this positive feedback the voltage across the resistor is $\underline{v} = -R \cdot \underline{i}$, again causing a negative input resistance. Using this topology, the resistance of the load has to be lower than R to have a loop gain higher than one, which is required to guarantee an oscillation. This kind of NIC is stable if the port is open or even if a load greater than R, is connected. Consequently, a series resonance circuit can be used as load. To compensate the losses R_1 of a series LC tank, a resistor with a negative resistance with an absolute value $|-R_2|$ larger than R_1 has to be applied.

But what happens when a resonator, which is a combination of parallel and series resonance circuit, is connected to a NIC? In Figure 4.3 we can see two constellations: In the first case, C_0 is detached from the resonator and therefore acts as a part of the NIC [56]; whereas in the second case C_0 is part of the resonator. Applying Barkhausen's criterion (equation 4.4) does not provide a unique solution, because there exist three possibilities, where the sum of the real and the sum of the imaginary part of the impedances can be zero. In case one, when C_0 is part of the NIC, the parallel connection of C_0 and $-R_{\mathrm{NIC}}$ has to be transformed into a series connection of

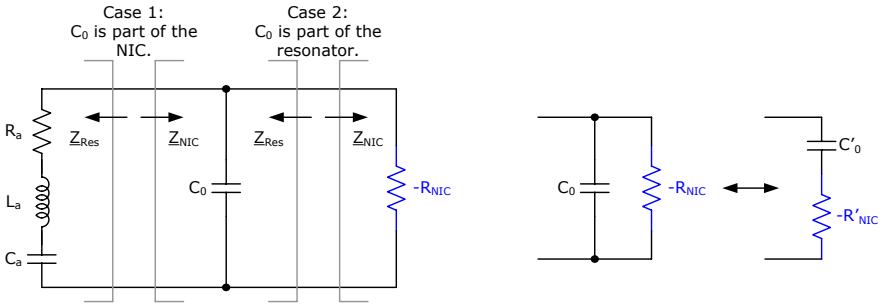


Figure 4.3: C_0 can be considered as part of the resonator or as part of the NIC.

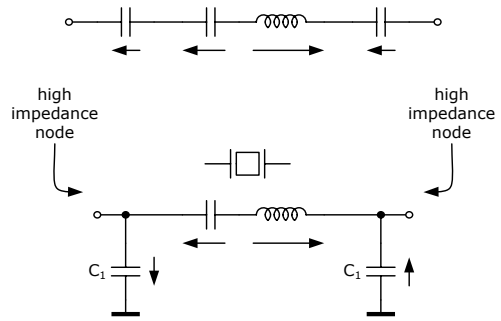


Figure 4.4: Although the resonator is in series resonance, the capacitors C_1 can be used to generate high impedance nodes.

C_0' and $-R_{\mathrm{NIC}}'$ by using the following equations:

$$\begin{aligned} -R_{\mathrm{NIC}}' &= -R_{\mathrm{NIC}} \frac{(\frac{1}{\omega C_0})^2}{(\frac{1}{\omega C_0})^2 + R_{\mathrm{NIC}}^2} \\ \frac{1}{\omega C_0'} &= \frac{1}{\omega C_0} \frac{R_{\mathrm{NIC}}^2}{(\frac{1}{\omega C_0})^2 + R_{\mathrm{NIC}}^2} \end{aligned} \tag{4.6}$$

Hence the resonance frequency can be calculated to $\omega_1 = \frac{1}{\sqrt{L_a C_a}} \sqrt{1 + \frac{C_a}{C_0'}}$. Since C_0' is larger than C_0 the oscillator can oscillate on every arbitrary frequency between the series and parallel resonance frequency. Because of the dependency of C_0' on R_{NIC}, the resonance frequency will be very close to the series resonance frequency for a small R_{NIC} (C_0' is large) and on the other hand, the resonance frequency will be very close to the parallel resonance frequency if R_{NIC} is large (C_0' is equivalent to C_0). These two possible extreme values of the resonance frequency can be seen easily from case two, where C_0 is part of the resonator. At the series resonance frequency the impedance of the resonator is at its minimum and purely resistive, which can be compensated by $-R_{\mathrm{NIC}}$ to fulfill equation 4.4. The same can be true for the parallel resonance frequency, where the impedance is at its maximum. Then a larger value of $-R_{\mathrm{NIC}}$ is required to satisfy equation 4.4. Thus from Barkhausen's criterion the only information that can be gained is that the frequency of the oscillation

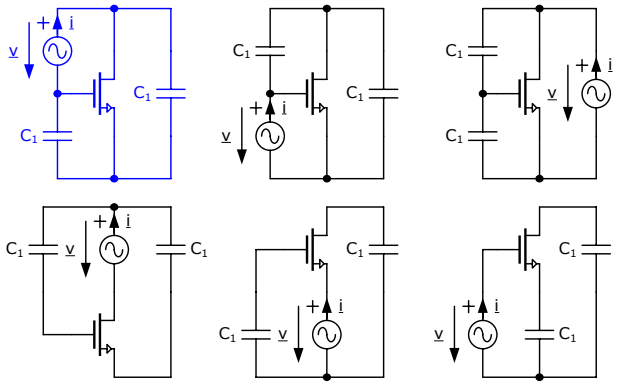


Figure 4.5: Single-transistor circuits, but only the blue configuration can provide a negative input impedance.

is between the series resonance ($\omega_\mathrm{s} = \frac{1}{\sqrt{L_\mathrm{a} C_\mathrm{a}}}$) and the parallel resonance frequency ($\omega_p = \frac{1}{\sqrt{L_\mathrm{a} C_\mathrm{a}}} \sqrt{1 + \frac{C_\mathrm{a}}{C_0}}$), although the impedance of the NIC is purely resistive.

Resonance occurs when capacitors and inductors are involved and electrical energy oscillates between them. If only the motional capacitance C_a and inductance L_a are involved, the oscillator oscillates at the series resonance frequency. If the bulk capacitance C_0 is involved too, the oscillator will operate at its parallel resonance frequency. As already shown, the external circuit has an impact on this involvement. In many practical cases the impedance of the NIC additionally has a capacitive part. In this case it is quite obvious that the resonator must operate in its inductive region between series and parallel resonance frequency. Since only one type of one-transistor oscillator exists, and the oscillation frequency can exhibit arbitrary values between ω_s and ω_p, a subdivision into different types makes no sense. This is also supported by the argument that the series resonance frequency can easily be transformed into a high impedance node by using simple circuits. Such a circuit is illustrated in Figure 4.4. Although the resonator is operating at the series resonance frequency, the in- and output node are high impedance nodes. Furthermore, the output is shifted by 180° with respect to the input. A differentiation makes sense for two-stage oscillators as will be explained in the chapter after next.

4.2 One-Transistor Oscillators

A single transistor is sufficient to generate a negative resistance. In addition to the transistor, components for realizing the positive feedback are required. In the following, only capacitors are considered, because they can be integrated easily. In general, inductors or transformers can also be used, resulting in different groups of oscillators, such as Hartley or Meissner [42]. In Figure 4.5 all possible combinations of one single transistor with two capacitors are depicted. The voltage source represents the port. If a voltage $\underline{v}$ causes a current $\underline{i}$ flowing in the opposite direction, the

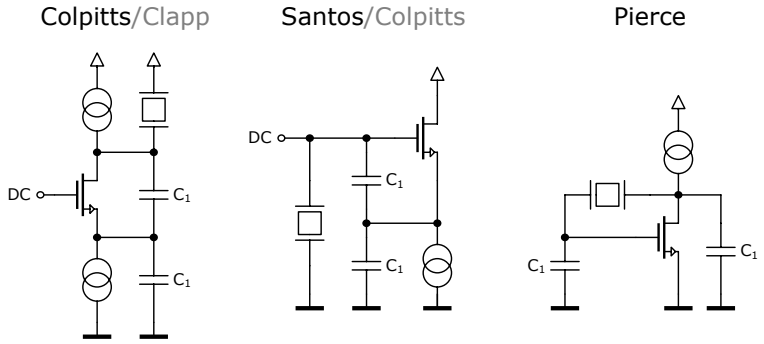


Figure 4.6: Different single-transistor oscillators, depending on the grounded node of the transistor.

circuit acts as an active device. Unfortunately, the analyses of these basic configurations showed that only one input impedance of these 6 circuits exhibits a negative resistance. For this reason, only one basic single-transistor oscillator exists (the blue circuit in Figure 4.5). Depending on the node, which is connected to ground, three different types of oscillators can be distinguished. These types are illustrated in Figure 4.6. The naming of these three basic types of single-transistor oscillators is not consistent in literature, the most common [55] is also given in Figure 4.6. All these basic types have the same input impedance, which can easily be calculated to [20]:

$$\underline{Z}_{\mathrm{NIC}} = -\frac{g_{\mathrm{m}}}{\omega^2 C_1^2} - \mathrm{j}\frac{2}{\omega C_1} \tag{4.7}$$

Sometimes it is advantageous to consider C_0 of the resonator to be part of the oscillator. If the impedance $\frac{1}{\mathrm{j}\omega C_0}$ is connected in parallel to the impedance given in equation 4.7, the input impedance of the oscillator can be calculated to:

$$\underline{Z}_{\mathrm{NIC\_C_0}} = \frac{g_{\mathrm{m}} + 2\mathrm{j}\omega C_1}{\mathrm{j}\omega C_0 g_{\mathrm{m}} - \omega^2 C_1^2 - 2\frac{C_0}{C_1}\omega^2 C_1^2} \tag{4.8}$$

To simplify the calculation of the oscillation frequency, the Nyquist stability criterion will be applied. A system is unstable and will start oscillating if the two complex conjugate poles of the transfer function are on the right side of the complex plane. These poles are determined by calculation of the zeros of the denominator polynomial of equation 4.1. As before, the impedances are plugged into the equation. But now both definitions of in- and output yield to the following equation 4.9:

$$\underline{Z}_{\mathrm{NIC}}(s) + \underline{Z}_{\mathrm{Res}}(s) = 0 \quad \rightarrow \text{poles} \tag{4.9}$$

To give an example, a simple LC series tank is used as resonator. The impedances

are given by:

$$\begin{aligned} \underline{Z}_{\mathrm{Res}}(s) &= R_{\mathrm{a}} + \frac{1}{sC_{\mathrm{a}}} + sL_{\mathrm{a}} \\ \underline{Z}_{\mathrm{NIC}}(s) &= -R_{\mathrm{NIC}} \end{aligned} \tag{4.10}$$

Hence the conjugate complex poles can be calculated to:

$$s_{1,2} = \frac{R_{\mathrm{NIC}} - R_{\mathrm{a}}}{2L_{\mathrm{a}}} \pm \mathrm{j}\sqrt{\frac{1}{L_{\mathrm{a}}C_{\mathrm{a}}} - \frac{(R_{\mathrm{NIC}} - R_{\mathrm{a}})^2}{4L_{\mathrm{a}}^2}} \tag{4.11}$$

To ensure that the poles are on the right complex plane, R_{NIC} must be larger than R_{a}. This is the same result as that shown in the bottom example of Figure 4.2. A second condition for oscillation is that the two poles are complex conjugate. A pure real pole on the right plane would only cause a DC instability. To satisfy the requirements for oscillation, R_{NIC} has to fulfill following condition 4.12:

$$R_{\mathrm{a}} \leq R_{\mathrm{NIC}} \leq R_{\mathrm{a}} + \sqrt{\frac{4L_{\mathrm{a}}}{C_{\mathrm{a}}}} \tag{4.12}$$

Considering the initial condition, which defines the amplitude A_0 and phase φ_0 at the time $t = 0$, the solution of the differential equation can be described by:

$$\begin{aligned} v_{\mathrm{out}}(t) &= A_0 \cdot e^{\Re\{s_{1,2}\}t} \cos(\Im\{s_{1,2}\}t + \varphi_0) = \\ &= A_0 \cdot e^{\frac{R_{\mathrm{NIC}} - R_{\mathrm{a}}}{2L_{\mathrm{a}}}t} \cos(\sqrt{\frac{1}{L_{\mathrm{a}}C_{\mathrm{a}}} - \frac{(R_{\mathrm{NIC}} - R_{\mathrm{a}})^2}{4L_{\mathrm{a}}^2}}t + \varphi_0) \end{aligned} \tag{4.13}$$

The considerations used in this simple example can now be applied to the one-transistor oscillator shown in Figure 4.5. The impedance $\underline{Z}_{\mathrm{NIC}}$ is given in equation 4.7 and in equation 4.8 respectively. The equivalent circuit of the BAW resonator is very similar to the equivalent circuit of a quartz crystal, and hence the results can be used for both types of resonators. To point out the challenges of the BAW oscillator design, both resonators are directly compared in the following figures. The used model of the 10 MHz quartz crystal was taken from [55] and the values are $C_{\mathrm{a}} = 26\,\mathrm{fF}$, $L_{\mathrm{a}} = 10\,\mathrm{mH}$, $R_s = 5\,\Omega$, and $C_0 = 5\,\mathrm{pF}$. To allow a simple comparison of the resonance frequency, the pulling factor [56] is introduced. The pulling factor is the relative deviation of the oscillation frequency from the series resonance frequency (equation 4.14).

$$p = \frac{\omega - \omega_{\mathrm{s}}}{\omega_{\mathrm{s}}} = \frac{f - f_{\mathrm{s}}}{f_{\mathrm{s}}} \tag{4.14}$$

The analytical solution of equation 4.9 was obtained by using the symbol tool box of MATLAB®. Because of the complexity of the solutions, only the results are presented in this work. In the left plot of Figure 4.7 the real part of the complex conjugate poles is illustrated. The value of the real part of the poles affects the turn on time

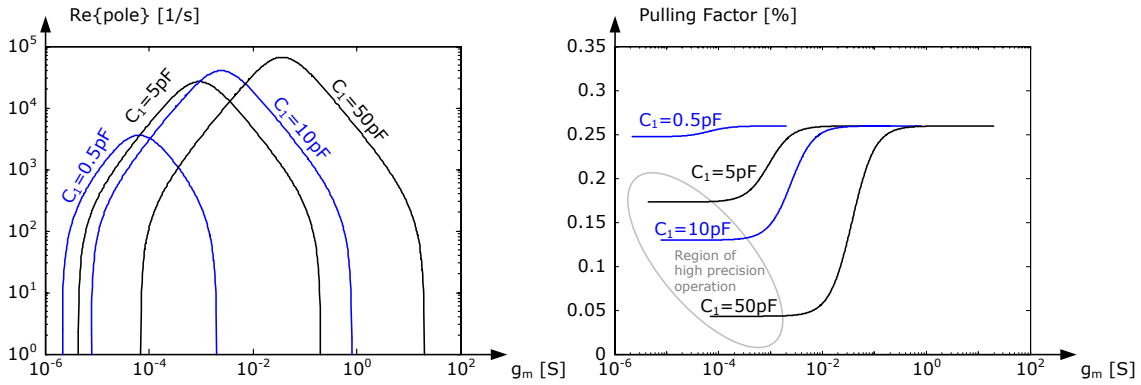


Figure 4.7: Plot of the real part of the complex conjugate poles and of the pulling factor against transconductance g_m (10 MHz quartz crystal).

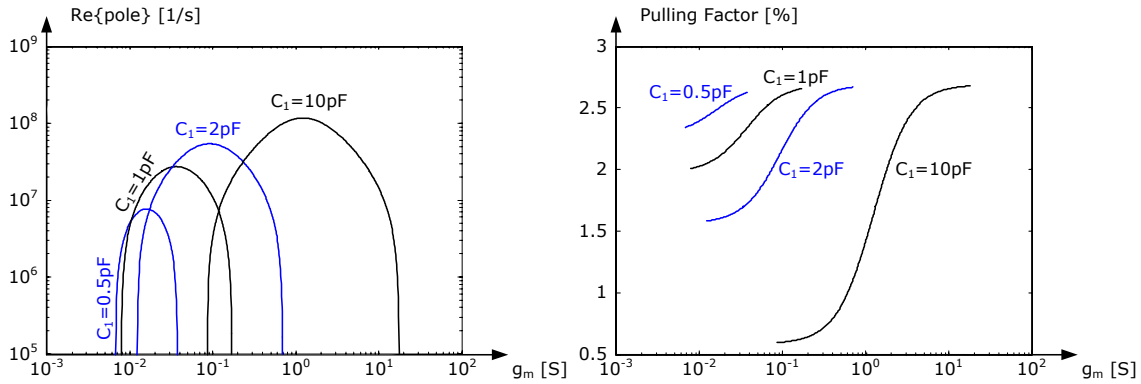


Figure 4.8: Plot of the real part of the complex conjugate poles and of the pulling factor against transconductance g_m (2.1 GHz BAW resonator).

of the oscillator. On the right side of Figure 4.7 the pulling factor can be seen. The pulling factor is calculated from the imaginary part of the poles. All curves are given for different values of C_1. From the curves a minimum g_m required for oscillation can be found. This minimum g_m increases with a higher value of C_1 and consequently so does the current consumption. On the other hand, a higher C_1 will cause the oscillator to resonate more closely to the series resonance frequency. For quartz crystal oscillators, a resonance frequency close to the series resonance frequency is preferred, because the parallel resonance frequency depends on C_0, which is mainly caused by the parasitic capacitances, such as the package capacitance. A further advantage of a high C_1 is that the resonance frequency is nearly constant with varying g_m. The value of C_1 is the only design choice [55] which can be made. As long as the oscillator's input impedance is capacitive, the oscillator operates in the inductive region of the resonator. So the pulling factor is limited for quartz crystals to values between 0% (series resonance frequency) and about 0.25% (parallel resonance frequency).

In Figure 4.8 the same plots are given for a BAW resonator. Since the equivalent circuit of a BAW resonator is very similar to that of a quartz crystal, the curves look

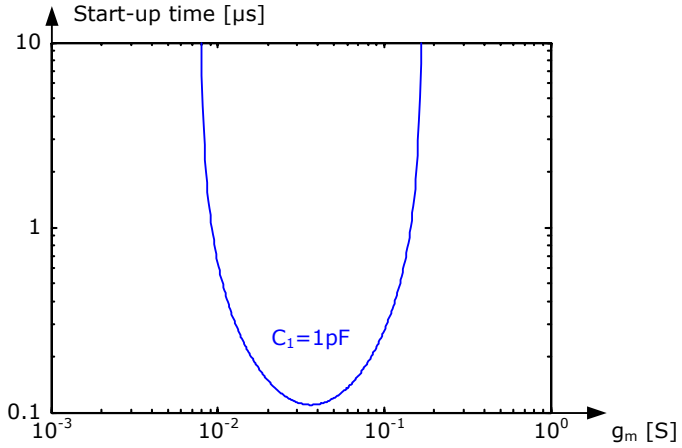


Figure 4.9: Start-up time of the one-transistor oscillator against transconductance g_m (2.1 GHz BAW resonator).

quite similar. But these plots show several important differences:

- A much higher g_m is required to start up an oscillation.
- The real part of the poles is three orders of magnitude higher and for this reason the start-up time is much shorter.
- The dependency of the oscillating frequency on the transconductance g_m is much higher.
- The difference between series and parallel resonance is much higher (about 2.5%) compared to that of the quartz crystal (about 0.25%) and hence the tuning range can be wider.

The absolute value of the real part of the pole in equation 4.11 is the inverse time constant τ of the oscillator. It is assumed that three time constants are needed for the start-up. This results in an approximation for the start-up time:

$$t_{\mathrm{start\_up}} = 3 \cdot \tau = 3 \cdot \frac{2L_\mathrm{a}}{-\Re\{\underline{Z}_{\mathrm{NIC\_C_0}}\} - R_\mathrm{a}} \tag{4.15}$$

In this case the capacitance C_0 is considered to be part of the oscillator. Hence for $\underline{Z}_{\mathrm{NIC\_C_0}}$ equation 4.8 can be used. The start-up time for the largest used C_1 (1 pF) is plotted in Figure 4.9. The root locus of one pole is shown in Figure 4.10. The minimum required transconductance g_m of the one-transistor oscillator can be approximated by using equation 4.12. If the impact of C_0 is disregarded, the negative impedance of the NIC is given by equation 4.7. This approximation is only valid if the resonance frequency is close to the series resonance frequency of the resonator. Using the real part of $\underline{Z}_\mathrm{NIC}$ results in:

$$R_\mathrm{a} \leq |\Re\{\underline{Z}_\mathrm{NIC}\}| = \frac{g_\mathrm{m}}{\omega^2 C_1^2} \quad \rightarrow g_\mathrm{m} \geq \omega^2 C_1^2 R_\mathrm{a} \approx \omega \frac{C_1^2}{C_\mathrm{a}} \frac{1}{Q} \tag{4.16}$$

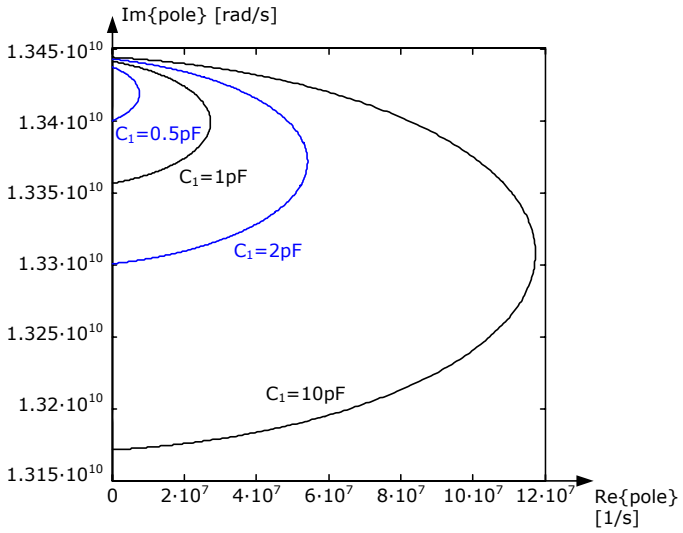


Figure 4.10: Root locus plot of one pole of the two complex conjugate poles (one-transistor oscillator and 2.1 GHz BAW resonator).

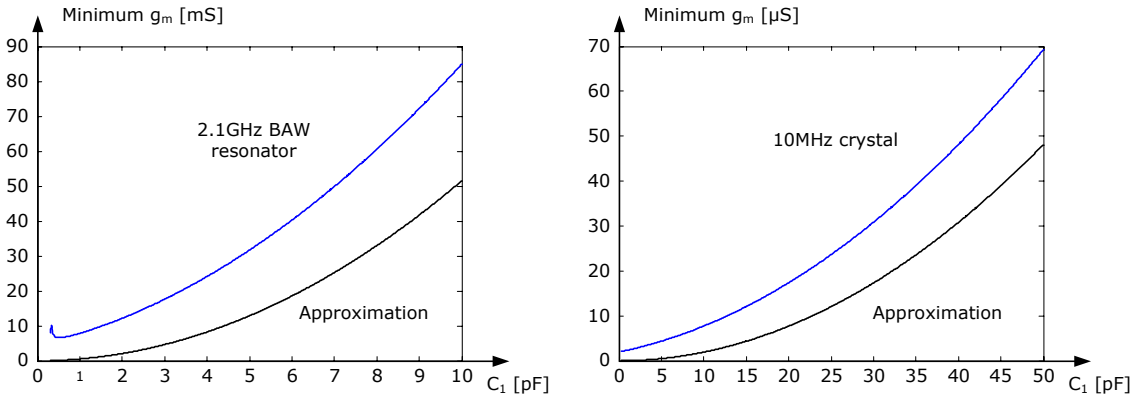


Figure 4.11: Minimum required transconductance g_m for a BAW and for quartz crystal based oscillator.

This approximation and the exact solution of the minimum g_m is illustrated in Figure 4.11. The required transconductance of the oscillator increases with increasing frequency and with higher C_1 squared and with increasing motional resistance R_a. Since the motional resistance of the equivalent circuit (see Figure 3.3 on page 55) of the BAW resonator and of the used crystal have approximately the same size, the required g_m is more than four orders of magnitude higher for the same value of C_1. Actually only smaller values of C_1 can be used for the high frequency BAW resonator. Assuming a four times smaller C_1 the required g_m is still three orders of magnitudes higher and because of this the current consumption of a one-transistor circuit for a BAW resonator is much higher too.

To illustrate the solution of equation 4.9, the impedances of the BAW resonator ($\underline{Z}_\mathrm{Res}$) and of the NIC ($\underline{Z}_\mathrm{NIC}$) are analyzed separately for different g_m. The left plot of

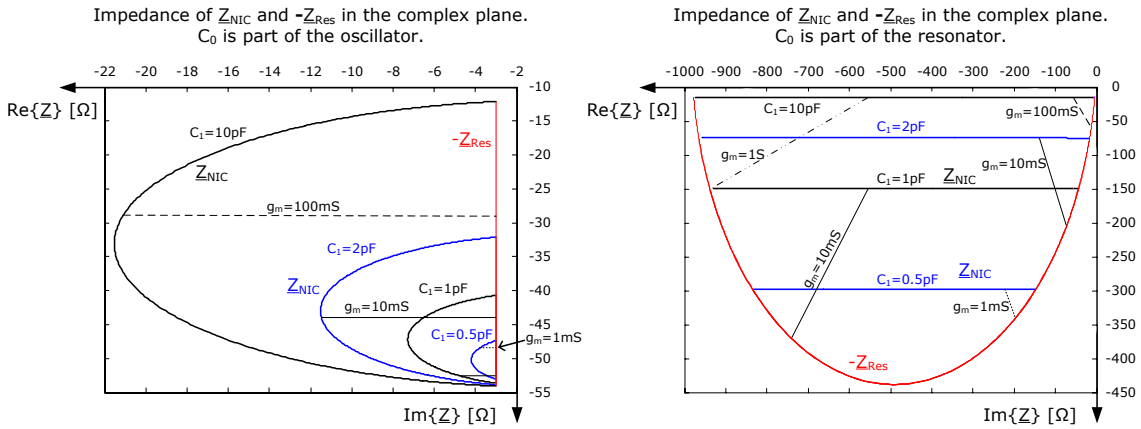


Figure 4.12: The impedances of the BAW resonator ($\underline{Z}_{\mathrm{Res}}$) and of the NIC ($\underline{Z}_{\mathrm{NIC}}$) for different g_{m}.

Figure 4.12 shows $\underline{Z}_{\mathrm{Res}}$ and $\underline{Z}_{\mathrm{NIC\_C_0}}$ (see equation 4.8), where C_0 is considered to be a part of the oscillator. This point of view simplifies the resonator to a simply series LC tank, which has a constant real part and hence can be described with a simple line in the complex plane. The right plot of Figure 4.12 illustrates the impedances where C_0 is part of the oscillator. In this case, the resonator is represented by a half circle ranging from a very low impedance (series resonance) to high impedances (parallel resonance). In both approaches, the resonator operates in the inductive region, whereas the oscillator behaves capacitively. In both plots, only pairs of $\underline{Z}_{\mathrm{NIC}}$ and $\underline{Z}_{\mathrm{Res}}$ which will oscillate are plotted. Some data pairs are connected with black lines. It is important to note that in both cases the sum of the real parts and the sum of the imaginary parts are only zero at two points. The sum of the real parts and the sum of the imaginary parts for both cases are plotted in Figure 4.13.

The absolute value of the impedances $\underline{Z}_{\mathrm{NIC}}$ and $\underline{Z}_{\mathrm{Res}}$ are shown in Figure 4.14. If C_0 is considered to be a part of the oscillator, the absolute value of $\underline{Z}_{\mathrm{NIC}}$ is always larger than the absolute value of $\underline{Z}_{\mathrm{Res}}$. In contrast, the absolute value of $\underline{Z}_{\mathrm{NIC}}$ is always smaller if C_0 is part of the resonator. Therefore the absolute value of the impedance cannot be a criterion for distinguishing between two different types of oscillators. For two-stage oscillators it makes more sense, as will be shown in the next chapter. As shown in the previous plots, the oscillation frequency only depends on the value of C_1 and g_{m}.

Why the one-transistor oscillators shown are not considered to be a good choice for a BAW oscillator in the 0.13 µm CMOS technology used can be summarized as follows:

- The required transconductance g_{m} of a one-transistor oscillator has to be very high for high frequencies. Hence the current consumption is quite high.
- The transconductance g_{m} has more impact on the resonance frequency compared to a quartz crystal oscillator, even if the oscillator is operating close to the series

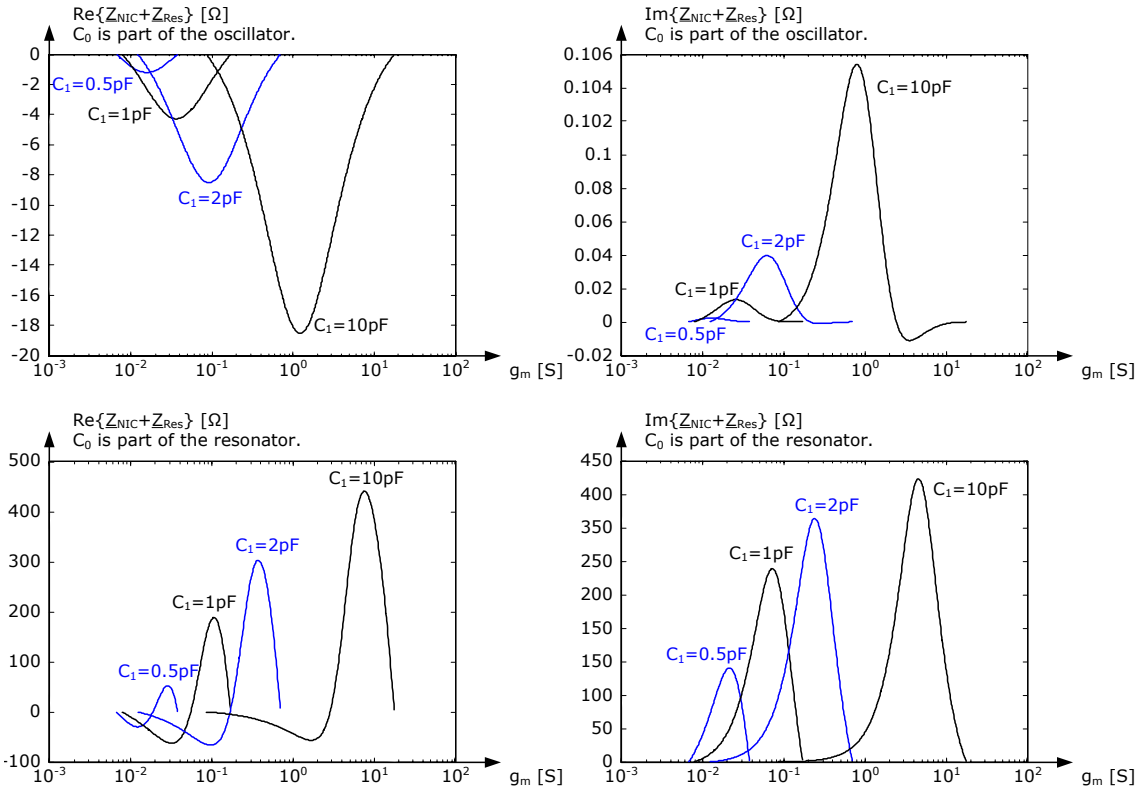


Figure 4.13: Real part and imaginary part of the sum of the impedances.

resonance frequency.

- A quartz crystal oscillator typically tends to operate very close to the series resonance frequency, which is the internal quartz crystal frequency [55]. For this reason, the capacitance C_0 has no impact and thus the resonance frequency of the oscillator is independent of packaging and mounting [55]. Additionally, the transconductance g_m has only a minor impact on the resonance frequency (see Figure 4.7). For a high frequency BAW resonator, the inductance of the interconnection between resonator and oscillator (e.g. bondwire) can have the same influence as parasitic capacitances. For example, a capacitor of 1 pF in parallel to the resonator detunes the parallel resonance frequency about 4800 ppm (10 MHz). But also an inductance of 1 nH in series to the resonator causes a shift in the series resonance frequency of about 6300 ppm. So accuracy is not an adequate reason to use an oscillator operating point close to the series resonance frequency for high frequency applications.

- As described in chapter 3 the quality factor Q_s at series resonance frequency can be different from the quality factor Q_p at parallel resonance frequency. Since a one-transistor oscillator is operating close to f_s, this topology may not be the best choice.

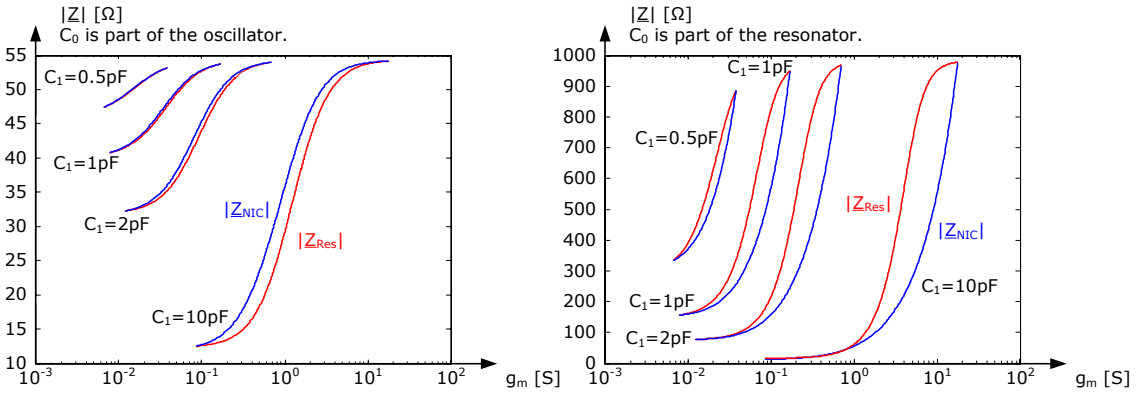


Figure 4.14: Absolute value of the impedances $\underline{Z}_{\mathrm{Res}}$ and $\underline{Z}_{\mathrm{NIC}}$.

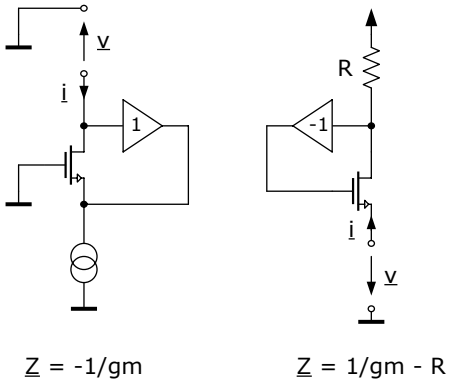


Figure 4.15: Two 2-stage oscillators.

4.3 Two-Stage Oscillators

In Figure 4.15 two basic principles of 2-stage oscillators are shown. In the left circuit the voltage $\underline{v}$ at the port is transferred via a buffer to the source of the transistor. At the source this voltage causes a current $\underline{i} = -\underline{v} \cdot g_{\mathrm{m}}$ flowing from the port through the transistor. Hence the input impedance of this circuit is $\underline{Z} = -\frac{1}{g_{\mathrm{m}}}$. This circuit is stable if the port is shorted or even connected to a load smaller than $|\underline{Z}|$. So this circuit is comparable with the first example shown in Figure 4.2, where the voltage $\underline{v}$ is also the input and the current $\underline{i}$ the output of the NIC. Now it is easy to calculate the minimum transconductance required to allow oscillation. For an impedance of 1 kΩ, which is a typical value for a BAW resonator at parallel resonance, and for 10 Ω, which would be typical for series resonance, the corresponding g_{m} can be found with equation 4.17. Again, oscillation at both extreme values is possible, but the current consumption is at a minimum at parallel resonance.

$$\begin{aligned} R_{\mathrm{load}} = 1\,\mathrm{k\Omega} \quad &\rightarrow \quad g_{\mathrm{m}} > 1\,\mathrm{mS} \\ R_{\mathrm{load}} = 10\,\Omega \quad &\rightarrow \quad g_{\mathrm{m}} > 100\,\mathrm{mS} \end{aligned} \tag{4.17}$$

In contrast, in the right circuit in Figure 4.15 the current causes a voltage drop across the resistor R. This voltage drop is transferred via an inverting buffer to the gate of the transistor. Taking the gate source voltage $\underline{v}_{\mathrm{gs}} = -\frac{\underline{i}}{gm}$ into account, the voltage at the output of the NIC can be calculated to be $\underline{v} = -\underline{i} \cdot R + \frac{\underline{i}}{g_{\mathrm{m}}}$. Now the input impedance can be determined to be $\underline{Z} = \frac{1}{g_{\mathrm{m}}} - R$. In this case, the circuit is stable if the port is open or even connected to a load greater than $|\underline{Z}|$, as illustrated in the bottom example shown in Figure 4.2. Under the assumption that the resistor R is 2 kΩ the minimum required transconductance g_{m} can be calculated (see equation 4.18). For this type of oscillator, the required transconductance and therefore the current consumption is lower when the oscillator is operating near the series resonance frequency.

$$\begin{aligned} R_{\mathrm{load}} = 1\,\mathrm{k\Omega} \quad &\rightarrow \quad g_{\mathrm{m}} > 1\,\mathrm{mS} \\ R_{\mathrm{load}} = 10\,\Omega \quad &\rightarrow \quad g_{\mathrm{m}} > 0.5\,\mathrm{mS} \end{aligned} \tag{4.18}$$

From this point of view, the oscillator itself can be attributed with the terms of series or parallel resonance according to whether the ideal operating point with minimum current consumption is close to the series or close to the parallel resonance of the resonator.

Operating near the series resonance frequency with the 2-stage circuit topology shown in Figure 4.15 on the right can pose some risk, especially at high frequency: A delay in one of the two stages will cause an inductive output behaviour of the NIC. If, for example, a capacitor is connected in parallel to the resistor R, the output impedance can be written as:

$$\underline{Z} = \frac{\underline{v}}{\underline{i}} = \frac{1}{g_{\mathrm{m}}} - \frac{R}{1 + \mathrm{j}\omega RC} = \frac{1}{g_{\mathrm{m}}} - \frac{R}{1 + \omega^2 R^2 C^2} + \mathrm{j}\frac{\omega RC}{1 + \omega^2 R^2 C^2} \tag{4.19}$$

A related effect is the inductive peaking known in source followers if the gate connection exhibits some resistivity. Then a capacitive behaviour at the port, which can be caused, for example, by the ESD protection circuit or by the bulk capacitance of the resonator, can result in a parasitic oscillation. A possible implementation consisting of only one transistor is shown in Figure 4.16. Instead of two capacitors, as shown in the previous one-transistor oscillator circuits, a transformer is used to create feedback. Even without the coupling between the inductors it would be possible to generate a negative resistance. Because of the risk of parasitic oscillation, the chosen topology for the oscillator in the transmitter is a circuit which operates close to the parallel resonance frequency.

In [57] based on [58, 59] a classification of single-pin crystal oscillators is given. As already mentioned, it is common to operate crystal oscillators close to their series resonance frequency. Hence the current is sensed and amplified and a voltage is forced to the resonator to realize the required open-stable negative resistance [57] as shown in Figure 4.2. A single-pin configuration is also advantageous for the BAW-oscillator

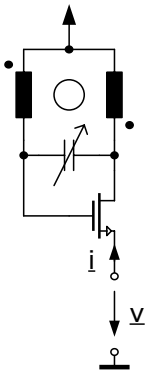


Figure 4.16: One-transistor oscillator using a transformer.

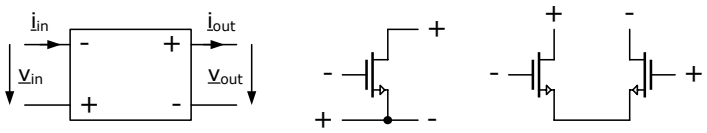


Figure 4.17: The nullor symbol and its simplest approximations.

since it allows easy DC-tuning and it also avoids problems arising from the unequal parasitic capacitances of the electrodes. Normally the bottom electrodes of SMRs have a higher capacitance against substrate due to their proximity. In the following chapter, all possible configurations of single-pin oscillators presented in [57] have been expanded with short-stable oscillators. These types of oscillators are commonly not used for crystal oscillators.

The main idea of [57] is to use an amplifier with infinite gain in a feedback configuration so that the behaviour is mainly affected by the feedback components. The ideal high-gain amplifier is modelled with a nullor. The symbol of the nullor and its simplest approximations are shown in Figure 4.17. The transfer characteristic of an amplifier is described with ABCD-parameters given in equation 4.20.

$$\begin{pmatrix} \underline{v}_{\mathrm{in}} \\ \underline{i}_{\mathrm{in}} \end{pmatrix} = \underline{\mathbf{A}} \begin{pmatrix} \underline{v}_{\mathrm{out}} \\ \underline{i}_{\mathrm{out}} \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} \underline{v}_{\mathrm{out}} \\ \underline{i}_{\mathrm{out}} \end{pmatrix} \tag{4.20}$$

The input impedance ($\underline{Z}_{\mathrm{in}}$) and the output impedance ($\underline{Z}_{\mathrm{out}}$) can be determined with the help of the transmission parameters and with the help of the source impedance ($\underline{Z}_{\mathrm{source}}$) and load impedance ($\underline{Z}_{\mathrm{load}}$), respectively:

$$\underline{Z}_{\mathrm{in}} = \frac{A\underline{Z}_{\mathrm{load}} + B}{C\underline{Z}_{\mathrm{load}} + D} \quad \text{and} \quad \underline{Z}_{\mathrm{out}} = \frac{B + D\underline{Z}_{\mathrm{source}}}{A + C\underline{Z}_{\mathrm{source}}} \tag{4.21}$$

The four ABCD-parameters of the nullor without feedback are zero, since the input voltage and input current are zero. A feedback loop can be used to force these parameters to a certain value. There exist four different kinds of feedback: a volt-

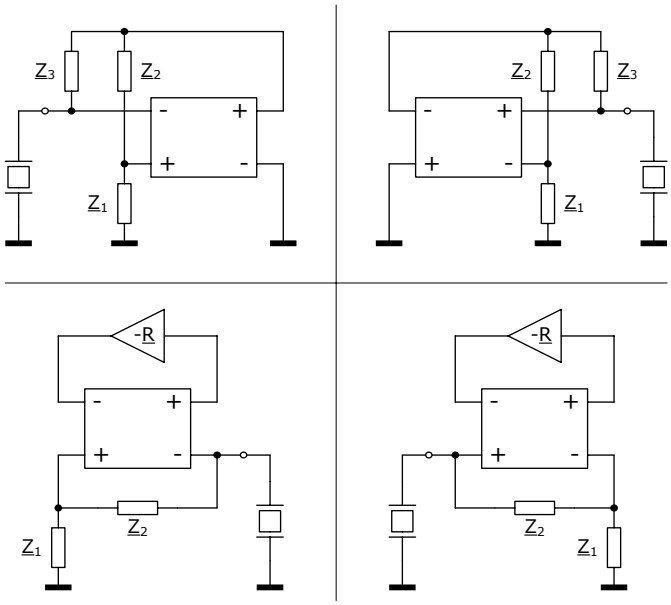


Figure 4.18: Basic configurations of open-stable single-pin oscillators [57].

age-to-voltage, a current-to-voltage, a voltage-to-currrent, and a current-to-current feedback. If one feedback is implemented, one of the four transmission parameters can be set to the required value. For example, if a part of the output voltage is sensed and fed back to the input (voltage-to-voltage feedback), the voltage gain ($1/A$) is determined by the feedback elements. But the input impedance is still infinite and the output impedance is still zero. Each feedback loop essentially sets only one transfer parameter [58]. From equation 4.21 it can be seen that at least two parameters have to be different from zero to generate a negative input or a negative output resistance. Hence two feedback loops have to be applied to accomplish oscillation. Selecting two feedbacks out of four possible feedback structures results in six possible combinations. But only four out of these six combinations create a negative impedance which does not depend on the load or source impedance. For example, if A and C are not equal to zero and B and D are zero, the input impedance $\underline{Z}_{\mathrm{in}}$ depends directly on the load impedance $\underline{Z}_{\mathrm{load}}$. The remaining four different circuits applying dual loop feedbacks are shown in Figure 4.18. In these configurations the positive feedback is implemented to realize an open-stable negative resistance [57].

The negative feedback of the circuits depicted in Figure 4.18 is at its maximum if the port is open and therefore they are called open-stable. In Figure 4.19 the polarity of the inputs of the nullor are interchanged. Thus the positive feedback is prevented if the port is shorted and thus these configurations are stable if the port is shorted, as opposed to the open-stable oscillators shown in Figure 4.18.

The simplest open-stable configuration can be derived from the two possibilities shown an the bottom of Figure 4.18 [57]: The result of making the impedance $\underline{Z}_1$ infinite and impedance $\underline{Z}_2$ zero is depicted in Figure 4.20. It is important to bear in

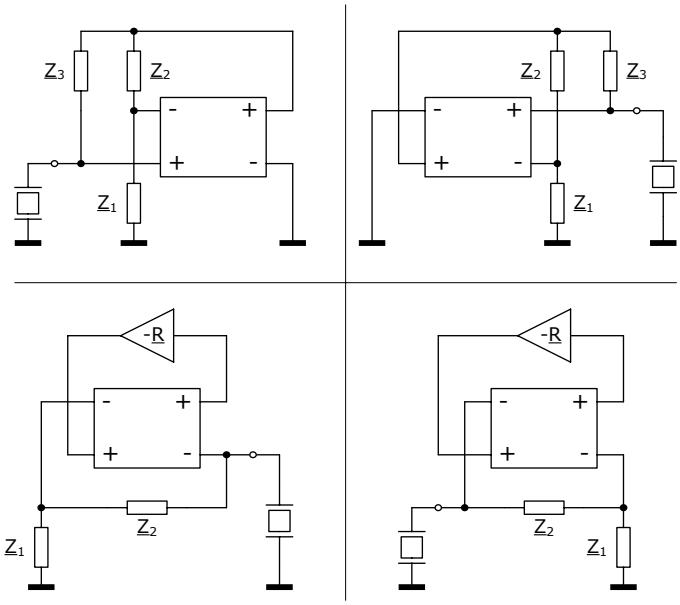


Figure 4.19: Basic configurations of short-stable single-pin oscillators.

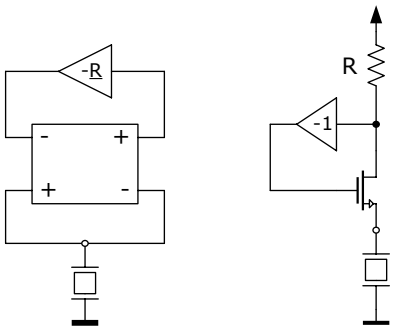


Figure 4.20: Simple open-stable single-pin configuration [57].

mind that the approximation of this configuration is identical to the basic open-stable circuit shown in Figure 4.15. If g_{m} is high enough, the negative resistance equals $-1/R$. Hence the oscillator only relies on the feedback element. As opposed to this, the negative resistance of the basic short-stable circuit is a function of g_{m}. The idea of using a high-gain amplifier was that the negative impedance is only affected by the feedback components. Unfortunately, the use of a high-gain amplifier results in a complex short-stable configuration. It is important to note that both the basic short--stable NIC type shown in Figure 4.2 and the basic short-stable circuit in Figure 4.15 rely on a finite gain and therefore the nullor approach cannot be applied. The simplest short-stable circuit where the negative resistance is only affected by feedback elements is illustrated in Figure 4.21.

The topology used in the proposed transmitter is derived from the circuit illustrated in Figure 4.22. This topology cannot be derived from the basic inventory based on

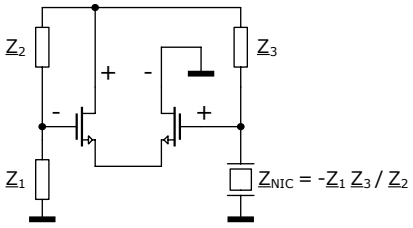


Figure 4.21: Simple short-stable single-pin configuration.

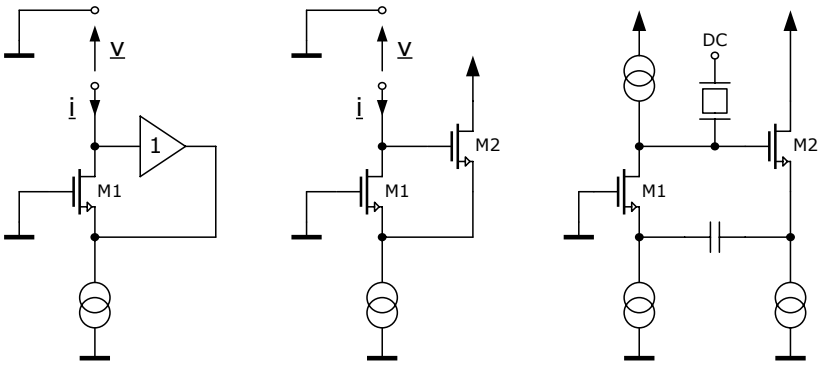


Figure 4.22: Further development of the 2-stage oscillator.

the nullor approach. But this circuit also has dual loop feedback. The buffer can be replaced by a source follower (see circuit in the middle of Figure 4.22). Unfortunately, the BAW resonator does not provide a DC path as, for example, an LC tank. Using a current source allowing a DC current to flow results in a high DC gain and hence the oscillator would latch. A solution to this problem is shown in the right circuit in Figure 4.22. A DC decoupling capacitor opens the feedback loop for DC and prevents the latch-up. Additionally, one of the two current sources in the same branch has to be controlled to have a defined operating point.

An advantage of this single-ended circuit is that one terminal of the resonator is connected to ground. This terminal can be used to apply a DC voltage for tuning the resonance frequency in a small range. As already mentioned, one terminal of the used BAW resonator has a higher capacitance against substrate. This also has no impact in single-ended operational mode. Connecting the gate of transistor M1 to the source of transistor M2 would bring additional gain. This leads to a combination of a differential gain stage and a phase shift, which is caused by the capacitor (see Figure 4.23). The combination is shown in Figure 4.24. The proposed topology is quite similar to the differential oscillator circuit proposed in [91]. Assuming the sources of transistors M1 and M2 in Figure 4.24 are connected to ground, the signal on node A amplified by M1 results in a 180° shifted signal on node B. To avoid any additional phase shift, node B should not be capacitively loaded and hence a simple resistor is used as load element. The capacitive load of node A is not so critical because it only causes a shift in the BAW resonance frequency and degrades the impedance as already discussed.

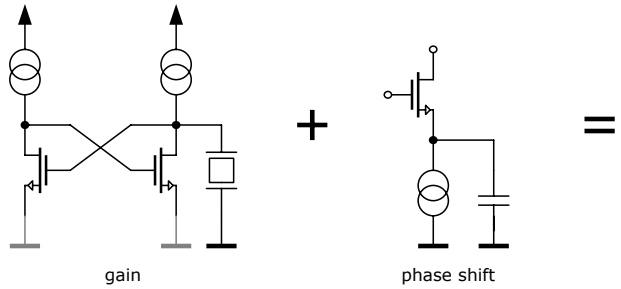


Figure 4.23: Combining a differential gain stage and phase shift.

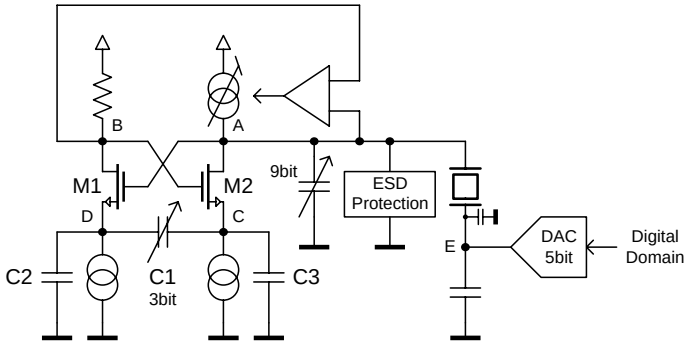


Figure 4.24: Basic principle of the BAW oscillator.

So as not to damp the high Q resonance circuit, the resonator should be connected to a high impedance node. Therefore instead of a resistor a current source is used as load element of transistor M2. With the sources of M1 and M2 connected to ground, the circuit obviously would not oscillate but latch and nodes A and B would saturate [86]. Therefore, the combination of C1, C2, and C3 together with two further current sources was introduced for DC decoupling. With C1 the phase shift can be trimmed, which can also be used for tuning the frequency in a very small range (3bit).

4.4 BAW Oscillator Implementation

The high gain of the oscillator core shown in Figure 4.24 could cause stability problems in the control loop of the current source operating as load of transistor M2. In order to maintain stability more easily, a replica circuit without the cross coupling of transistors M1 and M2 is applied (see Figure 4.25). The proposed oscillator is tunable over a frequency range of about 10 MHz to enable temperature compensation, process compensation, and modulation. To overcome temperature drift effects of the resonance frequency (typ. -18 ppm/°C, [64]) in the range of -40°C through 125°C, the temperature is measured and compensated by means of digitally controlled capacitors in parallel to the resonator. In addition to the capacitor bank, the BAW can be tuned with a variable DC biasing. Biasing the resonator causes a change in the stiff-

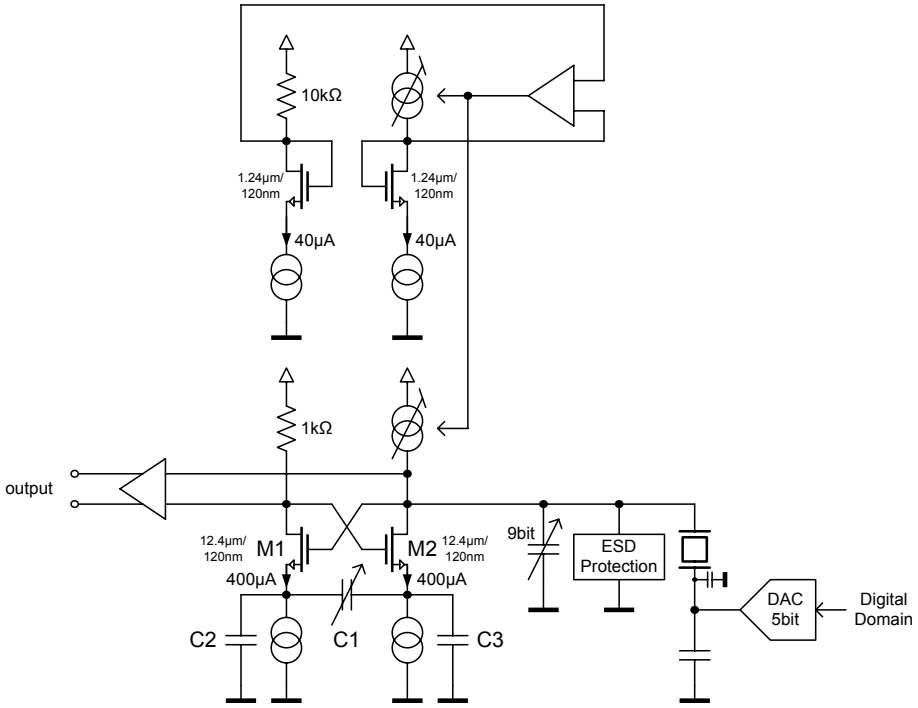


Figure 4.25: BAW oscillator with biasing network.

ness of the piezoelectric BAW-material and hence the resonance frequency is slightly shifted. More details on tuning can be found in chapter 4.5 on page 81.

A critical design issue is the fact that the impedance of the resonator is relatively low, even at the parallel resonance frequency. Without any tuning capacitors in parallel the impedance is in the range of 2 kΩ but with all tuning capacitors in parallel the impedance may drop to even below 500 Ω. To guarantee proper start-up of oscillation the transconductance of the oscillator core must be sufficiently high. In addition to the tuning capacitors, the ESD protection circuit significantly contributes to the capacitive load. The ESD protection was designed to withstand 500 V (based on the human body model - HBM) during bonding. To avoid any deviation from the desired frequency, the phase shift of the oscillator core has to be very low while keeping the gain high. In the proposed design a two-stage oscillator core is used to meet these requirements.

The poles of the oscillator can be calculated by using a first order equivalent circuit. The root locus plot is shown in Figure 4.26. If the transconductance g_m of the transistors is higher than a certain minimum, only two poles are on the right side of the plane and the oscillator will start to oscillate. As one can see from Figure 4.26 two further poles are present. As long as the transconductance g_m does not exceed a certain limit, they stay in the left plane and therefore they have no impact on the steady state solution. But if the transconductance g_m becomes higher, the two complex conjugate poles can reach the right plane and cause a parasitic oscillation. A

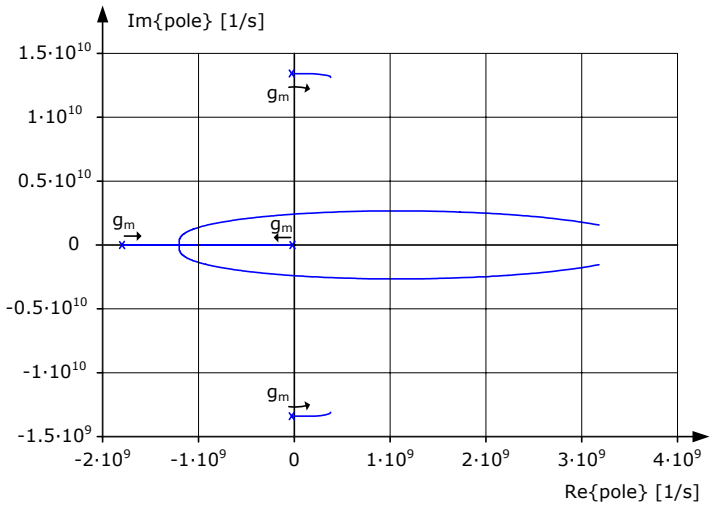


Figure 4.26: Root locus plot of the proposed BAW oscillator.

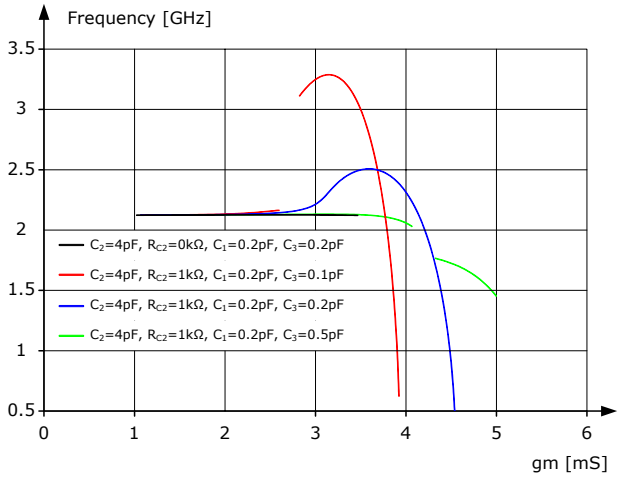


Figure 4.27: Oscillation frequency of the BAW oscillator versus g_m.

more detailed view on these issues is provided by Figure 4.27. In this plot we can see the frequency of oscillation, determined by the imaginary part of the instable, complex conjugate pole pair. In Figure 4.27 only points are plotted if exactly one pole pair is on the right side of the complex plain. If there is no point for a certain value of g_m, the oscillator does not oscillate or a parasitic oscillation interferes. In this way it is possible to find a combination of the passive components of the oscillator, where variations of g_m are acceptable.

The measured phase noise of the carrier at the output of the transmitter is shown in Figure 4.28. Because of the high quality factor of the resonator used, these values are quite good compared to VCOs using on-chip inductors. This comparison is however unfair because in a PLL based transmitter many building blocks have an impact on the phase noise at the output of the transmitter. The comparison between the phase

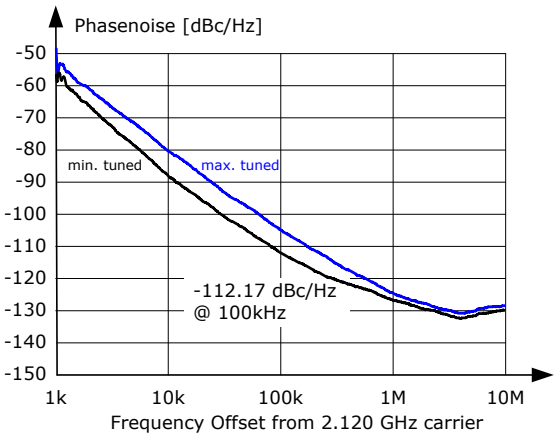


Figure 4.28: Phase noise of the oscillator measured with minimum and maximal capacitor tuning setting.

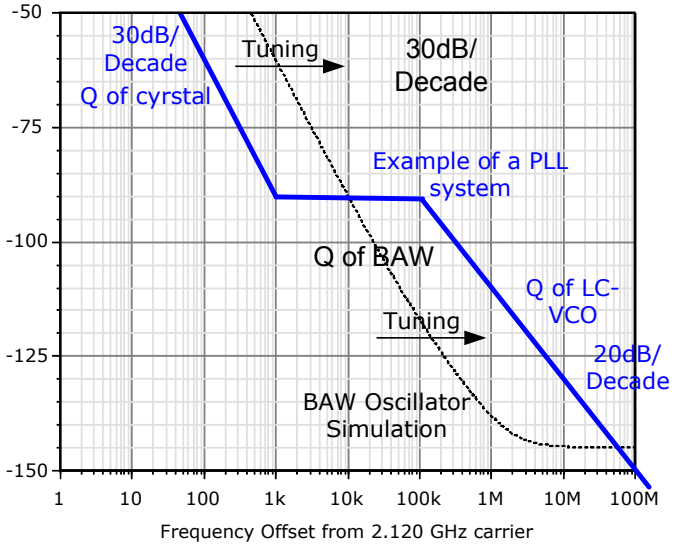


Figure 4.29: Comparison phase noise of the BAW oscillator and phase noise of a typical PLL system.

noise of a typical PLL system and the BAW oscillator is depicted in Figure 4.29. For low frequencies the control loop of the PLL works and the properties of the reference frequency are transformed to RF. Hence in this region the PLL has a better phase noise performance due to the high Q-factor of the quartz crystal used in the reference oscillator. On the other hand, the phase noise at high frequencies can be affected by the VCO. In this region the BAW based transmitter shows a better performance.

The start-up time was measured by means of directly connecting a 20 GSa/s oscilloscope to the 50 Ω RF output. The transient plot of the ASK modulated carrier is depicted in Figure 4.30. In ASK the power amplifier is turned on and off. Optionally the transmitter architecture (see Figure 2.16 on page 47) allows the turning-off of the

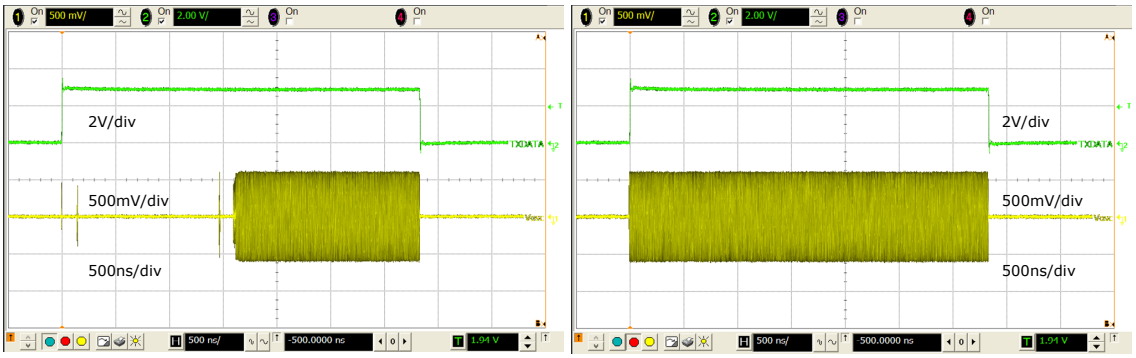


Figure 4.30: Directly measured antenna output with an 20 GSa/s oscilloscope (left: ASK using the BAW-oscillator; right: ASK using the PA).

BAW oscillator and single to differential conversion block during ASK 0. This reduces the power consumption dramatically, since the current consumption is almost zero for half of the time. But in this mode the data rate is limited due to the start-up time of the oscillator. This mode can also be used for measuring the start-up time, which is lower than 2 µs, as can be read from the left plot of Figure 4.30.

4.5 BAW Tuning (Temperature Compensation and Modulation)

Besides the properties given in chapter 3 (f_s, f_p, Q_s, Q_p, Z, Z_min, Z_max, C_0, BW_BAW, and k^2_eff) process tolerances and temperature drift of the BAW resonance frequency are very important characteristics. A state-of-the-art BAW device without any countermeasures against temperature drift exhibits a drift of the resonance frequency of about -18 ppm/°C [64]. A common approach to reduce the temperature drift effects is the integration of an additional SiO_2 layer into the acoustic stack of the BAW and hence making use of the unique property of SiO_2 in that it gets harder with temperature. Or, in other words, the stiffness of SiO_2 has a positive temperature coefficient and this can be used to compensate the temperature coefficient of AlN. A new BAW device for the transceiver utilizing a temperature compensation based on an additional SiO_2 layer was developed by e-Cubes project partners [71, 72]. The proposed temperature drift is 35 ppm over a temperature range of 0°C to 100°C [71, 72]. Without any compensation, the variation is about 3000ppm in the range of -40°C through 125°C, which corresponds to 6.3 MHz.

Another issue is the frequency accuracy. To get an accurate resonance frequency of the BAW device, a uniform deposition of thin-films is mandatory. The best thin-film deposition system in the semiconductor industry cannot provide better than 2% (=20,000 ppm!, 3σ-value) uniformity across the wafer [68]. This would result in a variation of about 42 MHz for a 2.1 GHz resonator. Because of this, the vendors introduced a trimming process [68] using a tuning layer (see Figure 3.2 on page 54). The tuning layer is locally milled by a narrow ionized particle beam. The required

thickness of milling is determined by single test structures, which are distributed on the wafer. The achievable frequency accuracy after trimming is less than 0.05% = 500 ppm [65]. Hence the remaining process variation can be about 1 MHz. The variation of the used resonators is slightly higher (2 MHz). This is still too inaccurate for many applications and hence an additional electrical calibration step is introduced.

Another source for a frequency shift is the oscillator itself, its ESD protection circuit, and the tuning capacitor bank. Due to the variations of the on-chip circuitry, the variation of the impedance ($\underline{Z}_{\mathrm{NIC}}$) will cause a shift in the resonance frequency. The task of the implemented calibration unit is to compensate all sources of drifts and process variations. Since a compensation algorithm has to be implemented to overcome process variations the absolute value of the temperature drift is not so important as long as the drift can be reliably expressed by an equation. But a mechanical temperature compensation could simplify the calibration itself: for example, only one process calibration step at one temperature is needed.

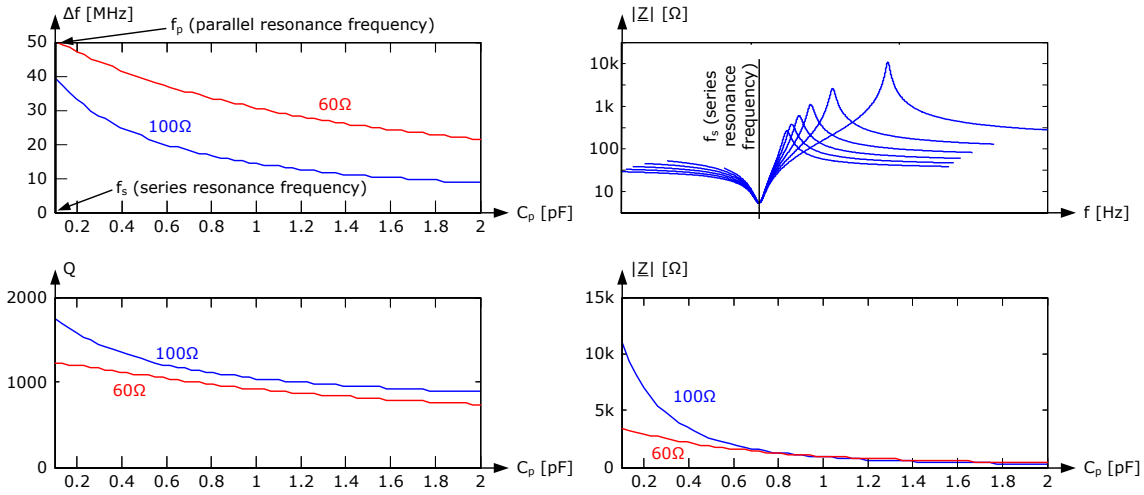


Figure 4.31: Simulated frequency shift, quality factor (Q_{p}), and absolute value of the impedance versus tuning capacitance C_{p} in parallel to the BAW resonator.

4.5.1 Capacitive Tuning

Both the RX and TX oscillators, which are shown in Figure 2.16 on page 47, are tunable over a frequency range of about 10 MHz to enable temperature compensation and process compensation. The tuning is achieved by connecting digitally controlled capacitors C_{p} in parallel to the BAW resonator. Using the equivalent circuit of the BAW (Figure 3.3 on page 55) the parallel resonance frequency f_{p} can be calculated to [42]:

$$f_{\mathrm{p}} = \frac{1}{2\pi\sqrt{L_{\mathrm{a}}C_{\mathrm{a}}}} \cdot \sqrt{1 + \frac{C_{\mathrm{a}}}{C_0 + C_{\mathrm{p}}}} \tag{4.22}$$

Tuning with digitally controlled tuning capacitors can also be used for modulation of the TX oscillator. But in this case the nonlinear and process dependent relationship between capacitance and resonance frequency has to be taken into account. The simulated frequency shift using the modified Butterworth-Van Dyke model for two different types of BAW resonators is shown in Figure 4.31. The deviation Δf from the series resonance frequency f_s is given for a $Z_{C_0} = 60\,\Omega$ and for a $Z_{C_0} = 100\,\Omega$ resonator. Z_{C_0} is the absolute value of the impedance of C_0 at $(f_\mathrm{p} + f_\mathrm{s})/2$.

Looking at the equivalent circuit (Figure 3.3 on page 55) the capacitors C_0 can be thought to be in series with C_a and L_a. Hence the effective capacitance C is reduced and the parallel resonance frequency is always slightly higher than the series resonance frequency. This can be expressed with the relative bandwidth of the resonator $BW_\mathrm{BAW} = (f_\mathrm{p} - f_\mathrm{s})/f_\mathrm{p}$. The relative bandwidth is directly connected to the effective piezoelectric coupling factor, which was already introduced in chapter 3.

$$k^2_\mathrm{eff} = \frac{\pi^2}{4}\frac{f_\mathrm{s}}{f_\mathrm{p}}\frac{f_\mathrm{p} - f_\mathrm{s}}{f_\mathrm{p}} \approx 2.4 \cdot BW_\mathrm{BAW} \tag{4.23}$$

With a good material with a high coupling factor the $L_\mathrm{a}C_\mathrm{a}$ tank, which represents the mechanical oscillator, can be implemented with a small area and therefore with a small bulk capacitance C_0. If the bulk capacitance is small, the parallel resonance frequency is large and so the resonator exhibits a high relative bandwidth BW_BAW. As a result, the coupling factor is directly proportional to the relative bandwidth.

By applying a capacitor in parallel to the resonator, the parallel resonance frequency is shifted towards the lower series resonance frequency, which is the theoretical limit of tuning. The series resonance frequency can be shifted to a lower value by connecting an inductor in series to the resonator. This is a side effect of the bonding wire used in the prototype, where the chip dies are directly bonded onto a PCB (in the 3D stack the inductance of the stud bumps is negligible). The quality factor of a series and a parallel LC tank is given by [36]:

$$Q_\mathrm{s} = \frac{\sqrt{\frac{L}{C}}}{R_s} \qquad Q_\mathrm{p} = \frac{R_p}{\sqrt{\frac{L}{C}}} \tag{4.24}$$

From equation 4.24 one might suspect that even an ideal capacitor or inductor connected to the resonator could have an impact on the quality factor. If the resonator is operating at its parallel resonance frequency, then L_a and C_a work together as an inductance, and this inductance is in resonance with the sum of the capacitances C_0 and C_p. If C_p is large, this inductance has to be small. This small inductance in combination with the resistance R_a results in a reduction of the quality factor. Subsequently tuning causes a reduction of the quality factor. The simulated quality factor against the tuning capacitance C_p and the impedance of the resonator are illustrated in Figure 4.31.

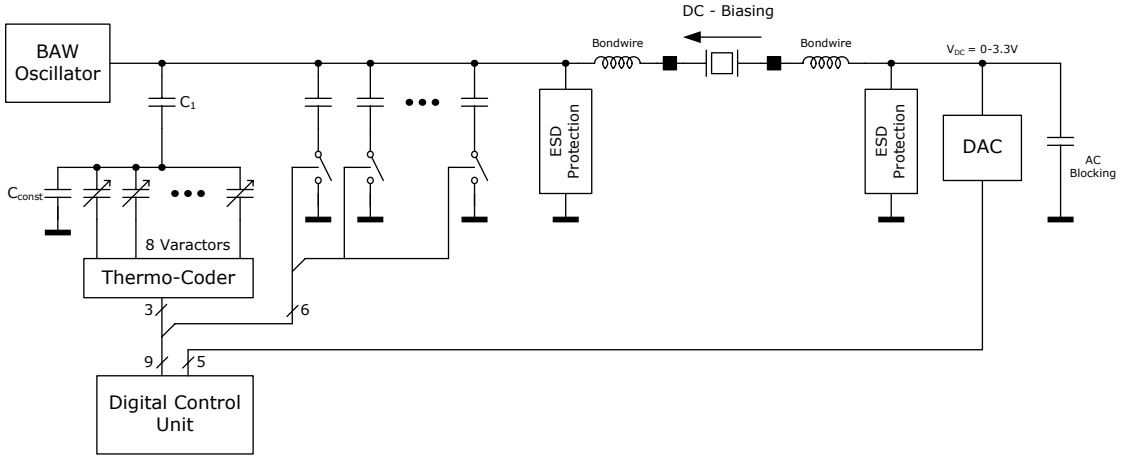


Figure 4.32: Basic principle of the tuning unit.

It is important to note that the insertion of an additional layer into the resonator stack for temperature compensation purposes results in a reduction of the effective coupling factor. Thus the relative bandwidth and the quality factor are decreased, which are the same consequences as tuning causes. Indeed the insertion of a layer between two electrodes is very similar to connecting a capacitor (which is also a material between two electrodes) to the resonator.

The implementation of the tuning unit is shown in Figure 4.32. To allow tuning of about 10 MHz the capacitance has to be about 1 pF whereas the constant value, which is always connected, should be as low as possible. The 3σ-value of the variation of the capacitance ΔC due to local mismatch can be calculated using the constant A_C in $[\%\mu\mathrm{m}]$. The capacitance C is proportional to the area A and to the process constant C_A in $[\mathrm{fF}/\mu\mathrm{m}^2]$. From this it follows:

$$\Delta C = \frac{\mathrm{A}_C}{\sqrt{A}} C, \quad C = \mathrm{C}_A A \quad \rightarrow \quad \Delta C = \mathrm{A}_C \sqrt{C \mathrm{C}_A} \tag{4.25}$$

A binary weighted capacitor bank is limited in its resolution because of this mismatch. Therefore the smallest step in the bank C_{LSB} has to be larger than the variation ΔC. The worst case ΔC is caused by the largest capacitor $C_{\max}/2$ in the bank. The maximum value, when all capacitors are turned on, is limited in this application. Thus the number of achievable bits N can be determined with:

$$C_{\mathrm{LSB}} = \frac{C_{\max}}{2^N} \gg \Delta C = \mathrm{A}_C \sqrt{\frac{C_{\max}}{2} \mathrm{C}_A} \quad \rightarrow \quad N \ll \mathrm{ld}(\sqrt{2 \frac{C_{\max}}{\mathrm{C}_A}} \frac{1}{\mathrm{A}_C}) \tag{4.26}$$

Another limiting factor are the parasitics of the capacitors, of the wiring, and of the switches. Especially the small capacitors in the bank, which are in the range of femto Farad, cannot be easily implemented. Because of this, a capacitor C_1 is connected in series to eight varactors. A thermocoder controls the varactors in such a way that

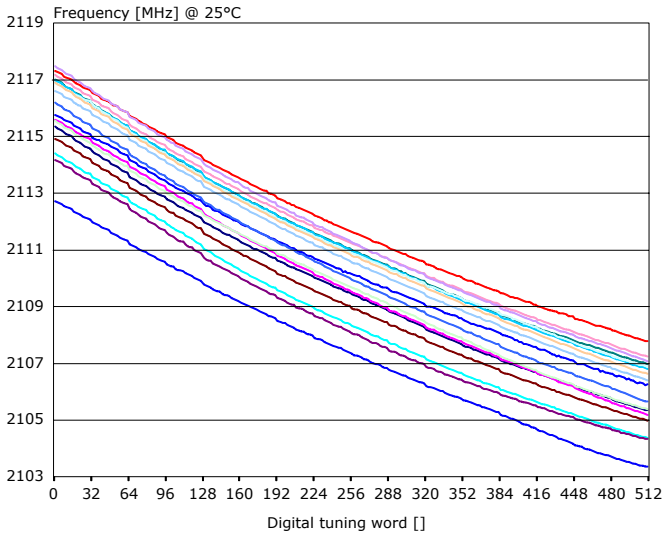


Figure 4.33: Measured frequency shift due to tuning by means of digitally controlled capacitors (9bit) at room temperature (25°C).

monotonicity can be guaranteed. The purpose of the capacitor C_1 and the capacitor C_{const} in parallel to the varactors (see Figure 4.32) is to transform the capacitance of the varactors to lower values, so that the implementation is simpler and more accurate. The transformation is performed in equation 4.27. If C_x, which represents the capacitance when all varactors are turned on, is much lower than $(C_1 + C_{\text{const}})$ the transformation is linear.

$$
\begin{aligned}
&C = \frac{1}{\frac{1}{C_1} + \frac{1}{C_x + C_{\text{const}}}} = C_0 + k \cdot C_x \quad \text{with} \\
&C_0 = \frac{C_1 C_{\text{const}}}{C_1 + C_{\text{const}}}, \quad k = \frac{C_1^2}{(C_x + C_1 + C_{\text{const}})(C_1 + C_{\text{const}})} \\
&\text{if } C_x \ll C_1 + C_{\text{const}} \quad \text{then} \quad k \approx \frac{C_1^2}{(C_1 + C_{\text{const}})^2}
\end{aligned}
\tag{4.27}
$$

The measured frequency of the oscillator versus different digital settings of the digitally controlled capacitors is shown in Figure 4.33 for several samples. The same plot is also given in Figure 4.34 for three different temperatures: -40°C, 27°C, and 125°C. From this plot it can be seen that the adjustable frequency window is quite narrow. If the selected tuning word is set to zero, all samples should oscillate at a higher frequency than the target frequency. And if the maximum tuning word is selected all samples should oscillate at a lower frequency. If a sample exhibits a higher frequency than the target frequency at -40°C with maximum tuning word, or if a sample exhibits a lower frequency at 125°C although the tuning word is set to zero, the resonator cannot be used. Depending on the temperature range, process variations, and temperature drift, a yield loss of the BAW resonators has to be taken into account. To maximize the yield the target frequency was set to 2109.3 MHz. To

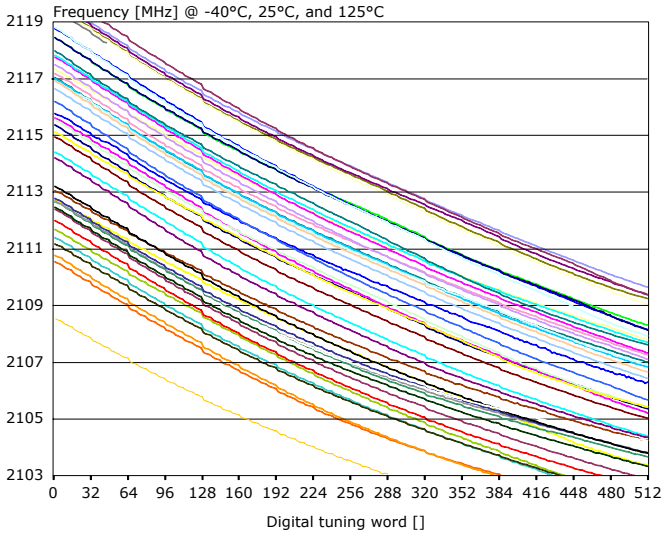


Figure 4.34: Measured frequency shift due to tuning by means of digitally controlled capacitors (9bit) at three different temperatures (-40°C, 25°C, and 125°C).

increase the yield the following measures can be considered:

- The tuning range can be increased by increasing the capacitor bank. But a larger capacitor bank causes a larger fixed capacitance, which is always connected. This capacitance consumes some of the possible tuning range BW_{BAW} and also makes the resonator more insensitive to the capacitance switched by the capacitor bank. And so the curves in Figure 4.31 become flatter for high values of C_{p}. Additionally, the impedance at parallel resonance becomes smaller and therefore the oscillator needs more current to guarantee a proper start-up. And, last but not least, the quality factor is reduced and this results in a worse phase noise performance.

- The fixed capacitance can be minimized by optimizing the wiring, the ESD protection circuit, the capacitor bank, interconnection and all other circuitry connected to the resonator. Alternatively, a portion of the fixed capacitance can be compensated by an inductor. This inductor can be implemented as a passive component or can be introduced by the oscillator making its output inductive due to the implemented phase shift.

- The yield can also be increased by using a different BAW resonator with less process variation and/or temperature drift. Resonators with less process variation are available: An example with a process variation of about 500 ppm is reported in [65]. A resonator with integrated temperature compensation eliminates the need for calibration at different temperatures and therefore complexity is reduced. But calibration might be needed for some applications due to the remaining process variation (also caused by the circuitry). But as already mentioned,

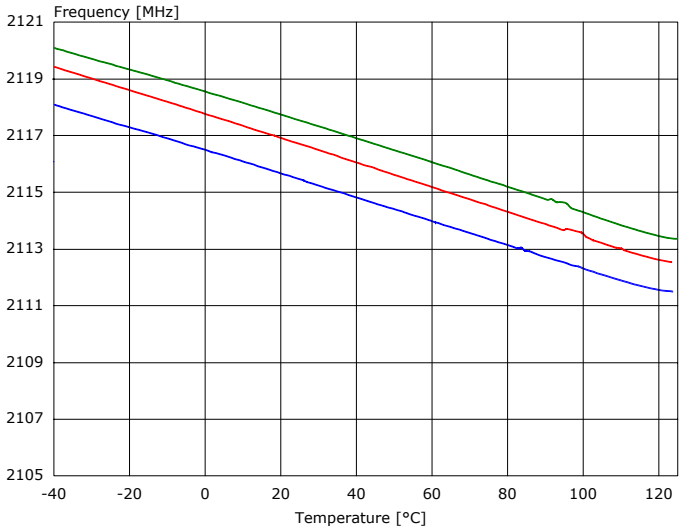


Figure 4.35: Measured frequency versus temperature for a fixed tuning word.

the tuning range is also reduced if a mechanical temperature compensation is integrated into the resonator due to the decreased coupling factor k_{eff}^2.

- As illustrated in chapter 1 (page 17) 3D integration technology can be advantageous compared to a system-on-chip (SoC): The very small resonator itself can be measured and if its specification is not satisfied, only a small fraction of area on the resonator wafer is lost and not a whole transceiver die.

- The IF bandwidth determines how much frequency variation of the transmit frequency and of the LO at the receiver is tolerable. A smaller transmit frequency reduces the absolute value of the tolerances and hence it is easier to implement. A smaller frequency can be obtained by using a resonator with a smaller resonance frequency, or alternatively by dividing the output of the oscillator. Another benefit of this approach is the prevention of oscillator pulling and it might be helpful for generating a signal with a certain duty cycle. This duty cycle is required to increase the efficiency of the power amplifier (see chapter 6.2 on page 122).

In Figure 4.35 the frequency drift for a fixed tuning word for three different samples is shown. It can be seen that the drift is quite linear but a closer look shows that the BAW resonator is also affected by higher order drift effects.

The transmitter is equipped with a temperature sensor which is connected to a 10bit ADC. The ADC is also used to convert the received signal strength indicator (RSSI) signal provided by the limiter (see transceiver block diagram shown in Figure 2.16 on page 47). A voltage proportional to the absolute temperature (PTAT) is generated by a bandgap reference, where two bipolar transistors are biased by two different current densities with a ratio of n. Hence the voltage difference between these two

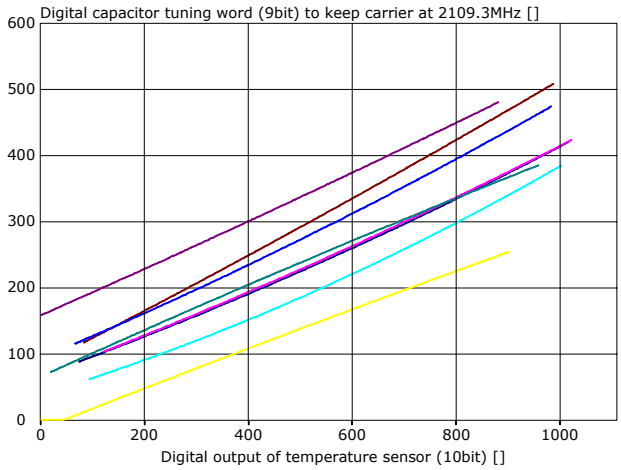


Figure 4.36: Plot of digital capacitor tuning word, which is required to keep carrier at 2109.3 MHz, against digital output of the temperature sensor (different samples).

devices is proportional to $\mathrm{kq}/T \cdot \ln(n)$. Also the reference voltages for the ADC are gained from the bandgap voltage provided by the bandgap reference. Figure 4.36 shows the capacitor tuning word, which has to be programmed to shift the oscillator to the desired frequency of 2109.3 MHz, versus the digital output of the temperature sensor. As long as the relationship of the tuning word and the digital output of the temperature sensor can be reliably expressed by an equation, the microcontroller can initialize a temperature measurement and can afterwards set the tuning word accordingly. If no second order effects are present, the relation in Figure 4.36 would show the $1/\sqrt{LC}$ behaviour of equation 4.22, which can be fitted by a second order polynomial in a precise way. Additionally, some second order drift effects are overlying, but they are considered by the second order polynomial. The second order polynomial used for approximation is given by:

$$tuning\_word = a_2 \cdot (dig\_temp)^2 + a_1 \cdot dig\_temp + a_0 \tag{4.28}$$

The constant term (a_0) of the polynomial is basically determined by the process variation of the resonator, by the process variation of the fixed capacitance connected to the resonator and by the absolute inaccuracy of the temperature sensor. The linear term (a_1) is affected by the capacitor tuning bank and by the slope of the temperature sensor characteristic. The quadratic term (a_2) is required because of the nonlinear tuning behaviour ($1/\sqrt{LC}$) and second order drift effects.

The three coefficients of equation 4.28 have to be found for each sample in a separate calibration step. Therefore three different tuning words have to be found at three different temperatures by applying a successive approximation algorithm. By means of consecutively setting the individual bits of the tuning word, the measured carrier frequency is aligned with the target frequency. This has to be done for the

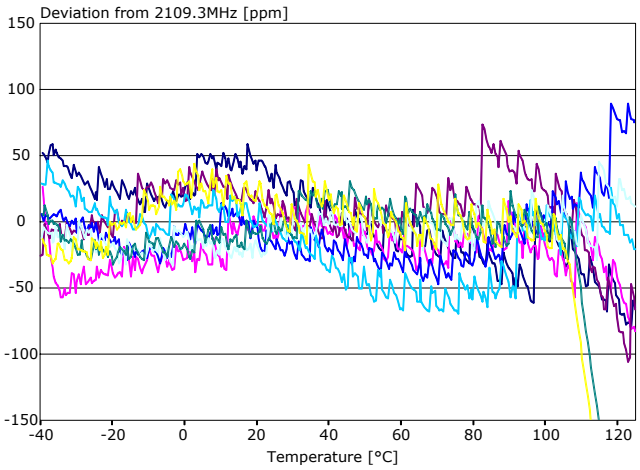


Figure 4.37: Deviation of the carrier from 2109.3 MHz after applying the temperature compensation algorithm (different samples).

BAW oscillator supplying the receiver front end and for the second oscillator supplying the transmitter respectively. The carrier can be measured at the antenna or for the receiver at the intermediate frequency (IF) output, or alternatively the divided clock signal can be measured at the test pin. It is important to note that the three calibration steps can be carried out at three arbitrary temperatures, and knowledge of the absolute value of the temperature is not a precondition for the calibration. If the correct tuning word and the corresponding digital output of the temperature sensor are found and stored, one point of the curve shown in Figure 4.36 is found. With three points, the calculation of the coefficients a_0, a_1, and a_3 is straightforward. Hence the temperature sensor and the oscillator are considered as one unit and they are calibrated together in the same step. But placement of the temperature sensor close to the BAW resonator is mandatory for an accurate function of the calibration. If additionally the absolute value of the temperature is monitored, the temperature sensor can also be used for temperature measurement.

The remaining frequency deviation after applying the temperature compensation algorithm is given in Figure 4.37. The considerable deviation of two samples at high temperature can be explained by a saturation effect of the temperature sensor, which is an impairment of the current sensor implementation. The response of the temperature sensor can be found in Figure 4.38, where the saturation for these two samples can be seen. Despite all these measures, the typical accuracy of a quartz crystal, which is in the range of 5 to 50 ppm [44], cannot be achieved.

The remaining frequency deviation for a single sample is illustrated in Figure 4.39. For one curve the temperature is increased starting from -40°C, whereas for another curve the temperature is decreased starting from 125°C, and a third curve is generated by a fast temperature change. Hence the temperature depicted on the x-axis can differ from the real temperature of the resonator.

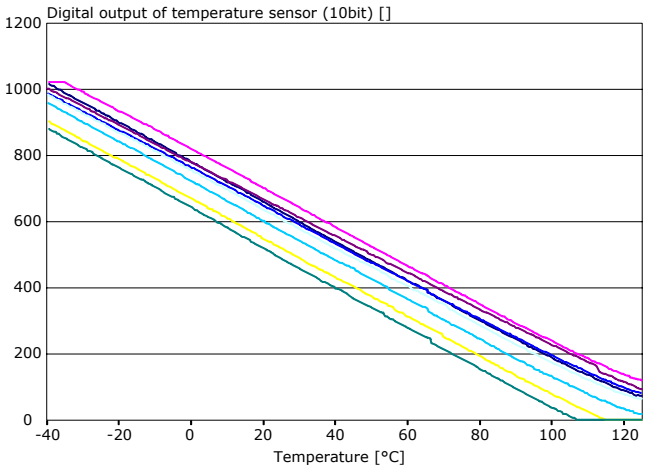


Figure 4.38: Output of the 10bit temperature sensor.

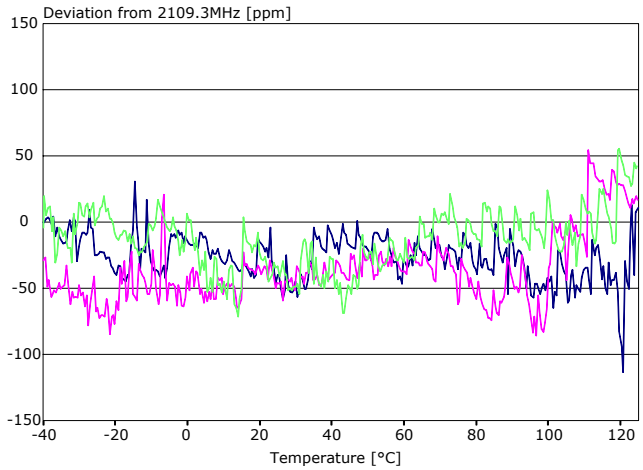


Figure 4.39: Deviation of the carrier from 2109.3 MHz after applying the temperature compensation algorithm (same sample).

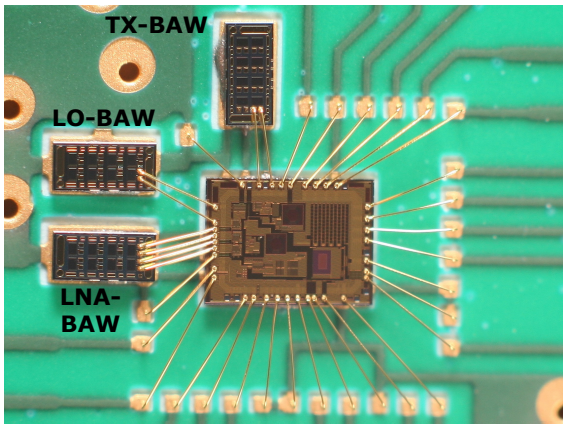


Figure 4.40: First prototype (not stacked) of the transceiver directly bonded onto a PCB.

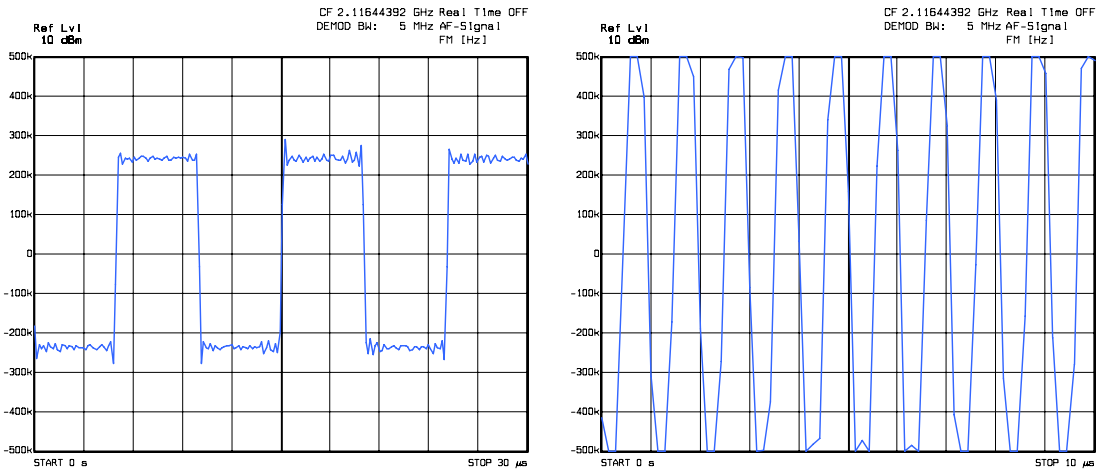


Figure 4.41: Demodulated output signal of the transmitter (left: 100 kbit/s, deviation 250 kHz; right: 2 Mbit/s, deviation 500 kHz) using a spectrum analyzer.

The shown measurements were performed on the first prototype, where the transceiver ASIC and the BAW dies are arranged next to each other and directly bonded onto a PCB (see Figure 4.40). The used BAW resonators are not equipped with a cavity, which would be required if the resonators were molded into a package. It was quite challenging for this prototype to prevent particles or condensed water from affecting the mechanical oscillation. Nonetheless environmental conditions, such as humidity and atmospheric pressure, may have influenced the measurements. Also an impact of light intensity was detected, since it changes all biasing currents provided by the bandgap. Molding is mandatory for the operation in the tire.

The dynamic potential of the capacitive tuning is shown in Figure 4.41. In this plot the carrier was FSK modulated with an 0-1-0-1 bit string. The deviation is 250 kHz at a data rate of 100 kbit/s in the left part of Figure 4.41, and 500 kHz with 2 Mbit/s at the right plot. For the plot the carrier was demodulated with a vector analyzer. The number of points in the right plot is limited by the capability of this vector analyzer.

4.5.2 DC Biasing Tuning

In addition to the capacitor bank, the BAW can be tuned with variable DC biasing. Biasing the resonator causes a change in the stiffness of the piezoelectric BAW-material and hence the resonance frequency is slightly shifted. The relation between frequency and DC biasing voltage, which is shown in Figure 4.42, is linear over a wide range with a typical slope of about 40 kHz/V. The variable output of a 5bit DAC is applied at the bottom electrode (AC ground), while the potential of the top electrode is constant. Due to the fast response of the resonator, this effect is used for FSK modulation of the carrier in transmit mode. As already shown, direct carrier modulation and frequency tuning is also possible with the digitally controlled tuning capacitors, but the

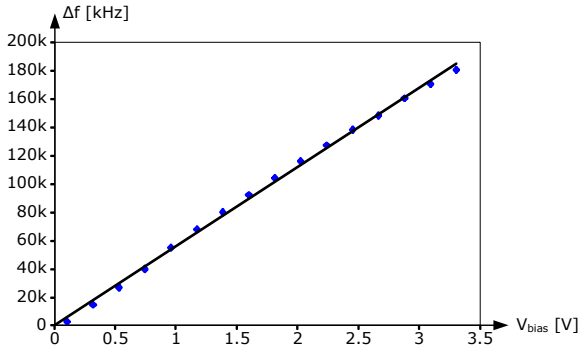
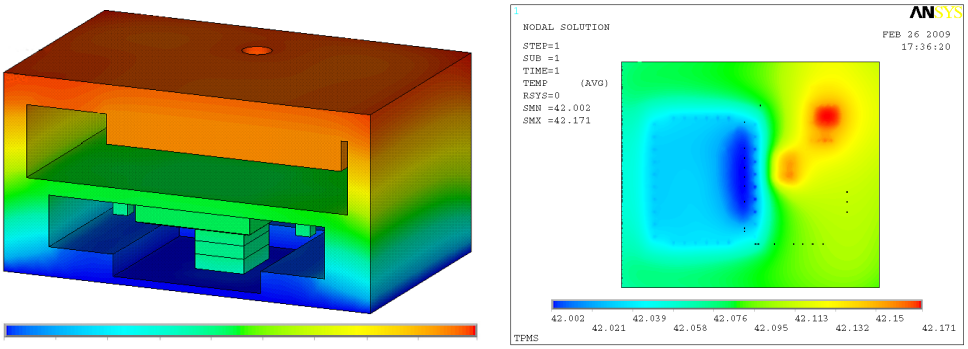


Figure 4.42: Measurement of the frequency shift versus applied DC biasing voltage V_{bias}.



Source: Fraunhofer-IIS EAS, Dresden **Source: Fraunhofer-IIS EAS, Dresden**

Figure 4.43: Simulated temperature of the whole sensor node caused by environmental change (left), and temperature variations of the chip stack (topview) due to self heating (right) [34].

nonlinear and process dependent relationship between capacitance and resonance frequency has to be taken into account.

4.5.3 Operation under Temperature Variations

The following chapter was taken from [8, 9, 14] (own publications). My contribution to this work was to provide the power consumption profile during transmission for the different blocks. The simulations were done by project partner Roland Martin (FhG IIS EAS, Dresden).

The temperature drift and process variation of the BAW resonator need to be compensated. For this reason the temperature is measured and then the desired tune word of the digitally controlled capacitors can be calculated by using the calibration information stored in the flash memory. It is important that the difference between the temperature at the sensor and at the BAW device is sufficiently low. In [14] the impact of the different heat sources on the temperature distribution was analyzed. The sensor node including the 3D integrated ASIC stack was modelled and a partial dif-

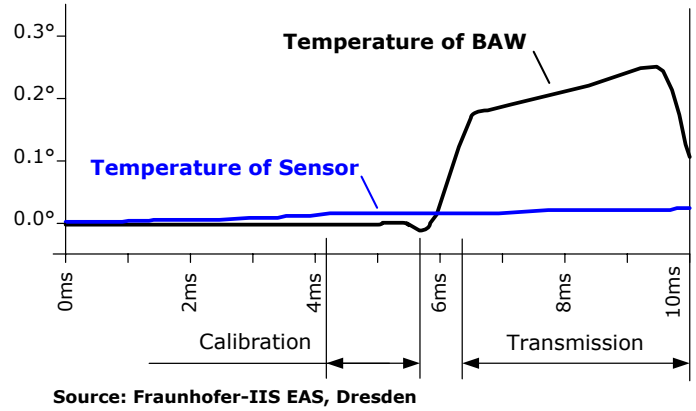


Figure 4.44: Simulated temperature variations during one transmission on BAW die and temperature sensor [9, 14].

ferential equation (PDE) solver was applied to enable detailed thermal analysis [34]. The simulated temperature distribution can be seen in Figure 4.43. In order to keep the overall peak current low, the temperature measurement and RF transmissions are not performed at the same time. In Figure 4.44 the resulting temperature difference between the temperature sensor and the BAW during one transmission cycle is illustrated. Additionally, in [14] the effects of environmental temperature changes were investigated, which seems to have only a minor impact on the unwanted temperature difference between sensor and resonator. Using the simulation results shown and the temperature drift of the resonator employed (18 ppm/°C, 2.1 GHz, [64]), the frequency shift due to self heating can be calculated to be 11 kHz. This can be disregarded.

4.6 Figure-of-Merit (FoM) and Comparison with State-of-the-Art

A traditional Figure-of-Merit (FoM) for oscillators was proposed in [76]. This FoM can be calculated with the help of equation 4.29. It contains the center frequency f_c, the phase noise performance $L(f_\mathrm{m})$ at an offset frequency f_m, and the power dissipation $P_\mathrm{diss} = V_\mathrm{DD} \cdot I$. But the tuning range is not taken into account in this FoM.

$$\begin{aligned} FoM_\mathrm{Osc}[\mathrm{dB}] &= 10\log\left(\left(\frac{f_\mathrm{c}}{f_\mathrm{m}}\right)^2 \frac{1}{L(f_\mathrm{m})V_\mathrm{DD}I}\right) = \\ &= -L(f_\mathrm{m})[\mathrm{dB}] + 20\log(\frac{f_\mathrm{c}}{f_\mathrm{m}}) - 10\log(P_\mathrm{diss}) \end{aligned} \tag{4.29}$$

A Figure-of-Merit (FoM) including the relative frequency tuning range (FTR) was defined in [75]. This FoM (see equation 4.30) was originally invented for VCOs, but was

Reference	IC Technology	Oscillator Topology				BAW Type	fc	Supply Voltage	Current Consum.	Power Dissipation	Temp. Range	Tuning Range	Phase Noise	Phase Noise	Phase noise	FoM OSC	FoM VCO
		Nr. Stages	Single Ended / Differential	Name	series / parallel		[GHz]	[V]	[mA]	[mW]	[°C]	[MHz]	@10kHz [dBc/Hz]	@100kHz [dBc/Hz]	@1MHz [dBc/Hz]	@100kHz [dB]	@100kHz [dB]
This Work	**CMOS 0.13µm**	**2**	**SE**		**f_p**	**SMR**	**2.1**[1]	**1.5**	**0.9**	**1.35**	**-40...125**	**10**	**-88**	**-112**	**-127**	**197**	**171**
[Vincent08]	CMOS 0.13µm	-	Diff		f_p	SMR	2.2	1	6	6	-	220	-84[2]	-112[2]	-135.7	191	191
[Aabbaoui09]	BiCMOS	1	SE	Santos	f_s	SMR	2.11	2.7	8	21.6	-	-	-103[2]	-127	-146[2]	200	-
[Aabbaoui09]	BiCMOS	-	Diff	Balanced Santos	f_s	SMR	2.11	2.7	8	21.6	-	-	-115[2]	-137	-154[2]	210	-
[Hu09]	CMOS 0.13µm	-	Diff		f_p	FBAR	1.58	1	0.5	0.5	-10...100	1.35	-85	-114	-138	201	160
[Rai07]	CMOS 0.13µm	-	Diff		f_p	FBAR	2.1	1	0.6	0.6	-	<21	-95[2]	-128[2]	-144	217	197
[Ito08]	CMOS 65nm	-	Diff		f_p	FBAR	1.7	0.9	1.7	1.5	-	6.4	-97	-114[2]	-133[2]	197	168
[Rai09]	CMOS 0.35µm	1	SE	Pierce	f_s	FBAR	1.5	-	-	0.95	0...100	0.3	-	-125	-	209	155
[Otis03]	CMOS 0.18µm	1	SE	Pierce	f_s	FBAR	1.9	1	0.3	0.3	-	-	-100	-120	-140	211	-
[Guillot08]	CMOS 65nm	-	Diff		f_p	SMR	2	-	-	0.9	-	4	-116	-128	-152	214	180
[Chabloz07]	CMOS 0.18µm	-	Diff		f_p	?	2.5	1.2 (?)	1.6	1.9	-	-	-93	-115[3]	-133[3]	200	-
[Dossou08]	CMOS 65nm	-	Diff		f_p	SMR	2.1	1.2	0.05	0.06	-	-	-95	-124	-141	214	-
[Chee05]	CMOS 0.13µm	1	SE	Pierce	f_s	FBAR	1.9	0.43	0.21	0.089	-	-	-98	-120	-138	211	-
[Aissi06]	BiCMOS 0.35µm	-	Diff	Balanced Santos	f_s	FBAR	5.46	-	-	-	-	-	-	-121	-	-	-
[Razafimandimby07]	SiGe BiCMOS 0.25µm	1	SE	Colpits	f_s	SMR	2.145	2.5	4.8	12	-	-	-	-124	-	191	-
[Vanhelmont06]	BiCMOS	1	SE	Butler	f_s	SMR	2	2.7	1.5	4.05	-	-	-99	-120	-138[2]	200	-
[Pang07]	CMOS 0.35µm	1	SE	Santos	f_s	FBAR	0.6	3.3	2	6.6	-	-	-132	-151	-160	218	-
[Pang08]	CMOS 0.35µm	1	SE	Santos	f_s	FBAR	0.6	3.3	1.61	5.3	-35...85	-	-130	-149	-152	217	-
[Östman06]	SiGe BiCMOS 0.25µm	2	SE		f_s	FBAR	2.1	2.4	30	72	-	57	-93[2]	-124[2]	-144	192	181

[1] Oscillator was also tested with 2.45GHz BAW resonator, values are given for 2.1GHz BAW.
[2] These values are read from graphs.
[3] These values are extrapolated.

[Vincent08] = [77]	[Aabbaoui09] = [78]	[Hu09] = [79]
[Rai07] = [81] or [80]	[Ito08] = [82]	[Rai09] = [83]
[Otis03] = [84]	[Guillot08] = [85]	[Chabloz07] = [86]
[Dossou08] = [87]	[Chee05] = [88] or [89]	[Aissi06] = [90]
[Razafimandimby07] = [92]	[Vanhelmont06] = [93]	[Pang07] = [94]
[Pang08] = [95]	[Östman06] = [96]	

Table 4.1: Comparison of this work with other high performance BAW oscillators including Figure-of-Merit (FoM).

also applied to BAW based oscillators for example in [77].

$$FoM_{\mathrm{VCO}}[\mathrm{dB}] = -L(f_{\mathrm{m}})[\mathrm{dB}] + 20\log(\frac{f_{\mathrm{c}}}{f_{\mathrm{m}}}) + 20\log(\frac{FTR}{10}) - 10\log(P_{\mathrm{diss}}) \tag{4.30}$$

A performance comparison is given in Table 4.1 and a graphical representation of the FoM versus the dissipated power can be found in Figure 4.45. The proposed oscillator is outperformed by oscillators using FBAR resonators or by using a more advanced technology. As already explained in chapter 4.5, in the majority of cases the quality factors of FBAR resonators are higher compared to that of SMR resonators due to lower losses into the substrate. As one might suspect, a better quality factor helps to decrease the phase noise of an oscillator. Additionally, the absolute impedance at parallel resonance of the resonator is important for the performance of the oscillator. Amongst other things, this impedance is affected by the quality factor. Furthermore, the proposed oscillator includes an ESD protection circuit. The lossy capacitance caused by this circuit also reduces the performance and this is also not considered by the FoM.

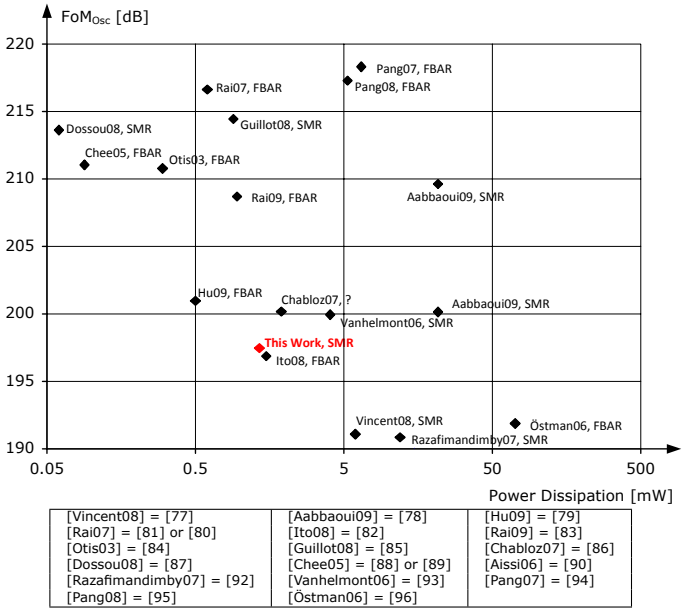


Figure 4.45: Figure-of-Merit (FoM) of different oscillators versus dissipated power.

4.7 Conclusion

A quartz crystal oscillator always tends to operate very close to the series resonance frequency, which is the internal quartz crystal frequency. Then the resonance frequency of the oscillator is independent from packaging and mounting [55]. Additionally, the transconductance g_{m} has only a minor impact on the resonance frequency. For a high frequency BAW resonator, the inductance of the interconnection between resonator and oscillator (for instance the bondwire) can have the same impact as parasitic capacitances. For example, an inductance of 1 nH in series to the resonator already causes a shift of the series resonance frequency of about 6300 ppm. The required transconductance g_{m} of a one-transistor oscillator has to be very high for high frequencies. Hence the current consumption is quite high. Because of this, the proposed BAW oscillator consists of two gain stages. The use of two gain stages while also operating close to the series resonance frequency implies the risk of parasitic oscillation. Hence the proposed oscillator topology oscillates close to the parallel resonance frequency. The oscillator core consumes 800 µA, and a further 80 µA are needed for biasing. The start-up time is lower than 2 µs and the phase noise is -112 dBc/Hz at a distance of 100 kHz from the carrier.

The proposed oscillator is tunable over a frequency range of about 10 MHz to enable temperature and process compensation. Tuning is achieved by connecting digitally controlled capacitors of about 1 pF in parallel to the BAW resonator. The remaining frequency deviation after applying the temperature compensation algorithm is lower than ±150ppm.

In addition to the capacitor bank, the BAW can be tuned with variable DC biasing.

This can be used for modulation. The relation between frequency and DC biasing voltage is linear over a wide range with a typical slope of about 40 kHz/V.

5 Asynchronous Dividers

The text of the chapters 5.1 to 5.6 was taken from [3] (own publication). Preliminary work was done in the related diploma thesis [15].

Even in a PLL-less implementation, dividers are needed to generate the clock signal for the digital domain. But, as shown in chapter 2 on page 35, a BAW oscillator in combination with a PLL can be advantageous. First, a short introduction into the timing problem in dual modulus dividers used in PLLs is given. This is followed by a basic description of the principle of asynchronous state machines. Based on the dividers proposed in [46] a low power asynchronous 1/2/3 multi-modulus divider will be presented. The proposed divider was not implemented in the transmitter, but was tested on a test chip produced in a 0.24 µm technology and simulated in a 0.13 µm technology.

5.1 Introduction into the Timing Problem of Dual Modulus Dividers

To avoid high power consumption, it is necessary to clock as few transistors as possible at high frequencies. So the dual modulus divider cannot be an ordinary synchronous state machine. The swallow counter technique (see Figure 5.1) employs the conventional design, which consists of a dual modulus prescaler, a pulse- and

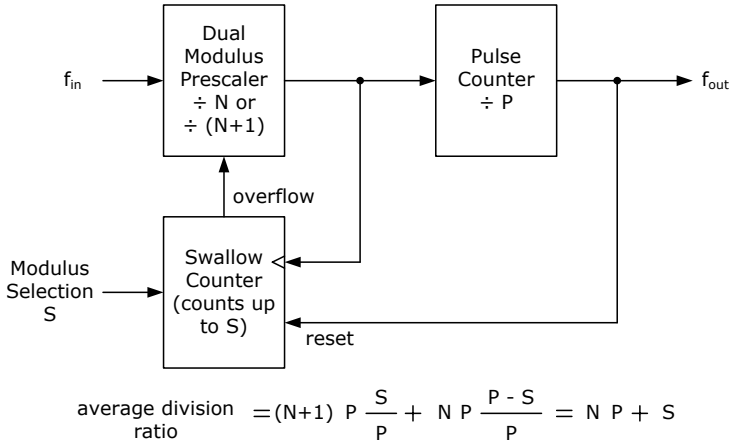


Figure 5.1: Basic principle of the swallow counter technique.

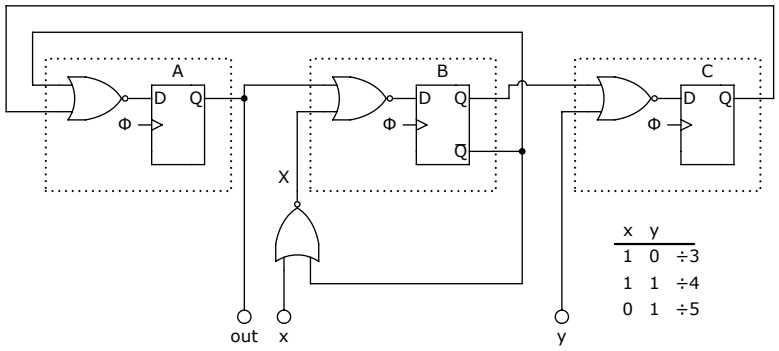


Figure 5.2: State-of-the-art implementation of a multi-modulus prescaler.

a swallow counter. After the initial reset the prescaler divides by $(N + 1)$ until the swallow counter overflows, changing the modulus control signal. The prescaler then divides by N until the pulse counter reaches P counts. Then a reset of the swallow counter follows. The average division ratio can be calculated as shown in Figure 5.1. For S out of P pulses, the division ratio is $(N + 1) \cdot P$, and for the remaining $(P - S)$ pulses, the division ratio is $N \cdot P$. So the average division ratio is equal to $(N \cdot P + S)$. The advantage of this design is that the dual modulus prescaler can be built with a small N - so only few transistors are clocked at the highest frequency.

An example of a multi-modulus prescaler (with a division rate of 3/4/5) is illustrated in Figure 5.2. By analysis of the shown divider one recognizes that for a correct state sequence, the control signals of the multi-modulus prescaler has to be valid in a particular time window. A simplified analysis (the flip flops and logic gates have no delay, no hold time and the setup time is one clock cycle) is shown in Figure 5.3. In the worst case, this time window begins two clock periods after the significant edge of the output of the prescaler and ends three periods later. That is why the maximum delay of the control signal for controlling the division rate is two periods of the clock signal.

The delay of the control signal (see Figure 5.4) is caused by the delay of the reset impulse (caused by the pulse counter and swallow counter) and the delay of the overflow signal (caused by the swallow counter).

A simple and often used application of the swallow counter technique is illustrated in Figure 5.5: A $M/(M + 1)$ (with $M = N \cdot P$) dual modulus divider is realized with a dual modulus prescaler, a pulse counter and a simple gate (is equivalent to a swallow counter with $S = 1$). As mentioned above, the advantage of this construction is that only as few transistors as possible are clocked at the highest frequency. The delay for the generation of the reset pulse is only caused by the first flip flop (the remaining flip flops in the chain are already in the correct state) and by the gate necessary for decoding the control input.

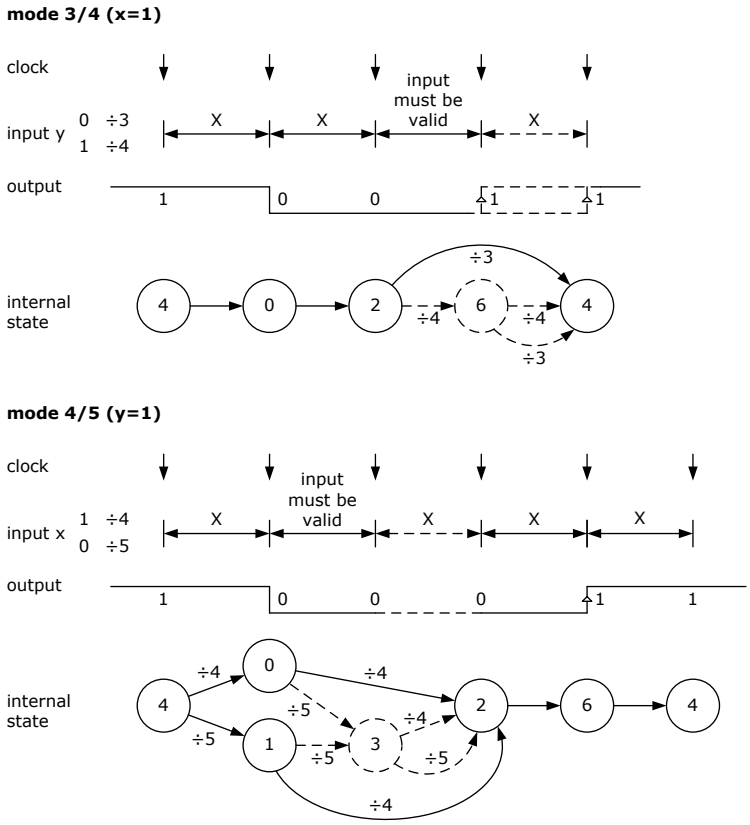


Figure 5.3: Simplified analysis of the multi-modulus prescaler illustrated in Figure 5.2.

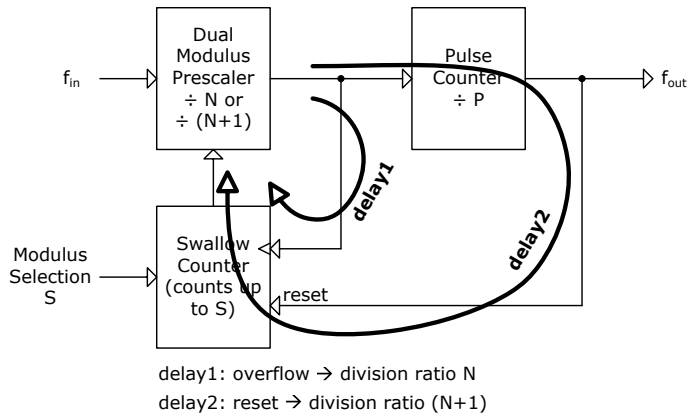


Figure 5.4: Delay in the control signal for the prescaler.

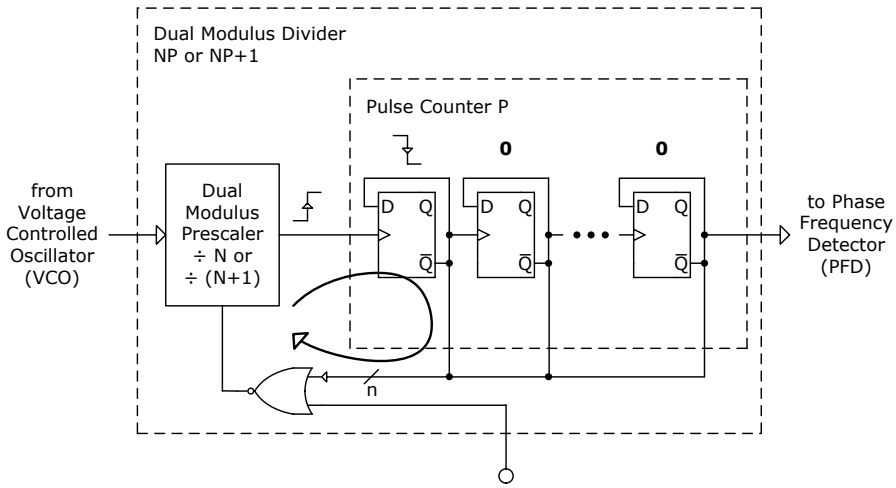


Figure 5.5: Simplest form of the swallow counter technique.

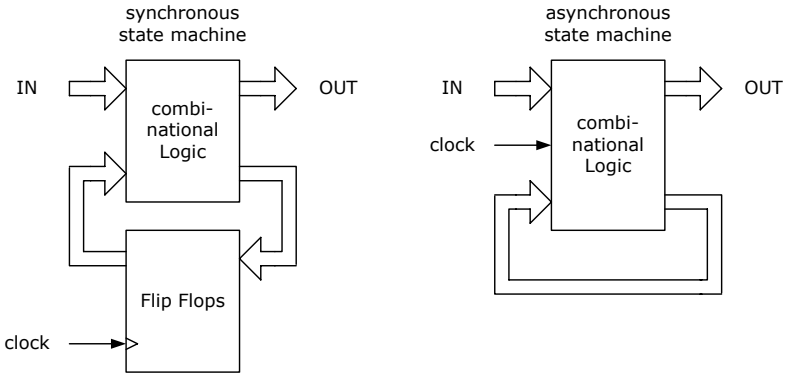


Figure 5.6: Synchronous versus asynchronous state machine.

5.2 Basic Principle of the Asynchronous Counter

Flip flops are used in synchronous systems (pictured in Figure 5.6). Such a system consists of a combinational logic and registers, which hold the system state.

Hence all registers are controlled by a single global clock and therefore the system is called synchronous. The counterpart of this synchronous state machine is an asynchronous one. A possible definition of an asynchronous state machine could be a state machine only consisting of combinational logic with feedback. Basically, a flip flop is built as such an asynchronous state machine. This is why one could refer to synchronous state machines as a subclass of asynchronous ones. There exist mathematical methods for the development of asynchronous state machines, hence it is possible to synthesize ideal (high speed, low power) flip flops and ideal dividers. The state diagram of such an ideal divider by 3 is illustrated in Figure 5.8.

This divider by 3 was presented in [46] in 1972 and first used in an electronic wristwatch. The logical structure for this divider cell is the first original result of

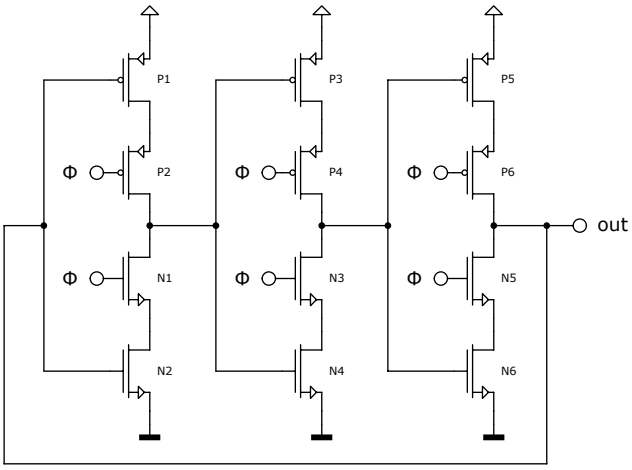


Figure 5.7: Implementation of an ideal asynchronous divider by 3.

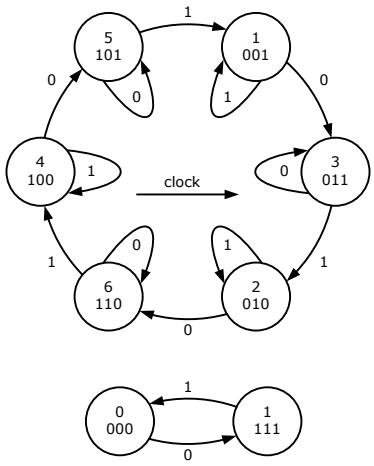


Figure 5.8: State diagram of an ideal divider by 3.

an attempt to synthesize all possible asynchronous state machines realizable with a given number of two level gates [46]. It was obtained manually by means of a special algorithm based on the standard Huffman method [46]. The realization can be seen in Figure 5.7.

The basic principle (see Figure 5.9) of the divider by 3 is very simple: In a chain of three inverters, one inverter always tries to change its output. For example, if A=1, B=1, C=0 the inverter B will change its output to zero - but this is only possible in the clock high state. After the clock high phase (A=1, B=0, C=0) the inverter C will be able to load node C to supply. So in each clock phase one node always changes its state. In a real implementation it is recommended that the order of switches and inverter transistors be changed as shown in Figure 5.7.

To obtain an ideal divider with a division rate of two (is equivalent to a flip flop), two states in Figure 5.8 can simply be skipped. The corresponding circuit (taken

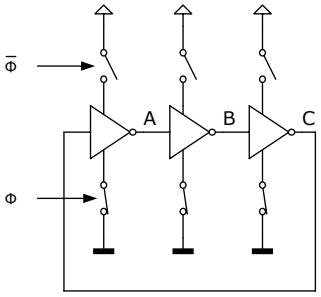


Figure 5.9: Basic principle of the ideal asynchronous divider by 3.

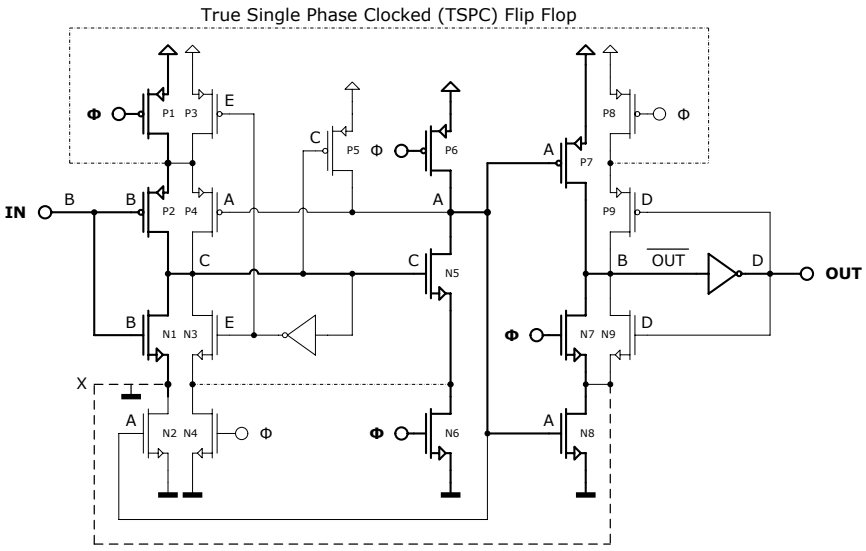


Figure 5.10: Implementation of an ideal flip flop (bold=dynamic=Yuan-Svensson flip flop [47]).

from [46]) can be found in Figure 5.10. If the output is connected to the input, the circuit operates as a divider - otherwise the circuit represents a D-type flip flop with an inverted output.

It is important to keep in mind that the circuits are the result of the synthesis of an asynchronous state machine. This is why one can easily develop a dynamic and a static version. The dynamic version (only the bold transistors in Figure 5.10) is fundamentally the same circuit as in Figure 5.7, except that the transistors N1, P3 and P6 are left out. If these transistors are missing, two states of the state diagram in Figure 5.8 are skipped and the division rate of 2 is chosen. This kind of flip flop is known as Yuan-Svensson flip flop [47]. The reader is invited to analyze the static version of the D-type flip flop, because these additional (narrow) transistors can be used on demand to solve isolation problems known in this kind of flip flops. These transistors offer better solutions than the commonly used ones, proposed in [48].

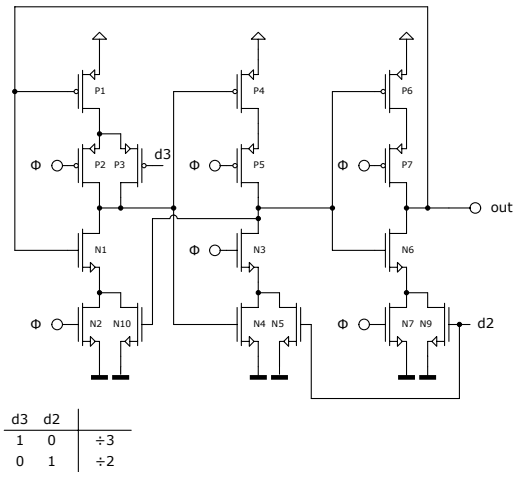


Figure 5.11: An asynchronous divider by 2 (d2=1) and by 3 (d3=1).

5.3 An Asynchronous 2/3 Divider

The circuit of an ideal divider by 3 and the appropriate state diagram can be seen in Figure 5.7 and Figure 5.8. For a division rate of 2, two (state 3 and state 2) out of six states have to be skipped, resulting in the circuit illustrated in Figure 5.10. The first idea is to make this adaptation of the division rate dynamic. The circuit is shown in Figure 5.11. The state diagram of this divider is more complicated: the transition from one state to another depends on the input clock and on the control signals d2 and d3. Every state can be left with 4 possible transitions: two possibilities if the clock is high (bold arrows) and two possibilities if the clock is low (narrow arrows). X indicates that it does not matter if d2 or d3 is high. Note that one out of the two control signals d2 and d3 must be high. The combinations d2=0, d3=0 and d2=1, d3=1 are forbidden. If d3 is set to high (and d2 to low) the state machine runs through the states 1, 3, 2, 6, 4, and 5. If d2 is set to high (and d3 to low), states 3 and 2 are skipped (theoretically the finite state machine runs to these states too, but the states are left immediately). The output of the asynchronous finite state machine is set to the last digit of the state (bold digit). The whole state diagram can be seen in Figure 5.12.

5.4 Timing Problem with the proposed 2/3 Divider

Compared to the multi-modulus divider illustrated in Figure 5.2, timing is more complicated in asynchronous state machines. Provided that the calculation of the division control signal (done by the pulse counter and by the swallow counter) starts with the positive edge at the output of the 2/3 dual modulus divider, the maximum delay can be one clock cycle. For explanation see Figure 5.13: In this time response diagram the clock signal, the output (with the current state), and the control signals are dis-

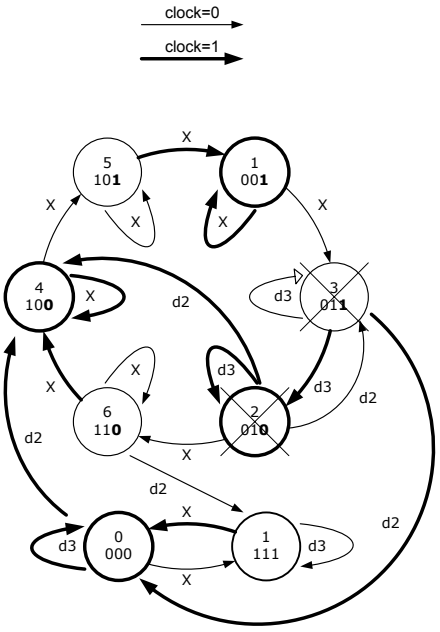


Figure 5.12: Complete state diagram of the 2/3 divider.

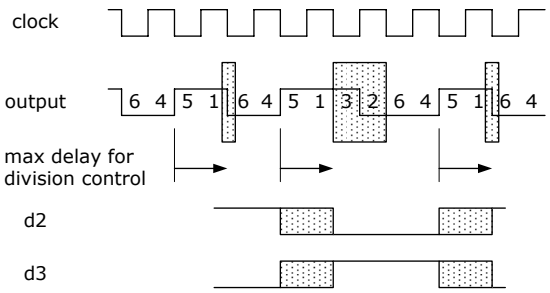


Figure 5.13: Timing window for the proposed 2/3 divider.

played. The analysis of the state diagram shows that the control signals must be stable in a particular time window (dotted area). Therefore, only one clock cycle is available for the calculation of the control signals after the significant positive edge. In other words, this means that delays through the pulse and swallow counter have to be smaller than one clock period. Consider now the often used application with a dual modulus divider M/(M+1). In this special case, no swallow counter is needed. The pulse counter is decoded as mentioned earlier. To avoid a gate with n inputs, it is easier to decode the state 000...0 recursively, as shown in Figure 5.14.

The delay caused by the pulse counter is given by the delay through the first flip flop in the asynchronous divider chain, the delay through one NOR-gate, and the delay through one inverter. This is equivalent with the statement that the first stage of the pulse counter must be able to be clocked with the input clock signal. For the flip flops of the pulse counter, the use of the circuit displayed in Figure 5.10 is recommended.

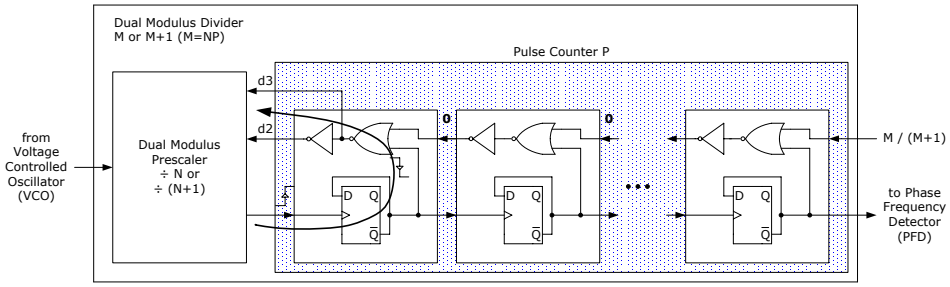


Figure 5.14: Typical application for the proposed asynchronous 2/3 divider.

The dynamic version should be utilized for the first stages and the static version for the stages at the end of the chain, which are clocked with a lower frequency. In Figure 5.15 the simulated output waveforms are illustrated. It might be a problem to meet the timing condition described earlier.

To increase the maximum allowed delay, the output of the asynchronous 2/3 counter can be inverted (this is equivalent to using negative edge triggered flip flops). The inverter is convenient because of its driving ability. If the calculation of the control signal starts at the negative edge, the time available for the computation is doubled (see Figure 5.16).

But there is a disadvantage: The control signal has to keep its old value half a period after the significant edge. To meet this condition over process parameters, supply voltage, and temperature range, a latch can be inserted in the first stage of the pulse counter (see Figure 5.17). A realization of the p-latch is shown in Figure 5.18.

5.5 An Asynchronous 1/2/3 Divider

The proposed 2/3 divider can be extended to a 1/2/3 divider. To achieve a division rate of one, two other states in the state diagram (Figure 5.8) have to be skipped. As this state diagram is quite complicated, it is not illustrated here. However, the circuit implementation is surprisingly simple (see Figure 5.19).

To prove the functionality in case of division by one, look at Figure 5.20: Assuming that the output is the inverted clock signal, the first stage remains at high (transistors N1 and N2 are never conducting at the same time). Because of a high input, the second stage is low and that is why transistor P5 is conducting and so the third stage inverts the clock.

If the 1/2/3 divider is used as a 1/2 dual modulus divider (in most cases this is only theoretical, because 2/3 is more energy efficient) the timing is simple and can be seen in Figure 5.21.

If the computation starts with the negative edge (the output of the circuit in Figure 5.19 is inverted) there is one period time to get the control signals stable. The latch mentioned earlier is not necessary here, because there is no required minimum

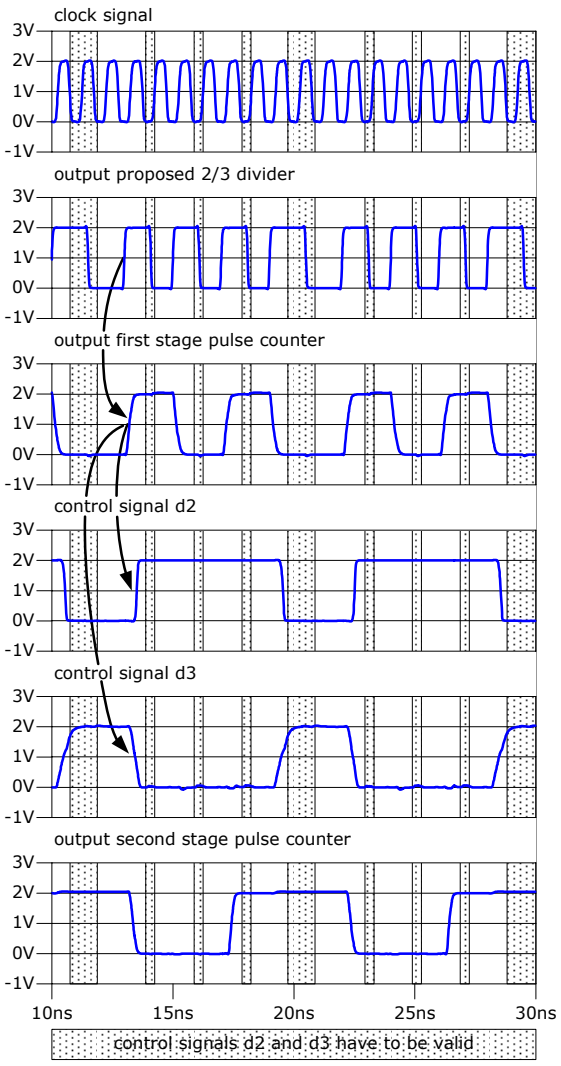


Figure 5.15: Simulated waveforms in a 0.24 µm technology.

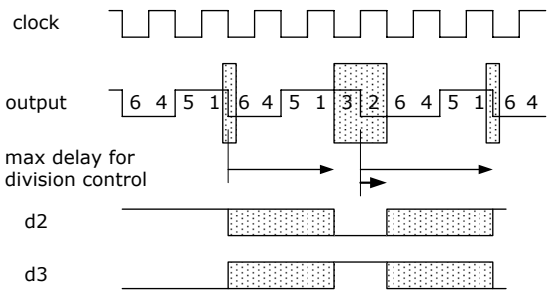


Figure 5.16: Timing window if computation is started with negative edge.

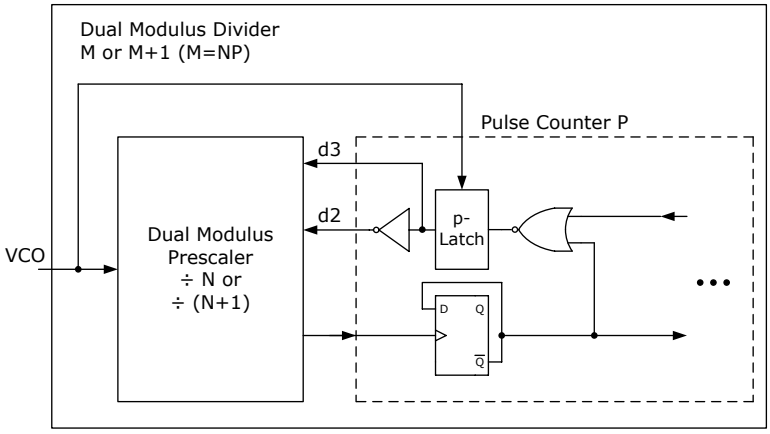


Figure 5.17: A p-latch inserted in the first stage of the pulse counter.

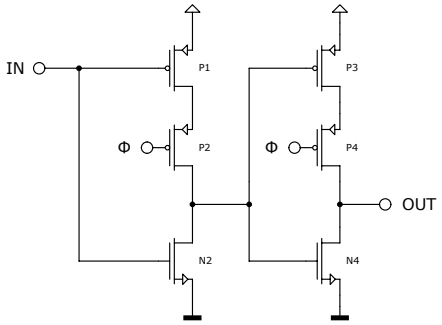


Figure 5.18: Implementation of the non precharged true single phase clocked p-latch.

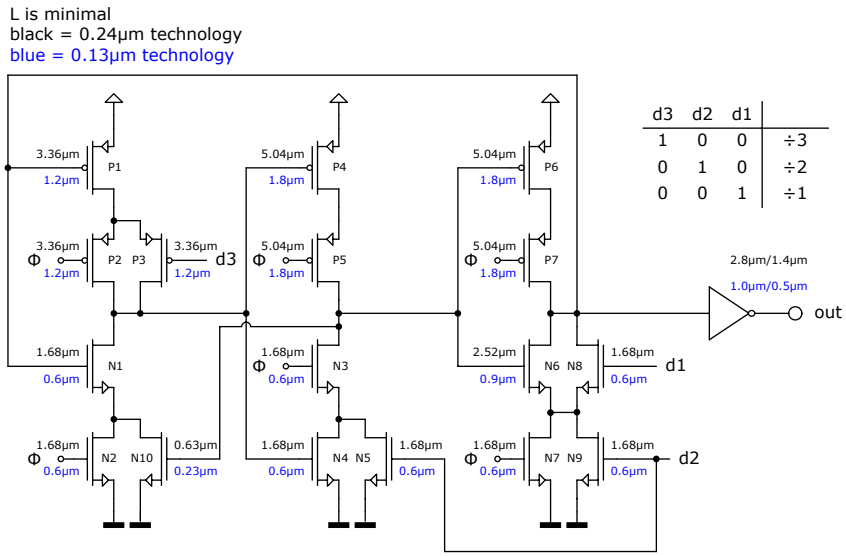


Figure 5.19: Implementation of the proposed 1/2/3 divider.

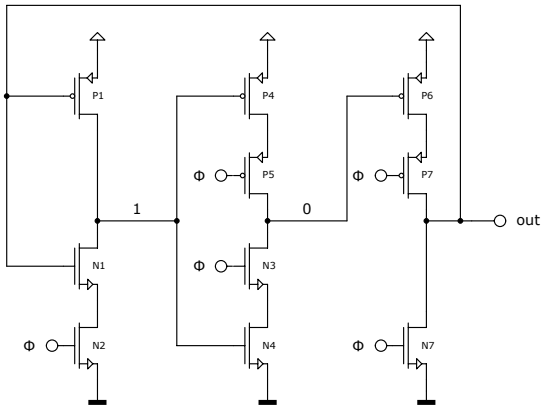


Figure 5.20: Circuit of Figure 5.19 if d1 is high and d2 and d3 are low.

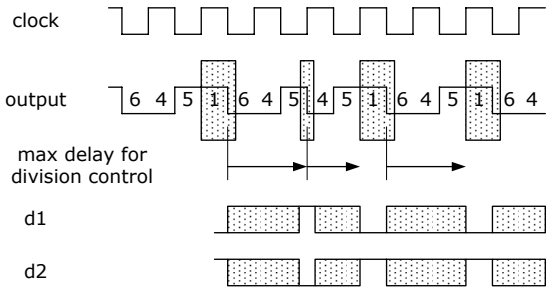


Figure 5.21: Timing window of 1/2 divider if computation is started with negative edge.

delay. If the 1/2/3 divider is applied in a modulus PLL, the timing gets difficult: If we start with the positive edge, only half of the clock period is available for computation. If we insert a latch (necessary in division mode 3), the advantage of a longer delay (one period of the clock signal) is reduced by the delay of the latch.

The proposed novel 1/2/3 divider is not part of the proposed transmitter, but was tested on a test chip implemented in a 0.24 µm CMOS process. The divider was also simulated using a 0.13 µm process. At 2.45 GHz it consumes 75 µA, 85 µA, and 60 µA, in division by 1, 2, and 3 mode, respectively. The divider operates at a supply voltage of 1.5 V within a temperature range of -40°C to 125°C.

5.6 Typical Application of a 1/2/3 Divider

The proposed divider may be very useful if a permanent change of the division rate is needed. A possible implementation for ISM (Industrial, Scientific, and Medical) frequencies below 1 GHz can be seen in Figure 5.22.

If the synthesizer drives an open drain power amplifier, the duty cycle of the output signal has a deep impact on the efficiency. Efficiency over the duty cycle is illustrated

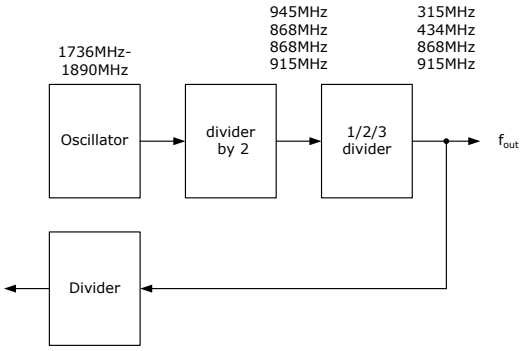


Figure 5.22: Possible application of a 1/2/3 Divider.

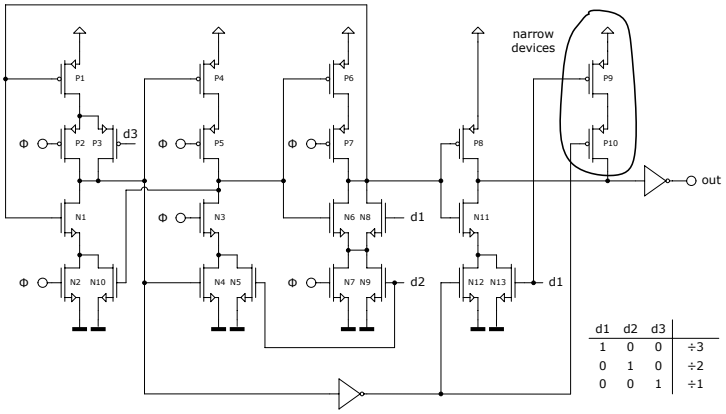


Figure 5.23: Proposed 1/2/3 divider with duty cycle correction.

in Figure 6.11 on page 122 and the maximum can be found at a duty cycle of about 20-30%. To achieve this duty cycle at least at the division rate 2 a slight modification is necessary. This modification is illustrated in Figure 5.23. The simulated output waveforms can be seen in Figure 5.24. It is important to notice that without duty cycle correction the output duty cycle in division by 3 mode is 50%. This would not be possible with a synchronous state machine (the output changes once at the positive and once at the negative edge). The proposed circuit is not part of the proposed transmitter, but was tested in a 0.24 µm CMOS process. The active area of the divider measures approximately 13 µm × 55 µm. The divider operates at 1 GHz within a temperature range from -40°C up to 125°C.

5.7 A 1.5 Divider

The approach of an asynchronous divider can be used to design a divider with a division ratio of a fraction of an integer (e.g. 1.5). There exist several reasons why this can be very advantageous:

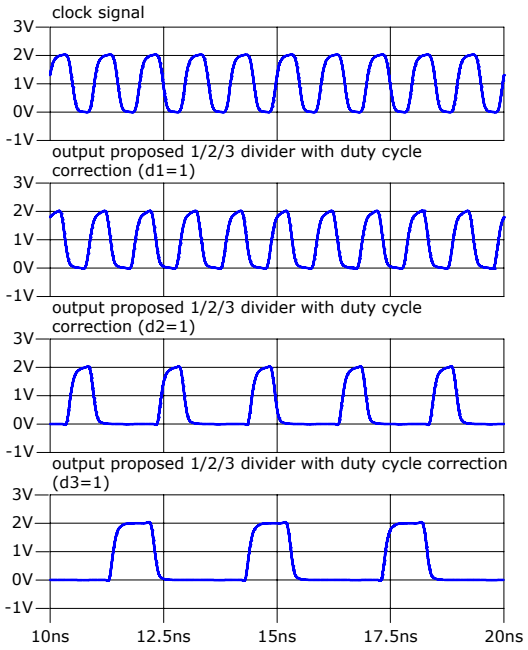


Figure 5.24: Output wave form of 1/2/3 divider with duty cycle correction.

- As already mentioned in chapter 2.2 on page 42 in a BAW based transmitter, it can be very important that the oscillator frequency is not an integer multiple of the transmitted frequency, otherwise one must guarantee that there is no coupling between the power amplifier and oscillator (VCO pulling). The effect of such coupling would be an unintended frequency shift when the power amplifier is turned on, or in the worst case a frequency shift if the environment of the sensor node changes (e.g. by keeping the hand close above the transmitter ASIC) due to the different coupling. A 1.5 divider can create a perfect isolation between oscillator and other blocks.

- In a receiver a very similar problem can occur: If the received frequency is an integer multiple of the BAW oscillator or of the reference oscillator in general, the sensitivity can be decreased. Also in this case a 1.5 divider can be used to overcome this problem.

- In an integer-PLL based synthesizer only integer multiples of the reference clock can be generated. To increase the number of synthesizable frequencies the reference clock can be decreased by using an additionally frequency divider (reference divider). However, the reference clock of a PLL cannot be arbitrarily small, because the design of the PLL control loop becomes quite challenging. A 1.5 divider can be used to increase the number of synthesizable frequencies.

- In some fractional-N-PLLs frequencies close to integer multiple of the reference signal cannot be synthesized, because for good noise shaping, a division factor

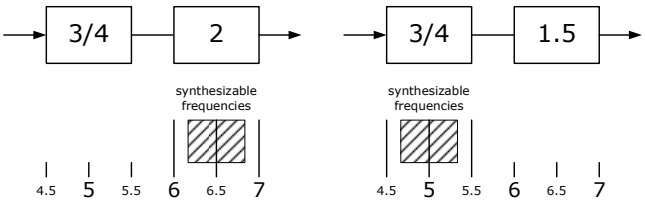


Figure 5.25: Synthesizable frequencies with an N/N+1 dual modulus divider.

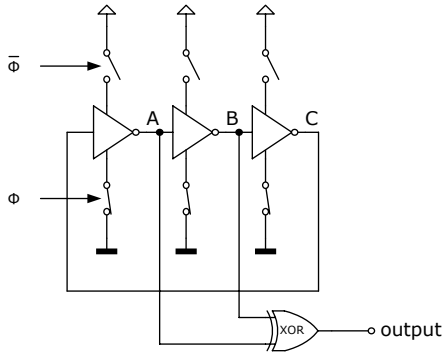


Figure 5.26: Implementation of an asynchronous 1.5 divider.

N close to {1.5, 2.5, 3.5, 4.5 ...} is preferred (in case of an often used N/(N+1) dual modulus divider). If a 1.5 divider is implemented, this can be shifted to an integer value.

- In almost all receivers and transmitters the VCO does not run on the RF-carrier frequency in order to avoid disturbances and coupling between the power amplifier and the VCO. In a typical implementation the VCO runs on twice the frequency of the RF-carrier. By making use of the 1.5 divider, the VCO frequency can be reduced to 1.5 times of the carrier frequency. This can help to reduce the power consumption of the (RC) VCO and additionally the output of the 1.5 divider has a duty cycle of 33%, which is advantageous for switched power amplifier (e.g. class C or class E). This is also true in the case of a BAW based transmitter.

- In general, integer division ratios can easily be achieved. Non-integer division ratios are difficult to realize and require considerable effort. An asynchronous 1.5 frequency divider might offer new possibilities.

To implement a 3/2 (=1.5) division ratio, two different nodes of the divider shown in Figure 5.7 are combined with an XOR as illustrated in Figure 5.26. The output of the XOR exhibits two periods in one period of the divided by 3 signal. So in principle the clock signal is divided by 3 and multiplied by 2 without making use of an injection locked divider or oscillator. The corresponding time plots are given in Figure 5.27.

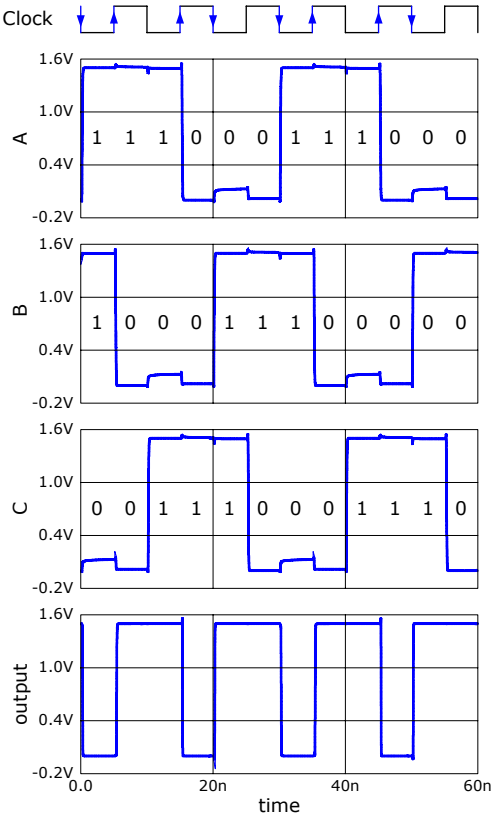


Figure 5.27: Simulated time response of node A, B, and C and the output (A XOR B).

Note that the output (A XOR B), shown in Figure 5.27, changes its state sometimes with the rising, and sometimes with the falling, clock edge.

Figure 5.28 shows the simulated output spectra of a 100 MHz clock signal and the 66.7 MHz output of such a divider. The harmonics of the clock signal and the harmonics of the output signal do not occur at the same frequency.

The proposed 1.5 divider is not part of the e-Cubes transmitter. The idea of a 1.5 divider arises since the transmitters suffer from the pulling effect as already shown in chapter 2.2. The divider was not implemented on a test chip; all results are based on simulation.

5.8 Figure-of-Merit (FoM) and Comparison with State-of-the-Art

A comparison of different multi-modulus dividers is not easy, because a lot of conditions have to be taken into account. In recently published papers it is often not clear whether or not the current for driving the input was considered. Clearly the load also has a deep impact on the current consumption. Maybe there is also a great

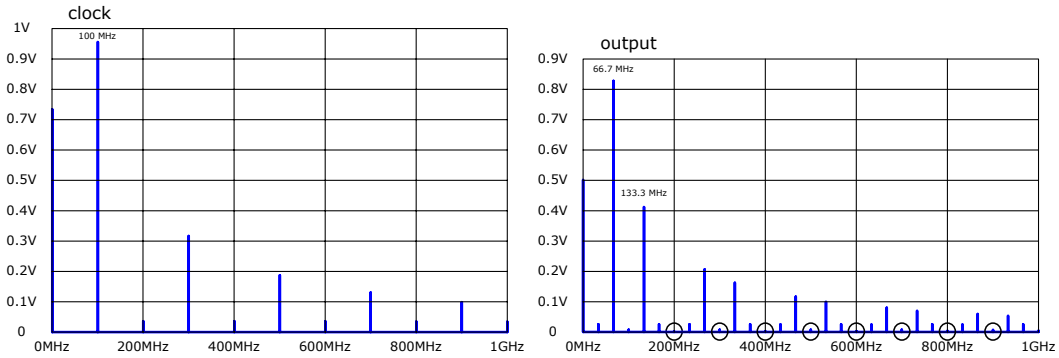


Figure 5.28: Output spectrum of the clock signal and of the output.

Reference	IC Technology	Division Ratio / Architecture	fc [GHz]	Supply Voltage [V]	Current Consum. [µA]	Power Consum. [µW]	Temp. Range [°C]	Energy per clock edge [pJ]	Power Efficiency [GHz/mW]
[This Work]	**CMOS 0.13µm**	**1/2/3 - TSPC**	**2.45**	**1.5**	**85**	**128**	**-40...125**	**0.052**	**19.2**
[Ray2009]	SiGe 0.13µm	2/3 - CML	13.84	2.2	500	1100	-	0.079	12.6
[Ray2009]	SiGe 0.13µm	2/3 - CML	6.92	2.2	250	550	-	0.079	12.6
[Vaucher2000]	CMOS 0.35µm	2/3 - SCL	2	2.2	100	220	-	0.110	9.1
[Vaucher2000]	CMOS 0.35µm	2/3 - SCL	1	2.2	50	110	-	0.110	9.1
[Sandireddy2004]	SiGe 47GHz f_T	2/3 - CML	7.5	-	7000	-	-	-	-
[Kim2010]	CMOS 0.25µm	2/3 - E-TSPC	3	2	1360	2720	-	0.907	1.10
[KRISHNA2010]	CMOS 0.18µm	2/3 - E-TSPC	4.9	1.8	-	306	-	0.062	16.0
[KRISHNA2010]	CMOS 0.18µm	2/3 - E-TSPC	4.9	1.8	-	1030	-	0.210	4.76
[Yu2006]	CMOS 0.18µm	2/3 - E-TSPC	4	1.8	-	3300	-	0.825	1.21

[Ray2009] = [49]	[Vaucher2000] = [53]	[Sandireddy2004] = [50]
[Kim2010] = [51]	[Krishna2010] = [52]	[Yu2006] = [54]

Table 5.1: Comparison of the proposed 1/2/3 divider with other high performance 2/3 dual modulus divider.

difference in the current consumption between different divider settings. Additionally, in many papers the current consumption of the whole divider chain is given. Nevertheless, a comparison of different multi-modulus dividers is given in Table 5.1. As Figure-of-Merit the power-efficiency is used (see equation 5.1).

$$FoM_{\mathrm{MMD}} = \frac{f}{P_{\mathrm{MMD}}} \tag{5.1}$$

For the proposed divider, the power for driving the input was not considered. The circuit is loaded with a buffer as shown in Figure 5.19 and the current consumption was specified for when the divider is dividing by 2, which is the worst case. A visual impression of the performance can be obtained from Figure 5.29.

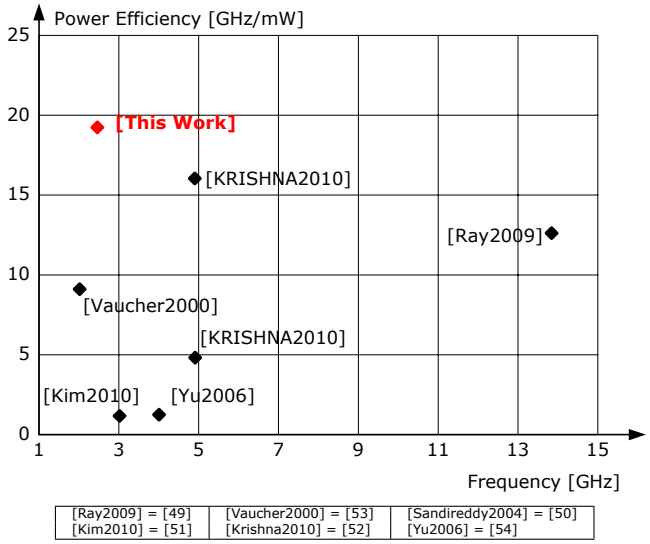


Figure 5.29: Power-efficiency of different dual modulus dividers versus frequency.

5.9 Conclusion

A new kind of asynchronous 1/2/3 divider was presented [15]. This novel divider comprises two ideal, well-known counters: an ideal divider by 2 [47] and an ideal divider by 3 [46]. The combination of these two circuits provides the ability to change the division ratios between 2 and 3. The divider can be used for instance in a fractional divider as dual modulus prescaler. If the 1/2/3 counter is used as an integer divider in a PLL, a duty cycle correction can be performed to increase the efficiency of the open drain power amplifier. A state-of-the-art (synchronous) solution for a 2/3 dual modulus divider needs 2 flip flops and perhaps (if not included in the flip flops) some logic. A comparison with other high performance dividers showed that the power consumption can be reduced by using this approach. The divider was simulated using a 0.13 µm process. At 2.45 GHz it consumes 75 µA, 85 µA, and 60 µA, in division mode 1, 2, and 3, respectively. The divider operates at a supply voltage of 1.5 V within a temperature range from -40°C up to 125°C. The proposed 1/2/3 divider is not part of the proposed transmitter test chip, but was also tested on a test chip implemented in a 0.24 µm CMOS process.

A new asynchronous 1.5 frequency divider, based on the divider by 3 [46], can also be used to overcome several issues. The main issue is the isolation between the BAW oscillator (or VCO, or quartz crystal oscillator in a PLL) and other building blocks (e.g. the power amplifier). By dividing the reference signal by a factor of 1.5, the harmonics of the clock signal and the harmonics of the output signal do not occur at the same frequency.

6 Matching Network and Power Amplifier

6.1 Matching Network and RX/TX switch

Common transceivers contain a matching network to connect the power amplifier to the antenna in such a way that the power amplifier can deliver the desired output power. Simultaneously, efficiency should be as high as possible. To do this, the matching network has to provide the correct load impedance to the power amplifier. This load impedance is normally not matched to the output impedance of the power amplifier, because otherwise the efficiency would be limited to 50%. For a high efficiency the load resistance should be much higher than the output resistance of the power amplifier.

Another task of the matching network is to deliver the maximum power from the antenna to the low noise amplifier (LNA). In this case the real part of the LNA input impedance is matched to the real part of the antenna output impedance. Therefore it is required to have a resistive component in the input impedance of the LNA, although in CMOS the input of a common source amplifier or of a differential pair is almost purely capacitive. In this case, the target of the matching network is not to deliver the maximum power; instead, the matching network should deliver the highest possible voltage at the LNA input.

Another issue is that in on-chip networks the available capacitors and especially inductors have very bad quality (Q) factors, which make on-chip matching very difficult. For this special application the proposed circuit tries to overcome the impairment of the on-chip devices.

6.1.1 Matching Theory

Figure 6.1 shows the equivalent circuit of an antenna, consisting of a voltage source and a noiseless resistor, together with a load resistor. The noise of the resistor is modelled as noise voltage. Assuming a received signal power S, the voltage of the voltage source can be expressed as $V_S = \sqrt{4 \cdot R_\mathrm{A} \cdot S}$. The noise power $N = \mathrm{k} \cdot T \cdot BW$ can be translated into a noise voltage of $V_N = \sqrt{4 \cdot R_\mathrm{A} \cdot \mathrm{k} \cdot T \cdot BW}$. The power transferred to the load can be calculated as:

$$P_\mathrm{L} = V_S^2 \frac{R_\mathrm{L}}{(R_\mathrm{A} + R_\mathrm{L})^2} = 4 \cdot R_\mathrm{A} \cdot S \frac{R_\mathrm{L}}{(R_\mathrm{A} + R_\mathrm{L})^2} \tag{6.1}$$

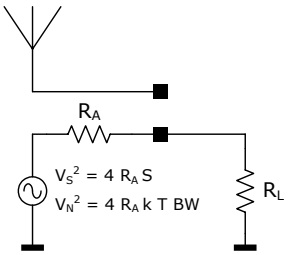


Figure 6.1: Available power at the antenna.

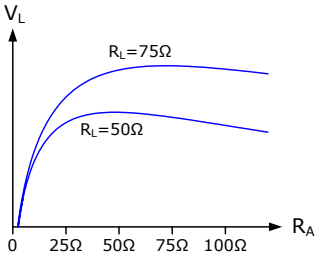


Figure 6.2: Available voltage at the load versus antenna impedance for two different load impedances.

By analyzing equation 6.1, one might suspect that the maximum is at $R_\mathrm{A} = R_\mathrm{L}$. When the load resistor R_L is equal to the source resistor R_A, then the power transferred to R_L is equal to the signal power from the antenna. Typically, a matching network is used to transform R_L to be equal to R_A in order to transfer the maximum power to the load. Because of the additional noise of the load resistor, the noise figure is limited to at least 3 dB.

As already mentioned, in some situations it is not maximum power that is required but rather maximum voltage. In this case, matching does not lead to an optimum. When the circuit is matched, the load voltage is only half the source voltage. The plot in Figure 6.2, which represents equation 6.1, shows that the higher the load resistance, the higher the transferred voltage. Additionally, the resistance of the antenna should be as close to the load resistance as possible (if the load resistance is fixed). To sum up, the conditions for maximum voltage transfer can be described as follows:

1. The load resistance should be as high as possible. For the same value of R_A, the $R_\mathrm{L} = 75\,\Omega$ curve is always better than the $R_\mathrm{L} = 50\,\Omega$ curve.

2. Antenna impedance should be matched to the LNA input (local optimum).

In matching networks, this does not always mean that the noise figure is at its minimum, although the maximum power is transferred. As already mentioned, the best achievable noise figure for a matched circuit is 3 dB. If the circuit is not matched, the

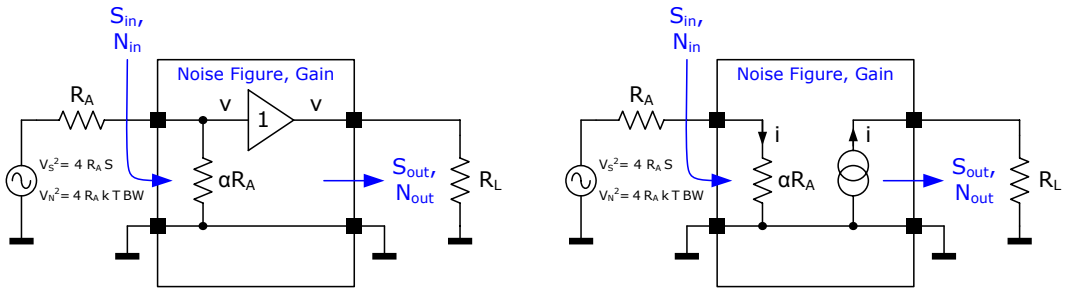


Figure 6.3: Noise figure when the antenna is loaded with αR_A and the voltage (left) or the current (right) is observed.

noise figure can be lower. The noise figure can be calculated [55] with equation 6.2:

$$NF = \frac{total\ \ output\ \ noise\ \ power}{output\ \ noise\ \ due\ \ to\ \ input\ \ source} = \frac{N_{\mathrm{out\_tot}}}{N_{\mathrm{out\_in}}} \tag{6.2}$$

If the antenna is loaded with αR_A and if the voltage is observed (see left side of Figure 6.3), the output noise due to the input and the total output noise can be expressed as:

$$N_{\mathrm{out\_in}} = \frac{\left(\sqrt{4 \cdot R_\mathrm{A} \cdot \mathrm{k} \cdot T \cdot BW}\,\frac{\alpha R_\mathrm{A}}{\alpha R_\mathrm{A} + R_\mathrm{A}}\right)^2}{R_\mathrm{L}} \tag{6.3}$$

$$N_{\mathrm{out\_tot}} = N_{\mathrm{out\_in}} + \frac{\left(\sqrt{4 \cdot \alpha \cdot R_\mathrm{A} \cdot \mathrm{k} \cdot T \cdot BW}\,\frac{R_\mathrm{A}}{\alpha R_\mathrm{A} + R_\mathrm{A}}\right)^2}{R_\mathrm{L}} \tag{6.4}$$

Considering equations 6.3 and 6.4, the noise figure can be determined with the help of equation 6.2 to:

$$NF = \frac{4 \cdot R_\mathrm{A} \cdot \mathrm{k} \cdot T \cdot BW\left(\frac{\alpha^2}{(1+\alpha)^2} + \frac{\alpha}{(1+\alpha)^2}\right)}{4 \cdot R_\mathrm{A} \cdot \mathrm{k} \cdot T \cdot BW\,\frac{\alpha^2}{(1+\alpha)^2}} = \frac{1+\alpha}{\alpha} \tag{6.5}$$

If the circuit is matched ($\alpha = 1$), the noise figure is limited to 2 (3 dB). But when the antenna is not loaded ($\alpha = \infty$), the noise figure can reach the lowest possible value of 1 (0 dB). If the current of the antenna is observed (see right side of Figure 6.3), the output noise due to the input and the total output noise can be calculated as:

$$N_{\mathrm{out\_in}} = \left(\frac{\sqrt{4 \cdot R_\mathrm{A} \cdot \mathrm{k} \cdot T \cdot BW}}{\alpha R_\mathrm{A} + R_\mathrm{A}}\right)^2 \cdot R_\mathrm{L} \tag{6.6}$$

$$N_{\mathrm{out\_tot}} = N_{\mathrm{out\_in}} + \left(\frac{\sqrt{4 \cdot \alpha \cdot R_\mathrm{A} \cdot \mathrm{k} \cdot T \cdot BW}}{\alpha R_\mathrm{A} + R_\mathrm{A}}\right)^2 \cdot R_\mathrm{L} \tag{6.7}$$

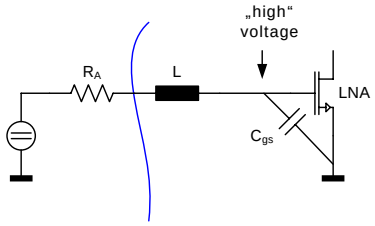


Figure 6.4: Series inductor in front of an LNA (represented by a simple transistor).

Considering equations 6.6 and 6.7, the noise figure can be calculated as:

$$NF = \frac{4 \cdot \mathrm{k} \cdot T \cdot BW(\frac{1}{(1+\alpha)^2} + \frac{\alpha}{(1+\alpha)^2})}{4 \cdot \mathrm{k} \cdot T \cdot BW \frac{1}{(1+\alpha)^2}} = \frac{1+\alpha}{1} \tag{6.8}$$

Here again, the noise figure is limited to 2 (3 dB) if the circuit is matched ($\alpha = 1$). But if the antenna is shorted ($\alpha = 0$), the noise figure can reach the lowest possible value of 1 (0 dB).

A method for increasing the voltage at the input of the LNA considerably is to build a resonance circuit for the desired frequency. In a common source amplifier, the input consists of the gate of a transistor. So the input is almost purely capacitive and the LNA does not absorb any power. With a series inductor connected to the input of the LNA (see Figure 6.4), the circuit can be brought into resonance, and the input impedance is equal to the parasitic resistance of the inductor and the transistor, which is zero for ideal devices. In this way, the antenna is shorted. The voltage at the LNA input can be calculated [55] using equation 6.9.

$$\underline{i} = \frac{V_S}{R_\mathrm{A}} \quad \rightarrow \quad |\underline{v}_\mathrm{LNA}| = \frac{V_S}{\omega C R_\mathrm{A}} \tag{6.9}$$

Hence the voltage at the LNA can be very high. For example, for $C_\mathrm{gs} = 150\,\mathrm{fF}$, $f = 2.1\,\mathrm{GHz}$, and $R_\mathrm{A} = 50\,\Omega$, the voltage gain of the resonance circuit is 20 dB.

However, the power is not absorbed. Instead, the whole power is reflected from the LNA. If there are any discontinuities in the wave guide between the antenna and the LNA, then the reflected power is reflected again and the original signal is disturbed [55]. But although no energy is absorbed, the voltage at the LNA input is very high.

A state-of-the-art approach tries to make the input impedance of the LNA resistive and match the antenna to this impedance. There exist several ways to achieve a certain resistive input impedance in an LNA [62]. The reactive components of the impedance can then be tuned out applying an LC network.

- Resistive termination: The straightforward approach to achieving a certain resistive input impedance is to simply connect a resistor between the input terminals. The drawback of this approach is that the resistor itself adds thermal noise to the input signal, and it attenuates the signal by a factor of two.

- Common gate Amplifier: As the input impedance of a common gate amplifier is $1/g_{\mathrm{m}}$, it can be dimensioned to exhibit the desired value.
- Feedback circuit: In general, with a certain feedback circuit the resistive part of the input impedance can be brought to the desired value. One example of a feedback circuit is inductive source degeneration: If an inductor is added in the source, then the input impedance exhibits an resisitive part. This resisitive part can be matched to any desired value using reactive components.

The commonly used technique of using a feedback circuit has one big advantage: As this method does not really insert a load resistor, but generates the resistive behaviour through a feedback loop, the noise figure can be below 3 dB.

6.1.2 Matching to the Losses of a Resonance Circuit

Parts of the following chapter was taken from [1, 7] (own publications).

The input impedance of the presented transceiver has been chosen to be 50 Ω. This work presents a network that produces a resonance at the LNA input and additionally the antenna is matched so that no energy is reflected. Unfortunately, the on-chip resonance circuit is very lossy. The highest voltage amplification of a resonance circuit is gained by pumping as much power into the circuit as possible. This can be done by matching the antenna to the losses of this network, which is the core idea of this approach. So it is a combination of power matching and a resonance circuit. The aim of the circuit is to provide a desired input impedance matched with an antenna on the one hand, and to generate a resonance gain on the other hand. In Figure 6.7 and Figure 6.8 the implementation of the whole matching network for the 2.1 GHz and for the 2.4 GHz variant is shown.

As the input of the LNA is capacitive, an inductor is required to generate the resonance. The applied on-chip inductor only has a quality (Q) factor of around 6, which is a typical value for a pure CMOS process without RF extension. The on-chip coil has a parasitic resistance in series of 14 Ω. Simulations showed that this circuit can be equivalently represented as a parallel circuit of an ideal coil with 5 nH and a parallel resistor with 630 Ω at the desired frequency. The losses of the resonance circuit are dominated by the parasitic resistance of the inductor. The capacitance of the LNA input (C_{LNA}) is assumed to be 105 fF, a parasitic capacitance of 350 fF is caused by parasitics of the coil. Hence another capacitor of 650 fF is required to get a total capacitance of 1.15 pF which results in a resonance circuit at 2.1 GHz together with the 5 nH inductance. A digitally controlled varactor bank C_{tuneLNA} is used to tune the resonant frequency.

First the resistance of 630 Ω is transformed to about 125 Ω by making use of a capacitive voltage divider consisting mainly of C_{series} and C_{ESD}. More details are shown in Figure 6.5. The capacitor between the LNA and the RX/TX switch in combination with a part of the capacitance of the ESD protection makes up the capacitive voltage

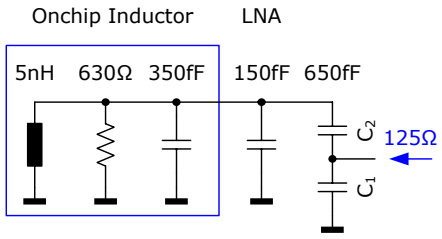


Figure 6.5: Parallel equivalent circuit of on-chip inductor together with capacitive voltage divider.

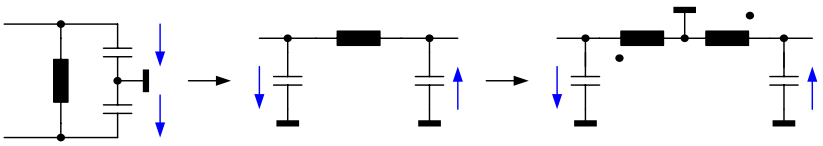


Figure 6.6: Conversion to differential signal.

divider used for impedance transformation. Another on-chip inductor L_{int} is used to compensate the remaining C_{ESD}. C_{tuneESD} is a bank of switched capacitors and can be used to fine-tune the circuit's process variations. The best digital setting of C_{tuneLNA} (codeword A) and of C_{tuneESD} (codeword B) can be found automatically by optimizing the RSSI signal provided by the limiting amplifier. The measured input impedance for different settings of A and B can be found in Figure 6.9.

The impedance of about 125 Ω is reduced to about 100 Ω due to additional losses caused by the ESD protection circuit and the second inductor L_{int}. The remaining resistance of 100 Ω is then transformed to 50 Ω by making use of the inductive bond-wire and an external inductor L_{ext}, which can be integrated into the antenna.

To allow the use of a differential LNA, a single-ended to differential conversion has to be performed by making use of the principle shown in Figure 6.6. The coil for this conversion is the 5 nH coil in Figure 6.5. The mutual inductance allows to feed the DC biasing voltage to the input transistors of the LNA.

In the first 2.1 GHz implementation the RX/TX switch was in series with the capacitor acting as voltage divider. In the second version the RX/TX switch was connected to ground to minimize the losses caused by the current flowing into the bulk substrate during reception (see Figure 6.7 and Figure 6.8). The resulting matching network provides a voltage gain of 10 dB and a noise figure slightly higher than 3 dB at an input resistance of 50 Ω. The advantage of this approach is that this resonance circuit can be easily connected to the power amplifier in case of transmit mode. In this situation, the power amplifier pumps the energy into resonance circuit and the energy is mostly radiated by the antenna. In transmit mode the transistor acting as TX/RX switch is turned off. With a different setting of C_{tuneESD}, L_{int} can be brought into resonance. C_{PA} is the coupling capacitor of the power amplifier. In this mode the power amplifier sees a purely resistive load of about 100 Ω.

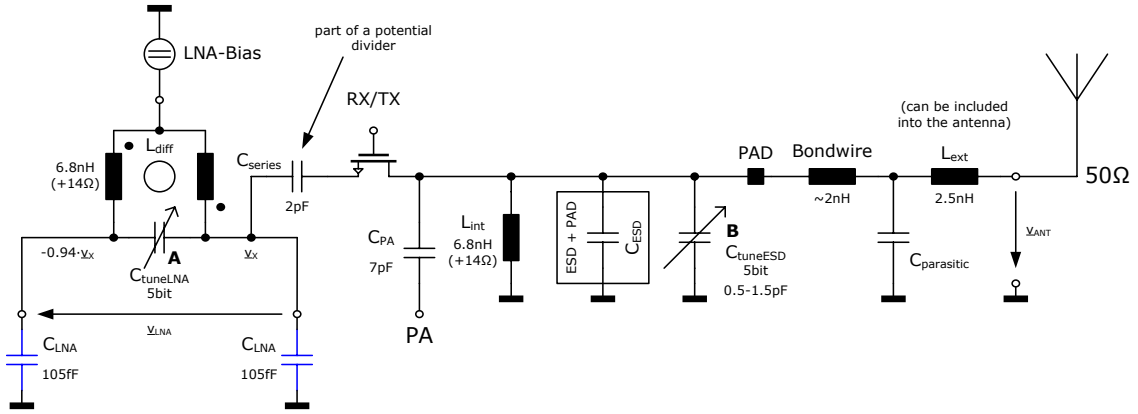


Figure 6.7: Implementation of the matching network (2.1 GHz variant).

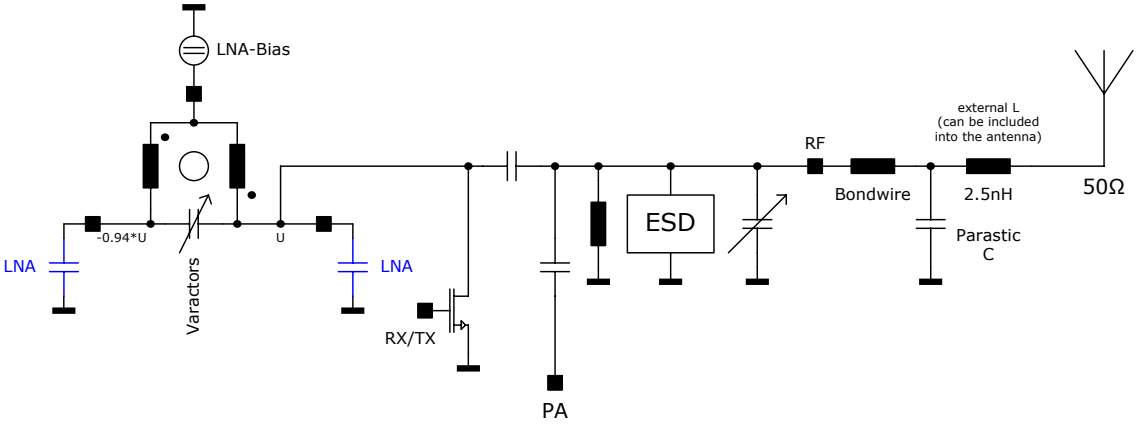


Figure 6.8: Implementation of the matching network (2.4 GHz variant).

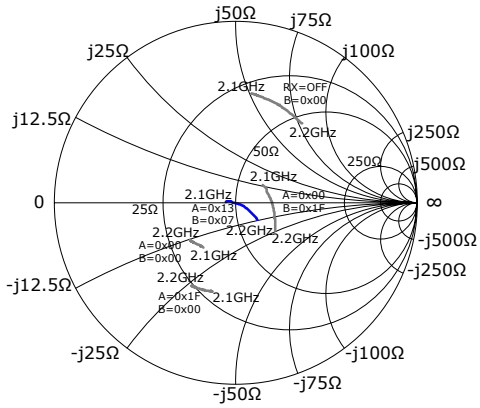


Figure 6.9: Measurement of the input impedance with different digital settings A and B.

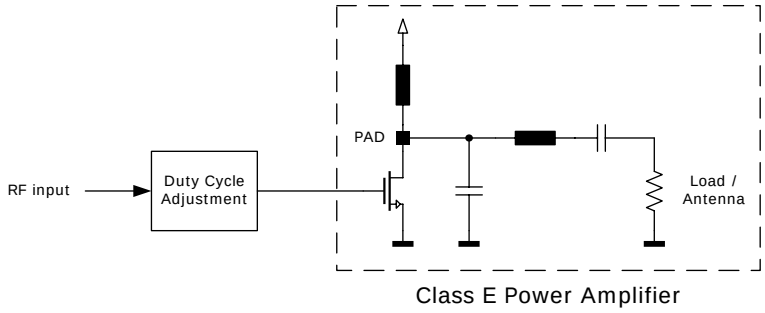


Figure 6.10: Basic principle of the class E power amplifier.

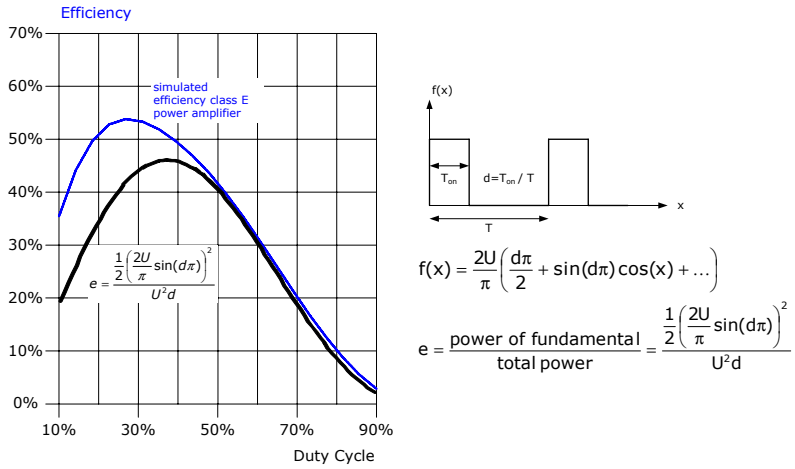


Figure 6.11: Simulated efficiency of a open drain power amplifier over duty cycle.

6.2 Class E RF Power Amplifier with Duty Cycle Adjustment

The basic principle of a class E power amplifier, which was presented in [97], with external matching network is shown in Figure 6.10. The duty cycle of such an open drain power amplifier input signal has a deep impact on the efficiency. The efficiency of the PA over duty cycle of the input signal is drawn in Figure 6.11. The maximum efficiency can be found at a duty cycle of about 20-30%. A state-of-the-art solution to achieve such an ideal duty cycle is illustrated in Figure 6.12: If the VCO or BAW oscillator operates at a higher frequency than the carrier frequency, the signal is divided. Then the duty cycle can be adjusted by a simple logic. For example, in the case of a master-slave flip flop (division ratio 2) with an AND gate. The conjunction of the two 90° shifted signals of the master and slave latch realizes a 25% signal for the power amplifier. Another possibility to achieve the desired duty cycle would be a division of the VCO Signal by the factor of 3. The output signal of the divider (with a division ratio of 3) has 33% duty cycle. Generally there exist two problems with state-of-the-art solutions: How can the 25% signal be generated if the VCO operates at the carrier frequency (for example in the proposed transceiver architecture)? The

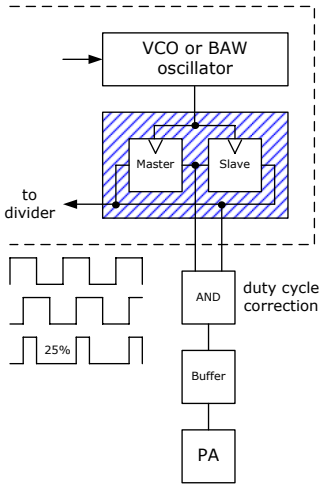


Figure 6.12: State-of-the-art duty cycle generation.

second problem is that for some solutions (for example an asymmetric inverter) the duty cycle can change unacceptably taking process variation into account. This is why a circuit which can generate arbitrary duty cycles will be shown. The circuit is placed in front of the power amplifier transistor (see Figure 6.10). The principle of the circuit for duty cycle adjustment is very simple: Since the duty cycle of a squared wave signal is proportional to its DC value, the duty cycle can be measured by a simple low pass. So, for example, an operational amplifier can control the PMOS of an inverter (see Figure 6.13). In many cases an inverter chain is used to pre-amplify the signal for driving the PA. In such a case no additional current consuming devices are needed. There exist many possible solutions for the controller - in the simplest case it could be an operational amplifier - but it would be more advantageous to control the current through the inverter directly. The target value for the controller, in the proposed example $(1 - duty\ cycle) \cdot V_{\mathrm{DD}}$, can be generated by a voltage divider. So the desired duty cycle can be changed ad lib (for example if more output power is required). The ideal signals A, B, C, D, and E of the circuit can be found in Figure 6.14.

Figure 6.15 shows the corner analyses of the output signal (duty cycle 33%, $R_2 = 2R_1$), under process variation (fast, nominal, slow), temperature variation (-40°C, 0°C, and 125°C), and supply variation (1.5 V, 1.2 V and 1 V) in a 0.13 µm process. Figure 6.16 (top) shows the settling process for different input duty cycles and in Figure 6.16 (bottom) the corresponding control voltage (of the PMOS transistor) and output signal (no change of duty cycle) is shown. The proposed circuit was considered not to be used in the e-Cubes transmitter after the decision for low output power was made. The output power can be approximated with equation 6.10 [62].

$$P_{\mathrm{out}} \approx 0.577 \frac{V_{\mathrm{DD}}^2}{R_{\mathrm{load}}} \tag{6.10}$$

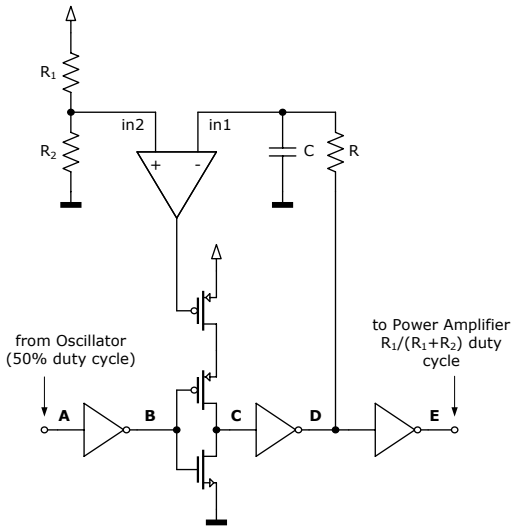


Figure 6.13: Basic principle of duty cycle adjustment circuit.

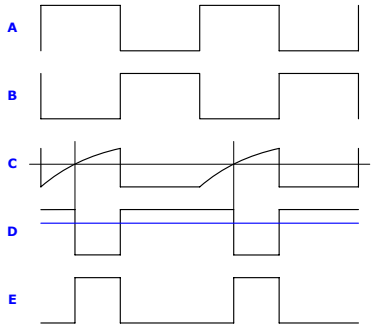


Figure 6.14: Signals A, B, C, D, and E of circuit Figure 6.13 over time.

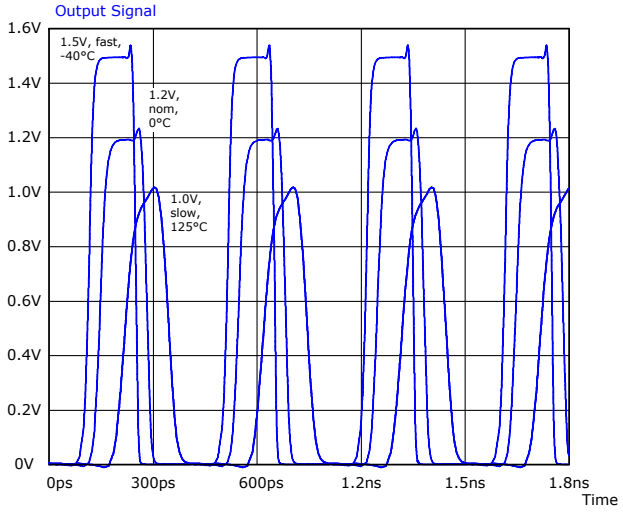


Figure 6.15: Output signal over variation of process, temperature, and supply voltage.

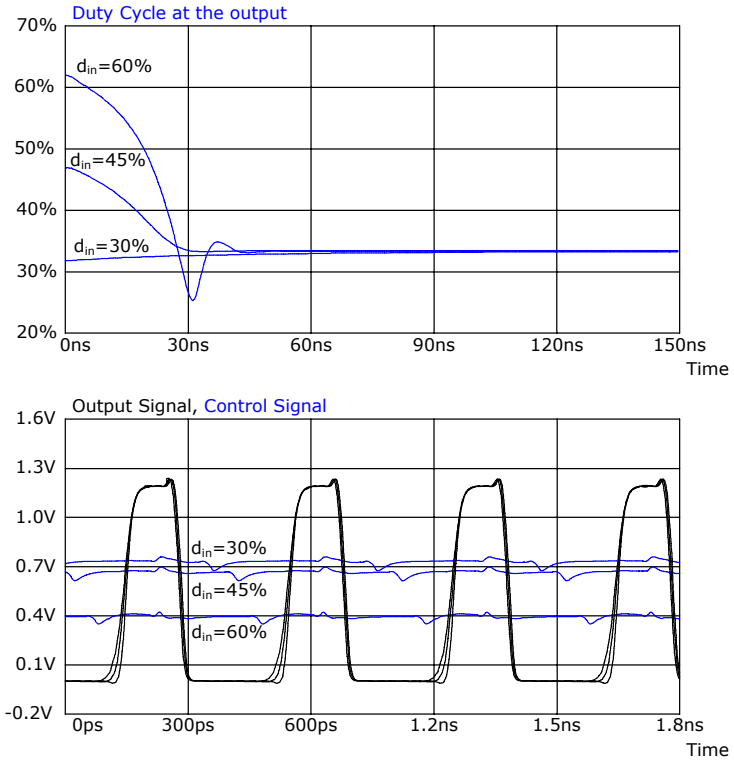


Figure 6.16: Settling process (top), output signal and control signal (bottom) with different input duty cycles.

For an output power $P_{\mathrm{out}} = 0\,\mathrm{dBm}$ and for a supply voltage of $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, the desired load for the power amplifier should be about $R_{\mathrm{load}} = 1300\,\Omega$. As already shown in Figure 6.5 in chapter 6.1.2 on page 119, the equivalent circuit of an on-chip inductor exhibits a parasitic resistor of about 630 Ω connected in parallel to the ideal device. Such an inductor is needed in parallel to the power amplifier transistor to provide the DC current and to compensate the capacitance at this node. So this inductor is in parallel to the load impedance. Hence, for such a high load impedance, the losses of an on-chip matching network are too high. Because of this, the class C power amplifier introduced in the next chapter was implemented in the transmitter. But the proposed duty cycle adjustment circuit together with an class E power amplifier was implemented on a test chip.

6.3 Class C RF Power Amplifier with Non-Overlapping Clock Generation

A simple inverter is used as a switched power amplifier in the proposed transmitter. In an inverter, which can be used for small output power (1 dBm), the cross-current through the N and P channel transistors contributes a considerable part to the total

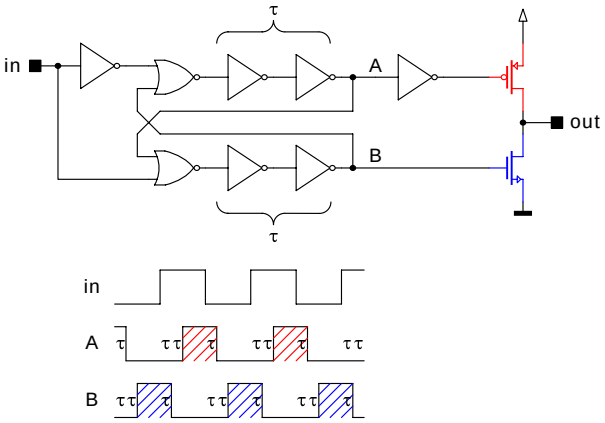


Figure 6.17: State-of-the-art non-overlapping clock generation.

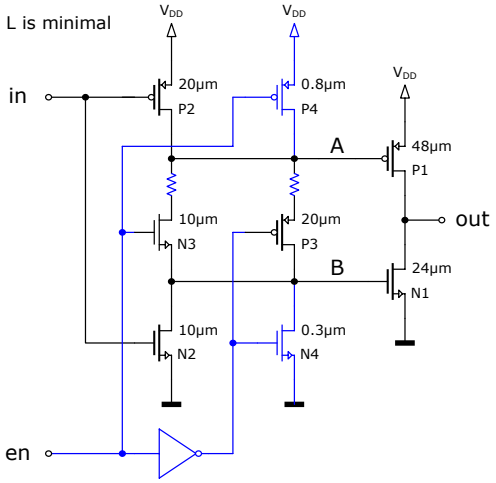


Figure 6.18: Circuit of the non-overlapping clock tristate buffer used as power amplifier in the transmitter.

current consumption. The power consumption of such an inverter can be reduced by an intelligent control signal at the input of the transistors. The goal is to switch one transistor off before the other begins to conduct (break before make).

Figure 6.17 shows a state-of-the-art solution for non-overlapping clock generation, which requires several gates to generate the required delay such that the conducting transistor is always turned off, before the other one is turned on. The disadvantage of such a solution is that for high frequency applications the power consumption of the non-overlapping clock generation is higher than the power saving due to the concept of break before make.

In Figure 6.18 a non-overlapping clock tristate buffer is shown. In receive mode the enable signal (en) is set to low and the transistors N3 and P3 are turned off. Hence, node A is connected to V_{DD} via transistor P4 and node B is connected to ground via transistor N4 respectively. So no current flows through the transistors P1

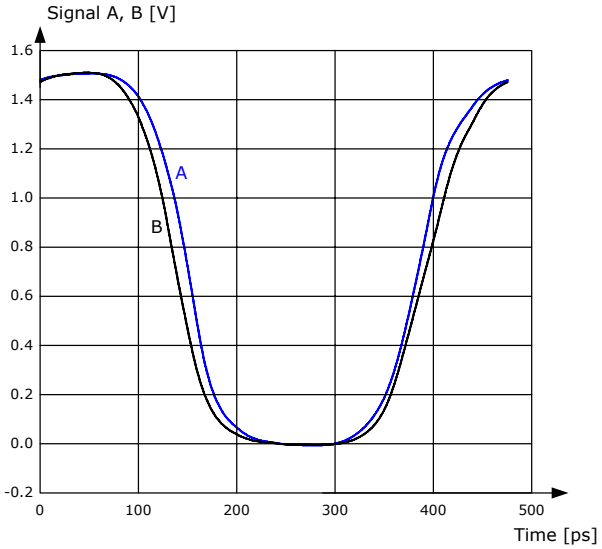


Figure 6.19: Time plot of the gate control signals of the power amplifier.

and N1 and the buffer is in its high impedance state. The width of transistors N4 and P4 can be very small in order to avoid any additional capacitive load at nodes A and B. If the buffer is active (enable is set to high), transistors N3 and P3 are on. This results in a connection between node A and node B. So N2 and P2 can operate as a common inverter driving the gates of N1 and P1. The output of the tristate buffer now equals the input. If the input changes from high to low transistor P2 is switched on and current flows into node A. Node B is charged from node A via the transmission gate P3 and N3. Because of the finite conductivity of transistors P3 and N3 (illustrated as an additional resistor in Figure 6.18) the charging of node B is delayed and therefore it is guaranteed that transistor P1 is turned off before transistor N1 is on. For discharging nodes A and B, a similar effect can be observed. Figure 6.19 shows the time responses of node A and node B at 2.1 GHz.

The PA is supplied with 1.5 V and the current consumption is about 3.5 mA, which can be split into 2.7 mA caused by the second stage (N1 and P1) and 0.8 mA caused by the first stage. The output power at nominal conditions is 1.7 dBm. The measured output power and the measured current consumption of the transceiver in transmit mode over temperature is illustrated in Figure 6.20. From these results, the efficiency can be calculated to 36.5%, considering only the second stage, and to 28.2% including the first stage respectively. The input capacitance of the second stage is 97 fF. Hence, theoretically, no input power is needed to drive the PA. To load the input capacitance from 0 V to 1.5 V in every period of the RF carrier, a power of 0.46 mW is required. This is what an ideal inverter without any crosscurrent would need for driving the gates of the PA. Under this assumption, the power added efficiency (PAE) can be determined to 25.1% and the power gain to 5 dB.

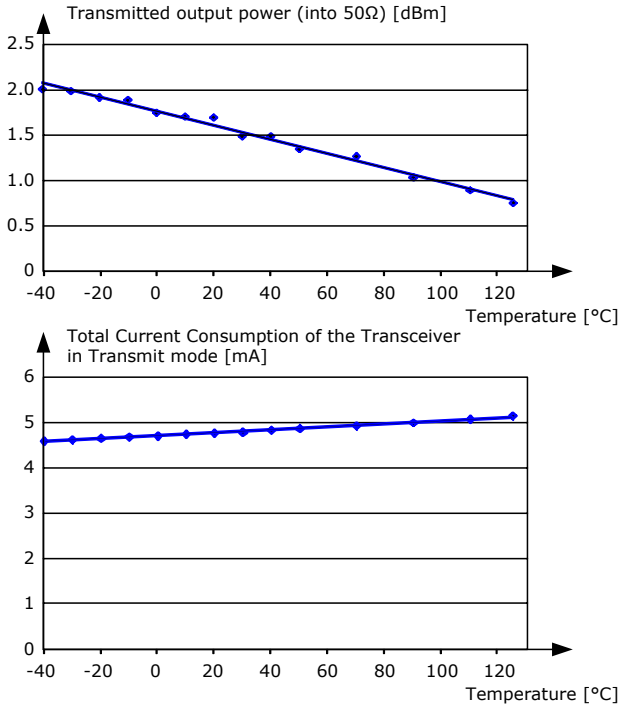


Figure 6.20: Measured output power and measured current consumption of the transceiver in transmit mode versus temperature.

6.4 Figure-of-Merit (FoM) and Comparison with State-of-the-Art

The losses in the matching network have a deep impact on the performance of the power amplifier. Many PAs use external matching components, which results in increased efficiency. The proposed PA only makes use of internal devices and additionally the receiver input causes some losses due to the non-ideal RX/TX switch. On the other hand, a linear PA is much more challenging in terms of achieving efficiency. In Table 6.1 a short comparison with similar PAs is given. The PA presented in [102] (last row of Table 6.1) is a pure transmitter matching which make use of external components. Additionally, it is a class E amplifier operating at a lower frequency. But ultimately, the PA presented is not much worse than this example. The PA proposed in [107] (=[Chee05]) is a differential solution where the output of the PA transistors is directly connected to the passive mixer. Due to the low supply voltage, no impedance matching is needed which allows the high efficiency.

Reference	IC Technology	PA Application	fc	Supply Voltage	Current Consum.	Power Consum.	Transmitted Power		Efficiency	PAE
			[GHz]	[V]	[mA]	[mW]	[mW]	[dBm]	[%]	[%]
[This Work]	**CMOS 0.13µm**	**WSN (eCubes) - *Class C***	**2.1**[1]	**1.5**	**2.7**	**4.05**	**1.48**	**1.7**	**36.5**	**25.1**
[Otis05]	CMOS 0.13µm	WSN (PicoRadio) - LPA	1.9	0.9-1.3	-		0.38	-4.2	27.5	-
[Yuan09]	CMOS 0.18µm	UWB - DA	3.1-4.5	1.8	9.5	17	0.05	-13	0.3	-
[Chee05]	CMOS 0.13µm	WSN	1.9	0.28	-	-	1	0	32[2]	-
[Huang2010]	CMOS 90nm	WSN / WBAN	2.4	1	3.14	3.14	1	0.0	32	-
[Cook06]	CMOS 0.13µm	WSN	2.34	0.4	-	-	0.32	-4.9	44	-
[Staszewski05]	CMOS 90nm	GSM/EDGE - Class E PA	0.824	1.2	6	7.20	3.98	6.0	55.3	-

[1] Oscillator was also tested with 2.45GHz BAW resonator, values are given for 2.1GHz BAW.
[2] These values are calculated.

[Otis05] = [89] [Cook06] = [105]	[Staszewski05] = [102] [Chee05] = [107]	[Yuan09] = [103] [Huang2010] = [109]

Table 6.1: Comparison of proposed PA with others.

6.5 Conclusion

A new on-chip network was proposed: The almost purely reactive LNA is part of a resonance circuit, which is matched to the 50 Ω antenna to obtain the maximum amplitude of oscillation. The highest voltage amplification of a resonance circuit is gained by pumping as much power into the circuit as possible. This can be done by matching the antenna to the losses of this network achieving a voltage gain of around 10 dB at a noise figure of slightly higher than 3 dB. The advantage of this approach is that this resonance circuit can easily be connected to the power amplifier in the case of transmit mode. In this situation, the power amplifier pumps the energy into the resonance circuit and the energy is mostly radiated by the antenna.

The PA is supplied with 1.5 V and the current consumption is about 3.5 mA, which can be split into 2.7 mA caused by the second stage and 0.8 mA caused by the first stage. The output power at nominal conditions is 1.7 dBm. From these results the efficiency can be calculated to be 36.5%, considering only the second stage, and to be 28.2% including the first stage respectively.

Because only low output power was required, a simple inverter was used as power amplifier. In such an inverter, the cross-current through the N and P channel transistors contributes a considerable part of the total current consumption. The power consumption of such an inverter can be reduced by an intelligent control signal at the input of the transistors. The goal is to switch one transistor off before the other begins to conduct (break before make). The circuitry offers a very simple and small non-overlapping clock generation for a tristate buffer used in RF applications.

It was shown that a class E power amplifier is not useful for a low output power, because the losses of an on-chip matching network are too high. Nevertheless some investigations have been made: The duty cycle of an open drain class E power amplifier input signal has a deep impact on efficiency. The maximum efficiency can be found at a duty cycle of about 20-30%. A state-of-the-art solution to achieve such ideal duty cycle is using an oscillator operating at a higher frequency and dividing

its output signal with flip flops. The duty cycle can then be adjusted by a simple logic - for example, the conjunction of the two 90° shifted signals of the master and slave latch realizes a 25% signal for the power amplifier. The proposed circuitry can provide arbitrary duty cycles and there is no need for a higher frequency than the output frequency and this increases the efficiency significantly.

7 Conclusion and Research Summary

In-Tire Pressure Monitoring and the BAW based Transmitter

Chapter 1 and Chapter 2:
State-of-the-art Tire Pressure Monitoring Systems (TPMS) are wireless sensor nodes mounted on the rim. Attaching the node on the inner liner of a tire allows the sensing of important technical parameters and enables the storage of additional information, such as date of manufacture and type of the tire (winter or summer tire). The challenges are high: The maximum weight of the sensor is limited to a few grams, robustness is required, the node size is limited and finally a long power supply lifetime must be achieved.

It was shown that a system-in-package (SiP) can be advantageous in terms of price compared to a system-on-chip (SoC) implementation, although the BAW technology is compatible with a standard integrated circuit (IC) process and it is possible to integrate BAW resonators above an IC [74]. The reason for this is the relatively low yield of the BAW resonators caused by the process variation of the resonance frequency. Since the BAW resonator is very small, the costs of the stand-alone resonator are negligible. But if the resonator is integrated on top of the relatively large and expensive transceiver ASIC, the overall yield is reduced dramatically. Exploiting BAW resonators, the use of a bulky and shock-sensitive quartz crystal and a PLL can be avoided. This makes the system more robust and radically reduces the start-up time from a few ms as in state-of-the-art quartz crystal oscillator based systems to 2 µs.

A 3D chip stack was developed in the project by project partners to provide best compactness, lowest volume, and highest robustness. Design issues when using this integration technique were considered. It was shown that an optimized structure where three round TSVs are placed at the corners of an equal-sided triangle can significantly reduce losses into the substrate.

The Shannon-Hartley theorem can help to find the optimum transmitted signal power. It was shown that for the proposed transmitter implementation, a data rate in the range of 100 kBit/s is sufficient. A further increase would not save much more power. At this operating point, the transmit power is in the range of 0 dBm and the DR/BW indicates that this is the limit where a low complexity modulation can be used instead of complex modulation. Of course, the amount of transferred bits and the required distance between transmitter and receiver have an deep impact on this operating point. Furthermore, it was shown that the implementation of this novel

transmitter is competitive with other high performance transmitters.

BAW oscillator

Chapter 3, Chapter 4, and Chapter 4.5:
A quartz crystal oscillator always tends to operate very close to the series resonance frequency, which is the internal quartz crystal frequency. Then the resonance frequency of the oscillator is independent from packaging and mounting [55]. Additionally, the transconductance g_{m} has only a minor impact on the resonance frequency. For a high frequency BAW resonator, the inductance of the interconnection between resonator and oscillator (for instance the bondwire) can have the same impact as parasitic capacitances. For example, an inductance of 1 nH in series to the resonator already causes a shift in the series resonance frequency of about 6300 ppm. The required transconductance g_{m} of a one-transistor oscillator has to be very high for high frequencies. Hence the current consumption is quite high. Because of this, the proposed BAW oscillator consists of two gain stages. The use of two gain stages while also operating close to the series resonance frequency implies the risk of parasitic oscillation. Hence the proposed oscillator topology oscillates close to the parallel resonance frequency. The oscillator core consumes 800 µA, and a further 80 µA are needed for biasing. The start-up time is lower than 2 µs and the phase noise is -112 dBc/Hz at a distance of 100 kHz from the carrier.

The proposed oscillator is tunable over a frequency range of about 10 MHz to enable temperature compensation and process compensation. The tuning is achieved by connecting digitally controlled capacitors of about 1 pF in parallel to the BAW resonator. The remaining frequency deviation after applying the temperature compensation algorithm is lower than ±150ppm.

In addition to the capacitor bank, the BAW can be tuned with variable DC biasing. This can be used for modulation. The relation between frequency and DC biasing voltage is linear over a wide range with a typical slope of about 40 kHz/V.

Asynchronous Dividers

Chapter 5:
A new kind of asynchronous 1/2/3 divider was presented [15]. This divider comprises two ideal, well-known counters: an ideal divider by 2 [47] and an ideal divider by 3 [46]. The combination of these two circuits makes it possible the ability to change the division ratios between 2 and 3. The divider can be used for instance in a fractional divider as dual modulus prescaler. If the 1/2/3 counter is used as an integer divider in a PLL, a duty cycle correction can be done to increase the efficiency of the open drain power amplifier. A state-of-the-art (synchronous) solution for a 2/3 dual modulus

divider needs 2 flip flops and possibly (if not included in the flip flops) some logic. This is why the power consumption is reduced by half.

A 1.5 frequency divider, based on the divider by 3 [46], can be used to overcome several issues. The main issue is the isolation between the BAW oscillator (or VCO, or quartz crystal oscillator in a PLL) and other building blocks (e.g. the power amplifier). By dividing the reference signal by the factor of 1.5, the harmonics of the clock signal and the harmonics of the output signal do not occur at the same frequency.

Matching Network and Power Amplifier

Chapter 6:
A new on-chip network was proposed: The almost purely reactive LNA is part of a resonance circuit, which is matched to the 50 Ω antenna to obtain the maximum amplitude of oscillation. The highest voltage amplification of a resonance circuit is gained by pumping as much power into the circuit as possible. This can be done by matching the antenna to the losses of this network achieving a voltage gain of around 10 dB at a noise figure of slightly higher than 3 dB. The advantage of this approach is that this resonance circuit can easily be connected to the power amplifier in the case of transmit mode. In this situation, the power amplifier pumps the energy into the resonance circuit and the energy is mostly radiated by the antenna.

The PA is supplied with 1.5 V and the current consumption is about 3.5 mA, which can be split into 2.7 mA caused by the second stage and 0.8 mA caused by the first stage. The output power at nominal conditions is 1.7 dBm. From these results the efficiency can be calculated to be 36.5%, considering only the second stage, and to be 28.2% including the first stage respectively.

Because only low output power was required, a simple inverter was used as power amplifier. In such an inverter the cross-current through the N and P channel transistors contributes a considerable part of the total current consumption. The power consumption of such an inverter can be reduced by an intelligent control signal at the input of the transistors. The goal is to switch one transistor off before the other begins to conduct (break before make). The circuitry offers a very simple and small non-overlapping clock generation for a tristate buffer used in RF applications.

It was shown that a class E power amplifier is not useful for a low output power, because the losses of an on-chip matching network are too high. Nevertheless some investigations were made: The duty cycle of an open drain class E power amplifier input signal has a deep impact on efficiency. The maximum efficiency can be found at a duty cycle of about 20-30%. A state-of-the-art solution achieving such an ideal duty cycle is using an oscillator operating at a higher frequency and dividing its output signal with flip flops. The duty cycle can then be adjusted by a simple logic - for example the conjunction of the two 90° shifted signals of the master and slave latch realizes a 25% signal for the power amplifier. The proposed circuitry can provide

arbitrary duty cycles and there is no need for a higher frequency than the output frequency; this significantly increases efficiency.

Conclusion and Outlook

The newly developed analog circuitry of the asynchronous dividers, the power amplifier and the matching network can be applied in practical implementations of receivers or transmitters. They can help to improve performance and to decrease current consumption. It was shown that a transmitter based on a BAW resonator is quite challenging due to the frequency variations, but possible. Such a solution provides several advantages, such as integration capability and robustness. The required frequency accuracy depends on the application. There exist many applications with relaxed frequency accuracy, and therefore discrete SAW based transmitters have been in widespread use [43]. The presented work applies this simple transmitter architecture in combination with the advantages provided by the IC technology. However, the performance of a PLL based system cannot be reached. Some further works will show which combination of a PLL, a BAW oscillator, a silicon clock reference, or a quartz crystal is most advantageous for in-tire TPMS.

Own Publications

[1] M. **Flatscher**, M. Dielacher, T. Herndl, T. Lentsch, R. Matischek, J. Prainsack, W. Pribyl, H. Theuss, and W. Weber, "A Bulk Acoustic Wave (BAW) Based Transceiver for an In-Tire-Pressure Monitoring Sensor Node," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 1, pp. 167–177, Jan. 2010.

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