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Towards Understanding and Controlling the Device Characteristics of OTFTs

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Second star to the right

…and straight on 'til morning.

James Tiberius Kirk
[*Star Trek VI: The Undiscovered Country*]

Abstract

In the present work, pentacene based organic thin-film transistors (OTFTs) with different layers applied to the interface between the gate-dielectric and the organic semiconductor have been studied. In addition to the electrical characterization, complementary techniques like contact angle measurements, atomic force microscopy and x-ray reflectivity are used to characterize the growth of the pentacene thin films in the course of various collaborations.

In the first part of this work, photoreactive polymers have been used to modify two of the most important device parameters in OTFTs – namely the charge carrier mobility and the threshold voltage. By a posteriori illuminating the devices with ultraviolet (UV)-light the threshold voltage could be shifted over a broad range. This paved the way for a straightforward realization of depletion-load inverters. Illumination of the photoreactive layers prior to the pentacene deposition allowed controlling the growth of the pentacene layer und thus tuning the room temperature mobility. It was also found to influence the temperature dependence of the device characteristics modifying the activation energy for charge carrier hopping.

In the second part of this thesis the focus shifts entirely to the impact of temperature on the device parameters: Studies include the investigation of the impact of a number of interface modification schemes in a temperature range from 25 to 400 K. Charge carrier mobilities are extracted from these measurements and are interpreted in the context of the multiple-trapping and thermal release model. Additionally the temperature dependence of the contact resistance and of the threshold voltage are investigated. The devices studied include top-contact shadow mask evaporated TFTs with channel lengths in the order of tens of micrometers and bottom-contact nanoimprinted devices with channel lengths of several hundred nanometers.

Kurzfassung

Die vorliegende Arbeit beschäftigt sich mit organischen Dünnschichttransistoren (TFTs) aus Pentacen. Diese werden durch das Einbringen verschiedener Zwischenschichten an der Grenzfläche zwischen dem Gate Dielektrikum und dem organischen Halbleiter modifiziert.. Zusätzlich zur elektrischen Charakterisierung der Transistoren wird – im Rahmen zahlreicher Kollaborationen – das Wachstum der Pentacenfilme auf den verschiedenen Zwischenschichten mittels Kontakwinkelmessungen, Rasterkraftmikroskopie und Röntgenreflektometrie untersucht.

Im ersten Teil der vorliegenden Arbeit werden photoreaktive Polymere zur Veränderung zweier wichtiger Kenngrößen von Transistoren verwendet: der Ladungsträgermobilität und der Schwellspannung. Durch UV-Belichtung der Transistoren konnte die Schwellspannung über einen großen Bereich verschoben werden. Durch Belichtung der Zwischenschicht vor der Pentacenabscheidung konnte hingegen das Pentacenwachstum kontrolliert werden, was zu einer Verränderung der Ladungsträgermobilität bei Raumtemperatur führte. Zusätzlich wurden dabei auch die Temperaturabhängigkeit der Transistorcharakteristiken und vor allem die Aktivierungsenergie des Ladungsträgertransports modifiziert.

Der zweite Teil dieser Arbeit widmet sich dann ausschließlich der Temperaturabhängigkeit diverser Kenngrößen organischer Transistoren. In einem Temperaturbereich zwischen 25 und 400 Kelvin wurde der Einfluss verschiedener Zwischenschichten auf die Transistorkennlinien studiert. Die Temperaturabhängigkeit der Ladungsträgermobilität wurde berechnet und im Rahmen des „Multiple Trapping and Thermal Release“- Modells interpretiert. Zusätzlich wurde auch die Temperaturabhängigkeit der Schwellspannung und des Kontakwiderstands analysiert. Zu den untersuchten Transistoren gehören einerseits TFTs mit oben liegenden Source/Drain Kontakten welche durch Pentacenaufdampfen durch eine Schattenmaske erzeugt wurden und anderseits TFTs mit unten liegenden Source/Drain Kontakten welche durch

Nanoimprintlithographie erzeugt wurden. Bei ersteren hat man es mit Kanallängen in der Größenordnung mehrerer zehn Mikrometer zu tun, bei letzteren Kanallängen im Ausmaß mehrerer hundert Nanometer.

Rather than starting inside,
I start outside and reach the mental through the physical.
Jim Morrison

I. Introduction*

The start of modern electronics was the realization of the first transistor by J. Bardeen[1] in 1947. Earlier, in the so called vacuum tube era of electronics, the vacuum triode[2] was the standard device for radio communications. In comparison to the triode the transistor had a lot of advantages. It was smaller and lighter, produced less heat and consumed less power, and was all in all more reliable. In 1959 the first silicon metal-oxide-semiconductor field-effect transistor (MOS-FET) was produced by Bell Labs.[3] This was the beginning of the success story of the material silicon that still holds on today, since the silicon MOS-FET is still the standard for electronic applications. Every processor in a PC consists of billions of MOS-FETs, and radio and TV wouldn't be imaginable in the way they are without silicon technology.

Also starting from the 1950s an alternative technology to silicon – the organic semiconductors - slowly surfaced and has gained more and more attention since then. In 1964 systematic studies based on aromatic and heterocyclic compounds were presented with electrical conductivities up to 0.5 S/cm,[4] soon followed by studies on the influence of doping, pressure and chain length on the conductivity.[5] The kick-start for organic semiconductors meant the work of A.J Heeger, A.G. MacDiarmid and H. Shirakawa in 1977, who presented the iodine-doping of polyacetylene with a conductivity up to 38 S/cm.[6] For this invention they were awarded the Nobel Prize in Chemistry in 2000. It took another ten years until the first working organic thin-film transistor (OTFT), which based on polythiophene was produced.[7]

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* This chapter structurally builds up on a more detailed timeline of electronics written from the Museum of Computer History (www.computerhistorymuseum.com)

In 1995 the first organic n-type TFT was demonstrated using C_{60},[12] clearing the way for organic complementary metal-oxide semiconductor (CMOS) technology. The first CMOS inverters have been published a year later.[13] Finally, in 2000 ambipolar behaviour (simultaneous p- and n-conductivity) was measured for the first time in organic materials.[14]

Since the invention of OTFTs their performance has improved continuously over the years (Figure 1.1.[15]), and is comparable to amorphous silicon field-effect transistors (FETs) nowadays. The use of this new OTFT-technology enables new fabrication processes and applications. Since polymers are soluble, they can be processed by printing.[16] This enables high volume and high speed processing and, consequently, reduces the production costs. Envisioned (or already existing) products include electronic paper,[17] flexible displays,[18] radio frequency identification tags (RFID)[19] and low-cost sensors.[20]

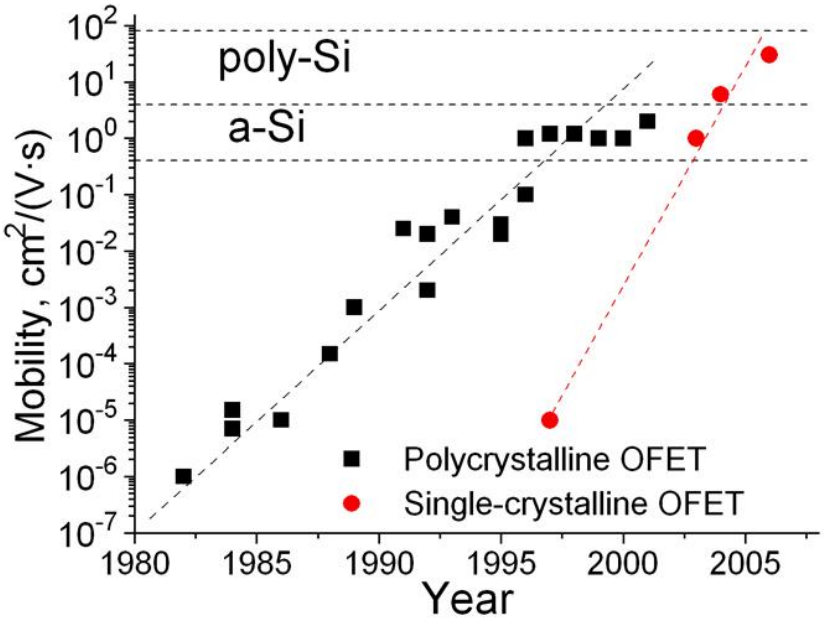

Figure 1.1) Published mobility values in organic field-effect transistors over the last 3 decades. Plot taken from Reference 15.

1.1) Structure of this thesis

This thesis is structured in three main parts. The first part, which consists of the following two chapters, deals with the theoretical and experimental basics of organic TFTs. The second part (consisting of chapter 4 and chapter 5) deals with photoreactive layers that allow for controlling and switching of the most important device properties in OTFTs. The final part of this thesis focuses on temperature dependent device properties of organic TFTs. To improve readability literature references are placed directly at the end of each chapter.

The second chapter of this thesis is an extended introduction to the topic of OTFTs. It explains the basic setup and operation principles of OTFTs and gives a short introduction to OTFT theory and to the extraction of device parameters.

The third chapter is an experimental chapter which sums up the production steps of OTFTs and introduces the lab equipment used for OTFT production and characterization. All analytical methods for an additional characterization of the devices (e.g. characterization of the thickness of organic layers) like contact angle measurements (CA), atomic force microscopy (AFM) measurements and many more are presented here. Additionally the setup for the temperature dependent measurements is presented.

In the fourth chapter a photoreactive polymer is presented which is inserted at the gate dielectric-semiconductor interface and allows for the control of the charge carrier mobility through different UV-illumination times. Through the UV-illumination process the properties of the gate dielectric are changed. To further clarify the influence of the dielectric temperature dependent measurements have been performed.

In the fifth chapter the same class of polymers is used to tune the threshold voltage of OTFTs. Through different UV-illumination times it is possible to

switch the transistors from enhancement to depletion mode operation. An organic depletion load inverter is demonstrated with this experimental setup.

In the sixth chapter the devices properties of pentacene TFTs with different gate dielectric layers are characterized as a function of temperature. This builds up on the measurements at the end of chapter four, but this time with four completely different gate dielectrics.

In the seventh chapter two new device setups for temperature dependent measurements are introduced and the first measurement results for top-contact shadow mask evaporated TFTs and for bottom contact TFTs, which were produced by Nanoimprint lithography (NIL) are presented. The main focus in this chapter lies on the temperature dependence of the contact resistance in TFTs.

1.2) References

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Now this is not the end.
It is not even the beginning of the end.
But it is, perhaps, the end of the beginning.
Winston Churchill

II. OTFT Basics

This chapter describes the basic principles of Organic Thin Film Transistors, the device layout, the working principle and their electrical characteristics. Further the most basic electronic circuit element, which can be built with two transistors, the inverter, is explained in detail.

2.1) OTFTs – a simple model

In the following a simple model to describe OTFTs is presented. This model is enough to understand the basic principles of OTFTs and will be expanded in the later chapters, when the temperature dependence of certain OTFT parameters is discussed.

It has to be noted here that a couple of approximations have to be made, to describe a TFT in that way.[1] Namely:

a) The gradual channel approximation: The transverse electric field induced by the gate voltage has to be much higher than the longitudinal field, which is induced by the source-drain voltage. This assumption is usually justified by the geometry of OTFTs, since the length of the channel L is much higher than the thickness of the oxide.
b) The mobility has to be constant all over the channel, which is only the case when the mobility is gate field and charge carrier density independent. This approximation is fulfilled for most conventional inorganic semiconductors but can lead to problems for organic

semiconductors. In the case of amorphous/polycrystalline organic semiconductors the mobility depends on the density of the charge carriers.

c) The contact resistance is small in comparison to the channel resistance.

The device layout of an OTFT in bottom gate, top-contact configuration is shown in Figure 2.1.[2] Field Effect transistors are three terminal devices; they have three contacts – namely source, drain and gate, where a voltage can be applied. The distance between the source and the drain electrodes is called channel length L, the transverse dimension (the width of source and drain electrodes) is called the channel width W. The third electrode, the gate, is electrically isolated from the active region of the device by a thin insolating layer.

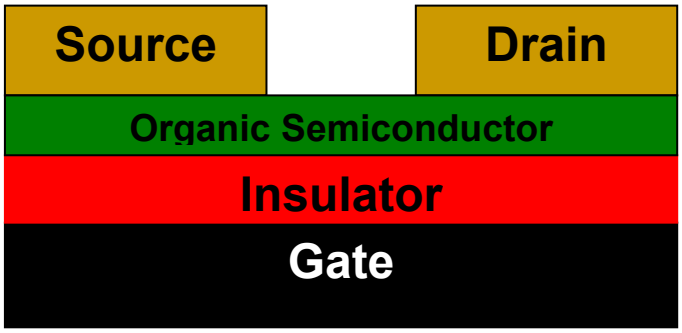

Figure 2.1) Device layout of an OTFT in bottom-gate top-contact geometry.

The device layout in Figure 2.1 is not the only one imaginable for TFTs. The position of the source and drain electrodes and of the organic semiconductor can switch places leading to the so called bottom-gate, bottom-contact geometry. Furthermore the whole structure can be turned upside down, forming the top-gate, top-contact or the top-gate, bottom-contact geometry. Figure 2.2 sums up these different design schemes.[3]

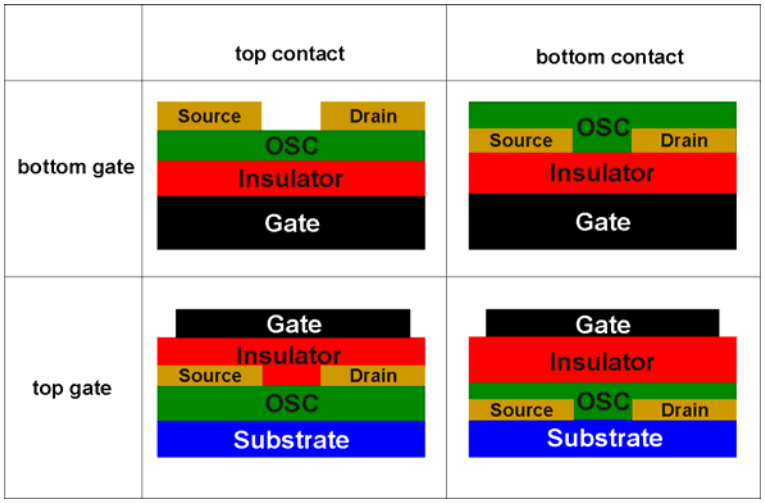

Figure 2.2) The most common OTFT layouts beginning from the top left in a clockwise direction. a) bottom-gate top-contact. b) bottom-gate bottom-contact. c) top-gate bottom-contact. d) top-gate top-contact.

When a voltage is applied to the gate electrode, charge carriers are accumulated at the insulator semiconductor interface and a channel is formed at that interface and charges begin to flow from the source to the drain electrode. By increasing the drain voltage, V_D, the source-drain current, I_D, increases linearly. The transistor is working in linear regime and can be described by Equation 2.1

$$I_D = \frac{W}{L}\mu C_i \left[(V_G - V_{Th}) V_D - \frac{1}{2} V_D^2 \right], \qquad \textbf{(2.1)}$$

where I_D is the drain current, W and L are the channel width and length, μ is the charge carrier mobility, C_i is the insulator capacitance (per unit area), V_G is the gate voltage, V_{Th} the threshold voltage and V_D the drain voltage.

This equation holds as long as V_D is much smaller than the gate voltage V_G. Further increasing V_D results in a saturation of the drain current I_D. The channel is pinched off and the transistor now works in the saturation regime which can be described through Equation 2.2.

$$I_D = \frac{W}{2L}\mu C_i\left[\left(V_G - V_{Th}\right)^2\right]. \qquad \textbf{(2.2)}$$

In References 3-6 a more detailed description on the working principles of OTFTs can be found. Figure 2.3 explains the upper paragraph in more detail.

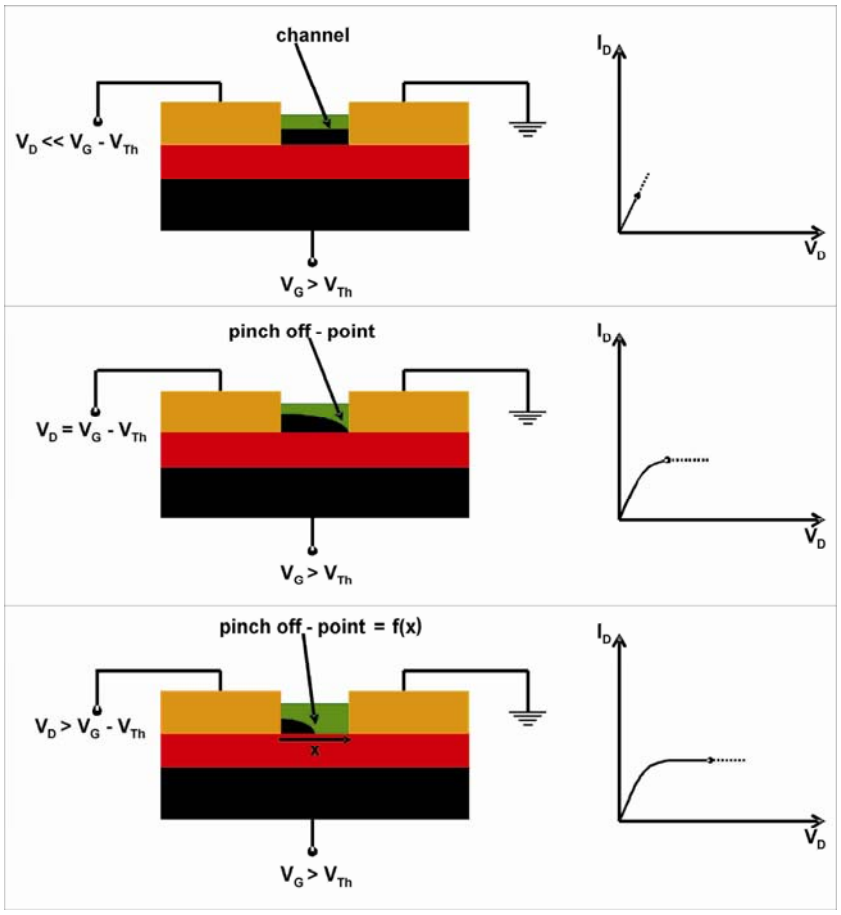

Figure 2.3) Schematic illustration of the operation regimes in OTFTs; (top) linear regime; (middle) start of the saturation regime when $V_D = V_G - V_{Th}$; (bottom) saturation regime. On the right hand side the corresponding I_D/V_D-characteristics for all three cases can be seen. Adapted from Reference 5.

When electrically characterizing OTFTs two basic kinds of characteristics can be identified. These are the transfer and the output characteristics. One obtains the transfer characteristic by sweeping V_G while V_D is fixed. The output

characteristic is obtained by a sweep of V_D while V_G is fixed. An example for both curves can be seen in Figure 2.4. Usually the drain current of the transfer characteristic is plotted in two ways – on a logarithmic scale and on a linear scale, when describing an OTFT in the linear regime and on logarithmic scale and on a square-root scale for devices in the saturation regime.

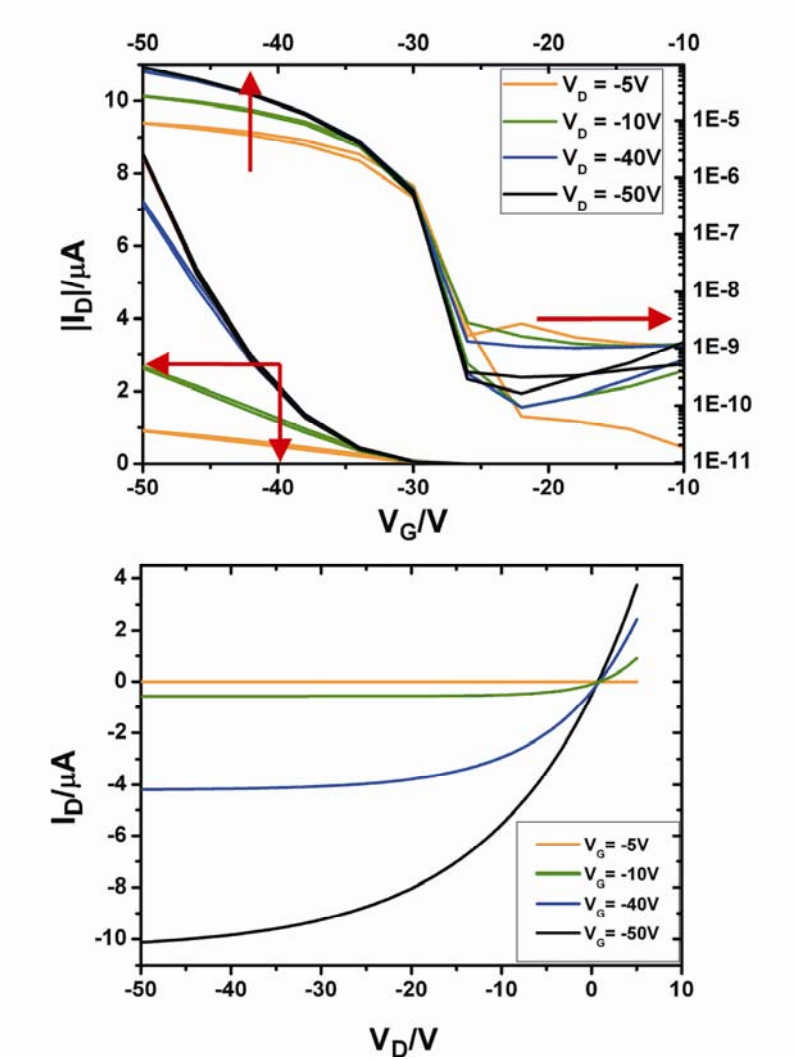

Figure 2.4) Examples for a transfer (top) and an output characteristic (bottom) of a randomly chosen pentacene OTFT. The red arrows in the transfer plot show which transfer lines belong to which axis.

Since these transfer characteristic plots will frequently appear in this work, it should be mentioned that, when looking at Figure 2.4(top) the left and the

bottom axis always belong to the transfer line in linear scale and the top and the right axis always belong to the logarithmic scale. Both scales have their advantages. While the linear scale allows for a determination of the threshold voltage V_{Th}[7] (by plotting the tangent of the curve at its maximum slope), in the logarithmic plot the on- and the off-currents I_{on} and I_{off} (and consequently the on-off ratio), the onset voltage V_{on}, and the subthreshold slope S can easily be seen. The output curve is less informative and will not be used for the determination of any exact OTFT-parameters. It is nevertheless of big importance to measure both characteristics when characterizing OTFTs since the output curve can be used to identify two conditions which an OTFT has to fulfill.

(i) At high negative V_D a nice saturation behavior (constant $I_D(V_G)$ should be observable. This is especially important for further applications like inverters and complementary electronics.[8]

(ii) The existence of a high contact resistance can be checked. A (too) high contact resistance leads to a nonlinear behavior at low drain voltages.[9] A method to quantify the contact resistance in OTFTs is the so called Transfer-Line Method which will be explained in more detail later on.

Another effect observable in both characteristics when measuring a forward and a backward sweep is the effect of hysteresis. Focusing on transfer characteristics this means that a measurement starts at high positive gate voltages and then sweeps down to high negative gate voltages (the forward sweep). Then a second transfer curve is measured starting at a negative gate voltage and then sweeping “backwards” to a positive gate voltage. In a “perfect” transistor there should not be a difference between those two curves. In real devices, this is almost never the case. A so called hysteresis is observed. There are many theories regarding the underlying reason for hysteresis,[10] which can be classified in three main categories (following Reference 10):

(i) effects of mobile charges in (or close to) the semiconducting channel; e.g. trapped charger in the channel or mobile ions in the semiconductor, but also for example the formation of bipolarons in the channel

(ii) effects resulting in a polarization of the gate dielectric; e. g. mobile ions in the dielectric

(iii) a charge injection from the gate electrode into the dielectric

In Reference 10 a very detailed review of all possible causes for hysteresis is given, and in the next chapter a survey about the extraction of all above-mentioned OTFT parameters can be found.

2.1.1) The Transfer-Line Method (TLM)

A possibility to determine the contact resistance in TFTs is the so called transfer line method.[7] Originally this method was developed for a-Si:H transistors,[11] but since then it was also often applied to organic devices.[12,13] The basic idea of this method is that only the channel resistance is proportional to the channel length while the contact resistance remains independent of it. Consequently, the method consists of measuring transfer characteristics in the linear regime of devices with different channel lengths. Plotting the width normalized total resistance as a function of channel length leads to straight lines, the slopes of which are corresponding to the channel resistance while the extrapolation of the line to zero length gives the contact resistance. Equation 2.3 shows these dependencies in more detail and Figure 2.5 gives an example for a TLM-plot.

$$\frac{V_D}{I_D} = R_{tot} = R_{con} + R_{ch} = R_{con} + \frac{L}{WC_i\mu(V_G - V_{Th})}, \qquad \textbf{(2.3)}$$

here R_{tot} is the total resistance, R_{con} the contact resistance and R_{ch} the channel resistance

It should be mentioned here that this method can only be applied under the assumption that all used samples have similar device properties (mobility, threshold voltage, contact resistance). Since the device to device variance of OTFTs is usually quite high the results of this model must be handled with great care. Additionally, the crucial assumption of this method – namely that the contact resistance is completely independent of the channel length and of the drain current I_D – is not a given fact in organic devices.

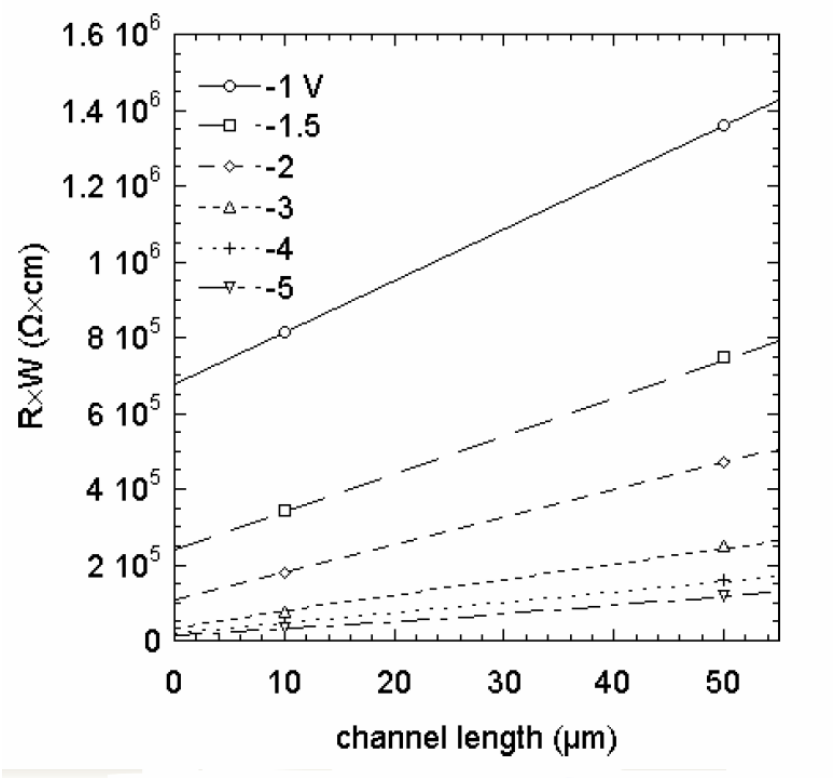

Figure 2.5) Example of a transfer-line-method plot. The width-normalized total resistance is plotted as a function of channel length. This should result in a linear relationship. Plot taken from Reference 7.

2.1.2) The Temperature dependence of the mobility in OTFTs

In metals and conventional inorganic semiconductors charge transport is associated with band transport. This transport model is governed by delocalized

states and the charge carrier mobility is limited by phonon scattering. This leads to a reciprocal relationship between charge carrier mobility and temperature, e.g. increasing the temperature leads to a decrease of mobility.[14] In organic semiconductors, where the mobilities are usually much lower, this is not the case. In this type of materials charge transport is thermally activated – increasing the temperature leads to higher charge carrier mobility. To explain this effect alternative models, which include localized states, had to be developed.

The following explanations focus on polycrystalline and amorphous materials, and do not hold for single organic crystals (rubrene, pentacene single crystal). In a polycrystalline material, highly ordered regions (grains) are interrupted by basically non ordered regions (grain boundaries). Prototypes for this kind of materials are vapor deposited small molecules, like pentacene and oligothiophenes.
Conduction in this type of materials is thermally activated and governed by trap states. A trap is a state where a charge is localized for a given time. In general, the energy of this trap states lies in the band gap between HOMO and LUMO.

There exist multiple models to explain the conduction mechanism in organic semiconductors, which can roughly be organized in two classes.

a) <u>carrier hopping between localized states:</u>

In the case of completely amorphous semiconductors, the theory of hopping between localized states is the most common. Within this class of theories various different models have been developed, starting with theories of tunneling[15,16] or polaron hopping based on the Marcus theory of electron transfer[17] to more complicated theories like the variable-range-hopping model.[18] This variable-range hopping theory was again refined by people like Bässler[19] or Vissenberg/Matters.[20]

b) band like transport in delocalized stated after thermal activation of a localized charge carrier:

These theories – mostly used for polycrystalline materials - combine band-like transport with localized states dividing the total amount of charge carriers into two parts – trapped charges and mobile charges. The resulting effective charge carrier mobility in an organic semiconductor then depends on the ratio of mobile charges to the total amount of charges. Again there exist different models like the mobility-edge model[21] or the multiple trapping and thermal release model (MTR).[1,22] In the following we will focus on the MTR-model, since it is best suited for the polycrystalline pentacene devices, that were used throughout this work.

The MTR –model:

The temperature dependence of the mobility can be explained with the multiple trapping and thermal release (MTR) – model, which applies when the following assumptions are fulfilled.

a) Carriers that arrive at a trap are instantaneously captured with a probability close to one.
b) The release of a trapped charge is a thermally activated process.

Figure 2.6 shows the principle of this transport model. In a first approximation, a single trap energy level E_t with a density of states (DOS) N_{tot} is assumed.[1,25]

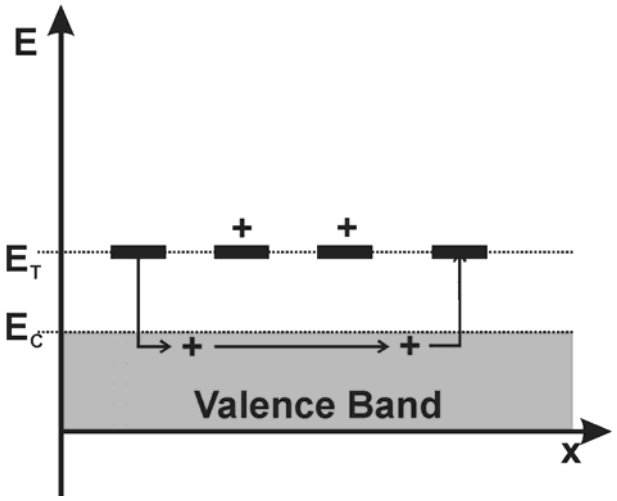

Figure 2.6: The principle of charge transport in the framework of the multiple-trapping and thermal release model.

This total DOS splits up in a density of free charge carriers n_F and into a density of trapped carriers n_T, and both densities can be described by Boltzmann statistics.

$$n_F = N_C e^{-\frac{E_C - E_F}{k_B T}}, \text{ and } \quad n_T = N_T e^{-\frac{E_T - E_F}{k_B T}} \qquad \textbf{(2.4)}$$

Here E_C is the energy of the transport band edge, E_T is the (single) trap energy, and E_F is the Fermi energy.

One arrives at the temperature dependent charge carrier mobility, when evaluating the ratio of the trapped charges to the total charge carrier density. The resulting effective mobility is given by Equation 2.5

$$\mu_{eff} = \mu_0 \alpha e^{-\frac{(E_C - E_T)}{k_B T}}. \qquad \textbf{(2.5)}$$

Here μ_0 is the mobility in the transport band and α in this case is the ratio of the trapped charges to the total amount of charges.

This simple model already leads to a thermally activated mobility. In general the dependence of mobility on temperature is plotted in a so-called Arrhenius plot,

where the mobility is plotted in a logarithmic scale as a function of inverse temperature. Following equation 2.4 this results in a straight line, were the slope of the line can be related to the activation energy E_A of the material. Figure 2.7 shows a standard Arrhenius plot.

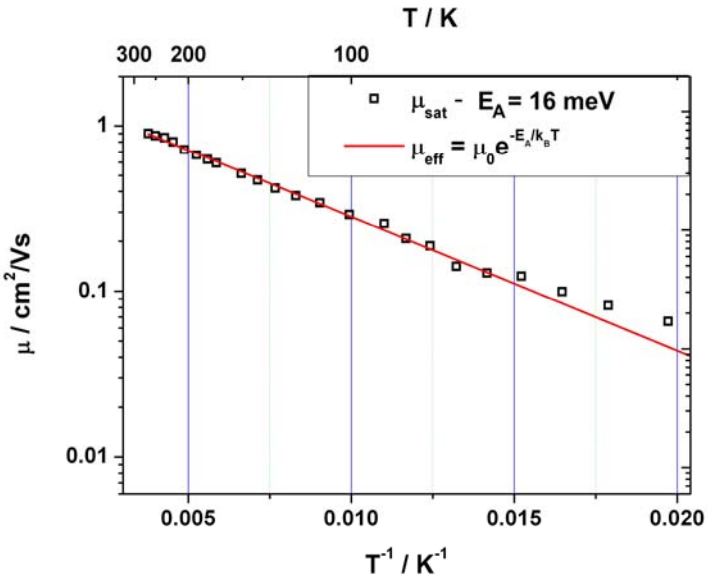

Figure 2.7: An exemplary Arrhenius plot of a pentacene OTFT measured in the helium cryostat. The charge carrier mobility decays exponentially as a function of inverse temperature.

An enhancement of the simple MTR model which assumes an energy distribution of the trap levels already results in a gate voltage dependent mobility.[23,24] Depending on the chosen transport model the density of the traps follows a certain distribution (in the case of the MTR model an exponential DOS is assumed). The only crucial assumption to arrive at a gate voltage and temperature dependent mobility is that the number of free charges is a lot smaller than the number of trapped charges. In the end one arrives at Equation 2.6

$$\mu_{eff} \propto \mu_0 \left[\frac{C_i (V_G - V_{Th})}{qN_t} \right]^{\frac{T_C}{T}-2} \qquad \textbf{(2.6)}$$

Here T_C is a characteristic temperature, that is responsible for the shape of the trap DOS.

Additionally a refinement of the MTR model will be used throughout this work to deal with the temperature dependence of the mobility in polycrystalline pentacene OTFTs. This model was originally developed by Horowitz for polycrystalline oligothiophene thin film transistors,[26,27,28,29] but can be adapted to similar materials without any difficulty.

The polycrystalline transport model[26,27,28,29]

To describe charge transport in polycrystalline materials the medium is divided into low and high conductivity regions – the grain boundaries and the grains, respectively. The size of the high conductivity regions (grains) is assumed to be much greater than the size of the low conductivity regions (grain boundaries). Since grains and grain boundaries are connected in series, the overall effective mobility of a polycrystalline medium can be expressed as

$$\frac{1}{\mu}=\frac{1}{\mu_g}+\frac{1}{\mu_b}, \qquad \textbf{(2.7)}$$

where μ_g and μ_b are the mobilities in a grain and in the grain boundary regions. As long as μ_g is much bigger than μ_b the overall mobility is limited by the mobility within the grain boundaries. This model yields a linear relationship between the effective mobility and grain size as long as the average grain size is bigger than the Debye length $L_D=\sqrt{\varepsilon_S kT/q^2 N}$ of the organic material:

$$\mu=\frac{q<v>l}{8k_BT}\exp\left(-\frac{E_B}{k_BT}\right), \qquad \textbf{(2.8)}$$

where q is the elementary charge, <v> is the electron mean velocity, E_B is the barrier height at the domain boundary, k_B is the Boltzmann constant, T is the absolute temperature, ε_S the permittivity of the semiconductor and N the doping level). As can be seen by Equation 2.8 and by Figure 2.8 this model yields a linear increase of the mobility with increasing grain length l.

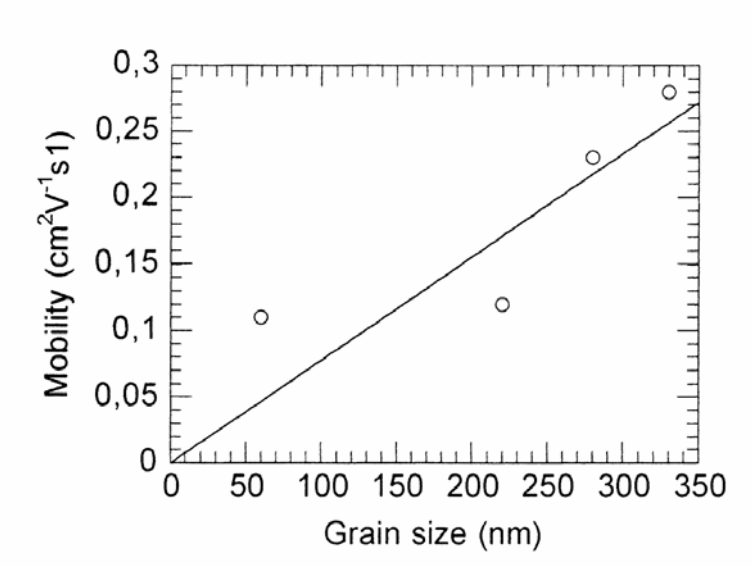

Figure 2.8) Dependence of mobility on the grain size. The straight line is a guide to the eye. This plot was taken from Reference 26.

This so called polycrystalline model yields the same temperature dependence as the MTR-model. More details on this topic will be given in chapter 6.

Concluding, it should be mentioned that in spite of the many theories that exist characterizing charge transport in organic materials, those theories do not exclude each other and all yield an exponential relationship between mobility and inverse temperature. A more detailed review about all different charge transport models can be found in the master thesis of A. Golubkow,[30] in Reference 25, or in the review or Coropceanu et al.[31] Also “Organic Field-Effect

Transistors"[1] edited from Zhenan Bao & Jason Locklin describes some of this models in more detail.

2.2) The Inverter

A standard inverter (also called NOT-gate) is an electrical circuit that outputs a voltage representing the opposite logic level of its input.[32] It also is the most-basic unit for a logic circuit. Table 2.1 shows the truth table of an inverter.

Table 2.1) Truth table of an inverter

Vin	Vout
1	0
0	1

Figure 2.9 shows a so called "voltage transfer curve". In principle this simple plot explains the whole device. The most important device parameters can be extracted from this plot. The black plot in Figure 2.9 corresponds to the curve of a realistic device, while the blue curve is an ideal inverter characteristic. The three coloured regions belong to three important parameters of inverters.
The red coloured region in the middle of the plot is the so called transition region. The gain of the inverter is calculated here. The gain is a measure for how fast an inverter switches and is defined as the slope of the V_{out}/V_{in} curve. Consequently, an ideal inverter would have a slope of infinity. The green region shows the output voltage at the low level ($V_{out, LL}$) which should be close to zero. The orange region shows the output voltage at the high level ($V_{out, HL}$) which should reach the same amount as the supply voltage V_{DD} (in the case of Figure 2.9 the supply voltage is equal to one volt).

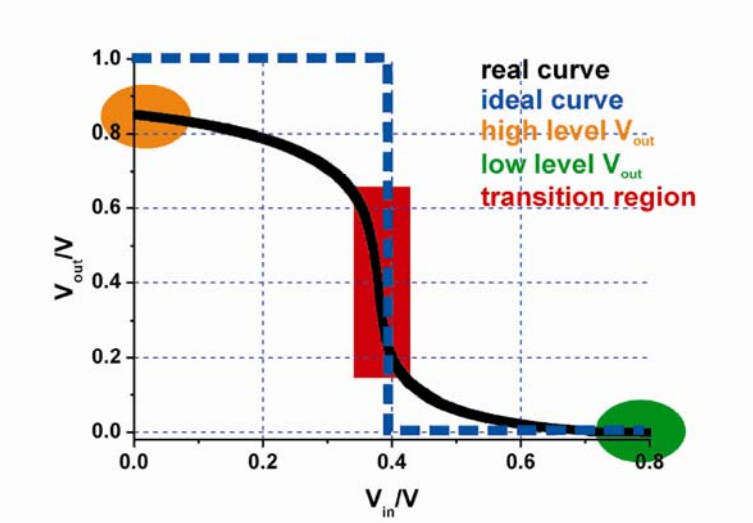

Figure 2.9) A so called "voltage transfer curve" relating the output voltage, V_{out}, of the device to the input voltage, V_{in}, of a real and an ideal inverter. The colored regions show three important device parameters of an inverter. Namely: the output voltage at the low level, the output voltage at the high level and the gain.

Nowadays the standard inverter is a CMOS (complementary metal oxide semiconductor) inverter, which consists of two transistors. One of them is p- and one is n-type. Due to the problems of this design already mentioned in the introduction of this chapter, in organics often the concept of the depletion-load inverter is used.

2.2.1) The depletion-load inverter

A depletion load inverter (as can be seen in Figure 2.10) consists of two p-type (or two n-type) transistors operating in different working regimes. In comparison to the CMOS inverter the technology is more simple (since only p-channel transistors are needed), but the power consumption of this devices is higher.[32] The load transistor is a TFT with a positive threshold voltage and works in depletion mode. The transistor is called normally-on because he is already

switched on at zero gate bias. The switch TFT is a normally-off transistor with a negative V_{Th} and works in enhancement mode.

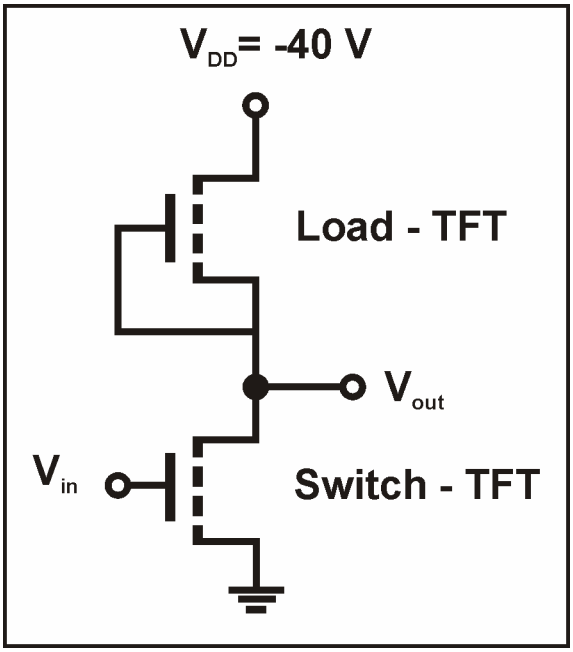

Figure 2.10) Electric circuit of a depletion-load inverter

When the input voltage V_{in} is 0 V both transistors have an identical gate bias: V_G = 0V. In this case, most of the supply voltage V_{DD} drops over the switch-TFT and the output voltage V_{out} is close to V_{DD}. When now increasing V_{in}, the switch TFT draws more and more current and consequently V_{out} decreases. As long as the load transistor stays in the linear regime this decrease of V_{out} is rather slow. As soon as the load TFT operates in saturation mode the voltage drop of V_{out} goes fast and the maximum gain is reached. When further increasing V_{in} all the voltage drops over the switch and the output voltage is in the order of 0 V. This voltage transfer curve of the inverter can easily be approximated by the output curves of the two transistors through the so called loadline construction method, which is depicted in Figure 2.11

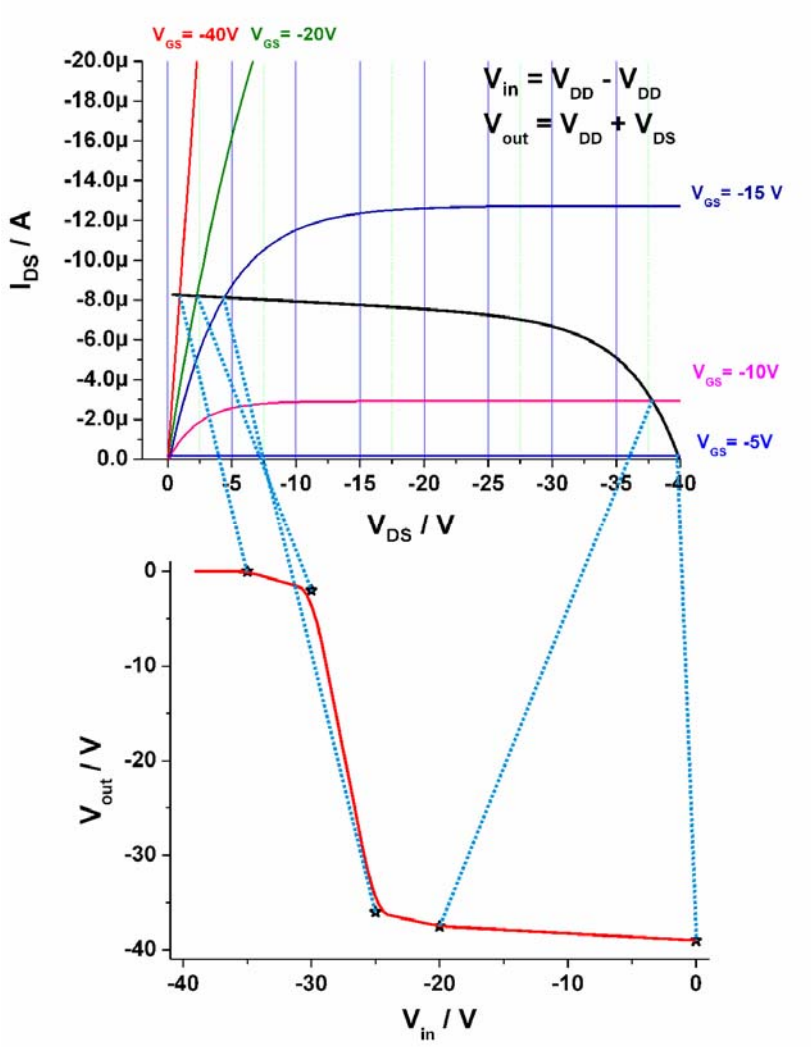

Figure 2.11) Loadline Construction Method. top) the output field of the switch TFT and the loadline of the load-TFT are shown. From the intercepts of this curves the bottom) loadline of the inverter can be constructed.

One needs the output curve of the load transistor at zero gate voltage. This so called “loadline” is shifted by the supply voltage, so that it starts at -40V instead of 0 V, as can be seen in Figure 2.11. Additionally, one needs a set of output curves for the switch TFT for as many different gate voltages as possible.

From the intercepts of the loadline and Equations 2.9, the voltage transfer curve can easily be constructed.

$V_{in}=V_{DD}-V_{DS}$ and $V_{out}=V_{DD}+V_{GS}$ **(2.9)**

From Figure 2.11 it can easily be seen which conditions both transistors have to fulfil in order to yield a well working inverter:

- In order to reach the low level of the output voltage it is necessary to have a nice linear increase of the drain current with drain voltage of the load transistor
- The switching point of the inverter is controlled by the threshold voltage of the switch TFT in comparison to the threshold voltage of the load TFT.
- For the high level of the output voltage it is necessary to reach a nice saturation in the output characteristic of the load transistor. Additionally, the load transistor must have a low contact resistance since only with a low contact resistance a transistor has a nice linear build-up of the drain current for low drain voltages in the output curves.

2.3) References

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All life is an experiment.
The more experiments you make the better.
Ralph Waldo Emerson

III) Experimental Section

This chapter deals with the fabrication and electrical characterization of Organic Thin Film Transistors (OTFTs), as it was done in the course of this thesis. It includes the device setup, the experimental methods for device production and device measurement (at room temperature, elevated and low temperatures) and the extraction methods for the device parameters. Additionally, all technical lab equipment is introduced and the analytical methods for device characterization are briefly described.

3.1) Analytical Methods

3.1.1) Contact Angle (CA)

The contact angle is defined as the angle at which a liquid meets a solid surface. This contact angle is specific for any liquid-solid combination and is determined by the surface tension between the solid, the liquid and the surrounding atmosphere. This dependence is called Young's equation

$$\gamma_{SG} = \gamma_{SL} + \gamma_{LG}\cos\theta \,. \qquad (3.1)$$

Here, γ_{SG}, γ_{SL} and γ_{LG} are the surface tensions between the three phases and θ is the contact angle between the solid surface and the envelope of the liquid.

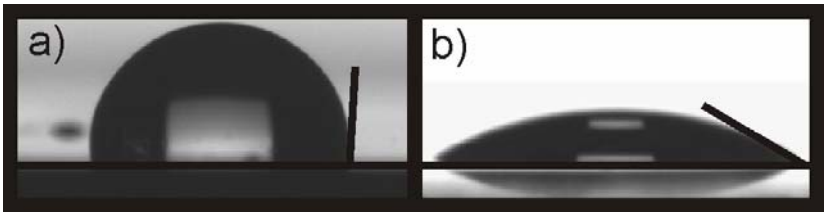

Figure 3.1) water (a) and diiodomethane (b) droplet on a plain silicon oxide surface without any further surface treatment.

Thus, measuring the contact angle is a simple and fast method to measure the surface tension of a solid. In the context of this work, the knowledge of the surface tension was necessary, because it is one of the crucial parameters that determines the growth of organic molecules on a certain surface. Moreover, it is often used to determine the successful treatment of a certain surface (e.g, by plasma-etching)

The method employed in this work is the static sessile drop method, where a fixed drop volume is applied to the surface. The droplet is photographed and by using an image recognition software the angle between the envelope of the droplet and the solid surface is evaluated. Camera, PC software and measuring stage are implemented into the Drop Shape Analysis System DSA 100 (Krüss GmbH. Hamburg, Germany). When using two test liquids with a well known but different surface tension (in this work water and diiodomethane) the exact surface tension of the sample, its polar and dispersive components and its polarity can be evaluated by the method of Owens and Wendt.[1] Following this theory, the surface energy is divided in two components – the dispersive part of the surface energy and the polar part of the surface energy. The resulting principle equation is the equation of a straight line, so that the polar and the dispersive components of the surface energy are related to the slope and the intercept of the resulting line. In practise a number of contact angles with different probe liquids (in our case two: water and diiodomethane) is measured and than a straight line is fitted to the resulting data points. Figure 3.1 shows the contact angles of water and diiodomethane on a plain silicon oxide surface without any further surface treatment. In the course of this work most CA measurements have been performed by Lucas Hauser.

3.1.2) Fourier Transform Infrared-spectroscopy (FT-IR)

FT-IR is a standard technique for the classification of organic (and inorganic) materials. Chemical compounds are identified based on how infrared radiation is absorbed by the compounds' chemical bonds. For most materials, or at least functional groups, IR data is easily available.[2] A molecule composed of n atoms has 3n-6 vibrational modes which can be seen via IR-spectroscopy. Figure 3.2 shows an exemplary IR spectrum of the molecule formaldehyde.[3] In practice, the number of observed absorptions may be increased by additive and subtractive interactions leading to combination tones and overtones of the fundamental vibrations, in much the same way that sound vibrations from a musical instrument interact.

In FT-IR spectroscopy, the material to be analyzed is illuminated with infrared light and the transmitted intensity I_{trans} is measured. This intensity is compared to a background spectrum. In this work first an IR-transparent substrate was used for recording the background spectrum I_0. Afterwards, another substrate with a thin layer of the analyte was measured. By calculating the transmittance T (Equation 3.2) the infrared spectrum is obtained

$$T = \frac{I_{Trans}}{I_O}. \qquad \textbf{(3.2)}$$

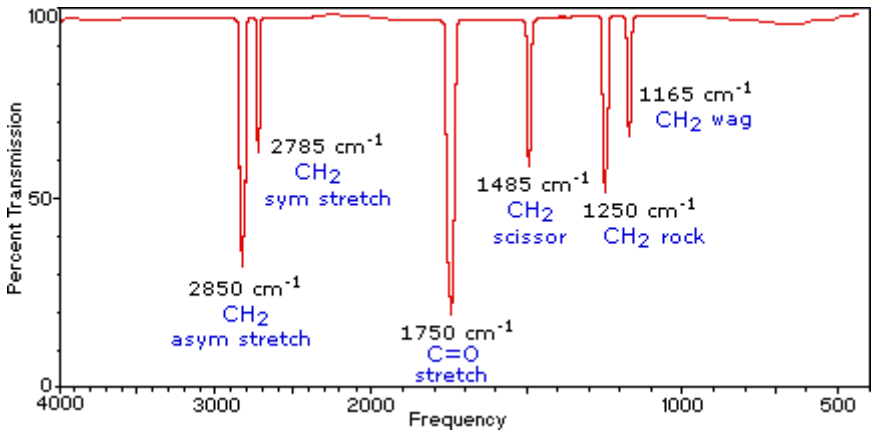

Figure 3.2: Exemplary IR spectrum of the formaldehyde molecule (CH_20) with all characteristic peaks, taken from Reference 3.

In this context it has to be mentioned that the adsorbance of water onto the substrate is a big problem. This water leads to large peaks in the IR-spectra (that lie in the same wavelength range as the actual peaks of the organic material under observation) that often by far surpass the actual signal of the thin film. To overcome this problem, all IR measurements were conducted in vacuum. Most IR-spectra shown in later chapters were recorded by Matthias Edler and Thomas Griesser.

3.1.3) X-ray reflectivity (XRR)

XRR is a powerful tool for the investigation of thin films at the submicron scale, since it can be used to determine the thickness of a given film, the electron density of the materials and the surface roughness as well as the interface roughness at the same time. The following description closely follows Reference 4.

In principle, the refractive index of materials is slightly less than unity when using x-ray radiation. Consequently, there exists a critical angle below which total reflection of x-rays occurs. Specular XRR measurements are performed with incidence angles slightly above the critical angel. Here the incident beam is partially reflected from and partially transmitted through the material. The reflected intensity is determined as a function of the reziprocal space vector perpendicular to the surface (q_z) through the Fresnel relationship. Rough surfaces will be less reflecting than ideally flat surfaces and thus reduce the reflectivity by a Deybe-Weller factor.[5] Statistically the root mean square of the roughness (σ_{RMS}) can be evaluated.

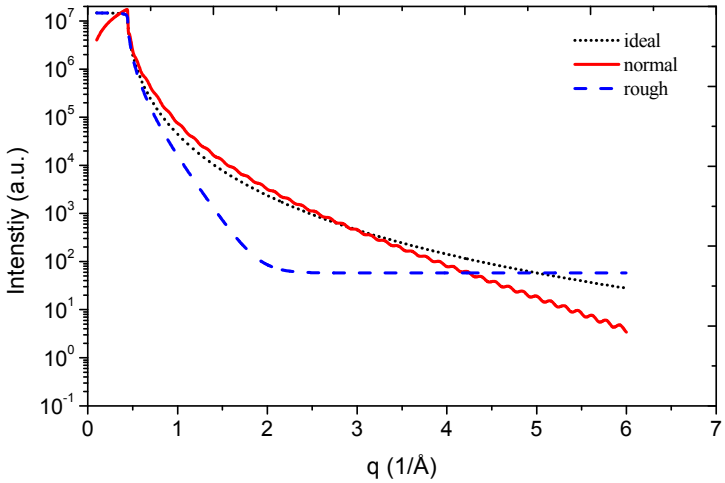

Figure 3.3: Simulated XRR curves of a silicon waver. The dotted black curve shows an ideally flat surface and the dashed blue curve introduces a very high surface roughness where the effect of reduced specular reflectivity is observed. The red curve shows the fit of a silicon waver with a rather smooth surface. This plot was made by Alfred Neuhold.

Any additional layer on top of a flat substrate (e.g. an organic material on a surface of silicon oxide) increases the complexity of the system. Since the incident wave is partially reflected and partially transmitted at every surface reflected waves interfere with each other. The reflected intensity can be obtained by a recursive formalism invented by Parratt.[6] The layer thickness is determined by the distance of the minima of the Kiessig fringes in the XRR pattern.[7] Figure 3.3 shows exemplary XRR-curves showing these phenomena. Throughout this work a Bruker diffractometer D8 Discover, set up in Bragg – Brentano configuration with a copper sealed tube (wavelength = 1.54 Å) and a point detector was used for XRR measurements. Measurements were performed by Heinz-Georg Flesch, Alfred Neuhold, Jiri Nowak and Armin Moser from the group of Roland Resel.

3.1.4) Atomic Force Microscopy (AFM)

The AFM, which was developed in 1986[8] allows for an atomic resolution. The basic setup can be seen in Figure 3.4. Principally it consists of a cantilever with a sharp tip that is used to scan the specimen surface. When the tip is brought near to the surface, forces lead to a deflection of the cantilever. Typically, this deflection is measured by a laser spot which is reflected from the cantilever and detected in some nearby photo diodes.

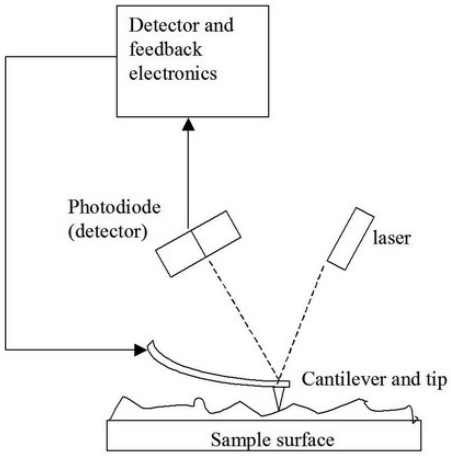

Figure 3.4: Schematic block diagram of an AFM, taken from Reference 9.

There exist several different imaging modes for an AFM (e.g. contact mode, non-contact mode, tapping mode). During this work the tapping mode was the only one used. In this mode the cantilever is driven to oscillate near its resonance frequency by a small piezoelectric element. In proximity to the surface under observation forces (e.g. Van der Waal, electrostatic forces…) change the amplitude of this oscillation. An electronic servo adjusts the height of the cantilever to keep the amplitude of the oscillation constant while the tip scans over the surface. This method is especially “soft”, concerning the amount of damage done to the tip and to the surface. It is especially suited for operation in non-vacuum or ambient conditions and when investigating soft materials. In

the course of this thesis most AFM pictures have been taken by Anja Haase and Alexander Fian.

3.2) Lab Equipment

3.2.1) Evaporation Chamber

Evaporation chambers were used, on the one hand for the application of the organic semiconductor pentacene (which was performed at the NMP Weiz by different co-workers) and, on the other hand, for the evaporation of gold source and drain contacts through a shadow mask. In principle such an apparatus consists of a vacuum chamber, and two specimen holders, - one for the material to be evaporated (formed for example by a tungsten boat) and one for the substrates. The specimen holder for the substrates can be heated by an external substrate heater to hold the substrates at a fixed temperature during evaporation. Additionally a so called shutter exists, situated directly under the substrates which allows to control whether or not the evaporation material is deposited onto the substrates or not. Typically the shutter is closed during the first and the last seconds of evaporation, where the material is not vaporized homogeneously. Figure 3.5 shows a scheme for a standard evaporation chamber. By applying a high voltage to the tungsten boat, the contained material is evaporated. The vacuum allows vapour particles to directly travel to the target area (e.g. the substrate), where they condense. A quartz crystal microbalance allows controlling the thickness of the evaporated layer (as long as the density of the material is known) by measuring the change in resonance frequency of a quartz crystal.
Details for our evaporation processes for pentacene and gold can be found later in this chapter and in the “OTFT Preparation”-sections of each chapter.

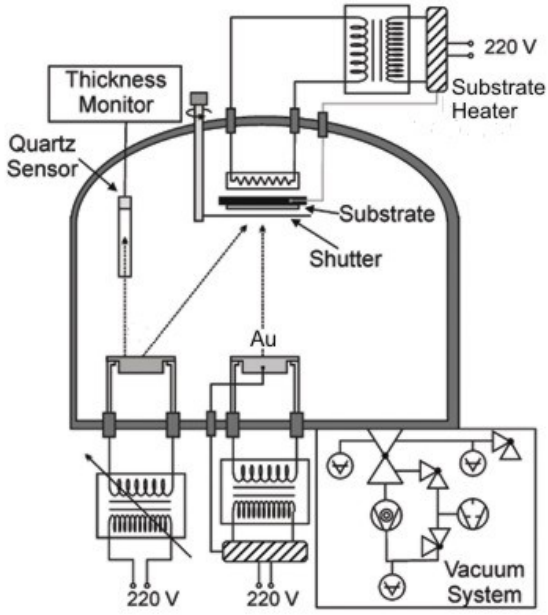

Figure 3.5: Principal setup of an evaporation chamber adapted from Reference 10 to suit the setup used for the experiments in this thesis

3.2.2) Plasma Etcher

In the course of this work plasma etching was necessary as a cleaning process for all silicon wafers before actual OTFTs could be built with these wafers.
The most important components of a plasma etcher are the vacuum chamber, the vacuum pump and the high frequency generator.[11] The working principle can easily be explained with Figure 3.6. At first, the vacuum chamber is evacuated to 0.2 mbar. Then the valve for the gas inlet is opened and oxygen fills the chamber until an equilibrium pressure of around 0.2 mbar is reached. When the generator is activated the process gas is ionized. All silicon wafer were plasma etched for 30 seconds with a plasma power of 100 W.

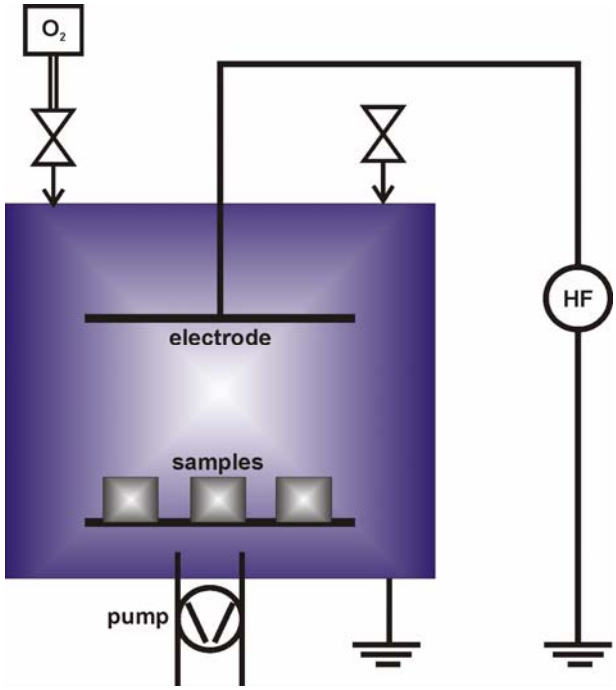

Figure 3.6: Principal setup of a plasma etcher

The oxygen plasma has two main effects on the substrates.

- It cleans the surface of the substrate from any organic residues.
- The surface of the substrate is activated and gets hydrophilic because the number of free OH groups at the surface is increased.

3.2.3) Cryostat

For measurements below room temperature, an Oxford Instruments (Oxford, UK) cryostat was used. For this purpose it was unavoidable to transfer the transistors through air. The principle setup of the cryostat is shown in Figure 3.7

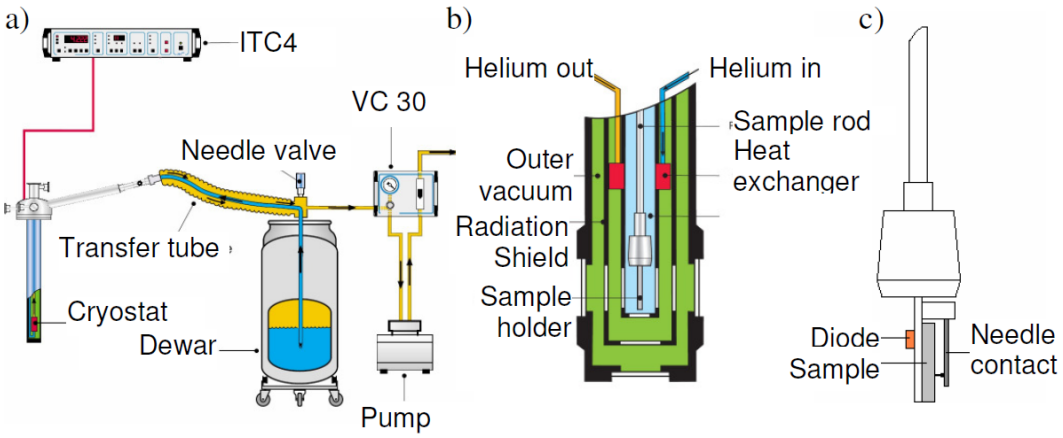

Figure 3.7: Setup of the Oxford Instruments cryostat including the temperature controller ITC4 and the nitrogen/helium dewar; b) closer view into the specimen chamber of the cryostat; c) schematic diagram of the sample holder. Drawings made by G. Slanitsch[12]

The actual cryostat is connected to a dewar (either nitrogen or helium) via a transfer tube. The liquid cooling gas flows from the dewar to the heat exchanger, where it is evaporated. The flow is controlled by the VC 30 flow control meter and pumped out by a membrane pump. In theory the possible temperature range for operation with helium is between 4.2 to about 400 K. The lowest reachable temperature in practise was 25K, probably due to bad vacuum conditions in the outer shielding. For the investigated devices this temperature range was more than sufficient, since at temperatures below 50 K the currents were already that small in comparison to the measurement error. The temperature range for the operation with nitrogen ranged from 400 K to about 77K. Since the thermal conductivity to the sample would be too small for temperatures below 100 K (in comparison to a completely evacuated sample chamber) the sample chamber is flooded with gaseous helium. Additionally, any other gas would condense in the sample chamber and make a reliable device measurement impossible. The sample TFT is placed at the end of a specimen holder. The helium cryostat was used for the measurements in chapter 6.

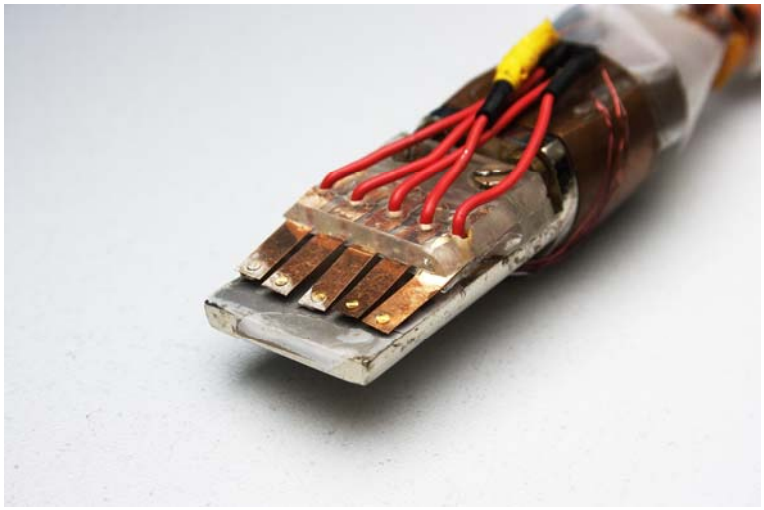

Figure 3.8: Homemade sample holder (designed by Andrey W. Golubkov) designed to fit into the specimen chamber of the cryostat. This setup allowed for the simultaneous measurement of 2 transistors during one cooling cycle.

3.2.4) Heating Stage:

For device characterization at elevated temperatures a DHS 900 heating stage (originally designed for the use in x-ray diffractometers) with a TCU 150 Temperature Control Unit (Anton Paar, Graz, Austria) was used. The heating stage is shown in Figure 3.9. It was transported into the glove box to realize measurements in inert atmosphere. In theory, the heating stage allows for temperatures up to 900°C but for the devices under investigation here, only temperatures of up to 100°C were necessary.

Figure 3.9) The DHS 900 heating stage. The wafer is placed onto the middle of the stage and can be fixed with the clamps.

3.2.5) Combined heating/cooling setup with SIM - contacts

Since the device setup was changed during the experiments to allow for the simultaneous contacting of more than two TFTs and because more different channel lengths were necessary, the whole setup for cooling and heating was adapted. Figure 3.10 and Figure 3.11 show the new heating/cooling setup. The devices were contacted in a standard SIMcard-holder which was inserted into a cooling stage. This cooling stage could be cooled down with liquid nitrogen, which was inserted into the stage through the inlets on the lower side of the box in Figure 3.10. Additionally, a heating element was inserted into the box to realize fixed temperatures during the cool-down and to perform a heat-up as well. With this new setup a temperature range from 100 K to 400 K was accessible.

Figure 3.10) The combined cooling/heating stage. Through the window in the middle of the box, the SIMcard holder, with the TFT in it can be seen. Nitrogen was ingested to the box through the inlet at the bottom side of the box.

Figure 3.11) Closer look into the inside of the cooling/heating stage. In the middle the Simcard holder can be seen.

3.3) Electrical Characterization and Parameter Extraction

The electrical characterization at room temperature in the argon glove box was conducted with an Agilent E5262A Parametric Analyzer (Agilent Technologies, Santa Clara, CA, USA). Devices were contacted with 3 needles, using MDL positioners from Cascade Microtech (Beaverton, Oregon, USA). For the temperature dependent characterization the home-made specimen holder described above was used.

All device parameters were calculated from the transfer characteristics in the saturation as well as in the linear region. In most cases there were no big differences between linear and saturation regime mobilities and threshold voltages.

The OTFT-**mobility** in linear regime was calculated from the slope k_{lin} of the tangent in the linear transfer curve. Equation 2.1 – slightly rewritten – gives the equation of a straight line.

$$I_{D,lin} = k_{lin}[V_G - V_{Th}] + d_{lin} \qquad \text{with} \qquad k_{lin} = \mu \frac{W}{L} C_i V_D \qquad \textbf{(3.3)}$$

The mobility in the saturation regime is calculated in a similar way by rewriting Equation 2.2, plotting the square root of the drain current as a function of the gate voltage and again fitting a tangent.

There exist multiple methods to extract the **threshold voltage** in an OTFT.[13] Throughout this work the threshold voltage was calculated using the Extrapolation in the linear/saturation region-method.[13] In the case of the threshold voltage in the linear regime a tangent is plotted to the linear transfer curve at its point of maximum slope. Then this tangent is extrapolated and its intercept with the gate voltage axis calculated (or graphically evaluated). The threshold voltage V_{Th} is calculated by adding $V_D/2$ to the gate voltage axis intercept. The method for the saturated threshold voltage is similar, but the intercept with the gate voltage axis already yields V_{Th} in this case. For other methods Reference 13 is a very good review.

The **on-voltage** V_{on} is defined as the point in the $I_D(V_G)$ curve where the exponential growth of the drain current starts.

To quantify the amount of **hysteresis** the area within the off-to-on and on-to-off sweep was calculated numerically by a matlab-routine. The resulting number was divided by the maximum value of the on-current to scale the hysteresis. This easy method was compared to the deltam method[14] (in this method tangents are fitted to the transfer curves of the on-to-off and the off-to-on sweep and the amount of hysteresis is defined as the difference between the slopes of the resulting tangents) and others, and essentially yielded the same results.

There are many possible explanations for the hysteresis in OTFTs.[15] The one that will be used throughout this work relates the hysteresis to hole traps in the active layer.[16,17] Figure 3.12 will be used to explain this model.

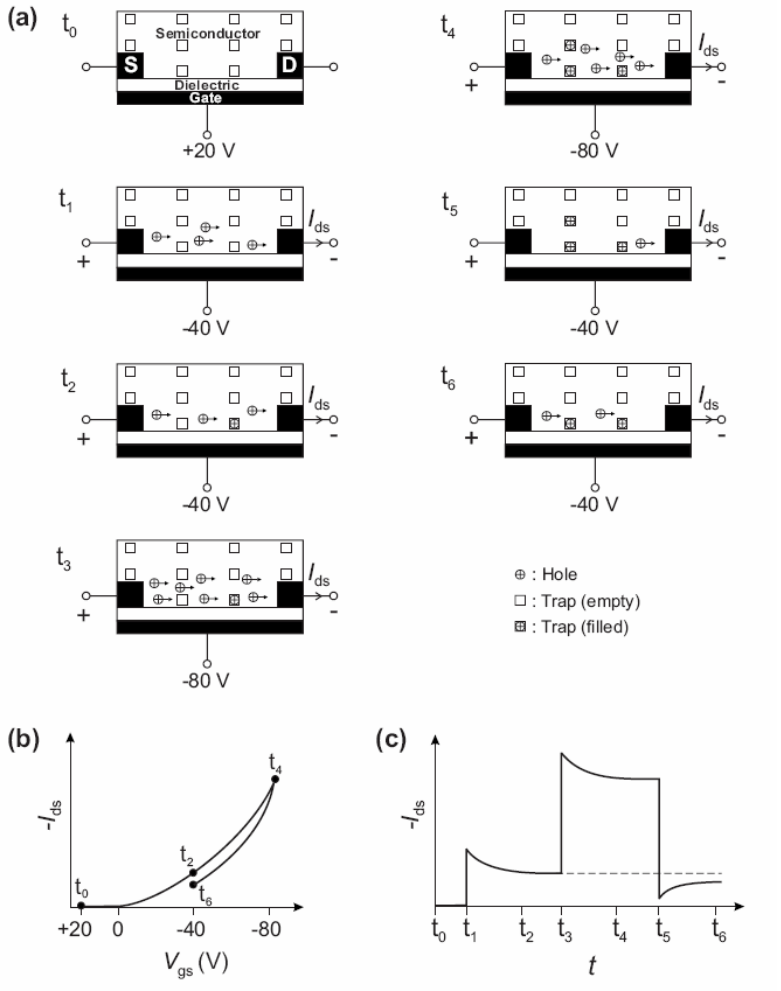

Figure 3.12) (a) Schematic cross section of an bottom-contact TFT showing the charge carrier and hole trap distribution in the semiconductor during a gate voltage sweep. (b) Transfer characteristic of the same OTFT. (c) The drain current of the same OTFT as a function of time. This figure was taken from Reference 16.

In the scheme of Figure 3.12 a “standard” gate voltage sweep is considered. The drain voltage is set to a constant negative value, while the gate voltage is swept from +20 V to -80 V and back again to -40V.

At t = t_0 a positive V_G is applied and no current flows from source to drain. Thus all hole traps are empty. At t = t_1 a negative gate voltage is applied with $V_G > V_{Th}$. This gate bias accumulates a certain number (which is constant for each value of gate voltage) of holes at the dielectric/semiconductor interface and a current begins to flow from source to gate. Over time some of the holes are trapped and the drain current decreases exponentially (t = t_2). The same happens when the gate voltage is further increased (t = t_3 and t = t_4). Now, when sweeping back the gate voltage to a less negative value (t = t_5) I_D will decrease with decreasing gate voltage but will increase with time (t= t_6) as more holes are released from their traps. Thus, at t = t_6 less current than at t = t_2 will flow because a lot of holes are still trapped from the off-to-on sweep. These trapped holes reduce the number of mobile holes and therefore reduce the net current. This mechanism only works when the release rate of the traps is slower than the scan rate. Since this also implicates that fast sweeps must show larger hysteresis than slow sweeps it is quite easy to proof this theory. Indeed this effect was observable in all devices throughout this work.

The **on-off ratio** I_{on}/I_{off} was not calculated automatically following equations like equation 3.3[18]

$$\frac{I_{on}}{I_{off}} = \frac{\max(I_D)}{\min(I_D)}, \qquad \textbf{(3.3)}$$

This method essentially yields exaggerated results, because very often the off-current briefly jumps down some orders of magnitude before it begins to rise again in the region of the onset voltage. The second possibility shown in equation 3.4[18]

$$\frac{I_{on}}{I_{off}} = \frac{\max(I_D)}{I_D(V_G=0)}, \qquad \textbf{(3.4)}$$

is highly arbitrary and for a lot of cases showed in this manuscript even wrong. This equation stems from “ideal” anorganic electronics, where the onset voltage of a transistor lies exactly at a gate voltage of 0 V. To correctly adapt this equation for organic transistors it was a little bit changed.

The value of I_D in the denominator was defined as the drain current at the on voltage V_{on}, while I_D in the numerator was again the maximum of the drain current.

The **substhreshold swing** S_{Sth} was calculated following

$$S_{STh} = \frac{|V_{on} - V_{Th}|}{N_{Dec}}, \qquad \textbf{(3.5)}$$

where N_{Dec} is the number of decades crossed by the drain current in the voltage region V_{on}-V_{Th}. This equation comes from conventional inorganic semiconductor physics[19] and was simply adopted for organic devices.

In the region between turn-on voltage and threshold voltage already a small current can flow although the mobility is still very low.[20] This region is mostly dominated by bulk and interface traps.[21,22] Hence through this quantity the maximum number of interface traps can be evaluated according to Reference 22 using equation 3.6.

$$N_{max} \leq \left(\frac{qS_{STh}\log(e)}{k_B T} - 1 \right) \frac{C_i}{q} \qquad \textbf{(3.6)}$$

where N_{max} is an upper estimate for the number of interface traps, q is the electronic charge, S_{STh} the calculated subthreshold swing, k_B is the Boltzmann constant, T the temperature and C_i the capacitance (per area) of the dielectric.

To summarize and clarify all above definitions Figure 3.13 shows a transfer curve where all parameters have been evaluated.

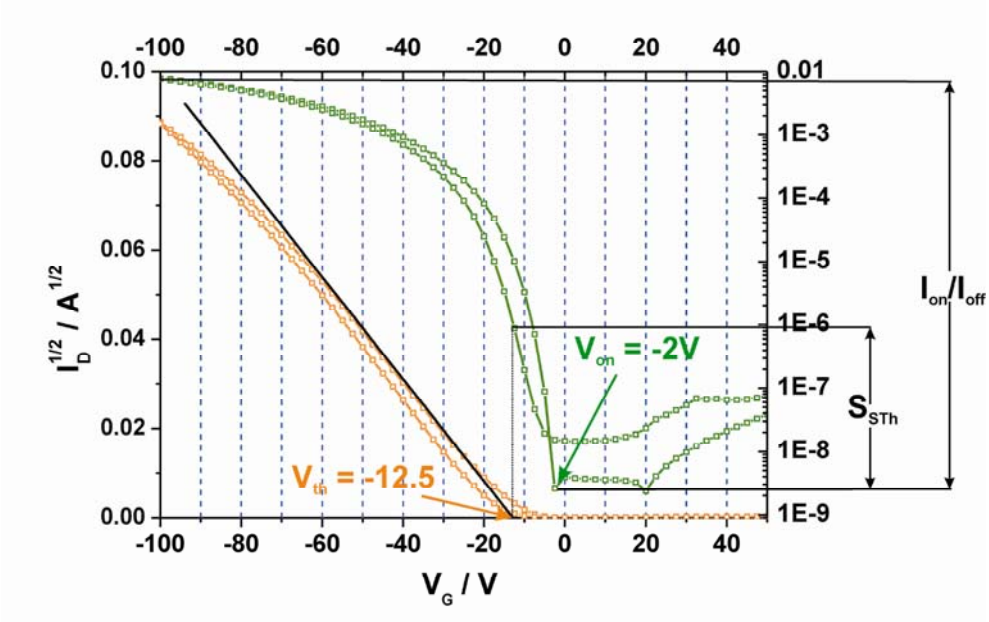

Figure 3.13) Exemplary transfer characteristic of a pentacene OTFT with the device parameters threshold voltage V_{Th}, onset voltage V_{on}, subthreshold swing S_{STh} and on/off-ratio I_{on}/I_{off}. Also the device shows a small hysteresis.

All above-mentioned parameters are of great importance in OTFTs and have to be considered for device optimization. The mobility has to be high to reach high switching rates.[23] A low threshold voltage and a low subthreshold swing are necessary in order to operate a device with low driving voltages.[24] The hysteresis in OTFTs should be minimized in order to allow for reproducible forward and backward sweeps in organic circuits.[25] The on/off-ratio should be high to achieve a good signal to noise ratio.[26] Furthermore, it is of crucial importance to minimize the device-to-device variation and increase the reproducibility of certain device properties. More than this, the stability of device properties with respect to ambient condition and the overall device lifetime have to be increased. Some of these challenges were also the motivation for and the main topic in this thesis. For example, chapter 4 deals with an easy method to

reach higher mobilities and chapter 5 shows a new approach to shift the threshold voltage in TFTs. The device to device variation proofed to be one of the biggest challenges for the following chapters.

3.4) OTFT-production and device setup

Throughout this work, three different transistor setups have been used; each of them looks a little bit different and was produced in a different way. The following part will explain the OTFT production steps for all used setups.

3.4.1) OTFT-setup 1

In the first part of this work (chapters 4 – 6) highly p-doped silicon wafers were used as a substrate and as the gate electrode at the same time. A thin (around 150nm) layer of thermally oxidized $Si0_2$ was used as the gate insulator. The oxidized wafers were purchased from Siegert Consulting e. K. (Aachen Germany) already pre-cut into 2 x 2 cm substrates.

All wafers were O_2-plasma etched (femto-UHP Diener electronic GmbH + Co. KG, Ebhausen, Germany) for 30 seconds with a plasma power of 100 W (40kHz) and afterwards rinsed in deionised water in an ultrasonic bath for 2 minutes. There were two main reasons for this treatment. On the one hand, the 0_2 plasma cleans the wafers and removes any organic residuals on the surface and on the other hand, the $Si0_2$ surface is highly hydrophilic after this treatment. To check the effectiveness of this treatment the contact angle of these wafers with water was measured. An effective pre-treatment resulted in low contact angles below 10°.

Afterwards, pentacene layers with an average thickness of 35nm (as determined by a quartz microbalance) were evaporated at a base pressure of $1x10^{-5}$ mbar with the substrates held at 65°C. The first 5nm of pentacene were

deposited at a rate of 0.02Å/sec and the subsequent 30nm at a rate of 0.1Å/sec. The pentacene evaporation was conducted by our co-workers at the NMP Weiz.

50nm thick layers of Au were deposited through a shadow mask at a base pressure of around 2-5x10^{-6} mbar to form the source, drain and gate electrodes. The layout scheme for this shadow mask can be seen in Figure 3.14. The channel was formed through a tungsten wire with a radius of 25 µm or 50 µm respectively.

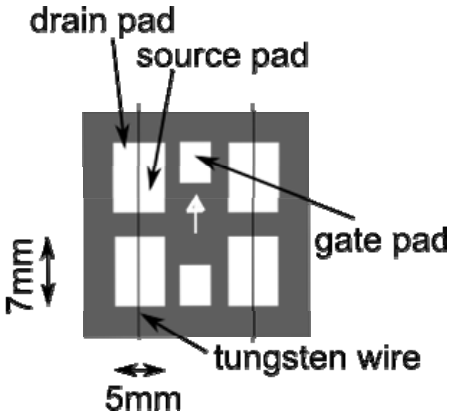

Figure 3.14) Layout of the shadow mask for OTFT-setup 1. The channel was formed using a tungsten wire. This shadow mask yielded in substrates consisting of four 7x5mm big transistors and two smaller gate pads.

Figure 3.15 shows an optical micrograph image of the resulting channel – proving that the channel length really corresponds to the radius of the tungsten wire, though it would be impossible to see a very thin homogenous layer of gold at the bottom of the channel by this method.

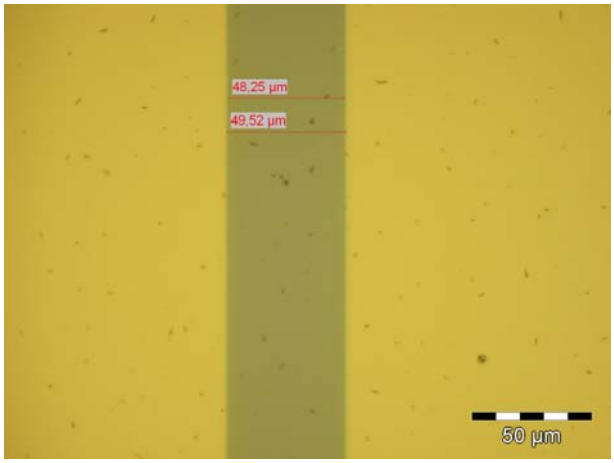

Figure 3.15) Optical microscope image of a TFT channel. In this case the gold electrodes were deposited through a 50nm thick tungsten wire.

Figure 3.16 shows the picture of a silicon substrate containing 4 transistors and 2 gate pads. These gate pads were introduced for the temperature dependent measurements, to fit into the specimen holder of the cryostat. To allow for the contacting of the gate from above – in spite of the bottom gate structure – all substrates were scratched through at the future position of the gate pads prior to the gold evaporation process. This scratching regionally destroyed the silicon oxide and thus the golden gate pads were in direct contact to the common silicon gate electrode. This device setup was compatible with the specimen holder geometry for the cryostat and allowed for the simultaneous measurement of 2 transistors during one cooling cycle.

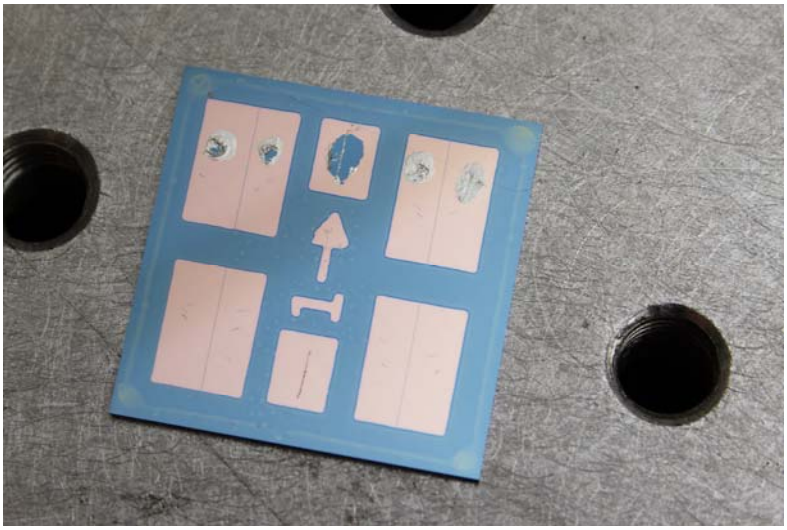

Figure 3.16) Picture of a finished substrate with 4 transistors and 2 gate pads. The scratched surface of the upper 5 pads is a result of the measuring process in the cryostat.

This transistor setup was used for all measurements contained in chapters 4, 5 and 6.

5.4.2) OTFT setup II

To allow for the simultaneous measurement of more than 2 OTFTs, a new specimen holder and a new shadow mask were designed. The layout follows the setup of an eight-pin SIMcard holder, and allows the contacting of six transistors at the same time. Since the SIMcard holder only allowed for the simultaneous contacting of eight pins 3 transistors share a common source electrode though each device has its own drain electrode. This setup maximized the amount of TFTs on one substrate. The gate electrode is contacted from the bottom of the wafer. Figure 3.17 shows the transistor wiring. All 6 TFTs have different channel lengths, L ,and channel widths, W, but have a constant W/L-ratio. The constant W/L-ratio was chosen to guarantee similar on-currents for all six transistors. This setup allows an easy application of the Transfer Line Method (TLM) to evaluate the contact resistance of the devices.

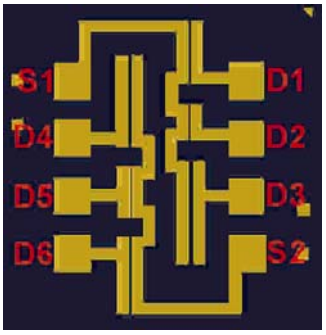

Figure 3.17) Design scheme for the OTFT-setup II. On each side of the substrate are 3 drain pads and 1 source pad. Each transistor has a different channel length L and a different channel width W.

This transistor setup was used for the measurements of chapter 7. More details on the OTFT production can be found in this chapter.

5.4.3) OTFT-setup III

The last OTFT-setup can be seen in Figure 3.18. These devices were processed by Nanoimprint lithography (a process that will be described in more detail in chapter 8) and thus the channel lengths were smaller in comparison to the previous setups. Additionally all TFTs were bottom-contact TFTs. The devices were contacted electrically in analogy to device setup II.
This transistor setup was also used for chapter 7 and a more detailed description of the NIL-process and the OTFT production steps will be given in this chapter.

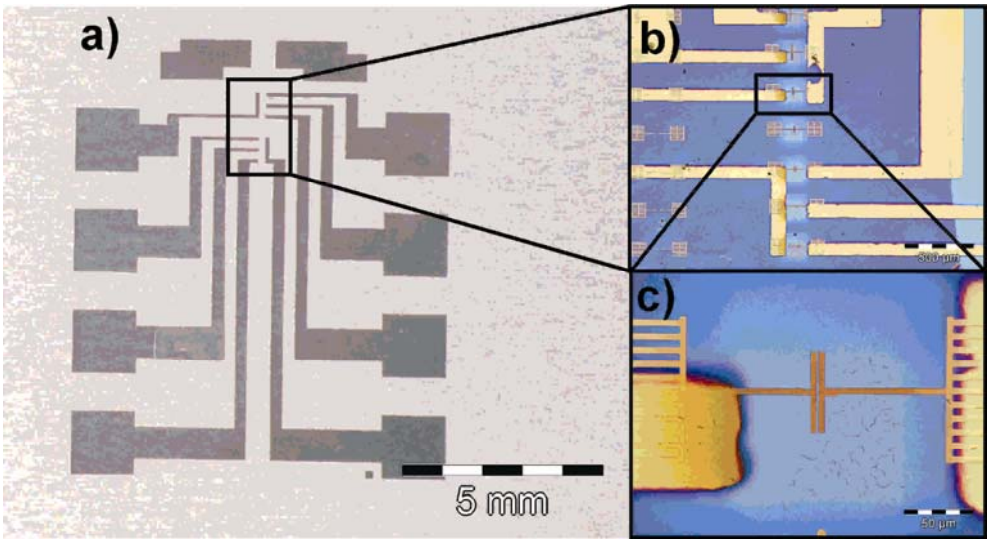

Figure 3.18) a) Design scheme for the OTFT-setup III. The contact pads correspond to OFT-geometry II; b) Closer look at the device setup. On each side of the substrate are 3 drain pads and 1 source pad. Each transistor has a different channel length L and a different channel width W; c) closer look at one NIL-processed transistor.

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To achieve great things, two things are needed;
a plan, and not quite enough time.
Leonard Bernstein

IV) Photochemical Control of the Charge Carrier Mobility in OTFTs.

Preface:

This chapter builds on the basics presented throughout the first three chapters of this manuscript. It focuses on one of the most important device parameters of OTFTs – the mobility, and presents an easy technique to maximize it.
The content of this chapter was published in Applied Physics Letters as follows:

Marco Marchl, Andrej W. Golubkov, Matthias Edler, Thomas Griesser, Peter Pacher, Anja Haase, Barbara Stadlober, Maria R. Belegratis, Gregor Trimmel, and Egbert Zojer:* Photochemical control of the carrier mobility in pentacene-based organic thin-film transistors. Appl. Phys. Lett. **96**, 2010. 213303

To improve the readability the text and content of the paper and the supporting information were intermingled and an extended introduction was added. Additionally, results for temperature dependent device characterization were added.

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*author contributions:

T. Griesser, M. Edler & G. Trimmel: chemical synthesis of the polymer, IR spectroscopy and guides for chemical questions

A. Haase, B. Stadlober, M. R. Belegratis: evaporation of the pentacene films, AFM pictures;

P. Pacher, G. Trimmel & E. Zojer: supervisors & guides for physical problems

M. Marchl & A. W. Golubkov: OTFT preparation & characterization

4.1) Introduction

Impressive progress has been made regarding the production of high mobility organic thin films, but a full understanding of the connection between macroscopic device parameters and the microscopic properties of the semiconductor layers often remains elusive. In literature, the impact of the grain size in polycrystalline layers on the charge carrier mobility in OTFTs is still controversial. It is typically observed that the charge carrier mobility scales with the grain size,[1,2,3] although few reports state that smaller grains result in higher mobilities.[4,5] There are many possibilities known to influence the morphology of pentacene on the dielectric surface: i.e., treating the dielectric surface with self-assembled monolayers and multilayers of, for example, octadecyltrichlorosilane[6] or hexamethyldisilazane,[7] improving the wettability of the dielectric surface by O2 plasma cleaning or etching,[8] changing the temperature of the substrate during semiconductor deposition,[9] irradiating the already deposited pentacene by infrared light,[10] or simply using different dielectrics.[11] Also changing the roughness of the dielectric surface without modifying the surface chemistry,[12] has been shown to have an impact on the charge carrier mobility. The approach presented here, allows for a more precise control combined with a continuous tunability of the pentacene grain size. We use a spin-cast thin layer of the photoreactive polymer poly(endo,exo-bis(2-nitrobenzyl) bicycle[2.2.1]hept-5-ene-2,3-dicarboxylate (PBHND)[14] on top of the SiO_2 gate dielectric. Its chemical composition, in particular, at the surface can be changed in a straightforward manner by exposure to UV light. The UV exposure time of the PBHND layer is found to directly influence the morphology of the pentacene film grown on top of that layer, which allows controlling the effective field effect mobility in OTFT device structures

4.2) Material Characterization

4.2.1) Chemistry

Poly(endo,exo-bis(2-nitrobenzyl) bicyclo[2.2.1]hept-5-ene-2,3dicarbo-xylate) (PBHND), which is a photoacid generator, was prepared analogous to poly(endo,exo-bispheny bicyclo[2.2.1]hept-5-ene-2,3-dicarboxylate) as described in Ref. 14 using nitrobenzylalcohol for monomer synthesis and a Grubbs initator for polymerization. The chemical structure of PBHND before and after the photoreaction can be seen in Figure 4.1. The result of the reaction is a carboxylic acid directly situated at the polymer backbone and a leaving group which is of no further interest.

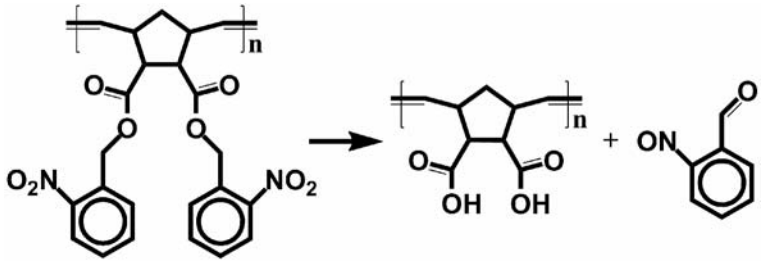

Figure 4.1) The photoreaction of PBHND upon irradiation with UV lights at wavelengths below 350 nm

4.2.2) Infrared Spectroscopy

To proof the generation of the photoacid IR spectra (Bruker IFS 66v/S FTIR spectrometer) have been measured. The changes in the IR spectra of the films upon irradiation depicted in Figure 4.2 confirm the occurrence of the photoreaction: The bands associated with the nitro groups at 1526cm^{-1} and at 1342cm^{-1} vanish and a new band at 1709cm^{-1} appears that is related to the carboxylic acid.[15] To exclude that a heating of the film (e.g., during pentacene evaporation) has any consequence on its composition, also PBHND films

heated to 100°C for 1h were investigated, but no changes in the IR-spectra were observed.

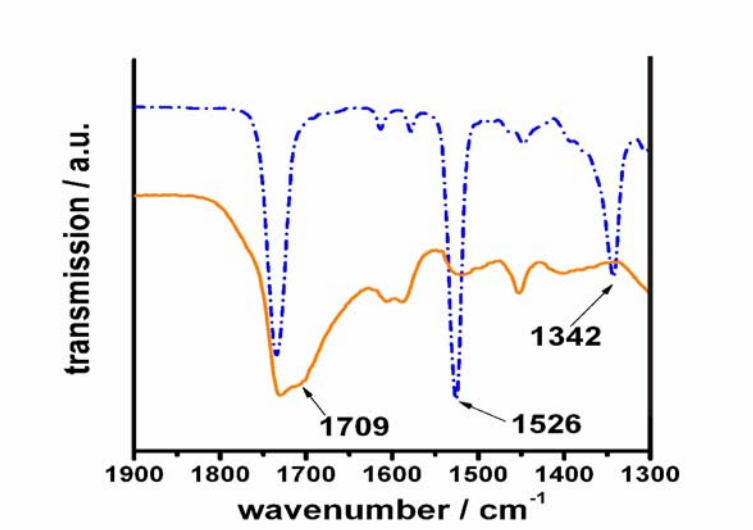

Figure 4.2) IR spectra of a PBHND layer spincast onto a silicon wafer before (blue dots) and after (orange line) UV illumination for 1200 seconds with wave lengths ranging from 320 to 440 nm. The bands at 1526cm^{-1} and 1342cm^{-1} are related to the nitro groups and that band at 1709cm^{-1} to the carboxylic acid generated in the photoreaction. The IR spectrum was recorded by Thomas Griesser & Matthias Edler.

4.2.3) Contact Angle Measurements

Contact angles were measured with water and diiodomethane with a Drop Shape Analysis System DSA 100 from Krüss GmbH. To simulate the effect of transport of the substrates through air and the vacuum conditions during pentacene evaporation, three different sets of measurement have been conducted. The results are summarized in Table 4.1 for (i) a non-illuminated sample, (ii) a sample illuminated for 120 s, and (iii) a sample illuminated for 1200 s. In the first series, contact angles were measured directly after

illumination (resp. spin-coating) of the PBHND layer (first line); in the second series the devices have been stored for 18h in vacuum at a base pressure of $4x10^{-6}$mbar (second line) and in the third series the substrates were stored in ambient atmosphere (third line).

Table 4.1) Contact angles for water and diiodomethane for a PBHND surface for three different illumination times and three different storage methods. The standard deviations for all contact angles are below 2°. This contact angle measurements were performed by Lucas Hauser.

	illumination time /s					
	CA / °					
	0		120		1200	
	Resulting contact angles					
	H_20	CH_2I_2	H_20	CH_2I_2	H_20	CH_2I_2
directly after spincoating	84.1	22.3	80.7	30.7	83.9	36.9
18 h storage in vacuum	91.2	21.2	86.8	32.4	87.7	36.1
18 h storage on air	84.3	22.0	85.1	28.3	85.1	35.9

Following the method of Owens and Wendt[i16] the surface energy has been calculated. The results are summarized in Table 4.2. All three measurement series show the same behaviour; i.e., independent of the storage conditions of the sample, the surface energy is decreased by 5 mJ/m² upon illumination for 1200 S.

Table 4.2) Surface energies for a PBHND surface for three different illumination times and three different storage methods calculated by the Owens/Wendt method.

	illumination time /s γ / mJ/m²		
	0	**120**	**1200**
directly after spincoating	47.6	45.4	42.3
18 h storage in vacuum	47.4	43.7	42.0
18 h storage on air	47.7	45.5	42.5

This is a further evidence for the photoreaction, since the generation of an acid should lead to a more hydrophilic surface and consequently to a decrease of the surface energy.

4.2.4) X-Ray Reflectivity measurements

Since it was the goal to achieve a thick compact layer of the PBHND film (without any holes to the silicon dioxide surface), different concentrations of PBHND in the solvent have been tried. All those solvents were spincoated onto a wafer and XRR measurements have been performed A linear relation between the concentration and the resulting layer thickness was observed, as can be seen in Figure 4.3.

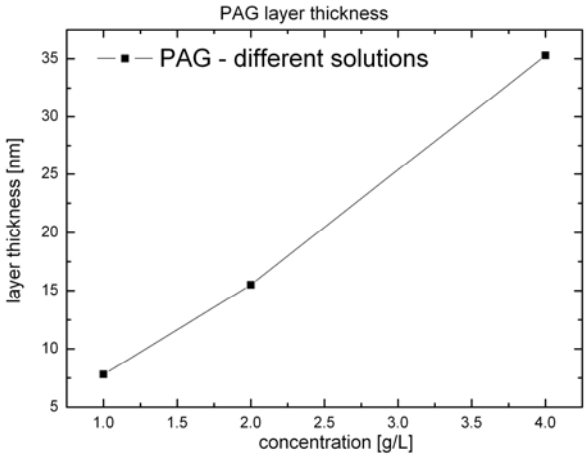

Figure 4.3) Layer thickness of the PBHND layer as a function of concentration. A linear behaviour is observed.

Figure 4.4) shows an XRR curve of a film spincoated from a 4mg/ml solution of PBHND in THF and the theoretical fit showing a resulting layer thickness of around 35 nm. For all later experiments this solution concentration was used. In data not shown here, also illuminated films of PBHND were investigated. No change in layer thickness was observed.

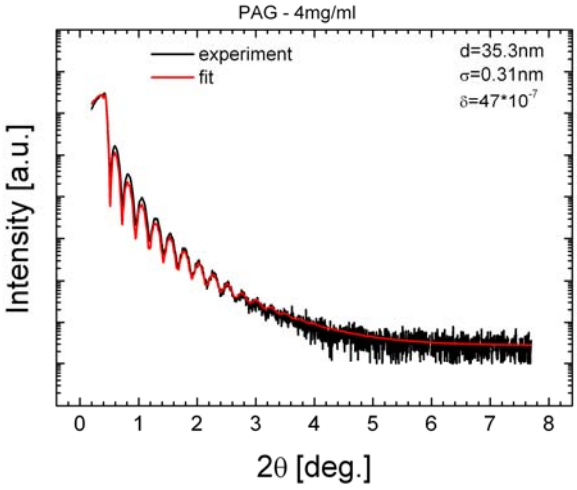

Figure 4.4) XRR curve of PBHND layer spincoated from a 4mg/ml solution in THF. A layer thickness of around 35 nm is observed.

4.2.5) AFM

To check the influence of a long UV illumination time upon the surface of the PBHND layer (concerning roughness and overall morphology) AFM pictures of the PBHND surface have been recorded. In Figure 4.5 the surface of a non-illuminated PBHND layer is compared to a layer that was illuminated for 1200s. No morphological difference can be seen.

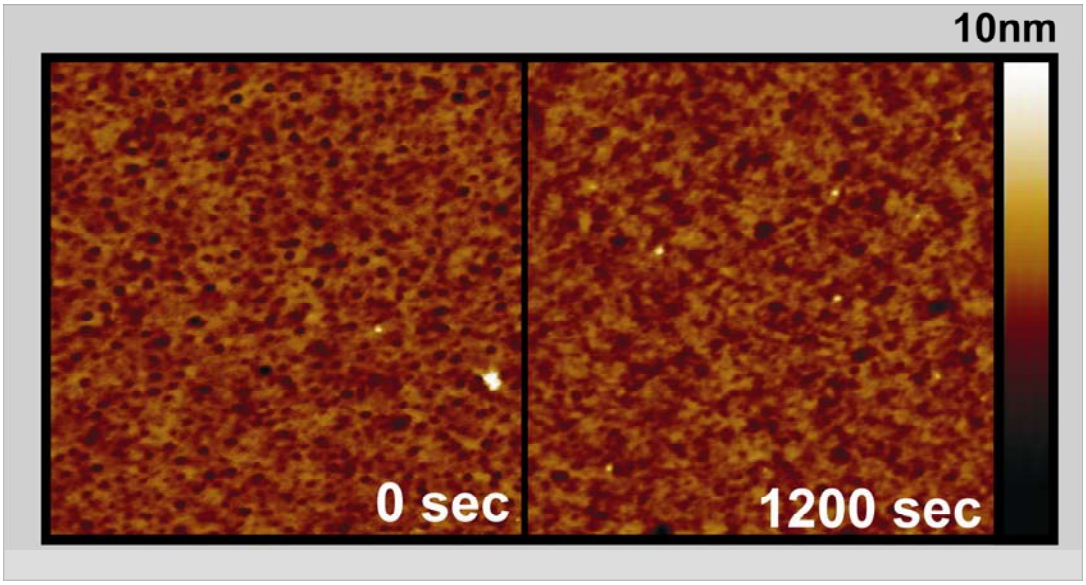

Fig. 4.5) AFM pictures (2x2µm) of a non-illuminated PBHND surface (left) and a PBHND surface after 1200 s of illumination. No qualitative difference of the morphology can be seen.

4.3) OTFT Preparation

TFTs were prepared following the recipe given in chapter 3. After the initial cleaning steps PBHND was spin-cast from a 4mg/ml solution in Tetrahydrofuran (THF) at 1000 rpm during the first 9 seconds and at 2000 rpm during the subsequent 40 seconds. The characterization of those films can be found in the previous chapter. Then, the films were exposed to UV light (EFOS Novacure from 2 to 1200 seconds). The intensity of the light source was set to I_{UV} = 3W/cm^2. During the illumination, the substrates were kept in a nitrogen atmosphere to avoid photooxidation. After this illumination step, there was no further cleaning step to remove possible remaining by-products of the photo reaction. Subsequently, pentacene layers with an average thickness of 35nm (as determined by a quartz microbalance) were evaporated at a base pressure of 1x10^{-5} mbar with the substrates held at 65°C. Between the illumination and the evaporation step the samples were stored in air. To ensure that the observed effects were not related to thermally induced reactions in the interfacial layer, we performed test experiments where the substrates were kept at room temperature during pentacene growth, were we obtained similar results. 50nm thick layers of Au were deposited through a shadow mask at a base pressure of around 4x10^{-6} mbar to form the source and drain electrodes. The resulting channel length was 50 µm and the channel width 7mm. It should be mentioned that devices were exposed to ambient air both before and after electrode deposition.

All experimental findings were reproduced for a total of six exposure series and three different batches of freshly synthesized PBHND.

4.4) OTFT Characterization at Room Temperature

4.4.1) Characterization of the Pentacene surface

Before describing the impact of the interfacial layer on pentacene growth and the electrical device characteristics of the OTFTs, a short summary of the crucial findings of the material analysis:

- AFM investigations revealed no changes in the PBHND film morphology upon UV irradiation.
- The surface energy, γ, decreased from 47.4 to 42.0 mJ/m² upon UV irradiation for 1200 seconds. It is known from literature [18,19] that even smaller changes in surface energy can completely change film growth conditions.

To investigate the effect of the change in surface energy on the growth of pentacene on differently long illuminated PBHND layers AFM pictures (Veeco Dimension 3100 in tapping mode) have been made. AFM images for three different exposure times and an unexposed polymer layer are shown in Figure 4.6. The nucleation and growth behaviour of pentacene thin films is strongly influenced by the UV-induced surface modification. Pentacene growth on pristine PBHND exhibits a high nucleation density and average grain diameters of 0.2µm are observed. The size of the pentacene grains increases with the UV exposure time, $t_{UV,}$ and for t_{UV} = 1200 s dendritic growth is observed. The average pentacene grain sizes were estimated from the AFM pictures using the watershed algorithm of the Open Source software Gwyddion.[17]

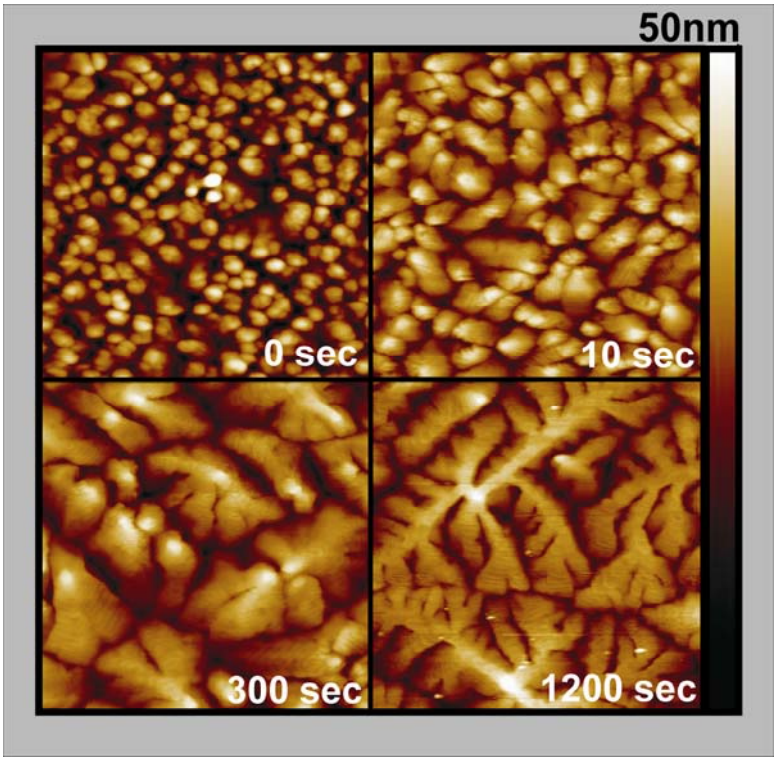

Figure 4.6) AFM images of the pentacene surface on PBHND after different illumination times. Each image corresponds to a 5x5µm section of the pentacene surface. AFM pictures taken by A. Haase & M. R. Belegratis

In this context it should also be mentioned that X-ray diffraction (XRD) data point towards a modification of the crystallographic structure of pentacene films from the Campbell bulk phase[20] to the thin film phase[21] upon increasing UV-exposure. Figure 4.7 shows the XRD results for pentacene grown onto a not illuminated PBHND film and for pentacene on a PBHND film that was illuminated for 1200 seconds. Plotted as logarithmic colormaps. Black circles correspond to spots that belong to the Campbell phase of pentacene and white circles correspond to the thin-film phase.

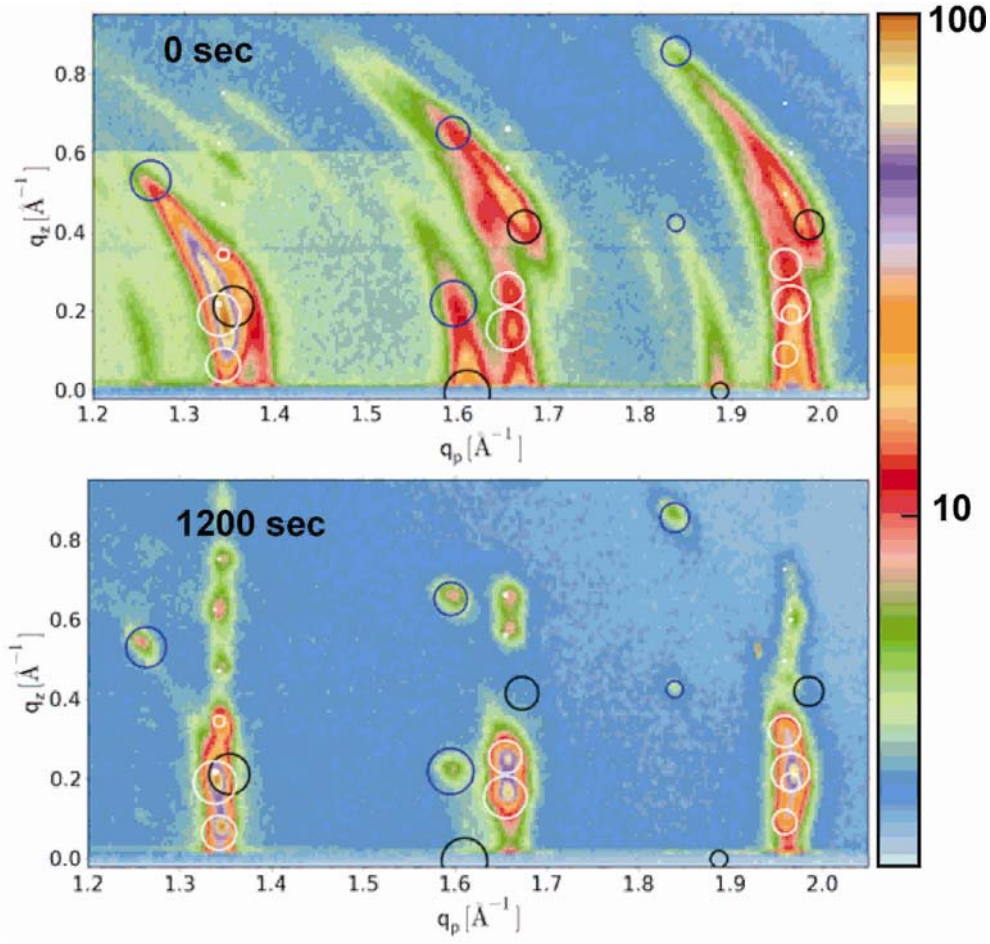

Figure 4.7: XRD-colormaps for a pentacene film evaporated onto top) a not illuminated film of PBHND and bottom) a PBHND sample that was illuminated for 1200 seconds. Black circles correspond to the Campbell phase and white circles to the thin-film phase. This XRD measurement was performed by Armin Moser.

As can easily be seen from the two plots in Figure 4.7 there is far more intensity from the bulk phase measured in the case of the pentacene film evaporated onto the not illuminated sample of PBHND. In the case of the 1200 seconds illuminated sample the thin-film phase dominates.

This, however, is expected to have only a minor impact on the effective mobility as the latter is primarily determined by the carrier transport between the grains as will be shown below.

4.4.2) Electrical Characterization of OTFTs

Electrical device characterization was performed using a Parametric Analyzer (Agilent Technologies – E5262A) in an argon glove-box. In Figure 4.8 the transfer characteristics of the devices from two exemplary exposure series are shown. The on-current and the slopes (and thus the mobilities) rise with increasing exposure times. The hysteresis is very small in spite of the repeated air exposure during device fabrication and the on/off ratios are found to be independent of exposure time. The threshold voltage is slightly shifted to more positive values with increasing illumination time due to a chemical doping mechanism.[22,23,24] Exposure times longer than 1200 seconds resulted in a massive deterioration of the performance of the resulting devices. Mobilities μ and threshold voltages have been determined in the saturation regime and in the off-to-on sweep of the transfer. There is no qualitative difference in the data for the linear regime or the on to off sweep of the OTFT.

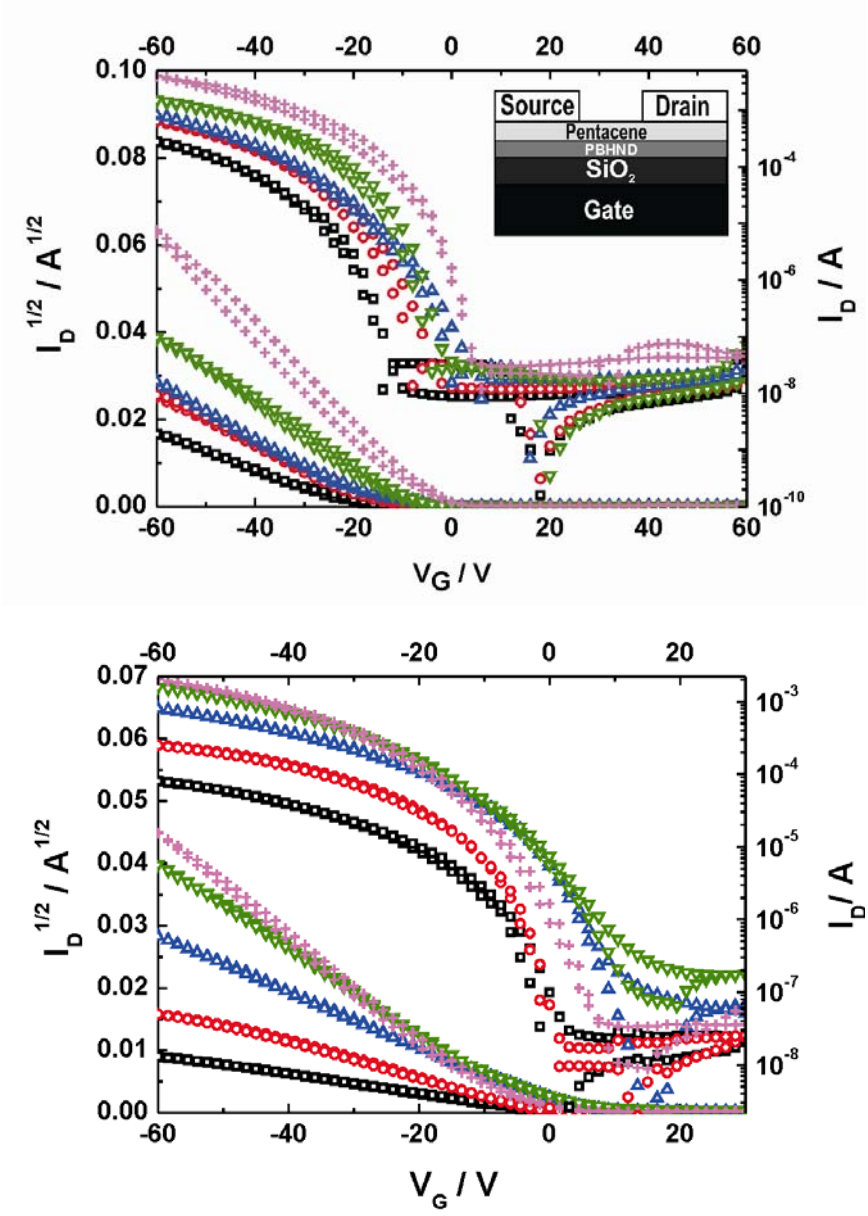

Figure 4.8) Transfer characteristics at V_D = -45 V of two series of pentacene/PBHND OTFTs for different illumination times: ■ unexposed, ●10 seconds, ▲60 seconds, ▼300 seconds, + 1200 seconds.

Figure 4.9 (bottom left) shows the dependence of the mobility on the UV exposure time of the PBHND. A clear increase of the mobility by approximately one order of magnitude is observed upon exposure. This trend correlates well with the evolution of the average grain size, gs, with exposure time (Figure 4.9, top left) The values for the grain sizes given in Figure 4.8 represent the mean

value for all visible grains on a 5x5µm AFM-picture. (e.g. Figure 4.6) Although gs can only be regarded as an effective parameter considering the changes in island shapes depicted in Figure 4.6, relating the effective hole mobility to the average grain size (Figure 4.9 (right)), yields a linear relation.

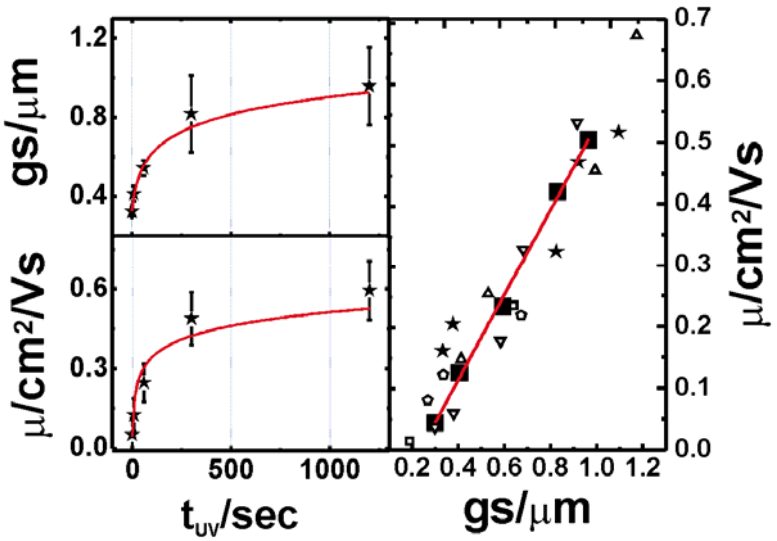

Figure 4.9) Top left: Average grain size as a function of illumination time. Bottom left: OTFT mobility as a function of illumination time. The logarithmic fit in both plots is a guide to the eye. Right: OTFT mobility as a function of grain size. The large symbols denote the average values for 0s, 10s, 60 s, 300s and 1200 s UV exposure times. The small symbols denote the values for each illumination series averaged over all transistors on a particular substrate. The linear fit is a guide to the eye.

These results match those of Di Carlo et al.[1] and Horowitz[9,25] and show that in the present devices inter- rather than intra-grain transport is the mobility limiting factor. Saturation of mobility as shown by others, [1, 25] was not observed in our study because our average grain sizes never exceeded 2 µm.

4.4.3) The role of interface traps

The interface between the dielectric and the organic semiconductor is of crucial importance for the device performance of OTFTs. One cannot exclude that this

interface changes through the illumination in our experiments. There are, however, a number of reasons, why such changes cannot be held responsible for the mobility changes described above.

(i) As can be seen in Figure 4.5, the interface morphology of the PBHND does not change upon illumination.

(ii) The occurrence of deep hole traps would result in a shift of the threshold voltage to more negative values for increasing illumination doses, which is not observed.

(iii) Instead, we see a shift to more positive turn-on voltages, which can be well explained by interfacial doping as already mentioned above.

(iv) Shallow interface traps should lead to a decrease in the sub-threshold swing (S_{STh}).[26] No systematic dependence of S_{STh} on the illumination time is, however, observed. The slight non-systematic variations observed (see Figure 4. 8 above) are within the device to device variance.

(v) An important observation in this context is that μ increases with illumination time. Consequently, illumination would have to decrease the trap density. An underlying mechanism is hard to imagine.

(vi) The impact of traps should, in a first approximation, be linear with the trap density, which – at least for the low trap concentrations that one might envision – should in turn be close to linear with illumination time. We, however, observe a strongly non-linear dependence of μ on illumination time.

(vii) In contrast, μ is linearly dependent on the grain size consistent with the model given in Ref. 9 and Ref. 25. This model was briefly summarized above.

(viii) A dependence of the mobility on the grain size as observed in the current manuscript is exactly what one expects also from more elaborate theories.[1]

(ix) Moreover, when changing the grain-size by different techniques[1] also a linear increase of μ with grain diameter has been observed for grain diameters in the range as in the present paper.

(x) In test experiments on samples illuminated for 1200 s, where we varied the grain size by changing the pentacene deposition rate, we also observed a correlation between grain diameter and mobility. The obtained grain size differences when changing the deposition rate between 1 Å/min and 100 Å/min were, however, only relatively minor.

4.5) Temperature-dependent OTFT Characterization

To further evaluate the influence of the average grain size of pentacene on the transport in OTFTs, devices with different illumination times were cooled down to lower temperatures. Transfer characteristics were recorded. The field effect mobility is plotted as a function of the inverse temperature in Figure 4.10. As can be seen, not only the mobility at room temperature is a function of illumination time of the interfacial layer (and hence the grain size) but also the activation energy E_A is strongly influenced by the grain size. Unfortunately not all devices could be cooled down to 100 K, so probably E_A is too low for the OTFTs with longer illumination time. This experimental finding would indicate that not only the total amount of traps increases with illumination time, but also that the trap energy E_T increases with illumination time, thus lowering the activation energy of the mobility.

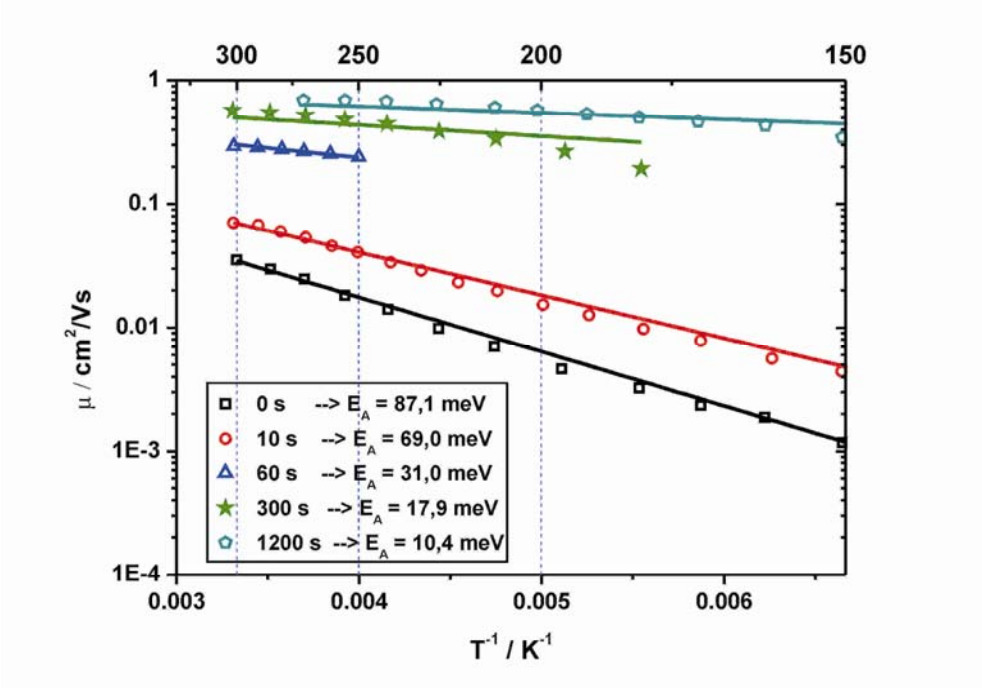

Figure 4.10) Field effect mobility as a function of inverse temperature for differently long illuminated devices.

4.6) Conclusion

In conclusion we have presented pentacene-based OTFTs in which the effective hole mobility can be varied by an order of magnitude (between 0.06 and 0.7cm²/Vs) through a photoreactive interfacial layer. Also the activation energy can be switched from 87.1 meV to 10.4 meV. The best results were obtained with exposure times of 1200 s. This can be related to the size of the pentacene grains being controlled by the exposure of the interfacial layer consistent with the polycrystalline transport model.

4.7) References

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But man is not made for defeat.
A man can be destroyed but not defeated.
Ernest Hemingway

V) Photochemical Control of the Threshold Voltage in OTFTs

Preface

The photoacid polymers introduced in the previous chapter play again the main role in this section. This time they are used to control and fine-tune another device parameter in organic transistors - the threshold voltage.
The text of this chapter builds up on a paper that was published in Advanced Materials.

Marco Marchl, Matthias Edler, Anja Haase, Alexander Fian, Gregor Trimmel, Thomas Griesser, Barbara Stadlober & Egbert Zojer. Tuning the threshold voltage in organic thin-film transistors by local channel doping using photoreactive interfacial layers. Adv. Mat. 22, 2010, 5361*

Again the main paper was intermingled with the supporting information, to increase the readability and an extended introduction was added.

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*author contributions:

M. Edler, G. Trimmel & T. Griesser: chemical synthesis of the photoreactive polymers, IR measurements and guides for chemical questions

A. Haase & A. Fian: pentacene evaporation & AFM pictures

B. Stadlober: guide for inverter performance

E. Zojer: supervisor

M. Marchl: OTFT preparation & electrical characterization, inverter characterization

5.1) Introduction

In recent years, organic thin film transistors (OTFTs) have attracted a great deal of attention due to their potential applications in low cost sensors,[1] memory cards,[2] and integrated circuits.[3] Great efforts are under way to design OTFTs with high performance, high stability, high reproducibility, and low cost.[4] Two of the most crucial device parameters are the charge carrier mobility and the threshold voltage (V_{Th}). Concerning the mobility, the main goals for most applications is its maximization.[5] - as already mentioned in the previous chapter. For V_{Th}, the situation is more complex: For example, for integrated circuits it would be desirable to tune V_{Th} over a broad range,[6] e.g., for inverter applications. In silicon technology, complementary circuits that consist of p-channel and n-channel transistors are typically used.[7] There have been many attempts to adapt this technology to organic TFTs and fabricate organic complementary inverters.[2,8,9] They, however, suffer from poor n-type transistor performance and/or air instability of n-type semiconductor materials. An alternative approach is the adaptation of unipolar depletion-load inverters enabling simplified processing instead, even if they do not provide the low power consumption and the simple circuit design intrinsic to complementary logic.[10,11] Depletion-load inverters consist of an enhancement-mode driver transistor and a depletion-mode load transistor and can be realized using only p-type organic thin film transistors. So far there have been attempts to achieve this target by using a level shifter,[12,13] or a dual gate structure.[14] The main objective is to find a reproducible method to realize driver and load transistors with equivalent device characteristics (in particular mobilities), but different V_{Th}'s. The concept of the depletion load inverter will be explained below in more detail.

Over the years, a number of methods have been developed to tune threshold voltages: For example, oxygen plasma treatment of an organic gate dielectric (parylene) results in a large shift of V_{Th} to more positive values.[15] This shift is related to the generation of charged surface states at the dielectric-

semiconductor interface but the exact mechanism is only poorly understood. The same holds for UV-ozone treatments[16] of the parylene and for the UV treatment of a poly-4-vinylphenol layer,[16] where the latter has been used to realize and eventually to optimize depletion-load inverters. V_{Th} can also be tuned by changing the capacitance of the dielectric,[18] by inserting a polarisable layer into the dielectric,[19,20,21] or by using this polarisable layer as an encapsulation.[22] With the latter methods, V_{Th} can be controllably and reversibly shifted over a wide range. The drawback of such approaches is, however, that a high "programming" voltage is needed to tune V_{Th}. Another possibility to tune V_{Th} is by insertion of self-assembled monolayers[23,24] or chemically reactive thin layers.[25,26] The latter have been shown to tune V_{Th} by a local channel doping using acids groups that can be combined with dedoping reactions using bases. The disadvantage of the latter methods is that a local patterning of threshold voltages is not straightforward. Such a patterning is, however, a prerequisite for the realization of integrated electronic circuits.

Here, we significantly refine the concept of chemical channel doping by replacing the covalently bonded silane layers bearing sulfonic acid groups used in Refs. [25,26] with photoacid generator polymers.[27] The goal hereby is to use them as an interface-modification layer (see Fig. 1a), whose properties can be patterned photochemically, as (in contrast to the molecules used in Refs. [25,26]) the acid group is formed only upon illumination. This paves the way for a photo-lithographic patterning of the interfacial doping and, thus, for controlling, which transistors in a circuit operate in depletion or in enhancement mode. In other words, it enables an accurate local control of V_{Th} through the illumination dose by a method that is fully compatible with lithographic techniques omnipresent in conventional semiconductor industry.

5.2) Material Characterization

5.2.1) Chemistry

The first molecule used here, PBHND, was already characterized in the previous chapter, so the material characterization chapter here will focus on the second molecule – poly-[(endo,exo-N-hydroxy bicyclo[2.2.1]hept-5-ene-2,3-dicarboximide perfluoro-1-butane- sulfonate)-co-(endo,exobicyclo[2.2.1]hept-5-ene-2,3-dicarboxylic acid-dimethyl-ester)] (PHDBD). The chemical structure of this molecule and its photoreaction can be seen in Figure 5.4. The monomer synthesis and the polymerization process are the same for both molecules. In contrast to PBHND this time a sulfonic acid is formed, which is not linked to the polymer backbone but to the leaving group.

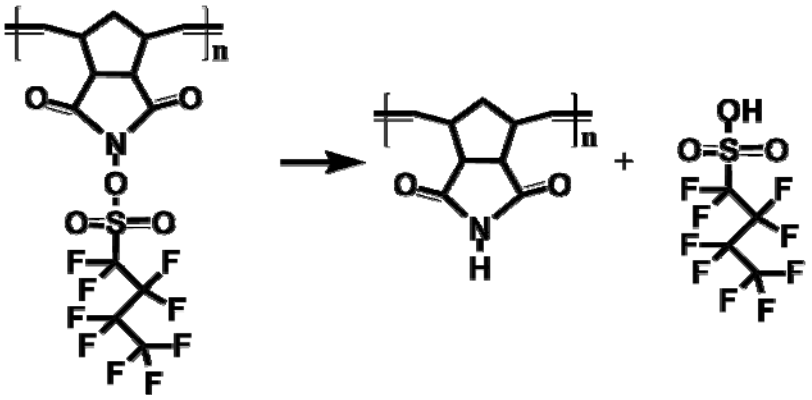

Figure 5.4) Photoreaction of PHDBD upon irradiation with UV light. A sulfonic acid is produced upon illumination.

5.2.2) Infrared Spectroscopy Measurements

As before, IR spectra have been recorded. Again the spectra, which are shown in Figure 5.5 proof the occurance of the photoreaction. Upon illumination two new bands appear. The first band associated with the sulfonic acid groups appears at 3480 cm^{-1} and the second one appears at 3250 cm^{-1} that corresponds to the NH-stretching of the imid-group. The CO stretching shifts from 1750 cm^{-1} to 1710 cm^{-1} upon illumination.[28] Also here, to exclude that a

heating of the film (e.g., during pentacene evaporation) has any consequence on its composition, PHDBD films heated to 100°C for 1h were investigated, but again no changes in the IR-spectra were observed.

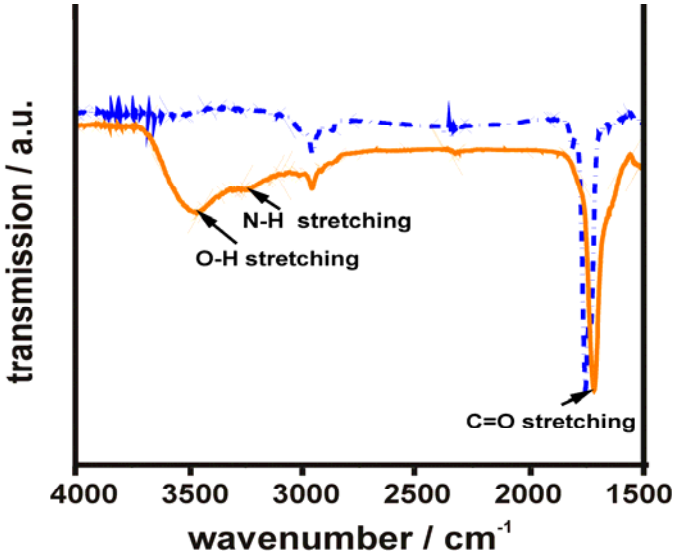

Figure 5.5) IR spectra of a PHDBD layer spincast onto a silicon wafer before (orange line) and after (blue dots) UV-illumination.

5.2.4) X-ray reflectivity measurements

Again different concentrations of PHDBD in THF were evaluated and a linear relation was observed (data not shown here). A 4 mg/ml solution resulted in films of about 16 nm thickness. Figure 5.6 shows the single XRR measurements of a not illuminated PHDBD film (top left) and the result for an illuminated layer (top right). At the bottom part of this figure both results are plotted into one graph for easy comparison. Concerning layer thickness and roughness there is no difference between those two layers.

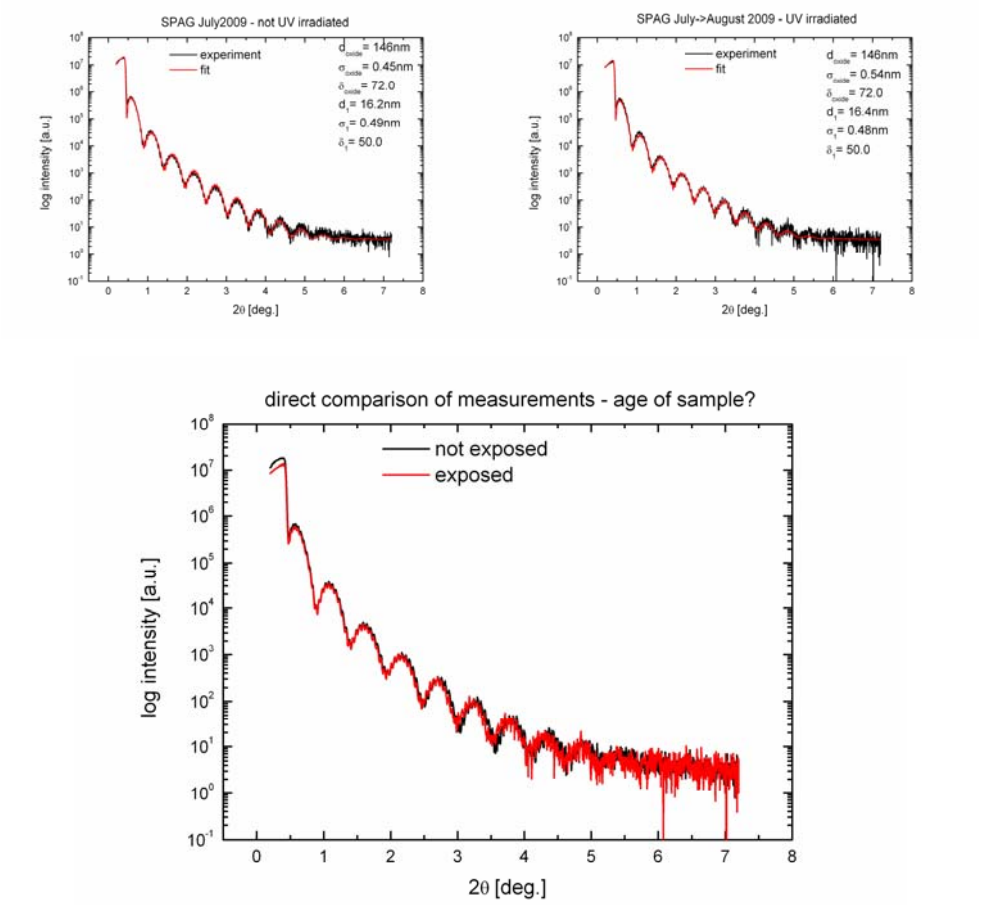

Figure 5.6) XRR curves of PHDBD layers spincoated from a 4mg/ml solution in THF before (top left) and after illumination (top right). A layer thickness of around 16 nm is observed, which stays constant in spite of the illumination. In the bottom part of the figure both results are plotted into one graph.

5.3) Experimental details

The OTFT preparation steps are similar to those described in the previous chapter, but this time there was no illumination step between the spin coating of the polymers and the pentacene deposition. After deposition of the gold source and drain contacts devices were measured, then illuminated and so on. For the post-growth illumination, the PBHND TFTs were illuminated for a time between 1 s and 300 s with an intensity of I_{UV} = 3 W/cm^2 with an EFOS (now EXFO, Mississauga, Canada) Novacure lamp. PHDBD TFTs were illuminated for 1 to

60 s with a 100 W polychromatic medium pressure mercury lamp from Heraeus (Hanau, Germany) in a Newport (Irvine, USA) model 66990 housing. For the latter experiments, the light intensity (power density) at the sample surface was measured with a spectroradiometer (Solatell (Stroud, UK), Sola Scope 2000TM, measuring range from 230 to 470 nm). The integrated power density for the spectral range 230nm-400 nm was 20.9 mW/cm². Two different lamps had to be used because of the different wavelength that was needed for the photoreaction. The devices were characterized immediately after the illumination in an argon glove box (no through air transport) with a Parametric Analyzer (Agilent Technologies (Santa Clara, USA) – E5262A).[29] This is another difference to the experiments of the last chapter since there all device were transported through air before they were characterized. Threshold voltages are extracted from the low-voltage (i.e., saturation) regime of the transfer characteristics as this is the voltage region most relevant for the inverter characteristics.[30] This is useful here in spite of the issues arising from carrier-density dependent mobilities. For the fabrication of the inverters, the devices were illuminated directly in the argon glove box. The wiring was performed externally through two Parametric Analyzers (HP4145, mb technologies (Grosswilfersdorf, Austria)). This was necessary, as substrates with common gate structures were used, due to which the switch and load transistor had to be fabricated on different substrates. There is, however, no fundamental reason, why the two transistors cannot be fabricated next to each other on the same substrate, with a photo tuning of V_{Th} of the load transistor through a mask, when patterned gate structures are available.

5.4) Electrical Characterization of OTFTs

5.4.1) OTFT characteristics

The results in Figure 5.7 show that varying the illumination time indeed allows tuning the threshold voltage over several volts by increasing the UV-illumination time from 0 to 5 seconds in a PBHND containing OTFT. The shape of the

curves is essentially the same for the different illumination times; especially the slopes (and thus the mobilities) of the OTFTs remain constant. Also the drain current in the output characteristics (Figure 5.8) increases with illumination consistent with an increased channel doping. The hysteresis of the transistors becomes somewhat larger but remains small even after 5 s of illumination (ΔVG = 2 V at ID = 0.10 mA). Also the off-current remains in the range of nA and hardly changes by the UV treatment. The devices, for which the data are shown in Figure 5.7 were kept in an argon glove-box throughout all process steps – so no detrimental effects due to contact with O_2 or H_2O did occur.

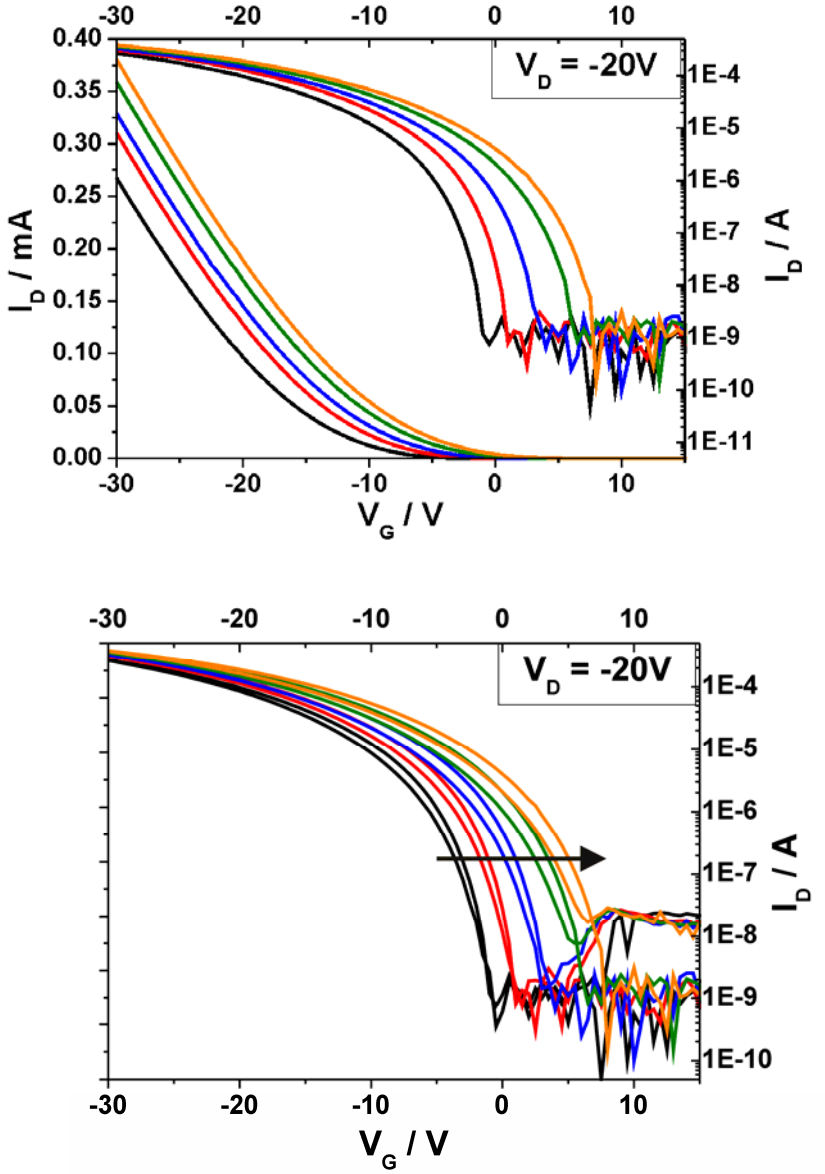

Figure 5.7)Transfer characteristics at V_D = -20 V of one series of pentacene/PBHND OTFTs for different illumination times: ■ unexposed, ■ 2 seconds, ■ 3 seconds, ■ 4 seconds, ■ 5 seconds. The arrow indicates the direction of longer illumination times. Top: linear und logarithmic transfer characteristics without hysteresis. Bottom: logarithmic transfer characteristic with hysteresis.

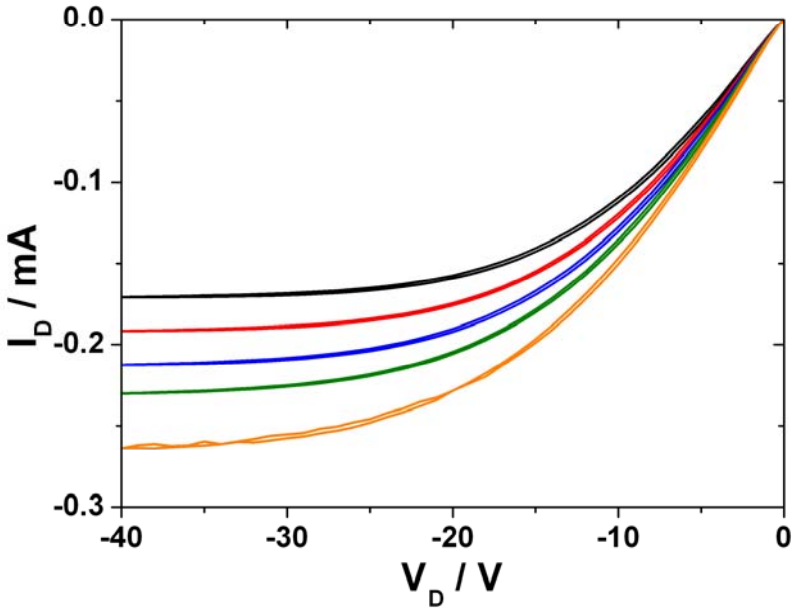

Figure 5.8) Output characteristics corresponding to the transfer characteristics in Figure 5.7.

While the V_{Th} shifts shown in Figure 5.7 are sufficient for the realization of a depletion load inverter (vide infra), we have also explored the impact of longer illumination times (see left part of Figure 5.9). The time-scales for illumination cannot be directly compared, as different lamps with different emission spectra had to be used for the two different polymers, The observed threshold voltages changes reach close to 50V both for PBHND and PHDBD interfacial layers. However, the threshold values without illumination differ significantly between the two photoacid generator polymers (only the PBHND devices are actually switched from enhancement to depletion mode operation).

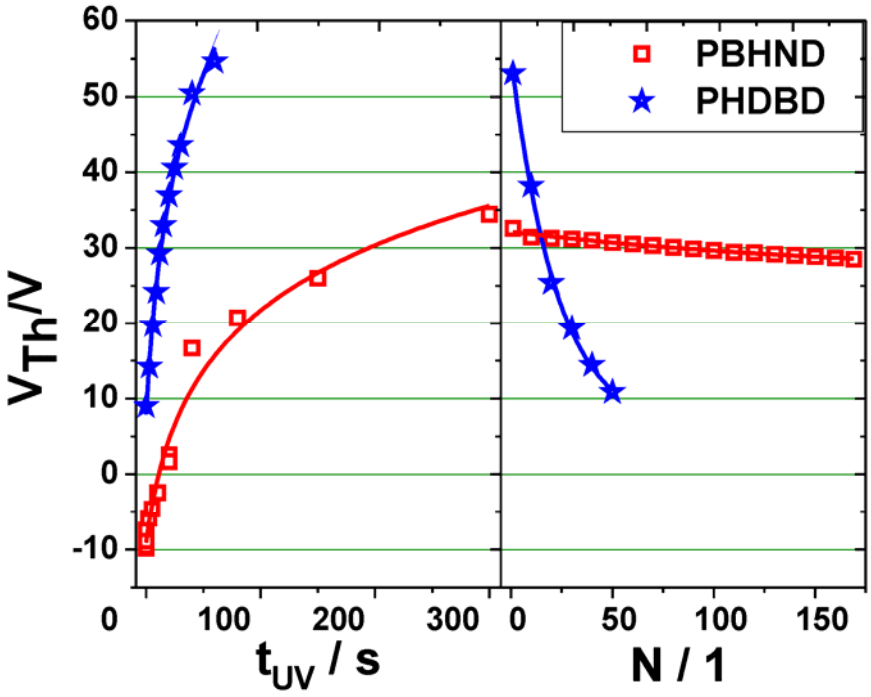

Figure 5.9) left: Evolution of the threshold voltage as a function of illumination time for OTFTs containing PHBND (open, red squares) and PHDBD (filled, blue stars) interfacial layers. Note that two different lamps had to be used for the two polymers because of their different absorption spectra (see Methods section). The logarithmic fit is a guide to the eye; right: Stability of the threshold voltage shift in PHDBD- and PHBND-containing OTFTs as a function of the number of measurement cycles. The measurements have been performed at varying time intervals. The fact that still a smooth curve is obtained indicates that only the measurement cycle itself adversely affects the device characteristics, i.e., the decrease of Vth is essentially a bias stress effect. For the sake of clarity a symbol is plotted for only every tenth measurement point. The exponential fits are guides to the eye.

When taking a closer look at devices that were illuminated for longer times a couple of additional (mostly detrimental respective to device performance) effects appear. Figure 5.10 (PBHND) compares a non-illuminated device with a device that was illuminated for 300 seconds. Figure 5.11 shows an illumination series for the PHDBD devices (ranging from 0 to 60 seconds). Note that every plot depicts a pentacene TFT with a **different** interface polymer.

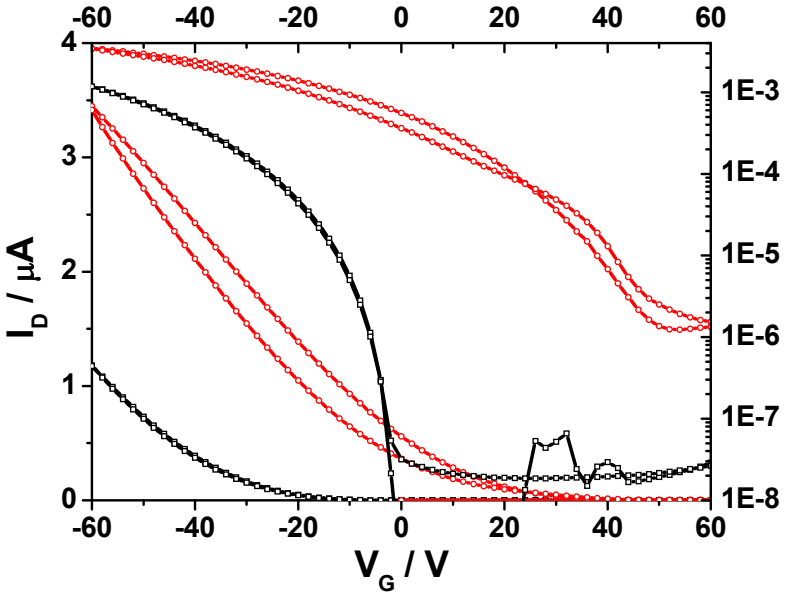

Figure 5.10) Transfer curves of a non- illuminated PBHND TFT (black curve) and a PBHND TFT that was illuminated for 300 seconds (red curve) measured at VD = -45 V. The slightly higher off-currents compared to Figure 5.7 are attributed to an exposure of the current devices to air during the fabrication process, which has been strictly avoided for the devices in Figure 5.7 and for the inverters described later.

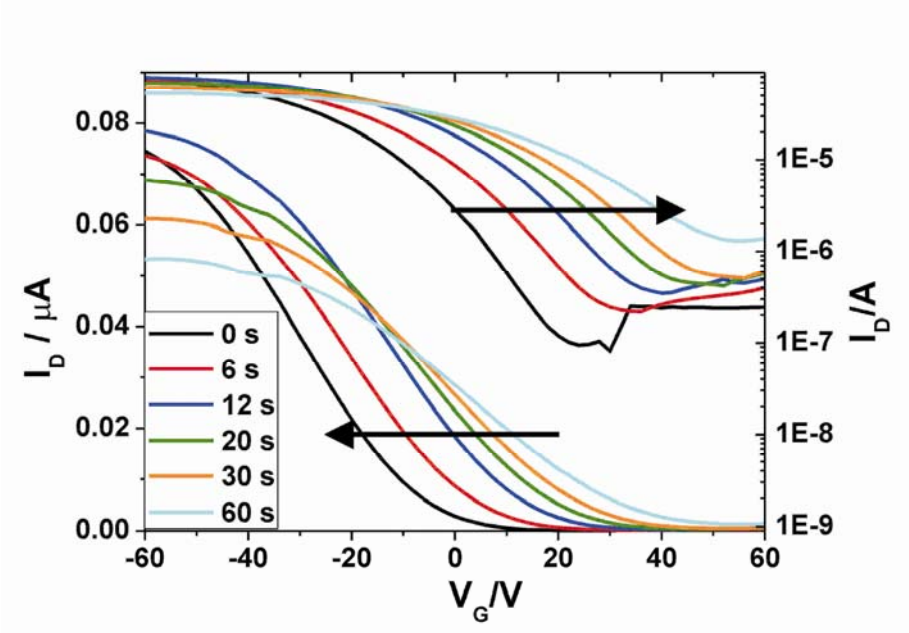

Figure 5.11) Transfer characteristics at V_D = -45 V of one series of pentacene/PHDBD OTFTs for different illumination times. The arrows indicate the direction of longer illumination times. Hysteresis again is omitted to increase visibility.

When looking at the transfer curves in those two plots, the following effects can be identified.

- *Increase of the off-current for long illumination times (Figure 5.10 & Figure 5.11):*

The increase of the off-current is accompanied by an increase of the gate leakage current. Possibly, the UV-illumination damages the $Si0_2$ dielectric.

- *Increase of the subthreshold swing (Figure 5.10 & Figure 5.11):*

When looking at the transfer characteristics plotted with a logarithmic scale in those two figures, one sees on the first glance that the slope decreases with increasing illumination time. This slope measured in Volts/dec is the so called subthreshold swing. Following equation 5.2 of Unni et al.[31] the upper limit of the trap density N_{max} can be related
to the subthreshold swing.

$$N_{max} = [\frac{qSlog(e)}{kT} - 1]\frac{C_{Ox}}{q} \qquad \textbf{(5.2)}$$

Here, q is the electronic charge and S the subthreshold swing in V decade-1. k is Boltzmann's constant, C_{ox} the capacitance per area of the gate dielectric and T the temperature.
This implies that the increased sub-threshold swing for long illumination times is the consequence of a formation of traps through the illumination with UV-light.

- *Increase of hysteresis (Figure 5.11a):*

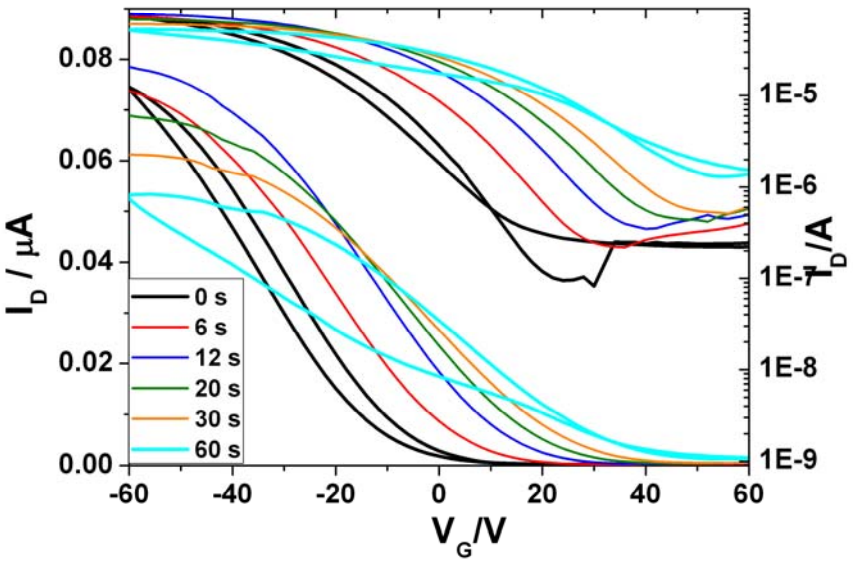

Figure 5.11a) Transfer characteristics at V_D = -45 V of one series of pentacene/PHDBD OTFTs for different illumination times. The arrows indicate the direction of longer illumination times. Hysteresis was plotted for a not illuminated device and for the device with the longest UV-exposure. It increases dramatically.

Figure 5.11a again shows the same measurements as plotted in Figure 5.11, but this time also the on-to-off sweep is plotted for the not illuminated TFT and for the TFT illuminated for 60 seconds, to show the dramatically increasing

hysteresis. The hysteresis and the off-current increase dramatically with increasing UV-illumination time. (ΔVG = 25V at ID = 0.04 mA after 60 seconds of illumination) The effect of hysteresis in OTFTs can also be associated with hole traps.[32] Thus, the increase of the hysteresis with increasing illumination time can also be explained by the photogeneration of traps in the semiconductor or at the surface of the gate dielectric.

- *Decrease of the on current for long illumination times in the case of PHDBD devices (Fig. 5.11):*

The sudden decrease of the on-current at high negative gate voltages has been described earlier[33,34] and was explained by a continuous increase of the contact resistance. Possibly, the illumination with UV light (in this special spectral range) has an adverse effect on the contact between gold and pentacene. Alternatively this effect could also be explained by mobility degradation. This means that with increasing gate voltages more and more charge carriers are forced to the first monolayers of the semiconductor, where the growth of pentacene is worse than in a bigger distance from the dielectric surface.

These effects, however, play a role only for illumination times far beyond the 3 s needed for the optimum inverter operation.

The biggest difference between the two polymers appears when looking at the stability of the threshold voltage shift, as a function of the number of measurements after the last illumination (right plot in Figure 5.9).
For the PBHND-based OTFTs, even after more than 200 measurements the threshold voltage has not shifted back considerably. The small decrease during the first measurements is mostly due to a decrease of hysteresis in these devices. The hysteresis is at least in part a result of the need to briefly transport the devices through air before the illumination (which again happened under inert atmosphere). One also has to keep in mind that the chosen measurement range for the device characteristics (from -60 V to 60 V) induces a significantly larger amount of bias stress than in any inverter-based application. The small

offset between the final data point in the left plot and the first data point in the right plot is a consequence of using devices on different substrates. In contrast to the pentacene/PBHND-TFTs, TFTs built onto the PHDBD surface do not show a stable threshold voltage shift. From measurement to measurement a decrease of V_{Th} can be seen. After only 50 measurements the shift completely vanishes and illuminated device have the same threshold voltage as devices that were not illuminated. The difference in device stability for the illuminated PBHND and PHDBD containing devices can be attributed to the different positions of the acids formed in the photochemical process. As mentioned above, in PBHND the acid is linked directly to the polymer backbone, while it is on the leaving group in PHDBD.

All measurements (threshold voltage shift and stability) for the PHDBD devices have been reproduced for several samples. The PHBND measurements have been reproduced for two batches of freshly synthesized polymer and for various samples within one batch.

To verify that the observed effects are indeed a consequence of interfacial acid doping, we have performed two test experiments. First, we exposed the devices to a strong base (NH3 as in Refs. [25, 26]). As can be seen in Figure 5.12 this treatment results in a neutralisation of the acid, i.e., a dedoping of the channel and after 10 minutes of exposure to ammonia the devices were switched back to a situation similar to that prior to UV exposure.

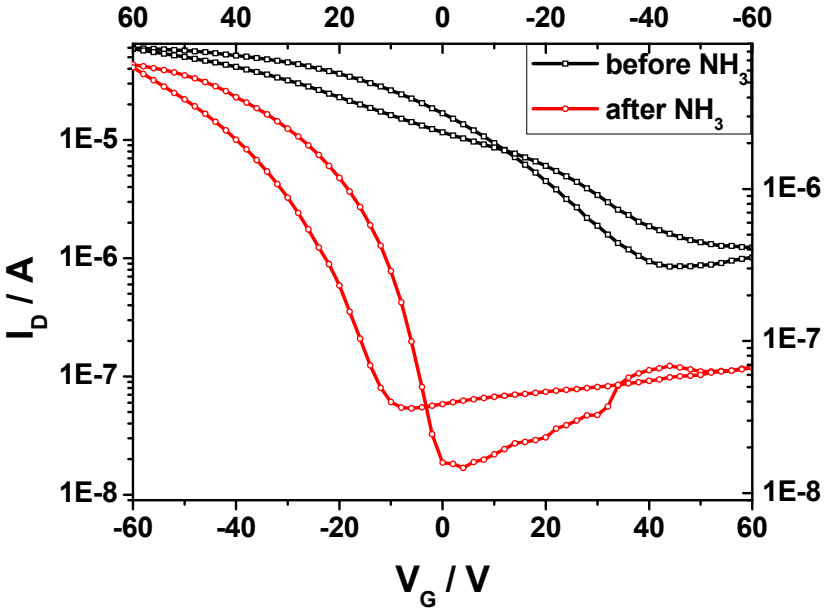

Figure 5.12) Transfer curves for a PBHND OTFT before (black line) and after (red line) the reaction with ammonia.

As a second test, shown in Figure 5.13, we also illuminated devices containing no interfacial layer. Here, even after 20 minutes of UV exposure no changes in the transfer and output characteristics were observed.

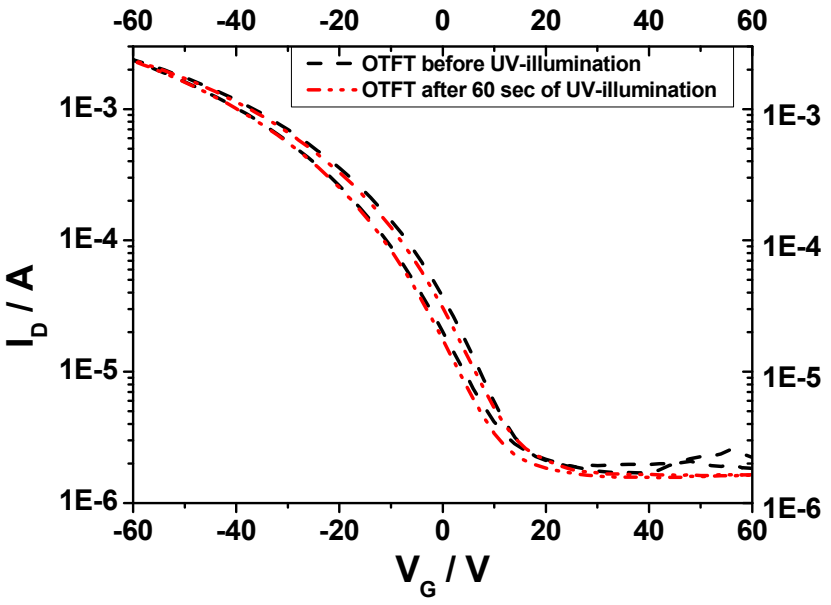

Figure 5.13) Transfer curves for a pentacene OTFT, without any interface modification before and after illumination with UV-light stemming from the EFOS Novacure lamp The higher off-currents compared to Figure 5.7 are again attributed to an exposure of the current devices to air during the fabrication process, which has been strictly avoided for the devices in Figure 5.7 and for the inverters later on.

This provides us with all the tools necessary to perform the next step in the direction of integrated p-type organic electronic devices, which is the fabrication of a (tuneable) depletion-load inverter.

5.5.) Characterization of the depletion-load inverter

The wiring diagram of such an inverter is replotted as an inset of Figure 5.14. The switch transistor is realized by a non-illuminated PBHND-containing device that has a negative threshold voltage of around V_{th}= – 10 V. The load transistor (also a device containing a PBHND interfacial layer) was illuminated in steps of 1s in an argon glove-box after the inverter wiring had been realized.

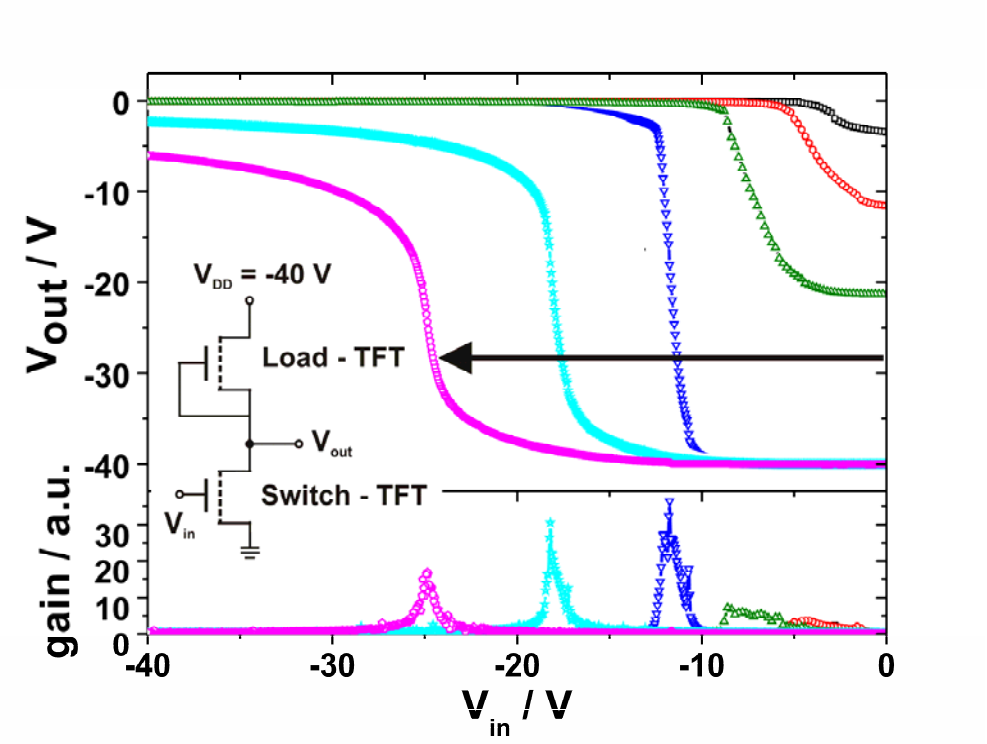

Figure 5.14) top) Inverter characteristics with differently (for 0,1,2,3,4 and 5 seconds) illuminated load-TFTs; the arrow shows the trend for increasing illumination times; bottom) the corresponding gains of the inverters; inset: wiring diagram of a depletion-load inverter.

As can be seen in Figure 5.14, the inverter characteristic is very poor prior to illumination, the gain of the inverter is negligible and the reachable output voltage at the low level is only -4 V. This is because the non-illuminated load transistor is normally-off and works in enhancement mode. By increasing the illumination time of the load transistor and shifting its threshold towards the positive voltage regime, the inverter characteristic improves significantly. The turn-on voltage of the inverter is shifted to more negative values and the gain of the inverter increases. After illuminating the load transistor for 3s, an optimum value of $V_{th,load}$ with respect to the threshold voltage of the switch-transistor is reached resulting in a steep inverter transition with a maximum gain of about 40 (see bottom graph in Fig. 5.14). Further increasing the illumination time results in a deterioration of the inverter performance. At this point it should be

noted that we did not make any attempts for optimizing the inverter characteristics other than tuning $V_{Th,load}$. Therefore, further significant improvements can be expected by adapting the W/L ratio between load and switch and by optimizing the performance of individual transistors with respect to mobility, gate leakage etc.

5.6) Conclusion

In conclusion, an easy and reproducible way to switch OTFTs from enhancement to depletion mode by a photochemical reaction using photoacid generators as interfacial layers is shown, and it is demonstrated that this allows the fabrication of good quality depletion-load inverters with tuneable characteristics. The suggested fabrication method can easily be adapted to monolithically integrated circuits by illuminating individual transistors through shadow or photo masks, when patterned gate electrodes are used (in this way simultaneously reducing leakage and parasitic effects).

5.7) References

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All great deeds and all great thoughts have a ridiculous beginning.
Great works are often born on a street corner or in a restaurant's revolving door.
Albert Camus

VI) Temperate Dependent Device Characterization of Pentacene OTFTs with different interface modifications.

Preface

In chapter 4 the room temperature mobility and the temperature dependence of the mobility was changed through differently long UV-illumination times of the interfacial photoreactive layer. In this chapter the main focus lies on the temperature dependence of the mobility and of other device parameters. Additionally the impact of different interface modifications, like reactive and non-reactive self assembled monolayers and non reactive polymers, on the temperature dependence of these parameters is investigated But before presenting results for the temperature dependent measurements an extended overview of literature will be given in the introduction of this chapter.

Following this introduction pentacene OTFTs with differently modified interfaces between the gate oxide and the semiconductor have been produced. At first there will be a short introduction of the known properties of each molecule used for interface modification. Every single layer has been characterized by all means possible in our lab environment (XRR, AFM) and afterwards TFTs have been built with 50 nm of pentacene and 50 nm of gold source and drain contacts (channel length = 50µm and channel width = 7mm) to fit in the cryostat specimen holder. At first, the devices have been measured at room temperature already in the vacuum of the cryostat after a brief transport through air in the dark. Transfer curves were measured for all interface modifications. Their main differences will be discussed. Then temperature dependent device properties were measured in the cryostat. The cooling was done with liquid helium, so in theory temperatures down to 3.2 K should be feasible. In reality the lowest reachable temperature turned out to be 25 K. For most of the devices, this was

no real drawback because the transfer curves at those low temperatures did not allow the extraction of reliable device parameters anyway. It should also be mentioned here that all measurements, which are presented in this chapter, were done during one week. Since liquid helium is not easily available and extremely expensive devices had to be measured in short succession and no big changes in the whole experimental setup were possible. This is the reason why not all open questions could be answered and some data had to be recorded under non-perfect conditions. Additionally, it should be noted that during these measurements the contact resistance between the Au electrodes and the semiconductor pentacene was not regarded. For the extraction of the contact resistance one would need devices of the same type with different channel lengths. During the measurements discussed here, all devices had the same channel length of 50 µm. Since the contact resistance is a very important parameter the next two chapters will primarily deal with its theory, its extraction methods and with measurements of it.

6.1) Introduction:

Whenever one is interested in OTFTs not only from the technological point of view, but also wants to study the fundamentals of charge transport processes in organic semiconductors, temperature dependent measurements of organic transistors[1] are the method of choice. It was already discussed in the second chapter of this work that transport in organic semiconductors is thermally activated, but we will discuss this topic in more detail here.

First of all, the relation between mobility and temperature naturally depends on the organic semiconductor material used for transistor production.[2,3,4,5,6] Since throughout this work only pentacene was used as active material, we will describe solely this material. Additionally, it makes a strong difference if the material used for FET-operation is polycrystalline or a single crystal.[7,8,9,10] In the case of pentacene, there exist numerous

papers that focus on the charge transport properties of a pentacene single crystal.[11,12] Since in this work only polycrystalline pentacene was used, we will focus on literature on this material. For the sake of completeness, the main differences between single crystal- and polycrystalline pentacene[12,13,14] are summed up in Figure 6.1.

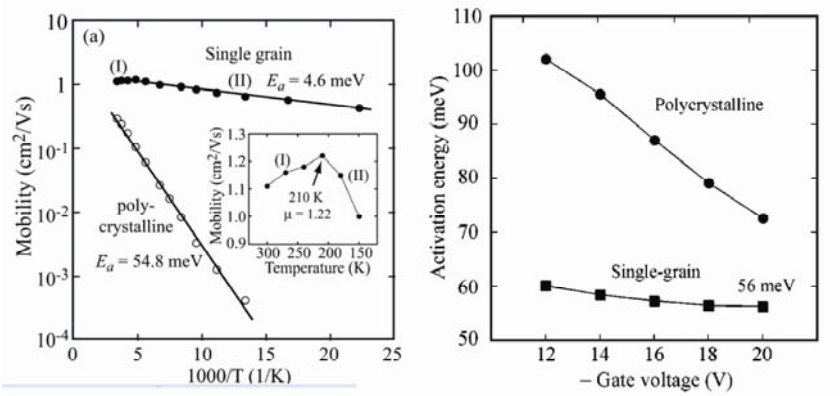

Figure 6.1) left) Arrhenius plots of single-grain and polycrystalline pentacene OTFTs within the temperature range of 300 to 45 K, taken from Reference 14. right) Activation energies (as extracted from the Arrhenius plots) for the field-effect mobility as a function of the gate voltage taken from Reference 13.

As can be seen in Figure 6.1 the charge carrier mobility is much higher in the case of single-grain OTFTs and it also decays much more slowly with decreasing temperature. When describing OTFTs with the multiple trapping and thermal release model (MTR) - already presented in chapter 2 through Equation 6.1

$$\mu = \mu_0 \exp\left(-\frac{E_A}{k_B T}\right), \qquad \textbf{(6.1)}$$

this results in a higher activation energy for polycrystalline devices.

Additionally, this activation energy is almost independent of the gate voltage for a single-grain OTFT. In a single crystal one is also dealing with a significant anisotropy of the mobility.[15]

Even in the case of polycrystalline vacuum evaporated pentacene, the quality of the pentacene film and thus the mobility in an OTFT is very sensitive to parameters like temperature, pressure, deposition rate, chemical purity and the substrates surface condition.[16] This sensibility on the production conditions led to various results of a thermally activated,[17] a thermally independent[1] and finally a thermally deactivated[18],[19] mobility in pentacene polycrystalline transistors. In fact most authors in literature agree upon the fact, that the charge carrier transport in pentacene OTFTs is thermally activated, but in Reference 19, Nelson et al. claim to have found a high mobility pentacene TFT (with silicon gate and Au source/drain contacts), whose overall mobility increases by a factor of two in the temperature range from 300K to 10 K. In the same set of devices they also find TFTs with "normal" thermally activated behaviour. Also in the high temperature region Sekitani et al.[18] present temperature deactivated behaviour for temperatures above 80°C. Horowitz et al.[1] also describe a temperature range (from 40K to 100 K), where the mobility is totally independent of the temperature in polycrystalline oligothiophene TFTs.

To make things even more complicated, the performance of the transistor additionally depends on the used dielectric (as shown in the previous two chapters), on the used geometry[20] (top contact vs. bottom contact) and on the thickness of the pentacene layers.[21]

In the following the polycrystalline transport model, which has already been introduced in chapter 2, will be used to discuss the temperature dependence of polycrystalline pentacene OTFTs. We will give an overview about experimental findings in literature and will present some known literature values for the room temperature mobility and the activation energy in pentacene OTFTs. Afterwards also the temperature dependence of the threshold voltage and of the hysteresis (as known from literature) will be discussed.

For the dependence of the mobility on temperature Horowitz found following experimental relationship for oligothiophenes. (Figure 6.2) In this case the mobility was calculated through the channel conductance method ($g_d = \frac{\partial I_D}{\partial V_D} \approx \frac{Z}{L}\mu C_i (V_G - V_{Th})$ for low drain voltages in the saturation region.

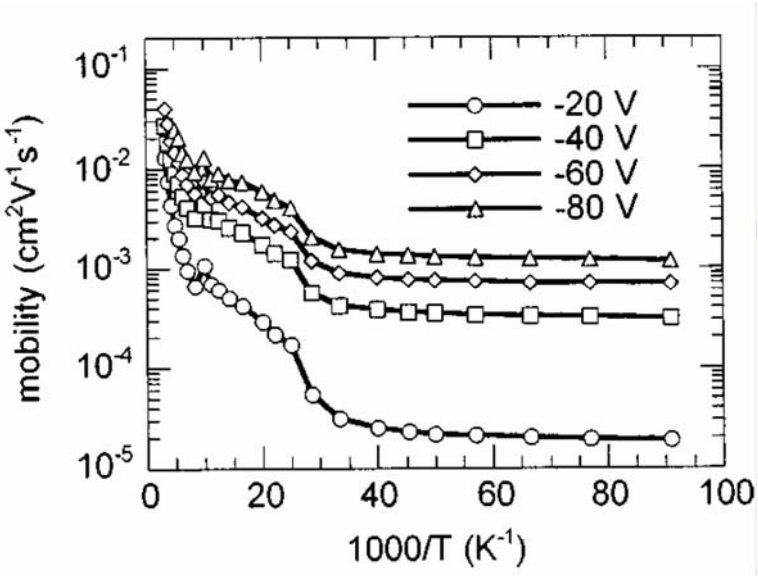

Figure 6.2) Arrhenius plot of the temperature dependent mobility of polycrystalline sexithiophene. The different curves correspond to different gate voltages. This plot was taken from Reference 1.

The curves in Figure 6.2 can be analyzed as follows. In the high temperature region (ranging from 300 to 100 K), where the current between grains is limited by thermionic emission, the mobility is thermally activated with an activation energy around 0.1 eV. At extremely low temperatures below 25 K temperature independent tunnel transfer through the grain boundaries is dominant. At intermediate temperatures, thermally activated tunnelling takes place, which has a smaller activation energy in comparison with the activation energy for thermionic emission.

For polycrystalline pentacene in literature most of the time only one activation energy is extracted and no hint of a temperature independent mobility at very

low temperature (below T = 100K) is given. An exception is the work of Kang et al.[25] Figure 6.3 shows the temperature dependence of the mobility of pentacene TFTs in a temperature range of 300K to 15K. They identify Arrhenius like behaviour down to 100 K and temperature independent behaviour for lower temperatures.

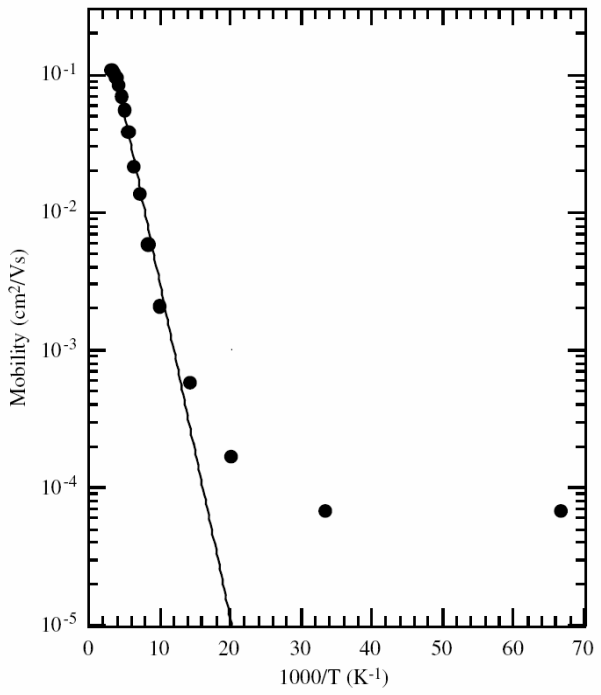

Figure 6.3) Temperature dependence of the field-effect mobility of a pentacene TFT in the temperature range of 300 K to 15 K, showing the thermally activated mobility in the temperature range T>100 and a thermally independent mobility at lower temperatures taken from Reference 25.

There is no indication for the intermediate region of thermally activated tunnelling of the charge carriers as shown in Figure 6.2 for thiophene. The explanation for the two observed regions are the same as in the work of Horowitz. (thermionic emission and tunnelling)

6.1.2) The temperature dependence of mobility

Table 6.1 sums up the experimental values for the activation energy of polycrystalline pentacene OTFTs. Please note that the composition of the TFT regarding dielectric and electrodes was different in all cases and also the calculation of the mobility followed different methods. In the following a short overview about the TFT composition and the mobility evaluation methods for each paper will be given:

Reference 13: silicon gate, 120 nm of SiO2, Au source/drain electrodes; 25 nm pentacene vacuum sublimated at 353 K, channel conductance method in the saturation regime

Reference 16: silicon gate, 300 nm of SiO2, Au source/drain electrodes, pentacene vacuum sublimated at room temperature: channel transconductance method in the linear regime

Reference 25: ITO gate, 922nm PVP as dielectric, Au source/drain electrodes, 100 nm pentacene; mobility calculated through the slope of the transfer characteristic in the saturation regime

Reference 26: silicon gate, 200nm auf SiO2 as dielectric, Au source/drain electrodes, 30-50 nm of pentacene (precursor spincoated from solution), transconductance method in the linear regime.

Reference 27: silicon gate for all devices: pentacene deposited by organic molecular bean deposition. mobility calculated through the slope of the transfer characteristic in the saturation regime

Charge 1: 200nm SiO2 dielectric, Au source/drain electrodes

Charge 2 : 500nm PVCN dielectric, PEDOT source/drain electrodes

Table 6.1 Activation energy for the mobility in polycrystalline pentacene OTFTs. Values taken from References 13, 16, 25, 26, 27 T_{high} and T_{low} are the highest and lowest temperates at which the mobility was evaluated. μ_{RT} is the charge carrier mobility at room temperature, is the highest gate voltage at which the mobility was evaluated and EA is the resulting activation energy of the mobility following equation 6.1. The last column labelled Ref. gives the reference to the paper where the data was taken from.

T_{high} / K	T_{low} / K	μ_{RT} / cm²/Vs	V_G / V	E_A / meV	Ref.
320	70	0.5	-30	54,8	13
318	298	0.33	-50	72,0	16
300	100	0.15	-80	49	25
320	170	0.01	-30	100	26
300	100	0.0023	-30	130	27
300	200	0.0022	-30	330	

6.1.3) The temperature dependence of the threshold voltage.

Less information on the temperature dependence of OTFT parameters other than the mobility can be found in literature.

Horowitz published a slight increase of the threshold voltage (evaluated by the extrapolation in the saturation regime method)with decreasing temperature for his oligothiophene TFTs,[1] as can be seen in Figure 6.4. His explanation for the temperature dependence of the threshold voltage is, that with decreasing temperature more injected charged are required to fill the traps in the semiconductor.

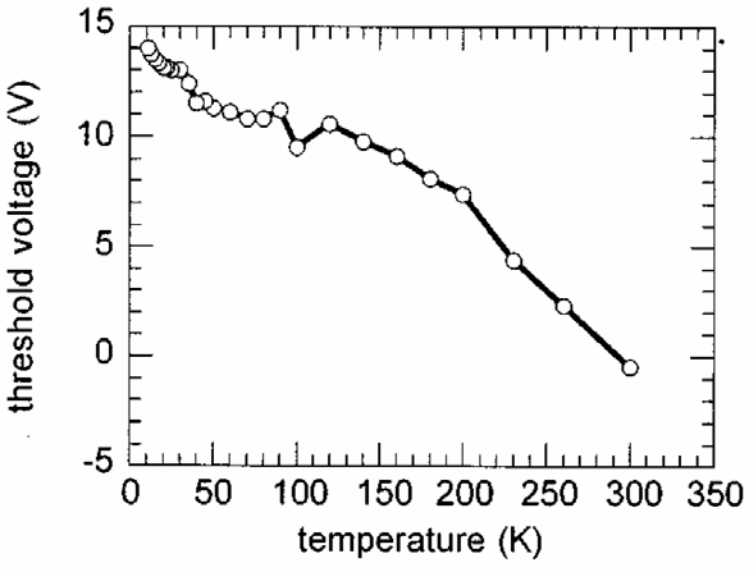

Figure 6.4) Variation of V_{Th} of a polycrystalline sexithiophene TFT as a function of temperature taken from Reference 1.

The first observation of a temperature dependence of the threshold voltage in polycrystalline pentacene transistors is again the paper of Kang et al.[25] Their results are shown in Figure 6.5. and they claim that the reason for this behaviour is an increase of the trapping of charges at localized states at low temperatures.

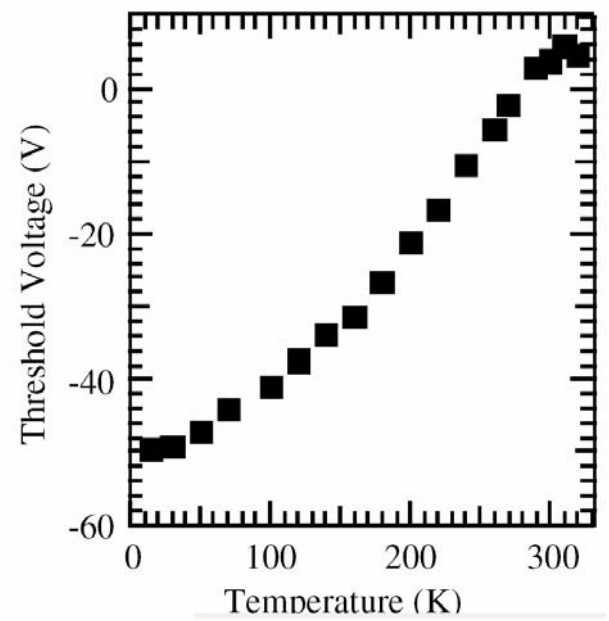

Figure 6.5) Temperature dependence of V_{Th} taken from Reference 25.

In 2010 finally a consistent and unified explanation for the thermally activated transport in polycrystalline pentacene and the decrease of threshold voltage with decreasing temperature was presented.[28] In the paper of Letizia et al. seven different organic semiconductors (including p-type, n-type and ambipolar semiconductors) were analyzed over a broad temperature range. Figure 6.6 shows the temperature dependence of mobility and threshold voltage for all those materials, proofing that the phenomenon of a temperature dependent threshold voltage is a common effect for a lot of organic semiconductors. Both parameters have been calculated in the saturation regime, with the same methods that are used in this thesis.

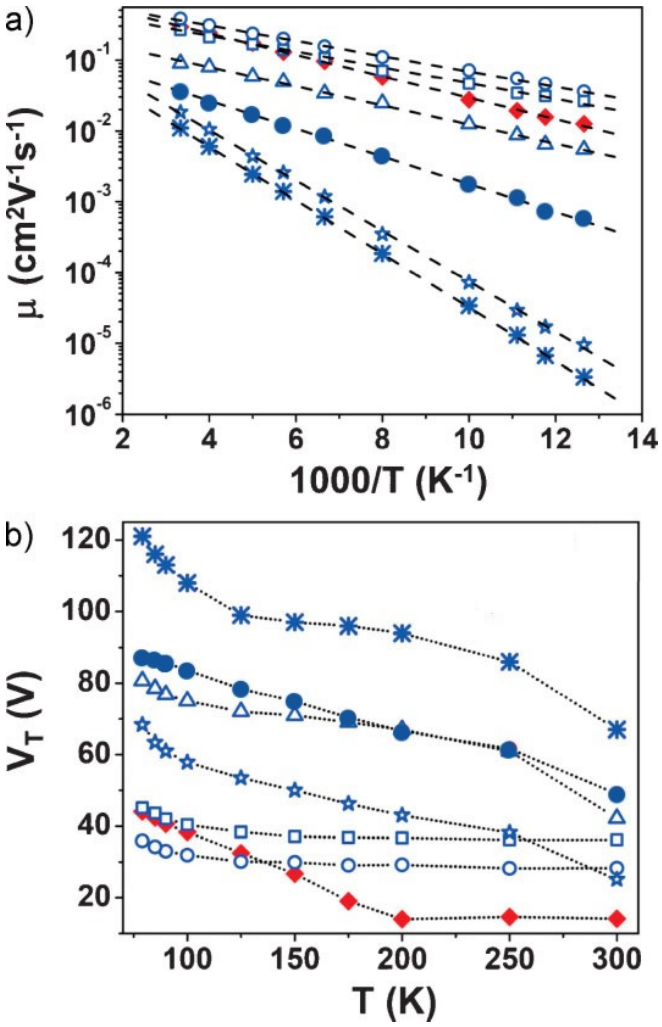

Figure 6.6) red dots correspond to the values for pentacene; a) plot of the temperature dependence of mobility. the dotted line is a least-square fit to the Arrhenius relation; b) threshold voltage as a function of temperature (in the case of pentacene the absolute value is plotted); the dotted line is a guide to the eye. The other materials of this study include

○ 5,5-bis(perfluorophenacyl)-2,2:5,2:5,2-quaterthiophene,

□ 5,5-bis(perfluorohexyl carbonyl)-2,2:5,2:5,2-quaterthiophene,

Δ 5,5-bis(hexylcarbonyl)-2,2:5,2:5,2-quaterthiophene,

● 5,5-bis-(phenacyl)-2,2: 5,2:5,2-quaterthiophene,

¤ 2,7-bis((5-perfluorophenacyl)thiophen-2-yl)-9,10 phenanthrenequinone

***poly(N-(2-octyldodecyl)-2,2 bithiophene-3,3-dicarboximide) Taken from Reference 28.**

This temperature dependence of the threshold voltage can be interpreted as a definitive evidence of charge trapping and allows drawing a clear correlation between the change in threshold voltage ΔV_{Th} and the effective mobility at room temperature μ_0 defined in Equation 6.1.

The trapped charge density at room temperature can be calculated using the subthreshold swing following the famous formula of Unni et al.[29] (rewritten into a numerical value equation to follow the formalism of the paper of Letizia et al.)

$$N_{max} = \left[\frac{0.43429 q S_{STh}}{k_B T} \right] \frac{C_i}{q} \qquad \textbf{(6.2)}$$

The change in threshold voltage ΔV_{Th} can then be converted to a change of the trapped charge density ΔN_T, [30,31,32,33]

$$\Delta N_T = \frac{C_i}{q} \Delta V_{Th} \qquad \textbf{(6.3)}$$

[NOTE: Equation 6.3 was taken from the paper of Mühlenen et al. though it also appeared in the paper of Letizia at al. but written in a wrong way. They state the equation as follows: $\Delta N_T = q \Delta V_{Th} C_i$]

These two relationships allow a calculation of the trapped charge density for all temperatures.

Physically this means that with decreasing temperature charge carriers can no longer be thermally released from shallow charge traps. This leads to a locally fixed built-in field of charges, which shifts the threshold voltage.

6.1.4) The temperature dependence of the hysteresis.

Almost no information of the temperature dependence of the hysteresis in OTFTs can be found in literature especially for pentacene TFTs. The following example is taken from the work of Egginger et al.[34,35] where the temperature dependent magnitude of the hysteresis in C_{60} field effect transistors with a poly(vinylalcohol) (PVA) gate dielectric is analyzed, as can be seen in Figure 6.7.

[NOTE: it is questionable how well one can compare their results with the results obtained on pentacene TFTs, but since it is the only study that deals with the temperature dependence of the hysteresis, their results will be described anyway]

They observe that the magnitude of the hysteresis decreases with decreasing temperature. The reason given for their observations is a thermally activated motion of sodium ions in the PVA dielectric. Unfortunately the lowest measuring temperature was 253 K and no information of the development of the hysteresis for lower temperatures was given.

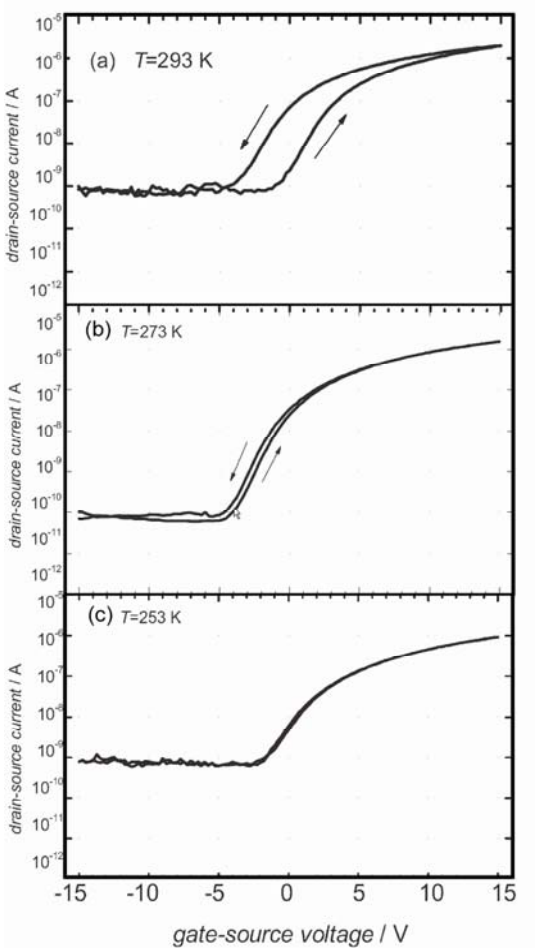

Figure 6.7 Transfer characteristics of a C60 field effect transistor for various temperatures.

6.2) Proposed model to explain the temperature dependence of the mobility, the threshold voltage and the hysteresis.

To explain for the temperature dependence of the mobility, the threshold voltage and the hysteresis at the same time, we propose the following model.
In an organic semiconductor like pentacene, there exist three energetically different kinds of traps.

- **Shallow traps:** These traps are responsible for the temperature dependence of the mobility, and their energy level (or at least the mean

value of the energy level) can be calculated through Equation 6.1. Whenever in literature a trap energy E_A is given it is this deep trap energy.

- **Deep traps:** These traps are responsible for the temperature dependent shift of the threshold voltage. With decreasing temperature more and more charge carriers are trapped and thus shift the threshold voltage to more negative values. These traps should have a much higher binding energy in comparison to the deep traps. Later when discussing the measurement results, a Boltzmann distribution will be fitted to the temperature dependence of the threshold voltage and another "activation" energy E_{ST} will be determined.
- **Intermediate traps:** Following the trapping mechanism of Ucurum et al. another type of traps is responsible for the hysteresis. These traps have an intermediate lifetime, and thus an intermediate binding energy. They are filled and emptied during one measurement cycle. Additionally it is difficult to extract a material parameter like an activation energy for these traps, since the magnitude of the hysteresis is influenced by number of measurements during one cycle and by the time for each ($I_D(V_G)$ datapoint.

Again it should be noted, that during these measurements no correction for the contact resistance is included. It should also be noted, that the assignment, whether or not a certain trap is a shallow trap or a deep one, also depends on the chosen measurement temperature. With decreasing temperature more and more initially intermediate traps "freeze out" and become deep traps, which shift the threshold voltage.

6.3) Different Interface Modifications

It is obvious from the previous section that a wide variety of different room temperature mobilities and activation energies can be extracted from the transfer characteristics in pentacene OTFTs. In chapter 4 it was shown that the

temperature dependence of the mobility strongly depends on the growth behaviour of pentacene and thus on the surface of the dielectric. In this section we now “explicitly” change the property of this surface by introducing different interfacial layers. Through these different interfacial layers we will change the growth behaviour of pentacene on this surface and therefore introduce a different amount of traps with different trap depths.

The chemical structures of the molecules chosen for the surface modification are summarized in Figure 6.8. Reference samples - so-called “plain” devices – just consist of a precleaned and O_2-plasma activated $Si0_2$ surface. T-SC/SA and Hexamethyldisilizan (HMDS) form self assembled mono (SAM) - or multilayers (SAMT) on the substrate and Parylene C is a polymer, which was chemical vapour deposited with two different thicknesses.

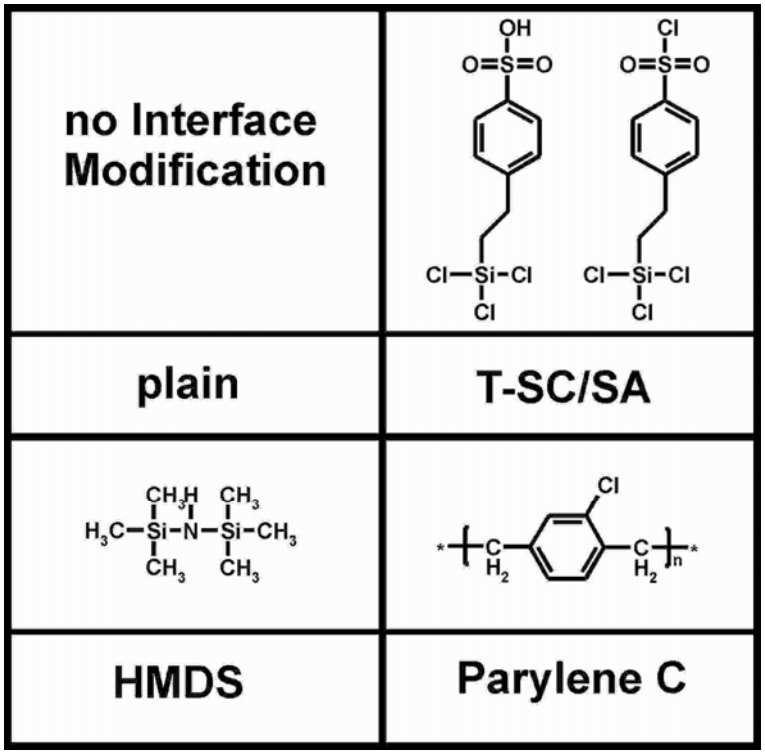

Figure 6.8) Chemical structures of the interface modifications in this chapter.

a) plain devices:

As already mentioned above, plain devices were not especially modified. They just were 0_2-plasma etched and afterwards rinsed in deionised water for 2 minutes. These steps were also performed for all other devices prior to any other interface modification.

b) T-SC/SA – SAM :

The T-SC/SA layer consists of two molecules, which form a SAM on the silicon oxide surface. The T-SC/SA molecules were purchased from ABCR GmbH & Co Kg (Karlsruhe, Germany) in a 50% solution in toluene. It consists of two different molecules, namely 2-(4-chlorosulfonylphenyl)ethyltrichlorosilane (T-SC / 70%) and its sulfonic acid analogue (T-SA / 30%). It is known to shift the threshold voltage in organic transistors[36,37,38,39], because of a doping reaction with the active layer material.

After the above mentioned cleaning steps the silicon wafers were transferred into an argon glove box where they were inserted into 10 ml toluene containing 10 µl T-SC/SA for 16 hours. After this time they were put into a fresh glass containing only toluene and were ultrasonicated for 2 minutes. This step was performed under ambient conditions. Afterwards the wafers were dried with $C0_2$ spray and annealed for 30 minutes in vacuum at a temperature of 100° C.

c) HMDS – SAM :

Hexamethyldisilizan [40] is a commercially available and vastly used surface primer in inorganic semiconductor fabrication.[41] On SiO2-surfaces it builds a self-assembled monolayer. When used in combination with organic semiconductors it is often applied to lower the surface energy of the gate dielectric or to reduce the number of charge carrier traps at the dielectric surface. These changes normally have the purpose to increase the grain size of the semiconductor and thus increase the overall charge carrier mobility.[42] The HMDS used in this work was purchased from Sigma-Aldrich with a certified purity of >99,9% and was not cleaned any further.

The procedure used for the application of HMDS was performed with a hotplate. The HMDS was stored in its liquid form in a glass vessel, while the substrates were stored in a process chamber, which can be evacuated and flooded with nitrogen. The process chamber was evacuated and heated. Afterwards, the HMDS was transported into the chamber using a carrier gas (air). After the application of HMDS the chamber was cooled down and flooded with nitrogen. More details on the HMDS application process can be found in Reference 43. The application of HMDS was performed together with A. Meingast at the NTC Weiz in the group of E.J.W. List.

d) parylene C – polymer:[44]

This polymer is often used in organic electronics as a dielectric layer[45] for OTFT applications or as an additional coating material.[46] The polypara-chloroxylylene (parylene-C)[47] films have been prepared using chemical vapour deposition (CVD) starting from the commercially available dimer dipara-chloroxylylene. After sublimation the dimer has been decomposed at 650 ◦C and deposited at room temperature as a stable polymer on the substrate. The growth has been monitored by a quartz micro balance, leading to nominal layer thicknesses of 5 and 20 nm respectively. The application of the parylene C layers was performed by Ján Jakabovič at the Slovak University of Technology in Bratislava.

6.4) Characterization of the different interfacial layers

XRR measurements yielded the average layer thickness of the different interfacial layers. All XRR measurements were performed by H. G. Flesch. The thickness of the $Si0_2$-dielectric layer was 154nm. The total thickness of the T-SC/SA-SAM was 1.04nm which approximately corresponds to the length of one molecule in its all-trans form. This indicates that a real monolayer had grown on the substrate. The two different Parylene C layers had nominal thicknesses of 5nm and 20nm, respectively. XRR measurements yielded actual thicknesses of 7.45nm and 23.7nm. The HMDS layer could not be measured by XRR, but its

existence was proofed with Contact Angle measurements. The contact angle of water changed from 45.3° for the $Si0_2$ surface to 85.1° after HMDS deposition. Concerning the roughness of the surface the values for the two parylene and the T-SC/SA layers are two times higher than the roughness of plain wafers. The XRR measurement results are summed up in Figure 6.9

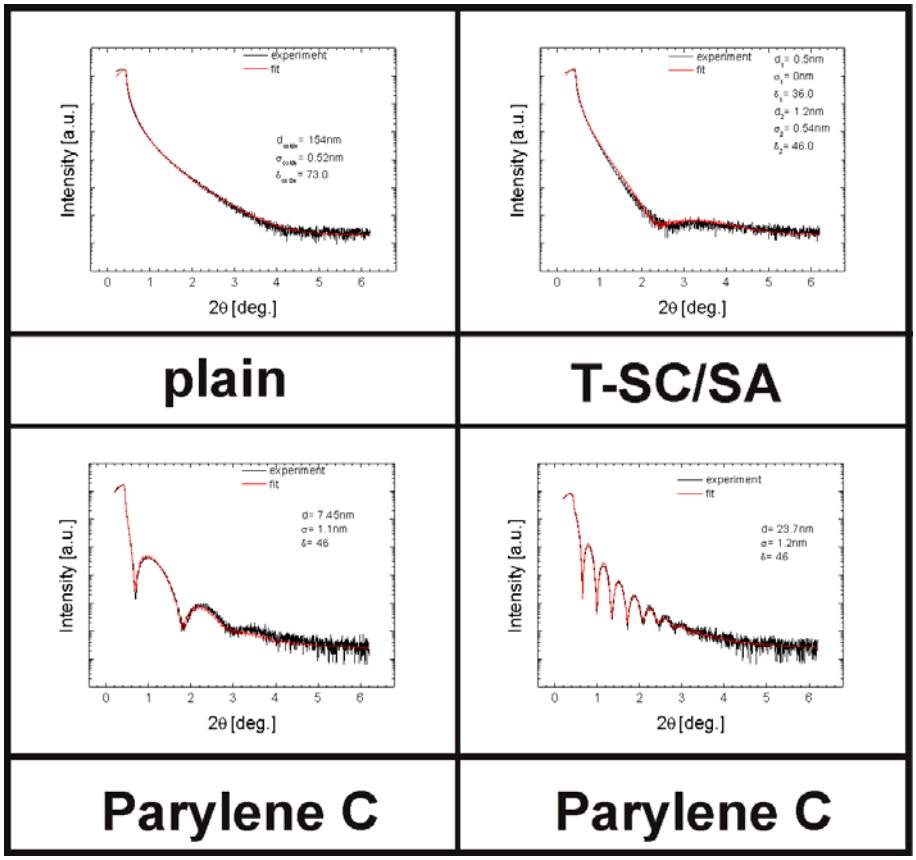

Figure 6.9) XRR measurements for the different interface layers. XRR measurements were performed by H. G. Flesch.

Additionally, AFM measurements of the interfacial layers as shown in Figure 6.10 have been performed by A. Haase at the NMP Weiz.

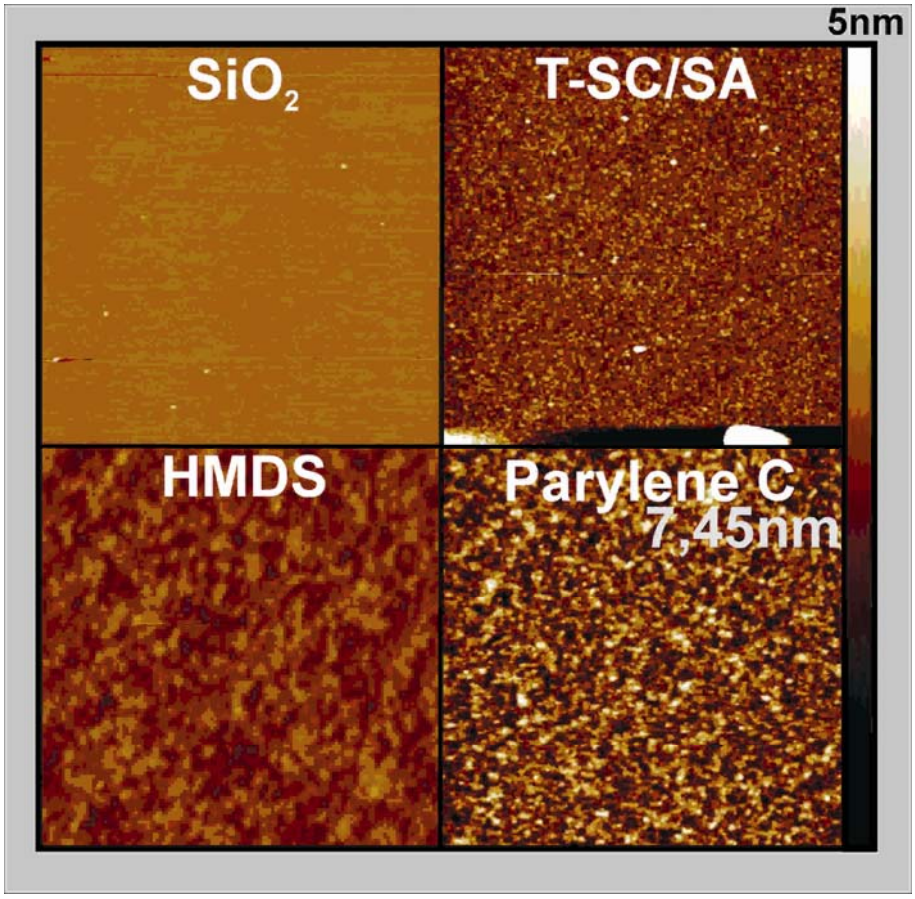

Figure 6.10) AFM measurements of the different interfaces. Every picture depicts a 5x5 µm big detail of the surface. AFM pictures taken by A. Haase.

From these pictures again the surface roughness could be evaluated. HMDS treated and plain devices yielded a much smoother surface than wafers treated with TSC/SA or Parylene C. Moreover, the roughness of the Parylene C surface did not depend on its thickness; both pictures looked the same.

Onto these interfacial layers, pentacene was vacuum-evaporated at the NMP Weiz by various coworkers and again AFM pictures were taken. Figure 6.11 shows the AFM pictures for four different interface modifications. Again there was no visible difference for the two different thicknesses of the Parylene layers. The growth of the pentacene crystallites strongly depends on the chosen interface modification. Surfaces with a high roughness like T-SC/SA and Parylene yielded small pentacene grains. On lower roughness surfaces the

pentacene grains became bigger and dendritic growth was observed. The biggest grains grow on the HMDS surface, which also has a big contact angle with water.

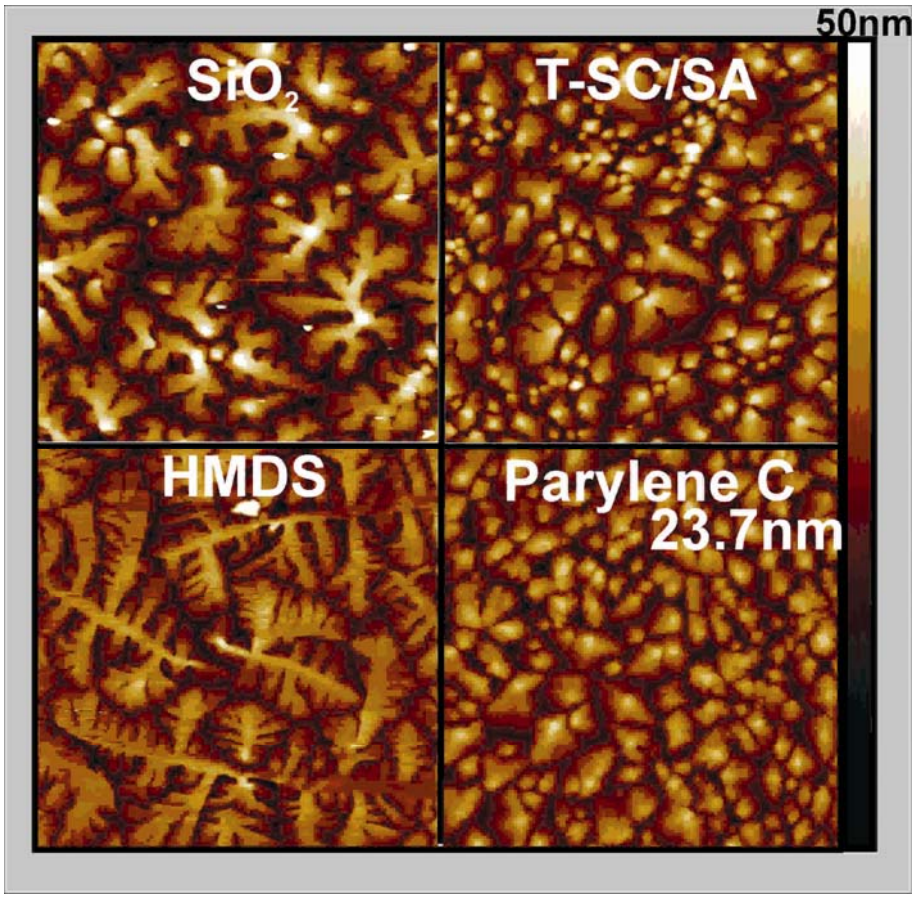

Figure 6.11) AFM measurements of the pentacene surface vacuum evaporated onto the differently modified interfaces. The $Si0_2$, T-SC/SA and Parylene C pictures depict a 5x5 µm section of the surface, the HMDS picture is 10x10 µm big. AFM pictures taken by A. Haase

6.5) OTFT characterization at room temperature.

Figure 6.12 shows typical transfer curves for the 5 different OTFTs at room temperature. In Table 6.2 all parameters are summarized. At first glance, one can see some differences between the transfer curves. The fact that probably strikes the eye first is the high threshold voltage of the T-SC/SA (blue curve) modified OTFT. While all other interface modifications lead to a slightly negative V_{Th} the T-SC/SA TFTs show positive threshold voltages. This is caused by the interfacial doping as mentioned earlier. Since the T-SC/SA layer in this case is a real monolayer the transfer curve is only shifted by around 20 V. Another phenomenon - also common for T-SC/SA TFTs - is the high subthreshold swing. This high subthreshold swing and the doping mechanism also are held responsible for the high off-currents that can be seen in Figure 6.12. The variation of the off-currents for the other four interface modifications is not significant, because off-currents always vary in this order of magnitude as a matter of device-to-device-variance.

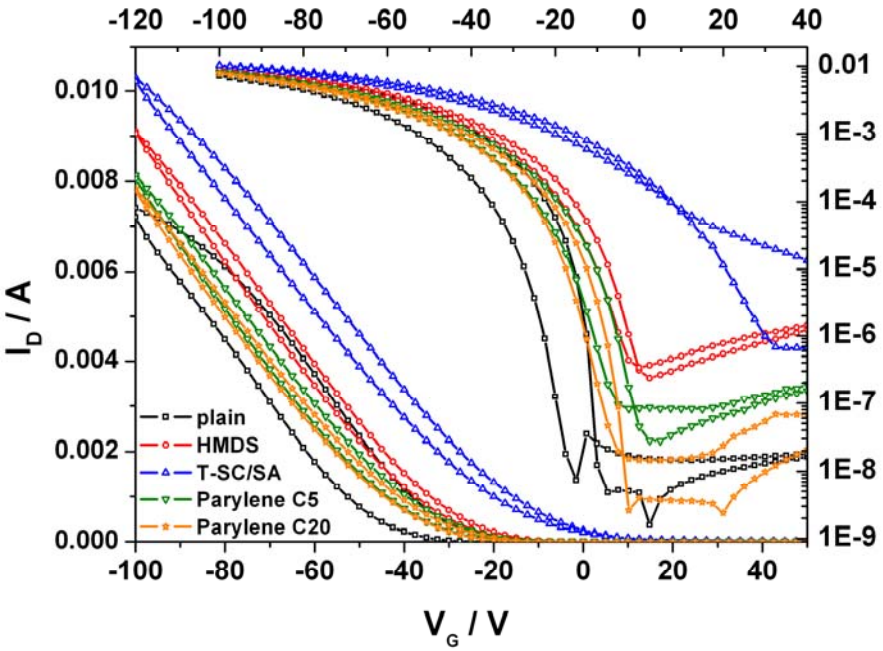

Figure 6.12) Transfer Curves at room temperature of pentacene OTFTs with different interface modifications.

In comparison to all OTFTs with modified interfaces the hysteresis for plain devices is extremely big. This is not only true for the special device shown in Figure 6.12 but was discovered for all plain devices . Since the highly hydrophilic (after the O2 plasma treatment even more) silicon oxide surface was not sealed with an additional organic dielectric layer as in all the other devices a lot of water induced traps are formed at the interface. A longer evacuation time would probably reduce the hysteresis (and actually does so, as will be discussed later) but in the context of this experiment a fixed evacuation time (pfeiffer vacuum TC100 turbo-molecular pump) of 5 minutes between the installation of the device into the cryostat and the first measurement was chosen.

Table 6.2) Most important OTFT parameters, evaluated in the saturation regime of the off-to-on sweep at room temperature as extracted from the transfer lines. μ_{RT} is the room temperature mobility, V_{Th} the threshold voltage, A_{Hyst} a numerical value corresponding to the amount of hysteresis, I_{on}/I_{off} is the on/off-ratio, I_{off} the off-current and S_{STh} the subthreshold swing.

	μ_{RT} / cm^2/Vs	V_{Th} / V	A_{Hys} / a.U.	I_{on} / I_{off} / 1	I_{off} / A	S_{STh}/ V/dec
Plain	0.73	-16	**13**	10^6	10^{-8}	4
HMDS	**1.1**	-9	3	10^4	10^{-6}	3
T-SC/SA	0.43	**13**	5	10^3	10^{-5}	**10**
Parylene C 7	0.49	-13	4	10^5	10^{-7}	2.5
Parylene C 23	0.43	-9	4	10^6	10^{-8}	1.5

The devices with the two differently thick Parylene C layers look alike. The only small difference is the smaller off-current for the thicker layer devices. The best OTFTs are the HMDS modified devices. They are characterized by a high mobility and a small subthreshold swing, while hysteresis and threshold voltage

are average. Only the slightly high off-current could be mentioned as a disadvantage. It is a common observation from literature that HMDS improves the device characteristics of pentacene/silicon-TFTs.[48,49] In fact, such a device layout yielded some of the highest mobilities ever measured for pentacene.[50] Remembering the giant grains shown in the AFM-picture of the pentacene surface in Figure 6.11, this is not very surprising.

6.6) Temperature dependent OTFT Characterization

After the installation of the TFTs in the specimen holder, the specimen holder was inserted into the helium cryostat, and the specimen chamber was evacuated for 5 minutes to reach a good vacuum and remove any contamination of air and water. Afterwards, the sample chamber was flooded with high purity helium. This step was necessary to allow a faster cooling rate. Then the cooling started. For all devices the same cooling/measuring procedure was applied. In the range from 300 to 200 K measurements were made every 15 K; below 200 K the temperature steps were reduced to 10 K. Below 100 K, the temperature difference between subsequent measurements was further reduced to 5 K. This was a concession to the reciprocal temperature scale of the Arrhenius plots. Whenever, one of these target temperatures was approached, equilibrium between cooling and heating was established and the temperature was held fixed for one minute before the measurement was made. Then the cooling started again. To avoid any additional stress effects, no output curves were measured.

6.6.1) Discussion of the transfer characteristics

In this part, characteristic transfer curves for the measured temperature range will be shown for all interface modifications. Additionally, the shape of the curves will be discussed briefly – in comparison to the plain reference devices.

A more detailed discussion of the device properties will follow in the next subchapter, where the results for all devices will be compared with each other.

a) plain devices

Figure 6.13 shows selected transfer curves for different temperatures, beginning at room temperature and going down as deep as 25 K. The plain devices were meant as reference. Because of the high hysteresis this goal was not really achieved. Actually the transfer curve at 250 K has a higher mobility and a smaller hysteresis than the transfer curve at room temperature. Unfortunately this effect was observed too late during the evaluation of the measurements, when no liquid helium was available any more. As already mentioned above this is an effect of the contamination with air and water. To proof this test experiments were conducted later, were a longer evacuation time of 30 minutes was chosen before actually performing the first measurement. This indeed significantly reduced the hysteresis. For the later analysis of the activation energy of the temperature activated transport the first 4 curves have been omitted in the case of plain devices, and every analysis started at 250 K.

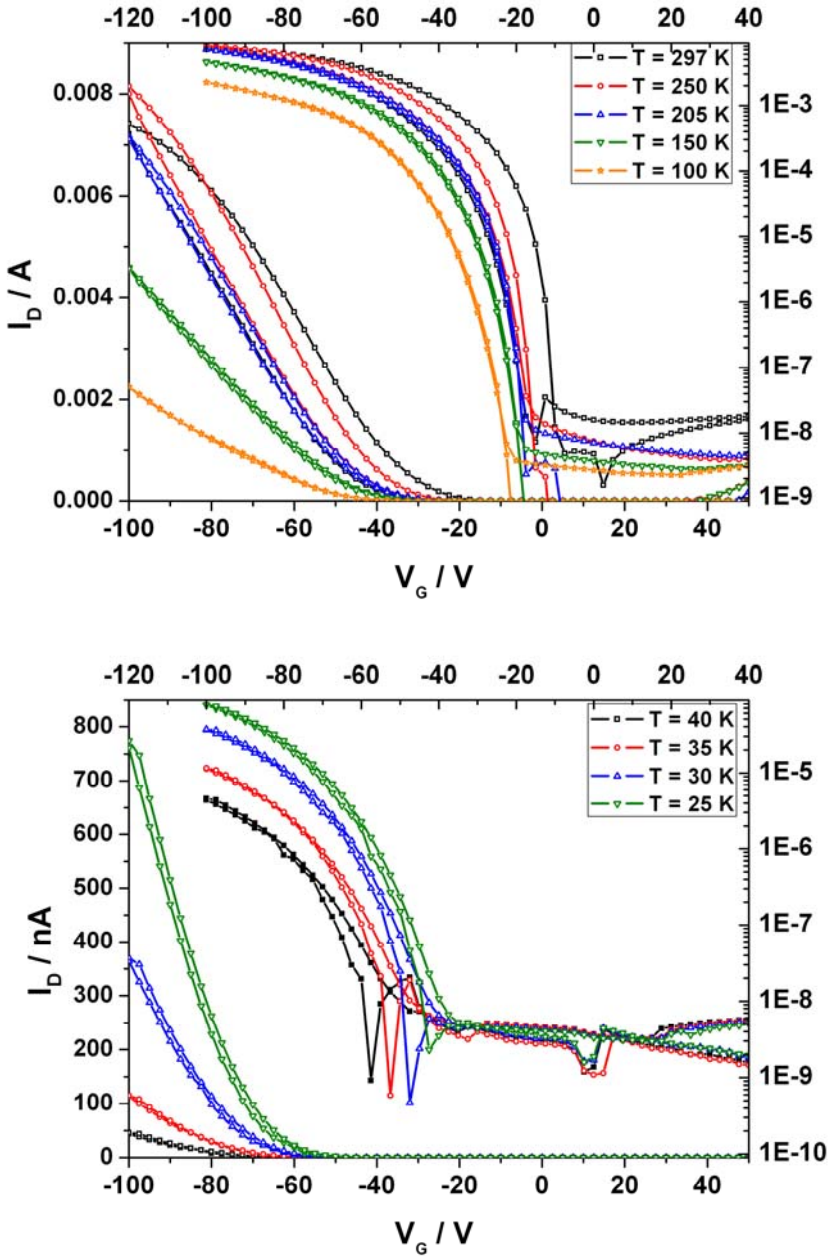

Figure 6.13) Transfer characteristics for a plain pentacene/$Si0_2$ TFT for temperatures ranging from room temperature down to 25 K.

Apart from the high temperature curves, the transfer characteristics for the plain device show good OTFT behaviour for all observed temperatures. The on/off-ratio is very high at room temperature ($I_{onoff} = 10^6$) and stays high even at the lowest temperatures ($I_{onoff} = 10^4$). The off-current is also almost independent of the temperature of the devices.

b) HMDS – devices

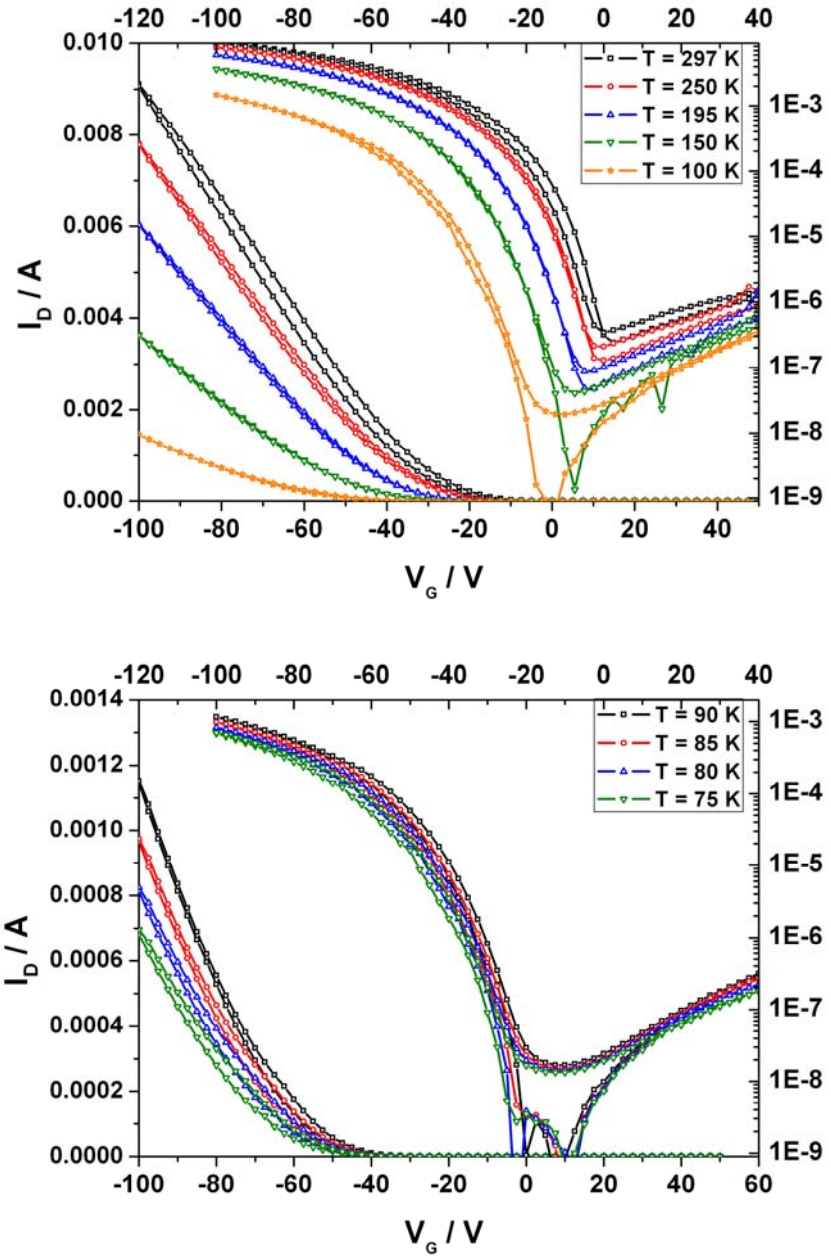

Figure 6.14) Transfer characteristics for a pentacene/HMDS TFT for temperatures ranging from room temperature down to 75 K.

Compared to plain devices, a couple of differences are observed. The room temperature threshold voltage is shifted to positive gate voltages, the hysteresis of these devices is much smaller, and the off-current is higher and depends on temperature. Also the room temperature mobility is higher for these devices.

c) **Parylene C – films (7 & 23 nm)**

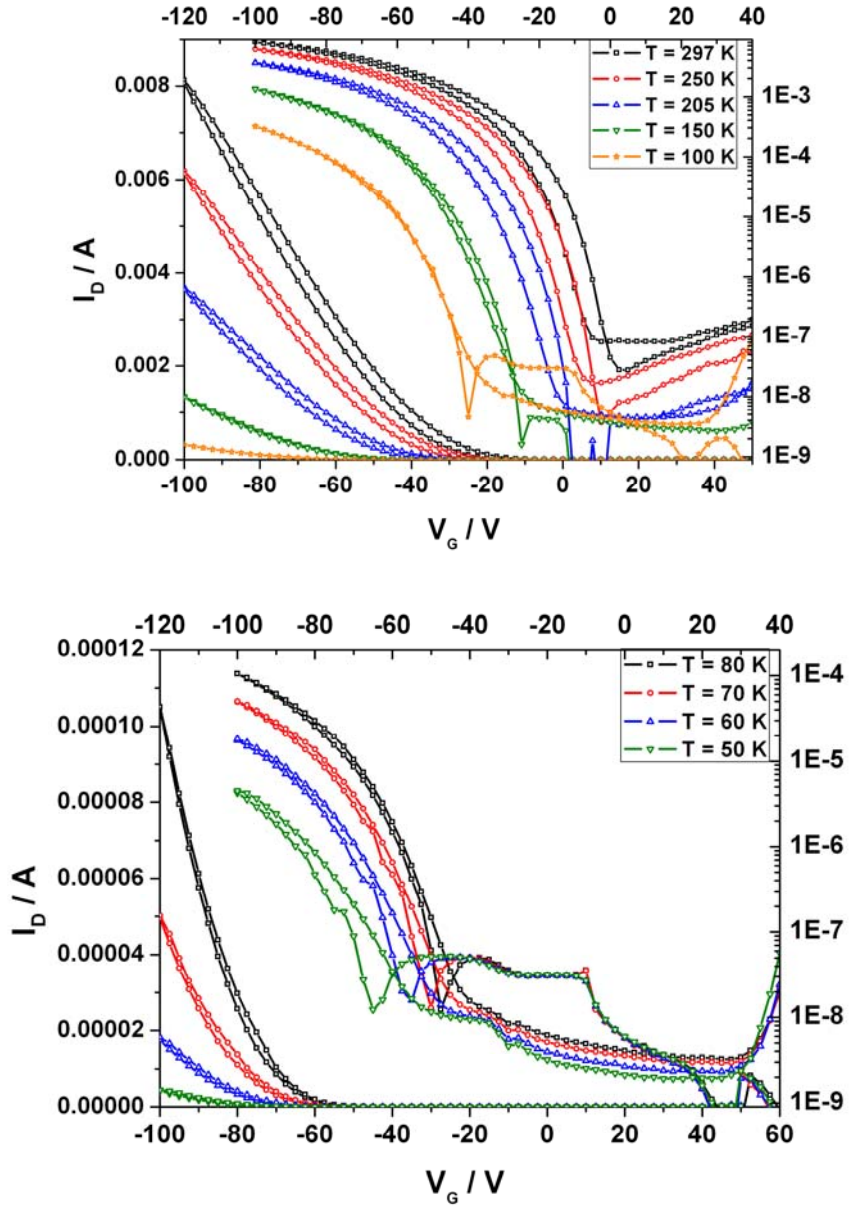

Figure 6.15) Transfer characteristics for a pentacene TFT with a 7nm thick layer of Parylene C on top of the silicon oxide for temperatures ranging from room temperature down to 50 K.

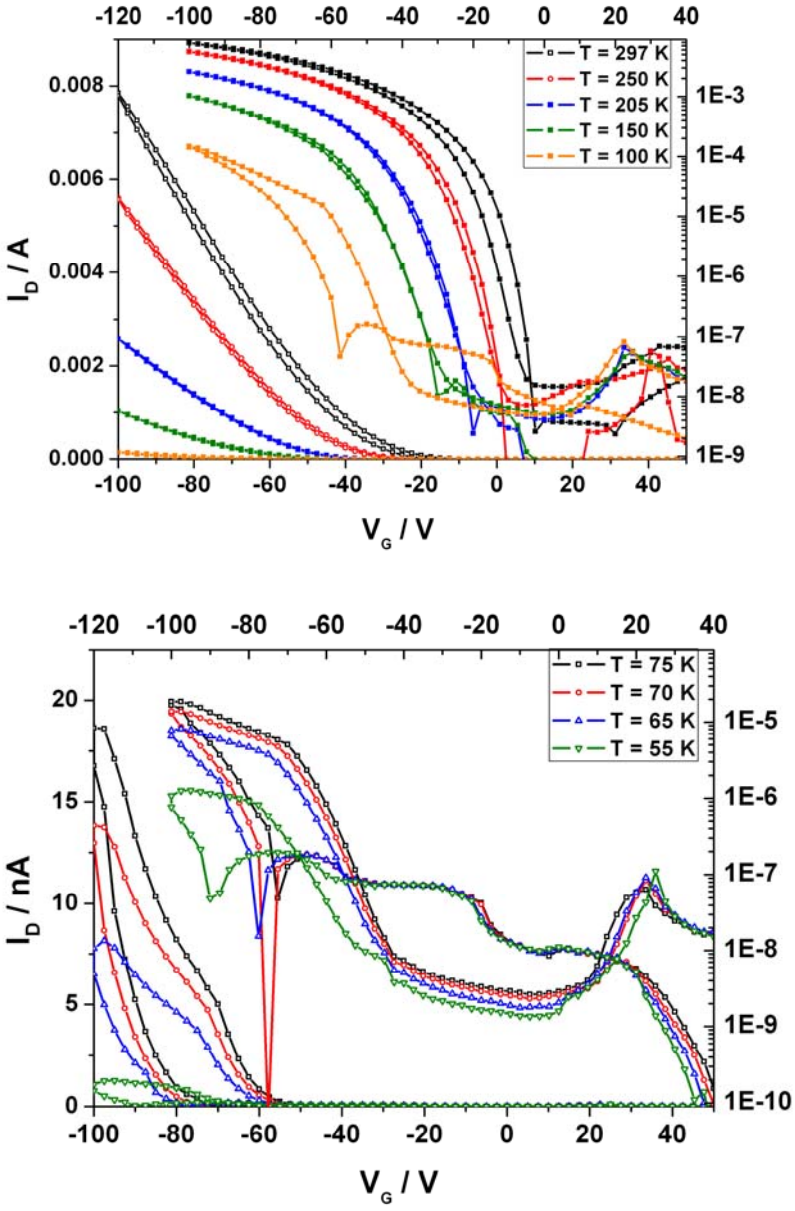

Figure 6.16) Transfer characteristics for a pentacene TFT with a 23 nm thick layer of Parylene C on top of the silicon oxide for temperatures ranging from room temperature down to 55 K.

Devices built with differently thick Parylence C-layers could not be measured down to temperatures of 25K, since the transfer characteristics do not allow for the extraction of device parameters at temperatures below 70 K. Figure 6.15 and Figure 6.16 give good examples for this fact. Especially in the off-current

region the current fluctuates over two orders of magnitude. It is unclear why these problems only appeared in the case of Parylene C devices.

d) T-SC/SA

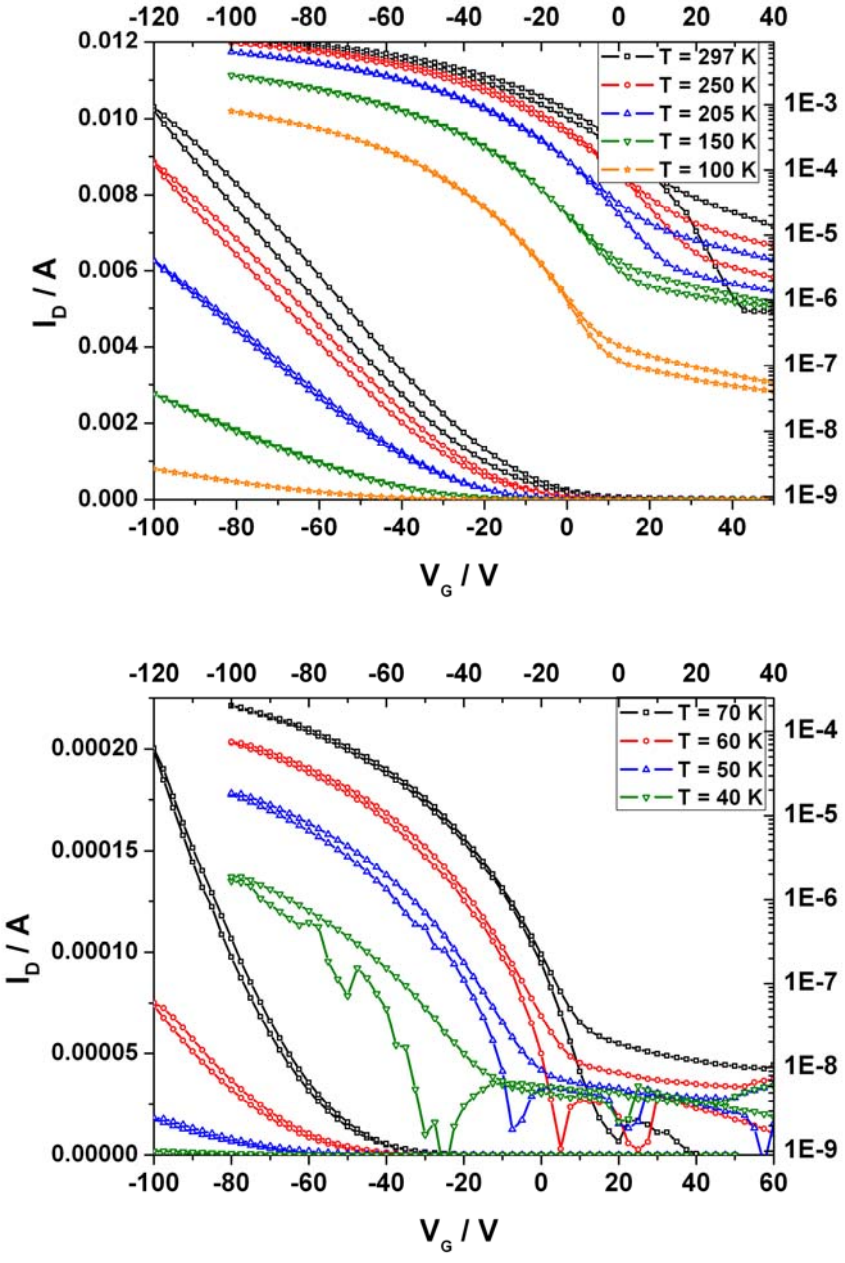

Figure 6.17) Transfer characteristics for a pentacene TFT with a monolayer of T-SC/SA on top of the silicon oxide for temperatures ranging from room temperature down to 40 K.

Devices with the T-SC/SA layer showed a pronounced temperature dependence of the off-current. Probably this phenomenon also is caused by the interfacial doping mechanism.

6.6.2) Characterization of the device properties

In the following figures the mobility and the threshold voltage were always evaluated in the saturation regime of the off-to-on sweep. However, the analysis was also performed in the linear regime and also for the on-to-off sweep. Hence, for every temperature step four different values for the mobility and the threshold voltage were extracted. Qualitatively there was no difference in the temperature dependence for all those values.

Figure 6.18 shows exemplary mobility data for a plain and a T-SC/SA device, evaluated for all four different possibilities. The difference in activation energy for those four methods is smaller than the standard deviation of the exponential fit.

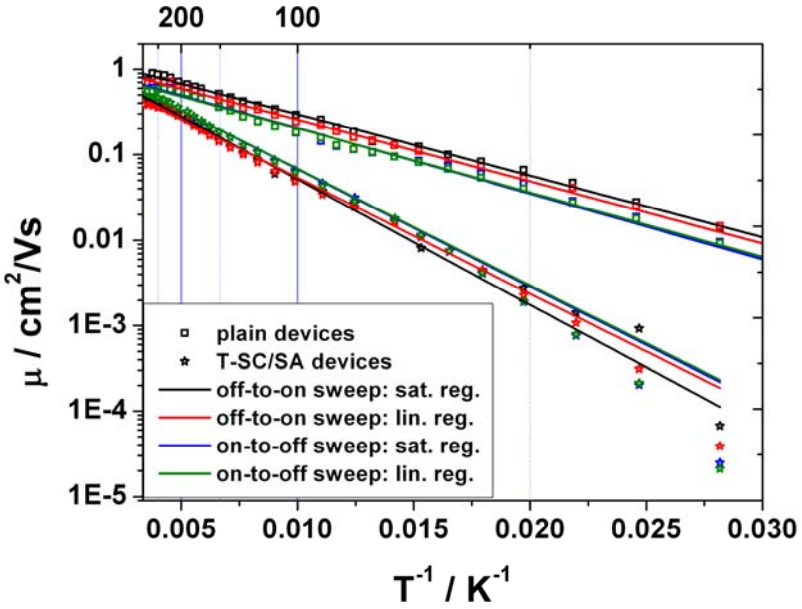

Figure 6.18) Arrhenius plots for plain devices (squares) and T-SC/SA devices (stars), showing the mobility evaluated in the saturation regime of the off-to-on sweep, in the linear regime of the off-to-on sweep, in the saturation regime of the on-to-off sweep and in the linear regime of the on-to-off sweep. No qualitative difference can be observed.

Figure 6.19 shows the temperature dependence of the threshold voltage. Again no qualitative difference is visible. The small difference between values calculated in the off-to-on sweep and those calculated in the on-to-off sweep results from the hysteresis.

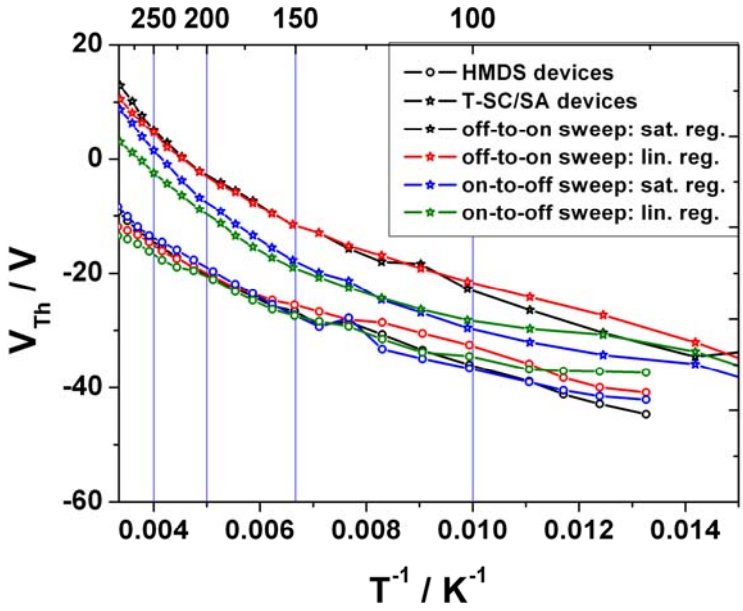

Figure 6.19 Threshold voltages for HMDS devices (circles) and T-SC/SA devices (stars), as a function of temperature evaluated in the saturation regime of the off-to-on sweep, in the linear regime of the off-to-on sweep, in the saturation regime of the on-to-off sweep and in the linear regime of the on-to-off sweep. No qualitative difference can be observed.

Another point that should be mentioned before showing the measured results is the device to device variance. Figure 6.20 shows uncorrected (uncorrected in this case means that all transfer curves were used for the parameter extraction, even bad ones as in Figure 6.15 and 6.16 for the low temperature region; additionally runaway values were not deleted) data from 6 different temperature measurements performed for 6 different transistors on 3 different substrates for plain pentacene devices. As can be seen the calculated activation energy ranges from 14 meV to 22.7 meV for plain devices. The activation energy range is in the same order of magnitude for all 5 different interface modifications. At first glance this variation looks huge, but as already mentioned above we are talking about uncorrected data points here. When cleaning up these measurements, (e.g. deleting runaway values and omitting curves with to few datapoints (in Figure 6.20 this would include the red and the blue curves)), the

results get better and we can extract a activation energy between 14 to 17.5 meV. The data shown in the following chapter always correspond to the best measurement results (e.g. in Figure 6.20 the best measurement result would be the green curve, since the scattering of the data points is minimal and the device was measured over a broad temperature range).

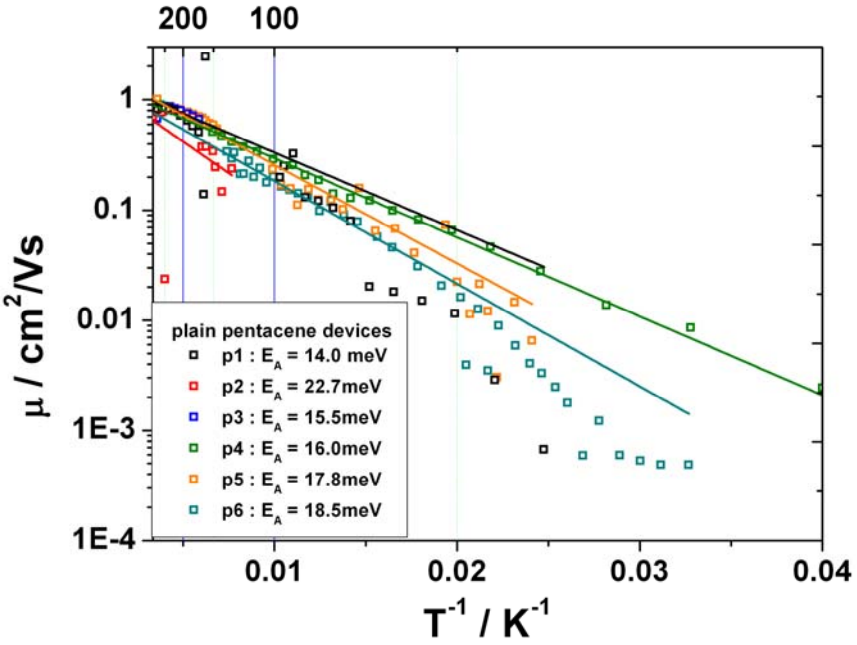

Figure 6.20: Mobility as a function of temperature for all plain transistors, which were measured during this measurement session.

a) mobility

Figure 6.20 shows the resulting Arrhenius plots of the 5 different devices. All measured data points are least-squares fitted to a two parameter exponential function $y = ae^{bx}$. The measured data correlates well with the exponential fit, only in the Parylene C 23nm devices a strong deviation from the linear relationship is observed at lower temperatures. When looking at Figure 6.18 the reason for that becomes obvious. It is simply impossible to perform a reliable fit to those transfer curves.

The activation energies E_A and room temperature mobilities are summed up in Table 6.3. Altogether, the results presented here match those of chapter 4.

Table 6.3) The room temperature mobility μ_{RT} and the activation energy of the mobility E_A for all five different interface modifications. The activation energy was calculated through equation 6.1.

	μ_{RT}/ cm²/Vs	E_A/ mV
plain	0.73	16.0
HMDS	1.1	19.0
T-SC/SA	0.43	29.1
parylene C 7	0.49	30.8
parylene C 23	0.43	41.7

Devices with bigger pentacene grain sizes also have a higher mobility and smaller activation energy. So again the number of grain boundaries and thus traps defines the room temperature mobility. Moreover, it seems that devices with more traps (the amount of traps should depend on the amount of grain boundaries, following the polycrystalline transport model) also have deeper traps and therefore higher activation energy. Numerically the activation energy of plain devices is smaller than the activation energy of HMDS devices (by only 3 meV, which lies in the standard deviation of the fit).

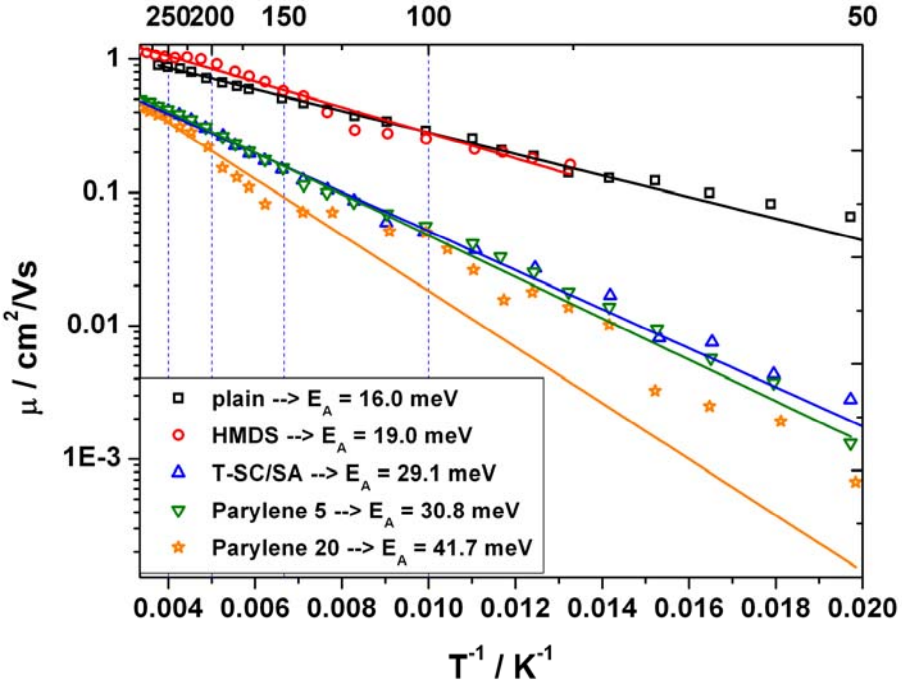

Figure 6.20) Arrhenius plots of the 5 different devices and the resulting activation energy

b) threshold voltage

Figure 6.21 sums up the temperature dependence of the threshold voltage for all interface modifications. All non-reactive layers (i. e. excluding T-SC/SA) have a similar, slightly negative threshold voltage at room temperature; The dependence of V_{Th} on temperature can be described as an exponential decay (the data points for the parylene C 25 case again deviate because of the bad looking transfer curves at low temperatures). Equation 6.4 is a shifted Boltzmann distribution

$$\Delta V_{Th}(T) = V_{Th,0} e^{\frac{E_{ST}}{k_B T}} \qquad \textbf{(6.4)}$$

$V_{Th,0}$ is a fitting term and E_{ST} gives the trap energy of the deep traps, which are responsible for the threshold voltage shift.

As can be seen from Figure 6.21 this function hits the data points pretty well, with three explainable exceptions. In the Parylene C 23 case again the data values are too scattered for the low temperature region, which again is based on the bad transfer curves in this case. In the high temperature region, the data

points for the TSC/SA and plain devices are systematically higher than the exponential function. Those are also the two curves, which have the largest hysteresis at room temperature; moreover the doping mechanism in the TSC/SA case probably cannot solely be described with such an equation. In Figure 6.22 the threshold voltage is plotted again as a function of temperature for the TSC/SA and the plain devices. This time the first 4 data points are omitted and the fit is only performed for the other data points, yielding good agreement with the exponential fit. The calculated trap energies E_{ST} can be found in Table 6.4. (the two values given in brackets correspond to the second exponential fit from Figure 6.22) They are systematically lower that the thermal activation energies of the mobility, showing that a completely different kind of traps (with a lower energy) is responsible for the shift in the threshold voltage. This energy contradicts the trapping model, that was introduced earlier, since a much higher activation energy was expected. We conclude that not the energetic position is responsible for the determination, if a trap is responsible for a shift in threshold voltage or in mobility, but the spatial position in the device. We think, that deep traps which lie in the grain boundaries are responsible for the decrease of the charge carrier mobility and that shallow traps, at the interface are responsible for the observed shift in threshold voltage.

The total magnitude of the shift in the temperature range from 300 to 70K is different and depends on the chosen interface modification. With this total shift and Equation 6.3 the change in the trapped charge density was calculated. The greatest amount of thermally trapped charges corresponds well with the amount of grain boundaries in pentacene (i. e. Interface modifications that lead to small pentacene grains trap more charges than interface modification that lead to large pentacene grains.)

Table 6.4) The room temperature threshold voltage V_{Th}, the total shift of threshold voltage in the temperature range 300K -70, the resulting change in trap charge density in this temperature range ΔN_T following Equation 6.3, and the trap energy E_{ST}, resulting from the fit of Equation 6.4 For TSC/SA and plain devices two values are given, the second one corresponding to Figure 6.22

	V_{Th} / V	ΔV_{Th}/ V	ΔN_T/ $10^{12}cm^{-2}$	E_{ST} / meV
plain	-16	43	5.4	6.1 (4.5)
HMDS	-9	36	4.5	10.8
T-SC/SA	13	80	10	4.4 (2.8)
parylene C 7	-13	51	6.4	18.5
parylene C 23	-9	67	8.4	15.1

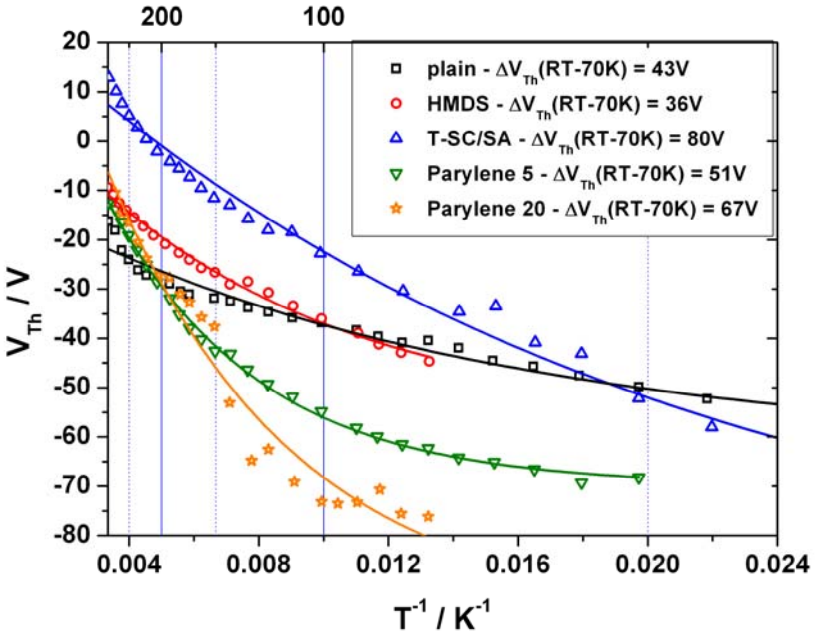

Figure 6.21) Threshold voltage (calculated in the saturation regime of the off-to-on sweep) as a function of decreasing temperature. The lines correspond to an exponential fit after Equation 6.4

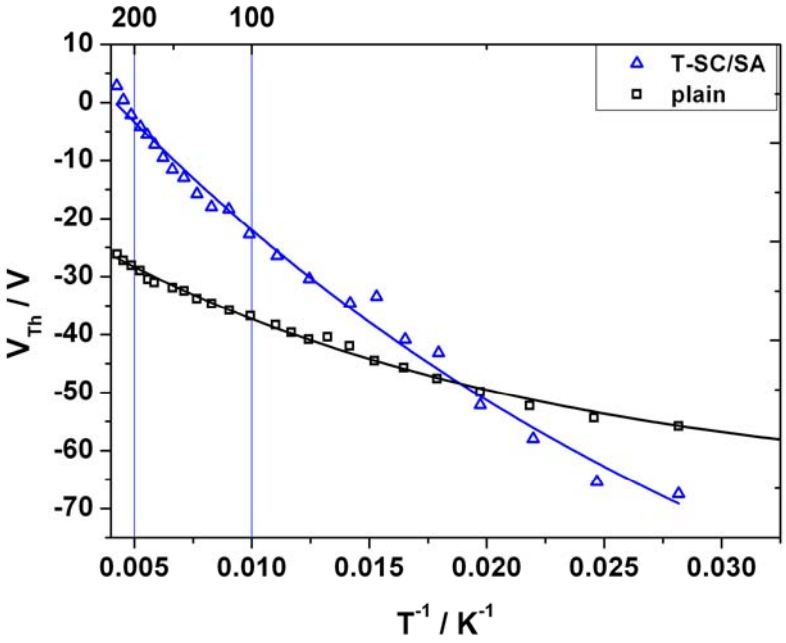

Figure 6.22) Threshold voltage (calculated in the saturation regime of the off-to-on sweep) as a function of decreasing temperature for T-SC/SA and plain devices. The lines correspond to an exponential fit after Equation 6.4

c) hysteresis

Last but not least the temperature dependence of the hysteresis is shown in Figure 6.22. All devices behave similarly; the hysteresis decreases in the beginning and virtually disappears around 170 K. When further decreasing the temperature, the hysteresis increases again, but this time in the other direction (the off-to on sweep has now lower drain currents than the on-to off sweeps. Since this behaviour is similar for all interface modifications we conclude that this is no measurement of a material parameter but an artefact that comes through the measurement time for every (I_D, V_G)-set. Probably, when changing this measurement time from 0.1s to any bigger or smaller value the temperature, when the hysteresis disappears would also be shifted to higher/lower values.

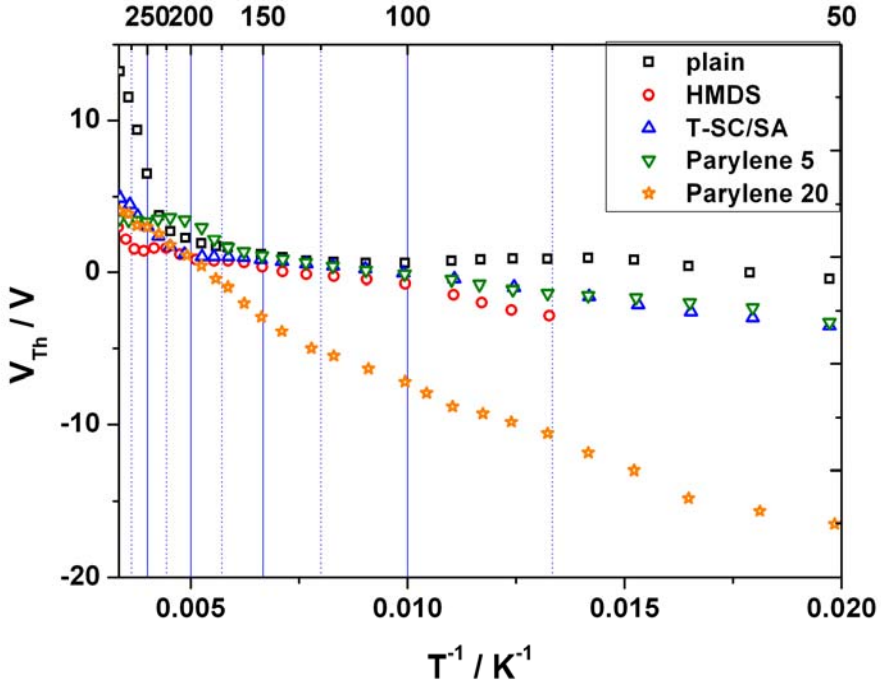

Figure 6.22 The hysteresis as a function of decreasing temperature.

6.6) Conclusion

In this chapter pentacene TFTs with different interface modifications have been characterized as a function of temperature. Results for the temperature dependence of the mobility were interpreted following the MTR-model. The activation energy of the mobility could be varied in the range from 40 to 15 meV, and scaled with the grain size from the AFM pictures, meaning that not only the total amount of traps increases with the number of grain boundaries but also the energetic depth of the traps increases.

Additionally, a second trap energy was fitted, which accounts for the shift of the threshold voltage. In all cases, this second energy is much smaller than the activation energy for the mobility. This gives the hint, that another kind of traps in the semiconductor is responsible for the shift in threshold voltage and the model proposed earlier is inaccurate. Probably deep traps in the grain boundaries are responsible for the decrease of mobility and shallow traps at the

interface are responsible for the shift of the threshold voltage. The shift in threshold voltage is also a parameter for the amount of trapped charges. With decreasing temperature more and more charges are trapped and thus the threshold voltage is shifted.

For the hysteresis no material parameter was extracted. We conclude that the temperature dependence of the hysteresis is in first approximation caused by the measurement setup and not by the interface modification.

All in all, the results of this chapter show that the interface between dielectric and semiconductor plays a crucial role for the properties of OTFTs.

At this point it should be stressed that all these results were obtained without considering the contact resistance. The contact resistance is however a very important parameter, when describing TFTs and should not be neglected when talking about the temperature dependence of the mobility. The next chapter will primarily deal with the contact resistance and different attempts to extract it.

6.7) References

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A man who dares to waste one hour of time,
has not discovered the value of life.
Charles Darwin

VII) Attempt of a Temperature Dependent Characterization of the Contact Resistance in Different TFTs.

Preface:

As already mentioned at the end of the previous chapter, all measurement results of this previous chapter are only of a “qualitative” character, as long as the contact resistance of the TFTs is not considered. The present chapter deals with the contact resistance, and with the search for a reliable method to extract it as a function of temperature. The chapter begins with a review over literature, introducing past results on this matter. The used method for contact resistance determination is the Transfer Line Method (TLM), which was already introduced in section 2.1.1 of this thesis.

After the introduction, two different device schemes will be presented and the contact resistance will be extracted for both schemes as a function of temperature. Unfortunately the TLM-method did not yield satisfactory results in both cases. Pentacene TFTs that were analyzed in this chapter include, top contact TFT, which were evaporated through a shadow mask, as well as bottom contact TFTs, which were produced by Nanoimprint Lithography. Both types of TFTs were produced at the Joanneum Research in Weiz by A. Fian and his coworkers. The temperature dependent measurements were partly performed by me at the TU Graz and partly at the Johanneum Research in Weiz.

7.1) Introduction – contact resistance in literature.

This chapter will mostly follow the work of Hamadani & Natelson,[1] who performed their study on polycrystalline poly(3-hexylthiophene) (P3HT)-TFTs, but will also include some measurement results of pentacene TFTs.

In the work of Hamadani & Natelson, OTFTs with channel lengths ranging from 0.4 µm to 40 µm and a channel width of 5 µm were produced in a bottom contact structure. The TLM plot is shown in Figure 7.1. At room temperature (300K) and at a gate voltage of -90 V the analysis yielded a width-normalized contact resistance of $R_{con}w = 1x10^{3} - 1x10^{4}$ Ωcm.

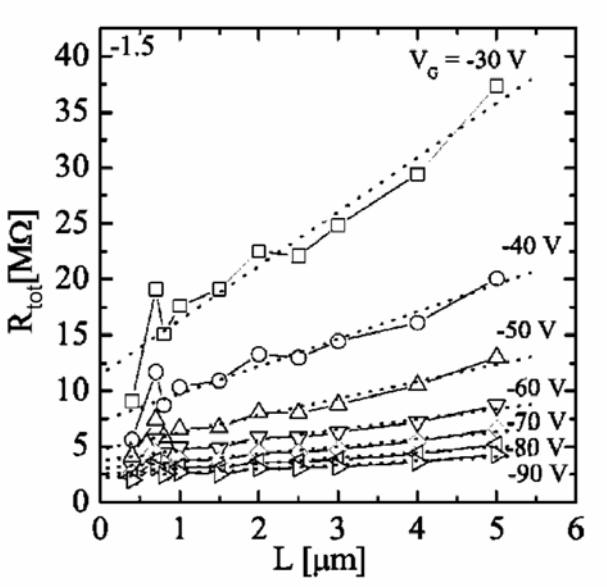

Figure 7.1: Total resistance R_{tot} plotted as a function of channel length L. for P3HT-OTFTs with a common channel width of 5 µm taken from Reference 1.

These devices were cooled down to temperatures of 100K and a TLM-analysis was performed over the whole temperature range. The temperature dependence of the mobility and of the contact resistance are plotted in Figure 7.2.

The lines in the mobility plot of Figure 7.2 correspond to a linear fit, according to the MTR model – resulting in activation energies of E_A(at 90 V) = 29.4 meV. The contact resistance also shows temperature activated behaviour; it increases with decreasing temperature with almost the same activation energy as the mobility. This effect could easily be explained by the theory of organic semiconductor-metal contacts developed by Scott & Malliaras.[2] Their theory builds on earlier work, that simulated the injection of charges into poor conductors,[3] where the mobility is so small that back-diffusion from the semiconductor into the metal already plays a mayor role. They show that the rate of thermionic injection into a semiconductor is a function of the mobility in the semiconductor and can be explained by Equation 7.1.

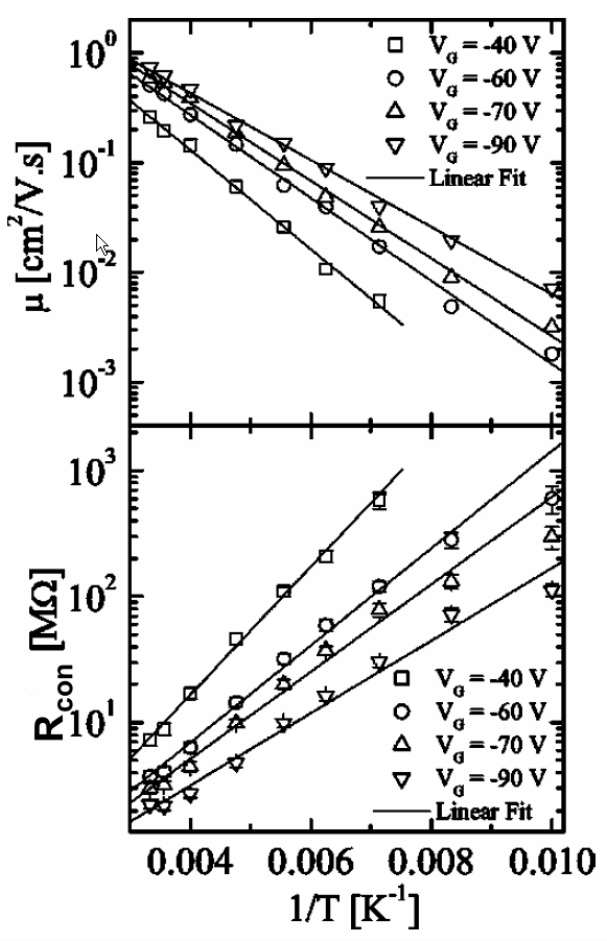

Figure 7.2) Temperature dependence of top) the mobility and bottom) the contact resistance for several gate voltages for bottom contact P3HT-TFTs. This plot was taken from Reference 1.

$$J_{inj}=4\Psi(f)^2 N_0 e\mu E e^{\frac{-\Phi_B}{k_B T}} e^{f^{1/2}} \quad \textbf{(7.1)}$$

Here $\Psi(f)$ is a slowly varying function of the electric field that corresponds to Schottky barrier lowering, N_0 is the density of localized states that are available for hopping conduction, μ is the electron mobility in the semiconductor, E the electric field, Φ_B is the Schottky barrier between the metal and the semiconductor, k_B the Boltzmann Constant, T the temperature and $f=\frac{e^3 E}{4\pi\varepsilon\varepsilon_0(k_B T)^2}$ is a term due to Schottky barrier lowering. Provided that the Schottky barrier between the metal and the semiconductor is low and the electric fields are quite low, the temperature dependence of the contact resistance is determined by the temperature dependence of the mobility and the injection barrier Φ_B following Equation 7.2.

$$R_{con} \propto e^{\frac{[E_A+\Phi_B]}{k_B T}} \quad \textbf{(7.2)}$$

This implies that the contact resistance is inversely proportional to the mobility $R_{con} \propto \frac{1}{\mu}$. Indeed Hamadani & Natelson found that when plotting the contact resistance as a function of mobility, as can be seen in Figure 7.3 the dependence of the contact resistance on mobility can be approximated with a power law of $R_{con} \approx \frac{1}{\mu^{1.09}}$.

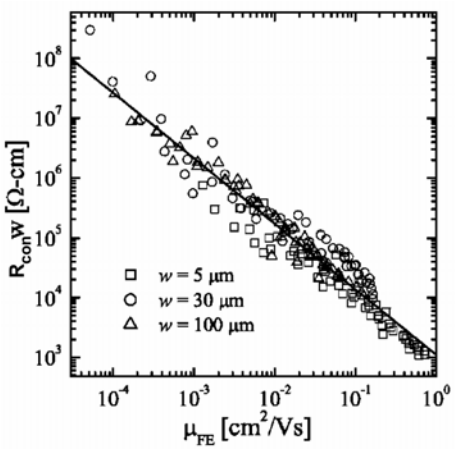

Figure 7.3 Contact resistance as a function of mobility for all measured device and all temperatures. The fit is to a power law with exponent -1.09 taken again from Reference 1.

Apart from the used semiconductor, the magnitude of the contact resistance also depends on the used electrodes[4] and the device layout. Top contact geometries often show a much smaller contact resistance than bottom contact geometries.[5,6]

For similar transistors as those under investigation here (namely Au source-drain electrodes & pentacene as organic semiconductor) there even exist temperature dependent gated four probe measurements[7] (which is a more sophisticated approach than then the TLM method) performed by Pesavento et al.[7] Their results can be compared to the results shown here. At a gate voltage of V_G = - 75 V and a drain voltage V_D = -10V they obtained a value of $R_{con}w$ = 2.25x10^4 Ωcm for the contact resistance at room temperature. This value is consistent with the values obtained by Necliudov et al.[5,6] with TLM measurements, where they obtained a width normalized contact resistance at a gate voltage of V_G = -30V of R_{con} = 5x10^4 Ωcm (w = 1.2cm). Pesavento et al. also extracted the temperature dependence of the contact resistance and found three regimes shown in Figure 7.4. In the temperature region from 180 K to 50 K they found thermally activated behaviour. Below 50 K the resistance saturates (not shown). In the region between 300 K and 180 K the resistance is also thermally activated but with a much bigger activation energy. They extract an

activation energy for the contact resistance of E_A = 30meV for V_G = -40V, while they received an activation energy of the mobility of E_A = 22meV. With the same measurement technique, Yagi et al.[8] extracted a room temperature contact resistance for a gate voltage of -40V in the order of $R_{con}w = 8.8x10^5$ Ωw (w = 1.1cm) for pentacene TFTs with a spincoated HMDS layer on top of the $Si0_2$ dielectric. They also extracted an activation energy for the contact, as well as the channel resistance in the temperature range from 300 to 100 K – being $E_{A,con}$ = 88 meV and $E_{A,ch}$ = 42 meV respectively. Another group[9] obtained values of around 3 x 10^5 Ωcm for the contact resistance for Au/pentacene transistors.

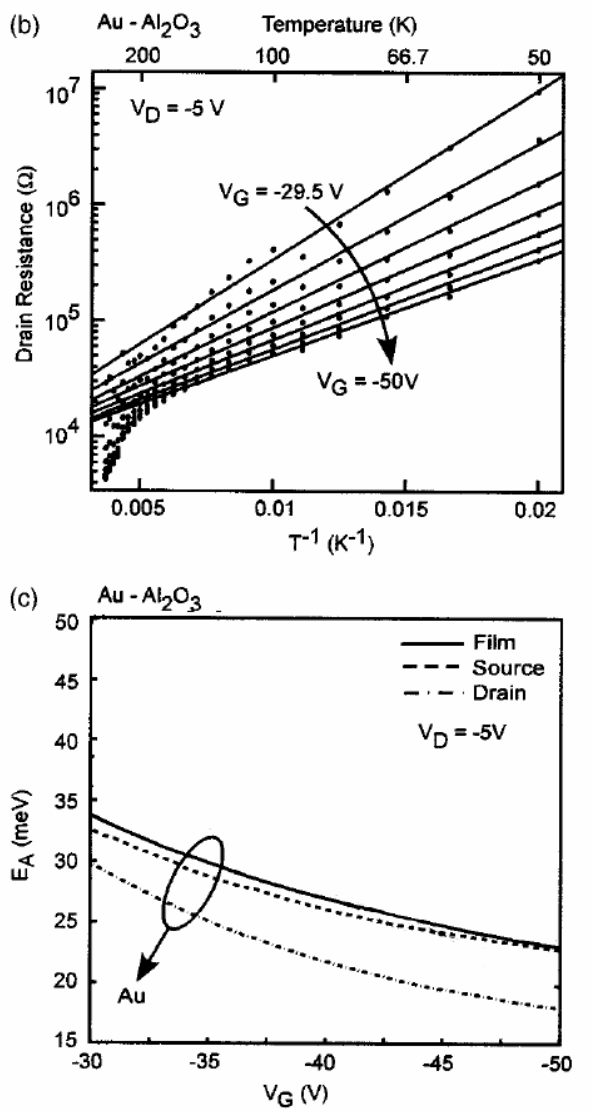

Figure 7.4: top) Temperature dependence of the contact resistance of pentacene OTFT with Au electrodes obtained by gated four-probe measurement. Bottom) Gate voltage dependence of the activation energy of the contact resistance taken from Reference 7.

Last but not least, we want to present a model, which allows estimating a contact resistance corrected mobility μ_{corr}, without really measuring the contact resistance. Under the usual assumption – namely the gradual channel approximation and a constant mobility all over the channel (see, section 2.1) the

correction of the contact resistance can be calculated following a model of Jain[10], that was adapted for organic TFTs by Horowitz et al.[11] with Equation 7.3.

$$\sqrt{\mu_{corr}}(V_G - V_{Th}) = \frac{I_D}{V_D}\sqrt{\frac{LV_D}{WC_i}}\frac{1}{\sqrt{g_m}} \qquad \textbf{(7.3)}$$

μ_{corr} is the corrected mobility, and g_m the transconductance, which is calculated as $g_m = \frac{\partial I_D}{\partial V_G}$, as the slope of the transfer curve for small drain voltages. Horowitz et al. used this model to describe oligothiophene TFTs, but again the model can easily be adopted for pentacene TFTs.

In Figure 7.5 the effect of this correction can be seen. Especially for high gate voltages the correction is necessary, because normally the mobility is highly underestimated. For lower gate voltages, the mobility is smaller, because the assumption, that the mobility is constant all over the channel is no longer valid.

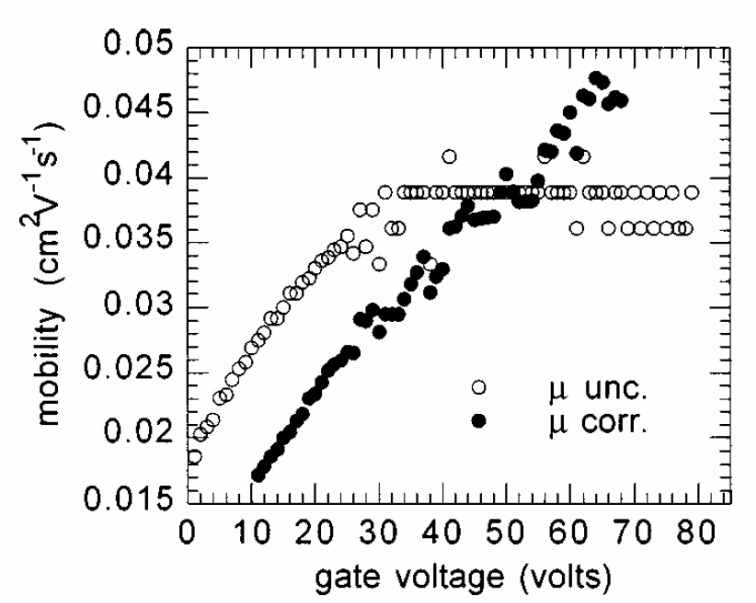

Figure 7.5.Field-effect mobility of sexithiophene TFTs with (dark circles) and without (open circles) correction for the contact resistance following Equation 7.1. This plot was taken from Reference 11.

7.2) Contact resistance evaluation for top-contact vacuum evaporated pentacene OTFTs

After this short review of literature we now come to measurement results, obtained in our laboratory. The first thing to do, to allow for an easy evaluation of the contact resistance, was to change the OTFT design scheme. Since different channel lengths are necessary for the application of the TLM method, we chose a device setup, which consists of six transistors with different channel lengths on one substrate. The wafer setup is shown in Figure 7.6 and the channel lengths and widths as measured with optical microscopy are shown in Table 7.1. Those TFTs were built at the Joanneum Research in Weiz by A. Fian and corworkers.

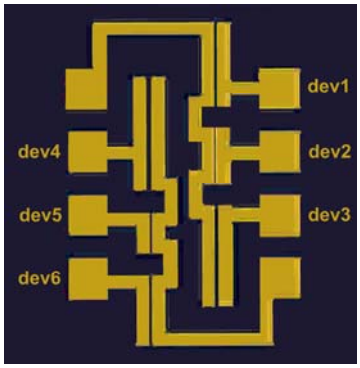

Figure 7.6: Picture of an OTFT with 6 transistors on one wafer (3 transistors sharing one common source electrode)

Table 7.1 Properties of the channels for the 6 transistors in the new shadow mask design

OTFT number	L / µm	W / mm
dev1	178	3.51
dev2	117	2.27
dev3	206	4.15
dev4	245	4.76

dev5	89	1.68
dev6	150	2.9

The goal of this design was to characterize the transistors with respect to their contact and channel resistances with the TLM.

7.2.1) Measurements at room temperature

At first, measurements were conducted at room temperature for TFTs following the new design scheme. 3 sets of TFTs were measured at that temperature in an argon glovebox or in the nitrogen filled cooling stage respectively. A typical set of transfer curves is shown in Figure 7.7.

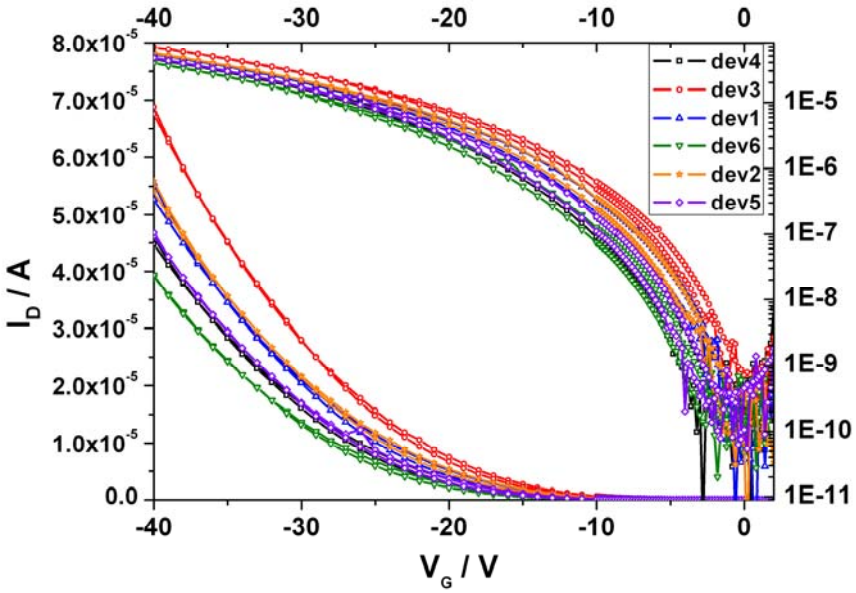

Figure 7.7) Set of transfer curves at room temperature (305 K) at a drain voltage of -10 V for the new OTFT design scheme, measured under inert conditions.

As can be seen, the mobilities and the threshold voltages of these six transistors are quite different and thus it is dubious if the basic requirements for

the TLM method are met. Unfortunately, Figure 7.6 shows the “best values” for all transistors measured. On all other wafers the devices were even more different from each other. For the sake of completeness we will perform the TLM method anyway. Transfer curves were recorded in the linear regime with drain voltages at -2, -5, and -10 V respectively. An exemplary TLM plot can be seen in Figure 7.8.

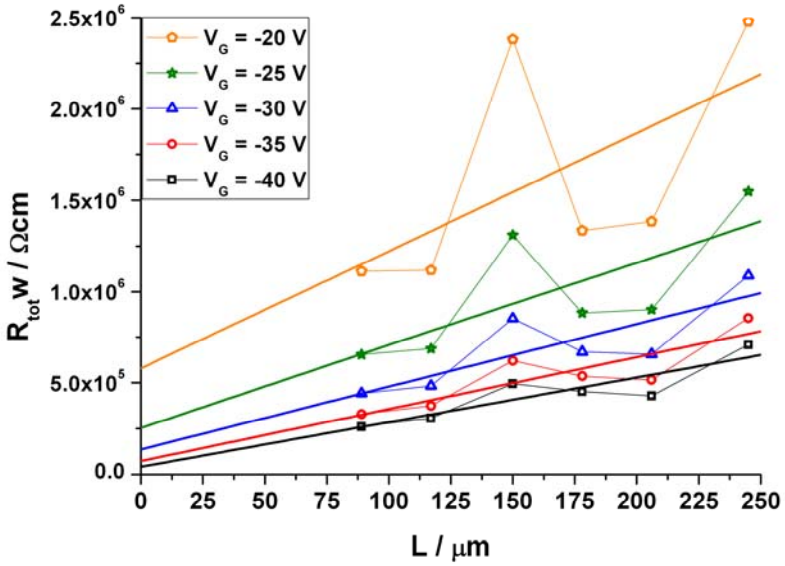

Figure 7.8) TLM – plot for an exemplary device series, measured with a drain bias of -10 Volts.

The contact resistance analysis was conducted only down to gate voltages of -20 V, to be sure to still be in the linear regime of the transfer curve. This analysis was conducted for all three sets of devices, yielding uniformly a width normalized contact resistance of $R_{con}w(V_G$ = -40V & V_D = -10V) = (6 ± 2) x 10^4 Ωcm. The channel resistance per 100micrometer in all samples was of the same order of magnitude and yielded results from $R_{ch}w$ = (7 ± 2) x 10^4 Ωcm (for a transistor with a channel length of 150μm). The given error margin is only the statistical error when performing a linear fit; the systematic error is not included. When looking at Figure 7.8 on sees on first glance that no clear trend for an

increase of the total resistance with the channel length is given. As already mentioned above, the device to device variance is quite high even when comparing six transistors on the same substrate. Even for the devices shown in Figure 7.7 the threshold voltage of the 6 different devices scatters by approximately 5 Volts, which makes an application of the TLM method problematic.

Since it was never possible to get a set of devices with a uniform threshold voltage and a uniform mobility, we tried another possibility to correct for these differing threshold voltages. In this approch all curves were shifted by their onset voltage, so that all curves uniformly start at a gate voltage of 0 V. The reason why the onset voltage instead of the threshold voltage was chosen for this shift is, because its determination required no further mathematical analysis using equations with inherent shortcomings. One can see on the first glance if a number of curves has the same onset voltage and no further mathematical analysis is required. This shifted transfer curves can be seen in Figure 7.8.

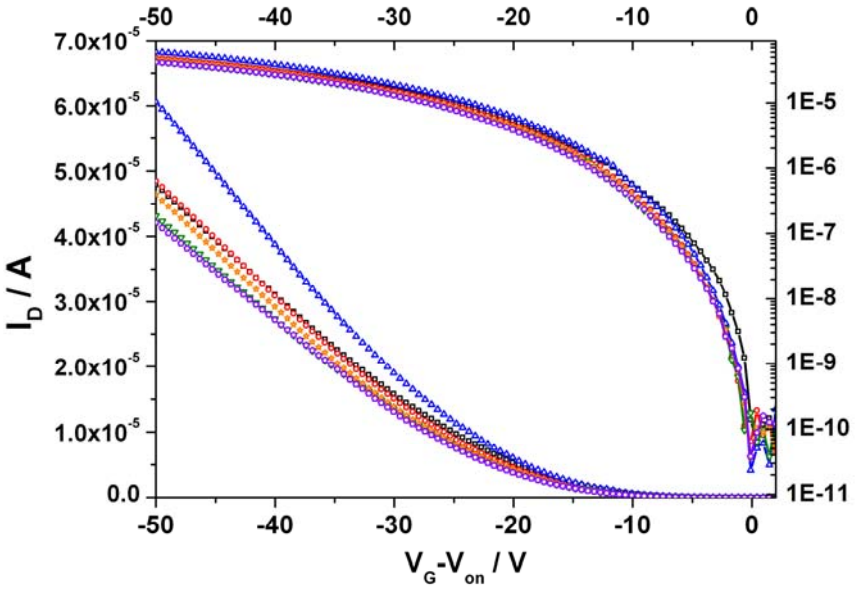

Figure 7.9) Set of the same transfer curves as in Figure 7.7 at room temperature (305 K) at a drain voltage of -10 V shifted to a common onset voltage of zero volts.

Now all curves were interpolated and extrapolated to a gate voltage of – 50 V and the TLM analysis was performed again. The TLM plot can be seen in Figure 7.10. Although the data points now clearly show that the total resistance increases with channel length, the TLM analysis is not satisfying, since the method yields a negative resistance for the data points for gate voltages of V_G = -40 and -50 Volts. For a gate voltage of V_G = -50 V the width normalized contact resistance for example is R_{con} = -(5 ± 3) x 10^4 Ωcm.

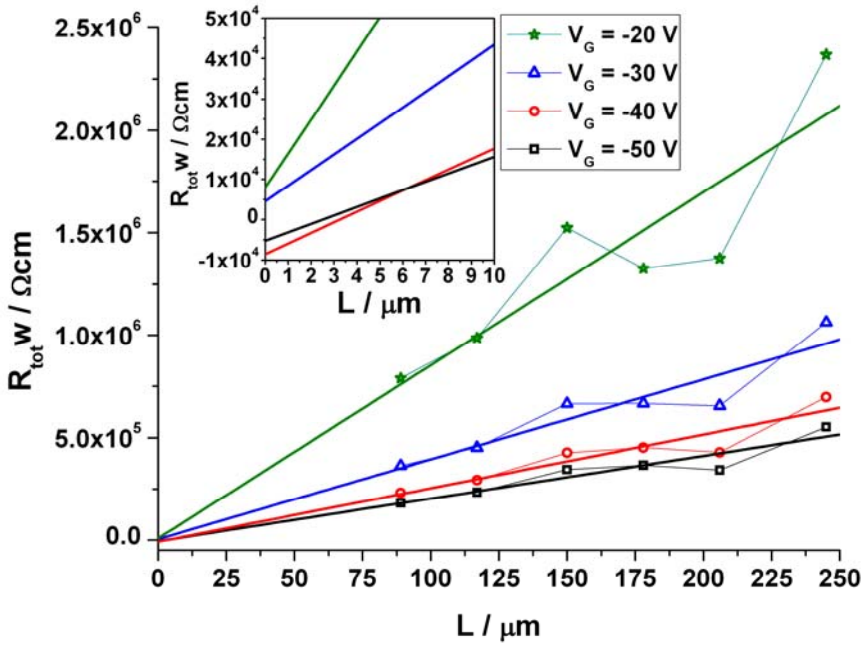

Figure 7.10) TLM – plot for an exemplary device series, measured with a drain bias of -10 Volts and shifted to a common onset voltage of zero volts. Inset) Magnification of the short channel region ranging from 0 to 10 µm showing the negative y-axis intercept.

Nevertheless this data show a clear trend, namely a decreasing contact resistance with increasing gate voltage. This could be interpreted as an indication, that the contact resistance is quite low in this set of devices. Nevertheless great care has to be taken.

Table 7.2 sums up the contact resistances for the 3 different drain voltages that were extracted as measured, showing that the contact resistance also has a small dependency on the drain voltage.

Table 7.2) Contact resistances obtained from the TLM method at a gate voltage of V_G = -40V for different drain voltages. The error margin given in this table is the statistical error when fitting a straight line and ignores all systematical problems

V_D	R_{con} / Ω	Δ R_{con} / Ω
-2	2×10^4	1×10^4
-5	1.5×10^4	0.9×10^4
-10	1×10^4	0.3×10^4

Unfortunately, it was never possible to decrease the device-to device variation to acceptable orders of magnitude. The reason why the devices differ that much even on the same substrate is not easily answered. A different pentacene growth for each device could be the reason. Nevertheless, the temperature dependent measurements were performed and even – for the sake of completeness – a temperature dependence of the contact resistance was extracted. Again, the results should be handled with great care.

7.2.2) Measurements at elevated temperatures

During a first set of experiments, it was tried to measure a complete set of characteristics for every device in a temperature range from room temperature (28° C) up to 110° C. These first experiments were performed with the THS – heating stage in the argon glovebox. Unfortunately it was not possible to receive any good transfer curves with this measurement setup.

a) further experiments: (SIMcard holder in cooling/heating stage)

The next measurements were already performed with the “new cooling/heating stage” (section 3.2.5) with the device being contacted in the SIMcard holder and stored under a nitrogen atmosphere during electrical characterization. An exemplary plot of a device is shown in Figure 7.11 in the temperature range from room temperature (25°C) to a temperature of 110°C. The on-current and, consequently, the mobility increase with increasing temperature, and the threshold voltage is shifted by some volts into the positive direction. This happened for all devices under observation and with this measurement setup. At even higher temperatures the gate leakage current began to increase characteristically and the mobility at first saturated and then decreased again. Because of the high leakage currents, those measurements are not shown here.

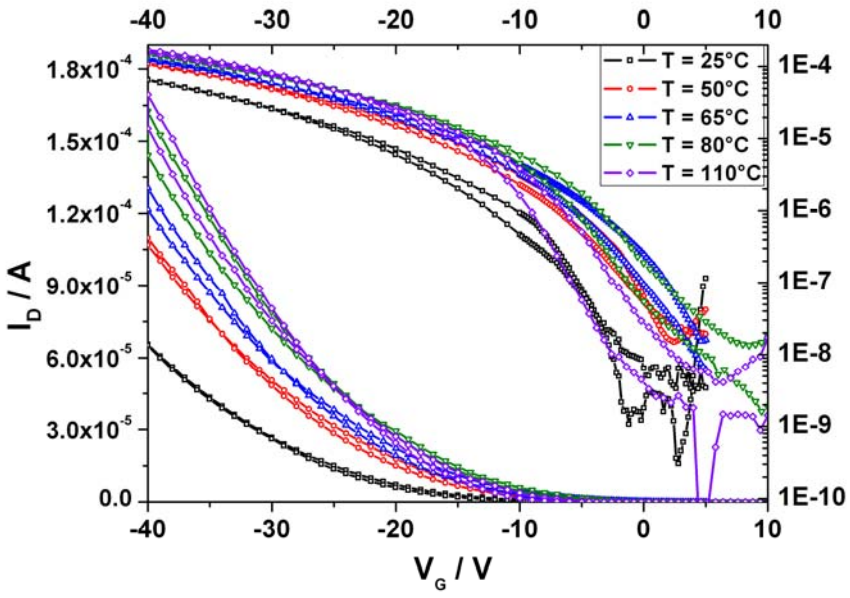

Figure 7.11) Exemplary transfer curves (in this case dev3) for OTFTs at elevated temperatures. The on-current and consequently the mobility increase.

These transfer characteristics were used to evaluate the mobilities of the transistors in the linear regime. Additionally the TLM-method was applied for all temperatures (except for 110°C where already some of the transistors were destroyed or influenced by a high gate leakage current). All results can be seen in Figure 7.12.

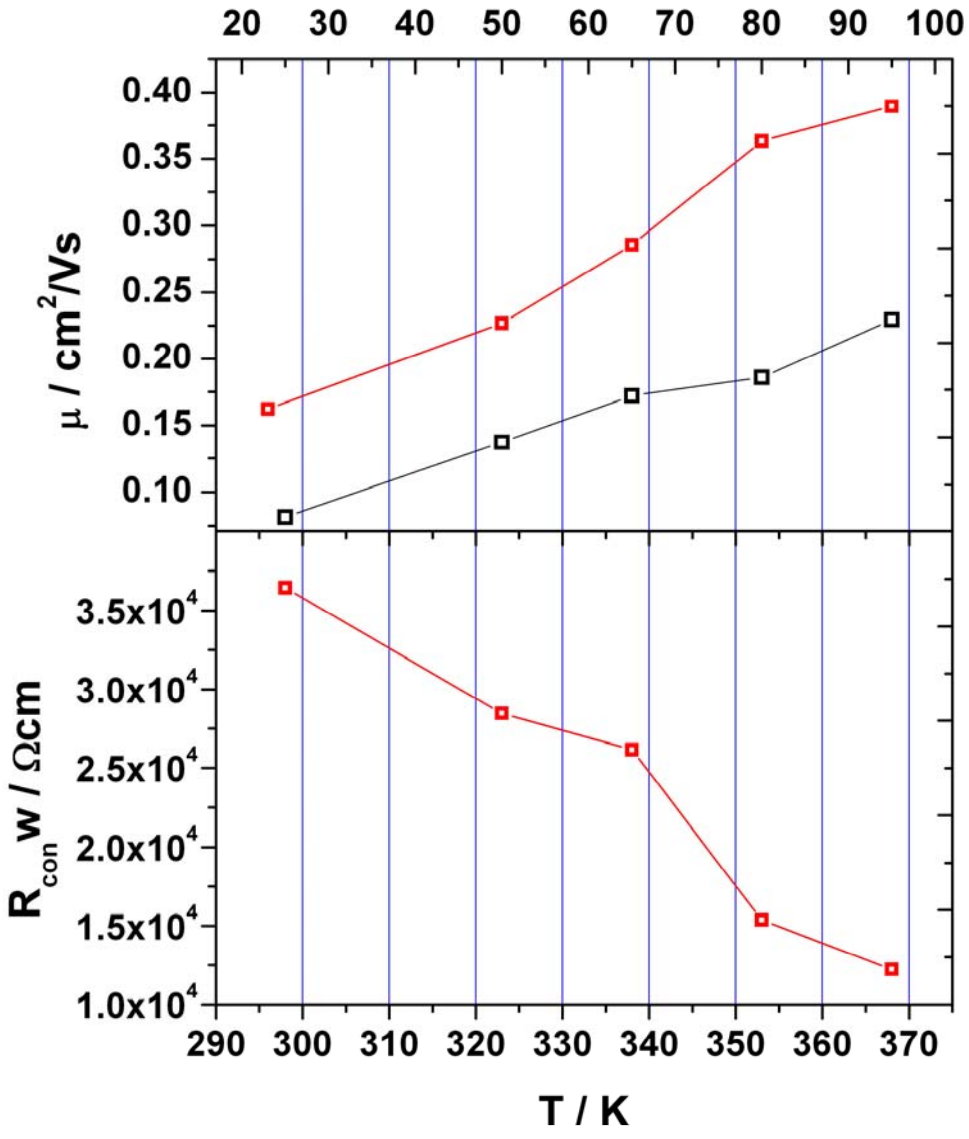

Figure 7.12) top) Temperature dependence of the mobility for high temperatures; the red line corresponds to the mobility as evaluated from Equation 2.1, the red line corresponds to mobility values corrected for the contact resistance (Equation

7.4); bottom) Temperature dependence of the contact resistance for high temperatures.

In Figure 7.12 two sets of datapoints, for the mobility are given. The red mobility values were calculated without correcting for the contact resistance with Equation 2.4, while the black datapoints correspond to a contact resistance corrected mobility. Since all measurements were performed with small drain and gate voltages, the contact resistance corrected mobility values are smaller.

7.2.3) Measurements at low temperatures

Measurements at low temperatures were conducted in the SIM-card holder with the same setup as for the measurements at elevated temperatures. The cooling was performed with liquid nitrogen, while the device was stored in a nitrogen atmosphere. During the cooling the next measurement temperature was manually chosen, and then the cooling was performed automatically. To get the real temperature of the transistor in the SIMcard holder, a second temperature sensor was inserted into the cooling chamber in close proximity to the device. Figure 7.13 shows the error between OTFT temperature and the temperature of the cooling stage. The difference between these two temperature measurements is a result of a bad thermal contact of the transistor to the cooling finger in the measurement chamber. In the measurement chamber the TFT is contacted inside a plastic SIMcard holder, which causes this bad thermal contact.

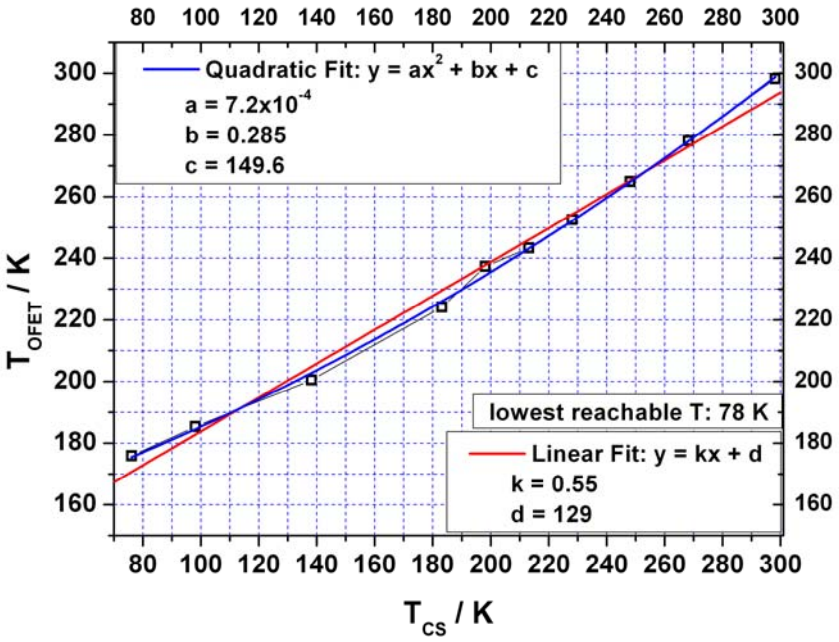

Figure 7.13: Offset between the temperature of the TFT and the nominal temperature of the cooling stage. The red line is a linear fit, and the blue line a polynomial fit. All temperatures were calculated with the polynomial fit.

Exemplary transfer characteristics for a full cooling cycle are shown in Figure 7.14. The mobility decreases with decreasing temperature and the threshold voltage is shifted to more negative voltages.

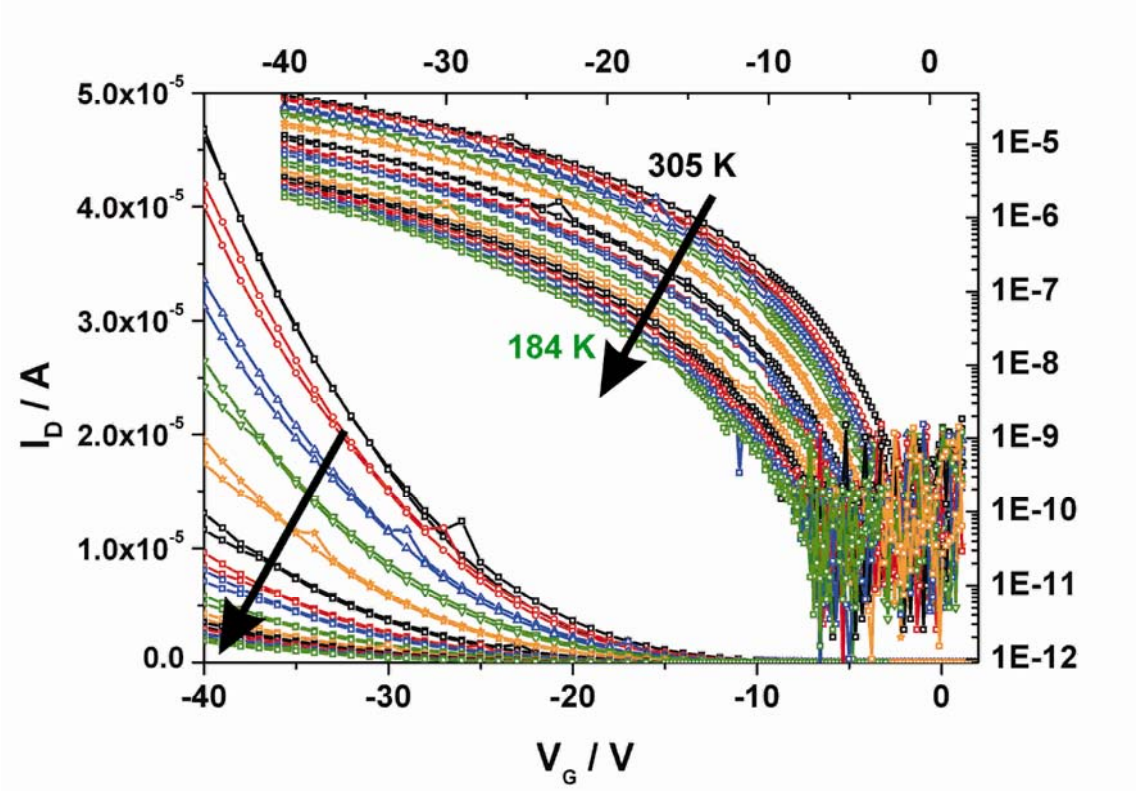

Figure 7.14) Exemplary transfer curves for a pentacene TFTs (dev5) for a temperature measurement from 305 K to 184 K. The arrows in the figure show the direction of decreasing temperature.

Again, the mobility follows the Arrhenius relationship of the MRT model yielding an activation energy of E_A = (113 ± 5) meV when using Equation 2.5 for its determination. Also the contact resistance follows a similar relation (E_A = (137 ± 10) meV). Additionally the mobility was corrected for the contact resistance in this plot, yielding a slightly larger activation energy of E_A = 147,4 8meV).

Figure 7.15 sums up the temperature dependence of both parameters.

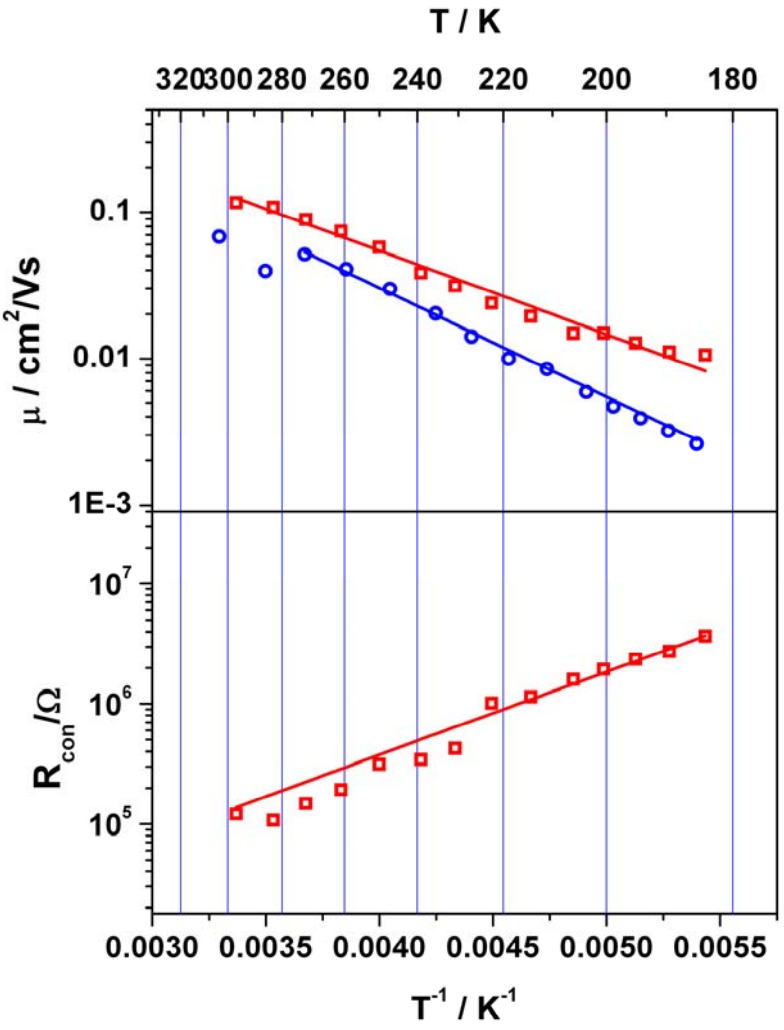

Figure 7.15) top) Mobility of a pentacene TFT with a channel length of 178 µm (dev1) as a function of temperature (evaluated in the linear regime of the off-to-on sweep. The red line is a fit to the Arrhenius relationship yielding an activation energy of E_A = (113 ± 5) meV meV; The second blue dataset corresponds to the mobility values of the same device but corrected for the contact resistance with Equation 7.1. The activation energy is 147,4 ± 8 meV bottom) Contact resistance as a function of temperature for the same device as in the top part of the picture. The red line is a fit to an Arrhenius relationship leading to a similar activation energy as for the mobility. E_A = (137 ± 10) meV

Additionally Figure 7.16 shows the temperature dependence of the threshold voltage and again of the mobility.

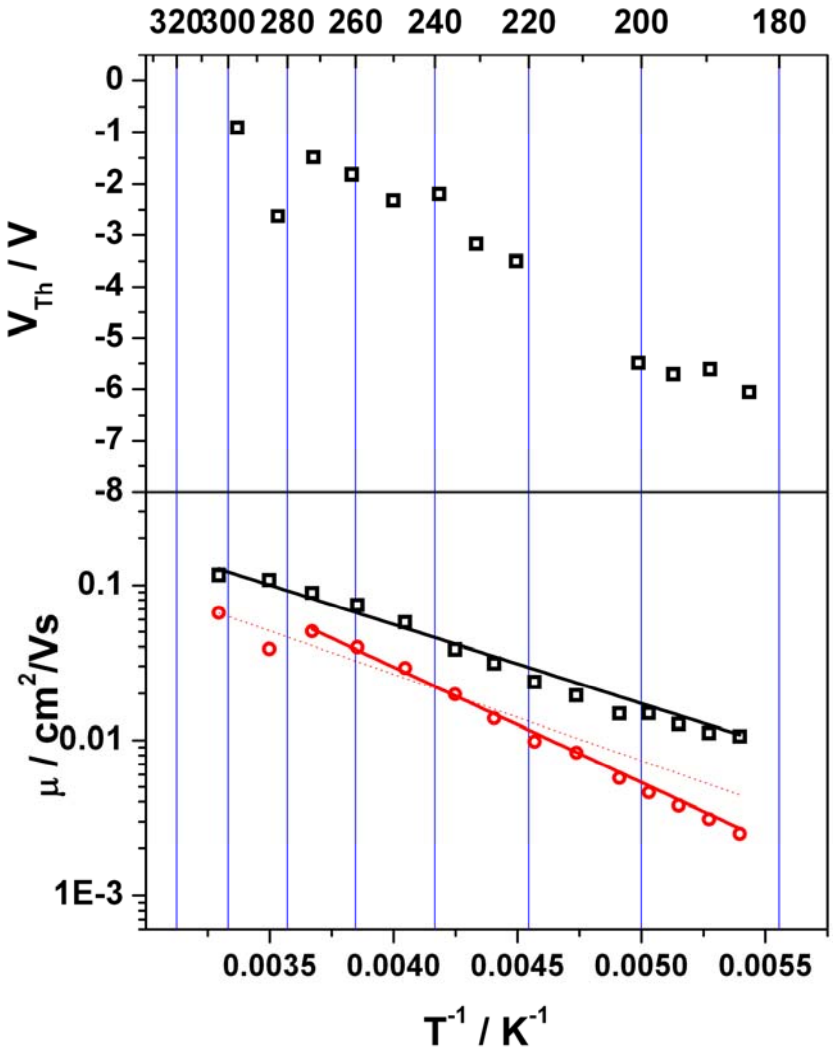

Figure 7.16: top) temperature dependence of the threshold voltage and bottom) temperature dependence of the mobility in the linear regime of a pentacene TFT with a channel length of 178 µm. The black datapoints correspond to the mobility (E_A = 113 ± 5 meV) and the red datapoints correspond to the mobility values corrected for the contact resistance (E_A = 147.4 meV)

Though it is not possible to mathematically extract a numerical value for the contact resistance, we still have the possibility to estimate its magnitude. When comparing the room temperature mobilities and the activation energies of devices with differently long channels, we should see a dependence on the channel length for both parameters, if those devices have a big contact resistance. Figure 7.17 shows the temperature dependence of all six devices on one substrate.

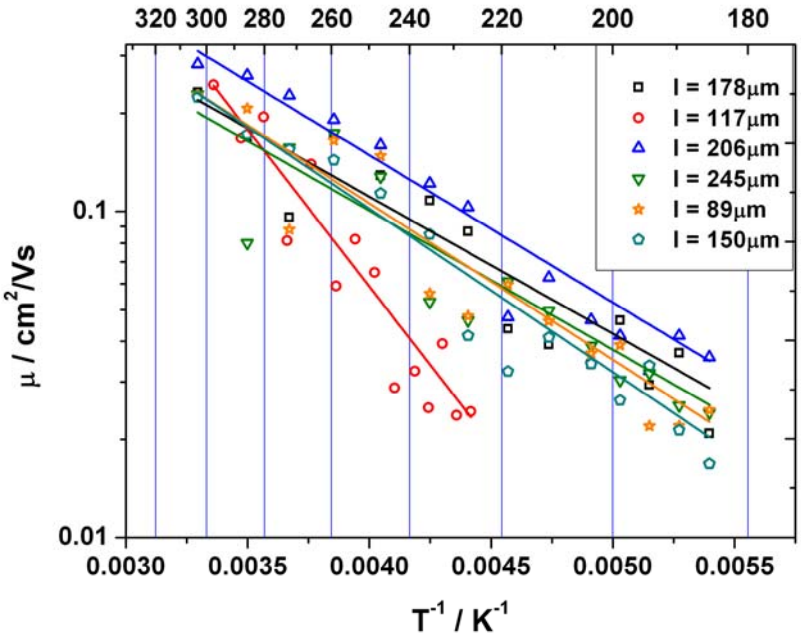

Figure 7.17: Temperature dependence of the mobility, (calculated in the saturation regime) for six pentacene transistors with different channel lengths. The red line corresponds to a damaged device and was omitted for the later evaluations.

As one can already estimate from this plot, the channel length does not have any systematic influence on the room temperature mobility, or the activation energy of the mobility. To clarify this more, Table 7.3 shows the extracted values for the room temperature mobility and the activation energy.

Table 7.3. Room temperature mobilities μ_{RT} and activation energies E_A for devices on one substrate with different channel lengths L.

L/µm	μ_{RT}/cm²/Vs	E_A/mV
89	0.23	95.2
150	0.22	99.4
178	0.23	83.4
206	0.28	89.6
245	0.23	84.6

It can easily be seen from Table 7.3, that both variables do not depend systematically on the channel length. This can mean only one thing – given that the theory of splitting the whole resistance in a TFT in a channel and a contact resistance is accurate - : the contact resistance is quite small in this kind of devices. If the contact resistance would be dominant a clear dependence of the mobility and the activation energy on the channel length should be observable. This is the second indication (in Figure 7.10 we already could estimate a quite small contact resistance) that these top-contact devices are not dominated by the influence of the contact resistance.

We also want to explain at this point, why the activation energies in this chapter are 4 to 5 times higher, than in the case of the plain devices in chapter 6. This question is easily answered, if one also compares the room temperature mobilities in both cases. A room temperature mobility of μ_{RT}= 0.23 cm²/Vs is also 4-5 times lower than the room temperature mobility of plain devices in chapter 6 (or 2 times smaller than the mobility in case of Parylene C devices). These two findings both indicate that the pentacene growth for all the transistors of the present chapter was not ideal, and that the typical grain size was quite small.

Since it was not possible to get any definitive data on the contact resistance within this subsection, we tried a completely new approach in the next section, with a completely new device setup and a new production technique for OTFTs.

7.4) Contact resistance evaluation for bottom-contact pentacene OTFTs produced with Nanoimprint Lithography

Since it was not possible to generate reproducible and trustworthy data with the shadowmasked TFTs, the TFT-design setup was changed, in the hope to build more reproducible devices. Therefore, this section all devices were processed via Nanoimprint lithography. This leads to two big differences concerning the device geometry. On one hand, the NIL technology allows for much smaller channel lengths in the order of some 100nm and, on the other hand, all devices are in the bottom-contact geometry. The hope was, that with the NIL-technology it would be easier to reduce the device-to-device variance to an acceptable order of magnitude. Due to difficulties with this new technology and problems with the contacting in the temperature measurement stage the analysis of these devices was only performed at room temperature. In future also temperature dependent measurements are planned. This subsection will start with a short introduction to Nanoimprintlithography, which will closely follow the introduction of a proposal, that was sent to the FFG under the project title “Device simulation and temperature dependent measurements of critical OTFT parameters for the optimisation of the semiconductor growth in NIL-processed active devices” (NILsimtos).[12] Afterwards the new device geometry will be introduced and the results of the room temperature measurements will be presented.

7.4.1) Introduction

Nanoimprint Lithography (NIL) is a novel but highly demanded method for patterning objects down to the range of some nanometres. Downscaling the critical dimensions of electrical components (like, for example, the channel length in field effect transistors) is one of the master strategies in semiconductor industry[13] to increase performance and speed and to decrease power and area consumption of electronic circuits. With commonly used patterning technologies, like printing or photolithography it is almost impossible to achieve channel lengths below 5 µm with organic materials.[14] This translates to a maximum cut-off frequency in the 10kHz range. Though this is sufficient for low level applications like electronic newspapers[15] or disposable sensors,[15] more advanced products in the field of organic electronics need higher speed. This applies, for example, to RF-ID tags or intelligent sensor networks.[16-19]

There have been several papers over the last years which report on the fabrication of OTFTs with channel lengths below 1 µm.[20,21] Most of them refer to e-beam lithographic patterning of gold electrodes on top of the gate dielectric $Si0_2$. Most of those devices also have a common gate electrode.[22,23] This process has several drawbacks. On one hand, e-beam lithography is a very slow serial patterning process which does not have the industrially requested potential for low-cost production. One the other hand, the $Si0_2$ gate dielectric always involves an expensive high temperature process which is not compatible with the demand for organic electronics on flexible plastic substrates. In order to realize the low-cost advantage of using polymers also the patterning process must have a high throughput, and should be inexpensive. At best it also should be compatible to a reel-to-reel process.

The NIL-process has all above-mentioned advantages. The high resolution of this process is particularly suited for defining the channel lengths in OTFTs, by depositing the electrodes of the devices by nanolithography.[24] Until now the fabrication of polymer thin-film transistors with channel lengths L < 100nm have been demonstrated on $Si0_2$.[20] On flexible plastic substrates channel lengths around 400nm have already been produced by hot embossing.[25]

Hot-embossing is a special kind of nanoimprint lithography and was used for the structuring of the source-drain electrodes throughout this work. The production steps for OTFT-production can be seen in Figure 7.18. The substrate used here is a 1x1cm silicon wafer with a 100 nm thick layer of thermally oxidized $Si0_2$. On each wafer 6 transistors are located having a common gate structure. For the structuring of the source-drain electrodes, a hard stamp with the same source-drains structure is necessary. It was realized through a silicon stamp that was fabricated by e-beam lithography.

In the first step of the imprinting process the silicon wafer is covered with an imprint resist (mr I7030 by Microresist). The stamp has to be aligned with the substrate (step A) which is not the problem here, since no structured gate electrodes exist.

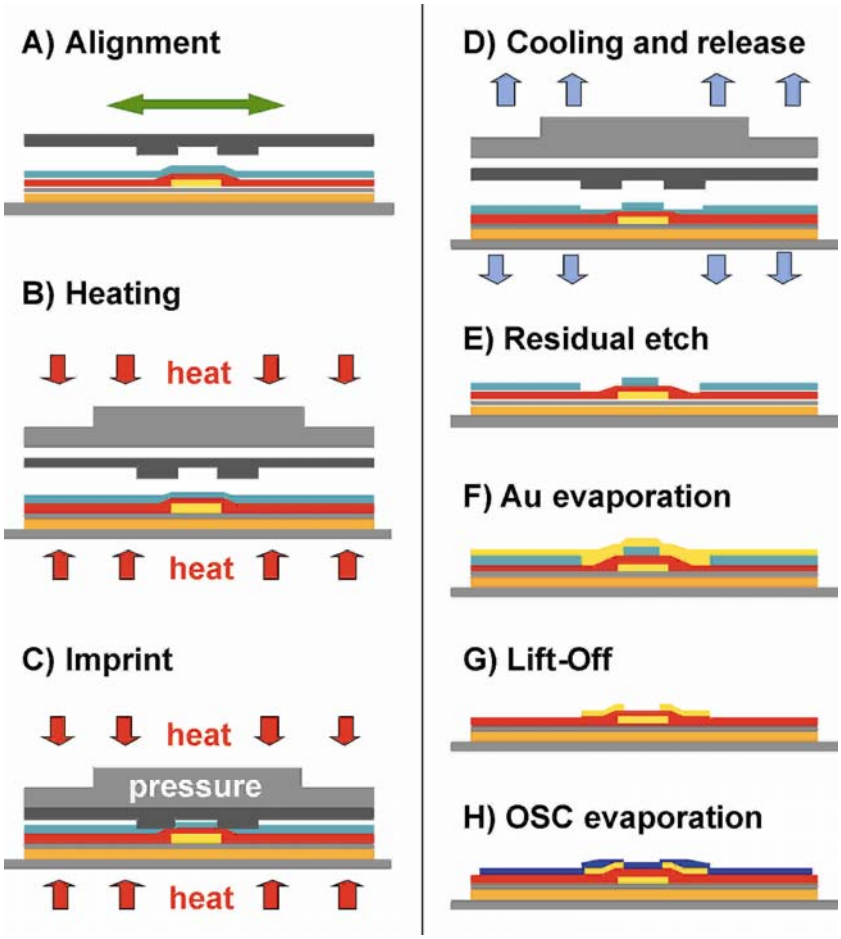

Figure 7.18) Scheme of the NIL process. In comparison to these scheme the transistors that were produced for this chapter, did not have a structured gate. The NIL-process scheme was taken from Reference 26.

After that stamp and substrate are transferred to the imprinting tool (EVG 520) where the stamp is brought into contact with the substrate. They are heated up to 140°C (step B) which is high above the glass transition temperature of the resist (TG = 60°C). Now the stamp is pressed into the resist layer with a force of 1200 N for 5 minutes (step C). Through this force almost the full resist is displaced by the stamp, with only a thin residual layer with an approximate thickness of 50nm remaining on the substrate. Now the whole system is cooled down again to 60° C with the pressure remaining constant to allow the resist to harden again. After release of the stamp at this low temperature the resist has the same structure as the stamp (step D). The thin residual layer of the imprint

resist is now removed by a short anisotropic oxygen plasma etch (step E). Now 40 nm of Au are e-beam evaporated onto the whole substrate (step F). After that the whole sample is rinsed in acetone which dissolves the remaining imprint resist and consequently only the gold structures on top of the SiO_2 surface remain (lift-off step G). In the end pentacene is evaporated thermally through a shadow mask directly into the region of the source-drain electrodes. The typical pentacene thickness was 40nm as measured by a quartz microbalance. The first 5 nm of pentacene were evaporated with a rate of 2 Å/min and the remaining 35nm with a rate of 8 Å/min. A more detailed description of the NIL-process can be found in Reference 26. It should also be mentioned here, that the whole NIL process, was performed at the NMP Weiz by A. Haase, A. Fian & coworkers. In principal the TFTs are finished after this step, but to allow for a contacting through the SIMcard holder (which was necessary for the temperature dependent measurements) 2 subsequent steps followed. At first a sticking layer was evaporated again through a shadow mask. This sticking layer is necessary since gold itself would not stick onto the silicon dioxide surface. As sticking layers either 5nm of chromium or a thin layer of aluminium nitride was used. Afterwards gold is vacuum evaporated through a shadow mask onto this sticking layer to form the contact pads.

7.4.2) NIL-Device setup

The device configuration for the nanoimprinted TFTs looked the same as device setup II. Again six transistors with different channel lengths were placed onto one substrate. The small geometries in the middle of Figure 7.19b actually correspond to the nanoimprinted TFTs. In 7.19c one nanoimprinted TFT can be seen. The lattice structure, to the left and the right in this picture, corresponds to the gold pads, which were made with NIL. [The “fence-type” structure is necessary, since a stamping would not be possible if this pad would be closed] To allow for a contacting in the specimen holder for the temperature dependent measurements, another layer of gold had to be deposited through a shadow

mask to reach the same device geometries as in OTFT-setup II. This can be seen in Figure 7.19. This second contacting step (to contact the NIL-pads with a shadow mask evaporated gold layer, to allow for a contacting in the SIMcard holder) also proofed the most difficult one in the whole device production setup. Since the gold would not stick onto the plain silicon dioxide surface an additional sticking layer was necessary. A lot of organic and inorganic sticking layers had to be tried, but in the end with poor results (vide infra). In the end two types of experiments were performed. In the first experiments, the devices were contacted in the SIMcard holder at the shadowmask gold pads, which can be seen in Figure 7.19a. Since this type of contacting most of the time yielded poor results, another set of experiments was performed, where the NIL-contacts ("fence-type structure in Figure 7.19c) were directly contacted with nano-needles in the glove box

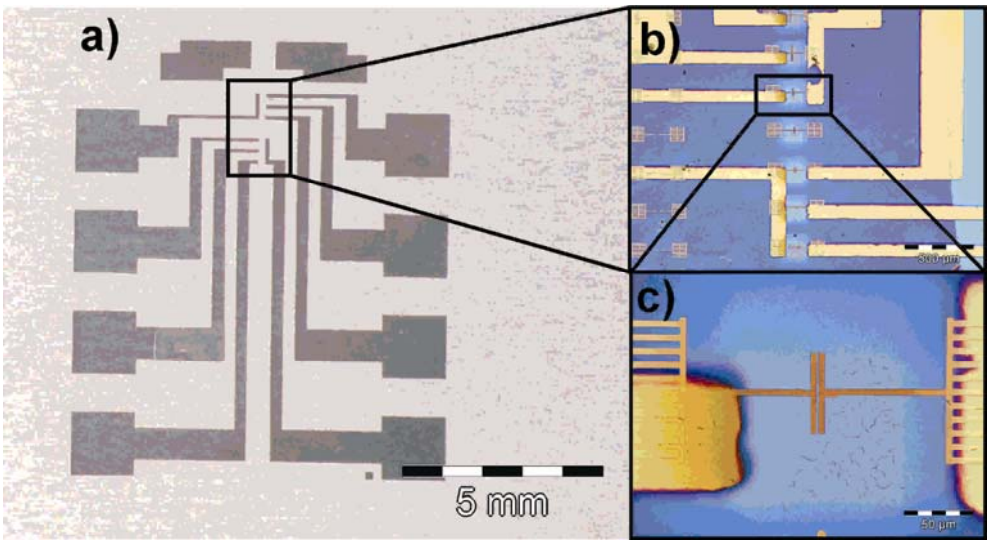

Figure 7.19) a) Layout Scheme for NIL-devices; b) closer look at the device setup. On each side of the substrate are 3 drain pads and 1 source pad; c) closer look at one NIL-processed transistor.

Table 7.4 sums up the channel lengths and widths for all six NIL-devices and the two different layout schemes used on one substrate. The channel lengths are two to three magnitudes lower in comparison to all earlier evaluated TFTs.

Table 7.4 Properties of each transistor with the two different NIL-masks that were used for the imprint.

	Design Scheme I		Design Scheme II	
OTFT number	**L / nm**	**W / mm**	**L / nm**	**W / mm**
dev1	1200	0.06	300	0.015
dev2	900	0.045	400	0.02
dev3	800	0.04	600	0.03
dev4	700	0.035	900	0.045
dev5	600	0.03	1200	0.06
dev6	500	0.025	2400	0.12

7.4.3) Measurements at room temperature

The TFTs have been measured in two ways. On one hand, they were contacted in the glovebox and measured with needles via the gold pads fabricated using the shadow mask (as were all devices before); unfortunately it was not possible to achieve any satisfactory results (as can be seen in the next subchapter). The devices discussed in that subchapter had a sticking layer made of chromium.

On the other hand, the TFTs could also be contacted directly at the gold pads, fabricated by Nanoimprint lithography. This in the end allowed to measure reproducible results and allowed to apply the TLM-method at least at room temperature. There was no way to perform temperature dependent measurements with this setup, since the small NIL pads, could not be externally contacted with a SIMcard holder. This later devices had a sticking layer consisting of aluminium nitride.

a) contacting via the "shadow-mask" gold pads

Typical transfer curves for the NIL-transistors on one substrate are shown in Figure 7.20. Again we have the same problem, as with shadowmasked transistors – a big device to device variance. Moreover it was impossible to find 6 working transistors on one substrate. Figure 7.20 shows again a "best result", with 5 working transistors. From the transfer curves it is again highly questionable, that the TLM-method is applicable.

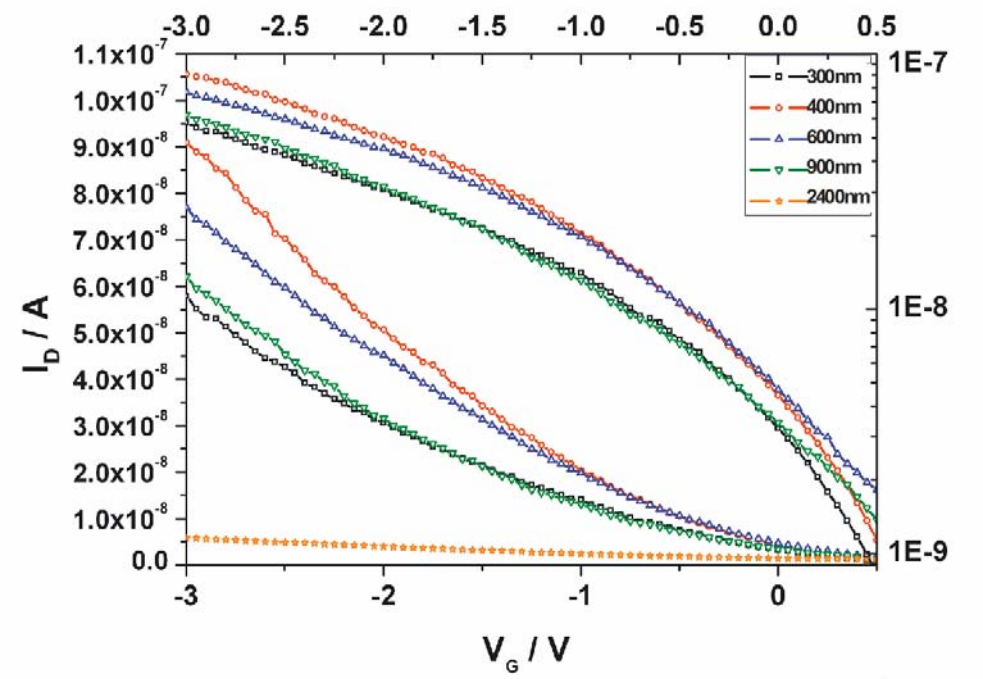

Figure 7.20) Exemplary transfer curves for 5 of 6 NIL-transistors on one substrate. The orange line was omitted in the logarithmic plot for good visibility.

Nevertheless the TLM analysis was conducted. It, however, did not yield any meaningful results as can be seen in Figure 7.21.

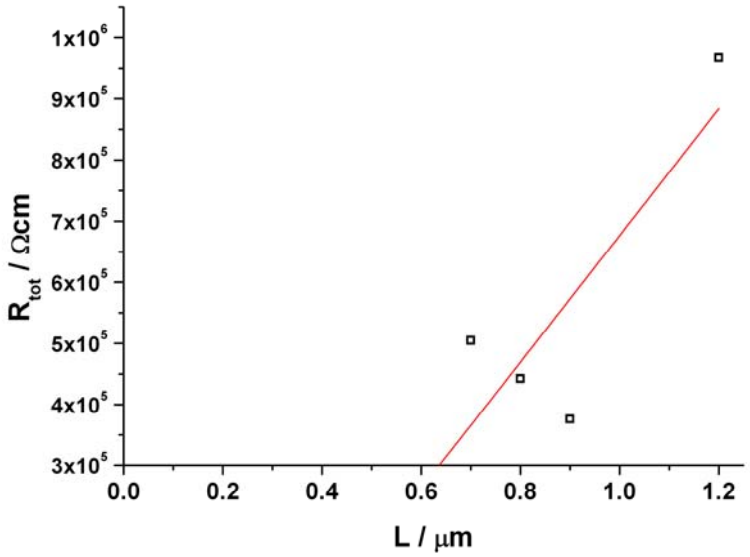

Figure 7.21) "TLM-plot" of a set of NIL-transistors yielding a negative contact resistance.

Since it was never possible to get usable results, when contacting the TFTs at the outside shadowmasked electrodes, it was tried to measure the devices directly at the NIL-pads.

b) contacting of the nanoimprinted pads

It is a well known fact from literature that the contact resistance in bottom contact TFTs is generally much higher than for top contact TFTs.[27-30] Following Scheinert et al.[30] such a high contact resistance can easily be verified when looking at the output curves of organic TFTs. In the low drain-source voltage region of the output characteristic a nonlinearity should be visible.
Figure 7.22 shows an output characteristic, with a significant nonlinearity in the low drain-voltage region, indicating that these bottom-contact transistors really have a high contact resistance.

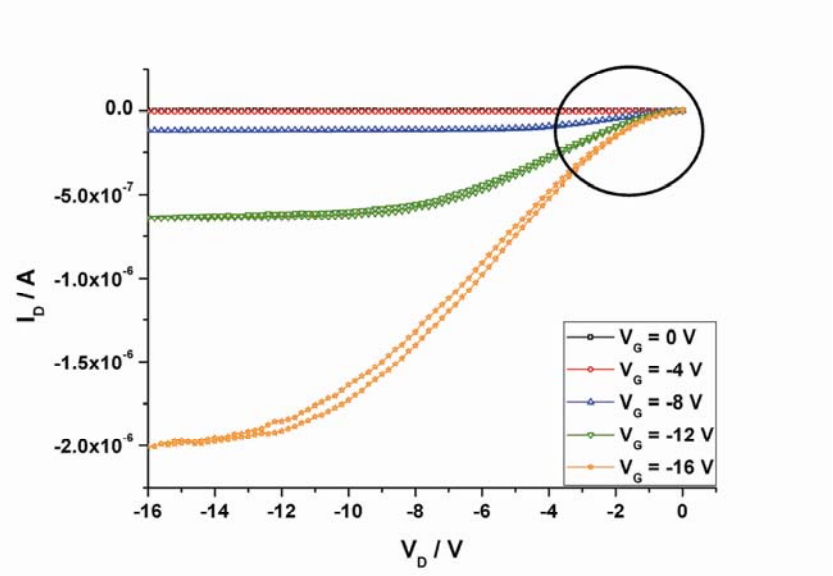

Figure 7.22) Exemplary output field for a NIL fabricated bottom contact transistor, contacted directly at the nanoimprinted pads. In the low drain voltage region a significant nonlinearity can be seen.

Figure 7.23 shows the corresponding transfer curves of 4 working transistors on one substrate (there were again 6 transistors on every substrate, though never all of them worked). On the first glance the transfer curves look quite uniform and also a closer look affirms that the threshold voltage is in the same voltage range for all four measurable devices.

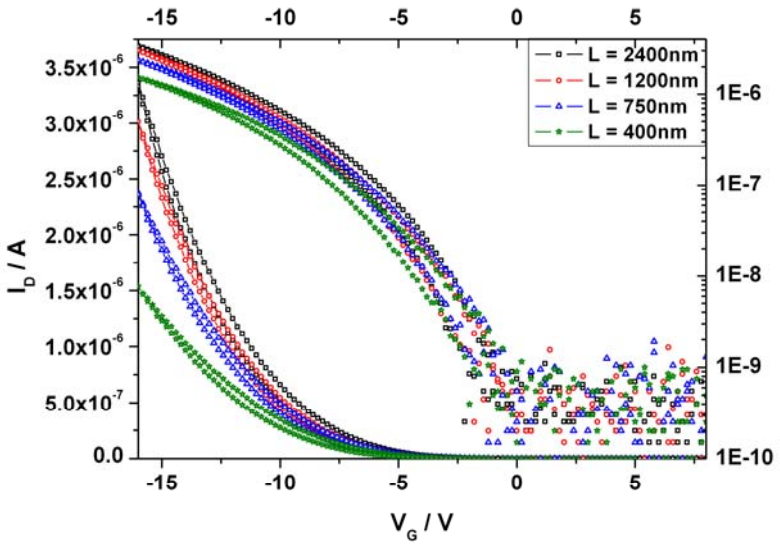

Figure 7.23) Exemplary transfer curves for 4 of 6 NIL-transistors on one substrate. Mobility and threshold voltages of all devices are in the same order of magnitude

Thus, the TLM method was applied, which can be seen in Figure 7.24. For the first time, the method actually works. A clear trend is visible in the plot, showing an increasing total resistance with increasing channel length.

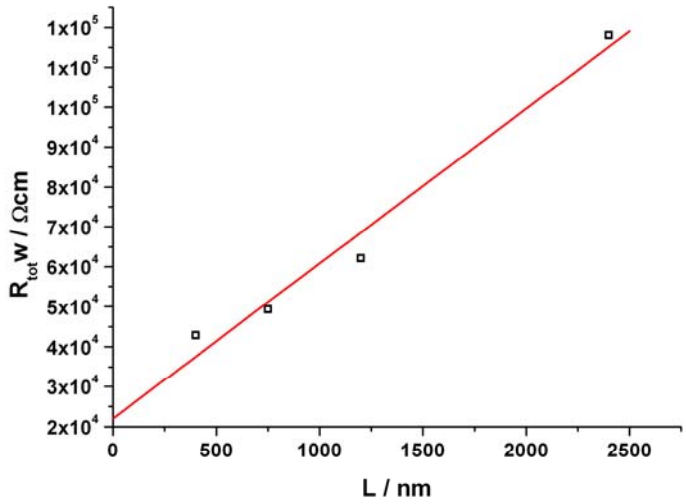

Figure 7.24) TLM-plot of a set of 4 NIL-transistors, for a gate voltage of -16 V and a drain voltage of -8 V.

The value obtained for the width normalized contact resistance $R_{con}w$ (V_G= -16V & V_D = -8V) = (22 $\pm$ 6) x 10^4 Ωcm and significantly higher in comparison to the results for top-contact devices.

7.5) Conclusion

In this chapter two different types of TFTs were investigated; on the one hand, top-contact TFTs with channel lengths in the hundreds of micrometer scale, which were evaporated through a shadow mask, and on the other hand, NIL-fabricated bottom-contact TFTs, with channel lengths of some ten nanometers.

When looking at the results for the top-contact TFTs, we have to do this with caution. Although all results seem to fit to the results obtained from literature they should be handled with great care for above mentioned reasons.
Since the total resistance in the TLM plots showed no clear dependency on the channel length it is difficult to justify all later obtained results. The big device to device variation and the non-uniformity of the threshold voltage make it impossible to apply the TLM-method and get any reliable results. Nevertheless we got two indications that these devices do not have a very big contact resistance. On the one hand, when applying the TLM-method to transistors, which were artificially set to a uniform onset voltage of V_{on} = 0 V we could extract very small (or even negative) values for the contact resistance. On the other hand, devices with differently long channels had the same room temperature mobility and the same activation energy.
In future, in order to obtain really reliable results, it is important to decrease the device to device variance in the first place.

Concerning NIL-transistors, the reproducible production of NIL-transistors for temperature dependent measurements and a temperature dependent analysis of the contact resistance was unfortunately not possible due to various problems:

- The gold wires and contact pads that were vacuum evaporated through a shadow mask made the device to device variance to high for the TLM method.
- Additionally there were still problems with the electrical contact between those gold pads and the SIM card holder.
- Since devices could only be measured at the nanoimprinted contact pads, the recording of temperature dependent data was impossible.

Therefore the analysis was only performed at room temperature and only when directly measuring the TFTs via the nanoimprinted pads satisfactory results were possible. This at least proofs that the production of TFTs with the NIL-technique is possible and that a analysis of the contact resistance with the TLM method is possible. As expected from literature the contact resistance is much higher for bottom contact NIL transistors than for top contact shadowmask transistors.
In the future also temperature dependent measurements should be possible as soon as the problems with the electrical contacts between the nanoimprinted pads and the shadow masked “measurement”-pads can be overcome.

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