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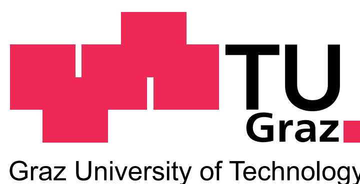
Controlling Proton Transfer Doping of Organic Thin-Film Transistors by Acidic Polymer and Self Assembled Molecular Layers

MASTER THESIS

For obtaining the academic degree
Diplom-Ingenieur

Master Programme of
Technical Physics



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Graz, November 2011

Deutsche Fassung:
Beschluss der Curricula-Kommission für Bachelor-, Master- und Diplomstudien vom 10.11.2008
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Acknowledgements

Above all I want to express sincere thanks to my supervisor Prof. Dr. Egbert Zojer for his guidance and also patience. His vast knowledge in science, the awareness of latest literature paired with the permanent willingness for advices and discussions constitute a fruitful framework for scientific team work. The great degree of freedom but still a permanent support made it a honor for me to be a part of his group.

Likewise I am especially grateful to Simon Außerlechner for his help and companionship during my thesis. In this sense I would also like to thank all group members who accompanied me in the lab and the third floor of the physics building. Work should always be combined with fun, and it was. There are few more important things than a solid caffeine level.

Furthermore special thanks to Heinz Georg Flesch, Alfred Neuhold, Jiří Novák and Markus Neuschitzer for the XRR measurements and Manfred Gruber for simulations. Same thanks are dedicated to Anja Haase and Alexander Fian from the Institute of Surface Technology and Photonics of Joanneum Research for the pentacene evaporation and AFM pictures.

Thanks to the FWF, project number P19959-IV20, for funding this thesis.

Beside the thesis related work, I would like to thank all my other friends who went with me through the physics studies. Learning, musing, discussing and arguing together was always a great pleasure. The same gratitude is directed to all my other friends, here in Graz and everywhere else. Thanks to all my bartisans for keeping me from finishing this work earlier.

Most of all of course I want to thank my family who always supported me and, ultimately, made this thesis possible.

Abstract

It was shown that several parameters of organic thin film transistors can be tuned by the application of a functionalized interface between the insulator and the active layer. One approach is acid layers at the interface, which results in a threshold voltage shift by proton transfer doping. Two different sulfonic acid layers, one based on self assembled monolayers and one consisting of a solvent processed polymer were investigated in polythiophene and pentacene devices. Threshold and onset voltage as well as the charge carrier mobility were evaluated and it was shown that proton transfer doping also occurs in pentacene devices, which results in a static threshold voltage shift of up to several ten volts.

Based on the modification of the interface layer thickness, the impact of the acid on the transistor was further studied. A characteristic linear dependence of the threshold voltage on the layer thickness was observed, whereby the SAM and the polymer layer show different impacts at the same thickness. The ability of chemical sensing was investigated by studying the influence of ammonia gas on the transistor. Measurements during the exposure show a fall of the threshold voltage while the transistor stays fully operational. These measurements, however, require further investigations since some aspects of the results cannot be consistently explained yet.

The present investigation of the impact of the interface layer thickness on the threshold voltage and the characteristic behavior during ammonia exposure finally helps to elucidate the working principle of proton transfer doping and the gas sensing ability of OTFTs.

Zusammenfassung

Es wurde bereits gezeigt, dass organische Dünnschichttransistoren durch das Einfügen einer funktionalen Schicht zwischen Dielektrikum und Halbleiter wesentlich in ihren Eigenschaften beeinflusst werden können. In dieser Arbeit wurde ein Mechanismus, der zu einem Ansteigen der Schwellspannung führt, näher untersucht. Zu diesem Zweck wurden Sulfonsäuren sowohl als selbstassemblierte Monolagen als auch als spingecoatete Polymerschichten in Pentacen und Polythiophen Transistoren integriert. Ihre Auswirkungen auf Schwellspannung, Ladungsträgermobilität und Einschaltspannung wurde weiter untersucht. Es konnte nachgewiesen werden, dass die von Polythiophen bekannte Protontransferdotierung auch bei Pentacen funktioniert. Die Schwellspannung steigt statisch von ungefähr null Volt auf bis zu mehrere zehn Volt an.

Basierend auf einer Dickenänderung der Zwischenschichten wurde der Einfluß von verschiedenen Säurekonzentrationen auf den Transistor weiter studiert. Es zeigte sich eine charakteristische Abhängigkeit der Schwellspannung von der Zwischenschichtdicke, sowohl für auf SAMs basierende als auch für saure Polymere enthaltende Bauelemente. Als weiterer Schritt wurden die Transistoren Ammoniak ausgesetzt, das als basisches Gas die Dotierung des Halbleiters rückgängig macht und so die Schwellspannung wieder senkt. Transfermessungen während des Einwirkens von Ammoniakgas zeigten die volle Funktionsfähigkeit des Bauelemente während der Expositionszeit. Einige Aspekte der Einwirkung von Ammoniak auf die Transistoren sind jedoch nicht vollständig geklärt und bedarfen noch einer weiterfürenden Untersuchung.

Die vorliegende Untersuchung der schichtdickenabhängigen Erhöhung der Schwellspannung und des charakteristischen Zurückschiebens unter Ammoniakgas hilft schlussendlich die Funktionsweise der Protontransferdotierung besser zu verstehen und einen weiteren Schritt in Richtung Sensorapplikationen zu gehen.

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Chapter 1

Introduction

A semiconductor is a material with unique electronic properties. Basically it is an insulator, but it can be made conductive by various means, reversible and non-reversible. The first switch constructed on this basis was invented by Julius Edgar Lilienfeld in 1925 [1]. This invention laid the foundation for the MOSFET technology, invented 35 years later [2], which succeeded the slow and energy consuming cathode ray tubes in logic circuits. The following minimization and integration of MOSFETs finally changed the whole world in way nobody could have ever expected fifty years ago. Today, semiconductor technology has led to the greatest democratization of technology, knowledge and information that ever happened in society. Computers, the formation of the internet, real time networks, and mobile communication over the whole planet triggered an enormous economic growth, supported democratic movements, and enabled independent reporting and media. On the other hand it should not be forgot that living, trading, and the information flow also speeded up in such a fast way, that our society, economy, and environment hardly can keep pace to it.

Beside this technologies, which are based on state of the art inventions and high performance semiconductors, there is another development, which is based more on the integration of simple electronic devices in everyday life. Here, the attention is focused primarily on cheap production and easy integration rather than on efficiency, high performance or durability. Very promising materials for these requirements are organic semiconductors. Various ways of processing, like ink-jet and offset printing, or spin coating make organic semiconductors accessible for cheap mass production, even on flexible substrates [3].

Discovered in the 1940s, [4] organic semiconductors became more and more important in the last 30 years. The basis was the invention of the organic field-effect transistor by Koezuka in 1987 [5]. Even though these materials have been a field of great interest in recent research, many of their properties are still under investigation and not yet fully understood. Three publications about the investigation of the same feature, but with contradicting conclusions, show an episode of this [6][7][8].

In the beginning of this work, the basic principles of a transistor will be discussed,

including semiconductor basics, structure, device characteristics as well as their modelling. This considerations, made for inorganic semiconductors, will be transferred to the organic thin-film transistor. Differences will be pointed out, and peculiarities of organic systems will be explained.

The experimental part, after a description of the used characterisation and experimental methods, will present the fabrication and critical evaluation of OTFTs with acidic interface layers. In the first place the development of acidic interface layers with defined thicknesses will be demonstrated. Afterwards the characterisation of transistors including these layers will show their impact on the device performance and parameters like the threshold voltage. As an alternative approach to tune the threshold voltage and in order to reverse the shift, induced by the interface layers, the effect of ammonia gas on the device will also be presented. In the last part, the outcome of this thesis will be briefly discussed and suggestions for a continuation given.

Part I

Basics

Chapter 2

A Brief Overview of Semiconductor Physics

2.1 Mobility

An important parameter for semiconductor devices is the charge carrier mobility. It describes the response of the electrons to an electric field and is an important criterion for identifying the transport mechanism. The following derivation is based on [9, p.203]. We start with the definition for the current density and the Ohm's law

$$\boldsymbol{j} = nq\boldsymbol{v_d} \tag{2.1}$$
$$\boldsymbol{j} = \sigma\boldsymbol{E} \tag{2.2}$$

with the charge carrier density n, elementary charge q, average drift velocity $\mathbf{v_d}$, conductivity σ and $\mathbf{E}$ being the electric field. Combining these equations one comes to the following expression for the conductivity

$$\sigma = nq\frac{|\boldsymbol{v_d}|}{|\boldsymbol{E}|} = nq\mu \tag{2.3}$$

The ratio between the average drift velocity and the electric field is then called *mobility*

$$\mu = \frac{|\boldsymbol{v_d}|}{|\boldsymbol{E}|} \tag{2.4}$$

This parameter has a distinctive temperature dependence [9, p.263] and cannot be measured directly, therefore, it is depending on the method of determination.

2.2 Junctions

The usual way for comparing the electronic structure of two materials is to plot their band structure in an energy diagram. Two separated solids obviously share the same vacuum level. Upon establishing contact charges will flow from one material into the other due to different workfunctions, which results in the Fermi-level alignment as indicated in picture 2.1. This charges at the interface cause a bending of the band and for materials of equal band gaps an alignment of their conduction and valence band. The extend of the bending into the bulk depends on the amount of mobile charges present respectively the ability of mobile charges to shield the potential originating from the different workfunctions.

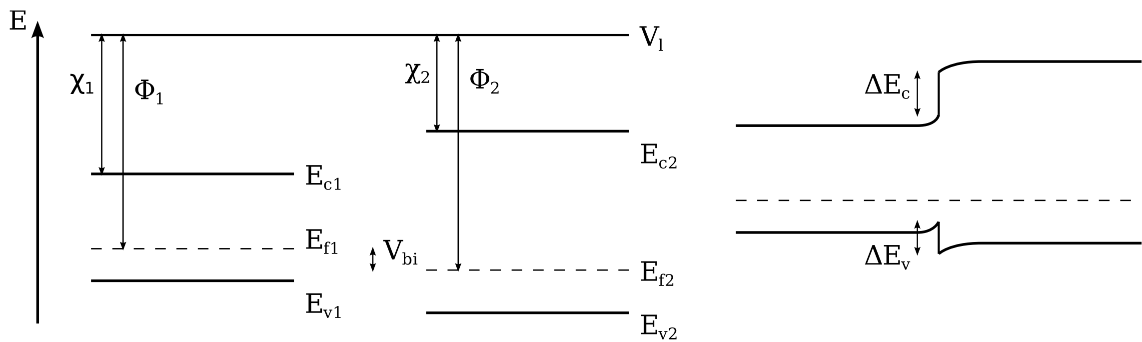


Figure 2.1: *Fermi alignment: From isolated materials to a junction in case of a heterojunction.* V_{bi} *is the built-in potential which results from different workfunction* Φ_1 *and* Φ_2 *of the materials*

2.2.1 Semiconductor-Semiconductor Junction

There are two cases, hetero- and homojunctions as depicted in figure 2.2. The former consists of two materials of different, the latter of same bandgaps respectively materials. Homojunctions form smooth bandstructures, like the typical pn-junction. Heterojunctions however inevitably form an incontinouity at the junction resulting in an energy barrier. For LEDs for instance, this barrier is a major goal since longer residence times at the junction enhance the probability of a charge recombination.

2.2.2 Metal-Semiconductor Junction

Again, different workfunctions induce a rearrangement of charges and one ends up with a band structure as can be seen in picture 2.2 on the right side. Evidently, there is no band bending in the metal due to a virtually infinite electron reservoir and high conductivity. For effective charge injection in a device it's necessary to minimize the

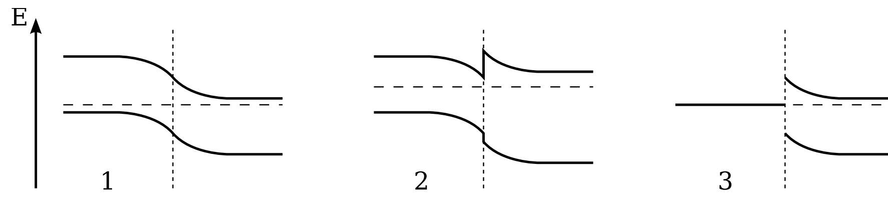


Figure 2.2: *Different junctions: 1 - homojunction; 2 - heterojunction; 3 - metal-semiconductor junction*

injection barrier for the desired charge carrier species. Therefore, the choice of the metal has to be tuned to the semiconductor and the intended charge carrier species.

For semiconductor devices different goals, like charge separation for solar cells or recombination for LEDs, make the understanding and control of junctions and interfaces the crucial factor in engineering.

2.3 Metal-Insulator-Semiconductor Structure

Loosely following reference [10], this junction will be discussed in more detail since it is the basic element of a field effect transistor. Also called MIS-capacitor, the important part of this structure is the insulator, respectively, dielectric layer, which separates the metal from the semiconductor. This prevents charge transport from the metal to the semiconductor but allows the application of electric fields by the metal contact.

Picture 2.3 shows the MIS capacitor in real space, the band diagram, and the charge distribution of a cross section in different working modes. On the left is the metal contact, where a voltage can be applied, then the dielectric layer, and on the right side of the structure is a p-doped semiconductor.

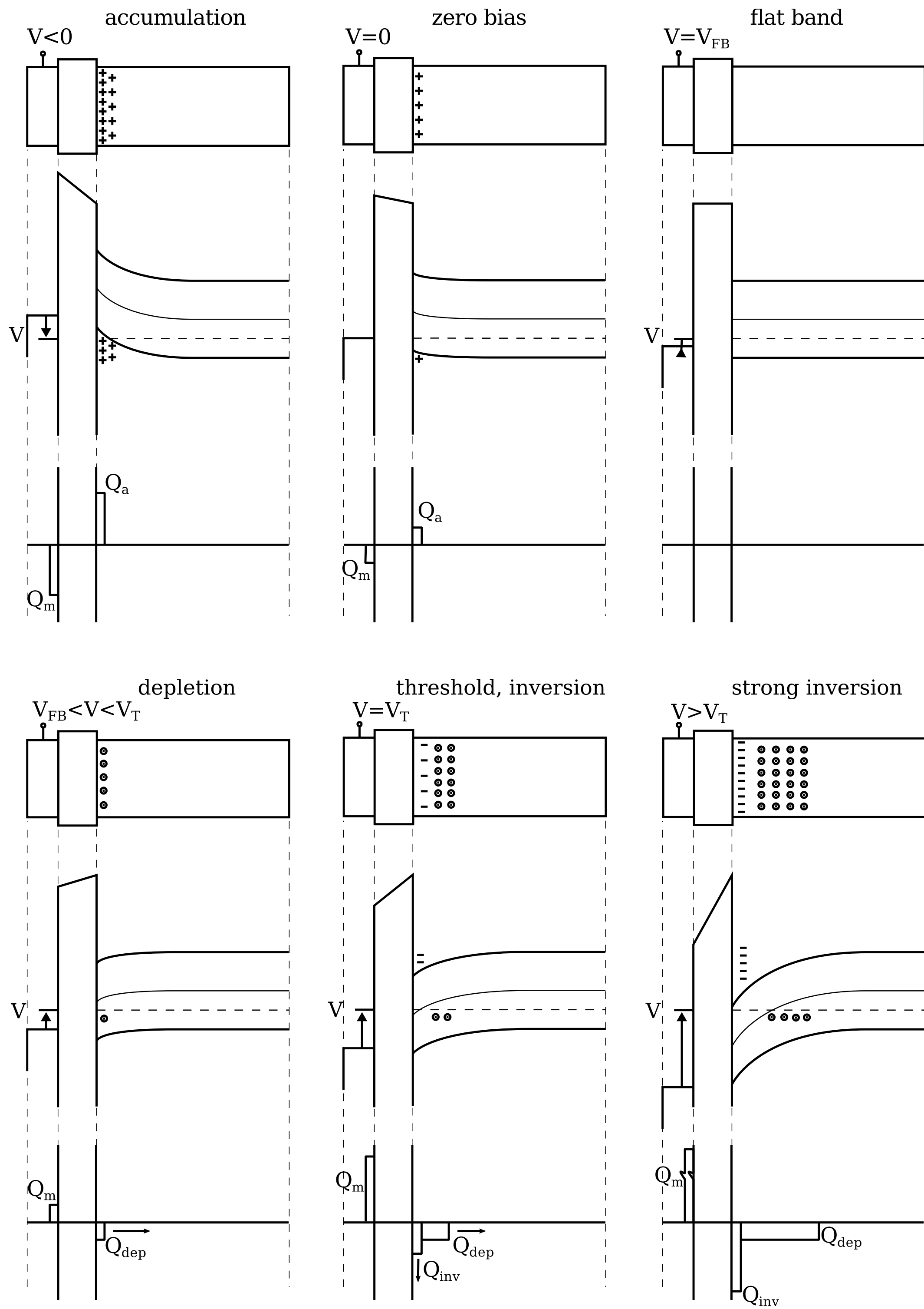


Figure 2.3: *Charges in a MIS structure under differently biased conditions illustrated in the structure, the band diagram and the charge distribution*

In *accumulation mode*, a negative bias at the metal contact accumulates mobile holes at the insulator-semiconductor surface. Like in a capacitor the negative charges are accumulated at the metal-dielectric interface by the applied voltage. At *zero bias* only the holes which originate from the doping of the the semiconductor are left, which are fully compensated by a positive bias in the *flat band condition.* In this case, the semiconductor is charge neutral. From now on, with higher voltages, a *depletion zone* forms at the interface and extends with increasing bias further into the bulk. The depletion zone originates from emptied dopants, so it's shape is depending on the dopant density. Some mobile electrons start to accumulate synchronously and form a conducting charge sheet at the interface in *inversion mode. Strong inversion* sets in when the accumulated charges exceed the dopant density.

These previous described modes coexist in the bulk as the potential decreases with rising distance as illustrated in figure 2.4.

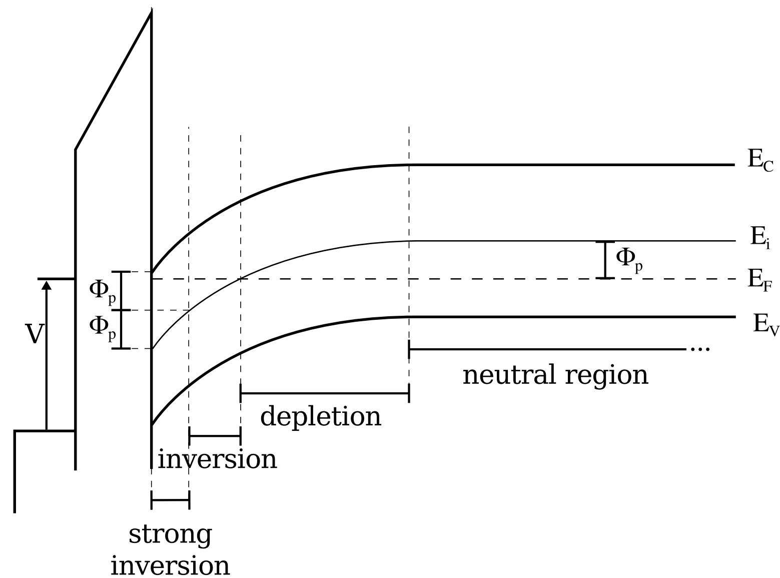


Figure 2.4: *Characteristic regions of a MIS structure: in the strong inversion and inversion zone mobile minority charge carriers are present; space charges resulting from emptied dopants form the depletion zone, based on reference [10]*

As we have seen, there are two conditions where mobile charges are generated at the interface, namely in accumulation or inversion modes. We will derive now one limiting case for the establishment of mobile charges in the semiconductor (based on reference [10]). Starting point is the flat band condition. In section 2.2 it was discussed that the workfunction difference between the two materials is responsible for the band bending. Other effects, that can cause a bending can be included by adding an artificial space-charge layer σ_{sp} and a dipole layer. The dipole layer is described by two space-charge layers σ_{dip} in the distance d_{dip} with k regarding the medium between the space-charge

layers. So for this general description the flat-band voltage V_{FB}, which corresponds to the potential at the interface Φ_{int}, reads as

$$V_{FB} = \phi_{G-SC} + \frac{\sigma_{sp}}{C} + kd_{dip}\sigma_{dip} = \Phi_{int} \tag{2.5}$$

with the workfunction difference ϕ_{G-SC} between the semiconductor and the metal contact, from now on called *gate*. C is the capacitance of the dielectric and $kd_{dip}\sigma_{dip}$.

Additional there are charges originating from a dopant with the density N_a

$$Q_a = qN_a t \tag{2.6}$$

If the charge coming from the internal potential and from the doping is set to zero we get the limiting case.

$$C(qN_a t) + CV_{FB} = 0 \tag{2.7}$$

which yields to a voltage of

$$V_T = V_{FB} + C(qN_a t) \tag{2.8}$$

that has to be applied in order to compensate all mobile charge carriers. So for $V_G < V_T$ there is a conducting charge sheet at the semiconductor dielectric interface, for $V_G > V_T$ not (valid for a p-type MIS as treated before). This threshold to inversion can be regarded as the definition of the *threshold voltage* V_T in accumulation mode.

Most inorganic transistors however are operated in strong inversion mode, which implies another derivation for the threshold voltage due to the space charge layer from the depletion zone. But as organic transistors work in accumulation regime this derivation will be skipped.

2.4 Field-Effect-Transistor

As we have seen before, it is possible to create a conducting charge sheet at the semiconductor-dielectric interface plane by applying a bias at the gate contact. Now we add two metal terminals, named *source* and *drain* at the interface and apply a bias on the drain contact, whereas the source contact is grounded. Due to the potential difference, a current will flow between source and drain, but only, and that is the important thing, if the gate contact establishes mobile charges at the interface! This also explains the contact's name, which we already introduced for the MIS capacitor. This current switching function of the gate electrode is the working principle of a *field effect transistor* as depicted in figure 2.5. The widely used *MOSFET* design of the field effect transistor works in a different way which shouldn't be mixed up with the previous

description. Here, source and drain are doped conversely to the channel, thus, one pn junction is always reverse-biased. Only if a gate bias inverts the channel a current can run from source to drain. Note that due to the isolation between the gate contact and the semiconductor there is no net current from the gate electrode and therefore the switching does not consume power in theory.

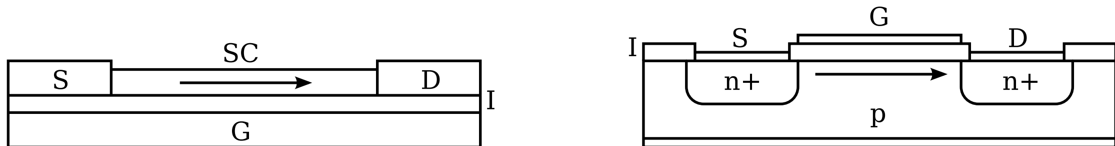


Figure 2.5: *Schematics of a field effect transistor and a MOSFET (right): S - source; D - drain; I - insulator; G - gate; the arrow indicates the current in the channel; SC - semiconductor, in the MOSFET with differently doped regions*

N-type transistors switch off at negative voltages whereas p-type do the opposite. These two types and the possibility to tailor their threshold voltage with the doping level are the basis of the *CMOS* technology.

All considerations from now on are based on a p-type FET which manifests in negative drain voltages and a conducting channel at negative gate bias.

2.4.1 Working Regimes of a FET

The gate and the drain electrode obviously interfere and define together the potential distribution in the transistor. Since the effective potential at the interface is responsible for the formation of the conducting layer one has to distinguish between two profoundly different cases.

Linear Regime

At high effective gate and small drain voltages $|V_G - V_T| \ll |V_D|$ the gate bias dominates the potential distribution in the channel. There is a nearly homogenous charge carrier density in the channel which results in an ohmic behavior with respect to the drain voltage, as can be seen in the *output characteristic* at the top of figure 2.6

Saturation Regime

If the effective potential below the drain contact equals zero one talks about the *pinch-off point*. Further decreasing the drain bias, so for $|V_D| > |V_G - V_T|$, the current starts

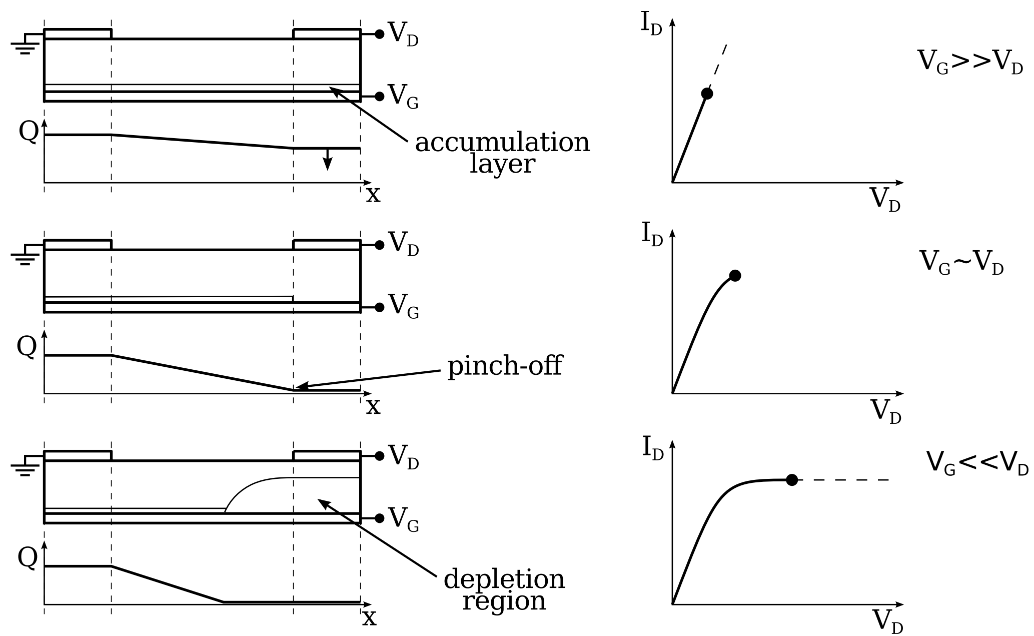


Figure 2.6: *Working regimes of a transistor: transistor view, charge density and output characteristic for three different bias situations. Picture inspired by reference [11]*

to saturate. A depletion region forms as described in section 2.3 and the current gets space charge limited.

2.4.2 Characteristics of a FET

As anticipated in the previous section with the output characteristic, a transistor has very typical voltage-current dependencies like shown in figure 2.7

Transfer Characteristic

In this case one sweeps the gate voltage at a constant drain voltage. Plotting V_G against I_D one gets the typical transistor characteristic known from many textbooks. Most common parameters like the threshold voltage and the mobility can be extracted from this measurement mode, hence different plots (linear, square root, logarithmic) are used for an intuitive readout.

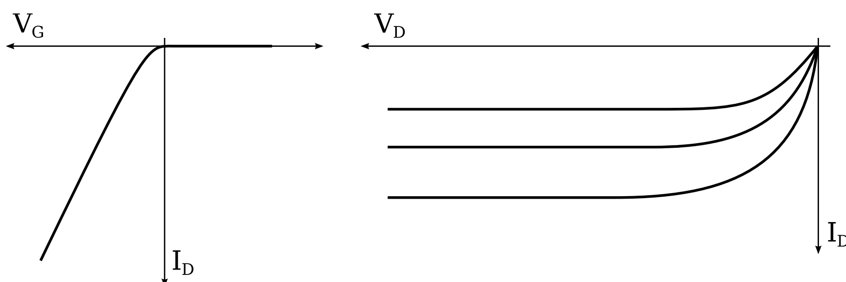


__Figure 2.7:__ Characteristics of a p-type transistor: transfer line (left) and output characteristic (right) for several gate voltages

Output characteristic

The different working regimes (see also picture 2.6) get visible in an output characteristic. The saturation behavior features bulk conductivity or makes a shortcut visible. The region around $V_D = 0$ let also conclude to the charge injection properties of the device. An injection barrier can only be overcome by applying a minimum drain voltage, which gets visible when the drain current gets very small in a symmetric region around $V_D = 0$.

A transistor is usually used for amplifiying or as a switching device in electrical circuits, logical devices and computer chips. Depending on the use and the load there are different desirable aims in engineering. Low power consumption and high frequency operation are crucial for computer processors whereas a linear transfer characteristic is desirable for amplification. The parameters of interest for our research are discussed in section 3.6.2

2.4.3 Modelling a FET

The following derivation of a simplified FET model is based on reference [12]. The goal are basic equations for the most important device parameters like drain current behavior and the threshold voltage. Since in operation one applies a gate and a source-drain voltage the interesting quantity is the resulting current. Therefore we begin with the resistance of the channel. The effective potential defines the charge transport in the channel, hence the channel conductivity σ changes along its length y and height z. Therefore the differential resistance reads as

$$dR = \frac{dy}{W \int \sigma(z, y)\, dz} \tag{2.9}$$

Now we can substitute the conductivity with the mobility as derived in section 2.1

$$\sigma(z,y) = qn(z,y)\mu \tag{2.10}$$

Assuming a homogeneous channel and a non gate bias dependent mobility we can integrate along the z-axis and get the following expression

$$\int \sigma(z,y)\,dz = Q(y)\,\mu \tag{2.11}$$

This point is crucial for the modelling of the device. The free charge carrier distribution in the channel is heavily depending on the quality and design of the FET and gets even more important for OTFTs [13] due to the usually high density of trapped charge carriers.

Free charges are present under accumulation and inversion conditions, the threshold voltage as derived in section 2.3 defines the point from which on the channel gets conducting.

In the easiest case we assume that the MIS structure acts as a capacitor. Hence, we can express the number of free charges by the effective potential at the point y.

$$Q(y) = C_{ox}(V_G - V_T - V(y)) \tag{2.12}$$

Inserting equation (2.11) and equation (2.12) into equation (2.9) and multiplying with the current in the channel yields the infinitesimal potential drop along the channel,

$$dV = I_D\,dR = \frac{I_D\,dy}{W\mu C_{ox}(V_G - V_T - V(y))} \tag{2.13}$$

which gives (after integration along the channel with the length L) the following expression for the drain current

$$I_D = \frac{W}{L}\int_0^{V_D} \mu C_{ox}(V_G - V_T - V)\,dV \tag{2.14}$$

some

In this equation, the channel width to length ratio W/L turns up, which is a very important geometric parameter for the experimental work with FETs. The next assumption we have to make is a constant non drain bias dependant mobility. Equation (2.14) then can be integrated easily and we get

$$I_D = \frac{W}{L}C_{ox}\mu(V_G - V_T - \frac{V_D}{2})V_D \tag{2.15}$$

This gets us back to section 2.4.1 and the I-V characteristics. We can distinguish between two cases:

$$V_D \ll V_G - V_T \qquad \text{and} \qquad V_D > V_G - V_T \tag{2.16}$$

In the first case the charge carrier density in the channel can be regarded as uniform and equation (2.15) simplifies to

$$I_D = \frac{W}{L} C_{ox} \mu (V_G - V_T) V_D \tag{2.17}$$

What we see is a linear dependence on the gate bias and the drain bias, which describes the current dependence in the *linear regime*.

The second case describes the regime where the current saturates with respect to the drain voltage, which can be described as

$$\begin{aligned} \frac{dI_D}{dV_D} &= \frac{W}{L} C_{ox} \mu (V_G - V_T - V_D) = 0 \\ \Rightarrow V_{D,sat} &= (V_G - V_T) \end{aligned}$$

Therefore the current dependence in the *saturation regime* reads as

$$I_D = \frac{W}{L} C_{ox} \mu (V_G - V_T)^2 \tag{2.18}$$

Equation (2.17) and (2.18) are usually the basis of the parameter extraction for the threshold voltage and the mobility from the transfer characteristic of a device [14].

Chapter 3

Organic Semiconductors

We would like now to transfer the previous chapter to organic electronics. In the following, the basic concepts of organic semiconductors will be explained, differences pointed out and new features will be discussed.

As introduced before, the charge transport in inorganic systems takes place in energy bands. There are mature models for the band theory and the transport, as well as for junctions and devices. In organics the situation is much more complicated due to the higher degree of disorder in the systems.

The covalent bonds in a molecule lower the energy barrier between the involved atoms. Therefore, new orbitals establish which extend over more atoms or even the whole molecule. Since the energy state and shape of these orbitals is defined by the molecule as a whole they are called molecular orbitals. In a molecular solid the molecules are held together only by weak van der Waals interaction, which results in a bigger potential barrier between molecules as depicted in figure 3.1.

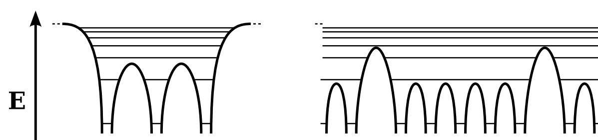


Figure 3.1: *Electronic structure of a molecular crystal: left - an isolated molecule of three atoms; right - molecular crystal*

A complication for the band theory is the usually large energygap and the lack of mobile charge carriers [15]. Small defects can change the Fermi-level significantly, so Fermi-level alignment in junctions exists only qualitatively [15]. Of course different workfunctions of the materials lead to an electric field in the junction. But due to the low number of mobile charge carriers in the organic layer, band bending is also limited to a great extend. Moreover, in thin films the assumption of a rigid band is very reasonable [15].

3.1 Material Selection

Organic Semiconductors consist of π-conjugated molecules, sp an sp_2 hybridized carbon compounds, which are coupled by weak intermolecular forces like *Van-der-Waals*, dipole or Coulomb interaction interaction. A good overview of organic semiconducters can be found in reference [16]. In general there are two classes of organic semiconductors, polymers and small molecules.

Small Molecules

Molecules typically form crystals respectively polycrystalline layers. The structure is generally determined by the intermolecular forces [9, p.26] where multiple phases for one molecule are usual. Depending on the length and shape of the molecule, sandwich and herringbone structures are most common structures.

Polymers

The crystallinity of polymers strongly depends on the deposition technique and the side chains of the polymer. There is only one singlecrystalline polymer known [9, p.35], hence polycrystalline and partially crystalline regimes in an amorphous structure are more likely.

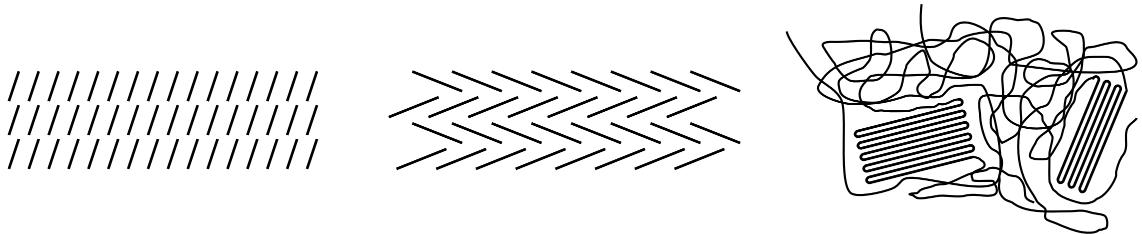


Figure 3.2: *Typical structure of organic layers: left - sandwich; middle - herringbone; right - polymer crystallization*

3.2 Charge Transport

Transport in inorganic crystalline semiconductors is band-based, hence charge carriers are delocalized and have typical residence time of only 10^{-16} s. This is about an order of magnitude lower than the typical lattice relaxation time, thus the interaction with the lattice is dominated by *electron-phonon scattering*. This manifests in a decreasing mobility with higher temperatures.

Table 3.1: Residence and polarization times (taken from reference [17, p.82])

Residence times τ_{res}	Inorganic SC	10^{-16} s
	Molecular SC	10^{-14} s
Polarization times	Electronic τ_{el}	10^{-15} s
	Molecular τ_v	10^{-14} s
	Lattice τ_l	10^{-13} s

In organic semiconductors, charge carriers have much higher residence times (see table 3.1) which results in a relaxation and a polarization of the molecule lattice. The polarization cloud travels along with the charge carrier. This combined conceptual particle, the *polaron* describes this fact and hence is the physically relevant charge carrier [17, p.81].

Traps

The concept of traps is widely used to describe material and device features, even though it is only a description for energy states with certain residence times for the charge carrier. It does not tell anything about the physical sources of these states, it is a macroscopic description for energy states from various origins, like impurities. But there are some known trap states at defined energies, like water induced traps in pentacene [18], the formation of bipolarons [19] or other ambient influences [20] [21].

3.3 Transport Models

This section is mainly based on the Andrej Golubkov's master thesis [22], another good overview can be found in reference[17].

In a fully pi-conjugated system a polaron can be regarded as delocalized. The transition to another molecule or polymer chain however is complicated by an energy barrier as illustrated in picture 3.1. Grain boundaries, disordered tacticity or impurities from the chemical synthesis also induce energy barriers or wells (traps) which disturbs the charge transport further.

There are many transport models proposed which account for these peculiarities. These models often originate from modelling amorphous silicon, where alike problems exist. In general the models can be divided into two groups

3.3.1 Extended State Transport

The main proposition of these models is that part of the charge carriers are trapped and do not contribute to the transport. The ratio of trapped to mobile charges yields an effective mobility which, due to thermally or bias activated detrapping, rises with higher temperature unlike in band-based transport. The main issue for the validity of these model is the energy distribution and density of the trap sites, hence different approaches have been made.

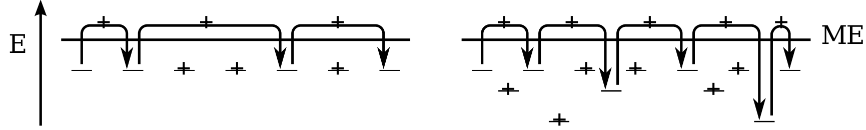


Figure 3.3: *Principle of extended state transport: the charge carrier is excited above the mobility edge, there it travels further and relaxes again into another energy state*

3.3.1.1 Mobility Edge Model

This models separate the charge carriers into trapped (e.g. at grain boundaries) and delocalized, mobile ones (e.g. inside a crystallite). An excitation of the trapped charges by thermal activation or a bias beyond a well defined energy (the mobility edge) releases it into the conducting state. Dhoot et al. [23] also included electric field induced tunneling between the trap sites, which gains in importance when working at low temperatures and high electric fields.

For the standard model the effective mobility reads as

$$\mu_{eff} = \mu_0 \frac{n_{mob}}{n_{tot}} \tag{3.1}$$

The number of mobile charges, in this case for holes can be written as

$$n_{mob}(V_G, T) = \int_{-\infty}^{E_v} D(E) f(E_f, E)\, dE \tag{3.2}$$

since the transport is limited to energies below the valence band. The density of states $D(E)$ has to be modeled for the trap density, usually as an exponential decrease, and follows the typical $\sqrt{E}$ in the conducting band. The gate voltage dependence originates from the evaluation of the Fermi energy from the transistor capacitance and the temperature enters with the Fermi-Dirac distribution. So the gate voltage populates the conducting band by pushing the Fermi energy in its direction and the

temperature smears out the Fermi-Dirac distribution, which also leads to a higher ratio of mobile charges.

The previously presented evaluation has to be done numerically and the temperature dependence of the mobility cannot be expressed explicitly, which is the big drawback of this model.

3.3.1.2 Multiple Trapping and Release (MTR) Model

To meet the demand of an analytical solution for temperature predictions the MTR model was developed by Gilles Horowitz[17, p.86-89]. The main simplification concerns the trap energy distribution.

Single Trap Energy

The separation between mobile and trapped charges follows the law

$$n_{mob} = N_c e^{-\frac{E_c - E_f}{k_B T}} \tag{3.3}$$

and

$$n_t = N_t e^{-\frac{E_t - E_f}{k_B T}} \tag{3.4}$$

with N_c the effective density of states at the bang edge with the energy E_c. N_t is the number of trap sites which is required to be high enough so they never fill up. The single trap energy E_t is assumed to be constant, which yields the following expression for the effective mobility

$$\mu = \mu_0 \frac{n_{mob}}{n_{mob} + n_t} = \mu_0 \frac{N_t}{N_c} \frac{1}{1 + e^{\frac{E_c - E_t}{k_B T}}} \approx \mu_0 \frac{N_t}{N_c} e^{-\frac{E_c - E_t}{k_B T}} \tag{3.5}$$

The lack of a gate voltage dependence can be solved by the introduction of a non-constant trap energy

Distributed Trap Energy

Assuming exponentially distributed traps

$$D(E) = \frac{N_t}{k_B T_c} e^{-\frac{E}{k_B T_c}} \tag{3.6}$$

and a Fermi-Dirac distribution approximated by a step function the effective mobility still can be solved analytically. The critical temperature T_c accounts for the step function approximation and again a much higher trap density than induced charge carriers is assumed. The effective mobility then can be calculated to

$$\mu_{eff} \propto \left(\frac{C_i(V_G - V_T)}{qN_t} \right)^{\frac{T_c}{T}-2} \tag{3.7}$$

with C_i the capacitance of the transistor,$(V_G - V_T)$ the effective gate voltage. The critical temperature and total trap density can be assumed around 450 K and $4\times10^{20}\,\text{cm}^{-3}$ [24].

3.3.2 Hopping Transport

Models including hopping transport accredit for a transport below the conduction band, for instance tunneling or polaron hopping.

3.3.2.1 Tunneling Transport

A charge with an exponentially decreasing residence probability density is able to tunnel into another trap state if an overlap of the wavefunctions at both states exist. If R is the distance to the next trap site and R_0 the delocalization radius of the state the probability of the charge carrier is described by the *Miller-Abrahams* formula [25]

$$\gamma_{ij} = \begin{cases} \gamma_0 e^{-\frac{2R}{R_0}} e^{-\frac{E_j - E_i}{k_B T}} & \text{for } E_j > E_i, \\ \gamma_0 e^{-\frac{2R}{R_0}} & \text{for } E_j > E_i \end{cases} \tag{3.8}$$

with the delocalization radius

$$R_0(E) = \sqrt{\frac{\hbar^2}{m(E - E_c)}} \tag{3.9}$$

where E_c is the conduction band edge and E the energy of the trap site. The As can be seen in equation 3.8 the tunneling probability gets temperature independent if the two trap sites are of equal energies. The temperature dependence yields also to a dominant role for tunneling charge transport at low temperatures.

3.3.2.2 Polaron Hopping

The polaron is a quasiparticle which combines a charge carrier with the polarization of its surrounding. This relaxation of the surrounding lattice lowers the binding energy of

Table 3.2: *Overview of different transport models and their predictions for the temperature dependence of the mobilities, taken from reference [17]*

Extended state transport	
Mobility edge model	$\mu_0 = f(V_G, T)$
MTR model	$\ln(\mu) \propto 1/T$
Hopping transport	
Tunneling model	$\mu \neq f(T)$ for $E_t = const$
Bässler's model	$\ln(\mu) \propto 1/T^2$; $\mu = f(\boldsymbol{E})$
Variable range hopping model	$\ln(\mu) \propto 1/T^{\frac{1}{2}}$

the polaron significantly compared to the isolated charge carrier and, therefore, allows a transport at lower energies. The dominant parameters for the charge transport is the reorganization energy and the overlap of the molecular orbitals. A detailed description of polaron hopping can be found in [17, p.80-86]

3.3.3 Temperature Dependence of the Mobility

To compare the presented and some additional transport models, the temperature dependence of the mobility is shown in table 3.2

Thus, if one is interested in the transport mechanism, the obvious experimental approach is to make temperature dependant measurements.

3.4 Junctions

For organic transistors the metal-semiconductor junction is of great interest. Charge injection and the contact resistance are a crucial factor for the device performance. Since the contacts are usually deposited by thermal evaporation the interface of the junction is poorly determined [15]. The hot metal atoms may react with the layer or diffuse into the bulk, which results rather in a three layer system with an injection barrier than a smooth transition from the metal to the semiconductor [15].

The same difficulty applies to the deposition of the organic layer on the dielectric. For example residues, activated surface atoms, or dirt from pre-treatment may manifest in a space-charge layer, poor growth of the molecules, or a high trap density.

3.5 Selected Materials

3.5.1 Polythiophene

Different derivates of polythiophene are used for organic semiconductor devices [26]. The backbone of the polymer consists of thiophenes (as depicted in figure 3.4 on the left) which leads to a fully pi-conjugated chain and, therefore, good semiconducting properties. For better solubility and crystallisation, different functional groups are added to the backbone, so regioregularity and the functional groups open up many possibilities for optimizing the polythiophene's properties. The most widely used derivate is *regioregular-poly 3 hexylthiophene (rr-P3HT)*, which is commercially available from various companies in different qualities.

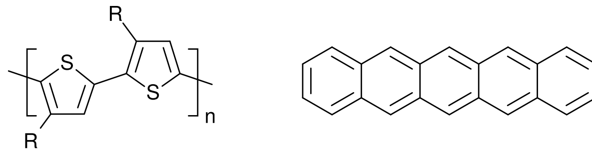


Figure 3.4: *Structure of polythiophene and pentacene*

3.5.2 Pentacene

Pentacene is a common organic semiconductor with very good properties. Achievable mobilities in the transistor geometry of up to $3\,\mathrm{cm}^2/\mathrm{Vs}$ [16] can compete with amorphous silicon and it's relatively stable in ambient conditions. The molecule consists of five linearly fused benzene rings as illustrated in figure 3.4 on the right, which results in a plane, fully pi-conjugated system. In a bulk pentacene packs in a *herringbone* structure [27]. The unit cell depends on the growth mechanism, as free grown single crystal it is *triclinic* [28] whereas in its thin film phase it is nearly *orthorhombic* [27]. Charge transport takes place in the a-b plane direction [17, p.270] from the molecular axis as depicted in picture 3.5.

3.6 Organic Thin-Film Transistors

Organic TFTs are already used in display technologies and other products, for these applications the easy fabrication over large areas, possible transparency, deposition on flexible substrates and low cost production are reasons for a further penetration of organic technologies into the mass market.

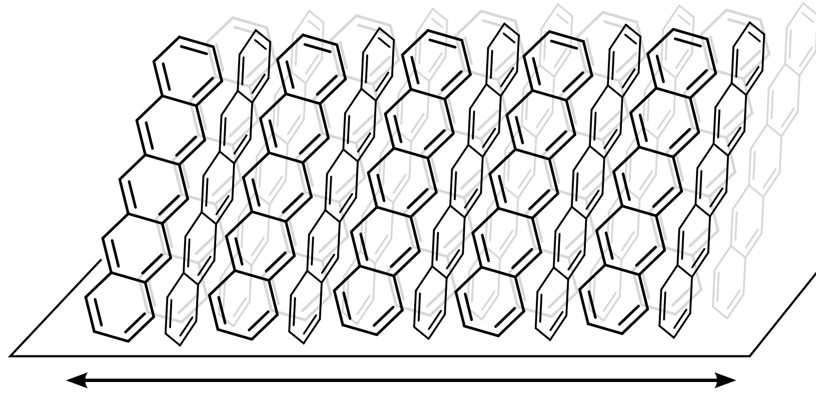


Figure 3.5: Charge transport direction in pentacene

3.6.1 Design

For laboratory use OTFTs are often built, quite ironically, on heavily doped single-crystalline silicon as substrate, since a well controlled system is favorably over low cost production. Indeed, newer projects trend to use glass or other amouphous materials as insulator. The dielectric layer is realized by a layer of thermally grown silicon oxide, self assembled monolayers, polymers or a combination of these depending on the application and intended charge carrier species.

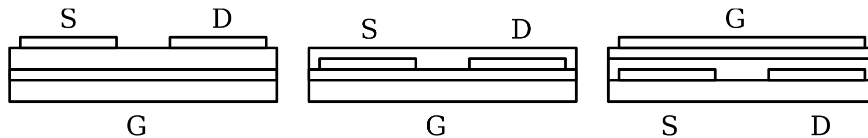


Figure 3.6: Typical OFET layouts: top contact; bottom contact; top gate

Basically n and p-type transistors are possible even with the same semiconductor, e.g. pentacene [29], if the metal contacts and especially the dielectric are tuned to the particular purpose. P-type pentacene transitors are usually built with gold contacts, which results in a workfunction difference of 0.7 to 1.0 eV [30], and, therefore, a built-in threshold voltage of 1 . The dielectric influences mostly the hysteresis and bias stress of the device, but not the basic functionality. Contrary, n-type transistors are more sensitive to the dielectric, as silicon oxide is known to trap electrons. Contact materials in n-type devices are usually metals with lower workfunctions like aluminum or calcium [29]

In order not to get too much into detail further considerations are based on a pentacene device with bottom gate, siliconoxide as dielectric and evaporated gold contacts. Analoguous considerations for other systems differ mainly in the importance

of the individual factors for the device performance and of course the charge carrier species.

3.6.2 Important Parameters

The fundamental research on organic transistors concentrates usually on a few parameters.

Threshold Voltage

Theoretically, this parameter describes the gate voltage, at which the channel gets conductive (see section 2.3). Since in practice, this onset of the conduction is not well defined the term threshold voltage is used in many, different ways. From a simple current threshold to different definitions originating from several extraction methods [31][32], which, again, often depend on the device models.

The threshold voltage as such is crucial for switching or building logical devices and, therefore, of great interest in research.

Mobility

As defined in section 2.1, the mobility is in first place a material property, even though, as effective parameter heavily depending on the extraction method. But especially for a critical evaluation of a device's or process' quality this parameter has a high significance. Some literature claims a postive dependence on the grain size of the active material[33], but others state the opposite indeed [7]. Still, its temperature dependence gives some indication of the charge transport mechanism as summarized in section 3.3.3.

Contact Resistance

The contact resistance is a parameter of great interest for high mobility OTFTs. It gains in importance since in this case it is the main contribution to the channel resistance and, therefore, the limiting factor for the performance. The contact resistance can be regarded as originating from two different parts [34]. The metal-semiconductor contact itself is dominated by the energy level alignment and the interface quality, whereas the second part considers the transfer of the charges to the conducting accumulation layer through a poorly conducting region. In top contact devices, this is the less conducting bulk between the contact and the conducting accumulation layer, which is only several layers thick [35]. In bottom contact devices one associates it with the region of poorer growth on top and at the edge of the metal contacts.

On/Off Ratio

The ability for switching is described by the ratio of the highest current to the off current. Obviously, this is not very distinctive without the notation of the drain and $\mathrm{V_G - V_T}$ voltage. Indeed, it is usually declared without the declaration of the effective gate voltage.

Subthreshold Swing

Equation 2.17 and 2.18 predict a zero drain current for $V_G \geq V_T$ (for a p-type transistor), which is not observed. In fact, the current undergoes an exponential decrease after the threshold which saturates at a certain level. So the subthreshold regime is visible in a logarithmic plot of the transfer curve and describes the steep descent after the kink in the threshold voltage region. It is related to a conduction below the threshold. In OTFTs the filling and emptying of traps is responsible for this feature [36], in a classical MOSFET, operated in strong inversion, one talks about the conduction in weak inversion. The subthreshold swing is given in volts per decade.

3.6.3 Parameter Extraction

Parameters like the threshold voltages, onset voltages and mobility are usually extracted from the device characteristics using teh equations derived in section 2.4.3. Mansouri et al.[37] developed a device model with a gate dependent mobility, in order to include and evaluate the contact resistance.

Since all parameters mutually interfere the obtained parameters are heavily dependent on the actual extraction method.

Threshold Voltage

There are multiple ways [32] to extract the threshold voltage of which two are commonly used. The first originates from equation 2.17 and 2.18 and is based on an extrapolation at its maximum first derivative (slope) point in the transfer characteristic as shown in figure 3.7.

In the linear regime, for $V_D \ll V_G - V_T$ one takes the highest gradient of the characteristic and makes a linear extrapolation to the gate voltage cross section. For $V_D > V_G - V_T$, the saturation regime one takes the square root plot of the drain current since there is a quadratic dependence on the threshold voltage.

The second method takes the second derivative of the transfer characteristic and defines the threshold voltage as the point of the highest curvature. In many cases, the second derivative of the logarithmic drain current is taken which makes the method less susceptible to noise.

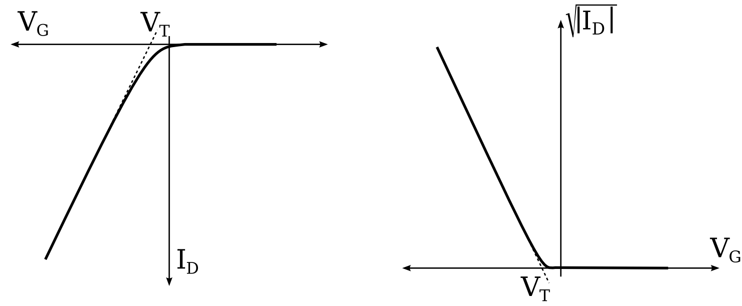


Figure 3.7: *Parameter extraction from the transfer characteristic: left - extrapolation in a linear plot for the linear regime; right - extrapolation in a square root plot in the saturation regime*

It is widely discussed if the parameter which gets extracted by the latter method actually is still the threshold voltage. Instead it is often defined as the *current onset voltage.*

Onset Voltage

As described before, the threshold voltage is defined by a theoretical model. At very low currents there are other transport mechanisms like trapping and detrapping [36], which are not taken into account by most models. Therefore, one stated the onset voltage which is derived as described before, from the highest second derivative of the transfer characteristic. So the onset voltage does not take any model into account, just the obvious point from which on the current starts to flow. Threshold and onset voltage are often mixed up and depending on the author used in a different way.

In this thesis, the threshold voltage will be extracted by linear extrapolation in the linear, respectively square root plots. The term onset volteage will be used , when referring to the maximum second derivative in the logarithmic plot.

Mobility

The slope of the linear and the square root plot in each case corresponds, according to the model from section 2.4.3, to the mobility. The extraction is made by the maximum slope of the transfer characteristic, which relativizes its significance due to the often neglected gate voltage dependence.

Contact Resistance

There are mainly three procedures for evaluating the contact resistance. The *four-point probe method* [17, p.149] uses additional contacts in the channel and extrapolates the

contact resistance from the channel resistance. Another method where the devices have to be manipulated is the *transmission-line method*. several different channel lengths are used in this method. Then one plots the channel resistance over the channel length and linearly extrapolates the resistance to zero channel length. Obviously the remaining offset states the contact resistance [17, p.148]. The third method extracts the contact resistance from the device characteristic [37], which is only possible if the threshold voltage is previously determined in a different way.

3.6.4 Deviations from Ideal Behavior

In the previous chapters it was pointed out that factors like the dielectric layer, interfaces, and junctions are crucial for the device performance, but especially in the organic system badly controllable. The next uncertainty is the active layer itself. There are several aspects, like the chemical purity of the molecules or polymers. This is usually guaranteed by the supplier to a certain level but indeed alters from badge to badge. The deposition techniques, growth rates, environment and atmosphere during deposition, storage, and characterisation play an important role.

All these uncertainty factors can have a great impact on the device themselves, and taken together give plenty of error sources for processing and characterizing. Slightest changes can have huge consequences, demanding very much care when performing experiments and especially when interpreting results.

After the previous discussion of the ideal OTFT we next consider a real transistor with typical non ideal characteristics and strong deviations from theoretical behavior. Working with OTFTs, one will necessarily come across many of these features, so it is important to know their origins and peculiarities. Many of these phenonema are often traced back to the presence of trap sites, which is still no fully microscopic explanation.

Bias Stress

OTFTs trend to change their device characteristics under operation, often reversible but also non reversible. This phenomenon is generally referred to as bias stress and usually manifests itself in a decreasing drain current and a shift of the threshold voltage towards the applied gate voltage. The magnitude of the stress effects mostly depends on the active material, the dielectric and the atmosphere. Common sources for this feature are high trap densities, which change the concentration of the mobile charge carriers and subsequently also the conductivity. Finally it was suggested, that bias stress is an intrinsic feature of organic materials due to the charge transport mechanism. The proposed reason is the formation of bi-polarons under bias stress [19].

Hysteresis

Another feature, that is often connected to high trap densities is a hysteresis. A hystesesis can be measured when double sweeps are performed. This means that the measurement process is starts from high to low voltages and back to high voltage (respectively vice versa), so one forward sweep and one backward. Still there are many publications containing only single sweeps, neglecting any hysteresis. Ambient influences like reactive gases, the dielectric, and processing of the active layer have a big impact on the magnitude of the hysteresis by creating trap states. An overview of the microscopic mechanisms taken from Egginger et al.[38] can be found in picture 3.8

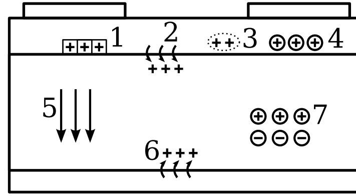


Figure 3.8: *Hysteresis mechanisms, taken from reference [38]: 1 - traps at the channel 2 - charge injection from the channel into the dielectric; 3 - slow reactions of the charge carriers in the organic layer; 4 - mobile ions in the semiconductor; 5 - polarization in the dielectric; 6 - mobile ions in the dielectric; 7 - charge injection from the gate electrode into the dielectric*

A further problem with the hysteresis is the measurement procedure and the measurement time per data point. Sweeping from a lower gate voltage to higher and back yields to different results from a measurement, that would have started the higher voltage. The extraction of the device parameters is either applied at the first measurement sweep or the second, impairing comparability further. The difference between bias stress effects and hysteresis is the timescale. Shallow, fast traps cause a hysteresis whereas bias stress is usually attributed to deep and slowly emptied traps.

Off Current

The off current is limited by the bulk conductivity, but the measurement setup and, especially, the geometry of the electrodes have also to be taken into account. A reasonable off current is in the nano or picoampere range, which makes any leakage in isolation crucial. In fast measurement sweeps emptying and filling of traps may also resemble an off current. The metal contacts are usually made by thermal evaporation through a shadow mask. It cannot be ruled out that some gold is also deposited on top of the channel, which would also provoke a shortcut similar to the constant bulk conductivity. This can be ruled out by the measurment of an output characteristic, since the current then shows ohmic behaviour.

Leakage Current

The current measured at the gate electrode is usually referred to as the leakage current, which is not entirely appropriate. Many contributions to this current come from capacitive charging currents of the gate electrode and the measurement setup. Talking about a real leakage current shorts to one of the electrodes are the usual origin, which in some cases can be checked by switching drain and source.

Linearity

The threshold voltage is usually extracted by a linear extrapolation either in the linear or the saturation regime since we assumed a non gate bias dependent mobility. But usually that is not the case, instead the mobilty varies with the gate voltage. After a increase there is usually a mobility degradation at high negative gate voltages (for a p-type transistor) [39]. The characteristic shows an upward curvature at low and a downward curvature at high gate voltages. Consequently, the threshold voltage is usually extracted at the highest slope of the transfer characteristic, which gets problematic, if the device shows a big subthreshold swing.

3.7 Threshold Voltage Tuning

In section 2.4 it was already discussed that tuning V_T is of great importance for engineering electronic circuits. Various methods to adjust the threshold voltage were developed. Bulk doping [40], treatment of the dielectric surface by UV, UV - ozone or oxygen plasma [41][42], or adding dipole or space charge interface layers [43][44]. The fundamental research of one mechanism for a $\mathrm{V_T}$ shift is the central topic of this thesis, hence we will have a closer look at the theory behind it.

We already derived the threshold voltage for the accumulation mode

$$V_T = V_{FB} + \frac{qN_a t}{C} \tag{3.10}$$

with q, the elementary charge, N_a the dopant concentration, t the semiconductor density and C the dielectric capacitance. So one possibility for shifting V_T is to alter the bulk dopant concentration N_a and therefore the Fermi-level, the other one to tune the flat-band voltage V_{FB}.

Charge transport in the channel takes place in the first few pentacene layers [39]. In an OTFT with active layer thicknesses of some ten nanometers one usually doesn't talk about a bulk, so this doping term vanishes as a first approximation [45]. Since a higher dopant concentration also influences the on/off ratio

$$\frac{I_{on}}{I_{off}} = \left(\frac{\mu}{\sigma}\right) \frac{C^2}{qN_a t^2} {V_D}^2 \tag{3.11}$$

negatively it is more favorably to modulate V_{FB}.

Of course, talking about a flat band condition is difficult for OTFTs, but in this case simple electrostatics are the basis of the following consideration of V_{FB}:

$$V_{FB} = \phi_{G-SC} + \frac{\sigma_{sp}}{C} + kd_{dip}\sigma_{dip} \tag{3.12}$$

In equation 3.12 three qualitatively different contributions to V_T turn up:

- The work function difference ϕ_{G-SC} of the gate and active layer is given by the very basic layout of the OTFT.
- The dielectric capacitance C and the space charge layer density σ_{sp} in the second term are two experimentally relatively easy accessible parameters.
- The third term $kd_{dip}\sigma_{dip}$ describes a dipole layer at the interface which is also experimentally accessible.

3.7.1 Analyzing a Threshold Voltage Shift

Experimentally it is more the other way round. It has been observed that after modifying the interface in an OTFT the threshold voltage changed. First publications ascribed the V_T shift to a dipole layer [43], others claimed a space charge layer for the shift [44]. Various experiments, simulations and calculations have been made to clarify this phenomenon, of which the most important will be explained in the following. The starting point is the definition of the threshold voltage, not to forget that it was derived with certain simplifications.

$$V_T = \phi_{G-SC} + \frac{\sigma_{sp}}{C} + kd_{dip}\sigma_{dip} + \frac{qN_a t}{C} \tag{3.13}$$

Assuming that only a space charge layer is responsible for a shift, there has to be a dependence on the capacitance of the dielectric. This can be examined by altering the dielectric thickness, since

$$C = \epsilon_0 \epsilon \frac{A}{d} \tag{3.14}$$

and therefore

$$V_T \sim d \tag{3.15}$$

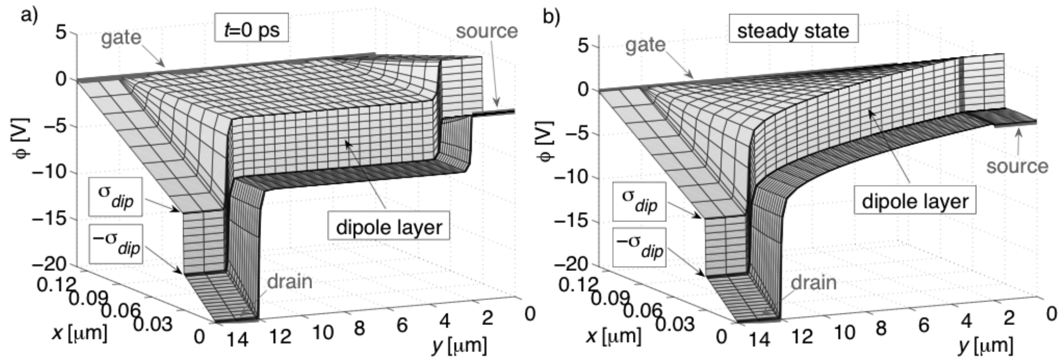


Figure 3.9: *Simulation of a interface dipole layer: the potential distribution of the device before (left) and after charge injection (steady state - right); The potential drop occurs immediatly at the interface; Picture taken from reference [46]*

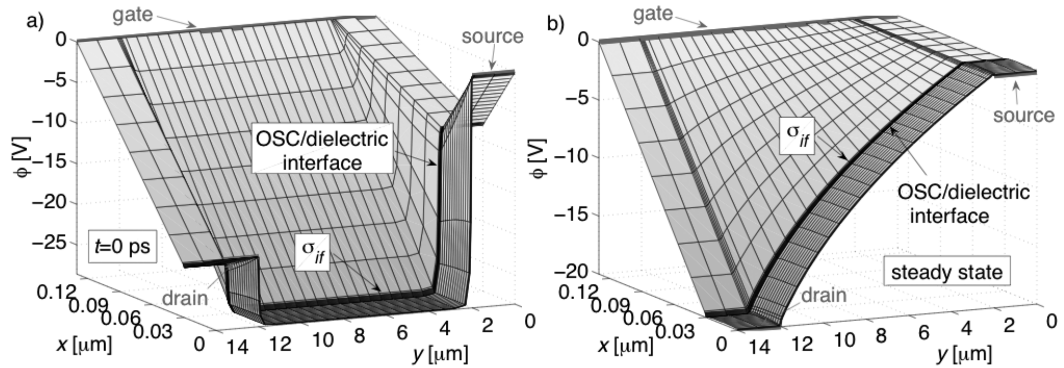


Figure 3.10: *Simulation of a interface space-charge layer: the potential distribution of the device before (left) and after charge injection (steady state - right); The potential drops linearly across the dielectric to the interface; Picture taken from reference [46]*

Thus, when the V_T shift varies with the oxide thickness and there is no change in the on/off ratio it would be a strong evidence for the V_T shift being caused by a space charge layer. If the on/off ratio collapses simultaneously, a bulk doping contribution has to be reconsidered.

Contrary, no shift as a function of the dielectric thickness would clearly indicate a dipole layer. A space charge layer lowers the potential linearly over the dielectric, while a dipole layer induces an instant potential drop at the surface.

Possanner et al.[46] performed drift diffusion simulations of these two cases for an OTFT. The difference between picture 3.10 and picture 3.9 is striking. Obviously

the prediction fo the MOSFET model also holds for an OTFT. In case of the space-charge layer the potential linearly drops along the channel whereas the dipole induces an abrupt drop at the interface.

Another possibility to distinguish between the mechanisms follows from simple estimations and calculations. We start with a V_T shift due to a space charge layer.

$$V_T = \frac{\sigma_{sp}}{C_{ox}} = \frac{ne \cdot d_{ox}}{\epsilon_0 \epsilon_{ox} A} = \frac{ned_{ox}}{A \epsilon_0 \epsilon_{ox}} \tag{3.16}$$

With the elementary charge $e = 1,602 \cdot 10^{-19}$ As, an oxide thickness of $d_{ox} = 150$ nm and the permitivitties $\epsilon_0 = 8,854 \cdot 10^{-12}$ As/Vm and $\epsilon_{ox} = 3,9$ we can estimate the number of charges per area for a 40 V shift to

$$\frac{n}{A^2} = \frac{40 \cdot 8,854 \cdot 10^{-12} \cdot 3,9}{150 \cdot 10^{-9} \cdot 1,602 \cdot 10^{-19}} \approx 0.057\,\mathrm{nm}^{-2} \tag{3.17}$$

Many interface layers consist of a SAM. The footprint of a densely packed monolayer is known to be about 25 Å^2 [46] which gives a density of about 4 molecules per square nanometer. From the previous calculation we can estimate that only about five percent of the molecules have to contribute to a spacecharge layer in order to induce a V_T shift of 40 V.

As a next step we analogously estimate the impact of a dipole layer. This is more complicated because the interaction of the dipoles lowers the effective dipole moment. This effect is accounted for by the relative permetivitty of the dipole ϵ_{dip}, which is for the most common systems in a single digit range [47]. An appropriate evaluation of ϵ_{dip} can only be made by a simulation of the continuous layer with the knowledge of the structure, hence this will settle with unfavorable assumptions.

$$V_T = \frac{d_{dip} \sigma_{dip}}{\epsilon_0 \epsilon_{dip}} = \frac{M_{dip}}{\epsilon_0 \epsilon_{dip} A} \tag{3.18}$$

A represents again the footprint of the densely packed layer with 25 Å^2 and a shift of 40 V is evaluated. For the most unfavorable result we set $\epsilon_{dip} = 1$. This assumptium is reasonable since the dipole layer's thickness is usually some nm which can be neglected compared to the 150 nm of the dielectric layer. This results in the molecular dipole of

$$M_{dip} = 40 \cdot 25 \cdot 10^{-20} \cdot 8,854 \cdot 10^{-12} = 88,54 \cdot 10^{-30}\,\mathrm{Cm} = 26.54\,\mathrm{D} \tag{3.19}$$

There are no known molecules with a dipole moment of several ten Debye which shows that for most common systems a dipole induced V_T shift of several ten volts is unlikely.

Overall in most real systems the origin of the shift is a superposition of many contributions but the proceeding analysis is a good way to investigate the main causes.

3.7.2 Acidic Interface Layers

Pacher et al. [44] found that an acidic interface layer constitutes a space charge layer by proton-transfer doping to a P3HT active layer. The layer was realized by a self-assembled monolayer consisting of molecules containing acidic components. The formation of the space charge layer happens by the steps illustrated in picture 3.11

- **Proton dissociation and migration**

  A fraction of the acidic molecules dissociate in an equilibrium with the active layer. Latest measurements indicate that this dissociation equilibrium can be shifted by external excitation like light or voltage [48], which would be consistent with the general theory of a equilibrium reaction.

- **Docking to active material**

  The protons stabilize at places with high proton affinities and react with the polythiophene

- **Mobile hole formation**

  The covalent bonded proton influences the conjugation of the pi-bonds creating a mobile hole. If this hole is extracted by a bias, only the negative charged acid residue is left, establishing a space charge layer.

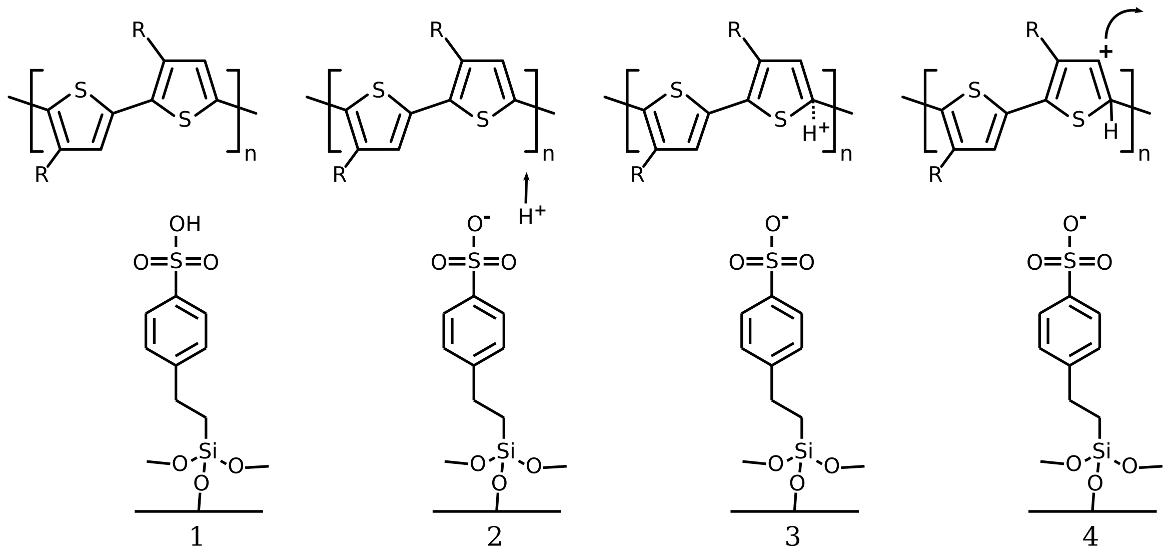


Figure 3.11: *Proton transfer doping in P3HT*

After this process, the situation in the transistor resembles the steady state in a transistor with an isolated space charge layer as depicted in figure 3.10. The crucial process is the transformation of the proton into a mobile hole which participates in the charge transport. As seen in equation 3.17 only five percent of the acid molecules actually have to form a mobile hole to induce a V_T shift of 40 V.

3.7.3 Reversing the V_T Shift by Exposure to Ammonia

Since a space charge layer can be established by an acid layer it is obvious that a base should be able to reverse that process. This effect was also shown by Pacher et al.[44] with ammonia gas for P3HT devices and used for a continuous tuning of V_T by Etschmaier et al.[49]. The process in it's latest understanding takes place as described below.

- **Diffusion through the bulk and Ionization**

  The ammonia molecules diffuse through the bulk to the channel to the dielectric interface. The proton, which induced a mobile hole binds to the ammonia molecule. Mobile holes vanish and due to subsequent charge neutrality, the space charge layer disappears continuously.

- **Acid-base reaction**

  Subsequently the ammonia reacts with the acid rest forming a NH_4OH salt, thus a part of the ammonia stays within the transistor after the exposure. During the dedoping process, the active layer theoretically should stay charge neutral since all protons for forming $NH4^+$ still origin from the acid.

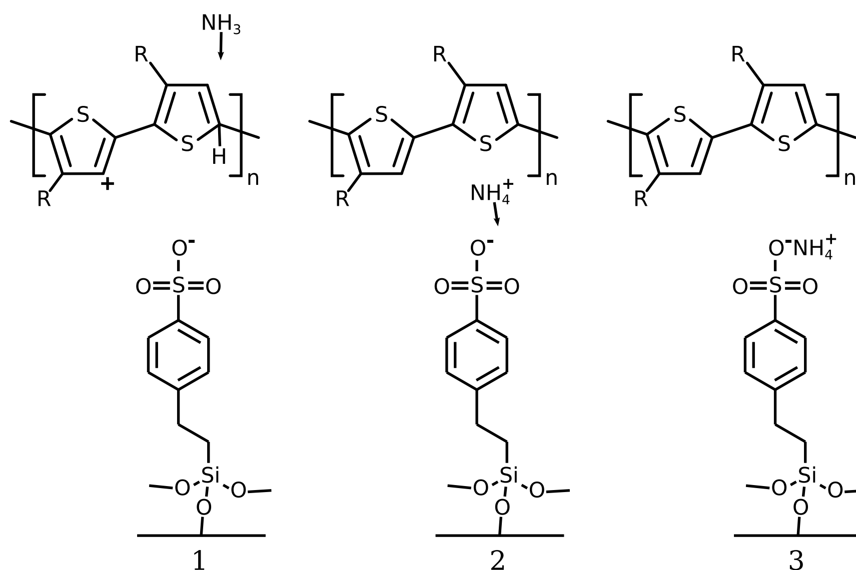


Figure 3.12: *Dedoping mechanism of ammonia*

Further research on the previously presented doping and dedoping mechanism in pentacene is presented in the experimental part of this thesis.

Chapter 4

Self Assembled Monolayers

Self assembled monolayers or *SAMs* are covalent bonded coatings consisting of well arranged and densely packed molecules. In micro and molecular electronics research, SAMs are of great interest since surface and material properties such as the work-function can be controlled. The molecules characteristically consist of three parts, as depicted in graphic 4.1.

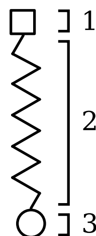


Figure 4.1: *Structure of a SAM molecule: 1 - functionalized surface group; 2 - spacer; 3 - highly reactive head group*

- **Head group**

  Also known as *docking group*, it consist of a highly reactive group, which has to be tuned to the surface (i.e. tri- or mono chlorosilanes, $SiCl_3$ and SiCl) which react exothermically with the surface atoms.

- **Spacer**

  The most common SAM molecules consist of a alkyl chain spacer of different lengths, but also benzene rings can take this function. The length and shape of the spacer affects the packing of the layer due to van der Waals interaction and has a great impact on the ideal processing temperature [50].

- **Surface group**

  This groups constitute the later surface of the coated substrate, therefore they are used for tailoring certain surface and electronic properties.

4.1 Layer Formation

This section is mainly based on reference [51] and [50]. The deposition of silane bonded SAMs is made under inert atmosphere since the molecules would aggregateand crosslink in the presence of water. Deposition is carried out either in a reaction bath like dried tolouene or by vapor deposition, but the four steps of the bonding process remain the same. The substrate has to be prepared by dry etching (see picture 5.4) or a treatment with strong acids and subsequent rinsing with water in order to get a high density (about 10^{15}/,cm^2) of hydroxyle groups on the surface. The SAM formation mechanism then involves the following steps as illustrated in picture 4.2 for trichlorosilane SAMs:

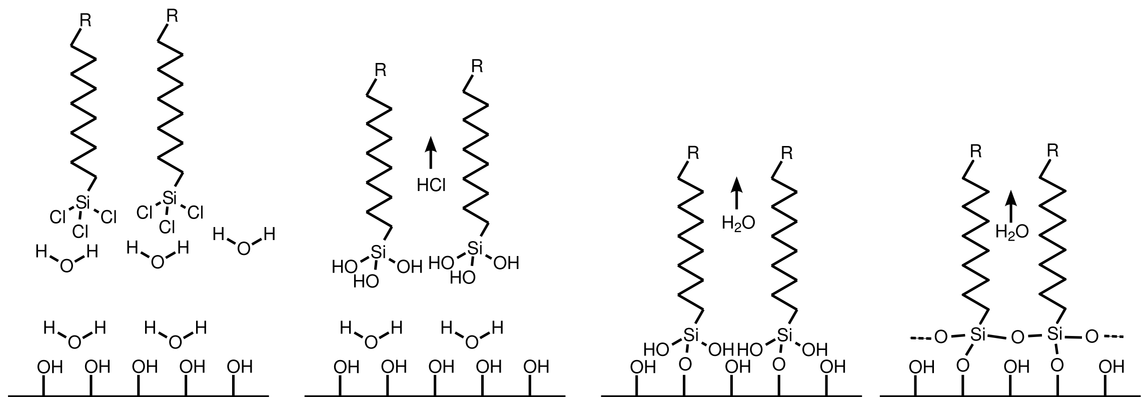


Figure 4.2: *Bonding mechanism of a SAM, picture inspired by reference [51]*

- **Physisorption**

  The substrate is dipped in the reaction bath where a layer of water adsorbs at the hydroxylated surface. The SAM molecules are added in the last moment in order to prevent unwanted agglomeration [52] or crosslinking in the solvent. The molecules physisorb at the surface, depending on the temperature and spacer group the molecules rearrange at the surface.

- **Hydrolysis**

  The chlorosilane groups react with the water building hydroxyle groups and releasing hydrochloric acid. The adsorbed water layer is crucial for the reaction so rinsing of the wafer with water or a certain rest amount in the dried toluene is important for the bonding process. Too much water, however, favors the polymerization of the molecules in the tolouene solution.

- **Covalent bonding**

  In this step, the molecules finally link to the surface, water is released as a reaction product. The molecules are covalently bond to the surface and therefore stable at ambient conditions for further processing.

- **Crosslinking**

  The hydroxyle groups of trifunctional silanes do not link only to the surface groups; instead they also crosslink to their neighbor molecules. This makes the SAM coating more stable, on the one hand, but induces disorder, on the other hand.

4.2 Formation Kinetics

The arrangement of an ordered layer shows a strong dependence on the length of the molecules and on the temperature [50]. Longer molecules need a higher temperature of the reaction bath whereas for small molecule a cooling could be necessary. The formation time is mainly dependent on the docking group and the water content.

There are two processes described as shown in figure 4.3, which lead to a densely packed monolayer. Homogenous growth at the whole surface or island growth where molecular nuclei are the origin from growth. Studies have shown that the growth mechanism strongly depends on the molecule's size [50]. It is supposed that after physisorbtion, the molecules are still able to reorganize by diffusion on the surface. The higher interaction of longer molecules would promote nucleation and therefore island growth takes place, whereas small molecules energetically do not benefit this much from dense packing and, hence, grow homogeneously.

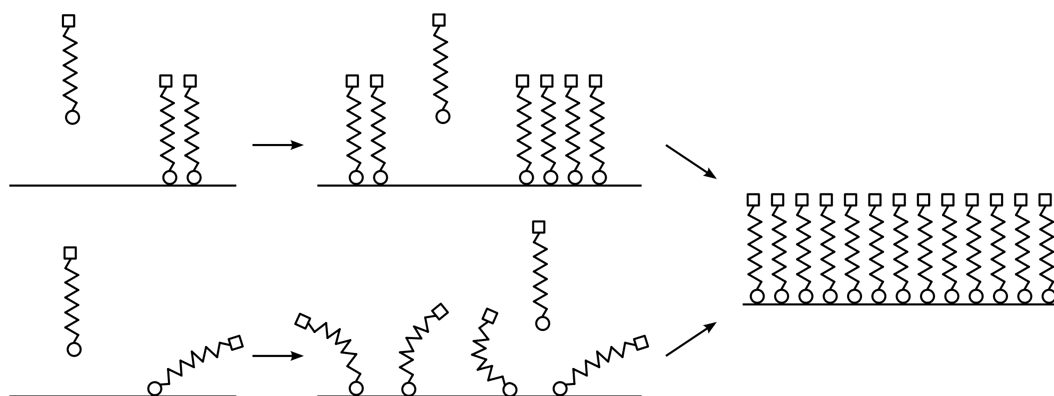


Figure 4.3: *Growth mechanisms of SAMs: island growth (top) and homogenous growth (bottom); both result in a densely packed layer*

Part II

Experimental and Discussion

Prelude

Many experimental problems occurred during this thesis. For the previous work by Peter Pacher, Harald Etschmaier and Simon Außerlechner with acidic SAM interfaces polythiophene was used as active layer. The initial idea was to continue this work with P3HT, but due to changes in the quality by the supplier (Plextronics) no properly working P3HT OTFTs could be produced anymore. After long experiments to get this system back to work we switched to evaporated pentacene, which was deposited at the Institute of Surface Technology and Photonics in Weiz. First, we obtained two badges of high quality pentacene FETs which changed, to devices with high trap densities and sensitivity to ambient conditions, which was not observed before. Paired with a broken down oxygen sensor in the glove box and the breakdown of two regeneration tubes, this resulted in problems regarding the reproducibility. Additionally, repeated breakdowns of the XRR machine stalled the development of the interface layers. At the end of this thesis it turned out, that the supplier of the P3HT sold us a non working derivate, and the evaporation process of the pentacene had been changed by our partners without notice.

Chapter 5

Experimental Methods

5.1 Atomic Force Microscopy

This very common surface analysis method gives indication of the surface structure of a sample at the scale of nanometers. A sample is scanned by a cantilever with a tip probe and the deflection of the lever due to interaction with the surface is measured. In *constant mode* the lever is directly deflected by the surface, whereas in *dynamic* mode the lever oscillates and harmonics induced by the surface indicates the height. The measurement of the deflection is realized by an optical probe or a capacitor.

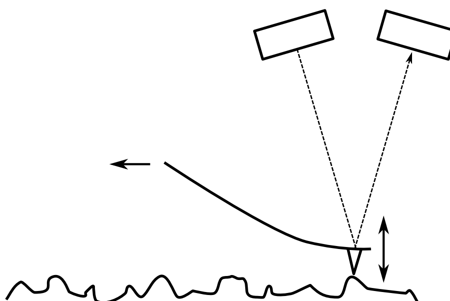


Figure 5.1: *AFM working principle: a metal tip gets dragged over a surface, the cantilever deflection is measured by an optical probe*

5.2 X-Ray Reflectivity

For the determination of layer thicknesses, *x-ray reflectivity* measurements were performed by Heinz Georg Flesch, Alfred Neuhold, Jiří Novák and Markus Neuschitzer. This technique is perfectly suited for the evaluation of very thin layers in the nm range, providing also multilayer and roughness information. The XRR scan is performed in

a $\theta - 2\theta$ mode at very low angles. Hence the x-ray source and the detector have to be moved synchronously keeping incidence and scattering angle the same.

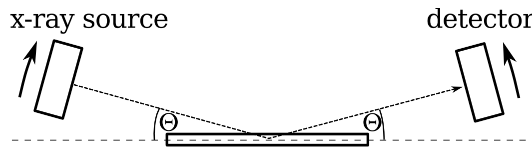


Figure 5.2: *XRR working principle: the x-ray source and the detector move synchronously at low angles*

In the typical XRR diffractogram in picture 5.2, one can see the total reflection at the surface at very small angles. Once this point is passed the x-ray beam partly penetrates the layer, getting scattered at the next interface. Again, part of the beam is reflected, leaving the sample and interferes, the other part penetrates further into the sample, again partly reflected and scattered. In the end one detects the interference of all the back scattered beams as. The frequency and the modulation depths carry the information of the layer's thicknesses and interfaces.

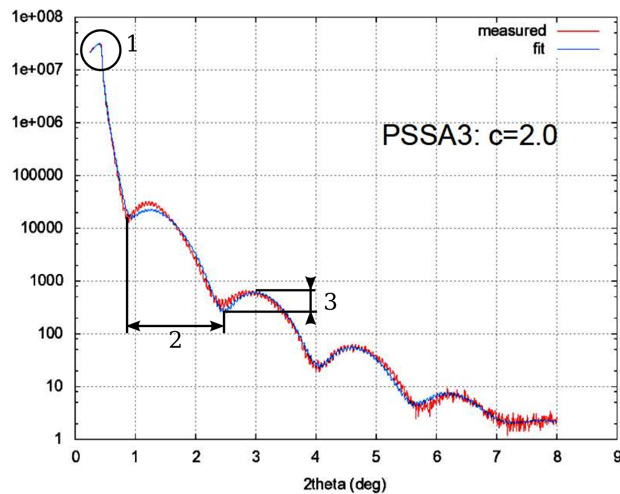


Figure 5.3: *Typical XRR spectrum: 1 - critical angle for total reflection; 2 - slow oscillations correspond to a thin layer; 3 - the amplitude of the oscillations is influenced by the electron density, hence properties like surface or interface roughness are accessible (measurement by Jiří Novák)*

Physical quantities, which are accessible by XRR measurements, are [53]:

- **Thickness**

  The frequency of the oscillations lets conclude to the thickness of the layers as the thicker the layer, the higher the frequency.

- **Roughness**

  A high surface roughness manifests itself in less accentuated or even disappearing oscillations at higher angles. Contrary, a small electron density difference between the investigated layer and the surrounding air results in a lower modulation depth at small angles.

- **Interface roughness**

  If the layer is simulated by a two or more layer system the interface roughness can also be determined. A high interface roughness manifests itself in less accentuated oscillations for higher angles then for the surface roughness but with a faster drop of intensity and, therefore, a typical kink.

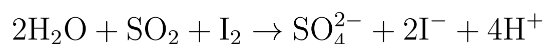
- **Electron density**

  A high absolute electron density influences the oscillation amplitudes positively as they get smaller for low densities. As already mentioned a small electron contrast gets visible in less intense oscillation features at small angles.

Since all these effects interfere, the evaluation of a XRR spectra requires a sophisticated simulation in which a set of parameters has to be optimized to fit the experimental data. As the measurements, the evalutions were also made by Heinz Georg Flesch, Alfred Neuhold, Jiří Novák and Markus Neuschitzer. The measurements for this thesis were performed on a *Bruker D8 Discover* diffractometer or at the HASYLAB.

5.3 Karl-Fischer Titration

The Karl-Fischer setup is an electrochemical analysis method for measuring the water content of solids, liquids and vapor down to the ppm range. It is based on a solution of sulfur dioxide and iodine which reacts in the presence of water.



$$2H_2O + SO_2 + I_2 \rightarrow SO_4^{2-} + 2I^- + 4H^+$$

This reaction stops when all the water of the sample is exhausted. Measured by coulometry, the result is the water amount of the whole sample. Thus, either knowing the volume or the weight, the result is in mg/ml or mg/g. Since the buffer solution exhausts during the measurement and due to leakage it has to be refreshed after some time, usually after about a month.

5.4 Plasma Etching

This process is usually used for surface cleaning and modifying. The etching process is performed in a vacuum chamber in the low mbar range. In this chamber an etching

gas (usually oxygen) gets ionized by an oscillating electric field and creates a highly reactive ambient. This plasma uniformly skims a few atomic layers of the surface of the samples and activates the surface, hence changing the hydrophilicity of the surface.

Plasma etching is one possible pretreatment for the deposition of SAMs onto siliconoxide surfaces [51]. In this case the etching process exposes dangling oxygen bonds which react with water to a hydroxyle group. This hydroxylation is crucial for the binding process of the SAM molecules (see section 4).

5.5 Spin-Coating

A widely used method for casting thin layers from solution is spin coating. Polymer or small molecule solutions are dispersed by rotation of the substrate and subsequently dried, often resulting in very smooth layers. The quality and thickness of the layers depend on a variety of process parameters.

There are semi-empirical models for the thickness-dependence of the spin coating process [54], usually regarding the rotation speed, concentration of the solution, and other parameters like the molecular wheight. The difficulty of a generally valid comprehensive model lies in the complexity of the whole system. From the material point of view, vapor pressure of the solvent, the molecular weight of the molecules and the substrate-solvent interaction have a great impact. In general the coating process can be devided in three parts as depicted in figure 5.4.

- **Deposition**

  A defined amount of solution is dropped onto the substrate. The time between deposition and the start of spinning affects the result since the molecules get some time for reorganization. Heating the substrate is another parameter for optimizing this process step.

- **Dispersion**

  The acceleration of the substrate disperses the solution and removes the redundant amount. In this process the acceleration and final rotation speed, the viscosity of the solution and shear thinning or thickening effects due to the dilluted molecules play the most important role.

- **Drying**

  After the dispersion of the solution the layer is dried upon rotation. The vapor pressure of the solvent and the rotation speed affect the reorganization of the molecules and hence the structure. Annealing after the spin coating process also influences the crystallinity of the layer.

As a rough rule of thumb, the layer thickness is linearly proportional to the concentration and inversly proportional to the rotation speed.

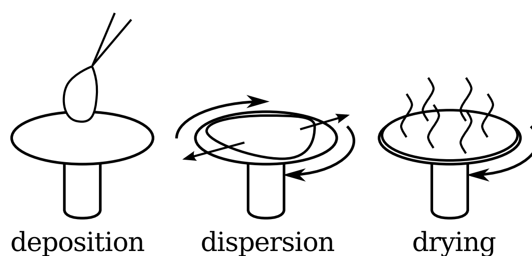


Figure 5.4: *spin coating process*

5.6 Thermal Evaporation

Thin films of metal are commonly made by thermal evaporation under high vacuum conditions. The metal is melted in a boat of tungsten or another material with a high melting point till the metal evaporates and leaves the boat more or less in a beam. Heating is usually realized by running high currents through the boat. For a mean free path in the size of the vacuum chamber a pressure about 10^{-6} mbar is needed. The cold vacuum chamber adsorbs any hot metal particles and scattering due to the long main free path can be neglected, hence all particles of the beam reach the substrate at a more or less straight trajectory from the boat. This makes thermal evaporation very well suited for the use of shadow masks to structure the film.

Pentacene is also thermally evaporated in vacuum at the Insitute of Surface Technology and Photonics in Weiz in two different evaporation systems. The evaporation process is more complicated since the crystallisation on the substrate is crucial for the later device performance. Therefore pentacene is evaporated very slowly and in steps of different evaporation rates. For a higher crystallinity of the bottom layer the substrate is heated, which was in Weiz only available in one evaporation chamber. The whole evaporation setup of our laboratory is illustrated in figure 5.5.

Thickness Control

Control of the thickness is realized by a quartz microbalance in the vacuum chamber which gets coated along with the sample. A quartz crystal has a typical resonance frequency which gets shifted if mass is added the quartz. As a first approximation the shift of the resonance frequency is given by

$$\frac{\Delta f}{f} = \frac{\Delta m}{m}$$

With the knowledge of the density of the evaporated material one can directly evaluate the layer thickness. In our case excitation of the oszillator and the evaluation is done

by one instrument, which displays the thickness of teh deposited layer after specifying the density. Slight deviations which originate from the different position of the crystal oscillator and the samples were evaluated by XRR measurements of the layer and regarded in the later process.

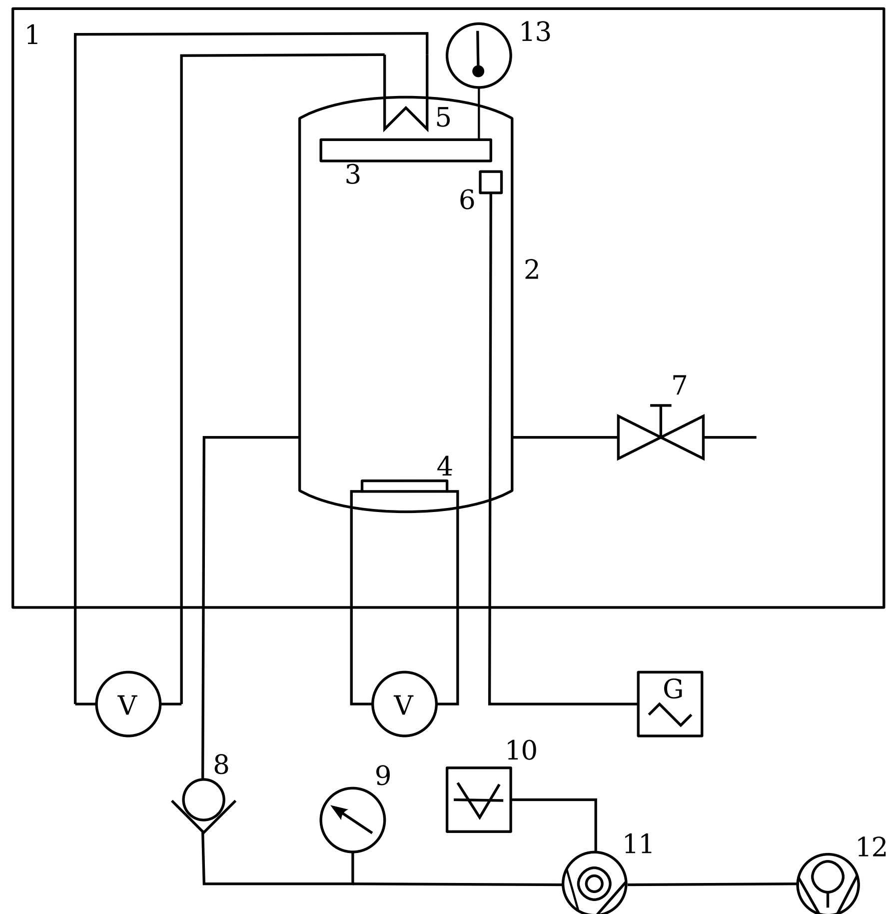


Figure 5.5: *Schematics of the evaporation system: 1 - inert ambient in argon glove box; 2 - vacuum chamber; 3 - mount for substrate holder and shadow mask; 4 - tungsten boat; 5 - substrate heating; 6 - quartz microbalance; 7 - vent valve; 8 - back pressure valve; 9 - pressure indication; 10 - turbo pump control; 11 - turbo pump; 12 - rotary vane pump*

Vacuum Generation

To achieve the low pressure needed for thermal evaporation a rotary vane pump generates a prevacuum in the 10^{-4} mbar range. From this point on a turbomolecular pump evacuates the chamber to the low 10^{-6} mbar range, depending on pumping time and leakproofness of the vacuum chamber.

Vacuum Measurement

The measurement head of the pressure measurement is situated after the back pressure valve outside the glove box, therefore, the measured pressure is lower than the the actual pressure in the vacuum chamber. Two different measurement principles for two pressure ranges are used. Down to 10^{-3} mbar a Pirani gauge is used, which measures the change of resistivity of a heated filament due to a reduced heat transfer at a lower pressure. Below that range a Penning gauge is applied. It measures the ionization current between a cathode and an anode.

5.7 Glove Box

Especially oxygen and water in the ambient air have a high impact on many solvents, chemicals and materials. Therefore, measurements and preparation typically have to be performed in inert atmosphere. For this purpose two glove boxes, filled with argon gas were used. One is used for wet preparation with solvents and chemicals and another for device characterization, thermal evaporation, and storage of devices.

The preparation glove box is suited with a moisture and oxygen content probe. Water and Oxygen amount were typically lower than 1 ppm.

The measurement glovebox was equipped with a catalytic oxygen probe, which has a high cross-sensitivity for hydrocarbons since they split at the high working temperatures of the probe. Therefore the oxygen amount was not under control all time. Occasionally a plausibility check was made by an opened light bulb, whose lifetime correlates to the oxygen amount in the box. A breakdown of the regeneration circuit caused a massive oxygen and water inbrake, which affected all the devices which were stored in the box.

5.8 Measurement Setup

The characterization of the devices is performed via a computer controlled two channel voltage source, which simultainously measures the current of each channel. The measurement setup consists of three parts, the computer, the sourcemeter and a sample holder as depicted in figure 5.6 (here together with the ammonia exposure setup).

Software Package

The sourcemeter can be programmed via the front panel, but for a better controllable interface it is controlled via ethernet by a labview program on an extern computer. The software, which has been written by Thomas Obermüller during his master thesis

offered many possibilities for device characterization. Measurements are possible in three modes:

- **Transfer characteristics**

  In order to evaluate the most important device parameters transfer lines were used. Single sweeps (only one measurent run, e.g. from high to small voltage) for faster evaluation or minimization of stress effects or double sweeps (two measurment runs, e.g. from high to small, and back to high voltage) which account for the hysterisis can be measured. The program allows to adjust the gate voltage boundaries, step size and step time, multiple curves for different drain voltages and also pulsed measurements for a reduced stressing of the device.

- **Output characteristics**

  The same interface as for the transfer characteristic allows to sweep the drain voltage with multiple constant gate voltages.

- **Time evolution**

  In this mode, a constant drain and gate voltage is applied and the corresponding currents are measured over a certain period with no restrictions in time. Usual applications were the evaluation of bias stress or during exposure external infulences. An additional possibility in this mode is to measure single sweep transfer curves in certain time steps.

Keithley Sourcemeter

The *Keithley 2636* sourcemeter is a two channel high precision voltage, respectively, current source and measurement device. Currents can be measured down to the femtoampere range whereas a maximum voltage of 200 V can be applied. It is connected via ethernet to the computer and triax cables to the contacting instrument. The sourcemeter measures small currents by the integration over a longer period. For this reason, it can happen that the device internally overrules the measurement step size given by the measurement routine. Another feature that may provoke outlier artifacts is the sourcemeter's internal switch of the measurement range.

Contacting Instruments

Since the devices were kept under inert conditions also the measurements have been performed in the glovebox. There were two possibilities for contacting. Either with three probe tips, which are adjusted manually for each device on a stage or with a measurement cell, which was actually developed for the measurements in which the devices were exposed to ammonia. One advantage of the cell is that three substrates and, therefore, 12 devices can be contacted at a time. After that the contacting is not sensible to vibrations or other influences. The possibility of measurements in

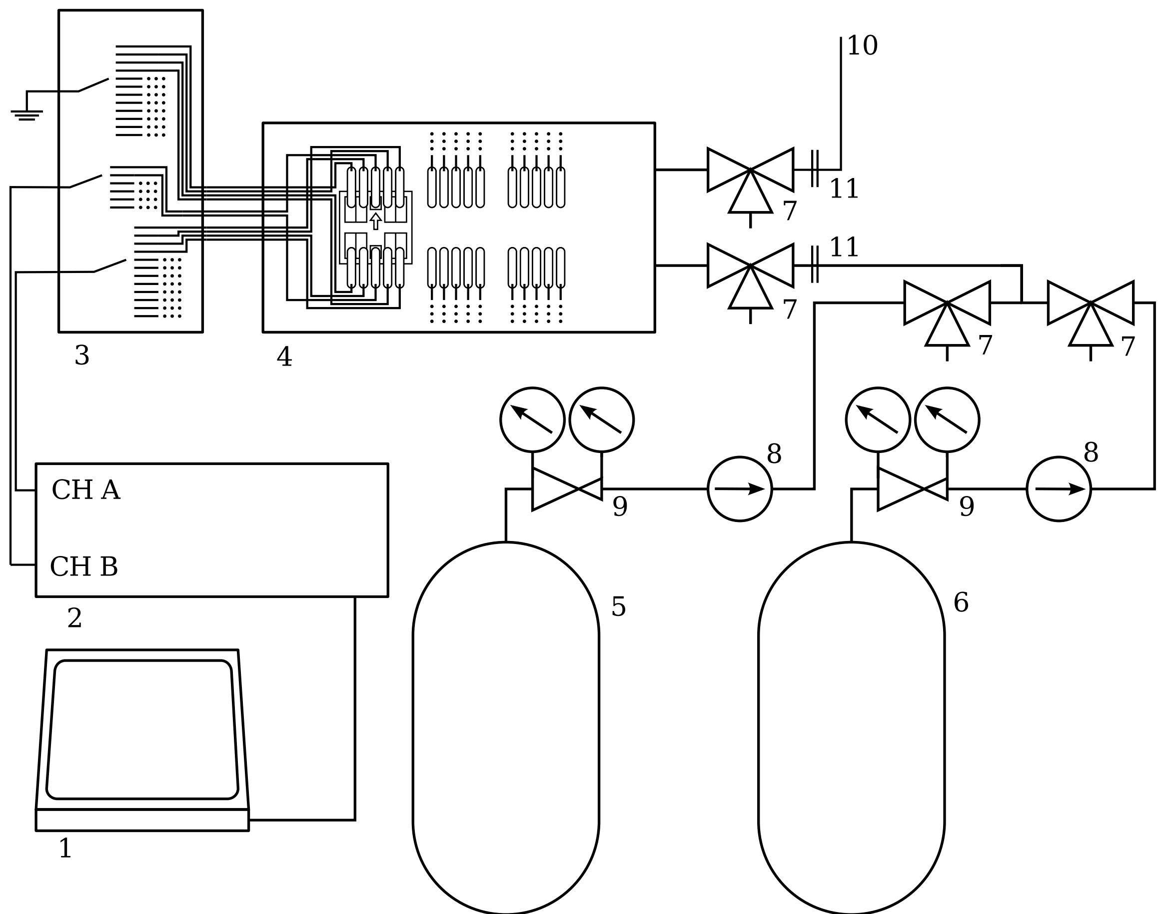


Figure 5.6: *Schematics of the measurement setup: 1 - computer with labview and measurement software; 2 - Keithley sourcemeter; 3 - switching box; 4 - measurement cell; 5 - argon gas bottle; 6 - ammonia gas bottle; 7 - 3-way valve; 8 - flowmeter; 9 - pressure reducing valve; 10 - exhaust to the rooftop; 11 - connection flange*

vacuum, overpressure, darkness, exposure to gas or a well defined light source, make the measurement cell a versatile tool for many fields of interest. The only drawback is a higher off-current compared to the probes. The reasons for that are a longer signal path, much more soldering joints and the braids of the multicore cable are not shielded separatly. In picture 5.6 one can see the layout of the cell, as well as the switching box which gates the three channels of the sourcemeter between the 28 contacts (three substrates with each four devices and two common gate contacts) of the devices.

Setup for the Exposure to Ammonia

For shifting back the threshold voltage as described in section 3.7.3, ammonia gas was used. Pure ammonia from a Linde gas bottle, if neccessary diluted with argon gas, was purged through the measurement cell for a certain time. The ammonia and the argon flow were controlled by the needle valves of two Krohne DK 800 rotary flowmeters. The different flow ranges of 10 to 100 l/h for the argon and 1 to 10 l/h of the ammonia allows a dilution from 1:1 to 1:100 of the ammonia gas, assuming the mass flow is proportional to the mixing ratio. All measurements were performed in a fumehood due to the toxicity of ammonia.

Chapter 6

Sample Preparation

6.1 Substrate

All devices produced for this work were based on heavily phosphorous doped silicon wafers with a thermally grown oxide layer of about 150 nm. The actual layer thickness was occasionally measured and always between 147 and 151 nm, which has no considerable impact on further evaluation. The substrates were provided by *Sigert Consulting* and precutted into 2×2 cm squares. Before any processing, all substrates were pretreated as follows

- The substrates were unloaded from the storage container inside a flow box, preventing any electrostatical charging by grounding oneself.
- The surface was blown off with CO_2.
- Further cleaning and surface activation by plasma etching for 30 s at maximum power at an oxygenflow of $8\,\mathrm{ls}^{-1}$.
- Again surface cleaning with a CO_2 gas stream.
- Transfer into flasks filled with deionized water with a specific resistance of $16\,\mathrm{M\Omega/cm}$.
- 2 minutes ultrasonic bath without heating.
- Unloading and rinsing with deionized water.
- Drying with the CO_2 spray.
- Transfer into a petri dish.

This pretreatment yields to a highly hydrophilic surface and was always made within about 5 minutes before further processing.

6.2 Organic Semiconductor

In our top contact devices the active layer is applied the second last before the evaporation of the gold contacts.

6.2.1 Polythiophene Layer

Two polythiophene bagdes, one provided by *Plextronics*, the other one by *Sigma Aldrich* was dissolved in chloroform at a concentration of 2 mg/ml. Then the solution was cast by spincoating under inert conditions in the preparation glove box at 1500 rpm for 40 seconds. After spin coating, the substrates are baked out at 100 °C for 5 minutes. All polythiophene devices were always stored under inert conditions but were exposed to light.

6.2.2 Pentacene Layer

The deposition of pentacene was made at the the Institute of Surface Technology and Photonics in Weiz by Anja Haase and Alexander Fian. To that aim, the freshly prepared substrates were stored under inert condition in a box and transported to Weiz. The application of the pentacene film was usually made the same day or the following day in the morning. Afterwards the substrates were transferred back, again under inert conditions.

The evaporation process was made in high-vacuum in the range of 10^{-6} mbar in two steps. A surface layer of 5 nm at a rate of 0.02 Å/s and at 0.1 Å/s for the following 30 nm. For the first two badges, made by Anja Haase, the substrates were heated. For the subsequent badges, made by Alexander Fian, the substrate heating was not used, which had an impact on the device performance.

The resulting pentace film was occasionally measured by atomic force microscopy. Picture 6.1 shows pentacene grown on substrates with different SAM layers as shown in picture 6.2. The smoother surface of the SAM monolayer obviously induces a much better crystal growth and grain size as the very rough surface of the thicker layer (the layers will be discussed in section 6.4.1) on the right side of the picture.

6.3 Electrodes

Source and drain contacts were made by thermal evaporation of gold and structured by a shadow mask. The copper mask is structured by photolitography, the channel is realized by a 25 micron tungsten wire which is tensioned over the mask and fixed with superglue. The geometry of the shadow mask for one substrate is shown in picture 6.3. On each substrate there are four OTFT devices with 25 μm channel length, 7 mm width

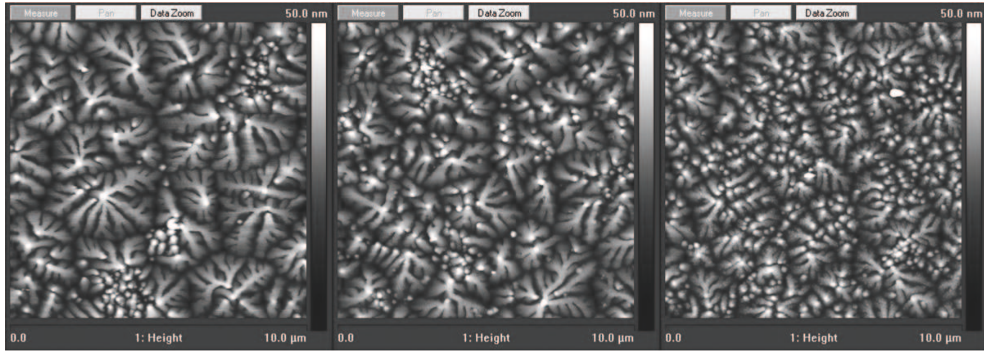


Figure 6.1: *AFM picture of pentacene layers grown on the SAM layers as depicted in picture 6.2 (Pictures made by Anja Haase)*

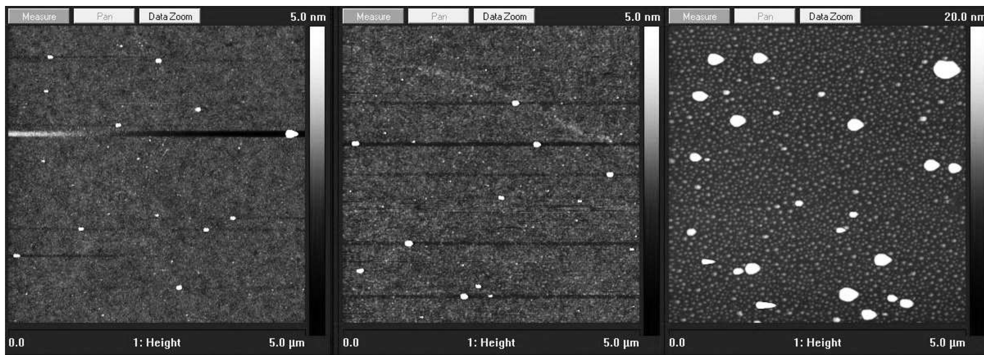


Figure 6.2: *AFM picture of three SAM layers: left - 30 min in dried toluene; middle - 16 h in dried toluene; right - 16 h in toluene (Pictures made by Anja Haase)*

and a common gate. Note that the channel is 3 orders of magnitude longer and 6 orders wider than the thickness of the active layer. The two contacts in the middle can be used for contacting the gate, provided the dielectric layer was scratched below the pad with a diamond cutter before evaporation. Top contacted gate electrodes were mostly used for the measurement cell. With the probe tips the gate was usually contaced from the bottom by a carbon tape, since for top contacting, the proximity of the gat contact to source and drain may involve leakage currents.

The gold is evaporated from a tungsten boat at a pressure in the low 10^{-6} mbar range measured next to the turbomolecular pump as described in section 5.6 in a few seconds to a contact thickness of 50 nm. The target is a mount for four to six substrates which is situated about 15 cm over the tungsten boat. After evaporation, the vacuum chamber cools down for 10 minutes and the finished devices can be extracted.

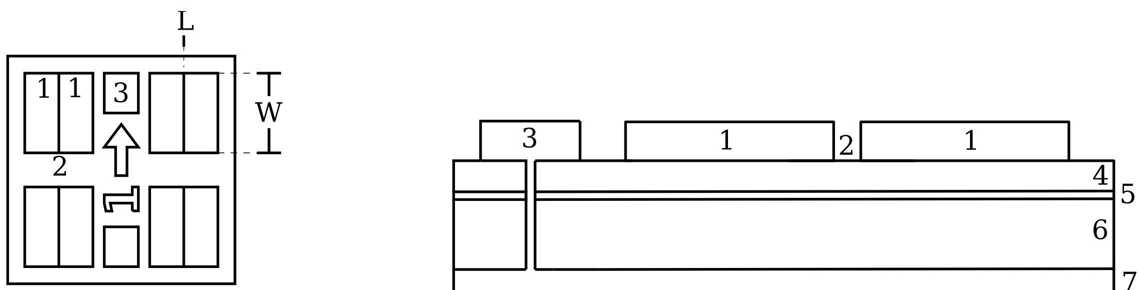


Figure 6.3: Shadowmask and device setup: left - shadow mask layout for four TFT devices (clockwise from top left: 1L, 1R, 2R, 2L), 2 gate contacts and markers; right - schematic structure of one device; 1 - 50nm gold source resp. drain pads; 2 - channel, 3 - 50nm gold top gate contacts; 4 - 35nm active layer; 5 - 1 to 10nm acidic interface layer; 6 - 150nm siliconoxide; 7 - highly p-doped silicon common gate

6.4 Interface Modification

The aim of this thesis was to control the threshold voltage by the interface layer thickness. Therefore, all devices were equipped with a layer right after the pretreatment of the substrate. Only the reference devices skipped this procedure, which is not entirely justifiable. The dielectric interface has a great impact on the device performance, especially the hysteresis. Thus, it would have been better to use the same polymers or SAM molecules without acidic groups, an inert derivate, as interface for the reference devices. Due to the lack of these materials and the risk of introducing some uncertainty, plain substrates were used.

6.4.1 SAMs

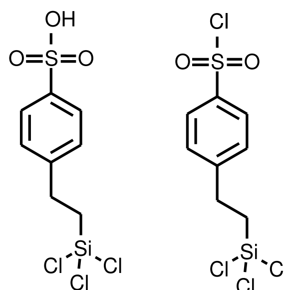


Figure 6.4: SAM molecules used for this work: left - 4-(2-(trichlorosilyl)ethyl)benzenesulfonic acid; right - 4-(2-(trichlorosilyl)ethyl)benzene-1-sulfonyl chloride

Actually a SAM is a defined as a monolayer and therefore the layer thickness is defined by the molecule length and the alignment. In this case we tried to get thicker layers than the monolyer, hence we are talking about mono, and multilayers.

A blend of trichlorosilanes as shown in figure 6.4 consisting of 4-(2-(trichlorosilyl)ethyl)benzene-1-sulfonyl chloride (70 %), shortened TS-C and the acidic 4-(2-(trichlorosilyl)ethyl)benzenesulfonic acid, T-SA (30 %) in a 50 wt% solution in toluene provided by *Sigma Aldrich* was used for growing the layers. The length of the molecules was calculated to 9.6 Å[], hence the monolayer thickness should be around this value. All flasks which were used for the reaction bath and the storage bath were extensively cleaned with Hellmanex in an ultrasonic bath two times and subsequently rinsed with distilled water twice. After this treatment they were stored in a dry oven at 80 °C for at least 24 hours.

The basic processing steps were the following:

- The pretreated substrate and two baked out flasks are transferred into the preparation glove box.
- One flask, the reaction bath, is filled with 10 ml toluene of a defined water content. The other flask is filled with 6 ml of toluene with a water content of about 28 ppm for the curing bath.
- The substrate is deposited in the reaction bath.
- 10 μl of the T-SC/T-SA solution is added to the reaction bath.
- After a defined reaction time the substrate is transferred into the curing bath, where the SAM growth stops.
- The flask is transferred out of the box and opened under the fumehood, since the reaction has stopped and the surface is not sensitive to water any more.
- The substrates are rinsed extensively with toluene and dried with the CO_2 spray.
- Transfer into a vacuum chamber (about 0.6 mbar) where the substrate is annealed for 30 minutes at 100 °C
- After cooling down to ambient temperature the chamber is flooded with argon and the SAM coated devices are ready for further use.

Thickness variation

In order to achieve different layer thicknesses three different approaches were tried, inspired by growth mechanisms described in literature [51] [50].

- **Growth temperature**

  A rather unsuccessfull attempt was to change the temperature of the reaction bath during the growth time. To realize that, the flasks were sealed, transferred out of the box and into a refrisgerator held at constant 6 °C for 16 hours.

- **Growth time**

  The formation time in the reaction bath was altered, from half an hour to 16 hours.

- **Water content**

  Since the growth mechanism is water moderated [50] the third and most promising approach was to vary the water content in the reaction bath. Toluene is a hydrophilic solvent and we usually worked with dried toluene. A first try was to use toluene which was in contact with air and therefore had a higher water concentration.

Simon Außerlechner already experimented with SAMs of different thickness. His approach was to add water saturated toluene to dried toluene, which did not lead to reprod

The layers were characterized by atomic force microscopy by Anja Haase at the NMP Weiz and x-ray reflectivity by Heinz-Georg Flesch. For the XRR evaluation the layers had to be modeled as a two layer system with differenent electron densities, which seems reasonable for the benzene head and the less dense docking and spacer group. The AFM pictures are shown in picture 6.2 and the results of the XRR evaluation in table 6.1. All the substrates which were used for this thesis were named with *L* and a continuous number.

Table 6.1: *t1, t2 - thickness of the two layers; r1, r2 - roughness of the layers; t - total thickness*
XRR results of first SAM badge: L1, L2 - 16 hours in dry toluene; L3, L4 - 30 minutes in dry toluene; L6 - 16 hours in toluene; L7, L8 - 16 hours in dry toluene, cooled

Sample	t1 / nm	r1 / nm	t2 / nm	r2 / nm	t / nm
L1	0.7	0.35	0.6	0.3	1.3
L2	0.7	0.45	0.75	0.35	1.45
L3	0.7	0.4	0.5	0.3	1.2
L4	0.7	0.2	0.5	0.33	1.2
L6	0.7	0.45	5.4	1.6	6.1
L7	0.7	0.43	0.8	0.68	1.5
L8	0.7	0.48	0.95	0.8	1.65

As can be seen the best result for a monolayer was achieved in a short time with dried toluene, the layer thickness of 1.2 nm is close to the calculated molecule length of 0.96 nm [44]. The water content had a strong impact on the layer thickness, therefore, for a second series it was decided to vary it by changing the water content in the reaction bath. In order to get a controlled amount of water in the solvent, the toluene

was first characterized. Therefore, the dried toluene and standard toluene from Sigma-Aldrich were measured by *Karl-Fischer titration*. To quantify the influence of time, samples of freshly unloaded toluene and samples from toluene which was already in use for a month, were compard. Water saturated toluene was prepared by adding a large amount of water, mixing and then extracting the toluene, which seperates from the water with a syringe. A possible influence of the flasks or the wafers on the water content was ruled out by additional measurements (results see table 6.2).

Table 6.2: *Karl-Fischer titration results in μg/g: m1 to m3 - measurements; 1 - dried toluene fresh; 2 - dried toluene old, 3 - Sigma-Aldrich toluene fresh; 4 - Sigma-Aldrich toluene old; 5 - water saturated toluene; 6 - dried toluene in dried flask, 7 - dried toluene in dried flask with wafer*

Sample	m1	m2	m3
1	5.8	5.6	7.8
2	7.9	6.2	7.6
3	24.6	30.1	-
4	27.9	29.1	-
5	463.7	487.5	-
6	5.2	-	-
7	7.1	-	-

Obviously neither aging nor the water, introduced or absorbed by the flask and the wafer, have a relevant impact beyond the measurement uncertainty.

Based on this results the growth time was limited to 30 min and four reaction baths with a different water amount were used. One with pure dried toluene ($\Rightarrow\sim 6\,\mu$g/g), one with a 9/1 mixture ($\Rightarrow\sim 9\,\mu$g/g), 7/3 mixture ($\Rightarrow\sim 15\,\mu$g/g) with standard toluene from Sigma-Aldrich and one only with standard toluene from Sigma-Aldrich (~ 28 ppm).

The characterization of the layers was made by Jiří Novák with XRR. The results are shown in table 6.3. The dependence of the resulting layer thickness on the water content in the toluene bath is shown in figure 6.5. There are too less data points for a solid interpretation, but the thickness of the layers seems to saturate for higher water concentrations.

Table 6.3: *XRR results of the SAM layers grown in toluene reaction baths with different water contents: c - water concentration in reaction bath; t - layer thickness; et - layer thickness error; r - roughness; er - roughness error; the layers show a rising roughness with the layer thickness*

c / ppm	t / nm	et / nm	r / nm	er / nm
6	1.33	0.02	0.34	0.02
6	1.37	0.03	0.33	0.03
6	1.59	0.03	0.37	0.03
9	3.67	0.05	0.72	0.05
15	6.2	0.1	1.2	0.3
28	9.4	0.4	1.8	0.2

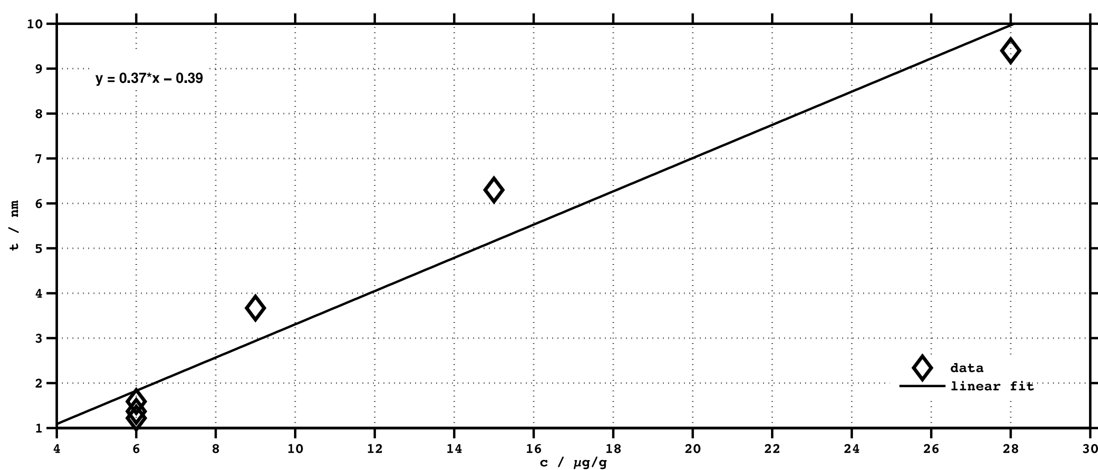


Figure 6.5: *Thickness to water content of the growth bath correlation of the SAM layers: The monolayers at a value around 1.3 nm were evaluated more often,*

An interesting feature is the layer thickness to roughness correlation, which is shown in picture 6.6. The growth mechanism seems to change under the presence of water. Residues of SAM molecule aggregations, which can also be seen in picture 6.2, also indicate an increasing roughness with respect to the layer thickness.

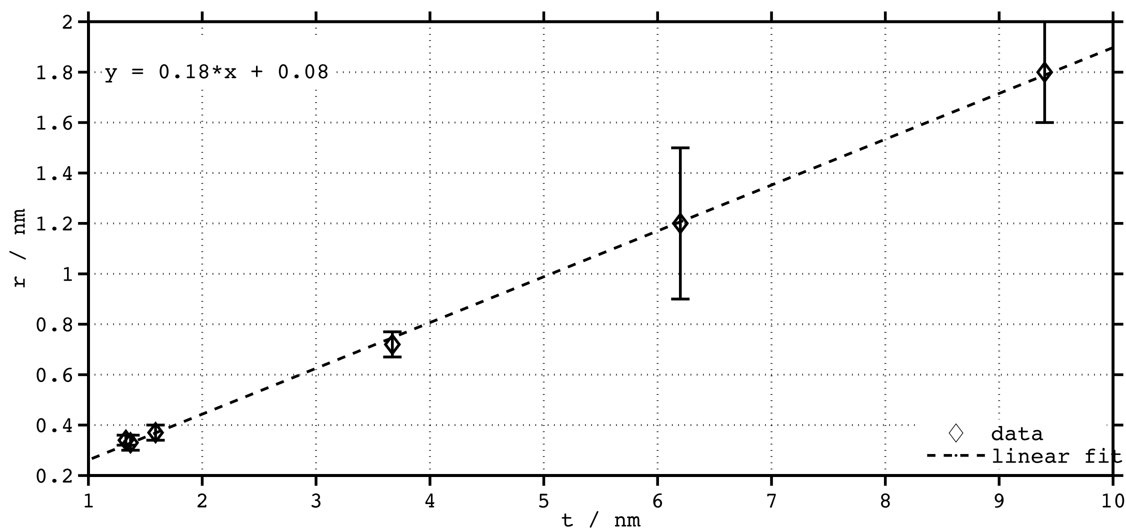


Figure 6.6: *Thickness to roughness correlation of the SAM layers: the surface roughness is linearly related to the layer thickness.*

6.4.2 Polymer Layers

As an alternative approach for introducing an acidic functionality at the dielectric/semiconductor interface to the SAMs, polymers with acidic groups were tested.

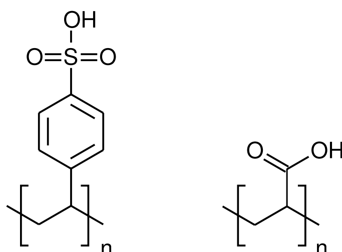


Figure 6.7: *Polymers for the interface modification: left - polystyrenesulfonic acid (PSSA); right - poly-acryl acid (PAA)*

Two acidic polymers were used and deposited by spin coating. 18 $wt\%$ poly(4-styrenesulfonic acid) and 30 $wt\%$ poly-acryl acid, as depicted in picture 6.7, were both provided by Sigma Aldrich in an aqueous solution. First tests were made to evaluate the influence of the rotation speed and the concentration (see tab 6.4). Obviously the 4 mg/ml solution results in a twice as thick layer as the 2 mg/ml.

Table 6.4: *XRR results of the polymer layers: double concentration results in a doubled layer thickness*
c - concentration; rpm - rotation speed of the two coating steps; t - layer thickness

acid	c / mg/ml	rpm 1	rpm 2	t / nm
PSSA	4	1000	2000	18.6
PSSA	4	2000	3500	11.3
PSSA	2	2000	3500	5.5
PAA	4	1000	2000	8.8

The rotation speed of the spin coater is limited which makes a series towards smaller thicknesses difficult. For this reason it was decided to vary the thickness with the concentration and leave the rotation speed constant. Additionally, only the sulfonic acid was used due to its higher acidity. This led to the following specific process steps, which were followed for all concentrations:

- Mounting of the pretreated substrates on the vacuum table of the spin coater
- Surface cleaning with CO_2
- Deposition of 150 μl solution with a pipet and wetting of the whole substrate

- Spinning for 9 s at 2000 rpm and 40 s at 3500 rpm

A solution series with concentrations from 0.5 to 4 mg/ml was fabricated and evaluated by x-ray reflectivity. The result is shown in table 6.5. The 0.5 mg/ml layer was not accessible by means of XRR. As expected the thickness to concentration dependence shows a linear behaviour with virtually no deviations as depicted in figure 7.11. The vanishingly small roughness of the layers of 0.05 nm indicates perfectly smooth surfaces, which should suit well for the growth of the active layer.

Table 6.5: *XRR results of the PSSA concentration series: c - concentration; t - thickness; et - thickness error; r - roughness; er - roughness error; d - electron density; the data of the 4 mg/ml layer was characterized in an earlier measurment, where the rougness was not evaluated*

c / mg/ml	t / nm	et / nm	r /nm	er / nm	d / g/cm^3
0.5	-	-	-	-	-
1	2.76	0.33	0.05	0.02	1.39
1.4	3.75	0.32	0.05	0.01	1.39
2	5.54	0.34	0.02	0.01	1.46
2.5	6.80	0.36	0.05	0.02	1.45
3	8.03	0.34	0.05	0.01	1.48
4	11.3	0.30	-	-	-

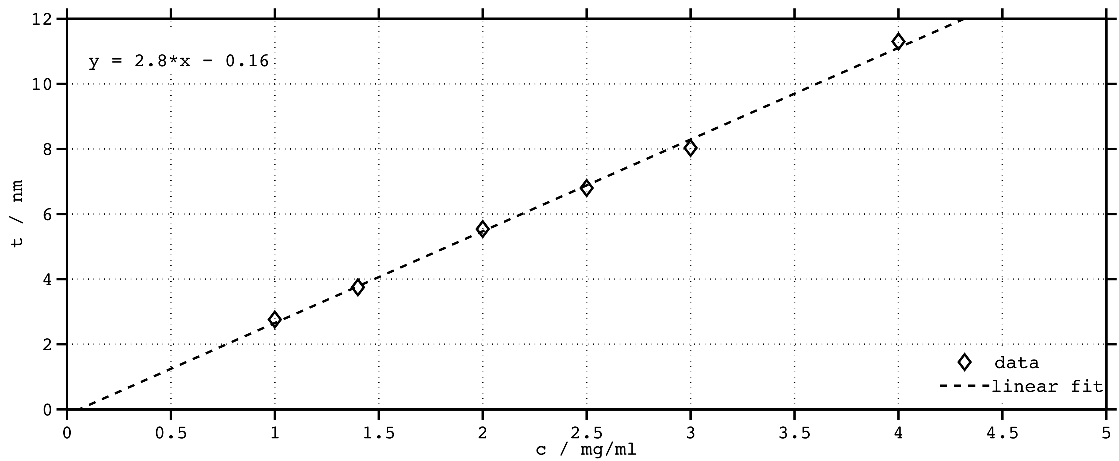


Figure 6.8: *Thickness to concentration relation of the PSSA layers: a strictly linear realtion with vanishing errors is found; the exact values with roughness and error can be found in tab 6.5*

These substrates with layers of different, defined thicknesses, either achieved by SAM growth or polymer spincoating, were subsequently used to built devices, as described in the beginning of this chapter.

Chapter 7

Device Performance

The devices, which were built as described in the previous chapter, were characterized by transfer curves and parameters like the mobility, threshold, and onset voltage were extracted. All measurements were performed in the measurement cell under inert conditions (in the glove box), while exposing the devices to the "standard" laboratory illumination and at ambient pressure, unless stated differently. The delay time (time of each measurement step between the application of the voltage and measurement of the current) was set to 0.1 s, the drain voltage to -2 V for pentacene and -45 V for P3HT devices, also unless stated otherwise. Before measuring, the active layer around source and drain pads (naturally not in the channel) was removed with a scalpel or the tip of a tweezer, which reduces the leakage current by about 1 to 2 orders of magnitude. The contact between the cell probes and the gold pads was always checked with a resistance measurement by a Fluke 83 multimeter before starting the measurements.

The device parameters were extracted from the first measurement sweep (from positive to negative gate voltage). Following section 3.6.3, the threshold voltage of the pentacene devices is extracted in the linear regime by the linear extrapolation method. The P3HT devices were characterized with a higher drain voltage, thus the extrapolation was made with the square root of the drain current in the saturation regime. The onset voltage was determined by the highest second derivative method on a logarithmic scale.

As already mentioned the substrates were continuously numbered. Some of the substrates were used for the development of the interfacial layers and, therfore, not used for building devices. An overview and the naming of the devices, including their active layer and interfacial layer, can be found in table 7.1.

Table 7.1: *Overview of fabricated devices: L1-L72 - continuous substrate naming; several substrates were used for the characterisation by x-ray reflectivity*

name	active layer	interface layer	comments
L1 - L17	P3HT Plextrinics	misc. layers	preliminary tests
L18	P3HT Sigma Aldrich	reference device	degenerated after 1 week
L19	P3HT Sigma Aldrich	1.4 nm SAM	degenerated after 1 week
L20 - L29	P3HT Sigma Aldrich	references and SAMs	no properly working devices
L30	Pentacene	1.4 nm SAM	-
L32	Pentacene	3.7 nm SAM	source-drain shortcut
L33	Pentacene	6.2 nm SAM	-
L34	Pentacene	reference	-
L35 -L38	P3HT Sigma Aldrich	polymer layers	no working devices
L39 -L45	P3HT Plextronics	misc. SAMs	no working devices
L46 -L48	P3HT Plextronics	polymer layers	no working devices
L49 - L52	Pentacene	5.5 nm PSSA	badge 1
L53, L54	Pentacene	references	-
L55, L56	Pentacene	3.8 nm PSSA	badge 2
L57, L58	Pentacene	5.5 nm PSSA	-
L59, L60	Pentacene	8.0 nm PSSA	-
L61, L62	Pentacene	3.8 nm PSSA	badge 3
L63, L64	Pentacene	5.5 nm PSSA	-
L65, L66	Pentacene	8.0 nm PSSA	-
L67	Pentacene	1.2 nm PSSA	badge 4
L68	Pentacene	2.8 nm PSSA	source-drain shortcut
L69	Pentacene	3.8 nm PSSA	-
L70	Pentacene	5.5 nm PSSA	-
L71	Pentacene	6.8 nm PSSA	-
L72	Pentacene	8.0 nm PSSA	-

7.1 P3HT Devices

Many experiments had to be made in order to get working devices. Since the P3HT provided by *Plextronics* did not work, another derivate by *Sigma Aldrich* was used. Our initial supposition that the layer thickness is too high, hindering charge injection, was discarded after a XRR measurement. These measurements indicated a layer thickness of 9.2 ± 0.2 nm for the Plextronics P3HT and 11.7 ± 0.3 nm for the P3HT from Sigma Aldrich, which is reasonably thin. Fresh solvent, a new solution and different concentrations also did not improve the results very much. Even though, some reasonable working devices were realized with the Sigma-Aldrich P3HT. Measurements indicated, that these devices were susceptible to bias stress, which is indeed typical for P3HT.

A representative sample displaying the bias stress effect is shown in figure 7.1. The device L19 is a P3HT device with a 1.3 nm SAM interface layer. After two subsequent measurements there is the characteristic, bias-stress induced shift of the onset and threshold voltage towards negative bias. The difference of the mobility and threshold voltage is indicated by the linear extrapolation in the squareroot plot. The extracted device parameters before and after the bias stress are shown in table 7.3.

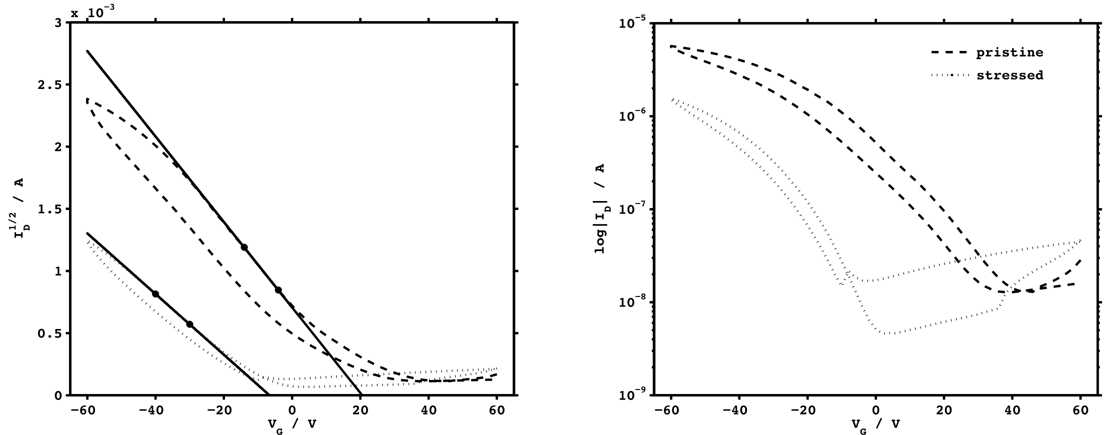


Figure 7.1: *Logarithmic and root plot of the transfer characteristic of a P3HT device with a 1.3 nm SAM, measured at -45 V drain voltage: The dotted line represents the transfer curve after two subsquent measurments, which changed substantially because of bias stress. The parameter extraction by linear extrapolation is indicated in the square-root plot*

These devices, however, degenerated after about a week, which manifested itself in high off currents and leakage currents. Later on a severe water and oxygen inbrake in the glove box was discovered which explains the instability of the devices retrospectively.

Table 7.2: *n - number of subsequently performed measurements;* V_T *− thresholdvoltage;* V_0 *− onsetvoltage;*μ *- mobility; Parameter evaluation of a P3HT device L19 with a 1.3 nm SAM interface before and after bias stress*

n	V_T / V	V_0 / V	μ / cm²/Vs
2	20.6	42	$4{\cdot}10^{-4}$
4	-3.8	0	$2{\cdot}10^{-4}$

Another device, the reference device L18 also suffered from this degeneration. In order to reduce the influence of the atmosphere some measurements in vacuum were performed as shown in figure 7.2.

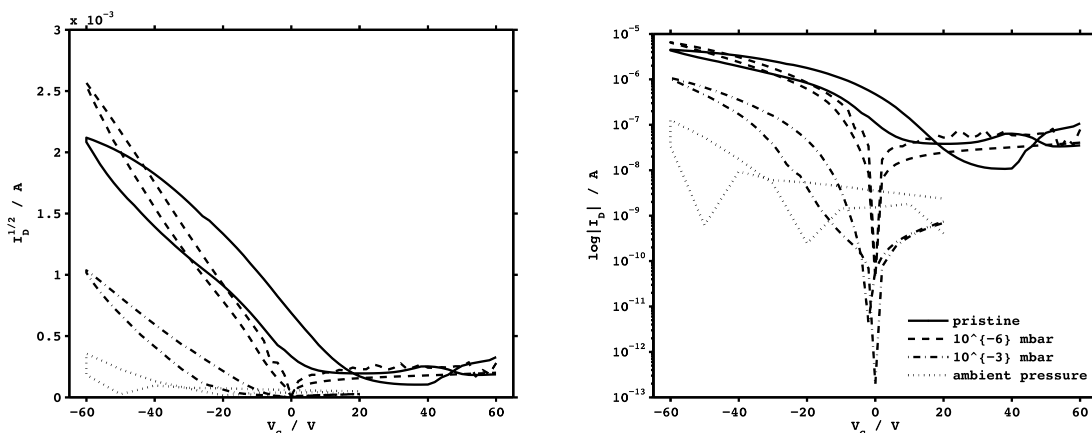


Figure 7.2: *Logarithmic and root plot of the transfer characteristic of a P3HT reference device, measured at -45 V drain voltage: solid line - 10*^{3} *mbar; dashedline −* 10^{-6} *mbar; dash-dotted line - darkness and 10*$^{-3}$ *mbar; light dotted line - 10*^{3} *mbar*

The transfer curves reveal some interesting features. In comparison to the device L19 with the SAM interface the onset voltage before the vacuum treatment (solid line) is smaller and shows also a smaller subthreshold swing, which could be expected for the reference device. After evacuating the measurement chamber to about 10^{-6} mbar (dashed line), measured at the turbomolecular pump - not in the chamber, the subshreshold swing vanishes. The current at 0 V gate voltage is nearly zero, respectively below the measurement range of the sourcemeter. The hysteresis, also decreases significantly, which lets conclude the following: As discussed earlier, the sub-threshold swing and the hysteresis are usually connected to a high trap density. This trap sites often originate from water and oxygen molecules, which diffuse into the P3HT bulk

Table 7.3: *p - pressure in the measurment chamber;* $V_T -$ *thresholdvoltage;* $V_0 -$ *onsetvoltage;*μ *- mobility; Parameter evaluation of the P3HT reference device L18 at different pressure conditions*

device	p / mbar	V_T / V	V_0 / V	μ / cm^2/Vs
L18	10^3	0	30	$9 \cdot 10^{-4}$
L18	10^{-6}	1	0	$7 \cdot 10^{-4}$
L18	10^{-3}	-13	-2	$2 \cdot 10^{-4}$
L18	10^3	-29	-	-

[20] [21]. Apparantly, these impurities can be extracted by vacuum, which reduces the trap density and, subsequently, also the hysteresis and sub-threshold swing. Unfortunatly, after an increase of the pressure, the device suffers a complete breakdown. The extracted parameters of the shown transfer curves can be found in table 7.3

Over all, the performance and especially stability of the P3HT devices were too poor for extensive investigations using interface layers. The application of the water diluted polymer layers is also questionable since small water residues would affect the performance of the P3HT.

7.2 Pentacene Devices

The previous results forced us to switch the active material to pentacene, which is known to be more stable to water and oxygen on the one hand, but its deposition more complex, on the other hand. A threshold voltage shift in pentacene devices as a result of acidic groups has already been observed by Marchl et al. [55]. When this thesis started, there was evidence, that the mechanism in pentacene is based on proton transfer doping, but it was not yet clearified. The experiments of this thesis, and the parallel work of Reinhard Hetzel and especially Simon Außerlechner gave well-founded indications that proton transfer doping, indeed, works also in pentacene.

7.2.1 T-SC/T-SA Interface Layers

Devices were built with the SAM layers according to section 6.4.1 and characterized. Unfortunatly the device with the 3.7 nm SAM had a shortcut between between source and drain due to underevaporated gold. Therefore only the four devices of the substrates L30 with a 1.3 nm layer and the four devices of substrate L33 with a 6.2 nm SAM were available for characterisation. The evaluation of these devices showed stable and defined transistor characteristics with small hysterisis and reasonable mobilities. The devices were repeatedly characterized about once per week to two weeks in order to record the threshold voltage shift. During this time the devices were stored in petri dishes in the glove box and exposed to the usual laboratory illumination.

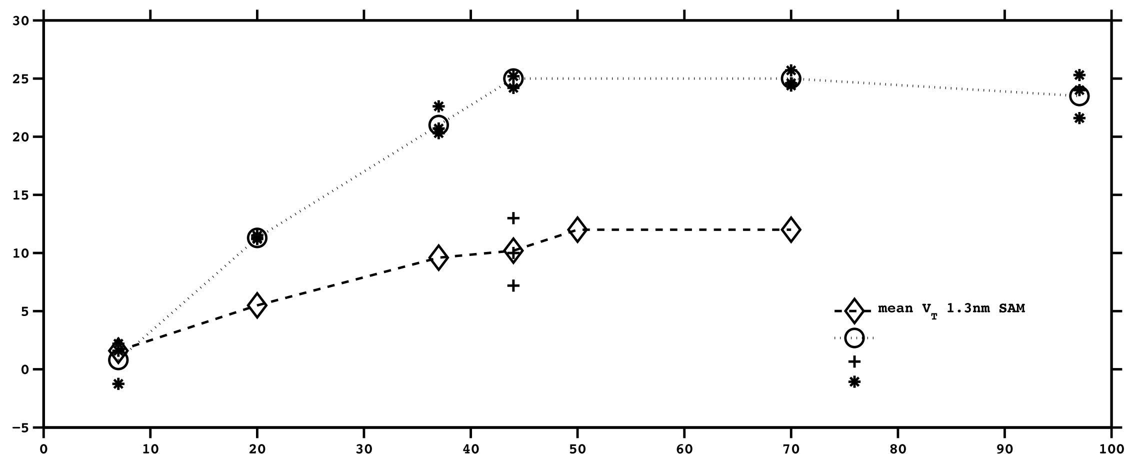


Figure 7.3: *Threshold voltage's time development of pentacene devices with a SAM interfacial layer: the circles represent mean values of devices with a 6.2 nm SAM; the tilted squares stand for a device with a 1.3 nm SAM*

The time development of the the threshold voltage's mean value of devices of the two substrates L30 and L33 is shown in picture 7.3, where a faster increase of the device

with the thicker interface layer is visible as well as the saturation of the increase for both devices after about 50 days.

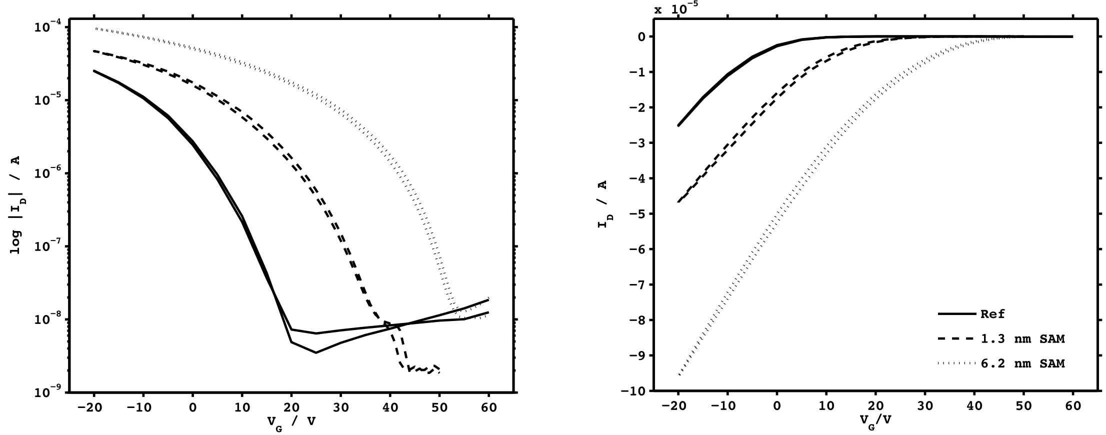


Figure 7.4: *Logarithmic and linear plot of transfer characteristic of pentacene devices with SAM interfacial layers and a reference device, after the V_T shift was completed; measured at -2 V drain voltage: solid line - reference device; dashed line - 1.3 nm SAM, dotted line 6.2 nm SAM*

After the completion of the threshold voltage shift, the transistors still show a small hysterisis and a good performance as shown in figure 7.4. As can be seen for the device without interface layer, the reference, also there the onset voltage is indeed positive and all devices show a subthreshold swing, which indicates a not negligible trap density. The off current apparently does not increase with respect to the threshold voltage, which indicates a doping only at the interface region and not for the whole bulk. Unfortunatley, due to extensive measurements (especially devices from substrate L30 suffered a disruptive breakdown) and the complicated fabrication the evaluation of the final threshold voltage shift was only possible with 4 devices, three with the 6.2 nm and one with the 1.3 nm SAM. The extracted parameters of these devices are shown in table 7.4.

Allthough one would expect the opposite, the mobilities of the reference device and the devices with the rougher interface layer are practically the same. Measurements of Simon Außerlechner [56], showed a much bigger V_T shift of nominally equivalent devices with a 1.2 nm TS-C/TS-A layer. He grew the SAMs in 16 hours. Obviously the longer growth time, compared to the half hour, which was used for the growth of the layers used in the present work, has a impact on the density of the SAM layer.

Figure 7.5 shows the threshold voltage shift to the SAM layer thickness. The linear fit does not make too much sense for two data points, but it gives an indication that the thin SAM has already a relativly big impact. This fact will be discussed in more detail

Table 7.4: *t - thickness of the SAM;* $V_T - thresholdvoltage; V_0 -$ *onsetvoltage;*μ *- mobility; Parameter evaluation of the pentacene reference device and the pentacene devices with a SAM interfacial layer*

t / nm	V_T / V	V_0 / V	μ / cm^2/Vs
-	3	25	0.16
1.3	12	36	0.15
6.2	22	54	0.16
6.2	24	46	0.16
6.2	25	54	0.16

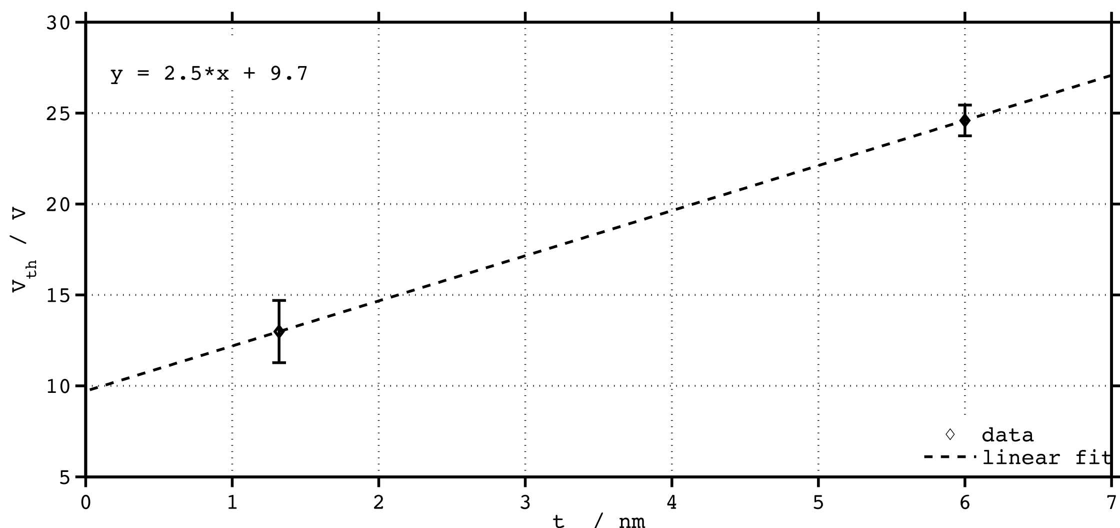


Figure 7.5: *Threshold voltage to SAM thickness dependence of pentacene devices with a SAM interfacial layer: a linear extrapolation results in a threshold voltage of 10 V for a device with no interfacial layer (reference device)*

in the next section, when the results are compared with those of the PSSA interface layers. More transfer characteristics of the devices, which were measured during the evolution of the threshold voltage shift can be found in the appendix of this chapter.

Overall, the results for pentacene devices with the SAM based interface layers are very conclusive with the big drawback of the difficult fabrication of the SAMs. A fully controlled preparation would include a water content measurement of the toluene, XRR characterisation of the SAMs, and an AFM characterisation of the SAMs and the pentacene layers. Since all these measurements are performed by different groups at different places, this fabrication sequence is very difficult to arrange.

7.2.2 PSSA Interface Layers

Compared to the SAMs the PSSA layers showed a very smooth surface, reproducable layer thickness and easy fabrication. Although residues of the solvent water would induce trap sites (water causes trap levels of 0.6 eV in pantacene [18]), the approach by spin coated polymers as active interfacial layer seemed very promising.

According to the results from section 6.4.2, several badges of devices were built with PSSA layers from about 1.3 to 8.0 nm (corresponds to spin casting from 0.5 to 3.0 mg/ml PSSA solutions). The first badge with the internal naming L49 to L54, then L55 to L60, L61 to L66 and finally L67 to L72 to close the data gaps of the 0.5, 1 and 2.5 mg/ml layers (a detailed list of the devices and their namings can be found in table 7.1).

One important thing, which was discovered after completion of experimental work, is that the pentacene evaporation procedure was changed in comparison to the pentacene devices with the SAM. The substrates with the PSSA layers were not heated anymore during the evaporation of the pentacene. This affects the comparability with the devices with the SAM interfacial layer and the device performance itself. Heating of the substrates has an influence on crystal growth [27], and, therefore on the mobility and trap density. Furthermore, possible water residues, which increase the trap density, are also reduced by heating. Retrospectively, many features occuring in the PSSA based devices, like a bigger hysteresis compared to the SAM based devices, bias stress, big subthreshold swing, varying mobilities, or a high off current in darkness, could partly be explained by the presence of an uncontrolled amount of water. The arbitary water content in the device is much more compensated out by the heating.

It is supposed that the water residues were affected by the temperature (varied from 20 °C to about 25 °C) and humidity (the absolute humidity is strongly temperature dependent, but only the relative humidity was known) in the laboratory, or possible leakage of the transport box during transport has an impact on the water residue. Thus, if anything, the water content and, therefore, the trap density of one badge for the same layer thickness can be assumed to be constant.

Analoguously to the devices with the SAM layers, the transistors were characterized by transfer curves at a drain voltage of -2 V. The measurement procedure changed a little bit over time, since bias stress was discovered and several devices suffered a disruptive breakdown at gate voltages above 80 V. Therefore, measurements later on were performed with lower gate voltages, the devices were not stressed too much and, thus, characterized less often.

Before the outcome of the threshold voltage shift will be discussed, the previously commented deviations from the typical behaviour of pentacene OTFTs, fabricated with substrate heating, will be discussed.

7.2.2.1 Bias Stress

Some devices showed a big susceptibility to bias stress effects, which was previously not observed in our measurements. The stress effect manifested itself in a shift of the threshold and, especially the onset voltage to higher voltages, when applying a gate voltage above about 80 V. It is supposed, that this feature is related to the water processed polymer layer.

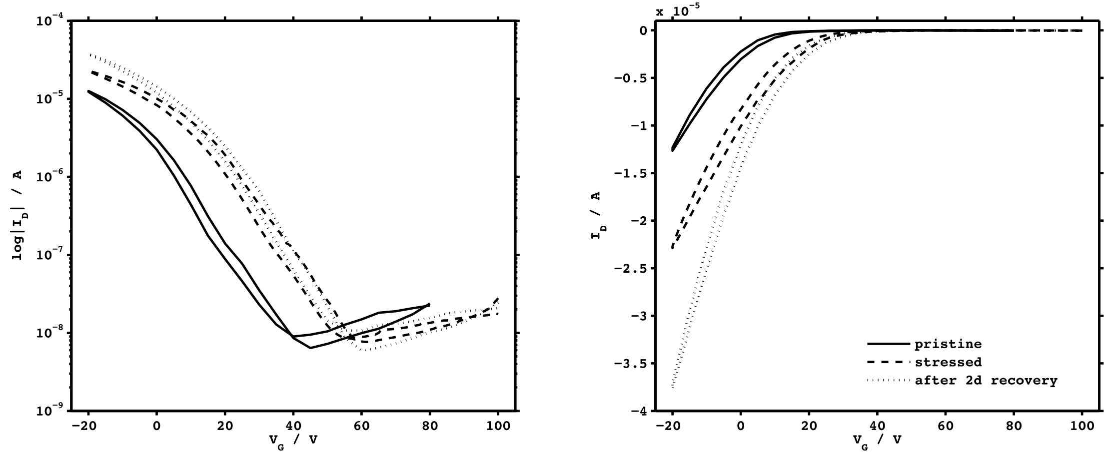


Figure 7.6: *Logarithmic and linear plot of transfer characteristic of the pentacene device L 61 with a 3.8 nm PSSA interfacial layer, in pristine condition, stressed and after 2 d recovery; measured at -2 V drain voltage: solid line - pristine; dashed line - stressed, dotted line - after 2 d recovery*

The effect was encountered first for a device with a 3.8 nm PSSA layer (L61, third badge - see table 7.1), before the acid induced threshold voltage shift was completed. After several subsequent measurements, the threshold voltage increased from 4 to 16 V and decreased again to 11 V after two days of recovery. The steady state of the (acid induced) threshold voltage shift was reached six weeks later at a value of 21 V. It seemed, that the bias stress did not affect the functionality of the proton transfer doping, since it was reversible and later on cought up with the steady shift induced by the PSSA layer.

Figure 7.6 shows the transfer characteristics of the mentioned device in pristine and stressed conditions, and after after 2 d recovery. The shift back to 11 V is not very well visible, because of the better mobility (see next section). For this reason all parameters of the device in the different conditions are listed in table 7.5. As a consequence of the bias stress, extensive measurements were avoided in further characterisations.

Table 7.5: *V_T – thresholdvoltage; V_0 – onsetvoltage; μ - mobility; Parameter evaluation of the pantacene device L61 with a 3.8 nm PSSA layer at the interface before and after stressing and after 2 d recovery*

condition	t / nm	V_T / V	V_0 / V	μ / cm^2/Vs
pristine	3.8	4	20	0.04
stressed	3.8	16	35	0.05
2 d recovery	3.8	11	40	0.09

7.2.2.2 Mobility

All devices with the PSSA interfacial layer showed an improvement of the mobility with the time. Starting from about 0.03 cm^2/Vs the mobilities improved to about (0.10 ± 0.02) cm^2/Vs for the devices with the thinner interface layers. It was observed, that the devices with the thicker interface layers (6.8 and 8.0 nm) showed higher mobilities of about (0.13 ± 0.02) cm^2/Vs, comparable with those of the reference devices. Figure 7.7 shows the increase of the mobility of a representative pentacene device with a 3.8 nm interface layer.

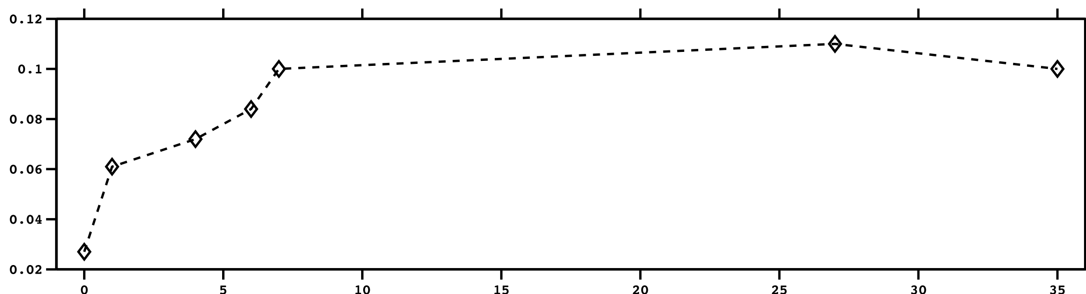


Figure 7.7: *Mobility increase with time of a pentacene device with a 3.8 nm PSSA layer: the mobility increases fast within several days and saturates around 0.1 cm^2/Vs*

This improvement could be caused by various effects, like maturing of the crystal structure, but is to a small part caused by the extraction of the mobility values. Obviously, the effective gate voltage is larger for a device with a threshold voltage of 40 V, compared to one with 10 V. Thus, the extraction of the mobility is applied in a different range of the current curve. Again it is also proposed, that a high density of shallow traps, caused by water residues of the PSSA layers, is causing this effect. Drying in the glove box, could explain the improvement.

One feature, for which no explanation has been found yet, was that two devices showed

deviations from the usual mobility values. On two substrate, one device had a mobility of only 0.05 cm^2/Vs, whereas the others featured the usual values around 0.1 cm^2/Vs. A very improbable but obvious explanation would be, that the tungsten wire, which structures the channel would have been changed to 50 microns accidentially, since others on the laboratory worked with longer channel lengths and we used the same evaporation masks.

For the sake of presentability, when comparing different transistors, devices with comparable mobilities were chosen.

7.2.2.3 Impact of Light

One would expect that light increases the off current, which was also often observed [57]. Few of the pentacene devices with the PSSA layers, especially from the later badges, however, showed an opposite behaviour. The off current rose, when the devices were characterized in darkness. Figure 7.8 shows a transfer characteristic of a device fabricated by Simon Außerlechner. Before closing the measurment box, the transistor shows a defined characteristic with small hysteresis. After closing the box, the current of the backsweep shows a kink, which can also be observed at high doping levels [58][40][59]. For the next measurment, the box was opened again and the device was exposed to the usual laboratory illumination again. The transfer characteristic coincides with the curve before again.

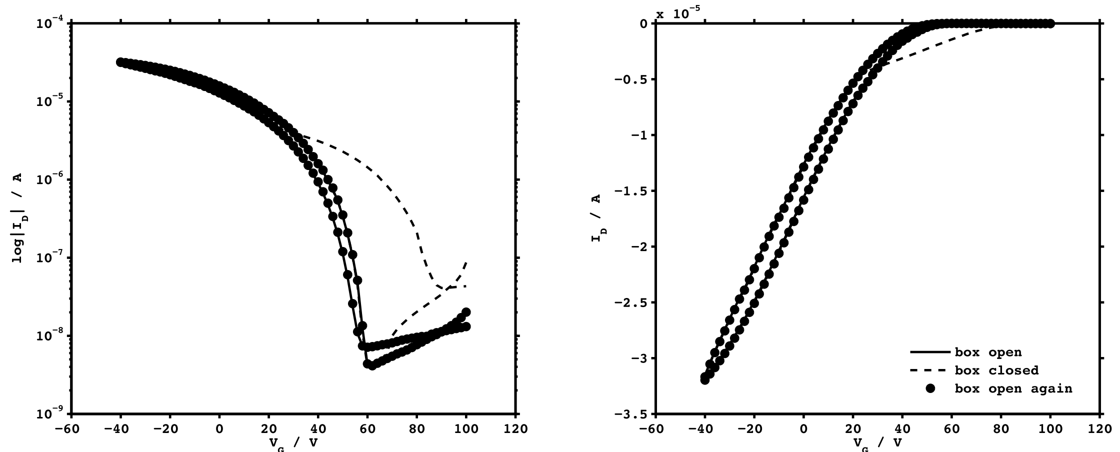


Figure 7.8: Logarithmic and linear plot of transfer characteristic of a pentacene device with PSSA interfacial layers exposed to light and in darkness; measured at -2 V drain voltage: solid line - exposed to light; dashed line - darkness, closed measurment box, data points - again exposure to light

This effect was particularly present in devices with a high treshold voltage. It was

supposed, that the light continuously emptied a high number of trap states, which were filled in darkness and provoked a high off current. This was actually shown once in one measurement with 10 s delay time (the time between application of voltage and measurment of current) in darkness, which resulted in the same characteristic as in light. But due to the high stress of this measurement procedure, it was not tried on more devices.

One big drawback of the sensitivity to light concerned the measurements during exposure to ammonia, which had to be performed in the closed measurement cell. Furthermore it should be mentioned, that the sensitivity to light was only a problem of the devices fabricated in Weiz. The devices, which were fabricated later (after completion of my experimental work) in our lab did not show this feature.

7.2.2.4 Threshold Voltage shift

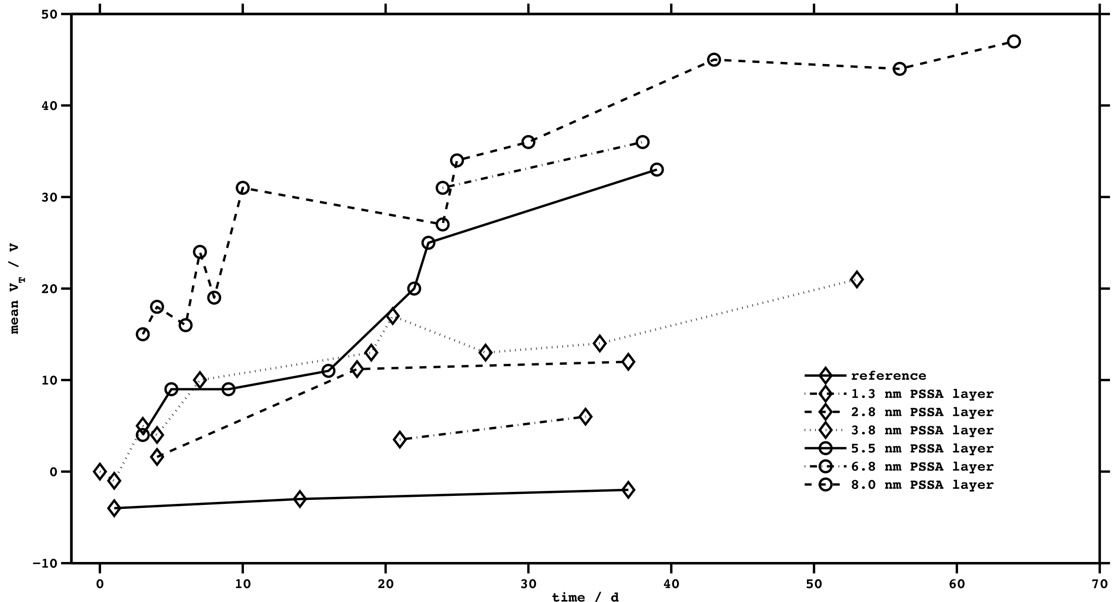


Figure 7.9: *Threshold voltage's time development of PSSA/pentacene devices: In comparison to the SAM/pentacene devices the shift sets in much faster.*

All the previously mentioned problems evidently influenced the evaluation of the PSSA layer induced threshold voltage shift. Changing mobilities, the bias stress and the influence of light are capable of varying the result, since the extraction methods still have their shortcomings. As a matter of fact, the results of the threshold voltage evaluation did vary for the same interface layer. Some proposed reasons are the possibly different water residues, a difference in the temporal evolution of the devices (the shifts saturate after a different time) and the previously mentioned points concerning the

evaluation. For this reason it was decided to work with the mean value and only look at the trends the parameters, instead of comparing each device seperatly.

In figure 7.9 the development of the devices' threshold voltage is plotted. The data points represent the median value of multiple measurements of several devices. The transistors with the 1.3 nm and 6.8 nm interfacial layer were the last devices built, and after being aware of the bias stress were measured only twice. Compared to the development of the SAM devices, The transistors with the PSSA layers show already very early a significant V_T shift. The transfer characteristics during the evolution of the threshold voltage shift can be found in the appendix of this chapter.

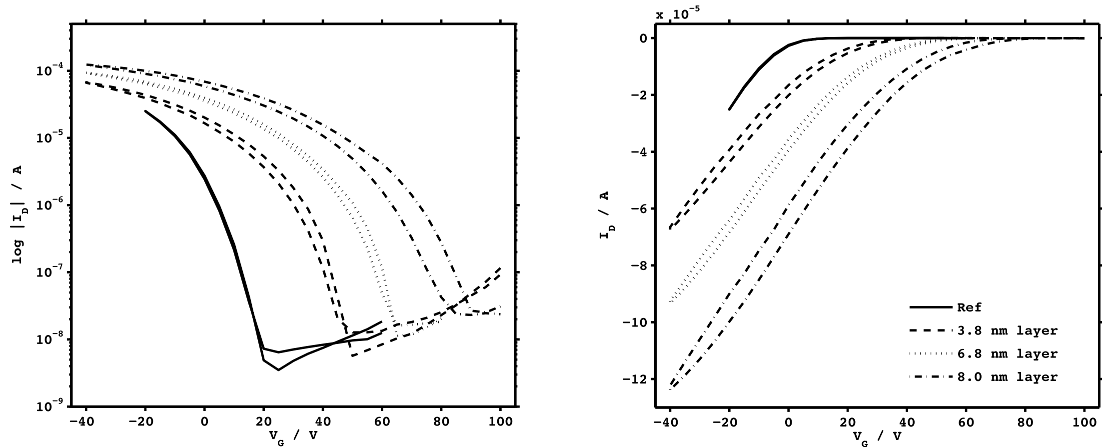


Figure 7.10: *Logarithmic and linear plot of transfer characteristic of pentacene devices with PSSA interfacial layers and a reference device, after the V_T shift was completed; measured at -2 V drain voltage: solid line - reference device; dashed line - 3.8 nm PSSA layer, dotted line - 6.8 nm PSSA layer, dash-dotted line - 8.0 nm PSSA layer*

After about two months, all devices reached a steady state and the acidic layer thickness obviously showed an impact on the increase of the threshold voltage. Transfer curves for three representative PSSA devices with comparable mobilites and device without interfacial layer are shown in figure 7.10, where a parallel shift analogous to the SAM devices but also a higher hysterisis are evident.

Figure 7.11 shows a nice linear dependence of the threshold voltage to the layer thickness. As can be seen, there are deviations from the single data points to the mean value. Especially the values of the devices with the 5.5 nm interfacial layer vary, which relativizes a little bit considering the circumstances of the parameter evaluation. These were the first fabricated devices and follow-ups were produced in three different badges. Therefore, the measurement procedure change, after being aware of the bias, affected this devices most.

An overview of the mean values of the threshold voltage compared to the interfacial layer thickness can be found in table 7.6.

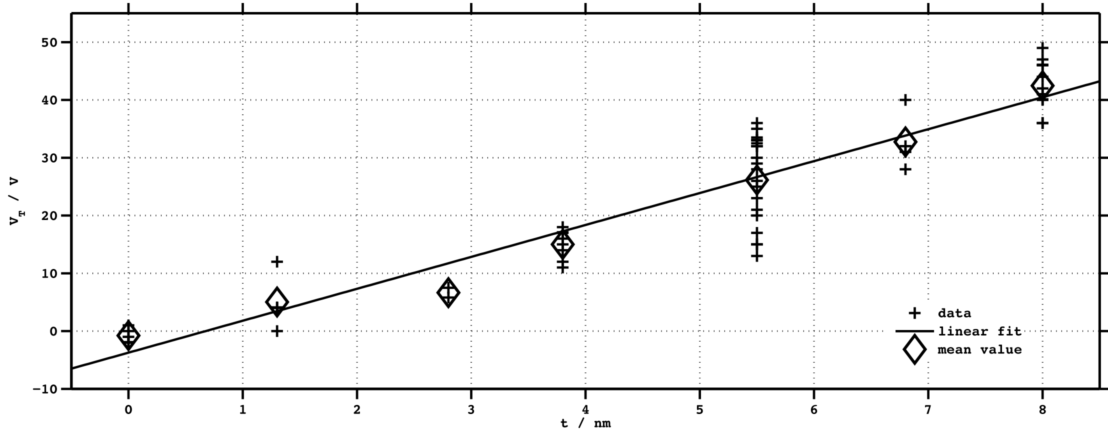


Figure 7.11: *Threshold voltage to PSSA interface layer thickness dependence: The mean values are plotted as the big tilted squares, the single data points as small crosses.*

Table 7.6: *c - concentration of PSSA solution; t - thickness of PSSA layers; mean* $\mathrm{V_T}$ *- mean value of all extracted* $\mathrm{V_T}$ *with standard deviation; Threshold voltage to PSSA interface layer thickness corralation of pentacene devices*

c / mg/ml	t / nm	mean $\mathrm{V_T}$ / V	std dev / V
0.0	0	-1	1.3
0.5	~ 1.3	5	5.0
1.0	2.8	7	1.2
1.4	3.8	15	2.5
2.0	5.5	24	7.9
2.5	6.8	36	5.7
3.0	8.0	42	4.3

7.2.3 Comparison of the Impact of the SAM and the PSSA Layers

As already mentioned comparing the results of the devices with the SAMs with those made with the PSSA layers is difficult, since the pentacene evaporation technique changed. Indeed, some remarkable differences between the results of the two layer systems will be discussed and an interpretation tried. These difference concern the following: The SAM causes a higher threshold voltage shift at a thickness of 1.3 nm than the PSSA layer, but the shifts of the 6.3 nm SAM and 6.8 PSSA layer are more or less the same. The next difference is, that the devices with the polymer layer show bias stress and a bigger hysteresis. And last, the faster onset of the threshold voltage shift in the polymer devices.

It is assumed, that the last feature is based on the difference of the pentacene crystal growth. Protons migration from the acid into the pentacene could be enhanced by more grain bounderies, therefore, this feature is most probably caused by the change of the evaporation technique.

The other features however, could be based on a profound difference between the SAM and the polymer layers. The TS-C/TS-S molecules covalently dock onto the oxide and passivate the dielectric. As a consequence, the acid groups are all directed towards the active layer and the properties of the dielectric are also improved. The chains of the polymer, on the other hand are arbitarily oriented. So for the same density there are fewer acid groups directly in contact with the pentacene, which may explain the higher impact of the SAM on the threshold voltage (The T-SC/T-SA molecules and a PSSA monomer have a comparable weight, since the SAM is only a blend with a third acidic groups the acid mass density is approximatly a third of the SAM).

Bias stress and hysteresis are known to be strongly dependent on the dielectric. Here, again, the polymer has worse properties, since it does not fully passivate the surface, and, protons can dissocate into the oxide, probably enhanced by the gate bias. This feature is known to cause bias stress and hysteresis [60]. Therefore, this difference in the device characteristics is also more likely to be caused by the different layer types.

7.2.4 Conclusion

What both interface types definetly have in common, is, that they induce a threshold voltage shift, based on the presence of acidic groups. It was shown, that the purposeful fabrication of devices with more or less defined threshold voltages can be achieved by the variation of the interfacial layer's thickness.

The outcome of these experiments, as did previous measurements with pentacene and acidic layers [55], indicate again a proton transfer based doping in the pentacene crystal.

The full functionality and more substantial results for the verification of proton transfer doping can be found in the latest reference [56]. For the sake of completeness, the suggested working principle of the doping process of the acidic groups is shown in figure 7.12.

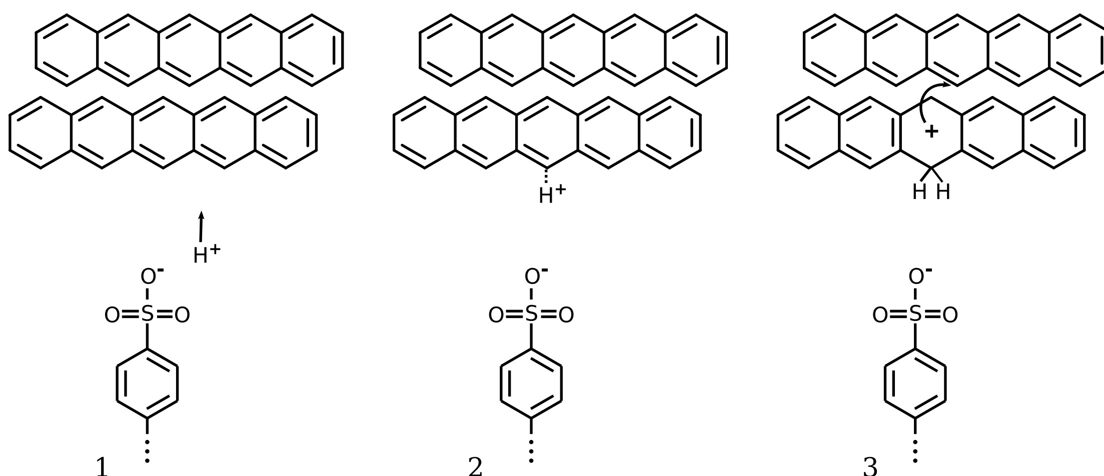


Figure 7.12: *Proton-transfer doping in pentacene according to reference [56]: 1 - a proton dissociates from the acidic group; 2 - the proton binds to the pentacene; 3 - a mobile hole is formed*

APPENDIX: Collection of Characteristics

Pentacene Devices with SAM interfacial layers

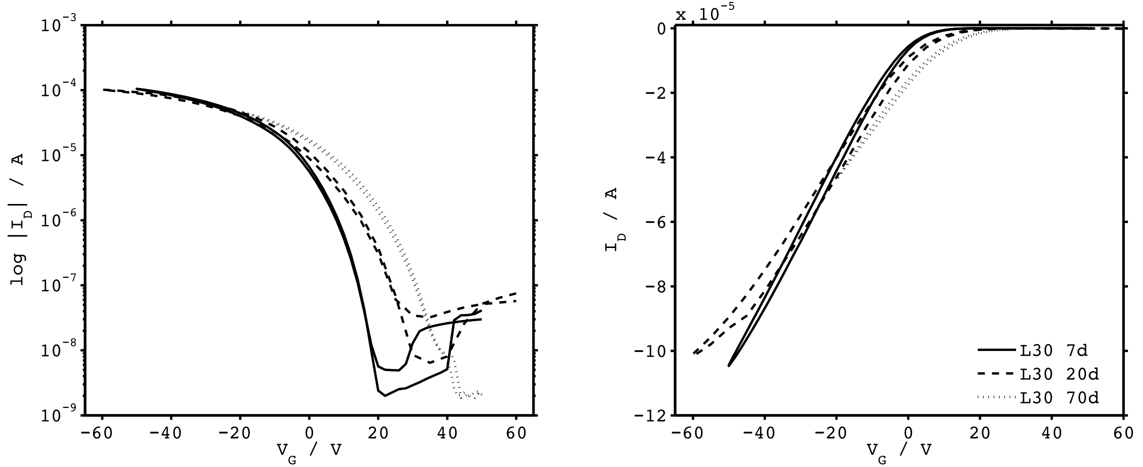


Figure 7.13: *Logarithmic and linear plot of the transfer characteristic; time evolution of a pentacene device with a 1.2 nm SAM interfacial layer; measured at -2 V drain voltage*

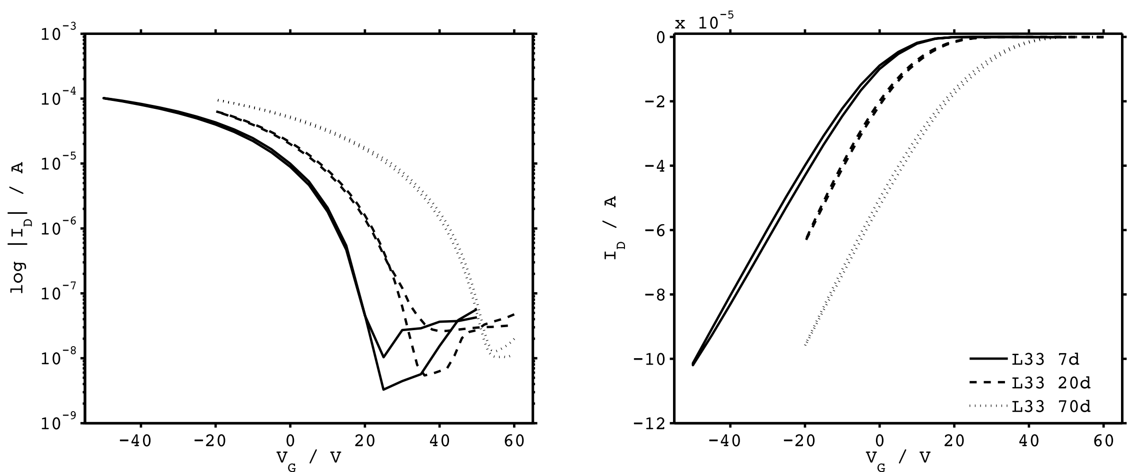


Figure 7.14: *Logarithmic and linear plot of transfer characteristic; time evolution of a pentacene device with a 6.3 nm SAM interfacial layer; measured at -2 V drain voltage: compared to the 1.2 nm layer the shift develops faster.*

Pentacene Devices with a 1.3 nm PSSA layer

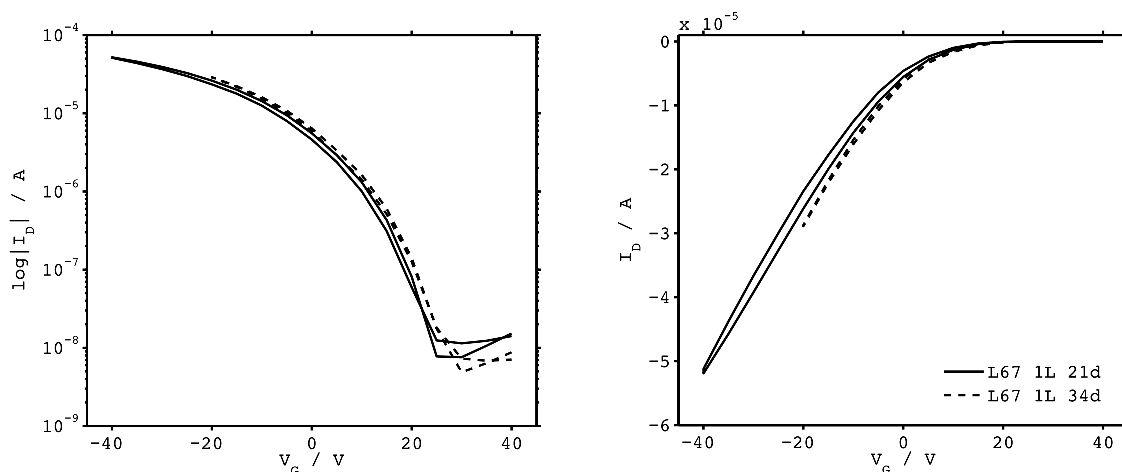


Figure 7.15: *Logarithmic and linear plot of transfer characteristic; time evolution of a pentacene device with a 1.3 nm PSSA interfacial layer; measured at -2 V drain voltage: The first measurements were made after 21 days in order not to stress the device (bias stress was observed in the previous badge), 13 days later the shift is completed*

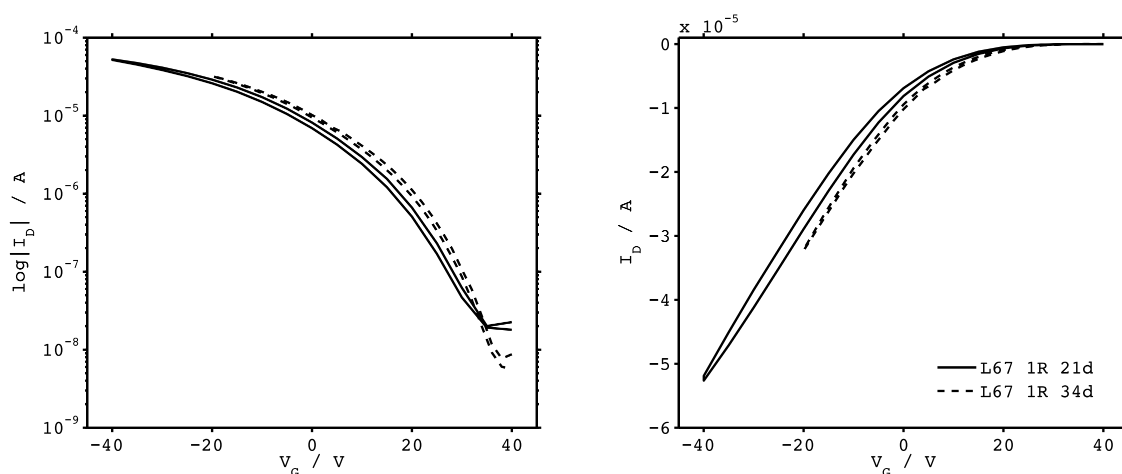


Figure 7.16: *Logarithmic and linear plot of transfer characteristic; time evolution of a pentacene device with a 1.3 nm PSSA interfacial layer; measured at -2 V drain voltage*

Pentacene Devices with a 3.8 nm PSSA layer

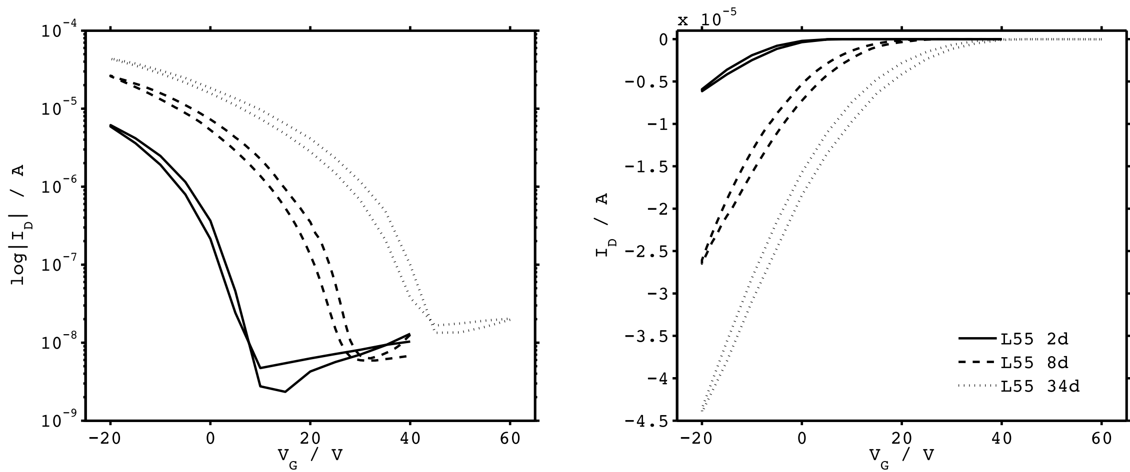


Figure 7.17: *Logarithmic and linear plot of transfer characteristic; time evolution of a pentacene device with a 3.8 nm PSSA interfacial layer; measured at -2 V drain voltage: There is a small rise of the off current visible*

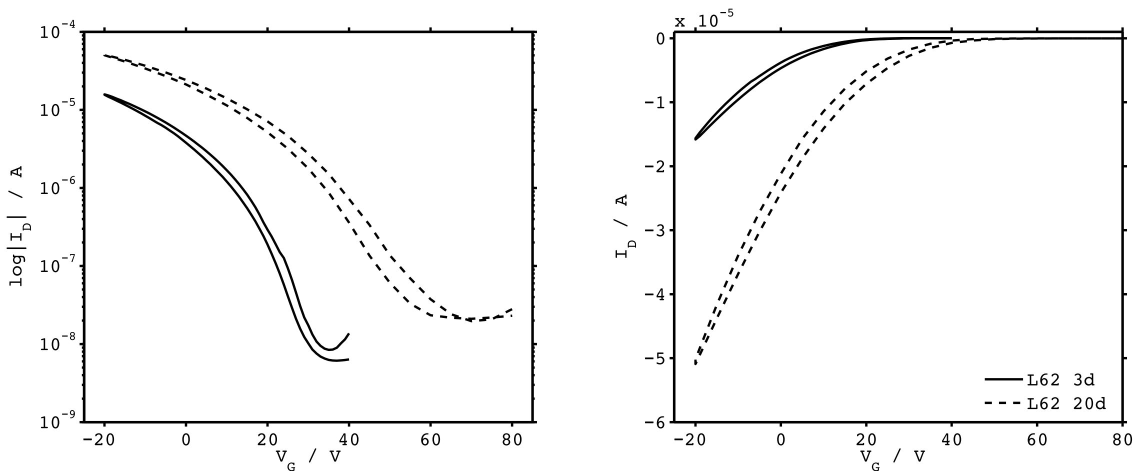


Figure 7.18: *Logarithmic and linear plot of transfer characteristic; time evolution of a pentacene device with a 3.8 nm PSSA interfacial layer; measured at -2 V drain voltage: The device developed it's shift faster and shows a less distinct onset voltage. This behaviour was observed at some few devices and due to the shift of the onset voltage traced back to oxygen exposure[60].*

Pentacene Devices with a 5.5 nm PSSA layer

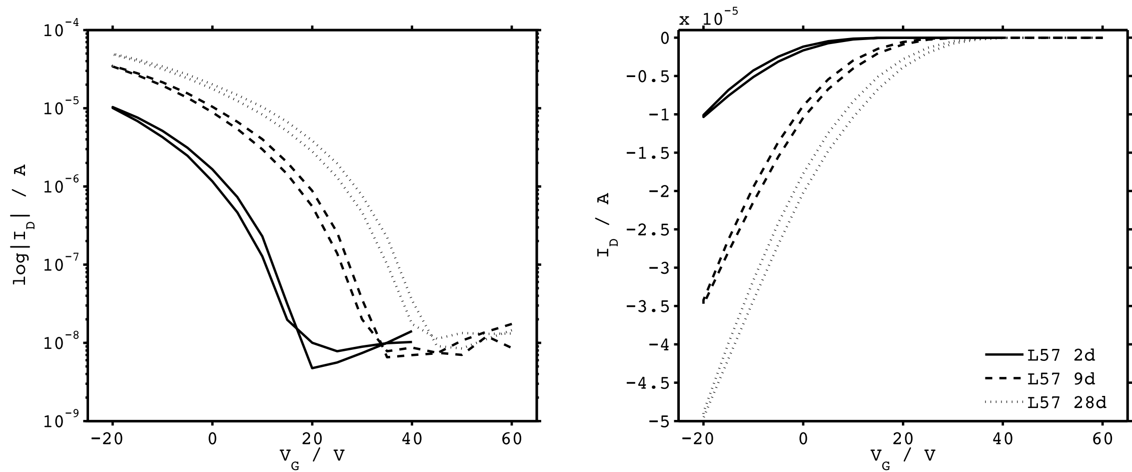


Figure 7.19: *Logarithmic and linear plot of transfer characteristic; time evolution of a pentacene device with a 5.5 nm PSSA interfacial layer; measured at -2 V drain voltage*

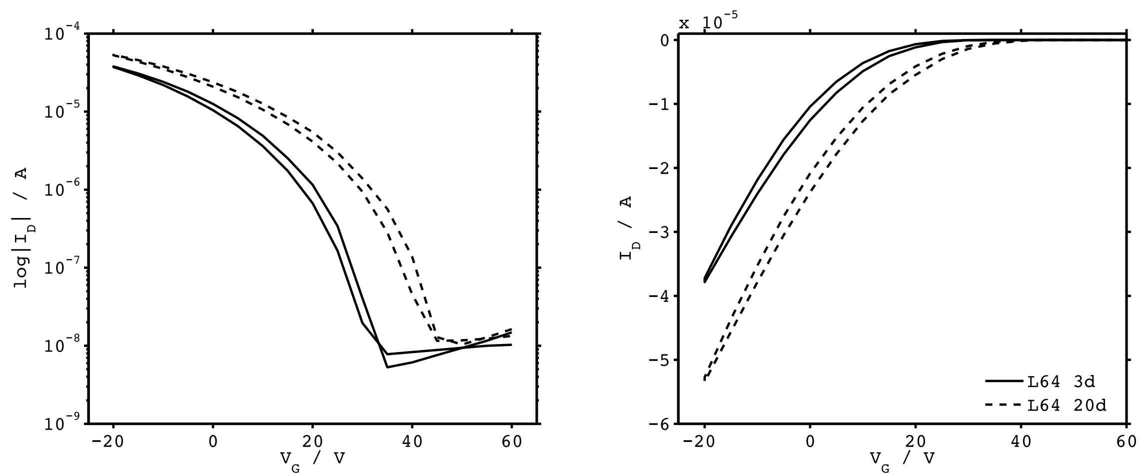


Figure 7.20: *Logarithmic and linear plot of transfer characteristic; time evolution of a pentacene device with a 5.5 nm PSSA interfacial layer; measured at -2 V drain voltage: this device shifts faster but saturates at the same* V_T *and* V_0 *values.*

Pentacene Devices with a 6.8 nm PSSA layer

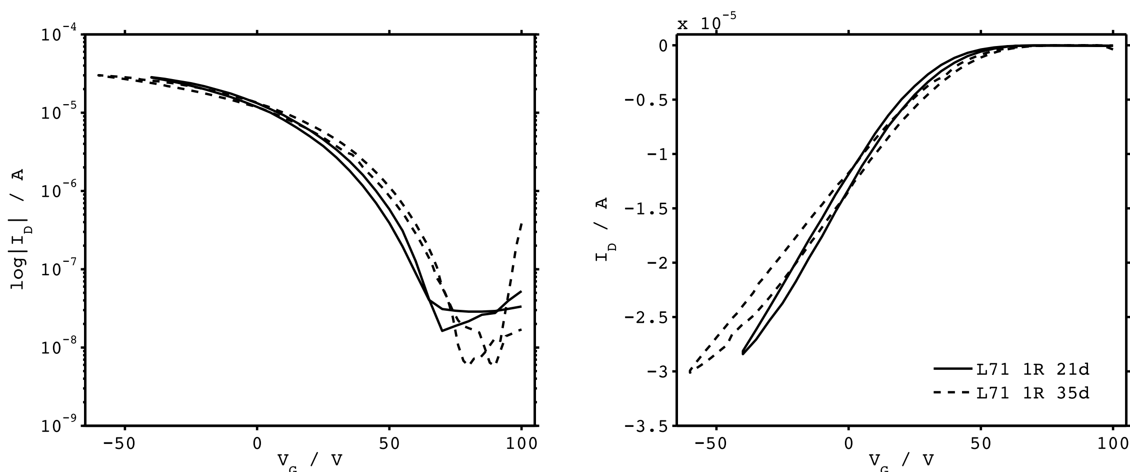


Figure 7.21: *Logarithmic and linearplot of transfer characteristic; time evolution of a pentacene device with a 6.8 nm PSSA interfacial layer; measured at -2 V drain voltage. Due to the bias stress which was observed in the badge L60-L66 this device was measured after 21 days the first time.*

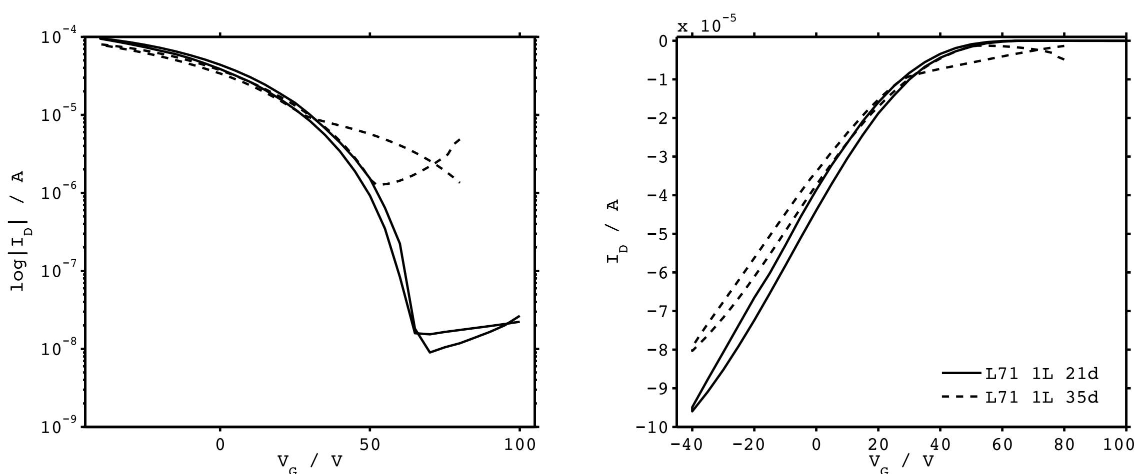


Figure 7.22: *Logarithmic and linear plot of transfer characteristic; time evolution of a pentacene device with a 6.8 nm PSSA interfacial layer; measured at -2 V drain voltage. The curve with the high off current was measured in the dark. (compare section 7.2.2.3 and references [58][40][59]).*

Pentacene Devices with a 8.0 nm PSSA layer

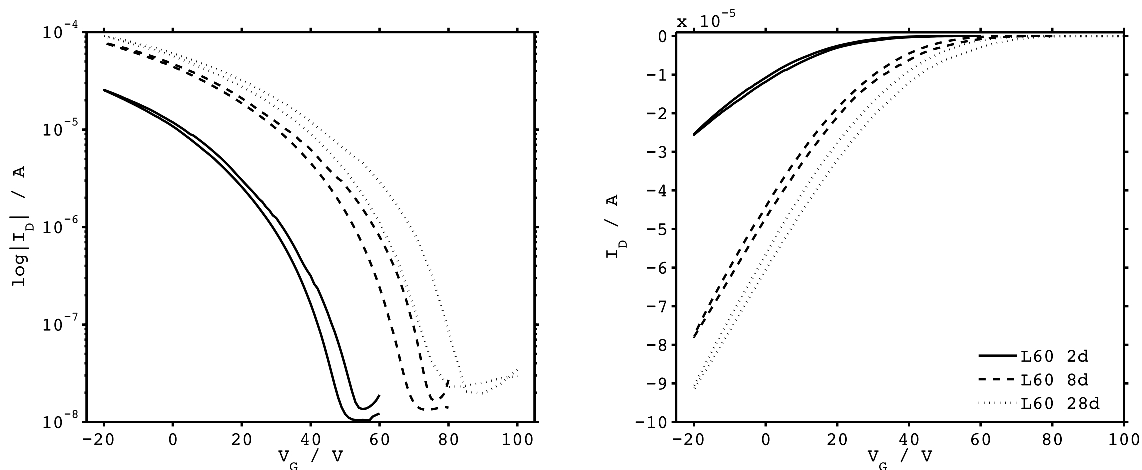


Figure 7.23: *Logarithmic and linear plot of transfer characteristic; time evolution of a pentacene device with a 8.0 nm PSSA interfacial layer; measured at -2 V drain voltage. A nearly linear shift with a slight rise of the off current indicates bulk doping*

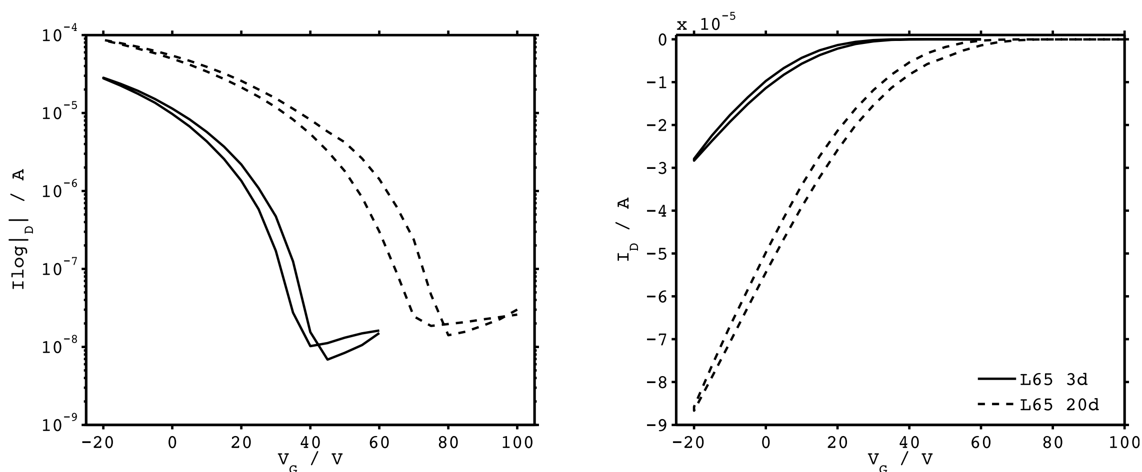


Figure 7.24: *Logarithmic and linear plot of transfer characteristic; time evolution of a pentacene device with a 8.0 nm PSSA interfacial layer; measured at -2 V drain voltage.*

Chapter 8

Measurements during Exposure to Ammonia

A threshold voltage shift due to proton transfer doping, has been shown to be reversible [44][49][56] when the devices were exposed to ammonia. Ammonia, as a base neutralizes the acid and, therefore, the space charge layer is removed. Figure 8.1 shows the transfer characteristic of a device with a 8.0 nm PSSA interface layer. Due to the acidic interface, the transistor had a threshold voltage of 40 V before it was exposed to ammonia. After the treatment, the threshold voltage is reduced to -7 V, which is even less than that of a pentacene device without interface layer.

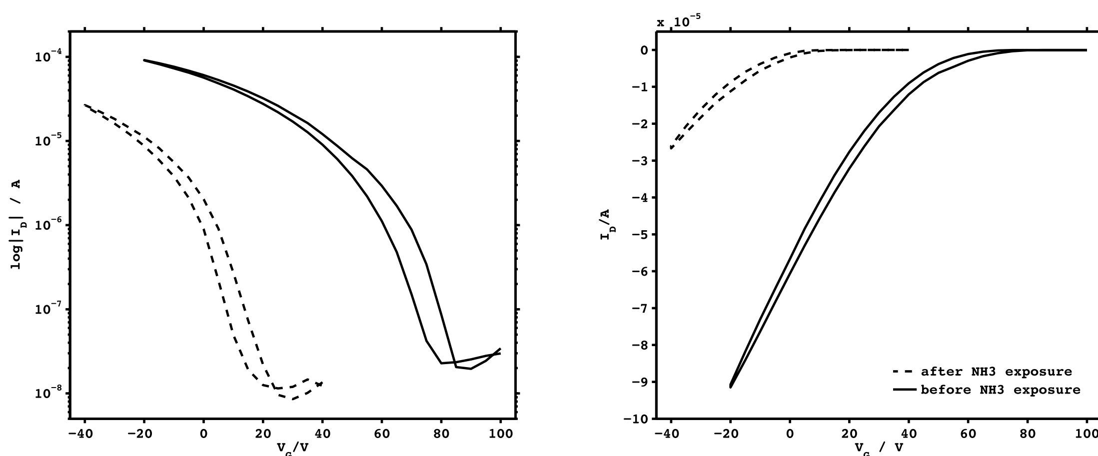


Figure 8.1: *Logarithmic and root plot of transfer characteristic of a pentacene device with a 8.0 nm PSSA interface layer: solid line - before exposure to ammonia, dashed line - after exposure to ammonia*

This feature is already well known, but not yet comprehensivly investigated. For this reason the measurement box was constructed for a characterisation of devices

during the exposure to ammonia, which enabled time resolved measurements during the dedoping phase. Harald Etschmaier[49] performed time resolved measurements on P3HT devices during exposure to ammonia in his master thesis and observed an instantanious impact of ammonia on parameters like the mobility or onset voltage.

8.1 Measurement Procedure

The basic procedure for the time resolved measurements was always the same (compare to the schematics in figure 5.6).

- The measurement cell containing the contacted devices was atteched to the ammonia setup
- The pressure of the ammonia was set to 1.5 bar and the argon to 2 bar with the pressure reducing valves.
- The tubes to the first first 3-way valves were rinsed with argon, respectively, ammonia for about 5 min in order to avoid water inclusion, the argon flow adjusted to about 90 ls^{-1} and the ammonia flow to 9 ls^{-1}
- The tube to the 3-way valve of the intake of the measurement cell was rinsed for another 5 min. After that the whole tube system to the measurment cell was mostly free of water residues.
- The valves of the ammonia and the argon tubes were closed and the valves of the cell intake and the exhaust were opened. Subsequently, the cell was flooded with argon by opening the argon valve. The volume stream usually had to be readjusted to 90 ls^{-1}
- The devices were now exposed to an argon stream. In this condition, the measurement sequence was started, which means, that from this point on the gate current and drain current were constantly measured every two seconds. A reference current was measured for about 100 s
- Subsequently the ammonia was conducted into the cell by opening the ammonia valve and simultainously closing the argon valve.
- The ammonia flow usually also had to be readjusted to about 9 ls^{-1}.
- Due to the toxicity of ammonia, the measurement cell was tested for leakage with an acid-base indicator
- About 100 s before the measurement sequence ended, the ammonia valve was closed and the argon valve opened again. The measurement was ended.
- The cell was rinsed for at least another 30 min with argon till no ammonia could be be detected any more at the exhaust.

- Afterwards all valves were closed and the cell was disassembled from the ammonia setup.

8.2 Transistor Characterisation during the Exposure to Ammonia

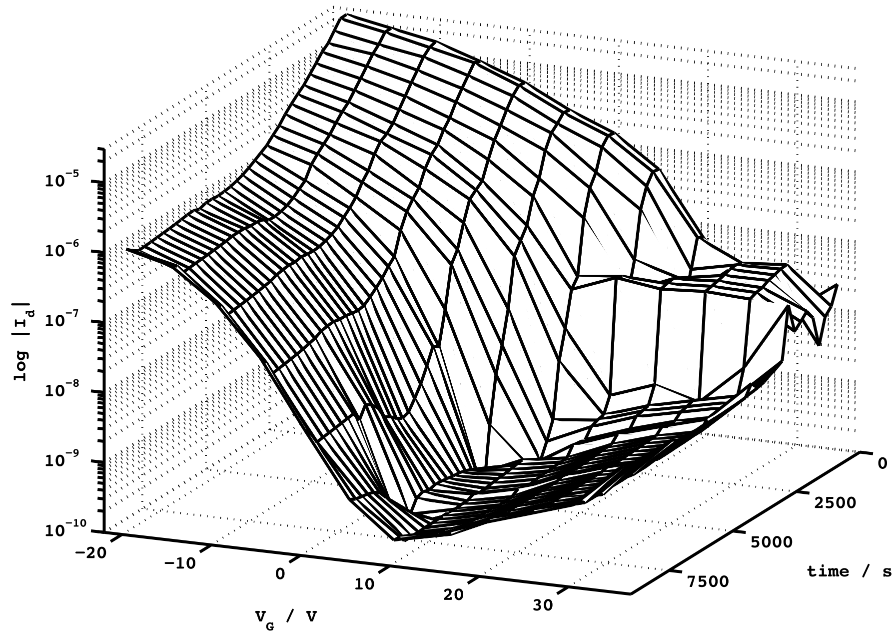


Figure 8.2: *Transfer characteristics of a pentacene device with a 1.3 nm PSSA interface layer during ammonia exposure: a continuous decrease of the onset voltage and the drain current*

A first series of measurements was made to evaluate the transistor's functionality under the influence of ammonia. Hence, measurements of transfer curves were performed every minute for half an hour at a drain voltage of -2 V during the exposure. In order to record enough transfer curves, the ammonia was dilluted 1:10 in argon gas. The gate sweep was set from -20 V to 40 V. First, a device with a 1.3 nm PSSA layer was characterized. The time evolution of the transfer characteristics on a logarithmic scale is shown in figure 8.2 and on a linear scale in figure 8.3.

It can be seen, that the device stays fully operational and threshold and onset voltage decrease continuously. Obviously, ammonia also decreases the off current, but the reason for the plateau at the beginning of the measurement is not yet understood. On the linear scale, a strong mobility degradation is visible.

The threshold voltage and the mobility were extracted for each measurement step. The result is plotted in figure 8.4 and shows the fast decrease of the mobility and V_T. The steps at 3000 s and at 5400 and 5700 s are extraction artifacts.

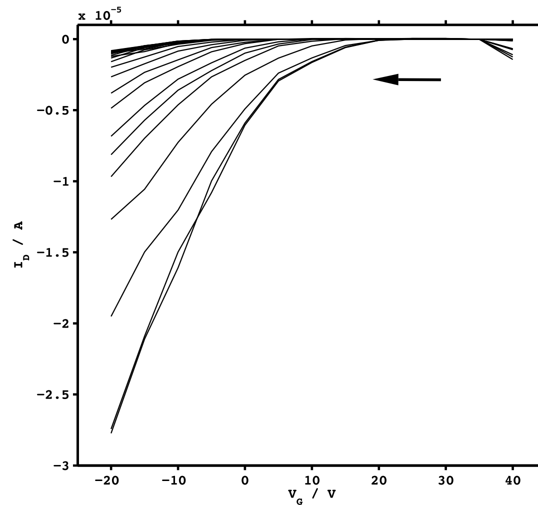


Figure 8.3: *Transfer characteristic on the linear scale of a pentacene device with a 1.3 nm PSSA interface layer during ammonia exposure: the current curve moves towards a lower voltage and the mobility decreases very fast*

The same experiments were made with a device with a 6.8 nm thick PSSA interfacial layer. As mentioned in the corresponding chapter, some pentacene devices showed a strong increase of the off current, when measured in darkness (necessarily, these measurements had to be performed in darkness). The high off current of this device with the 6.8 nm thick PSSA interfacial layer is even visible on the linear scale, as depicted in figure 8.5.

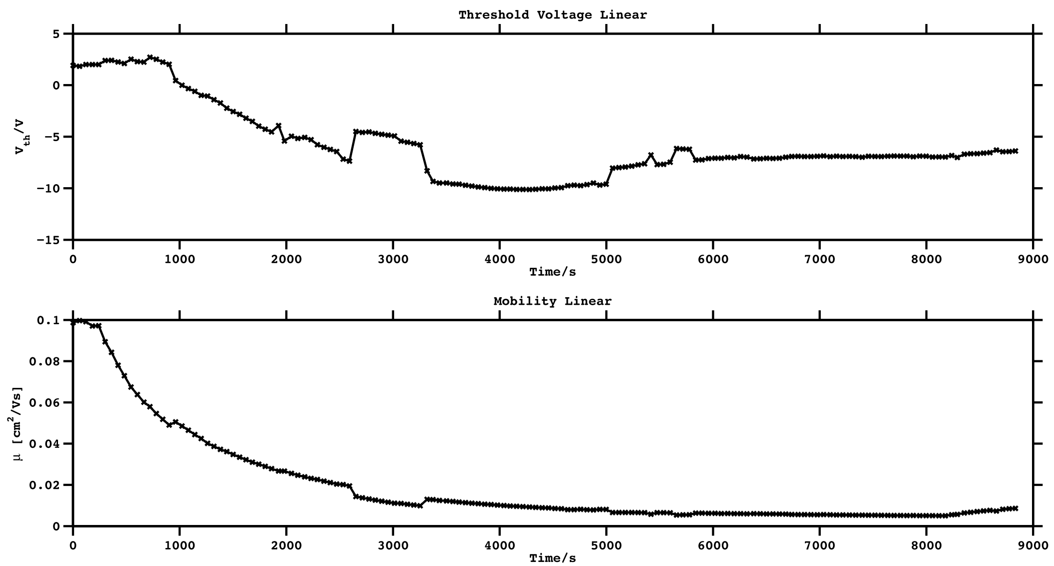


Figure 8.4: *Mobility and threshold voltage of a pentacene device with a 1.3 nm PSSA interface layer during ammonia exposure*

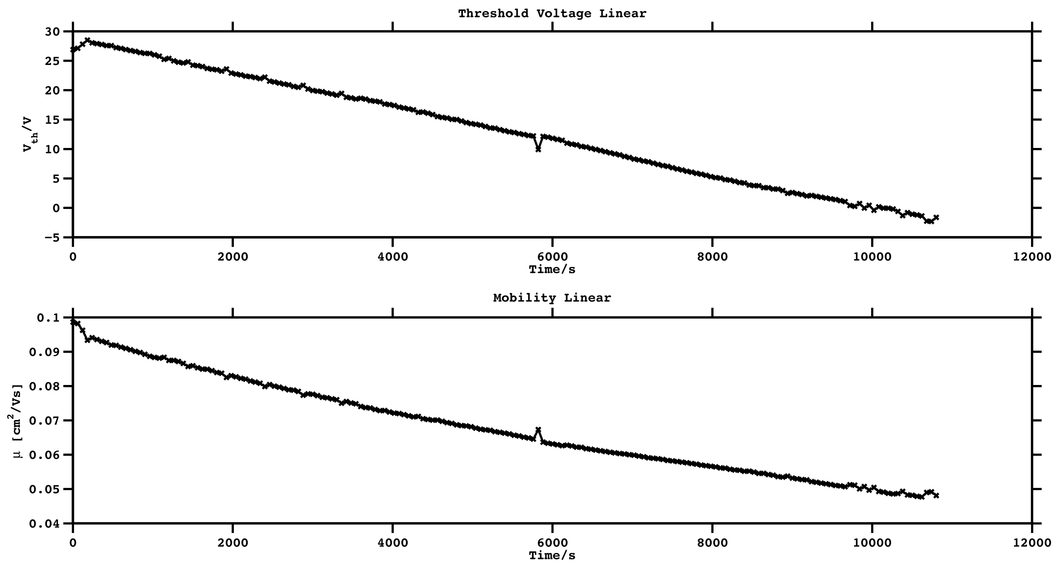


Figure 8.6: *Mobility and threshold voltage of a pentacene device with a 6.8 nm PSSA interface layer during ammonia exposure: both parameters decrease steadily*

The extracted device parameters are plotted in figure 8.6. In contrast to the device with the thinner layer, both, the threshold voltage and the mobility decrease linearly

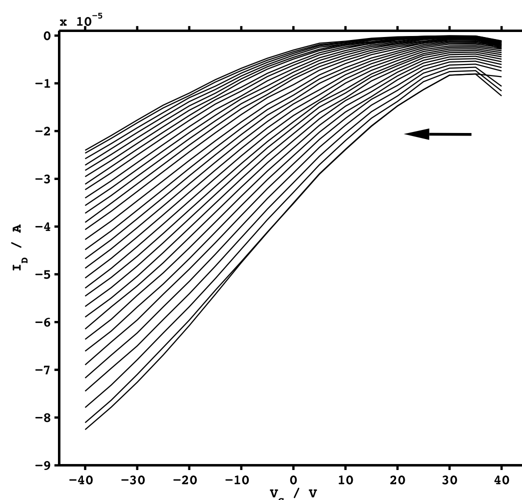


Figure 8.5: *Transfer characteristic on the linear scale of a pentacene device with a 6.8 nm PSSA interface layer during ammonia exposure: the current curve moves towards a lower voltage and the mobility decreases continuously but slowly*

with exposure time.

The previous measurements proved the functionality of the transistor during the ammonia exposure and showed, that the mobility and threshold voltage do not decrease abruptly, rather in a steady decrease. But for a deeper understanding of the dedoping process, the procedure had to be changed. The constant charging and decharging due to the transfer measuremements interfered with the drain current and gate current measurement. To be more precise, the drain current had a sawtooth pattern because of the transfer measurements, bit the decrease of the current was visible. The gate current, however was dominated by the charging and decharging currents for the transfer measuremements.

8.3 Gate and Drain Current Evolution during Exposure to Ammonia

For the previously mentioned reason the measurement of transfer lines was quitted and only the drain and gate current were evaluated at -2 V drain voltage and 0 V gate voltage.

Before the results will be presented it shall be shortly discussed, what we would have expected. Since all measurements indicate a proton transfer doping in pentacene, the dedoping mechanism is also proposed to be the same as in P3HT, like depicted in figure 8.7.

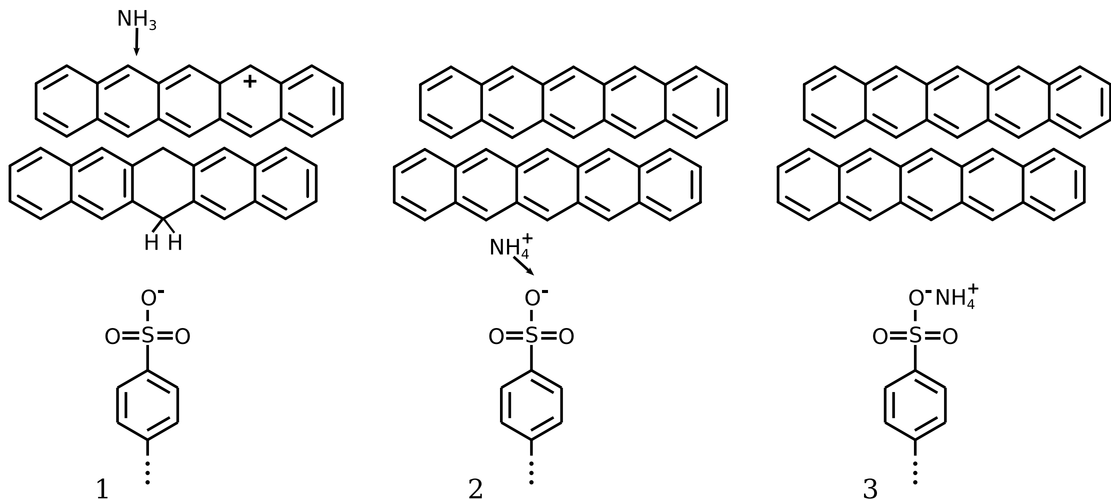


Figure 8.7: *Dedoping of pentacene by ammonia: 1- an ammonia molecule diffuses through the bulk; 2 - on the way it binds a proton from a doped pentacene molecule forming* NH_4^+*, 3 - the* NH_4^+ *reacts with the acid rest in an acid - base reaction and neutralized the space charge layer*

As discussed in section 3.7.2, the situation in the device after the acid protonated the pentacene and created a hole, should resemble the steady state of a transistor with a space charge layer. As can be seen in picture 3.10 there is no voltage drop from source to gate. Therefore, both sides, the gate and the active layer should be charge neutral.

The previously considered model of a charged capacitor due to the space charge layer had to be discarded because the charge of the space charge layer is fully compensated by the holes, created by the protons. During the dedoping process, a neutral ammonia molecule binds to a proton. The mobile hole vanishes and the negative acid residue gets compensated by the NH_4^+. It is important to notice, that the proton, which the ammonia needs to form the base, is dissociated from the acid in the doping step. Thus, also in the dedoping step, the active layer theoretically is charge neutral.

As a result of these considerations one would expect a decreasing drain current due to the vanishing mobile holes, and no relevant gate current. From this point of view, the effect can be illustrated as if the transfer characteristic gets “dragged along” the gate voltage axis towards lower voltages. Theoretically the drain current would be essentially zero, when the threshold voltage is shifted back to zero volts.

If we assume a linear decrease of the treshold voltage with the time, as observed in the device with the 6.8 nm PSSA layer (see figure 8.6), the resulting drain current would have exactly the shape of the transfer characteristic with the gate voltage axis projected on the time axis.

Indeed, all the measurements revealed a profoundly different behaviour of the transis-

tors. Figure 8.8 shows the drain current on a logarithmic scale and the gate current on a linear scale for three different devices. One is a reference device, one has a SAM interfacial layer and the third a PSSA interfacial layer. The logarithmic scale was chosen to show some interesting features.

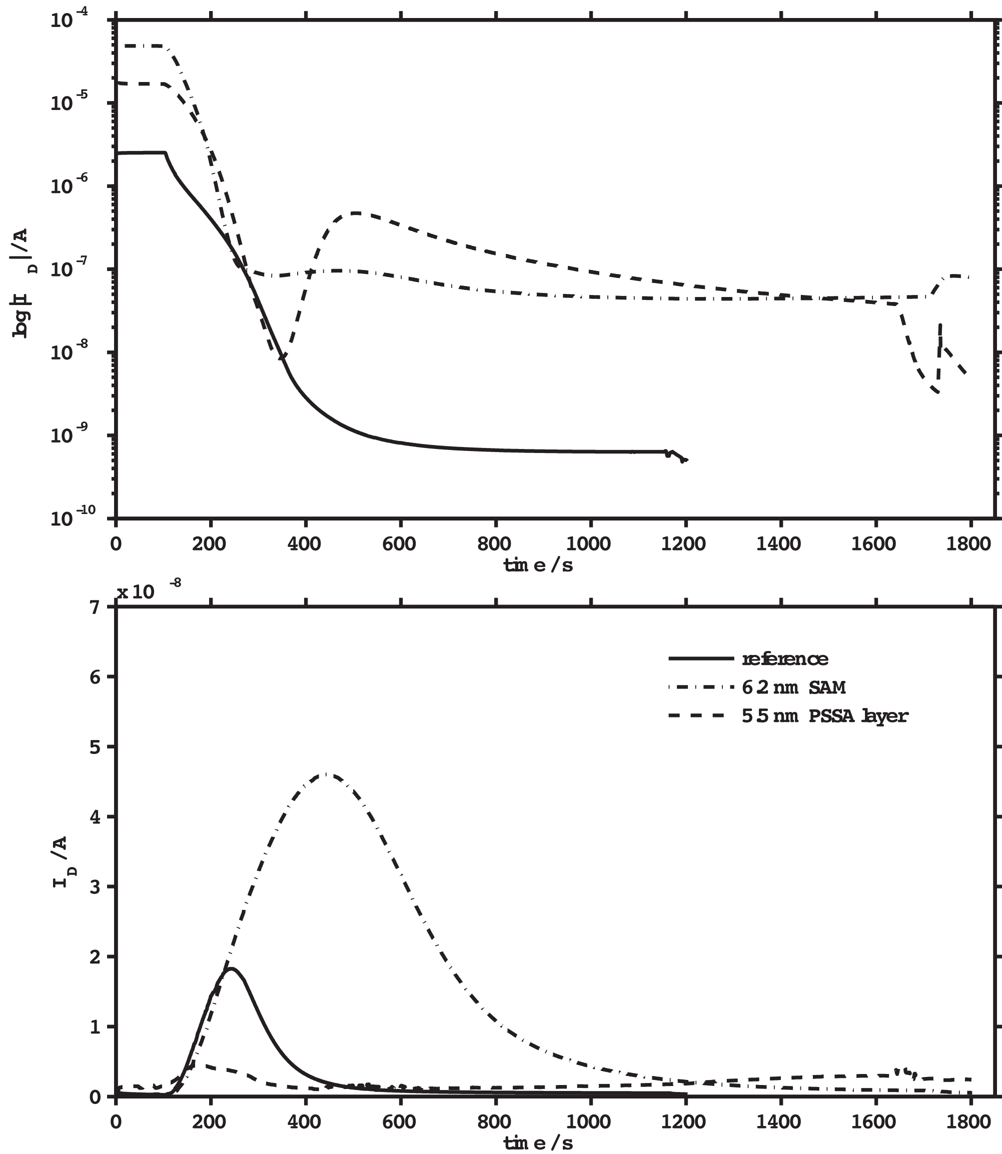


Figure 8.8: *Time evolution of drain and gate current of three pentacene devices during ammonia exposure: solid line - reference device; dashed line - device with a 5.5 nm PSSA interface layer; dash-dotted line - device with a 6.2 nm SAM;*

The most eye-catching feature concerns the device with the PSSA layer. There is a big backswing of the drain current, after a fast increase it decreases again. This feature

mainly occurs in the devices with the PSSA layers, the backswing of the transistor with the SAM is negligible small. The backswing will be discussed in more detail on the basis of more plots later on. First, the strong decrease of the drain current of the device with no interface layer and the kinks at the end of the measuremements, marked with arrows in figure 8.8 will be elucidated.

As seen at the beginning of this chapter, the threshold voltage transistors exposed to ammonia drecreases to a value which is below that of a reference device. Thus, the decrease of the drain current of the reference device (solid line) is not surprising, since small changes of the threshold voltage - if it is already around zero volts - have a big impact on the current. The decrease of the drain current of the device with the SAM interface layer (dash-dotted line) is also more or less like one would have expected. The current decreases fast but levels out at comparably high 10^{-7} A. The device with the PSSA interface layer (dashed line) also levels out at about 10^{-7} A.

However, close to the end of the measurement sequence (at 1680 s for the device with the PSSA layer, and 1720 s for the device with the SAM respectively), when the ammonia flow was stopped and the cell flooded with argon, the current of the device with the PSSA layer instantly drops more than a order of magnitude. Contrary, the drain current of the device with the SAM layer increases again. Obviously the ammonia, beside the dedoping effect has an impact on the conduction, enhancing charge transport in the devices with the polymer interface layer and reducing it in devices with SAM interfacial layers.

The different impact of the two interfacial layers on the device performance (see previous chapter) indicates that the contribution of the ammonia is also based either on the different crystal growth on PSSA and the SAM or the different shielding of the oxide from the protons. Since the effect of the ammonia is opposite for the two layer systems, the impact of the oxide is more likely causing this effect than the modulated crystal growth. A varying crystal growth would vary the result, but is rather unlikely to be able to reverse a effect.

The current characteristics of transistors with 3.8 nm PSSA interfacial layers (all devices had a comparable threshold voltage and mobility), shown in figure 8.9 feature the same drop of the current, when the ammonia exposure was discontinued. In the current evaluation of the devices with the 8.0 nm PSSA layers (figure 8.10), the measurement sequence was stopped before the cell was flooded with argon, thus, the current characteristics lack this feature. Unfortunatly there are no more clues to the character of this ammonia moderated conduction from this current characteristics. Suggestions for a further examination of this effect are given in the outlook chapter.

As mentioned before, the most eye-catching feature of the drain current concerns only the devices with a PSSA interfacial layer. As can be seen in figure 8.8(dashed lined) and figure 8.9 and 8.10 at the beginning of the measurement sequence, the current drops fast, but rises again after about 300 s, after which it decreases slowly again. The temporal differences of the onset of this current backswing is not very distinctive, since the measurement cell had to be adapted inbetween the measurements. Thus,

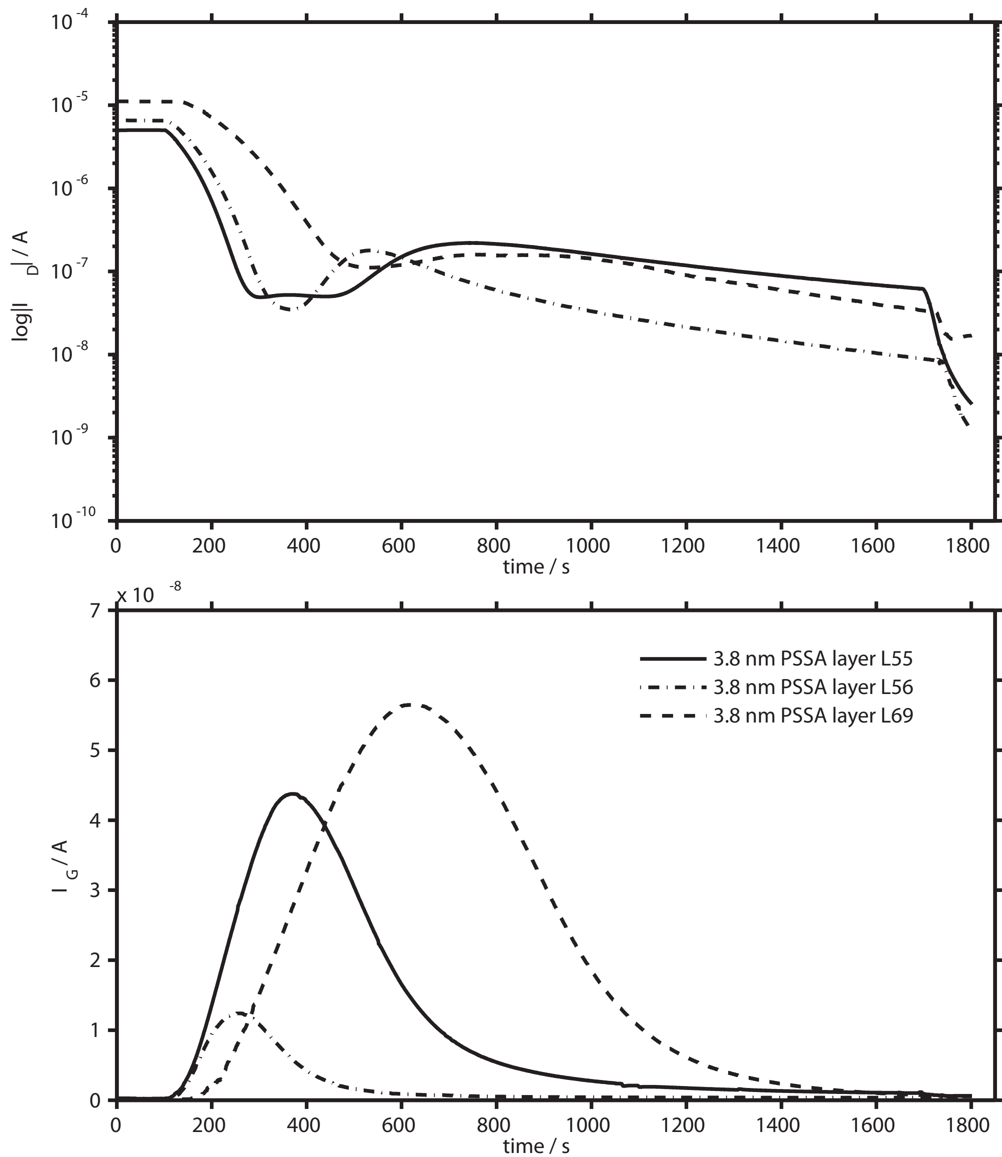


Figure 8.9: *Time evolution of drain and gate current of three pentacene devices with a 3.8 nm PSSA interface layer during ammonia exposure; The device L69 was constructed with a bottom contacted gate, in order to rule out currents between saurce and drain contact*

the ammonia flow inside the box changed, which affects the comparability of the time scales of the experiments.

The fact, that this feature only occured in devices with PSSA interface layers to this extend, lets again suppose that it is related to the oxide. Assuming there are dissociated protons trapped in the oxide, they would constitute a positive space charge layer, which would reduce the threshold voltage (which is still positive, because the majority of the

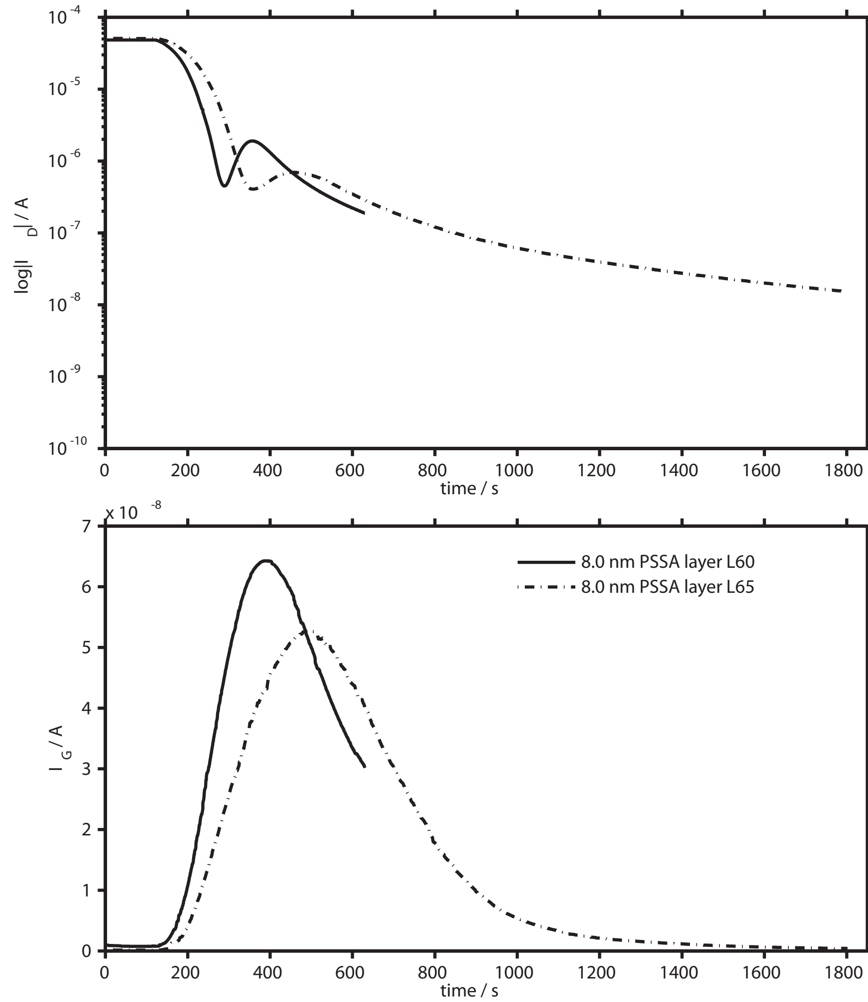


Figure 8.10: *Time evolution of drain and gate current of three pentacene devices with a 8.0 nm PSSA interface layer during ammonia exposure*

acid groups doped the pentacene). When the ammonia diffuses through the bulk it will bind the protons at the pentacene first, which results in the dedoping and the decrease of drain current. When ammonia diffuses further to the oxide it supposedly binds the protons, which are trapped in the oxide. This process impacts the devices in a way opposite to the dedoping of the pentacene. The positive space charge layer is reduced, therefore the threshold voltage and subsequently the drain current rises again. But this process is only speculation, also this feature of the device measurement during the ammonia exposure needs further investigations. Again, suggestions for further evalution of this effect are given in the outlook chapter.

The third and most inexplicable result of these measurements are the high values of the gate current. As stated at the beginning of this chapter, we expected no relevant

Table 8.1: *area - reference area; size - size of the area; charge - charge, necessary for a threshold voltage shift of 40 V; Estimation of the amount of charges to incude a threshold voltage shift of 40 V*

area	size / mm^2	charge / As
channel	0.175	$1.75 \cdot 10^{-9}$
pads	42	$4.2 \cdot 10^{-7}$
substrate	400	$4 \cdot 10^{-6}$

gate current, since the active layer is supposed to be charge neutral. Obviously this assumption is not reflected by the experiments. A current in the range of 10^{-8} A is discharged from the gate. The position of the gate current peak is always behind the fast decrease of the threshold voltage (the drain current is on a logarithmic scale, the gate current on a linear!). Obviously it does not correlate with the backswing either, since the device with the SAM shows also a rather high gate current. Possible correlations to device paramaters like mobility, threshold voltage or onset voltage were also ruled out. A shortcut from the gate to source was also checked by a change of the geometry of gate and drain electrode. This, however, did not show any impact either.

To see if the inadequat model of the charged capacitor is indeed reasonable, some estimations were made. In chapter 3.7.2 it was calulated that for a threshold voltage shift of 40 V, a space charge layer with 0.06 charges per nm^2 has to be applied, which corresponds to about 10^{-8} As/mm^2. An uncertainty for the estimation is, which reference area of the device should be used, since there is the area of the channel, the area below the source and drain pads, and finally the area of the whole substrate since the transistors work with a common gate. The charge, which is accumulated at the corresponding areas is listed in table 8.1.

So we can estimate a value of the charge, which can be discharged from the gate electrode from 10^{-9} to a maximum of 10^{-6} As. In the measurements, however, the gate current is in the 10^{-8} A range for several hundret seconds. Thus, if the view of the charged capacitor would be appropriat, the only process that ppossibly could enable a current of this magnitude is the decharging of the whole substrate by one transistor. This could be reasonable, therefore one more experimetn was made in order to clearifiy the capacitor model.

In this measurement, only the drain pad and the gate were contacted and a voltage of 0 V applied. The gate current dropped two orders of magnitude in this experiment and suffered from a very poor signal to noise ratio. Therefore, a median filter over 30 data points was applied, which resulted in a current curve resembling the previous measurments. The result is shown in figure 8.11. As expected, the integral over drain and gate currents amount to the essentially the same charges (from gate $2.4 \cdot 10^{-8}$ As and from drain $-3.1 \cdot 10^{-8}$ As) with opposite signs. But the charge is two orders of magnitude smaller than measured in the previous experiments. The fact, that the

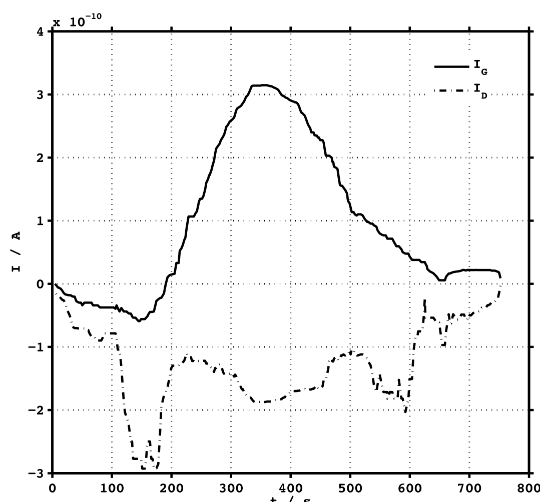


Figure 8.11: *Decharging of a pentacene device with a 8.0 nm PSSA layer under influence of ammonia; contacted as capacitor only with drain and gate*

drain voltage was reduced from -2 to zero volts can be neglected, considering that a threshold voltage shift of 40 V is equivalent to applying a gate voltage of -40 V.

For this reason, the capacitor model is also questionable from the experimental point of view. Also from the theoretical side, it would be still unclear why the capacitor would not discharge earlier. To get back on figure 3.10, not discharging would mean that the transistor never gets into the steady state but still is able to operate as a transistor.

Another reason for the high gate current could be the manifestation of a dipole layer during dischargement. The moment, the ammonia molecules bind to the protons, the threshold voltage decreases. But until they diffuse to the interface, the ammonia constitues, together with the acid residue, a diploe layer, which gets continuously smaller and vanishes after the acid-base reaction. But also this explanation is very vague.

Summarized, some of the experiments with the ammonia contradict the model of the proton transfer doping. There is no apparent explanation for this deviation. Still, there are more distinctive and better verified experiments, which prove the validity of the proton transfer doping and the dedoping mechanism, therefore there is no need to question it so far. But particularly for this reason, the measurements with ammonia require further examination, in order to get a deeper understanding of OTFTs, the doping and the dedoping mechanism.

Chapter 9

Outlook

The target of the present work was to tune the threshold voltage through varying the thickness of an acidic interfacial layer and to investigate the impact of ammonia on the devices. The outcome should have helped to understand the mechanism of the proton transfer doping and the dedoping process by ammonia. The results of the thickness variation were consistent with the latest understanding of the doping mechanism. The measurements during exposure to ammonia, however, raise some questions. Proposals for a continuation of the investigation on the impact of the layer thickness on the device and for further experiments, which would help to elucidate the results of the ammonia part, are given in this chapter.

9.1 Thickness Variation

Beside some optimization in the systematics of the measurements like the layout of the reference device and a more controlled pentacene layer, there is one key feature for further investigations. The kinetics of the proton migration and reaction with the pentacene is not yet fully understood, even though, many of the experiments made should have given some indications. Suggestions for a further examination of the reaction kinetics of the acid with the pentacene include:

Extension of the Thickness Series

The data gaps of SAM layers need to be closed first and then the thickness series of both layer types extended. One would expect a saturation of the threshold voltage shift for very thick layers, since the protons would have a limited diffusion range due to electrostatic interaction.

Extensive Examination of the Time Evolution

More different measurements should be made during the evolution of the threshold voltage shift. These measurements could include standard device characterisation including output characteristics, XRR measurments to examine a change of the oxide - acid - pentacene layer system and AFM measurements.

Simulation of the Threshold voltage shift

Drift-diffusion simulations of the device should be able to describe the the shift of the threshold voltage with time. A comparison to the experimental data would give some indications of the diffusion and reaction rates.

9.2 Ammonia Measurements

Further investigations of ammonia exposed devices are necessary to clearifiy the contradictions with the proton transfer doping.

Verification

First of all, the result of the device with the SAM layer needs to be verified, since it is the only data of a transistor with a SAM and many proposed conclusion were based on the difference between the SAM interface layer and the polymer layers.

Investigation of the Role of the Dielectric

As next step PSSA layers on top of HMDS passivated oxides should give very distinctive indications for the role of the oxide. A reference device could be included with only a HMDS layer.

Total Current Balance

With a second Keithley device, the source current could also be measured. Then one would have a complete balance of all charges, that are extracted, injected or originate from an unknown process inside the active layer, acid or dielectric. The temporal evolution of these currents could give good indications to the time scales of processes like ammonia diffusion, the acid base reaction or different trapping and detrapping rates.

It is suggested, that during the dedoping process, there are constantly traps emptied and filled (probably on different time scales). Such features could be evaluated, if anything, in an exact comparison of the currents with respect to the time. It is also conceivable, that undissociated acids have an impact, possibly redoping the pentacene or establishing a new dipole or space charge layer in connection with the presence of ammonia molecules. All these processe could only be investigated if all currents in the transistor are measured.

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