Graz University of Technology

Masterthesis

A Memristor-Based Stored-Reference Receiver for IR-UWB

conducted at the
Signal Processing and Speech Communications Laboratory
Graz University of Technology, Austria

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Abstract

Ultra-wideband communications is a promising future technology given that a robust and energy-efficient receiver can be found. Auto-correlation receiver concepts have the potential to solve this problem. This work is based on an available concept of an analog, stored reference correlation receiver using memristors for storing the reference and performing the correlation operation. Memristors are the rediscovered fourth basic circuit element. They have attracted a lot of attention recently due to the prove that the realization of such devices is possible.

In this thesis, the potential of such a memristor-based receiver has been evaluated. System level simulations have shown promising results. Therefore a circuit level design has been developed in this work. Different concepts for critical building blocks such as the required analog delay line are presented and investigated in terms of suitability and performance.

As a second part of the work, a new digital concept for a memristor receiver is presented. Even though some problems of the analog solution can be avoided, new challenges have to be solved mainly caused by the quantization noise. The potential of improved reference receiving algorithms as well as the performance of the whole system are investigated. Finally a comparison between the analog and the digital concepts is done.

Kurzfassung

Ultra Breitband Kommunikation wird als vielversprechende Zukunftstechnologie gehandelt, wobei die Entwicklung von robusten und energieeffizienten Empfängern der limitierende Faktor ist. Autokorrelationsempfänger haben das Potential dieses Problem zu lösen. Als Basis für diese Arbeit dient der bereits vorhandene Entwurf für einen Speicherreferenzempfänger. Dieser verwendet Memristoren um das empfangene Referenzsignal zu speichern und die Korrelationssumme zu berechnen. Der Memristor ist das wiederentdeckte vierte elektrische Grundbauteil, das durch den kürzlich erfolgen Beweis seiner physikalischen Realisierbarkeit große Aufmerksamkeit auf sich gezogen hat.

Die vorliegende Arbeit beschäftigt sich mit dem Potential, das dieses Empfängerkonzept besonders im Bezug auf die Realisierbarkeit bietet. Nach erfolgreicher Simulation auf Systemebene, wurden verschiedene Möglichkeiten bezüglich des Entwurfs wichtiger Bestandteile des Systems, allen voran der analogen Verzögerungsleitung miteinander verglichen.

Im zweiten Teil der Arbeit wird ein alternatives Konzept, nämlich eine digitale Lösung vorgestellt. Auch wenn damit einige Probleme des ursprünglichen Ansatzes vermieden werden können, müssen neue, hauptsächlich im Quantisierungsrauschen begründete, Herausforderungen gelöst werden. Das Potential verbesserter Algorithmen zur Speicherung des Referenzsignals wirds genauso wie die Leistungsfähigkeit des gesamten Empfängers untersucht. Den Abschluss der Arbeit bildet ein Vergleich der beiden zuvor vorgestellten Lösungen.

Acknowledgments

Foremost I would like to thank my supervisor, Klaus Witrisal, who gave me the opportunity to work on this interesting topic and always had answers on my questions and Ivan Russo for the tips with the RF design. Furthermore thanks to my family and friends for the outstanding support over the last years.

Matthias Leeb

Statutory Declaration

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

date (signature)

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1 Introduction and Motivation

1.1 Introduction

Ultra-wideband (UWB) communications has been a hot topic in signal processing over the last years as it offers new possibilities in localization and near-field communication. It gas become evident that UWB is a promising future technology at the latest when the IEEE 802.15 standard has been released. The large bandwidth of 500 MHz and more offers new possibilities to transmit data with a very high rate over a short distance. Furthermore a precise separation of multipath components is possible. This is needed in many fields of application like personal area communication (WPAN), sensor networks as well as in high accuracy positioning which make ranging, even indoor, possible. In all those fields low power and low cost are critical design aspects. In combination with the very high bandwidth, meeting those requirements is a real challenge.

While transmitters for UWB-communication are easy to implement, the practical realization of a low-power receiver is still a challenge. The specified bandwidth of the pulses in the regulation of UWB communications is 3.1 to 10.6 GHz. Due to this, a very high sampling rate is required. This is way beyond the capability of today's digital signal processing systems. So an analog or low-complexity digital solution has to be found.

1.2 Objective

To solve this problem, Witrisal [1] presents the design of an all-analog, coherent stored-reference receiver circuit for UWB applications. For decoding the received pulses memristors are used as a basic circuit component. The properties of memristive devices allows to perform complex mathematical operations as correlation in a very simple way, allowing a low-complexity receiver topology resulting in low power consumption and low cost. The proposed solution shows the basic idea and presents simulation results of such an analog receiver. However, towards a practical implementation many recent questions are left open. The objective of this thesis is to investigate those open questions by transferring the existing system-level model into a circuit-level model and as a second step to develop and investigate different solutions for unsolved problems.

1.3 Outline

After having presented a short introduction and the objective of this thesis, in Chapter 2, an overview over the theoretical background behind this work is given. First an outline of the history of the memristor is given, the fourth basic circuit element, from its discovery to the first available device and possible future fields of application is given. This is followed by some considerations about modeling memristive devices for simulation purposes. Further a summary about the motivation behind UWB communications, possibilities how to achieve high bandwidth, and finally a comparison of different transceiver architectures is given. At the end of the chapter, the test environment for the designed circuits including test vectors, means of performance measurement and reference results are described.

Chapter 3 deals with design considerations for the basic all-analog solutions, presented in the paper which this work bases on. It starts with the adaption of the high-level simulation, the transfer to a circuit-level simulation and finally design aspects for a suitable delay line and suitable switches are described. Based on the results of the chapter before, Chapter 4 is about a totally new design idea. Instead of an analog solution, all the signal processing is started with a quantization step and followed by digital signal processing. Finally Chapter 5 provides a discussion of the obtained results and persisting problems as well for the analog as for the digital solution, concluded by an outlook to possible further work.

1.4 UWB Systems

During the last decade a lot of research has been done on UWB systems motivated by the basic benefits over traditional communication systems, which are among others:

- high data rate with low transmission power
- little fading of the signal amplitude
- the ability of precise localization

In order to make use of those advantages different approaches have been made, according to signal schemes and transceiver topologies have been investigated [2].

1.4.1 Signal schemes

Ultra-wideband systems are characterized by the very high signal bandwidth of at least 500 MHz. Several different signal schemes have been presented to achieve this high bandwidth. Most popular are multi-carrier schemes and the *Impulse Radio* (IR) scheme. Multi-carrier schemes as for instance *Orthogonal Frequency Division Multiplexing* (OFDM), which is already in use for contemporary, narrow-band wireless communication systems like WLAN or DVB-T, divide the available bandwidth into multiple sub-bands with an own carrier each. The multi-carrier architecture implies some advantages as the possibility to avoid narrow-band interferences by simply not using one or more carriers in the distorted band.

Impulse Radio in contrary renounces the use of one or several high frequency carriers but achieves the desired bandwidth by using very short, typically sub-nanosecond long, baseband pulses [3]. The two main advantages of IR are first the higher robustness to multipath fading including a high accuracy to detect multipath components due to the very short pulse duration. Second the receiver architecture can be kept simpler than for multi carrier systems because no demodulation has to be performed, so no inverse Fourier transform is required. However on the other hand the baseband transmission which is keeping the hardware complexity low results in

the major disadvantage of this signal scheme. As said before the high bandwidth is achieved by very short pulses which require very fast signal processing to generate and decode the transmitted pulses.

1.4.2 IR Transceivers

As this work focuses on the design of an IR system, this short overview limits itself to this kind of transceivers. IR is a quite simple coding scheme, so the design of a transmitter is not the main challenge. The real challenge is the design of the receiver architecture. One can distinguish between three main concepts, coherent, non-coherent and auto-correlation receivers. In the sense of communications theory coherent receivers are optimal. So called *rake receivers* detect all resolvable multipath components and, in addition, must estimate the arrival time, amplitude and phase for each of the components. Since there are hundreds of multipath components resolvable in a UWB channel, the complexity of such an optimal receiver is enormous and almost not practical. Avoiding the need of channel parameter estimation is the idea of non-coherent energy detectors. Instead of estimating each multipath component, they analyze the envelope energy of the signal which allows low-cost, low-power receivers with the disadvantage of noise enhancement due to the nonlinear squaring device. The third way to implement a receiver, the one used in this work, is the auto-correlation receiver, which has the same advantages as non-coherent receivers and in addition it is also suitable for antipodal signal schemes as it correlates a reference pulse with a data pulse and therefore is independent of the channel parameters [4].

1.5 The Analog UWB receiver

Using the properties of the memristor, a concept for an analog UWB receiver has been developed and published by Witrisal [1]. Contrary to many other works proposing the concept of non-coherent receiver architectures, this concept describes a coherent receiving having the advantage of conserving the phase information of the received waveform. The idea behind this design is to exploit two properties of the memristor. First its ability to 'remember' the amount of charge that has been transferred over it which is used to store a reference pulse by setting the memristance of multiple parallel devices to values corresponding to the samples of the reference pulse. Second the ability of an array of memristors to calculate the correlation operation of a reference pulse $v(t_0)$ with the received pulse $v(t)$ by performing multiplication and summation of the N sampling points.

$$\Phi_{v(t_0),v(t)}(t) = \sum_{n=1}^{N} v_n(t_0)v_n(t) \tag{1.1}$$

The receiver architecture as shown in Fig. 1.1 consists of N equal stages, each processing the n-th part of the signal $v(t)$, sampled in the capacitors C. The receiving process has four steps. In the first step, the switches marked with '1' are closed. The reference pulse travels over the delay line and gets stored in the N capacitors while at the same time all the memristors are set to a defined initial state by connecting one terminal to V_0 and the other one to ground for a sufficiently long time. The second step (switches marked with 2 are closed) is to program the memristors by transfering the charge from the capacitors over the devices, resulting in a memristance set to a value proportional to V_{Cn}. The n-th memristance can be written as

$$M_n = R_{off}(1 - \frac{\mu_v R_{on}}{D^2} C[V_0 + v_n(t_0)]) \tag{1.2}$$

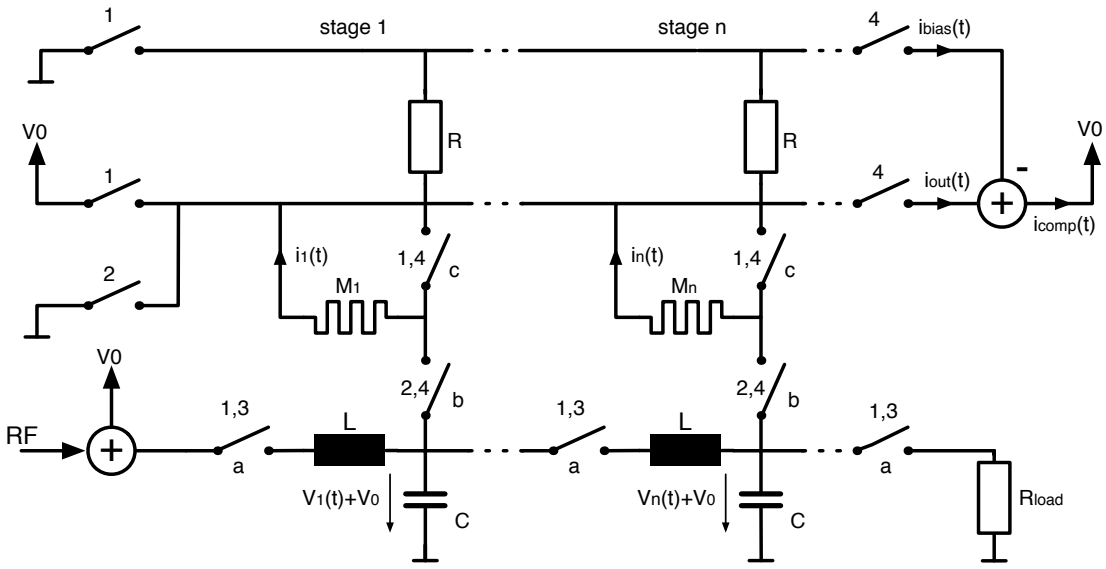


Figure 1.1: Receiver Circuit, see [1]

Next, as third step a data pulse is passed through the delay line, equal to step one. In the final step the switches marked with four are closed and the voltages $v_n(t)$ drive currents

$$i_n(t) = v_n(t)\frac{1}{R_{off}}\frac{1}{1-K[V_0+v_n(t_0)]} \approx v_n(t)\frac{1}{R_{off}}(1+K[V_0+v_n(t_0)]) \quad where \quad K = \frac{\mu_v R_{on} C}{D^2} \tag{1.3}$$

over each single memristor. By summing them up to

$$i_{out}(t) = \frac{1}{R_{off}}\sum_{n=1}^{N}[Kv_n(t)v_n(t_0) + (1+KV_0)v_n(t)]) \tag{1.4}$$

the result looks already similar to the desired correlation operation.

To get rid of the linear term the resistors R are set to $\frac{R_{off}}{1+KV_0}$ and the sum of the currents over all the resistors gets subtracted from the correlation result. The output current can then be directly sampled and used as a decision variable for the detection of the data pulses.

2 Fundamentals and Background of this Work

2.1 Memristor Basics

2.1.1 History

To understand the function of the proposed receiver, some basic knowledge about memristors and its way of operation is required. There are many papers available dealing with the details of this topic. So this chapter tries to focus on the issues which are necessary for the present work.

The four basic circuit variables voltage, current, charge, and flux are used in the definition of the three well known basic circuit elements. By putting up a table with the six combinations, the four variables offer, one can quickly see that only five of the relations are needed to describe the three existing circuit elements. So one component is missing. In the early 70s Leon O. Chua has published a theoretical work [5] on this missing fourth circuit element that described its electrical properties. However almost forty years passed until in 2009 researchers of the HP Labs have been able to build a first prototype of this circuit element [6] and thereby have proved it's existence. A nanometer thin layer of titanium dioxide is being surrounded by two platinum electrodes. One part of the titanium-dioxide layer is doped with oxygen holes and the other part is undoped [Fig. 2.1]. As soon as an electric field gets applied to the titanium layer, the dopants start to drift, the space-charge region moves and with it the conductance of the active layer changes dependent on the field's direction. So the conductance of the device depends on position of the space-charge region in the active layer. As its position is connected to former happenings, which is the basic property of memory, and as the current status of the memory is represented as a resistance, the name memristor has been chosen being a short form of memory-resistor.

2.1.2 Modeling

Even if real memristors are neither available yet nor any measurement results except of the basic proof of operation have been published yet, numerous models to describe the operation of the device have been published. Three of them will be shortly presented here. The simplest mathematical description for the behavior of the memristor is the voltage current relation:

$$v = M(w) * i \tag{2.1}$$

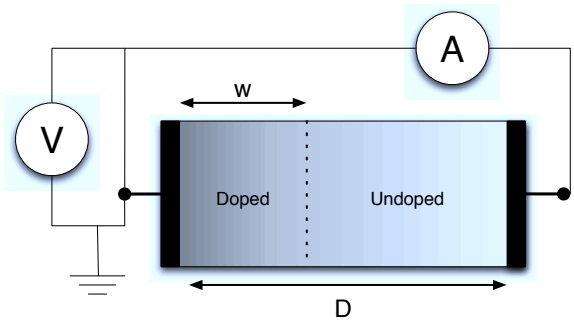


Figure 2.1: Fundamental operation of a memristor

where

$$M(w) = R_{on}(\frac{w}{D}) + R_{off}(1 - \frac{w}{D}) \text{and} \frac{dw(t)}{dt} = \mu_v \frac{R_{on}}{D} i(t) \tag{2.2}$$

While R_{off} is the resistance of the device when the 'active' area is totally undoped, R_{on} is the resistance when the size of the doped region w is equal to D, the maximal size of the region. From equation 2.1 one can see that the static behavior of this memristor is comparable to a resistor but looking at the other equations, one can easily see that the dynamic behavior is quite different. As w depends on the current over the device, the memristance changes according to the flowing current. This model is called the *model with linear dopant drift* and is sufficient for some basic considerations because it reproduces the characteristic time hysteresis behavior. However for closer investigation this model is not sufficient. One major effect that is not modeled is the nonlinear dopant drift. In the linear model already small voltages lead to quite large electric fields, which does not fit to the rules of electrodynamics. Another thing is the fact that in reality, no matter how much current flows over the device, the size of the doped region w will of course never get smaller than zero and never larger than D, which would be possible following the equations. The most used way to deal with those deficiencies, is to modify the formula to calculate $\frac{dw}{dt}$ by adding a nonlinear window function $f(x)$ where $x = \frac{w}{D}$.

Two models were chosen to show the differences to the linear version:

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{on}}{D} i(t) f(\frac{w}{D}) \tag{2.3}$$

First the model of Biolek et al. [7] who proposed to choose the nonlinear window function by:

$$f(x) = 1 - (x - sgn(i))^{2p} \tag{2.4}$$

And second the model of Prodromakis [8] et al., where the window was defined as:

$$f(x) = j(1 - [(x - 0,5)^2 + 0,75)^p] \tag{2.5}$$

Prodromakis' model has a higher flexibility because of two freely adjustable scale factors, however the so called 'terminal state problem' occurs. When the width of the doped region reaches its minimum or maximum, the window function will get zero and the model gets stuck in this state forever. Biolek's model does not have this problem but suffers from discontinuities when the current changes direction.

Recent publications have shown, that a combined integration of CMOS logic and memristors on a single chip is already possible [9], [10]. This affirms the believe that a realization of memristor-

based signal processing devices will be possible in the near future.

2.2 Receiver Modeling and Analysis

The possibility to compare the different implementations of the receiver architecture and different levels of circuit simulation is essential, so the test conditions have to stay constant. Hence the testbed and test signal presented here have been used for all the simulations performed.

2.2.1 Signal Scheme

In Section 1.4 it has been mentioned that for stored reference auto-correlation receivers a special signal scheme is necessary which will be presented here. The receiver correlates a received reference pulse with the following data pulses. As the present receiver is not able to calculate a continuous output signal but only a snapshot at the sampling time, pulse amplitude modulation (PAM) is a suitable modulation scheme. In it's easiest form as BPAM either 0/1 or 1/-1 encoding can be chosen, where 1/-1 has the advantage that 0 is a forbidden state and so works as a built-in error detection. Tab. 2.1 shows the signal parameters used for the simulations.

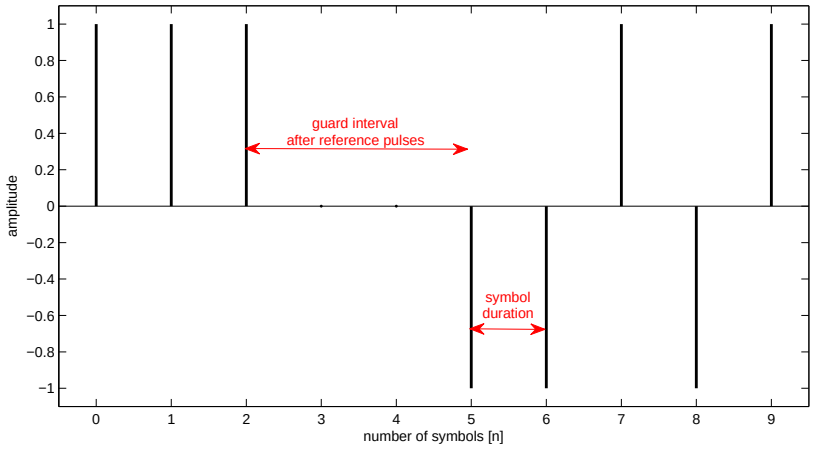


Figure 2.2: Binary Pulse Amplitude Modulation

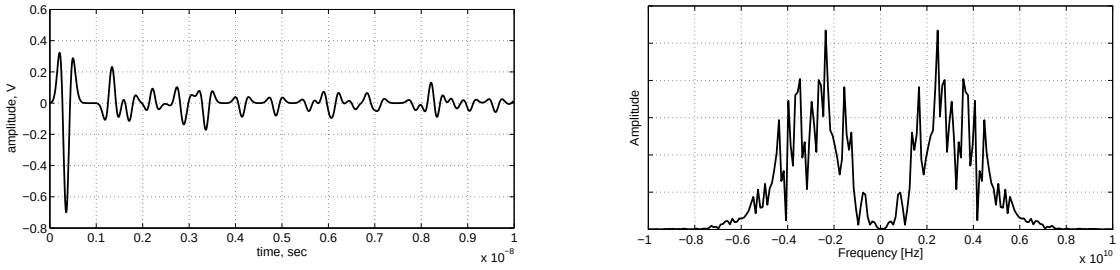
name	value	description
T	$10ns$	symbol frequency
T_s	$50ps$	typical sampling frequency
T_g	$30ns$	guard interval after reference symbol
N	100	typical number of symbols

Table 2.1: Simulation Timings

2.2.2 Channel Model

The input signal for the receiver is generated by the convolution of the presented pulse stream with the impulse response of the UWB channel. To determine the channel's impulse response,

the same channel model as in [11] has been used. Fig. 2.3 shows a sample pulse and it's spectrum which is important for the bandwidth requirements of the analog building blocks.



(a) Single Pulse (b) Spectrum

Figure 2.3: IR-Pulse and it's Spectrum

2.2.3 Measuring the Performance

In order to be able to compare the performance of the simulations , three different means of measurement have been determined.

- **number of misclassified symbols:** As shown above the data stream consists of a certain number of training pulses of the same polarity, followed by a random data stream. After the received data has been sampled the result of the sampling gets compared to the original data stream and the misclassified symbols are counted.
- **mean output levels:** For a robust sampling of the correlation result, a strong output signal is important, so the mean level of the output current at the sampled points is measured and used to determine the performance of the receiver.
- **signal to noise ratio of the sampled points:** In the ideal correlation operation, the output signal always has the same level, when the correlation result reaches its maximum. By taking the mean level of the sampling points and calculating the variance at every point, a signal to noise ratio can be determined, which is then a mean to measure the capability of the circuit to suppress noise.
- **error probability derived from the sample statistics:** Similar to misclassified symbols, the Q function also determines the likelihood that an error occurs in the detection of the data pulses. However the simple counting of the pulses requires several errors to occur which can, if the performance is good, take a quite long time. In contrary the value of the Q-function corresponds to the tail probability of the normal distribution at a certain value Fig. 2.4. In other words given a mean and a variance of the data samples, the Q-function determines the probability that one sample passes the decision border (γ) which is equal to the bit-error rate (equation 2.6).

$$P_e = Q\left(\frac{\mu - \gamma}{\sigma}\right) \tag{2.6}$$

2.2.4 Reference Results

To have something to compare the results of the following simulations to, numerical simulations of the correlation result at different noise levels should give the golden standard. In addition a bit

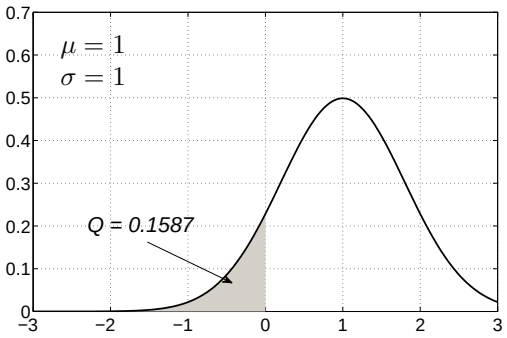


Figure 2.4: Q-function

error rate curve has been generated by using the same reference and data pulses but corrupting each with different simulations of noise. The result shows the probability of a bit error when correlating one reference pulse with 100 data pulses (Fig. 2.5). One can see that the designed receiver is an optimal receiver as it's BER curve is almost the same as the theoretical result for a BPAM decoder [12].

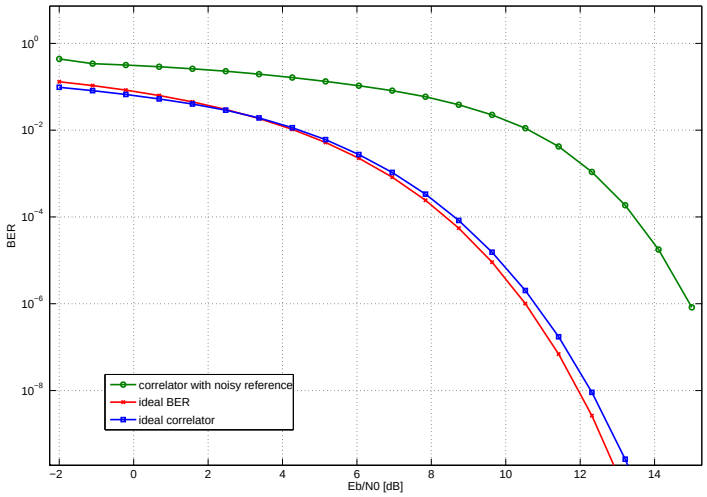


Figure 2.5: Bit Error Rate of the Ideal Correlation Result

3 An All-Analog Solution

3.1 Design Considerations

From previous work, a MATLAB simulation has been available to demonstrate the fundamental functionality of the architecture. In the original simulation some idealizations have been made, to make it simpler and easier to understand, how the circuit works. Those simplifications should be removed to bring the design closer to reality and different ways of implementation should be investigated. The rest of this section explains the simplifications that were made in the original simulation and a modification of the original receiving scheme. The next two sections give an overview of possible solutions for the switches and the delay line.

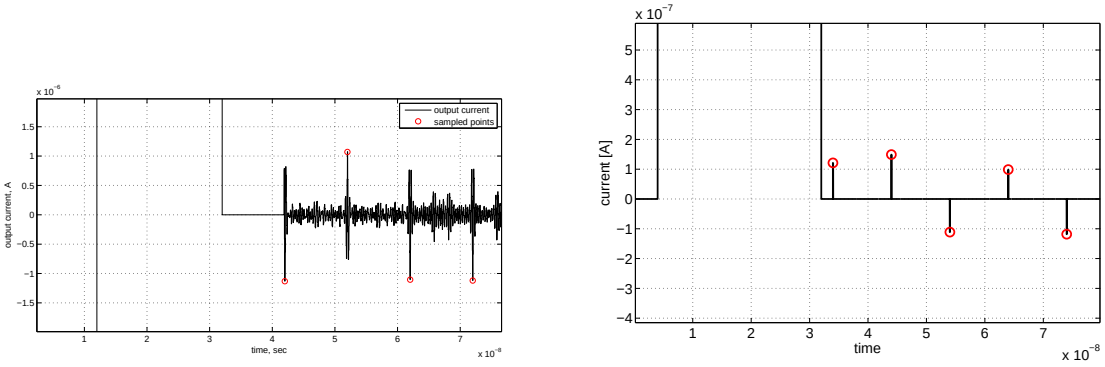
3.1.1 System Level Simulation

Fig. 3.1 shows the output current of the system including the different steps. The decoded data stream looks like a set of almost perfect correlation results. The most obvious simplification in the simulation was to neglect the fact that the capacitors get discharged. In a real circuit no continuous output signal but only short pulses of the correlation result at the peak are generated at the output, which is presented in Fig. 3.1(b). This fact shows that very good timing is essential to keep track of the correlation peaks.

To simplify the design of the missing parts of the receiver architecture, the delay line and the switches, a modification in the basic high-level simulation has been performed. As every additional stage in the sampling chain means losses, the number of stages and hence the timing has been modified. Originally the time distance between the pulses was $10ns$, sampled by 200 stages, resulting in a time resolution of $50ps$ which equals a sampling frequency of $\frac{1}{50}ps = 20GHz$, that is sufficient for resolving the defined UWB bandwidth of $10GHz$. Looking at one single pulse and its energy distribution, see Fig. 3.2 one can see that around 80% of the pulse's energy is transmitted in the first fifth of the pulse. Therefore it should be sufficient to sample just this part of the pulse and neglect the rest, resulting in reduction of the amount of required stages by four fifth to 40. Tab. 3.1 shows the loss of performance by applying this simplification.

3.1.2 Circuit Design

All the circuit design and simulations have been performed in Agilent's Advanced Design System because it combines an analog RF simulator for the simulation of the actual analog circuit and a



(a) continous (b) discrete

Figure 3.1: Continous and discrete output of the receiver simulation

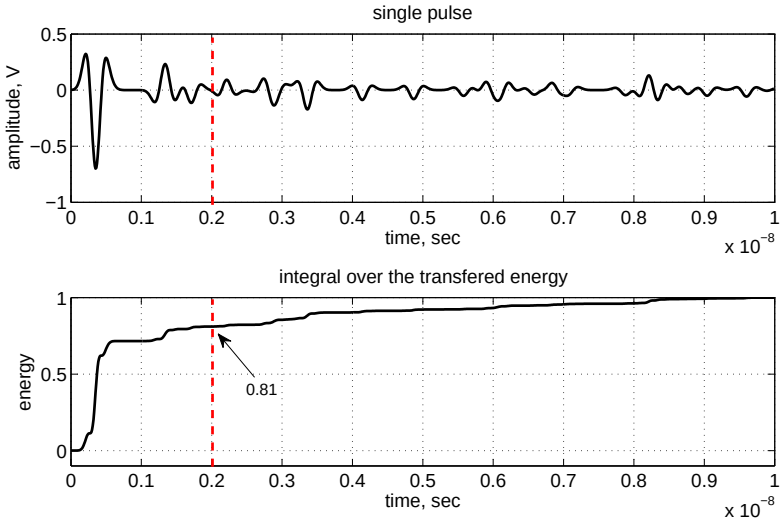


Figure 3.2: Sample Pulse and Pulse Energy

	200 stages	40 stages
mean current	$1.20\mu A$	$0.89\mu A$
SNR	19.5 dB	21.4 dB
P_e	$1.6 * 10^{-21}$	$4.8 * 10^{-20}$

Table 3.1: performance of the receiver with 200 and 40 stages

fast DSP simulator for the testbed. The aim has been implementing the whole circuit in CMOS and avoid faster but considerably more expensive BiCMOS or GaAs processes. To achieve realistic results, a suitable process technology and a fitting MOSFET models have been used. In contrast to digital circuit design, where production processes, allowing gate lengths of $32nm$ and beyond are in use, analog circuit design still sticks to 'older' technologies. For this work a $130nm$ process with a supply voltage of $1.5V$ has been selected. To model the transistors in the design, the BSIM model 3.3 [13] has been used because it is suitable for analog circuit design and has advantages in modeling transistors when using small supply voltages. Furthermore it is part of the available ADS model library. Determining the optimal dimensions of the transistors

has been done by first roughly estimating the sizes an then by optimizing through simulations rather than by putting up precise calculations.

3.1.3 Advantages of the Design

In general the acquisition and the correlation of impulse radio signals requires high precision in the circuitry to not distort the result. However the advantage of the stored reference design is that systematic errors do not influence the correlation result on condition that they are not too big and stay constant over the whole time of receiving. Those systematic errors are for example:

- delay variations between the single stages
- variations in the values of the devices (Memristors, Capacitors, ...)
- modifications in the signal due to reduced bandwidth

3.1.4 Memristor Model for the Simulation

As a very first step to set up the simulation, a suitable way of modeling the memristor in SPICE has to be found. There are several papers available proposing solutions how to model the memristor with components that are commonly available in SPICE simulators. As the memristor is a basic circuit element, it is not possible to find an equivalent circuit by only using the three other basic circuit elements. Most models like [14] and [15] are founded on the idea to have resistor in series with a controlled voltage source representing the memristor itself. In addition there is a controlling circuit for the voltage source. A capacitor in the controlling circuit respectively the amount of charge stored in it represents the state variable w. The current over the memristor is measured and charges the capacitor. The voltage of the capacitor sets the output of the controlled voltage source and with it the resistance seen from outside the circuit. Nonlinear memristive behavior can be modeled by a suitable control equation of the voltage source.

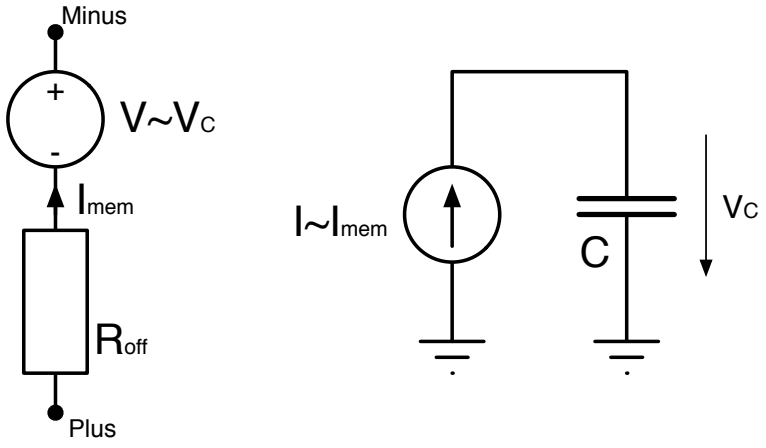


Figure 3.3: Principle of operation for a memristor spice implementation

3.2 Switches

As an essential part of the receiver, the switches in and between the receiver stages are of high importance, as their performance will influence the behavior of the whole circuit. In this section

different topologies for suitable switches are discussed and compared according to their suitability in the context of the proposed receiver.

3.2.1 Specifications

To determine the specifications, the desired field of operation has to be found first. The signal voltage in the receiving chain is always held between $V_{bias} \pm |V_{signal}|$. Simulations have shown best performance of the receiver, when the bias voltage is set to $0.3V$. In combination with the fact that the amplitude of the signal voltage always stays under $0.1V$, only the range between 0.2 and 0.4 volts is essential for the measurements of the performance.

The three places where switches are used in the circuit are for pull-up or pull-down, in between the capacitors and the memristors respectively the bias-resistors, and as part of the delay line. In the first two cases, the frequency response is not so important, due to a long setting time, but little on-resistance is essential as the switch is a voltage divider with the memristor and the bias resistor. The on-resistance should be as small as possible to transfer as much charge as possible during the guard interval of $20ns$ (phase 2 of the receiving) over the switch.

In the third case, where the switch is part of the delay line, frequency response and a good transient behavior are very important in order to distort the RF signal as little as possible. Aside that, the following requirements count for all three cases:

- high isolation to have little charge leakage over the whole bandwidth
- good transient behavior resulting in a high switching speed
- no offset voltage when turned on
- little power consumption
- simple topology and small size as they are very frequently used

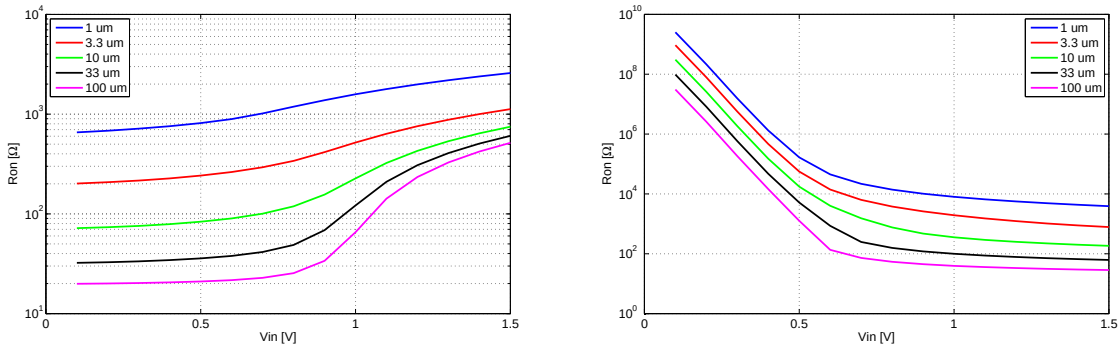
3.2.2 Single Transistor Switch (NMOS or PMOS)

Basically MOS transistors fulfill those requirements. They have a very high off-resistance, low on-resistance in the range of several hundred ohms, no offset voltage and a good high frequency behavior. The most simple switch topology in the chosen technology is a single NMOS or PMOS transistor which is switched form cut-off to saturation by a control voltages applied its gate.

This is only true, if, in on-state, the source voltage and/or the drain voltage is higher than the supply voltage minus the threshold voltage V_{th} for NMOSTs, and GND minus the threshold voltage for PMOSTs. Otherwise the switch cannot equalize the source and drain voltage. In the used technology, the threshold voltage is around $0.3V$, too high for the PMOS transistor to work properly, (see Fig. 3.4), so an NMOST is the only option for this application.

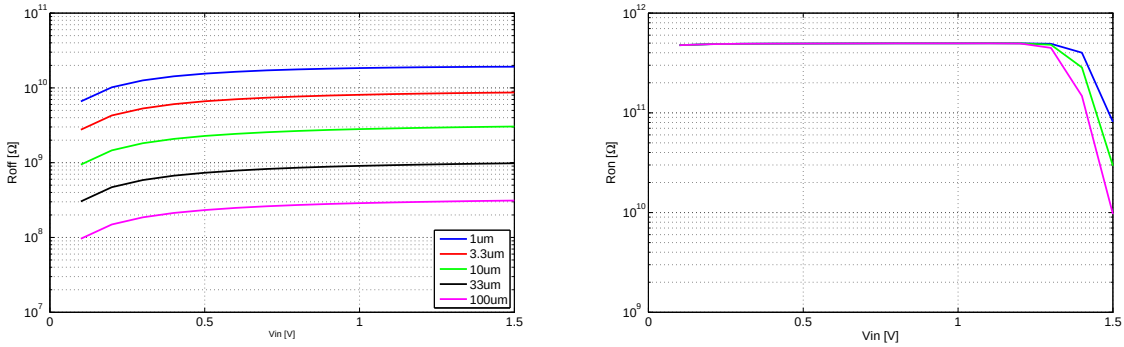
The two DC parameters on-resistance and off-resistance are controlled by the width of the transistor. They stand in contradiction to each other when looking at MOS transistors, so a good trade- off between them has to be found. The length of the switch is kept minimal ($0.12um$), first to save size and second to optimize the high frequency behavior so the scaling was only done by adjusting the width. Simulations have shown, that a width of around $10um$ gives the best performance trade off for the resistances as well as for the required space on the chip.

The size of the transistor also has influence on the AC characteristics of the switch. On the one hand, the bigger the gate area is, the larger are the parasitic capacitors and the bandwidth goes down. On the other hand, a bigger switch drives more current and increases the bandwidth of the following LC element and the amplifier stage (Fig. 3.6). Another fact, that speaks for a



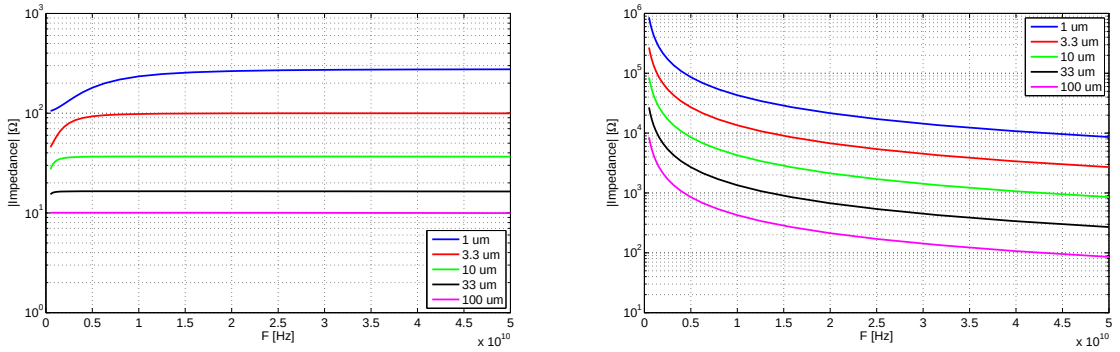
(a) NMOST (b) PMOST

Figure 3.4: On resistances (insertion loss) at DC for NMOS and PMOS transistor switches vs. signal voltage



(a) NMOST (b) PMOST

Figure 3.5: Off resistances (isolation) at DC for NMOS and PMOS transistor switches vs. signal voltage



(a) insertion loss (b) isolation

Figure 3.6: Isolation and insertion loss vs. signal frequency

small gate is that in case the gate is too big, the frequency where clock feed-through comes into play is in the range of the signal frequency.

The result for the on state is satisfying while the off state will cause problems due to the low isolation which is in the range of M_{off} of the memristors.

The big advantage of the MOST switch is the fact that in steady state, it consumes almost no

power, only while changing state, the gate has to be charged or discharged.

3.2.3 Diode Switch

A second option in this technology is the use of diodes as switches. The proposed switch consists of four diodes which are connected in pairs to Vdd respectively ground over a resistor (Fig. 3.7). The DC behavior has been measured at different resistances. The results were similar to the transistor switch with the difference that the resistances have to be fit to the level of the data signal as the signal is not free of offset. The isolation at high frequencies is better than for a single transistor however the the energy consumption is a problem. While the current over the MOS transistor gets almost zero when switched on or off, the diode switch consumes energy all the time, which is not desirable in this case.

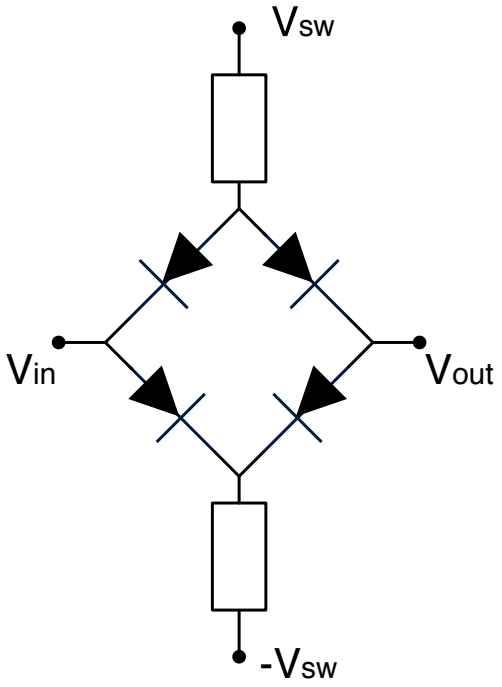
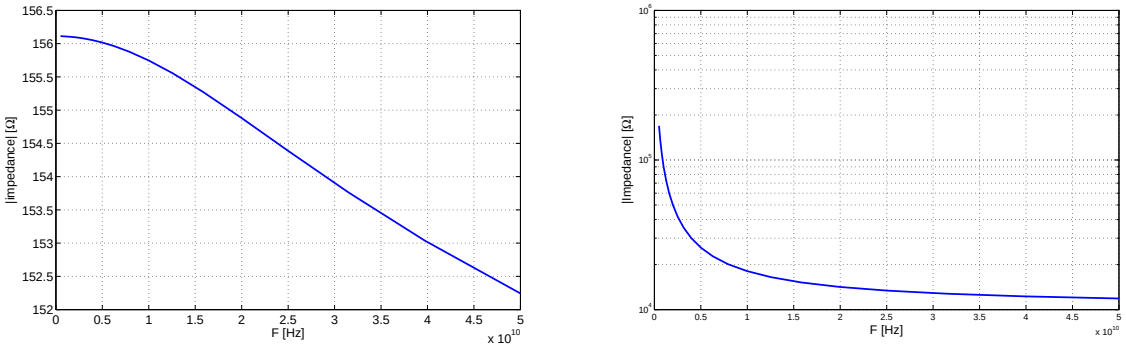


Figure 3.7: Principle of the diode switch

3.2.4 Conclusion

Except of the bad isolation at high frequencies, the transistor could fulfill the specifications, where the size of the gate is the critical parameter. The diode switch on the one hand could solve the isolation problem partly but on the other hand needs a lot of power and generates an offset voltage which has to be compensated. The final choice of a suitable switch is dependent on the rest of the system and which drawbacks are tolerable. for the following simulations, an NMOS transistor of the dimensions $L = 0.12um$ and $W = 10um$ has been chosen.



(a) insertion loss

(b) isolation

Figure 3.8: Isolation and insertion loss of the diode switch vs. signal frequency

3.3 Delay Line

3.3.1 Specifications

Aside the memristors, the analog delay line is another main part of the receiver. Hence proper functionality is essential for good performance of the whole system which results in high requirements on the design. An ideal delay line would only delay the signal by the desired amount of time independent of its frequency components or its amplitude. In addition this should happen without altering either the spectrum or the power of the signal. However, as mentioned above, the presented approach uses the stored reference principle, where all unwanted modifications of the signal are applied to the reference pulse as well as the data pulses and therefore do not severely influence the correlation result as long as they stay constant over time and in a reasonable range.

In case of the delay line, those modifications are:

- A time delay close to $50ps$ for every stage.
- Equal amplitude of the signal over the whole delay line
- Bandwidth of $5GHz$ at the minimum.

The most important parameter of the delay line is of course the time delay. In Section 3.1 it has been mentioned that the stages of the receiver should always contain a $2ns$ long piece of the input signal which should be divided in 40 samples spread by $50ps$. Small tolerances in the time delay between the stages are allowed. Next, to be able to process a UWB signal, the cut-off frequency has to be higher than the signal's highest frequency, in this case higher than $6GHz$. In connection to the bandwidth, also the amplification between the stages of the line has to be close to 1 for all involved frequencies. While a varying amplification over the whole spectrum will influence the correlation result when summing the currents up, a frequency depending amplification which is equal to filtering will make detection impossible.

The task of the delay line is to charge each capacitor to the right voltage. In case of an ideal LC-delay line this was done by simply propagating the signal through a series of LC elements. The time delay of all 40 stages is calculated by

$$Td = \sqrt{C_t * L_t} \tag{3.1}$$

where C_t and L_t are the total line capacitance and line inductance. As the delay of all stages together is $2ns$ and a single capacitor has the size of $1pF$, a single inductor must have $2.5nH$ [16] to fulfill this requirement. A practical realization of such a line suffers from continuous losses

over the whole length due to the on-resistance of the switches and the series resistance of the inductors. Fig. 3.9 shows the signal propagating over the first five stages.

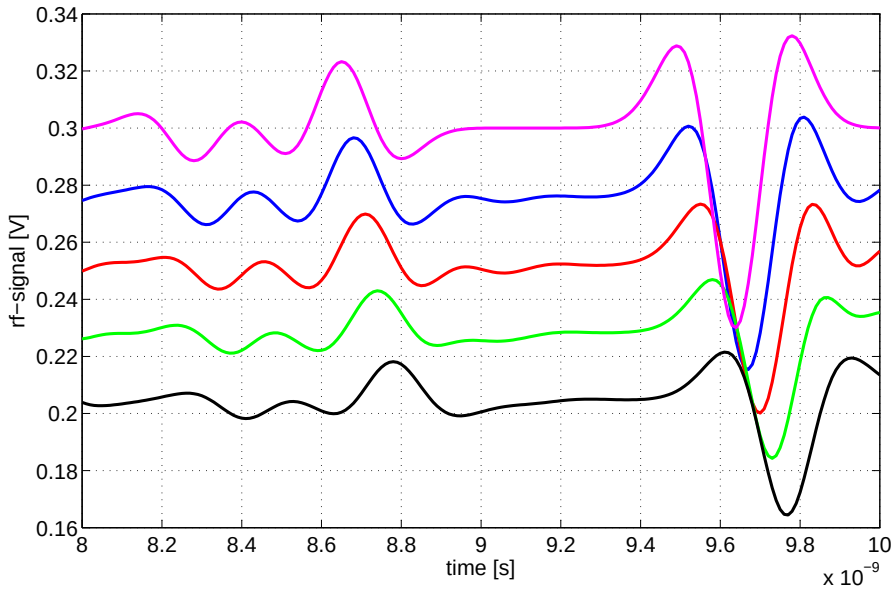


Figure 3.9: Signal propagation over the delay line without amplification

In order to compensate or avoid the losses, an active delay line is necessary. In the following, three different concepts are presented to solve this problem. The first approach is to simply put a low noise amplifier between the stages of the delay line to compensate the losses. The second idea is to avoid the analog delay line and charge the capacitors by connecting them to the input one after the other. In a third version, the first two ideas are combined. The serial delay line gets shorted to 5-10 stages connected by amplifiers and 4-8 of those modules get stacked on top of each other and switched on after one another.

3.3.2 Amplified Serial Delay Line

When the pulses propagate over the LC delay line, their power decreases more and more because of unwanted resistances of the elements of the line. Amplifiers between the stages should compensate those losses but at the same time change the signal as little as possible. Thus the desired amplifier should have an AC-gain of $A \approx 2dB$ and a DC gain of exactly 1. Its input impedance should avoid reflections and the output should be able to drive the following LC element. The input signal consists of the RF signal itself ($\hat{V} \approx 0.1V$) and a DC offset of typically $0.3V - 0.4V$. The stored reference principle would basically allow inverting amplifiers but because of the DC offset only a non-inverting transfer characteristic is possible.

Different topologies have been tried out, where the one presented here has been considered to be best suitable to fulfill the requirements. A first limiting factor is the input impedance, which has to be fit to the LC element in front of the amplifier in order to avoid reflections. For this purpose a common gate amplifier has been chosen due to it's low input impedance [17]. It works as the actual gain stage, amplifying the signal. After this first stage, a second stage, in form of a source follower, is used to shift the amplified signal back to the right DC level. Fig. 3.11 shows the input RF signal and the delayed and amplified output signal after two LC elements and one amplifier.

Adjustments in the offset and the amplification can be made by altering the bias voltages of the the PMOS transistors. The frequency transfer characteristic (Fig. 3.12) shows some losses

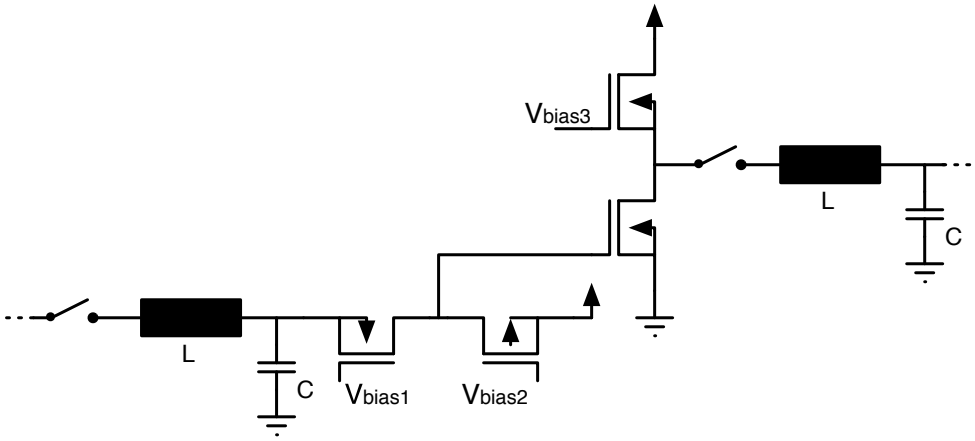


Figure 3.10: Principle of the serial delay line

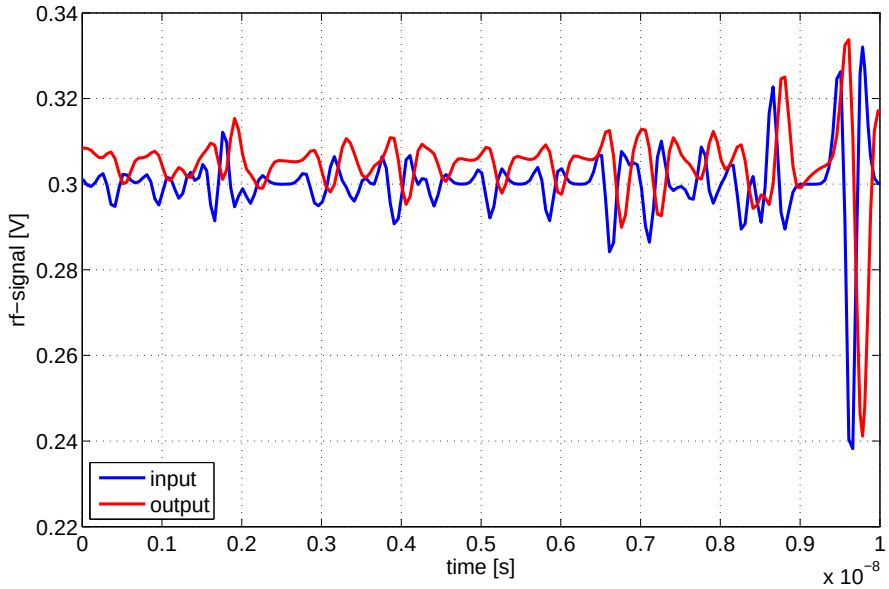


Figure 3.11: Transient simulation of the active delay line

above $3.5GHz$, which is not a problem to achieve a good correlation result for one or two stages but summing it up over 40 stages will degrade the spectrum of the signal severely.

Possible solutions would be redesign of the amplifier. The easiest change to increase the bandwidth is to reduce the transistor size and compensate the smaller gain by an advanced current mirror with higher output impedance like a Wilson current mirror. This leads to an increase of the unity gain frequency to about $4.5GHz$. Further improvement requires a different technology. Just for comparison, a BiCMOS amplifier has been tested and improves the unity gain frequency to $6GHz$ which would be sufficient for this topology.

A slightly modified approach is to have an amplifier after 5 stages of the passive delay line instead after every stage. Needless to say that the losses after stages are bigger, demanding a higher gain. The first stage is kept the same however the second stage would not give enough gain and therefor is replaced by a common source stage which should give sufficient gain. The active load of the second stage is used to add the right amount of offset and set the DC level

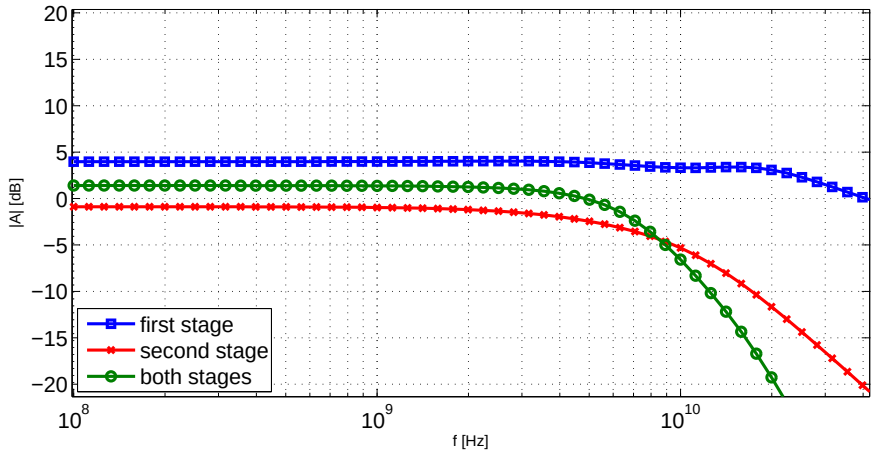


Figure 3.12: Frequency thransfer characteristic of the two stage amplifier

correctly. Fig. 3.13 shows the result of the transient simulation where the caractaristics of the signal are still visible but some unwanted reflections as well. Fig. 3.14 shows the AC transfer characteristic of the used amplifier in the BiCMOS version. In comparison with Fig. 3.12, the gain of the second stage has been severely increased. in addition the unity gain frequency of the whole amplifier is now about $1.5GHZ$ higher.

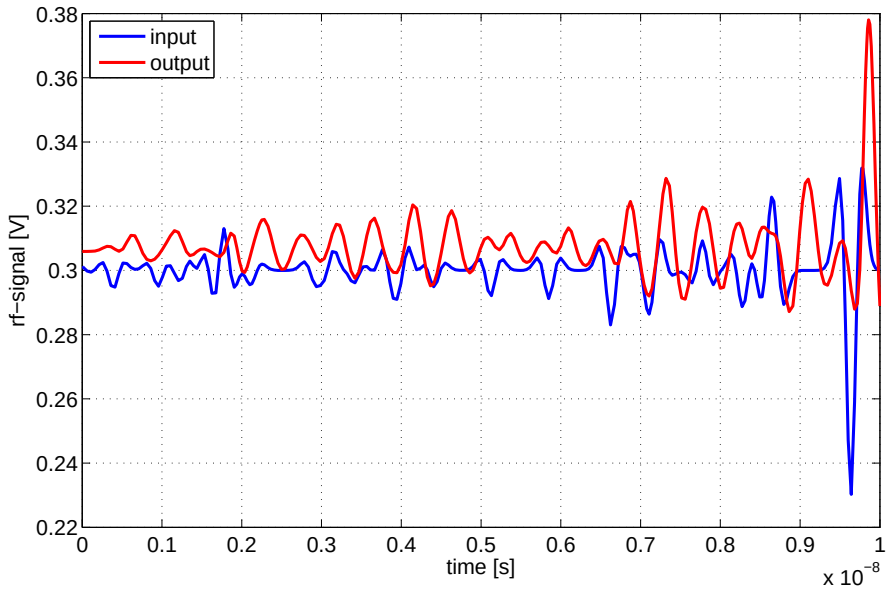


Figure 3.13: Transient simulation of the delay line with 5 stages per amplifier

It has been tried to simulate the full delay line with stages and an amplifier each. Even if ideal components with no tolerances have been simulated, it was almost impossible to keep the gain close to one. Already a small variation in the gain makes the whole system unstable.

3.3.3 Parallel Charging

As mentioned above, in this solution the signal does not get processed through a delay line but the capacitors get charged by connecting them to the input signal one after the other by turning

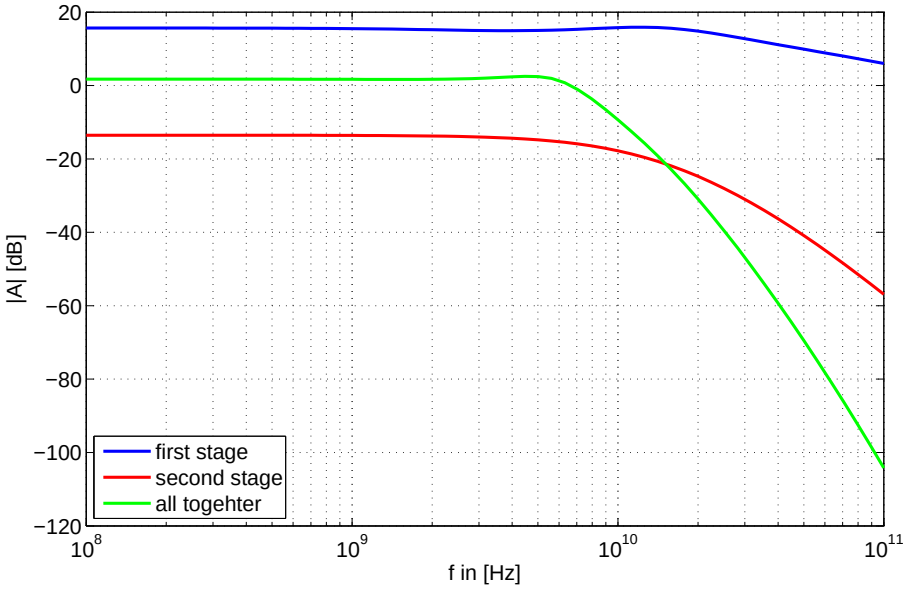


Figure 3.14: Frequency transfer characteristic of the BiCOMS CS stage

on a switch in front of each, see Fig. 3.15, similar to a sample and hold circuit. This transfers the delay line problem from the signal path to the control of the switches, which is assumed to be way easier as no analog signal has to be delayed but simple, binary pulses for turning the switches on and off.

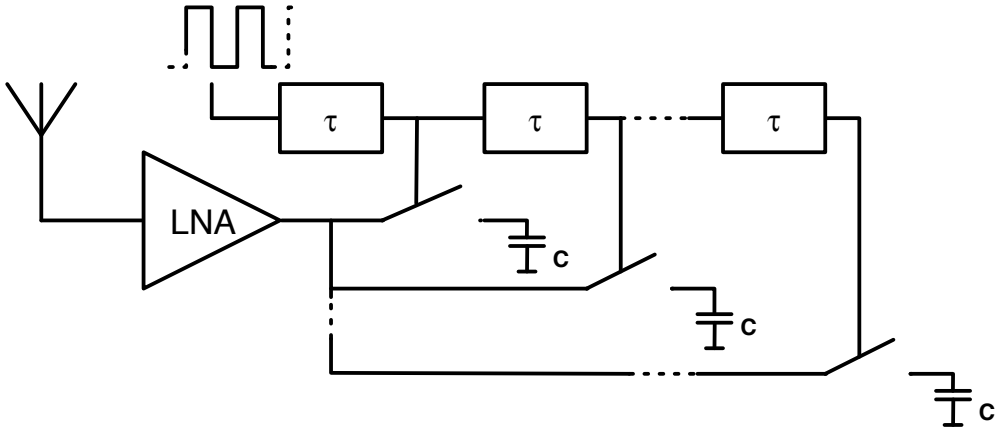


Figure 3.15: Principle of the parallel delay line

For the delay of the switching signals, a series of inverters has turned out to be most suitable. Always a pair of inverters is between two switches and set up to realize a delay of the desired $50ps$. Fig. 3.16 shows the principle of sampling with three parallel samplers. First the samplers follow the signal until the switches get opened one after the other with a time delay of $50ps$

In the ideal case, the switching pulse would also have a length of $50ps$, whereby only one switch is turned on at the time. However as the circuit works like a sample and hold element, it follows the voltage until the end of the control pulse. Simulations have shown that so short pulses cause problems to send them through the digital delay line and prolonging the pulse duration to about the double reduces this effect. The critical points in this line are first the inverters as they have

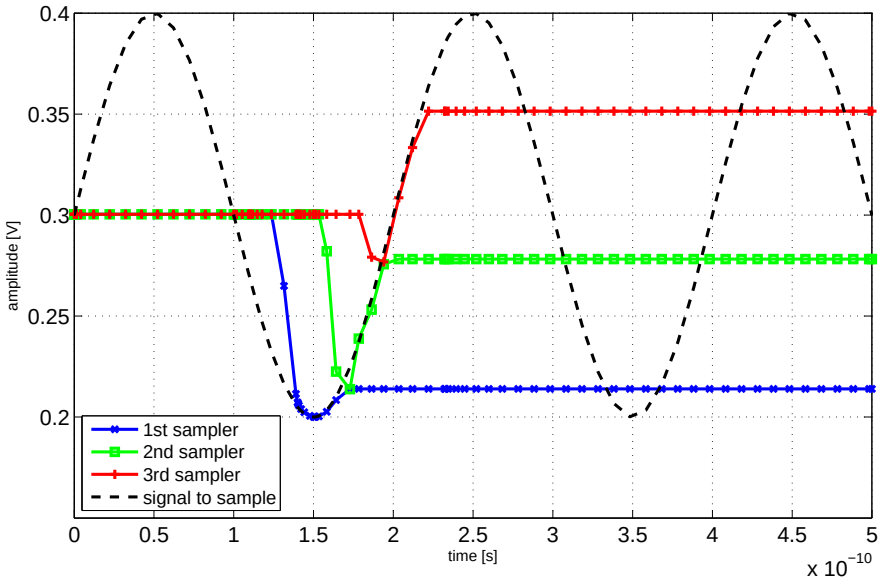


Figure 3.16: Sampling of a sinusoidal signal by three parallel samplers

to drive the switches in front of the capacitors and second the resistance of the switches itself as this factor limits the charging time of the capacitors. Assuming an ideal LNA, the maximum resistance to achieve a sufficiently high cut-off frequency of $6GHz$ is

$$f_{-3dB} = 6GHz = \frac{1}{2\pi RC} \rightarrow R_{max} = \frac{1}{2\pi f_{-3dB} C} = 26.52\Omega \tag{3.2}$$

which is approximately 4-5 times lower than the resistance of the tested switches. Possible solutions would be either to reduce the impedance of the switches by taking several transistors in parallel, which increases the required current, the delay line has to drive. Or, it would also be possible to make the capacitors smaller in order to decrease the time constant, as they do not influence the time delay like in the solution before. However the charge stored will then be smaller, which decreases the dopant drift in the memristors and thereby influences the correlation result negatively. An advantage of this solution is the fact, that no inductors are used. In integrated circuits it is preferable to avoid inductors if possible due to high costs caused by the big area they occupy on the chip.

3.3.4 Combined Delay Line

The conclusion of trying to realize the serial concept is that finding a suitable amplifier topology and fitting it's parameters to achieve the right amount of gain and offset is very difficult. Further the robustness of this delay line solution is not very good. Already a small change in one of the amplifier stages, severely influences the performance of the whole system as the operation point has to be set exactly because an error will propagate through the whole line which makes it not suitable for a practical realization. This is the reason, why the two other concepts have been developed. The stack of sample-and-hold elements basically works given the fact that the control signal for the switches is of good quality.

This third approach combines the first two concepts in order to exploit their strengths and compensate their disadvantages. The idea is to divide the whole line into several blocks of serial delay stages with amplifiers in between them. As the concept of one amplifier after several stages turned out to be the better solution this concept has been used. Those blocks are put in parallel

and switched on one after the other to spread the signal over the line (Fig. 3.17).

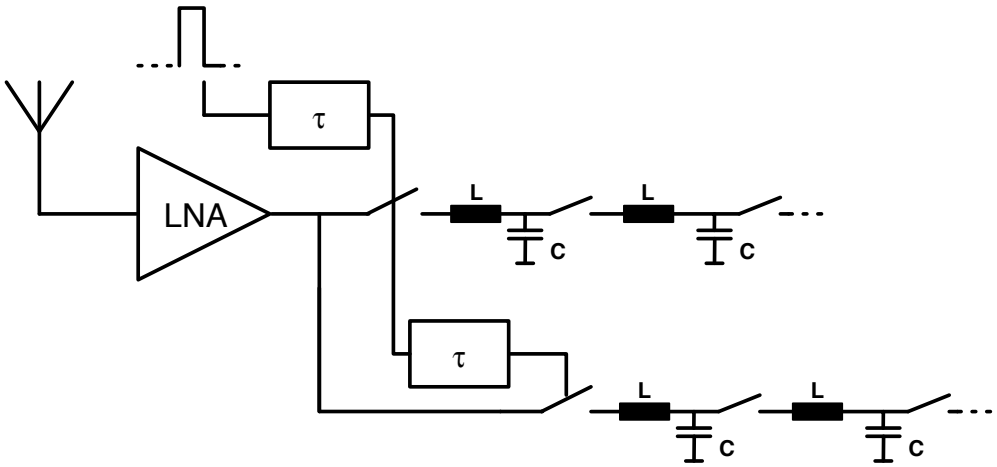


Figure 3.17: Principle of the combined delay line

3.3.5 Summary

As already mentioned, using a series of amplified delay stages is not very stable and does not allow to build a robust circuit with reasonable effort. A set of simple, parallel sample-and-hold circuits totally avoids those problems. However, new challenges occur as the digital delay line has to drive the switches fast enough and the single sample-and-hold stages have to follow the RF signal fast enough. A combination of the first two approaches could be a solution but is still not ideal. The use of inductors is not preferable in integrated circuits and reaching the required bandwidth when taking all undesirable side effects into account will be challenging.

4 A Digital Solution

4.1 Idea

The results of the first part of this work show significant challenges in the realization of essential parts of the circuitry, especially the delay line. Due to that a new idea has been born with the goal of simplifying the delay line as much as possible. Instead of processing an analog signal with high precision through the line, it would be way easier to use a digital one. However this contradicts to what was said in the introduction, that conventional digital signal processing systems are not fast enough to be used in this case. Hence a very simple analog-to-digital converter and a very simple delay line have to be designed to meet the speed and the bandwidth requirements. The most simple quantizer one can think about is a one-bit quantizer. It has the big advantage of being very simple to implement and being fast, fast enough for this application. However it has the drawback of introducing a very high quantization noise which can make a robust detection impossible. In the following chapter, possible solutions on how to deal with this high noise and how to make detection robust anyway are presented. This is followed by simulation results and in the end of the chapter comparisons with the ideal case and the analog version are be made.

4.2 Sampling

A high accuracy of the stored reference signal is very important for a high quality of detection. To achieve a higher accuracy with only a threshold quantizer, two different techniques were applied. Both are founded on the concept of sampling the reference pulse multiple times to gain new information out of it every time.

4.2.1 Swept Threshold

To easily sample an input signal with one bit resolution, a comparator is the device of choice. Usually the threshold of the comparator is set to a fixed value as ground or $\frac{Vdd}{2}$ which gives a simple one-bit sampling. To get a higher resolution with only this one comparator, the same concept as in flash analog to digital converters (ADC) has been used with the difference that in this case the sampling happens not in parallel but serially by sampling the same input several times with different thresholds of the comparator. So while for example for a resolution of 4

bits in a flash ADC 2^4 comparator stages are necessary, this system only needs one stage which means a huge reduction in complexity with the drawback of needing 2^4 steps to do the conversion. Fig. 4.1 In order to be able to combine the different sampling results a counter is necessary to save the sampled bits. Instead of a digital counter, in this work, the memristors are used as analog accumulators by changing their memristance to values corresponding to the output of the comparator. As the memristance decreases with the amount of charge transferred over the device, it will be inverse proportional to the sampled signal. This works perfectly until the amount of noise is bigger than the distance between the thresholds. Then the quality of the detection decreases.

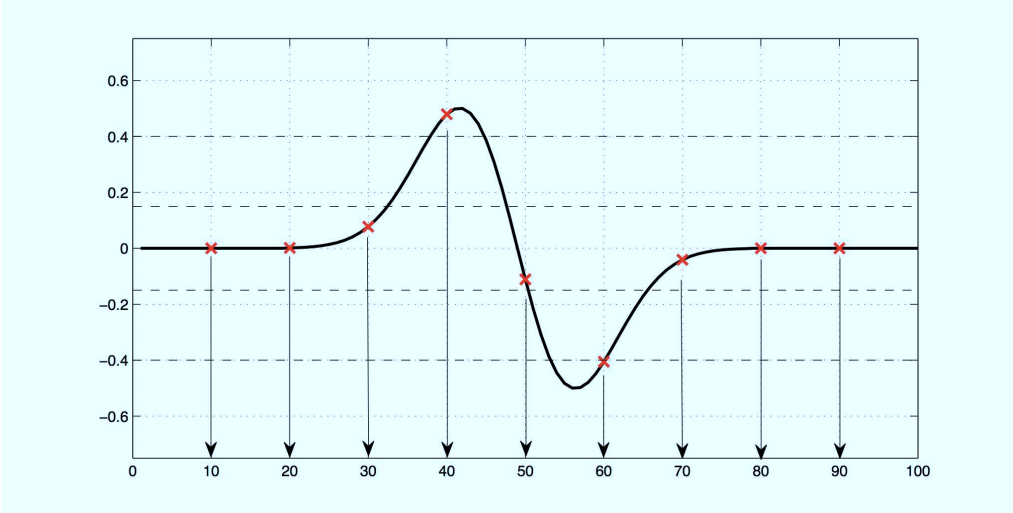


Figure 4.1: Principle of swept threshold sampling

4.2.2 Stochastic Resonance

Swept threshold sampling works well for signals with a high SNR, which will be shown later Section 4.4. To increase the performance of the sampler for noisy signals, a new method has been chosen. Stochastic resonance (SR) is usually understood to be a method to permit the detection of a weak signal by a digital sampling system, where weak is assumed to be equivalent to subthreshold. In that case noise helps the signal to overcome the threshold and allow detection even though its subthreshold property. For suprathreshold signal this effect totally disappears. However the assumption that this effect disappears in suprathreshold signals is only valid for single threshold sampling systems. In multithreshold systems an effect called suprathreshold stochastic resonance (SSR) comes into play. In this case multithreshold does not mean several different thresholds as before but that the same signal corrupted by independent noise is sampled several times, where the thresholds of the samplers can be the same. SSR helps to reject the unwanted noise in a communication signal on the one hand and on the other hand to increase the performance of a one-bit sampler by adding more degrees of freedom and by that generating information. The following example should help to demonstrate the effect: As a sample pulse

a first-order derivative of a Gauss curve is used and as detector a simple one bit thresholder. Independent of the amount of samplers, as long a no noise is present, only the positive peak can be detected. Only the sampling of a noise corrupted pulse (in this example $\sigma = 0.2$) can detect it's true shape. Assuming to the amplitude of the sample, the added noise gives a certain probability for it to overcome the threshold or not. For the first value -0.07 at $t = 30$, the probability to be above the threshold is 34% So when performing 100 measurements the counter should be 34 while for the second value -0.4 at $t = 60$ the counter is only 2, as 98% of the samples is 0 (Fig. 4.2). Assuming that the amount of samplers is sufficient, the signal can be perfectly detected.

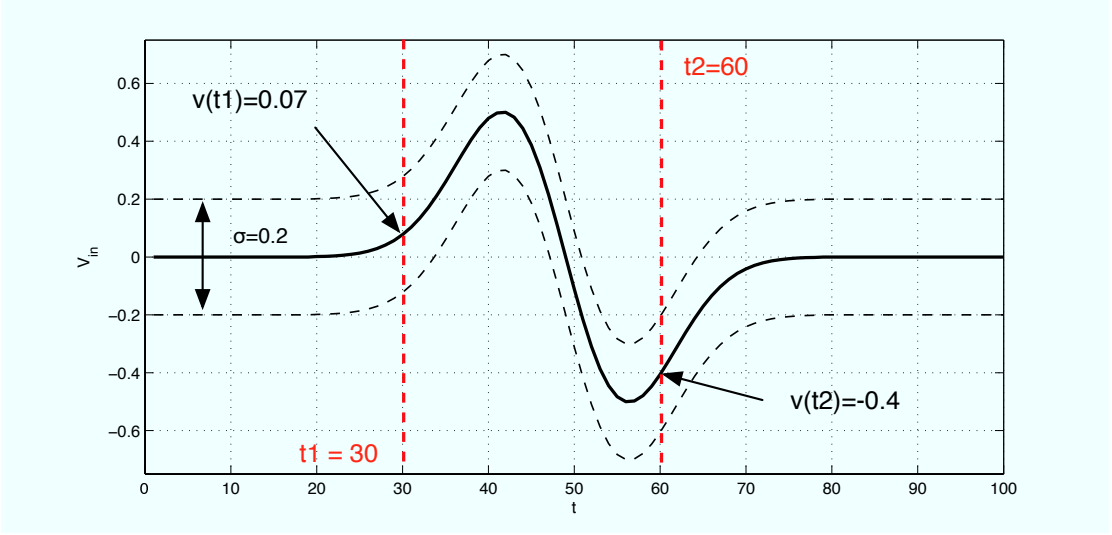
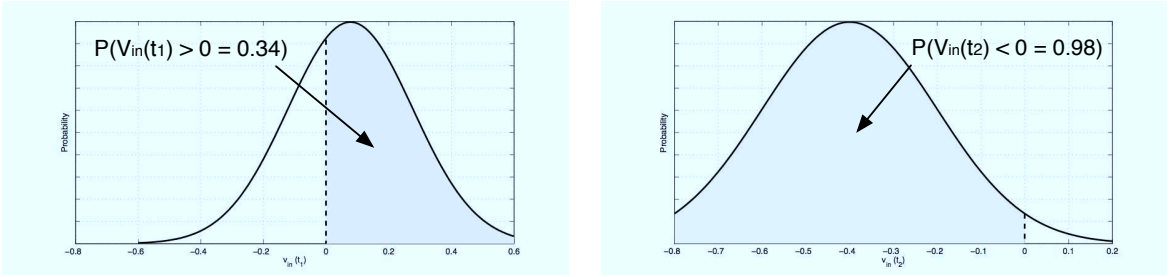


Figure 4.2: Example pulse for SSR



(a) t1 (b) t2

Figure 4.3: PDF at two example sampling points

4.2.3 Hybrid Sampler

To combine the qualities of both presented sampling methods, good performance at low noise levels with swept threshold and good performance at higher noise levels for SSR, a hybrid sampler has been designed similar to [18] however as it is not realizable with our simple circuit the additional average sampler used there has been left out. The hybrid sampler works as a swept threshold and stochastic resonance sampler at the same time. At every threshold level, multiple

reference pulses get sampled in order to achieve SSR. This combination promises highly accurate sampling with a low-complexity circuit.

4.3 Redesign of the receiver

Based on the concept of the analog solution, the new digital circuit has been designed and simulated. The functionality of is kept the same. First a reference signal gets quantized, propagates through the delay line and per stage one sample of the signal is stored by setting the memristance to a corresponding value. Afterwards the data pulse is transferred through the delay line and correlated with the reference pulse in the same way as it is done on the analog receiver. The resulting output current then corresponds to the correlation result. The principle of the new circuit is shown in (Fig. 4.4).

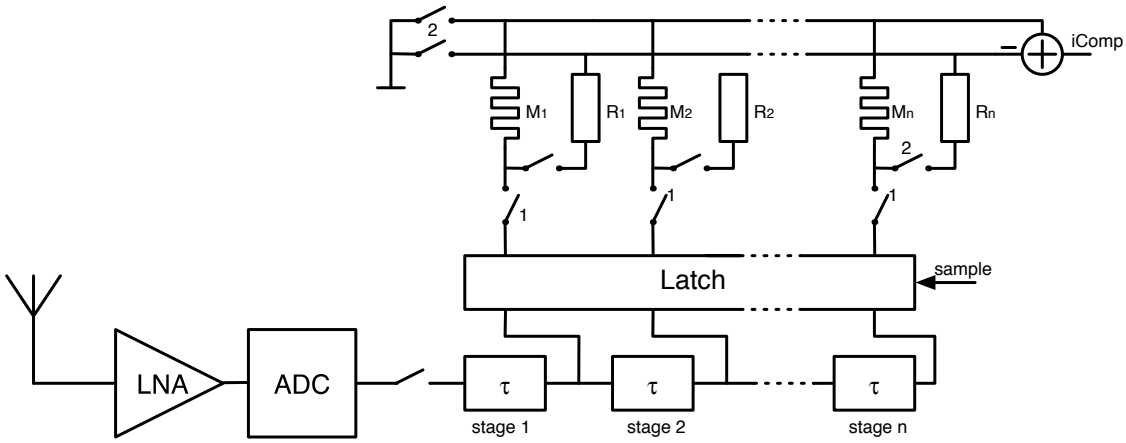


Figure 4.4: Overview over the digital receiver circuit

4.3.1 Analog to Digital Converter

The principle of the analog to digital converter has been adopted from [18] and [19]. An LNA amplifies the signal to simplify quantization. It is followed by a cascade of common source amplifiers serving as a quantizer to generate the digital bit stream. Due to its high bandwidth and its high amplification, a telescopic cascade amplifier has been used as LNA. In order to be able to perform the different types of sampling described in Section 4.2, a level shifter is necessary. A cascade of clipping common source amplifiers with low amplification (around $3-4dB$ per stage) has been chosen as a quantizer because their amplification-bandwidth product is higher as if a simple inverter would have been used. The whole input stage is shown in Fig. 4.5.

4.3.2 Delay Line and Storage

The possibility to use a simple delay line was the main reason to change the analog design and try a new approach. Instead of a complex analog delay line, a simple chain of inverters is used to propagate the signal. As switches, the same switches as in the analog solution are used. The signal level in the delay line is $\pm V_{dd}$ which is good for the setting phase of the memristors. For the convolution phase, however, this high signal amplitude would change the values of the memristors too much and distort the detection. For this reason, an additional resistor is used to divide the current over the memristor by a factor of approximately 10. In the analog solution

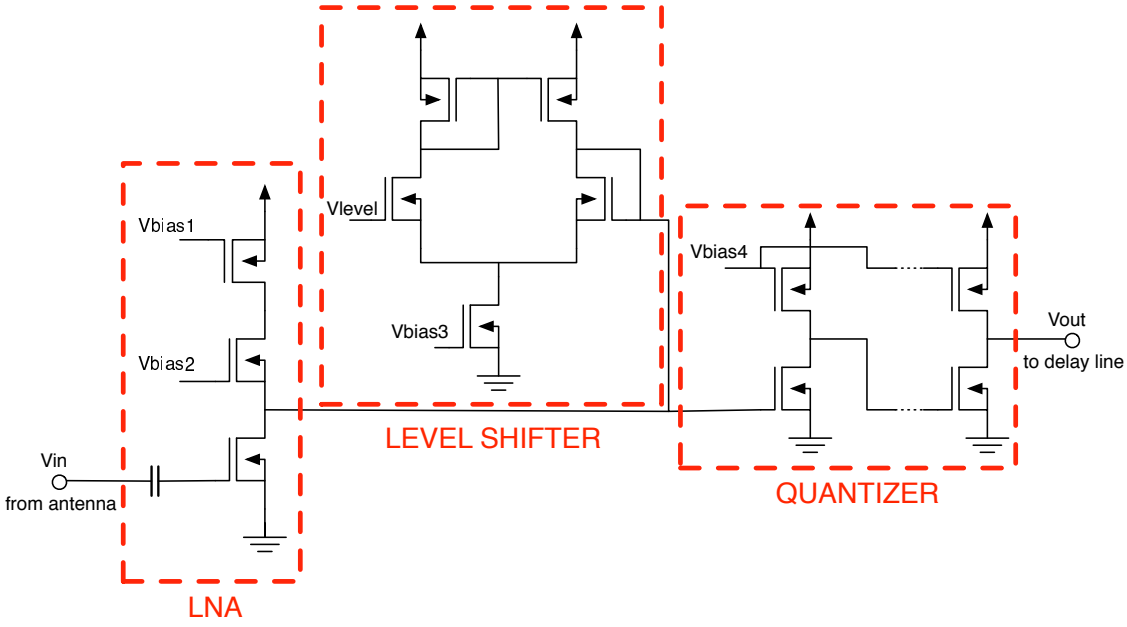


Figure 4.5: The input stage at transistor level

bias resistors have been used to get rid of the offset in the output current 4.1.

$$i_{out}(t) = \frac{1}{R_{off}} \sum_{n=1}^{N} [K v_n(t) v_n(t_0) + (1 + KV_0) v_n(t)]) \tag{4.1}$$

The resistors R have been set to $\frac{R_{off}}{1+KV_0}$. The quantizer in the digital solution uses no offset, so the new value for R is equal to R_{off}. This assumption has been tested in simulations and proven right.

4.3.3 Weighted Correlation

A big drawback in the single-bit A/D conversion is that all samples in a pulse are weighted the same. For example the peak of the pulse is as well set to high as a small peak caused by noise. This makes the performance of the receiver suffer a lot and a detection already at moderate noise levels almost impossible, see Section 4.4. The most obvious solution to overcome this problem would be using a more complex A/D converter. However this is in contradiction to the intention of this implementation so an other solution had to be found. The detection of the polarity of the pulse is done at the estimated maximum of the convolution, where $\tau = 0$. At this point, the two signals (reference and data) are overlapping exactly. In a noisy signal then the area around the peak of the pulse decides whether it is positive or negative. Hence putting emphasis on this area will make detection easier. Two different methods to realize this emphasis have been investigated. The first method was to vary the time delay of the delay stages in a way that where the peak of the pulse is stored the delay is shorter and so the sampling rate higher and lower in the other areas. The second method was to introduce a weight function before calculation the correlation sum by adding up the currents over the memristors. Again the area around the pulse peak gets more weight than the rest of the samples. Equation 4.2 shows the new calculation of

the convolution sum.

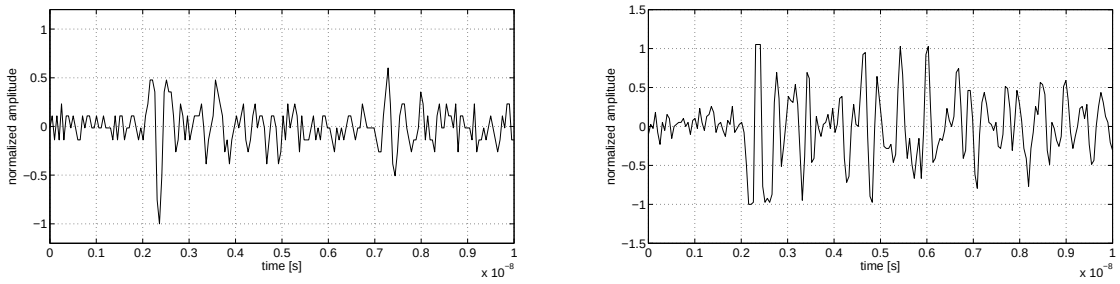
$$\Phi_{v(t_0),v(t)}(t) = \sum_{n=1}^{N} (v_n(t_0)v_n(t))w(n) \tag{4.2}$$

where $w(n)$ can be any weight function with the maximum at the peak of the pulse. Simulations have shown that a Gaussian curve with a standard derivation of about half the stages has performed best.

4.4 Results

4.4.1 Numeric Test

As a first step it should be shown that the concepts presented in Section 4.2 are suitable for the UWB pulse stream. For evaluation, the same test signal as for the analog receiver has been used. First the reference pulse was sampled with the hybrid sampling method at a sampling rate of $20Gs/s$ and then correlated to the sampled data pulse. Fig. 4.6 shows the sampled pulses with swept threshold and SSR sampling methods at a signal to noise ratio of $+20dB$ at the input while Fig. 4.7 shows the result of the swept threshold and SSR at a SNR of $3dB$ at the input. For stochastic resonance 100 pulses have been used while for swept threshold sampling, 16 thresholds have been sampled. For a better comparability, the amplitudes sampled signals have been normalized.



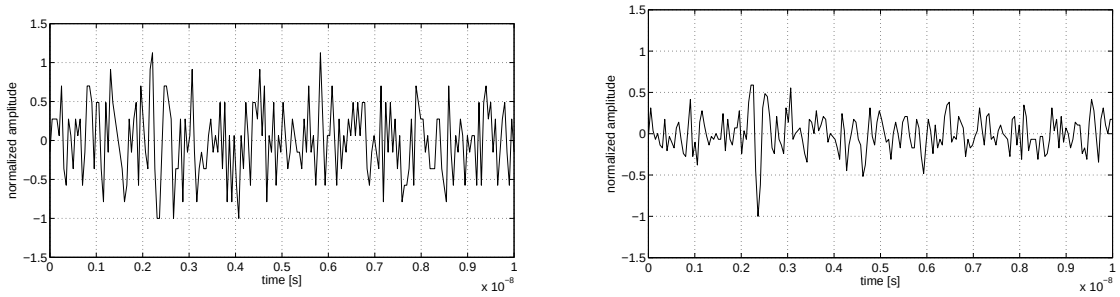
(a) (b)

Figure 4.6: Sampling result of the swept threshold sampler (a) and the stochastic resonance sampler (b) at a noise level of $20dB$

As expected, the swept threshold sampling works better for low noise levels and SSR better for higher noise levels of the input signal. To prove that, the quality of sampling has been measured over increasing SNR of the test signal. Fig. 4.8 shows the calculated similarity of the sampling result over increasing SNR. Both samplers contribute to an increasing performance at all noise levels. The swept threshold sampler contributes more at low noise levels and the SSR sampler more at high noise levels.

In contrast to the reference pulse, the data pulses are sampled only once. The reason for this are first the high costs in sense of circuit complexity which is would be needed to store the intermediate results and second the severe decrease of detection speed if every data pulse has to be sent several times.

The basic bit error rate simulation (Fig. 4.9) shows a very good result for the hybrid sampling. The bit error rate is higher than the ideal result, but should be sufficient for an implementation,



(a) (b)

Figure 4.7: Sampling result of the swept threshold sampler (a) and the stochastic resonance sampler (b) at a noise level of 3dB

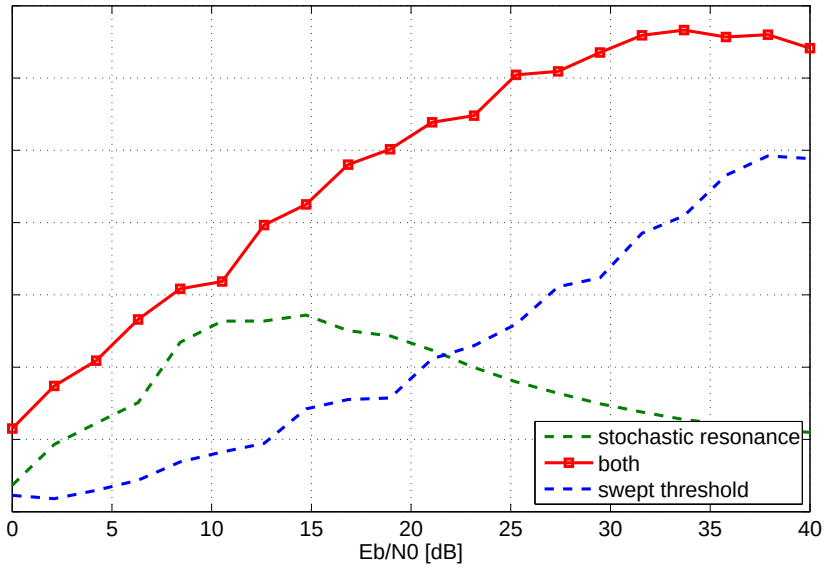


Figure 4.8: performance of the two different sampling schemes and the combination of both

while the single sampling of the reference pulse requires a very high E_b/N_0, that the bit-error rate is sufficiently low. This shows, that good detection of the reference signal, especially at a high E_b/N_0 at the input is very important.

4.4.2 Circuit Test

After the first simulations have been successful, a circuit simulation has been set up. Due to the high simulation effort, a MATLAB simulation with an ideal delay line has been used. Two different reference receiving methods have been investigated.

- simple reference sampling with only one reference pulse.
- hybrid reference sampling as described above with 160 reference symbols (16 levels with 10 pulses each). The number is considered to be a good tradeoff between performance improvement and accuracy.

Both methods have been tested with two different numbers of stages. 200 stages resulting in a sampling interval of $50ps$ and 500 stages resulting in a sampling interval of $20ps$. The higher

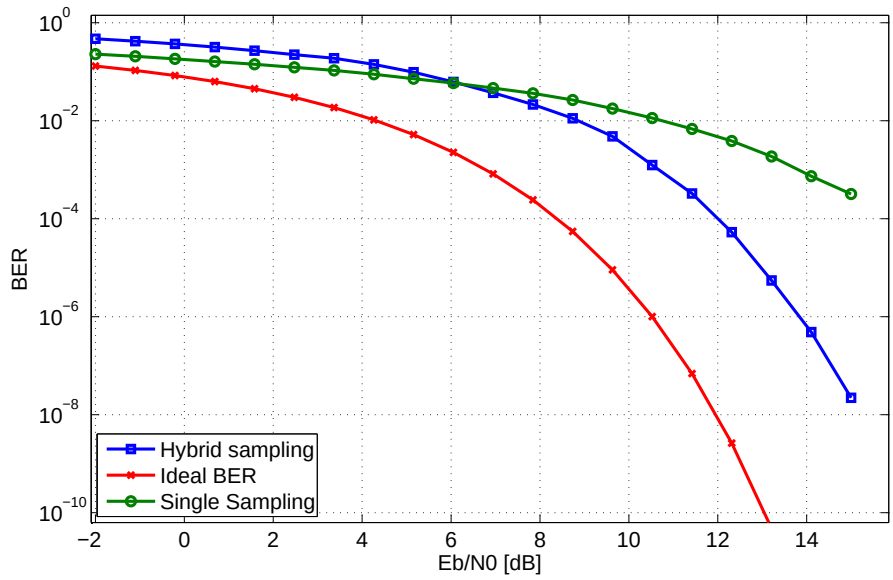


Figure 4.9: result of the numeric calculations of both sampling methods

sampling rate is supposed to improve the tolerance against noise. Wrong quantized samples, caused by noise, should equal each other out better when the correlation sum is calculated. In addition weighted correlation has been combined with the two best performing setups to see if it can improve the result.

In order to estimate the performance of the different receiving methods, a bit-error rate simulation has been done with all possible combinations of sampling intervals, reference methods and weighted correlations for the hybrid sampler. If possible the number of bits that are detected wrong is counted, otherwise the bit-error rate estimation is done using the Q function. When conducted several times, the results of the simulations show a high variance and seem to be very dependent on the input signal. The presented results show a mean value of multiple simulations to enable a meaningful interpretation of the results.

As it has been expected from the first simulations, there is a measurable difference in performance, if the receiver gets programmed only with one reference pulse (Fig. 4.10) or when it gets programmed with many reference pulses (Fig. 4.11). In the case the signal has a high E_b/N_0, both receivers show acceptable performance. However only the multi-sampling version can keep up the good performance when the noise becomes stronger. Even at an E_b/N_0 of less than $6dB$ the bit error rate stays around 2%. Remarkable is that for the single reference receiver, it does not matter if a sampling interval of 20ps or 50ps has been chosen.

For weighted correlation, a Gaussian curve with the mean at the estimated peak of the pulse and a standard derivation of $\frac{\#stages}{10}$ has been chosen. The method of weighted correlations can improve the detection with the drawback, that the peak of the pulse has to be in the right position.

4.4.3 Comparison With the Analog Solution

In this section the properties of the two different approaches for a memristor receiver are compared first by summing up some of the inherent properties of each solution and second by comparing the bit-error rate which complies with the system's performance.

The drawbacks of the analog receiver have been the reason for thinking about a digital solution. First of all the delay line is very complex and uses many inductors, which is not very suitable for

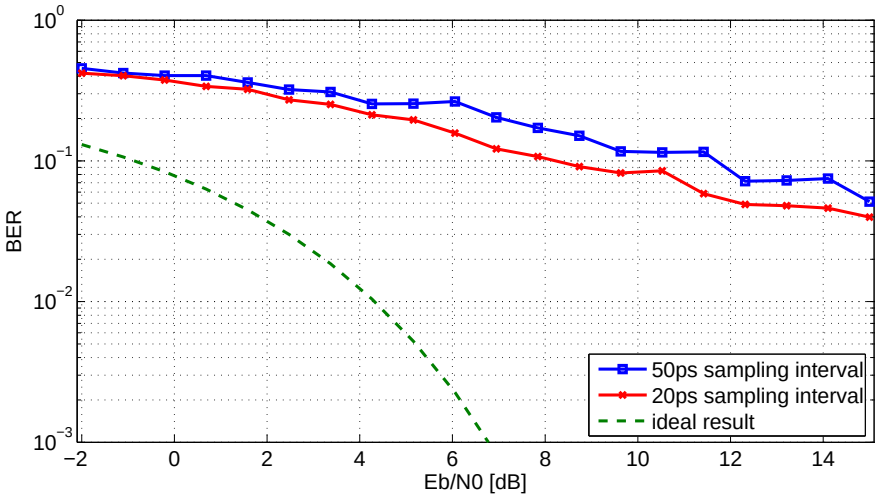


Figure 4.10: Bit-error rate with single reference sampling

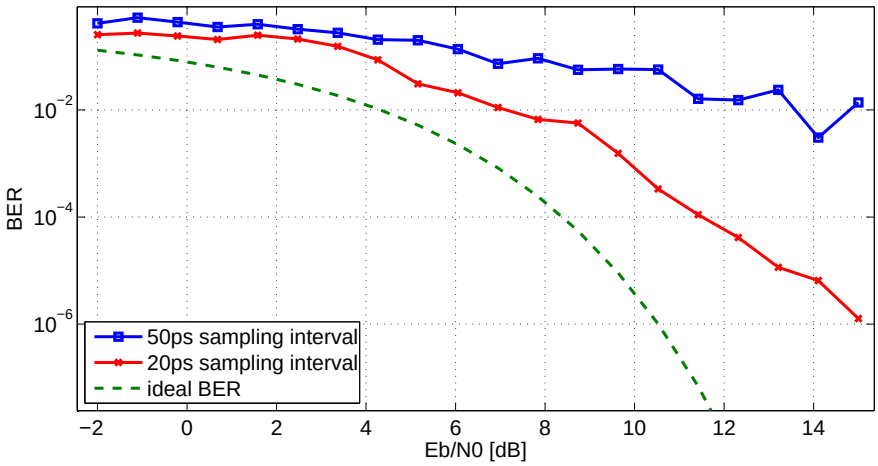


Figure 4.11: Bit-error rate with hybrid-multi reference sampling

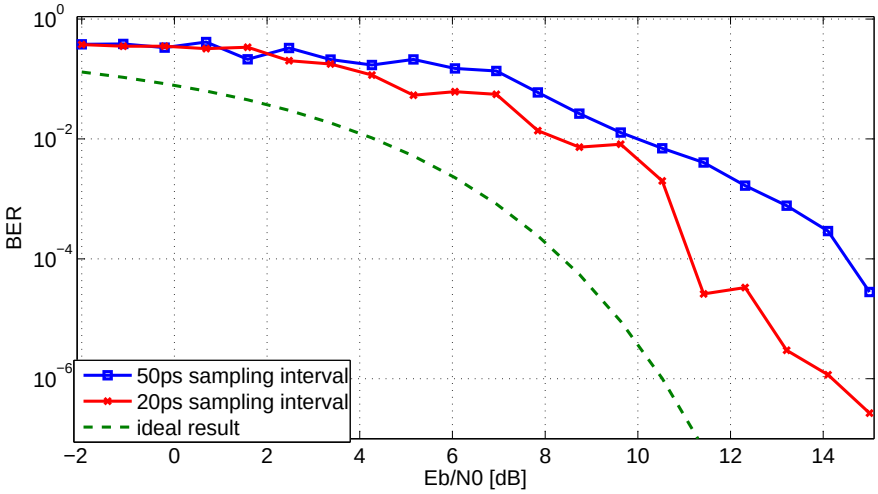


Figure 4.12: Bit-error rate with hybrid-multi reference sampling and weighted correlation

integrated circuits. Furthermore the analog ultra-wide-band signal is susceptible to distortions while being detected. Another drawback is, as said before, the fact that the analog receiver only gives discrete output pulses without any possibility to verify, if this pulses are really the maximum of the correlation.

The digital receiver in contrast provides a continuous output current, offering the possibility to use time synchronization algorithms, as early-late tracking [20] for instance, which is important due to the high requirements of the detection on timing, Another advantage of this receiver is the possibility of using memristors with a lower dopant drift velocity. In the simulations presented above, a drift velocity of $10^{-8}m^2V^{-1}s^{-1}$ has been used, which is quite high. However, this is necessary to set the memristance properly with the little charge stored in the capacitors of the delay line. The inverter delay line in contrast is capable of providing an extensively larger amount of charge.

Despite all advantages, also the digital solution is not ideal. The biggest disadvantage is the large amount of reference symbols that is required to compensate the inaccurate quantization. Furthermore double as many sampling stages are necessary to achieve a good performance. In a quickly fading channel that makes reprogramming frequently necessary, this means a serious decrease of the data rate. Tab. 4.1 summarizes the major advantages and drawbacks of the two concepts

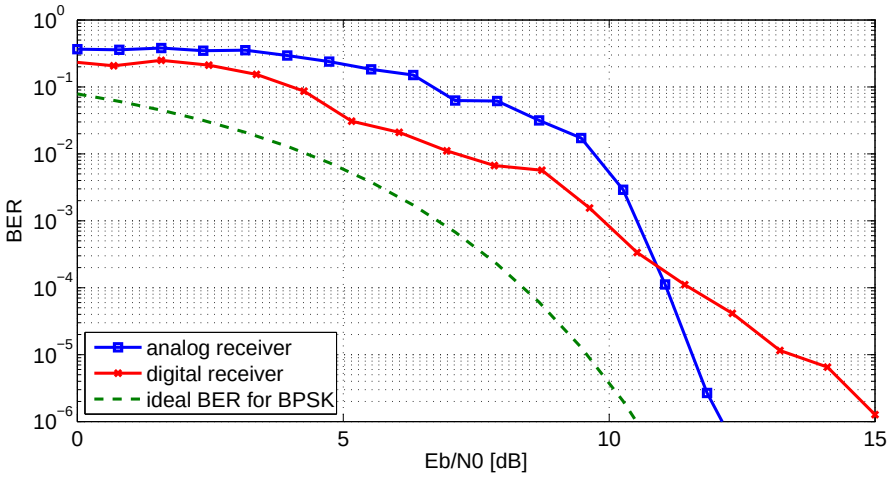


Figure 4.13: Comparison of the analog and the best digital version

The superior performance at low and moderate noise levels speaks for the analog solution, while at high noise levels the qualities of the stochastic resonance sampler, which is able to filter a lot of noise, comes into play (Fig. 4.13).

name	analog	digital
BER	better at low & moderate noise	better at high noise
output	pulsed	continuous
reference receiving	fast & simple	slow
circuit complexity	very high	moderate
required drift velocity	high	low

Table 4.1: Advantages and disadvantages of the two concepts

5 Discussion and Outlook

In this work the potential of a practical realization of a memristor-based auto-correlation receiver has been investigated. The aim was to present different approaches how to make use of the properties of the memristor in such a receiver. This chapter provides a summary of the achieved results and an outlook to possible further work.

5.1 Conclusion

The available model of the receiver left open questions concerning essential building blocks. As a first step this model has been analyzed to find the critical components which turned out to be, aside the memristors, the switches and the analog delay line. Therefore the focus had been set on those components.
Good isolation and little insertion loss were the important parameters for the switches. Beside that good high frequency behavior and simplicity were essential. Both investigated concepts first a MOS transistor and a diode-based switch provided good results. However the MOST switch has its drawback in the low isolation at high frequencies and the diode switch suffers from high power consumption. Both concepts are suitable but not optimal for this task.
The next element of the receiver that has been investigated was the analog delay line. The original circuit, using a passive LC delay line, only works in the ideal case. Three possible solutions to compensate the losses have been presented. The first one is the use of amplifier stages within the delay line. In the used technology, the designed amplifiers are of the limit of the possible bandwidth. Furthermore this concept requires a very precise fitting of the amplifier stages, which is not really possible in practical use. The second idea dismisses the whole delay line and suggests a stack of sample-and-hold elements. The results of this solution are better than the results before but short pulse durations of the control signal cause problems. The third proposal was the combination of the two solutions presented first in order to avoid their drawbacks.
In the second part of the thesis a digital version of the receiver has been presented and analyzed. It had been shown that the concept is able to perform similarly to the analog solution. A combination of swept threshold and stochastic resonance has been able to sample the reference pulse even though the noise level has been very high. A possible circuit design for the analog-to-digital converter has been presented as well as a concept for the full receiving system. At the end of the work, a comparison between the analog receiver and the digital concept has been made,

showing that the digital solution performs almost equally while having a more robust circuit design.

5.2 Outlook

This work shows possible solutions for a memristor receiver, rather than presenting a final circuit layout. Apart from the fact that real memristors are not available for experimenting yet, there are several more problems to be solved on the way to a physical realization of such a receiver. A full system simulation on circuit level as well for the analog as for the digital receiver is necessary to find out how the system parts play together. All the presented solutions are not dedicated to a direct implementation. Especially the semiconductor technologies, used for the analog circuits is on the limit regarding the available bandwidth. Different semiconductor technologies could help to overcome this limitation.

Furthermore the peripherals of the receiver, the antenna, a sampler for the correlation result and a control circuitry for the switches have to be designed. In connection to that further work on the long time stability, meaning variations in the timing of the control signals and how the receiver reacts on a fading channel, would be interesting.

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